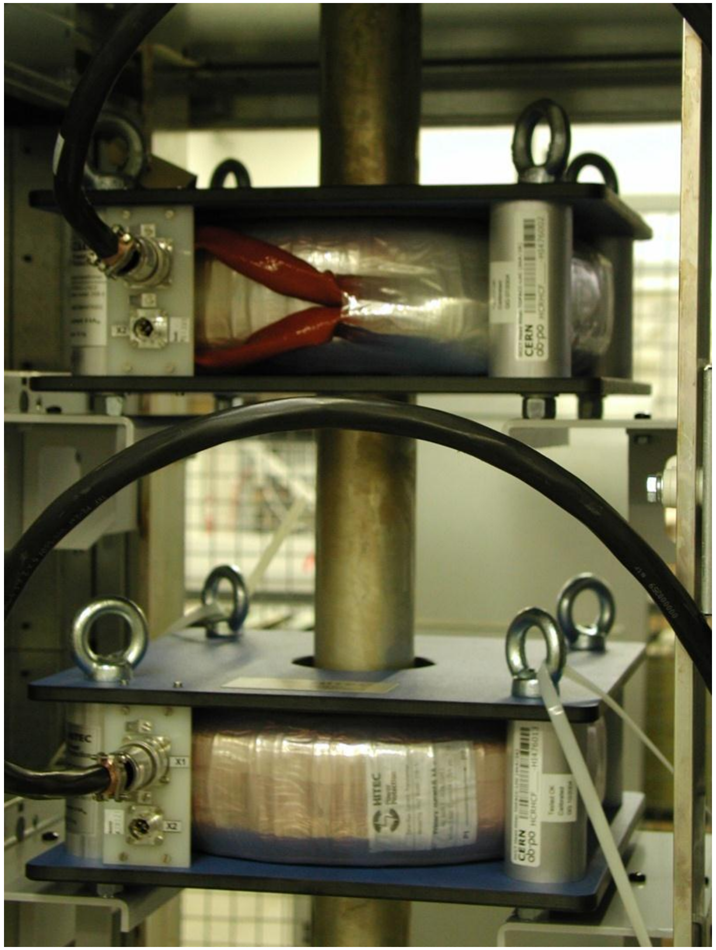
CURRENT MEASUREMENT FOR POWER CONVERTERS

- TUTORIAL -



POCPA Conference

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- **Review of current measurement devices**
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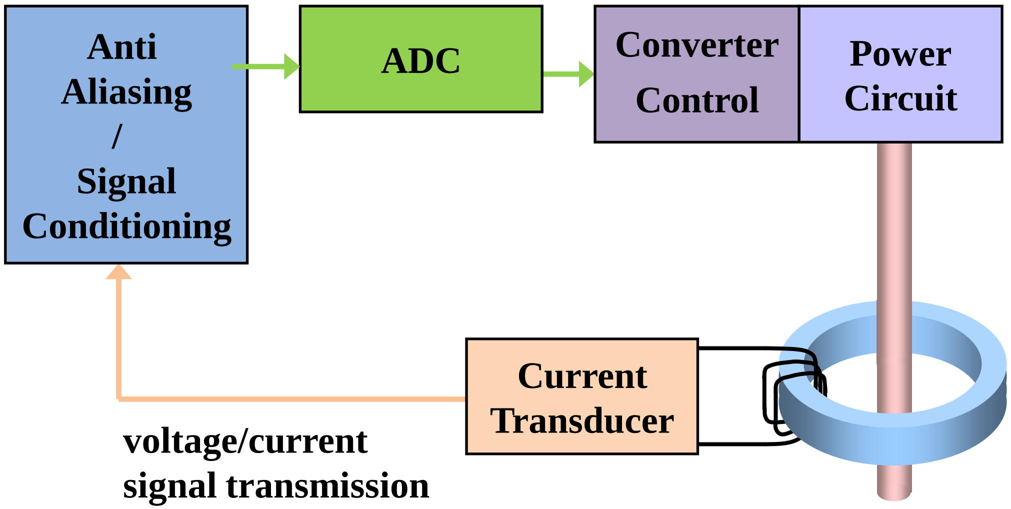
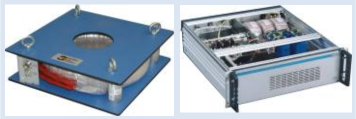
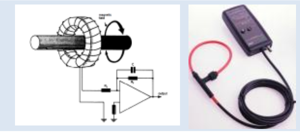
- **Signal conditioning and anti-alias filtering**
- **Precision components (Voltage references, network resistors and op-amps)**
- **ADC choices (SAR/ΔΣ)**
- **Temperature coefficient and compensation**
- **Powering, PCB layout**

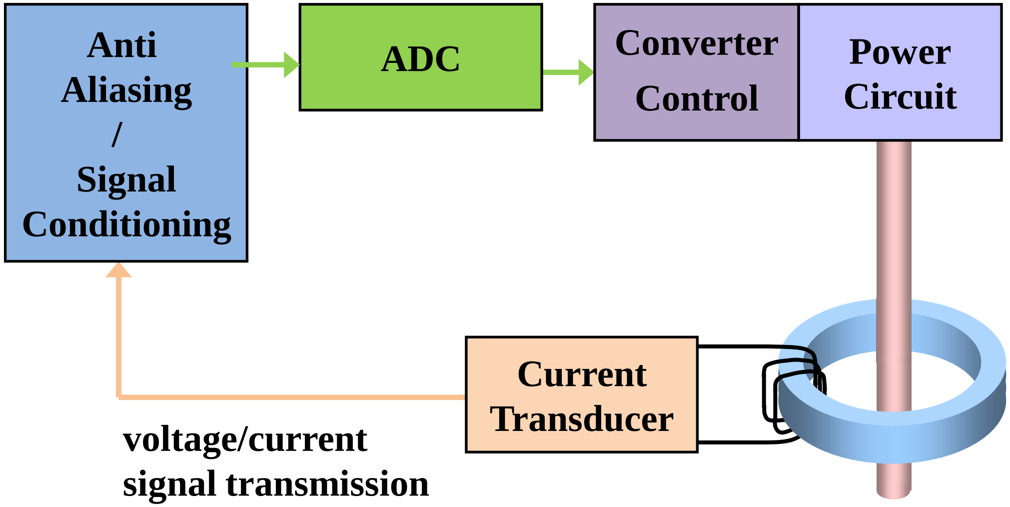
- **Power converter current loop with digital control**



CURRENT MEASUREMENT TECHNOLOGIES

	DCCTs	Hall effect	CTs	Rogowsky	Shunts
					
Principle	Zero flux detection	Hall effect	Faraday's law	Faraday's law	Ohm's law
Output	Voltage or current	Voltage or current	Voltage	Voltage	Voltage
Accuracy	Best devices can reach a few ppm stability and repeatability	Best devices can reach 0.1%	Typically not better than 1%	Typically %, better possible with digital integrators	Can reach a few ppm for low currents, <% for high currents
Ranges	50A to 20kA	hundreds mA to tens of kA	50A to 20kA	high currents possible, up to 100kA	From <mA up to to several kA
Bandwidth	DC ..kHz for the higher currents, DC..100kHz for lower currents	DC up to couple hundred kHz	Typically 50Hz up to a few hudreds of kHz	Few Hz possible, up to the MHz	Up to some hundreds of kHz with coaxial assemblies
Isolation	Yes	Yes	Yes	Yes	No
Error sources	**Magnetic** (remanence, external fields, centering) **Burden resistor** (thermal settling, stability, linearity, tempco) **Output amplifier** (stability, noise, CMR, tempco)	**Magnetic** **Burden resistor** **Output amplifier** **Hall sensor stability** (tempco, piezoelectric effect)	**Magnetic** (remanence, external fields, centering, magnetizing current) **Burden resistor**	**Magnetic** **Integrator** (offset stability, linearity, tempco)	Power coefficient, tempco, ageing, thermal voltages

SIGNAL TRANSMISSION



SIGNAL TRANSMISSION

Noise Source → Coupling Channel → Receptor (DCCT, cable, acq. electronics)

Methods of noise coupling:

- Conductive coupling
- Common impedance coupling
- Capacitive and inductive coupling

The main aspects to be considered in a mitigation strategy are:

- Grounding
- Cabling and shielding
- Circuit impedance level
- Isolation, filtering, balancing

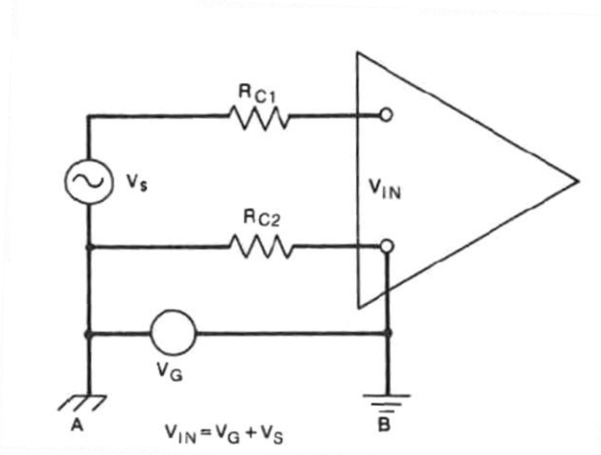
First Rule: Equipotentiality of reference GND ! (in frequency as well as in DC)

- Electronic chassis: use conductive surfaces on chassis and ground planes on PCBs
- Racks – use conductive surfaces and the rack structure for equipotentiality
- Between racks – ensure "solid", non inductive ground connections

Common mode noise

Non perfect grounds often translate into common mode noise problems.

CMV couples into a circuit if grounded at more than one point. The coupling can happen via a noise current flowing through a **common impedance** or by **induction** of a noise voltage in the ground loop.



Some well known mitigation methods are:

- **Single ground systems** (float source or receiver)
- **Open ground loop** (CM chokes, transformers, optos, isolation amplifiers)
- **Common mode filtering**
- **Balanced transmission/differential amplifiers**
- **Guarded amplifiers**

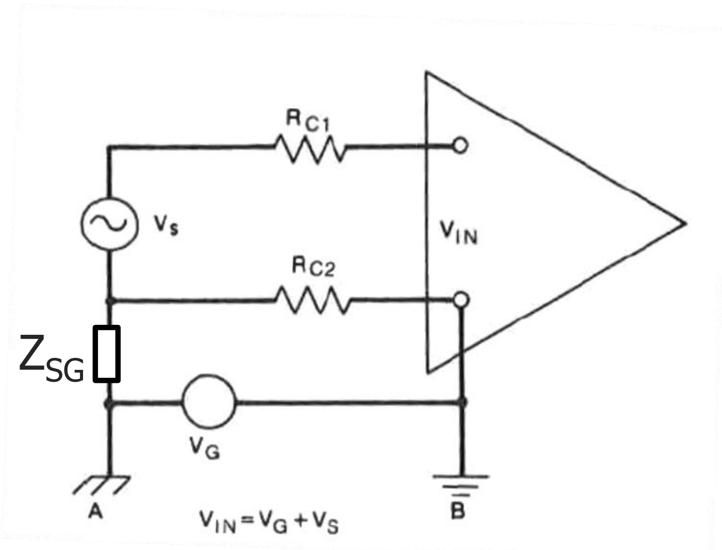
- **Single ground point**

Z_{SG} is the isolation impedance

If Z_{SG} is high then I_{c2} is strongly reduced.

Shielding reduces the capacitive nature of Z_{SG}.

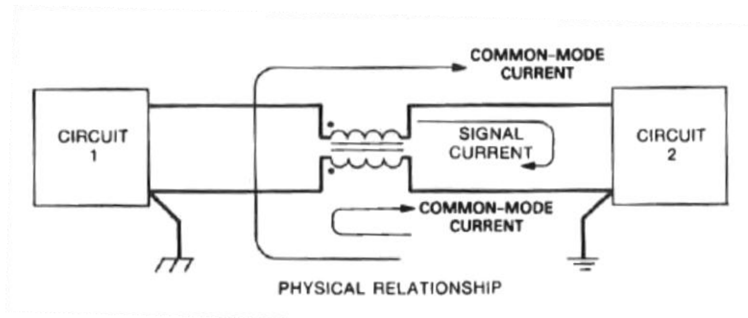
Often not possible to float the source.

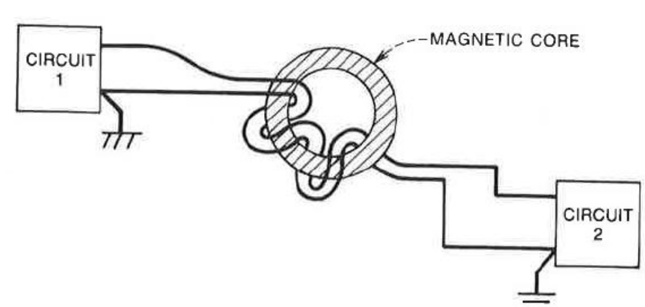


- **Common mode chokes**

CM currents generate a non cancelling flux in the choke.

In practice, due to physical limitations such as limited permeability and number of turns, common mode chokes provide only moderate attenuation to CM noise.

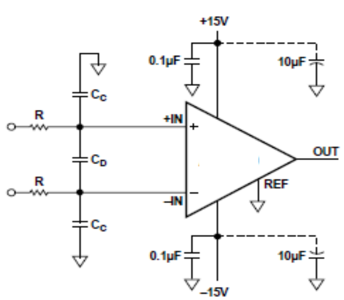




- ## CM filtering

Attenuation of HF common mode at frequencies where the receiver amplifier circuit has limited or no common mode rejection.

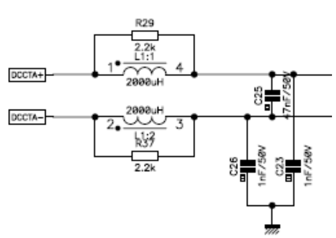
Passive filters (LC or RC) are commonly used. An example of an RF filter for an instrumentation amplifier is shown below.



$$FilterFreq_{DIFF} = \frac{1}{2\pi R(2C_D + C_C)}$$

$$FilterFreq_{CM} = \frac{1}{2\pi RC_C}$$

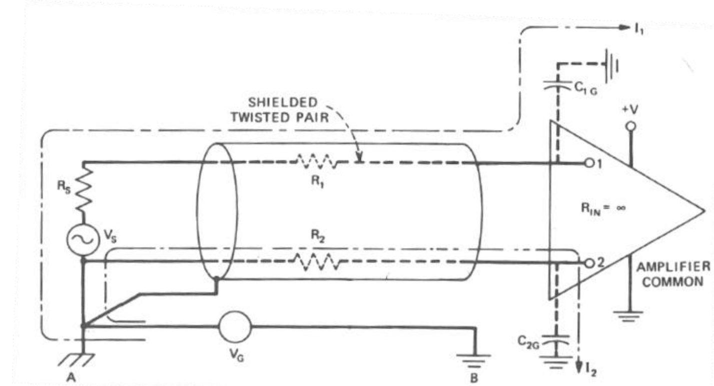
where $C_D \geq 10\, C_C$.

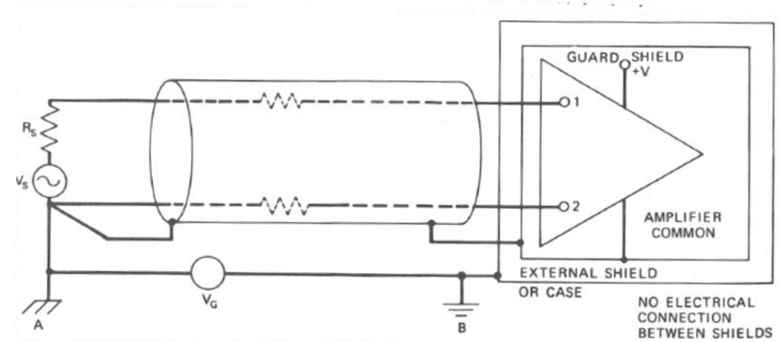


- ## Guarded amplifiers

The guard shield works in conjunction with a floating receiver and a shielded cable to reduce capacitive coupled common mode noise.

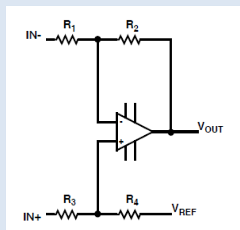
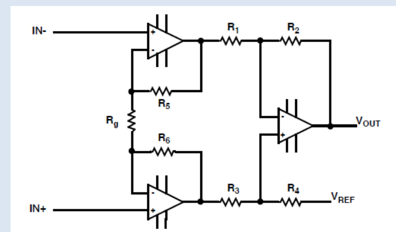
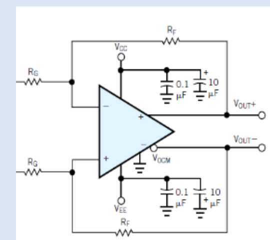
Without the guard, CM noise would flow from A back to B through R1 and R2.

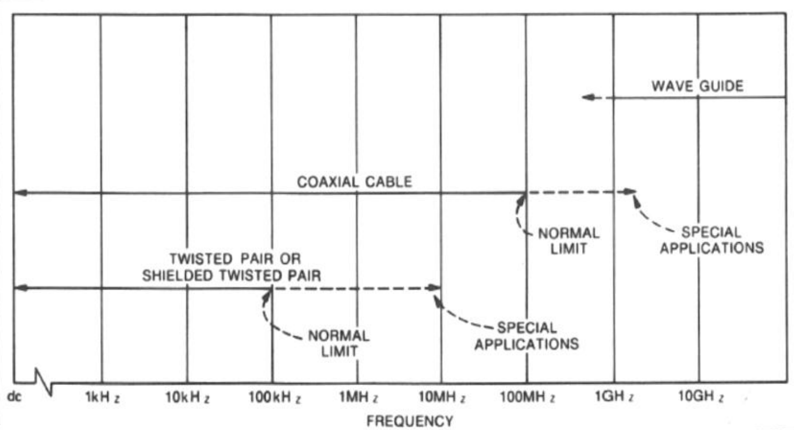




- **Differential/balanced inputs**

Different types of differential input circuits can be used:

	Difference amplifier	Instrumentation amplifier	Fully differential amplifier
Circuit			
Input impedance	**kΩ range** – depends on gain resistors, which can't be too high to limit noise	**High** – corresponds to the input impedance of the buffer amplifiers	**kΩ range** – depends on the gain resistors, which can't be too high to limit noise
CMR	**Depends on matching** between gain resistor ratios ! Matched networks often used	**High**, at least in the case of integrated instrumentation amplifiers	**Depends on matching** between gain resistor ratios ! Matched networks often used
ADC signal conditioning	Easy level adapting for ADC inputs	Easy level adapting for ADC inputs	Well suited for driving differential ADC inputs and transmission lines. Easy level adapting and anti alias filtering
Other	-	Needs return path for the bias current in case of floating source.	-



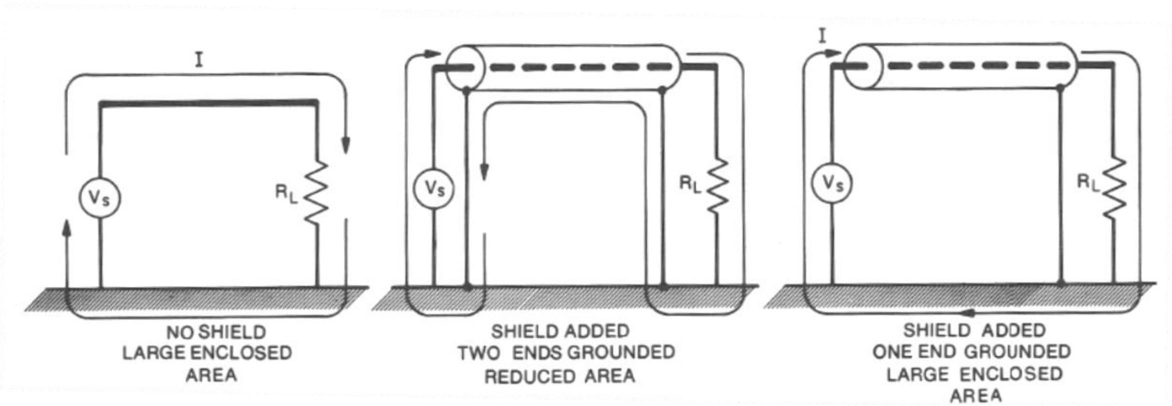
- **Coaxial vs Shielded twisted pair**

  STP: preferred below 100kHz. Shield is not a signal conductor.

  Coaxial: more uniform characteristic impedance, lower losses. Shield is part of signal path, so noise currents should not be allowed to flow. For high frequencies, skin effect makes it behave like a triax.

- **Where and how should shields be grounded ?** The answer depends on:
  - Type of cable (Coaxial or STP)
  - Frequency range of the transmitted signal and noise voltages
  - Nature of the noise coupling (capacitive or magnetic?)
  - Circuit impedances (source and receiver floating or grounded?)

- A grounded shield **protects against capacitive coupling**. If large CMVs are present a shield grounded on both sides will conduct a noise current that can couple with the inner conductors.
- Copper shields provide no magnetic shielding. The best way to shield against magnetic coupling is to **reduce the surface of the signal loop** -> twisted pair cables. Use coaxial for frequencies where the signal current returns via the shield and not through ground (f > 5 fshield_cutoff).
- In low level systems grounded at both ends where magnetic fields are present, the **surface of the ground loop** (LO to GND) must also be minimized.



Shielded twisted pair

- Where **power frequency common mode voltages are present**, and the signal being transmitted is a low level, low frequency voltage signal, the shield should be grounded on **one side only** (receiver end).

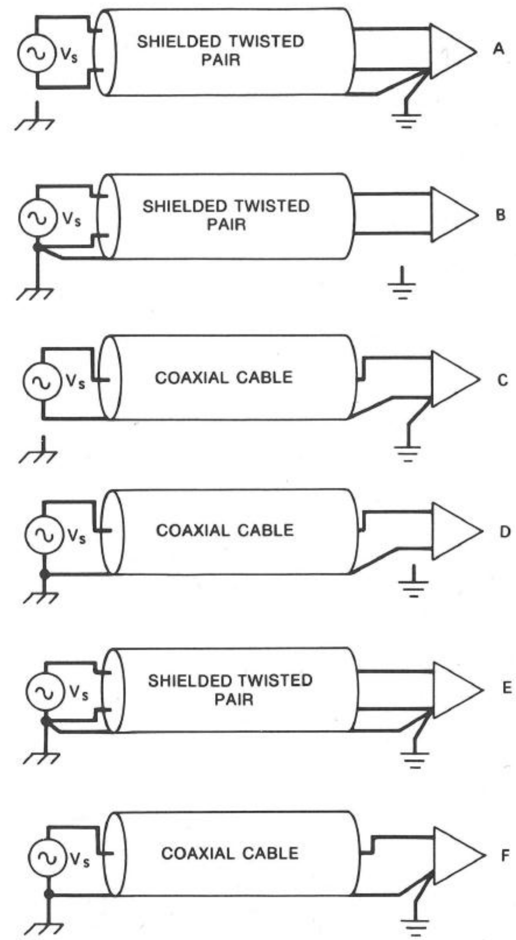
- If either the source or the load are floating the shield should be grounded at **one side only** as shown in A and B (except for the case of a guard shield).

- **For all other cases**, shields should be grounded on **both sides** (E).

Coaxial cable

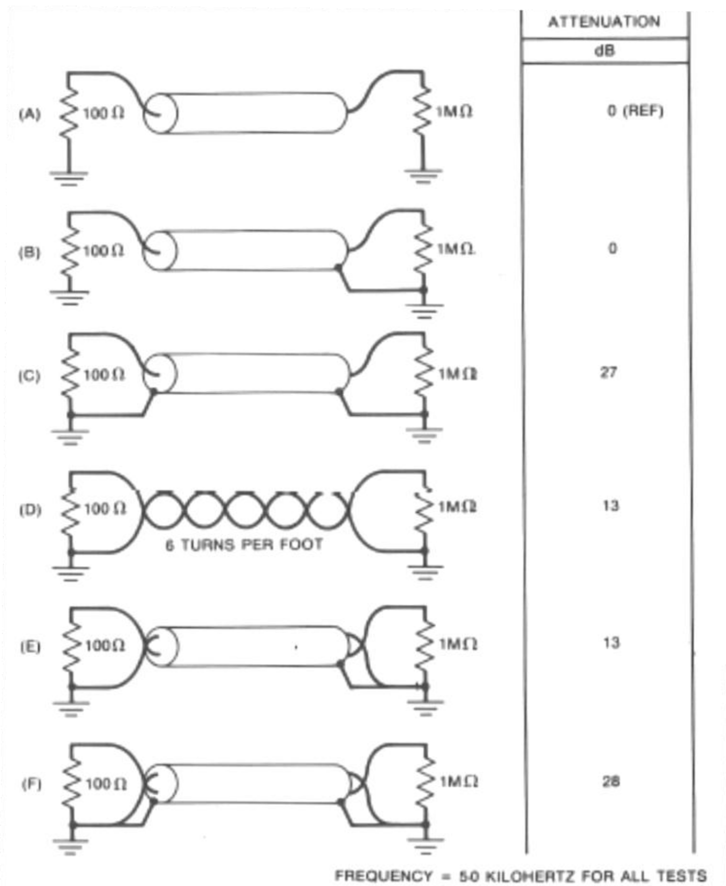
- If either the source or the load are floating the shield should only be grounded at **one side only** (C,D).

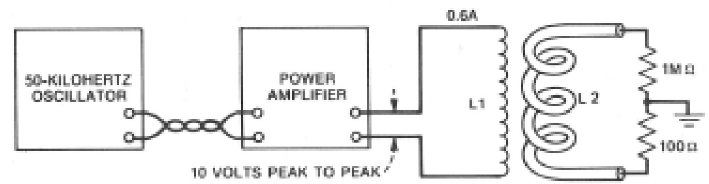
- **For all other cases**, shields should be grounded on **both sides** (F).

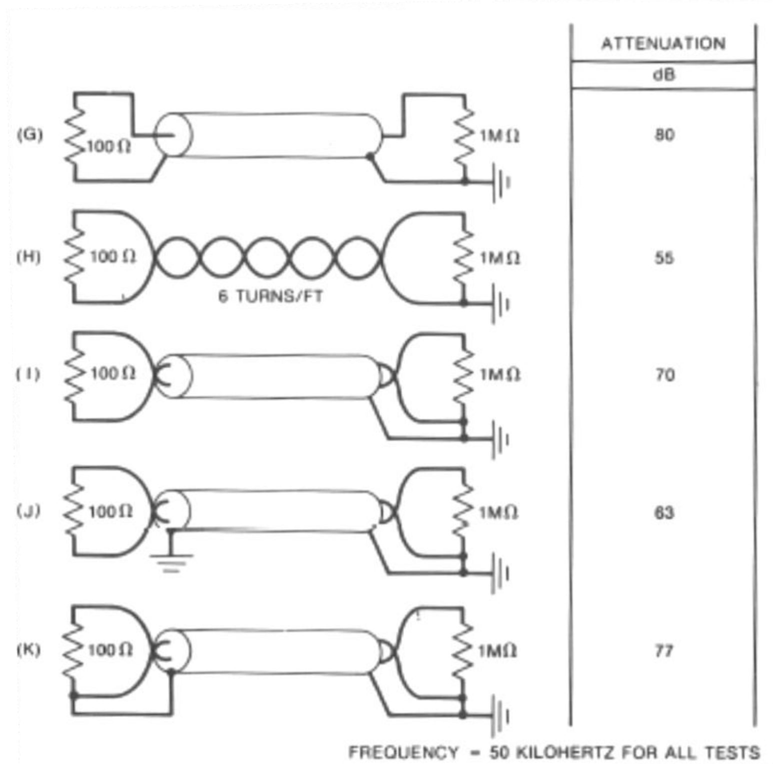


Preferred grounded schemes for shielded, twisted pairs and coaxial cable

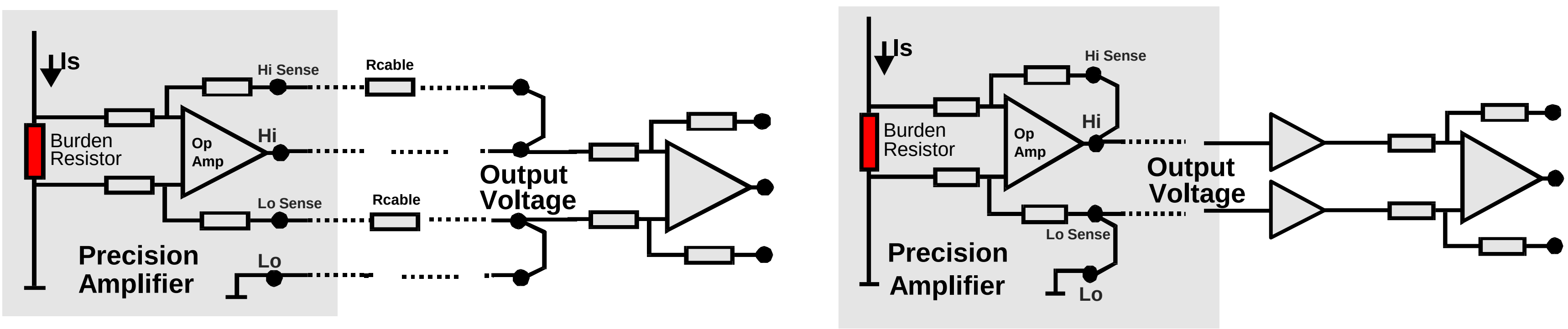
Example reflecting some of the concepts discussed before (Single ground, type of cable, shielding):







➢ **Current transducer output** – remote sensing ?

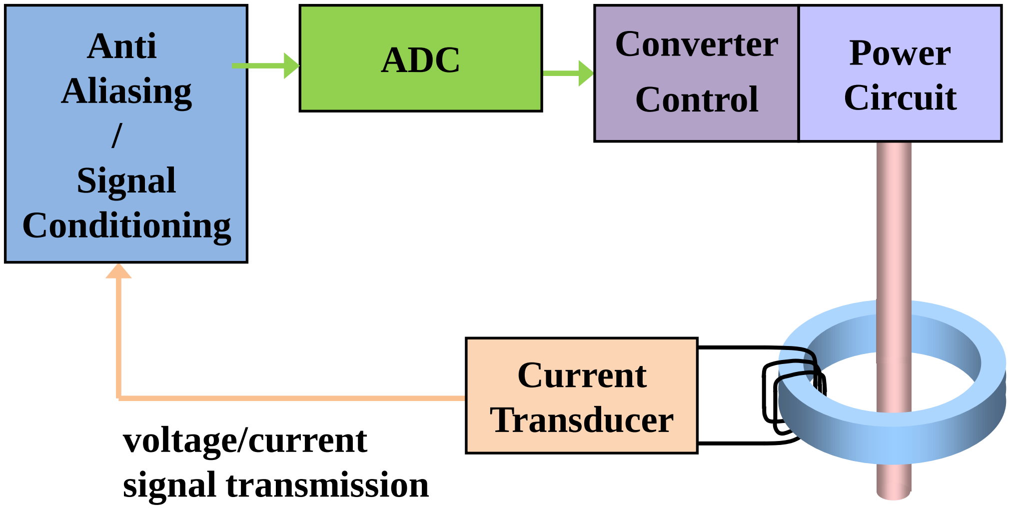


- DCCT outputs are often available in **4 wire** for remote sensing.

  \+ Eliminates error due to voltage drop in the cable

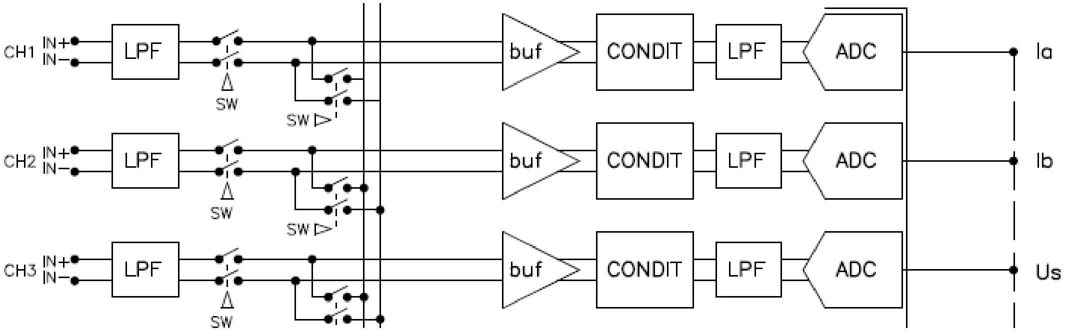
  \- Gain of the differential amplifier becomes dependent of cable impedance

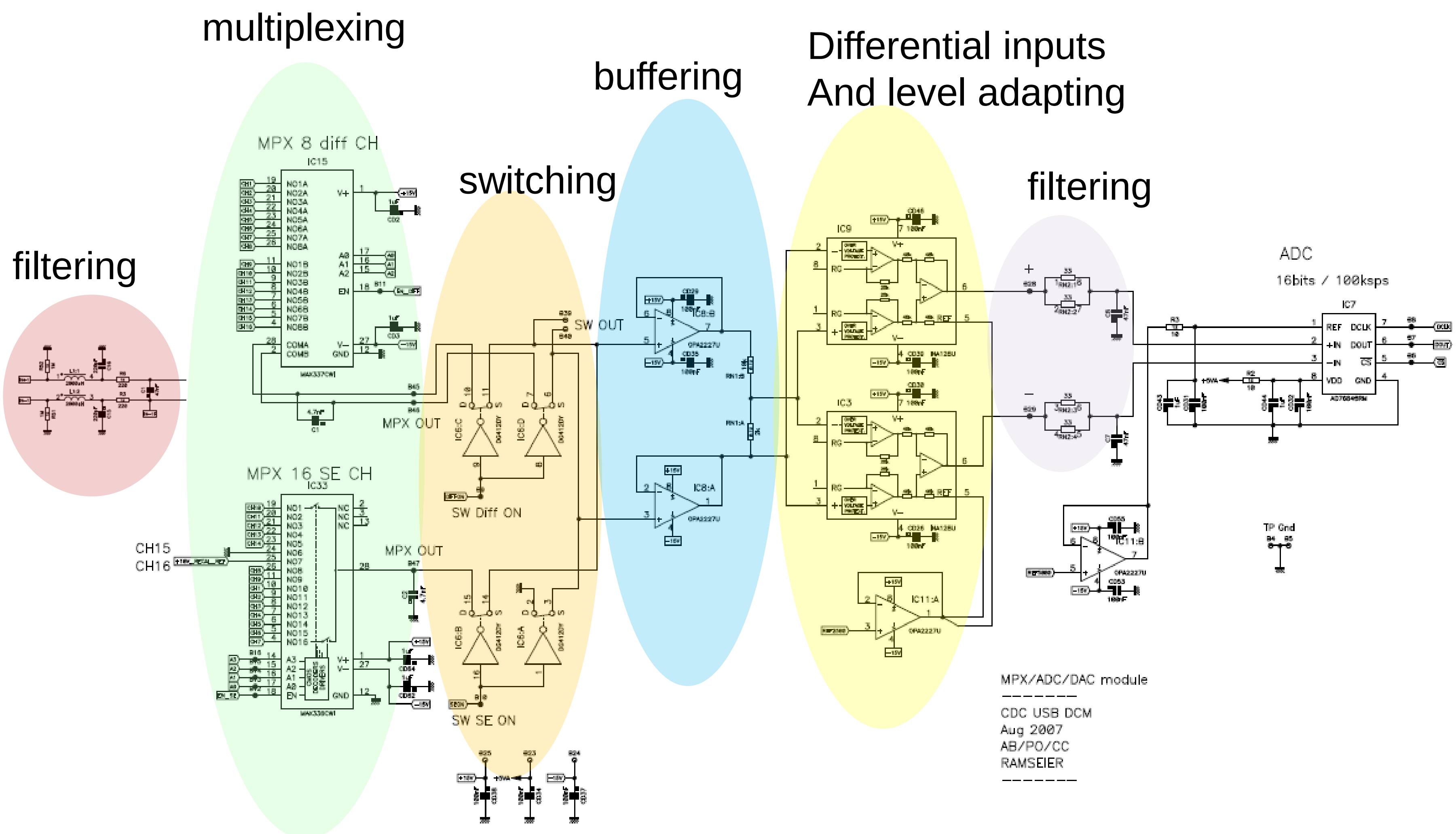
- A **two wire** transmission with a high impedance differential input at the receiver end gives good results. The differential input provides the required CMR.


Anti
Aliasing
/
Signal
Conditioning
ADC
Converter
Control
Power
Circuit
Current
Transducer
voltage/current
signal transmission

➤ The functions to be performed by the **signal conditioning circuits** derive from the nature of both the signal and the receiver and may comprise:

- **Current to voltage conversion** (not covered here)
- **Filtering: CM and series** (discussed in previous section)
- **Multiplexing/switching**
- **Buffering/ impedance adapting**
- **Differential input**
- **Level adaptation**
- **Anti Alias filtering**




multiplexing
buffering
Differential inputs
And level adapting
switching
filtering
filtering
MPX 8 diff CH
IC15
MPX 16 SE CH
IC33
CH15
CH16
MPX OUT
MPX OUT
SW OUT
SW Diff ON
SW SE ON
IC8:B
IC8:A
OPA2227U
IC9
IC3
INA128U
IC11:A
ADC
16bits / 100ksps
IC7
REF
+IN
−IN
VDD
DCLK
DOUT
GND
TP Gnd
MPX/ADC/DAC module
CDC USB DCM
Aug 2007
AB/PO/CC
RAMSEIER

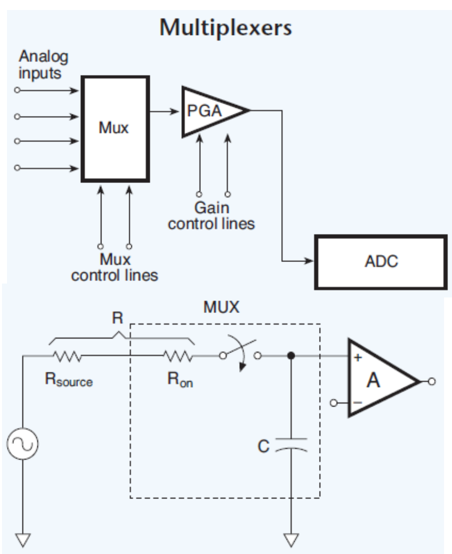
SIGNAL CONDITIONING

Multiplexing/switching

Use high impedance inputs to eliminate errors due to mux's ON resistance.

Cross talk and settling time might occur due to source impedance combined with mux's stray capacitance.

Low source impedance also minimizes effect of charge injection from the multiplexer.

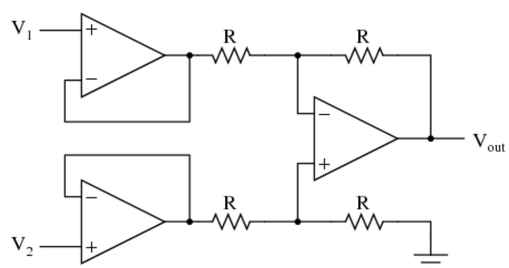


Buffering/ impedance adapting

Z_{Source} and $Z_{receiver}$ form voltage divider. Buffering ensures $Z_{receiver}$ is large, maximizing the voltage signal at the receiver input.

Buffers are used in combination with differential amplifiers to create balanced inputs.

Unity gain amplifiers are sensitive to capacitive loads – particular important if dynamics is an issue

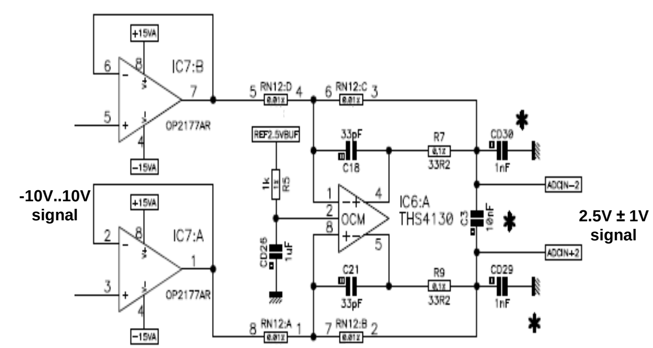


Level adapting

Attenuation or amplification of a voltage signal using voltage dividers and op amp circuits.

Level shifting, in particular for ADCs with differential inputs.

On fully diff amplifiers the Vocm pin allows the output CMV to be adjusted for precision level shifting.



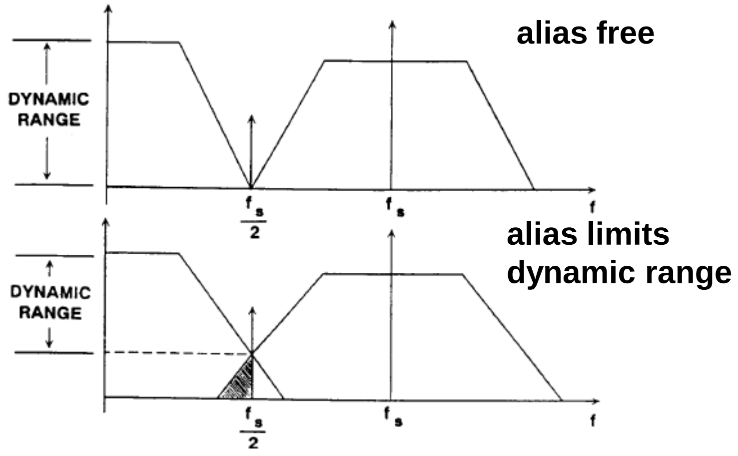
The **anti-alias** requirements/strategy depend on the sampling strategy:

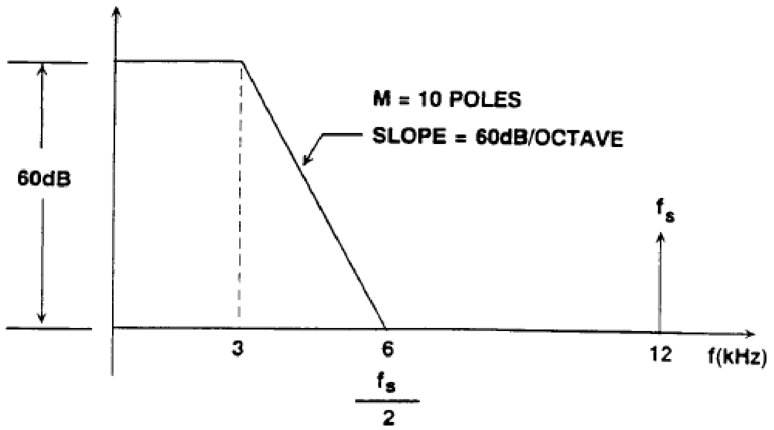
- **Nyquist-Shannon sampling**: $f_{sampling} > 2.f_{max.signal}$

The anti-alias filter must provide appropriate attenuation above F_{max}.

Cutoff frequency and filter order depend on desired dynamic range.

Below we can see the effect of aliasing on dynamic range. On the right we see the response of a 10th order anti alias filter designed to achieve 60dB dynamic of range for a 3kHz signal bandwidth and 12kSPS sampling speed.





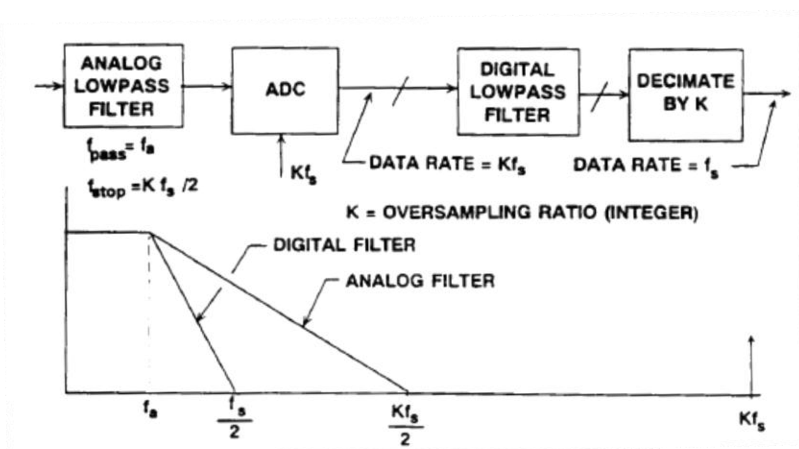
➢ Oversampling and decimation

$f_{sampling} >>> f_{Nyquist}$

Input analogue anti-alias filter significantly relaxed. The filter roll off needs to guarantee the dynamic range for (k.fs)/2 instead of fs/2.

Signal is subsequently digitally filtered and decimated down to the band of interest.

Digital low pass has to provide anti alias for fs/2 to guarantee the decimation process is alias free.

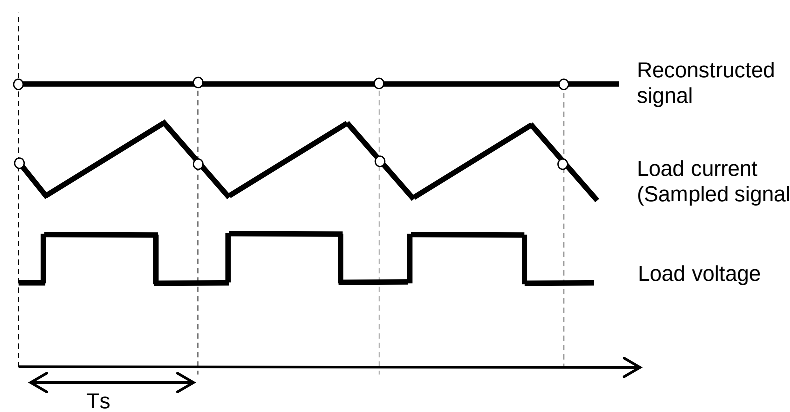


➢ Synchronized sampling

In PC applications with well known ripple noise, such as PWM converters, aliasing can be used to achieve ripple elimination.

In this case, Shannon’s theorem **is not respected** but used for our advantage.

If sampling and switching are perfectly synchronised, the effect of aliasing will be the reconstruction of the average value of the sampled signal, eliminating the ripple.

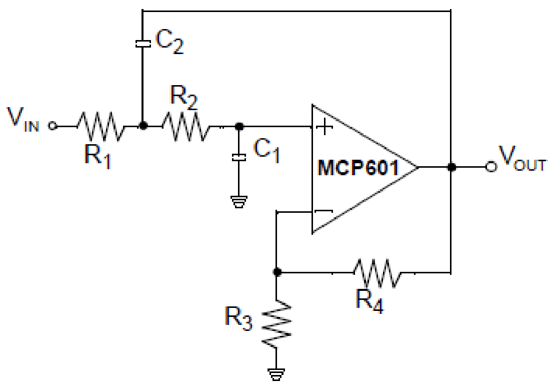


ANTI ALIAS FILTERS

- **One pole passive filters** are still used where impedance does not impact the conversion process like at input of DS converters. Otherwise **active filters** are preferred as they provide isolation and low output impedance.

A commonly used circuit is the non inverting second order **Sallen-Key** filter. Another popular circuit is the inverting **double pole multiple feedback** shown below. Cascading several stages allows higher order filtering.

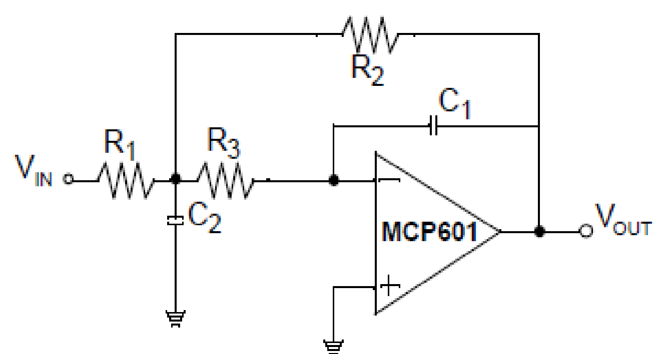
Sallen-Key



$$\frac{V_{OUT}}{V_{IN}} = \frac{K/(R_1R_2C_1C_2)}{s^2+s(1/R_1C_2+1/R_2C_2+1/R_2C_1-K/R_2C_1+1/R_1R_2C_1C_2)}$$

$$K = 1 + R_4/R_3$$

Double pole multiple feedback



$$\frac{V_{OUT}}{V_{IN}} = \frac{-1/R_1R_3C_5C_6}{s^2C_2C_1 + sC_1(1/R_1 + 1/R_2 + 1/R_3) + 1/(R_2R_3C_2C_1)}$$

Main technologies:

- **Bandgap**: Temperature compensated. Low cost, medium accuracy applications.
- **Buried Zener:** Very good long-term stability and low noise. High accuracy applications, higher cost.

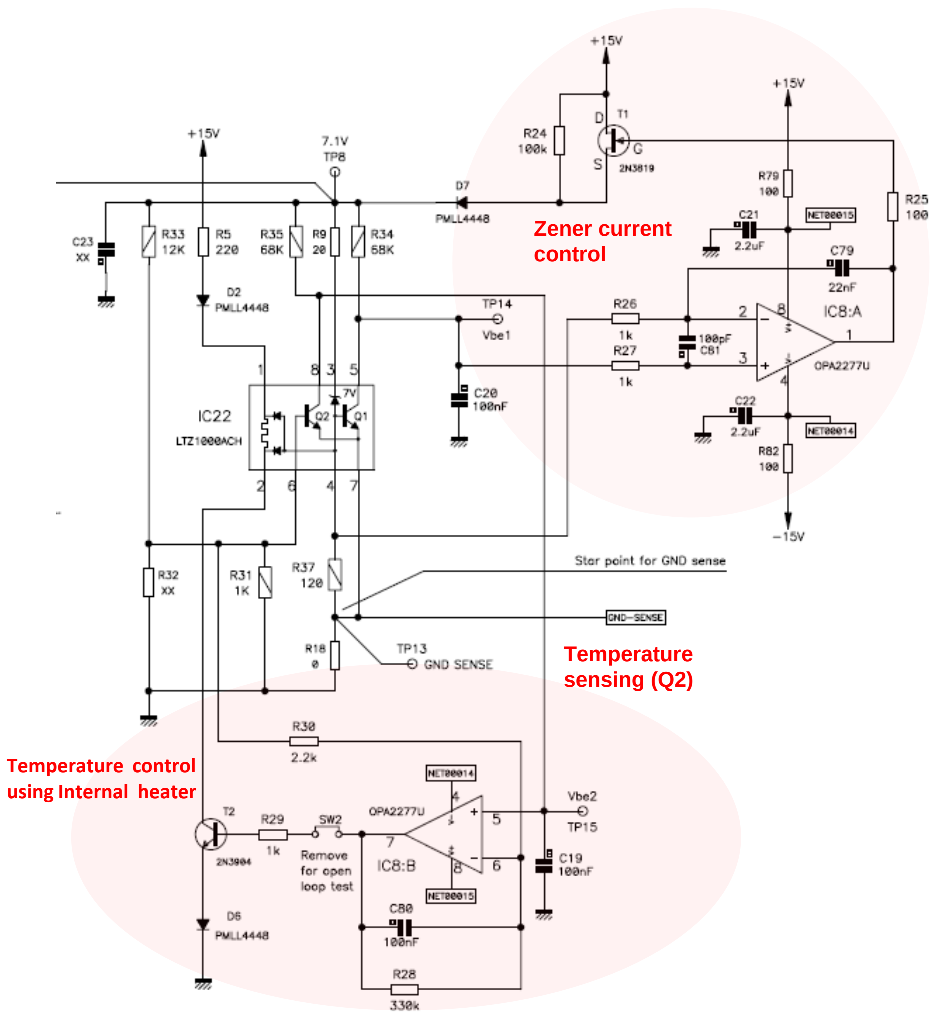
Both types can include additional on-chip circuitry to further minimize temperature drift.

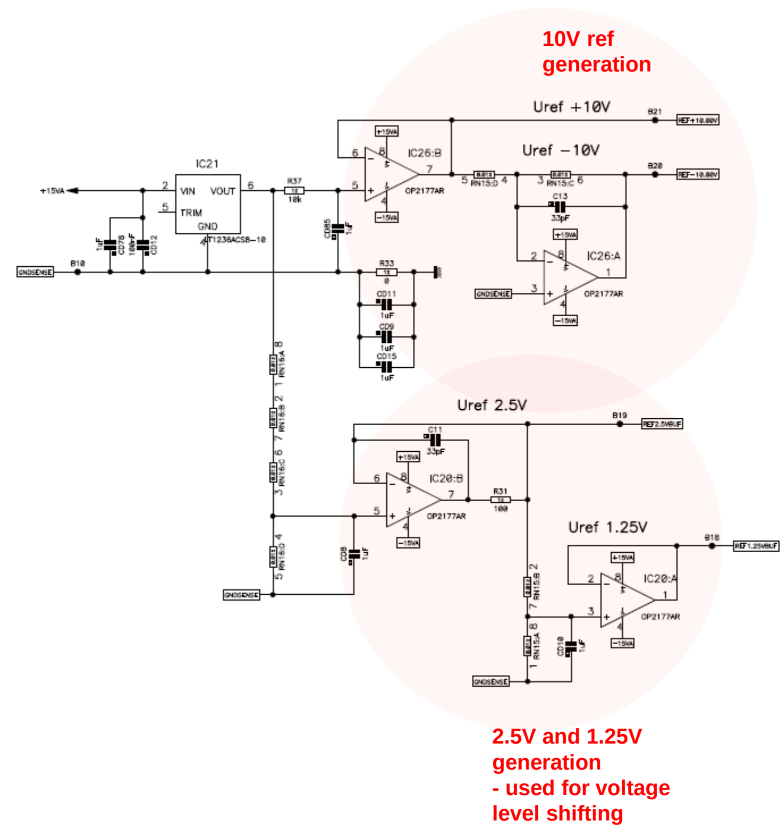
Important specification parameters

- **Initial error:** importance of this parameter depends on calibration strategy
- **Temperature coefficient:** auxiliary circuits might be included in the reference for better TC
- **Thermal hysteresis:** change in output voltage after temperature cycling. Function of packaging, IC layout. Can often be improved by a burn in process.
- **Noise:** Includes broadband thermal noise and 1/f noise.
- **Long term drift:** can be improved by a burn in process which normally involves several days power cycling at $T_{ambient}$>80ºC.
- **Line and load regulation**

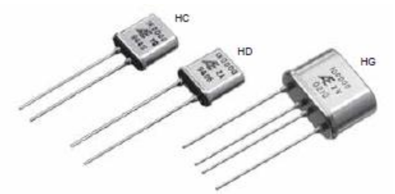
PARAMETER	THALER CORP. VRE3050 TEMPERATURE RANGE –40°C to +85°C	MAXIM MAX6250 TEMPERATURE RANGE –40°C to +85°C	ANALOG DEVICES ADR293 TEMPERATURE RANGE –40°C to +85°C
Output voltage	5.000 V	5.000 V	5.000 V
Initial error	0.01%	0.04%	0.06%
Temperature coefficient	0.6 ppm/°C	3.0 ppm/°C	8.00 ppm/°C
Noise (0.1–10 Hz)	3.0 μV_{p-p}	3.0 μV_{p-p}	15.0 μV_{p-p}
Thermal hysteresis 25°C→50°C→25°C	2 ppm	20 ppm	15 ppm
Long-term stability	6.0 ppm/1000 hrs.	20.0 ppm/1000 hrs.	0.2 ppm/1000 hrs.
Power supply	8.0 V–36 V	8.0 V–36 V	6.0 V–15 V
Turn-on settling time	10 µs	10 µs	<10 µs
Line regulation (8 V ≤ V_{IN} ≤ 10 V)	25 ppm/V	35.00 ppm/V	100.00 ppm/V
Load regulation (source 0 mA ≤ I_O ≤ 15 mA)	5 ppm/mA	7 ppm/mA	100 ppm/mA
PSRR (10 Hz–900 Hz)	95 dB	90 dB	40 dB

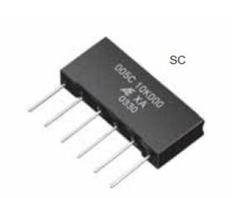
- **Voltage references**
  - Examples – ultra precision voltage reference with buried zener LTZ1000 and precision reference circuit with the LT1236, using precision network resistors to generate multiple reference voltages.

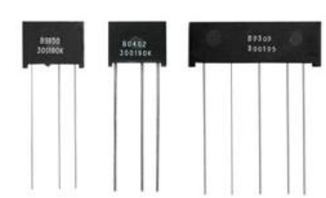


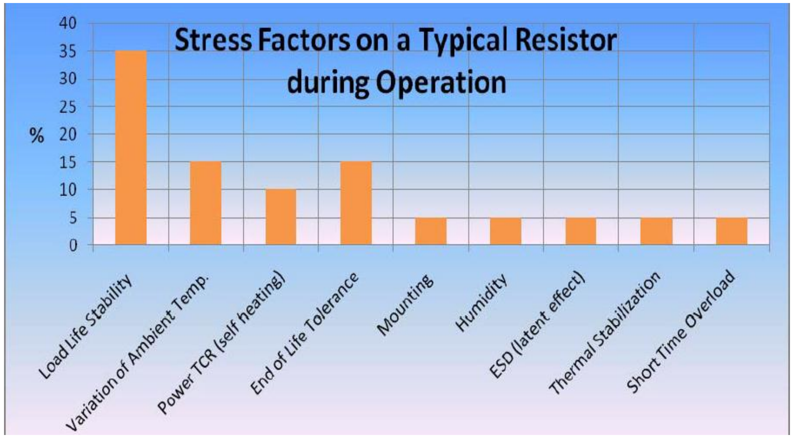


- **Network resistors**
  - For voltage division or amplification, precise ratio devices are now readily found. **TCR tracking** is of most importance for resistors used as ratio devices
  - Metal foil reaches best accuracies, followed by thin film
  - **Tolerance ≠ Precision** (a 0.05% thin film will eventually drift to 1% and prove worse than a 0.5% metal foil which has much better stability).
  - **Power coefficient** – change due to self heating (TC: changes due to ambient temperature). In an amplifier configuration with gain > 1 the power $P_{R2} > P_{R1}$ which means gain resistor internal heating will be different. Minimizing absolute TC (linked to PC) is therefore also an important factor.
  - **Load life stability** – mechanical effect of stress relaxation of the resistive element's internal construction, normally hundreds/thousands of hours.
  - **Thermal and current noise**



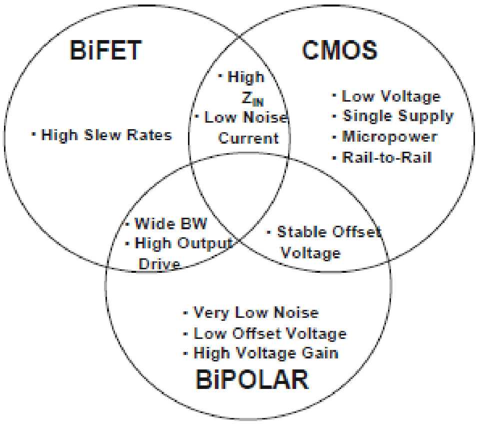






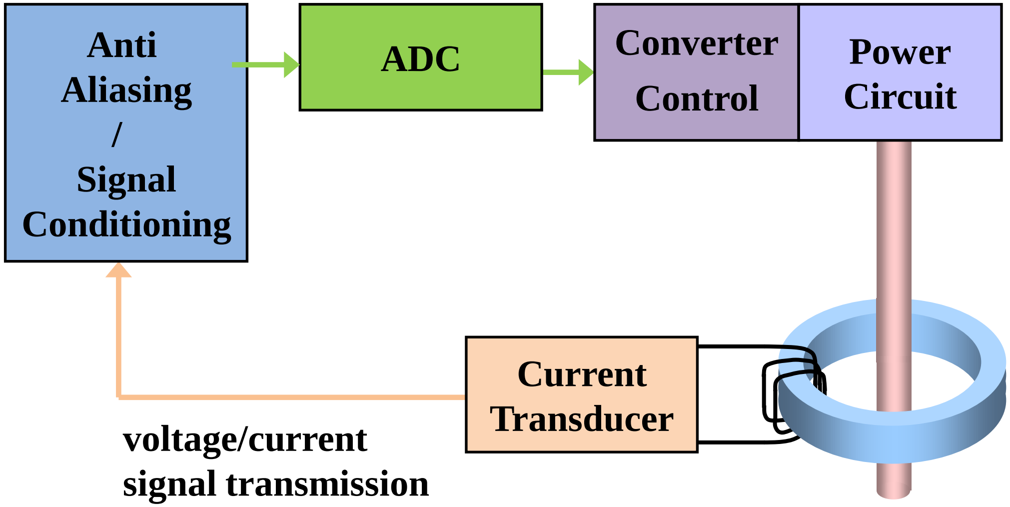
- **Important specification parameters**
  - **Input impedance**
  - **Input Offset Voltage and offset TC**
    Particularly important with high CL loop gain
  - **Input Bias Current, input noise current**
    Particularly important in applications with high value gain resistors
  - **Open Loop Gain**
    Defines the feedback loop error
  - **Opamp noise**
    (1/f) at low frequency and white at other frequencies
  - **PSRR and CMRR**
  - **Gain Bandwidth product**
    Too much bandwidth is not an advantage. Limiting the bandwidth by using a capacitor in parallel with the gain resistor is common practice.

- **Technologies: Bipolar, BiFET, CMOS**



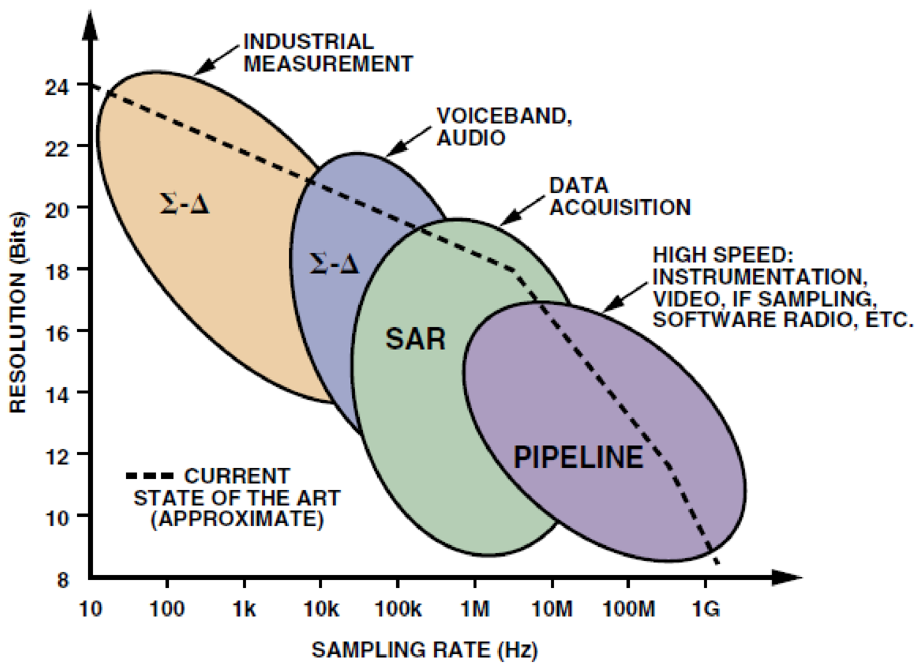
- Amplifier loading can affect output accuracy, output swing and stability.
- Of particular interest for low level high precision applications are zero drift amplifiers:
  - **Chopper stabilized amplifiers**
    Modulation/demodulation technique (e.g. LTC1052). Normally requires bandwidth limitation to exclude chopper noise
  - **Auto zero amplifiers**
    Uses switched capacitors to store and null the offset (eg AD8638)

ANALOGUE TO DIGITAL CONVERTERS



➢ Choice of ADC architecture

- **Criteria:** precision, resolution, dynamic range, speed
- **Successive Approximation Register** (SAR) converters typically range from 8 to 18 bits with sample speeds up to several MSPS. They have the ability to be connected to multiplexed inputs at a high data acquisition rate.
- **Delta-sigma converters** (ΔΣ) have virtually replaced the integrating-type ADCs (e.g. dual-slope) for applications requiring high resolution (16 bits to 24 bits) and low speed. They are inherently linear and monotonic.



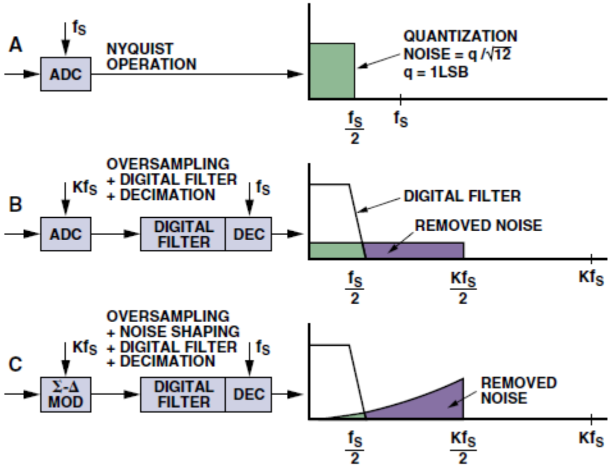
➢ Delta Sigma – Oversampling, noise shaping, digital filtering and decimation

- Figure A shows the noise spectrum for a "Nyquist" ADC sampling at fs. Figure B shows how oversampling at a K.fs (k = oversampling ratio) spreads the noise energy over a wider frequency range. Figure C shows the effect of the DS integrator in shaping the noise. This shaping can be exploited to remove most of the noise using a digital filter.

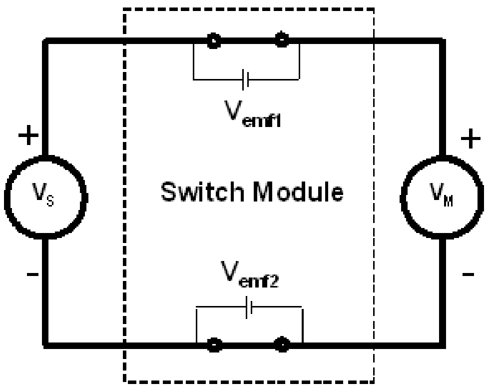
- The resolution that can be obtained with a DS depends on the **oversampling** ratio, **noise shaping** and the **digital filter**. On designing the digital filter, a tradeoff between bandwidth and resolution has to be done.

- Because of oversampling and **latency**, sigma-delta converters are not often used in multiplexed signal applications.

- **Idle tones** can be a problem in DS ADCs: Tones are caused whenever the modulator output sequence falls into a cyclic mode. They depend on the modulator (dc) input signal and the initial conditions of the integrator outputs.



- **Temperature related errors** (TC, thermal voltages) can be minimized by:
  - Choosing components with minimum TC
  - Using cancelling and compensation techniques (ratio devices, diff sensing)
  - Minimizing temperature variations and gradients
    - Temperature control – choice of control range very important: testing as close as possible to field conditions.
      - Peltier
      - Resistive element
    - Thermal isolation – isolation box, cover, pcb slots



Voltage Equation for Circuit Is:

$V_M + V_{emf1} - V_S - V_{emf2} = 0$

$V_M = V_S - V_{emf1} + V_{emf2}$

$V_M - V_S = V_{emf2} - V_{emf1}$

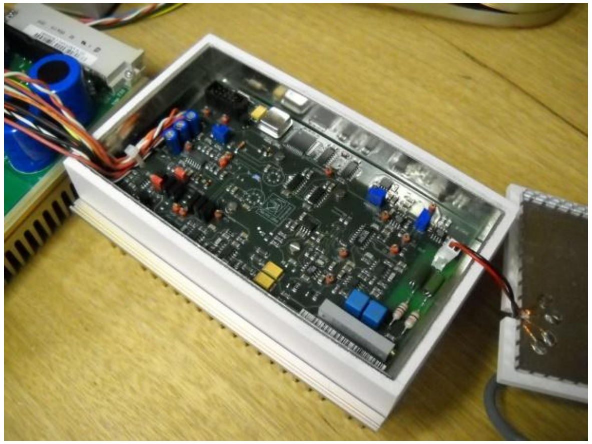
Therefore:

As $\Delta emf \rightarrow 0, (V_M - V_S) \rightarrow 0$

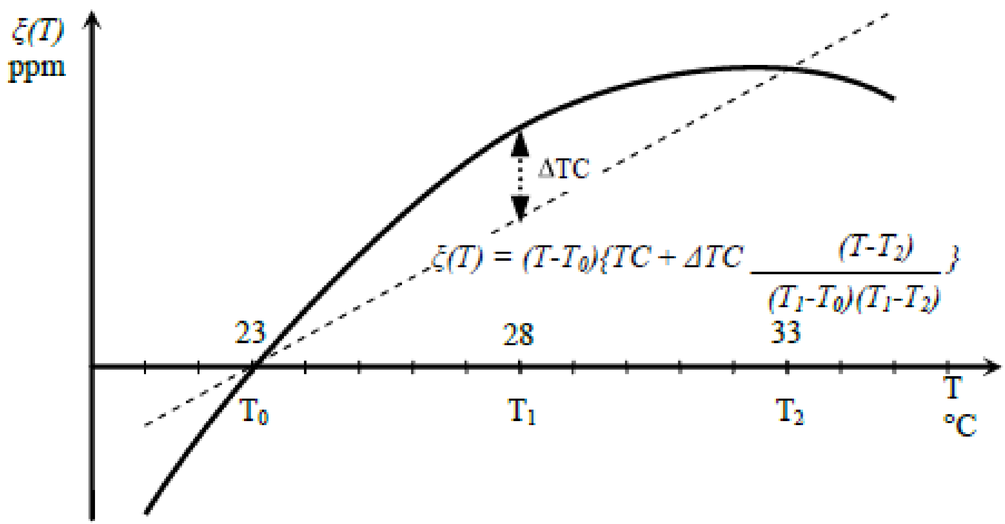
In case of DPST relays:

$V_{emf1} \cong V_{emf2}$

$\therefore V_M \cong V_S$

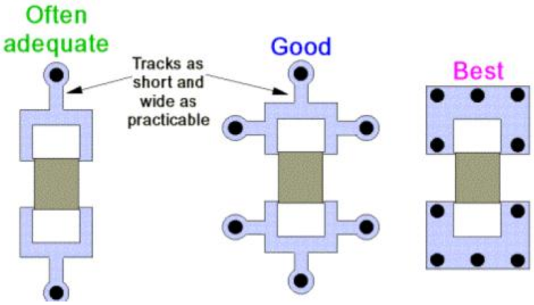


- Temperature related errors (TC, thermal voltages) can be minimized by:
  - Using **compensation algorithms**
    - First order vs second order – the TC can vary with temperature so a linear compensation might not be enough
    - Individual vs standard TCs
      It might not be possible to use individual TC values for the elements to be compensated, so an average TC might be used as long as the TC spread is not too important.



- Prefer **linear power supplies** over switching !
- If not possible, **filter**, **regulate**
- Power supply **decoupling** – keep PS impedance <1Ω across frequency
  Due to track inductance, local decoupling is necessary:
  - At the PCB entry level + at the IC level
  - Should be done with short, non-inductive connections to gnd
  - Low ESD required, might need paralleling capacitors

  Local decoupling also reduces the area of supply current loops.
- Only **gnd planes** provide proper reference and shielding
- Circuit location in the pcb is important, **think of return currents** – vias and slots increase inductance
- **Circuit segregation** can solve noise and thermal problems. If proper segregation is achieved, gnd plane splitting is not necessary.



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