D026A

# CALIBRATION and SERVICING HANDBOOK

## Volume 1

## 1271

**selfcal digital multimeter**

datron WAVETEK

# CALIBRATION and SERVICING HANDBOOK

for

# THE DATRON 1271

## SELFCAL DIGITAL MULTIMETER

## Volume 1

## Calibration and Servicing Information

## Technical Descriptions

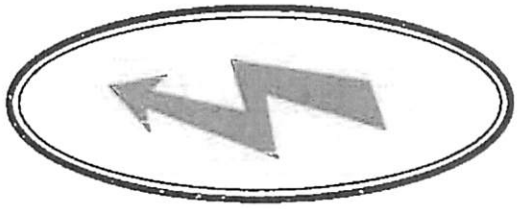
For any assistance contact your nearest Datron Sales and Service center.
Addresses can be found at the back of this handbook.

**850252** **Issue 1 (AUG 1989)**

Due to our policy of continuously updating our products, this handbook may contain minor differences in specification, components and circuit design to the actual instrument actually supplied. Amendment sheets precisely matched to your instrument serial number are available on request.

# DANGER
## HIGH VOLTAGE

**THIS INSTRUMENT IS CAPABLE OF DELIVERING**
**A LETHAL ELECTRIC SHOCK !**
**when connected to a high voltage source**



FRONT or REAR terminals carry the Full Input Voltage
**THIS CAN KILL !**

Guard terminal is sensitive to over-voltage
**It can damage your instrument !**

Unless **you** are **sure** that it is **safe** to do so,
**DO NOT TOUCH**
the **I+ I- Hi** or **Lo leads** and **terminals**

# DANGER

# Volume 1 Contents

Servicing Diagrams and Component Lists. — Refer to Volume 2

General Description, Installation, Controls, Operation, Applications; Specification, Specification Verification and Routine Calibration. — Refer to User's Handbook

# SECTION 1 CALIBRATION

## 1.1 Routine Calibration

The main features of the routine calibration facilities are described in the User's Handbook, covering:

| | |
|---|---|
| External Calibration | Section 8. |
| Internal Source Calibration | Section 8. |
| Self Calibration | Section 4. |

## 1.2 Internal Access

The high accuracy of the instrument demands that its internal environment remains undisturbed. The manufacturer's calibration certificate is invalidated if either of the covers is removed; this implies that at least a full External Calibration with Internal Source Characterization must follow any internal access, such as battery-changing, fault-finding or replacement of PCBs. Refer to *Section 4*.

N.B. Any displayed **CORRECTIONS ON** message refers to **Selfcal** corrections, generated by the most-recent self-calibration. If this was performed before the events mentioned in the above paragraph, then these corrections are not traceable to the new External Calibration and Internal Source Calibration. The message should be regarded as invalid until a **new Selfcal** is performed.

## 1.3 Remote Calibration via the IEEE 488 Interface

The 1271 is designed as a standards multimeter, its levels of accuracy demanding that it be calibrated against primary laboratory standards. The traceabilities of such standards are derived through physical devices which are as yet not remotely programmable, although the calibration facilities of the 1271 are included in its conformity to IEEE 488.2, against a time when such standards are available on the bus.

It is possible to characterize an individual calibration standard such as the Datron model 4708 at the levels required to calibrate a 1271 to its specification. The Datron 'Portocal' system can be programmed to perform these tasks automatically providing a 4708 in the system is adequately characterized. If the 1271 is not required to operate at its full specification, a regular 4708 in a remote system (e.g. Portocal) can easily be programmed to perform this task.

## 1.4 Special Calibration

The main purpose of this section is to describe four Special Calibrations which may be required under certain conditions. These are listed on the **SPCL** menu, which is accessed via the **EXT CAL** menu when in **CAL** mode. They are:

**Adc** Calibration of the instrument's main multi-slope analog-to digital converter. *Refer to paras 1.4.2.*

**Dac** Calibration of the digital-to-analog converter used for the optional 'Analog Output' of the instrument. *Refer to paras 1.4.3.*

**Freq** Calibrating the frequency detector responsible for the frequency readout in the **SIGNAL FREQUENCY** menu, which is accessed via the **Monitor** hard key then the **Freq** key in the **MONITOR** menu. The detector also provides the frequency readout used during **SPOT CAL** calibration. *Refer to paras 1.4.4.*

**ClrNv** Clearing a section of the non-volatile RAM. *Refer to paras 1.4.5.*

### Special Calibration following Memory Corruption.

*(e.g. When the battery which supplies the non-volatile calibration memory has been changed with the power off - see Section 4)*

Section 2 (Fault Diagnosis) describes the device-dependent error codes resulting from internal tests. Error codes which are generated for calibration memory faults are listed on page 2-15.

Some of these refer to individual calibration correction errors, and others to combined errors.

When faced with any of these error codes, please seek advice or assistance from your nearest Datron Service Center.

When it is deemed necessary to carry out special calibration as a result of non-volatile memory corruption, the starting point should be to clear the calibration memory before proceeding with other individual calibrations.

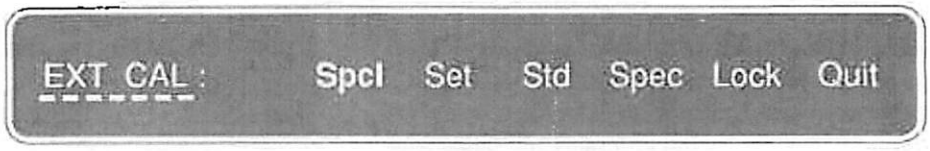
Selecting **ClrNv** in the **SPCL** menu transfers to the **CLEAR NV RAM** menu which offers a choice of clearing one or all of three sections of RAM. The selection should be chosen as a result of consultation with technical staff at the service center.

# Special Calibration Procedures

## 1.4.1 Entry into the SPCL Menu

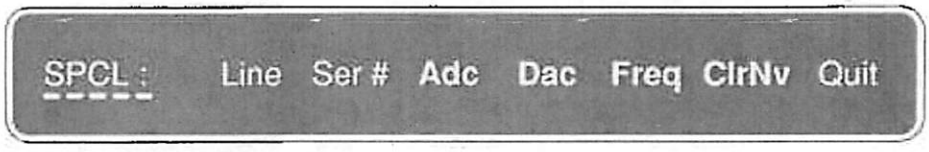
To carry out anyof the four special calibrations it is first necessary to enter the **SPCL** menu via the **EXT CAL** menu. The **EXT CAL** menu is protected, and once active, the **Caltrig** key is enabled. For these reasons, users are referred to the **'Preparation'** procedure detailed on page 8-7 of the User's handbook. Further details of the calibration facilities are described in Section 4 of the User's Handbook, beginning on page 4-40; the **EXT CAL** menu description starts on page 4-49.

### The EXT CAL Menu




Once the **EXT CAL** menu is active, pressing the **Spcl** soft key transfers to the **SPCL** menu.

### The SPCL Menu




The selection for setting the instrument to the local (50Hz or 60Hz) line frequency, and access for setting the instrument's serial nu are also on this menu. We are not concerned with these here; details can be found in the User's Handbook Section 4 page 4-51.

The four special calibrations highlighted in the above menu diagram are described in the following sub-sections 1.4.2 to 1.4.5.

## 1.4.2 Adc Key

*To calibrate the main multi-slope analog-to digital converter.*

The soft Adc key calibrates the different resolutions available from the main A-D converter, so that there are no significant differences in readings seen when changing resolutions with a constant input value.

This calibration is provided for use at manufacture and should need no further adjustment during the life of the instrument. However, if the calibration stores have been cleared or corrupted for any reason (for instance if the battery has been changed with the power off); or if a significant difference is found to exist between measurements of a constant input taken at different resolutions; then Adc calibration may be necessary.

### 1.4.2.1 To Calibrate:

No equipment is required, and the instrument does not need to be in any particular function or range.

Once in the **SPCL** menu, merely press the **Adc** soft key.

### 1.4.2.2 A-D Modes and Resolution

| | Fast-on | Fast-off |
|---|---|---|
| resln5+ | C | D |
| resln6+ | D | E |
| resln7+ | F | F |
| resln8+ | F | F |

### 1.4.2.3 A-D Modes and Power Line Cycles

| A-D Mode | Power Line Cycles |
|---|---|
| C | 312µs |
| D | 1 |
| E | 4 |
| F | 16 |

## 2.4 List of Error Code Numbers

If the A-D calibration is not successful, one of the codes in the following table may be presented on the Menu display. If so, it is possible to re-run the individual test associated with the Error Code. Refer to Section 2, page 2-13 for access to the test pathways. As this is a complex A-D, it is stongly recommended that any problems should be referred to your nearest service center.

| Error Code No. | Test Pathway No. | Power Line Freq (Hz) | A-D Mode (Power Line Cycles) | Rdgs (Discd) Avgd | Test Type | Measured Function | Test Limits |
|---|---|---|---|---|---|---|---|
| 2030 | PXXY | 50 | F (16) | (0) 8 | Zero Noise | Std. Devn. | < 0.2ppm |
| 2033 | PXXV | 50 | E (4) | (0) 8 | Zero Noise | Std. Devn. | < 1ppm |
| 2034 | PXXV | 50 | E (4) | (0) 8 | Ext. Zero Noise | Std. Devn. | -200ppmR < 50Hz 4plc Zero < +200ppmR |
| 2035 | PXXX | 50 | D (1) | (0) 8 | Zero Noise | Std. Devn. | < 2ppm |
| 2036 | PXXX | 50 | D (1) | (0) 8 | Ext. Zero Noise | Std. Devn. | -200ppmR < 50Hz 1plc Zero < +200ppmR |
| 2037 | PXXW | 50 | C (312µs) | (0) 8 | Zero Noise | Std. Devn. | < 10ppm |
| 2038 | PXXW | 50 | C (312µs) | (0) 8 | Ext. Zero Noise | Std. Devn. | -200ppmR < 50Hz 312µs Zero < +200ppmR |
| 2040 | PXXY | 60 | F (16) | (0) 8 | Zero Noise | Std. Devn. | < 0.2ppm |
| 2041 | PXXY | 60 | F (16) | (0) 8 | Ext. Zero Noise | Std. Devn. | -200ppmR < 60Hz 16plc Zero < +200ppmR |
| 2044 | PXXV | 60 | E (4) | (0) 8 | Zero Noise | Std. Devn. | < 1ppm |
| 2045 | PXXV | 60 | E (4) | (0) 8 | Ext. Zero Noise | Std. Devn. | -200ppmR < 60Hz 4plc Zero < +200ppmR |
| 2046 | PXXX | 60 | D (1) | (0) 8 | Zero Noise | Std. Devn. | < 2ppm |
| 2047 | PXXX | 60 | D (1) | (0) 8 | Ext. Zero Noise | Std. Devn. | -200ppmR < 60Hz 1plc Zero < +200ppmR |
| 2048 | PXXW | 60 | C (312µs) | (0) 8 | Zero Noise | Std. Devn. | < 10ppm |
| 2049 | PXXW | 60 | C (312µs) | (0) 8 | Ext. Zero Noise | Std. Devn. | -200ppmR < 60Hz 312µs Zero < +200ppmR |
| [illegible]0 | PXYY | 50 | F (16) | (8) 8 | +FR Noise | Std. Devn. | < 0.2ppm |
| [illegible]53 | PXYV | 50 | E (4) | (8) 8 | +FR Noise | Std. Devn. | < 1ppm |
| 2054 | PXYV | 50 | E (4) | (8) 8 | +FR + Ext. Zero | +FR gain | +FR - 100ppm < 50Hz 4plc +gain< +FR + 100ppm |
| 2055 | PXYX | 50 | D (1) | (8) 8 | +FR Noise | Std. Devn. | < 2ppm |
| 2056 | PXYX | 50 | D (1) | (8) 8 | +FR + Ext. Zero | +FR gain | +FR - 100ppm < 50Hz 1plc +gain< +FR + 100ppm |
| 2057 | PXYW | 50 | C (312µs) | (8) 8 | +FR Noise | Std. Devn. | < 10ppm |
| 2058 | PXYW | 50 | C (312µs) | (8) 8 | +FR + Ext. Zero | +FR gain | 1.000500 x FR < 50Hz 312µs +gain< 1.001000 x FR |
| 2060 | PXYY | 60 | F (16) | (8) 8 | +FR Noise | Std. Devn. | < 0.2ppm |
| 2063 | PXYY | 60 | F (16) | (8) 8 | +FR + Ext. Zero | +FR gain | +FR - 100ppm < 60Hz 16plc +gain< +FR + 100ppm |
| 2064 | PXYV | 60 | E (4) | (8) 8 | +FR Noise | Std. Devn. | < 1ppm |
| 2065 | PXYV | 60 | E (4) | (8) 8 | +FR + Ext. Zero | +FR gain | +FR - 100ppm < 60Hz 4plc +gain< +FR + 100ppm |
| 2066 | PXYX | 60 | D (1) | (8) 8 | +FR Noise | Std. Devn. | < 2ppm |
| 2067 | PXYX | 60 | D (1) | (8) 8 | +FR + Ext. Zero | +FR gain | +FR - 100ppm < 60Hz 1plc +gain< +FR + 100ppm |
| 2068 | PXYW | 60 | C (312µs) | (8) 8 | +FR Noise | Std. Devn. | < 10ppm |
| 2069 | PXYW | 60 | C (312µs) | (8) 8 | +FR + Ext. Zero | +FR gain | 1.000500 x FR < 60Hz 312µs +gain< 1.001000 x FR |
| 2070 | PXZY | 50 | F (16) | (8) 8 | -FR Noise | Std. Devn. | < 0.2ppm |
| 2073 | PXZV | 50 | E (4) | (8) 8 | -FR Noise | Std. Devn. | < 1ppm |
| 2074 | PXZV | 50 | E (4) | (8) 8 | -FR + Ext. Zero | -FR gain | -FR - 100ppm < 50Hz 4plc -gain< -FR + 100ppm |
| 2075 | PXZX | 50 | D (1) | (8) 8 | -FR Noise | Std. Devn. | < 2ppm |
| 2076 | PXZX | 50 | D (1) | (8) 8 | -FR + Ext. Zero | -FR gain | -FR - 100ppm < 50Hz 1plc -gain< -FR + 100ppm |
| 2077 | PXZW | 50 | C (312µs) | (8) 8 | -FR Noise | Std. Devn. | < 10ppm |
| 2078 | PXZW | 50 | C (312µs) | (8) 8 | -FR + Ext. Zero | -FR gain | 1.000500 x FR < 50Hz 312µs +gain< 1.001000 x FR |
| 2080 | PXZY | 60 | F (16) | (8) 8 | -FR Noise | Std. Devn. | < 0.2ppm |
| 2081 | PXZY | 60 | F (16) | (8) 8 | -FR + Ext. Zero | -FR gain | -FR - 100ppm < 60Hz 16plc -gain< -FR + 100ppm |
| 2084 | PXZV | 60 | E (4) | (8) 8 | -FR Noise | Std. Devn. | < 1ppm |
| 2085 | PXZV | 60 | E (4) | (8) 8 | -FR + Ext. Zero | -FR gain | -FR - 100ppm < 60Hz 4plc -gain< -FR + 100ppm |
| 2086 | PXZX | 60 | D (1) | (8) 8 | -FR Noise | Std. Devn. | < 2ppm |
| 2087 | PXZX | 60 | D (1) | (8) 8 | -FR + Ext. Zero | -FR gain | -FR - 100ppm < 60Hz 1plc -gain< -FR + 100ppm |
| 2088 | PXZW | 60 | C (312µs) | (8) 8 | -FR Noise | Std. Devn. | < 10ppm |
| [illegible]9 | PXZW | 60 | C (312µs) | (8) 8 | -FR + Ext. Zero | -FR gain | 1.000500 x FR < 60Hz 312µs +gain< 1.001000 x FR |

# Special Calibration Procedures (Contd.)

## 1.4.3 Dac Key

*To calibrate the digital-to-analog converter used for the optional 'Analog Output' of the instrument.*

### Analog Output Calibration

The Analog Output (Option 70) can be provided to give an output scaled from any Function/Range combination to 1 V Full Range at low impedance, whose purpose is to drive a logging chart or other recording device.

The Analog Output is calibrated at manufacture, and its accuracy is limited to 0.5% by the resolution of the Digital-to-Analog converter which produces the signal. The stability is such that further calibration of the D-A should be unnecessary during the life of the instrument. However, if the calibration stores have been cleared or corrupted for any reason (for instance if the battery has been changed with the power off); or if an analog output error is suspected to be greater than the specification; then Dac calibration may be required.

### Calibration Method

Calibration consists of stimulating the D-A from an internal digital source (representing nominal outputs), feeding the analog outputs from the I/O port back to the front panel Hi and Lo terminals (so that an output is known to exist at the I/O port pins) and using the (previously calibrated) 1 V DC range to take accurate measurements. The values of these measurements determine digital corrections which are held in non-volatile memory.

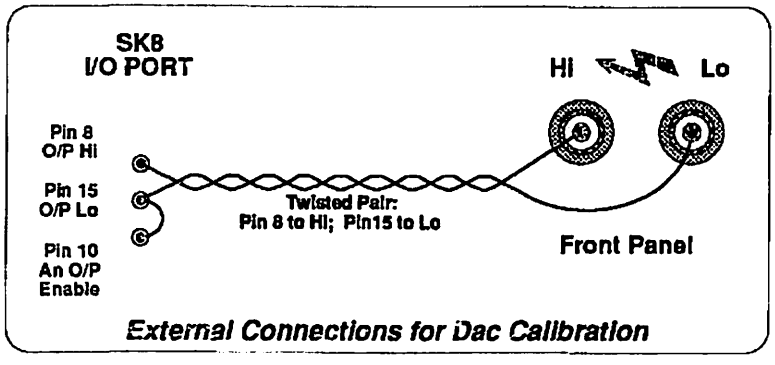
No equipment is required other than the external connections shown in the diagram.

Once the external signal path has been connected; the analog output has been enabled; and the 1V DC range has been selected; the calibration can be performed automatically by pressing the **Dac** soft key.

### To Calibrate:

Ensure that the 1V DC range has already been calibrated.

Connect the Analog Output to the Front Panel **HI** and **Lo** terminals as shown in the diagram. The connection between pins 10 and 15 of SK8 enables the Analog Output.




*External Connections for Dac Calibration*

Select the **1V DC** range and enter the **SPCL** menu via the **EXT CAL** menu.

Once in the **SPCL** menu, merely press the **Dac** soft key.

# Special Calibration Procedures (Contd.)

## 4.4 Freq

To calibrate the frequency detector responsible for the frequency readout in the **SIGNAL FREQUENCY** menu.

### Frequency Readout Calibration

The frequency of an incoming AC signal can be read out by pressing the **Freq** soft key when in the **MONITOR** menu. The **SIGNAL FREQUENCY** menu appears, with a live frequency reading which changes as the input frequency changes.
*Refer to the User's Handbook starting at page 4-23.*

The frequency detector responsible for the frequency readout is calibrated at manufacture. The frequency stability of the detector is such that further calibration should be unnecessary during the life of the instrument. However, if the calibration stores have been cleared or corrupted for any reason (for instance if the battery has been changed with the power off); or if a frequency error is suspected; then **Freq** calibration may be required.

### Calibration Method

Calibration consists of taking a measurement of an accurate 1MHz signal on the 1V AC range, and informing the computing system that the frequency is an accurate 1MHz. The measured frequency value contains the measurement error, which is used to determine a digital correction. This is held in non-volatile memory and applied for subsequent frequency readouts.

An accurate 1MHz source is required to provide an external stimulus at between 0.6V and 5.0V peak-to-peak
*Example* Datron Model 4708

Once the external signal is injected; the 1V AC range has been selected; the calibration can be performed automatically by entering the **SPCL** menu via the **EXT CAL** menu and pressing the **Freq** soft key.

### To Calibrate:

Select the **1V AC** range and enter the **SPCL** menu via the **EXT CAL** menu.

Connect an accurate source of 1MHz at between 0.6V and 5.0V peak-to-peak to the Front Panel **HI** and **Lo** terminals.

Press the **Freq** soft key.

# Special Calibration Procedures (Contd.)

## 1.4.5 ClrNv

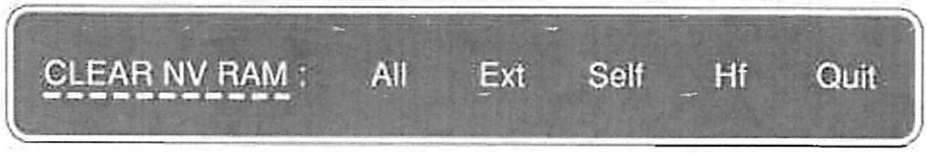
To clear a section of the non-volatile RAM used for calibration memory.

### Caution:

**Do not clear any section of RAM unless you are sure that it is absolutely necessary. You could destroy an expensive calibration!**

### The CLEAR NV RAM Menu

Selecting **ClrNv** in the **SPCL** menu transfers to the **CLEAR NV RAM** menu which offers a choice of clearing one or all of three sections of RAM. The selection should be chosen only as a result of consultation with technical staff at your nearest service center.




#### Menu Choices

| | |
|---|---|
| **All** | Returns all the non-volatile RAM calibration memories to nominal values determined by firmware. |
| **Ext** | Returns the external calibration and internal source characterization memories to nominal values determined by firmware. |
| **Self** | Returns the self calibration memories to nominal values determined by firmware. |
| **Hf** | Returns the calibration memories which hold the AC HF corrections to nominal values determined by firmware. |
| **Quit** | Transfers back to the **SPCL** menu. |

# SECTION 2 GUIDE TO 1271 FAULT DIAGNOSIS

## 2.1 Introduction

### 2.1.1 Use of Error Codes

The 1271 incorporates an extensive set of error messages, each of which includes a code number. These messages can summarize incorrect application programming via the IEEE 488 bus, or a fault within the instrument. They are intended to give the user a first indication that all is not well with the measurement which has been set up, and point the way to possible corrective action.

### 2.1.2 Code Groupings

The instrument is programmed in firmware to monitor its own operation, including interface protocols used via the IEEE 488 bus. As a result it will generate certain error codes to indicate that routine operations (including remote operation and some aspects of external calibration) are unsuccessful. Other error codes can be generated only from internal tests which are part of particular facilities initiated by the user, such as Selftest or Selfcal.

Because the remote operation of the instrument is designed to conform to the IEEE 488.2 standard, the large-scale categories of errors decreed by the standard have been used as the general basis for all error-reporting. This means that error codes and messages reported on the front panel display are consistent, as far as possible, with those reported via the IEEE 488 bus.

The type-names given to groupings of errors are thus primarily determined by those described in the IEEE 488.2 Standard specifications. Some categories apply only to bus operation, and are covered in Section 5 of the User's Handbook. Those which can be useful for diagnosing faults within the instrument are described in this section.

#### Non-Recoverable Errors

For all **Fatal System Errors**, the error condition is reported only via the front panel (this may fail if the fault is severe enough and unfortunately located). The processor stops after displaying the message. A user must respond by first recording any Error Code and accompanying message displayed on the front panel. It is then permissible to power off and restart operation from power on. If this does not clear the error condition, repair should be initiated by communicating with the nearest Datron Service Center.

#### Recoverable Errors

These consist of **Command Errors, Execution Errors** and **Device-Dependent Errors**. The reported Execution and Device-Dependent Errors are each identified by a code number, placed in two separate Last-in/First-out queues.

The codes are displayed on the instrument front panel when in local control, or can be accessed at the controller when operating in remote control via the IEEE 488 bus. Many of the messages can be reported by both methods. The code number displayed on the instrument front panel is also accompanied by an error message.

'Command' and 'Execution' errors occur mainly because of incompatible remote programming via the IEEE 488 bus. 'Execution' and 'Device-Dependent' codes can result from specific errors during External Calibration, Self Calibration, Internal Reference parameter characterization or Input Zero operations. Some messages originate whenever a particular type of fault occurs. In addition to these automatic generations, self-testing can obtain a report about deviations from specified performance. Thus whenever it is suspected that a measurement (or a series of measurements) has not been completed successfully, a self test should be run which will either confirm the instrument's performance or localize any problem via the code number system.

# 2.1 Introduction (Contd.)

## 2.1.3 'Full' and 'Fast' Selftest

The front-panel test facilities are summarized in Section 4 of the User's Handbook (*page 4-30*). Two forms of self-test are available in the TEST menu, obtained by pressing the Test hard key:

**Full Selftest**
This measures the accuracy of all main instrument functions (DCV, ACV, DCI, ACI and Ohms) and ranges of those functions, after checking the internal references and A-D operation. 'PASS' or 'FAIL' results depend on the measurements falling within tolerance limits which reflect the instrument's specification. The accuracy of these tests depends on an initial comparison between the output voltages from the two internal reference modules, and then comparing the ratio of the two against the same ratio which existed at the 'Internal Source Characterization' carried out after the most-recent external calibration to obtain a 'Drift' figure.

**Fast Selftest**
This is a subset of the set of tests allocated to a Full Selftest. It is intended as a quick 'Confidence' check to show that no serious defect is present to affect the instrument's operation. To increase the speed, only the most significant measurements from the full test are included, and most checks are run at reduced resolution (but the comparison between the reference ratio drift measurement is performed at full resolution).

The error code descriptions for Full Selftest are given in sub-section 2.6, and those codes used for Fast Selftest are repeated in sub-section 2.7 for easier access.

## 2.1.4 References in this Section

The messages are interpreted in this section to assist in fault localization:

| | |
|---|---|
| **Fatal System Errors:** | 2.2 |
| **Command Errors:** | 2.3 |
| **Execution Errors:** | 2.4 |
| **Device-Dependent Errors - Index:** | 2.5 |
| **Device-Dependent Errors - Full Test List:** | 2.6 |
| **Device-Dependent Errors - Fast Test List:** | 2.7 |

A grouped index of Device-Dependent error codes is given in sub-section 2.5. Each code carries a further reference to specific paragraphs and pages of sub-sections 2.6 and 2.7, in which the relevant element of the self-test responsible for generating the code number is described. Further references to the layout and circuit diagrams of Section 11 in Volume 2 also appear in sub-sections 2.6 and 2.7.

# 2.2 9000 Series Codes - Fatal System Errors

## 2.2.1 Introduction

System errors which cannot be recovered cause the system to halt with a message displayed (the processor stops after displaying the message). The error condition is reported only via the front panel, but this may fail if the fault is severe enough and unfortunately located.

## 2.2.2 Immediate Action

1. Record any Error Code and accompanying message displayed on the front panel. Also record the hardware environment and any operations in progress at the time of failure. Fatal System errors are generally caused by hardware or software faults.
2. Power OFF and ON again to try to restart operation.
3. If (2) is unsuccessful, power OFF again and allow the instrument to cool for 15 minutes; then try powering ON.
4. If the error condition does not recur, repeat the original operations. Check that no temperature or configuration factors cause the error condition to return. If successful, carefully proceed with further measurements as required.
5. If (2) or (3) do not clear the error condition, or if it recurs in (4); communicate with your nearest Datron Service Center, quoting the recorded data from (1), and any other details. A form of failure report is given on the sheet inside the rear cover of this handbook.

## 2.2.3 Fatal System Error Codes

| Code | Type of Fault |
|---|---|
| 9000 | System Kernel Fault |
| 9001 | Run Time System Error |
| 9002 | Unexpected Exception |
| 9003 | PROM Sumcheck Failure |
| 9004 | RAM Check Failure |
| 9005 | Serial Interface Fault |
| 9006 | Option Test Failure |
| 9007 | Unknown Engine Instruction |
| 9099 | Undefined Fatal Error |

# 2.3 Command Errors

Command Errors are reported in remote operation over the IEEE 488 bus. They are generated when the command has been 'parsed', but does not conform, either to the device command syntax, or to the IEEE 488.2 generic syntax.

The CME bit (5) is set true in the Standard-defined Event Status Byte, but there is no associated queue so no index can be given. The error is reported by the mechanisms described in the sub-section dealing with status reporting, in Section 5 of the User's Handbook.

# 2.4 1000 Series Codes - Execution Errors

## 2.4.1 Introduction

An Execution Error is generated if a command is recognized as valid (ie can be parsed and does not generate a Command Error), but cannot be executed because it is incompatible with the current device state, or because it attempts to command parameters which are out-of-limits.

### Local Operation

Most normal operations, from the front panel, lock out the conditions which would give rise to Excecution errors, by the choices not being offered in the appropriate menus. However, some selections can be made using hard keys (such as pressing ACV when the option is not present in the instrument) which cannot be locked out. In these cases the Execution error is used as an aide-memoire for the user's convenience. The error code number appears on the front-panel Menu display, accompanied by an error message.

### Remote Operation

The EXE bit (4) is set true in the Standard-defined Event Status Byte, and the error code number is appended to the Execution Error queue. The error is reported by the mechanisms described in the sub-section dealing with status reporting in Section 5 of the User's Handbook, and the queue entries can be read destructively as LIFO by the Common query command *EXQ?.

## 2.4.2 Execution Error Codes

| Code | Type of Error |
|---|---|
| 1000 | EXE queue empty when recalled |
| 1001 | Option not installed |
| 1002 | Calibration disabled |
| 1003 | Ratio/Function combination not allowed |
| 1004 | Filter incompatible with Function |
| 1005 | Input Zero not allowed |
| 1006 | Calibration not allowed in Ratio |
| 1007 | Data entry error |
| 1008 | Must be in AC Function |
| 1009 | Pass Number entry error |
| 1010 | Divide-by-zero not allowed |
| 1011 | Must be in SpotF Function |
| 1012 | No more errors in the queue |
| 1013 | Data out of limit |
| 1014 | Illegal Range/Function combination |
| 1015 | Command allowed only in Remote |
| 1016 | Not in Special Calibration |
| 1017 | Calibration not allowed with Math |
| 1018 | Key not in the Cal Enabled position |
| 1019 | Spec not compatible with Function |
| 1020 | Internal Source Cal required |
| 1021 | Test not allowed when Cal enabled |
| 1022 | No parameter for this Function |

# 2.5 2000 Series Codes - Device-Dependent Errors - Index

## 2.5.1 Introduction

A Device-Dependent Error is generated if the device detects an internal operating fault (eg. during Selfcal or Selftest). The DDE bit (3) is set *true* in the Standard-defined Event Status Byte, and the error code number is appended to the Device-Dependent Error queue.

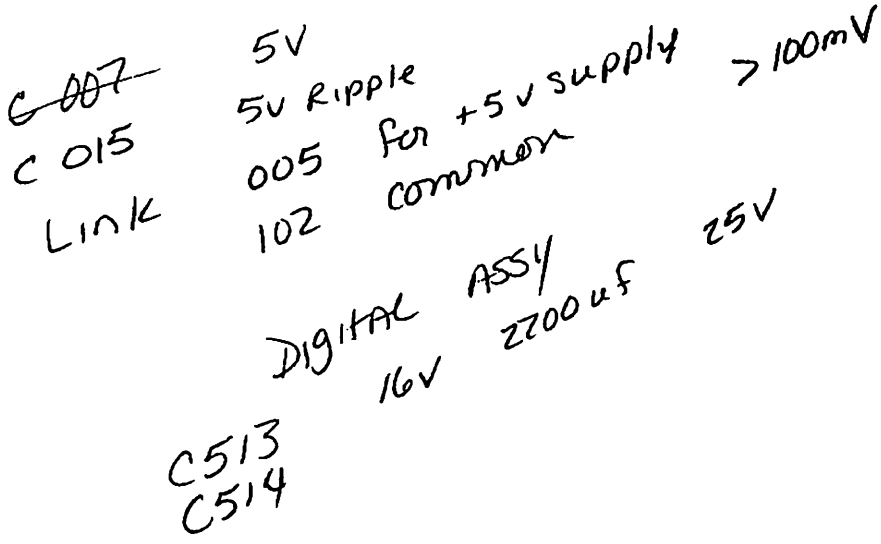
### Remote Operation

In Remote, the error is reported by the mechanisms described in the sub-section dealing with status reporting in Section 5 of the User's Handbook, and the queue entries can be read destructively as LIFO by the query DDQ?.

### Local Operation

In Local, the Device-Dependent Error queue is checked at the end of the operation (eg. Cal, Zero, Test). If *true*, an error has occurred, and the contents of the most-recent entry in the queue is displayed on the front panel. The act of displaying the message deletes its code from the queue, so the next most-recent code comes to the front of the queue and is available to be displayed. The queue must be empty for normal operation to continue.

If both bus and front panel users attempt to read the queue concurrently, the data is read out destructively on a first-come, first-served basis. Thus one of the users cannot read the data on one interface as it has already been destroyed by reading on the other. This difficulty should be solved by suitable application programming to avoid the possibility of a double readout. Ideally the IEEE 488 interface should set the instrument into REMS or RWLS to prevent confusion. The bus can ignore the queue, but the front panel user will have to read it to continue.



## 2.5.2 Index of Device-Dependent Error Codes

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| 2004 | | 2.6.4.1 | 2-15 | | |
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| 2833 | | 2.6.12 | 2-52 | | |
| 2841 | | 2.6.12 | 2-52 | | |
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## 2.6 2000 Series Codes - Device-Dependent Errors - Localization

*Codes used for Internal Source Cal, Selfcal and Full Test Start Overleaf*

*Codes used for Fast Test are in Sect 2.7, Starting on Page 2-56*

# 2.6 2000 Series Codes - Device-Dependent Errors - Localization

*(Codes used for Fast Test are in Sect 2.7)*

## 2.6.1 Introduction

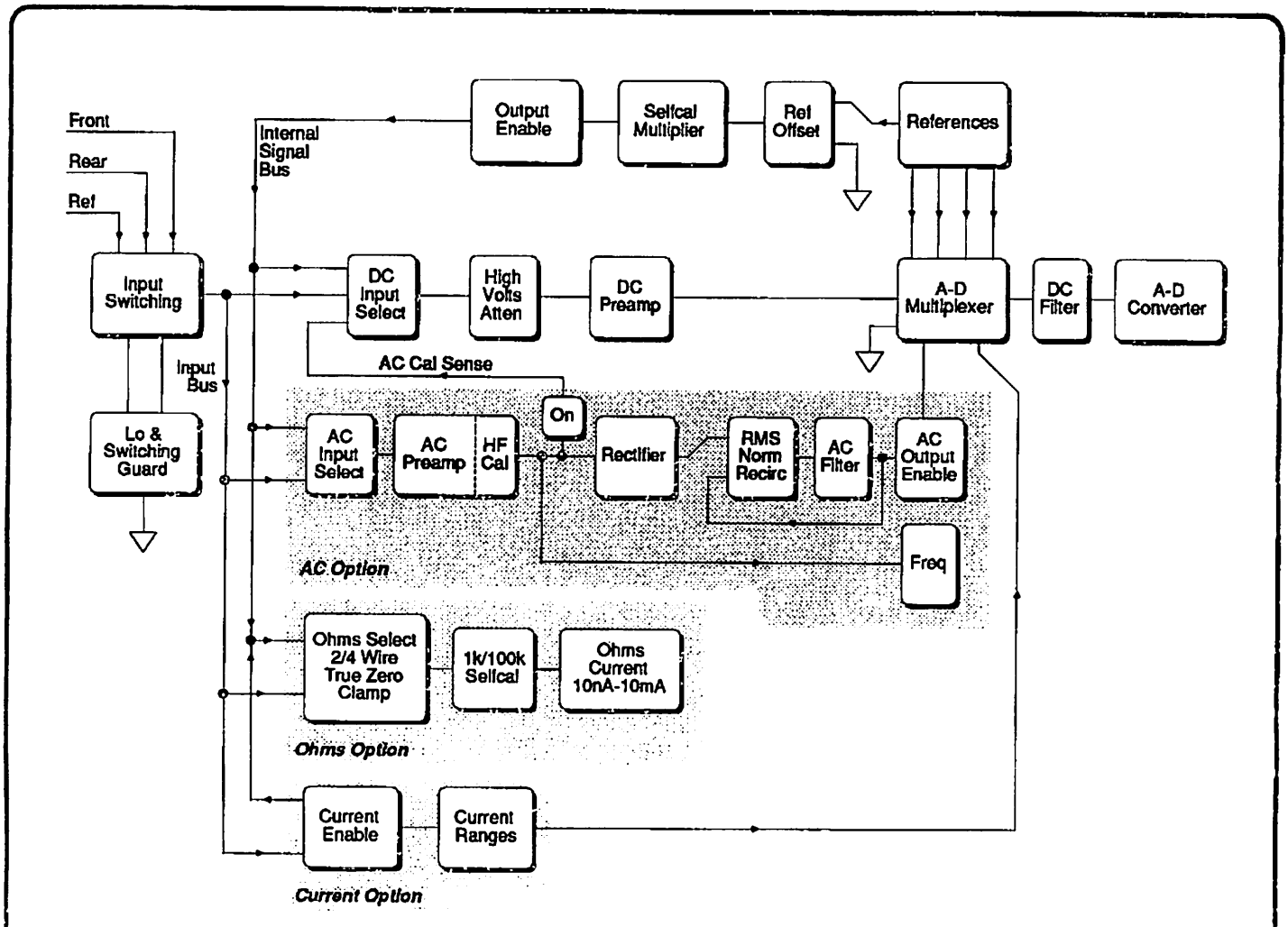
The 1271 firmware incorporates a program to run a comprehensive Self Test of the instrument's operating parameters, utilizing an internal reference as a source to stimulate measurements for the test.

There are two versions of the test: a full check of all parameters against the published specification, whose run time is about 10 minutes (for an instrument fully-loaded with all options); and a faster check of selected parameters, usually with reduced accuracy at a 'Confidence' level, which takes only 1 minute to run. Failure to meet the accuracy tolerance for any one of the parameters will generate an error code.

Error codes for parameter failures are stored in a queue to which the user has access. Sub-section 2.5 is merely an an easy-access index which provides immediate-action information and refers to sub-sections 2.6 and 2.7 which deal with 'Device-Dependent Errors', related directly to the internal operations of the 1271 itself.

The purpose of this sub-section is to identify the nature of each test and the part of the instrument which is being checked; to show test paths, with stimulation and measurement points; and to define the tolerance limits for each check. For each test that can generate an error code, references identify and locate the stimulation and measurement points on the layout and circuit diagrams in Volume 2 of this handbook.

The meanings of 'Fatal System Error', 'Command Error' and 'Execution Error' codes are described Section 5 of the User's Handbook, as they are concerned mainly with IEEE 488 operations.




*1271 Software Model*

## 2.6.2 Access to Error Codes via the 1271 Menu Keys

*(Refer to the User's Handbook, Page 4-31)*

### 2.1 Reading the Error Codes

Each of the two forms of self test runs at high speed, and does not stop unless it is aborted by the user. The error code for the first failure is noted on the Menu display, and this does not change on completion of the self test when the failure menu is displayed. At this point the user can list the codes for all the failures, reading them onto the Menu display in the order last-in, first-out (LIFO). Once an error appears on the display, it is deleted from the queue and cannot be recalled again, so the code numbers should be noted as they appear.

When the self test has stopped, and the error code numbers have been noted, it is possible to access information about each test. Each error code is associated with a unique test pathway, which is numbered, the path number being shown on the tables (indexed by error code).

### 2.6.2.2 Access to Pathway Information

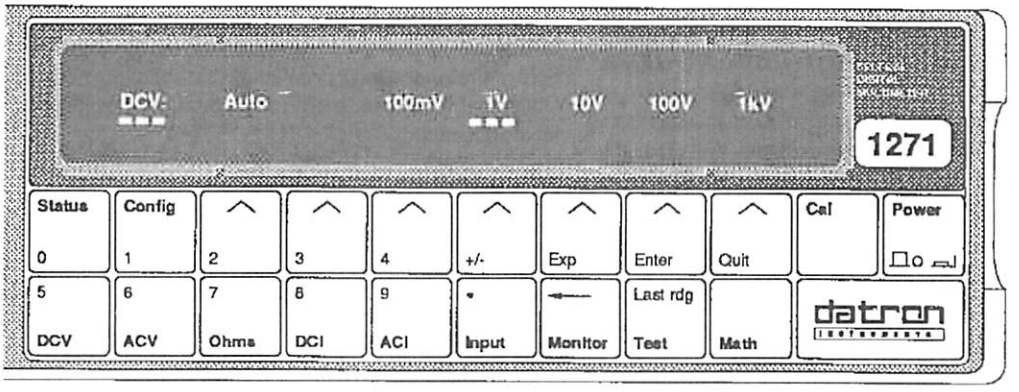
Certain menu keys allow a user to select path numbers. For each selection the live measurement readings for the path are presented on the Main Display, and can be compared against the limits shown in the table which carries the path number.

The path measurement reading on the Main Display is normalized to the range which was already selected. So before using the pathway keys it is advisable to select the 1V DC range, to obtain a *normalized* reading which only requires the range multiplier to be implemented to obtain the reading in the same form as in the table.

The method of accessing the path numbers and associated pathway information is illustrated in the following diagrams.

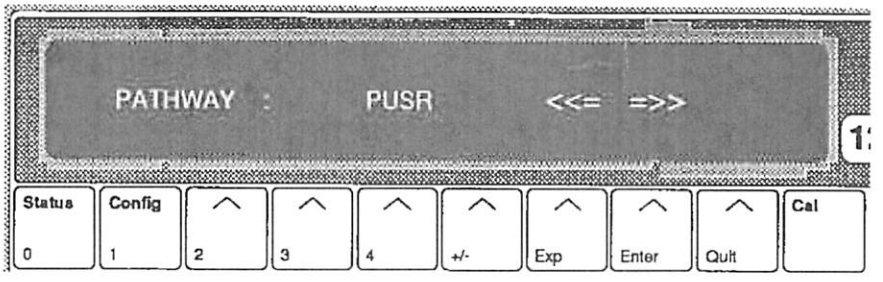
## Select the 1V DC Range

☞ Press the DCV key and then the '1V' soft key:




## Select the Pathway Facility

☞ Press the Status key, then the Config key; and finally the soft key labelled '+/-'




PUSR indicates that the present pathway is as defined by the user's previous selection of front panel keys;

<<= *(Exp)* decrements the path number by 1;

*(+/-)* decrements the path number by 20;

=>> *(Enter)* increments the path number by 1.

*(Quit)* increments the path number by 20.

Press the =>> soft key once. This reveals the number of power-line cycles in use by the A-D. For the basic 1V DC range it will show PL 16.

Press the =>> soft key a second time. This selects pathway P001; the next press selects pathway P002, and so on.

## 2.6.3 Composition of the Error Code

### 2.6.3.1 4-Digit Significance

The codes for these operations are the individual test numbers in the sequence of checks or calibrations implemented by the processor. They will appear as Error Codes only if the process has not been successful, providing data for fault diagnosis. If the fault cannot be diagnosed locally, the data should be recorded and reported for interpretation to your nearest Datron Service Center.

The four-figure code numbers for these operations are constructed as follows:

There are four decimal digits; say w, x, y and z such that in the number wxyz:

- w identifies the code as belonging to the device-dependent group - always 2;
- xy is a two-digit step number, as listed in the tables;
- z is both the measurement number and error number, of which several can be allocated within each step. Each error number is defined only for its own measurement.

### 2.6.3.2 Test Descriptions

A 'Path' number (a 3-figure number prefixed by a capital 'P') describes a single test arrangement, in which several readings are taken. A first group of readings (number of readings depends on the setup) is discarded to allow settling to take place. A second group is then taken to establish a statistical field of results. Significant measurements are made by processing the results through different digital calculations to derive up to three main characteristics:

**Standard Deviation:**
gives a noise figure;

**Mean Value:**
provides mean magnitude;

**Mean minus the Previously-Calibrated Mean:**
is a measure of the mean magnitude drift since the most-recent Internal Source Calibration.

Each characteristic results from a single measurement which, if selected for checking, is compared against specific limits of tolerance allocated in that particular setup for the characteristic. Each selected check constitutes a single measurement in the testing sequence to which a measurement number is attached: this number becomes the Error Code if the step result exceeds its tolerance limits.

### 2.6.3.3 Tables

In the following pages the list of measurements carried out during a test sequence are grouped as a table on the right page of each opening. Each table is associated with a test setup diagram on the facing left page. The tables are arranged in groups, each group being associated with a single main signal route through the main software model, from which the individual test setup diagrams are derived. Small variations of the route (due to switching within the blocks) are listed as numbered test 'paths'. These are not detailed further, as the switching information is contained within the setup description.

The tables give the test path number; test type; points of stimulus and measurement; number of readings discarded and processed; and the tolerance limits allocated to each measurement.

References to Layout and Circuit diagrams allow rapid access to the stimulus and measurement nodes.

The measurements are listed in the tables in error-code sequence. Those appearing in sub-section 2.6 are all included in 'Full Selftest', 'Selfcal' and 'Internal Source Cal'. But not all are included in 'Fast Selftest'. Sub-section 2.7 lists those measurements which form the Fast Selftest. For these steps, the Fast Selftest limits are wider than for Full Selftest, Selfcal or Internal Source Cal. Also, because of the lower resolution in Fast Selftest, more readings can be taken in the same number of line cycles. Generally, different path numbers are allocated to Fast Selftest measurements.

Note Abbreviations:
FR = Full Range (Nominal).
FS = Full Scale.

## 2.6.4 External Calibration Operations

### 2.6.4.1 Correction Errors

2000 Zero
2001 Gain+
2002 Gain-
2003 HF trim
2004 Input
2005 Lol Zero
2006 Lol Gain
2008 A-to-D
2009 Reference
2010 Frequency
2011 D-to-A
2012 Standardize

### 2.6.4.2 Corruptions

2013 Key/Pass# flags
2014 Serial Number
2015 Cal Due Date
2016 Self-corrections flag
2017 Bus Address
2018 Line Frequency
2019 Bad data from analog sub-system
2020 Measurement corrections corrupt
2021 Measurement corrections invalid
2022 NV RAM write failure
2030-2089 A-D Correction Error *(Refer to Section 1.4.2 page 1-3)*

## 2.6.5 Memory Tests

### 2.6.5.1 Non-volatile RAM Checksum Errors

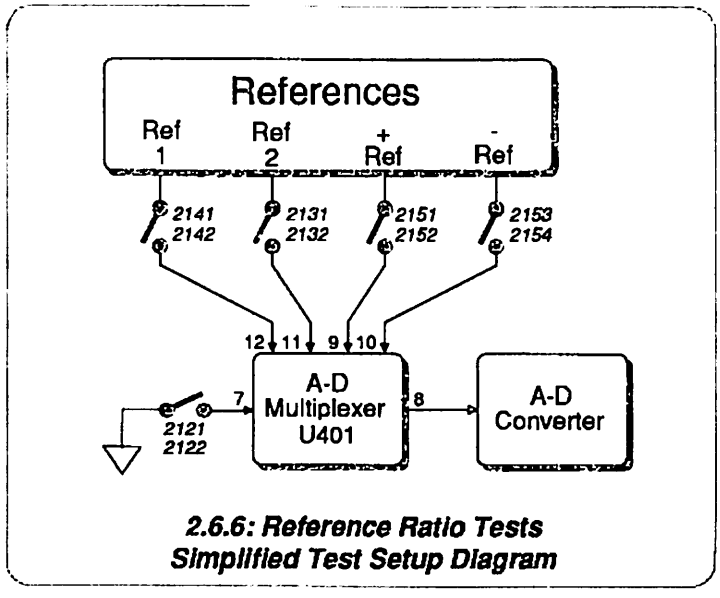
2100 Primary.
2101 Secondary.
2102 Input Zero.
2103 Frequency.

### 2.6.5.2 Fuse Tests

2111 Fuse is open circuit.
(P084) +ve value OK

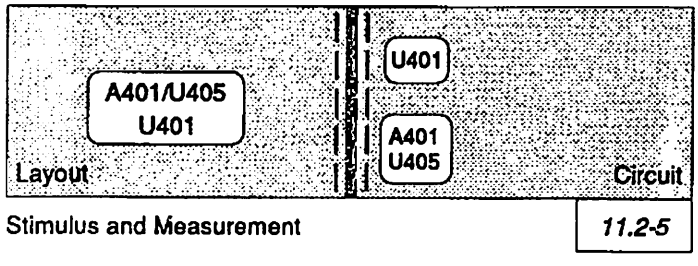
## 2.6.6 Reference Ratio Tests

**Test Setup Model**




***2.6.6: Reference Ratio Tests Simplified Test Setup Diagram***

**Volume 2 References**



## List of Reference Ratio Tests

P001 **Ref Zero Checks**
Input: Hard Zero to A-D Multiplexer. Measure: via A-D. No. of Readings: 1 Discarded; 6 Processed.

| | | |
|---|---|---|
| 2121 | Noise | Standard Deviation ≤ 5ppm of FR |
| 2122 | Magnitude | \| Mean Ref zero \| ≤ 200ppm of FR |

P003 **Ref 2 Checks**
Input: Ref 2 to A-D Multiplexer. Measure: via A-D. No. of Readings: 1 Discarded; 6 Processed.

| | | |
|---|---|---|
| 2131 | Noise | Standard Deviation ≤ 5ppm of FR |
| 2132 | Magnitude | -1.460 ≤ Mean Ref 2 ≤ -1.340 |

P002 **Ref 1 Checks**
Input: Ref 1 to A-D Multiplexer. Measure: via A-D. No. of Readings: 1 Discarded; 6 Processed.

| | | |
|---|---|---|
| 2141 | Noise | Standard Deviation ≤ 5ppm of FR |
| 2142 | Magnitude | -1.47492 ≤ Mean Ref 1 ≤ -1.41708 |

Dig. **Ref 1 : Ref 2 Magnitude Ratio Drift**
Digital comparison of the present ratio against the ratio recorded at the most-recent Internal Source Cal.

| | | |
|---|---|---|
| 2143 | Ratio Drift | -90ppm < Ratio Drift < +90ppm |

P004 **Positive Ref Checks**
Input: +Ref to A-D Multiplexer. Measure: via A-D. No. of Readings: 4 Discarded; 8 Processed.

| | | |
|---|---|---|
| 2151 | Noise | Standard Deviation ≤ 5ppm of FR |
| 2152 | Magnitude | +1.9992 < Mean +Ref < +2.0008 |

P005 **Negative Ref Checks**
Input: -Ref to A-D Multiplexer. Measure: via A-D. No. of Readings: 4 Discarded; 8 Processed.

| | | |
|---|---|---|
| 2153 | Noise | Standard Deviation ≤ 5ppm of FR |
| 2154 | Magnitude | -2.0008 < Mean -Ref < -1.9992 |

Dig. **+Ref 1 : -Ref 2 Magnitude Ratio**
Digital calculation of +Ref : -Ref.

| | | |
|---|---|---|
| 2155 | Magnitude Ratio | -1.0002 < +Ref / -Ref < -0.99998 |

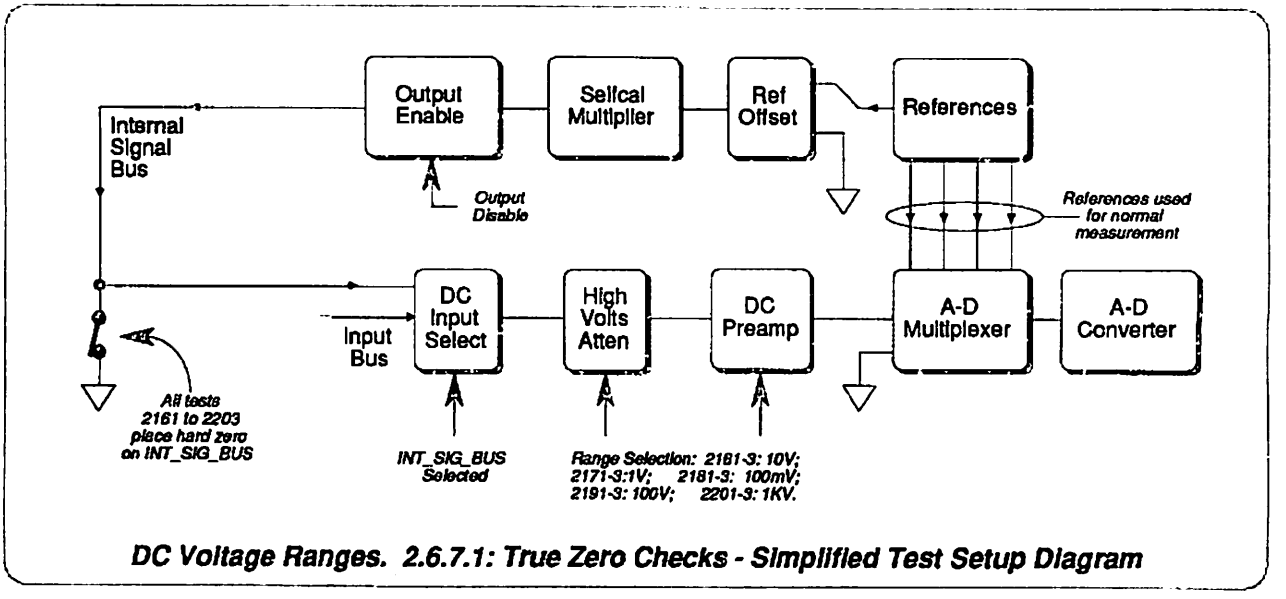
Dig. **+Ref 1 : -Ref 2 Magnitude Ratio Drift**
Digital comparison of the present ratio against the ratio recorded at the most-recent Internal Source Cal.

| | | |
|---|---|---|
| 2156 | Ratio Drift | -20ppm < Ratio drift < +20ppm |

# 2.6.7 DC Voltage Tests

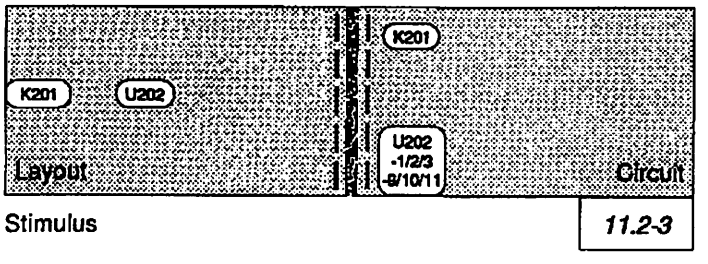
## 2.6.7.1 True Zero Checks

### Test Setup Model

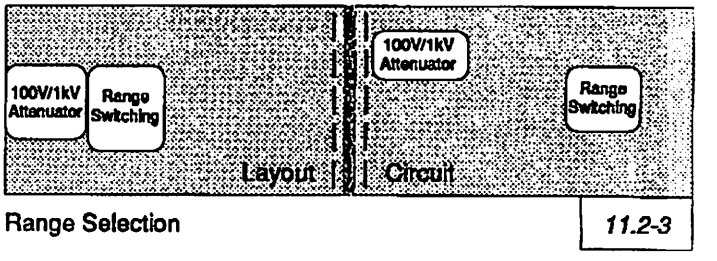



*DC Voltage Ranges. 2.6.7.1: True Zero Checks - Simplified Test Setup Diagram*

### Volume 2 References




Stimulus 11.2-3




Range Selection 11.2-3

## List of True Zero Measurements

P006 **10V Range True Zero Checks**
Input: Zero to 10VDC Range. Measure: via A-D. No of Readings: 4 Discarded; 16 Processed.

| | | |
|---|---|---|
| 2161 | Noise | Standard Deviation ≤ 1ppm |
| 2162 | Magnitude | -10ppm < Mean 10V Zero < +10ppm |

Dig. **10V Range True Zero Magnitude Ratio Drift**
Digital comparison of the present magnitude against that recorded at the most-recent Internal Source Cal.

| | | |
|---|---|---|
| 2163 | Zero Drift | -4ppm < 10V Zero Drift < +4ppm |

P011 **1V Range True Zero Checks**
Input: Zero to 1VDC Range. Measure: via A-D. No of Readings: 1 Discarded; 8 Processed.

| | | |
|---|---|---|
| 2171 | Noise | Standard Deviation ≤ 2ppm |
| 2172 | Magnitude | -25ppm < Mean 1V Zero < +25ppm |

Dig. **1V Range True Zero Magnitude Ratio Drift**
Digital comparison of the present magnitude against that recorded at the most-recent Internal Source Cal.

| | | |
|---|---|---|
| 2173 | Zero Drift | -8ppm < 1V Zero Drift < +8ppm |

P016 **100mV Range True Zero Checks**
Input: Zero to 100mVDC Range. Measure: via A-D. No of Readings: 1 Discarded; 8 Processed.

| | | |
|---|---|---|
| 2181 | Noise | Standard Deviation ≤ 5ppm |
| 2182 | Magnitude | -250ppm < Mean 100mV Zero < +250ppm |

**100mV Range True Zero Magnitude Ratio Drift**
Digital comparison of the present magnitude against that recorded at the most-recent Internal Source Cal.

| | | |
|---|---|---|
| 2183 | Zero Drift | -40ppm < 100mV Zero Drift < +40ppm |

P021 **100V Range True Zero Checks**
Input: Zero to 100VDC Range. Measure: via A-D. No of Readings: 1 Discarded; 8 Processed.

| | | |
|---|---|---|
| 2191 | Noise | Standard Deviation ≤ 10ppm |
| 2192 | Magnitude | -10ppm < Mean 100V Zero < +10ppm |

Dig. **100V Range True Zero Magnitude Ratio Drift**
Digital comparison of the present magnitude against that recorded at the most-recent Internal Source Cal.

| | | |
|---|---|---|
| 2193 | Zero Drift | -8ppm < 100V Zero Drift < +8ppm |

P028 **1kV Range True Zero Checks**
Input: Zero to 1kVDC Range. Measure: via A-D. No of Readings: 1 Discarded; 8 Processed.

| | | |
|---|---|---|
| 2201 | Noise | Standard Deviation ≤ 10ppm |
| 2202 | Magnitude | -10ppm < Mean 1kV Zero < +10ppm |

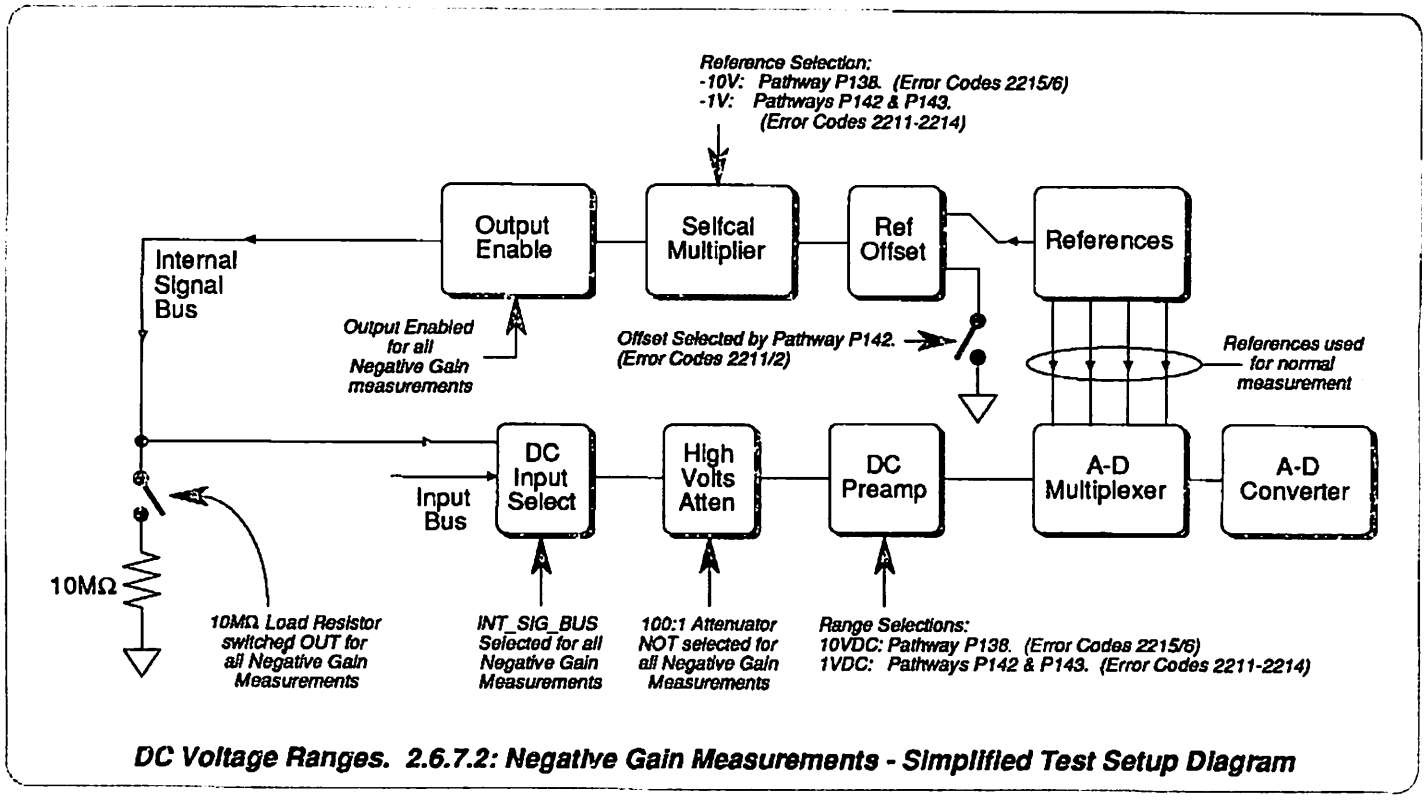
Dig. **1kV Range True Zero Magnitude Ratio Drift**
Digital comparison of the present magnitude against that recorded at the most-recent Internal Source Cal.

| | | |
|---|---|---|
| 2203 | Zero Drift | -4mV < 1000V Zero Drift < +4mV |

## 2.6.7 DC Voltage Tests (Contd)

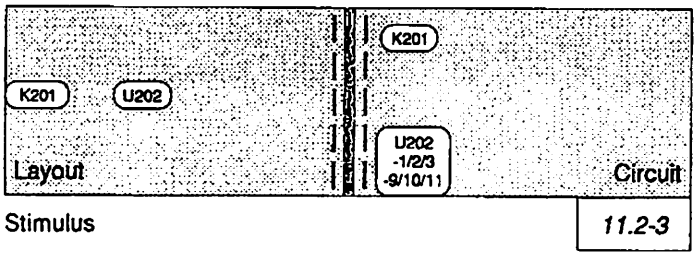
### 2.6.7.2 Negative Gain Measurements [Offset (Zero) and References]

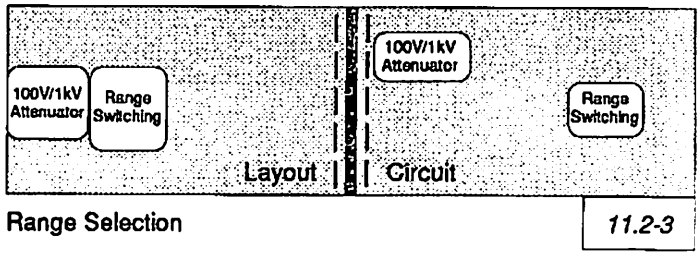
**Test Setup Model**




***DC Voltage Ranges. 2.6.7.2: Negative Gain Measurements - Simplified Test Setup Diagram***

**Volume 2 References**



## List of Negative Gain Measurements

P142 **1V Range -Offset Zero Checks**
Input: -1V Offset to 1VDC Range. Measure: via A-D. No of Readings: 32 Discarded; 8 Processed.

| | | |
|---|---|---|
| 2211 | Noise | Standard Deviation ≤ 0.01 |
| 2212 | Magnitude | -2500ppm < Mean -1V Offset < +2500ppm |

P143 **1V Range -Reference Checks**
Input: -1V Reference to 1VDC Range. Measure: via A-D. No of Readings: 16 Discarded; 8 Processed.

| | | |
|---|---|---|
| 2213 | Noise | Standard Deviation ≤ 0.01 |
| 2214 | Magnitude | -1.040V < Mean -1V Ref < -0.960V |

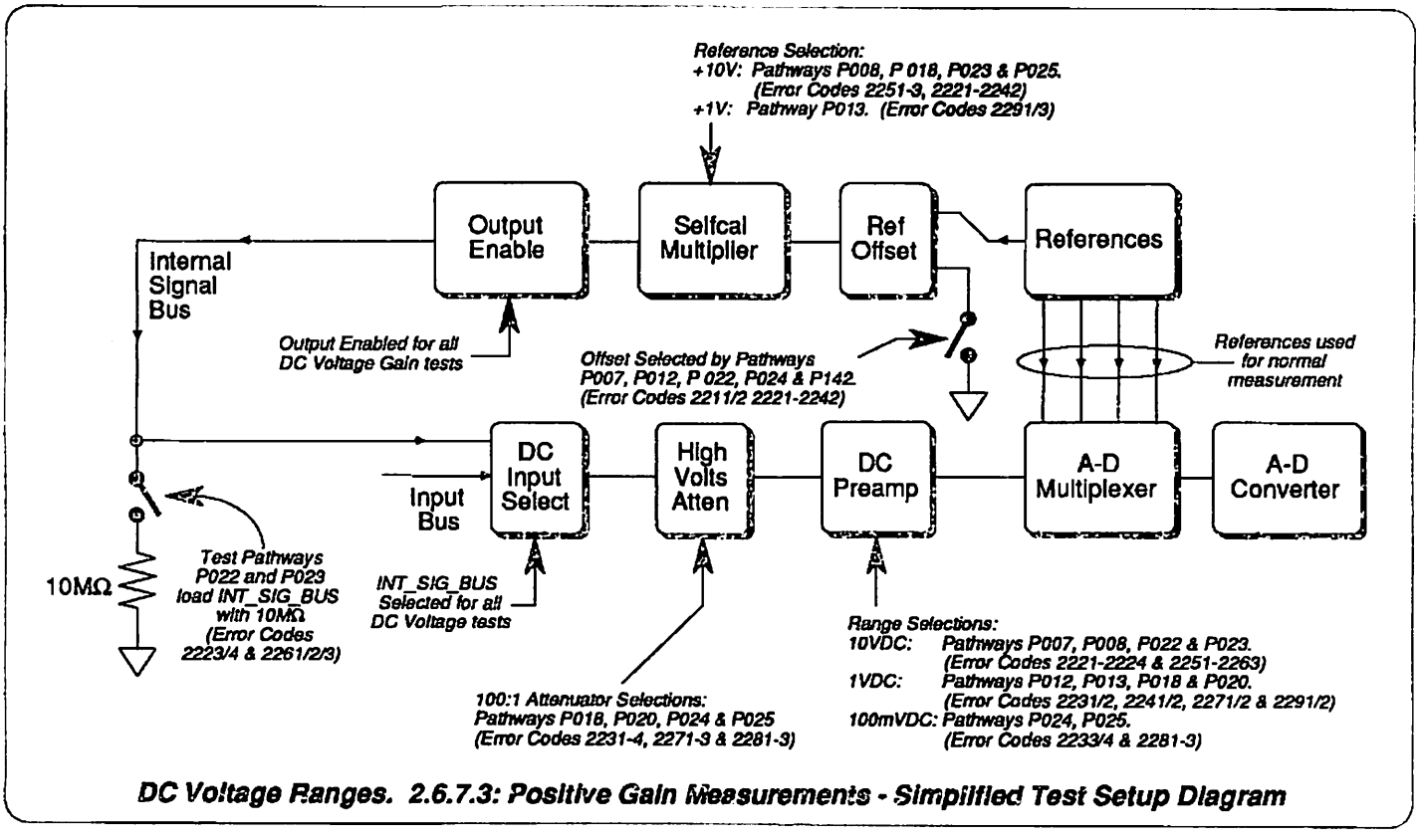
P138 **10V Range -Reference Checks**
Input: -10V Reference to 10VDC Range. Measure: via A-D. No of Readings: 16 Discarded; 8 Processed.

| | | |
|---|---|---|
| 2215 | Noise | Standard Deviation ≤ 0.01 |
| 2216 | Magnitude | -10.2V < -10V Ref < -9.5V |

## 2.6.7 DC Voltage Tests (Contd)

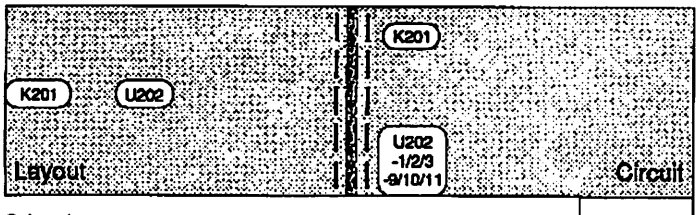
### 2.6.7.3 Positive Gain Measurements [Offset (Zero) and References]

**Test Setup Model**

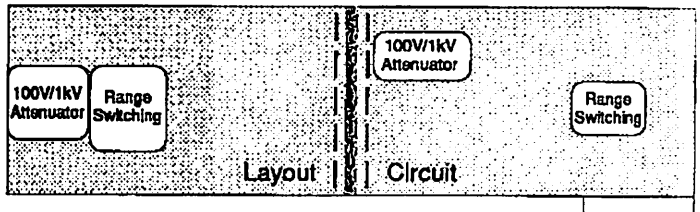



***DC Voltage Ranges. 2.6.7.3: Positive Gain Measurements - Simplified Test Setup Diagram***

**Volume 2 References**




Stimulus 11.2-3




Range Selection 11.2-3

## List of Positive Gain Measurements

P007 **10V Range +10V Offset Zero Checks**
Input: +10V Offset to 10V DC Range. Measure: via A-D. No of Readings: 24 Discarded; 8 Processed.

| | | |
|---|---|---|
| 2221 | Noise | Standard Deviation ≤ 2ppm |
| 2222 | Magnitude | -50ppm < Mean + 10V Offset < +50ppm |

P022 **10V Range - Loaded +10V Offset Zero**
Input: +10V Offset to 10MΩ Load and 10V DC Range. Measure: via A-D.
No of Readings: 4 Discarded; 8 Processed.

| | | |
|---|---|---|
| 2223 | Noise | Standard Deviation ≤ 2ppm |
| 2224 | Offset Magnitude | -50ppm < Mean +10V Offset < +50ppm |

P020 **1V Range - Attenuated +10V Offset Zero**
Input: +10V Offset via attenuator to 1V DC Range. Measure: via A-D.
No of Readings: 4 Discarded; 32 Processed.

| | | |
|---|---|---|
| 2231 | Noise | Standard Deviation ≤ 2ppm |
| 2232 | Magnitude | -50ppm < Mean +1V Offset < +50ppm |

P024 **100mV Range - Attenuated +10V Offset Zero**
Input: +10V Offset via attenuator to 100mV DC Range. Measure: via A-D.
No of Readings: 4 Discarded; 16 Processed.

| | | |
|---|---|---|
| 2233 | Noise | Standard Deviation ≤ 2ppm |
| 2234 | Magnitude | -500ppm < +100mV Offset < +500ppm |

P012 **1V Range - +1V Offset Zero**
Input: +1V Offset to 1V DC Range. Measure: via A-D. No of Readings: 8 Discarded; 12 Processed.

| | | |
|---|---|---|
| 2241 | Noise | Standard Deviation ≤ 3ppm |
| 2242 | Magnitude | -500ppm < +Offset < +500ppm |

P008 **10V Range - +Reference Checks**
Input: +10V Reference to 10V DC Range. Measure: via A-D. No of Readings: 8 Discarded; 8 Processed.

| | | |
|---|---|---|
| 2251 | Noise | Standard Deviation ≤ 2ppm |
| 2252 | Magnitude | +0.94 < +10V Ref < +1.01 |

Dig. **+10V Ref Magnitude Drift**
Digital comparison of the present magnitude against that recorded at the most-recent Internal Source Cal.

| | | |
|---|---|---|
| 2253 | Magnitude Drift | 0.999940 < drift < 1.000060 |

P023 **10V Range - Loaded +10V Reference Checks**
Input: +10V to 10MΩ Load and 10V DC Range. Measure: via A-D.
No of Readings: 4 Discarded; 8 Processed.

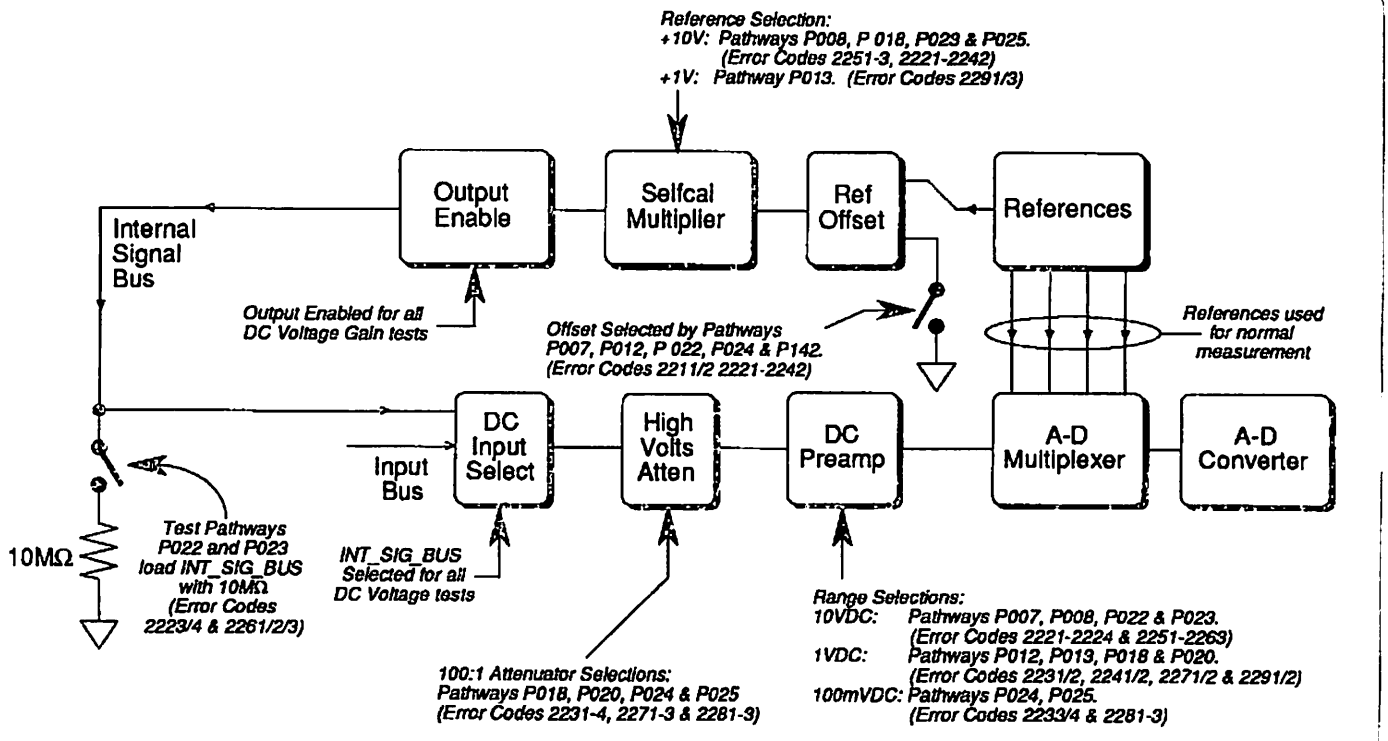
| | | |
|---|---|---|
| 2261 | Noise | Standard Deviation ≤ 3ppm |
| 2262 | Magnitude | +.94 < 10V Gain < +1.01 |

Dig. **10V Range - Loaded +10V Ref Magnitude Drift**
Digital comparison of the present magnitude against that recorded at the most-recent Internal Source Cal.

| | | |
|---|---|---|
| 2263 | Magnitude Drift | 0.999940 < drift < 1.000060 |

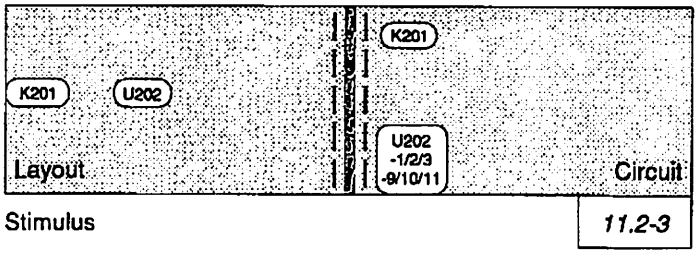
## 2.6.7.3 Positive Gain Measurements (Contd)
[Offset (Zero) and References]

**Test Setup Model**

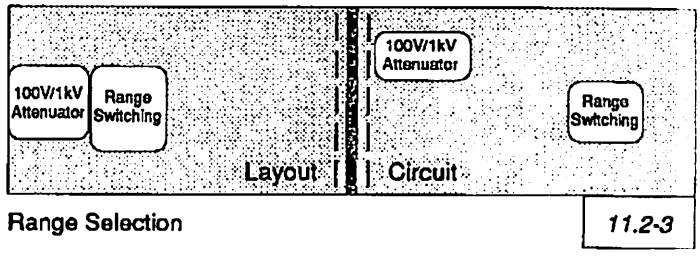



***DC Voltage Ranges. 2.6.7.3: Positive Gain Measurements - Simplified Test Setup Diagram***

**Volume 2 References**




Stimulus 11.2-3




Range Selection 11.2-3

## List of Positive Gain Measurements (Contd.)

P018 **1V Range - Attenuated +10V Reference Checks**
Input: +10V DC via 100:1 attenuator to 1V DC Range. Measure: via A-D.
No of Readings: 4 Discarded; 32 Processed.

| | | |
|---|---|---|
| **2271** | +100mV Signal Noise | Standard Deviation of +100mV Signal ≤ 10ppm |
| **2272** | Magnitude | +0.095 < +100mV Signal Magnitude < +0.101 |

Dig. **1V Range - Attenuated +10V Ref Magnitude Drift**
Digital comparison of the present magnitude against that recorded at the most-recent Internal Source Cal.

| | | |
|---|---|---|
| **2273** | +100mV Signal Mag. Drift | +0.999910 < drift < +1.000090 |

P025 **100mV Range - Attenuated +10V Reference Checks**
Input: +10V DC via 100:1 attenuator to 100mV DC Range. Measure: via A-D.
No of Readings: 4 Discarded; 16 Processed.

| | | |
|---|---|---|
| **2281** | +100mV Signal Noise | Standard Deviation of +100mV signal ≤ 10ppm |
| **2282** | Magnitude | +0.94 < +100mV Signal Magnitude < +1.01 |

Dig. **100mV Range - Attenuated +10V Ref Magnitude Drift**
Digital comparison of the present magnitude against that recorded at the most-recent Internal Source Cal.

| | | |
|---|---|---|
| **2283** | +100mV Signal Mag. Drift | +0.9999 < drift < +1.0001 |

P013 **1V Range - +1V Reference Checks**
Input: +1V Reference to 1V DC Range. Measure: via A-D. No of Readings: 8 Discarded; 12 Processed.

| | | |
|---|---|---|
| **2291** | Noise | Standard Deviation ≤ 3ppm |
| **2292** | Magnitude | +0.965 < +1V Ref < +1.025 |

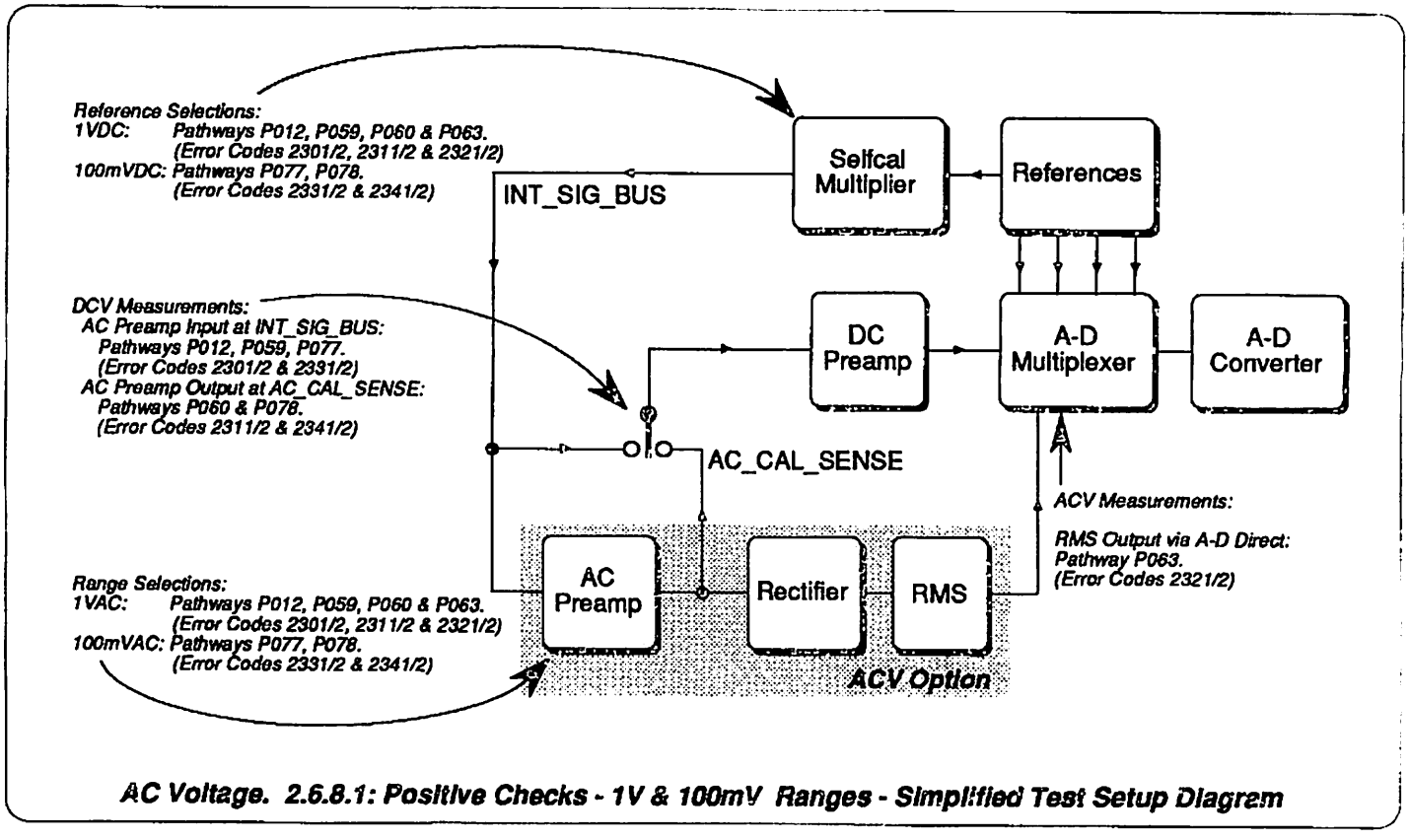
Dig. **1V Range - +1V Ref Magnitude Drift**
Digital comparison of the present magnitude against that recorded at the most-recent Internal Source Cal.

| | | |
|---|---|---|
| **2293** | Drift | +0.999940 < Ref drift < +1.000060 |

## 2.6.8 AC Voltage Tests

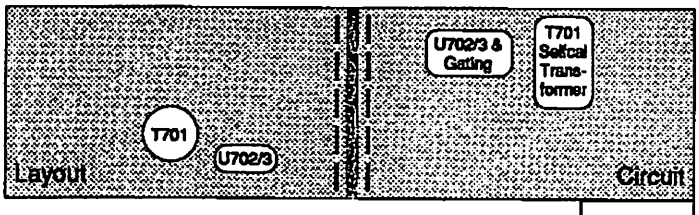
### 2.6.8.1 Positive Tests

**Test Setup Model**

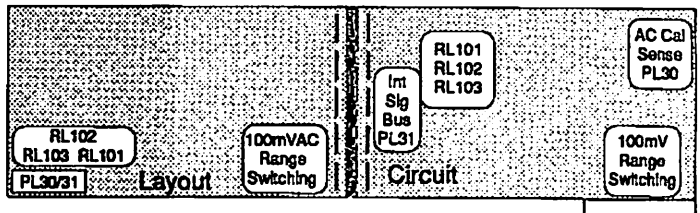



***AC Voltage. 2.6.8.1: Positive Checks - 1V & 100mV Ranges - Simplified Test Setup Diagram***

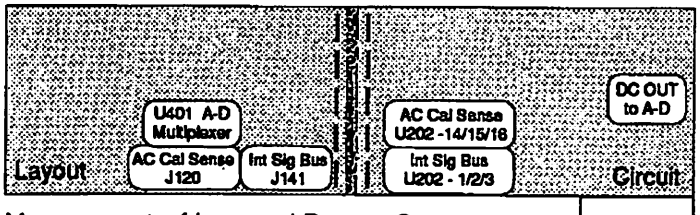
**Volume 2 References**



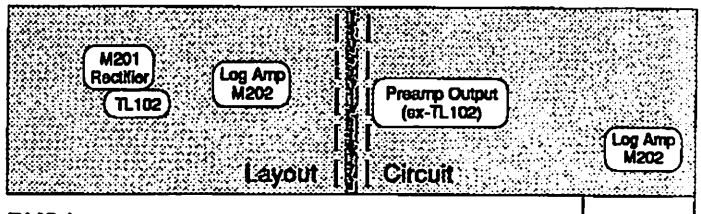

Stimulus *11.2-8*



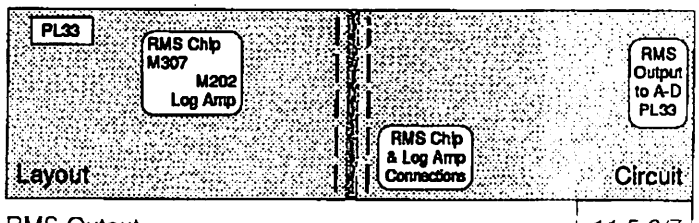

Signal Application, Range Selection and Preamp Output Sensing *11.5-1/5*




Measurement of Input and Preamp Output via DC Voltage Ranges *11.2-3*




RMS Input *11.5-2/6*




RMS Output *11.5-3/7*

## List of Positive Measurements

### 1VAC Range

P012 **1V AC Range - Settling Time**
Input: +1VDC to AC Preamp set to 1VAC Range. Measure: Input using 1V DC Range at INT_SIG_BUS.
No. of Readings: 0 Discarded; 8 Processed then Discarded to generate settling time.

| | | |
|---|---|---|
| | Measure and Discard | — (settling) |

P059 **1V AC Range - +1V DC Input Checks**
Input: +1VDC to AC Preamp set to 1VAC Range. Measure: Input using 1V DC Range at INT_SIG_BUS.
No. of Readings: 8 Discarded; 8 Processed.

| | | |
|---|---|---|
| 2301 | Input Noise | Standard Deviation ≤ 20ppm of FS |
| 2302 | Input Magnitude | +0.96 < Mean Signal < +1.04 |

P060 **1V AC Range - +1V DC Input - Checks at AC Preamp Output**
Input: +1VDC to AC Preamp set to 1VAC Range.
Measure: Preamp Output using 1V DC Range at AC_CAL_SENSE.
No. of Readings: 2 Discarded; 16 Processed.

| | | |
|---|---|---|
| 2311 | Preamp Output Noise | Standard Deviation ≤ 50ppm of FS |
| 2312 | Preamp Output Magnitude | -1.04 < Mean Signal < -0.96 |

P063 **1V AC Range - +1V DC Input - Checks at RMS Converter Output**
Input: +1VDC to AC Preamp set to 1VAC Range. Measure: RMS Output via A-D.
No. of Readings: 2 Discarded; 16 Processed.

| | | |
|---|---|---|
| 2321 | +RMS Output Noise | Standard Deviation ≤ 50ppm of FS |
| | +RMS Output Magnitude | +0.96 < Mean Signal < +1.04 |

### 100mV AC Range

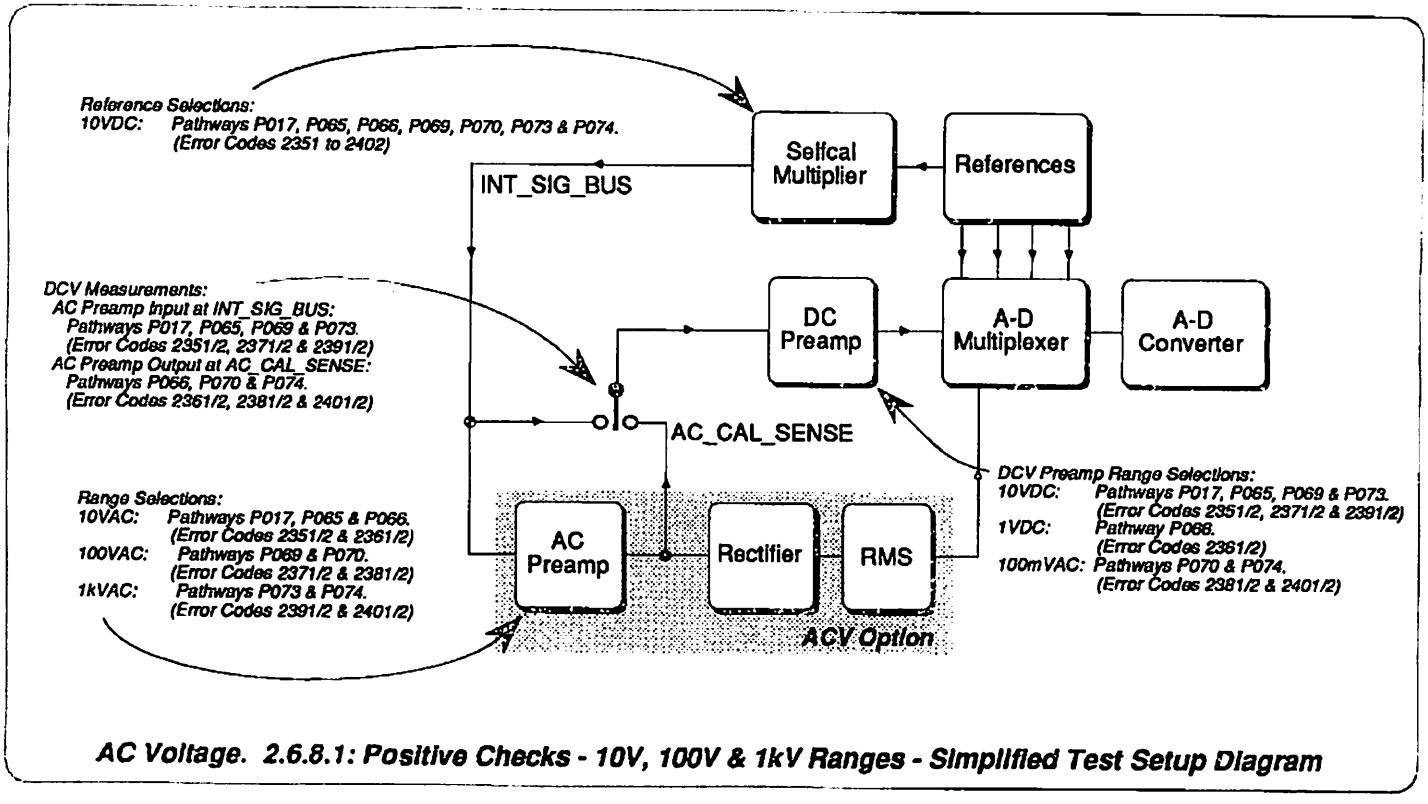
P077 **100mV AC Range - +100mV DC Input Checks**
Input: +100mVDC to AC Preamp set to 100mVAC Range.
Measure: Input using 100mV DC Range at INT_SIG_BUS.
No. of Readings: 8 Discarded; 8 Processed.

| | | |
|---|---|---|
| 2331 | Input Noise | Standard Deviation ≤ 20ppm of FS |
| 2332 | Input Magnitude | +1.70 < Mean Signal < +2.00 |

P078 **100mV AC Range - +100mV DC Input - Checks at AC Preamp Output**
Input: +100mVDC to AC Preamp set to 100mVAC Range.
Measure: Preamp Output using 1V DC Range at AC_CAL_SENSE.
No. of Readings: 2 Discarded; 32 Processed.

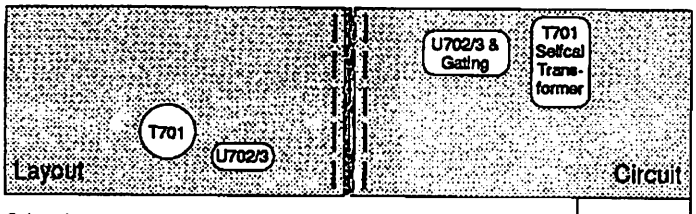
| | | |
|---|---|---|
| 2341 | Preamp Output Noise | Standard Deviation ≤ 50ppm of FS |
| 2342 | Preamp Output Magnitude | -2.00 < Mean Signal < -1.70 |

**Test Setup Model**



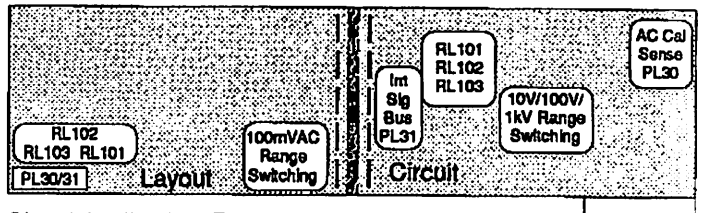

***AC Voltage. 2.6.8.1: Positive Checks - 10V, 100V & 1kV Ranges - Simplified Test Setup Diagram***

**Volume 2 References**



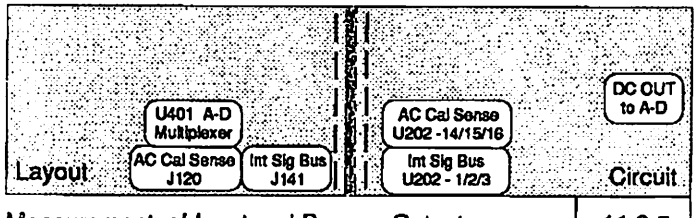

Stimulus

*11.2-8*




Signal Application, Range Selection and Preamp Output Sensing

*11.5-1/5*




Measurement of Input and Preamp Output via DC Voltage Ranges

*11.2-5*

## List of Positive Measurements (Contd.)

### 10V AC Range

P017 **10V AC Range - Settling Time**
Input: +10VDC to AC Preamp set to 10VAC Range.
Measure: Input using 10V DC Range at INT_SIG_BUS.
No. of Readings: 0 Discarded; 8 Processed then Discarded to generate settling time.

| | | |
|---|---|---|
| | Measure and Discard | — (settling) |

P065 **10V AC Range - +10V DC Input Checks**
Input: +10VDC to AC Preamp set to 10VAC Range. Measure: Input using 10V DC Range at INT_SIG_BUS.
No. of Readings: 8 Discarded; 8 Processed.

| | | |
|---|---|---|
| 2351 | Input Noise | Standard Deviation ≤ 20ppm of FS |
| 2352 | Input Magnitude | +0.94 < Mean Signal < +1.02 |

P066 **10V AC Range - +10V DC Input - Checks at AC Preamp Output**
Input: +10VDC to AC Preamp set to 10VAC Range.
Measure: Preamp Output using 1V DC Range at AC_CAL_SENSE.
No. of Readings: 2 Discarded; 8 Processed.

| | | |
|---|---|---|
| 2361 | Preamp Output Noise | Standard Deviation ≤ 50ppm of FS |
| 2362 | Preamp Output Magnitude | -1.02 < Mean Signal < -0.95 |

### 100V AC Range

P069 **100V AC Range - +10V DC Input Checks**
Input: +10VDC to AC Preamp set to 100VAC Range. Measure: Input using 10V DC Range at INT_SIG_BUS.
No. of Readings: 8 Discarded; 8 Processed.

| | | |
|---|---|---|
| 2371 | Input Noise | Standard Deviation ≤ 20ppm of FS |
| 2372 | Input Magnitude | +0.94 < Mean Signal < +1.02 |

P070 **100V AC Range - +10V DC Input - Checks at AC Preamp Output**
Input: +10VDC to AC Preamp set to 100VAC Range.
Measure: Preamp Output using 100mV DC Range at AC_CAL_SENSE.
No. of Readings: 2 Discarded; 16 Processed.

| | | |
|---|---|---|
| 2381 | Preamp Output Noise | Standard Deviation ≤ 50ppm of FS |
| 2382 | Preamp Output Magnitude | -1.02 < Mean Signal < -0.94 |

### 1kV AC Range

P073 **1kV AC Range - +10V DC Input Checks**
Input: +10VDC to AC Preamp set to 1kVAC Range. Measure: Input using 10V DC Range at INT_SIG_BUS.
No. of Readings: 8 Discarded; 8 Processed.

| | | |
|---|---|---|
| 2391 | Input Noise | Standard Deviation ≤ 20ppm of FS |
| 2392 | Input Magnitude | +0.94 < Mean Signal < +1.02 |

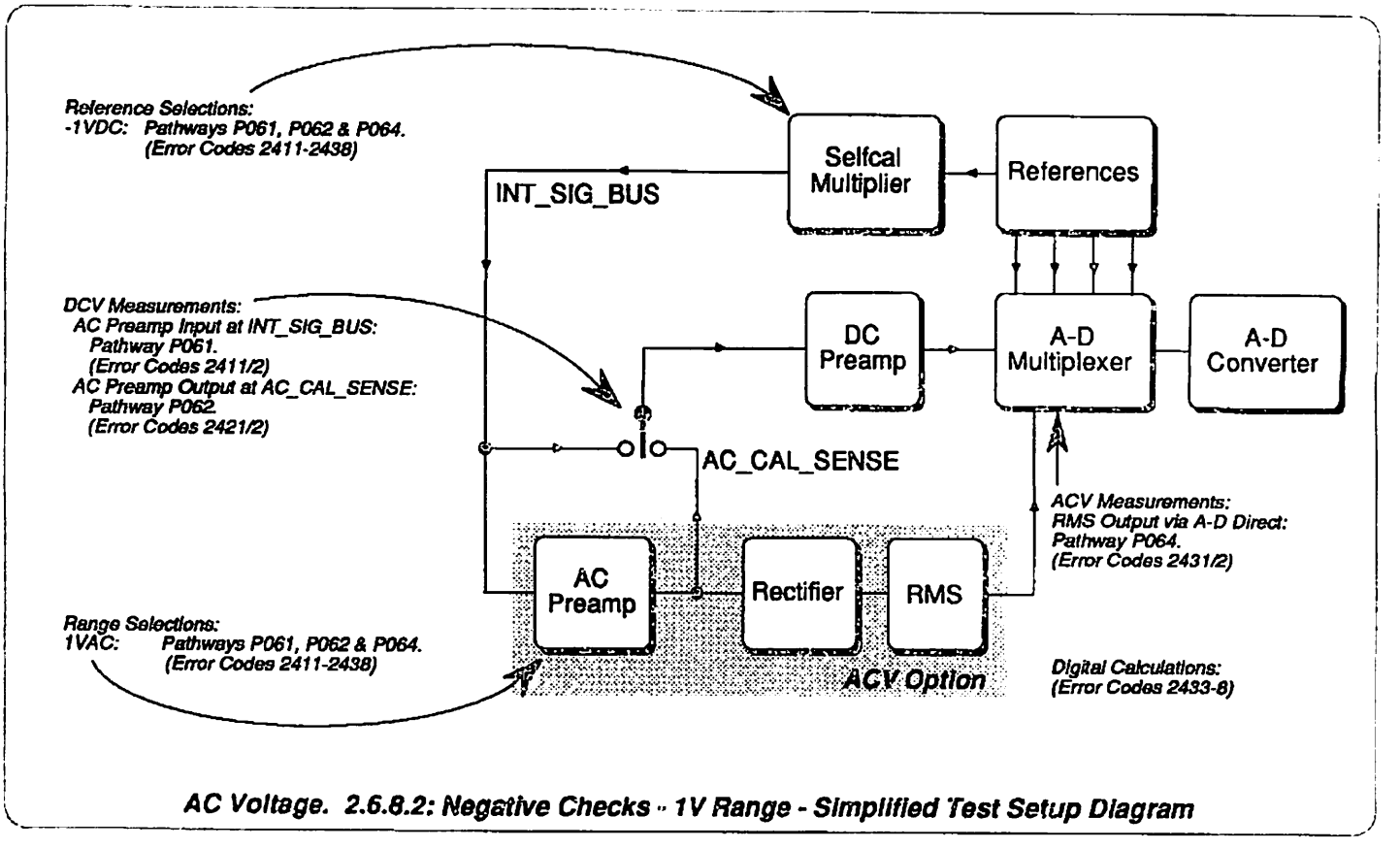
P074 **1kV AC Range - +10V DC Input - Checks at AC Preamp Output**
Input: +10VDC to AC Preamp set to 1kVAC Range.
Measure: Preamp Output using 100mV DC Range at AC_CAL_SENSE.
No. of Readings: 2 Discarded; 16 Processed.

| | | |
|---|---|---|
| | Preamp Output Noise | Standard Deviation ≤ 50ppm of FS |
| 2402 | Preamp Output Magnitude | -0.2017596 < Mean Signal < -0.1862397 |

## 2.6.8 AC Voltage Tests (Contd.)

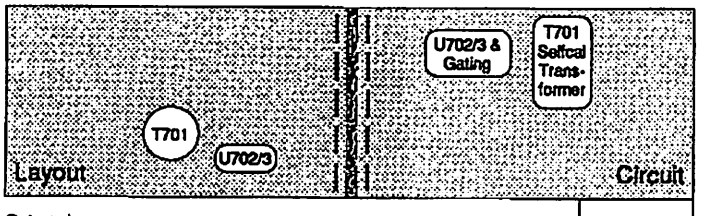
### 2.6.8.2 Negative Tests

**Test Setup Model**

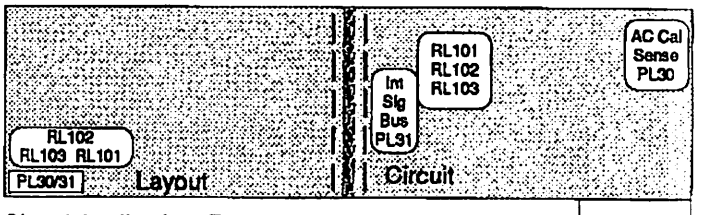



*AC Voltage. 2.6.8.2: Negative Checks - 1V Range - Simplified Test Setup Diagram*

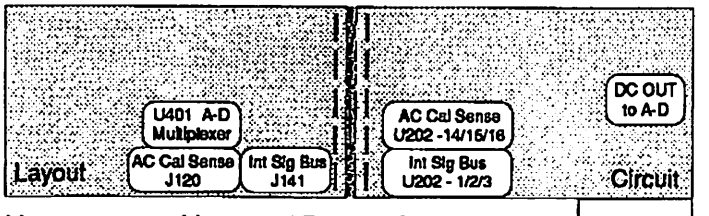
**Volume 2 References**



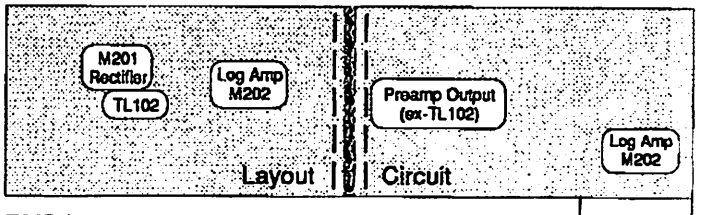

Stimulus *11.2-8*



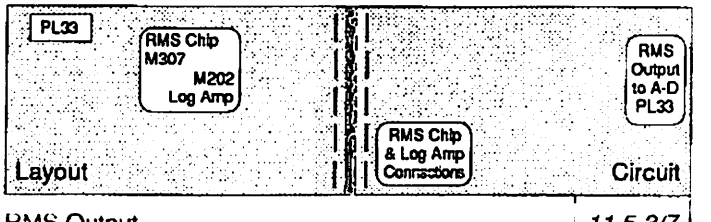

Signal Application, Range Selection and Preamp Output Sensing *11.5-1/5*




Measurement of Input and Preamp Output via DC Voltage Ranges *11.2-3*




RMS Input *11.5-2/6*




RMS Output *11.5-3/7*

## 3.7.2 Low Voltage Transformer Assembly

*To fit a low voltage transformer after removal, an M3 torque spanner capable of setting to 3Nm is required.*
*For early versions: to refit requires a length of double-sided adhesive tape.*

- Remove rear corner blocks, top and bottom covers: 3.4.1 and 3.4.2.

- **Removal**

*(Page 11.1-1, Drawing DA400891 Sh. 2)*
*(Facing page 11.1-4, Drawing DA400893 Sh. 1)*
*(Page 11.1-5, Drawing DA400893 Sh. 4)*
*(Page 11.1-8, Drawing 480750 Sh. 1)*
*(Facing page 11.4-2, Drawing DA400901 Sh. 1)*

a. Ensure that the instrument is inverted.

b. Identify the Low Voltage Transformer in the center of the sub-chassis at the rear of the instrument.

c. Identify the **green/yellow** ground bonding lead from the low voltage transformer to the bonding point between the power input plug and the power fuse, on the sub-chassis.

d. Remove the nut from the bonding point and remove the green/yellow lead identified in (c) above. Replace the nut to retain the other bonding leads.

e. Turn the instrument to its upright position and disconnect the Molex sockets of the two low voltage transformer cables from PL5 and PL6 on the Digital PCB Assembly. Carefully feed the cables and sockets back through the gap at the end of the sub-chassis, to the same side as the transformer.

f. Identify the two white 'guard' bonding leads from J103 at the rear of the DC PCB to the two rivetted bonding points on the rear of the guard box and the tongue of its horizontal screen.

g. Disconnect the Molex socket of the low voltage transformer cable from J103 on the DC PCB Assembly.

h. On the free socket, use a miniature screwdriver to extract the two pins of the leads identified in (f) above from the Molex socket:

Press the screwdriver into the pin's slot in the socket body to release the pin latch, while gently pulling the lead and pin out. When refitting, providing it has not been strained, the latch tongue will snap into place when the pin is pushed home.

j. Stand the instrument on its right side. Carefully feed the cable and socket back through the cutout in the guard box screen to the same side as the transformer.

k. Return the instrument to its inverted position.

l. Release one end of the perspex cable retainer, by pressing the peg in the center of the plastic split pin and withdrawing the pin. Lift the cable and socket out of the cutout, and re-secure the retainer in position using the split pin.

m. Remove the two M3 nuts and shakeproof washers which attach the low voltage transformer to the sub-chassis studs.

*Note: In early versions the transformer is secured using long M3 countersunk screws, which are inserted from the upper side of the sub-chassis, and screwed into nuts encapsulated in epoxy resin in the transformer body. Access to the screwheads is more difficult in this case, as the rear panel, the digital assembly, and the insulating card on the upper surface of the sub-chassis must be removed to expose the screwheads. Double-sided adhesive tape is required to secure the card after refitting a low voltage transformer.*

n. Carefully lift out and remove the low voltage transformer, cables and leads.

- **Fitting**

a. Reverse the dismantling procedure. Pay particular attention to the following points:

i. Take care not to trap any wiring when fitting the transformer.

ii. Tighten the transformer securing nuts to a torsion of 3Nm using a torque spanner.

iii. For some early versions, double-sided adhesive tape is required to secure the insulating card on the upper surface of the sub-chassis after refitting a low voltage transformer.

iv. Carry out a final inspection to ensure that the components are correctly fitted. Check that the wiring is set in the correct routing, is not trapped, and the connections are mechanically secure.

# SECTION 4 SERVICING

## 4.1 Routine Servicing

The only routine servicing required under normal conditions is the replacement of the Lithium battery which powers the non-volatile calibration memory.

The calibration requirements after changing the battery are different depending on whether the change was done with power off or with power on. These requirements are summarized in the table below.

**Summary**

**After Battery Change**

| Servicing and Time Interval | Procedure Section 4 | Calibration Required | Calibration Procedure |
|---|---|---|---|
| **Change the Internal Battery with Power On** | | | |
| Not greater than 5 years | 4.3 | Routine External Cal | User's Handbook Sect 8 |
| | | Internal Source Cal | User's Handbook Sect 8 |
| **Change the Internal Battery with Power Off** | | | |
| Not greater than 5 years | 4.3 | Special Cal | Sect. 1.4 |
| | | Routine External Cal | User's Handbook Sect 8 |
| | | Internal Source Cal | User's Handbook Sect 8 |

## 4.2 Adjustment Following Replacement of PCBs

The high accuracy of this instrument demands that its internal environment remains undisturbed after calibration. Thus the manufacturer's calibration certificate is invalidated by removal of the top or bottom cover.

Section 2 gives help in locating the general area of a fault from the error code displayed after a self test. It follows that any investigation which involves access to PCBs will require that recalibration be carried out after the covers are replaced. This principle naturally extends to any PCB replacement.

It is therefore strongly recommended that before proceeding with any investigation, a user should contact the nearest Datron Servicing Center for advice or assistance.

# 4.3 LITHIUM BATTERY - REPLACEMENT

(Datron Part No. 920049)

## FIRST READ THESE NOTES!

- The lithium battery which powers the non-volatile RAM should be changed at or before 5 years from new, and at no greater than 5-year intervals thereafter.
- The following procedures assume that the instrument will remain powered-up during the operations of disconnecting the old battery and connecting the new battery. To ensure memory integrity the soldering iron used must be isolated from line ground (mains earth) by at least 50kΩ.

  External calibration with internal source characterization will be required *(User's Handbook Section 8)* because of the high accuracy of the instrument, whose internal environment will have been disturbed by removing and replacing the top cover. **Removal of either of the covers automatically invalidates the manufacturer's calibration certificate.**

  If instrument power does not remain ON during the whole of the procedure **4.3.1** (or **4.3.2** for earlier versions), disconnecting the battery will reset the calibration memory to its nominal state. This will require a **Special** Calibration to be carried out *(Section 1.4)* as well as the full External Calibration, before the instrument specification can be realized, as calibration data will be corrupted.

  It is therefore strongly recommended that the battery be changed with **Power ON**, immediately prior to a scheduled external calibration.

### 4.3.1 Digital Assembly 400901 - Procedure

a. Ensure that power ON is selected.

b. Remove the top cover *(Section 3 para. 3.4.1)*.

c. Remove the battery (refer to *Fig. 4.1*):

   i. Attach a heatsink to resistor R104 soldered to the battery positive terminal. Unsolder R104 from the battery terminal.

   ii. Attach a heatsink to the wire between the negative battery terminal and E101. Unsolder the wire from the battery terminal.

   iii. Remove the battery from its clip.

d. Observing correct polarity, reverse the procedure of step (c) to fit a new battery and solder it in.

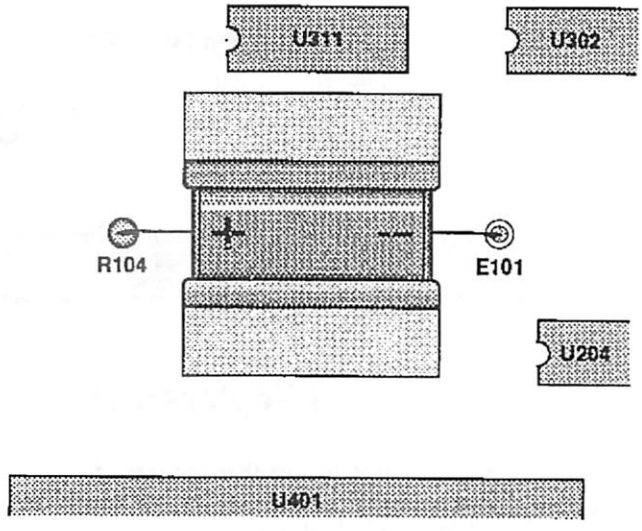



*Fig. 4.1 View of Battery from Rear of Instrument*

### 4.3.2 Digital Assembly 400740 (earlier version) - Procedure

a. Ensure that power ON is selected.

b. Remove the top cover *(Section 3 para. 3.4.1)*.

c. Remove the battery (refer to *Fig. 4.1*):

   i. Unsolder the wire from the positive battery terminal.

   ii. Attach a heatsink to R73. Unsolder R73 from the negative battery terminal.

   iii. Remove the battery from its clip.

d. Observing correct polarity, reverse the procedure of step (c) to fit a new battery and solder it in.

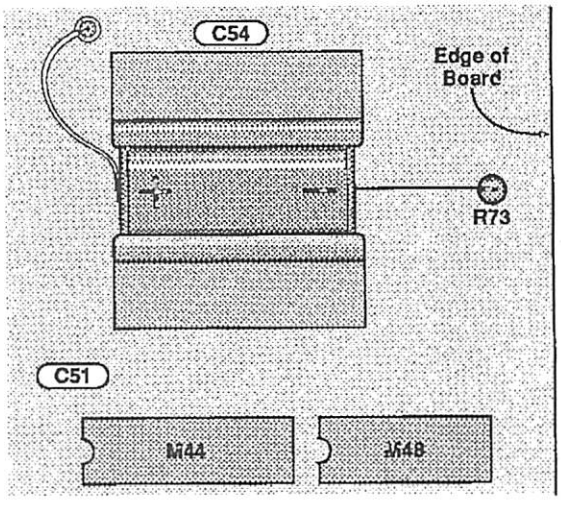



*Fig. 4.2 View of Battery from Rear of Instrument*

### 4.3.3 Return to Use

a. Refit the top cover *(Section 3 para. 3.4.1)*.

b. If the instrument power was turned off during the battery-change procedure, carry out the **Special** Calibration detailed in Section 1.4.

c. Carry out **Full** Routine Recalibration with Internal Source Characterization *(User's Handbook Section 8)*.

# SECTION 5
# TECHNICAL DESCRIPTIONS

# SECTION 5 TECHNICAL DESCRIPTIONS

## 5.1 Principles of Operation

### 5.1.1 Simplified Block Diagram

Figure 5.1.1.1 illustrates the general functions and signal flow within the 1271.

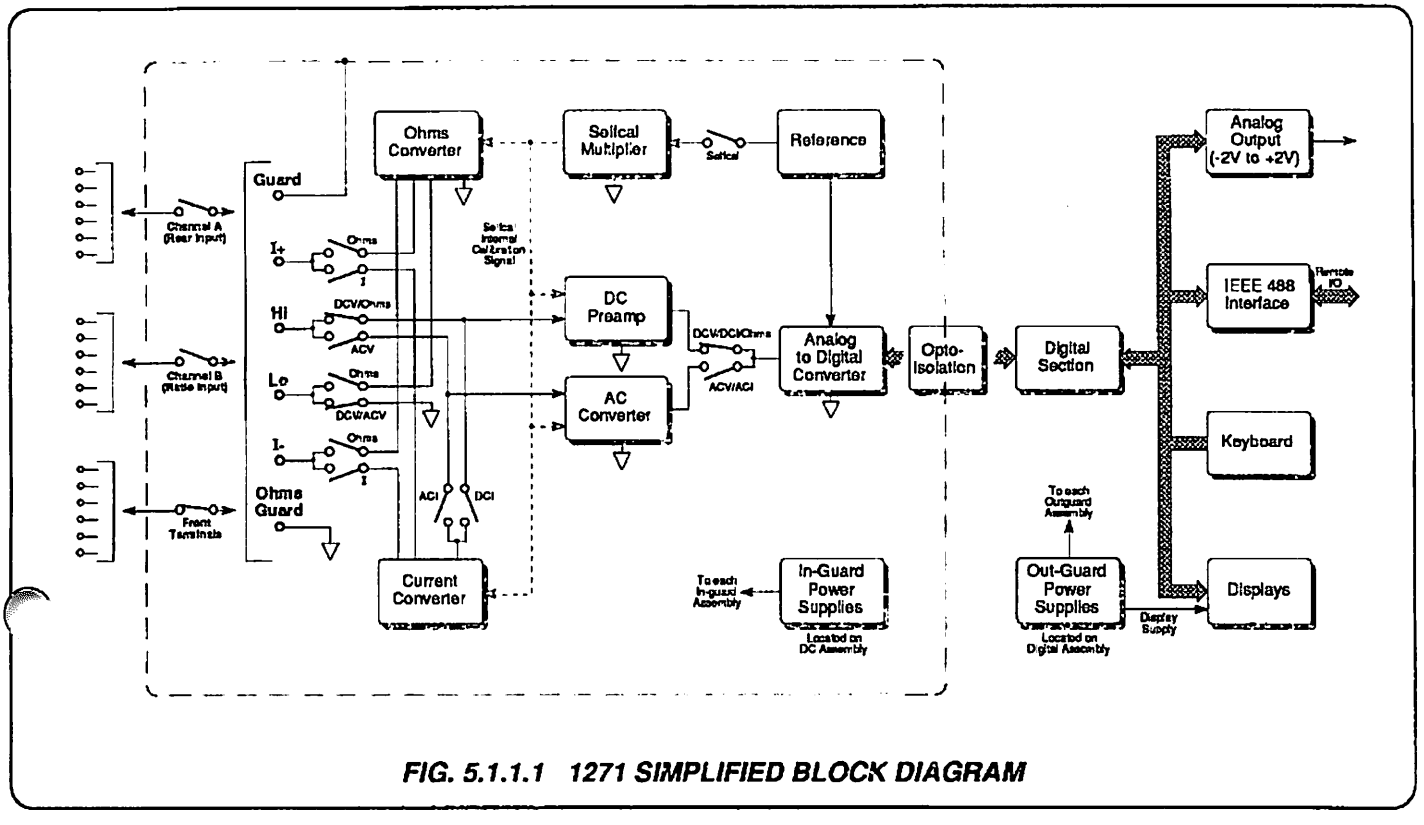



*FIG. 5.1.1.1 1271 SIMPLIFIED BLOCK DIAGRAM*

### 5.1.2 General Description

**The Datron 1271** is a premium digital multimeter, designed for the system specialist, with performance optimized for military and aerospace test applications. Its low drift and low temperature coefficients are derived from the inherent qualities of critical accuracy-defining components, which are selected and conditioned before assembly. Conditioning continues after assembly, and further checks are performed to ensure that the instrument as a whole performs well within its specification.

The 1271 employs a method of internal calibration which is designed to enhance performances across the entire range of its functions. After characterizing a low-drift/low-TC internal reference immediately following external calibration, the instrument can be regularly self-calibrated to extend its performance (maintaining approximately 90-day accuracies) up year from external calibration.

The instrument is electrically split into two sections divided by ground and guard planes. Measurement circuits are 'in guard'; whereas control circuits and display functions are 'out guard'. Front and rear inputs are routed directly to the measurement circuitry, which includes the multi-slope A-D converter.

Digital computation circuits are out of guard; but digital control of some forty separate in-guard analog parameters, together with transfer of raw digital readings from the A-D converter and any messages from the analog circuits, are effected via a serial interface whose data and control lines are passed in and out of guard through opto-isolators.

#### 5.1.2.1 DC Voltage

The input signal is switched to a DC preamp which amplifies or attenuates the analog signal to a level compatible with the requirements of the Analog to Digital converter. The amplifier is also used to measure resistance and current (Options 20 and 30).

#### 5.1.2.2 Option 10 / Option 12 - AC Voltage

AC voltages are conditioned by the AC preamp, which can be switched to measure AC-only or AC+DC signals. The preamp output is rectified by a precision full-wave rectifier, then passed to an electronic RMS converter which produces a DC level representative of the RMS of the applied signal. This DC level is then digitized by the A-D.

The RMS converter can be switched to provide an AC to DC transfer measurement. This involves sampling and holding the RMS output, and recirculating it twice to obtain a correction for the RMS Converter gain.

#### 5.1.2.3 Option 20 - Resistance

A constant current is passed through the resistor under test. The voltage developed across it due to the current is measured using the DC voltage circuits of the instrument. A wide range of constant currents and DC voltage ranges is employed to optimize performance for differing external conditions.

A 'True Ohms' facility can be programmed which takes two readings: the first is of the resistance plus the DC offset across the resistor with the current flowing; the second is of the DC offset alone with the current off. Subsequent digital calculations subtract the second reading from the first, to eliminate the effects of the DC offset, and the result is presented as the 'True Ohms' measurement.

#### 5.1.2.4 Option 30 - DC and AC Current

*(Option 10 is required for AC Current)*

The unknown current is passed through precision internal shunts and the DC or AC voltages developed across them is measured using the DCV or ACV sections of the instrument. Heavy physical and electronic protection is applied.

#### 5.1.2.5 Option 40 - Ratio

*(Option 40 also provides the third input - Channel B)*

Both Channel A (the standard rear input) and Channel B are independently zeroed and separately guarded. The Ratio option gives DC/DC, AC/DC, AC/AC and Ω/Ω comparison; reference inputs up to 250V RMS can be applied, and outputs can be expressed as a ratio, a difference or a deviation.

#### 5.1.2.6 Analog to Digital Converter

The instrument's multi-slope, multi-ramp A-D converter is a third-generation development of the basic dual-slope integrator and null detector. It has inherent sub-0.1ppm linearity combined with high speed due to signal and reference being applied simultaneously. Flexibility in ramp control permits resolution (and hence speed) to be programmed from 5.5 digits at 1000 readings per second to 8.5 digits in 'Fast' mode at 1 reading per 6 seconds.

Once converted to digital form, readings are transferred out of guard via the serial interface to be managed by the instrument's microprocessor for calibration and display.

#### 5.1.2.7 Internal References

The A-D converter references are derived from specially conditioned and selected DC Reference Modules. These modules are also used as the internal sources of reference for the self-calibration process.

### 5.1.2.8 Serial Interface

**Transmission**

This is a data transfer system in which a control word is loaded into an ASIC on the digital PCB, and its bits are passed serially through a single opto-isolator into guard. The control word represents an instrument state demanded by the user, in conjunction with firmware programming.

**Control Functions**

In guard, the word is clocked serially through a set of control registers on the DCV, ACV, Ohms and Current PCBs until each bit is located in the specific register appropriate to its control function. At this time, the bits are clocked to the outputs of the registers (or clocked into ULAs to control their functions) and the analog control circuits are switched by the overall bit pattern which, in turn, also represents the demanded instrument analog state.

**Analog Data Returns**

Some in-guard registers are programmed to act as serial transmitters. In these cases the data bits presented at their inputs are clocked into the serial stream, and returned through a single opto-isolator out of guard. The serial data returning to the ASIC are assembled into messages and presented to the processor for decoding and subsequent action.

**Serial Path Circulation Errors**

The control word is transmitted in both true and complement forms; and when it ultimately returns out of guard via another single opto-isolator, circulation errors are checked by comparing it with the original construct.

**Benefits of Serial Interfacing**

Use of the serial interface allows the passage of many data bits across the guard plane, while reducing the number of opto-isolators to eight (some of these are required to control the operation of the interface). If each data bit passed through its own dedicated isolator, then not only would the volume occupied by the isolators set a severe design problem, but also the capacitive and leakage effects in such a large number of isolators would impose prohibitive coupling between in-guard and out-guard areas of the instrument.

### 5.1.2.9 Digital Circuitry

All major communication, control, keyboard and display processing is performed out of guard, managed by a MC68000 microprocessor. The 68000 is programmed in firmware, using 128k x 16 of EPROM to contain the operating program, look-up tables etc. Workspace consists of 32k x 16 of RAM, with an extra 8k x 8 of RAM permanently powered as a non-volatile memory to store calibration corrections.

# 5.2 PCB Descriptions

*N.B. The A-D section of the DC PCB is described in Sect 5.2.5.*

## 5.2.1 DC PCB

### 5.2.1.1 Input Switching

*(Circuit Diagram DC400866 sht 1 p11.2-2)*

The front channel input terminals are connected to the DC PCB at J100/101/102 on the left front of the board. Rear input Channels A and B connect to the left rear at J150/151/152 and J160/161/162 respectively.

The leads of each input channel pass through the channel's common mode choke before being subjected to input switching. To enable the instrument to the connected into a system analog bus, each channel is separately isolated by relays when not selected. Separate relays are used throughout for **HI** and **Lo** switching to reduce interaction by leakage and capacitive coupling, latching relays being employed to maintain low thermal EMFs. These aspects are shown on *page 11.2-2*.

Separate **Lo** switching (Relay K109) is necessary to accomodate the different connection required for operation in Ohms function, when the **Lo** terminals connect to the **OHMS LOW SENSE** input of the Low Follower on the Ohms PCB. The **Ω Guard** terminals are loosely coupled (K108/R102) to the main signal common 'MECCA', except in Ohms function, when they are directly connected.

The **Guard** terminals are always loosely coupled (R101) to MECCA; whereas the internal guard shields and tracks are directly connected to MECCA in **Local Guard** as shown (K107), or to the Guard terminals in **Remote Guard.**

The **BS** line from the output of the DCV Bootstrap Buffer U203 (*p11.2-3*) is connected to the screens of the **HI** and **I+** leads in the input cable loom to provide a low-impedance guard.

**AC_CAL_SENSE** is used during the AC voltage Selfcal process, and **INT_SIG_BUS** has several uses, mainly to carry internal signals when in Selfcal (*Refer to Section 2: Fault Diagnosis*).

### 5.2.1.2 Internal Signal Bus

*(Circuit Diagram DC400866 sht2 p11.2-3)*

Quad CMOS gate U202 provides switching mainly for operation in Current measurement and in Selfcal. The **INT_SIG_BUS** line is used to connect various inputs to the DC voltage measurement circuits when they are being employed to measure internal voltages, and not for voltages input from the front terminals. Relay K201 makes this selection.

The internal signal bus comes into operation when the **INTERNAL-H** signal on U202-1 is at logic-1.

The **AC_CAL_SENSE** line is connected to the bus by the **AC_SENSE-H** signal on U202-16 at logic-1.

When it is necessary to load the signal being transmitted via the internal signal bus, the 10MΩ resistor R220 is connected by the **10M_LOAD-L** signal on U202-8 at logic-Ø.

Similarly, a hard zero can be connected on the bus by the **CAL_ZERO-L** signal on U202-9 at logic-Ø.

Refer to *Section 2: Fault Diagnosis* for the occasions when these facilities are required.

### 5.2.1.3 DC Voltage Block Diagram

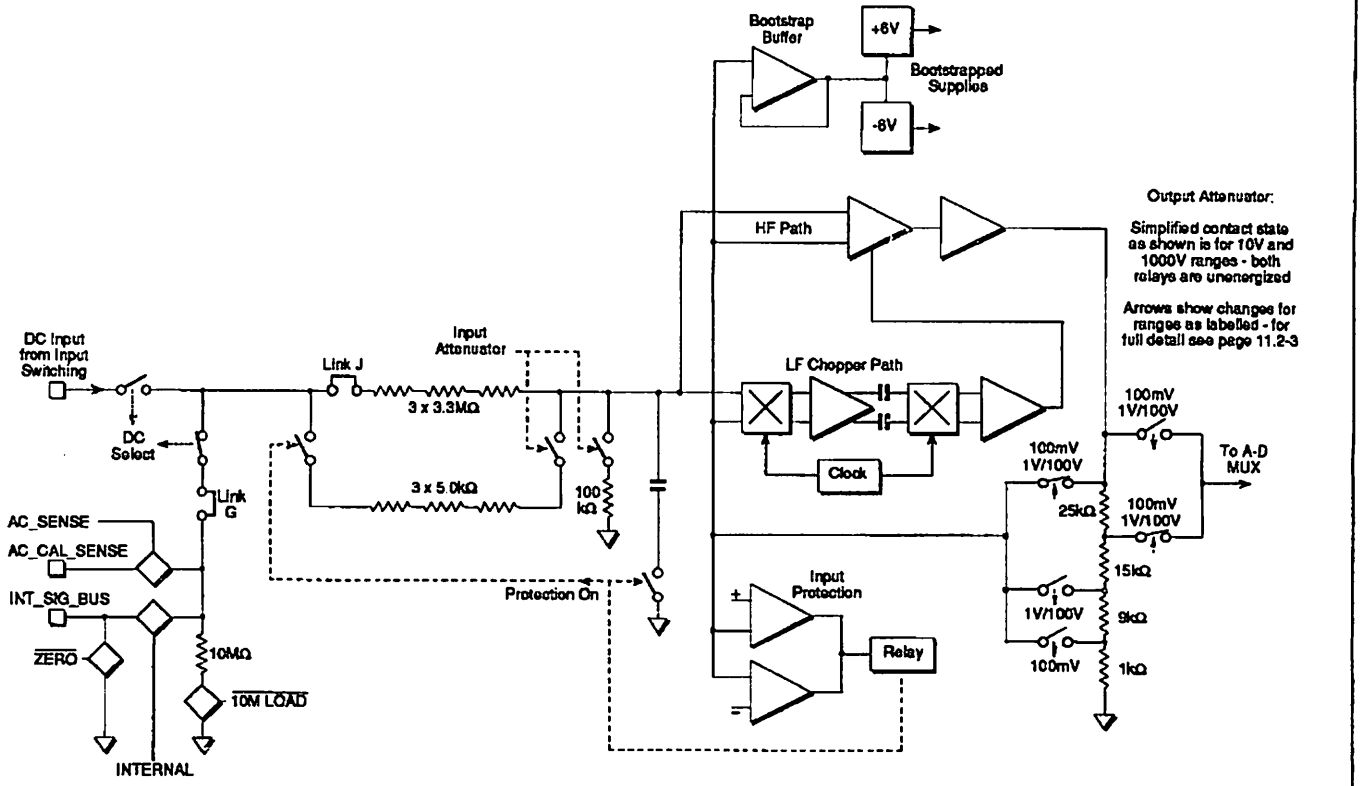



*FIG. 5.2.1.1 DC VOLTAGE PREAMPLIFIER - SIMPLIFIED SCHEMATIC*

### 5.2.1.4 DC Voltage Preamp

*(Circuit Diagram DC400866 shts 2 & 3 pp11.2-3 and 11.2-4)*

The DC Voltage Preamp is based on a chopper circuit (*p11.2-4*). The required input characteristics are achieved by splitting into LF and HF paths in a multistage design, to ensure good bandwidth and overall gain characteristics. In each path a differential FET input gives low input current characteristics.

This basic design is enhanced by employing a synchronized chopper configuration in the LF path. Noise is also reduced by this method. The signal is chopped by Q304/5/6/7 to modulate the input to differential amplifier Q308/Q309/Q310. The amplifier output signal is AC-coupled to the four U301 gates, which demodulate at the same frequency. After further amplification by U303 the demodulated signal is fed to the output driver stage.

Both paths are combined in a final amplifier stage which provides most of the forward gain with the frequency gain-compensation necessary to give an effective amplifier bandwidth of 600kHz.

### 5.2.1.5 Bootstrap Buffer

*(Circuit Diagram DC400866 sht 2 p11.2-3)*

To effect high input impedance, the DC amplifier also drives a Bootstrap buffer U203 (*p11.2-3*), which ensures that all in-guard power supplies used for the DC amplifier are made to track the input signal level by reference to Bootstrap. The DC amplifier thus sees no change in input signal relative to its supplies, so achieves very high common mode rejection, eliminating any potential common mode non-linearities. In addition, the buffer output sets the potential of PCB tracking which guards the input Hi track, to absorb PCB leakage currents that could otherwise be picked up by input Hi.

## 1.6 Range Switching

*(Circuit Diagram DC400866 sht2 p11.2-3)*

Extremely stable resistance units configure the DC amplifier gain to define the DC Voltage ranges. Two attenuators, one at the input and one at the output of the DC Preamp, are switched for range selection.

Refer to *page 11.2-10*

The output attenuator control signals, at serial interface register U902-18/17, are passed via level-shifter U907 and relay driver U908 to operate relays K204 and K205. The contacts of these relays are shown in the output attenuator on *page 11.2-3*.

The input attenuator relay K203 is controlled from U902-1 via U907 and U908. K203 contacts are shown in the input attenuator on *page 11.2-3*.

**100mV - 10V Ranges**

For these low voltage ranges, the energized relay K203 disconnects R205, so the input attenuator is not effective. K202 contacts and the remainder of K203 contacts are closed to pass the signal through the 15kΩ input chain in parallel with the 10MΩ high voltage input chain. Refer to *Fig. 5.2.1.1.*

In the **10V Range** both relays K204 and K205 are unenergized (the state shown on *page 11.2-3*). The DC Preamp is connected as a voltage follower, and the output voltage is halved in the output attenuator giving a stage gain of 0.5. Thus input voltages in the range of 0V±20V are reduced to the range 0V±10V for presentation to the A-D.

Relay K204 only is energized for the **1V Range**. The feedback fraction is set at 0.2 by the output attenuator, and the Preamp output is passed without attenuation to the A-D. The stage gain is 5.0, so that input voltages in the range of 0V±2V are amplified to the range 0V±10V at the A-D input.

Relay K205 only is energized for the **100mV Range**. The output attenuator sets the feedback fraction to 0.02, and the Preamp output is passed directly to the A-D. The stage gain is 50.0, so that input voltages in the range of 0V±200mV are amplified to the range 0V±10V for input to the A-D.

**100V & 1kV Ranges**

For the high voltage ranges the 15kΩ shunt input chain is disconnected by the de-energized contacts of K203, which also connects R205; so the input attenuator reduces the input voltage by a factor of 100 ahead of the Preamp.

The feedback fraction for the **100V Range** is set at 0.2 by the energized relay K204 in the output attenuator (as for the 1V range) and the Preamp output is passed without attenuation to the A-D. The stage gain is 0.05, so that input voltages in the range of 0V±200V are reduced to the range 0V±10V at the A-D input.

In the **1kV Range** both K204 and K205 are unenergized as in the 10V range, so the DC Preamp is connected as a voltage follower and the output voltage is halved in the output attenuator giving a stage gain of 0.005. Thus input voltages in the range of 0V±1000V are reduced to the range 0V±5V for presentation to the A-D.

### 5.2.1.7 Protection

*(Circuit Diagram DC400866 sht 2 p11.2-3)*

The instrument can measure up to 1000V. It must therefore be able to withstand continuous application of 1000V on all DCV ranges, to ensure that such a voltage applied inadvertently does not damage internal components.

When the input attenuator is switched in on the 100V or 1kV ranges, 1000V at the input terminals will be reduced to 10V at the input to the DC Preamp. But on low voltage ranges the attenuator is switched out, so static and dynamic methods are used for added protection.

**Preamp Input Protection**

The obvious way to protect the Preamp non-inverting input is by a series resistor chain and two back-to-back zener diodes. The 10MΩ series element of the input attenuator could be used as the resistor chain, but it would create far too much Johnson noise to be used alone for low voltage ranges. However, as its dissipation is low (100mW for an applied voltage of 1kV) it could form an efficient limiter if it were switched in only when the low voltage ranges are in overload. This is the method chosen for the 1281, using the shunt 15kΩ chain for normal operation. It will activate the back-to-back zeners for an overload greater than 24V at the Preamp input while preventing problems due to Johnson noise. But it is practicable only in the short-term as it will develop some 60W of heat for an applied voltage of 1kV.

To effect the changeover from the 15kΩ operating chain to the 10MΩ limiting chain, the non-inverting input to the Preamp needs to be sensed for overload. As the Bootstrap Buffer is already connected to the inverting input, it provides a suitable low impedance output (B) which follows the input. This is applied to a window comparator U201 which de-energizes K202 only when the overload threshold of 21V is exceeded. Under non-overload conditions K202 is energized, holding the two chains in parallel; but for overload conditions the K202 contacts disconnect the 15kΩ chain.

**Protection against High-Voltage HFAC and Transients**

As the Bootstrap is designed not to follow high frequencies and transients, it is necessary to couple these into the comparator from the input. This is done by R201 and C201, with zeners D203/4/5/6 clamping the comparator inputs to 0V±22V. The time constant of R217/R218/C203 ensures that when the comparator de-energizes K202 due to a transient, it cannot be re-energized before its contacts have changed over.

**Preamp Output Protection**

As Bootstrap is driven from the feedback point it is vital that the two inputs of the Preamp remain at the same potential. Once the input and Bootstrap are clamped to 24V by the two back-to-back zeners, the Preamp output could lock up due to loss of Bootstrap (and hence collapse of the Preamp's bootstrapped supplies). The Preamp therefore has two clamps: a relative clamp between the output and inverting input to hold these points within 12V of each other, and an absolute limiter as the output approaches the 35V rails.

**Guarding**

The input zeners and output clamps are guarded out by Bootstrap to prevent clamp leakage causing inaccuracies during normal operation.

### 5.2.2 AC PCB - Options 12 and 10

## 5.2.2 AC PCB - Options 12 and 10

*N.B. References to the Volume 2 of this handbook are aimed at the high accuracy option: Option 12. Where there are differences between Option 12 and the high speed Option 10; these are noted at the appropriate point in the text, and a reference to the Option 10 drawing is also given.*

### 5.2.2.1 AC Voltage - General Principles

The preamplifier buffers and ranges the signal in order to present its output to the RMS to DC converter at the required voltage levels.

Once converted to an equivalent DC signal, it is applied to the main A-D converter on the DC PCB.

The description is based on Option 12, so differences for Option 10 are pointed out within the text. Generally, Option 12 is optimized for accuracy, and Option 10 for speed of operation. The AC hardware is different for the two options; Transfer mode is made available in Option 12, but not in Option 10.

### 5.2.2.2 AC Preamp

*(Circuit Diagram 430741 sht1 pl15-5)*

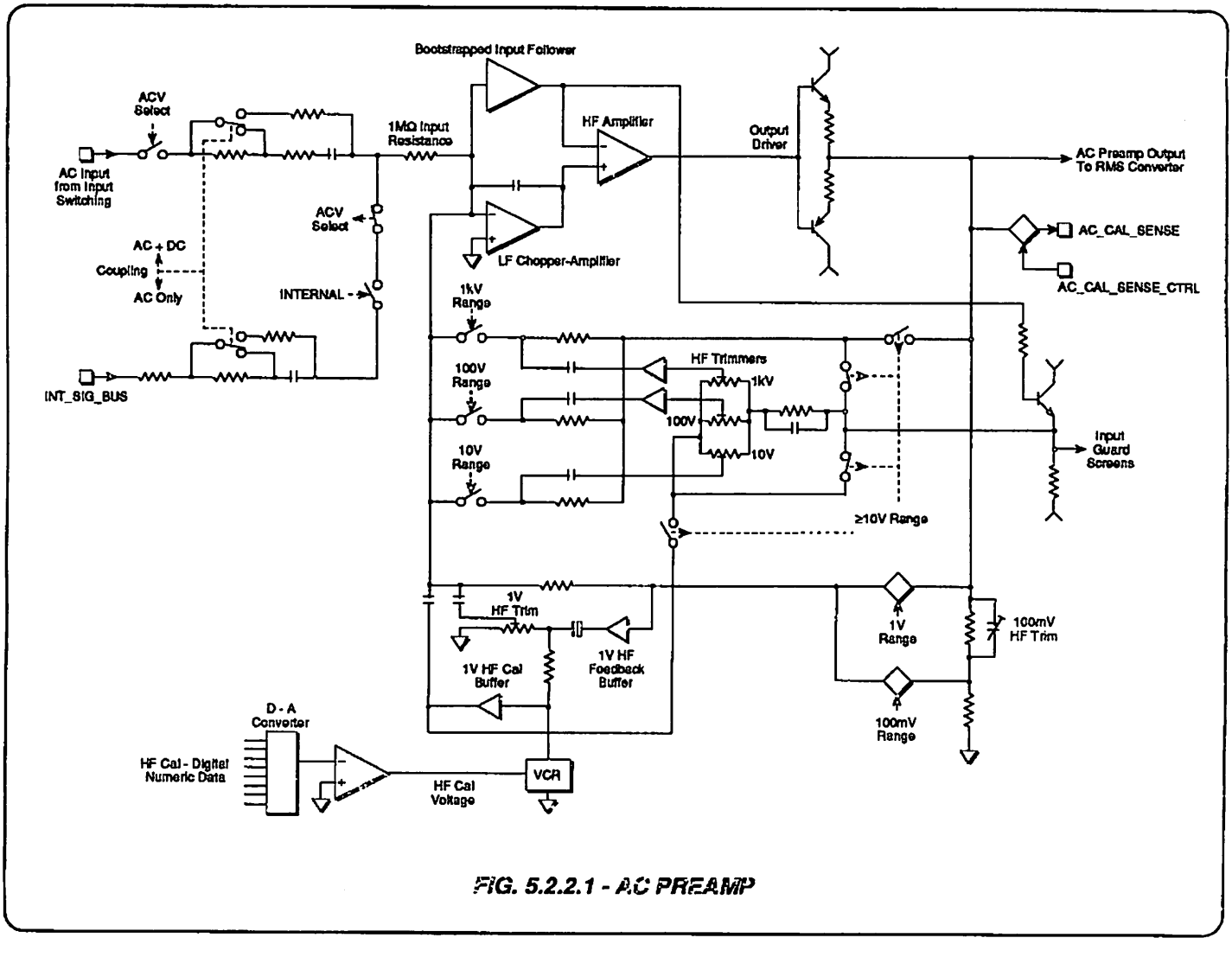



*FIG. 5.2.2.1 - AC PREAMP*

The requirement for the inverting preamp is to provide good flatness from DC to 1MHz, while the offset voltage at its output must be minimized to ensure good DC-coupled performance. This complex design uses several gain elements in conjunction with each other.

### Inputs

For normal ACV operation, the input **HI** is fed from the DC PCB at PL32-4. Relay RL101 connects **HI** to an AC/AC+DC changeover network, and ensures that the INT_SIG_BUS is disconnected from the input to the Preamp. RL102 performs the changeover by shunting the AC coupling capacitor C101 when AC+DC is selected.

During AC Current operation or Selfcal, RL101 disconnects **HI**, and connects the **INT_SIG_BUS** to the Preamp input instead. A second AC/AC+DC changeover network is switched by RL102 for use in these modes.

### Low Frequencies

As the Preamp is an inverting amplifier, the closed loop gain at low frequencies is set by input and feedback resistance. The input resistance of 1MΩ is formed by four 250kΩ resistors in a series chain, spreading the input voltage and power on the 1kV range, and permitting simple compensation at high frequencies. This input chain is present on all AC Voltage ranges.

Feedback resistance is switched to select voltage ranges. The basic range is the 1V range with an overall gain of 1, using two 500kΩ resistors in series as feedback. FET Q116 is switched on for all ranges except the 100mV range. For the 100mV range, the feedback is divided in the ratio 1:10 by R186/R187 by switched Q116 off and Q117 on, still using the 1V range resistors to feed back to the input.

For the three higher voltage ranges, relay RL107 connects the preamp output to the three feedback resistors. For the 10V range, feedback resistor R168 is effectively connected in parallel with the 1V range feedback resistance R148/R169 by relay RL106. For the 100V range, feedback resistor R167 is added in parallel with the combined 10V range feedback resistance by relay RL105; and for the 1kV range, RL104 adds R191 in parallel with the combined 100V feedback resistance. As the 1kV range has both a full range and full scale of 1kV, it is not necessary to reduce the gain to .0001. Using the larger value of 2.4kΩ for R191 gives an overall gain of approx .0019, reducing the value of the required compensation capacitor. The 1kV range thus behaves internally as though it were a 500V range with 100% overrange.

### High Frequencies

The feedback resistors are shunted by compensating capacitors which determine the closed loop gain at high frequencies, swamping the stray capacitance around the preamp. Trim resistors allow the compensation to be pre-set once the AC PCB is fitted into its guarded environment in the instrument. Voltage followers M103 buffer the HF feedback drive on the 100V and 1kV ranges, which have lower-value feedback resistors and hence larger compensation capacitors.

FET Q115 and transistor Q120 form an HF feedback buffer for the 1V and 100mV ranges. After DC isolation by electrolytic C140, the buffered output is trimmed by pot R178 and fed back via C148. The buffered output also energizes the HF autocalibration voltage divider formed by R174 and VCR FET Q119.

### LF Autocalibration

The low frequency gain is calibrated by correcting the digital output from the A-D while inputting a known signal. The corrections are stored digitally in non-volatile RAM, and are subsequently reapplied by digital computation during normal operation.

### HF Autocalibration

To calibrate the HF gain, separate digital correction factors are derived from measurements of known HF inputs, and reapplied as a DC voltages to M104 via a ladder network D-A converter R189. The HF correction factor for the currently-selected range is passed from the microprocessor to the AC PCB via the serial interface, latched into M402 (page *11.5-8)*, and delivered direct to the D-A R189 *(page 11.5-5)*.

The output of M104 controls FET Q119, which acts as a voltage-controlled resistor. The buffered and isolated preamp output voltage is developed across R174 and Q119, and the voltage across Q119 is applied via Q118 and C147 to the preamp input. Thus the correction factor embodied in the bit pattern on the input to the D-A R189 controls the amplitude of the HF feedback and hence the HF gain of the preamp.

FET Q114 is included to compensate for any non-linearity in FET Q119, the two FETs forming a matched pair, with common-value bias resistors. Thus the source-drain currents in both FETs are identical, the amplitude of the AC voltage across Q119 is linearly proportional to the resistive current from the D-A to M104 input, and hence is also proportional to the quantative value of the bit pattern delivered to R189.

### Selfcal

For self-calibration and self-testing purposes, the internal DC Source can be characterized during external calibration. During Selfcal, the appropriate value of DC reference is applied via the INT_SIG_BUS line, and the AC+DC gain of the preamp is measured by the DC voltage system via the AC_CAL_SENSE line. Further measurements are taken from the output of the RMS section directly via the A-D.

### 5.2.2.3 Electronic RMS

The principles behind the RMS conversion technique are shown in Fig. 5.2.2.2.

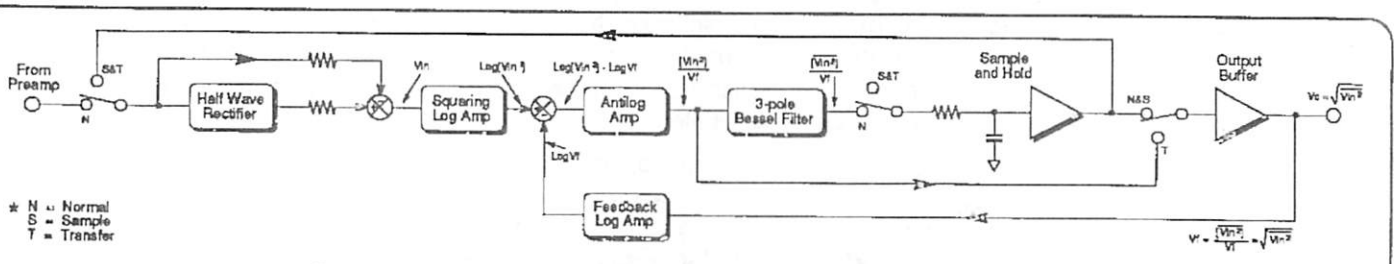



FIG. 5.2.2.2 - PRINCIPLES OF ELECTRONIC RMS CONVERSION

#### Rectifying the Preamp Output

With the instrument set to its 'Normal' mode, and for the first of three readings when using the 'Transfer' facility; the output signal from the Preamp is applied to the Precision Rectifier. This is required to provide full-wave rectification with identical AC and DC gain for both positive and negative excursions, and to ensure that the crest factor of sinusoidal and non-sinusoidal signals is not altered in the process.

To achieve this, positive excursions are removed by half-wave rectification, the negative excursions being inverted by the rectifier. The amplitude of the rectifier output can be adjusted using the DC-to-DC Turnover control, which incrementally changes the rectifier gain around a factor of 2. The rectifier output is then summed with the Preamp output. The result, shown in Fig. 5.2.2.3 for a sine waveform, is a full-wave signal which can be set to give identical gain on both positive and negative excursions. This is input to the squaring log amp (as Vin).

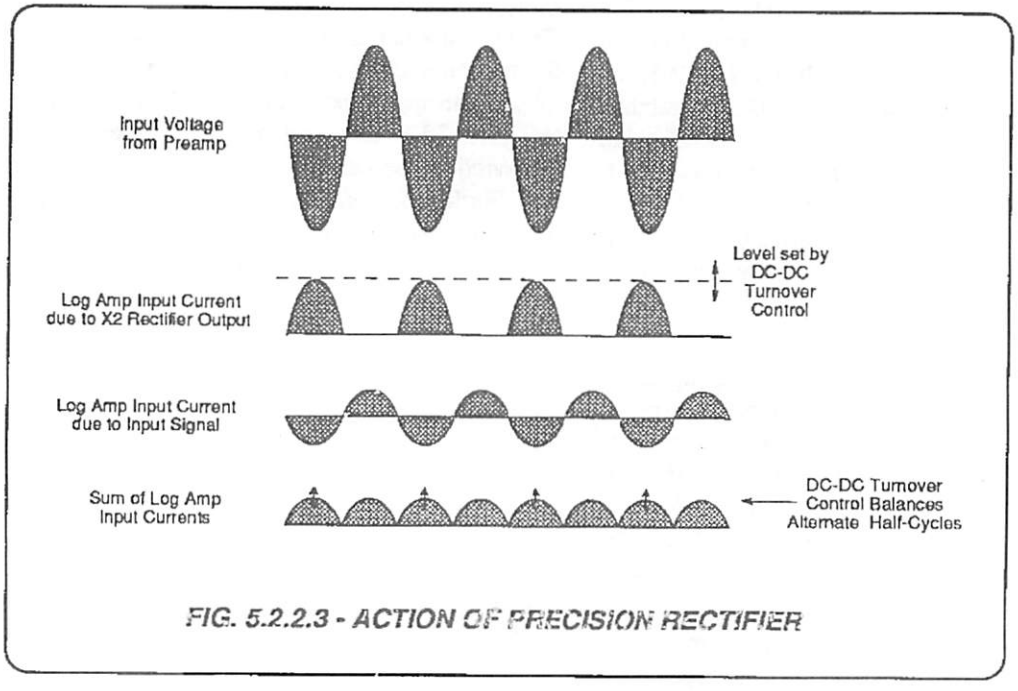



FIG. 5.2.2.3 - ACTION OF PRECISION RECTIFIER

### Squaring the Rectified Input

The Log Amp squares instantaneous values of Vin, by converting them into logarithmic values and then multiplying by two. Its instantaneous log output voltage is therefore proportional to 2logVin, which can be expressed as log[Vin]2.

### Dividing by the Converter Output

The Log Amp output voltage is applied to a summing circuit, together with a feedback DC voltage whose value is proportional to -logVf (Vf is a DC voltage - the mean output voltage from the converter, returned via the feedback Log Amp). The current from the summing junction is proportional to $\log[Vin]^2$-logVf, which can be rewritten as $\log[Vin^2/Vf]$. It drives an exponential stage whose output voltage is proportional to the antilog of its input current, in this case proportional to $Vin^2/Vf$.

### Taking the Mean

The output from the exponential stage is smoothed by a 3-pole Bessel filter, resulting in a DC voltage for a settled periodic signal. This is therefore proportional to the mean of $[Vin^2/Vf]$.

As Vf is DC and therefore equal to its mean, this is the same as:

$$[\text{mean } Vin^2]/Vf.$$

### Closing the Square-Root Loop

The feedback loop is closed by feeding Vf back into the computation, as mentioned earlier, to ensure that the DC output signal $Vf = [\text{mean } Vin^2]/Vf$. From this it can be seen that $Vf^2 = [\text{mean } Vin^2]$, and $Vf = \sqrt{[\text{mean } Vin^2]}$, which is the normalized root-mean-square value of Vin.

### Normal Mode Settling

The Bessel filter is chosen for its optimum settling time, and offers selectable configurations to permit operation down to 1Hz. A sample and hold circuit with isolating buffer (for use in 'Transfer' mode - see below) provides further filtering at higher frequencies, after which the smoothed signal is taken to an amplifying buffer which drives the instrument's analog to digital converter.

### Simplified Circuitry

A simplified version of the RMS analog computing circuitry is given at Fig. 5.2.2.4. Note that the input and feedback components responsible for the logging, squaring and antilogging are contained within the 'RMS Chip'.

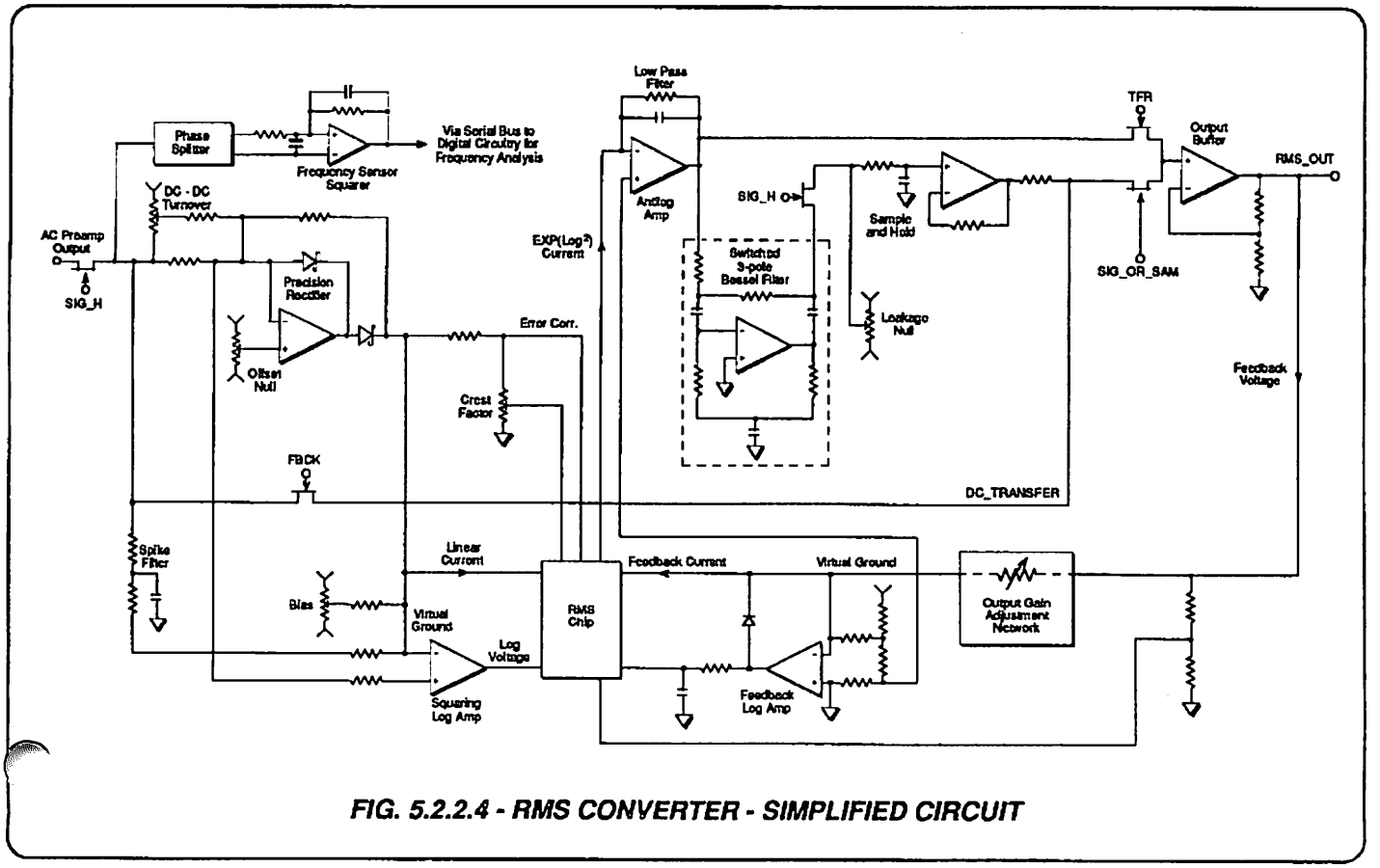



*FIG. 5.2.2.4 - RMS CONVERTER - SIMPLIFIED CIRCUIT*

### 5.2.2.4 AC-DC Transfer Mode (Not Option 10)

So far, the described circuit is a straightforward electronic RMS measuring system. As an alternative, Option 12 also employs a refinement on the basic technique, using an AC-DC transfer mechanism to improve linearity by measuring and correcting the gain of the RMS Converter.

This requires three readings, shown in Fig. 5.2.2.5 as 'Normal', 'Sample' and 'Transfer', equivalent to the switching positions shown on Fig. 5.2.2.2.

Refer to Fig. 5.2.2.5, and to Option 12 *Circuit Diagrams 430741 Sheets 2 and 3; pages 11.5-6 and 11.5-7.*

Note that on the equivalent Option 10 *Circuit Diagrams DC400870 sheets 2 and 3; pages 11.5-2 and 11.5-3*, the transfer components are not present.

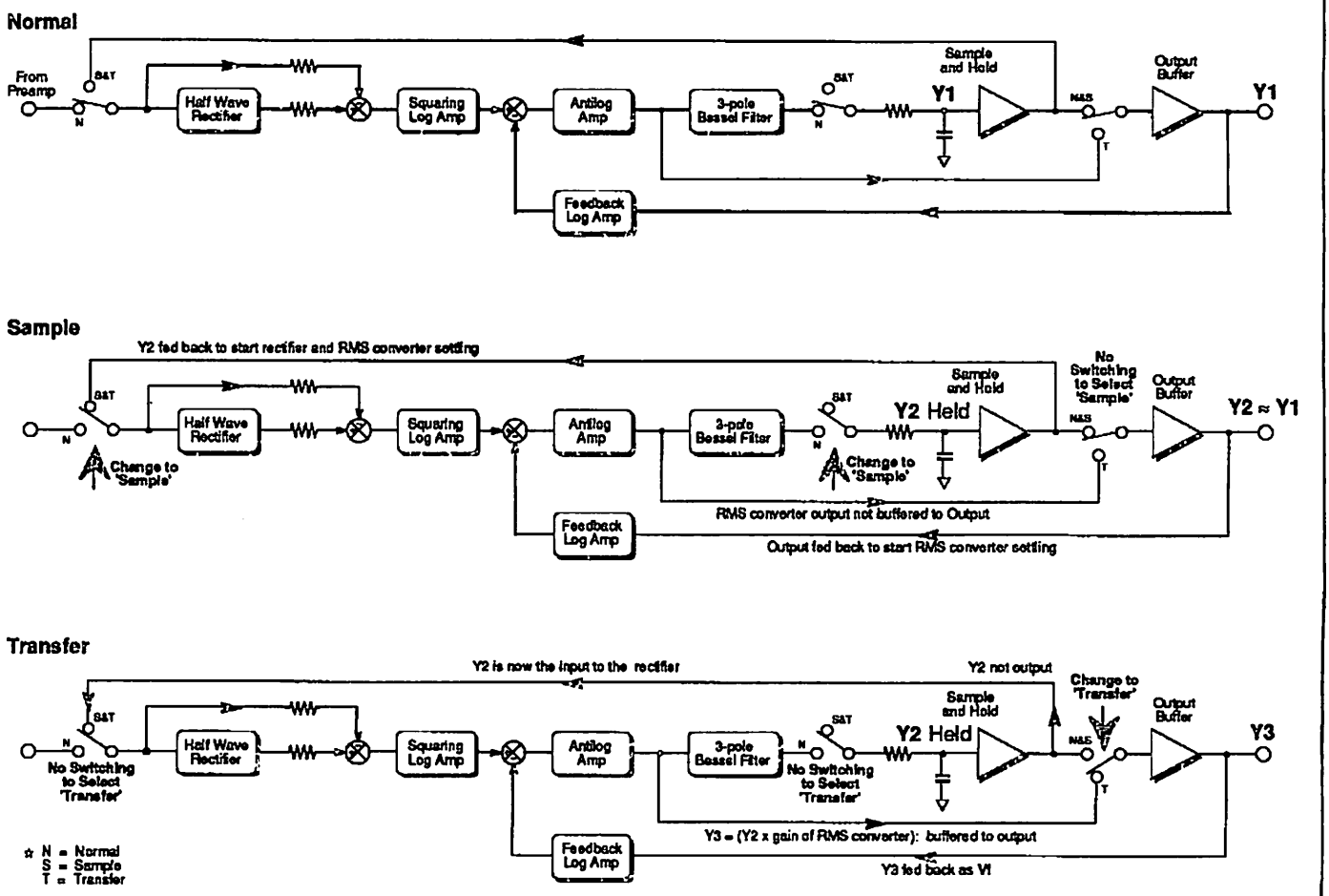



*FIG. 5.2.2.5 - OPTION 12 - TRANSFER MODE - STAGES*

**First Reading - Normal**

With the circuit connected as in Normal Mode, a reading **Y1** is taken and delivered via the A-D to the digital circuitry. This is memorized by the microprocessor. Meanwhile the Sample and Hold capacitor has charged up to Y1.

**Second Reading - Sample**

The input to the Sample and Hold circuit is removed to store the capacitor voltage. A second 'Sample' reading **Y2** is taken via the A-D. This reading is the instantaneous value at the time when the input signal was removed. It is approximately equal to Y1.

**Third Reading - Transfer**

The Sampled voltage **Y2** is passed through the RMS Converter, and the output from the Antilog Amp is measured as **Y3**.

There are now three digitally stored readings:

- **Y1:** is the fully-converted uncorrected reading of the input to the instrument;
- **Y2:** is the voltage stored on the sample-and-hold capacitor;
- **Y3:** is the result of recirculating the sample-and-hold voltage through the RMS Converter (the signal does not require filtering as it is already DC).

The second reading Y2 is necessary only because the input could have been broken at the peak or trough of the small amount of ripple which could be present. Both Y2 and Y3 are now taken with respect to the same DC voltage, so the ratio Y3/Y2 is a measure of the DC gain of the RMS Converter. To correct for the RMS Converter gain, the inverse ratio Y2/Y3 can now be applied to the raw signal Y1.

The microprocessor therefore computes the corrected reading of the input to the instrument by:

**Corrected Reading = Y1 x (Y2 / Y3)**

Because the second and third readings use only the DC sample-and-hold voltage as input, the correction is equivalent to an AC to DC conversion. Because the signal level of the DC readings is at the same level as the signal to be corrected, any gain or linearity errors in the RMS conversion are virtually eliminated.

### 5.2.2.5 Frequency Sensing and Display

*(Fig. 5.2.2.4 and Circuit Diagrams 430741 sheets 2 & 4, Pages 115-6 & 115-8)*

**Frequency Sensing**

The Preamp output is AC-coupled to differential buffer Q201 *(page 115-6)*. This provides split-phase versions of the signal to drive M409 comparator *(page 115-8)*, which squares the fundamental while suppressing harmonics. The resulting output from the comparator is passed to the FLL ULA M412.

**Counting and Encoding**

The frequency is counted by the ULA within a long or short gate initiated by the CI2_R signal. The output from the 4MHz crystal clock X401 is also counted, within the selected gate, as frequency reference. The ULA computes the frequency by comparison between the two counts, and constructs a data word representing the signal frequency. This word is placed into the ULA serial interface register and the microprocessor is alerted by the RTX_R signal that a message is ready.

**Frequency Display**

The processor then performs the necessary serial transfer to obtain the message for decoding and display. The frequency can be presented on the menu display at the same time as its RMS value is being shown on the main display, by using **Freq** in the **MONITOR** menu when **ACV** is selected. If the instrument is in **ACV SPOT FREQUENCY** mode there is also an indication when a **Spot** frequency is active.

### 5.2.2.6 Spot Frequency Calibration

Each ACV range can be spot calibrated at up to six independent user-defined frequencies, reducing flatness errors within ±10% of the spot frequency. The process is performed entirely in software, no alteration to the hardware configuration being involved.

### 5.2.2.7 AC Current Measurement

The input AC current to be measured is passed through one of the shunts on the Current PCB, and the resulting shunt voltage is transferred to the AC PCB to be measured on the 100mV range. The voltage is developed between INT_SIG_BUS and 0V(10) on the Current PCB, and appears between INT_SIG_BUS and 0V(7) on the AC PCB. Both commons are joined at MECCA on the DC PCB.

## 5.2.3 Resistance - Option 20

This function is achieved using a set of constant current sources in conjunction with the DCV measurement capability.

### 5.2.3.1 Normal Ohms - Functional Block Diagram

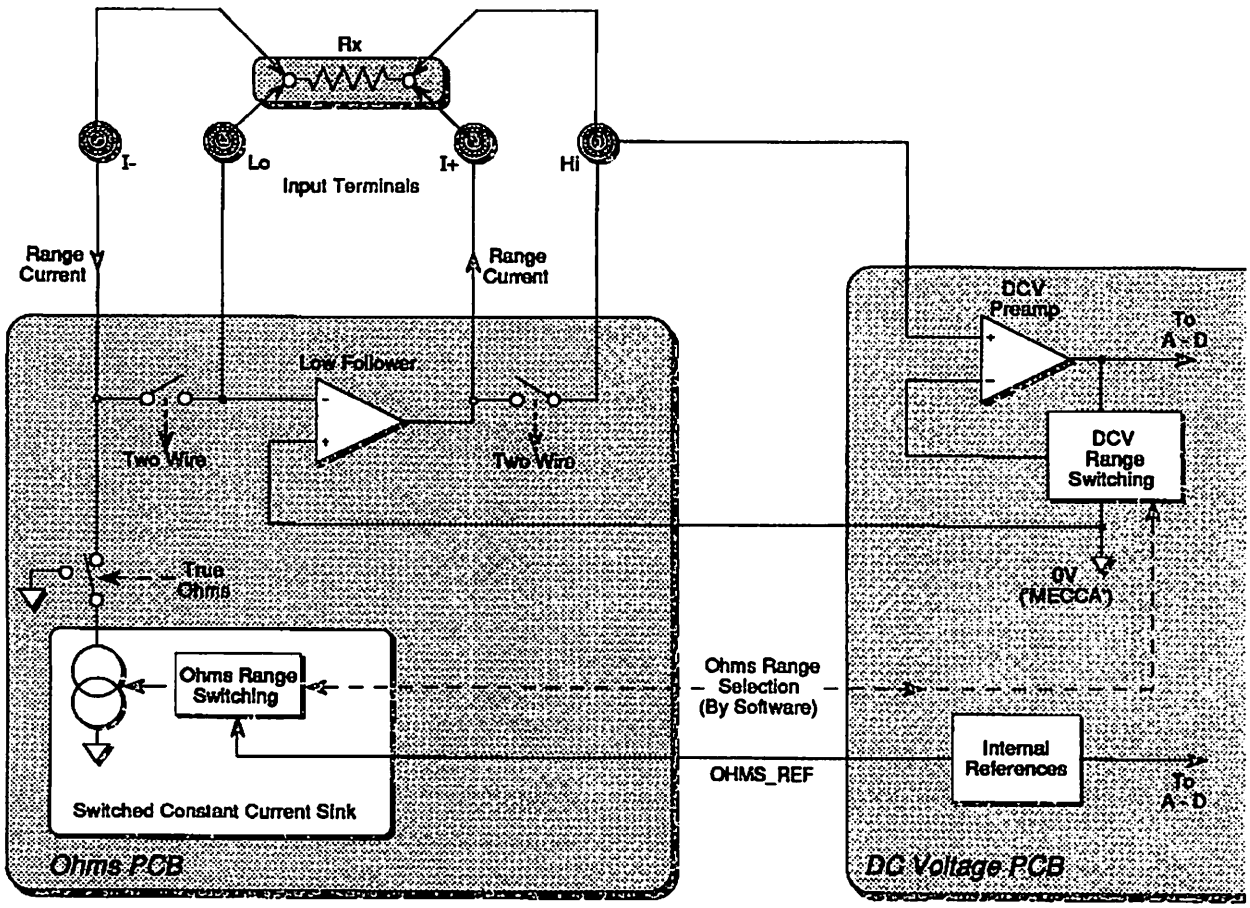



*FIG. 5.2.3.1 OHMS BLOCK DIAGRAM*

### 5.2.3.2 Switched Constant Current Sink

*(Circuit Diagram 430742 Sheet 2 Page 11.6-2)*

**Reference**

The accuracy of all the values of current available for resistance measurement is derived from the Internal Reference on the DC PCB. The reference voltage is one of the outputs of the Reference Buffer U406 *(page 11.2-5)*, which is developed between OHMS_REF and 0V(12). On the Ohms PCB, this is isolated by a 'Flying Capacitor' pump circuit switched by astable multivibrator M204. M204 is enabled only when resistance measurements are to be taken, or when an Ohms constant current is to be used as input to the current-to-voltage converter on the Current PCB in Selfcal and Self Test. At times when the pump circuit is disabled, the zener D202 is used as reference for the voltage mirror.

The astable M204 is enabled by the 'OSC' signal, which passes from the processor to the Ohms PCB via the serial interface, latched into M301 *(page 11.6-3)*. It is then decoded, and delivered to M204-4/9 *(page 11.6-2)*.

**Sink Circuit**

Voltage mirror M203/Q208 maintains a constant voltage across a series resistor chain R204, R214, R219 and R217/R218 (parallel to spread the load for 10mA selection).

**Constant Current Switching**

By shunting and picking off currents, any one of the range of constant currents can be drawn through the resistor under test. Each Resistance Mode and Range combination is assigned its own value of current, the FET/Relay activation pattern being controlled in firmware. Switching arrangements for the currents are shown in simplified form on Fig. 5.2.3.2. Table 5.2.3.1 relates the constant current value to the Mode and Ohms range selected by the user.

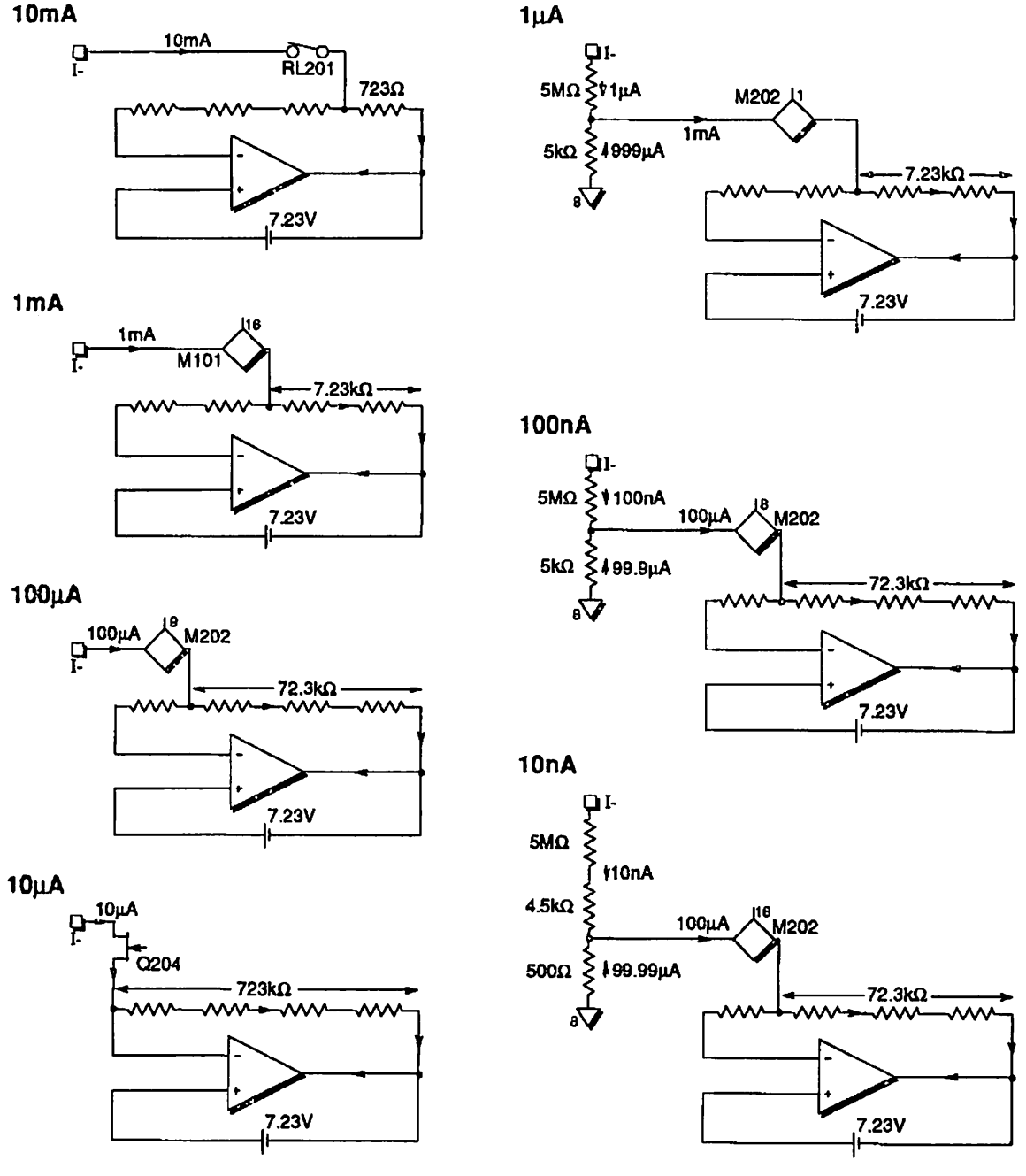



*FIG. 5.2.3.2 OHMS CURRENT SWITCHING*

### 5.2.3.3 Low Current Ohms

Where low compliance or low open circuit voltages across the DMM's terminals are needed, a special low current mode (LoI) can be selected. Applications where this can be useful include in-circuit measurement of components in parallel with diode junctions, or the measurement of temperature using Platinum Resistance Thermometers, where the self-heating effects of the current passing through the resistive element are important.

The 100mV DC Voltage range is used for all low current Ohms measurements

### 5.2.3.4 True Ohms

In addition, for those applications where external thermal emfs present measurement problems, a mode is provided where a zero reference reading is automatically taken with the measurement current turned off (Tru Ω). This zero measurement is subsequently subtracted from that made with the current flowing, to give a resultant value where the effect of any thermal emfs have been eliminated.

### 5.2.3.5 Low Follower and Voltage Detection

External errors produced by specific connections can be reduced using four-wire sensing and Ohms guarding techniques. Four-wire sensed measurement can be made with up to 100Ω in any lead with no degradation in accuracy. Furthermore, errors caused in external leakage paths can be eliminated using an Ohms Guard terminal which may also be used for in-circuit measurement of components in parallel with other resistive elements.

The aim of the Low Follower is to separate the current path from the voltage detection circuit, so that in 4-wire connection the current flows through the resistor under test, and the voltage across it is detected at the resistor itself with no other common wiring.

**Current Path** *(Fig 5.2.3.1)*
*(Circuit Diagram 430742 Sheet 1 Page 11.6-1)*
The resistor under test **Rx** is connected between I+ and I-. The energizing current is drawn from I- by the constant current sink, and sourced through the power output stage of the Low Follower into I+. The value of the constant current is switched at the sink as described above.

Lo is connected to the Low Follower inverting input, and because this places Rx as the feedback resistor, Lo is forced to the same potential as Common-8 at the Low-Follower non-inverting input. Virtually no current flows in the low line, as the bias current required by the Low Follower is very low .

When measuring in 4-wire, I- and Lo are connected together only at Rx, so current in the I- line does not pass through any part of the Lo line, and the resistor Lo terminal is held at the potential of Common-8. With 2-wire selected, the constant current does pass through part of the Lo line, and an IR drop is generated across the ends of the path. At the Hi end of the resistor, the source current is drawn through the I+ line, and in 4-wire it does not pass through any part of the Hi line.

**Voltage Measurement across Rx**
The voltage due to the constant current in Rx alone is presented between Hi and Lo with no other IR drop. The Lo end is held at Common-8, which is the same as the 'MECCA' on the DC PCB. The DC Preamp presents an extremely high impedance to Hi, so the voltage measured by the DC Voltage circuitry is that across the resistor Rx alone.

When a particular Resistance range is selected, its energizing current value is determined by firmware, the results of the measurements being modified by calibration constants. The setup must have optimum constant current and optimum DC Voltage measurement range for low noise and stability. This choice is predetermined and set in the program; the range of setup conditions are shown in Table 5.2.3.1.

**Low Follower Amplifiers**
The Low Follower is a compound amplifier, with M103 and Q108 DC-stabilizing Q104 and M102. The two paths are recombined by M104 summing amplifier.

**Alternate Current Sourcing**
For thermal reasons, Q110 is supplied from +35V for low current values, and +5V for high currents. The changeover occurs via diode D106.

**Clamping**
Clamping is used to limit the voltage drive to Q110, at values dependent on the DCV range used to measure the voltage across Rx. For the 10V range, the **CLAMP** signal (Q115 gate) is at +5V, and the voltage at the junction of R137/138 limits at +25V. With the 100mV or 1V range in use, CLAMP changes to 0V and the limit is reduced to +5V. The CLAMP signal is set by the processor via the serial data link, the programmed level appearing at DIO7, pin 12 of M301 *(page 11.6-3)*.

**Ohms Low Sense**
The input channel **Lo** terminal cannot not taken directly to 'MECCA' common when resistance is being measured; instead it is switched to the **Ω LOW SENSE** line into the Ohms PCB. It is maintained at high impedance while being referred to 0V(8) by the action of the Low Follower.

Low switching is performed by relay K109 on the DC PCB *(Circuit Diagram DC400866 page 11.2.2)*.

**2-Wire/4-Wire Switching**
The input channel **Hi** is fed directly to the DC PCB for the voltage measurement across the resistor Rx, and for this purpose does not need to appear on the Ohms PCB. However, the 2-wire/4-wire switching is performed by Ohms relay RL101 between **Hi** and **I+**, so Hi is brought on to the Ohms PCB to be switched. On the Lo side, RL101 connects **Ω LOW SENSE** to **I-** in 2-wire. The 2-wire links are protected by thermistors.

**True Ohms Switching**
The first of the pair of True Ohms readings is a the same as normal, with relay RL104 energized at contact 1. The second is taken with no current drawn through Rx via I-, as RL104 is unenergized at contact 14. Thus the constant current sink is sourced directly from Common-2.

**Selfcal and Selftest**
During self-calibration the Ohms ranges are calibrated with reference to two standard resistors fitted on the Ohms PCB - R105 and R106. These are switched out by RL102 being energized during normal operation, but for Selfcal and Selftest the I+ input is disconnected, and the Ohms circuit measures the values of the two resistors as they are switched in by the contacts of the de-energized RL102. For a low standard resistance R106 (1.0kΩ) is selected on its own, and for high resistance R105 and R106 are connected in series (101kΩ); the switching being performed by RL105. The software models for Selfcal and Selftest are given in Section 2.

**Filter**
C108 and R126 provide HF compensation for the whole Low Follower. When Filter is selected, the **F** signal at +5V introduces C107 in parallel with C108 to reduce the frequency response of the follower. In this state, Q107 is turned off to turn Q106 on. The **F** signal originates on the DC PCB as **FILTER** *(page 11.2-10)*, its level having been set at pin 15 of the register U902, by the processor via the serial data interface. So both the DC Voltage and Ohms filters are switched in and out simultaneously.

### 5.2.3.6 3-Bit Word Transfer and Decoding

A 3-bit word which represents the current switching pattern is passed from the microprocessor to the Ohms PCB via the serial interface, latched into M301 *(page 11.6-3)*, and DIO 2/3/4 is delivered to M304-1/2/3 for decoding. Signal DIO 4 is also added to the decode, and the resulting decoded lines are used to generate the FET/Relay switching pattern.

When a particular Mode/Range combination is selected in Resistance Function, the Processor translates the selection into the corresponding 3-bit pattern to activate the current. It also sets the appropriate DC Voltage range. Table 5.2.3.1 relates the constant current value and DC Voltage range used, to the Mode and Ohms range selected by the user.

**Table 5.2.3.1 Ohms Range, Mode and Current; with DC Voltage Range Employed**

| Ohms Range | Ohms Current | | | | | | |
|---|---|---|---|---|---|---|---|
| | 10nA | 100nA | 1µA | 10µA | 100µA | 1mA | 10mA |
| 10Ω | | | | | | | TruΩ 100mV |
| 100Ω | | | | | | Lol 100mV | Normal 1V<br>TruΩ 1V |
| 1kΩ | | | | | Lol 100mV | Normal 1V<br>TruΩ 1V | - |
| 10kΩ | | | | Lol 100mV | Normal 1V<br>TruΩ 1V | - | |
| 100kΩ | | | Lol 100mV | - | Normal 10V<br>TruΩ 10V | | |
| 1MΩ | | Lol 100mV | - | Normal 10V | | | |
| 10MΩ | Lol 100mV | - | Normal 10V | | | | |
| 100MΩ | - | HiΩ 10V | | | | | |
| 1GΩ | HiΩ 10V | | | | | | |

## 5.2.4 DC and AC Current - Option 30

The DC Current function is achieved using a set of precision shunts in conjunction with the DCV measurement capability. The AC current function uses the same set of shunts in conjunction with the ACV measurement capability. Option 30 requires Option 20 also to be fitted, as it is self-tested and self-calibrated using currents provided by the Ohms circuitry.

### 5.2.4.1 Functional Block Diagram

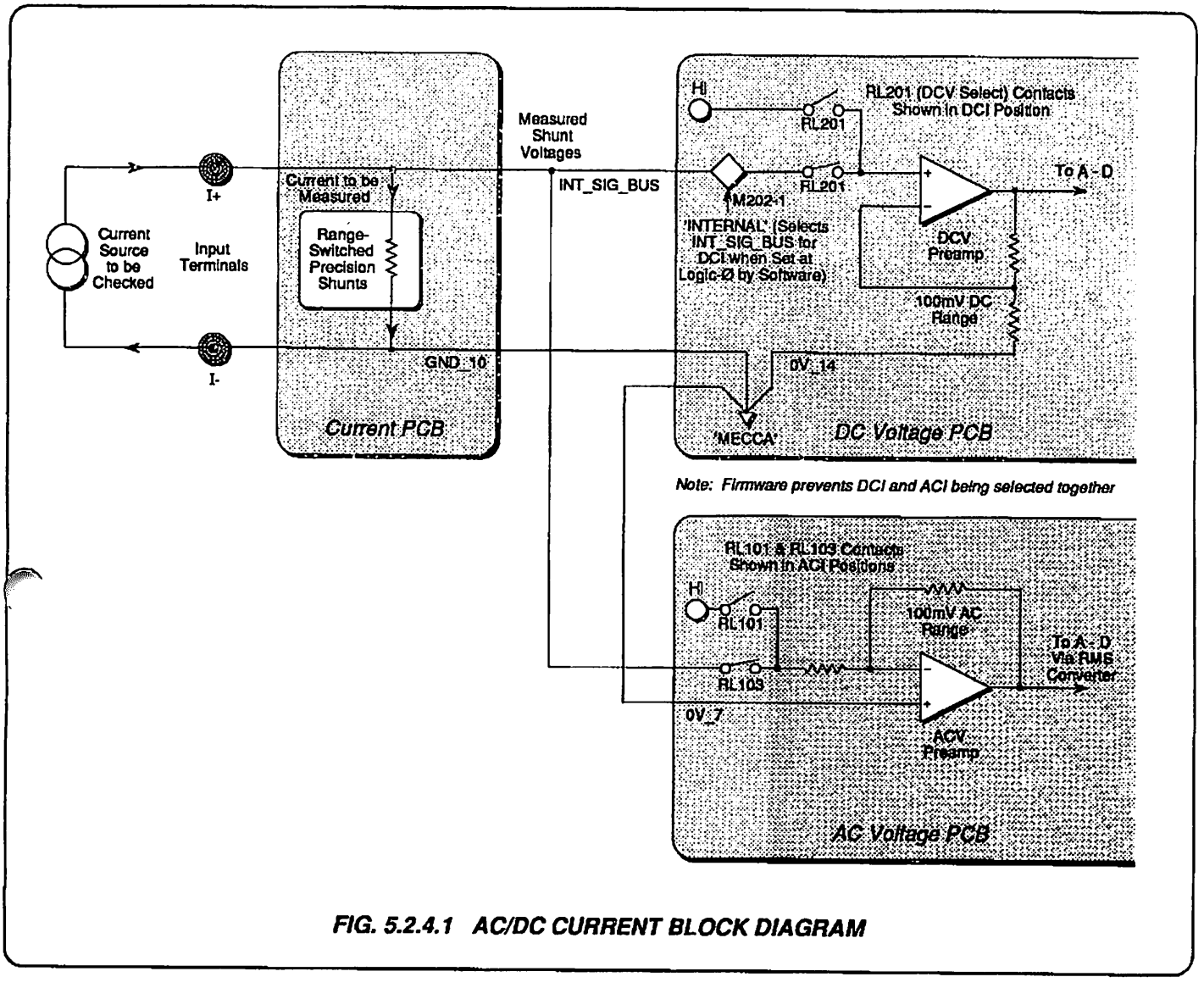



*FIG. 5.2.4.1 AC/DC CURRENT BLOCK DIAGRAM*

### 5.2.4.2 Switched Current Shunts

**General**

For Current measurement, five precision shunts are switched internally to correspond with selection of the five ranges. The unknown current passes through one or more of these shunts, and the resulting voltage is measured using the 100mV DC or AC range circuitry. The shunts and the source of the current are protected both electronically and by a 1.6A fuse, accessible on the rear panel.

**Input Current Routing**

The current from the selected input channel enters the Current PCB at PL52-1 (Hi), passes through the fuse and selected shunt(s), and exits by PL50-6 (Lo).

On the Current PCB the current path is interrupted by three open contacts of RL100 when the Current Function is not selected. The contacts are closed in Current Function.

**Shunt/Range Correspondence**
Table 5.2.4.1 relates the range switching to the selected range and range shunts utilized.

**Table 5.2.4.1 Current Range Switching**

| Range | Shunts | | | | |
|---|---|---|---|---|---|
| | R111 900Ω | R112 90Ω | R113 9Ω | R114 1Ω | R115 0.1Ω |
| 100µA | M101-9 / Q101 | | | | |
| 1mA | M101-16 / Q102/103 | | | | |
| 10mA | RL102 | | | | |
| 100mA | RL103 | | | | |
| 1A | RL104 | | | | |

### 5.2.4.3 Shunt Voltage Measurement

**Sensing**
For each range, the voltage to be measured across the range shunt(s) appears between common **GND_10** at PL51-1 and **INT_SIG_BUS** at PL51-2. GND_10 is connected as **0V_10** directly to MECCA via J141-1 on the DC PCB *(page 11.2-2)*.

For all the ranges up to 100mA, the unenergized relay RL104 contacts 2/3 (closed) and 4/5 (open) connect GND_10 to R114, switching out the volts drop across the 1A shunt R115 (although the input current for each range passes through R115 on its way to I-). On the 1A range, RL104 is energized to connect GND_10 to R115 instead of R114.

**Measurement (DC Current)**
The DC voltage circuitry is referred to MECCA *(page 11.2-2)*. For the DC Current function, the input to the DC Voltage preamp is connected to INT_SIG_BUS instead of the external inputs. The INT_SIG_BUS line is selected on the DC PCB by U202-1 and the unenergized relay K201 *(page 11.2-3)*. The DC preamp passes the conditioned DC signal to the A-D.

**Measurement (AC Current)**
The AC voltage circuitry is referred to MECCA via common **0V_7** *(page 11.2-2)*. For the AC Current function, the input to the AC Voltage preamp is connected to INT_SIG_BUS instead of the external inputs. The INT_SIG_BUS line is selected on the AC PCB by RL103-5/4 and the unenergized relay RL101-2/3/9/8 *(page 11.5-1)*. The AC circuitry converts the AC voltage to a DC (RMS) voltage, which is passed to the A-D.

### 5.2.4.4 Protection

**Fuse**
The 1.6A Current fuse is located for access on the rear panel, and connected in series with the I+ line via PL54-1/2. The fuse is tested during Selftest (see below), and although not specifically tested in Selfcal, will cause Selfcal to fail if it is not intact.

**Diodes**
Four diodes D103-D106 protect the shunts when an attempt is made to measure a current which is too large for the range in use, limiting the voltage across the shunt(s) and blowing the fuse if the excess current is large enough. For normal operation, any leakage current in the diodes is guarded out by the bootstrap M102.

**Bootstrap**
M102 buffers the voltage at the high end of the shunt chain as 0V_B, which in Current function drives the center connection of the four protection diodes. Thus there is no voltage across the top two diodes, so all the input current passes through the shunt(s). The bootstrap forces the shunt voltage across the bottom two diodes, so leakage current is diverted to GND_10 and back into the power supply for buffer M102.

In Selftest and Selfcal, the input test current is sourced, via the I+ line, from the Low Follower output on the Ohms PCB. It returns to (and is controlled by) the constant current sink on the Ohms PCB, via the I- line. In this case RL101 is energized, forcing 0V_2 at the diode junction. This maintains zero voltage across the bottom pair of diodes, and diverts leakage current from the top two diodes into 0V_2, instead of into the constant current sink. The bootstrap buffer is not used.

In both the above cases, leakage current in the protection diodes is diverted from the voltage measurement circuit, and so does not affect the shunt voltage passed out via INT_SIG_BUS.

### 5.2.4.5 Selfcal and Selftest

**Circuit Changes**

As mentioned above, the internal circuitry is changed to perform these functions. The Input switching disconnects the I+ and I- s from the input channel terminals. Current to test the Current PCB is sourced from the output stage of the Low Follower on the Ohms PCB, via the I+ line; and controlled by the Ohms constant current sink, via the I- line.

The shunt voltage is no longer referred to GND_10. Instead, the low end of the shunt is switched to a special **LO_SENSE** line, which provides the low input to the low follower. Relay RL101 on the Current PCB is energized during Selfcal and Selftest to perform this changeover. The voltage at the high end of the shunt chain is passed to the DC PCB via the INT_SIG_BUS line as in normal Current function.

In effect, the resistance of the shunt chain is measured by the Ohms function. All five ranges are calibrated and tested by this method. The DC arrangement is shown on the Test Setup Diagram in Section 2 *(page 2-36 to 2-40)*.

For AC current the voltage at the high end of the shunt is passed to the ACV PCB for measurement. This arrangement is shown on the Test Setup Diagram in Section 2 *(page 2-42)*.

**Fuse Test**

This is performed as part of Selftest. The instrument is programmed into the DC 10mA range, with the test current being drawn from the Ohms PCB. If the fuse is intact, the voltage measured on the INT_SIG_BUS will be positive, and a pass condition is registered. If it has blown, the voltage will be negative o the Ohms constant current being forced to zero, indicating a failure condition.

## 5.2.5 Analog-to-Digital Conversion

### 5.2.5.1 Functional Diagram

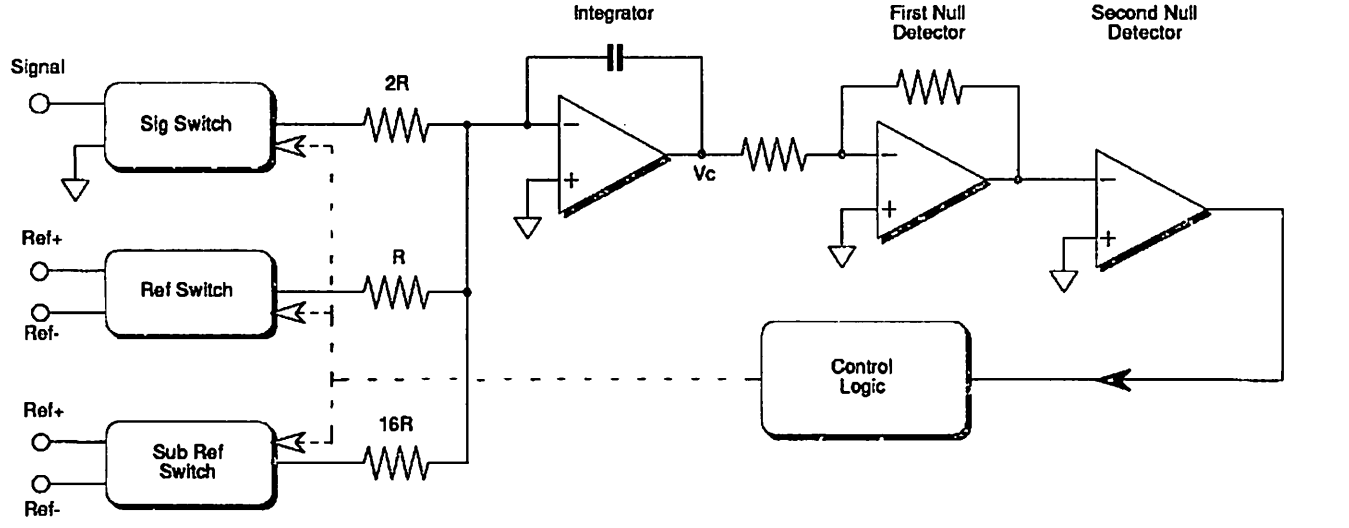



*FIG. 5.2.5.1 A-D CONVERTER - SIMPLIFIED SCHEMATIC*

### 5.2.5.2 Introduction

The instrument converts conditioned analog signals to a digital form using a multi-ramp, multi-slope, integrating A-D. This provides:

1. High linearity - < 0.2ppm without adjustment;
2. Low noise of < 0.05ppm of full scale;
3. High speed - signal and reference are applied together simultaneously, greatly reducing the conversion time;
4. 100% overrange, giving a maximum discrimination of 1 part in 200 million;
5. Flexible operation - resolution (and hence speed) are programmable, from 5.5 digits at 1000 readings per second to 8.5 digits per second at one reading per 6 seconds.

A digital autozero system avoids the need for the more common sample-and-hold type of autozero circuit.

Multislope operation permits the integration capacitor value to be smaller than normally required for a more conventional circuit, greatly reducing problems due to dielectric absorption.

'Line locking' is incorporated to present a deep and narrow 60dB rejection notch, which is independent of the input amplifier response time and supports high data rates. This continuously-tracking notch combats line-related EMI, as the critical A-D timing waveforms synchronize precisely with the frequency of the incoming power line.

The control logic determines the parameters of the conversion, by counts and timings which are selected by the processor and transferred via the serial interface in four bytes of data. Timing, counting and control are executed by a custom 'ASIC' (Application-Specific Integrated Circuit), resulting in a design which offers both variable integration times and user-selectable resolutions.

The digital result of a measurement is transferred back to the processor via the serial data interface.

Reference switching errors are reduced to a constant value, which are subtracted from the reading by the instrument's microprocessor.

### ..5.3 Reset

'Reset' mode replaces the more conventional analog 'Autozero'. It is imposed by the ASIC except when a conversion is in progress. The four phases of reset activate the converter to ramp through small excursions about zero, eliminating zero drift and holding the converter in a quiescent state. The ramps and timings are shown in Fig. 5.2.5.2.

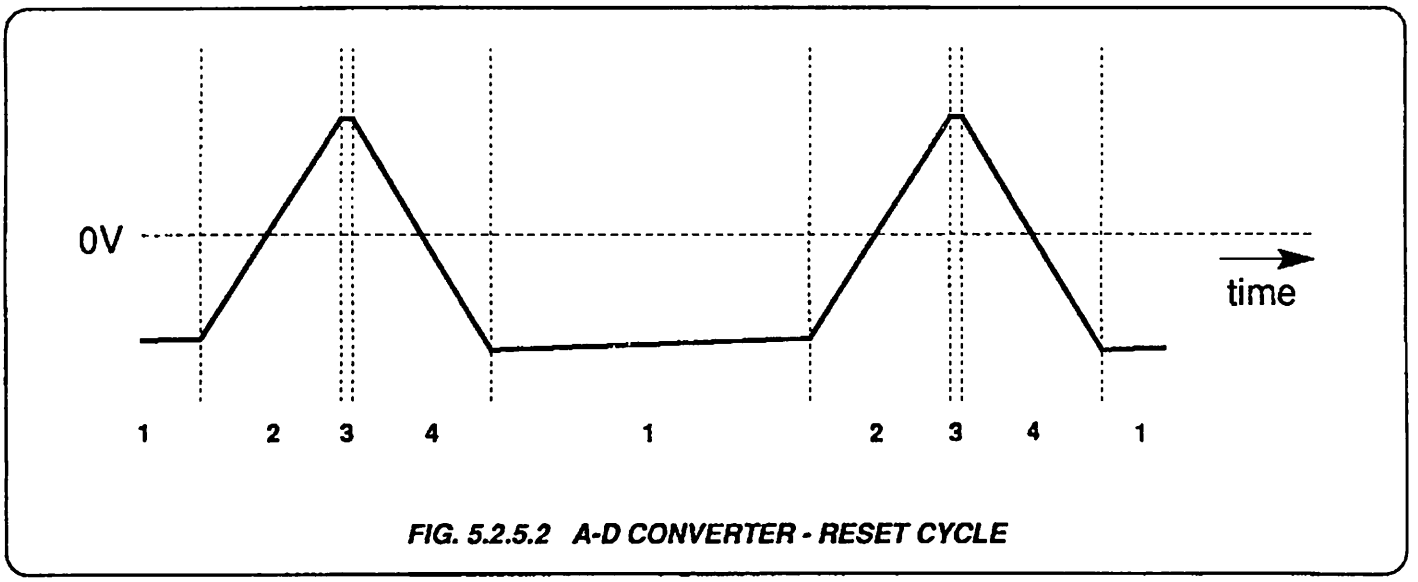



*FIG. 5.2.5.2 A-D CONVERTER - RESET CYCLE*

**The Reset Cycle**

There are four phases in the reset cycle, numbered on Fig. 5.2.5.2:

ø1. Zero is applied to both Signal and Reference inputs. This time is set by the ASIC, and the slope is determined by the integrator drift (exaggerated on the diagram).

ø2. Zero is applied to the Signal input, and -Ref/256 to the Reference input. The integrator ramps up and crosses zero. The Null Detector has a standard delay, and for a fixed period after this, the ASIC continues to apply -Ref/256. These three times constitute the time of phase 2.

ø3. Zero is applied to both Sig and Ref inputs as in phase 1 for a very short period, to guard against any overlap in switching. The integrator drifts during this time.

ø4. Zero is applied to the Signal input, and +Ref/256 to the Reference input. The integrator ramps down and crosses zero. The Null Detector has the same delay, and again the ASIC continues to apply the +Ref/256 for a further fixed period. These three times constitute the time of phase 4.

The cycle is repeated, maintaining the integrator output near zero (within approx. 25µV). The overshoot in phases 2 and 4 is deliberately introduced to ensure a clean transition through zero. As can be seen from the diagram, the integrator output always reaches the same value at the end of Phase 4, due to the two fixed ramps, even though drift may occur in phase 1.

Because of its low amplitude and short timings, this reset waveform is difficult to view accurately.

**End of Reset**

The A-D continues in Reset mode until instructed to start a reading conversion. A separate control line (CI1-R), with its own opto-coupler (U803-3/6), initiates the conversion.

### 5.2.5.4 Conversion Initiation

**Triggering**

Depending on the type of measurement trigger received, the instrument can be called upon to execute single or multiple readings, the latter being processed in some way to arrive at a 'measurement'. This could be as a result of an external trigger, a manual trigger (sample) or a trigger received over the IEEE 488 interface. The number of readings to be taken depends on the instrument state and the type of trigger received.

**'Conversion Initiate' Signal**

For each reading required, the **Conversion Initiate** signal (CI1-R) is set high to start a conversion on its rising edge. As a result, the A-D executes a Reset cycle, ensuring that the conversion starts from a known integrator output value. The cycle is terminated by the ASIC SIG lines being activated to apply the conditioned signal to the integrator input. The result of CI1-R is shown in Fig. 5.2.5.3 for a negative signal input.

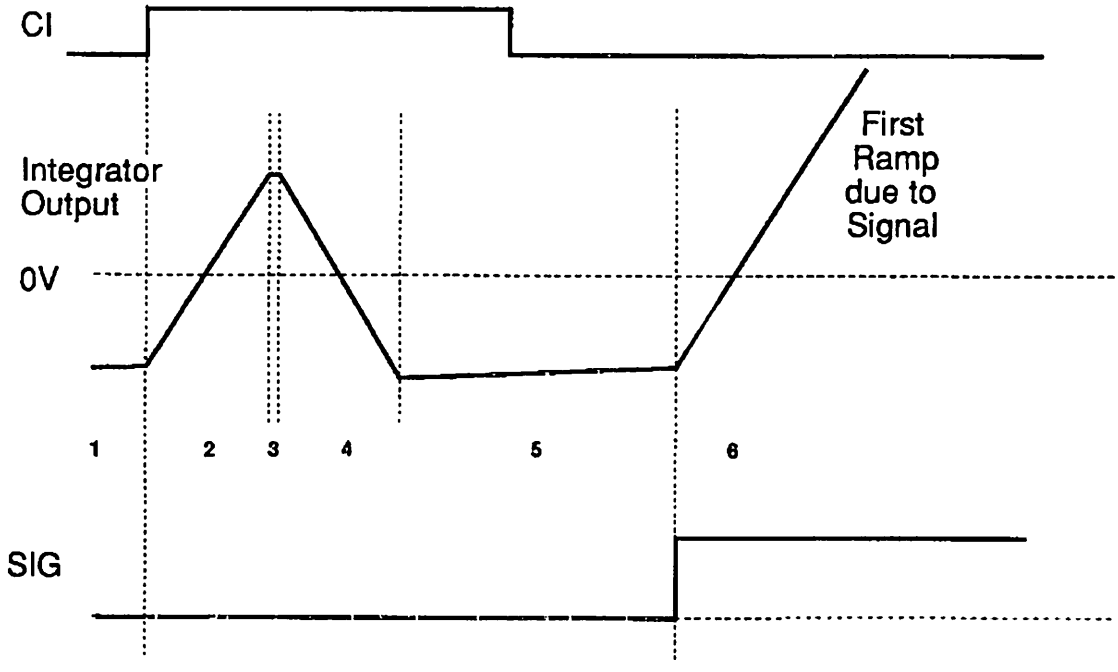



*FIG. 5.2.5.3 A-D CONVERTER - EFFECT OF 'CONVERSION INITIATE' SIGNAL*

# Single and Multiple Ramp Conversions

## Notes

Pages 5-30 to 5-35 illustrate examples of the forms of conversions used in the 1271. Because of the wide range of amplitudes and timings which are involved in the sequences, the waveforms given in the figures are not to scale - some exaggeration is required to show the changes.

The control signal waveforms are intended to illustrate sequencing only - in some cases there are several versions of a signal. Polarities and amplitudes in the figures are therefore not to be regarded as accurate.

### 5.2.5.5 Single Ramp Conversions

The integrator output and control signals for a single conversion with positive and negative inputs are illustrated in Fig. 5.2.5.4 and 5.2.5.5 respectively. Time starts at Phase 5 after the Reset initiated by the CI signal. There are several versions of the control signals, those shown in the diagrams indicate timing only, and not polarity.

Note that the time "t" is fixed, as are the durations of phases 11, 12, 13 and 14. There is also the fixed Null Detector delay, and a fixed overshoot delay after null is detected in phase 10. Bias is applied during phase 8.

---

**Positive Signal Input**

The phases in the conversion cycle for positive signal input are numbered on Fig. 5.2.5.4:

ø5. Zero is applied to both Signal and Reference inputs, this is the final stage of CI.

ø6. The positive signal is applied to the Signal input, with zero on the Reference input. The integrator ramps down for a fixed period.

ø7. The signal is applied to the Signal input, with +Ref on the Reference input. This 'bias' is applied for a fixed period with Ref polarity determined by the state of the Null Detector. It is arranged for the integrator to ramp further away from null.

ø8; ø9:
Zero is applied to both Sig and Ref inputs to ensure that two references are not applied together.

ø10. Zero is applied to Sig input and -Ref to the Ref input. The integrator ramps up and eventually crosses null. The Null Detector has the standard delay, and the ASIC continues to apply -Ref for a further fixed period. The integrator therefore overshoots.

ø11. Zero is applied to Sig and Ref inputs for a fixed period. This 'wait' allows the dielectric absorption in the integrator capacitor to be recovered. Note that the conditions of phase 11 are applied three times.

ø12. Zero is applied to Sig input and +Ref/16 to the Ref input. The integrator ramps down and crosses null. The Null Detector has the standard delay, the ASIC continues to apply the +Ref/16 for a further fixed period, and the integrator overshoots.

ø13. Zero is applied to Sig input and -Ref/16 to the Ref input. The integrator ramps up and overshoots null, controlled by the Null Detector and ASIC delays.

ø14. Zero is applied to Sig input and +Ref/256 to the Ref input. The integrator ramps down very slowly and crosses null. The integrator overshoots null, controlled by the Null Detector and ASIC delays.

**End of Conversion - RTX Signal**

The conversion is now complete and the A-D reverts to Reset mode. To signify the end of the conversion the ASIC sets RTX high. Data may now be shifted out of the A-D via the serial interface. RTX remains high until the next CI is received.

Observe that at the end of phase 14 the integrator output is negative due to the same delays and +Ref/256 as at the end of Reset phase 4, so it is back where it started before the conversion. Hence the accumulated amount of the references applied is a measure of the signal applied.

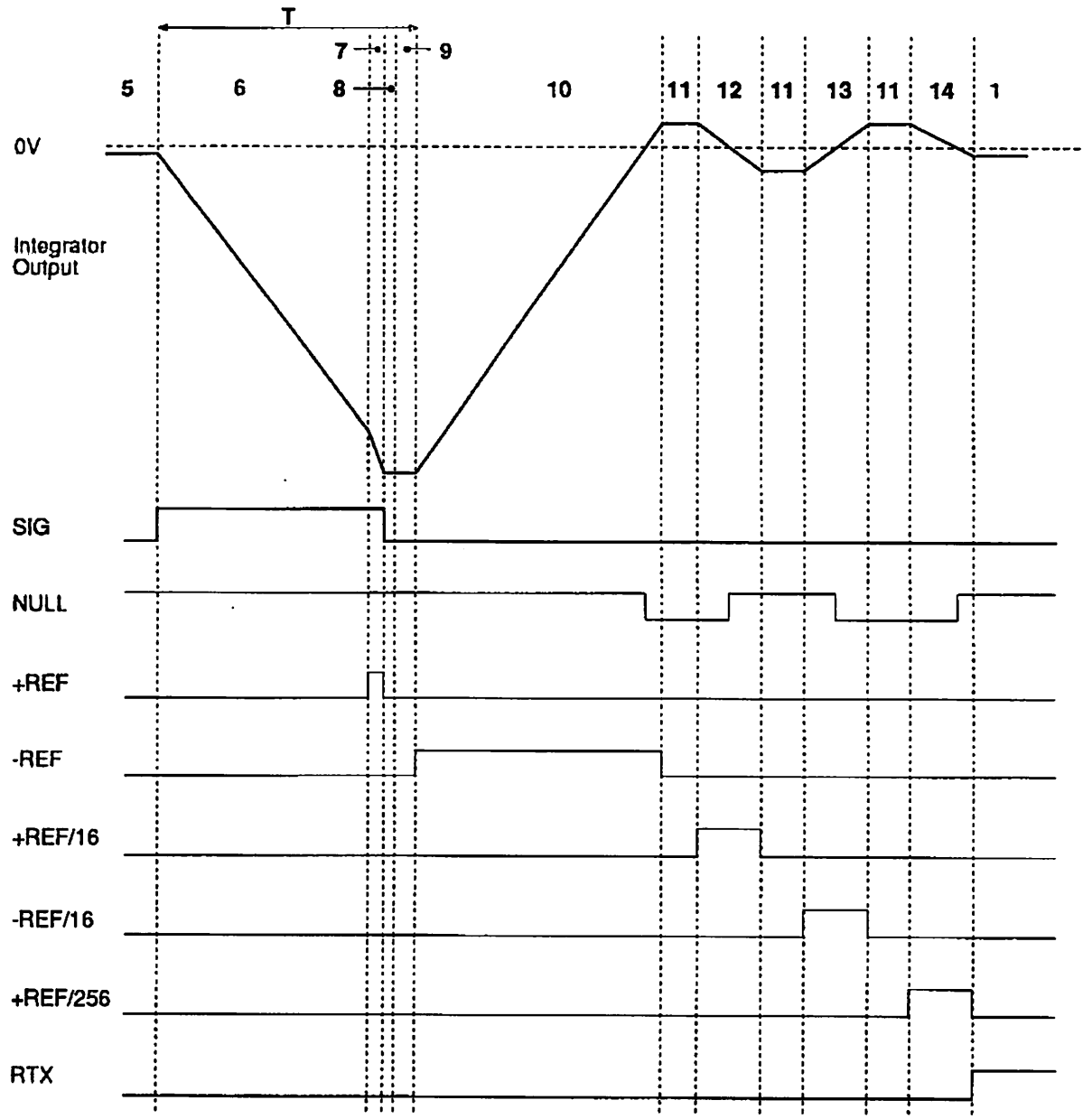



*FIG. 5.2.5.4 SINGLE RAMP CONVERSION - POSITIVE INPUT*

### 5.2.5.5 Single Ramp Conversions (Contd.)

**Negative Signal Input**

The phases in the conversion cycle for negative signal input are numbered on Fig. 5.2.5.5. The conversion is subtly different, because of the integrator output starting and finishing at a negative value. This shifts some of the null crossings, and the general waveform is not merely an inversion of that for the positive input. Nevertheless, the principle of operation and sequence of phases remain the same.

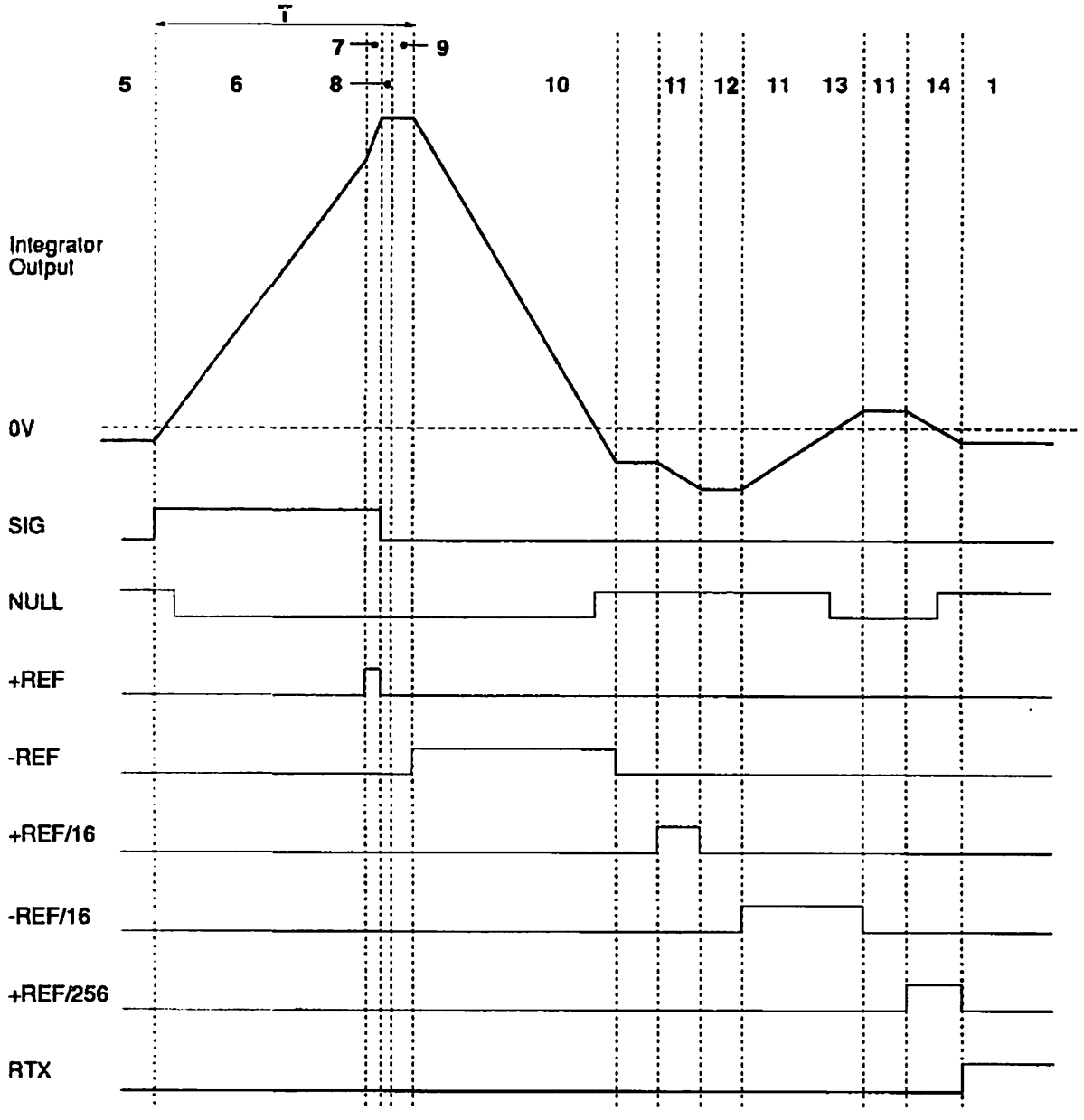



*FIG. 5.2.5.5 SINGLE RAMP CONVERSION - NEGATIVE INPUT*

### 5.2.5.6 Multiple-Ramp Conversion

**Sequence of Phases**

The integrator output and control signals for a multi-ramp conversion with positive input is illustrated in Fig. 5.2.5.6.

ø1 to ø5 These are as described earlier for Reset.

ø6 and ø7 These are the same as in the single-ramp conversion.

ø8 to ø14 These are the same as in the positive single-ramp conversion.

ø15 This is similar to ø8 for the single ramp; but the positive input signal is reapplied to the Signal Input instead of zero. The slope of the ramp is the same as in ø6.

ø16 Signal and Reference are applied. The polarity of the chosen reference is such as to ramp back towards null. The ramp overshoots null due to null detector and ASIC delays.

ø17 Signal only is applied. No 'wait' time is required between ø16 and ø17, as the reference is not applied in ø17, and so there is no possibility of shorting two references together. The slope of the ramp is the same as in ø6.

The cycle of phases 17, 7, 15 and 16 continues for as many ramps as are required for the programmed configuration. The final cycle is the same as the single-ramp version.

Once again, the accumulated amount of the references applied is a measure of the signal applied.

**Integrator Output Waveshape**

As the magnitude of the input changes, so does the shape of the integrator waveform.

At full scale the ramps are symmetrical and of equal height. As the signal is reduced the ramps begin to lean over with the null point moving to the left. The first ramp is reduced to about half the size of subsequent ones, and they are not all the same size. This is normal behavior, and is not indicative of a fault.

**Counting**

The rules for counting the amount of reference applied are quite simple:

1. Counting occurs whenever a reference is applied.
2. The count is **up** for negative references; **down** for positive references.
3. If Ref is applied the count increments in units of 256.
4. If Ref/16 is applied the count increments in units of 16.
5. If Ref/256 is applied the count increments in units of 1.

This ensures that even with overshoot the correct result is obtained. A normal 32-bit up/down counter within the ASIC is used, that is reset to zero by the signal CI.

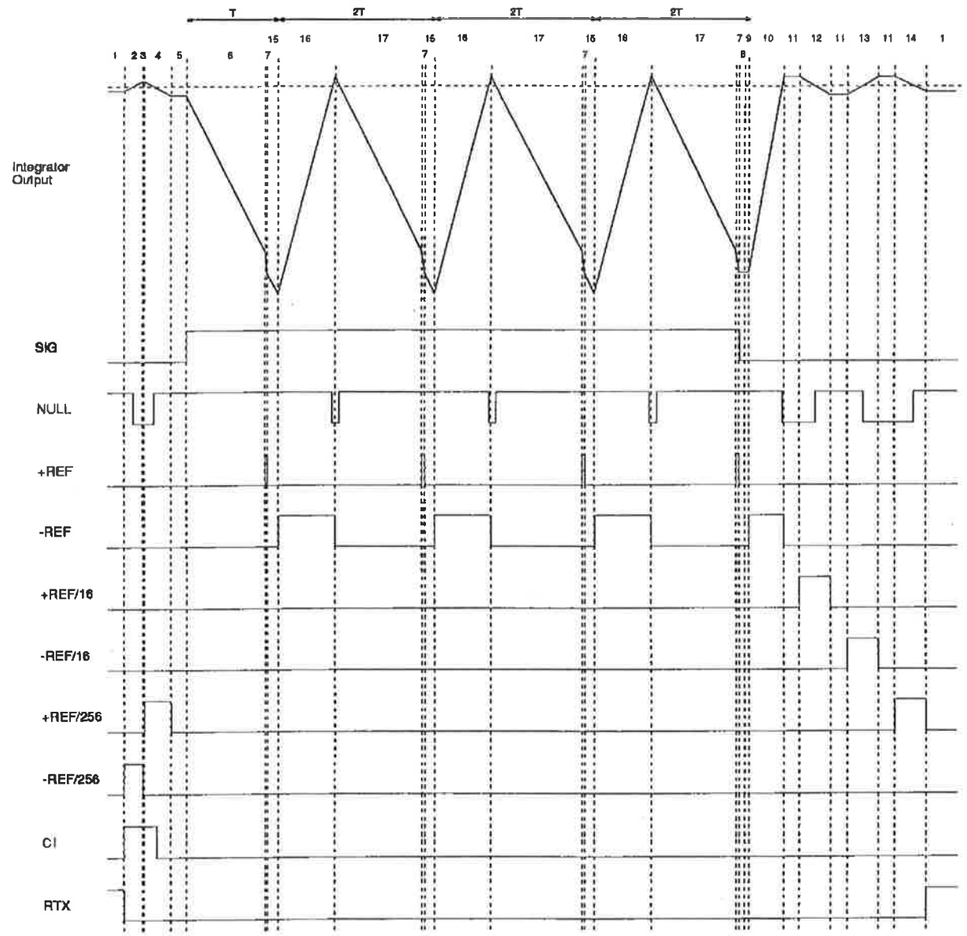



*FIG. 5.2.5.6 MULTIPLE RAMP CONVERSION - POSITIVE INPUT*

## 5.2.6 Internal References

### 5.2.6.1 Reference Modules

**Module Description**

The reference used in the analog to digital conversion is derived from specially conditioned zener reference modules. Each contains the reference device and its associated circuits.

The modules are stable to within ±3ppm per year, produce noise of less than 0.1ppm, and have temperature coefficients of better than 0.1ppm/°C. This temperature coefficient is held over a very wide temperature span of 0°C to 70°C, and the references exhibit negligible temperature shock hysteresis.

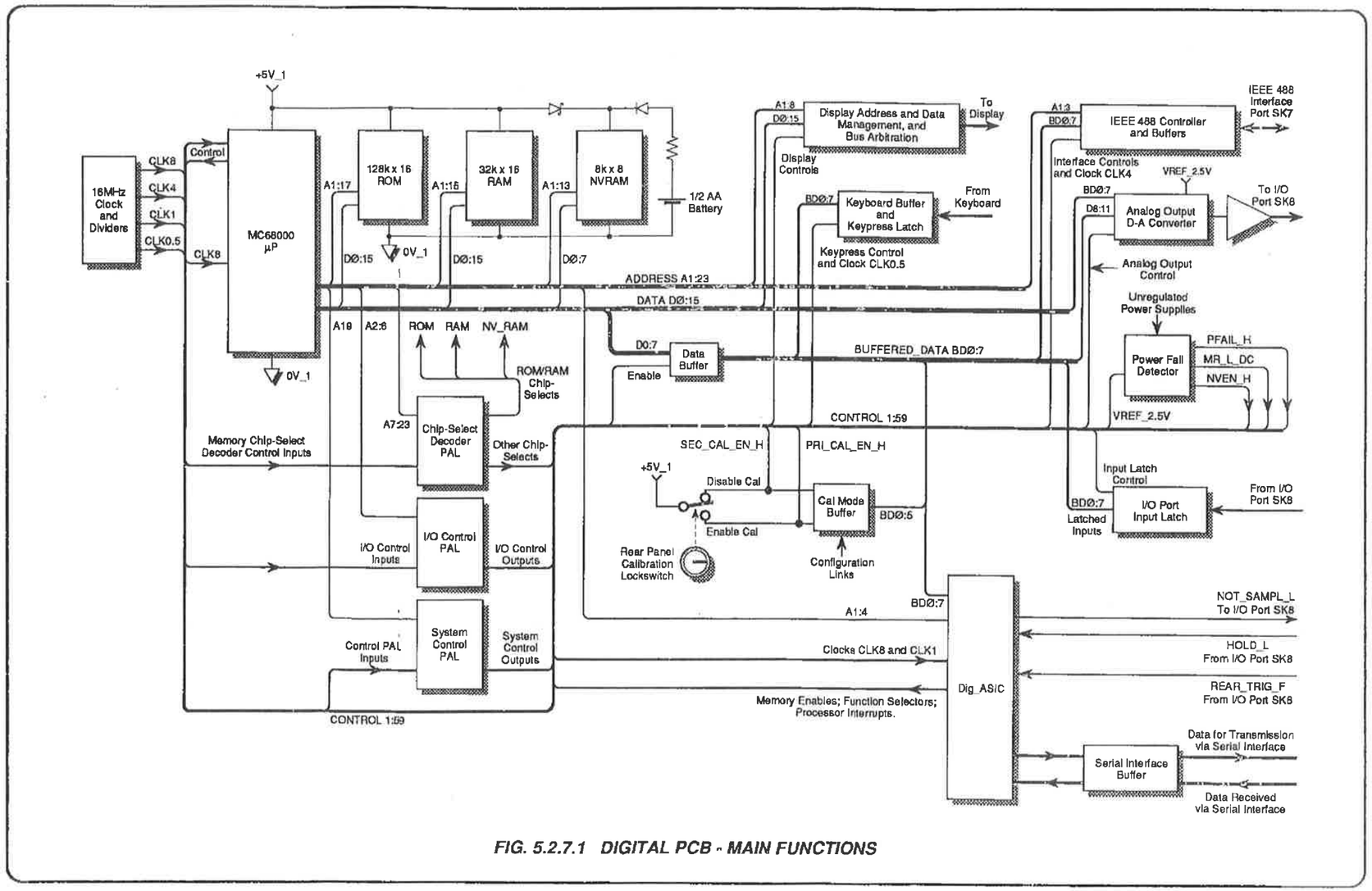



*FIG. 5.2.7.1 DIGITAL PCB - MAIN FUNCTIONS*

### 5.2.6.2 Reference Generation

**Master Reference**

*(Circuit Diagram DC400866 Sheet 4; page 11.2-5)*
The -7V reference is amplified to -10V by REF AMP U403. This is inverted by a flying capacitor REF INVERTER U404 to produce a 10V reference. The positive and negative references are buffered by U407 and U408 respectively.

Gates U502-16 and U503-1 compensate for the effects of the attenuator switching gates at the A-D input.

*(Circuit Diagram* DC400866 *Sheet 5; page 11.2-6)*
The outputs from Q408 and Q409 are the two compensated reference signals '+VREF_COMP' and '-VREF_COMP. These are fed to the REF SWITCH U502/U503 and SUBREF SWITCH U504/U501, which select the A-D reference levels under the control of ASIC U509.

**Ohms Reference**

REF BUFFER U406 buffers the averaged output from the reference modules to generate OHMS_REF, which is passed out via J107-11 to the Ohms PCB at PL43-11. This level is also passed, as the 'CAL REF' signal, to the Selfcal Multiplier circuit *(p11.2-8)*. During Selfcal and Selftest CAL REF is switched as the input to the Error Amplifier of the Selfcal Multiplier to provide its DC reference voltage.

## 5.2.7 Digital Control

### 5.2.7.1 Functional Block Diagram

. 5.2.7.1 opposite shows the main groups of functional circuits on the Digital PCB.

### 5.2.7.2 Processing, Memory and Organization

**Clocks**

*(Circuit Diagram DC400901 Sheet 1; Page 11.4-2)*
All synchronizing clocks used on the Digital PCB are derived from 16MHz crystal oscillator Y101. Four are required; produced by division in U101:

**CLK8:** 8MHz for the Processor and Digital ASIC *(p 11.4-3)*;
**CLK4:** 4MHz for the IEEE 488 I/F Controller *(p 11.4-5)*;
**CLK1:** 1MHz for the Digital ASIC *(p 11.4-3)*;
**CLK0.5:** 500kHz for the Display Controller *(p 11.4-4)*.

**Processor**

*(Circuit Diagram DC400901 Sheet 1; Page 11.4-2)*
The instrument is internally controlled by a 68000-series microprocessor. It ultimately translates all information, from the front panel keys and IEEE 488 interface, into control signals which determine the instrument's operation.

**Data Transfers**

Normal data transfers are processed via all address lines A1:23 (Address Bus) and all data lines DØ:15 (Data Bus), using the inherent 68000 word and byte divisions and strobes. Other control signals in and out of the processor are grouped in the circuit diagrams as a 'Control Bus', but this is merely for clarity - the lines distributed on the PCB.

Different devices need different access times, and the processor requires read/write cycles to be terminated by the handshaking device to achieve maximum operating speed. The instrument accounts for three different access times:

| | |
|---|---|
| 250ns: | Normal RAM, EPROM, ASIC and Interrupt Acknowledge; |
| 500ns: | IEEE 488 Controller, NV RAM, Display and I/O Port; |
| 1µs: | Switches |
| 2µs: | Analog-Output D-A. |

**Memory Assignment**

*(Circuit Diagram DC400901 Sheet 1; Page 11.4-2)*
EPROMs U103 and U104 hold the 128k x 16 of operating program and fixed data; RAMs U112 and U105 contain 32k x 16 of workspace.

U106 is a low-power static 8k x 8 RAM which is permanently powered: either by the +5V supply, or by 1/2 AA battery BT1 when the instrument is switched off. Its 'non-volatile' memory is occupied by constants which are stored during calibration, and subsequently used to correct readings when in normal use.

**Memory Access**

All memory is held in 8-data-bit devices.

The EPROM chips are device-enabled by the Decoder PAL U110 from addresses A20:23. U103 and U104 are chip-enabled together by A19, and addressed via lines A1:17. Data bytes are read in parallel by simultaneous addressing; U103 provides the 'upper' byte onto data bus lines D8:15, and the 'lower' byte is read from U104 onto DØ:7.

The workspace RAM chips are selected by the Decoder PAL U110, and addressed via lines A1:15. Data bytes are read in parallel by simultaneous addressing. For RAM data, U112 is served by the 'upper' byte D8:15 and U105 by the 'lower' byte DØ:7. Device-enable and read-write are selected via the control bus.

The non-volatile RAM is also selected by the Decoder PAL U110, and addressed via lines A1:14. For RAM data, U106 is served by the 'lower' byte DØ:7. Device-enable and read-write are selected via the control bus, and write is inhibited unless calibration is enabled. NV RAM (U106; *page 11.4-2*) is divided into three areas:

1. Primary Calibration Constants (External Calibration);
2. Secondary Calibration Constants (Self Calibration);
3. User NV (Input Zero, Password, Bus Address etc.).

The Primary Calibration Constant area is protected against unauthorised Write access by the rear panel Cal/Run keyswitch. Secondary Calibration Constants and User NV, by necessity, are not keyswitch protected.

**Control Decoding**

*(Circuit Diagram DC400901 Sheet 1; Page 11.4-2)*
Three PALs: U107, U110 and U111, manipulate the various signals which are used to control instrument operation. Generally, U110 deals mainly with memory selection and calibration processes; the inputs to U111 are decoded to select devices other than memory. U107 operates mainly on handshake signals to and from devices which require longer access times.

**Buffered Data Bus**

*(Circuit Diagram DC400901 Sheet 2; Page 11.4-3)*
The lower data bus DØ-7 is connected to the two-way buffer U201 to provide the Buffered Data Bus BDØ:7. This is used to access several devices: Keyboard, Cal Mode Buffer, Digital ASIC, IEEE 488 Interface Controller, Analog Output D-A Converter and the I/O Port. U201 is enabled by EN_BUF_L, and its direction is controlled by signal BR_HW_L.

### 5.2.7.3 Digital ASIC

The Digital ASIC *(U203 on page 11.4-3)* is a 68000 support chip for digital multimeters. It interfaces via 16 read-write registers and an interrupt handler.

**Functions**

*(Circuit Diagram DC400901 Sheet 2; Page 11.4-3)*

1. 68000 bus time-out for one or more wait state pairs (DTACK). Bus error generation on invalid address time-out (BERR).
2. 68000 reset power delay PFAIL to RESET.
3. Switching counter 1 to 256ms delay gives interrupt.
4. Tick interrupt 10ms or 100ms period.
5. Internal counter - free-running for internal triggers 0s to 10s: 10-bit with four prescales (10µs; 100µs; 1ms and 10ms). Software triggers are used for delays greater than 10 seconds.
6. Delay counter - one-shot to delay conversion after trigger 0s to 10s: 10-bit with four prescales (10µs; 100µs; 1ms and 10ms). Software delays are used for intervals greater than 10 seconds.
7. Serial Interface - two-way communication between the 68000 and the Analog Sub-System.
8. Measurement time-out interrupt if the A-D Converter locks up.
9. Write enable for non-volatile memory; and lockout circuit to detect illegal access.
10. Trigger conditioning:

    **GET** from IEEE 488 interface or front panel SAMPLE key.
    **TRIG** from rear panel BNC socket.
    **HOLD** from I/O Port.
    Internal interval counter.

11. 68000 interrupt handler - interrupts from serial interface, triggers and external pins (NMI; GPIA; ERR; FPINT; RTCINT).

### 5.2.7.4 Conversion Initiate (CI_R)

**Triggers**

Firmware determines the way triggers are treated in the digital ASIC trigger conditioning circuit. Triggers may be disabled, cause an interrupt, or produce CI_R depending on conditions. The maximum rate at which the analog sub-system can respond to CI_R's is determined by the mode of the A-D convertor and the need to collect measurement information via the serial interface between triggers. Three sources of triggers are:

**Internal:** Interval Counter - Hardware or Software
**External:** TRIG_F - rear Trigger BNC connector.
GET_R - from the IEEE bus.
SAMPLE - from the Front Panel key

A timer in the digital ASIC produces CI_R (20-40 CLK1 periods) from the various triggers.

Internal triggers are generated by the Interval Counter in the digital ASIC at a rate controlled over the data bus by the processor. Where the trigger period is less than 10 seconds a programmable free running counter produces 'direct' triggers at a rate set by the processor. For trigger intervals greater than 10 seconds, 'indirect' triggers are produced by software in response to RTX_R.

External triggers are conditioned; the conditioned triggers causing either an 'immediate' or 'delayed' trigger, or an interrupt, depending on the configuration set by the processor. In the case of an interrupt, the trigger is eventually produced from the interval counter via software.

If the interval between two external triggers is too short, the second is stored and acted upon at the earliest opportunity. If repetitive external triggers occur above the maximum rate allowed by the set configuration, triggering continues at the maximum possible rate and 'Trigger Too Fast' is flagged. The processor signals this to the I/O port via the data bus and U208-6 *(page 11.4-3)*.

To summarize trigger forms:

1. Internal triggers - Interval counter:
   Hardware: < 10 Seconds
   Software: > 10 Seconds
2. External triggers - Software
3. Direct triggers come from hardware.
4. Indirect triggers come from software.
5. Delayed triggers pass through the Delay Counter (max 10 Second delay).
6. Immediate triggers by-pass the Delay Counter.

In order to offer external control facilities (other than the IEEE bus), an I/O Port has been fitted in the instrument rear panel. This could be used; for example: in conjunction with the Rear Trigger input in a process control system.

The rear Trigger input is a BNC connector on the rear panel.

### 5.2.7.5 Display Management
*(page 11.4-4)*

Data to be displayed on the front panel is stored in RAM. The processor employs 'Bus Arbitration' so that the Display Management System can gain access to this information.

**Display Data Access**

When Display Management requires data, it asserts BR_L (Bus Request). In reply, the processor asserts BG_L (Bus Grant) to indicate that control of the bus will be released at the end of the current processor cycle. The end of the cycle is signalled to each of the control PALs by AS_L being cleared, which is decoded with BG_L by U107 (System Control PAL) as ST_BG_L.

This signal causes the Display Management system to take control, which it acknowledges by asserting BGACK_L (Bus Grant Acknowledge).

Display Management now has control of the bus. Signal DMA_L (Direct Memory Access) enables the RAM, and data is extracted using the Address and Data buses. Control of the bus is returned to the processor when BGACK_L is cleared.

**Anode Data**

DSHFT_R clocks anode data into the display's 100-bit serial register *(page 11.3-1)* as seven 16-bit words via DDATA_H. DLTCH_H latches this pattern when the next pattern is shifted in. The display is scanned by walking a Logic-1 along the 20-bit grid register, one step for each 7-word set of anode data. The Logic-1 is clocked by DLTCH_H.

**DDATA_H**

U309 and U310 form a 16-bit serial-in/parallel-out register to provide the serial data stream DDATA_H.

**RAM Addressing**

U304 is a ÷16 counter whose output DMA_REQ_H signals completion of each word to U305 and the Bus Arbitration System. U305 divides by seven and provides a word count for RAM addressing on WRDØ, WRDØ and WRDØ.

The output from the ÷20 counter U306/U307 is a character (grid) count used for RAM addressing via octal buffer U303.

Tthe divide-by-16 counter U304 is clocked by CLK0.5 through U302-8, U311-4 and U308-4. At the count of 15 the carry out bit U304-15 goes high setting DMA_REQ_H at U312-12. on the next edge of CLK0.5, BR_L is set at U312-8 to request bus control. While BR_L is set, the CLK0.5 input is disabled by U313/U302 and all counting and shifting is stopped.

The processor asserts BG_L but ST_BG_H stays low until AS_L is cleared. When AS_L goes high at the end of the processor cycle, ST_BG_H goes high and U313-6 is clocked low by CLK8 to assert BGACK_L.

As well as being the response to BG_L, BGACK_L provides an enable for the parallel-in/serial-out Display Data Shift Registers U309/U310.

CLK0.5 remains inhibited, now via U313-5, U311-1 to U302-12. U313-5 also sets U313-12 high, and on the next CLK8, DMA_L is set at U313-8. This clears BR_L.

DMA_L enables RAM U112 and U105 via SEL_RAM_L from U110-19 *(page 11.4-2)*. DMA_L also enables the address buffer U303, so the address set by WRDØ:2 and CHRØ:4 is applied to the address bus. The first of the seven anode data words is thus loaded into U309/U310 via the data bus.

In reponse to BGACK_L the processor clears BG_L, and hence ST_BG_H.

U313-9 going low removes the inhibit on CLK0.5 at U302-12, causes DMA_L to be cleared at U313-8, and thus removes the enable on address buffer U303.

DSHFT_R is produced from CLK0.5 via U302-8, U308-4 and U311-10. Sixteen edges of DSHFT_R load the U309/U310 data word into the display anodes serial register. The series of sixteen CLK0.5 clocks also produces another DMA_REQ_H at U304-15, so the DMA cycle is repeated.

U305 counts DMA_REQ_H to generate the seven-word count, U305-15 incrementing the character counter U306/U307 after each seven words, latching the pattern on the Front Panel. This causes the Logic-1 in the display grid register to be shifted to the next grid by DLTCH_H via U308-12.

WRD1, WRD2 and CLK0.5 are gated by U207-11 and U312-5 to produce DBLK_H which blanks the display while the last two of each group of seven words are being loaded.

DG20_H is produced at U308-8 from U307-15 after each set of 20 characters (140 words) to load a Logic-1 into the display grid register.

After a system reset, the display is blanked for approx. 500ms by R306/C302 to allow the RAM to be re-initialized by the processor; and to allow the display registers to synchronize with the Display Management address counters.

Display scan is inhibited by the action of DBLK_H in the display circuit.

The facility for display blanking by DOFF_H is not used in the 1281. DOFF_H is cleared by the processor via the data bus and U208-19 *(page 11.4-3)* at power up reset.

### 5.2.7.6 Keyboard Interrupt

*(pages 11.4-2 to 11.4-4)*

KB5 from the keyboard encoder sets the Key Press Latch by clocking U302-3. This signals FP_INT_L to the digital ASIC interrupt Handler at U203-39 *(page 11.4-3)*.

The digital ASIC sets the interrupt level '2' on IPL1 and IPL0/2 (U203-40/41) to indicate an interrupt to the processor.

The processor compares the interrupt level with its internal mask. Assuming that the interrupt is of higher priority, the processor completes the current instruction then sets its mask at level 2.

The processor then sets the interrupt level 2 on A1-A3, asserts AS_L and sets R_H/W_L high. At the same time FC0_H, FC1_H and FC2_H are set, asserting IACK_L at U107-19 *(page 11,4-2)*.

R_H/W_L and AS_L with IACK_L at U203-4/57/58 cause the digital ASIC to output the relevant exception number on BDØ:7. Access time-out is by U107 setting UIDTACK_L, which drives the processor via U110-16.

The processor is now in an exception cycle. From ROM it fetches the exception vector indicated by the digital ASIC. The two vector words hold the first of a series of addresses which contain the instructions to read the front panel keys.
(Note: should an interrupt of higher level occur (such as ERR_L from in-guard), the processor will terminate the read from the front panel.)

The processor places the 'Read Front Panel' address on the address bus. This is decoded to assert RDFP_L by the address decoder U111 at pin 19. RDFP_L carries out the following actions:

1. resets the Key Press Latch by U302-1;
2. enables the Keyboard Buffer U301;
3. causes DTACK_L to be asserted after 500ns via the digital ASIC access timeout circuit.

The Keyboard Buffer places the encoded key number at KBØ:5 onto the buffered data bus BDØ:7. The two-way buffer U201 (page 11.4-3) has been enabled by AS_L (IACK.AS_L) and its direction has been set by R_H/W_L. The keyboard code is thus passed via DØ:7 to the processor which takes appropriate action determined by the particular key which was pressed.

### 5.2.7.7 I/O Port Sk8

The I/O Port is a 'D' connector allowing the following TTL compatible inputs and outputs.

**Inputs:**

HOLD_L
: Input to the digital ASIC which may be used to disable triggering.

TRACK_H; SAVE_F
: Not used - Track and Hold options are not fitted in the 1281.

REAR TRIG
: Trigger input via SK9 to the digital ASIC trigger conditioning circuit.

**Outputs:**

DATA VALID_L
: Indicates that outputs are valid.

TRIG TOO FAST
: Indicates missed triggers.

HIGH LIMIT_L
: Asserted when the applied input signal is more positive than a limit preset via the instrument keyboard.

LOW LIMIT_L
: Asserted when the applied input signal is more negative than a limit pre-set via the instrument keyboard.

Note: The above outputs are driven by the processor via latch U208 on the buffered data bus. U208 is enabled by WR_LTCH_L from address decoding (U111-16, *page 11.4-2*). When limits are set they are stored in the user area of NV RAM.

NOT SAMPL_L
: Asserted between measurements to indicate that the input signal may be changed. This output is an inversion of the Digital ASIC output SMPL_L derived in the trigger conditioning circuit.

ANALOG 0V
: Separate ground to minimise processor noise on the Analog output.

ANALOG O/P
: DC level via the D-A converter. The output is bipolar with 2V representing full scale input on any range.

#### 5.2.7.8 Analog Output

Analog output voltage is derived from measurement data stored in RAM (corrected by calibration constants). The processor writes data to the D-A convertor U205 on BDØ:7 and D8:11. Data is latched into the DAC by SEL_WORD_L (UDS_L and LDS_L combined at U111-15 *page 11.4-2*). U205 is selected by WR_DAC_L from address decoding U111-13.

When all the data is Logic-1, the Analog Output is -2.45V. All data at Logic-Ø produces +2.45V. An output of 0V is theoretically produced for inputs between hex 7FF and hex 8ØØ. In practice the output, although linear, is initially offset and requires calibration.

D201 provides a +2.45V reference to the 'R/2R' DAC. The DAC's Analog ground is connected to current mirror U206-1. U206-7 is a conventional inverting amplifier which sums the DAC output with the mirrored analog ground current from the DAC. This provides bipolar operation and output drive.

R205 protects U206-7 output, C203 and C205 prevent oscillation and D202-D205 are clamps. The Analog output is filtered by R205 and C204.

#### 5.2.7.9 IEEE Interface

The IEEE controller (GPIA) U401 is connected to the IEEE bus via the buffers U402 and U403. Data is passed to and from the GPIA on the buffered data bus. Note that BDØ connects to D7, BD1 to D6 etc.

The GPIA is addressed via A1-A3, and runs on CLK4 to maintain bus handshake speed. It is enabled by SEL GPIA_L, derived from U111-18 *(page 11.4-2)* and read/write is selected by BR_HW_L from U107-17. LWR_L from U109-3 must also be asserted for the processor to be able to write to the GPIA.

When a valid Group Execute Trigger is received over the IEEE bus, it is transferred via the buffered data bus to U208 for decoding, then passes as GET_R from U208-16 to the digital ASIC. If triggers are allowed, CI_R is produced to initiate a measurement. Interrupts generated at U401-9 (GPIA_INT_L) are fed to the interrupt handler in the digital ASIC.

The buffers U402 and U403 are selected to Send or Receive by the GPIA U401-21. Additionally, U403 may be switched to controller mode by U401-30 (If for example there was a requirement for the 1281 to control its own 'CAL'). Special firmware would be required to employ this facility.

The GPIA has some internal de-bounce capability but extra provision has been made by fitting filter R401/C401 and R402/C402 to avoid problems which could arise due to external noise on IFC and REN.

Fig. 5.2.8.1

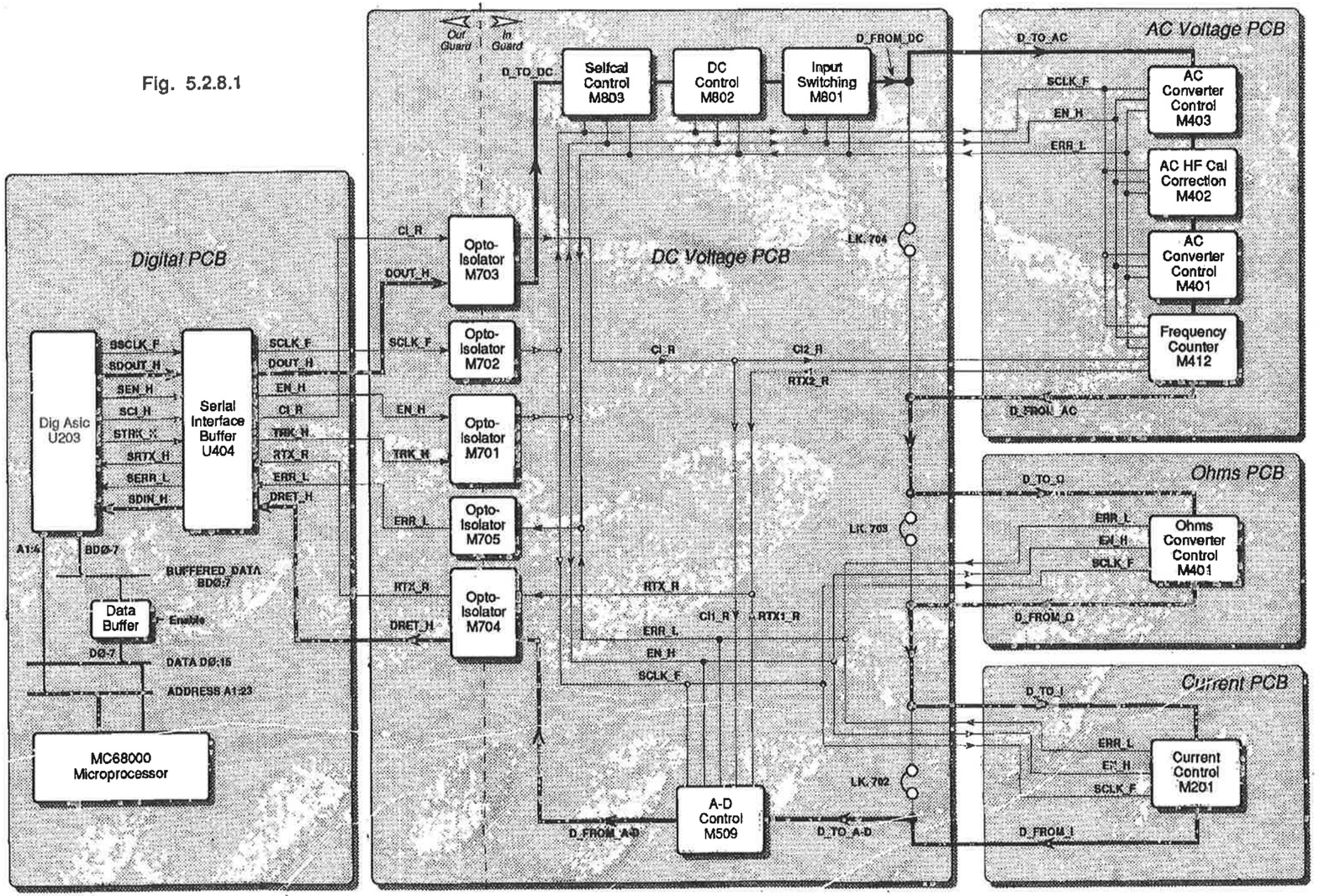



FIG. 5.2.8.1 SERIAL INTERFACE FUNCTIONAL LOOP

## 5.2.8 Serial Data Interface

### .8.1 Functional Block Diagram

Fig. 5.2.8.1 (opposite) shows the elements and routing of the Serial Data Interface.

### 5.2.8.2 Need for a Serial Interface

If the analog control signals and the necessary analog status signals were to be passed through the guard plane, each through its own dedicated isolator, then more than 50 isolators would be required. This would impose space penalties and introduce intolerable capacitive coupling and leakage between in-guard and out-guard circuits.

By passing a stream of data around an out-guard/in-guard serial loop, which needs only two isolators, the total number of active devices is reduced to seven (the TRK_H signal is not used in the 1271). This includes provision for two asynchronous signals (not directly connected with interface transfers) and three interface control signals.

### 5.2.8.3 Interface Control

**Processor Control of the Interface**

The Interface Controller is incorporated into the Digital ASIC. The 68000 processor controls the interface using A1:4 and DBØ:7, together with address decodes SEL_ULA_L, LDS_L, R_HW_L and AS_L. Signal UDTACK_L handshakes acknowledgement of sufficient access time (250ns).

There are three main states of the interface:

**WAIT:** The interface is quiescent, awaiting instructions from the processor.

**WRITE:** The processor commands a change of instrument analog state via the interface.

**READ:** Status data is passed back to the processor from the analog circuits.

The processor instructs the Interface Controller to change the state of the interface by writing to the ASIC's command register over the buffered data bus BDØ:7. The controller can find out the interface state and any status information by reading the ASIC's status register via BDØ:7.

The Interface Controller can instruct the ASIC to request a processor interrupt via the IPLØ:2 lines. When requested the processor responds by returning the same priority level via the FCØ:2 lines. When the processor reaches the interface interrupt in the interrupt queue, it services it by setting IACK_L low at the ASIC. This acts as a chip-select, and the interrupt data is read back to the processor via the buffered data bus. As a result the processor carries out the next step in the write or read cycle.

**Power-up and Reset**

The ASIC is placed into Reset condition at power-up. When it is released from reset, at this or any other time, the Interface Controller places the interface into the WAIT state. This causes all the in-guard Tx/Rx devices to take their serial registers off-line, and they become 'transparent' to any signals on the serial path, which effectively bypasses them.

From this point the processor controls the state of the interface, and via the interface, the instrument analog state.

**Changing the Instrument Analog State**

The processor commands the interface state to WRITE and a write cycle begins. Control data to be transmitted via the interface is passed over the buffered data bus in 'Long Words' (32 bits). This data is transferred over the interface in a series of 64-bit groups, each comprising four bytes of true data interlaced with four bytes of complement data. The ASIC implements the word-group conversion. The in-guard Tx/Rx devices are set to receive.

**Obtaining Measurement and Status Data**

To do this the processor commands the interface state to READ and a read cycle begins. The in-guard Tx/Rx devices are set to transmit. The 8-bit registers become transparent on the signal path. Measurement or status data to be returned from the A-D ULA and Frequency ULA are loaded into their serial registers, and are transmitted through guard to the digital ASIC.

## 3.4 Data and Control Lines

**DOUT_H and DRET_H**
The Digital ASIC is buffered from the opto isolators on the DC PCB by U403 *(page 11.4-5)*. From Fig.5.2.8.1 it can be seen that the data line loops around all the Tx/Rx devices in the analog sub-system, entering via the opto-isolator U803 on the DC PCB as DOUT_H, and returning via U805 as DRET_H.

**SCLK_F (Transfer Clock)**
Clock pulses on the SCLK_F line are fed to all Tx/Rx devices through U802 on the DC PCB. Their purpose is to clock the data round the serial loop.

**EN_H (Transfer Enable)**
This signal goes high to enable data transfers around the loop. The condition of the serial data line during the first four SCLK_F pulses when EN_H is high determines the 'Receive/Send' state of the in-guard Tx/Rx devices. When EN_H is low, the Tx/Rx devices are placed into 'WAIT' state.

**TRK_H**
This signal is not used.

**ERR_L (Transfer Error Warning)**
During a write cycle the Tx/Rx devices compare the transmitted bytes of true data against their transmitted complements. If there is any disparity, ERR_L is asserted. The ERR_L line remains high when there are no errors.

The ERR_L line can also be pulled low if a Tx/Rx device does not recognize the bit-pattern of its received true data as a valid command, or if its internal processing is defective.

**CI_R (Conversion Initiate)**
This signal is used to initiate an A-D conversion. Once the correct trigger is present, and the analog sub-system has been configured by data transfers, and any digital delays have expired, the CI_R line is set high. The rising edge of CI_R into U509 on the DC PCB initiates a reading conversion. At the same time, for AC measurements, the frequency counter M412 on the AC PCB is activated.

**RTX_R (Conversion and Count Complete)**
The A-D ULA (U509 on the DC PCB) has an open-collector output RTX1, which is pulled low during a conversion as a result of CI_R. Once the conversion is completed the A-D ULA turns its open-collector device off. Similarly the frequency counter (M412 on the AC PCB) has an open-collector output RTX2, which CI_R causes to be pulled to low.

Once the count is complete RTX2 is released from low. When both RTX1 and RTX2 have been released, pull-up resistors on the DC PCB set the RTX line to high. This is passed through isolator U805 to the Digital ASIC, where the rising edge signifies that the two operations are finished.

### 5.2.8.5 WRITE Cycle

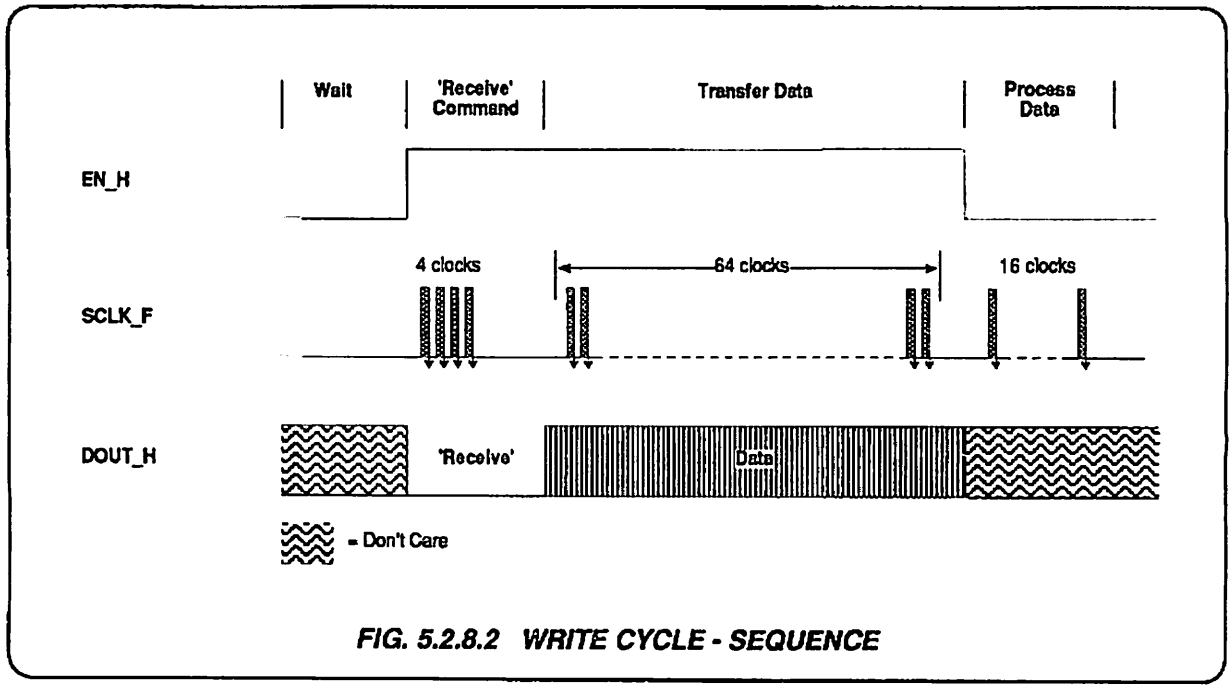



*FIG. 5.2.8.2 WRITE CYCLE - SEQUENCE*

There are four phases in the cycle, controlled by EN_H, SCLK_F and the data line DOUT_H itself. They are:

**Wait:**
EN_H is low, no clock pulses are present. All in-guard Tx/Rx devices ignore any data on the data line, which bypasses their serial registers.

**Instruct All Tx/Rx Devices to Receive:**
EN_H goes high to enable the data transfer, and DOUT_H is set low. Four SCLK_F pulses are transmitted, while DOUT_H is held low, to announce that the processor is about to command a change of instrument analog state. The in-guard Tx/Rx devices activate to receive data from DOUT_H, placing their serial registers into the data path. During the time taken to place the registers on line at the start of EN_H true, the inputs and outputs of the Tx/Rx devices are still shorted, so the whole of the signal path has time to fall to low.

**Transfer Data:**
EN_H remains high. The 64 serial data bits of the first group are injected into the data path via DOUT_H, a bit at a time, while 64 SCLK_F pulses clock the bits through the serial registers of the Tx/Rx devices. This transmission of 64-bit groups continues until the data is located in the correct Tx/Rx serial registers for the instrument's option fit. Each 8-bit device in fact introduces a 16-bit serial register into the data path, half for a true data byte, the other half for its following complement data byte. This allows error checking in the Process Data phase.

**Process Data:**
EN_H goes low to disable the data transfer. The data in the Tx/Rx serial data registers is held, as the registers are taken out of the data path. Sixteen SCLK_F pulses are transmitted which cause the Tx/Rx devices to check the true data against its complement.

If there is no corruption, the true control data is latched into the device's DIO lines (a similar checking facility is incorporated into the A-D and frequency counter ULAs, but correct true data is latched internally). The data is used to reconfigure the analog circuits controlled by the device.

If a device discovers an error, it pulls its ERR_L line low, and latches its DIO lines at high impedance. In this condition, a set of pull up/down resistors dominates the device's DIO output lines, setting a safe analog state.

ERR_L is an open-collector output *and* input. When it is pulled low for an error by one device, the change is detected by all the other devices in the loop, which also set their DIO lines to high impedance (but without latching). This causes the whole analog sub-system to revert to a safe condition.

There is a further benefit in latching only the device which detected the error. When fault-finding, if the Tx/Rx chips are removed one at a time, then the ERR_L line will remain low until the one which reported the error is removed. This locates the part of the data stream which is corrupted, as a lead-in to subsequent diagnosis.

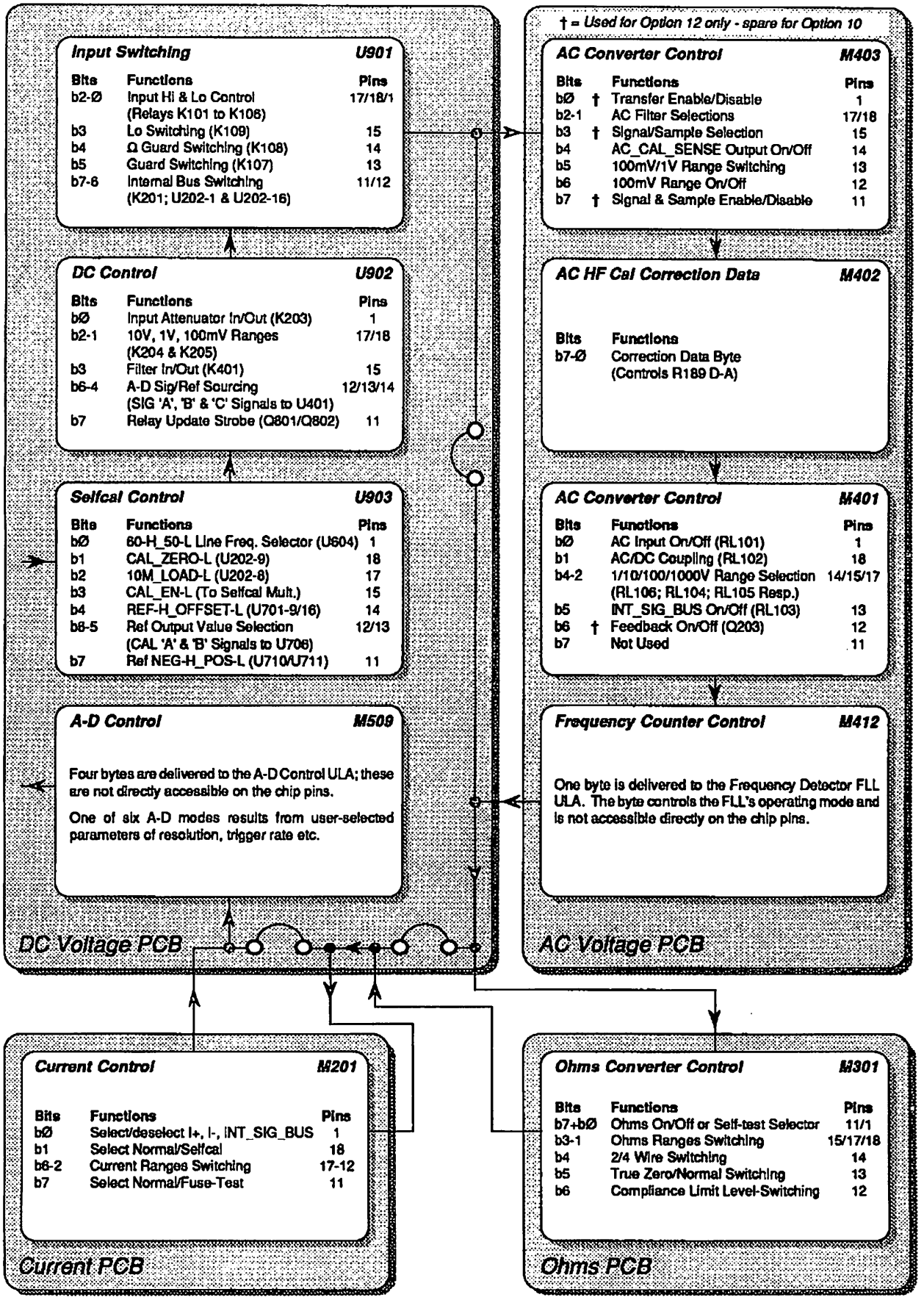



*FIG. 5.2.8.3 SERIAL INTERFACE REGISTERS - COMMAND DATA (DEVICES SET TO RECEIVE)*

### 5.2.8.6 READ Cycle

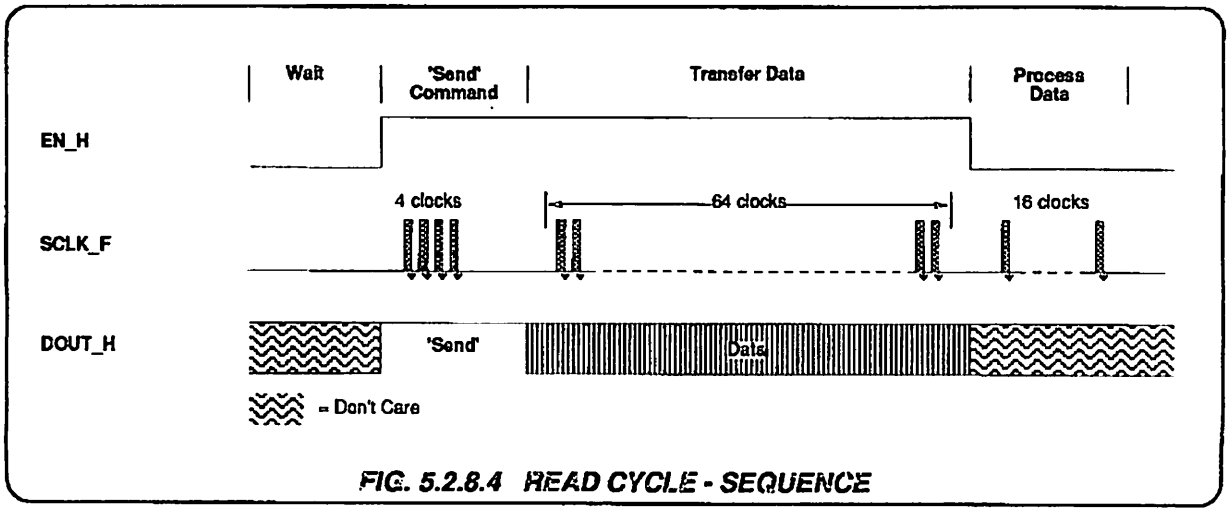



*FIG. 5.2.8.4 READ CYCLE - SEQUENCE*

There are four phases in the read cycle, also controlled by EN_H, SCLK_F and the data line DOUT_H. They are:

**Wait:**
EN_H is low, no clock pulses are present. All in-guard Tx/Rx devices ignore any data on the data line, which bypasses their serial registers.

**Instruct All Tx/Rx Devices into their Preset Send Modes:**
EN_H goes high to enable the data transfer. Four SCLK_F pulses are transmitted, while DOUT_H is held high, to announce that the processor is about to command the 'Send' devices to transmit data. The 8-bit in-guard Tx/Rx devices are preset in hardware as 'receiver only' and so assume the 'Wait' condition, in which they are transparent to signals on the serial data path. The A-D and Frequency ULAs activate to transmit data via DRET_H, placing their serial registers into the data path. During the time taken to place the registers on line at the start of EN_H true, the inputs and outputs of the Tx/Rx devices are still shorted, so the whole of the signal path has time to rise to high.

**Transfer Data:**
EN_H remains high. 64 preset serial data bits of the first group are injected into the data path via DOUT_H, a bit at a time, while 64 SCLK_F pulses clock the bits through the A-D and Frequency ULA serial registers. This transmission of 64-bit groups continues until the preset data is returned to the digital ASIC serial registers. The two ULAs introduce both true and complement data bytes, to permit error checking by the digital ASIC during the Process Data phase.

**Process Data:**
EN_H goes low to disable the data transfer. The data in the Tx/Rx serial data registers is held, as the registers are taken out of the data path. Sixteen SCLK_F pulses are transmitted which cause the two ULAs to check the preset data against its complement. During this time the ASIC checks the returned true and complement data from the ULAs.

If there is no corruption, the returned true data is transferred to the processor.

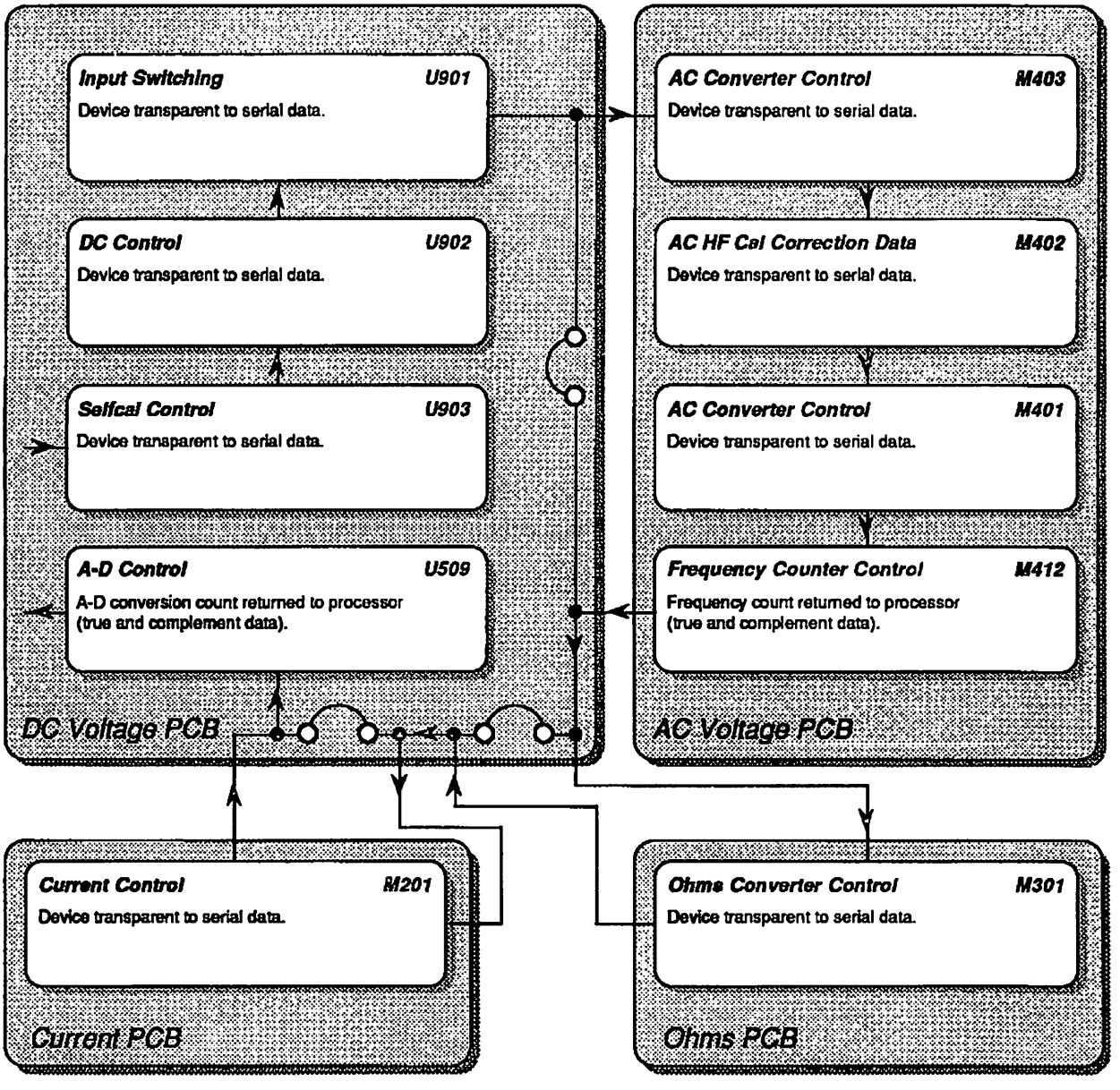



*FIG. 5.2.8.5 SERIAL INTERFACE REGISTERS - MEASUREMENT DATA (DEVICES SET TO SEND)*

### 5.2.8.7 Option Test

*N.B. It is assumed that all instruments will contain an A-D converter, so the A-D ULA is excluded from the Option Test procedure.*

**Introduction**

This is one of the first transfer commands from the processor to the Interface Controller following a Reset (including the power-up reset). Its is included so that the processor can discover which options are fitted in the instrument, to enable the correct firmware options to be selected: e.g. how many 64-bit groups are required for a complete transfer during the write cycle (the read cycle is fixed at one group only). The facility caters for recognition of other future options which may be fitted in place of the standard options. Option Test also serves to set the analog sub-system to a known safe state before it is configured into the default mode.

The 8-bit Tx/Rx devices are preset in hardware to act only as receivers, but they are designed so that this preset can be overridden when commanded via the serial interface. Once overridden, they can revert to 'receiver only' only when the override is cancelled by a write cycle, or after a reset.

The Option Test command generates three transfers, overriding the hardware preset. The first two are abbreviated Read cycles, which command all Tx/Rx devices (except the A-D ULA) to convert into 'Senders' and set their DIO lines at high impedance. The analog sub-system is thus configured safe by the dominant pull-up/down resistors on the DIO lines. This imposes a unique bit-pattern for each Tx/Rx, which is detected by the device as an input from the DIO lines, and is loaded (with its complement data) into the device's serial register in the serial data path.

The third transfer is a standard Read cycle, which passes the data from the Tx/Rx devices to the digital ASIC. After checking for errors, the ASIC releases the data for the processor to read. The processor interprets the unique bit-patterns as 'options fitted' information.

**Wait:**

EN_H is low, no clock pulses are present. All in-guard Tx/Rx devices ignore any data on the data line, which bypasses their serial registers.

**Instruct Tx/Rx Devices to Select Option Test Mode:**

EN_H goes high. Four SCLK_F pulses are transmitted, while DOUT_H is held high. EN_H immediately returns to low, and 16 SCLK_F pulses are transmitted to clock the 'Process Data' sequence in the Tx/Rx devices. Each in-guard Tx/Rx device (except the A-D ULA) interprets this sequence as the overriding 'All Send Option Data' command. It reconfigures itself as a sender, setting its DIO lines at high impedance and loading the DIO bit-pattern into its serial register. During the time taken to place the registers on line at the start of EN_H true, the inputs and outputs of the Tx/Rx devices are still shorted, so the whole of the signal path has time to rise to high.

To ensure that the Tx/Rx devices have enough time to reconfigure themselves, the instruction is repeated a second time.

**Instruct Tx/Rx Devices to Send Data:**

The processor commands a Read cycle to obtain the option state. Because the option fit is not known at this point, it is necessary for this cycle to return 4 x 64-bit groups (required for the possibility that the instrument is fully-loaded).

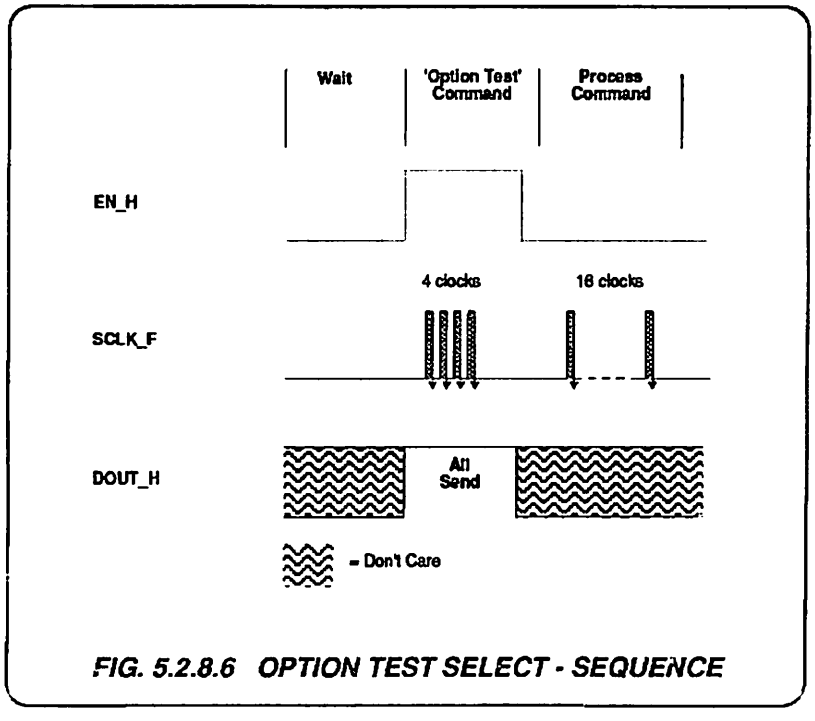



*FIG. 5.2.8.6 OPTION TEST SELECT - SEQUENCE*

## 3.8 Power On and Reset

### Interface Flushing

At power on, the digital master reset MR_L is asserted, to be turned off after 200ms-300ms. The Tx/Rx device serial data registers could power up any random condition, so they must be initialized. The first action by the processor on the interface is to flush the in-guard data path by 16 SCLK_F pulses, while DOUT_H and EN_H are held low. The Tx/Rx devices' are thus in the safe 'Wait' state, their DIO lines being at high impedance due to EN_H being low, serial data registers off-line, and serial data inputs and outputs shorted together. The 16 SCLK_F pulses are therefore sufficient to set the whole of the serial data path to low.

### Interface Reset

Two Write cycles are processed with DOUT_H remaining low. This time the Tx/Rx registers are put into the serial data path by EN_H high, and are all reset to zero by the low on the data path. This is a safe state, and after the reset the Tx/Rx devices return to 'Wait' state.

### Option Test

Two option test commands are transmitted to ensure that all Tx/Rx devices are forced to become senders, then a Read cycle is processed, using four 64-bit groups so that a complete test of all options will be completed if the instrument is fully loaded. If an interface error occurs at this time the processor will abort the option test, deal with the error, and then re-start the test.

The Tx/Rx devices remain in their 'Wait' condition, imposing the Power On Reset (default) condition on the analog sub-system, until a Write cycle is processed to change their serial register contents. The processor now knows the instrument's option fit, and so tailors subsequent interface operations to accommodate the correct number and positions of the serial registers in the serial data path.

### A-D Action

After the digital master reset has been removed, CI_R remains inactive until the option test has been successfully completed, to allow the A-D ULA to stabilize the A-D analog circuit. With 0V at its signal input, the A-D powers up with its integrator output positive, and the A-D ULA imposes +REF/256 to return this very slowly towards zero. Meanwhile, during the master reset period, the A-D and Frequency ULAs had released their open-circuit RTX_R outputs, which remain pulled to high.

After the Option Test has been completed successfully, a conversion is initiated by CI_R being set high for some 30ms. The rising edge of CI_R has the effect of imposing +REF at the A-D input, which rapidly drives the A-D output to zero, and the A-D starts a conversion with zero input. At the same time the RTX_R line is forced low. The processor waits for the RTX_R line to rise to high again to show that this first conversion has been completed. If this does not happen within 2.25 seconds, the processor assumes that an A-D fault is present.

A successful first conversion sets RTX_R back to high, and the interface power-on sequence is complete. Unless the instrument is commanded otherwise, the power-on default state persists, and the A-D is internally triggered continuously to produce 6.5-digit normal conversions (16 power line cycles).

**DATRON INSTRUMENTS FAILURE REPORT.**

Please complete all sections and return with your instrument.

Company: .....

Division: ..... Department/Mail Stop .....

User, Name: ..... Telephone ..... Ext .....

Serial number: .....

Datron Return Authorisation number ..... Date of failure .....

Brief description of fault: .....

.....

.....

.....

.....

**Fault details:**

is the fault present on all ranges? Yes ☐ No ☐ Not Applicable ☐

if no describe: .....

is the fault present on all functions? Yes ☐ No ☐ Not Applicable ☐

is the fault: Permanent ☐ Intermittent ☐

if intermittent under what conditions does the fault re-appear .....

.....

Does the instrument pass 'self test?' Yes ☐ No ☐

Any fail/error message displayed:

Now: Yes ☐ No ☐ if yes describe .....

.....

At the time of fault: Yes ☐ No ☐

if yes describe .....

.....

Prior to fault: Yes ☐ No ☐

if yes describe .....

.....

Is the instrument used on I.E.E.E 488 bus? Yes ☐ No ☐

Is the instrument normally enclosed in a rack? Yes ☐ No ☐

Approximate ambient temperature .....

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The acceptance of a quotation, of any goods supplied, advice given or service rendered includes the acceptance of the following terms and conditions and no variation of or addition to the same shall be binding upon us unless expressly agreed in writing by us. Any order shall be subject to our written acceptance.

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Unless previously withdrawn our quotation is open to acceptance in writing within the period stated or where no period is stated within thirty (30) days after its date. We reserve the right to correct any errors or omissions in our quotation. Unless otherwise stated all quotations are firm and fixed. The prices quoted are based on manufacture of the quantity and type ordered and are subject to revision when interruptions, engineering changes or changes in quantity are caused or requested by the customer.

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Payment shall be made net cash within thirty (30) days of delivery or in accordance with the payment terms set out in the quotation. Unless specifically stated to the contrary payment shall be in pounds sterling. In the event of any payment to us being overdue we may without prejudice to any other right suspend delivery to you or terminate the contract and/or charge you simple interest on overdue amounts at the rate of 2.5% above the ruling Bank of England Minimum Lending Rate. No payment to us shall in any circumstance be offset against any sum owing by us to you whether in respect of the present transaction or otherwise.

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If any contract or any part of it shall become impossible of performance or otherwise frustrated we shall be entitled to a fair and reasonable proportion of the price in respect of the work done up to the date thereof. For this purpose any monies previously paid by you shall be retained against the sum due to us under this provision. We may dispose of the goods as we think fit due allowance being made to you for the net proceeds thereof.

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If the purchaser shall become bankrupt or insolvent, or being a Limited Company commence to be wound up or suffer a Receiver to be appointed, we shall be at liberty to treat the contract as terminated and be relieved of further obligations. This shall be without prejudice to our right to claim for damages for breach of contract.

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