CALIBRATION AND SERVICING HANDBOOK

for

THE DATRON 4200

AUTOCAL AC STANDARD

Volume 1

Calibration and Servicing Information

850056

Issue 1 (May 1986)

For any assistance contact your nearest Datron Sales and Service Centre.
Addresses can be found at the back of this handbook.

Due to our policy of continuously updating our products, this handbook may contain minor differences in specification, components and circuit design to the instrument actually supplied. Amendment sheets precisely matched to your instrument serial number are available on request.

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DANGER
HIGH VOLTAGE

THIS INSTRUMENT IS CAPABLE OF DELIVERING

A LETHAL ELECTRIC SHOCK!

FRONT or REAR terminals carry the Full Output Voltage.

THIS CAN KILL!

Guard terminal is sensitive to over-voltage

It can damage your instrument!

Unless **you** are **sure** that it is **safe** to do so,
DO NOT TOUCH the
I+ I− Hi or **Lo leads** and **terminals**

DANGER

CONTENTS

ILLUSTRATIONS

SECTION 1

CALIBRATION

1.1 INTRODUCTION

1.1.1 Manufacturer's Initial Calibration

The 4200 is fully calibrated before leaving the factory, and remains within the appropriate specification for the time periods detailed in Section 6 of the User's Handbook.

Caution

Removal of the Top Ground/Guard Assembly invalidates the manufacturer's calibration certification.

1.1.2 Need to Recalibrate

Sections 1.2 to 1.5 detail the procedures necessary to recalibrate instrument functions to known specifications. The occasions for recalibration are as follows:

1. PERIODIC ROUTINE AUTOCALIBRATION

The specifications for the 4200 are based on standard intervals of up to 24 hours, 90 days or 1 year from calibration. Users may wish to choose alternative schemes, accounting for:

a. The accuracy required when in use,

b. The scheduled calibration intervals normally adopted by the user's organization, and

c. The instrument specifications (User's Handbook Section 6)

2. RE-STANDARDIZATION

Occasions may arise when it is necessary to trim the instrument's internal Master Reference.

For example, when the 4200 is to be made traceable to a different National Standard, after transportation from one country to another.

The procedure for "STD" autocalibration is detailed in Section 1.2.8.
(Refer to Section 1.2.8, para 3, note C).

3. SPOT FREQUENCIES

The 4200 stores the spot frequencies, and their amplitude corrections, in memories which are separate from those used for wideband corrections.

Enhanced accuracy is obtained as any flatness errors in the wideband correction are eliminated. Accuracy tables are given in Section 6 of the User's Handbook, with an example showing Spot F linearity.

4. BATTERY CHANGE

The Lithium battery which powers the non-volatile calibration memory should be replaced after 5 years (Refer to Section 5.3).

After replacement, a full Pre-calibration is required (Section 1.4) followed by a Routine Autocalibration (Section 1.2).

5. CRITICAL PARTS

Recalibration (or Verification) is necessary after replacement of a critical PCB assembly or a critical component.

These are listed in Table 1.1, indicating the extent of the recalibration necessary.

1.1.3 Recalibration Procedures in this Section

(See Section 7 of the User's Handbook for Verification Procedures).

Routine Autocalibration
(Section 1.2)

The Routine Calibration procedures are sufficient for all normal recalibration purposes, except when Pre-cal is called for (Refer to Table 1.1).

Remote Calibration over the IEEE 488 Bus
(Section 1.3)

Section 1.3 describes the device-dependent commands necessary for routine calibration of the 4200 over the IEEE 488 bus, as a supplement to Section 5 of the User's Handbook. A guideline example is given, but this needs to be adapted for the bus controller in use.

Pre-calibration Procedures
(Section 1.4)

In an initial internal calibration process at manufacture, certain "Pre-cal" parameters are established in a special calibration memory.

Under certain conditions (detailed in Table 1.1) these parameters need to be re-established by the 'Pre-Cal' procedure in Section 1.4, before the Routine Autocalibration of Section 1.2.

Current Option Internal Adjustment
(Section 1.5)

If the Power Supply/Current Heatsink has been changed it may be necessary to adjust the quiescent bias current (I_Q) by internal adjustment. Refer to Section 5.4 for further information.

Assembly	Components Replaced	Precal required	Routine recal
Digital (7.2)	Complete Assembly	Full	Full
	Lithium Battery (Sect. 5.3)	Full	Full
	Non-volatile RAM (M10/M23)	Full	Full
	Non-volatile RAM Supply-Commutator components	Full	Full
Reference Divider (7.4)	Complete Assembly	Full	Full
	Reference Assembly (7.4-7)	Full	Full
	Any set of main, guard or LSD switch FET's	Full	Full
	Reference Buffer	Full	Full
	Switch Driver Flip Flops or their preselected resistors	Full	Full
	R79	Full	Full
Output Control (7.5)	Complete Assembly	—	Full
Sine Source (7.6)	Complete Assembly	Specification Verification at user's discretion	
AC (7.7)	Complete Assembly	—	Full
	Sense Amplifier	—	Full
	Reference Inverter	—	Full
	AC/DC Transfer & Integrators	—	Full
Current (7.8)	Complete Assembly	—	All I Ranges
	M8 and associated components	—	
	Current Shunts		
	Feedback resistor R45		
All Other Assemblies Not Specified Above		Specification Verification at user's discretion	

TABLE 1.1 LIST OF CRITICAL PCBS AND COMPONENTS

1.2.1 Introduction

The 4200 possesses excellent short and long term stability. Some users will wish to maintain the highest accuracy by recalibrating at short intervals (e.g. every 24 hours). In these cases, recalibration of the 4200 becomes a routine task. For this reason, Routine Autocalibration procedures are repeated in Section 8 of the User's Handbook. It is emphasized that the 4200 can be used immediately after recalibration.

1.2.2 The 4200 Autocal Feature

Full or part calibration may be carried out for all routine purposes from the front panel. Removal of covers is unnecessary, therefore avoiding thermal disturbance. Calibration corrections are stored in an internal memory which remains energized by a battery even when the instrument power supply is switched off. The life of the battery is estimated at 10 years, and it is normally changed at 5 year intervals. On power-up, the 4200 performs a self-test which includes a check of the contents of the calibration memory.

1.2.3 Equipment Requirements

This summary relates to the recommended method of calibrating the 4200:

AC VOLTAGE
(IV - 1000V Full Range Values and 10V Range Linearity)

An Adjustable DC Voltage Source of suitable accuracy.
Example:
Datron 4000 or 4000A Autocal Standard.

An AC/DC Thermal Transfer Standard capable of operating over the range 1V to 1100V RMS.

AC VOLTAGE
2-WIRE COMPENSATION AT HIGH FREQUENCY
(1V and 10V Full Range values)

An AC voltmeter of suitable accuracy.
Example: Datron 1081

AC MILLIVOLTS
(1mV - 100mV Full Range Values)

At LF and HF;
An AC DVM of suitable accuracy and frequency response.
Example: Datron 1081 or similar.

at LF;
A commercially-available Inductive Voltage Divider of suitable accuracy and frequency response; with ratios of 10:1, 100:1 and 1000:1.

at HF;
The 4200 under test with the correction figure for 10% of its 10V Range at HF.

AC CURRENT
(1mA - 1A Full Range Values)

A DC Current Source of suitable accuracy, and an AC/DC Thermal Transfer complete with a set of Calibrated Thermal-Transfer Current Shunts of suitable accuracy.

AC CURRENT (Alternative Method)
(1uA - 1A Full Range Values)

A set of calibrated AC Shunts of suitable value and accuracy, and

An AC DVM of suitable accuracy and frequency response.
Example: Datron 1081 or similar.

1.2.3.1 Notes on the Use of the Thermal Transfer

Four points are important:

1. **Start with OUTPUT OFF.**
The 4200 should be connected to the Thermal Transfer Standard only when the 4200 OUTPUT OFF LED is lit. (With Output OFF, the I+, I−, Hi and Lo terminals are at high impedance).

2. **Sensitivity.**
Always set the Thermal Transfer Standard to its lowest sensitivity before connecting up. Increase sensitivity when necessary to obtain the required input level.

3. **WARNING**
During Performance checks and calibration the full range voltage is present at the Thermal Transfer Standard input terminals. On 1000V checks this voltage is potentially lethal, so EXTREME CAUTION must be observed when making adjustments to the Thermal Transfer Standard sensitivity.

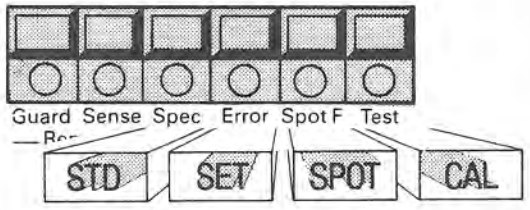
4. **CAUTION**
The Thermal Transfer Standard used must be able to withstand peak voltages up to 1600V between its input terminals. Such voltages may be present during the time that the 4200 is ramping from zero to 1100V Full Scale after setting OUTPUT ON.

1.2.4 Interconnections

Interconnection instructions in this section are necessarily simple and basic. It is recognised that they may need to be adapted to meet an individual user's requirements. It is assumed that users will possess knowledge of the operation and use of standards equipment.

1.2.5 Calibration Modes

Special keys are used in the Autocal mode. They are illustrated below:



The three keys labelled **STD, SET** and **SPOT** preselect alternative calibration modes. To finally implement any calibration, the **CAL** key must be pressed.

Fig. 1.1 CALIBRATION MODES

These keys are activated by a simple procedure:

On the rear panel there are two switches: the IEEE 488 address switch, and a security keyswitch labelled 'RUN/CAL ENABLE'.

By setting the address switch to 31 (ADD 11111) for Front Panel calibration, and the keyswitch to CAL ENABLE; four of the front panel 'MODE' keys are reassigned to calibration functions, permitting access to the correction memories.

When these modes are active, the legend 'cal' is presented on the MODE display.

1.2.5.1 General Procedure

The OUTPUT display is set to the Calibration Standard value, the 4200 output is switched ON, and one of the calibration mode preselector keys (STD, SET or SPOT) is pressed. The 4200 output is adjusted to equal the Calibration Standard value, and the CAL key is pressed to execute the calibration.

1.2.5.2 Autocal Facilities

SET — The SET key allows calibration to any value between 20% and 200% of nominal Full Range value (20% to 110% on 1000V range). If, for instance, an adjustable DC voltage standard is not available, the SET key permits the 4200 to be calibrated against a Thermal Transfer standard whose reference is a buffered bank of Standard Cells.

SPOT — When SPOT is pressed, the 4200 assumes that the spot frequency is to be changed, and so defaults frequency to 1kHz. When used with SET, SPOT calibration can be carried out within 10% of full range value, but when SPOT is used without SET, the 4200 assumes that the calibration is to be at Full Range. After SPOT calibration, selecting Spot F at the calibrated value achieves the highest possible specification. For Recall procedures see the User's Handbook Section 4, page 4-11.

STD — The STD key allows a user to trim the value of the internal Master Reference voltage. The facility can be used to correct for any long term drift, or to avoid a full recalibration of the 4200 when Laboratory References have been re-standardized. STD calibration effectively changes the gain of all voltage and current ranges in the same ratio, by a simple procedure available on either the 1V or 10V range.

CAL — The CAL key executes, then cancels, the preselected AUTOCAL mode.

CAL only — If the CAL key is pressed without first pressing SET, SPOT or STD, the 4200 assumes that the selected range is to be calibrated at the exact Full Range, at either LF or HF or both.

1.2.6 General Notes

Remote Sense is available as follows:

1V 10V 100V 1000V	- Local/Remote Sense
1mV 10mV 100mV	- Local Sense only
All current ranges	- not applicable

(Local = 2-wire sense; Remote = 4-wire sense)

Output must be OFF to change sense connection (except that Remote changes automatically to Local when switching to Millivolt Ranges).

On 1V and 10V ranges a Local/Remote difference correction can be stored; for the calibration procedure refer to Section 1.2.9.

Upranging — OUTPUT OFF Default.
The 4200 cannot enter High-Voltage State (>75V) with OUTPUT ON. Consequently, when ranging-up, the operating system allows the upranging to occur, but defaults to OUTPUT OFF for two specific cases:

a. When upranging to the 1000V Range,
b. When upranging to the 100V Range; to a voltage of 75V or more.

Otherwise, OUTPUT remains ON when changing OUTPUT RANGE (refer to User's Handbook Section 4, pages 4-7 and 4-8).

High Frequency Calibrations. Several iterations may be required to achieve satisfactory calibration; particularly if the initial errors are large, or if the Transfer System being used imposes a long calibration time.
Repeat the procedure as necessary.

1000V Range Calibration Sequence: LF calibration must be completed first. However HF1/HF2 bands may, if the user requires, be calibrated in reverse order.SET mode must be used for 700V/HF2.

SPOT Memory Erasure. To prevent unwanted calibrations at unused spot frequencies, it is possible to 'Uncalibrate' any spot frequency on any range. The procedure is:

Select **Zero** Output, set **OUTPUT ON** and Press **CAL.** When the CAL-ENABLE/RUN Switch is set to RUN, any subsequent selection of that particular Spot F will cause the message 'SFX---' to appear on the MODE/FREQUENCY display (X is the store number). This indicates that the spot is uncalibrated.

1.2.7 Calibration Sequence

The sequence of operations for full calibration of the 4200 Autocal Standard is given below:

Preparation	Section 1.2.7.1
AC Voltage	1.2.8
2-wire HF compensation	1.2.9
AC Current	1.2.10
Return to use	1.2.7.2

WARNING: During performance checks and calibration a common mode voltage equal to the full range voltage may be present at the Thermal Transfer input terminals. On 1000V checks this voltage is potentially lethal, so EXTREME CAUTION must be observed when making adjustments to the Thermal Transfer sensitivity.

CAUTION: The Thermal Transfer Standard used must be able to withstand peak voltages up to 1600V between its input terminals. Such voltages may be present during the time that the 4200 is ramping from zero to 1100V Full Scale after setting OUTPUT ON.

1.2.7.1 Preparation

Before any calibration from the front panel is carried out, prepare the 4200 as follows:

1. Turn on the instrument to be checked and allow minimum of 4 hours to warm-up in the specified environment.
2. IEEE 488 Address switch:
   Set to ADD 11111 as shown (Address 31).
3. CALIBRATION ENABLE Key switch (Rear Panel).
   Insert Calibration Key and turn to ENABLE.

These actions activate the four calibration modes (labelled in red), and present the 'cal' legend on the MODE display.

4. Ensure that the OUTPUT OFF LED is lit.

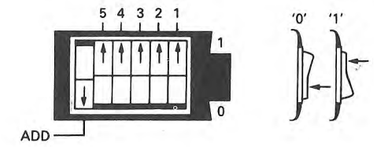
1.2.7.2 Return to Use

When any calibration is completed, return the 4200 to use as follows:

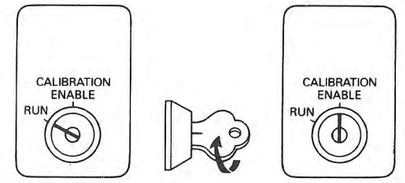
1. Ensure that the OUTPUT OFF LED is lit.
2. CALIBRATION ENABLE key switch (Rear Panel):
   Turn to RUN and remove the calibration key.
3. IEEE 488 Address switch:
   Restore to the correct address if the 4200 is to be used in an IEEE 488 system.

The activation procedure is illustrated below:

IEEE 488 Address Set to: ADD 11111 (Address 31)

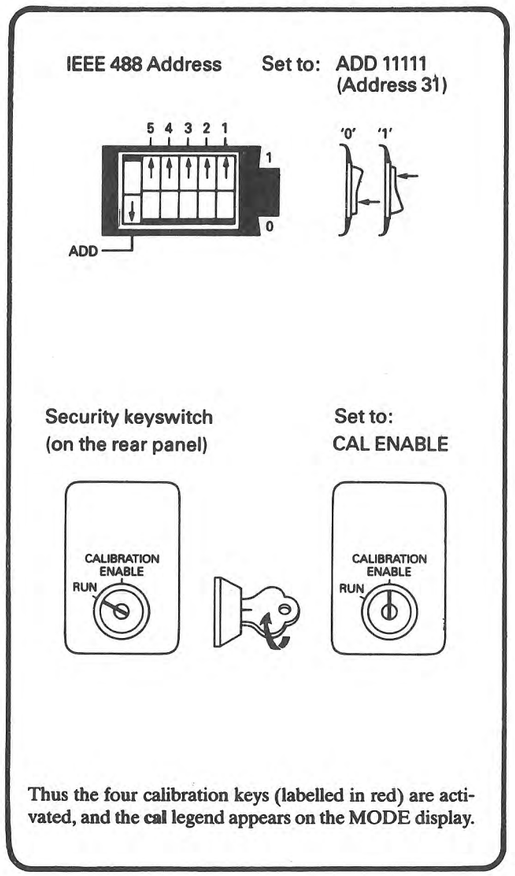


Security keyswitch (on the rear panel) Set to: CAL ENABLE



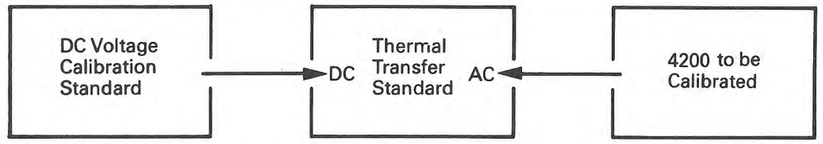
Thus the four calibration keys (labelled in red) are activated, and the **cal** legend appears on the MODE display.

The activation procedure is illustrated below:



Thus the four calibration keys (labelled in red) are activated, and the cal legend appears on the MODE display.

1.2.8 AC Voltage Full Range Calibration (1V–1000V)
(Using Thermal Transfer Standard and DC Calibration Standard)



Calibrate the 4200 at or close to the calibration points in the table, selecting SET and/or SPOT as required as part of the following procedure:

WARNING:

THE TERMINALS MARKED WITH THE SYMBOL CARRY THE OUTPUT OF THE 4200. THESE TERMINALS AND ANY OTHER CONNECTIONS TO THE LOAD UNDER TEST COULD CARRY LETHAL VOLTAGES. UNDER NO CIRCUMSTANCES SHOULD USERS TOUCH ANY OF THE FRONT (OR REAR) PANEL TERMINALS UNLESS THEY ARE FIRST SATISFIED THAT NO DANGEROUS VOLTAGE IS PRESENT.

Note

Any existing stored HF 2-wire compensation is cleared during normal 4-wire HF calibration. The procedure in Section 1.2.9 allows a user to re-establish HF compensation for 2-wire measurement.

Nominal Cal. Points for 1V to 1000V Ranges.

DC Standard OUTPUT Voltage	4200 OUTPUT RANGE/ FREQUENCY	4200 Nominal OUTPUT Voltage	Freq. Band set by 4200
1.000000V	1V 1kHz	1.000000V	LF
1.000000V	1V 1MHz	1.000000V	HF
10.00000V	10V 1kHz	10.00000V	LF
10.00000V	10V 1MHz	10.00000V	HF
100.0000V	100V 1kHz	100.0000V	LF
100.0000V	100V 100kHz	100.0000V	HF
1000.000V	1000V 1kHz	1000.000V	LF
1000.000V	1000V 30kHz	1000.000V	HF1

700V at 100kHz:
'SET' Calibration must be employed.

700.000V	1000V 100kHz	700.000V	HF2

1. **4200 & DC Voltage Standard**
With OUTPUT OFF, connect to the Thermal Transfer AC and DC inputs, respectively.

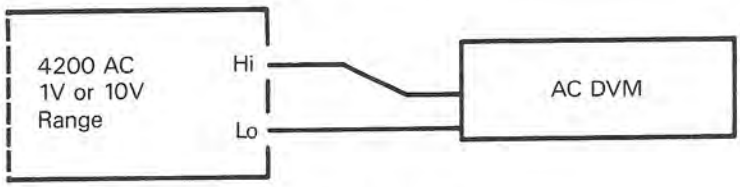
2. **Thermal Transfer Standard**
Configure for DC measurement at the required Calibration Voltage.

3. **DC Voltage Calibration Standard**
Set to the Cal. voltage, OUTPUT ON.

4. **Thermal Transfer Standard**
   a. Adjust for Null at the Cal. Voltage.
   b. Configure for AC measurement at the Cal. Voltage.

5. **4200**
   a. On AC FUNCTION, select the required OUTPUT RANGE.
   b. Select the required FREQUENCY RANGE (or if a Spot Frequency is to be calibrated: Press SPOT and select F1 - F5).
   c. Use FREQUENCY ↑↓ keys to display the required Cal. Frequency.
   d. Use OUTPUT ↑↓ keys to display the required Cal. Voltage (if at Nominal Full Range, merely press the Full Range key).
   e. Set 4200 OUTPUT ON (and if NOT at Nominal Full Range, Select SET).
   f. Use the OUTPUT ↑↓ keys to adjust the OUTPUT Display reading to obtain a null on the Thermal Transfer.
   g. Execute the calibration by pressing the CAL key (and if calibrating a Spot Frequency, repress the SPOT key to deselect).

1.2.9 AC Voltage - HF 2-wire Compensation (1V & 10V range).
(Using an AC DVM)



Calibration of HF 2-wire Compensation

On the 1V and 10V ranges there are two HF calibration memories. One holds the correction value obtained during Remote Sense (4-wire) 'wideband' calibration; the other contains a 2-wire HF compensation value which is added to the wideband correction, when Remote Sense is not selected (local sense).

During a 4-wire HF calibration on the 1V or 10V range, the stored HF 2-wire compensation value is cleared to zero. Any 4-wire HF calibration to be performed must therefore be completed before the 2-wire compensation is executed.

Calibrate the 4200 at or close to the calibration points in the table, selecting SET as required.

Nominal Cal. Points for 2-wire HF Compensation.

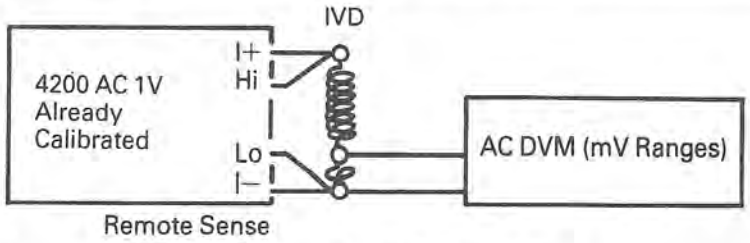
DC Standard OUTPUT Voltage	4200 OUTPUT RANGE/ FREQUENCY	4200 Nominal OUTPUT Voltage	Freq. Band set by 4200
1.000000V	1V 1MHz	1.000000V	HF
10.00000V	10V 1MHz	10.00000V	HF

1. **4200 & AC Voltmeter**
With 4200 OUTPUT OFF, make 4-wire connections between the 4200 and the AC DVM.

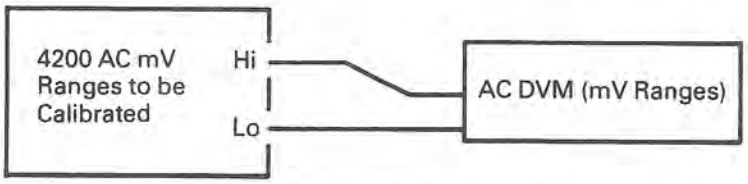
2. **AC Voltmeter**
Configure for AC measurement at the required Calibration Voltage.

3. **4200**
   a. On AC FUNCTION, select the required OUTPUT RANGE.
   b. Select the required FREQUENCY RANGE.
   c. Use the FREQUENCY ↑↓ keys to display the required Calibration Frequency.
   d. Use the OUTPUT ↑↓ keys to display the required Calibration Voltage.
   (If at Nominal Full Range, merely press the Full Range key.)

4. **HF 2-wire Calibration Sequence**
   a. Set 4200 OUTPUT ON (and if NOT at Nominal Full Range, Select SET).
   b. Record the DVM reading.
   c. Set 4200 OUTPUT OFF.
   d. On the 4200 deselect Remote Sense.
   e. Connect the DVM to the 4200 Hi and Lo terminals for 4-wire measurement of the 4200 2-wire output.
   f. Set 4200 OUTPUT ON.
   g. Use the 4200 OUTPUT ↑↓ keys to display the DVM reading recorded at (b).
   h. Press 'CAL'



Standardization of DVM Millivolt Ranges



Calibration of 4200 LF Millivolt Ranges

Calibrate the 4200 at or close to the calibration points in the table, selecting SET and/or SPOT as required, as part of the following procedure:

Note:
It is assumed that for a SPOT calibration, the 1V Range has already been Spot calibrated at the required calibration point.

Nominal Cal. Points for Millivolt Ranges.

IVD Ratio (1V Range to mV Range)	4200 OUTPUT RANGE/ FREQUENCY	4200 Nominal OUTPUT Voltage	Freq. Band set by 4200
10 : 1	100mV 1kHz	100.0000mV	LF
100 : 1	10mV 1kHz	10.0000mV	LF
1000 : 1	1mV 1kHz	1.0000mV	LF

1. **4200, IVD and AC DVM**
With OUTPUT OFF, connect the circuit for Standardization.

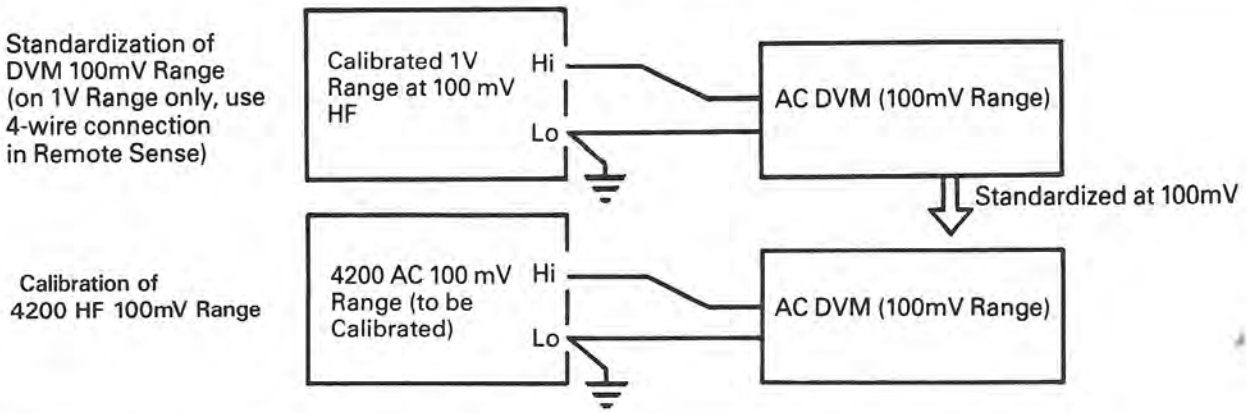
2. **IVD**
Set the ratio as required for the Millivolt Range to be calibrated.

3. **AC DVM**
Configure for measurement at the required Calibration Point.

4. **4200**
   a. On AC FUNCTION, select 1V RANGE.
   b. Select the required FREQUENCY RANGE (or if a Spot Frequency is to be calibrated: Press SPOT and select F1 - F5).
   c. Use FREQUENCY ↑↓ keys to display the required Calibration Frequency.
   d. Use OUTPUT ↑↓ keys to display the required IVD input voltage.
   (If at Nominal Full Range, merely press the Full Range key.)
   e. Set OUTPUT ON; note DVM reading as 'V1'.
   f. Set OUTPUT OFF, and reconnect the circuit for Calibration.
   g. Select the required Millivolt OUTPUT RANGE.
   h. Use OUTPUT ↑↓ keys to set the Calibration Voltage on the OUTPUT Display.
   (If at Nominal Full Range, merely press the Full Range key.)
   j. Set 4200 OUTPUT ON (and if NOT at Nominal Full Range, Select SET).
   k. Use the ↑↓ keys to adjust the OUPUT Display reading to obtain 'V1' on the DVM.
   l. Execute the calibration by pressing the CAL key (and if calibrating a Spot Frequency, repress the SPOT key to deselect). Set OUTPUT OFF.

1.2.11 Millivolts (HF) Full Range Calibration (1mV–100mV)

(Using calibrated 4200 1V and 10V Ranges, 10% Range Correction Factor and AC DVM)



N.B.

These Calibrations are not fully traceable. Calibrate the 4200 at or close to the calibration points in the table, selecting SET and/or SPOT as required, as part of the following procedure:

Note:

It is assumed that the 1V and 10V Ranges have been Wideband-calibrated (and for SPOT calibration, the 1V Range has already been Spot calibrated) at the required HF calibration points.

Nominal Cal. Points for HF Millivolt Ranges.

4200 OUTPUT RANGE/ FREQUENCY	4200 Nominal OUTPUT Voltage	Freq. Band set by 4200
100mV 1MHz	100.0000mV	HF
10mV 1MHz	10.0000mV	HF
1mV 1MHz	1.0000mV	HF

1. 4200 and AC DVM

a. Measure 10.00000V output on the 10V Range at the HF Calibration Frequency using the Thermal Transfer.
Note the reading: call it 'V1'.

b. Measure 1.00000V output on the 10V Range at the HF Calibration Frequency using the Thermal Transfer.
Note the reading: call it 'V2'.

c. Divide V1 by V2; divide the result by 10. This gives the 10% Range Correction Factor, 'C'.

$$C = \frac{V1}{10 \times V2}$$

This factor subsequently corrects a DVM measurement at 10% of one range, to standardize the DVM for calibration of the next millivolt range down.

d. With OUTPUT OFF, connect the circuit for Standardization.

2. 4200

a. On AC FUNCTION, select 1V OUTPUT RANGE.

b. Select the required FREQUENCY RANGE (or if a Spot Frequency is to be calibrated: Press SPOT and select F1 - F5).

c. Use FREQUENCY ↑|↓ keys to display the required Calibration Frequency.

d. Using the OUTPUT ↑|↓ keys, adjust the OUTPUT Display to the 100mV Calibration Voltage on the 1V Range.

e. Set the 4200 OUTPUT ON and note the DVM reading. Multiply the reading by 'C', and note the results as 'Vc'.
(If the DVM being used is a Datron Autocal instrument, the Maths function can do this automatically.)

f. With OUTPUT OFF, connect the circuit for Calibration.

g. Set 4200 OUTPUT OFF, select 100mV Range, and again use the OUTPUT ↑|↓ keys to set the OUTPUT Display to the Calibration Voltage.
(If at Nominal Full Range, merely press the Full Range key).

h. Set 4200 OUTPUT ON (and if NOT at Nominal Full Range, Select SET).

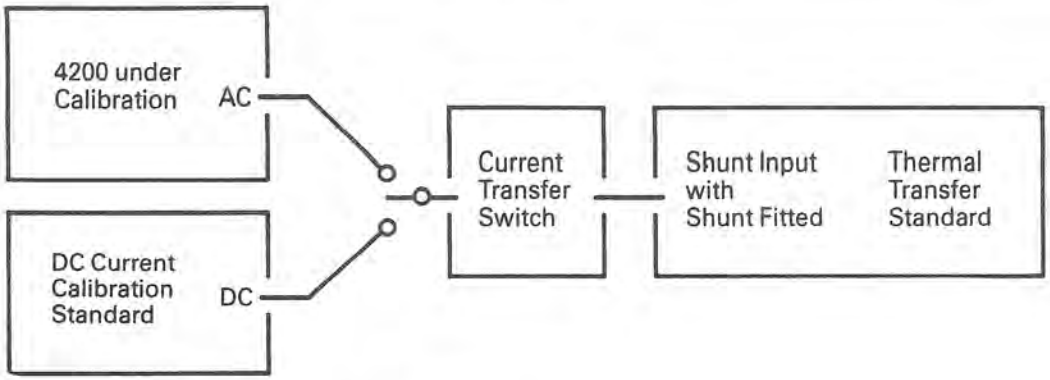
j. Adjust the OUTPUT ↑|↓ keys for a reading of 'Vc' on the DVM.

k. Execute the calibration by pressing the CAL key (and if calibrating a Spot Frequency, re-press the SPOT key to deselect). Set OUTPUT OFF.

l. Repeat operations 2 (a) to (k), selecting 10mV on the 100mV Range to standardize the DVM, and calibrating the 10mV Range, using the same correction factor 'C'.

m. Repeat operations 2 (a) to (k), selecting 1mV on the 10mV Range to standardize the DVM, and calibrating the 1mV Range, using the same correction factor 'C'.

1.2.12 Current Full Range Calibration (1mA–1A)
(Using Thermal Transfer, Current Shunts and DC Current Standard)



Calibrate the 4200 at or close to the calibration points in the table, selecting SET and/or SPOT as required, as part of the following procedure:

Calibrate 1mA Range only if the Thermal Transfer is adequately calibrated at these levels.

Nominal Cal. Points for 1mA to 1A Ranges.

DC Standard OUTPUT Current	4200 OUTPUT RANGE/ FREQUENCY	4200 Nominal OUTPUT Current	Freq. Band set by 4200
1.000000mA	1mA 300Hz	1.000000mA	LF
1.000000mA	1mA 5kHz	1.000000mA	HF
10.00000mA	10mA 300Hz	10.00000mA	LF
10.00000mA	10mA 5kHz	10.00000mA	HF
100.0000mA	100mA 300Hz	100.0000mA	LF
100.0000mA	100mA 5kHz	100.0000mA	HF
1.000000A	1A 300Hz	1.000000A	LF
1.000000A	1A 5kHz	1.000000A	HF

1. **Thermal Transfer Standard**
Configure for DC measurement at the required Calibration Current and connect the appropriate shunt.

2. **DC Current Standard**
   a. With OUTPUT OFF, connect across the Thermal Transfer shunt, and set to the required Calibration Current.
   b. Set OUTPUT ON.

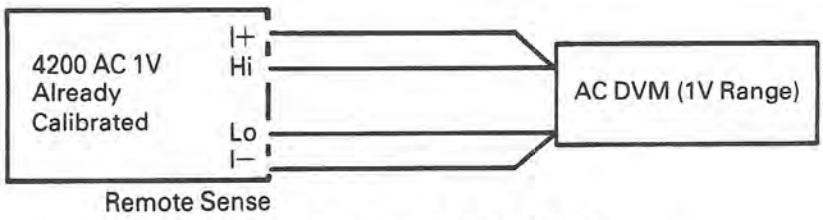
3. **Thermal Transfer Standard**
Adjust for null at the Calibration Current.

4. **DC Current Standard**
   a. Set OUTPUT OFF.
   b. Disconnect from the shunt.

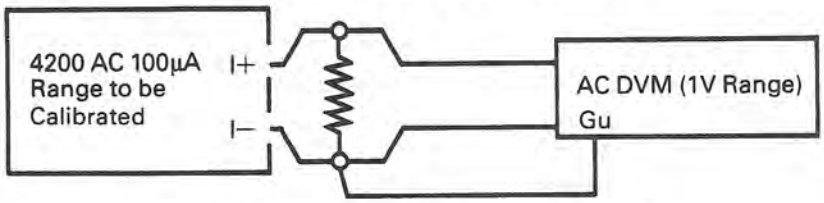
5. **4200**
   a. With OUTPUT OFF, connect the I+ and I– terminals across the Shunt.
   b. On I FUNCTION, select the required OUTPUT RANGE.
   c. Select the required FREQUENCY RANGE (or if a Spot Frequency is to be calibrated: Press SPOT and select F1 – F5).
   d. Use FREQUENCY ↑↓ keys to display the required Calibration Frequency.
   e. Use OUTPUT ↑↓ keys to display the required Calibration Current.
   (If at Nominal Full Range, press the Full Range key.)
   f. Set 4200 OUTPUT ON (and if NOT at Nominal Full Range, Select SET).
   g. Use the OUTPUT ↑↓ keys to adjust the OUTPUT Display reading to obtain a null on the Thermal Transfer.
   h. Execute the calibration by pressing the CAL key (and if calibrating a Spot Frequency, repress the SPOT key to deselect). Set OUTPUT OFF.

1.2.13 Current Full Range Calibration (100μA-1A)

(Alternative Method using verified 4200 1V Range, Calibrated Standard AC Shunts and AC DVM).



Standardization of DVM 1V Range



Calibration of 4200 Current Ranges

Calibrate the 4200 at or close to the calibration points in the table, selecting SET and/or SPOT as required, as part of the following procedure:

Note:

It is assumed that for a SPOT calibration, the 1V Range has already been Spot calibrated at the required calibration point.

Nominal Cal. Points for 100μA to 1A Ranges.

4200 OUTPUT RANGE/ FREQUENCY	4200 Nominal OUTPUT Current	Freq. Band set by 4200
100μA 300Hz	100.0000μA	LF
100μA 5kHz	100.0000μA	HF
1mA 300Hz	1.000000mA	LF
1mA 5kHz	1.000000mA	HF
10mA 300Hz	10.00000mA	LF
10mA 5kHz	10.00000mA	HF
100mA 300Hz	100.0000mA	LF
100mA 5kHz	100.0000mA	HF
1A 300Hz	1.000000A	LF
1A 5kHz	1.000000A	HF

1. **4200 and AC DVM**
   With OUTPUT OFF, connect the 4200 and DVM for Standardization.
   Select the 1V Range on the AC DVM.

2. **4200**

   a. Set to the 1V Range at the Calibration Frequency and adjust for calibrated 1.000000V output.

   b. Set OUTPUT ON and note the DVM reading as 'V1'.

   c. Set OUTPUT OFF, and reconnect the test circuit for Calibration, using the correct shunt for the range to be calibrated.

   d. On I FUNCTION, select the required OUTPUT RANGE.

   e. Select the required FREQUENCY RANGE (or if a Spot Frequency is to be calibrated: Press SPOT and select F1 - F5).

   f. Use FREQUENCY ↑↓ keys to display the required Calibration Frequency.

   g. Use OUTPUT ↑↓ keys to display the required Calibration Current.
   (If at Nominal Full Range, press the Full Range key).

   h. Set 4200 OUTPUT ON (and if NOT at Nominal Full Range, Select SET).

   j. Use the OUTPUT ↑↓ keys to adjust the OUTPUT Display reading to obtain a DVM reading of 'V1'.

   k. Execute the calibration by pressing the CAL key (and if calibrating a Spot Frequency, repress the SPOT key to deselect). Set OUTPUT OFF.

1.3 REMOTE CALIBRATION GUIDELINES

1.3.1 Introduction

The operation of the 4200 in systems applications, via the IEEE 488 interface, is described in Section 5 of the User's Handbook.

In addition to its capability as a programming calibrator, the 4200 can itself be calibrated under remote control. Full autocalibration of the instrument over the bus implies availability of programmable standards, a programmable thermal transfer standard and a suitably-programmed controller.

1.3.2 Calibration Commands

Table 1.2 lists the device-dependent calibration commands used in the 4200. The transfer of calibration facilities to remote control is illustrated in Fig. 1.2.

Note.

With the Calibration keyswitch set to ENABLE, the 'I' code (User's Aide-Memoire) accesses an alpha-numeric store for up to 16 ASCII characters.

Command Codes		AUTOCAL Mode	AC Voltage (AC)	AC Current (I)
CØ	CAL only	Gain calibration (at nominal FR)	ALL RANGES	ALL RANGES
C1 and CØ	SET and CAL	Gain for range at User's selected value	ALL RANGES	ALL RANGES
C2 and CØ	STD and GAIN CAL		1V and 10V Ranges only	—
C3 and CØ	PRECAL and GAIN CAL		10V Range	—
T1 to T5 and CØ	Spot Frequency 1 to Spot Frequency 5 and GAIN CAL		ALL RANGES	ALL RANGES
T1 to T5 and C1 and CØ	Spot Frequency 1 to Spot Frequency 5 and Gain for range at User's selected value		ALL RANGES	ALL RANGES
TØ	Cancel Spot Frequency		ALL RANGES	ALL RANGES
I	User's Message		See para. 1.3.2	

TABLE 1.2 AVAILABILITY OF COMMAND CODES

These commands can only be activated when two conditions have been fulfilled:

1. The CALIBRATION ENABLE keyswitch on the 4200 Rear Panel must be set to ENABLE.
2. The IEEE Interface command-code W1 must have been received and activated.

In addition the bus command C3 (PRECAL) can only be activated when the internal 'PRE-CAL ENABLE' switch is enabled.

When the 4200 is under remote control over the bus, the command code WØ overrides the settings of the CALIBRATION ENABLE and internal PRE-CAL ENABLE switches, disabling the 'C' codes.

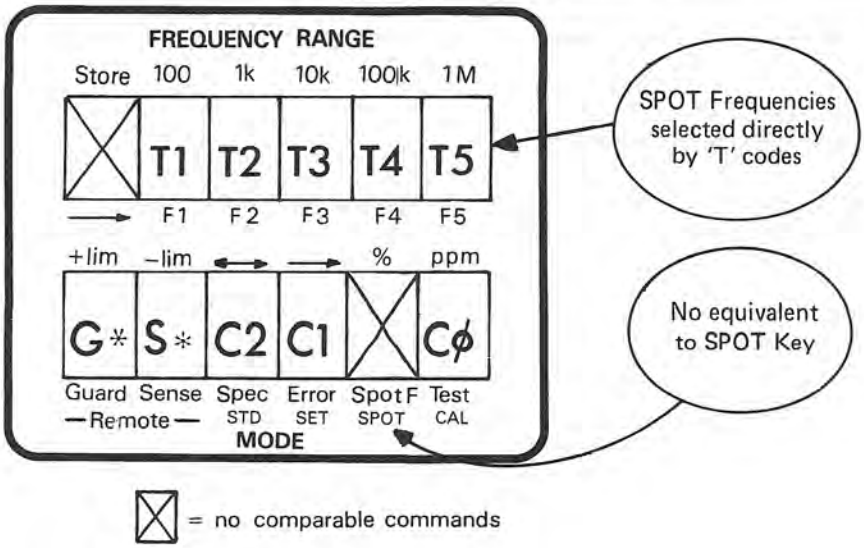


FIG. 1.2 TRANSFER OF CALIBRATION FACILITIES TO REMOTE CONTROL

1.3.2.1 General Procedure

The Main Register is set to the Calibration Standard value (M***...), the 4200 Output is switched ON (O1), and one or a specified sequence of the calibration mode command codes (C1, C2, C3, I, T1-T5) may be transmitted.

The 'M' Code is adjusted to obtain a null at the Calibration Standard value, and CØ is transmitted to execute the calibration.

1.3.2.2 Command Code Facilities

C1 (SET) C1 allows calibration to any value between 20% and 200% of nominal Full Range value (20% to 110% on 1000V range). If, for instance, an adjustable DC voltage standard is not available, C1 permits the 4200 to be calibrated against a Thermal Transfer standard whose reference is a buffered bank of Standard Cells.

C2 (STD) C2 allows a user to trim the value of the internal Master Reference voltage. The facility can be used to correct for any long-term drift, or to avoid a full recalibration of the 4200 when Laboratory References have been re-standardized.

C2 calibration effectively changes the gain of all voltage and current ranges in the same ratio, by a simple procedure available either on the 1V or 10V range.

T1-T5 (SPOT) The SPOT facility is not directly related to the manual SPOT key. The spot frequencies are directly accessible using 'T' codes, T1 to T5 corresponding to the F1 to F5 store keys, but in SPOT frequency mode. When a T code is received in calibration mode, the 4200 assumes that the spot frequency is to be changed, and so defaults frequency to 1kHz.

When a T code is used with SET; SPOT calibration can be carried out within 10% of full range value, but when used without SET, the 4200 assumes that the calibration is to be at Full Range.

After SPOT calibration, selecting Spot F at the calibrated value achieves the highest possible specification. For Recall procedures see the User's Handbook Section 4.

C3 (PRECAL) C3 is used to enable 'pre-calibration'. This is a procedure which is used at manufacture, and must also be used whenever all the calibration memories are cleared to zero (for example if the supply to the non-volatile RAM has been disrupted).

C3 accesses a special calibration memory, as part of a two-stage calibration on the 10V range. (Refer to para. 1.4.5).

CO CØ executes the programmed procedure which was previously selected by the C1; C2; T1 to T5; or C3 code. No calibration is complete until a CØ code has been received.

CAL only If CØ is sent without preselecting one of the other modes, the 4200 assumes that the selected range is to be calibrated at the exact Full Range, at either LF or HF or both.

1.3.3 Programming Guidelines

1.3.3.1 An Example

The following sequence suggests a method of calibrating the 4200 1V Range Gain against a standard cell value of +1.018057V.

It is assumed that the 4200 is correctly addressed, its Calibration Keyswitch set to ENABLE and that the 4200 Output is OFF.

It is also assumed that a Thermal Transfer has been nulled against the buffered standard cell, is now set to low sensitivity and connected between the 4200 Hi and Lo terminals as in Fig 1.1 (a) of Section 1.2.8.

		4200 Codes
a.	Command the 4200:	
	AC Volts	F1
	1V Range	R5
	Local Guard and Sense	GØ SØ
	Calibration Enable	W1
	Output Value to calibration point	M+1.018057
	Select 'SET' Calibration mode	C1
	Output ON	O1
b.	Establish null tolerance limits.	
c.	Command the Thermal Transfer: Recall Sensitivity Range and Reading; Increase Sensitivity Range and repeat recall until reading exceeds half-scale.	
d.	Calculate 4200 setting for null. Set 4200 output to calculated value.	M***...
e.	Repeat (c) and (d) until null is within limits.	
f.	Command the 4200 to execute 'CAL'	CØ.

The example suggests only the broad outline of one of many sequences which could be used to perform 4200 calibrations.

1.3.3.2 Calibration Command Strings

The following command strings are given for the sole purpose of illustrating the methodology designed into the 4200 for remote calibration modes. Some reference to external operations is inferred. The nulling operation is separated into its own string, as it is likely to be iterative.

It is assumed that the 4200 has previously been programmed in function and range (not autorange RØ) and that the external circuit is set up correctly. The 4200 is already programmed into its calibration mode by W1, with the calibration keyswitch set to ENABLE, and output OFF.

a. Nominal Full Range LF Gain Calibration:
H(LF) A1 O1=M (for null)=CØ=OØ=

b. Nominal Full Range HF Gain Calibration:
H(HF) A1 O1=M (for null)=CØ=OØ=

c. Combined Nominal LF and HF Gain Cal:
H(LF) A1 O1=M (for null)=C0=
H(HF)=M (for null)=C0=O0=

d. Non-nominal LF Gain Calibration:
H(LF) M(20%–200% FR) C1=
O1=M(for null)=CØ=OØ=

e. Non-nominal HF Gain Calibration:
H(HF) M(20%–200% FR) C1=
O1=M (for null)=C0=O0=

f. Combined Non-nominal LF and HF Gain Cal:
H(LF) M(20%–200% FR) C1=
O1=M(for null)=CØ=
H(HF) M(20%–200% FR) C1=
M(for null)=CØ=OØ=

g. SPOT Calibration at Nominal Full Range:
T(1 to 5) H(required spot frequency)
A1 O1=M(for null)=CØ=OØ=

h. SPOT Calibration at a value within ± 10% of Full Range:
T(1 to 5) H(required spot frequency)
M(± 10% FR) C1=O1=M(for null)=CØ= OØ=

j. Standardization at Nominal Full Range (1V or 10V Range only):
H(LF) A1 C2 O1=M(for null)=CØ=OØ=

k. Standardization at a Non-nominal value (1V or 10V range only):
H(LF) M(20%–200% FR) C2=
O1=M(for null)=CØ=OØ=

The string for code C3 appears in para 1.4.5.2.

1.4 PRE-CALIBRATION

For all normal purposes, the routine procedures detailed in Section 1.2 (and repeated in the User's Handbook Section 8) are sufficient to maintain 4200 calibration.

In an initial internal calibration process at manufacture, certain 'PRE-CAL' parameters are established in a special calibration memory to define the overall linearity of the 4200, and to allow maximum routine calibration memory span for adjustments. Thereafter all routine calibrations may be performed from the front panel or over the IEEE Interface without removing the covers.

The stored parameters are invalidated by replacement of certain critical parts of the instrument; detailed below.

After replacement of any of these parts, new parameters must be stored in the PRE-CAL memory, by procedures (in manual or remote control) detailed in this section.

NB. Removal of the upper or lower Guard/Ground shields invalidates any previous calibration by the Datron Factory or Service Centre.

Critical Parts

1. The Lithium battery which powers the whole calibration memory when the instrument supply is switched off. This should be replaced at five-year intervals.
   (Refer to Section 5.3).

The following parts are normally replaced only on failure. A full list appears in Section 1.1 Table 1.1.

2. The Digital Assembly
3. The Reference Divider Assembly
4. Critical components in the Digital or Reference Divider, AC and Sine Source assemblies

Pre-Calibration must be followed by a full Routine Calibration of the whole instrument (Section 1.2).

1.4.1 Validity

The adjustments detailed in the following sequences include intentionally clearing the instrument's calibration memory, which loses all previous calibration information.

Therefore before proceeding make certain that the reasons for carrying out a complete recalibration are valid. (If in any doubt, consult your Datron Service Center).

1.4.2 Calibration Standards Equipment Required

1. A precision voltmeter capable of 1V AC measurement with a stability between readings of better than ± 5ppm.
   Example: Datron Instruments 1081
2. An inductive voltage divider with ratios of x1.0 and x0.1 capable of dividing 10.000,00V to 1.000,000V to an accuracy better than ± 1ppm.

1.4.3 Preparation

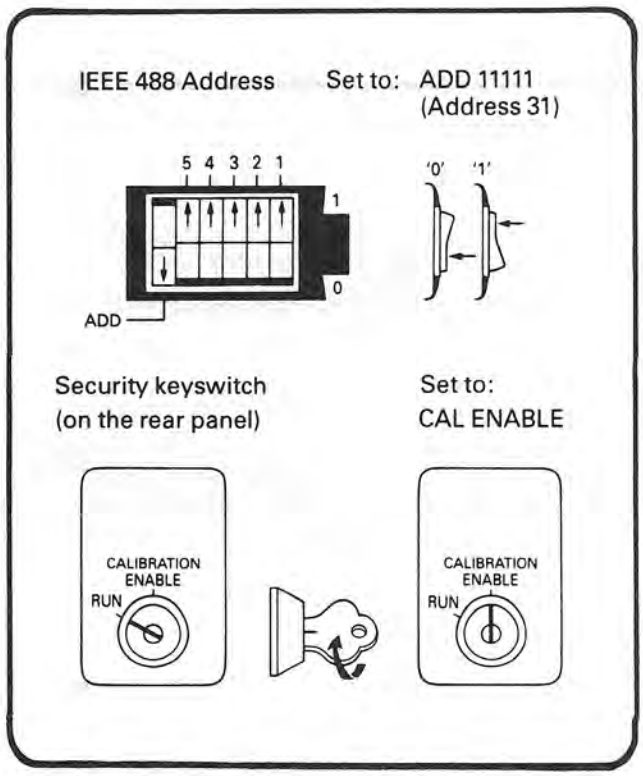
1.4.3.1 Manual Calibration Mode

Before any calibration is carried out, prepare the 4200 as follows:

a. Turn on the instrument to be checked and allow a minimum of 4 hours to warm-up in the specified environment.

b. IEEE 488 Address switch:
   Set to ADD 11111 as shown (Address 31).

c. CALIBRATION ENABLE key switch:
   Insert Calibration Key, and turn to ENABLE.



1.4.3.2 Interconnections

a. Ensure the 4200 OUTPUT OFF LED is lit.
Cancel any MODE keys.
Select Remote Sense.
Deselect Remote Guard.
Select the 1kHz Frequence Range.

b. Select ACV FUNCTION and connect the IVD to the 4200 terminals as shown. Use short leads.

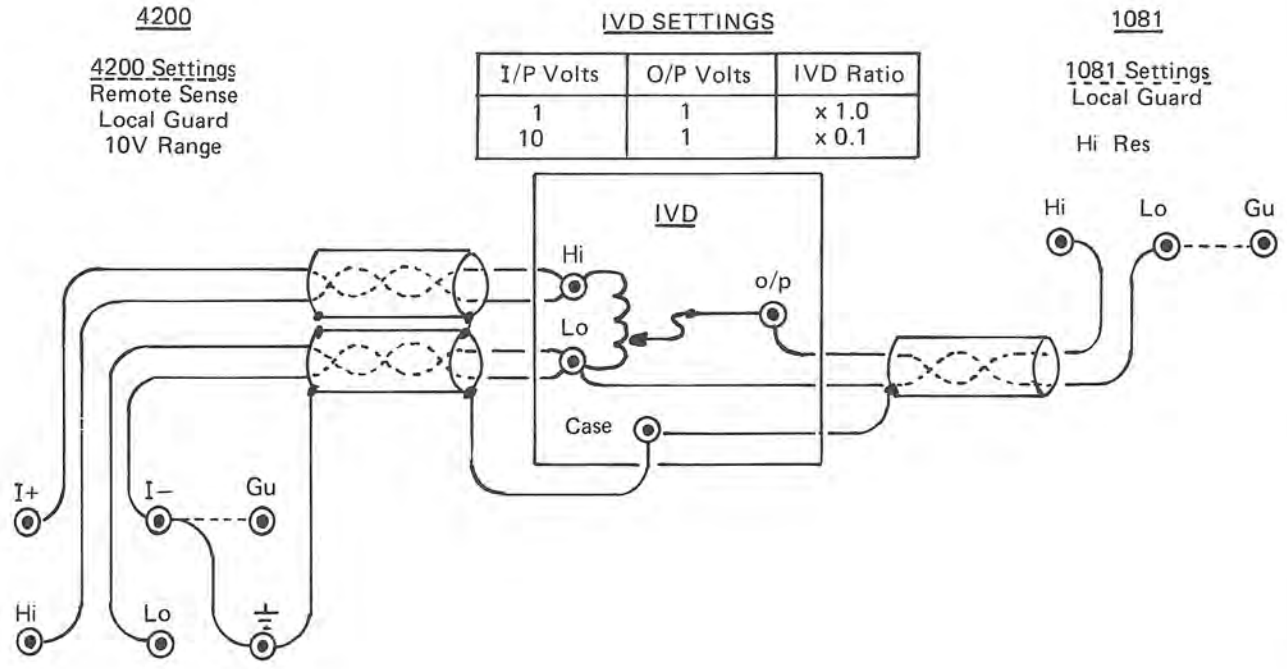


FIG. 1.3

1.4.3.3 Identification of Access Holes
(Fig. 1.4)

These give access to the 'PRE-CAL ENABLE' switch and the 'CLEAR CALIBRATION MEMORY' switch.

DO NOT OPERATE EITHER SWITCH YET!

Operation of these switches in included in the procedure of Section 1.4.4.

a. Release 6 screws retaining the top cover.

b. Lift the top cover at the front of the instrument and locate the two holes which give access to the two-position 'PRE-CAL ENABLE' switch and the press-button 'CLEAR CALIBRATION MEMORY' switch.

c. Replace the top cover, do not secure.

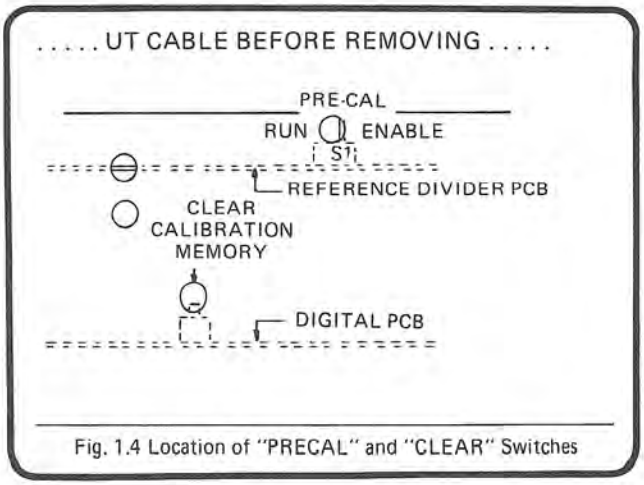


Fig. 1.4 Location of "PRECAL" and "CLEAR" Switches

1.4.4.1 'PRE-CAL ENABLE' and 'CALIBRATION MEMORY CLEAR' Switches

a. Cover
Lift the top cover at the front.

b. ENABLE
Locate the hole which gives access to the PRE-CAL ENABLE switch.

Insert an insulated tool in the hole and move the pre-cal switch to the right (Enable).

The legend 'cal', as presented on the MODE display, also appears on the OUTPUT display.

Caution! The following operation (c) clears all the calibration memory stores as part of pre-calibration. Proceed only if this is required.

c. CLEAR
Locate the hole which gives access to the Calibration Memory CLEAR push-button.

Insert an insulated tool in the hole and press the button to clear the calibration memory.
Refit the top cover but do not secure.

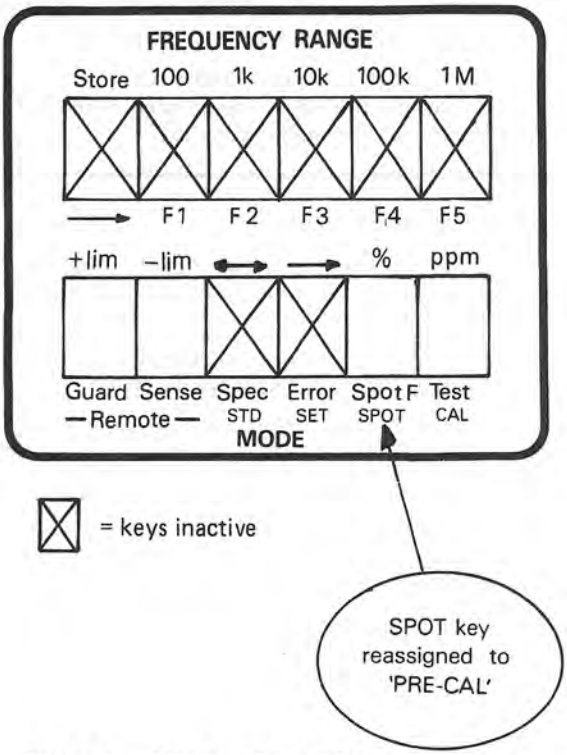


FIG. 1.5 PRECALIBRATION – USE OF MANUAL KEYS

1.4.4.2 Setting the Pre-cal Parameters

a. IVD
Select x1.0 ratio.

b. 4200
Select 10V range, at 1kHz on the 1kHz Frequency range.
Select 1.000,00V.
Press the SPOT key, its LED lights.
Use 4200 OUTPUT ↑|↓ keys to adjust the DVM reading to 1V.
Press CAL: the SPOT LED remains lit.

c. IVD
Select the x0.1 ratio to divide the 4200 output by 10.

d. 4200
Select Full Range.
Use 4200 OUTPUT ↑|↓ keys to adjust the DVM reading to 1V.
Press the CAL key; the SPOT LED goes OFF and display reverts to nominal 10V. Pre-cal is now completed.

Select OUTPUT OFF and disconnect.

1.4.4.3 4200 PRE-CAL ENABLE Switch

CAUTION! **DO NOT** press the internal push-button which clears the calibration memory. If this is done, any parameters stored in the calibration memory are cleared; so pre-calibration in cancelled, and must be repeated.

a. Cover
Lift the top cover at the front.

b. Locate
Locate the hole which gives access to the PRE-CAL ENABLE switch.

c. Disable
Insert an insulated tool in the hole Pre-cal and move the switch to the left (RUN).

d. Display
The legend 'cal' remains on the MODE display, but disappears from the OUTPUT display.

e. Cover
Refit and secure the top cover.

1.4.5 Remote Pre-Calibration Guidelines

The operation of the 4200 for remote calibration via the IEEE 488 interface, is described in Section 1.3.

Table 1.2 lists the device-dependent calibration commands used in the 4200. The transfer of Pre-calibration to remote control is illustrated in Fig. 1.6.

1.4.5.1 General Procedure

The general procedure follows that for remote Routine Calibration; the external circuit is connected as for manual pre-calibration.

The bus command C3 (PRECAL) can be activated only after three conditions have been fulfilled:

1. The CALIBRATION ENABLE Keyswitch on the 4200 Rear Panel must be set to ENABLE,
2. The IEEE Interface command-code W1 must have been received and activated.
3. The internal 'PRE-CAL ENABLE' switch is set to ENABLE.

When the 4200 is under remote control over the bus, the command code WØ overrides the settings of the CALIBRATION ENABLE and internal PRE-CAL ENABLE switches, disabling the 'C' codes.

In the case of C3 preselection, the procedure is in two stages, so a first transmission of CØ merely transfers to the second stage. The second CØ transmission cancels the preselected mode.

For C3, the CPU uses the value input by 'M' Code to distinguish between Full Range or 10% of Full Range gain calibration.

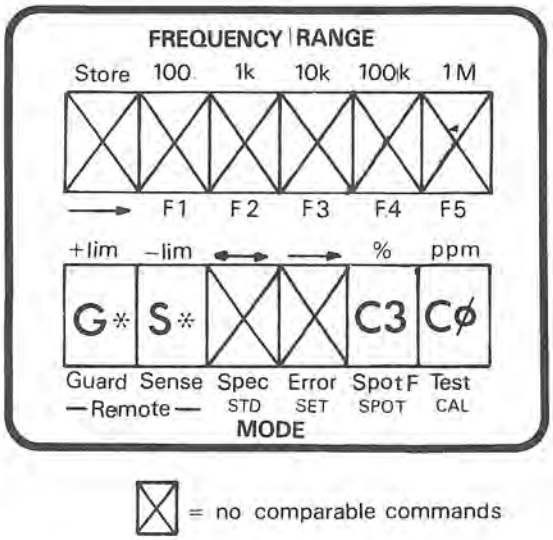


FIG. 1.6 TRANSFER OF PRECALIBRATION TO REMOTE CONTROL

1.4.5.2 Pre-Calibration Command Strings

The following six command strings are given for the sole purpose of illustrating the methodology for the remote pre-calibration mode. Some reference to external operations is inferred. The nulling operation is separated into its own string, as it is likely to be iterative.

It is assumed that the 4200 has previously been programmed into the 10V range at a frequency in the LF band (refer to the User's Handbook Section 8, Page 8-2), and that the external circuit is set up correctly.

The 4200 has already been programmed into its calibration mode by W1, with the calibration keyswitch and the internal PRE-CAL ENABLE switch set to ENABLE.

The calibration memory stores have been cleared, and the 4200 Output is OFF.

The string sequence for pre-calibration is as follows:

H	(LF)
C3	(automatically sets nominal Full Range)
O1	(Output On)
=	
M***	(adjust for null at Full Range)
=	
CØ	(executes the first-stage calibration)
=	
M***	(adjust for null at 10% Full Range)
=	
CØ	(executes the second-stage calibration)
=	
OØ	(Output Off)
=	

The precalibration should be terminated as detailed in para 1.4.4.3.

SECTION 2

FAULT DIAGNOSIS

WARNING **HAZARDOUS ELECTRICAL POTENTIALS ARE EXPOSED WHEN THE INSTRUMENT COVERS ARE REMOVED.**
ELECTRIC SHOCK CAN KILL

CAUTION The instrument warranty can be invalidated if damage is caused by unauthorised repairs or modifications. Check the warranty detailed in the "Terms and Conditions of Sale". It appears on the invoice for your instrument.

2.1 INTRODUCTION

2.1.1 Use of Diagnostic Guides

The diagnostic guides given in Section 2.2 are intended to aid the user in locating a failed printed circuit board or other assembly. The self-diagnostic capabilities of the 4200 provide the first step in fault analysis by displaying a FAIL message on the mode display. Initial actions to be taken after the occurrence of a FAIL message are given, where applicable, in the diagnostic guides of Section 2.2. The FAIL message localizes the failure into a distinct functional area and the "Fault Condition" summary in each guide relates the function failure to a probable hardware boundary.

The identities of the assemblies involved in the failure are given beneath the fault condition summary, but it is unlikely that all assemblies listed will prove to be faulty. For successful failure analysis, it is advisable to be familiar with the electronic functioning of the instrument and with the physical location of the assemblies. To assist in these aspects, the diagnostic guides include references to relevant parts of this publication.

2.1.2 Effects of Protective Measures on Diagnosis

2.1.2.1 Protective Suppression of Fault Conditions

The 4200 incorporates built-in protection in hardware and software. To minimize damage, protective circuitry acts immediately, backed up by a pre-programmed CPU response to detected failure symptoms. The CPU informs the user by presenting a failure message on the MODE display.

When investigating a failure, it should therefore be anticipated that protective measures will have suppressed the original fault conditions. A useful starting-point is to identify the origin of the failure message to localize the area of search.

2.1.2.2 FAIL 5 as Default State

Faults which result in display messages FAIL 2, 3 or 4 can pose a safety hazard to the operator, and apply excessive voltage to external circuitry. To protect against this, the instrument is programmed to default to FAIL 5 state as rapidly as possible after its initial response to the failure symptoms. The CPU switches Output OFF and trips the safety monitor (Watchdog). If the conditions of the original failure message have been removed the display changes to FAIL 5.

In normal use, an operator will probably notice only FAIL 5, and miss the original failure message. In FAIL 5 state, front panel control is inhibited until Safety Reset is pressed. This returns the instrument to the state for which the original fault conditions and failure message were produced, but with Output OFF.

2.1.2.3 To Observe the Original Failure Message

Two procedures can be used:

(a) Carry out the self-test routine of Section 2.3. The failure message may recur during this test.

(b) Reset the instrument to reproduce the fault, carefully watching the MODE display. The original failure message should reappear momentarily, prior to defaulting into FAIL 5.

Then select the appropriate diagnostic guide in Section 2.2.

2.2.1 FAIL 1 Display Message

DISPLAY: FAIL 1

Excessive Internal Temperature

INITIAL ACTION

1. Switch Power OFF.
2. Allow to cool for 15 minutes.
3. Switch Power ON—If FAIL 1 persists, repeat 1 & 2.
4. Select operating mode when FAIL 1 clears.
5. No failure display—no further action.
   FAIL 1 recurs —fault persists.

FAULT CONDITION

High temperature sensed in:

1. Positive Heatsink Assembly

   or

2. Negative Heatsink Assembly

Fault indication signal OVERTEMP active.

POSSIBLE FAULT LOCATION

1.	Positive Heatsink Assembly	400538
2.	Negative Heatsink Assembly	400539
3.	Power Amplifier Assembly	400450

FURTHER INFORMATION IN THIS HANDBOOK

Page numbers: 7.13, 7.9.
Technical descriptions: Section 4.12

2.2.2 FAIL 2 Display Message

DISPLAY: FAIL 2

Over-Voltage

INITIAL ACTION

N.B. This failure can be caused by injection of an external voltage across the 4200 terminals. The trip level is between 75V and 110V RMS.

1. Ensure that OUTPUT IS OFF (4200 should have tripped to FAIL 5).
2. Disconnect external leads from 4200 terminals.
3. Press Safety Reset.
4. Carry out self-test sequence.
5. FAIL 2 recurs—fault persists.
6. No failure display—Reproduce original conditions in Local Sense with no external connections.
7. No failure display—check external circuit and proceed with careful use.
8. FAIL 2 recurs—fault persists.

FAULT CONDITION

1. Over voltage circuit on the Output Control Assembly has detected the excess voltage at between 75V and 110V RMS between PHi and PLo lines, and has activated $\overline{\text{HV ST}}$ signal to the CPU AND
2. The CPU has recognized that the instrument is not in High Voltage State, so has generated FAIL 2 display. THEN
3. The CPU has switched Output OFF, tripped the watchdog and generated FAIL 5 display.

POSSIBLE FAULT LOCATION

1.	Injection of external voltage	
2.	Output Control Assembly	400550
3.	Power Amplifier Assembly	400450

FURTHER INFORMATION IN THIS HANDBOOK

Page numbers: 7.5, 7.9.
Self-test procedure: Section 2.3.
Technical descriptions: Section 4.12.

2.2.3 FAIL 3 Display Message

DISPLAY: FAIL 3

Control Data Corrupted.

INITIAL ACTION

No immediate action required.

FAULT CONDITION

1. Control data corrupted.
2. CPU has detected errors in serial transfer of data between out-guard and in-guard circuits, and generated FAIL 3 display. THEN
3. The CPU has switched Output OFF, tripped the watchdog and generated FAIL 5 display.

POSSIBLE FAULT LOCATION

1.	Reference Divider Assembly	400535
2.	Analog Interface Assembly	400570

FURTHER INFORMATION IN THIS HANDBOOK

Page numbers: 7.4, 7.3.

Technical descriptions: Section 4.5.

2.2.4 FAIL 4 Display Message

DISPLAY: FAIL 4

Precision Divider Fault.

INITIAL ACTION

No immediate action required.

FAULT CONDITION

1. Precision divider fault.
2. CPU has detected errors in the most-significant data bits set in the precision divider input data latches, and generated FAIL 4 display. THEN
3. The CPU has switched Output OFF, tripped the watchdog and generated FAIL 5 display.

POSSIBLE FAULT LOCATION

Analog Interface Assembly	400570

FURTHER INFORMATION IN THIS HANDBOOK

Page number: 7.3.

Technical description: Section 4.6.

2.2.5 FAIL 5 Display Message

DISPLAY: FAIL 5

Safety Monitor (Watchdog) Tripped.

INITIAL ACTION

Use the checking sequence below, watching the MODE display carefully at each stage to detect any FAIL number appearing momentarily before FAIL 5. If no failure message occurs, carry on to the next stage.

Stage 1: Press Safety Reset.

Stage 2: Carry out self-test sequence (Section 2.3).

Stage 3: Set Output ON.

Stage 4: Proceed with careful use.

If FAIL 2 occurs at stage 3, ensure that it is not due to injection of an excessive external voltage by disconnecting the 4200 terminals and repeating the checks. If FAIL 5 alone occurs, proceed to "Fault Condition" below. For any FAIL other than FAIL 5, transfer to the diagnostic guide for that message.

FAULT CONDITION

18mS monostable (M10 in reference divider) has been deprived of at least two trigger pulses and has timed out, activating "BARK" and "BARK DELAYED" (BARK+47mS) signals from M13 in the reference divider pcb.

Summary of "BARK" effects:

1. Removes the drive from the High Voltage (1kV) transformer.
2. $\overline{\text{BARK DELAYED}}$ Disables the 400V Power Supply.
3. Status message sent to CPU signalling a failure.
4. CPU starts controlled shut-down.

Summary of "BARK DELAYED" effects:

1. Disconnects the AC voltage Power and Sense circuits from the instrument output terminals.
2. Disables the registers of the serial/parallel data converters.
3. Outputs from control latches in the reference divider pcb are disabled by setting into "Tristate". Each output line has a pull-up or pull-down resistor which sets the analog circuitry into a safe condition.

POSSIBLE FAULT LOCATION

1. Digital Assembly (No gated WRT STRB pulses at J2/J3-29) 400534
2. Analog Interface Assembly (No SSDA strobe pulses; or Watchdog disabled) 400570
3. Reference Divider Assembly (Incorrect functioning of Watchdog setup circuitry) 400535

N.B. The Watchdog is designed primarily to ensure that CPU malfunctions do not set up dangerous conditions in the analogy circuitry.

FURTHER INFORMATION IN THIS HANDBOOK

Page number: 7.2, 7.3, 7.4.

Technical description: Section 4.5.

2.2.6 FAIL 6 Display Message

DISPLAY: FAIL 6

Calibration Memory Fault.

INITIAL ACTION

1. Select Output OFF, Spec OFF, Error OFF.
2. Perform self-test sequence (Section 2.3).
3. No failure display—no further action.
4. FAIL 6 recurs—recalibration required.
5. Select Cal
6. Recalibrate

   } Refer to Section 1.
7. Calibration failure—fault persists.

FAULT CONDITION

Calibration memory fault on Digital pcb assembly.

POSSIBLE FAULT LOCATION

Digital Assembly	400534

FURTHER INFORMATION IN THIS HANDBOOK

Page numbers: 7.2.

Self-test procedures: Section 2.3.

Calibration procedures: Section 1.

Technical descriptions: Section 4.2.

2.2.7 FAIL 7 Display Message

DISPLAY: FAIL 7

P.A. 400V Power Failure

INITIAL ACTION

1. Switch Power OFF.
2. Check line supply is correct for input voltage setting.
3. Switch power ON—no failure display—no further action.
4. FAIL 7 recurs—fault persists.

FAULT CONDITION

1. Positive or Negative 400V power supply failure.
2. Fault indication signal 400V(2) FAIL active.
3. Check line input voltage.
4. It is possible for a misleading FAIL 7 message to occur, caused by a logic supply failure in particular −15 Volts. Refer for fault location and further information to FAIL 9.

POSSIBLE FAULT LOCATIONS

1.	Power Amplifier Assembly	400450
2.	Reference Divider Assembly	400535
3.	Positive Heatsink Assembly	400538
4.	Negative Heatsink Assembly	400539
5.	Power Supply/I Heatsink Assembly	400540
6.	Mother Board	400532

FURTHER INFORMATION IN THIS HANDBOOK

Page number: 7.9, 7.4, 7.13, 7.16.

Technical descriptions: Sections 4.12 and 4.16.

2.2.8 FAIL 8 Display Message

DISPLAY: FAIL 8

P.A. 38V Power Failure.

INITIAL ACTION

1. Switch power OFF.
2. Check line supply is correct for input voltage setting.
3. Switch power on—no failure display—no further action.
4. FAIL 8 recurs—fault persists.

FAULT CONDITION

1. Positive or Negative 38V power supply failure.
2. Fault indication signal 38V(2) FAIL active.
3. Check line input voltage.
4. It is possible for a misleading FAIL 8 message to occur, caused by a logic supply failure, in particular −15 Volts. Refer to fault location and further information to FAIL 9.

POSSIBLE FAULT LOCATIONS

1.	Power Amplifier Assembly	400450
2.	Reference Divider Assembly	400535
3.	Power Supplies	400544
4.	Mother Board	400532

FURTHER INFORMATION IN THIS HANDBOOK

Page number: 7.9, 7.4, 7.12, 7.16.
Technical descriptions: Section 4.16.

2.2.9 FAIL 9 Display Message

DISPLAY: FAIL

P.A. 15V Power Failure

INITIAL ACTION

1. Switch power OFF.
2. Check line supply is correct for input voltage setting.
3. Switch power on—no failure display—no further action.
4. FAIL 9 recurs—fault persists.

FAULT CONDITION

1. Positive or Negative 15V power supply failure.
2. Fault indication signal 15V(2) FAIL active.
3. Also 400V power supply is disabled.
4. Check line input voltage.

POSSIBLE FAULT LOCATIONS

1.	Power Amplifier Assembly	400450
2.	Reference Divider Assembly	400535
3.	Power Supplies	400554

FURTHER INFORMATION IN THIS HANBOOK

Page number: 7.9, 7.4, 7.11.
Technical descriptions: Section 4.16.

2.2.10 Error OL Display Message

DISPLAY: ERROR OL

AC Volts: Output current limit exceeded.

Current: Output compliance voltage limit exceeded.

INITIAL ACTION

1. If AC Voltage range selected:
   (a) Set Output OFF (automatic if 100 or 1000V range selected).
   (b) Disconnect external circuit.
   (c) Set Output ON:
   — If no Error OL or FAIL message, check external circuit for low resistance, drawing output current in excess of specification (Table 2.1). Ensure Capacitive Load constraints are not exceeded, refer to User's Handbook Section 6 page 6.5.
   — If Error OL recurs, internal fault persists.
2. If I range selected:
   (a) Set Output OFF.
   (b) Short Output terminals I+ to I−.
   (c) Set Output ON:
   — If no Error OL or FAIL message, check external circuit for high resistance, developing output voltage in excess of 3V compliance limit.
   — If Error OL recurs, internal fault persists.

OUTPUT CURRENT LIMIT	OUTPUT RANGE	FREQUENCY RANGE
25mA	1V	All Ranges
60mA	10V	All Ranges
120mA	100V	All Ranges
15mA	1kV	100Hz/1kHz
65mA	1kV	10kHz/100kHz/1MHz

FAULT CONDITION

1. If 1mV, 10mV, 100mV or IV range:
   Sine Source Assembly overcurrent sense circuit (M49a/M49b) has detected a current in the AC 1V line of approximately 25mA RMS or more, and has activated $\overline{\text{LIM ST}}$ signal to the CPU.
2. If 10V range:
   10V overload detector in the Power Amplifier Assembly has detected a current in the I+ line of approximately 60mA RMS or more. In this condition a hardware limit comes into effect.
3. If High Voltage ranges (100V or 1kV):
   Either
   (a) 100V Overload detector in the Power Amplifier Assembly has detected a load in excess of 120mA RMS on the 400V power supply,
   (b) 1kV Current Overload detector (M8) in the Output Control assembly has detected an excessive output current,
   or
   (c) 1kV Overvoltage Detector in the Output Control Assembly has detected a voltage on the PHI(V) line in excess of 1440V RMS.
   In these ranges the output is switched off automatically by the CPU.
4. If I range selected:
   Overvoltage detector circuit has detected a terminal voltage of 3V RMS or more and has activated $\overline{\text{LIM ST}}$ signal to the CPU. If 100mA or 1A range selected, the CPU switches Output OFF.

POSSIBLE FAULT LOCATIONS

1. External circuit
2. Sine Source Assembly 400446
3. AC Assembly 400447
4. Output Control Assembly 400550
5. Power Amplifier Assembly 400450
6. IAssembly 400555

FURTHER INFORMATION IN THIS HANDBOOK

Page numbers: 7.6, 7.7, 7.5, 7.9, 7.8.

Technical descriptions:

Low AC Voltage ranges: Section 4.11.

100 or 1000V ranges: Section 4.12.

I ranges: Section 4.15.

2.3 SELF-TEST SEQUENCE

2.3.1 General

The self-test sequence is performed in two stages:

Stage 1 is a fully automated test of safety monitoring and high-voltage safety interlocks;

Stage 2 is a semi-automatic test of keyboard and display functions, which also responds to operator's key selections.

2.3.2 Stage 1 (Fig. 2.1)

Entry into Stage 1 is selected automatically whenever the TEST key is pressed for the first time (the test is not allowed if OUTPUT ON, ERROR or SPEC are selected or when in remote control).

Indication of test mode is given by the LED in the TEST key being lit. The full sequence of Stage 1 must be completed before exit from the test mode can be made. The tests performed in Stage 1 are as follows:

1. Safety Monitor Watchdog Test. In this, the safety monitor is tripped causing the word SAFEtY to appear in the Mode display, the Safety Reset LED flashes and the buzzer sounds continuously. It is necessary for the operator to reset the safety monitor by pressing the Safety Reset key, after which the SAFEtY display is replaced by the 'running' message, and the test sequence continues.
2. Calibration Memory Test. The contents of the non-volatile calibration RAM are checked for validity. Failure results in the message FAIL 6 appearing on the Mode display.
3. High-voltage Protection. This test ensures that a voltage demand made to the power amplifier does not trip the software voltage detector when immediately below the detector threshold level, but when raised to a level above the detector threshold the detector is tripped.

   Incorrect detect action is shown by the message FAIL 2 on the Mode display. No voltages appear at the output terminals during this test.

   Fail messages are updated as the test sequence progresses through the calibration memory and high-voltage tests.

   After completion of the high-voltage test, the test mode ends and the Test LED is cancelled. If faults were encountered the last FAIL message will remain on the display replacing the running message. Fault diagnosis can now be performed. If no faults are encountered during Stage 1, the message PASS is displayed. The calibrator can now be returned to normal operation, or Stage 2 of the self-test sequence can be selected.

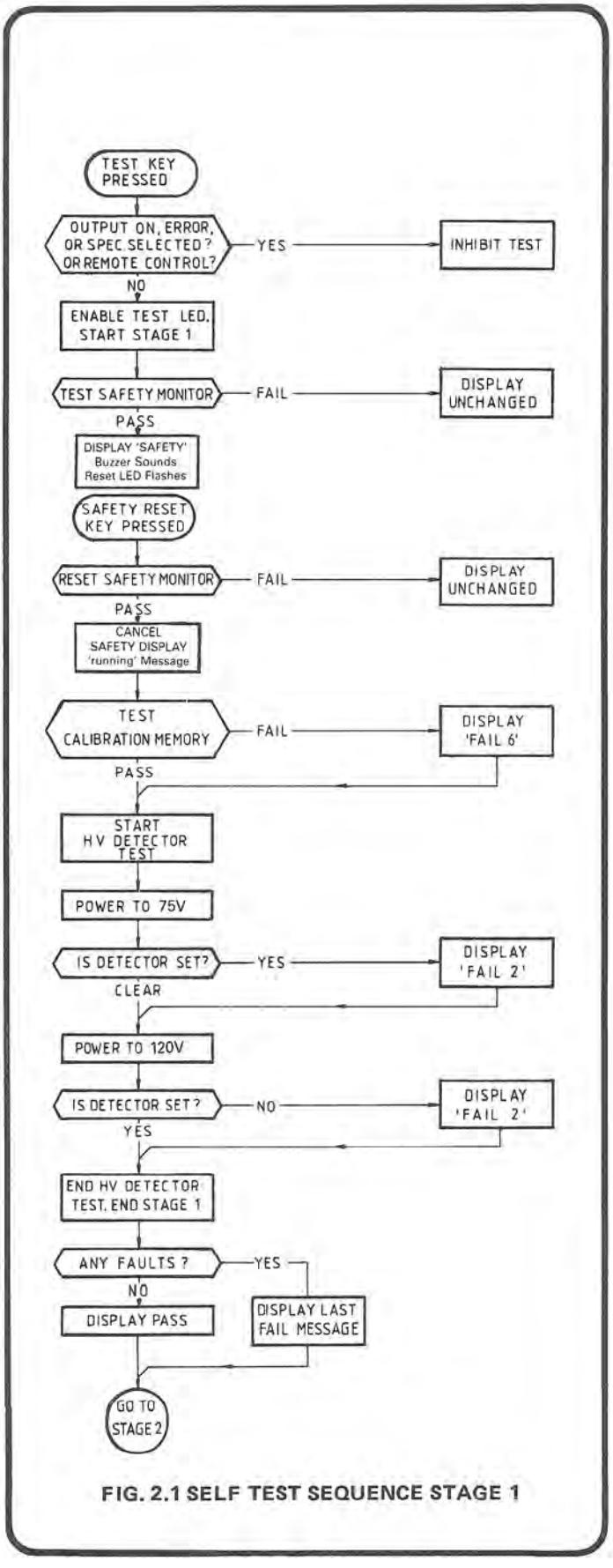


FIG. 2.1 SELF TEST SEQUENCE STAGE 1

2.3.3 Stage 2 (Fig. 2.2)

Entry into Stage 2 of the self-test sequence is made when the Test key is pressed AFTER the completion of Stage 1. The test proceeds by sequentially displaying all segments and legends.

The test continues, showing segment-by-segment, all seven-segment digits, legends and commas.

After all digits have been displayed, the keyboard LED indicators are lit in a sequence which proceeds from left to right. (Test LED remains lit).

The next test in the sequence requires operator participation in order to check key functions. Two half-digit symbols are shown on the mode display to indicate that the keys are ready to be checked.

Operation of Up, Down and Output Selection keys are shown by a symbol on the display immediately above the key; operation of Frequency Range, Mode, Range, Function and Output keys are shown by the key's LED. In these tests the display or LED remains lit until another key is pressed.

At any part of Stage 2, pressing Test or Zero key will end the test and cancel the Test LED.

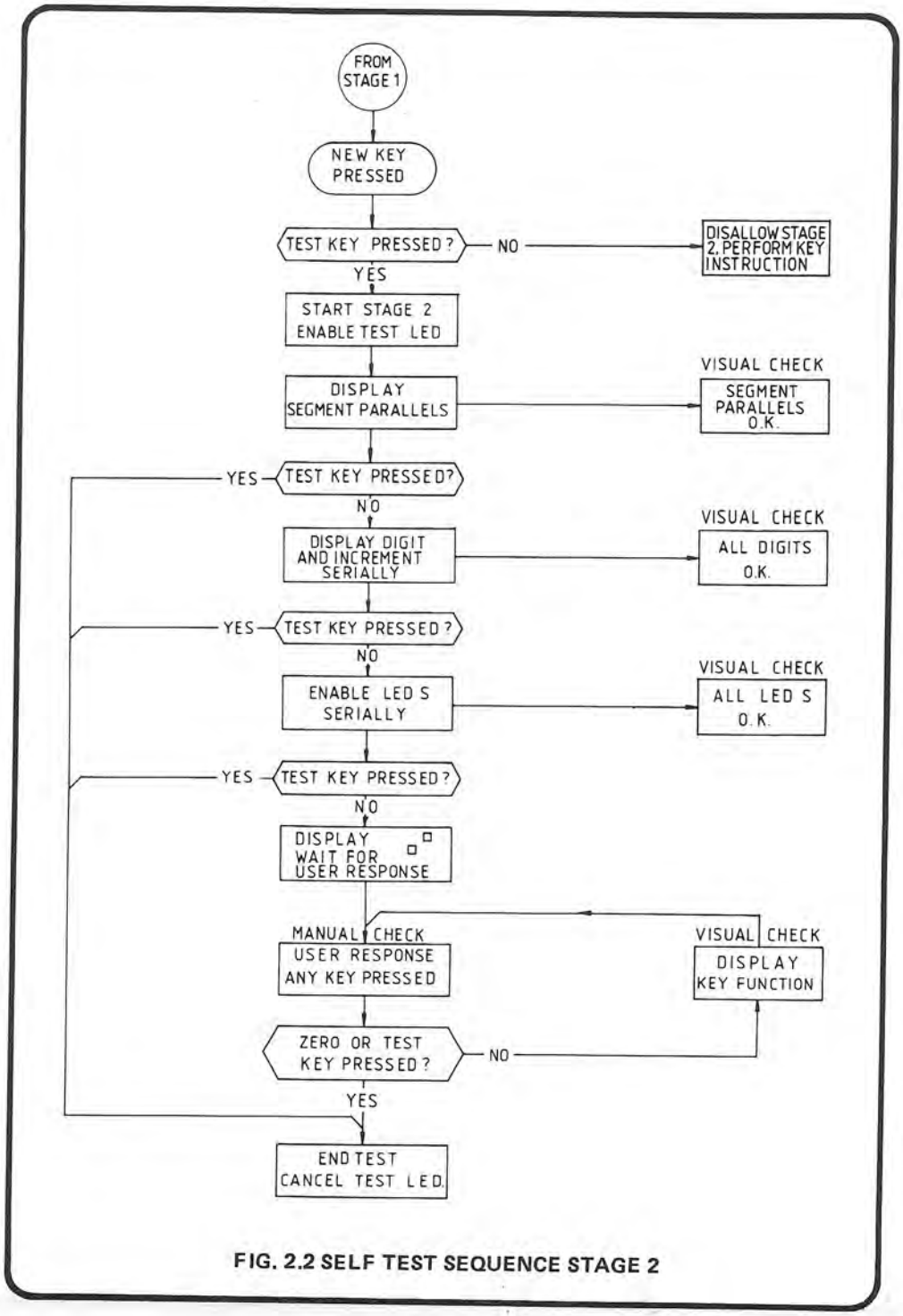


FIG. 2.2 SELF TEST SEQUENCE STAGE 2

2.4 Fuse Protection

In addition to the electronic protection devices used in the 4200, fuses are provided to protect against catastrophic component failure.

2.4.1 Fuse Replacement

A blown fuse is merely a symptom of failure, in the large majority of cases the cause lies elsewhere.

CAUTION Every occurrence of a blown fuse should be investigated to find the cause. Only when satisfied that the cause is known, and has been removed, should a user replace a fused link by a serviceable item.

2.4.2 Reasons For Fusing

The fuses in the 4200 fall into two groups:

i) Clip-in anti-surge fuses in the Power Supplies and Mother Board protect the power source from damage.

ii) Soldered-in fuses are used in some locations to ensure that the printed circuit tracks are protected in the unlikely event of extreme failure conditions.

Table 2.1 lists their locations.

2.4.3 Locating a Blown Fuse

The ultimate causes of blown fuses are so extensive that it is impractical to list them. In many cases the underlying cause, or the blown fuse itself, will activate an electronic protective process which can conceal some of the symptoms.

Fault location in the 4200 should proceed from the primary indications of fault condition (e.g. failure messages described in Section 2.2). These will lead to particular areas of investigation, and at this point the relevant circuit fuses should be checked first. Whether fuses are blown or not, the checks will add to the information available for further diagnosis. Table 2.1 is indexed in Assembly Circuit Diagram page order, giving fuse values. The types of fuses to be used can be found in the component lists of Section 6.

Location and Page numbers	Designator/Value	Protected Circuits	Clip-in	Solder-in
Power Input Module Page 7.18-6 (15)	F1 (3.15A for 220/240V) (6.25A for 100/120V)	(Power Input fuse)	*	
AC Assembly Page 7.7-1	F1 1A	1V range only and Current ranges up to 10mA		*
	F2 1A	All AC Voltage ranges		*
Mother Board Page 7.16-5	F1 1A	Transformer secondary to 400V PSU	*	
	F2 1A	Transformer secondary to 400V PSU	*	
	F3 2.5A	Transformer secondary to 38V PSU		*
	F4 2.5A	Transformer secondary to 38V PSU		*
Power Supply (38V) Page 7.12-1	F1 1A	—38V Supply Line		*
	F2 1A	+38V Supply Line		*
Output Control Page 7.5-1	F1 1A	Power Lo		*
	F2 1A	Power Lo		*
	F3 1A	PHI(V)		*
Power Supply (IG) Page 7.11-1	F1 4A	Supplies —22V(2)	*	
	F2 4A	Supplies +22V(2)	*	
	F3 3.15A	Supplies +15V(2)	*	
	F4 3.15A	Supplies —10V(2), —15V(2)	*	
Page 7.11-2	F5 1A	Supplies —8V(2)	*	
	F6 1A	Supplies +8V(2)	*	
Current Assembly Page 7.8-1	F5 375mA	All Current outputs		*
Power Supply (OG) Page 7.10-1	F1 4A	Digital and Display supplies	*	

Table 2.1 Fuse Location and Purpose

SECTION 3

DISMANTLING AND REASSEMBLY

3.1 GENERAL PRECAUTIONS

3.1.1 WARNINGS

(1) **ISOLATE THE INSTRUMENT FROM POWER SUPPLIES BEFORE DISMANTLING OR REASSEMBLING.**

(2) **THE COMBINED REMOVAL OF TOP AND BOTTOM COVERS, GROUND/GUARD ASSEMBLIES AND REAR PANEL ASSEMBLY; LEAVES THE MOULDED INTERNAL CHASSIS UNSUPPORTED. THIS CAN CONSTITUTE A SAFETY HAZARD TO BOTH PERSONNEL AND EQUIPMENT.**

3.1.2 CAUTIONS

(1) Removal of the Top Ground/Guard Assembly invalidates the manufacturers calibration certification.

(2) Handle the instrument carefully, especially when inverted, to avoid shaking printed circuit boards loose.

(3) Do not touch the pcb edge connectors with the hands.

(4) Ensure that no wires are trapped when fitting ground/guard assemblies.

(5) Ensure that washers, nuts etc. do not fall into the instrument, and are correctly refitted at subsequent reassembly.

3.2 General Mechanical Layout

The 4200 AUTOCAL STANDARD can be used as a benchtop instrument, or it may be rack mounted in a standard 19" rack. All circuits are housed within a single unit on printed circuit board assemblies, the eight major PCBs being plugged into a "Mother" PCB assembly.

A labelled view of the open instrument is shown in Volume 2 (page 7.0-1). Exploded views are shown on pages 7.18-1 to 7.18-6.

3.2.1 Front Panel

Six output terminals with captive, insulated caps are provided. Alternatively, the terminals can be fitted to the rear panel (Option 42) at manufacture.

A printed overlay on the front panel labels all the controls, and retains polarizing filters for the displays.

The Calibration Enable switch (with removable key), and the External Reset socket (J53) are mounted directly on the panel between the Power Input module and the cooling-air intake filter.

The intake filter is retained by a grille but is removable for cleaning. At the extreme left of the panel, an extractor fan draws cooling air through the filter and internal heat exchangers, discharging to atmosphere.

The IEEE 488 standard connector socket (J27) with instrument address switch, the Calibration Interval Switch and switch S53 (not used on the 4200); are all mounted on the Interconnection PCB assembly. This is fitted on spacers to the inside face of the panel with external components protruding to the rear.

3.2.2 Rear Panel

The recessed Power Input plug, Power Fuses and Line Voltage Selector are contained in an integral filter module at the centre of the rear panel.

3.3 LOCATION AND ACCESS

3.3.1 External Construction

Rigid side extrusions, together with the front and rear panel assemblies, form the basic chassis of the instrument. The side extrusions have handles and rear spacers fitted for bench-top use, or are fitted with 'ears' and slides for rack mounting (see User's Handbook, Section 2).

The top cover locates into the side extrusions and is secured by screws. The bottom cover is attached in the same way, and includes six domed feet. An operator's instruction card pulls forward from below.

3.3.2 Internal Construction

The chassis is enclosed top and bottom by ground and guard screens. The upper ground and guard screens allow most internal adjustments to be performed without removal. Locations of adjustable components, instructions and warnings are printed on its upper surface.

The interior of the chassis is divided into two compartments. A thermally-enclosed compartment occupies the forward half of the chassis, and is used to house the low power, precision printed circuit board assemblies.

The rear compartment contains high power components, is air-cooled and further subdivided. One section is positioned across the intake airflow, housing the In-guard and Out-guard Power Supply assemblies and providing anchorage for the Mains (Line) Transformer assembly. The other section houses three Heatsink assemblies, provides anchorage for the LF Transformer assembly, High Voltage assembly and 38V Power Supply assembly.

Filtered air passes over the power supplies, mixes with air in the rear copartment, is drawn through the heatsink assemblies, and is finally expelled from the instrument by the extractor fan.

Guard screens are provided against the outer walls of the power supply sub-compartment and the heat-sink compartment.

Interconnections between the Power Amplifier assembly, all forward-compartment assemblies, and the Front assembly are made via a Mother PCB. The latter fits across the bottom of the forward compartment, extending at the front to the Front assembly and at the rear to the 38V Power Supply. Four moulded stiffeners keep the mother pcb rigid, also providing lateral locating slots for printed circuit boards and guard screens.

The main printed circuit boards in the forward compartment fit across the full width of the instrument chassis. They slide into vertical slots cut into the moulded chassis, their PCB edge-connection fingers making electrical contacts with sockets mounted on the Mother Assembly. Interleaved between the assemblies are screening shields. These are also guided by slots, and make similar electrical contact.

The Power Amplifier assembly PCB slots in behind the forward compartment across the full width. It connects to the Mother PCB in the same way, but has additional discrete electrical connections for the high power lines.

Each PCB is identified by the color of its ejector lever. The color name is coded at the correct location on the top of the internal moulded chassis (refer to Table 3.1). Also, each assembly's edge connector is uniquely configured to prevent incorrect fitting.

The Front PCB assembly, carrying the display components, connects into the front end of the mother PCB outside the thermally-insulated compartment.

3.4 GENERAL ACCESS

ENSURE THAT POWER IS OFF.

Heed the Warnings and cautions 3.1.1 & 3.1.2.

If, during a procedure, sufficient access has been obtained then no further dismantling is required.

3.4.1 TOP COVER REMOVAL
(7.18-2 Details 11)

a. Remove the eight M4×12mm socket head countersunk screws from cover.
b. Remove cover by lifting at the front.

3.4.2 TOP COVER FITTING

Locate cover at rear first, then reverse procedure of para. 3.4.1.

3.4.3 BOTTOM COVER REMOVAL
(7.18-2 Detail 11)

a. Invert the instrument.
b. Remove the eight M4×12mm socket head countersunk screws from cover.
c. Remove cover by lifting at the front.

3.4.4 BOTTOM COVER FITTING

Locate cover at rear first, then reverse procedure of para. 3.4.3.

3.4.5 FRONT PANEL—REMOVAL
(7.18-4 Detail 6)

a. Remove the four M4×8mm taptite screws from the front panel.
d. Remove the Front Panel.

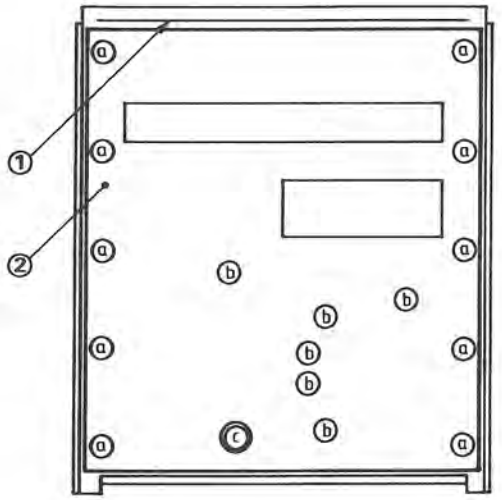
3.4.6 FRONT PANEL—FITTING

Reverse the procedure of para. 3.4.5, referring to Page 7.18-4.

TABLE 3.1 INTERNAL LOCATION AND ACCESS
(Top Cover and Top Ground/Guard assembly removed)

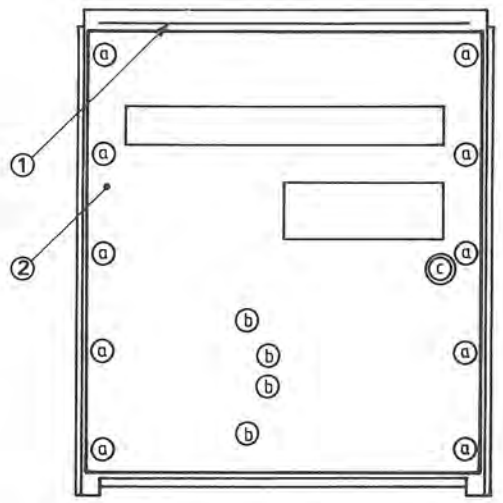
Note:
Unless removing the Instruction Card or the Rear Panel only; remove the Top Cover: Sub-section 3.4.1.
In addition to the following Location instructions, refer to Volume 2 page 7.0-1.

Assembly	Access Required (Heed Caution 3.1)	Location (Page Detail in bracket)	Ejector Color	Section	Page (Volume 2)
Instruction Card	—	7.18-2 (12) —	—	3.5.1	—
Front Assembly	3.4.3 & 3.4.5		—	3.5.2	7.1-1
Digital Analog Interface Reference Divider Output Control Sine Source AC Current (OR Current Link pcb)	3.4.7	Chassis Identifier Code BLK BRN RED ORG YEL GRN BLU BLU	BLACK BROWN RED ORANGE YELLOW GREEN BLUE BLUE	3.5.4	7.2-1 7.3-1 7.4-1 7.5-1 7.6-1 7.7-1 7.8-1
Common Guard and Ground Screens	3.4.7	7.18-5 (13) —	—	3.5.6	—
Power Amplifier	3.4.7	7.18-1 (4) VLT	VIOLET	3.5.8	7.9-1
Power Supplies Out-Guard In-Guard ± 38V	3.4.7	 7.18-1 (1) — 7.18-1 (2) — 7.18-1 (5) —	 — — —	 3.5.10 3.5.12 3.5.14	 7.10-1 7.11-1 7.12-1
Heatsinks	3.4.7	7.18-1 (4) —	—	3.5.16	7.13-1
High Voltage	3.4.7	7.18-1 (5) —		3.5.18	7.14-1
Transformers Mains HF LF	3.4.7	 7.18-5 (9) — 7.18-4 (6) — 7.18-5 (10) —	 — — —	 3.5.20 3.5.22 3.5.24	 — — —
Mother Board	—	7.18-3 (3) —	—	—	7.16-1
Interconnection Board	3.5.28	7.18-6 (15) —	—	—	7.17-2
Terminal Board	3.4.5	7.18-4 (8) —	—	3.5.26	7.17-3
Rear Panel	—	7.18-4 (6) —	—	3.5.28	7.18-6



1. FRONT PANEL ASSEMBLY
2. TOP GROUND/GUARD ASSEMBLY

FIG. 3.4.1 FITTING TOP GROUND/GUARD



1. FRONT PANEL ASSEMBLY
2. BOTTOM GROUND/GUARD ASSEMBLY

FIG. 3.4.2 FITTING BOTTOM GROUND/GUARD

3.4.7 TOP GROUND/GUARD ASSEMBLY REMOVAL
(Fig. 3.4.1)

CAUTION

Before proceeding it must be noted that removal of the Top ground/guard shield involves breaking Datrons calibration seal and renders manufacturers calibration invalid.

Access

Remove the top cover (para. 3.4.1).

a. Refer to Fig. 3.4.1 and remove:
   1. from position 'a', ten M4×8mm pozi-countersunk screws;
   2. from position 'b', six M3×6mm pozi-pan screws and M3 shakeproof washers;
   3. from position 'c', one M3×12mm pozi-pan screw and M3 shakeproof washer.

b. Remove the top ground/guard assembly.

3.4.8 TOP GROUND/GUARD ASSEMBLY FITTING

Reverse the procedure of para. 3.4.7.

3.4.9 BOTTOM GROUND SHEET ASSEMBLY—REMOVAL
(Fig. 3.4.2)

Access

Invert the instrument.
Remove the bottom cover (para 3.4.3).

a. Refer to Fig. 3.4.2 and remove:
   1. from positions 'a', ten M4×8mm pozi-countersunk screws;
   2. from positions 'b', four M3×6mm pozi-pan screws and M3 shakeproof washers;
   3. from position 'c', one M3×12mm pozi-pan screw and M3 shakeproof washer.

b. Remove the bottom ground sheet assembly.

3.4.10 BOTTOM GROUND SHEET ASSEMBLY—FITTING

Reverse the procedure of para. 3.4.9.

3.4.11 BOTTOM GUARD PLATE—REMOVAL
(Page 7.18-1 Detail 8)

Access

Invert the instrument.
Remove the bottom cover (para. 3.4.3).
Remove the bottom ground sheet assembly (para. 3.4.9).

a. Refer to Page 7.18-1 Detail 8 and remove nine M3×6mm pozi-countersunk screws.

b. Remove the bottom guard plate.

3.4.12 BOTTOM GUARD PLATE—FITTING

Reverse the procedure of para. 3.4.11 ensuring that no wiring is strained or trapped.

3.5 REMOVAL AND FITTING

3.5.1 INSTRUCTION CARD

a. Pull the instrument card forward to its fullest extent.

b. Bow the card and release the rear lugs from the slots.

c. Refit in reverse procedure.

3.5.2 FRONT ASSEMBLY—REMOVAL
(Page 7.18-3 Detail 4)

a. Remove two screws retaining the power switch, together with their two shakeproof washers and four plain washers.

b. Fold the power switch and its cable clear of the pcb.

c. Remove the M3×6mm pozi-pan screws from 13 positions on the circuit board.

d. Ease the lower edge of the PCB away from the Mother PCB, to disengage the mating connectors. Remove two M2.5×10mm pozi-pan screws and disconnect the power Switch (Page 7.18-3 Detail 4).

e. Remove the assembly.

3.5.3 FRONT ASSEMBLY—FITTING

Reverse the procedure of para. 3.5.2. Ensure all mating connectors are fully engaged and that the surfaces of displays are clean.

3.5.16 HEATSINK ASSEMBLIES—REMOVAL
(Page 7.18-5 Detail 12)

Heed the Warnings and Cautions 3.1.1 & 3.1.2.

a. Remove the six M3×12mm pozi-countersunk screws from the heatsink retaining plate.

b. Remove the heatsink retaining plate.

CAUTION
Allow heatsinks to cool before handling.
Do not pull on the connector wires.

Note:
Although the heatsink assemblies are discrete items, removal is simplified when performed in the following order:

1. Negative Heatsink assembly;
2. Positive Heatsink assembly;
3. Power Supply/Current Heatsink assembly.

When disconnecting connectors, some resistance to movement will be felt from the locking clips of the connector bases.

c. Disconnect connectors at the following points:
J1—Positive Heatsink assembly.
J2—Power Amplifier assembly.

d. Remove Negative Heatsink assembly.

e. Disconnect J3 at the Power Amplifier assembly.

f. Remove the Positive Heatsink assembly.

g. Disconnect at the following points:

Connector	Assembly
J1	Power Amplifier Assembly
J31, J19	Mother Assembly
J1	In-Guard PSU Assembly

h. Remove the Power Supply/Current Heatsink assembly.

3.5.17 HEATSINK ASSEMBLY—FITTING

Reverse procedure of para. 3.5.16.

To ensure correct location, orient the PCB side of each heatsink to face inwards.

3.5.18 HIGH VOLTAGE ASSEMBLY—REMOVAL
(Page 7.18-1 Detail 5)

a. Lift the assembly upwards as shown on Page 7.18-1 Detail 5.

b. Remove the connections J2, J3 and J4, shown in the diagram.

c. Lift the assembly clear of the instrument.

3.5.19 HIGH VOLTAGE ASSEMBLY—FITTING

Reverse the procedure of para. 3.5.18 referring to Page 7.18-1 Detail 5.

3.5.20 MAINS TRANSFORMER ASSEMBLY—REMOVAL
(Page 7.18-5 Detail 9)

a. Remove the Out-Guard and In-Guard Power Supply assemblies (see paras 3.5.10 and 3.5.12).

b. Disconnect the connectors from the transformer at the following assemblies:

J32 — Mother Assembly
J6 — Interconnection Assembly (fixed on the rear panel—see page 7.18-4 Detail 8).

c. Turn the instrument to stand on its left side (on Left Hand extrusion).

d. Release the four M8×110mm bolts, washers and nylock nuts.

e. Remove the M3×8mm pozi-countersunk screw, M3 steel nut and shakeproof washer which secures the solder tag terminals of four ground wires. Fold back the wire which is fitted to the rear panel assembly.

f. Remove the Mains (Line) Transformer assembly.

3.5.21 LINE TRANSFORMER ASSEMBLY—FITTING

Reverse procedure of para. 3.5.20, referring to Page 7.15.1 for re-assembly of items to the M8 transformer bolts.

3.5.22 HF TRANSFORMER ASSEMBLY—REMOVAL
(Page 7.18-4 Detail 6)

a. Remove four M3×8mm pozi-pan screws (Page. 7.18-4 Detail 6).

b. Disconnect connectors at the following points:

J2—High Voltage Assembly;
J5—Power Amplifier Assembly.

c. Remove the HV transformer assembly.

3.5.23 HF TRANSFORMER ASSEMBLY—FITTING

Reverse procedure of para. 3.5.22 referring to Page 7.15-2 for assembly of items to the M4 transformer bolts.

3.5.24 LF TRANSFORMER ASSEMBLY—REMOVAL
(Page 7.18-5 Detail 10)

a. Remove High Voltage assembly 3.5.18 and the Heatsinks 3.5.16.

b. Disconnect connector J2 and J5 from the Power Amplifier and High Voltage assembly.

c. Turn the instrument to stand on its right hand side (on R.H. extrusion).

d. Remove the HV transformer assembly.

3.5.25 LF TRANSFORMER ASSEMBLY—FITTING

Reverse procedure of para. 3.5.24 and refer to Page 7.15-2 for assembly of items to the M4 transformer bolts.

3.5.26 TERMINAL PCB ASSEMBLY
(Page 7.17-3)

Access:
Front panel (para 3.4.5)

a. Remove the four M3×6mm pozi-pan screws (7.18-4 Detail 8)

b. The terminal board can be tipped down to facilitate component access.

3.5.27 TERMINAL PCB ASSEMBLY—FITTING

Reverse the procedure of para 3.5.26.

3.5.28 REAR PANEL ASSEMBLY—REMOVAL
(Page 7.18-6)

WARNING.
DO NOT REMOVE THE REAR PANEL ASSEMBLY WHEN TOP AND BOTTOM COVERS AND GROUND/GUARD ASSEMBLIES ARE REMOVED.

Note:
This procedure provides access to rear panel-mounted components by releasing the Rear Panel assembly and moving it away from the chassis to the extent allowed by internal wiring connections.

Perform the following operations with Top and Bottom Covers and Ground/Guard assemblies fitted, or with AT LEAST the Top OR Bottom Ground Sheet assembly fitted.

a. Remove the six screws of the two rear spacers 7.18-4 Detail 7.

b. Remove the two rear spaces.

c. Remove the four screws of the filter grill.

d. Remove the filter grille and filter.

e. Remove the Pozi-pan screw revealed by the removal of the filter and grill.

f. Remove the four rear panel screws (Page 7.18-4 Detail 6).

g. Looking at the rear, locate the upper right hand screw, securing the extractor fan. Above this screw, locate an M3×6mm Pozi-pan screw. Removal of the latter allows the rear panel to be detached (see cut-away sketch of Rear Panel in Detail 6 of page 7.18-4).

CAUTION—Do not stress the wires.

h. Gently pull the Rear Panel assembly away from the chassis to the extent allowed by the wiring.

3.5.29 REAR PANEL ASSEMBLY—FITTING

a. Press the Rear Panel assembly to the chassis while ensuring that:

1. The wires lay in the cut-out in the moulded internal chassis;
2. The ribbon cables fit in the recess in the moulded internal chassis;
3. All other wires are free and not trapped by the rear panel assembly.

b. Fit screws, filter, filter grille and rear spacers, reversing the procedure of para. 3.5.28.

SECTION 4

TECHNICAL DESCRIPTION

4.1 PRINCIPLES OF OPERATION

SIMPLIFIED BLOCK DIAGRAM

Fig. 4.1.1. illustrates the general functions and signal flow within the 4200.

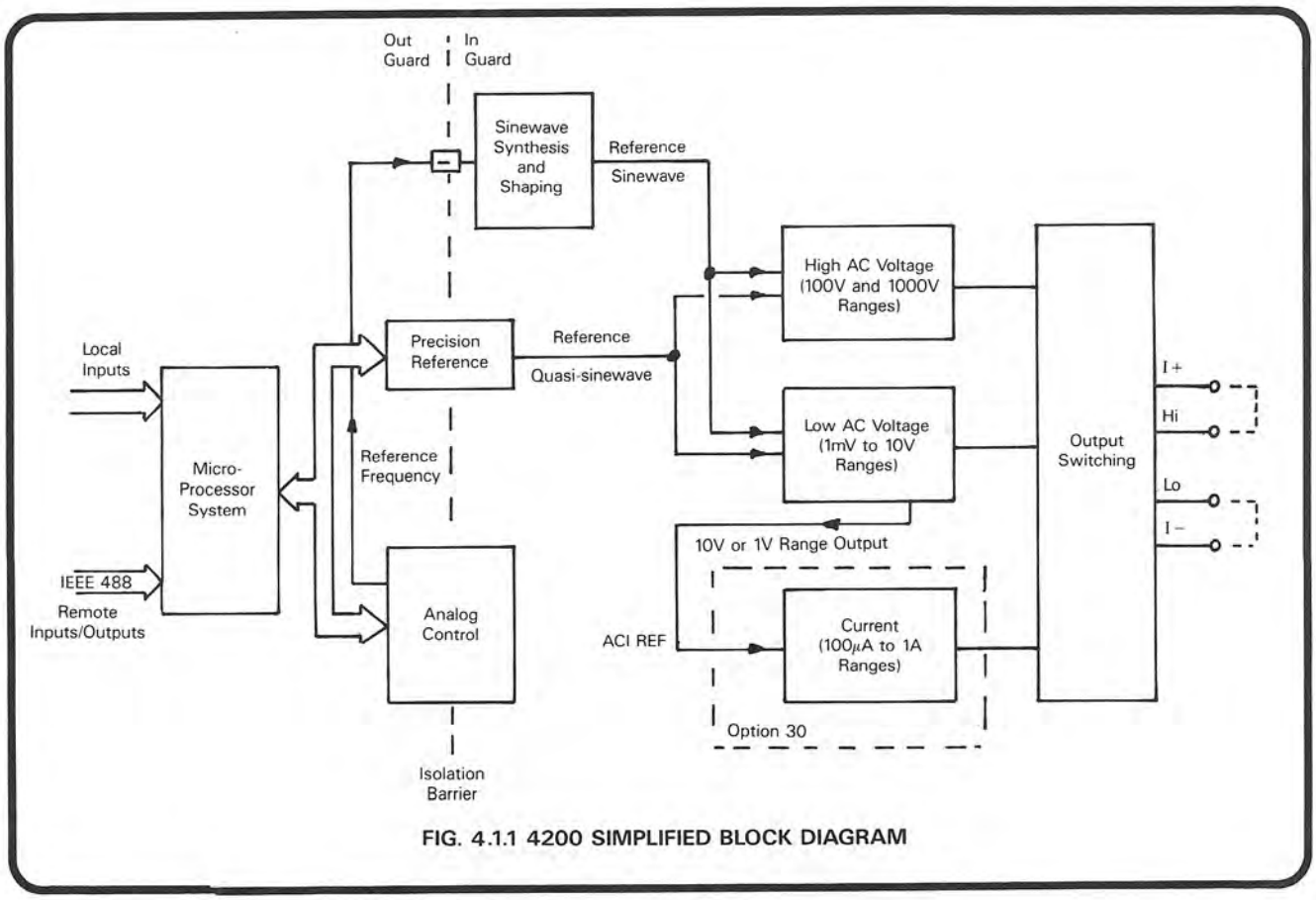


FIG. 4.1.1 4200 SIMPLIFIED BLOCK DIAGRAM

The 4200 AC calibrator is an accurate sinewave source, whose output frequency and amplitude are determined by user-inputs (within the specifications detailed in the User's Handbook).

Internally, the calibrator output frequency is synthesized using a crystal-controlled oscillator as a frequency reference. For amplitude control, an adjustable precision reference is derived from pre-conditioned zener diodes.

FUNCTIONAL BLOCK DIAGRAM

FIG. 4.1.2 (overleaf) breaks the main functional divisions into smaller blocks. It can be thrown clear of the handbook to provide a functional overview; it is also an index to other subsections of Section 4.

4.1.1 Inputs

The microprocessor accepts inputs from two main sources:

(i) The front panel keyboard provides local control inputs.

(ii) The IEEE 488 bus system provides remote control inputs.

4.1.2 Digital Outputs

The microprocessor system outputs digital information to five main areas:

(i) The front panel displays provide local monitoring outputs.

(ii) The IEEE 488 bus system provides remote monitoring outputs.

(iii) The frequency synthesizer and sinewave oscillator, which together determine the frequency and purity of the output sinewave signal.

(iv) The precision reference generator produces a reference quasi-sinewave to determine the amplitude of the output signal.

(v) Various decoders control functions and range selection, internal processes and status monitoring.

4.1.3 Precision Reference

The circuits produce a DC reference voltage which can be set between +0.126V and +2.794V, and which in turn is used to determine the amplitude of a stepped 'quasi-sinewave' signal. This is used as reference in the error sensing loop, having a waveform whose crest factor closely approaches that that of a true sinewave.

The circuitry is divided into three main areas:

(i) The period division comparator, outside guard, consists of a binary counter and comparator, both covering 25 bits. The counter is driven by a crystal-controlled clock; the comparator is set by data from the microprocessor system.

When the binary count matches the data set in the comparator, a switching pulse (reset) is produced. The counter continues to overflow point when it produces a second switching pulse (set). Thus accurate mark-period timing is generated.

(ii) The switching integrator receives the pulses across guard. They are used to drive a solid-state switch which chops the output from a very stable 20V DC Master Reference. This in turn produces a square wave which is very accurately defined both in mark-period ratio and amplitude.

This resultant square wave is integrated by an active low-pass filter with high rejection at the chopping frequency, to produce the DC Reference.

(iii) The quasi-sinewave generator uses the DC Reference voltage to set the positive and negative inputs to a center-tapped potential divider. The outputs from the divider are selected in equal time-steps by digital logic, with the division ratios so designed as to produce a periodic signal of quasi-sinusoidal form.

The signal's waveform has a crest factor of 1.397, close to that of a sinewave. Although its amplitude is adjustable by the DC Reference voltage, it remains stable once set. The RMS difference between sinewave and quasi-sinewave is stored during calibration, and reapplied as correction during normal use.

For accurate sine/quasi-sine RMS comparison, it is important that both the quasi-sinewave steps and the comparator sequence are synchronized to zero-crossing points in the sensed output sinewave. This is ensured by including the divide-by-ten logic of the quasi-sinewave generator as part of the range-divider chain for the frequency synthesizer. The quasi-sinewave frequency is also fed to the comparator, to synchronize a ten-step sequence which controls the RMS comparison process.

4.1.4 Analog Conrol

The analog circuitry is controlled by data held in a 48-bit in-guard latch. The microprocessor regularly updates the latch contents, using the serial link to pass the data (through opto-isolators) across the isolation barrier. Certain analog status signals are returned to microprocessor, also using the serial link.

4.1.5 Sinewave Synthesis and Shaping

The frequency synthesizer and quadrature oscillator together generate a reference sinewave of stable amplitude and high purity.

4.1.5.1 Frequency Synthesis

The user-demanded frequency is related to frequency range selection and expressed as a binary number 'n' by the microprocessor. It is passed into guard together with binary-coded frequency-range data, to control the frequency of the synthesizer.

The master crystal-controlled clock, at 4.096MHz, clocks the binary counter outputs in the reference divider. The counter outputs a 16kHz frequency reference signal to the synthesizer, where it is divided by two to 8kHz.

In the synthesizer, binary subdivisions of 'n' switch the capacitors of a voltage-controlled oscillator, adjusting its relaxation time-constant so as to cover five possible frequency bands within each frequency range. The VCO output frequency is divided by 'n', then compared in phase with the 8kHz reference. The integrated output from the phase comparator controls the charge and discharge current of the capacitors in the VCO. Thus the VCO frequency is adjusted to $n \times 8kHz$.

The frequency range data is decoded and used to define division ratios in a series of frequency dividers, which act on the output from the VCO. The result is the user-selected frequency, to an accuracy of 100ppm.

4.1.5 Sinewave Shaping

The binary number 'n' and the decoded frequency range data switch the circuit constants of the quadrature oscillator, to tune it approximately to the user-selected frequency. The oscillator and synthesizer frequencies are input to a second phase comparator, whose output pulls the oscillator frequency to that of the synthesizer.

The quadrature oscillator feedback is conditioned to ensure that 360° loop phaseshift occurs only at a specific amplitude; at the synthesized frequency.

The oscillator output is fed as reference sinewave to the VCA.

4.1.6 Low AC Voltage Output

4.1.6.1 Voltage-Controlled Amplifiers

The output from the quadrature oscillator is applied to two cascaded voltage-controlled amplifiers. The gain of the second of these (the 1V buffer) is adjusted in coarse steps; the gain of the first being adjusted in response to the error between the sensed and scaled output amplitude and that of the quasi-sinewave reference.

The settling curve of the 7-pole filter in the precision reference divider is imposed on the 1V buffer slew rate, by using the filter's DC reference output as control for the coarse gain. This signal is changed into a ten bit number by an analog-to-digital converter, whose digital output adjusts the input resistance of the 1V buffer in steps of 1000ppm of Full Scale. To compensate for the effect of this control on the gain of the error loop, the same 10-bit word is used to scale the error signal applied to the first VCA.

4.1.6.2 Low Voltage Outputs

On the 1V range, the output from the 1V buffer is passed to the I+ and I+ terminals directly.

For the 10V range, the 10V amplifier (on the Power Amplifier assembly) is included in the output path to the I+ and I− teminals.

For the millivolt ranges, the 1V buffer output signal is reduced by switched, passive attenuators before being output via the Hi and Lo terminals.

4.1.6.3 Low Voltage Sensing

On the 1V range, the input from the Hi and Lo (sense) terminals is applied to the non-inverting input of the 1V/10V sense amplifier, which acts as a voltage follower.

For the 10V range, the sense amplifier is configured as a divide-by-ten inverter.

For the millivolt ranges, there is no remote sensing. To complete the sense feedback, the 1V buffer output is input directly into the sense amplifier, which is a configured as for the 1V range.

4.1.6.4 Sine/Quasi-Sine RMS Comparator

In a strict sense, this circuit does not compare RMS values directly. Instead, it compares the magnitudes of the mean-squares of its two inputs, but if these are equal, then the RMS values are equal.

A cycling sequence is continuously imposed, each cycle with a duration of ten quasi-sinewave periods, whereby during the first cycle:

(i) the quasi-sinewave input is first squared and integrated as a DC analog reference;

(ii) the DC reference is memorized in a sample-and-hold circuit;

(iii) the sensed sinewave is squared, the DC reference value in (ii) being subtracted from the squared value;

(iv) the DC analog result is memorized in a second sample-and-hold circuit, and output as the AC error signal.

On subsequent cycles, the DC reference is also subtracted from the squared quasi-sinewave, so that both DC reference and AC error signals converge to steady states as the 4200 output reaches the demanded voltage.

The AC error signal is passed through the error scaling circuit to control the VCA.

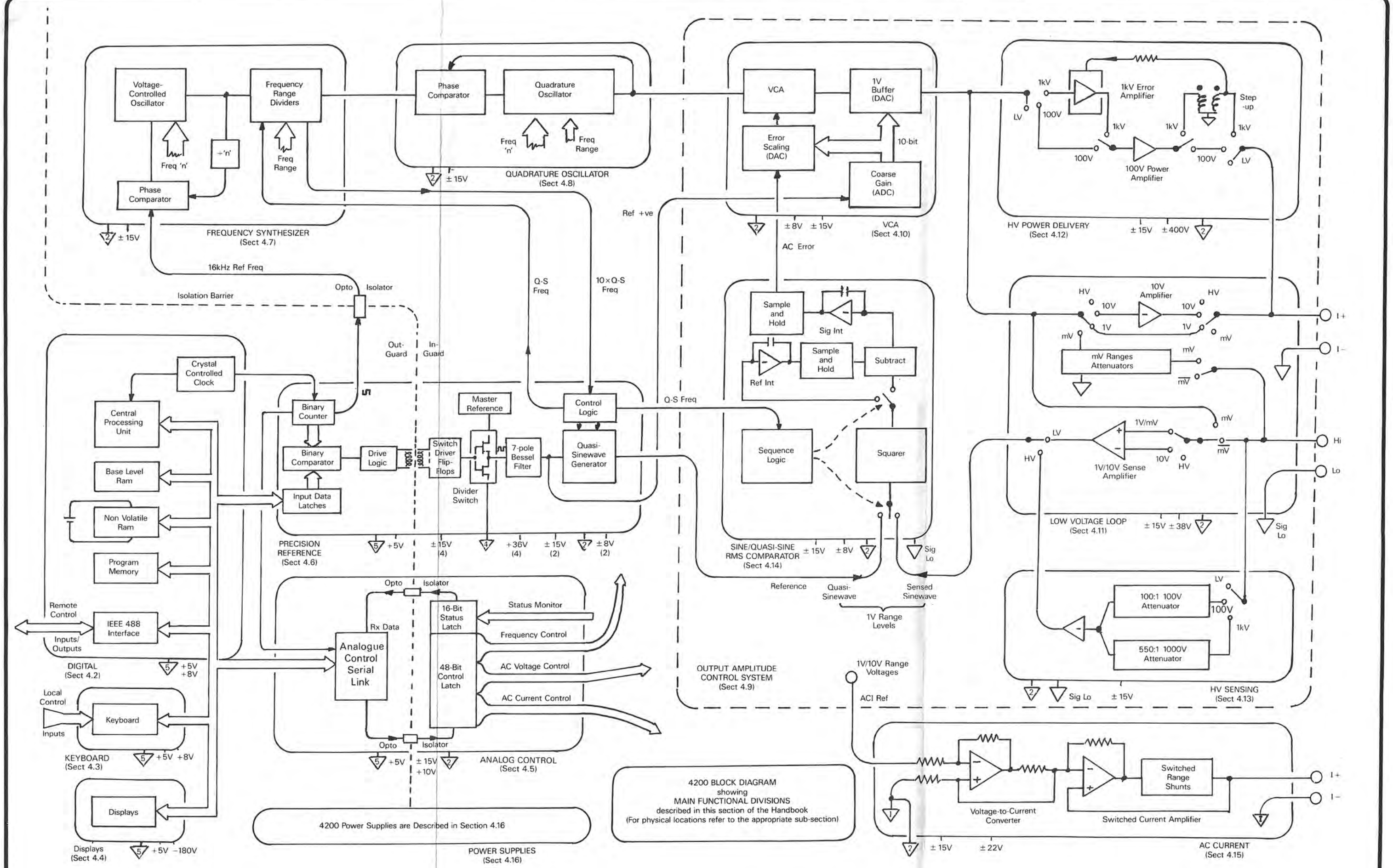


Fig. 4.1.2 4200 BLOCK DIAGRAM

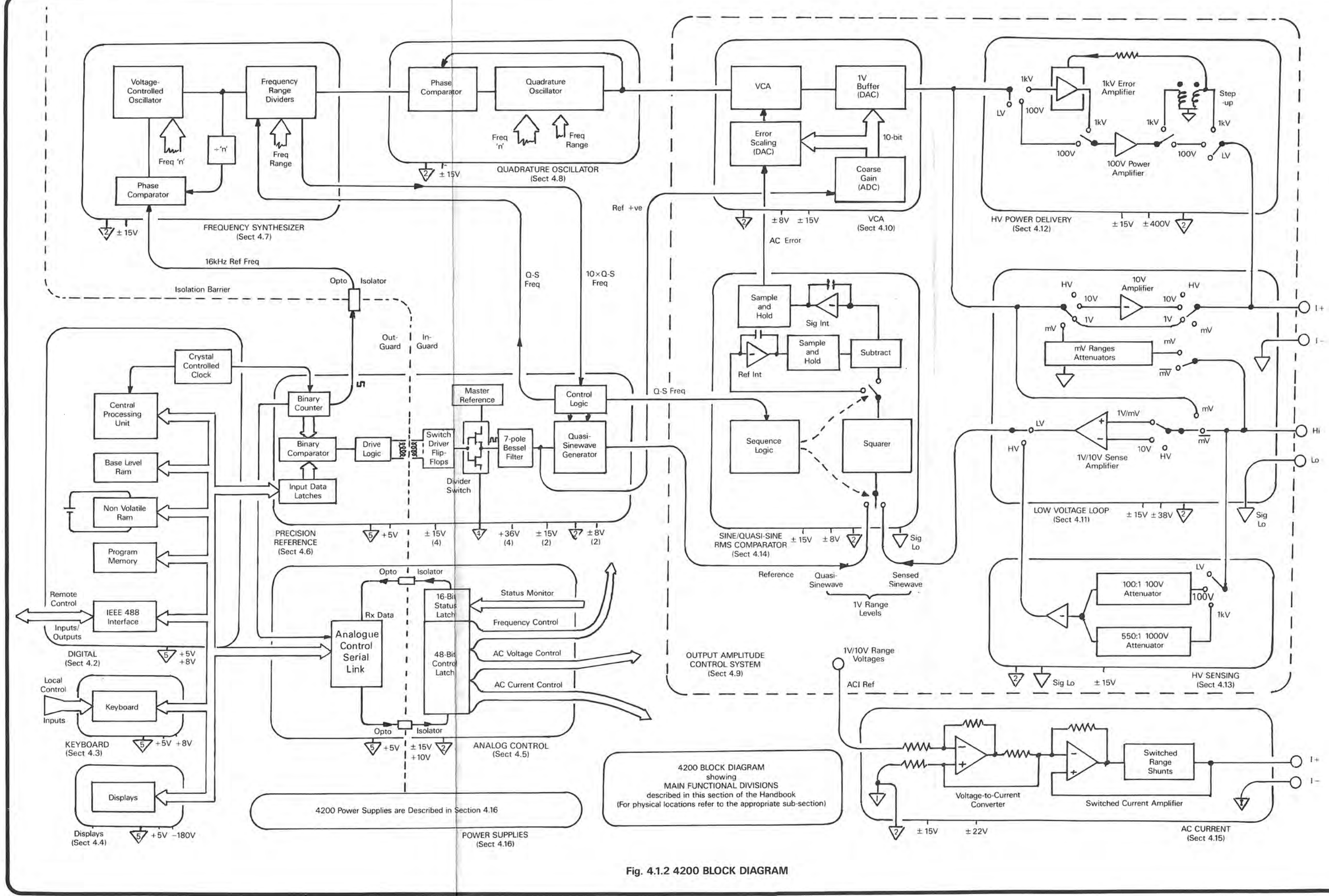


Fig. 4.1.2 4200 BLOCK DIAGRAM

4.1.7 High AC Voltage Loop

The high voltage loop uses much of the low voltage circuitry; the only differences being in the power amplification to the range voltages, and the attenuation of the sensed output down to 1V range levels.

4.1.7.1 High Voltage Outputs

On the 100V range, the 100V amplifier (on the Power Amplifier assembly) is included in the output path from the 1V buffer to the I+ and I− terminals.

On the 1000V range, the output from the 100V amplifier is transformed up by 6:1 before being passed to the I+ and I− terminals. An error amplifier is inserted in the input to the 100V amplifier to receive the feedback from the transformers; the HF transformer is selected as frequency is increased above 3kHz, and the other (LF) as frequency is reduced below 3.3kHz.

4.1.7.2 High Voltage Sensing

A separate inverting sense amplifier is used for the 100V and 1000V ranges. The basic amplifier is common to both, but each range has its own input attenuator and feedback ratio.

On the 100V range, the amplifier reduces the sensed sinewave by a ratio of 100:1, but on the 1000V range this ratio is 550:1.

For the 1000V range only, software scales the reference divider digital input to set the quasi-sinewave RMS value to the equivalent of 1100V Full Scale.

4.1.8 Current Output (Option 20)

For Current outputs either the 10V (for the 1mA, 10mA and 100mA ranges) or 1V (for the 100μA and 1A ranges) range circuitry is activated to generate the ACI reference signal. This is switched to drive a voltage-to-current converter, followed by current amplifier.

The various ranges are selected by digital control signals from the microprocessor system. Shunts in the current amplifier are switched into the output circuit to scale the current.

4.1.9 'AUTOCAL'

Although the instrument's circuitry utilizes precision components in all critical locations; frequency roll-off, offset and gain errors remain (in analog terms) uncorrected. At calibration these errors are measured and stored digitally in non-volatile memory.

In subsequent use, characteristic equations are applied to the stored errors to generate software corrections, which are then used to modify the reference divider ratios and so compensate for the analog errors.

4.2 DIGITAL

The circuits described in this section perform the following functions:

(1) Central processing, with supporting memory, for management of instrument operation.

(2) Storage of calibration constants in non-volatile memory.

(3) Generation of Master clocks, with clock-waveform shaping.

(4) Address decoding to generate control signals.

(5) Controlled power-up and power-down of digital circuits.

(6) Servicing IRQs from asynchronous sources.

(7) Interfacing the 4200 to the IEEE 488 bus.

The functions are performed by circuits located mainly on the Digital PCB Assembly (400534). Master Clock generation, synchronization and division is carried out by circuits on the Analog Interface PCB Assembly (400570).

Fig. 4.2.1 shows the arrangement and main inter-connections of the central digital circuits.

4.2.1 General

The 4200 is managed by a 6802-series microprocessor system, under the control of an operating program held in 24k bytes of EPROM. All front and rear panel controls provide direct inputs to the sysem, except for the Power ON/OFF switch and Safety Reset Key. The System ensures that the processor reverts to a safe state on power-up and power-down.

2k bytes of random-access memory (RAM) are used for work space and stack. A further 2k bytes of CMOS RAM act as a non-volatile memory to hold calibration constants, powered by a back-up Lithium battery when the instrument is turned off.

4.2.1.1 Synchronous Operation

The operating program manipulates the internal circuitry by activating control signals. These result from providing peripheral decoders with specific address combinations. The program is run at 680kHz cycling frequency, originally derived from a 4.096MHz master crystal oscillator.

4.2.1.2 Asynchronous Operation

Any Key operation (other than Safety Reset), or one of two internal conditions, will initiate an asynchronous interrupt (IRQ) which suspends the CPU's current task. The CPU absorbs the new instructions, rearranges its schedule to conform to the demanded new configuration, then continues with the interrupted task until it is completed. It next returns to the initial operation of the amended task schedule and proceeds synchronously.

Three main sources of interrupt are used:

Remote Command via the Digital Interface

Keyboard Command

Real-time Clock Pulses (8ms intervals)

The CPU identifies the source by polling the data bus each time it receives an IRQ interrupt.

4.2.1.3 Output Generation

From user inputs of output value, frequency, error and calibration constants, the CPU computes a binary value to a resolution of 25 bits. This is used to adjust the mark/period ratio of the Reference Divider switch which ultimately controls the Working Reference Voltage for the output analogue circuitry.

4.2.1.4 Display Refresh

The gas discharge display is continuously refreshed by cycling through character data stored in a separate display-image RAM. To alter the display the processor merely alters the contents of the RAM.

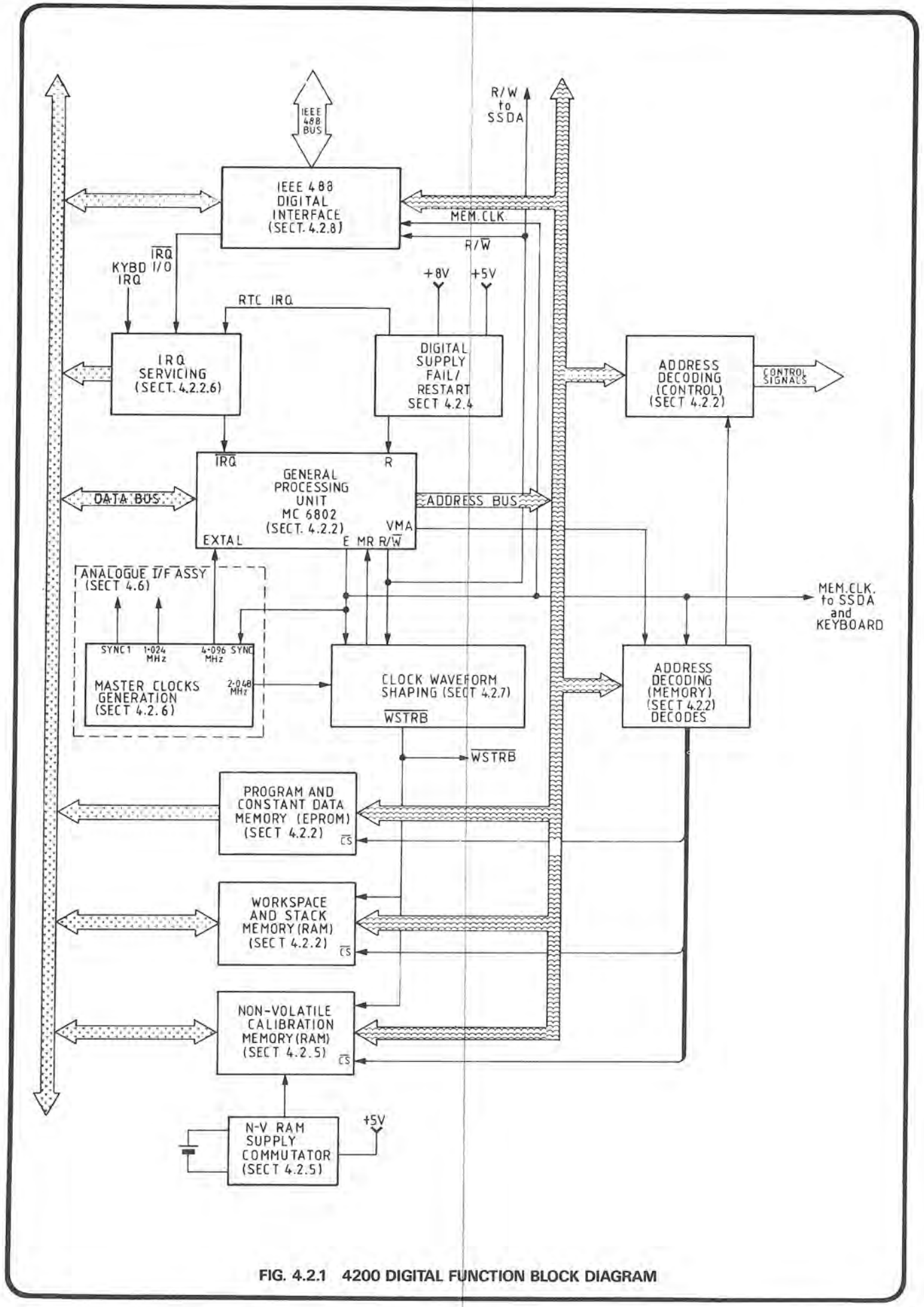


FIG. 4.2.1 4200 DIGITAL FUNCTION BLOCK DIAGRAM

4.2.2 Central Processor and Memory

(Circuit Diagram 430534 Pages 7.2-2 and 7.2-3)

A 6802 microprocessor, (M34), together with its memory, controls communication throughout the whole instrument.

4.2.2.1 Memory

The memory can be split into five main areas:

(1) Program Memory (M19, 20, and 21)	defines and controls the operational functions of the whole instrument system.
(2) Constant Data Memory (held in EPROM with the Program Memory)	e.g. Instrument specification for use in 'Spec' mode, key mapping tables and other fixed factors.
(3) Non-Volatile Calibration Memory (M23)	stores all the calibration constants, determined during the 'Auto-cal' cycle, which are used for each output value.
(4) Volatile Memory (M22)	used for volatile data storage, e.g. display images, computational stores, present output value.
(5) Operating Memory (M22)	used for scratch pad operations and storage.'

The 6802 microprocessor internal RAM is not used.

Separate memory is used for special purposes, such as the Display Image RAM (M16) which is synchronously loaded but asynchronously read; the storage areas in the IEEE 488 GPIA (M29) and the Keyboard Interface (M6 on Front Assembly); and the Memory Address decoder PROM (M3). These are described in later sections.

4.2.2.2 Central Processing Unit

(Circuit Diagram 430534 Page 7.2-2)

The MC6802 (M34) is a monolithic 8-bit microprocessor, with interrupt and clock-stretching facilities. It is driven by a single phase 4.096MHz square wave generated by the Master Clock X1 in the Analog Interface Assembly. (This clock synchronizes the reference divider switch with the processor cycle).

4.2.2.3 Address and Data Lines

Address lines A_{15-11} are decoded as chip-select signals for the RAM/ROM circuit, and lines A_{13-0} are connected to the instrument address bus. Data lines D_{7-0} are linked via programming plug JL1 to the instrument data bus.

4.2.2.4 E, MR and MEMCLK

The 4.096MHz clock input at M34-39 (EXTAL) is divided by four and used as output at M34-37(E). Although the natural frequency of E is 1.024MHz, the action of the waveform shaping input to MR reduces it to approx. 680kHz as MEMCLK for the Front and Analog-Interface assemblies.

4.2.2.5 $\overline{\text{NMI}}$

The internal switch S1 provides a non-maskable hardware interrupt which has two functions.

(1) With the external CALIBRATION switch set to RUN, $\overline{\text{NMI}}$ initializes the processor system.

(2) With the CALIBRATION switch set to ENABLE, $\overline{\text{NMI}}$ clears the non-volatile calibration memory (M23) before initializing the processor system.

4.2.2.6 $\overline{\text{IRQ}}$

Any one of three asynchronous Interrupt Request signals are able to activate the maskable $\overline{\text{IRQ}}$ input at M34-4:

(1) RTC IRQ is a real-time clock which occurs every 8ms to provide timing information for the processor's monitoring facility.

(2) KYBD IRQ occurs each time a front panel key is depressed. (Not Safety Reset).

(3) $\overline{\text{IRQ}}$ IO occurs when the IEEE 488 Interface has a transaction to communicate to the processor.

D1, D2 and Q1 constitute a DTL OR-gate to isolate the IRQ inputs from each other. On receipt of Logic-Ø on pin 4, M34 stores its register contents in stack RAM, and vectors to IRQ service addresses FFF8 and FFF9, saving the current processor environment.

The IRQ Service Routine addresses M51 and M52, generating logic-Ø at M52-9 which enables the tristate buffers M36 and M37 at M36-1 and 15, M37-15. This sets IRQ data bits D5, D6 and D7 on the data bus so that the processor can identify the source of the IRQ and select the appropriate sub-routine to service the interrupt request.

The IRQ inputs are released as part of the service sub-routine, and after its completion, the processor recovers its environment from stack RAM and proceeds with the interrupted operation.

4.2.2.7 Software Interrupt

The 6802 will also recognise Opcode 3F on the data bus as an interrupt request ('Implied' addressing mode'). In the 4200 this code is hard-wired via R9, R10 and AN3 onto the data bus so that if the CPU tries to access a non-available address, the floating bus will be pulled to 3F, initiating the software interrupt. The CPU vectors to FFFA and FFFB, whose contents cause the 6802 to re-initialise the whole system.

4.2.2.8 Read-write line R/$\overline{\text{W}}$

The processor sets the R/$\overline{\text{W}}$ line to logic-1 when it is in Read state, and logic-Ø when it has data to write into the addressed device. The R/$\overline{\text{W}}$ signal is passed only to the SSDA on the Analogue Interface assembly, and to the IEEE 488 GPIA (M29). All other devices which require read-write control, operate from RDSTRB and WRTSTRB signals generated from R/$\overline{\text{W}}$ by M49/50.

4.2.3 Software Overview

The software management organisation is shown in Figure 4.3.2. The machine cycle, which progresses through the task schedule shown, is modified by the requirements of real-time-conscious activities and by those dedicated to remote commands. Real time and remote command interrupts suspend the current activity of the processor in order to service the immediate task requirement; the suspended task is then resumed.

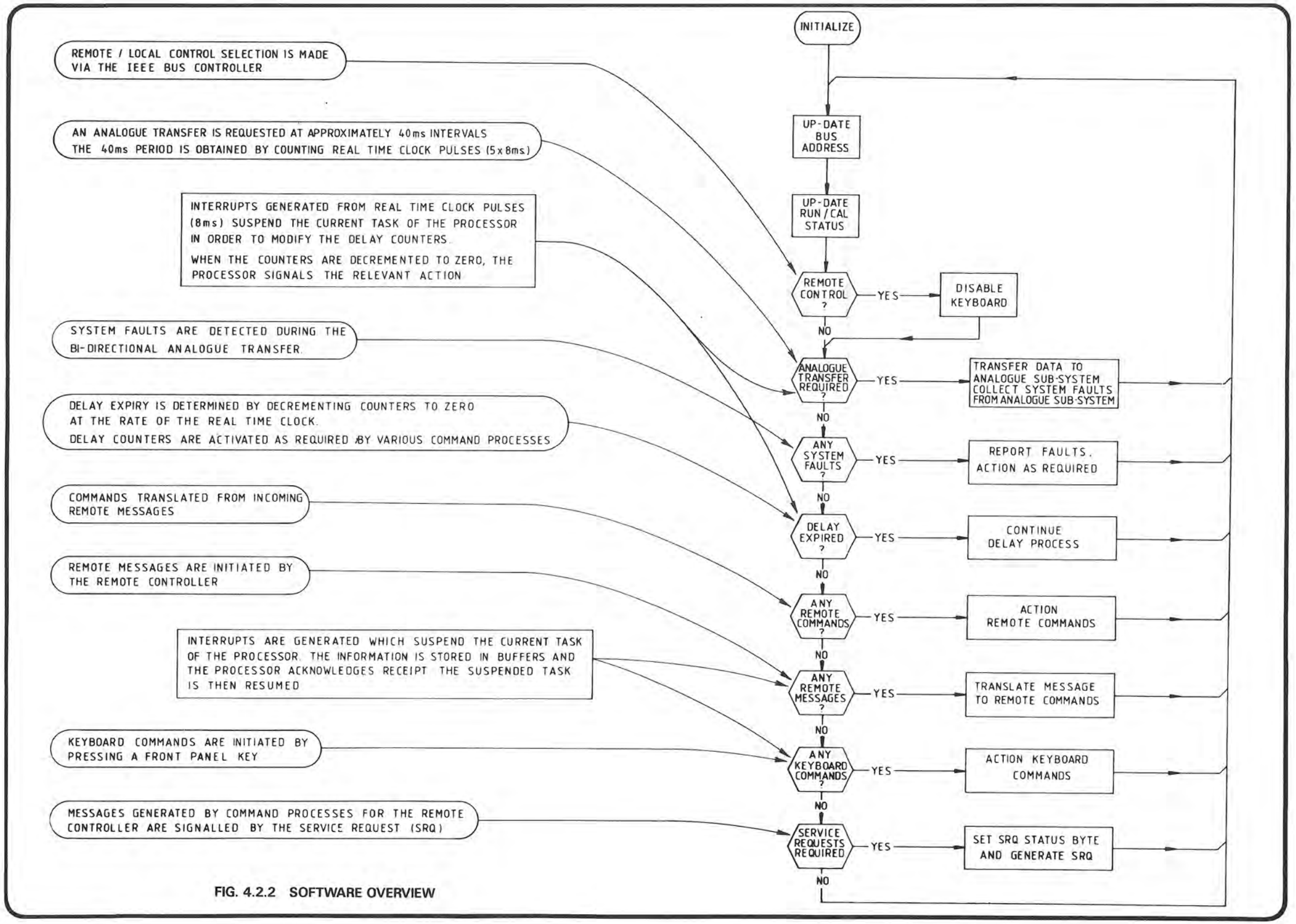


FIG. 4.2.2 SOFTWARE OVERVIEW

4.2.4 Digital Supply Fail/Restart Circuitry

Power-up, restart and shut-down of the digital circuitry are performed in a controlled sequence to safeguard against hardware failures or a software crash. A continuous surveillance of the software management is performed by the safety monitor (Watchdog – refer to Section 4.5). This will shut-down the instrument in the event of a failure in either the digital control circuits or in software management.

4.2.4.1 Power-up Sequence
(Circuit Diagram 430534 Page 7.2-2)

Power-on is first sensed by the Supply Fail Detector circuit. This draws its supplies from the +8V DC unregulated supply, which is the first of the power supplies to rise to a working level. The comparator circuit of M28 has a nominal threshold of +7.1V DC, above which a good working level of the +5V DC supply is assured.

As the +8V supply rises, below +7V, M28-2 follows until Zener D6 avalanches, when it is held at +2.45V. At this level M28-3 voltage is less than 1V, so M28-1 remains at 0V holding M8-5 'D' input at logic-Ø and M7-3 at logic-1. Thus M8 and M9 are held in reset, initiating and maintaining the following state:

(1) M8-2 ($\bar{Q}$) at logic-1, PWR ON RST active. Fed to the front panel assembly, this logic-1 level holds keyboard encoder M6 in Reset and disables the LED cathode driver decoder M4.

(2) M6-4 at logic-Ø, $\overline{\text{PWR ON RST}}$ active. This logic-Ø level holds the microprocessor M34 in Reset state. Its VMA output at M34-5 is held at logic-Ø disabling address decoder M3, setting all M3 address outputs to logic-1. This combination gives logic-1 at M5-13, but M6-2 at logic-Ø gives logic-1 at M5-11 and subsequently logic-1 at M7-2.

The logic-Ø of $\overline{\text{PWR ON RST}}$ also holds the IEEE 488 GPIA M29 (page 7.2-4) in Reset. It is also fed to the Analog Interface assembly where it holds the SSDA M44 in Reset.

When the +8V supply rises above about +7.1V, M28-3 voltage rises above the +2.45V on M28-2, so M28-1 rises to place a logic-1 both on M8-5 (D input) and M7-1. M7-3 falls to logic-Ø, removing the resets from 14-bit counter M9 and restart flip-flop M8. So M8 is enabled to receive its clock from M9, which itself is clocked from 2.048MHz.

At full count, 8ms after M9 is enabled, M9-3 clocks M8. As M8 'D' input is already at logic-1, this is clocked through to M8-1 (Q), and logic-Ø to M8-2 (Q). PWR ON RST and $\overline{\text{PWR ON RST}}$ change to their inactive states, and start-up proceeds:

(1) PWR ON RST at logic-Ø.:

Enables keyboard encoder M6 and LED cathode driver decoder M4 on the Front assembly.

(2) $\overline{\text{PWR ON RST}}$ at logic-1:

a. Removes reset from CPU M34, allowing software initialization to commence, and enables IEEE bus controller M29 on the Digital assembly.
(Part of the instrument initialization procedure is a software reset for M29).

b. Removes reset from the SSDA M44 on the Analog Interface assembly.

(3) M8-1 to logic-1:

a. Provides an enabling input to M10-1 (See Non-Volatile RAM Supplies Section 4.2.5).

b. Triggers monostable M53-4. This monostable has a relaxation period of 470ms; during which time it holds the $\overline{\text{FP RST}}$ output at logic-Ø, allowing the watchdog circuits to reset on the Reference Divider.
(See Safety Monitor Section 4.5).

c. Enables RTC IRQ via M7-13.

Address decoder M51-5 is normally held at logic-1, so M7-11 and M8-10 at logic-Ø allow M9-3 clock to affect the RTC IRQ output at M8-13.

For so long as the +8V supply holds up above +7.1V, M9 continues cycling through its full count, clocking M8-11 at 8ms intervals.

To terminate an RTC IRQ service sub-routine, the CPU addresses M51, pulsing M51-5 (M7-12) to logic-Ø (RTC RST). M7-11 is pulsed to logic-1, resetting M8-13 (RTC IRQ) to logic-Ø.

At the next full count of M9; M8-13 is clocked to logic-1, initiating the next RTC IRQ.

The actions of M9, M8 and M51 thus generate a 'Real-Time Clock IRQ' at 8ms intervals.

Pulses from M9-3 also regularly clock the binary state of M8-5 throught to M8-1, monitoring the supply status. When running normally, M8-5 and M8-1 are both logic-1. If the supply fails, M8-5 reverts to logic-Ø, but a fast reset is also provided by M7-1 logic-Ø to M8-4 logic-1, rather than waiting for the next clock pulse. M7-3 also resets the 8ms counter to zero count at M9-11.

4.2.4.2 CPU Re-start

(Circuit Diagram 430534 page 7.2-2)

Memory addressing by the CPU is monitored by the NAND logic of M4, M5 (four elements) and M7-3. In the correct addressing sequence there are two basic conditions:

(1) CPU VMA = Logic-Ø
M3-D0 to D7 = Logic-1

(2) Valid memory address:
CPU VMA = Logic-1
CPU E = Logic-1
M3-D0 to D7 = One address line logic Ø

Conditions (1) and (2) both result in a logic-Ø from M7-3, allowing clock M9 and flip-flop M8 to function normally. The possibility of a glitch occurring at the change-over between conditions (1) and (2) is gated from the control line by switching at M5-5. Incorrect addressing sequence in the CPU would be shown by:

CPU VMA = Logic-1 } The CPU indicates that it has
CPU E = Logic-1 } selected a valid external address.
M3-D0 to D7 = Logic-1 No address is selected.

This situation is most likely with a software failure. The logic control path through M4, M5 now gives a logic-Ø at M7-2 and thus a logic-1 at M7-3 which:

(1) Resets counter M9 to zero;

(2) Forces M8-1 to Logic-Ø. This forces RTC RST at M7-11 and removes an enable from M10-1. (See Non-volatile RAM supplies Section 4.2.5).

(3) Forces M8-2 to logic-1. This change:
a. Resets the CPU by M34-40 to logic-Ø. VMA is forced to logic-Ø which in its turn removes the reset from M9-11 and M8-4 via M6-2 (at logic-Ø), and the M4-M5 control path.
b. Makes PWR ON RST and $\overline{\text{PWR ON RST}}$ signals active, thus resetting the other software-controlled areas.

After 8ms from CPU reset, flip-flop M8-3 is triggered from clock M9. M8-1 and M8-2 change state and the start-up sequence proceeds.

4.2.5 Non-volatile RAM Supply Commutation

4.2.5.1 Non-volatile RAM Inhibit (NV INHIBIT)

(Circuit Diagram 430534 page 7.2-2)

Chip-select to the non-volatile memory M23 is inhibited during power-up, re-start and power-down operations. Memory access to the non-volatile RAM is enabled during normal running by the chip-select input $\overline{\text{NV INHIBIT}}$ being held at logic-1. The NAND logic gates M10, used to control the inhibit, remain powered from the RAM standby supply after power-down.

Conditions for normal running are as follows:

(1) Supply fail detector circuit provides a logic-1 (supplies valid) output to opto-coupler M11. This causes the coupled transistor of M11 to conduct and hold M10-2 at logic-1.

(2) M10-8 is held at logic-1 (to +5V via R6).

(3) M10-1 is held at logic-1 by flip-flop M8-1.

The above conditions ensure a logic-1 output from M10-10 ($\overline{\text{NV INHIBIT}}$ not active).

During power-up, $\overline{\text{NV INHIBIT}}$ is held active until the power supplies have settled and the CPU has gained control of memory:

The input to M10-8 is delayed on the +5V supply by the time-constant C8, R6. Also, the input to M10-1 is held at logic-Ø by flip-flop M8-1 until the CPU reset is removed.

At power-down, or in the event of a supply failure, the $\overline{\text{NV INHIBIT}}$ becomes active before 5V supply fails:

The first indication of supply failure is made by supply fail detector M28 output going to logic-Ø. This cuts off the opto-coupler M11 which takes M10-2 to logic-Ø. M10-8 is held at logic-1 by the +5V supply, thus M10-9 is taken to logic-1 and M10-10 to logic-Ø ($\overline{\text{NV INHIBIT}}$ active).

In the event of a CPU reset, the $\overline{\text{NV INHIBIT}}$ is made active for the period of reset by the switching action of M8-1 and M10-9.

4.2.5.2 Supply Commutator

(Circuit Diagram 430534 page 7.2-3)

This circuit provides the non-volatile RAM M23 with a battery-driven standby supply when the instrument is in the power-down condition. It ensures continuity of supply in the change-over between main and standby, and minimizes battery current leakage.

In the power-down condition, the battery powers M10 and M23, returning from battery common (TP13) via D7 and R60. The battery common is isolated from the general common 5A by transistor Q2, which is cut-off.

During power-up, M28 is powered from the +8V supply before the +5V supply voltage becomes established. As long as the +5V supply voltage is less than the battery voltage, Q3-4 is biased negatively, and Q3 is unbalanced in favour of heavy conduction through Q3-6. M28-5 is held low, so M28-7 remains at Common-5A potential, and so opto-coupler M39 is not energized.

Q2 remains cut off, maintaining isolation of the battery supply from Common-5A.

M10 and M23 remain powered from the battery.

As the +5V supply voltage increases, D7 cathode potential rises, reducing Q3-4 bias, reaching zero when its voltage is equal to the battery voltage (less than 10mV is developed across R60).

When the +5V supply voltage exceeds the battery voltage, Q3 becomes biased in favour of heavy conduction through Q3-2, pulling M28-6 low and reversing the differential input to M28. M28-7 rises to the +8V rail and energizes the opto-coupler M39, which switches Q2 on, connecting battery common to common-5A. M10 and M23 are now powered from the +5V supply and the standby battery is isolated by reverse-biased diode D7.

During power-down, Q3 compares the +5V supply against the battery, switching Q2 off via M28 and M39 when the +5V supply voltage falls below the battery voltage, and the non-volatile RAM supply commutates to standby battery. Alternatively, Q2 is switched off by failure of the +8V supply to M28 if this occurs before the +5V supply voltage falls below the battery voltage.

Eventually the +5V and +8V supplies both fall to zero, the battery provides the supply to the non-volatile RAM, and battery common is isolated from Common-5A by Q2.

4.2.6 Master Clock Generation

(Circuit Diagram 430570 page 7.3-3)
(Refer to Fig. 4.2.3 for waveforms)

The master clock generator is based on crystal oscillator XI which provides a precision 4.096MHz squarewave reference frequency output.

The primary frequency of 4.096MHz is divided by JK flip-flop stages M41, both of which are connected to toggle when clocked. The first division stage is synchronized at its reset input, M41-3, to the memory clock via flip-flop M42. This ensures correct phasing of the 2.048MHz squarewave output from M41-14.

M41-11 and M41-10 outputs provide complementary 1.024 and $\overline{1.024\text{MHz}}$ squarewaves respectively. Monostable M40, triggered at 2.048MHz from M41-15 provides the positive-going 2.048MHz synchronizing pulses, SYNC 1.

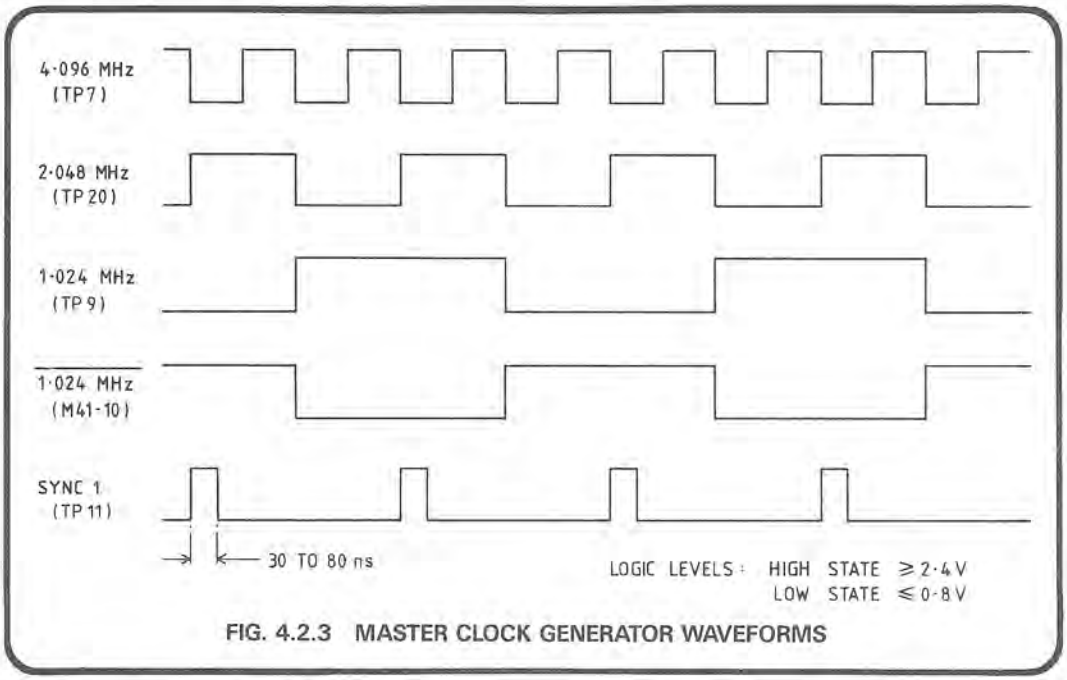


FIG. 4.2.3 MASTER CLOCK GENERATOR WAVEFORMS

4.2.7 Clock Waveform Shaping

(Circuit Diagrams 430534 page 7.2-2
and 430570 page 7.3-3)

NB As the circuit locations in Fig. 4.2.5 are clearly marked, and as there are no duplicate designators in the circuits, this description does not refer to a component's location except where necessary.

NOTE To avoid confusion, the terms 'high' and 'low' are used to replace 'logic-1' and 'logic-Ø' respectively in this description.

The crystal oscillator on the Analog Interface Assembly provides a 4.096MHz Master Clock signal (X1-8) for the whole instrument. This drives the 6802 microprocessor at M34-39 (EXTAL) so M34-38 is not connected. M41 divides 4.096MHz to generate a 2.048MHz clock for the Memory Clock Stretching Circuit (M35/M49).

The CPU (M34) divides the EXTAL input internally by 4 and outputs the result as E (Enable) at M34-37, to act as a 'Phase 2' Memory Clock for the SSDA on the Analog Interface and the keyboard controller on the Front assembly.

If M34-3 (MR—Memory Ready) were permanently held at +5V, the E signal would be 1.024MHz. But in the 4200, a 'stretching' circuit (M35/M49) doubles the Logic High (+5V) time of E by switching MR to Logic Low (0V) for part of the cycle. This is shown on Fig. 4.2.4.

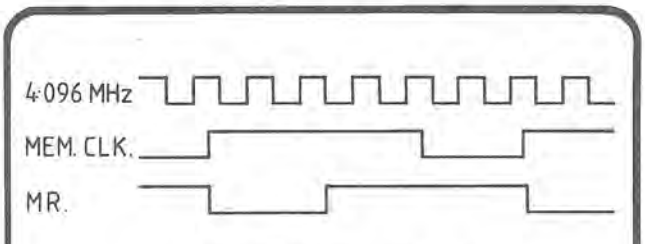


FIG. 4.2.4 MEMCLK TIMING

The frequency of E is thus reduced to approximately 680kHz, with 1μs available for access to the SSDA, Keyboard Controller, IEEE GPIA and memory.

4.2.7.1 Memory Clock Stretching Circuit
(Fig. 4.2.5)

The action of M35 and M49 is dependent upon the finite propagation time between clocks at M35-1/M35-6 and Q output at M35-15.

When M34-3 (MR) is +5V; M34-37 (E) is toggled by alternate positive-going edges of the 4.096MHz clock, with a propagation delay of approximately 80ns.

Also, the 4.096MHz signal is divided by 2 in M41, resulting in 2.048MHz signal whose negative-going edges clock M35.

M35 cascade action is controlled by the condition of the Memory Clock (E) and affected by its own propagation times.

4.2.7.2 Shaping Action
(Figs. 4.2.5 and 4.2.6)

At T1 and T2:
The 4.096MHz clock edge at T1 causes E to rise from low to high at T2. As M35-10 is also high, MR changes from high to low at T2, holding E high. M35 pin state is 4 and 10 high, 9, 12 and 16 low.

At T3 the 2.048MHz falling edge clocks M35, and M35-9 rises to high awaiting the next clock edge (not until T5). M35-10 remains high, so MR is held low and E stays high.

At T4, MR is still low, so the 4.096MHz clock has no effect on E, and E is stretched.

At T5, MR is returned to high when the logic-1 on M35-9 is clocked as a logic-Ø to M49-4. This allows the 6802 to toggle E at the next effective clock edge.

At T6 the rising edge of the 4.096MHz clock causes E to fall to low, setting up M35-4 to low, M35-12 and 16 to high. M35-9 is already high.

At T7, M35-10 is toggled to high, but as M49-5 is now low, MR remains high to allow E to be toggled at the next effective processor clock edge (not until the next T1).

Also at T7, M35-15 is clocked to low to set M35-9 ready for the next (T3) clock edge. The circuit is now set up to its initial (pre-T1) condition so the action repeats.

4.2.7.3 M41 Reset
(Fig. 4.2.5)

A remote possibility exists, that a severe disturbance could upset the synchronization of the 'E' signal with the 2.048MHz clock. To guard against this, M42 acts as a monostable to provide negative reset pulses into M41-3. Under all normal conditions, these will occur when M41 is already toggled in its reset state.

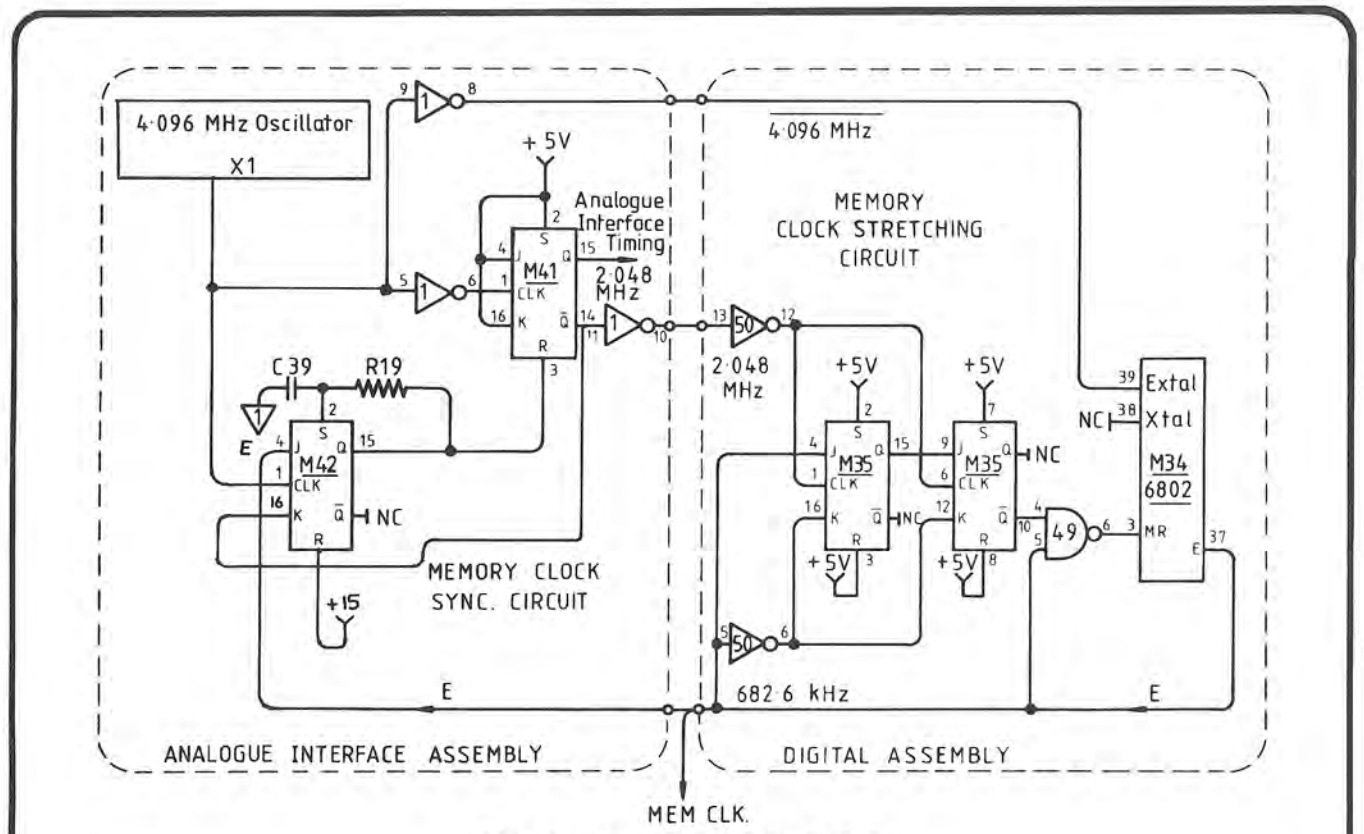


FIG. 4.2.5 CLOCK SHAPING CIRCUIT

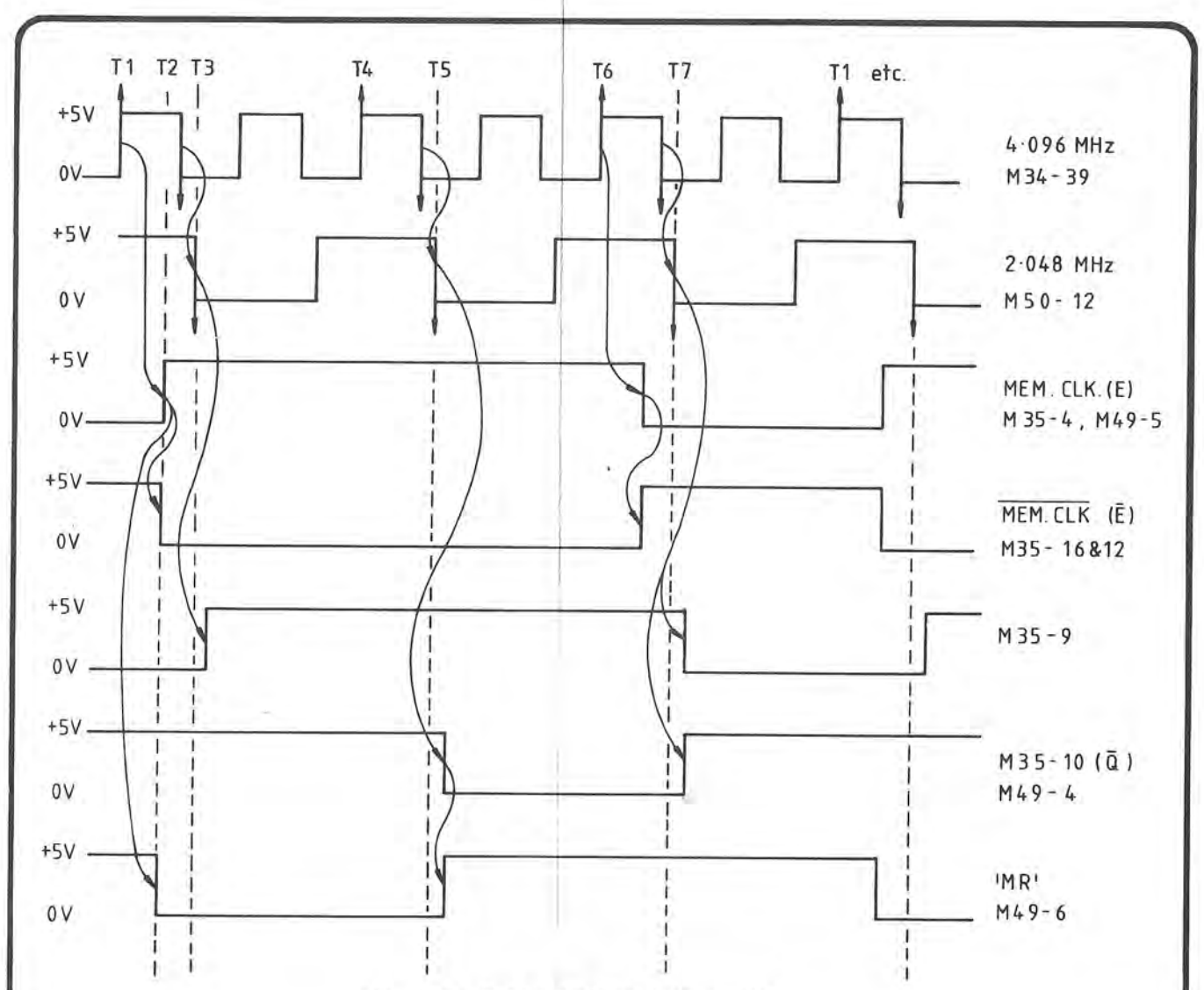


FIG. 4.2.6 CLOCK SHAPING WAVEFORMS

4.2.8 IEEE 488 Digital Interface

(Circuit Diagram 430534 Page 7.2-4)

The IEEE Interface circuitry is located on the bottom right-hand corner of the Digital PCB (viewed from the front of the instrument). M29, M40, M47 and M48 execute and decode interface functions, and transfer data (input/output).

The General Purpose Interface Adaptor (GPIA) M29, is software-driven by the 6802 CPU, as part of its normal function. M29 is addressed at C5 by $\overline{\text{XIOBBD}}$ from M51, and its internal registers are accessed by A_0, A_1 and A_2 from the address bus.

The GPIA is clocked by Memory Clock E, with read or write control direct from the processor R/$\overline{W}$ signal at M29-5, and at 4200 power-on M29 is initialized at M29-19 by the $\overline{\text{PWR ON RST}}$ signal from the Restart Generator circuit (M6-4).

Information is passed between M29 and the CPU (M34), via the data bus D_0-D_7. The address switch data is linked to D_0-D_6 by tristate buffers M47. During initialization and at subsequent intervals, the state of M29-4 (ASE) changes from +5V to 0V, enabling M47. The status of the address switches on the 4200 rear panel is transferred into M29 via M47 and the data bus for comparison with the received address.

M40 and M48 are bidirectional bus-driver arrays. The drivers for bus management lines: IFC, ATN and REN are permanently held in Receive state, and the SRQ driver in Transmit state. The EOI line driver is switched from Receive to Transmit by M29-28 (T/$\overline{R}$1) changing from 0V to +5V as required by M29. M29-27 (T/$\overline{R}$2) is normally held at 0V for reception of system data via DIO 1-8 bus lines, and set to +5V for 4200 data to be sent over the bus.

Some system controllers output excessive noise along the REN line. To avoid spurious switching of M29 between Local and Remote control states, the noise is filtered by R58 and C31.

Difficulty has been experienced with certain controllers in that NDAC can transfer data on to the bus too early. R62 and C7 slows down the transitions of NDAC to overcome this problem.

M29-40 ($\overline{\text{IRQ}}$) is used to inform the CPU when certain states occur. In particular, the $\overline{\text{IRQ IO}}$ signal is generated at each byte-transfer over the bus, whether the byte is sent or received. Additionally, $\overline{\text{IRQ IO}}$ is activated whenever certain specific commands are received, e.g: 'DAC', 'SPA', and changes between Remote and Local Status.

When the CPU receives $\overline{\text{IRQ IO}}$, it addresses M29's 'Interrupt' Status Register, then M29 identifies the reason via the instrument data bus.

For further information refer to 'Getting Aboard the 488 Bus' published by Motorola, or the appropriate device data sheets.

4.3 KEYBOARD

(Circuit Diagram 430533 Page 7.1-1)

The circuitry described in this section performs the following functions:

(1) Provides front-panel operator control of 4200 Output, Function, Range and Mode circuitry, by push-button keys. Key operation is detected internally and transferred to the CPU via the instrument data bus.

(2) Indicates the current instrument state by means of LEDs fitted in the Keys.

(3) Generates audible warning of high voltage at the Output Terminals.

In addition a rocker switch sets instrument Power ON and OFF (refer to Section 4.16) and a 'Safety Reset' Key provides a hardware reset for the safety monitor (Watchdog) circuits (refer to Section 4.5). The circuitry is located on the Front PCB Assembly (400533), linked to the CPU by control signals and the data bus.

4.3.1 Key and LED Matrices

The keys are electrically arranged in a 8 x 7 matrix as shown in the circuit diagram. The seven columns are scanned by M5; any key contact is detected on one of the eight return lines RL_{0-7}, memorized by M6 and signal KYBDIRQ is passed to the CPU. The CPU responds by interrogating M6 Keyboard memory and acting on the specific key command.

The key LEDs are electrically arranged in an 8×4 matrix. The four rows are scanned by M4, and the eight columns receive the appropriate bit patterns from M6 display memory. This memory is up-dated as required from the CPU data bus D_0-D_7.

4.3.2 Programmable Interface M6

(Fig. 4.3.1)

M6 interfaces the keyboard and LEDs to the instrument data bus. It is addressed by $\overline{KYBDCS}$ from the digital assembly, to chip-select $\overline{CS}$ which enables commands or data to flow via the data bus DB_{0-7}. The CPU sets address A_0 to logic-Ø for data flow; but for programming the interface during initialisation or for mode change, A_0 is set to logic-1.

4.3.2.1 Read/Write Control

The $\overline{WRTSTRB}$ signal from the digital assembly is applied to M6 $\overline{WR}$. Data or Command is input to M6 from the CPU data bus during $\overline{WR}$ low and $\overline{CS}$ low, and is latched on the $\overline{WR}$ positive-going edge. The $\overline{RDSTRB}$ signal from the digital assembly is applied to M6 $\overline{RD}$. Data is output from M6 on to the data bus during $\overline{RD}$ low and $\overline{CS}$ low.

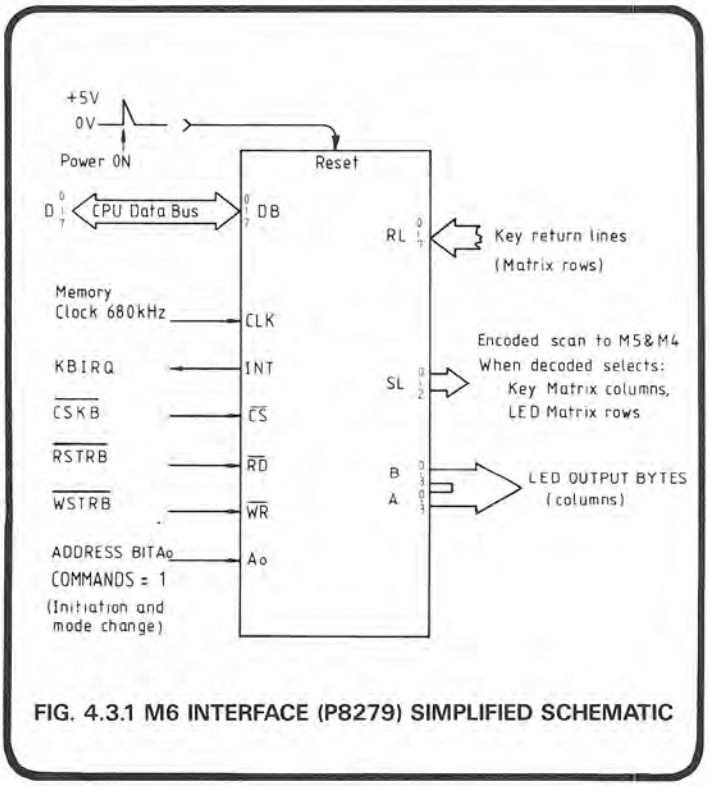


FIG. 4.3.1 M6 INTERFACE (P8279) SIMPLIFIED SCHEMATIC

4.3.2.2 M6 Initialization

When the 4200 is switched on, M6 is cleared by the PWR ON RESET pulse from the digital assembly. The interface is then programmed during initialization as follows:

Clock divider set to 'divide by eight':
The memory clock (E) at approximately 680kHz is divided by 8 to give an internal clock frequency of 85kHz.

An inherent division by 16 reduces the scan clock to 5kHz giving a scan cycling frequency of 333Hz.

Encoded Keyboard Scan:
The scan output from SL_{3-0} is a 4-bit binary count.

SL_3 is not used; SL_{2-1} scans M4, and SL_{2-0} scans M5.

Keyboard Mode:
The internal keyboard RAM is programmed as FIFO, input routed via RL_{7-0} return lines. Two-key lockout is employed with debounce.

Display Mode:
Eight character left entry for the LED display.

Inter-digit blanking: all 1's on B_{0-3} and A_{0-3} between digits.

4.3.2.3 M6 Reprogramming

The Frequency Store and Spot keys, the 12 dual ↑/↓ keys and the Zero key have a reprogrammable function. When one of these keys is pressed, the P8279 is reprogrammed into Scanned Sensor Mode. When released, the P8279 reverts to Encoded Keyboard Scan Mode.

4.3.3 Scan Decoding

The encoded scan output from M6 (approximately 333Hz cycle frequency at SL_{2-0}) is decoded by M5 to energize each key-matrix column line once every scan cycle. SL_{2-1} scan outputs are also decoded by M4 to energize each LED-matrix cathode driver once in every scan cycle for a period of two digits.

4.3.4 Key Selection

The keys are electrically grouped within a matrix of 8 rows of 7 (some positions vacant). This does not conform to their physical grouping on the front panel. The eight return lines RL_{0-7} each define a row in the matrix, whose columns are scanned by M5 (Low active).

In M6, the internally-synchronized keyboard memory stores the state of each of the 48 keys. The use of 2-key lockout rejects two or more simultaneous contacts. Any single key depression is debounced, initiating the interrupt KYBDIRQ to the CPU which then interrogates the keyboard RAM in the P8279. The next action depends upon the Key's function:

'Zero' or '↑/↓' key pressed:

a. M6 is reprogrammed into Scanned — Sensor mode for as long as the key is pressed, the CPU acting on the key information.

b. If an appropriate ↑ key is pressed while 'Zero' is held down, the resolution of the Output display is changed.

c. If a single ↑ or ↓ key is held down for longer than half a second, the display enters 'auto ↑/↓' mode, running at about 3 digits/second.

d. When the key is released, M6 is returned to Encoded Keyboard Scan mode.

'Store' or 'Spot' key pressed:

a. M6 is reprogrammed into Scanned — Sensor mode for as long as the key is pressed, the CPU acting on the key information.

b. If an F1 to F5 key is pressed while 'Store' or 'Spot' is held down, the appropriate frequency memory location is accessed, and the 4200 frequency is reset to the value in the memory.

c. When the key is released, M6 is returned to Encoded Keyboard Scan mode.

Any other key pressed (not Safety Reset):

a. M6 remains in Encoded Scan mode; the scan continues as the CPU is acting on the key information.

b. KYBDIRQ interrupts are generated only by the low-going edges of the key contact pulses, so M6 remains sensitive to subsequent key depressions.

4.3.5 Key LED Operation

After performing the change requested by the key depression, the CPU changes the bit-patterns stored in M6 internal display RAM. As this is scanned internally in synchronism with the decoded outputs of M4, each output byte of B_{0-3} A_{0-3} drives the row of LEDs accessed by M4 output lines.

The bit-pattern of the byte selects the LEDs to be lit in that row:

B_{0-3} A_{0-3} bits high = unlit,
low = lit.

During changes of output from one byte to the next, all B_{0-3} A_{0-3} lines are all set high to avoid spurious LED flashes. Transistors Q25-Q32 drive the LED anodes from a +5V supply regulated by M2, Darlington amplifiers Q21-Q24 driving the LED cathodes.

4.3.6 Audible Warning Buzzer

M48 and M1 act as a control latch for the quartz warning buzzer. With $\overline{\text{ALARM}}$ at logic-1 (+5V) M1 remains unchanged; but with $\overline{\text{ALARM}}$ at logic-Ø (0V) the state of M1 depends on the condition of Ao:

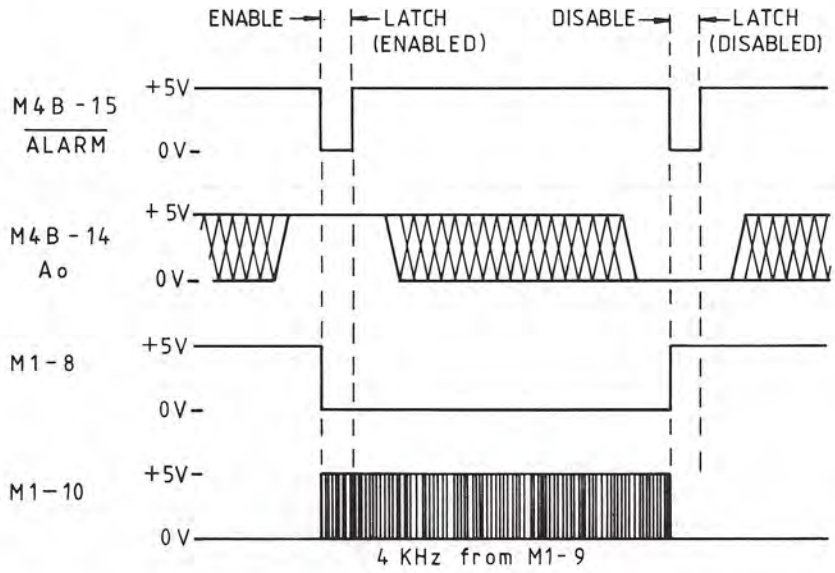
Ao at logic-1: the alarm sounds a 4kHz tone.
Ao at logic-Ø: the alarm is silent.

The latch is operated at CPU speed. Two $\overline{\text{ALARM}}$ pulses are used for each burst of sound. The first, with Ao at logic-1, starts the burst; the second, with Ao at logic-Ø, ends it. The waveforms and truth table in Fig. 4.3.2 illustrate the action of the latch.

During Power ON initialization, the combination of $\overline{\text{ALARM}}$ at logic-Ø, Ao at logic-Ø, is applied to M4B to force power-up in the disabled condition.

The 4kHz tone signal at M1-9 originates in the Precision Divider counter which is situated on the Analog Interface Assembly.
(Refer to Circuit Diagram 430570 Page 7.3-1).

Note that Ao may be used for other purposes when $\overline{\text{ALARM}}$ is at logic-1, but this will not affect the buzzer state.



M4B / M1 TRUTH TABLE

$\overline{E_B}$ ($\overline{\text{ALARM}}$)	A_B (A_o)	$Q0_B$	$Q1_B$	M1 - 8	BUZZER
0	0	1	0	1	DISABLED
0	1	0	1	0	ENABLED
1	X	0	0	NO CHANGE	NO CHANGE

0 = 0V, 1 = +5V, X = either 1 or 0

FIG. 4.3.2 ACTION OF BUZZER CONTROL LATCH

4.4 DIGITAL DISPLAYS

The circuits described in this section perform the following functions:

(1) Storage of display data in a Display Image RAM, updated under CPU control.

(2) Generation of multiplex count which selects segment data from the RAM, and energizes the appropriate digital blocks in synchronism.

(3) Distribution of high voltage supplies to energize the plasma displays.

Part of the Digital assembly (400534) houses the display multiplexer, which includes the display image RAM, the interdigit and multiplex counters, and control circuitry.

The two plasma displays, the block multiplex decoder, segment drivers and high voltage circuits are located on the Front assembly (400533). Fig. 4.4.1 shows the arrangement and main interconnections of the display circuitry.

4.4.1 General
(Fig. 4.4.1)

The purpose of the Display Image RAM is to accept and store current display data, which is read out to drive the display segments. The Display Block Counter generates a 4-bit count at 2kHz which scans the 11 digit-blocks of both displays in parallel. The same count scans the RAM, selecting segment information for each block in turn. As there are two displays, and therefore Two RAM bytes to read for each block, the 'MODE' display data is first entered into a holding latch during the inter-digit blanking period at the start of the time-slot for its block.

To update the displayed characters, the CPU writes into the RAM at high speed (680 kHz), using signal XDDSP to connect the Address bus through the Address Source Switch to the RAM. XDDSP also connects the Data Bus to the RAM through the Data Bus Buffers, writing the new segment data into the selected RAM Address. The high speed of the transfer, compared with the much slower scanning speed in Read mode, avoids spurious effects appearing on the displays.

Each RAM address contains only 8 bits, but there are nine segments in each display block. Comma-segment information is therefore not written into its normal block address in the RAM, but stored as a bit in a separate 'Commas' byte, which holds the data for all eight blocks which have a comma. The byte is read out into a Commas Data Holding Latch, once every block-scan cycle, and then selected for display by a Commas Multiplexer 8-into-1 switch.

4.4.2 Static Conditions
(Circuit Diagram 430533 Page 7.1-2)

The plasma displays are driven from +5V (anode supply) and -175V (cathode supply). The supplies are connected by conduction of anode and cathode driver transistors:

Anodes:
Both Displays – Q10 to Q20,

Cathodes:
MODE Display – Q2 to Q9, and Q41,
OUTPUT Display – Q33 to Q40, and Q42.

When not energized, all anodes and cathodes are held at –70V by the action of 75V zener D17.

To energize a particular block, (on both displays simultaneously), the multiplex decoder causes the relevant anode driver transistor to conduct, and lift its two anodes to +5V.

At the same time the two sets of data, for the characters to be displayed in the two blocks, are extracted from the Display Image RAM and applied to the segment cathode drivers. Those segments selected for illumination are pulled to –175V, striking the discharge.

Four keep-alive electrodes in each digit block, two anodes and two cathodes, are maintained at voltages of +5V and –175V respectively. This ensures a rapid strike when a digit is energized, and helps to prevent inter-block 'streaming'.

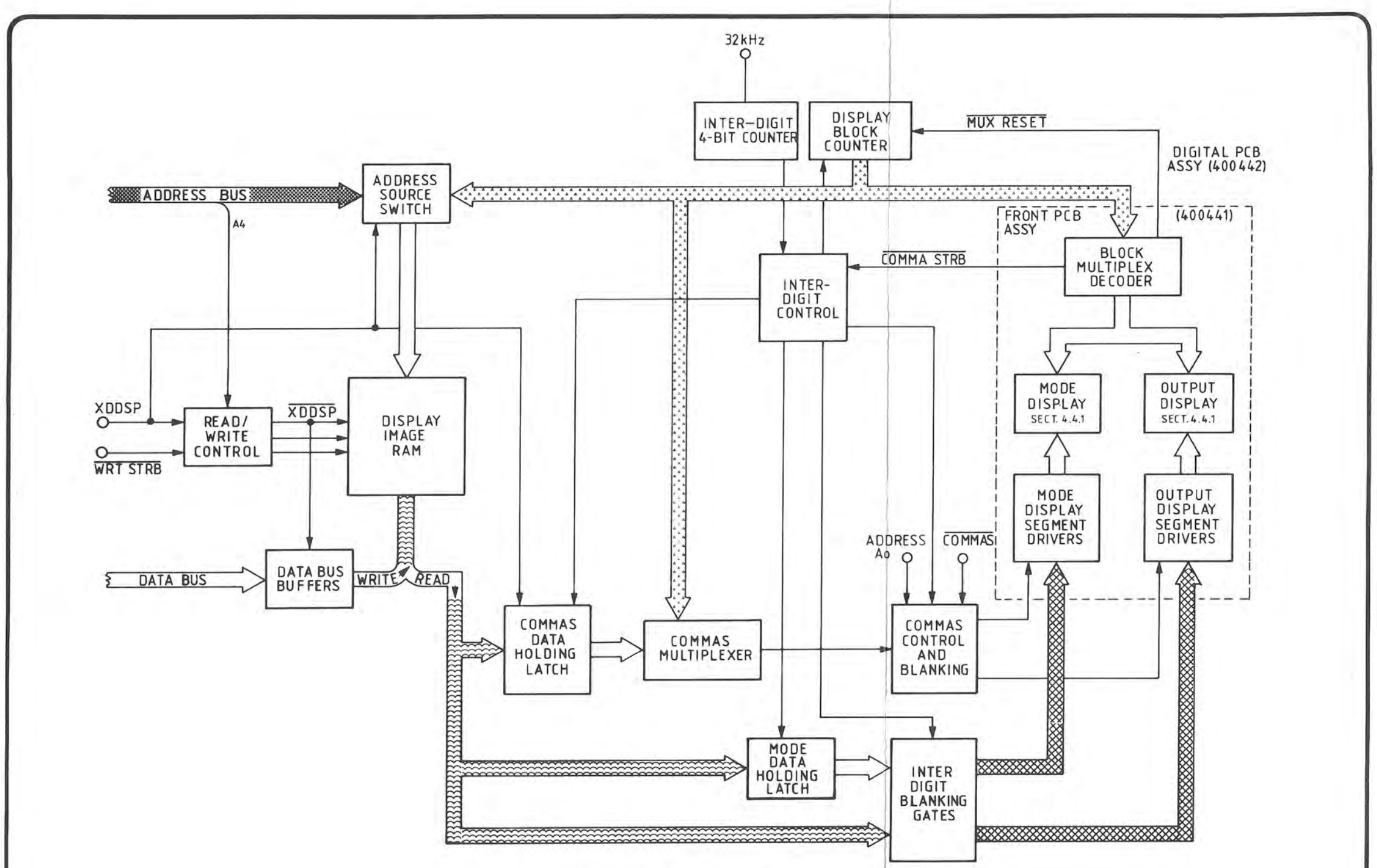


FIG. 4.4.1 MODE AND OUTPUT DISPLAYS—FUNCTIONAL BLOCK DIAGRAM

4.4.3 Write Mode
(Fig. 4.4.2)

Whenever the CPU is programmed to update a display (e.g. Range, Function, Mode or Value change) it sets address decode XDDSP to logic-1 with each byte of data to be transferred. This causes M31 and M33 to select the CPU address lines A_{4-0} which are mapped directly to the RAM address input lines A_{4-0}. The RAM is placed into its write mode by signal XDDSP at logic-Ø (M17-8, TP5, M16-16).

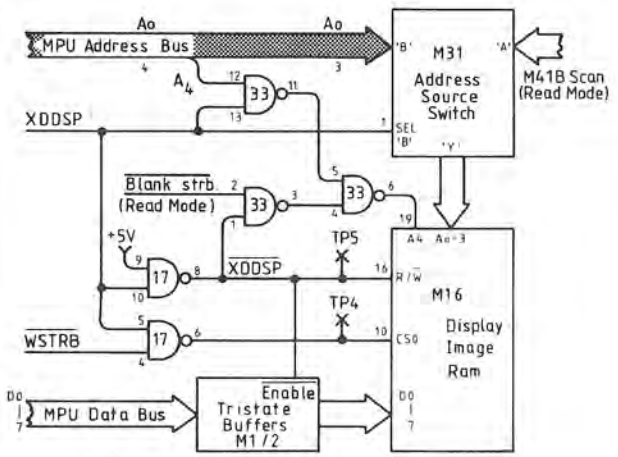


FIG. 4.4.2 RAM ACCESS—WRITE MODE LOGIC

The RAM M16 is divided into two sections, using the address bit A_4 to differentiate between OUTPUT and MODE Display images. When the CPU is loading the RAM with OUTPUT Display data, it sets A_4 to logic-1, translating to set M16-19 (A4) input to logic-1. MODE Display and COMMAS images are written into M16 with A4 at Logic-Ø (M33-4 and 13 at Logic-1 in write mode).

(In Read mode M16-19 is again used to differentiate between the two image sections).

The signal $\overline{\text{XDDSP}}$ (M17-8) enables the tri-state buffers M1 and M2, connecting the CPU data bus to M16 data input/output lines D_{0-7}. The CPU also generates the write strobe signal $\overline{\text{WRTSTRB}}$ with each byte of display data. This is combined with XDDSP (M17-6, M16-10, TP4) to enable M16 internal Input/Output tri-state buffers to accept the data byte (chip select CS_0). Once the display data has been loaded into the RAM, the CPU returns XDDSP to logic-Ø and the RAM reverts to Read mode.

4.4.4 Read Mode
(Fig. 4.4.3)

Unless the CPU has data to update, the signal XDDSP remains at logic-Ø, to hold the display multiplexer circuitry in Read mode. The RAM data bus is isolated from the CPU data bus by tri-state buffers M1/M2, and M16 is chip-selected in read mode by M17-6 and M17-8 at logic-1.

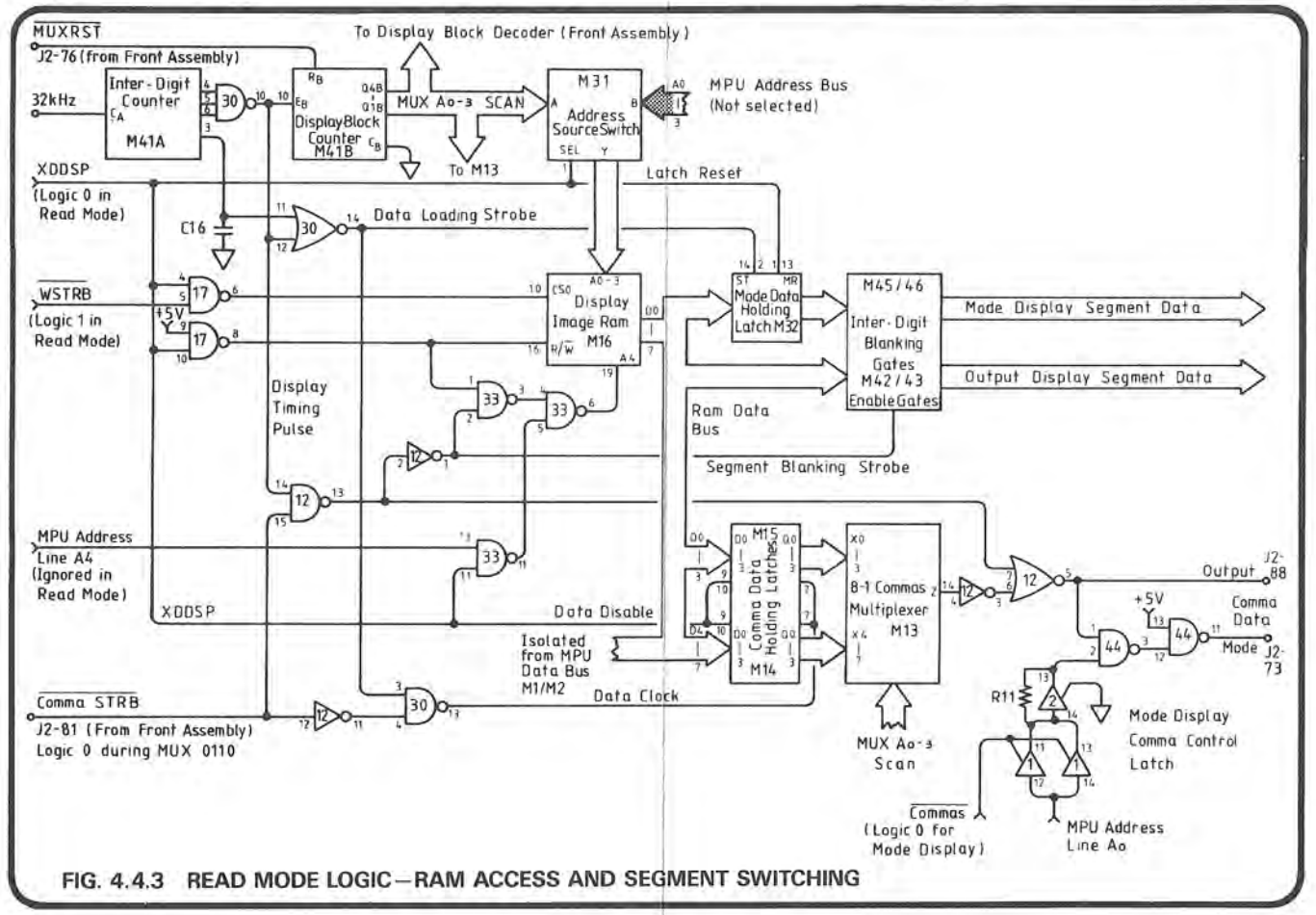


FIG. 4.4.3 READ MODE LOGIC—RAM ACCESS AND SEGMENT SWITCHING

4.4.4.1 Display Scan Address Interlacing
(Figs. 4.4.3 and 4.4.4)

M31-1 (SEL) at logic-Ø causes the RAM to be addressed from the display block scan, mapping M41B outputs: Q4B, Q3B, Q2B, Q1B to RAM address input lines: A_0, A_3, A_2, A_1 respectively. This bit-rotation interlaces the extraction of display data, in synchronism with the interlaced block selection by the Front Assembly Scan decoder.

4.4.4.2 Block Multiplex Decoding
(Circuit Diagram 430533 page 7.1-2)

The 4-bit Block scan output MUX A_{3-0} from the multiplex scan counter M41B (dig) is used at $DATA_{4-1}$ input to M3, which decodes it into a low-active 16-line scan S_{15-0}.

M3 output S_6 generates the comma strobe signal $\overline{\text{COMMA STRB}}$, S_{13} terminates each scan by resetting M41B (dig) ($\overline{\text{MUX RESET}}$), and S_7, S_{14} and S_{15} are not used.

The other eleven outputs from M3 switch Q10-Q20 on sequentially, to drive the anodes of both plasma displays in synchronism. As can be seen from Fig. 4.4.4, the interlace is maintained to avoid consecutive activation of adjacent blocks, thus preventing inter-block 'streaming'.

MUX A_{3-0} SCAN				M3 (Front Assy.)	
A_3	A_2	A_1	A_0	M3 Output (Low Active)	Energised Line (Both displays' Anodes and Signals)
M_3 D_4	$DATA_{4-1}$ Input D_3	D_2	D_1		
M_{16} (Dig Assy) Display Image RAM) A_{3-0} Input					
A_0	A_3	A_2	A_1		
0	0	0	0	S_0	A_1
0	0	0	1	S_1	A_3
0	0	1	0	S_2	A_5
0	0	1	1	S_3	A7
0	1	0	0	S_4	A_9
0	1	0	1	S_5	A_{11}
0	1	1	0	S_6	$\overline{\text{COMMA STRB}}$
0	1	1	1	S_7	Not used
1	0	0	0	S_8	A_2
1	0	0	1	S_9	A_4
1	0	1	0	S_{10}	A_6
1	0	1	1	S_{11}	A_8
1	1	0	0	S_{12}	A_{10}
1	1	0	1	S_{13}	$\overline{\text{MUX RESET}}$
1	1	1	0	S_{14}	Not included in cycle ($\overline{\text{MUX RESET}}$ at S_{13})
1	1	1	1	S_{15}	

FIG. 4.4.4 DISPLAY SCAN ENERGISING SEQUENCE

4.4.4.3 OUTPUT And MODE Display Data Selection

When the processor writes display data into the Display Image RAM, the A_4 input is used to select the MODE or OUTPUT Display data storage area (see para 4.4.3 and Fig. 4.4.4). In Read mode also, A_4 is set to logic-1 to read OUTPUT Display data, and to logic-Ø for MODE or COMMA data.

For an alpha-numeric display block, 18 bits of data could be required:

One byte for the OUTPUT Display block segments;
One byte for the MODE Display block segments;
Two bits for COMMAS (one for each display).

The problem of transferring two bytes of data along the single-byte RAM data bus is overcome by strobing each MODE display segment byte into a holding latch (M32), during the first 30μs of its block selection time-slot. The MODE display section of the RAM is selected by setting its A_4 input to Logic-Ø for this 'Inter-digit' period, during which the inter-digit blanking gates (M42/43, M45/46) set all segment lines to the Front Assembly to logic-Ø (segments OFF).

COMMAS data are stored as a separate byte as described in Section 4.4.4.6.

4.4.4.4 Display Timing (Fig. 4.4.5)

Read mode is driven by a 32kHz square wave (Waveform 'A', generated from the 13-bit counter in the Analog Interface Assembly M15-11), used as clock for a 4-bit counter (M41A). The three most significant bits are combined at M30-10 to produce Waveform B, the display master-timing pulse, used also for Inter-digit blanking.

The following example explains how the display data is set up for the next display block in sequence, during the 62.5μs of the display timing pulse.

EXAMPLE

Initial State:
M41B count has already reached 1001, and the block 4 anodes of both displays are energized (Fig. 4.4.4).

The OUTPUT Display data for block 4 is selected in the Display Image RAM (M16) to drive the segment cathodes for a figure '6', which appears on the OUTPUT Display.

Block 4 of the MODE Display is showing a figure '3', and the data for this is being output from the Mode display holding latch (M32).

The data held in M16 for the next byte (Block 6 of both displays) is:

OUTPUT Display — Figure '8'
MODE Display — Figure '7'

Block Changeover:
The next block is selected during the display master timing pulse (Fig. 4.4.5, Waveform B).

a. The negative-going leading edge triggers the scan counter (M41B) whose output advances to 1010 (block 6). On the Front Assembly, M3 de-energizes A_4 anodes and energizes A_6 anodes.

b. For the duration of the display master timing pulse (Logic-Ø at M12-14), the A_4 input to M16 is set to Logic-Ø as A_{3-0} inputs are advanced to 0101. Mode display data for figure '7' is loaded onto the RAM data bus as follows:

i) M17-6 at Logic-1 chip-selects M16 at M16-10,

ii) M17-8 at logic-1 holds M16 in Read mode,

iii) RAM address A_{4-0} = 00101 reads block 6 MODE Display data onto the RAM data bus (M1/M2 isolates from the CPU data bus),

iv) M30-14 at logic-1 strobes the byte into M32 during the 30μs of Waveform D, then returns to logic-Ø leaving figure '7' data latched at M32 output.

v) M12-1 at logic-Ø blanks the two displays by setting M45/M46/M42/M43 outputs to logic-Ø, regardless of their inputs from M32 and the RAM data bus.

c. The positive-going edge of Waveform 8 lifts the RAM A_4 input (M16-19) to logic-1, addressing the OUTPUT Display section of memory. A_{3-0} is still at 0101, selecting block 6 display data (in our example a figure '8') which it loads on to the RAM data bus.

The end of the master timing pulse also releases the blanking by enabling the gates M42/M43/M45/M46, so the data for both MODE and OUTPUT Displays are now delivered to the cathode drivers on the Front Assembly, to strike the gas discharge in the two energized A_6 blocks.

This condition persists for 437.5μs until the next master timing pulse, when Waveforms B and C repeat the process for the next block of stored display data.

At any time during the cycle, the CPU may force Write mode. This will not disturb the scan from M41B, but XDDSP will reset M32 outputs to logic-Ø (M32-1/13). However, the speed of byte transfer from the CPU ensures that transferring data is not visible on the displays. Subsequently, each block will be driven by its new stored data.

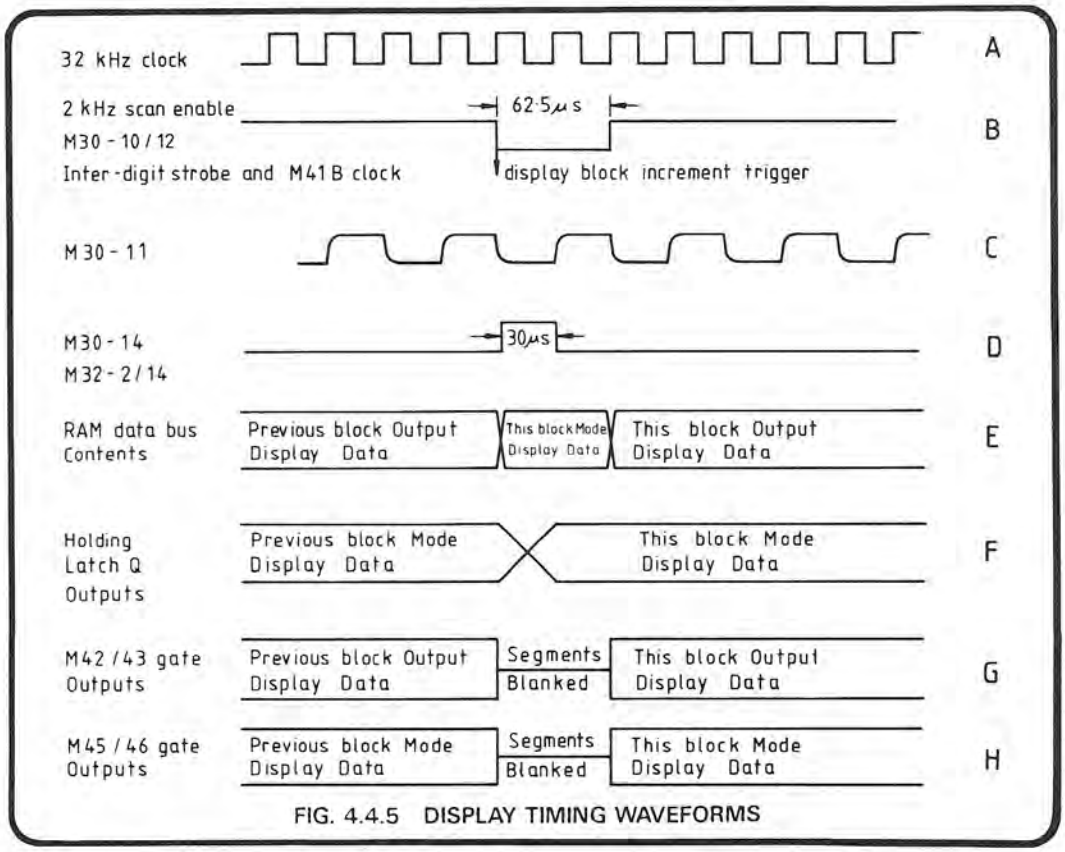


FIG. 4.4.5 DISPLAY TIMING WAVEFORMS

4.4.4.5 Display Segment Drive

(Circuit Diagram 430533 Page 7.1-2)

The strobed segment signals from the Digital Assembly are input to the Front Assembly on J1-67 to J1-75 (MODE Display) and J1-82 to J1-90 (OUTPUT Display). These are already synchronized to their blocks by the 4-bit block scan MUX A_{3-0} within the Digital assembly.

For each block in sequence, the appropriate segment bit-pattern is set at the input to the segment drivers. For bits at logic-1, the rise is passed through line capacitors to reverse-bias DC restoration diodes and forward bias their driver - transistor bases. The resultant collector currents pull the segment cathodes from their quiescent −70V, to −170V. The correct block anode is simultaneously lifted from −70V to +5V by its anode driver transistors, striking the gas discharge and displaying its digit. For bits at logic-Ø the cathode drivers remain cut off.

The driver emitter resistors control the segment cathode currents for uniform brilliance.

During change-over between blocks, all segment inputs at logic-1 are returned to logic-Ø by the inter-digit blanking strobes M42/43/45/46 (dig). This turns off the drive transistors and blanks the display. The high scan frequency and persistence of the operator's vision prevent the blanking being observed on the display.

4.4.4.6 Comma Logic

(Fig. 4.4.6)
(Circuit Diagram 430534 Page 7.2-1)

The comma is the ninth segment (i) in each of the numerical display blocks. It cannot fit into a block's byte in memory, as there are only eight bits per byte. But all the comma information can be stored in a single byte of memory in the RAM (RAM address 01100). This is possible although there are nine numerical blocks, because the ninth block never requires a comma. Legend blocks A_{10} and A_{11} do not have a segment (i).

The RAM COMMA data is updated by the CPU in Write mode, and is read out (as though it were another display block) by M41B scan 0110 during the master display pulse (Waveform B sets RAM A_4 input to logic-Ø). The same MUX combination 0110 selects S_6 output from M3 decoder on the Front Assembly, which sets the signal $\overline{\text{COMMA STRB}}$ to logic-Ø.

Thus for the duration of $S_{6=0}$ (500μs), the COMMA data is on the RAM data bus, but the blanking gates prevent it reaching segments (a)-(h).

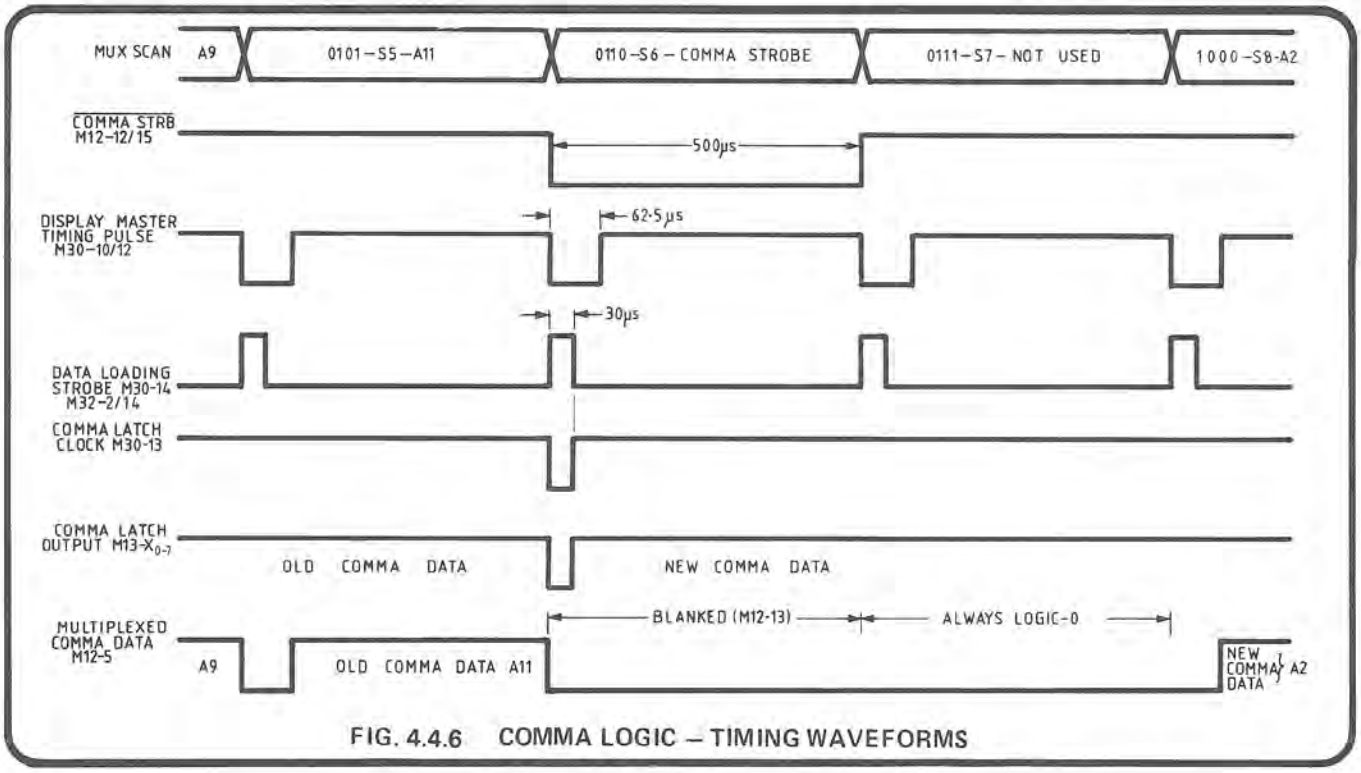


FIG. 4.4.6 COMMA LOGIC – TIMING WAVEFORMS

4.4.4.7 Comma Drive Multiplexing

Signal $\overline{\text{COMMA STRB}}$ is inverted and combined with the Data Loading Strobe at M30-13 as a logic-0 pulse, whose positive-going edge clocks the comma data into latches M14/15, approximately 30μsec after it has been loaded on to the RAM data bus. The permanently-enabled outputs from these latches are input as X_{0-7} into the 8-into-1 multiplexer M13 for a complete MUX scan until the next $\overline{\text{COMMA STRB}}$ signal.

The block-multiplex scan from M41B selects the correct X input to synchronize with activation of its display block anode. This is output from M13-14(Z), into blanking gates M12.

Comma information is blanked during $\overline{\text{COMMA STRB}}$ and by inter-digit blanking during display-block change-over (M12-7).

The Comma drive line from M12-5 to the front panel via J2-88, controls segment (i) cathode driver for the OUTPUT Display.

If commas are required on the MODE Display (e.g. in 'Spec' operating mode +Lim or −Lim) they will always be in the same display blocks as the OUTPUT Display. When this mode is selected, the CPU pulses the $\overline{\text{COMMAS}}$ line to logic-Ø at the same time as Address line A_0 goes to logic-1. Tristate buffer outputs M1-11 and 13 go to +5V, setting M2-13 output to +5V (logic-1). Outputs M1-13 and M1-11 go tristate when the $\overline{\text{COMMAS}}$ line returns to logic-1, leaving M2-13 latched to +5V by the positive feedback action of R11. So M44-2 enables the comma data to the MODE Display segment driver via J2-73 to copy the OUTPUT Display commas on to the MODE Display.

When Mode display commas are not required, A_0 is set to logic-Ø (0V) with $\overline{\text{COMMAS}}$ signal at logic-Ø. Thus M2-13 latches to logic-Ø and M44-2 disables the flow of comma data to the Mode display.

4.5 ANALOG CONTROL INTERFACE

The circuitry described in this section performs the following functions:

(1) Provides a two-way interface via a serial data link between out-guard digital processing and in-guard analog control circuitry on the reference divider pcb. (See Fig. 4.5.1).

(2) Monitors the CPU operation, serial transfer, digital supply failure and restart operations (watchdog), imposing a controlled safety default condition if there is a danger of losing digital control of the analog functions.

A manual reset of the safety monitor is provided on the front panel. (See Fig. 4.5.4).

4.5.1 General

Safety and Control information is input from Digital (400534) and Front (400533) Assemblies to out-guard circuits located on the Analog Interface Assembly (400570), processed and transferred across the 'Guard' isolation barrier to in-guard circuits in the Reference Divider Assembly (400535). After further processing in the Reference Divider Assembly, safety and control information is output to the following assemblies:

Sine Source Assembly (400446),
AC Assembly (400447),
PA Assembly (400450),
Output Control Assembly (400550),
Current Assembly (400555), and
High Voltage Assembly (400565).

Certain selected 'Status' signals, originating in the analog assemblies, are returned to the CPU during the data transfer. Thus, the data link forms a continuous loop, as shown in Fig. 4.5.1.

4.5.2 Serial Data Transfer (Fig. 4.5.1)

(Circuit Diagrams: 430534 Page 7.2-2, 430570 Page 7.3-3, 430535 Page 7.4-4 and Page 7.5-5)

A bi-directional serial data link passes information across the guard isolation screen; conveying CPU instructions to control the in-guard analog circuitry, and transferring critical status signals from the guarded circuits back to the CPU.

The link is managed by a synchronous serial data adapter (SSDA) which, having first been loaded with three bytes of control instructions by the microprocessor; transmits the resultant 24-bit word across guard one bit at a time, via its Tx DATA channel.

The 48 bits necessary to control the analog circuitry thus require two successive 24-bit transmissions.

Simultaneously with each 24-bit transmission, the SSDA receives a 24-bit word via its Rx DATA channel, enabling the CPU to obtain the status of the analog functions.

4.5.2.1 The Transfer Cycle (Fig. 4.5.1)

The CPU uses an address-code signal $\overline{\text{AN I/F STRT}}$ (Analog Interface Start) to initiate each 24-bit shift, by triggering a separate clock generator (M2, M3, M4) which produces a burst of 24 clocks per shift. Data is clocked in a serial string through a continuous loop comprising:

the 48-bit, serial in/parallel out, analog control shift register;

the 16-bit, parallel in/serial out, status shift register;

back to the SSDA receiver (Rx DATA).

The serial data string is correctly located after two 24-bit shifts, so then the SSDA generates a strobe pulse which:

(1) Transfers the data present in the serial data string of the six 8-bit analog-control shift registers (M27, M25, M31, M19, M30, M15) into their enabled parallel output registers and onto the analog control bus.

When the strobe ends, further transfer is disabled and the registers' output data is latched.

(2) Injects the status data at each of the parallel inputs of the two 8-bit status shift registers (M18, M22) into corresponding locations in the serial data string.

When the strobe ends, the parallel inputs to the status registers are disabled.

After the strobe pulse, the CPU initiates a further circulation of serial data (including the status data), in order to obtain the status data and return the analog control bits to the SSDA Rx DATA register for parity checking by the CPU.

This extra (confirmatory) circulation requires three more 24-bit shifts, so a complete data transfer consists of five shifts. If no error is detected, the SSDA provides a trigger-enable to allow updates to prevent activation (BARK) of the watchdog circuits.

If an error is detected on the first transfer, the CPU activates a second complete transfer, and then a third if an error is detected on the second. If the error persists after the third transfer, the trigger-enable is withheld, and the instrument will shut-down under the control of the watchdog safety monitor.

All interfacing between out-guard and in-guard circuits is achieved using electrically-isolating opto-couplers.

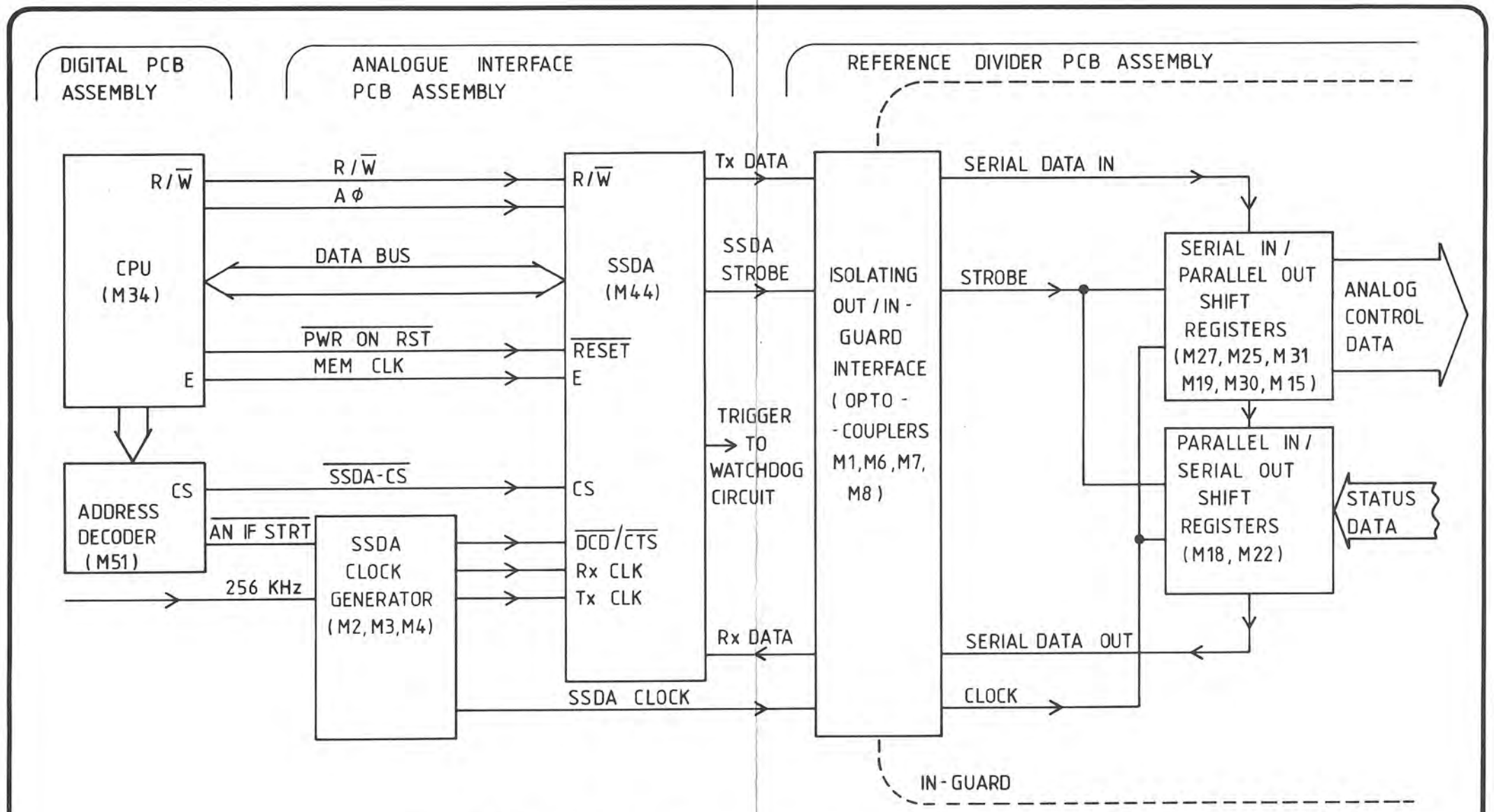


FIG. 4.5.1 SERIAL DATA LINK—SIMPLIFIED FUNCTIONAL BLOCK DIAGRAM

4.5.2.2 Data Transfer Organisation
(Fig. 4.5.2)

Data is transferred serially via the SSDA, control registers and status registers as directed by the CPU.

The exchange of data between the CPU and SSDA is made on the 8-bit instrument data bus, each exchange comprising three bytes (24 bits) of parallel data.

The shifts of serial data through the in-guard circuit are synchronized by clocks which are controlled from the CPU, and the SSDA Rx return registers are cleared when read by the CPU.

Once the in-guard serial data is correctly positioned at the inputs to the control registers, the SSDA generates a strobe which enables its transfer to the parallel outputs of the control registers. The same strobe enables injection of the data on the parallel inputs of the status registers into the serial data string.

The transfer operation requries five serial data shifts, each of three bytes, through the registers. During this operation: the control registers are loaded with bytes of new data (ND); the status registers are loaded with new status data (NS); and the whole of the ND and NS data is returned to the CPU, which:

a. verifies that the analog control bits of the serial data string return to the SSDA Rx DATA register without error. This confirmation indicates that at least, the correct bit pattern was applied to the analog control register inputs at the time the strobe was generated.

and

b. acts upon the status data received.

4.5.2.3 Transfer Sequence

The sequence of events in the transfer operation is as follows, refer to Fig. 4.5.2:

(A) Three bytes of new data, ND1, 2 and 3 are loaded into the SSDA transmitter registers; this data is destined for control registers D1, 2 and 3. The SSDA receiver registers were cleared when last read by the CPU.

(B) A burst of 24 clock pulses, initiated by the CPU, shifts all data three bytes to the right. After the shift is completed, the transmitter registers are loaded with new data bytes ND4, 5 and 6 (destined for control registers D4, 5 and 6). During this period, no transfers are made between the serial data string and the parallel control or status registers.

(C) A second burst of 24 clock pulses again shifts all data three bytes to the right. New data bytes ND1 to 6 are now correctly positioned in control registers D1-D6. After completion of the shift, three dummy bytes are loaded into the transmitter registers. Old data (OD) in the receiver register is ignored.

(D) With new data bytes ND1 to 6 correctly located, the SSDA generates a strobe pulse. This pulse:

(1) latches the 48 bits of bytes ND1 to 6 at the parallel outputs of control registers D1 to 6;

(2) enables the parallel inputs of status registers S1 and 2, loading two new status bytes NS1 and 2 and clearing old data OD5 and 6 from the registers.

(E) A third burst of 24 clocks again shifts all data three bytes to the right. The CPU reads bytes NS1, NS2 and ND1 from the SSDA receiver registers (the CPU may take immediate action on NS returns). After the shift is complete, new data bytes ND1, 2 and 3 are re-loaded into the transmitter registers.

(F) A fourth burst of 24 clocks again shifts all data three bytes to the right. The CPU reads bytes ND2, 3 and 4 from the receiver registers. After the shift is complete, new data bytes ND4, 5 and 6 are re-loaded into the transmitter registers.

(G) A fifth burst of 24 clocks again shifts all data three bytes to the right. Bytes ND5 and 6 are read from the receiver registers. The CPU has now read all new data and status bytes and the transfer sequence ends. If an error is detected between new data transmitted and new data received, the transfer process is repeated; three attempts are allowed before a fault condition is declared.

4.5.3 Synchronous Serial Data Adaptor
(Circuit Diagram 430570 Page 7.3-5)

4.5.3.1 SSDA Initialization

When power supplies are first switched on or an external reset EXT RST is applied, the signal $\overline{\text{PWR ON RST}}$ (Power On Reset) is held at logic-Ø for approximately 8ms.

During this period, the SSDA is latched in a reset condition to prevent erroneous output transitions at its Tx and Rx interfaces; the internal transmit registers are inhibited to prevent the loading of data from the data bus and the SSDA strobe output is held at logic-1.

After $\overline{\text{PWR ON RST}}$ returns to logic-1; the latches, registers and SSDA strobe are cleared in software, during the initialization routine.

4.5.3.2 Parallel Data Input From CPU

The conditions for parallel data on the data bus to be accepted by the SSDA are as follows:

(1) Chip-select $\overline{\text{SSDA CS}}$ at logic-Ø.

(2) Read/Write command R/$\overline{\text{W}}$ at logic-Ø. This controls the direction of data flow via the Data Bus through the SSDA input/output port. When R/$\overline{\text{W}}$ is at logic-Ø, data on the Data Bus is written into a selected register within the SSDA.

(3) The memory clock 'MEMCLK' 682.6kHz square wave is present to synchronize the SSDA operating cycle to that of the CPU.

With input conditions present as above and register address bit Ao at logic-1, the SSDA accepts data from the data bus into an internal 3-byte FIFO register. This data is entered over several MEMCLK cycles and stored in the FIFO register in readiness for serial transmission from the SSDA.

Software programming of the SSDA is performed when the address bit Ao is at logic-Ø. For details of 'Control Byte' operation, refer to Motorola 6852 data sheet.

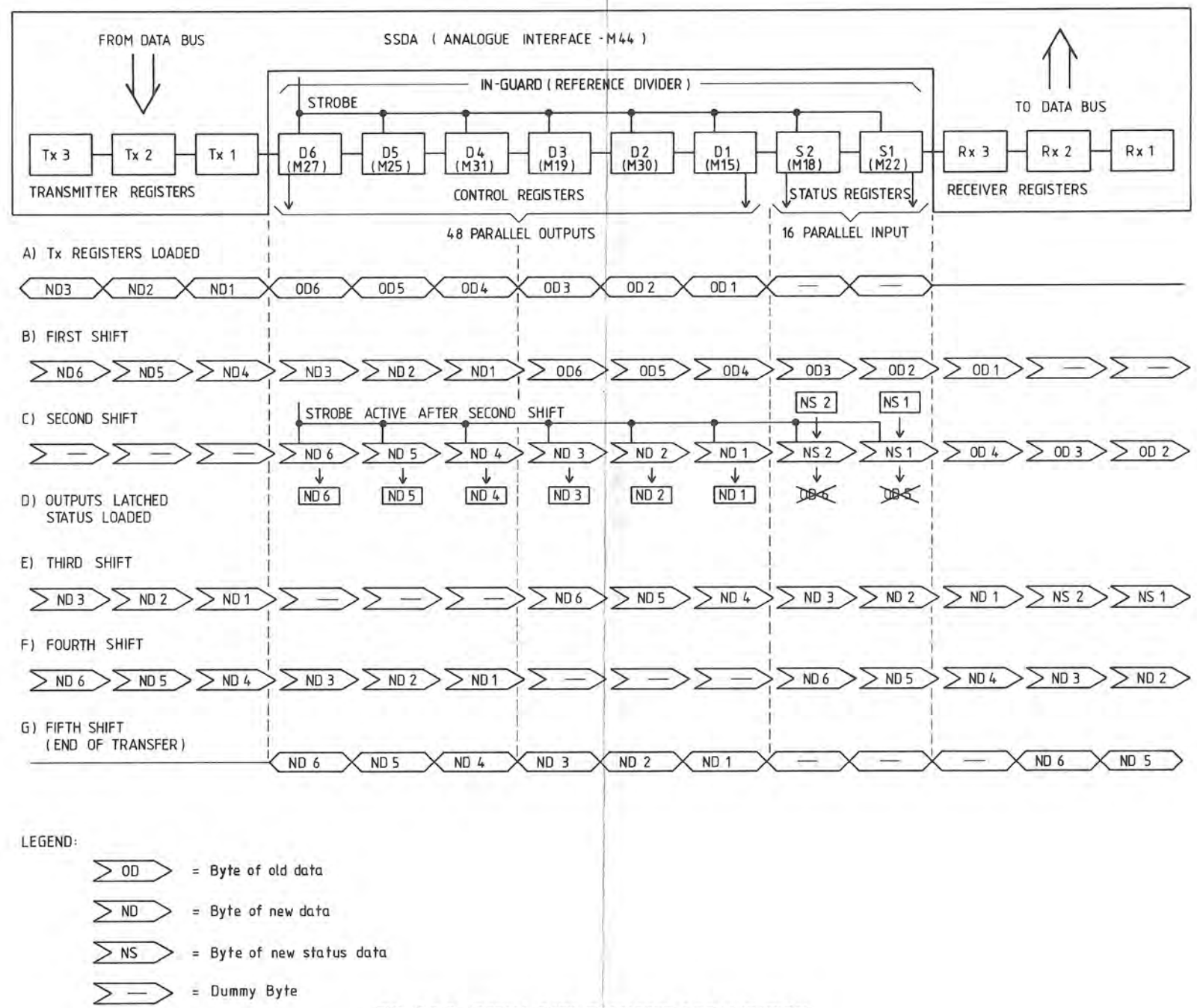


FIG. 4.5.2 SERIAL DATA TRANSFER ORGANIZATION

4.5.3.3 Parallel Data Output to CPU

The conditions for data to be read back from the SSDA on to the data bus are as follows:

(1) Chip-select $\overline{\text{SSDA CS}}$ at logic-Ø.

(2) Read/Write command R/$\overline{\text{W}}$ at Logic-1.

(3) Memory clock, MEM CLK, present.

The data read from the SSDA may be from one of two sources, selection being made by address bit Ao:

With Ao at logic-1, received data from the serial data input FIFO is transferred to the data bus.

With Ao at logic-Ø, the CPU reads an internal SSDA status register.

4.5.3.4 Serial Data Transmission

Serial data transmission is controlled by the $\overline{\text{CTS}}$ (clear to send) input to the SSDA. Transmission is inhibited by $\overline{\text{CTS}}$ at logic-1, and enabled when $\overline{\text{CTS}}$ is set to logic-Ø by the CPU address-code signal $\overline{\text{AN I/F STRT}}$. The first serial bit is transmitted by the negative transition of the first full positive Tx clock pulse (256 kHz) after $\overline{\text{CTS}}$ has been set to logic-Ø. $\overline{\text{CTS}}$ is held at logic-Ø by the $\overline{\text{AN I/F STRT}}$ latch for the duration of 24 full Tx clock pulses, thus enabling the serial shift transmission of the 24 data bits from the Tx Data FIFO in the SSDA.

4.5.3.5 Serial Data Reception

Serial data is received by the SSDA, controlled by the $\overline{\text{DCD}}$ (data carrier detect) level and clocked by Rx CLOCK. $\overline{\text{DCD}}$ is common to the transmit control $\overline{\text{CTS}}$ so that transmission to, and reception from the serial/parallel shift registers is synchronous. Both Rx CLOCK and Tx CLOCK have the same frequency but Rx CLOCK is inverted with respect to the latter. The first bit arriving at its Rx DATA input is clocked into the SSDA Receive FIFO register on the positive transition of the first full Rx clock after $\overline{\text{DCD}}$ is set to logic-Ø.

4.5.4 SSDA Clock Generation

Serial data is transmitted and received in bursts of 24 data bits. Three clocks are used to time the flow of bits, ensuring that:

(1) Data has time to settle before being clocked along the shift registers.

(2) The first Rx data sample is taken before it is lost by the first bit-shift.

(3) Subsequent Rx data has time to settle before being sampled by the SSDA.

(4) Exactly 24 bits are shifted in each burst.

4.5.4.1 SSDA, Tx and Rx Clock Action
(Fig. 4.5.3)

The three clocks are derived from the 256 kHz square wave output from the 13-bit counter (Circuit Diagram 430570 Page 7.3-2). The 256 kHz squarewave is used directly as 'Tx clock' into the SSDA. The negative transition of the first full positive pulse after $\overline{\text{CTS}}$ is set to logic-Ø; triggers the first serial Tx data bit setup (Refer to Fig. 4.5.3 Waveforms G and H).

'Rx clock' is an inverted version of the 256 kHz squarewave. The positive transition of the first full Rx clock cycle, after $\overline{\text{DCD}}$ is set to logic-Ø; triggers the SSDA to sample the first Rx data bit before the first SSDA clock has triggered the shift registers. (Refer to Fig. 4.5.3 Waveforms K and J).

'SSDA clock' is also an inverted version of the 256 kHz squarewave. The inversion allows approximately 2ms of data setup time for all serial data bits prior to clocking the data along the shift registers. SSDA clock is gated at M2-3 by the action of M3-12 to ensure that the first Rx data is sampled before it is lost by the first bit-shift. 24 SSDA clock pulses are counted by M4, allowing 24 bits to be shifted before resetting the Analog Interface Start latch M2-11 (TP3) to logic-1. (Refer to Fig. 4.5.3 Waveform I).

4.5.4.2 SSDA Clock Circuitry
(Circuit Diagram 430570 Page 7.3-3)

The following paragraphs describe the action of the SSDA clock generator circuitry.

The action of the SSDA clock generator is initiated by the command $\overline{\text{AN I/F STRT}}$ from the CPU. This occurs after the parallel data has been loaded into the SSDA transmit registers from the data bus. The logic-Ø pulse of $\overline{\text{AN I/F STRT}}$ sets flip-flop M2-10/11 to give a logic-Ø at TP3 which then:

(1) Sets the D input level of flip-flop M3-5;

(2) Removes 'set' to enable shift register M3 at M3-6 and M3-8;

(3) Removes 'reset' to enable counters M4 at M4-7 and M4-15.
(Refer to Fig. 4.5.3 Waveforms A and C).

At the next rising edge of the inverted 256 kHz (Rx clock) from M43-8 after $\overline{\text{AN I/F STRT}}$, the shift register M3 is clocked but only M3-1 'Q' output changes state to logic-Ø. This is applied to the SSDA $\overline{\text{CTS}}$ and $\overline{\text{DCD}}$ inputs, thus releasing the inhibits on the SSDA transmit and receive registers.

(Refer to Fig. 4.5.3 Waveforms D and E).

At the next (second) rising edge of the clock to M3, M3-12 changes to logic-1. This allows NAND M2-3 to pass 256 kHz clock pulses via buffer M5-12 to the Reference Divider Assembly as the clock which shifts the serial data string along the analog-control and status registers.
(Refer to Fig. 4.5.3 Waveforms D, F and I).

The 256 kHz clock at NAND M2-3 is applied to the 4-bit up-counter clock input at M4-1, each rising edge causing the counter to increment by 1.

The divide-by-16 output M4-6 is applied to the enable input at M4-10; the falling edge of this output occurs at count-16 and increments the second counter to give, at M4-11, a logic-1 output. At count-24, M4-6 changes again to logic-1, and together with M4-11 output, gives a logic-Ø from NAND M2-4, causing the following actions:

(1) Flip-flop M2-12 is reset to give logic-1 at TP3.

(2) The logic-1 at TP3 sets shift register M3 to give:

a. logic-1 at M3-1, thus inhibiting $\overline{DCD}$ and $\overline{CTS}$;

b. logic-Ø at M3-12, disabling NAND M2-3 and thus stopping any further SSDA clocks.

(3) The logic-1 at TP3 resets the up-counters M4 causing:

a. the counter outputs to fall to logic-Ø, inhibiting further counting;

b. NAND M2-5 to rise to logic-1, re-setting flip-flop M2-12 to prepare for the next $\overline{AN\ I/F\ STRT}$ input.

(Refer to Fig. 4.5.3 Waveforms I, B, C, E and F).

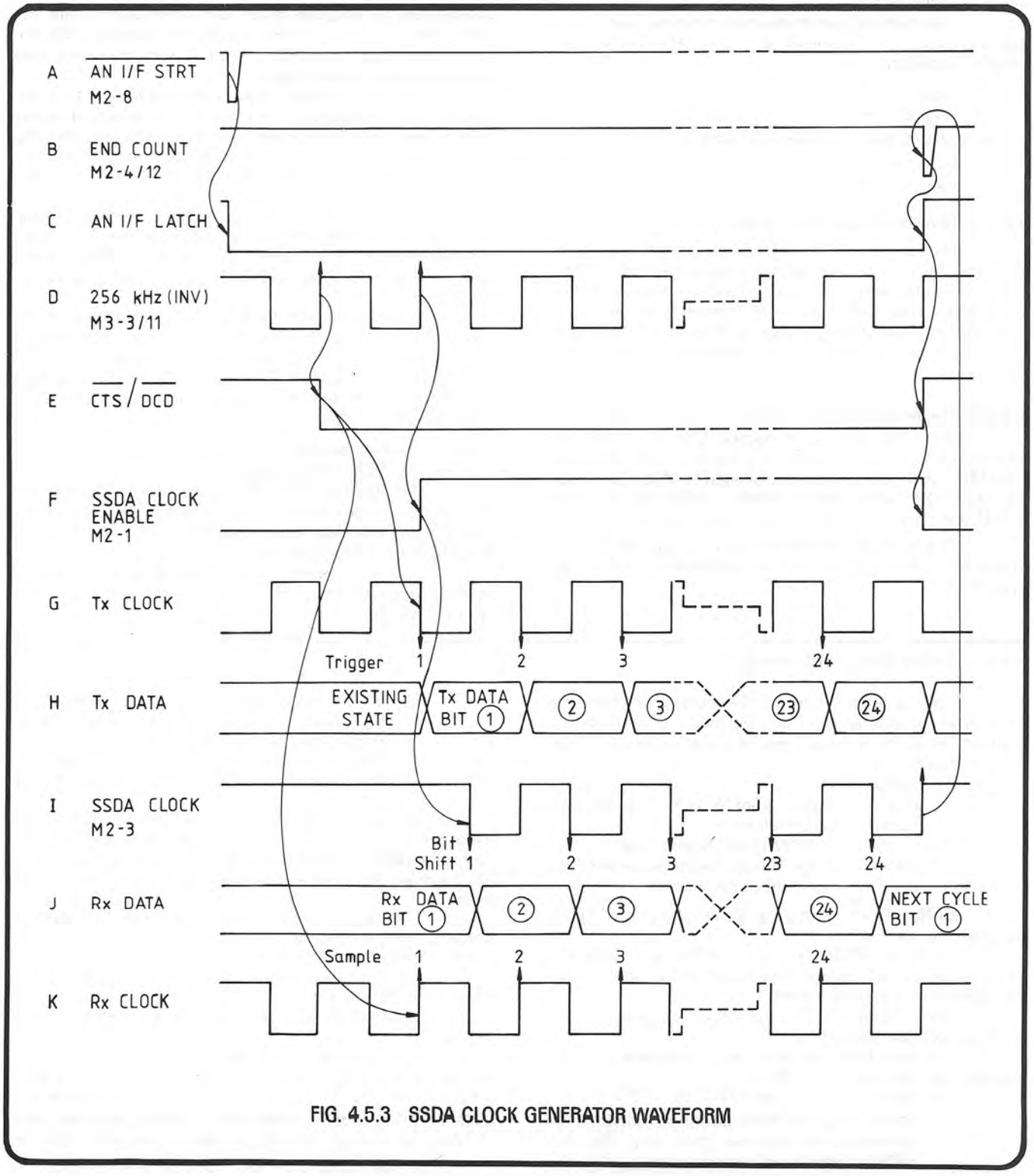


FIG. 4.5.3 SSDA CLOCK GENERATOR WAVEFORM

4.5.5 Serial/Parallel Data Converter

(Circuit Diagram 430535 Pages 7.4-4 and 7.4-5)

Serial control data transmitted from the SSDA (Analog Interface Assembly), together with their control signals (SSDA strobe and SSDA clock), enter the Reference Divider Assembly via the Mother Assembly.

The data and signals cross the isolation barrier through opto-isolators M6, M7 and M8 into guard.

Serial control and status data is returned out of guard to the SSDA receiver via opto-isolator M1.

4.5.5.1 Logic Levels

The nominal logic levels used in the out-guard SSDA circuits (logic-1=+5V, logic-Ø=0V) are offset at the opto-isolator outputs to:

logic-1=10V,
logic-Ø=-15V;

and level-shifted for the in-guard circuitry to:

logic-1=0V,
logic-Ø=-15V

4.5.5.2 Serial-In/Parallel-Out Control-Data Convertors

Six 8-bit serial shift registers M27, M25, M31, M19, M30 and M15 each have latchable parallel outputs. Their serial "D" inputs and "Q's" outputs are cascaded to form a single 48-bit serial shift register. M27 receives 'serial data in' from M8 via level-shifting buffer M36-4, and M15 passes serial data on to the Parallel-in/Serial-out Status-Data converters.

4.5.5.3 Parallel-In/Serial-Out Status-Data Converters

Two 8-bit serial shift registers M18 and M22 each have parallel inputs. M18 serial "Ds" input accepts serial data from M15; M18 "Q8" output is cascaded to M22 "Ds" input; and M22 "Q8" output delivers SERIAL DATA OUT to buffer M11-11 and back to the SSDA via M1 opto-isolator.

M18 and M22 thus form a 16-bit serial shift register whose 16 parallel inputs states can be inserted into the serial data string.

4.5.5.4 Serial Data Cycling

The serial data, organized in five blocks of three bytes (Refer to Section 4.5.2.2) is accompanied by synchronized bursts of 24 clocks. The output from opto-coupler M7 is buffered via level-shifter M36-2 and then inverted at M14-6. The timing of the positive clock edges allows all bits of serial data (distributed throughout the shift registers) to stabilize before being clocked on.

After the CPU has generated two bursts of data and clock pulses, the serial control data has shifted into the correct positions in control registers M27, M25, M31, M19, M30 and M15. So before the third burst of three bytes, the SSDA produces a strobe which writes the control data into their parallel outputs. Simultaneously, the strobe also fills the 16-bit serial register of M18 and M22 with the status data present on their parallel inputs.

When the strobe ends, further transfers between serial and parallel registers are disabled. The new control data remains latched in the parallel control registers, and the new status data is in the serial status register ready for shifting through guard to the SSDA Rx DATA register.

The control and status bits in the registers are then circulated by three further bursts of clock pulses, until the CPU has read both the new status data and all the control data that were written by the strobe. Verification that the returned control data is identical to the transmitted data, ends the transfer.

If after three attempts, the returned data does not match the transmitted data; the CPU omits to re-trigger monostable M10 in the Reference Divider Assembly. M10 times out and allows $\overline{\text{BARK DEL}}$ to go to logic-Ø. This disables the 48 control data outputs by 'tri-stating' the registers M27, M25, M31, M19, M30 and M15.

4.5.5.5 Parallel Control-Data Outputs and Status-Data Inputs

The data latched in M27, M25, M31, M19, M30 and M15 outputs controls the operation of the Analog circuitry. The effects are therefore described in the sub-sections relevant to their destinations.

As this is a multi-purpose converter, designed for use in more than one model of instrument, some of the control lines are not used.

4.5.6 Safety Monitor (Watchdog)

(Fig. 4.5.4)

The watchdog circuits continuously monitor the CPU/SSDA functional process. Detection of a processor malfunction by the watchdog results in the following actions:

BARK.

This signal:

a. removes the drive from the primary of the High Voltage (1kV) transformer,
b. disables the 400V Power Supply, and
c. disconnects the Current Assembly output from the instrument output terminals.

$\overline{\text{BARK}}$. This is returned as a status bit to the CPU via the SSDA to signal a failure.

BARK DELAYED. This occurs 47ms after BARK and disconnects the AC Voltage Power and Sense circuits from the instrument output terminals.

$\overline{\text{BARK DELAYED}}$. This disables the registers of the serial/parallel data converters.

The watchdog outputs are manipulated by the power-on are set circuits as follows:

(1) BARK DELAYED and $\overline{\text{BARK DELAYED}}$ are held active for 80ms from power-on and then are allowed to the inactive state only after two SSDA strobes have been detected.
(2) BARK is forced active until CPU/SSDA functioning has been verified; the latter must occur within 470ms of power-on.
(3) $\overline{\text{BARK}}$ is held inactive for 470ms from power-on, after which it provides a FAIL message to the CPU.

Operation of the Safety Reset control on the front panel provides a further 100ms period for the CPU/SSDA functional process to settle, during which time the watchdog circuits must verify correct functioning before its outputs are reset.

The watchdog is tripped if a failure to transmit analog-control updates to the analog circuitry occurs. The updates are of two types:

Transfer of 'Output value' data via the Analog Interface comparators,

Transfer of analog switching data via the SSDA every 40ms.

The CPU generates pulses at 8ms intervals to verify that the correct output value has been latched into the Analog Interface comparators. These pulses are allowed to pass into guard only if the SSDA verifies that the analog switching data is being transferred normally at 40ms intervals. Once in

guard, the pulses prevent the watchdog flip-flops from generating their four BARK and BARK DELAYED output signals; by re-triggering a monostable (M10-4 : 18ms).

If two or more pulses are missing, M10 releases the hold, and the watchdog flip-flops 'Bark', activating the safety circuitry. They will be missing if the output value comparators are incorrectly updated, or if the SSDA fails to generate 'Transmit' IRQ pulses for a period exceeding 470ms, or if the CPU crashes.

The in-guard watchdog circuits are located on the Referece Divider pcb; the out-guard control signals originate in the Digital pcb and are processed in the Analog Interface pcb.

4.5.6.1 Out-Guard Watchdog
(Circuit Diagrams 430570 Section 7.3 and 430535 Section 7.4)

The CPU verifies the validity of each serial-interface transfer by instructing the SSDA to generate a 'Watchdog Enable' trigger. This pulse, termed W.DOG ENBL SET (M44-7 on p7.3-3), triggers watchdog-enabling monostable M29-11 (p7.3-1).

W.DOG ENBL SET triggering and retriggering extends the natural (470ms) unstable state of M29 indefinitely. Unless the retriggers fail, W.DOG ENABLE at M29-9 remains at logic-Ø. Absence of W.DOG ENBL SET retriggers for longer than 470ms allows M29-9 to restabilize to logic-1.

W.DOG ENABLE is inverted at M43-3 and applied to NAND M46-12 (p7.3-4).

During each successful processor cycle, the CPU addresses M51-9 (Digital Assembly p7.2-2). The resulting low active pulses at 8ms intervals are inverted, and gated with WRT STRB to generate the active-low signal W.DOG at M49-11.

W.DOG travels via the Mother Assembly to the Analog Interface Assembly where it is gated with the W.DOG ENABLE signal at NAND M46 (p7.3-4). The resulting signal at M46-13, W.DOG, consists of positive-going pulses at 8ms intervals when the CPU/SSDA system is working normally, or a logic-1 level if the SSDA fails.

The W.DOG signal travels via the Mother Assembly to be passed into guard on the Reference Divider Assembly (Opto-coupler M9 on p7.4-5).

4.5.6.2 In-Guard Watchdog
(Circuit Diagram 430535 Page 7.4-5)

NOTE: The operating levels of the in-guard CMOS circuits are negatively displaced as follows (nominal voltages):

Opto-coupler output circuits
- logic-1: -10Vdc
- logic-Ø: -15Vdc

Digital CMOS circuits
- logic-1: 0V
- logic-Ø: -15Vdc

Level-shifter M36 carries out the interfacing between these two levels.

The signal, W.DOG, is opto-coupled into guard by M9. During normal operation the W.DOG in-guard positive-going 8ms pulses trigger and successively re-trigger the monostable M10-4 to give a continuing logic-Ø at M10-7. The 18ms unstable state of the monostable allows for the absence of one pulse, but the absence of two or more pulses allows M10 to reset, taking M10-7 to logic-1.

The logic level from M10-7 is applied to the set input of flip-flop M13-6. With reset M13-4 at logic-Ø during normal operation, the output conditions of M13-1 and M13-2 are as follows:

(1) Set input M13-6=logic-Ø (no fault);
M13-1 (Q)=logic-Ø — BARK not active
M13-2 (Q)=logic-1 — BARK not active

(2) Set input M13-6=logic-1 (malfunction);
M13-1 (Q)=logic-1 — BARK active
M13-2 (Q)=logic-Ø — BARK active

The action of M13-2 changing to logic-Ø, triggers monostable M10-11 which has a relaxation time of 47ms. After 47ms, M10-9 output clocks flip-flop M13-11 to give the command BARK DEL from M13-13 and BARK DEL from inverter M14-12.

4.5.6.3 Power-On Reset (Circuit Diagram 430535 Page 7.4-5)

When power is first applied, the build-up of the -15V supply forces shift register M37 Set inputs to logic-Ø, but its Reset inputs are held at logic-1 by the charging action of R122/C7.

So M37 is forced into reset state for about 80ms:
M37-2 imposes logic-1 at M13-8 Set input.
M37-1 at logic-Ø holds M10 inactive at M10-3, thus preventing random triggering at M10-4 from erratic W.DOG inputs, as the SSDA/CPU functions start up. 'Q' output M10-7 holds M13-6 Set input at logic-1.

Also, the Reset inputs M13-4 and M13-10 are held at logic-1 for a period of 470ms from power-on by the signal FP RST, generated by the power-on reset action of M53 on the Digital Assembly (p7.2-2).

Therefore, the Set/Reset inputs M13-8/M13-10, initially both at logic-1, force M13-13 output to logic-1 to give active BARK DELAYED and BARK DELAYED outputs.

The Set/Reset inputs M13-6 and M13-4, also initially both at logic-1, force:
M13-1 to logic-1 (Active BARK), and
M13-2 to logic-1 (Non-active BARK).

The output conditions of M37 (M37-1=logic-Ø, M37-2=logic-1) remain unchanged after the 80ms time constant at M37 Reset inputs, but then M37-11 is free to be triggered from the SSDA strobe input. Two strobe inputs must occur before M37-1 clocks to logic-1 and M37-2 to logic-Ø. M13-13 now changes to logic-Ø, making BARK DELAYED and BARK DELAYED inactive, and the inhibit is removed from M10-3.

The outputs M13-1 and M13-2 remain unchanged until M10-7 fals to logic-Ø by the clocking action of pulses on the W.DOG input. This must occur before M13-4 returns to logic-Ø (at 470ms from power-on) for BARK to be made inactive, otherwise BARK remains active and BARK is set to logic-Ø, giving a fail status bit to the CPU.

4.5.6.4 Malfunction (Fig 4.5.4)

Any malfunction which introduces one of the following conditions will cause the watchdog to bark:

a. CPU WRT STRB fails at logic-Ø.
b. M51 on the Digital Assembly does not receive the address to activate M51-9.
c. The SSDA fails to transmit bursts of the W.DOG ENABLE SET pulses to M29 (SSDA is not transferring serial data).
d. The SSDA Strobe is not triggering M37.
e. W.DOG pulses are not triggering M10.

In addition to failures at these points, the CPU is informed via SSDA Status byte transfer of certain analog malfunctions. Subsequent CPU action can include deliberate activation of the watchdog by omitting to address M51 as in (b) above.

4.5.6.5 Safety Reset

Once the watchdog has 'Barked' it can be reset, if the malfunction has cleared, by pressing the Safety Reset control on the front panel.

The Safety Reset input to the watchdog circuit, FP RST, is active for 100ms after pressing the Safety Reset key. (M53-9 on Digital Assembly p7.2-2). During this period, the Reset inputs at M13-4 and M13-10 are held at logic-1, allowing the correct pulse inputs from the processor and SSDA to hold M13-6 at logic-Ø, and to reset M13-13 to logic-Ø. The watchdog will not reset if the malfunction persists.

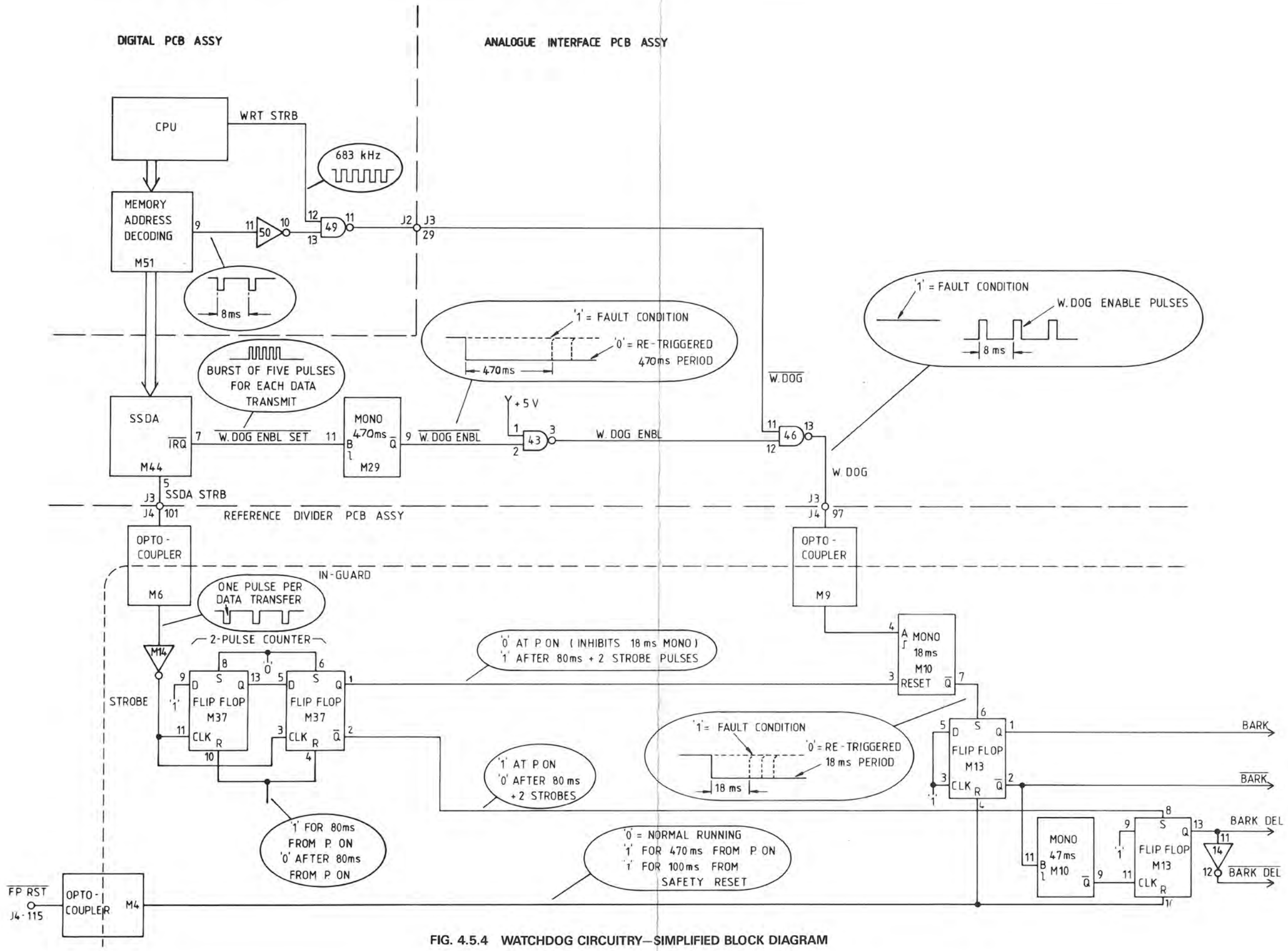


FIG. 4.5.4 WATCHDOG CIRCUITRY—SIMPLIFIED BLOCK DIAGRAM

4.6 PRECISION DIVIDER

The out-guard circuitry described in this section performs the following functions:

(1) Receives and latches the demanded output value from the CPU in the form of a 25-bit word.

(2) Generates a continuous 13-bit up-count from the 1.024MHz Master Clock (8ms count cycle).

(3) Compares the 13-bit count with the 13 most-significant bits of the 25-bit word, generating 'Set' and 'Reset' pulses. These are transferred into guard to trigger the 'Most Significant' JFET switch in the Reference Divider.

(4) Compares the 12 most-significant bits of the count with the 12 least-significant bits of the 25-bit word, generating, 'Set' and 'Reset' pulses. These are transferred into guard to trigger the 'Least-Significant' JFET switch in the Reference Divider.

The out-guard circuitry is located on the Analogue Interface Assembly.

The in-guard circuitry performs the following functions:

(5) Provides a Master Reference Voltage (20.6V) which is chopped by the 'Most Significant' JFET switch to generate a square-wave, whose Mark/Period ratio is controlled by the 13 most-significant bits of the 25-bit word. The square-wave is smoothed by a 7-pole Bessel filter, to provice a DC voltage whose value varies directly as the Mark/Period ratio of the MSB square-wave.

(6) Provides a Buffered Reference Voltage (8.83V) which is chopped by the 'Least-Significant' JFET switch to generate a square-wave, whose Mark/Period ratio is controlled by the 12 least-significant bits of the 25-bit word. The square-wave is smoothed by a 3-pole Bessel filter to provide a DC voltage whose value varies directly as the Mark/Period ratio of the LSB square-wave.

(7) Conditions the two DC voltages produced by the 7-pole and 3-pole filters, delivering them via full 4-wire connections to be summed on the AC Assembly as a 'Working Reference Voltage' between 0.126V and 2.79V; whose value is accurately proportional to the value demanded by the CPU's 25-bit word.

(8) Digitally generates a stepped AC reference voltage whose peak value is equal to the DC Working Reference Voltage. This gives the RMS Comparator (described in sub-section 4.14) the considerable advantage of comparing AC sense against AC Reference. (If AC were compared with DC, small DC offsets would magnify and lead to 'DC turnover' errors). The AC waveform is constructed in ten steps by a digitally controlled switching network. It has been given the name 'Quasi-Sinewave'.

The in-guard circuitry is located on the Reference Divider PCB Assembly.

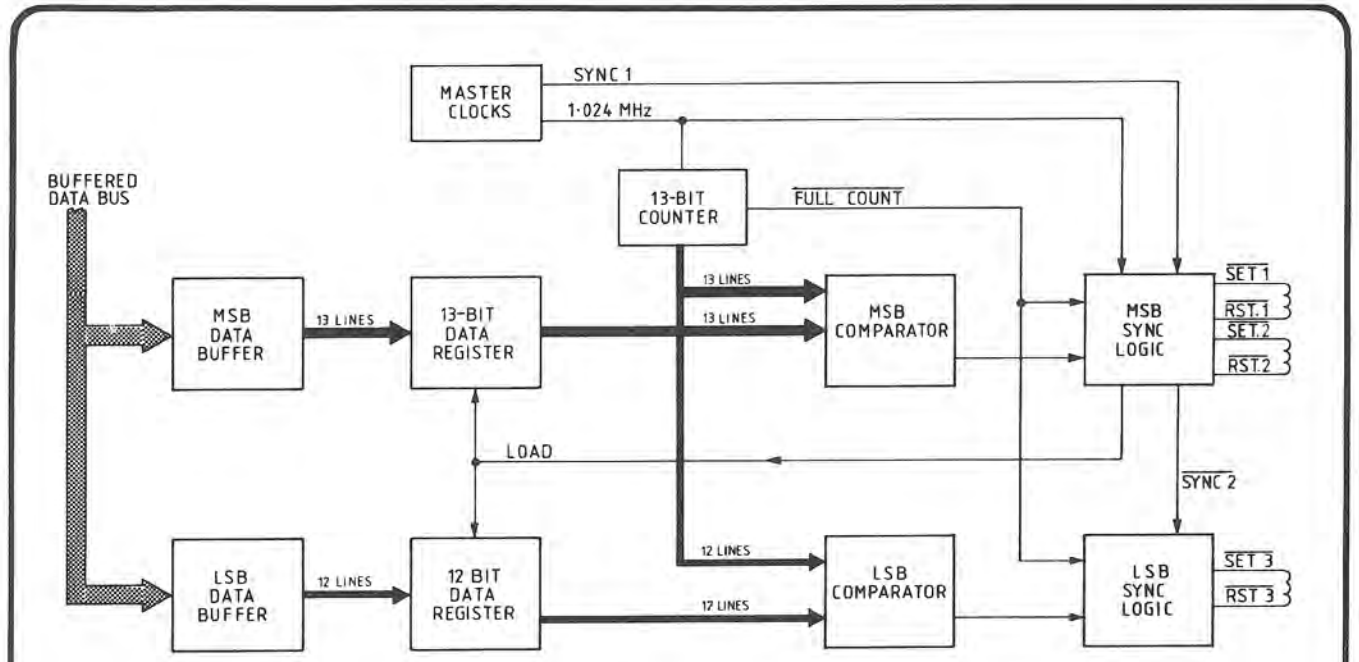


FIG. 4.6.1 PRECISION DIVIDER OUT-GUARD CIRCUITRY—SIMPLIFIED BLOCK DIAGRAM

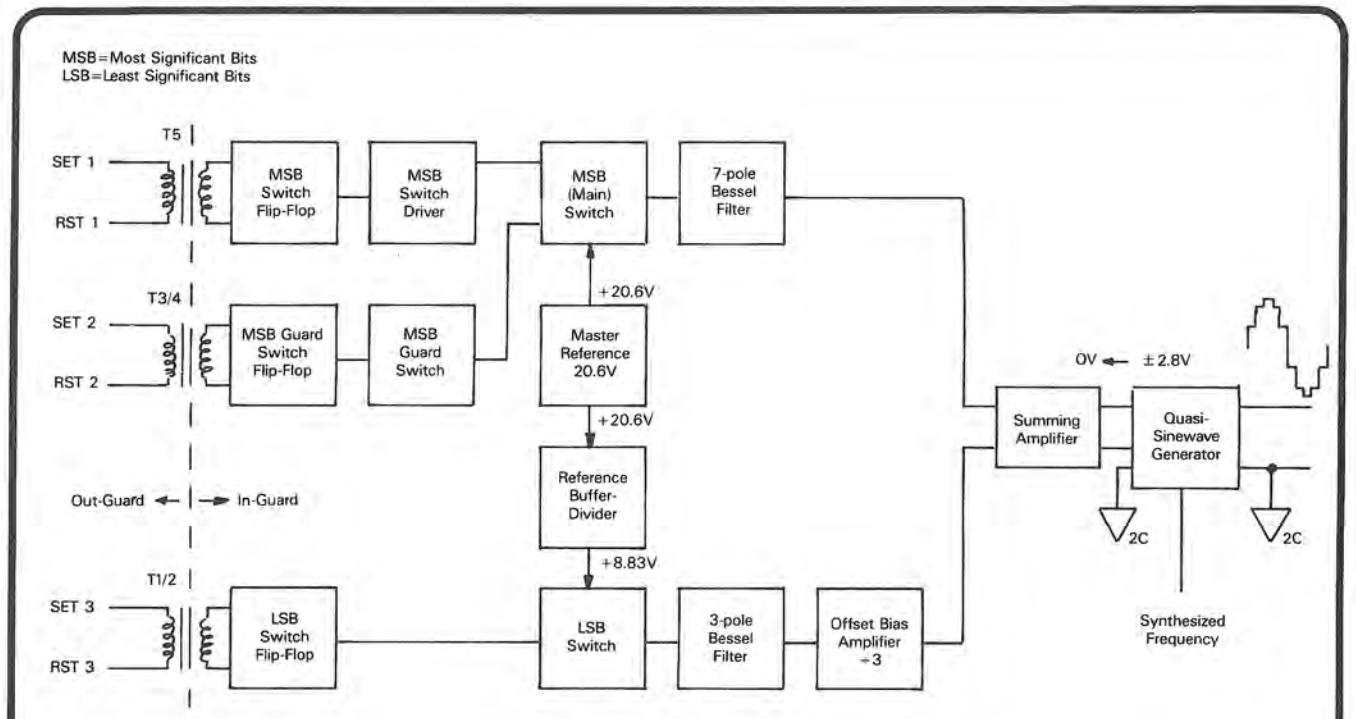


FIG. 4.6.2 PRECISION DIVIDER IN-GUARD CIRCUITRY—SIMPLIFIED BLOCK DIAGRAM

4.6.1 Precision Divider Comparators
(Circuit Diagram No. 430570)

4.6.1.1 General (Figs. 4.6.1 and 4.6.2)

The comparators are designed as a means of translating a binary word into the accurately defined Mark/Period ratio of a square-wave. The ratio of the square-wave's average value to its peak value subsequently defines the division ratio applied to the Master Reference, and must be adjustable at high resolution.

The required decimal resolution translates into a binary word of 25 bits in length, and each bit needs to exert control of the division ratio.

A single comparator of this length would require more than 30 million clocks to scan, which at sensible clock frequencies would occupy several seconds. To filter out the resultant chopping frequency would require large and expensive components, and force unrealistic operational time-constraints.

In the 4200, by splitting the word into two parts: the 13 most-significant bits (MSB) and the 12 least-significant bits (LSB), a scan-cycling frequency of 125Hz is obtained from a 1.024MHz clock.

Both MSB and LSB comparators are scanned concurrently by the same 13-bit counter, forming two separate square-waves. These act on two separate reference divider switches and filters to generate two separate DC voltages which are subsequently recombined in the AC Assembly.

In summary, the two comparators translate information from the CPU into time-related pulses which control mark/period switching in the reference divider. One comparator translates the 13 most-significant bits of CPU data; the other, the 12 least-significant bits. The comparators perform concurrently, cycling continuously at 125Hz, taking 8ms per full count.

At the start of each 8ms counting period, each comparator generates a SET pulse to start its reference divider 'Mark'. Then after precisely-measured delay times, each generates a RESET pulse to terminate the 'Mark', and start the 'Space'.

At each 8ms full-count, the clock resets and continues up-counting from zero.

4.6.1.2 Comparator Operation (Fig. 4.6.1)

The MSB and LSB Data Buffers are periodically loaded and latched with binary 'Demanded Output Value' data under the control of the CPU.

At the end of each comparator counting cycle, the 13-bit counter $\overline{\text{FULL COUNT}}$ output enables the generation of set pulses $\overline{\text{SET 1}}$, $\overline{\text{SET 2}}$ and $\overline{\text{SET 3}}$ by the MSB and LSB 'Sync Logic' circuits.

$\overline{\text{FULL COUNT}}$ also generates the LOAD command. This writes the data, currently latched in the buffers, into working data latches which form the 13-bit and 12-bit Data Registers, updating the earlier 'Demanded Output Value' priming the comparator.

The MSB and LSB comparators translate this binary data into 'RESET' pulses, whose time relationships to the 'SET' pulses are established by the value of their binary words.

4.6.1.3 13-Bit (MSB) Comparator
(Circuit Diagram No. 430570 Page 7.3-2)

The 13 binary outputs of the up-counter scan the 13 Exclusive-OR elements of the MSB Comparator. With the least-significant bit at 512kHz, and the most-significant at 125Hz, the 8ms scan time thus divides into 8192 time elements, each of 977ns.

Each time element has a unique binary code, incrementing by one bit on its predecessor. When this coincides with the bit-pattern set in the data register, the comparator provides an output pulse to the MSB sync logic. The latter generates reset pulses $\overline{\text{RST 1}}$ and $\overline{\text{RST 2}}$ in synchronism with the signal SYNC 1 (2.048MHz).

4.6.1.4 12-Bit (LSB) Comparator
(Circuit Diagram No. 430570 Page 7.3-1)

This functions in the same manner as the MSB comparator, but only 12 bits are scanned over the same 8ms counting period. This accomodates 4096 time elements of 1954ns for each binary increment.

SYNC 2 pulses, generated in the MSB Sync Logic circuitry at half the rate of SYNC 1, synchronize the $\overline{\text{RST3}}$ output from the LSB Sync Logic.

4.6.2 Comparator Circuit Action

4.6.2.1 Input Data Latches
(Circuit Diagram 430570 Pages 7.3-1 and 7.3-2)

The input buffered data latches M31 to M34 and M37 to M39 receive 27 data bits in four bytes from the buffered data bus. Latches are selected by signals REF DIV 1, 2, 3 or 4 from the memory address decoding on the digital pcb. Data is clocked to the 'Q' outputs of the latches on the positive-going edge of $\overline{\text{WRT STRB}}$.

Data from the input latches is used as follows:

25 bits form a data word to the comparator registers M47, M48, M49 (part), M51 and M52. One bit triggers monostable M29 (part), the Q output of which is inverted and buffered to provide the control $\overline{\text{UPD (OG)}}$ used in the relay drive logic for analog switching. One bit, EXT FREQ divided by 10, is not used in the 4200.

4.6.2.2 13-Bit Counter

(Circuit Diagram 430570 Page 7.3-2)
(Refer to Fig. 4.6.3 for Waveforms)

The counter comprises three 4-bit binary counters M15, M16, M17 and J-K flip-flop M42 (half dual package). The squarewave outputs from the counter are on 13 binary-coded lines, the first (least-significant) being a 512kHz squarewave, the others successively divided in frequency to the most significant output of 125Hz.

Bit 1 is provided by J-K flip-flop M42, which toggles on each falling edge of the 1.024MHz clock to give 512kHz Q and $\overline{Q}$ outputs. These outputs are used as follows:

(1) Q and $\overline{Q}$ complementary outputs together provide the least-significant input to the 13-bit comparator;

(2) The Q output controls the counting rate of M15, synchronizes M16 and M17, and is used in the gating of $\overline{\text{FULL COUNT}}$.

Counters M15, M16 and M17 are cascaded as a 12-bit counter and synchronously clocked by the 1.024MHz. M15 counting is enabled only when M42 Q output is logic-1 at the count-enable input M15-7.

As M42 output is at 512kHz, clocking of M15 occurs on the rising edge of alternate 1.024MHz clocks, thus giving outputs of 256, 128, 64 and 32kHz squarewaves from M15.

Counter M16 is enabled by the carry output from M15 together with 512kHz from M42 at the count-enable pins M16-10 and 7 respectively, thus giving outputs of 16, 8, 4 and 2 kHz squarewaves from M16.

Counter M17 functions in a similar manner to give outputs of 1kHz, 500, 250 and 125Hz squarewaves.

The 2μs-long carry output from M17 occurs at the end of the 125Hz output when all counter outputs are at logic-1. The carry output is NANDed with M42 Q output to give the 1μs-long logic command $\overline{\text{FULL COUNT}}$. The counting cycle resets and continues, starting from bit 1.

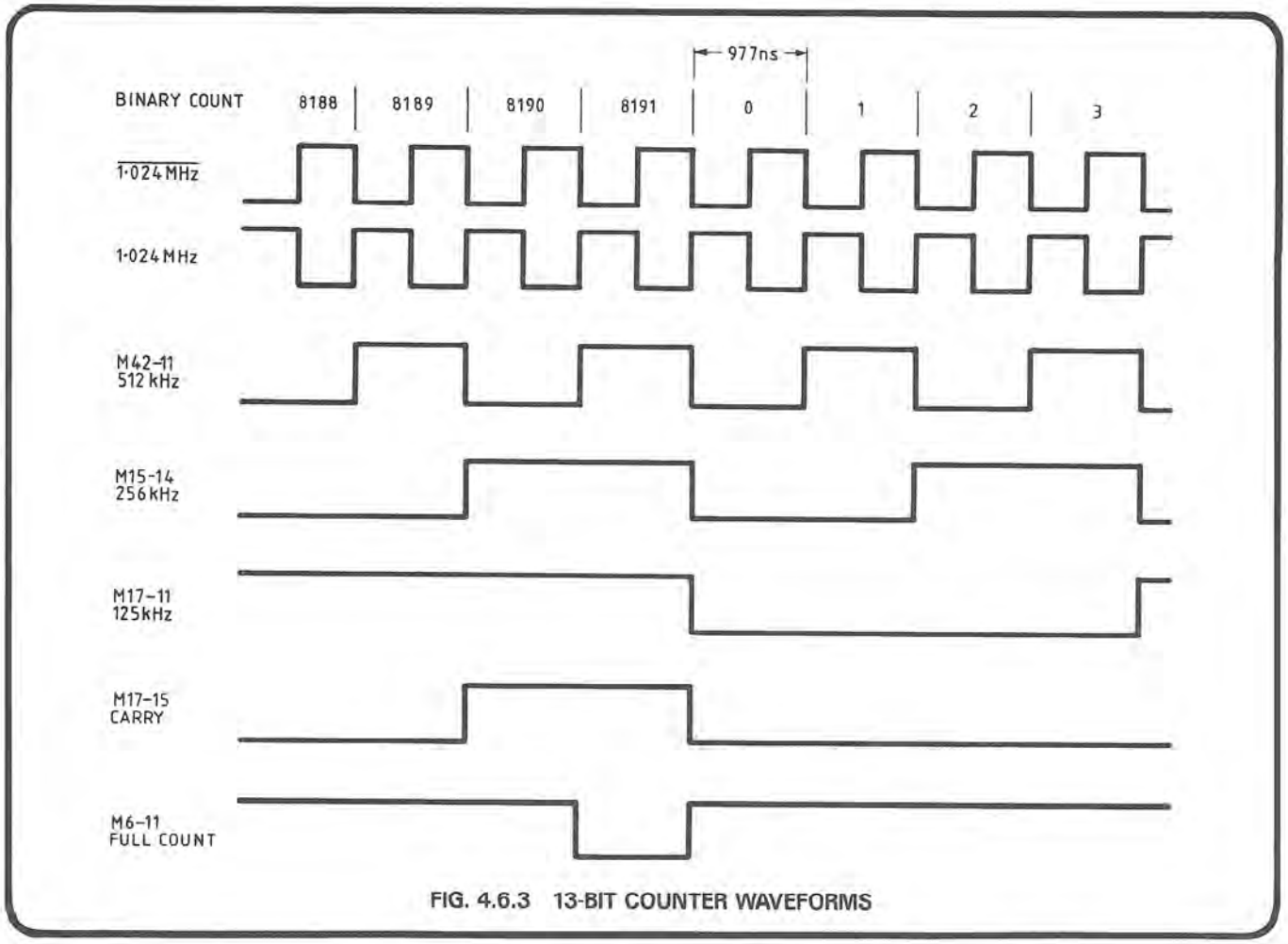


FIG. 4.6.3 13-BIT COUNTER WAVEFORMS

4.6.2.3 13-Bit Comparator Action
(Circuit Diagram 430570 Page 7.3-2)

The 13-bit comparator provides a logic-1 output at TP12 whenever a coincidence occurs between the following two sets of data:

(1) Data set in registers M47, M48 and M49-1;

(2) Data from 13-bit counter M42, M15, M16 and M17.

Twelve exclusive-OR elements M25, M26, M27 and three NOR gates of M12 are used to detect a coincidence. The data in the registers is preset by the CPU, while that presented by the 13-bit counter cycles through every binary combination possible on 13 lines.

Two coincident inputs to an exclusive-OR gate provide a logic-Ø to the 12-input NOR gates M24/M23; full coincidence in bits 2 to 13 is shown by a logic-Ø at NAND M13-6. Coincidence at bit 1 is shown by logic-Ø at M12-13 and M12-4 as follows:

M12 INPUT PINS			M12 OUTPUT PINS		
6	11	9/12	4	13	
0	1	0	0	0	only 4 input combinations available
0	1	1	1	0	
1	0	0	0	1	
1	0	1	0	0	

A $\overline{\text{BUSY}}$ signal is generated by the comparator at NAND M50-13 (TP2) when the 13-bit counter approaches full count. Bits 8 to 13 are at logic-1 for the period of 125μs preceding the end of the counter cycle (see Fig. 4.6.4). The $\overline{\text{BUSY}}$ level is applied to the D input at M49-9 and is synchronously clocked through as $\overline{\text{REF BUSY}}$ to buffer M45-2 by 1.024MHz.

As described earlier, the demanded output value is defined by the CPU to a resolution of 25 bits, contained in four data bytes. The time needed for the 4-byte transfer could allow the latches to contain spurious data until they were fully loaded, and an inaccurate parity could be registered with the counter still running. The counter must not be interrupted, as its full count defines the 'period' of the mark-to-period ratio, which is used to control the division of the reference voltage. It is therefore necessary to reduce the loading time, and this is achieved by double-latching the data.

When the CPU has data to load into the input data latches, it first interrogates the comparator by enabling buffers M45 through $\overline{\text{REV DIV RD}}$. The $\overline{\text{REF BUSY}}$ signal at logic-1 (M45-3) indicates to the CPU that sufficient time is available for the latch-loading process to take place (at least 125μs remain before the LOAD pulse occurs).

If the $\overline{\text{REF BUSY}}$ signal is at logic-Ø, the CPU waits until it returns to logic-1 again.

When the $\overline{\text{REF BUSY}}$ signal is at logic-1, the CPU loads the data by first carrying out four transfers of one byte each into the seven quad buffer latches M31 to M34, and M37 to M39. Each byte's destination is addressed by one of the chip-select signals $\overline{\text{REF.DIV.1}}$ to $\overline{\text{REF.DIV.4}}$, which enables the selected buffer latches. The data is latched by the $\overline{\text{WRT STRB}}$ signal.

Once the full 25-bit word has been latched into the buffers, it is available as a single word at the data inputs of the comparator latches M47, M48, M49, M51 and M52. The CPU again interrogates the comparator by $\overline{\text{REF DIV RD}}$, and five of the elements of M45 buffer the five most-significant data bits back to the CPU.

If parity with the transmitted data is confirmed, the CPU takes no action. When the counter times out, the $\overline{\text{FULL COUNT}}$ signal is clocked through to M14-6 by $\overline{\text{SYNC 2}}$ as the LOAD signal, and the new data is transferred into the comparator latches.

If the data latched in the buffers is not as transmitted, the CPU initiates the FAIL 4 message procedure to the operator.

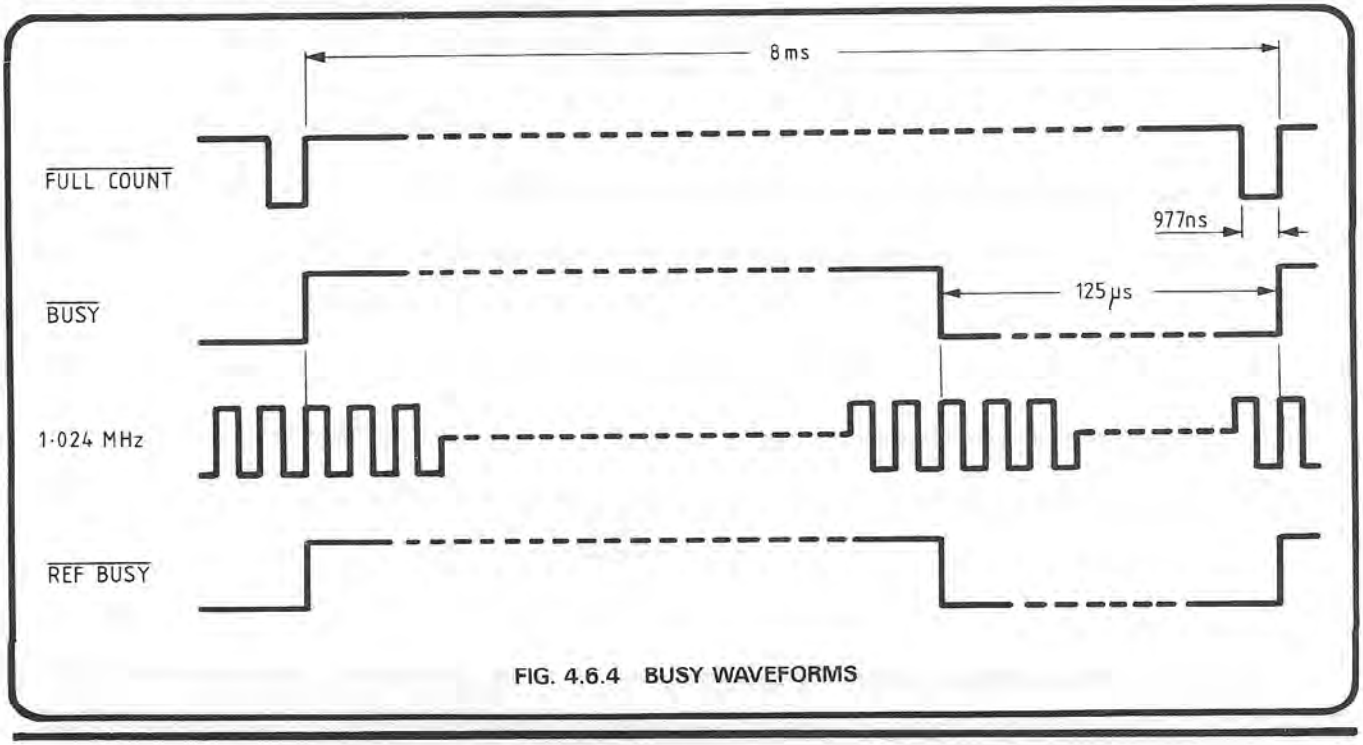


FIG. 4.6.4 BUSY WAVEFORMS

4.6.2.4 'Most Significant Bits' SYNC Logic

(Circuit Diagram 430443 Page 7.3-2)
(Refer to Fig. 4.6.5 for Waveforms)

This circuit, M14, M6, M7 and M8, provides the following signals: $\overline{\text{SYNC 2}}$, LOAD, $\overline{\text{SET 1}}$, $\overline{\text{SET 2}}$, $\overline{\text{RST 1}}$ and $\overline{\text{RST 2}}$.

$\overline{\text{SYNC 2}}$ is obtained by NAND gating 1.024MHz and SYNC 1 to give a synchronizing pulse at half the rate of SYNC 1. (See Fig. 4.6.5).

The LOAD pulse enables the 13-bit comparator registers, and is generated at M14-6 towards the end of the counter's full-count output. $\overline{\text{FULL COUNT}}$ sets the D input M14-2 and the level is clocked, inverted, from M14-6 by the next two $\overline{\text{SYNC 2}}$ pulses that occur.

The inverse of LOAD is used to time the pulse $\overline{\text{SET 1}}$ by NOR gating at M7-4 with 1.024MHz. The pulse at M7-4 is then NAND gated with SYNC 1 to provide $\overline{\text{SET 1}}$ from M8-1. The pulse $\overline{\text{SET 2}}$, which occurs 977ns before $\overline{\text{SET 1}}$, is obtained by gating $\overline{\text{FULL COUNT}}$ with 1.024MHz at NOR M7-10 and then NAND gating at M8-10 with SYNC 1.

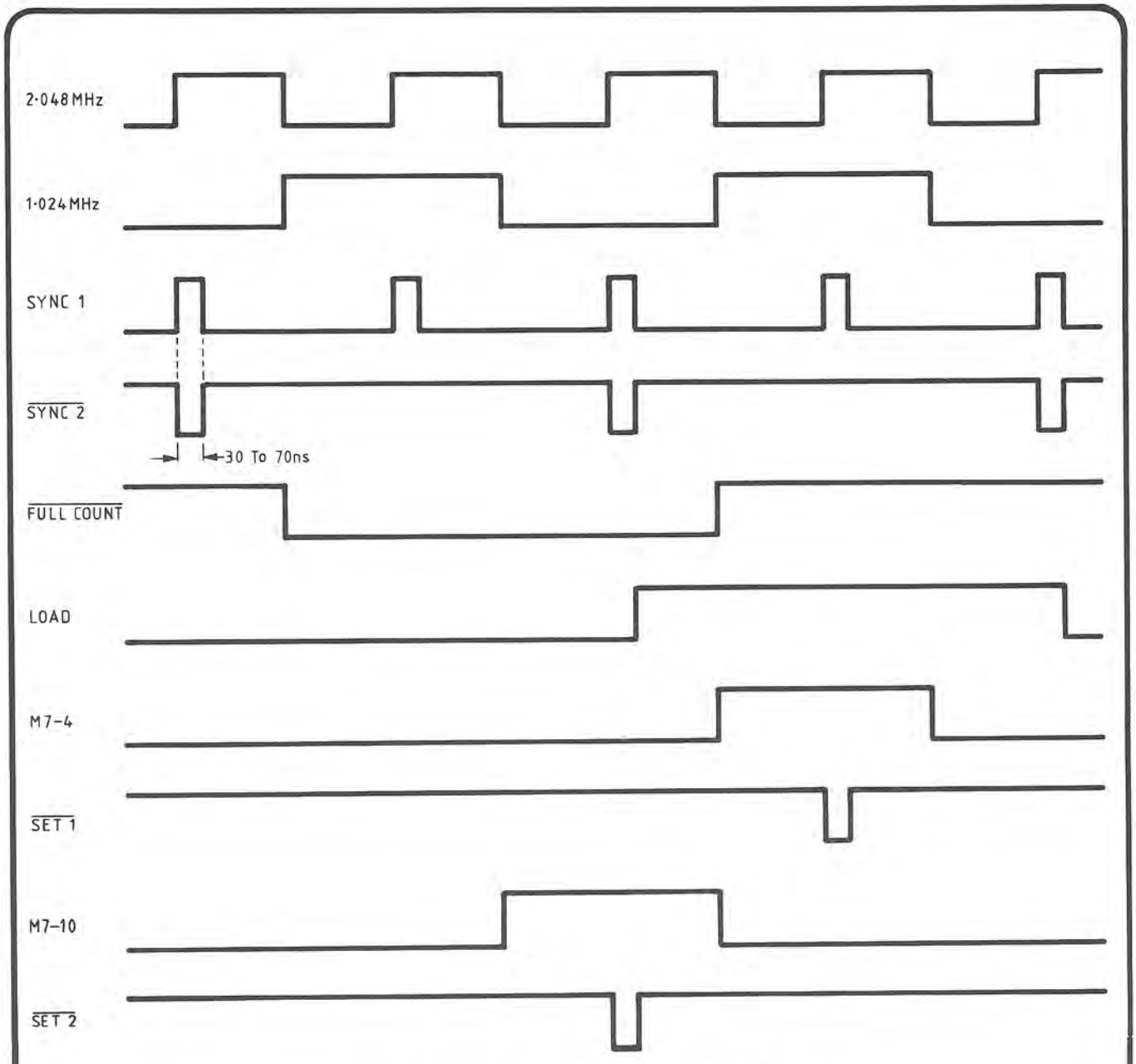


FIG. 4.6.5 MSB SYNC LOGIC WAVEFORMS

Reset pulse generation (see Fig. 4.6.6) is initiated by a logic-1 level at TP12. This can occur at any one of the 8192 binary counts of the 13-bit counter, the actual time slot in which it appears depends on the binary count at which the coincidence occurs.

The coincidence level at TP12 is NAND gated at M6-8; M6-10 being at logic-1 for all binary counts except 8191. The logic-Ø at M6-8 is NOR-gated at M7-1 with 1.024MHz, this is then used to select the next SYNC 1 pulse via NAND M8-4 to provide the pulse $\overline{\text{RST 1}}$.

The coincidence level at TP12 is used to set the D input at flip-flop M14-12. This level is clocked to NAND M6-5 by the next $\overline{\text{SYNC 2}}$ pulse. NAND input M6-4 is at logic-1 except when LOAD is active, thus M14-9 output is inverted at M6-6 to be NOR-gated with 1.024MHz at M7-13. This is then used to select the next SYNC 1 pulse via NAND M8-10 to provide the pulse $\overline{\text{RST 2}}$.

The pulse-timing example given in Fig. 4.6.6 shows the generation of $\overline{\text{RST 1}}$ and $\overline{\text{RST 2}}$ when coincidence occurs in the comparator at binary count = 0 (waveforms in continuous lines).

Coincidence occurring at binary count 1 causes $\overline{\text{RST 1}}$ and $\overline{\text{RST 2}}$ to increment in time by 977ns with respect to the $\overline{\text{SET 1}}$ and $\overline{\text{SET 2}}$ pulses (waveforms in broken lines).

$\overline{\text{RST 1}}$ and $\overline{\text{RST 2}}$ are generated with the same relationship in time to the comparator coincidence when the latter occurs in any binary count time slot from 0 to 8190 (inclusive).

Note that as the comparator word increments in value, $\overline{\text{RST 1}}$ and $\overline{\text{RST 2}}$ increment in time after $\overline{\text{SET 1}}$ and $\overline{\text{SET 2}}$, which remain stationary with respect to $\overline{\text{FULL COUNT}}$ and LOAD.

$\overline{\text{RST 1}}$ and $\overline{\text{RST 2}}$ are inhibited when coincidence occurs at binary count 8191 to allow for the re-loading of the input registers at the end of the counter cycle. The inhibit is performed by the $\overline{\text{FULL COUNT}}$ level going to logic-Ø and NAND M6-10 which prevents $\overline{\text{RST 1}}$ being generated, and by flip-flop M14-5 output going to logic-Ø for the period of the load pulse which inhibits $\overline{\text{RST 2}}$.

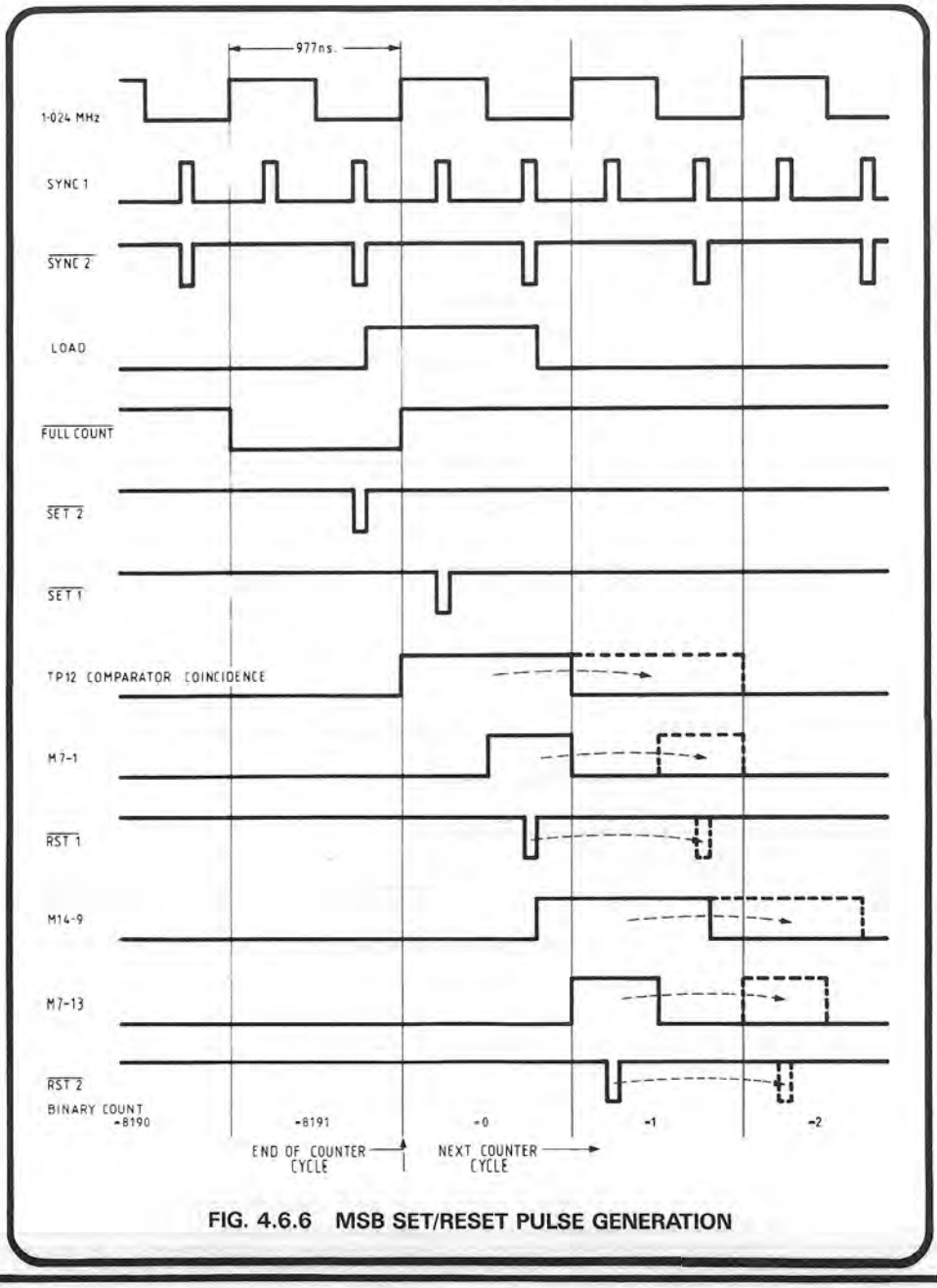


FIG. 4.6.6 MSB SET/RESET PULSE GENERATION

4.6.2.5 12-Bit Comparator Action
(Circuit Diagram 430570 Page 7.3-1)

This functions in an identical manner to the 13-bit comparator previously described. Twelve exclusive OR gates, M19, M20 and M21, receive the 12-bit binary output from the common counter and compare these bits with the data in the data registers. The least-significant bit changes at a rate of 256kHz, and the most-significant bit at 125Hz. Coincidence occurring in any of the 4096 binary-count time slots available in the comparator cycle is shown as a logic-Ø at TP5 for a period of 1954ns.

4.6.2.6 'Least Significant Bits' SYNC Logic
(Refer to Fig. 4.6.7 for Waveforms)

The timing of $\overline{\text{SET 3}}$ is controlled by the $\overline{\text{FULL COUNT}}$ pulse from the 13-bit counter. The inverted $\overline{\text{FULL COUNT}}$ at M43-6 is gated with the inverted $\overline{\text{SYNC 2}}$ from M43-11 to give, at M46-1, $\overline{\text{SET 3}}$.

The comparator coincidence logic level is inverted to logic-Ø at M12-1; M12-2 being at logic-Ø except when $\overline{\text{FULL COUNT}}$ is low. The waveform at M12-1 is of 1954ns duration and therefore allows two consecutive $\overline{\text{SYNC 2}}$ pulses to be gated to M46-4 ($\overline{\text{RST 3}}$).

This condition exists for all $\overline{\text{RST 3}}$ timings except at the binary count of 4095; in this instance, the $\overline{\text{FULL COUNT}}$ pulse occurs after the gating of the first $\overline{\text{SYNC 2}}$ pulse, sets M12-2 to logic-1 and so prevents the second pulse appearing at $\overline{\text{RST 3}}$. In practice, the second pulse of $\overline{\text{RST 3}}$ has no operational significance.

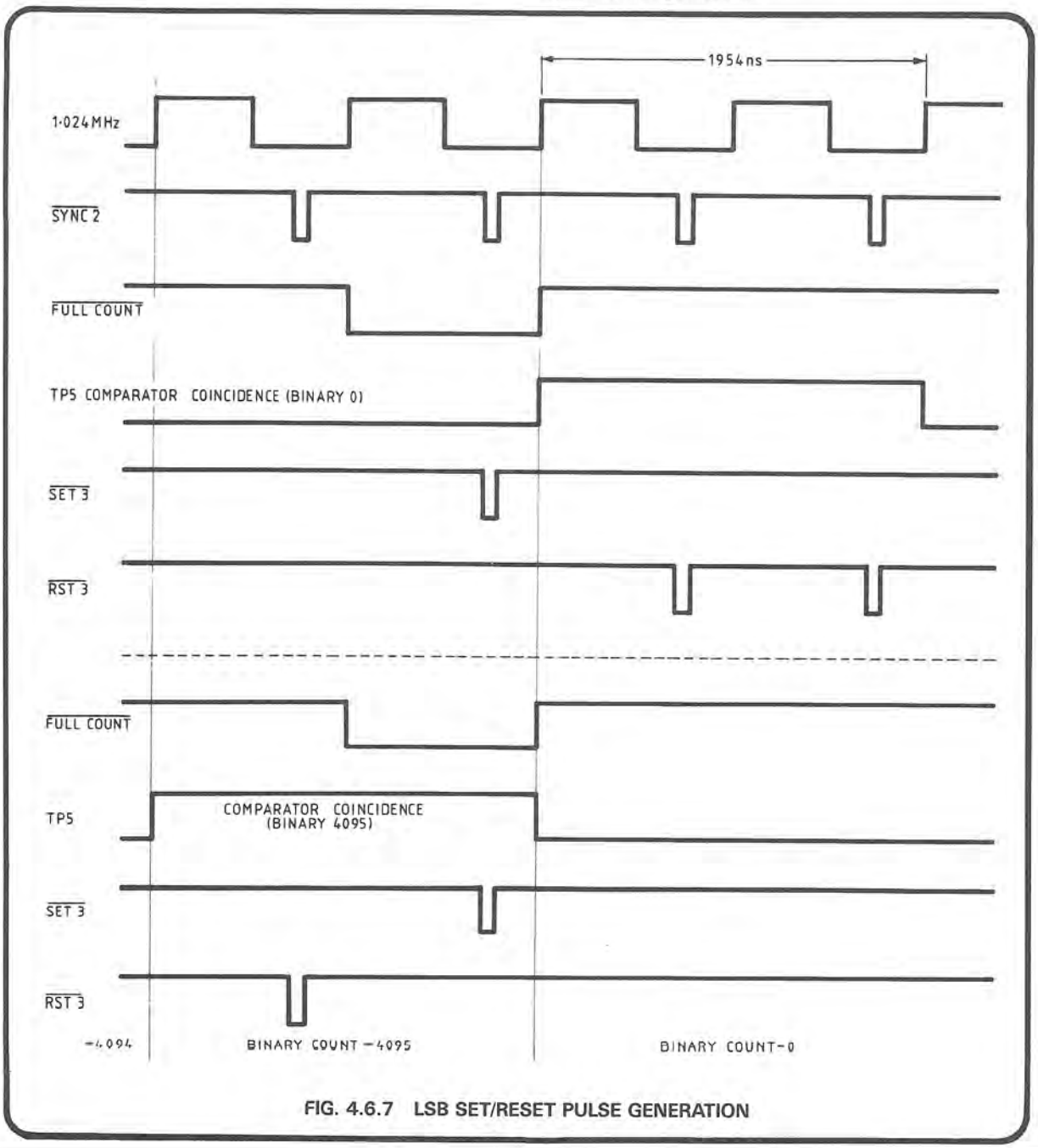


FIG. 4.6.7 LSB SET/RESET PULSE GENERATION

4.6.3 References and Reference Divider

(Circuit Diagrams 430535 Section 7.4)
(Refer also to Fig. 4.6.2)

The set and reset pulses from the precision divider comparators control the timing of JFET switches which chop the Master Reference voltages.

The chopped references are filtered to generate two voltages whose levels are proportional to the MSB and LSB squarewaves' mark:period ratio (duty cycle). These MSB and LSB voltages are conditioned, and transferred to the AC Assembly by full 4-wire sensed connection where they are summed at a star-point to generate a Working Reference: 'REF+Ve'.

REF+Ve is adjustable at high resolution (0.03ppm:approx. 0.6μV increments), with a maximum possible range of adjustment of 0-20V.

The Reference Divider and Master Reference are also employed in other Calibrators of the series, where the high available resolution is advantageous. In the 4200, however, such resolution is not necessary for the 6½-digit accuracies associated with AC outputs. Also, the basic range is the 1V Range, all other ranges employing either attenuation or amplification. The working reference is therefore reduced to 0.126V to 2.79V by software, which results in a reduction of the maximum mark:period ratio of the chopping waveform to about 0.14.

4.6.4 Master Reference

(Circuit Diagram 430553 page 7.4-4)
(Refer also to Fig. 4.6.8)

The Master Reference determines the fundamental long and short-term stability of the 4200. It is a separate pcb mounted on the Reference Divider Assembly.
(Refer to the Layout Drawing facing Page 7.4-7)

The basic circuit shown in Fig. 4.6.8 acts as a constant-current generator for a zener reference.

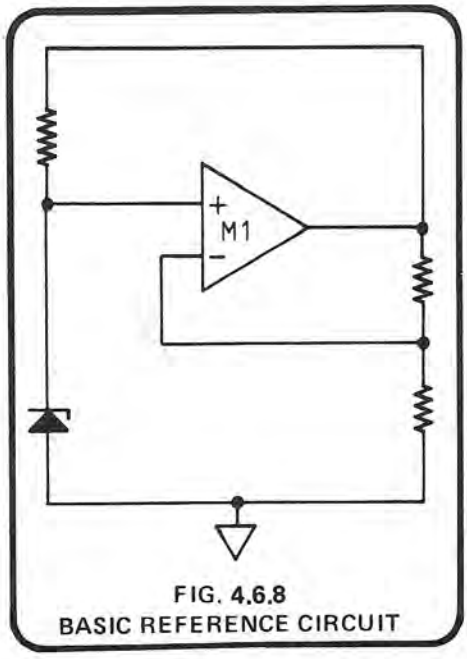


FIG. 4.6.8
BASIC REFERENCE CIRCUIT

The random character of zener drift in the short-to-medium term may in the long term be regarded as averaging to zero. The averaging action of the four zener diodes on Page 7.4-7 reduces the short and medium term variations (due to drift and noise) by a factor of $\sqrt{4}$, effectively twice as stable as a single zener diode.

The diodes and resistors are selected and matched for near-zero temperature coefficient; the overall instrument values are shown together with the stability and accuracy specifications in Section 6 of the User's Handbook.

At manufacture, the zener operating current is adjusted for zero temperature coefficient, by selectively removing links TLA1-5.

The zener voltage of +24.5V at TP3, with respect to Common-R1, is reduced by R24/R25/R26 to +20.6V. This is an approximate value, but it has high temperature and time stability. It is corrected by constants stored in non-volatile memory during calibration. The +20.6V is then buffered by M2 for transmission, at the same value, to the 'Most Significant' Switch in the Reference Divider. Delivery is by sensed connection, the Reference Common-R1 being connected to the Reference Divider Common-4, by a low-resistance wire link from pin A.

4.6.4.1 Buffer M2—Temperature Compensation

(Circuit Diagram 430553 page 7.4-7)

In the 4200 instrument, the temperature compensation applied to M2 is adjusted at manufacture by R29 (set TC slope). This adjustment requires specialised test equipment and should not be attempted by users.

If a fault is suspected on the Reference PCB Assembly (400553), contact your Datron Service Center.

4.6.5 Reference Buffer-Divider

(Circuit Diagram 430535 page 7.4-2)

R80/81 drop the 20.6V Master Reference voltage (V_{Ref}) to +8.83V. M23/Q40 is a voltage-follower providing +8.83V wrt common-4 at the star-point TP11 to supply the least-significant digit switch.

4.6.6 Least-Significant-Digits Switching
(Fig. 4.6.9)

4.6.6.1 Switch Driver

$\overline{\text{SET 3}}$ and $\overline{\text{RST 3}}$ pulses from the LSB Comparator in the Analog Interface Assembly are transferred into guard via pulse transformers T1 and T2, whose centre-tapped secondaries are balanced about Common-4 0V (T1) and +9V (T2).

Q5-Q7 form a fast bistable using emitter-coupled logic, to switch TP1 between +9V (mark) and +20V (space).

During the "Mark" time after SET 3 pulse, Q29 and Q30 are switched ON, connecting LKA to +9V Ref. Q1-Q4 have the same bistable action, switching Q31 off during the "Mark" period by −11V at TP2, thus disconnecting LKA from common-4 (0V).

During the "Space" time after $\overline{\text{RST 3}}$ pulse, Q29 and Q30 disconnect LKA from +9V Ref, and Q1-Q4 switch Q31 on, connecting LKA to common-4 (0V).

Fig. 4.6.9 demonstrates this action.

4.6.6.2 JFET Switch and 3-Pole Filter

The combined action of the switch FETs alternately provides charging current for the 3-pole filter (during 'mark') and discharging current (during 'space').

Two JFETs in parallel (Q29 and Q30) are necessary to equalise the charging and discharging time-constants by matching the "ON" resistances. This preserves linearity of the filter output voltage over the full range of mark/period ratios applied via the set and reset pulses.

The 3-pole filter has the advantage of not being in series with the DC output signal. The 125Hz ripple content is reduced to an acceptable level for the overall instrument specification. The filter output is buffered by voltage-follower M16.

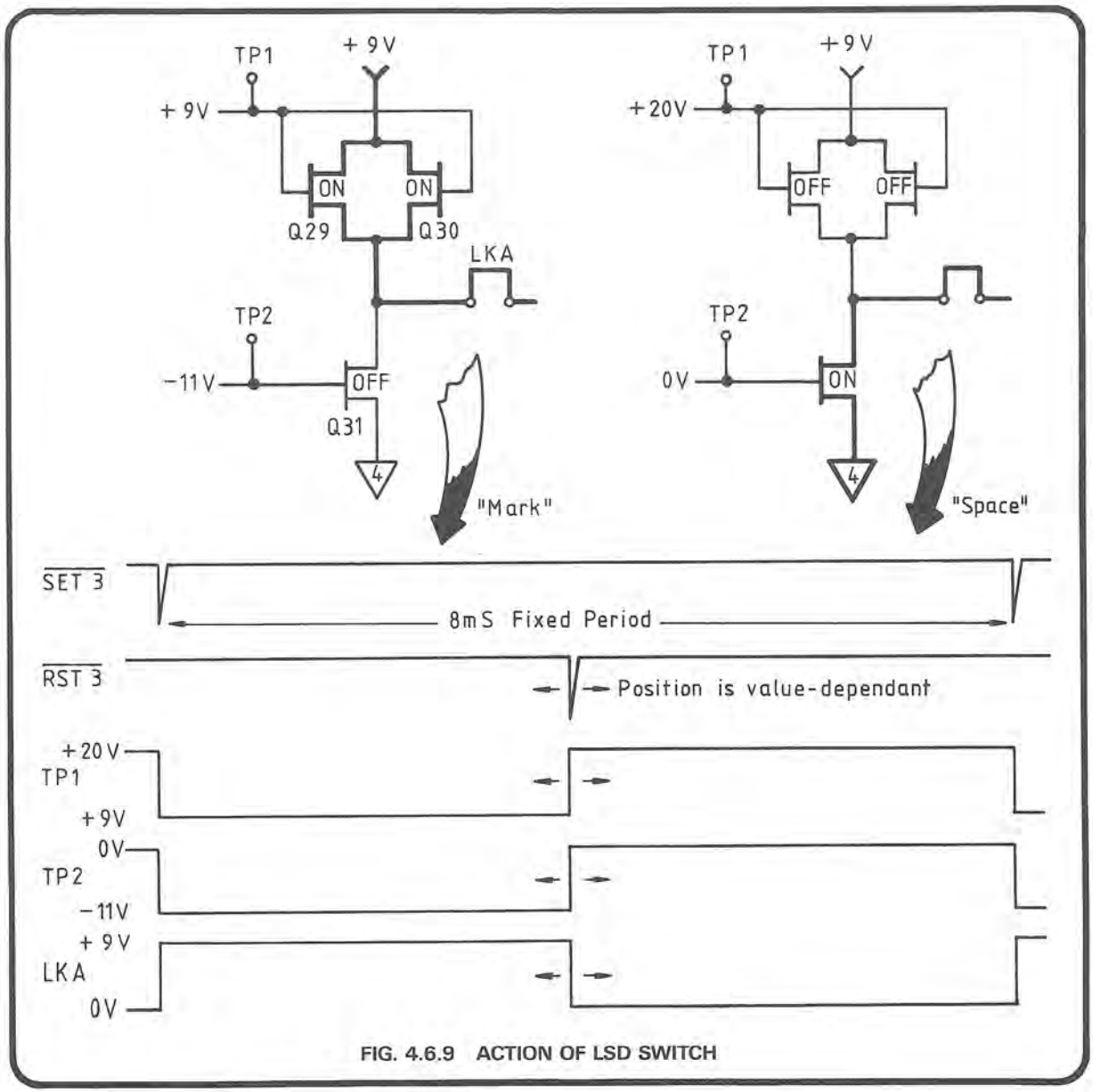


FIG. 4.6.9 ACTION OF LSD SWITCH

4.6.6.3 Offset Bias Amplifier

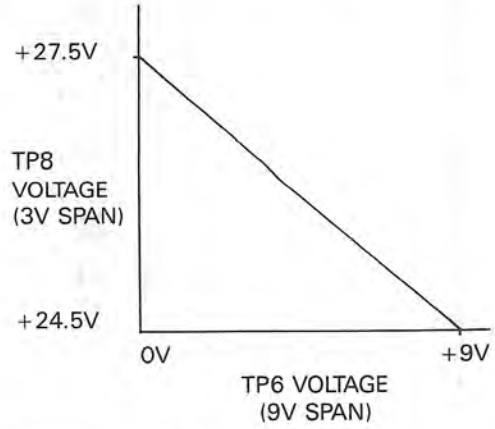
M20 performs a dual role:

(1) Its gain is set to $\frac{1}{3}$ by $\frac{R65}{R64}$

(2) Its output is level-shifted to provide an offset bias for summing (this allows the summed output to have a negative zero offset).

Also a small thermal coefficient zero correction is factory-preset (D10/R85).

M20 transfer function is approximately as follows:



The actual values are as set digitally in software, affecting the mark:period ratio of the JFET switches, using stored calibration constants.

4.6.7 Most-Significant-Bits Switching

(Circuit Diagram No. 430535 Page 7.4-1)

The large reference voltage (20.6V) and the need for higher resolution makes the MSB Switching circuitry more complex than for LSB; but the principle is the same: the set and reset pulse-timing adjusts the mark:period ratio of the square wave fed to the filter.

The arrangement used for the MSB switching satisfies two essential requirements:

(1) The charge and discharge path resistances for the 7-pole filter must be closely matched.

(2) The leakage current of the path switched off must be minimal.

Requirement (1) demands that the matched devices used in both paths are of the same type (P-channel JFETs have approximately 10 times the "on" resistance of N-channel types). But without the voltage standoff and leakage current shunt created by the guard switch, the pinch-off gate voltage for one of the paths would be high enough to generate gate-leakage current in excess of requirements (2).

4.6.8 Main And Guard Switches (Fig. 4.6.10)

(Circuit Diagram 430535 Page 7.4-1)

Refer to Fig. 4.6.10, in which only the Space to Mark (SET) state transfer a-b-c is shown.

(The Mark to Space (RESET) transfer is symmetrical c-b-a)

The switch driver flip-flops establish the voltage shown at TP3, 4 and 5 as controlled by the set and reset pulses. The drivers are ECL fast bistables, but note that Q19 and Q20 are included in the main switch driver as a level-shifter for Q32/Q35.

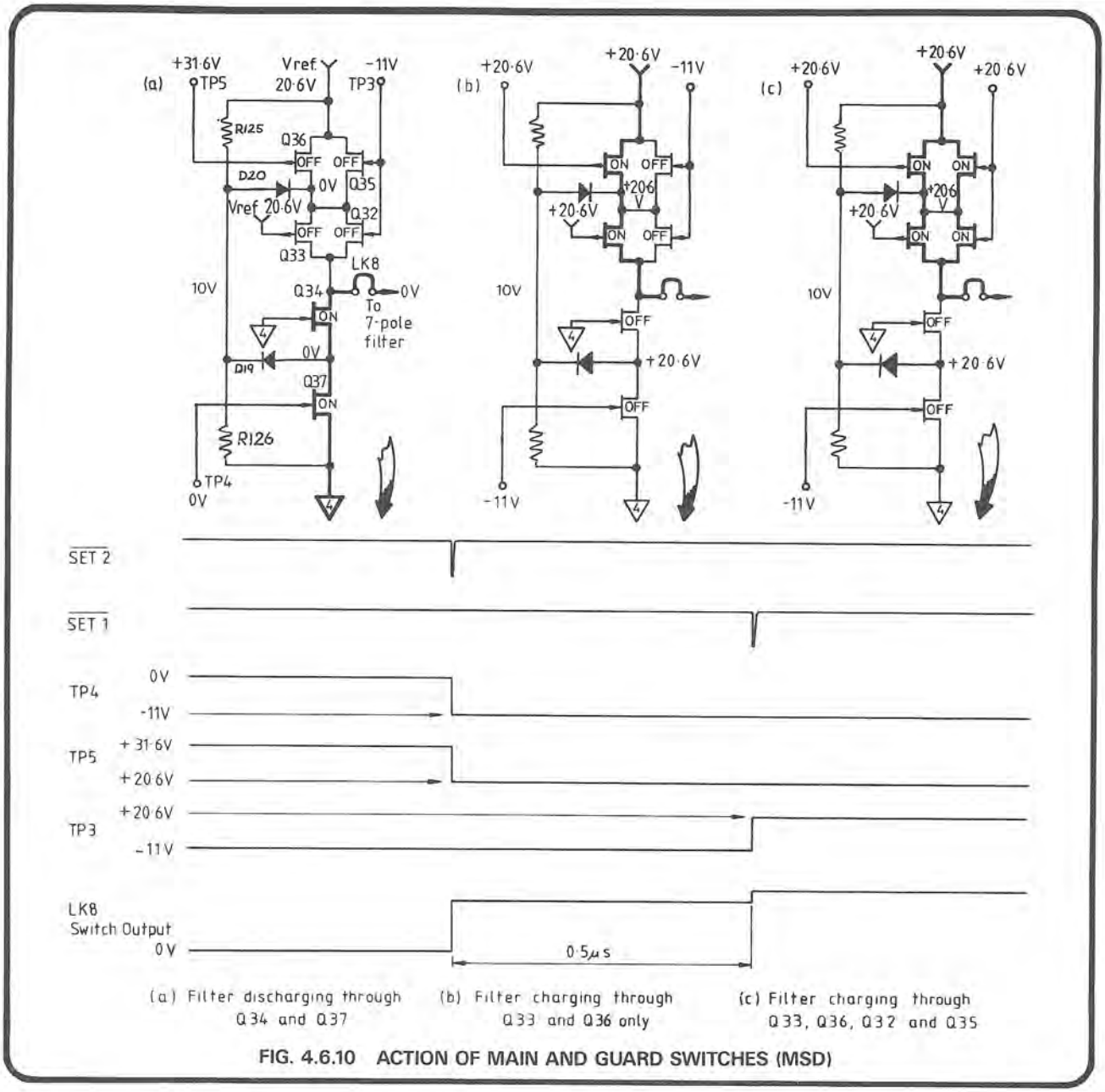


FIG. 4.6.10 ACTION OF MAIN AND GUARD SWITCHES (MSD)

4.6.8.1 Switch Timing
(Fig. 4.6.10)

$\overline{\text{SET 1}}$ pulse is delayed by 0.5μs after $\overline{\text{SET 2}}$ pulse, and $\overline{\text{RST 2}}$ is delayed by 0.5μs after $\overline{\text{RST 1}}$.

$\overline{\text{SET 2}}$ and $\overline{\text{RST 2}}$ pulses control the timing of Q36, Q33, Q34 and Q37 in the main switch (TP4 and 5).

$\overline{\text{SET 1}}$ and $\overline{\text{RST 1}}$ pulses turn Q35 and Q32 on and off (TP3). Because of the 0.5μs delays, Q35 and Q32 conduct only during the time that Q36 and Q33 are also conducting.

4.6.8.2 Filter Discharge Path

In Fig. 4.6.10(a) the switches are in "space" state:

Q37 and Q34 are turned on by TP4 at OV, to provide the filter discharge path.
Q33 and Q36 are turned off by TP5 at +31.6V,
Q32 and Q35 are turned off by TP3 at −11V.

The filter discharges via resistor R79 and FETs Q34 and Q37. During both Mark and Space periods, R79 (78.7kOhms) is a major determinant of the 7-pole filter charge and discharge currents. Because in 'space' state the 'On' resistances of Q34 and Q37 (3-5 Ohms each) are very small in comparison, the potential at link B can be regarded as zero when considering the effects of the other switching voltages.

Reverse leakage currents in JFET junctions are normally of the order of a few picoamps unless the junction voltages are much in excess of 20V. To control leakage effects from the four JFETs which are turned off, the cathode of diode D20 is connected to the common junction of the four devices. Its anode is returned to the junction of R125 and R126, close to +10V.

The reverse leakage characteristics for a J108 FET (Q35 and Q32) are generally several times heavier than for a J174 (Q36 and Q33). This means that in this switch, the leakage currents via Q35 and Q32 out of the common junction are 4-5 times greater than those entering via Q36 and Q33.

The net leakage out of the junction holds D20 slightly in forward bias, so that its cathode cannot rise above about +10.3V, when the four FETs are turned off in 'space' state. Thus D20 guards the 'buffer' FETs Q33 and Q32 from the effects of the relatively high voltage on Q36 gate. The effects of the buffer FETs' own leakages on the voltage at the filter input can be regarded as negligible, because Q33 leakage currents towards LKB are virtually balanced by those away via Q32.

4.6.8.3 Filter Charge Path

To preserve linearity over the full range of Mark:Period ratios, the filter charging path time constant must closely match that of the discharge path. Q35 and Q32 are factory-selected to form a matched set with Q34 and Q37, all J108 N-channel FETs (The 'on' resistance of P-channel FETs in a true complementary switch would be much higher: 30-40 Ohms). Nevertheless, to avoid high voltages being developed across Q35/Q32 when changing between states (causing excessive leakage), P-channel FETs are employed. Q36/Q33 are switched on before (and switched off after) Q35/Q32.

Fig. 4.5.10(b) shows this intermediate state after $\overline{\text{SET 2}}$ and before $\overline{\text{SET 1}}$, and Fig. 4.6.10(c) shows the fully-conducting state after $\overline{\text{SET 1}}$. Note that for descriptive purposes, the second step on LKB waveform is heavily exaggerated, and is not readily viewed on an oscilloscope. The slightly longer charging time-constant during this half micro-second, due to the higher resistance of Q36/Q33, is not sufficient to disturb the linearity of the filter in excess of specification.

The voltage between TP4 and LKB during 'mark' state is some 31 volts. In the absence of D19, an adverse voltage distribution could cause excessive reverse leakage in Q37. D19 controls the distribution by limiting the voltage at its cathode to about +10V, constraining Q37 source-gate voltage to a tolerable 20.5V.

4.6.9 7-Pole Filter

(Circuit Diagram 430535 Page 7.4-1)

M26, M28, M32, Q41 and Q42, together with associated capacitors and resistors, form a 7-pole Bessel filter in three active elements; providing approximately 135dB of attenuation at the 125Hz switching frequency and increasing at a rate of 140dB/decade. This allows sufficient bandwidth to avoid excessive settling time while reducing the output ripple to within instrument specification. Q41 and Q42 source-followers provide input bias currents for M26 and M28 from the 15V supplies, and buffer the line from bias-current effects. M32 bias-current effects are insignificant.

The filter output at TP13 is fed to a buffer amplifier as '+Ve SUMMING AMP', to be subsequently added to the output from the Least-Significant Switch offset-bias amplifier. R101 and C51 prevent spikes from the chopper-stabilized buffer amplifier being fed back into the filter.

4.6.10 Summing Amplifier

(Circuit Diagram 430535 Page 7.4-3)

4.6.10.1 '+VE SUMMING AMP' Buffer

M33, M34 and Q44 buffer the '+Ve SUMMING AMP' voltage output from the 7-pole filter (this is proportional to the Mark/Period ratio of the 13 most-significant bits of the binary word which defines the instrument output value demand).

M33 is a high-gain, chopper stabilized integrator with a bandwidth of approximately 10Hz, and Q44 provides additional bandwidth for rejection of HF common-mode noise.

M35, D14, D15, Q48 and Q49 generate boot-strapped supplies to preserve full dynamic-range linearity. Q46 and Q47 establish 3mA constant-current drives for D14 and D15.

The whole amplifier acts as a voltage-follower, M34/Q45 providing the output drive, buffering the output of M33 and Q44. The output is delivered as 'Hi O/P' to the AC Assembly via RL2 (RL1 being permanently de-energized in the 4200). The output is sensed in the AC Assembly to account for the volts-drops in the connecting circuit. The sense feedback voltage 'Hi SENSE' is applied to the inverting input of the whole buffer via R98.

For a zero count in the MSB comparator, the filter output voltage is approximately +3.2mV, and a full count of 8191 would produce +20.6V. These are the voltages which are developed at the buffer output.

4.6.10.2 '–VE SUMMING AMP' Buffer

M38, M39 and Q51 buffer the '+Ve SUMMING AMP' voltage output from the Offset Bias Amplifier derived from the 3-pole filter (this is proportional to the Mark/Period ratio of the 12 least-significant bits of the binary word which defines the instrument output value demand).

The dynamic range of the filter output voltage was originally defined by the Reference Buffer (8.83V) for efficient operation of the FET switching circuitry.

It was scaled in the Offset Bias Amplifier to give +27.5V for an LSB comparator count of zero (from approx. +1.1mV at TP6), and +24.5V for a full count of 4095 (from +8.83V at TP6). It now needs to be scaled down so that its proportionality to the '+Ve SUMMING AMP' dynamic range is correct.

R99 and R100 attenuate the '–Ve SUMMING AMP' input voltage by a factor of 0.8545×10^{-3}. At zero count, +27.5V is reduced to +23.5mV, and at full count +24.5V reduces to +20.9mV. These are the extremes of voltage developed at the buffer output.

The whole amplifier acts as a voltage-follower, but without bootstrapped supplies (the small input voltage dynamic range of approx. 2.5mV does not warrant it). Otherwise the circuit is identical to the '+Ve SUMMING AMP'. M39/Q52 provide the output drive, buffering the output of M38 and Q51. The output, 'Lo O/P', is delivered via RL2 to be sensed in the AC Assembly. The sense feedback voltage 'Lo SENSE' is applied to the inverting input of the whole buffer via R127.

4.6.10.3 Summing

On the AC Assembly, the outputs from the two buffers are summed by defining the 'Lo O/P' level as 'Reference Common' (Common 2C), and the 'Hi O/P' level as 'REF +Ve'. Thus the voltage at 'REF +Ve' with respect to 'Reference Common' will always be 'Hi O/P' minus 'Lo O/P' at their current values.

The reference voltages and reference division circuitry are chosen to allow for software calibration adjustments, so the span of the summing amplifier overlaps the possible full Span of 0 to 19.999999V at both extremes:

With an overall 25-bit count of zero in the comparators, REF+Ve is +3.2mV minus +23.5mV, a negative overlap of −20.3mV.

At overall full count, REF+Ve is+20.6V minus +20.9mV, approximately+20.58V.

4.6.10.4 Bipolar Reference Switching

Relays RI1 and RL2 are used in DC calibrators for polarity reversal. This is not necessary in the 4200, and during operation RL1 is always de-energized, while RL2 is energized. Thus all outputs from the summing buffers are fed to the AC Assembly via RL2.

4.6.11 Quasi-Sinewave Generation

4.6.11.1 Quasi-Sinewave Reference

In the Sense/Reference comparator, a considerable advantage is gained by comparing AC with AC. (If AC sense were compared with DC reference, small DC offsets would be magnified, leading to 'DC turnover' errors). The AC waveform used as reference is constructed in ten steps by a digitally controlled switching network, based on the DC reference as its peak value. It has been given the name 'Quasi-Sinewave'.

The comparator produces an error to drive the VCA, which is proportional to the difference in 'Mean Square' values, and is driven to zero by the action of the Output-Sense loop. At zero error the RMS value of the comparator's sense input has thus been adjusted by the loop to be equal to the RMS value of its reference input.

On the 1V Range there is neither amplification nor attenuation in the Output-Sense loop. The quasi-sinewave is designed so that with the 1V Range selected, its RMS value is equal to the voltage demanded on the front panel OUTPUT display, (with small, controlled adjustments for calibration).

On higher ranges, decades of amplification are switched in to set the output to the demanded voltage. Switched decades of attenuation reduce the sensed sinewave back to the 1V-Range level for comparison with the quasi-sinewave.

On millivolt ranges the 1V sense loop is used with precise, passive, decade attenuators reducing the output to the values on the display.

On current ranges, the current reference is derived from either the closed 1V or 10V Range Output/Sense loop.

Therefore on all ranges the Output/Sense loop gain is driven to a magnitude of 1, so that the VCA and the comparator both operate at 1V Range levels.

4.6.11.2 4200 DC Reference Scaling

The Reference Divider hardware is common to several instruments. In DC calibrators, the basic voltage range is usually the 10V Range, with 100% overrange at Full Scale. In these cases the full span of reference values is employed, generating the resolution necessary to accommodate the DC accuracy available.

The same accuracy is not available for AC, so the high resolution is not necessary. Moreover, the linearity of the analog circuitry is improved by using a smaller dynamic range in the reference circuits. So in the 4200 the 1V Range is the basic range, and the software scales its demanded value accordingly.

In the 4200 the sensed output is compared against the quasi-sinewave whose characteristics match those of the sensed sinewave. To construct the quasi-sinewave, the DC reference voltage needs to be set at its peak value.

The microprocessor program imposes, in software, the scaling factors which establish the reference voltage at the peak value of the quasi-sinewave. Thus the full span of the 25-bit comparator, and hence the possible dynamic range of the DC reference, are realized only at times when the Reference Divider itself is being calibrated. Before initial calibration, the maximum obtainable reference voltage is slightly greater than 2.8V, and the minimum is slightly less than 125mV. This overlaps the peak voltages of the quasi-sinewaves corresponding to the maximum and minimum values of sensed output; giving a margin for accurate calibration, from digital gain factors held in the non-volatile calibration memory.

4.6.11.3 DC Reference Voltage Values

As mentioned earlier, the DC Reference is used to establish the amplitude of the quasi-sinewave. When the 1V Range is selected, the reference is set to the peak value of the quasi-sinewave, which is 1.397 times the demanded RMS (sinewave) voltage output of the instrument. In normal use, therefore, the reference voltage is adjusted by front panel OUTPUT display selections; between 125.7mV (for 0.9V selection) and 2.79V (for 1.999999V selection), plus or minus any user-calibration corrections.

On higher and lower ranges, analog range switching in the sense amplifiers scales the sense voltages for comparison with the same voltage span of quasi-sinewaves.

4.6.11.4 Reference Inverter

(Circuit Diagram 430447 page 7.7-2)

The quasi-sinewave is derived by a specific form of D-A converter, selecting voltages from a divider network. Because negative values are required, the divider is strung between positive and negative reference voltages; the unity-gain Reference Inverter generates the negative reference 'REF-Ve' by inverting 'REF+Ve'.

M1, M2 and Q1 perform the inversion. M2 generates the bandwidth necessary for amplitude switching operations, while chopper-stabilized integrator M1 removes DC offsets, always referring the inverter output to Common-2C. To compensate for RMS value changes in the quasi-sinewave (due to switching errors arising from frequency changes), feedback from the quasi-sinewave is applied via R1, C4, R4 and C5. Q1 provides the output drive to the quasi-sinewave generator.

4.6.11.5 Quasi-Sinewave Generator

(Circuit Diagram 430447 page 7.7-3)

The SYNCØ input to M11 RESET is a decoded address which, when set to logic-1, disables the Quasi-sinewave sequence counter M11. It is permanently held at logic-Ø in the 4200, to enable the quasi-sinewave for both AC Voltage and Current functions.

The quasi-sinewave is generated at a frequency determined by the Frequency Synthesizer 100Hz-4kHz output (para 4.7.3.3 describes the synthesis), clocking the decade counter M11 via J7.50. This continuously recycles M11 in ascending count through $Q_Ø$ to Q_9, ten clocks constituting one cycle of the quasi-sinewave. So the quasi-sinewave runs at a frequency of between 10Hz and 400Hz, indeed the carry C_{out} of M11 returns to the Synthesizer via J7-51 to be selected as the reference frequency for the 100Hz (10-330Hz) frequency range.

With increase of frequency range, the difference between the frequencies of output and quasi-sinewave increases in decade steps. As the comparison of sense and quasi-sinewave signals is performed at mean-square DC levels, this difference theoretically does not matter, so long as the signal is at an exact multiple of the quasi-sinewave frequency. However, to achieve optimum operation of the Sense/Reference comparator, the zero crossings of the quasi-sinewave are synchronized to occur coincident with a sense signal zero crossing.

Synchronization is achieved by the clock input to M9, controlling the timing of the quasi-sinewave switches M8 and M14. Using the same clocks, M11 and M10 transit times prevent the data from arriving at M9 'D' inputs until the data already established there by the previous clock pulse has been latched at its outputs. Thus data ripples through M11 and M9 at successive clock pulses.

The ripple rotates the data by one clock period and would, if left uncorrected, put the switching out of sequence. The arrangement of the connections between M11 outputs and M9 data inputs, combines appropriate outputs so as to correct the switching pattern. The table in Fig. 4.6.11 demonstrates the rotation of 1 clock period; the quasi-sinewave steps being labelled at M9 inputs and outputs.

The quasi-sinewave is output to the transfer switching input to the Sig/Ref comparator at M16-1. The action of the transfer switch is described in section 4.14.

A second output is filtered and fed back as compensation to the Reference Inverter as described earlier (para 4.6.11.4).

Step	0	1	2	3	4	5	6	7	8	9
M11 Output at Logic-1:	Q_9	$Q_Ø$	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	Q_8
M10 Output pin at Logic-1:	4	11	—	11	4	10	3	—	3	10
M9 Output pin at Logic-1:	O_1	O_4	O_5	O_4	O_1	O_2	$O_Ø$	O_3	$O_Ø$	O_2
Switch Energized M8 pin: / M14 pin:	5 / —	6 / —	13 / —	6 / —	5 / —	— / 5	— / 6	— / 13	— / 6	— / 5
Step Voltage Fed to M16-1:	+0.42	+1.16	+1.397	+1.16	+0.42	−0.42	−1.16	−1.397	−1.16	−0.42

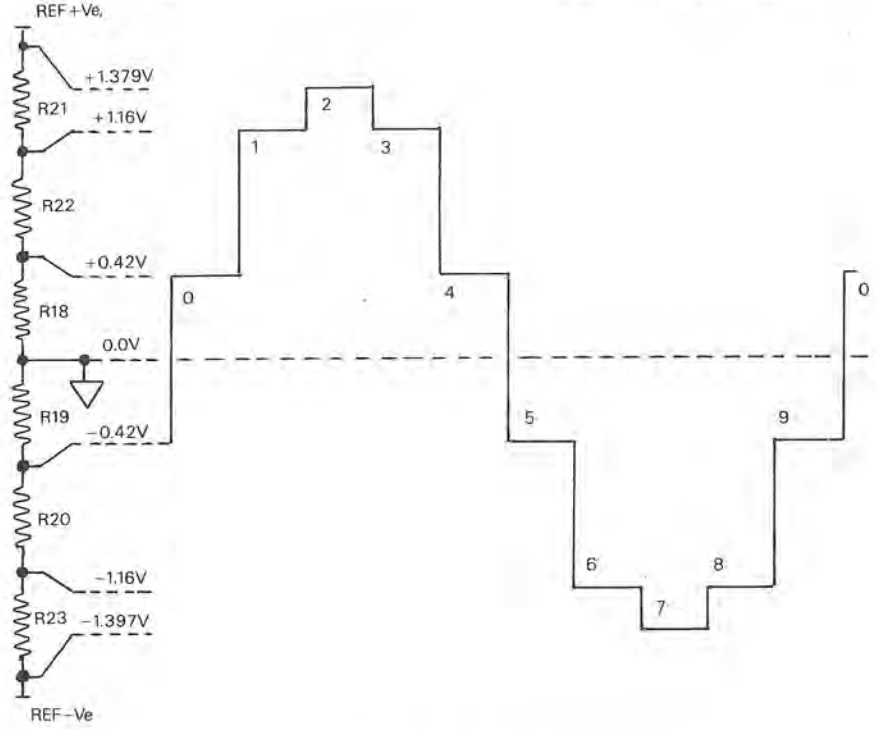


FIG. 4.6.11 QUASI-SINEWAVE GENERATION

4.7 DIGITAL FREQUENCY SYNTHESIZER
(Fig. 4.7.1)

4.7.1 General

Users normally set the 4200 operating frequency by a combination of 'FREQUENCY RANGE' and 'FREQUENCY' display selections. These are memorized by the CPU and translated into two binary control words:

'$FREQR_{2\text{-}\emptyset}$', a three-bit word, five of whose codes represent the five frequency ranges.

'$FREQ_{8\text{-}\emptyset}$', a nine-bit word whose value 'n' defines the chosen frequency with respect to the selected frequency range.

Users can select a frequency by means other than pressing a FREQUENCY RANGE key and setting a frequency on the display; for example by using 'Store', 'Spot F' or the IEEE488 digital interface. But regardless of the selection method, the CPU will always compute the two binary words, which then synthesize the selected frequency in the Sine-Source Assembly.

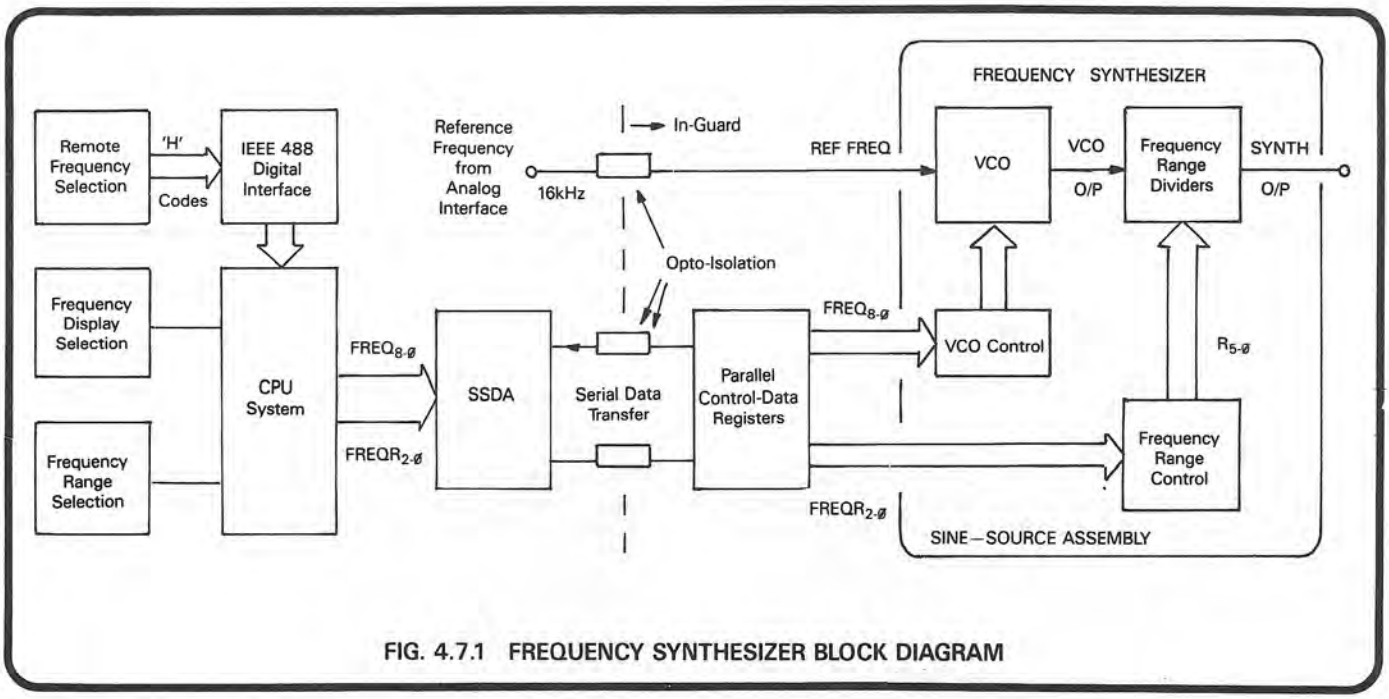


FIG. 4.7.1 FREQUENCY SYNTHESIZER BLOCK DIAGRAM

Both words are passed into guard via the SSDA, and latched at the outputs of the Reference Divider Parallel Control registers. A 16kHz reference frequency is also taken into guard, to be divided by two to 8kHz in the Sine-Source.

After entering the Sine-Source assembly, $FREQ_{8\text{-}\emptyset}$ effectively multiplies the 8kHz reference by 'n' to determine the frequency of a Voltage Controlled Oscillator (VCO). The VCO frequency (signal 'VCO O/P') is input into a series of frequency dividers, whose ratios are set by $FREQR_{2\text{-}\emptyset}$. The division ratios are chosen so as to make the dividers generate the Frequency Synthesizer output signal ('SYNTH O/P') at the user-selected frequency.

The purpose of the synthesizer is to provide an accurate frequency reference for the quadrature sinewave oscillator. The oscillator is approximately tuned by selection of circuit constants using '$FREQR_{2\text{-}\emptyset}$' and '$FREQ_{8\text{-}\emptyset}$'.

'SYNTH O/P' acts as the reference in the phase comparator of a Phase-Locked Loop, controlling the frequency of the main Quadrature Sinewave Oscillator to an accuracy determined by the crystal oscillator.

4.7.2 Voltage Controlled Oscillator

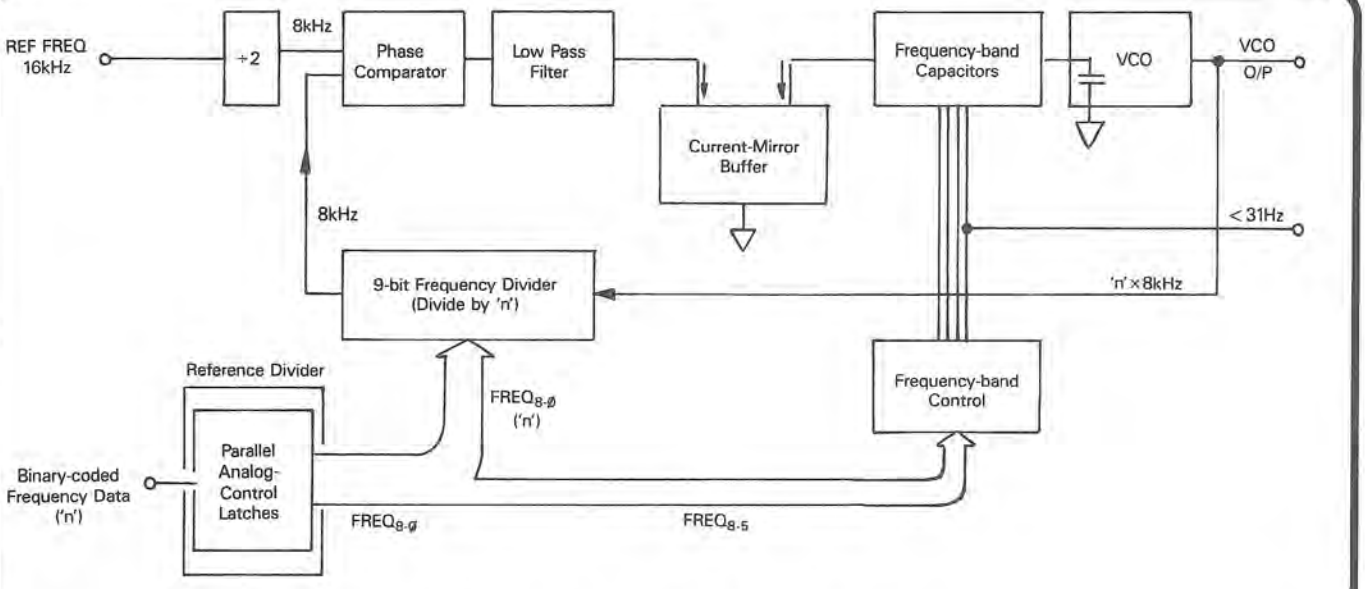


FIG. 4.7.2 VCO BLOCK DIAGRAM

4.7.2.1 Generation of 16kHz Reference

(Circuit Diagrams 430570 page 7.3-2, 430535 page 7.4-5 and 430446 page 7.6-4)

On page 7.3-2, the 16kHz is picked off M16-14 in the Analog Interface and buffered out on page 7.3-1 as '16kHz(OG). It arrives on the Reference Divider (page 7.4-5) at J4-104, passing into guard via opto-isolator M3. It is gated with 'BARK' and 'DISABLE REF FREQUENCY' in M24, filtered by R86/C38 to reduce harmonics from the transmission path, and is sent via the Mother Assembly to J6-53 on the Sine-Source Assembly (page 7.6-4).

Schmitt-trigger M14 inverts the 16kHz into a symmetrical squarewave, which is then applied as clock to M13a, a bistable connected to divide by two. The resulting 8kHz squarewave is taken as the reference frequency for phase comparator M12. Note that in this configuration the SIG input of M12 is used for the reference, and the divided VCO output signal is applied to the REF input. This is necessary to provide the correct sense in the phase control element M50, because of the inversion of integrator M11.

4.7.2.2 Squarewave Generation by the VCO

The VCO is a discrete-component ECL relaxation oscillator generating an output of frequency 'n' x 8kHz. Its natural frequency is dependent on:

a. the value of the timing capacitor C2 (or C2 plus one of C3-C6 in parallel),

b. the value of its continuous discharge current through the phase control element (current mirror M50), and

c. the value of its charging current through Q2 on alternate half cycles (4.7mA).

Consider C2 fully discharged. Q4 is off, so the 4.7mA from Q6 is all passing through Q5. The collector voltage of Q4 is close to the positive rail, and is emitter-followed to the base of Q5 via R9, holding Q5 on. Also, because Q3 is turned off by Q4 collector voltage, Q2 is turned on at its emitter, passing 4.7mA into C2 and the current mirror M50.

C2 charges until Q4 turns on at its base-emitter threshold. Cumulative Schmitt action passes the fall at Q4 collector to the base of Q5, ensuring a rapid transition between states so the 4.7mA is transferred from Q5 to Q4. Q3 turns on, its emitter falling quickly to cut Q2 off, so the charging path to C2 etc. is interrupted.

M50 continues to discharge C2, whose voltage falls slowly until Q4 starts to cut off again. The cumulative action is repeated to turn Q2 on, recharging C2. The cycle of charge and discharge continues, generating 'VCO O/P' squarewaves at buffer Q12 emitter.

4.7.2.3 Coarse Frequency Control

(Circuit Diagram 430446 Page 7.6-4, and Fig. 4.7.2)

At any time, only one of the capacitors C3, C4, C5 and C6 can be connected in parallel with C2, by conduction of its associated transistor. This splits the frequency range of the VCO into five bands, governed by the four most-significant bits of the frequency control word $FREQ_{8-\emptyset}$ acting on M8. The association is shown in Table 4.7.1, note that the VCO frequency bands quoted in the table are correct only because the VCO is under the fine control of comparator M12, within the phase-locked loop.

$FREQ_{8-5}$ bits 8 7 6 5	Range of 'n' Values	M8 Outputs at Logic-1	C2-C6 Selection	VCO Frequency Band (kHz)
0 0 0 0	10 to 31	$X_\emptyset$	C2 and C6	80 to 248
0 0 0 1	32 to 63	X_1	C2 and C5	256 to 504
0 0 1 X	64 to 127	X_{3-2}	C2 and C4	512 to 1016
0 1 X X	128 to 255	X_{7-4}	C2 and C3	1024 to 2040
1 X X X	256 to 500	NONE	C2 only	2048 to 4000

TABLE 4.7.1 COARSE FREQUENCY CONTROL

4.7.2.4 Fine Frequency Control

(Circuit Diagram 430446 Page 7.6-4, and Fig. 4.7.2)

In the following description, capacitors C3, C4, C5 and C6 are ignored, but references to C2 should be read as including the appropriate additional capacitor.

The VCO output is fed back to M12 phase comparator via M9 and M13b, which are connected to act as a 9-bit frequency divider. Because the divider is controlled by $FREQ_{8-\emptyset}$, the VCO output frequency is always divided by 'n' before being applied to the REF input of the comparator. The output from the comparator will only be zero if the frequency fed back to M12-6 is 8kHz (ie. the VCO frequency is n×8kHz), and in phase with the 8kHz REF FREQ at M12-3 (TP14).

The output from M12 is integrated by M11 to drive a DC current into the current mirror M50. The current mirror has a gain of two, its output current being drawn from the charge on C2. During the half-cycles of the VCO oscillation when C2 is being charged, the mirror obtains its current from Q2 conduction.

The phase control loop seeks to phase-lock the two inputs to the comparator. If they are in phase, the comparator output is at high impedance ('TRISTATE'). In this condition the integrator capacitors C16 and C18 have no charge or discharge path, so M11's extremely high gain maintains the charge on the capacitors, and the voltage at TP6. M11 supplies the input current for M50, the mirror continues to draw the same discharge current from C2, so the frequency of VCO oscillation remains constant. Thus the loop stabilizes only when the frequency divided by 'n' from the VCO output is in phase with (and therefore at the same frequency as) the reference 8kHz.

In stable operation, therefore, the loop maintains VCO oscillation at n×8kHz, and the feedback dividers reduce this frequency by a factor of 'n' to 8kHz.

Any disturbance in the loop will generate corrections to restore zero phase difference at the inputs of M12. Frequency deviations are therefore detected at an early stage as phase changes, giving a measure of 'phase advance' correction.

4.7.2.5 'INHIBIT' (VCO Off)

The VCO can be switched off by a logic-1 of OV at the base of Q11 (INHIBIT signal). This originates in the CPU system, setting $FREQR_{2-\emptyset}$ code to 111 (a non-existent 'R7' range). This INHIBIT signal is not used in the 4200.

4.7.2.6 VCO Supply Rail Protection

To prevent VCO oscillations appearing on the ± 15V power rails, which also supply the integrator M11 and current mirror M50, the positive rail is heavily decoupled, regulated by Q8, and all devices whose currents are likely to disturb the rails are supplied through constant current sources (Q1, Q6, Q9 and Q13).

4.7.2.7 VCO Output

The VCO, integrator and current mirror operate from the ± 15V supplies. The phase comparator, divide-by-'n' counter and the frequency dividers which follow the VCO, all operate from the in-guard logic supplies of 0V and −15V. The VCO output from Q12 emitter is therefore limited by D1 to logic supply levels. A conversion from logic supply levels back to ± 15V levels is accomplished at the input to the integrator M11, as TP31 pulses are negative at M11 input.

D1 is a Schottky hot carrier diode of reverse capacitance approx. 2pF to avoid distorting the high frequency squarewaves it is limiting (for 1MHz 4200 output, the VCO oscillates at 4MHz).

The output is passed through R12 to avoid loading the VCO, and then fed as 'VCO O/P' to the frequency dividers at M5-9 (page 7.6-5)

4.7.3 Frequency Range Dividers
(Fig. 4.7.3)

As mentioned earlier in para 4.7.1, the purpose of the synthesizer is to provide an accurate frequency reference for the quadrature sinewave oscillator. The VCO frequency (signal 'VCO O/P') is input to a series of frequency dividers, whose ratios are set by '$FREQR_{2\text{-}\emptyset}$', so as to make the dividers generate the selected frequency as 'SYNTH O/P'. $FREQR_{2\text{-}\emptyset}$ is a three-bit word, five of whose codes represent the five frequency ranges.

A second purpose is to clock the Quasi-Sinewave Generator in synchronism with the synthesizer output (and hence with the main quadrature sinewave oscillator output). The synthesizer frequency is a multiple of the Quasi-Sine frequency, except on the 100Hz frequency range, where they are both at the same frequency. Thus the divider ratios are also chosen to generate the correct frequencies for the quasi-sinewave clock, for each frequency range selected.

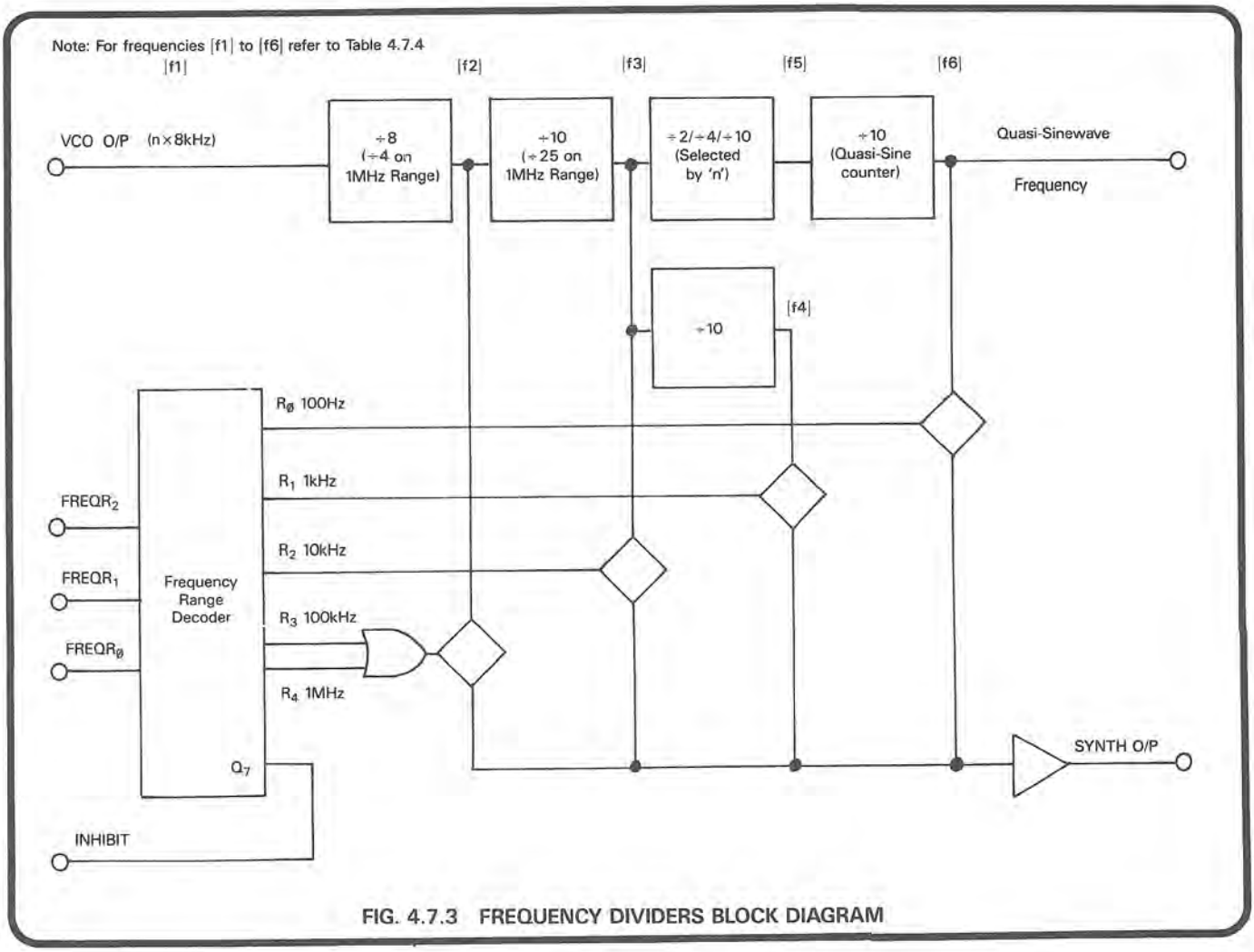


FIG. 4.7.3 FREQUENCY DIVIDERS BLOCK DIAGRAM

4.7.3.1 Divider Ratios
(Circuit Diagram 430446 Page 7.6-5)

Binary/BCD Divider M5 is set for binary division by M5-2 and M5-10 set to Logic-Ø. Conversely, M1 is set for decimal division by M1-2 and M1-10 at Logic-1.

BCD counter M2 is set to count up, by M2-10 at Logic-1. Its $\overline{\text{CARRY OUT}}$ signal at M2-7 is at one tenth of its clock frequency, and its Q1 output on M2-6 is at half its clock frequency. Flip-flop M4 is connected to divide its clocks by two.

Multiplexer M6 selects the appropriate source frequency to clock the Quasi-Sinewave generator. In particular, on the 100Hz Range it selects the $\overline{\text{CARRY OUT}}$ from M2, which is divided by 10 in the quasi-sinewave counter, and returned via J6-51 to be used as SYNTH O/P.

4.7.3.2 Ratio Selection by Frequency Range
(Fig. 4.7.3 and Table 4.7.2)

The frequency range selection word $FREQR_{2\text{-}\emptyset}$ is decoded by M29 into five range lines $R_{4\text{-}\emptyset}$. These lines perform the following functions:

a. They switch ranges in the quadrature sinewave oscillator by relay RL1-RL8 selection of integrator capacitors (page 7.6-1);

b. They switch ranges in the Cosine Squarer output filter (page 7.6-2);

c. They adjust the division ratios of Frequency Range Dividers M5 and M1 (page 7.6-5) for range R4 (1MHz Range); and

d. They select appropriate outputs from the Frequency Range Dividers (page 7.6-5).

Functions (a) and (b) are described later in Section 4.8. In this description we are concerned only with functions (c) and (d).

Table 4.7.2 shows how frequency range switching derives the synthesizer output frequencies by selecting the appropriate outputs from the dividers. Note that except for the 1MHz Range R4, the ratios of individual dividers are not altered.

On the 100Hz Range RØ the overall division ratio of 8000 is achieved as for the 1kHz Range, but with a further division by 10 in the quasi-sinewave counter M11 on the AC Assembly.

On the 1MHz Range R4, the division ratio of M5 is changed from 8 to 4. The DP_A inputs M5-5 and M5-6 are primed to Logic-1 and Logic-Ø respectively, whereas on all other ranges the priming is reversed. Range R4 also alters the division ratio of M1 from 10 to 25, by changing its priming bit-pattern, to correct the quasi-sinewave frequency; but as the synthesizer output is taken through M10-4/3 from M5 output, the adjustment to M1 does not affect the SYNTH O/P frequency.

FREQ. RANGE	FREQUENCY DISPLAY	VCO OUTPUT (n × 8kHz)	OVERALL DIVISION RATIO	RELEVANT DIVIDER RATIOS				QUASI-SINE CLOCK FREQUENCIES	SYNTHESIZER OUTPUT
				M5	M1	M2	M11* (AC PCB)		
	Hz	kHz						(J6-50)*	(J6-52)
100Hz (RO)	10-63 64-127 128-330	80-504 512-1016 1024-2640	8000	8 8 8	10 10 10	10 10 10	10 10 10	Hz 100-630 640-1270 1280-3300	Hz 10-63 64-127 128-330
1kHz (R1)	0.30k-0.63k 0.64k-1.27k 1.28k-3.30k	240-504 512-1016 1024-2640	800	8 8 8	10 10 10	10 10 10		kHz 1.5-3.15 1.6-3.175 1.28-3.3	Hz 300-630 640-1270 1280-3300
10kHz (R2)	3.0k-6.3k 6.4k-12.7k 12.8k-33.0k	240-504 512-1016 1024-2640	80	8 8 8	10 10 10			kHz 1.5-3.15 1.6-3.175 1.28-3.3	kHz 3.0-6.3 6.4-12.7 12.8-33.0
100kHz (R3)	30k-63k 64k-127k 128k-330k	240-504 512-1016 1024-2640	8	8 8 8				kHz 1.5-3.15 1.6-3.175 1.28-3.3	kHz 30-63 64-127 128-330
1MHz (R4)	0.30M-1.00M	1200-4000	4	4				kHz 1.2-4.0	kHz 300-1000

* Quasi-sine counter M11 on the AC Assembly divides VCO output at all frequencies, but contributes to SYNTH O/P only on the 100Hz Frequency Range.

TABLE 4.7.2 SYNTHESIZER OUTPUT—DIVISION RATIOS

4.7.3.3 Frequency Synthesis for the Quasi-Sinewave Generator
(Fig. 4.7.3 and Table 4.7.3)

The 100Hz frequency range uses the quasi-sinewave counter as a divider in deriving its SYNTH O/P frequency. Although not directly related to the frequency of the SYNTH O/P signal on other ranges, the quasi-sinewave frequency is deliberately derived in the synthesizer, so that the zero-crossings of its waveform can be synchronized at a time when the main sinewave is also crossing zero. (The main sinewave, of course, can be at a high multiple of the quasi-sinewave frequency.)

The quasi-sinewave frequency is held to a maximum of 330Hz (400Hz on the 1MHz range), to limit errors due to high harmonics. The 1MHz frequency range contains only one frequency band, but the other four ranges are each divided into three bands, corresponding to the three most significant bits of the frequency word $FREQ_{8-Ø}$.

Table 4.7.3 illustrates the way that the three bands affect the quasi-sine frequencies. Note that division ratios of 2, 4 or 10, by M2 and M4a, are selected by $FREQ_6$, $FREQ_7$, and $FREQ_8$ at M6 pins 11, 10 and 9 respectively. Frequency range RØ at M7-2 ensures that on the 100Hz range, the divide-by-10 output of M2 is always selected, regardless of the state of these three bits.

To ensure that the Divide-by-2 outputs of M2 and M4a are locked into the correct phase for quasi-sinewave generation, a 'CHOP LOCK' synchronizing signal is derived from the quasi-sinewave counter 'Q_0' output, entering at J6-75. Following DC-restoration from ±8V supplies to the normal 0V/−15V logic supplies by C20/D3/R15/M7, the signal is applied to M4a SET input, and M2 RESET input.

For all 4200 frequency ranges, the '100-5kHz' quasi-sinewave generator clock is passed to the AC Assembly via J6-50 and the Mother Assembly. This output is level-shifted by Q42, to the ±8V supplies which are used in the quasi-sinewave generator circuitry. Quasi-sinewave synchronizing signal 'SYNC Ø (IG)' (which was transferred into Guard by M2 on the Reference Divider), is input to the Sine-Source Assembly on J6-48 to be similarly level-shifted by M43, before being passed to the AC Assembly via J6-49.

For other details of the quasi-sinewave generator refer to para 4.6.11.

FREQ. RANGE	FREQUENCY DISPLAY Hz	FREQUENCIES SYNTHESIZED IN SINE-SOURCE ASSEMBLY				QUASI-SINE FREQUENCY (& J7-51) Hz	4200 OUTPUT FREQUENCY Hz
		VCO OUTPUT (n×8kHz) kHz	DIVIDER RATIOS for QUASI-SINEWAVE M5 M1 M2 M4a	OVERALL DIVISION RATIO	QUASI-SINE CLOCK FREQUENCY (J7-50)		
100Hz (RØ)	10-63 64-127 128-330	80-504 512-1016 1024-2640	8 10 10 – 8 10 10 – 8 10 10 –	800 800 800	Hz 100-630 640-1270 1280-3300	10-63 64-127 128-330	10-63 64-127 128-330
1kHz (R1)	0.30k-0.63k 0.64k-1.27k 1.28k-3.30k	240-504 512-1016 1024-2640	8 10 2 – 8 10 2 2 8 10 10 –	160 320 800	kHz 1.5-3.15 1.6-3.175 1.28-3.3	150-315 160-317.5 128-330	0.30k-0.63k 0.64k-1.27k 1.28k-3.30k
10kHz (R2)	3.0k-6.3k 6.4k-12.7k 12.8k-33.0k	240-504 512-1016 1024-2640	8 10 2 – 8 10 2 2 8 10 10 –	160 320 800	kHz 1.5-3.15 1.6-3.175 1.28-3.3	150-315 160-317.5 128-330	3.0k-6.3k 6.4k-12.7k 12.8k-33.0k
100kHz (R3)	30k-63k 64k-127k 128k-330k	240-504 512-1016 1024-2640	8 10 2 – 8 10 2 2 8 10 – –	160 320 800	kHz 1.5-3.15 1.6-3.175 1.28-3.3	150-315 160-317.5 128-330	30k-63k 64k-127k 128k-330k
1MHz (R4)	0.30M-1.00M	1200-4000	4 25 10 –	1000	kHz 1.2-4.0	120-400	0.30M-1.00M

TABLE 4.7.3 QUASI-SINEWAVE FREQUENCY DERIVATION IN FREQUENCY SYNTHESIZER

4.7.3.4 Synthesizer Frequency Analysis

Table 4.7.4 is provided to allow a complete analysis of the frequencies to be found in the divider circuitry. In part, it duplicates figures from tables 4.7.2 and 4.7.3.

FREQ. RANGE (NOM)	FREQUENCY DISPLAY Hz	VCO DIVISOR 'n'	f1 VCO OUTPUT (n × 8kHz) kHz	f2 M5 OUTPUT (f1÷8) kHz	f3 M1 OUTPUT (f2÷10) kHz	f4 M2 OUTPUT (f3÷10) Hz	f5* M6 OUTPUT (M6-3) Hz			f6 J6-51 INPUT (f5÷10) Hz
							M6 Input Channels and Division Ratios			
							$X_{ø}$ (f3÷2)	X_1 (f3÷4)	$X_{2\text{-}7}$ (f3÷10)	
100Hz (RØ)	10-63 64-127 128-330	10-63 64-127 128-330	80-504 512-1016 1024-2640	10-63 64-127 128-330	1.0-6.3 6.4-12.7 12.8-33.0	100-630 640-1270 1280-3300			100-630 640-1270 1280-3300	[10-63] [64-127] [128-330]
1kHz (R1)	0.30k-0.63k 0.64k-1.27k 1.28k-3.30k	30-63 64-127 128-330	240-504 512-1016 1024-2640	30-63 64-127 128-330	3.0-6.3 6.4-12.7 12.8-33.0	[100-630] [640-1270] [1280-3300]	1500-3150	1600-3175	1280-3300	150-315 160-317.5 128-330
10kHz (R2)	3.0k-6.3k 6.4k-12.7k 12.8k-33.0k	30-63 64-127 128-330	240-504 512-1016 1024-2640	30-63 64-127 128-330	[3.0-6.3] [6.4-12.7] [12.8-33.0]	100-630 640-1270 1280-3300	1500-3150	1600-3175	1280-3300	150-315 160-317.5 128-330
100kHz (R3)	30k-63k 64k-127k 128k-330k	30-63 64-127 128-330	240-504 512-1016 1024-2640	[30-63] [64-127] [128-330]	3.0-6.3 6.4-12.7 12.8-33.0	100-630 640-1270 1280-3300	1500-3150	1600-3175	1280-3300	150-315 160-317.5 128-330
1MHz (R4)	Hz 0.30M-1.00M	'n' 150-500	kHz 1200-4000	(f1÷4) kHz [300-1000]	(f2÷25) kHz 12-40	(f3÷10) Hz 1200-4000			1200-4000	Hz 120-400

Note:
Frequency spans in square brackets [. .] are the SYNTH O/P frequencies on those ranges.
Other frequencies are present and may be tested.

*Quasi-sine counter M11 on the AC Assembly divides VCO output at all frequencies, but contributes to SYNTH O/P only on the 100Hz Frequency Range.

TABLE 4.7.4 SYNTHESIZER DIVIDERS—FREQUENCY ANALYSIS

4.8 QUADRATURE SINEWAVE OSCILLATOR
(FIG. 4.8.1)

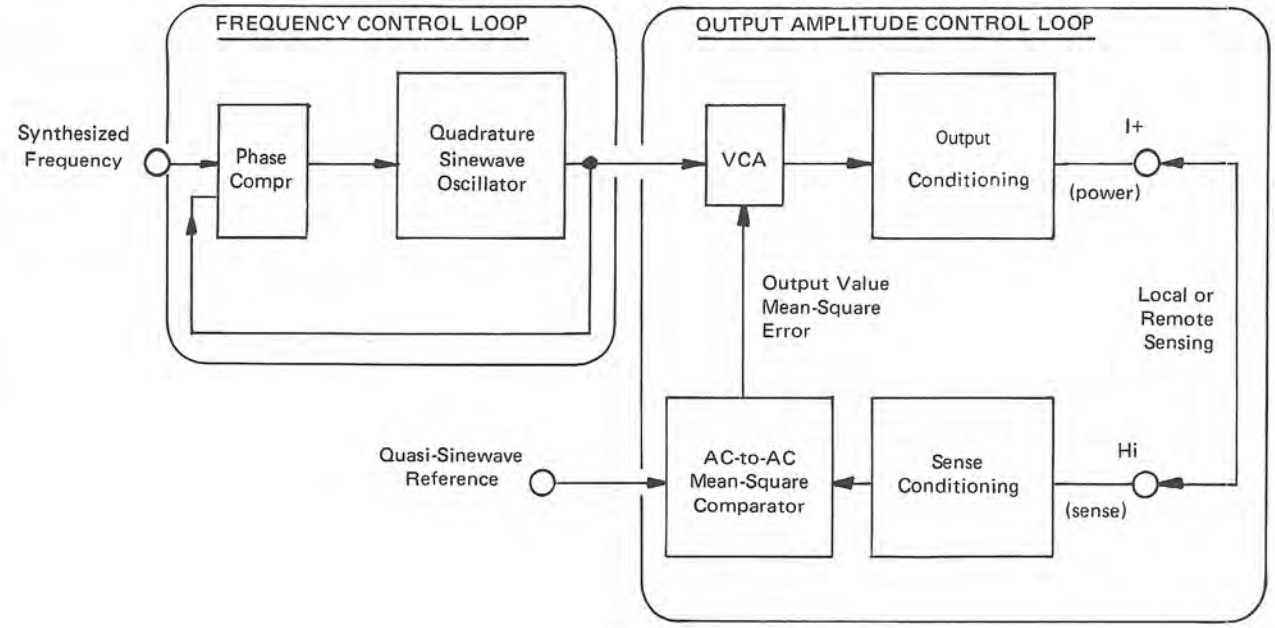


FIG. 4.8.1 THE QUADRATURE SINEWAVE OSCILLATOR AND ITS SYSTEM ENVIRONMENT

4.8.1 Purpose and Environment

The purpose of the oscillator is to define the amplitude-stability, purity and frequency of the sinusoidal output of the instrument on all ranges. Its output is of sufficient constant amplitude to drive the subsequent signal-conditioning circuitry.

After originating in the oscillator, the sinewave amplitude is accurately defined in two output-sense loops, using a low-distortion VCA as control element. The sinewave is set close to its demanded value by analog conditioning in the output circuits.

The output voltage is sensed, attenuated to its 1V Range equivalent, then its mean-square value is compared against that of the quasi-sinewave reference. The difference is converted into a DC error voltage which corrects the output by adjusting the VCA gain.

As the purity and amplitude-stability of the output sinewave depend substantially upon its source, a high quality oscillator is necessary. A 'quadrature' (dual-integrator) circuit is chosen for two main reasons:

a. This arrangement allows extensive phase and amplitude controls to be applied, to establish the required high specification.

b. Its natural frequency can be easily programmed by electrical selection of its component values.

The oscillator is approximately tuned by selection of circuit constants using the two CPU-derived binary words '$FREQR_{2\text{-}\emptyset}$' and '$FREQ_{8\text{-}\emptyset}$'. These also accurately define the crystal-sourced frequency of the Digital Frequency Synthesizer output, to which the oscillator is phase-locked. Thus the output sinewave frequency accuracy is held to 100ppm.

4.8.2 Simple Quadrature Oscillator
(Fig. 4.8.2)

4.8.2.1 Basic Circuit

The circuit consists of two RC integrators and an inverter, connected in a positive feedback loop. The nominal phase-shift around the loop is 360° (actually 720°: 270° in each integrator, 180° in the inverter).

Assuming perfect integrators, matched components and an inverter gain of exactly −1, this circuit will undergo stable oscillation at a frequency given by:

$$\omega_o = \frac{1}{R.C}$$

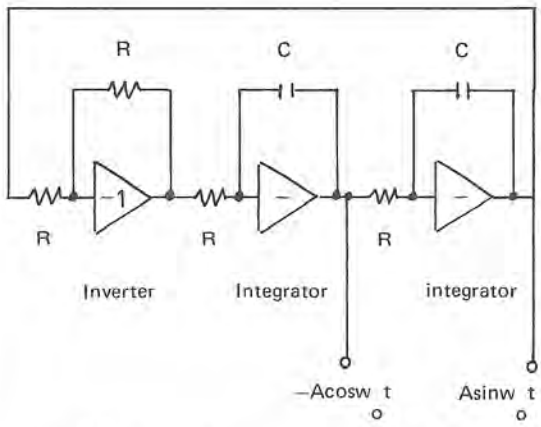


FIG. 4.8.2 BASIC QUADRATURE OSCILLATOR

4.8.2.2 Inadequacies of the Basic Circuit
(Fig. 4.8.2)

For an unrefined practical implementation of the basic circuit, the loop gain and phase response would be as shown in Fig. 4.8.3.

The two main conditions for stable oscillation at constant amplitude are: exactly unity loop gain, and exactly 360° (or multiple of 360°) of loop phase-shift; so the circuit of Fig. 4.8.2 clearly does not satisfy these conditions. Without some attempt to control gain and phase, the loop would be either over- or under-damped, so oscillations would either die away or increase in amplitude until limited by the supply rails.

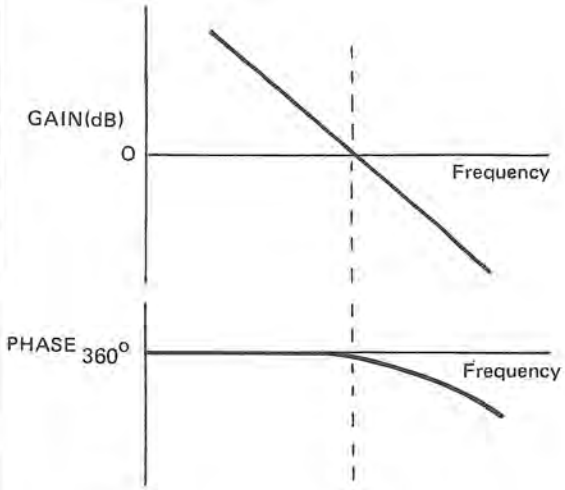


FIG. 4.8.3 GAIN AND PHASE RESPONSE OF PRACTICAL CIRCUIT

4.8.3 Practical Quadrature Oscillator
(Fig. 4.8.4)

The method chosen to refine the simple circuit corrects the loop phase-shift to exactly 360° using a feedback signal. Furthermore, it is arranged that this signal is correct only at a given output amplitude, so the amplitude of stable oscillation is defined. In Fig. 4.8.4 the correction circuit is added.

4.8.3.1 Phase Correction

The loop phase is corrected by introducing a small cosine term (B.cosωt) to be summed with the sine feedback (A.sinωt) at the input to the inverter. The resultant output of the inverter is thus given by:

$$V(t) = -(A.\sin\omega t + B.\cos\omega t) = M.\sin(\omega t + \phi) \qquad \text{——— 1}$$

where $M = \sqrt{A^2 + B^2}$

$\sin\phi = \frac{B}{M}$, and $\cos\phi = \frac{A}{M}$

Hence $\phi = \tan^{-1}\frac{B}{A}$

and for B << A: $\phi \approx \frac{B}{A}$ ——— 2

The ϕ term represents an additional phase shift in the inverter, which by suitable scaling can be made equal to the phase error in the basis oscillator loop. Scaling is achieved by multiplying A.cosωt by the DC amplitude error ($A^2 - I_{REF}$), as described below.

4.8.3.2 Constant Amplitude Control

The above method of phase correction plays its part in controlling the output amplitude. With both sine and cosine terms available, a DC analog of the sinusoidal output amplitude can be obtained utilizing the identity:

$$\sin^2\omega t + \cos^2\omega t = 1.$$

Equal-amplitude sine and cosine outputs are squared in 4-quadrant multipliers. Their squares are summed to generate amplitude feedback in the form:

$$\begin{aligned} & A^2.\sin^2\omega t + A^2.\cos^2\omega t \\ &= A^2(\sin^2\omega t + \cos^2\omega t) \\ &= A^2. \end{aligned}$$

This method therefore expresses the square of the output amplitude as a DC current analog, from which is subtracted a constant DC reference current 'I_{REF}'. The difference current '$A^2 - I_{REF}$' is taken as the amplitude error, which defines the fraction 'B' of the cosine term to be fed back to the inverter as 'B.cosωt'.

In a perfect oscillator, this 'cos' feedback would be driven to zero. But in any practical circuit, some small remnant of B.cosωt persists at the correct loop phase-shift, correcting the loop gain to within the stability specification.

Acting thus together, the combined feedbacks correct both loop gain and phase simultaneously. The method of amplitude correction prevents the appearance of AC components in the amplitude error signal, thus avoiding unacceptable levels of harmonic distortion due to the cosine multiplier.

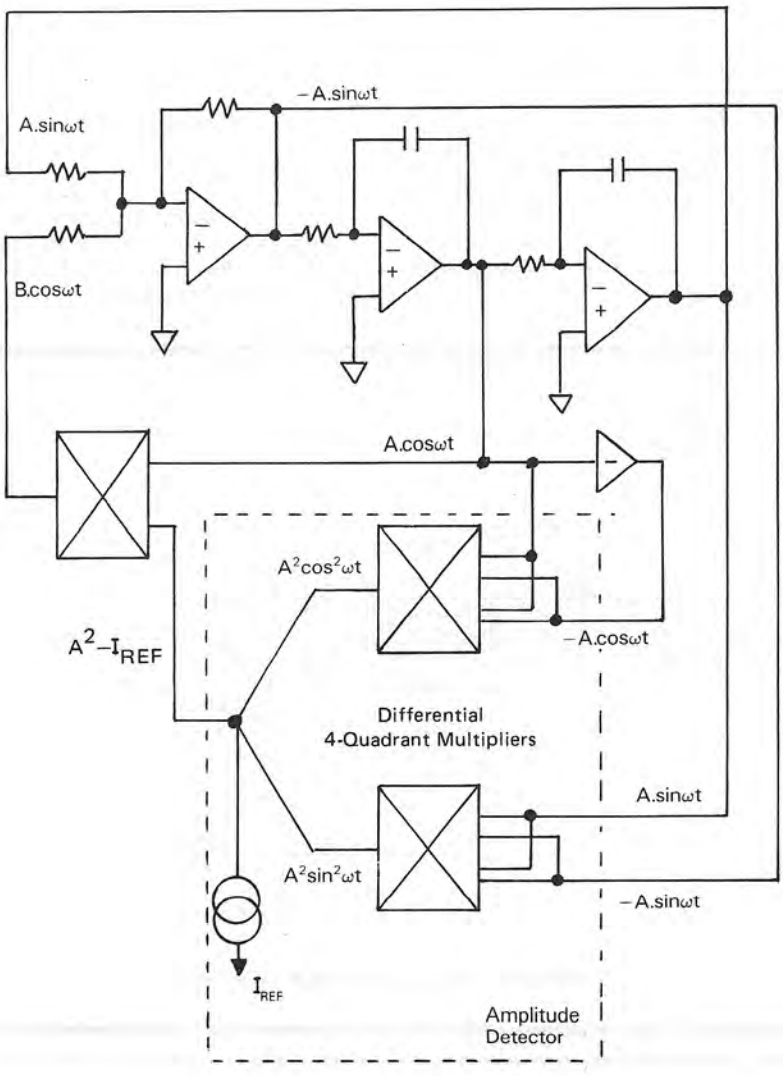


FIG. 4.8.4 CORRECTED QUADRATURE OSCILLATOR

4.8.4 Frequency Control
(Fig. 4.8.5)

Section 4.7 describes frequency generation in the Frequency Synthesizer. Binary control words computed by the CPU represent user-selections of FREQUENCY RANGE and FREQUENCY. These adjust frequency division ratios in the feedback circuit of a phase-locked loop, and division ratios in subsequent frequency dividers, to set the Synthesizer output signal 'SYNTH O/P' to the selected frequency. Stability and accuracy are assured by a crystal-sourced reference of 16kHz.

4.8.4.1 Coarse Adjustment

The Sinewave Oscillator is already approximately tuned to the selected frequency by the two binary control words, which select from weighted values of integration capacitance and resistance:

a. Frequency ranges are selected by the control word $FREQR_{2-\emptyset}$, which controls relays to change the values of integrator capacitance.

b. Frequencies within a range are selected by the control word $FREQ_{8-\emptyset}$, which controls FETs to change the values of integrator resistance.

4.8.4.2 Fine Adjustment

The oscillator's output is converted into a squarewave and applied as 'signal' to the phase comparator of a second phase-locked loop. The Synthesizer output signal 'SYNTH O/P' is input as reference frequency to the same comparator. The difference is integrated to produce a DC phase error signal, which is applied to control the gain of the inverter stage of the oscillator.

It can be seen that the actual operating frequency is a function of the inverter gain:

In the frequency domain, the oscillator loop transfer function is given by:

$$G.\frac{\omega_o}{s} \cdot \frac{\omega_o}{s}$$

where G is the inverter gain,
ω_o is the unity-gain frequency
$s = j.\omega$, where ω is the actual frequency of operation.

For stable oscillation, the loop transfer function must equal 1 angle 0.

Hence $\frac{G.\omega_o^2}{s^2} = 1\underline{/0}$

Therefore $G.\omega_o^2 = j^2.\omega^2 = -1.\omega^2$

and $\underline{\underline{w = -\omega_o.G^{1/2}}}$

Thus by adjusting the gain of the inverter, the phase error signal from the comparator exerts fine control of the oscillator frequency. This phase-locks the oscillator to the Frequency Synthesizer.

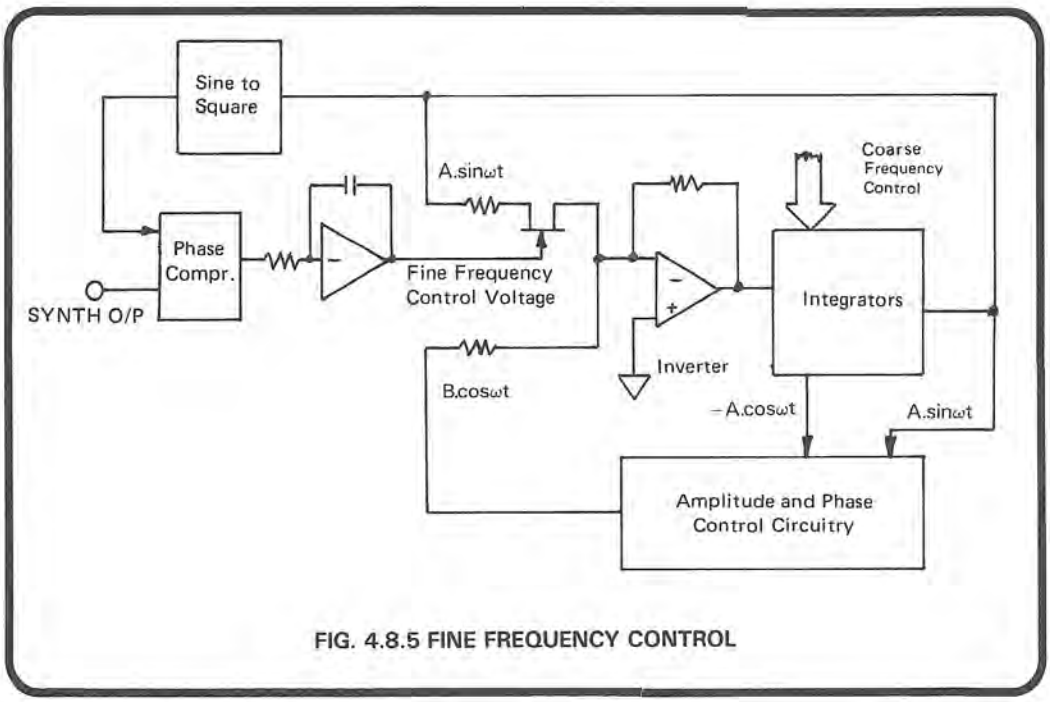


FIG. 4.8.5 FINE FREQUENCY CONTROL

4.8.5 Oscillator Output

The A.sinωt signal is inverted and buffered out to provide the drive to the output loop VCA. The buffer feedback resistors are positive TC thermistors which compensate for the TC of the VCA input FETs (refer to section 4.9).

4.8.6 Main Integrators

(Circuit Diagram 430446 page 7.6-1)

The cascaded integrators consist of M19 and M30 together with their input resistors and feedback capacitors. Both circuits are identical in operation, although some slight differences in implementation exist. Adjustments to the natural oscillation frequency are made by switching the integrator time constants.

4.8.6.1 Frequency Range Switching

The feedback capacitors are selected by the binary control word '$FREQR_{2\text{-}\emptyset}$'. This is decoded into five lines $R_{4\text{-}\emptyset}$ (page 7.6-5), each representing a frequency range. The capacitors for R_4 (1MHz) are fixed, one other set being added in parallel when its range is selected. Relays RL1 to RL8 perform the switching.

4.8.6.2 Frequency Increments

The integrator input resistors are connected in a binarily-weighted ladder network, the total input resistance depending on the pattern of FET conduction. Each FET is turned on by its corresponding binary digit in the frequency control word $FREQ_{8\text{-}\emptyset}$ (appearing as $A_{8\text{-}\emptyset}$ and $B_{8\text{-}\emptyset}$ at the FET gates).

The least-significant bits, representing low frequencies, control the highest-value resistors at the base of the ladder. The most-significant bits, which represent the highest frequencies, control the lowest-value resistors at the top.

Any user-selected frequency in a given frequency range is thus represented by a bit-pattern in the control word, which is repeated in the FET conduction pattern and resistance selection at the input of both integrators.

4.8.6.3 Slew Rate and Protection

Emitter-followers at the outputs of the integrator operational amplifiers allow the high slew-rates necessary to be achieved, by buffering loading effects. The diode clamp networks between output and input prevent latch-up by imposing unity-gain feedback when output peaks exceed approx. 5V.

4.8.6.4 Output Offset Control

The amplitude detector circuit squares the outputs from both integrators. It is therefore important that their DC offset voltages are not included in the squaring computation.

The 'Cosine' offset is removed by adjustment of R50 at the non-inverting input of M30, and the 'Sine' offset by R49 at the input of inverter M15. This latter adjustment removes the combined offsets of M15 and M19. (At manufacture, and after any replacement of major board components, the controls are iteratively adjusted for minimum AC fundamental component in the DC amplitude control signal 'V_G' at link 'B'.)

4.8.7 Inverter Stage

The inverter completes the positive feedback loop of the basic oscillator. The very high bandwidth device used for M15 is compensated by C27, and its TO8 case is grounded. As mentioned earlier, its DC input offset is adjusted by R49 to null the sine DC offset.

4.8.7.1 Gain Control

The inverter has three inputs:

a. $A.\sin\omega t$ from the second integrator, the basic oscillator feedback loop.

b. $B.\cos\omega t$ from the Amplitude correction loop.

c. 'FREQ ERROR', a DC current which alters the inverter's input resistance (and hence its gain) by controlling FET conduction, phase-locking the oscillator to the synthesizer output frequency (refer to para 4.8.4.2).

Inputs a and b ($A.\sin\omega t$ and $B.\cos\omega t$) are summed as currents at the inverting input. The amplitude of the $B.\cos\omega t$ signal is determined by the action of the amplitude control loop, described in sections 4.8.8 and 4.8.9.

Input c controls the gain of the inverter. The $A.\sin\omega t$ is applied via two input resistors R28 and R41 in series. R28 is shunted by the two FETs of Q29, whose the source-drain resistance is altered by the 'FREQ ERROR' current via current-mirrors M16 and M18.

Two FETs in series are required for the amplitude levels reached by $A.\sin\omega t$. R41 is selected to account for differing 'on' resistances of different batches of FETs. This input circuit is a scaled-down version of that employed for the VCA in the main output loop, details of which appear in section 4.9.

A description of the action of the frequency tracking loop follows at para 4.8.7.2.

4.8.7.2 Frequency Tracking – General

As described in para 4.8.4.2, the oscillator's output is applied to the comparator of a phase-locked loop. The Synthesizer output is input as reference frequency to the same comparator. The phase-difference pulse train from the comparator is integrated to produce a DC phase error signal, which is applied to control the gain of the inverter stage of the oscillator. This exerts fine control of the oscillator frequency, tracking the Synthesizer frequency.

4.8.7.3 Tracking Comparator

(Circuit Diagram 430447 Page 7.7-6)

After buffering and invertion by M47 on the Sine-source Assembly (page 7.6-1), the oscillator A.sinωt output is passed to the AC Assembly via J6-45 and J7-45.

On the AC Assembly, the sinewave is converted into a squarewave by Schmitt bistable Q23/Q33, and level-shifted to logic supply levels of 0V and −15V by D25/Q28. Q28 provides a current-limited load for maximum gain, while D24 and D25 prevent voltage saturation of Q32. Q23 buffers the resulting squarewave into the phase comparator input at M30-6.

The slower zero-crossings at the lowest frequencies could be susceptible to HF noise, so this is filtered, on the 100Hz frequency range only, by Q27 and C48.

The 'SYNTH O/P' squarewave, at the demanded frequency, is transmitted from the Sine-source Assembly at low (1V Full Range) level. This holds the maximum slew rate to a value which avoids inducing interference in other internal circuits. Q20 and Q21 amplify the signal to the CMOS logic levels of 0V and −15V required by the comparator input at M30-3.

Note that current steering is used between Q32 and Q33, and between Q20 and Q21. Also, a constant current source Q22 provides Q23 emitter current. These measures prevent the fast switching edges in the schmitt and amplifier circuits from injecting spikes into the supply rails.

Phase-comparator output M30-5 consists of positive pulses (0V) when the oscillator lags the synthesizer, or negative (−15V) when the oscillator leads. When both are in phase, M30-5 is at high impedance.

At integrator M31 input, zener diode D30 holds the non-inverting input at −6.4V; so for in-phase signals into the comparator, the inverting input seeks the same level. The integrator tends to hold its voltage level (with very slight drift due to capacitor leakage but limited to −9.8V by D32/D33). When the oscillator output lags the synthesizer output, the positive-going comparator pulses are integrated to drive M31-6 slowly more negative. When the phase of the oscillator leads, the integrator output becomes more positive.

The phase control loop seeks to phase-lock the two inputs to the comparator. If they are in phase, the comparator output is at high impedance ('TRISTATE'). In this condition the integrator capacitors C53 and C56 have no charge or discharge path, so M31's extremely high gain maintains a constant charge on the capacitors. The constant voltage on Q37 base maintains a constant 'FREQ ERROR' current.

Q37 appears to be an open-collector amplifier. However, its collector current passes via J7-44 and J6-44, into the two current-mirrors at the input to the oscillator inverter on the Sine-source Assembly (page 7.6-1), and thence to the −15V rail.

With constant input current, the mirrors continue to draw the same output current from the AN4 bias network for Q29, so the frequency of the dual-integrator oscillator remains constant. Thus the loop stabilizes only when the oscillator frequency is in phase with (and therefore at the same frequency as) the Frequency Synthesizer output.

The overall action is for a lagging oscillator (frequency lower than the synthesizer) to increase the DC current flowing into the two current mirrors, and vice-versa if the oscillator leads. The two inputs to the comparator are in phase when the sinewave output from the oscillator is at the synthesizer frequency.

Any disturbance in the loop will generate corrections to restore zero phase difference at the inputs of M30. Frequency deviations are therefore detected at an early stage as phase changes, giving a measure of 'phase advance' correction.

4.8.8 Oscillation Amplitude Detector

The method of amplitude measurement relies on the identity '$\sin^2\omega t + \cos^2\omega t = 1$' to convert AC output signals from the oscillator into a representative DC signal.

Squaring Asinωt and Acosωt:

$$A^2\sin^2\omega t = \frac{A^2}{2} - \frac{A^2}{2}\cos 2\omega t$$

$$A^2\cos^2\omega t = \frac{A^2}{2} + \frac{A^2}{2}\cos 2\omega t$$

The AC waveforms of $A^2\cos^2\omega t$ and $A^2\sin^2\omega t$ are inverted versions of each other, at twice the original frequency, and both are symmetrical about the DC mean value of $\frac{A^2}{2}$.

By summing the two, the AC waveforms are eliminated, leaving a DC signal, A^2, representing the square of the amplitude.

In the Amplitude Detector, the Vsin and Vcos outputs from the oscillator are squared electronically and summed as a differential current I^2. This is compared with a constant DC reference current I_{ref} to generate the error current ($I^2 - I_{ref}$), which is passed through resistors to derive an amplitude error voltage 'V_G'. This is filtered and passed to the Amplitude Control circuits (page 7.6-5).

V_G is driven to zero by the action of the amplitude control loop, so that $I^2 - I_{ref} = 0$, and thus $I^2 = I_{ref}$. The loop will therefore stabilize only when the two are equal, at a constant amplitude.

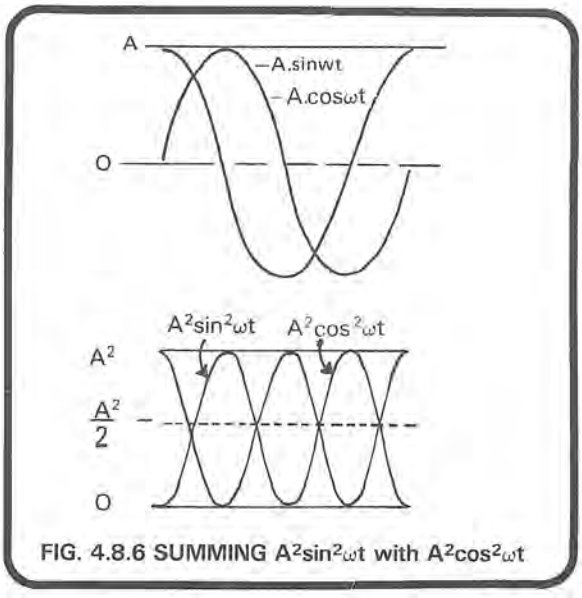


FIG. 4.8.6 SUMMING $A^2\sin^2\omega t$ with $A^2\cos^2\omega t$

4.8.8.1 Squaring Circuit Inputs
(Circuit Diagram 430446 Page 7.6-1)

Vcos and Vsin are squared independently in a pair of differential 4-Quadrant multipliers, each with two identical differential inputs. The Sine Squarer receives $V\sin\omega t$ from the second integrator M30 (Q44 emitter), and $-V\sin\omega t$ from the main inverter (M15-6). As $+V\cos\omega t$ is the only natural cosine output from the oscillator, $-V\cos\omega t$ is derived by inversion in M31. These are both fed as inputs to the Cosine Squarer.

4.8.8.2 Cosine Squarer
(Circuit Diagram 430446 Page 7.6-2)

Isolating the Cosine circuit alone as an example, there are two differential inputs. One is applied across M34 pins 13 and 16, and the other across pins 6 and 10.

The multiplying action of the squaring circuitry relies on the exponential transconductance between a transistor's base voltage and its emitter-collector current:

$$I_c \propto \exp(V_{be})$$
$$\text{and } V_{be} \propto \text{Ln}(I_c)$$

The difference between the currents in M34-1 and M34-14 collectors is linearly proportional to $V\cos\omega t$ (due to M34 emitter resistors AN15). The currents are drawn from the supply through Q55 (which is connected as two matched diodes), but because of the exponential transconductance, Q55 base-emitter voltages increase logarithmically with increase of emitter current. Therefore the differential voltage at Q56 and Q57 bases due to Q55 emitter currents is logarithmic:

$$V_{Q55\text{-}4} - V_{Q55\text{-}3} \propto \text{Ln}(V.\cos\omega t)$$

The difference between the currents in M34-9 and M34-7 collectors is also linearly proportional to $V\cos\omega t$ (due to other M34 emitter resistors AN15). But each collector current is divided between the two halves of the dual transistor in its collector circuit, regulated both by the dual transistor's exponential transconductance, and by its logarithmic differential base voltage.

The combined effect of these two factors is similar to the mathematical operation of multiplying by adding logarithms: a term is produced in each Q56 and Q57 collector current, proportional to the linear product of the two input voltages.

By cross coupling the collectors of Q56 and Q57 as shown, other constant terms are suppressed, and the difference between the currents drawn from AN15-7/8 and AN16-9/10 is proportional to:

$$V\cos\omega t \times V\cos\omega t$$

The inputs are equal, so the differential output current is proportional to $V^2\cos^2\omega t$.

4.8.8.3 Sine Squarer

The Sine Squarer behaves in the same way, producing a differential current in its collector loads proportional to $V^2\sin^2\omega t$.

4.8.8.4 Cos^2, Sin^2 and I_{ref} Summing

In the 4200 squaring circuits, the currents from both Sine and Cosine Squarers are combined in common loads. The voltages developed across the loads will therefore also differ by an amount proportional to $V^2\cos^2\omega t + V^2\sin^2\omega t$. Thus if a reference current was not superimposed, and utilizing the well-known identity '$\sin^2 + \cos^2 = 1$', a DC voltage would exist between TP9 and TP10 (TP9 positive), equal to:

$$KV^2(\cos^2\omega t + \sin^2\omega t) = KV^2$$

where 'K' is a constant at constant temperature, dependent upon identical circuit values in both squarers, and 'V' is the amplitude of both sine and cosine outputs from the oscillator.

However, a reference current is superimposed. The DC current I_{ref} is drawn through the 1kohm load AN15 by M40 (pin 2), reducing the positive value of TP9 voltage with respect to TP10 to ($KV^2 - KV_{ref}$). The reference current is established at a value which includes the scaling factor 'K', by D26 and R91. (The value of R91 for correct oscillator amplitude is determined at manufacture). M34 is connected as a diode to compensate for M40 V_{be} temperature drift.

Voltage $K(V^2 - V_{ref})$ is applied to the input of M35a, the unity-gain Summing Amplifier. M35a is connected to remove any common mode present at its input, so at TP11, $K(V^2 - V_{ref})$ is referred to common 2A. At this point it can be recognized as the Amplitude Error Voltage. Moreover, the amplitude loop adjusts the oscillator outputs to drive the error voltage to zero, so the action of the loop also drives V^2 to equal V_{ref}.

4.8.8.5 Filtering

Because components cannot be matched exactly, some small differences can exist between the $\sin^2$ and $\cos^2$ terms. Such differences appear in V_G as the fundamental and second harmonics of the oscillator frequency. These are limited by the filter formed by M35b and its associated circuit.

It would be possible to set a single low-pass bandwidth for all ranges, but as this would need to filter down to 20Hz for the 100Hz range, it would also impose inconveniently long settling times for the higher frequency ranges. The low-pass bandwidth of the filter is therefore switched between frequency ranges by the $R_{4\text{-}\emptyset}$ signals decoded from $FREQR_{2\text{-}\emptyset}$ in the synthesizer (page 7.6-5).

The frequency range signals select the appropriate feedback components, by conduction of only one FET from Q47-Q52 per range.
(Q48 is not used in the 4200).

The filter output is the oscillator amplitude DC error signal 'V_G', limited to a maximum of approx. $\pm 6V$ by the action of back-to-back clamp diodes D24 and D25. V_G passes via link B (see page 7.6-1), to the 'Amplitude Control' circuitry. The value of V_G determines the fraction, and its polarity the phase, of the $V.\cos\omega t$ signal which is to be added to $V.\sin\omega t$ at M15 input.

4.8.9 Amplitude Control Implementation
(Circuit Diagram 430446 Page 7.6-1)

Before describing the control circuitry, it is useful to review the various controls imposed on the oscillator (see Figs. 4.8.1 and 4.8.4):

a. Frequency control by phase-locked loop to the frequency of the synthesizer output (albeit with a constant phase lag). This is effected by controlling the gain of the inverter stage of the oscillator. (Input resistance of M15 is changed by adjusting the conduction of FETs Q29.)

b. Phase control to establish exactly 360° loop phase-shift by injecting a small amount of $V\cos\omega t$ into the oscillator inverter input (via R29).

c. Amplitude control by adjusting the sense and amplitude of $V.\cos\omega t$ added to $V.\sin\omega t$, so that the loop gain is exactly unity at 360° loop phase-shift, at a constant output amplitude, and at the synthesizer frequency.
(M23 gain is adjusted by varying the attenuation of its input signal, using Q41a and Q41b.)

Amplitude error is corrected by adding a fraction of $V\cos\omega t$ or $-V\cos\omega t$ to the $V\sin\omega t$ feedback being applied to the main inverter M15. A push-pull control circuit is employed in order to adjust both amplitude and sense. $V\cos\omega t$ is input from Q31 emitter to R71, and its inverse is input to R70 from the output of M31, which also provides the $-V\cos\omega t$ input for the cos squarer.

4.8.9.1 $V.\cos\omega t$ Amplifier — M23

M23 is connected as a summing VCA, with a fixed feedback resistor R53. $V\cos\omega t$ and $-V\cos\omega t$ are applied to opposite ends of its balanced input resistor chain R71, R65, R64 and R70. The center of the chain is the virtual ground of M23, so if the 'on' resistances of $Q41_a$ and $Q41_b$ are equal, the balance is not disturbed and M23 output voltage is zero.

When the Loop-gain Error is zero (V_G = OV), the static conditions set approx. −3V bias on both FETs (depletion mode) to reduce crossover distortion. The FET gates are also bootstrapped by M24 and M25 to half the AC voltage between source and drain.

The DC conditions are:

$Q41_a$	Q46 emitter	—	−0.75V
	M26 I_{in}	—	150μA
	M26 I_{out}	—	300μA
	$Q41_a$ V_{gs}	—	−1.5V
$Q41_b$	M32-6	—	OV
	Q45 emitter	—	−0.75V
	M27 I_{in}	—	150μA
	M27 I_{out}	—	300μA
	$Q41_b$ V_{gs}	—	−1.5V
Amplitude Error:			
	M23-6	—	zero

The Amplitude Error adjusts the 'on' resistance of $Q41_a$ and $Q41_b$ differentially, due to the inverter M32 in the side feeding $Q41_b$. In the case of a positive V_G of about 0.5V:

$Q41_a$	Q46 emit.	—	−0.25V
	M26 I_{in}	—	50μA
	M26 I_{out}	—	100μA
	$Q41_a$ V_{gs}	—	−0.5V (more conduction)
$Q41_b$	M32-6	—	−0.5V
	Q45 emit.	—	−1.25V
	M27 I_{in}	—	250μA
	M27 I_{out}	—	500μA
	$Q41_b$ V_{gs}	—	−2.5V (less conduction)

The output voltage at M23-6 is in the same phase as $V\cos\omega t$, increasing with larger amplitude error.

For a negative V_G, M23-6 output voltage assumes the same phase as $-V\cos\omega t$, increasing with larger amplitude error.

Transistors Q45 and Q46 act as voltage-to-current converters to drive the 'X2' current mirrors M27 and M26. Voltage reference diodes D20 and D22 provide the crossover bias. D21 and D23 provide clamping when Q45 and Q46 bases are driven positive, preventing V_{be} breakdown.

M23 output (now recognized as '$B.\cos\omega t$') is summed with the basic oscillator feedback ($V\sin\omega t$) at the main inverter input (M15-5). When the amplitude is correct, and the loop phase is exactly 360°, M23 output is zero and does not inject any 'cos' component into the loop.

If the loop gain or phase is in error, then the squarers' output current is not equal to the reference current, V_G is not zero, and a small amount of cos component is fed into the loop. This adjusts the loop phase and gain to correct the oscillator amplitude.

4.9 OUTPUT AMPLITUDE CONTROL SYSTEM

This complex system generates the whole range of 4200 voltage outputs, as defined by its inputs. For the Current function, an AC voltage is derived from the internal voltage amplitude loop on the 1V or 10V range to act as an accurate reference. Thus the following description applies also to the generation of that reference.

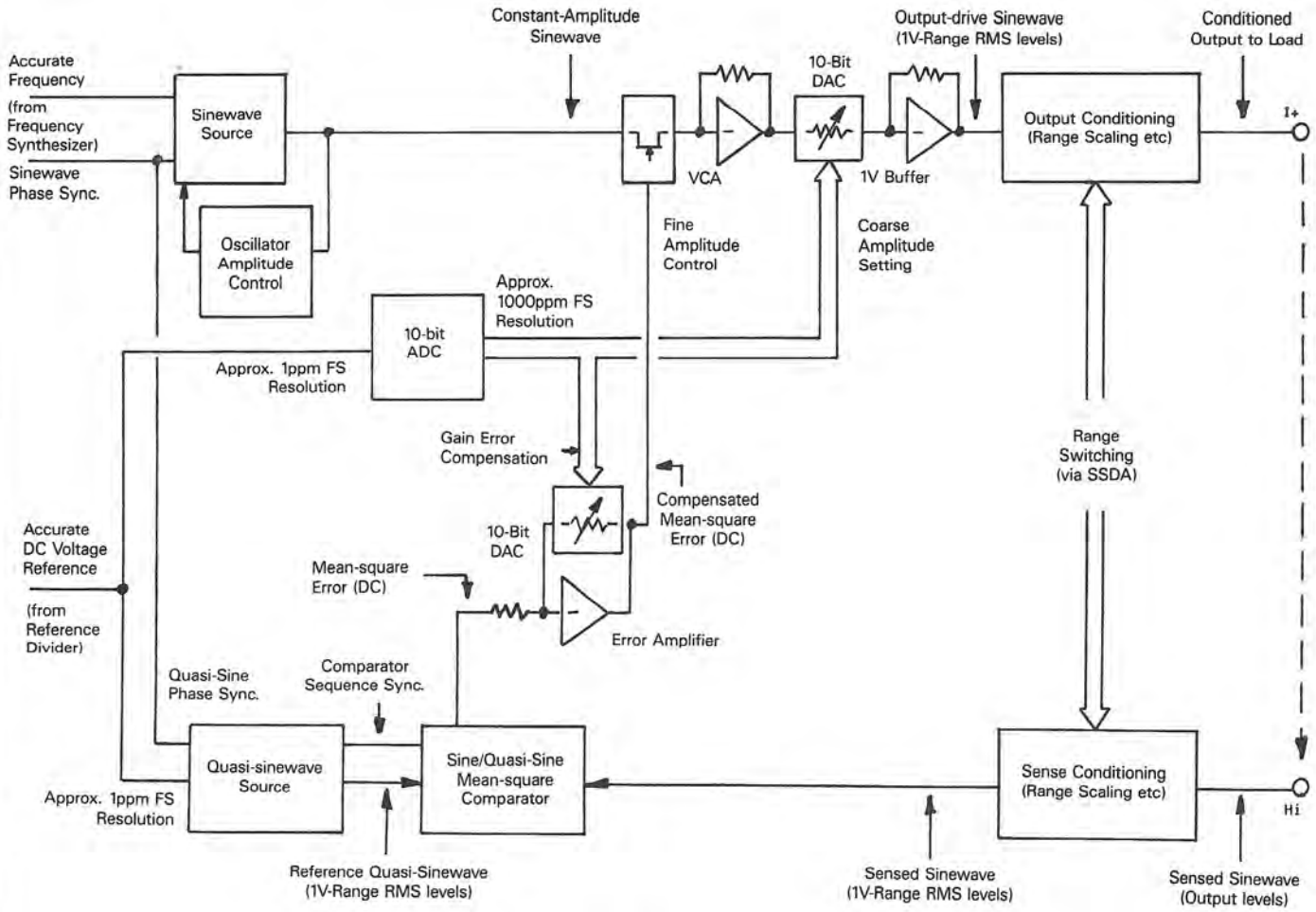


FIG. 4.9.1 OUTPUT AMPLITUDE CONTROL SYSTEM.

Characteristic of 4200 Output	*Controlling Element*	*Controlling Input to Loop*
Frequency:	Frequency Synthesizer (Crystal Sourced)	Constant-amplitude sinewave from Quadrature Oscillator
Sinewave Purity:	Quadrature Oscillator	Constant-amplitude sinewave
Voltage Range:	Processor, via SSDA and Reference Divider Control Latches	Ranging Signals
Coarse Amplitude:	Reference Divider	Accurate DC Reference Voltage (Resolution reduced to approx. 1000ppm of Full Scale by the 10-bit DAC).
Fine Amplitude:	Reference Divider and Quasi-sinewave Generator	Quasi-sinewave RMS value at a resolution of approx. 1ppm of Full Scale.

4.9.1 System Block Diagram (Fig. 4.9.1)

The system elements are described individually in the five sub-sections from 4.10 to 4.14. The system block diagram at Fig. 4.9.1 throws clear of the handbook, so that it can be used for reference when reading these descriptions.

4.9.2 Frequency and Waveshape Control

Sinewave sourcing is the subject of sub-sections 4.7 (Frequency Synthesizer) and 4.8 (Quadrature Oscillator). The result is a high-purity sinewave of constant 1.9V amplitude, input to the VCA.

4.9.3 Output Ranging

The microprocessor passes Voltage and Current range selections into guard via the serial data link as described in sub-section 4.5.

This range information is held in the Analog Control latches in the Reference Divider Assembly, providing signals to the Output and Sense conditioning circuitry. Their effects are described in sub-sections 4.11 to 4.13.

4.9.4 Coarse Amplitude Setting

The 1V Buffer also acts as a coarse amplitude control within each range. The value of its input resistance is adjusted to control its gain, which is incremented in steps of approximately 1000ppm of Full Scale by a 10-bit digital-to-analog converter.

The increments are defined by a 10-bit analog-to-digital converter, which responds to the accurate DC Reference voltages generated by the Reference Divider. The value of the 'DC Ref' voltage is proportional to the values set on the front panel OUTPUT display, as described in sub-section 4.6.

This coarse adjustment of output amplitude allows the fine control element (the VCA) to operate within a small dynamic range, minimizing introduced distortion and thus maintaining the high purity of the output sinewave.

The operation of the coarse amplitude control is described in sub-section 4.10.

4.9.5 Fine Amplitude Control

4.9.5.1 Error Loop

The output amplitude is controlled within the coarse increments by an 'error' loop. The output is sensed at the load for 4-wire connections, or at an internal point in the forward path when 2-wire connection is selected (or imposed).

The sensed output is reduced to 1V Range RMS levels by the Sense Conditioning circuitry (as described in section 4.11 and 4.13), and its mean-square value is compared with that of the Reference Quasi-sinewave. The difference between the two values is expressed as a DC error, and fed to control the gain of the VCA.

Because the coarse amplitude control adjusts the error loop gain, and the error itself results from comparison with an amplitude analog, the gain of the error loop would not be naturally constant. Compensation is therefore applied to the error to reduce the loop gain in synchronism with increasing increments of coarse amplitude. (The Error Amplifier feedback resistance is reduced by a second DAC in step with the coarse amplitude ADC. The result is that the loop gain, and therefore the loop dynamics, are virtually linear.)

Details of VCA operation and error compensation are described in sub-section 4.10.

4.9.5.2 Mean-Square Comparator

When a value is set on the OUTPUT Display, it describes the RMS value of the output. From the displayed value the Reference Divider generates an accurate DC Reference voltage (stepping in increments of approximately 1ppm of Full Scale), which results in a quasi-sinewave whose peak voltage has the same value.

(Thus at 1V Full Range output, the DC Reference voltage and the quasi-sinewave peak voltage are both 1.397V.)

The Crest Factor for any wave is defined as its Peak value divided by its RMS value. For a pure sinewave the figure is $\sqrt{2}$ (say 1.414), whereas the quasi-sinewave crest factor is 1.397. So for the same RMS value of 1V Full Range output, the quasi-sinewave input to the comparator has a peak value of 1.397V, against the feedback peak of 1.414V. The comparison is between mean-square rather than RMS values, but when the mean-square difference is zero, so is the RMS difference.

Generation of DC Reference voltage and Quasi-sinewave are described in sub-section 4.6.

4.9.5.3 Synchronization

The comparator is based on a sequence of squaring, integration, sampling and subtraction. Its operation and accuracy rely heavily on the synchronism of sinewave and quasi-sinewave, each state-change in the sequence occurring at zero-crossings of both waveforms. Thus both waveforms synchronize to clocks from the synthesizer, even when the sinewave is at a multiple of the quasi-sinewave frequency. The comparison sequence cycles once every ten quasi-sinewave periods.

Comparator operation and synchronization details are described in sub-section 4.14.

4.10 VOLTAGE CONTROLLED AMPLIFIERS
(Circuit Diagram 430446, page 7.6-3)

The circuits described in this section perform the following functions:

(1) Modify the output of the Sine Source by coarsely tracking the gain of the output amplitude loop with the requested output voltage, providing stepped coverage of the instrument's dynamic range.

(2) Provide smooth adjustment of gain, within the coarse steps, in response to mean-square error signals from the Sine/Quasi-Sine Comparator.

(3) Impose the settling rate of the true analog DC reference voltage on both the coarse gain adjustment and the mean-square error (AC AMPL ERROR) scaling.

(4) Sense excess currents in the output buffer, providing a $\overline{\text{LIM ST}}$ signal to the CPU via the analog control interface.

All the circuits described in this section are located on the Sine Source Assembly. On the circuit diagram, two voltage-controlled amplifiers are shown:

a. The 1 Volt Buffer, comprising M45, M46 and the discrete output circuit. The buffer's input resistance is controlled by DAC, M43.

b. The main VCA, M48/Q88, whose input resistance is determined by the FET chain Q76 and Q77.

For a general description of the Output Amplitude Control System refer to section 4.9.

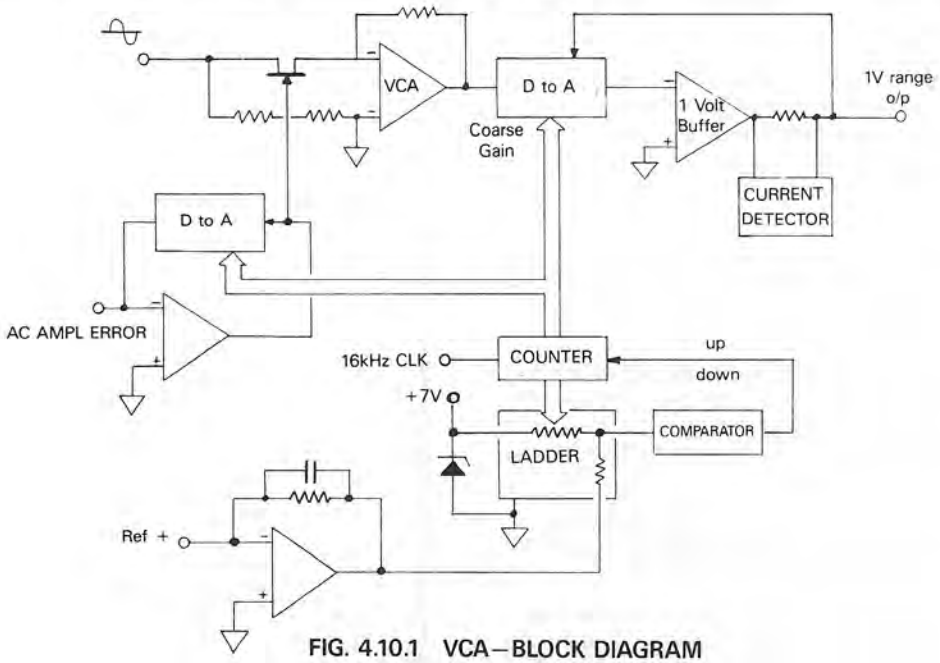


FIG. 4.10.1 VCA—BLOCK DIAGRAM

4.10.1 General (Fig. 4.10.1)

The main VCA receives a constant amplitude sinewave input from the Quadrature Oscillator (Sect. 4.4.8). Its gain is controlled by an error voltage, which is obtained by comparing the sensed sinewave output of the instrument with the reference quasi-sinewave.

The 1 Volt Buffer is included in the output signal path on all voltage and current ranges. It also acts as a VCA, since its input resistance is controlled by its 10-bit Digital-to-Analog Converter. The DAC receives its binary input from an Analog-to-Digital Converter, whose numerical output tracks the user's output demand, in increments of size approximately 1000ppm of full scale.

It is also necessary to ensure that the rate of coarse gain adjustment tracks the settling-time characteristics of the DC Reference filter. To achieve this, the ADC is controlled by the level of the DC Reference voltage. The Reference settling time is thus imposed on the ADC digital output, and hence on the gain adjustments of the 1V Buffer.

For reasons given in section 4.9, it is also necessary to compensate the output loop gain error synchronously with the coarse gain steps. The tracking ADC therefore drives a second DAC, which selects values of feedback resistor in the Error Amplifier. This increments the output-amplitude error loop gain, modifying the AC AMPL ERROR which originated in the mean-square comparator.

The tracking ADC and its DACs ensure that the loop has the fastest possible settling time for any selected frequency.

4.10.1.1 VCA and Buffer

The VCA and 1V Buffer combine in cascade to modify the amplitude of the sinewave output from the sine oscillator, accurately covering the 4200's dynamic range (see Section 4.9). The eventual output from the 1V Buffer (AC 1V FR) forms the instrument's basic 1V range.

The VCA gain is adjusted by the 'AC AMPL ERROR' signal, scaled by M41 and M42. The coarse gain scaling of the 1V buffer derives from the DC Reference voltage 'Ref +'.

4.10.2 Main Voltage-Controlled Amplifier
(Circuit Diagram 430446 Pages 7.6-1 & 7.6-3).

The Sine Oscillator output from divide-by-two buffer M47 (page 7.6-1) is emitter-followed by Q75 to the VCA FET input chain Q76/Q77 (page 7.6-3). These dual FETs are enclosed with M47 PTC feedback resistors R136 and R137, in a metal heatsink. The matched FETS Q76/Q77 ($R_{DS}ON$ within 1%) form the variable gain element for the low input-offset amplifier M48, to provide linear and distortion-free control of gain.

Each FET gate is current-bootstrapped from the divider AN18, to maintain a linear relationship between gain and input voltage. C106 and C117 drive the chain at HF. The centre of the FET chain is also bootstrapped, M44 ensuring precise AC tracking. Resistors R143 and R135 divide and limit the maximum input resistance, preventing the gain from falling to zero.

The thermal linking to M47 feedback resistors compensates for the FET chain temperature coefficient. The inertia of the heatsink's thermal time-constant also prevents gain modulation due to draughts.

The DC signal 'AC AMPL ERROR' is scaled and then fed to each gate by transistors Q78 to Q81, which have low collector capacitance. The voltage control element formed by these transistors adjusts the DC gate voltages of the FETs in the chain, and hence the input resistance of the VCA.

M48 output is emitter-followed and passed through DC-isolating (and AC-compensating) capacitors C121 and C122 into M43, the 1V buffer DAC.

4.10.3 The 1V Buffer

The buffer consists of a voltage follower with hard current limiting. Amplifiers M45 and M46 buffer the Class A power stage from the capacitance of the input DAC. The first buffer M45 has extremely high DC gain, rolling off at HF due to the feedback of C108. It removes the input DC offsets of M46.

M46 controls the buffer's AC performance; C112 ensures that the non-inverting input appears as a virtual AC ground at HF, allowing source-follower Q74 to develop the AC input across R159.

The discrete output stage provides class A current amplification, avoiding any cross-over distortion particularly at HF. Power transistor Q93 is provided with load and quiescent currents, from constant-current source Q94 (70mA) and constant-current sink Q86 (140mA). Refer to Fig. 4.10-2.

With zero input conditions Q94 is saturated, limiting the quiescent current at 70mA. Only the small bias current for Q92 flows in R144, so the output voltage is just +Vb.

The input signal to Q92 controls Q93, allowing a small signal transistor with good HF performance to adjust the large output currents flowing in R144.

Voltage amplifier Q92 cuts off during positive half-cycles of input, reducing Q93 conduction. The quiescent current still flows in R114, but is now shunted through the output circuit via R112 and L7.

During negative half-cycles of input; Q92 conducts, so Q93 conduction increases, drawing its extra (load) current through R144, and its quiescent current from Q94. The emitter of Q92 also attempts to go negative, drawing current directly from the load. The combined currents flow into the current sink, so Q86 must be able to sink 70mA quiescent + 70mA load.

In the output line, inductor L7 and resistor R112 provide phase compensation for capacitive loading at HF.

If any components in the discrete output amplifier are changed, re-adjustment of gain (using M48 feedback resistor R149) may be necessary.

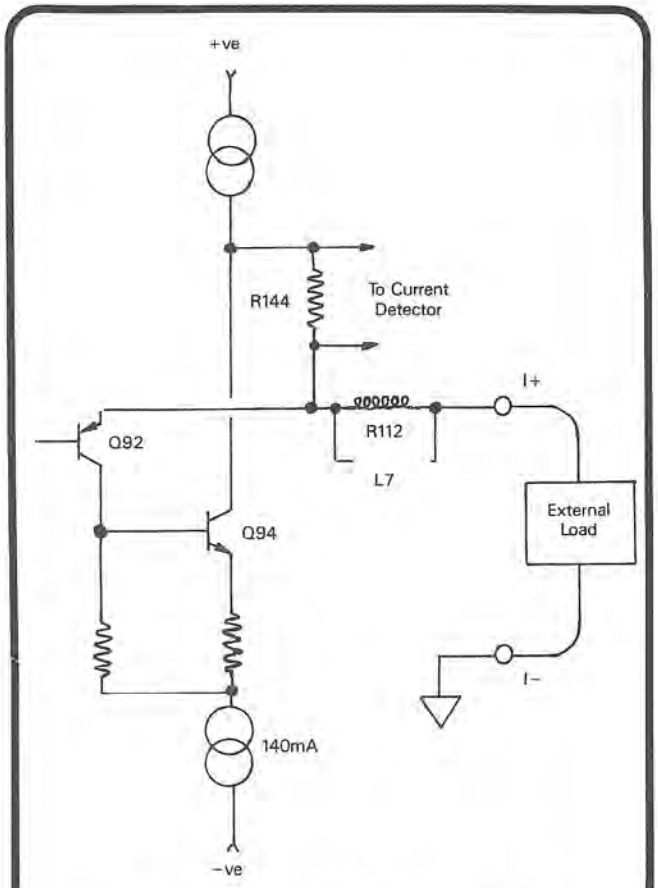


FIG. 4.10.2 1V BUFFER-OUTPUT STAGE

4.10.4 Current Detector

Except for a small bias current, all output current from the discrete buffer stage flows in R144, so the current level can be detected by sensing the differential voltage across it. This sense voltage rides on the output voltage; thus to capture it, the current detector is bootstrapped to the AC 1V output.

High-speed dual comparator M49 forms the basis of the Current Detector circuit. Its supplies are bootstrapped via TP29 to the junction of R144 and R112 in the 1V Buffer output. Q82 and Q84 provide constant current drive to 6.2V Zeners D40 and D41, with Q83 and Q85 providing the regulation for the bootstrapped rails at TP35 and TP36.

The comparator latching levels are set by dividers R151/R152 and R153/R154, their values allowing for bias current error in R144. The comparator's output is open-collector when the peak voltage across R144 is less than the positive or negative latch level. Line drivers Q90 and Q91 are cut off, so the $\overline{\text{LIM ST}}$ line at J6-70 is pulled to +15V by AN2 in the Reference Divider (page 7.4-4).

When the level is exceeded in either polarity, then either M49a or M49b output goes negative. This turns Q90 and Q91 on, pulling the $\overline{\text{LIM ST}}$ line to −15V (in-guard logic-Ø). The signal is passed to the CPU via the serial data link.

This limit is set much lower than the hard current limit of the buffer. If exceeded, the instrument displays 'Error OL', described in Section 2 (Fault Diagnosis). In overload, a built-in margin of safety allows the instrument to meet most of its specifications at 35-40mA.

4.10.5 ADC-DAC Tracking

As mentioned earlier, it is necessary to track the coarse gain stepping rate to the settling-time imposed by the DC Reference filtering. A tracking Analog-to-Digital Converter (ADC) is used to synchronize stepping, ensuring the fastest possible settling time at the selected frequency.

To set circuit conditions for the required output within a range, the gain of the main VCA is set in response to fine amplitude information, in the form of an error signal from the Sine/Quasi-Sine comparator. For constant output amplitude loop gain, the error loop gain also needs to track the coarse amplitude stepping.

For an overall outline of the Output Amplitude Control System, refer to Section 4.9.

4.10.5.1 Use of 'REF+'

(Circuit Diagram 430446 page 7.6-3)

The ADC requires a voltage input which tracks the value of 4200 AC output demanded by the user, with settling times imposed by the Reference filter. The DC 'REF+' voltage exhibits these characteristics, so is used in this circuit to determine the numerical value of the ADC binary output.

'REF+' originates in the Reference Divider and is used to set the peak value of the quasi-sinewave in the AC assembly. Its value ranges from +0.126V at 9% of Full Range, through +1.397V at Full Range, to +2.794V at Full Scale.

REF+ is input to the Sine-Source assembly between J6-57 and J6-56, then applied to amplifier M41b, which is connected to remove any common mode present at its input. Thus at TP47, M41b output is referred to Common-2A.

Capacitors C99, C130 and C131 filter any HF pickup from the reference voltage, and M41b scales up the DC voltage levels by a factor of 2.43, to:

9% of Full Range	: −0.306V,
Full Range	: −3.395V,
Full Scale	: −6.789V.

A positive version of this Full Scale value is also generated (Q66/D30/D31) as a reference for the tracking ADC M38.

4.10.5.2 Tracking ADC M38

(Fig. 4.10.3)

M38 is a 'System DAC' which can be employed either in 'READ' or 'WRITE' mode. WRITE mode is not used in the 4200.

In READ mode the binary count can be output continuously from the ten pins $DB_{9\text{-}0}$. An internal 10-bit counter is clocked at 16kHz into pin 9 via level shifters Q53 and Q54. The counter can be controlled by two level-sensitive inputs: CONT1 and CONT2 (logic-1=+5V; logic-Ø=0V) as follows:

CONT1	CONT2	Effect on Count
Ø	Ø	not used
Ø	1	Incremented
1	Ø	Decremented
1	1	Frozen

An internal 12kOhm reference resistor and switched resistor ladder form a potentiometer between pin 27 (Vref) and pin 1 (Rfb). The junction between them is brought out to pin 2 (OUT1).

The ladder is switched by the 10-bit counter. At zero count it is open-circuit; as the count is increased the ladder resistance reduces in inverse proportion, until at full count of 2^{11}-1 (which corresponds to the 4200 Full Scale output), it reaches its minimum of 12kOhms. See Fig. 4.10.4.

At Full Scale (FS) the M41b output voltage is −6.789V, into Rfb, and the fixed reference into Vref is the positive version of this input, so at FS the OUT1 voltage is balanced at zero.

For 4200 output values below FS, the negative M41b output voltage is linearly reduced, so that the OUT1 voltage tends to increase positively. By feeding an external comparator which drives the CONT1 and CONT2 counter controls, the OUT1 voltage is used to provide automatic control of the count itself. In the case of a reduced output demand, a lower count is required to increase the resistance of the ladder, resetting OUT1 to the zero balance.

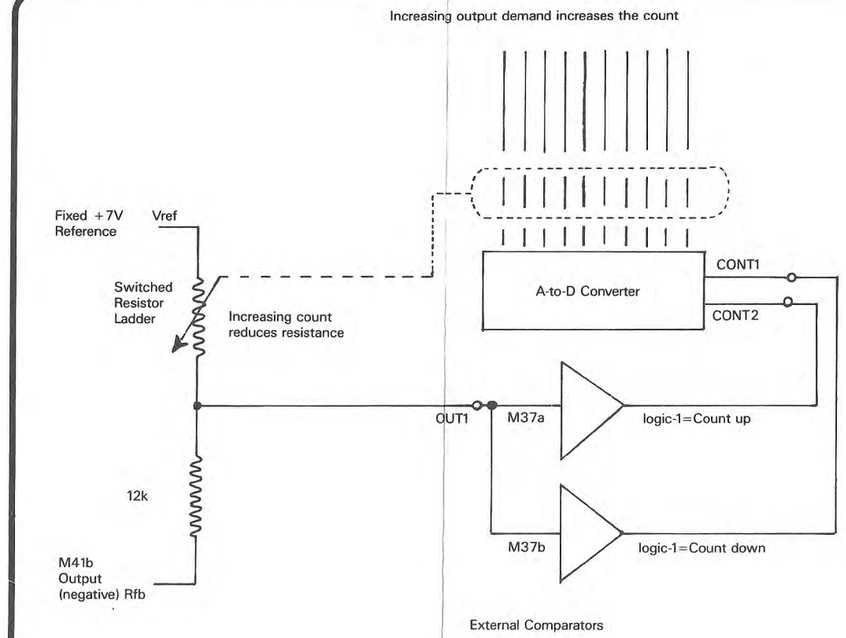


FIG. 4.10.3 SIMPLIFIED DIAGRAM OF TRACKING ANALOG-TO-DIGITAL CONVERTER

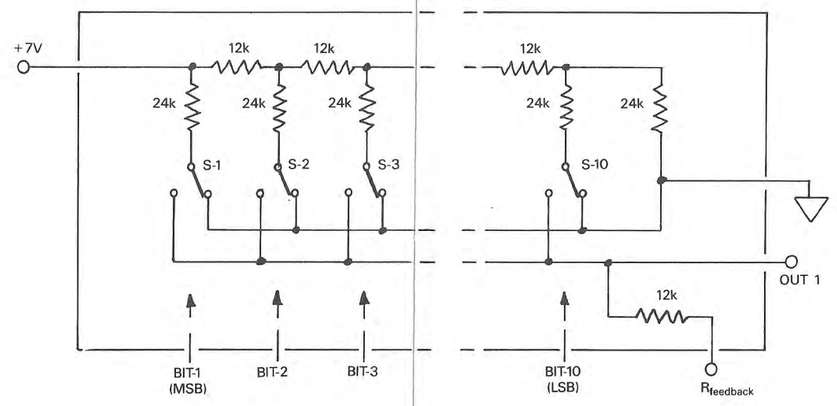


FIG. 4.10.4 A-D TRACKING — R — 2R NETWORK

4.10.5.3 Window Comparator

M37 is a high-speed dual comparator, which accepts OUT1 as its input voltage, and controls the M38 counter via CONT1 and CONT2. The 'Counter Freeze' condition of M38, resulting from both CONT inputs being at logic-1, allows hysteresis bias to be applied the comparator to create the 'Dead Band' window.

Each of the two outputs of M37 responds to its input in the same way: high impedance when its non-inverting input is more positive than its inverting input, and pulled low when the inverting input is more positive (uncommitted-collector).

M37a is connected as a non-inverting device, but M37b inverts its input. OUT1 is input to both circuits. Both inputs are biassed by approximately 15mV to generate the dead-band hysteresis: M37a by R96/R98, R37b by R100/R101.

4.10.5.4 Action for OUT1=Zero

Because of the bias, both M37 outputs are pulled low when the OUT1 voltage is zero. The inverting level-shifters Q67 and Q68 are both cut off by −15V on their gates, so CONT1 and CONT2 are at logic-1. M38 is thus put in the 'Freeze' condition, so its 10-bit output value is held.

In this condition, M36-12 and M36-13 inputs are both at −15V, so M36-10 is also −15V. R99 is therefore placed in parallel with R100, increasing the bias on M37b. The bias on M37a is also increased by Q69 being cut off, placing AN11 and R97 in parallel with R96. The 'Freeze' window is therefore widened, to improve the comparator's noise rejection. Refer to Fig. 4.10.5.

4.10.5.5 Action when OUT1 Voltage Changes

When a user demands a new (greater) output from the 4200, REF+ increases as the Reference filter settles, and the OUT1 voltage becomes more negative. The bias on M37b is eroded and finally exceeded, so M37-7 is placed at high impedance, pulled up to Common-2C by AN13. Q67 conducts, setting CONT1 to logic-Ø and the count increments to step up the gain in the 1V Buffer.

Simultaneously, M36-12 is set to 0V (in guard logic-1). M36-10 rises from −15V to 0V, switching R99 to shunt R101 instead of shunting R100. Q69 conducts, switching R97 to shunt R98 instead of shunting R96. The bias levels shift back to ± 15mV, narrowing the hysteresis window.

If the user had demanded a lower output, OUT1 would have become more positive, exceeding M37a bias. CONT2 would have fallen to logic-Ø, decrementing the counting and reducing the 1V Buffer gain. The effect on the comparator bias would be the same as for the incrementing case.

As the counter changes its numerical value, M38's internal resistance ladder is switched to back-off the OUT1 voltage. When REF+ finally settles, the OUT1 voltage once again enters (and widens) the comparator's dead band, the count freezes, and the 1V Buffer gain remains constant.

Thus the OUT1 voltage remains close to zero as the comparator and tracking ADC respond to the variations of REF+.

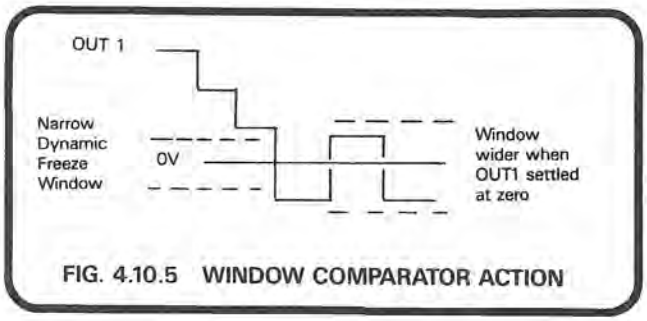
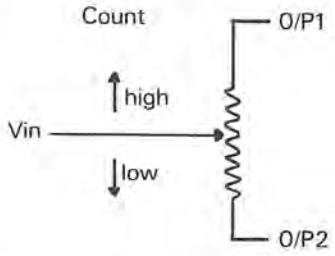


FIG. 4.10.5 WINDOW COMPARATOR ACTION

4.10.5.6 10-bit Digital-to-Analog Converters

M42 and M43 binary inputs are identically connnected, so they both behave in the same way:



For low counts the resistance between Vin and O/P1 is large, and small between Vin and O/P2. The condition is incrementally reversed as the count increases to high values.

As we have seen; an increase in user output demand increases the DC Reference voltage REF+, so a higher ADC count results. This reduces the resistance between M43 pins 15 (Vin) and 1 (O/P1), increasing the gain of the 1V Buffer and thus increasing the 4200 output. This is the coarse gain adjustment referred to in section 9.

M42 has a different function. The fine adjustment of output value is incorporated in the 'Gain Error Loop', in which the output sinewave and quasi-sinewave are compared. The AC AMPL ERROR is generated by this comparison, to be used in controlling the VCA gain.

The error loop thus also passes through the 1V Buffer, and the effect of an increase in ADC count would be to increase the error loop gain, possibly overloading the VCA input FETs. This is prevented by reducing the gain of the error amplifier M41a, using M42 to track the steps of the coarse gain adjustment.

With an increase of the ADC count, M41a feedback is increased, as the resistance between M42 pins 15 and 1 is reduced. This reduces the error loop gain to compensate for the increase due to M43. Thus the fine gain remains virtually constant over the full span of coarse gain adjustment.

4.11 LOW VOLTAGE LOOP

The circuits described in this section perform the following functions:

(1) Connect the VCA output to the terminals to provide the basic 1V range:
0.09V to 2V

(2) Amplify the VCA output voltages to the instrument's terminals, for the 10V range:
0.9V to 20V

(3) Attenuate basic 1V range voltages to provide the millivolt ranges:
9mV to 200mV on 100mV Range
0.9mV to 20mV on 10mV Range
90μV to 2mV on 1mV Range

(4) Sense the voltages at the output terminals (or at the load in Remote Sense) and scale the signal to the 1V RMS Full-Range level for comparison with the quasi-sinewave.

(5) Provide switching of AC voltage output, Range, Guard and Sense, under the control of signals from the Analog Control Interface.

(6) Detect excess currents in the output circuit, providing a status signal to the CPU via the Analog Control Interface.

(7) Detect excess voltages on the PHi (I+) output line, providing a status signal to the CPU via the Analog Control Interface.

The circuits in this section are located as follows:

Millivolt attenuator and sense circuitry:
— AC Assembly

Power amplification:
— Power Amplifier Assembly.

Output control:
— Output Control Assembly.

Terminals:
— Mother Assembly.
— Terminal Board.

A simplified block diagram of the low voltage loop and routing appears in Fig. 4.11.1.

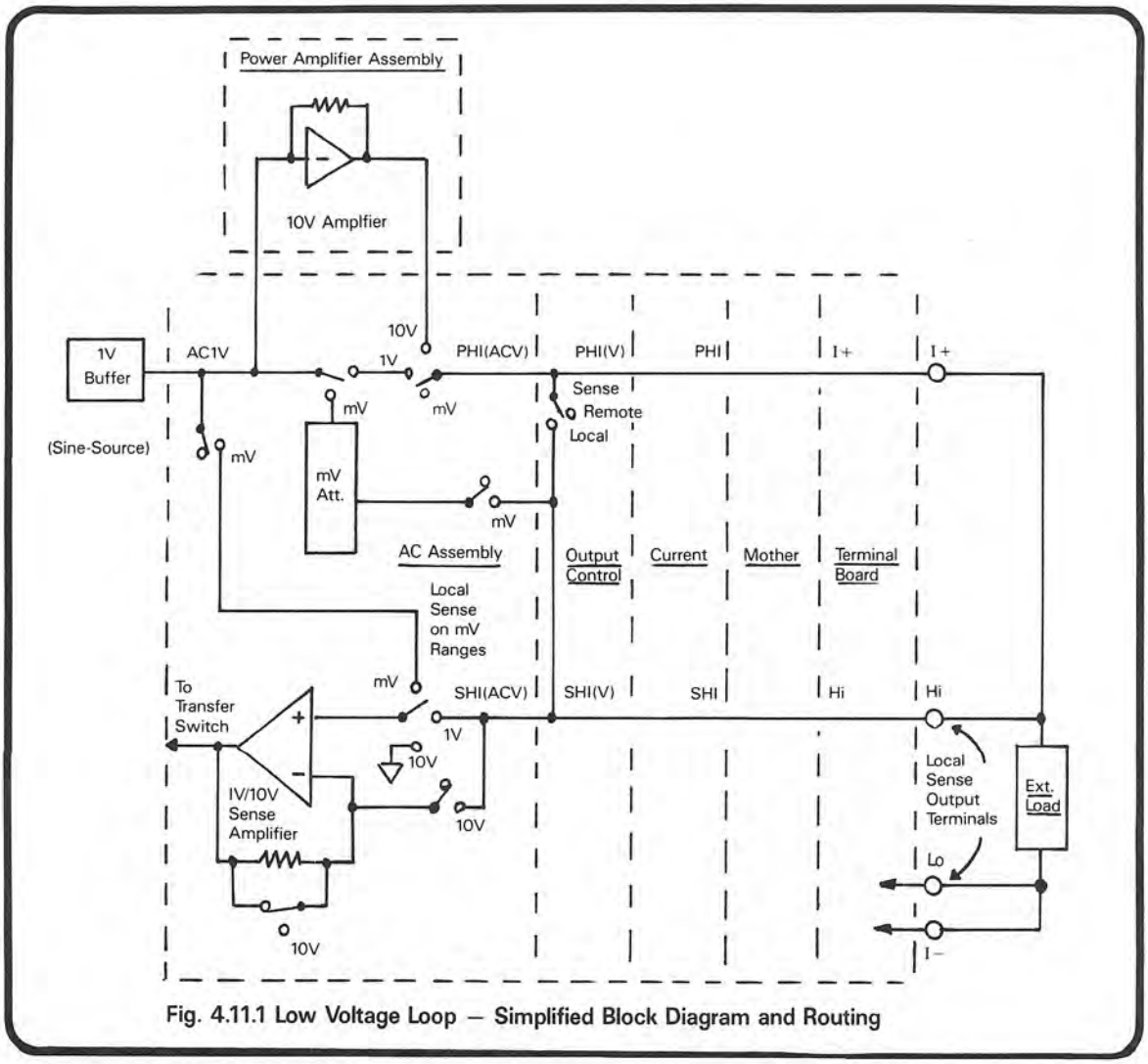


Fig. 4.11.1 Low Voltage Loop — Simplified Block Diagram and Routing

4.11.1 General

This description follows the 1V range path from the VCA buffer to the Sine/Quasi-Sine Comparator (at the input of the transfer switch M16). The 10V and millivolt output and sense conditioning are included.

On the circuit diagrams, the relay contacts are shown in the un-energized condition.

For High Voltage output and sense conditioning see Sections 4.12 and 4.13.

4.11.2 1V Loop — Power Delivery

4.11.2.1 Sine-Source Assembly
(Circuit diagram 430446 Page 7.6-3)

The 1V Buffer (page 7.6-3) is described in Sect 4.10, as part of the output amplitude control circuitry. Its output voltage, signal 'AC 1V' ranging between 0.9V to 2V RMS; is fed out of the Sine-Source assembly on J6-41, via the Mother assembly, and input to the AC assembly on J7-41 (page 7.7-1).

4.11.2.2 AC Assembly
(Circuit diagram 430447 Page 7,7-1)

With the 1V Range selected, relays RL7 (1V) and RL19 ($\overline{1kV}$) are closed, and relays RL4, 5, 6, 17, 18 and 20 are open. So the AC 1V signal is passed directly out of the AC assembly, via RL7, fuse F1, RL19 and fuse F2 as the Power-Hi signal 'PHI(ACV)' at J7-27.

The power common 'PLO(ACV)' is derived from the in-guard Common-2 supply at the star-point Common-2B, and passed out via the three energized contacts of AC Voltage selector relay RL10 to J7-31.

PHI(ACV) and PLO(ACV) travel via the Mother assembly to the Output Control assembly at J5-25 and J5-29 respectively (Page 7.5-1).

4.11.2.3 Output Control Assembly
(Circuit diagram 430550 Page 7.5-1)

In normal 4-wire operation (Remote Sense selected) with OUTPUT 'ON' on the 1V Range, relays RL3, 4, 5 and 6 are energized. The PHI(ACV) signal bypasses the 1kV Range output current sensing resistors via RL1-6 contact, passing through fuse F3 and RL6 contacts to J5-19 as PHI(V).

PLO(ACV) travels via F2, F1, RL3 and RL5 contacts to J5-23 as PLO(V).

The front panel 'Guard' terminals are permanently connected to the internal guard shields via J5-15/16 and J5-11/12. With 'Remote Guard' selected, C19 isolates the guard system from PLO(V) (I− terminal connection), bypassing any HF spikes. With Remote Guard off, RL7 connects the guards to PLO(V) via PTC thermistor R40, which assists in reducing noise on the millivolt ranges.

With Remote Sense not selected, relays RL3 and 4 are un-energized. RL4 contacts short PHI(ACV) to the sense Hi input SHI(ACV). RL3-2/8 contacts short PLO(ACV) to the sense Lo input SLO(ACV); the RL3-5/11 contacts disconnecting the front panel I− terminal from PLO(ACV).

As with all voltage and current ranges, connection to the front panel terminals is through the Current assembly. PHI(V) and PLO(V) travel via the Mother assembly to the Current assembly at J8-25 and J8-29 respectively.

4.11.2.4 Current Assembly
(Circuit Diagram 430555 page 7.8-1)

With any Voltage Range selected, relays RL8 and 9 are un-energized as shown. RL23 is energized; connecting PHI(V) to J8-8/9 as 'PHI' and PLO(V) to J8-16/17 as 'PLO'.

PHI and PLO then pass into the Mother assembly.

If the Current option is not fitted, a Link PCB (part No. 410182) is fitted in its place. This shorts:
J8-25 — PHI(ACV) to J8-8/9 — PHI.
J8-29 — PLO(ACV) to J8-16/17 — PLO.
The connections do not involve relay switching.

4.11.2.5 Mother Assembly
(Circuit Diagram 430532 page 7.16-1)

PHI and PLO enter at J8-8/9 and J8-16/17 respectively.

PLO passes through the common mode choke L1 via J23-3 and J26-4 as 'I−' to the Terminal Board assembly.

PHI is switched by relay RL1. If Remote Sense is not selected, RL1 is un-energized as shown; disconnecting PHI from the I+ terminal circuit, and shorting it to the sense SHI input line. When in Remote Sense RL1 is energized, and PHI passes through the common mode choke L1 via J23-1 and J26-1 as 'I+' to the Terminal Board assembly.

4.11.2.6 Terminal Board Assembly
(Circuit Diagram 430634 page 7.17-3)

I+ and I− are filtered and passed to the front panel terminals. Ferrite bead FB1 and C2 protect the internal circuitry from the effects of HF pickup in the external circuit.

4.11.2.7 Option 42 — Rear Terminal Output
(Circuit Diagram 430530 page 7.17-1
Layout Drawing 480603 page 7.19-2)

Option 42 is incorporated at manufacture. With rear output terminals, the Terminal Board assembly is not fitted. The connections to the rear are taken fro J26 on the Mother assembly. A capacitor C1 connects Guard to Earth (Ground), and ferrite beads are fitted on the Hi, I+ and Guard leads at the terminals. The mV range filter relay is not fitted.

4.11.3.1 Terminal Board Assembly
(Circuit Diagram 430634 page 7.17-3)

For the users with Option 42 — Rear Output, the circuitry at the terminals is changed. Refer to sect. 4.11.2.7.

If Remote Sense is selected, the front panel sense terminals Hi and Lo are connected externally to I+ and I− respectively, at the load.

The sensed voltage is filtered by FB2 and C3 to remove external HF pickup. This rejection is augmented by C1 for the millivolt ranges and for 'AC Zero' output selection. A signal ('R−', 'R+'), originating as 'TERM FILTER' in the Reference Divider, operates relay RL1 on the millivolt ranges. (Circuit Diagram 430535 page 7.4-4).

The filtered sense voltage is fed into the Mother assembly between J26-2 (HI) and J26-5 (LO). (No external sensing is provided for the millivolt ranges. See para 4.11.5 and Fig. 4.11.1 for the local sensing arrangement.)

4.11.3.2 Mother Assembly
(Circuit Diagram 430532 page 7.16-1)

LO passes through the common mode choke and directly to the Current assembly at J8-18 as SLO.

HI also passes through the choke and enters the Current assembly as SHI at J8-10. However, if Remote Sense is not selected, it is shorted to PHI by relay RL1. RL1 is energized from the REM SENSE + and − lines from the Output Control assembly.

4.11.3.3 Current Assembly
(Circuit Diagram 430555 page 7.8-1)

With any Voltage Range selected, relays RL8 and 9 are un-energized as shown. RL23 is energized; connecting SHI into the Mother assembly as 'SHI(V)' via J8-26, and SLO via J8-30 as 'SLO(V)'.

If the Current option is not fitted, the Link PCB shorts:

J8-10 — SHI to J8-26 — SHI(V),
J8-18 — SLO to J8-30 — SLO(V).

The connections do not involve relay switching.

4.11.3.4 Output Control Assembly
(Circuit Diagram 430550 page 7.5-1)

In normal 4-wire operation (Remote Sense selected) with OUTPUT 'ON' on the 1V Range, relays RL3, 4, 5 and 6 are energized. SHI(V) enters from the Mother assembly at J5-20 and is passed directly through RL6 contacts (OUTPUT ON) and out via J5-26 as SHI(ACV).

SLO(V) travels via RL5 contacts (OUTPUT ON) to J5-30 as SLO(ACV).

With Remote Sense not selected, relays RL3 and 4 are un-energized. RL4 contacts short SHI (ACV) to the power Hi output PHI(ACV). RL3-2/8 contacts short SLO(ACV) to the power Lo output PLO(ACV).

SHI(ACV) and SLO(ACV) travel via the Mother assembly to the AC assembly at J7-28 and J7-32 respectively (Page 7.7-1).

4.11.3.5 AC Assembly
(Circuit Diagram 430447 page 7.7-1)

SLO(ACV) passes via the energized contact of the AC Voltage selector relay RL10, to be referred to the Sense Amplifier common 'SIG LO'.

With the IV Range selected, relay RL19 ($\overline{1kV}$) contacts are closed, so SHI(ACV) appears at RL19-11 as 'SENSE HI' (Refer to the circuit diagram on page 7.7-2).

With the 1V Range selected, relay RL8 (1V) is energized, thus SENSE HI is applied to the non-inverting input of the Sense Amplifier via R126. RL14 is un-energized as shown, so the inverting input via R115 is referred to SIG LO.

RL3 ($\overline{100V + 1kV}$) is energized, connecting the Sense Amplifier output to the Sine/Quasi-Sine comparator transfer switch M16-11 (page 7.7-3).

A description of the Sense Amplifier appears in Section 4.11.4.

4.11.4 1V Sense Amplifier

(Circuit Diagram 430447 page 7.7-2)

The same amplifier is used on the 10V, 1V, 100mV, 10mV and 1mV Ranges. Its main purpose is to buffer the sense voltage, providing a high impedance input, low DC offset and flat frequency response.

On the 1V and millvolt ranges it is connected as a voltage-follower, sensing always being carried out at the 1V level. The 1V range sense signal originates at the load in Remote Sense, or in the Output Control assembly in local sense. For the millivolt ranges the 'AC1V' drive to the millivolt attenuators is sensed directly (see sect. 4.11.5).

On the 10V range an inverting configuration is employed. The circuit divides by 10, scaling the sense signal down to 1V range levels, for input to the Sine/Quasi-Sine comparator.

Separate arrangements are made for attenuation and scaling on the 100V and 1kV ranges. These are described in Section 4.13.

4.11.4.1 General

A discrete amplifier is used to provide the required slew rate up to 1MHz, all time constants being set well above 1MHz, with the first pole above 5MHz. It is configured into its follower circuit by relay switching.

Relays RL8, RL12 and RL3 are all energized on the 1V range. Relays RL11, RL13, RL14, RL15 and RL16 remain un-energized as shown in the diagram.

Dual JFET Q41 is a unity gain buffer in totem pole configuration. It drives the input protection diodes D37-D40, D44-D47, and the screen of Q40 inverting input; also driving the bootstrap buffer Q46. The total input capacitance is thus reduced to 1 – 1.5pF.

The differential input amplifier, Dual FET Q40, has low input capacitance, and low input current. Q36 provides constant-current drive to Q40 and the bootstrapped followers Q38/Q39. R107 permits initial DC input-offset cancellation. The stage gain is low.

Emitter-followers Q34 and Q35 buffer the high-impedance low-gain FET stage, driving a differential signal into the high gain voltage amplifier Q29/Q30. This arrangement has the advantage of placing all the gain in one stage. The single-ended drive to Q31 output stage is taken from Q30 collector.

Q24 and Q25 form a current mirror to equallize the collector currents of Q29 and Q30, preventing signal injection into the sense amplifier power rails.

L6 and L7 isolate the amplifier power rails from the 15V supply at HF. C50 is the main frequency-response compensation capacitor, providing smooth roll-off, with unity gain at around 5MHz.

On the IV Range, the output from Q31 is returned at low impedance, as 100% negative feedback to the amplifier input, via the closed contacts of RL12-8/14.

4.11.5 Millivolt Loop

(Circuit Diagram 430447 pages 4.7-1 and 4.7-2)

The basic 1V loop is extended by inserting a switched, passive, attenuator network. The switching circuit connects the selected millivolt output via RL19-11/8 directly to the SHI(ACV) line, not 'PHI'. Thus only the two front panel Sense Hi and Lo terminals are used to connect to the load.

The software forces Remote Sense OFF in the millivolt ranges. Except for a series resistor (R154) on the 1mV range, the AC1V signal is connected directly to the input of the Sense Amplifier at RL8-13. The Amplifier circuit remains permanently in its non-inverting 1V configuration for all three millivolt ranges, so local sensing is carried out at 1V range levels.

Thus the output value at the terminals depends on both the calibrated value of the AC1V signal and the division ratio of the attenuator. In addition to the 1V range calibration, each millivolt range is also 'Autocalibrated' separately (refer to Section 1).

4.11.5.1 Millivolt Attenuators

(Fig. 4.11.2)

The AC1V signal is diverted from its 1V range route by the un-energized contacts of relay RL7. It is applied to the attenuator network via RL7-11.

The fixed chain (formed by R120 in series with the parellel combination of R112B and R110) is permanently connected between RL7-11 and the Common-2 star-point. Three levels of attenuation are achieved by switching R112A and R118. Relay RL5 is eneregized for the 10mV range only, RL6 for the 100mV range. The three arrangements are shown in Fig. 4.11.2.

On the 1mV range, the series resistor R154 is connected between RL7-11 and the Sense Amplifier input via RL11-5, but it is shorted on the 10mV and 100mV ranges by the closed contacts of RL5 and RL6 respectively.

Relay RL4 is energized on all millivolt ranges. The attenuator output is passed out to the SHI(ACV) line via RL4-8/9 and RL19-11/8. Capacitor C89 defines the specified bandwidth, filtering noise at HF.

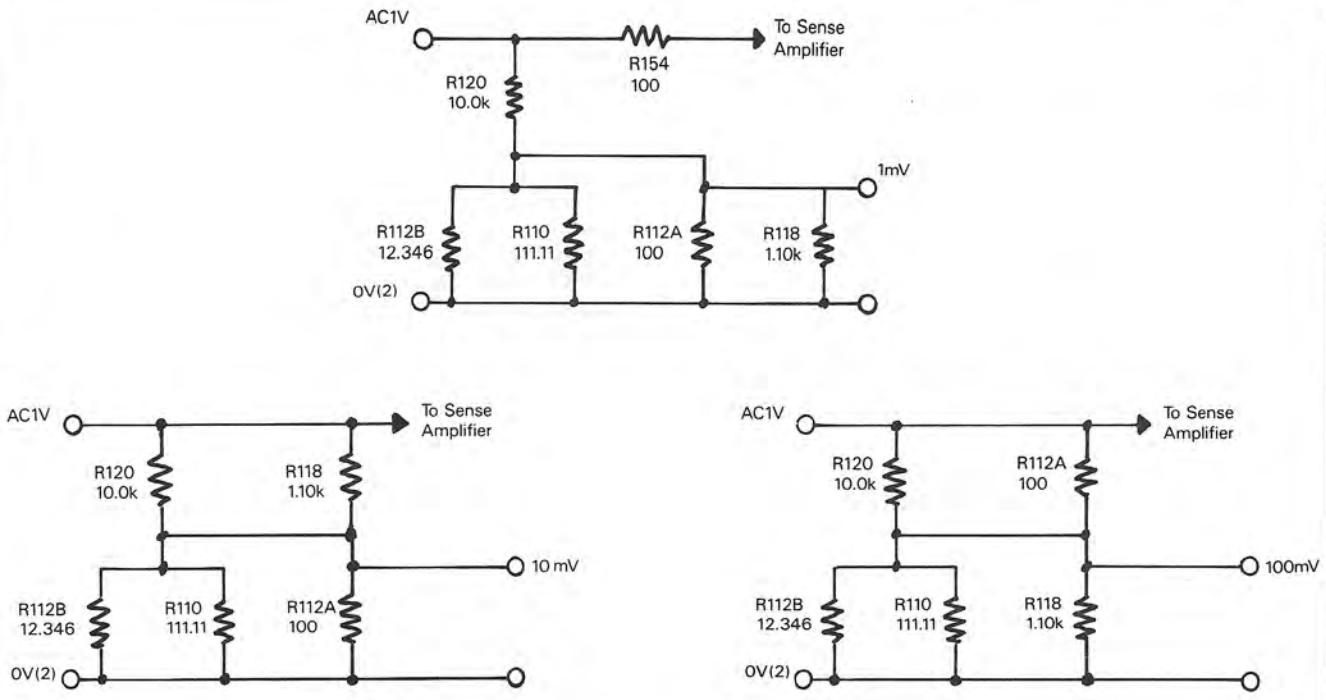


FIG. 4.11.2 MILLIVOLT ATTENUATORS
(Resistance in Ohms)

4.11.6 10V Loop

(Circuit Diagrams: 430446 page 7.6-3,
430450 page 7.9-1 and 430447 page 7.7-1)

As noted in section 4.11.2, the 1V Buffer is part of the power delivery system for all ranges. On the 10V range its output (AC1V) passes via J6-41 from the Sine-Source assembly and into the Power Amplifier assembly (PA) at J9-36.

The AC1V signal is amplified by a factor of 10 in the inverting 10V Power Amplifier, whose output is switched onto the 'AC 10V + 100V' line. This 10V range signal returns to the AC assembly at relay contacts RL17-13/4. It passes through RL19-2/5 to the PHI(ACV) line at J7-27.

The 10V range outputs then follow the same route (to and from the output terminals) as the 1V signals. Whether in Remote Sense or not, the sensed voltages return via the SHI(ACV) line to the same Sense Amplifier used for 1V range signals.

With 10V range selected, the sense amplifier has an inverting gain of 0.1, returning the signal to the 1V levels required by the Sine/Quasi-Sine comparator.

4.11.7 10V Power Amplifier

(Circuit Diagram 430450 page 7.9-2)

The AC1V signal enters the PA assembly at J9-36, passing to the input of the 10V Power Amplifier via relays RL4-9/13 and RL3-9/13. It is referred to common 2B by developing a voltage across R124. The amplifier is best regarded as having separate DC and AC paths.

4.11.7.1 DC Path

The DC path is blocked by C56; M17 is the DC input amplifier, connected as an integrator with diode clamping. M19 operates as an inverter in open loop, so applies high DC gain to the output from M17 on M19-2.

The output from M19 drives both halves of the symmetrical, inverting, discrete power amplifier through current-limiters Q21 and Q24, and is buffered by emitter-followers Q22 and Q23. Q27 and Q29 form a voltage amplifier, driving the complementary output stage Q32 and Q33. R119 and R120 set the gain of the discrete stages to approximately 4.5.

The forward amplification contains three inversions, DC negative feedback being applied to M17 inverting input by R122, defining an overall gain of 10 in conjunction with input resistor R123.

The effect of the DC path is to sense and correct the DC offsets throughout the whole AC amplifier, referring the output to Common-2A at M17-3.

4.11.7.2 AC Path

The AC path is blocked by the integrator M17, but is applied to the non-inverting input of M19 through the blocking capacitor C56. M19 operates in open loop, applying its output to the discrete power amplifier (see 4.11.7.1 above).

The amplifier AC gain is also set to 10 by R122 and R123, the circuit time constants being selected to allow overall instrument output operation over the full frequency range of 10Hz to 1MHz.

4.11.7.3 Power Supplies

M17 and M19 are supplied from ± 15V common-2A rails, the discrete amplifier from the ± 38V supply, which is used solely for this purpose.

4.11.7.4 Overload Detection

The $\overline{\text{LIM ST}}$ line, connected to D74 anode, is pulled up to 0V (in-guard logic-1) in the Reference Divider assembly (page 7.4-4) by AN2-9/1 (1MOhm). The Error OL message results from this line being driven to logic-Ø.

Overload detector Q31 reaches Vbe threshold on output current peaks, when the RMS value in R139 and R141 exceeds approximately 80mA. Similarly, Q34 detects peak currents in R147 and R149. In either case, Q34 conducts, pulling diodes D71 and D74 cathodes down to −15.7V. The $\overline{\text{LIM ST}}$ line is driven to logic-Ø, so the status message is returned to the CPU via the SSDA serial interface, and the Error OL message is displayed.

This does not preclude further increase in output current, but the accuracy specification is not guaranteed.

4.11.7.5 Overload Limiting

If the RMS output current increases to approximately 100mA, the peaks of current cause the Vbe threshold of Q28 or Q30 to be exceeded, shunting the base current of the corresponding voltage amplifier. Thus the output drive to the final stage is limited.

4.11.7.6 Output Protection

The output current passes through the combination of R144 and L8. At low frequencies the inductor provides a low output impedance, whereas at high frequencies the resistor stabilizes the amplifier when driving capacitive loads.

4.11.8 10V Sense Amplifier

(Circuit Diagram 430447 page 7.7-2)

The same amplifier is used on the 10V, 1V, 100mV, 10mV and 1mV Ranges. Its main purpose is to buffer the sense voltage, providing a high impedance input, low DC offset and flat frequency response.

On the 10V range an inverting configuration is employed. The circuit divides by 10, scaling the sense signal down to 1V range levels, for input to the Sine/Quasi-Sine comparator.

On the 1V and millivolt ranges it is connected as a voltage-follower. The millivolt ranges are simply the 1V range after passive attenuation, sensing always being carried out at the 1V level.

Separate arrangements are made for attenuation and scaling oin the 100V and 1kV ranges. These are described in Section 4.13.

4.11.8.1 General

A general description of the Sense Amplifier is given in Section 4.11.4.1 for the 1V range.

4.11.8.2 10V Range Configuration

On the 10V Range, relays RL14 and RL3 are both energized. Relays RL8, RL11, RL12, RL13, RL15 and RL16 remain un-energized as shown in the diagram.

The 'SENSE HI' signal is routed to the inverting input of the amplifier through the closed contacts of RL14 and resistor R115. With relays RL8 and RL11 not energized, the non-inverting input is referred to SIG LO.

The output from Q31 is returned via R121 as negative feedback to the amplifier input, the contacts of RL12-8/14 being open.

Thus the circuit is configured as an inverting amplifier, resistors R115 and R121 scaling the sense signal down by a factor of 10. Extensive screening is employed at the amplifier's virtual ground, bootstrapped by buffers Q46 and Q41 to follow the virtual-common potential. This reduces the input capacitance, which is further compensated by feedback capacitor C60.

4.11.9 AC Assembly Logic and Relay Drives
(Circuit Diagrams 430447 page 7.7-5)

The analog control signals are transferred into guard on the Reference Divider assembly, and latched as 'Q' outputs in the Serial/Parallel Data Converter. Offset positive logic is used:

logic-Ø = −15V, logic-1 = 0V.

The signals enter the AC assembly via J7 from the Mother assembly.

M28 and M29 are inverting, open-collector Darlington drivers. The relay-drive logic places a logic-1 (0V) on the input of the selected drivers and logic-Ø (−15V) on those not required. A selected driver operates its relay by pulling its output to −14V.

Whenever a switching command has been received, the CPU performs a control-data transfer and the $\overline{\text{UPD (IG)}}$ line from J7-53 is pulsed to logic-Ø for 50ms. Q19 is turned on, applying +15V to the relays connected to its collector. The selected relays are thus energized by 30V, but after the $\overline{\text{UPD(IG)}}$ pulse has ended Q19 turns off,and they are held on by the -12.6V between−1.4V at the cathode of D20 and−14V at the selected driver output. This method reduces the heat, generated locally by energized relay solenoids, in the relay contacts.

FETs Q42 and Q43 damp the coil of RL12 and RL13; diodes D59 and D60 isolate the parts of the printed circuit to these relays which are sensitive to power-common breakthrough, when they are deselected. D55 and D56 are overswing diodes.

4.11.9.1 Range Switching
(Page 7.7-5)

Range control data is input as a 3-bit code on AC RØ, AC R1 and AC R2 lines. The bit-pattern is decoded to '1 of 8' by M25, to energize the correct relays for the selected range.

In the 4200 only eight of the M25 'Q' outputs are connected. The resulting variants are listed in Table 4.11.1 against range selections.

Function Note |1|	Range	Range Code $ACR_{2-Ø}$ ACR_2	ACR_1	$ACR_Ø$	M25 Output at Logic-1 'Q'	Pin	Relays Energized [* = Energized] 2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
AC Volts	1000V	0	0	0	QØ	3	*								*			*			*				*
	100V	0	0	1	Q1	14	*								*					*		*		*	
$\overline{\text{(AC FNCT}}$ at Logic-Ø,	10V	0	1	0	Q2	2	*	*							*				*			*		*	
	1V	0	1	1	Q3	15	*	*				*	*		*		*							*	
$\overline{\text{IFNCT}}$ at Logic-1)	100mV	1	0	0	Q4	1	*	*	*		*				*	*	*							*	
	10mV	1	0	1	Q5	6	*	*	*	*					*	*	*							*	
	1mV	1	1	0	Q6	7	*	*							*	*	*							*	
	Any	1	1	1	Q7	4	*	*							*								*	*	
AC Current $\overline{\text{(AC FNCT}}$ at Logic-1,	100μA, 1A	0	1	1	Q3	15	*	*				*	*	*			*							*	
$\overline{\text{IFNCT}}$ at Logic-Ø)	1mA, 10mA, 100mA	0	1	0	Q2	2	*	*						*					*			*		*	

Note |1| With the 4200 operating normally: either $\overline{\text{AC FNCT}}$ or $\overline{\text{I FNCT}}$, but not both, will be at logic-Ø; unless SAFEtY message is displayed.

TABLE 4.11.1 AC ASSEMBLY SWITCHING LOGIC

4.11.9.2 $\overline{\text{AC FNCT}}$ and I $\overline{\text{FNCT}}$ Logic
(Page 7.7-5)

In addition ot its primary function of controlling Voltage range switching, the AC assembly logic also needs to respond to Current range selections if Option 30 is fitted; because the AC voltage reference for the Current assembly is generated by the Voltage circuitry. For this purpose the two signals $\overline{\text{AC FNCT}}$ and I $\overline{\text{FNCT}}$ are used.

$\overline{\text{AC FNCT}}$ is at logic-Ø only when Voltage output is selected, holding M25-11 'D' input at logic-1, and energizing relays RL2 and RL10. The bit-patterns controlling the voltage range switching are shown on Table 4.11.1.

$\overline{\text{I FNCT}}$ is at logic-Ø only when Current output is selected, holding M25-11 'D' input at logic-1, and energizing relays RL2 and RL9. This connects the ACI REF lines (J7-69 to J7-72) to the ACV lines. The 10V range circuitry is used on the 100mA, 10mA and 1mA Current ranges, but the 1V range circuitry is used on the 100μA and 1A ranges. The bit-patterns controlling the current range switching are also shown on TAble 4.11.1.

The signals $\overline{\text{AC FNCT}}$ and I $\overline{\text{FNCT}}$ are never at logic-Ø at the same time in normal operation. The only time they are at logic-1 together is when all outputs from the Control Data latches in the Reference Divider are 'Tristated'.

4.11.9.3 'AC Zero'

For zero output, the lines from the voltage generators to the I + and I − terminals are disconnected by deselection of the ranges, and a hard short is placed across the output lines by RL18.

The AC $R_{2-Ø}$ code is '1,1,1'. This sets M25-4 to logic-1 (energizing relays RL18) and all other M25 range outputs to logic-Ø (the resultant bit-pattern is shown in Table 4.11.1). Thus all ranges are deselected, but relays RL2 (ACV and ACI), RL3 (Low Voltage Output), RL10 (ACV) and RL19 ($\overline{\text{1kV}}$) remain energized). Relay RL18 connects the star-point of Common-2B (PLO) to the PHI (ACV) line.

4.11.9.4 'BARK DELAYED'

The 'BARK' signal does not affect the AC assembly relays. However, if the Watchdog is activated, the CPU imposes OUTPUT OFF conditions and forces the Precision DC Reference to ramp down to zero, so the PHI REF voltage also falls to zero.

All outputs from the Control Data latches in the Reference Divider are 'Tristated' by the 'BARK DELAYED' signal. This allows the pull-up resistors (AN4 and AN5) to become effective.

The $\overline{\text{AC FNCT}}$ and $\overline{\text{I FNCT}}$ are pulled to logic-1, and the AC $R_{2-Ø}$ code is '1,1,1'. This imposes 'AC Zero' conditions on the analog sircuit, but RL2 and RL10 are also de-energized. So the DC precision reference is disconnected from the quasi-sinewave generator; the Sense and Power Lo lines are disconnected from the sense amplifiers.

4.11.10 Output Control Assembly, Logic and Relay Drives
(Circuit Diagrams 430550 Page 7.5-1)

The analog control signals are transferred into guard on the Reference Divider assembly, and latched as 'Q' outputs in the Serial/Parallel Data Converter. Offset positive logic is used:

logic-Ø = —15V, logic-1 =0V.

The signals enter the Output Control assembly via J5 from the Mother assembly.

The five inverters of M3 are open-collector Darlington drivers. The relay-drive logic places a logic-1 (0V) on the input of the selected drivers and logic-Ø (—15V) on those not required. A selected driver operates its relay by pulling its output to —14V.

Whenever a switching command has been received, the CPU performs a control-data transfer and the $\overline{\text{UPD (IG)}}$ line from J5—104 is pulsed to logic-Ø for 50ms. Q1 is turned on, applying +15V to the relays connected to its collector. The selected relays are thus energized by 30V, but after the $\overline{\text{UPD (IG)}}$ pulse has ended Q1 turns off, and they are held on by the —12.6V between —1.4V at the cathode of D1 and —14V at the selected driver output. This method reduces the heat, generated locally by energized relay solenoids, in the relay contacts.

4.11.10.1 Remote Sense Logic

With Remote Sense selected, the REM SENSE signal is at logic-1. RL3 and RL4 are energized via M1-6 and M3-16 removing the shorts from across the PHI/SHI lines and PLO/SLO lines. Also, RL3-5/11 completes the circuit of PLO to the voltage output relay RL5. With Remote Sense off, RL3 and RL4 are un-energized, and their contacts are as shown (but see 4.11.10.3 below for Current ranges operation).

4.11.10.2 Remote Guard Logic

With Remote Guard selected, the REM GU signal is at logic-1. RL7 is energized via M1-2 and M3-13 disconnecting the internal guards and the Guard terminals from PLO. With Remote Guard not selected, the guards and terminals are connected to PLO as shown.

4.11.10.3 $\overline{\text{AC FNCT}}$ and $\overline{\text{I FNCT}}$ Logic
(Page 7.5-1)

In addition to its primary function of controlling the output switching, the Output Control assembly logic also needs to respond to Current function selection.

If Option 30 is fitted, the outputs from the voltage circuits need to be isolated from the output terminals. Also, because the AC voltage reference for the Current assembly is generated by the Voltage circuitry, the output/sense loop is completed in the AC assembly. Thus the local sense connections between PHI and SHI, and between PLO and SLO, are not required, and could generate noise in the loop. For this purpose the two signals $\overline{\text{AC FNCT}}$ and $\overline{\text{I FNCT}}$ are used.

$\overline{\text{AC FNCT}}$ is at logic-Ø only when Voltage output is selected, energizing relays RL5 and RL6 via M4-6 and M3-11, providing the Output is On and the watchdog has not 'barked'. For Current ranges, $\overline{\text{AC FNCT}}$ is at logic-1, so RL5 and RL6 are un-energized as shown, breaking the lines between the voltage circuitry and the output terminals.

$\overline{\text{I FNCT}}$ is at logic-Ø only when Current output is selected, ensuring that relays RL3 and RL4 are energized, even though Remote Sense is not selected on Current ranges. This removes the local sense shorts, as though in Remote Sense.

The signals $\overline{\text{AC FNCT}}$ and $\overline{\text{I FNCT}}$ are never at logic-Ø at the same time in normal operation. The only time they are at logic-1 together is when all outputs from the Control Data latches in the Reference Divider are 'Tristated'.

4.11.10.4 'HIGH I LIMIT' and 'AC 1kV RANGE' Logic

The effects of these signals are described in paras 4.11.2.3 and 4.12.7.5.

4.11.11 High Voltage Status Detector
(Circuit Diagram 430550 Page 7.5-2)

In order to provide information to the CPU, so that it can decide whether the High/Low voltage state is as demanded, the voltage level on the PHI(ACV) line is sensed and compared against a reference.

M5 is a dual comparator whose hysteresis is set to ±0.9V by D8/D9, R34/R35 and R37/R36. For as long as the voltage on the PHI(ACV) line remains within approx. ±125V, the division ratio of M7 keeps the input to M5-5/9 within the ±0.9V hysteresis, and M5-12/7 remains at logic-1 (approx. +14V).

Monostable M2 is set to produce a logic-1 at its Q output (M2-7) unless its B input at M2-5 is edge-triggered negatively. In 'Low Voltage State' conditions no trigger is given, so M2-7 remains at logic-1, D4 is reverse-biased, Q2 is cut off and the $\overline{\text{HV ST}}$ line remains at the analog control logic-1 level of 0V.

If the instantaneous PHI(ACV) voltage exceeds the ±125V limits (corresponding to a sinewave RMS of >90V), either M5-7 or M5-12 pulls towards logic-Ø. Current source Q3 permits only 3mA to flow in M5 output circuit, so the voltage input to M2-5 (B trigger) suffers a negative-going trigger edge.

Monostable M2 produces a negative-going pulse of 130ms duration, which forward-biasses D4, Q2 conducts and the $\overline{\text{HV ST}}$ line transmits a logic-Ø pulse of 130ms duration. This is passed to the CPU, via the status register in the reference divider and the serial data interface.

The CPU has to make a decision, as to whether the programmed output voltage and the detected state are compatible. If they are not, the CPU displays 'FAIL 2', switches Output OFF, trips the watchdog and sets 'FAIL 5' display. Refer to section 2.

4.11.12 Overvoltage Detector
(Circuit Diagram 430550 Page 7.5-2)

An absolute limit of 1440V RMS is placed on the operation of the internal output circuitry. In order to give effect to this limit, the voltage level on the PHI(ACV) line is sensed and compared against a reference.

M6 is a dual comparator whose hysteresis is set to ±1.22V by D8 and D9. For as long as the voltage on the PHI(ACV) line is less than 1440V RMS, the division ratios of M7, R26 and R25 keep the input to M6-5/9 within the ±1.22V hysteresis, and M6-12/7 remains at logic-1 (approx. −1V). Q2 is cut off and the LIM DET line remains at the analog control logic-Ø level of −15V, due to D6 being below threshold.

If the instantaneous PHI(ACV) voltage exceeds the 1440V RMS limits (corresponding to a sinewave peak of ±2025V), either M6-7 or M6-12 pulls towards logic-Ø. Q4 conducts, forward biassing D6 and lifting the LIM DET line to approx. −1V (analog control logic-1 level). This is passed to the $\overline{\text{LIM ST}}$ logic circuitry.

Refer to Section 4.12 for subsequent action. The event is reported to the CPU via the $\overline{\text{LIM ST}}$ logic, resulting in an 'Error OL' display.

4.12 HIGH VOLTAGE POWER DELIVERY
(Circuit Diagram 430450 page 7.9-1)

The AC1V signal, generated by the 1V Buffer in the Sine-Source assembly, enters the Power Amplifier as for the 10V range; but the 10V Amplifier is bypassed for the high voltage ranges.

On the 100V range, the signal is switched directly into the 100V Amplifier, where it is scaled up by a factor of 100, the amplifier output being delivered via the 'AC 10V+100V' line to the PHI (ACV) line on the AC assembly.

For the 1000V range the DC Reference is scaled in software, so that the AC1V signal Full Scale value represents 1100V output. The signal is routed through extra stages of amplification before being applied to the 100V Amplifier, whose output now drives one of two 1:6 step-up transformers (LF or HF). The power-amplifier gain on the 1000V range is controlled by feedback from the transformer secondary, into the input of the 1000V Error Amplifier. The 'AC 1kV' line transfers the transformer output to the AC assembly, where it is switched onto the PHI(ACV) line.

4.12.1 100V Range Power Routing
(Circuit Diagrams: 430450 pages 7.9-2 and 7.9-3; 430447 page 7.7-1)

'AC1V' enters the Power Amplifier assembly at J9-36 (page 7.9-2). Relay RL3 is un-energized, shorting the 10V Amplifier input; and RL4 is energized, routing the AC1V signal to the 100V Amplifier as '100V I/P' (page 7.9-3).

Energized relay contacts RL2-8/4 apply the signal to the Gain Stage, which provides drive to the power amplifiers in the positive and negative heat sinks, via J3-12 and J3-11. The single-ended output from the heatsinks at J3-9 passes via R89, L7 and relay RL2-13/9, to RL3-6 (page 7.9-2), and onto the 'AC 10V+100V' line via RL4-4/8.

On the AC assembly (page 7.7-1), the signal is routed to the PHI(ACV) line as for the 10V range.

4.12.2 100V Power Amplifier

The 100V amplifier is in three stages:

(1) **Gain Stage:** this is similar to the first stage of the 10V amplifier, but with a different distribution of gain.

(2) **Driver Stage:** providing most of the gain, this stage runs from a regulated 400V supply.

(3) **Buffer Output Stage:** two complementary MOSFET circuits, located on the positive and negative heatsinks, provide a single-ended output with the required voltage swing, at low impedance.

The voltage gain for the whole 100V amplifier is set at 100 by the input resistors R74/R71 and the feedback resistor R88.

The 100V amplifier is also used on the 1000V range to drive the step-up transformer.

4.12.3 Gain and Driver Stages
(Circuit Diagram 430450 pages 7.9-2 and 7.9-3)

The AC1V signal enters the PA assembly at J9-36, passing to the input of the 100V Power Amplifier via relays RL4-9/13 and RL2-8/4. It is referred to common 2B by developing a voltage across R72.

4.12.3.1 DC Offset Correction

Integrator M10 is the DC input amplifier, with diode clamping. It provides a DC input to the non-inverting input of the AC input amplifier, M8, controlling its DC offset. This is similar to the arrangement in the 10V Amplifier.

4.12.3.2 AC Signal Processing

M8 is a high speed hybrid amplifier operating as an inverter. With link LKD normally made, its stage gain is approximately 2.5, frequency compensated by C18 and C72. It operates from the ±15V Common-2B supplies, but its signal output is converted into a current by Q10 and Q8; allowing its mean DC voltage to reach the −400V levels required to operate the driver MOSFET output circuit. Diodes D44, D43 and D36 prevent negative latch-up.

Voltage Regulator M21 sets its pin 1 to +12V. Common-emitter buffer Q10 drives the capacitance of Q8 source-gate from the output of M8, forming a cascode current generator. The drain of p-channel MOSFET Q8 passes the signal current to the mirror Q12/Q11 at voltages close to −400V.

The current-mirror output transistor M11 is also in cascode with its associated MOSFET Q9. Emitter resistor R53 defines the current in Q9, the ratio R52/R53 setting the mirror's current gain.

MOSFETs are inherently capacitive, so measures are taken to nullify the effects, on slew rate, of the capacitive currents between Q9 electrodes. The cascode arrangement ensures that any source-gate and source-drain capacitive currents join the main flow of source current and have little effect on slew rate.

The Miller feedback of the drain-gate capacitance has the greatest effect on slew rate, generating AC currents between anti-phase electrodes which normally pass into the input circuit. In this arrangement, Q13 diverts these currents back into the cascode current, while maintaining a standing bias of about 4 volts between gate and source. Both these measures minimize the reduction of Q9 operating bandwidth.

R51 and D42 provide Q13 base bias, and D51 protects the bias curcuit. The high-power resistor R49 refers the bias circuit to Common-2, and C26 stabilizes the base-emitter bias of Q13. Zener diode D39 protects the MOSFET from source-gate voltage breakdown.

4.12.3.3 Driver Regulator

At Full Scale on the 100V range, the output from the driver is 200V RMS. This requires Q9 drain to provide a peak-to-peak voltage swing approaching 600 Volts, as there is no voltage gain in the heatsink power amplifiers. The positive supply which provides Q9 current therefore needs special regulation.

The 400 volt supply is at this point unregulated, so can contain line ripple and level variations, this noise level being critical to the output performance. To define a stable supply voltage, a DC restoration circuit is employed as a trough detector, maintaining a level about 5V below the most negative excursions of the ripple.

At power-up, 75V zener D57 allows a rapid charge of reservoir capacitors C49 and C59, until the charge reduces D57 voltage below the avalanche level. When D57 cuts-off, R100 provides a charge path of 1Mohm, giving a time constant of approx. 10 seconds. The smoothed voltage across C49/C59 is divided by R101, R86 and R87; so a small voltage is dropped across R101, and M20 gate is held about 5V below the +400V(2)B line voltage. The N-channel source-follower Q20 thus provides a quiet, low-impedance DC supply voltage.

Zener diodes D60 and D61 divide the voltage across C49 and C59, so that their breakdown voltages are not exceeded. The 10V zener D54 protects the TMOS gate/source from excessive voltages. D55 is included to prevent C49/C59 discharging into the 400V rail in the event of its being shorted.

The opto-coupler M16 permits the 400V supply to be switched off, allowing D56 to assume forward bias, connecting the rail to the +38V supply. This facility is not available on the 4200 AC calibrator, the 'POSITIVE' signal from the processor being permanently set to logic-1 (0V). Thus M16-6 is isolated from M16-5.

At HF, inductor L6 appears as a current source, increasing the impedance of Q9 drain load with frequency to compensate for capacitive loading. It has the advantage of not increasing the net power dissipated in the stage; any active current source would have significant output capacitance. The 12-watt resistor R65 is the main resistive drain load for Q9.

4.12.3.4 Driver Output

The driver develops its output voltage, which can involve peak-to-peak swings of up to 600V, across the load resistor R65. Zener diode D41 is included to clamp the output in the event of the heatsinks being disconnected. This is normally held below avalanche by the current passing through a series bias divider in the Positive Heatsink assembly, via J3-11 and J3-12.

The main frequency compensation is performed by capacitor C12. This could have been connected to the drain of Q9, but the output line slew rate is sensitive to capacitive loading. Instead it is connected via J2-7 to a low impedance point in the Negative Heatsink assembly, which follows the driver output voltage swing.

4.12.4 100V Buffer Output Stage

(Circuit Diagrams 430538 page 7.13-1 and 430539 page 7.13-2)

The 100V buffer output stage is split between the Positive and Negative Heatsink assemblies. The driver output voltage is connected into the Positive assembly, and the frequency compensation feedback is derived in the Negative assembly.

The whole circuit is a complementary, single-ended push-pull amplifier with unity voltage gain. To achieve the full ±300V peak voltage output, two MOSFET source-followers are connected in cascode, for each polarity, in a totempole arrangement.

To obtain the required peak current levels, each source-follower consists of two MOSFETs in parallel. In all, therefore, eight MOSFET devices are used.

On the 100V range, the output currents are such as to bias the amplifier in class A, but on the 1000V range the output currents impose class AB conditions. Crossover distortion is minimized by a regulated bias generated by a Vbe multiplier.

Power for the amplifier is provided by the same ±400V supply that serves the driver circuit. To improve efficiency, overall power loss is reduced by regulation only where required. Thus only the driver stage is regulated, allowing the power amplifier to take power directly from the unregulated supply. Being source-followers, the 400V rail ripple is not transmitted.

4.12.4.1 Positive Heatsink Assembly

(Circuit Diagram 430538 Page 7.13-1)

N-channel MOSFETs Q1 and Q2 are connected in parallel, as are Q3 and Q4. All devices are matched for power dissipation and threshold voltage for an even dissipation of approx. 400W between the two heatsinks. All gate-source potentials are limited by 10V zeners.

The input voltage swing from the driver is present at J3-11 and J3-12, and the driver load current passes through resistors R18, R17 and the bias control R10. The Vgs multiplier Q5 acts as a shunt regulator, generating a bias of between 5V and 9V, set by R10. Zener diode D7 responds to the temperature of the heatsink to compensate for the temperature coefficients of the MOSFETs.

The 'DRIVE−' voltage at J3-11 is transferred directly to the negative heatsink input via J1-7 (Circuit Diagram 430539 page 7.13-2).

The 'DRIVE+' voltage at J3-12 is buffered by Q7 and applied to the gates of Q3 and Q4. In the event of an output short-circuit, Q6 detects the output current as a voltage across R14, imposing a hard limit of 1.5A by reducing the signal voltage at the input to the MOSFET gates.

The series gate resistors R5 and R6, together with their associated drain-gate capacitances, form the dominant pole of the amplifier. Damping resistor R19, with ferrite bead FB1, prevent local oscillations by emitter-follower Q7.

Q1 and Q2 act as buffers to provide a bootstrapped supply for the output devices Q3 and Q4. The gates of Q1 and Q2 are driven from the output line, obtained from the divider R16/R22/R23/R15. Capacitors C10 and C13 decouple any noise on the 400V rail; C11 and C12 correct any lag which may be generated by C10 and C13. C5 and C6 control the division ratio at HF, swamping any stray capacitance.

The drains of Q3 and Q4 are shorted together, and connected via J1-5 by a 10nF capacitor to the corresponding point in the Negative Heatsink, completing an AC bootstrap (BS). J1-4 and J1-1 are similarly linked to their corresponding points. This ensures that the AC swings in both polarities are identical.

The combined output from the Positive and Negative Heatsinks is transmitted back to the Power Amplifier assembly along the screen of the input connection.

4.12.4.2 Negative Heatsink Assembly

(Circuit Diagram 430538 Page 7.13-2)

This is virtually a mirror image of the positive heatsink circuit. However, because the P-channel MOSFETs are operating closer to their maximum voltage rating, they are protected by Zener diodes which limit their gate-source potentials.

The HF swamp capacitors are not required, as the whole circuit is AC-bootstrapped to corresponding points in the positive heatsink assembly, via C1, C2 and C4.

HF compensation for the driver and output stages is derived at low impedance from the junction of R2 and D12. It feeds back via J2-7 to the driver output circuit, through C12 in the Power Amplifier assembly, to avoid capacitively loading the driver output line.

4.12.4.3 Over-Temperature Detection

The two NTC thermistors in each heatsink circuit are part of a bridge network which detects excessive temperatures on the heatsinks. The action of the bridge is described in section 4.12.9.6.

4.12.4.4 100V Output Connection

DANGER **For guarding purposes, the output from the heatsinks is transmitted back to J3-9 of the Power Amplifier assembly along the screen of the input cable.**

The voltages on this screen are POTENTIALLY LETHAL. Utmost caution should be exercised when working in its vicinity.

4.12.4.5 Heatsink Removal

The 100V Amplifier can work with the heatsinks removed, because of the clamp diode in series with the driver load. If they are removed, however, J3-9 must be connected to J3-11 to maintain the feedback. In this condition, the gain falls due to loading of the driver by the AC assembly.

4.12.5 1000V Range Power Routing

(Circuit Diagrams: 430450 pages 7.9-2 and 7.9-3; 430447 page 7.7-1; 430565 page 7.14-1)

'AC1V' enters the Power Amplifier assembly at J9-36 (page 7.9-2). Relay RL3 is un-energized, shorting the 10V Amplifier input; and RL1 is energized, routing the AC1V signal to the 1000V Amplifier chain.

Energized relay contacts RL1-8/4 apply the signal to the Gain X2 Stage, whose output is summed with error feedback, providing drive to the 1kV Error Amplifier.

The 1kV Error Amplifier output is passed as '1kV ERROR O/P' via relay RL1-9/13 to the 100V Amplifier (page 7.9-3). It is input through the contacts of un-energized relay RL2-6/4.

The heatsink output J3-9 is transferred directly, as the 'OUTPUT' signal, to the 1kV ENABLE relay contacts RL6-8 and RL6-9. Relay RL7 determines whether the LF or HF transformer assembly is to be used, the OUTPUT signal being applied to the appropriate primary winding.

The secondaries of both transformers are connected into the High Voltage assembly (page 7.14-1). Relay RL2 or RL3 selects the appropriate output to be passed on to the AC assembly, via J1-28 and J1-22, as the AC 1kV signal.

The AC 1kV signal is also applied as the negative 'Error' feedback to the 1000V amplifier system. It passes through R138 and R155 on the PA assembly (pages 7.9-1 and 7.9-2), to be summed at the inverting input of M18a-2. A single net inversion is present around this loop.

On the AC assembly (page 7.7-1), the AC 1kV signal is routed by the contacts of energized relay RL20, and through fuse F2 to the PHI(ACV) line at J7-27.

4.12.6 1kV Power Amplifier

(Circuit Diagram 430450 page 7.9-1)

Amplification to a maximum of 1100V is in four stages:

(1) **Gain X2 Stage:** the AC1V signal is HF-boosted and amplified. For the 1000V range the DC Reference is scaled in software, so that the AC1V signal Full Scale value represents 1100V output.

(2) **1kV Error Amplifier:** the Gain X2 Stage output is summed with error feedback from the secondary of the step-up transformer.

(3) **100V Amplifier:** possessing a gain of 100, the output from its heatsinks drives one of two (LF or HF) step-up transformers.

(4) **Step-up Transformer:** a ratio of 1:6 allows sufficient gain in the system to provide a maximum RMS output of 1100V.

The frequency response of the amplifier is matched to the step-up transformer in use. The 'LF' signal into the amplifier is at logic-1 (0V) only when the 1kV range, and either the 100Hz or the 1kHz frequency range, is selected.

4.12.6.1 Gain X2 Stage

(Circuit Diagram 430450 page 7.9-2)

The AC1V signal is routed via relay RL1-8/4 to be developed across resistor R160. It is filtered by R162/C30 and applied to the non-inverting input of M15.

The feedback divider generates the X2 gain in M15; R159 and C67 providing HF lift. FET Q35 adds C68 on the 100Hz and 1kHz frequency ranges, activated by the LF signal at logic-1, to boost the lift.

Output from the X2 stage is applied to the 1kV Error Amplifier via its input resistors R156/R95.

4.12.6.2 1kV Error Amplifier

The input resistance to M18a is split between R156 and R95 to allow the saturation detector to reduce the gain in the event of transformer saturation.

At the inverting input of M18a the signal input is summed with the AC 1kV negative feedback signal, output from the selected transformer secondary. The resulting error is amplified by the 2 stages of M18.

On the 100kHz frequency range, the maximum voltage available from the instrument is 750V. A tapping on the HF step-up transformer secondary reduces the maximum output to this level. The signal '1kV GAIN' is therefore set to logic-Ø only on the 100kHz range, cutting off FET Q19 and restoring adequate loop gain.

The second stage, M18b, adjusts the bandpass of the amplifier to match the selected step-up transformer:

100Hz and 1kHz ranges:
Q26 connects C58 and R126 across the input resistor R97; relay RL5 connects C34 and R93 across the feedback resistor R92, also shorting C38 in the output line.

10kHz and 100kHz ranges:
Q26 connects C57 and R125 across the input resistor R97; relay RL5 connects C33 and R94 across the feedback resistor R92, and leaves C38 dominant in the output line.

These measures give the necessary loop compensation for each transformer.

When the 1000V range is selected the amplifier output is fed to the 100V Amplifier via RL1-9/13.

4.12.6.3 100V Amplifier

This operates as for the 100V range, and its output signal 'OUTPUT' is fed to relay RL6 contacts for application to the step-up transformer.

4.12.6.4 '1kV ENABLE' Relay RL6

Relay RL6 allows the OUTPUT signal from the 100V Amplifier to energize a step-up transformer, providing the following conditions are met:

The $\overline{1kV}$ signal is at logic-Ø:
This is a processor-controlled signal, set to logic-Ø when the 4200 output is switched on, in the 1000V range.

The watchdog has not 'Barked'.

The '1kV ENABLE' switch S1 on the Power Amplifier assembly is set to 'ENABLE'. S1 is situated below the left-hand ejector lever (viewed from the front of the 4200), facing the rear of the instrument. It allows the high voltage to be switched off for servicing purposes. A red LED glows when all other conditions are met.

When RL6 is closed, the OUTPUT signal from the 100V Amplifier is switched through to the contact of RL7.

4.12.6.5 LF/HF Transformer Selection

Relay RL7 is activated by the 'LF' signal, applying the 100V amplifier output to the HF step-up transformer for the 10kHz and 100kHz frequency ranges, and to the LF transformer for the 100Hz and 1kHz ranges.

The two transformer are separately located, their secondaries being connected into the High Voltage assembly. The HF transformer is selected when RL7 is un-energized, its primary being returned to Common-2C. RL7 is energized to select the LF transformer, whose primary current is sensed by the Saturation Detector.

4.12.6.6 Saturation Detector

To obtain the required performance, the LF transformer core is constructed from a material with high remanence. It is possible for the 1kV range to be deselected when the core is magnetized, and subsequently reselected in the same sense, with resultant saturation.

The Saturation Detector circuit is activated by sensing any excess primary current in R114, associated with the loss of reactance. It progressively removes the signal input to M18b during half cycles of the appropriate sense until the core recovers, then automatically returns to its quiescent mode.

The dual amplifier M20 is biassed by R115-R118 to approximately 1V on each input. Under normal operating conditions, the unsaturated core reactance holds R114 current down, so the voltage developed across R114 is insufficient to overcome the bias. The output from both amplifiers is of negative polarity, both diodes D58 and D59 are reverse-biassed, and FET Q18 is cut off by its gate being pulled down to −15V.

When the core saturates, the current in R114 rises rapidly and its voltage exceeds the bias on one of the detector amplifiers. One diode conducts, forcing Q18 into conduction, so the current in the transformer core is reduced to zero.

On the next half-cycle the current is reversed, so saturation is reduced. If the core saturates on successive half-cycles, they again activate the detector with further reduction. The process continues until the core remains unsaturated over the full dynamic range of the primary current, when the detector becomes inactive.

4.12.7 Power Supplies and Protection

Three main power supplies are employed in the Power Amplifier:

(1) **±15V Common-2 in-guard supply.**
This is used for all low voltage applications, including the switching and functional logic. For the most part the logic conforms to the standard: logic-Ø= −15V; logic-1=0V.

(2) **±38V Common-2 supply.**
Required solely for the 10V Power Amplifier, this supply is generated on the separate 38V Power Supply assembly (Refer to page 7.12-1). Part of the supply circuit is situated on the Mother Assembly.

(3) **±400V Power supply.**
Supplies the 100V Power Amplifier used for the 100V and 1000V ranges. The line transformer secondary output is rectified and smoothed on the Mother assembly, and the main regulator circuitry for the driver stage is contained on the Power Supply / Current Heatsink. The power output stage of the 100V Amplifier receives unregulated ±400V supply.
Extensive protection is incorporated.

4.12.7.1 ±38V Supply
(Circuit Diagram 430544 Page 7.12-1)

The mains (line) transformer secondary centre tap is referred to Common-2 on the Mother assembly after passing through the 38V Power Supply assembly. This secondary also provides an adjustable AC output for the 'Common Mode Null' balancing circuit.

A single bridge rectifier on the Mother assembly provides both positive and negative raw supplies for the foldback regulator in the 38V Power Supply assembly.

The 38V supply circuit is fully described in Section 4.16, para 4.16.3.4.

4.12.7.2 ±400V Transformation and Rectification
(Circuit Diagram 430532 Page 7.16-5)

The mains (line) transformer secondary centre tap is referred to Common-2 on the Mother assembly. The secondary is switched with the secondary for the ±38V supply, to allow a lower voltage to drive the 100V power amplifier for servicing purposes. Under operational conditions in the 4200, this switch, which is situated prominently on the Mains Transformer assembly, is set to the 400V position.

A single bridge rectifier on the Mother assembly uses series diodes to achieve the high peak inverse voltage performance required for the 400V supply.

After smoothing, and part-loading by a bleeder resistor chain (the bleeder resistors also balance the voltages across the capacitors); the rectifier output is passed via J31, to provide both positive and negative raw supplies for the foldback regulator in the PS/I Heatsink assembly.

4.12.7.3 ±400V Current Control
(Circuit Diagram 430540 Page 7.13-3)

When the 400V supply is enabled, the LEDs in opto-isolators M1 and M2 are conducting, allowing their opto-transistors to be energized. As the circuits for both polarities are otherwise symmetrical, only the positive circuit is described.

Zener Diode D8 protects the source-gate circuit of level-shifter Q3. This N-channel MOSFET supplies a current of 1.4mA, as defined by Q8, to the current-monitor reference zener diode D7. This current is available only if the 400V supply is enabled by M1, otherwise Q4 base is pulled down by D1/R9, Q4 conducts via D7 and Q9 is pinched off.

Under normal conditions the Power Amplifier supply current is drawn through the P-channel MOSFET Q9, which is held in conduction by R8, R12 and D2. The current is sensed by the parallel combination of resistors R17 and R32. Although the peaks of the current taken by the power amplifier can reach 1.4A, the mean value is less than 0.5A. Ripple currents making up the difference are smoothed by the main reservoir capacitors C31 and C22 on the Power Amplifier assembly.

For mean currents more than approximately 0.5A (in particular for output short-circuits); the voltage sensed across R17/R32, subsequently divided by the attenuator R10/R9, exceeds the threshold of Q4/D7. Q4 conducts to pass current into R8, reducing the drive to Q9 gate, so the +400V(2)B voltage at D5 anode falls. When the voltage dropped by Q9 reaches 56V, zener D5 conducts and pulls Q4 base down, further reducing the drive to Q9 gate. This cumulative action is slowed only by the time constant of the combination R34/C15, so that both voltage and current on the +400V(2)B line are simultaneously closed down.

With a persistent 400V overload, the circuit cannot recover naturally from this 'foldback' mode. However, the 400V voltage is monitored. If the 400V monitor senses a failure, a status bit is passed back to the CPU via the SSDA serial link. The CPU makes three attempts to reinstate correct operation by removing the PA bias while restarting the supply via the 400V enable line. If after the third attempt the voltage does not recover, the CPU assumes that a hardware fault is present, so displays the 'FAIL 7' message.

4.12.7.4 100V Overload Detector

(Circuit Diagram 430450 Page 7.9-6)

The ±400V(2)B lines enter the Power Amplifier assembly from the PS/I Heatsink at J1-8/6 and are filtered by L1 and L2 before being applied across two neon lamps LP1 and LP3. These lamps are visible from the top and rear of the instrument when the PA board is exposed, indicating that a dangerous voltage is present.

The 400V(2)B lines continue on to power the driver stage of the 100V amplifier, where the voltage is regulated as described in sect 4.12.3.3.

The ±400V(2)C lines supply the power amplifier in the Positive and Negative Heatsinks. On the 100V range, the current in each of these lines is used as an analog of the load placed on the amplifier. (On the 1000V range, any overload is sensed by a series detector in the OUTPUT control assembly.)

The '100V A' line is set to logic-1 (0V) only when the 100V range is selected ('100V D' is not used in the 4200). Driver Q7 pinches off the two FET switches Q6 and Q37, removing the shorts from R37 and R21, thus allowing the overload detector to operate. In normal use, links LK B and LK C are not connected. Their test purpose is to allow the current mirrors Q1 and Q3 to be powered without the level-shifters Q2 and Q4.

Most of the positive output current for the heatsinks passes through the series combination of R34 and D27, the negative currents through R9 and D4. As the both positive and negative circuits are symmetrical, only the positive circuit is described.

Current mirror Q3 diverts approx. 1.8% of the positive supply current into the level-shifter Q4, R36 and into the common resistor R37. Similarly Q1 draws current out of R37. Under no terminal load conditions these two currents are balanced, even if the output voltage is high.

Any AC output load current from the power amplifier is reflected by ripple currents in both positive and negative supplies. The net instantaneous current flowing in R37 alternates in synchronism with the output cycles, its amplitude increasing as the load current increases. So the amplitude of the alternating voltage across R37 is an analog of the output load current, and can be compared against a scaled reference voltage.

A window comparator is formed from the two halves of M2 and the voltage across R37 is applied to both halves. The outputs at M2-12 and M2-7 are uncommitted. Each half is biassed by approx. 1.025V in the correct polarity, so that unless any voltage peak across R37 exceeds this level, both M2 outputs will be pulled to 0V by R21. So Q9 remains cut-off.

Any peak greater than 1.025V ovrcomes the bias on one half, causing its output to fall to −15V, so Q5 conducts, lifting TP2 to 0V (logic-1). Diode D13 is part of a wired-OR gate which then sets the limit detector latch M5a (page 7.12-5), resulting in the $\overline{\text{LIM ST}}$ status bit being set to logic-1. This is passed to the CPU via the SSDA serial link. Meanwhile the LIM DET signal passes via D38, becoming the 'I LIM 100V AMP' signal to Q14 (page 7.12-3) in the gain stage of the 100V amplifier. Q14 conducts, shorting the input to the amplifier to Common-2, and reducing the amplifier output.

The CPU tries to toggle the latch, and will succeed once the overload is removed. While it is clocking the toggle with 'I LIM RST', it displays the message 'Error OL'. Note that the action described trips the output off. Thus removing a terminal overload will not restore the output.

4.12.7.5 1000V Overload Detector

(Circuit Diagram 430550 Page 7.5-1)

For the 1000V range, so as to protect the step-up transformers, overloads are detected directly in the output lines to the terminals. For this range only, two resistors are inserted in the PHI(V) line in the Output Control assembly. The voltage across the resistor is rectified and compared against a reference. If the voltage is excessive, the comparator generates a LIM DET signal.

The 'AC 1kV RANGE' signal enters at J5-102. This is at logic-1 to energize relay RL1, only if the 1000V range is selected. RL1 removes the short from R31 and R32.

The 'HIGH I LIMIT' signal enters at J5-98. When the 1000V range is selected, this is at logic-1 only for the 10kHz, 100kHz and 1MHz frequency ranges. It energizes relay RL2, shorting R32, so that higher currents are required to trip the LIM DET signal. As frequency increases, so do the currents taken by the capacitance of the internal tracking and wiring; R31 is compensated by C16 to bypass this capacitive loading.

A diode-bridge rectifies the voltage developed across the selected resistor(s). The voltage is limited to 10V by D14, and resistor R33 sets the trip current level for the opto-isolator M8.

The isolator operates from the 5 volts between −10V and −15V. In normal operation M8 output at M8-6 is open-collector so Q5 does not conduct. When the output current is sufficient to trip M8, Q5 emitter is pulled low and so Q5 conducts, its collector current being drawn through R21 and R20 (page 7.5-2). Q4 is switched on, setting the LIM DET line to logic-1.

4.12.8 PA Power Supply Monitors
(Circuit Diagram 430450 Page 7.9-4)

All three power supply voltages: 15V, 38V and 400V; are monitored using three virtually identical comparators to initiate individual 'FAIL' messages. In addition, if either the 400V or the 15V circuit detects a low power supply voltage, the 400V supply is disabled. Because the monitors are so similar, only the 400V circuit is fully described.

4.12.8.1 400V Monitor

Zener diode D5 is the 2.45V reference for all three comparators. It is ballasted by R30, and its +2.45V is applied to the non-inverting input of M3d. Its voltage is divided equally by two sections of AN3, applying +1.23V to the inverting input of M3a.

The +400V(2)B line voltage is divided down to approximately 3.25V by R3 and R16, and applied to the inverting input of M3d. This is sufficient to hold M3d-14 output negative. Diode D20 is held below threshold by R7 and a 1Mohm pull-up on the 400V(2) status line in the Reference Divider. If the +400V line voltage falls to 300V, M3d output goes positive, limited by D6. D20 conducts, setting the status line to logic-1 (0V), positively limited by D8.

The −400V(2)B line voltage is similarly divided down to approximately +0.9V by R4 and R26, and applied to the non-inverting input of M3a. This is sufficient to hold M3a-1 output negative. Diode D23 is also held below threshold. If the −400V line voltage falls to −315V, M3a output goes positive, limited by D7. D23 conducts, again setting the status line to logic-1 (0V).

The output line gives an input to the 400V enable logic (sect 4.12.9.4).

In normal 400V operation R31 is shorted by the 400V/50V switch on the Mains (line) transformer. When this is set to 50V, the 'Lo SUPPLY A' line is connected to −15V, effectively disabling the monitor output by holding the 400V(2) line at logic-Ø.

4.12.8.2 38V Monitor

The thresholds for operation of the 38V fail flag are: +32V and −33V. Otherwise the action is the same as the 400V monitor.

4.12.8.3 15V Monitor

The thresholds for operation of the 15V fail flag are: +12.05V and −12.3V. The action is similar to the 400V monitor, but because the 15V circuit is running from the supply it is monitoring, extra precautions are required and the action is slightly modified.

Under normal operating conditions, D21 and D22 are reverse-biased, so the 15V(2) FAIL line is pulled to logic-Ø by R17.

If the −15V supply fails, the action is as before, but in this case it is assisted by M3 power supply being between +15V and 0V. D22 will conduct to drive the 15V(2) FAIL line to logic-1.

On the other hand, if the +15V supply fails, the reference supply to D5 would collapse and both amplifiers would run between 0V and −15V (D32, shown on page 7.9-6, prevents the +15V line reversing). The 2V zener D16 then ensures that as the +15V supply collapses, M3c-9 is pulled more negative than M3c-10 at all times, regardless of supply levels. Thus M3c-8 output is driven to its positive rail, which can source enough current to hold the 15V(2) FAIL line at logic-1.

The 15V monitor output line also gives an input to the 400V enable logic (sect 4.12.9.4).

4.12.9 PA Logic and Relay Drives
(Circuit Diagrams 430450 Pages 7.9-4 and 7.9-5)

The CMOS logic operates between 0V and −15V, with logic-1=0V, and logic-Ø=−15V. Relays are tied to +15V on one side, and controlled on the other by the uncommitted collector of an inverting Darlington driver. Thus when the input to the driver is logic-1, the relay is energized by ± 15V; and when the driver input is logic-Ø, its output is high impedance, releasing the relay.

4.12.9.1 Range Switching
(Page 7.9-5)

In the 4200, the inputs to decoder M7a are not connected outside the PA assembly. They are therefore all pulled to logic-1 by AN4, including the 'E' input, so all 'Q' outputs are at logic-Ø.

The three inputs AC RØ, AC R1, AC R2; carry the range switching information, and are decoded by M7b as follows:

	M7b outputs			M7b inputs		
	Q2	Q1	QØ	E	B	A
Range Select	AC R2	AC R1	AC RØ			
1000V	Ø	Ø	Ø	Ø	Ø	1
100V	Ø	Ø	1	Ø	1	Ø
10V	Ø	1	Ø	1	Ø	Ø
1V	Ø	1	1	Ø	Ø	Ø
100mV	1	Ø	Ø	Ø	Ø	Ø
10mV	1	Ø	1	Ø	Ø	Ø
1mV	1	1	Ø	Ø	Ø	Ø

10V Range Logic

The input to Q6-1 is always logic-1. On the 10V range only, the input to Q6-2 is logic-Ø, giving logic-1 at M6-3. Thus relay RL3 operates only when the 10V range is selected.

100V Range Logic

The input to Q12-8 is logic-Ø only when the 10V range is not selected, and the input to Q12-9 is logic-Ø only on the 100V range. This gives logic-1 at M12-10, so relay RL2 operates only when the 100V range is selected.

1000V Range Logic

The input to Q13-4 is logic-Ø only when the 1000V range is selected, so relay RL1 operates only when the 1000V range is selected. An 'AC 1kV RANGE' signal is also passed to the Output Control assembly to select the overload sense resistor.

4.12.9.2 Range-Changing Logic

In the 4200, the input to M12-13 is held permanently at logic-Ø. Except during range changes, the $\overline{\text{AC FNCT}}$ and $\overline{\text{I FNCT}}$ signals are always of opposite logic. Although M7a-4 is always at logic-Ø, the logic-1 from M6-11 is sufficient to energize relay RL4. During range changes both function signals are driven to logic-1, momentarily releasing RL4.

4.12.9.3 1kV Enable Logic

With the 1000V range selected, and if the watchdog has not 'barked', M12-3 is at logic-1 and LED D70 is lit. Relay RL6 is energized if the 1kV ENABLE switch on the PA assembly is set to ENABLE.

For other ranges, or if the watchdog barks, RL6 is de-energized, removing the AC drive to the step-up transformers. LED D70 is also de-energized.

4.12.9.4 '400V ENABLE' Logic

The '400V(2) OFF' signal from the CPU is normally at logic-Ø for voltage ranges; but after a 'FAIL 7' message indicates a 400V supply failure, it is toggled three times, attempting to restore the supply.

In normal operation, therefore, with BARK at logic-Ø, the PS1 OFF signal from M11-4 is also at logic-Ø, and is input to M1-1/6 (page 7.9-4). M1 consists of six inverting drivers, each with uncommitted-collector output (as used for the relay drivers). M1-1 at logic-Ø allows M1-2 to be pulled to logic-1 by AN1-1/2, or to logic-Ø by M1-14. In the lower chain with four inversions, M1-14 is also open-collector, if a 400V or 15V failure has not been detected by the monitors.

Thus for normal operation M1-2 is pulled to logic-1 and the 'ENABLE 400V−' line from M1-15 is held at logic-Ø (−15V). With the 'ENABLE 400V+' line it energizes the opto-isolator LEDs in the 400V power supply (PS/I heatsink page 7.13-3).

A failure of either the 400V or 15V supply pulls M1-3 to logic-1, disabling the 400V supply by setting the ENABLE 400V− line to logic-1. If the +15V or −15V rail collapses, the opto-isolator current is cut off in any case, due to zener D24.

4.12.9.5 'BIAS OFF' Logic

On the 100V or 1000V ranges, after receiving a 400V FAIL signal from the monitor, the CPU attempts three times to restore the 400V supply. The foldback current limiting for the supply (in the PS/I heatsink) prevents reinstatement if an overload persists. Thus it is necessary to remove the overload if the supply is to be restored. This is done by setting the BIAS OFF line to logic-Ø (−15V), cutting off Q10 (page 7.9-3) and removing the output drive.

The attempts are made by toggling the 400V (2) OFF line (described in sect 4.12.9.4). Each time the supply is enabled, R6 and C1 hold the BIAS OFF signal at logic-Ø for about 1ms to allow the supply to build up before the load is reapplied.

After three unsuccessful attempts, the CPU assumes a permanent hardware fault and holds the 400V (2) OFF signal at logic-1.

4.12.9.6 '$\overline{\text{LIM ST}}$' Logic

This status signal is passed back to the CPU via the SSDA serial link to indicate that certain limits have been exceeded. The $\overline{\text{LIM ST}}$ signal entering the Reference Divider assembly at J4-76 (page 7.4-6) can be activated to logic-Ø by any one of six detectors, as illustrated in the simplified diagram of Fig. 4.12.1.

The signal output from the Power Amplifier at J9-67 (page 7.9-2) can result from the LIM DET signal setting the latch M5a (page 7.9-5).

LIM DET is set to logic-1 by the 100V Overload Detector (page 7.9-6), if the 400V supply current peaks are excessive. It can also be set by the 1000V Overload Detector or Overvoltage Detector in the Output Control assembly (page 7.5-1/2). The logic-1 is immediately transferred via D38 as 'I LIM 100V AMP' to the gate of Q14 (page 7.9-3). Q14 conduction reduces the 100V amplifier input to zero, so if the overload is external the LIM DET signal should rever to logic-Ø.

The latch M5a is set by logic-1 on pin 6, for as long as LIM DET remains at logic-1. Its 'Q' output reinforces and latches the 'I LIM 100V AMP' signal. Its 'Q' output is the '$\overline{\text{LIM ST}}$' signal, so the CPU is informed. The CPU initiates a series of clock pulses on the 'I LIM RST' line via the SSDA and Reference Divider, so that M5a can be reset as soon as the LIM DET signal clears to logic-Ø, M5a 'D' input being strapped to −15V. The CPU also displays the 'Error OL' message.

If the LIM DET line has cleared to logic-Ø, the 100V Amplifier input is reinstated by M5a being reset. Furthermore, if the overload was temporary, the LIM DET line remains at logic-Ø, and operation returns to normal. The CPU is informed by $\overline{\text{LIM ST}}$ at logic-1, so the reset pulses are discontinued, and the Error message is removed.

For a persistent overload, the detectors operate once again. The cycle repeats until other user action is taken to remove the overload. The Error message continues to be displayed.

If the overload is an internal fault, it is likely that another protection circuit will have detected it and taken its own action.

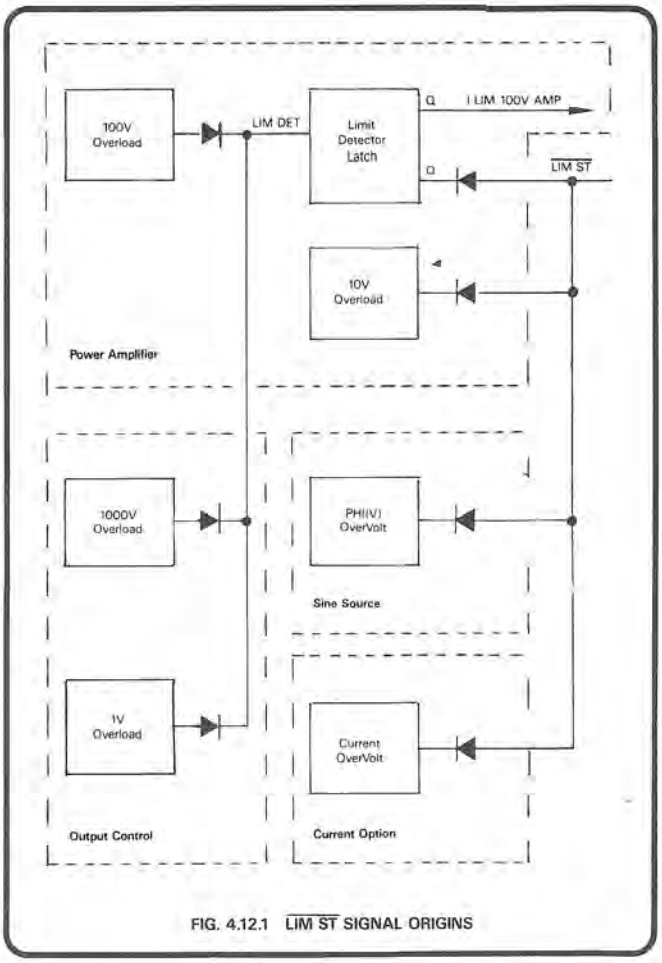


FIG. 4.12.1 $\overline{\text{LIM ST}}$ SIGNAL ORIGINS

4.12.9.7 'LF', '$\overline{\text{LF}}$' and '1kV GAIN'

These are signals used to control the gain and compensation of the 1kV amplifiers (Refer to section 4.12.6).

The 'LF' signal is set to logic-1 by the CPU via the SSDA serial link and Reference Divider latches, when the 1000V range and the 100Hz or 1kHz frequency ranges are selected. It is inverted as 'LF' at M11-12, and subsequently inverted as buffered '$\overline{\text{LF}}$' at M11-10.

'FREQ RØ' is also CPU-controlled. It is set to logic-1 when either the 1kHz or 100kHz frequency range is selected.

'LF' and 'FREQ RØ' are combined at M6-10 to give the '1kV GAIN' signal, which is at logic-Ø only when the 100kHz range is selected. (The software prevents the 1MHz range being selected on the 1000V range).

4.12.9.8 Thermistor Comparator

Two NTC thermistors situated in different positions on each PA heatsink are part of a bridge network which detects excessive temperatures on the heatsinks.
(Section 4.12.4.3 and pages 7.13-1/2 refer.)

The reference arm of the bridge is formed by R169 and AN9-7/10 in parallel, both in series with AN9-6/11.

The sense arm has four parallel sections, each consisting of one section of AN9 in series with one of the NTC thermistors. Four null detectors are used (M22 and M23), each comparing the voltage at the reference arm junction with that at the junction of one of the sections:

TEMP +R
TEMP −R
TEMP +F
TEMP −F

At 25°C each thermistor resistance is 10kohms. The bridge is unbalanced in favour of open-collector outputs from the four comparators, pulled up to Common-2 by R163 and R164. Q36 is therefore cut off, and the 'OVERTEMP' signal at J9-31 is at logic-Ø (−15V).

If one of the chip temperatures exceeds 100°C, its thermistor resistance falls to the extent that the bias on its null detector is reversed. The null detector output is taken low to −15V, Q36 conducts and the OVERTEMP signal goes to logic-1.

The OVERTEMP status signal is passed to one of the Reference Divider status registers, (page 7.4-4), where for safety reasons it is pulled-up by a 1Mohm section of AN2. The CPU reacts to the signal by displaying the 'FAIL 1' message, and forcing a recovery sequence:

OUTPUT OFF;
Reference Divider ramp to zero;
Remote Sense OFF;
Analog Control 'OFF' bit set;
Analog Control '1kV' line disabled;
Display and Keyboard locked;

After approximately 1 minute, the CPU defaults the instrument to the normal 'OUTPUT OFF' state in the selected ranges with output set to zero. The FAIL 1 message is removed, and the user is at liberty to make another attempt.

Under normal power-up conditions, with the Power Amplifier assembly plugged in and Q36 cut off, R167 holds the line more negative than −14V (logic-Ø). If the Power Amplifier is removed, no over-temperature information is available from the heatsinks. In this event, the OVERTEMP signal rises to logic-1, indicating failure.

4.13 HIGH VOLTAGE SENSING

(Circuit Diagram 430447 pages 7.7-1 and 7.7-2)

The SHI (ACV) signal, returned from the terminals via the Current and Output Control assemblies, enters the AC assembly as for the 10V range; but the 1V/10V Sense Amplifier is bypassed for the high voltage ranges.

On these ranges, the signal is switched into one of two guarded attenuators, both housed in the Attenuator/Cage assembly plugged directly into the AC assembly. Each attentuator is a separate resistor chain which acts as the input resistor to the inverting amplifier M32. The output of the amplifier is passed to the Comparator transfer switch.

4.13.1 100V Sense Amplifier

The SHI (ACV) signal passes through the contacts of energized relays RL19 and RL15, and is applied via the four pins of J1 into the 100V attenuator chain. The attenuator consists of four 25kohm 0.1% resistors in series. To guard out stray capacitance, each junction between the resistors is taken to an equivalent voltage point on a chain of four capacitors, C64 to C67. The capacitive chain is also driven from the sense signal.

Relay RL13 is un-energized on this range, so R124 acts alone as the feedback resistor, producing an amplifier gain of 1/100. The sense signals are thus reduced to 1V range levels. The amplifier output is routed through the contacts of unenergized relay RL3 as the comparator 'SIG' input, to transfer switch M16-11 (page 7.7-3).

4.13.2 1000V Sense Amplifier

The SHI (ACV) signal is blocked by the contacts of un-energized relay RL15, but RL16 is energized, applying the '1kV SENSE' signal via link LK1 into the 1000V attenuator chain. The chain has ten 50kohm 1% resistors in series. The guards are taken to equivalent voltage points on a chain of eight capacitors, C70 to C77, again driven from the sense signal.

Relay RL13 is energized on the 1000V range, so R123 and R124 act in parallel as the feedback resistance, giving a gain of 1/550. The sense signals are thus reduced to 1V range levels (the 1000V range FS voltage is 1100V; the equivalent 1V range voltage is 2V). The amplifier output is routed to transfer switch as for the 100V range.

4.14 Sine/Quasi-sine RMS Comparator

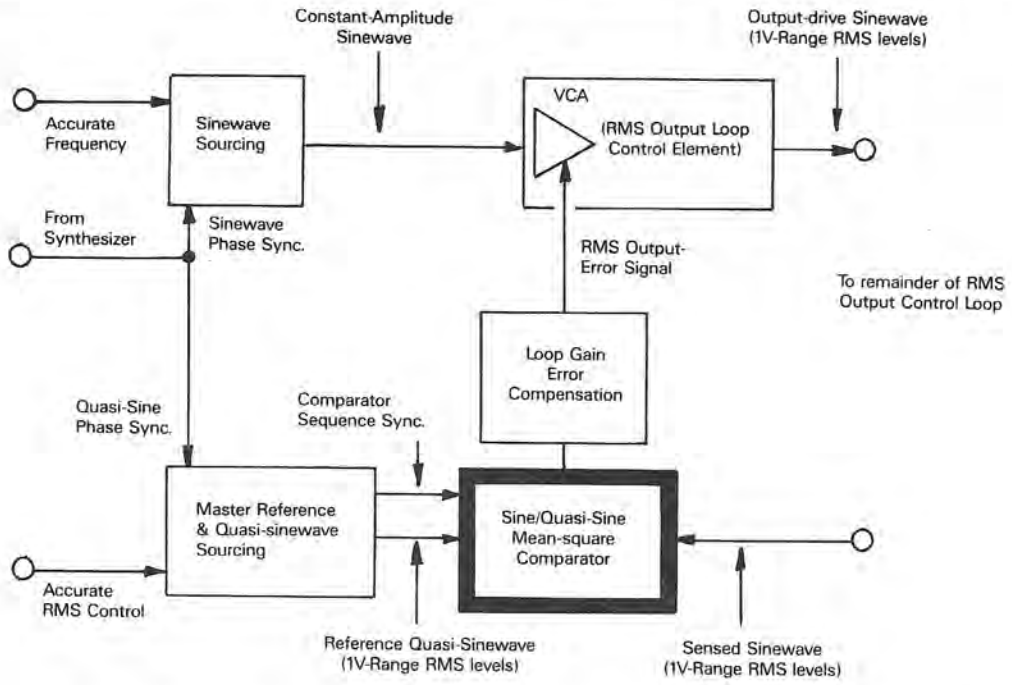


FIG. 4.14.1 THE SINE/QUASI-SINE COMPARATOR AND ITS SYSTEM ENVIRONMENT

4.14.1 Purpose and Environment
(Fig. 4.14.1)

The VCA acts as the control element of the Fine Amplitude Control Loop, having variable gain which is adjusted to change the 4200 output value.

The main purpose of the comparator, in conjunction with the coarse amplitude control, is to cause the 4200 output RMS value to track the value set on the front panel OUTPUT display. It generates a DC error voltage which adjusts the VCA gain.

Because it is part of the fine amplitude control loop, the comparator also corrects output RMS changes due to loading and other disturbances, within the instrument specification.

The Comparator receives two analog inputs:

a. The reference quasi-sinewave whose RMS value is set by the value on the OUTPUT Display, and is also modified by stored calibration data (Refer to section 4.6), and

b. The sensed and conditioned output sinewave (Refer to section 4.12), which is compared against the reference quasi-sinewave.

The Comparator output is the DC error voltage resulting from the difference between the RMS values of the two inputs. As the VCA gain (and hence the output RMS level) is adjusted, the RMS value of the comparator's sense input approaches that of the reference, and the error voltage is driven towards zero. The output value stabilizes when the RMS values of the two inputs are equal.

The buffered DC error signal output from the comparator is adjusted in approx. 1000ppm FS steps by the action of the Coarse Amplitude DAC, to give a virtually constant loop gain. The effects are described in sub-section 4.10.

4.14.2 Implementation

Both inputs are scaled to 1V Range levels and compared in an Integration/Sample-and-Hold system. They are sequentially steered through a common squaring circuit into separate 'REF' (reference^2) and 'SIG' (reference^2 minus sense^2) averaging integrators.

A capacitor and voltage follower samples and holds the settled REF integrator voltage. It generates a DC 'REF^2' signal which is subtracted from the AC 'SIG^2' signal. The result is applied to the SIG integrator, then another sample-and-hold circuit generates the 'AC ERROR' signal from the integrator's output.

'AC ERROR' is thus a DC analog of the difference between the 'mean-square' values of the two inputs. It is buffered and applied to the VCA via the Error Amplifier.

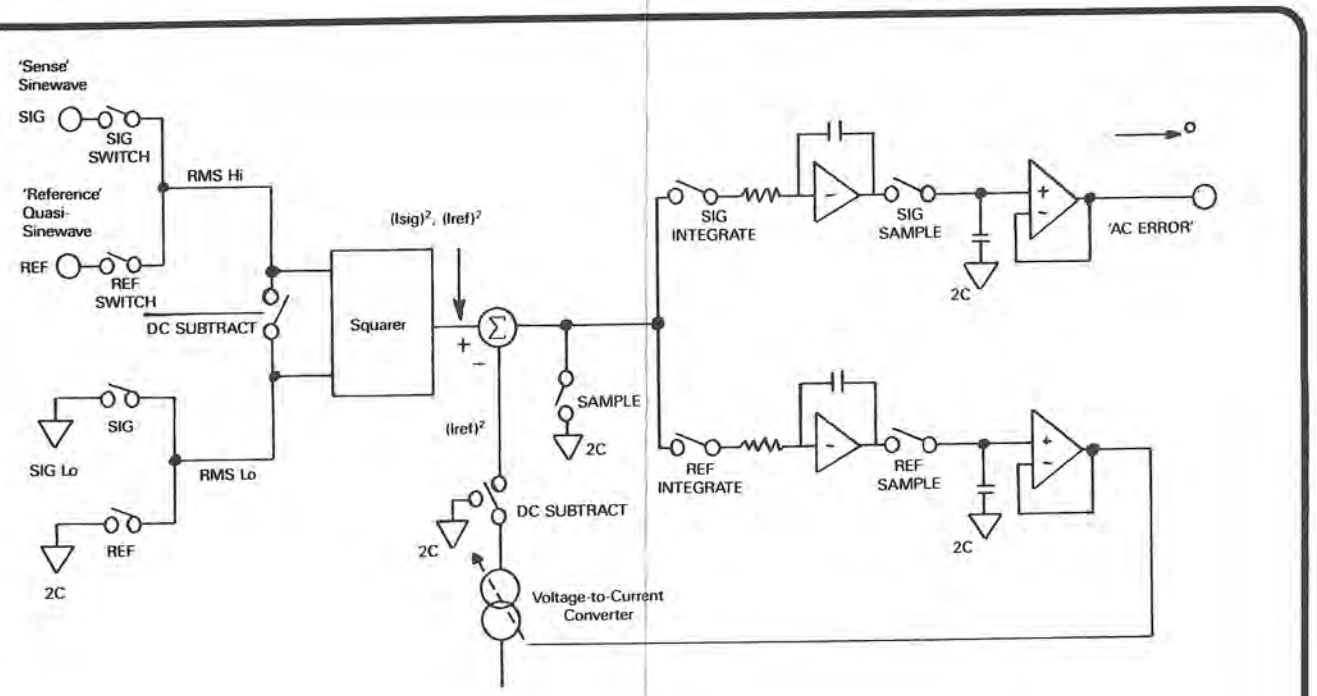


FIG. 4.14.2 SINE/QUASI-SINE COMPARATOR—BLOCK DIAGRAM

'X' indicates that switch is closed.	COMPARATOR CYCLING PERIODS									
	C 1	C 2	C 3	C 4	C 5	C 6	C 7	C 8	C 9	C Ø
States	REFERENCE PATTERN					SENSE (SIG) PATTERN				
(a) Squarer input	← quasi-sine →			zero		← sine →			zero	
(b) REF SWITCH	X	X	X							
(c) REF INTEGRATE	X	X	X	X						
(d) REF SAMPLE					X					
(e) SIG SWITCH						X	X	X		
(f) SIG INTEGRATE						X	X	X	X	
(g) SIG SAMPLE										X
(h) DC SUBTRACT	X	X	X			X	X	X		
(i) $\overline{\text{DC SUBTRACT}}$				X	X				X	X
(k) SAMPLE					X					X
(l) RMS Lo	COMMON-2C					SIG LO				2C

FIG. 4.14.3 SINE/QUASI-SINE COMPARATOR—SEQUENCE CYCLE

4.14.3 Method of Comparison
(Figs. 4.14.2 and 4.14.3)

The comparator is based on a ten-state recycling sequence of squaring, integration, sampling and subtraction. Operation and accuracy rely heavily on synchronization between sinewave and quasi-sinewave.

At relevant points in the following description, reference is made to a specific output frequency of 500Hz (1kHz Range), as an example to clarify the following points:

a. As the output sinewave frequency is varied, the quasi-sinewave tracks an exact sub-multiple of its frequency; except on the 100Hz Range, where both are at the same frequency. In our example at 500Hz, the quasi-sinewave has half the output frequency.

   The various relationships between output and quasi-sinewave frequencies for different frequency ranges are detailed in Section 4.7, Table 4.7.3.

b. The duration of each comparison cycle is always equal to ten quasi-sinewave periods (here 40ms), and each of the 'C' periods persists for one quasi-sinewave period (for 500Hz output – 4ms). This effect can be observed using an oscilloscope, say at TP46.

c. Using this specific case also gives a point of reference for examination of the circuit waveforms using an oscilloscope.

4.14.3.1 The Comparator Sequence
(Figs. 4.14.2 and 4.14.3)

The table in Fig. 4.14.3 shows the conduction patterns of the switches in the block diagram of Fig. 4.14.2, within a complete sequence cycle. The cycle is broadly divided into two similar patterns ('REF' and 'SIG'), each occupying five quasi-sinewave periods. The cycle repeats continuously.

In the following analysis, the effects of the closed switches are described; all other switches are open.

Periods C1, C2 and C3

a. REF SWITCH is closed to input the quasi-sinewave to the squarer.

b. REF INTEGRATE steers the squarer output current into the Reference Integrator.

c. DC SUBTRACT allows Isub to be drawn from the summing junction.

d. RMS Lo has been connected to common 2C since the start of CØ in the previous period, in preparation for REF squaring.

The quasi-sinewave is squared, and the result is output as a current (at twice the input frequency) into the summing junction. The DC current Isub is subtracted at the junction, and the residue goes to charge the Reference Integrator capacitor.

(Note that every time the 4200 OUTPUT OFF is selected, REF and SIG integrator capacitors are discharged, driving both 'AC ERROR' and 'Isub' to zero. During the first REF integration when OUTPUT ON is next selected, Isub remains at zero so the integrator capacitors start charging from zero.)

Period C4

a. REF SWITCH is opened, removing the input to the squarer.

b. DC SUBTRACT is opened, subtraction ceases.

c. $\overline{\text{DC SUBTRACT}}$ closes to input a hard zero to the squarer.

d. REF INTEGRATE remains closed, allowing the squarer and integrator to settle.

e. RMS Lo remains connected to common 2C until the integrator has settled.

The REF integrator remains in its integrating (on) condition during period C4, to ensure that any energy stored in the squarer during C1 and C3 is acquired.

DC subtraction during period C4 would generate an error, as full subtraction was already applied during period C1. DC SUBTRACT is therefore turned off by transferring the source of Isub from the summing junction to Common 2.

Period C5

a. REF INTEGRATE opens, stopping the integrator action.

b. SAMPLE closure forces the squarer output to a hard zero, to nullify any leakage effects in the integrator switch.

c. REF SAMPLE closes to charge the sampling capacitor to the integrator capacitor voltage, by current from the integrator op-amp.

d. RMS Lo is switched from the Ref common 2C to the Sense SIG Lo in preparation for SIG squaring.

As the sampling capacitor changes its charge, its voltage-follower drives the voltage-to-current converter to change the DC subtraction current. During this period the new Isub is sourced from Common 2, but during the next SIG and REF integration periods, it will be subtracted from the squarer output current at the summing junction.

Periods C6 to CØ

As can be seen from Fig. 4.14.3, the closure pattern is repeated for SIG squaring, integration and sampling. The SIG circuit action is identical to REF, except that:

a. the squarer input is now the sensed sinewave;

b. the subtraction current has been set to a new value during period C5. This does not change again until period C5 of the next cycle;

c. During period CØ, the 'AC ERROR' output from the SIG sample-and-hold voltage follower is changed, updating the VCA gain via the error buffer and Error Amplifier.

d. RMS Lo was switched from the common 2C to SIG Lo during period C5 in preparation for SIG squaring. It remains connected to SIG Lo during the squaring periods C6, C7 and C8, and also during period C9 for the Sig integrator settling. At Period CØ it is reconnected to common 2C in preparation for REF squaring.

4.14.3.2 Comparator Action

The sequence described in 4.14.3.1 is necessarily simplified. When a new output demand changes the amplitude of the quasi-sinewave, a few sequence cycles are required to stabilize the conditions of the REF integrator, SIG integrator, subtraction current and AC ERROR OUTPUT. The circuit must also respond to demands for reduced output in addition to those for increases.

The comparator forms part of the output amplitude control loop, ultimately affecting the output voltage and hence the sensed voltage input to the squarer as 'SIG'. As the sequence recycles, the mean-square value of the SIG input sinewave will approach that of the REF quasi-sinewave, and as it does so the AC ERROR output must approach a steady-state value.

The squarer output current has an AC component in its waveform, but Isub being subtracted at the summing junction is a DC current. In the settled condition, Isub is driven on successive cycles to balance the quasi-sinewave REF^2 AC current (being applied to its integrator) about zero. The final level of Isub is just sufficient to be self-sustaining.

Meanwhile, the sensed SIG^2 current approaches the REF^2 value, and the same Isub is a DC analog of the quasi-sinewave mean-square voltage. In the output loop, the VCA is driven until the 4200 output (and sensed SIG input) is at the correct level just to generate a self-sustaining 'AC ERROR'.

In the comparator, Isub is subtracted from both SIG^2 and REF^2 currents. This maintains the AC AMPL ERROR as an analog of the difference between the quasi-sinewave and the output sinewave mean-square voltages (when the latter is reduced by sense conditioning to 1V Range levels). Thus when the sensed SIG input voltage approaches the quasi-sinewave REF voltage (mean-square values), the AC ERROR approaches stability and the system settles.

A further complication: a bias is applied to the squaring circuit to avoid distortion by maintaining permanent conduction. The bias is controlled by the value of the positive reference voltage, and a bias current is superimposed on the subtraction current. These factors will be discussed later during the circuit analysis.

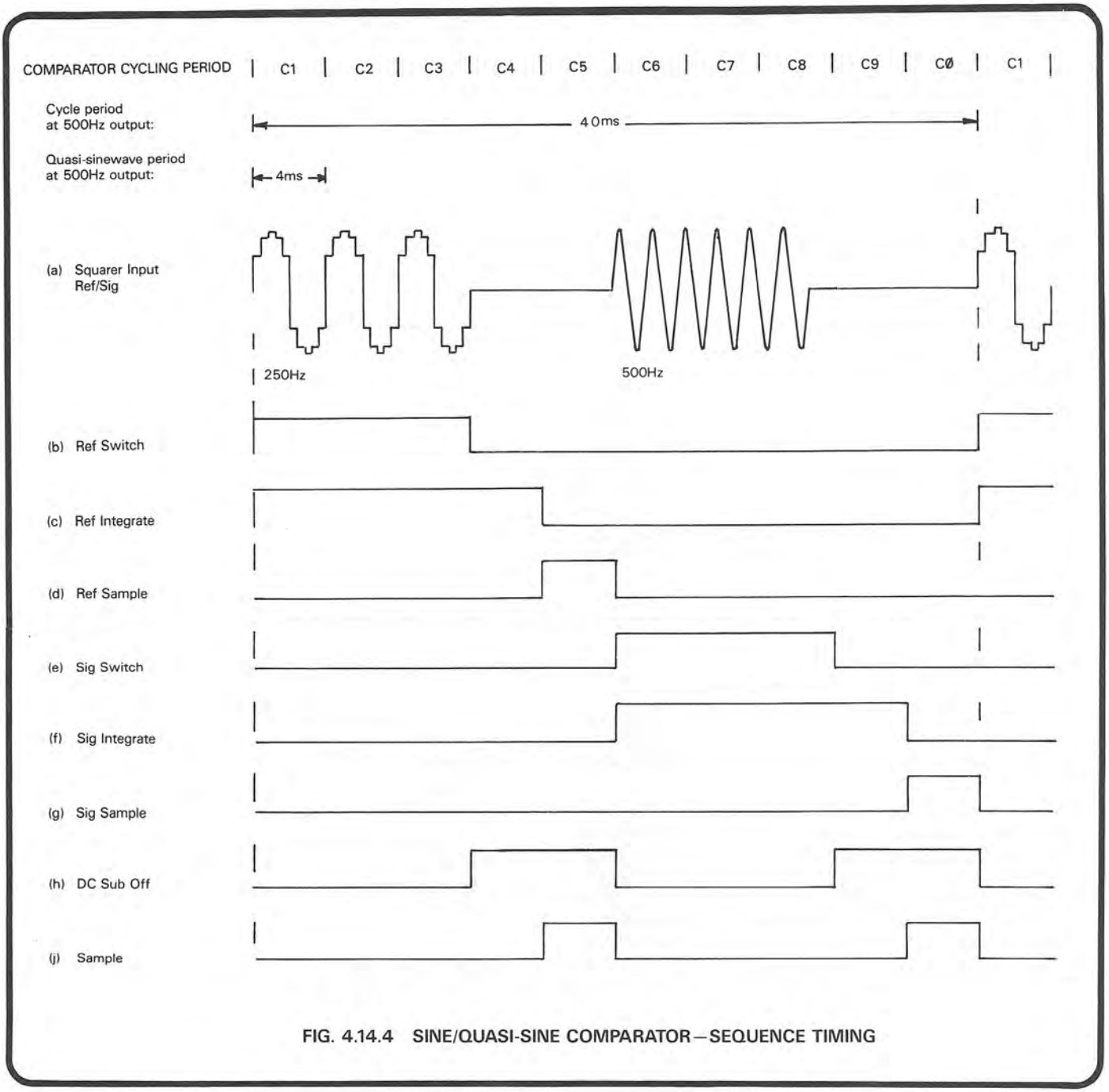


FIG. 4.14.4 SINE/QUASI-SINE COMPARATOR—SEQUENCE TIMING

4.14.4 Comparator Control Logic
(Circuit Diagram 430447 page 7.7-3)

TheComparator operating cycle originates at M15, which is a 10-bit sequencing counter, clocked at the quasi-sinewave frequency by the carry-out from M11-12.

The SYNCØ input to M15 RESET is a decoded address, whose function at logic-1 is to disable counters M11 and M15, inhibiting operation of the comparator and generation of the quasi-sinewave. In the 4200, SYNCØ is held permanently at logic-Ø, enabling both quasi-sinewave and comparator for Voltage and Current functions.

The clock continuously recycles M15 in ascending count through $Q_Ø$ to Q_9, ten clocks (ie ten quasi-sinewave periods) constituting one cycle of the comparator sequence. Only one 'Q' output is at logic-1 (+8V) at a time, the rest being at logic-Ø (−8V).

With increase of frequency range, the difference between the frequencies of sensed sinewave and reference quasi-sinewave increases in decade steps. As the comparison is performed at mean-square levels, this frequency difference does not matter, so long as the sinewave is at an exact multiple of the quasi-sinewave frequency. However, to optimize the operation of the Sense/Reference comparator, the zero crossings of the quasi-sinewave are synchronized to occur coinincident with a sinewave zero crossing, and all comparator state changes are also synchronized to sinewave zero-crossings.

Synchronization is achieved by clocking M17 so that all the analog switching data changes simultaneously. Thus data is latched from M17 'D' inputs to its permanently-enabled outputs, one complete quasi-sinewave period after it was clocked through M15. This ensures that the transit times of M15, M18 and M20 do not affect synchronism with the quasi-sinewave zero-crossing.

The data is thus strobed through M15 and M17, delaying the data by one clock period. This does not affect the operation of the comparator, although it must be accounted for when observing waveforms on an oscilloscope.

The sequence, as described in sub-section 4.14.3, starts with REF SWITCH connecting the quasi-sinewave to the squarer input during period C1. The logical origin of the comparator switch state during C1 corresponds to M15-2 (Q1 output) at logic-1; but because of the data delay its actual timing is coincident with M15-4 (Q2 output) at logic-1.

4.14.5 Comparator Timing Logic
(Fig. 4.14.5)

The comparator timing waveforms for the sequence are shown at Fig. 4.14.5. To illustrate the data delay, the main waveforms are grouped into two blocks: 'REF' and 'SIG', each headed by the states of the comparator cycle. Line (b) shows which of M15 (Q) outputs is at logic-1 during each of the states. It can be seen that the effects of M15 output states are delayed by 1 clock period, in the translation to comparator states.

4.14.5.1 Squarer Commons Switching
['REF' and 'SIG' waveforms (d) and (k)]

Waveform (c) shows the variation of M15-12 (Cout). Waveforms (d) and (k) are the direct results of Cout inputs to M17 after the translation by one clock shift (note the inversion at M20-10).

During the states CØ to C4, waveform (d) at logic-1 connects the squarer common (RMS Lo) to Common-2 at M16-4 for quasi-sinewave squaring; whereas during states C5 to C9, waveform (k) connects RMS to Lo to SIG Lo at M16-8 for sensed sinewave squaring. In both cases, the appropriate common is connected one period ahead of the squarer input, and disconnected at the end of the integrator settling time.

4.14.5.2 Squarer Input Switching
['REF SW' and 'SIG SW' waveforms (e) and (l)]

M15 outputs Q1 to Q3 are 'OR' gated at M18-6 and applied as D2 input to M17. The result is to generate the REF SW waveform (e) at M17-7.

REF SW connects the quasi-sinewave as input to the squarer by M16-13 only during states C1 to C3.

Similarly, SIG SW waveform (l), logically derived from M15 outputs Q6 to Q8, is at logic-1 only during states C6 to C8, connecting the sensed sinewave as input to the squarer by M16-12.

4.14.5.3 Integration and Sample Switching

'INT' and 'SAMPLE' waveforms (f) and (h)

At any instant, the comparator is either sampling or integrating. The INT waveform is thus the inverse of the SAMPLE waveform.

SAMPLE

M15 outputs QØ and Q5 are 'OR' gated at M18-9 and applied as D3 input to M17. The result is to generate the SAMPLE waveform (h) at M17-10.

Therefore, CØ and C5 only, SAMPLE provides two enabling inputs to AND gates M13 at M13-2 and M13-5. It also places a hard zero on the squarer output by M7-5 (page 7.7-4) when this is disconnected from both integrator inputs. With both input and output at zero volts, any offsets are removed in preparation for the subsequent squaring and integration sequence.

INT

The 'SAMPLE' output of M18-9 is inverted at M20-4, applying logic-1 to the D1 input of M17 for the whole of the cycle except for CØ and C5. The INT output at M17-5 is waveform (f), which enables M13-1 and M13-13.

REF INT

INT is 'AND-gated' with REF waveform (d) at M13-11 to generate the 'REF INT' waveform (g), which is at logic-1 only during periods C1 to C4. During this time M7-12 (page 7.7-4) at logic-1 connects the squarer output to the REF Integrator input.

SIG INT

INT is 'AND-gated' with SIG waveform (k) at M13-10 to generate the 'SIG INT' waveform (m), which is at logic-1 only during periods C6 to C9. During this time M7-6 (page 7.7-4) at logic-1 connects the squarer output to the SIG Integrator input.

REF SAM

'SAMPLE' is 'AND-gated' with SIG waveform (k) at M13-4 to generate the 'REF SAM' waveform (j), which is at logic-1 only during state C5. During this time driver M6-1 (page 7.7-4) at logic-1 causes FET Q2 to conduct, connecting the REF Integrator output to the REF Sample-and-Hold input.

SIG SAM

'SAMPLE' is 'AND-gated' with REF waveform (d) at M13-3 to generate the 'SIG SAM' waveform (n), which is at logic-1 only during state CØ. During this time driver M6-7 (page 7.7-4) at logic-1 causes FET Q3 to conduct, connecting the SIG Integrator output to the SIG Sample-and-Hold input.

4.14.5.4 DC Subtraction

'DC SUBTRACT OFF' waveform (p)

Subtraction is required only when either input is being applied to the squarer. As REF SW and SIG SW already exist, it remains only to provide an OR function or join them. The analog circuits need an inverted waveform, so a NAND gate is used. For loading purposes two elements of M20 are connected in parallel: REF SW and SIG SW are combined as waveform (p) at M20-3 and M20-11.

Squarer Input Short

When at logic-1 during C4-C5 and C9-CØ, M7-13 places a hard short between RMS Hi to RMS Lo; otherwise the short is released.

Subtraction Current Control

During C1 to C3 and C6 to C8, DC SUBTRACT OFF at logic-Ø cuts off D8 (page 7.7-4), allowing Q6 to draw subtraction current through D6, D5 and R54. When at logic-1, D8 conducts and sets D5 and D6 in reverse bias, diverting the subtraction current.

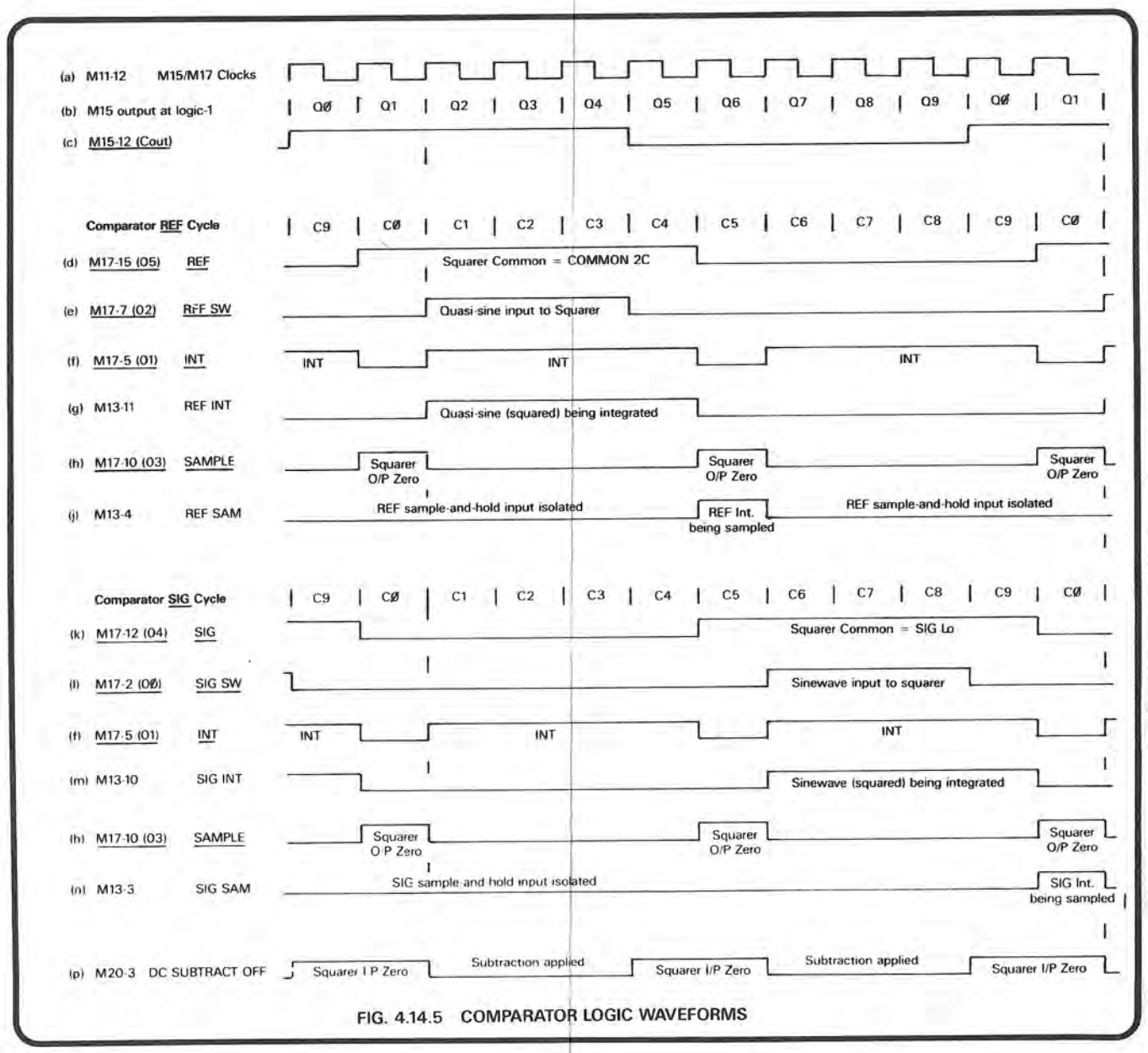


FIG. 4.14.5 COMPARATOR LOGIC WAVEFORMS

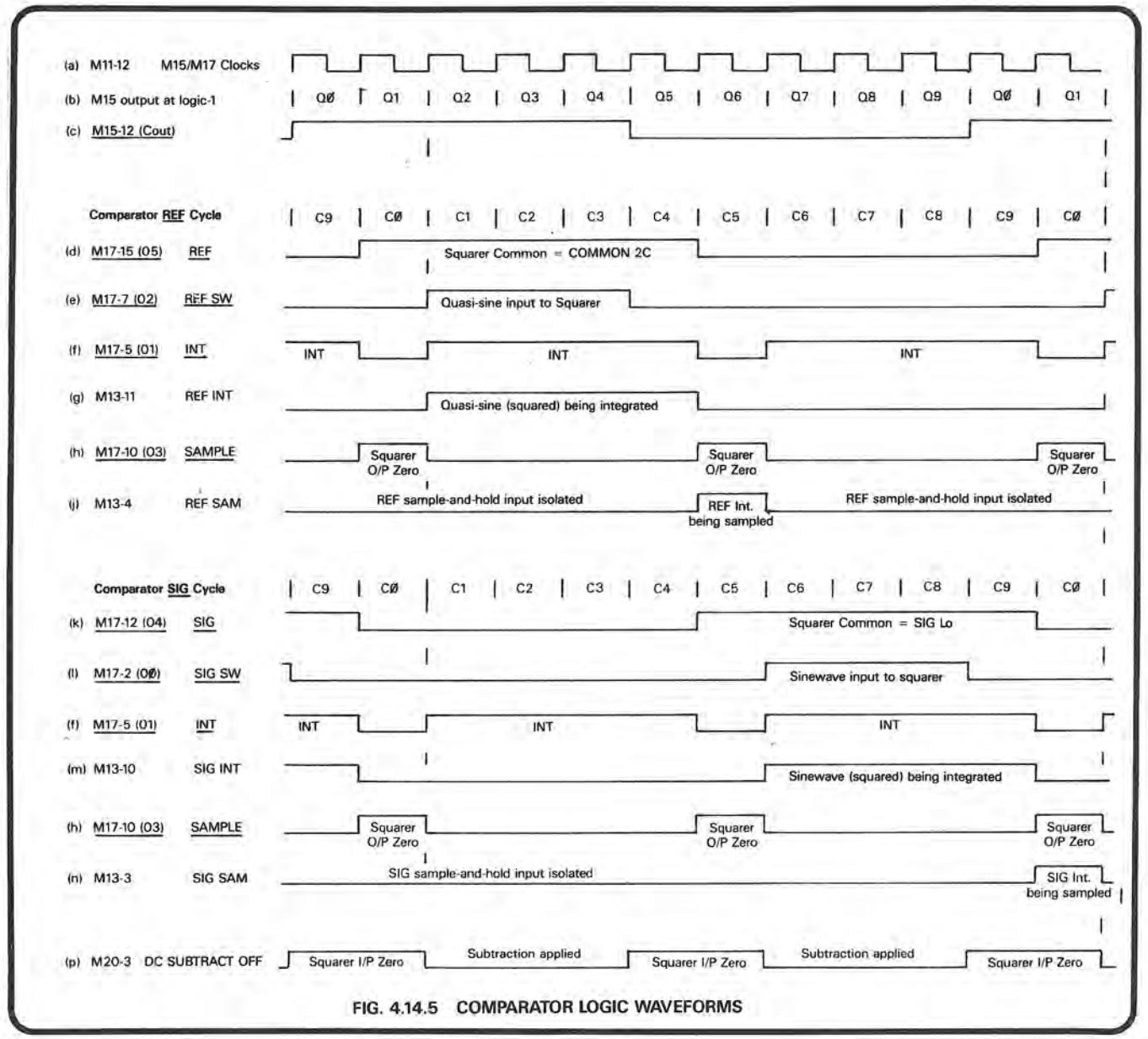


FIG. 4.14.5 COMPARATOR LOGIC WAVEFORMS

4.14.6 Square Law Detector Circuit
(Circuit Diagram 430447 Page 7.7-4)

The basic action of the squaring circuitry is the same as is used for $\sin^2$ and $\cos^2$ in the Sinewave Oscillator amplitude loop, but there are some differences in detail (Refer to Sect. 4.8.8).

The Square Detector is biassed in such a way that it is permanently turned on, to improve bandwidth and permit control of gain scaling. Its differential output current at AN3-3 and AN3-2 is proportional to the square of its input voltage divided by the bias voltage. The bias is derived from the DC version of the demanded signal level REF+ve, the DC output from the Reference Divider.

Thus the transfer proportionality of the signal magnitude is given by:

Vout α $Vin^2/Vbias$

but as Vbias is derived from REF+ve,

Vin/Vbias is a constant: k,

and the instantaneous squarer gain is:

$$\frac{d(Vout)}{d(Vin)} = \frac{d\left[\frac{kVin^2}{Vin}\right]}{d(Vin)} = 2k$$

Thus the basic gain equation has no amplitude or frequency components, so is constant over a wide bandwidth and dynamic range. The squarer therefore has a fast response at all signal levels.

The bias is applied as currents to Q17 and Q18 emitter circuits. The transistors in the array of M22 are all used as current generators.

4.14.6.1 Bias Control

The input to Reference Amplifier M24 is the positive DC REF+ve voltage, which varies between approx. 0.14V and 2.8V, depending on the output value selection.

M24 output voltage rises until M22-9 pulls enough current through R50 to reduce M24-3 to zero. The other transistors in M22 act as current mirrors, so their collector currents are defined by the REF+ve voltage and the resistance of R50.

Thus bias current is applied to Q17 and Q18 in direct proportion to the REF+ve voltage, which is an accurate analog of the demanded output value.

4.14.6.2 Current Driver

The 'SIG^2' and 'REF^2' current outputs from the square detector develop a differential voltage input between TP48 and TP49, to the current driver Q9/Q10/M19. This amplifier generates a single-ended current drive to the integrators.

Q9(B) collector drives the output directly, but in order to establish a stable DC voltage reference level, Q9(A) collector current is mirrored by Q10(B).

M19 bootstrap steers Q9(A) collector current through Q10(A), maintaining Common-2C potential at Q10(A) collector.

Q10(B) mirrors the Q9(A)/Q10(A) collector current so that when the differential input voltage between TP48 and TP49 is zero, Q9(B) collector current is all taken by Q10(B), and the potential at TP9 is the Common-2C zero, at high impedance.

Differential input variations between TP48 and TP49, due to 'SIG^2' and 'REF^2' outputs from the Square Detector are translated to differential currents into and out of the junction at TP9. The current difference passes through R35 and R148 during SIG INT states, and to R149 during REF INT states.

At other times, when the integrator input switches M7-8/9 and M7-11/10 are both open, the 'SAMPLE' waveform closes M7-4/3 to pass any difference current to Common-2C. (During the SAMPLE periods, DC SUBTRACT OFF is zeroing the Square Detector input RMS Hi anyway, by shorting to RMS Lo via M7-2/1.)

Resistors R35, R148 and R149 are of very low value compared with Q9(B) and Q10(B) output impedance, so the driver compliance is high.

4.14.6.3 Output Amplitude Loop —LF Gain Reduction

On the 100Hz Frequency range the gain around the output amplitude loop needs to be less than on other ranges. It is convenient to adjust the error immediately following its generation in the square detector, by shunting the input to the current driver.

Adjustment is in two stages, using dual open-collector comparator M21:

a. **For 100Hz Range selection**
The '100Hz' signal input to M21-3 is derived in the Frequency Synthesizer, and is at logic-1 when the 100Hz Range is selected by the operator. M21-1 is pulled up by R41 and Q7 conducts, connecting R43 and R44 between TP48 and TP49, thus shunting R49 and the base-emitter junctions of Q9. For a given 'SIG^2' or 'REF^2' signal, the input feed to the current driver is reduced.

b. **For frequency selections below 32Hz**
The '>31Hz' signal input to M21 is also generated in the Synthesizer.

i. For any frequency above 31Hz, the >31Hz signal is at logic-1, M21 output is at logic-Ø (−15V) and Q8 does not conduct.

ii. For frequencies of 31Hz and below, the >31Hz signal is at logic-Ø, M21 output is pulled up by R42. Q8 conducts, connecting R45 and R46 between TP48 and TP49, in addition to R43 and R44. For a given 'SIG^2' or 'REF^2' signal, the input feed to the current driver is further reduced.

4.14.7 Generation of the DC Subtraction Current

4.14.7.1 'REF' Integration

The integrator circuit is very basic. Feedback for M12 is by C25, but the input resistance is formed by R149, R35 and the output impedance of the Current Driver, which is heavily predominant. The current from the driver is virtually unaffected by R35 and R149.

M7-11/10 conducts for periods C1 to C4 (REF INT). During C1 to C3 the REF SW waveform inputs the quasi-sinewave to the squarer, and during C4 the squarer settles to its zero input.

The REF^2 output from the driver is an AC current, which for a constant quasi-sinewave amplitude is integrally charge-balanced about zero due to the DC subtraction, at twice the quasi-sinewave frequency. C25 therefore receives equal positive and negative charge during each cycle of quasi-sinewave, so the mean voltage at M12-1 does not change.

A discharge path for C25 is provided by Q5/R30. The 'INT HOLD' signal at J7-46 is at logic-1 when the 4200 is in 'OUTPUT OFF' condition, discharging both REF and SIG integrators. For so long as the 4200 output remains 'ON', the INT HOLD signal remains at logic-Ø, and the integrators are never discharged other than by the action of their inputs.

4.14.7.2 'REF' Sample-and-Hold

Q2 conducts during each 'REF SAM' period, when the charge on C25 has settled for the cycle. M12 drives C12 to the voltage on C25, and the voltage follower M4 passes the same voltage as 'REF ERROR' on to the REF V to I Converter.

Q2, C12 and M4 are low-leakage devices, and M4 input circuit is screened at low impedance to the sampled voltage. Thus the 'Droop' is specified as less than 20 microvolts during the 'Hold' part of the cycle when Q2 is not conducting.

4.14.7.3 REF V to I Converter

The circuit of M19 and Q6 converts the DC voltage output of M4 into the subtraction current. A second function is to draw an extra DC current which compensates for the bias control currents.

The DC 'REF ERROR' voltage from M4-6 is divided by R37/R31 and applied to the non-inverting input of M19. A second input results from the DC bias current drawn by M22-14, defined by the 'REF+ve' voltage and the two resistors AN2-10/7 and R141.

M19 drives FET Q6, which draws current via Q12-3 emitter, R54, D5 and D6. The current is sunk into Common-2C via R47, R38 and AN2-12/5, and into the −15V supply via the M22-14/12 bias circuit.

Capacitor C34 filters out any HF transients remaining from the REF SAMPLE switching edges, and D7 protects against positive excursions of Q6 gate.

In the simplified diagram of Fig. 4.14.2, the subtraction current is shown as being sourced by the summing junction. In reality, it is taken from Q12-3 emitter for three main reasons:

a. The Current Driver input bias is removed, allowing a zero-offset reference.

b. The control bias for the squarer is compensated at the earliest opportuity, reducing the required dynamic range of the driver.

c. Q12 emitter voltage remains virtually constant for all squarer inputs.

Relocating the subtraction point does not affect the essential action of the square detector and driver, because of the current-mirror action of the driver.

Subtraction is valid only during times when a quasi-sinewave or sensed sinewave is being input to the Square Detector. Thus for periods C1 to C3 and C6 to C8, diode D8 is held in reverse bias by the signal 'DC SUBTRACT OFF' at logic-Ø. During periods C4, C5, C9 and CØ, the signal is at logic-1, so D8 conducts and cuts off D5 and D6. The subtraction current passed by Q6 is then diverted through D8 from M20-11/3, the parallel 'DC SUBTRACT OFF' NOR gates' output being at logic-1 (page 7.7-3).

When an operator selects a different output value, the result is a change in amplitude of the quasi-sinewave. This unbalances the integrator input, so C25 charges to a different mean voltage at M12-1. The DC subtraction current change takes place over a few comparator cycles until balance is restored, when C25 and C12 will have charged to a new voltage.

4.14.8 'AC ERROR' Signal Generation

4.14.8.1 Integration and Sampling Circuit

The SIGNAL Integration and Sample-and-Hold circuitry is identical to the REF arrangement described in Section 4.14.7. Moreover, the SIGNAL Integrator M12 is the other half of a matched pair with the REF Integrator.

The difference lies in the timing. Switch M7-6 allows current to pass into the SIG integrator only during the periods C6 to C9, so it is the SIGNAL ($|\text{sensed sinewave}|^2$) current minus the ($|\text{DC REF}|^2$) subtraction current which is integrated.

The integrator voltage is sampled and output as the DC 'AC ERROR' voltage, into the output amplitude control loop (Section 4.9).

4.14.8.2 Output Amplitude Loop Action

Consider the case of 'OUTPUT OFF'

a. The quasi-sinewave has an amplitude determined by the 'OUTPUT' display value:

b. The quasi-sinewave is squared and appears as a current in R35 during periods C1-C4, but because Q5 is conducting, the REF integrator capacitor C25 is discharged. Thus the DC subtraction current is effectively zero (it is actually sufficient to cancel the DC current in R35 due to the squarer bias).

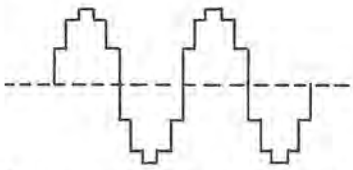
c. The AC ERROR signal voltage is zero, as Q5 conduction prevents any charge on the SIG integrator capacitor C26. Also, the output amplitude is zero, hence the sensed output applied to the squarer is zero.

Therefore during periods C6-C9 the current in R35 is zero.

Now consider the case when OUTPUT is switched ON, with the OUTPUT display set to the minimum value of 9% of range:

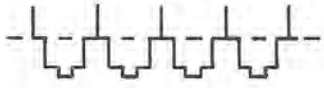
As the quasi-sinewave is already present, it is squared into a negative-going waveform in R35.

Quasi-Sinewave Input



During the first comparator cycle, this appears as a voltage at TP9 thus:

$(\text{Quasi-Sinewave})^2$
Zero Reference



The standing bias on the Ref. V to I Converter has immediately set the $(\text{quasi-sinewave})^2$ to an approximate zero mean.

The $(\text{quasi-sinewave})^2$ current is integrated across C25, resulting in a positive 'REF ERROR' voltage after period C5, and hence a positive subtraction current in R35. The effect of the current can be seen in the TP9 voltage waveform: an increase of $(\text{quasi-sinewve})^2$ amplitude is accompanied by a positive shift as its mean value seeks coincidence with zero.

After a few comparator cycles the current in R35 becomes charge-balanced about zero, the DC subtraction current stabilizing to a steady-state value.

Meanwhile, during the 'SIG' sections of the comparator cycle, the positive subtraction current is integrated across C26. A negative 'AC ERROR' voltage is generated, which increases the 4200 output voltage via the VCA. This increase is detected by the sense feedback circuits. After squaring, the result is an AC current in R35, whose mean level begins to offset the effect of the subtraction current on the SIG integrator.

After a few comparator cycles, the AC SIG^2 mean current and the DC subtraction current are equal and opposite, so the current fed through R35 into the integrator is charge-balanced about zero. The itegrator capacitor C26 is thus being charged and discharged by the same amount during each half-cycle of output (SIG^2 current being at twice the output frequency), and so the AC ERROR voltage stabilizes.

Fig. 4.14.6 illustrates three stages in the process of increasing output from zero; observing the current in R35 (ie. the voltage at TP9), the 'AC ERROR' signal, and the output sinewave. The waveforms are not to scale.

Stage 1. This is the first cycle that the quasi-sinewave starts to charge C25. During period C6 a non-zero subtraction current is applied to the SIG integrator, resulting in a non-zero value of 'AC ERROR', starting at CØ as the integrator voltage is sampled. This causes the 4200 sinewave output to rise from zero.

Stage 2. On the next cycle the subtraction current imposes a positive shift on the R35 waveform during C1-C3 and C6-C8. The squared quasi-sinewave does not change in amplitude, but it is more equally balanced about zero, so the next increase in subtraction current will not be so great.

During C6-C8 the sinewave is being applied to the squarer, so TP9 exhibits its squared waveform shifted positively by the subtraction current. A smaller increase in 'AC ERROR' and output sinewave results, as the AC input to the SIG integrator is more equally balanced about zero.

Stage 3. In this state the loop has stabilized. The squared quasi-sinewave and sensed sinewave are both charge-balanced about zero, the subtraction current and 'AC ERROR' have reached constant values, and the 4200 output is stable.

4.14.8.3 'AC ERROR' V-to-I Converter

(Circuit Diagram 430447 page 7.7-6)

To avoid pick-up during transit, the AC ERROR voltage is converted into a current, for transmission to the Error Amplifier on the Sine-Source Assembly. One half of M3 is used as a unity-gain inverting buffer, and the other as a voltage-to-current converter. The relay RL1 is not fitted, so M3-7 is linked directly to the test switch S1 'NORM' terminal.

At M3-7 the DC 'AC ERROR' voltage is inverted and used to drive the current converter via AN1-3/12. The current in AN1-4/13 is mirrored by the current in AN1-11/6 (AC AMPL ERROR), which is sourced in the Sine-Source Assembly by M41a, the Error Amplifier (Circuit Diagram 430446 page 7.6-3).

As the AC ERROR signal DC voltage is varied by the comparator, the current in M41a input resistance also varies, and is converted into a varying voltage at M41a-1. This voltage is used to control the main voltage-controlled amplifier M48 via Q71.

For further information refer to Section 4.10.

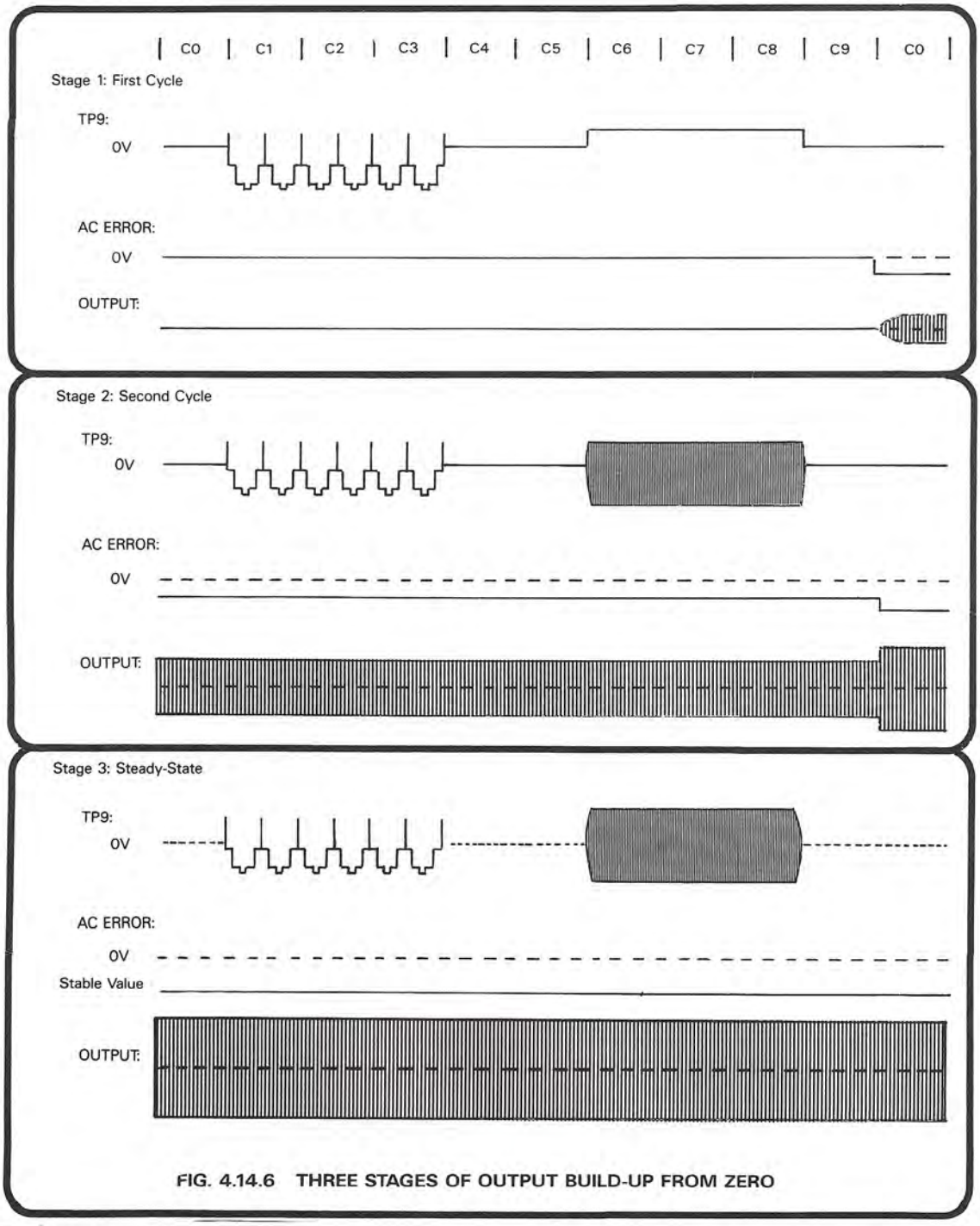


FIG. 4.14.6 THREE STAGES OF OUTPUT BUILD-UP FROM ZERO

The circuits described in this section perform the following functions:

(1) Convert the ACI Reference Voltage into a reference current, having a high-impedance source.
(2) Generate output currents whose value varies directly as the value of the ACI REF voltage.
(3) Provide switching of the AC Current Output and Range, under the control of the Analog Control Interface.
(4) Sense excess output (compliance) voltage, providing a $\overline{\text{LIM ST 1}}$ status signal to the CPU via the Analog Control Interface.

The voltage-to-current converter is located on the Current assembly, providing five ranges of current output. The output is drawn from the 4200 I+ and I− terminals; the Hi and Lo terminals not being used. The five ranges are 1A, 100mA. 10mA, 1mA and 100μA, each extending to 100% overrange.

The output currents are controlled within each range by the value and frequency of the ACI(REF) voltage. This reference voltage is generated by the circuitry used for voltage ranges: the 1V range for the 100μA and 1A ranges; the 10V range for the 1mA, and 100mA ranges. The highest frequency available is 5kHz.

4.15.1 Basic Voltage-to-Current Converter

The basic arrangement is shown in Fig. 4.15.1. A variable AC reference voltage is developed across R1 between the output and the inverting input of the high-gain operational amplifier. The non-inverting input is connected to the output by a resistor network, part or all of wich is current carrying.

With both positive and negative feedback the amplifier forces its differential input to zero. It can only do this by adjusting the current in the current-carrying part of the positive feedback path until the full value of the reference is developed across the path. For example in Fig. 4.15.1 no current flows in R2, so all of VRef is developed across Rs.

The values of VRef and 'shunt' Rs thus determine the value of current flowing in the external circuit. In the 4200 the values of Rs are switched to select the range in use, and VRef is adjusted to vary the output current within the selected range.

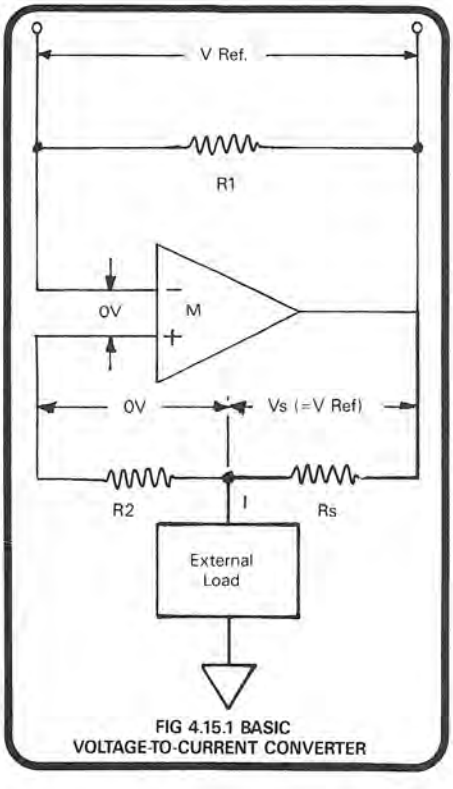


FIG 4.15.1 BASIC VOLTAGE-TO-CURRENT CONVERTER

4.15.2 Two-stage Current Generator

(Circuit Diagrams 430555 Page 7.8-1 and 430540 Page 7.13-3)

Because an 'I−' terminal is necessary to provide a return path for the output current, a 'compliance' signal voltage will be generated at the output terminal 'I+' with respect to I−. The magnitude of the compliance voltage is specified in the User's Handbook. This specification is met by employing a two-stage circuit.

A fixed voltage-to-current conversion stage is followed by a range-switchable current amplifier. The combination is simplified at Fig. 4.15.2.

The AC Reference voltage is applied via two resistors R1 and R3 to both inputs of the first stage. It is arranged for the resistor values to conform to:

$$\frac{R2}{R1} = \frac{R4}{R3},$$

so the output impedance of the stage is virtually infinite, and its output 'floats'.

The second stage is a current amplifier, receiving the output current of the fixed stage to generate a voltage across R5. This voltage is repeated across R6, whose value is range-switched. Any resistor Rs does not affect the output, as it carries no current. Bootstrap supplies are used for the current amplifier, to improve common mode rejection.

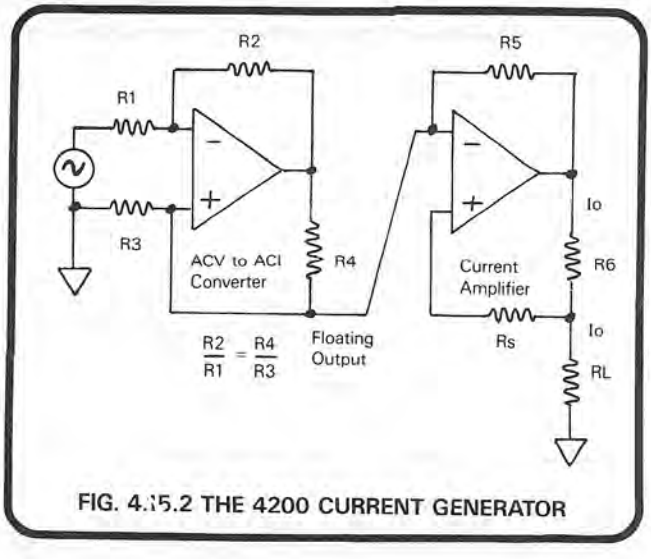


FIG. 4.15.2 THE 4200 CURRENT GENERATOR

4.15.3 Current Reference 'PHI (ACI REF)'

(Circuit Diagram 430447 Page 7.7-1)

On the 100μA and 1A ranges, the 1V range circuitry provides the 2V RMS Full Scale reference voltage; but on the 1mA, 10mA and 100mA ranges the 10V circuitry provides 20V RMS at Full Scale.

On the AC assembly, when the 'I' function is selected, relay RL29 is energized and RL10 is not. The reference voltage for the current generator is derived from PHI (ACV) and PLO (ACV) signals; and sensed at the input to the Current assembly. The sensed ACI REF is returned to the appropriate connections of the 1V/10V Sense Amplifier. The 4-wire connections are made via J7, pins 69 to 71, to the same pins of J8 on the Current assembly.

4.15.4 Range Selection

Fig. 4.15.3 shows two Range configurations of the current amplifier. In each case VRef is 10% of the ACI REF voltage. RL1 is a bistable latching relay, in which solenoid current is required only to change state.

In the 4200, the voltage across the I+ and I− terminals is allowed to rise to 3V RMS with full compliance. Each range incorporates a series resistive element connecting the range selection relay contact to the I+ terminal. These resistors enhance the stability of the circuit, with reactive loads.

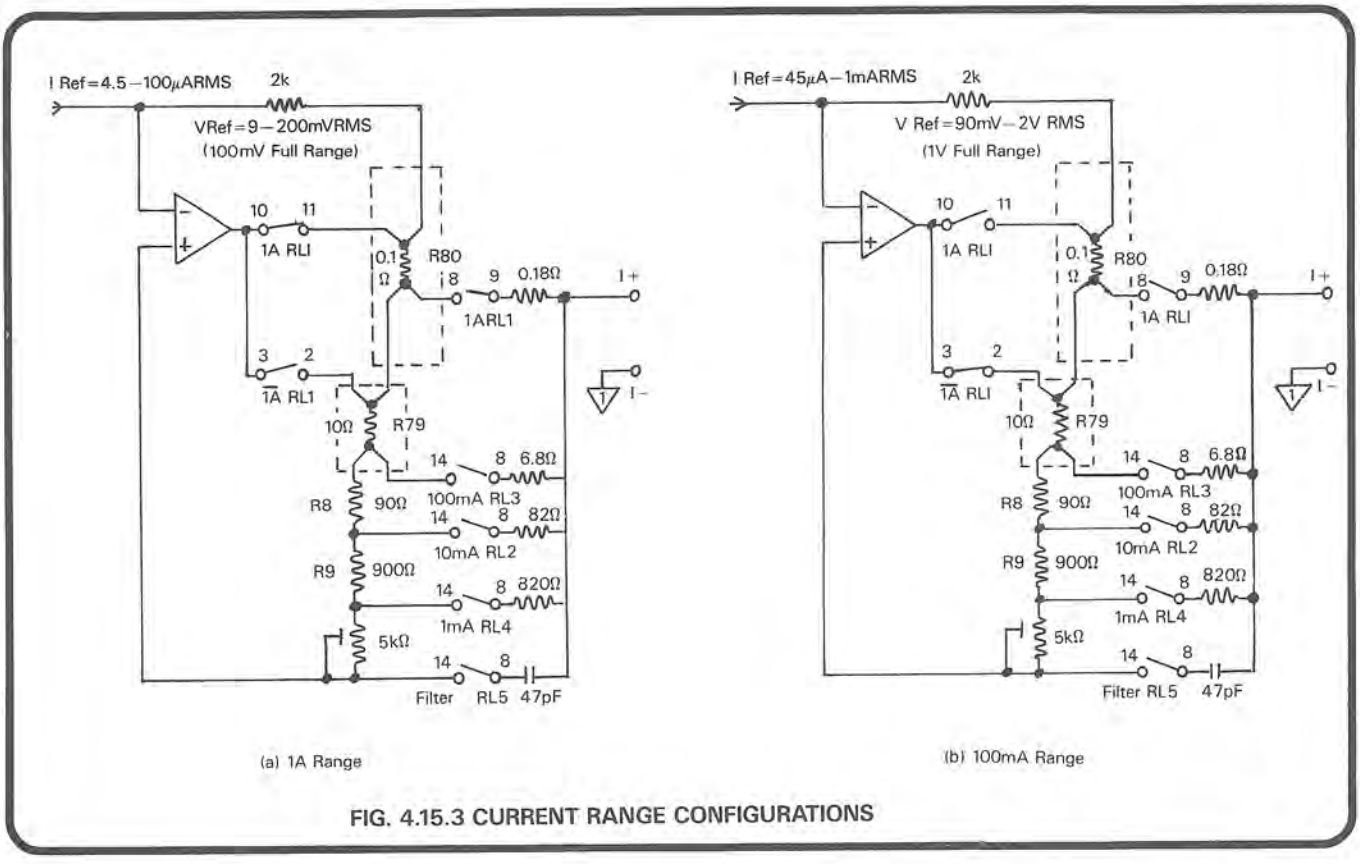


FIG. 4.15.3 CURRENT RANGE CONFIGURATIONS

4.15.4.1 1A Range

(Refer to Fig. 4.15.3a)

Relay RL1 is energized, but RL2, 3, 4, and 5 are not. The only current path available is through the 0.1ohm shunt R80. As VRef is scaled to 100mV RMS Full Range, the full range current in the shunt must be:

$$\frac{100mV}{0.1ohm} = 1A.$$

4.15.4.2 100mA, 10mA, amd 1mA Ranges
(Refer to Fig. 4.15.3b)

Relay RL1 is un-energized, contact RL1-3/2 is closed, contacts RL1-10/11 and 8/9 are open. One relay from RL2, 3 and 4 is energized by range, RL5 is also energized on the 10mA and 100mA ranges for extra HF filtering. All currents now avoid the 0.1ohm shunt, passing instead through the 10ohm shunt R79.

R79 is mounted with R80 on a separate heatsink assembly, plugged into the main Current assembly (refer to the Layout Drawing, page 7.8-1 for alternative versions).

On the 100mA range, VRef is scaled to 1V RMS Full Range, so the full range current flowing through R79 to the I+ terminal via RL3-14/8 must be:

$$\frac{1V}{10ohms} = 100mA.$$

For the 10mA range, R8 (90.00ohms) is included in the current path, so the full range output current is reduced to 10mA. 900ohms (R9) is added on the 1mA range.

4.15.4.3 100μA Range
(Refer to Fig. 4.15.3b)

The hardware is switched as for the 1mA range, but the ACI REF voltage is obtained, as for the 1A range, from the 1V range circuitry. Thus VRef is scaled to 100mA RMS Full Range, and the full range output current is 100μA.

4.15.5 Voltage-to-Current Converter
(Circuit Diagram 430555 Page 7.8-1)

The reference voltage PHI (ACI REF) is applied to the inverting input of M8 via resistor R45A, with R45B as feedback resistor. Similarly R46A and R46B are connected on the non-inverting side. The 18Mohm resistors R82 and R83 shunt R46A to allow compliance adjustment by R51. R86 refers the input to Common-I1, the main 'signal' common.

4.15.5.1 Feed to the Current Amplifier

The output current from the converter, flowing through R46B to restore M8 input virtual-common, passes via R85 into the Current Amplifier feedback resistor R43. It generates a reference voltage between the output of the whole Current Amplifier and its inverting input. This is reflected on its non-inverting side by the current flowing through the range-switched output 'shunts'.

4.15.6 Voltage Preamplifier

M3, M4 and Q6 form a high-gain, chopper-stabilized voltage amplifier. The input offset of Q6 is trimmed by M3, itself a chopper-stabilized amplifier of high gain and approximately 10Hz bandwidth. Q6 provides the bandwidth necessary to pass the signal frequencies and reject common-mode noise.

M4 contributes additional gain and drives the high-current output stage via link TLE. Its load, consisting of R26, R23 and R28 shunted by Q7 in the Heatsink assembly, is supplied with a constant current by Q9, D6 and Q11. Additional frequency compensation is provided by C43 and R81.

The supplies to Q6 and M3 are bootstrapped by M7 for common-mode rejection, also linearizing the preamplifier's dynamic response. Extensive screening and filtering is employed to eliminate the effects of the chopping spikes at the inputs and output of M3.

4.15.7 High Current Output Stage
(Circuit Diagrams 430555 Page 7.8-1 and 430540 Page 7.13-3)

The main current amplifier and temperature-sensing driver load (Q7) are located on the PS/I Heatsink assembly. The quiescent current 'SET IQ' adjustment is situated on the Current assembly.

4.15.7.1 Temperature Compensation

Transistor Q7, in parallel with R26, R23 and R28 on the Current assembly, acts as the load for the preamp. buffer. As the heatsink temperature increases, Q7 conduction increases, reducing the drive to the current amplifier. This compensates for increased intrinsic quiescent current in the two Darlington output devices.

4.15.7.2 Quiescent Current Adjustment

FET Q9 acts as constant 1.4mA ballast for the 3.3V zener diode D6, which sets the voltage across R27 to approx. 2.6V. This establishes a constant current in the buffer load.

The voltage across the load is supplied to the PS/I heatsink as drive for the high-current amplifier. The tapping at J8-110 sets the base conduction level of Q7 on the heatsink, which in turn sets the level of its collector conduction, adjustable by R23. This adjusts the quiescent current in the output devices Q1 and Q2.

4.15.7.3 Current Amplifier

Darlington emitter-followers Q1 and Q2 form the current output amplifier, current-limited by Q5 and Q6. The bias is set to provide some 100mA of quiescent current, which reduces the output resistance of the stage, improving the dynamic response of the output current. This also suppresses any tendency for the drive from the preamp. buffer to fluctuate for output currents around zero; as the drive voltage must slew through approximately 1.3V after switching one device off before the other is switched on.

The current shunts complete the feedback and output circuits as described in paras 4.15.1 and 4.15.4, the output current being fed to the I+ terminal via protection circuitry and output switching.

4.15.8 Output Protection

Diodes D18 and D19 are 5V, 5Watt zeners, placing an absolute limit on the excursions of output voltage. The output compliance specification is valid only up to 3V RMS across the output terminals. Nevertheless, occasions may arise when a user overloads the circuit by attempting to drive current into open circuit (e.g. by disconnecting from a load with OUTPUT ON). In this case D18 and D19 protect any voltage-sensitive load by limiting the output voltage to 5V. But before the voltage reaches this limit, the overload protection circuit generates the $\overline{\text{LIM ST 1}}$ signal.

4.15.8.1 Guard Buffers

M1 guards out the leakage of D18 and D19 in normal operation, and protects against other leakage, by maintaining the output screens and shields around the output circuitry at the output potential.

In addition to its bootstrap function, M7 also acts as a buffer for guards around the amplifier input, thus preventing any common-mode disturbances from affecting the performance of the main amplifier.

4.15.8.2 Overvoltage Detection

The output guard buffer M1 drives the overvoltage detection circuit. M15 divides the output voltage by two and acts as an inverting full-wave rectifier, accommodating both polarities. The full-wave rectified voltage at M15-14 thus increases negatively as the AC output increases, charging C32 to its mean value at M15-10. M15-9 is biassed to −2.2V, so M15-8 reverse biasses D10 unless the terminal voltage exceeds 4.8V RMS, when M15-8 swings the negative rail and pulls the $\overline{\text{LIM ST 1}}$ line to −15V (logic-Ø).

The diode D10 is part of a diode-OR gate, linking $\overline{\text{LIM ST 1}}$ to the $\overline{\text{LIM ST}}$ line, which enters the Reference Divider at J4-76. The CPU receives the $\overline{\text{LIM ST}}$ status signal via the SSDA serial interface, and if at logic-Ø presents the 'Error OL' message on the MODE display. If in the 100mA or 1A range, the 4200 Output is turned off and the DC precision reference is ramped to zero, to limit the power developed as heat within the instrument.

4.15.8.3 Current Switching Logic

(Circuit Diagram 430555 Page 7.8-2)

The analog control signals are transferred into guard on the Reference Divider assembly, and latched as 'Q' output in the Serial/Parrallel Data Converter. Offset positive logic is used:

logic-Ø = −15V, logic-1 = 0V.

The signals enter the Current assembly via J8 from the Mother assembly.

M12 and M14 are Darlington open-collector inverting drivers. The relay drive logic places a logic-1 (0V) on the input of the selected drivers and logic-Ø (−15V) on those not required. A selected driver operates its relay by pulling its output to −14V.

Whenever a switching command has been received, the CPU performs a control-data transfer and the $\overline{\text{UPD (IG)}}$ line from J8-60 is pulsed to logic-Ø for 50ms. Q1 is turned on, applying +15V to the relays connected to its collector. The selected relays are thus energized by 30V, but after the $\overline{\text{UPD(IG)}}$ pulse has ended they are held on by the 13.3V between −0.7V at the cathode of D1 and −14V at the selected driver output. This method reduces the local heat, generated by energized relay solenoids, in the relay contacts.

RL1 is a bistable latching relay with two operating solenoids. A logic-Ø at pin 6 switches the 1A range on, and at pin 1 switches it off. Normally both pins are floating on open collectors, so the relay remains latched on in one bistable state with both solenoids un-energized. During the 50ms $\overline{\text{UPD (IG)}}$ pulse, M16-1 and M16-12 are enabled, allowing the 1A range switching-logic state to change RL1 over (if required), before the $\overline{\text{UPD (IG)}}$ pulse ends.

4.15.8.4 Range Switching

Range control data is input as a 3-bit code on IRØ, IR1 and IR2 lines. The bit-pattern is decoded to '1 of 8' by M6, to energize the correct relays for the selected range. In the 4200, only five of the M6 'Q' outputs are connected (Links LKQ and LKS are broken). The resulting variants are listed in table 4.15.1 against range selections.

4.15.8.5 Current Zero-Output

For zero output, the lines from the current generator to the I+ and I− terminals are disconnected. The 'OFF' signal is set to logic-1, and the $IR_{2-Ø}$ code is '0,0,0'. This sets all M6 outputs to logic-Ø, so RL1 latches in the $\overline{1A}$ position (R79 is selected in preference to R80). Relays RL8 and RL9 are de-energized by the OFF signal, to disconnect the output from the I+ and I− terminals, and short it to the current common-I1.

The Current Range relays RLs 2, 3 and 4, and the filter relay RL5, are all un-energized. While setting OFF to logic-1, the CPU also forces the Precision DC Reference to ramp down to zero, so the ACI REF voltage also falls to zero, and the current generator has no input. Thus the high current amplifier is not trying to produce an output current, and will not be damaged.

4.15.8.6 Function Switching

When the Current function is deselected, this means that the Voltage function is selected. The $\overline{\text{I FNCT}}$ signal is set to logic-1 to energize relay RL23, which connects the voltage output lines to the front panel terminals.

The $IR_{2-\emptyset}$ code is '1,1,1', setting only M6 'Q7' output to logic-1 (pin 4). Thus the range relays RLs 2, 3 and 4 are all un-energized. Relays RL8 and RL9 are un-energized, disconnecting the current output and shorting it to the current common-I1. RL1 is latched in the $\overline{1A}$ position, selecting R79 in preference to R80; and RL5 connects the 10mA/100mA filter.

In the AC assembly (Circuit Diagram 430447 pages 7.7-1 and 7.7-5), the $\overline{\text{I FNCT}}$ signal (J7-86) at logic-1 de-energizes RL9. This disconnects the ACI REF lines (J7-69 to J7-72) from the ACV lines. Thus the voltage to current converter (M8 on the Current assembly) receives no input voltage, and so no current is generated.

4.15.8.7 'BARK DELAYED'

The 'BARK' signal does not affect the Current assembly relays. However, if the Watchdog is activated, all outputs from the Control Data latches in the Reference Divider are 'Tristated' by the 'BARK DELAYED' signal. This allows the pull-up resistors (AN1) and pull-down resistor R84 to become effective. Thus the lowest current range is selected and current output is cut off.

4.15.8.8 $\overline{\text{I ST}}$

The $\overline{\text{I ST}}$ line at J8-98 is pulled down to −15V (logic-Ø) for as long as the Current assembly is fitted in the instrument. This state is passed back via the Reference Divider (J4-68) and the SSDA serial link to the CPU (Circuit Diagram 430535 page 5). Thus the CPU recognizes that option 30 is fitted, and can operate the appropriate programs.

Function	Range	Range Code $IR_{2-\emptyset}$			M6 Output Pins					Signals		Relays Energized						
					Q2	Q3	Q4	Q5	Q7			RL1	RL2	RL3	RL4	RL5	RL8 RL9	RL23
		IR_2	IR_1	$IR_\emptyset$	2	15	1	6	4	OFF	$\overline{\text{I FNCT}}$	6/7 1/12						
ACV/ON	N/A	1	1	1					1		1	*				*		*
ACI/ON	100μA	1	0	1				1				*			*		*	
	1mA	1	0	1				1				*			*		*	
	10mA	1	0	0			1					*	*			*	*	
	100mA	0	1	1		1						*		*		*	*	
	1A	0	1	0	1							*				*	*	
ACI ZERO	Any	0	0	0						1		*						
'BARK DELAYED'	Any	1	0	1				1		1	1	*			*			*

Table 4.15.1 Current Assembly Switching Logic

4.16 POWER SUPPLIES

The circuits described in this section perform the following functions:

(1) Line power switching, fusing, filtering, voltage selection and transformation.

(2) Main digital supply generation and distribution (Outguard)

(3) Display high voltage supply generation.

(4) In-guard stabilized supply generation for Common-2 and Common-4 circuitry.

A simplified power-distribution block diagram appears at Fig. 4.16.1.

The power input module is mounted on the rear panel. The mains (line) transformer is located in the rear section of the instrument, close to the In-guard and Out-guard Power Supply assemblies. (For details of location and attachment, refer to Section 3; and Section 7, page 7.0-1).

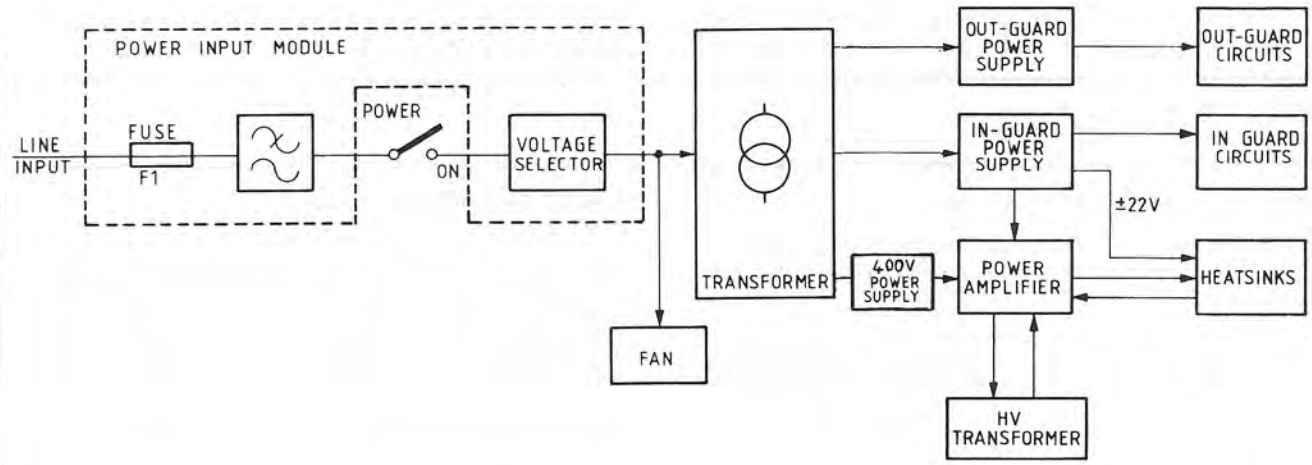


FIG. 4.16.1 POWER DISTRIBUTION BLOCK DIAGRAM

4.16.1 Line Power Distribution (Fig.4.16.1) (Circuit Diagram 430439 Page 7.17-2)

The single phase line supply enters the 4200 via a 3-pole input cable at the rear of the instrument. The cable connector plugs into a power input module which contains a fuse, filter and line voltage selector pcb. (For details of fuse values and operating voltage selection refer to the User's handbook, Section 2).

Both 'line' and 'neutral' rails are filtered by a low-pass LC network before being fed through the instrument to the two-pole 'Power' switch on the front panel.

The switched supply is fed back to the power input module, to the voltage selector pcb, which configures the line transformer primary circuit as determined by the user. Power for the air circulation fan is provided directly from the power input module.

All line transformer secondaries are electrostatically decoupled from the primaries by a ground screen between the windings. The secondaries which supply the Common-2 and Common-4 in-guard circuits are decoupled by an additional screen which is connected to the instrument guard.

4.16.2 Out-Guard Power Supplies
(Circuit Diagram 430561 Page 7.10-1)

4.16.2.1 Digital Main Supply

This circuit provides:

(1) +8V unregulated supply for use in the Front and Digital assemblies.

(2) +5V regulated supply for out-guard digital circuits.

4.16.2.2 +8V Unregulated Supply

This is taken directly from full-wave rectifier D1, D2 via fuse F1 (rated at 4A).

4.16.2.3 +5V Regulated Supply

The output voltage is controlled by series regulator Q5, Q6. Load current is sensed by R1 in the base-emitter circuit of Q1, which increases the conduction of Q5 and Q6 parallel combination for increases of load current. The 2.45V zener D4 provides the reference voltage for comparator M1 at M1-3. The output voltage is sensed between the +5V and DIG common rails on the Mother assembly, and divided down to reference potential at M1-2. R8 and R9 ensure that regulation persists even if the sense links are disconnected.

M1 output drives Q2 whose collector voltage controls Q5 and Q6 conduction. If the +5V rail voltage falls due to loading, Q2 collector voltage rises, increasing Q5 and Q6 conduction to restore the rail voltage. Zener D5 prevents the positive excursion of the +5V rail in the event of regulation breakdown. Zener D3 restricts positive excursions of Q2 base voltage, and hence the drive to Q5 and Q6, to provide current limiting. C9 and C10 give a controlled fast response to reduce the effects of transients on the +5V rail.

PTC thermistor R7 protects the power supply from high ground-leakage currents, notably in the external circuits of the IEEE 488 bus system. R7 presents a minimum of 80ohms between the digital common line and ground; this resistance increasing with increasing current.

4.16.2.4 −180V Display Supply

180 Volts are required to operate the digital plasma displays on the Front assembly. Because the display anode drivers are powered from the Digital Main Supply +5V rail, the 180V positive pole is referred to this rail in the power supply. The display cathode is therefore at a potential of −175V. Refer to Section 4.4 for further details.

Series regulation is provided by D6, R16 and Q3; and shunt regulation by D7 and Q4. A supplementary +5V supply is fed out to the front assembly from J4-21. This is available to power the LEDs in the front panel keys, but is not used on the 4200.

4.16.2.5 Common Mode Null

This circuit provides a line-hum cancelling (bucking) output to the instrument guard network. For adjustment procedure refer to Section 5.8.

4.16.3 In-Guard Power Supplies
(Circuit Diagram 430554 Pages 7.11-1/2)

4.16.3.1 In-Guard Common-2 Supplies

The general ± 15V supply for the analog circuitry is provided by three integrated-circuit regulators (page 7.11-1) as follows:

+15V from M2. Because of the high current taken from this supply, the regulator power dissipation is shared. The rectifier output is first regulated to +18.5V by Q1, Q3 and D9; and then to +15V by M2.

−15V from M1. This is a mirror image of the positive supply.

−10V from M6, derived from the −15V supply.

The supply is protected by 3.15A fuses F3 and F4 at the bridge rectifier output. Chokes L4 and L5 attenuate HF transients on the AC input.

The ±8V supply for the Sine-Source assembly is provided by two integrated-circuit regulators M8 and M9 (page 7.11-2). The supply is protected by 1A fuses F5 and F6 at the bridge rectifier output. Chokes L7 and L9 attenuate HF transients on the AC input.

4.16.3.2 Current Option Supply

This provides +22V and −22V unregulated power outputs to the PS/I Heatsink assembly. Both supplies are protected at 4A by fuses F1 and F2, the AC input being HF-filtered by chokes L2 and L3. The ±22V common return is maintained close to the common-2 return potential by resistor R1.

4.16.3.3 Reference Divider Common-4 Supplies

This circuit provides +36V, +15V and −15V regulated outputs to the Reference Divider in-guard circuits. The +36V supply is also used to power the +20V Master DC Reference.

Two secondary windings of the line transformer are used, and inter-supply transients are reduced by the special coupling arrangements of common-mode choke L10. The rectified output from bridge W4 is series-regulated by M3 to produce the +36V supply. R2/R3 sense the output voltage.

D11 and M4 reduce the +36V to generate the +15V regulated supply.

The −15V supply is provided by bridge W3 and regulator M7.

4.16.3.4 ± 38V Common-2 Supply
(Circuit Diagrams 430532 Page 7.16-5
and 430544 Page 7.12-1)

The ± 38V regulated supply is solely used to power the 10V Amplifier in the Power Amplifier assembly. It is plugged into the Mother assembly in the rear compartment next to the Heatsinks.

The mains (line) transformer 40VRMS secondary centre tap is referred to Common-2 on the Mother assembly. It provides a variable AC output by R25 on the Mother assembly to balance line-induced voltages on the guard screens. The 40V is rectified, filtered and smoothed on the Mother assembly before being passed to the regulator at approximately ± 50V DC.

On the 38V Supply assembly the output voltage is controlled by series regulators Q2 and Q1. As the regulator is symmetrical, only the positive side is described.

The output voltage is divided by R26 and R25 to provide a sense signal for comparator M1, which is powered by a local shunt regulator D8/R16/C8. The 2.45V reference for the comparator is derived by D6/R23 from the comparator supply.

M1 output drives Q8 whose collector voltage controls Q6 and hence Q2 conduction. If the +38V rail voltage falls due to loading, Q8 collector voltage rises, increasing Q5 and Q6 conduction to restore the rail voltage.

Load current is sensed by R24 in the base-emitter circuit of Q5, which is normally cut off unless the load current exceeds 170mA. At this point Q5 conducts and pulls down the base of Q6, setting a hard current limit.

Zener diode D2 turns Q5 hard on in the event of an output short circuit, providing a rapid response to catastrophic failure in the 10V power amplifier circuitry. As the output voltage falls below +22V, D2 arrests the fall on Q5 base, switching Q5 hard on and tuning Q6 and Q2 off. This leaves D2, R8 and R9 controlling the output current, which falls to less than 500μA.

When the load is removed, the conduction of Q5 via R26/R25 is insufficient to hold Q6 cut off, especially as Q8 is also cut off by the comparator. So Q2 is allowed to conduct, the output voltage rises until first D2, and then Q5, cut off and the output voltage is restored to comparator control.

The ± 38V output is taken through wired-in fuses F1 and F2. These merely protect the PCB tracking in the event of an output short-circuit. The output voltages are protected from reverse polarity by D1 and D2 on the Mother assembly.

4.16.3.5 ± 38V Supply Failure
(Circuit Diagram 430450 Page 7.9-4)

The ± 38V output voltage is monitored in the Power Amplifier assembly. For a description of the monitor refer to Section 4.12, para 4.12.8.

4. 16. 3. 6. ± 400v Common -2 Supply
Refer to section 12, para 4. 12. 7. 2.

SECTION 5

SERVICING AND INTERNAL ADJUSTMENTS

5.1 INTRODUCTION

This section provides procedures for maintenance operations which require removal of covers or partial dismantling. The operations fall into three categories, as described in Table 5.1 below.

Category A Routine Servicing	Servicing Required	Time Interval	Procedure Section 5	Calibration Required	Calibration Procedure
	Clean the Air Intake Filter	1 year (or less in adverse conditions)	5.2	No	—
	Change the Lithium Battery (non-volatile calibration memory)	5 years	5.3	(a) Full pre-cal THEN (b) Full routine recalibration	Section 1.4 Section 1.2
Category B	Internal calibration adjustments	—	—	NONE REQUIRED	

Category C	PCB Assembly	Adjustments	Procedure Section 5	Calibration required	
				Pre-cal (Sect.1.4)	Routine (Section 1.2)
Adjustment following replacement of PCBs (see notes opposite).	Terminal	Capacitive Load Test	5.5	—	Full
	Digital	—	—	Full	Full
	Reference Divider	—	—	Full	Full
	Output Control	Capacitive Load Test	5.5	—	Full
	Sine Source	—	—	—	Full
	AC	Capacitive Load Test Sense Amp zeros	5.5 5.9	— —	Full
	Current	Quiescent Current Compliance	5.6 5.7	— —	All I ranges
	Power Amp	± 120V	5.4	—	—
	Mother	Common-mode null	5.8	—	—
	Out-guard PSU	Common-mode null	5.8	—	—
	Heatsinks +ve & −ve PSU & I	± 120V Quiescent Current	5.4 5.6	— —	— All I ranges
	Transformer HF or LF Mains (Line)	— Common-mode null	— 5.8	— —	1kV Range —

TABLE 5.1 CATEGORIES OF SERVICING AND INTERNAL ADJUSTMENTS

WARNING

HAZARDOUS ELECTRICAL POTENTIALS ARE EXPOSED WHEN THE INSTRUMENT COVERS ARE REMOVED.

ELECTRIC SHOCK CAN KILL!

CAUTION

After any maintenance operations which include removal of top or bottom ground assembly, carry out the Full Self-Test sequence (Section 2.3) before returning to normal use.

CAUTION

The instrument warranty can be invalidated if damage is caused by unauthorised repairs or modifications. Check the warranty detailed in the "Terms and Conditions of Sale". It appears on the invoice for your instrument.

5.1.1 GENERAL

(a) Set Power OFF before attempting to dismantle the instrument (for dismantling and reassembly instructions consult Section 3).

(b) After servicing ensure that all connections have been made (Section 3, Fig.3.6) and that Top and Bottom shields and covers have been replaced. Leave assembled instrument powered-up for at least 1 hour before carrying out any adjustment.

(c) Although replacement assemblies are set up by the manufacturer, the internal adjustments recommended in Table 5.1 must be carried out to ensure correct operation. These adjustments need to be carried out when the assembly is in the user's instrument, in order to account for interaction between assemblies.

WARNING

HAZARDOUS ELECTRICAL POTENTIALS ARE EXPOSED WHEN THE INSTRUMENT COVERS ARE REMOVED.

ELECTRIC SHOCK CAN KILL!

CAUTION

After any maintenance operations which include removal of top or bottom ground assembly, carry out the Full Self-Test sequence (Section 2.3) before returning to normal use.

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(c) Although replacement assemblies are set up by the manufacturer, the internal adjustments recommended in Table 5.1 must be carried out to ensure correct operation. These adjustments need to be carried out when the assembly is in the user's instrument, in order to account for interaction between assemblies.

5.2 CLEANING THE AIR INTAKE FILTER
DATRON PART NO. 450277-1
(REFER TO SECTION 3.14, FIG.3.8)

5.2.1 Servicing Frequency

The filter should be cleaned at intervals no greater than one year. In dusty conditions the frequency should be increased.

5.2.2 Removal (Fig.3.8)

(a) Remove the four M3 x 10mm pozi-countersunk screws (11) which retain the filter grille (12).

(b) Remove the filter grille and reticulated foam filter.

5.2.3 Cleaning

(a) Wash the foam filter in a dilute solution of household detergent (hand hot). Rinse thoroughly in clean hand-hot water and dry completely, without using excessive heat.

(b) Clean the grille, and the grille holes in the rear panel (Use a vacuum cleaner and soft brush on the rear panel).

5.2.4 Inspection

Examine the foam filter for wear, replacing if links are broken.

5.2.5 Reassembly

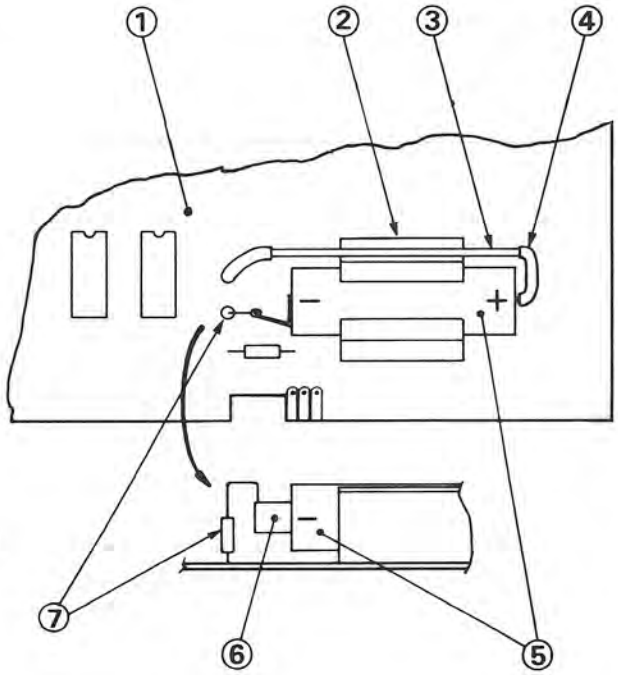
Place the filter in the grille housing and secure the grille to the rear panel using the screws removed in 5.2.2 above.

5.3 LITHIUM BATTERY

(DATRON PART No.920101)

This procedure is to be performed at invervals of 5 years from new.

CAUTION The **full** Pre-cal and Routine Recalibration Procedures (Section 1.4 and 1.2) **must** follow the fitting of a new battery, before the instrument specification can be realized, as calibration data will be corrupted. It is therefore recommended that the battery be replaced immediately prior to a scheduled full recalibration.



1. DIGITAL PCB ASSEMBLY
2. BATTERY CLIP
3. RED WIRE
4. SLEEVE
5. BATTERY
6. NEGATIVE BATTERY TERMINAL WRAPPED AROUND WIRE FROM RESISTOR R60
7. RESISTOR R60

FIG. 5.1 DIGITAL PCB BATTERY REPLACEMENT

5.3.1 Procedure

(a) Ensure that power OFF is selected.

(b) Remove the top cover and top ground/guard assembly
(Section 3 paras. 3.2.1 and 3.4.1).

(c) Remove the digital pcb assembly from the chassis
(Section 3 para. 3.6.1).

CAUTION Do not place the digital pcb on any conducting surface. Do not touch the gold edge connector.

(d) Remove battery as follows (Refer to Fig.5.1).

(1) Push sleeve (4) back along the red wire to expose the solder joint.

(2) Unsolder the red wire (3) from the positive terminal of the battery.

(3) Unsolder the negative terminal of the battery (5) from resistor R60 at the wrap-joint.

(4) Remove battery (5) from battery clip (2).

(e) Fit a new battery, reversing the procedure of step (d).

(f) Refit the digital pcb assembly into the chassis (Section 3 para. 3.6.2).

(g) Refit the top ground/guard assembly into the chassis
(Section 3 para. 3.4.2).

(h) Refit the top cover
(Section 3 para. 3.2.2).

NB The top cover will need to be removed again for precalibration.

5.3.2 Return to Use

Carry out full Pre-calibration then full Routine Calibration in accordance with Section 1.4 and 1.2 respectively.

5.4 ± 120 VOLTS

Adjustment of the 100V/1kV amplifier bias voltages must be carried out after fitting a replacement Power amplifier assembly or Heatsink assembly. The following procedure ensures the drain voltages of Q4 and Q2 are +120V and −120V respectively.

USE EXTREME CARE THROUGHOUT THE FOLLOWING PROCEDURES.

5.4.1 Test Equipment Required

Digital voltmeter
(Datron Instruments model 1071)

5.4.2 Initial Conditions

Remove Top cover.
Remove Top ground/Guard assembly.
Ensure 38V/400V selector is set to 400V.

5.4.3 Procedure

(a) Set 4200 Output OFF.

(b) Connect DVM in DC function, between Lo (⏚2C near Q20) to Hi Q4 drain (Tab).

(c) Adjust R10 for a reading of +120V (±0.5V).

(d) Carefully move DVM high probe to Q2 drain (Tab).

(e) Check reading is −120V (±5V).

(f) Power OFF, disconnect DVM.

5.4.4 Return to Use

Refit Top ground/guard shield and Top cover.

5.5 CAPACITIVE LOAD TEST

(Refer to Layout Drawing 480550)

The 1kv current overload detector, on the Output Control assembly, monitors output current.

After replacing the Output Control assembly, the Terminal assembly, AC assembly or the HF transformers it is necessary to ensure the limit level is set to account for capacitance changes.

The initial value of resistor R33 for the following procedure is 2k ohms. This value is deliberately chosen to give an ERROR OL display with the capacitive load conditions in step (d). If display at step (c) is also ERROR OL then slightly increase value of R33 and restart procedure.

5.5.1 Test Equipment Required

(1) Capacitive Load (150pF ± 3pf, capable of withstanding 2kV).

(2) Digital Voltmeter fitted with AC (Datron Instruments 1071).

5.5.2 Initial Conditions

Top cover removed.
Remove Top ground/guard assembly.
Ensure 38V/400V power supply selector set to 400V.

5.5.3 Procedure

WARNING **THE PROCEDURES INVOLVE THE MEASUREMENT OF LETHAL VOLTAGES. USE EXTREME CARE TO AVOID ELECTRIC SHOCK.**

(a) On the DVM select ACV 1kV range and connect between 4200 Hi and Lo terminals with no load connected.

(b) Select 1kV range on the 4200 and adjust OUTPUT ↑/↓ keys for 750V on the OUTPUT display. Set the frequency to 10kHz and select OUTPUT ON. Adjust OUTPUT ↑/↓ keys for a DVM reading of 750V ± 1V.

(c) Note OUTPUT display reading. Set OUTPUT OFF and disconnect the DVM. Connect the Capacitive Load between the Hi and Lo terminals.

(d) Select 100kHz, OUTPUT ON. Check Mode display for the presence of the ERROR OL message.

(e) On 4200 Select OUTPUT OFF, Power OFF (DO NOT TOUCH RESISTOR R33 WITH POWER ON)

(f) Increase the value of resistor R33 on the Output Control board. Set Power ON and re-establish OUTPUT display reading.

(g) Repeat (d) to (f) until the 4200 will just drive the Capacitive Load at 100kHz, at the output voltage noted in (c), without producing the ERROR OL message.

(h) Finally increase R33 value by the smallest available increment and refit the Output Control assembly in the instrument.

5.5.4 Return to Use

Refit Top ground/guard shield and Top cover.

5.6 CURRENT PCB—QUIESCENT CURRENT ADJUSTMENT

To allow a measurement of quiscent current in the power amplifier stage, its power supply lines are broken and a 0.1ohm resistor inserted in series with each 22V supply line.

The voltage developed across either of these resistors gives a current measurement. The quiescent current is set by adjustment of R23 on the Current assembly.

5.6.1 Test Equipment Required

(1) Digital Voltmeter
(Datron Instruments model 1071)

(2) Two 2.5 watt resistors, 0.10 Ohms, ± 10%, Wire Wound (Welwyn W21 or equivalent)

5.6.2 Initial Conditions

Top cover removed.
Top ground/guard assembly removed.

5.6.3 Procedure

(Refer to Layout Drawing No.480555 and Circuit Diagram No.430555 Page 7.8-1)

(a) Switch the 4200 Power OFF.

(b) Break the 22V supply connections to the Voltage-to-Current converter power stage by removing connector J1 from the In-guard power supply pcb.

(c) Re-make each 22V supply connection from its female pin on the freed J1 connector to its corresponding male pin on the In-guard P.S pcb, using one 0.1 Ohm resistor in series with each supply line (Red and Brown wires).

(d) Connect the digital voltmeter across one of the 0.1 Ohm resistors fitted in (c).

(e) Switch 4200 Power ON.

(f) Ensure 10V range selected with Output OFF.

CAUTION In the following step (g), use a thin insulated screwdriver.

(g) Carefully adjust R23 on I pcb assembly for a digital voltmeter reading of 10mV ±0.5mV (equivalent to 100mA through a 0.1 Ohm resistor).

(h) Switch 4200 Power OFF.

(i) Disconnect and remove both 0.1 Ohm resistors and the digital voltmeter from J1. Reconnect J1 to the In-guard Power Supply pcb pins.

5.6.4 Return to Use

Refit top ground/guard assembly and Top cover.

5.7 COMPLIANCE ADJUSTMENT

Ensure that the Quiescent Current Adjustment Procedure has been completed (Section 5.6).

In the following procedure a DVM is used to measure output current as a voltage developed across a load resistor. Series resistance is then added to one of the power leads to establish a compliance voltage. The change in current output due to compliance is measured and an adjustment made to bring the instrument within manufacturer's specification.

5.7.1 Test Equipment Required

(1) Digital Multimeter fitted with AC (Datron Instruments model 1081).

(2) Test leads, (each containing a 22.1 ohm resistor).

(3) One 2.5 watt load resistor of 0.10 Ohms, ± 10%, Wire Wound. (Welwyn W21 or equivalent).

(4) A 1.4 Ohm resistor to introduce compliance voltage.

5.7.2 Initial Conditions

Remove Top cover.
Remove Top ground/guard assembly.

5.7.3 Procedure

(Refer to Layout Drawing 480555 Page 7.8-1)

(a) Connect the 0.1 Ohm load resistor between the 4200 current output terminals (I+ /I−).

(b) **LF Adjustment**

Select ACI, 1A full range output at 500Hz. Select OUTPUT ON.

(c) With the DVM, measure the AC voltage across the load and note the reading. Set OUTPUT OFF.

(d) Introduce the 1.4 Ohm compliance resistor in series with the I+ lead. Set OUTPUT ON. Use the DVM to measure the AC voltage across the load and note the reading.

(e) Remove compliance resistor. If there is a change of reading $\geq 5\mu V$ between (c) and (d) adjust R31 to reduce the reading to $< 5\mu V$. After any adjustment of R31 repeat (c) to (e).

(f) **HF Adjustment**

Complete above procedure, leaving the 4200 as selected (ACI, 1A Full Range), but change frequency to 5kHz.

(g) Set OUTPUT ON. With the DVM measure the AC voltage across the load and note the reading.

(h) Introduce the compliance resistor in series with the I+ lead. Use the DVM to measure AC voltage across load and note reading.

(i) If change of reading in (g) and (h) is $\geq 10\mu V$ adjust R10. If any adjustment is made then remove compliance resistor and repeat (g) to (i).

(j) If an adjustment was made at (i) repeat complete procedure from (b) until no further adjustments are required.

(k) Output OFF, disconnect load resistor.

5.7.4 Return to Use

Replace Top ground/guard assembly and Top cover.

5.8 COMMON MODE NULL ADJUSTMENTS

The procedure ensures that after replacement of Outguard Power Supply, Mains transformer or Mother Assembly, any power supply noise breakthrough on the Lo or Guard terminals is adjusted to a minimum. Resistor R12 on the Outguard Power Supply Assembly (accessible through a hole in the Top earth shield) is adjusted to minimize the voltage between Lo and Ground. R25 on the Mother Assembly (accessible through a hole in the Bottom ground shield) is adjusted to minimize noise between Guard and Ground.

5.8.1 Test Equipment Required

Oscilloscope
(with AC input and sensitivity to 100mV/div).

5.8.2 Initial Conditions

Remove Top and Bottom covers.
Ensure all guard/earth screws are correctly tightened.

5.8.3 Procedure

(a) Set 4200 to AC 10V range with Output OFF.

(b) Ensure that the OUTPUT display is 0.000,00 V with local guard selected.

(c) Connect the oscilloscope AC input between 4200 ⏚ (Ground) and Lo Terminals.

(d) Locate R12 on the Outguard Power Supply pcb through the hole in the Top ground/guard assembly (refer to Layout Drawing No.480561 Page 7.10-1).

(e) Select OUTPUT ON and adjust the oscilloscope controls to obtain the noise waveform.

(f) Without touching the Top ground/guard assembly, adjust R12 for minimum waveform amplitude. This should not exceed 1V peak-to-peak.

(g) Select Remote Guard, transfer the oscilloscope AC input connection from Lo to the Guard terminal, and obtain a noise waveform.

(h) Locate R25 on the Mother pcb assembly through the hole in the Bottom ground/guard assembly (refer to Layout Drawing No.480532 Page 7.16-5).

(i) Without touching the Bottom ground assembly, adjust R25 for minimum waveform amplitude.

(j) Select OUTPUT OFF. Disconnect the oscilloscope.

5.8.4 Return to Use

(a) Refit Top cover.

(b) Refit Bottom cover.

5.9 SENSE AMPLIFIER ZEROS

The sense amplifier, located on the AC assembly, is provided with access holes located in the Top ground/guard shield. In the following procedure the reading and adjustment steps are always taken with the 4200 OUTPUT ON and at one-tenth of the selected Full Range value.

5.9.1 Test Equipment Required

Digital voltmeter
(Datron Instruments model 1071).

5.9.2 Initial Conditions

Remove Top cover only.

5.9.3 Procedure

(a) Connect the DVM Hi to TP5 on the AC Assembly. Connect its Lo to the 4200 Lo terminal. On the DVM select the 10V range with filter in.

(b) On the 4200 select the 100V range and set the frequency to 1kHz. Select OUTPUT ON and adjust R122 on the AC assembly for a DVM reading of less than 200μV.

(c) On the 4200 select the 10V range, OUTPUT ON.

(d) Note the DVM reading.

(e) On the 4200 select the 1V range, OUTPUT ON.

(f) Note the DVM reading.

(g) Adjust R107 on the AC assembly to set both (d) and (f) readings to less than 200μV.

(h) If R107 has been adjusted then repeat procedure from step (a) ensuring that the difference between all ranges is less than 400μV when taking polarity into account.

(i) Disconnect the DVM.

5.9.4 Return to Use

Refit Top cover.

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