

DATRON
4708

CALIBRATION &
SERVICING
HANDBOOK

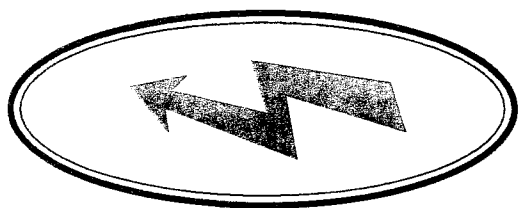
VOLUMES 1 & 2



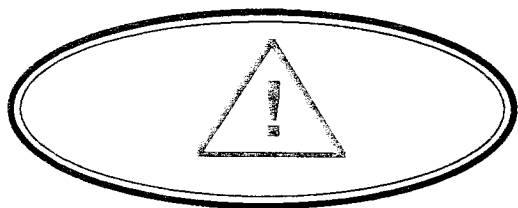
DANGER
HIGH VOLTAGE



**THIS INSTRUMENT IS CAPABLE
OF DELIVERING
A LETHAL ELECTRIC SHOCK !
when connected to a high voltage source**



FRONT or REAR terminals
carry the Full Input Voltage
THIS CAN KILL !



Guard terminal is sensitive to
over-voltage
**It can damage your
instrument !**

Unless **you** are **sure** that it is **safe** to do so,
DO NOT TOUCH
the **I+ I- Hi or Lo leads and terminals**

DANGER

CONTENTS

| | |
|---|-------------------|
| Servicing Diagrams and Component Lists | Refer to Volume 2 |
| General Description, Installation, Controls, Connections and Operation; | Refer to |
| Applications, Specification and Specification Verification | User's Handbook |

PART 1 CALIBRATION AND SERVICING INFORMATION

| Section | Title | Page |
|-------------|---|------|
| 1 | CALIBRATION | |
| 1.1 | Guide to Routine Calibration | 1-1 |
| 1.2 | DC Calibration: | |
| 1.2.1 | Zeros | 1-5 |
| 1.2.2 | Voltage | 1-9 |
| 1.2.3 | Current | 1-14 |
| 1.3 | AC Calibration: | |
| 1.3.1 | Introduction | 1-16 |
| 1.3.2 | Voltage | 1-18 |
| 1.3.3 | Current | 1-26 |
| 1.4 | Resistance Calibration | 1-28 |
| 1.5 | Remote Calibration Guidelines | 1-31 |
| 1.6 | Pre-Calibration: | |
| 1.6.1 | Introduction | 1-33 |
| 1.6.2 | Procedure | 1-34 |
| 1.6.3 | Remote Pre-Calibration Guidelines | 1-37 |
| 1.7 | Ohms Option Internal Adjustment | 1-38 |
| Appendices: | | |
| 1 | Notes on the Use of the Null Detector | 1-A1 |
| 2 | Calibration Source Zero Offsets | 1-A2 |
| 2 | FAULT DIAGNOSIS | |
| 2.1 | Introduction | 2-1 |
| 2.2 | Diagnostic Guides | 2-2 |
| 2.2.1 | FAIL 1 (Excessive internal Temperature) | 2-2 |
| 2.2.2 | FAIL 2 (Over-Voltage) | 2-2 |
| 2.2.3 | FAIL 3 (Control Data Corrupted) | 2-3 |
| 2.2.4 | FAIL 4 (Precision Divider Fault) | 2-3 |
| 2.2.5 | FAIL 5 (Safety Circuits 'Watchdog' Tripped) | 2-4 |
| 2.2.6 | FAIL 6 (Calibration Memory Fault) | 2-5 |
| 2.2.7 | FAIL 7 (P. A. 400V Power Failure) | 2-5 |
| 2.2.8 | FAIL 8 (P. A. 38V Power Failure) | 2-6 |
| 2.2.9 | FAIL 9 (P. A. 15V Power Failure) | 2-6 |
| 2.2.10 | Error EF (External Frequency selected but not detected) | 2-7 |
| 2.2.11 | Error OL (Output Limits exceeded) | 2-8 |
| 2.3 | Self-Test Sequence | 2-9 |
| 2.4 | Fuse Protection | 2-11 |
| 3 | DISMANTLING AND REASSEMBLY | |
| 3.1 | General Precautions | 3-1 |
| 3.2 | General Mechanical Layout | 3-1 |
| 3.3 | Location and Access | 3-2 |
| 3.4 | General Access | 3-3 |
| 3.5 | Removal and Fitting | 3-5 |
| 4 | SERVICING AND INTERNAL ADJUSTMENTS | |
| 4.1 | Introduction | 4-1 |
| 4.2 | Cleaning the Air Intake Filter | 4-3 |
| 4.3 | Lithium Battery - Replacement | 4-4 |
| 4.4 | Standard Resistor Adjustment - Current/Ohms Assembly | 4-6 |
| 4.5 | Bias Current Adjustment - 100V PA | 4-7 |
| 4.6 | Capacitive Load Test | 4-8 |
| 4.7 | Quiescent Current Adjustment - Current/Ohms Assembly | 4-9 |
| 4.8 | Compliance Adjustment | 4-10 |
| 4.9 | Common Mode Null Adjustments | 4-11 |
| 4.10 | Sense Amplifier Zeros | 4-12 |

PART 2 TECHNICAL DESCRIPTIONS

| Section | Title | Page |
|-----------|---|------|
| 5 | PRINCIPLES OF OPERATION | |
| 5.1 | Block Diagrams | 5-1 |
| 5.2 | Inputs | 5-1 |
| 5.3 | Digital Outputs | 5-1 |
| 5.4 | Precision Reference | 5-2 |
| 5.5 | Analog Control | 5-3 |
| 5.6 | DC Voltage Outputs | 5-3 |
| 5.7 | AC Voltage Outputs | 5-3 |
| 5.8 | 1000V Ranges | 5-5 |
| 5.9 | DC/AC Current Outputs; Resistance Outputs | 5-5 |
| 5.10 | Datron 'Autocal' | 5-5 |
| 6 | DIGITAL CIRCUITS; REFERENCE CIRCUITS; POWER SUPPLIES | |
| 6.1 | Digital | 6-1 |
| 6.2 | Keyboard | 6-11 |
| 6.3 | Digital Displays | 6-15 |
| 6.4 | Analog Control Interface | 6-22 |
| 6.5 | Precision Divider | 6-30 |
| 6.6 | AC Reference - the Quasi-Sinewave | 6-43 |
| 6.7 | Power Supplies | 6-47 |
| 7 | DC VOLTAGE OUTPUTS - AMPLITUDE CONTROL SYSTEM | |
| 7.1 | Introduction | 7-1 |
| 7.2 | Low Voltage Loops | 7-2 |
| 7.3 | DC 1V Loop | 7-3 |
| 7.4 | 100mV Range | 7-6 |
| 7.5 | 100 μ V - 10mV Ranges | 7-7 |
| 7.6 | DC 10V Loop | 7-7 |
| 7.7 | DC High Voltage Loops | 7-9 |
| 7.8 | 100V Range | 7-10 |
| 7.9 | 1000V Range | 7-15 |
| 7.10 | Logic Control of DC Outputs | 7-20 |
| 7.11 | DC Assembly Relay Drives and Logic | 7-21 |
| 7.12 | PA Assembly Logic and Relay Drives | 7-24 |
| 8 | AC VOLTAGE OUTPUTS - FREQUENCY CONTROL SYSTEM | |
| 8.1 | Digital Frequency Synthesizer | 8-1 |
| 8.2 | Quadrature Sinewave Oscillator | 8-9 |
| 8.3 | External Frequency Lock | 8-17 |
| 9 | AC VOLTAGE OUTPUTS - AMPLITUDE CONTROL SYSTEM | |
| 9.1 | Introduction | 9-1 |
| 9.2 | AC Voltage Amplitude Control System - Block Diagram | 9-2 |
| 9.3 | Voltage Controlled Amplifiers | 9-3 |
| 9.4 | AC Low Voltage Loop | 9-7 |
| 9.5 | AC High Voltage Loops | 9-12 |
| 9.6 | AC 100V Range | 9-13 |
| 9.7 | AC 1000V Range | 9-15 |
| 9.8 | AC High Voltage Sensing | 9-18 |
| 9.9 | Sine/Quasi-Sine RMS Comparator | 9-19 |
| 9.10 | Logic Control of AC Outputs | 9-30 |
| 10 | CURRENT OUTPUTS AND RESISTANCE | |
| 10.1 | DC and AC Current | 10-1 |
| 10.2 | Resistance | 10-5 |
| 10.3 | Function Switching | 10-6 |
| 10.4 | Current/Ohms Assembly Analog Control | 10-7 |

ILLUSTRATIONS

PART 1 CALIBRATION AND SERVICING INFORMATION

| Title | Page |
|---|------|
| 1 CALIBRATION | |
| Calibration Mode Keys | 1-3 |
| DC Calibration: | |
| Zeros: | |
| ±0 Alignment Check..... | 1-6 |
| ±0 Realignment..... | 1-7 |
| Range Zero Connections..... | 1-8 |
| Voltage: | |
| Low Voltage Connection..... | 1-10 |
| High Voltage Connection | 1-12 |
| Current: | |
| 100µA to 1A..... | 1-15 |
| AC Calibration: | |
| Mid-frequency Exclusions | 1-16 |
| Voltage (1V to 1000V): | |
| Connections | 1-18 |
| 2-wire Compensation Connections | 1-20 |
| Millivolts: | |
| LF Connections | 1-21 |
| HF Connections | 1-22 |
| Current: | |
| Connections for Thermal Transfer, Current Shunts and DC Current Standard | 1-26 |
| Alternative Method using Verified 4707, Calibrated Standard AC Shunts and AC DVM..... | 1-27 |
| Resistance Calibration: | |
| 4-wire | 1-29 |
| 2-wire | 1-30 |
| Remote Calibration Guidelines: | |
| Transfer of Calibration Facilities | 1-31 |
| Pre-Calibration: | |
| Identification of Access Holes | 1-33 |
| Procedure: | |
| DC Connections..... | 1-34 |
| AC Connections (LF)..... | 1-35 |
| AC Connections (HF)..... | 1-36 |
| Pre-Cal Disable..... | 1-36 |
| Remote Pre-Calibration Guidelines: | |
| Transfer of DC Pre-Calibration Facilities | 1-37 |
| Transfer of AC Pre-Calibration Facilities | 1-37 |
| 2 FAULT DIAGNOSIS | |
| Self Test Sequence: | |
| Stage 1 | 2-9 |
| Stage 2 | 2-10 |
| 3 DISMANTLING AND REASSEMBLY | |
| HF Transformer Assembly: | |
| HF Transformer | 3-10 |
| LF Transformer Assembly: | |
| LF Transformer | 3-11 |
| 4 SERVICING AND INTERNAL ADJUSTMENTS | |
| Battery Replacement | 4-5 |

PART 2 TECHNICAL DESCRIPTIONS

| Section | Figure | Title | Page |
|---------|---|--|------|
| 5 | 5.1 | 4708 Simplified Block Diagram | 5-0 |
| | 5.2 | 4708 Block Diagram - Digital, Control and References | 5-7 |
| | 5.3 | 4708 Block Diagram - DC Operation | 5-9 |
| | 5.4 | 4708 Block Diagram - AC Operation | 5-11 |
| 6 | 6.1 | Digital Function Block Diagram | 6-2 |
| | 6.2 | Software Overview | 6-4 |
| | 6.3 | Master Clock Waveforms | 6-8 |
| | 6.4 | Clock Shaping Circuit | 6-9 |
| | 6.5 | Clock Shaping Waveforms | 6-9 |
| | 6.6 | M6 Interface (P8279) - Simplified Schematic | 6-11 |
| | 6.7 | Action of Buzzer Control Latch | 6-13 |
| | 6.8 | Mode and Output Displays - Functional Block Diagram | 6-14 |
| | 6.9 | RAM Access - Write Mode Logic | 6-16 |
| | 6.10 | Read Mode Logic - RAM Access and Segment Switching | 6-17 |
| | 6.11 | Display Scan Sequences | 6-17 |
| | 6.12 | Display Timing Waveforms | 6-19 |
| | 6.13 | Comma Logic - Timing Waveforms | 6-20 |
| | 6.14 | Serial Data Link - Simplified Functional Block Diagram | 6-22 |
| | 6.15 | Serial Data Transfer Organization | 6-23 |
| | 6.16 | SSDA Clock Generator Waveforms | 6-25 |
| | 6.17 | WATCHDOG Circuitry - Simplified Block Diagram | 6-29 |
| | 6.18 | Precision Divider Out-Guard Circuitry - Simplified Block Diagram | 6-30 |
| | 6.19 | Precision Divider In-Guard Circuitry - Simplified Block Diagram | 6-30 |
| | 6.20 | 13-Bit Counter Waveforms | 6-32 |
| 6.21 | BUSY Waveforms | 6-33 | |
| 6.22 | MSB Sync Logic Waveforms | 6-34 | |
| 6.23 | MSB Set/Reset Pulse Generation | 6-35 | |
| 6.24 | LSB Set/Reset Pulse Generation | 6-36 | |
| 6.26 | Action of LSD Switch | 6-38 | |
| 6.27 | Action of Main and Guard Switches (MSD) | 6-40 | |
| 6.28 | Quasi-Sinewave Generation | 6-45 | |
| 6.29 | Power Distribution Simplified Block Diagram | 6-47 | |
| 7 | 7.1 | Low Voltage DC Operation - Simplified Functional Diagram | 7-2 |
| | 7.2 | DC High Voltage Loop - Simplified Block Diagram and Routing | 7-9 |
| | 7.3 | Action of Constant-Current Source | 7-18 |
| | 7.4 | UPD(IG) Signal Distribution | 7-21 |
| | 7.5 | Typical Clamped Buffer | 7-22 |
| | | Circuit Diagram 430668.....DC Clamp Circuit | 7-23 |
| | 7.6 | Limit Status Signal Origins | 7-26 |
| 8 | 8.1 | Frequency Synthesizer Block Diagram | 8-1 |
| | 8.2 | VCO Block Diagram | 8-2 |
| | 8.3 | Frequency Dividers Block Diagram | 8-4 |
| | 8.4 | The Quadrature Sinewave Oscillator and its System Environment | 8-9 |
| | 8.5 | Basic Quadrature Sinewave Oscillator | 8-10 |
| | 8.6 | Gain and Phase Response of Practical Circuit | 8-10 |
| | 8.7 | Corrected Quadrature Oscillator | 8-11 |
| | 8.8 | Fine Frequency Control | 8-12 |
| | 8.9 | Summing $A^2\sin^2\omega t$ with $A^2\cos^2\omega t$ | 8-14 |
| | 8-10 | External Frequency Lock - Block Diagram | 8-17 |
| | 8-11 | 1MHz/10MHz detector Waveforms | 8-18 |
| 9 | 9.1 | Output Amplitude Control System | 9-1 |
| | 9.2 | VCA - Block Diagram | 9-3 |
| | 9.3 | 1V Buffer - Output Stage | 9-4 |
| | 9.4 | Simplified Diagram of Tracking Analog-to-Digital Converter | 9-5 |
| | 9.5 | A-D Tracking - R/2R Network | 9-5 |
| | 9.6 | Window Comparator Action | 9-6 |
| | 9.7 | Low Voltage Loop - Simplified Block Diagram and Routing | 9-7 |
| | 9.8 | Millivolt Attenuators | 9-10 |
| | 9.9 | The Sine/Quasi-Sine RMS Comparator and its System Environment | 9-19 |
| | 9.10 | Sine/Quasi-Sine RMS Comparator - Block Diagram | 9-20 |
| | 9.11 | Sine/Quasi-Sine RMS Comparator - Sequence Cycle | 9-20 |
| | 9.12 | Sine/Quasi-Sine RMS Comparator - Sequence Timing | 9-22 |
| | 9.13 | Comparator Timing Logic | 9-25 |
| | 9.14 | Three Stages of Output Build-up from Zero | 9-29 |
| 10 | 10.1 | Basic Voltage-to-Current Converter | 10-1 |
| | 10.2 | AC Current Generation | 10-1 |
| | 10.3 | Current Range Configurations | 10-3 |
| | 10.4 | Routing of Functions on Current/Ohms Assembly | 10-6 |
| | 10.5 | Typical Clamped Buffer | 10-8 |
| | Circuit Diagram 430669.....Current/Ohms Clamp Circuit | 10-9 | |

CONTENTS

| | |
|-------|-----|
| | 1 |
| | 2 |
| | 3 |
| | 4 |
| | 5 |
| | 6 |
| | 7 |
| | 8 |
| | 9 |
| | 10 |
| | 11 |
| | 12 |
| | 13 |
| | 14 |
| | 15 |
| | 16 |
| | 17 |
| | 18 |
| | 19 |
| | 20 |
| | 21 |
| | 22 |
| | 23 |
| | 24 |
| | 25 |
| | 26 |
| | 27 |
| | 28 |
| | 29 |
| | 30 |
| | 31 |
| | 32 |
| | 33 |
| | 34 |
| | 35 |
| | 36 |
| | 37 |
| | 38 |
| | 39 |
| | 40 |
| | 41 |
| | 42 |
| | 43 |
| | 44 |
| | 45 |
| | 46 |
| | 47 |
| | 48 |
| | 49 |
| | 50 |
| | 51 |
| | 52 |
| | 53 |
| | 54 |
| | 55 |
| | 56 |
| | 57 |
| | 58 |
| | 59 |
| | 60 |
| | 61 |
| | 62 |
| | 63 |
| | 64 |
| | 65 |
| | 66 |
| | 67 |
| | 68 |
| | 69 |
| | 70 |
| | 71 |
| | 72 |
| | 73 |
| | 74 |
| | 75 |
| | 76 |
| | 77 |
| | 78 |
| | 79 |
| | 80 |
| | 81 |
| | 82 |
| | 83 |
| | 84 |
| | 85 |
| | 86 |
| | 87 |
| | 88 |
| | 89 |
| | 90 |
| | 91 |
| | 92 |
| | 93 |
| | 94 |
| | 95 |
| | 96 |
| | 97 |
| | 98 |
| | 99 |
| | 100 |

PART 1

CALIBRATION AND SERVICING INFORMATION

- SECTION 1 Calibration.**
- SECTION 2 Fault Diagnosis**
- SECTION 3 Dismantling and Reassembly.**
- SECTION 4 Servicing and Internal Adjustments.**

SECTION 1 CALIBRATION

(User's are recommended to have first completed the Verification procedures in Section 7 of the User's Handbook.)

1.1 GUIDE TO ROUTINE CALIBRATION

Circumstances Calling For Subsequent Recalibration

SCHEDULED RECALIBRATION

Routine calibration is carried out from the front panel, avoiding thermal disturbance and allowing immediate return to use. The 4708 is fully calibrated before leaving the factory. The specifications for the 4708 are based on standard intervals of up to 24 hours, 90 days or 1 year from calibration. Some users will wish to maintain the highest accuracy by recalibrating at short intervals (e.g. every 24 hours). In these cases, recalibration becomes a routine task. For this reason, Routine Autocalibration procedures are also explained in Section 8 of the User's Handbook.

Users may wish to choose alternative schemes, accounting for:

- The accuracy required when in use,
- The instrument specifications (*User's Handbook Section 6*)
- The scheduled calibration intervals normally adopted by the user's organization

The Routine Calibration procedures are sufficient for all normal recalibration purposes, except when Pre-cal is called for (*Refer to Table 1.1*).

RE STANDARDIZATION

Occasions may arise when it is necessary to trim the instrument's internal Master Reference. For example, when the 4708 is to be made traceable to a different National Standard, after transportation from one country to another (*Refer to AUTOCAL FACILITIES page 1-3*).

CALIBRATION MEMORY CORRUPTION

Battery Change

Calibration corrections are stored in an internal memory which remains energized by a battery. The Lithium battery which powers the non-volatile calibration memory should be replaced after 5 years (*Refer to Section 4.3*). After replacement, a full Pre-calibration is required followed by a complete Routine Autocalibration.

Memory Check failure

When cal is pressed the constant is checked to be within prescribed limits before being stored. Values outside prescribed limits flag a *Fail 6*. The same check is performed:

- When the instrument is powered-up
- Each time the output is switched ON
- During each self-test routine

CRITICAL PART CHANGES

Recalibration (or Verification) is necessary after replacement of a critical PCB assembly or a critical component. These are listed in Table 1.1 (*see flap of this page*), indicating the extent of the recalibration necessary.

Ohms Internal Adjustments

- If the Power Supply/Current Heatsink has been changed it may be necessary to adjust the quiescent bias current (IQ) by internal adjustment. Refer to *Section 4.7* for further information.
- If a standard resistor value has been changed by subjecting to undue stress, it may be possible to recalibrate by internal adjustment. Refer to *Section 4.4* for further information.

Recalibration Procedures in this Section

ROUTINE AUTOCALIBRATION

The Routine Calibration procedures are sufficient for all normal recalibration purposes, except when Pre-cal is called for (*refer to Table 1.1 on flap of this page*).

REMOTE CALIBRATION OVER THE IEEE 488 BUS

The device-dependent commands necessary for routine calibration of the instrument over the IEEE 488 bus are described as a supplement to Section 5 of the User's Handbook. A guide line example is given, but this needs to be adapted for the bus controller in use.

PRE-CALIBRATION PROCEDURES

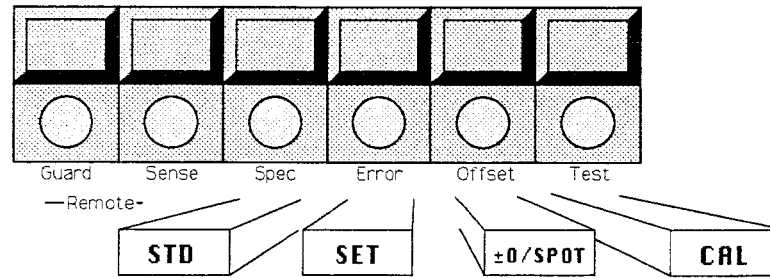
In an initial internal calibration process at manufacture, certain 'Pre-cal' parameters are established in a special calibration memory.

Under certain conditions (detailed in Table 1.1) these parameters need to be re-established by completing the 'Pre-Cal' procedure before a Full Routine Autocalibration.

| Assembly | Components Replaced | Calibration Required |
|--|---|--|
| Digital (11.2) | Complete Assembly Lithium Battery (<i>Sect. 4.3</i>) Non-volatile RAM (M10/M23) Non-volatile RAM Supply commutator components | Pre- & Routine Calibration Pre- & Routine Calibration Pre- & Routine Calibration Pre- & Routine Calibration |
| Reference Divider (11.4) | Complete Assembly Reference Assembly (<i>11.4-7</i>) Any set of main, guard or LSD switch FET's Reference Buffer Switch Driver Flip Flops or their preselected resistors R79 | Pre- & Routine Calibration Pre- & Routine Calibration Pre- & Routine Calibration Pre- & Routine Calibration Pre- & Routine Calibration Pre- & Routine Calibration |
| DC Assembly (11.5) | Complete Assembly 1V attenuator R73/R74 100mV attenuator R69/70/71 72/75/76 100V/1000V attenuator R8/9/25/26/46/47/64/65 88/95/98 | DC (All Ranges) only. DC (1V, 100mV, 10mV, 1mV, 100 μ V Ranges) only. DC (100mV, 10mV, 1mV, 100 μ V Ranges) only. DC (100V, 1000V Ranges) only. |
| Sine Source (11.6) | Complete Assembly | Specification Verification at User's Discretion |
| AC (11.7) | Complete Assembly Sense Amplifier Reference Inverter AC/DC Transfer & Integrators | Routine Calibration Routine Calibration Routine Calibration Routine Calibration |
| I/Ω Option (11.8) | Complete Assembly (N.B. Internal Adjustment required, refer to <i>Section 4.5</i>) +10 attenuator (R43/44) (DCI function) Current shunts R8/9/10/79/80 (DCI function) M8 and associated components Current Shunts Feedback resistor R45 Standard Resistors, associated pre-selected/variable trimmer resistors (Ω function) | I/ Ω DCI DCI ACI I/ Ω Option internal adjustment (<i>Section 1.5</i>) Ω calibration (replaced values only) |
| All Other Assemblies Not Listed Above | | Specification Verification at User's Discretion |

Table 1.1

AUTOCAL FACILITIES



These keys are activated by two rear panel switches (*refer to flap of page 1-2 'Preparing the 4708'*). When these modes are active, the legend 'cal' is presented on the MODE display.

The following is a general description of the facilities available. For specific information see the introduction proceeding each of the function's calibration routines.

CAL

The 4708 assumes that the selected range is to be calibrated at the exact Full Range value or at Zero. The instrument decides on 'Zero Offset' or 'Full Range Gain' from the OUTPUT display value (defined by the same limits as for 'SET'), and executes the calibration. If the value initially set on the OUTPUT display is below 2% of Full Range value, the instrument assumes that an offset calibration is requested, and if at 2% or above, a gain calibration is assumed.

CAL (with pre-selection)

If the CAL key is pressed after first pressing STD SET or ±0. The CAL key executes, then cancels, the preselected AUTOCAL mode.

Caution

The following keys preselect an AUTOCAL mode, modifying the action of the 'CAL' key.

SET

The SET key allows gain or offset calibration to a Calibration Standard value which cannot be adjusted to a nominal Full Range value or to absolute zero.

Before selecting SET, the $\uparrow\downarrow$ keys are operated to place the Calibration Standard value on the OUTPUT display and set the 4707 output level.

Pressing SET then informs the 4708 that calibration is to be carried out at this value. The instrument acknowledges by duplicating the value on the MODE display.

Next, the $\uparrow\downarrow$ keys are manipulated to null the 4708 output against the Calibration Standard (the OUTPUT display changes during this adjustment).

Pressing the CAL key executes the calibration. The 4708 memorizes the difference between the two display values, and exits from SET mode. This is shown by transfer of the Standard value from the MODE display to the OUTPUT display. The instrument uses the difference to modify stored constants, which in 'RUN' mode correct both positive and negative outputs on the calibrated range only.

±0 / SPOT

On the DCV function, the ±0 key is used to align the ON+ and ON- zeros of all DC voltage and current ranges, by a two part calibration on the 10V range. It is only necessary when the ON+ and ON- zeros of the 10V range do not coincide at the same null.

On the ACV and ACI function, the function of the key changes to SPOT Frequency calibration. When SPOT is pressed, the 4708 assumes that the spot frequency is to be changed, and so defaults the frequency to 1kHz. When used with SET, SPOT calibration can be carried out within 10% of the full range value, but when SPOT is used without SET, the 4708 assumes that the calibration is to be at Full Range. After SPOT calibration, selecting Spot F at the calibrated value achieves the highest possible accuracy. It is only necessary to perform Spot Frequency calibration if the accuracy achievable is required in use. For recall procedures see the User's Manual page 4-10.

STD

The STD key allows a user to re-standardize by trimming the value of the internal Master Reference voltage effectively changing the gain of all DC voltage and current ranges in the same ratio. The facility can be used to avoid a full recalibration of the 4708 when Laboratory References have been re-standardized (for instance when the instrument has been moved from one country to another).

First check ±0 Alignment. The STD calibration is carried out on either the 1V or 10V range, using the DC Low Voltage procedure. Select STD after placing the Calibration standard value on the OUTPUT display. Continue the routine from step (1.). Procedurally STD differs from SET only in the use of the STD key instead of the SET key.

Caution

Using the 'STD' key changes the gain of all voltage and current ranges

GENERAL NOTES

INTERCONNECTIONS

It is recognised that interconnection instructions may need to be adapted to meet an individual user's requirements. It is assumed that users will possess some knowledge of the operation and use of standards equipment.

SENSE AVAILABILITY AS FOLLOWS

| | | |
|--------------------|---|--------------------|
| 1V 10V 100V 1000V | - | Local/Remote Sense |
| 1mV 10mV 100mV | - | Local Sense only |
| All current ranges | - | not applicable |

(Local: 2-wire sense, Remote: 4-wire sense)

Output must be OFF to change sense connection (except that Remote changes automatically to Local when switching to Millivolt Ranges).

OUTPUT OFF DEFAULT WHEN UPRANGING

The 4708 cannot enter High-Voltage state with OUTPUT ON. Consequently, when ranging-up, the operating system allows the upranging to occur, but defaults to OUTPUT OFF for two specific cases:

- When upranging to the 1000V Range
- When upranging to the 100V Range;
To a voltage of 90V or more on DC
To a voltage of 75V or more on AC

Otherwise, OUTPUT remains ON when changing OUTPUT RANGE (refer to *User's Handbook Section 4, pages 4-7 to 4-9*).

GENERAL PROCEDURE

Prepare the instrument for calibration (refer to '*Preparing the 4708 procedure on flap of page 1-2*'). Note that your instrument will not necessarily have all options fitted - Option 10 incorporates the DC Voltage function, Option 20 the AC Voltage function and Option 30 adds the Resistance and Current functions. The message *Error 3* appears on the MODE display for any attempt to select an inappropriate mode. Select the equipment and procedures to be used. Set all sources to zero and all measurement devices to low sensitivity and configure using the interconnection diagram provided. If calibrating DC function, start with ± 0 Alignment check routine. When all calibration has been completed use the 'Return to Use' routine on the flap of page 1-2.

Calibration Routine

Set the 4708 to OUTPUT ON and Full Range value. Adjust the 4708 output to equal the calibration standard and press 'cal'. The OUTPUT display changes to nominal.

Calibration Routine (with preselection)

The OUTPUT display is set to the Calibration Standard value, the 4708 output is switched ON, and one of the calibration mode preselector keys (STD, SET or ± 0) is pressed. The 4708 output is adjusted to equal the Calibration Standard value, and the CAL key is pressed to execute the calibration.

1.2 DC CALIBRATION

1.2.1 Zero Calibrations

The following procedures are available;

±0 ALIGNMENT CHECK
±0 CALIBRATION
RANGE ZERO CALIBRATION

±0 ALIGNMENT CHECK

±0 alignment can be checked without affecting the stored constants. If necessary recalibrate before proceeding with DC Range Zero, DC Voltage, DC Current or DC Current Range Zero calibration (*refer to Appendix 2 - Calibration Source Zero Offsets*).

NOTE

For alignment checks only, set the security keyswitch to RUN.

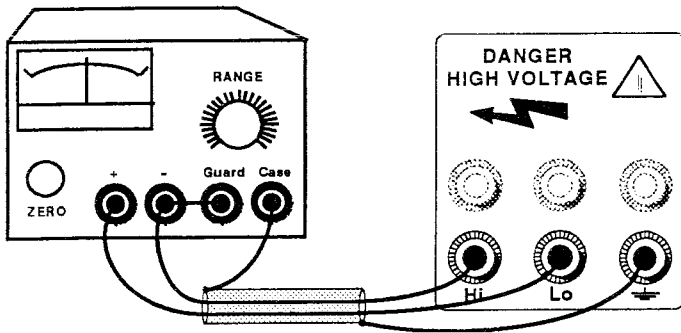
±0 CALIBRATION

The ±0 key is used to align the ON+ and ON- zeros of all DC voltage and current ranges, by a two part calibration on the 10V range. It is only necessary when the ON+ and ON- zeros of the 10V range do not coincide at the same null. Available in DC function only.

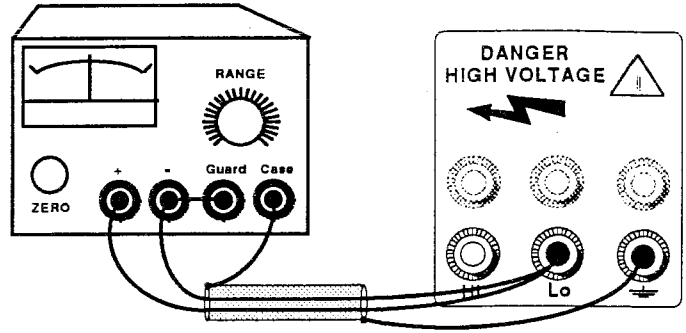
RANGE ZERO CALIBRATION

All the procedures for DC Gain calibration take into account the zero offsets. However a Range Zero calibration will allow the 4708 ON+ zero output to be set as close as possible to absolute zero. The procedure adjusts each range to a null detected across the sense 'Hi' and 'Lo' terminals.

±0 ALIGNMENT CHECK



4708 ON+ & ON- ALIGNMENT MEASUREMENT



NULL DETECTOR SELF-ZERO

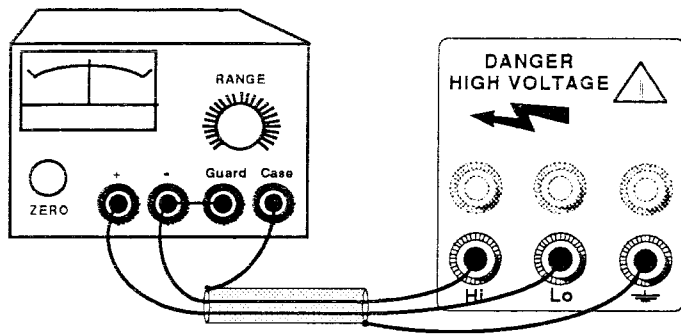
The following checks the ON+ and ON- zero turnover. The alignment should be checked and if necessary calibrated before proceeding with DC or DCI calibration (refer to *Appendix 2 - Calibration Source Zero Offsets*). It is not necessary to be in 'CAL' mode to perform the alignment check.

ROUTINE:

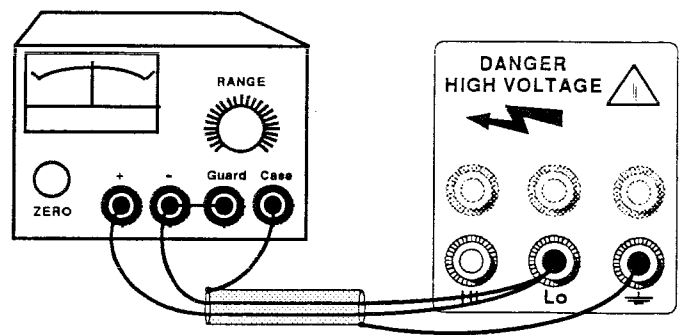
1. **Null Detector**
Set to Low sensitivity
2. **4708**
With OUTPUT OFF, Select DC, OUTPUT Zero.
Select 10V RANGE and ON+.
3. **Null Detector**
 - a. Successively increase sensitivity range, using 'self-zero' control to give near-zero readings; until a range is reached which clearly resolves a single increment of the least-significant digit on the 4708 OUTPUT display.
 - b. Disconnect Hi lead from the 4708 Hi terminal, and connect to Lo as illustrated for Null Detector self-zero.
 - c. Adjust Null Detector to zero using self-zero control.
 - d. Disconnect Hi lead from the 4708 Lo terminal, and reconnect to Hi.
 - e. Note Null detector reading.
4. **4708**
Select 'ON-'.
 5. **Null Detector**
Note Null detector reading.

If the turnover is considered excessive the user can recalibrate as close as possible to absolute zero (*refer on to ±0 CALIBRATION*)

±0 CALIBRATION



4708 ON+ & ON- ALIGNMENT



NULL DETECTOR SELF-ZERO

EXPLANATORY NOTE: After '±0' is selected; the calibration firmware stores the OUTPUT display value every time the CAL key is pressed, until it has received one reading from each polarity (as defined by the ON state). If it receives only one polarity it will continue to update the stored value until it stores the other polarity. It then carries out the necessary calculations to align the two zeros. Thus the ±0 calibration can be performed in either direction: ON+ first, then ON-; or ON- first, then ON+; and it is possible to correct the nulling for the first polarity, but not for the second (opposite). This procedure will allow, at time of calibration, the turnover error to be reduced to $\leq 5\mu\text{V}$ taking polarity into account. Use of the ±0 key should be followed by a complete Range Zero Calibration.

ROUTINE:

1. Null Detector

Set to low sensitivity.

2. 4708

- With OUTPUT OFF, Select DC, OUTPUT Zero.
- Select 10V RANGE and ON+.

3. Null Detector

- Successively increase sensitivity range, using 'self-zero' control to give near-zero readings; until a range is reached which clearly resolves a single increment of the least-significant digit on the 4708 OUTPUT display.
- Disconnect from the 4708 Hi terminal, and connect to Lo as illustrated for Null Detector self-zero.
- Adjust to zero using self-zero control.
- Disconnect from the 4708 Lo terminal, and reconnect to Hi.

4. 4708

Press ±0 Key: ±0 LED lights,
Adjust the OUTPUT $\uparrow\downarrow$ keys to null the detector.
Press CAL key: CAL LED lights

5. Null Detector

Reduce Null Detector sensitivity

6. 4708

Select 'ON-'

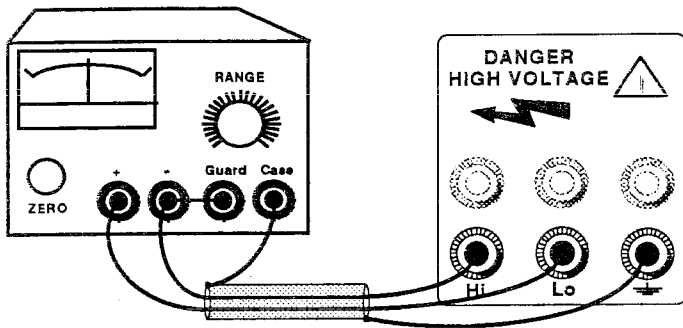
7. Null Detector

Successively increase sensitivity range, using the 4708 OUTPUT $\uparrow\downarrow$ keys to give near-zero readings; until the zeroed range is reached.

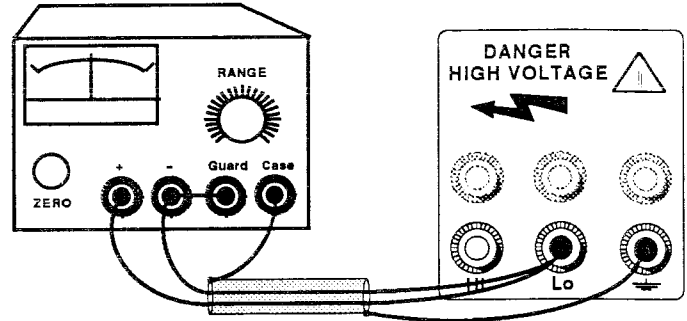
8. 4708

Press CAL key: CAL LED goes off.
±0 LED goes OFF, OUTPUT display falls to zero.

RANGE ZERO CALIBRATION



4708 ON+ RANGE ZERO



NULL DETECTOR SELF-ZERO

Calibration of DC Voltage Range Zeros.

The routine below includes a sequence for zeroing the Null Detector on the correct sensitivity range. This is necessary, because for most Null Detectors the zero is range-dependent. The self-zero input should include the Hi and Lo leads as shown in the connection illustration. Commencing with the lowest range calibrate the DC Zeros in the sequence of the table using the Zero Calibration Routine for each range selected.

ROUTINE:

1. **Null Detector**
Set to Low sensitivity
2. **4708**
With OUTPUT OFF, Select DC, OUTPUT Zero.
Select RANGE from table and ON+.
3. **Null Detector**
Successively increase sensitivity range, using 'self-zero' control to give near-zero readings; until a range is reached which clearly resolves a single increment of the least-significant digit on the 4708 OUTPUT display.
- a. Disconnect from the 4708 Hi terminal, and connect to Lo as illustrated for Null Detector self-zero.
- b. Adjust to zero using self-zero control.
- c. Disconnect Hi lead from the 4708 Lo terminal, and reconnect to Hi.
4. **4707**
Use OUTPUT $\uparrow\downarrow$ keys to zero the Null Detector reading. Continue until a single increment of the least-significant digit on the OUTPUT display gives the closest approach to zero. Press CAL key. CAL LED flashes once. OUTPUT display reverts to zero. The Range is now calibrated at zero to the Null Detector zero value.

Nominal Calibration Points for Range Zeros

| 4708 Range | Calibration Operation | 4708 Output Setting | AUTOCAL Key Used |
|------------|-----------------------|---------------------|--|
| 100mV | ON+ zero | (ON+) 0.0000mV | OUTPUT $\uparrow\downarrow$ then 'CAL' |
| 1V | ON+ zero | (ON+) .000000V | OUTPUT $\uparrow\downarrow$ then 'CAL' |
| 10V | ON+ zero | (ON+) 0.00000V | OUTPUT $\uparrow\downarrow$ then 'CAL' |
| 100V | ON+ zero | (ON+) 0.0000V | OUTPUT $\uparrow\downarrow$ then 'CAL' |
| 1000V | ON+ zero | (ON+) 0.000V | OUTPUT $\uparrow\downarrow$ then 'CAL' |

1.2.2 Voltage

INTRODUCTION

The following routines:

DC Low voltage (100mV to 10V) and
DC High Voltage (100V to 1kV)

adjust all DC Voltage Range gains against a Calibration Source, after correcting for the Source's zero offset.

The procedures assume that the 4708 'ON+' and 'ON-' output zero levels are coincident, and that all DC Voltage Range zeros have been adjusted to a null detected across the Sense 'Hi' and 'Lo' terminals (Refer to '±0 Alignment Routine').

Caution

First read 'Notes on the use of the Null Detector' (*Appendix 1*), and 'Calibration Source Zero Offsets' (*Appendix 2*).

1. CONNECTIONS

Ensure that all source outputs are OFF and Null Detector is set to Low Sensitivity. Use short leads and connect the Null Detector between the 4708 and Calibration Source as shown.

2. CALIBRATION ROUTINES

Start with the lowest Nominal Calibration Point from the table. Use the accompanying routine and repeat for each 4708 Range to be calibrated. Ensure that the interconnecting circuit has thermally stabilised before carrying out each 'Autocal' operation.

Notes:

- The Null Detector should be approximately self-zeroed before use to avoid excessive deflections. It is not necessary to do this on the sensitivity range used for final gain calibration, as the reference zero is set in operation (e.).
- The routine assumes calibration at nominal Full Range values. To trim the internal Master Reference Voltage on the 1V or 10V Range, or to calibrate at a non-nominal value, refer to following description of SET and STD keys.

DC AUTOCAL FACILITIES

CAL

If the CAL key is pressed the 4708 assumes that a calibration at either Zero or Full Range is required. It uses the value on the OUTPUT display to distinguish between Zero (Offset calibration) and Full Range (Gain calibration).

Caution

Below 2% of Range, the 4708 corrects for an assumed offset error; at 2% of Range and above the correction is for an assumed gain error.

If SET or STD has been pressed the CAL key executes the preselected AUTOCAL mode.

SET

The SET key allows calibration to any value in the selected Range (e.g. at a standard cell voltage). Press SET after operation (k.) and before operation (l.). The SET LED lights green and the OUTPUT display reading also appears on the MODE display. Continue the routine but note that on pressing CAL (step (n.)) the MODE display clears as its value is transferred to the OUTPUT display. The SET LED goes off.

Caution

If the value initially set on the OUTPUT display is below 2% of Full Range value, the instrument assumes that an offset calibration is requested, and if at 2% or above, a gain calibration is assumed.

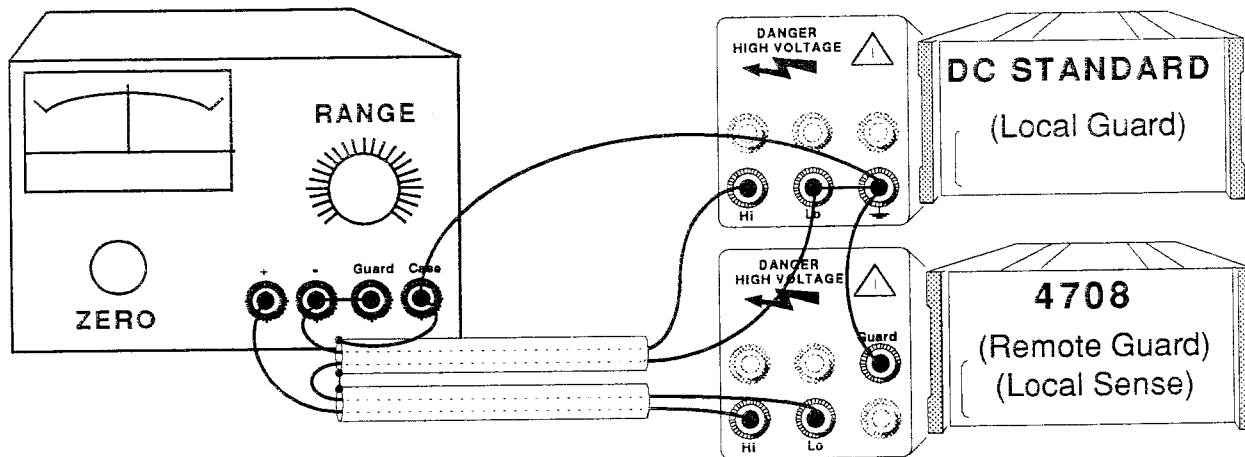
STD

The STD key allows a user to trim the value of the internal Master Reference voltage. STD calibration in DC mode effectively changes the gain of all voltage and current ranges in the same ratio. It does not affect values of AC or Ohms functions. STD calibration can be carried out on either 1V or 10V Ranges and differs from the SET procedure only in the use of the STD key instead of the SET key.


±0

DO NOT USE - refer to earlier ±0 Alignment routine.

DC LOW VOLTAGE (100mV to 10V)



WARNING:

Terminals marked with the  symbol carry the output of the 4708. These terminals and any other connections to the load under test could carry lethal voltages. Under no circumstances should users touch any of the front (or rear) panel terminals unless they are first satisfied that no dangerous voltage is present.

CAUTION:

Connection or disconnection of measurement circuitry should only be attempted when all voltage sources are OUTPUT OFF.

Before setting OUTPUT ON ensure that the correct polarities have been selected and any measurement device has been set to low sensitivity.

Routine:

- a. **Null Detector**
Set to Low sensitivity.
- b. **4708**
Ensure OUTPUT OFF.
Select OUTPUT Zero DC and required RANGE.
- c. **Calibration Source**
Set to 'ON+' Zero.
Select correct Range.
- d. **4708**
Press the ON+ key.
- e. **Null Detector**
Successively increase sensitivity range, using self-zero to give near-zero readings; until a range is reached which clearly resolves a single increment of the least-significant digit on the 4708 OUTPUT display.
- f. **4708**
Reselect OUTPUT Zero.
- g. **Null Detector**
Use the 'Self-zero' control to give an accurate zero.
- h. **4708**
Press the OFF key.
- j. **Calibration Source**
Set to the required voltage for Range gain calibration.

- k. **4708**
Use Full Range or OUTPUT $\uparrow\downarrow$ keys to set the required positive value on the OUTPUT display.
Press the ON+ key and select Full Range.

N.B. At this stage do not readjust the Null-Detector self-zero.

- l. **4708**
Use OUTPUT $\uparrow\downarrow$ keys to zero the Null Detector reading. Continue until a single increment of the least-significant digit on the OUTPUT display gives the closest approach to zero.

- m. **Null Detector**
Set to LOW sensitivity.

- n. **4708**
Press CAL key:
CAL LED flashes once.

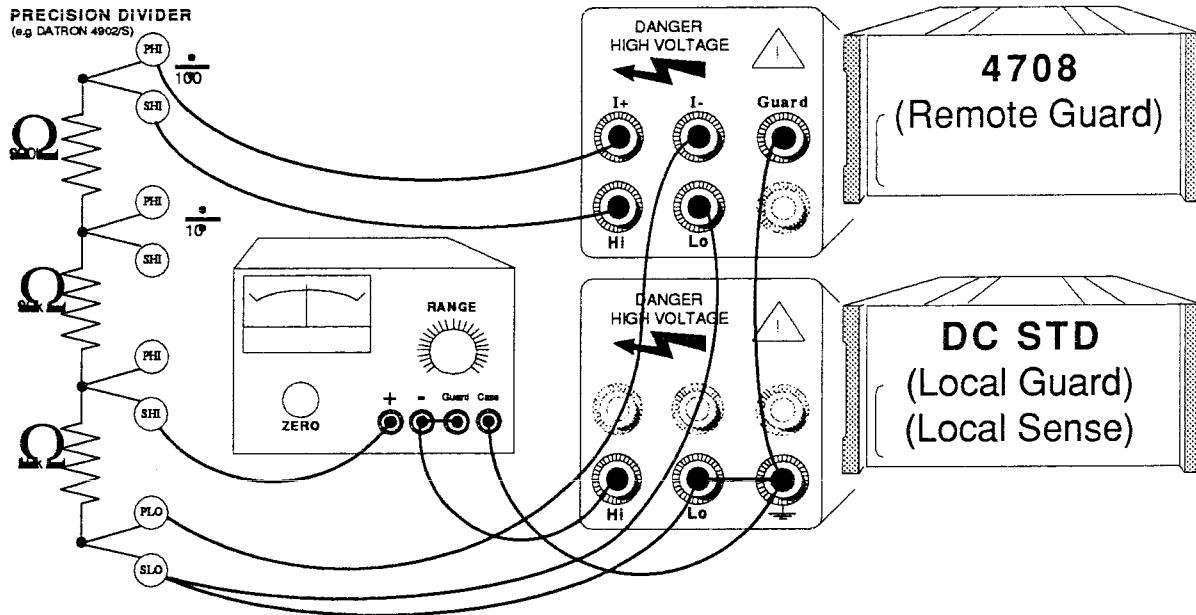
The 4708 is now gain-calibrated at this voltage.

Nominal Calibration Points for Low Voltage


| 4708 Range | Calibration Operation | Calibration Source & 4708 Output (ON+ Nominal) [1] | Control to be Adjusted to Obtain Null | Press 'CAL' Key to Calibrate |
|----------------|---------------------------|--|--|------------------------------|
| 100mV 100mV | Zero offset Range gain | 0.0000mV 100.0000mV | Null Det. 'Zero' 4708 OUTPUT $\uparrow\downarrow$ | Not used [2] 'CAL' |
| [3] 1V 1V | Zero offset Range gain | .000000V 1.000000V | Null Det. 'Zero' 4708 OUTPUT $\uparrow\downarrow$ | Not used [2] 'CAL' |
| [3] 10V 10V | Zero offset Range gain | 0.00000V 10.00000V | Null Det. 'Zero' 4708 OUTPUT $\uparrow\downarrow$ | Not used [2] 'CAL' |

- [1] It is expected that many users will wish to calibrate Range gains at values other than the nominals shown. In these cases set the Calibration Source voltage and 4708 OUTPUT display to in-house standard values near nominal.
- [2] For non-nominal gain calibration; use 'SET' key after entering value on the OUTPUT display before adjusting for null.
- [3] To trim the internal Master Reference voltage on 1V or 10V Range: use 'STD' key after entering value on 4708 OUTPUT Display before adjusting for null (Refer to Calibration Routine and description of 'STD').

DC HIGH VOLTAGE (100V to 1000V)



WARNING:

Terminals marked with the  symbol carry the output of the 4708. These terminals and any other connections to the load under test could carry lethal voltages. Under no circumstances should users touch any of the front (or rear) panel terminals unless they are first satisfied that no dangerous voltage is present.

CAUTION

Connection or disconnection of measurement circuitry should only be attempted when all voltage sources are OUTPUT OFF.

Before setting OUTPUT ON ensure that the correct polarities have been selected and any measurement device has been set to low sensitivity.

Note: On the diagram, the terminals of the Precision Divider are marked 'PHI', 'PLO', 'SHI' and 'SLO'. These are terms which apply to the Datron 4902 and 4902S, referring to their Power Hi & Lo inputs and Hi & Lo Sense points, for true 4-wire connections (described in their User's Handbook).

For other dividers, it is important that true 4-wire connections are made directly to the elements of the divider, and that the divider has been calibrated at the connection points.

Routine:

- a. **Null Detector**
Set to Low sensitivity.
- b. **4708**
Ensure OUTPUT OFF.
Select OUTPUT Zero DC and required RANGE.
- c. **Calibration Source**
Set to 'ON+' Zero.
Select correct Range.
- d. **4708**
Press the ON+ key.
- e. **Null Detector**
Successively increase sensitivity range, using self-zero to give near-zero readings; until a range is reached which clearly resolves a single increment of the least-significant digit on the 4708 OUTPUT display.
- f. **4708**
Reselect OUTPUT Zero.
- g. **Null Detector**
Use the 'Self-zero' control to give an accurate zero.
- h. **4708**
Press the OFF key.
- j. **Calibration Source**
Set to the required voltage for Range gain calibration.

- k. **4708**
Use Full Range or OUTPUT $\uparrow\downarrow$ keys to set the required positive value on the OUTPUT display.
Press the ON+ key and select Full Range.

N.B. At this stage do not readjust the Null-Detector self-zero.

- l. **4708**
Use OUTPUT $\uparrow\downarrow$ keys to zero the Null Detector reading. Continue until a single increment of the least-significant digit on the OUTPUT display gives the closest approach to zero.

- m. **Null Detector**
Set to LOW sensitivity.

- n. **4708**
Press CAL key:
CAL LED flashes once.

The 4708 is now gain-calibrated at this voltage.

Nominal Calibration Points for High Voltage

| 4708 Range | Calibration Operation | Precision Divider Select | Calibration Source (ON+ Nominal) [1] | 4708 Output (ON+ Nominal) [1] | Control to be Adjusted to Obtain Null | Press 'CAL' Key to Calibrate |
|------------|-----------------------|--------------------------|--------------------------------------|-------------------------------|---|------------------------------|
| 100V | Zero offset | +10 | 0.00000V | 0.0000V | Null Det. 'Zero' 4708 OUTPUT $\uparrow\downarrow$ | Not used [2] 'CAL' |
| 100V | Range gain | +10 | 10.00000V | 100.0000V | | |
| 1000V | Zero offset | +100 | .00000V | 0.000V | Null Det. 'Zero' 4708 OUTPUT $\uparrow\downarrow$ | Not used [2] 'CAL' |
| 1000V | Range gain | +100 | 10.00000V | 1000.000V | | |

[1] It is expected that many users will wish to calibrate Range gains at values other than the nominals shown. In these cases set the Calibration Source voltage and 4708 OUTPUT display to in-house standard values near nominal.

[2] For non-nominal gain calibration; use 'SET' key after entering value on the OUTPUT display before adjusting for null.

1.2.3 Current

The following routine:

DC Current Calibration (100 μ A to 1A)

adjusts all DC Current Range Zeros and Range Gains against a Standardized DVM, using a set of calibrated current shunts. The routine sets an independent output zero level using the standard calibration load for the Range. The Range Zero calibration has not been separated from the Range Gain calibration, because of the need to change shunts between ranges.

The procedure assumes the following:

- The 4708 'ON+' and 'ON-' output zero levels are coincident, having been adjusted to a null detected across the Sense 'Hi' and 'Lo' terminals on the 10V Range (*refer 'Zero Alignment Check'*) and
- that the 4708 DC 1V and 100mV Full Range values have already been calibrated or verified.
- the DVM used has been correctly Standardized (*sic*)

GENERAL PROCEDURE

1. STANDARDIZATION

First read 'Calibration Source Zero Offsets'. Note that any offset in the source's output must be nullified before gain calibration is carried out.

The Zero and Full Range routines assume that the preferred shunt values (*refer to table*) are used and therefore the DVM has been standardized against the 1V and 100mV Ranges of the 4708.

Preferred Shunt Values

| 4708 Range | Nominal Shunt value | Minimum Wattage | Nominal DVM Reading |
|-------------|---------------------|-----------------|---------------------|
| 100 μ A | 10k Ω | 1mW | 1V |
| 1mA | 1k Ω | 10mW | 1V |
| 10mA | 100 Ω | 100mW | 1V |
| 100mA | 10 Ω | 1W | 1V |
| 1A | 0.1 Ω | 1W | 100mV |

2. CONNECTIONS

Ensure that the 4708 OUTPUT OFF LED is lit and select DCI function. Connect the calibrated current shunt and DVM across the 4708 Hi and Lo terminals as shown. Use short leads and ensure that the DVM is set to the 1V Range.

3. CALIBRATION ROUTINE

Caution

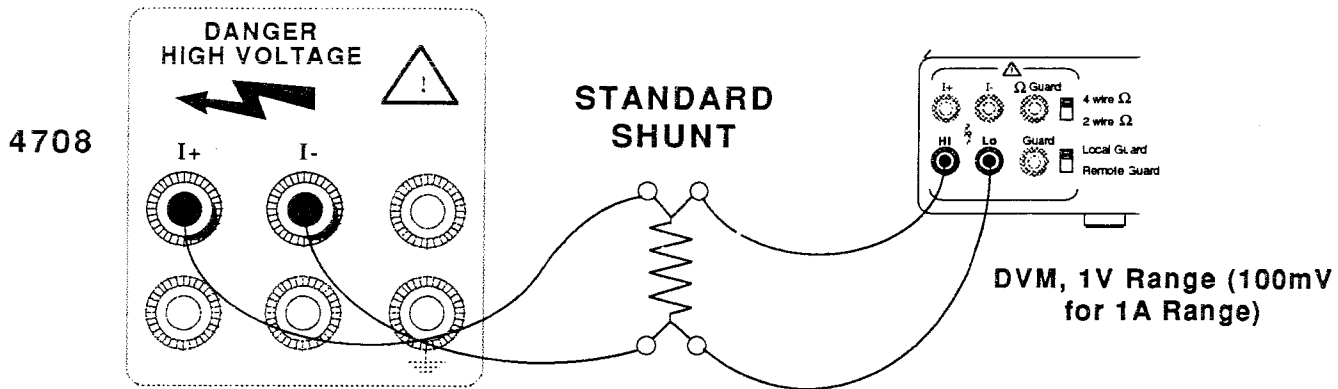
The combined Zero and Full Range procedure assumes that the DVM used has been standardized on the required voltage ranges.

EXPLANATORY NOTE

The offset voltage developed across the shunt is measured by the DVM. However as the shunt is unlikely to be exactly a nominal value, the voltage measured across the shunt for a Nominal Full Range current must be calculated from the product of the shunts Actual Value and the Nominal Full Range Current. The 4708 OUTPUT $\uparrow\downarrow$ keys are adjusted to give this reading and the 'CAL' key is pressed.

Use the routine and accompanying table, start with the 100 μ A Range and repeat the procedure for each 4708 Range. Ensure that the interconnecting circuit has thermally stabilised before carrying out each 'Autocal' operation.

DC CURRENT (100µA to 1A)



Zero Calibration:

1. **4708**
Ensure OUTPUT OFF
Select RANGE as detailed in the table below.
2. **DVM**
Press 'Input Zero' key.
3. **4708**
Ensure 'Zero' OUTPUT is selected.
Select OUTPUT 'ON+'.
Increment the OUTPUT value until the DVM reads zero.
Continue until a single increment of the least-significant digit on the OUTPUT display gives the closest approach to zero.
Press CAL. CAL LED flashes once.
OUTPUT display reverts to zero.

Range Gain Calibration:

4. **4708**
Select Full Range.
Increment the OUTPUT value until the DVM reads the product of the Shunt value and the Nominal Full range output.
Press CAL. The Range has now been gain-calibrated at this current.
Select Zero and OUTPUT OFF. Select next range and shunt value.
Repeat the routine from Step 1.

| 4708 Range | Calibration Operation | 4708 OUTPUT | To correct DVM reading: | 4708 Autocal |
|------------|--------------------------------------|--------------------------|--|------------------------------|
| 100µA | DVM Zero Range Zero Range Gain | OFF ON+ FULL RANGE | DVM 'Input Zero' 4708 OUTPUT ↑↓ keys 4708 OUTPUT ↑↓ keys | -Not Used- 'CAL' 'CAL' |
| 1mA | DVM Zero Range Zero Range Gain | OFF ON+ FULL RANGE | DVM 'Input Zero' 4708 OUTPUT ↑↓ keys 4708 OUTPUT ↑↓ keys | -Not Used- 'CAL' 'CAL' |
| 10mA | DVM Zero Range Zero Range Gain | OFF ON+ FULL RANGE | DVM 'Input Zero' 4708 OUTPUT ↑↓ keys 4708 OUTPUT ↑↓ keys | -Not Used- 'CAL' 'CAL' |
| 100mA | DVM Zero Range Zero Range Gain | OFF ON+ FULL RANGE | DVM 'Input Zero' 4708 OUTPUT ↑↓ keys 4708 OUTPUT ↑↓ keys | -Not Used- 'CAL' 'CAL' |
| *1A | DVM Zero Range Zero Range Gain | OFF ON+ FULL RANGE | DVM 'Input Zero' 4708 OUTPUT ↑↓ keys 4708 OUTPUT ↑↓ keys | -Not Used- 'CAL' 'CAL' |

*DVM on 100mV Range for 1A.

1.3 AC CALIBRATION

The following routines:

- AC Voltage Calibration (1Volt to 1000Volts)
- 2-Wire HF Compensation (1Volt & 10Volt)
- Millivolts LF (1mVolt to 100mVolts)
- Millivolts HF (1mVolt to 100mVolts)
- AC Current Calibration (1mA to 1A)
- AC Current Calibration (100 μ A to 1A)

adjust the Gain of all AC Voltage and Current Ranges.

1.3.1 Introduction

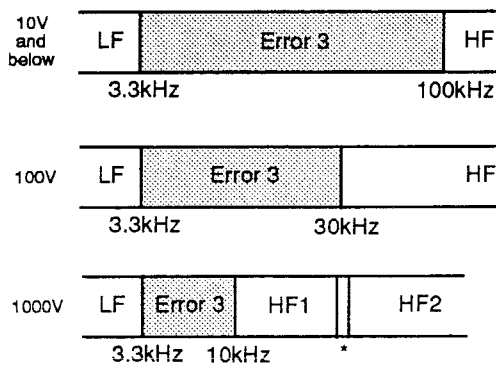
'Wideband' Calibration

When CAL is pressed without preselecting SET, or STD; the instrument makes the assumption that each OUTPUT Range is to be calibrated at the exact Full Range value, at either LF or HF, or both.

This allows two correction values to be stored for each output range. From their difference, the microprocessor calculates a compensation factor, which affects the corrections applied at all subsequently-selected frequencies on that output range. In this way, the instrument can be calibrated to meet its 'Wideband' specification.

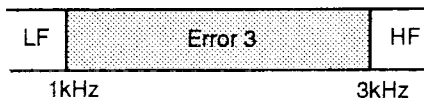
To ensure that the selected Low and High frequencies have sufficient separation for the compensation to be effective over the full frequency range, calibration is automatically prohibited in an 'excluded' band of frequencies for each output range. Because of the extended frequency range of lower Voltage ranges, and the Voltage/Frequency constraints on higher Voltage ranges, the exclusion band can differ from one output range to another. If an excluded frequency is selected, the calibration is cancelled and **Error 3** is displayed. The following diagram illustrates the mid-frequency exclusions:

Voltage Ranges:



* HF1/HF2 cross-overs are Frequency-Range dependent:
 HF1 is available up to 33kHz on the 10kHz Range.
 HF2 is only available above 30kHz on the 100kHz Range.
 (Note for 700V HF2 SET mode must be used)

All Current Ranges:



'Spot' Calibration

Spot Calibration is not required for operation of the AC functions - it is merely a method of achieving the highest possible levels of accuracy. For each output range, a user may select five frequencies for SPOT calibration. The 4708 stores frequencies and their amplitude corrections, in memories that are separate to those used for wideband corrections. Enhanced accuracy is obtained at these spots, as any flatness errors in the wideband calibration are eliminated.

AC AUTOCAL FACILITIES

SET

The SET key allows calibration to any value between 20% and 200% of nominal Full Range value (20% to 110% on 1000V range). If, for instance, an adjustable DC voltage standard is not available, the SET key permits the 4708 to be calibrated against a Thermal Transfer standard whose reference is a buffered bank of Standard Cells. SET can also be used as a means of compensating for known errors in the Measurement System.

Press SET after selecting the Full Range OUTPUT value. The SET LED lights green and the OUTPUT display reading also appears on the MODE display. Continue the routine but note that on pressing CAL the MODE display clears as its value is transferred to the OUTPUT display. The SET LED goes off.

STD

CAUTION

This calibration affects all Voltage and Current Ranges and is NOT recommended - Use DC standardization procedure for highest accuracy.

The STD facility is restricted to the 1V and 10V Ranges, on the 100Hz and 1kHz Frequency Ranges only. STD calibration differs from SET procedure only in the use of the STD key instead of the SET key.

± 0 / Spot

When SPOT is pressed in either ACV or ACI functions, the 4708 assumes that the spot frequency is to be changed, and so the frequency defaults to 1kHz. The Frequency \updownarrow keys are then used to program the required frequency. When used with SET, spot calibration can be carried out within 10% of the full range output, but when spot calibration is attempted without the use of SET, the 4708 assumes that the calibration is performed at full range.

AC CALIBRATION SEQUENCE

INTRODUCTION

Because most users will calibrate the 4708 AC ranges via thermal transfer standards, the calibration procedures assume that this method will be employed. However, details of setting up a thermal transfer standard are not included, as several different models are in use, each with its own methods of connection and procedures.

Instead it is assumed that users will be able to operate their own equipment correctly, according to the manufacturer's instructions. The procedures which follow therefore concentrate on the operation of the 4708 during calibration, accepting that the required thermal transfer will be set up to a DC source of suitable accuracy.

AC PROCEDURES

AC Voltage Calibration (1V to 1000V)

Select AC and the desired frequency, set the 4708 OUTPUT display to the Calibration Standard value, and switch the 4708 OUTPUT ON. If calibrating a non-nominal voltage value, SET needs to be selected. Adjust the 4708 output to obtain a null at the Calibration Standard value, and press the CAL key to execute the calibration.

LF Millivolts Calibration

Because 'Flatness' data is passed on to the millivolt ranges from the 1V Range calibration, the 1V range must be calibrated first. A DVM is then standardized at the required millivolt value and frequency, using the calibrated 1V Range and an Inductive Voltage Divider (IVD). The desired frequency is selected, the OUTPUT display set to Full Range, and incremented or decremented to give the required value on the DVM. If calibrating at a non-nominal value SET must be selected. The CAL key is pressed to execute the calibration.

HF Millivolt Calibration

From the 10V Range a 10% Range correction is calculated. This is applied at 100mV on the 1V Range to standardize a DVM, which is subsequently used to calibrate the 100mV Full Range. The process is extended to calibrate the 10mV Range from 10% of the 100mV Range, and 1mV Range from 10% of the 10mV Range.

Current calibration

(Using Thermal Transfer, Current Shunts and DC Current Standard)
The method employs a DC Current Standard, so that the shunt remains connected for both AC and DC nulling of the Thermal Transfer Standard.

Alternative Current Calibration

(Using verified 4708 1V Range, Calibrated Standard AC Shunts and AC DVM)

This method required Standard Current Shunts which have been designed to give a flat frequency response. Each current range requires its own specific value of shunt, calibrated to develop either 1V or 100mV Full Range at LF and HF. An AC DVM is standardized to the appropriate voltage, and the Current range is calibrated when the voltage across its shunt is correct.

High Frequency Calibrations

Several iterations may be required to achieve satisfactory calibration; particularly if the initial errors are large, or if the Transfer System being used imposes a long calibration time.

CAUTION:

Connection or disconnection of measurement circuitry should only be attempted when all voltage sources are OUTPUT OFF. Before setting OUTPUT ON ensure the correct polarities have been selected and that any measurement device has been set to low sensitivity.

SPOT Memory Erasure

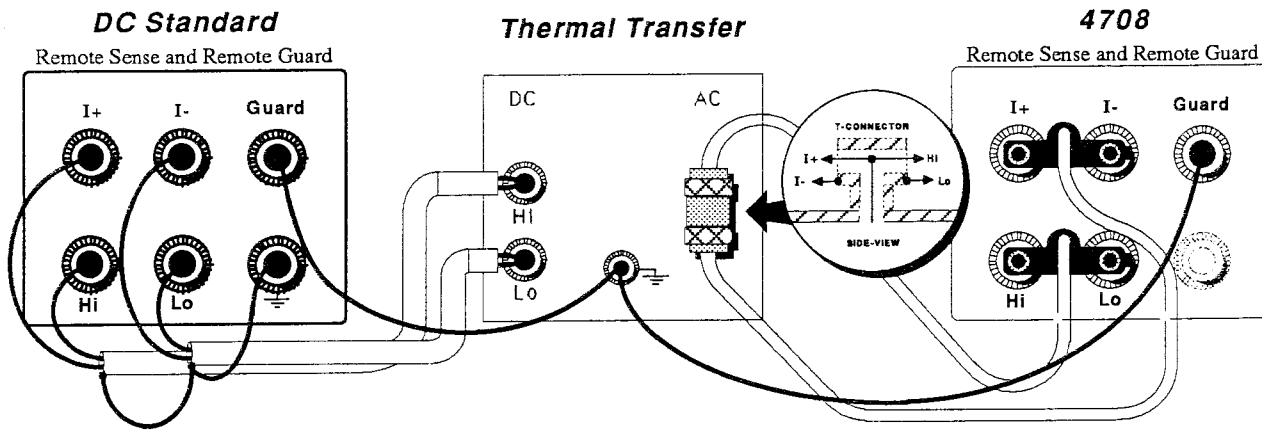
To prevent unwanted calibrations at obsolete spot frequencies, it is possible to 'uncalibrate' any spot frequency on any range. The procedure is:

- 1 Select SPOT
- 2 Select zero output
- 3 Set Output ON
- 4 Press Cal


Any subsequent selection of SPOT will cause the message 'SFX ---' to be displayed.

1.3.2 Voltage

AC VOLTAGE CALIBRATION (1V to 1000V)



WARNING:

Terminals marked with the  symbol carry the output of the 4708. These terminals and any other connections to the load under test could carry lethal voltages. Under no circumstances should users touch any of the front (or rear) panel terminals unless they are first satisfied that no dangerous voltage is present.

Note: For the arrangement shown in the diagram, the coaxial T-connector provides true 4-wire connection to the AC coaxial input of the Thermal Transfer.

For Thermal Transfers with other AC terminations, it is important that true 4-wire connections are made directly to the AC input terminals, and that the device has been calibrated at the connection points.

Ensure case of Thermal Transfer Standard is adequately grounded.

Commencing with the 1V Range, calibrate the 4708 at the calibration points in the table as part of the following procedure:

1. 4708 & DC Voltage Standard

With OUTPUT OFF, connect to the Thermal Transfer AC and DC inputs, respectively.

2. 4708

- a. On A C FUNCTION, select the required OUTPUT RANGE.
- b. Select the required FREQUENCY RANGE.
- c. Use FREQUENCY $\uparrow\downarrow$ keys to display the required Calibration Frequency.
- d. Press the Full Range key to display the required Calibration Voltage.
- e. Set 4708 OUTPUT ON.

3. DC Voltage Calibration Standard

Set to the Calibration Voltage, OUTPUT ON.

4. Thermal Transfer Standard

- a. Configure for DC measurement at the required Calibration Voltage.
- b. Adjust for Null at the Calibration Voltage.
- c. Configure for AC measurement at the Calibration Voltage.

5. 4708

- a. Use the OUTPUT $\uparrow\downarrow$ keys to adjust the OUTPUT Display reading to obtain a null on the Thermal Transfer.
- b. Execute the calibration by pressing the CAL key. Repeat (a.) to (b.) until satisfactory null is achieved.

Calibration Points for 1V to 1000V Ranges.

| DC Standard OUTPUT Voltage | 4708 OUTPUT RANGE/ FREQUENCY | | 4708 Nominal OUTPUT Voltage | Freq. Band set by 4708 |
|----------------------------|------------------------------|--------|-----------------------------|------------------------|
| 1.000000V | 1V | 1kHz | 1.000000V | LF |
| * 1.000000V | 1V | 1MHz | 1.000000V | HF |
| 10.00000V | 10V | 1kHz | 10.00000V | LF |
| * 10.00000V | 10V | 1MHz | 10.00000V | HF |
| 100.0000V | 100V | 1kHz | 100.0000V | LF |
| 100.0000V | 100V | 100kHz | 100.0000V | HF |
| 1000.000V | 1000V | 1kHz | 1000.000V | LF |
| 1000.000V | 1000V | 30kHz | 1000.000V | HF1 |
| **700.000V | 1000V | 100kHz | 700.000V | HF2 |

* Note that at these points a 2-wire calibration is also possible.

** Note that SET must be used for this calibration point.

2-WIRE HF COMPENSATION (1V & 10V) (Using AC DVM)

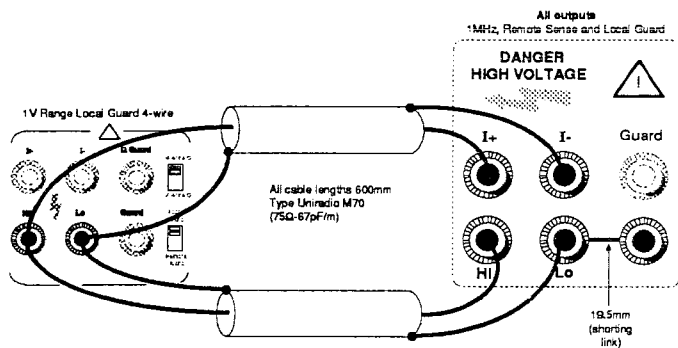


Fig. 1 AC DVM Standardization

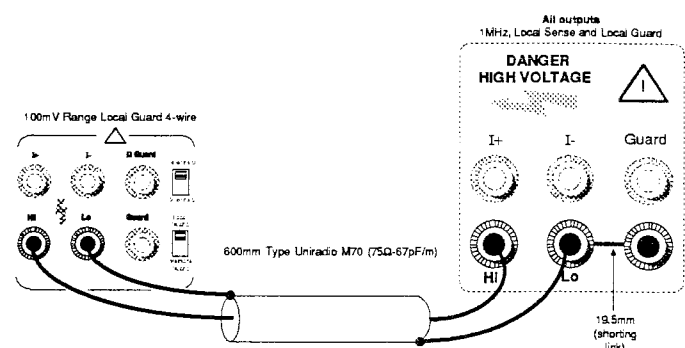


Fig. 2 4708 Calibration

On the 1V and 10V ranges there are two HF calibration memories. One holds the correction value obtained during Remote Sense (4-wire) 'wideband' calibration; the other contains a 2-wire HF compensation value which is added to the wideband correction, when Remote Sense is not selected (local sense).

During a 4-wire HF calibration on the 1V or 10V range, the stored HF 2-wire compensation value is cleared to zero. Any 4-wire HF calibration to be performed must therefore be completed before the 2-wire compensation is executed.

Calibrate the 4708 at the calibration points in the table, commencing with the 1V Range as part of the following procedure:

1. 4708 & AC Voltmeter

With 4708 OUTPUT OFF, connect the AC DVM to the 4708 terminals using the exact 4-wire connections as in Fig. 1.

2. AC Voltmeter

Configure for AC measurement at 1V or 10V.

3. 4708

- On AC FUNCTION, select the required OUTPUT RANGE.
- Select the required FREQUENCY RANGE.
- Use FREQUENCY keys to display the required Calibration Frequency.
- Press the Full Range key to display the required Calibration Voltage.
- Set 4708 OUTPUT ON.

4. HF 2-wire Calibration Sequence

- Record the DVM reading.
- Set 4708 OUTPUT OFF.
- On the 4708 deselect Remote Sense.
- Connect the DVM to the 4708 Hi and Lo terminals for measurement of the 4708 2-wire output as shown in Fig. 2.
- Set 4708 OUTPUT ON.
- Use the 4708 OUTPUT keys to display the DVM reading recorded at (a.)
- Execute the calibration by pressing the CAL key.

Calibration Points for 2-wire HF Compensation.

| DC Standard OUTPUT Voltage | 4707 OUTPUT RANGE/ FREQUENCY | 4707 Nominal OUTPUT Voltage | Freq. Band set by 4707 |
|----------------------------|------------------------------|-----------------------------|------------------------|
| 1.000000V | 1V 1MHz | 1.000000V | HF |
| 10.00000V | 10V 1MHz | 10.00000V | HF |

MILLIVOLTS (LF) FULL RANGE CALIBRATION (1mV - 100mV)

(Using calibrated 4708 1V Range, Inductive Voltage Divider (IVD) and AC DVM)

4708

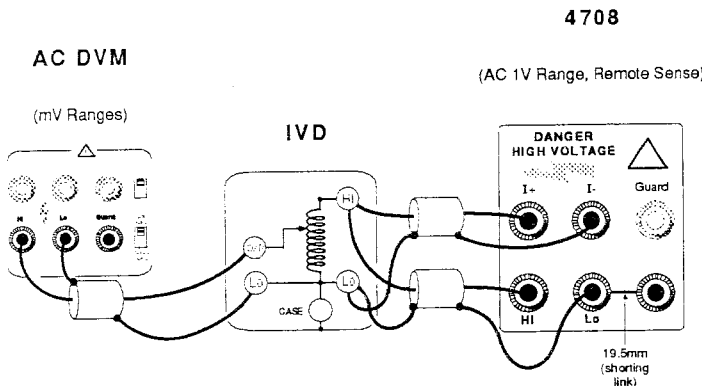


Fig. 1 Standardization of DVM

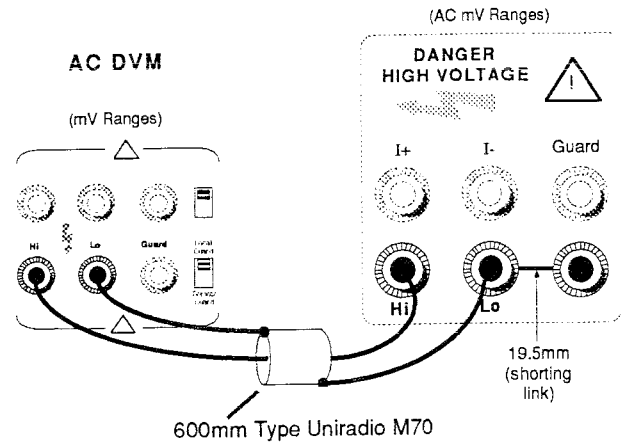


Fig. 2 Calibration of 4708

CALIBRATION PROCEDURE

Standardize and calibrate at the calibration points in the table using the following procedures:

Stage 1

Connect as Fig. 1, to standardize the DVM.

1 4708, IVD and AC DVM

With OUTPUT OFF, connect the circuit for Standardization.

2 IVD

Set ratio as required for the Millivolt Range to be calibrated.

3 AC DVM

Configure for measurement at the required Calibration Point.

4 4708

- On AC FUNCTION, select 1V RANGE.
- Select the required Frequency Range.
- Use FREQUENCY $\uparrow\downarrow$ keys to display the required Calibration Frequency.
- Use OUTPUT $\uparrow\downarrow$ keys to display the required IVD input voltage (if at Nominal Full Range, merely press the Full Range key).
- Set OUTPUT ON and note DVM reading as V1.
- Set OUTPUT OFF, and reconnect the circuit for Calibration.

Stage 2

Connect as Fig. 2, to calibrate the 4708.

1 4708

Selecting SET as required in the following procedure:

- Select the required Millivolt OUTPUT RANGE.
- Use OUTPUT $\uparrow\downarrow$ keys to display the Calibration Voltage on the OUTPUT Display (if at Nominal Full Range, merely press the Full Range key).
- Set 4708 OUTPUT ON (and if NOT at Nominal Full Range, Select SET).
- Use the $\uparrow\downarrow$ keys to adjust the OUTPUT Display reading to obtain V1 on the DVM.
- Execute the calibration by pressing the CAL key. Repeat (d.) to (e.) as required. Set OUTPUT OFF.

Nominal Cal. Points for Millivolt Ranges.

| IVD Ratio (1V Range to mV Range) | 4708 OUTPUT RANGE/ FREQUENCY | 4708 Nominal OUTPUT Voltage | Freq. Band set by 4708 |
|----------------------------------|------------------------------|-----------------------------|------------------------|
| 10 : 1 | 100mV 1kHz | 100.0000mV | LF |
| 100 : 1 | 10mV 1kHz | 10.0000mV | LF |
| 1000 : 1 | 1mV 1kHz | 1.0000mV | LF |

MILLIVOLTS (HF) CALIBRATION PROCEDURE (1mV to 100mV)
 (Using verified 4708 1V and 10V Ranges, 10% Range Correction factor and AC DVM)

SUMMARY

The verified output values of 1V on the 1V Range; and 10V on the 10V Range are used to measure the 4708 linearity error at 1V on the 10V range. From the linearity measurement, a 10% of range Linearity and Scaling Factor 'C' is derived.

This factor is subsequently used to correct the 4708 output setting at 10% of range, to standardize a DVM for calibration of the next range down.

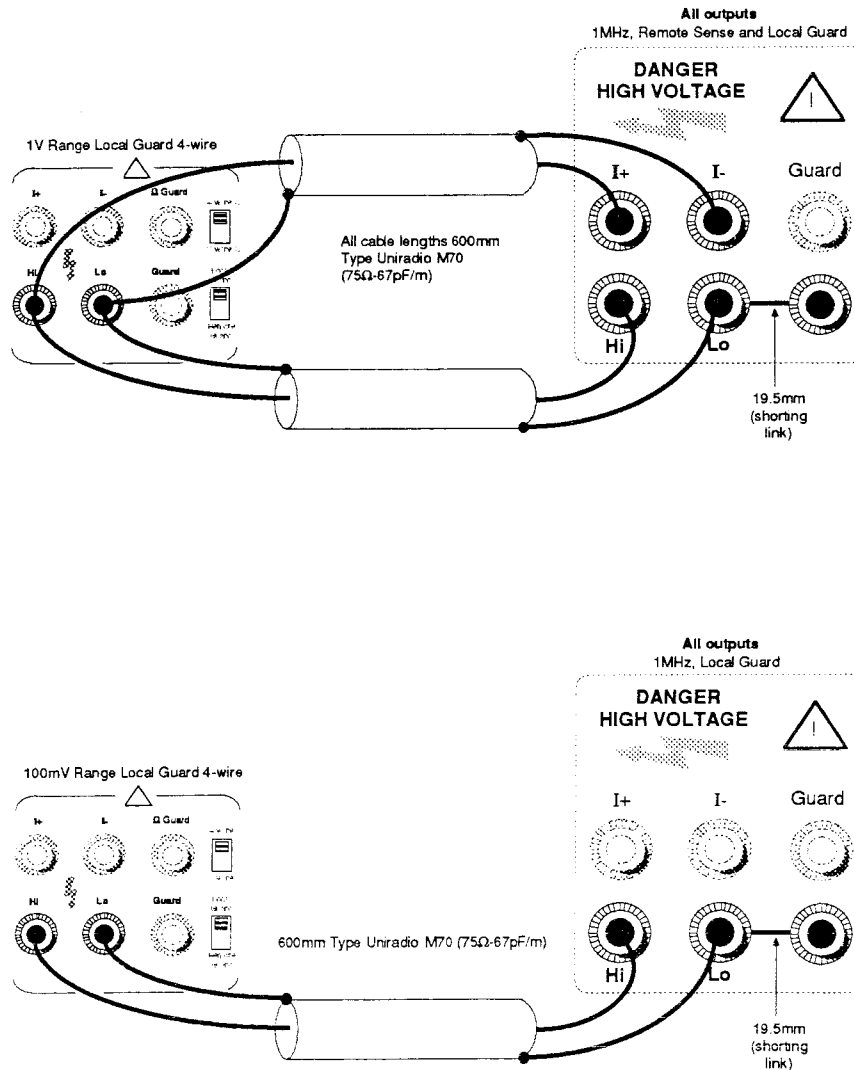
N.B. Calibrate the 4708 at or close to the calibration points in the table, selecting SET as required as part of the following procedure.

Note:

It is assumed that the 1V and 10V ranges have been Wideband calibrated at the required HF calibration points. It is also assumed that the Millivolts (LF) Calibration has been completed.

Nominal Cal. Points for HF Millivolt Ranges.

| 4708 OUTPUT RANGE/ FREQUENCY | | 4708 Nominal OUTPUT Voltage | Freq. Band set by 4708 |
|------------------------------|------|-----------------------------|------------------------|
| 100mV | 1MHz | 100.0000mV | HF |
| 10mV | 1MHz | 10.0000V | HF |
| 1mV | 1MHz | 1.0000mV | HF |



Stage 1

Derive the Linearity and Scaling Factor 'C' as follows
(C is a number of value close to 0.1):

- a. Ensure that the Millivolts (LF) Calibration has been completed.

Ensure that the 4708 has been calibrated and verified at 10V and 1V HF (1MHz) Full Range.
Record the measured values as follows:

4708 10V FR setting - 10.000,00V
Actual output voltage - 'V1'

4708 1V FR setting - 1.000,000V
Actual output voltage - 'V2'

- b. Calculate 1V correction 'V3' = $\frac{1}{V2}$

- c. With OUTPUT OFF connect a DVM to the 4708 terminals using the exact 4-wire connections as in Fig. 1.
Set the DVM to measure AC on its 1V range.

- d. On 4708, select the 1V range and Remote Sense.
Set FREQUENCY to 1MHz.
Set OUTPUT display reading to V3.
Set OUTPUT ON, and note the DVM reading as 'Vt'.
Set OUTPUT OFF.

- e. On 4708, select the 10V range (Remote Sense).
Set 4708 OUTPUT display reading to 1V.
Set OUTPUT ON.
Adjust the OUTPUT display for a DVM reading of Vt.

- f. Note the 4708 OUTPUT display reading as 'V4'.
Set OUTPUT OFF.

- g. From the values V1 and V4 calculate the 10V range linearity correction and scaling factor 'C' as follows:

$$C = \frac{V1 \times V4}{100}$$

Note:

The optimum resolutions quoted above the boxes in this column may not be achievable with the DVM in use. In these cases it is permissible to reduce the resolution by a maximum of 1 digit only.

Record in 6^{1/2} digits resolution

| |
|-------------|
| V1 =V |
| V2 =V |
| V3 =V |

Vt is a transfer value

| |
|-------------|
| Vt =V |
|-------------|

Record in 6^{1/2} digits resolution

| |
|-------------|
| V4 =V |
|-------------|

Calculate in 6^{1/2} digits resolution

| |
|-----------|
| C = |
|-----------|

N.B. The following calibration from the front panel can only be carried out if the IEEE Address switch on the rear panel is set to Address 31 (11111).

Stage 2

To Calibrate the 100mV Range Full Range Output

- a. Insert the Calibration security key into the 'CALIBRATION ENABLE' switch on the rear panel, and turn to 'ENABLE'.
- b. Ensure that the DVM is still connected to the 4708 terminals as shown in Fig. 1.
- c. Set the 4708 to the 1V range.
Calculate the value 'V3 x C'.
Set OUTPUT display to this value.
- d. Set the DVM to measure 100mV.
- e. Set 4708 OUTPUT ON, allow the output to settle.
Note the DVM reading as 'V(100t)'.
- f. Set 4708 OUTPUT OFF and reconnect the DVM to the 4708 terminals in 2-wire as shown in Fig. 2.
- g. Set 4708 to its 100mV range.
(Remote Sense is automatically deselected.)
Set OUTPUT ON and adjust the 4708 Output for a DVM reading of V(100t).
Press the 'CAL' pushbutton and observe the DVM reading.
- h. Repeat operation (g.) until the post-CAL DVM reading is within 1µV of V(100t).

Calculate in 6^{1/2} digits resolution

$$V3 \times C = \dots\dots\dots V$$

V(100t) is a transfer value

$$V(100t) = \dots\dots\dots mV$$

Stage 3

To Calibrate the 10mV Range Full Range Output

- a. Ensure that the DVM is still connected to the 4708 terminals as shown in Fig. 2.
- b. Ensure that the 4708 is set to the 100mV range.
Calculate the value '100mV x C'.
Set OUTPUT display to this value.
- c. Set the DVM to measure 10mV.
- d. Allow the output to settle.
Note the DVM reading as 'V(10t)'.
- e. Set 4708 to its 10mV range.
- f. Adjust the 4708 Output for a DVM reading of V(10t).
Press the 'Cal' pushbutton and observe the DVM reading.
- g. Repeat operation (f.) until the post-CAL DVM reading is within 1µV of V(10t).

Calculate in 6^{1/2} digits resolution

$$100mV \times C = \dots\dots\dots mV$$

V(10t) is a transfer value

$$V(10t) = \dots\dots\dots mV$$

Stage 4

To calibrate the 1mV Range Full Range Output

- a. Ensure that the DVM is still connected to the 4708 terminals as shown in Fig. 2.
- b. Ensure that the 4708 is set to the 10mV range.
Calculate the value '10mV x C'.
Set OUTPUT display to this value.
- c. Set the DVM to measure 1mV.
- d. Allow the output to settle.
Note the DVM reading as 'V(lt)'.
- e. Set 4708 to its 1mV range.
- f. Adjust the 4708 Output to give a settled DVM reading of V(lt).
Press the 'CAL' pushbutton and observe the DVM reading.
- g. Repeat operation (f.) until the post-CAL DVM reading is within 1μV of V(lt).

Calculate in 5^{1/2} digits resolution

| |
|---|
| $10\text{mV} \times C = \dots\dots\dots\text{mV}$ |
|---|

V(lt) is a transfer value

| |
|---|
| $V(\text{lt}) = \dots\dots\dots\text{mV}$ |
|---|

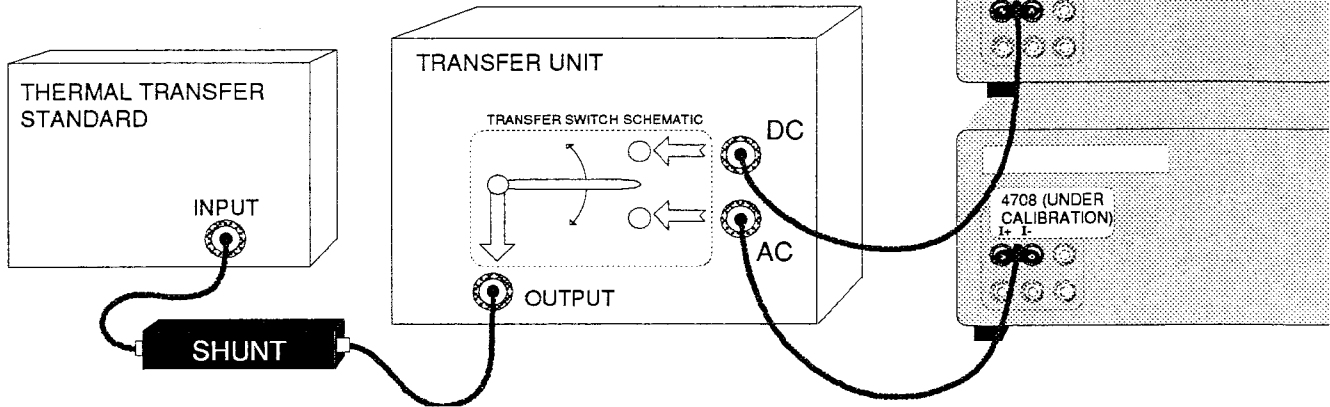
Stage 5

Calibration Disable

- a. Turn the Calibration security key, inserted in the 'CALIBRATION ENABLE' switch on the rear panel, to 'RUN'. Remove the key.

1.3.3 AC Current

AC CURRENT CALIBRATION (1mA - 1A) (Using Thermal Transfer, Current Shunts and DC Current Standard)



For all connections use low loss co-axial cable and keep leads as short as possible. Some types of shunt can be directly fitted to the Thermal Transfer.

Note

Calibrate 1mA Range only if the Thermal Transfer is adequately calibrated at these levels.

Routine

Commencing with the lowest Range, calibrate the 4708 at the calibration points in the table as part of the following routine:

1. Thermal Transfer Standard

Configure for DC measurement at the required developed voltage and connect with the appropriate shunt to the Transfer Unit.

2. DC Current Standard

- a. With OUTPUT OFF, connect to the Transfer Unit and set to the required calibration current.
- b. Set OUTPUT ON.

3. 4708

- a. With OUTPUT OFF, set to the required calibration Current and Frequency and connect to the Transfer Unit.
- b. Set OUTPUT ON.

4. Transfer Unit

Switch for DC output.

5. Thermal Transfer Standard

Adjust for null at the Calibration Current.
Configure for AC measurement at reduced sensitivity.

6. Transfer Unit

Switch for AC output.

7. Thermal Transfer & 4708

Use the OUTPUT keys to adjust the OUTPUT Display reading to obtain a null on the Thermal Transfer increasing the Transfer sensitivity as required.

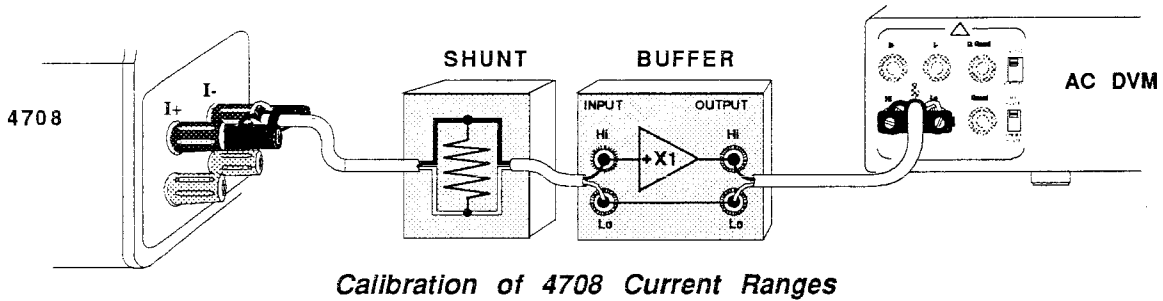
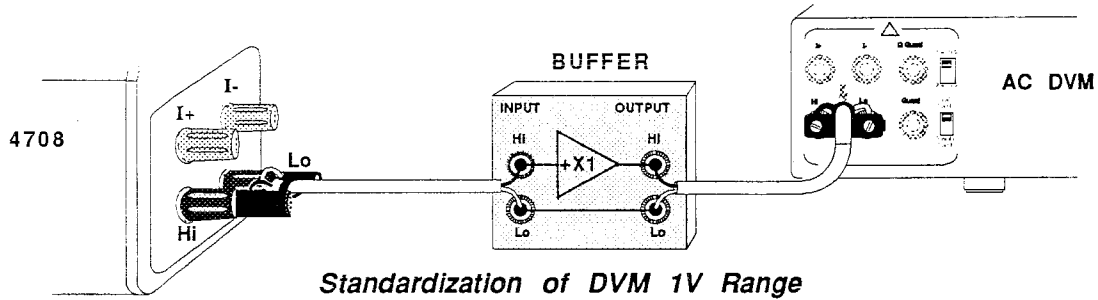
Execute the calibration by pressing the CAL key.

Nominal Cal. Points for 1mA to 1A Ranges.

| DC Standard OUTPUT Current | 4708 OUTPUT RANGE/ FREQUENCY | 4708 Nominal OUTPUT Current | Freq. Band set by 4708 |
|----------------------------|------------------------------|-----------------------------|------------------------|
| 1.000000mA | 1mA 300Hz | 1.000000mA | LF |
| 1.000000mA | 1mA 5kHz | 1.000000mA | HF |
| 10.000000mA | 10mA 300Hz | 10.000000mA | LF |
| 10.000000mA | 10mA 5kHz | 10.000000mA | HF |
| 100.000000mA | 100mA 300Hz | 100.000000mA | LF |
| 100.000000mA | 100mA 5kHz | 100.000000mA | HF |
| 1.000000A | 1A 300Hz | 1.000000A | LF |

CURRENT FULL RANGE CALIBRATION (100µA - 1A)

(Alternative Method using verified 4708 1V Range, Calibrated Standard AC Shunts and AC DVM).



100µA to 1A procedure

Commencing with the 100µA Range, calibrate the 4708 at the calibration points in the table as part of the following procedure:

1. 4708 and AC DVM

With OUTPUT OFF, connect the 4708 and DVM for Standardization. Select the 1V Range on the AC DVM.

2. 4708

- a. Set to the 1V Range at the Calibration Frequency and adjust for calibrated 1.000000V output.
- b. Set OUTPUT ON and note the DVM reading as 'V1'.
- c. Set OUTPUT OFF, and reconnect the test circuit for Calibration, using the correct shunt for the range to be calibrated.
- d. On I FUNCTION, select the required OUTPUT RANGE.
- e. Select the required FREQUENCY RANGE .
- f. Use FREQUENCY keys to display the required Calibration Frequency.
- g. Press the Full Range key.
- h. Set 4708 OUTPUT ON.
- j. Use the OUTPUT keys to adjust the OUTPUT Display reading to obtain a DVM reading of 'V1'.
- k. Execute the calibration by pressing the CAL key. Set OUTPUT OFF.

Calibration points for 100µA to 1A Ranges.

| 4708 OUTPUT RANGE/ FREQUENCY | 4708 Nominal OUTPUT Current | Freq. Band set by 4708 |
|---------------------------------------|--------------------------------------|---------------------------------|
| 100µA 300Hz | 100.0000µA | LF |
| 100µA 5kHz | 100.0000µA | HF |
| 1mA 300Hz | 1.000000mA | LF |
| 1mA 5kHz | 1.000000mA | HF |
| 10mA 300Hz | 10.00000mA | LF |
| 10mA 5kHz | 10.00000mA | HF |
| 100mA 300Hz | 100.0000mA | LF |
| 100mA 5kHz | 100.0000mA | HF |
| 1A 300Hz | 1.000000A | LF |

1.4 RESISTANCE CALIBRATION

(Measurement and Storage of the values of an internal resistor.)

Calibration Memory

In Ω function, each RANGE key selects a nominal-value standard resistor. Adjustment of the resistor value is not routinely necessary unless *Error 6* occurs during calibration (*refer to Section 4.4*). During calibration the actual value is measured and stored in the calibration memory to be displayed whenever that range is selected. Separate memory stores exist for Remote Sense (4-wire), Local Sense (2-wire) and Local Sense zero. Zero calibration is not available in Remote Sense.

4-wire Calibration Limits

The value measured in 4-wire Remote Sense does not include the resistance of internal or external wiring because of the measurement techniques used.

The instrument accepts any value within ± 200 ppm of nominal as a valid calibration.

2-wire Calibration Limits

The value measured in 2-wire Local Sense is greater than for 4-wire Remote Sense, as it includes the resistance of internal wiring and relay contacts. The instrument will not accept any 2-wire value less than the stored value for 4-wire, so the 4-wire Remote Sense calibration must be carried out before attempting 2-wire Local Sense. The extra internal resistance depends on range, so the instrument accepts the following values x as valid 2-wire calibrations:

Zero calibration.

10 Ω to 1M Ω Ranges: $0 \leq x < 0.9000\Omega$

Value calibrations.

10 Ω to 1M Ω Ranges: 4-wire value $\leq x < (4\text{-wire value} + 1.999\Omega)$

Error 6 appears on the MODE display for any attempt to enter a value outside the 4-wire or 2-wire limits.

Note:

When resistance is calibrated in Remote Sense, the instrument overwrites the Local Sense calibration memory with the new 4-wire value. For this reason 2-wire calibration should always be performed after 4-wire calibration.

General Procedure.

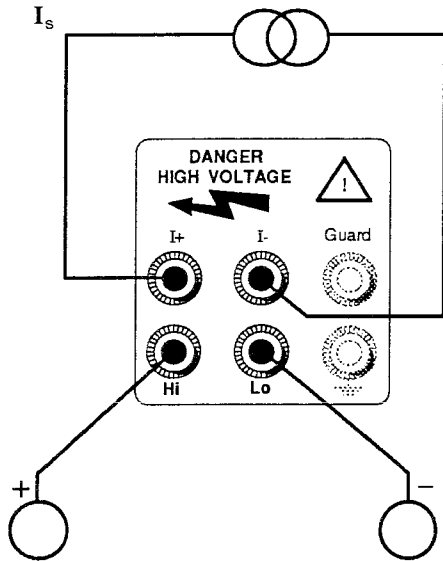
Prepare the 4708 for calibration. Connect as required and use the following calibration routines to calibrate the resistors in sequence, commencing with the 100M Ω Range.

Note

All measurements use 4-wire connections to exclude the effect of external lead resistance from the measured value.

4-WIRE RESISTANCE CALIBRATION

(Remote Sense selected)



CALIBRATION SEQUENCE

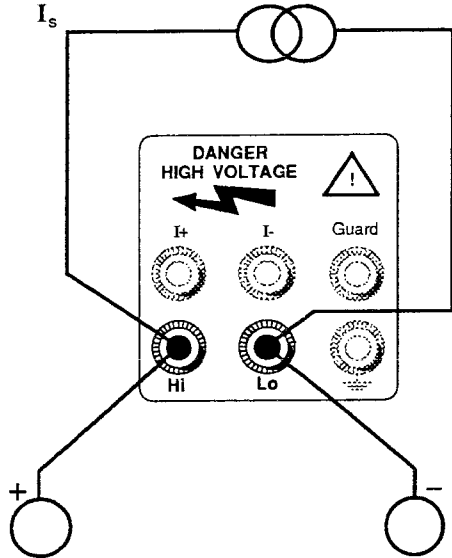
1. **4708**
Select **OUTPUT OFF** and Ω .
Select **Remote Sense**.
2. **4708**
Press required (**RANGE**) key; The previously-calibrated value appears on the **OUTPUT** display.
3. **4708 and resistance-measuring equipment**
Press **OUTPUT ON+** and measure the value of the internal resistor.
4. **4708**
Using the **OUTPUT** $\uparrow\downarrow$ keys, set the measured value on the **OUTPUT** display.
Press **CAL** Key to store **OUTPUT** display value.
Set **OUTPUT OFF**.
5. Repeat operations (2) to (4) for each **RANGE**.

Nominal Calibration Points and Limits for 4-wire calibration.

| Range | Measured Resistance | |
|---------------|----------------------|----------------------|
| | Minimum | Maximum |
| 100M Ω | 99.9800 1 M Ω | 100.01999 M Ω |
| 10M Ω | 9.99800 1 M Ω | 10.001999 M Ω |
| 1M Ω | .999800 1 M Ω | 1.0001999 M Ω |
| 100k Ω | 99.9800 1 k Ω | 100.01999 k Ω |
| 10k Ω | 9.99800 1 k Ω | 10.001999 k Ω |
| 1k Ω | .999800 1 k Ω | 1.0001999 k Ω |
| 100 Ω | 99.9800 1 Ω | 100.01999 Ω |
| 10 Ω | 9.99800 1 Ω | 10.001999 Ω |

2-WIRE RESISTANCE CALIBRATION

(Remote Sense OFF. Note: 2-wire calibration should always be performed after 4-wire calibration.)



CALIBRATION SEQUENCE

1. **4708**
Select OUTPUT OFF and Ω . **Deselect** Remote Sense.
2. **4708**
Press required resistor (RANGE) key; The previously-calibrated value appears on the OUTPUT display.
3. **4708 and resistance-measuring equipment**
Press OUTPUT ON+ and measure the value of the internal resistance.
4. **4708**
Using the OUTPUT \updownarrow keys set the **measured value** on the OUTPUT display.
Press CAL Key to store OUTPUT display value
5. **4708**
Press Zero Key and repeat operations (3) to (4) for this RANGE selection. Set OUTPUT OFF.
6. Repeat operations (2) to (5) for each RANGE value of the Table.

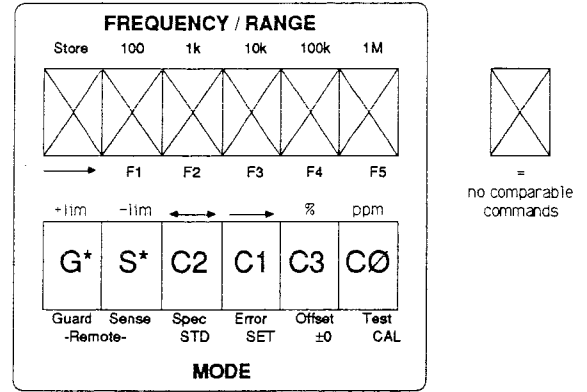
Nominal Calibration Points and Zero Limits for 2-wire calibration.

* The Local Limit Span: Lower Limit = Remote Value; Upper Limit = Remote Value + 'U' (digits).

| Range | *Local Limit Span 'U' (digits) | Measured Zero Limit | |
|---------------|--------------------------------|---------------------|--|
| 1M Ω | +19 | | |
| 100k Ω | +199 | | |
| 10k Ω | +199 | | |
| 1k Ω | +1999 | | |
| 100 Ω | +1999 | | |
| 10 Ω | +1999 | | |

1.5 REMOTE CALIBRATION GUIDELINES

The operation of the instrument in systems applications via the IEEE 488 interface, is described in Section 5 of the User's Handbook. In addition to its capability as a programmable calibrator, the 4708 can itself be calibrated under remote control. Full autocalibration of the instrument over the bus implies availability of a suitably programmed controller, programmable standards, programmable Null Detector, and a programmable Thermal Transfer.



Calibration Commands

The table below lists the device-dependant commands used for Routine Calibration. The relevant calibration codes are also listed.

These commands can only be activated when two conditions have been fulfilled:

- the CALIBRATION ENABLE Keyswitch on the instrument Rear Panel must be set to ENABLE, and
- the IEEE Interface command-code W1 must have been received and activated.

Additional commands can be activated when 'PRE-CAL ENABLE' switch is enabled. Refer to 1.6.3 Remote Pre-Calibration Guidelines.

Transfer of calibration facilities

When the 4708 is under remote control over the bus, the command-code W0 overrides the settings of the CALIBRATION ENABLE and internal PRE-CALIBRATION ENABLE switches, disabling the 'C' codes.

General Procedure

The Main Register is set to the Calibration Standard value (M***...), the 4708 Output is switched ON (01), and one or a specified sequence of the calibration mode command codes (C1, C2, C3, I) may be transmitted.

The 'M' Code is adjusted to obtain a null at the Calibration Standard value, and C0 is transmitted to execute the calibration.

Availability of Command Codes

| Command Codes (Key caps) | Description | Functions and Facilities | | | | | |
|-----------------------------|--|---|------------|-----------------|------------|---------------------------------|-----------------|
| | | DC Voltage | DC Current | AC Voltage | AC Current | 2-Wire Ω | 4-Wire Ω |
| C0 | Range Zero | 100mV-1000V Ranges | All Ranges | | | 10 Ω -1M Ω Ranges | |
| | Gain calibration to Nominal Full Range | 100mV-1000V Ranges | All Ranges | All Ranges | All Ranges | 10 Ω -1M Ω Ranges | All Ranges |
| *C1 (SET) | Zero offset for range at User's selected value | All Ranges | All Ranges | | | | |
| | Gain for range at User's selected value | All Ranges | All Ranges | All Ranges | All Ranges | | |
| *C2 (STD) | Internal Reference gain at user's Standard value | 1V & 10V Ranges | | 1V & 10V Ranges | | | |
| *C3 (± 0) | Alignment of internal ON+ and ON- zeros | 10V Range | | | | | |
| I | User's Message | Refer to User's Handbook Section 5 'Programming of Bus Transmissions' | | | | | |

*Preselector - must be activated later by command code C0 (CAL)

Command Code Facilities (Routine Calibration)

For a General description see 'Autocal Facilities' page 1-3.

C1 (SET)

C1 gives calibration at any point in the selected range by allowing the user to input the value of the calibration standard used (initial M code used). Before executing the calibration CØ uses the final 'M' Code value to distinguish between Zero (Offset calibration) and Full Range (gain calibration). The limits of Offset or Full Range depend on function selected (refer Sect 1.2 DC Calibration and Sect 1.3 AC Calibration).

C2 (STD)

C2 allows a user to compensate for changes of the internal Master Reference voltage. For best accuracy it is recommended this procedure is carried out in DC function. Note that the gain of all voltage and current ranges change in the same ratio. Execute with CØ

CØ (execute pre-selection)

CØ executes one of the above preselected AUTO-CAL modes.

CØ (CAL ONLY)

If Command CØ is sent without pre-selection code C1/C2 the instrument assumes that the selected range is to be calibrated at either Zero or Full Range. It uses the value input by the 'M' Code to distinguish between Zero (Offset calibration) and Full Range (gain calibration) according to the function selected (refer Sect 1.2 DC Calibration and Sect 1.3 AC Calibration).

Guidelines - An Example

The following sequence suggests a method of calibrating the instrument 1V Range Gain against a buffered standard cell value of +1.018057V. It is assumed that the instrument is correctly addressed with its Calibration Keyswitch set to ENABLE and the instrument Output is OFF. Connect the Null Detector, set to low sensitivity, between the Standard Cell buffer and the 4708. The nulling operation is seperated into its own string, as it is likely to be iterative.

SET Calibration of 1V DC Gain

FØR5GØSØW1M+1.018057C1Ø1=M(for null)CØ

The example suggests only the broad outline of one of many sequences which could be used to perform instrument calibrations.

Calibration Command Strings

The following AC command strings are given for the sole purpose of illustrating the methodology designed into the 4708 for remote calibration modes. Some reference to external operations is inferred. The nulling operation is seperated into its own string, as it is likely to be iterative.

It is assumed that the 4708 has previously been programmed in function and range (not autorange RØ) and that the external circuit is set up correctly. The 4708 is already programmed into its calibration mode by W1, with the calibration keyswitch set to ENABLE, and output OFF.

- a. Nominal Full Range LF Gain Calibration:
H(LF)A1Ø1=M(for null)=CØ=ØØ=
- b. Nominal Full Range HF Gain Calibration:
H(HF)A1Ø1=M(for null)=CØ=ØØ=
- c. Combined Nominal LF and HF Gain Cal:
H(LF)A1Ø1=M(for null)=CO=
H(HF)=M(for null)=CO=ØØ=
- d. Non-nominal LF Gain Calibration:
H(LF) M(20%-200%FR)C1=
Ø1=M(for null)=CØ=ØØ=
- e. Non-nominal HF Gain Calibration:
H(HF) M(20%-200%FR)C1=
Ø1=M(for null)=CO=ØØ=
- f. Combined Non-nominal LF and HF Gain Cal:
H(LF)M(20%-200%FR)C1=
Ø1=M(for null)=CØ=
H(HF)M(20%-200%FR)C1=
M(for null)=CØ=ØØ=
- g. Standardization at Nominal Full Range
1V or 10V Range only):
H(LF)A1C2Ø1=M(for null)=CØ=ØØ=
- h. Standardization at a Non-nominal value
(1V or 10V range only):
H(LF)M(20%-200%FR)C2=
Ø1=M(for null)=CØ=ØØ=

1.6 PRE-CALIBRATION

1.6.1 Introduction

In an initial calibration process at manufacture, certain 'PRE-CAL' parameters are established in a special calibration memory to define the overall linearity of the instrument, and to allow maximum routine calibration memory span for adjustments. For normal purposes, these factory defined pre-calibration parameters are valid for the life of the instrument, and subsequent Routine Calibration procedures are sufficient to maintain calibration.

Preparation for the pre-calibration operation includes removal of the Top Cover, to facilitate selection of pre-calibration mode and operation of the calibration memory clear push-button. DC and AC pre-calibration must then be completed followed by a Full Routine Recalibration. Thereafter all routine calibrations may be performed from the front panel or over the IEEE Interface without removing the covers.

Circumstances Calling for Pre-Calibration

The stored parameters are invalidated by replacement of certain critical parts of the instrument.

- The Lithium battery which powers the whole calibration memory when the instrument supply is switched off. This should be replaced at five-year intervals (*Refer to Section 4.3*).
- The Digital Assembly
- The Reference Divider Assembly
- Critical components in the Digital or Reference Divider, AC and Sine Source assemblies

A full list appears on flap of page 1-1. After replacement of any of these parts, new parameters must be stored in the pre-calibration memory, by procedures (in manual or remote control) detailed in this section.

EQUIPMENT REQUIREMENTS

DC

- A precision divider capable of dividing 20,000,000V to 10,000,000V to a ratio error of better than 0.1ppm between tapings. For example a Datron 4902/S precision divider or alternatively a Datron 4903 DC Calibration Unit.
- A DC 10V reference with an accuracy of better than 2ppm. Example: Datron Instruments 4000A or a bank of standard cells.

AC

- A precision voltmeter capable of 1V AC measurement with a stability between readings of better than ± 5 ppm. Example: Datron Instruments 1281
- An inductive voltage divider with ratios of $\times 1.0$ and $\times 0.1$ capable of dividing 10,000,00V to 1,000,000V to an accuracy better than 2ppm.
- An AC/DC Thermal Transfer Standard. Example: Holt Model 6B

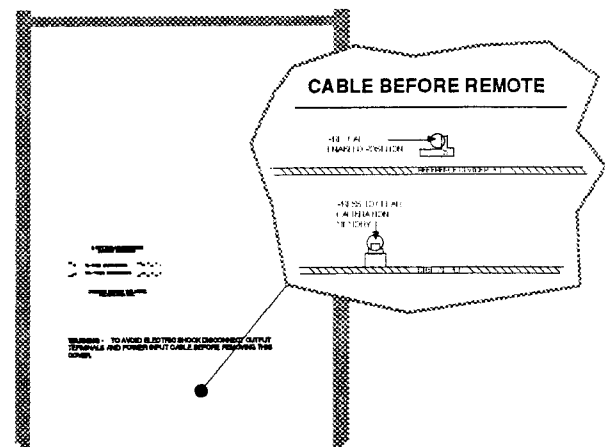
PREPARING THE 4708

Before clearing the pre-calibration store, prepare the 4708 as described on flap of page 1-2. The adjustments detailed in the following sequences include intentionally clearing the instrument's pre-calibration memory, which loses **all** previous calibration information. Therefore before proceeding make certain that the reasons for carrying out a complete recalibration are valid. (If in any doubt, consult your Datron Service Centre)

Identification of Access Holes

These give access to the 'PRE-CAL ENABLE' switch and the 'CLEAR CALIBRATION MEMORY' switch.

- a. Release 6 screws retaining the top cover.
- b. Lift the top cover at the front of the instrument and locate the two holes which give access to the two-position 'PRE-CAL ENABLE' switch and the press-button 'CLEAR



- c. Locate the hole which gives access to the PRE-CAL ENABLE switch. Insert an insulated tool in the hole and move the pre-cal switch to the right (Enable). The legend 'cal', as presented on the MODE display, also appears on the OUTPUT display.

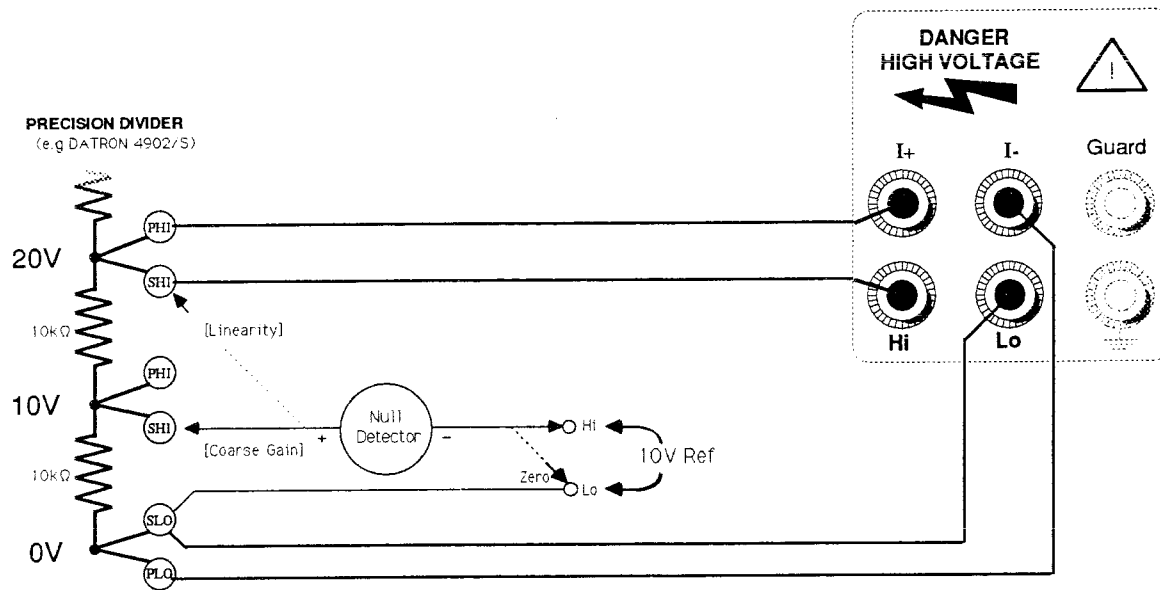
Caution

The following operation (d.) clears all the calibration memory stores as part of pre-calibration. Proceed only if this is required.

- d. Locate the hole which gives access to the Calibration Memory CLEAR push-button. Insert an insulated tool in the hole and press the button to clear the calibration memory.
- c. Refit the top cover but do not secure.

Complete the following pre-calibration procedure.

1.6.2 Procedure



First complete the ± 0 calibration procedure on page 1-7, but with precalibration mode selected.

Ensure the 4708 OUTPUT OFF LED is lit, cancel any MODE keys, select Remote Sense and deselect Remote Guard. Select DCV FUNCTION and 10V RANGE. Connect the Precision Divider to the instrument terminals as shown. Use short leads.

a. 4708

Ensure OUTPUT OFF and select the 10V RANGE.

b. Precision Divider/Null Detector

Set the Null Detector to Low sensitivity and connect to the Precision Divider at 10V tapping.

c. 4708

Connect to the precision divider as shown. Select +ON with zero OUTPUT

d. Reference/Null Detector

If the reference is a buffered bank of standard cells, switch the Buffer output to zero. However if an electronic reference is used connect Null Detector -ve lead to Reference Low.

Set Null Detector to high sensitivity. Zero Null Detector. Reduce Null Detector sensitivity.

Switch on or reconnect the 10V reference Hi to Null detector.

e. 4708

Select SET, its LED lights. Adjust the OUTPUT keys for Full Scale OUTPUT (+19.999999V).

Use instrument OUTPUT keys to adjust the Null Detector reading to zero.

Press CAL: the SET LED goes out.

f. Precision Divider/Null Detector

Increase Null Detector sensitivity. Reconfigure Null Detector Hi to divider 20V tapping.

g. Reference/Null Detector

If the reference is a buffered bank of standard cells, switch the Buffer output to zero. However if an electronic reference is used connect Null Detector -ve lead to Reference Low.

Set Null Detector to high sensitivity. Zero Null Detector. Reduce Null Detector sensitivity.

Switch on or reconnect the 10V reference Hi to Null detector.

h. 4708

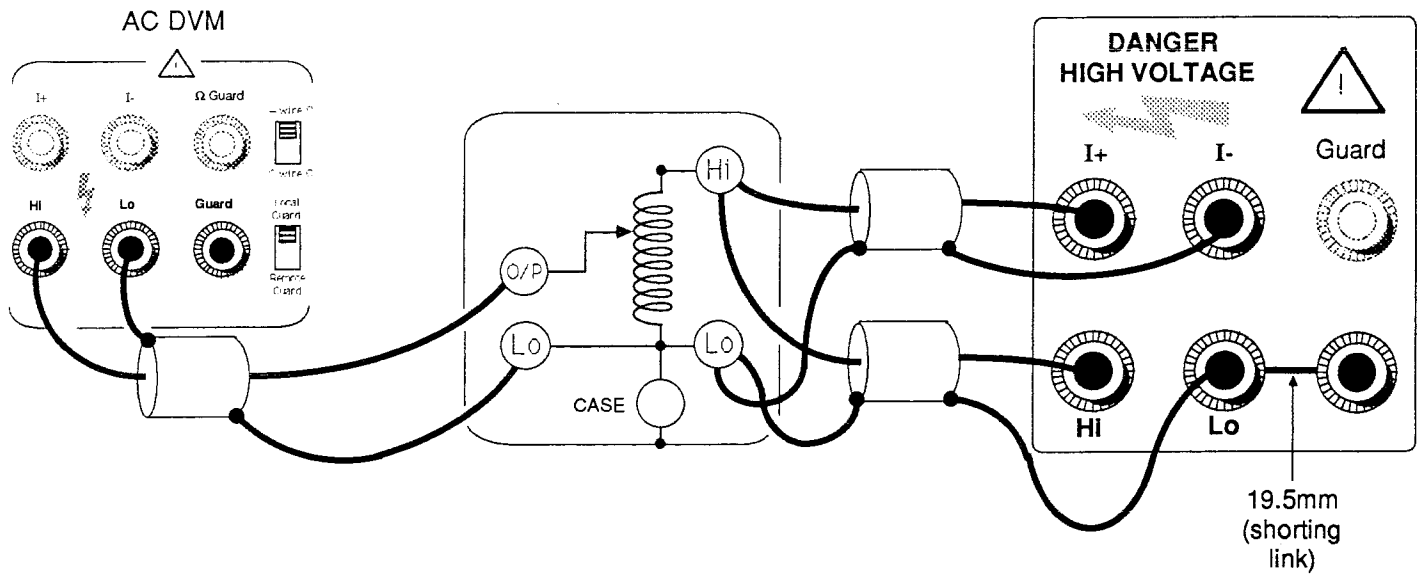
Select STD, its LED lights. Press +ON and Full Range OUTPUT (10.000000V).

j. Null Detector

Increase Null Detector sensitivity and use 4708 OUTPUT keys to adjust the reading to zero.

k. 4708

Press the CAL key: the STD LED goes OFF. Pre-cal is now completed. Select OUTPUT OFF and disconnect.



Ensure the 4708 OUTPUT OFF LED is lit, cancel any MODE keys, select Remote Sense and deselect Remote Guard. Select ACV FUNCTION and connect the IVD to the instrument terminals as shown. Use short leads. Select the 1kHz Frequency Range.

a. IVD

Select x1.0 ratio.

b. 4708

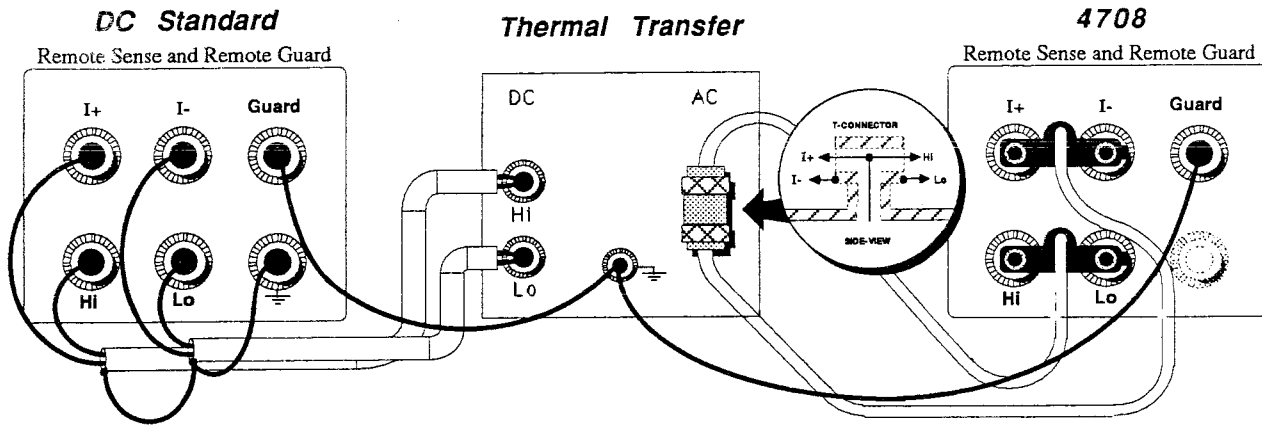
Select 10V range, at 1kHz on the 1kHz Frequency range. Select 1,000,00V. Press the ± 0 key, its LED lights. Use instrument OUTPUT keys to adjust the DVM reading to 1V. Press CAL: the ± 0 LED remains lit and 1,000,00V (nominal 10% Full Range) appears on the OUTPUT display.

c. IVD

Select the x0.1 ratio to divide the 4708 output by 10.

d. 4708

Select Full Range. Use instrument OUTPUT keys to adjust the DVM reading to 1V. Press the CAL key: the ± 0 LED goes OFF. Recheck, without pre-selection, at 1V and 10V. If required repeat the procedure. Select OUTPUT OFF and disconnect. Pre-cal is now completed. Disable pre-cal and complete a Full Routine Calibration.



- a. **4708 & DC Voltage Standard**
With OUTPUT OFF, connect to the Thermal Transfer AC and DC inputs, respectively.
- b. **4708**
On AC function, select the 10V range, select the 1MHz frequency range and use the FREQUENCY keys to display 1MHz. Use the OUTPUT keys to output 1V and set OUTPUT ON. Press the SPOT / ± key.
- c. **DC Voltage Standard**
Set to 1V output and set OUTPUT ON.
- d. **Thermal Transfer Standard**
Configure for DCV measurement at the 1V level and adjust for Null. Configure for ACV measurement at the 1V level.
- e. **4708**
Use the OUTPUT keys to adjust the OUTPUT display reading to obtain a null on the Thermal Transfer Standard. Press the CAL key.
- f. **DC Voltage Standard**
Set to 10V Output, select Output on.
- g. **Thermal Transfer Standard**
Configure for DCV measurement at the 10V level and adjust for Null. Configure for ACV measurement at the 10V level.
- h. **4708**
Press Full range key to display 10V and use the OUTPUT keys to obtain a null on the Thermal Transfer. Press the CAL key.

PRE-CAL DISABLE

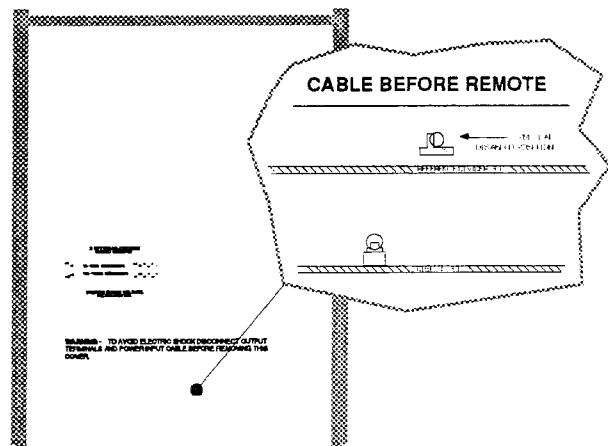
When pre-calibration is complete the pre-cal enable switch must be set to RUN.

Caution

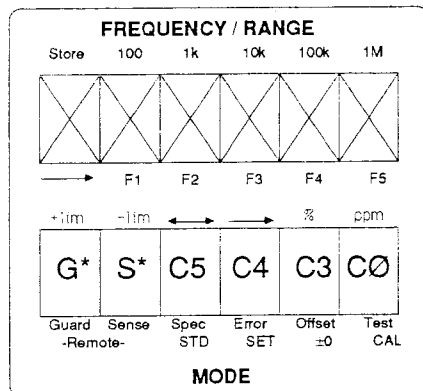
DO NOT press the internal push-button which clears the calibration memory. If this is done, any parameters stored in the calibration memory are cleared; so pre-calibration is cancelled, and must be repeated.

- a. Lift the top cover at the front.
- b. Locate the hole which gives access to the PRE-CAL ENABLE switch.
- c. Insert an insulated tool in the hole Pre-cal and move the switch to the left (RUN). The legend 'cal' remains on the MODE display, but disappears from the OUTPUT display.
- d. Refit and secure the top cover.

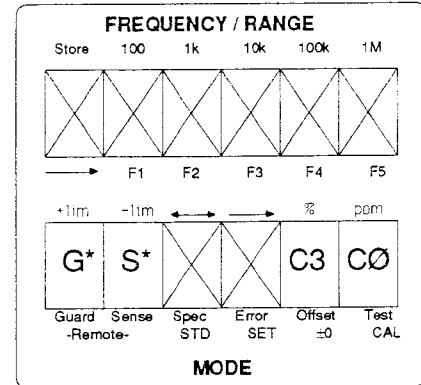
A Full Routine Calibration is necessary before completion of the Return to Use procedure on page of page 1-2.



1.6.3 REMOTE PRE-CALIBRATION GUIDELINES



Transfer of DC precalibration facilities



Transfer of AC precalibration facilities

General Procedure

The transfer of Pre-calibration facilities to remote control is illustrated above. The general procedure follows that for remote Routine Calibration; the external circuit is connected as for manual pre-calibration.

These commands can only be activated when the following conditions have been fulfilled:

- The CALIBRATION ENABLE Keyswitch on the instrument Rear Panel must be set to ENABLE
- Ensure that the IEEE address switch is set correctly
- The IEEE Interface command-code W1 must have been received and activated.
- The internal 'PRE-CAL ENABLE' switch is set to ENABLE.

When the 4708 is under remote control over the bus, the command code W0 overrides the setting of the CALIBRATION ENABLE and internal PRE-CAL ENABLE switches, disabling the 'C' codes.

Pre-Calibration Command Strings

The following command strings are given for the sole purpose of illustrating the methodology for the remote pre-calibration mode. Some reference to external operations is inferred. The nulling operation is separated into its own string, as it is likely to be iterative.

It is assumed that the external circuit is set up correctly.

The 4708 has already been programmed into its calibration mode by W1, with the calibration keyswitch and the internal PRE-CAL ENABLE switch set to ENABLE.

The calibration memory stores have been cleared, and the 4708 Output is OFF.

The string sequence for DC pre-calibration is as follows:

1) ±Zero

F0R6M+001C3= (Set-up and ±0 preselection)
M***= (Iterative nulling operation)
C0=M-0= ('CAL' and -ON)
M***= (Iterative nulling operation)
C0=00= ('CAL' then OUTPUT OFF)

2) Coarse Gain and Linearity

F0R6C4M+19.99999901= (Set-up and linearity preselection)
M***= (Iterative nulling operation)
C0=00= ('CAL' then OUTPUT OFF)
C5=M+10.00000001= (Set-up and linearity preselection)
M***= (Iterative nulling operation)
C0=00= ('CAL' then OUTPUT OFF)

The string sequence for AC pre-calibration is as follows:

Full Range and 1/10th Range Linearity for first LF, and then for HF

F1R6H***C301=M***= (Program to frequency and voltage)
M***= (Iterative nulling operation)
C0=M***= (First 'CAL' of two-part process)
M***= (Iterative nulling operation)
C0=00 (Second 'CAL' cancels preselected mode)

1.7 Ω OPTION INTERNAL ADJUSTMENT

The Autocal procedure for routine calibration of the 4708 resistance Function is described in Section 1.4.

The method of calibration is to measure the value of each standard resistor, and store the measured value in non-volatile calibration memory. Subsequently, each time a resistance RANGE is selected, the previously calibrated value is displayed.

If a standard resistor has been subjected to undue stress, its value may have moved outside its tolerance (signalled by an *Error 6* message during Routine Autocalibration). If the value is less than approx. 50ppm outside tolerance, it can be adjusted internally using a variable trimmer. For values out of tolerance in excess of 50ppm it is likely that the resistor has been over-stressed - consult your Datron Service Centre.

Manual Trimming Procedure

The following procedure is a supplement to Routine Autocalibration. It is necessary only when the 4-wire calibration of Section 1.4 has resulted in an '*Error 6*' message.

It can also be used when, for operational reasons, it is necessary to adjust a resistor to its nominal value. For this purpose a continuously-reading method of measurement is convenient.

- a. Release eight screws retaining the top cover.
- b. Lift the top cover at the front of the instrument and locate the 8 holes giving access for ' Ω OPTION ADJUSTMENT'.
- c. Insert an insulated screw driver tool in the hole for the range selected, and adjust the preset resistor (rotating clockwise increases the resistance value).
- d. Re-measure the 4-wire value and repeat operation (c.) until the desired value is obtained.
- e. Re-calibrate the range for 4-wire and 2-wire connections as detailed in Section 1.4.
- f. Repeat the manual trimming procedure above for all ranges as required.
- g. Finally refit and secure the top cover using the eight screws removed in (a.), above.

Appendix 1 - Notes on the Use of the Null Detector

The Null Detector is normally connected in series with the 4708 Hi lead. A high-impedance-input device should be chosen to reduce off-null currents due to differences in the outputs of the DC voltage source and the 4708. A battery-operated instrument is preferred to ensure adequate isolation. Some Null Detectors possess high input impedance only when their readings are on-scale, so care should be taken to ensure that drain currents from the DC Voltage source do not become excessive. This applies particularly if the DC source is a standard cell or a bank of cells. Six points are important:

1. The null detector should be connected to the 4708 (or 4708 load resistor) only when the 4708 OUTPUT OFF LED is lit. (with output OFF, the I+, I-, Hi and Lo terminals are at high impedance).
2. Always set the null detector to its lowest sensitivity before connecting up, and increase sensitivity only when the voltages output by the DC Voltage source and the 4708 are close in value.
3. Do not change polarity of the 4708 or DC Voltage source without first switching the 4708 OUTPUT OFF. Care must be taken to ensure that the correct polarity ON key is pressed, to avoid excessive voltages being connected across the null detector, particularly when checking the 4708 directly against a standard cell.
4. Most Null Detectors are equipped with a 'Self-zero' or 'Zero-check' facility. For maximum accuracy, the Null Detector range zero should be checked before each calibration nulling operation is performed. However, when gain-calibrating the 4708 Voltage and Current Ranges, the zero offset of the calibration voltage source is nullified by adjustment of the Null Detector zero control. This setting should not be altered until the corresponding Range gain has been calibrated.
5. **WARNING**
During performance checks and calibration a common mode voltage equal to the full range voltage is present at the Null Detector input terminals. On 1000V checks this voltage is potentially lethal, so **EXTREME CAUTION** must be observed when making adjustments to the null detector sensitivity.
6. **CAUTION**
The Null Detector used must be able to withstand voltages up to 1200V between its input terminals. Such voltages will be present during the time that the 4708 is ramping from zero to 1000V Full range after setting OUTPUT ON. Inadvertent disconnection of the Precision Divider terminals can transfer full output across the Null detector.

Appendix 2 - Calibration Source Zero Offsets

It is common practice to accept a small offset in the output of a voltage calibration standard, providing that the same offset is present at all output values, including zero.

A more difficult situation arises if there is a 'DC turnover offset' between the source's positive and negative output values. In this case, a difference in DC value will be observed when switching the source between its positive and negative outputs with zero volts selected. This type of error is normally adjusted out on the 4708 by a preliminary ' ± 0 ' calibration on the 10V Range, to a null detected across its output terminals. This sets both ON+ and ON- zeros to the same DC level; and as the same linear analog circuitry is used to generate both output polarities, range calibration of zero and gain in positive polarity is then all that is required.

The 4708 analog circuitry is fully floating, so its output may be referred to any common mode voltage within the range specified on page 6.1 of the User's Handbook. In particular, each Range zero may be aligned to absolute zero in Local Sense by calibration to a null across its Hi and Lo (Sense) terminals. But if it is then gain-calibrated against an offset source without re-zeroing to that source's offset zero, normal mode gain errors will result. It is therefore essential that any offset in the source's output be nullified before gain calibration is carried out. This can be done at Range zero, simply by trimming the Null Detector null.

Thus the notional sequence of calibration for the 4708 should be as follows:

- a. ± 0
Check that the 10V Range 'ON+' and 'ON-' zeros coincide at absolute zero (Adjust if necessary).
- b. **Range Zeros**
Carry out 'ON+' zero calibration on all Ranges against the same absolute zero.
- c. **Range Gain**
Each Range Gain in turn. (Null Detector connections as shown for Voltage or Current)
 - i. At 'ON+' zero output from both source and 4708, trim the Null Detector for null.
 - ii. At the required positive DC level, calibrate the 4708 Range gain.

This sequence ensures that the 4708 'ON+' and 'ON-' zeros are both set to absolute zero, and that both positive and negative polarities are accurately gain-calibrated to a unipolar source. If it is required to check the 4708 'ON-' gain calibrations against a bipolar source, the source's 'ON-' zero offset must first be nullified, as described in c. i. above.

SECTION 2

FAULT DIAGNOSIS

WARNING
HAZARDOUS ELECTRICAL POTENTIALS ARE EXPOSED WHEN THE INSTRUMENT COVERS ARE REMOVED.
ELECTRIC SHOCK CAN KILL

CAUTION
The instrument warranty can be invalidated if damage is caused by unauthorised repairs or modifications. Check the warranty detailed in the "Terms and Conditions of Sale". It appears on the invoice for your instrument.

2.1 INTRODUCTION

2.1.1 Use of Diagnostic Guides

The diagnostic guides given in Section 2.2 are intended to aid the user in locating a failed printed circuit board or other assembly. The self-diagnostic capabilities of the instrument provide the first step in fault analysis by displaying a FAIL message on the mode display. Initial actions to be taken after the occurrence of a FAIL message are given, where applicable, in the diagnostic guides of Section 2.2. The FAIL message localizes the failure into a distinct functional area and the "Fault Condition" summary in each guide relates the function failure to a probable hardware boundary.

The identities of the assemblies involved in the failure are given beneath the fault condition summary, but it is unlikely that all assemblies listed will prove to be faulty. For successful failure analysis, it is advisable to be familiar with the electronic functioning of the instrument and with the physical location of the assemblies. To assist in these aspects, the diagnostic guides include references to relevant parts of this publication.

2.1.2 Effects of Protective Measures on Diagnosis

2.1.2.1 Protective Suppression of Fault Conditions

The 4708 incorporates built-in protection in hardware and software. To minimize damage, protective circuitry acts immediately, backed up by a pre-programmed CPU response to detected failure symptoms. If possible the CPU informs the user by presenting a failure message on the MODE display.

When investigating a failure, it should therefore be anticipated that protective measures will have suppressed the original fault conditions. A useful starting-point is to identify the origin of the failure message to localize the area of search.

2.1.2.2 FAIL 5 as Default State

Faults which result in display messages FAIL 2, 3 or 4 can pose a safety hazard to the operator, and apply excessive voltage to external circuitry. To protect against this, the instrument is programmed to default to FAIL 5 state as rapidly as possible after its initial response to the failure symptoms. The CPU switches Output OFF and trips the safety monitor (Watchdog). If the conditions of the original failure message have been removed the display changes to FAIL 5.

In normal use, an operator will probably notice only FAIL 5, and miss the original failure message. In FAIL 5 state, front panel control is inhibited until Safety Reset is pressed. This returns the instrument to the state for which the original fault conditions and failure message were produced, but with Output OFF.

2.1.2.3 To Observe the Original Failure Message

Two procedures can be used:

- a. Carry out the self-test routine of Section 2.3.
The failure message may recur during this test.
- b. Reset the instrument to reproduce the fault, carefully watching the MODE display.
The original failure message could reappear momentarily, prior to defaulting into FAIL 5.

Then select the appropriate diagnostic guide in Section 2.2.

2.1.3 FAIL 6

FAIL 6 reports two types of NV RAM failure.

- a. Overall sumcheck failure.
The values are calculated at Power on, Self-Test and recovery from FAIL). If the instruments stored calibration constants are outside maximum or minimum permissible values a Fail 6 message is displayed.
- b. Limits check of the calibration constants.
Values are checked when read from the NV RAM at every OUTPUT change. When a Fail 6 occurs the output remains on and the stored gain or zero correction value is defaulted to x1 or x0 respectively.

2.2 DIAGNOSTIC GUIDES

2.2.1 FAIL 1 (Excessive Internal Temperature)

INITIAL ACTION

1. Wait approximately 1 minute until the CPU has defaulted the instrument to OUTPUT OFF. The CPU clears the FAIL 1 message and enables the keyboard.
2. Switch OUTPUT ON.
3. No failure display - no further action. FAIL 1 recurs - fault persists.

FAULT CONDITION

High temperature sensed in:

- Positive Heatsink Assembly, or
- Negative Heatsink Assembly.

Fault indication signal OVERTEMP active.

POSSIBLE FAULT LOCATIONS

- Positive Heatsink Assembly (*page 11.13-1*).
- Negative Heatsink Assembly (*page 11.13-2*).
- Power Amplifier Assembly (*page 11.9-1*).

FURTHER INFORMATION IN THIS HANDBOOK

Technical Descriptions: *Section 7.12.9*.

2.2.2 FAIL 2 (Over-Voltage)

INITIAL ACTION

1. Ensure that OUTPUT is OFF (4708 should have tripped to FAIL 5).
2. Power OFF any external voltage source.

N.B.

This failure can be caused by injection of an external voltage across the terminals OR the output of high voltage when not requested by the user.

DC - voltages in excess of 130V.

AC - voltages between the limits of 75V to 110V RMS.

2. Disconnect external leads from the terminals.
3. Press Safety Reset.
4. Carry out self-test sequence.
5. FAIL 2 recurs - fault persists.
6. No failure display - Reproduce original conditions in Local Sense with no external connections.
7. No failure display - check external circuit and proceed with careful use.
8. FAIL 2 recurs - fault persists.

FAULT CONDITION

1. Over voltage circuit on the DC Assembly has detected the excess voltage between PHi and PLo lines and has activated HV ST signal to the CPU, and
2. The CPU has recognized that the instrument is not in High Voltage State, so has generated FAIL 2 display, then
3. The CPU has switched Output OFF, tripped the watchdog and generated FAIL 5 display.

POSSIBLE FAULT LOCATIONS

- Injection of external voltage.
- D.C Assembly (*page 11.5-1*).
- Power Amplifier Assembly (*page 11.9-1*).

FURTHER INFORMATION IN THIS HANDBOOK

Self-test procedure: *Section 2.3*.

Technical descriptions: *Section 7.3.7*.

2.2.3 FAIL 3 (Control Data Corrupted)

INITIAL ACTION

No immediate action required.

FAULT CONDITION

1. Control data corrupted.
2. CPU has detected errors in serial transfer of data between out-guard and in-guard circuits, and generated FAIL 3 display, then
3. The CPU has switched Output OFF, tripped the watchdog and generated FAIL 5 display.

POSSIBLE FAULT LOCATIONS

- Reference Divider Assembly (*page 11.4-1*).
- Analog Interface Assembly (*page 11.3-1*).

FURTHER INFORMATION IN THIS HANDBOOK

Technical descriptions: *Section 6.4*.

2.2.4 FAIL 4 (Precision Divider Fault)

INITIAL ACTION

No immediate action required.

FAULT CONDITION

1. Precision divider fault.
2. CPU has detected errors in the most-significant data bits set in the precision divider input data latches, and generated FAIL 4 display, then
3. The CPU has switched Output OFF, tripped the watchdog and generated FAIL 5 display.

POSSIBLE FAULT LOCATION

- Analog Interface Assembly (*page 11.3-1*).

FURTHER INFORMATION IN THIS HANDBOOK

Technical description: *Section 6.5.2.3*.

2.2.5 **FAIL 5** (Safety Circuits 'Watchdog' Tripped)

INITIAL ACTION

Use the checking sequence below, watching the MODE display carefully at each stage to detect any FAIL number appearing immediately before FAIL 5. If no failure message occurs, carry on to the next stage.

- Stage 1: Press Safety Reset.
- Stage 2: Carry out self-test sequence (Section 2.3).
- Stage 3: Set Output ON.
- Stage 4: Proceed with careful use.

If FAIL 2 occurs at stage 3, ensure that it is not due to injection of an excessive external voltage by disconnecting the instrument terminals and repeating the checks. If FAIL 5 alone occurs, proceed to "Fault Condition" below. For any FAIL other than FAIL 5, transfer to the diagnostic guide for that message.

FAULT CONDITION

18mS monostable (M10 in reference divider) has been deprived of at least two trigger pulses and has timed out, activating "BARK" and "BARK DELAYED" (BARK +47mS) signals from M13 in the reference divider assembly.

Summary of "BARK" effects:

1. Removes the drive from the High Voltage (1kV) transformer.
2. Disables the 400V Power Supply.
3. BARK status message sent to CPU signalling a failure.
4. CPU starts controlled shut-down.

Summary of "BARK DELAYED" effects:

1. Disconnects the voltage Power and Sense circuits from the instrument output terminals.
2. BARK DELAYED disables the registers of the serial/parallel data converters.
3. Outputs from control latches in the reference divider pcb are disabled by setting into "Tristate". Each output line has a pull-up or pull-down resistor which sets the analog circuitry into a safe condition.

POSSIBLE FAULT LOCATIONS

- Digital Assembly (No gated WRT STRB pulses at J2/J3-29) (*page 11.2-1*).
- Analog Interface Assembly (No SEDA strobe pulses; or Watchdog disabled) (*page 11.3-1*).
- Reference Divider Assembly (Incorrect functioning of Watchdog setup circuitry) (*page 11.4-1*).

NB.

The Watchdog is designed primarily to ensure that CPU malfunctions do not set up dangerous conditions in the analog circuitry.

FURTHER INFORMATION IN THIS HANDBOOK

Technical description: *Section 6.4*.

2.2.6 FAIL 6 (Calibration Memory Fault)

INITIAL ACTION

1. Select Output OFF, Spec OFF, Error OFF.
2. Perform self-test sequence (Section 2.3) or select Output ON at the requested value.
3. No failure display - no further action.
4. FAIL 6 recurs - recalibration required.
5. Select Cal (*refer to Section 1*).
6. Recalibrate (*refer to Section 1*).
7. Calibration failure - fault persists.

FAULT CONDITION

Calibration memory fault on Digital pcb assembly.

POSSIBLE FAULT LOCATION

- Digital Assembly (*page 11.2-1*)

FURTHER INFORMATION IN THIS HANDBOOK

Self-test procedures: *Section 2.3*.

Calibration procedures: *Section 1*.

Technical descriptions: *Section 6.1*.

2.2.7 FAIL 7 (P.A. 400V Power Failure)

INITIAL ACTION

1. Switch power OFF.
2. Check line supply is correct for input voltage setting.
3. Switch power ON - no failure display - no further action.
4. FAIL 7 recurs - fault persists.

FAULT CONDITION

- Positive or Negative 400V power supply failure
- Fault indication signal 400V(2) FAIL active
- Check line input voltage

POSSIBLE FAULT LOCATIONS

- Power Amplifier Assembly (*page 11.9-1*).
- Reference Divider Assembly (*page 11.4-1*).
- Positive Heatsink Assembly (*page 11.13-1*).
- Negative Heatsink Assembly (*page 11.13-2*).
- Power Supply/I Heatsink Assembly (*page 11.13-3*).
- Mother Board (*page 11.16-1*).

FURTHER INFORMATION IN THIS HANDBOOK

Technical descriptions: *Sections 6.7*.

2.2.8 **FAIL 8** (P.A.38V Power Failure)

INITIAL ACTION

1. Switch power OFF.
2. Check line supply is correct for input voltage setting.
3. Switch power on - no failure display - no further action.
4. FAIL 8 recurs - fault persists.

FAULT CONDITION

- Positive or Negative 38V power supply failure.
- Fault indication signal 38V(2) FAIL active.
- Check line input voltage.
- It is possible for a misleading FAIL 8 message to occur, caused by a logic supply failure, in particular -15 Volts. The FAIL 9 message will have been displayed momentarily. Refer for fault location and further information to FAIL 9.

POSSIBLE FAULT LOCATIONS

- Power Amplifier Assembly (*page 11.9-1*).
- Reference Divider Assembly (*page 11.4-1*).
- Power Supplies (*page 11.12-1*).
- Mother Board (*page 11.16-1*).

FURTHER INFORMATION IN THIS HANDBOOK

Technical descriptions: *Section 6.7*.

2.2.9 **FAIL 9** (P.A. 15V Power Failure)

INITIAL ACTION

1. Switch power OFF.
2. Check line supply is correct for input voltage setting.
3. Switch power on - no failure display - no further action.
4. FAIL 9 recurs - fault persists.

FAULT CONDITION

- Positive or Negative 15V power supply failure. This is indicated by a transitory Fail 9 followed by Fail 8.
- Fault indication signal 15V(2) FAIL active.
- Also 400V power supply is disabled.
- Check line input voltage.

POSSIBLE FAULT LOCATIONS

- Power Amplifier Assembly (*page 11.9-1*).
- Reference Divider Assembly (*page 11.4-1*).
- Power Supplies (*page 11.11-1*).

FURTHER INFORMATION IN THIS HANDBOOK

Technical descriptions: *Section 6.7*.

2.2.10 Error EF
(External Frequency selected but not detected)

INITIAL ACTION

- If External Frequency Lock is not required:
Ensure external frequency selection switch (S53) is set to **OFF**.
- If External Frequency Lock reference is required:
 1. Ensure reference frequency is available at Rear Panel connector J53.
 2. Ensure Rear Panel switch S53 is set to **ON**.

FAULT CONDITION

- The external reference signal detector has set 'EXT REF ST' to Logic \emptyset .

POSSIBLE FAULT LOCATIONS

- External circuit.
- Interconnection Assembly (*page 11.17-2*).
- Mother Assembly (*page 11.16-4*).
- Analog Interface Assembly (*page 11.3-4*).

FURTHER INFORMATION IN THIS HANDBOOK

Technical descriptions:
External Frequency Lock: Section 8.3.

2.2.11 Error OL (Voltage: Output current limit exceeded)
(Current: Output compliance voltage limit exceeded)

INITIAL ACTION

- If Voltage range selected:
 1. Set Output OFF (Automatic if 100 or 1000V range selected).
 2. Disconnect external circuit.
 3. Set Output ON:
 - If no Error OL or FAIL message, check external circuit for low resistance, drawing output current in excess of specification (refer to User's Handbook *Section 6*). Ensure Capacitive Load constraints are not exceeded, *page 6.7*.
 - If Error OL recurs, internal fault persists.

- If I range selected:
 1. Set Output OFF.
 2. Short Output terminals I+ to I-.
 3. Set Output ON:
 - If no Error OL or FAIL message, check external circuit for high resistance, developing output voltage in excess of compliance limit.
 - If Error OL recurs, internal fault persists.

FAULT CONDITION (IN DC RANGES)

- If Low DC Voltage range (100 μ V -10V):
DC Overcurrent Detector circuit (*Vol 2 page 11.5-2*) has detected a current in the PLO(DCV) line of approx 28mA or more, and has activated LIM ST signal to the CPU.

- If High Voltage range (100V or 1000V): Either
 - a. DC Overcurrent Detector circuit (*Vol 2 page 11.5-2*) has detected excessive current in the PLO(DCV) line and has activated LIM DET signal to the CPU, or
 - b. DC 1000V Over-Voltage detector (*Vol 2 page 11.14-2*) has detected an output voltage in excess of 1440V and has activated LIM DET signal to the CPU.

In either condition **a.** or **b.**, M10 in the power amplifier removes the 16kHz drive from the input to the PA, and generates HI I ST signal to the CPU; which responds by setting Output OFF, and DC Reference voltage to zero.

- If I range selected:
Overvoltage detector circuit (M15 in I/ohms Assembly) has detected a terminal voltage of 4.4V or more and has activated LIM ST signal to the CPU. If 100mA or 1A range selected, the CPU switched Output OFF and reduces DC Reference voltage to zero.

FAULT CONDITION IN AC RANGES

- If 1mV, 10mV, 100mV or 1V Range:
Sine Source Assembly overcurrent sense circuit (M49a/M49b) has detected a current in the AC 1V line of approximately 25mA RMS or more, and has activated LIM ST signal to the CPU.

- If 10V range:
10V overload detector in the Power Amplifier Assembly has detected a current in the I+ line of approximately 60mA RMS or more. In this condition a hardware limit comes into effect.

- If High Voltage ranges (100V or 1kV): Either
 - a. 100V Overload detector in the Power Amplifier Assembly has detected a load in excess of 120mA RMS on the 400V power supply,
 - b. 1kV Current Overload detector (M8) in the Output Control assembly has detected an excessive output current, or
 - c. 1k Overvoltage Detector in the Output Control Assembly has detected a voltage on the PHI(V) line in excess of 1440V RMS.

In these ranges the output is switched off automatically by the CPU.

- If I range selected:
Overvoltage detector circuit has detected a terminal voltage of 3V RMS or more and has activated LIM ST signal to the CPU. If 100mA or 1A range selected, the CPU switched Output OFF.

POSSIBLE FAULT LOCATIONS

- External circuit.
- Sine Source Assembly (*page 11.6-1*).
- AC Assembly (*page 11.7-1*).
- DC Assembly (*page 11.5-1*).
- Power Amplifier Assembly (*page 11.9-1*).
- I/Ohms Assembly (*page 11.8-1*).

FURTHER INFORMATION IN THIS HANDBOOK

Technical descriptions:
Low DC Voltage ranges: Section 7.3 and 7.6.
Low AC Voltage ranges: Section 9.4.
100 or 1000V ranges: Section 9.5.
I ranges: Section 10.

2.3 SELF-TEST SEQUENCE

2.3.1 General

The self-test sequence is performed in two stages:

Stage 1 is a fully automated test of safety monitoring and high-voltage safety interlocks;

Stage 2 is a semi-automatic test of keyboard and display functions, which also responds to operator's key selections.

2.3.2 Stage 1 (Fig. 2.1)

Entry into Stage 1 is selected automatically whenever the TEST key is pressed for the first time (the test is not allowed if OUTPUT ON, ERROR or SPEC are selected or when in remote control). Indication of test mode is given by the LED in the TEST key being lit. The full sequence of Stage 1 must be completed before exit from the test mode can be made. The tests performed in Stage 1 are as follows:

1. Safety Monitor Watchdog Test. In this, the safety monitor is tripped causing the word SAFETy to appear in the Mode display, the Safety Reset LED flashes and the buzzer sounds continuously. It is necessary for the operator to reset the safety monitor by pressing the Safety Reset key, after which the SAFETy display is replaced by the 'running' message, and the test sequence continues.
2. Calibration Memory Test. The contents of the non-volatile calibration RAM are checked for validity. Failure results in the message FAIL 6 appearing on the Mode display.
3. High-voltage Protection. This test ensures that a voltage demand made to the power amplifier does not trip the software voltage detector when immediately below the detector threshold level, but when raised to a level above the detector threshold the detector is tripped.

Incorrect detect action is shown by the message FAIL 2 on the Mode display. No voltages appear at the output terminals during this test.

Fail messages are updated as the test sequence progresses through the calibration memory and high-voltage tests. After completion of the high-voltage test, the test mode ends and the Test LED is cancelled. If faults were encountered the last FAIL message will remain on the display replacing the running message. Fault diagnosis can now be performed. If no faults are encountered during Stage 1, the message PASS is displayed. The calibrator can now be returned to normal operation, or Stage 2 of the self-test sequence can be selected.

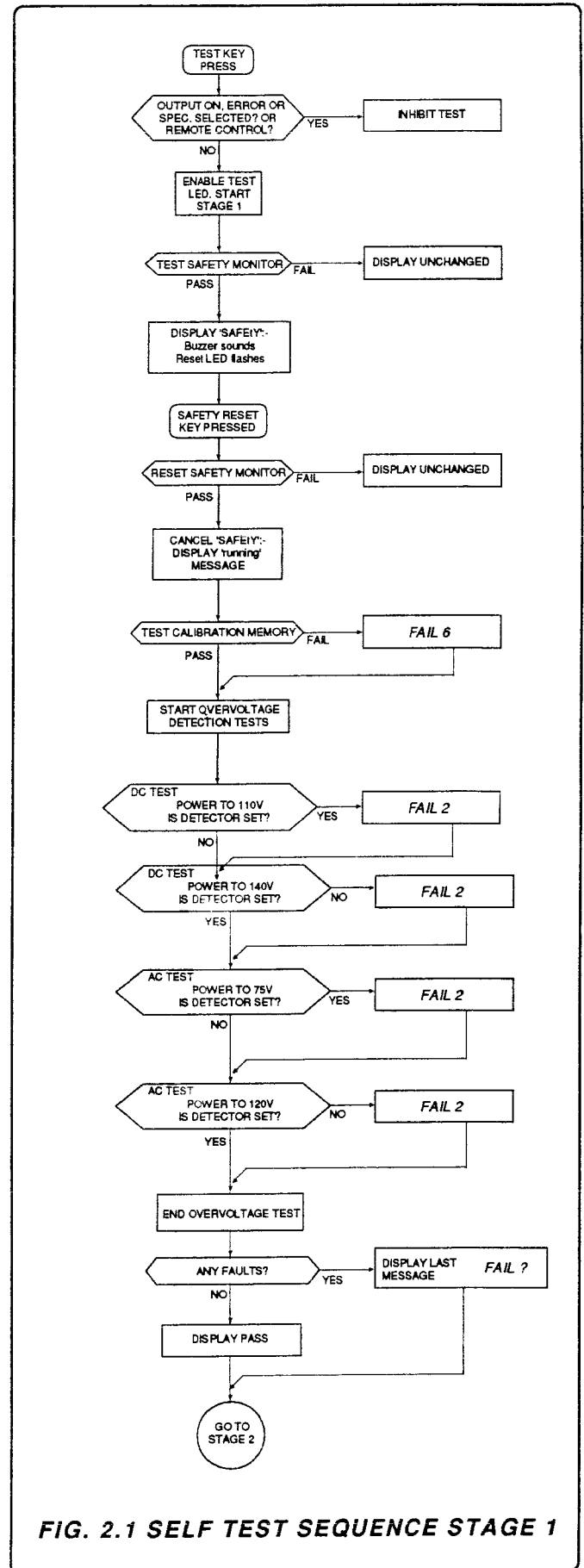


FIG. 2.1 SELF TEST SEQUENCE STAGE 1

2.3.3 Stage 2 (Fig. 2.2)

Entry into Stage 2 of the self-test sequence is made when the Test key is pressed AFTER the completion of Stage 1. and BEFORE any other key.

The test proceeds by sequentially displaying all segments and legends.

The test continues, showing segment-by-segment, all seven-segment digits, legends and commas.

After all digits have been displayed, the keyboard LED indicators are lit in a sequence which proceeds from left to right. (Test LED remains lit).

The next test in the sequence requires operator participation in order to check key functions. Two half-digit symbols are shown on the mode display to indicate that the keys are ready to be checked.

Operation of Up, Down and Output Selection keys are shown by a symbol on the display immediately above the key; operation of Frequency Range, Mode, Range, Function and Output keys are shown by the key's LED. In these tests the display or LED remains lit until another key is pressed.

At any part of Stage 2, pressing Test or Zero key will end the test and cancel the Test LED.

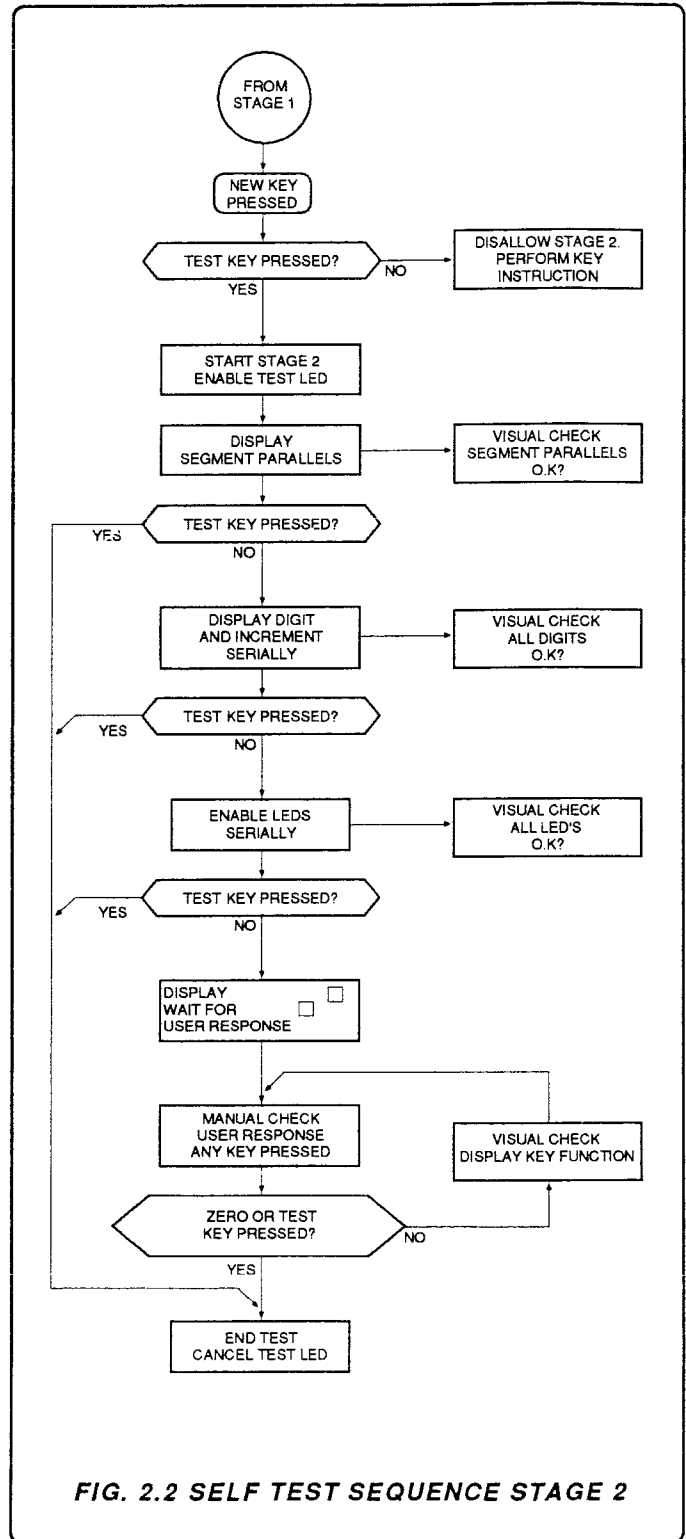


FIG. 2.2 SELF TEST SEQUENCE STAGE 2

2.4 FUSE PROTECTION

In addition to the electronic protection devices used in the instrument, fuses are provided to protect against catastrophic component failure.

2.4.1 Fuse Replacement

A blown fuse is merely a symptom of failure, in the large majority of cases the cause lies elsewhere.

CAUTION

Every occurrence of a blown fuse should be investigated to find the cause. Only when satisfied that the cause is known, and has been removed, should a user replace a fused link by a serviceable item.

2.4.2 Reasons For Fusing

The fuses in the calibrator fall into two groups:

- a. Clip-in anti-surge fuses in the Power Supplies and Mother Board protect the power source from damage.
- b. Soldered-in fuses are used in some locations to ensure that the printed circuit tracks are protected in the unlikely event of extreme failure conditions.

2.4.3 Locating a Blown Fuse

The ultimate causes of blown fuses are so extensive that it is impractical to list them. In many cases the underlying cause, or the blown fuse itself, will activate an electronic protective process which can conceal some of the symptoms.

Fault location in the Calibrator should proceed from the primary indications of fault condition (e.g. failure messages described in Section 2.2). These will lead to particular areas of investigation, and at this point the relevant circuit fuses should be checked first. Whether fuses are blown or not, the checks will add to the information available for further diagnosis. Table 2.1 is indexed in Circuit Diagram page order, giving fuse values. The types of fuses to be used can be found in the component lists of Section 12.

Table 2.1 (overleaf) lists their locations.

| LOCATION AND DESIGNATOR | VALUE/FITTING | PROTECTED CIRCUITS | Page |
|---------------------------|-----------------|---|---------|
| DC Assembly | | | |
| F1 | 1A/Solder-in | DC 10V, 100V & 1kV Error | 11.5-1 |
| F2 | 250mA/Solder-in | SHI(DCV) | 11.5-2 |
| F3 | 1A/Solder-in | Power Lo/Guard | 11.5-2 |
| F4 | 1A/Solder-in | Power Lo | 11.5-2 |
| F5 | 1A/Solder-in | DC 1kV | 11.5-1 |
| F6 | 1A/Solder-in | PHI(V) | 11.5-2 |
| AC Assembly | | | |
| F1 | 1A/Solder-in | 1V range only & Current ranges up to 10mA | 11.7-1 |
| F2 | 1A/Solder-in | All AC Voltage ranges (PHI(ACV)) | 11.7-1 |
| I/Ω Assembly | | | |
| F1 Not used | --- | --- | --- |
| F2 | 375mA/Solder-in | PLO(Ohms) | 11.8-3 |
| F3 | 1A/Solder-in | SLO(Ohms) | 11.8-3 |
| F4 | 375mA/Solder-in | PHI(Ohms) | 11.8-3 |
| F5 | 2.5A/Solder-in | All Current/Ohms Outputs | 11.8-1 |
| Power Supply (OG) | | | |
| F1 | 4A/Clip-in | Digital and Display supplies | 11.10-1 |
| Power Supply (IG) | | | |
| F1 | 4A/Clip-in | Supplies -22V(2) | 11.11-1 |
| F2 | 4A/Clip-in | Supplies +22V(2) | 11.11-1 |
| F3 | 3.15A/Clip-in | Supplies +15V(2) | 11.11-1 |
| F4 | 3.15A/Clip-in | Supplies -10V(2), -15V(2) | 11.11-1 |
| F5 | 1A/Clip-in | Supplies -8V(2) | 11.11-2 |
| F6 | 1A/Clip-in | Supplies +8V(2) | 11.11-2 |
| Power Supply (38V) | | | |
| F1 | 1A/Solder-in | -38V Supply Line | 11.12-1 |
| F2 | 1A/Solder-in | +38V Supply Line | 11.12-1 |
| Mother Board | | | |
| F1 | 1A/Clip-in | Transformer secondary to 400V PSU | 11.16-5 |
| F2 | 1A/Clip-in | Transformer secondary to 400V PSU | 11.16-5 |
| F3 | 2.5A/Solder-in | Transformer secondary to 38V PSU | 11.16-5 |
| F4 | 2.5A/Solder-in | Transformer secondary to 38V PSU | 11.16-5 |
| Power Input Module | | | |
| 220/240V | 3A/Clip-in | All circuits | 11.18-6 |
| 100/120V | 6.25A/Clip-in | All circuits | 11.18-6 |

TABLE 2.1 FUSE LOCATION AND PURPOSE

SECTION 3

DISMANTLING AND REASSEMBLY

3.1. GENERAL PRECAUTIONS

3.1.1 WARNINGS

1. ISOLATE THE INSTRUMENT FROM LINE SUPPLY BEFORE ANY DISMANTLING OR REASSEMBLING.
2. THE COMBINED REMOVAL OF TOP AND BOTTOM COVERS, GROUND/GUARD ASSEMBLIES AND REAR PANEL ASSEMBLY LEAVES THE MOULDED INTERNAL CHASSIS UNSUPPORTED. THIS CAN CONSTITUTE A SAFETY HAZARD TO BOTH PERSONNEL AND EQUIPMENT.

3.1.2 CAUTIONS

1. REMOVAL OF THE TOP GROUND/GUARD ASSEMBLY INVALIDATES MANUFACTURER'S CALIBRATION CERTIFICATION.
2. HANDLE THE INSTRUMENT CAREFULLY WHEN INVERTED, TO AVOID SHAKING PRINTED CIRCUIT BOARDS LOOSE.
3. DO NOT TOUCH THE PCB EDGE CONNECTORS.
4. ENSURE THAT NO WIRES ARE TRAPPED WHEN FITTING GROUND/GUARD ASSEMBLIES.
5. DO NOT ALLOW WASHERS, NUTS ETC. TO FALL INTO THE INSTRUMENT.

3.2 General Mechanical Layout *(Volume 2, pages 11.0-1 and 11.18-1 to 11.18-7).*

All circuits are housed within a single unit on printed circuit board assemblies, the eight major PCBs being plugged into a "Mother" PCB assembly.

The 4708 MULTIFUNCTION CALIBRATOR can be used as a bench-top instrument, or it may be rack mounted in a standard 19" rack.

3.2.1 Front Panel

Six output terminals with captive, insulated caps are provided. Alternatively, the terminals can be fitted to the rear panel (Option 42) at manufacture (*page 11.19-2*).

A printed overlay on the front panel labels all the controls, and retains polarizing filters for the displays.

The intake filter is retained by a grille but is removable for cleaning. At the extreme left of the panel, an extractor fan draws cooling air through the filter and internal heat exchangers, discharging to atmosphere.

3.2.2 Rear Panel

The recessed Power Input plug, Power Fuses and Line Voltage Selector are contained in an integral filter module at the centre of the rear panel.

The Calibration Enable switch (with removable key), and the External Frequency Input BNC socket (J53) are mounted directly on the panel between the Power Input module and the cooling-air intake filter.

The IEEE 488 standard connector socket (J27) with instrument address switch, the Calibration Interval Switch and the external frequency switch (S53) are all mounted on the Interconnection PCB assembly. This is fitted on spacers to the inside face of the panel with external components protruding to the rear. Socket J54 is provided to facilitate future expansion.

3.3 LOCATION AND ACCESS

3.3.1 External Construction

Rigid side extrusions, together with the front and rear panel assemblies, form the basic chassis of the instrument. The side extrusions have handles and rear spacers fitted for bench-top use, or are fitted with 'ears' and slides for rack mounting (see User's Handbook, *Section 2*).

The top cover locates into the side extrusions and is secured by screws. The bottom cover is attached in the same way, and includes six domed feet. An operator's instruction card pulls forward from below.

3.3.2 Internal Construction

The chassis is enclosed top and bottom by ground and guard screens. The upper ground and guard screens allow most internal adjustments to be performed without removal. Locations of adjustable components, instructions and warnings are printed on its upper surface.

The interior of the chassis is divided into two compartments. A thermally-enclosed compartment occupies the forward half of the chassis, and is used to house the low power, precision printed circuit board assemblies.

The rear compartment contains high power components, is air-cooled and further subdivided. One section is positioned across the intake airflow, housing the In-guard and Out-guard Power Supply assemblies and providing anchorage for the Mains (Line) Transformer assembly. The other section houses three Heatsink assemblies, provides anchorage for the LF Transformer assembly, High Voltage assembly and 38V Power Supply assembly.

Filtered air passes over the power supplies, mixes with air in the rear compartment, is drawn through the heatsink assemblies, and is finally expelled from the instrument by the extractor fan.

Guard screens are provided against the outer walls of the power supply sub-compartment and the heatsink compartment.

Interconnections between the Power Amplifier assembly, all forward-compartment assemblies, and the Front assembly are made via a Mother PCB. The latter fits across the bottom of the forward compartment, extending at the front to the Front assembly and at the rear to the 38V Power Supply. Four moulded stiffeners keep the mother pcb rigid, also providing lateral locating slots for printed circuit boards and guard screens.

The main printed circuit boards in the forward compartment fit across the full width of the instrument chassis. They slide into vertical slots cut into the moulded chassis, their PCB edge-connection fingers making electrical contacts with sockets mounted on the Mother Assembly. Interleaved between the assemblies are screening shields. These are also guided by slots, and make similar electrical contact.

The Power Amplifier assembly PCB slots in behind the forward compartment across the full width. It connects to the Mother PCB in the same way, but has additional discrete electrical connections for the high power lines.

Each PCB is identified by the color of its ejector lever. The color name is coded at its correct location on the top of the internal moulded chassis (refer to *Table 3.1*). Also, each assembly's edge connector is uniquely configured to prevent incorrect fitting.

The Front PCB assembly, carrying the display components, connects into the front end of the mother PCB outside the thermally-insulated compartment.

3.4 GENERAL ACCESS

- ENSURE THAT POWER IS OFF.
- Heed the General Precautions 3.1.1 & 3.1.2.

If, during a procedure, sufficient access has been obtained then no further dismantling is required.

3.4.1 TOP COVER (11.18-2 Detail 10)

- **Removal**
 - a. Remove the eight M4 x 12mm socket head countersunk screws from cover.
 - b. Remove cover by lifting at the front.

- **Fitting**

Locate cover at rear first, then reverse removal procedure.
-

3.4.2 BOTTOM COVER (11.18-2 Detail 10)

- **Removal**
 - a. Invert the instrument.
 - b. Remove the eight M4 x 12mm socket head countersunk screws from cover.
 - c. Remove cover by lifting at the front.

- **Fitting**

Locate cover at rear first, then reverse removal procedure.
-

3.4.3 FRONT PANEL (11.18-4 Detail 6)

- Remove covers 3.4.1 & 3.4.2
- **Removal**
 - a. Remove the four M4 x 8mm taptite screws from the front panel.
 - b. Remove Earth Connector.
 - c. Remove the Front Panel.

- **Fitting**

Reverse the removal procedure, referring to *Page 11.18-4*.
-

3.4.4 TOP GROUND/GUARD SHEET (11.18-2 Detail 9)

- Removal of the Top ground/guard shield involves breaking Datron's calibration seal and renders manufacturer's calibration invalid.
- Instrument cooling air-flow adversely affected. Internal temperature rise triggers Fail 1. Power OFF and allow to cool as required.
- Remove the top cover (*para. 3.4.1*).

- **Removal**

- a. Refer to *Page 11.18-2* Detail 9 and remove:
 - i. ten M4 x 8mm pozi-countersunk screws
 - ii. six M3 x 6mm pozi-pan screws and M3 shakeproof washers
 - iii. one M3 x 12mm pozi-pan screw and M3 shakeproof washer
- b. Remove the top ground/guard assembly.

- **Fitting**

Refer to *Page 11.18-2* Detail 9 and reverse the removal procedure.

3.4.5 BOTTOM GROUND SHEET (Page 11.18-1 Detail 8)

- Invert the instrument
- Remove the bottom cover (*para. 3.4.2*).

- **Removal**

- a. Refer to *Page 11.18-1* Detail 8 and remove:
 - i. ten M4 x 8mm pozi-countersunk screws
 - ii. six M3 x 6mm pozi-pan screws and M3 shakeproof washers
- b. Remove the bottom ground sheet assembly.

- **Fitting**

Reverse the removal procedure.

3.4.6 BOTTOM GUARD PLATE (Page 11.18-1 Detail 7)

- Invert the instrument. Remove the bottom cover (*para. 3.4.2*). Remove the bottom ground sheet assembly (*para. 3.4.5*).

- **Removal**

- a. Refer to *Fig. 11.18-1* Detail 7 and remove ten M3 x 6mm pozi-countersunk screws.
- b. Remove the bottom guard plate.

- **Fitting**

Reverse the removal procedure, ensuring that no wiring is strained or trapped.

3.5. REMOVAL AND FITTING

Note:

Do not remove the Top Ground/Guard sheet (*para 3.4.4*) if only selecting pre-cal, erasing cal memory, removing Instruction Card or Rear Panel.

In addition to the following Location instructions, refer to Volume 2 page 11.0-1.

| Assembly | Access Required (Heed Caution 3.1) | Location (Page Detail in bracket) | Ejector Color | Section | Page (Vol 2) |
|---|---------------------------------------|---|--|----------------------------|--|
| Instruction Card | - | 11.18-2 (11) | - | 3.5.1 | - |
| Front Assembly | 3.4.5 | 11.18-3 (4) | - | 3.5.2 | 11.1-1 |
| Digital Analog Interface Reference Divider Output Control Sine Source AC Current (OR Current Link pcb) | } 3.4.4 | Chassis Identifier Code { BLK BRN RED ORG YEL GRN BLU BLU | BLACK BROWN RED ORANGE YELLOW GREEN BLUE BLUE | 3.5.4 | 11.2-1 11.3-1 11.4-1 11.5-1 11.6-1 11.7-1 11.8-1 |
| Common Guard and Ground Screens | 3.4.4 | 11.18-5 (13) | - | 3.5.6 | - |
| Power Amplifier | 3.4.4 | 11.18-1 (4) VLT | VIOLET | 3.5.8 | 11.9-1 |
| Power Supplies Out-Guard In-Guard ±38V | } 3.4.4 | 11.18-1 (1) 11.18-1 (2) 11.18-1 (5) | - - - | 3.5.10 3.5.12 3.5.14 | 11.10-1 11.11-1 11.12-1 |
| Heatsinks | 3.4.4 | 11.18-1 (4) | - | 3.5.16 | 11.13-1 |
| High Voltage | 3.4.4 | 11.18-1 (5) | - | 3.5.18 | 11.14-1 |
| Transformers Mains HF LF | } 3.4.4 | 11.18-5 (9) 11.18-4 (6) 11.18-5 (10) | - - - | 3.5.20 3.5.22 3.5.24 | 11.15-1 11.15-2 11.15-2 |
| Mother Board | - | 11.18-3 (3) | - | - | 11.16-1 |
| Interconnections | 3.5.28 | 11.18-6 (15) | - | - | 11.17-1 |
| Terminal Board | 3.4.3 | 11.18-4 (8) | - | 3.5.26 | 11.17-3 |
| Rear Panel | - | 11.18-4 (6) | - | 3.5.28 | 11.18-6 |
| Instrument Assembly | - | - | - | - | 11.20-1 |

TABLE 3.1 INTERNAL LOCATION AND ACCESS

3.5.1 INSTRUCTION CARD

- a. Pull the instruction card forward to its fullest extent.
- b. Bow the card and release the rear lugs from the slots.
- c. Refit in reverse procedure.

3.5.2 FRONT ASSEMBLY (Page 11.18-3 Detail 4)

- Remove Front Panel (*para. 3.4.3*)

- **Removal**

- a. Remove two screws retaining the power switch, together with their two shakeproof washers and four plain washers.
- b. Fold the power switch and its cable clear of the pcb.
- c. Remove the M3 x 6mm pozi-pan screws and wavey washers from 11 positions on the circuit board.
- d. Ease the lower edge of the PCB away from the Mother PCB, to disengage the mating connectors.
- e. Remove the assembly.

- **Fitting**

Reverse the removal procedure. Ensure all mating connectors are full engaged and that the surfaces of displays are clean.

3.5.3 MAJOR PCB ASSEMBLIES

- ENSURE THAT THE INSTRUMENT POWER IS OFF.

- **Removal**

- a. Identify the PCB assembly to be removed (*see Table 3.1*)

Note (operations c to e):

The I/Ω's Link PCB has only one ejector. To remove, grip the top edge and pull gently while levering the ejector upwards and outwards.

- b. Place the thumb of each hand under the lip of the two ejectors on the PCB assembly to be removed.
- c. Gently lever the ejectors upwards and outwards to release the edge connectors.
- d. Remove the assembly.

- **Fitting**

- a. Identify the chassis location of the PCB assembly to be fitted (*See Table 3.1 and page 11.0-1*).

Note:

The single ejector of the I/Ω's Link PCB locates to the 'BLU' identifier of the chassis.

- b. Ensure the ejectors are in the 'down' position.
- c. Insert the PCB edges into the identified slots in the side walls of the chassis.
- d. Allow the PCB to slide down to the Mother PCB, then press home by gently pushing down on the ejectors.

3.5.4 COMMON, GUARD AND GROUND SCREENS (Page 11.18-5 Detail 12)

- The first screen (counting from front to back) is the Ground Screen and has two securing screws. Of the six remaining screens the first five are aluminium, single screw and interchangeable. The rearmost screen is steel and not interchangeable. Each plate mates with a miniature connector on the mother PCB adjacent to the side wall of the chassis.

- **Removal**
 - a. Remove any adjacent assemblies to obtain access.
 - b. Undo securing screw/s.
 - c. Grip the plate and lift out from the chassis.
- **Fitting**
 - a. Insert the plate into the correct slots in the side walls of the chassis (ensure correct orientation).
 - b. Allow the plate to slide down to the Mother PCB, then gently press home.
 - c. Secure with a 3 x 6mm Pozi-screw and shakeproof washer (two for the ground screen).
 - d. Replace assemblies removed for access.

3.5.5 POWER AMPLIFIER ASSEMBLY (Page 11.18-1 Detail 4)

- Do not pull on the connector wires. Some resistance to movement will be felt from the locking clips of the connector bases.

- **Removal**
 - a. Disconnect the five connectors from the assembly as shown on *Page 11.18-1 Detail 4*.
 - b. Fold back the connectors and wires clear of the assembly.
 - c. Place the thumb of each hand under the lip of the two ejectors.
 - d. Gently lever the ejectors upwards and outwards to release the edge connectors.
 - e. Remove the assembly.
- **Fitting**
 - a. Ensure that all wires and connectors are clear of the PCB area.
 - b. Insert the PCB edges into their respective slots in the side walls of the chassis; component side facing the rear of the instrument.
 - c. Allow the assembly to slide down to the Mother PCB taking care not to trap any wires.
 - d. Ensure the ejectors are in the 'down' position then press the assembly home by gently pushing down on the ejectors.
 - e. Identify and fit the five connectors J1 to J5, as shown on *Page 11.18-1 Detail 4*.

3.5.6 OUT-GUARD POWER SUPPLY (Page 11.18-1 Detail 1)

- Do not pull on the connector wires. Some resistance to movement will be felt from the locking clips of the connector bases.

- **Removal**
 - a. Disconnect J1, J2, and J3 from the In-Guard Power Supply Assembly.
 - b. Disconnect the connector J3 from the PCB.
 - c. Fold back the connectors and wires clear of the assembly.
 - d. Grip the top edge of the PCB and lift gently from the chassis.
 - e. Remove the assembly.

- **Fitting**
 - a. Ensure that all wires and connectors are clear of the PCB area.
 - b. Insert the PCB edges into their respective slots in the chassis sub-compartment.
 - c. Allow the assembly to slide down to the miniature connectors on the chassis, taking care not to trap any wires.
 - d. Fit the J3 connector to the assembly.
 - e. Press the assembly home by gently pushing down on the top edge of the PCB.
 - f. Fit J1, J2 and J3 to the In-Guard Power Supply Assembly.

3.5.7 IN-GUARD POWER SUPPLY (Page 11.18-1 Detail 2)

- Do not pull on the connector wires. Some resistance to movement will be felt from the locking clips of the connector bases.
- The Out-Guard Power Supplies components can obstruct the removal of the In-Guard Power Supply. Remove Out-Guard Power Supply Assembly (*para 3.5.6*)

- **Removal**
 - a. Disconnect the three connectors J1, J2 and J3 from the PCB.
 - b. Fold back the connectors and wires clear of the assembly.
 - c. Grip the top edge of the PCB and lift gently from the chassis.
 - d. Remove the assembly.

- **Fitting**
 - a. Ensure all wires and connectors are clear of the PCB area.
 - b. Insert the PCB edges into the respective slots in the chassis sub-compartment.
 - c. Allow the assembly to slide down to the miniature connectors on the chassis, taking care not to trap any wires.
 - d. Press the assembly home by gently pushing the top edge of the PCB.
 - e. Fit the Out-Guard Power Supply (*para. 3.5.6*)
 - f. Identify and fit the three connectors J1, J2 and J3 as shown on *Page 11.18-1 Detail 2*.

3.5.8 38V POWER SUPPLY (Page 11.18-1 Detail 5)

- Heed the General Precautions 3.1.

- **Removal**
 - a. Grip the edges of the pcb and pull the assembly vertically upwards. Some resistance will be felt from the edge connector.

- **Fitting**
 - a. Locate the assembly into the guides
 - b. Apply downward pressure until the connector is felt to have engaged.

3.5.9 HEATSINK ASSEMBLIES (Page 11.18-1 Detail 3)

- Heed the Warnings and Cautions 3.1.1 & 3.1.2. Allow heatsinks to cool before handling. Do not pull on the connector wires. When disconnecting connectors, some resistance to movement will be felt from the locking clips of the connector bases.
- Although the heatsink assemblies are discrete items, removal is simplified when performed in the following order:
 1. Negative Heatsink assembly
 2. Positive Heatsink assembly
 3. Power Supply/Current Heatsink assembly.

- **Removal**

- a. Remove the six M3 x 12mm pozi-countersunk screws from the heatsink retaining plate.
- b. Remove the heatsink retaining plate.
- c. Disconnect connectors:

J1 at the Negative Heatsink Assembly
J2 at the Power Amplifier Assembly
- d. Remove Negative Heatsink assembly.
- e. Disconnect J3 at the Power Amplifier assembly
- f. Remove the Positive Heatsink assembly

- g. Disconnect at the following points:

| | |
|----------|--------------------------|
| J1 | Power Amplifier Assembly |
| J31, J19 | Mother Assembly |
| J1 | In-Guard PSU Assembly |

- h. Remove the Power Supply/Current Heatsink assembly.

- **Fitting**

Reverse the removal procedure. To ensure correct location, orient the PCB side of each heatsink to face inwards

3.5.10 HIGH VOLTAGE ASSEMBLY (Page 11.18-1 Detail 5)

- **Removal**

- a. Lift the assembly upwards as shown on Page 11.18-1 Detail 5.
- b. Remove the connections J2, J3, and J4 as shown in the diagram.
- c. Lift the assembly clear of the instrument.

- **Fitting**

Reverse the removal procedure, referring to Page 11.18-1 Detail 5.

3.5.11 MAINS TRANSFORMER ASSEMBLY (Page 11.18-5 Detail 9)

- Remove the Out-Guard and In-Guard Power Supply Assemblies (see paras 3.5.10 and 3.5.12).

- **Removal**

- a. Disconnect the connectors from the transformer at the following assemblies:

J32 - Mother Assembly (Page 11.18-1 Detail 3)
J6 - Interconnection Assembly
(fixed on the rear panel see page 11.18-4 Detail 8)
J4 - H.V Assembly (Page 11.18-1 Detail 5)
J33 - Mother Assembly (Page 11.18-1 Detail 3)

- c. Release the four M8 x 110mm bolts, washers and nylock nuts.
- d. Remove the M3 x 8mm pozi-countersunk screw, M3 steel nut and shakeproof washer which secures the solder tag terminals of four ground wires. Fold back the wire which is fitted to the rear panel assembly.
- e. Remove the Mains (Line) Transformer assembly.

- b. Turn the instrument to stand on its left side (on Left Hand extrusion)

- **Fitting**

Reverse the removal procedure, referring to Page 11.18-5 Detail 9.

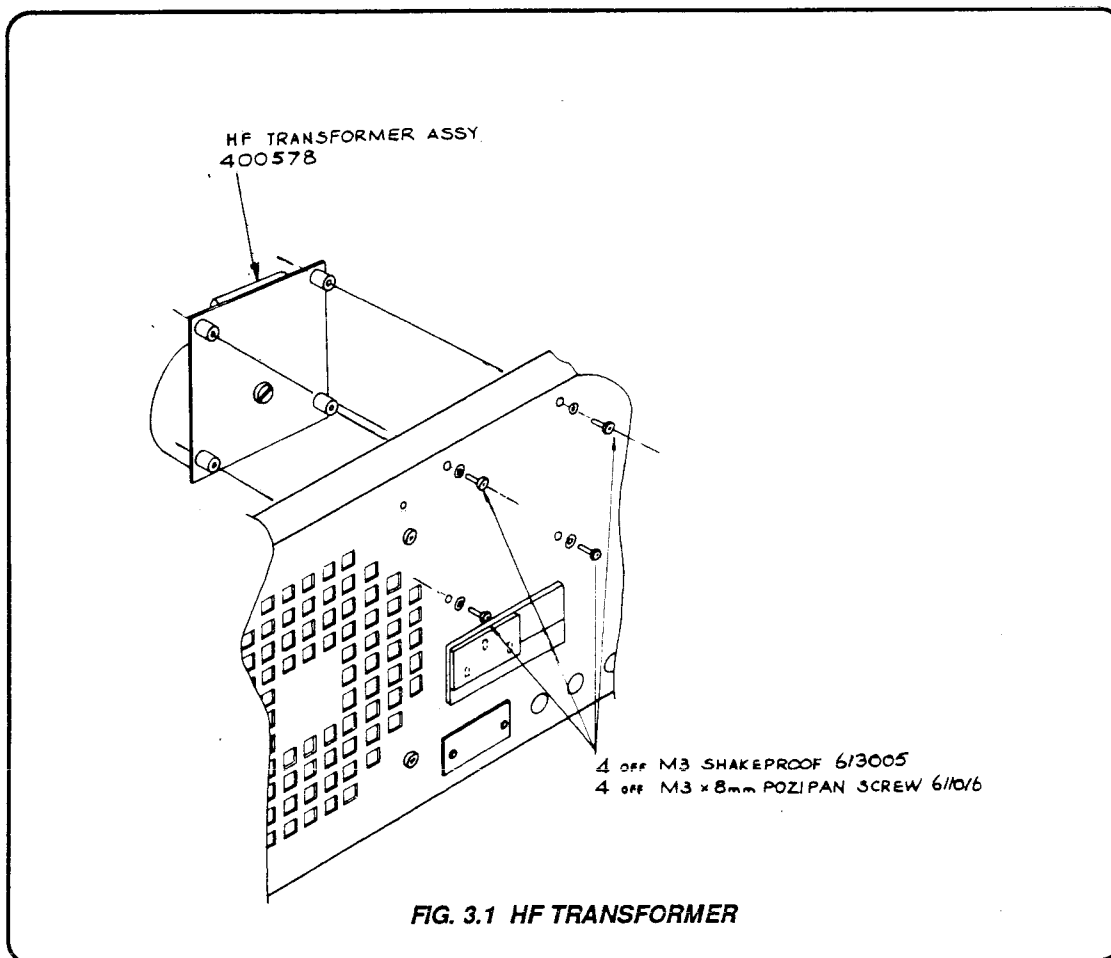
3.5.12 HF TRANSFORMER ASSEMBLY (Page 11.15-2)

• Removal

- a. Remove four M3 x 8mm pozi-pan screws (see Fig. 3.1).
- b. Disconnect connectors at the following points:
J2 - High Voltage Assembly;
J5 - Power Amplifier Assembly.
- c. Remove the HF transformer assembly.

• Fitting

Reverse removal procedure, referring to Fig. 3.1.



3.5.13 LF TRANSFORMER ASSEMBLY (Page 11.15-2 Detail 1 to 4)

- Remove High Voltage Assembly (3.5.18) and the Heatsinks (3.5.16.)

Removal

- Disconnect connector J4 from the Power Amplifier and J3 from the High Voltage Assembly (see Fig. 3.2).
- Turn the instrument to stand on its right hand side (on R.H. extrusion).
- Desolder J34 from the mother board and connections A, B, M, H, K, & L. Unscrew supporting clips.
- From the LF Transformer; remove the four M5 nylock nuts and flat steel washers, Remove the pair of transformer assembly M5 x 65mm screws closest to the rear panel and the transformer bolt plate.
- Slide out the LF Transformer.

Fitting

Reverse the removal procedure, referring to Fig. 3.2 and Page 11.15-2 Detail 1 to 4.

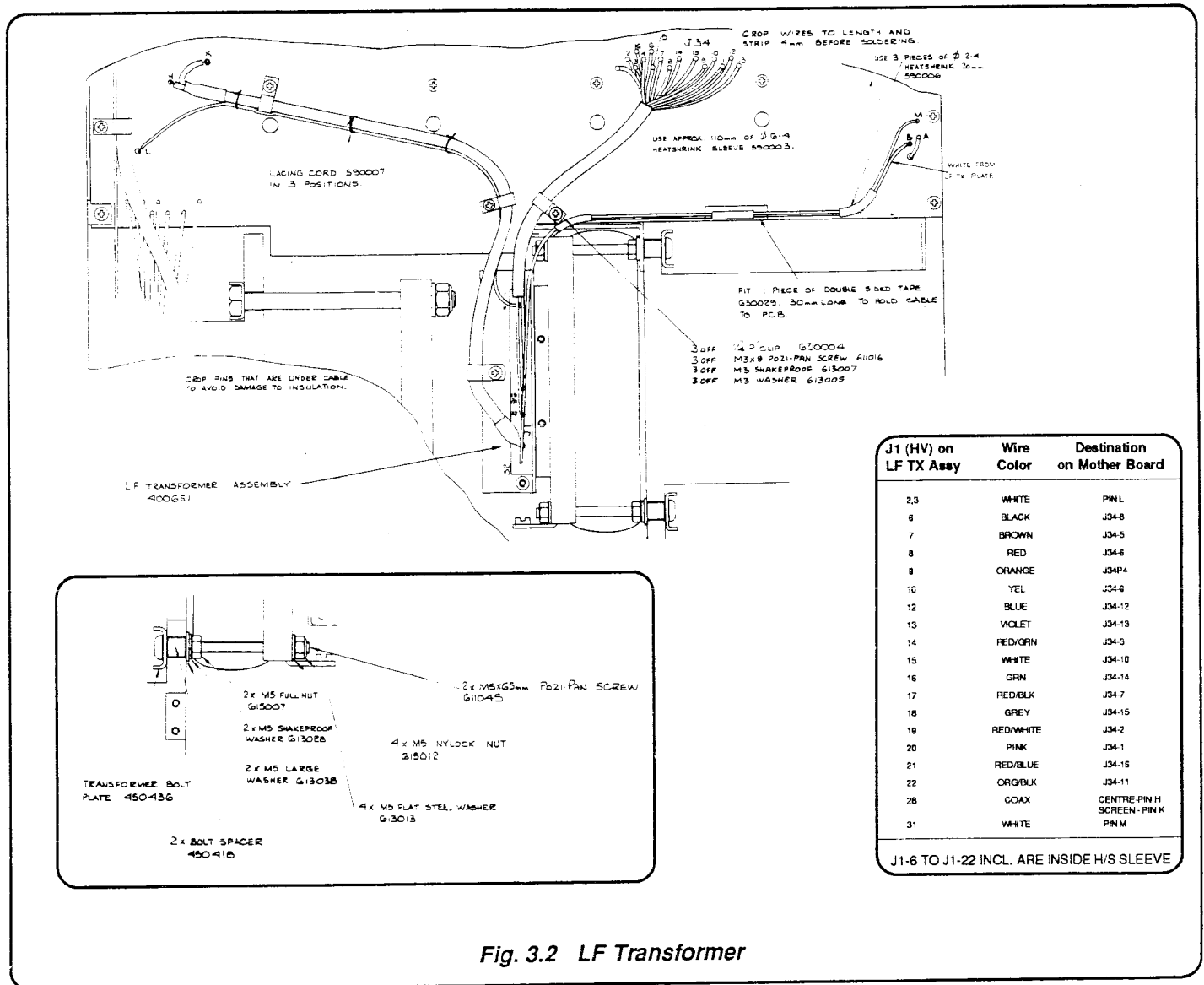


Fig. 3.2 LF Transformer

3.5.14 TERMINAL PCB ASSEMBLY (Page 11.17-3)

- Remove Front panel (*para 3.4.3*).
 - **Removal**
 - a. Remove the four M3 x 6mm pozi-pan screws (*11.18-4* Detail 8)
 - b. The terminal board can be tipped down to facilitate component access. If leads are short remove Bottom Guard Plate (*para. 3.4.6*) and desolder as required.
 - **Fitting**
 - Reverse the removal procedure.
-

3.5.15 REAR PANEL ASSEMBLY (Page 11.18-6)

- Do not remove the rear panel assembly when Top and Bottom covers and Ground/Guard assemblies are removed. Perform the following operations with Top and Bottom Covers and Ground/Guard assemblies fitted, or with AT LEAST the Top OR Bottom Ground Sheet assembly fitted.
 - This procedure provides access to rear panel-mounted components by releasing the Rear Panel assembly and moving it away from the chassis to the extent allowed by internal wiring connections.
 - **Removal**
 - a. Remove the six screws of the two rear spacers *11.18-4* Detail 7.
 - b. Remove the two rear spacers.
 - c. Remove the four screws of the filter grill.
 - d. Remove the filter grille and filter.
 - e. Remove the Pozi-pan screw revealed by the removal of the filter and grill.
 - f. Remove the four rear panel screws (*Page 11.18-4* Detail 6)
 - g. Looking at the rear, locate the upper right hand screw securing the extractor fan. Above this screw, locate an M3 x 6mm Pozi-pan screw (screw fixing hole only shown on cut-away sketch above Rear Panel in Detail 6 of *page 11.18-4*). Removal of the screw allows the rear panel to be detached.
 - h. Gently pull the Rear Panel assembly away from the chassis to the extent allowed by the wiring. Do not stress the wires.
 - **Fitting**
 - a. Press the Rear Panel assembly to the chassis while ensuring that:
 - i. The wires lay in the cut-out in the moulded internal chassis
 - ii. The ribbon cables fit in the recess in the moulded internal chassis
 - iii. All other wires are free and not trapped by the rear panel assembly.
 - b. Fit screws, filter, filter grille and rear spacers, reversing the removal procedure.
-

SECTION 4 SERVICING & INTERNAL ADJUSTMENTS

4.1 INTRODUCTION

This section provides procedures for any maintenance or calibration operations which require removal of covers or partial dismantling. The operations fall into three Categories:

- A: Routine Servicing (TABLE 4.1a),
- B: Internal Calibration Adjustments (TABLE 4.1b)
- C: Adjustment Following Replacement of PCBs (TABLE 4.1c - overleaf).

| Category A | Routine Servicing | | | |
|---|---|-----------------------|---|------------------------|
| Servicing Required | Time Interval | Procedure (Section 4) | Calibration Required | Calibration Procedure |
| Clean the Air Intake Filter | 1 year (or less in adverse conditions) | 4.2 | - | - |
| Change Lithium Battery (non-volatile calibration memory) | 5 years | 4.3 | (a) Full pre-cal then (b) Full routine recalibration | Sect. 1.4 Sect. 1.2 |

TABLE 4.1a.

| Category B | Internal Calibration Adjustments | | | |
|---|----------------------------------|-----------------------|----------------------------------|-----------------------|
| Indication | Adjustment Required | Procedure (Section 4) | Calibration Required | Calibration Procedure |
| "ERROR 6" (during Routine Recalibration) | Re-set internal trimmers | 4.4 | Routine 4-wire & 2-wire Ω | Sect. 1.2 |

TABLE 4.1b.

4.1.1 General Procedure Notes

- a. Set Power OFF before attempting to dismantle the instrument (for dismantling and reassembly instructions consult Section 3).
- b. If Top ground/guard assembly is removed subsequent testing with Power On should be completed in less than 5 minutes to avoid overheating.
- c. After servicing ensure that all connections have been made (Section 3, Fig. 3.6) and that Top and Bottom shields and covers have been replaced. Leave assembled instrument powered-up for at least 1 hour before carrying out any adjustment.
- d. Although replacement assemblies are set up by the manufacturer, the internal adjustments recommended in Table 4.1 must be carried out to ensure correct operation. These adjustments need to be carried out when the assembly is in the user's instrument, in order to account for interaction between assemblies.

WARNING

**HAZARDOUS ELECTRICAL POTENTIALS
ARE EXPOSED WHEN THE INSTRUMENT
COVERS ARE REMOVED.**

ELECTRIC SHOCK CAN KILL!

CAUTION

AFTER ANY MAINTENANCE OPERATIONS WHICH INCLUDE REMOVAL OF TOP OR BOTTOM GROUND ASSEMBLY, CARRY OUT THE FULL SELF-TEST SEQUENCE (Section 2.3) BEFORE RETURNING TO NORMAL USE.

DAMAGE CAUSED BY UNAUTHORISED REPAIRS OR MODIFICATIONS CAN INVALIDATE INSTRUMENT WARRANTY. CHECK THE WARRANTY DETAILED IN THE "TERMS AND CONDITIONS OF SALE". IT APPEARS ON THE INVOICE FOR YOUR INSTRUMENT.

4.1.1 General Procedure Notes

- a. Set Power OFF before attempting to dismantle the instrument (for dismantling and reassembly instructions consult *Section 3*).
- b. If Top ground/guard assembly is removed subsequent testing with Power On should be completed in less than 5 minutes to avoid overheating.
- c. After servicing ensure that all connections have been made (*Section 3, Fig. 3.6*) and that Top and Bottom shields and covers have been replaced. Leave assembled instrument powered-up for at least 1 hour before carrying out any adjustment.
- d. Although replacement assemblies are set up by the manufacturer, the internal adjustments recommended in *Table 4.1* must be carried out to ensure correct operation. These adjustments need to be carried out when the assembly is in the user's instrument, in order to account for interaction between assemblies.

WARNING

**HAZARDOUS ELECTRICAL POTENTIALS
ARE EXPOSED WHEN THE INSTRUMENT
COVERS ARE REMOVED.**

ELECTRIC SHOCK CAN KILL!

CAUTION

AFTER ANY MAINTENANCE OPERATIONS WHICH INCLUDE REMOVAL OF TOP OR BOTTOM GROUND ASSEMBLY, CARRY OUT THE FULL SELF-TEST SEQUENCE (*Section 2.3*) BEFORE RETURNING TO NORMAL USE.

DAMAGE CAUSED BY UNAUTHORISED REPAIRS OR MODIFICATIONS CAN INVALIDATE INSTRUMENT WARRANTY. CHECK THE WARRANTY DETAILED IN THE "TERMS AND CONDITIONS OF SALE". IT APPEARS ON THE INVOICE FOR YOUR INSTRUMENT.

| Category C | | Adjustment Following Replacement of PCBs | | |
|--------------------------------|---|--|------------------------|--------------------------------------|
| PCB Assembly | Adjustments | Procedure (Section 4) | Pre-cal (Sect. 1.4) | Routine cal (Sect. 1.2) |
| Terminal | Capacitive Load Test | 4.6 | - | Full |
| Digital | - | - | Full | Full |
| Reference Divider | - | - | Full | Full |
| DC | Capacitive Load Test | 4.6 | - | Full |
| Sine Source | - | - | - | Full |
| AC | Capacitive Load Test Sense Amp zeros | 4.6 4.10 | - | Full |
| Current/Ohms Assembly | Quiescent Current Compliance Resistance | 4.7 4.8 4.4 | - | All I ranges All I ranges Ohms |
| Power Amp | 100V PA bias | 4.5 | - | - |
| Mother | Common-mode null | 4.9 | Full | Full |
| Out-guard PSU | Common-mode null | 4.9 | - | Full |
| Heatsinks +ve & -ve | 100V PA bias | 4.5 | - | - |
| Power supply Current Heatsinks | Quiescent Current | 4.7 | - | All I ranges |
| HF or LF Transformer | - | - | - | 1kV Range |
| Mains (line) Transformer | Common-mode null | 4.9 | - | - |

TABLE 4.1c.

4.2 **CLEANING THE AIR INTAKE FILTER**

(Datron Part No. 450277-1) (Refer to *Section 3.14, Fig. 3.8*)

4.2.1 **Servicing Frequency**

The filter should be cleaned at intervals no greater than one year.
In dusty conditions the frequency should be increased.

4.2.2 **Removal** (*Fig. 3.8*)

- a. Remove the four M3 x 10mm pozi-countersunk screws (11) which retain the filter grille (12).
- b. Remove the filter grille and reticulated foam filter.

4.2.3 **Cleaning**

- a. Wash the foam filter in a dilute solution of household detergent (hand hot).
Rinse thoroughly in clean hand-hot water and dry completely, without using excessive heat.
- b. Clean the grille, and the grille holes in the rear panel (use a vacuum cleaner and soft brush on the rear panel).

4.2.4 **Inspection**

Examine the foam filter for wear, replacing if links are broken.

4.2.5 **Reassembly**

Place the filter in the grille housing and secure the grille to the rear panel using the screws removed in 4.2.2 above.

4.3 LITHIUM BATTERY - REPLACEMENT

(Datron Part No. 920101)

FIRST READ THESE NOTES!

- This procedure is to be performed at intervals of 5 years from new.
- Procedure 4.3.1 allows calibration memory to be retained during battery replacement. This requires the use of an Extender Card (Datron Part No. 400625) to give access to the battery and during its removal provide a supply to the non-volatile RAMs. To ensure memory integrity the soldering iron used must be isolated from mains earth by at least 50k Ω .
- Procedure 4.3.3 resets the calibration memory to its nominal state (but does not require the use of an extender card) during replacement of the battery. If this method is used a Precalibration and full Routine Recalibration (*Section 1.4* and *1.2*) **must** follow before the instrument specification can be realized, as calibration data will be corrupted. In this case it is therefore recommended that the battery be replaced immediately prior to a scheduled full recalibration.

4.3.1 Procedure (Calibration Maintained)

- a. Ensure that power OFF is selected.
- b. Remove the top cover and top ground/guard assembly (*Section 3 paras. 3.2.1* and *3.4.1*).
- c. Remove the Digital Assembly from the chassis (*Section 3 para. 3.6.4*).
Do not place the assembly on any conducting surface or touch the gold edge connector.
- d. Place extender card in digital assembly slot.
Push Digital Assembly onto extender card

Caution

- If the calibrator has been in use; allow to cool for 2 hours. From power ON (step f.) the internal temperature of the instrument will begin to rise. Ensure the procedure is completed within approximately 15 minutes; any Fail 1 message which occurs during this time period can be safely ignored.
 - Precautions must be taken to prevent solder or other material falling into the calibrator.
 - Ensure continuity of mains supply while battery is disconnected.
- e. Select power ON. To reduce power dissipation ensure output remains OFF.
 - f. Remove battery (refer to *Fig. 4.1*).

- i. Push sleeve back along the red wire to expose the solder joint.
- ii. Unsolder the red wire from the positive terminal of the battery.
- iii. Unsolder the negative terminal of the battery from resistor R60 at the wrap-joint.
- iv. Remove battery from battery clip

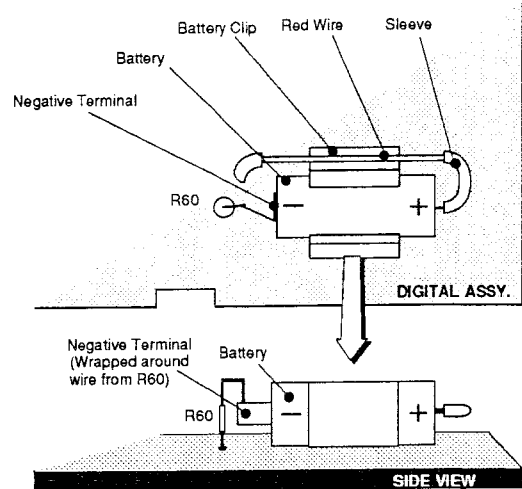


FIG. 4.1 BATTERY REPLACEMENT

- g. Fit and solder in a new battery, reversing the procedure of step (f.) Select power OFF (calibration maintained).
- h. Refit the Digital Assembly into the chassis (*Section 3 para. 3.5.5*).

4.3.2 Return to Use

Refit the top ground/guard assembly into the chassis (*Section 3 para. 3.4.8*).
 Refit the top cover (*Section 3 para. 3.4.2*).

- Users having followed procedure 4.3.3 must now carry out Pre-calibration and full Routine Calibration in accordance with *Section 1.4* and *1.2* respectively.

4.3.3 Procedure (Calibration lost)

Follow the procedure 4.3.1 (ignore steps (d.) and (e.)) and 4.3.2.

4.4 OHMS FUNCTION-STANDARD RESISTOR ADJUSTMENT

4.4.1 Introduction

Routine adjustment of the standard resistors used in Ω function is not required. A resistor is calibrated by the user entering its measured value into a non-volatile calibration memory. This value is subsequently recalled and displayed to the user each time the resistor is selected.

4.4.2 'Error 6' Message

'Error 6' is displayed if the value entered by the user during calibration is outside the resistor's tolerance (*Section 1.2*) i.e. outside the calibration memory span. Under normal use the resistor drift is well within the tolerance, so 'Error 6' appears only if the user enters an erroneous value.

4.4.3 Undue Resistor Stress

If the resistor has been subjected to undue stress, it is possible that its value may have changed slightly, and be outside its tolerance. If it is less than approximately 50ppm outside tolerance an internal trimmer can be adjusted, and the value can be calibrated.

4.4.4 Possible Damage

A stressed resistor may have been damaged if its value is greater than 50ppm outside its tolerance. It is advisable to have such a resistor tested or replaced by Datron Service Center.

4.4.5 To Reset Internal Trimmers

Follow the procedure detailed in *Section 1.7* to adjust the resistor value. If this is unsuccessful contact your Datron Service Center.

4.5 Bias Current Adjustment - 100V PA

(Refer to *Layout Drawing 480618* and *480637*)

Adjustment of the 100V/1kV amplifier bias voltages must be carried out after fitting a replacement Power amplifier assembly or Heatsink assembly. The following procedure ensures the drain voltages of Q4 and Q2 are +120V and -120V respectively.

USE EXTREME CARE THROUGHOUT THE FOLLOWING PROCEDURES.

4.5.1 Test Equipment Required

Digital voltmeter (any Datron Autocal voltmeter)

4.5.2 Initial Conditions

Remove Top cover.
Remove Top ground/Guard assembly.
Ensure 38V/400V selector is set to 400V.

4.5.3 Procedure

- a. Set 4708 Power OFF to connect DVM as follows;
- b. Power Amplifier Assembly Connect DVM in DC function, Lo to ∇ 2C (near Q20) and Hi to Tab of Q4.

WARNING. At Power ON (even with Output OFF) the heatsinks are maintained at LETHAL VOLTAGES!
Use insulated adjustment tool.

- c. Select Power ON .
- d. Positive Heatsink Assembly Adjust R10 for a reading of +120V (5V).
- e. Power OFF, disconnect DVM.

4.5.4 Return to Use

Refit Top ground/guard shield and Top cover.

4.6 CAPACITIVE LOAD TEST

(Refer to *Layout Drawing 480536*)

The AC 1kv current overload detector, on the DC Assembly monitors output current. ERROR OL is displayed when output current limit is exceeded.

After replacing the DC Assembly, the Terminal assembly, AC assembly, PA assembly, Positive or Negative Heatsinks, or the HF transformers it is necessary to ensure the limit level is re-set to account for any capacitance changes. The value of R84 will lie between 2k43Ω and 3k65Ω. R84 will be selected from the E96 (1%) series.

4.6.1 Test Equipment Required

- a. Test Load (1kΩ non-inductive resistor, capable of dissipating 20 Watts).
- b. Digital Voltmeter fitted with AC Volts Ranges (any Datron Autocal multimeter)

4.6.2 Initial Conditions

Top cover removed.
Remove Top ground/guard assembly.
Ensure 38V/400V power supply selector set to 400V.

4.6.3 Procedure

**WARNING THE PROCEDURES INVOLVE THE MEASUREMENT OF LETHAL VOLTAGES.
USE EXTREME CARE TO AVOID ELECTRIC SHOCK.**

- a. Ensure 4708 Power OFF.
- b. On DC board remove Link J, and make Link L. DC assembly must be fitted in chassis (not on extender card)
- c. Monitor Link L with respect to ∇ 2B with scope set to 5V per division.
- d. Connect Load resistor across the 4708 output terminals.
- e. Connect the DVM across the Load resistor and select AC 1kV range on DVM.
- f. Set 4708 Power ON.
- g. On 4708 select AC 1kV Range and adjust OUTPUT \updownarrow keys for 90V on the OUTPUT display. Select 10kHz range and set frequency to 4kHz. Set OUTPUT ON.
- h. Increment demanded voltage and check that 'Scope goes to zero volts when the DVM indicated between 108V and 112V. Select output OFF.

WARNING Calibrator Power must be OFF when changing R84. Lethal voltages are present!

- j. If outside limits set in (h.) reselect R84 and repeat from step (f.).
- k. When correct operation occurs solder in R84 break Link L and replace Link J.

4.6.4 Return to Use

Refit Top ground/guard shield and Top cover.

4.7 QUIESCENT CURRENT ADJUSTMENT - CURRENT/OHMS ASSEMBLY

(Refer to *Layout Drawing No. 480614 and Page 11.8*)

To allow a measurement of quiescent current in the power amplifier stage, its power supply lines are broken and a 0.1 Ω resistor inserted in series with each 22V supply line. The voltage developed across either of these resistors gives a current measurement. The quiescent current is set by adjustment of R23 on the Current/Ohms Assembly.

4.7.1 Test Equipment Required

- a. Digital Voltmeter (any Datron Autocal voltmeter)
- b. Two 2.5-watt resistors, 0.1 Ω , 10%, wire wound (Welwyn W21 or equivalent)

4.7.2 Initial Conditions

- Top cover removed.
- Top ground/guard assembly removed.

4.7.3 Procedure

- a. Switch the 4708 Power OFF.
- b. Break the 22V supply connections to the Voltage-to-Current converter power stage by removing connector J1 from the In-guard power supply pcb.
- c. Re-make each 22V supply connection from its female pin on the freed J1 connector to its corresponding male pin on the In-guard P.S pcb, using one 0.1 Ω resistor in series with each supply line (Red and Brown wires).
- d. Connect the digital voltmeter across one of the 0.1 Ω resistors fitted in step (c.).
- e. Switch 4708 Power ON. Select AC Current, 1Amp Range, ensure OUTPUT OFF.

CAUTION In the following (step f.), use a thin insulated screwdriver.

- f. Carefully adjust R23 on I/ Ω assembly for a digital voltmeter reading of 10mV \pm 1mV (equivalent to 100mA through a 0.1 Ω resistor).
- g. Switch 4708 Power OFF.
- h. Disconnect and remove both 0.1 Ω resistors and the digital voltmeter from J1. Reconnect J1 to the In-guard Power Supply pcb pins.

4.7.4 Return to Use

Refit top ground/guard assembly and Top cover.

4.8 COMPLIANCE ADJUSTMENT

(Refer to *Layout Drawing 480614 Page 11.8*)

Ensure that the Quiescent Current Adjustment Procedure has been completed (*Section 4.7*).

In the following procedure a DVM is used to measure output current as a voltage developed across a load resistor. Series resistance is then added to one of the power leads to establish a compliance voltage. The change in current output due to compliance is measured and an adjustment made to bring the instrument within manufacturer's specification.

4.8.1 Test Equipment Required

- a. Digital Multimeter fitted with AC Volts Ranges. (Datron Instruments model 1081).
- b. Test leads, (each containing a 22.1Ω resistor).
- c. One 2.5-watt load resistor of 0.10Ω , 10%, Wire Wound. (Welwyn W21 or equivalent).
- d. A 1.4Ω resistor to introduce compliance voltage.

4.8.2 Initial Conditions

Remove Top cover.
Remove Top ground/guard assembly.

4.8.3 Procedure

- a. Connect the 0.1Ω load resistor between the 4708 current output terminals (I+/I-).
- b. HF adjustment. Select ACI, 1A full range output at 5kHz. Select OUTPUT ON.
- c. With the DVM, measure the AC voltage across the load and note the reading. Set OUTPUT OFF.
- d. Introduce the 1.4Ω compliance resistor in series with the I+ lead. Set OUTPUT ON (Test should be done in less than 5 minutes to avoid overheating). Use the DVM to measure the AC voltage across the 0.1Ω load and note the reading.
- e. Remove compliance resistor. If there is a change of reading $>10\mu\text{V}$ between (c.) and (d.) adjust R10 to reduce the change of reading to $<10\mu\text{V}$. After each adjustment of R10 repeat (c.) to (e.).
- f. LF Adjustment. Complete above procedure, leaving the 4708 as selected (ACI, 1A Full Range), but change frequency to 500Hz and limit to $5\mu\text{V}$.
- g. If change of reading in (d.) is $>5\mu\text{V}$ adjust R31.
- h. If an adjustment was made to R31 repeat complete procedure from (b.) until no further adjustments are required.
- j. Output OFF, disconnect load resistor.

4.8.4 Return to Use

Replace Top ground/guard assembly and Top cover.

4.9 COMMON MODE NULL ADJUSTMENTS

(Refer to *Diagram 480561 Page 11.10-1* & *Diagram 480604 Page 11.18-4*)

The procedure ensures that after replacement of Outguard Power Supply, Mains transformer or Mother Assembly, any power supply noise breakthrough on the Lo or Guard terminals is adjusted to a minimum. Resistor R12 on the Outguard Power Supply Assembly (accessible through a hole in the Top earth shield) is adjusted to minimize the voltage between Lo and Ground. On the Mother Assembly (accessible through a hole in the Bottom ground shield) R25 is adjusted to minimize noise between Guard and Ground.

4.9.1 Test Equipment Required

Oscilloscope (with AC input and sensitivity to 100mV/div).

4.9.2 Initial Conditions

Remove Top and Bottom covers.
Ensure all guard/earth screws are correctly tightened.

4.9.3 Procedure

- a. Set 4708 to AC 10V range with Output OFF.
- b. Ensure that the OUTPUT display is 0.000,00 V with local guard selected.
- c. Connect the oscilloscope AC input to the 4708 Guard terminal and the oscilloscope Ground to the 4708 Ground terminal.
- d. Locate R12 on the Outguard Power Supply assembly (accessible through the hole in the Top ground/guard assembly)
- e. Select OUTPUT ON and adjust the oscilloscope controls to obtain the line related noise waveform.
- f. Without touching the Top ground/guard assembly, adjust R12 for minimum waveform amplitude.
- g. Select Remote Guard and obtain a noise waveform.
- h. Locate R25 on the Mother pcb assembly through the hole in the Bottom ground/guard assembly
- j. Without touching the Bottom Ground Assembly, adjust R25 for minimum waveform amplitude.
- k. Repeat procedure from step (b.) to step (j.) until minimum waveform amplitude is obtained.
- l. Select OUTPUT OFF. Disconnect the oscilloscope.

4.9.4 Return to Use

- a. Refit Top cover.
- b. Refit Bottom cover.

4.10 SENSE AMPLIFIER ZEROS

(Refer to *Layout Drawing 480844*)

The sense amplifier, situated on the AC Assembly, is provided with access holes located in the Top ground/guard shield. In the following procedure the reading and adjustment steps are always taken with the 4708 OUTPUT ON and at one-tenth of the selected Full Range value.

4.10.1 Test Equipment Required

Digital voltmeter
(Datron Instruments model 1081 or 1071).

4.10.2 Initial Conditions

Remove Top cover only.

4.10.3 Procedure

- a. Connect the DVM Hi to TP5 on the AC Assembly (accessible via the hole in the upper guard shield). Connect its Lo to the 4708 Lo terminal. On the DVM select the DC 10V range with filter in.
- b. On the 4708 select the AC 100V range, set 10V and 1kHz output. Select OUTPUT ON and adjust R122 for a DVM reading of less than $200\mu\text{V}$.
- c. On the 4708 select the AC 10V range, 1V output. Select OUTPUT ON.
- d. Note the DVM reading.
- e. On the 4708 select the 1V range, 100mV output. Select OUTPUT ON.
- f. Note the DVM reading.
- g. Adjust R107 on the AC assembly to set both (d.) and (f.) readings to less than $200\mu\text{V}$.
- h. Repeat procedure from (b.) to (g.) until readings are correct and the difference between all ranges is less than $400\mu\text{V}$ taking polarity into account.
- j. Disconnect the DVM.

4.10.4 Return to Use

Refit Top cover.

PART 2

TECHNICAL DESCRIPTIONS

- SECTION 5 Principles of Operation.**
- SECTION 6 Digital, Control and References; Power Supplies**
- SECTION 7 DC Voltage Outputs - Amplitude Control System.**
- SECTION 8 AC Outputs - Frequency Control System.**
- SECTION 9 AC Voltage Outputs - Amplitude Control System**
- SECTION 10 Current Outputs; Resistance.**

PART 2 TECHNICAL DESCRIPTIONS

SECTION 5 PRINCIPLES OF OPERATION

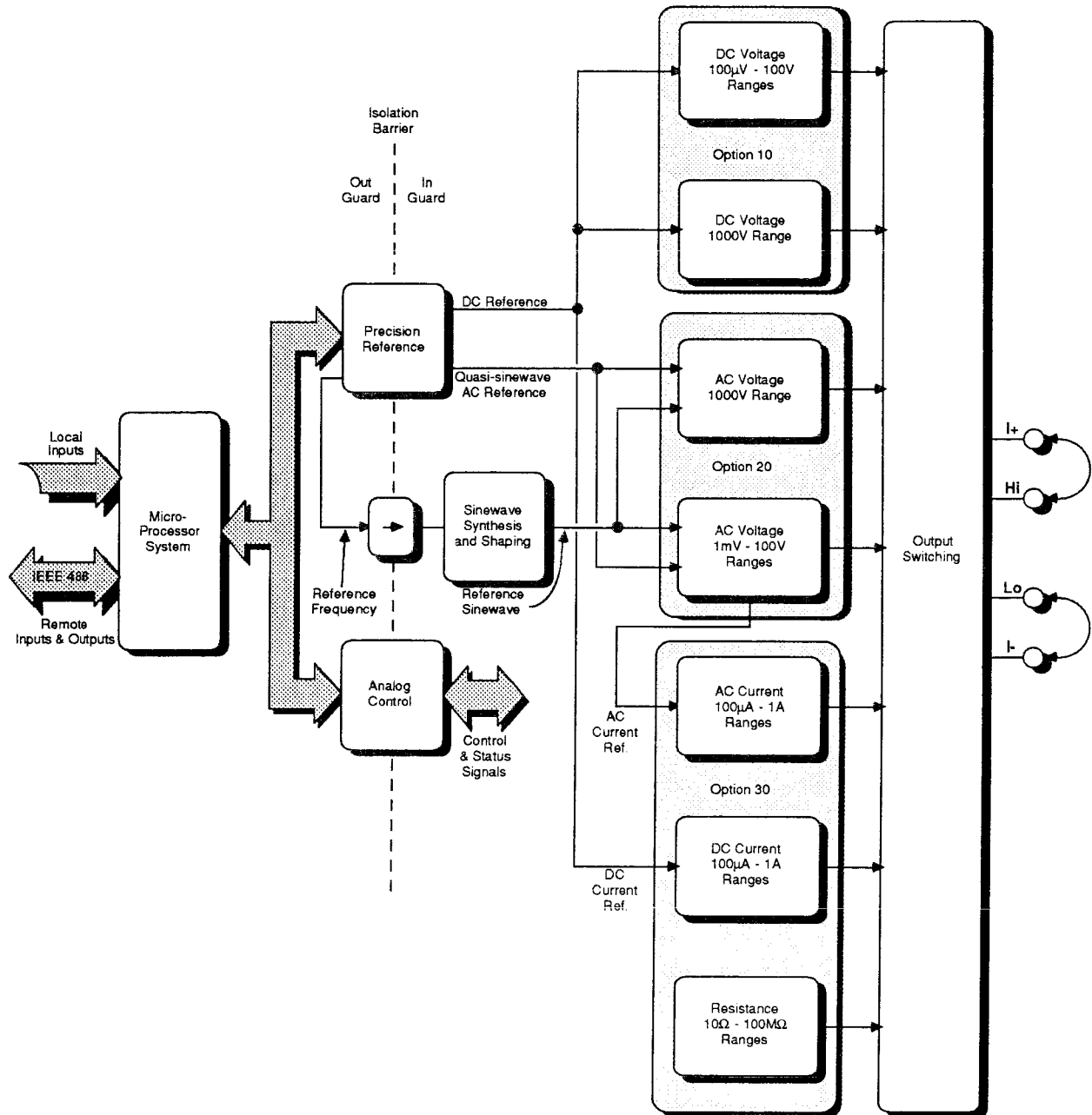


FIG. 5.1 4708 SIMPLIFIED BLOCK DIAGRAM

5.1 BLOCK DIAGRAMS

5.1.1 SIMPLIFIED BLOCK DIAGRAM

Figure 5.1 illustrates the general functions and signal flow within the 4708.

5.1.2 GENERAL DESCRIPTION

The Datron 4708 Autocal Multifunction Standard mainframe contains just a microprocessor system and IEEE-488 interface. To provide any useful function, one or both of Options 10 and 20 must be installed.

Option 10 provides the 4708 with the capability of sourcing DC Voltages in decade ranges from $100\mu\text{V}$ to 1000V , with accuracies and capabilities published in Section 6 of the User's Handbook.

Option 20 provides the 4708 with the capability of sourcing AC Voltages in decade ranges from 1mV to 1000V , at variable frequencies between 10Hz and 1MHz , with accuracies and capabilities as described in Section 6 of the User's Handbook.

Option 30 adds the functions of DC and AC current ranges, and eight accurately defined resistor values, in decades.

For DC and AC amplitude control, an adjustable precision reference is derived from a pre-conditioned zener diode.

For AC outputs, the calibrator frequency is synthesized using a crystal-controlled oscillator as a frequency reference.

5.1.3 FUNCTIONAL BLOCK DIAGRAMS

Figures 5.2 (Digital, Control and References), 5.3 (DC/ Ω) and 5.4 (AC) break the main functional divisions into smaller blocks.

They can be thrown clear of the handbook to provide a functional overview; they also form an index to other sections of Part 2.

5.2 INPUTS

The microprocessor accepts inputs from two main sources:

- The front panel keyboard provides local control inputs.
- The IEEE 488 bus system provides remote control inputs.

5.3 DIGITAL OUTPUTS

The microprocessor system outputs digital information to five main areas:

- The front panel displays provide local outputs for monitoring and control.
- The IEEE 488 bus system provides remote outputs.
- The precision reference generator produces an accurate DC reference for output-amplitude control. Sensed DC outputs are scaled and compared against the DC reference directly. Sensed AC outputs are scaled and compared against a 'quasi-sinewave' reference, whose peak value is set by the DC reference.
- The frequency synthesizer and sinewave oscillator together determine the frequency and purity of the AC output sinewave signal.
- Various decoders control function and range selection, internal processes and status monitoring.

5.4 PRECISION REFERENCE

(Fig. 5.2)

5.4.1 AMPLITUDE REFERENCE

The circuits produce a DC reference voltage which can be set between 0V and ± 20 V for DC outputs, and between +0.126V and +2.794V for AC outputs. The value of the reference is set by the value on the OUTPUT display, modified in software by range scaling and calibration corrections.

For DC, the range-scaled sense voltage is compared directly with the reference - the resulting error controls the DC output value directly. For AC outputs it determines the amplitude of the 'quasi-sinewave', a stepped waveform which is used as the AC amplitude reference. This operates in the error sensing loop, having a shape whose crest factor closely approaches that of a true sinewave.

The circuitry is divided into four main areas:

- a. The period division comparator, outside guard, consists of a binary counter and comparator, both effectively of 25 bits. The counter is driven by a crystal-controlled clock; the comparator being set by latched data from the microprocessor system.

When the binary count matches the data set in the latches, the comparator produces a switching pulse (reset). The counter fills to overflow point, at which the comparator produces a second pulse (set). Thus accurate mark-period timing is generated.

- b. The switching integrator receives the pulses across guard. They are used to drive solid-state divider switches, chopping the output from a very stable 20V DC Master Reference. The resulting square wave is very accurately defined, both in mark-period ratio and amplitude. Integration of the square wave, by an active low-pass filter with high rejection at the chopping frequency, generates the DC Reference voltage.
- c. For DC outputs, the selected output polarity controls a switch which inverts the DC Reference for negative outputs.
- d. For AC outputs, a negative version of the DC reference is generated by inversion. Both positive and negative versions are passed to the quasi-sinewave generator, which sets the positive and negative inputs to a potential divider, whose centre-tap is tied to reference common.

The outputs from the divider are selected in ten equal time-steps by digital logic, the ratios being selected so as to produce a

periodic signal of quasi-sinusoidal form. The Crest Factor of this signal (Peak value divided by RMS value) is 1.397, close to that for a pure sinewave. The RMS ratio of sinewave to quasi-sinewave is stored during calibration, and reapplied as correction during normal use.

Because the amplitude of the quasi-sinewave depends on the value of the DC Reference voltage, its settling time to a stable value is determined by the 7-pole DC reference filter.

For accurate sine/quasi-sine RMS comparison, it is important that both the quasi-sinewave steps and the comparator sequence are synchronized to zero-crossing points in the sensed output sinewave. This is ensured by first:

including the divide-by-ten logic of the quasi-sinewave generator as part of the range-divider chain for the frequency synthesizer,

and then:

feeding the quasi-sinewave frequency to the comparator to synchronize the ten-step sequence which controls the RMS comparison process.

5.4.2 FREQUENCY REFERENCE

When the 4708 is operating in AC function, its internal frequency reference is derived from the 13-bit counter in the Precision Reference out-guard circuitry. The counter is tapped at 16kHz, which is fed directly to the synthesizer to establish the frequency of the VCO oscillation.

For users who wish to lock the output frequency of the 4708 to an external frequency source, a phase-locked loop ensures that the 16kHz reference frequency phase is tied to that of the external Reference Frequency. With correct frequency selection on the front panel, this ensures that the 4708 output frequency locks to the external reference frequency.

This function is performed in the External Reference Frequency Buffer.

5.5 ANALOG CONTROL

(Fig. 5.2)

The analog circuitry is controlled by data held in a 48-bit in-guard latch. The microprocessor regularly updates the latch contents, using the serial link to pass the data (through opto-isolators) across the isolation barrier. Certain analog status signals are returned to the microprocessor, also using the serial link.

5.6 DC VOLTAGE OUTPUTS

(Fig. 5.3)

5.6.1 LOW VOLTAGE - 100 μ V TO 10V RANGES

5.6.1.1 Power Delivery

The basic DC range of the 4708 is 10V (19.999,999V FS). The 10V range output is derived from a buffered 'Error' amplifier, which compares the sensed output directly with the DC Reference.

For the 1V range, the DC reference is attenuated by 10:1 before being applied to the error amplifier. The error amplifier output is buffered before being applied to the I+ and I- terminals.

For the 100mV range, the 1V DC buffer output signal is reduced by a passive 10:1 attenuator before passing to the Hi and Lo terminals. The I+ and I- terminals are not used.

The 100mV attenuator also serves the 100 μ V, 1mV and 10mV ranges. Output values on these ranges are set purely by scaling the DC reference in software, and the consequent reduction in output resolution available is matched by the resolution of the OUTPUT display.

5.6.1.2 Sensing

On the 1V and 10V ranges, the input from the Hi and Lo (sense) terminals is applied to the error amplifier.

For the millivolt ranges and the 100 μ V range, there is no remote sensing. To complete the sense feedback, the 1V DC buffer output is applied directly to the error amplifier, which is configured as for the 1V range.

5.6.2 HIGH VOLTAGE - 100V RANGE

The 10V range signal is applied to the 100V power amplifier, which drives the output terminals directly from the VMOS output stage. The sensed signal is attenuated before being applied to the error amplifier.

5.7 AC VOLTAGE OUTPUTS

(Fig. 5.4)

5.7.1 SINEWAVE SYNTHESIS AND SHAPING

To control AC outputs, the frequency synthesizer and quadrature oscillator together generate a reference sinewave of stable amplitude and high purity.

5.7.1.1 Frequency Synthesis

The user-demanded frequency is related to frequency range selection, and is expressed as a binary number 'n' by the microprocessor. It is passed into guard together with binary-coded frequency-range data, to control the frequency of the synthesizer.

The binary counter in the reference divider is synchronized to the 4.096MHz master crystal-controlled clock. This counter outputs a 16kHz frequency reference signal to the synthesizer, where it is divided by two to 8kHz.

In the synthesizer, binary subdivisions of 'n' switch the capacitors of a voltage-controlled oscillator, adjusting its relaxation time-constant so as to cover five possible frequency bands within each frequency range. The VCO output frequency is divided by 'n', then phase-compared with the 8kHz reference. The integrated output from the phase comparator controls the charge and discharge current of the capacitors in the VCO.

Thus the VCO frequency is adjusted to: $n \times 8\text{kHz}$.

The frequency range data is decoded and used to define division ratios in a series of frequency dividers, which act on the output from the VCO. The result is the user-selected frequency, to an accuracy of 100ppm.

5.7.1.2 Sinewave Shaping

The quadrature oscillator is approximately tuned to the user-selected frequency by the binary word 'n', together with the decoded frequency range data, which combine to switch its circuit constants. The oscillator output is applied to a second phase comparator, and referred to the synthesizer frequency. The comparator output adjusts the oscillator frequency to that of the synthesizer.

The quadrature oscillator feedback is conditioned to ensure that its unity loop gain and its 360° loop phaseshift occur together, only at a specific amplitude, and at the synthesized frequency.

The oscillator output passes as reference sinewave to the VCA.

5.7.2 VOLTAGE-CONTROLLED AMPLIFIERS

The output from the quadrature oscillator is applied to two cascaded voltage-controlled amplifiers. The gain of the second of these (the 1V buffer) is adjusted in coarse steps; the gain of the first being adjusted in response to the error between the scaled output amplitude, and that of the quasi-sinewave reference.

The settling curve of the 7-pole filter in the precision reference divider is imposed on the 1V buffer slew rate, by using the filter's DC reference output to control the coarse gain. This signal is changed into a 10-bit word by an analog-to-digital converter, whose digital output adjusts the input resistance of the 1V buffer in steps of 1000ppm of Full Scale. As the 1V buffer is part of the error loop, this adjustment injects an undesirable scaling into the loop. Therefore, to correct the loop gain, the same 10-bit word is used to apply inverse scaling to the error signal from the comparator, before it reaches the first VCA.

5.7.3 LOW VOLTAGE - 1mV TO 10V RANGES

5.7.3.1 Power Delivery

On the 1V range, the output from the 1V buffer is passed to the I+ and I- terminals directly.

For the 10V range, the 10V amplifier (a X10 amplifier on the Power Amplifier assembly) is inserted between the 1V buffer and the I+ and I- terminals.

For the millivolt ranges, the 1V buffer output signal is reduced by switched, passive attenuators before being output via the Hi and Lo terminals.

5.7.3.2 Sensing

On the 1V range, the input from the Hi and Lo (sense) terminals is applied to the non-inverting input to the 1V/10V sense amplifier, which acts as a voltage follower.

For the 10V range, the sense amplifier is configured as a divide-by-ten inverter.

For the millivolt ranges, there is no remote sensing. To complete the sense feedback, the 1V buffer output is input directly into the sense amplifier, which is configured as for the 1V range.

5.7.3.3 Sine/Quasi-Sine RMS Comparator

The output sinewave is sensed and scaled to 1V levels before being applied to the comparator, which compares it with the reference quasi-sinewave to generate a DC signal whose value represents the output RMS error.

In a strict sense, this circuit does not compare RMS values directly. Instead, it compares the magnitudes of the mean-squares of its two inputs, but if these are equal, then the RMS values are equal. The error loop gain is virtually linear, due to the scaling applied to the error amplifier.

A cycling sequence is continuously imposed, each cycle having a duration of ten quasi-sinewave periods. During the first cycle:

- a. the reference quasi-sinewave is first squared and integrated as an analog DC signal (REF), which is memorized in a sample-and-hold circuit;
- b. the sensed sinewave input is squared, the (REF) value is subtracted, and the result is integrated and memorized as the DC (SIG) signal in a second sample-and-hold circuit;
- c. the DC (SIG) value is output as the mean-square AC error signal.

On subsequent cycles, the (REF) value is also subtracted from the squared quasi-sinewave, so that both (REF) and (SIG) signals converge to steady states as the 4708 output reaches the demanded voltage.

The mean-square AC error signal is passed through the scaled error amplifier to control the VCA.

5.7.4 HIGH VOLTAGE - 100V RANGE

The high voltage loop uses much of the low voltage circuitry; the only differences being in the power amplification to the range voltages, and the attenuation of the sensed output down to 1V range levels.

5.7.4.1 Power Delivery

On the 100V range, the 100V amplifier (on the Power Amplifier assembly) is included in the output path from the 1V buffer to the I+ and I- terminals.

5.7.4.2 Sensing

The 1V/10V sense amplifier is not used on the 100V range. Instead, a separate inverting sense amplifier reduces the sensed sinewave by a ratio of 100:1.

5.8 1000V RANGES

5.8.1 DC 1000V RANGE

(Fig. 5.3)

5.8.1.1 Power Delivery

An AC voltage-amplifier/rectifier system is employed to transform the DC Reference levels up to the high voltages required for the DC 1000V range.

The error voltage, which results from comparison between the scaled sense voltage and the DC Reference, controls the amplitude of a 16kHz AC signal output from a DC modulator. The modulated signal drives the HF step-up transformer via the 100V AC Power Amplifier. A high voltage rectifier and elliptical filter convert the AC transformer output into the DC voltage output. Output polarity is determined by a changeover switch, inserted between the rectifier and the filter.

5.8.1.2 Sensing

The sensed signal is reduced to DC Reference levels by an extensively-guarded precision attenuator, before being applied to the error amplifier.

5.8.2 AC 1000V RANGE

(Fig. 5.4)

5.8.2.1 Power Delivery

The output from the AC 1V Buffer is pre-amplified by the 1kV error amplifier, before being applied to the 100V power amplifier. The 100V amplifier output is transformed up by 1:6, then passed to the I+ and I- terminals. The error amplifier receives feedback from the transformer secondary.

To cover the full frequency range, two transformers with a frequency overlap are employed. The HF transformer is selected as frequency is increased above 3kHz, but the LF transformer is used as frequency is reduced below 3.3kHz. A second feedback loop from the LF transformer primary only, eliminates any saturation of its magnetic circuit.

5.8.2.2 Sensing

The amplifier used to sense the 100V range is also employed for the 1000V range. Although the basic amplifier is common to both, each range has its own input attenuator and feedback ratio. On the 1000V range this ratio is 550:1, and software scales the reference divider digital input to set the quasi-sinewave to values which at full scale are equivalent to 1100V RMS. The amplifier output is compared with the quasi-sinewave in the RMS comparator, the resulting error signal being used to control the output from the VCA.

5.9 OPTION 30: DC/AC CURRENT Outputs; RESISTANCE Outputs

Option 30 adds a separate PCB assembly which introduces both DC and AC Current functions, together with the Resistance function.

5.9.1 DC CURRENT (Fig. 5.3)

The DC Reference is switched to drive a voltage-to-current converter (this converter is the current amplifier used for the AC Current function).

The various ranges are selected by digital control signals from the microprocessor system. The converter shunts are switched into the output circuit to scale the current.

5.9.2 AC CURRENT (Fig. 5.4)

The ACI Reference signal is obtained by activating either the AC 10V range (used for the 1mA, 10mA and 100mA ranges), or the AC 1V range (for the 100 μ A and 1A ranges). This is switched to drive a voltage-to-current converter, followed by a current amplifier.

Range selection is the same as for DC current output.

5.9.3 10A CURRENT RANGE (Fig 5.3, 5.4)

If the 4708 is fitted with Option 30 (the resistance and current option), then it has the capability of slave mode control over the model 4600 Autocal Transconductance Amplifier, extending the AC and DC Current functions to effectively include a 10A range, controlled from the front panel or IEEE-488 interface of the 4708. An analog bus to the model 4600 carries the reference voltages (either DC or AC) which the 4600 will 'convert' to an output current, while a digital bus carries status and control signals between the 4600 and the 4708.

5.9.3 RESISTANCE (Fig. 5.3)

Eight fixed precision resistors, in a decade range (from 10 Ω to 100M Ω) are switched to the output terminals. The resistors are fully floating, being selected by relays under the control of digital signals from the microprocessor system.

5.10 DATRON 'AUTOCAL'

Precision components are used in all critical locations. Individual analog corrections for frequency-response, gain and offset errors are not applied. Instead, the accumulated errors are measured during calibration, and stored digitally in non-volatile memories.

In subsequent use, characteristic equations are applied to the stored errors to generate software corrections, which are then used to modify the reference divider ratios and so compensate for the accumulated analog errors.

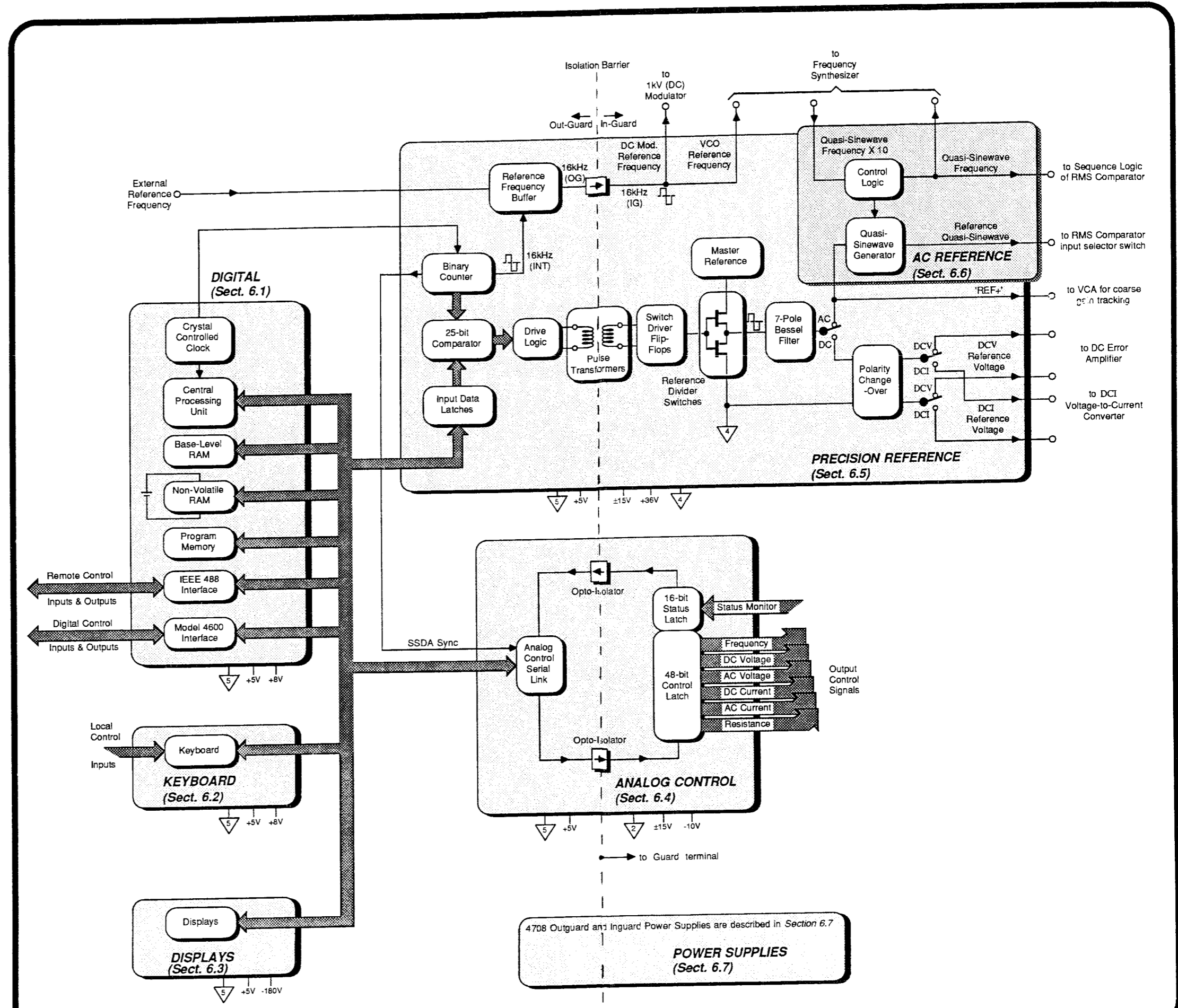


FIG. 5.2 4708 BLOCK DIAGRAM - DIGITAL, CONTROL AND REFERENCES

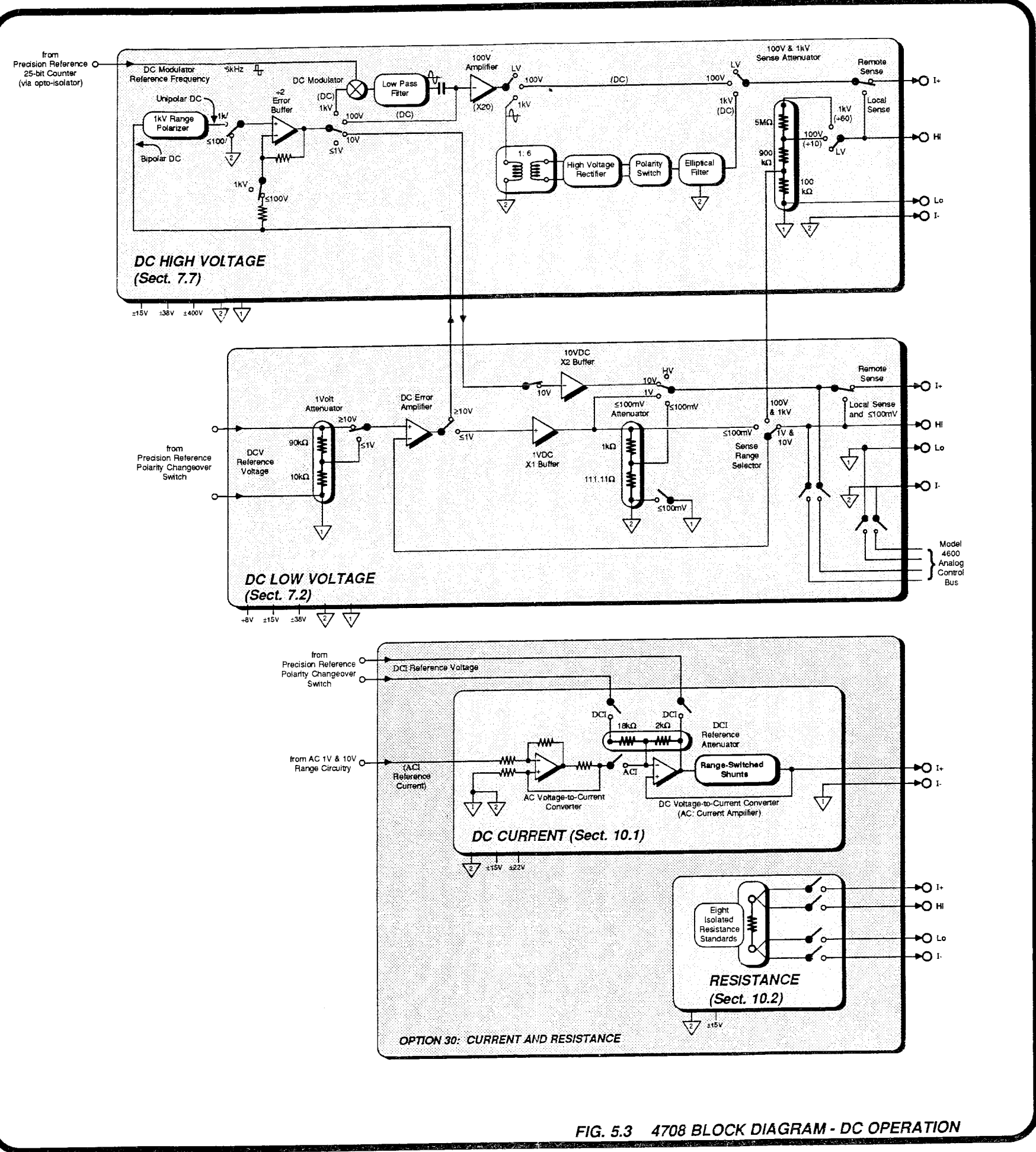


FIG. 5.3 4708 BLOCK DIAGRAM - DC OPERATION

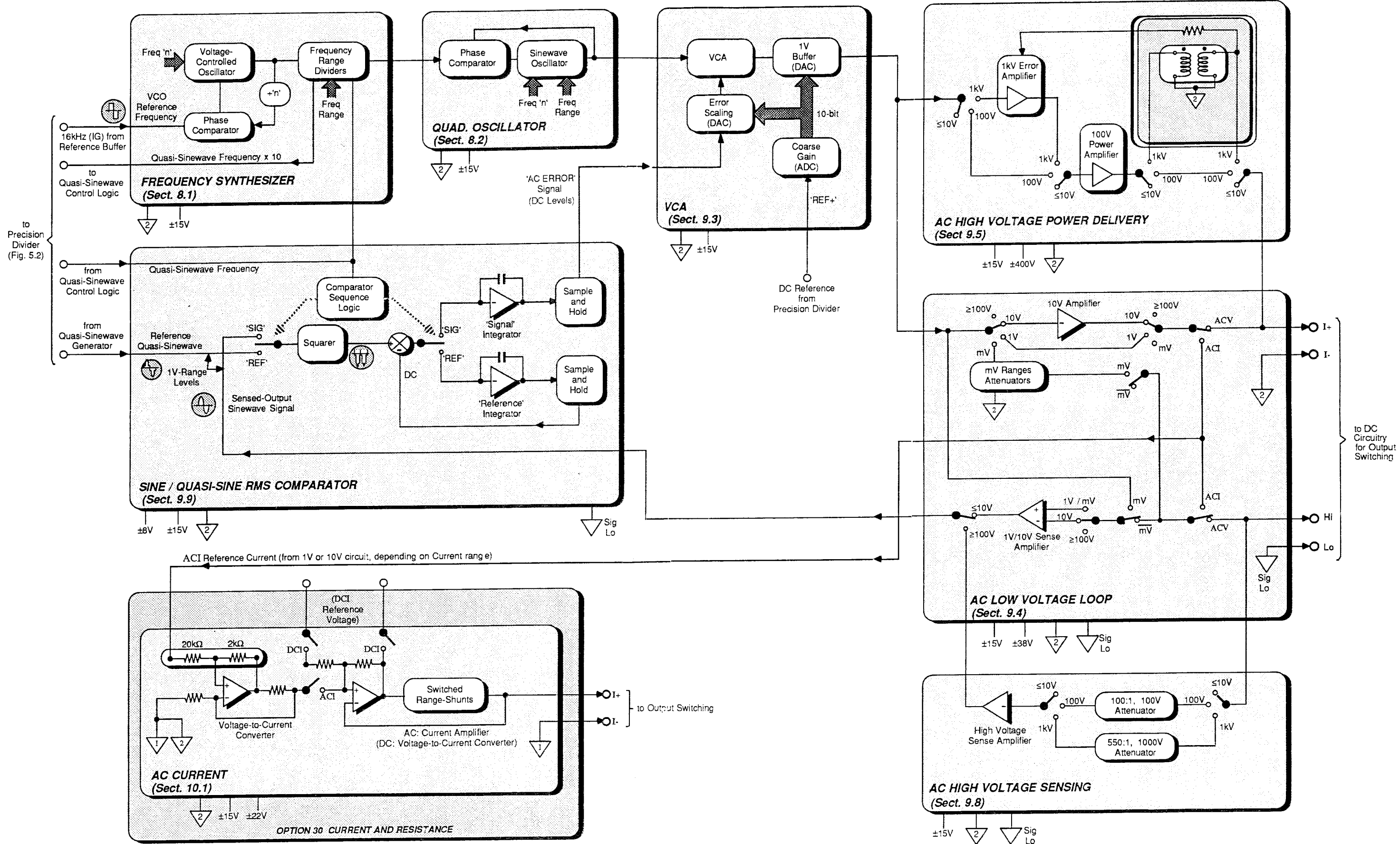


FIG. 5.4 4708 BLOCK DIAGRAM - AC OPERATION

SECTION 6

DIGITAL CIRCUITS; REFERENCE CIRCUITS; POWER SUPPLIES

6.1 DIGITAL

The circuits described in this sub-section perform the following functions:

- Central processing, with supporting memory, for management of instrument operation.
- Storage of calibration constants in non-volatile memory.
- Generation of Master clocks, with clock-waveform shaping.
- Address decoding to generate control signals.
- Controlled power-up and power-down of digital circuits.
- Servicing IRQs from asynchronous sources.
- Interfacing the instrument to the IEEE 488 bus.

The functions are performed by circuits located mainly on the Digital Assembly (400796). Master Clock generation, synchronization and division is carried out by circuits on the Analog Interface Assembly (400648).

Fig. 6.1 shows the arrangement and main interconnections of the central digital circuits.

6.1.1 GENERAL

The instrument is managed by a 6802-series micro-processor system, under the control of an operating program held in 26k bytes of EPROM. All front and rear panel controls provide direct inputs to the system, except for the Power ON/OFF switch and Safety Reset Key. The system ensures that the processor reverts to a safe state on power-up and power down.

Work space and stack is provided by 2k bytes of random-access memory (RAM). A further 2k bytes of CMOS RAM act as a non-volatile memory to hold calibration constants, powered by a back-up Lithium battery when the instrument is turned off.

6.1.1.1 Synchronous Operation

The operating program manipulates the internal circuitry by activating control signals. These result from providing peripheral decoders with specific address combinations. The program is run at 680kHz cycling frequency, originally derived from a 4.096MHz master crystal oscillator.

6.1.1.2 Asynchronous Operation

Any Key operation (other than Safety Reset), or one of two internal conditions, will initiate an asynchronous interrupt (IRQ) which suspends the CPU's current task. The CPU absorbs the new instructions, rearranges its schedule to conform to the demanded new configuration, then continues with the interrupted task until it is completed. Finally it returns to the initial operation of the amended schedule and proceeds synchronously.

Three main sources of interrupt are used:

- Remote Command via the Digital Interface
- Keyboard Command
- Real-time Clock Pulses (8ms intervals)

The CPU identifies the source by polling the data bus each time it receives an IRQ interrupt.

6.1.1.3 Output Generation

From user inputs of output value, frequency, error and calibration constants, the CPU computes a binary value to a resolution of 25 bits. This is used to adjust the mark/period ratio of the Reference Divider switch which ultimately controls the Working Reference Voltage for the output analogue circuitry.

6.1.1.4 Display Refresh

The gas discharge display is continuously refreshed by cycling through character data stored in a separate display-image RAM. To alter the display the processor merely alters the contents of the RAM.

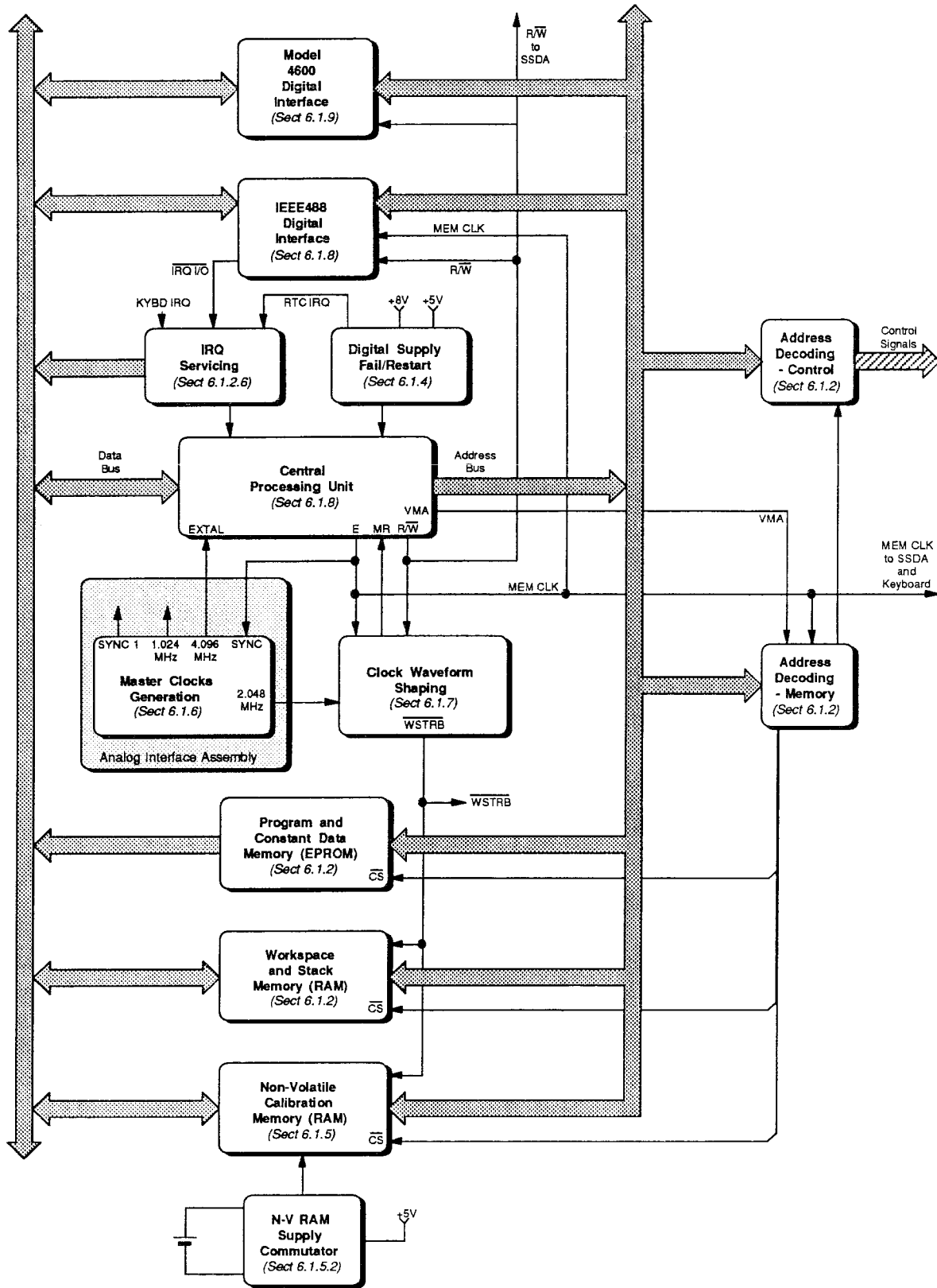


FIG. 6.1 DIGITAL FUNCTION BLOCK DIAGRAM

6.1.2 CENTRAL PROCESSOR and PROCESSOR MEMORY

(Circuit Diagram 430796 Pages 11.2-2 and 11.2-3)

A 6802 microprocessor (M34), together with its memory, controls communication throughout the whole instrument.

6.1.2.1 Memory

The memory can be split into four main areas, the microprocessor RAM not being used:

- **Program Memory** (M18, M19, M20 and M21) defines and controls the operational functions of the whole instrument system.
- **Constant Data Memory** (held in EPROM with the Program Memory) - stores fixed factors used in processing; such as the key mapping tables, and the instrument specification tables that are used in 'Spec' Mode.
- **Non-Volatile Calibration Memory** (M23) - stores all the calibration constants used to correct each output value, which are determined during the 'Auto-cal' cycle.
- **Volatile Operating Memory** (M22) - used for volatile data storage such as display images, computation results and present output value. This memory is also used for scratch pad operations.

Separate memory is used for special purposes, such as the Display Image RAM M16 (which is synchronously loaded but asynchronously read); the storage areas in the IEEE 488 GPIA (M29) and the Keyboard Interface (M6 on Front Assembly); and the Memory Address decoder PROM (M3). These are described in later sub-sections.

6.1.2.2 Central Processing Unit

(Circuit Diagram 430796 Page 11.2-2)

The MC6802 (M34) is a monolithic 8-bit micro-processor, with interrupt and clock-stretching facilities. It is driven by a single phase 4.096MHz square wave generated by the Master Clock X1 in the Analogue Interface Assembly. (This clock synchronizes the reference divider switch with the processor cycle).

6.1.2.3 Address and Data Lines

Address lines A₁₅₋₁₁ are decoded as chip-select signals for the RAM/ROM circuit, lines A₁₃₋₀ are connected to the instrument address bus. Data lines D₇₋₀ are linked via programming plug JL1 to the instrument data bus.

6.1.2.4 E, MR and MEMCLK

The 4.096MHz clock input at M34-39 (EXTAL) is divided by four and used as output at M34-37 (E). Although the natural frequency of E is 1.024MHz, the action of the waveform shaping input to MR reduces it to approx. 680kHz as MEMCLK for the IEEE 488 interface; and for the Analogue-Interface and Front assemblies.

6.1.2.5 $\overline{\text{NMI}}$

The internal switch S1 provides a non-maskable hardware interrupt which has two functions.

- With the external CALIBRATION switch set to RUN, $\overline{\text{NMI}}$ initializes the processor system.
- With the CALIBRATION switch set to ENABLE, $\overline{\text{NMI}}$ clears the non-volatile calibration memory (M23) before initializing the processor system.

6.1.2.6 $\overline{\text{IRQ}}$

Any one of three asynchronous Interrupt Request signals are able to activate the maskable $\overline{\text{IRQ}}$ input at M34-4:

- **RTC IRQ** is a real-time clock occurring every 8ms to provide timing information for the processor's monitoring facility.
- **KYBD IRQ** occurs each time a front panel key is pressed. (Not Safety Reset).
- **IRQ IO** occurs when the IEEE 488 Interface has a transaction to communicate to the processor.

D1, D2 and Q1 constitute a DTL OR-gate to isolate the IRQ inputs. On receipt of Logic-0 on pin 4, M34 stores its register contents in stack RAM, and vectors to IRQ service addresses FFF8 and FFF9, saving the current processor environment.

The IRQ Service Routine addresses M51 and M52, setting Logic-0 at M52-9 which enables the tristate buffers M36 and M37 (at M36-1 and 15, M37-15). This sets IRQ data bits D₅, D₆ and D₇ on the data bus so that the processor can identify the source of the IRQ and select the appropriate sub-routine to service the interrupt request.

The IRQ inputs are released as part of the service sub-routine, and after its completion, the processor recovers its environment from stack RAM and proceeds with the interrupted operation.

6.1.2.7 Software Interrupt

The 6802 will also recognise Opcode 3F on the data bus as an interrupt request ('Implied' addressing mode). This code is hard-wired via R9, R10 and AN3 onto the data bus so that if the CPU tries to access a non-available address, the floating bus will be pulled to 3F, initiating the software interrupt. The CPU vectors to FFFA and FFFB, whose contents cause the 6802 to re-initialize the system.

6.1.2.8 Read-Write Line $\overline{\text{R/W}}$

The processor sets the $\overline{\text{R/W}}$ line to Logic-1 when it is in Read state, and Logic-0 when it has data to write into the addressed device. The $\overline{\text{R/W}}$ signal is passed only to the SSDA on the Analogue Interface assembly, and to the IEEE 488 GPIA (M29). All other devices which require read-write control, operate from the $\overline{\text{RD STRB}}$ and $\overline{\text{WRT STRB}}$ signals generated from $\overline{\text{R/W}}$ by M49/50.

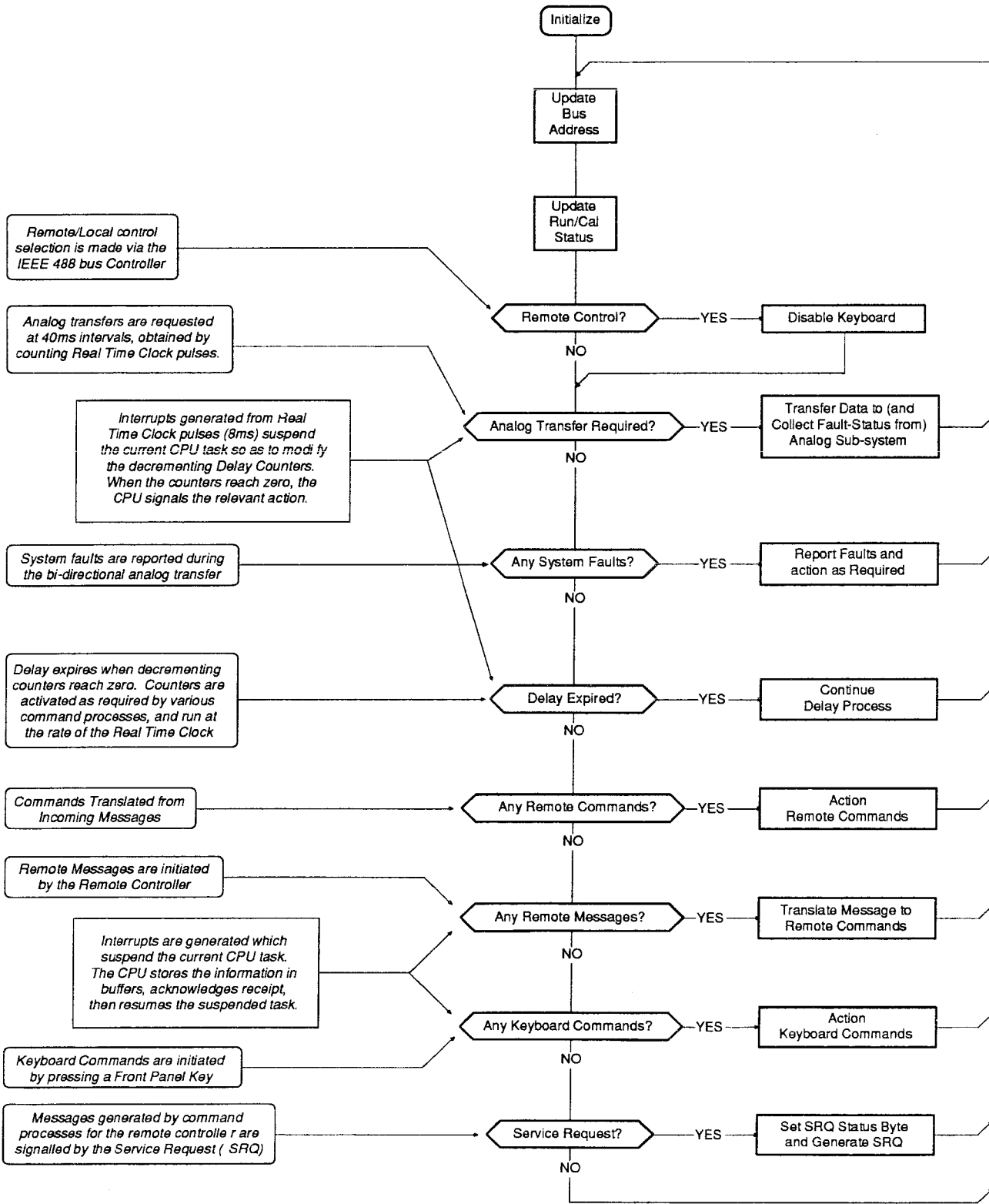


FIG. 6.2 SOFTWARE OVERVIEW

6.1.3 SOFTWARE OVERVIEW

The software management organization is shown in *Figure 6.2*. The machine cycle progresses through the task schedule as illustrated, being interrupted by the demands of activities dependent on real time, and those dedicated to local and remote commands. Real time and

command interrupts suspend the current activity of the processor so that the immediate task can be serviced. The processor then resumes the suspended task and continues with the programmed routine, accounting for any alterations introduced by the interrupt.

6.1.4 DIGITAL SUPPLY: FAIL/RESTART CIRCUITRY

Power-up, restart and shut-down of the digital circuitry are performed in a controlled sequence to safeguard against both hardware and software failures. The Safety Monitor ('Watchdog' - *Section 6.4.6*) maintains a continuous surveillance of the software management, and shuts down the instrument in the event of a failure either in the digital control circuits or in software management.

6.1.4.1 Power-up Sequence (Circuit Diagram 430796 Page 11.2-2)

Power-on is first sensed by the Supply Fail Detector circuit. This draws its supplies from the +8V DC unregulated supply, which is the first of the power supplies to rise to a working level. The comparator circuit of M28 has a nominal threshold of +7.1V, above which a good working level of the +5V DC supply is assured.

As the +8V supply rises, but still below +7V, M28-2 follows until the Zener D6 avalanches, when it is held at +2.45V. At this level M28-3 voltage is less than 1V, so M28-1 remains at 0V holding the 'D' input of M8-5 at Logic-0 and M7-3 at Logic-1. Thus M8 and M9 are held in reset, initiating and maintaining the following states:

- a. M8-2 (\bar{Q}) at Logic-1, PWR ON RST active. This signal is fed to the Front Panel assembly, holding the keyboard encoder M6 in reset, and disabling the LED cathode driver decoder M4.
- b. M6-4 at Logic-0, $\overline{\text{PWR ON RST}}$ active. This signal holds the microprocessor M34 in reset state. The VMA output at M34-5 is held at Logic-0, disabling address decoder M3, setting all M3 address outputs to Logic-1. This combination sets M5-13 to Logic-1, but the Logic-0 at M6-2 sets Logic-1 at M5-11, ultimately setting Logic-1 at M7-2.

The Logic-0 of $\overline{\text{PWR ON RST}}$ also holds the IEEE 488 GPIA M29 (*page 11.2-4*) in reset. It is also fed to the Analog Interface assembly where it holds the SSDA M44 in reset.

When the +8V supply rises above about +7.1V, M28-3 voltage rises above the +2.45V on M28-2, so M28-1 rises to place a Logic-1 both on M8-5 (D input) and M7-1. M7-3 thus falls to Logic-0, removing the resets from 14-bit counter M9 and restart flip-flop M8. So M8 is enabled to receive its clock from M9, which itself starts to count its own 2.048MHz clocks.

At full count, 8ms after M9 is enabled, M9-3 clocks M8. As M8 'D' input is already at Logic-1, this is clocked to M8-1 (Q), with Logic-0 to M8-2 (\bar{Q}). The PWR ON RST and $\overline{\text{PWR ON RST}}$ signals revert to their inactive states, and start-up proceeds:

a. PWR ON RST at Logic-0:

On the Front assembly, enables keyboard encoder M6 and LED cathode driver decoder M4.

b. $\overline{\text{PWR ON RST}}$ at Logic-1:

- i. Removes reset from CPU M34, allowing the software to initialize; and also removes the reset from the IEEE bus controller M29 (*page 11.2-4*).
- ii. Removes the reset from the SSDA M44 on the Analog Interface assembly.

c. M8-1 to Logic-1:

- i. Provides an enabling input to M10-1 (See Non-Volatile RAM Supplies - *Section 6.1.5*).
- ii. Triggers monostable M53-4. This monostable has a relaxation period of 470ms, during which time it holds the $\overline{\text{FP RST}}$ output at Logic-0. On the Reference Divider assembly this allows the Watchdog circuits to reset. (See *Section 6.4.6*)
- iii. Enables the 'Real-Time Clock' IRQ via M7-13 and flip-flop M8-10. The actions of M9, M8 and M51 interrupt the software routine every 8ms. 'RTC IRQ' sets five external states onto lines D₄₋₀ of the Data bus (M36 and M37), and forces the CPU to observe them.

Address decoder M51-5 is normally held at Logic-1, so the Logic-1 at M7-11 and M8-10 allows M9-3 clock to affect the RTC IRQ output at M8-13. For so long as the +8V supply holds above +7.1V, M9 continues cycling through its full count, clocking M8-11 to initiate the RTC IRQ at 8ms intervals.

The CPU terminates each RTC IRQ service sub-routine by addressing M51, pulsing M51-5 (M7-12) to Logic-0 (Real-time clock reset 'RTC RST'). M7-11 and M8-10 are pulsed to Logic-1, resetting M8-13 (RTC IRQ) to Logic-0. At the next full count of M9; M8-13 is once again clocked to Logic-1, initiating another RTC IRQ.

Pulses from M9-3 regularly clock the binary state of M8-5 through to M8-1, monitoring the supply status. When running normally, M8-5 and M8-1 are both at Logic-1. If the supply fails, M8-5 reverts to Logic-0, but M7-1 at Logic-0 provides a fast reset setting M8-4 to Logic-1 without waiting for the next clock pulse. M7-3 also resets the 8ms counter to zero count at M9-11.

6.1.4.2 CPU Re-start

(Circuit Diagram 430796 page 11.2-2)

Memory addressing by the CPU is monitored by the NAND logic of M4, M5 (four elements) and M7-3. In the correct addressing sequence there are two basic conditions:

- **Invalid memory address:**
CPU VMA = Logic- \emptyset ,
and M3 outputs (D \emptyset -7) = Logic-1.
- **Valid memory address:**
CPU VMA = Logic-1
CPU E = Logic-1
M3 outputs (D \emptyset -7) = One address line set to Logic- \emptyset

Both these conditions disable M5-11, setting a Logic- \emptyset at M7-3 which allows the clock M9 and flip-flop M8 to function normally. The possibility of a glitch occurring at the change-over between the two conditions is gated from the control line by switching at M5-5.

Incorrect addressing sequence in the CPU would be shown by:

- CPU VMA = Logic-1, and E = Logic-1, the CPU indicating that it has selected a valid external address;
- All M3 outputs = Logic-1, no address is selected.

This situation is most likely with a software failure. The logic control path via M4 and M5 now gives a Logic- \emptyset at M7-2 and thus a Logic-1 at M7-3 which:

- Resets counter M9 to zero;
- Forces M8-1 to Logic- \emptyset . This forces RTC RST at M7-11 and removes an enable from M10-1.
(See Non-Volatile RAM Supplies *Section 6.1.5*)
- Forces M8-2 to Logic-1. This change:

Resets the CPU by M34-40 to Logic- \emptyset . VMA is forced to Logic- \emptyset which in its turn removes the reset from M9-11 and M8-4 via M6-2 (Logic- \emptyset), and the M4/M5/M7 control path.

Makes PWR ON RST and $\overline{\text{PWR ON RST}}$ signals active, thus resetting the other software-controlled areas.

After 8ms from CPU reset, flip-flop M8-3 is triggered from clock M9. M8-1 and M8-2 change state and the start-up sequence proceeds again.

6.1.5 NON-VOLATILE RAM

6.1.5.1 'NV INHIBIT' Signals

(Circuit Diagram 430796 pages 11.2-2 and 11.2-3)

Chip-select to the non-volatile memory M23 is inhibited during power-up, re-start and power-down operations, by the logic signal 'NV INHIBIT' being set to Logic-1. During normal running this signal reverts to Logic-0. With the $\overline{\text{NV INHIBIT}}$ signal at Logic-1 (M10-4) during normal running; write access to the NV RAM is available, but only enabled if the calibration security keyswitch on the rear panel is set to ENABLE. The NAND logic gates M10, used to control the inhibit, remain powered from the RAM standby supply after power-down.

Conditions for normal running are as follows:

- Supply fail detector circuit provides a Logic-1 (supplies valid) output to opto-coupler M11. This action causes its optically-coupled transistor to conduct and hold M10-2 at Logic-1.
- M10-8 is held at Logic-1 (to +5V via R6).
- M10-1 is held at Logic-1 by flip flop M8-1.

The above conditions ensure a Logic-1 output from M10-10 (by holding $\overline{\text{NV INHIBIT}}$ inactive).

During power-up, $\overline{\text{NV INHIBIT}}$ is held active until the power supplies have settled and the CPU has gained control of memory:

The input to M10-8 is delayed on the +5V supply by the time-constant C8, R6. Also, the input to M10-1 is held at Logic-0 by flip-flop M8-1 until the CPU reset is removed.

At power-down, or in the event of a supply failure, $\overline{\text{NV INHIBIT}}$ becomes active before +5V supply fails:

The first indication of supply failure is made by supply fail detector M28 output going to Logic-0. This cuts off the opto-coupler M11 which takes M10-2 to Logic-0. M10-8/12/13 are held at Logic-1 by the +5V supply, thus M10-9 is taken to Logic-1 and M10-10 to Logic-0 ($\overline{\text{NV INHIBIT}}$ active).

In the event of a CPU reset, the $\overline{\text{NV INHIBIT}}$ is made active for the period of reset by the switching action of M8-1 and M10-9.

6.1.5.2 Supply Commutator

(Circuit Diagram 430796 page 11.2-3)

This circuit provides the non-volatile RAM M23 with a battery-driven standby supply when the instrument is in the power-down condition. It also ensures continuity of supply during the change-over period between normal (line) operation and standby, minimizing battery current leakage.

In the power-down condition, the battery powers M10 and M23, returning from battery common (TP13) via D7 and R60. The battery common is isolated from the general common 5A by transistor Q2, which is cut-off.

During power-up, M28 is powered from the +8V supply before the +5V supply voltage becomes established. As long as the +5V supply voltage is less than the battery voltage, Q3-4 is biased negatively, and Q3 is unbalanced in favour of heavy conduction through Q3-6. M28-5 is held low, and M28-6 high as the +5V supply voltage increases, so M28-7 remains at Common-5A potential, and opto-coupler M39 is not energized. Q2 stays off, maintaining isolation of the battery supply from Common-5B. M10 and M23 remain powered from the battery.

As the +5V supply voltage increases, D7 cathode potential rises, reducing Q3-4 bias, reaching zero when the supply voltage is equal to the battery voltage (less than 10mV is developed across R60).

When the +5V supply voltage exceeds the battery voltage, Q3 becomes biased in favour of heavy conduction through Q3-2, pulling M28-6 low and reversing the differential input to M28. M28-7 rises to the +8V rail and energizes the opto-coupler M39, which switches Q2 on, connecting common-5A to the battery common. M10 and M23 are now powered from the +5V supply and the standby battery is isolated by reverse-biased diode D7.

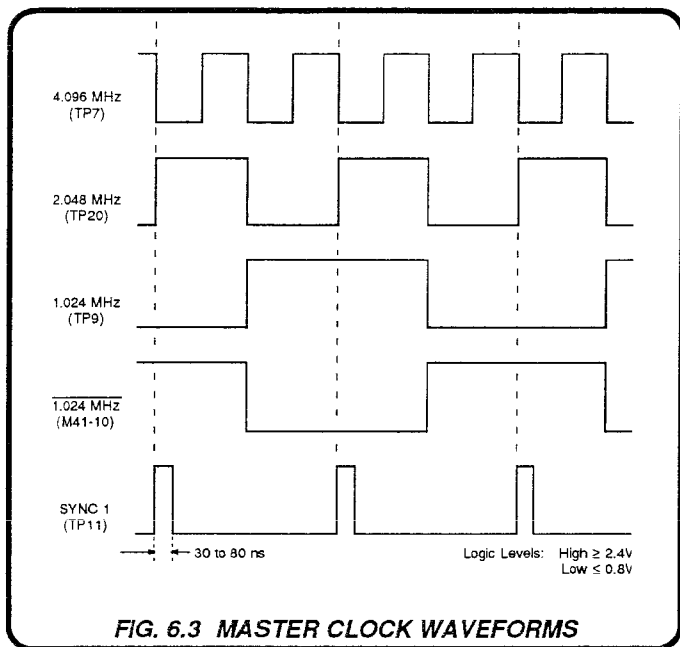
During power down, Q3 compares the +5V supply against the battery, switching Q2 off via M28 and M39 when the +5V supply voltage falls below the battery voltage, and the non-volatile RAM supply commutates to standby battery. Alternatively, Q2 is switched off by failure of the +8V supply to M28 if this occurs before the +5V supply voltage falls below the battery voltage.

Eventually the +5V and +8V supplies both fall to zero, the battery provides the supply to the non-volatile RAM, and battery common is isolated from Common-5A by Q2.

6.1.6 MASTER CLOCK GENERATION

(Circuit Diagram 430648 page 11.3-3)

(Refer to Fig. 6.3 for waveforms)



The master clock generator is based on crystal oscillator X1 which provides a precision 4.096MHz squarewave reference frequency output.

The primary frequency of 4.096MHz is divided by JK flip flop stages M41, both of which are connected to toggle when clocked. The first division stage is synchronized at its reset input, M41-3, to the memory clock via flip-flop M42. This ensures correct phasing of the 2.048MHz squarewave output from M41-14.

M41-11 and M41-10 outputs provide complementary 1.024MHz and 1.024MHz squarewaves respectively. Monostable M40, which is triggered at 2.048MHz from M41-15, provides the positive-going 2.048MHz synchronizing pulses, SYNC1.

6.1.7 CLOCK WAVEFORM GENERATION

(Circuit Diagrams 430796 page 11.2-2

and 430648 page 11.3-3)

NB As the circuit locations in Fig 6.4 are clearly marked, and as there are no duplicate designators in the circuits, this description does not refer to a component's location except where necessary.

NOTE To avoid confusion, the terms 'high' and 'low' are used to replace 'Logic-1' and 'Logic-0' respectively in the following description.

The crystal oscillator on the Analog Interface Assembly provides a 4.096MHz Master Clock signal (X1-8) for the whole instrument. This drives the 6802 CPU at M34-39 (EXTAL) so M34-38 is not connected. M41 divides 4.096MHz to generate a 2.048MHz clock for the Memory Clock Stretching Circuit (M35/M49).

The CPU (M34) divides the EXTAL input internally by 4 and outputs the result as E (Enable) at M34-37, to act as a 'Phase 2' Memory Clock for the SSDA on the Analog Interface and the keyboard controller on the Front assembly.

If M34-3 (MR-Memory Ready) were permanently held at +5V, the E signal would be 1.024MHz. But in the 4708, a 'stretching' circuit (M35/M49) doubles the Logic High (+5V) time of E by switching MR to Logic Low (0V) for part of the cycle. This is shown on Fig.6.4.

The frequency of E is thus reduced to approximately 680kHz, with 1µs available for data access to the SSDA, Keyboard Controller, IEEE GPIA and memory.

6.1.7.1 Memory Clock Stretching Circuit

(Fig. 6.4)

The action of M35 and M49 is dependent upon the finite propagation time between clocks at M35-1/M35-6 and Q output at M35-15. When M34-3 (MR) is +5V; M34-37 (E) is toggled by alternate positive-going edges of the 4.096MHz clock, with a propagation delay of approximately 80ns. Also, the 4.096MHz signal is divided by 2 in M41, resulting in 2.048MHz signal whose negative-going edges clock M35. M35 cascade action is controlled by the condition of the Memory Clock (E) and affected by its own propagation times.

6.1.7.2 Shaping Action (Figs. 6.4 and 6.5)

At T1 and T2: The 4.096MHz clock edge at T1 causes E to rise from low to high at T2. As M35-10 is also high, MR changes from high to low at T2, holding E high. M35 pin state is 4 and 10 high, 9, 12 and 16 low.

At T3: The 2.048MHz falling edge clocks M35, and M35-9 rises to high awaiting the next clock edge (not until T5). M35-10 also remains high, so MR is held low and E stays high.

At T4: MR is still low, so the 4.096MHz clock has no effect on E, and E is stretched.

At T5: MR returns to high when the Logic-1 on M35-9 is clocked as a Logic-0 to M49-4. This allows the 6802 to toggle E at the next effective clock edge.

At T6: The rising edge of the 4.096MHz clock causes E to fall to low, setting up M35-4 to low, M35-12 and 16 to high. (M35-9 is already high.)

At T7: M35-10 is toggled to high, but as M49-5 is now low, MR remains high to allow E to be toggled at the next effective processor clock edge (not until the next T1). Also at T7, M35-15 is clocked to low to set M35-9 ready for the next (T3) clock edge. The circuit is now set up to its initial (pre-T1) condition so the action repeats.

Note:

A remote possibility exists, that a severe disturbance could upset the synchronization of the 'E' signal with the 2.048MHz clock. To guard against this, M42 acts as a monostable to provide negative reset pulses into M41-3. Under all normal conditions, these will occur when M41 is already toggled in its reset state.

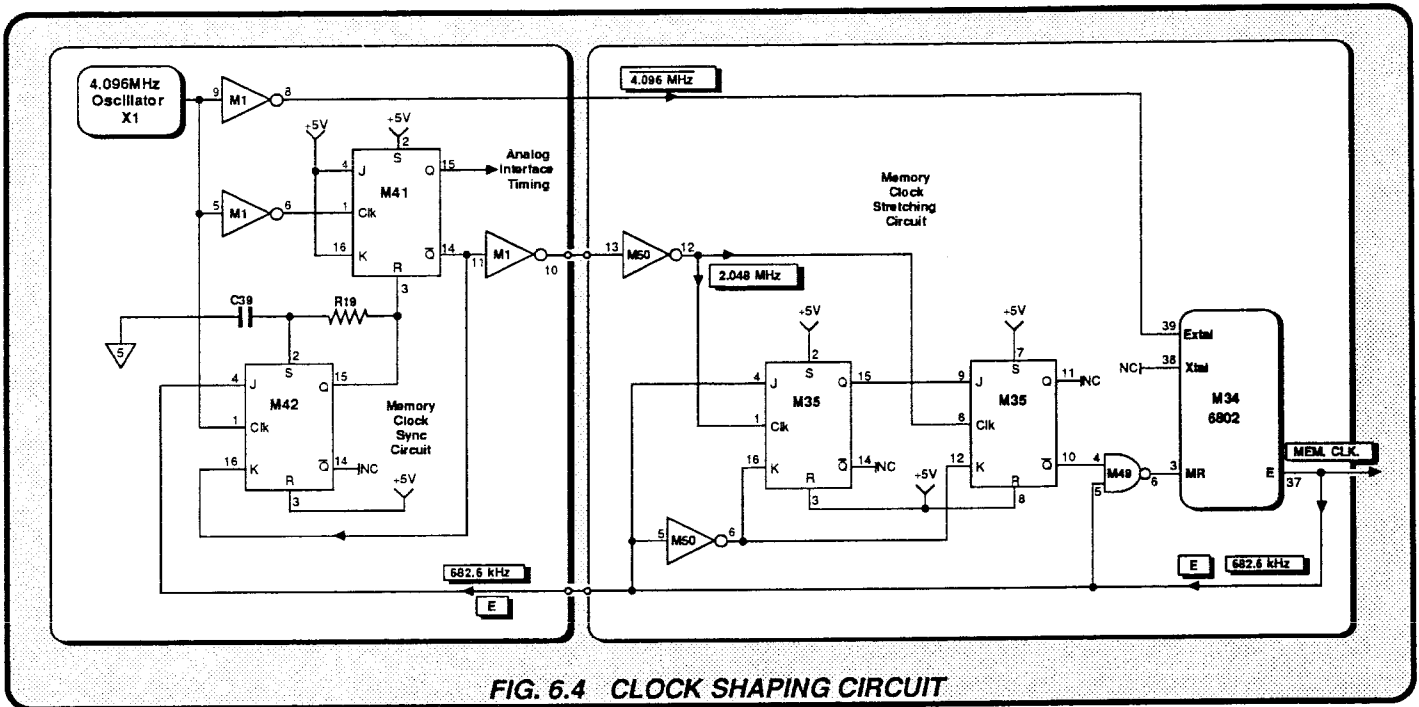


FIG. 6.4 CLOCK SHAPING CIRCUIT

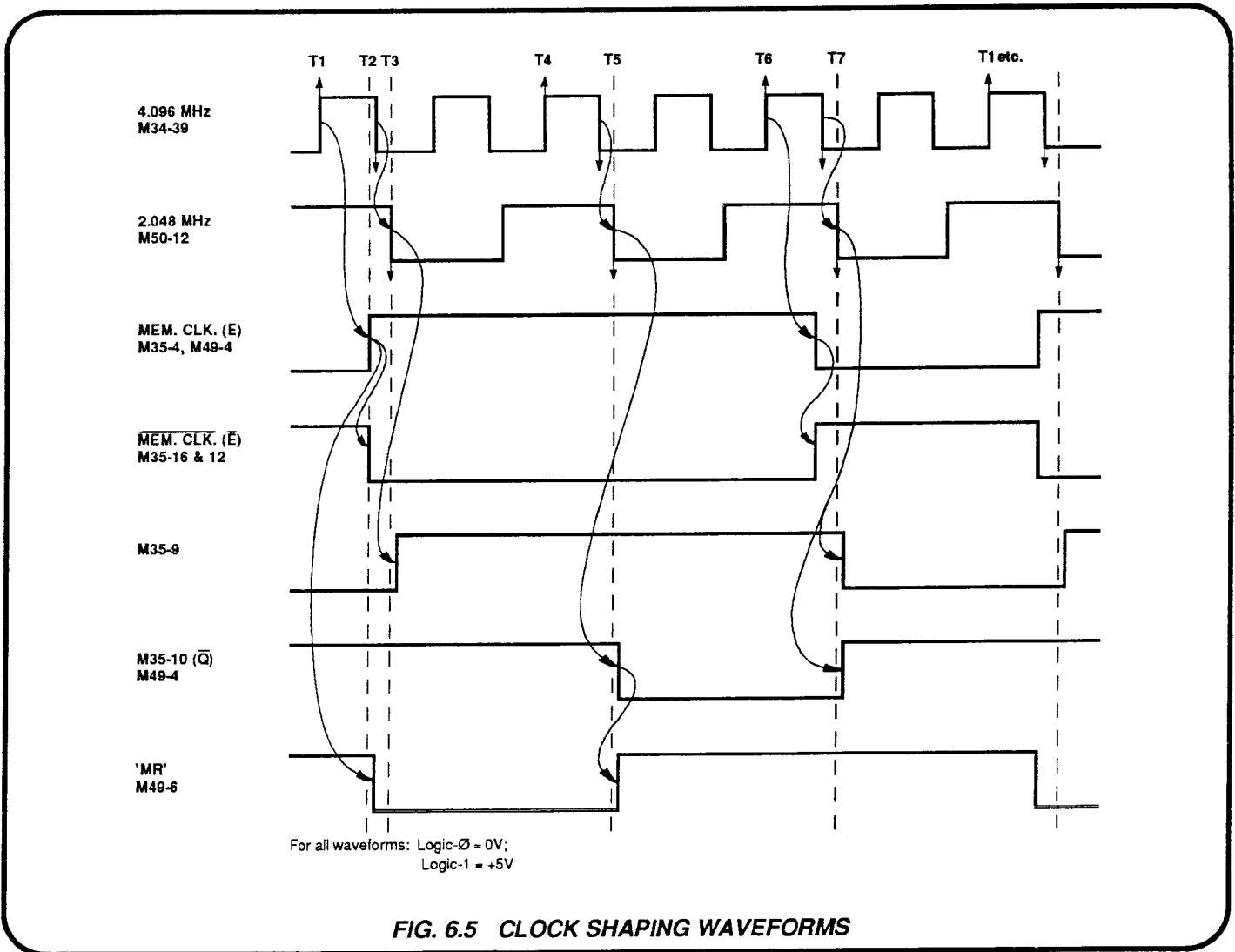


FIG. 6.5 CLOCK SHAPING WAVEFORMS

6.1.8 IEEE 488 DIGITAL INTERFACE

(Circuit Diagram 430796 Page 11.2.4)

The IEEE Interface circuitry is located on the bottom right-hand corner of the Digital PCB (viewed from the front of the instrument). M29, M40, M47 and M48 execute and decode interface functions, and transfer data (input/output).

The General Purpose Interface Adaptor (GPIA) M29, is software-driven by the 6802 CPU, as part of its normal function. M29 is addressed at CS by $\overline{\text{XIOBBD}}$ from M51, and its internal registers are accessed by A_0 , A_1 and A_2 from the address bus.

The GPIA is clocked by Memory Clock E, with read or write control direct from the processor R/W signal at M29-5; and at instrument power-on, the signal $\overline{\text{PWR ON RST}}$ from the Restart Generator circuit (M6-4) initializes M29 at M29-19.

Information is passed between M29 and the CPU (M34), via the data bus D_0 - D_7 . The address switch data is linked to D_0 - D_6 by tristate buffers M47. During initialization and at subsequent intervals, the state of M29-4 (ASE) changes from +5V to 0V, enabling M47. The status of the address switches on the 4708 rear panel is transferred into M29 via M47 and the data bus for comparison with the received address.

M40 and M48 are bidirectional bus-driver arrays. The drivers for bus management lines: IFC, ATN and REN are permanently held in Receive state, and the SRQ driver in Transmit state. The EOI line

driver is switched from Receive to Transmit by M29-28 ($\overline{\text{T/R1}}$) changing from 0V to +5V as required by M29. M29-27 ($\overline{\text{T/R2}}$) is normally held at 0V for reception of system data via DIO_{1-8} bus lines, and set to +5V for instrument data to be sent over the bus.

Some system controllers output excessive noise along the REN line. To avoid spurious switching of M29 between Local and Remote control states, the noise is filtered by R58 and C31.

Difficulty has been experienced with certain controllers in that NDAC can transfer data on to the bus too early. Resistor R62 and capacitor C7 slow down the transitions of NDAC to overcome this problem.

M29-40 ($\overline{\text{IRQ}}$) is used to inform the CPU when certain states occur. In particular, the $\overline{\text{IRQ IO}}$ signal is generated at each byte-transfer over the bus, whether the byte is sent or received. Additionally, $\overline{\text{IRQ IO}}$ is activated whenever certain specific commands are received, e.g: 'DAC', 'SPA', and changes between Remote and Local Status.

When the CPU receives $\overline{\text{IRQ IO}}$, it addresses M29's 'Interrupt' Status Register, then M29 identifies the reason via the instrument data bus.

For further information refer to 'Getting Aboard the 488 Bus' published by Motorola, or the appropriate device data sheets.

6.1.9 MODEL 4600 DIGITAL INTERFACE

(Circuit Diagram 430796 Page 11.2.3)

The processor communicates with the 4600 using 9 signals in the digital bus. Eight signals are controlled by the processor using the PIA M26, which drives the digital bus via the IEEE bus buffer M25. The signal IDIGBUSON is driven from +5V (circuit diagram 430604-2.0 page 11.16-4) so that the model 4600 may detect that the 4708 is turned on.

The data on the digital bus IAD0 to IAD4 is bi-directional so model 4600 control data can be written from the model 4708, and status information read back. Writing occurs when signal $\overline{\text{IWR}}$ pulses low and reading occurs when the signal $\overline{\text{IRD}}$ pulses low. When $\text{IA}/\overline{\text{D}}$ is low, they are in data mode as described, when high, they are in

address mode. The address mode is used during a write or read to determine which address is to be written or read. The 4600 latches the address on lines IAD0 to IAD4 when $\text{IA}/\overline{\text{D}}$ is high and $\overline{\text{IWR}}$ pulses low. All subsequent writes and reads are to this address until another address is latched. The 4600 uses only addresses 0,1,2 and 3. The remaining addresses 4 to 31 are reserved for future expansion.

The processor reads the 4600 status registers each 40ms to check for malfunctions, that the analog bus is connected, and the status of the on/off keys. The digital bus is reset by driving both $\overline{\text{IWR}}$ and $\overline{\text{IRD}}$ low, either by the processor or M24 (ie BARK DEL (OG) is set).

6.2 KEYBOARD

(Circuit Diagram 430558 Page 11.1-1)

The circuitry described in this section performs the following functions:

- Provides front-panel operator control of instrument Output, Function, Range and Mode circuitry, by push-button keys. Key operation is detected internally and transferred to the CPU via the instrument data bus.
- Indicates the present instrument state by means of LEDs fitted in the keys.
- Generates audible warning of errors, failures, and high voltage at the Output Terminals.

(Also see Circuit Diagram 430648 Page 11.3-3)

In addition a rocker switch sets instrument Power ON and OFF (refer to Section 6.7) and a 'Reset' key provides a hardware reset for the safety monitor (Watchdog) circuits (refer to Section 6.4). The circuitry is located on the Front PCB Assembly (400558), linked to the CPU by control signals and the data bus.

6.2.1 KEY and LED MATRICES

The keys are electrically arranged in an 8 x 7 matrix as shown in the circuit diagram. The seven columns are scanned by M5; any key contact is detected on one of the eight return lines RL₀₋₇, memorized by M6, and signal KYBD IRQ is passed to the CPU. The CPU responds by interrogating M6 Keyboard memory and acting on the specific key command.

The LEDs in the keys are electrically arranged in an 8 x 4 matrix. The four rows are scanned by M4, and the eight columns receive the appropriate bit patterns from M6 display memory. This memory is up-dated as required from the CPU data bus D₀₋₇.

6.2.2 PROGRAMMABLE INTERFACE M6

(Fig. 6.6)

M6 interfaces the keyboard and LEDs to the instrument data bus. It is addressed by $\overline{\text{KYBD CS}}$ from the Digital assembly, to chip-select $\overline{\text{CS}}$ which enables commands or data to flow via the data bus at DB₀₋₇. The CPU sets address A₀ to Logic-0 for data flow; but for programming the interface for mode change or during initialization, A₀ is set to Logic-1.

6.2.2.1 Read/Write Control

The $\overline{\text{WRT STRB}}$ signal from the Digital assembly is applied to M6 $\overline{\text{WR}}$. Data or Command is input to M6 from the CPU data bus during $\overline{\text{WR}}$ low and $\overline{\text{CS}}$ low, and is latched on the $\overline{\text{WR}}$ positive-going edge.

The $\overline{\text{RD STRB}}$ signal from the Digital assembly is applied to M6 $\overline{\text{RD}}$. Data is output from M6 on to the data bus during $\overline{\text{RD}}$ low and $\overline{\text{CS}}$ low.

6.2.2.2 M6 Initialization

Switching power on to the instrument causes M6 to be cleared by the PWR ON RESET pulse from the Digital assembly. The interface is then programmed during initialization as follows:

- Clock divider set to 'divide by eight':** The memory clock (E) at approximately 680kHz is divided by 8 to give an internal clock frequency of 85kHz.
- An inherent division by 16** reduces the scan clock to 5kHz giving a scan cycling frequency of 333Hz.
- Encoded Keyboard Scan:**
The scan output from SL₃₋₀ is a 4-bit count. SL₃ is not used; SL₂₋₁ scans M4, SL₂₋₀ scans M5.
- Keyboard Mode:**
The internal keyboard RAM is programmed as FIFO, input being routed via RL₇₋₀ return lines. Two-key lockout is employed with debounce.
- Display Mode:**
 - Eight character left entry for the LED display.
 - Inter-digit blanking:
 - all 1's on B₀₋₃ and A₀₋₃ between digits.

6.2.2.3 M6 Reprogramming

The Frequency Store key and the 13 dual \updownarrow keys have a reprogrammable function. When one of these keys is pressed, the P8279 is reprogrammed into Scanned Sensor Mode. When released, the P8279 reverts to Encoded Keyboard Scan Mode.

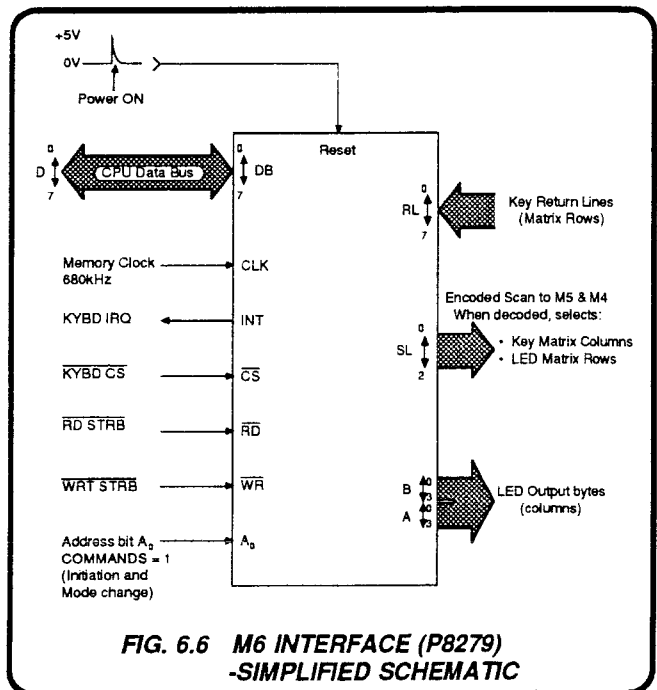


FIG. 6.6 M6 INTERFACE (P8279)
-SIMPLIFIED SCHEMATIC

6.2.3 SCAN DECODING

The encoded scan output from M6 (approximately 333Hz cycle frequency at $SL_{2,0}$) is decoded by M5 to energize each key-matrix column line once every scan cycle. $SL_{2,1}$ scan outputs are also decoded by M4A to energize each LED-matrix cathode driver once in every scan cycle for a period of two digits.

6.2.4 KEY SELECTION

The keys are electrically grouped within a matrix of 8 rows of 7 (one position vacant - the Reset key is not part of the matrix). This does not conform to their physical grouping on the front panel. Each of the eight return lines $RL_{0,7}$ defines a matrix row, whose seven elements are scanned by M5 (Low active).

The keyboard memory RAM in the P8279 (M6) is an image of the key matrix, internally synchronized to the $SL_{2,0}$ column scan, and receiving row inputs from $RL_{0,7}$. It thus stores the state of each of the 55 keys. The use of 2-key lockout rejects two or more simultaneous contacts. Any single key depression is debounced, initiating the interrupt KYBD IRQ to the CPU which then interrogates the keyboard image RAM in the P8279.

The next action depends upon the key's function:

a. \updownarrow key pressed:

- i. M6 is reprogrammed into Scanned - Sensor mode for as long as the key is pressed, the CPU acting on the key information.
- ii. If a single \up or \downarrow key is held down for longer than half a second, the display enters 'auto \updownarrow ' mode, running at about 3 digits per second.
- iii. When the key is released, M6 is returned to Encoded Keyboard Scan mode.

b. 'Store' key pressed:

- i. M6 is reprogrammed into Scanned - Sensor mode for as long as the key is pressed, the CPU acting on the key information.
- ii. If an F1 to F5 key is pressed while 'Store' is held down, the appropriate frequency memory location is accessed, and the output frequency is reset to the value in the memory.
- iii. When the 'Store' key is released, M6 is returned to Encoded Keyboard Scan mode.

c. Any other key pressed (not 'Reset'):

- i. M6 remains in Encoded Scan mode; the scan continues as the CPU is acting on the key information.
- ii. KYBD IRQ interrupts are generated only by the low-going edges of the key contact pulses, so M6 remains sensitive to subsequent key depressions.

6.2.5 KEY LED OPERATION

After performing the change requested by the key depression, the CPU changes the bit-patterns stored in M6 internal display RAM. As this is scanned internally in synchronism with the decoded outputs of M4A, each output byte of $B_{0,3}$ / $A_{0,3}$ drives the row of LEDs accessed by M4A output lines.

The bit-pattern of the byte selects the LEDs to be lit in that matrix row:

| | |
|--------------------------------|-----------------------|
| $B_{0,3}$ / $A_{0,3}$ bits at: | Logic-1 = LEDs unlit; |
| | Logic-0 = LEDs lit. |

During changes of output between successive bytes, all the lines from $B_{0,3}$ / $A_{0,3}$ are set to Logic-1 to avoid spurious LED flashes.

Transistors Q25-Q32 drive the LED anodes, from a +5V supply regulated by M2. Darlington amplifiers Q21-Q24 drive the LED cathodes.

6.2.6 AUDIBLE WARNING BUZZER

There are two reasons for an audible warning from the calibrator:

- When the instrument enters High Voltage State (>110VDC or >75VRMS). A 4kHz tone is used, pulsed as described in the User's Handbook.
- When an inappropriate selection is attempted, or if any FAIL or Error message is displayed. For this purpose a single 500Hz 'Beeper' pulse is generated.

6.2.6.1 High Voltage State Alarm Control (Circuit Diagram 430558 page 11.1-1)

M4B and M1 act as a control latch for the quartz warning buzzer. With ALARM at Logic-1 (+5V) M1 remains unchanged; but with ALARM at Logic-0 (0V) the state of M1 depends on the condition of the A₀ line:

A₀ at Logic-1: the buzzer sounds a tone.
A₀ at Logic-0: the buzzer is silent.

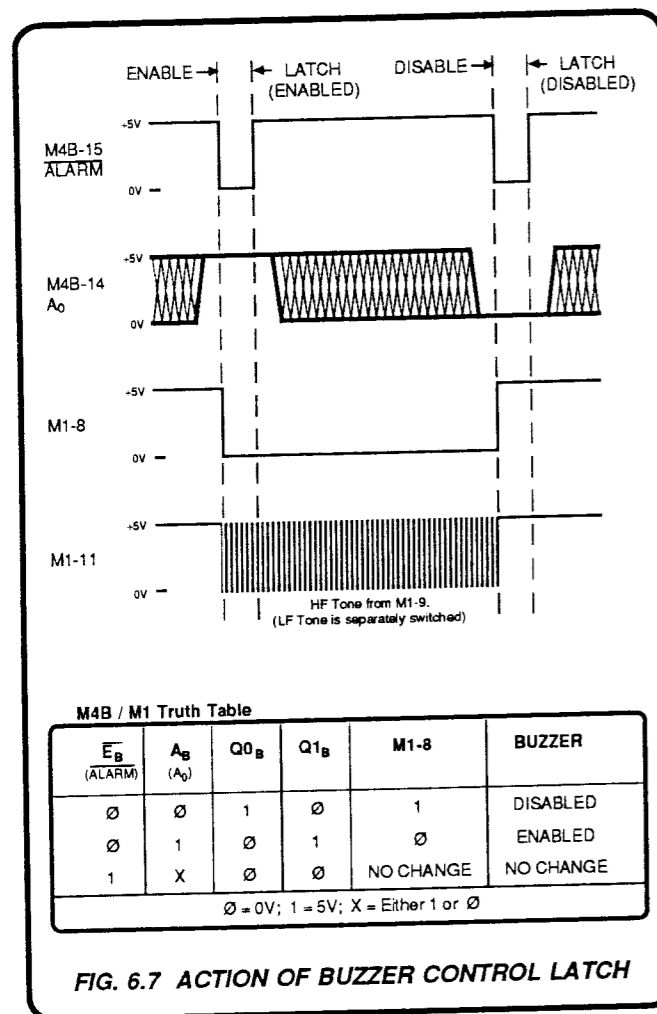


FIG. 6.7 ACTION OF BUZZER CONTROL LATCH

The latch is operated at CPU speed. Two \overline{ALARM} pulses are used for each burst of sound. The first, with A₀ at Logic-1, starts the burst; the second, with A₀ at Logic-0, ends it.

The waveforms and truth table in Fig.6.7 illustrate the action of the latch, with M1-13 at Logic-0.

During POWER ON initialization, the combination of \overline{ALARM} at Logic-0 and A₀ at Logic-0; is applied to M4B to force power-up in the disabled condition.

The 4kHz HF TONE signal at M1-9 originates in the Precision Divider counter which is situated on the Analog Interface Assembly. (Refer to Circuit Diagram 430648 page 11.3-2).

The 500Hz LF TONE signal at M1-13 remains at Logic-0 unless the 'Beeper' in the Analog Interface assembly is switched. (See section 6.2.6.2).

Note that A₀ may be used for other purposes when \overline{ALARM} is at Logic-1, but this will not affect the buzzer state.

6.2.6.2 'Beeper' Control

(Circuit Diagrams: 430558 page 11.1-1,
430648 page 11.3-3)

The Alarm Control circuitry on the Front assembly is overridden for Beeper control. During a 'Beep', the HF TONE signal is inhibited, and the LF TONE signal at M1-13 is enabled to control the buzzer output.

On the Analog Interface assembly (page 11.3-3) the Beeper consists of a monostable timer and NAND logic. Unless a requirement arises for a 500Hz warning, the \overline{BEEP} signal is at Logic-1. Thus M55-3 is at Logic-0, so M54-5 at Logic-1 inhibits the LF TONE signal, M54-4 remaining at Logic-0. M54-8 is at Logic-0 enabling the 4kHz HF TONE, which is passed to the Front assembly at M1-9 (page 11.1-1).

When required, a single 'Beep' is originated by the CPU pulsing M34-3 (page 11.3-1) to Logic-0. This is the \overline{BEEP} signal applied to the monostable M55-2. M55-3 rises to Logic-1 for approx. 150ms until the monostable times out, then reverts to Logic-0. M54-8 is at Logic-1 during this period, inhibiting the HF tone and setting M54-11 to Logic-1. This is passed to M1-9 on the Front assembly, where it ensures that M1-12 is at Logic-0 to override any High Voltage alarm. M54-5 at Logic-0 enables the 500Hz LF TONE signal to pass via M54-4 to M1-13 on the Front assembly (see page 11.1-1). As M1-12 is held at Logic-0 during the beep, the buzzer produces 150ms of audible 500Hz output.

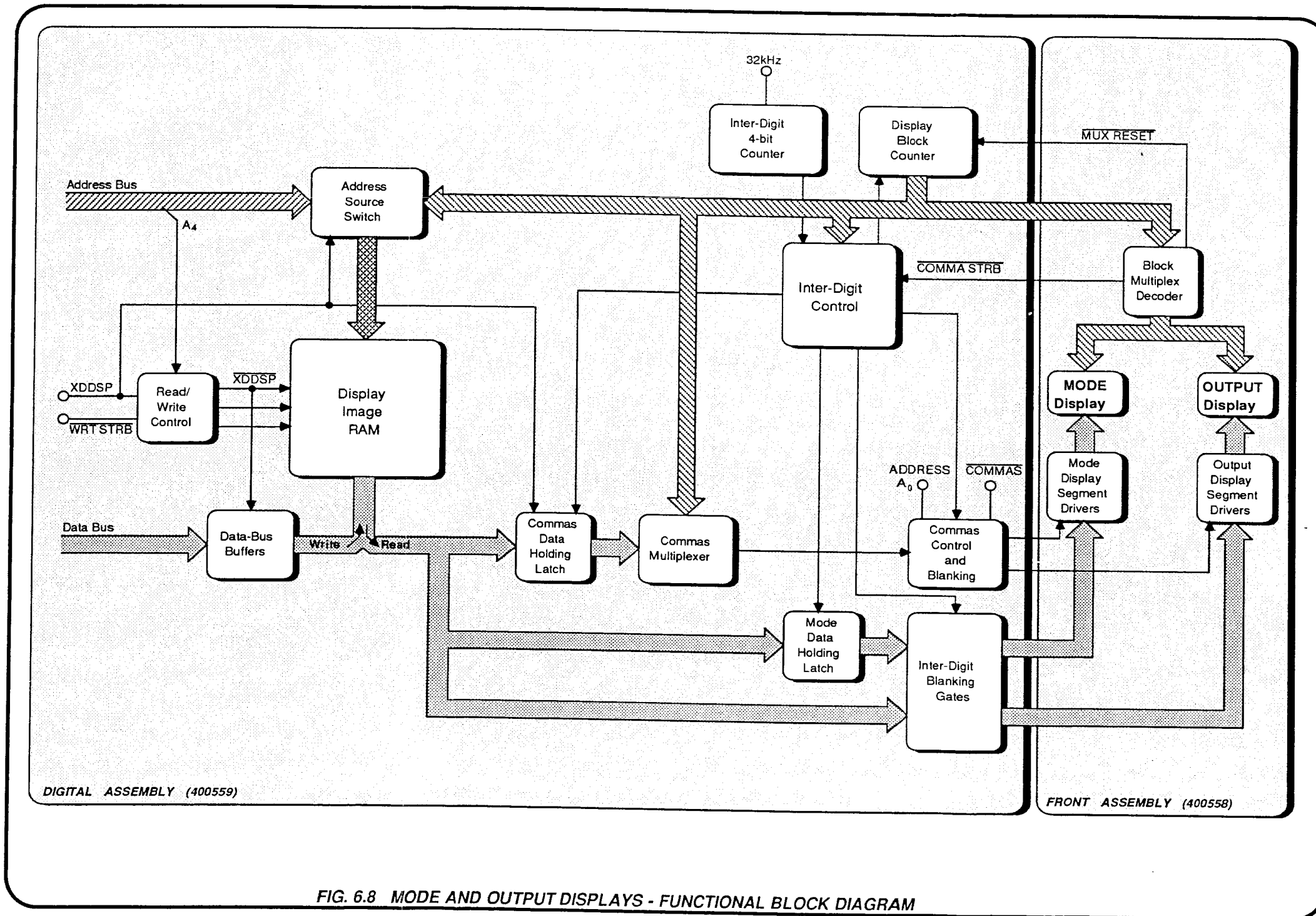


FIG. 6.8 MODE AND OUTPUT DISPLAYS - FUNCTIONAL BLOCK DIAGRAM

6.3 DIGITAL DISPLAYS

The circuits described in this section perform the following functions:

- Storage of display data in a Display Image RAM, updated under CPU control.
- Generation of multiplex count which selects segment data from the RAM, and energizes the appropriate digital blocks in synchronism.
- Distribution of high voltage supplies to energize the plasma displays.

Part of the Digital assembly (400796) houses the display multiplexer, which includes the display image RAM, the interdigit and multiplex counters, and control circuitry.

The two plasma displays, the block multiplex decoder, segment drivers and high voltage circuits are located on the Front assembly (400558). The block diagram of *Fig.6.8* shows the arrangement and main interconnections of the display circuitry.

6.3.1 GENERAL (*Fig.6.8*)

The purpose of the Display Image RAM is to accept and store current display data, which is read out to drive the display segments. The Display Block Counter generates a 4-bit count at 2kHz which scans the 11 digit-blocks of both displays in parallel. The same count scans the RAM, selecting segment information for each block in turn. As there are two displays, and therefore two RAM bytes to read for each block, the 'MODE' display data is first entered into a holding latch during the inter-digit blanking period at the start of the time-slot for its block.

To update the displayed characters, the CPU writes into the RAM at high speed (680 kHz), using signal XDDSP to connect the Address bus through the Address Source Switch to the RAM. XDDSP also connects the Data Bus to the RAM through the Data Bus Buffers, writing the new segment data into the selected RAM Address. The high speed of the transfer, compared with the much slower scanning speed in Read mode, avoids spurious effects appearing on the displays.

Each RAM address contains only 8 bits, but there are nine segments in each display block. Comma-segment information is therefore not written into its normal block address in the RAM, but stored as a bit in a separate 'Commas' byte, which holds the data for all eight blocks having a comma. The byte is read out into a Commas Data Holding Latch, once every block-scan cycle, and then selected for display by a Commas Multiplexer 8-into-1 switch.

6.3.2 STATIC CONDITIONS (Circuit Diagram 430558 *Page 11.1-2*)

All plasma display block anodes are driven from the +5V supply and all segment cathodes from the -175V supply. The supplies are connected by conduction of anode and cathode driver transistors:

| | |
|------------------|----------------------|
| Anodes: | |
| Both Displays - | Q10 to Q20, |
| Cathodes: | |
| MODE display - | Q2 to Q9, and Q41, |
| OUTPUT display - | Q33 to Q40, and Q42. |

When not energized, all anodes and cathodes are held at -70V by the action of 75V zener D17.

To energize a particular block (simultaneously on both displays), the multiplex decoder causes the relevant anode driver transistor to conduct, lifting its two anodes to +5V.

At the same time, the two sets of data (for the characters to be displayed in the two blocks) are extracted from the Display Image RAM, and applied to the segment cathode drivers. Those segments selected for illumination are pulled to -175V, striking the discharge.

Four keep-alive electrodes in each digit block (two anodes and two cathodes) are maintained at +5V and -175V respectively. This ensures a rapid strike when a digit is energized, helping to prevent inter-block 'streaming'.

6.3.3 WRITE MODE

(Fig. 6.9)

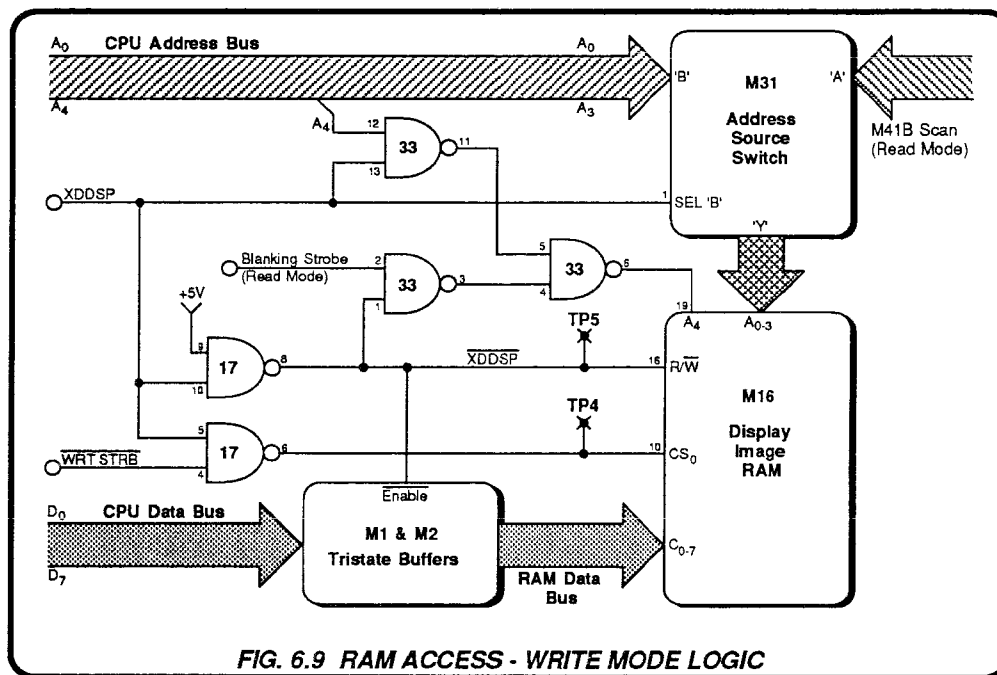


FIG. 6.9 RAM ACCESS - WRITE MODE LOGIC

Whenever the CPU is programmed to update a display (eg. for Range, Function, Mode or Value change) it sets address decode XDDSP to Logic-1 with each byte of data to be transferred. This causes M31 and M33 to select the CPU address lines A₄₋₀ which are mapped directly to the RAM address input lines A₄₋₀. The RAM is placed into its write mode by signal XDDSP at Logic-0 (M17-8, TP5, M16-16).

The RAM M16 is divided into two sections, using the address bit A₄ to differentiate between OUTPUT and MODE display images. When the CPU is loading the RAM with OUTPUT display data, it sets A₄ to Logic-1, passing to set M16-19 (A₄) input to Logic-1. MODE display and COMMAS images are written into M16

with A₄ at Logic-0 (M33-4 and 13 at Logic-1 in write mode). (In Read mode M16-19 is again used to differentiate between the two image sections).

The signal XDDSP (M17-8) enables the tri-state buffers M1 and M2, connecting the CPU data bus to M16 data input/output lines D₀₋₇. With each byte of display data, the CPU also generates the write strobe signal WRT STRB. This is combined with XDDSP (M17-6, M16-10, TP4) to enable M16 internal Input/Output tri-state buffers to accept the data byte (chip select CS₀). Once the display data has been loaded into the RAM, the CPU returns XDDSP to Logic-0 and the RAM reverts to Read mode.

6.3.4 READ MODE

(Fig. 6.10)

Unless the CPU has data to update, the signal XDDSP remains at Logic-0, to hold the display multiplexer circuitry in Read mode. The RAM data bus is isolated from the CPU data bus by tri-state buffers M1/M2, and M16 is chip-selected in read mode by M17-6 and M17-8 at Logic-1.

6.3.4.1 Display Scan Address Interlacing

(Circuit Diagram 430796 Page 11.2-1)

M31-1 (SEL) at Logic-0 causes the RAM to be addressed from the display block scan, mapping M41B outputs: Q4B, Q3B, Q2B, Q1B to RAM address input lines: A₀, A₃, A₂, A₁ respectively. This bit-rotation interlaces the extraction of display data, in synchronism with the interlaced block selection by the Front Assembly Scan decoder.

6.3.4.2 Block Multiplex Decoding

(Circuit Diagram 430558 Page 11.1-2)

(Figs. 6.10 and 6.11)

The 4-bit Block scan output MUX A₃₋₀ from the multiplex scan counter M41B (dig) is used at DATA₄₋₁ input to M3 (on the Front assembly), which decodes it into a low-active 16-line scan S₁₅₋₀.

To strobe the commas, M3 output S₆ generates the signal COMMA STRB, and its S₁₃ terminates each scan by resetting M41B in the Digital assembly (MUX RESET). Outputs S₇, S₁₄ and S₁₅ are not used.

The other eleven M3 outputs switch transistors Q10 - Q20 on sequentially, driving the anodes of both plasma displays in synchronism. As can be seen from Fig. 6.11, the interlace is maintained to avoid consecutive activation of adjacent blocks, thus preventing inter-block 'streaming'.

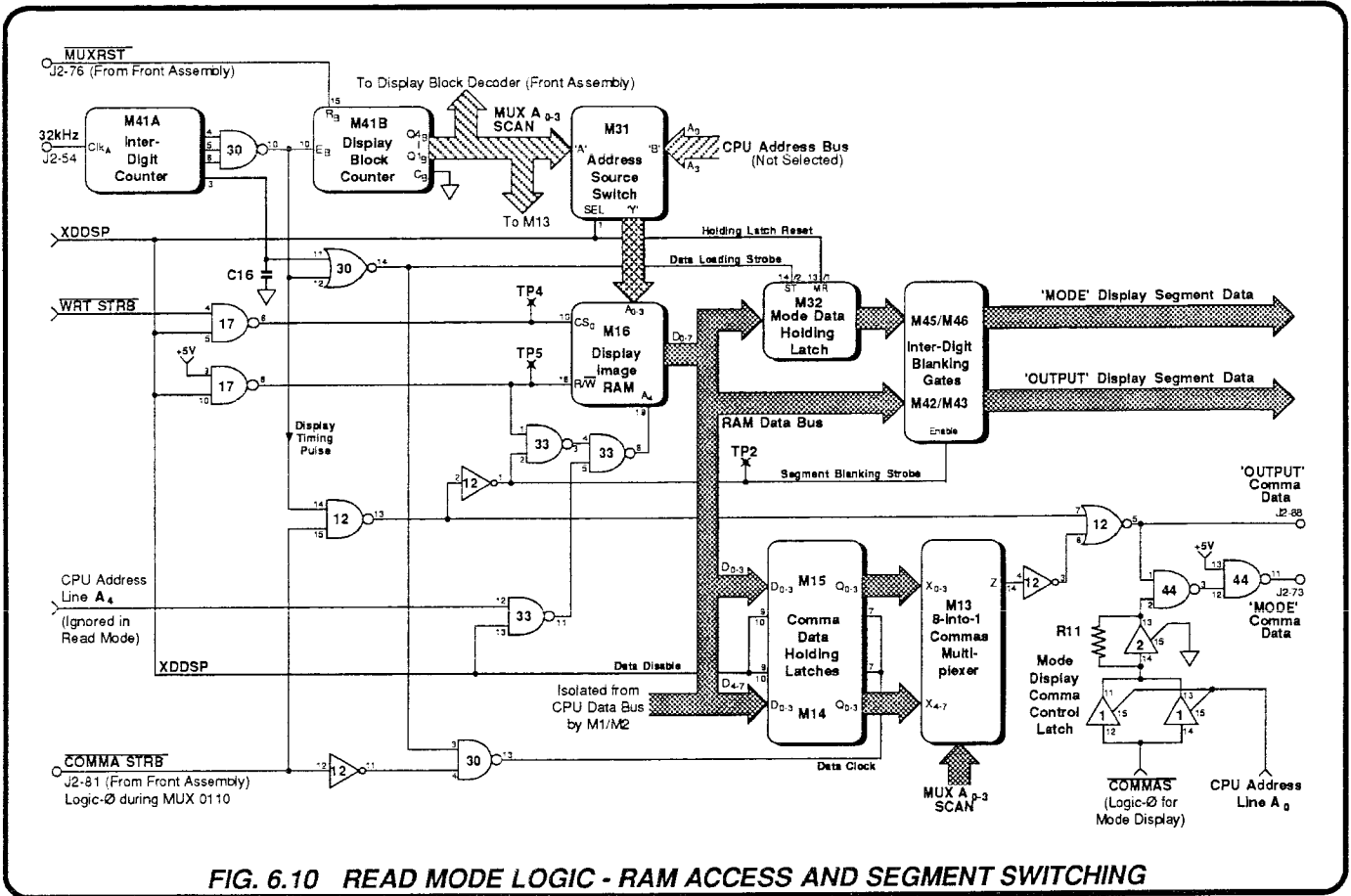


FIG. 6.10 READ MODE LOGIC - RAM ACCESS AND SEGMENT SWITCHING

6.3.4.3 Display Data Selection

(Circuit Diagram 430796 Page 11.2-1)

When the processor writes display data into the Display Image RAM, the A₄ input is used to select the MODE or OUTPUT display data storage area (see para 6.3.3 and Fig. 6.11). In Read mode also, A₄ is set to Logic-1 to read OUTPUT display data, and to Logic-0 for MODE or COMMA data.

For an alpha-numeric display block, 18 bits of data could be required:

- One byte - OUTPUT display block segments;
- One byte - MODE display block segments;
- Two bits - COMMAS (one for each display).

The problem of transferring two bytes of data along the single-byte RAM data bus is overcome by strobing each MODE display segment byte into a holding latch (M32), during the first 30μs of its block selection time-slot. The MODE display section of the RAM is selected by setting its A₄ input to Logic-0 for this 'Inter-digit' period, during which the inter-digit blanking gates, (M42/43, M45/46), set all the segment lines going to the Front Assembly to Logic-0 (segments OFF).

COMMAS data are stored in the Display Image RAM as a separate byte (refer to Section 6.3.4.6).

| MUX A ₃₋₀ SCAN A ₃ A ₂ A ₁ A ₀ | M3 Output 'S' Low Active (Front Assembly) | Display Block Anode Energized, or Signal Selected (for both displays simultaneously) |
|--|--|--|
| M3 DATA 4-1 Input D ₄ D ₃ D ₂ D ₁ | | |
| M16 A ₃₋₀ Input (Display Image RAM - Digital Assembly) A ₀ A ₃ A ₂ A ₁ | | |
| 0 0 0 0 | S ₀ | A ₁ |
| 0 0 0 1 | S ₁ | A ₃ |
| 0 0 1 0 | S ₂ | A ₅ |
| 0 0 1 1 | S ₃ | A ₇ |
| 0 1 0 0 | S ₄ | A ₉ |
| 0 1 0 1 | S ₅ | A ₁₁ |
| 0 1 1 0 | S ₆ | COMMA STRB |
| 0 1 1 1 | S ₇ | Not Used |
| 1 0 0 0 | S ₈ | A ₂ |
| 1 0 0 1 | S ₉ | A ₄ |
| 1 0 1 0 | S ₁₀ | A ₆ |
| 1 0 1 1 | S ₁₁ | A ₈ |
| 1 1 0 0 | S ₁₂ | A ₁₀ |
| 1 1 0 1 | S ₁₃ | MUX RESET |
| 1 1 1 0 | S ₁₄ | } Not included in cycle (MUX RESET at S ₁₃) |
| 1 1 1 1 | S ₁₅ | |

FIG. 6.11 DISPLAY SCAN SEQUENCES

6.3.4.4 Display Timing

(Fig. 6.12)

Read mode is driven by a 32kHz square wave (Waveform 'A', generated from the 13-bit counter in the Analog Interface Assembly M15-11), used as clock for a 4-bit counter (M41A). The three most significant bits are combined at M30-10 to produce Waveform B, the display master-timing pulse, used also for inter-digit blanking.

The following example explains how the display data is set up for the next display block in sequence, during the 62.5µs of the display timing pulse.

Example

Initial State:

M41B count has already reached 1001, and the block-4 anodes of both displays are energized (Fig.6.11).

The OUTPUT display data for block 4 is selected in the Display Image RAM (M16) to drive the segment cathodes for a figure '6', which appears on the OUTPUT display.

Block 4 of the MODE display is showing a figure '3', and the data for this is being output from the MODE display Holding Latch (M32). The data held in M16 for the next byte (Block 6 of both displays) is:

OUTPUT display - Figure '8'
MODE display - Figure '7'

Block Changeover: The next block is selected during the display master timing pulse (Fig. 6.12, Waveform B).

- a. The negative-going leading edge triggers the scan counter (M41B) whose output advances to 1010 (block 6). On the Front Assembly, M3 de-energizes A₄ anodes and energizes A₆ anodes.
- b. For the duration of the Display Master Timing Pulse (Logic-Ø at M12-14), the A₄ input to M16 is set to Logic-Ø as A_{3,0} inputs are advanced to 0101. MODE display data for figure '7' is loaded onto the RAM data bus as follows:

- i. M17-6 at Logic-1 selects M16 at M16-10,
 - ii. M17-8 at Logic-1 holds M16 in Read mode,
 - iii. RAM address A_{4,0} = 00101 reads MODE display block 6 data onto the RAM data bus (M1/M2 isolates from the CPU data bus),
 - iv. M30-14 at Logic-1 strobes the byte into M32 during the 30µs of Waveform D, then returns to Logic-Ø leaving figure '7' data latched at M32 output.
 - v. M12-1 at Logic-Ø blanks the two displays by setting M45/M46/M42/M43 outputs to Logic-Ø, regardless of their inputs from M32 and the RAM data bus.
- c. The positive-going edge of Waveform B lifts the RAM A₄ input (M16-19) to Logic-1, addressing the OUTPUT display section of memory. A_{3,0} is still at 0101, selecting block 6 display data (in our example a figure '8') which it loads on to the RAM data bus.

The end of the master timing pulse also releases the blanking by enabling gates M42/M43/M45/M46, so the data for both MODE and OUTPUT displays are now delivered to the cathode drivers on the Front assembly, to strike the gas discharge in the two energized A₆ blocks.

This condition persists for 437.5µs until the next master timing pulse, when Waveforms B and C repeat the process for the next block of stored display data.

At any time during the cycle, the CPU may force Write mode. This will not disturb the scan from M41B, but XDDSP will reset M32 outputs to Logic-Ø (M32-1/13). However, the speed of byte transfer from the CPU ensures that the data being transferred is not visible on the displays. Subsequently, each block will be driven by its new stored data.

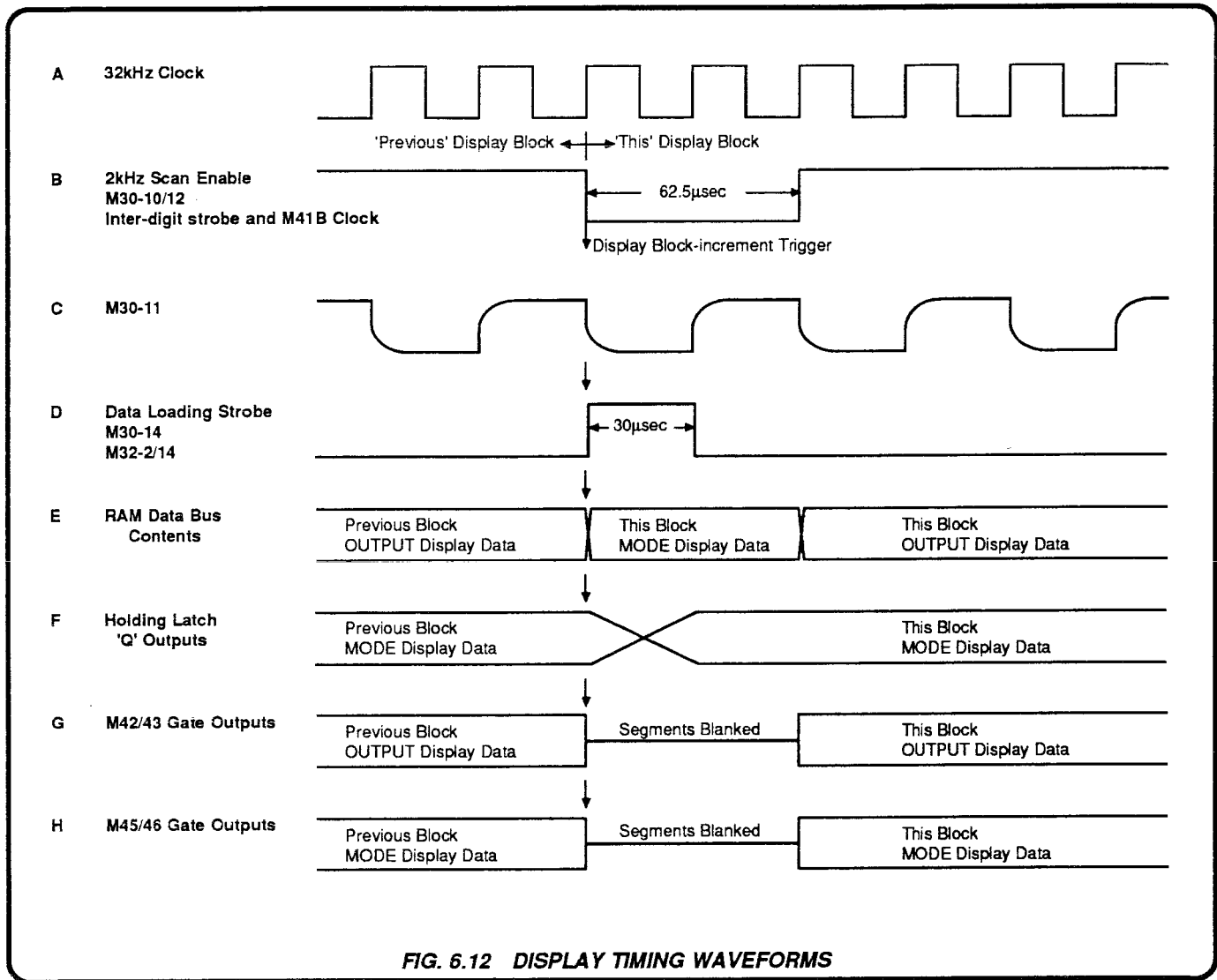


FIG. 6.12 DISPLAY TIMING WAVEFORMS

6.3.4.5 Display Segment Drive (Circuit Diagram 430558 Page 11.1-2)

The strobed segment signals from the Digital Assembly are input to the Front Assembly on J1 pins 67-75 (MODE display) and J1 pins 82-90 (OUTPUT display). These are already synchronized to their blocks by the 4-bit block scan MUX A₃₋₀ within the Digital assembly.

For each block in sequence, the appropriate segment bit-pattern is set at the input to the segment drivers. For bits at Logic-1, the rise is passed through line capacitors to reverse-bias the DC restoration diodes and forward bias their driver-transistor bases. The segment cathodes are pulled down to -170V by the resultant collector currents, from their quiescent -70V. The correct block anode is simultaneously lifted from -70V to +5V by its anode driver transistor, striking the gas discharge and displaying its digit. For bits at Logic-0 the cathode drivers remain cut off.

The above action proceeds for both displays simultaneously. The anode driver transistor energizes its corresponding block anode on both displays, at the same time as the cathode drivers are loaded with the correct block bit-pattern for their own display.

The cathode driver emitter resistors control the segment cathode currents for uniform brilliance of all segments.

During change-over between blocks, all segment inputs at Logic-1 are returned to Logic-0 by the inter-digit blanking strobes M42/43/45/46 on the Digital assembly. This turns off the drive transistors and blanks the display. The high scan frequency and persistence of the operator's vision prevents the blanking being observed on the display.

6.3.4.6 Comma Logic (Figs. 6-10 and 6.13)
(Circuit Diagram 430559 Page 112-1)

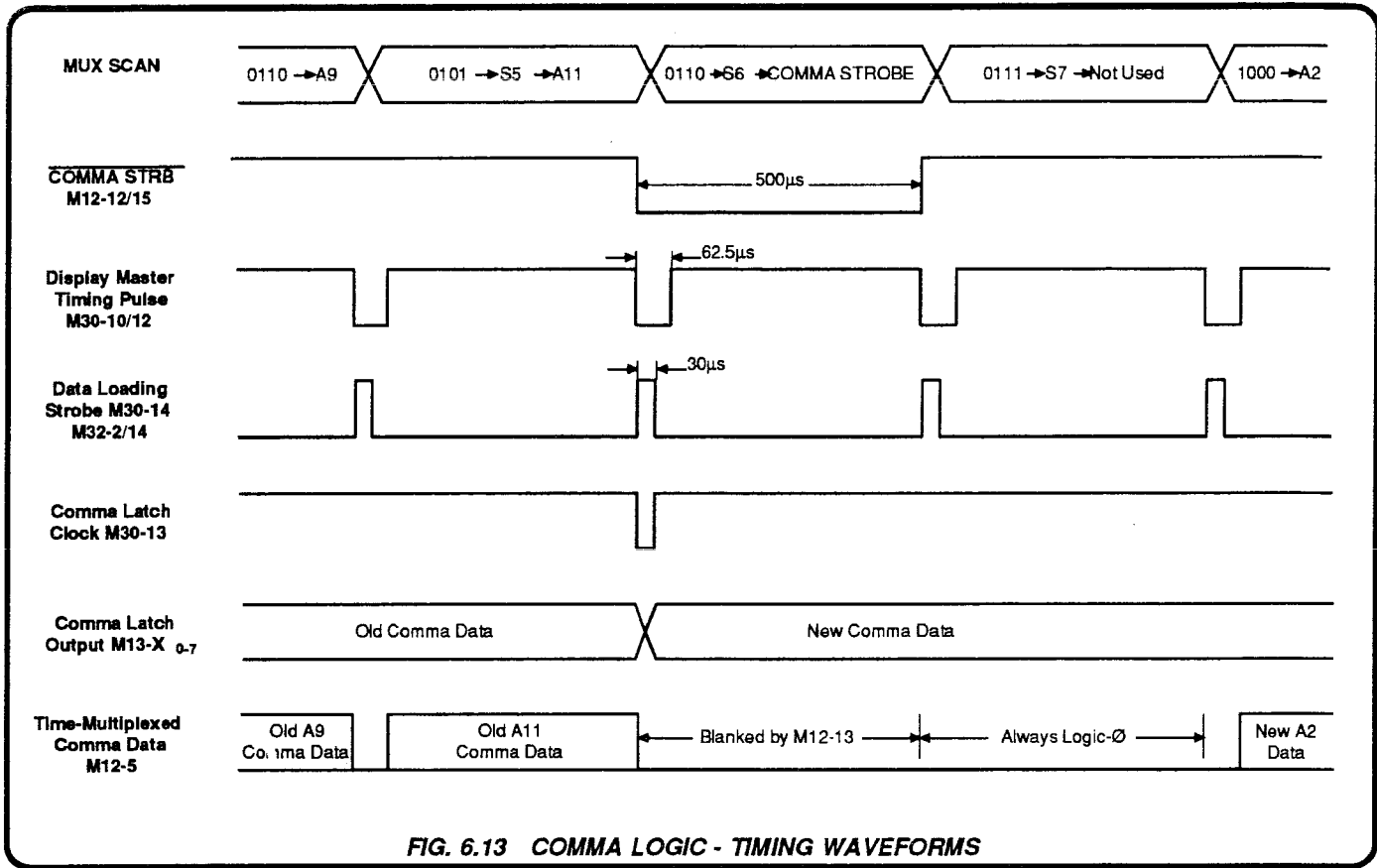


FIG. 6.13 COMMA LOGIC - TIMING WAVEFORMS

The comma is the ninth segment (i) in each of the numerical display blocks. It cannot fit into a block's byte in memory, as there are only eight bits per byte. But all the comma information can be stored in a single byte of memory in the RAM (RAM address 01100). This is possible although there are nine numerical blocks, because the ninth block never requires a comma. Legend blocks A₁₀ and A₁₁ do not have a segment (i).

The RAM COMMA data is updated by the CPU in Write mode, and is read out (as though it were another display block) by M41B scan 0110 during the master display pulse (Waveform B sets RAM A₄ input to Logic-0). The same MUX combination 0110 selects S₆ output from M3 decoder on the Front Assembly, which sets the signal COMMA STRB to Logic-0.

Thus for the duration of S₆ = 0, (500µs); the COMMA data is on the RAM data bus, but the blanking gates prevent it reaching segments (a)-(h).

6.3.4.7 Comma Drive Multiplexing

The COMMA STRB signal is inverted and combined with the Data Loading Strobe at M30-13 as a Logic-0 pulse, whose positive-going edge clocks the comma data into latches M14/15, approximately 30µsec after it has been loaded on to the RAM data bus. The permanently-enabled outputs from these latches are input as X₀₋₇ into the 8-into-1 multiplexer M13 during a complete MUX scan until the next COMMA STRB signal.

The block-multiplex scan from M41B selects the correct X input to synchronize with activation of its display block anode. This is output from M13-14 (Z), into blanking gates M12.

Comma information is blanked during COMMA STRB, and by inter-digit blanking during display-block change-over (M12-7).

The Comma drive line from M12-5 to the front panel, via J2-88, controls segment (i) cathode driver for the OUTPUT display.

If commas are required on the MODE display (e.g. in 'Spec' operating mode +Lim or -Lim) they will always be in the same display blocks as the OUTPUT display. When this mode is selected, the CPU pulses the COMMAS line to Logic-0 at the same time as Address line A₀ goes to Logic-1. Tristate buffer outputs M1-11 and 13 go to +5V, setting M2-13 output to +5V (Logic-1). Outputs M1-13 and M1-11 go tristate when the COMMAS line returns to Logic-1, leaving M2-13 latched to +5V by the positive feedback action of R11. So M44-2 enables the comma data to the MODE display segment driver, via J2-73, to copy the OUTPUT display commas on to the MODE display.

When MODE display commas are not required, Logic-0 (0V) is set on A₀ with COMMAS signal at Logic-0. Thus M2-13 latches to Logic-0 and M44-2 disables the flow of comma data to the MODE display.

6.4 ANALOG CONTROL INTERFACE

The circuitry described in this section performs the following functions:

- Provides a two-way interface via a serial data link between out-guard digital processing and in-guard analog control circuitry on the reference divider assembly (see Fig. 6.14).
- Monitors the CPU operation, serial transfer, digital supply failure and restart operations (watchdog), imposing a controlled safety default condition if there is a danger of losing digital control of the analog functions.

A manual reset of the safety monitor is provided on the front panel (see Fig. 6.17).

6.4.1 GENERAL

Safety and Control information is input from Digital (400796) and Front (400558) Assemblies to out-guard circuits located on the Analog Interface Assembly (400648), processed and transferred across the 'Guard' isolation barrier to in-guard circuits in the Reference Divider Assembly (400652). After further processing in the Reference Divider Assembly, safety and control information is output to the following assemblies:

- Sine Source Assembly (400446),
- AC Assembly (400844),
- PA Assembly (400618),
- DC Assembly (400536),
- Current/Ohms Assembly (400614), and
- High Voltage Assembly (400537).

Certain selected 'Status' signals, originating in the analog assemblies, are returned to the CPU during the data transfer. Thus, the data link forms a continuous loop, as shown in Fig. 6.14.

6.4.2 SERIAL DATA TRANSFER (Fig. 6.14)

(Circuit Diagrams: 430796 Page 11.2-2, 430648 Page 11.3-3, 430652 Pages 11.4-4 and 11.4-5)

A bi-directional serial data link passes information across the guard isolation screen; passing CPU commands to control the in-guard analog circuitry, and returning critical status signals from the guarded circuits back to the CPU.

The link is managed by a synchronous serial data adaptor (SSDA) which, having first been loaded with three bytes of control instructions by the microprocessor; transmits the resultant 24-bit word across guard one bit at a time, via its Tx DATA channel.

The 48 bits necessary to control the analog circuitry thus require two successive 24-bit transmissions.

Simultaneously with each 24-bit transmission, the SSDA receives a 24-bit word via its Rx DATA channel, enabling the CPU to parity-check its returned data, and obtain the status of the analog functions.

6.4.2.1 The Transfer Cycle (Fig. 6.14)

The CPU uses an address-code signal AN I/F STRT (Analog Interface Start) to initiate each 24-bit shift, by triggering a separate clock generator (M2, M3, M4) which produces a burst of 24 clocks per shift. Data is clocked in a serial string through a continuous loop comprising:

- the 48-bit, serial in/parallel out, analog control shift register;
- the 16-bit, parallel in/serial out, status shift register;
- back to the SSDA receiver (Rx DATA).

The serial data string is correctly located after two 24-bit shifts, so then the SSDA generates a strobe pulse which:

- Transfers the data present in the serial data string of the six 8-bit analog-control shift registers (M27, M25, M31, M19, M30, M15) into their enabled parallel output registers and onto the analog control bus.

When the strobe ends, further transfer is disabled and the registers' output data is latched.

- Injects the status data at each of the 8-bit parallel inputs of the two status shift registers (M18, M22) into corresponding locations in the serial data string.

When the strobe ends, the parallel inputs to the status registers are disabled.

After the strobe pulse, the CPU initiates a further circulation of serial data (including the status data), in order to obtain the status data and return the analog control bits to the SSDA Rx DATA register for parity checking by the CPU.

This extra (confirmatory) circulation requires three more 24-bit shifts, so a complete data transfer consists of five shifts. If no error is detected, the SSDA provides a trigger-enable to allow updates to prevent activation (BARK) of the watchdog circuits.

If an error is detected on the first transfer, the CPU activates a second complete transfer, and then a third if an error is detected on the second. If the error persists after the third transfer, the trigger-enable is withheld, and the instrument will shut down under the control of the 'Watchdog' safety monitor.

All interfacing between out-guard and in-guard circuits is achieved using electrically-isolating opto-couplers.

6.4.2.2 Data Transfer Organization (Fig. 6.15)

Data is transferred serially via the SSDA, control registers and status registers as directed by the CPU.

The exchange of data between the CPU and SSDA is made in bytes of 8 bits on the instrument data bus, each exchange comprising three bytes (24 bits) of parallel data.

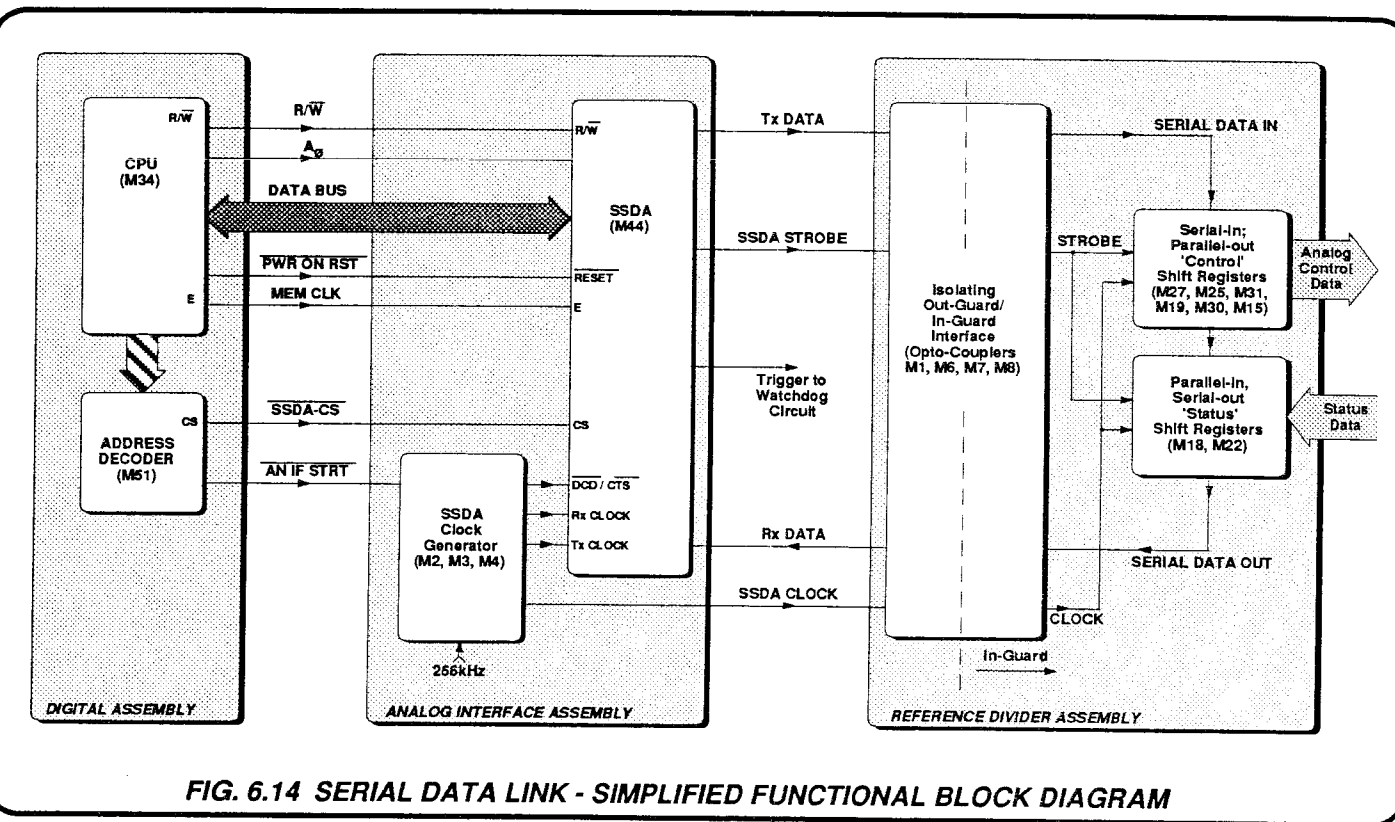


FIG. 6.14 SERIAL DATA LINK - SIMPLIFIED FUNCTIONAL BLOCK DIAGRAM

The shifts of serial data through the in-guard circuit are synchronized by clocks which are controlled from the CPU, and the SSDA Rx return registers are cleared when read by the CPU.

Once the in-guard serial data is correctly positioned at the inputs to the control registers, the SSDA generates a strobe which enables its transfer to the parallel outputs of the control registers. The same strobe enables injection of the data on the parallel inputs of the status registers into the serial data string.

The transfer operation requires five serial data shifts, each of three bytes, through the registers. During this operation: the control registers are loaded with bytes of new data (ND); the status registers are loaded with new status data (NS); and the whole of the ND and NS data is returned to the CPU, which:

- a. verifies that the analog control bits of the serial data string return to the SSDA Rx DATA register without error. This indicates that at least, the correct bit pattern was applied to the analog control register inputs at the time the strobe was generated.
- b. acts upon the status data received.

6.4.2.3 Transfer Sequence

The sequence of events in the transfer operation is as follows, referring to *Fig. 6.15*:

- a. Three bytes of new data, ND1, ND2 and ND3 are loaded into the SSDA transmitter registers; this data is destined for control registers D1, D2 and D3. The SSDA receiver registers were cleared when last read by the CPU.
- b. A burst of 24 clock pulses, initiated by the CPU, shifts all data three bytes to the right. After the shift is completed, the transmitter registers are loaded with new data bytes ND4, ND5 and ND6 (destined for control registers D4, D5 and D6). During this period, no transfers are made between the serial data string and the parallel control or status registers.
- c. A second burst of 24 clock pulses again shifts all data three bytes to the right. New data bytes ND1 to ND6 are now correctly positioned in control registers D1 - D6. After completion of the shift, three dummy bytes are loaded into the transmitter registers. Old data in the receiver register is ignored.
- d. With new data bytes ND1 to ND6 correctly located, the SSDA generates a strobe pulse. This pulse:
 - i. latches the 48 bits of bytes ND1 to ND6 at the parallel outputs of control registers D1 to D6;
 - ii. enables the parallel inputs of status registers S1 and S2, loading two new status bytes NS1 and NS2 and clearing old data OD5 and OD6 from the registers.
- e. A third burst of 24 clocks again shifts all data three bytes to the right. The CPU reads bytes NS1, NS2 and ND1 from the SSDA receiver registers (the CPU may take immediate action on NS returns). After the shift is complete, new data bytes ND1, ND2 and ND3 are re-loaded into the transmitter registers.

- f. A fourth burst of 24 clocks again shifts all data three bytes to the right. The CPU reads bytes ND2, ND3 and ND4 from the receiver registers. After the shift is complete, new data bytes ND4, ND5 and ND6 are re-loaded into the transmitter registers.
- g. A fifth burst of 24 clocks again shifts all data three bytes to the right. Bytes ND5 and ND6 are read from the receiver registers. The CPU has now read all new data and status bytes and the transfer sequence ends. If an error is detected between new data transmitted and new data received, the transfer process is repeated; three attempts are allowed before a fault condition is declared.

6.4.3 SYNCHRONOUS SERIAL-DATA ADAPTOR

(Circuit Diagram 430648 Page 113-3)

6.4.3.1 SSDA Initialization

When power supplies are first switched on or an external reset signal EXT RST is applied, the signal $\overline{\text{PWR ON RST}}$ (Power On Reset) is held at Logic-0 for approximately 8ms.

During this period, the SSDA is latched in a reset condition to prevent erroneous output transitions at its Tx and Rx interfaces; the internal transmit registers are inhibited to prevent the loading of data from the data bus and the SSDA strobe output is held at Logic-1.

After $\overline{\text{PWR ON RST}}$ returns to Logic-1; the instrument state is initialized by the firmware program. This routine clears the latches, registers and SSDA strobe.

6.4.3.2 Parallel Data Input From CPU

The conditions for parallel data on the data bus to be accepted by the SSDA are as follows:

- a. Chip-select $\overline{\text{SSDA CS}}$ at Logic-0.
- b. Read/Write command $\overline{\text{R/W}}$ at Logic-0. This controls the direction of data flow via the Data Bus through the SSDA input/output port. When $\overline{\text{R/W}}$ is at Logic-0, data on the Data Bus is written into a selected register within the SSDA.
- c. The memory clock 'MEM CLK' 682.6kHz square wave synchronizes the SSDA operating cycle to that of the CPU.

With register address bit A₀ at Logic-1 and input conditions present as above, the SSDA accepts data from the data bus into a 3-byte internal FIFO register. The data is entered over several MEM CLK cycles and stored in the FIFO register in readiness for serial transmission from the SSDA.

When the address bit A₀ is at Logic-0, data transferred into the SSDA are recognised as programming instructions. The SSDA is programmed as part of the initialization routine. For details of 'Control Byte' operation, refer to Motorola 6852 data sheet.

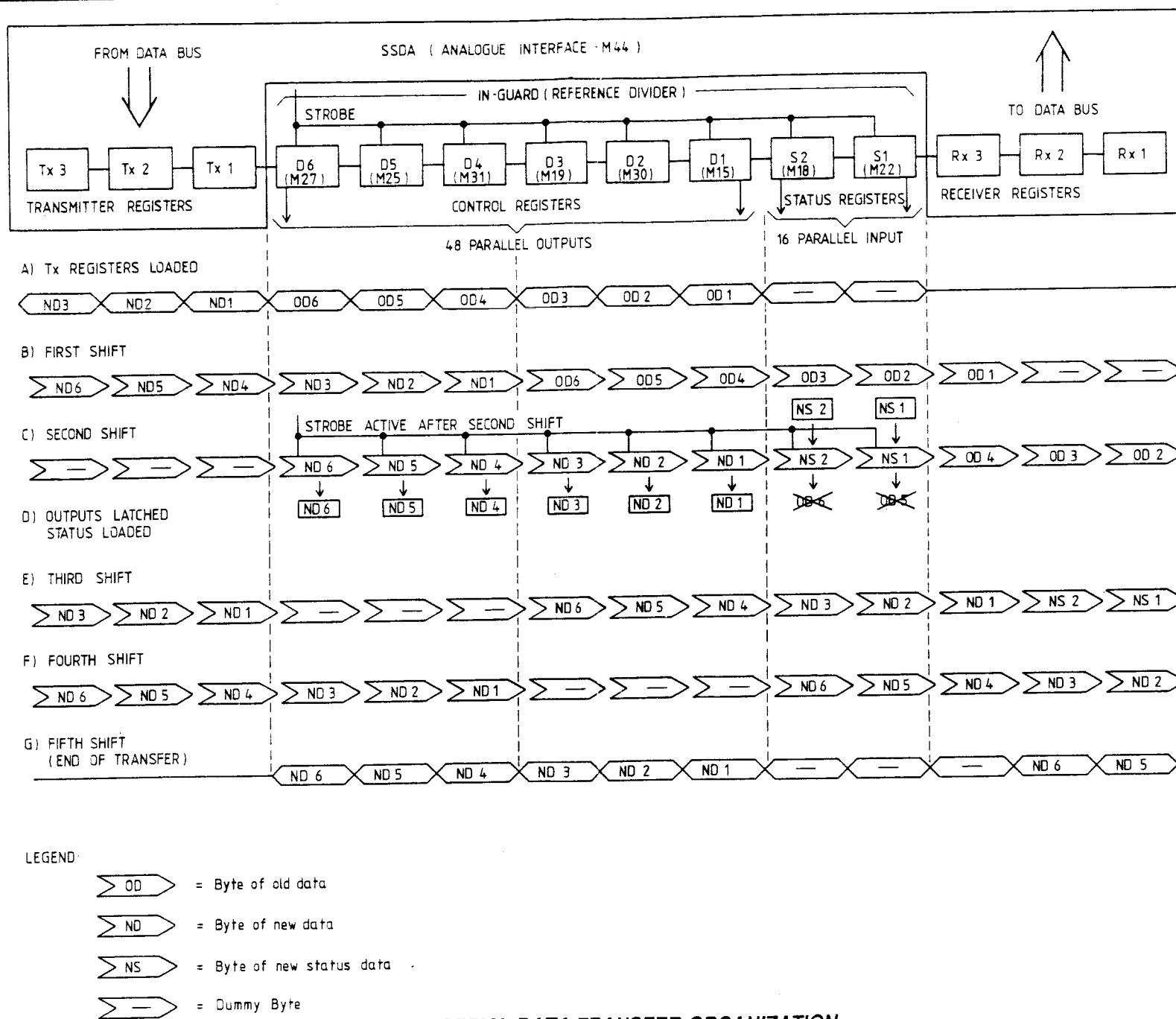


FIG. 6.15 SERIAL DATA TRANSFER ORGANIZATION

6.4.3.3 Parallel Data Output to CPU

The conditions for data to be read back from the SSDA on to the data bus are as follows:

- Chip-select $\overline{\text{SSDA CS}}$ at Logic-0.
- Read/Write command $\text{R}/\overline{\text{W}}$ at Logic-1.
- Memory clock, MEM CLK, present.

The data read from the SSDA may be from one of two sources, selection being made by address bit A_0 :

- With A_0 at Logic-1, received data from the serial data input FIFO is transferred to the data bus.
- With A_0 at Logic-0, the CPU reads an internal SSDA status register.

6.4.3.4 Serial Data Transmission

Serial data transmission is controlled by the $\overline{\text{CTS}}$ (clear to send) input to the SSDA. Transmission is inhibited by $\overline{\text{CTS}}$ at Logic-1, and enabled when $\overline{\text{CTS}}$ is set to Logic-0 by the CPU address-code signal $\overline{\text{AN I/F STRT}}$. The first serial bit is transmitted by the negative transition of the first full positive Tx clock pulse (256 kHz) after $\overline{\text{CTS}}$ has been set to Logic-0. $\overline{\text{CTS}}$ is held at Logic-0 by the $\overline{\text{AN I/F STRT}}$ latch for the duration of 24 full Tx clock pulses, thus enabling the serial shift transmission of the 24 data bits from the Tx Data FIFO in the SSDA.

6.4.3.5 Serial Data Reception

Serial data is received by the SSDA, controlled by the $\overline{\text{DCD}}$ (data carrier detect) level and clocked by Rx CLOCK. $\overline{\text{DCD}}$ is common to the transmit control $\overline{\text{CTS}}$ so that transmission to, and reception from the serial/parallel shift registers is synchronous. Both Rx CLOCK and Tx CLOCK have the same frequency but Rx CLOCK is inverted with respect to the latter. The first bit arriving at its Rx DATA input is clocked into the SSDA Receive FIFO register on the positive transition of the first full Rx clock after $\overline{\text{DCD}}$ is set to Logic-0.

6.4.4 SSDA CLOCK GENERATION

Serial data is transmitted and received in bursts of 24 data bits. Three clocks are used to time the flow of bits, ensuring that:

- Data has time to settle before being clocked along the shift registers.
- The first Rx data sample is taken before it is lost by the first bit-shift.
- Subsequent Rx data has time to settle before being sampled by the SSDA.
- Exactly 24 bits are shifted in each burst.

6.4.4.1 SSDA, Tx and Rx Clock Action

(Fig. 6.16)

The three clocks are derived from the 256 kHz square wave output from the 13-bit counter. The 256 kHz squarewave is used directly as the signal 'Tx CLOCK' into the SSDA.

(Refer to Circuit Diagram 430648 Page 11.3-2 - M15-14).

After $\overline{\text{CTS}}$ is set to Logic-0, the negative transition of the first full positive pulse triggers the first serial Tx data bit setup. (Refer to Fig. 6.16 Waveforms G and H).

'Rx CLOCK' is an inverted version of the 256kHz squarewave. After $\overline{\text{DCD}}$ is set to Logic-0, the positive transition of the first full Rx clock cycle triggers the SSDA. The SSDA thus samples the first Rx data bit before the SSDA clock triggers the shift registers. (Fig. 6.16 Waveforms K and J).

'SSDA CLOCK' is also an inverted version of the 256kHz squarewave. The inversion allows approximately 2ms of data setup time for all serial data bits prior to clocking the data along the shift registers. SSDA CLOCK is gated at M2-3 by the action of M3-12 to ensure that the first Rx data is sampled before it is lost by the first bit-shift. 24 clock pulses are counted by M4, allowing 24 bits to be shifted before resetting the Analog Interface Start latch M2-11 (TP3) to Logic-1.

(Refer to Fig. 6.16 Waveform I).

6.4.4.2 SSDA Clock Circuitry

(Circuit Diagram 430648 Page 11.3-3)

The following paragraphs describe the action of the SSDA clock generator circuitry.

The action of the SSDA clock generator is initiated by the command $\overline{\text{AN I/F STRT}}$ from the CPU. This occurs after the parallel data has been loaded into the SSDA transmit registers from the data bus. The Logic-0 pulse of $\overline{\text{AN I/F STRT}}$ sets flip-flop M2-10/11 to give a Logic-0 at TP3 which then:

- Sets the D input level of flip-flop M3-5;
- Removes 'SET' to enable shift register M3 at M3-6 and M3-8;
- Removes 'RESET' to enable counters M4 at M4-7 and M4-15. (Refer to Fig. 6.16 Waveforms A and C).

At the next rising edge of the inverted 256 kHz (Rx CLOCK) from M43-8 after $\overline{\text{AN I/F STRT}}$, the shift register M3 is clocked but only M3-1 'Q' output changes state to Logic-0. This is applied to the SSDA $\overline{\text{CTS}}$ and $\overline{\text{DCD}}$ inputs, thus releasing the inhibits on the SSDA transmit and receive registers.

(Refer to Fig. 6.16 Waveforms D and E).

At the next (second) rising edge of the clock to M3, M3-12 changes to Logic-1. This allows NAND M2-3 to pass 256 kHz clock pulses via buffer M5-12 to the Reference Divider Assembly to shift the serial data string along the analog-control and status registers.

(Refer to Fig. 6.16 Waveforms D, F and I).

The 256 kHz clock at NAND M2-3 is applied to the 4-bit up-counter clock input at M4-1, each rising edge causing the counter to increment by 1.

The divide-by-16 output M4-6 is applied to enable M4 at its M4-10 input ; the falling edge occurring at count-16 and incrementing the second counter to produce, at M4-11, a Logic-1 output. Later, at count-24, M4-6 changes again to Logic-1, and together with M4-11 output, gives a Logic-0 from NAND M2-4, causing the following actions:

- a. Flip-flop M2-12 is reset to give Logic-1 at TP3.
- b. The Logic-1 at TP3 sets shift register M3 to give:
 - i. Logic-1 at M3-1, thus inhibiting $\overline{\text{DCD}}$ and $\overline{\text{CTS}}$;

- ii. Logic-0 at M3-12, disabling NAND M2-3 and thus stopping any further SSDA clocks.

c. The Logic-1 at TP3 resets the up-counters M4 causing:

- i. the counter outputs to fall to Logic-0, inhibiting further counting;
- ii. NAND M2-5 to rise to Logic-1, re-setting flip-flop M2-12 to prepare for the next $\overline{\text{AN I/F STRT}}$ input.

(Refer to Fig. 6.16 Waveforms I, B, C, E and F).

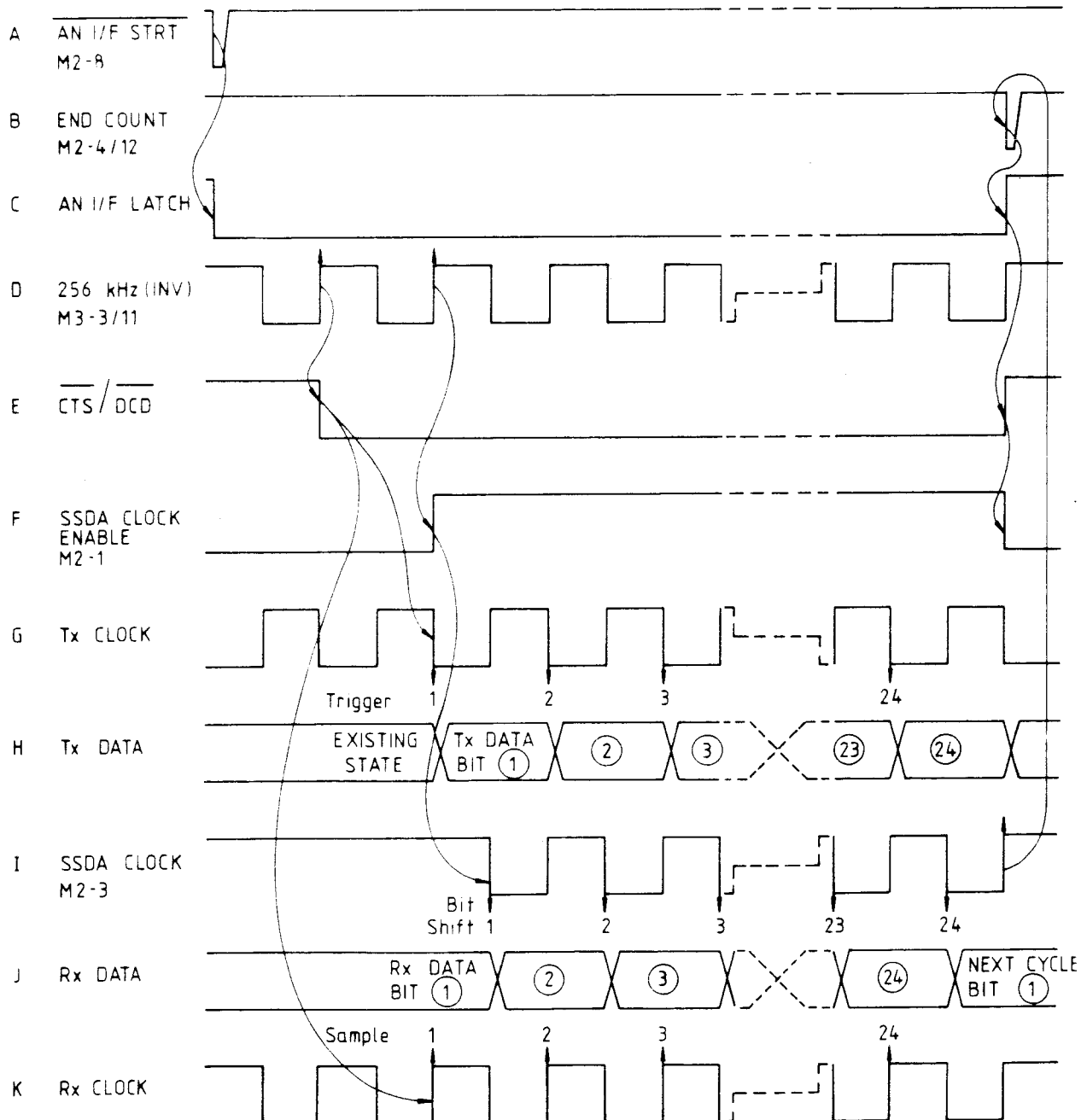


FIG. 6.16 SSDA CLOCK GENERATOR WAVEFORMS

6.4.5 SERIAL/PARALLEL CONVERTER

(Circuit Diagram 430652 Pages 11.4-4 and 11.4-5)

Serial control data transmitted from the SSDA (Analog Interface Assembly), together with their control signals (SSDA strobe and SSDA clock), enter the Reference Divider Assembly via the Mother Assembly.

The data and signals cross the isolation barrier through opto-isolators M6, M7 and M8 into guard.

Serial control and status data is returned out of guard to the SSDA receiver via opto-isolator M1.

6.4.5.1 Logic Levels

The nominal logic levels (Logic-1 = +5V, Logic-Ø = 0V) used in the out-guard SSDA circuits, are offset at the opto-isolator outputs to:

$$\text{Logic-1} = 10\text{V}, \quad \text{Logic-Ø} = 15\text{V};$$

and level-shifted for the in-guard circuitry to:

$$\text{Logic-1} = 0\text{V}, \quad \text{Logic-Ø} = 15\text{V}$$

6.4.5.2 Serial-In/Parallel-Out Control-Data Convertors

Six 8-bit serial shift registers M27, M25, M31, M19, M30 and M15 each have latching parallel outputs. Their serial "D" inputs and "Q's" outputs are cascaded to form a single 48-bit serial shift register. M27 receives 'serial data in' from M8 via the level-shifting buffer M36-4, and M15 passes serial data on to the Parallel-in/Serial-out Status-Data converters.

6.4.5.3 Parallel-In/Serial-Out Status-Data Converters

Two 8-bit serial shift registers M18 and M22 each have parallel inputs. M18 serial "Ds" input accepts serial data from M15; M18 "Q8" output is cascaded to M22 "Ds" input; and M22 "Q8" output delivers SERIAL DATA OUT to buffer M11-11 and back to the SSDA via M1 opto-isolator.

M18 and M22 thus form a 16-bit serial shift register whose 16 parallel inputs' states can be inserted into the serial data string.

6.4.5.4 Serial Data Cycling

The serial data, organized into five blocks of three bytes (*Refer to Section 6.4.2.2*), is accompanied by synchronized bursts of 24 clocks. The output from opto-coupler M7 is buffered via level-shifter M36-2 and then inverted at M14-6. The timing of the positive clock edges allows all bits of serial data (distributed throughout the shift registers) to stabilize before being clocked on.

After the CPU has generated two bursts of data and clock pulses, the serial control data has shifted into the correct positions in control registers M27, M25, M31, M19, M30 and M15. So before the third

burst of three bytes, the SSDA produces a strobe which writes the control data into their parallel outputs. Simultaneously, the strobe also fills the 16-bit serial register of M18 and M22 with the status data present on their parallel inputs.

When the strobe ends, further transfers between serial and parallel registers are disabled. The new control data remains latched in the parallel control registers, and the new status data is in the serial status register ready for shifting to the SSDA Rx DATA register through guard.

The control and status bits in the registers are then circulated by three further bursts of clock pulses, until the CPU has read both the new status data and all the control data that were written by the strobe. Verification that the returned control data is identical to the transmitted data, ends the transfer.

If after three attempts, the returned data does not match the transmitted data; the CPU omits to re-trigger monostable M10 in the Reference Divider Assembly. M10 times out and allows the signal BARK DEL to go to Logic-Ø, disabling the 48 control data outputs by 'tri-stating' the registers M27, M25, M31, M19, M30 and M15.

6.4.5.5 Parallel Control-Data Outputs and Status-Data Inputs

The data latched in M27, M25, M31, M19, M30 and M15 outputs control the operation of the Analog circuitry. The effects are therefore described in the sub-sections relevant to their destinations.

As this is a multi-purpose converter, designed for use in more than one model of instrument, some of the control and status lines are not used.

6.4.6 SAFETY MONITOR (WATCHDOG)

(Fig.6.17)

6.4.6.1 Watchdog Signals

The watchdog circuits continuously monitor the CPU/SSDA functional process. Detection of a processor malfunction by the watchdog results in the following actions:

- a. **BARK.** This signal:
 - i. removes the drive from the primary of the High Voltage (1kV) transformer,
 - ii. disables the 400V Power Supply, and
 - iii. disconnects the Current Assembly output from the instrument output terminals.
- b. **BARK.** This is returned as a status bit to the CPU via the SSDA to signal a failure.
- c. **BARK DELAYED.** This occurs 47ms after BARK and disconnects the AC Voltage Power and Sense circuits from the instrument output terminals.
- d. **BARK DELAYED.** This signal disables the registers of the serial/parallel data converters.

6.4.6.2 Effects at Power-on

The watchdog outputs are manipulated by the power-on reset circuits as follows:

- $\overline{\text{BARK DELAYED}}$ and $\overline{\text{BARK DELAYED}}$ are held active for 80ms from power-on and then are allowed revert to the inactive state only after two SSSA strobes have been detected.
- BARK is forced active until CPU/SSDA functioning has been verified; the latter must occur within 470ms of power-on.
- $\overline{\text{BARK}}$ is held inactive for 470ms from power-on, after which it provides a FAIL message to the CPU.

6.4.6.3 Effects after 'Reset'

Operation of the Reset control on the front panel provides a further 100ms period for the CPU/SSDA functional process to settle, during which time the watchdog circuits must verify correct functioning before their outputs are reset.

6.4.6.4 Watchdog Trip Action

The watchdog is tripped if the system fails to transmit analog-control updates to the analog circuitry. The updates are of two types:

- Transfer of 'Output value' data via the Analog Interface comparators,
- Transfer of analog switching data via the SSSA every 40ms.

The CPU generates pulses at 8ms intervals to verify that the correct output value has been latched into the Analog Interface comparators. These pulses are allowed to pass into guard only if the SSSA verifies that the analog switching data is being transferred normally at 40ms intervals. Once in guard, the pulses prevent the watchdog flip-flops from generating their four BARK output signals, by re-triggering a monostable (M10-4: 18ms) to hold it in its unstable state.

If two or more pulses are missing, M10 releases the hold, and the watchdog flip-flops 'Bark', activating the safety circuitry. They will be missing if the output value comparators are incorrectly updated; if the SSSA fails to generate 'Transmit' pulses for a period exceeding 470ms; or if the CPU crashes.

6.4.7 WATCHDOG CIRCUITRY

6.4.7.1 Out-Guard Watchdog

(Circuit Diagrams 430648 *Section 11.3*
and 430652 *Section 11.4*)

The CPU verifies the validity of each serial-interface transfer by giving the SSSA an instruction to generate a 'Watchdog Enable' trigger. This ' $\overline{\text{W.DOG ENBL SET}}$ ' pulse (M44-7 on *page 11.3-3*), triggers watchdog-enabling monostable M29-11 (*page 11.3-1*).

$\overline{\text{W.DOG ENBL SET}}$ triggering and retriggering extends the natural (470ms) unstable state of M29 indefinitely. Unless the retrigger fails, the M29-9 output ($\overline{\text{W.DOG ENABLE}}$) remains at Logic-0. Absence of $\overline{\text{W.DOG ENBL SET}}$ retriggers, for longer than 470ms, allows M29-9 to restabilize to Logic-1.

$\overline{\text{W.DOG ENABLE}}$ is inverted at M43-3 and applied to NAND gate M46-12 (*page 11.3-4*).

During each successful processor cycle, the CPU addresses M51-9 (Digital Assembly *page 11.2-2*). The resulting low active pulses at 8ms intervals are inverted, and gated with WRT STRB to generate the active-low signal $\overline{\text{W.DOG}}$ at M49-11.

$\overline{\text{W.DOG}}$ travels via the Mother Assembly to the Analog Interface Assembly to be gated with the $\overline{\text{W.DOG ENABLE}}$ signal at NAND M46 (*page 11.3-4*). The resulting signal at M46-13, $\overline{\text{W.DOG}}$, consists of positive-going pulses at 8ms intervals when the CPU/SSDA system is working normally, or a Logic-1 level if the SSSA fails.

The $\overline{\text{W.DOG}}$ signal travels via the Mother Assembly to be passed into guard on the Reference Divider Assembly (Opto-coupler M9 on *page 11.4-5*).

6.4.7.2 In-Guard Watchdog

(Circuit Diagram 430652 Page 11.4-5)

NOTE:

The operating levels of the in-guard CMOS circuits are negatively displaced as follows (nominal voltages):

- Opto-coupler output circuits

Logic-1: -10VDC Logic-Ø: -15VDC

- Digital CMOS circuits

Logic-1: 0V Logic-Ø: -15VDC

Level-shifter M36 carries out the interfacing between these two levels.

The 'W.DOG' signal is opto-coupled into guard by M9. During normal operation: the W.DOG in-guard positive-going pulses, at 8ms intervals, keep re-triggering the monostable M10-4 to give a continuous Logic-Ø at M10-7. The 18ms unstable state of M10 allows for one pulse to be absent, but if two or more pulses are missing, M10 resets, taking M10-7 to Logic-1.

The logic level from M10-7 is connected directly to the set input of flip-flop M13-6. With the reset input to M13-4 held at Logic-Ø during normal operation, the output conditions of M13-1 and M13-2 are as follows:

- Set input M13-6 = Logic-Ø (no fault);
M13-1 (Q) = Logic-Ø - $\overline{\text{BARK}}$ not active
M13-2 (Q) = Logic-1 - $\overline{\text{BARK}}$ not active
- Set input M13-6 = Logic-1 (malfunction);
M13-1 (Q) = Logic-1 - $\overline{\text{BARK}}$ active
M13-2 (Q) = Logic-Ø - $\overline{\text{BARK}}$ active

The action of M13-2 changing to Logic-Ø triggers the monostable M10-11 which has a relaxation time of 47ms. After 47ms, M10-9 output clocks flip-flop M13-11 to give the command BARK DEL from M13-13 and $\overline{\text{BARK DEL}}$ from inverter M14-12.

6.4.7.3 Power-On Reset

(Circuit Diagram 430652 Page 11.4-5)

When power is first applied, the build-up of the 15V supply forces shift register M37 Set inputs to Logic-Ø, but its Reset inputs are held at Logic-1 by the charging action of R122/C7.

So M37 is forced into reset state for about 80ms:

- M37-2 imposes Logic-1 at M13-8 Set input.
- M37-1 at Logic-Ø holds M10 inactive at M10-3, thus preventing random triggering at M10-4 from erratic W.DOG inputs, as the SSDA/CPU functions start up. 'Q' output M10-7 holds M13-6 Set input at Logic-1.

Also, the Reset inputs M13-4 and M13-10 are held at Logic-1 for a period of 470ms from power-on by the signal $\overline{\text{FP RST}}$, generated by the power-on reset action of M53 on the Digital Assembly. (page 11.2-2).

Therefore, the Set/Reset inputs M13-8/M13-10, initially both at Logic-1, force M13-13 output to Logic-1 to give active BARK DELAYED and $\overline{\text{BARK DELAYED}}$ outputs.

The Set/Reset inputs M13-6 and M13-4, also initially at Logic-1, force:

- M13-1 to Logic-1 (Active BARK), and
- M13-2 to Logic-1 (Non-active $\overline{\text{BARK}}$).

The output states of M37 (M37-1 = Logic-Ø, M37-2 = Logic-1) remain unchanged after the 80ms time constant at M37 Reset inputs, but then M37-11 is free to be triggered from the SSDA strobe input. Two strobe inputs must occur before M37-1 clocks to Logic-1 and M37-2 to Logic-Ø. M13-13 now changes to Logic-Ø, making BARK DELAYED and $\overline{\text{BARK DELAYED}}$ inactive, and the inhibit is removed from M10-3.

The outputs M13-1 and M13-2 remain unchanged until M10-7 falls to Logic-Ø by the clocking action of pulses on the W.DOG input. This must occur before M13-4 returns to Logic-Ø (at 470ms from power-on) for BARK to be made inactive, otherwise BARK remains active and $\overline{\text{BARK}}$ is set to Logic-Ø, producing a fail status bit which is passed to the CPU.

6.4.7.4 Malfunction

(Fig 6.17)

Any malfunction which introduces one of the following conditions will cause the watchdog to bark:

- a. CPU WRT STRB fails at Logic-Ø.
- b. M51 on the Digital Assembly does not receive the address to activate M51-9.
- c. Failure of transmission of bursts of the W.DOG ENABLE SET pulses from the SSSA to M29 (The SSSA is not transferring serial data).
- d. The SSSA Strobe is not triggering M37.
- e. W.DOG pulses are not triggering M10.

As well as these failures the CPU is informed, via SSSA Status byte transfer, of certain analog malfunctions. Subsequent CPU action can include deliberate activation of the watchdog by omitting to address M51 as in (b) above.

6.4.7.5 Reset

Once the watchdog has 'Barked' it can be reset, if the malfunction has cleared, by pressing the Reset control on the front panel.

The Reset input to the watchdog circuit, FP RST, is active for 100ms after pressing the Reset key. (M53-9 on Digital Assembly page 112-2). During this period, the Reset inputs at M13-4 and M13-10 are held at Logic-1, allowing the correct pulse inputs from the processor and SSSA to hold M13-6 at Logic-Ø, and to reset BARK DEL at M13-13 to Logic-Ø. The watchdog will not reset if the malfunction persists.

DIGITAL PCB ASSEMBLY

ANALOG INTERFACE ASSEMBLY

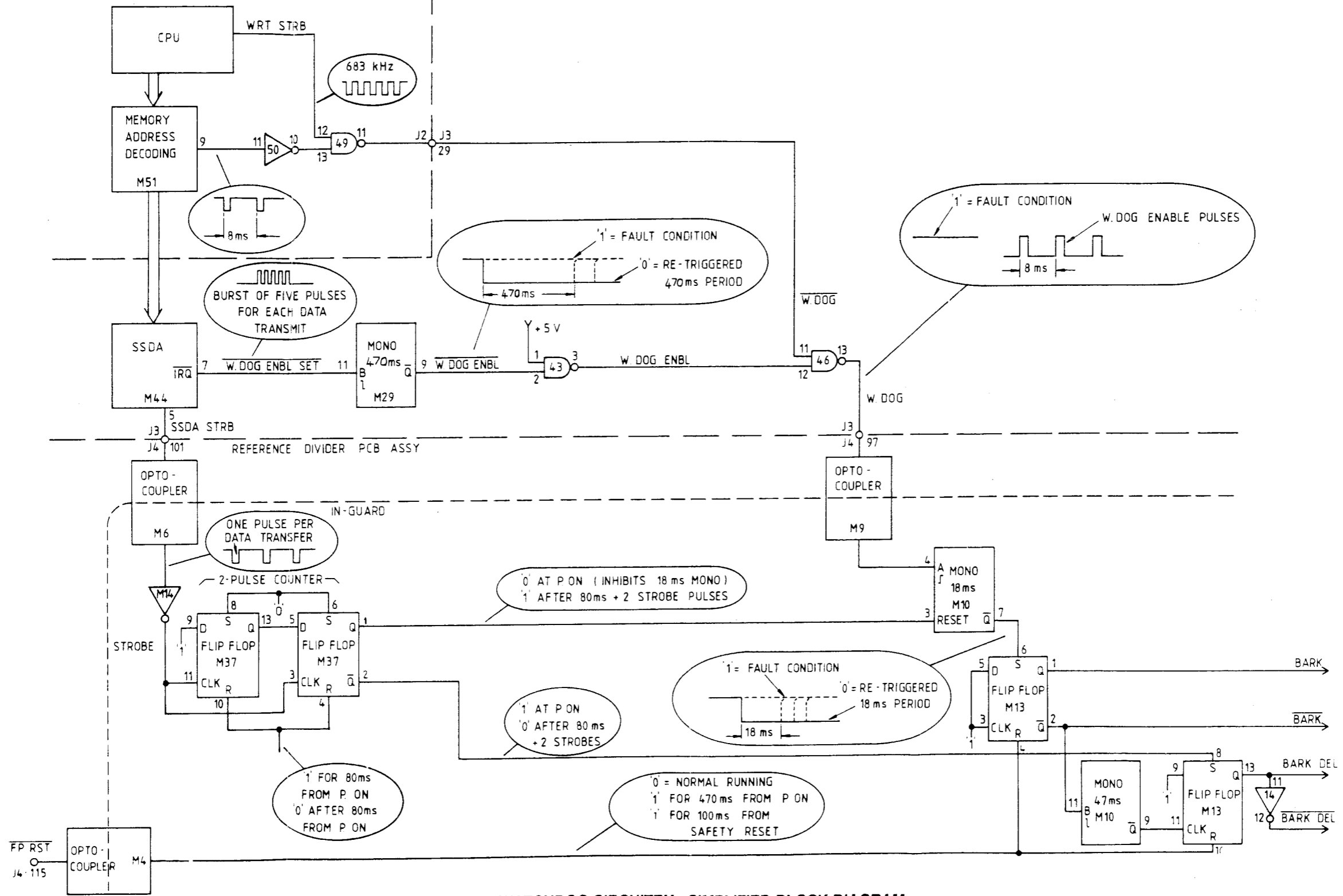


FIG. 6.17 WATCHDOG CIRCUITRY - SIMPLIFIED BLOCK DIAGRAM

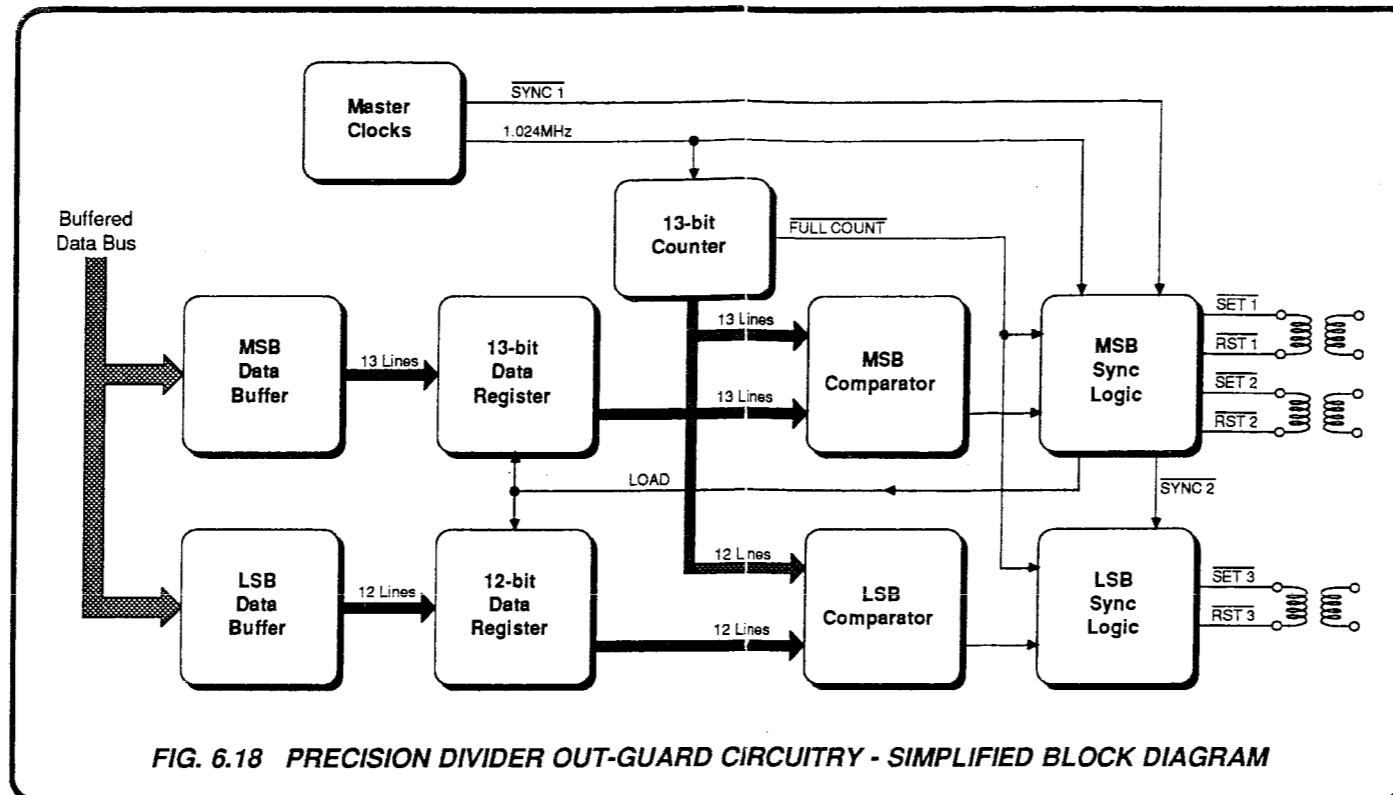


FIG. 6.18 PRECISION DIVIDER OUT-GUARD CIRCUITRY - SIMPLIFIED BLOCK DIAGRAM

6.5 PRECISION DIVIDER

The out-guard circuitry described in this section performs the following functions:

- Receives and latches the demanded output value from the CPU in the form of a 25-bit word.
- Generates a continuous 13-bit up-count from the 1.024MHz Master Clock (8ms count cycle).
- Compares the 13-bit count with the 13 most-significant bits of the 25-bit word, generating 'Set' and 'Reset' pulses. These are transferred into guard to trigger the 'Most Significant' JFET switch in the Reference Divider.
- Compares the 12 most-significant bits of the count with the 12 least-significant bits of the 25-bit word, generating 'Set' and 'Reset' pulses. These are transferred into guard to trigger the 'Least-Significant' JFET switch in the Reference Divider.

The out-guard circuitry is located on the Analogue Interface Assembly.

The in-guard circuitry performs the following functions:

- Provides a Master Reference Voltage (20.6V) which is chopped by the 'Most Significant' JFET switch to generate a square-wave, whose Mark/Period ratio is controlled by the 13 most-significant bits of the 25-bit word. A 7-pole Bessel filter smooths the square-wave to provide a DC voltage, whose value varies directly as the Mark/Period ratio of the MSB square-wave.
- Provides a Buffered Reference Voltage (8.83V) which is chopped by the 'Least-Significant' JFET switch to generate a square-wave, whose Mark/Period ratio is controlled by the 12 least-significant bits of the 25-bit word. A 3-pole Bessel filter smooths the square-wave to provide a DC voltage, whose value varies directly as the Mark/Period ratio of the LSB square-wave.
- Conditions the two DC voltages produced by the Bessel filters, delivering them via full 4-wire connections to be summed on either the DC assembly (for DC output selections) or on the AC assembly (for AC outputs) as a DC 'Working Reference'.

The value of this reference voltage is accurately proportional to the value demanded by the CPU's 25-bit word. For DC outputs, with polarity changeover switching, it can have values between +20V and -20V (including zero); but as a reference for AC outputs, its value lies between +0.126V and +2.79V.

- For AC outputs only, the in-guard circuitry digitally generates a stepped AC reference voltage whose peak value is equal to the DC Working Reference Voltage. This gives the Sense/Reference Comparator (described in sub-section 9.5) the considerable advantage of comparing AC Sense against AC Reference. (If AC were compared with DC, small DC off-sets would magnify and lead to 'DC turnover' errors). The AC waveform is constructed in ten steps by a digitally controlled switching network. It has been given the name 'Quasi-Sinewave'.

The in-guard circuitry is located on the Reference Divider Assembly.

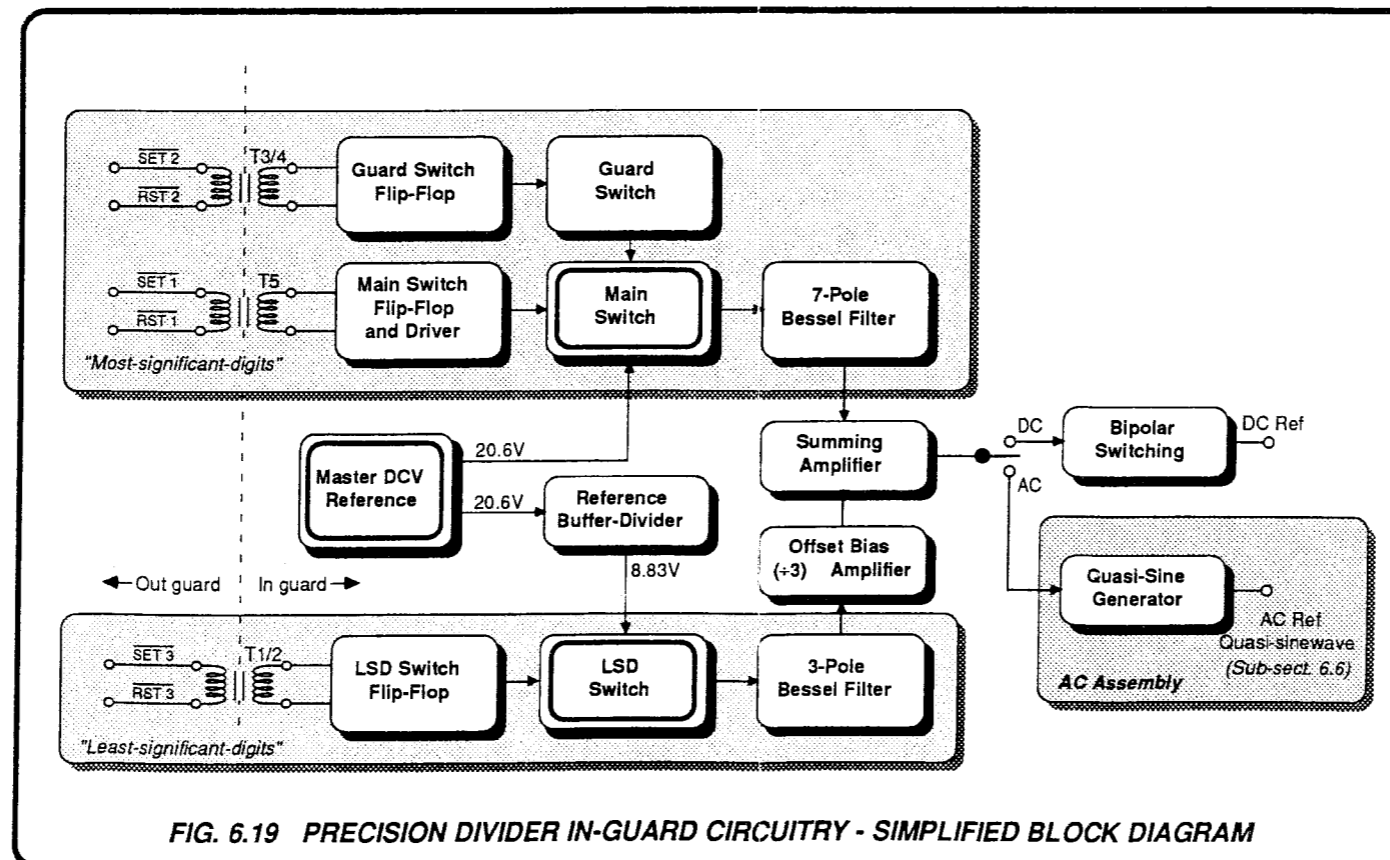


FIG. 6.19 PRECISION DIVIDER IN-GUARD CIRCUITRY - SIMPLIFIED BLOCK DIAGRAM

6.5.1 PRECISION DIVIDER COMPARATORS

(Circuit Diagram No. 430648 *Section 11.3*)

6.5.1.1 General (*Figs. 6.18 and 6.19*)

The comparators are designed as a means of translating a binary word into the accurately defined Mark/Period ratio of a square-wave. The ratio of the square-wave's average value to its peak value subsequently defines the division ratio applied to the Master Reference, and must be adjustable at high resolution.

The required decimal resolution translates into a 25-bit binary word, each bit needing to exert control of the division ratio. A single comparator of this length would require more than 30 million clocks to scan, which at sensible clock frequencies would occupy several seconds. To filter out the resultant chopping frequency would require large and expensive components, and force unrealistic operational time constraints.

In the Datron Precision Divider, the 25-bit word is split into two parts (13 most-significant bits - MSB; 12 least-significant bits - LSB), a scan-cycling frequency as high as 125Hz is obtained.

Both MSB and LSB comparators are scanned concurrently by the same 13-bit counter, forming two separate square-waves. These act on two separate reference divider switches and filters to generate two separate DC voltages which are subsequently recombined, giving the required resolution.

In summary, the two comparators translate information from the CPU into time-related pulses which control mark/period switching in the reference divider. One comparator operates on the thirteen most-significant bits of CPU data; the other deals with the twelve least-significant bits. The comparators perform concurrently, cycling continuously at 125Hz, taking 8ms per full count.

At the start of each 8ms counting period, each comparator generates a SET pulse to start its reference divider 'Mark' element. Then after precisely-measured delay times, each generates a RESET pulse to terminate the 'Mark', and start the 'Space'.

At each 8ms full-count, the clock resets and continues up-counting from zero.

6.5.1.2 Comparator Operation (*Fig. 6.18*)

The MSB and LSB Data Buffers are periodically loaded and latched with binary 'Demanded Output Value' data under the control of the CPU.

At the end of each comparator counting cycle, the 13-bit counter FULL COUNT output enables the generation of set pulses SET 1, SET 2 and SET 3 by the MSB and LSB 'Sync Logic' circuits.

FULL COUNT also generates the LOAD command. This writes the data, currently latched in the buffers, into working data latches which form the 13-bit and 12-bit Data Registers, updating the earlier 'Demanded Output Value' which is resident in the comparator.

The MSB and LSB comparators translate this binary data into 'RESET' pulses, whose time relationships to the 'SET' pulses are established by the value of their binary words.

6.5.1.3 13-Bit (MSB) Comparator

(Circuit Diagram No. 430648 *Page 11.3-2*)

The 13 binary outputs of the up-counter scan the 13 Exclusive-OR elements of the MSB Comparator. With the least-significant bit at 512kHz, and the most-significant at 125Hz, the 8ms scan time thus divides into 8192 time elements, each of 977ns.

Each time element has a unique binary code, incrementing by one bit on its predecessor. When this coincides with the bit-pattern set in the data register, the comparator provides an output pulse to the MSB sync logic. The latter generates reset pulses $\overline{RST\ 1}$ and $\overline{RST\ 2}$ in synchronism with the signal SYNC1 (2.048MHz).

6.5.1.4 12-Bit (LSB) Comparator

(Circuit Diagram No. 430648 *Page 11.3-1*)

This functions in the same manner as the MSB comparator, but scanning only twelve bits over the same 8ms counting period, thus accommodating 4096 time elements of 1954ns for each binary increment.

SYNC2 pulses, generated in the MSB Sync Logic circuitry at half the rate of SYNC1, synchronize the $\overline{RST\ 3}$ output from the LSB Sync Logic.

6.5.2 COMPARATOR CIRCUIT ACTION

6.5.2.1 Input Data Latches

(Circuit Diagram 430648 *Pages 11.3-1 and 11.3-2*)

The input buffered data latches M31 to M34 and M37 to M39 receive 27 data bits in four bytes from the buffered data bus. Latches are selected by signals REF DIV 1, 2, 3 or 4 from the memory address decoding on the digital pcb. Data is clocked to the 'Q' outputs of the latches on the positive-going edge of $\overline{WRT\ STRB}$.

Data from the input latches is used as follows:

25 bits form a data word to the comparator registers M47, M48, M49 (part), M51 and M52. The remaining 3 bits from the data latches are used for separate functions:

- M34-5 triggers monostable M29 (part), whose Q output is inverted and buffered to provide the control $\overline{UPD\ (OG)}$ used in the relay drive logic for analog switching.
- M34-4 (EXT FREQ SEL) selects between the internal 16kHz synchronizing frequency and the 16kHz output from the External Frequency Input Buffer.
- M34-3 (\overline{BEEP}) triggers the Beeper monostable M55, which is activated to draw attention to display messages.

6.5.2.2 13-Bit Counter

(Circuit Diagram 430648 Page 11.3-2)

(Refer to Fig 6-20 for Waveforms)

The counter consists of three 4-bit binary counters M15, M16, M17 and J-K flip flop M42 (half dual package). The squarewave outputs from the counter are on 13 binary-coded lines, the first (least-significant) being a 512kHz squarewave, the others successively divided in frequency to the most significant output of 125Hz.

Bit 1 is provided by J-K flip flop M42, which toggles on each falling edge of the 1.024MHz clock to give 512kHz Q and \bar{Q} outputs. These outputs are used as follows:

- a. The two complementary 'Q' outputs together provide the least-significant input to the 13-bit comparator;
- b. The Q output controls the counting rate of M15, synchronizes M16 and M17, and is used in the gating of FULL COUNT.

Counters M15, M16 and M17 are cascaded as a 12-bit counter and are synchronously clocked by the 1.024MHz. M15 can count only when its count-enable input M15-7 is set to Logic-1 by the Q output of M42.

As M42 output is at 512kHz, clocking of M15 occurs on the rising edge of alternate 1.024MHz clocks, thus giving outputs of 256, 128, 64 and 32kHz squarewaves from M15.

Counter M16 is enabled by the carry output from M15 together with 512kHz from M42 at the count-enable pins M16-10 and M16-7 respectively, thus giving outputs of 16, 8, 4 and 2kHz squarewaves from M16.

Counter M17 functions in a similar manner to give outputs of 1kHz, 500, 250 and 125Hz squarewaves.

The 2μs-long 'Carry' output from M17 occurs at the end of the 125Hz output when all counter outputs are at Logic-1. The carry output is NAnDED with M42Q output to give the 1μs-long logic command FULL COUNT. The counting cycle resets and continues, starting from bit 1.

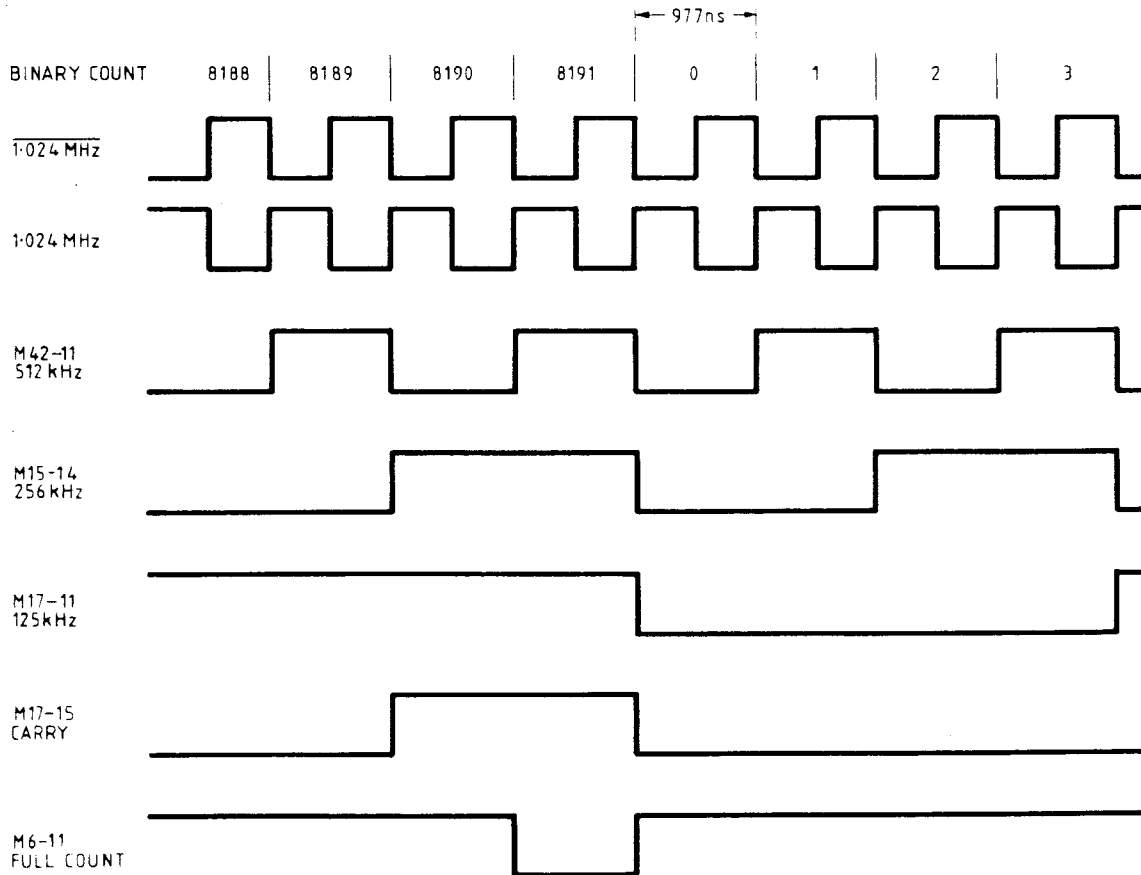


FIG. 6.20 13-BIT COUNTER WAVEFORMS

6.5.2.3 13-Bit Comparator Action
(Circuit Diagram 430648 Page 11.3-2)

The 13-bit comparator provides a Logic-1 output at TP12 whenever a coincidence occurs between the following two sets of data:

- a. Data set in registers M47, M48 and M49-1;
- b. Data from 13-bit counter M42, M15, M16 and M17.

Twelve exclusive-OR elements M25, M26, M27 and three NOR gates of M12 are used to detect a coincidence. The data in the registers is preset by the CPU, while that presented by the 13-bit counter cycles through every binary combination possible on 13 lines.

Two coincident inputs to an exclusive-OR gate provide a Logic-0 to the 12-input NOR gates M24/M23; full coincidence in bits 2 to 13 is shown by a Logic-0 at NAND M13-6. Coincidence at bit 1 is shown by Logic-0 at M12-13 and M12-4 (M12 acting as an exclusive-OR gate) as follows:

| M12 INPUT PINS | | | OUTPUT PINS | |
|----------------|----|------|-------------|----|
| 6 | 11 | 9/12 | 4 | 13 |
| 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 | 0 |

} Only 4 input combinations available

A $\overline{\text{BUSY}}$ signal is generated by the comparator at NAND M50-13 (TP2) when the 13-bit counter approaches full count. Bits 8 to 13 are at Logic-1 for the period of 125 μs preceding the end of the counter cycle (see Fig. 6-21). The $\overline{\text{BUSY}}$ level is applied to the M49 D-input at pin 9 and is synchronously clocked through as the signal $\overline{\text{REF BUSY}}$ to buffer M45-2 by 1.024MHz.

As described earlier, the demanded output value is defined by the CPU to a resolution of 25 bits, contained in four data bytes. The time needed for the 4-byte transfer could allow the latches to contain

spurious data until they were fully loaded, and an inaccurate parity could be registered with the counter still running. The counter must not be interrupted, as its full count defines the 'period' of the mark-to-period ratio used to control the division of the reference voltage. It is therefore necessary to reduce the loading time, and this is achieved by double-latching the data.

When the CPU has data to load into the input data latches, it first interrogates the comparator by enabling buffers M45 using the signal $\overline{\text{REV DIV RD}}$. The $\overline{\text{REF BUSY}}$ signal at Logic-1 (M45-3) indicates to the CPU that enough time is available to load the latches (at least 125 μs remain before the LOAD pulse occurs).

If the $\overline{\text{REF BUSY}}$ signal is at Logic-0, the CPU waits until it returns to Logic-1 again.

When the $\overline{\text{REF BUSY}}$ signal is at Logic-1, the CPU loads the data by first carrying out four transfers of one byte each into the seven quad buffer latches M31 to M34, and M37 to M39. Each byte's destination is addressed by one of the chip-select signals $\overline{\text{REF.DIV.1}}$ to $\overline{\text{REF.DIV.4}}$, which enables the selected buffer latches. The data is latched by the $\overline{\text{WRT STRB}}$ signal.

Once the full 25-bit word has been latched into the buffers, it is available as a single word at the data inputs of the comparator latches M47, M48, M49, M51 and M52. The CPU again interrogates the comparator by $\overline{\text{REV DIV RD}}$, and five of the elements of M45 buffer the five most-significant data bits back to the CPU. If parity with the transmitted data is confirmed, the CPU takes no action. When the counter times out, the $\overline{\text{FULL COUNT}}$ signal is clocked through to M14-6 by $\overline{\text{SYNC 2}}$ as the LOAD signal, and the new data is transferred into the comparator latches.

If the data latched in the buffers is not as transmitted, the CPU initiates the FAIL 4 message procedure to the operator.

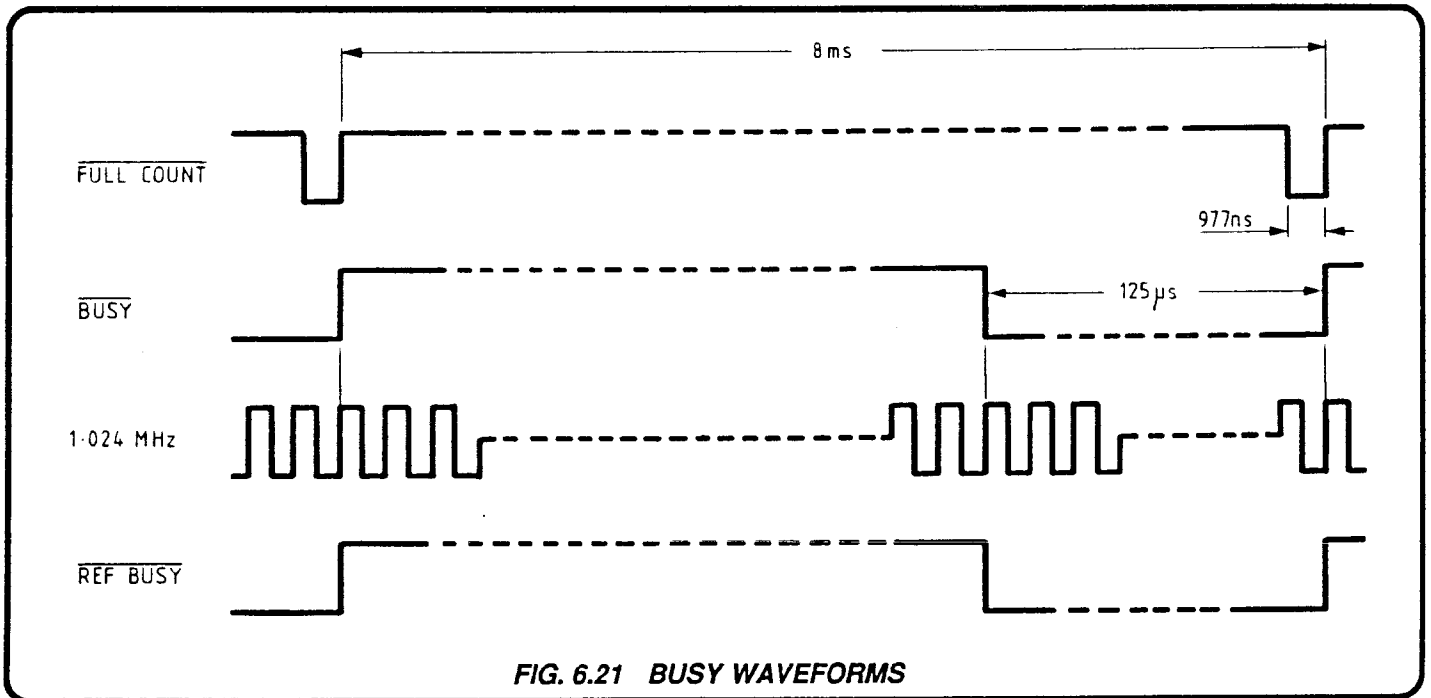


FIG. 6.21 BUSY WAVEFORMS

6.5.2.4 'Most Significant Bits' SYNC Logic

(Circuit Diagram 430648 Page 11.3-2)

(Refer to Fig. 6.22 for Waveforms)

This circuit, M14, M6, M7 and M8, provides the following signals: $\overline{\text{SYNC 2}}$, LOAD, $\overline{\text{SET 1}}$, SET 2, $\overline{\text{RST 1}}$ and $\overline{\text{RST 2}}$.

$\overline{\text{SYNC 2}}$ is obtained by NAND gating 1.024MHz and SYNC1 to give a synchronizing pulse at half the rate of SYNC1.

The LOAD pulse enables the 13-bit comparator registers, and is generated at M14-6 at the end of the counter's full-count output. FULL COUNT sets the D input M14-2 and the level is clocked, inverted, from M14-6 by the next two $\overline{\text{SYNC 2}}$ pulses that occur.

The inverse of LOAD is used to time the pulse $\overline{\text{SET 1}}$ by NOR-gating at M7-4 with 1.024MHz. The M7-4 pulse is NAND-gated

with SYNC1 to provide $\overline{\text{SET 1}}$ from M8-1. The pulse $\overline{\text{SET 2}}$, which occurs 977ns before $\overline{\text{SET 1}}$, is obtained by gating the signal FULL COUNT with 1.024MHz at NOR M7-10 and then NAND-gating at M8-10 with SYNC1.

Reset pulse generation (see Fig. 6.23) is initiated by a Logic-1 level at TP12. This can occur at any one of the 8192 binary counts of the 13-bit counter, its actual time slot depending on the binary count at which the coincidence occurs.

The coincidence level at TP12 is NAND gated at M6-8; M6-10 being at Logic-1 for all binary counts except 8191. The Logic-0 at M6-8 is NOR-gated at M7-1 with 1.024 MHz, this is then used to select the next SYNC1 pulse via NAND M8-4 to provide the pulse $\overline{\text{RST 1}}$.

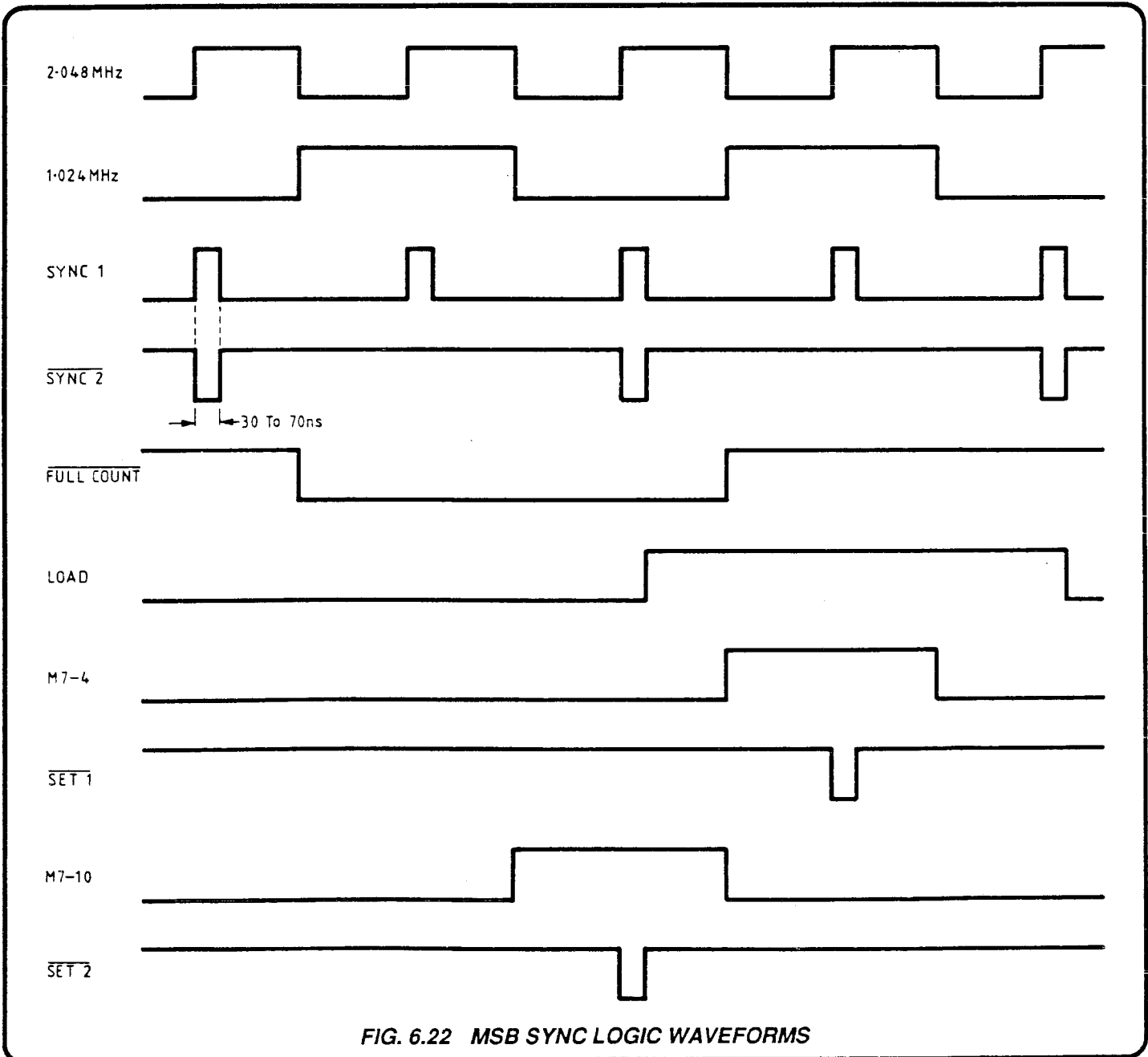


FIG. 6.22 MSB SYNC LOGIC WAVEFORMS

The coincidence level at TP12 is used to set the D input at flip-flop M14-12. This level is clocked to NAND M6-5 by the next SYNC 2 pulse. NAND input M6-4 is at Logic-1 except when LOAD is active, thus M14-9 output is inverted at M6-6 to be NOR-gated with 1.024MHz at M7-13. This is then used to select the next SYNC1 pulse via NAND M8-10 to provide the pulse $\overline{RST\ 1}$.

The pulse-timing example given in Fig.6.23 shows the generation of $\overline{RST\ 1}$ and $\overline{RST\ 2}$ when coincidence occurs in the comparator at binary count = 0 (waveforms in continuous lines).

Coincidence occurring at binary count 1 causes $\overline{RST\ 1}$ and $\overline{RST\ 2}$ to increment in time by 977ns with respect to the SET 1 and SET 2 pulses (waveforms in broken lines).

$\overline{RST\ 1}$ and $\overline{RST\ 2}$ are generated with the same relationship in time to the comparator coincidence when the latter occurs in any binary count time slot from 0 to 8190 (inclusive).

Note that as the comparator word increments in value, $\overline{RST\ 1}$ and $\overline{RST\ 2}$ increment in time after SET 1 and SET 2, which remain stationary with respect to FULL COUNT and LOAD.

$\overline{RST\ 1}$ and $\overline{RST\ 2}$ are inhibited when coincidence occurs at binary count 8191 to allow for the re-loading of the input registers at the end of the counter cycle. The inhibit is performed by the level of FULL COUNT going to Logic-0 and NAND M6-10, preventing $\overline{RST\ 1}$ being generated; and by flip-flop M14-5 output going to Logic-0 for the period of the load pulse, inhibiting $\overline{RST\ 2}$.

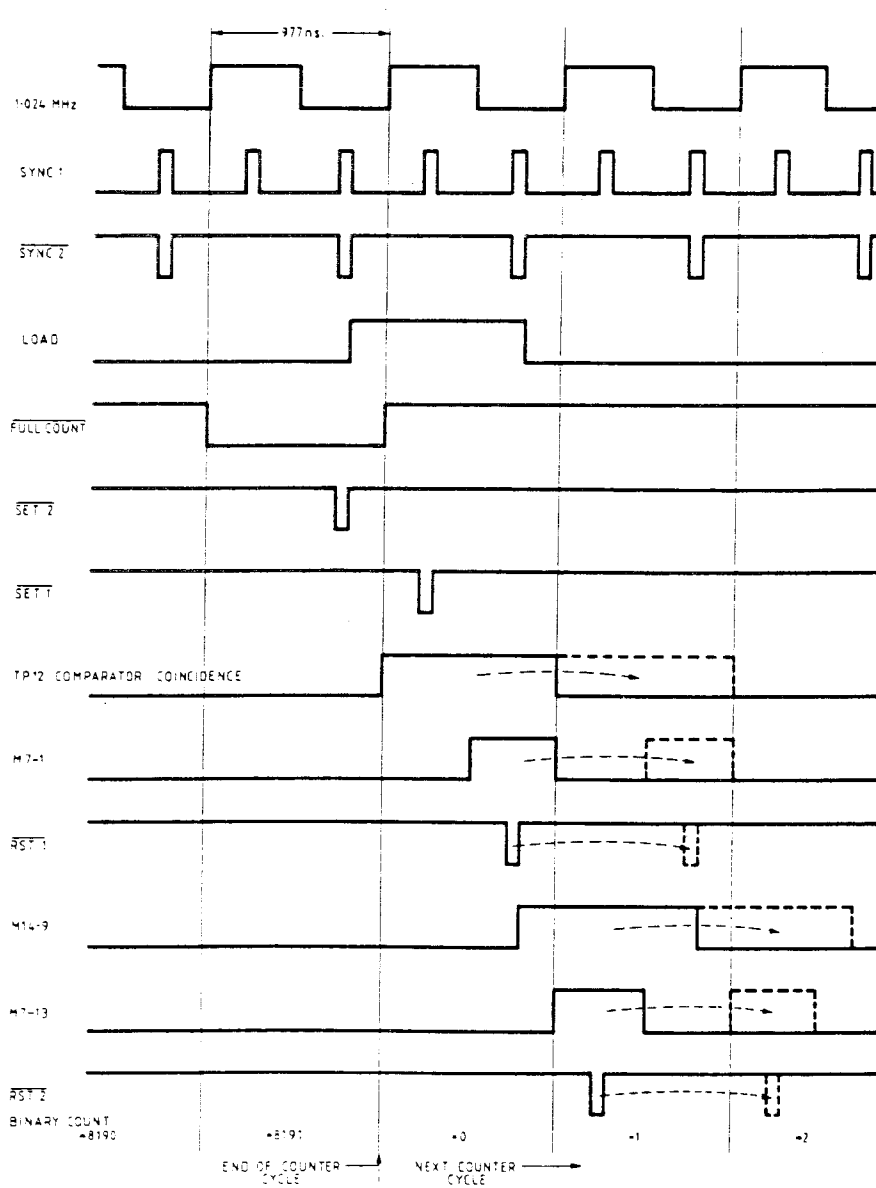


FIG. 6.23 MSB SET/RESET PULSE GENERATION

6.5.2.5 12-Bit Comparator Action
(Circuit Diagram 430648 Page 11.3-1)

This functions in an identical manner to the 13-bit comparator previously described. Twelve exclusive-OR gates, M19, M20 and M21, receive the 12-bit binary output from the common counter and compare these bits with the data in the data registers.

The least-significant bit changes at a rate of 256kHz, and the most-significant bit at 125Hz. Coincidence occurring in any of the 4096 binary-count time slots available in the comparator cycle is shown as a Logic-0 at TP5 for a period of 1954ns.

6.5.2.6 'Least Significant Bits' SYNC Logic
(Refer to Fig. 6.24 for Waveforms)

The timing of $\overline{\text{SET 3}}$ is controlled by the $\overline{\text{FULL COUNT}}$ pulse from the 13-bit counter. The inverted $\overline{\text{FULL COUNT}}$ at M43-6 is gated with the inverted $\overline{\text{SYNC 2}}$ from M43-11 to give, at M46-1, $\overline{\text{SET 3}}$.

The comparator coincidence logic level is inverted to Logic-0 at M12-1; M12-2 being at Logic-0 except when $\overline{\text{FULL COUNT}}$ is low. The waveform at M12-1 lasts for 1954ns and therefore allows two consecutive $\overline{\text{SYNC 2}}$ pulses to be gated to M46-4 ($\overline{\text{RST 3}}$).

This condition exists for all $\overline{\text{RST 3}}$ timings except at the binary count of 4095; in this instance, the $\overline{\text{FULL COUNT}}$ pulse occurs after the gating of the first $\overline{\text{SYNC 2}}$ pulse, sets M12-2 to Logic-1 and so prevents the second pulse appearing at $\overline{\text{RST 3}}$. In practice, the second pulse of $\overline{\text{RST 3}}$ has no operational significance.

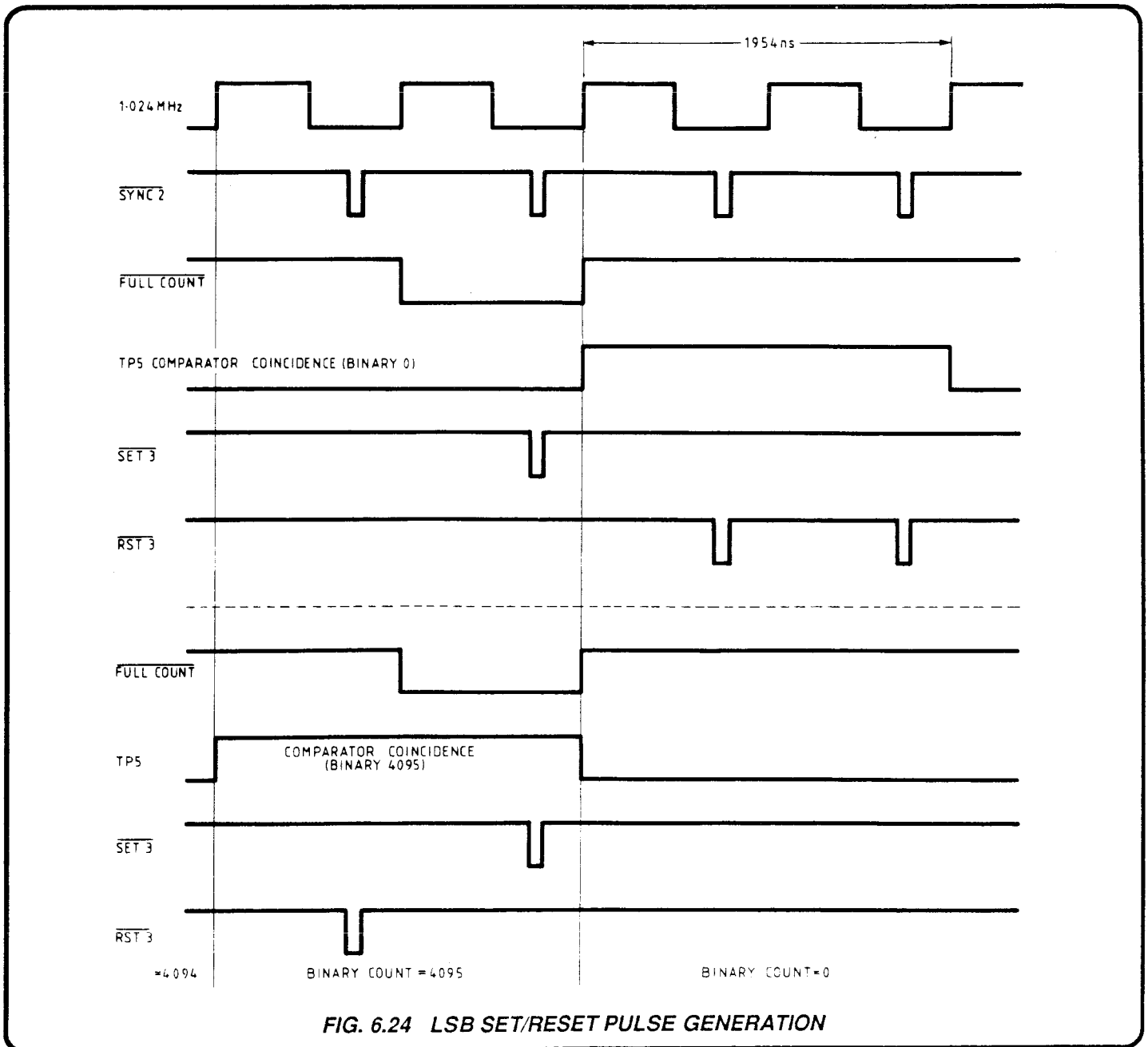


FIG. 6.24 LSB SET/RESET PULSE GENERATION

6.5.3 REFERENCES and REFERENCE DIVIDER

(Circuit Diagrams 430652 Section 11.4)

(Refer also to Fig. 6.19)

The set and reset pulses from the precision divider comparators control the timing of JFET switches, which in turn chop the Master Reference voltages.

The chopped references are filtered to generate two voltages whose levels are proportional to the MSB and LSB squarewaves' mark:period ratio (duty cycle). These MSB and LSB voltages are conditioned, and transferred to the AC Assembly by full 4-wire sensed connection where they are summed at a star-point to generate a Working Reference: 'REF+Ve'. The output voltage increments at high resolution (0.03ppm: approx. 0.6 μ V), with a maximum possible range of adjustment of 0-20V.

The high resolution associated with the full 13-bit count and a 20V reference is advantageous for DC outputs. Such resolution, however, is not strictly necessary for the accuracies associated with AC outputs; and also the 1V Range is the basic AC range, all other ranges employing either attenuation or amplification.

For AC outputs, therefore, the working reference is reduced to a range from 0.126V to 2.79V by software. This results in a reduction of the maximum mark:period ratio of the chopping waveform to about 0.14.

6.5.4 MASTER REFERENCE

(Circuit Diagram DC400761 Page 11.4-2)

The Master Reference determines the fundamental long and short term stability of the whole calibrator. It is a separate PCB mounted on the Reference Divider assembly.

(Refer to the Layout Drawing facing Page 11.7-7)

At the heart of the reference circuit is the zener diode chip M2, which also contains a coarse temperature compensating element (the base-emitter junction between pins 4 and 7) and a temperature sensing element (the base-collector junction between pins 6 and 8). The voltage generated across pins 6 and 8 varies with the temperature of the chip M2, which also contains the Zener Diode element. Amplifier M1A and associated circuitry provide a constant current bias for the zener diode element and temperature compensating element of M2. Amplifier M1B and the circuitry associated with it detect the temperature of the chip M2 and drive a variable current through the heater element between pins 1 and 2. Careful design of the entire thermal and electrical system ensures that this feedback loop, when equilibrium is reached, will maintain the temperature of the Zener Diode chip to within a few millidegrees.

The output of the Zener Diode is approximately 7.2V, which is amplified to 20.6V by amplifier M3. This is an approximate value, but it has high time and temperature stability. Correction constants are stored for the Absolute Reference value are stored in non-volatile memory and applied to affect the mark/period ratio of the JFET Reference Divider switching squarewave. During Instrument recalibration, these constants are updated. M4 and Q2 provide a remote sensing 4-wire drive of this voltage to the 'Most Significant' Switch in the Reference Divider.

The master reference circuit, including Zener Diode chip, temperature control amplifier, output amplifier and 4-wire sensing amplifier are assembled, conditioned and tested as a single entity, and therefore there is no method of repairing and testing a reference module without specialized test equipment and processes. If a fault is suspected on the Reference PCB Assembly, (DC400761), contact your Datron Service Center.

6.5.5 REFERENCE BUFFER-DIVIDER

(Circuit Diagram 430652 Page 11.4-2)

R80 and R81 drop the 20.6V Master Reference voltage (V Ref) to +8.83V. M23/Q40 is a voltage-follower providing +8.83V with respect to Common-4 at the star-point TP11 to supply the Least-Significant Digit switch.

6.5.6 LEAST-SIGNIFICANT-DIGITS SWITCHING
(Fig.6.26)

6.5.6.1 Switch Driver

$\overline{\text{SET}}\ 3$ and $\overline{\text{RST}}\ 3$ pulses from the LSB Comparator in the Analog Interface Assembly are transferred into guard via pulse transformers T1 and T2, whose centre-tapped secondaries are balanced about Common-4 0V (T1) and +9V (T2).

Q5-Q8 form a fast bistable using emitter-coupled logic, to switch TP1 between +9V (mark) and +20V (space). During the "Mark" time after $\overline{\text{SET}}\ 3$ pulse, Q29 and Q30 are switched ON, connecting LKA to +9V Ref. Q1-Q4 have the same bistable action as Q5-Q8, switching Q31 off during the "Mark" period by -11V at TP2, thus disconnecting LKA from Common-4 (0V). During the "Space" time after $\overline{\text{RST}}\ 3$ pulse, Q29 and Q30 disconnect LKA from +9V Ref, and Q1-Q4 switch Q31 on, connecting LKA to Common-4 (0V). Fig.6.26 demonstrates this action.

6.5.6.2 JFET Switch and 3-Pole Filter

The combined action of the switch FETs alternately provides charging current for the 3-pole filter (during "mark") and discharging current (during 'space').

Two JFETs in parallel (Q29 and Q30) are necessary to equalize the charging and discharging time-constants by matching the "ON" resistances. This preserves linearity of the filter output voltage over the full range of mark/period ratios applied via the set and reset pulses.

The 3-pole filter has the advantage of not being in series with the DC output signal. The 125Hz ripple content is reduced to a level which is acceptable within the overall instrument specification. The filter output is buffered by voltage-follower M16.

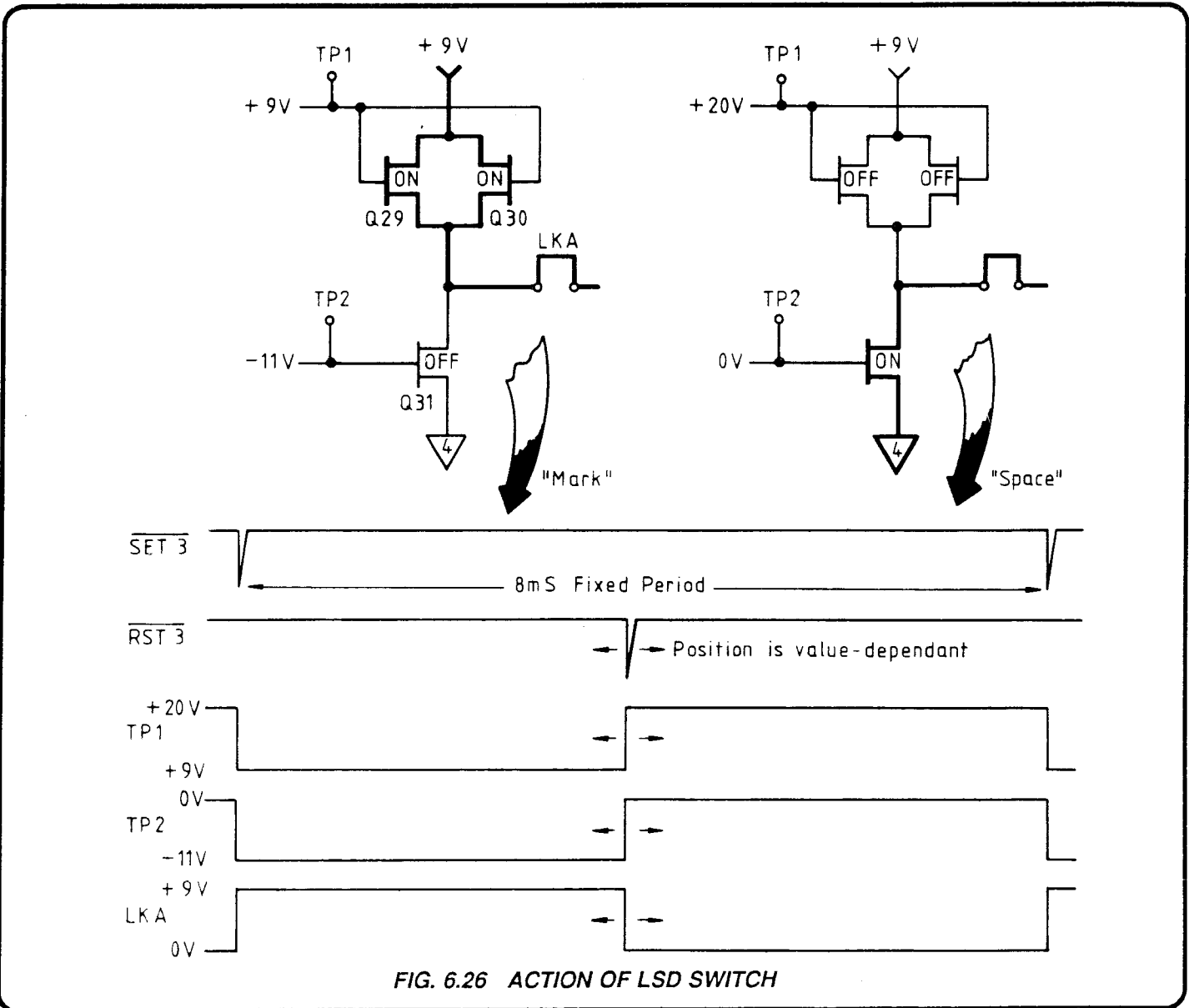


FIG. 6.26 ACTION OF LSD SWITCH

6.5.6.3 Offset Bias Amplifier

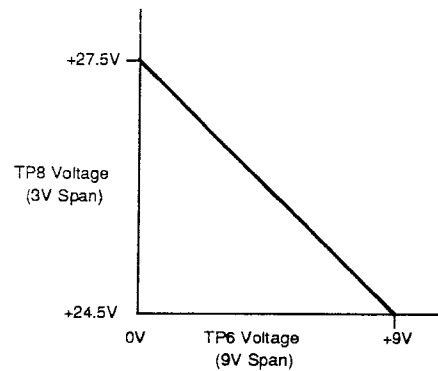
M20 performs a dual role:

- a. Its gain is set to 1/3 by R65/R64
- b. Its output is level-shifted to provide an offset bias for summing (this allows the summed output to have a negative zero offset).

Also a small thermal coefficient zero correction is factory-preset (D10/R85).

M20 transfer function is approximately as shown.

The actual values are as set digitally in software, affecting the mark:period ratio of the J-FET switches, using stored calibration constants.



6.5.7 MOST-SIGNIFICANT-DIGITS SWITCHING (Circuit Diagram No. 430652 Page 11.4-1)

The large reference voltage (20.6V) and the need for higher resolution makes the MSB Switching circuitry more complex than for LSB; but the principle is the same: the set and reset pulse-timing adjusts the mark:period ratio of the square wave fed to the filter.

The arrangement used for the MSB switching satisfies two essential requirements:

- a. The charge and discharge path resistances for the 7-pole filter must be closely matched.

- b. The leakage current of the path switched off must be minimal.

Requirement (a) demands that the matched devices used in both paths are of the same type (P-channel JFETs have approximately 10 times the "on" resistance of N-channel types). But without the voltage standoff and leakage current shunt created by the guard switch, the pinch-off gate voltage for one of the paths would be high enough to generate gate-leakage current in excess of requirement (b).

A description of the Main and Guard Switch action is given overleaf.

6.5.8 MAIN and GUARD SWITCHES (Fig. 6.27)
(Circuit Diagram 430652 Page 11.4-1)

Refer to Fig. 6.27, in which only the Space to Mark (SET) state transfer a-b-c is shown.

The Mark to Space (RESET) transfer is symmetrical c-b-a.

The switch driver flip-flops establish the voltage shown at TP3, 4 and 5 as controlled by the set and reset pulses. The drivers are ECL fast bistables, but note that Q19 and Q20 are included in the main switch driver as a level-shifter for Q32/Q35.

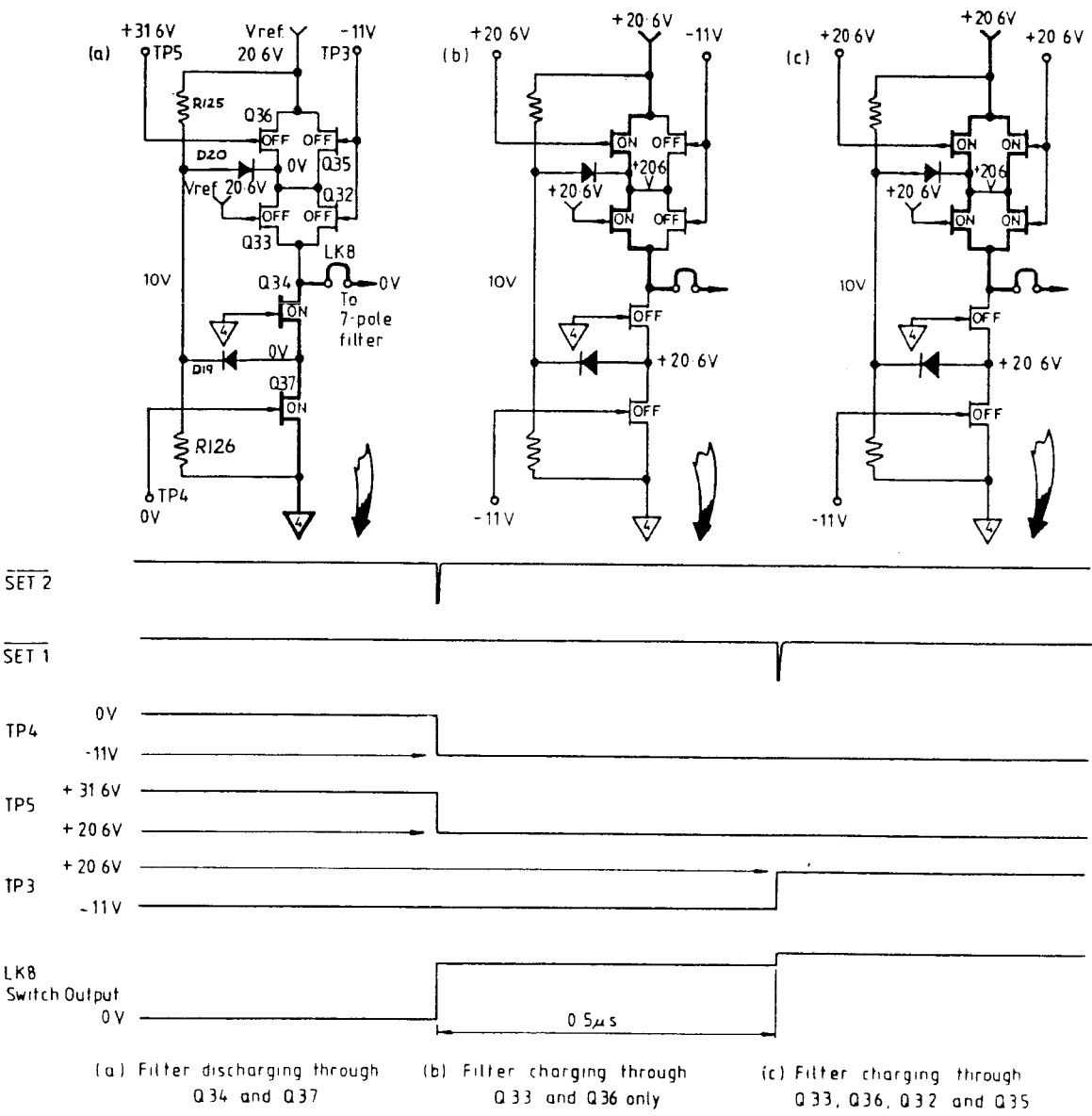


FIG. 6.27 ACTION OF MAIN AND GUARD SWITCHES (MSD)

6.5.8.1 Switch Timing
(Fig. 6.27)

$\overline{\text{SET}} 1$ pulse is delayed by $0.5\mu\text{s}$ after $\overline{\text{SET}} 2$ pulse, and $\overline{\text{RST}} 2$ is delayed by $0.5\mu\text{s}$ after $\overline{\text{RST}} 1$.

$\overline{\text{SET}} 2$ and $\overline{\text{RST}} 2$ pulses control the timing of Q36, Q33, Q34 and Q37 in the main switch (TP4 and TP5).

$\overline{\text{SET}} 1$ and $\overline{\text{RST}} 1$ pulses turn Q35 and Q32 on and off (TP3). Because of the $0.5\mu\text{s}$ delays, Q35 and Q32 conduct only during the time that Q36 and Q33 are also conducting.

6.5.8.2 Filter Discharge Path

In *Fig. 6.27(a)* the switches are in "space" state:

Q37 and Q34 are turned on by TP4 at 0V, to provide the filter discharge path.

Q33 and Q36 are turned off by TP5 at +31.6V,

Q32 and Q35 are turned off by TP3 at -11V.

The filter discharges via resistor R79 and FETs Q34 and Q37. During both Mark and Space periods, R79 (78.7k Ω) is a major determinant of the 7-pole filter charge and discharge currents. Because in 'space' state the 'On' resistances of Q34 and Q37 (3 Ω -5 Ω each) are very small in comparison, the potential at link B can be regarded as zero when considering the effects of the other switching voltages.

Reverse leakage currents in JFET junctions are normally of the order of a few picoamps unless the junction voltages are much in excess of 20V. To control leakage effects from the four JFETs which are turned off, the cathode of diode D20 is connected to the common junction of the four devices. Its anode is returned to the junction of R125 and R126, close to +10V.

The reverse leakage characteristics for a J108 FET (Q35 and Q32) are generally several times heavier than for a J174 (Q36 and Q33). This means that in this switch, the leakage currents via Q35 and Q32 out of the common junction are 4-5 times greater than those entering via Q36 and Q33.

The net leakage out of the junction holds D20 slightly in forward bias, so that its cathode cannot rise above about +10.3V, when the four FETs are turned off in 'space' state. Thus D20 guards the 'buffer' FETs Q33 and Q32 from the effects of the relatively high voltage on Q36 gate. The effects of the buffer FETs' own leakages on the voltage at the filter input can be regarded as negligible, because Q33 leakage currents towards LKB are virtually balanced by those away via Q32.

6.5.8.3 Filter Charge Path

To preserve linearity over the full range of Mark:Period ratios, the filter charging path time constant must closely match that of the discharge path. Q35 and Q32 are factory-selected to form a matched set with Q34 and Q37, all J108 N-channel FETs (the 'on' resistance of P-channel FETs in a true complementary switch would be much higher, of the order of 30 Ω -40 Ω). Nevertheless, to avoid high voltages being developed across Q35/Q32 when changing between states (causing excessive leakage), P-channel FETs are employed. Q36/Q33 are switched on before (and switched off after) Q35/Q32.

Fig. 6.27(b) shows this intermediate state after $\overline{\text{SET 2}}$ and before $\overline{\text{SET 1}}$, and *Fig. 6.27(c)* illustrates the fully-conducting state after $\overline{\text{SET 1}}$. Note that for descriptive purposes, the second step on LKB waveform is heavily exaggerated, and is not readily viewed on an oscilloscope. The slightly longer charging time-constant during this half micro-second, due to the higher resistance of Q36/Q33, is not sufficient to disturb the linearity of the filter in excess of specification.

The voltage between TP4 and LKB during 'mark' state is some 31 volts. In the absence of D19, an adverse voltage distribution could cause excessive reverse leakage in Q37. D19 controls the distribution by limiting the voltage at its cathode to about +10V, constraining Q37 source-gate voltage to a tolerable 20.5V.

6.5.9 7-POLE FILTER

(Circuit Diagram 430652 Page 11.4-1)

M26, M28, M32, Q41 and Q42, together with associated capacitors and resistors, form a 7-pole Bessel filter in three active elements; providing approximately 135dB of attenuation at the 125Hz switching frequency and increasing at a rate of 140dB/decade. This allows sufficient bandwidth to avoid excessive settling time while reducing the output ripple to within instrument specification. Q41 and Q42 source-followers provide input bias currents for M26 and M28 from the 15V supplies, and buffer the line from bias-current effects. M32 bias-current effects are insignificant.

The '+Ve SUMMING AMP' filter output DC voltage (TP13), is fed to a buffer amplifier for subsequent summing with the output from the Least-Significant Switch offset-bias amplifier. R101 and C51 prevent any spike remnants from the chopper-stabilized buffer amplifier being fed back into the filter.

6.5.10 SUMMING AMPLIFIER (Circuit Diagram 430652 Page 11.4-3)

6.5.10.1 '+VE SUMMING AMP' Buffer

M33, M34 and Q44 buffer the '+Ve SUMMING AMP' voltage output from the 7-pole filter (this is proportional to the Mark/Period ratio of the 13 most-significant bits of the binary word which defines the instrument output value demand).

M33 is a high-gain, chopper-stabilized integrator with a bandwidth of approximately 10Hz, and Q44 provides additional bandwidth for rejection of HF common-mode noise.

M35, D14, D15, Q48 and Q49 generate boot-strapped supplies to preserve full dynamic-range linearity. Q46 and Q47 establish 3mA constant-current drives for D14 and D15.

The whole amplifier acts as a voltage-follower, M34/Q45 providing the output drive, buffering the output of M33 and Q44. The output 'Hi O/P' is delivered to the DC assembly via RL2 for positive DC outputs, or via RL1 if the output is to be negative. For AC outputs, it is always delivered to the AC assembly via RL2 (RL1 being permanently de-energized for AC ranges). The output is sensed either in the DC or AC assembly to account for the volts-drops in the connecting circuit. The sense feedback voltage 'Hi SENSE' is applied to the inverting input of the whole buffer via R98.

For a zero count in the MSB comparator, the filter output voltage is approximately +3.2mV, and a full count of 8191 would produce +20.6V. These are the voltages which are developed at the buffer output.

6.5.10.2 '-VE SUMMING AMP' Buffer

M38, M39 and Q51 buffer the '-Ve SUMMING AMP' voltage output from the Offset Bias Amplifier derived from the 3-pole filter (this is proportional to the Mark/Period ratio of the 12 least-significant bits of the binary word which defines the instrument output value demand).

The dynamic range of the filter output voltage was originally defined by the Reference Buffer (8.83V) for efficient operation of the FET switching circuitry.

It was scaled in the Offset Bias Amplifier to give +27.5V for an LSB comparator count of zero (from approx. +1.1mV at TP6), and +24.5V for a full count of 4095 (from +8.83V at TP6). It now needs to be scaled down so that it has correct proportionality to the '+Ve SUMMING AMP' dynamic range.

R99 and R100 attenuate the '-Ve SUMMING AMP' input voltage by a factor of 0.8545×10^{-3} . At zero count, +27.5V is reduced to +23.5mV, and at full count +24.5V reduces to +20.9mV. These are the extremes of voltage developed at the buffer output.

The whole amplifier acts as a voltage-follower, but without bootstrapped supplies (the small input voltage dynamic range of approx. 2.5mV does not warrant it). Otherwise the circuit is identical to the '+Ve SUMMING AMP'. M39/Q52 provide the output drive, buffering the output of M38 and Q51.

The output 'Lo O/P' is delivered to the DC assembly via RL2 for positive DC outputs, or via RL1 if the output is to be negative. For AC outputs, it is always delivered to the AC assembly via RL2 (RL1 being permanently de-energized for AC ranges).

The feedback voltage, sensed in the DC or AC assembly, is returned via the appropriate relay, and applied to the inverting input of the whole buffer via R127.

6.5.10.3 Summing

On the DC or AC assembly, the outputs from the two buffers are summed by defining the 'Lo O/P' level as 'Reference Common' (Common-1 for DC, Common-2C for AC), and the 'Hi O/P' level as 'REF+Ve'. Thus at any instant, the voltage developed as 'REF+Ve' with respect to 'Reference Common' will always be 'Hi O/P' minus 'Lo O/P', at their current values.

The reference voltages and reference division circuitry are chosen to allow for software calibration adjustments, so the summing span overlaps the possible required span of 0V to 19.999999V at both extremes:

With an overall 25-bit count of zero in the comparators, REF+Ve is +3.2mV minus +23.5mV, a negative overlap of 20.3mV.

At overall full count, REF+Ve is +20.6V minus +20.9mV, approximately +20.58V.

6.5.10.4 Bipolar Reference Switching

Relays RL1 and RL2 are used in DC ranges for polarity reversal. However, this is not necessary for AC operation, for which RL1 is un-energized, and RL2 is energized, outputs from the summing buffers being fed to the AC assembly via RL2.

6.5.10.5 DC and AC References

For DC operation, the summed DC reference is applied to the Error Amplifier directly (*refer to page 11.5-1*), but for AC operation, the DC reference is applied to a voltage divider which is used to provide a 'Quasi-sinewave' AC reference signal.

The generation of this signal is described in *Section 6.6*.

6.6 AC REFERENCE - THE QUASI-SINEWAVE

6.6.1 AC-to-AC SENSE/REF COMPARISON

In the Sense/Reference comparator, a considerable advantage is gained by comparing AC with AC. (If AC sense were compared with DC reference, small DC offsets would be magnified, leading to 'DC turnover' errors). The AC waveform used as reference is constructed in ten steps by a digitally controlled switching network, based on the DC reference as its peak value. It has been given the name 'Quasi-Sinewave'.

To drive the VCA, the comparator produces a DC error signal which is proportional to the difference in 'Mean Square' values, and is driven to zero by the action of the Output-Sense loop. At zero error the RMS value of the comparator's sense input has thus been adjusted by the loop to be equal to the RMS value of its reference input.

On the 1V Range there is neither amplification nor attenuation in the Output-Sense loop. The quasi-sinewave is designed so that with the 1V Range selected, its RMS value is equal to the voltage demanded on the front panel OUTPUT display, (with small, controlled adjustments for calibration).

On higher ranges, decades of amplification are switched in to set the output to the demanded voltage. Switched decades of attenuation reduce the sensed sinewave back to the 1V-Range level for comparison with the quasi-sinewave.

For millivolt ranges, the instrument output terminals are not within the output/sense loop. Instead, the AC 1V output from the 1V buffer is sensed internally and applied to the comparator to complete the loop. The AC 1V signal is reduced to the selected millivolt range levels at the terminals by precise, passive, decade attenuators.

On current ranges, the current reference is derived from either the closed 1V or 10V Range Output/Sense loop.

Therefore on all ranges the Output/Sense loop gain is driven to a magnitude of 1, so that the VCA and the comparator both operate at 1V Range levels.

6.6.2 DC REFERENCE - SCALING for AC

The Reference Divider hardware is common to both DC and AC outputs. On DC ranges, the basic voltage range is the 10V Range, with 100% overrange at Full Scale. In these cases the full span of reference values is employed, generating the resolution necessary to accommodate the DC accuracy available.

The same analog accuracy is not available for AC, so the high resolution is not necessary. Moreover, the linearity of the analog circuitry is improved by using a smaller dynamic range in the reference circuits. So for AC outputs the 1V Range is the basic range, and the software scales its demanded value accordingly.

The sensed output is compared against the quasi-sinewave, whose characteristics match those of the sensed sinewave. To construct the quasi-sinewave, the DC reference voltage needs to be set as its peak value.

The software imposes the scaling factors which establish the reference voltage at the peak value of the quasi-sinewave. Thus the full span of the 25-bit comparator, and hence the possible dynamic range of the DC reference, are realized only on DC ranges and at times when the Reference Divider itself is being calibrated.

Before initial calibration, the maximum obtainable reference voltage for AC is slightly greater than 2.8V, and the minimum is slightly less than 125mV. This overlaps the peak voltages of the quasi-sinewaves corresponding to the maximum and minimum values of sensed output; giving a margin for accurate calibration from digital gain factors held in the non-volatile calibration memory.

6.6.3 DC REFERENCE - VOLTAGE VALUES for AC

As mentioned earlier, the DC Reference is used to establish the amplitude of the quasi-sinewave. When the 1V AC Range is selected, the reference is set to the peak value of the quasi-sinewave, which is 1.397 times the demanded RMS (sinewave) voltage output of the instrument. In normal use, therefore, the reference voltage is adjusted by front panel OUTPUT display selections; between 125.7mV (for 0.9V selection) and 2.79V (for 1.999999V selection), plus or minus any user-calibration corrections.

On higher and lower AC ranges, analog range switching in the sense amplifiers scales the sense voltages for comparison with the same RMS voltage span of quasi-sinewaves.

6.6.4 REFERENCE INVERTER (Circuit Diagram 430844 page 11.7-2)

The quasi-sinewave is derived by a specific form of D-A converter, selecting voltages from a divider network. Because negative values are required, the divider is strung between positive and negative reference voltages. The unity-gain Reference Inverter generates the negative reference 'REF-Ve' by inverting 'REF+Ve'.

M1, M2 and Q1 perform the inversion. M2 generates the bandwidth necessary for amplitude switching operations, while chopper-stabilized integrator M1 removes DC offsets, always referring the inverter output to Common-2C. To compensate for RMS value changes in the quasi-sinewave (due to switching errors arising from frequency changes), feedback from the quasi-sinewave is applied via R1, C4, R4 and C5. Q1 provides the output drive to the quasi-sinewave generator.

6.6.5 QUASI-SINEWAVE GENERATOR (Circuit Diagram 430844 page 11.7-3)

The SYNC \emptyset input to M11-15 RESET, if set to Logic-1, would disable the Quasi-sinewave sequence counter M11. The facility is not required in this application so J7-49 is unconnected on the Mother assembly (page 11.16-2). M11-15 is thus pulled down to logic- \emptyset by R40 to enable the quasi-sinewave for both AC Voltage and AC Current functions.

The quasi-sinewave is generated at a frequency determined by the Frequency Synthesizer 100Hz-4kHz output (para 8.1.3.3 describes the synthesis), clocking the decade counter M11 via J7-50. This continuously recycles M11 in ascending count through Q₀ to Q₉, ten clocks constituting one cycle of the quasi-sinewave, so the quasi-sinewave runs at a frequency of between 10Hz and 400Hz. The carry C_{out} of M11 returns to the Synthesizer via J7-51 to be selected as the reference frequency for the 100Hz (10-330Hz) frequency range.

With increase of frequency range, the difference between the frequencies of output and quasi-sinewave increases in decade steps. As the comparison of sense and quasi-sinewave signals is performed at mean-square DC levels, this difference theoretically does not matter, so long as the signal is at an exact multiple of the quasi-sinewave frequency. However, to achieve optimum operation of the Sense/Reference comparator, each zero crossing of the quasi-sinewave is synchronized to coincide with a sense-signal zero crossing.

Synchronization is achieved by the clock input to M9, which controls the timing of the quasi-sinewave switches M8 and M14. Using the same clocks, M11 and M10 transit times prevent the data from arriving at M9 'D' inputs until the data already established there by the previous clock pulse has been latched at its outputs. Thus data ripples through M11 and M9 at successive clock pulses.

The ripple delays the data by one clock period and would, if left uncorrected, put the switching out of sequence. The arrangement of the connections between M11 outputs and M9 data inputs, combines appropriate outputs so as to correct the switching pattern. The table in Fig. 6.28 demonstrates the rotation of 1 clock period; the quasi-sinewave steps being labelled at M9 inputs and outputs.

The quasi-sinewave is output to the transfer switching input to the Sig/Ref comparator at M16-1. The action of the transfer switch is described in Section 9.5.

A second output is filtered and fed back as compensation to the Reference Inverter as described earlier (para 6.6.4).

| Step | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 |
|---|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| M11 Output at Logic-1: | Q ₉ | Q ₀ | Q ₁ | Q ₂ | Q ₃ | Q ₄ | Q ₅ | Q ₆ | Q ₇ | Q ₈ |
| M10 Output pin at Logic-1: | 4 | 11 | - | 11 | 4 | 10 | 3 | - | 3 | 10 |
| M9 Output pin at Logic-1: | O ₁ | O ₄ | O ₅ | O ₄ | O ₁ | O ₂ | O ₀ | O ₃ | O ₀ | O ₂ |
| Switch Energized M8 pin: M14 pin: | 5 - | 6 - | 13 - | 6 - | 5 - | - 5 | - 6 | - 13 | - 6 | - 5 |
| Step Voltage fed to M16-1: | +0.42 | +1.16 | +1.397 | +1.16 | +0.42 | -0.42 | -1.16 | -1.397 | -1.16 | -0.42 |

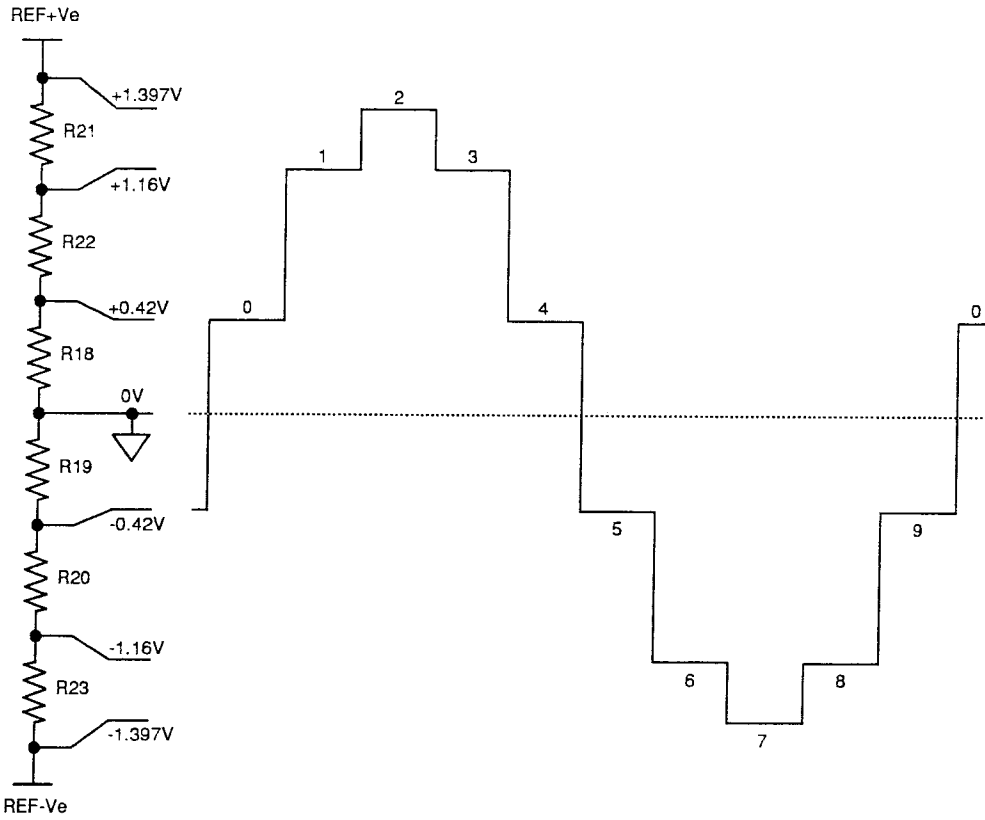


FIG. 6.28 QUASI-SINEWAVE GENERATION

6.7 POWER SUPPLIES

The circuits described in this section perform the following functions:

- Line power switching, fusing, filtering, voltage selection and transformation.
- Main digital supply generation and distribution (Out-guard).
- Display high voltage supply generation.
- In-guard stabilized supply generation for Common-2 and Common-4 circuitry.

A simplified power-distribution block diagram appears at *Fig. 6.29*.

The power input module is mounted on the rear panel. The mains (line) transformer is located in the rear section of the instrument, close to the In-guard and Out-guard Power Supply assemblies.

(For details of location and attachment, refer to *Section 3*; and *Section 11*, page 11.0-1).

6.7.1 LINE POWER DISTRIBUTION (*Fig.6.29*) (Circuit Diagram 430830 Page 11.17-2)

The single phase line supply enters via a 3-pole input cable at the rear of the instrument. The cable connector plugs into a power input module which contains a fuse, filter and line voltage selector pcb. (For details of fuse values and operating voltage selection refer to the *User's handbook*, Section 2).

Both 'line' and 'neutral' rails are filtered by a low-pass LC network before being fed through the instrument to the two-pole 'Power' switch on the front panel.

The switched supply is fed back into the power input module, to the voltage selector pcb, which configures the line transformer primary circuit as determined by the user. Power for the air circulation fan is provided directly from the power input module.

All line transformer secondaries are electrostatically decoupled from the primaries by a ground screen between the windings. The secondaries which supply the Common-2 and Common-4 in-guard circuits are decoupled by an additional screen which is connected to the instrument guard.

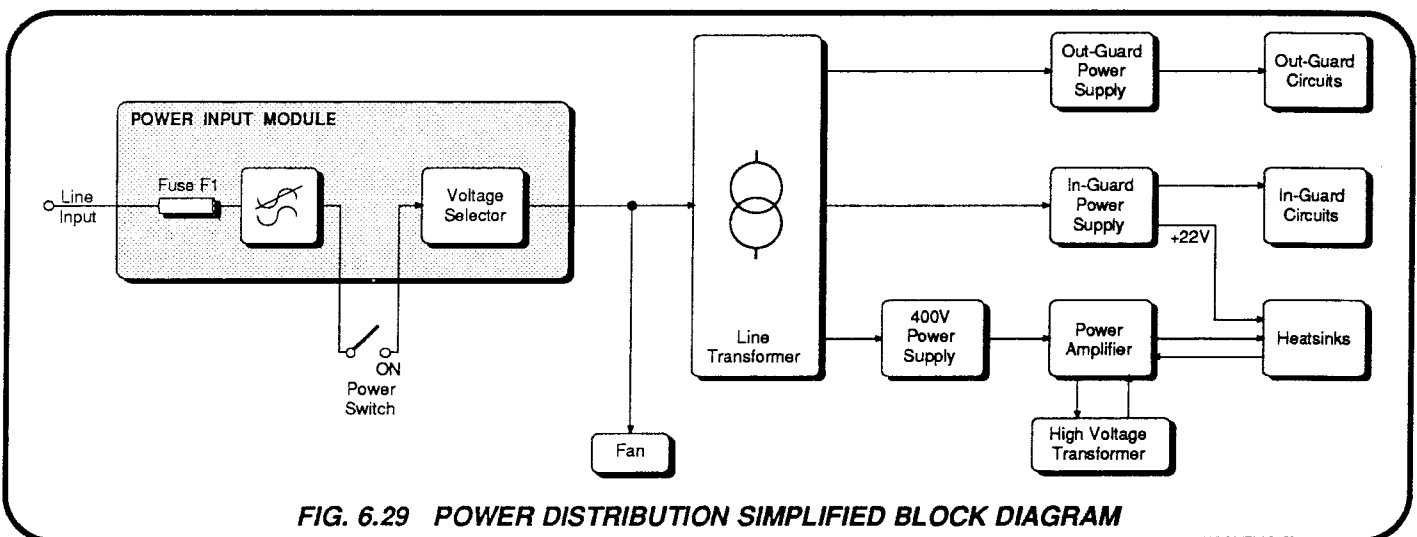


FIG. 6.29 POWER DISTRIBUTION SIMPLIFIED BLOCK DIAGRAM

6.7.2 OUT-GUARD POWER SUPPLIES

(Circuit Diagram 430561 Page 11.10-1)

6.7.2.1 Digital Main Supply

This circuit provides:

- **+8V unregulated** supply for the Front and Digital assemblies.
- **+5V regulated** supply for out-guard digital circuits.

6.7.2.2 +8V Unregulated Supply

This is taken directly from full-wave rectifier D1, D2 via fuse F1 (rated at 4A).

6.7.2.3 +5V Regulated Supply

The output voltage is controlled by series regulator Q5, Q6. Load current is sensed by R1 in the base-emitter circuit of Q1, which increases the conduction of Q5 and Q6 parallel combination for increases of load current. The 2.45V zener D4 provides the reference voltage for comparator M1 at M1-3. The output voltage is sensed between the +5V and DIG COMMON rails on the Mother assembly, and divided down to reference potential at M1-2. R8 and R9 ensure that regulation persists even if the sense links are disconnected.

M1 output drives Q2 whose collector voltage controls Q5 and Q6 conduction. If the +5V rail voltage falls due to loading, Q2 collector voltage rises, increasing Q5 and Q6 conduction to restore the rail voltage. Zener D5 prevents the positive excursion of the +5V rail in the event of regulation breakdown. Zener D3 restricts positive excursions of Q2 base voltage, and hence the drive to Q5 and Q6, to provide current limiting. C9 and C10 give a controlled fast response to reduce the effects of transients on the +5V rail.

PTC thermistor R7 protects the power supply from high ground-leakage currents, notably in the external circuits of the IEEE 488 bus system. R7 presents a minimum of 80Ω between the digital common line and ground; this resistance increasing with increasing ground-leakage current.

A supplementary +5V supply is fed out to the Front assembly from J4-21. This is available to power the LEDs in the front panel keys, but is not used in this instrument, as a regulator on the Front assembly produces the required +5V supply from the unregulated +8V supply (*para 6.7.2.2*).

6.7.2.4 180V Display Supply

180 Volts are required to operate the digital plasma displays on the Front assembly. Because the display anode drivers are powered from the Digital Main Supply +5V rail, the 180V positive pole is referred to this rail in the power supply. The negative pole is therefore at a potential of -175V. Refer to *Section 6.3* for further details.

Series regulation is provided by D6, R16 and Q3; and shunt regulation by D7 and Q4.

6.7.2.5 Common Mode Null

This circuit provides a line-hum cancelling (bucking) output to the instrument guard network. For adjustments refer to *Section 4.9*.

6.7.3 IN-GUARD POWER SUPPLIES

(Circuit Diagram 430554 Pages 11.11-1/2)

6.7.3.1 In-Guard Common-2 Supplies

The general 15V supply for the analog circuitry is provided by three integrated-circuit regulators (*page 11.11-1*) as follows:

- **+15V from M2.**
Because of the high current taken from this supply, the regulator power dissipation is shared. The rectifier output is first regulated to +18.5V by Q1, Q3 and D9; and then to +15V by M2.
- **-15V from M1.**
This is a mirror image of the positive supply.
- **-10V from M6,**
derived from the -15V supply.

The supply is protected by 3.15A fuses F3 and F4 at the bridge rectifier output. Chokes L4 and L5 attenuate HF transients on the AC input.

The 8V supply for the Sine-Source assembly is provided by two integrated-circuit regulators M8 and M9 (*page 11.11-2*). The supply is protected by 1A fuses F5 and F6 at the bridge rectifier output. Chokes L7 and L9 attenuate HF transients on the AC input.

6.7.3.2 ±22V PS/I Heatsink Supply

This provides +22V and -22V unregulated power outputs to the PS/I Heatsink assembly. Both supplies are protected at 4A by fuses F1 and F2, the AC input being HF-filtered by chokes L2 and L3. The 22V common return is maintained close to the common-2 return potential by resistor R1.

6.7.3.3 Reference Divider Common-4 Supplies

(Circuit Diagram 430554 Pages 11.11-2)

This circuit provides +36V, +15V and -15V regulated outputs to the Reference Divider in-guard circuits. The +36V supply is also used to power the +20V Master DC Reference.

Two secondary windings of the line transformer are used, and inter-supply transients are reduced by the special coupling arrangements of common-mode choke L10. The rectified output from bridge W4 is series-regulated by M3 to produce the +36V supply. R2/R3 sense the output voltage.

D11 and M4 reduce the +36V to generate the +15V regulated supply.

The -15V supply is provided by bridge W3 and regulator M7.

6.7.3.4 38V Common-2 Supply (Circuit Diagrams 430653 Page 11.12-1 and 430604 Page 11.16-5)

The 38V regulated supply is used for two purposes:

- to power the 10V Amplifier in the Power Amplifier assembly;
- to provide a lower positive source voltage to reduce dissipation on the Power Amplifier assembly, when negative voltages are being output on the 100V DC Range (refer to *sub-section 7.8.3.4*).

It is plugged into the Mother assembly in the rear compartment next to the Heatsinks.

The mains (line) transformer 40VRMS secondary centre tap is referred to Common-2 on the Mother assembly. It provides a variable AC output by R25 on the Mother assembly to balance line-induced voltages on the guard screens. The 40V is rectified, filtered and smoothed on the Mother assembly before being passed to the regulator at approx. 50VDC.

On the 38V Power Supply assembly the output voltage is controlled by series regulators Q2 and Q1. As the regulator is symmetrical, only the positive side is described.

The output voltage is divided by R26 and R25 to provide a sense signal for comparator M1, which is powered by a local shunt regulator D8/R16/C8. The 2.45V reference for the comparator is derived by D6/R23 from the comparator supply.

M1 output drives Q8 whose collector voltage controls Q6 and hence Q2 conduction. If the +38V rail voltage falls due to loading, Q8 collector voltage rises, increasing Q5 and Q6 conduction to restore the rail voltage.

Load current is sensed by R24 in the base-emitter circuit of Q5, which is normally cut off unless the load current exceeds 170mA. At this point Q5 conducts and pulls down the base of Q6, setting a hard current limit.

Zener diode D2 turns Q5 hard on in the event of an output short circuit, providing a rapid reponse to catastrophic failure in the power amplifier circuitry. As the output voltage falls below +22V, D2 arrests the fall on Q5 base, switching Q5 hard on and turning Q6 and Q2 off. This leaves D2, R8 and R9 controlling the output current, which falls to less than 500 μ A.

When the load is removed, the conduction of Q5 via R26/R25 is insufficient to hold Q6 cut off, especially as Q8 is also cut off by the comparator. So Q2 is allowed to conduct, the output voltage rises until first D2, and then Q5, cut off and the output voltage is restored to comparator control.

The 38V output is taken through wired-in fuses F1 and F2. These merely protect the PCB tracking in the event of an output short-circuit. The output voltages are protected from reverse polarity by D1 and D2 on the Mother assembly.

6.7.3.5 38V Supply Failure (Circuit Diagram 430618 Page 11.9-4)

The 38V output voltage is monitored in the Power Amplifier assembly. The monitor is described in *Section 7, para 7.8.6.3*.

6.7.3.6 400V Common-2 Supply

This is described in *Section 7, paras 7.8.5 and 7.8.6.4*.

SECTION 7

DC VOLTAGE OUTPUTS - AMPLITUDE CONTROL SYSTEM

7.1 INTRODUCTION

7.1.1 GENERAL PROCESS

When DC Voltage Function is selected, a relay (RL2) on the Reference Divider assembly feeds the output of the summing amplifier into the DC assembly as DC Ref (Hi and Lo), the value of which represents the demanded output voltage and polarity.

The DC Voltage circuitry selects the required range, from switching data transmitted into guard via the Serial Data Link. The appropriate range circuit generates the demanded voltage at the output terminals. Output switching and protection are provided.

7.1.2 DC VOLTAGE SYSTEM BLOCK DIAGRAM

The DC Voltage Amplitude Control System is briefly described in *Section 5*, and illustrated in the Block diagram of *Fig. 5.3*.

DC Voltage Ranges up to 100V are described in *Section 5.6*, and the DC 1000V Range in *Section 5.8.1*; at block diagram level.

7.1.3 CIRCUIT OPERATION

The circuits described in this section perform the following functions:

- Buffer the DC Ref voltage (-20V to +20V) and provide output voltages to the instrument terminals, on the 10V DC Range.

- Amplify the DC Ref voltage providing output voltages:

-200V to +200V on 100V Range
-1100V to +1100V on 1000V Range

- Attenuate the DC Ref voltage and provide output voltages between -2V and +2V on the 1V DC Range.

- Further attenuate the 1V Range voltages and provide output voltages:

-200mV to +200mV on 100mV Range
-20mV to +20mV on 10mV Range
-2mV to +2mV on 1mV Range
-200µV to +200µV on 100µV Range.

- On the 10V Range, sense the output voltage (at the load in Remote Sense), making continuous, direct comparisons in a closed negative-feedback loop with the DC Ref voltage input from the Precision Divider. The comparison generates an 'error' voltage which corrects the output voltage.

- On the 1V Range, sense the output voltage at 1V Range levels, comparing the sensed voltage with the attenuated DC Ref input, and correcting the output as on the 10V Range.

- On the sub-volt ranges; sense the 1V Buffer output at 1V Range levels, correcting its output as on the 1V Range.

- On the 100V Range, sense the output voltage at 100V levels, and reduce the sensed voltage to 10V levels. Compare the attenuated voltage with the DC Ref input from the Reference Divider and correct the output voltage as on the 10V Range.

- On the 1000V Range, provide a VCA drive from the Error Amplifier, to a DC Modulator for the high voltage amplification circuits. Attenuate the sensed output voltage, comparing the attenuated voltage with the DC Ref input at 10V Range levels, and correcting the output as on the 10V Range.

- Provide switching of DC Voltage Output, Range, Guard and Sense, under the control of signals from the Analog Control Interface.

- Sense excess currents in the output circuit, providing a $\overline{\text{LIM ST}}$ status signal to the CPU via the Analog Control Interface.

- Sense High Voltage State (at approx. >130V) on the PHI (I+) output line, providing a $\overline{\text{HV ST}}$ signal to the CPU via the Analog Control Interface.

Many of the circuits described in this section are located on the DC PCB assembly. The major exceptions are as follows:

| | |
|-----------------------------|---|
| 10V Range Buffer stage | - Power Amplifier assembly, |
| 100V Amplifier | - Power Amplifier assembly and Heatsink assemblies, |
| 1000V Range output circuits | - LF and HF transformer assemblies and the High Voltage assembly, |
| Function Switching | - Current/Ohms assembly, |
| Output Filtering | - Terminal Board assembly. |

7.2 LOW VOLTAGE LOOPS (Fig. 7.1)

Although the 10V range is regarded as the basic DC range of the instrument, this is because the full 20V Reference is used, and suffers no overall voltage attenuation nor amplification in its output loop. However, it does require power amplification at dissipations which preclude its positioning within the thermal shield, so its output buffer is located on the Power Amplifier assembly. This factor complicates the routing of its signals.

The 1V range loop is more direct; its buffer is located on the DC assembly, and there are fewer circuit elements to describe in its path. For reasons of simplicity, therefore, the 1V range is chosen for this description of the basic DC output loop.

The descriptions in Section 7.2.1 and Section 7.3 concentrate on the signal path of the 1V Range loop; from the polarity switch in the Precision Divider, out to the 'Power' terminals, and back to the 'Sense' input of the Error Amplifier.

For descriptions of the alterations to the 1V loop to accommodate the other DC voltage ranges, refer to the following sub-sections:

| | |
|----------------------------|-----|
| 100mV Range | 7.4 |
| 100 μ V to 10mV Ranges | 7.5 |
| 10V Range | 7.6 |
| 100V Range | 7.8 |
| 1kV Range | 7.9 |

On the circuit diagrams in Section 11, all relay contacts are shown with their relays in the unactivated condition.

7.2.1 1V RANGE SUMMARY

The low voltage loop and routing are illustrated in the simplified diagram of Fig. 7.1. Switching contacts are shown in positions set for the 1V Range.

DC Ref is variable between -20V and +20V referred to common-1, and the 1V attenuator provides voltages between -2V and +2V. The Error Amplifier and 1V Buffer are connected to form a voltage-follower when I+ is connected to Hi (in either local or remote sense).

The output from the 1V Buffer is connected directly to the I+ terminal via power switching, the sense feedback returning from the Hi terminal, via sense switching, to the Error Amplifier inverting input. The sensed output voltage is adjusted by the feedback until it equals the attenuated DC Ref Value, i.e. for zero differential input to the Error Amplifier.

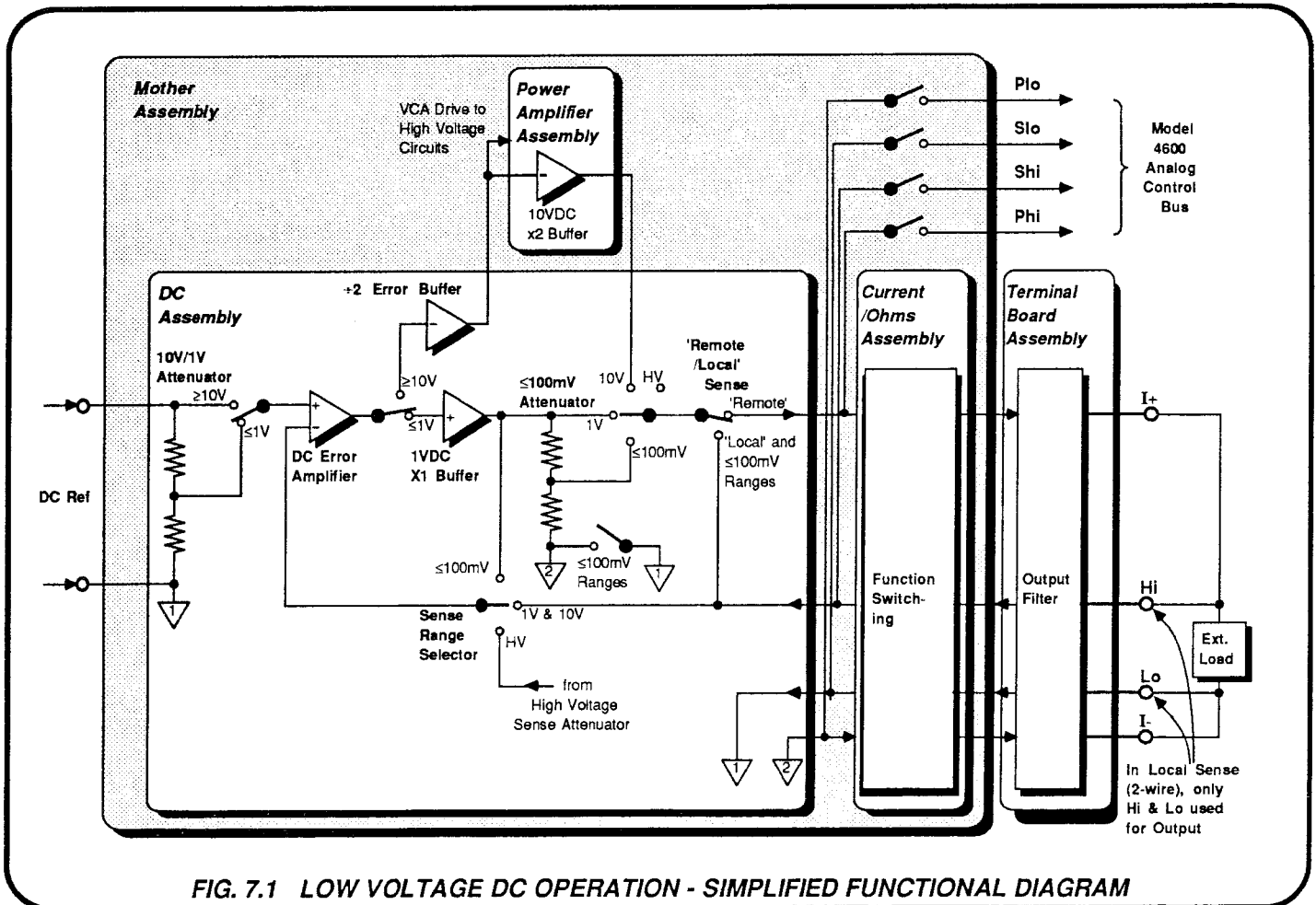


FIG. 7.1 LOW VOLTAGE DC OPERATION - SIMPLIFIED FUNCTIONAL DIAGRAM

7.3 DC 1V LOOP

7.3.1 REFERENCE DIVIDER ASSEMBLY

(Circuit diagram 430652 Page 11.4-3)

For positive outputs, the positive DC Reference PHI(REF), PLO(REF), SHI(REF) and SLO(REF) pass via energized relay RL2, to be output as a 4-wire sensed connection into the DC assembly. The four lines are routed out at J4 pins 9, 10, 11 and 12 into the Mother assembly. For negative outputs, energized relay RL1 configures the lines to give a negative DC reference.

7.3.2 DC ASSEMBLY

(Circuit diagram 430536 Page 11.5-1)

The DC Reference enters at J5 pins 1, 2, 3 and 4. On DC Voltage ranges, RL18 connects the power and sense lines to the two star-points TP2 and TP3. TP3 is the signal Common-1 point, to which all instrument DC voltage sense inputs are referred.

For the 1V and lower ranges, RL16-5/4 connects the output of the 1V attenuator to the non-inverting input of the Error Amplifier. (On the 10V and higher ranges, RL16-8/9 connects the full DC Reference to the Error Amplifier.)

7.3.3 ERROR AMPLIFIER

The DC Ref Voltage from the Reference Divider is applied to two amplifiers: M21 is a high-gain chopper-stabilized integrator of approximately 10Hz bandwidth, Q5 provides additional bandwidth for rejection of HF common-mode noise. M20 provides additional gain and output drive, through a transient-suppressing diode clamp circuit.

The whole amplifier is bootstrapped by M22, D48, D49, Q6, Q7 and Q10. Q8/Q9 provide 1.4mA constant-current drives for D48/D49 over the range of BS-Common variation (-20V to +20V on the 10V and higher ranges). Power for the bootstrapped amplifier is obtained originally from the $\pm 38V$ supply; used also to power the 10V Buffer in the PA assembly, referred to Common-2.

Extensive screening and filtering is used to eliminate the effects of the chopping spikes at inputs and output of M21.

7.3.4 1V BUFFER

On the 1V and lower ranges the error amplifier output is applied to the 1V Buffer, via the closed contacts 10/11 of energized relay RL16. A current amplifier M23 is chosen, as the buffer has to drive the external load directly via the output switching, output lines and external leads.

It also drives the 100mV Attenuator on the 100 μ V - 100mV ranges.

M23 is powered by a separate individually-filtered 8V supply (*refer to pages 11.5-4 and 11.11-2*). Its input and output are protected by back-to-back zener diodes.

The output from the 1V buffer is connected, via contacts 12/7 of energized relay RL3, to the '1V+10V+100V' PHI(DCV) star point.

7.3.5 RANGE SWITCHING

On the 1V and 10V ranges the 1V+10V+100V star point is decoupled to Common-2A by C28 via contacts 2/3 of energized relay RL4.

Relay RL5 is energized on the 1V and 10V ranges; and after passing through the back-to-back contacts RL5-8/9, which cancel their own thermal EMFs, the DC1V+10V+100V signal is renamed PHI(DCV).

7.3.6 OUTPUT SWITCHING

(Circuit Diagram 430536 Page 11.5-2)

The PHI(DCV) output and other connections from the Range relays (*Page 11.5-1*) are passed to the instrument output terminals via several relay contacts which provide switching for Remote or Local Sense, Remote or Local Guard, and Output On/Off.

The output does not travel directly to the terminals from the DC assembly, as further switching is required. If Option 30 is fitted, function changes switch the terminal lines on the Current/Ohms assembly. When Option 30 is not fitted, a Current/Ohms Link PCB (Part No. 410288) is fitted in place of the Current/Ohms assembly. This PCB provides direct connections for the signals, on their route to the instrument terminals (*para 7.3.8.1*).

7.3.6.1 DCV/ACV Switching

For DC voltage ranges, relays RL10 and RL11 are energized. The PHI(DCV) line from the range relays passes via RL10 contacts, TP8, 1A fuse F6, and RL15 contacts (if output is set ON); to the PHI(V) line at J5-19. For DC voltage outputs, the four ACV lines at J5-25/26/29/30 are disconnected by relays in the AC assembly.

In Remote Sense, the power return line PLO(DCV) is linked via RL11 contacts, 1A fuses F4 and F3, relay RL14 and RL15 contacts to J5-23 as PLO(V). PLO(DCV) is held close to Common-2A by R56/C30 (*page 11.5-1*), being protected against excessive departure from Common-2A potential by the back-to-back 3V zeners D13 and D25. The voltage developed across R56 by the output current is monitored by comparator M13 (*page 11.5-2*).

7.3.6.2 Output On/Off.

Because the DCV and ACV lines are separately switched, a single independent 4-pole relay RL15 can be used to set output on and off. Thus the lines at J5-19/20/23/24 carry either DCV or ACV signals to and from the output terminals. Where ACV and DCV join, the power lines change their names to PHI(V) and PLO(V).

7.3.6.3 Remote Sense Switching.

When Remote Sense is not selected, two-wire outputs to external loads can only be connected from the Hi and Lo terminals (a relay on the Mother assembly disconnects the I+ terminal). Relay contacts RL14-9/8 connect PHI(DCV) to SHI(DCV), and RL14-3/2 connect PLO(DCV) to SLO(DCV). Relay contact RL14-5/4 is open, severing the connection to the I- terminal.

In Remote Sense relay RL14 is energized, removing the connections between the power and sense lines, and RL14-5/4 reinstates the link from PLO(DCV) to the I- terminal. This gives full 4-wire sensing at the external load.

7.3.6.4 Remote Guard Switching

The front panel 'Guard' terminals are permanently connected to the internal guard shields via J5-15/16 and J5-11/12. With 'Remote Guard' selected, the direct connection between Guard and Lo is severed by the open contact of energized relay RL17. R121 damps any high frequency resonance in the combined internal and external guard circuits; C62 reducing HF noise on the millivolt ranges. With Remote Guard off, RL17 connects the guards to PLO(V) via PTC thermistor R97, which also assists in reducing millivolt noise.

7.3.7 OUTPUT PROTECTION

Two circuits are described in the following paragraphs:

- The DC Overcurrent Detector, which senses the current flowing in the PLO(DCV) return line, sending a signal to the status-reporting logic if the DC current exceeds approx. 28.5mA. On the 100V and 1kV DC ranges the 'LIM DET' signal is sent, but on the 10V DC and lower ranges the 'LIM ST' signal is made active.
- The Overvoltage Detector provides an indication to the CPU that the output voltage is in 'High Voltage State', ie. the 'HV ST' signal is activated if the output DC or peak AC voltage is greater than 110V. If the instrument has not been programmed into High Voltage State, then an anomaly exists, and remedial action is taken by the CPU.

The results of activating the overcurrent detector are described later in *sub-section 7.12.7*.

7.3.7.1 DC Overcurrent Detection

On DC voltage ranges of 1V and higher, the current taken by the instrument load develops a voltage across resistor R56 (*page 115-1*), which is applied to the resistor chain R31/R30/R36 (*page 115-2*). On 100mV and lower ranges R56 is shorted out by relays RL2-5/4 (*page 115-1*), RL11-2/5 & 11/8 and RL14-2/3 (*page 115-2*).

M13 is an open-collector comparator wired to detect excessive voltages across R30/R36 (R31 is the common bias resistor). Diodes D17 and D18 set the reference potential at M13-3 (for positive outputs) to approx. +285mV; and at M13-6 (negative outputs) to approx. -285mV. Under normal operation, when the output current is less than 25mA, both halves of M13 are held in open-collector. When the output current through R56 exceeds approximately 28.5mA, the voltage across it exceeds 285mV and one of the halves of M13 switches its output to the negative rail (analog logic-Ø). Diode D52 conducts, pulling M10-6 and M10-9 to logic-Ø:

LIM DET Activation:

On the 10V and lower DC ranges, M10-5 is permanently held at logic-1 disabling M10-6, so the overcurrent signal has no effect

on M10-4, which is held at logic-1 and D3 remains in reverse bias. The LIM DET signal is not activated.

On the 100VDC or 1kVDC range, M10-6 is enabled by M10-5 at logic-Ø, so the overcurrent signal sets M10-4 to logic-Ø and LIM DET is activated at logic-1.

LIM ST Activation:

In this case the effect of the 100VDC and 1kVDC signals is reversed, and M10-9 is sensitized to the DC overcurrent signal only on the 10V and 1V ranges, when M10-8 is at logic-Ø. For excessive DC output currents, M10-10 sets D9 cathode to logic-Ø pulling the LIM ST line to its logic-Ø active state.

The AC 1kV Overcurrent Detector receives no input on DC ranges, as no current passes through the sensing resistors R107 and R108.

7.3.7.2 High Voltage Status Detector ('Overvoltage')

In order to provide information to the CPU, so that it can decide whether the High/Low voltage state is as demanded, the voltage level on the PHI(V) line (TP8) is monitored and compared against a reference. The detector senses DC levels for DC voltage outputs, or peak levels for AC voltage outputs.

M17 is a dual comparator whose hysteresis is set to $\pm 1.22V$. For as long as the voltage on the PHI(V) line remains within approx. $\pm 125V$, the division ratio of M16 keeps the input to M17-5/9 within the $\pm 1.22V$ hysteresis, and M17-12/7 remains at logic-1 (0V).

The PHI(V) voltage at TP8 is applied via R83 and R62 to M16-2, which is referred to Common-2B, M16-3 being connected directly to this common. Resistors R61 and R68 apply feedback to M16, setting its gain to -0.0098. C29, C31 and R63 ensure that any transient switching spikes do not activate the comparator. The output from M16-6 is compared with $\pm 1.22V$ in comparator M17.

The open-collector comparator M17 is wired to detect excessive voltages at M16 output (R69 is the common bias resistor). Diodes D26 and D27 set the reference potential at M17-10 (for positive outputs) to +1.22V, and at M17-4 (negative outputs) to -1.22V. Under normal operation in low voltage state, the output voltage lies between -110V and +110V, and M16 output is between -1.07V and +1.07V. Both halves of M17 are thus held in open-collector,

If the DC PHI(V) voltage exceeds 125V (or for an AC peak corresponding to a sinewave RMS exceeding 90V), either M17-7 or M17-12 pulls towards logic-Ø. Current source Q2 permits only 3mA to flow in M17 output circuit, so the voltage input to D6 cathode and M12-11 (B trigger) suffers a negative-going trigger edge.

a. Effect of Overvoltage on DC Voltage Ranges

For DC outputs the 'Q' output of M12 is permanently held at logic-1 by DC FNCT at M12-13 set to logic-Ø, so the effect of the negative-going transition at M12-11 is suppressed. However, diode D6 conducts, pulling the HV ST line at J5-105 to logic-Ø (-15V). This is passed to the CPU, via the status register in the reference divider and the serial data interface.

The CPU is now aware that the DC output voltage exceeds 110V. The CPU has to make a decision, as to whether the programmed output voltage and the detected state are compatible. If High Voltage state has not been commanded, a fault is assumed and FAIL 2 message is presented on the MODE display.

b. Effect of Overvoltage on AC Voltage Ranges

For AC outputs the $\overline{DC\ FNCT}$ signal is inactive at logic-1, so M12-13 at logic-1 removes the reset. Monostable M12 is set to produce a logic-1 at its Q output (M12-9) unless its B input at M12-11 is edge-triggered negatively. In 'Low Voltage State' conditions no trigger is given, so M12-9 remains at logic-1, D7 and D6 are reverse-biased and the HV ST line remains at the logic-1 level of 0V.

When the comparator output switches to logic-0, D6 conducts instantaneously to obtain the earliest possible reaction to the overvoltage. But as this is a peak value, the $\overline{HV\ ST}$ signal would revert to logic-1 without monostable M12. M12 produces a logic-0 (-15V) pulse of 140ms duration, which forward-biases D7, and the HV ST line transmits a logic-0 pulse of 140ms duration. Successive positive or negative peaks of overvoltage retrigger the monostable, maintaining its Q output (and thus the $\overline{HV\ ST}$ signal) at logic-0.

7.3.8 ROUTING to the TERMINALS

The power and sense lines from J5-20/24 connect to the model 4600 analog bus via relays RL2 and RL3. When the 10A range is selected, these relays are closed and the front panel terminals isolated using relays on the Current/Ohms Assembly. Four wire sense is used, and the 4708 drives the analog bus with a -10V to +10V signal that the 4600 will convert to a -10A to +10A signal. The 4708 guard is transferred to the analog bus by the changeover relay RL4. The analog bus also contains a grounded signal ANABUSON which is used by the 4600 to detect that the 4708 is connected to the analog bus.

7.3.8.1 Current/Ohms Assembly (Circuit Diagram 430614 page 11.8-1)

With any Voltage Range selected, relays RL8 and 9 are un-energized as shown. Also, relays RL24 and RL25 (Ohms function switching - refer to page 11.8-3) are un-energized. Voltage Output relay RL23 is energized; connecting PHI(V) to J8-8/9 as 'PHI', and PLO(V) to J8-16/17 as 'PLO'.

PHI and PLO pass into the Mother assembly via at J8-25 and J8-29 respectively.

If the Current option is not fitted, a Link PCB (Part No. 410288) is fitted in its place. This shorts:

J8-25 [PHI(V)] to J8-8/9 [PHI],
J8-29 [PLO(V)] to J8-16/17[PLO].

These connections do not involve any switching.

7.3.8.2 Mother Assembly (Circuit Diagram 430604 page 11.16-1)

PHI and PLO enter at J8-8/9 and J8-16/17 respectively.

PLO passes through the common mode choke L1 via J23-3 and then J26-4 as 'I-' to the Terminal Board assembly.

PHI is switched by relay RL1. If Remote Sense is not selected, RL1 is un-energized as shown; disconnecting PHI from the I+ terminal circuit, and shorting it to the sense SHI input line. When in Remote Sense, RL1 is energized and PHI passes through the common mode choke L1 via J23-1 and J26-1, and as 'I+' to the Terminal Board assembly.

7.3.8.3 Terminal Board Assembly (Circuit Diagram 430640 page 11.17-3)

I+ and I- are filtered and passed to the front panel terminals. Ferrite bead FB1 and C2 protect the internal circuitry from the effects of HF pickup in the external circuit.

7.3.8.4 Option 42 - Rear Terminal Output (Circuit Diagram 430557 page 11.17-1 Layout Drawing 480603 page 11.19-2)

Option 42 is incorporated at manufacture. With rear output terminals, the Terminal Board assembly is not fitted. The connections to the rear are taken from J26 on the Mother assembly. A capacitor C1 connects Guard to Earth (Ground), and ferrite beads are fitted on the Hi, I+ and Guard leads at the terminals. The terminal filter relay is not fitted.

7.3.9 1V LOOP - OUTPUT SENSING

For users with Option 42 - Rear Output, the circuitry at the terminals is changed. Refer to Sect. 7.3.8.4.

7.3.9.1 Terminal Board Assembly (Circuit Diagram 430640 page 11.17-3)

If Remote Sense is selected, the front panel sense terminals Hi and Lo are connected externally to I+ and I- respectively at the load.

The sensed voltage is filtered by FB2 and C3 to reject external HF pickup. Except on the 1000V Range, a signal ('R-', 'R+') originates as 'TERM FILTER' in the Reference Divider to energize relay RL1, which introduces capacitor C1 to augment this HF rejection.

The filtered sense voltage is fed into the Mother assembly between J26-2 (Hi) and J26-5 (Lo). (No external sensing is provided for the millivolt ranges. See paras 7.3.6.3, 7.3.8.2, 7.3.9.2 and Fig. 7.1 for the simplified local sensing arrangement.)

7.3.9.2 Mother Assembly (Circuit Diagram 430604 page 11.16-1)

Lo passes through the common mode choke and directly to the Current assembly at J8-18 as SLO.

Hi also passes through the choke and enters the Current assembly as SHI at J8-10. However, if Remote Sense is not selected, it is shorted to PHI by relay RL1 for two-wire connection. RL1 is energized from the REM SENSE +ve and -ve lines from the DC assembly.

7.3.9.3 Current/Ohms Assembly (Circuit Diagram 430614 page 11.8-1)

With any Voltage Range selected, relays RL8 and 9 are unenergized as shown. Ohms function relays RL24 and RL25 are also unenergized (refer to page 11.8-3). RL23 is energized; connecting SHI into the Mother assembly as 'SHI(V)' via J8-26, and connecting SLO via J8-30 as 'SLO(V)'.

If the Current option is not fitted, the Link PCB shorts:

J8-10 [SHI] to J8-26 [SHI(V)],
J8-18 [SLO] to J8-30 [SLO(V)].

The connections involve no switching.

7.3.9.4 DC Assembly (Circuit diagram 430536 Page 11.5-2)

In normal 4-wire operation (Remote Sense selected) with OUTPUT 'ON' on the 1V and 10V Ranges, relays RL10, 11, 14 and 15 are energized.

SHI(V) enters from the Mother assembly at J5-20 and is passed directly through RL15 and RL10 contacts, 1A fuse F2, and to the range relays as SHI(DCV).

SLO(V) travels via RL15 and RL11 contacts to the range relays as SLO(DCV).

With Remote Sense not selected, relay RL14 is unenergized.
RL14-9/8 short SHI(V) to the power Hi output PHI(V).
RL14-2/3 short SLO(V) to the power Lo output PLO(V).

Refer to Page 11.5-1.

SLO(DCV) is referred to Reference Common-1. SHI(DCV) passes to the contacts 8/9/10/11 of energized 1V+10V range relay RL4, and via R77 to the inverting input of the Error Amplifier.

N.B. Although the relays are referred to above as 'energized' and 'un-energized', this is not strictly true as polarized relays are used to dispense with the power needed to hold the relays in.

This distinction is not significant to the present text, but is discussed later in *sect 7.11* where the relay logic is detailed.

7.4 100mV RANGE

The 1V Attenuator and 1V Buffer are connected into the circuit as for the 1V range. Relays RL1 and RL2 are energized. The output from the 1V buffer is connected to the star point at TP5 by RL1-7/12, and RL2-5/4 connects the Common-2 star point, at the base of the 100mV Attenuator, to Reference Common-1. Thus the 100mV Attenuator is connected across the 1V Buffer output.

The TP5 starpoint is connected directly to the Error Amplifier inverting input via RL2-9/8 and R77, completing the sense feedback. The Error Amplifier adjusts the voltage at TP5 until the error is reduced to zero; the TP5 voltage thus converges to that of the attenuated DC Ref at RL16-4.

The output of the 100mV Attenuator, at the TP6 star point, is therefore one hundredth of the DC Ref voltage, and can be varied between -200mV and +200mV. Note that the full DC Reference voltage resolution is available, so that the 100mV range resolution remains at 7½ digits. This is reflected in the resolution of the OUTPUT display on the instrument front panel.

The 100mV Attenuator output passes through RL2-2/3/10/11 to join the PHI(DCV) line. On ranges below 1V the Remote Sense relay

RL14 (*page 11.5-2*) cannot be energized; so with DC Voltage and Output ON selected, the 100mV range output is routed via RL14-9/8 and the SHI(V) line on towards the Hi terminal on the front panel for 2-wire connection.

The other connection to the load returns via the Lo terminal, arriving at the DC assembly as SLO(V), referred to Common-1 (*page 11.5-1*). Contacts 2 and 3 of unenergized Remote Sense relay RL14 connect the SLO(V) line to the PLO(DCV) line, and through the overcurrent sense resistor R56 to Common-2A. However, no overcurrent sensing is available on ranges below 1V, as R56 is shorted by the RL2-5/4 connection between Common-1 and Common-2A at the base of the 100mV Attenuator, and the contacts of the energized RL11 and un-energized RL14 (*page 11.5-2*).

N.B. Although the relays are referred to above as 'energized' and 'un-energized', this is not strictly true as polarized relays are used to dispense with the power needed to hold the relays in.

This distinction is not significant to the present text, but is discussed later in *sect 7.11* where the relay logic is detailed.

7.5 100 μ V - 10mV RANGES

These ranges use the same relay settings as 100mV Range, so the output voltages remain at 1/100 of the DC Ref voltages. The differences lie in the spans of DC Ref voltages used.

To achieve the correct DC Ref span, the appropriate scaling is computed digitally and the 4-byte binary words set in the 13-bit and 12-bit comparator latches of the Analog Interface. The DC Ref spans are scaled as follows:

| | | |
|-------------------|---|------------------|
| 10mV Range | - | -2V to +2V |
| 1mV Range | - | -200mV to +200mV |
| 100 μ V Range | - | -20mV to +20mV |

Because of this scaling, the resolution available on these ranges is reduced in proportion to the scaling ratio. The displayed output resolution is automatically adjusted according to range selection:

| | | |
|--------------------------|---|------------------------|
| 10V, 1V and 100mV Ranges | - | 7 $\frac{1}{2}$ digits |
| 10mV Range | - | 6 $\frac{1}{2}$ digits |
| 1mV Range | - | 5 $\frac{1}{2}$ digits |
| 100 μ V Range | - | 4 $\frac{1}{2}$ digits |

7.6 DC 10V LOOP

7.6.1 DC REF. and ERROR AMPLIFIER (Circuit diagram 430536 Page 11.5-1)

The DC Ref signal is derived as for the 1V range, entering the DC assembly at the same pins: J5 pins 1, 2, 3 and 4. Relay RL18 again connects the power and sense lines to the two star-points TP2 and TP3, TP3 being the signal Common-1 point.

On this range, RL16-8/9 connects full DC Ref to the non-inverting input of the Error Amplifier, which operates as for the 1V range, except that the span of voltages is now the full -20V to +20V.

7.6.2 DC \pm 2 ERROR BUFFER M14 (Circuit diagram 430536 Page 11.5-1)

The Error Amplifier output is blocked from the 1V Buffer by the open contacts 10/11 of RL16. Instead, it is connected by RL6-6/4 as input to M14.

For the 10V and 100V ranges, M14 is connected as an inverting \pm 2 line buffer by the un-energized relay RL6-6/4 and 11/13. For the 10V range, M14 output passes to the Power Amplifier assembly via J5-73 and the Mother assembly.

7.6.3 10V BUFFER (Power Ampl. Assembly) (Circuit Diagram No. 430618 pages 11.9-1/2).

The discrete, complementary, 10V Range buffer-amplifier is a dual-purpose circuit, generating power to the output terminals for both DC and AC functions.

As it provides the full output current, it is located on the Power Amplifier assembly so that the heat from its power stage can be developed outside the thermally-shielding Chassis assembly, and dissipated by forced-air cooling from the fan. Its output is fed back to the DC or AC assembly for range and output switching, as the 'DC10V+100V' signal.

The output from the line buffer M14 on the DC assembly (the signal 'DC 10V+100V+1kV ERROR') enters the PA assembly at J9-40, passing to the input of the 10V Power Amplifier via DC/AC selector relay RL4-11/13 and 10V selector RL3-9/13. The signal is attenuated by R171 and R124 in a ratio of 4.17:1. So a positive full range DC Ref signal of +10V from the Reference Divider appears at J9-40 as -5V, and is further attenuated by R171/R124 to approximately -1.2V across R124, which refers it to Common-2B.

The amplifier is best regarded as having separate DC and AC paths.

7.6.3.1 DC Path

The DC path is blocked by C56; M17 is the DC input buffer, connected as an integrator with diode clamping. M19 operates as an inverter in open loop, so applies high DC gain to the output from M17 on M19-2, referred to Common-2C by R112.

The output from M19 drives both halves of the symmetrical, inverting, discrete power amplifier through current-limiters Q21 and Q24, and is buffered by emitter-followers Q22 and Q23. Common-emitter devices Q27 and Q29 form a voltage amplifier, driving the complementary output stage Q32 and Q33. Resistors R119 and R120 set the gain of the discrete stages to approximately 4.5.

The forward amplification contains three inversions, negative DC feedback being applied to M17 inverting input by R122, defining an overall gain of 10 in conjunction with input resistor R123.

For DC range selections, the DC error signal is applied at M17-2, is amplified by 10 and output at TP11 via the low DC resistance of L8. The forward voltage gain, from the output of the Error Amplifier to the output of the 10V Buffer, is thus of the order of 1.2. This is more than sufficient to support the specified output current, when corrected to the demanded output voltage by the sense feedback to the Error Amplifier.

In AC operation, the effect of the DC path is to sense and correct the DC offsets throughout the whole AC amplifier, referring the output to Common-2A at M17-3.

7.6.3.2 AC Path

The AC path is blocked by the integrator M17, but is applied to the non-inverting input of M19 through the coupling capacitor C56. M19 operates in open loop, applying its output to the discrete power amplifier (see *para 7.6.3.1* above).

The amplifier AC gain is also set to 10 by R122 and R123, the circuit time constants being selected to allow overall instrument output operation over the full frequency range of 10Hz to 1MHz.

7.6.3.3 Overload Detection

The 10V FLAG line, connected to D71 cathode, is pulled up to 0V (in-guard logic-1) by 7.2k Ω (See *page 11.9-5* - R154 in parallel with R38). An Error OL message results from this line being driven to logic-0 by Q34. During DC operation, relay RL8 is un-energized, configuring the collector loads of emitter-followers Q32 and Q33 as low-pass filters. This de-sensitizes the overload detector and the overload limiters Q28 and Q30 from the effects of transient currents.

Overload detector Q31 reaches V_{be} threshold when the DC current value in R139 and R141 exceeds approximately 35mA. Similarly, Q34 detects currents in R147 and R149. In either case, Q34 conducts, pulling diode D71 cathode down to -15.7V. This drives the 10V FLAG line to logic-0, so the status message is returned to the CPU via the SSDA serial interface, and the 'Error OL' message is displayed.

This does not preclude further increase in output current, but under these conditions the instrument accuracy specification is not guaranteed.

During AC operation, relay RL8 is energized, the filter is removed, and the Overload Detector is adjusted to operate as a peak current detector. R172/R141 and R173/R147 cause the 10V FLAG to activate for RMS values of output sinewave current in excess of approximately 80mA.

7.6.4 RANGE SWITCHING (DC Assembly) (Circuit Diagram 430536 *Page 11.5-1*)

The DC 10V+100V signal enters the DC assembly from the Mother assembly at J5-37/38 and R73/L6 filter out any spikes picked up in transit. Relay RL4 is energized, shorting the high voltage resistor R67, so the signal goes directly through the 1Amp fuse F1 to the 1V+10V+100V star-point.

7.6.3.4 Overload Limiting

If the DC output current increases to approximately 39mA, the current in either R139 or R149 causes the V_{be} threshold of Q28 or Q30 to be exceeded, shunting the base current of the corresponding voltage amplifier. Thus the output drive to the final stage is limited.

In AC operation, if the RMS output current increases to approximately 100mA, the peaks of current cause the V_{be} threshold of Q28 or Q30 to be exceeded. The output drive to the final stage is limited at this level.

7.6.3.5 Output Protection

The output current passes through the combination of R144 and L8. At DC and low frequency AC, the inductor provides a low output impedance, whereas at high frequencies the resistor stabilizes the amplifier when driving capacitive loads.

7.6.3.6 10V Buffer Output

For DC and AC 10V ranges, relay RL3 is energized.

For DC, RL4 is un-energized, so the 10V Buffer output passes via RL3-8/4 and RL4-4/6 as the 'DC 10V+100V' signal, J19-19/20 to the Mother assembly, and thence to the DC assembly.

For AC, RL4 is energized, diverting the 10V Buffer output via RL4-4/8 as the 'AC 10V+100V' signal, and out at J19-15/16 via the Mother assembly to the AC assembly.

7.6.3.7 10V Amplifier Power Supplies

M17 and M19 are supplied from 15V Common-2A rails, but the discrete amplifier receives power from the 38V supply, which is also used for the Error Amplifier on the DC assembly.

7.6.5 REMAINDER OF THE 10V LOOP

From this point, the 10V range loop follows the same path as the 1V loop, both outwards to the I+ and I- terminals and back to the Error Amplifier inverting (sense) input. Of course, on the 10V range, the returning sense signal is compared with the full DC Ref voltage, rather than the attenuated DC Ref for the 1V range. Refer to *sub-section 7.3*; from *para. 7.3.6* onwards.

7.7 DC HIGH VOLTAGE LOOPS

The instrument includes two high voltage DC ranges. The 100V range extends from -200V to +200V full scale, the 1000V range from -1100V to +1100V full scale.

The simplified block diagram of Fig. 7.2 illustrates the high voltage DC circuit arrangement and signal flow. The details of the 100V and 1000V ranges are described in Sub-sections 7.8 and 7.9.

7.7.1 HIGH VOLTAGE DELIVERY

Both ranges employ the same referencing arrangement used for the 10V DC Range, but the techniques necessary to generate high voltages differ from those in the low voltage loops:

- For the 100V Range, a VMOS circuit amplifies the $\pm 20V$ Reference directly, as a DC signal, powered from a separate $\pm 400V$ supply. The 100V range voltages are passed back via the range switching circuitry in the DC assembly to be output from the instrument as for the low voltage ranges.

- For the 1000V Range, the DC reference is first converted to a 16kHz AC signal, amplified in the same 100V amplifier, then stepped up to 1000V range voltages through a separate transformer. Subsequent high voltage rectification, filtering and polarity-switching converts the AC output from the transformer secondary into a DC voltage. A separate line conveys the 1kV range voltage back to the DC assembly for range switching and output from the instrument.

7.7.2 HIGH VOLTAGE SENSING

A guarded high-voltage switched precision attenuator reduces the DC sense voltage from the Hi and Lo terminals to Reference levels. The attenuated sense voltage is compared with the DC Ref voltage, their difference being used as an error signal to correct the range output level.

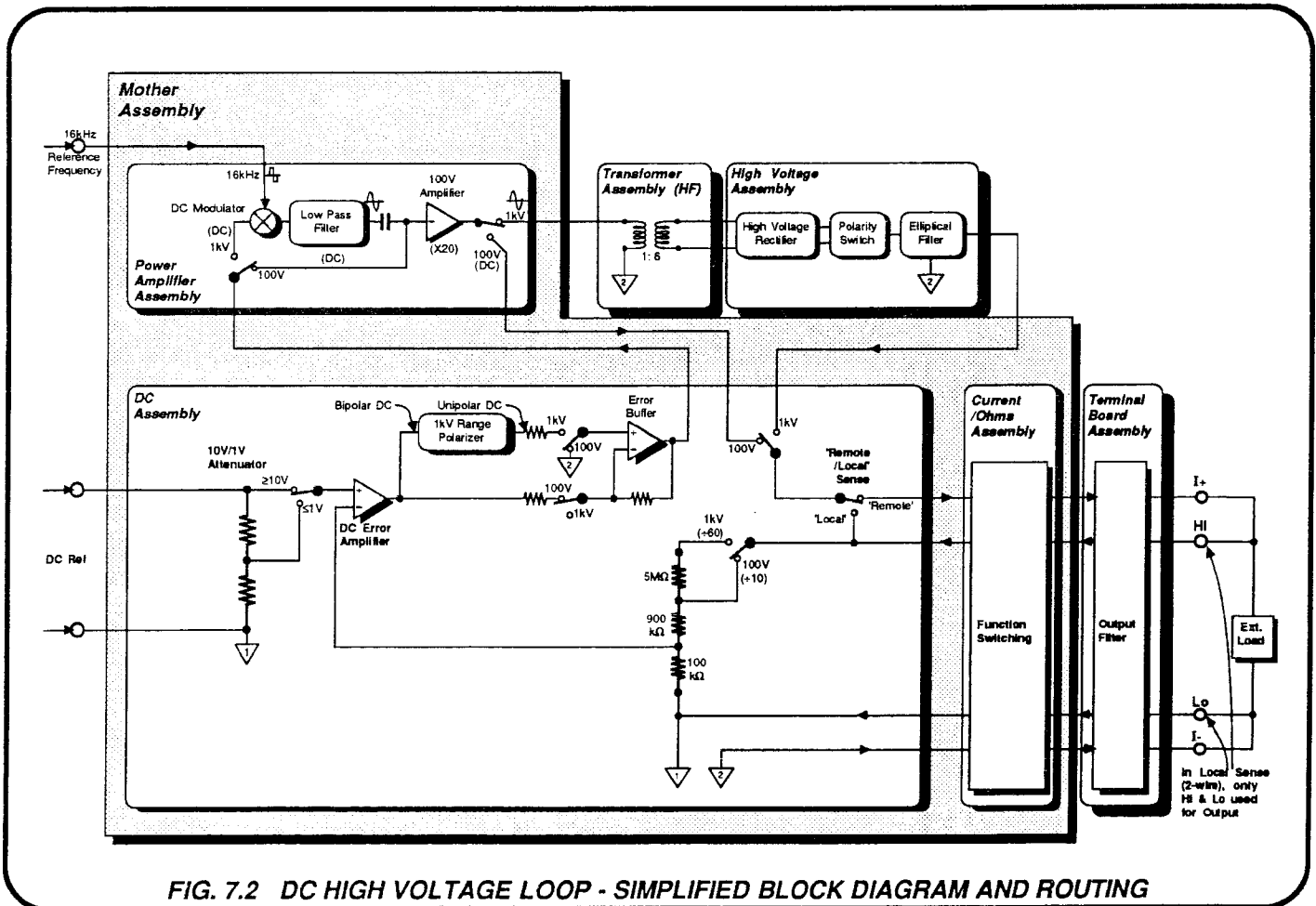


FIG. 7.2 DC HIGH VOLTAGE LOOP - SIMPLIFIED BLOCK DIAGRAM AND ROUTING

7.8 100V RANGE

7.8.1 INTRODUCTION

The '10V+100V+1000V DC ERROR' signal, generated by the +2 DC Error Buffer in the DC assembly, enters the Power Amplifier as for the 10VDC range; but the 10V Amplifier is bypassed for the high voltage ranges.

On the 100V range, the signal is switched directly into the 100V Amplifier, where it is scaled up by a factor of -20, the amplifier output being delivered via the 'DC 10V+100V' line to the PHI(DCV) line on the DC assembly. Thereafter the output is transferred to the instrument terminals as for the 10V range.

7.8.2 100V RANGE POWER ROUTING

7.8.2.1 DC Reference and Error Amplifier (Circuit diagram 430536 Page 11.5-1)

The DC Ref signal is derived as for the 1V range, entering the DC assembly at the same pins: J5 pins 1, 2, 3 and 4. Relay RL18 again connects the power and sense lines to the two star-points TP2 and TP3, the latter being the signal Common-1 point.

On the 100V range, RL16-8/9 connects the full DC Reference to the non-inverting input of the Error Amplifier, which operates as for the 1V range, except that the span of voltages is now the full -20V to +20V.

7.8.2.2 DC +2 Error Buffer M14

The Error Amplifier output is blocked from the 1V Buffer by the open contacts 10/11 of RL16. Instead, it is connected by RL6-6/4 as input to M14.

For the 10V and 100V ranges, M14 is connected as an inverting +2 line buffer by the un-energized relay RL6-6/4 and 11/13. For the 100V range, M14 output passes to the Power Amplifier assembly via J5-73 and the Mother assembly.

7.8.2.3 Power Amplifier and Output Routing (Circuit Diagrams: 430618 pages 11.9-2 and 11.9-3; 430536 page 11.5-1)

'DC Error' enters the Power Amplifier assembly at J9-40 (refer to page 11.9-2). Relay RL3 is un-energized, shorting the 10V Amplifier input; and RL4 is un-energized, routing the DC Error signal to the 100V Amplifier as signal '100V I/P' (page 11.9-3).

Energized relay contacts RL2-8/4 apply the signal to the Gain Stage, which provides drive to the power amplifiers in the positive and negative heat sinks, via J3-12 and J3-11. The single-ended output from the heatsinks at J3-9 passes via R89, L7 and relay RL2-13/9 (RL2 energized), to RL3-6 (page 11.9-2), and onto the 'DC 10V+100V' line via RL4-4/6, R174 and J9-19/20.

On the DC assembly (page 11.5-1), the signal is routed to the PHI(DCV) line as for the 10V range.

7.8.3 100V AMPLIFIER (Circuit Diagram 430618 page 11.9-3)

The 100V amplifier is in three stages:

- **Gain Stage:** this is similar to the first stage of the 10V amplifier, but with a different distribution of gain.
- **Driver Stage:** providing most of the gain, this stage runs from a regulated 400V supply.
- **Buffer Output Stage:** complementary MOSFET circuits, located on the positive and negative heatsinks, provide a single-ended output with the required voltage swing, at low impedance.

The voltage gain for the whole 100V amplifier is set at 100 by the input resistors R74/R71 and the feedback resistor R88.

The 100V amplifier is also used for 100V AC outputs, and on the DC and AC 1000V ranges to drive the step-up transformer. For this reason the following description is applicable to both DC and AC signal processing, and will be referred to in the sub-sections dealing with those functions and ranges.

7.8.3.1 Input to Gain and Driver Stages (Circuit Diagram 430618 pages 11.9-2 and 11.9-3)

The DC ERROR signal enters the PA assembly at J9-40, passing to the input of the 100V Power Amplifier via relays RL4-11/13 and RL2-8/4. It is referred to common 2B by developing a voltage across R72.

7.8.3.2 DC Offset Correction

M10 is the DC offset integrator, with diode clamping. It provides a DC input to the non-inverting input of the voltage gain amplifier M8, controlling its DC offset. This is similar to the arrangement in the 10V Amplifier.

7.8.3.3 Signal Processing

M8 is a high speed hybrid amplifier operating as an inverter. With link LKD normally made, its stage gain is approximately 2.5, frequency compensated by C18 and C72. It operates from the 15V Common-2B supplies, but its signal output is converted into a current by Q10 and Q8; allowing its mean DC voltage for AC signals to reach the -400V levels required to operate the driver MOSFET output circuit. Diodes D44, D43 and D36 prevent negative latch-up.

Voltage Regulator M21 sets its pin 1 to +12V. Common-emitter buffer Q10 drives the capacitance of Q8 source-gate from the output of M8, forming a cascode current generator. The drain of p-channel MOSFET Q8 passes the signal current to the mirror Q12/Q11 at voltages close to the negative 400V rail.

The current-mirror output transistor Q11 is also in cascode with its associated MOSFET Q9. Emitter resistor R53 defines the current in Q9, the ratio R52/R53 setting the mirror's current gain.

MOSFETs are inherently capacitive, so measures are taken to nullify the effects, on slew rate, of the capacitive currents between Q9 electrodes. The cascode arrangement ensures that any source-gate and source-drain capacitive currents join the main flow of source current and have little effect on slew rate.

The Miller feedback of the drain-gate capacitance has the greatest effect on slew rate, generating AC currents between anti-phase electrodes which normally pass into the input circuit. In this arrangement, Q13 diverts these currents back into the cascode current, while maintaining a standing bias of about 4 volts between gate and source. These measures minimize the reduction of Q9 operating bandwidth.

R51 and D42 provide Q13 operating bias, and D51 protects the bias circuit. The high-power resistor R49 refers the bias circuit to Common-2, and C26 stabilizes the base-emitter bias of Q13. Zener diode D39 protects the MOSFET from source-gate voltage breakdown.

7.8.3.4 Driver Regulator

At Full Scale on the 100V AC range, the output from the driver is 200V RMS. This requires Q9 drain to provide a peak-to-peak voltage swing approaching 600 Volts, as there is no voltage gain in the heatsink power amplifiers. The positive supply which provides Q9 current therefore needs special regulation.

The 400 volt supply is at this point unregulated, so can contain line ripple and level variations, this noise level being critical to the output performance. To define a stable supply voltage, a DC restoration circuit is employed as a trough detector, maintaining a level about 5V below the most negative excursions of the ripple.

At power-up, 75V zener D57 allows a rapid charge of reservoir capacitors C49 and C59, until the charge reduces D57 voltage below the avalanche level. When D57 cuts-off, R100 provides a charge path of $1M\Omega$, giving a time constant of approximately 10 seconds. The smoothed voltage across C49/C59 is divided by R101, R86 and R87; so a small voltage is dropped across R101, and Q20 gate is held about 5V below the +400V(2)B line voltage. The N-channel source-follower Q20 thus provides a quiet, low-impedance DC supply voltage.

Zener diodes D60 and D61 divide the voltage across C49 and C59, so that their breakdown voltages are not exceeded. The 10V zener D54 protects the TMOS gate/source from excessive voltages.

The opto-coupler M16 permits the 400v supply to be switched off, allowing D56 to assume forward bias, thus connecting the rail to the +38V supply. This facility is made available to reduce the voltage across R65, and hence its continuous power loading, when the instrument is delivering a DC output of negative polarity. M16 is turned off for AC and positive DC outputs, by the 'POSITIVE' signal from the processor being set to logic-1 (0V). Thus M16-6 is isolated from M16-5, and the +400V rail out of the regulator remains energized. For negative DC outputs, the cathode of the LED in M16 is pulled to logic-0 (the POSITIVE signal being set to -15V on M16-3 - see page 11.9-5); the LED emits, and M16-6/5 shorts out D54 turning Q20 off. The total supply voltage for negative outputs is then limited to 438V.

At HF, inductor L6 appears as a current source, increasing the impedance of Q9 drain load with frequency to compensate for capacitive loading. It has the advantage of not increasing the net power dissipated in the stage; any active current source would have significant output capacitance. The 12-watt resistor R65 is the main resistive drain load for Q9.

7.8.3.5 Driver Output

The driver develops its output voltage, which can involve peak-to-peak AC swings of up to 600V, across the load resistor R65. Zener diode D41 is included to clamp the output in the event of the heatsinks being disconnected. This is normally held below avalanche by the current passing through a series bias buffer (Q8) in the Positive Heatsink assembly, via J3-11 and J3-12.

The main frequency compensation is performed by capacitor C12. This could have been connected to the drain of Q9, but the output line slew rate is sensitive to capacitive loading. Instead it is connected via J2-7, to a low impedance point in the Negative Heatsink assembly, which follows the driver output voltage swing.

7.8.4 100V POWER AMPLIFIER

(Circuit Diagrams 430637 page 11.13-1
and 430539 page 11.13-2)

The 100V power amplifier stage is split between the Positive and Negative Heatsink assemblies. The driver output voltage is connected into the Positive assembly, and the frequency compensation feedback is derived in the Negative assembly.

The whole circuit is a complementary, single-ended push-pull amplifier with unity voltage gain. To achieve the full 300V peak voltage output, two MOSFET source-followers are connected in cascode, for each polarity, in a totempole arrangement.

To obtain the required peak current levels, each source-follower consists of two MOSFETs in parallel. In all, therefore, eight MOSFET devices are used.

On 100V ranges, the output currents are such as to bias the amplifier in class A, but on 1000V ranges the output currents impose class AB conditions. Crossover distortion is minimized by a regulated bias, generated by a V_{gs} multiplier (M1 in the Positive Heatsink assembly).

Power for the amplifier is provided by the same 400V supply that serves the driver circuit. To minimize internal temperature by improving efficiency, overall power loss is reduced by regulation only where required. Thus only the driver stage is regulated, allowing the power amplifier to take power directly from the unregulated supply. Being source-followers, the ripple on their 400V rail is not transmitted.

7.8.4.1 Positive Heatsink Assembly (Circuit Diagram 430637 Page 11.13-1)

N-channel MOSFETs Q1 and Q2 are connected in parallel, as are Q3 and Q4. All devices are matched for power dissipation and threshold voltage for an even dissipation of approximately 400W between the two heatsinks. All gate-source potentials are limited by 10V zeners.

The input voltage from the driver is present at J3-11 and J3-12. Most of the driver load current passes through the bias buffer Q8, and the voltage developed across Q8/R21 is applied to the bias control R10. The Vgs multiplier M1/Q8 acts as a high gain shunt regulator, generating a bias of between 5V and 9V, set by R10. The regulator's own bias chain of Q9, D8, and Q5 (which is connected as a diode) responds to the temperature of the heatsink to compensate for the temperature coefficients of the MOSFETs.

The 'DRIVE-' voltage at J3-11 is transferred directly to the negative heatsink input via J1-7 (Circuit Diagram 430539 page 11.13-2).

The 'DRIVE+' voltage at J3-12 is buffered by Q7 and applied to the gates of Q3 and Q4. In the event of an output short-circuit, Q6 detects the output current as a voltage across R14, imposing a hard limit of 1.5A by reducing the signal voltage at the input to the MOSFET gates.

The series gate resistors R5 and R6, together with their associated drain-gate capacitances, form the dominant pole of the amplifier. Damping resistor R19 with ferrite bead FB1, prevent local oscillations in emitter-follower Q7.

Q1 and Q2 act as buffers to provide a bootstrapped supply for the output devices Q3 and Q4, splitting the overall power dissipation to four points of application to the heatsink. The gates of Q1 and Q2 receive their drive from the output line, obtained via the divider R16/R22/R23/R15. Capacitors C10 and C13 decouple any noise on the 400V rail; C11 and C12 correct any lag which may be generated by C10 and C13. C5 and C6 control the division ratio at HF, swamping any stray capacitance.

The drains of Q3 and Q4 are shorted together, and connected via J1-5 by a 10nF capacitor to the corresponding point in the Negative Heatsink, completing an AC bootstrap (BS). The gates of Q3/Q4 (J1-1) and Q1/Q2 (J1-4) are similarly linked to their corresponding points in the negative heatsink. This ensures that AC swings in both polarities are identical.

The combined output from the Positive and Negative Heatsinks is transmitted back to the Power Amplifier assembly via along the screen of the input connection.

7.8.4.2 Negative Heatsink Assembly (Circuit Diagram 430539 Page 11.13-2)

This is virtually a mirror image of the Positive Heatsink circuit. However, because the P-channel MOSFETs are operating closer to their maximum voltage rating, they are further protected by Zener diodes which limit their drain-gate potentials.

The HF swamp capacitors are not required, as the whole circuit is AC-bootstrapped to corresponding points in the Positive Heatsink assembly, via C1, C2 and C4.

HF compensation for the driver and output stages is derived at low impedance from the junction of R2 and D12. It feeds back via J2-7 to the driver output circuit, through C12 in the Power Amplifier assembly, to avoid capacitively loading the driver output line.

7.8.4.3 Over-Temperature Detection

The two NTC thermistors in each heatsink circuit are part of a bridge network which detects excessive temperatures on the heatsinks. The action of the bridge is described in section 7.12.9.

7.8.4.4 100V Output Connection

DANGER!

For guarding purposes, the output from the heatsinks is transmitted back to J3-9 of the Power Amplifier assembly along the screen of the input cable. The voltages on this screen are POTENTIALLY LETHAL. Utmost caution should be exercised when working in its vicinity.

7.8.4.5 Heatsink Removal

The 100V Amplifier can work with the heatsinks removed, because of the clamp diode (D41 on page 11.9-3) in series with the driver load. If they are removed, however, J3-9 and J3-11 in the disconnected socket of J3 must be connected together, to maintain the feedback. In this condition, the gain falls due to loading of the driver by resistors in the DC or AC assembly.

7.8.5 POWER SUPPLIES AND PROTECTION

Three main power supplies are employed in the Power Amplifier:

- **15V Common-2 in-guard supply.**

This is used for all low voltage applications, including the switching and functional logic. For the most part the logic conforms to the standard: logic-0 = -15V; logic-1 = 0V.

- **38V Common-2 supply.**

Required mainly for the 10V Power Amplifier, but also for negative DC outputs in the 100V Amplifier driver, this supply is generated on the separate 38V Power Supply assembly (Refer to page 11.12-1). Part of the supply circuit is situated on the Mother Assembly.

- **400V Power Supply.**

The 100V Power Amplifier used for the 100V and 1000V ranges, for both DC and AC outputs. The line transformer secondary output is rectified and smoothed on the Mother assembly, and the main regulator circuitry for the driver stage is contained on the Power Supply / Current Heatsink. The power output stage of the 100V Amplifier receives unregulated 400V supply. Extensive protection is incorporated.

7.8.5.1 38V Supply

(Circuit Diagram 430653 Page 11.12-1)

The mains (line) transformer secondary centre tap is referred to Common-2 on the Mother assembly after passing through the 38V Power Supply assembly. This secondary also provides an adjustable AC output for the 'Common Mode Null' balancing circuit.

A single bridge rectifier on the Mother assembly provides both positive and negative raw supplies for the foldback regulator in the 38V Power Supply assembly.

The 38V supply circuit is described in *Section 6.7, para 6.7.3.4*.

7.8.5.2 400V Transformation and Rectification

(Circuit Diagram 430604 Page 11.16-5)

The mains (line) transformer secondary centre tap is referred to Common-2 on the Mother assembly. The secondary is switched with the secondary for the 38V supply, to allow a lower voltage to drive the 100V power amplifier for servicing purposes. Under operational conditions in the 4708, this switch, which is situated prominently on the Mains Transformer assembly, is set to the 400V position.

A single bridge rectifier on the Mother assembly uses series diodes to achieve the high peak inverse voltage performance required for the 400V supply.

After smoothing, and part-loading by a bleeder resistor chain (the bleeder resistors also balance the voltages across the capacitors); the rectifier output is passed via J31, to provide both positive and negative raw supplies for the foldback regulator in the PS/I Heatsink assembly.

7.8.5.3 400V Current Control

(Circuit Diagram 430540 Page 11.13-3)

When the 400V supply is enabled, the LEDs in opto-isolators M1 and M2 are conducting, allowing their opto-transistors to be energized. As the circuits for both polarities are otherwise symmetrical, only the positive circuit is described.

Zener Diode D8 protects the source-gate circuit of level-shifter Q3. This N-channel MOSFET supplies a current of 1.4mA, as defined by Q8, to the current-monitor reference zener diode D7. This current is available only if the 400V supply is enabled by M1, otherwise Q4 base is pulled down by D1/R9, Q4 conducting via D7 so Q9 is pinched off.

Under normal operating conditions the Power Amplifier supply current is drawn through the P-channel MOSFET Q9, which is held in conduction by R8, R12 and D2. The current is sensed by the parallel combination of resistors R17 and R32. Although the peaks of the current taken by the power amplifier can reach 1.4A, the mean value is less than 0.5A. Ripple currents making up the difference are smoothed by the main reservoir capacitors C31 and C22 on the Power Amplifier assembly (*page 11.9-3*).

For mean currents more than approximately 0.5A (in particular for output short-circuits); the voltage sensed across R17/R32, subsequently divided by the attenuator R10/R9, exceeds the threshold of Q4/D7. Q4 conducts to pass current into R8, reducing the drive to Q9 gate, so the +400V(2)B voltage at D5 anode falls. When the voltage dropped by Q9 rises to 56V, zener D5 conducts and pulls Q4 base down, further reducing the drive to Q9 gate. This cumulative action is slowed only by the time constant of the combination R34/C15, so that both voltage and current on the +400V(2)B line are simultaneously closed down.

With a persistent 400V overload, the circuit cannot recover naturally from this 'foldback' mode. However, the 400V voltage is monitored. If the 400V monitor senses a failure, a status bit is passed back to the CPU via the SSDA serial link. The CPU makes three attempts to reinstate correct operation by removing the PA bias while restarting the supply via the 400V enable line. If after the third attempt the voltage does not recover, the CPU assumes that a hardware fault is present, so displays the 'FAIL 7' message.

7.8.5.4 100V Current Sense and 1kV Overvolts Detector

(Circuit Diagram 430618 Page 11.9-6)

This detector circuitry is used only for AC High Voltage ranges, and is described with the AC Voltage Amplitude Control system in *Section 9*. However, as the 400V supplies pass through the circuit for DC high voltage ranges, it is worth a mention at this point.

The 400V(2)B lines enter the Power Amplifier assembly from the PS/I Heatsink at J1-8/6 and are filtered by L1 and L2 before being applied across two neon lamps LP1 and LP3. These lamps are visible from the top and rear of the instrument when the PA board is exposed, indicating that a dangerous voltage is present.

The 400V(2)B lines pass on to power the driver stage of the 100V amplifier, where the voltage is regulated as described in *sect. 7.8.3.4*.

The 400V(2)C lines supply the power amplifier in the Positive and Negative Heatsinks.

On the AC 100V range, the current in each of these lines is used as an analog of the load placed on the amplifier. (On the 1000V ranges, any overload is sensed by an AC or DC overcurrent detector in the DC assembly.) On the AC 1000V Range, the voltage applied to the primary of the step-up transformer is fed via a resistor to the detector at M2-5/9. The '100V AC' line is set to logic-Ø (-15V) only when the 100V AC range is selected.

7.8.6 PA POWER SUPPLY MONITORS

(Circuit Diagram 430618 Page 11.9-4)

All three power supply voltages: 15V, 38V, and 400V; are monitored using similar comparators to initiate individual 'FAIL' messages. In addition, if either the 400V or the 15V circuit detects a low power supply voltage, the 400V supply is disabled.

7.8.6.1 Comparator Supply Protection

To ensure that failure of either the 15V or the 38V supply does not remove the power from the three comparators, these two sources are 'OR'ed by D5, D6, D15 and D16 (the 38V supply being ballasted by R1 and R15) to provide the V+ and V- supply to the Quad op-amp M3. In nine of the possible sixteen states of failure of these two supplies, power will still be applied to the comparators. The maximum values of V+ and V- are limited to +16V and -16V by zener diodes D7 and D14.

7.8.6.2 15V Monitor

Zener diode D29 is the 2.45V reference for the 15V comparator. It is ballasted by R27 to V+, and its +2.45V above the -15V rail is applied to the non-inverting input of M3c. The +15V to -15V supply is divided by R29/R30/R33, generating a voltage +2.50V above the -15V rail at the inverting input to M3c under normal operating conditions. Thus the output at M3c-7 remains at the negative (V-) rail, holding D28 in forward bias, and the 15V(2) FAIL line at J9-108 is held at Logic-Ø (-15V).

If the voltage between the ±15V supply rails falls to less than 29.4V, the voltage across R30/R33 falls to less than the reference 2.45V. The output at M3c-7 changes state to the V+ rail, reverse-biasing D28, so the 15V(2) FAIL line is pulled to logic-1 (0V) by R28.

The logic levels on the 15V(2) FAIL line pass via the Mother assembly to the Parallel/Serial status registers in the Reference Divider assembly (M18-5 on page 11.4-4). During each control data transfer, the SSDA also passes the condition of the status registers back across guard to be read by the CPU. When the 15V(2) FAIL line switches to logic-1 due to a 15V failure, this is detected by the CPU which produces the FAIL 9 message on the MODE display.

The 15V monitor output line also gives an input to the 400V enable logic (sect 7.12.5). The effect of a 15V failure is to disable the 400V(2)B regulated supply via D26 conduction and J1-3 at logic-1.

7.8.6.3 38V Monitor

The action is similar to the 15V monitor, but because of the higher voltage, the divider between the +38V and -38V lines is balanced by two 10kΩ droppers in each line. Without Q5, the 2.45V zener bias current would affect the sensing level. By employing Q5 as a voltage follower, D25 bias current can pass directly to the V- rail and still be referred to the R25/R26 junction. The V_{be} drops in Q5 cancel one another out, so the zener and the sensor R25/R32 are referred to the same potential.

In normal operation the voltage across the 715Ω of R25/R32 is approximately 2.62V, in excess of the 2.45V of D25.

If the 76V between the +38V and -38V rails fails by falling to 71V, the voltage at M3b-2 falls below that at M3b-3, and the output at M3b-1 changes state from -V to +V. The action of D22 and the 38V(2) FAIL line are the same as for the 15V monitor.

7.8.6.4 400V Monitor

The 400V Monitor is in two mirrored halves, each dealing with its own polarity of the supply, so only the positive half is described.

Zener D9 provides the +2.45V reference on the non-inverting input at M3d-12. The divided +400V is sensed across R16 at a normal operating voltage of +3.27V (referred to common-2C) and applied to the inverting input at M3d-13, thus setting the output at M3d-14 to the V- rail voltage. D20 is reverse-biassed so the 400V(2) FAIL voltage is pulled to logic-Ø (-15V) by R7.

If the +400V supply fails by falling below +300V, the voltage across R16 falls below the +2.45V reference and the M3d-14 output switches to the V+ rail voltage. D20 conducts, pulling the 400V(2) FAIL line at J9-106 to logic-1.

In normal 400V operation R31 is shorted by the 400V/50V switch on the Mains (line) transformer, via the 'Lo SUPPLY A' and 'Lo SUPPLY B' lines. When the switch is set to 50V, the Lo SUPPLY A line is connected to -15V, effectively disabling the monitor output by holding the 400V(2) FAIL line at logic-Ø.

The output line gives an input via D3 to the 400V enable logic (described in sub-section 7.12.5). Its effect is as for a 15V failure.

7.9 1000V RANGE

7.9.1 INTRODUCTION

7.9.1.1 Power Signal Processing

Method

The 1000V DC Range obtains its high voltages by using the 100V power amplifier to drive an AC signal into the primary of a step-up transformer. The AC signal is derived by modulating a 16kHz reference with the DC ERROR signal.

Error Signal Conditioning

The '10V+100V+1000V DC ERROR' signal is pre-conditioned by the VCA Drive circuitry in the DC assembly, before it enters the Power Amplifier. The 10V Amplifier is bypassed.

High AC Voltage Generation

The modulated 16kHz signal is passed from the DC modulator into the 100V Amplifier, where it is scaled up by a factor of -100, the amplifier output being delivered via the 'OUTPUT' line to the HF Transformer assembly.

Rectification and Output

The stepped-up secondary voltage is rectified and filtered in the High Voltage assembly:

- A constant-current source acts as a shunt to sustain the current drawn from the high-voltage secondary winding through the bridge rectifier. Polarity is switched with respect to common-2 via the LC-filtered 38V common-2 supplies. Positive polarity output is referred to -38V at zero output, to overlap with negative polarity output referred to +38V. The overlap allows digital calibration constants to be used to align zero voltage output in both polarities to the same calibrated zero.
- The main output filter is placed in the output line. This is a low-pass filter with a high rejection at 16kHz, reducing the ripple voltage to within specification limits.
- The output voltage is fed out through the Range switch on the DC assembly, where it is subject to Remote Sense and Output On/Off switching, before being passed to the I+ terminal by the same route as for low voltage ranges. High voltage status is detected on the DC assembly as described in *para 7.3.8.2* for the 1V Range.
- The external current is sunk into common-2 via the overcurrent detector, which warns the control processor when the output current exceeds approximately 28.5mA (*see para 7.3.8.1*). On the 1000V range the processor will switch the output off on receipt of the overcurrent signal from the overcurrent detector.

7.9.1.2 Sense Loop

Sense Attenuation

The sensed output voltage from the Hi and Lo terminals is reduced down to 'DC Ref' levels by a guarded precision attenuator on the DC assembly, and then applied to the inverting input of the Error Amplifier:

- The Lo terminal and Sense Attenuator Lo are both referred to Common-1 (DC Ref Lo). The attenuator is dual-purpose, being used for both 100V and 1000V ranges. The Hi sense voltage is divided in the Sense Attenuators by 10 (100V Range) or 60 (1000V Range).
- The attenuated output is compared against DC Ref Hi in the Error Amplifier, modifying its output to the VCA Drive.
- The 10V Bootstrap, in addition to supplying the Error Amplifier, also buffers DC Ref Hi as reference for the VCA Drive circuit.

Error Conditioning

The bipolar DC error voltage between the buffered DC Ref Hi and the Error Amplifier output is converted by a switched precision rectifier in the 'VCA Drive', to provide a suitable unipolar control signal for the DC modulator. The buffered output from the rectifier becomes the '10V+100V+1000V DC ERROR' signal which adjusts the amplitude of the 1000V Range outputs.

Loop Action and Reference Scaling

The Sense loop thus stabilizes the 1000V Range DC output to a value which is 60 times the DC Ref voltage, this value being determined by the division ratio of the precision sense attenuator. The DC Ref voltage is scaled digitally so that Full Scale of 20V corresponds to 1100V on the OUTPUT display and at the output terminals.

7.9.2 1000V RANGE POWER ROUTING

7.9.2.1 DC Reference and Error Amplifier (Circuit diagram 430536 *Page 11.5-1*)

The DC Ref signal is derived as for the 1V range, entering the DC assembly at the same pins: J5 pins 1, 2, 3 and 4. Relay RL18 again connects the power and sense lines to the two star-points TP2 and TP3, the latter being the signal Common-1 point.

On the 1000V range, RL16-8/9 connects the full DC Reference to the non-inverting input of the Error Amplifier, which operates as for the 1V range, except that the span of voltages is now the full -20V to +20V.

The Error Amplifier output is blocked from the 1V Buffer by the open contacts 10/11 of RL16. Instead, it passes as input to M15-5. The error signal is conditioned by the VCA Drive circuit M15/M14 and passed to the line buffer at M14-5. For the 1000V range, M14 is connected as a non-inverting line buffer by contacts 8/4 and 9/13 of energized relay RL6. M14-7 output passes to the Power Amplifier assembly via J5-73 and the Mother assembly.

7.9.2.2 Power Amplifier Routing (Circuit Diagrams: 430618 *pages 11.9-2 and 11.9-3*)

'DC Error' enters the Power Amplifier assembly at J9-40 (Refer to *page 11.9-2*). Relay RL3 remains un-energized, shorting across the 10V Amplifier input. The DC Error signal is routed via link LK.W and TP14 to the 1kV DC Modulator at R78. The route to the 100V Amplifier input as signal '100V I/P' via RL4-11/13 is blocked by the open contacts 8/4 of unenergized relay RL2 (*page 11.9-3*).

The output from the modulator is a 16kHz AC signal at TP15 whose amplitude is determined by the value of the DC Error signal. With RL1 unenergized on the 1kV DC Range, this AC signal passes via RL1-11/13 contacts to the '1kV ERROR O/P' line.

RL2-6/4 contacts (*page 11.9-3*) apply the signal to the Gain Stage, which provides drive to the power amplifiers in the positive and negative heat sinks, via J3-12 and J3-11. The single-ended output from the heatsinks at J3-9 passes via the OUTPUT line to the 1kV ENABLE relay contacts RL6-8/9 (*page 11.9-2*). RL6 is energized, and RL7 is unenergized on the DC 1kV Range, so the OUTPUT line is connected to J5-3 (PA assembly) and out as a direct link to the High Frequency Transformer assembly.

7.9.2.3 High Voltage Assembly Routing (Circuit Diagram 430537 *page 11.14-1*)

The high voltage output from the secondary of the HF transformer is input to the High Voltage assembly between its J2-1/2 and J2-8/9. After rectification, polarity switching and filtering, the DC 1kV signal is output via J1-2/3 to pin L on the Mother assembly, where it is again filtered before passing to the DC assembly on J5-33/34.

7.9.2.4 DC Assembly Power and Sense Routing (Circuit Diagram 430536 *page 11.5-1*)

On the DC assembly, the DC 1kV signal line is fused at 1A by F5, and the signal is routed through RL7-5/4. At this point the voltage is also used to energize the attenuator guard network R15 etc. It is routed to the PHI(DCV) line through RL7-10/11, then out to the I+ terminal and back from the Hi terminal on the SHI(DCV) line as for the 1V range. The current returning from the I- terminal is sunk into common-2 via the overcurrent detector R56 (*see para 7.3.8.1*).

SHI(DCV) is range switched on to the HV attenuator R17 etc. by RL7-8/9, the reduced voltage being taken off through RL9-10/11 and applied to the inverting input of the Error Amplifier.

7.9.3 VCA DRIVE CIRCUITRY (Circuit Diagram 430536 page 11.5-1)

The attenuated sense signal is applied to the inverting input of the Error Amplifier via RL9-10/11. This bootstrapped, high gain circuit compares the sense signal with DC Ref. When both are equal; the output at M20-6, the bootstrap common BS at TP1, DC Ref Hi and the sense signal are all at the same level. Therefore the differential input to the error buffer-comparator M15 is zero at M15-6/5.

The second M15 stage acts as a bipolar-unipolar switch which adapts the bi-polar action of the Error Amplifier to the unipolar sensitivity of the DC modulator:

- With the front panel OUTPUT ON+ LED lit, the POSITIVE control signal is at logic-1 (0V). FET Q1 conducts, setting the M15-3 non-inverting input to zero volts, so the amplifier inverts the input at M15-2.
- Alternatively, if the OUTPUT ON- LED is lit the POSITIVE signal is at logic-Ø (-15V), cutting off Q2. M15-3 follows the M15-7 voltage, so the amplifier acts as a voltage follower.

The gain from M15-7 to the I+ terminal is approx. x2000. R87 and C40 at the Error Amplifier input; and R40, C21 on the first stage of M14; provide frequency compensation for the overall loop.

For the 1000V range, the second M14 stage is connected as a non-inverting line buffer by contacts 8/4 and 9/13 of activated relay RL6. The output from M14-7 passes to the Power Amplifier assembly via J5-73 and the Mother assembly.

7.9.3.1 Action of VCA Drive Circuitry

If a user increases a positive OUTPUT display value, the positive DC Ref Hi voltage will increase (this is a demand to increase a positive output voltage). The polarity switch inverts the positive input from M15-7, so M15-1 feeds a negative output to M14. This is inverted at M14-1 and then buffered by voltage follower action at M14-7. It is passed via the Mother assembly to the DC modulator on the Power Amplifier assembly as an increasing positive DC signal.

In the case of an increasing negative OUTPUT display value, the negative DC Ref Hi value will increase negatively. But now the POSITIVE signal is at logic-Ø (-15V), so the output from M15-7 is not inverted and remains negative as for positive outputs. The action of M14 is not altered, so an increasing positive signal is sent to the DC modulator as before.

In both of the above cases the signal sent to the DC modulator is increasing positively, and this will result in an increasing 16kHz amplitude input to the 100V Amplifier. All polarity information is lost, so has to be re-inserted after rectification of the step-up transformer output, by the polarity switch in the High Voltage assembly.

7.9.4 DC MODULATOR

7.9.4.1 16kHz Derivation (Circuit Diagrams: 430648 page 11.3-2; 430652 page 11.4-5; 430618 pages 11.9-5 /11.9-2)

The 13-bit counter in the Analogue Interface generates 16kHz at pin 14 of M16 (page 11.3-2). This is transferred into guard through optoisolator M3 on the Reference Divider (page 11.4-5). The 16kHz square wave, switching between logic-1 = 0V and logic-Ø = -15V, enters the Power Amplifier assembly on J9-61 (page 11.9-5).

Providing the 1kV range is selected, and the 'PA CLAMP' signal is at logic-Ø (-15V), the full 15V p-p squarewave passes via M6-4 and M9-10 to inverter Q41 (page 11.9-2).

7.9.4.2 DC Error Signal Processing (Circuit Diagram 430618 page 11.9-2)

The modulator operates by alternately charging the low-pass filter formed by R83, C83 and C84 via the series switch Q39, and discharging it through Q40.

The 16kHz MOD DRIVE squarewave alternates between logic-1 (0V) and logic-Ø (-15V). After inversion in Q41, the signal at its collector switches between the +15V and -15V rails. Positive half-cycles of the MOD DRIVE signal make Q41 conduct, switching Q40 off and Q39 on, so the DC Error voltage charges the filter. For negative half-cycles the conditions are reversed and the filter is discharged to Common-2.

The DC Error signal is always positive, due to the polarity switch on the DC assembly. Its amplitude depends on the difference between the conditioned output voltage and the DC Ref Value, but is limited to +12V by D75.

The filter reduces the 32kHz and higher harmonic content of the squarewave, while passing 16kHz with little distortion. Its output is buffered by source-follower Q42, before being AC-coupled to the 100V Amplifier by a high pass filter (formed mainly by C86 with the approx. 400Ω input resistance of the amplifier).

The near-sinusoidal 16kHz signal input to the 100V Amplifier has amplitude which is proportional to the value of the DC Error signal, so acts as an AC analog of the difference between the normalized instrument DC output voltage and the value of the DC Ref voltage. It is based on a mean of 0V, and is passed as the '1kV ERROR O/P' signal via RL1-11/13 and RL2-6/4 into the Gain Stage of the 100V Amplifier (page 11.9-3).

7.9.5 100V AMPLIFIER

(Circuit Diagram 430618 page 11.9-3)

(For description refer to Subsections 7.8.3 and 7.8.4)

This operates as for the 100V range, but in this case the DC path simply maintains the zero offset of the AC signal, which is amplified along the AC path. The output signal 'OUTPUT' is fed from J3-9 to relay RL6 contacts (page 11.9-2) for application to the step-up transformer.

7.9.6 '1kV ENABLE' RELAY RL6

(Circuit Diagram 430618 page 11.9-2)

Relay RL6 allows the OUTPUT signal from the 100V Amplifier to energize the HF step-up transformer, providing the following conditions are met:

The $\overline{1kV}$ Signal is at Logic-0:

This is a processor-controlled signal, set to logic-0 when the instrument output is switched on, in the 1000V range.

The Watchdog has NOT 'Barked'.

The '1kV ENABLE' Switch S1 on the Power Amplifier assembly is set to 'ENABLE'.

S1 is situated below the left-hand ejector lever (viewed from the front of the instrument), facing the rear. It allows the high voltage to be switched off for servicing purposes. A red LED glows when all other conditions are met.

When RL6 is closed, the OUTPUT signal from the 100V Amplifier is switched through to the contacts of RL7.

7.9.7 LF/HF TRANSFORMER SELECTION

The two transformers are separately located, their secondaries being connected into the High Voltage assembly. The HF transformer is selected when RL7 is unenergized, its primary being returned to Common-2C. RL7 is energized to select the LF transformer.

For the 16kHz signal used with the 1000V DC Range, the HF transformer is selected by RL7 being unenergized.

7.9.8 HIGH VOLTAGE TRANSFORMER AND RECTIFIER

(Circuit Diagram No. 430537 page 11.14-1).

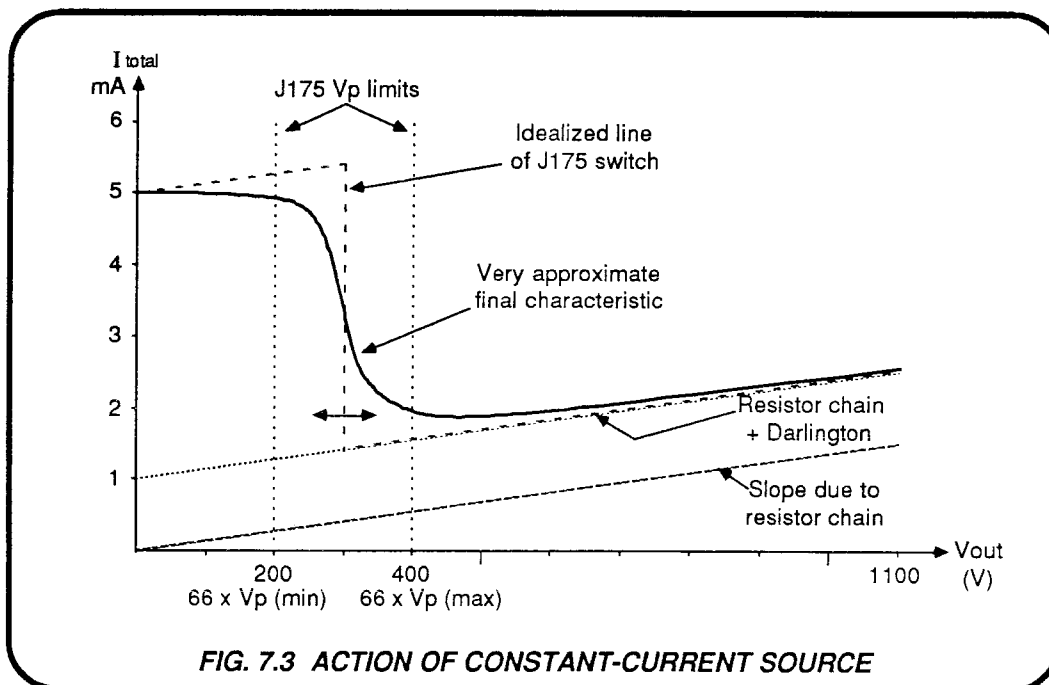
For the 1000V DC Range, the HF transformer gives a step up ratio of 1:6.17. This ratio generates secondary voltage outputs large enough to provide DC outputs from the instrument of 1100V. The AC relays RL2 and RL3 in the High Voltage assembly remain unenergized for the 1000V DC range, but the DC relay RL4 is energized, applying the HF transformer secondary voltage to the rectifier bridge via RL4-5/4 and RL4-2/3.

The rectifier bridge uses two series diodes in each arm. Each diode is current-rated at 1A, with a p.i.v. of 1.5kV.

N.B. The transformer secondary, and bridge rectifier are not directly referred to any common. This allows the rectifier output to float so that it may be used for either polarity.

7.9.9 CONSTANT-CURRENT ASSEMBLY

(Circuit Diagram 430563 page 11.14-2).



7.9.9.1 Constant-Current Source.

Q1-12 form a series Darlington chain, connected across the bridge rectifier output as a constant-current source, having two functions:

- It maintains conduction in diode bridge D56-D63 under no-load conditions.
- At higher voltages, D15-D17 limit Q11 base voltage to +2.4V, limiting the series current in R11, with Q13 pinched off. At lower voltages Q13 conducts, shunting R11 with 170-180 Ω (R10 plus Q13 'On' resistance which falls to approx 125 Ω), and increasing the discharge current. The approximate shape of the overall characteristic is shown in *Fig. 7.3*.

NB Note that the minimum voltage applied across the constant-current source is 38V. Even at zero output voltage and current, the diode bridge generates 38V to back off the positive or negative 38V connected to RL3.

7.9.9.2 Overvoltage Detection

Zener diodes D1 - D13 form a series chain across the High Voltage supply. When the voltage exceeds 1440V this chain conducts, lifting D13 cathode and driving opto-isolator M1. M1 collector falls, turning on Q14, whose collector voltage rises to provide a 'LIM DET' logic-1 (0V) output at pin 5. This signal travels from the High Voltage assembly at J1-14, via the Mother assembly, to the Power Amplifier assembly at J9-69.

The operation of the LIM DET circuitry and subsequent action is described in *Section 7.12*.

7.9.10 POLARITY SWITCHING

(Circuit Diagram 430537 *page 11.14-1*)

Double-pole relay RL5 performs the polarity-reversal. With RL5 un-energized as shown the output filter is connected to rectifier positive, and the -38V Common-2 supply is connected to rectifier negative. During zero calibration, the -38V is backed off to give a true zero output by an output from the rectifier.

Relay RL5 is controlled by the Exclusive-NOR gate M4-2, under the influence of the CPU's 'POSITIVE' and 'PA CLAMP ON' signals from the serial data-link parallel output registers. When negative outputs are selected, providing the PA is not clamped; RL5 is energized, the output filter is connected to rectifier negative, and the +38V Common-2 supply is connected to rectifier positive. Again, the +38V is backed off by an output from the rectifier for all negative outputs, including zero.

The requirements which decide the use of the Exclusive-NOR function are discussed in *sub-section 7.12.4*.

7.9.11 OUTPUT FILTERING

The high voltage output is filtered in three stages:

- a. L3, R1, C1 and C2 together form a 2-pole low-pass filter, which attenuates 16kHz by approx. 30dB and 32kHz by approx. 42dB.
- b. L4, L5 and their associated capacitors form a 5-pole filter with elliptical characteristics, attenuating by at least 60dB above 16kHz.
- c. The final stage is formed by R10, with C1, R84 and R85 on the Mother assembly (Circuit Diagram 430604 *page 11.16-1*). This provides further attenuation of approximately 30dB at 16kHz and 36dB at 32kHz.

7.9.12 1kV DC OVERCURRENT

The overcurrent detector on the DC assembly operates on the 1000V Range identically as on the 1V Range. Refer to *para 7.3.8.1*.

7.9.13 1kV and 100V SENSE ATTENUATION

(Circuit Diagram 430536 *page 11.5-1*)

Both ranges' output voltages are sensed on the SHI(DCV) line and reduced to 10V Range levels in the same guarded attenuator.

The 1000V Range output is developed across the full attenuator via relay RL7-8/9 contacts, and the guard chain is driven from the DC 1kV line via RL7-5/4.

The 100V output enters the attenuator at the tapping between R85 and R101 via RL8-9/8 contacts, the corresponding guard voltage being applied to the Guard chain via RL8-4/5.

The output tapping is common to both ranges, taken at the 900k Ω /100k Ω junction of R101. Thus the 1000V DC Range voltages are attenuated by 60:1, the 100V DC Range voltages by 10:1. The reduced output from the Sense attenuator is applied to the inverting input of the Error Amplifier.

Each junction between adjacent elements of the attenuator has its own guard screen. To eliminate leakage while providing an effective guard, a separate attenuator steps the power output voltage on the PHI(DCV) down to the correct voltage for each junction's guard screen.

The Sense attenuator sinks into Common-1, the 'reference' common to which the Error Amplifier and the 10V/1V attenuator are also referred. The guard attenuator sinks into Common-2, the general analog power common.

7.10 LOGIC CONTROL OF DC OUTPUTS

Two main aspects of analog control functions can be considered:

- a. The effects of the controls on the analog circuitry, which are discussed elsewhere in the descriptions of the relevant circuits;
- b. The methods of implementing the control logic, which have been developed to use the minimum number of control signals. It is also required to dissipate as little energy as possible inside the heat-shielding chassis assembly, to avoid temperature effects on the accuracy of the analog circuits themselves.

7.10.1 LOGIC LEVELS

In general, the analog control logic operates between 0V and -15V, with Logic-1 = 0V, and Logic-Ø = -15V. These levels are set originally at the serial/parallel control data latches in the Reference Divider assembly as outputs from the serial data link, and are accepted by the parallel/serial status data latches as inputs to the link back to the CPU. Some special control signals are passed into guard via opto-isolators, also in the Reference Divider, operating between -10V and -15V. These are subsequently adjusted to the normal control logic levels.

7.10.2 HEAT REDUCTION

Two methods are used to ensure that the energy dissipated by the relays is minimized:

- Use of bistable latching relays.
- Use of an 'Update' signal;

7.10.2.1 Update Considerations

For some heat-sensitive environments within the chassis assembly, polarized bistable latching relays are used which only require actuation, and hold on without a solenoid supply. Where relays need hold-on energization, they are usually tied to 0V or +15V on one side, and controlled on the other by the uncommitted collector of an inverting Darlington driver. Thus when the input to the driver is logic-1, the relay is held energized by its -15V output; and when the driver input is logic-Ø, its output is high impedance, releasing the relay.

For some relays it is necessary to hold the full actuating voltage across the solenoid for the whole time that it is energized. But where periodic updating will not cause difficulties, a relay is held on between 0V and -15V, raising the 0V side to +15V to actuate it during an update. Such relays have a secure hold-on voltage of approximately 12V, but require 20V or more to pull them in.

At intervals of 40ms (typically - depending on the priorities of the CPU's program), the CPU generates a data transfer across the serial interface, and an 'Update' signal is passed into guard by the CPU via an opto-isolator (M4 in the Reference Divider - *page 11.4-5*). This serves two purposes:

- It is mainly provided to ensure no delay in transferring important status data back to the CPU;
- It is available when it is required to update the analog state of the instrument functions, as demanded by reversionary modes or user inputs.

After passing into guard, the update signal is named 'UPD(IG)'

7.11 DC ASSEMBLY RELAY DRIVES AND LOGIC

7.11.1 INTRODUCTION

(Circuit Diagrams 430536 page 115-3
and 430668 page 7-23).

The analog circuitry is mainly controlled by low-thermal relays, many contacts being fitted back-to-back to further reduce temperature effects. For the fastest response, the output relay RL15 is not latched, but can trip out quickly if the power supply fails, removing any output voltage from the terminals.

The rest of the relays are latched, allowing hold-on without power, to reduce the internal temperature at their contacts. As they are polarized they require a bipolar actuating drive, which is provided by 'Tristate' relay drivers and a bias amplifier.

7.11.1.1 Latched Bistable Relays

(Circuit Diagram 430536 page 115-3).

As can be seen from the circuit diagram on page 115-3, the relays are strung out between the output of their bias amplifier (-7.5V approx. at M1-2) and the drive outputs from the Clamp assembly.

The bias amplifier M1 is a frequency-compensated voltage follower, buffering the tapping of attenuator R4/R5, to hold one side of each relay permanently at -7.5V. The relay drivers on the Clamp assembly can provide outputs at 0V or -15V when enabled by the $\overline{\text{UPD}}(\overline{\text{IG}})$ pulse, but return to tristate when disabled. A relay is therefore driven to one or the other of its bistable states during update, then latched in the chosen state when the driver output returns to open-circuit.

All the latched relays operate in the same polarity sense: when its driver output updates at logic-1 (0V), the relay latches to select its nominal function; for a logic-0 (-15V) update, the function is deselected. In the analog circuit diagrams, the relay contacts are shown in their deselected state, equivalent to the un-energized state of a conventional non-latching relay. For consistency, in the analog descriptions relays are referred to as being 'energized' or 'unenergized'.

7.11.1.2 'Tristate' Relay Drivers

(Circuit Diagram 430668 page 7-23).

The relay drivers (M1, M2, M3 on the Clamp assembly) are octal 'Tristate' buffers. Each chip is served by two inverted enable inputs on pins 1 and 19 (four buffers - half the chip - per enabling input).

Whenever a switching command has been received, the CPU performs a control data transfer and the $\overline{\text{UPD}}(\overline{\text{IG}})$ line from J5-104 is pulsed to -15V for 50ms.

The switching logic places a logic-1 (0V) on the input of selected drivers, and logic-0 (-15V) on those whose function is not selected. Because all the buffers are non-inverting, during the update pulse a driver selects its function by setting its output voltage to 0V, or deselected by pulling its output voltage to -15V.

7.11.2 CLAMP ASSEMBLY

(Circuit Diagrams 430536 page 115-3
and 430668 page 7-23).

On the DC Relay Drive Logic circuit diagram (page 115-3) the Clamp assembly is shown in block form. Also, the pcb pin numbers correspond to the pin numbers of the buffer chips: J7, J8 and J9 being the connections to M1, M2 and M3 respectively. For signals crossing the block from left to right, the output of each non-inverting buffer is drawn opposite its input, so the function remains unchanged as it crosses the block. As a further aid to identification, the pins of any one buffer are numbered so that the input and output numbers add up to 20.

7.11.2.1 $\overline{\text{UPD}}(\overline{\text{IG}})$ Distribution

As the $\overline{\text{UPD}}(\overline{\text{IG}})$ signal is distributed as the enable to many buffers, it is itself buffered before being fanned out. So the four $\overline{\text{UPD}}(\overline{\text{IG}})$ connections at the top of the block are inputs to four buffers (M1) which are permanently enabled by J7-19 at -15V. The outputs of two of these buffers are brought out to J7-5 and J7-7 which are not connected (and not shown on the circuit diagram).

The input at J7-11 emerges from the Clamp assembly at J7-9 to operate the driver for the non-latching relay RL15 (at M2-6). The fourth input at J7-17 emerges at J7-3, and is reconnected as the fanned-out enable to the other buffers on the assembly (see Fig. 7.4).

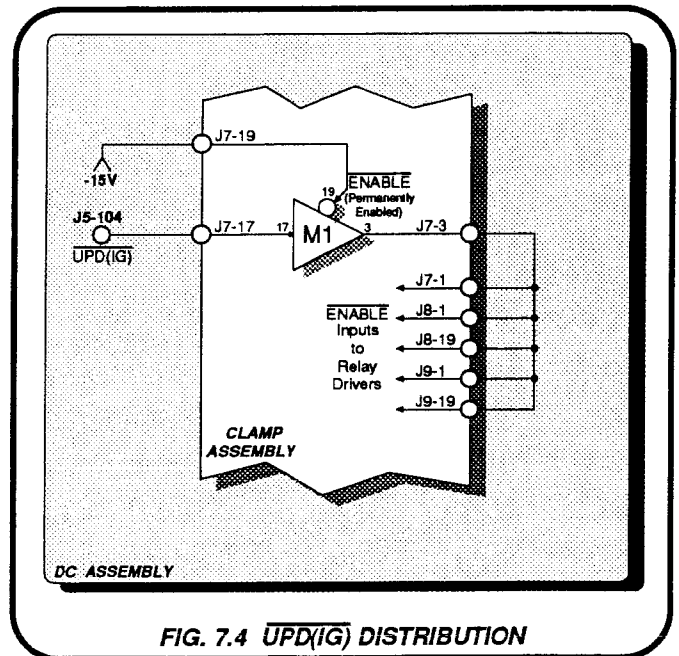


FIG. 7.4 $\overline{\text{UPD}}(\overline{\text{IG}})$ DISTRIBUTION

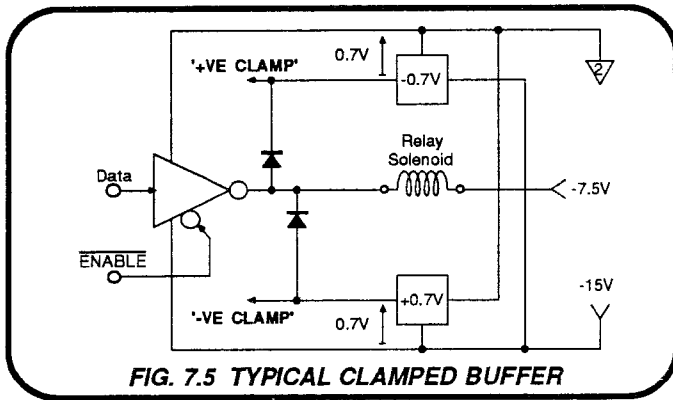
7.11.2.2 Buffer Clamping

(Circuit Diagram 430668 page 7-23).

The 40244 octal buffer can be sourced from several manufacturers. Some variants are protected against SCR avalanche if the output voltage were to exceed the rail voltage, but some are not. Each buffer drives its output into the solenoid of a relay, and is switched on and off by the update enable. The self-inductance of the solenoid can generate back EMF's well in excess of the rail voltage, so to guard against the possibility of catastrophic failure, it was decided to provide external protection in the form of a clamp circuit.

On the Clamp assembly Q1-Q4 form two power supplies, each delivering a regulated voltage of a diode-drop less than the rail voltage ('+VE CLAMP' and '-VE CLAMP'). A diode connected from the buffer output to each of the clamp lines permits the output voltage to rise to, but not exceed, the rail voltage (see Fig. 7.5).

Where two buffers are used in parallel to drive two relays, the clamp diodes can be omitted from one buffer output (eg. M2-9 and M2-7 are joined on the DC assembly between J8-9 and J8-7, so both are clamped).



7.11.3 DC ASSEMBLY SWITCHING LOGIC

(Circuit Diagram 430536 page 11.5-3).

The analog-control signals are transferred into guard on the Reference Divider assembly, and latched as 'Q' outputs in the Serial/Parallel Data Converter. Offset positive logic is employed (Logic-0 = -15V, Logic-1 = 0V) for the signals entering the DC assembly via J5 from the Mother assembly. For general analog control considerations refer to Sect. 7.10.

7.11.3.1 Range Switching Logic

Range control data is input as a 3-bit code on DCR0, DCR1 and DCR2 lines. The bit-pattern is decoded by M4 to select the correct range relays. As the 100µV, 1mV, 10mV and 100mV ranges all use the same analog circuitry, only one bit-combination (DCR2) is required for these four ranges. The resulting five combination variations are listed in Table 4.1 against the range selections, showing the states of M6 'Q' output pins and the relays energized for each range.

Note that deselection of DC function sets each DCR(2-0) to logic-1. The M6 'Q' outputs all fall to logic-0, deselecting all range relays except RL1, RL2, RL3 and RL16, which are selected by DCR2 being at logic-1.

7.11.3.2 Function and Output Switching Logic

Output voltages are passed through the DC assembly on all AC and DC ranges. RL15 connects the SHi, SLo, PHi and PLo to the Hi, Lo, I+ and I- terminals of the instrument. Four signals control this relay:

- OFF at logic-0 when Output is selected ON.
- BARK DEL at logic-0 unless the watchdog has tripped.
- AC FUNCT at logic-0 if AC Function is selected, or
- DC FUNCT at logic-1 if DC Function is selected.

Under these conditions M4 pins 1 and 2 are set to logic-1, M4-9 is at logic-0; M4 pins 3, 4 and 5 are at logic-0, M4-6 is at logic-1. So M2-2 is driven positive, and as M2-3 is biased at about -4.75V, then M2-1 goes to approx. -12V. During the update pulse J7-9 goes to -15V, so M2-7 goes to +15V. RL15 is thus actuated by some 27V, but after the UPD(IG) pulse is terminated, M2-7 returns to 0V and RL15 is held on. If AC and DC are both deselected, or if the output is set to OFF, or if the Watchdog barks; the -12V at M2-1 reverts to approx. +11.5V. If the UPD(IG) pulse is not present, the voltage across RL15 falls through zero and RL15 is de-energized. If it is present, only approx. 4.5V is connected across RL15, which is insufficient to hold the relay on. Under these conditions the instrument terminals are disconnected from the output.

Relays RL10 and RL18 are selected when DC voltage has been commanded, providing that the Watchdog has not barked. With DC FNCT at logic-1, M4-11/13 are at logic-0. If the Watchdog has not barked then BARK DEL is logic-0 at M14-12. As a result of both these conditions, M4-10 is at logic-1 and both relays RL10 and RL18 are selected. RL10 connects the PHI(DCV) and SHI(DCV) line to the PHI(V) and SHI(V) lines respectively, RL18 connects the DC Ref output from the Reference Divider to the DC Error Amplifier input.

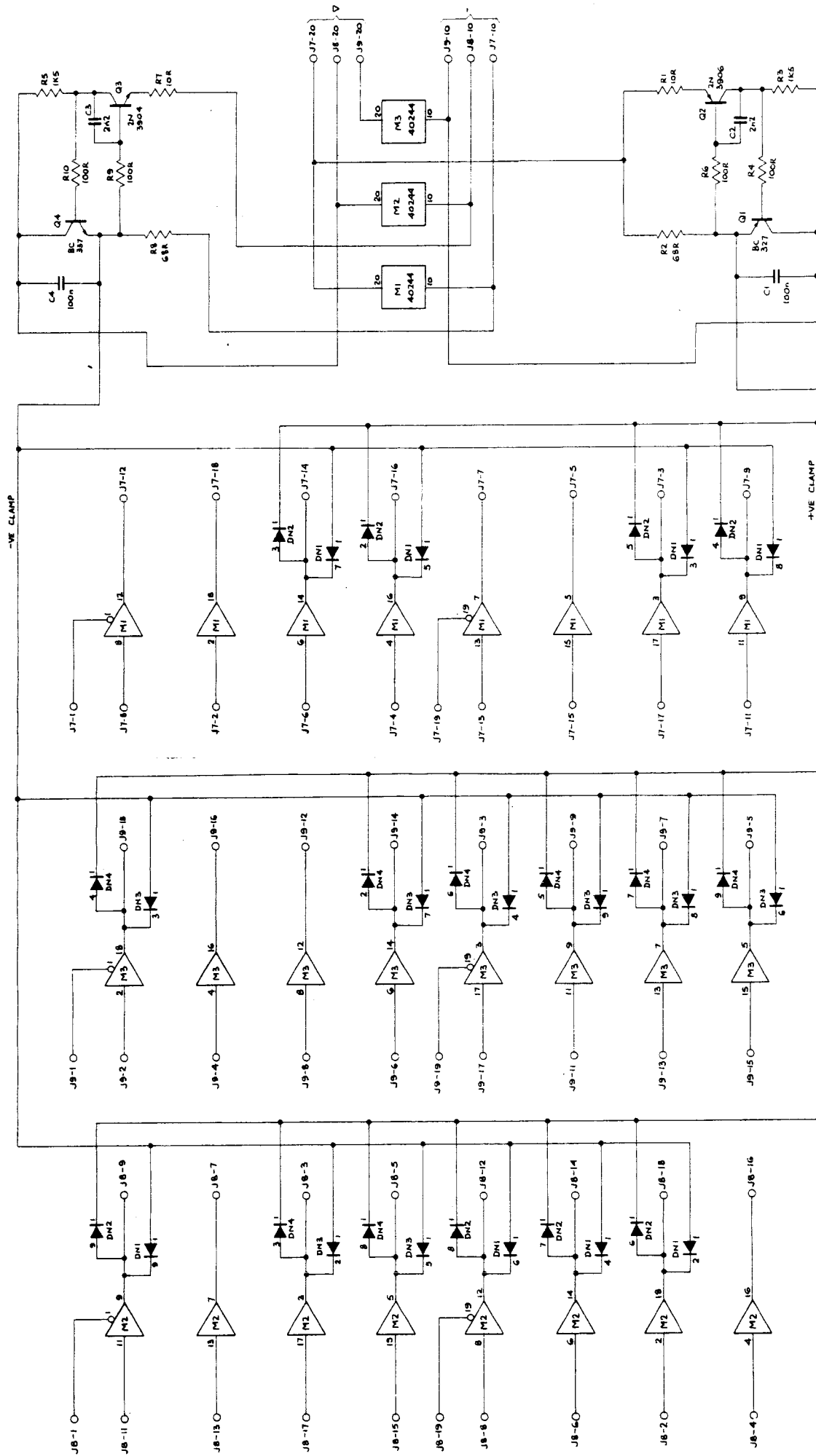
Relay RL11 connects the power and sense Lo lines back to their respective commons. Thus when RL10 and RL18 are selected for DC voltage outputs, so is RL11. But in Current Function it is also required to tie the Local Guard to Common-2. This also is done by selecting RL11. With Current Function selected, the IFNCT signal is at logic-0 so M3-13 is at logic-1 and RL11 is selected.

The Remote Sense Relay RL14 is also selected by the IFNCT signal, as well as by the front panel selection of remote sense. These are combined at OR-gate M10-3, before selecting RL14 directly via its buffer. RL14 removes the local sense short between the power and sense lines at both Hi and Lo signal levels. For Current Function this has negligible effect on the DC assembly, but the REM SENSE '+' and '-' signals are also passed out to RL1 on the Mother assembly (page 11.16-1). Although remote sense is not selectable for DC or AC Current ranges, it is necessary to route the current output to the I+ and I- terminals on the front panel. RL1 on the Mother assembly is energized to do this. (For Local Sense on voltage ranges, RL1 routes the power Hi line to the Hi terminal instead of I+).

REM GU selects the Remote Guard relay RL17 via its buffer.

The HIGH LIMIT and AC 1kV RANGE signals are concerned with the AC 1kV Overcurrent Detector circuit. The signals operate their relays RL12 and RL13 directly through their buffers. Section 9 discusses their effects. The effects of control signals '1kVDC', '100VDC', 'DC FNCT' and 'POSITIVE' are discussed in the descriptions of the analog circuitry at their destinations.

DN1 AND DN3 ARE CA-IN414B
 DN2 AND DN4 ARE CC-IN414B



DC CLAMP CIRCUIT Drawing 430668

7.12 PA ASSEMBLY LOGIC AND RELAY DRIVES

(Circuit Diagrams 430618 Pages 11.9-4 and 11.9-5)

The CMOS logic operates between the levels 0V and -15V, with logic-1 = 0V, and logic-0 = -15V. Relays are tied to +15V on one side, and controlled on the other by the uncommitted collector of an inverting Darlington driver. Thus when the input to the driver is logic-1, the relay is energized by 15V; and when the driver input is logic-0, its output is high impedance, releasing the relay.

7.12.1 DC RANGE SWITCHING

(Page 11.9-5)

The three inputs DCR0, DCR1 and DCR2 carry the DC range switching information, and are decoded by M7a as follows:

| Range Select | M7a inputs | | | M7a outputs | | |
|--------------|------------|------|------|-------------|----|----|
| | E | B | A | Q2 | Q1 | Q0 |
| | DCR2 | DCR1 | DCR0 | | | |
| 1000V | 0 | 0 | 0 | 0 | 0 | 1 |
| 100V | 0 | 0 | 1 | 0 | 1 | 0 |
| 10V | 0 | 1 | 0 | 1 | 0 | 0 |
| 1V | 0 | 1 | 1 | 0 | 0 | 0 |
| 100mV | 1 | 0 | 0 | 0 | 0 | 0 |
| 10mV | 1 | 0 | 0 | 0 | 0 | 0 |
| 1mV | 1 | 0 | 0 | 0 | 0 | 0 |
| 100µV | 1 | 0 | 0 | 0 | 0 | 0 |
| Deselect DC | 1 | 1 | 1 | 0 | 0 | 0 |

7.12.2 AC RANGE SWITCHING

(Page 11.9-5)

The three inputs ACR0, ACR1 and ACR2 carry the AC range switching information, and are decoded by M7b as follows:

| Range Select | M7b inputs | | | M7b outputs | | |
|--------------|------------|------|------|-------------|----|----|
| | E | B | A | Q2 | Q1 | Q0 |
| | ACR2 | ACR1 | ACR0 | | | |
| 1000V | 0 | 0 | 0 | 0 | 0 | 1 |
| 100V | 0 | 0 | 1 | 0 | 1 | 0 |
| 10V | 0 | 1 | 0 | 1 | 0 | 0 |
| 1V | 0 | 1 | 1 | 0 | 0 | 0 |
| 100mV | 1 | 0 | 0 | 0 | 0 | 0 |
| 10mV | 1 | 0 | 1 | 0 | 0 | 0 |
| 1mV | 1 | 1 | 0 | 0 | 0 | 0 |

7.12.3 FUNCTION AND RANGING LOGIC

DCV Logic

When un-energized, relay RL4 selects the DC ERROR signal in preference to the AC 1V signal, as input to the Power Amplifier when DC Voltage function is selected. When un-energized, Relay RL8 reduces the permissible overload on the output of the 10V Amplifier, also when DC Voltage is selected.

When 'DC' is selected on the front panel, both DC FNCT (J9-70) and $\overline{\text{I FNCT}}$ (J9-72) signals are at logic-1. Under these conditions both inputs to NAND M6-12/13 are at logic-1, so M6-11 is at logic-0 and both relays RL4 and RL8 are un-energized. For all other function selections DC FNCT is at logic-0, so M6-11 is at logic-1 to energize both relays.

AC & DC 10V Range Logic

On the DC 10V Range only, the input to M6-1 is logic-0; and on the AC 10V Range only, the input to M6-2 is logic-0. Logic-1 occurs at M6-3 to operate relay RL3 only when either the AC or DC 10V range is commanded.

AC & DC 100V Range Logic

The input to Q12-8 is logic-1 only when the DC 100V range is selected, and the input to Q12-9 is logic-1 only on the AC 100V range. Either input gives logic-1 at M12-10, so relay RL2 operates only when either the AC or DC 100V range is commanded.

AC 100V Range Logic

A '100V AC' signal is also passed to activate the 100V Current Sense circuit (see page 11.9-6), only on the AC 100V Range.

DC 100V Range Logic

The decoded DC 100V Range signal at M7a-5 is also connected to the cathode of D31. On other ranges the diode conducts to pull the DC INPUT CLAMP signal to logic-0 (Off), but on the DC 100V Range D31 releases the line so that the PA CLAMP ON signal can set it to logic-1 (On).

AC & DC 1000V Range Logic

The 1kV signal enters the Power Amplifier at J9-32. It is at logic-0 only when AC or DC 1000V Range is commanded by the CPU, with the OUTPUT set ON. 'BARK' enters at J9-66, and is at logic-0 only if the watchdog has not detected a failure (see Sect. 6). With both inputs to M4-8/9 at logic-0 the output at M4-10 is logic-1 which lights the internal warning LED D70. Relay RL6 is energized if the internal 1kV ENABLE switch on the PA assembly is set to its normal operating position of ENABLE. This allows the AC drive to be passed to the step-up transformers (16kHz signal in the case of the DC 1kV Range, to the HF transformer).

For other ranges, or if the watchdog barks, RL6 is de-energized, removing the AC drive to the step-up transformers. LED D70 is also de-energized.

AC 1000V Range Logic

The input to M13-3 is logic-1 to energize relay RL1 only when the AC 1000V range is commanded. A 'AC 1kV RANGE' signal is also passed to the DC assembly to select the overload sense resistor.

DC 1000V Range Logic

Although the combination of the universal 1kV Range signal and the AC 1kV signal is used to define the DC 1kV circuitry, two extra facilities are required for the DC 1kV Range. The 16kHz REF FREQ signal has to be switched to the DC modulator. For negative outputs on the 100V Range the 100V Amplifier positive rail is reduced to +38V instead of the +400V supply, so this has to be restored to +400V for the AC signals on the 1kV Range. For these applications the decoded DC 1kV Range signal at M7a-4 is used as input to M4-6 and M6-6.

The REF FREQ signal enters at J9-61 and is enabled at M6-5 by the 1kV Range decode on M6-6. Provided that the PA CLAMP ON signal is Off (ie. at logic-Ø), the 16kHz 'MOD DRIVE' signal is passed to the 1kV DC Modulator (*see page 11.9-2*).

The POSITIVE signal entering at J9-41 is input to M4-5 and the 1kV Range decode is input to M4-6. If a negative output on the 100V Range is commanded, then both inputs are at logic-Ø. The output at M4-4 is logic-1 and M15 causes the LED in M16 to conduct by pulling M16-3 to logic-Ø. The photo-transistor of M16 conducts (*see page 11.9-3*), placing a short circuit between the source and gate of Q20, which turns off the +400V supply to the 100V Amplifier driver stage. Q9 conduction causes D56 to conduct, so for negative outputs on the 100V Range the positive rail for the driver is sourced from the +38V supply.

On the DC 1kV Range the +400V supply is required to deal with the AC signal being amplified, so M4-6 at logic-1 inhibits the disabling photo-coupler; M13-15 being open-collector. The same inhibition results for positive outputs on the DC 100V Range (when the +400V is needed to power the driver stage) by M4-5 at logic-1.

7.12.4 'PA CLAMP ON' SIGNAL

PA CLAMP ON is applied before the 1kV DC control loop is broken by the 1kV line, and released when the loop is restored. It is also required on entry into and exit from the 100V DC Range. Other ranges are 'don't care' states.

7.12.4.1 DC 1000V Range Clamp

When the DC 1000V Range is selected, but Output is set Off, the drive is removed from the input to the step-up transformer. The High Voltage assembly polarity relay RL5, in the positive position, connects -38V to the base of the Constant Current chain at Pin 2. The other end of the chain is connected, via the instrument output lines, to the head of the 1kV sense attenuator on the DC assembly. The attenuator output is fed to the inverting input of the Error Amplifier.

Under these conditions, the Error Amplifier 'sees' a negative voltage at the Output terminals, and would drive heavily into saturation on its positive side to correct the output. This would occur regardless of the size of the positive DC Ref voltage being applied on its non-inverting input. When the positive Output was reset to On, the power circuitry could generate a massive swing which would result in catastrophic failure. A similar (but polarity-reversed) effect could be present for negative DC Output selections.

This excess loop gain is removed by reversing the position of the polarity switch during the time that the output is turned off, so that the Error Amplifier sees a positive voltage and backs off toward zero. The logic to reverse the polarity is driven by the PA CLAMP ON and POSITIVE signals, employing an exclusive-NOR gate.

In the High Voltage assembly, M2-4 feeds the driver for the polarity changeover relay RL5. The inputs at M4-5 and M4-6 are POSITIVE and PA CLAMP ON respectively.

The required reversal conditions are satisfied as shown:

| Selected Commands | 'POSITIVE' | PA CLAMP ON | M2-4 State | RL5 State | Nominal Output Polarity |
|-------------------|------------|-------------|------------|--------------|-------------------------|
| -VE-O/P ON | Ø | Ø | 1 | Energized | -ve |
| -VE-O/P OFF | Ø | 1 | Ø | Un-energized | +ve |
| +VE-O/P ON | 1 | Ø | Ø | Un-energized | +ve |
| +VE-O/P OFF | 1 | 1 | 1 | Energized | -ve |

The PA CLAMP ON signal at logic-1 also disables the 16kHz MOD DRIVE signal to the DC Modulator.

7.12.5 '400V ENABLE' LOGIC

The '400V(2) OFF' signal from the CPU is normally at logic-Ø for voltage ranges; but after a 'FAIL 7' message indicates a 400V supply failure, it is toggled three times, attempting to restore the supply.

Thus in normal operation, BARK is logic-Ø and the PSI OFF signal from M11-4, also logic-Ø, is input to M1-1/6 (*page 11.9-4*). M1 consists of six inverting drivers, each with uncommitted-collector output (as used for the relay drivers). M1-1 at logic-Ø allows M1-2 to be pulled to logic-1 by AN1-1/2, or to logic-Ø by M1-14. In the lower chain with four inversions, M1-14 is also open-collector, if a 400V or 15V failure has not been detected by the monitors.

Thus for normal operation M1-2 is pulled to logic-1 and the 'ENABLE 400V-' line from M1-15 is held at logic-Ø (-15V). With the 'ENABLE 400V+' line it energizes the opto-isolator LEDs in the 400V power supply (PS/I heatsink *page 11.13-3*).

A failure of either the 400V or 15V supply pulls M1-3 to logic-1, disabling the 400V supply by setting the ENABLE 400V- line to logic-1. If the +15V or -15V rail collapses, the opto-isolator current is cut off in any case, due to zener D24.

7.12.6 'BIAS OFF' LOGIC

On the 100V or 1000V ranges, after receiving a 400V FAIL signal from the monitor, the CPU attempts three times to restore the 400V supply. The foldback current limiting for the supply (in the PS/I heatsink) prevents reinstatement if an overload persists. Thus it is necessary to remove the overload if the supply is to be restored. This is done by setting the BIAS OFF line to logic-Ø (-15V), cutting off Q10 (*page 11.9-3*) and removing the output drive.

The three attempts are made by toggling the 400V(2) OFF line (described in *sub-section 7.12.5*). Each time the supply is enabled, R6 and C1 hold the BIAS OFF signal at logic-Ø for about 1ms to allow the supply to build up before the load is reapplied.

After three unsuccessful attempts, the CPU assumes a permanent hardware fault and holds the 400V(2) OFF signal at logic-1.

7.12.7 'LIM ST' LOGIC

This status signal is passed back to the CPU via the SSDA serial link to indicate that certain limits have been exceeded. The $\overline{\text{LIM ST}}$ signal entering the Reference Divider at J4-76 (page 114-4) can be activated to logic-0 by any one of nine detectors, as illustrated in the simplified diagram of Fig. 7.6.

7.12.7.1 'LIM DET'

The $\overline{\text{LIM DET}}$ signal output from the Power Amplifier at J9-67 (page 119-5) can result from the LIM DET signal setting the latch M5a. LIM DET is associated with the high voltage ranges, and can be activated by:

- DC Assembly (page 115-1/2)
AC 1kV Overcurrent Detector,
DC Overcurrent Detector (100V & 1000V DC ranges);
- High Voltage Assembly (Constant Current Source)
DC 1kV Overvoltage Detector;
- Power Amplifier Assembly
AC 100V Overcurrent Detector,
AC 1000V Overvoltage Detector.
(These two combine to generate the $\overline{100V \text{ FLAG}}$, which is NORed with 'DC FNCT' before becoming LIM DET.)

$\overline{\text{NOT100V FLAG}}$ is initiated by the AC 100V Overload Detector or AC 1000V Overvoltage Detector (page 119-6), whenever the 400V supply current peaks are excessive, or the AC 1kV Range drive voltage to the primary of the step-up transformer is excessive.

The LIM DET logic-1 is immediately transferred via M12-3 as the signal I LIM 100V AMP to the gate of Q14 (page 119-3). Q14 conduction reduces the 100V amplifier input to zero, so if the overload is external the LIM DET signal should revert to logic-0.

7.12.7.2 'LIM ST' Generation

The latch M5a is set by logic-1 on pin 6, for as long as LIM DET remains at logic-1. Its 'Q' output activates the $\overline{\text{LIM ST}}$ signal via M4-3, informing the CPU. It also reinforces and latches the 'LIM 100V AMP' signal. $\overline{\text{LIM ST}}$ is also activated if the overload signal 10V FLAG from the 10V Amplifier is at logic-0 when in AC 10V Range.

Other detectors which can provide the $\overline{\text{LIM ST}}$ signal are:

- DC Assembly (page 115-1/2)
DC Overcurrent Detector (1V & 10V DC ranges);
- Sine-Source Assembly (Constant Current Source)
AC 1V Buffer Overcurrent Detector;
- Current/Ohms Assembly
DC and AC Current ranges Overvoltage Detector

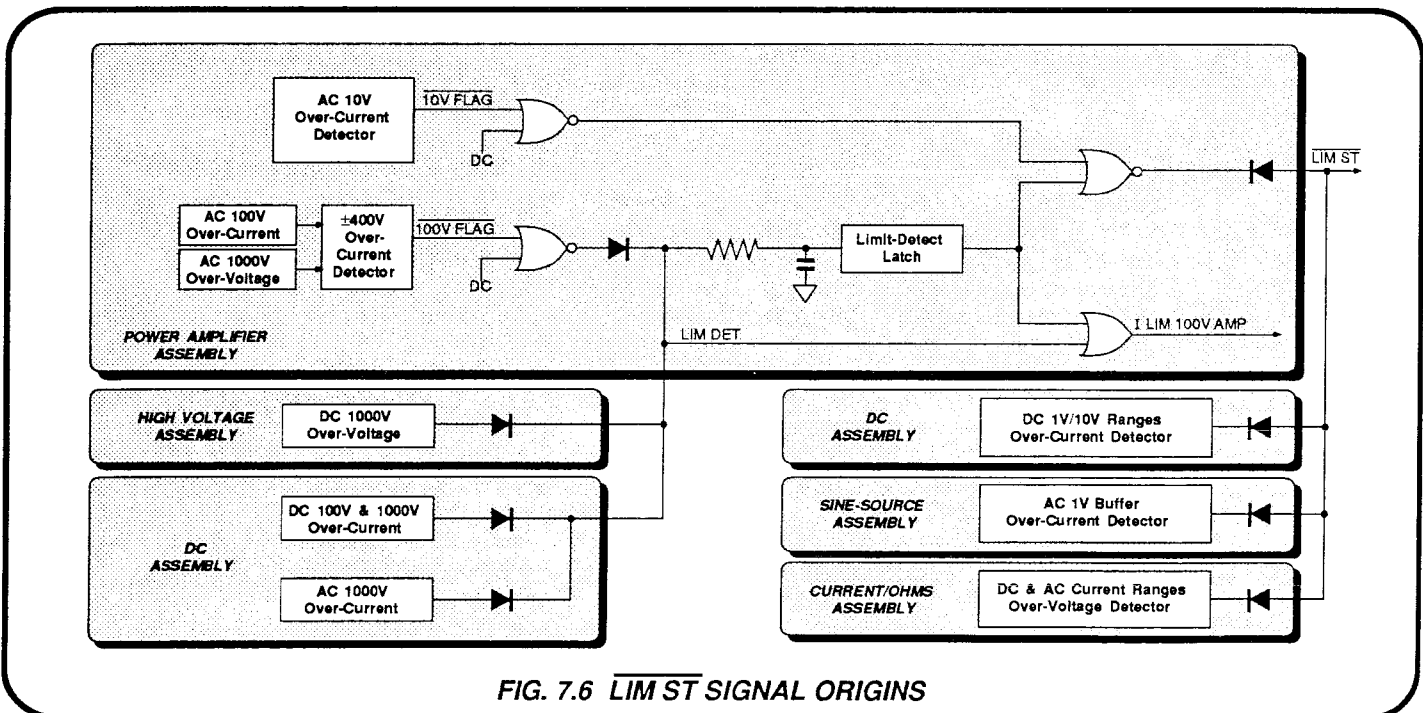


FIG. 7.6 $\overline{\text{LIM ST}}$ SIGNAL ORIGINS

7.12.7.3 CPU Response

On receipt of the $\overline{\text{LIM ST}}$ signal, the CPU initiates a series of clock pulses on the 'LIM RST' line via the SSDA and Reference Divider, so that M5a can be reset as soon as the LIM DET signal clears to logic-0, M5a 'D' input being strapped to logic-0 (-15V). The CPU also displays the 'Error OL' message.

If the LIM DET line has cleared to logic-0, the 100V Amplifier input is reinstated by M5a being reset. Furthermore, if the overload was temporary, the LIM DET line remains at logic-0, and normal operation resumes. The CPU is informed by $\overline{\text{LIM ST}}$ at logic-1, so the I LIM RST pulses are discontinued, and the Error message is removed.

For a persistent overload, the detectors operate once again. The cycle repeats until user action is taken to remove the overload. The Error message continues to be displayed.

If the overload is an internal fault, it is likely that another protection circuit will have detected it and taken its own action.

7.12.8 'LF', $\overline{\text{LF}}$ and '1kV GAIN'

These are signals used to control the gain and compensation of the AC 1kV amplifiers, (*Refer to section 9.?*).

The 'LF' signal is set to logic-1 by the CPU via the SSDA serial link and Reference Divider latches, when the AC 1000V range and the 100Hz or 1kHz frequency ranges are selected. It is inverted as $\overline{\text{LF}}$ at M11-12, and then inverted as buffered 'LF' at M11-10.

'FREQ R0' is also CPU-controlled. It is set to logic-1 when either the 1kHz or 100kHz frequency range is selected.

$\overline{\text{LF}}$ and 'FREQ R0' are combined at M6-10 to give the '1kV GAIN' signal, which is at logic-0 only when the 100kHz range is selected. (The software prevents the 1MHz range being selected on the 1000V range).

7.12.9 THERMISTOR COMPARATOR

Two NTC thermistors situated in different positions on each PA heatsink are part of a bridge network which detects excessive temperatures on the heatsinks.
(*Para 7.8.4.3 and pages 11.13-1/2 refer.*)

The reference arm of the bridge is formed by R165 and AN9-7/10 in parallel, both in series with AN9-6/11.

The sense arm has four parallel sections, each consisting of one section of AN9 in series with one of the NTC thermistors. Four null detectors are used (M22 and M23), each comparing the voltage at the reference arm junction with that at the junction of one of the sections (TEMP +R/-R/+F/-F).

At 25°C each thermistor resistance is 10kΩ. The bridge is unbalanced in favour of open-collector outputs from the four comparators, pulled up to Common-2 by AN2-3/4 and AN2-5/6. Q36 is therefore cut off, and the 'OVERTEMP' signal at J9-31 is at logic-0 (-15V).

If one of the chip temperatures exceeds 100°C, its thermistor resistance falls to the extent that the bias on its null detector is reversed. The null detector output is taken low to -15V, Q36 conducts and the OVERTEMP signal goes to logic-1.

The OVERTEMP status signal is passed to one of the Reference Divider status registers, (*page 11.4-4*), where for safety reasons it is pulled-up by a 1MΩ section of AN2. The CPU reacts to the logic-0 signal by displaying the 'FAIL 1' message, and forcing a recovery sequence:

OUTPUT OFF;

- Reference Divider ramp to zero;
- Remote Sense OFF;
- Analog Control 'OFF' bit set;
- Analog Control '1kV' line disabled;
- Display and Keyboard locked;

After approximately 1 minute, the CPU defaults the instrument to the normal 'OUTPUT OFF' state in the selected ranges with output set to zero. The FAIL 1 message is removed, and the user is at liberty to try another attempt.

Under normal power-up conditions, with the Power Amplifier assembly plugged in and Q36 cut off, AN2-7/8 holds the line more negative than -14V (logic-0). If the Power Amplifier is removed, no over-temperature information is available from the heatsinks. In this event, the OVERTEMP signal rises to logic-1, indicating failure.

SECTION 8 AC VOLTAGE OUTPUTS - FREQUENCY CONTROL SYSTEM

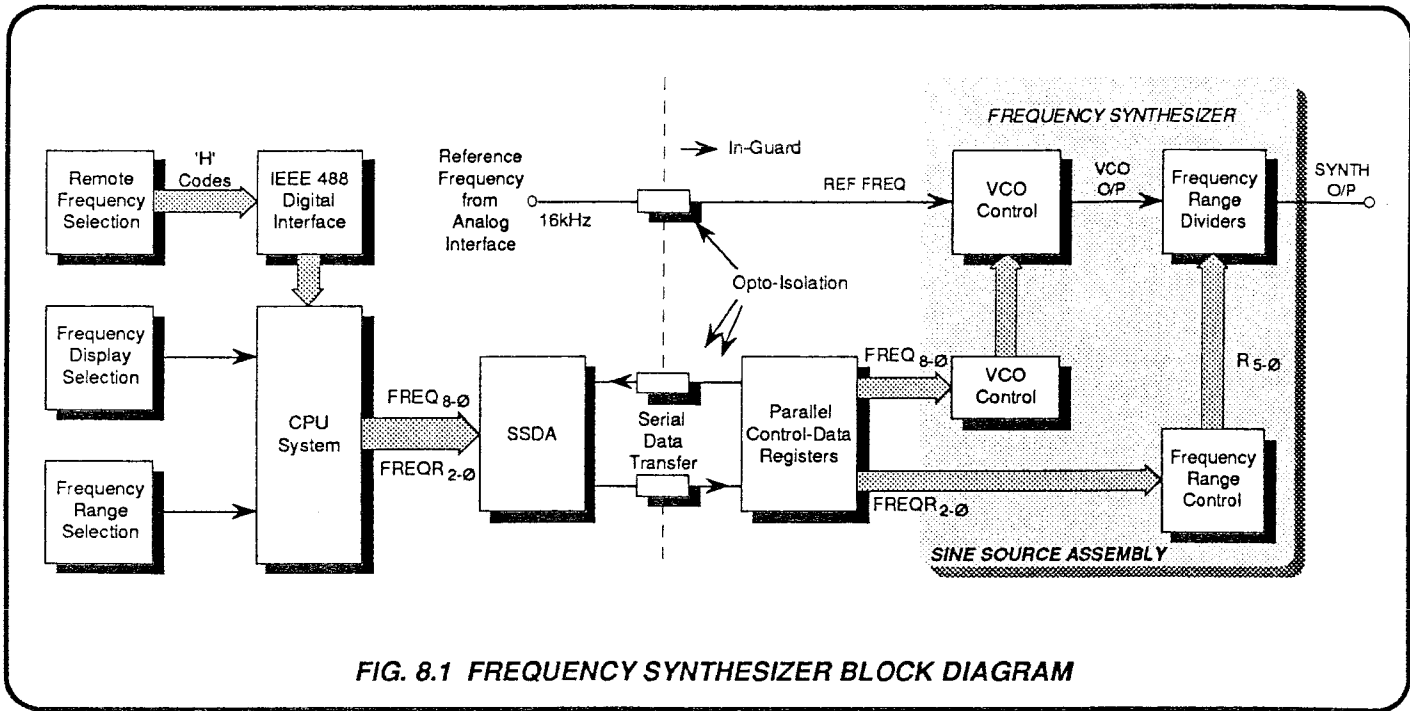


FIG. 8.1 FREQUENCY SYNTHESIZER BLOCK DIAGRAM

8.1 DIGITAL FREQUENCY SYNTHESIZER

(Fig. 8.1)

8.1.1 GENERAL

Users normally set the operating frequency by a combination of 'FREQUENCY RANGE' and 'FREQUENCY' display selections. These are memorized by the CPU and translated into two binary control words:

' $FREQ_{2-\theta}$ '

A three-bit word, five of whose codes represent the five frequency ranges.

' $FREQ_{8-\theta}$ '

A nine-bit word whose value 'n' defines the chosen frequency with respect to the selected frequency range.

Users can select a frequency by means other than pressing a FREQUENCY RANGE key and setting a frequency on the display; for example by using 'Store' or the IEEE 488 digital interface. But regardless of the selection method, the CPU will always compute the two binary words, which then synthesize the selected frequency in the Sine-Source Assembly.

Both words are passed into guard via the SSDA, and latched at the outputs of the Reference Divider Parallel Control registers. A 16kHz reference frequency is also taken into guard, to be divided by two to 8kHz in the Sine-Source assembly.

After entering the Sine-Source assembly, $FREQ_{8-\theta}$ effectively multiplies the 8kHz reference by a factor 'n' to determine the frequency of a Voltage Controlled Oscillator (VCO). The VCO frequency (signal 'VCO O/P') is input into a series of frequency dividers, whose ratios are set by $FREQ_{2-\theta}$. The division ratios are chosen to make the dividers generate the Frequency Synthesizer output signal ('SYNTH O/P') at the user-selected frequency.

The purpose of the synthesizer is to provide an accurate frequency reference for the quadrature sinewave oscillator. The oscillator is approximately tuned by selection of circuit constants using the combination of ' $FREQ_{2-\theta}$ ' and ' $FREQ_{8-\theta}$ '.

'SYNTH O/P' acts as the reference in the phase comparator of a Phase-Locked Loop, controlling the frequency of the main Quadrature Sinewave Oscillator to an accuracy determined by the crystal oscillator.

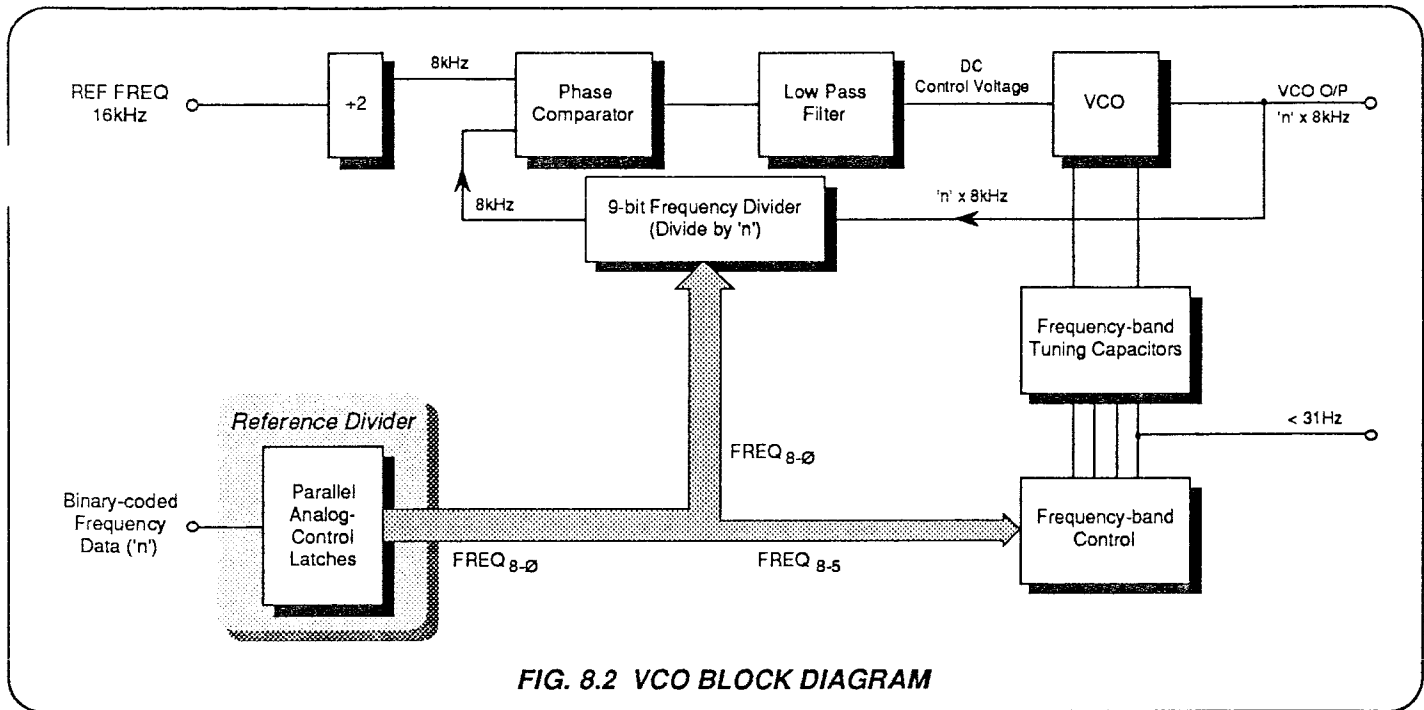


FIG. 8.2 VCO BLOCK DIAGRAM

8.1.2.1 Generation of 16kHz Reference

(Circuit Diagrams 430648 page 11.3-2, 430652 page 11.4-5 and 430446 page 11.6-4)

The 16kHz (INT) signal originates at M16-14 in the Analog Interface (page 11.3-2) and is buffered as '16kHz(OG)' (page 11.3-1). On the Reference Divider at J4-104, it passes into guard via opto-isolator M3 (page 11.4-5), gating with 'DISABLE REF FREQUENCY' and 'BARK' M24, filtered by R86/C38 to reduce harmonics from the transmission path, and is sent via the Mother Assembly to J6-53 on the Sine-Source Assembly (page 11.6-4).

Schmitt-trigger M14 inverts the 16kHz into an asymmetrical squarewave, which is then applied as clock to M13a, a bistable connected to divide by two. The resulting 8kHz squarewave is applied to the REF input of the phase comparator M12 as the reference frequency, and the divided VCO output signal is applied to M12 SIG input. This provides the correct sense for phase control of the VCO in the phase-locked loop.

8.1.2.2 Squarewave Generation by the VCO

The VCO is an integrated relaxation oscillator generating an output of frequency ' $n \times 8\text{kHz}$ '. Its natural frequency is dependent on:

- the value of capacitor C5 (or C5 plus one of C1 - C4),
- the value of its control voltage from the phase control element (phase comparator M12), and
- the value of the charging current for capacitors C1-C5, M11 pins 6-7 on alternate half cycles.

8.1.2.3 Coarse Frequency Control

(Circuit Diagram 430446 Page 11.6-4, and Fig. 8.2)

At any time, only one of the capacitors C1, C2, C3 and C4 can be connected in parallel with C5, by conduction of its associated JFET. This splits the frequency range of the VCO into five bands, governed by the four most-significant bits of the control word FREQ_{8-0} acting on M8. The association is shown in Table 8.1; note that the VCO frequency bands quoted in the table are correct only because the VCO is under the fine control of comparator M12, within the phase-locked loop.

| FREQ ₉₋₅ bits | | | | Range of 'n' Values | M8 Outputs at Logic-1 | C1-C5 Selection | VCO Frequency Band (kHz) |
|--------------------------|---|---|---|---------------------|-----------------------|-----------------|--------------------------|
| 8 | 7 | 6 | 5 | | | | |
| 0 | 0 | 0 | 0 | 10 to 31 | X ₀ | C5 and C4 | 80 to 248 |
| 0 | 0 | 0 | 1 | 32 to 63 | X ₁ | C5 and C3 | 256 to 504 |
| 0 | 0 | 1 | X | 64 to 127 | X _{3,2} | C5 and C2 | 512 to 1016 |
| 0 | 1 | X | X | 128 to 255 | X _{7,4} | C5 and C1 | 1024 to 2040 |
| 1 | X | X | X | 256 to 500 | NONE | C5 only | 2048 to 4000 |

TABLE 8.1 COARSE FREQUENCY CONTROL

8.1.2.4 Fine Frequency Control

(Circuit Diagram 430446 Page 11.6-4, and Fig. 8.2)

In the following description, capacitors C1, C2, C3 and C4 are ignored, but references to C5 should be read as including the appropriate additional capacitor.

The VCO output is fed back to M12 phase comparator via M9 and M13b, which are connected to act as a 9-bit frequency divider. Because the divider is controlled by FREQ₄₋₀, the VCO output frequency is always divided by 'n' before being applied to the SIG input of the comparator. The output from the comparator will only be zero if the frequency fed back to M12-3 is 8kHz (ie. VCO frequency is n x 8kHz), and in phase with the 8kHz REF FREQ at M12-6.

The output from M12 is the control voltage, fed to the VCO M11.

The phase control loop seeks to phase-lock the two inputs to the comparator. If they are in phase, the comparator output is at high impedance ('TRISTATE'). In this condition the filter capacitor C14 has no charge or discharge path, so the extremely high gain of the PLL maintains its charge, and thus the voltage at TP6. So the frequency of VCO oscillation remains constant. Thus the loop stabilizes only when the frequency divided by 'n' from the VCO output is in phase with (and therefore at the same frequency as) the reference 8kHz.

In stable operation, therefore, the loop maintains VCO oscillations at n x 8kHz, and the feedback dividers reduce this frequency by a factor of 'n' to 8kHz.

Any disturbance in the loop will generate corrections to restore zero phase difference at the inputs of M12. Frequency deviations are therefore detected at an early stage as phase changes, giving a measure of 'phase advance' correction.

8.1.2.5 'INHIBIT' (VCO Off)

The VCO can be switched off by a logic-1 of 0V at M11 pin 5 (INHIBIT signal). This originates in the CPU system, setting FREQ₂₋₀ code to 111 (a non-existent 'R7' range) when AC functions are deselected. It also resets the +2 flip-flop M13a, so that no reference frequency is passed into the phase comparator.

8.1.2.6 VCO Supply Rail Protection

To prevent VCO oscillations appearing on the 15V power rails, the positive rail is heavily decoupled. M50 and M51 provide separate voltage regulation for circuits which are sensitive to the 8kHz reference frequency, thus increasing decoupling at this frequency.

8.1.2.7 VCO Output

The VCO and M12 operate from the +15V/0V supplies. M13, M9 and the frequency dividers which follow the VCO, all operate from the in-guard logic 0V/-15V supplies. The VCO output is therefore level-shifted to logic supply levels by Q5, Q6 and Q7. A re-conversion back to 5V levels is accomplished at the input to the phase comparator M12.

D43 also shifts the level of the INHIBIT signal at M11-5 to match the M11 supply levels. D44 limits the maximum negative excursion of M11-5 to one diode drop.

The n x 8kHz 'VCO OUT' output signal from M11 is inverted and level-shifted by Q5, Q6 and Q7 to match the phase and voltage requirements of the frequency divider M9. It is also fed as 'VCO O/P' to the frequency dividers at M5-9 (page 11.6-5).

8.1.3 FREQUENCY RANGE DIVIDERS

(Fig 8.3)

As mentioned earlier in para 8.1.1, the purpose of the synthesizer is to provide an accurate frequency reference for the quadrature sinewave oscillator. The VCO frequency (signal 'VCO O/P') is input to a series of frequency dividers, whose ratios are set by 'FREQ R₂₋₀', to make the dividers generate the selected frequency as 'SYNTH O/P'. FREQ R₂₋₀ is a three-bit word, five of whose codes represent the five frequency ranges.

A second purpose is to clock the Quasi-Sinewave Generator in synchronism with the synthesizer output (and hence with the main quadrature sinewave oscillator output). The synthesizer frequency is a multiple of the Quasi-Sine frequency, except on the 100Hz frequency range, where they are both at the same frequency. Thus the divider ratios are also chosen to generate the correct frequencies for the quasi-sinewave clock, for each frequency range selected.

8.1.3.1 Divider Ratios

(Circuit Diagram 430446 Page 11.6-5)

Binary/BCD Divider M5 is set for binary division by fixing M5-2 and M5-10 at Logic-0. Conversely, M1 is set for decimal division by fixing M1-2 and M1-10 at Logic-1.

BCD counter M2 is set to count up, by fixing M2-10 at Logic-1. Its $\overline{\text{CARRY OUT}}$ signal at M2-7 is at 1/10 of its clock frequency, and its Q1 output on M2-6 is at half its clock frequency. Flip-flop M4a is connected to divide its clocks by two.

Multiplexer M6 selects the appropriate source frequency to clock the Quasi-Sinewave generator. In particular, on the 100Hz Range it selects the $\overline{\text{CARRY OUT}}$ from M2, which is then divided by 10 in the quasi-sinewave counter, and returned via J6-51 to be used as SYNTH O/P.

8.1.3.2 Ratio Selection by Frequency Range
(Fig. 8.3 and Table 8.2)

The frequency range selection word $FREQ R_{2-0}$ is decoded by M29 into five range lines R_{4-0} . These lines perform the following functions:

- a. Switch ranges in the quadrature sinewave oscillator by relays RL1-RL8 selection of integrator capacitors (page 11.6-1);
- b. Switch ranges in the Cosine Squarer output filter (page 11.6-2);
- c. Adjust the division ratios of Frequency Range Dividers M5 and M1 (page 11.6-5) for range R_4 (1MHz Range),
- d. Select appropriate outputs from the Frequency Range Dividers (page 11.6-5); and
- e. The INHIBIT line turns off the VCO for non-AC functions.

Functions (a) and (b) are described later in Section 8.2. In this description we are concerned mainly with functions (c) and (d).

Table 8.2 shows how frequency range switching derives the synthesizer output frequencies by selecting the appropriate outputs from the dividers. Note that except for the 1MHz Range R_4 , the ratios of individual dividers are not altered.

On the 100Hz Range R_0 the overall division ratio of 8000 is achieved as for the 1kHz Range, but with a further division by 10 in the quasi-sinewave counter M11 on the AC Assembly.

On the 1MHz Range, R_4 , the division ratio of M5 is changed from 8 to 4. The DP_A inputs M5-5 and M5-6 are primed to Logic-1 and Logic-0 respectively, whereas on all other ranges the priming is reversed. Range R_4 also alters the division ratio of M1 from 10 to 25, by changing its priming bit-pattern, to correct the quasi-sinewave frequency; but as the synthesizer output is taken through M10-4/3 from M5 output, the adjustment to M1 does not affect the SYNTH O/P frequency.

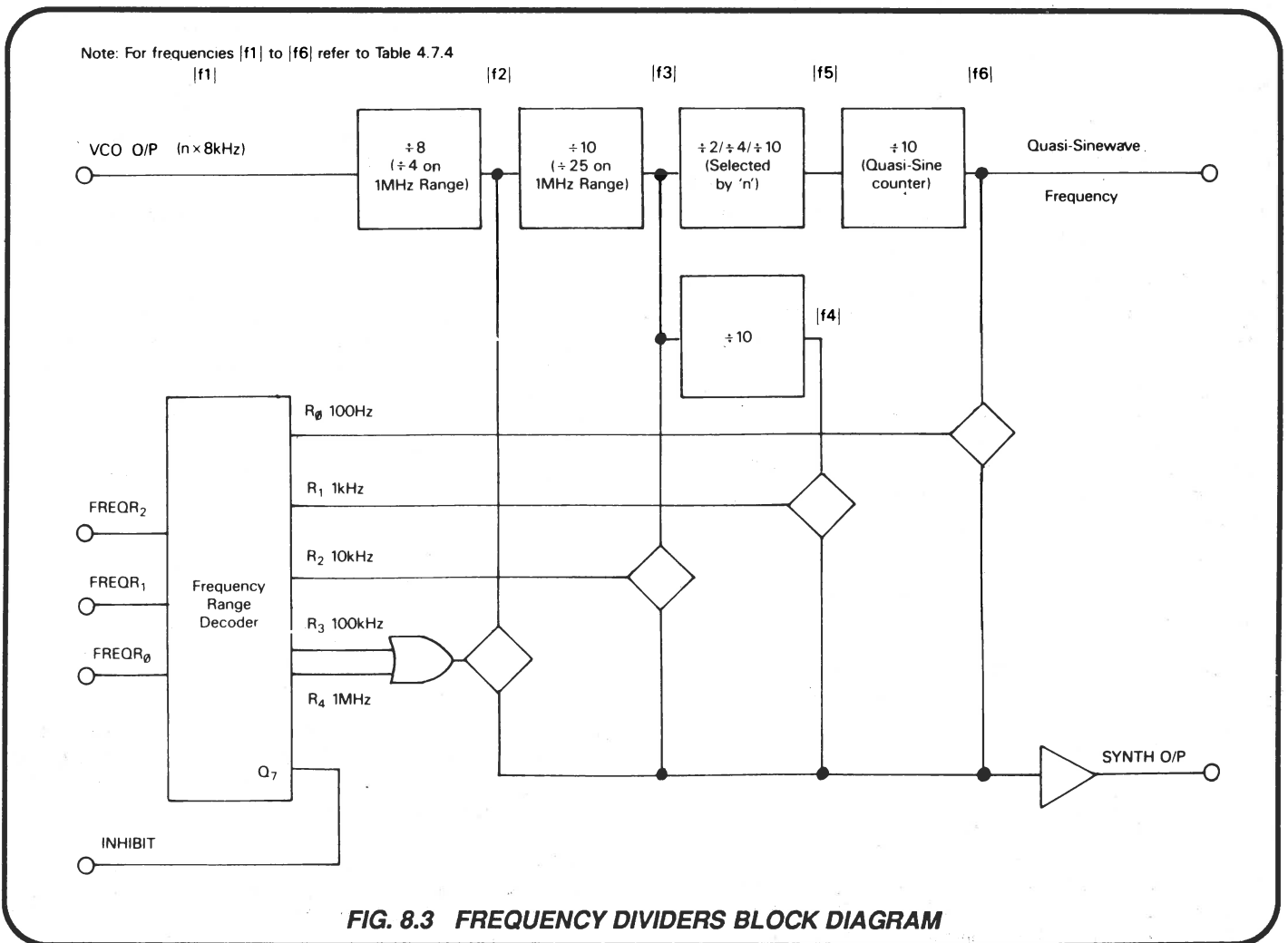


FIG. 8.3 FREQUENCY DIVIDERS BLOCK DIAGRAM

**Model 4708 -
Calibration and Servicing Handbook Vol. 1
Part No: 850246 Issue: 1**

Instrument Serial Number

24029-6

These advice sheets apply only to the instrument whose serial number is given above.

Introduction

AC Outputs - Improvement to Frequency Control System

In **Section 8**, Sub-section 8.1 deals with the Digital Frequency Synthesizer. Paras 8.1.2 on pages 8-1 to 8-3 describe the operation of the Voltage Controlled Oscillator.

This addendum changes paras 8.1.2, dealing with the introduction of an integrated VCO chip to replace the discrete VCO previously used, and modifications to the associated circuitry.

This upgrade improves the reliability and maintainability of the Digital Frequency Synthesizer by reducing the critical component count and easing fault diagnosis.

Contract No. F33659-90-C0065 specifies AC voltage (Option 20) and AC Current (Option 30) functions only. Therefore this addendum is pertinent to the contract

The above minor changes are detailed below.

Amendments to Section 8

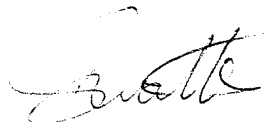
Pages 8-1, 8-2 and 8-3:

Delete the existing pages and substitute the new pages 8-1, 8-2 and 8-3 attached.

Amendments to the Contents and Illustrations List

No changes are required.

Checked by:



Date:

22nd May 92

SECTION 8 AC VOLTAGE OUTPUTS - FREQUENCY CONTROL SYSTEM

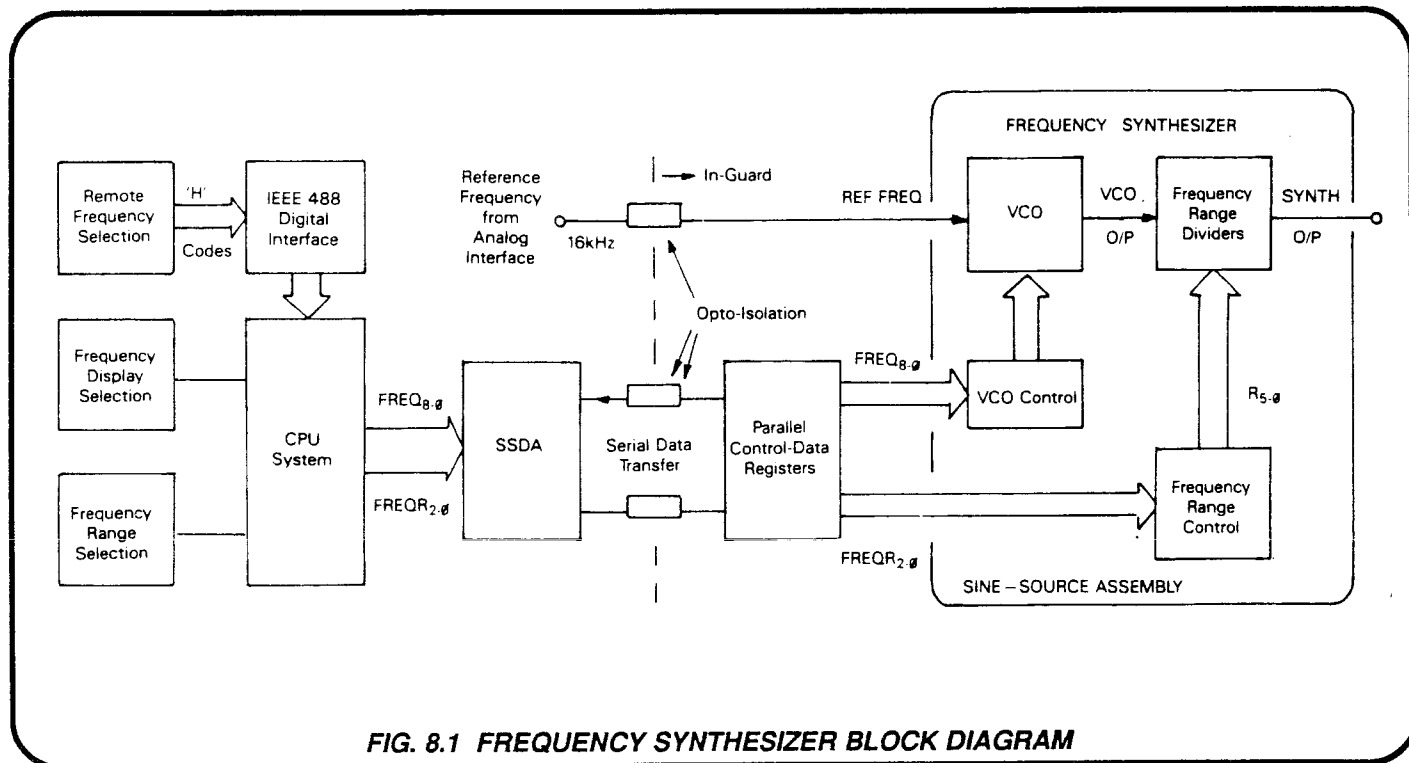


FIG. 8.1 FREQUENCY SYNTHESIZER BLOCK DIAGRAM

8.1 DIGITAL FREQUENCY SYNTHESIZER

(Fig. 8.1)

8.1.1 GENERAL

Users normally set the operating frequency by a combination of 'FREQUENCY RANGE' and 'FREQUENCY' display selections. These are memorized by the CPU and translated into two binary control words:

'FREQ R_{2-θ}'

A three-bit word, five of whose codes represent the five frequency ranges.

'FREQ_{8-θ}'

A nine-bit word whose value 'n' defines the chosen frequency with respect to the selected frequency range.

Users can select a frequency by means other than pressing a FREQUENCY RANGE key and setting a frequency on the display; for example by using 'Store' or the IEEE 488 digital interface. But regardless of the selection method, the CPU will always compute the two binary words, which then synthesize the selected frequency in the Sine-Source Assembly.

Both words are passed into guard via the SSDA, and latched at the outputs of the Reference Divider Parallel Control registers. A 16kHz reference frequency is also taken into guard, to be divided by two to 8kHz in the Sine-Source assembly.

After entering the Sine-Source assembly, FREQ_{8-θ} effectively multiplies the 8kHz reference by a factor 'n' to determine the frequency of a Voltage Controlled Oscillator (VCO). The VCO frequency (signal 'VCO O/P') is input into a series of frequency dividers, whose ratios are set by FREQ R_{2-θ}. The division ratios are chosen so as to make the dividers generate the Frequency Synthesizer output signal ('SYNTH O/P') at the user-selected frequency.

The purpose of the synthesizer is to provide an accurate frequency reference for the quadrature sinewave oscillator. The oscillator is approximately tuned by selection of circuit constants using the combination of 'FREQ R_{2-θ}' and 'FREQ_{8-θ}'.

'SYNTH O/P' acts as the reference in the phase comparator of a Phase-Locked Loop, controlling the frequency of the main Quadrature Sinewave Oscillator to an accuracy determined by the crystal oscillator.

8.1.2 VOLTAGE CONTROLLED OSCILLATOR

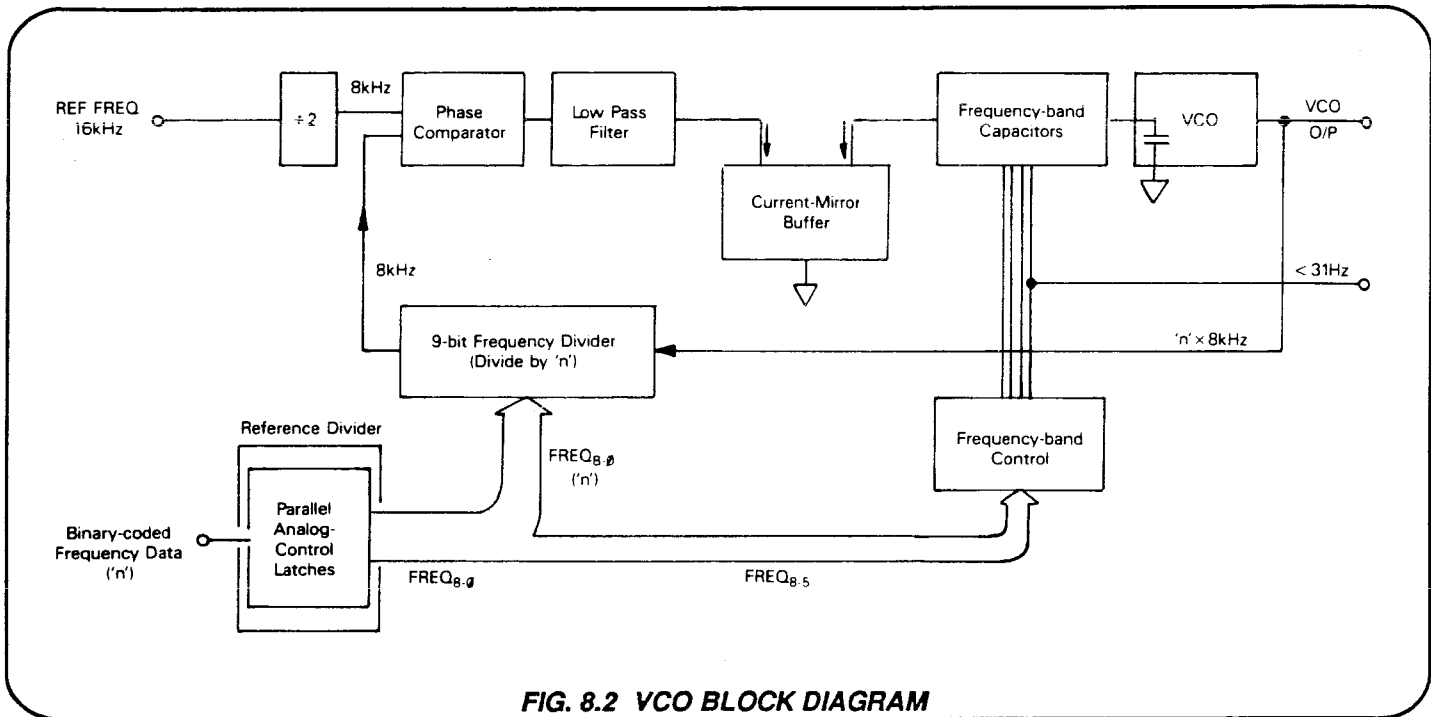


FIG. 8.2 VCO BLOCK DIAGRAM

8.1.2.1 Generation of 16kHz Reference (Circuit Diagrams 430648 page 11.3-2, 430652 page 11.4-5 and 430446 page 11.6-4)

The 16kHz (INT) signal originates at M16-14 in the Analog Interface (page 11.3-2) and is buffered as '16kHz(OG)' (page 11.3-1). On the Reference Divider at J4-104, it passes into guard via opto-isolator M3 (page 11.4-5), gating with 'DISABLE REF FREQUENCY' and 'BARK' in M24, filtered by R86/C38 to reduce harmonics from the transmission path, and is sent via the Mother Assembly to J6-53 on the Sine-Source Assembly (page 11.6-4).

Schmitt-trigger M14 inverts the 16kHz into a symmetrical squarewave, which is then applied as clock to M13a, a bistable connected to divide by two. The resulting 8kHz squarewave is taken as the reference frequency for phase comparator M12. Note that in this configuration the SIG input of M12 is used for the reference, and the divided VCO output signal is applied to the REF input. This is necessary to provide the correct sense in the phase control element M50, because of the inversion of integrator M11.

8.1.2.2 Squarewave Generation by the VCO

The VCO is a discrete-component ECL relaxation oscillator generating an output of frequency 'n' x 8kHz. Its natural frequency is dependent on:

- the value of capacitor C2 (or C2 plus one of C3 - C6),
- the value of its continuous discharge current through the phase control element (current mirror M50), and
- the value of its charging current through Q2 on alternate half cycles (4.7mA).

Consider C2 fully discharged. Q4 is off, so all the 4.7mA from Q6 passes through Q5. The collector voltage of Q4 is close to the positive rail, buffered by Q7 and R9 to hold Q5 on. Also, as Q3 is turned off by Q4 collector voltage, Q2 is turned on by its emitter, passing 4.7mA into C2 and the current mirror M50.

Capacitor C2 charges until Q4 turns on. Cumulative Schmitt action passes the fall at Q4 collector to the base of Q5, ensuring a rapid transition between states; so the 4.7mA is transferred from Q5 to Q4. Q3 turns on, its emitter falling quickly to cut Q2 off, so the charging path to C2 etc. is interrupted.

M50 continues to discharge C2, whose voltage falls slowly until Q4 starts to cut off again. The cumulative action is repeated to turn Q2 on, recharging C2. The cycle of charge and discharge continues, generating 'VCO O/P' squarewaves at buffer Q12 emitter.

8.1.2.3 Coarse Frequency Control (Circuit Diagram 430446 Page 11.6-4, and Fig. 8.2)

At any time, only one of the capacitors C3, C4, C5 and C6 can be connected in parallel with C2, by conduction of its associated transistor. This splits the frequency range of the VCO into five bands, governed by the four most-significant bits of the frequency control word $FREQ_{8,\emptyset}$ acting on M8. The association is shown in Table 8.1; note that the VCO frequency bands quoted in the table are correct only because the VCO is under the fine control of comparator M12, within the phase-locked loop.

| FREQ ₈₋₅ bits 8 7 6 5 | Range of 'n' Values | M8 Outputs at Logic-1 | C2-C6 Selection | VCO Frequency Band (kHz) |
|-------------------------------------|------------------------|-----------------------------|--------------------|--------------------------------|
| 0 0 0 0 | 10 to 31 | X ₀ | C2 and C6 | 80 to 248 |
| 0 0 0 1 | 32 to 63 | X ₁ | C2 and C5 | 256 to 504 |
| 0 0 1 X | 64 to 127 | X ₃₋₂ | C2 and C4 | 512 to 1016 |
| 0 1 X X | 128 to 255 | X ₇₋₄ | C2 and C3 | 1024 to 2040 |
| 1 X X X | 256 to 500 | NONE | C2 only | 2048 to 4000 |

TABLE 8.1 COARSE FREQUENCY CONTROL

8.1.2.4 Fine Frequency Control

(Circuit Diagram 430446 Page 11.6-4, and Fig. 8.2)

In the following description, capacitors C3, C4, C5 and C6 are ignored, but references to C2 should be read as including the appropriate additional capacitor.

The VCO output is fed back to M12 phase comparator via M9 and M13b, which are connected to act as a 9-bit frequency divider. Because the divider is controlled by FREQ₈₋₀, the VCO output frequency is always divided by 'n' before being applied to the REF input of the comparator. The output from the comparator will only be zero if the frequency fed back to M12-6 is 8kHz (ie. the VCO frequency is n x 8kHz), and in phase with the 8kHz REF FREQ at M12-3 (TP14).

The output from M12 is integrated by M11 to drive a DC current into the current mirror M50, which has a gain of two, its output current being drawn from the charge on C2. During the half-cycles of the VCO oscillation when C2 is being charged, the mirror obtains its current from Q2 conduction.

The phase control loop seeks to phase-lock the two inputs to the comparator. If they are in phase, the comparator output is at high impedance ('TRISTATE'). In this condition the integrator capacitors C16 and C18 have no charge or discharge path, so M11's extremely high gain maintains their charge, and thus the voltage at TP6. M11 supplies the input current for M50, the mirror continues to draw the same discharge current from C2, so the frequency of VCO oscillation remains constant. Thus the loop stabilizes only when the frequency divided by 'n' from the VCO output is in phase with (and therefore at the same frequency as) the reference 8kHz.

In stable operation, therefore, the loop maintains VCO oscillations at n x 8kHz, and the feedback dividers reduce this frequency by a factor of 'n' to 8kHz.

Any disturbance in the loop will generate corrections to restore zero phase difference at the inputs of M12. Frequency deviations are therefore detected at an early stage as phase changes, giving a measure of 'phase advance' correction.

8.1.2.5 'INHIBIT' (VCO Off)

The VCO can be switched off by a logic-1 of 0V at the base of Q11 (INHIBIT signal). This originates in the CPU system, setting FREQ R₂₋₀ code to 111 (a non-existent 'R7' range) when AC functions are deselected. It also resets the +2 flip-flop M13a, so that no reference frequency is passed into the phase comparator.

8.1.2.6 VCO Supply Rail Protection

To prevent VCO oscillations appearing on the 15V power rails, which also supply the integrator M11 and current mirror M50, the positive rail is heavily decoupled, regulated by Q8, and all devices whose currents are likely to disturb the rails are supplied through constant current sources (Q1, Q6, Q9 and Q13).

8.1.2.7 VCO Output

The VCO, M11 and M50 operate from the 15V supplies. M12, M9 and the frequency dividers which follow the VCO, all operate from the in-guard logic supplies of +0V and -15V. The VCO output from Q12 emitter is therefore limited by D1 to logic supply levels. A re-conversion back to 15V levels is accomplished at the input to the integrator M11, as TP31 pulses are negative at M11 input.

D1 is a Schottky hot carrier diode of reverse capacitance approx. 2pF. This avoids distorting the high frequency output squarewaves (for 1MHz output, the VCO oscillates at 4MHz).

The output passes through R12 to avoid loading the VCO, and then fed as 'VCO O/P' to the frequency dividers at M5-9 (page 11.6-5).

8.1.3 FREQUENCY RANGE DIVIDERS

(Fig 8.3)

As mentioned earlier in para 8.1.1, the purpose of the synthesizer is to provide an accurate frequency reference for the quadrature sinewave oscillator. The VCO frequency (signal 'VCO O/P') is input to a series of frequency dividers, whose ratios are set by 'FREQ R₂₋₀', so as to make the dividers generate the selected frequency as 'SYNTH O/P'. FREQ R₂₋₀ is a three-bit word, five of whose codes represent the five frequency ranges.

A second purpose is to clock the Quasi-Sinewave Generator in synchronism with the synthesizer output (and hence with the main quadrature sinewave oscillator output). The synthesizer frequency is a multiple of the Quasi-Sine frequency, except on the 100Hz frequency range, where they are both at the same frequency. Thus the divider ratios are also chosen to generate the correct frequencies for the quasi-sinewave clock, for each frequency range selected.

8.1.3.1 Divider Ratios

(Circuit Diagram 430446 Page 11.6-5)

Binary/BCD Divider M5 is set for binary division by fixing M5-2 and M5-10 at Logic-0. Conversely, M1 is set for decimal division by fixing M1-2 and M1-10 at Logic-1.

BCD counter M2 is set to count up, by fixing M2-10 at Logic-1. Its $\overline{\text{CARRY OUT}}$ signal at M2-7 is at 1/10 of its clock frequency, and its Q1 output on M2-6 is at half its clock frequency. Flip-flop M4a is connected to divide its clocks by two.

Multiplexer M6 selects the appropriate source frequency to clock the Quasi-Sinewave generator. In particular, on the 100Hz Range it selects the $\overline{\text{CARRY OUT}}$ from M2, which is subsequently divided by 10 in the quasi-sinewave counter, and returned via J6-51 to be used as SYNTH O/P.

8.1.3.2 Ratio Selection by Frequency Range
(Fig. 8.3 and Table 8.2)

The frequency range selection word $FREQ R_{2-0}$ is decoded by M29 into five range lines R_{4-0} . These lines perform the following functions:

- a. Switch ranges in the quadrature sinewave oscillator by relays RL1-RL8 selection of integrator capacitors (page 11.6-1);
- b. Switch ranges in the Cosine Squarer output filter (page 11.6-2);
- c. Adjust the division ratios of Frequency Range Dividers M5 and M1 (page 11.6-5) for range R_4 (1MHz Range),
- d. Select appropriate outputs from the Frequency Range Dividers (page 11.6-5); and
- e. The INHIBIT line turns off the VCO for non-AC functions.

Functions (a) and (b) are described later in Section 8.2. In this description we are concerned mainly with functions (c) and (d).

Table 8.2 shows how frequency range switching derives the synthesizer output frequencies by selecting the appropriate outputs from the dividers. Note that except for the 1MHz Range R_4 , the ratios of individual dividers are not altered.

On the 100Hz Range R_0 the overall division ratio of 8000 is achieved as for the 1kHz Range, but with a further division by 10 in the quasi-sinewave counter M11 on the AC Assembly.

On the 1MHz Range, R_4 , the division ratio of M5 is changed from 8 to 4. The DP_A inputs M5-5 and M5-6 are primed to Logic-1 and Logic-0 respectively, whereas on all other ranges the priming is reversed. Range R_4 also alters the division ratio of M1 from 10 to 25, by changing its priming bit-pattern, to correct the quasi-sinewave frequency; but as the synthesizer output is taken through M10-4/3 from M5 output, the adjustment to M1 does not affect the SYNTH O/P frequency.

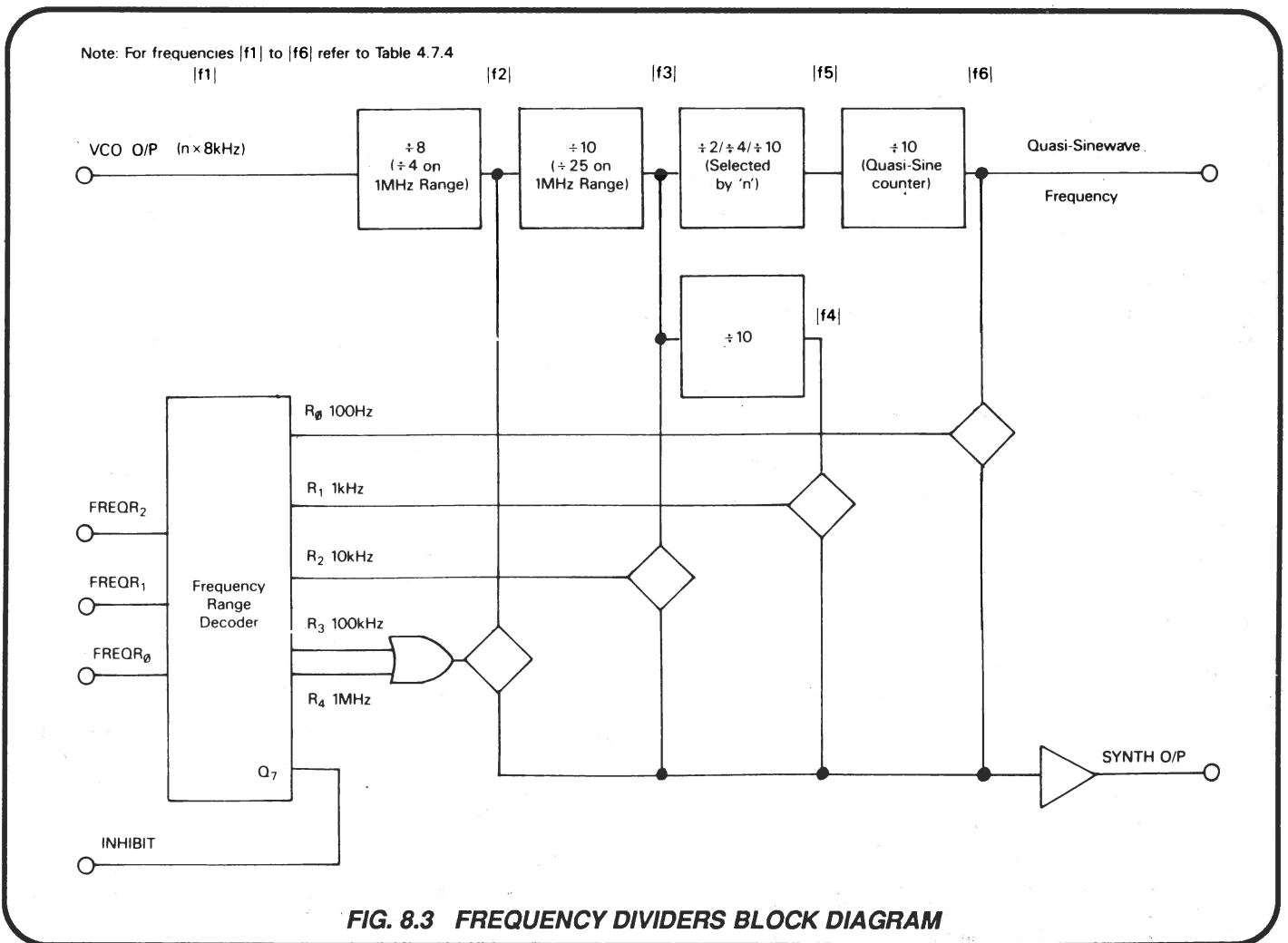


FIG. 8.3 FREQUENCY DIVIDERS BLOCK DIAGRAM

| FREQ. RANGE | FREQUENCY DISPLAY Hz | VCO OUTPUT (n × 8kHz) kHz | OVERALL DIVISION RATIO | RELEVANT DIVIDER RATIOS | | | | QUASI-SINE CLOCK FREQUENCIES (J6-50)* | SYNTHESIZER OUTPUT (J6-52) |
|----------------|---|-------------------------------------|------------------------|-------------------------|----------------|----------------|------------------|--|---|
| | | | | M5 | M1 | M2 | M11* (AC PCB) | | |
| 100Hz (R0) | 10-63 64-127 128-330 | 80-504 512-1016 1024-2640 | 8000 | 8 8 8 | 10 10 10 | 10 10 10 | 10 10 10 | Hz 100-630 640-1270 1280-3300 | Hz 10-63 64-127 128-330 |
| 1kHz (R1) | 0.30k-0.63k 0.64k-1.27k 1.28k-3.30k | 240-504 512-1016 1024-2640 | 800 | 8 8 8 | 10 10 10 | 10 10 10 | | kHz 1.5-3.15 1.6-3.175 1.28-3.3 | Hz 300-630 640-1270 1280-3300 |
| 10kHz (R2) | 3.0k-6.3k 6.4k-12.7k 12.8k-33.0k | 240-504 512-1016 1024-2640 | 80 | 8 8 8 | 10 10 10 | | | kHz 1.5-3.15 1.6-3.175 1.28-3.3 | kHz 3.0-6.3 6.4-12.7 12.8-33.0 |
| 100kHz (R3) | 30k-63k 64k-127k 128k-330k | 240-504 512-1016 1024-2640 | 8 | 8 8 8 | | | | kHz 1.5-3.15 1.6-3.175 1.28-3.3 | kHz 30-63 64-127 128-330 |
| 1MHz (R4) | 0.30M-1.00M | 1200-4000 | 4 | 4 | | | | kHz 1.2-4.0 | kHz 300-1000 |

* Quasi-sine counter M11 on the AC Assembly divides VCO output at all frequencies, but contributes to SYNTH O/P only on the 100Hz Frequency Range.

TABLE 8.2 SYNTHESIZER OUTPUT - DIVISION RATIOS

8.1.3.3 Frequency Synthesis for the Quasi-Sinewave Generator
(Fig. 8.3 and Table 8.3)

The 100Hz frequency range uses the quasi-sinewave counter as a divider in deriving its SYNTH O/P frequency. Although not a direct component of the frequency of the SYNTH O/P signal on other ranges, the quasi-sinewave frequency is deliberately derived in the synthesizer, so that the zero-crossings of its waveform can be synchronized at a time when the main sinewave is also crossing zero. (The main sinewave, of course, can be at a high multiple of the quasi-sinewave frequency.)

The quasi-sinewave frequency is held to a maximum of 330Hz (400Hz on the 1MHz range), to limit errors due to high harmonics. The 1MHz frequency range contains only one frequency band, but the other four ranges are each divided into three bands, corresponding to the three most significant bits of the frequency word $FREQ_{8-6}$.

Table 8.3 illustrates the way that the three bands affect the quasi-sine frequencies. Note that division ratios of 2, 4 or 10, by M2 and M4a, are selected by $FREQ_6$, $FREQ_7$ and $FREQ_8$ at M6 pins 11, 10 and 9 respectively. Frequency range R_0 at M7-2 ensures that on the 100Hz range, the divide-by-10 output of M2 is always selected, regardless of the state of these three bits.

To ensure that the Divide-by-2 outputs of M2 and M4a are locked into the correct phase for quasi-sinewave generation, a synchronizing signal 'CHOP LOCK' is derived from the quasi-sinewave counter 'Q₀' output, entering at J6-75. Following DC-restoration from 8V supplies to the normal 0V/-15V logic supplies by C20/D3/R15/M7, the signal is applied to M4a SET input, and M2 RESET input.

For all frequency ranges, the '100-5kHz' quasi-sinewave generator clock is passed to the AC Assembly via J6-50 and the Mother Assembly. This output is level-shifted by Q42, to the 8V supplies which are used in the quasi-sinewave generator circuitry.

The quasi-sinewave generator reset signal 'SYNC₀(IG)' (which was transferred into Guard by M2 on the Reference Divider), is input to the Sine-Source Assembly on J6-48 to be similarly level-shifted by M43, before being passed to the AC Assembly via J6-49. This signal, however, is not used on this instrument.

For other details of the quasi-sinewave generator refer to Section 6.6.

| FREQ. RANGE | FREQUENCY DISPLAY Hz | FREQUENCIES SYNTHESIZED IN SINE-SOURCE ASSEMBLY | | | | OVERALL DIVISION RATIO | QUASI-SINE CLOCK FREQUENCY (J7-50) | QUASI-SINE FREQUENCY (& J7-51) Hz | OUTPUT FREQUENCY Hz |
|-------------|-------------------------|---|---|----|----|------------------------|--|--------------------------------------|---|
| | | VCO OUTPUT (n × 8kHz) kHz | DIVIDER RATIOS for QUASI-SINEWAVE M5 M1 M2 M4a | | | | | | |
| 100Hz (R0) | 10-63 | 80-504 | 8 | 10 | 10 | — | Hz 100-630 640-1270 1280-3300 | 10-63 64-127 128-330 | 10-63 64-127 128-330 |
| | 64-127 | 512-1016 | 8 | 10 | 10 | — | | | |
| | 128-330 | 1024-2640 | 8 | 10 | 10 | — | | | |
| 1kHz (R1) | 0.30k-0.63k | 240-504 | 8 | 10 | 2 | — | kHz 1.5-3.15 1.6-3.175 1.28-3.3 | 150-315 160-317.5 128-330 | 0.30k-0.63k 0.64k-1.27k 1.28k-3.30k |
| | 0.64k-1.27k | 512-1016 | 8 | 10 | 2 | 2 | | | |
| | 1.28k-3.30k | 1024-2640 | 8 | 10 | 10 | — | | | |
| 10kHz (R2) | 3.0k-6.3k | 240-504 | 8 | 10 | 2 | — | kHz 1.5-3.15 1.6-3.175 1.28-3.3 | 150-315 160-317.5 128-330 | 3.0k-6.3k 6.4k-12.7k 12.8k-33.0k |
| | 6.4k-12.7k | 512-1016 | 8 | 10 | 2 | 2 | | | |
| | 12.8k-33.0k | 1024-2640 | 8 | 10 | 10 | — | | | |
| 100kHz (R3) | 30k-63k | 240-504 | 8 | 10 | 2 | — | kHz 1.5-3.15 1.6-3.175 1.28-3.3 | 150-315 160-317.5 128-330 | 30k-63k 64k-127k 128k-330k |
| | 64k-127k | 512-1016 | 8 | 10 | 2 | 2 | | | |
| | 128k-330k | 1024-2640 | 8 | 10 | 10 | — | | | |
| 1MHz (R4) | 0.30M-1.00M | 1200-4000 | 4 | 25 | 10 | — | kHz 1.2-4.0 | 120-400 | 0.30M-1.00M |

TABLE 8.3 QUASI-SINEWAVE FREQUENCY DERIVATION IN FREQUENCY SYNTHESIZER

8.1.3.4 Synthesizer Frequency Analysis

Table 8.4 is provided to allow a complete analysis of the frequencies to be found in the divider circuitry. In part, it duplicates figures from tables 8.2 and 8.3.

| FREQ. RANGE (NOM) | FREQUENCY DISPLAY Hz | VCO DIVISOR 'n' | f1 VCO OUTPUT (n x 8kHz) kHz | f2 M5 OUTPUT (f1-8) kHz | f3 M1 OUTPUT (f2-10) kHz | f4 M2 OUTPUT (f3-10) Hz | f5* M6 OUTPUT (M6.3) Hz | | | f6 J6-51 INPUT (f5-10) Hz |
|-------------------|---|----------------------------|----------------------------------|--|--|--|---------------------------------------|-----------------------|----------------------------------|--|
| | | | | | | | M6 Input Channels and Division Ratios | | | |
| | | | | | | | X ₀ (f3-2) | X ₁ (f3-4) | X _{2,7} (f3-10) | |
| 100Hz (R0) | 10-63 64-127 128-330 | 10-63 64-127 128-330 | 80-504 512-1016 1024-2640 | 10-63 64-127 128-330 | 1.0-6.3 6.4-12.7 12.8-33.0 | 100-630 640-1270 1280-3300 | | | 100-630 640-1270 1280-3300 | [10-63] [64-127] [128-330] |
| 1kHz (R1) | 0.30k-0.63k 0.64k-1.27k 1.28k-3.30k | 30-63 64-127 128-330 | 240-504 512-1016 1024-2640 | 30-63 64-127 128-330 | 3.0-6.3 6.4-12.7 12.8-33.0 | [100-630] [640-1270] [1280-3300] | 1500-3150 | 1600-3175 | 1280-3300 | 150-315 160-317.5 128-330 |
| 10kHz (R2) | 3.0k-6.3k 6.4k-12.7k 12.8k-33.0k | 30-63 64-127 128-330 | 240-504 512-1016 1024-2640 | 30-63 64-127 128-330 | [3.0-6.3] [6.4-12.7] [12.8-33.0] | 100-630 640-1270 1280-3300 | 1500-3150 | 1600-3175 | 1280-3300 | 150-315 160-317.5 128-330 |
| 100kHz (R3) | 30k-63k 64k-127k 128k-330k | 30-63 64-127 128-330 | 240-504 512-1016 1024-2640 | [30-63] [64-127] [128-330] | 3.0-6.3 6.4-12.7 12.8-33.0 | 100-630 640-1270 1280-3300 | 1500-3150 | 1600-3175 | 1280-3300 | 150-315 160-317.5 128-330 |
| 1MHz (R4) | Hz 0.30M-1.00M | 'n' 150-500 | kHz 1200-4000 | (f1-4) kHz [300-1000] | (f2-25) kHz 12-40 | (f3-10) Hz 1200-4000 | | | 1200-4000 | Hz 120-400 |

TABLE 8.4 SYNTHESIZER DIVIDERS - FREQUENCY ANALYSIS

8.2 QUADRATURE SINEWAVE OSCILLATOR

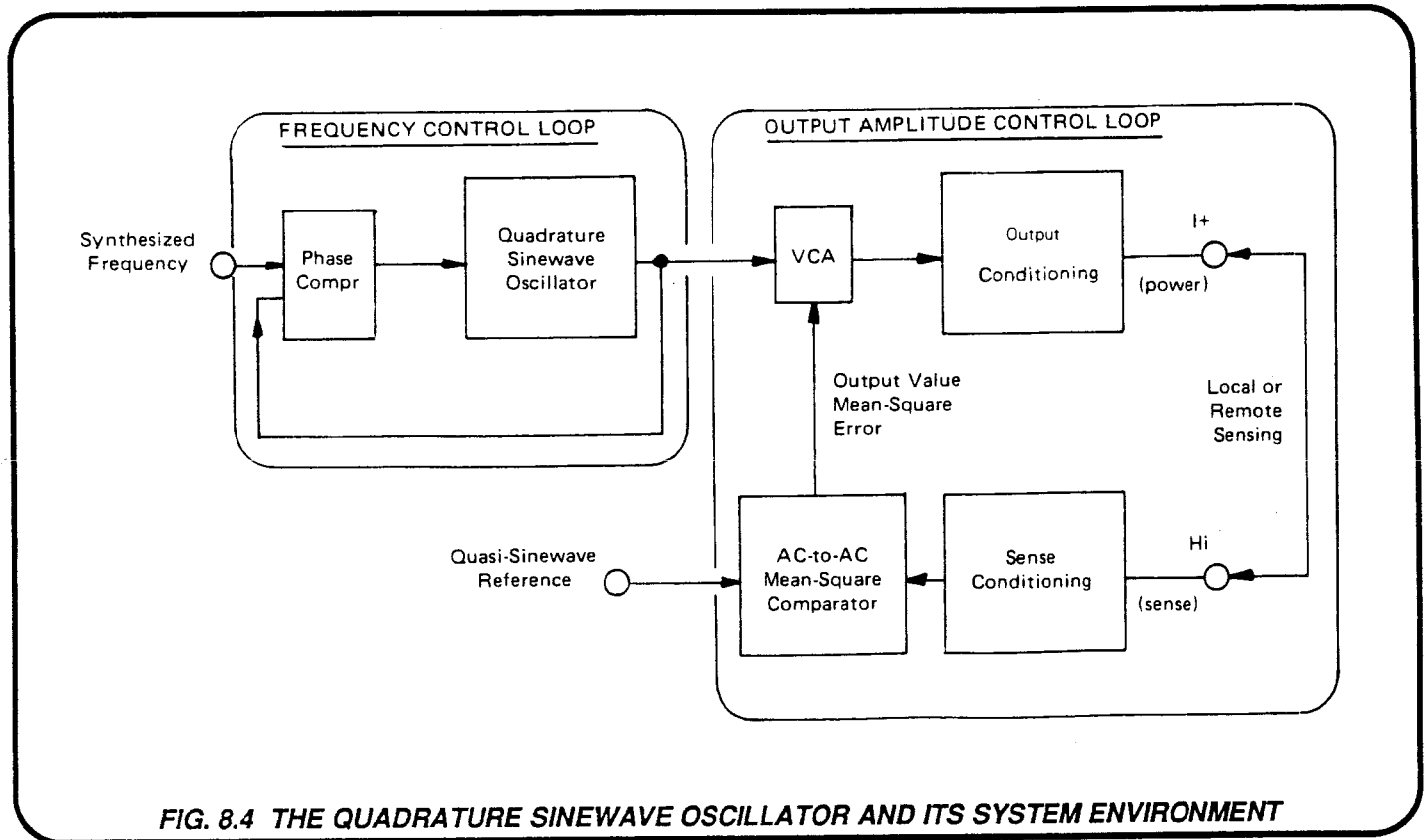


FIG. 8.4 THE QUADRATURE SINEWAVE OSCILLATOR AND ITS SYSTEM ENVIRONMENT

8.2.1 PURPOSE and ENVIRONMENT

(Fig. 8.4)

The purpose of the oscillator is to define the amplitude-stability, purity and frequency of the sinusoidal output of the instrument on all ranges. Its output is of sufficient constant amplitude to drive the subsequent signal-conditioning circuitry.

After originating in the oscillator, the sinewave amplitude is accurately defined in two output- sense loops, using a low-distortion VCA as control element. The sinewave is set close to its demanded value by analog conditioning in the output circuits.

The output voltage is sensed, attenuated to its 1V Range equivalent, then its mean-square value is compared against that of the quasi-sinewave reference. The difference is converted into a DC error voltage which corrects the output by adjusting the VCA gain.

As the purity and amplitude-stability of the output sinewave depend substantially upon its source, a high quality oscillator is necessary. A 'quadrature' (dual-integrator) circuit is chosen for two main reasons:

- This arrangement allows extensive phase and amplitude controls to be applied, to establish the required high specification.
- Its natural frequency can be easily programmed by electrical selection of its component values.

The oscillator is approximately tuned by selection of circuit constants using the two CPU-derived binary words 'FREQ R₂₋₀' and 'FREQ₃₋₀'. These also accurately define the crystal-sourced frequency of the Digital Frequency Synthesizer output, to which the oscillator is phase-locked. Thus the output sinewave frequency accuracy is held to 100ppm.

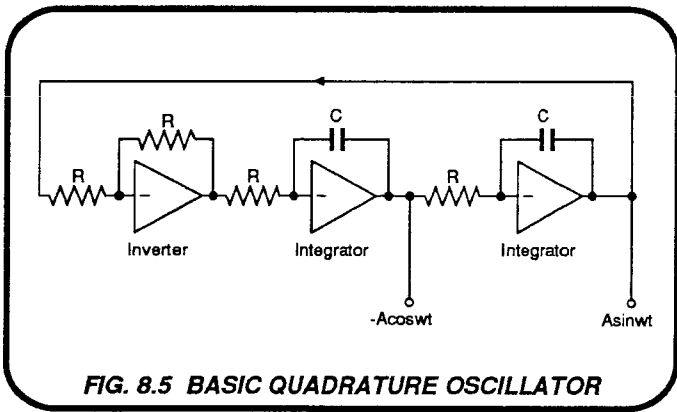
8.2.2 SIMPLE QUADRATURE OSCILLATOR

8.2.2.1 Basic Circuit (Fig. 8.5)

The circuit consists of two RC integrators and an inverter, connected in a positive feedback loop. The nominal phase-shift around the loop is 360° (actually 720° : 270° in each integrator, 180° in the inverter).

Assuming perfect integrators, matched components and an inverter gain of exactly -1, this circuit will undergo stable oscillation at a frequency given by:

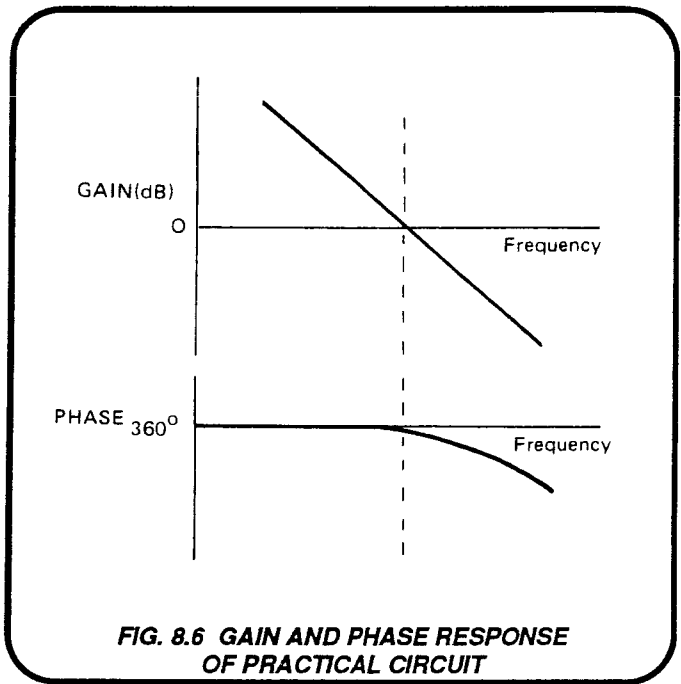
$$\omega = 1/RC$$



8.2.2.2 Inadequacies of the Basic Circuit (Figs. 8.5 and 8.6)

For an unrefined practical implementation of the basic circuit, the loop gain and phase response would be as shown in Fig. 8.6.

The two main conditions for stable oscillation at constant amplitude are: exactly unity loop gain, and exactly 360° (or multiple of 360°) of loop phase-shift; so the circuit of Fig. 8.5 clearly does not satisfy these conditions. Without some attempt to control gain and phase, the loop would be either over- or under-damped, so oscillations would either die away or increase in amplitude until limited by the supply rails.



8.2.3 PRACTICAL QUADRATURE OSCILLATOR (Fig. 8.7)

The method chosen to refine the simple circuit corrects the loop phase-shift to exactly 360° using a feedback signal. Furthermore, it is arranged that this signal is correct only at a given output

amplitude, so the amplitude of stable oscillation is defined. In Fig. 8.7 the correction circuit is added.

8.2.3.1 Phase Correction

The loop phase is corrected by introducing a small cosine term ($B \cdot \cos \omega t$) to be summed with the sine feedback ($A \cdot \sin \omega t$) at the input to the inverter. The resultant output of the inverter is thus given by:

$$V(t) = -(A \cdot \sin \omega t + B \cdot \cos \omega t) = M \cdot \sin(\omega t + \phi) \quad \text{----- 1}$$

where $M = \sqrt{A^2 + B^2}$
and $\sin \phi = B/M$; $\cos \phi = A/M$.

Hence $\phi = \tan^{-1}(B/A)$.
and for $B \ll A$: $\phi \approx B/A$ ----- 2

The ϕ term represents an additional phase shift in the inverter, which by suitable scaling can be made equal to the phase error in the basic oscillator loop. Scaling is achieved by multiplying $A \cdot \cos \omega t$ by the DC amplitude error ($A^2 - I_{REF}$), as described opposite.

8.2.3.2 Constant Amplitude Control

The above method of phase correction plays its part in controlling the output amplitude. With both sine and cosine terms available, a DC analog of the sinusoidal output amplitude can be obtained utilizing the identity:

$$\sin^2\omega t + \cos^2\omega t = 1.$$

Equal-amplitude sine and cosine outputs are squared in 4-quadrant multipliers. Their squares are summed to generate amplitude feedback in the form:

$$\begin{aligned} & A^2 \sin^2\omega t + A^2 \cos^2\omega t \\ &= A^2(\sin^2\omega t + \cos^2\omega t) \\ &= A^2. \end{aligned}$$

This method therefore expresses the square of the output amplitude as a DC current analog, from which is subtracted a constant DC reference current I_{REF} .

The difference current ' $A^2 - I_{REF}$ ' is taken as the amplitude error, which defines the fraction 'B' of the cosine term to be fed back to the inverter as ' $B \cdot \cos\omega t$ '.

In a perfect oscillator, this 'cos' feedback would be driven to zero. But in any practical circuit, some small remnant of $B \cdot \cos\omega t$ persists at the correct loop phase-shift, correcting the loop gain to within the stability specification.

Acting thus together, the combined feedbacks correct both loop gain and phase simultaneously. The method of amplitude correction prevents the appearance of AC components in the amplitude error signal, thus avoiding unacceptable levels of harmonic distortion due to the cosine multiplier.

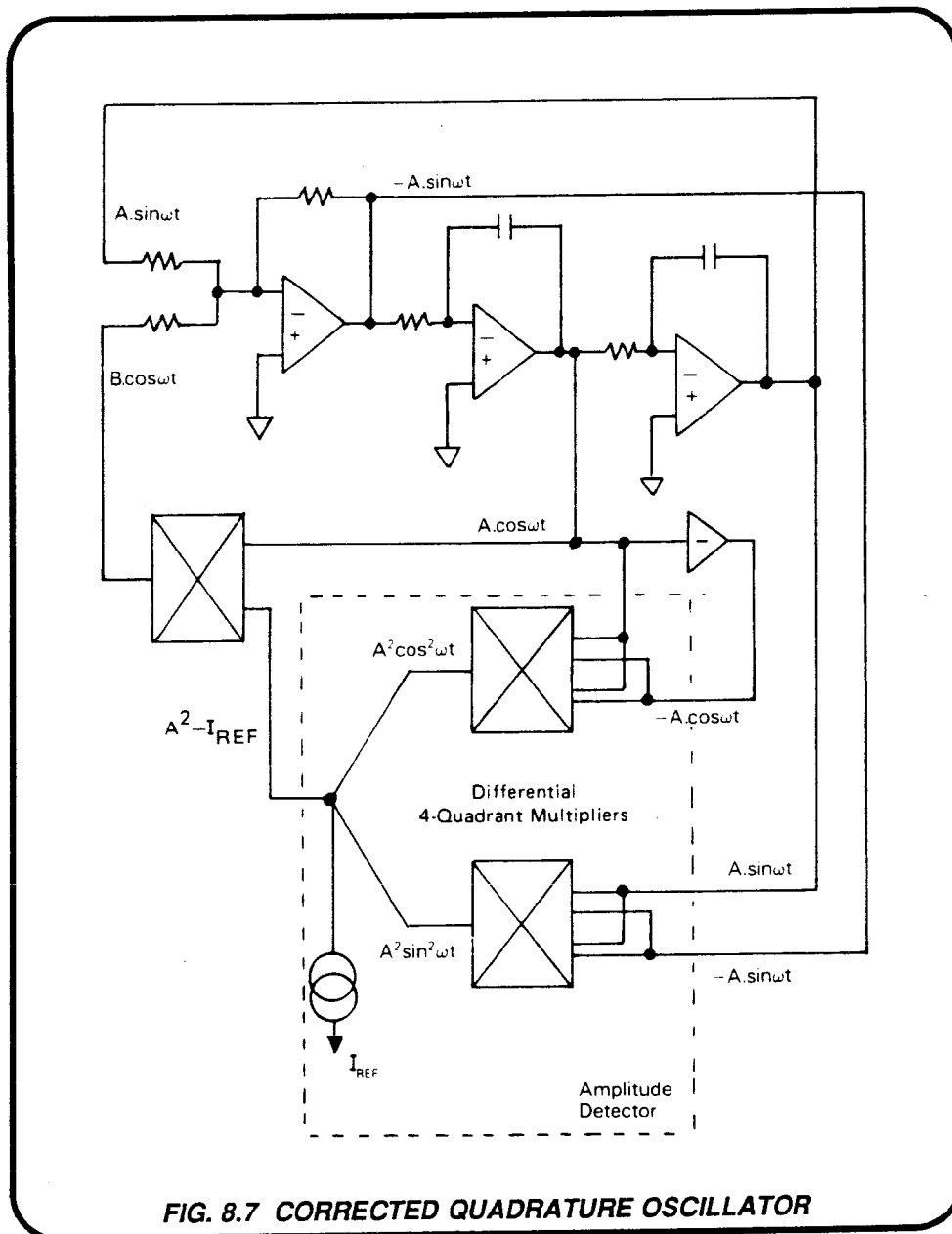


FIG. 8.7 CORRECTED QUADRATURE OSCILLATOR

8.2.4 FREQUENCY CONTROL

Section 8.1 describes frequency generation in the Frequency Synthesizer. Binary control words computed by the CPU represent user-selections of FREQUENCY RANGE and FREQUENCY. These adjust frequency division ratios in the feedback circuit of a

phase-locked loop, and division ratios in subsequent frequency dividers, to set the Synthesizer output signal 'SYNTH O/P' to the selected frequency. Stability and accuracy are assured by a crystal-sourced reference of 16kHz.

8.2.4.1 Coarse Adjustment

The Sinewave Oscillator is already approximately tuned to the selected frequency by the two binary control words, which select from weighted values of integration capacitance and resistance:

- **Frequency ranges** are selected by control word $FREQ R_{2-\phi}$, which controls relays to change the values of integrator capacitance.
- **Frequencies within a range** are selected by the control word $FREQ_{8-\phi}$, which controls FETs to change the values of integrator resistance.

8.2.4.2 Fine Adjustment

(Fig. 8.8)

The oscillator's output is converted into a squarewave and applied as 'signal' to the phase comparator of a second phase-locked loop. The Synthesizer output signal 'SYNTH O/P' is input as reference frequency to the same comparator. The difference is integrated to produce a DC phase error signal, which is applied to control the gain of the inverter stage of the oscillator.

It can be shown that the actual operating frequency is a function of the inverter gain. In the frequency domain, the oscillator loop transfer function is given by:

$$G \times (\omega_0/s) \times (\omega_0/s)$$

where G is the inverter gain,

ω_0 is the unity-gain frequency

$s = j\omega$, where ω is the actual frequency of operation.

For stable oscillation, the loop transfer function must equal $1/0$.

$$\text{Hence } G \cdot \omega_0^2 / s^2 = 1/0$$

$$\text{Therefore } G \cdot \omega_0^2 = j^2 \cdot \omega^2 = -1 \cdot \omega^2$$

$$\text{and } \omega = -\omega_0 \cdot G^{1/2}$$

Thus by adjusting the gain of the inverter, the phase error signal from the comparator exerts fine control of the oscillator frequency. This phase-locks the oscillator to the Frequency Synthesizer.

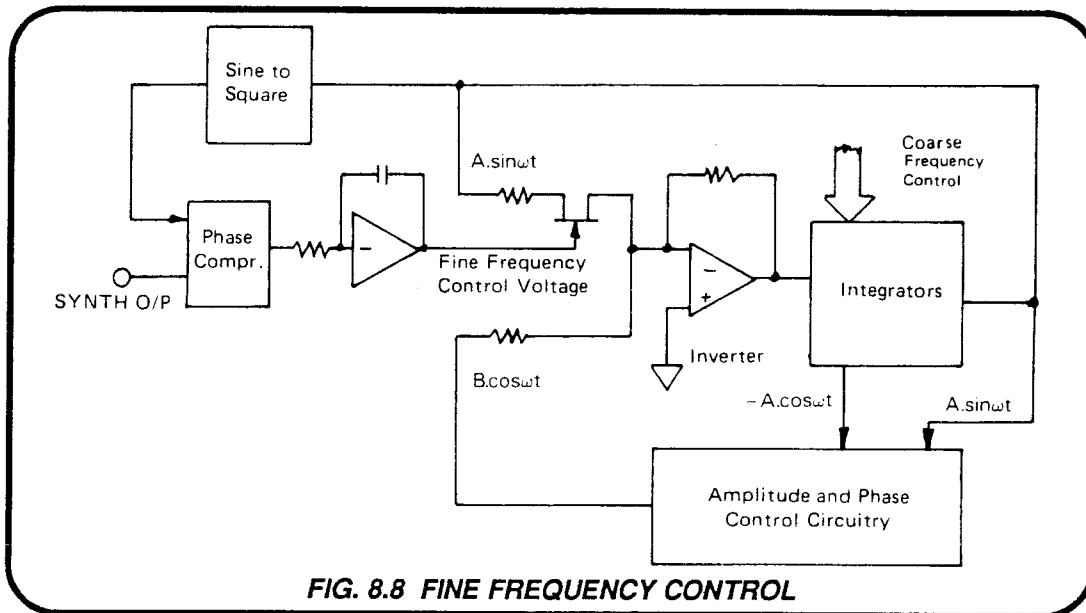


FIG. 8.8 FINE FREQUENCY CONTROL

8.2.5 OSCILLATOR OUTPUT

The $A \cdot \sin \omega t$ signal is inverted and buffered out to provide the drive to the output loop VCA. The buffer feedback resistors are positive TC thermistors which compensate for the TC of the VCA input FETs (refer to section 9).

QUADRATURE OSCILLATOR CIRCUIT DESCRIPTION

8.2.6 MAIN INTEGRATORS

(Circuit Diagram 430446 page 11.6-1)

The cascaded integrators consist of M19 and M30 together with their input resistors and feedback capacitors. Both circuits are identical in operation, although some slight differences in implementation exist.

Adjustments to the natural oscillation frequency are made by switching the integrator time constants.

8.2.6.1 Frequency Range Switching

The feedback capacitors are selected by the binary control word 'FREQ $R_{2-\emptyset}$ '. This is decoded into five lines $R_{4-\emptyset}$ (page 11.6-5), each representing a frequency range. The capacitors for R_4 (1MHz) are fixed, one other set being added in parallel when its range is selected. Relays RL1 to RL8 perform the switching.

8.2.6.3 Slew Rate and Protection

Emitter-followers at the outputs of the integrator operational amplifiers allow the high slew-rates necessary to be achieved, by buffering any loading effects. The diode clamp networks between output and input prevent latch-up by imposing unity-gain feedback when output peaks exceed approx. 5V.

8.2.6.2 Frequency Increments

The integrator input resistors are connected in a binary-weighted ladder network, the total input resistance depending on the pattern of FET conduction. Each FET is turned on by its corresponding binary digit in the frequency control word $FREQ_{8-\emptyset}$ (appearing as $A_{8-\emptyset}$ and $B_{8-\emptyset}$ at the FET gates).

8.2.6.4 Output Offset Control

The amplitude detector circuit squares the outputs from both integrators. It is therefore important that their DC offset voltages are not included in the squaring computation.

The least-significant bits, representing low frequencies, control the highest-value resistors at the base of the ladder. The most-significant bits, which represent the highest frequencies, control the lowest-value resistors at the top.

The 'Cosine' offset is removed by adjustment of R50 at the non-inverting input of M30, and the 'Sine' offset by R49 at the input of inverter M15. This latter adjustment removes the combined offsets of M15 and M19. (At manufacture, and after any replacement of major board components, the controls are iteratively adjusted for minimum AC fundamental component in the DC amplitude control signal 'V_G' at link 'B').

Any user-selected frequency in a given frequency range is thus represented by a bit-pattern in the control word, which is repeated in the FET conduction pattern and resistance selection at the input of both integrators.

8.2.7 INVERTER STAGE

The inverter completes the positive feedback loop of the basic oscillator. The very high bandwidth device used for M15 is compensated by C27, and its TO8 case is grounded.

As mentioned earlier, its DC input offset is adjusted by R49 to null the sine DC offset.

8.2.7.1 Gain Control

The inverter has three inputs:

- A.sinwt from the second integrator, the basic oscillator feedback loop.
- B.coswt from the Amplitude correction loop.
- 'FREQ ERROR', a DC current which alters the inverter's input resistance (and hence its gain) by controlling FET conduction, phase-locking the oscillator to the synthesizer output frequency (refer to para 8.2.4.2).

Two FETs in series are required for the amplitude levels reached by A.sinwt. R41 is selected to account for differing 'on' resistances of different batches of FETs. This input circuit is a scaled-down version of that employed for the VCA in the main output loop, details of which appear in Section 9. A description of the action of the frequency tracking loop follows at para 8.2.7.2.

Inputs (a) and (b) [A.sinwt and B.coswt] are summed as currents at the inverting input. The amplitude of the B.coswt signal is determined by the action of the amplitude control loop, described in sections 8.2.8 and 8.2.9.

8.2.7.2 Frequency Tracking - General

As stated in para 8.2.4.2, the oscillator's output is applied to the comparator of a phase-locked loop. The Synthesizer output is input as reference frequency to the same comparator. The phase-difference pulse train from the comparator is integrated to produce a DC phase error signal, which is applied to control the gain of the inverter stage of the oscillator. This exerts fine control of the oscillator frequency, tracking the Synthesizer frequency.

Input (c) controls the gain of the inverter. The A.sinwt is applied via two input resistors R28 and R41 in series. R28 is shunted by the two FETs of Q29, whose the source-drain resistance is altered by the 'FREQ ERROR' current via current-mirrors M16 and M18.

8.2.7.3 Tracking Comparator

(Circuit Diagram 430844 Page 11.7-6)

After buffering and inversion by M47 on the Sine-source Assembly (page 11.6-1), the oscillator $A \cdot \sin \omega t$ output is passed to the AC Assembly via J6-45 and J7-45.

On the AC Assembly, the sine wave is converted into a square wave by Schmitt bistable Q32/Q33, and level-shifted to logic supply levels of 0V and -15V by D25/Q28. Q28 provides a current-limited load for maximum gain, while D24 and D25 prevent voltage saturation of Q32. Q23 buffers the resulting square wave into the phase comparator input at M30-6.

The slower zero-crossings at the lowest frequencies could be susceptible to HF noise, so this is filtered, on the 100Hz frequency range only, by Q27 and C48.

The 'SYNTH O/P' square wave, at the demanded frequency, is transmitted from the Sine-source Assembly at low (1V Full Range) level. This holds the maximum slew rate to a value which avoids inducing interference in other internal circuits. Q20 and Q21 amplify the signal to the CMOS logic levels of 0V and -15V required by the comparator input at M30-3.

Note that current steering is used between Q32 and Q33, and between Q20 and Q21. Also, a constant current source Q22 provides Q23 emitter current. These measures prevent the fast switching edges in the schmitt and amplifier circuits from injecting spikes into the supply rails.

Phase-comparator output M30-5 consists of positive pulses (0V) when the oscillator lags the synthesizer, or negative (-15V) when the oscillator leads. When both are in phase, M30-5 is at high impedance.

At integrator M31 input, zener diode D30 holds the non-inverting input at -6.4V; so for in-phase signals into the comparator, the inverting input seeks the same level. The integrator tends to hold its voltage level (with very slight drift due to capacitor leakage but limited to -9.8V by D32/D33). When the oscillator output lags the synthesizer output, the positive-going comparator pulses are integrated to drive M31-6 slowly more negative. When the phase of the oscillator leads, the integrator output becomes more positive.

The phase control loop seeks to phase-lock the two inputs to the comparator. If they are in phase, the comparator output is at high impedance ('TRISTATE'). In this condition the integrator capacitors C53 and C56 have no charge or discharge path, so M31's extremely high gain maintains a constant charge on the capacitors. The constant voltage on Q37 base maintains a constant 'FREQ ERROR' current.

Q37 appears to be an open-collector amplifier. However, its collector current passes via J7-44 and J6-44, into the two current-mirrors at the input to the oscillator inverter on the Sine-source Assembly (page 11.6-1), and thence to the -15V rail.

With constant input current, the mirrors continue to draw the same output current from the AN4 bias network for Q29, so the frequency of the dual-integrator oscillator remains constant. Thus the loop stabilizes only when the oscillator frequency is in phase with (and therefore at the same frequency as) the Frequency Synthesizer output.

The overall action is for a lagging oscillator (frequency lower than the synthesizer) to increase the DC current flowing into the two current mirrors, and vice-versa if the oscillator leads. The two inputs to the comparator are in phase when the sine wave output from the oscillator is at the synthesizer frequency.

Any disturbance in the loop will generate corrections to restore zero phase difference at the inputs of M30. Frequency deviations are therefore detected at an early stage as phase changes, giving a measure of 'phase advance' correction.

8.2.8 SINEWAVE AMPLITUDE DETECTOR

The method of amplitude measurement relies on the identity ' $\sin^2 \omega t + \cos^2 \omega t = 1$ ' to convert AC output signals from the oscillator into a representative DC signal.

Squaring $A \sin \omega t$ and $A \cos \omega t$:

$$A^2 \sin^2 \omega t = (A^2 - A^2 \cos 2\omega t)/2,$$

$$A^2 \cos^2 \omega t = (A^2 + A^2 \cos 2\omega t)/2,$$

The AC waveforms of $A^2 \cos 2\omega t$ and $A^2 \sin 2\omega t$ are inverted versions of each other, at twice the original frequency, and both are symmetrical about the DC mean value of $A^2/2$.

By summing the two, the AC waveforms are eliminated, leaving a DC signal, A^2 , representing the square of the amplitude.

In the Amplitude Detector, the V_{\sin} and V_{\cos} outputs from the oscillator are squared electronically and summed as a differential current I^2 . This is compared with a constant DC reference current I_{REF} to generate the error current $(I^2 - I_{REF})$, which is used to derive an amplitude error voltage ' V_G '. This is filtered and passed to the Amplitude Control circuits (page 11.6-1).

V_G is driven to zero by the action of the amplitude control loop, so that $I^2 - I_{REF} = 0$, and thus $I^2 = I_{REF}$. The loop therefore stabilizes only when the two are equal, and at a constant amplitude.

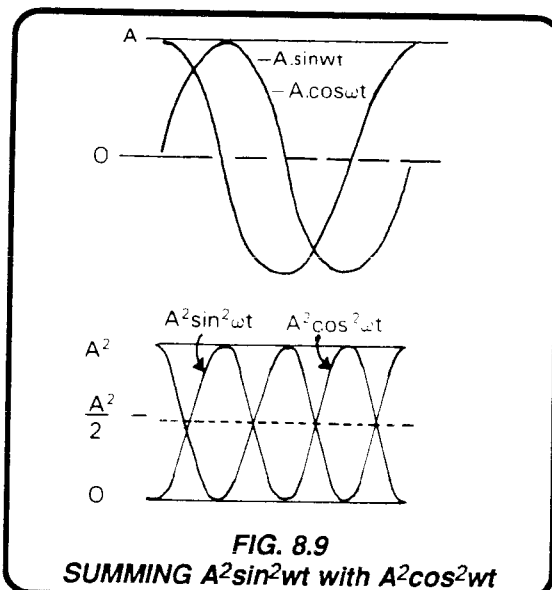


FIG. 8.9
SUMMING $A^2 \sin^2 \omega t$ with $A^2 \cos^2 \omega t$

8.2.8.1 Squaring Circuit Inputs (Circuit Diagram 430446 Page 11.6-1)

Vcos and Vsin are squared independently in a pair of differential four-Quadrant multipliers, each with two identical differential inputs.

The Sine Squarer receives Vsinwt from the second integrator M30 (Q44 emitter), and -Vsinwt from the main inverter (M15-11).

As +Vcoswt is the only natural cosine output from the oscillator, the -Vcoswt signal is derived by inversion in M31. These are both fed as inputs to the Cosine Squarer.

8.2.8.2 Cosine Squarer (Circuit Diagram 430446 Page 11.6-2)

Isolating the Cosine circuit alone as an example, there are two differential inputs. One is applied across M34 pins 13 and 16, and the other across pins 6 and 10.

The multiplying action of the squaring circuitry relies on the exponential transconductance between a transistor's base voltage and its emitter-collector current:

$$\begin{array}{l} I_c \text{ is proportional to } \exp(V_{be}) \\ \text{so } V_{be} \text{ is proportional to } \ln(I_c) \end{array}$$

The difference between the currents in M34-1 and M34-14 collectors is linearly proportional to Vcoswt (due to M34 emitter resistors AN15). The currents are drawn from the supply through Q55 (which is connected as two matched diodes), but because of the exponential transconductance, Q55 base-emitter voltages increase logarithmically with increase of emitter current. Therefore the differential voltage at Q56 and Q57 bases due to Q55 emitter currents is logarithmic:

$$(V_{Q55-4} - V_{Q55-3}) \text{ is proportional to } \ln(V_{\text{coswt}})$$

The difference between the currents in M34-9 and M34-7 collectors is also linearly proportional to Vcoswt (due to other M34 emitter resistors AN15). But each collector current is divided between the two halves of the dual transistor in its collector circuit, regulated both by the dual transistor's exponential transconductance, and by its logarithmic differential base voltage.

The combined effect of these two factors is similar to the mathematical operation of multiplying by adding logarithms: a term is produced in each Q56 and Q57 collector current, proportional to the linear product of the two input voltages.

By cross coupling the collectors of Q56 and Q57 as shown, other constant terms are suppressed, and the difference between the currents drawn from AN15-7/8 and AN16-9/10 is proportional to:

$$V_{\text{coswt}} \times V_{\text{coswt}}$$

The inputs are equal, so the differential output current is proportional to $V^2 \cos^2 wt$.

8.2.8.3 Sine Squarer

The Sine Squarer behaves in the same way, producing a differential current in its collector loads proportional to $V^2 \sin^2 wt$.

8.2.8.4 \cos^2 , \sin^2 and I_{REF} Summing

In this application, the currents from both Sine and Cosine Squarers are combined in common loads. The voltages developed across the loads will therefore also differ by an amount proportional to the expression $V^2 \cos^2 wt + V^2 \sin^2 wt$. Thus if a reference current was not superimposed, and utilizing the well-known identity ' $\sin^2 + \cos^2 = 1$ ', a DC voltage would exist between TP9 and TP10 (TP9 positive), equal to:

$$KV^2(\cos^2 wt + \sin^2 wt) = KV^2$$

where 'K' is a constant at constant temperature, dependent upon identical circuit values in both squarers, and 'V' is the amplitude of both sine and cosine outputs from the oscillator.

However, a reference current is superimposed. The DC current I_{REF} is drawn through the 1kohm load AN15 by M40 (pin 2), reducing the positive value of TP9 voltage to $(KV^2 - KV_{\text{REF}})$ with respect to TP10. (The reference current is established at a value which includes the scaling factor 'K', by D26 and R91. The value of R91 for correct oscillator amplitude is determined at manufacture). M34 is connected as a diode to compensate for M40 V_{be} temperature drift.

Voltage $K(V^2 - V_{\text{REF}})$ is applied to the input of M35a, the unity-gain Summing Amplifier. M35a is connected to remove any common mode present at its input, so at TP11, $K(V^2 - V_{\text{REF}})$ is referred to common 2A. At this point it can be recognized as the Amplitude Error Voltage. Moreover, the amplitude loop adjusts the oscillator outputs to drive the error voltage to zero, so the action of the loop also drives V^2 to equal V_{REF} .

8.2.8.5 Filtering

Because components cannot be matched exactly, some small differences can exist between the \sin^2 and \cos^2 terms. Such differences appear in V_G as the fundamental and second harmonics of the oscillator frequency. These are limited by filtering in the filter formed by M35b and its associated circuit.

It would be possible to set a single low-pass bandwidth for all ranges, but as this would need to filter down to 20Hz for the 100Hz range, it would also impose inconveniently long settling times for the higher frequency ranges. The low-pass bandwidth of the filter is therefore switched between frequency ranges by the R_{4-0} signals decoded from $\text{FREQ } R_{2-0}$ in the synthesizer (page 11.6-5).

The frequency range signals select the appropriate feedback components, by conduction of only one FET from Q47-Q52 per range. (Q48 is not used).

The filter output is the oscillator amplitude DC error signal ' V_G ', limited to a maximum of approximately 6V by the action of back-to-back clamp diodes D24 and D25. V_G passes via link B to the 'Amplitude Control' circuitry (see page 11.6-1). The value of V_G determines the fraction, and its polarity the phase, of the V_{coswt} signal which is to be added to V_{sinwt} at M15 input.

8.2.9 AMPLITUDE CONTROL IMPLEMENTATION

(Circuit Diagram 430446 Page 11.6-1)

Before describing the control circuitry, it is useful to review the various controls imposed on the oscillator (*see Figs. 8.4 and 8.7*):

- Frequency control by phase-locked loop to the frequency of the synthesizer output (albeit with a constant phase lag). This is effected by controlling the gain of the inverter stage of the oscillator. (Input resistance of M15 is changed by adjusting the conduction of FETs Q29.)
- Phase control to establish exactly 360° loop phase-shift by injecting a small amount of V_{coswt} into the oscillator inverter input (via R29).
- Amplitude control by adjusting the sense and amplitude of V_{coswt} added to V_{sinwt} , so that the loop gain is exactly unity at 360° loop phase-shift, at a constant output amplitude, and at the synthesizer frequency. (M23 gain is adjusted by varying the attenuation of its input signal, using FETs Q41_a and Q41_b.)

Amplitude error is corrected by adding a controlled fraction of either V_{coswt} or $-V_{\text{coswt}}$ to the V_{sinwt} feedback being applied to the main inverter M15. A push-pull control circuit is employed in order to adjust both amplitude and sense. V_{coswt} is input from Q31 emitter to R71, and its inverse is input to R70 from the output of M31, (which also provides the $-V_{\text{coswt}}$ input for the cosine squarer).

8.2.9.1 V_{coswt} Amplifier - M23

M23 is connected as a summing VCA, with a fixed feedback resistor R53. V_{coswt} and $-V_{\text{coswt}}$ are applied to opposite ends of its balanced input resistor chain R71, R65, R64 and R70. The center of the chain is the virtual ground of M23, so if the 'on' resistances of Q41_a and Q41_b are equal, the balance is not disturbed and M23 output voltage is zero.

When the Loop-gain Error is zero ($V_G = 0V$), the static conditions set approx. -3V bias on both FETs (depletion mode) to reduce crossover distortion. The FET gates are also bootstrapped by M24 and M25 to half the AC voltage between source and drain.

The DC conditions are:

| | | |
|------------------|----------------------------------|---------------|
| Q41 _a | Q46 emitter | - 0.75V |
| | M26 I_{in} | - 150 μ A |
| | M26 I_{out} | - 300 μ A |
| | Q41 _a V_{gs} | - -1.5V |
| Q41 _b | M32-6 | - 0V |
| | Q45 emitter | - -0.75V |
| | M27 I_{in} | - 150 μ A |
| | M27 I_{out} | - 300 μ A |
| | Q41 _b V_{gs} | - -1.5V |

Amplitude Error:

| | |
|-------|--------|
| M23-6 | - zero |
|-------|--------|

The Amplitude Error adjusts the 'on' resistance of Q41_a and Q41_b differentially, due to the inverter M32 in the side feeding Q41_b. In the case of a positive V_G of about 0.5V:

| | | |
|------------------|----------------------------------|---------------------------|
| Q41 _a | Q46 emitter | - -0.25V |
| | M26 I_{in} | - 50 μ A |
| | M26 I_{out} | - 100 μ A |
| | Q41 _a V_{gs} | - -0.5V (more conduction) |
| Q41 _b | M32-6 | - -0.5V |
| | Q45 emitter | - -1.25V |
| | M27 I_{in} | - 250 μ A |
| | M27 I_{out} | - 500 μ A |
| | Q41 _b V_{gs} | - -2.5V (less conduction) |

The output voltage at M23-6 is in the same phase as V_{coswt} , increasing with larger amplitude error.

For a negative V_G , M23-6 output voltage assumes the same phase as the $-V_{\text{coswt}}$ signal, increasing with larger amplitude error.

Transistors Q45 and Q46 act as voltage-to-current converters to drive the 'x2' current mirrors M27 and M26. Voltage reference diodes D20 and D22 provide the crossover bias. D21 and D23 provide clamping when Q45 and Q46 bases are driven positive, preventing V_{be} breakdown.

M23 output (now recognized as 'B.coswt') is summed with the basic oscillator feedback (V_{sinwt}) at the main inverter input (M15-5). When the amplitude is correct, and the loop phase is exactly 360°, M23 output is zero and does not inject any 'cos' component into the loop.

If the loop gain or phase is in error, then the squarers' output current is not equal to the reference current, V_G is not zero, and a small amount of cos component is fed into the loop. This adjusts the loop phase and gain to correct the oscillator amplitude.

8.3 EXTERNAL FREQUENCY LOCK

The External Frequency Lock allows the instrument output to be synchronized with an external reference frequency of either 1MHz or 10MHz (a tolerance of $\pm 1\%$ on these frequencies is specified).

The main use envisaged for this facility is for a user to improve on the $\pm 100\text{ppm}$ frequency accuracy of the instrument, by locking the internal frequency synthesizer to a customer's own frequency standard.

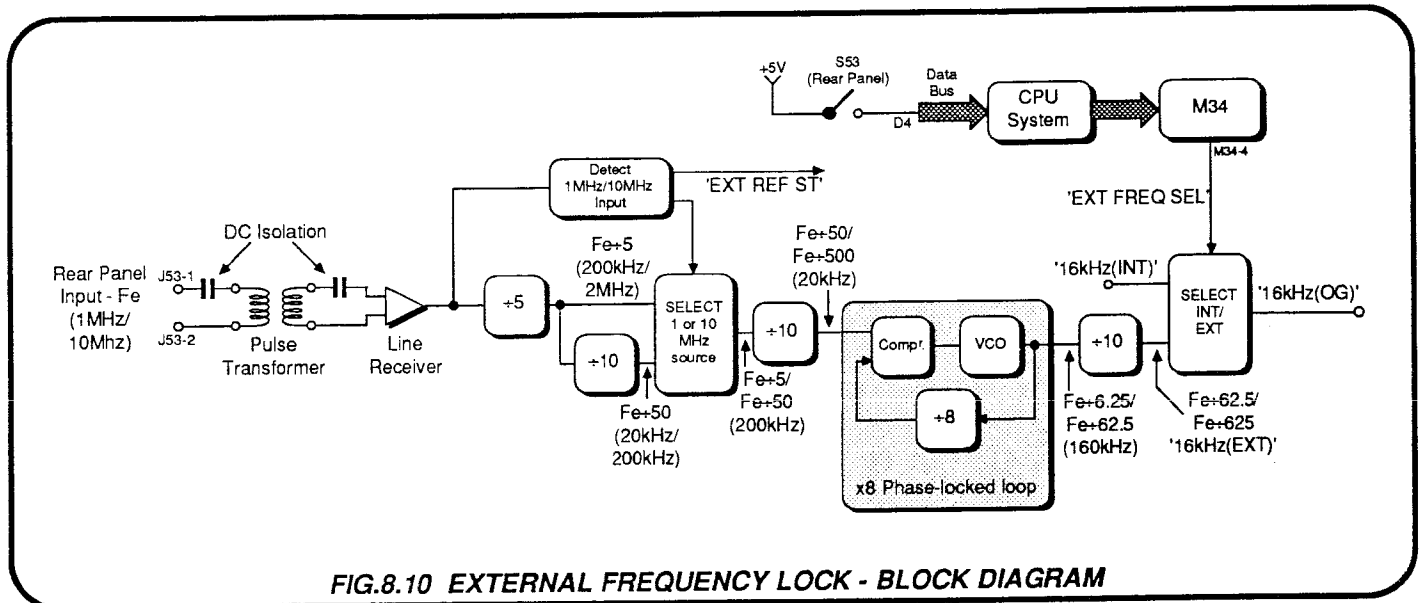


FIG.8.10 EXTERNAL FREQUENCY LOCK - BLOCK DIAGRAM

8.3.1 INTRODUCTION

The output sinewave frequency is synthesized in the Sine-Source assembly, normally synchronized to an internally-generated reference frequency of 16kHz. To lock the output to an external reference, it is necessary only to divide the frequency of the reference down to 16kHz and use this instead of the internal reference. The circuitry described in this sub-section is shown in block form in Fig. 8.10 and carries out the following functions:

- Isolates, limits and buffers the input reference signal to TTL levels.
- Divides the input frequency 'Fe' by 5 and then by 10 (Fig. 8.10).
- Detects whether the Fe is 1MHz or 10MHz; from this it sets the selector to choose either its +5 or +50 input, to give an output of 200kHz. The detector sets the status signal 'EXT REF ST' to Logic-1 whenever either of the two signals is present.
- Divides the selector output by 10, then multiplies by 8 in a phase-locked loop, finally dividing by 10 again to 16kHz to give the signal '16kHz(EXT)'.
- Selects either '16kHz(INT)' or '16kHz(EXT)' in response to the position of the Rear Panel switch S53, and to the presence of a 1MHz or 10MHz External Reference signal. The selected signal '16kHz(OG)' is transferred into guard by opto-isolator M3 on the Reference Divider assembly, and thence as 'REF FREQ' to the digital frequency synthesizer on the Sine Source assembly.

8.3.2 EXT REF SIGNAL INPUT

(Circuit Diagrams: 430830 Page 11.17-2;
430604 Page 11.16-4;
430648 Page 11.3-4.)

The External Reference signal of 1MHz or 10MHz enters the instrument via pins 1 (Hi) and 2 (Lo) of Rear-Panel connector J53 on the Interconnection assembly (page 11.17-2). It is transferred via J18 and J3 on the Mother assembly (page 11.16-4) to the buffer input circuit on the Analog Interface assembly (page 11.3-4).

C59 and R1 remove any DC components of the signal; and R15, D1 and D2 limit its excursions to approximately $\pm 0.7\text{V}$ before it is applied to the pulse transformer T1.

The output from T1 drives line receiver M9, C62 setting the DC offset to zero, and R16 providing some noise-immunity.

8.3.3 DIVISION CHAIN

8.3.3.1 '+5' and '+10' Counters M11

The line receiver output at TP24 clocks the +5 section of M11 counter. Its frequency is reduced to either 200kHz (for 1MHz input) or 2MHz (10MHz input), and this signal is used to clock the second (+10) section of M11. This section (and the other two +10 counters M28) is connected as a 'bi-quinary' divider to establish a symmetrical mark/space ratio. The frequency at M11-13 is either 20kHz (for 1MHz input) or 200kHz (10MHz input). The outputs from both counters are fed to the dual 4 into 1 line selector M18, which always chooses the 200kHz signal.

8.3.3.2 'EXT FREQ SEL'

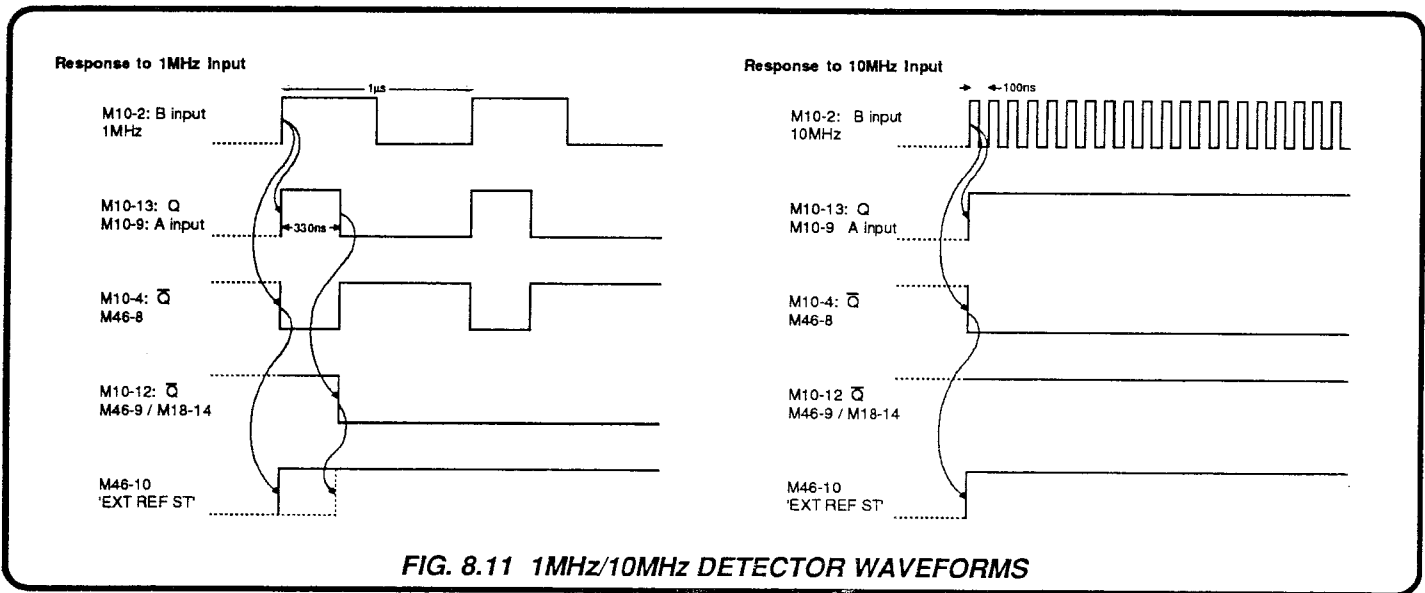
When S53 on the rear panel is closed to select External Reference, +5V from S53 enters the Digital assembly at J2-25 (page 11.2-2), setting line D2 on the Data bus to Logic-1 each time that M36 is enabled by any IRQ (ie. every 8ms in response to the internal signal RTC IRQ para 6.1.2.6). The CPU passes the information to the External Reference Buffer on the Analog Interface assembly via the Precision Divider Input Data Latches. The state of S53 is repeated at M34-4 (page 11.3-1) and input to M18-2 (B) to set M18 outputs.

8.3.3.3 1MHZ/10MHZ Detector M10

The state of the other input to M18 at M18-14 'A' depends on the frequency of the external reference signal at TP24, which is used to clock M10-2 'B'. Each positive-going edge triggers the first (330ns) monostable, initially setting M10-13 to Logic-1 (Fig. 8.11).

If the frequency is 1MHz, M10-13 times out and returns to Logic-0 before the next 1MHz trigger arrives, thus providing a train of negative-going triggers for the second (5.7µs) monostable at M10-9. The first negative-going edge sets M10-12 to Logic-0, but in this case each succeeding retrigger arrives before the monostable has timed out, and so M10-12 remains at Logic-0. The output from M10-12 drives M18 control input M18-14 (A).

If the frequency is 10MHz, M10-13 (330ns) cannot time out before the next retrigger arrives at M10-2, so it remains at Logic-1. No negative edges appear at M10-9 to trigger M10-12 to Logic-0, so the control input to M18-14 remains at Logic-1 as shown in Fig 8.11.



8.3.3.4 M18 Frequency Selections

The input sources to M18-10/11/12/13 are switched to M18-9 according to the following table. The *italicized* frequencies cannot

be obtained because it is **frequency** which controls the A input to M18:

| Reference Frequency | 'EXT FREQ SEL' M18-2 (B) | 1/10MHz Detect. M18-14 (A) | Source Transferred | M18-12 Frequency | M18-13 Frequency |
|--|--------------------------|----------------------------|--------------------|------------------|------------------|
| 1MHz | 1 | ∅ | M18-12 (2C2) | 200kHz | <i>20kHz</i> |
| 10MHz | 1 | 1 | M18-13 (2C3) | <i>2MHz</i> | 200kHz |
| No Input, or 10MHz (and Not Selected) | ∅ | 1 | M18-11 (2C1) | 0V | 0V |
| 1MHz (and Not Selected) | ∅ | ∅ | M18-11 (2C0) | 0V | 0V |

8.3.3.5 Further Division of M18 Output

The 200kHz output from M18-9 is divided by a further +12.5 before it becomes the signal '16kHz EXT'. This is achieved in three stages:

+10 (M28-3); x8 (PLL); +10 (M28-13).

The x10 dividers are connected as bi-quinary counters to maintain the symmetrical squarewave.

8.3.3.6 PLL Frequency Multiplier

The Phase-Locked Loop is formed by M30 and M53. The VCO oscillates at a frequency which when divided by 8 (M53-11) phase-locks to the 20kHz present at TP25. At this frequency (160kHz) the error voltage across C30 is a very low amplitude ripple balanced about 0V DC.

The loop can be regarded as a simplified version of the synthesizer VCO, described in *para 8.1.2.4*. The VCO output is low-pass filtered, then buffered and inverted by Q1 which drives the final +10 counter.

8.3.4 INT/EXT Reference Selection

The 16kHz (EXT) signal output from M28-13 is a symmetrical squarewave phase-locked to the External Reference frequency at TP27. It is passed into the same selector (M18) which carries out the 1MHz/10MHz and INT/EXT selection of the divided signal input. The 16kHz (INT) signal is also applied to M18. In this case the other half of the dual selector is employed.

The 16kHz(EXT)REF signal from TP27 is input via M18-3 and M18-4, whereas the 16kHz(INT) signal goes to M18-5 and M18-6. Switching between 1MHz and 10MHz (M18-14) has no effect, as the output at M18-7 selects from shorted input lines. The INT/EXT switching by EXT FREQ SEL (M18-2) selects between the two pairs of shorted inputs to give the 16kHz (OG) output from M18-7. This is buffered out via M5-6, J3-104 (*page 11.3-1*) and the Mother assembly to the Sine Source assembly at J6-53 (*page 11.6-4*).

8.3.5 'EXT REF ST' (M46)

If no external reference signal is present, both M10 monostables remain permanently in their relaxed (timed-out) state. Thus M10-4 and M10-12 are at Logic-1, both inputs to NAND M46 are Logic-1, so its output (EXT REF ST) is at Logic-∅. For signal frequencies of 1MHz or 10MHz one of the inputs to M46 is at Logic-∅, so EXT REF ST goes to Logic-1.

M46 output is returned to the CPU, being sensed on the data bus line D4 at each RTC IRQ (M37-13 *page 11.2-2*), so the CPU knows whether an external reference signal is present or not. It also knows when S53 is selected, and issues the 'Error EF' message on the MODE Display if S53 is selected but no external reference signal is present. This warns the user that with the external reference facility selected, the VCO in the Reference Buffer is free-running in the absence of a locking signal, and is still the reference for synthesis of the instrument output frequency. The output is thus unlocked both from the user's sync source and from the internal crystal oscillator. This is normally because no external reference has been connected to J53 on the rear panel!

SECTION 9 AC VOLTAGE OUTPUTS - AMPLITUDE CONTROL SYSTEM

9.1 INTRODUCTION

This complex system generates the whole range of AC voltage outputs, as defined by its inputs. For the AC Current function, an AC voltage is derived from the internal voltage amplitude loop on

the 1V or 10V range to act as an accurate reference. Thus the following description applies also to the generation of that reference.

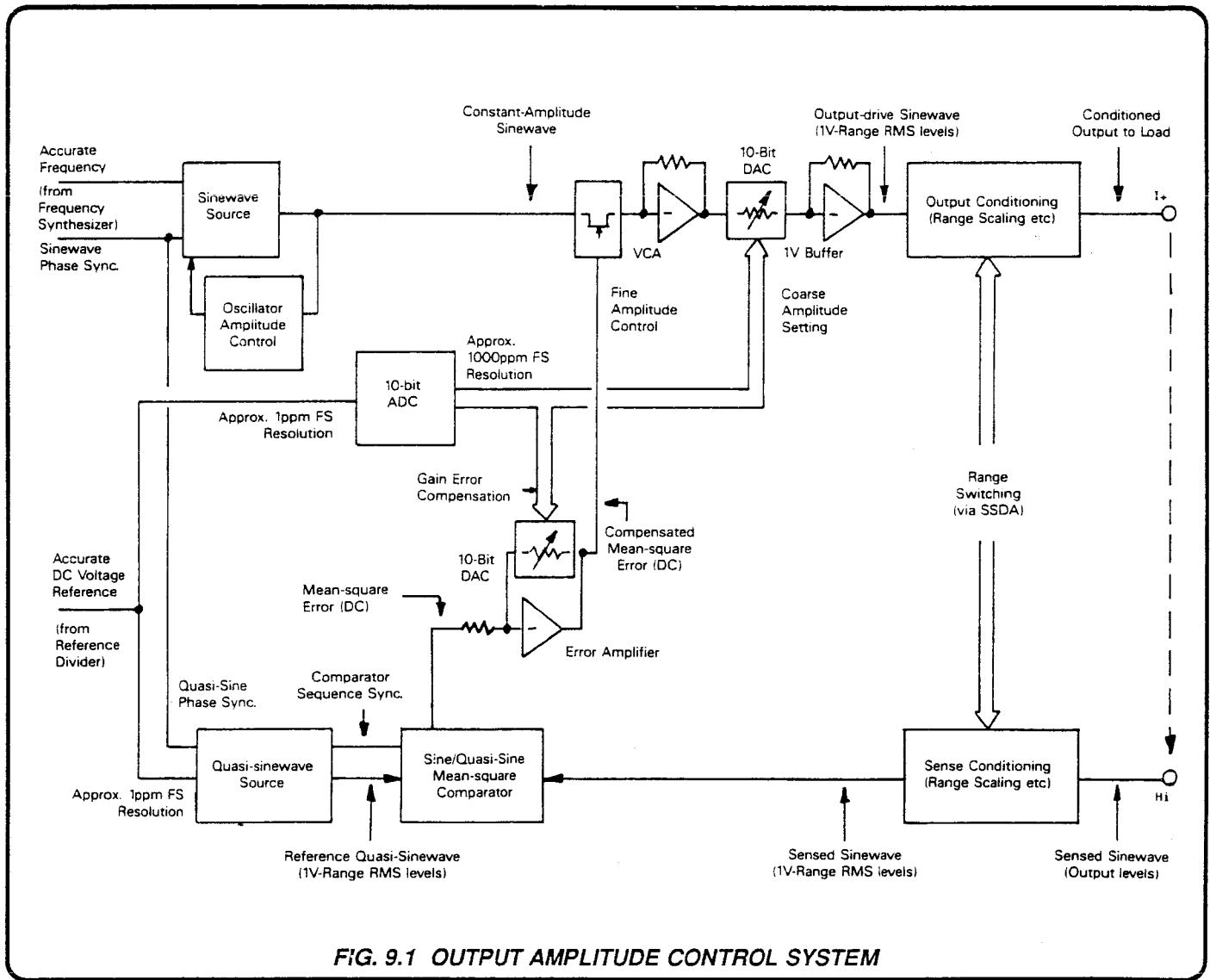


FIG. 9.1 OUTPUT AMPLITUDE CONTROL SYSTEM

| Feature of Output | Controlling Element | Controlling Input to Loop |
|-------------------|--|---|
| Frequency: | Frequency Synthesizer (Crystal-Sourced) | Constant-amplitude sinewave from Quadrature Oscillator |
| Sinewave Purity: | Quadrature Oscillator | Constant-amplitude sinewave |
| Voltage Range: | Processor, via SEDA and Control Latches | Ranging Signals |
| Coarse Amplitude: | Reference Divider | Accurate DC Reference Voltage (Resolution reduced to approx. 1000ppm FS by 10-bit DAC) |
| Fine Amplitude: | Reference Divider and Quasi-sinewave Generator | Quasi-sinewave RMS value at a resolution of approx. 1ppm FS |

9.2 AC VOLTAGE AMPLITUDE CONTROL SYSTEM - BLOCK DIAGRAM

(Fig. 9.1)

The system elements are described individually in the five sub-sections from 9.3 to 9.7. The system block diagram at Fig. 9.1

throws clear of the handbook, so that it can be used for reference when reading these descriptions.

9.2.1 FREQUENCY and WAVESHAPe CONTROL

Sinewave sourcing is the subject of *sub-sections* 8.1 (Frequency Synthesizer) and 8.2 (Quadrature Oscillator). The result is a high-purity sinewave of constant 1.9V amplitude, input to the VCA.

9.2.2 OUTPUT RANGING

The microprocessor passes Voltage and Current range selections into guard via the serial data link as described in *sub-section* 6.4.

This range information is held in the Analog Control latches in the Reference Divider Assembly, providing signals to the Output and Sense conditioning circuitry.

Their effects are described in *sub-sections* 9.4 to 9.6.

9.2.3 COARSE AMPLITUDE SETTING

The 1V Buffer also acts as a coarse amplitude control within each range. The value of its input resistance is adjusted to control its gain, which is incremented in steps of approximately 1000ppm of Full Scale by a 10-bit digital-to-analog converter.

The increments are defined by a 10-bit analog-to-digital converter, which responds to the accurate DC Reference voltages generated by the Reference Divider. The value of the 'DC Ref' voltage is proportional to the values set on the front panel OUTPUT display, as described in *sub-section* 6.5.

This coarse adjustment of output amplitude allows the fine control element (the VCA) to operate within a small dynamic range, minimizing introduced distortion and thus maintaining the high purity of the output sinewave. The operation of the coarse amplitude control is described in *sub-section* 9.3.

9.2.4 FINE AMPLITUDE CONTROL

9.2.4.1 Error Loop

The output amplitude is controlled within the coarse increments by an 'error' loop. The output is sensed at the load for 4-wire connections, or at an internal point in the forward path when 2-wire connection is selected (or imposed).

The sensed output is reduced to 1V Range RMS levels by the Sense Conditioning circuitry (as described in *sub-sections* 9.4 and 9.6), and its mean-square value is compared with that of the Reference Quasi-sinewave. The difference between the two values is expressed as a DC error, and fed to control the gain of the VCA.

Because the coarse amplitude control adjusts the error loop gain, and the error itself results from comparison with an amplitude analog, the gain of the error loop would not naturally be constant. Compensation is therefore applied to the error to reduce the loop gain in synchronism with increasing increments of coarse amplitude. (The Error Amplifier feedback resistance is reduced by a second DAC in step with the coarse amplitude ADC. The result is that the loop gain, and therefore the loop dynamics, are virtually linear.)

Details of VCA operation and error compensation are described in *sub-section* 9.3.

9.2.4.2 Mean-Square Comparator

When a value is set on the OUTPUT Display, it describes the RMS value of the output. From the displayed value the Reference Divider generates an accurate DC Reference voltage (stepping in increments of approximately 1ppm of Full Scale), which results in a quasi-sinewave whose peak voltage has the same value. (Thus at 1V Full Range output, the DC Reference voltage and the quasi-sinewave peak voltage are both 1.397V.)

The Crest Factor for any wave is defined as its Peak value divided by its RMS value. For a pure sinewave the figure is $\sqrt{2}$ (say 1.414), whereas the quasi-sinewave crest factor is 1.397. So for the same RMS value of 1V Full Range output, the quasi-sinewave input to the comparator has a peak value of 1.397V, against the sense feedback peak of 1.414V. The comparison is between mean-square rather than RMS values, but when the mean-square difference is zero, so is the RMS difference.

Generation of DC Reference voltage and Quasi-sinewave are described in *Section* 6.

9.2.4.3 Synchronization

The comparator is based on a sequence of squaring, integration, sampling and subtraction. Its operation and accuracy rely heavily on the synchronism of sinewave and quasi-sinewave, each state-change in the sequence occurring at zero-crossings of both waveforms. Thus both waveforms synchronize to clocks from the synthesizer, even when the sinewave is at a multiple of the quasi-sinewave frequency. The comparison sequence cycles once every ten quasi-sinewave periods.

Comparator operation and synchronization details are described later in *sub-section* 9.7.

9.3 VOLTAGE CONTROLLED AMPLIFIERS

(Circuit Diagram 430446, page 11.6-3)

The circuits described in this section perform the following functions:

- Modify the output of the Sine Source by coarsely tracking the gain of the output amplitude to the requested output voltage, providing stepped coverage of the instrument's dynamic range.
- Provide smooth adjustment of gain, within the coarse steps, in response to error signals from the Sine/Quasi-Sine Comparator.
- Impose the settling rate of the true analog DC reference voltage on both the coarse gain adjustment and the mean-square error (AC AMPL ERROR) scaling.
- Sense excess currents in the output buffer, providing a LIM ST signal to the CPU via the analog control interface.

All the circuits described in this section are located on the Sine Source Assembly. On the circuit diagram, two voltage-controlled amplifiers are shown:

- The 1 Volt Buffer (M45, M46 and the discrete output amplifier). Its input resistance is controlled by the DAC M43.
- The main VCA M48/Q88, whose input resistance is determined by the FET chain Q76 and Q77.

For a general description of the Output Amplitude Control System refer to *sub-sections 9.1 and 9.2.*

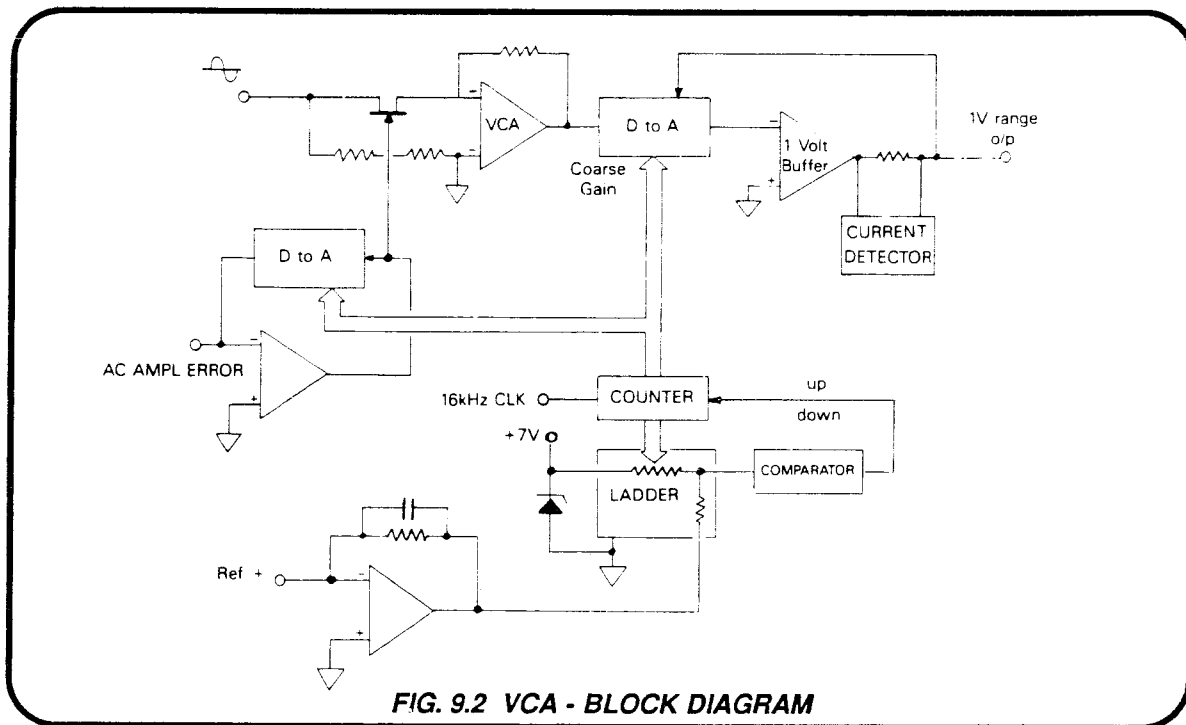


FIG. 9.2 VCA - BLOCK DIAGRAM

9.3.1 GENERAL (Fig. 9.2)

The main VCA receives a constant amplitude sinewave input from the Quadrature Oscillator (Sect. 8). Its gain is controlled by an error voltage, which is obtained by comparing the sensed sinewave output of the instrument with the reference quasi-sinewave.

The 1 Volt Buffer is included in the output signal path on all voltage and current ranges. It also acts as a VCA, since its input resistance is controlled by its 10-bit Digital-to-Analog Converter. The DAC receives its binary input from an Analog-to-Digital Converter, whose numerical output tracks the user's output demand, in increments of size approximately 1000ppm of full scale.

It is also necessary to ensure that the rate of coarse gain adjustment tracks the settling-time characteristics of the DC Reference filter. To

achieve this, the ADC is controlled by the level of the DC Reference voltage. The filtered reference's settling time is thus imposed on the ADC digital output, and hence on the 1V Buffer gain adjustments.

For reasons given in *sub-section 9.1*, it is also necessary to compensate the output loop gain error synchronously with the coarse gain steps. The tracking ADC therefore drives a second DAC, which selects values of feedback resistor in the Error Amplifier. This increments the output-amplitude error loop gain, modifying the AC AMPL ERROR signal which originated in the mean-square comparator.

The tracking ADC and its DACs ensure that the loop has the fastest possible settling time for any selected frequency.

9.3.1 VCA AND 1V BUFFER

The VCA and 1V Buffer combine in cascade to modify the amplitude of the sine wave output from the sine oscillator, accurately covering the instrument's dynamic range (see Section 9.1 and 9.2). The eventual output from the 1V Buffer (AC 1V FR) forms the instrument's basic 1V AC range.

9.3.1.1 Main Voltage-controlled Amplifier

(Circuit Diagram 430446 Pages 11.6-1 & 11.6-3).

The Sine Oscillator output from +2 buffer M47 (page 11.6-1) is emitter-followed by Q75 to the VCA FET input chain Q76/Q77 (page 11.6-3). These dual FETs are enclosed with M47 PTC feedback resistors R136 and R137, in a metal heatsink. The matched FETs Q76/Q77 ($R_{DS\ ON}$ within 1%) form the variable gain element for the low input-offset amplifier M48, to provide distortion-free and linear control of gain.

Each FET gate is current-bootstrapped from the divider AN18, to maintain a linear relationship between gain and input voltage. C106 and C117 drive the chain at HF. The center of the FET chain is also bootstrapped, M44 ensuring precise AC tracking. Resistors R143 and R135 divide and limit the maximum input resistance, preventing the gain from falling to zero.

9.3.1.2 The 1V Buffer

The buffer consists of a voltage follower with hard current limiting. Amplifiers M45 and M46 buffer the Class A power stage from the capacitance of the input DAC. The first buffer M45 has extremely high DC gain, rolling off at HF due to the feedback of C108. It removes the input DC offsets of M46.

M46 controls the buffer's AC performance; C112 ensures that the non-inverting input appears as a virtual AC ground at HF, allowing source-follower Q74 to develop the AC input across R159.

The discrete output stage provides class A current amplification, avoiding any cross-over distortion particularly at HF. Power transistor Q93 is provided with load and quiescent currents, from constant-current source Q94 (70mA) and constant-current sink Q86 (140mA). Refer to Fig. 9.3.

With zero input conditions Q94 is saturated, limiting the quiescent current at 70mA. Only the small bias current for Q92 flows in R144, so the output voltage is just +Vb.

The input signal to Q92 controls Q93, allowing a small signal transistor with good HF performance to adjust the large output currents flowing in R144.

Voltage amplifier Q92 conduction falls during positive half-cycles of input, reducing Q93 conduction. The quiescent current still flows in Q94, but part is now diverted through the output circuit via R144, R112 and L7.

During negative half-cycles of input; Q92 conduction increases, so Q93 conducts more heavily, drawing its extra (load) current through R144, and its quiescent current from Q94. The emitter of Q92 also attempts to go negative, drawing current directly from the load. The combined currents flow into the current sink, so Q86 must be able to sink 70mA quiescent + 70mA load.

The VCA gain is adjusted by the 'AC AMPL ERROR' signal, scaled by M41 and M42. The coarse gain scaling of the 1V buffer derives from the DC Reference voltage 'Ref+'.

The thermal linking to M47 feedback resistors compensates for the FET chain temperature coefficient. The inertia of the heatsink's thermal time-constant also prevents gain modulation due to draughts.

The DC signal 'AC AMPL ERROR' is scaled and then fed to each gate by transistors Q78 to Q81, which have low collector capacitance. The voltage control element formed by these transistors adjusts the DC gate voltages of the FETs in the chain, and hence the input resistance of the VCA.

M48 output is emitter-followed and passed through DC-isolating (and AC-compensating) capacitors C121 and C122 into M43, the 1V buffer DAC.

In the output line, inductor L7 and resistor R112 provide phase compensation for capacitive loading at HF.

If any components in the discrete amplifier are changed, re-adjustment of gain (using M48 feedback resistor R149) may be necessary.

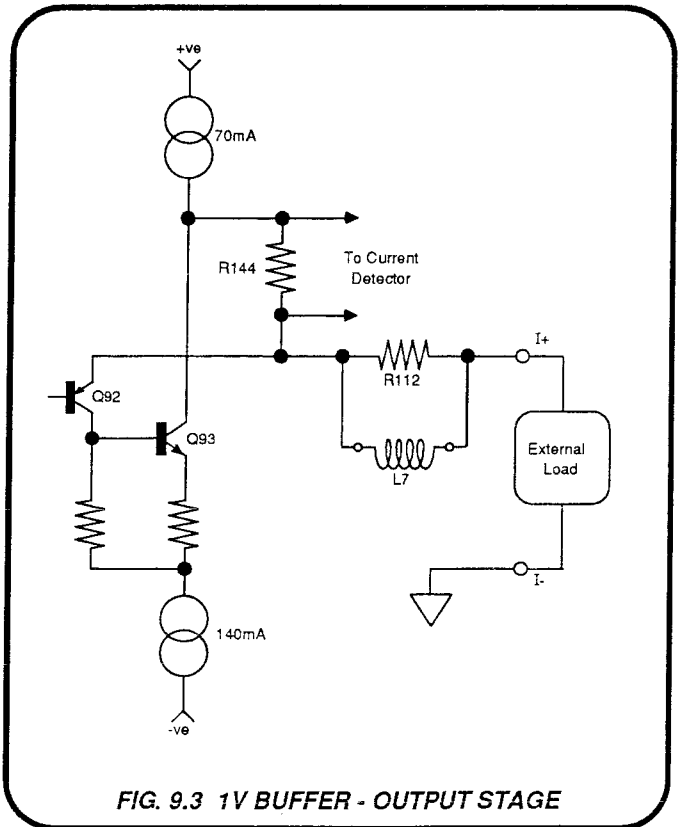


FIG. 9.3 1V BUFFER - OUTPUT STAGE

9.3.1.3 Current Detector

Except for a small bias current, all output current from the discrete buffer stage flows in R144, so the current level can be detected by sensing the differential voltage across it. This sense voltage rides on the output voltage; thus to capture it, the current detector is bootstrapped to the AC 1V output.

High-speed dual comparator M49 forms the basis of the Current Detector circuit. Its supplies are bootstrapped via TP29 to the junction of R144 and R112 in the 1V Buffer output. Q82 and Q84 provide constant current drive to 6.2V Zeners D40 and D41, with Q83 and Q85 providing the regulation for the bootstrapped rails at TP35 and TP36.

The comparator latching levels are set by dividers R151/R152 and R153/R154, their values allowing for bias current error in R144. The comparator's output is open-collector when the peak voltage across R144 is less than the positive or negative latch level. Line drivers Q90 and Q91 are cut off, so the LIM ST line at J6-70 is pulled to +15V by AN2 in the Reference Divider (page 11.4.4).

When the level is exceeded in either polarity, then either M49a or M49b output goes negative. This turns Q90 and Q91 on, pulling the LIM ST line to -15V (in-guard logic-0). The signal is passed to the CPU via the serial data link.

This limit is set much lower than the hard current limit of the buffer. If exceeded, the instrument displays 'Error OL', described in Section 2 (Fault Diagnosis). In overload at 35-40mA, a built-in margin of safety allows the instrument to meet most of its specifications.

9.3.2 ADC - DAC TRACKING

As mentioned earlier, it is necessary to track the coarse gain stepping rate to the settling time imposed by the DC Reference filtering. A tracking Analog-to-Digital Converter (ADC) is used to synchronize stepping, ensuring the fastest possible settling time at the selected frequency.

To set circuit conditions for the required output within a range, the gain of the main VCA is set in response to fine amplitude information, in the form of an error signal from the Sine/Quasi-Sine comparator. For constant output amplitude loop gain, the error loop gain also needs to track the coarse amplitude stepping.

For an outline of the Output Amplitude Control System, refer to the descriptions in sub-sections 9.1 and 9.2.

9.3.2.1 Use of 'REF+' (Circuit Diagram 430446 page 11.6-3)

The ADC requires a voltage input which tracks the value of instrument AC output demanded by the user, with settling times imposed by the Reference filter. The DC 'REF+' voltage exhibits these characteristics, so is used in this circuit to determine the numerical value of the ADC binary output.

'REF+' originates in the Reference Divider and is used to set the peak value of the quasi-sinewave in the AC assembly. Its value ranges from +0.126V at 9% of Full Range, through +1.397V at Full Range, to +2.794V at Full Scale.

REF+ is input to the Sine-Source assembly at J6-57 and J6-56, then applied to amplifier M41b, which is connected to remove any common mode present at its input. Thus at TP47, M41b output is referred to Common-2A.

Capacitors C99, C130 and C131 filter any HF pickup from the reference voltage, and M41b scales up the DC voltage levels by a factor of 2.43, to:

| | |
|------------------|------------|
| 9% of Full Range | : -0.306V, |
| Full Range | : -3.395V, |
| Full Scale | : -6.789V. |

A fixed positive version of this Full Scale value is also generated (Q66/D30/D31) as a reference for the tracking ADC M38 at M38-27.

9.3.2.2 Tracking ADC M38 (Fig.9.4)

M38 is a 'System DAC' which can be employed either in 'READ' or 'WRITE' mode. WRITE mode is not used for this function.

In READ mode the binary count can be output continuously from the ten pins DB₉₋₀. An internal 10-bit counter is clocked at 16kHz into pin 9 via level shifters Q53 and Q54. The counter can be controlled by two level-sensitive inputs: CONT 1 and CONT 2 (logic-1 = +5V; logic-0 = 0V) as follows:

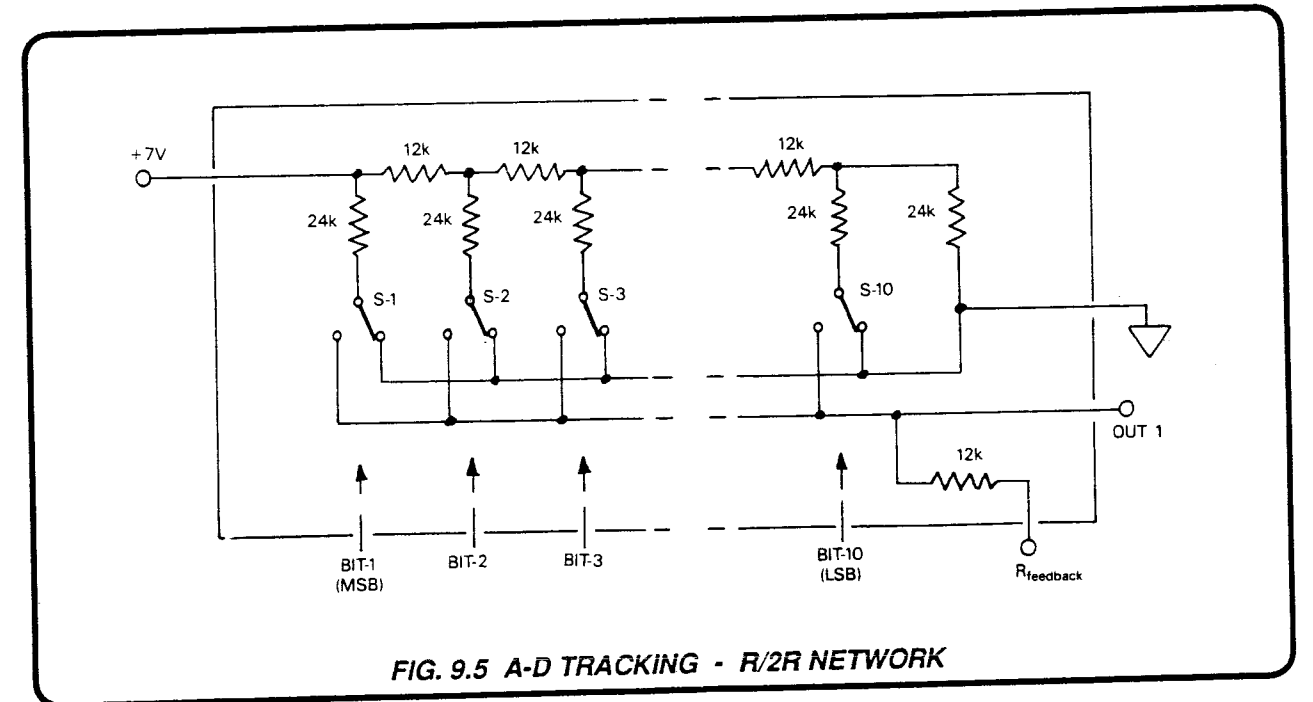
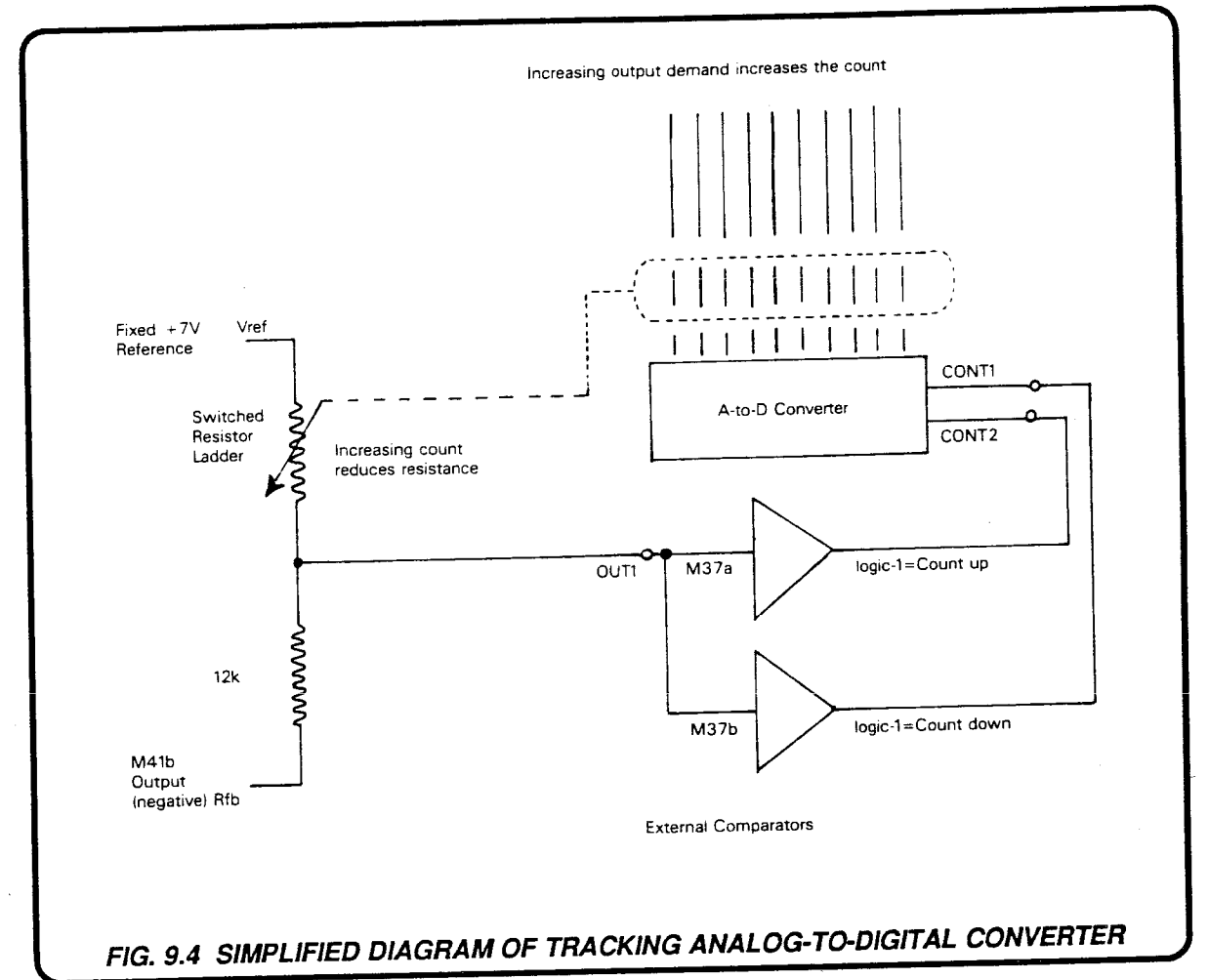
| CONT 1 | CONT 2 | Effect on Count |
|--------|--------|-----------------|
| 0 | 0 | not used |
| 0 | 1 | Incremented |
| 1 | 0 | Decrement |
| 1 | 1 | Frozen |

An internal 12kΩ reference resistor and switched resistor ladder form a divider between pin 27 (V_{REF}) and pin 1 (R_{FB}). Their junction is brought out to pin 2 (OUT 1). (See Figs. 9.4 and 9.5.)

The ladder is switched by the 10-bit counter. At zero count it is open-circuit; as the count is increased the ladder resistance reduces in inverse proportion, until at full count of 2¹¹ - 1 (corresponding to the instrument Full Scale output), it reaches its minimum of 12kΩ.

At Full Scale (FS) the M41b output voltage is -6.789V, into R_{FB}, and the fixed reference into V_{REF} is the positive version of this input, so at FS the OUT 1 voltage is balanced at zero.

For instrument output values below FS, the negative M41b output voltage is linearly reduced, so that the OUT 1 voltage tends to increase positively. By feeding an external comparator which drives the CONT 1 and CONT 2 counter controls, the OUT 1 voltage is used to provide automatic control of the count itself. In the case of a reduced output demand, a lower count is required to increase the resistance of the ladder, resetting OUT 1 to the zero balance.



9.3.2.3 Window Comparator

M37 is a high-speed dual comparator, which accepts OUT 1 as its input voltage, and controls the M38 counter via its CONT 1 and CONT 2 inputs. The 'Counter Freeze' condition of M38, resulting from both CONT inputs being at logic-1, allows hysteresis bias to be applied the comparator to create a 'Dead Band' window.

Each of the two outputs of M37 responds to its input in the same way: high impedance when its non-inverting input is more positive than its inverting input, and pulled low when the inverting input is more positive (uncommitted-collector).

M37a is connected as a non-inverting device, but M37b inverts its input. OUT 1 is input to both circuits. Both inputs are biased by approximately 15mV to generate the dead-band hysteresis: M37a by R96/R98, M37b by R100/R101.

9.3.2.4 Action for OUT 1 = Zero

Because of the bias, both M37 outputs are pulled low when the voltage at OUT 1 is zero. The inverting level-shifters Q67 and Q68 are both cut off by -15V on their gates, so CONT 1 and CONT 2 are at logic-1. M38 is thus put in the 'Freeze' condition, so its 10-bit output value is held.

In this condition, M36-12 and M36-13 inputs are both at -15V, so M36-10 is also -15V. R99 is therefore placed in parallel with R100, increasing the bias on M37b. The bias on M37a is also increased by Q69 being cut off, placing AN11 and R97 in parallel with R96. The 'Freeze' window is therefore widened, to improve the comparator's noise rejection. (Refer to Fig. 9.6.)

9.3.2.5 Action when OUT 1 Voltage Changes

When a user demands a new (greater) output from the instrument, REF+ increases as the Reference filter settles, and the OUT 1 voltage becomes more negative. The bias on M37b is eroded and finally exceeded, so M37-7 is placed at high impedance, pulled up to Common-2C by AN13. Q67 conducts setting CONT 1 to logic-0, which increments the count to step up the gain in the 1V Buffer.

Simultaneously, M36-12 is set to 0V (in guard logic-1). M36-10 rises from -15V to 0V, switching R99 to shunt R101 instead of shunting R100. Q69 conducts, switching R97 to shunt R98 instead of shunting R96. The bias levels shift back to 15mV, narrowing the hysteresis window.

If the user had demanded a lower output, OUT 1 would have become more positive, exceeding M37a bias. CONT 2 would have fallen to logic-0, decrementing the counter and reducing the 1V Buffer gain. The effect on the comparator bias would be the same as for the incrementing case.

As the counter changes its numerical value, M38's internal resistance ladder is switched to back-off the OUT 1 voltage. When REF+ finally settles, the OUT 1 voltage once again enters (and widens) the comparator's dead band. The count freezes, and the 1V Buffer gain remains constant.

Thus the OUT 1 voltage remains close to zero as the comparator and tracking ADC have a sensitive response to the variations of REF+; but once settled, the wider hysteresis window prevents the comparator from responding to noise.

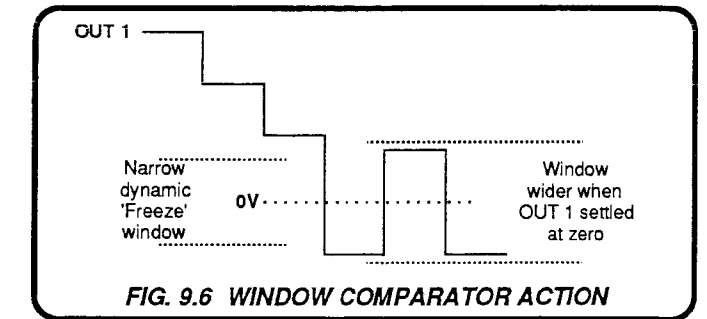
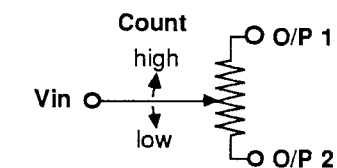


FIG. 9.6 WINDOW COMPARATOR ACTION

9.3.2.6 10-bit Digital-to-Analog Converters

M42 and M43 binary inputs are identically connected, so they both behave in the same way:



For low counts the resistance between Vin and O/P 1 is large, and small between Vin and O/P 2. The condition is incrementally reversed as the count increases to high values.

M43

As we have seen, an increase in user output demand increases the DC Reference voltage REF+, so a higher ADC count results. This reduces the resistance between M43 pins 15 (Vin) and 1 (O/P 1), and increases the resistance between Vin and O/P 2; increasing the gain of the 1V Buffer and thus increasing the instrument output. This is the stepped coarse gain adjustment referred to in sub-section 9.2.

M42

M42 has a different function. The fine adjustment of output value is incorporated in the 'Gain Error Loop', in which the output sinewave and quasi-sinewave are compared. This comparison generates the 'AC AMPL ERROR', to be used in controlling the VCA gain.

The error loop thus also passes through the 1V Buffer, and the effect of an increase in ADC count would be to increase the error loop gain, possibly overloading the VCA input FETs. This is prevented by reducing the gain of the error amplifier M41a, using M42 to track the steps of the coarse gain adjustment.

With an increase of the ADC count, M41a feedback is increased, as the resistance between M42 pins 15 and 1 is reduced. This reduces the error loop gain to compensate for the increase due to M43. Thus the fine gain remains virtually constant over the full span of coarse gain adjustment.

9.4 AC LOW VOLTAGE LOOP

The circuits described in this section perform the following functions:

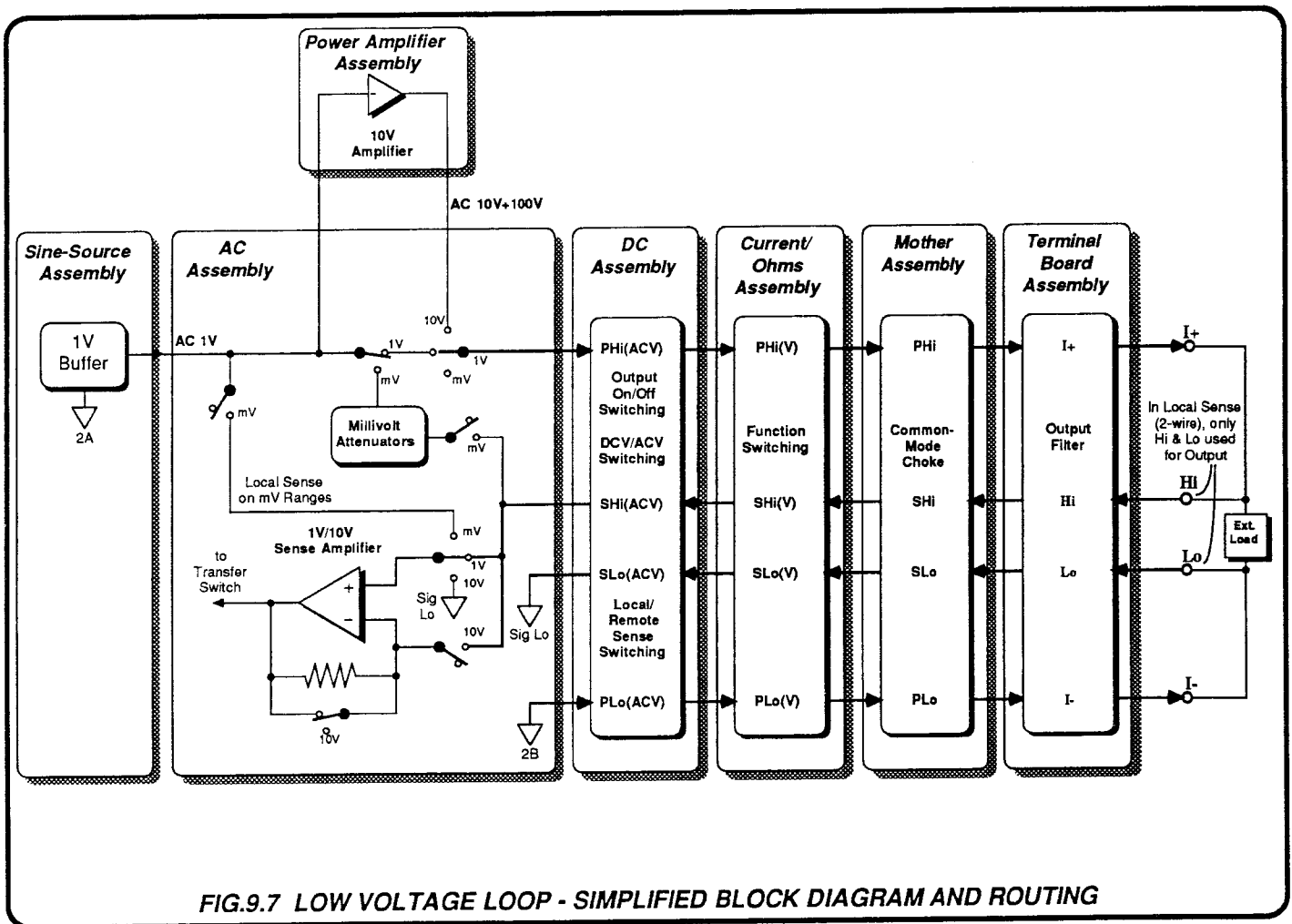
- Connect the VCA (1V buffer) output to the instrument's terminals to provide the **AC 1V Range: 0.09V to 2V**.
- Amplify the VCA output voltages and connect to the terminals for the **AC 10V Range: 0.9V to 20V**.
- Passively attenuate the basic AC 1V range voltages to provide the millivolt range outputs:
 - 9mV to 200mV** on the **AC 100mV Range**
 - 0.9mV to 20mV** on the **AC 10mV Range**
 - 90µV to 2mV** on the **AC 1mV Range**
- Sense the voltages at the output terminals (or at the load in Remote Sense) and scale the signal to the 1V RMS Full-Range level for comparison with the quasi-sinewave.

- Provide switching of AC voltage output, Range, Guard and Sense, under the control of signals from the Analog Control Interface.
- Detect excess currents in the output circuit, providing a status signal to the CPU via the Analog Control Interface.
- Detect excess voltages on the PHi (I+) output line, providing a status signal to the CPU via the Analog Control Interface.
- Switch the generated 10V range to the model 4600 analog control bus, as described in section 7.3.8. For clarity, these connections have been omitted from Fig 9.7

The circuits in this section are located as follows:

Millivolt attenuator and sensing: AC Assembly.
 Power amplification: Power Amplifier Assembly.
 Output control: DC Assembly.
 Output Terminals: Mother Assembly.
 Terminal Board.

A simplified block diagram of the low voltage loop and routing appears in Fig. 9.7.



9.4.1 GENERAL

The following description follows the 1V range path from the VCA buffer to the Sine/Quasi-Sine Comparator (at the input of the transfer switch M16). The 10V and millivolts outputs and sense conditioning are included, the outputs also being sourced from the 1V Buffer.

On the circuit diagrams, the relay contacts are shown in the un-activated condition.

For High Voltage output and High Voltage sense attenuation refer to Sections 9.5 and 9.6.

9.4.2 1V LOOP - POWER DELIVERY

9.4.2.1 Sine-Source Assembly

(Circuit diagram 430844 Page 11.6-3)

The 1V Buffer (page 11.6-3) is described in sub-section 9.3, as part of the output amplitude control circuitry. Its output sinewave, signal 'AC 1V' ranging between 0.09V and 2V RMS; is fed out of the Sine-Source assembly on J6-41, via the Mother assembly, and input to the AC assembly on J7-41 (page 11.7-1).

9.4.2.2 AC Assembly

(Circuit diagram 430663 Page 11.7-1)

With the 1V Range selected, relays RL7 (1V) and RL19 (1kV) are energized, but relays RL4, 5, 6, 17, 18 and 20 are not. Therefore the AC 1V signal is passed directly out of the AC assembly via RL7, fuse F1, RL19 and fuse F2 to become the Power-Hi signal 'PHI(ACV)' at J7-27.

The power common 'PLO(ACV)' is sourced from the in-guard Common-2 supply at the star-point Common-2B, passing out via the energized contacts of AC Voltage selector relay RL10, to J7-31.

PHI(ACV) and PLO(ACV) travel via the Mother assembly to the DC assembly at J5-25 and J5-29 respectively (Page 11.5-2).

9.4.2.3 DC Assembly

(Circuit diagram 430536 Page 11.5-2)

Output Switching

The PHI and PLO (ACV) connections are passed to the instrument output terminals via several relay contacts which provide switching for Remote or Local Sense, Remote or Local Guard, and Output On/Off.

If Option 20 is fitted, the terminal lines are switched for function changes on the Current/Ohms assembly. When Option 20 is not fitted, a Current/Ohms Link PCB (Part No. 410288) is fitted in place of the Current/Ohms assembly. This PCB provides direct connections for the signals, on their route to the instrument terminals.

ACV/DCV Switching

For AC voltage outputs, relays RL10 and RL11 are un-energized. The PHI(ACV) line for the 1V range bypasses the 1kV Range current sensing resistors R107 and R108, via contacts 7/10 of the un-energized relay RL13. It then passes directly via TP8, 1A fuse F6, and RL15 contacts (if output is set ON); to the PHI(V) line at J5-19.

When in Remote Sense, the power return line PLO(ACV) is linked from J5-29, via 1A fuses F4 and F3, RL14 and RL15 contacts to become PLO(V) at J5-23.

(For DC voltage outputs, the four ACV lines at J5-25/26/29/30 are disconnected by the Range relays and the ACV relay RL10 in the AC assembly).

9.4.2.4 Connections to the Terminals

(Section 7)

The PHI(V) and PLO(V) lines are routed to the I+ and I- terminals on the front panel exactly as for DC 1V Range outputs.

Descriptions of the processing and routing can be found in the following sub-sections of Section 7:

| | |
|------------------------|---------|
| Output On/Off: | 7.3.6.2 |
| Remote Sense: | 7.3.6.3 |
| Remote Guard: | 7.3.6.4 |
| Overvoltage Detection: | 7.3.7.2 |
| Output to Terminals: | 7.3.8 |

9.4.3 AC 1V LOOP - OUTPUT SENSING

The SHI(V) and SLO(V) lines are routed from the Hi and Lo terminals on the front panel exactly as for DC 1V Range outputs.

The processing and routing back to the DC assembly is described in *Section 7, sub-sections 7.3.9.1 to 7.3.9.3.*

9.4.3.1 DC Assembly

(Circuit diagram 430536 *Page 11.5-2*)

In normal 4-wire operation (Remote Sense selected) with OUTPUT 'ON' on the AC 1V Range, relays RL14 and 15 are energized; RL10 and 11 are un-energized.

SHI(V) enters from the Mother assembly at J5-20, passing directly through RL15 contacts, TP9 and R98, to J5-26 as SHI(ACV).

SLO(V) travels via RL15 contacts and TP10 to J5-30 as SLO(ACV).

With Remote Sense not selected, relay RL14 is unenergized:
RL14-9/8 short SHI(V) to the power Hi output PHI(V).
RL14-2/3 short SLO(V) to the power Lo output PLO(V).

SHI(ACV) and SLO(ACV) are routed from J5-26 and J5-30 via the Mother assembly to the AC assembly.

9.4.3.2 AC Assembly

(Circuit diagram 430844 *Page 11.7-1*)

SLO(ACV) passes via the energized contact of the AC Voltage selector relay RL10, to be referred to the Sine/Quasi-Sine comparator transfer switch common 'SIG LO'.

With the 1V Range selected, relay RL19 ($\overline{1kV}$) contacts are closed, so SHI(ACV) appears at RL19-11 as 'SENSE Hi'. (Refer to the circuit diagram on *page 11.7-2.*)

With the 1V Range selected, relay RL8 (1V) is energized, thus SENSE Hi is applied to the non-inverting input of the Sense Amplifier via R126. RL14 is un-energized as shown, so the inverting input via R115 is referred to SIG LO.

RL3 ($\overline{100V+1kV}$) is energized, connecting the Sense Amplifier output to the Sine/Quasi-Sine comparator transfer switch M16-11 (*page 11.7-3*). The amplifier is described in *sub-section 9.4.4.*

9.4.4 AC 1V SENSE AMPLIFIER

(Circuit Diagram 430844 *page 11.7-2*)

The same amplifier is used on the 10V, 1V, 100mV, 10mV and 1mV AC Ranges. Its main purpose is to buffer the sense voltage, providing a high impedance input, low DC offset and flat frequency response.

On the AC 1V and millivolt ranges it is connected as a voltage-follower, sensing always being carried out at the 1V level. The 1V Range sense signal originates at the load in remote sense, or in the DC assembly in local sense.

For the millivolt ranges the 'AC 1V' drive signal to the millivolt attenuators is sensed directly (*see sub-section 9.4.5*).

On the AC 10V range an inverting configuration is employed. The circuit divides by 10, scaling the sense signal down to 1V range levels, for input to the Sine/Quasi-Sine comparator.

Separate arrangements are made for attenuation and scaling on the 100V and 1kV AC ranges. These are described in *Section 9.6.*

9.4.4.1 General Arrangement

A discrete amplifier is used to provide the required slew rate up to 1MHz, all time constants being set well above 1MHz, with the first pole above 5MHz. It is configured into its follower circuit by relay switching.

Relays RL8, RL12 and RL3 are all energized on the 1V range. Relays RL11, RL13, RL14, RL15 and RL16 remain un-energized as shown in the diagram.

Dual JFET Q41 is a unity gain buffer in totem pole configuration. It drives the input protection diodes D37-D40, D44-D47; the screen on Q40 inverting input; and the bootstrap buffer Q46. The total input capacitance is thus reduced to 1-1.5pF.

The differential input amplifier, dual FET Q40, has low input capacitance and low input current. Q36 provides constant-current drive to Q40 and the bootstrapped followers Q38/Q39. R107 permits initial DC input-offset cancellation. The stage gain is low.

Emitter-followers Q34 and Q35 buffer the high-impedance low-gain FET stage, driving a differential signal into the high gain voltage amplifier Q29/Q30. This arrangement has the advantage of placing all the gain in one stage. The single-ended drive to Q31 output stage is taken from Q30 collector.

Q24 and Q25 form a current mirror to equalize the collector currents of Q29 and Q30, preventing signal injection into the sense amplifier power rails.

L6 and L7 isolate the amplifier power rails from the 15V supply at HF. C50 is the main frequency-response compensation capacitor, providing smooth roll-off, with unity gain at around 5MHz.

On the 1V Range, the output from Q31 is returned at low impedance, as 100% negative feedback to the amplifier input, via the closed contacts of RL12-8/14.

9.4.5 MILLIVOLT LOOP

(Circuit Diagram 430844 pages 11.7-1 and 11.7-2)

The basic 1V loop is extended by inserting a switched, passive, attenuator network. The switching circuit connects the selected millivolt output via RL4-13/9 and RL19-11/8 directly to the SHI(ACV) line, not 'PHT'. Thus only the two front panel Sense Hi and Lo terminals are used to connect to the load.

The software forces Remote Sense OFF in the millivolt ranges. Except for a series resistor (R154) on the 1mV range, the AC 1V signal is connected directly to the input of the Sense Amplifier via

RL11-4/5 at RL8-13. The amplifier circuit remains permanently in its non-inverting configuration for all three millivolt ranges, so local sensing is carried out at 1V range levels.

Thus the output value at the terminals depends on both the calibrated value of the AC 1V signal and the division ratio of the attenuator. In addition to the 1V range calibration, each millivolt range is also 'Autocalibrated' separately (refer to Section 1).

9.4.5.1 Millivolt Attenuators

(Fig. 9.8)

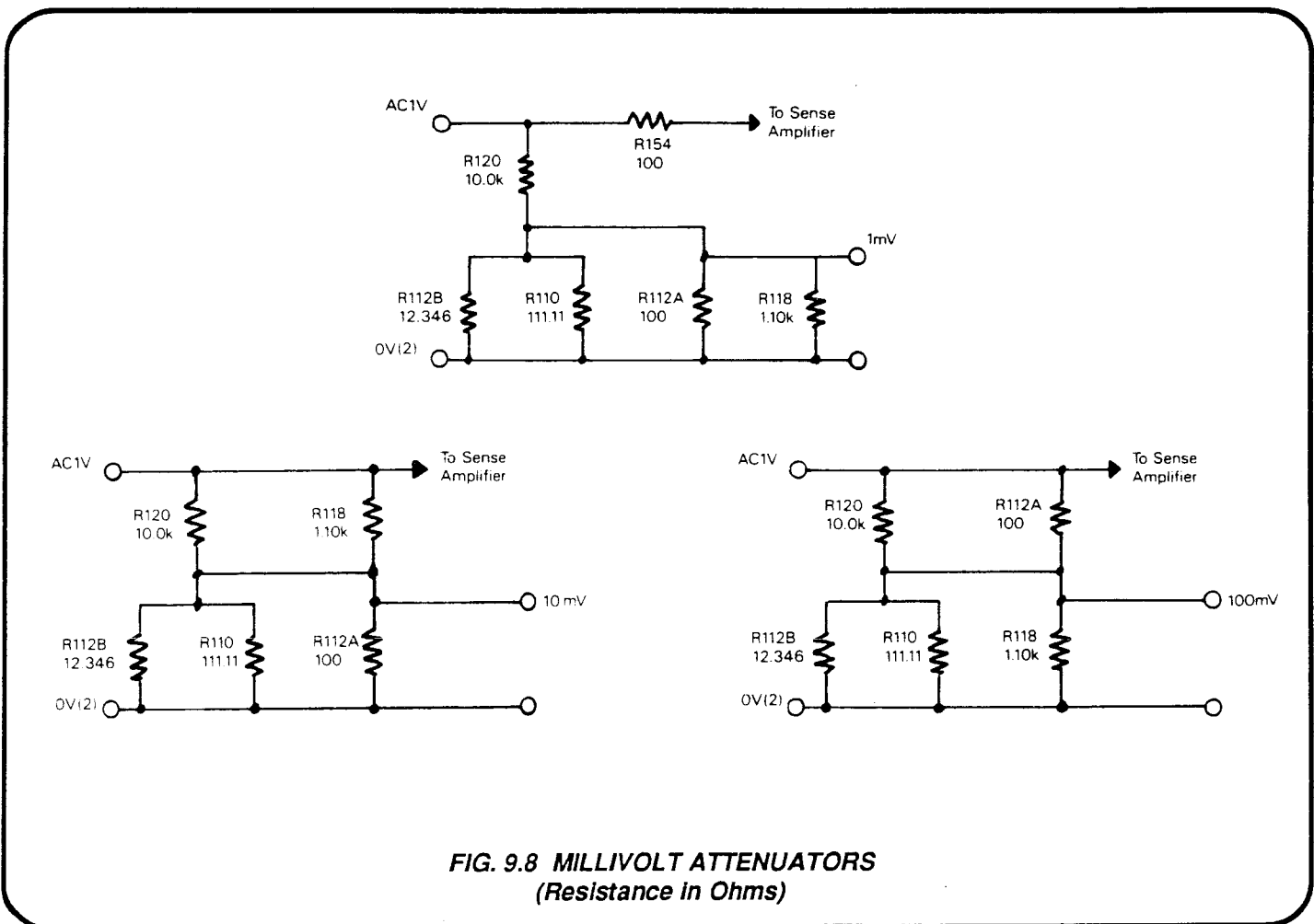
The AC 1V signal is diverted from its 1V range route by contacts 13/11 of un-energized relay RL7, and applied to the attenuator network.

The fixed chain (formed by R120 in series with the parallel combination of R112B and R110) is permanently connected between RL7-11 and the Common-2 star-point. Three levels of attenuation are achieved by switching R112A and R118. Relay RL5 is energized for the 10mV range only, RL6 for the 100mV range.

On the 1mV range, the series resistor R154 is connected between RL7-11 and the Sense Amplifier input via RL11-5, but it is shorted on the 10mV and 100mV ranges by the closed contacts of RL5 and RL6 respectively.

Relay RL4 is energized on all millivolt ranges. The attenuator output is passed out via RL4-8/9 and RL19-11/8 to the SHI(ACV) line. C89 defines the specified bandwidth, filtering noise at HF.

The three arrangements are shown in Fig. 9.8.



9.4.6 10V LOOP

(Circuit Diagrams: 430446 page 11.6-3, 430618 page 11.9-1/2 and 430844 page 11.7-1)

As noted in *sub-section 9.4.1*, the 1V Buffer is part of the power delivery system for all ranges. On the 10V range its output (AC 1V) passes via J6-41 from the Sine-Source assembly and into the Power Amplifier assembly (PA) at J9-36 (*page 11.9-2*).

The AC1V signal is amplified by a factor of 10 in the inverting 10V Power Amplifier, whose output is placed on the 'AC 10V+100V' line. This 10V range signal returns to the AC assembly at relay contacts RL17-13/4. It passes through RL19-2/5 to the PHI(ACV) line at J7-27.

The 10V range outputs then follow the same route (to and from the output terminals) as the 1V signals. Whether in Remote Sense or not, the sensed voltages return via the SHI(ACV) line to the same Sense Amplifier used for 1V range signals.

With 10V range selected, the sense amplifier has an inverting gain of 0.1, returning the signal to the 1V Range levels required by the Sine/Quasi-Sine comparator.

9.4.7 10V POWER AMPLIFIER

(Circuit Diagram 430618 page 11.9-2)

The AC 1V signal enters the PA assembly at J9-36, passing to the input of the 10V Amplifier via relays RL4-9/13 and RL3-9/13. It is referred to Common-2B by developing a voltage across R124.

The amplifier has already been described for the DC 10V Range; in this text, the effects on the 10V AC Range of its separate DC and AC paths are considered below.

9.4.7.1 DC Path

The DC path is blocked by C56; M17 is the DC input amplifier, connected as an integrator with diode clamping. M19 operates as an inverter in open loop, so applies high DC gain to the output from M17 on M19-2.

The output from M19 drives both halves of the symmetrical, inverting, discrete power amplifier through current-limiters Q21 and Q24, and is buffered by emitter-followers Q22 and Q23. Common-emitters Q27 and Q29 form a voltage amplifier, driving the complementary output stage Q32 and Q33. Input and feedback resistors R119 and R120 set the gain of the discrete stages to approximately 4.5.

The forward amplification contains three inversions, DC negative feedback being applied to M17 inverting input by R122, defining an overall gain of 10 in conjunction with input resistor R123.

The DC path senses and corrects the DC offsets throughout the whole AC amplifier, referring the output to Common-2A at M17-3.

9.4.7.2 AC Path

The AC path is blocked by the integrator M17, but is applied to the non-inverting input of M19 through the coupling capacitor C56. M19 operates in open loop, applying its output to the discrete power amplifier (*see 9.4.7.1 above*).

The amplifier AC gain is also set to 10 by R122 and R123, the circuit time constants being selected to allow overall instrument output operation over the full frequency range of 10Hz to 1MHz.

9.4.7.3 Power Supplies

M17 and M19 are supplied from $\pm 15V$ common-2A rails, but the discrete amplifier receives power from the $\pm 38V$ supply.

9.4.7.4 Overload Detection

The $\overline{10V\ FLAG}$ line, connected to TP12, is pulled up to 0V (in-guard logic-1) in the Reference Divider assembly (*page 11.4-4*) by AN2-9/1 (1M Ω). The Error OL message results from this line being driven to logic-0.

RL8 is energized for the AC 10V Range, so overload detector Q31 reaches V_{be} threshold on output current peaks, when the RMS value in R139/R172 and R141 exceeds approximately 80mA. Similarly, Q34 detects peak currents in R147 and R149/R173. In either case, Q34 conducts, pulling TP12 down to -15.7V. The $\overline{10V\ FLAG}$ line is driven to logic-0, so the status message is returned to the CPU via the SSDA serial interface, and the Error OL message is displayed.

This does not preclude further increase in output current, but the accuracy specification is not guaranteed.

9.4.7.5 Overload Limiting

If the RMS output current increases to approximately 100mA, the peaks of current cause the V_{be} threshold of Q28 or Q30 to be exceeded, shunting the base current of the corresponding voltage amplifier. This hard-limits the output drive to the final stage.

9.4.7.6 Output Protection

The output current passes through the combination of R144 and L8. At low frequencies the inductor provides a low output impedance, whereas at high frequencies the resistor stabilizes the amplifier when driving capacitive loads.

9.4.8 10V SENSE AMPLIFIER

(Circuit Diagram 430844 page 11.7-2)

9.4.8.1 General

A common sense amplifier is used for the 10V, 1V, 100mV, 10mV and 1mV Ranges. Its main purpose is to buffer the sense voltage, providing a high impedance input, low DC offset and flat frequency response.

The operation of the Sense Amplifier for the AC 1V and millivolt ranges, is described in *para 9.4.4.1*. For these ranges it is connected as a voltage-follower.

The AC millivolt ranges' outputs are simply the AC 1V range after passive attenuation; these levels are not sensed directly. The AC 1V signal is sensed before attenuation.

On the 10V range an inverting configuration is employed. The circuit divides by 10, scaling the sense signal down to 1V range levels, for input to the Sine/Quasi-Sine comparator.

Separate arrangements are made for attenuation and scaling on the 100V and 1kV ranges. These are described in *sub-section 9.6*.

9.4.8.2 10V Range Configuration

On the 10V Range, relays RL14 and RL3 are both energized. Relays RL8, RL11, RL12, RL13, RL15 and RL16 remain un-energized as shown in the diagram.

The 'SENSE HI' signal is routed to the inverting input of the amplifier through the closed contacts of RL14 and resistor R115. With relays RL8 and RL11 not energized, the non-inverting input is referred to SIG LO.

The output from Q31 is returned via R121 as negative feedback to the amplifier input, the contacts of RL12-8/14 being open.

Thus the circuit is configured as an inverting amplifier, resistors R115 and R121 scaling the sense signal down by a factor of 10. Extensive screening is employed at the amplifier's virtual ground, bootstrapped by buffers Q46 and Q41 to follow the virtual-common potential. This reduces the input capacitance, which is further compensated by feedback capacitor C60.

9.5 AC HIGH VOLTAGE LOOPS

The instrument includes two high voltage AC ranges. The 100V ranges extends from 9V to 200V full scale, the 1000V range from 90V to 1100V full scale.

Circuit Diagrams 430844 page 11.7-1 and 430618 page 11.9-1 together illustrate the high voltage AC circuit arrangement and indicate signal flow. The details of the 100V and 1000V ranges are described in *sub-sections 9.6 and 9.7*.

9.5.1 AC HIGH VOLTAGE DELIVERY

Both ranges employ the same precision sinewave oscillator and VCA arrangement used for the 1V AC Range, but the techniques necessary to generate high voltages differ from those in the low voltage loops:

- **On the 100V range**, the AC 1V signal is switched directly into the 100V Amplifier, where it is scaled up by a factor of 100, the amplifier output being delivered via the 'AC 10V+100V' line to the PHI(ACV) line on the AC assembly.
- **For the 1000V range** the DC Reference is scaled in software, so that the AC 1V signal Full Scale value represents 1100V output. The signal is routed through extra stages of amplification before being applied to the 100V Amplifier, whose output now drives one of two 1:6 step-up transformers (LF or HF). The power-amplifier gain on the 1000V range is controlled by feedback from the transformer secondary, into the input of the 1000V Error Amplifier. The 'AC 1kV' line transfers the transformer output to the AC assembly, where it is switched onto the PHI(ACV) line.

9.5.2 AC HIGH VOLTAGE SENSING

Guarded high-voltage precision attenuators reduce the AC sense voltage from the Hi and Lo terminals to 1V Range levels. The attenuated voltage is compared with the quasi-sinewave voltage, their mean-square difference being used as an error signal to correct the range output level by controlling the gain of the VCA.

9.6 AC 100V RANGE

9.6.1 INTRODUCTION

(Circuit Diagram 430618 *page 11.9-1*)

The AC 1V signal, generated by the 1V Buffer in the Sine-Source assembly, enters the Power Amplifier as for the 10V range; but the 10V Amplifier is bypassed for the high voltage ranges.

On the 100V range, the signal is switched directly into the 100V Amplifier, where it is scaled up by a factor of 100, the amplifier output being delivered via the 'AC 10V+100V' line to the PHI(ACV) line on the AC assembly. Thereafter the output is transferred to the instrument terminals as for the 10V range.

9.6.2 AC 100V RANGE POWER ROUTING

(Circuit Diagrams: 430618 *pages 11.9-2 and 11.9-3*;
430844 *page 11.7-1*)

'AC 1V' enters the Power Amplifier assembly at J9-36 (*page 11.9-2*). Relay RL3 is un-energized, shorting the 10V Amplifier input; and RL4 is energized, routing the AC 1V signal to the 100V Amplifier as '100V I/P' (*page 11.9-3*).

Relay contacts RL2-8/4 apply the signal to the Gain Stage, which provides drive to the power amplifiers in the positive and negative heat sinks, via J3-12 and J3-11. The single-ended output from the heatsinks at J3-9 passes via R89, L7 and relay RL2-13/9, to RL3-6 (*page 11.9-2*), and onto the 'AC 10V+100V' line via RL4-4/8.

On the AC assembly (*page 11.7-1*), the signal is routed to the PHI(ACV) line as for the 10V range.

9.6.3 100V AMPLIFIER

The AC 1V signal enters the PA assembly at J9-36, passing to the input of the 100V Power Amplifier via closed relays RL4-9/13 and RL2-8/4. It is referred to Common-2B by developing a voltage across R72.

The 100V Amplifier is described in *Section 7.8*, which deals with the 100V DC outputs.

The description is sub-divided as follows:

| | |
|--------------|------------------------------------|
| 7.8.3 | 100V Amplifier Introduction |
| 7.8.3.1 | Input to Gain and Driver Stages |
| 7.8.3.2 | DC Offset Correction |
| 7.8.3.3 | Signal Processing |
| 7.8.3.4 | Driver Regulator |
| 7.8.3.5 | Driver Output |
| 7.8.4 | 100V Power Amplifier |
| 7.8.4.1 | Positive Heatsink Assembly |
| 7.8.4.2 | Negative Heatsink Assembly |
| 7.8.4.3 | Over-Temperature Detection |
| 7.8.4.4 | 100V Output Connection |
| 7.8.4.5 | Heatsink Removal |

9.6.4 POWER SUPPLIES AND PROTECTION

The power supplies and protection for the 100V Amplifier are also described in *Section 7.8*.

The description is sub-divided as follows:

7.8.5 Power Supplies and Protection Introduction

7.8.5.1 38V Supply

(The 38V supply circuit is also described in *Section 6.7, para 6.7.3.4.*)

7.8.5.2 400V Transformation and Rectification

7.8.5.3 400V Current Control

7.8.5.4 100V Current Sense and 1kV Overvolts Detector

(This detector circuitry is used only for AC High Voltage ranges, and is therefore described in *sub-sections 9.6.4.1 and 9.7.6.1 below*).

7.8.6 PA Power Supply Monitors

7.8.6.1 Comparator Supply Protection

7.8.6.2 15V Monitor

7.8.6.3 38V Monitor

7.8.6.4 400V Monitor

9.6.4.1 100V Current Sense

(Circuit Diagram 430618 *Page 11.9-6*)

The 400V(2)B lines enter the Power Amplifier assembly from the PS/I Heatsink at J1-8/6 and are filtered by L1 and L2 before being applied across two neon lamps LP1 and LP3. These lamps are visible from the top and rear of the instrument when the PA board is exposed, indicating that a dangerous voltage is present.

The 400V(2)B lines continue on to power the driver stage of the 100V amplifier, where the voltage is regulated as described in *para 7.8.3.4*.

The 400V(2)C lines supply the power amplifier in the Positive and Negative Heatsinks. On the 100V range, the current in each of these lines is used as an analog of the load placed on the amplifier.

(On the 1000V range, any overload is sensed by a series detector in the DC assembly.)

The '100VAC' line is set to logic-1 (0V) only when the 100V range is selected. Driver Q7 pinches off the FET switch Q6, removing the short from R37, thus allowing the overload detector to operate. In normal use, links LKB and LKC are not connected. Their test purpose is to allow the current mirrors Q1 and Q3 to be powered without the level-shifters Q2 and Q4.

Most of the positive output current for the heatsinks passes through the series combination of R34 and D27, the negative currents through R9 and D4. As the both positive and negative circuits are symmetrical, only the positive circuit is described.

Current mirror Q3 diverts approx. 1.8% of the positive supply current into the level-shifter Q4, R36 and into the common resistor R37. Similarly Q1 draws current out of R37. Under no terminal load conditions these two currents are balanced, even if the output voltage is high.

Any AC output load current from the power amplifier is reflected by ripple currents in both positive and negative supplies. The net instantaneous current flowing in R37 alternates in synchronism with the output cycles, its amplitude increasing as the load current increases. So the amplitude of the alternating voltage across R37 is an analog of the output load current, and can be compared against a scaled reference voltage.

A window comparator is formed from the two halves of M2 and the voltage across R37 is applied to both halves. The outputs at M2-12 and M2-7 are uncommitted. Each half is biased by 2.45V in the correct polarity, provided by the reference zeners D9 and D17 in the 400V Monitor circuit. Unless any voltage peak across R37 exceeds this level, both M2 outputs will be pulled to 0V by R20.

The '100V FLAG' line (TP2) therefore remains at logic-1.

Any peak greater than 2.45V overcomes the bias on one half, causing its output to fall to -15V, resulting in the 100V FLAG line being pulled to logic-0. This signal then sets the limit detector latch M5a (*page 11.9-5*), as described in *para 7.12.7.1*.

9.7 AC 1000V RANGE

9.7.1 INTRODUCTION

(Circuit Diagram 430618 *page 11.9-1*)

The AC 1V signal, generated by the 1V Buffer in the Sine-Source assembly, enters the Power Amplifier as for the 10V range; but the 10V Amplifier is bypassed for the high voltage ranges.

On the 1000V range, the signal is switched via the 1kV x2 Amplifier and 1kV Error Amplifier, before being applied to the 100V Amplifier. The 100V Amplifier output is stepped up to 1000V Range levels by one of two (LF or HF) transformers, whose secondary voltage is delivered via the 'AC 1kV' line to the PHI(ACV) line on the AC assembly. Thereafter the output is transferred to the instrument terminals as for the 10V range.

9.7.2 1000V RANGE POWER ROUTING

(Circuit Diagrams: 430618 *pages 11.9-2 and 11.9-3*;
430844 *page 11.7-1*; 430537 *page 11.14-1*)

'AC 1V' enters the Power Amplifier assembly at J9-36 (*page 11.9-2*). Relay RL3 is un-energized, shorting the 10V Amplifier input; and RL1 is energized, routing the AC 1V signal to the 1000V Amplifier chain.

Energized relay contacts RL1-8/4 apply the signal to the Gain x2 Stage, whose output is summed with error feedback, providing drive to the 1kV Error Amplifier.

The 1kV Error Amplifier output is passed as '1kV ERROR O/P' via relay RL1-9/13 to the 100V Amplifier (*page 11.9-3*). It is input through the contacts of un-energized relay RL2-6/4.

The output from the heatsink at J3-9 is transferred directly, as the 'OUTPUT' signal, to the '1kV ENABLE' relay contacts RL6-8 and RL6-9 (*page 11.9-2*). Relay RL7 determines whether the LF or HF transformer assembly is to be used, the OUTPUT signal being applied to the appropriate primary winding.

The secondaries of both transformers are connected into the High Voltage assembly (*page 11.14-1*). Relay RL2 or RL3 selects the appropriate output to be passed on to the AC assembly, via J1-28 and J1-22, as the AC 1kV signal.

The AC 1kV signal is also applied as the negative 'Error' feedback to the 1000V amplifier system. It passes through R138 and R155 on the PA assembly (*pages 11.9-1 and 11.9-2*), to be summed at the inverting input of M18a-2. A single net inversion is present around this loop.

On the AC assembly (*page 11.7-1*), the AC 1kV signal is routed by the contacts of energized relay RL20, and through fuse F2 to the PHI(ACV) line at J7-27.

9.7.3 1kV POWER AMPLIFIER

(Circuit Diagram 430618 *page 11.9-1*)

Amplification to a maximum of 1100V is in four stages:

1. **Gain x2 Stage:** the AC 1V signal is HF-boosted and amplified. For the 1000V range the DC Reference is scaled in software, so that the AC 1V signal Full Scale value represents 1100V output.
2. **1kV Error Amplifier:** the Gain x2 Stage output is summed with error feedback from the secondary of the step-up transformer.
3. **100V Amplifier:** possessing a gain of 100, the output from its heatsinks drives one of two (LF or HF) step-up transformers.
4. **Step-up Transformer:** a ratio of 1:6.6 (LF) or 1:6.17 (HF) allows sufficient gain in the system to provide a maximum RMS output of 1100V.

The frequency response of the amplifier is matched to the step-up transformer in use. The 'LF' signal into the amplifier is at logic-1 (0V) only when the 1kV range, and either the 100Hz or the 1kHz frequency range, is selected.

9.7.3.1 Gain x2 Stage

(Circuit Diagram 430618 *page 11.9-2*)

The AC 1V signal is routed via relay RL1-8/4 to be developed across resistor R160. It is filtered by R162/C30 and applied to the non-inverting input of M15.

The feedback divider generates the x2 gain in M15; R159 and C67 providing HF lift to compensate the step-up transformer responses. FET Q35 adds C68 on the 100Hz and 1kHz frequency ranges, activated by the LF signal at logic-1, to boost the lift.

Output from the x2 stage is applied to the 1kV Error Amplifier via its input resistors R156/R95.

9.7.3.2 1kV Error Amplifier

The input resistance to M18a is split between R156 and R95 to allow the saturation detector to reduce the gain in the event of transformer saturation.

At the inverting input of M18a the signal input is summed with the AC 1kV negative feedback signal, output from the selected transformer secondary. The resulting error signal is amplified by the two stages of M18.

On the 100kHz frequency range, the maximum voltage available from the instrument is 750V. A tapping on the HF step-up transformer secondary reduces the maximum output to this level. The signal '1kV GAIN' is therefore set to logic-Ø only on the 100kHz range, cutting off FET Q19 and restoring adequate loop gain.

The second stage, M18b, adjusts the bandpass of the amplifier to match the selected step-up transformer:

100Hz and 1kHz ranges:

Q26 connects C58 and R126 across the input resistor R97; relay RL5 shorts R48, connecting C34 and R93 directly across the feedback resistor R92, also shorting C38 in the output line.

10kHz and 100kHz ranges:

Q26 connects C57 and R125 across the input resistor R97; relay RL5 shorts R47, connecting C33 and R94 directly across the feedback resistor R92, and leaves C38 dominant in the output line.

These measures give the necessary loop compensation for each transformer.

When the 1000V range is selected the amplifier output is fed to the 100V Amplifier via RL1-9/13 as the '1kV ERROR O/P' signal.

9.7.4 100V AMPLIFIER

This operates as for the 100V range, but its output signal 'OUTPUT' is fed directly to relay RL6 contacts for application to the step-up transformer.

The 100V Amplifier is described in *Section 7.8*, which deals with the 100V DC outputs.

The description is sub-divided as follows:

| | |
|--------------|------------------------------------|
| 7.8.3 | 100V Amplifier Introduction |
| 7.8.3.1 | Input to Gain and Driver Stages |
| 7.8.3.2 | DC Offset Correction |
| 7.8.3.3 | Signal Processing |
| 7.8.3.4 | Driver Regulator |
| 7.8.3.5 | Driver Output |
| 7.8.4 | 100V Power Amplifier |
| 7.8.4.1 | Positive Heatsink Assembly |
| 7.8.4.2 | Negative Heatsink Assembly |
| 7.8.4.3 | Over-Temperature Detection |
| 7.8.4.4 | 100V Output Connection |
| 7.8.4.5 | Heatsink Removal |

9.7.5 STEP-UP TRANSFORMER CIRCUITRY

9.7.5.1 '1kV ENABLE' Relay RL6

Relay RL6 allows the OUTPUT signal from the 100V Amplifier to energize a step-up transformer, providing the following conditions are met:

The $\overline{1kV}$ signal is at logic-Ø:

This is a processor-controlled signal, set to logic-Ø when the instrument AC output is switched on, in the 1000V range.

The watchdog has not 'Barked'.

On the PA assembly, the '1kV ENABLE' switch S1 is set to 'ENABLE'.

S1 is situated below the left-hand ejector lever (viewed from the front of the instrument), facing the rear of the instrument. It allows the high voltage to be switched off for servicing purposes. A red LED glows when all other conditions are met.

When RL6 is closed, the OUTPUT signal from the 100V Amplifier is switched through to the contacts of RL7.

9.7.5.2 LF/HF Transformer Selection

Relay RL7 is activated by the 'LF' signal, applying the 100V amplifier output to the HF step-up transformer for the 10kHz and 100kHz frequency ranges, and to the LF transformer for the 100Hz and 1kHz ranges.

The two transformers are separately located, their secondaries being connected into the High Voltage assembly. The HF transformer is selected when RL7 is un-energized, its primary being returned to Common-2C. RL7 is energized to select the LF transformer, whose primary current is sensed by the Saturation Detector.

9.7.5.3 Saturation Detector

To obtain the required performance, the LF transformer core is constructed from a material with high remanence. It is possible for the 1kV range to be deselected when the core is magnetized, and subsequently reselected in the same sense, with resultant saturation.

The Saturation Detector circuit is activated by sensing any excess primary current in R114, associated with the loss of reactance. It progressively removes the signal input to M18b during half cycles of the appropriate sense until the core recovers, then automatically returns to its quiescent mode.

The dual amplifier M20 is biased by R115-R118 to approximately 1V on each input. Under normal operating conditions, the unsaturated core reactance holds R114 current down, so the voltage developed across R114 is insufficient to overcome the bias. The output from both amplifiers is of negative polarity, both diodes D58 and D59 are reverse-biased, and FET Q18 is cut off by its gate being pulled down to -15V.

When the core saturates, the current in R114 rises rapidly and its voltage exceeds the bias on one of the detector amplifiers. One diode conducts, forcing Q18 into conduction; so the signal feed to M18a is shorted, the current in the transformer core is reduced to zero, and Q18 is cut off again.

On the next half-cycle the current is reversed, so saturation is reduced. If the core saturates on successive half-cycles, they again activate the detector with further reduction. The process continues until the core remains unsaturated over the full dynamic range of the primary current, when the detector becomes inactive.

9.7.6 POWER SUPPLIES AND PROTECTION

The power supplies and protection for the 100V Amplifier are described in *Section 7.8*.

The description is sub-divided as follows:

7.8.5 Power Supplies and Protection Introduction

7.8.5.1 38V Supply (The 38V supply circuit is more fully described in *Section 6.7, para 6.7.3.4.*)

7.8.5.2 400V Transformation and Rectification

7.8.5.3 400V Current Control

7.8.5.4 100V Current Sense and 1kV Overvolts Detector (This detector circuitry is used only for AC High Voltage ranges, and is therefore described in *sub-sections 9.6.4.1, and 9.7.6.1 below.*)

7.8.6 PA Power Supply Monitors

7.8.6.1 Comparator Supply Protection

7.8.6.2 15V Monitor

7.8.6.3 38V Monitor

7.8.6.4 400V Monitor

9.7.6.1 AC 1kV Overvoltage Detector (Circuit diagram 430618 *Page 11.9-6*)

On the 1000V Range the primary voltage of the step-up transformer in use is fed as 'AC OVERVOLTAGE DRIVE' from RL6-4/13 (*page 11.9-2*), via R176 and a screened lead, to the M2 comparator input (*page 11.9.6*). (The operation of the comparator is described for the 100V Current Sense application in *Section 9.6, para 9.6.4.*) On the 1000V Range the 100V overcurrent sense resistor R37 is shorted by Q6, whose gate is driven by $\overline{100V AC}$ at logic-1.

The HF (1:6.17) step-up transformer primary voltage is divided by R176 and R180 (ie by 1/116), but for the LF (1:6.6) transformer R181 shunts R180 (increasing the division ratio to 1/124.5), activated by the \overline{LF} signal and Q43. The result is that overvoltage is detected on the HF transformer primary at approx. 305V, but on the LF transformer primary at approx. 285V. Taking the step-up ratios into account, the 1kV Overvolts Detector trips at LF or HF for the same secondary voltage: approx. 1880V peak, 1330V RMS. This in turn activates the $\overline{100V FLAG}$ signal as on the 100V Range.

9.7.6.2 AC 1kV Overcurrent Detector (Circuit Diagram 430536 *Page 11.5-2*)

For the AC 1000V range, so as to protect the step-up transformers, overloads are detected directly in the output lines to the terminals. For this range only, resistance is inserted in the PHI(ACV) line in the DC assembly. The voltage across the resistance is rectified and compared against a reference. If the voltage is excessive, the comparator generates a LIM DET signal. At higher frequencies, where the internal and external connections to the load will draw extra capacitive current, part of the resistance is short circuited.

The 'AC 1kV RANGE' signal enters at J5-102 (*page 11.5-3*). This is at logic-1 to energize relay RL13, only if the 1000V range is selected. RL13 removes the short from R107 and R108.

The 'HIGH I LIMIT' signal enters at J5-98 (*also on page 11.5-3*). When the 1000V range is selected, this is at logic-1 only for the 10kHz and 100kHz frequency ranges. It energizes relay RL12, shorting R108, so that higher currents are required to trip the LIM DET signal. As frequency increases, so do the currents taken by the capacitance of the internal tracking and wiring; R107 is compensated by C45 and C49 to bypass this extra capacitive loading.

A diode-bridge rectifies the voltage developed across the selected resistor(s). The voltage is limited to 10V by D31, and resistor R84 sets the trip current level for the opto-isolator M19.

The isolator operates from the 5 volts between -10V and -15V. In normal operation M19 output at M19-6 is open-collector so Q4 does not conduct. When the output current is sufficient to trip M19, Q4 emitter is pulled low and so Q4 conducts, its collector current being drawn through R79.

M18 is a switch which under no-overload conditions is biased by R79 to +15V; and with its output at -15V, its non-inverting input is set to approx. -2V. When Q4 conducts, its collector is pulled down close to the -15V rail voltage. This is applied to the inverting input of M18, whose output reverses to +15V providing a positive trigger edge to M12-4.

For AC outputs the $\overline{DC FNCT}$ signal is inactive at logic-1, M12-3 at logic-1 removes the reset which is present for all DC voltage ranges. Monostable M12 is set to produce a logic-0 at its Q output (M12-6) unless its A input at M12-4 is edge-triggered positively. In normal conditions no trigger is given, so M12-6 remains at logic-0, D10 is unbiassed and the LIM DET line remains at the logic-0 level of -15V.

When M18 output reverses to +15V, M12-6 produces a logic-1 (0V) pulse of 1ms duration, which forward-biases D10, so the LIM DET line transmits a logic-1 pulse of 1ms duration. Successive positive or negative peaks of overcurrent retrigger the monostable, maintaining its Q output (and thus the LIM DET signal) at logic-1.

9.8 AC HIGH VOLTAGE SENSING

(Circuit Diagram 430844 Pages 11.7-1 and 11.7-2)

The SHI(ACV) signal, returned from the terminals via the Current and Output Control assemblies, enters the AC assembly as for the 10V range; but the 1V/10V Sense Amplifier is bypassed for the high voltage ranges.

On these ranges, the signal is switched into one of two guarded attenuators, both housed in the Attenuator/Cage assembly plugged directly into the AC assembly. Each attenuator is a separate resistor chain which acts as the input resistor to the inverting amplifier M32. The output of the amplifier is passed to the Comparator transfer switch.

9.8.1 100V SENSE AMPLIFIER

The SHI(ACV) signal passes through the contacts of energized relays RL19 and RL15, and is applied via the four pins of J1 into the 100V attenuator chain. The attenuator consists of four $25\text{k}\Omega$ 0.1% resistors in series. To eliminate leakage, each junction between the resistors is guarded, the guards being taken to equivalent voltage points on a chain of four capacitors, C64 to C67. The capacitive chain is also driven from the sense signal. The attenuator acts as the input resistor for the 100V/1000V Sense Amplifier M32.

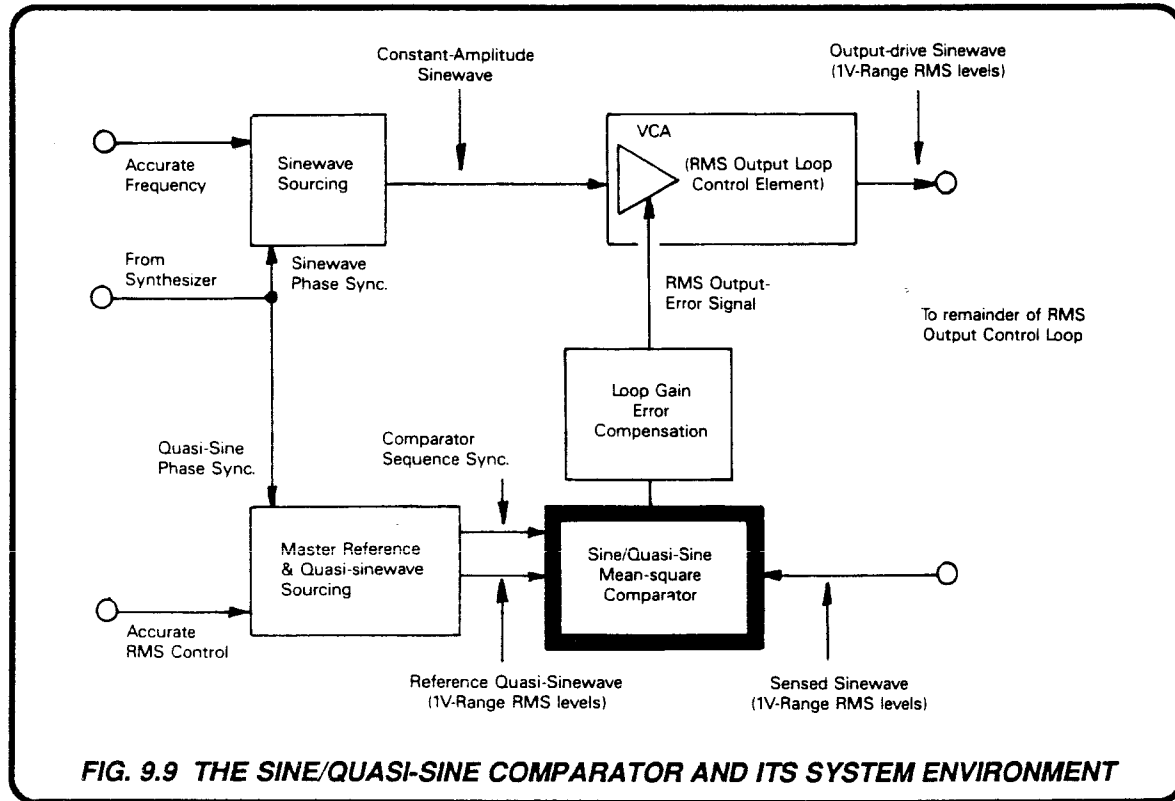
Relay RL13 is un-energized on this range, so R124 acts alone as the feedback resistor, producing an amplifier gain of 1/100. The sense signals are thus reduced to 1V range levels. The amplifier output is routed through the contacts of un-energized relay RL3 as the comparator 'SIG' input, to transfer switch M16-11 (*page 11.7-3*).

9.8.2 1000V SENSE AMPLIFIER

The SHI(ACV) signal is blocked by the contacts of un-energized relay RL15, but RL16 is energized, applying SHI(ACV) as the '1kV SENSE' signal via link LK1 into the 1000V attenuator chain. The chain has ten $50\text{k}\Omega$ 1% resistors in series, which combine to form the input resistance for M32. The guards are taken to equivalent voltage points on a chain of eight capacitors, C70 to C77, again driven from the sense signal.

Relay RL13 is energized on the 1000V range, so R123 and R124 act in parallel as the feedback resistance, giving a gain of 1/550. The sense signals are thus reduced to 1V range levels (the 1000V range FS voltage is 1100V; the equivalent 1V range FS voltage is 2V). The amplifier output passes to the transfer switch as on the 100V range.

9.9 SINE/QUASI-SINE RMS COMPARATOR



9.9.1 PURPOSE AND ENVIRONMENT

(Fig. 9.9)

The VCA acts as the control element of the Fine Amplitude Control Loop, having variable gain which is adjusted to change the output value.

The main purpose of the comparator, in conjunction with the coarse amplitude control, is to cause the output RMS value to track the value set on the front panel OUTPUT display. It generates a DC error voltage which adjusts the VCA gain.

Because it is part of the fine amplitude control loop, the comparator also corrects output RMS changes due to loading and other disturbances, within the instrument specification.

The Comparator receives two analog inputs:

- The reference quasi-sinewave whose RMS value is set by the value on the OUTPUT Display, and is also modified by stored calibration data (*sub-section 6.6*), and
- The sensed and conditioned output sinewave, which is compared against the reference quasi-sinewave (*sub-sections 9.4 and 9.5*).

The Comparator output is the DC error voltage resulting from the difference between the mean-square values of the two inputs. As the VCA gain (and hence the output RMS level) is adjusted, the RMS value of the comparator's sense input approaches that of the reference, and the error voltage is driven towards zero. The output value stabilizes when the RMS values of the two inputs are equal.

The buffered DC error signal output from the comparator is adjusted in approx. 1000ppm FS steps by the action of the Coarse Amplitude DAC, to give a virtually constant loop gain. The effects are described in *sub-section 9.3*.

9.9.2 IMPLEMENTATION

Both inputs are scaled to 1V Range levels and compared in an Integration/Sample-and-Hold system. They are sequentially steered through a common squaring circuit into separate 'REF' (Reference²) and 'SIG' (Reference² minus Sense²) averaging integrators.

A capacitor and voltage follower samples and holds the settled REF integrator voltage. It generates a DC 'REF²' signal which is subtracted from the AC 'SIG²' signal. The result is applied to the SIG integrator, then another sample-and-hold circuit generates the 'AC ERROR' signal from the integrator's output.

'AC ERROR' is thus a DC analog of the difference between the 'mean-square' values of the two inputs. It is buffered and applied to the VCA via the Error Amplifier.

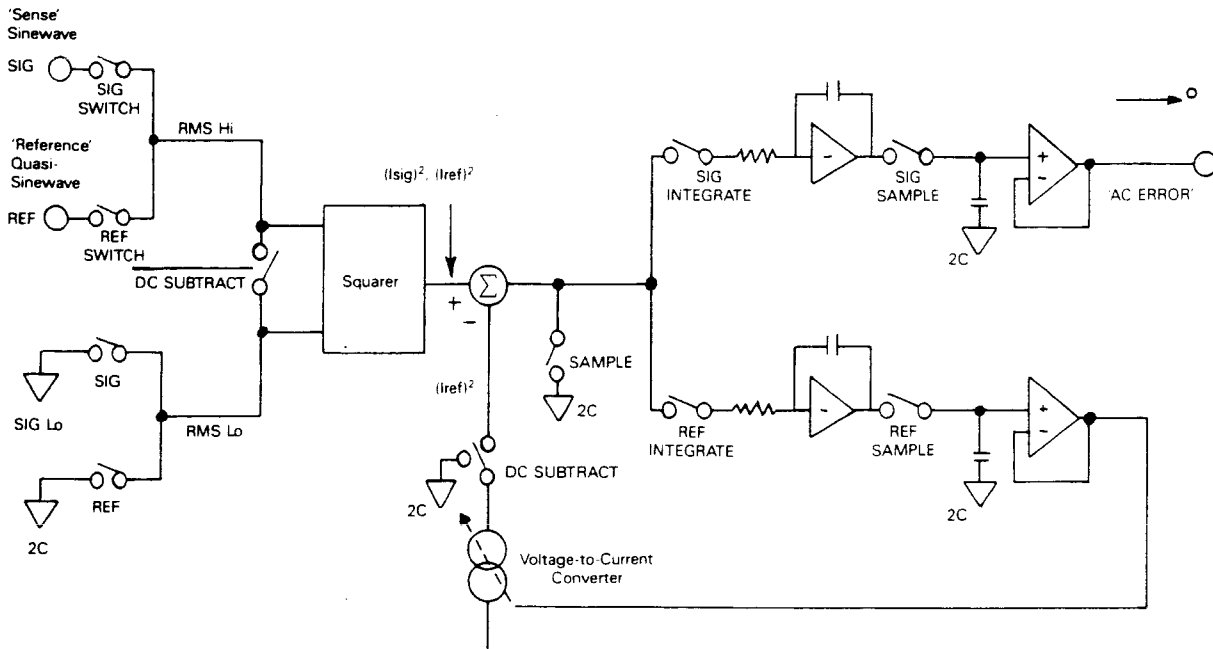


FIG. 9.10 SINE/QUASI-SINE COMPARATOR - BLOCK DIAGRAM

| | COMPARATOR CYCLING PERIODS | | | | | | | | | | |
|--------------------------------------|----------------------------|-----|-----|------|----------|---------------------|-----|------|-----|-----|---|
| | C 1 | C 2 | C 3 | C 4 | C 5 | C 6 | C 7 | C 8 | C 9 | C 0 | |
| 'X' indicates that switch is closed. | | | | | | | | | | | |
| States | REFERENCE PATTERN | | | | | SENSE (SIG) PATTERN | | | | | |
| (a) Squarer input | ← quasi-sine → | | | zero | ← sine → | | | zero | | | |
| (b) REF SWITCH | X | X | X | | | | | | | | |
| (c) REF INTEGRATE | X | X | X | X | | | | | | | |
| (d) REF SAMPLE | | | | | X | | | | | | |
| (e) SIG SWITCH | | | | | | X | X | X | | | |
| (f) SIG INTEGRATE | | | | | | X | X | X | X | | |
| (g) SIG SAMPLE | | | | | | | | | | X | |
| (h) DC SUBTRACT | X | X | X | | | | X | X | X | | |
| (j) DC SUBTRACT | | | | X | X | | | | | X | X |
| (k) SAMPLE | | | | | X | | | | | | X |
| (l) RMS Lo | COMMON-2C | | | | SIG LO | | | | 2C | | |

FIG. 9.11 SINE/QUASI-SINE COMPARATOR - SEQUENCE CYCLE

9.9.3 METHOD OF COMPARISON (Figs. 9.10 and 9.11)

The comparator is based on a ten-state recycling sequence of squaring, integration, sampling and subtraction. Operation and accuracy rely heavily on synchronization between sine and quasi-sine.

At relevant points in the following description, reference is made to a specific output frequency of 500Hz (1kHz Range), as an example to clarify the following points:

- As the output sinewave frequency is varied, the quasi-sinewave tracks an exact sub-multiple of its frequency; except on the 100Hz Range, where both are at the same frequency. In our example at 500Hz, the quasi-sinewave has half the output frequency. The various relationships between output and quasi-sinewave frequencies for different frequency ranges are detailed in Section 8, Table 8.3.
- The duration of each comparison cycle is always equal to ten quasi-sinewave periods (here 40ms), and each of the 'C' periods persists for one quasi-sinewave period (for 500Hz output - 4ms). This effect can be observed using an oscilloscope, say at TP46.
- Using this specific case also gives a point of reference for examination of the circuit waveforms using an oscilloscope.

9.9.3.1 The Comparator Sequence

(Figs. 9.10 and 9.11)

The table in Fig. 9.11 shows the conduction patterns of the switches in the block diagram of Fig. 9.10, within a complete sequence cycle. The cycle is broadly divided into two similar patterns ('REF' and 'SIG'), each occupying five quasi-sinewave periods. The cycle repeats continuously.

In the following analysis, the effects of the closed switches are described; all other switches are open.

Periods C1, C2 and C3

- a. REF SWITCH is closed to input the quasi-sinewave to the squarer.
- b. REF INTEGRATE steers the squarer output current into the Reference Integrator.
- c. DC SUBTRACT allows I_{ref}^2 to be drawn from the summing junction.
- d. RMS Lo has been connected to common 2C since the start of CØ in the previous period, in preparation for REF squaring.

The quasi-sinewave is squared, and the result is output as a current (at twice the input frequency) into the summing junction. The DC current I_{ref}^2 is subtracted at the junction, and the residue goes to charge the Reference Integrator capacitor.

(Note that every time that OUTPUT OFF is selected, REF and SIG integrator capacitors are discharged, driving both 'AC ERROR' and I_{ref}^2 to zero. During the first REF integration when OUTPUT ON is next selected, I_{ref}^2 remains at zero so the integrator capacitors start charging from zero.)

Period C4

- a. REF SWITCH is opened, removing the input to the squarer.
- b. DC SUBTRACT is opened, subtraction ceases.
- c. DC SUBTRACT closes to input a hard zero to the squarer.
- d. REF INTEGRATE remains closed, allowing the squarer and integrator to settle.
- e. RMS Lo remains connected to Common-2C until the integrator has settled.

The REF integrator remains in its integrating (on) condition during period C4, to ensure that any energy stored in the squarer during C1 to C3 is acquired.

DC subtraction during period C4 would generate an error, as full subtraction was already applied during period C1. DC SUBTRACT is therefore turned off by transferring the source of I_{ref}^2 from the summing junction to Common-2.

Period C5

- a. REF INTEGRATE opens, stopping the integrator action.
- b. SAMPLE closure forces the squarer output to a hard zero, to nullify any leakage effects in the integrator switch.
- c. REF SAMPLE closes, and current from the integrator op-amp charges the sampling capacitor to the integrator capacitor voltage.
- d. RMS Lo is switched from the Ref Common-2C to the Sense SIG Lo in preparation for SIG squaring.

As the sampling capacitor changes its charge, its voltage-follower drives the voltage-to-current converter to change the DC subtraction current. The new I_{ref}^2 is sourced from Common-2 during this period, but during the next SIG and REF integration periods, it will be subtracted from the squarer output current at the summing junction.

Periods C6 to CØ

As can be seen from Fig. 9.11, the closure pattern is repeated for SIG squaring, integration and sampling. The SIG circuit action is identical to REF, except that:

- a. the squarer input is now the sensed sinewave;
- b. the subtraction current has been set to a new value during period C5. This does not change again until period C5 of the next cycle;
- c. During period CØ, the 'AC ERROR' output from the SIG sample-and-hold voltage follower is changed, updating the VCA gain via the Error Buffer and Error Amplifier.
- d. RMS Lo was switched from Common-2C to SIG Lo during period C5 in preparation for SIG squaring. It remains connected to SIG Lo during the squaring periods C6, C7 and C8, and also during period C9 for the Sig Integrator settling. At Period CØ it is reconnected to Common-2C in preparation for REF squaring.

9.9.3.2 Comparator Action

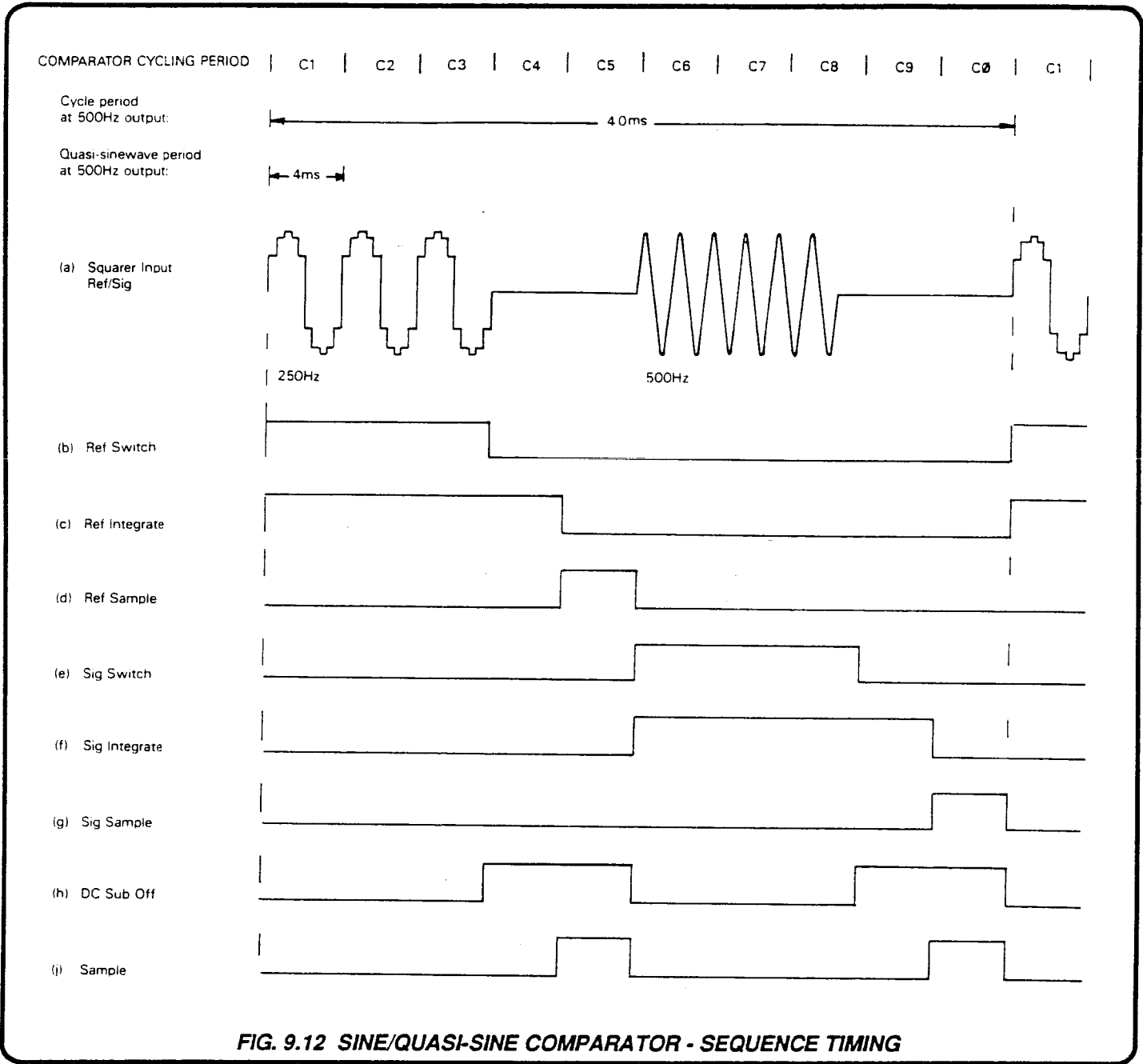


FIG. 9.12 SINE/QUASI-SINE COMPARATOR - SEQUENCE TIMING

The sequence described in 9.9.3.1 is necessarily simplified. When a new output demand changes the amplitude of the quasi-sinewave, a few sequence cycles are required to stabilize the conditions of the Ref integrator, Sig integrator, subtraction current and AC ERROR output. The circuit must also respond to demands for reduced output in addition to those for increases.

The comparator forms part of the output amplitude control loop, ultimately affecting the output voltage and hence the sensed voltage input to the squarer as 'SIG'. As the sequence recycles, the mean-square value of the SIG input sinewave will approach that of the REF quasi-sinewave, and as it does so the AC ERROR output must approach a steady-state value.

The squarer output current has an AC component in its waveform, but I_{ref}^2 being subtracted at the summing junction is a DC current. In the settled condition, I_{ref}^2 is driven on successive cycles to balance the quasi-sinewave REF^2 AC current (being applied to its integrator) about zero. The final level of I_{ref}^2 is just sufficient to be self-sustaining.

Meanwhile, the sensed SIG^2 current approaches the REF^2 value, and the same I_{ref}^2 is a DC analog of the quasi-sinewave mean-square voltage. In the output loop, the VCA is driven until the instrument output (and sensed SIG input) is at the correct level just to generate a self-sustaining 'AC ERROR'.

In the comparator, I_{ref}^2 is subtracted from both SIG^2 and REF^2 currents. This maintains the AC AMPL ERROR as an analog of the difference between the quasi-sinewave and the output sinewave mean-square voltages (when the latter is reduced by sense conditioning to 1V Range levels). Thus when the sensed SIG input voltage approaches the quasi-sinewave REF voltage (mean-square values), the AC ERROR approaches stability and the system settles.

A further complication: a bias is applied to the squaring circuit to avoid distortion by maintaining permanent conduction. The bias is controlled by the value of the positive reference voltage, and a bias current is superimposed on the subtraction current. These factors will be discussed later during the circuit analysis.

9.9.4 COMPARATOR CONTROL LOGIC (Circuit Diagram 430844 page 11.7-3)

The Comparator operating cycle originates at M15, which is a 10-bit sequencing counter, clocked at the quasi-sinewave frequency by the carry-out from M11-12.

The SYNC \emptyset input to M15 RESET is a decoded address, whose function at logic-1 is to disable counters M11 and M15, inhibiting operation of the comparator and generation of the quasi-sinewave. In this instrument, SYNC \emptyset is held permanently at logic- \emptyset , enabling both quasi-sinewave and comparator for AC Voltage and Current functions.

The clock continuously recycles M15 in ascending count through Q_0 to Q_9 , ten clocks (ie ten quasi-sinewave periods) constituting one cycle of the comparator sequence. Only one 'Q' output is at logic-1 (+8V) at a time, the remainder being at logic- \emptyset (-8V).

With increase of frequency range, the difference between the frequencies of sensed sinewave and reference quasi-sinewave increases in decade steps. As the comparison is performed at mean-square levels, this frequency difference does not matter, so long as the sinewave is at an exact multiple of the quasi-sinewave frequency. However, to optimize the operation of the Sense/Reference

comparator, the zero crossings of the quasi-sinewave are synchronized to occur coincident with a sinewave zero crossing, and all comparator state changes are also synchronized to sinewave zero-crossings.

Synchronization is achieved by clocking M17 so that all the analog switching data changes simultaneously. Thus data is latched from M17 'D' inputs to its permanently-enabled outputs, one complete quasi-sinewave period after it was clocked through M15. This ensures that the transit times of M15, M18 and M20 do not affect synchronism with the quasi-sinewave zero-crossing.

The data is thus strobed through M15 and M17, being delayed by one clock period. This does not affect the operation of the comparator, although it must be accounted for when observing waveforms on an oscilloscope.

The sequence, as described earlier in *sub-section 9.9.3*, begins with REF SWITCH connecting the quasi-sinewave to the squarer input during period C1. The logical origin of the comparator switch state during C1 corresponds to M15-2 (Q_1 output) at logic-1; but because of the data delay its actual timing is coincident with the Q_2 output of M15-4 at logic-1.

9.9.5 COMPARATOR TIMING LOGIC

(Fig. 9.13)

The comparator timing waveforms for the sequence are illustrated in Fig. 9.13. To highlight the data delay, the main waveforms are grouped into two blocks: 'REF' and 'SIG', each headed by the states of the comparator cycle. Line (b) shows which of M15 (Q) outputs is at logic-1 during each of the states. It can be seen that the effects of M15 output states are delayed by 1 clock period, in the translation to comparator states.

9.9.5.1 Squarer Commons Switching

['REF' and 'SIG' waveforms (d) and (k)]

Waveform (c) shows the variation of M15-12 (Cout). Waveforms (d) and (k) are the direct results of Cout inputs to M17 after the translation by one clock shift (note the inversion at M20-10).

During states C0 to C4, waveform (d) at logic-1 connects the squarer common (RMS Lo) to Common-2 at M16-4 for quasi-sinewave squaring; whereas during states C5 to C9, waveform (k) connects RMS Lo to SIG Lo at M16-8 for sensed sinewave squaring. In both cases, the appropriate common is connected one period ahead of the squarer input, and disconnected at the end of the integrator settling time.

9.9.5.2 Squarer Input Switching

['REF SW' and 'SIG SW' waveforms (e) and (l)]

M15 outputs Q1 to Q3 are 'OR' gated at M18-6 and applied as D2 input to M17. The result is to generate the REF SW waveform (e) at M17-7.

REF SW connects the quasi-sinewave as input to the squarer by M16-13 only during states C1 to C3.

Similarly, SIG SW waveform (l), logically derived from M15 outputs Q6 to Q8, is at logic-1 only during states C6 to C8, connecting the sensed sinewave as input to the squarer by M16-12.

9.9.5.3 Integration and Sample Switching

['INT' and 'SAMPLE' waveforms (f) and (h)]

At any instant, the comparator is either sampling or integrating. The INT waveform is thus the inverse of the SAMPLE waveform.

SAMPLE

M15 outputs Q0 and Q5 are 'OR' gated at M18-9 and applied as D3 input to M17. The result is to generate the SAMPLE waveform (h) at M17-10.

Therefore, for C0 and C5 only, SAMPLE provides two enabling inputs to AND gates M13 at M13-2 and M13-5. It also places a hard zero on the squarer output by M7-5 (page 11.7.4) when this is disconnected from both integrator inputs. With both input and output at zero volts, any offsets are removed in preparation for the subsequent squaring and integration sequence.

INT

The 'SAMPLE' output of M18-9 is inverted at M20-4, applying logic-1 to the D1 input of M17 for the whole of the cycle except for C0 and C5. The INT output at M17-5 is waveform (f), which enables M13-1 and M13-13.

REF INT

INT is 'AND-gated' with REF waveform (d) at M13-11 to generate the 'REF INT' waveform (g), which is at logic-1 only during periods C1 to C4. During this time M7-12 (page 11.7.4) at logic-1 connects the squarer output to the REF Integrator input.

SIG INT

INT is 'AND-gated' with SIG waveform (k) at M13-10 to generate the 'SIG INT' waveform (m), which is at logic-1 only during periods C6 to C9. During this time M7-6 (page 11.7.4) at logic-1 connects the squarer output to the SIG Integrator input.

REF SAM

'SAMPLE' is 'AND-gated' with SIG waveform (k) at M13-4 to generate the 'REF SAM' waveform (j), which is at logic-1 only during state C5. During this time driver M6-1 at logic-1 causes FET Q2 to conduct (page 11.7.4), connecting the REF Integrator output to the REF Sample-and-Hold input.

SIG SAM

'SAMPLE' is 'AND-gated' with REF waveform (d) at M13-3 to generate the 'SIG SAM' waveform (n) which is at logic-1 only during state C0. During this time driver M6-7 at logic 1 causes FET Q3 to conduct (page 11.7.4), connecting the SIG Integrator output to the SIG Sample-and-Hold input.

9.9.5.4 DC Subtraction

[DC SUBTRACT OFF waveform (p)]

Subtraction is required only when either input is being applied to the squarer. As REF SW and SIG SW already exist, it remains only to provide an OR function to join them. The analog circuits need an inverted waveform, so a NAND gate is used. For loading purposes two elements of M20 are connected in parallel: REF SW and SIG SW are combined as waveform (p) at M20-3 and M20-11.

Squarer Input Short

When at logic-1 during C4-C5 and C9-C0, M7-13 places a hard short between RMS Hi and RMS Lo; otherwise the short is released.

Subtraction Current Control

During C1 to C3 and C6 to C8, DC SUBTRACT OFF at logic-0 cuts off D8 (page 11.7-4), allowing Q6 to draw subtraction current through D6, D5 and R54. When at logic-1, D8 conducts and sets D5 and D6 in reverse bias, diverting the subtraction current.

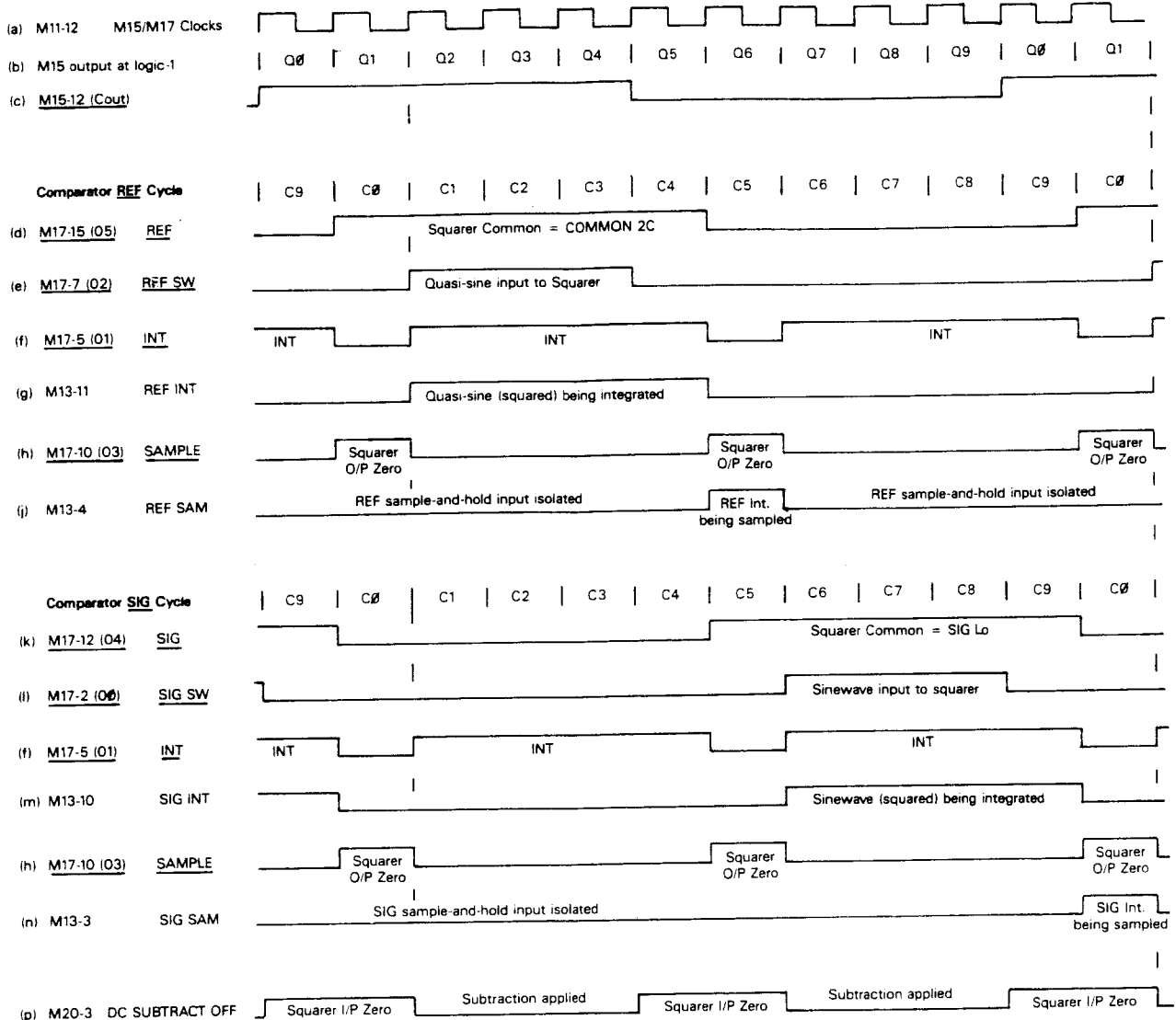


FIG. 9.13 COMPARATOR TIMING LOGIC

9.9.6 SQUARE LAW DETECTOR CIRCUIT

(Circuit Diagram 430844 Page 11.7-4 and DC400842 Page 11.7-7)

The basic action of the squaring circuitry is the same as is used for \sin^2 and \cos^2 in the Sinewave Oscillator amplitude loop, but there are some differences in detail (*refer to sub-section 8.2*).

The Square detector is biased in such a way that it is permanently turned on, to improve bandwidth and permit control of gain scaling. Its differential output voltage at Q109 and Q110 collectors is proportional to the square of its input voltage, divided by the bias voltage. The bias is derived from the DC version of the demanded signal level REF+ve, the DC output from the reference divider.

Thus the transfer proportionality of the signal magnitude is given by:
Vout is proportional to V_{in}^2 / V_{bias}

but as Vbias is derived from REF+ve,

V_{in} / V_{bias} is a constant: **k**,

and the instantaneous squarer gain is:

$$\frac{d(V_{out})}{d(V_{in})} = \frac{d(kV_{in}^2)}{d(V_{in})} = 2k$$

Thus the basic gain equation has no amplitude or frequency components, so is constant over a wide bandwidth and dynamic range. The squarer therefore has a fast response at all signal levels.

The bias is applied as currents to Q116 and Q117 emitter circuits. The transistors in the array of M22 are all used as current generators.

9.9.6.1 Bias Control

The input to Reference Amplifier M24 is the positive DC REF +ve voltage, which varies between approx. 0.14V and 2.8V, depending on the output value selection.

M24 output voltage rises until M22-9 pulls enough current through R50 to reduce M24-3 to zero. The other transistors in M22 act as current mirrors, so their collector currents are defined by the REF +ve voltage and the resistance of R50.

Thus bias current is applied to Q116 and Q117 in direct proportion to the REF +ve voltage, which is an accurate analog of the demanded output value.

9.9.6.2 Current Driver

The 'SIG²' and 'REF²' current outputs from the square detector develop a differential voltage input between the collectors of Q109 and Q110, to the current driver M103. This amplifier generates a single-ended current drive to the integrators.

M103-7 drives current out through R113 and R118 to the integrators while M103-1 supplies voltage feedback to maintain TP9 node at very near common 2 potential while maintaining high output impedance to the integrators.

Differential input variations between the collectors of Q110 and Q109, due to 'SIG²' and 'REF²' outputs from the Square Detector are translated to single ended currents into and out of the junction at TP9. The current difference passes through R118 to R148 during SIG INT states, and to R149 during REF INT states.

At other times, when both of the integrator input switches M7-8/9 and M7-11/10 are open, the 'SAMPLE' waveform closes M7-4/3 to pass any difference current to Common-2C. (During the SAMPLE periods, DC SUBTRACT OFF is zeroing the Square Detector input RMS Hi anyway, by shorting to RMS Lo via M7-2/1 - page 11.7-4.)

Resistors R118, R148 and R149 are of very low value compared with the output impedance at TP9, so the driver compliance is high.

9.9.6.3 Output Amplitude Loop - LF Gain Reduction

On the 100Hz Frequency range the gain around the output amplitude loop needs to be less than on other ranges. This compensates for the longer integration times at lower frequencies.

Adjustment is in two stages, using dual open-collector comparator M105:

a. For 100Hz Range selection

The '100Hz' logic signal input to M105-2 is derived in the frequency synthesizer and is at logic-1 when 100Hz range is selected. M105-1 is pulled up by R115 and Q108 conducts connecting R116 across R113, reducing the gain of the M103 voltage to current converter.

b. For frequency selections below 32Hz

The '>31Hz' signal input to M21 is also generated in the Synthesizer.

- i. Similar comparator action provides further loop gain reduction for frequencies of 31Hz and below. Both Q107 and Q108 are on to switch in both R116 and R116 across R113.

9.9.7 GENERATION OF THE DC SUBTRACTION CURRENT

9.9.7.1 'REF' Integration

The integrator circuit is very basic. Feedback for M12 is by C25, but the input resistance is formed by R149, R35 and the output impedance of the Current Driver, which is heavily predominant. The current from the driver is virtually unaffected by R35 and R149.

M7-11/10 conducts for periods C1 to C4 (REF INT). During C1 to C3 the REF SW waveform inputs the quasi-sinewave to the squarer, and during C4 the squarer settles to its zero input.

The REF² output from the driver is an AC current, which for a constant quasi-sinewave amplitude is integrally charge-balanced about

zero due to the DC subtraction, at twice the quasi-sinewave frequency. C25 therefore receives equal positive and negative charge during each cycle of quasi-sinewave, so the mean voltage at M12-1 does not change.

A discharge path for C25 is provided by Q5/R30. The 'INT HOLD' signal at J7-46 is logic-1 when the instrument is in 'OUTPUT OFF' condition, discharging both REF and SIG integrators. For so long as the output remains 'ON', the INT HOLD signal stays at logic-0, and the integrators are never discharged other than by the action of their inputs.

9.9.7.2 'REF' Sample-and-Hold

Q2 conducts during each 'REF SAM' period, when the charge on C25 has settled for the cycle. M12 drives C12 to the voltage on C25, and the voltage follower M4 passes the same voltage as 'REF ERROR' on to the REF V to I Converter.

Q2, C12 and M4 are low-leakage devices and M4 input circuit is screened, at low impedance, to the sampled voltage. Thus the 'Droop' is specified as less than 20 μ V during the 'Hold' part of the cycle when Q2 is not conducting.

9.9.7.3 'REF' V to I Converter

The circuit of M19 and Q6 converts the DC voltage output of M4 into the subtraction current. A second function is to draw an extra DC current which compensates for the bias control currents.

The DC 'REF ERROR' voltage from M4-6 is divided by R37/R31 and applied to the non-inverting input of M19. A second input results from the DC bias current drawn by M22-14, defined by the 'REF+ve' voltage and the two resistors AN2-10/7 and R141.

M19 drives FET Q6, which draws current via Q110 emitter, R54, D5 and D6. The current is sunk into Common-2C via R47, R38 and AN2-12/5, and into the -15V supply via the M22-14/12 bias circuit.

Capacitor C34 filters out any HF transients remaining from the switching edges of REF SAMPLE, and D7 protects against positive excursions of Q6 gate.

In the simplified diagram of *Fig. 9.10*, the subtraction current is shown as being sourced by the summing junction. In reality, it is taken from Q110 emitter for three main reasons:

- a. The Current Driver input bias is removed, allowing a zero-offset reference.
- b. The control bias for the squarer is compensated at the earliest opportunity, reducing the required dynamic range of the driver.
- c. Q110 emitter voltage remains virtually constant for all squarer inputs.

Relocating the subtraction point does not affect the essential action of the square detector and driver, because of the current-mirror action of the driver.

Subtraction is valid only during times when a quasi-sinewave or sensed sinewave is being input to the Square Detector. Thus for periods C1 to C3 and C6 to C8, diode D8 is held in reverse bias by the signal 'DC SUBTRACT OFF' at logic-0. During periods C4, C5, C9 and C0, the signal is at logic-1, so D8 conducts and reverse-biases D5 and D6. The subtraction current passed by Q6 is then diverted through D8 from M20-11/3, the 'DC SUBTRACT OFF' parallel NOR gates' output being at logic-1 (*page 11.7-3*).

When an operator selects a different output value, the result is a change in amplitude of the quasi-sinewave. This unbalances the integrator input, so C25 charges to a different mean voltage at the output of M12. The DC subtraction current change takes place over a few comparator cycles until balance is restored, when C25 and C12 will have charged to a new voltage.

9.9.8 'AC ERROR' SIGNAL GENERATION

9.9.8.1 Integration and Sampling Circuit

The SIGNAL Integration and Sample-and-Hold circuitry is identical to the REF arrangement described in *Section 9.9.7*. Moreover, the SIGNAL Integrator M12 is the other half of a matched pair with the REF Integrator.

The difference lies in the timing. Switch M7-6 allows current to pass into the SIG integrator only during periods C6 to C9, so it is the SIGNAL (sensed sinewave)² current minus the (DC REF)² subtraction current which is integrated.

The integrator voltage is sampled and output as the 'AC ERROR' DC voltage (*sub-sections 9.2.4 and 9.9.2*), into the output amplitude control loop.

9.9.8.2 Output Amplitude Loop Action

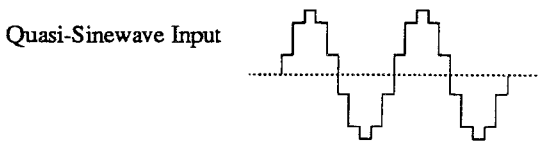
Consider the case of 'OUTPUT OFF'

- The quasi-sinewave has an amplitude determined by the 'OUTPUT' display value:
- The quasi-sinewave is squared and appears as a current in R35 during periods C1-C4, but because Q5 is conducting, the REF integrator capacitor C25 is discharged. Thus the DC subtraction current is effectively zero (it is actually sufficient to cancel the DC current in R35 due to the squarer bias).
- The AC ERROR signal voltage is zero, as Q4 conduction prevents any charge on the SIG integrator capacitor C26. Also, the output amplitude is zero, hence the sensed output applied to the squarer is zero.

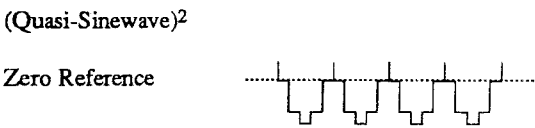
Therefore during periods C6-C9 the current in R35 is zero.

Now consider the case when OUTPUT is switched ON, with the OUTPUT display set to the minimum value of 9% of range:

As the quasi-sinewave is already present, it is squared into a negative-going waveform in R35.



During the first comparator cycle, this appears as a voltage at TP9 thus:



The standing bias on the Ref. V to I Converter has immediately set the (quasi-sinewave)² to an approximate zero mean.

The (quasi-sinewave)² current is integrated across C25, resulting in a positive 'REF ERROR' voltage after period C5, and hence a positive subtraction current in R35. The effect of the current can be seen in the TP9 voltage waveform: an increase of (quasi-sinewave)² amplitude is accompanied by a positive shift as its mean value seeks coincidence with zero.

After a few comparator cycles the current in R35 becomes charge-balanced about zero, the DC subtraction current stabilizing to a steady-state value.

Meanwhile, during the 'SIG' sections of the comparator cycle, the positive subtraction current is integrated across C26. A negative 'AC ERROR' voltage is generated, which increases the instrument output voltage via the VCA. This increase is detected by the sense feedback circuits. After squaring, the result is an AC current in R35, whose mean level begins to offset the effect of the subtraction current on the SIG integrator.

After a few comparator cycles, the AC SIG² mean current and the DC subtraction current are equal and opposite, so the current fed through R35 into the integrator is charge-balanced about zero. The integrator capacitor C26 is thus being charged and discharged by the same amount during each half-cycle of output (SIG² current being at twice the output frequency), so the AC ERROR voltage stabilizes.

Fig. 9.14 illustrates three stages in the process of increasing output from zero; observing the current in R35 (ie. the voltage at TP9), the 'AC ERROR' signal, and the output sinewave. The waveforms are not to scale.

Stage 1.

This is the first cycle that the quasi-sinewave starts to charge C25. During period C6 a non-zero subtraction current is applied to the SIG integrator, resulting in a non-zero value of 'AC ERROR', starting at C0 as the integrator voltage is sampled. This causes the instrument sinewave output to rise from zero.

Stage 2.

On the next cycle the subtraction current imposes a positive shift on the R35 waveform during C1-C3 and C6-C8. The squared quasi-sinewave does not change in amplitude, but it is more equally balanced about zero, so the next increase in subtraction current will not be so great.

During C6-C8 the sinewave is being applied to the squarer, so TP9 exhibits its squared waveform shifted positively by the subtraction current. A smaller increase in 'AC ERROR' and output sinewave results, as the AC input to the SIG integrator is more equally balanced about zero.

Stage 3.

In this state the loop has stabilized. The squared quasi-sinewave and sensed sinewave are both charge-balanced about zero, the subtraction current and 'AC ERROR' have reached constant values, and the instrument output is stable.

9.9.8.3 'AC ERROR' V-to-I Converter

(Circuit Diagram 430844 page 11.7-6)

To avoid pick-up during transit, the ACERROR voltage is converted into a current, for transmission to the Error Amplifier on the Sine-Source Assembly. One half of M3 is used as a unity-gain inverting buffer, and the other as a voltage-to-current converter. The relay RL1 is not fitted, so M3-7 is linked directly to the test switch S1 'NORM' terminal.

At M3-7 the DC 'AC ERROR' voltage is inverted and used to drive the current converter via AN1-3/12. The current in AN1-4/13 is

mirrored by the current in AN1-11/6 (AC AMPL ERROR), which is sourced in the Sine-Source Assembly by M41a, the Error Amplifier (Circuit Diagram 430446 page 11.6-3).

As the AC ERROR signal DC voltage is varied by the comparator, the current in M41a input resistance also varies, and is converted into a varying voltage at M41a-1. This voltage is used to control the main voltage-controlled amplifier M48 via Q71.

For further information about the VCA, refer to Section 9.3.

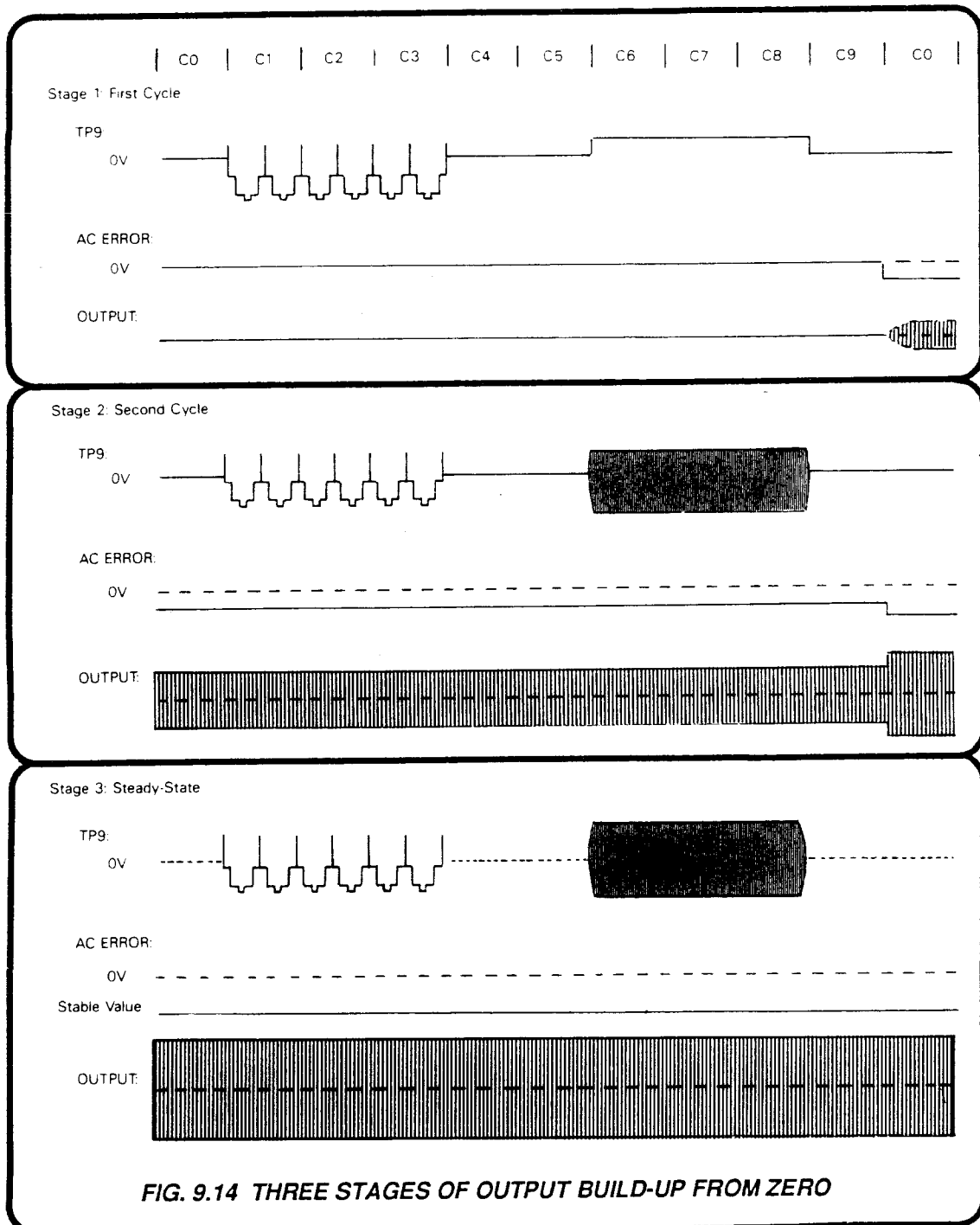


FIG. 9.14 THREE STAGES OF OUTPUT BUILD-UP FROM ZERO

9.10 LOGIC CONTROL OF AC OUTPUTS

The general aspects of analog control functions are discussed earlier in *sub-section 7.10*, subdivided as follows:

| | |
|-----------------|-------------------------------------|
| 7.10.1 | <i>Logic Levels</i> |
| 7.10.2 | <i>Heat Reduction</i> |
| 7.10.2.1 | <i>Update Considerations</i> |

The AC signals are routed through the DC assembly on their way to the terminals and back; for the 10V, 100V and 1000V ranges they are amplified in the Power Amplifier assembly. The signals are subject to digital controls incorporated in those assemblies.

Descriptions of the controls in the DC and PA assemblies are indexed in *sub-sections 9.10.1 and 9.10.2*, below.

9.10.1 DC ASSEMBLY - LOGIC AND RELAY DRIVES

(Circuit Diagram 430536 *Page 11.5-3*)

The AC voltage output and sense signals pass through the DC assembly, and are affected by the analog control signals present there.

The effects of the control logic on the DC assembly are detailed in *Section 7*, subdivided as indexed, except for the 'HIGH I LIMIT' and 'AC 1kV RANGE' Logic.

As these two signals are activated only on the AC 1kV Range, their effects are described in *sub-section 9.7.6* (but reference is also made to relays 12 and 13 in *para 9.4.2.3*).

| | |
|-----------------|---|
| 7.11.1 | <i>Introduction</i> |
| 7.11.1.1 | <i>Latched Bistable Relays</i> |
| 7.11.1.2 | <i>Tristate' Relay Drivers</i> |
| 7.11.2 | <i>Clamp Assembly</i> |
| 7.11.2.1 | <i>UPD(IG) Distribution</i> |
| 7.11.2.2 | <i>Buffer Clamping</i> |
| 7.11.3 | <i>DC Assembly Switching Logic</i> |
| 7.11.3.1 | <i>DC Range Switching Logic</i> |
| 7.11.3.2 | <i>Function and Output Switching Logic</i> |

9.10.2 PA ASSEMBLY - LOGIC AND RELAY DRIVES

(Circuit Diagram 430618 *Page 11.9-5*)

The extensive switching needed to control the many modes of operation of the Power Amplifier assembly, is described earlier in *Section 7.12*. The subjects are subdivided as listed below:

| | | | |
|---------------|--|-----------------|---|
| 7.12.1 | <i>DC Range Switching</i> | 7.12.7 | <i>'LIM ST' Logic</i> |
| 7.12.2 | <i>AC Range Switching</i> | 7.12.7.1 | <i>'LIM DET'</i> |
| 7.12.3 | <i>Function and Ranging Logic</i> | 7.12.7.2 | <i>'LIM ST' Generation</i> |
| 7.12.4 | <i>'PA CLAMP ON' Signal</i> | 7.12.7.3 | <i>CPU Response</i> |
| 7.12.5 | <i>'400V ENABLE' Logic</i> | 7.12.8 | <i>'LF', 'LF' and '1kV GAIN'</i> |
| 7.12.6 | <i>'BIAS OFF' Logic</i> | 7.12.9 | <i>Thermistor Comparator</i> |

9.10.3 AC ASSEMBLY LOGIC AND RELAY DRIVES (Circuit Diagrams 430844 Page 11.7-5)

The analog control signals are transferred into guard on the Reference Divider assembly, and latched as 'Q' outputs in the Serial/Parallel Data Converter. Offset positive logic is used:

$$\text{logic-}\emptyset = -15\text{V}, \text{logic-}1 = 0\text{V}.$$

The signals enter the AC assembly via J7 from the Mother assembly.

M28 and M29 are inverting, open-collector Darlington drivers. The relay-drive logic places a logic-1 (0V) on the input of the selected drivers and logic- \emptyset (-15V) on those not required. A selected driver operates its relay by pulling its output to -14V.

Whenever a switching command has been received, the CPU performs a control-data transfer and the $\overline{\text{UPD}}(\overline{\text{IG}})$ line from J7-53 is pulsed to logic- \emptyset for 50ms. Q19 is turned on, applying +15V to the relays connected to its collector. The selected relays are thus energized by 30V, but after the $\overline{\text{UPD}}(\overline{\text{IG}})$ pulse has ended Q19 turns off, and they are held on by the -12.6V between -1.4V at the cathode of D20 and -14V at the selected driver output. This method reduces the heat, generated locally by energized relay solenoids, in the relay contacts.

FETs Q42 and Q43 damp the coils of RL12 and RL13; diodes D59 and D60 isolate parts of the printed circuit to these relays, which are sensitive to power-common breakthrough when they are deselected. D55 and D56 are overswing diodes.

9.10.3.1 Range Switching (Page 11.7-5)

Range control data is input as a 3-bit code on ACR_0 , ACR_1 and ACR_2 lines. The bit-pattern is decoded to '1 of 8' by M25, to energize the correct relays for the selected range. In this instrument only eight of the M25 'Q' outputs are connected. The resulting variants are listed in *Table 9.1* against range selections.

9.10.3.2 $\overline{\text{AC FNCT}}$ and $\overline{\text{IFNCT}}$ Logic (Page 11.7-5)

In addition to its primary function of controlling AC Voltage range switching, the AC assembly logic also needs to respond to AC Current range selections if Option 20 is fitted; because the AC voltage reference for the Current/Ohms assembly is generated by the Voltage circuitry. For this purpose the two signals $\overline{\text{AC FNCT}}$ and $\overline{\text{IFNCT}}$ are used.

$\overline{\text{AC FNCT}}$ is at logic- \emptyset only when AC Voltage output is selected, holding M25-11 'D' input at logic- \emptyset , and energizing relays RL2 and RL10. This connects the star-point at Common-2B to the PLO(ACV) line (J7-31) and SIG LO to the SLO(ACV) line (J7-32) (*page 11.7-1*). The bit-patterns controlling the voltage range switching are shown on *Table 9.1*.

$\overline{\text{IFNCT}}$ is at logic- \emptyset only when Current output is selected, holding M25-11 'D' input at logic- \emptyset , and energizing relays RL2 and RL9. This connects the ACI REF lines (J7-69 to J7-72) to the ACV lines (*page 11.7-1*). The 10V range output is used as reference for the 100mA, 10mA and 1mA Current ranges, but the 1V range output is used for the 100 μ A and 1A ranges. The bit-patterns controlling the current range switching are also shown on *Table 9.1*.

The signals $\overline{\text{AC FNCT}}$ and $\overline{\text{IFNCT}}$ are never at logic- \emptyset at the same time in normal operation. The only time they are at logic-1 together is when all outputs from the Control Data latches in the Reference Divider are 'Tristated'. 'DCI' ensures that RL2 and RL9 cannot be energized by selection of DC Current ranges.

9.10.3.3 'AC Zero'

For zero output, the lines from the voltage generators to the I+ and I- terminals are disconnected by deselection of the ranges, and a hard short is placed across the output lines by RL18.

The $\text{ACR}_{2,0}$ code is '1,1,1'. This sets M25-4 to logic-1 (energizing relay RL18) and all other M25 range outputs to logic- \emptyset (the resultant bit-pattern is shown in *Table 9.1*). Thus all ranges are deselected, but relays RL2 (ACV and ACI), RL3 (AC Low Voltage Output), RL10 (ACV) and RL19 (1kV) remain energized. Relay RL18 connects the PLO(ACV) star-point of Common-2B to the PHI(ACV) line.

9.10.3.4 'BARK DELAYED'

The 'BARK' signal does not affect the AC assembly relays. However, if the Watchdog is activated, the CPU imposes OUTPUT OFF conditions and forces the Precision DC Reference to ramp down to zero, so the PHI REF voltage also falls to zero.

All outputs from the Control Data latches in the Reference Divider (*page 11.4-4*) are 'Tristated' by the 'BARK DELAYED' signal. This allows the pull-up resistors (AN4 and AN5) to become effective.

The $\overline{\text{AC FNCT}}$ and $\overline{\text{IFNCT}}$ are pulled to logic-1, and the $\text{ACR}_{2,0}$ code is '1,1,1'. This imposes 'AC Zero' conditions on the analog circuit, but RL2, RL9 and RL10 are also de-energized. So the DC precision reference is disconnected from the input to the quasi-sinewave generator; the ACI(REF) is disconnected from the input to the AC Current circuitry, and the Sense and Power Lo lines are disconnected from the sense amplifiers.

| Function Note [1] | Range | Range Code | | | M25 Output at Logic-1 | | Relays Energized [* = Energized] | | | | | | | | | | | | | | | | | |
|-------------------------|---------------------------|-------------------------|----------------------------|------------------|--------------------------|-----|----------------------------------|---|---|---|---|---|---|---|----|----|----|----|----|----|----|----|----|----|
| | | ACR ₂ | ACR ₁ | ACR _g | 'Q' | Pin | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 |
| AC Volts | 1000V | 0 | 0 | 0 | Q0 | 3 | . | | | | | | | | . | | | . | | | . | | | . |
| | 100V | 0 | 0 | 1 | Q1 | 14 | . | | | | | | | | . | | | . | | | . | | | . |
| | AC FNCT at Logic-0. | 10V | 0 | 1 | 0 | Q2 | 2 | . | . | | | | | | . | | | . | | | . | | | . |
| | | 1V | 0 | 1 | 1 | Q3 | 15 | . | . | | | . | . | | . | | | . | | | . | | | . |
| | IFNCT at Logic-1) | 100mV | 1 | 0 | 0 | Q4 | 1 | . | . | . | | . | | | . | . | . | | | | . | | | . |
| | | 10mV | 1 | 0 | 1 | Q5 | 6 | . | . | . | . | | | | . | . | . | | | | . | | | . |
| | | 1mV | 1 | 1 | 0 | Q6 | 7 | . | . | | | | | | . | . | . | | | | . | | | . |
| | Any | 1 | 1 | 1 | Q7 | 4 | . | . | | | | | | . | | | | | | . | | . | . | |
| AC Current | 100μA } 1A } | 0 | 1 | 1 | Q3 | 15 | . | . | | | . | . | . | | . | | | | | . | | | . | |
| | | IFNCT at Logic-1. | 1mA } 10mA } 100mA } | 0 | 1 | 0 | Q2 | 2 | . | . | | | | | . | | | | . | | . | | . | . |
| IFNCT at Logic-0) | | | | | | | | | | | | | | | | | | | | | | | | |

Note[1] In normal operation, unless the SAFETY message is displayed; either AC FNCT or IFNCT, but not both, will be at Logic-0.

TABLE 9.1 AC ASSEMBLY SWITCHING LOGIC

SECTION 10 CURRENT OUTPUTS AND RESISTANCE (Option 30)

10.1 DC AND AC CURRENT

The circuits described in this sub-section perform the following functions:

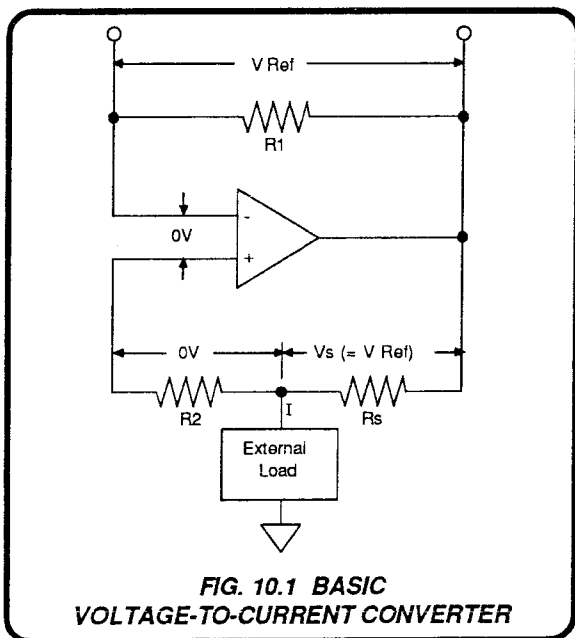
- Divide the DC reference voltage by 10 to (-2V to +2V).
- Generate a DC output current whose value varies directly as the reduced value of the DC reference Voltage.
- Convert the ACI Reference Voltage into an AC reference current, having a high-impedance source.
- Generate an output current whose value varies directly as the value of the AC reference current.
- Provide switching of the DC or AC Current Range and Output, under the control of the Analog Control Interface.
- Sense excess output (compliance) voltage, providing a status signal to the CPU via the Analog Control Interface.

The voltage-to-current converter is located on the Current/Ohms assembly, providing five DC and five AC ranges of current output. The nominal full range values are 1A, 100mA, 10mA, 1mA and 100µA, each extending to 100% overrange, for both DC and AC Current selections. The output is drawn from the instrument I+ and I- terminals; the Hi and Lo terminals not being used.

10.1.1 VOLTAGE-TO-CURRENT CONVERTER

Fig. 10.1 shows the basic arrangement. A DC or AC reference voltage is developed across R1 between the output and the inverting input of the high-gain amplifier. Its output connects to its other input by a 'shunt' network, part of which carries the output current.

The combined feedback forces the differential input to zero. The current in the positive feedback path is adjusted until the full value of the reference is developed across the path. For example in Fig. 10.1 no current flows in R2, so all of VRef is developed across Rs. The values of VRef and 'shunt' Rs thus determine the value of current flowing in the external circuit. Rs is switched to select the range, and VRef is varied to set the output current within the range.



10.1.2 AC CURRENT GENERATOR

(Circuit Diagrams 430614 Page 11.8-1 and 430540 Page 7.13-3)

Because a return path is needed for the output current, a 'compliance' signal voltage appears between the I+ and I- terminals. The magnitude of this voltage is specified in the User's Handbook, and the specification is met by floating the input to the output amplifier.

On the DC ranges the floating DC reference is input directly into the output amplifier, which therefore acts as a voltage to current converter in the style of Fig. 10.1. Resistors R44 and R45 provide 10:1 attenuation, to set the 'VRef' to 1/10 of the reference value.

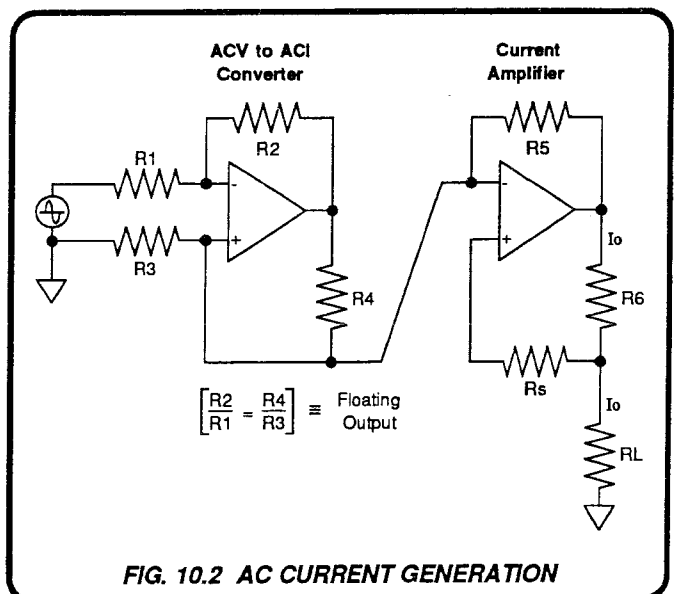
For AC ranges the ACI Reference is buffered from the output amplifier in a two-stage circuit. A fixed voltage-to-current conversion stage is followed by a range-switchable current amplifier (the latter is the voltage-to-current converter for DC ranges). The combination is simplified at Fig. 10.2.

In the figure, the AC Reference voltage is applied via two resistors R1 and R3 to both inputs of the first stage. It is arranged for the resistor values to conform to:

$$\frac{R_2}{R_1} = \frac{R_4}{R_3}$$

so the output impedance of the stage is virtually infinite, and its output 'floats'.

The second stage is a current amplifier, receiving the output current of the fixed stage to generate a voltage across R5. This voltage is repeated across R6, whose value is range-switched. Any resistor Rs does not affect the output, carrying no current. The current amplifier supplies are bootstrapped to improve common mode rejection.



10.1.3 DC AND AC REFERENCE - SOURCING AND SCALING

The DC output currents are bipolar, controlled within each range by the value of reference voltage (REF) applied directly from the Reference Divider. On all DC ranges, REF is divided by 10 in the input attenuator. On the 1mA, 10mA and 100mA ranges, the span is $\pm 20V$, so a full scale span of $\pm 2V$ can be applied across the selected range shunt.

To optimize the choice of components and minimize the number of relays required for range switching, the DC reference for the other two ranges is additionally divided by 10 in software. On the 1A Range a full scale span of $\pm 200mV$ can be applied across its 0.1Ω shunt, and for the $100\mu A$ Range the $\pm 200mV$ can be applied across the combined shunt resistance of 1000Ω assigned to the 1mA Range.

The AC output currents are controlled within each range by the value and frequency of the ACI(REF) voltage. This reference voltage is generated by the circuitry used for AC voltage ranges: the 10V Range for the 1mA, 10mA and 100mA ranges; but the 1V Range for the $100\mu A$ and 1A ranges. Thus the same shunt values and switching relays can be used for both AC and DC current outputs. The highest frequency available is 5kHz.

10.1.4 DC CURRENT REFERENCE '(REF)' (Circuit Diagrams 430652 Page 11.4-3 and 430614 Page 11.8-1)

The (REF) signal is the main DC reference for the whole instrument. It is sourced in the Reference Divider on J4-9/10/11/12 (page 11.4-3) as a 4-wire output, which enters the Current/Ohms assembly from the Mother assembly on J8-1/2/3/4 (page 11.8-1). Relay RL7 is activated for DC Current Ranges, so the PHI(REF) and PLO(REF) levels are sensed at TP3 and TP4 respectively.

(REF) is divided by R43/R44, so $1/10$ of (REF) is developed across R43, and applied between the inverting input of the V-I converter and the output of the Darlingtons on the PS/I heatsink at J19-7 (one of the relay contacts RL1-2/3 or RL1-10/11 is always made).

10.1.5 AC CURRENT REFERENCE 'PHI (ACI REF)' (Circuit Diagrams 430844 Page 11.7-1 and 430614 Page 11.8-1)

On the $100\mu A$ and 1A ranges, the AC 1V Range circuit provides the 2V RMS Full Scale reference; on the 1mA, 10mA and 100mA ranges the AC 10V Range circuit provides 20V RMS at Full Scale.

On the AC assembly (Page 11.7-1), for T' function, RL9 is energized and RL10 is not. The reference voltage for the current generator is derived from the PHI (ACV) and PLO (ACV) signals; and sensed at the input to the Current/Ohms assembly. The sensed ACI REF is returned to the appropriate connections on the 1V/10V Sense Amplifier. The 4-wire connections are made via J7, pins 69 to 71, to the same pins of J8 on the Current/Ohms assembly.

The AC preamplifier M8 divides the reference voltage by 10, so that the value of the RMS voltage applied to R43 is the same as the DC voltage applied for corresponding range and output settings.

10.1.6 RANGE SELECTION

Fig. 10.3 shows two Range configurations of the current amplifier. In each case V Ref is 10% of the reference voltage. RL1 is a bistable latching relay, in which the polarity of the solenoid current determines which state is selected. Solenoid current is not required for hold-on, being necessary only to change state.

The voltage across the I+ and I- terminals is allowed to rise to 3V DC or RMS with full compliance. Each range incorporates a series resistive element connecting the range selection relay contact to the I+ terminal. These resistors enhance the stability of the circuit, with reactive loads.

10.1.6.1 1A Range (Refer to Fig. 10.3a)

Relay RL1 is activated to close contacts 8/9, 11/10 and open contacts 2/3. Relays RL2, 3, 4, and 5 are not energized. The only output current path available is through the 0.1Ω shunt R80. Thus in the positive feedback path all of V Ref is developed across R80, and no current flows in R79, R8, R9 or R10. As V Ref is scaled to 100mV DC or RMS Full Range, the full range output current in R80 is: $100mV/0.1\Omega = 1A$.

10.1.6.2 100mA, 10mA, and 1mA Ranges (Refer to Fig. 10.3b)

Relay RL1 is activated so that contact RL1-3/2 is closed, contacts RL1-10/11 and 8/9 are open. One relay from RL2, 3 and 4 is energized by range, RL5 is also energized on the 10mA and 100mA ranges for extra HF filtering. All currents now avoid the 0.1Ω shunt, passing instead through the 10Ω shunt R79.

R79 is mounted with R80 on a separate heatsink assembly, plugged into the main Current/Ohms assembly (refer to the Layout Drawing, page 11.8-1 for alternative versions).

On the 100mA range, VRef is scaled to 1V DC or RMS Full Range, so the full range current flowing through R79 to the I+ terminal via RL3-14/8 is: $1V/10\Omega = 100mA$.

For the 10mA range, R8 (90.00Ω) is included in the current path, so the full range output current is reduced to 10mA. 900.0Ω (R9) is added on the 1mA range.

10.1.6.3 $100\mu A$ Range (Refer to Fig. 10.3b)

The hardware is switched as for the 1mA range, but either the DC REF voltage is scaled in software to 1V full range, or the ACI REF voltage is obtained, as for the 1A range, from the AC 1V range circuitry. Thus VRef is scaled to 100mV DC or RMS Full Range, and the full range output current is $100\mu A$.

10.1.6.4 10A Range

The selection of the 10A range is only possible if a model 4600 amplifier is connected to the instrument using the digital and analog control busses, as described in sections 6.1.9 and 7.3.8. Since the 4600 relies on the provision of an input voltage to convert to an output current, operation of the 4708 in 10A range is discussed in the DC Voltage and AC Voltage generation sections.

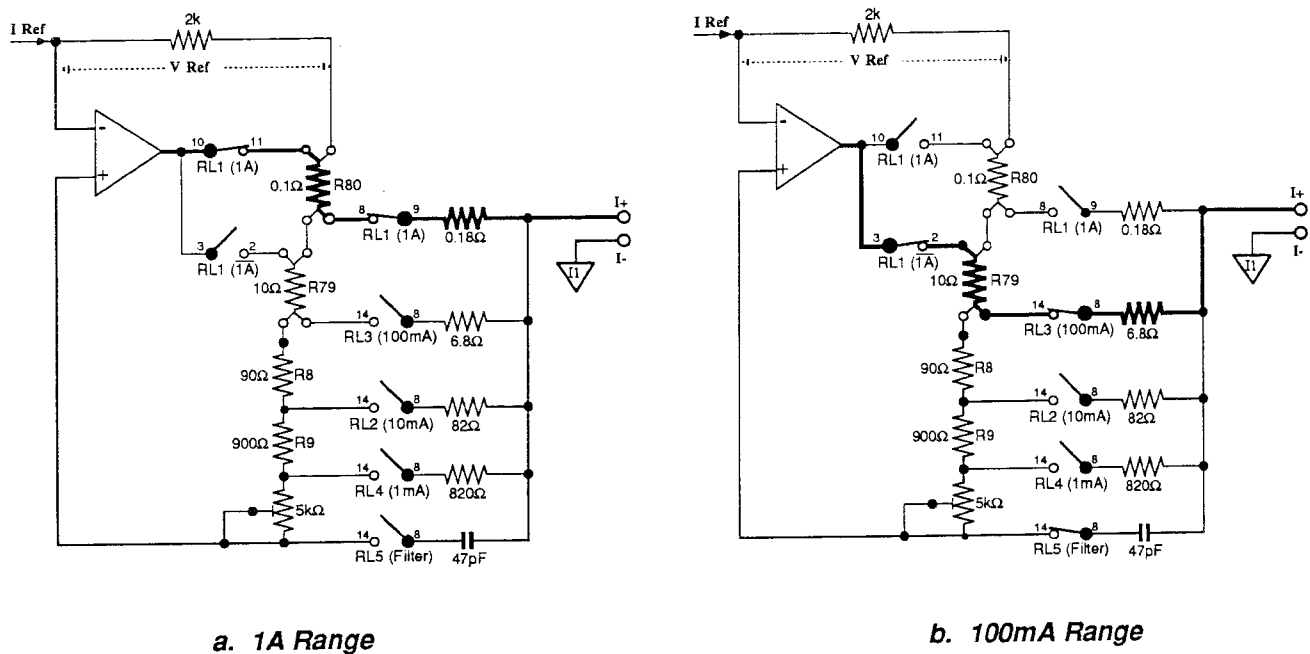


FIG. 10.3 CURRENT RANGE CONFIGURATIONS

10.1.7 DC VOLTAGE-TO-CURRENT CONVERSION

The value of the REF input sets the output current value, scaled for range as described earlier. REF is coupled: Hi (TP3) to the output, and Lo (TP4) to the inverting input through R44.

The conversion amplifier is in two sections: a voltage preamplifier on the Current/Ohms assembly (page 11.8-1), and a power amplifier on the PS/I Heatsink assembly (page 11.13-3). The latter is also drawn, for convenience, on page 11.8-1.

The whole amplifier is also used as the Current Amplifier for AC output currents. In that case it is preceded by the AC preamplifier M8 (sub-section 10.1.9).

10.1.7.1 Voltage Preamplifier

M3, M4 and Q6 form a high-gain, chopper-stabilized voltage amplifier. M3, itself a chopper-stabilized amplifier of high gain and approximately 10Hz bandwidth, trims the input offset of Q6, which provides the bandwidth necessary to pass the signal frequencies and reject common-mode noise.

M4 contributes additional gain and drives the high-current output stage via link TLE. Its load, consisting of R26, R23 and R28 shunted by Q7 in the Heatsink assembly, is supplied with a constant current by Q9, D6 and Q11. Additional frequency compensation is provided by C43 and R81.

The supplies to Q6 and M3 are bootstrapped by M7 for common-mode rejection, also linearizing the preamplifier's dynamic response. Extensive screening and filtering is employed to eliminate the effects of the chopping spikes at the inputs and output of M3.

10.1.7.2 High Current Output Stage

(Circuit Diagrams 430614 Page 11.8-1 and 430540 Page 11.13-3)

The main current amplifier and temperature-sensing driver load (Q7) are located on the PS/I Heatsink assembly. The quiescent current 'SET I_Q' adjustment is situated on the Current/Ohms assembly.

10.1.7.3 Temperature Compensation

Transistor Q7, thermally attached to the heatsink and in parallel with R26, R23 and R28 on the Current/Ohms assembly, acts as the load for the preamp. buffer. As the heatsink temperature increases, Q7 conduction increases, reducing the drive to the current amplifier. This compensates for increased intrinsic quiescent current in the two Darlington output devices.

10.1.7.4 Quiescent Current Adjustment

FET Q9 acts as constant 1.4mA ballast for the 3.3V zener diode D6, which sets the voltage across R27 to approx. 2.6V. This establishes the collector current in Q11, generating a constant current in the buffer load.

The voltage across the load is supplied to the PS/I heatsink as drive for the high-current amplifier. The tapping at J8-110 sets the base conduction level of Q7 on the heatsink, which in turn sets the level of its collector conduction, adjustable by R23. This therefore adjusts the quiescent current in the output devices Q1 and Q2.

10.1.7.5 Power Amplifier

Darlington emitter-followers Q1 and Q2 form the power output amplifier, current-limited by Q5 and Q6. The bias is set to provide some 100mA of quiescent current, which reduces the output resistance of the stage, improving the dynamic response of the output current. This also suppresses any tendency for the drive from

the preamp buffer to fluctuate for output currents around zero; as the drive voltage must slew through approximately 1.3V after switching one device off before the other is switched on. The current shunts complete the feedback and output current being fed to the I+ terminal via protection circuitry and output switching.

10.1.8 AC VOLTAGE-TO-CURRENT CONVERSION

10.1.8.1 AC Voltage-to-Current Converter M8

(Circuit Diagram 430614 Page 11.8-1)

The reference voltage PHI(ACI REF) is applied to the inverting input of M8 via resistor R45, with R46 as feedback resistor. Similarly R47 and R48 are connected on the non-inverting side. The 18M Ω resistors R82 and R83 shunt R47 to allow compliance adjustment by R31. R86 refers the input to Common-I1, the main 'signal' common.

10.1.8.2 Current Amplifier

The output AC current from the converter, flowing through R48 to restore M8 input virtual-common, passes via R85 into the Current Amplifier feedback resistor R43. It generates a reference AC voltage between the output of the whole Current Amplifier and its inverting input. This is reflected on its non-inverting side by the current flowing through the range-switched output 'shunts'.

The whole amplifier is also used as the Voltage-to-Current Converter for DC output currents (*sub-section 10.1.8*). The Preamplifier and Output sections have the same operation as in the DC case.

10.1.9 OUTPUT PROTECTION

Diodes D18 and D19 are 5V, 5 Watt zeners, placing an absolute limit on the excursions of output voltage. The output compliance specification is valid only up to 3V DC or RMS at the output terminals. Nevertheless, occasions may arise when a user overloads the circuit by attempting to drive current into open circuit (e.g. by disconnecting from a load with OUTPUT ON). In this case D18 and D19 protect any voltage-sensitive load by limiting the output voltage to 5V. But before the voltage reaches this limit, the overvoltage protection circuit generates the LIM ST signal.

10.1.9.1 Guard Buffers

M1 guards out the leakage of D18 and D19 in normal operation, and protects against other leakage, by maintaining the output screens and shields around the output circuitry at the output potential. In addition to its bootstrap function, M7 also acts as a buffer for guards around the amplifier input, thus preventing any common-mode disturbances from affecting the performance of the main amplifier.

10.1.9.2 Overvoltage Detection

The output guard buffer M1 drives the overvoltage detection circuit. M15 divides the output voltage by two and acts as an inverting full-wave rectifier, accommodating AC and both polarities of DC. The full-wave rectified voltage at M15-14 thus increases negatively as the output voltage increases, charging C32 to its mean value at M15-10. M15-9 is biased to -2.2V, so M15-8 reverse biases D10 unless the terminal voltage exceeds 4.8V RMS, when M15-8 swings to the negative rail and pulls the LIM ST line to -15V (logic-0).

The diode D10 is part of a diode-OR gate, linking LIM ST to the LIM ST line, which enters the Reference Divider at J4-76. The CPU receives the LIM ST status signal via the SSDA serial interface, and if at logic-0 presents the 'Error OL' message on the MODE display. If in the 100mA or 1A range, the Output is turned off and the DC precision reference is ramped to zero, to limit the power developed as heat within the instrument. Other sources and the effects of the LIM ST signal are described in *sub-section 7.12.7*.

10.2 RESISTANCE

10.2.1 INTRODUCTION

Eight standard resistors are mounted on the Current/Ohms Assembly, each being part of a combination whose total resistance is factory-adjusted to a value close to nominal. They are 4-wire connected to the instrument terminals by range-selection relays. Nominal values are 10 Ω , 100 Ω , 1k Ω , 10k Ω , 100k Ω , 1M Ω , 10M Ω and 100M Ω .

10.2.2 RESISTOR CIRCUITS

10.2.2.1 4-Wire Connection Symmetry. (Circuit Diagram No. 430614 Page 11.8-3).

For any given resistor combination, the connections on the Hi side are made through contacts of the same relays used for the Lo side, except for the ' Ω OUTPUT' relays RL24 and RL25. This ensures that both sides of each resistor connect to the front panel terminals through the same number of similar thermal connections.

To achieve the low leakage required for the Megohm ranges, particularly for the 100M Ω range, a further relay RL17 is used to isolate the parallel leakage paths of the lower range circuits.

The use of latching relays eliminates the heating effect from their solenoids. But it is important that all non-thermal relay contacts are made back-to-back to cancel thermal effects. Thus only the connections to non-latching relays RL24 and RL25 actually need to be back-to-back, although most others are.

This symmetrical, 4-wire arrangement transfers the stability and accuracy of each resistor to the front (or rear) panel terminals.

10.2.2.2 4-Wire Junctions and Pre-set Trimming.

R63, R64, R65 and R72 are 4-wire resistors, so for 10 Ω -10K Ω selections the 4-wire junction is at the standard resistor itself. These resistors are parallel-trimmed. R62, R74, R73 and R71 are two-wire resistors. For these higher resistance values, 100K Ω , 1M Ω , 10M Ω and 100M Ω , series trimming is used and the 4-wire junctions enclose the series chain.

Trimming resistors are selected and adjusted in the factory, in a carefully-controlled environment, against traceable standards.

10.2.3 METHODS OF CALIBRATION

10.2.3.1 Routine Autocalibration

The nominal value of each standard resistor is labelled below its RANGE key. When the key is pressed, the OUTPUT display does not show nominal; but instead gives the value measured at its most recent calibration. This is the main criterion for many users, rather than having the resistor internally trimmed to nominal. So routine recalibration consists of accurately measuring the resistor value and

setting the display to read that measured value, without removing the instrument covers (*sub-section 1.2.10*). The factor which corrects the nominal value to the measured value is stored in non-volatile RAM on the Digital assembly.

During recalibration, if a user enters a value on the OUTPUT display which is outside the span of the calibration memory, the instrument displays "Error 6" (*Section 1.2*). As any resistor drift is normally just a fraction of the span, "Error 6" appears only when an erroneous value is entered, (eg. if a resistor's value has been changed by the stress of an overload).

10.2.3.2 Internal Adjustment

A severe overload can alter a resistor's value, possibly taking it out of its calibration memory span. To restore the value to one which can be entered from the front panel, each resistor combination includes an internal trimmer (*para 10.2.2.2*). A procedure for adjustment of the trimmers is given in *sub-section 1.5*, but this should be limited to values less than about 50ppm outside tolerance. If a resistor is found to be more than ± 50 ppm outside its tolerance, it is likely to be unserviceably damaged, so it is advisable to have such a resistor tested or replaced by an agent of Datron Instruments.

10.2.4 USE OF 'Remote Sense' KEY

10.2.4.1 4-wire/2-wire Display Values.

In Ω function, selection of Remote Sense mode (Key LED lit) displays the measured value for the 4-wire connection, but with the Remote Sense LED unlit, the 2-wire value is displayed.

10.2.4.2 Two-wire Connections.

To avoid the intrusion of extra thermal voltages, no additional switching is employed for selection of 2-wire connections. Users are recommended to connect only to the Hi/Lo terminals, so the 2-wire mode should be recalibrated at these terminals.

10.2.5 OHMS ZERO

With Ω function selected, pressing the zero key on the front panel closes the contacts of relay RL16. This provides a true 4-wire short, the existing resistor remaining connected.

If the Remote Sense LED is lit, the displayed value is zero and cannot be calibrated; but if unlit, the resistance of the short plus internal wiring can be measured and entered on the display, using four-wire measurement at the Hi and Lo terminals. Subsequently, each time the 'Zero' key is pressed in ' Ω ' function with the Remote Sense key LED unlit, this entered value will be displayed.

10.3 FUNCTION SWITCHING.

10.3.1 OUTPUT CONNECTIONS - FUNCTION ROUTING

(Circuit Diagram 430614 Pages 11.8-1 and 11.8-3)

The PHI, PLO, SHI and SLO connections are routed via the Current/Ohms assembly, and it is there that they are switched between functions. The outputs of the three functions V, I and Ω are switched by separate relays onto the terminal lines (Fig 10.4):

Voltage Outputs

Relays RL8, RL9, RL24 and RL25 are de-energized as shown on pages 11.8-1 and 11.8-3. The DC or AC Voltage Power and Sense connections to the DC assembly are routed out to the I+, I-, Hi and Lo terminals via latching relay RL23 closed contacts.

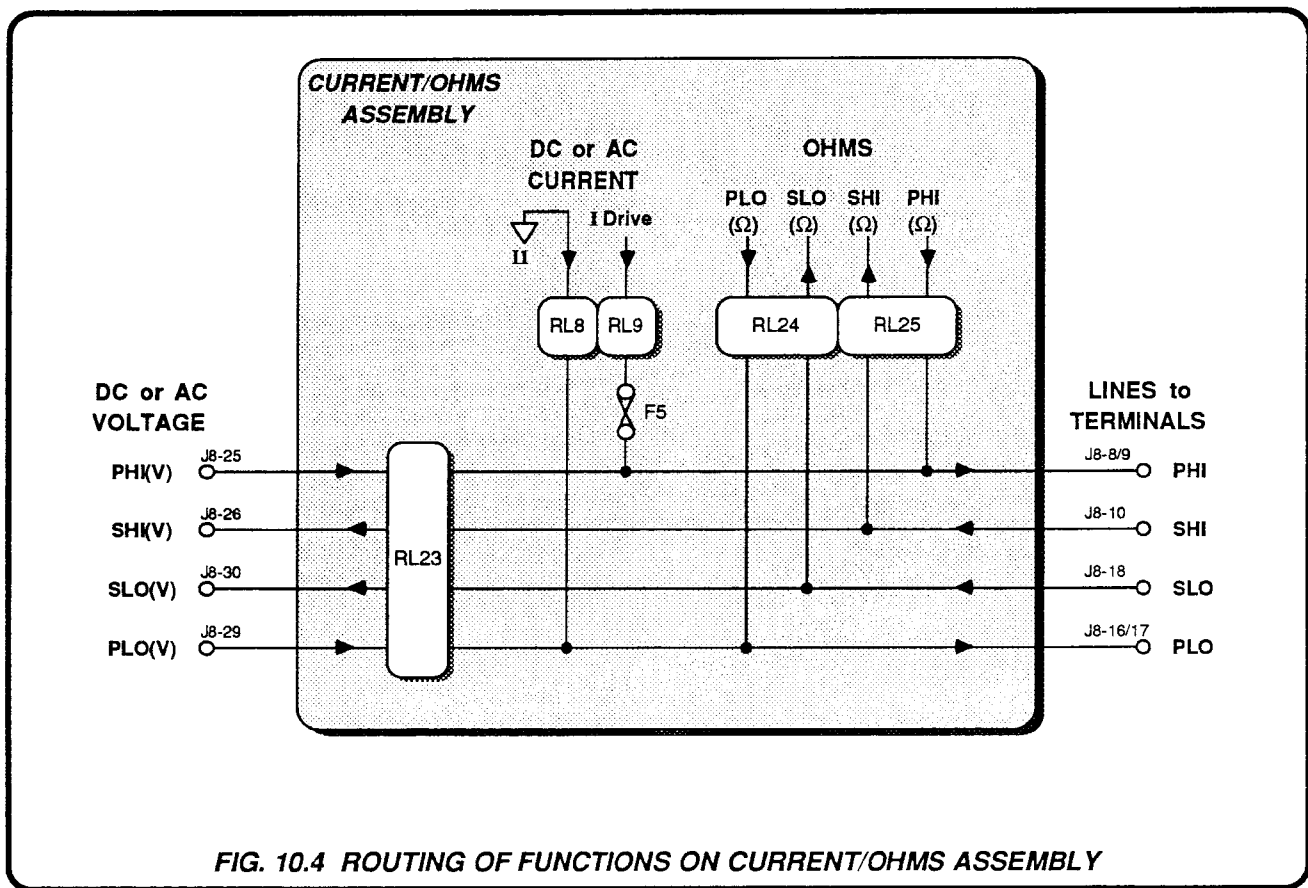
NB If Option 20 is not fitted, the Current/Ohms Link pcb is fitted in its place to make direct connection from the DC assembly to the terminals (Section 3).

Current Outputs

Relay RL23 contacts are latched open; relays RL24 and RL25 are un-energized; relays RL8 and RL9 are energized to connect the output from the selected shunt to the PHI and PLO lines only.

Resistance

Relay RL23 contacts are latched open; relays RL8 and RL9 are un-energized; relays RL24 and RL25 are energized to connect the selected standard resistor to the four PHI, PLO, SHI and SLO lines, regardless of the state of Remote/Local switching. To avoid the intrusion of extra thermal voltages, no additional switching is employed for selection of 2-wire connections.



10.4 CURRENT/OHMS ASSEMBLY ANALOG CONTROL

10.4.1 INTRODUCTION

(Circuit Diagram 430614 *Page 11.8-2*)

10.4.1.1 Control Signals

The analog control signals are transferred into guard on the Reference Divider assembly, and latched as 'Q' outputs in the Serial/Parallel Data Converter. Offset positive logic is used:

logic-Ø = -15V, logic-1 = 0V.

The signals enter the Current/Ohms assembly via J8 from the Mother assembly.

10.4.1.2 Types of Relays

Guarded Reed Relays

Relays RL2, 3, 4 and 5 are guarded reed relays activated and held on by 15V.

24V Relays

Relays RL 8, 9, 24 and 25 are 24V relays, activated during the 50ms $\overline{\text{UPD}}(\overline{\text{IG}})$ pulse by approx. 30V, but held on by 15V.

Polarized Relays

Relays RL1, 7, 10, 11, 12, 13, 14, 16, 17, 18, 19, 20, 23 and 26 are 6V latching relays, activated by approx. 7.5V; between M10-13 at -7.5V and either 0V or -15V from the drive output of the clamp assembly. These relays, strung out between the output of their bias amplifier (M10) and the Clamp assembly, are activated only during the 50ms $\overline{\text{UPD}}(\overline{\text{IG}})$ pulse. They are polarized bistable relays, which require no hold-on power.

10.4.2 LATCHING RELAYS AND CLAMPING

The Ohms and DC Current circuitry is mainly controlled by low-thermal relays, many contacts being fitted back-to-back to reduce temperature effects. For the fastest response, the output relays RL8, 9, 24 and 25 are not latched, but can trip out quickly if the power supply fails, removing any sensitive circuitry from the terminals.

All the other Ohms relays, the AC/DC Current changeover relays, 1A Range relay, and Voltage output relay are latched; allowing hold-on without power, to minimize the internal temperature at their contacts. As they are polarized they need a bipolar actuating drive, which is provided by 'Tristate' relay drivers and a bias amplifier.

10.4.2.1 Latched Bistable Relays

(Circuit Diagram 430614 *page 11.8-2*).

As can be seen from the circuit diagram on *page 11.8-2*, the relays are strung out between the output of their bias amplifier (-7.5V at M10-13) and the drive outputs from the Clamp assembly.

The bias amplifier M10 is a frequency-compensated voltage follower, buffering the tapping of attenuator AN5/R97. So one side of each relay is held permanently at -7.5V. The relay drivers on the Clamp assembly can provide outputs at 0V or -15V when enabled by the $\overline{\text{UPD}}(\overline{\text{IG}})$ pulse, but return to tristate when disabled. A relay is therefore driven to one or the other of its bistable states during update, then magnetically latched in the chosen state when the driver output returns to open-circuit.

All the latched relays except RL17 operate in the same polarity sense: when its driver output updates at logic-1 (0V), the relay latches to select its nominal function; for a logic-Ø (-15V) update, the function is deselected. For RL17 these conditions are reversed. In the analog circuit diagrams, the relay contacts are shown in their deselected state, equivalent to the un-energized state of a conventional non-latching relay. In the analog descriptions relays may be referred to as being 'energized' or 'un-energized'.

10.4.2.2 'Tristate' Relay Drivers

(Circuit Diagram 430669 *Page 10-9*).

The relay drivers (M1 and M3 on the Clamp assembly) are octal 'Tristate' buffers. Each chip is served by two inverted enable inputs on pins 1 and 19 (four buffers - half the chip - per enabling input).

Whenever a switching command has been received, the CPU performs a control data transfer and the $\overline{\text{UPD}}(\overline{\text{IG}})$ line from J8-60 is pulsed to -15V for 50ms.

Generally, the switching logic places a logic-1 (0V) on the input of selected drivers, and logic-Ø (-15V) on those whose function is not selected. Because all the buffers are non-inverting, during the update pulse a driver selects its function by setting its output voltage to 0V, deselecting by pulling its output voltage to -15V. The driver serving RL17 (M3-15/5) performs in reverse, J13-15 being pulled to logic-Ø to allow selection of the lower resistance ranges.

10.4.3 CLAMP ASSEMBLY

(Circuit Diagrams 430614 Page 11.8-2
and 430669 Page 10-9).

On the Current/Ohms Relay Drive Logic circuit diagram the Clamp assembly is shown in block form (page 11.8-2). Also, the pcb pin numbers correspond to the pin numbers of the buffer chips: J14 and J15 being the connections to M1 and M3 respectively. For signals crossing the block from bottom to top, the output of each non-

inverting buffer is drawn opposite its input, so the function remains unchanged as it crosses the block. As a further aid to identification, the pins of any one buffer are numbered so that the input and output numbers add up to 20.

10.4.3.1 $\overline{\text{UPD}}(\text{IG})$ Distribution

As the $\overline{\text{UPD}}(\text{IG})$ signal is distributed as the 'enable' to 16 buffers, it is itself buffered by M16 at M16-3 before being fanned out. So the four $\overline{\text{UPD}}(\text{IG})$ connections at the left of the block are inputs to four sets of four buffers.

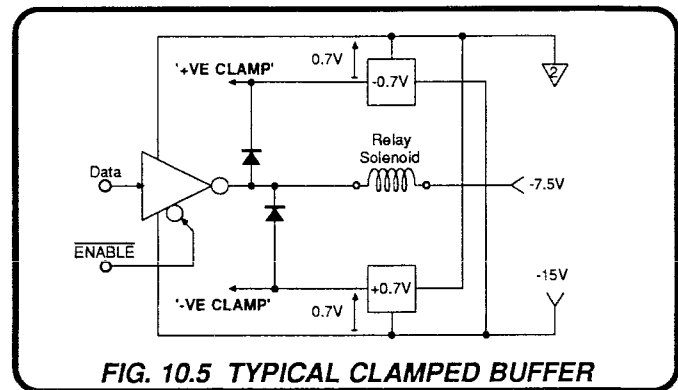
10.4.3.2 Buffer Clamping

(Circuit Diagram 430669 Page 10-9).

The 40244 octal buffer can be sourced from several manufacturers. Some variants are protected against SCR avalanche if the output voltage were to exceed the rail voltage, but some are not. Each buffer drives its output into the solenoid of a relay, and is switched on and off by the update enable. The self inductance of the solenoid can generate back EMFs well in excess of the rail voltage, so to guard against the possibility of catastrophic failure, it was decided to provide external protection in the form of a clamp circuit.

On the Clamp assembly Q1, Q2, Q3 and Q4 form two power supplies, each delivering a regulated voltage of a diode-drop less than the rail voltage, called '+VE CLAMP' and '-VE CLAMP'.

A diode connected from the buffer output to each of the clamp lines allows the output voltage to rise to the rail voltage but not to exceed it (see Fig. 10.5).

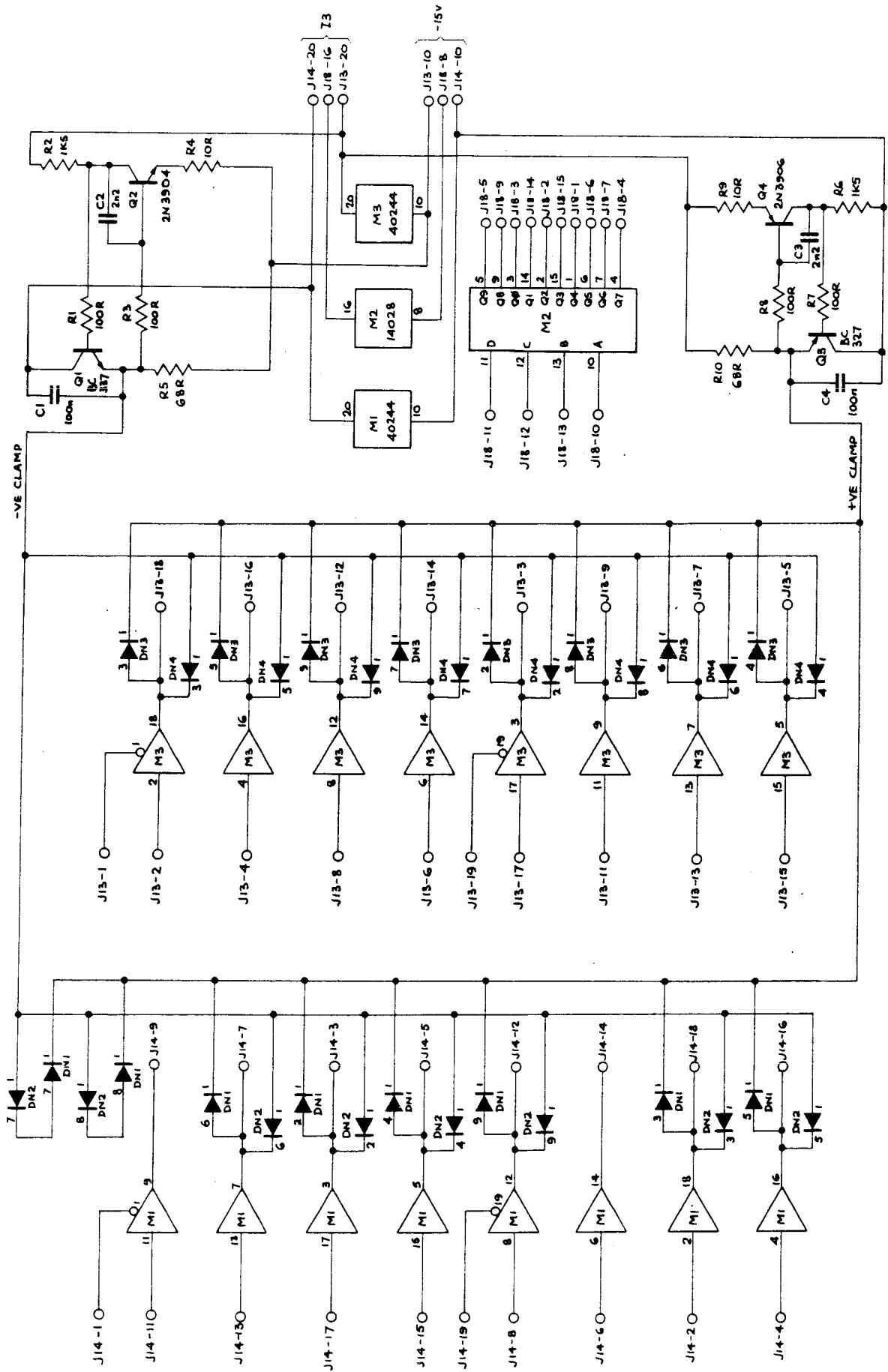


10.4.3.3 BCD - Decimal Decoder M2

The function of M2 is to decode the octal Ohms Ranging signal $R\Omega_{2-0}$ with the Ω ZERO signal, providing switching information for individual relays. To provide flexibility for other applications, the inputs and decoded outputs for M2 are taken out to pins of J18, the outputs being linked back to selected pins of J13 and J14. These connections are shown on page 11.8-2.

Refer to sub-section 10.4.6 and Table 10.3 for a discussion of the M2 decode and resultant relay operation.

DN1 AND DN3 ARE CC-IN4148
 DN2 AND DN4 ARE CA-IN4148



CURRENT / OHMS CLAMP CIRCUIT Drawing 430669

10.4.4 V, I AND Ω FUNCTION SWITCHING

10.4.4.1 Function Relays

The Function relays are located at top right of the circuit diagram on page 11.8-2.

RL8 and RL9, when energized, select the Current function.

RL24 and RL25 select the Ohms function.

RL23 connects the Voltage outputs to the instrument terminals.

For the analog connections refer to *sub-section 10.3*.

10.4.4.2 Voltage Output

Selection of the DC or AC Voltage function at the front panel also deselects Current and Ohms functions in software. The $\overline{I FNCT}$ and $\overline{\Omega FNCT}$ signals are set to logic-1, and decoded by M17-8, M16-10 and M16-11 to set the V OUTPUT signal to logic-1. This activates relay RL23, connecting the voltage output lines to the front panel terminals.

The $\overline{IR_{2-\emptyset}}$ code is '1,1,1', setting only M6 'Q7' (pin 4) output to logic-1. Thus the Current range relays RLs 2, 3 and 4 are all un-energized. Relays RL8 and RL9 are un-energized, disconnecting the current output and shorting it to the current common-I1. RL1 is latched in the \overline{IA} position, selecting R79 in preference to R80; and RL5 connects the 10mA/100mA filter.

Since $\overline{I FNCT}$ is at logic-1, the DCI and ACI signals are at logic- \emptyset ; relays RL7 and RL26 are un-energized, disconnecting the DC and AC references from the current circuitry.

(Refer to Circuit Diagram 430844 Pages 11.7-1 and 11.7-5)

In the AC assembly, the logic-1 $\overline{I FNCT}$ signal (J7-86) de-energizes RL9. This disconnects the ACI REF lines (J7-69 to J7-72) from the ACV lines. Thus the voltage to current converter (M8 on the Current/Ohms assembly) receives no input voltage, and so no current is generated. $\overline{AC FNCT}$ connects the ACV lines only for voltage ranges.

10.4.4.3 Current and Ohms Function Switching

Their Function selection logic is included later in the descriptions at *sub-sections 10.4.5 and 10.4.6*.

| Function | Signals | | | | | | Relays Activated | | | | | | | |
|----------|---------|------|---------------------|--------------------------|-----|----------------------|-----------------------|------|---|-------------|------|-----|------|--|
| | OFF | BARK | $\overline{I FNCT}$ | $\overline{\Omega FNCT}$ | DCI | $\overline{AC FNCT}$ | Current/Ohms Assembly | | | AC Assembly | | | | |
| | | | | | | | RL8 | RL24 | RL23 | RL7 | RL26 | RL9 | RL10 | |
| | | | | | | | RL9 | RL25 | (Latching Relays - * = Pin 1 at Logic-1) | | | RL2 | RL2 | |
| DCI | ∅ | ∅ | ∅ | 1 | 1 | 1 | * | | | * | | | | |
| ACI | ∅ | ∅ | ∅ | 1 | ∅ | 1 | * | | | * | | * | | |
| DCV | ∅ | ∅ | 1 | 1 | ∅ | 1 | | | * | | | | | |
| ACV | ∅ | ∅ | 1 | 1 | ∅ | ∅ | | | * | | | | * | |
| Ω | ∅ | ∅ | 1 | ∅ | ∅ | 1 | | * | | | | | | |

TABLE 10.1 CURRENT/OHMS ASSEMBLY - FUNCTION LOGIC

10.4.5 CURRENT SWITCHING LOGIC

(Circuit Diagram 430614 Page 11.8-2)

10.4.5.1 'I OUTPUT' Relays RL8 and RL9

Whenever a switching command has been received, the CPU performs a control-data transfer and the $\overline{UPD(IG)}$ line from J8-60 is pulsed to logic- \emptyset for 50ms. Q1 and Q7 remain cut off until the pulse arrives. The pulse turns Q1 and Q7 on, applying +15V to the relays connected to Q1 collector.

Any selected relays are thus energized by 30V, but after the $\overline{UPD(IG)}$ pulse has ended they are held on by the 13.3V between -0.7V at the

cathode of D2 and -14V at the selected driver (M20) output. This method reduces the local heat, generated by energized relay solenoids, in the relay contacts.

The $\overline{I FNCT}$ and OFF signals are decoded so that RL8 and RL9 are energized only when the Current function has been selected and Output is ON.

(i.e. RL8/9 are energized if M16-4 [$\overline{OFF \cdot I FNCT}$] = logic-1).

10.4.5.2 'DCI' and 'ACI' Relays RL26 and RL7

The $\overline{I\text{FNCT}}$, BARK and DC I signals are decoded so that RL7 and RL26 can be energized only when the Current function has been selected and the Watchdog has not 'BARK'ed.

Under these conditions; if DC Current is chosen, then the DC I signal is at logic-1, so M9-10 is also at logic-1 and RL7 closes its contacts to apply the DC Reference 'REF' to its voltage-to-current converter. If AC Current is chosen; DC I is at logic-0, so M9-9 goes to logic1 and RL26 closes its contact. This connects the output from its voltage-to-current converter M8 to the input of its current amplifier.

10.4.5.3 Current Range Relays RL1, 2, 3, 4 and 5

M12 is a Darlington open-collector inverting driver array. The relay drive logic places a logic-1 (0V) on the input of the selected drivers and logic-0 (-15V) on those not required. A selected driver operates its relay by pulling its output to -14V.

The octal Current Ranging signal $IR_{2,0}$ is decoded by M6 to provide four individual outputs for Range relays:

| Range | M6 Output | Relay | Reference Source | |
|-------|-----------|-------|------------------|-----------|
| | | | DC | AC |
| 1A | Q2 | RL1 | -2V to +2V | 1V Range |
| 100mA | Q3 | RL3 | -20V to +20V | 10V Range |
| 10mA | Q4 | RL2 | -20V to +20V | 10V Range |
| 1mA | Q5 | RL4 | -20V to +20V | 10V Range |
| 100µA | Q5 | RL4 | -2V to +2V | 1V Range |

The Q3 and Q4 decoded outputs for the 100mA and 10mA ranges are ORed at M17-6 to operate RL5, which introduces HF filter capacitor C49 on both these ranges.

RL1 is a bistable latching relay with a single operating solenoid. A logic-1 at pin 1 switches the 1A range on, and a logic-0 switches it off. Normally pin 1 is floating on open collector, so the relay remains latched in one bistable state with its solenoid un-energized. During the 50ms $\overline{UPD(IG)}$ pulse, non-inverting buffer M1 on the Clamp assembly is enabled, allowing the M6 Q2 state to change RL1 over (if programmed), before the $\overline{UPD(IG)}$ pulse ends.

10.4.5.4 Current Zero-Output

DC Current Zero

The DC Current output can be continuously incremented between its negative and positive Full-Scale outputs. Thus zero output can be selected by operator-adjustment of the 'REF' value using the 'OUTPUT' keys, or pressing the 'Zero' key, which ramps REF to zero. The zero value is corrected during Routine Autocalibration.

AC Current Zero

For AC zero output, as each range operates only between 9% and 200% of nominal, zero cannot be selected by adjustment of the OUTPUT keys. The AC zero is normally obtained by using the 'Zero' key which, through software, disconnects the lines from the current generator to the I+ and I- terminals.

The 'OFF' signal is set to logic-1, and the $IR_{2,0}$ code is '0,0,0'. This sets all M6 outputs to logic-0, so the Current Range relays RLs 2,3 and 4, and the filter relay RL5, are all un-energized, and RL1 latches in the \overline{IA} position (R79 is selected in preference to R80).

Relays RL8 and RL9 are de-energized by the OFF signal, to open-circuit the I+ and I- terminals, and short the current amplifier output to common-II. While setting OFF to logic-1, the CPU also forces the Precision DC Reference to ramp down to zero, so the AC reference voltage also falls to zero, and the current generator has no input. Thus the high current amplifier is not trying to produce an output current, and will not be damaged.

| Function | Range | Range Code | | | M6 Output Pins | | | | | Relays Activated | | | | | | | |
|------------------|-------|------------|--------|--------|----------------|----|----|----|----|------------------|-----|-----|-----|------------|-----|-----|-----|
| | | $IR_{2,0}$ | | | Q2 | Q3 | Q4 | Q5 | Q7 | RL1 | RL1 | RL2 | RL3 | RL4 | RL5 | RL8 | RL9 |
| | | IR_2 | IR_1 | IR_0 | 2 | 15 | 1 | 6 | 4 | 1+ | 1- | 12- | 12+ | (Latching) | | | |
| V or Ω | N/A | 1 | 1 | 1 | | | | | 1 | | | | | * | | * | |
| DCI or ACI | 100µA | 1 | 0 | 1 | | | | | 1 | | | | | * | | * | |
| | 1mA | 1 | 0 | 1 | | | | | 1 | | | | | * | | * | |
| | 10mA | 1 | 0 | 0 | | | | 1 | | | * | | | * | | * | |
| | 100mA | 0 | 1 | 1 | | | 1 | | | | * | | * | | * | * | |
| 1A | 0 | 1 | 0 | | | 1 | | | | * | | | | | * | | |
| ACI ZERO | Any | 0 | 0 | 0 | | | | | | | | | | * | | | |

TABLE 10.2 CURRENT RANGING LOGIC

10.4.6 RESISTANCE SWITCHING LOGIC
(Circuit Diagram No. 430614 Page 11.8-2).

10.4.6.1 Output Switching.

Whenever a switching command has been received, the CPU performs a control-data transfer and the $\overline{\text{UPD}}(\overline{\text{IG}})$ line from J8-60 is pulsed to logic-0 for 50ms. Q1 and Q7 remain cut off until the pulse arrives. The pulse turns Q1 and Q7 on, applying +15V to the relays connected to Q1 collector.

Any selected relays are thus energized by 30V, but after the $\overline{\text{UPD}}(\overline{\text{IG}})$ pulse has ended they are held on by the 13.3V between -0.7V at the cathode of D2 and -14V at the selected driver (M20) output. This method reduces the local heat, generated by energized relay solenoids, in the relay contacts.

The $\overline{\Omega \text{ FNCT}}$, BARK and OFF signals are decoded so that RL24 and RL25 are energized only when the Ohms function has been selected, Output is ON and the Watchdog has not barked.
(i.e. If M16-9 [$\overline{\text{OFF}} \cdot \Omega \text{ FNCT} \cdot \text{BARK}$] = logic-1, RL24 and RL25 are energized).

10.4.6.2 Range Switching

Range control data is input as a 3-bit code on ΩR_0 , ΩR_1 and ΩR_2 lines. The bit-pattern is decoded by M2 in the Clamp assembly to activate the correct relay(s) for the selected range. The resulting variants are listed in *Table 10.3* against range selections.

Relay RL17 is activated to connect the lower Ohms (<1M Ω) ranges to the output line only when the Megohm ranges are not activated. This reduces the parallel leakage (*para 10.2.2.1*). NOR gate M19-6 combines the signals which will activate RL17; bearing in mind that the polarized RL17 connections between its driver and the -7.5V rail are the reverse of all the other latching relays. Thus it closes its contacts when M19-6 is at logic-0 (-15V), **not** logic-1 (0V).

The signal states which cause RL17 to close its contacts are:

- $\overline{\Omega \text{ FNCT}}$ - logic-1 (Ohms function not selected);
- or $\Omega R2$ - logic-0 (10 Ω , 100 Ω , 1k Ω , or 10k Ω selected);
- or $\Omega \text{ ZERO}$ - logic-1 (Ohms Zero selected);
- or **J18-1** - logic-1 (Clamp assembly M2 Q4 @ logic-1 - 100k Ω range selected).

10.4.6.3 Ohms Zero.

The $\overline{\Omega \text{ FUNCT}}$ and $\Omega \text{ ZERO}$ signals are NORed by M19-10 and inverted by M17-12 so that RL16 is activated either when the Ohms function has been selected and the Zero Key has been pressed, or at times when the Ohms function is not selected.

| Range | Range Code (ΩR_{2-0}) | | | M2 'Q' Output (Clamp Assembly) | Relays Activated (All latching relays) | |
|--|------------------------------------|--------------|--------------|-----------------------------------|---|---|
| | ΩR_2 | ΩR_1 | ΩR_0 | | | |
| 10 Ω | 0 | 0 | 0 | Q0 | RL13 |) |
| 100 Ω | 0 | 0 | 1 | Q1 | RL10 |) |
| 1k Ω | 0 | 1 | 0 | Q2 | RL14 |) |
| 10k Ω | 0 | 1 | 1 | Q3 | RL12 |) |
| 100k Ω | 1 | 0 | 0 | Q4 | RL11 |) |
| 1M Ω | 1 | 0 | 1 | Q5 | RL20 |) |
| 10M Ω | 1 | 1 | 0 | Q6 | RL19 |) |
| 100M Ω | 1 | 1 | 1 | Q7 | RL18 |) |
| $\Omega \text{ Zero}$ | (All Range relays deselected) | | | | RL16 | Relay selects when pin 1 = Logic-1 (0V) |
| Ranges <1MΩ (excluding $\Omega \text{ Zero}$) | | | | | RL17 | Relay selects when pin 12 = Logic-1 (0V) |

TABLE 10.3 OHMS RANGING LOGIC

10.4.7 DEFAULT AND STATUS LOGIC

10.4.7.1 'OFF'

The OFF signal is combined with the $\overline{I\text{FNCT}}$ and $\overline{\Omega\text{FNCT}}$ signals to ensure that when the instrument OUTPUT OFF key is pressed, the selected function's circuitry is disconnected from the terminals. For Current outputs, RL8 and RL9 disconnect the terminals from the current output; and for Resistance, RL24 and RL25 disconnect the standard resistor.

10.4.7.2 'BARK'

The BARK signal is combined with the $\overline{\Omega\text{FNCT}}$ and DC I signals to ensure that when the Watchdog barks, the selected function is disabled. For DC Current outputs, RL7 disconnects the REF signal from the High-current V-to-I converter; for AC Current outputs, RL26 disconnects the drive from the AC reference V-to-I converter to the High current amplifier; and for Resistance, RL24 and RL25 disconnect the standard resistor.

The effects of $\overline{\text{BARK DELAYED}}$ follow after 47ms.

10.4.7.3 $\overline{\text{BARK DELAYED}}$

If the Watchdog is activated, the BARK signal is generated, and 47ms later all outputs from the Control Data latches in the Reference Divider are 'Tristated' by the $\overline{\text{BARK DELAYED}}$ signal. On the Current/Ohms assembly, this allows the pull-up resistors (AN1) and pull-down resistors (AN3) to become effective. At the same time the $\overline{\text{BARK DELAYED}}$ signal sets a -15V pulse on the $\overline{\text{UPD (IG)}}$ line for 1.5 seconds (M41 on *page 11.4-5*), to ensure that the latching relays on the DC and Current/Ohms assemblies will respond to the default state.

The full effect of the default is that relays RL5, RL16, RL17 and RL23 are activated, the remainder are not:

The Current and Ohms circuits are disconnected from the terminals, but relay RL23 connects the Power and Sense lines from the DC assembly to the terminals. However, on the DC assembly the same default has disconnected the voltage output from the lines.

The Current ranges are deselected, but relay RL5 holds the HF filter in circuit.

All Ohms standard resistors are deselected as well as disconnected from the terminals; the 4-wire Ohms-Zero short is activated, but is also isolated from the instrument terminals by RL24 and RL25.

As the Watchdog detects certain malfunctions in processor or Analog Control transfer operation, the default is a safe holding state, and subsequent changes will depend on the reaction of the CPU to the event. The Watchdog is described in *sub-section 6.4.6*.

10.4.7.4 'I/Ω ST'

The I/Ω ST line at J8-98 is pulled down to -15V (logic-0) for as long as the Current/Ohms assembly is fitted in the instrument. This state is passed back via the Reference Divider (J4-68) and the SSDA serial link to the CPU (Circuit Diagram 430652 *page 11.4-4*). Thus the CPU recognizes that the Current/Ohms assembly is fitted, and can operate the appropriate programs.

TERMS AND CONDITIONS OF SALE

1. GENERAL

The acceptance of a quotation, of any goods supplied, advice given or service rendered includes the acceptance of the following terms and conditions and no variation of or addition to the same shall be binding upon us unless expressly agreed in writing by us. Any order shall be subject to our written acceptance.

2. QUOTATION

Unless previously withdrawn our quotation is open to acceptance in writing within the period stated or where no period is stated within thirty (30) days after its date. We reserve the right to correct any errors or omissions in our quotation. Unless otherwise stated all quotations are firm and fixed. The prices quoted are based on manufacture of the quantity and type ordered and are subject to revision when interruptions, engineering changes or changes in quantity are caused or requested by the customer.

3. LIABILITY FOR DELAY

Any delivery times quoted are from the date of our written acceptance of any order and on receipt of all information and drawings to enable us to put the work in hand. Where delivery is to take place by instalments each such instalment shall constitute a separate contract. We will use our best endeavours to complete delivery of the goods or services in the period stated but accept no liability in damages or otherwise for failure to do so for any cause whatsoever. In all cases of delay the delivery time shall be extended by reasonable period having regard to the cause of delay.

4. PAYMENT

Payment shall be made net cash within thirty (30) days of delivery or in accordance with the payment terms set out in the quotation. Unless specifically stated to the contrary payment shall be in pounds sterling. In the event of any payment to us being overdue we may without prejudice to any other right suspend delivery to you or terminate the contract and/or charge you simple interest on overdue amounts at the rate of 2.5% above the ruling Bank of England Minimum Lending Rate. No payment to us shall in any circumstance be offset against any sum owing by us to you whether in respect of the present transaction or otherwise.

5. INSPECTION & TEST

All goods are fully inspected at our works and where practicable subjected to our standard tests before despatch. If tests are required to be witnessed by your representative notice of this must be given at the time of placing the order and notice of readiness will then be given to you seven (7) days in advance of such tests being carried out. In the event of any delay on your part in attending such tests or in carrying out inspection by you after seven (7) days notice of readiness the tests will proceed in your absence and shall be deemed to have been made in your presence and the inspection deemed to have been made by you. In any event you shall be required promptly after witnessing a test or receiving test results of witnessed or unwitnessed tests to notify us in writing of any claimed defects in the goods or of any respect in which it is claimed that the goods do not conform with the contract. Before you become entitled to reject any goods we are to be given reasonable time and opportunity to rectify them. You assume the responsibility that the goods stipulated by you are sufficient and suitable for your purpose and take all steps to ensure that the goods will be safe and without risk to health when properly used. Any additional certification demanded may incur extra cost for which a special quotation will be issued.

6. DELIVERY AND PACKING

All shipments are, unless otherwise specifically provided, Ex-works which is the address given on the invoice. An additional charge will be made for carriage and insurance as necessary with the provision that all shipments shall be insured and this insurance expense shall be paid by the purchaser. Where special domestic or export packing is specified a charge will be made to cover the extra expense involved.

7. DAMAGE IN TRANSIT

Claims for damage in transit or loss in delivery of the goods will only be considered if the carriers and ourselves receive notice of such damage within seven (7) days of delivery or in the event of loss of goods in transit within fourteen (14) days of consignment.

8. TRANSFER OF PROPERTY & RISK

Title and property of the goods shall pass when full payment has been received of all sums due to us whether in respect of the present transaction or not. The risk in the goods shall be deemed to have passed on delivery.

9. WARRANTY

We agree to correct, either by repair, or at our election, by replacement, any defects of material or workmanship which develop within the warranty period specified in the sales literature or quotation after delivery to the original purchaser. All items claimed defective must be promptly returned to us carriage paid unless otherwise arranged and will be returned to you free of charge. Unless otherwise agreed no warranty is made concerning components or accessories not manufactured by us. We will be released from all obligations under warranty in the event of repairs or modifications made by persons other than our own authorised service personnel unless such repairs are made with our prior written consent.

10. PATENTS

We will indemnify you against any claim of infringement of Letters Patent, Registered Design, Trade Mark or Copyright (published at the date of the contract) by the use or sale of any goods supplied or service rendered by us to you and against all costs and damages which you may incur and for which you may become liable in any action for such infringement. Provided always that this indemnity shall not apply to any infringement which is due to our having followed a design or instruction furnished or given by you or to the use of such goods or service in association or combination with any other article, material or service not supplied by us. This indemnity is conditional on your giving to us the earliest possible notice in writing of any claim being made or action threatened or brought against you and on your permitting us at our own expense to conduct litigation that may ensue and all negotiations for a settlement of the claim or action. You on your part warrant that any design or instruction furnished or given by you shall not cause us to infringe any Letter Patent, Registered Design, Trade Mark or Copyright in the execution of your order.

11. DOCUMENTATION

All drawings, plans, designs, software specifications, manuals and technical documents and information supplied by us for your use or information shall remain at all times our exclusive property and must not be copied, reproduced, transmitted or communicated to a third party without our prior written consent.

12. FRUSTRATION

If any contract or any part of it shall become impossible of performance or otherwise frustrated we shall be entitled to a fair and reasonable proportion of the price in respect of the work done up to the date thereof. For this purpose any monies previously paid by you shall be retained against the sum due to us under this provision. We may dispose of the goods as we think fit due allowance being made to you for the net proceeds thereof.

13. BANKRUPTCY

If the purchaser shall become bankrupt or insolvent, or being a Limited Company commence to be wound up or suffer a Receiver to be appointed, we shall be at liberty to treat the contract as terminated and be relieved of further obligations. This shall be without prejudice to our right to claim for damages for breach of contract.

14. LEGAL INTERPRETATION

Any contract will be deemed to be made in England and shall be governed and construed for all purposes and in all respects in accordance with English Law and only the Courts of England shall have jurisdiction.



Datron Sales and Service Representatives Worldwide

| COUNTRY and REPRESENTATIVE | Telephone | Telex | Fax |
|--|----------------------|---------------------------------|----------------------|
| AUSTRALIA | | | |
| Scientific Devices Pty. Ltd 2 Jacks Road, South Oakleigh, Victoria 3167 | 3 579 3622 | AA32742 | 3 579 0971 |
| AUSTRIA | | | |
| Walter Rekirsch Elektronisch Geraete GmbH & Co. Obachgasse 28, A-1220 Wien | 222 253626 | 134759 | 222 2572 75 |
| BELGIUM | | | |
| Air-Parts International B. V. Avenue Huart-Hamoir, 1-Box 34, 1030 Bruxelles | 2 241 6460 | 25146 AP1 B | 2 241 8130 |
| BRAZIL | | | |
| Comercial Goncalves Rua Deocleciana, 77, Cep 01106 Ponte Pequena, Sao Paulo SP | 11 2294044 | 22104 34272 | ----- |
| CHINA | | | |
| Tianjin Zhong Huan Scientific Instruments Corp. No. 59 Zhao Jia Chang Street, Hong Qiao Section, Tianjin | Tianjin 753732 | ----- | ----- |
| DENMARK | | | |
| Instrutek A/S, Christiansholmsgade 8700 Horsens | 5 611100 | 61656 | 5 615 658 |
| EASTERN EUROPE | | | |
| Amtest Associates Ltd Amtest House, 75-79 Guildford Street, Chertsey, Surrey KT16 9AS, England | 0932 568355 | 928855 | 0932 561919 |
| EGYPT & MIDDLE EAST | | | |
| EPIC 20-22 Ashmoun St, PO Box 2682, Horriya, Heliopolis | 2 661767 2 669861 | 23033 CHAKA UN 23315 EPIC UN | 2 662839 2 668924 |
| FINLAND | | | |
| Profelec OY PO Box 67, 00421 Helsinki 42 | 0 566 4477 | 125225 PROFE SF | 0 566 2998 |

| COUNTRY and REPRESENTATIVE | Telephone | Telex | Fax |
|---|---|----------------------------------|------------------------|
| FRANCE | | | |
| M. B. Electronique 606 Rue Fourny, Zi de Buc, 78530 Buc | 1 39 568131 | 695414 | 1 39 565344 |
| WEST GERMANY | | | |
| WAVETEK Electronics GmbH Freisinger Straße 34, 8045 Ismaning | 0 89 96 09 49-0 | 5 212 996 WVTK D | 0 89 96 71 70 |
| GREECE | | | |
| American Technical Enterprises SA PO Box 3156 39, Agiou Konstantinou Street, Athens 10210. | 5240620 5240740 | 216046 ATE GR | 5249995 |
| HONG KONG | | | |
| Eurotherm (Far East) Ltd 18/F., Gee Chang Hong Centre, 65 Wong Chuk Hang Road, Hong Kong | 5 8140311 (Sales) 5 546391 (Service) | 72449 EFELD HX 72449 EFELD HX | 5 8735974 5 8700497 |
| INDIA | | | |
| Technical Trade Links 42, Navketan Estate, Mahakali Caves Road, Andheri (East), Post Box No. 9447, Bombay 400 093 | 22 6322412 | 1179261 TTL IN | 9122 634 2204 |
| IRELAND | | | |
| Euro Electronic Systems Unit 3, Greenmount House, Greenmount Office Park, Harolds Cross, Dublin BW. | 0001 535955 | ----- | 0001 534229 |
| ISRAEL | | | |
| DAN-EL Technologies Office 60, Pinkas St. Tel-Aviv 62151. | 3 453157 | 342105 | 3 459281 |
| ITALY(1) | | | |
| Sistrel SPA Via Pellizza da Volpedo 59 20092 Cinisello Balsamo, Milano | 02 618 1893 | 334643 | 02 618 2440 |
| ITALY(2) | | | |
| Sistrel SPA Viale Erminio Spalla 41 00142 Roma | 06 504 0273 | 625857 | 06 504 0067 |
| ITALY(3) | | | |
| Sistrel SPA Via Cintia Parco S. Paolo 35 80126 Napoli | 081 767 9700 | ----- | 081 766 1361 |
| JAPAN | | | |
| G & G Japan Inc No. 406, 12-14, 4-Chome, Hongoh, Bunkyo-ku, Tokyo | 3 8130971 | 2722884 ICHAIN J | 3 8159216 |

| COUNTRY and REPRESENTATIVE | Telephone | Telex | Fax |
|---|------------------|---------------|------------|
| KOREA | | | |
| Sama Trading Corporation CPO Box 2447, Seoul | 2 733 9336 | K26375 SAMATR | 2 733 8481 |
| MALAYSIA | | | |
| TME Systems Pte Ltd 21 Moonstone Lane, No. 06-01, Poh Leng Building, Singapore 1232 | 286 4608 | 786 37545 | 288 5935 |
| MOROCCO | | | |
| Minhol SA 64 Rue El Mortada, Casablanca 02. | 254945 | 24064 | 254969 |
| NETHERLANDS | | | |
| Air Parts International BV PO Box 255, 12 Kalkoverweg, 2400 AG Alphen aan den Rijn | 1720 43221 | 39564 | 1720 20651 |
| NEW ZEALAND | | | |
| G. T. S. Engineering Ltd 5 Porters Avenue, Eden Terrace, PO Box 9613 Newmarket AUCKLAND | 9 392 464 | ----- | 9 392 968 |
| NORWAY | | | |
| Morgenstjerne & Co. Olaf Helsets vei 1, P.O. box 15 - Bogerud N-0621 Oslo 6 | 2 289490 | 71719 MOROF N | 2 289494 |
| PORTUGAL | | | |
| Decada SA Rua Margarida, Palla. 11, 1495 Alges. | 1 4103420 | 24476 ESPEC P | 1 4101844 |
| SAUDI ARABIA | | | |
| Electronic Equipment Marketing PO Box 3750, Riyadh 11481, | 1 4771650 | 401120 | 1 4785140 |
| SINGAPORE | | | |
| Mecomb Singapore Ltd Sime Darby Centre, 895 Dunearn Road, 04-2 Singapore 2158 | 469 8833 | RS 23178 | 467 1905 |
| SOUTH AFRICA | | | |
| Altech Instruments (Pty) Ltd PO Box 39451, Wynberg 2018 | 11 887 7455 | 422033 | ----- |
| SPAIN | | | |
| ESSA (Equipos y Systemas SA) C/Apolonio Morales 13-B, Madrid 16 | 1 458 0150 | 831 42856 | ----- |

| COUNTRY and REPRESENTATIVE | Telephone | Telex | Fax |
|--|------------------|-----------------------|----------------|
| SWEDEN | | | |
| Ferner Electronics AB Snormakarvagen 35, Box 125, S-16126 Stockholm-Bromma | 8 802540 | 10312 FERNER S | 8 250226 |
| SWITZERLAND | | | |
| Kontron Electronic AG Bernerstrasse-Süd 169, 8048 Zurich | 1 435 4111 | 822196 + KOEL CH | 1 432 2464 |
| TAIWAN | | | |
| Evergo Corporation Room A, 9th Floor, 305 Section, 3 Nan King East Road, P. O. Box 96-546, Taipei | 2 7150283/4/5 | 27027 EVERGOEC | 2 7122466 |
| UNITED KINGDOM | | | |
| Datron Instruments Ltd Hurricane Way, Norwich Airport, Norwich, Norfolk NR6 6JB, England | 0603 404824 | 975173 | 0603 483670 |
| UNITED STATES of AMERICA | | | |
| Datron Instruments Inc c/o Wavetek RF Products Inc. 5808 Churchman Bypass, Indianapolis, Indiana 46203 | (317) [REDACTED] | TWX (810) 341 3226 | (317) 788 5999 |
| Wavetek Northeast Area Sales 1 Executive Blvd. Suite 206, Suffern New York 10901 | (914) 357 5544 | ---- | (914) 357 5609 |
| Wavetek Western Area Sales 9045 Balboa Avenue, San Diego, California 92123 | (619) 565 9234 | TWX (910) 335 2007 | (619) 565 9558 |

For customers in countries not listed please contact DATRON INSTRUMENTS in the United Kingdom:

| | | | |
|---|-------------|--------|-------------|
| Datron Instruments Ltd Hurricane Way, Norwich Airport, Norwich, Norfolk NR6 6JB, England | 0603 404824 | 975173 | 0603 483670 |
|---|-------------|--------|-------------|

**Model 4708 -
Calibration and Servicing Handbook Vol. 1
Part No: 850246 Issue: 1**

Instrument Serial Number

24029-6

These advice sheets apply only to the instrument whose serial number is given above.

Introduction

Pre-Calibration - Improved Procedure

In Section 1, Sub-section 1.6.2; page 1-35 deals with the pre-calibration of the Full Range : 10% Full Range ratio. This addendum introduces an improved procedure for this pre-calibration, by providing a revised page 1-35.

The Volume 1 of the Calibration and Servicing Handbook for Model 4708 contains technical circuit descriptions.

AC 1V Buffer - Increased Output Current Capability

Section 9 describes the Amplitude Control System, and Sub-section 9.3 deals with the AC 1V Buffer. Paras 9.3.1.2 and 9.3.1.3 on page 9-16 refer to current levels in the AC 1V Buffer stage, and to the threshold levels of the output current detector circuit.

This addendum corrects these current levels for an upgraded output capability of 50mA from the 1V Buffer, with consequent changes to the overcurrent threshold levels.

The effects of this upgrade are to generate the Error OL fault condition at a higher output current threshold on the 1V AC range than hitherto.

In Section 2, (Page 2-8) the diagnostic guide for Error OL is amended by this addendum.

AC 1000V Range - Improvement to HF Transformer Performance

In Section 9, Sub-section 9.7 deals with the AC 1000V Range. Paras 9.7.5.2 on page 9-16 refer to selection of the appropriate step-up HF transformer.

This addendum adds a new paragraph 9.7.5.4, dealing with the introduction of a high wattage damping resistor to counter possible resonances in the 750V secondary of the HF Transformer.

This upgrade affects the dismantling and reassembly of the LF and HF Transformer Assemblies.

In Section 3, (Pages 3-10 and 3-11) the dismantling and reassembly procedures are amended by this addendum.

Options

The 4708 offers optional functions to suit user requirements.

Contract No. F33659-90-C0065 specifies AC voltage (Option 20) and AC Current (Option 30) functions only.

This handbook provides information on the whole range of options provided for the instrument. Users are therefore requested to ignore information related to options which were not purchased.

Specifically:

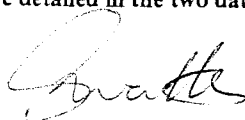
Because Option 10 was not ordered, the DC Assembly (part no. 400536, subsection 11.5) is not fitted in this instrument. Instead, the Output Control Assembly (400909; 11.5), resides in the same PCB slot.

Option 30 can cover three functions: DC Current, AC Current and Resistance; depending on other options fitted.

If Resistance is ordered, the 'Current/Ohms' PCB Assembly (part no. 400614; 11.8) is used. Because Resistance was not ordered, the Current Option PCB Assembly (401008; 11.8) is fitted in this instrument. This provides AC Current function, in conjunction with Option 20. All references to 'Current/Ohms Assembly' and part no. '400614' should be read as 'Current Option Assembly' and part no. '401008'

The above minor changes are detailed in the two data pages attached to this sheet.

Checked by:



Date:

22nd May '92

**Model 4708 -
Calibration and Servicing Handbook Vol. 1
Part No: 850246 Issue: 1**

Instrument Serial Number

24029-6

These advice sheets apply only to the instrument whose serial number is given above.

Introduction

AC Outputs - Improvement to Frequency Control System

In **Section 8**, Sub-section 8.1 deals with the Digital Frequency Synthesizer. Paras 8.1.2 on pages 8-1 to 8-3 describe the operation of the Voltage Controlled Oscillator.

This addendum changes paras 8.1.2, dealing with the introduction of an integrated VCO chip to replace the discrete VCO previously used, and modifications to the associated circuitry.

This upgrade improves the reliability and maintainability of the Digital Frequency Synthesizer by reducing the critical component count and easing fault diagnosis.

Contract No. F33659-90-C0065 specifies AC voltage (Option 20) and AC Current (Option 30) functions only. Therefore this addendum is pertinent to the contract

The above minor changes are detailed below.

Amendments to Section 8

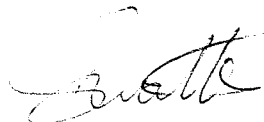
Pages 8-1, 8-2 and 8-3:

Delete the existing pages and substitute the new pages 8-1, 8-2 and 8-3 attached.

Amendments to the Contents and Illustrations List

No changes are required.

Checked by:



Date:

22nd May 92

SECTION 8 AC VOLTAGE OUTPUTS - FREQUENCY CONTROL SYSTEM

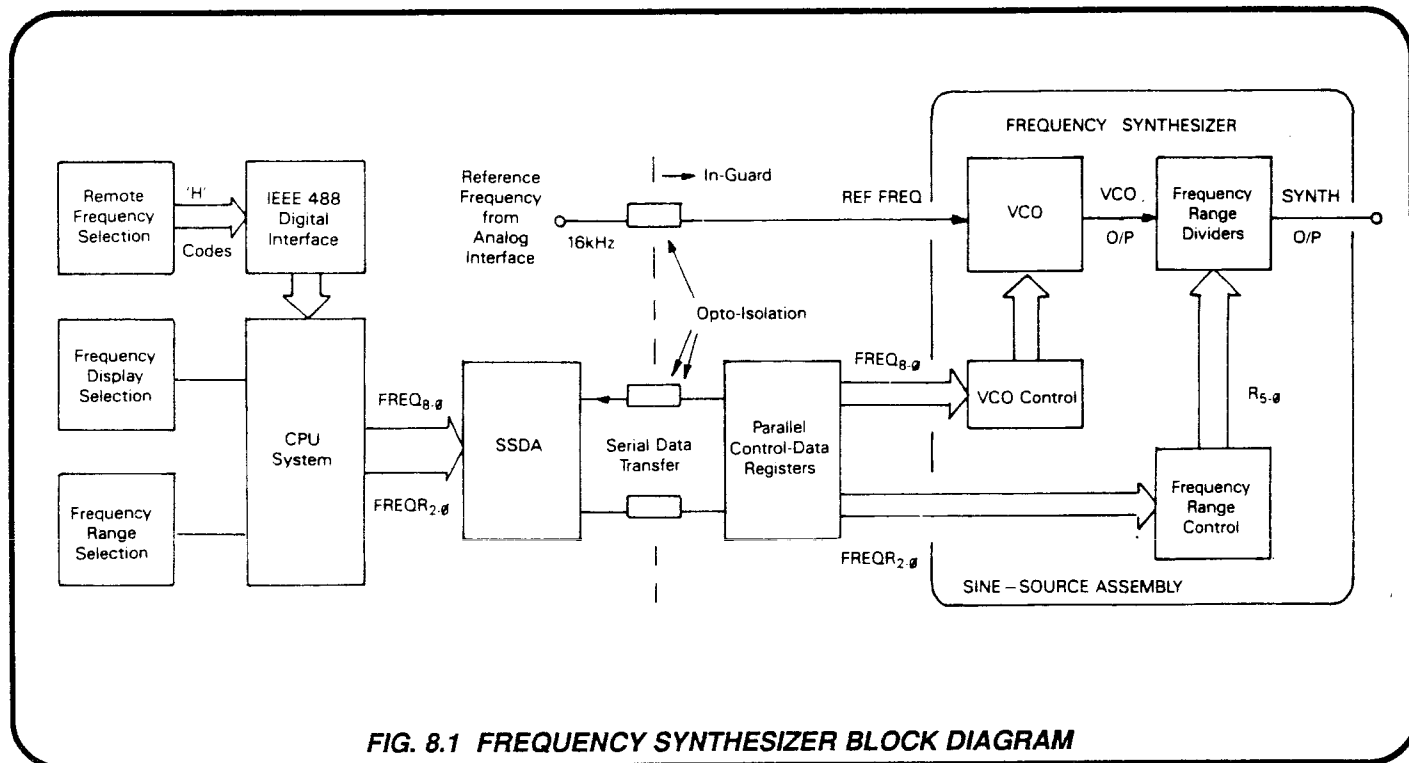


FIG. 8.1 FREQUENCY SYNTHESIZER BLOCK DIAGRAM

8.1 DIGITAL FREQUENCY SYNTHESIZER

(Fig. 8.1)

8.1.1 GENERAL

Users normally set the operating frequency by a combination of 'FREQUENCY RANGE' and 'FREQUENCY' display selections. These are memorized by the CPU and translated into two binary control words:

'FREQ R_{2-θ}'

A three-bit word, five of whose codes represent the five frequency ranges.

'FREQ_{8-θ}'

A nine-bit word whose value 'n' defines the chosen frequency with respect to the selected frequency range.

Users can select a frequency by means other than pressing a FREQUENCY RANGE key and setting a frequency on the display; for example by using 'Store' or the IEEE 488 digital interface. But regardless of the selection method, the CPU will always compute the two binary words, which then synthesize the selected frequency in the Sine-Source Assembly.

Both words are passed into guard via the SSDA, and latched at the outputs of the Reference Divider Parallel Control registers. A 16kHz reference frequency is also taken into guard, to be divided by two to 8kHz in the Sine-Source assembly.

After entering the Sine-Source assembly, FREQ_{8-θ} effectively multiplies the 8kHz reference by a factor 'n' to determine the frequency of a Voltage Controlled Oscillator (VCO). The VCO frequency (signal 'VCO O/P') is input into a series of frequency dividers, whose ratios are set by FREQ R_{2-θ}. The division ratios are chosen so as to make the dividers generate the Frequency Synthesizer output signal ('SYNTH O/P') at the user-selected frequency.

The purpose of the synthesizer is to provide an accurate frequency reference for the quadrature sinewave oscillator. The oscillator is approximately tuned by selection of circuit constants using the combination of 'FREQ R_{2-θ}' and 'FREQ_{8-θ}'.

'SYNTH O/P' acts as the reference in the phase comparator of a Phase-Locked Loop, controlling the frequency of the main Quadrature Sinewave Oscillator to an accuracy determined by the crystal oscillator.

8.1.2 VOLTAGE CONTROLLED OSCILLATOR

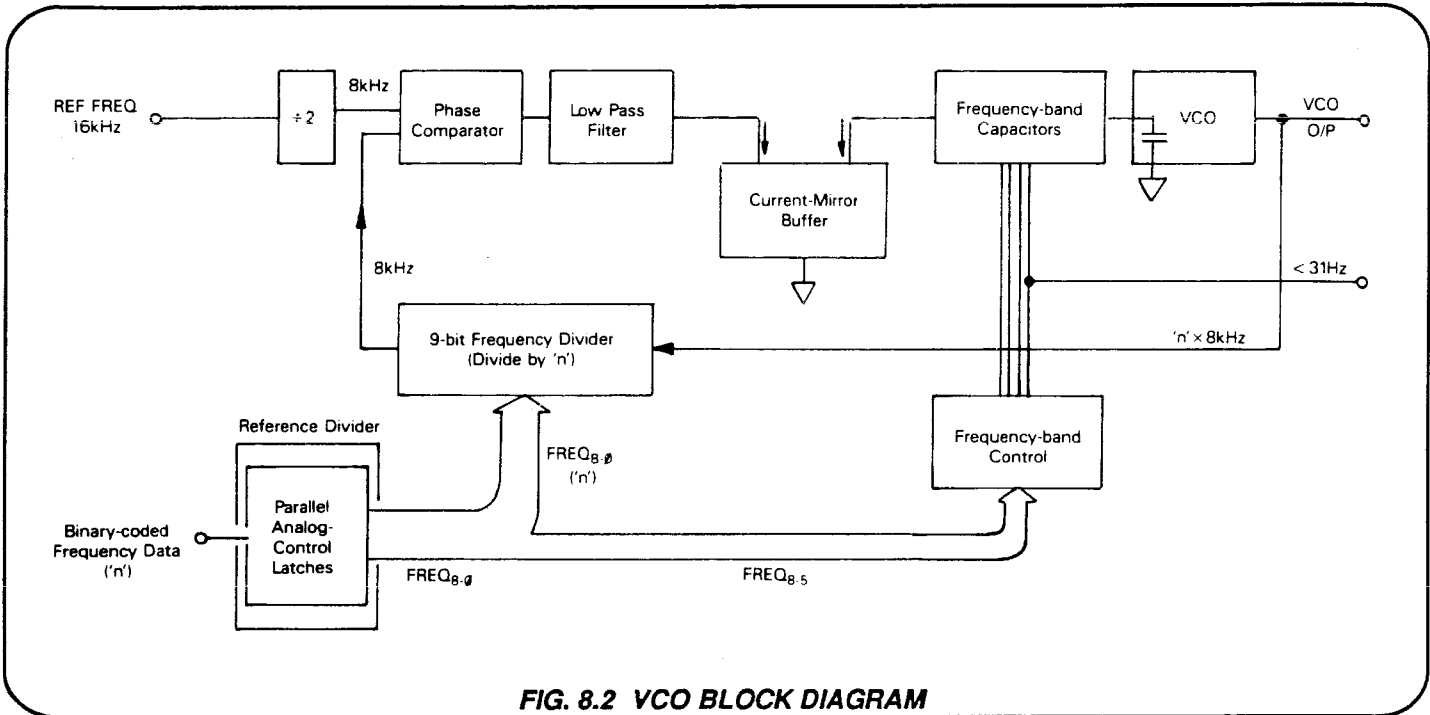


FIG. 8.2 VCO BLOCK DIAGRAM

8.1.2.1 Generation of 16kHz Reference

(Circuit Diagrams 430648 page 11.3-2, 430652 page 11.4-5 and 430446 page 11.6-4)

The 16kHz (INT) signal originates at M16-14 in the Analog Interface (page 11.3-2) and is buffered as '16kHz(OG)' (page 11.3-1). On the Reference Divider at J4-104, it passes into guard via opto-isolator M3 (page 11.4-5), gating with 'DISABLE REF FREQUENCY' and 'BARK' in M24, filtered by R86/C38 to reduce harmonics from the transmission path, and is sent via the Mother Assembly to J6-53 on the Sine-Source Assembly (page 11.6-4).

Schmitt-trigger M14 inverts the 16kHz into a symmetrical squarewave, which is then applied as clock to M13a, a bistable connected to divide by two. The resulting 8kHz squarewave is taken as the reference frequency for phase comparator M12. Note that in this configuration the SIG input of M12 is used for the reference, and the divided VCO output signal is applied to the REF input. This is necessary to provide the correct sense in the phase control element M50, because of the inversion of integrator M11.

8.1.2.2 Squarewave Generation by the VCO

The VCO is a discrete-component ECL relaxation oscillator generating an output of frequency ' $n \times 8\text{kHz}$ '. Its natural frequency is dependent on:

- the value of capacitor C2 (or C2 plus one of C3 - C6),
- the value of its continuous discharge current through the phase control element (current mirror M50), and
- the value of its charging current through Q2 on alternate half cycles (4.7mA).

Consider C2 fully discharged. Q4 is off, so all the 4.7mA from Q6 passes through Q5. The collector voltage of Q4 is close to the positive rail, buffered by Q7 and R9 to hold Q5 on. Also, as Q3 is turned off by Q4 collector voltage, Q2 is turned on by its emitter, passing 4.7mA into C2 and the current mirror M50.

Capacitor C2 charges until Q4 turns on. Cumulative Schmitt action passes the fall at Q4 collector to the base of Q5, ensuring a rapid transition between states; so the 4.7mA is transferred from Q5 to Q4. Q3 turns on, its emitter falling quickly to cut Q2 off, so the charging path to C2 etc. is interrupted.

M50 continues to discharge C2, whose voltage falls slowly until Q4 starts to cut off again. The cumulative action is repeated to turn Q2 on, recharging C2. The cycle of charge and discharge continues, generating 'VCO O/P' squarewaves at buffer Q12 emitter.

8.1.2.3 Coarse Frequency Control

(Circuit Diagram 430446 Page 11.6-4, and Fig. 8.2)

At any time, only one of the capacitors C3, C4, C5 and C6 can be connected in parallel with C2, by conduction of its associated transistor. This splits the frequency range of the VCO into five bands, governed by the four most-significant bits of the frequency control word $\text{FREQ}_{8,0}$ acting on M8. The association is shown in Table 8.1; note that the VCO frequency bands quoted in the table are correct only because the VCO is under the fine control of comparator M12, within the phase-locked loop.

| FREQ ₈₋₅ bits 8 7 6 5 | Range of 'n' Values | M8 Outputs at Logic-1 | C2-C6 Selection | VCO Frequency Band (kHz) |
|-------------------------------------|------------------------|-----------------------------|--------------------|--------------------------------|
| 0 0 0 0 | 10 to 31 | X ₀ | C2 and C6 | 80 to 248 |
| 0 0 0 1 | 32 to 63 | X ₁ | C2 and C5 | 256 to 504 |
| 0 0 1 X | 64 to 127 | X ₃₋₂ | C2 and C4 | 512 to 1016 |
| 0 1 X X | 128 to 255 | X ₇₋₄ | C2 and C3 | 1024 to 2040 |
| 1 X X X | 256 to 500 | NONE | C2 only | 2048 to 4000 |

TABLE 8.1 COARSE FREQUENCY CONTROL

8.1.2.4 Fine Frequency Control

(Circuit Diagram 430446 Page 11.6-4, and Fig. 8.2)

In the following description, capacitors C3, C4, C5 and C6 are ignored, but references to C2 should be read as including the appropriate additional capacitor.

The VCO output is fed back to M12 phase comparator via M9 and M13b, which are connected to act as a 9-bit frequency divider. Because the divider is controlled by FREQ₈₋₀, the VCO output frequency is always divided by 'n' before being applied to the REF input of the comparator. The output from the comparator will only be zero if the frequency fed back to M12-6 is 8kHz (ie. the VCO frequency is n x 8kHz), and in phase with the 8kHz REF FREQ at M12-3 (TP14).

The output from M12 is integrated by M11 to drive a DC current into the current mirror M50, which has a gain of two, its output current being drawn from the charge on C2. During the half-cycles of the VCO oscillation when C2 is being charged, the mirror obtains its current from Q2 conduction.

The phase control loop seeks to phase-lock the two inputs to the comparator. If they are in phase, the comparator output is at high impedance ('TRISTATE'). In this condition the integrator capacitors C16 and C18 have no charge or discharge path, so M11's extremely high gain maintains their charge, and thus the voltage at TP6. M11 supplies the input current for M50, the mirror continues to draw the same discharge current from C2, so the frequency of VCO oscillation remains constant. Thus the loop stabilizes only when the frequency divided by 'n' from the VCO output is in phase with (and therefore at the same frequency as) the reference 8kHz.

In stable operation, therefore, the loop maintains VCO oscillations at n x 8kHz, and the feedback dividers reduce this frequency by a factor of 'n' to 8kHz.

Any disturbance in the loop will generate corrections to restore zero phase difference at the inputs of M12. Frequency deviations are therefore detected at an early stage as phase changes, giving a measure of 'phase advance' correction.

8.1.2.5 'INHIBIT' (VCO Off)

The VCO can be switched off by a logic-1 of 0V at the base of Q11 (INHIBIT signal). This originates in the CPU system, setting FREQ R₂₋₀ code to 111 (a non-existent 'R7' range) when AC functions are deselected. It also resets the +2 flip-flop M13a, so that no reference frequency is passed into the phase comparator.

8.1.2.6 VCO Supply Rail Protection

To prevent VCO oscillations appearing on the 15V power rails, which also supply the integrator M11 and current mirror M50, the positive rail is heavily decoupled, regulated by Q8, and all devices whose currents are likely to disturb the rails are supplied through constant current sources (Q1, Q6, Q9 and Q13).

8.1.2.7 VCO Output

The VCO, M11 and M50 operate from the 15V supplies. M12, M9 and the frequency dividers which follow the VCO, all operate from the in-guard logic supplies of +0V and -15V. The VCO output from Q12 emitter is therefore limited by D1 to logic supply levels. A re-conversion back to 15V levels is accomplished at the input to the integrator M11, as TP31 pulses are negative at M11 input.

D1 is a Schottky hot carrier diode of reverse capacitance approx. 2pF. This avoids distorting the high frequency output squarewaves (for 1MHz output, the VCO oscillates at 4MHz).

The output passes through R12 to avoid loading the VCO, and then fed as 'VCO O/P' to the frequency dividers at M5-9 (page 11.6-5).

8.1.3 FREQUENCY RANGE DIVIDERS

(Fig 8.3)

As mentioned earlier in para 8.1.1, the purpose of the synthesizer is to provide an accurate frequency reference for the quadrature sinewave oscillator. The VCO frequency (signal 'VCO O/P') is input to a series of frequency dividers, whose ratios are set by 'FREQ R₂₋₀', so as to make the dividers generate the selected frequency as 'SYNTH O/P'. FREQ R₂₋₀ is a three-bit word, five of whose codes represent the five frequency ranges.

A second purpose is to clock the Quasi-Sinewave Generator in synchronism with the synthesizer output (and hence with the main quadrature sinewave oscillator output). The synthesizer frequency is a multiple of the Quasi-Sine frequency, except on the 100Hz frequency range, where they are both at the same frequency. Thus the divider ratios are also chosen to generate the correct frequencies for the quasi-sinewave clock, for each frequency range selected.

8.1.3.1 Divider Ratios

(Circuit Diagram 430446 Page 11.6-5)

Binary/BCD Divider M5 is set for binary division by fixing M5-2 and M5-10 at Logic-0. Conversely, M1 is set for decimal division by fixing M1-2 and M1-10 at Logic-1.

BCD counter M2 is set to count up, by fixing M2-10 at Logic-1. Its $\overline{\text{CARRY OUT}}$ signal at M2-7 is at 1/10 of its clock frequency, and its Q1 output on M2-6 is at half its clock frequency. Flip-flop M4a is connected to divide its clocks by two.

Multiplexer M6 selects the appropriate source frequency to clock the Quasi-Sinewave generator. In particular, on the 100Hz Range it selects the $\overline{\text{CARRY OUT}}$ from M2, which is subsequently divided by 10 in the quasi-sinewave counter, and returned via J6-51 to be used as SYNTH O/P.

8.1.3.2 Ratio Selection by Frequency Range
(Fig. 8.3 and Table 8.2)

The frequency range selection word $FREQ R_{2-0}$ is decoded by M29 into five range lines R_{4-0} . These lines perform the following functions:

- a. Switch ranges in the quadrature sinewave oscillator by relays RL1-RL8 selection of integrator capacitors (page 11.6-1);
- b. Switch ranges in the Cosine Squarer output filter (page 11.6-2);
- c. Adjust the division ratios of Frequency Range Dividers M5 and M1 (page 11.6-5) for range R_4 (1MHz Range),
- d. Select appropriate outputs from the Frequency Range Dividers (page 11.6-5); and
- e. The INHIBIT line turns off the VCO for non-AC functions.

Functions (a) and (b) are described later in Section 8.2. In this description we are concerned mainly with functions (c) and (d).

Table 8.2 shows how frequency range switching derives the synthesizer output frequencies by selecting the appropriate outputs from the dividers. Note that except for the 1MHz Range R_4 , the ratios of individual dividers are not altered.

On the 100Hz Range R_0 the overall division ratio of 8000 is achieved as for the 1kHz Range, but with a further division by 10 in the quasi-sinewave counter M11 on the AC Assembly.

On the 1MHz Range, R_4 , the division ratio of M5 is changed from 8 to 4. The DP_A inputs M5-5 and M5-6 are primed to Logic-1 and Logic-0 respectively, whereas on all other ranges the priming is reversed. Range R_4 also alters the division ratio of M1 from 10 to 25, by changing its priming bit-pattern, to correct the quasi-sinewave frequency; but as the synthesizer output is taken through M10-4/3 from M5 output, the adjustment to M1 does not affect the SYNTH O/P frequency.

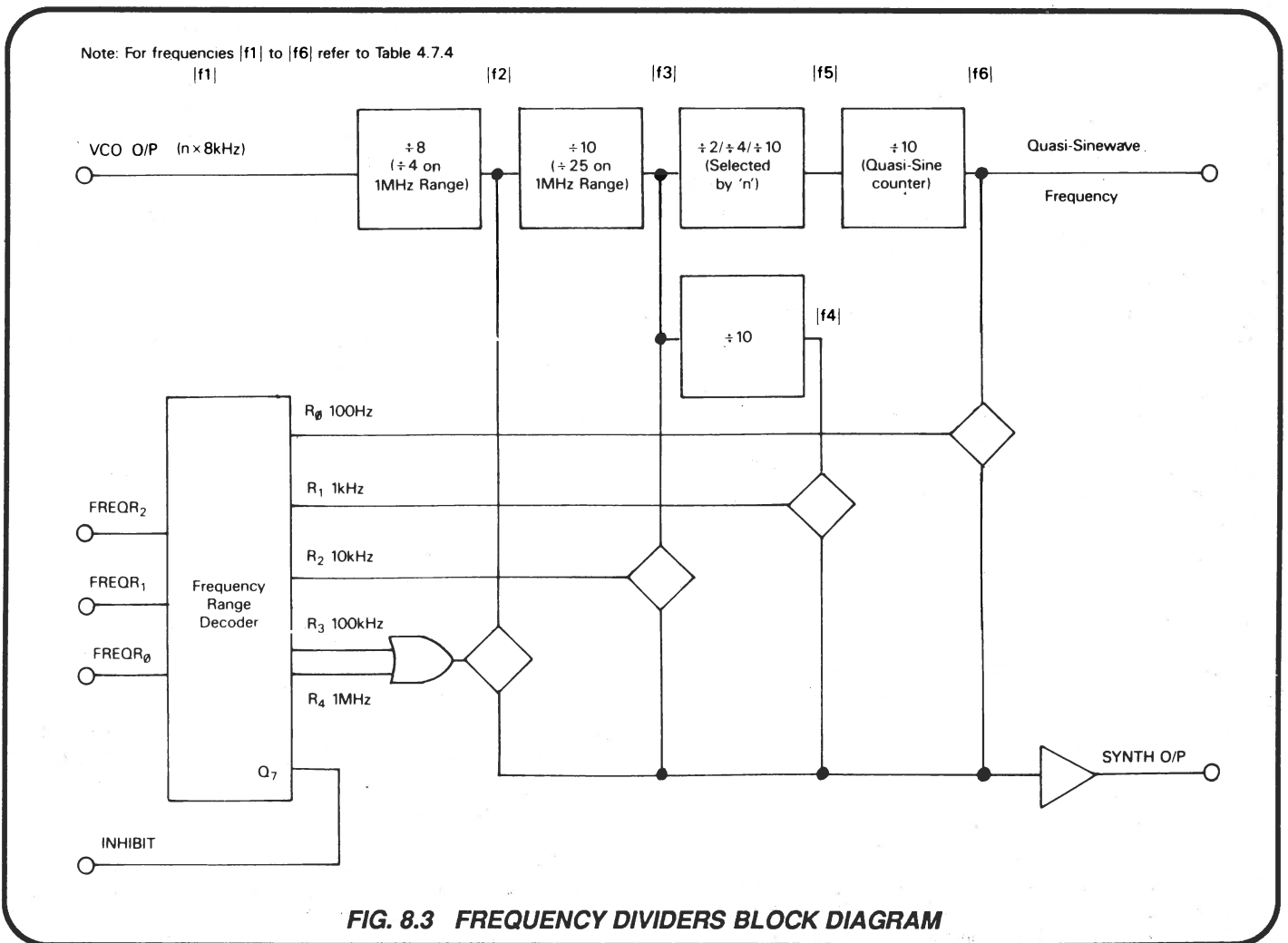


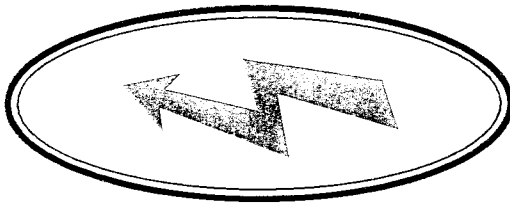
FIG. 8.3 FREQUENCY DIVIDERS BLOCK DIAGRAM



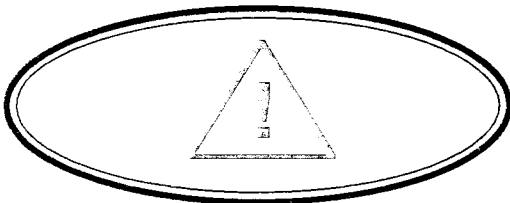
DANGER
HIGH VOLTAGE



THIS INSTRUMENT IS CAPABLE
OF DELIVERING
A LETHAL ELECTRIC SHOCK !
when connected to a high voltage source



FRONT or REAR terminals
carry the Full Input Voltage
THIS CAN KILL !



Guard terminal is sensitive to
over-voltage
It can damage your
instrument !

Unless you are sure that it is safe to do so,
DO NOT TOUCH
the I+ I- Hi or Lo leads and terminals

DANGER

PART 3

REFERENCE

SECTION 11 Servicing Diagrams

SECTION 12 Component Lists

SECTION 11 4708 SERVICING DIAGRAMS

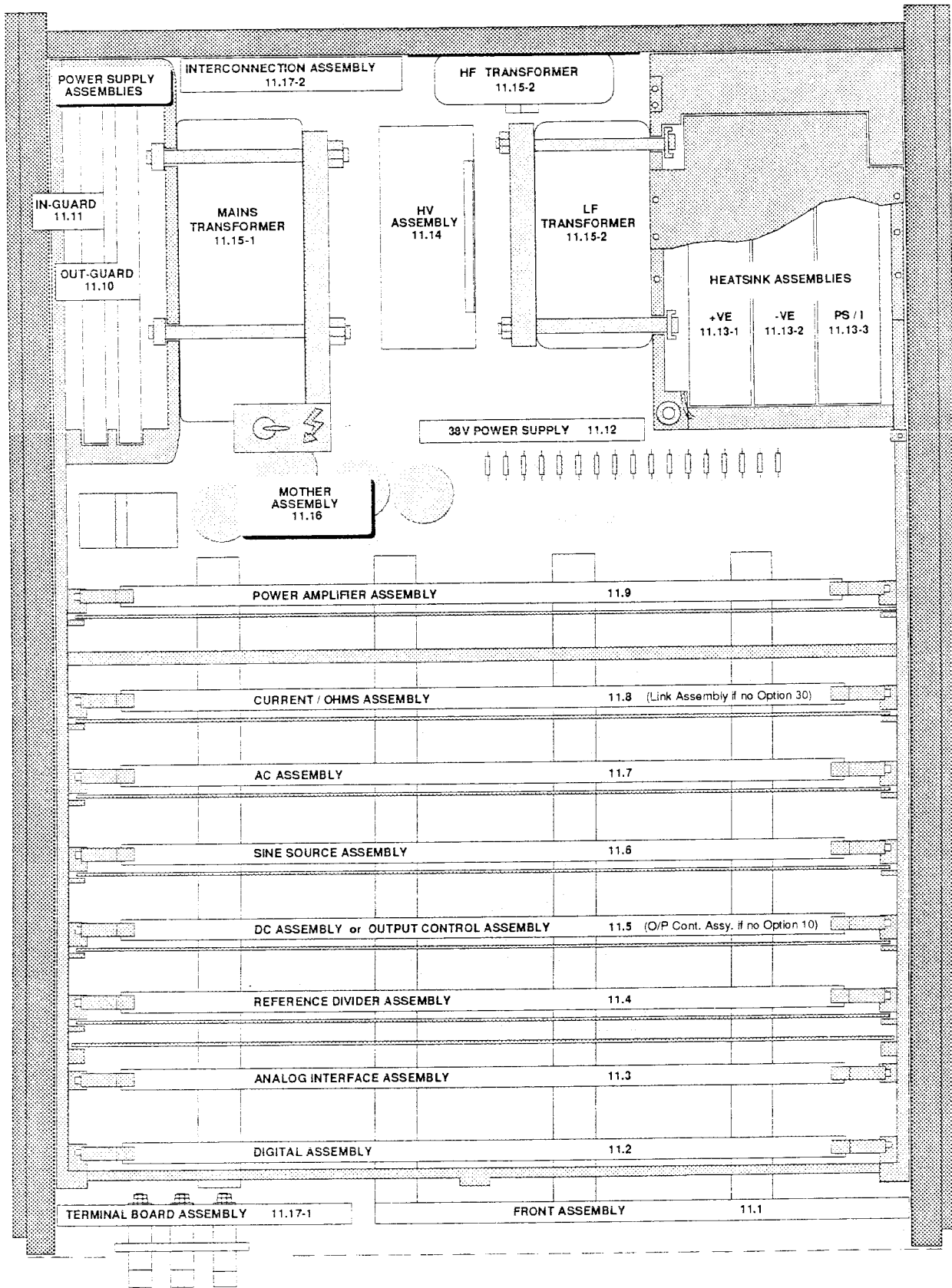


FIG. 11.1 ASSEMBLY LOCATIONS WITH INDEX

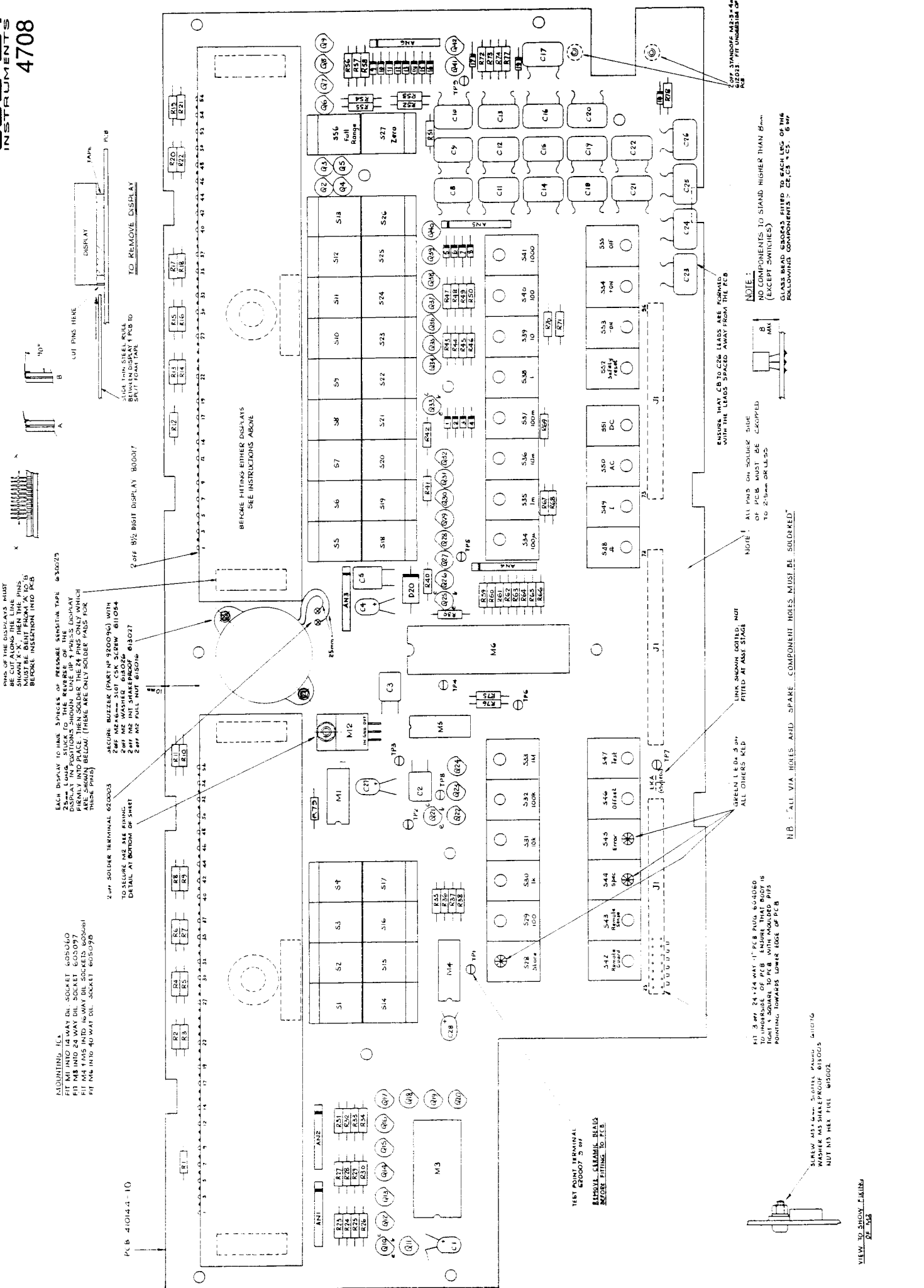
SECTION 11 4708 SERVICING DIAGRAMS

Contents

| | |
|--|--------|
| Front Assembly | |
| Keyboard Encoder and LED Driver | 11.1-1 |
| Display Driver High Voltage | 11.1-2 |
| Digital Assembly | |
| Display Multiplexing Logic | 11.2-1 |
| Microprocessor | 11.2-2 |
| Memory and Battery Backup | 11.2-3 |
| IEEE 488 Interface | 11.2-4 |
| I-C Power Supplies | 11.2-5 |
| Analog Interface Assembly | |
| Lower Reference Divider Counter | 11.3-1 |
| Upper Reference Divider Counter | 11.3-2 |
| Master Clocks and Analog Control Serial Link | 11.3-3 |
| Frequency Lock, Watchdog Driver and I-C Power Supplies | 11.3-4 |
| Reference Divider Assembly | |
| Most-Significant Switch and Filter | 11.4-1 |
| Least-Significant Switch and Filter | 11.4-2 |
| Summing Amplifier | 11.4-3 |
| Serial/Parallel Data Converter | 11.4-4 |
| Out/In Guard Interface and Watchdog | 11.4-5 |
| Power Supplies | 11.4-6 |
| Calibrator Reference Assembly | |
| Calibrator Reference Assembly | 11.4-7 |
| DC Assembly | |
| 100mV, 1V, 10V, 100V and 1kV Outputs | 11.5-1 |
| Output Switching and Overload Sense | 11.5-2 |
| Relay Drive Logic | 11.5-3 |
| Power Supplies | 11.5-4 |
| DC Clamp | 11.5-5 |
| Output Control Assembly | |
| Output Switching and Overload Sense | 11.5-6 |
| Relay Drive Logic | 11.5-7 |
| Power Supplies | 11.5-8 |
| Sine Source Assembly | |
| Sine Oscillator | 11.6-1 |
| Oscillator Amplitude-Detector and Reference | 11.6-2 |
| VCA, 1V Buffer and Current Detector | 11.6-3 |
| Digital Synthesizer | 11.6-4 |
| Frequency Range Dividers, Control Logic and Power Supplies | 11.6-5 |
| AC Assembly | |
| Switching Overview | 11.7-1 |
| Sense Amplifier and Reference Inverter | 11.7-2 |
| Quasi-Sine Generator and Timing Logic | 11.7-3 |
| AC/DC Transfer Detector and Integrators | 11.7-4 |
| Relay Drive Logic and Power Supplies | 11.7-5 |
| Phase Detector & Integrator and Power Supplies | 11.7-6 |
| Current / Ohms Assembly | |
| Voltage-to-Current Converter | 11.8-1 |
| Logic and Relay Drive | 11.8-2 |
| Standard Resistors and Switching | 11.8-3 |
| Current / Ohms Clamp | 11.8-4 |
| Power Amplifier Assembly | |
| Block Diagram | 11.9-1 |
| 10V and 1kV Amplifiers | 11.9-2 |
| 100V Amplifier | 11.9-3 |
| Power Supply Monitors | 11.9-4 |
| Logic and Relay Drives | 11.9-5 |
| 100V Overload Detector and Power Supplies | 11.9-6 |

| | |
|--|---------|
| Out-guard Power Supply Assembly | |
| Main Digital Supply, Display Supply and Common Mode Null | 11.10-1 |
| In-guard Power Supply Assembly | |
| Common-2 Supplies and Current Option Supply | 11.11-1 |
| Reference Common-4 and $\pm 8V$ Common-2 Supplies | 11.11-2 |
| $\pm 38V$ Power Supply Assembly | |
| $\pm 38V$ Power Supply with Mother Assembly Components | 11.12-1 |
| Heatsink Assemblies | |
| Output Power Amplifier (Positive Half) | 11.13-1 |
| Output Power Amplifier (Negative Half) | 11.13-2 |
| $\pm 400V(2)B$ Regulator; Current Option Output Stage | 11.13-3 |
| High Voltage Assembly | |
| High Voltage Switching and Logic | 11.14-1 |
| Constant Current Source Assembly | 11.14-2 |
| Transformer Assemblies | |
| Mains (Line) Transformer | 11.15-1 |
| L.F. and H.F. Transformer Assemblies | 11.15-2 |
| Mother Assembly (Edge Connector Pin Index with each Layout Drawing) | |
| Sheet 1 | 11.16-1 |
| Sheet 2 | 11.16-2 |
| Sheet 3 | 11.16-3 |
| Sheet 4 | 11.16-4 |
| Sheet 5 | 11.16-5 |
| Interconnections | |
| Circuit Diagrams Sheets 1 and 2 | 11.17-1 |
| Interconnection Assembly | |
| Connections with Power Input Module and Mains Transformer | 11.17-2 |
| Terminal Board Assembly | |
| Sheet 1 | 11.17-3 |
| Instrument Assembly | |
| 4708 Sheet 1 | 11.18-1 |
| Main Assembly Layout Drawings | |
| Sheet 1 | 11.18-1 |
| Sheets 2 and 3 | 11.18-2 |
| Chassis Assembly Layout Drawings | |
| Sheets 1 and 2 | 11.18-3 |
| Sheets 3 and 4 | 11.18-4 |
| Sheets 5 and 6 | 11.18-5 |
| Sheet 7 | 11.18-6 |
| Rear Panel Assembly | |
| Rear Panel Assembly | 11.18-6 |
| Option Fitting Instructions | |
| Option 20: Current / Ohms | 11.19-1 |
| Option 80: 115V 60Hz | 11.19-1 |
| Option 90: Rack Mounting | 11.19-1 |
| Option 42: Rear Output | 11.19-2 |
| Option 10: DC Voltage | 11.19-3 |
| Option 20: AC Voltage | 11.19-3 |
| Digital Assembly: Fitted Options Switch Positions | 11.19-3 |

FRONT ASSEMBLY



PINS OF THE DISPLAYS MUST BE CUT ALONG THE LINE SHOWN. ALL PINS MUST BE BENT FROM 'A' TO 'B' BEFORE INSERTION INTO PCB.

EACH DISPLAY TO HAVE 3 PIECES OF PRESSURE SENSITIVE TAPE (3.0x2.5) 25mm LONG. STICK TO THE REVERSE OF THE DISPLAY. STICK THE TAPE INTO THE DISPLAY. THE 84 PINS ONLY WHICH ARE SHOWN BELOW (THERE ARE ONLY SOLDER PADS FOR THESE PINS)

SECURE BUZZER (PART NO 320076) WITH 2mm MEASURED SLOT CSK 5.4x7mm 611054 2mm MEASURED 618026 618027 2mm MEASURED 618026 618027

2mm SOLDER TERMINAL 602003 TO SECURE M2 SIE PIPING DETAIL AT BOTTOM OF SHEET

ACCOUNTING, I.C.A.
FIT M1 INTO 14 WAY DIL SOCKET 605060
FIT M3 INTO 24 WAY DIL SOCKET 605097
FIT M4 INTO 16 WAY DIL SOCKET 605091
FIT M5 INTO 40 WAY DIL SOCKET 605096

PCB 41014.3-1.0

BEFORE HITTING EITHER DISPLAYS SEE INSTRUCTIONS ABOVE

BEFORE HITTING EITHER DISPLAYS SEE INSTRUCTIONS ABOVE

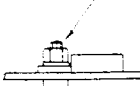
BEFORE HITTING EITHER DISPLAYS SEE INSTRUCTIONS ABOVE

TEST POINT TERMINAL 602007 2mm

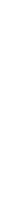
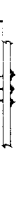
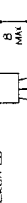
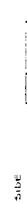
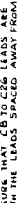
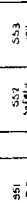
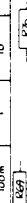
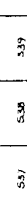
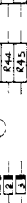
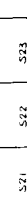
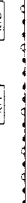
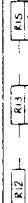
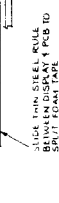
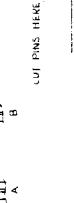
APPLY CLEANING FLUID BEFORE FINISHING TO PCB

M2, M3, M4, M5 MAY FIT PCB PINS 618026 TO UNDERSIDE OF PCB. ENSURE THAT BODY IS FLAT & SQUARE TO PCB WITH MOUNTED PIPS POINTING TOWARDS LOWER EDGE OF PCB

SREW M2.5x4mm SHOTDRILL PIPING 611076
WASHER M3 SHANK PROF 618005
NUT M3 HEX FULL 605002



VIEW TO SHOW FILING 611076



ENSURE THAT CB TO C26 LEADS ARE FORMED WITH THE LEADS SPACED AWAY FROM THE PCB.

NOTE: ALL PINS ON SOLDER SIDE OF PCB MUST BE CROPPED TO 2.5mm OR LESS

NOTE: NO COMPONENTS TO STAND HIGHER THAN 25mm (EXCEPT SWITCHES)

GLASS BEAD SOCKETS FITTED TO EACH LEG OF THE FOLLOWING COMPONENTS: C6, C3, C5, C6, 6mm

NOTE: ALL VIA HOLES AND SPARE COMPONENT HOLES MUST BE SOLDERED

LINK SHOWN COILED, NOT FITTED AT FACT STAGE

GREEN LED 5mm ALL OTHERS RED

2mm STANDOFF 6123-4mm 61203 FIT UNDERSTAMP

BUZZER CONTROL

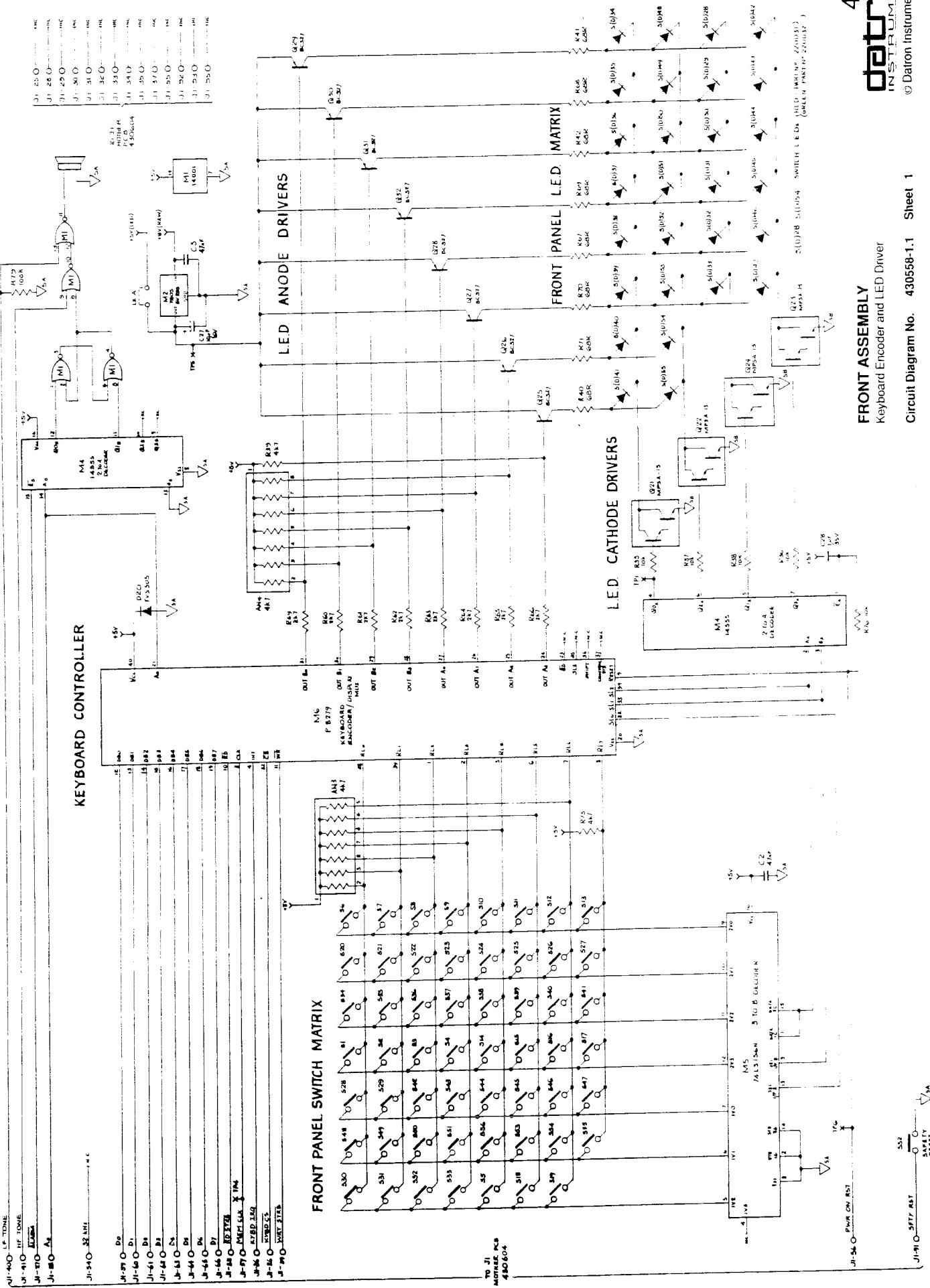
KEYBOARD CONTROLLER

FRONT PANEL SWITCH MATRIX

LED ANODE DRIVERS

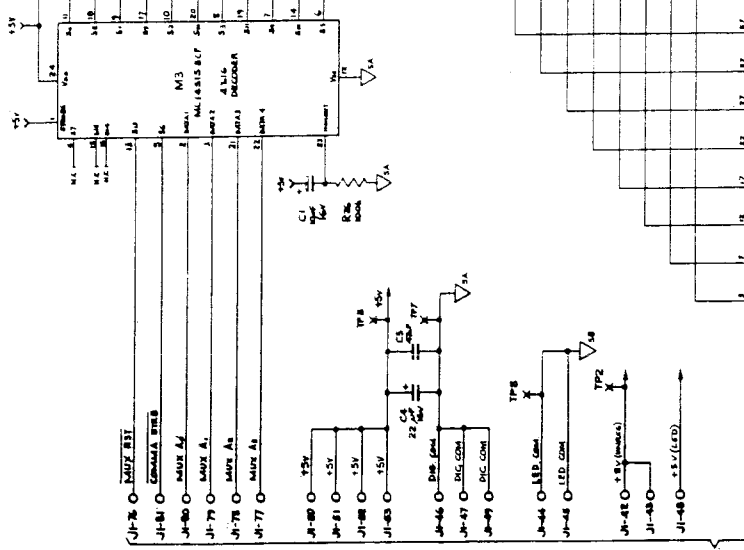
FRONT PANEL LED MATRIX

LED CATHODE DRIVERS

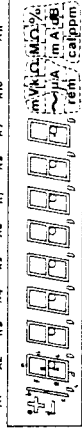


| | | |
|-------|---------|----|
| J1-40 | LF TDME | 1K |
| J1-41 | LF TDME | 1K |
| J1-42 | LF TDME | 1K |
| J1-43 | LF TDME | 1K |
| J1-44 | LF TDME | 1K |
| J1-45 | LF TDME | 1K |
| J1-46 | LF TDME | 1K |
| J1-47 | LF TDME | 1K |
| J1-48 | LF TDME | 1K |
| J1-49 | LF TDME | 1K |
| J1-50 | LF TDME | 1K |
| J1-51 | LF TDME | 1K |
| J1-52 | LF TDME | 1K |
| J1-53 | LF TDME | 1K |
| J1-54 | LF TDME | 1K |
| J1-55 | LF TDME | 1K |
| J1-56 | LF TDME | 1K |
| J1-57 | LF TDME | 1K |
| J1-58 | LF TDME | 1K |
| J1-59 | LF TDME | 1K |
| J1-60 | LF TDME | 1K |

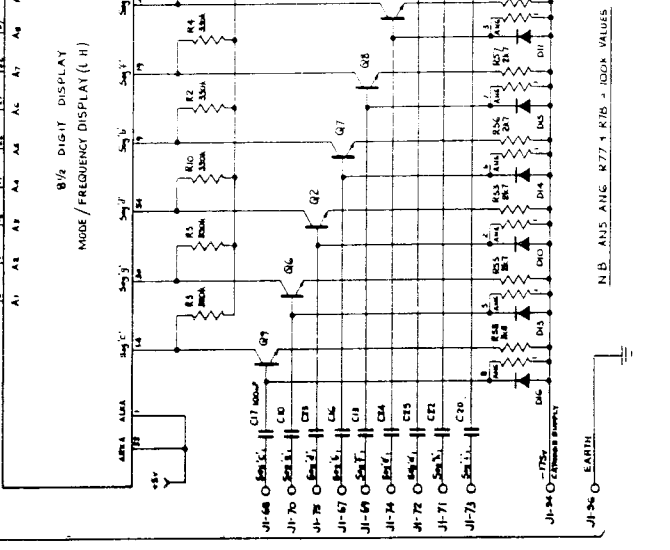
GAS DISCHARGE DISPLAY ANODE DRIVERS



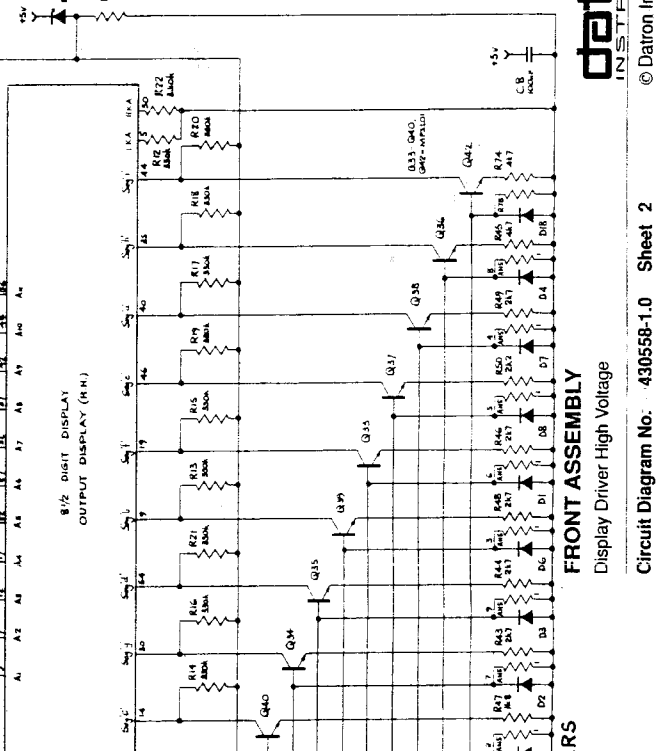
| SEC. | ANODE | A1 | A2 | A3 | A4 | A5 | A6 | A7 | A8 | A9 | A10 |
|------|-------|----|----|----|----|----|----|----|----|----|-----|
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| 3 | 3 | 3 | 3 | 3 | 3 | 3 | 3 | 3 | 3 | 3 | 3 |
| 4 | 4 | 4 | 4 | 4 | 4 | 4 | 4 | 4 | 4 | 4 | 4 |
| 5 | 5 | 5 | 5 | 5 | 5 | 5 | 5 | 5 | 5 | 5 | 5 |
| 6 | 6 | 6 | 6 | 6 | 6 | 6 | 6 | 6 | 6 | 6 | 6 |
| 7 | 7 | 7 | 7 | 7 | 7 | 7 | 7 | 7 | 7 | 7 | 7 |
| 8 | 8 | 8 | 8 | 8 | 8 | 8 | 8 | 8 | 8 | 8 | 8 |
| 9 | 9 | 9 | 9 | 9 | 9 | 9 | 9 | 9 | 9 | 9 | 9 |
| 10 | 10 | 10 | 10 | 10 | 10 | 10 | 10 | 10 | 10 | 10 | 10 |



GAS DISCHARGE DISPLAY CATHODE DRIVERS



FRONT ASSEMBLY
 Display Driver High Voltage



N.B. ANS ANG R77.1 R75 + BOOK VALUES

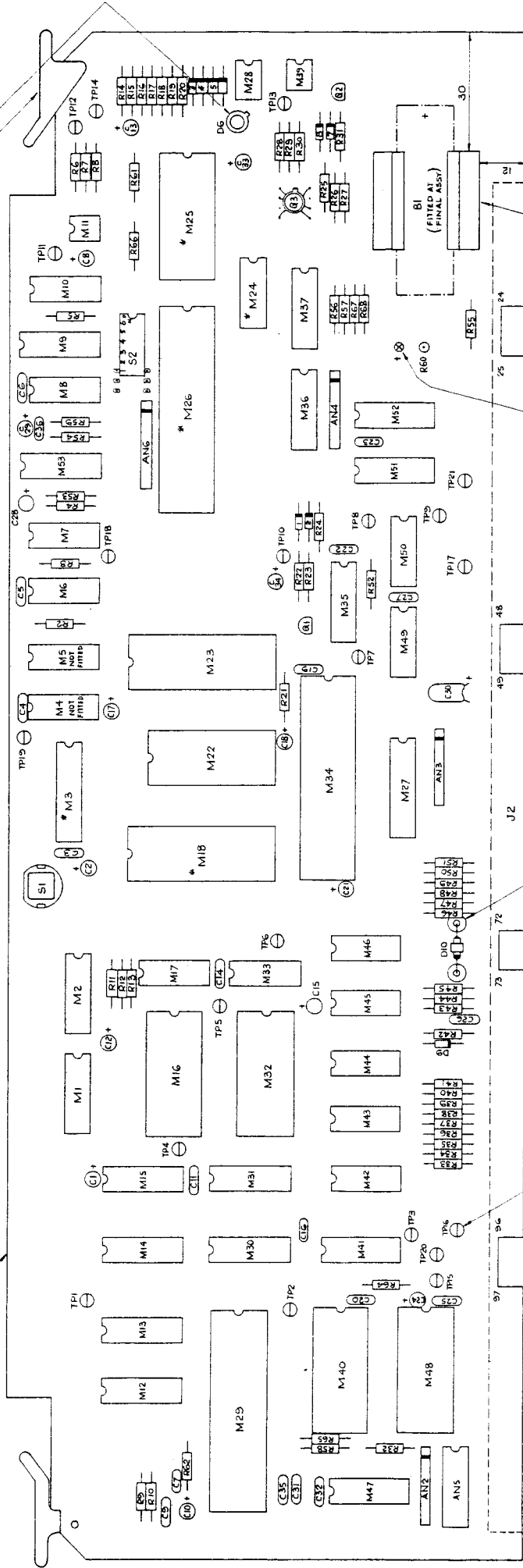
J1-96 O EARTH

DIGITAL ASSEMBLY

MOUNT DG OVER T018 TRANSISTOR MOUNTING PAD 61800 BEFORE SOLDERING INTO PCB.

CIRCUIT BOARD EJECTOR (BLACK) 630112 2.0"

PCB 410248-4



TEST POINT TERMINAL 620007 21 01T

16-DWG-DIELECTRIC BEAD 630024 2.0"

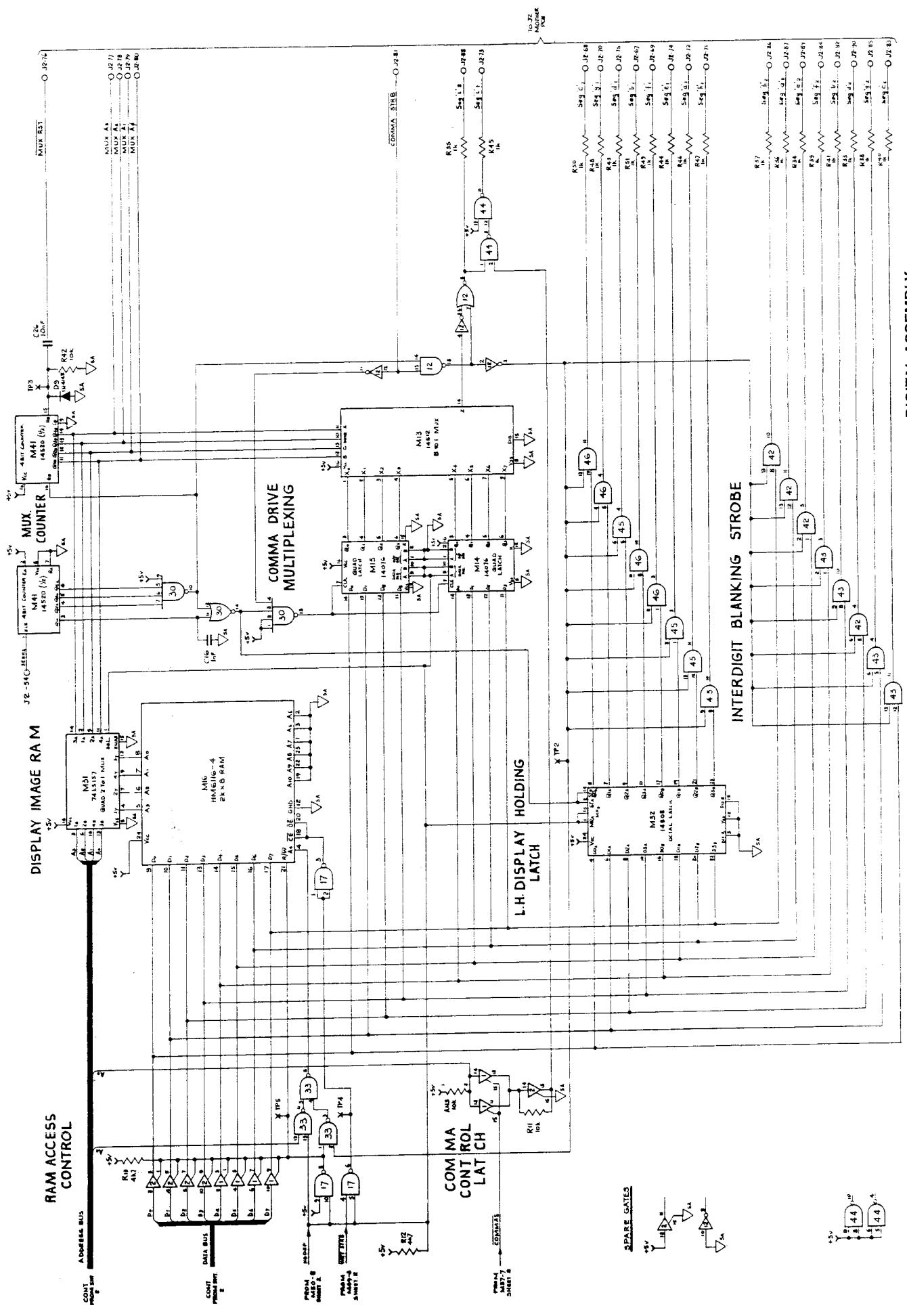
SOLDER TERMINAL 620003

BATTERY CLIP 630098

* NOTE: M3, M8, 24, 25, 42, 46 ARE NOT FITTED AT THIS ASSY STAGE.

THE FOLLOWING COMPONENTS TO HAVE ONE GLASS BEAD 630243 ON EACH LEG: 28 P1, C3-C6, C9, C11, C14, C15, C20, C22, C23, C25, C27 & C32.

| MOUNTING IC's | | |
|---------------|----------|---|
| No OF MNS | PART No. | No. OF USED POSITIONS |
| 6 | 605066 | 2 M11, M13 |
| 8 | 605059 | 1 M28 |
| 14 | 605060 | 14 M6-M8, M10, M17, M24, M33, M42, M46, M49, M50 |
| 16 | 605061 | 16 M16, M19, M12, M15, M30, M31, M35, M37, M41, M47, M51, M53 |
| 20 | 605070 | 2 M3, M27 |
| 24 | 605064 | 6 M16, M22, M25, M32, M40, M48 |
| 28 | 605065 | 2 M18, M23 |
| 40 | 605050 | 3 M26, M25, M34 |



DIGITAL ASSEMBLY
Display Multiplexing Logic

DIGITAL ASSEMBLY

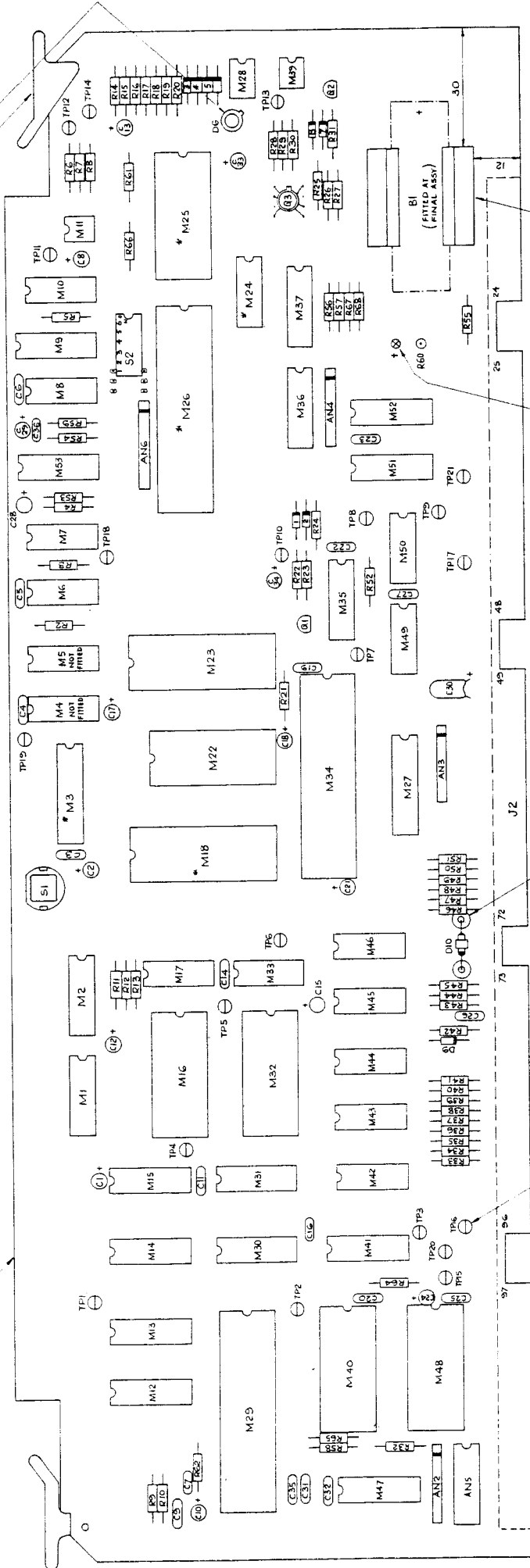
Datron
INSTRUMENTS

4708

MAXIMUM OVER TOP TRANSISTOR
MOUNTING PAD, 0.0004" BEFORE
SOLDERING INTO PCB.

CIRCUIT BOARD EJECTOR (BLACK)
620112 2.6H

PCB 410248-4



BATTERY CLIP 630098
SOLDER TERMINAL 620003

* NOTE: M13, M18, 24, 25 + 26 ARE NOT FITTED
AT THIS ASSY STAGE.

16 SWG STEEL BEAD
630024 2.6H

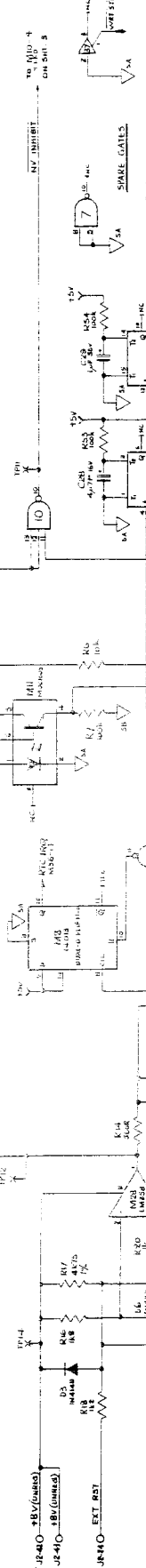
TEST POINT TERMINAL
620007 21.9H

THE FOLLOWING COMPONENTS TO HAVE ONE
GLASS BEAD 630243 ON EACH LIES 28 OH.
M1, M14, C15, C20, C21, C22, C23, C24, C25, C26, C27, C28.

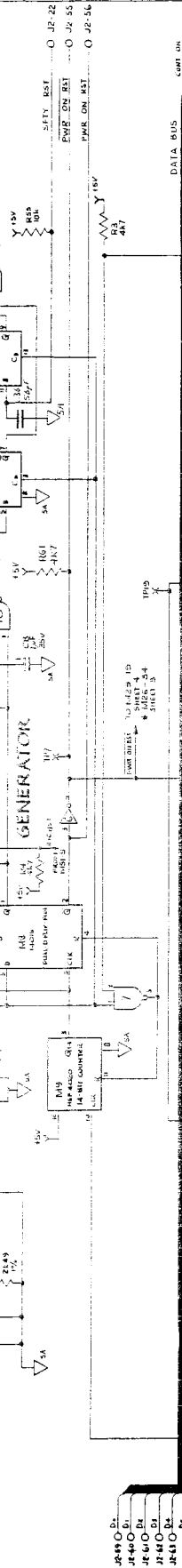
| MOUNTING I.C.'s | |
|-----------------|----------|
| NO OF WAFS | PART No. |
| 6 | 605066 |
| 8 | 605059 |
| 14 | 605060 |
| 16 | 605061 |
| 20 | 605070 |
| 24 | 605064 |
| 28 | 605065 |
| 40 | 605050 |

| NO OF WAFS | USED POSITIONS |
|------------|--|
| 2 | M11, M39 |
| 1 | M28 |
| 14 | M6-M8, M10, M17, M24, M33, M42-M46, M49, M50 |
| 17 | M1, M2, M5, M12, M15, M30, M31, M35, M37, M41, M47, M48, M51-M53 |
| 2 | M3, M27 |
| 6 | M16, M22, M25, M32, M40, M48 |
| 2 | M18, M23 |
| 3 | M26, M29, M34 |

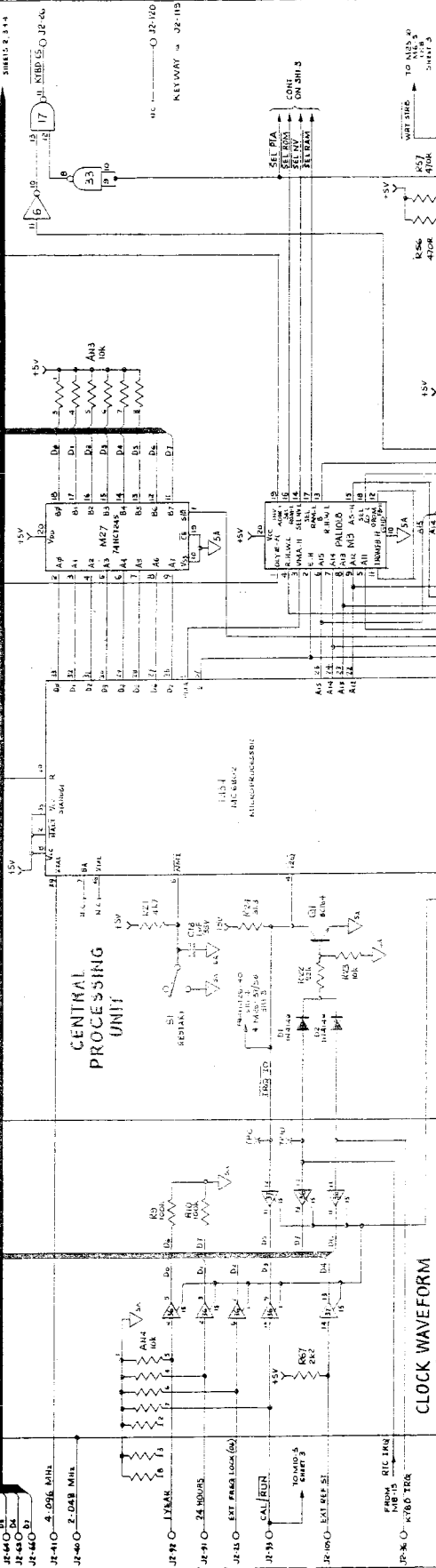
SUPPLY FAIL DETECTOR



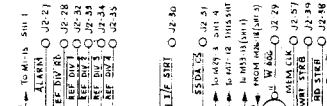
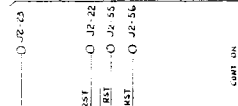
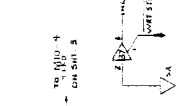
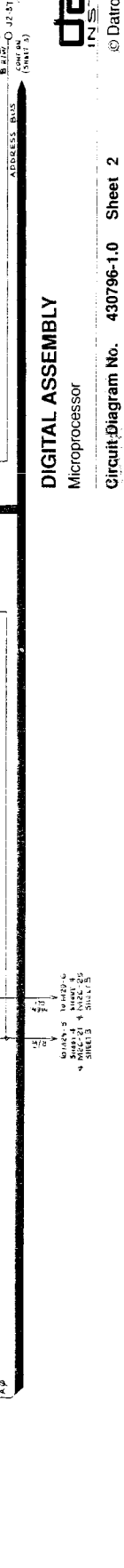
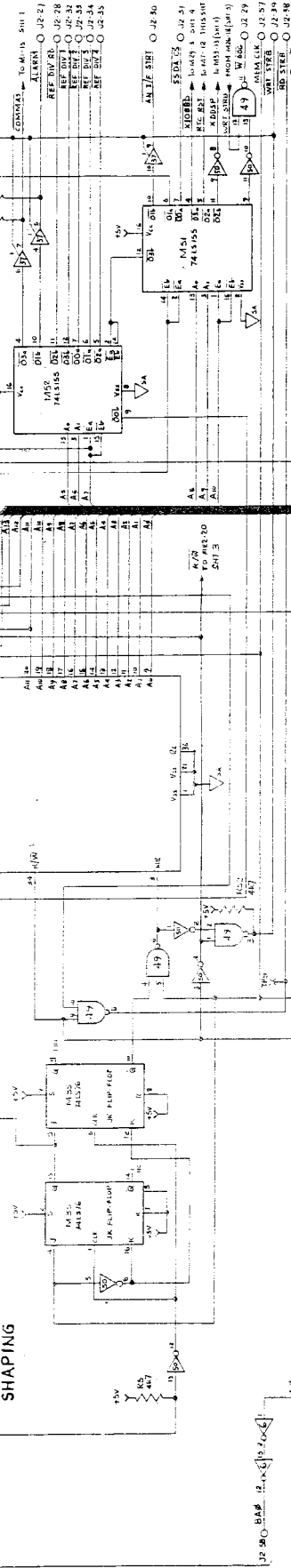
RESTART GENERATOR



CENTRAL PROCESSING UNIT



CLOCK WAVEFORM SHAPING



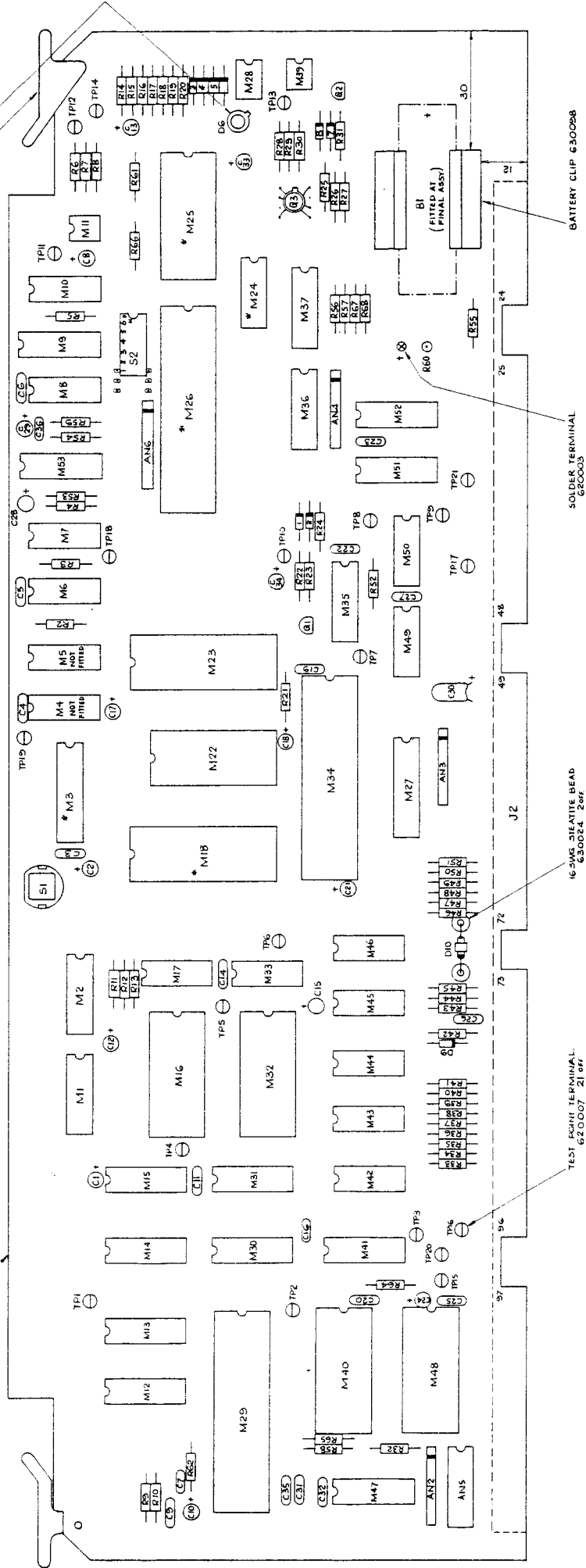
J1-40 18V (MIN/MS) J1-41 18V (MIN/MS) J1-42 EXT. RST J1-43 EXT. RST J1-44 EXT. RST J1-45 EXT. RST J1-46 EXT. RST J1-47 EXT. RST J1-48 EXT. RST J1-49 EXT. RST J1-50 EXT. RST J1-51 EXT. RST J1-52 EXT. RST J1-53 EXT. RST J1-54 EXT. RST J1-55 EXT. RST J1-56 EXT. RST J1-57 EXT. RST J1-58 EXT. RST J1-59 EXT. RST J1-60 EXT. RST J1-61 EXT. RST J1-62 EXT. RST J1-63 EXT. RST J1-64 EXT. RST J1-65 EXT. RST J1-66 EXT. RST J1-67 EXT. RST J1-68 EXT. RST J1-69 EXT. RST J1-70 EXT. RST J1-71 EXT. RST J1-72 EXT. RST J1-73 EXT. RST J1-74 EXT. RST J1-75 EXT. RST J1-76 EXT. RST J1-77 EXT. RST J1-78 EXT. RST J1-79 EXT. RST J1-80 EXT. RST J1-81 EXT. RST J1-82 EXT. RST J1-83 EXT. RST J1-84 EXT. RST J1-85 EXT. RST J1-86 EXT. RST J1-87 EXT. RST J1-88 EXT. RST J1-89 EXT. RST J1-90 EXT. RST J1-91 EXT. RST J1-92 EXT. RST J1-93 EXT. RST J1-94 EXT. RST J1-95 EXT. RST J1-96 EXT. RST J1-97 EXT. RST J1-98 EXT. RST J1-99 EXT. RST J1-100 EXT. RST

DIGITAL ASSEMBLY

MOUNT D6 OVER TOP TRANSISTOR MOUNTING PAD 618004 BEFORE SOLDERING INTO PCB.

CIRCUIT BOARD EJECTOR (BLACK) 650112 2.0F.

PLB 410248-4



GATTERY CLIP 630028

SOLDER TERMINAL 620005

16-PINS CREATIVE BEAD 630024 2.0F.

TEST POINT TERMINAL 620007 21.0F.

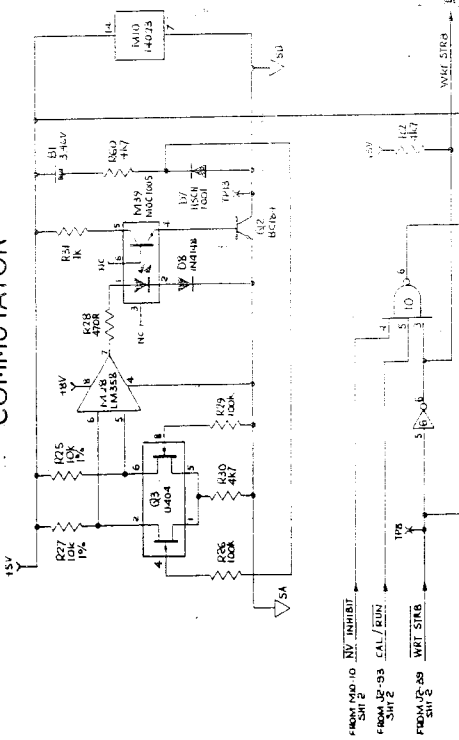
* NOTE: M3, 1B, 24, 25, 26 ARE NOT FITTED AT THIS ASSY STAGE.

THE FOLLOWING COMPONENTS TO HAVE ONE GLASS BEAD 630024 ON EACH LEG: 2B, 0F, C14, C15, C20, C21, C23, C24, C25, C27, & C32.

| MOUNTING IC'S | |
|---------------|-----------|
| No of WMS | PART No |
| 6 | 605066 2 |
| 8 | 605059 1 |
| 14 | 605060 14 |
| 16 | 605061 17 |
| 20 | 605070 2 |
| 24 | 605064 6 |
| 28 | 605065 2 |
| 40 | 605050 3 |

| USED POSITIONS | |
|--|----------------|
| IC No | USED POSITIONS |
| M11 | M39 |
| M28 | |
| M6-M8, M10, M17, M24, M33, M42-M46, M49, M50 | |
| M1, M2, M5, M12, M15, M30, M31, M35-M37, M41, M47, M51-M53 | |
| M3, M27 | |
| M16, M22, M25, M32, M40, M48 | |
| M18, M23 | |
| M26, M29, M34 | |

NON VOLATILE RAM SUPPLY COMMUTATOR



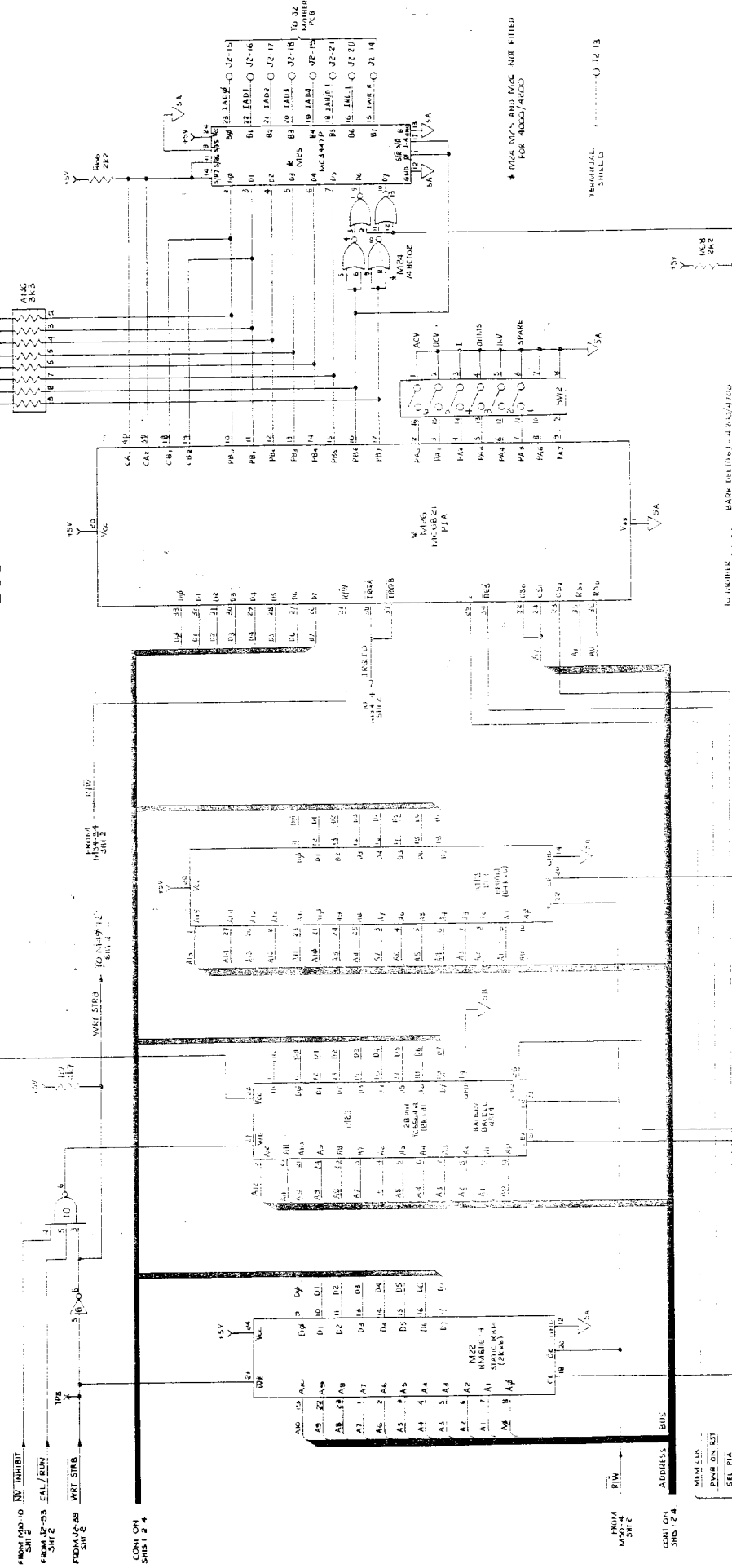
FROM MIO-10
SHEETS 1 & 2

FROM MIO-95
CAL/EUN
SHEET 2

FROM MIO-89
WPT STRS
SHEET 2

CONN ON
SHEETS 1 & 2

DIGITAL BUS



TO MIO-10
SHEETS 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 47, 48, 49, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 67, 68, 69, 70, 71, 72, 73, 74, 75, 76, 77, 78, 79, 80, 81, 82, 83, 84, 85, 86, 87, 88, 89, 90, 91, 92, 93, 94, 95, 96, 97, 98, 99, 100

DIGITAL ASSEMBLY

Display Memory and Battery Backup

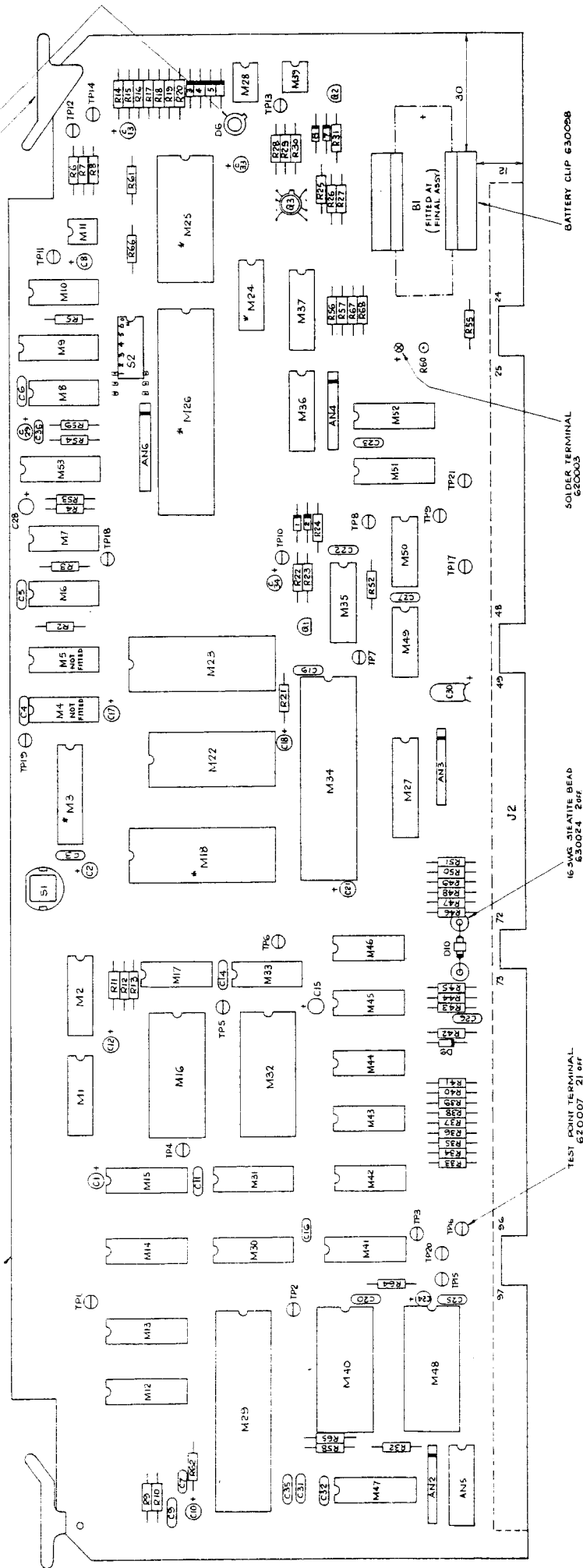
Circuit Diagram No. 430796-1.0 Sheet 3

DIGITAL ASSEMBLY

Mount on over this transistor
M10 M11 M12 M13 M14 M15 M16 M17 M18 M19 M20 M21 M22 M23 M24 M25 M26 M27 M28 M29 M30 M31 M32 M33 M34 M35 M36 M37 M38 M39 M40 M41 M42 M43 M44 M45 M46 M47 M48 M49 M50 M51 M52 M53 M54 M55 M56 M57 M58 M59 M60 M61 M62 M63 M64 M65 M66 M67 M68 M69 M70 M71 M72 M73 M74 M75 M76 M77 M78 M79 M80 M81 M82 M83 M84 M85 M86 M87 M88 M89 M90 M91 M92 M93 M94 M95 M96 M97 M98 M99 M100 M101 M102 M103 M104 M105 M106 M107 M108 M109 M110 M111 M112 M113 M114 M115 M116 M117 M118 M119 M120 M121 M122 M123 M124 M125 M126 M127 M128 M129 M130 M131 M132 M133 M134 M135 M136 M137 M138 M139 M140 M141 M142 M143 M144 M145 M146 M147 M148 M149 M150 M151 M152 M153 M154 M155 M156 M157 M158 M159 M160 M161 M162 M163 M164 M165 M166 M167 M168 M169 M170 M171 M172 M173 M174 M175 M176 M177 M178 M179 M180 M181 M182 M183 M184 M185 M186 M187 M188 M189 M190 M191 M192 M193 M194 M195 M196 M197 M198 M199 M200 M201 M202 M203 M204 M205 M206 M207 M208 M209 M210 M211 M212 M213 M214 M215 M216 M217 M218 M219 M220 M221 M222 M223 M224 M225 M226 M227 M228 M229 M230 M231 M232 M233 M234 M235 M236 M237 M238 M239 M240 M241 M242 M243 M244 M245 M246 M247 M248 M249 M250 M251 M252 M253 M254 M255 M256 M257 M258 M259 M260 M261 M262 M263 M264 M265 M266 M267 M268 M269 M270 M271 M272 M273 M274 M275 M276 M277 M278 M279 M280 M281 M282 M283 M284 M285 M286 M287 M288 M289 M290 M291 M292 M293 M294 M295 M296 M297 M298 M299 M300 M301 M302 M303 M304 M305 M306 M307 M308 M309 M310 M311 M312 M313 M314 M315 M316 M317 M318 M319 M320 M321 M322 M323 M324 M325 M326 M327 M328 M329 M330 M331 M332 M333 M334 M335 M336 M337 M338 M339 M340 M341 M342 M343 M344 M345 M346 M347 M348 M349 M350 M351 M352 M353 M354 M355 M356 M357 M358 M359 M360 M361 M362 M363 M364 M365 M366 M367 M368 M369 M370 M371 M372 M373 M374 M375 M376 M377 M378 M379 M380 M381 M382 M383 M384 M385 M386 M387 M388 M389 M390 M391 M392 M393 M394 M395 M396 M397 M398 M399 M400 M401 M402 M403 M404 M405 M406 M407 M408 M409 M410 M411 M412 M413 M414 M415 M416 M417 M418 M419 M420 M421 M422 M423 M424 M425 M426 M427 M428 M429 M430 M431 M432 M433 M434 M435 M436 M437 M438 M439 M440 M441 M442 M443 M444 M445 M446 M447 M448 M449 M450 M451 M452 M453 M454 M455 M456 M457 M458 M459 M460 M461 M462 M463 M464 M465 M466 M467 M468 M469 M470 M471 M472 M473 M474 M475 M476 M477 M478 M479 M480 M481 M482 M483 M484 M485 M486 M487 M488 M489 M490 M491 M492 M493 M494 M495 M496 M497 M498 M499 M500 M501 M502 M503 M504 M505 M506 M507 M508 M509 M510 M511 M512 M513 M514 M515 M516 M517 M518 M519 M520 M521 M522 M523 M524 M525 M526 M527 M528 M529 M530 M531 M532 M533 M534 M535 M536 M537 M538 M539 M540 M541 M542 M543 M544 M545 M546 M547 M548 M549 M550 M551 M552 M553 M554 M555 M556 M557 M558 M559 M560 M561 M562 M563 M564 M565 M566 M567 M568 M569 M570 M571 M572 M573 M574 M575 M576 M577 M578 M579 M580 M581 M582 M583 M584 M585 M586 M587 M588 M589 M590 M591 M592 M593 M594 M595 M596 M597 M598 M599 M600 M601 M602 M603 M604 M605 M606 M607 M608 M609 M610 M611 M612 M613 M614 M615 M616 M617 M618 M619 M620 M621 M622 M623 M624 M625 M626 M627 M628 M629 M630 M631 M632 M633 M634 M635 M636 M637 M638 M639 M640 M641 M642 M643 M644 M645 M646 M647 M648 M649 M650 M651 M652 M653 M654 M655 M656 M657 M658 M659 M660 M661 M662 M663 M664 M665 M666 M667 M668 M669 M670 M671 M672 M673 M674 M675 M676 M677 M678 M679 M680 M681 M682 M683 M684 M685 M686 M687 M688 M689 M690 M691 M692 M693 M694 M695 M696 M697 M698 M699 M700 M701 M702 M703 M704 M705 M706 M707 M708 M709 M710 M711 M712 M713 M714 M715 M716 M717 M718 M719 M720 M721 M722 M723 M724 M725 M726 M727 M728 M729 M730 M731 M732 M733 M734 M735 M736 M737 M738 M739 M740 M741 M742 M743 M744 M745 M746 M747 M748 M749 M750 M751 M752 M753 M754 M755 M756 M757 M758 M759 M760 M761 M762 M763 M764 M765 M766 M767 M768 M769 M770 M771 M772 M773 M774 M775 M776 M777 M778 M779 M780 M781 M782 M783 M784 M785 M786 M787 M788 M789 M790 M791 M792 M793 M794 M795 M796 M797 M798 M799 M800 M801 M802 M803 M804 M805 M806 M807 M808 M809 M810 M811 M812 M813 M814 M815 M816 M817 M818 M819 M820 M821 M822 M823 M824 M825 M826 M827 M828 M829 M830 M831 M832 M833 M834 M835 M836 M837 M838 M839 M840 M841 M842 M843 M844 M845 M846 M847 M848 M849 M850 M851 M852 M853 M854 M855 M856 M857 M858 M859 M860 M861 M862 M863 M864 M865 M866 M867 M868 M869 M870 M871 M872 M873 M874 M875 M876 M877 M878 M879 M880 M881 M882 M883 M884 M885 M886 M887 M888 M889 M890 M891 M892 M893 M894 M895 M896 M897 M898 M899 M900 M901 M902 M903 M904 M905 M906 M907 M908 M909 M910 M911 M912 M913 M914 M915 M916 M917 M918 M919 M920 M921 M922 M923 M924 M925 M926 M927 M928 M929 M930 M931 M932 M933 M934 M935 M936 M937 M938 M939 M940 M941 M942 M943 M944 M945 M946 M947 M948 M949 M950 M951 M952 M953 M954 M955 M956 M957 M958 M959 M960 M961 M962 M963 M964 M965 M966 M967 M968 M969 M970 M971 M972 M973 M974 M975 M976 M977 M978 M979 M980 M981 M982 M983 M984 M985 M986 M987 M988 M989 M990 M991 M992 M993 M994 M995 M996 M997 M998 M999 M1000

CIRCUIT BOARD EJECTOR (BLACK)
650112 2 or

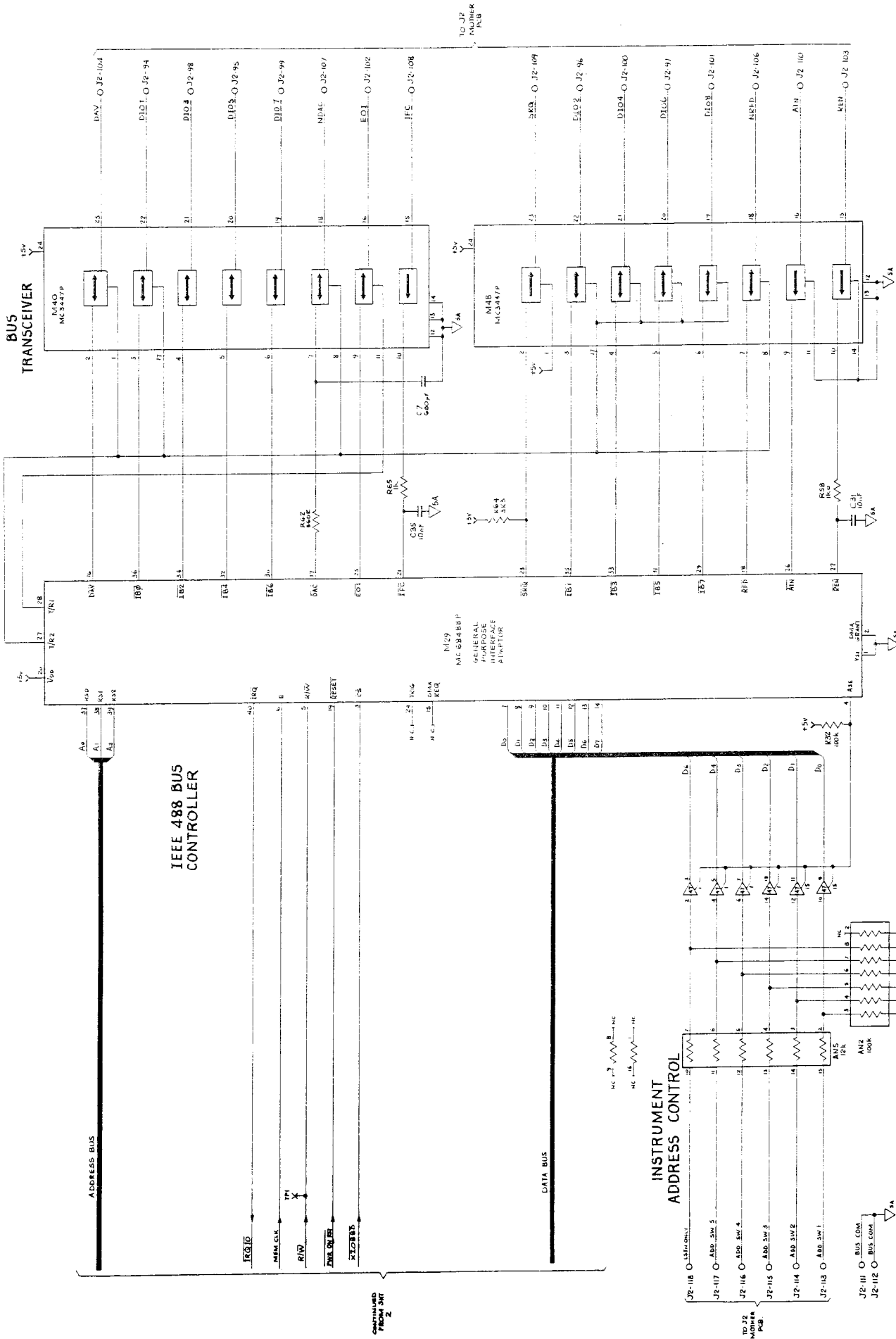
PCB 410245-4



* NOTE: M3, M5, M24, M25, & M26 ARE NOT FITTED AT THIS ASSY STAGE

THE FOLLOWING COMPONENTS TO HAVE ONE GLASS BEAD 630243 ON EACH LEG: M3, M5, M24, M25, M26, M27, M28, M29, M30, M31, M32, M33, M34, M35, M36, M37, M38, M39, M40, M41, M42, M43, M44, M45, M46, M47, M48, M49, M50, M51, M52, M53, M54, M55, M56, M57, M58, M59, M60

| MOUNTING I.C.'s | | |
|-----------------|---------|---|
| No of WMS | Part No | USED POSITIONS |
| 6 | 605064 | M11, M39 |
| 8 | 605059 | M28 |
| 14 | 605060 | M6, M8, M10, M17, M24, M33, M42, M46, M49, M50 |
| 16 | 605061 | M1, M2, M4, M7, M15, M30, M31, M35, M37, M41, M47, M51, M53 |
| 20 | 605070 | M3, M27 |
| 24 | 605064 | M16, M22, M25, M32, M40, M48 |
| 28 | 605065 | M18, M23 |
| 40 | 605050 | M26, M29, M34 |



BUS TRANSCEIVER

IEEE 488 BUS CONTROLLER

INSTRUMENT ADDRESS CONTROL

CONTINUED FROM SHEET 2

DIGITAL ASSEMBLY
IEEE 488 Interface

Circuit Diagram No. 430796-1.0 Sheet 4

DIGITAL ASSEMBLY

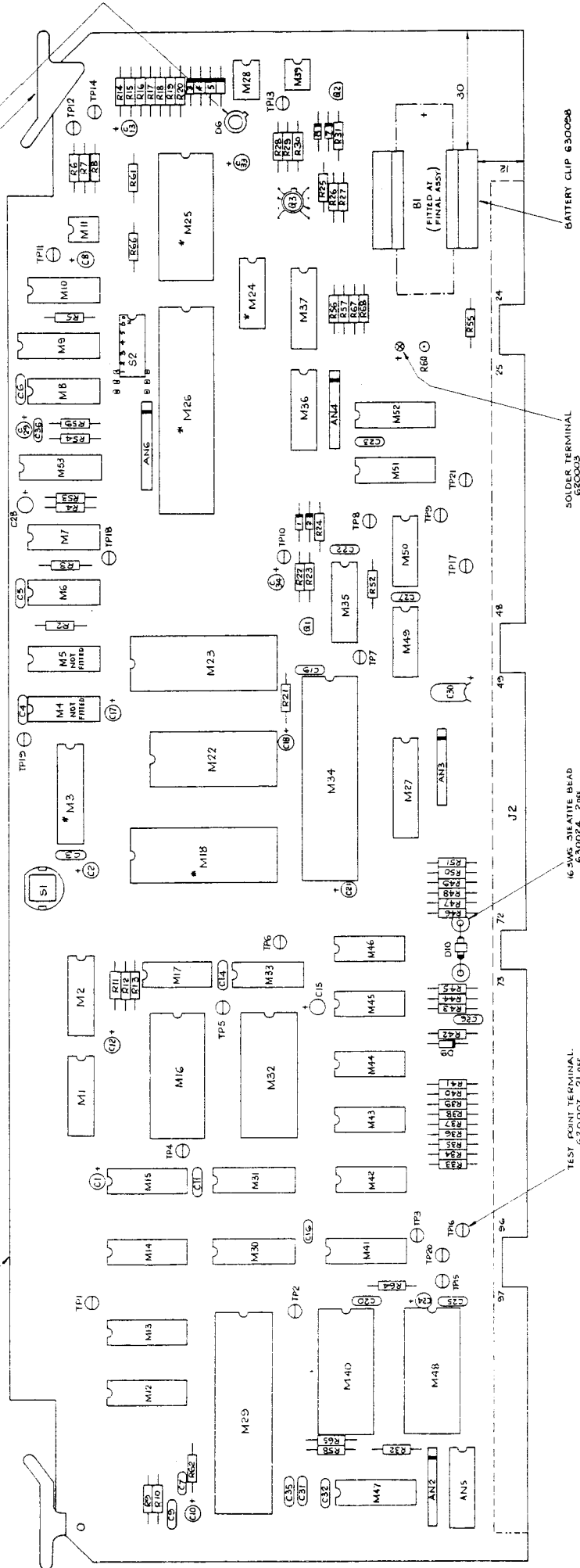
Datron
INSTRUMENTS

4708

Mount DC OVER TOLE TRANSISTOR
MOUNTING TABS BODY BEFORE
SOLDERING INTO PCB.

CIRCUIT BOARD EJECTOR (BLACK)
630112 2.0H

PCB 410248-4



* NOTE
M3, IB, 24, 25 + 26 ARE NOT FITTED
AT THIS ASSY STAGE

THE FOLLOWING COMPONENTS TO HAVE ONLY
GLASS BEAD 630243 ON EACH LEG 28 OH.
C3, C6, C9, C11, C14, C15, C20, C22, C23,
C25, C27 + C32.

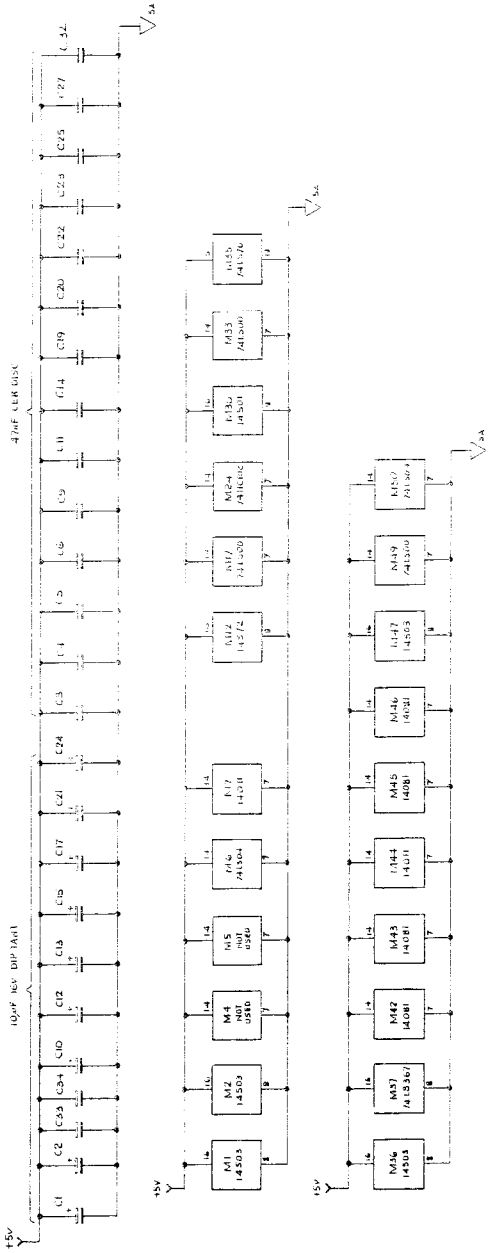
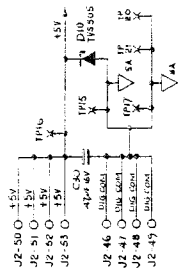
| MOUNTING IC's | | USED POSITIONS | |
|---------------|---------|----------------|---|
| No OF WAYS | FART No | No OF | USED POSITIONS |
| 6 | 605066 | 2 | M11, M39 |
| 8 | 605059 | 1 | M28 |
| 14 | 605060 | 14 | M6-M8, M10, M17, M24, M33, M42-M46, M49, M50 |
| 16 | 605061 | 17 | M1, M2, M5, M16-M18, M30, M31, M35-M37, M41, M47, M51-M53 |
| 20 | 605070 | 2 | M3, M27 |
| 24 | 605064 | 6 | M16, M22, M25, M32, M40, M48 |
| 28 | 605063 | 2 | M18, M23 |
| 40 | 605050 | 3 | M26, M29, M34 |

TEST POINT TERMINAL.
620007 21.0H

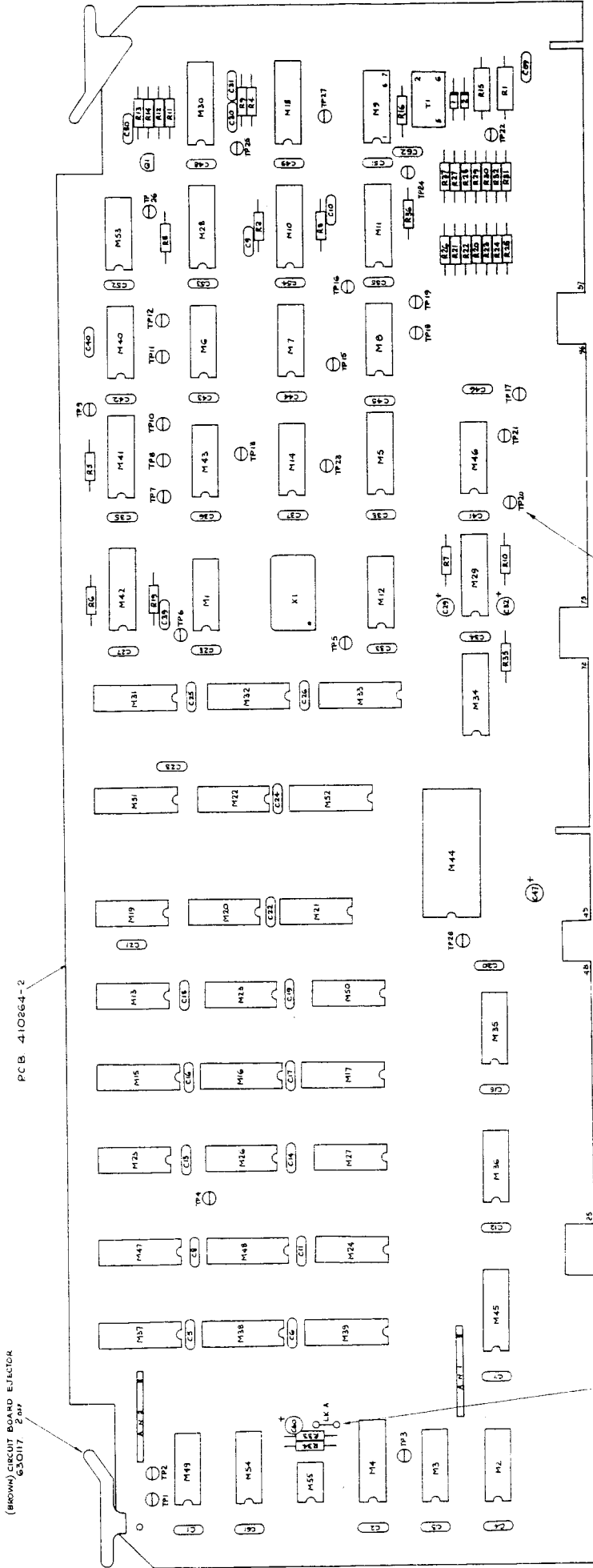
16-2WG DIAMITE BEAD
630054 2.0H

SOLDER TERMINAL
620003

BATTERY CLIP 630068



ANALOG INTERFACE ASSEMBLY



MAKE LINK FROM 22 SWG BTC WIRE
540002 LINK TO FORM LOW-HIGH
LOOP.

NR GLASS BEAD 630643 FITTED TO EACH LEG
OF THE FOLLOWING COMPONENTS: C1-C9,
C11-C13, C15, C16, C18, C19, C20,
C21-C23, C25, C26, C28, C29, C30

| MT-MMS PART # | USED TO MOUNT | MOUNT |
|---------------|--|-------|
| B 605059 | 55 | 1 |
| 14 605060 | 1, 3, 6, 9, 12, 14, 15, 17, 23, 36, 40, 43, 46, 49, 50, 53, 54 | 28 |
| 16 605061 | 4, 5, 15, 16, 17, 22, 31, 34, 37, 39, 41, 42, 45, 47, 48, 51, 52, 10, 11, 18, 25, 29, 30 | 55 |
| 24 605064 | 44 | 1 |

DATA BUS

15V

15V

15V

15V

15V

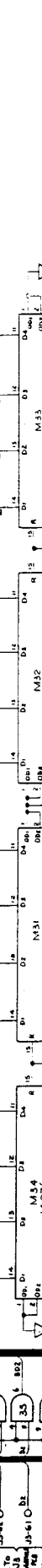
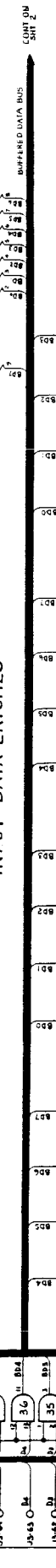
15V

15V

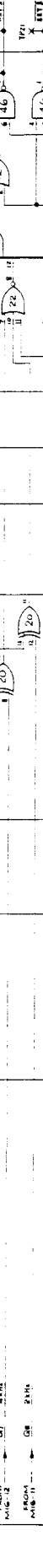
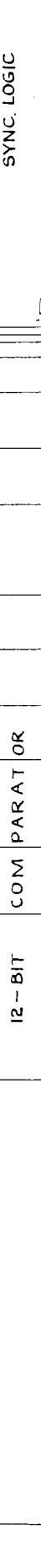
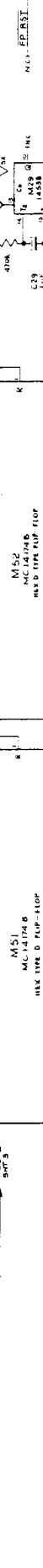
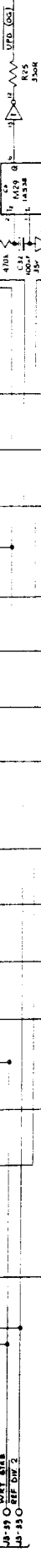
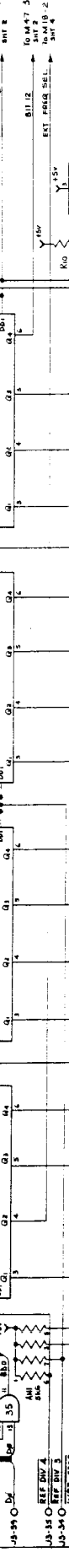
15V



INPUT-DATA LATCHES



12-BIT COMPARATOR



ANALOG INTERFACE ASSEMBLY

Lower Reference Divider Counter

Circuit Diagram No. 430648-1.0 Sheet 1

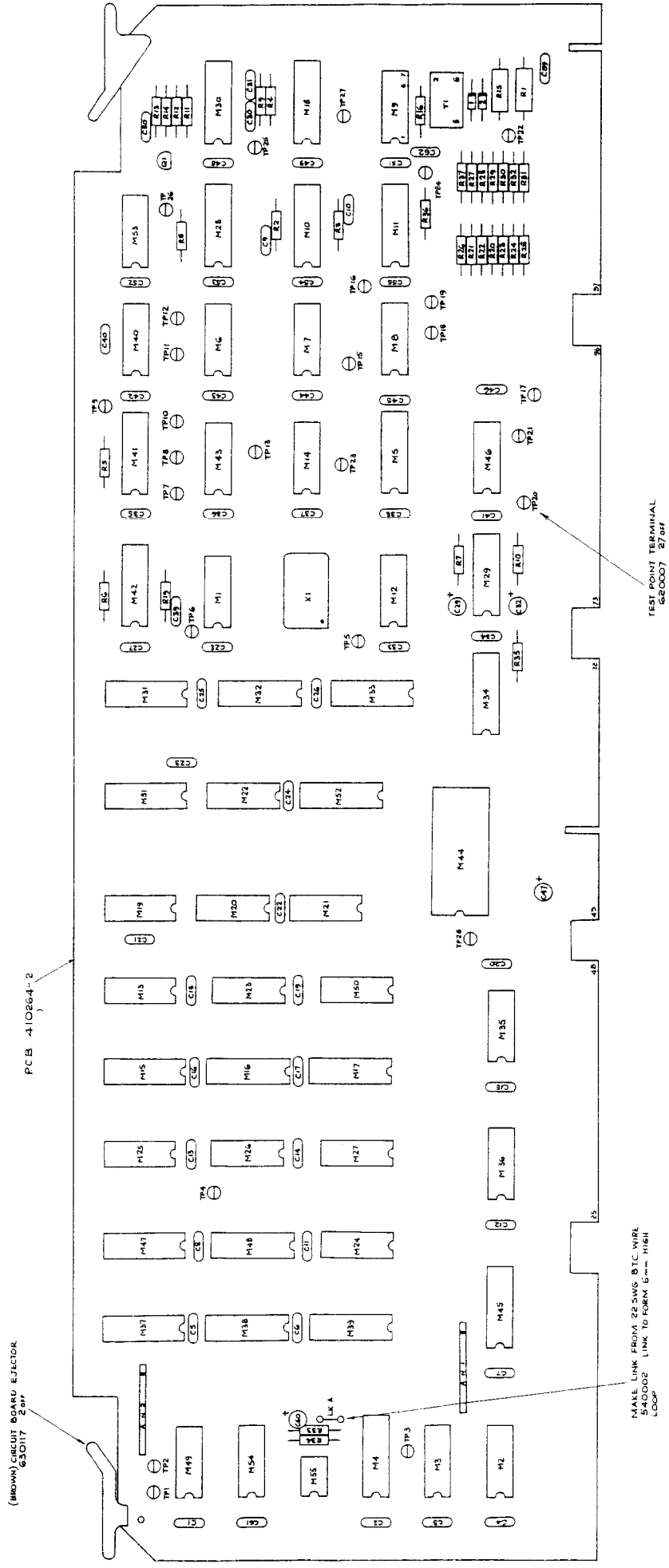
4708

DATRON INSTRUMENTS

© Datron Instruments 1989

11-3-1

ANALOG INTERFACE ASSEMBLY



N.B. GLASS BEAD 650643 FITTED TO EACH LEG OF THE FOLLOWING COMPONENTS: C1, C2, C3, C4, C5, C6, C7, C8, C9, C10, C11, C12, C13, C14, C15, C16, C17, C18, C19, C20, C21, C22, C23, C24, C25, C26, C27, C28, C29, C30, C31, C32, C33, C34, C35, C36, C37, C38, C39, C40, C41, C42, C43, C44, C45, C46, C47, C48, C49, C50, C51, C52, C53, C54, C55, C56, C57, C58, C59, C60, C61, C62, C63, C64, C65, C66, C67, C68, C69, C70, C71, C72, C73, C74, C75, C76, C77, C78, C79, C80, C81, C82, C83, C84, C85, C86, C87, C88, C89, C90, C91, C92, C93, C94, C95, C96, C97, C98, C99, C100, C101, C102, C103, C104, C105, C106, C107, C108, C109, C110, C111, C112, C113, C114, C115, C116, C117, C118, C119, C120, C121, C122, C123, C124, C125, C126, C127, C128, C129, C130, C131, C132, C133, C134, C135, C136, C137, C138, C139, C140, C141, C142, C143, C144, C145, C146, C147, C148, C149, C150, C151, C152, C153, C154, C155, C156, C157, C158, C159, C160, C161, C162, C163, C164, C165, C166, C167, C168, C169, C170, C171, C172, C173, C174, C175, C176, C177, C178, C179, C180, C181, C182, C183, C184, C185, C186, C187, C188, C189, C190, C191, C192, C193, C194, C195, C196, C197, C198, C199, C200, C201, C202, C203, C204, C205, C206, C207, C208, C209, C210, C211, C212, C213, C214, C215, C216, C217, C218, C219, C220, C221, C222, C223, C224, C225, C226, C227, C228, C229, C230, C231, C232, C233, C234, C235, C236, C237, C238, C239, C240, C241, C242, C243, C244, C245, C246, C247, C248, C249, C250, C251, C252, C253, C254, C255, C256, C257, C258, C259, C260, C261, C262, C263, C264, C265, C266, C267, C268, C269, C270, C271, C272, C273, C274, C275, C276, C277, C278, C279, C280, C281, C282, C283, C284, C285, C286, C287, C288, C289, C290, C291, C292, C293, C294, C295, C296, C297, C298, C299, C300, C301, C302, C303, C304, C305, C306, C307, C308, C309, C310, C311, C312, C313, C314, C315, C316, C317, C318, C319, C320, C321, C322, C323, C324, C325, C326, C327, C328, C329, C330, C331, C332, C333, C334, C335, C336, C337, C338, C339, C340, C341, C342, C343, C344, C345, C346, C347, C348, C349, C350, C351, C352, C353, C354, C355, C356, C357, C358, C359, C360, C361, C362, C363, C364, C365, C366, C367, C368, C369, C370, C371, C372, C373, C374, C375, C376, C377, C378, C379, C380, C381, C382, C383, C384, C385, C386, C387, C388, C389, C390, C391, C392, C393, C394, C395, C396, C397, C398, C399, C400, C401, C402, C403, C404, C405, C406, C407, C408, C409, C410, C411, C412, C413, C414, C415, C416, C417, C418, C419, C420, C421, C422, C423, C424, C425, C426, C427, C428, C429, C430, C431, C432, C433, C434, C435, C436, C437, C438, C439, C440, C441, C442, C443, C444, C445, C446, C447, C448, C449, C450, C451, C452, C453, C454, C455, C456, C457, C458, C459, C460, C461, C462, C463, C464, C465, C466, C467, C468, C469, C470, C471, C472, C473, C474, C475, C476, C477, C478, C479, C480, C481, C482, C483, C484, C485, C486, C487, C488, C489, C490, C491, C492, C493, C494, C495, C496, C497, C498, C499, C500, C501, C502, C503, C504, C505, C506, C507, C508, C509, C510, C511, C512, C513, C514, C515, C516, C517, C518, C519, C520, C521, C522, C523, C524, C525, C526, C527, C528, C529, C530, C531, C532, C533, C534, C535, C536, C537, C538, C539, C540, C541, C542, C543, C544, C545, C546, C547, C548, C549, C550, C551, C552, C553, C554, C555, C556, C557, C558, C559, C560, C561, C562, C563, C564, C565, C566, C567, C568, C569, C570, C571, C572, C573, C574, C575, C576, C577, C578, C579, C580, C581, C582, C583, C584, C585, C586, C587, C588, C589, C590, C591, C592, C593, C594, C595, C596, C597, C598, C599, C600, C601, C602, C603, C604, C605, C606, C607, C608, C609, C610, C611, C612, C613, C614, C615, C616, C617, C618, C619, C620, C621, C622, C623, C624, C625, C626, C627, C628, C629, C630, C631, C632, C633, C634, C635, C636, C637, C638, C639, C640, C641, C642, C643, C644, C645, C646, C647, C648, C649, C650, C651, C652, C653, C654, C655, C656, C657, C658, C659, C660, C661, C662, C663, C664, C665, C666, C667, C668, C669, C670, C671, C672, C673, C674, C675, C676, C677, C678, C679, C680, C681, C682, C683, C684, C685, C686, C687, C688, C689, C690, C691, C692, C693, C694, C695, C696, C697, C698, C699, C700, C701, C702, C703, C704, C705, C706, C707, C708, C709, C710, C711, C712, C713, C714, C715, C716, C717, C718, C719, C720, C721, C722, C723, C724, C725, C726, C727, C728, C729, C730, C731, C732, C733, C734, C735, C736, C737, C738, C739, C740, C741, C742, C743, C744, C745, C746, C747, C748, C749, C750, C751, C752, C753, C754, C755, C756, C757, C758, C759, C760, C761, C762, C763, C764, C765, C766, C767, C768, C769, C770, C771, C772, C773, C774, C775, C776, C777, C778, C779, C780, C781, C782, C783, C784, C785, C786, C787, C788, C789, C790, C791, C792, C793, C794, C795, C796, C797, C798, C799, C800, C801, C802, C803, C804, C805, C806, C807, C808, C809, C810, C811, C812, C813, C814, C815, C816, C817, C818, C819, C820, C821, C822, C823, C824, C825, C826, C827, C828, C829, C830, C831, C832, C833, C834, C835, C836, C837, C838, C839, C840, C841, C842, C843, C844, C845, C846, C847, C848, C849, C850, C851, C852, C853, C854, C855, C856, C857, C858, C859, C860, C861, C862, C863, C864, C865, C866, C867, C868, C869, C870, C871, C872, C873, C874, C875, C876, C877, C878, C879, C880, C881, C882, C883, C884, C885, C886, C887, C888, C889, C890, C891, C892, C893, C894, C895, C896, C897, C898, C899, C900, C901, C902, C903, C904, C905, C906, C907, C908, C909, C910, C911, C912, C913, C914, C915, C916, C917, C918, C919, C920, C921, C922, C923, C924, C925, C926, C927, C928, C929, C930, C931, C932, C933, C934, C935, C936, C937, C938, C939, C940, C941, C942, C943, C944, C945, C946, C947, C948, C949, C950, C951, C952, C953, C954, C955, C956, C957, C958, C959, C960, C961, C962, C963, C964, C965, C966, C967, C968, C969, C970, C971, C972, C973, C974, C975, C976, C977, C978, C979, C980, C981, C982, C983, C984, C985, C986, C987, C988, C989, C990, C991, C992, C993, C994, C995, C996, C997, C998, C999, C1000.

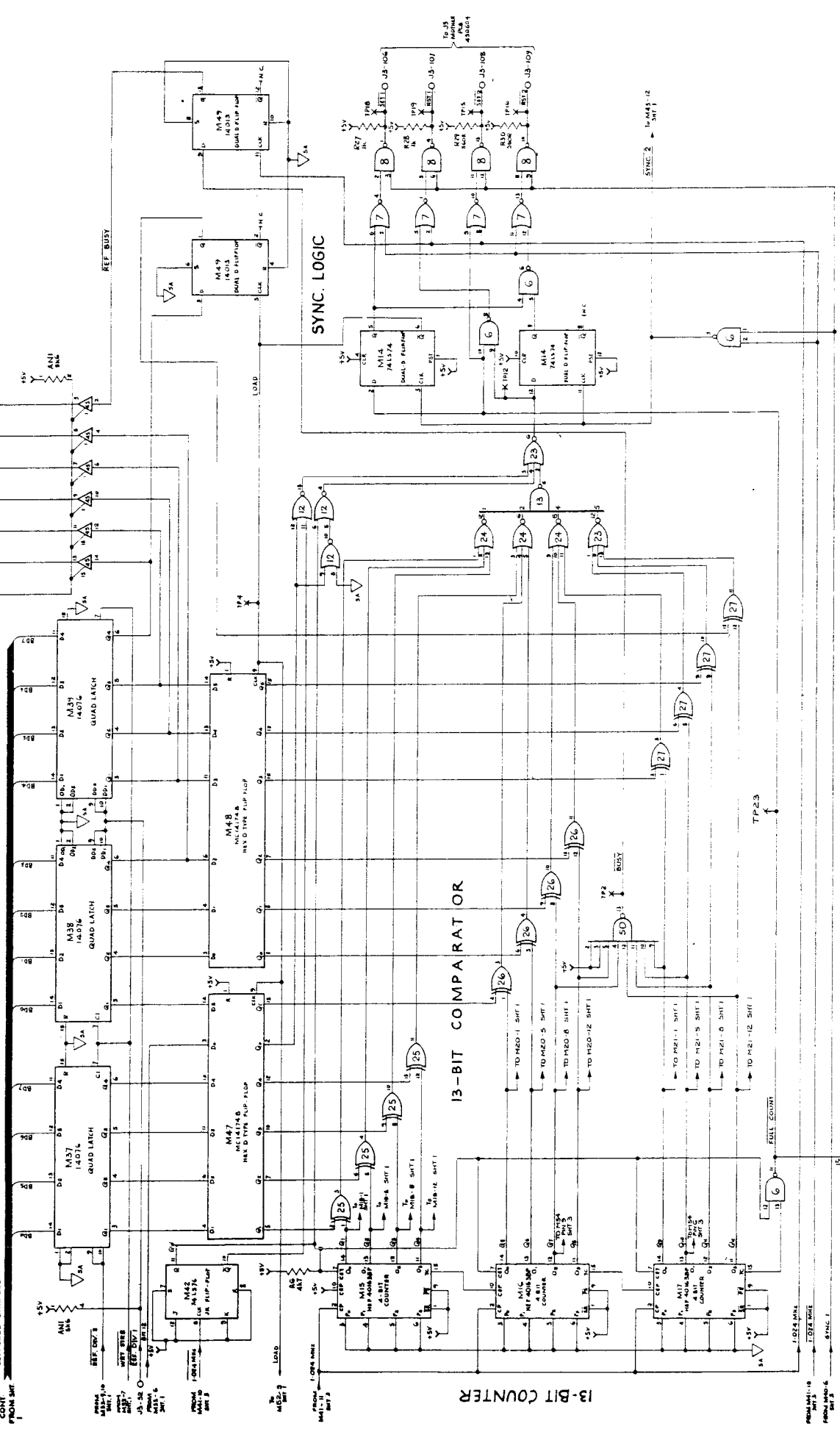
MAKE LINK FROM 22 SWG BTC-WIRE 1/4" LONG. LINK TO FORM 6mm HIGH LOOP

| MOUNTING IC's | |
|-----------------|--|
| N° WAYS PART N° | USED TO MOUNT |
| 8 605039 | 55 |
| 14 605060 | 13, 6, 9, 12, 14, 19, 27, 35, 40, 43, 45, 49, 50, 53, 54 |
| 16 605061 | 2, 3, 10, 16, 17, 23, 31, 34, 37, 39, 41, 42, 45, 47, 48, 51, 52, 10, 11, 18, 25 |
| 24 605064 | 44 |

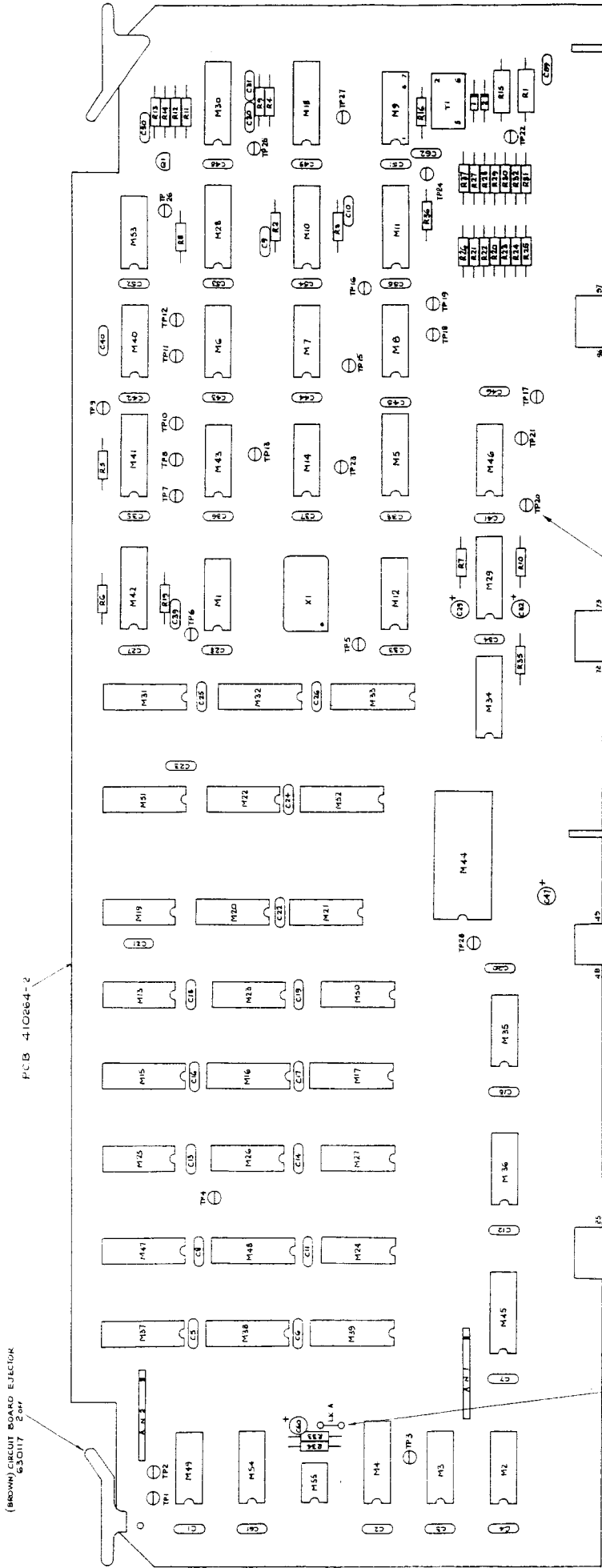
TEST POINT TERMINAL 620007 27 off

DATA BUS
CONT. FROM SHEET 1
CONT. TO SHEET 3

INPUT DATA LATCHES



ANALOG INTERFACE ASSEMBLY



PCB 410264-2

(BROWN) CIRCUIT BOARD EJECTION
630117 2.00

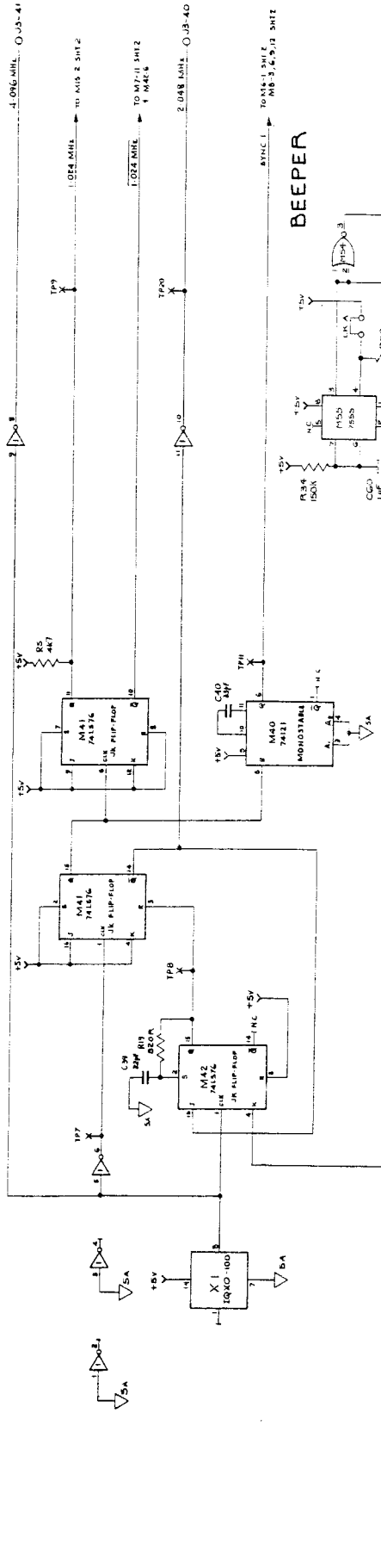
MAKE LINK FROM 22 SWG BIL WIRE
540002 LINK TO FORM HIGH
LOOP

TEST POINT TERMINAL
G20007 27.00

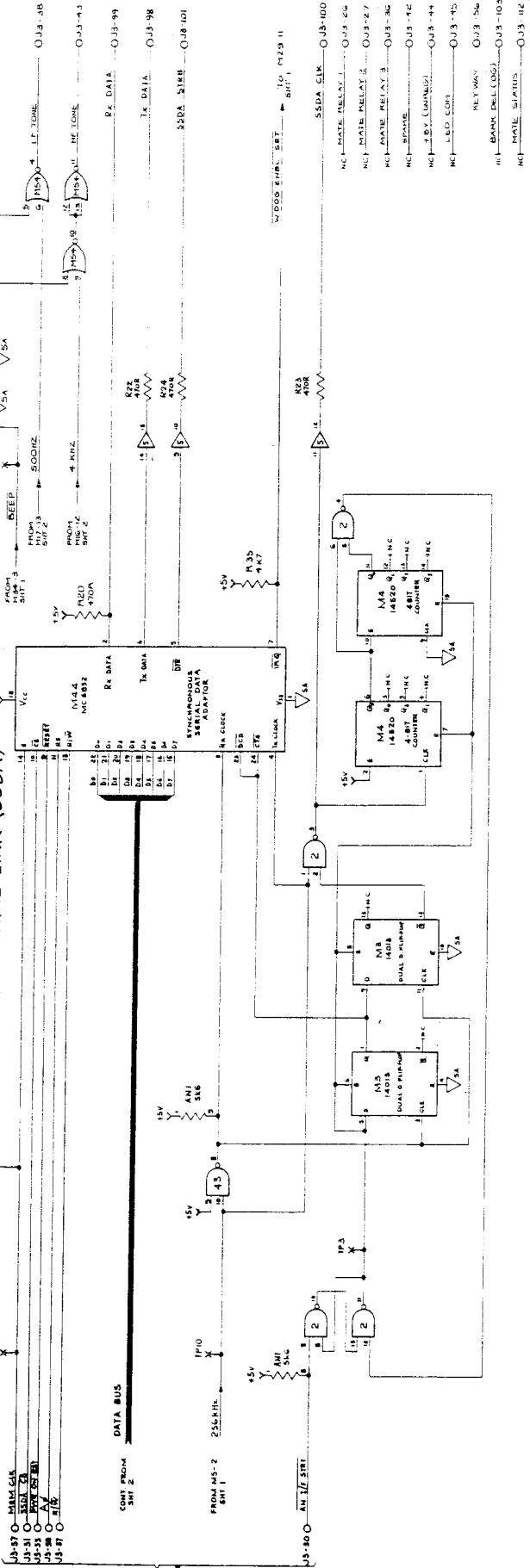
M18 GLASS BEAD 650P43, FITTED TO EACH LEG
OF THE FOLLOWING COMPONENTS: C1-C8,
C11, C13, C15, C18, C21, C23, C25,
C27, C29, C31, C33, C35, C37

| MOUNTING IC's | | | |
|---------------|----------|--|-----|
| USED TO MOUNT | | | |
| IN-WAYS | PART NO. | QUANTITY | REF |
| B | 605059 | 55 | 1 |
| 14 | 605060 | 1-3, 6-9, 12-14, 19-27, 35, 40, 43, 46-49, 50, 53, 54 | 28 |
| 16 | 605061 | 4, 5, 15, 16, 17, 20, 31-34, 37-39, 41, 42, 45, 47, 48, 51, 52, 10, 11, 18, 25, 26, 30 | 25 |
| 24 | 605064 | 44 | 1 |

MASTER CLOCKS

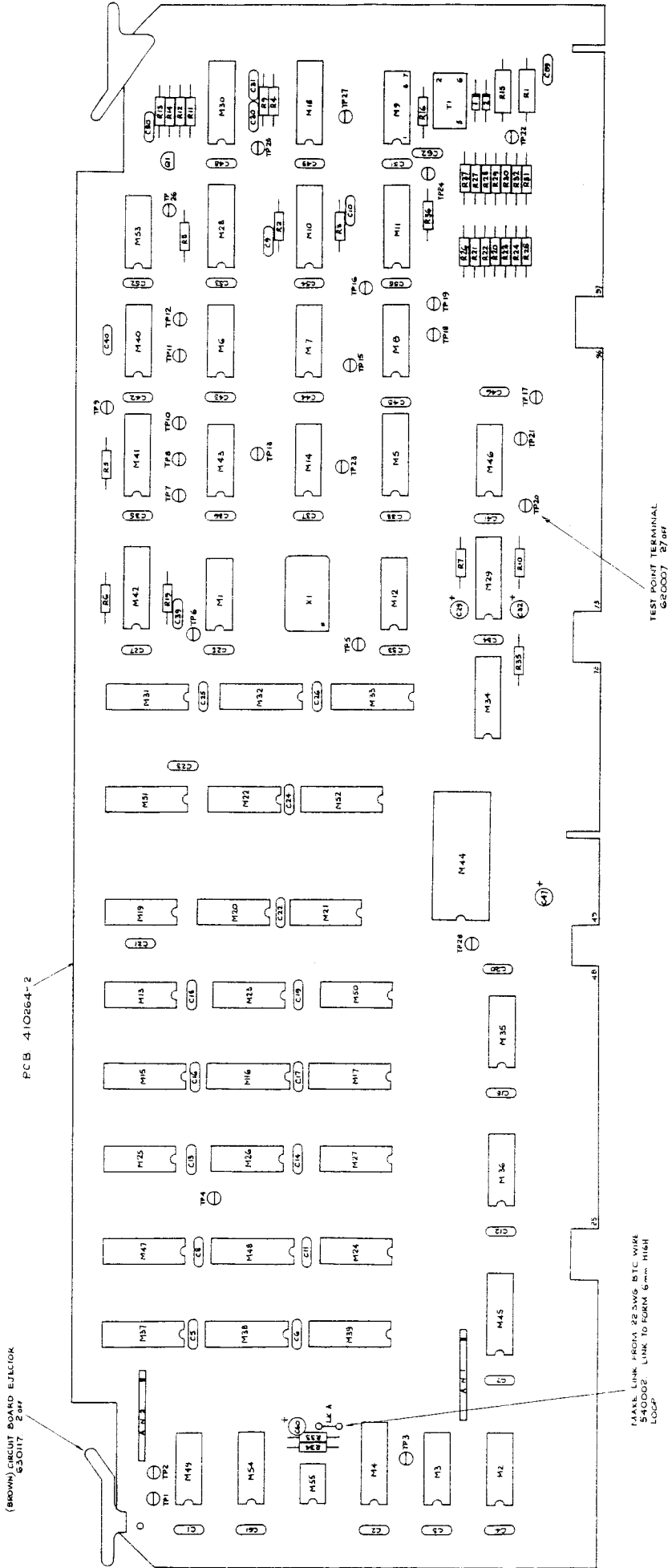


ANALOG CONTROL SERIAL LINK (SSDA)



ANALOG INTERFACE ASSEMBLY
Master Clocks and Analog Serial Link

ANALOG INTERFACE ASSEMBLY



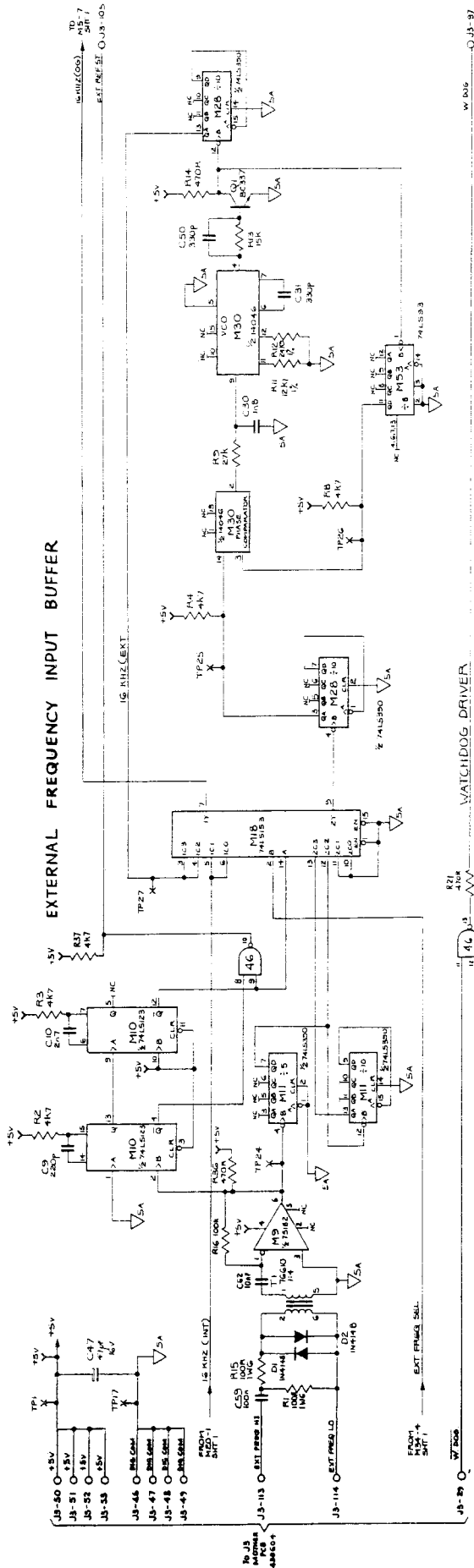
N.B. GLASS BEAD 630245 FITTED TO EACH LEG OF THE FOLLOWING COMPONENTS - CI-08, CI-09, CI-10, CI-11, CI-12, CI-13, CI-14, CI-15, CI-16, CI-17, CI-18, CI-19, CI-20, CI-21, CI-22, CI-23, CI-24, CI-25, CI-26, CI-27, CI-28, CI-29, CI-30, CI-31, CI-32, CI-33, CI-34, CI-35, CI-36, CI-37, CI-38, CI-39, CI-40, CI-41, CI-42, CI-43, CI-44, CI-45, CI-46, CI-47, CI-48, CI-49, CI-50, CI-51, CI-52, CI-53, CI-54, CI-55.

| MOUNTING I.C.s | | USED TO MOUNT | |
|----------------|----------|--|----------|
| IC NO. | PART NO. | IC NO. | PART NO. |
| 1 | 605059 | 55 | |
| 2 | 605060 | 1, 3, 6, 9, 12, 14, 19, 27, 35, 36, 40, 43, 46, 49, 50, 53, 54 | 28 |
| 3 | 605061 | 4, 5, 15, 16, 17, 23, 31, 34, 37, 39, 41, 42, 45, 47, 48, 51, 52, 50, 55 | 25 |
| 4 | 605064 | 44 | 1 |

PARALLEL LINK FROM 22 SWG BTC WIRE 1/32" DIAM. 1/4" LONG. LINK TO FORM 6mm HIGH LOOP.

TEST POINT TERMINAL GROUND 87 OH

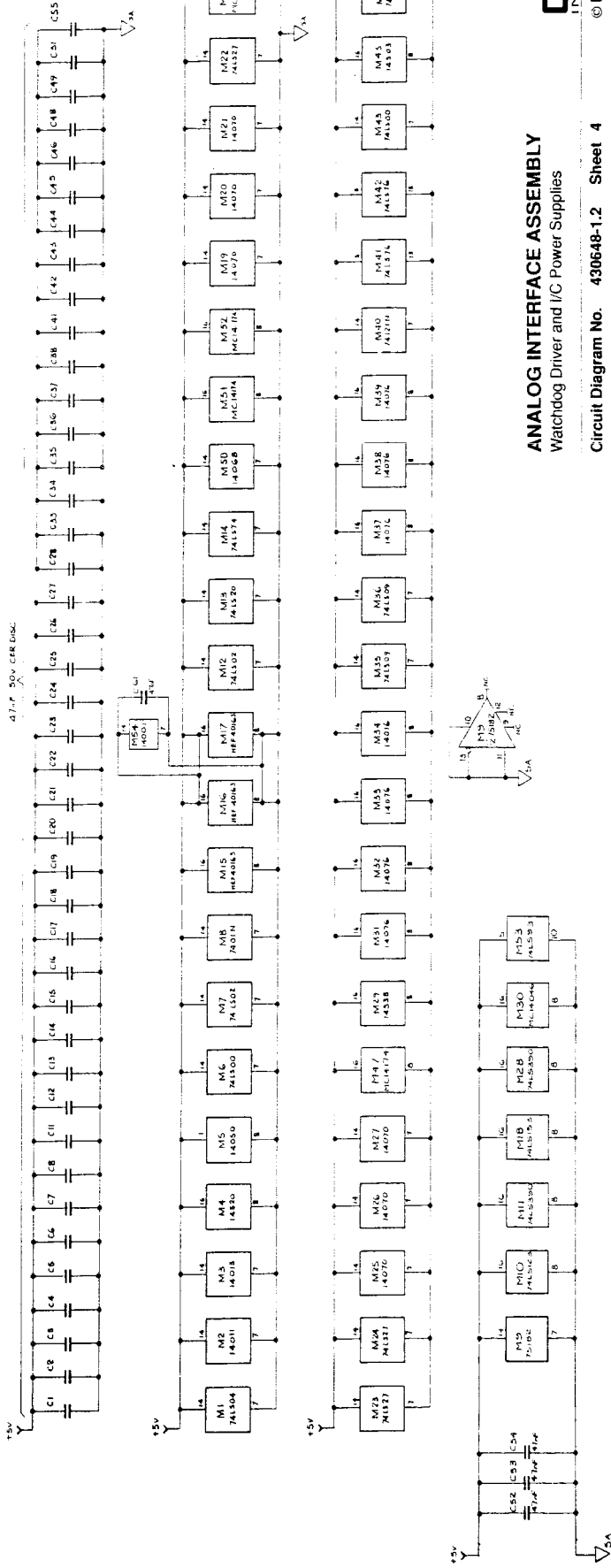
EXTERNAL FREQUENCY INPUT BUFFER



WATCHDOG DRIVER

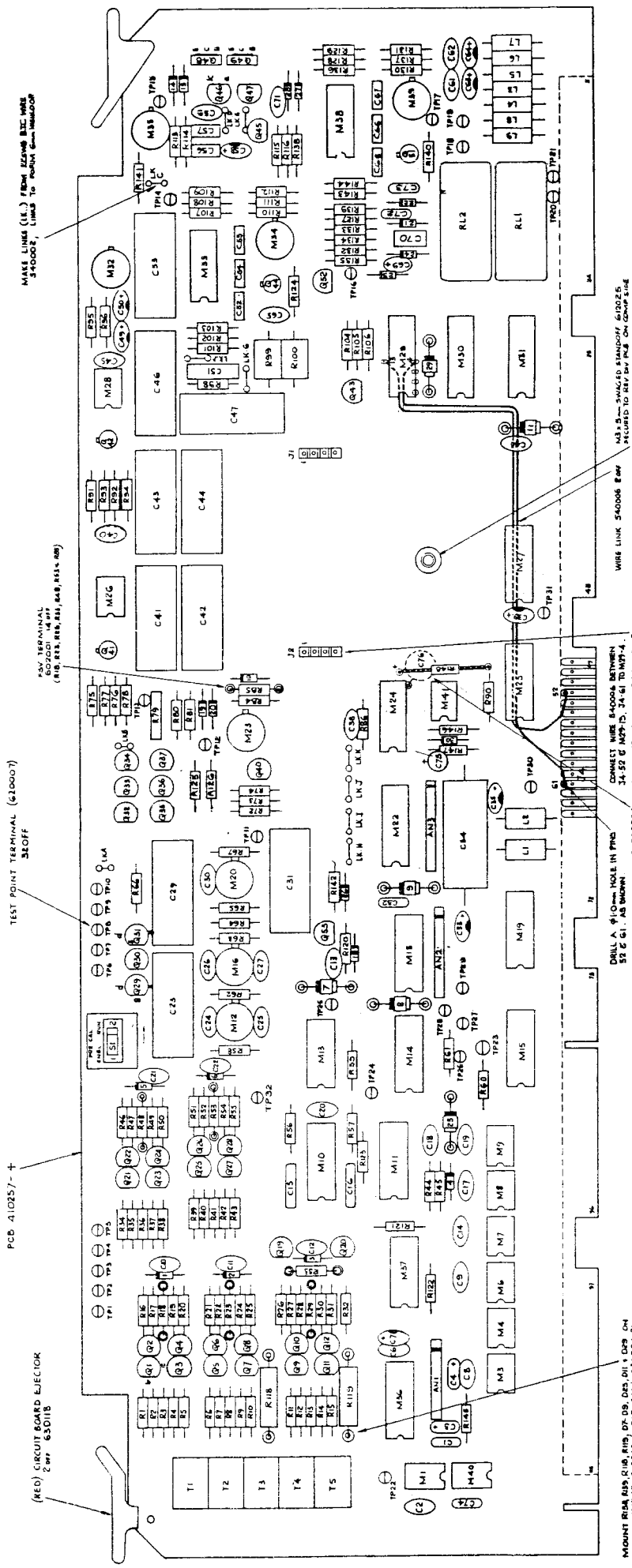


47.7kV 50V CERAMIC



ANALOG INTERFACE ASSEMBLY
 Watchdog Driver and I/C Power Supplies
 Circuit Diagram No. 430648-1.2 Sheet 4

REFERENCE DIVIDER ASSEMBLY



TEST POINT TERMINAL (410007) 3E0FF

PCB 410257-4

(RED) CIRCUIT BOARD EJECTOR 2WFF 63D115

MAKE LINES (L.L.) FROM BOARD BSC WIRE 300004, LEAD TO POINT FROM BOARD

28V TERMINAL TO BOARD 14 PIN (R10, R11, R12, R13, R14, R15, R16, R17, R18, R19, R20, R21, R22, R23, R24, R25, R26, R27, R28, R29, R30, R31, R32, R33, R34, R35, R36, R37, R38, R39, R40, R41, R42, R43, R44, R45, R46, R47, R48, R49, R50, R51, R52, R53, R54, R55, R56, R57, R58, R59, R60, R61, R62, R63, R64, R65, R66, R67, R68, R69, R70, R71, R72, R73, R74, R75, R76, R77, R78, R79, R80, R81, R82, R83, R84, R85, R86, R87, R88, R89, R90, R91, R92, R93, R94, R95, R96, R97, R98, R99, R100, R101, R102, R103, R104, R105, R106, R107, R108, R109, R110, R111, R112, R113, R114, R115, R116, R117, R118)

M3.5 3-WAY 2-PIN SHUNTER 600225 ATTACHED TO BOARD BY THE CONDUCTIVE

WIRE LINK 540006 2WFF

CONNECT WIRE 540006 BETWEEN 24-52 OF M3.5 TO 2A-61 TO M3.4. 4-WAY 1" PCB PLUG GOALR3 2WFF SOLDERED INTO MAIN PCB

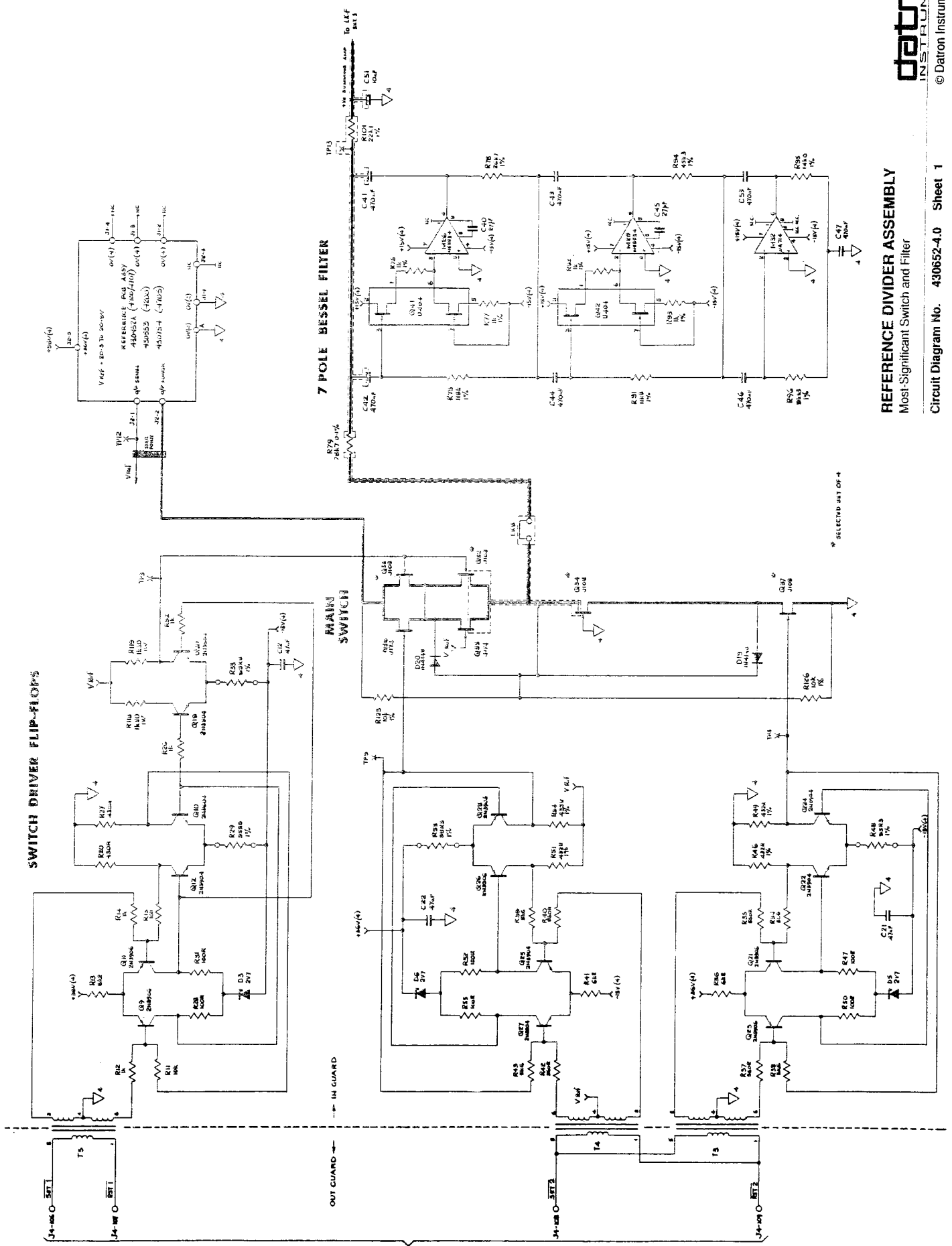
DRILL A 4/10mm HOLE IN PCB 53 & 61. AS SHOWN. BED CN IN SILICONE RUBBER 500004, 24-52 OF M3.5 TO 2A-61 TO M3.4. KEEP SILICONE RUBBER AT LEAST 2mm FROM BOARD. SOLDER WIRE FROM 550004 & WIRE CUT THROUGH COMP SIDE OF BOARD UNDER RIB PORTION.

MOUNT RIB R19, R10, R10, 07-09, DES DIL 1 D28 ON INSULATING BEAD (1-PIN LEAD) 610024 2WFF

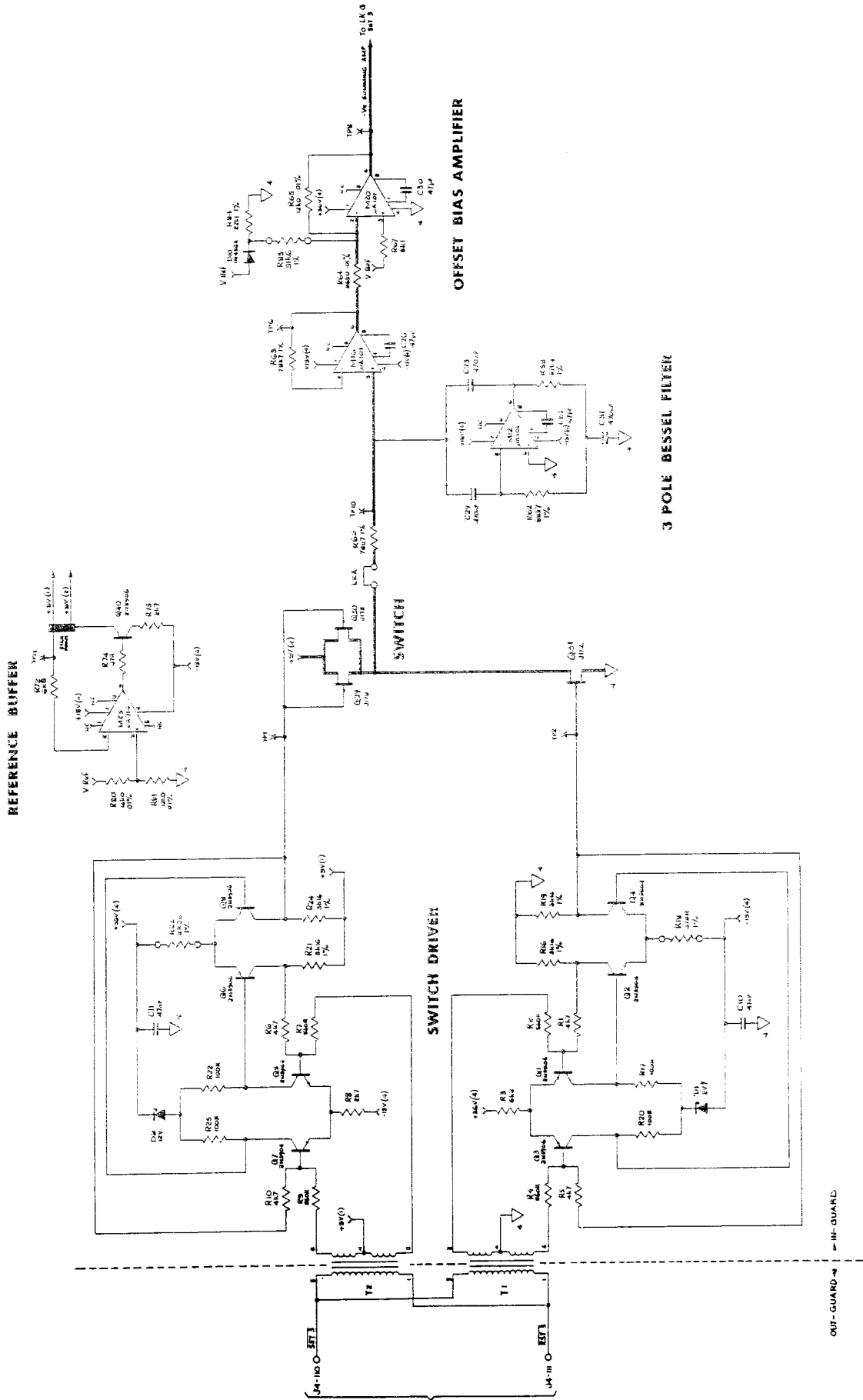
- MOUNTING I.C.**
- FIT M1, M2, M3, M4, M5, M6, M7, M8, M9, M10, M11, M12, M13, M14, M15, M16, M17, M18, M19, M20, M21, M22, M23, M24 ON 16-PIN DIL SOCKET 603053 II 2WFF
 - FIT M13, M24, M25, M26, M27, M28, M29, M30, M31, M32, M33, M34, M35, M36, M37, M38, M39, M40, M41, M42, M43, M44, M45, M46, M47, M48, M49, M50, M51, M52, M53, M54, M55, M56, M57, M58, M59, M60, M61, M62, M63, M64, M65, M66, M67, M68, M69, M70, M71, M72, M73, M74, M75, M76, M77, M78, M79, M80, M81, M82, M83, M84, M85, M86, M87, M88, M89, M90, M91, M92, M93, M94, M95, M96, M97, M98, M99, M100, M101, M102, M103, M104, M105, M106, M107, M108, M109, M110, M111, M112, M113, M114, M115, M116, M117, M118 ON 16-PIN DIL SOCKET 603054 13WFF

REFERENCE DIVIDER ASSEMBLY
 Most-Significant Switch and Filter

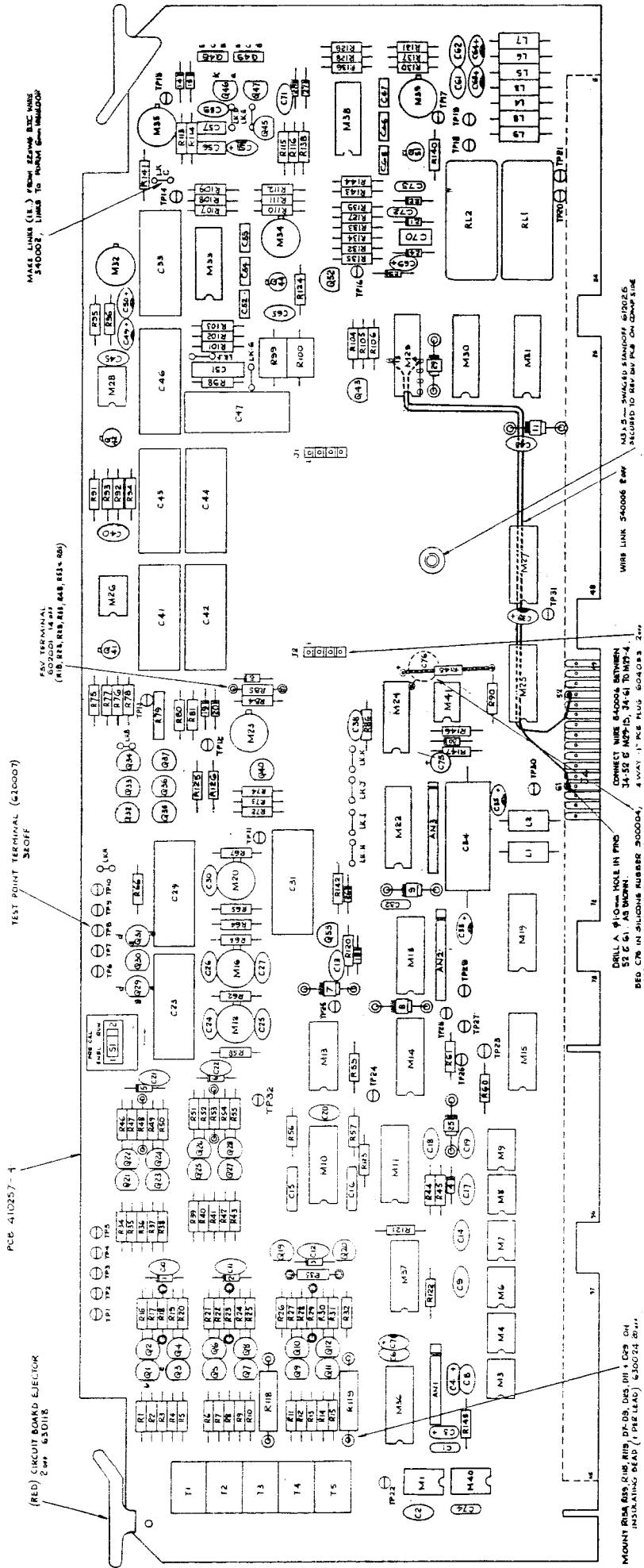
Circuit Diagram No. 430652-4.0 Sheet 1



70 J4 MOTHER PCB 430652-4.0



REFERENCE DIVIDER ASSEMBLY



TEST POINT TERMINAL (610007) 3K OFF

PCB 410257-4

(RED) CIRCUIT BOARD ELECTRO 2.00 65018

MOUNTING IC.

M15, M14, M13, M12, M11, M10, M9, M8, M7, M6, M5, M4, M3, M2, M1, M18, M19, M20, M21, M22, M23, M24, M25, M31, M32, M33, M34, M35, M36, M37, M38, M39, M40, M41, M42, M43, M44, M45, M46, M47, M48, M49, M50, M51, M52, M53, M54, M55, M56, M57, M58, M59, M60, M61, M62, M63, M64, M65, M66, M67, M68, M69, M70, M71, M72, M73, M74, M75, M76, M77, M78, M79, M80, M81, M82, M83, M84, M85, M86, M87, M88, M89, M90, M91, M92, M93, M94, M95, M96, M97, M98, M99, M100

MOUNTING IC. FIT MOUNTING, MIC-M9, M40, M26, M28, M41 ON 8-PIN DIP SOCKET 605093 II 1.50 FIT M15, M24, M45, M47, M38 ON 4-PIN DIP SOCKET 605060 5.00 FIT M10, M11, M14, M16, M18, M19, M20, M21, M22, M23, M24, M25 ON 8-PIN DIP SOCKET 605093 1.50 FIT M1, M2, M3, M4, M5, M6, M7, M8, M9 ON 8-PIN DIP SOCKET 605093 1.50

MOUNTING IC. FIT MOUNTING, MIC-M9, M40, M26, M28, M41 ON 8-PIN DIP SOCKET 605093 II 1.50 FIT M15, M24, M45, M47, M38 ON 4-PIN DIP SOCKET 605060 5.00 FIT M10, M11, M14, M16, M18, M19, M20, M21, M22, M23, M24, M25 ON 8-PIN DIP SOCKET 605093 1.50 FIT M1, M2, M3, M4, M5, M6, M7, M8, M9 ON 8-PIN DIP SOCKET 605093 1.50

MASSE LINKS (L.S.) FROM BOARD BSC WIRE 5400027. LINKS TO MAIN GND MOUNTING

PCB TERMINAL 605001 14 071 (R10, R25, R38, R48, R51, R55)

DRILL A .910 HOLE IN PWB 24-32 G TAP (P.L.S.) 34-36 TO MTP-4. 4.00 COLLECTED INTO MAIN PCB

DRILL A .910 HOLE IN PWB 24-32 G TAP (P.L.S.) 34-36 TO MTP-4. 4.00 COLLECTED INTO MAIN PCB

DRILL A .910 HOLE IN PWB 24-32 G TAP (P.L.S.) 34-36 TO MTP-4. 4.00 COLLECTED INTO MAIN PCB

DRILL A .910 HOLE IN PWB 24-32 G TAP (P.L.S.) 34-36 TO MTP-4. 4.00 COLLECTED INTO MAIN PCB

WIRE LINK 540006 BAW

WIRE LINK 540006 BAW

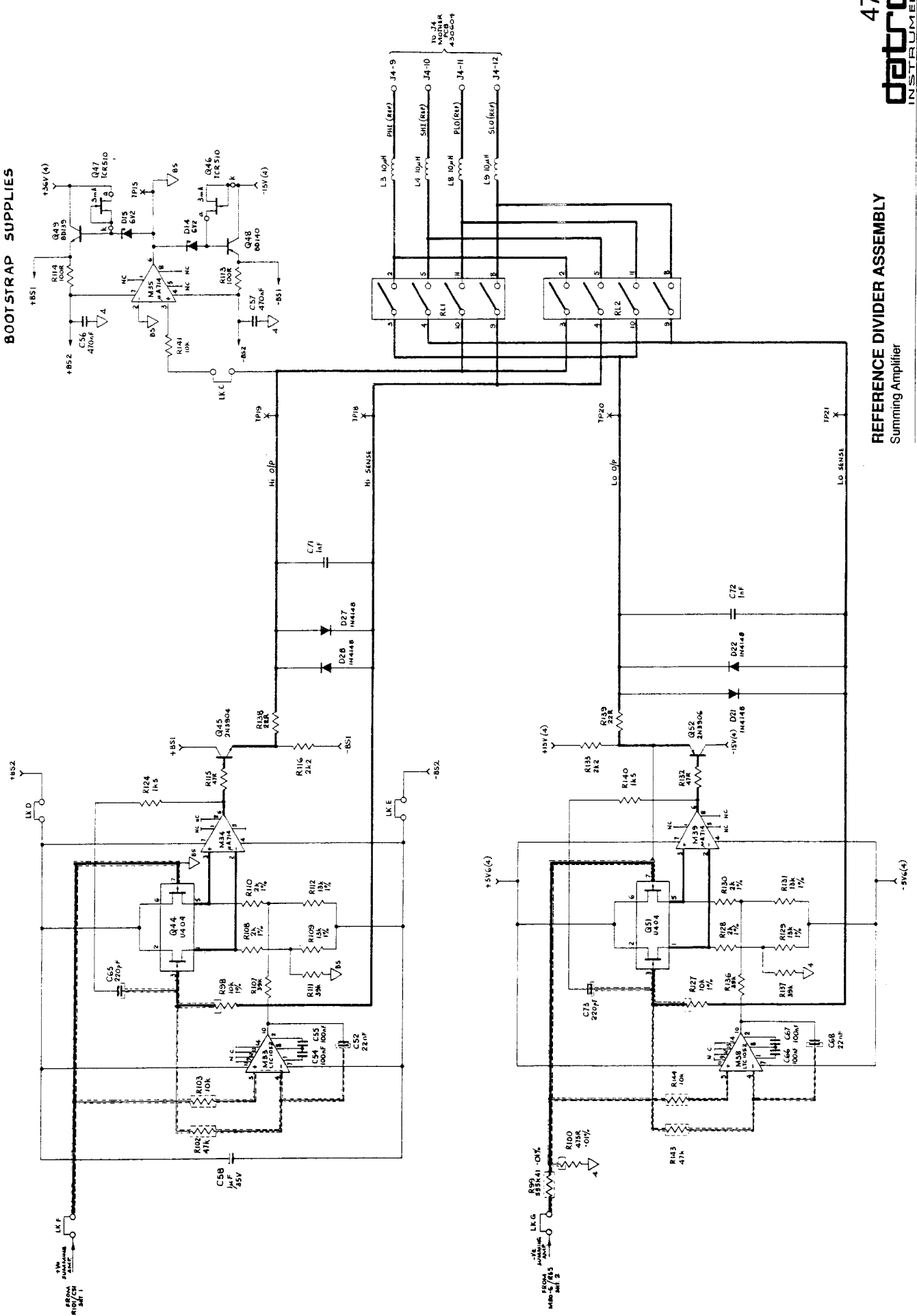
WIRE LINK 540006 BAW

WIRE LINK 540006 BAW

WIRE LINK 540006 BAW

WIRE LINK 540006 BAW

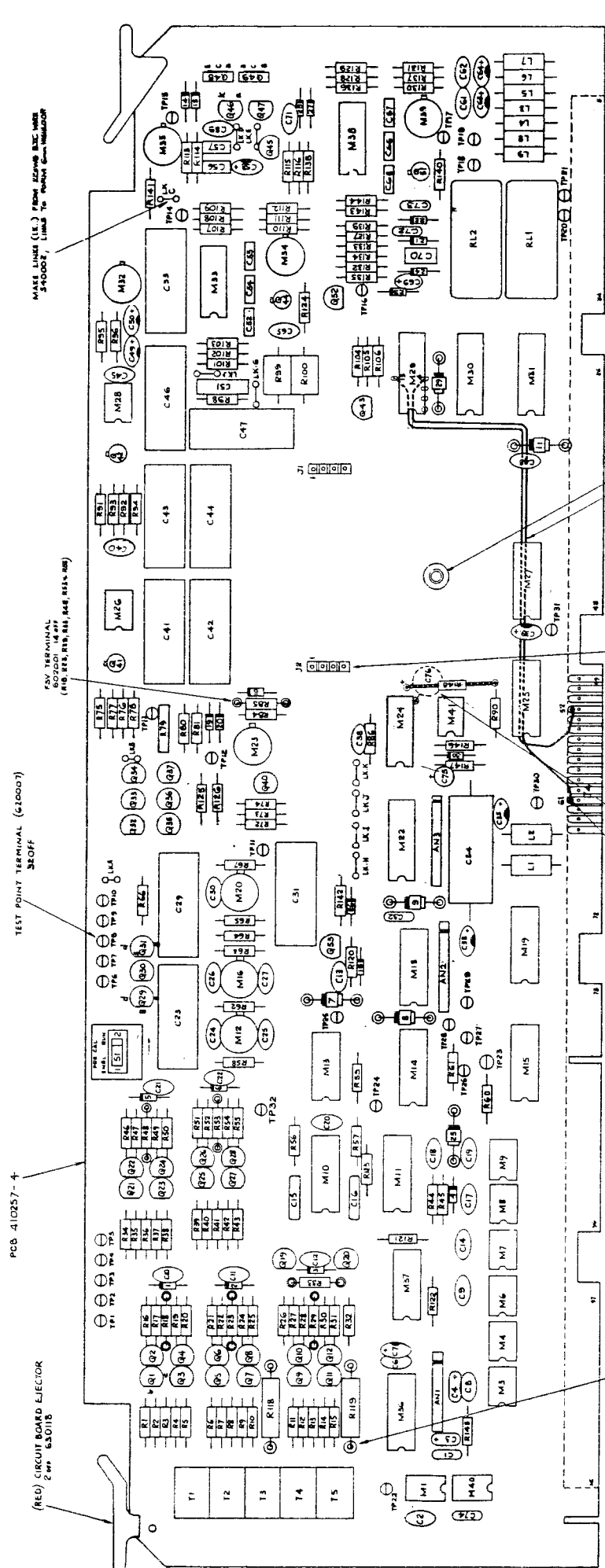
BOOTSTRAP SUPPLIES



REFERENCE DIVIDER ASSEMBLY
Summing Amplifier

Circuit Diagram No. 430652-4.0 Sheet 3

REFERENCE DIVIDER ASSEMBLY



PCB 410257-4

TEST POINT TERMINAL (420007) 3E0FF

FSV TERMINAL 14 8FF (R1, R2, R3, R4, R5, R6)

MAKE LINES (I.E.) FROM 820008 BIC WIRE 840008, LINK TO POINT 820008

WIRE LINK 840008 8 2W

CONNECT WIRE 840008 BETWEEN 34, 52 & 61 TO INT-4. 4-WAY 1" PCB PLUG 804008 2W SOLDERED INTO MAIN PCB

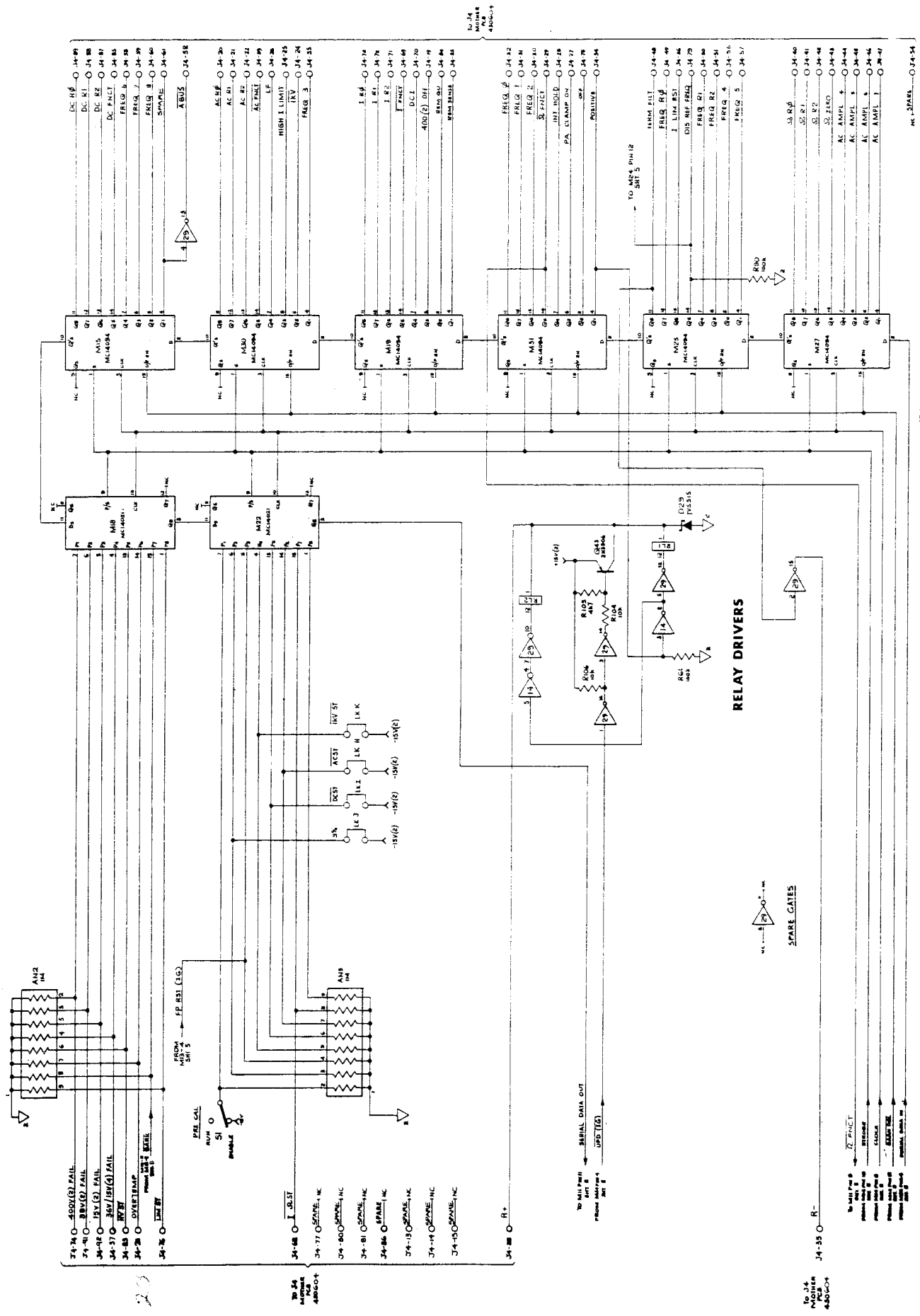
DRILL A 9/16" HOLE IN PWB 52 & 61 AS SHOWN. DES. CR IN SILICONE RUBBER 200004. 1.5" DIA. HOLE IN PWB. 1.5" DIA. HOLE IN PWB. 1.5" DIA. HOLE IN PWB. 1.5" DIA. HOLE IN PWB. CUT TRACK ON COMP. SIDE OF BOARD UNDER R-46 POSITION.

MOUNT R18, R19, R19, R19, R19, R19 ON INSULATING BEAD (1 IN LEAD) 610024 20 8FF

MOUNTING I.C.S.
 FIT M1, M14, M2, M3, M4, M5, M6, M7, M8, M9, M10, M11, M12, M13, M14, M15, M16, M17, M18, M19, M20, M21, M22, M23, M24
 ON 8 WAY DIL SOCKET 603059 11 8FF
 FIT M12, M24, M33, M37, M38
 ON 14 WAY DIL SOCKET 605060 3 8FF
 FIT M10, M11, M14, M15, M16, M17, M18, M19, M20, M21, M22, M23, M24
 ON 16 WAY DIL SOCKET 605061 12 8FF

REFERENCE DIVIDER ASSEMBLY

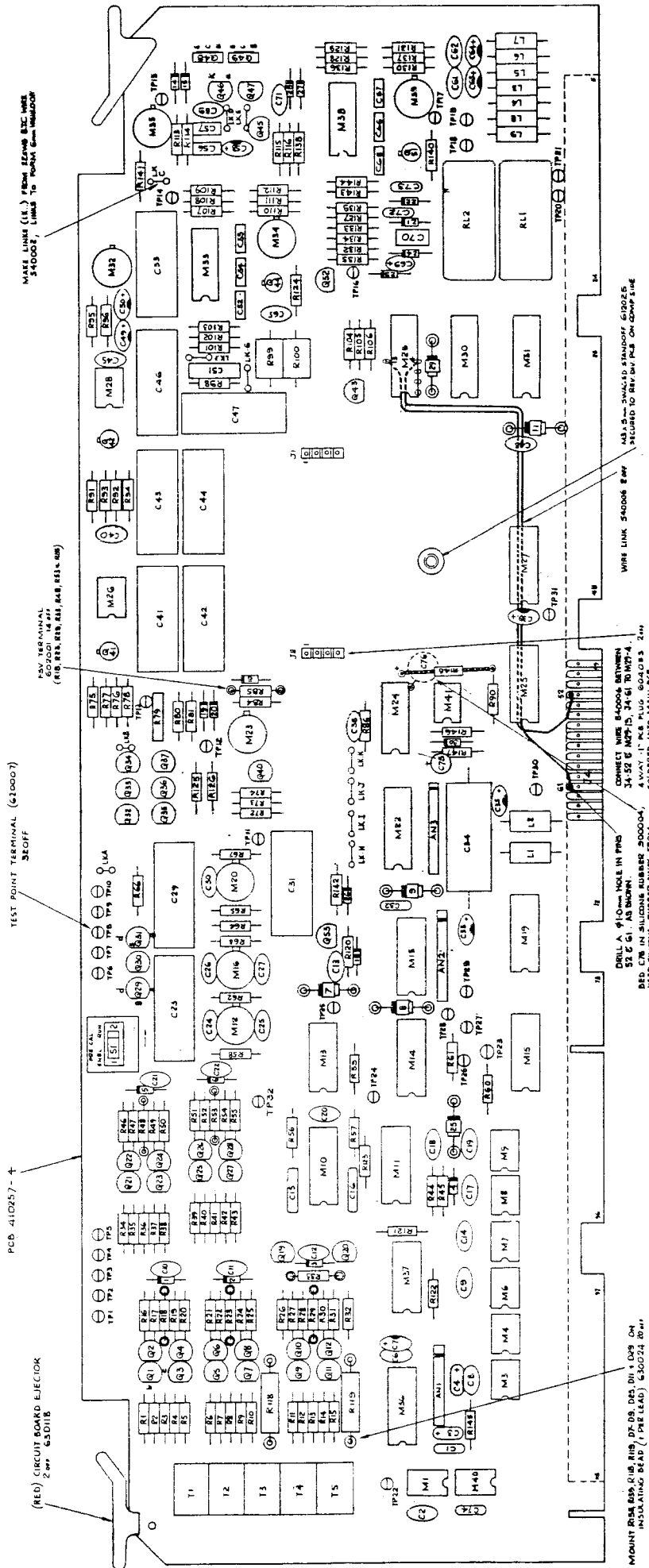
Serial / Parallel Data Converter



REFERENCE DIVIDER ASSEMBLY

datron
INSTRUMENTS

4708



(RED) CIRCUIT BOARD ELEC.
2.00 630118

PCB 410257-4

TEST POINT TERMINAL (620007)
3500FF

NEW TERMINAL
605001 14.00
(RIB, R22, R19, R41, R48, R51 & 509)

MAKE LINKS (I.E.) FROM LEADS ETC. WIRE
540002, LINKS TO POINTS ON WINDUP

- MOUNTING I.C.
 FIT M1, M14, M6, M9, M40, M28, M38, M41
 ON 8-WAY DIL SOCKET 605059 11.00
 FIT M15, M28, M33, M37, M38
 ON 14-WAY DIL SOCKET 605060 5.00
 FIT M40, M41, M44, M45, M49, M50, M51, M54, M57
 ON 16-WAY DIL SOCKET 605061 13.00

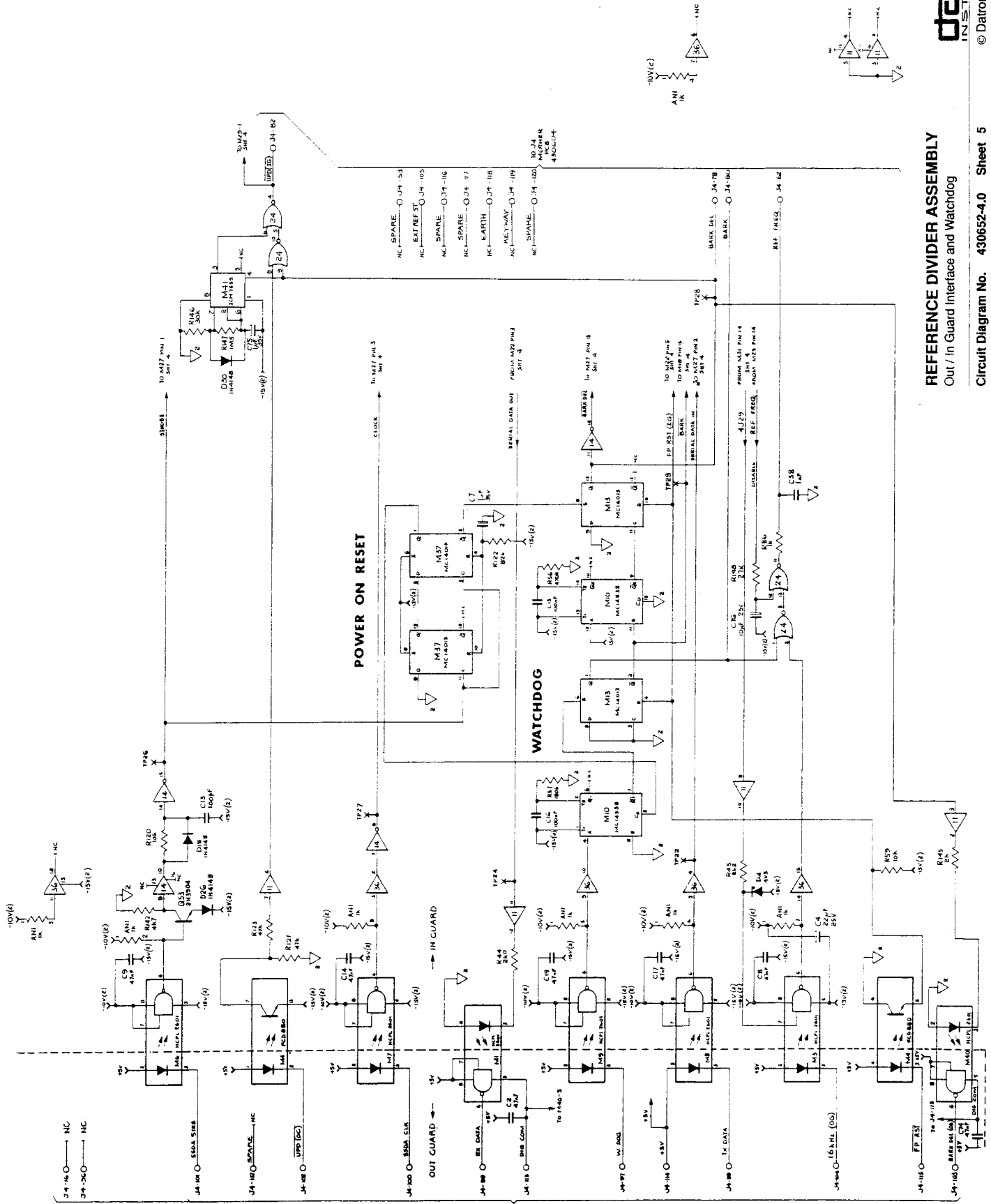
MOUNT RIBS, R55, R119, DP-D8, DES-D11 & D45 ON
INSULATING BEAD (1 PER LEAD) 630024 20.00

DRILL A .10mm HOLE IN FRIB
53 & 61 AS SHOWN.
RED CN IN SILICONE RUBBER 500004,
4-WAY, 1" PER PLUG, 605055 2.00
I.E. LANS (CHECK SIZE OF SOLETS)
SILVY PLASTIC 500004 4 WIRE
CUT TRACK ON COMP SIDE OF BOARD
UNDER THIS POSITION.

CONNECT WIRE 540006 BETWEEN
34-55 & MP-15, 34-61 TO MP-4.
4-WAY, 1" PER PLUG, 605055 2.00
ASSEMBLED INTO MAIN PCB

M31, 5-THREADED STANOFF 500025.
REQUIRED TO REV. DIV. LINE ON COMP. LINE

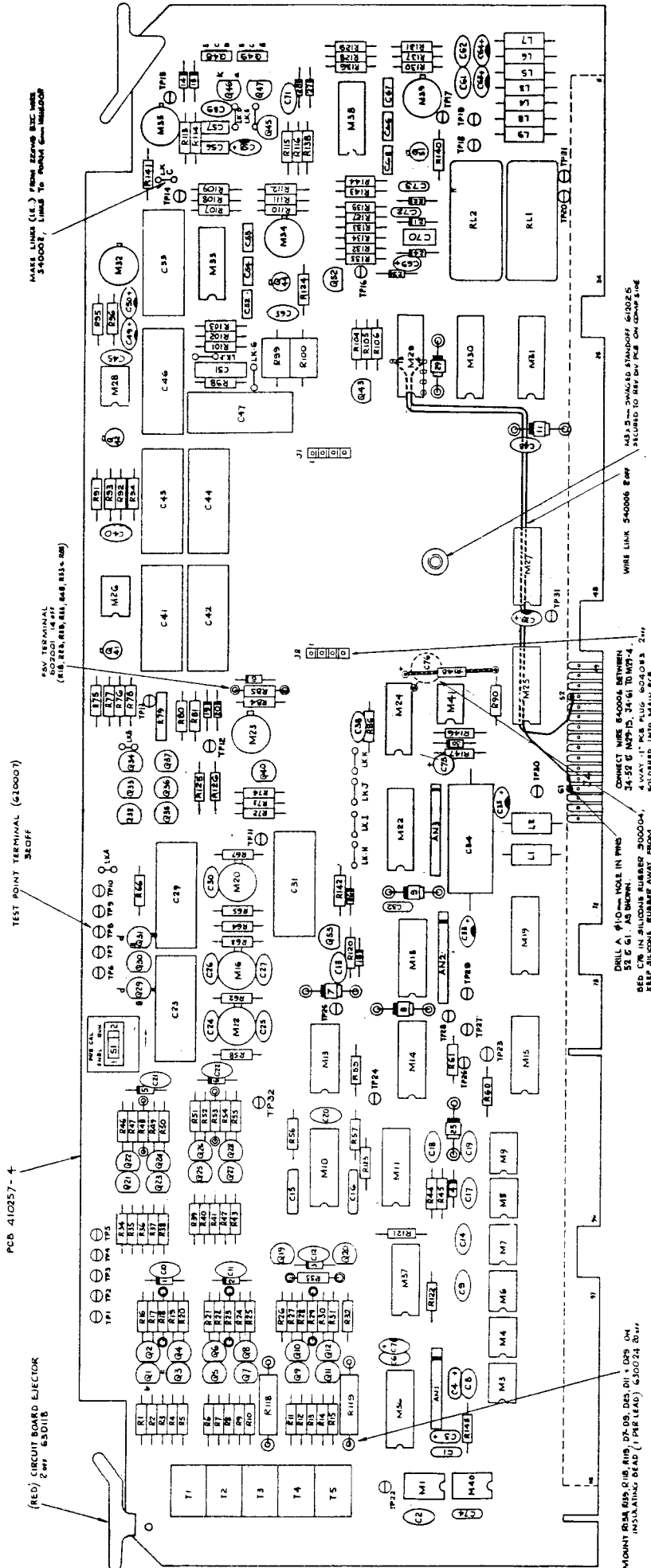
WIRE LINK 540006 2.00



REFERENCE DIVIDER ASSEMBLY
Out / In Guard Interface and Watchdog

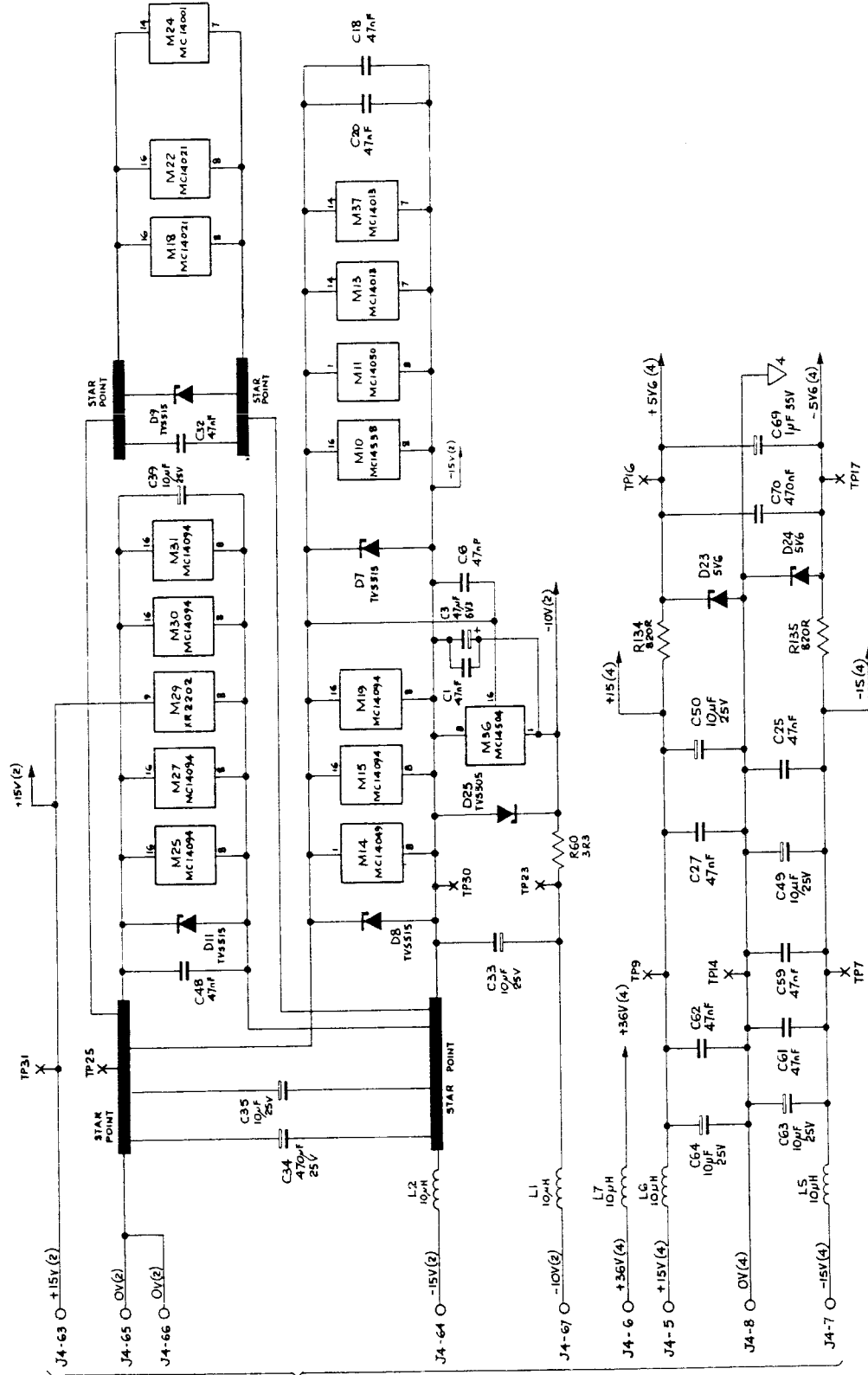
Circuit Diagram No. 430652-4.0 Sheet 5

REFERENCE DIVIDER ASSEMBLY



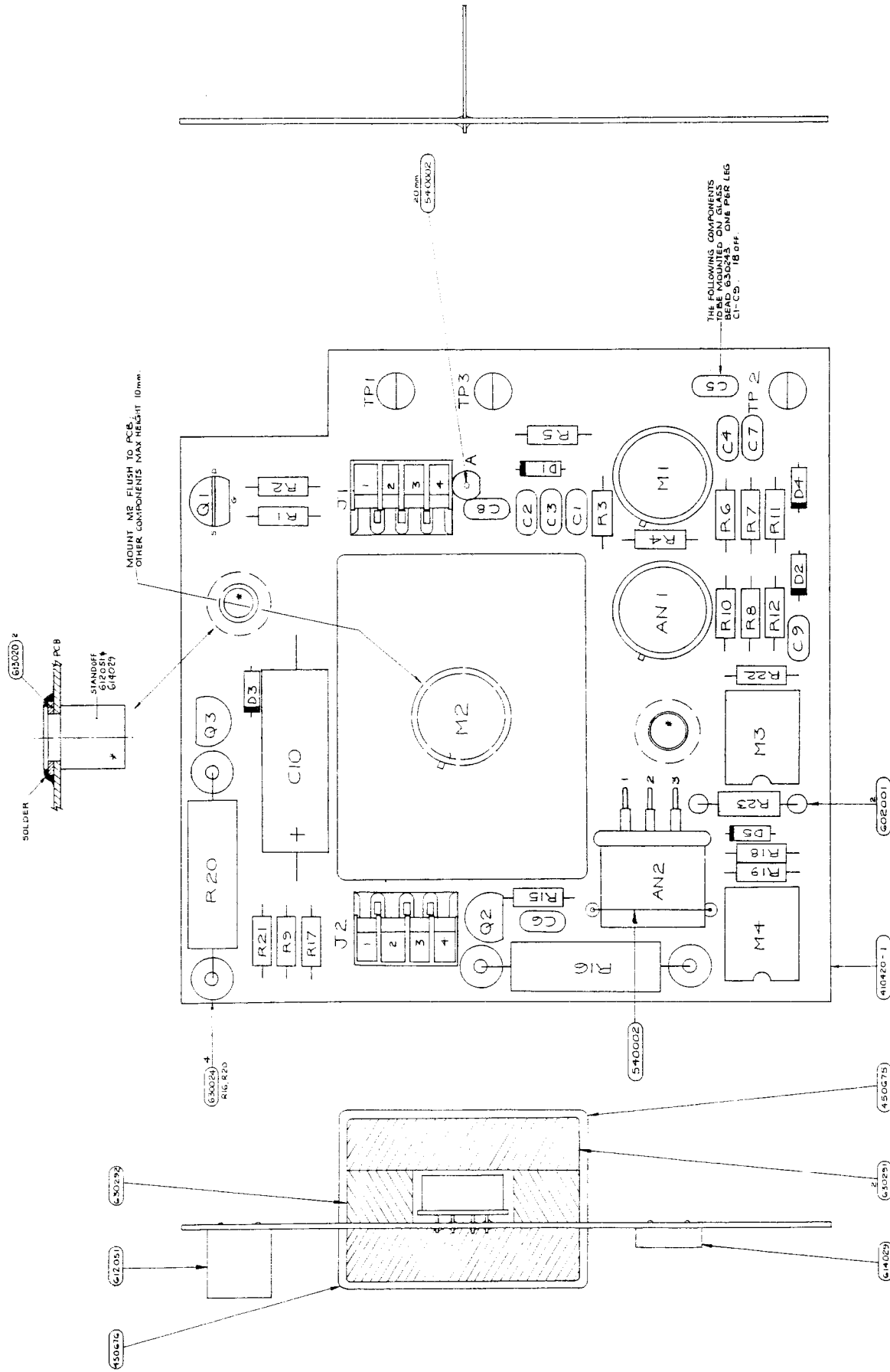
MOUNTING I.C.
 FIT WITH M14, M15, M16, M17, M18, M19, M20, M21, M22, M23, M24, M25, M26, M27, M28, M29, M30, M31, M32, M33, M34, M35, M36, M37, M38, M39, M40, M41, M42, M43, M44, M45, M46, M47, M48, M49, M50, M51, M52, M53, M54, M55, M56, M57, M58, M59, M60, M61, M62, M63, M64, M65, M66, M67, M68, M69, M70, M71, M72, M73, M74, M75, M76, M77, M78, M79, M80, M81, M82, M83, M84, M85, M86, M87, M88, M89, M90, M91, M92, M93, M94, M95, M96, M97, M98, M99, M100.

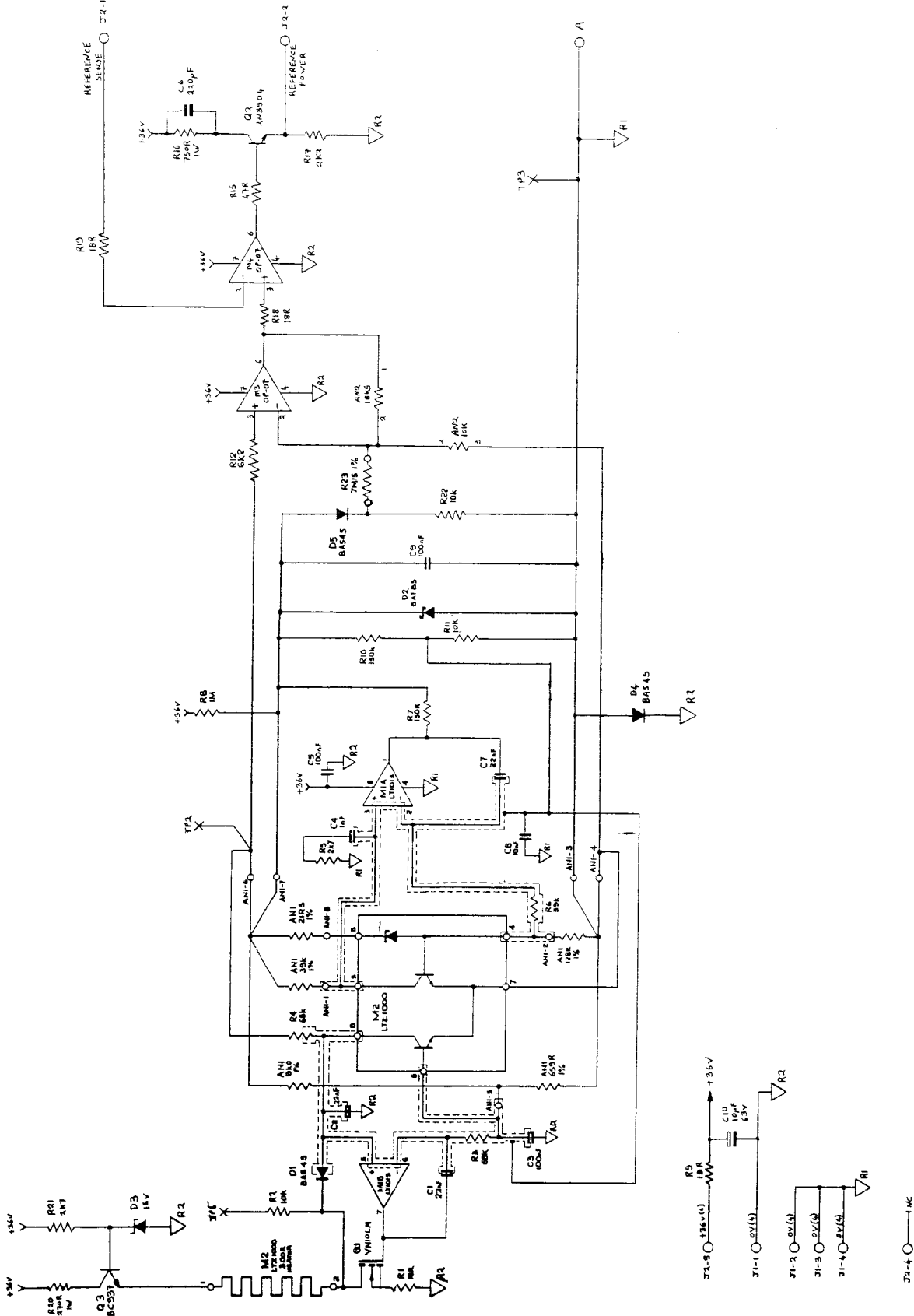
MOUNTING I.C.
 FIT WITH M14, M15, M16, M17, M18, M19, M20, M21, M22, M23, M24, M25, M26, M27, M28, M29, M30, M31, M32, M33, M34, M35, M36, M37, M38, M39, M40, M41, M42, M43, M44, M45, M46, M47, M48, M49, M50, M51, M52, M53, M54, M55, M56, M57, M58, M59, M60, M61, M62, M63, M64, M65, M66, M67, M68, M69, M70, M71, M72, M73, M74, M75, M76, M77, M78, M79, M80, M81, M82, M83, M84, M85, M86, M87, M88, M89, M90, M91, M92, M93, M94, M95, M96, M97, M98, M99, M100.



TO J4
M1-M24
4306004

CALIBRATOR REFERENCE



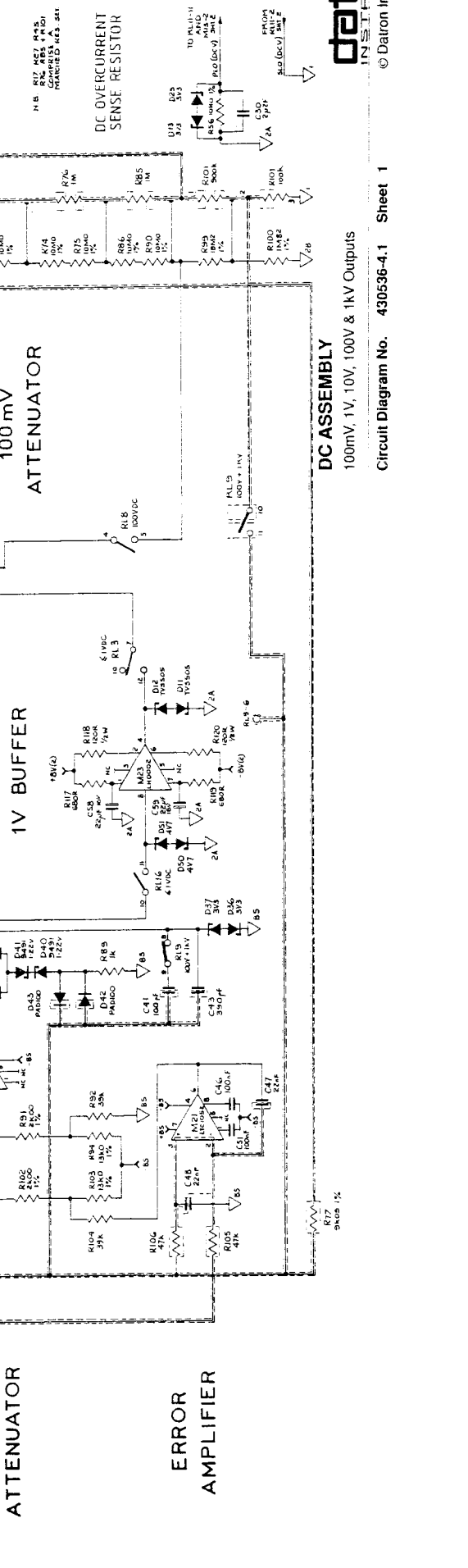
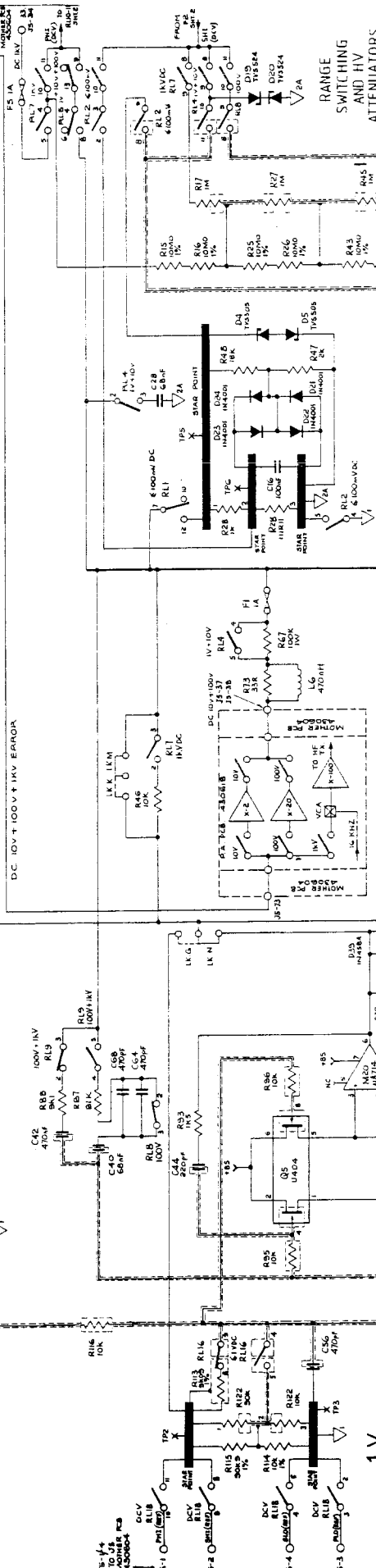
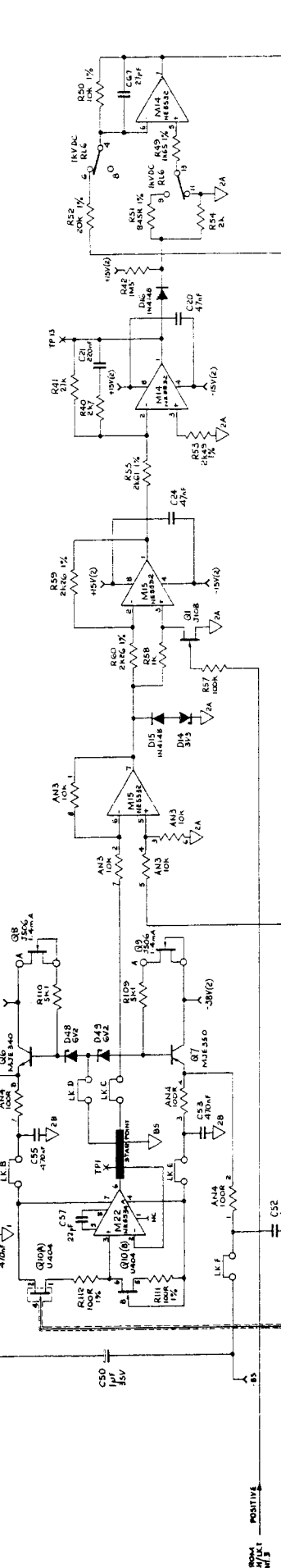


CALIBRATOR REFERENCE

Circuit Diagram No. DC400761-1.0 Sheet 1

BOOTSTRAP SUPPLIES

VCA DRIVE



N.B. CLASS BEAD 8004S BITTED TO EACH LEG OF THE FOLLOWING COMPONENTS: C13, C14, C15, C16, C17, C18, C19, C20, C21, C22, C23, C24, C25, C26, C27, C28, C29, C30, C31, C32, C33, C34, C35, C36, C37, C38, C39, C40.

THE FOLLOWING COMPONENTS TO BE FINISHED ON SMALL CERAMIC BEADS W5002G: R1-E, C30, R1 PER LEAD R85, R108, C49, 2 PER LEAD

EXAMINE THE FOLLOWING COMPONENTS ON LARGE CERAMIC BEADS W5002.4: 2 PER LEAD: R17, R27, R45, R76, R85, R101, R107, R122 THE FOLLOWING COMPONENTS TO BE MARKED: ALSO DRAWN BEAD-LESS: R104, R105, R106, R107, R108, R109, R110, R111, R112, R113, R114, R115, R116, R117, R118, R119, R120, R121, R122, R123, R124, R125, R126, R127, R128, R129, R130, R131, R132, R133, R134, R135, R136, R137, R138, R139, R140, R141, R142, R143, R144, R145, R146, R147, R148, R149, R150, R151, R152, R153, R154, R155, R156, R157, R158, R159, R160, R161, R162, R163, R164, R165, R166, R167, R168, R169, R170, R171, R172, R173, R174, R175, R176, R177, R178, R179, R180, R181, R182, R183, R184, R185, R186, R187, R188, R189, R190, R191, R192, R193, R194, R195, R196, R197, R198, R199, R200, R201, R202, R203, R204, R205, R206, R207, R208, R209, R210, R211, R212, R213, R214, R215, R216, R217, R218, R219, R220, R221, R222, R223, R224, R225, R226, R227, R228, R229, R230, R231, R232, R233, R234, R235, R236, R237, R238, R239, R240, R241, R242, R243, R244, R245, R246, R247, R248, R249, R250, R251, R252, R253, R254, R255, R256, R257, R258, R259, R260, R261, R262, R263, R264, R265, R266, R267, R268, R269, R270, R271, R272, R273, R274, R275, R276, R277, R278, R279, R280, R281, R282, R283, R284, R285, R286, R287, R288, R289, R290, R291, R292, R293, R294, R295, R296, R297, R298, R299, R300, R301, R302, R303, R304, R305, R306, R307, R308, R309, R310, R311, R312, R313, R314, R315, R316, R317, R318, R319, R320, R321, R322, R323, R324, R325, R326, R327, R328, R329, R330, R331, R332, R333, R334, R335, R336, R337, R338, R339, R340, R341, R342, R343, R344, R345, R346, R347, R348, R349, R350, R351, R352, R353, R354, R355, R356, R357, R358, R359, R360, R361, R362, R363, R364, R365, R366, R367, R368, R369, R370, R371, R372, R373, R374, R375, R376, R377, R378, R379, R380, R381, R382, R383, R384, R385, R386, R387, R388, R389, R390, R391, R392, R393, R394, R395, R396, R397, R398, R399, R400, R401, R402, R403, R404, R405, R406, R407, R408, R409, R410, R411, R412, R413, R414, R415, R416, R417, R418, R419, R420, R421, R422, R423, R424, R425, R426, R427, R428, R429, R430, R431, R432, R433, R434, R435, R436, R437, R438, R439, R440, R441, R442, R443, R444, R445, R446, R447, R448, R449, R450, R451, R452, R453, R454, R455, R456, R457, R458, R459, R460, R461, R462, R463, R464, R465, R466, R467, R468, R469, R470, R471, R472, R473, R474, R475, R476, R477, R478, R479, R480, R481, R482, R483, R484, R485, R486, R487, R488, R489, R490, R491, R492, R493, R494, R495, R496, R497, R498, R499, R500, R501, R502, R503, R504, R505, R506, R507, R508, R509, R510, R511, R512, R513, R514, R515, R516, R517, R518, R519, R520, R521, R522, R523, R524, R525, R526, R527, R528, R529, R530, R531, R532, R533, R534, R535, R536, R537, R538, R539, R540, R541, R542, R543, R544, R545, R546, R547, R548, R549, R550, R551, R552, R553, R554, R555, R556, R557, R558, R559, R560, R561, R562, R563, R564, R565, R566, R567, R568, R569, R570, R571, R572, R573, R574, R575, R576, R577, R578, R579, R580, R581, R582, R583, R584, R585, R586, R587, R588, R589, R590, R591, R592, R593, R594, R595, R596, R597, R598, R599, R600, R601, R602, R603, R604, R605, R606, R607, R608, R609, R610, R611, R612, R613, R614, R615, R616, R617, R618, R619, R620, R621, R622, R623, R624, R625, R626, R627, R628, R629, R630, R631, R632, R633, R634, R635, R636, R637, R638, R639, R640, R641, R642, R643, R644, R645, R646, R647, R648, R649, R650, R651, R652, R653, R654, R655, R656, R657, R658, R659, R660, R661, R662, R663, R664, R665, R666, R667, R668, R669, R670, R671, R672, R673, R674, R675, R676, R677, R678, R679, R680, R681, R682, R683, R684, R685, R686, R687, R688, R689, R690, R691, R692, R693, R694, R695, R696, R697, R698, R699, R700, R701, R702, R703, R704, R705, R706, R707, R708, R709, R710, R711, R712, R713, R714, R715, R716, R717, R718, R719, R720, R721, R722, R723, R724, R725, R726, R727, R728, R729, R730, R731, R732, R733, R734, R735, R736, R737, R738, R739, R740, R741, R742, R743, R744, R745, R746, R747, R748, R749, R750, R751, R752, R753, R754, R755, R756, R757, R758, R759, R760, R761, R762, R763, R764, R765, R766, R767, R768, R769, R770, R771, R772, R773, R774, R775, R776, R777, R778, R779, R780, R781, R782, R783, R784, R785, R786, R787, R788, R789, R790, R791, R792, R793, R794, R795, R796, R797, R798, R799, R800, R801, R802, R803, R804, R805, R806, R807, R808, R809, R810, R811, R812, R813, R814, R815, R816, R817, R818, R819, R820, R821, R822, R823, R824, R825, R826, R827, R828, R829, R830, R831, R832, R833, R834, R835, R836, R837, R838, R839, R840, R841, R842, R843, R844, R845, R846, R847, R848, R849, R850, R851, R852, R853, R854, R855, R856, R857, R858, R859, R860, R861, R862, R863, R864, R865, R866, R867, R868, R869, R870, R871, R872, R873, R874, R875, R876, R877, R878, R879, R880, R881, R882, R883, R884, R885, R886, R887, R888, R889, R890, R891, R892, R893, R894, R895, R896, R897, R898, R899, R900, R901, R902, R903, R904, R905, R906, R907, R908, R909, R910, R911, R912, R913, R914, R915, R916, R917, R918, R919, R920, R921, R922, R923, R924, R925, R926, R927, R928, R929, R930, R931, R932, R933, R934, R935, R936, R937, R938, R939, R940, R941, R942, R943, R944, R945, R946, R947, R948, R949, R950, R951, R952, R953, R954, R955, R956, R957, R958, R959, R960, R961, R962, R963, R964, R965, R966, R967, R968, R969, R970, R971, R972, R973, R974, R975, R976, R977, R978, R979, R980, R981, R982, R983, R984, R985, R986, R987, R988, R989, R990, R991, R992, R993, R994, R995, R996, R997, R998, R999, R1000.

| MOUNTING T.C.S. | | |
|-----------------|--------|---------------|
| HT WAYS | PART # | USED TO MOUNT |
| 8 | 605059 | 5 |
| 14 | 605060 | 4 |
| 16 | 605061 | 3 |
| 20 | 605070 | 3 |

148 6047 AND 6048 SHOULD BE COLOURED MARKED BLUE 7/8 THE WHITE WIRE SHOULD BE COLOURED MARKED RED

MARKING KB4 ON FSV TERMINALS 620007 21 OF

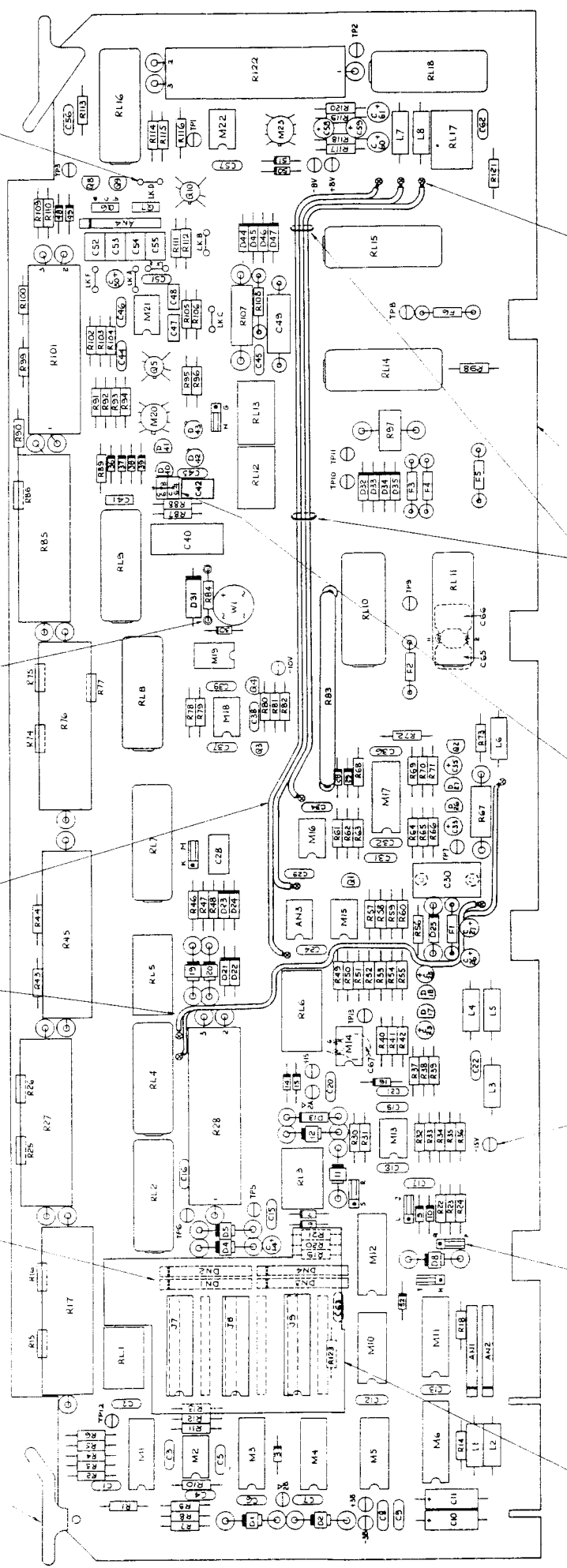
MAKE SURE THE 1.5% FROM 200006 01-NR-24-0000

118 FIVE WIRE LEADS SHOULD BE COLOURED MARKED BLUE 7/8 THE WHITE WIRE SHOULD BE COLOURED MARKED RED

TEST POINT TERMINAL 620007 21 OF

3-WAY 1-PCB PLUS 604046 6 6047 FIT 2-WAY 1-PCB SHORTING UNIT 605127 IN POSITIONS J M N P R AND T 6 604

DC CLAMP ASSY 4000066



SOLENER TURRET 620006 10 OF

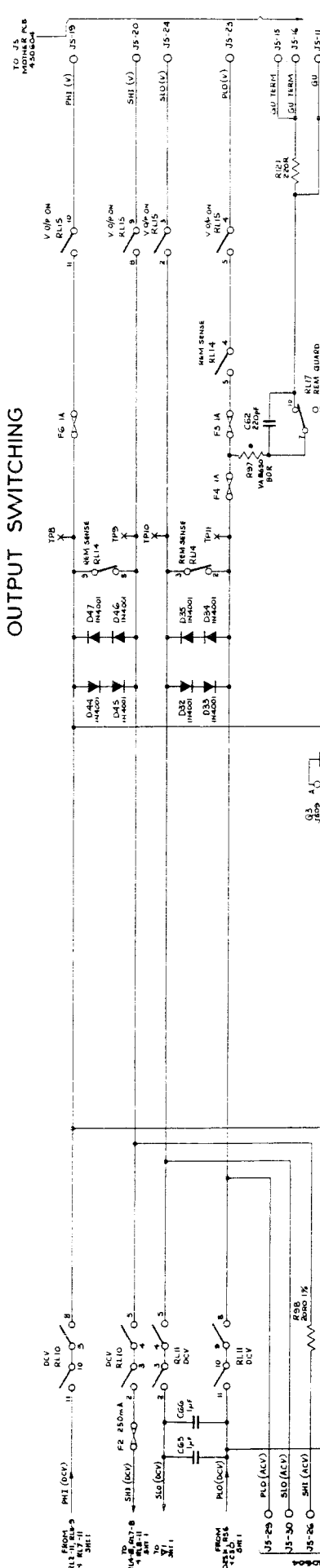
SECURE WIRES TO PCB USING LACING CORD 410008-2 590007

NB KEEP SOLDER JOIN AS CLOSE TO GLASS CAP BODY AS POSSIBLE SLEEVE 590004 PCB ASSY OF C64/C68

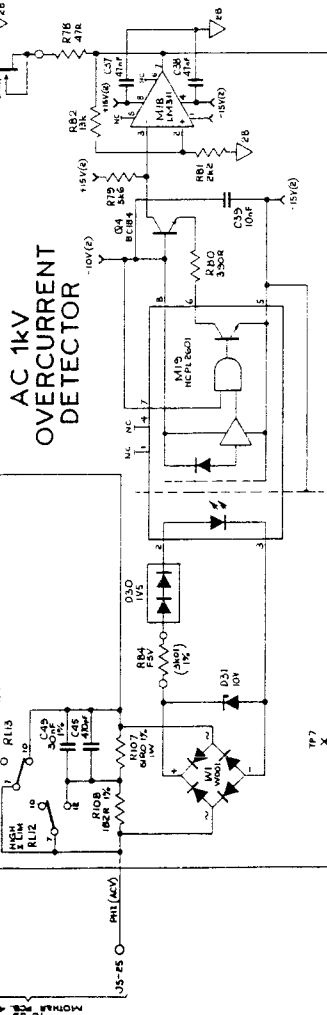
TEST POINT TERMINAL 620007 21 OF

DC CLAMP ASSY 4000066

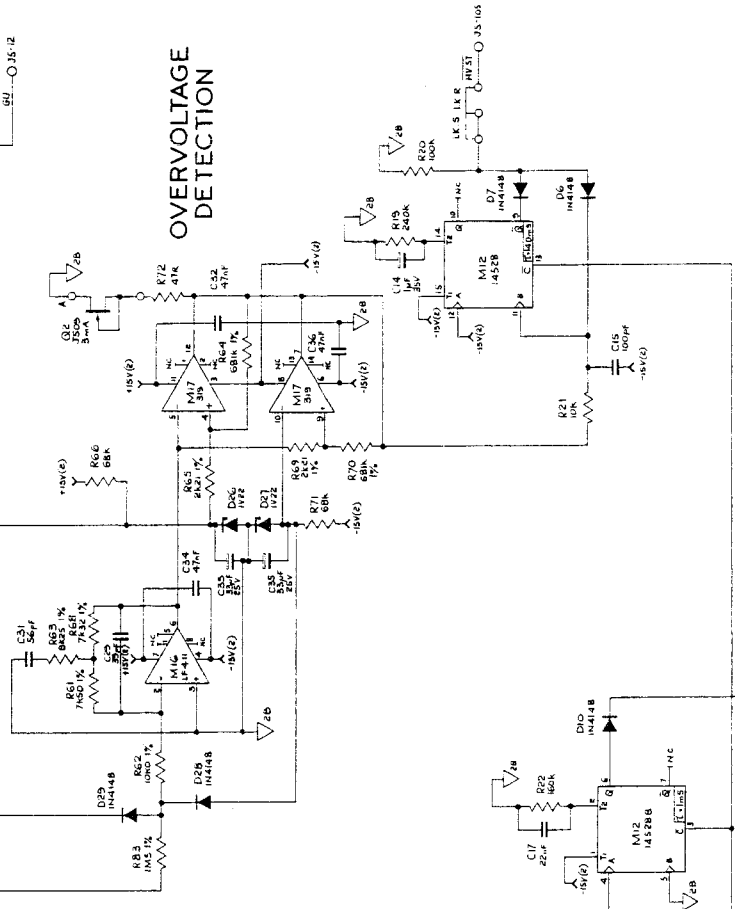
OUTPUT SWITCHING



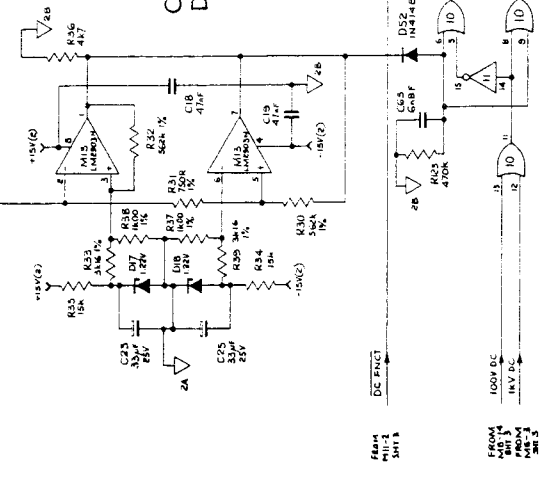
AC 1kV OVERCURRENT DETECTOR



OVERVOLTAGE DETECTION



DC OVERCURRENT DETECTOR



DC ASSEMBLY
Output Switching and Overload Sense
Circuit Diagram No. 430536-4.0 Sheet 2

| MOUNTING I.C.S. | | |
|-----------------|--------|------|
| WIRE | PART # | WIRE |
| 8 | 605055 | 5 |
| 14 | 605060 | 6 |
| 16 | 605061 | 3 |
| 20 | 605070 | 3 |

MOUNT THE FOLLOWING COMPONENTS ON LARGE CERAMIC BEADS 600024, 2 PER LEAD. R15, R16, R17, R18, R19, R20, R21, R22. THE FOLLOWING COMPONENTS TO BE MOUNTED ON SMALL CERAMIC BEADS 600006, 1 PER LEAD. D4, D5, D6, D11, D12, D13, D14, D15, D16, D17, D18, D19, D20, D21, D22, D23, D24, D25, D26, D27, D28, D29, D30, D31, D32, D33, D34, D35, D36, D37, D38, D39, D40, D41, D42, D43, D44, D45, D46, D47, D48, D49, D50, D51, D52, D53, D54, D55, D56, D57, D58, D59, D60, D61, D62, D63, D64, D65, D66, D67, D68, D69, D70, D71, D72, D73, D74, D75, D76, D77, D78, D79, D80, D81, D82, D83, D84, D85, D86, D87, D88, D89, D90, D91, D92, D93, D94, D95, D96, D97, D98, D99, D100.

THE FOLLOWING COMPONENTS TO BE MOUNTED ON SMALL CERAMIC BEADS 600006, 1 PER LEAD. R85, R108, C95, 2 PER LEAD.

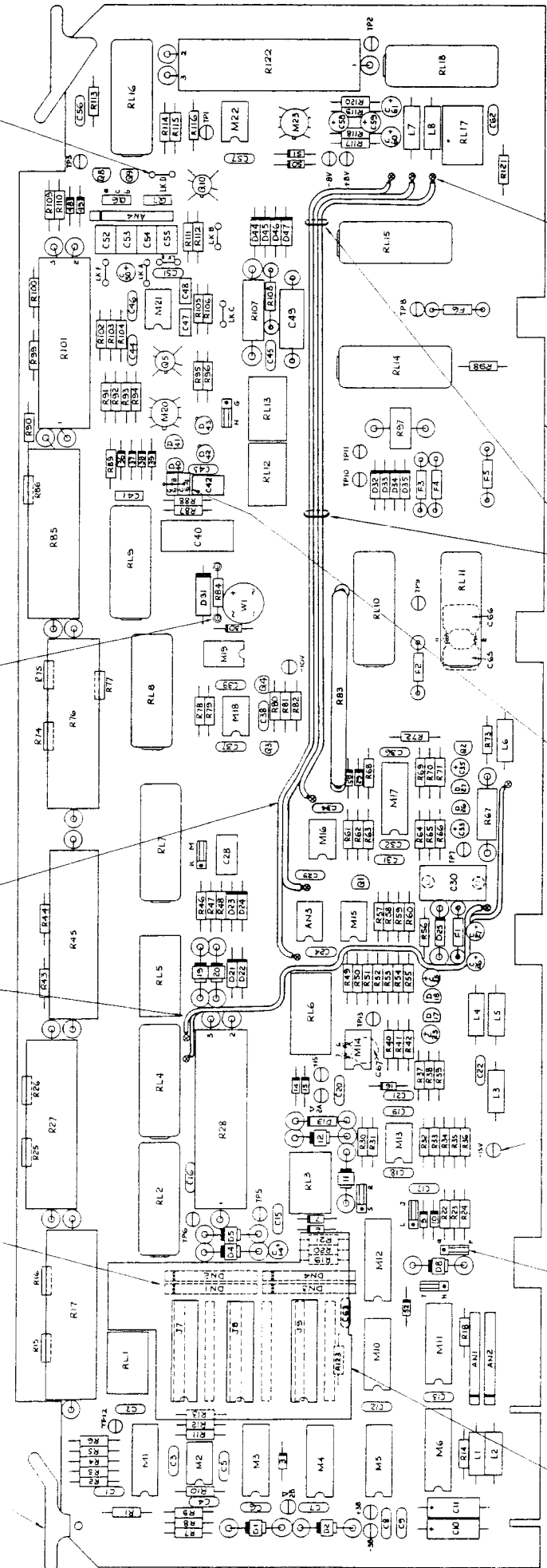
N.B. CLASS BEAD 600045 FITTED TO EACH LEG OF THE FOLLOWING COMPONENTS - R15, R16, R17, R18, R19, R20, R21, R22.

CIRCUIT BOARD SELECTOR (ORANGE)

MOUNT R84 ON FSV TERMINALS 600200, 2 PER

NB D11 AND D13 SHOULD BE COLORED MARKED BUT D11 AND D13 SHOULD BE COLORED MARKED BUT 7/2 FILL WHITE WIRE 510059

MAKE WIRE LINKS FROM 22 SWG B.T.C. WIRE 540000



3 WAY 17 PCB PLUG 600046 6WY FIT 2 WAY 77 SHORING JACK 600027 IN POSITIONS J1 N P R AND T 609

DC CLAMP ASSY 400066

TEST POINT TERMINAL 600007 21 PER

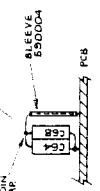
NB KEEP SOLDER JOINTS CLEAN AND SOLDER BRIDGE AS POSSIBLE

3 WAY 17 PCB PLUG 600046 6WY FIT 2 WAY 77 SHORING JACK 600027 IN POSITIONS J1 N P R AND T 609

SECURE WIRES TO PCB USING LACING WIRE 550007

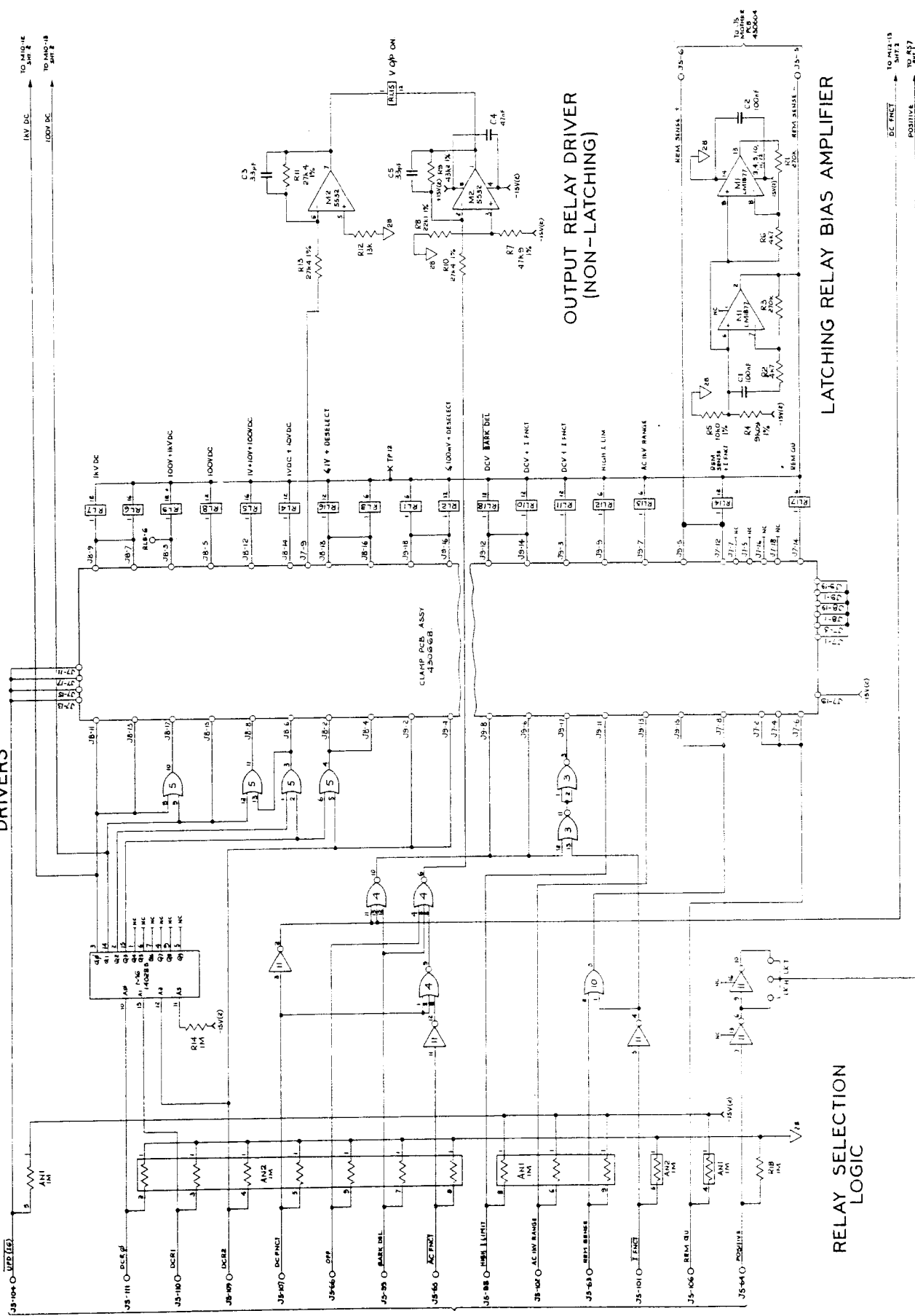
SOLDER TURRET 600006 10 PER

MAKE WIRE LINKS FROM 22 SWG B.T.C. WIRE 540000



ASSY OF C64/C66

TRI-STATE DRIVERS



LATCHING RELAY BIAS AMPLIFIER

OUTPUT RELAY DRIVER
 (NON-LATCHING)

RELAY SELECTION LOGIC

DC ASSEMBLY

N.B. CLASS READ 650043 FITTED TO EACH LEG OF
 PCB TO ALLOW CONNECTION TO 200V AC SUPPLY.
 PCB TO BE 400V RATED. USE CLASS 2 WIRE.

THE FOLLOWING COMPONENTS TO BE MOUNTED ON
 CERAMIC BEADS 650024, 2 PER LEAD.
 R17, R27, R28, R45, R76, R85, R101, R107, R122.
 ALSO ON LARGE BEADS, 1 PER LEAD.
 R1, R2, R3, R4, R5, R6, R7, R8, R9, R10, R11, R12, R13, R14, R15, R16, R18, R19, R20, R21, R22, R23, R24, R25, R26, R29, R30, R31, R32, R33, R34, R35, R36, R37, R38, R39, R40, R41, R42, R43, R44, R46, R47, R48, R49, R50, R51, R52, R53, R54, R55, R56, R57, R58, R59, R60, R61, R62, R63, R64, R65, R66, R67, R68, R69, R70, R71, R72, R73, R74, R75, R77, R78, R79, R80, R81, R82, R83, R84, R85, R86, R87, R88, R89, R90, R91, R92, R93, R94, R95, R96, R97, R98, R99, R100, R102, R103, R104, R105, R106, R108, R109, R110, R111, R112, R113, R114, R115, R116, R117, R118, R119, R120, R121, R123, R124, R125, R126, R127, R128, R129, R130, R131, R132, R133, R134, R135, R136, R137, R138, R139, R140, R141, R142, R143, R144, R145, R146, R147, R148, R149, R150, R151, R152, R153, R154, R155, R156, R157, R158, R159, R160, R161, R162, R163, R164, R165, R166, R167, R168, R169, R170, R171, R172, R173, R174, R175, R176, R177, R178, R179, R180, R181, R182, R183, R184, R185, R186, R187, R188, R189, R190, R191, R192, R193, R194, R195, R196, R197, R198, R199, R200.

MOUNT THE FOLLOWING COMPONENTS ON
 CERAMIC BEADS 650024, 2 PER LEAD.
 R17, R27, R28, R45, R76, R85, R101, R107, R122.
 ALSO ON LARGE BEADS, 1 PER LEAD.
 R1, R2, R3, R4, R5, R6, R7, R8, R9, R10, R11, R12, R13, R14, R15, R16, R18, R19, R20, R21, R22, R23, R24, R25, R26, R29, R30, R31, R32, R33, R34, R35, R36, R37, R38, R39, R40, R41, R42, R43, R44, R46, R47, R48, R49, R50, R51, R52, R53, R54, R55, R56, R57, R58, R59, R60, R61, R62, R63, R64, R65, R66, R67, R68, R69, R70, R71, R72, R73, R74, R75, R77, R78, R79, R80, R81, R82, R83, R84, R85, R86, R87, R88, R89, R90, R91, R92, R93, R94, R95, R96, R97, R98, R99, R100.

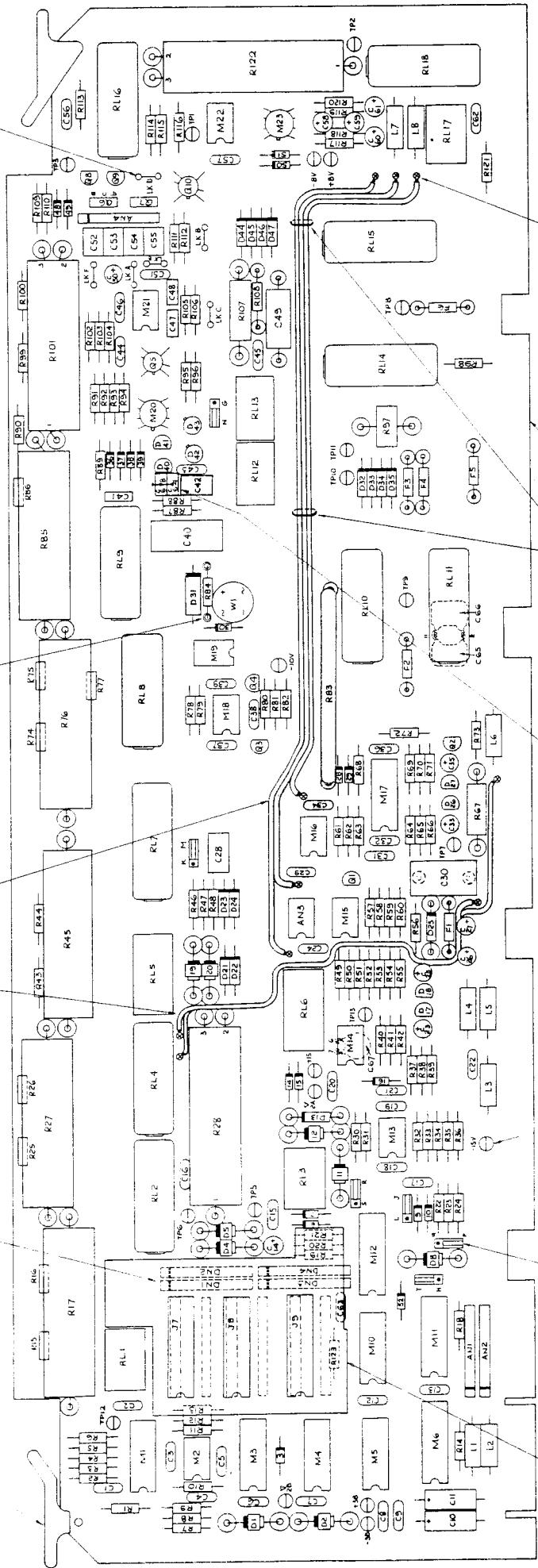
| MOUNTING I.C.3 | |
|----------------|--------|
| P# | WATS |
| 1 | 605059 |
| 2 | 605060 |
| 3 | 605061 |
| 4 | 605062 |
| 5 | 605063 |
| 6 | 605064 |
| 7 | 605065 |
| 8 | 605066 |
| 9 | 605067 |
| 10 | 605068 |
| 11 | 605069 |
| 12 | 605070 |
| 13 | 605071 |
| 14 | 605072 |
| 15 | 605073 |
| 16 | 605074 |
| 17 | 605075 |
| 18 | 605076 |
| 19 | 605077 |
| 20 | 605078 |

CONNECT BOARD ELEMENTS (CHANGE)
 650043, 2 PER

N.B. USE RED WIRE SHOULD BE COLOUR MARKED RED
 1/2" 7/8" WHITE WIRE SHOULD BE COLOUR MARKED RED

MOUNT R84 ON PSY TERMINALS
 650007, 2 PER

MAKE LINKS 1/4" 1/8" 450M
 250006, 1 PER



3 WAY 1" PCB PLUS 650046, 6 PER
 IN POSITIONS J, M, P, R AND T, 6.0H

DC CLAMP ASSY
 400566

TEST POINT TERMINAL
 650007, 21 PER

N.B. USE FOLDED WIRE
 AS CLOSE TO BOARD AS
 POSSIBLE

BLEEVE
 650004

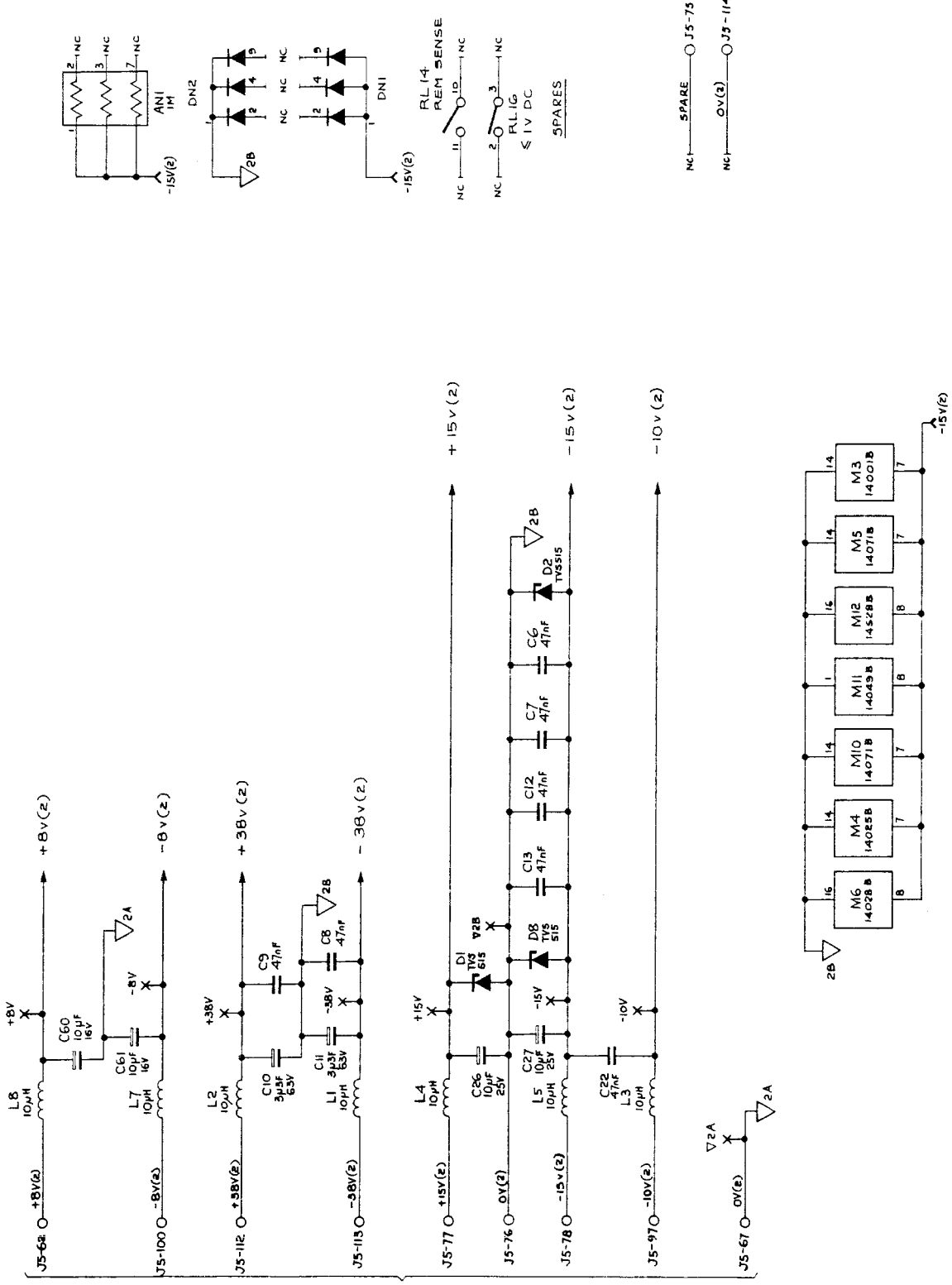
ASSY OF C64/C65

SOLDER TURRET
 650006, 10 PER

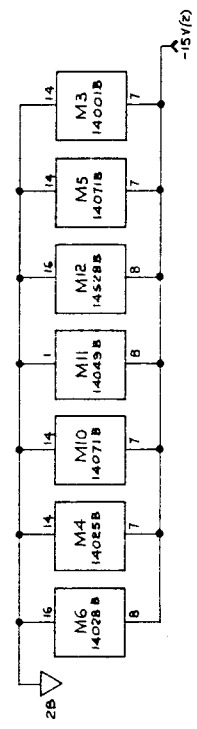
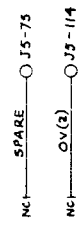
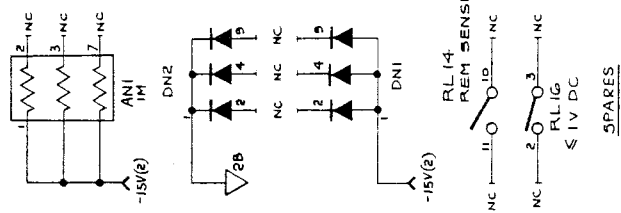
PCB
 410558-2

SECURE WIRE TO PCB
 USING LACING CORE
 650007

ASSY OF C64/C65



TO J5
MOTHER
PCB.
430604

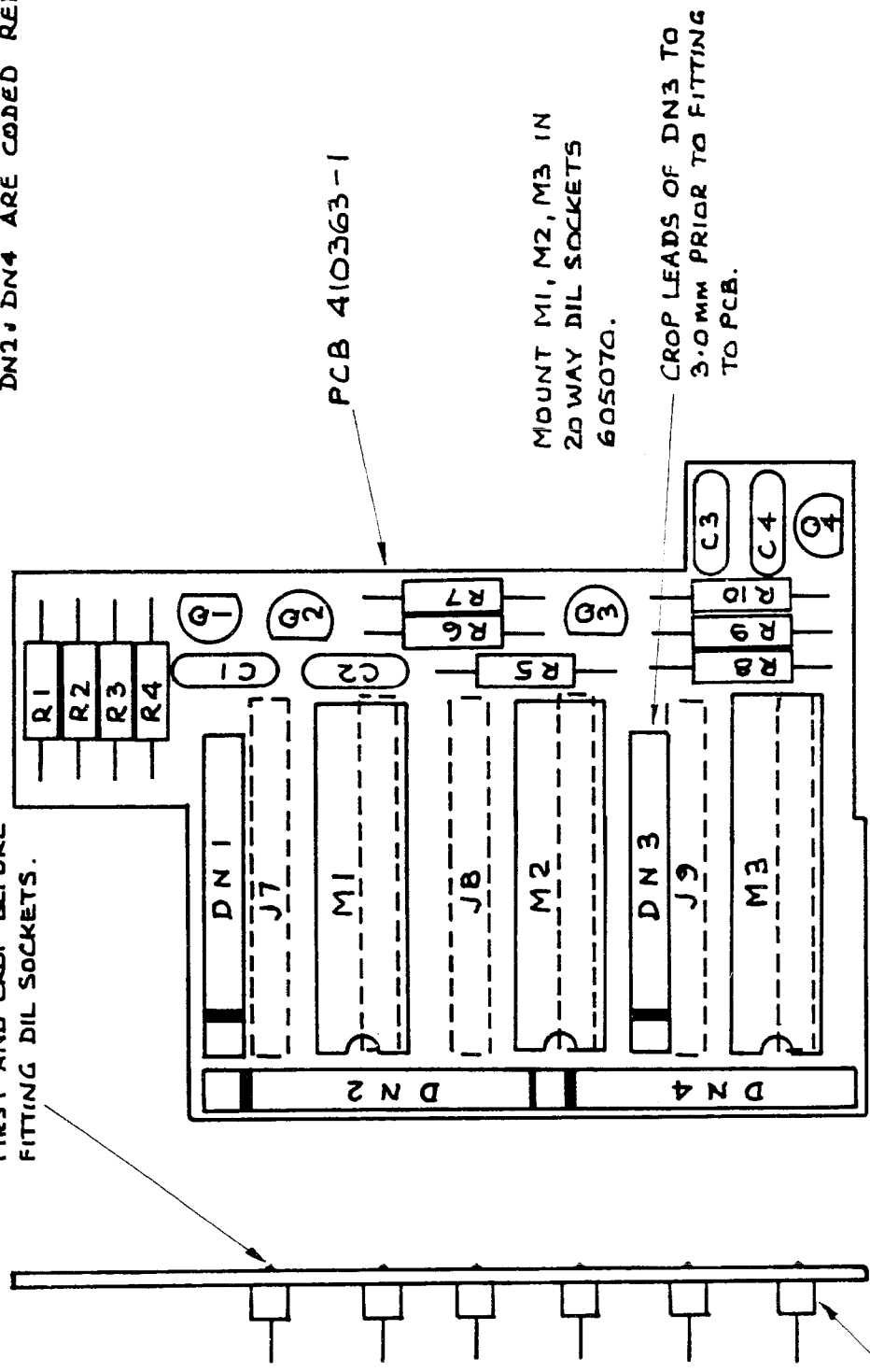


DC ASSEMBLY
Power Supplies

DC CLAMP ASSEMBLY

NOTE. DN1 & DN3 ARE CODED BLUE
DN2 & DN4 ARE CODED RED

N.B. FIT HEADER PLUGS
FIRST AND CROP BEFORE
FITTING DIL SOCKETS.



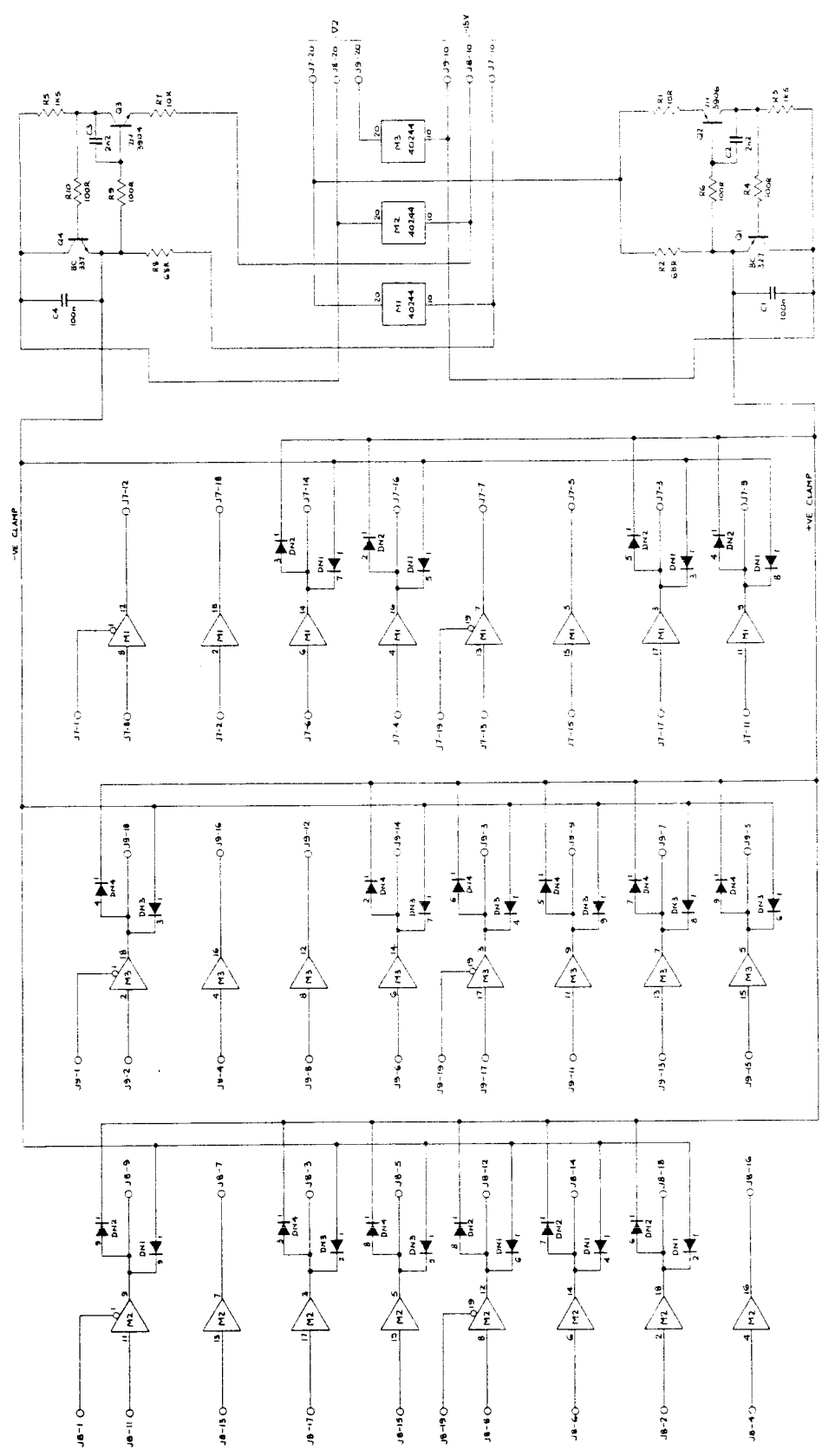
PCB 410363-1

MOUNT M1, M2, M3 IN
20 WAY DIL SOCKETS
605070.

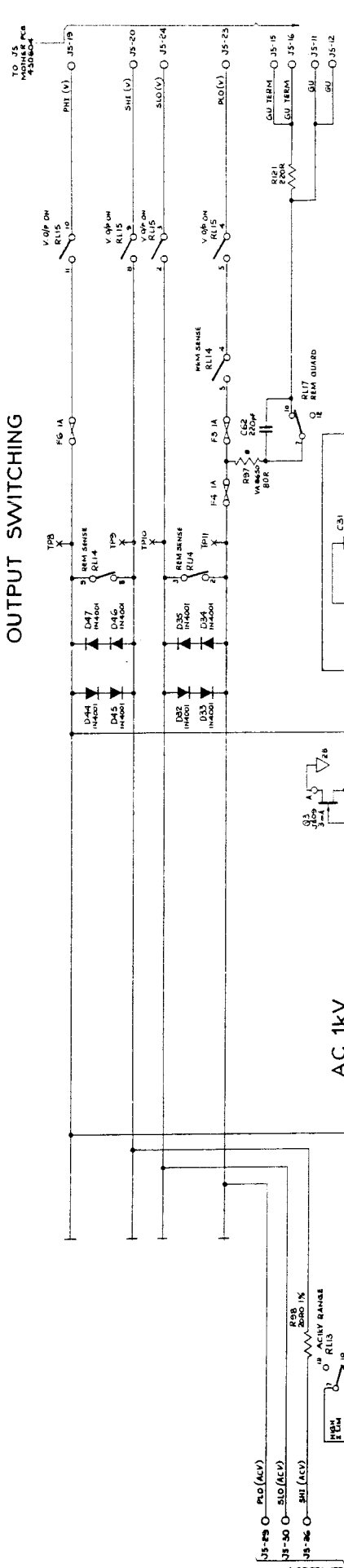
CROP LEADS OF DN3 TO
3.0MM PRIOR TO FITTING
TO PCB.

MAKE HEADER PLUGS
FROM 604057 (6 OFF)

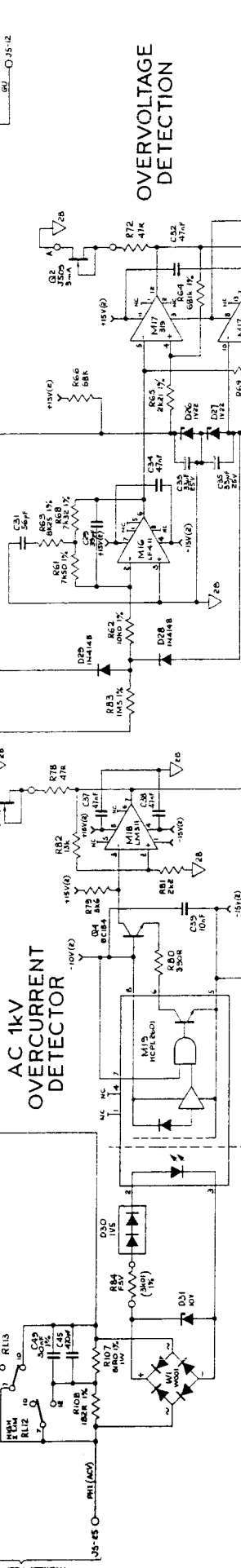
DN1 AND DN3 ARE CA-1N4148
 DN2 AND DN4 ARE CC-1N4148



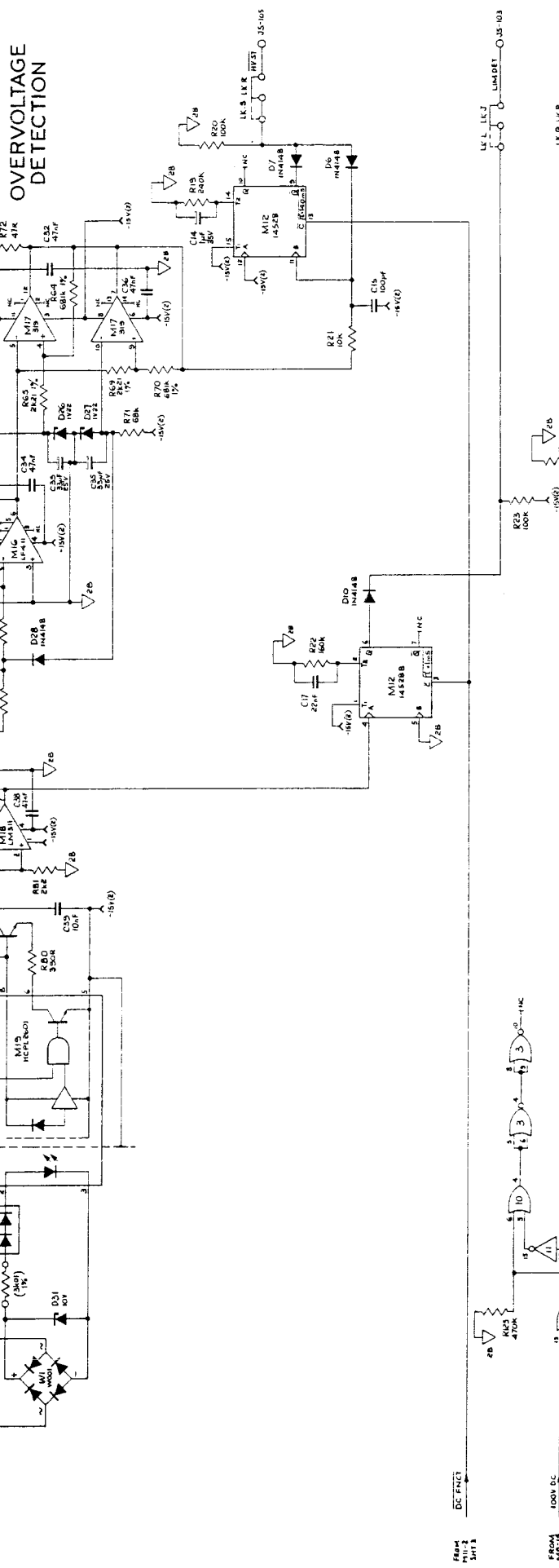
OUTPUT SWITCHING



AC 1kV OVERCURRENT DETECTOR



OVERVOLTAGE DETECTION



OUTPUT CONTROL ASSEMBLY

Output Switching and Overload Sense



OUTPUT CONTROL ASSEMBLY

N.B. CLASS READ BEADS FITTED TO PINS 15, 16, 17 OF THE FOLLOWING BEAD CARTRIDGES:
C33, C34, C35, C36, C37, C38, C39, C40, C41, C42, C43, C44, C45, C46, C47, C48, C49, C50, C51, C52, C53, C54, C55, C56, C57, C58, C59, C60, C61, C62, C63, C64, C65, C66, C67, C68, C69, C70, C71, C72, C73, C74, C75, C76, C77, C78, C79, C80, C81, C82, C83, C84, C85, C86, C87, C88, C89, C90, C91, C92, C93, C94, C95, C96, C97, C98, C99, C100.

THE FOLLOWING COMPONENTS TO BE MOUNTED ON SMALL CERAMIC BEAD CARTRIDGES:
R83, R108, C43, 2 PER LEAD

MOUNT THE FOLLOWING COMPONENTS ON CERAMIC BEAD CARTRIDGE 1, 2 PER LEAD:
R107

THE FOLLOWING COMPONENTS TO BE MOUNTED ALSO ON LARGE BEADS, 1 PER LEAD, DI D8 D8 R97

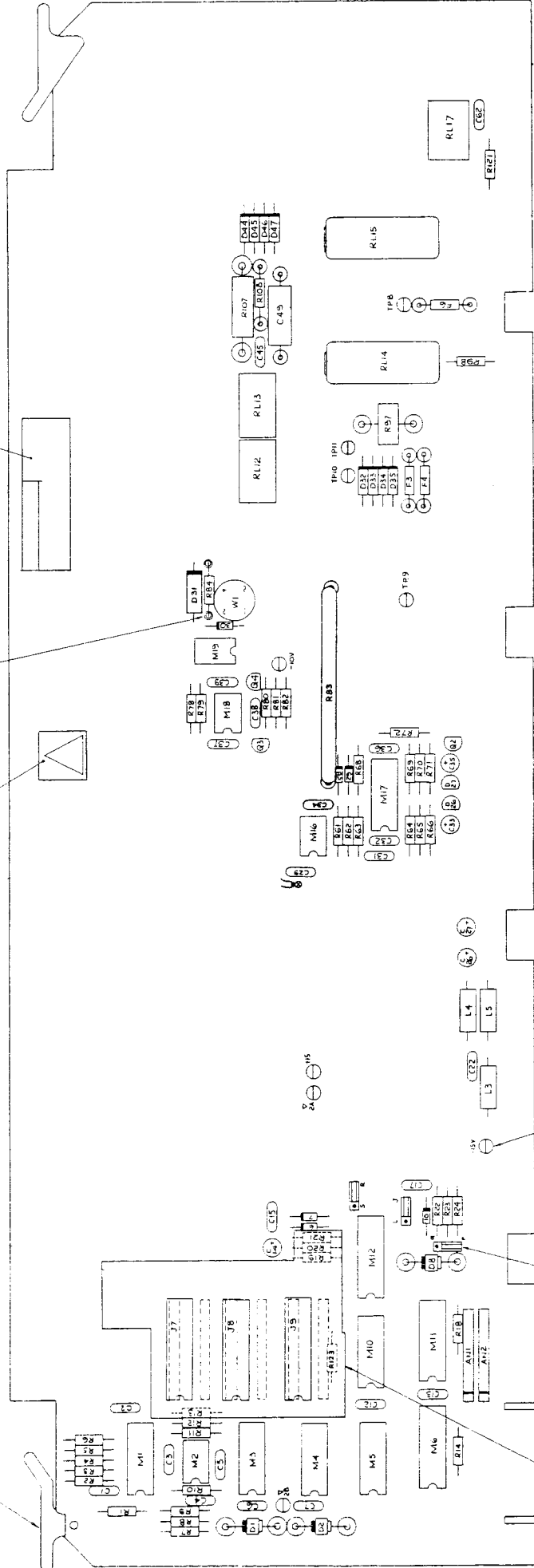
| MOUNTING ICs | | |
|--------------|-------------|---------------|
| IC PART NO. | IC PART NO. | USED TO MOUNT |
| 8 | 605055 | 4 |
| 14 | 605060 | 6 |
| 16 | 605061 | 3 |
| 20 | 605010 | 3 |

SSD LABEL
42012-1

MOUNT K84 ON FSV TERMINALS
605001, 2 WFT

SERIAL N° LABEL
420098

CIRCUIT BOARD ELECTRON (ORANGE)
605005, 2 WFT



PCB
410258-2

TEST POINT TERMINAL
605001, 7 60

3 WAY 1 PCB PLUG 608046 6 WFT
FIT 2 WAY 1 SHORTING STRIP 605127
IN POSITIONS J7 IN P.H. AND 1-3 ON

DC CLAMP ASSY
400668

OUTPUT CONTROL ASSEMBLY

MOUNT THE FOLLOWING COMPONENTS ON LARGE CERAMIC BEADS 650024, 2 PER LEAD. LARGE R107.

THE FOLLOWING COMPONENTS TO BE MOUNTED ALSO ON CERAMIC BEADS: 1 PER LEAD: D1 D2 D8 R97

MOUNT THE FOLLOWING COMPONENTS TO EACH LEG OF SMALL CERAMIC BEADS 650024, 2 PER LEAD.

THE FOLLOWING COMPONENTS TO BE MOUNTED ON CERAMIC BEADS: 1 PER LEAD: R83, R108, C49, 2 PER LEAD.

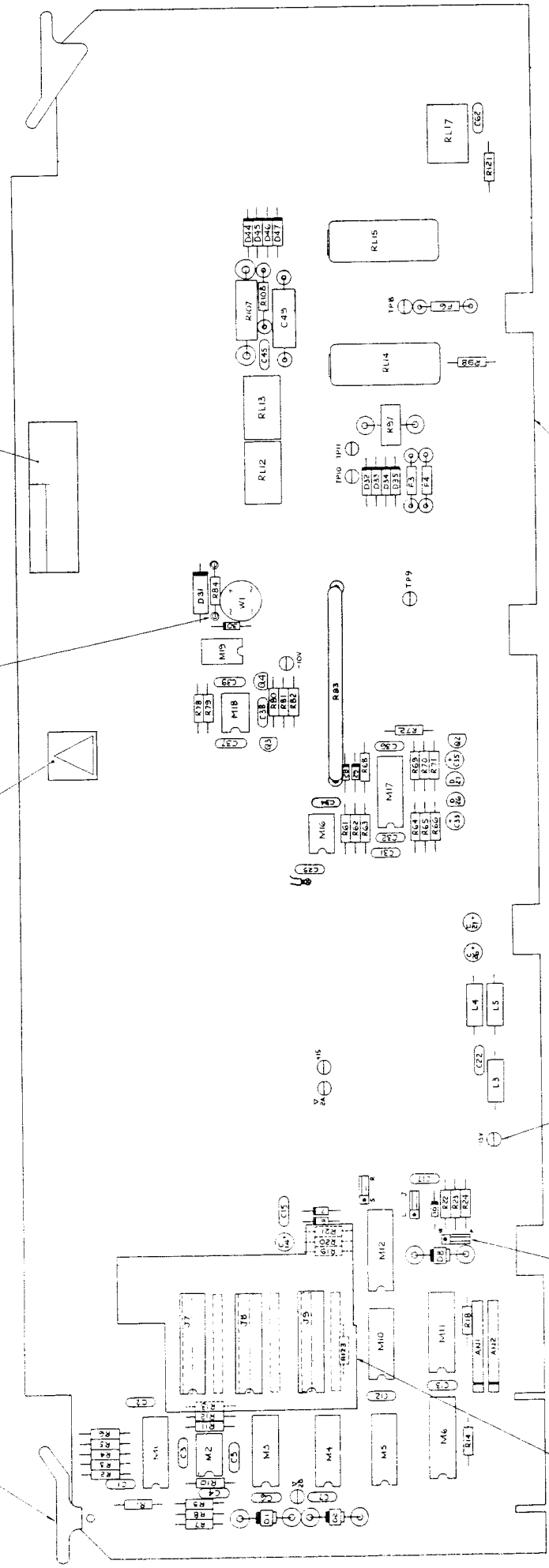
| MOUNTING JCS | | |
|--------------|---------|----------------|
| NP WAYS | PART NO | USED TO MOUNT |
| 8 | 650055 | M2 16 18 19 |
| 14 | 650060 | M1 3 4 5 10 11 |
| 16 | 650061 | M4 11 12 |
| 20 | 650070 | M3 7 8 5 |

CIRCUIT BOARD REFLECTION (CHANGE) 650115, 2 PER

S&D LABEL 422012

MOUNT R84 ON FSV TERMINALS 652001, 2 PER

SERIAL NO LABEL 420058

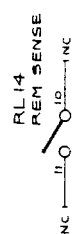
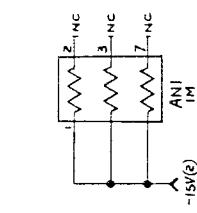
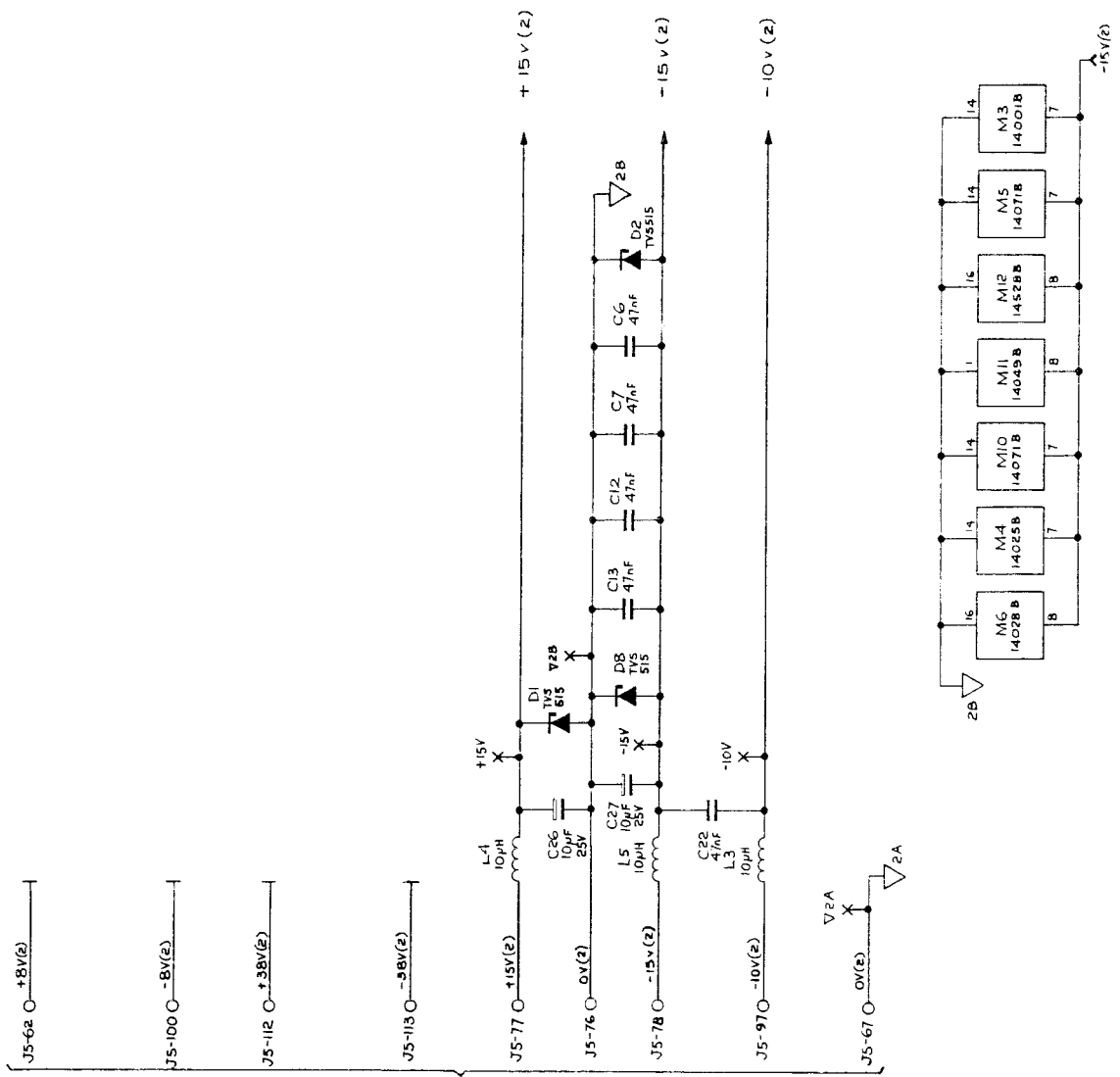


DC CLAMP ASSY 400666

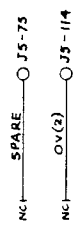
3 WAY J1, J6, J15, J16, 650046, 6 PER
PIT 2 WAY J11, SHORTING SW1, 650127
IN POSITIONS J1 M N P AND 1, 3 PER

TEST POINT TERMINAL 652007, 7 PER

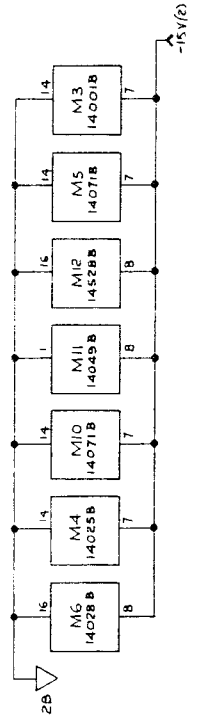
PCB 410255-2



SPARES



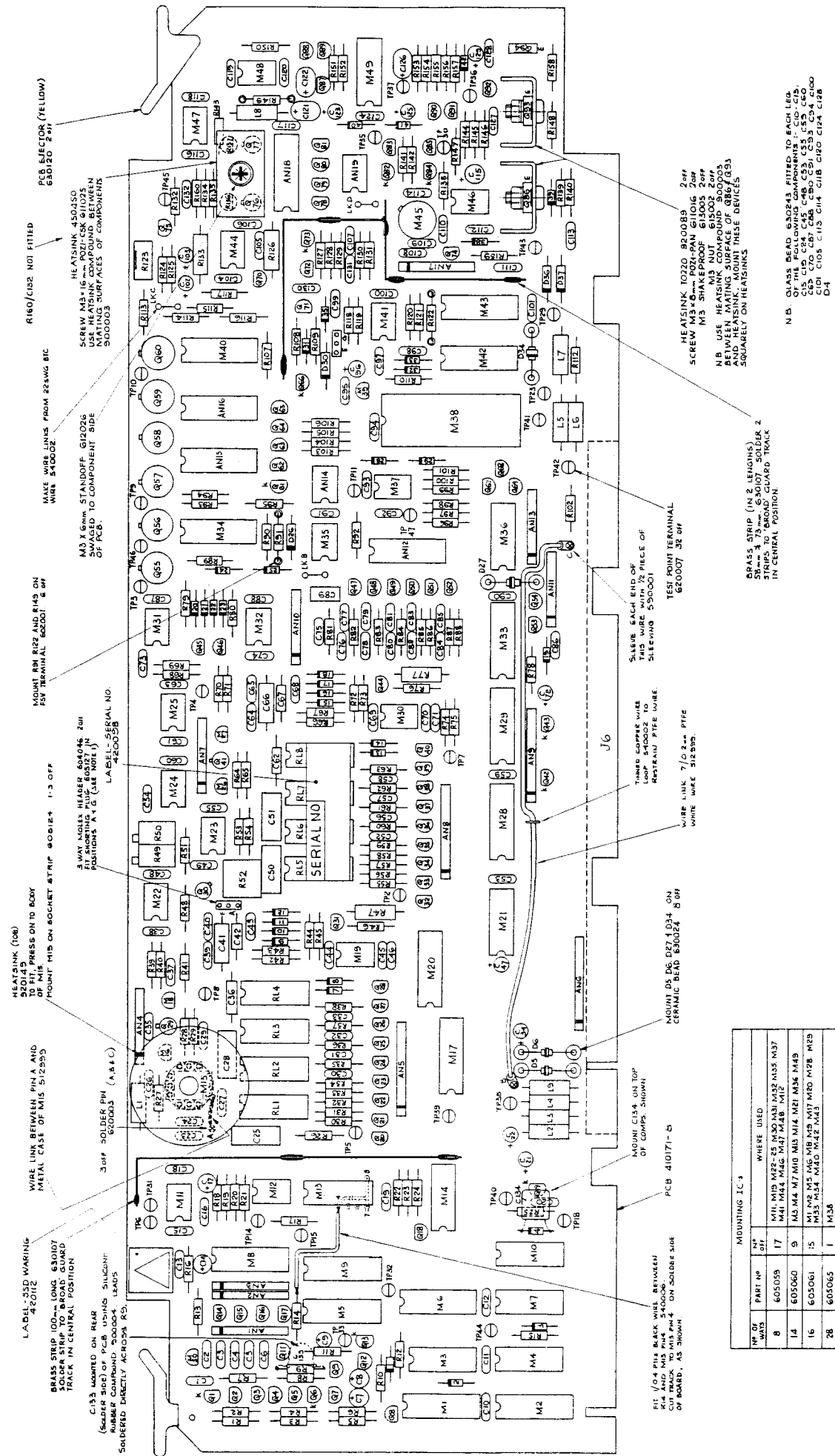
TO JS
 MOTHER
 PCB
 430604



OUTPUT CONTROL ASSEMBLY
 Power Supplies
 Circuit Diagram No. DC400909-1.0 Sheet 3

SINE SOURCE ASSEMBLY

NOTE: RT LINK 'E' AND LINK 'F' IN P
LINK 'A' AND LINK 'G' FOR T



HEATSINK (106)
250149
TO FIT, PRESS ON TO BODY
OF M18. M18 ON SOCKET STRIP
POINT MID ON SOCKET STRIP
420058

WIRE LINK BETWEEN PIN A AND
METAL CASE OF M15 512953

LABEL - 3SD MARKING
BRASS STRIP 0.004" LONG 630127
ON BOARD IN CENTRAL POSITION

C133 MOUNTED ON REAR
(SOLDER SIDE) OF PCB USING SILICONE
RUBBER COMPOUND 900004. LEADS
SOLDERED DIRECTLY ACROSS R5.

3-WAY MOLEX HEADER 604046 201
POSITIONS 'A', 'G' (SEE NOTE J)
LABEL - SERIAL NO.
420058

MOUNT R21, R22 AND R45 ON
TSV TERMINAL 600001 5 OHM
WIRE 540002

M3 X 0.6mm STANDOFF G12026
SWAGED TO COMPONENT SIDE
OF PCB.
900003

HEATSINK 450150
USE HEATSINK COMPOUND BETWEEN
SURFACES OF COMPONENTS
900003

PCB SECTOR (YELLOW)
630128 2 OHM

MAKE WIRE LINKS FROM 22AWG BIC
WIRE 540002

HEATSINK 10220 920089
SCREW M3 X 0.6mm 600100 20mm
M3 SHIM 615002 20mm
M3 NUT 615002 20mm
NB USE HEATSINK COMPOUND 900003
BETWEEN SURFACES OF 900107, 931
AND HEATSINK MOUNT THESE DEVICES
SQUARELY ON HEATSINKS

WIRE LINK 7/0 2mm PTFE
WHITE WIRE 512953

THINNE COPPER WIRE
LOOP 500002 TO
RESTRAIN PIPE JOINT

SLICER EACH END OF
THIS WIRE TO PRICE OF
SLEEPING 550001

TEST POINT TERMINAL
600007 3E OHM

WIRE LINK 7/0 2mm PTFE
WHITE WIRE 512953

MOUNT C154 ON TOP
OF COMPS. SHOWN

PCB 410711- 5

WIRE LINK 7/0 2mm PTFE
WHITE WIRE 512953

WIRE LINK 7/0 2mm PTFE
WHITE WIRE 512953

WIRE LINK 7/0 2mm PTFE
WHITE WIRE 512953

WIRE LINK 7/0 2mm PTFE
WHITE WIRE 512953

WIRE LINK 7/0 2mm PTFE
WHITE WIRE 512953

WIRE LINK 7/0 2mm PTFE
WHITE WIRE 512953

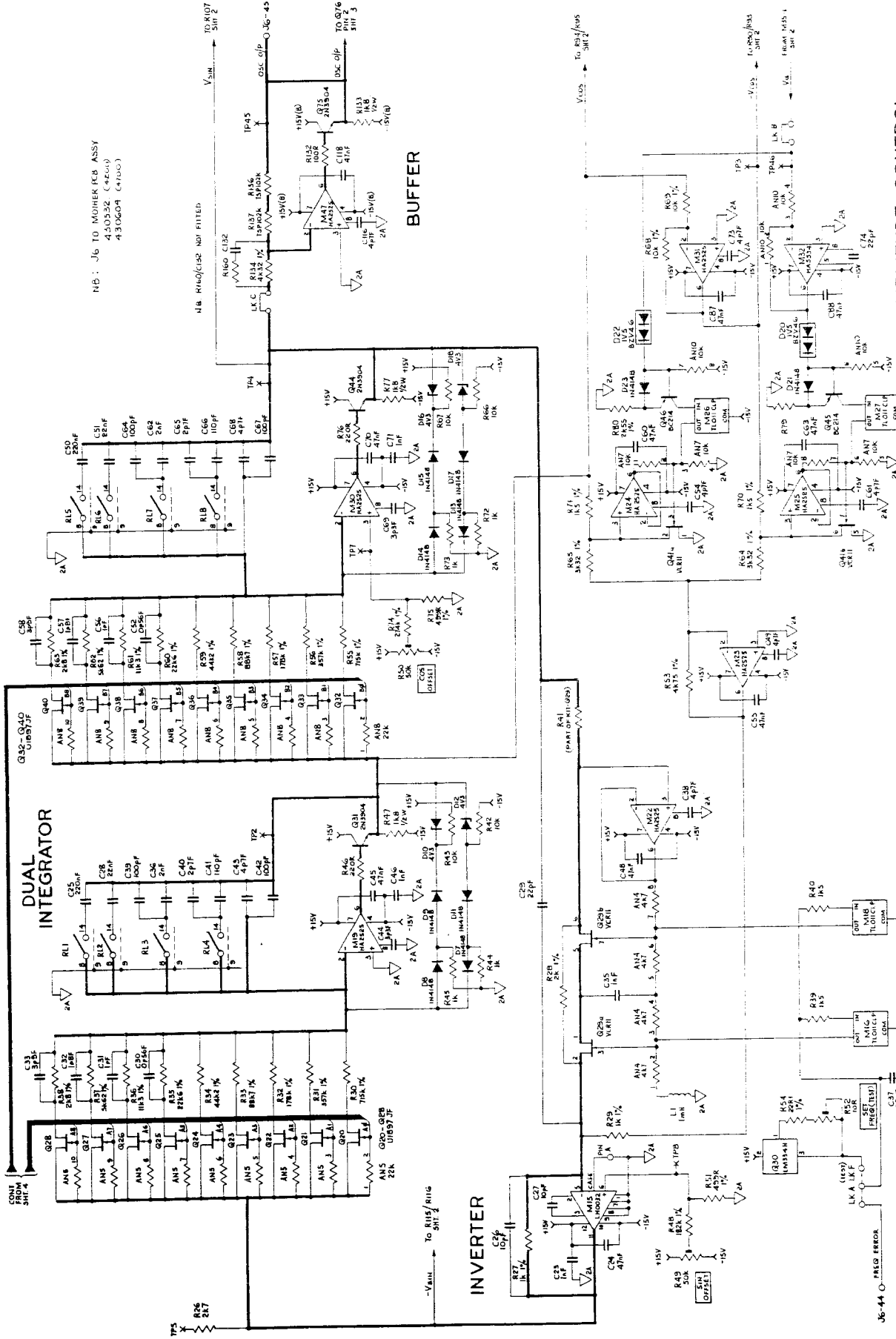
WIRE LINK 7/0 2mm PTFE
WHITE WIRE 512953

WIRE LINK 7/0 2mm PTFE
WHITE WIRE 512953

1/16" PHX BRASS WIRE BETWEEN
R14 AND M15 PH4 540026
CUT TRACK TO M15 PH4 ON SOLDER SIDE
OF BOARD. AS SHOWN

| MOUNTING IC 3 | | |
|---------------|-------------------------------------|--|
| PT | WHERE USED | |
| 17 | M11 M15 M22 2E 2A20 M31 M32 M33 M37 | |
| 8 | M41 M44 M45 M47 M48 M12 | |
| 14 | M3 M4 47 M10 M13 M14 M21 M36 M49 | |
| 16 | M1 M2 M5 M6 M9 M16 M17 M20 M28 M29 | |
| 28 | M33 M34 M40 M42 M43 | |

N.B. Q1A35 BEAD 630264 PLACED ON EACH LEG
C15 C19 C24 C45 C48 C53 C55 C56 C60
C67 C71 C87 C88 C93 C95 C96 C100
C101 C105 C115 C118 C119 C120 C124 C128
D-4



AMPLITUDE CONTROL
SINE SOURCE ASSEMBLY

Sine Oscillator

FREQUENCY CONTROL

HD: J6 TO MOHREK PCB ASSY
4300322 (REV.0)
4300604 (REV.0)

TO Q17
PIN 2
SH 2

OSC O/P
TO Q16
PIN 2
SH 3

TO Q33/Q35
SH 2

TO Q17
PIN 2
SH 2

TO Q17
PIN 2
SH 2

TO Q17
PIN 2
SH 2

TO Q17
PIN 2
SH 2

TO Q17
PIN 2
SH 2

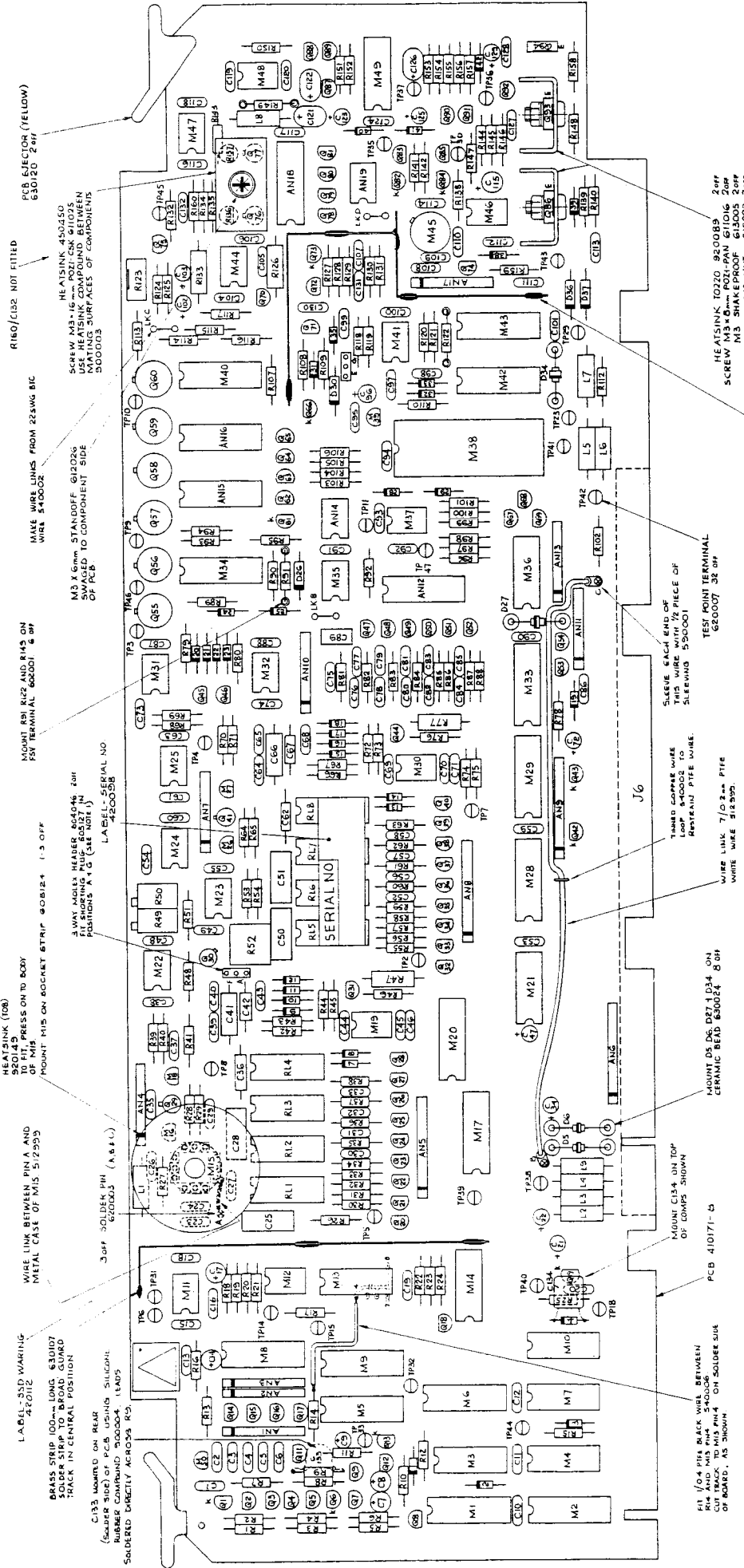
TO Q17
PIN 2
SH 2

TO Q17
PIN 2
SH 2

TO Q17
PIN 2
SH 2

SINE SOURCE ASSEMBLY

NOTE: FIT LINK P AND LINK F IN P LINK A AND LINK G FOR 1



HEAT SINK (TOB)
9200B 2 off
PRESS ON TO BODY
OF M15
MOUNT THIS ON SOCKET STRIP 608124 1-3 OFF

WIRE LINK BETWEEN PIN A AND METAL CASE OF M15 512955
MOUNT THIS ON SOCKET STRIP 608124 1-3 OFF

WIRE LINK (IN 8 LEADS) STRIPS TO "BROAD" GUARD TRACK IN CENTRAL POSITION

HEAT SINK TOZZO 9200B 2 off
SCREW M3x0.6mm POSITION 61006 2 off
M3 NUT 615002 2 off
N.B. USE HEAT SINK COMPOUND 800003 AND HEAT SINK MOUNT THESE DEVICES SQUARELY ON HEAT SINKS

HEAT SINK TOZZO 9200B 2 off
SCREW M3x0.6mm POSITION 61006 2 off
M3 NUT 615002 2 off
N.B. USE HEAT SINK COMPOUND 800003 AND HEAT SINK MOUNT THESE DEVICES SQUARELY ON HEAT SINKS

HEAT SINK TOZZO 9200B 2 off
SCREW M3x0.6mm POSITION 61006 2 off
M3 NUT 615002 2 off
N.B. USE HEAT SINK COMPOUND 800003 AND HEAT SINK MOUNT THESE DEVICES SQUARELY ON HEAT SINKS

HEAT SINK TOZZO 9200B 2 off
SCREW M3x0.6mm POSITION 61006 2 off
M3 NUT 615002 2 off
N.B. USE HEAT SINK COMPOUND 800003 AND HEAT SINK MOUNT THESE DEVICES SQUARELY ON HEAT SINKS

HEAT SINK TOZZO 9200B 2 off
SCREW M3x0.6mm POSITION 61006 2 off
M3 NUT 615002 2 off
N.B. USE HEAT SINK COMPOUND 800003 AND HEAT SINK MOUNT THESE DEVICES SQUARELY ON HEAT SINKS

HEAT SINK TOZZO 9200B 2 off
SCREW M3x0.6mm POSITION 61006 2 off
M3 NUT 615002 2 off
N.B. USE HEAT SINK COMPOUND 800003 AND HEAT SINK MOUNT THESE DEVICES SQUARELY ON HEAT SINKS

HEAT SINK TOZZO 9200B 2 off
SCREW M3x0.6mm POSITION 61006 2 off
M3 NUT 615002 2 off
N.B. USE HEAT SINK COMPOUND 800003 AND HEAT SINK MOUNT THESE DEVICES SQUARELY ON HEAT SINKS

HEAT SINK TOZZO 9200B 2 off
SCREW M3x0.6mm POSITION 61006 2 off
M3 NUT 615002 2 off
N.B. USE HEAT SINK COMPOUND 800003 AND HEAT SINK MOUNT THESE DEVICES SQUARELY ON HEAT SINKS

MOUNTING IC-4

| NO. OF WIRDS | PART NO. | WHERE USED |
|--------------|----------|---|
| 8 | 605059 | M11 M15 M22-25 M40 M41 M42 M43 M47 |
| 14 | 605060 | M41 M44 M46 M47 M48 M52 |
| 16 | 605061 | M3 M4 M7 M10 M13 M14 M21 M43 M49 |
| 28 | 605065 | M1 M2 M5 M6 M8 M9 M17 M20 M28 M29 M33 M34 M40 M42 M43 |

R1, 1/24. P14. P15. BACK WIRE BETWEEN R14 AND M13 PH4 540006 CUT TRACK TO M13 PH4 ON SOLDER SIDE OF BOARD. AS SHOWN

MOUNT D5, D6, D27 1 D34 ON CERAMIC BEAD 630024 8 OH

WIRE LINK 7/0.2mm PTFE TUBED COPPER WIRE LOOP 840002 TO RESTRAIN PTFE WIRE.

SLEEVE EACH END OF THIS WIRE WITH 1/2" PIECE OF SLEEVE 530001

TEST POINT TERMINAL 620007 38 OH

BRASS STRIP (IN 8 LEADS) STRIPS TO "BROAD" GUARD TRACK IN CENTRAL POSITION

MAKE WIRE LINKS FROM 22AWG BIC WIRE 840002

M3 1/8" STALDORF 610003 SPACED TO COMPONENT SIDE OF PCB

HEAT SINK 450065 SCREW M3x0.6mm POSITION 61006 USE HEAT SINK COMPOUND BETWEEN MATING SURFACES OF COMPONENTS 800003

PCB EJECTOR (YELLOW) 630120 2 PH

Instrument Serial Number

24824-6

This advice sheet applies only to the Instrument whose serial number is given above.

AC Outputs - Improvement to Frequency Control System

Section 11.6 contains the layout and circuit diagrams of the Sine Source Assembly.

This addendum changes pages 11.6-1 to 11.6-5, and associated component lists in Section 12, dealing with the introduction of an integrated VCO chip to replace the discrete VCO previously used, and modifications to the associated circuitry.

This upgrade improves the reliability and maintainability of the Digital Frequency Synthesizer by reducing the critical component count and easing fault diagnosis.

Contract No. F33659-90-C0065 specifies AC voltage (Option 20) and AC Current (Option 30) functions only. Therefore this addendum is pertinent to the contract

The above minor changes are detailed below.

Minor Revision

Amend the affected pages as follows:

| Section | Pages | Description | Action |
|---------|------------------------------|----------------------|---|
| 11 | 11.6-1) to) 11.6-5) | Sine Source Assembly | Delete the five pages, and substitute the attached five new pages 11.6-1 to 11.6-5 |
| 12 | 400446 Sheets 1-27 | Sine Source Assembly | Delete the 27 pages. Substitute the attached: LD400446-11.5 Sheet 1 and LP400446-11.5 Pages 1-12 |

Checked by:

Date:

22 Oct May '92



HEATSINK 450450
 SCREW M3x6mm
 MOUNTING SURFACES OF COMPONENTS
 MOUNTING SURFACES OF COMPONENTS
 5000003

R160, C27, C28, C44, C49,
 C51, C52, C73, C104,
 C107, C132 NOT FITTED

MAKE WIRE LINKS FROM 22AWG BIC
 WIRE 4100028

M3 X 6mm STANDOFF G10202
 SWAGED TO COMPONENT SIDE
 OF PCB

MOUNT R81, R105, R122 AND R145 ON
 P57 TERMINAL 6200101 5 0FF

3 WAY WIGGLER HEADER 404246 20FF
 MOUNTING SURFACES OF COMPONENTS
 MOUNTING SURFACES OF COMPONENTS
 4200558

NOTE 1. FIT LINK 'E' AND LINK 'F' IN PLACE OF
 LINK 'X' AND LINK 'G' FOR TEST

BRASS STRIP 100mm LONG 630107
 SOLDER STRIP TO BROAD GUARD
 TRACK IN CENTRAL POSITION

PCB EJECTOR (YELLOW)
 6501020 20FF

HEATSINK T0220 9200089 20FF
 SCREW M3x6mm P021-PAN G10106 20FF
 M3 SHAKEPROOF 6130053 20FF
 NB. USE HEATSINK MOUNTING SURFACES
 BETWEEN MOUNTING SURFACES OF Q867/Q893
 AND HEATSINK. MOUNT THESE DEVICES
 SQUARELY ON HEATSINKS

SOLDER PIN
 6200003 20FF

TEST POINT TERMINAL
 6200077 310FF

SLEEVE EACH END OF
 THIS WIRE WITH 7/8 PIECE OF
 SLEEVING 5900001

WIRE LINK 7/0 2mm PTFE
 WIRE WIRE 512595

MOUNT D8, D9, D17 & D34 ON
 CERAMIC BEAD 6300054 5 0FF

PCB 410171-1

M3 X 4mm STANDOFF 612004 400FF
 FIT TO SOLDER SIDE (NOT SHOWN)
 FIT SHIELD 450841 (USING
 M3 X 6mm SCREW P021-C5K G11007

BRASS STRIP (IN 8 INCHES)
 ON 2mm WIDE SOLDER STRIP
 STRIPS TO BROAD GUARD TRACK
 IN CENTRAL POSITION

PCB 410171-1

| MT. OF WAVE | PART NO. | WHERE USED |
|----------------|----------|---|
| B | 605039 | M18, M22, R4, M20, M1, M32, M35, M37 |
| 14 | 605060 | M41, M44, M40, M47, M48, M12, M15 |
| 16 | 605061 | M3, M4, M7, M10, M15, M16, M17, M18, M19 |
| 78 | 605065 | M2, M5, M6, M9, M11, M13, M14, M16, M17, M18, M19, M20, M21, M23, M24, M25, M26, M27, M28, M29, M30, M31, M32, M33, M34, M36, M38 |

* - NOT FITTED

NB: J6 TO MOMENT PCB ASSY
430532 (4200)
430609 (4700)

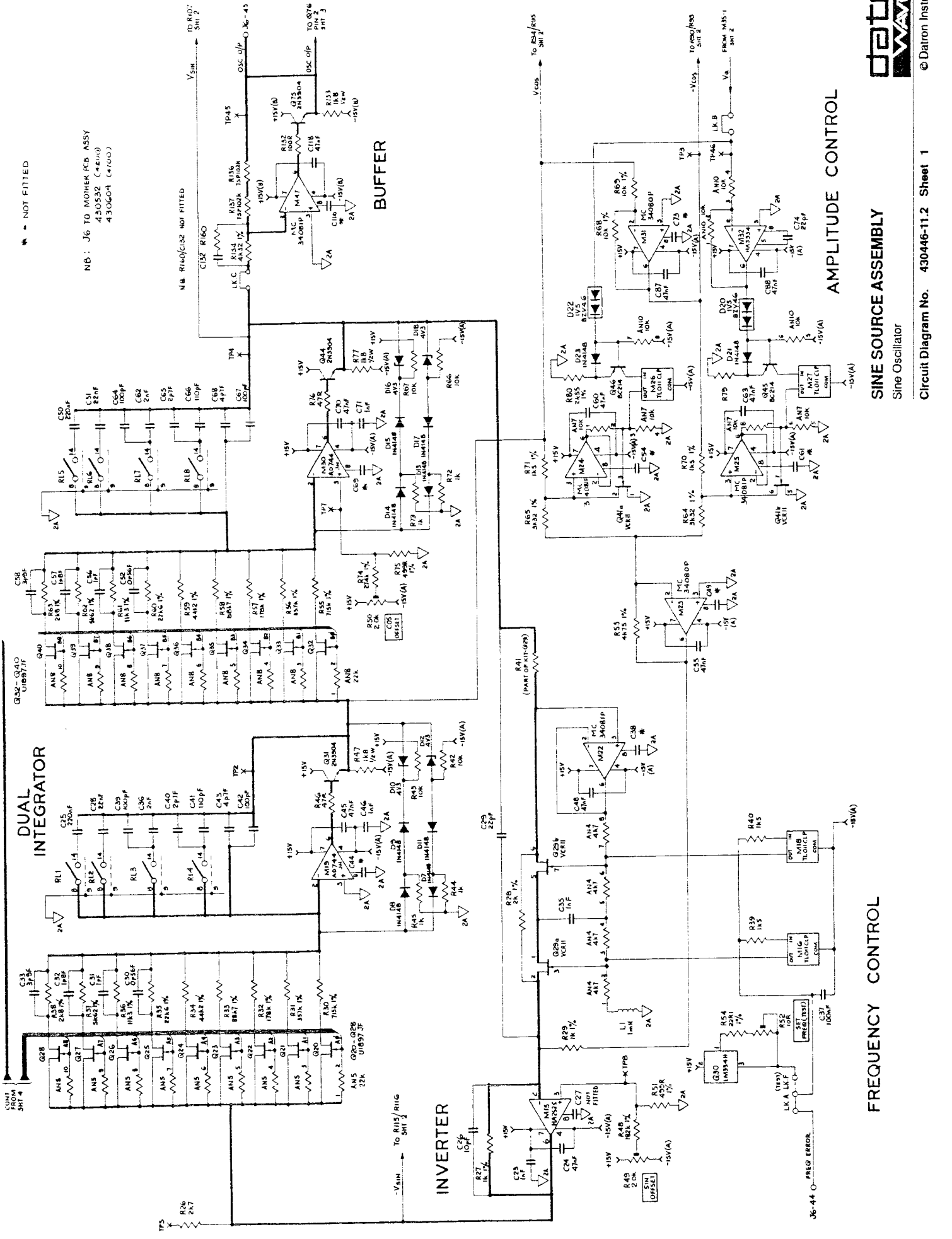
TO R10
SMT 2

OSC o/p
SMT 3

TO R3/RES
SMT 1

TO R50/RES
SMT 2

FROM MS-1
SMT 2



AMPLITUDE CONTROL

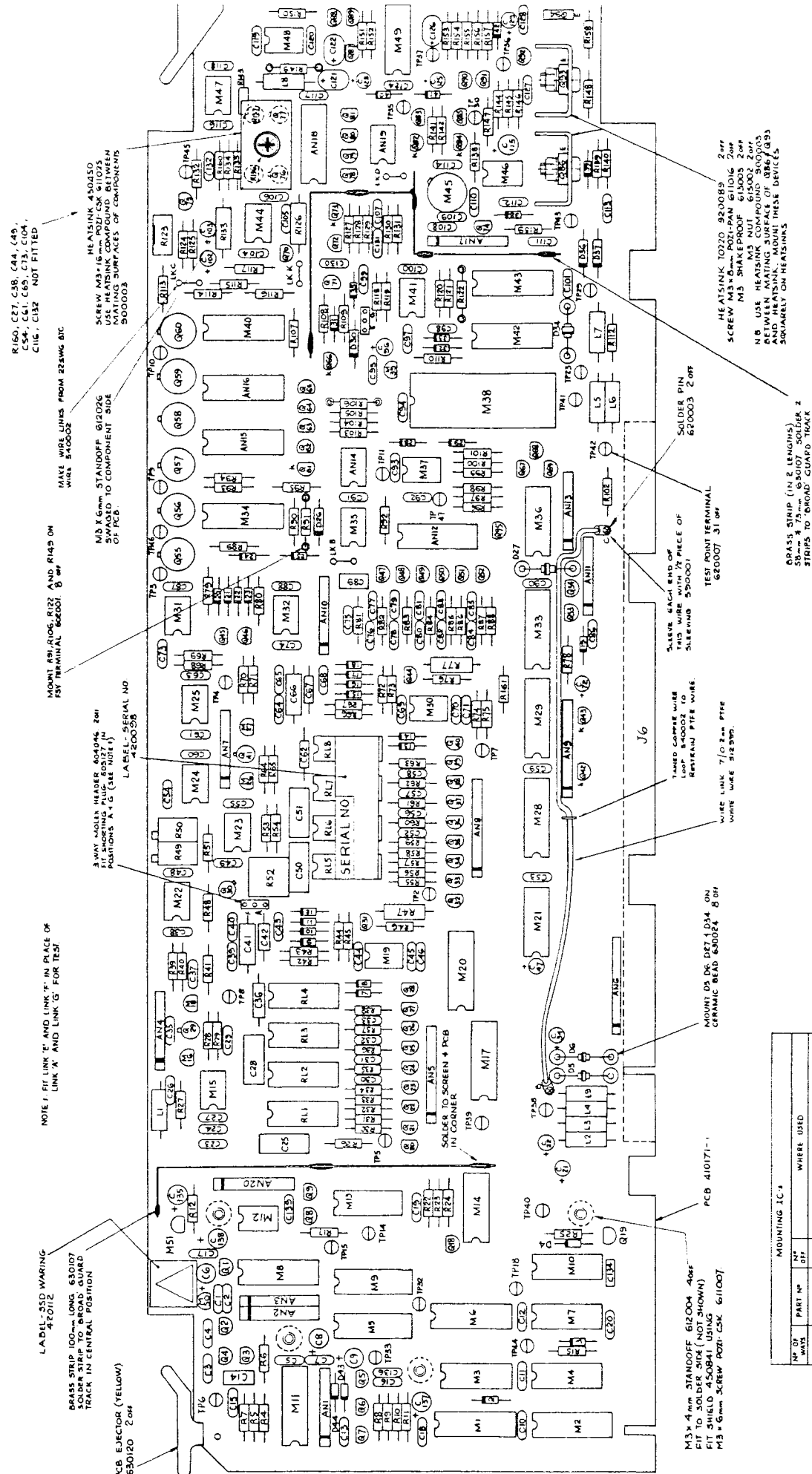
FREQUENCY CONTROL

SINE SOURCE ASSEMBLY

Sine Oscillator



SINE SOURCE ASSEMBLY



HEATSINK 404050
SCREW M3X4mm
USE HEATSINK COMPOUND BETWEEN
SURFACES OF COMPONENTS
9000003

MAKE WIRE LINKS FROM 22SWG BTC
WIRE 640002

M3 X 6mm STANDOFF 612026
SPACED TO COMPONENT SIDE
OF PCB

MOUNT R1, R106, R122 AND R145 ON
FSV TERMINAL 620001 8 OH

3 WAY HEADER BOARDING 2OH
POSITIONS A, G (SEE NOTE 1)
LABEL-SERIAL NO
620058

NOTE 1: FIT LINK 'F' AND LINK 'F' IN PLACE OF
LINK 'A' AND LINK 'G' FOR TEST

LABEL-5SD MARKING
62012

BRASS STRIP 100mm LONG 630107
FIT TO SOLDER SIDE (NOT SHOWN)
TRACK IN CENTRAL POSITION

PCB EJECTOR (YELLOW)
630120 2 OH

HEATSINK 10220 830089
SCREW M3X6mm PZL-PAN 61006 2 OH
M3 SHAKEPROOF 615005 2 OH
M3 NUT 615002 2 OH
M3 WASHER 615003 2 OH
BETWEEN HEATING SURFACES OF IC'S
AND HEATSINK. MOUNT THESE DEVICES
SQUARELY ON HEATSINKS

SOLDER PIN
620003 2 OH

TEST POINT TERMINAL
620007 31 OH

SLEEVE EACH END OF
THIS WIRE WITH 7/16" PIECE OF
SLEEVING 590001

WIRE LINK 7/16" PTFE
WIRE WIRE STRIP

MOUNT DS.D6 D27 1.034 ON
CERAMIC BEAD 630024 8 OH

M3 X 4mm STANDOFF 612004 4 OH
FIT TO SOLDER SIDE (NOT SHOWN)
USE TO SPACER BOARDING
M3 X 6mm SCREW PZL-CBK 610007

SOLDER TO SCREEN + PCB
IN CORNER

PCB 410171-1

PCB 61007

PCB 410171-1

PCB 410171-1

PCB 410171-1

PCB 410171-1

PCB 410171-1

PCB 410171-1

BRASS STRIP (IN 2 LENGTHS)
50mm x 75mm 630107 SOLDER 2
STRIPS TO BROAD GUARD TRACK
IN CENTRAL POSITION

WIRE LINK 7/16" PTFE
WIRE WIRE STRIP

WIRE LINK 7/16" PTFE
WIRE WIRE STRIP

WIRE LINK 7/16" PTFE
WIRE WIRE STRIP

WIRE LINK 7/16" PTFE
WIRE WIRE STRIP

WIRE LINK 7/16" PTFE
WIRE WIRE STRIP

WIRE LINK 7/16" PTFE
WIRE WIRE STRIP

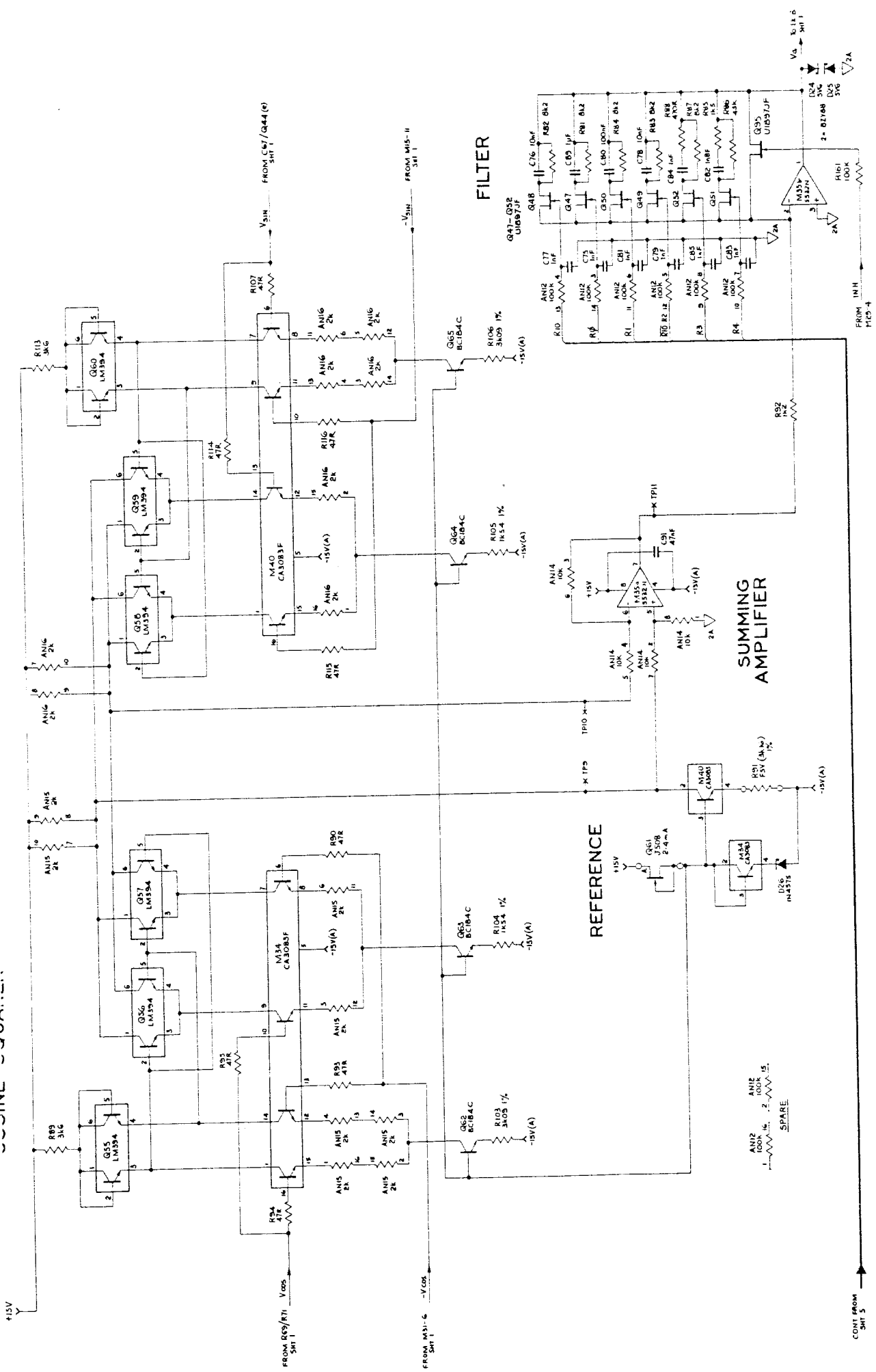
WIRE LINK 7/16" PTFE
WIRE WIRE STRIP

| NO OF MOUNTS | PART NO | WHERE USED |
|-----------------|---------|-----------------------------------|
| 1 | M18 | M22-E5 M50 M81 M37 M35 M37 |
| 8 | 605089 | M41 M44 M46 M47 M48 M12 M15 |
| 14 | 605060 | M5 M4 M7 M10 M15 M14 M21 M36 M49 |
| 16 | 605061 | M1 M2 M5 M6 M8 M9 M17 M20 M28 M25 |
| 28 | 605065 | M3 |

| NO OF MOUNTS | PART NO | WHERE USED |
|-----------------|---------|-----------------------------------|
| 1 | M18 | M22-E5 M50 M81 M37 M35 M37 |
| 8 | 605089 | M41 M44 M46 M47 M48 M12 M15 |
| 14 | 605060 | M5 M4 M7 M10 M15 M14 M21 M36 M49 |
| 16 | 605061 | M1 M2 M5 M6 M8 M9 M17 M20 M28 M25 |
| 28 | 605065 | M3 |

SC YER

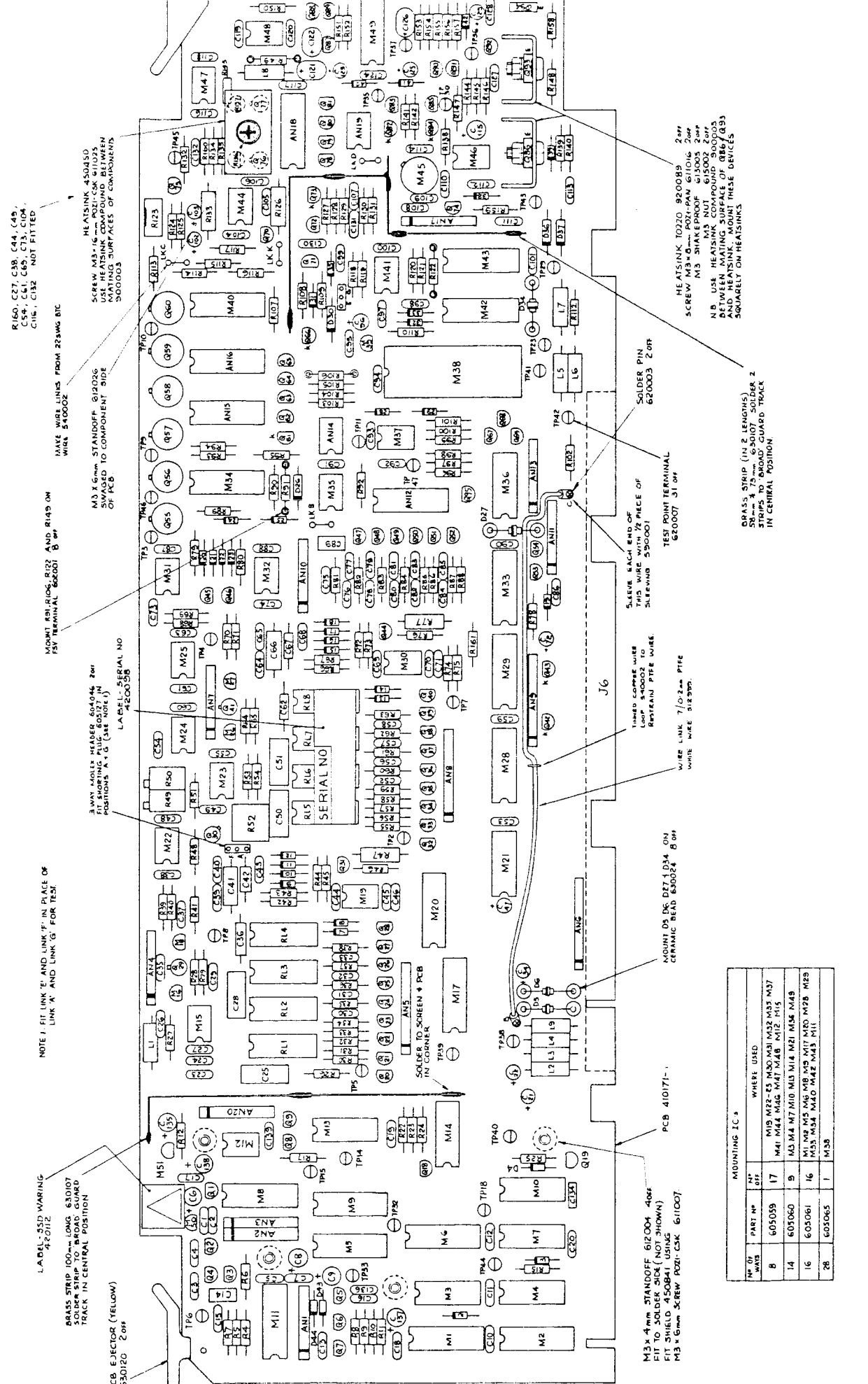
WINE -JUA...



SINE SOURCE ASSEMBLY
Oscillator Amplitude Detector and Reference



SINE SOURCE ASSEMBLY



R160, C27, C38, C44, C49, C54, C61, C65, C73, C104, C116, C132 NOT FITTED

HEATSHINK 450040
SCREW M3x6mm
USE HEATSHINK COMPOUND BETWEEN MATING SURFACES OF COMPONENTS 620003

MAKE WIRE LINKS FROM 22SWG BIC WIRE 540002

M3x4mm STANDOFF 612026 SWAGED TO COMPONENT SIDE OF PCB

MOUNT R1,R10,C,R122 AND R149 ON FS7 TERMINAL 620001 8 OH

3WAY HEADER 604046 2OH POSITIONING IN 1,3 (SEE NOTE J) LABEL SERIAL NO 4200358

NOTE 1: FIT LINK 'E' AND LINK 'F' IN PLACE OF LINK 'A' AND LINK 'G' FOR TEST.

LABEL 55D WAVING 420112

BRASS STRIP 100mm LONG 63007 SOLDER STRIP TO BRASS GUARD TRACK IN CENTRAL POSITION

PCB EJECTOR (YELLOW) 630120 2OH

HEATSHINK T0220 820089 2OH
SCREW M3x6mm POZI-PAN 611016 2OH
M3 SHAKEPROOF 613005 2OH
N.B. USE HEATSHINK NUT 615002 2OH BETWEEN MATING SURFACE OF 0801093 AND HEATSHINK. MOUNT THESE DEVICES SQUARELY ON HEATSHINKS

SOLDER PIN 620003 2OH

BRASS STRIP (IN 2 LENGTHS) 58mm x 4.75mm 630107 SOLDER 2 STRIPS TO BRASS GUARD TRACK IN CENTRAL POSITION

SLEEVE EACH END OF THIS WIRE WITH 1/2 PIECE OF SLEEVING 590001

TEST POINT TERMINAL 620007 31 OH

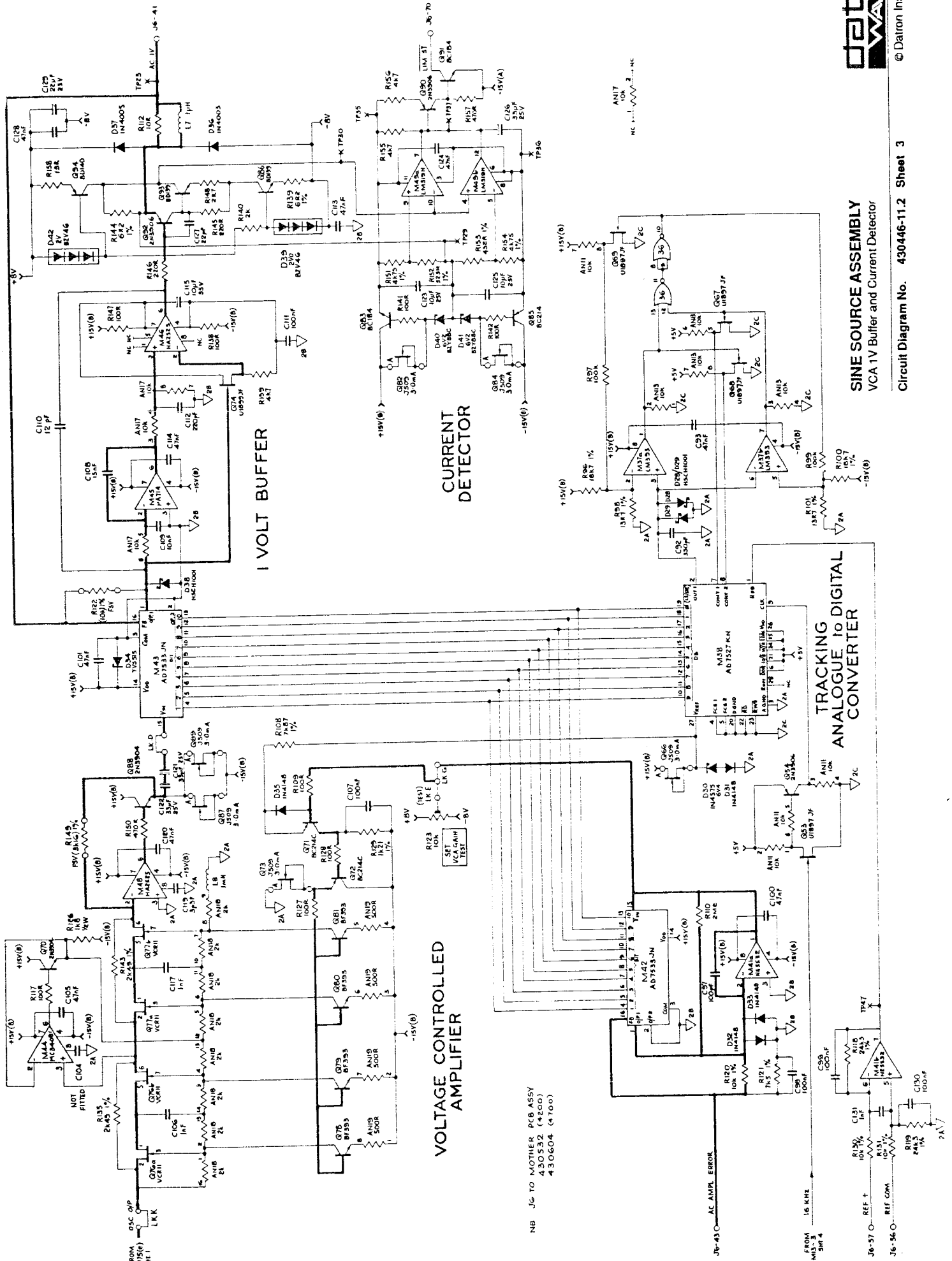
MOUNT D5,D6,D7,D134 ON CERAMIC BEAD 630024 8 OH

PCB 410171-1

M3x4mm STANDOFF 612004 4OH
FIT SOLDER BRASS GUARD TRACK
M3x6mm SCREW POZI-CSK 611007

| MP OF PARTS | MP PART # | WHERE USED |
|-------------|-----------|--|
| B | 605059 | M19, M22, R5, M30, M31, M32, M33, M37 |
| I4 | 605060 | M41, M44, M46, M47, M48, M12, M15 |
| I6 | 605061 | M3, M4, M7, M10, M13, M14, M21, M34, M48 |
| Z8 | 605065 | M1, M2, M5, M6, M8, M9, M11, M17, M20, M28, M29, M33, M34, M40, M42, M43, M45, M11 |

ASSEMBLY IC 4



NB J6 TO MOTHER PCB ASSY
430532 (+200)
430604 (+700)

TRACKING ANALOGUE TO DIGITAL CONVERTER

I VOLT BUFFER

CURRENT DETECTOR

VOLTAGE CONTROLLED AMPLIFIER

SINE SOURCE ASSEMBLY VCA 1V Buffer and Current Detector

SINE SOURCE ASSEMBLY

R160, C27, C38, C44, C49, C54, C61, C65, C73, C104, C116, C132 NOT FILLED

HEAT SINK 450150
USE HEAT SINK COMPOUND BETWEEN MATING SURFACES OF COMPONENTS 900003

MAKE WIRE LINKS FROM 22AWG BIC WIRE 540002

MOUNT R81, R106, R122 AND R145 ON FSV TERMINAL 620001 2 OFF

3WAY MOLEX HEADER 604046 2MM FIT SHORTING PLUG 600127 IN POSITIONS A+G (SEE NOTE 1) LABEL-SERIAL NO. 420058

NOTE 1: FIT LINK 'E' AND LINK 'F' IN PLACE OF LINK 'X' AND LINK 'G' FOR TEST

LABEL-350 MARKING 420112

BRASS STRIP 100mm LONG 631007 SOLDER STRIP TO BROAD GUARD TRACK IN CENTRAL POSITION

PCB EJECUTOR (YELLOW) 630120 2 OFF

SOLDER TO SCREEN + PCB IN CORNER

M3 x 4mm STANDOFF 612004 4066 FIT TO SOLDER SIDE (NOT SHOWN) FIT SHIELD 450841 USING M3 x 6mm SCREW POZI-CSK 611007

MOUNT D5, D6, D8, D134 ON CERAMIC BEAD 600024 8 OFF

WIRE LINK 7/0 2mm PTFE WIRE 518996

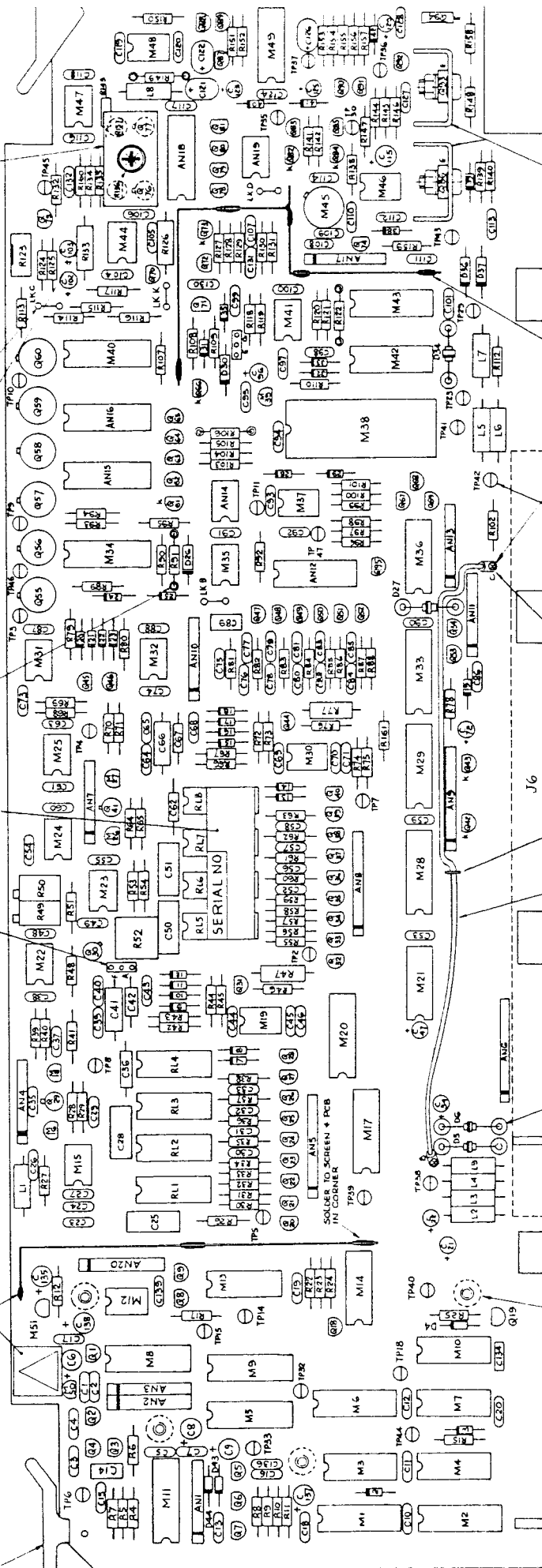
REMOVE EACH END OF THIS WIRE WITH 1/8" PIECE OF SLEEVING 530001

SOLDER PIN 620003 2 OFF

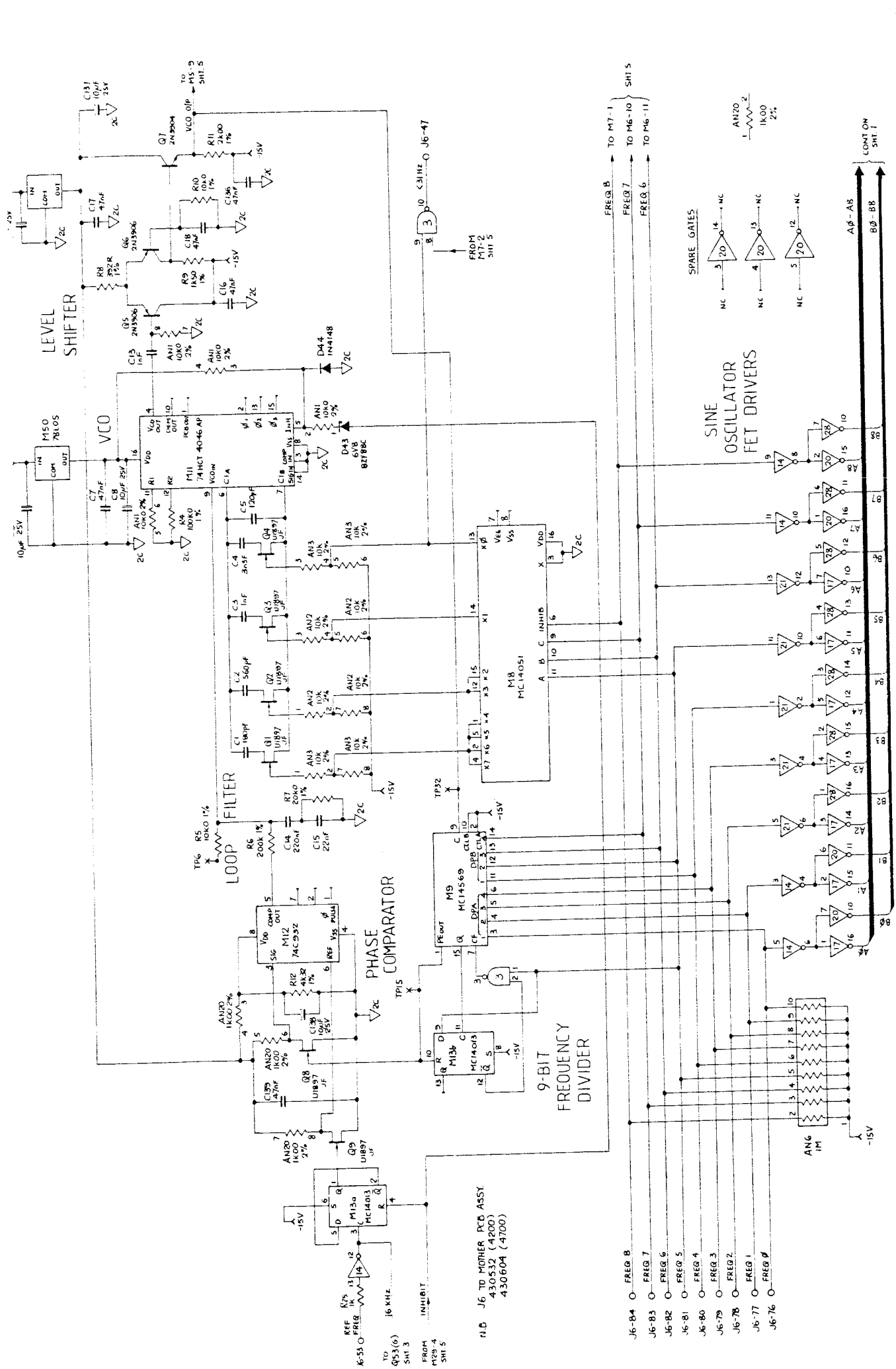
TEST POINT TERMINAL 620007 31 OFF

HEAT SINK T020, 920089 2 OFF
SCREW M3 x 6mm POZI-CSK 611007 2 OFF
M3 SHAKEPROOF 613005 2 OFF
M3 NUT 615002 2 OFF
NB USE HEAT SINK COMPOUND 900003 ON MOUNTING SURFACES OF R81, R106, R122 AND R145
HEAT SINK MOUNT THESE BOLTS SQUARELY ON HEAT SINKS

BRASS STRIP (IN 2 LENGTHS) ON 7/0 2mm PTFE SOLDER 2 STRIPS TO BROAD GUARD TRACK IN CENTRAL POSITION



| UP OF WAVE | PART NO | QTY | WHERE USED |
|------------|---------|-----|---|
| 8 | 605039 | 17 | M15, M22, E5, N-MO, M31, M32, M33, M37, M41, M42, M46, M47, M48, M12, M15 |
| 14 | 605060 | 9 | M3, M4, M7, M10, M13, M14, M21, M36, M45 |
| 16 | 605061 | 16 | M1, M6, M5, M8, M9, M11, M17, M18, M28, M29, M35, M38, M40, M42, M43, M11 |
| 28 | 605065 | 1 | M38 |



SINE SOURCE ASSEMBLY
 Digital Synthesizer - VCO

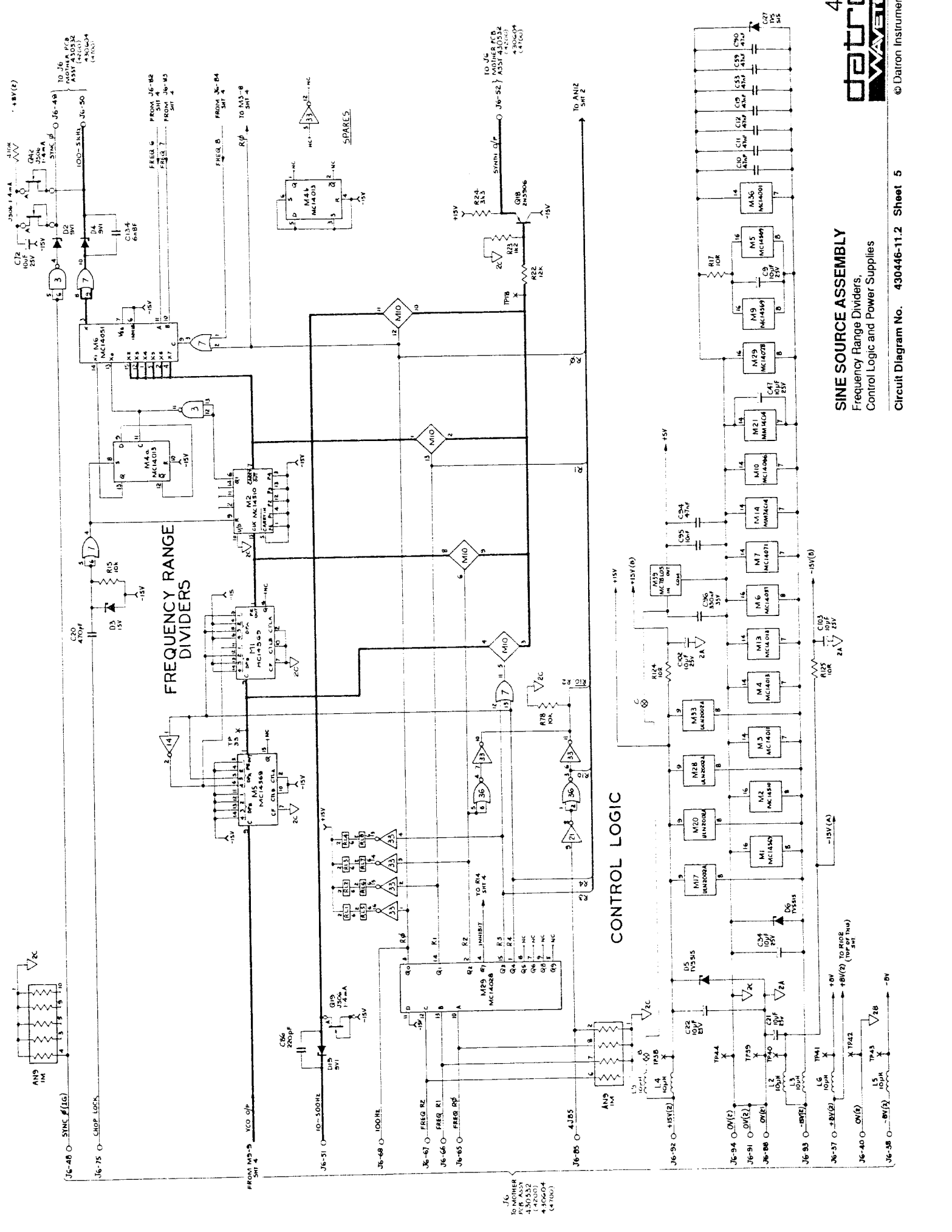
Circuit Diagram No. 430446-11.1 Sheet 4

- J6-84 ○ FREQ 8
- J6-83 ○ FREQ 7
- J6-82 ○ FREQ 6
- J6-81 ○ FREQ 5
- J6-80 ○ FREQ 4
- J6-79 ○ FREQ 3
- J6-78 ○ FREQ 2
- J6-77 ○ FREQ 1
- J6-76 ○ FREQ 0



N.D. J6 TO MOTHER PCB ASSY
 430532 (4200)
 430604 (4700)

SINE SOURCE ASSEMBLY
Frequency Range Dividers,
Control Logic and Power Supplies



| DATE | | ECO | | REVISION | | ISSUE | |
|-----------|------|------|------|----------|------|-------|------|
| 5.7.85 | 8.0 | 1958 | 8.0 | 8.0 | 1958 | 8.0 | 1958 |
| 29.10.85 | 8.1 | 2045 | 8.1 | 8.1 | 2045 | 8.1 | 2045 |
| 20.3.86 | 9.0 | 2168 | 9.0 | 9.0 | 2168 | 9.0 | 2168 |
| 5.6.86 | 9.1 | 2283 | 9.1 | 9.1 | 2283 | 9.1 | 2283 |
| 11.81 | 9.1 | 2404 | 9.1 | 9.1 | 2404 | 9.1 | 2404 |
| 23/1/86 | 9.2 | 2306 | 9.2 | 9.2 | 2306 | 9.2 | 2306 |
| 23/1/86 | 9.3 | 2497 | 9.3 | 9.3 | 2497 | 9.3 | 2497 |
| 25/1/86 | 9.4 | 2561 | 9.4 | 9.4 | 2561 | 9.4 | 2561 |
| 4.8.89 | 10.0 | 2658 | 10.0 | 10.0 | 2658 | 10.0 | 2658 |
| 19.9.89 | 10.1 | 2659 | 10.1 | 10.1 | 2659 | 10.1 | 2659 |
| 2.2.81 | 10.1 | 2748 | 10.1 | 10.1 | 2748 | 10.1 | 2748 |
| 28.4.89 | 10.2 | 2850 | 10.2 | 10.2 | 2850 | 10.2 | 2850 |
| 6.5.89 | 10.2 | 2775 | 10.2 | 10.2 | 2775 | 10.2 | 2775 |
| 19.5.81 | 10.3 | 2902 | 10.3 | 10.3 | 2902 | 10.3 | 2902 |
| 22.6.88 | 10.4 | 2946 | 10.4 | 10.4 | 2946 | 10.4 | 2946 |
| 16.8.88 | 10.5 | 2987 | 10.5 | 10.5 | 2987 | 10.5 | 2987 |
| 23.8.88 | 10.6 | 3006 | 10.6 | 10.6 | 3006 | 10.6 | 3006 |
| 20.3.88 | 11.0 | 3287 | 11.0 | 11.0 | 3287 | 11.0 | 3287 |
| 13.7.88 | 11.1 | 3378 | 11.1 | 11.1 | 3378 | 11.1 | 3378 |
| 14.12.88 | 11.2 | 3500 | 11.2 | 11.2 | 3500 | 11.2 | 3500 |
| 1 NOV 89 | 11.3 | 3713 | 11.3 | 11.3 | 3713 | 11.3 | 3713 |
| REVIAT | 11.4 | 3853 | 11.4 | 11.4 | 3853 | 11.4 | 3853 |
| 19 DEC 89 | 11.5 | 4005 | 11.5 | 11.5 | 4005 | 11.5 | 4005 |

| DESCRIPTION | DRAWING NUMBER | SHEET NUMBER | ISSUE | REVISION |
|-----------------------|----------------|--------------|-------|----------|
| COMPONENT LAYOUT | 480446 | 1 | 8.0 | 8.0 |
| PARTS LIST | LP400446 | ALL | 9.0 | 9.1 |
| SCHEMATIC | 430446 | 1 | 8.0 | 8.0 |
| SCHEMATIC | 430446 | 2 | 8.0 | 8.0 |
| SCHEMATIC | 430446 | 3 | 8.0 | 8.0 |
| SCHEMATIC | 430446 | 4 | 8.0 | 8.0 |
| SCHEMATIC | 430446 | 5 | 8.0 | 8.0 |
| FUNCTIONAL TEST PROC. | 460446/FT | 1-7 | 8.0 | 8.0 |
| FUNC. TEST TICK LIST | 470446/FT | 1 | 8.0 | 8.0 |
| PCB | 410171 | - | 10.0 | 10.0 |

| | | | | | | | |
|-------|---|------------------------------------|--------|---------|---------|----------------------------|--------------|
| NOTES | INDICATES NO CHANGE TO DOCS AT ISSUE LEVEL CHANGE | datron INSTRUMENTS NORWICH ENGLAND | DRN | CHK'D | APP'D | TITLE | DRAWING No. |
| | | | 11. | 150 | 5/ | 4200 SINE SOURCE PCB ASSY. | LD400446 |
| | | | DATE | DATE | DATE | | SHEET 1 OF 1 |
| | | | 5.7.85 | 10.7.85 | 23.7.85 | | |

DATRON INSTRUMENTS LTD PARTS LIST 07-Jan-92 DESC: ASSY PCB SINE SOURCE 4700 DRG NO: LP400446-11 REV: 5 PAGE NO: 1

| DESIG | PART NO | DESCRIPTION | PRINC MANUF | MANUF PART NUMBER | CLASS | UM | QUANTITY | CHANGES |
|-------|----------|-----------------------------|-------------|-------------------|-------|----|----------|---------|
| R4 | 011003 | RES MF 100K 1% .12W 50PPM | MEC | H8 100K 1% 50PPM | A | EA | 1 | |
| R5 | 011002 | RES MF 100K 1% .12W 50PPM | MEC | H8 100K 1% 50PPM | A | EA | 8 | |
| R6 | 012003 | RES MF 200K 1% .12W 50PPM | MEC | H8 200K 1% 50PPM | A | EA | 1 | |
| R7 | 012002 | RES MF 200K 1% .12W 50PPM | MEC | H8 200K 1% 50PPM | A | EA | 1 | |
| R8 | 013920 | RES MF 392R 1% .12W 50PPM | MEC | H8 392R 1% 50PPM | A | EA | 1 | |
| R9 | 011501 | RES MF 1K50 1% .12W 50PPM | MEC | H8 1K50 1% 50PPM | A | EA | 3 | |
| R10 | 011002 | RES MF 100K 1% .12W 50PPM | MEC | H8 100K 1% 50PPM | A | EA | - | |
| R11 | 012001 | RES MF 2K00 1% .12W 50PPM | MEC | H8 2K00 1% 50PPM | A | EA | 2 | |
| R12 | 014321 | RES MF 4K32 1% .12W 50PPM | MEC | H8 4K32 1% 50PPM | A | EA | 2 | |
| R15 | 000103 | RES CF 10K 5% .25W | NEOHM | CFR25 10K 5% | A | EA | 6 | |
| R17 | 000100 | RES CF 10R 5% .25W | NEOHM | CFR25 10R 5% | A | EA | 4 | |
| R22 | 000123 | RES CF 12K 5% .25W | NEOHM | CFR25 12K 5% | A | EA | 1 | |
| R23 | 000122 | RES CF 1K2 5% .25W | NEOHM | CFR25 1K2 5% | A | EA | 2 | |
| R24 | 000332 | RES CF 3K3 5% .25W | NEOHM | CFR25 3K3 5% | A | EA | 1 | |
| R25 | 000102 | RES CF 1K0 5% .25W | NEOHM | CFR25 1K0 5% | A | EA | 5 | |
| R26 | 000272 | RES CF 2K7 5% .25W | NEOHM | CFR25 2K7 5% | A | EA | 1 | |
| R27 | 011001 | RES MF 1K00 1% .12W 50PPM | MEC | H8 1K00 1% 50PPM | A | EA | 2 | |
| R28 | 012001 | RES MF 2K00 1% .12W 50PPM | MEC | H8 2K00 1% 50PPM | A | EA | - | |
| R29 | 011001 | RES MF 1K00 1% .12W 50PPM | MEC | H8 1K00 1% 50PPM | A | EA | - | |
| R30 | 047153 | RES MF 715K 1% .12W 50PPM | MEC | H8 715K 1% 50PPM | A | EA | 2 | |
| R31 | 013573 | RES MF 357K 1% .12W 50PPM | MEC | H8 357K 1% 50PPM | A | EA | 2 | |
| R32 | 011783 | RES MF 178K 1% .12W 50PPM | MEC | H8 178K 1% 50PPM | A | EA | 2 | |
| R33 | 018872 | RES MF 88K7 1% .12W 50PPM | MEC | H8 88K7 1% 50PPM | A | EA | 2 | |
| R34 | 014422 | RES MF 44K2 1% .12W 50PPM | MEC | H8 44K2 1% 50PPM | A | EA | 2 | |
| R35 | 012262 | RES MF 22K6 1% .12W 50PPM | MEC | H8 22K6 1% 50PPM | A | EA | 2 | |
| R36 | 011132 | RES MF 11K3 1% .12W 50PPM | MEC | H8 11K3 1% 50PPM | A | EA | 2 | |
| R37 | 015621 | RES MF 5K62 1% .12W 50PPM | MEC | H8 5K62 1% 50PPM | A | EA | 2 | |
| R38 | 012801 | RES MF 2K80 1% .12W 50PPM | MEC | H8 2K80 1% 50PPM | A | EA | 2 | |
| R39 | 000152 | RES CF 1K5 5% .25W | NEOHM | CFR25 1K5 5% | A | EA | 3 | |
| R40 | 000152 | RES CF 1K5 5% .25W | NEOHM | CFR25 1K5 5% | A | EA | - | |
| R41 | 239060-1 | TRAN JFET N-CHAN DUAL - RES | DATRON | SEE DRG | | S2 | 1 | |
| R42 | 000103 | RES CF 10K 5% .25W | NEOHM | CFR25 10K 5% | A | EA | - | |
| R43 | 000103 | RES CF 10K 5% .25W | NEOHM | CFR25 10K 5% | A | EA | - | |
| R44 | 000102 | RES CF 1K0 5% .25W | NEOHM | CFR25 1K0 5% | A | EA | - | |
| R45 | 000102 | RES CF 1K0 5% .25W | NEOHM | CFR25 1K0 5% | A | EA | - | |
| R46 | 000470 | RES CF 47R 5% .25W | NEOHM | CFR25 47R 5% | A | EA | 10 | |
| R47 | 001182 | RES CF 1K8 5% .5W | NEOHM | CFR50 1K8 5% | A | EA | 4 | |
| R48 | 011823 | RES MF 182K 1% .12W 50PPM | MEC | H8 182K 1% 50PPM | A | EA | 1 | |
| R49 | 067203 | RES CT 20K SIDE ADJ M/T | BECKMAN | 68X | A | EA | 2 | |
| R50 | 067203 | RES CT 20K SIDE ADJ M/T | BECKMAN | 68X | A | EA | - | |
| R51 | 014990 | RES MF 499R 1% .12W 50PPM | MEC | H8 499R 1% 50PPM | A | EA | 2 | |
| R52 | 063100 | RES CT 10R TOP ADJ S/T | BECKMAN | 72P | A | EA | 1 | |
| R53 | 014751 | RES MF 4K75 1% .12W 50PPM | MEC | H8 4K75 1% 50PPM | A | EA | 3 | |
| R54 | 012218 | RES MF 22R1 1% .12W 50PPM | MEC | H8 22R1 1% 50PPM | A | EA | 1 | |
| R55 | 047153 | RES MF 715K 1% .12W 50PPM | MEC | H8 715K 1% 50PPM | A | EA | - | |

- 8 JAN 1992

| DESIG | PART NO | DESCRIPTION | PRINC MANUF | MANUF PART NUMBER | CLASS | UM | QUANTITY | CHANGES |
|-------|---------|---------------------------|-------------|-------------------|-------|----|----------|---------|
| R56 | 013573 | RES MF 357K 1% .12W 50PPM | MEC | H8 357K 1% 50PPM | A | EA | - | |
| R57 | 011783 | RES MF 178K 1% .12W 50PPM | MEC | H8 178K 1% 50PPM | A | EA | - | |
| R58 | 012872 | RES MF 88K7 1% .12W 50PPM | MEC | H8 88K7 1% 50PPM | A | EA | - | |
| R59 | 014422 | RES MF 44K2 1% .12W 50PPM | MEC | H8 44K2 1% 50PPM | A | EA | - | |
| R60 | 012262 | RES MF 22K6 1% .12W 50PPM | MEC | H8 22K6 1% 50PPM | A | EA | - | |
| R61 | 011132 | RES MF 11K3 1% .12W 50PPM | MEC | H8 11K3 1% 50PPM | A | EA | - | |
| R62 | 015621 | RES MF 5K62 1% .12W 50PPM | MEC | H8 5K62 1% 50PPM | A | EA | - | |
| R63 | 012801 | RES MF 2K80 1% .12W 50PPM | MEC | H8 2K80 1% 50PPM | A | EA | - | |
| R64 | 013321 | RES MF 3K32 1% .12W 50PPM | MEC | H8 3K32 1% 50PPM | A | EA | 2 | |
| R65 | 013321 | RES MF 3K32 1% .12W 50PPM | MEC | H8 3K32 1% 50PPM | A | EA | - | |
| R66 | 000103 | RES CF 10K 5% .25W | NEOHM | CFR25 10K 5% | A | EA | - | |
| R67 | 000103 | RES CF 10K 5% .25W | NEOHM | CFR25 10K 5% | A | EA | - | |
| R68 | 011002 | RES MF 10K0 1% .12W 50PPM | MEC | H8 10K0 1% 50PPM | A | EA | - | |
| R69 | 011002 | RES MF 10K0 1% .12W 50PPM | MEC | H8 10K0 1% 50PPM | A | EA | - | |
| R70 | 011501 | RES MF 1K50 1% .12W 50PPM | MEC | H8 1K50 1% 50PPM | A | EA | - | |
| R71 | 011501 | RES MF 1K50 1% .12W 50PPM | MEC | H8 1K50 1% 50PPM | A | EA | - | |
| R72 | 000102 | RES CF 1K0 5% .25W | NEOHM | CFR25 1K0 5% | A | EA | - | |
| R73 | 000102 | RES CF 1K0 5% .25W | NEOHM | CFR25 1K0 5% | A | EA | - | |
| R74 | 012743 | RES MF 274K 1% .12W 50PPM | MEC | H8 274K 1% 50PPM | A | EA | 1 | |
| R75 | 014990 | RES MF 499R 1% .12W 50PPM | MEC | H8 499R 1% 50PPM | A | EA | - | |
| R76 | 000470 | RES CF 47R 5% .25W | NEOHM | CFR25 47R 5% | A | EA | - | |
| R77 | 001182 | RES CF 1K8 5% .5W | NEOHM | CFR50 1K8 5% | A | EA | - | |
| R78 | 000103 | RES CF 10K 5% .25W | NEOHM | CFR25 10K 5% | A | EA | - | |
| R79 | 012551 | RES MF 2K55 1% .12W 50PPM | MEC | H8 2K55 1% 50PPM | A | EA | 2 | |
| R80 | 012551 | RES MF 2K55 1% .12W 50PPM | MEC | H8 2K55 1% 50PPM | A | EA | - | |
| R81 | 000822 | RES CF 8K2 5% .25W | NEOHM | CFR25 8K2 5% | A | EA | 5 | |
| R82 | 000822 | RES CF 8K2 5% .25W | NEOHM | CFR25 8K2 5% | A | EA | - | |
| R83 | 000822 | RES CF 8K2 5% .25W | NEOHM | CFR25 8K2 5% | A | EA | - | |
| R84 | 000822 | RES CF 8K2 5% .25W | NEOHM | CFR25 8K2 5% | A | EA | - | |
| R85 | 000152 | RES CF 1K5 5% .25W | NEOHM | CFR25 1K5 5% | A | EA | - | |
| R86 | 000433 | RES CF 43K 5% .25W | NEOHM | CFR25 43K 5% | A | EA | 1 | |
| R87 | 000822 | RES CF 8K2 5% .25W | NEOHM | CFR25 8K2 5% | A | EA | - | |
| R88 | 000471 | RES CF 470R 5% .25W | NEOHM | CFR25 470R 5% | A | EA | 4 | |
| R89 | 000362 | RES CF 3K6 5% .25W | NEOHM | CFR25 3K6 5% | A | EA | 2 | |
| R90 | 000470 | RES CF 47R 5% .25W | NEOHM | CFR25 47R 5% | A | EA | - | |
| R91 | 013161 | RES MF 3K16 1% .12W 50PPM | MEC | H8 3K16 1% 50PPM | A | EA | 2 | |
| R92 | 000122 | RES CF 1K2 5% .25W | NEOHM | CFR25 1K2 5% | A | EA | - | |
| R93 | 000470 | RES CF 47R 5% .25W | NEOHM | CFR25 47R 5% | A | EA | - | |
| R94 | 000470 | RES CF 47R 5% .25W | NEOHM | CFR25 47R 5% | A | EA | - | |
| R95 | 000470 | RES CF 47R 5% .25W | NEOHM | CFR25 47R 5% | A | EA | - | |
| R96 | 011872 | RES MF 18K7 1% .12W 50PPM | MEC | H8 18K7 1% 50PPM | A | EA | 2 | |
| R97 | 000104 | RES CF 100K 5% .25W | NEOHM | CFR25 100K 5% | A | EA | 3 | |
| R98 | 011378 | RES MF 13R7 1% .12W 50PPM | MEC | H8 13R7 1% 50PPM | A | EA | 2 | |
| R99 | 000104 | RES CF 100K 5% .25W | NEOHM | CFR25 100K 5% | A | EA | - | |
| R100 | 011872 | RES MF 18K7 1% .12W 50PPM | MEC | H8 18K7 1% 50PPM | A | EA | - | |

| DESIG | PART NO | DESCRIPTION | PRINC MANUF | MANUF PART NUMBER | CLASS | UM | QUANTITY | CHANGES |
|-------|---------|---------------------------|-------------|-------------------|-------|----|----------|---------|
| R101 | 011378 | RES MF 13R7 1% .12W 50PPM | MEC | H8 13R7 1% 50PPM | A | EA | - | |
| R102 | 000471 | RES CF 470R 5% .25W | NEOHM | CFR25 470R 5% | A | EA | - | |
| R103 | 013091 | RES MF 3K09 1% .12W 50PPM | MEC | H8 3K09 1% 50PPM | A | EA | 2 | |
| R104 | 011541 | RES MF 1K54 1% .12W 50PPM | MEC | H8 1K54 1% 50PPM | A | EA | 2 | |
| R105 | 011541 | RES MF 1K54 1% .12W 50PPM | MEC | H8 1K54 1% 50PPM | A | EA | - | |
| R106 | 013091 | RES MF 3K09 1% .12W 50PPM | MEC | H8 3K09 1% 50PPM | A | EA | - | |
| R107 | 000470 | RES CF 47R 5% .25W | NEOHM | CFR25 47R 5% | A | EA | - | |
| R108 | 017871 | RES MF 7K87 1% .12W 50PPM | MEC | H8 7K87 1% 50PPM | A | EA | 1 | |
| R109 | 000101 | RES CF 100R 5% .25W | NEOHM | CFR25 100R 5% | A | EA | 9 | |
| R110 | 000225 | RES CF 2M2 5% .25W | NEOHM | CFR25 2M2 5% | A | EA | 1 | |
| R112 | 000100 | RES CF 10R 5% .25W | NEOHM | CFR25 10R 5% | A | EA | - | |
| R113 | 000362 | RES CF 3K6 5% .25W | NEOHM | CFR25 3K6 5% | A | EA | - | |
| R114 | 000470 | RES CF 47R 5% .25W | NEOHM | CFR25 47R 5% | A | EA | - | |
| R115 | 000470 | RES CF 47R 5% .25W | NEOHM | CFR25 47R 5% | A | EA | - | |
| R116 | 000470 | RES CF 47R 5% .25W | NEOHM | CFR25 47R 5% | A | EA | - | |
| R117 | 000101 | RES CF 100R 5% .25W | NEOHM | CFR25 100R 5% | A | EA | - | |
| R118 | 012432 | RES MF 24K3 1% .12W 50PPM | MEC | H8 24K3 1% 50PPM | A | EA | 2 | |
| R119 | 012432 | RES MF 24K3 1% .12W 50PPM | MEC | H8 24K3 1% 50PPM | A | EA | - | |
| R120 | 011002 | RES MF 10K0 1% .12W 50PPM | MEC | H8 10K0 1% 50PPM | A | EA | - | |
| R121 | 017501 | RES MF 7K50 1% .12W 50PPM | MEC | H8 7K50 1% 50PPM | A | EA | 1 | |
| R122 | 011002 | RES MF 10K0 1% .12W 50PPM | MEC | H8 10K0 1% 50PPM | A | EA | 1 | |
| R123 | 066103 | RES CT 10K SIDE ADJ S/T | BECKMAN | 72XW | A | EA | - | |
| R124 | 000100 | RES CF 10R 5% .25W | NEOHM | CFR25 10R 5% | A | EA | - | |
| R125 | 000100 | RES CF 10R 5% .25W | NEOHM | CFR25 10R 5% | A | EA | - | |
| R126 | 001182 | RES CF 1K8 5% .5W | NEOHM | CFR50 1K8 5% | A | EA | - | |
| R127 | 000101 | RES CF 100R 5% .25W | NEOHM | CFR25 100R 5% | A | EA | - | |
| R128 | 000101 | RES CF 100R 5% .25W | NEOHM | CFR25 100R 5% | A | EA | - | |
| R129 | 011211 | RES MF 1K21 1% .12W 50PPM | MEC | H8 1K21 1% 50PPM | A | EA | 1 | |
| R130 | 011002 | RES MF 10K0 1% .12W 50PPM | MEC | H8 10K0 1% 50PPM | A | EA | - | |
| R131 | 011002 | RES MF 10K0 1% .12W 50PPM | MEC | H8 10K0 1% 50PPM | A | EA | - | |
| R132 | 000101 | RES CF 100R 5% .25W | NEOHM | CFR25 100R 5% | A | EA | - | |
| R133 | 001182 | RES CF 1K8 5% .5W | NEOHM | CFR50 1K8 5% | A | EA | - | |
| R134 | 014321 | RES MF 4K32 1% .12W 50PPM | MEC | H8 4K32 1% 50PPM | A | EA | - | |
| R135 | 012491 | RES MF 2K49 1% .12W 50PPM | MEC | H8 2K49 1% 50PPM | A | EA | 2 | |
| R136 | 090063 | THERMISTOR PTC | PHILIPS | KTY81-120 | A | EA | - | |
| R137 | 090063 | THERMISTOR PTC | PHILIPS | KTY81-120 | A | EA | - | |
| R138 | 000101 | RES CF 100R 5% .25W | NEOHM | CFR25 100R 5% | A | EA | - | |
| R139 | 050153 | RES MF 6R2 1% .5W 50PPM | WELWYN | MFR4 | A | EA | 2 | |
| R140 | 000202 | RES CF 2K0 5% .25W | NEOHM | CFR25 2K0 5% | A | EA | 1 | |
| R141 | 000101 | RES CF 100R 5% .25W | NEOHM | CFR25 100R 5% | A | EA | - | |
| R142 | 000101 | RES CF 100R 5% .25W | NEOHM | CFR25 100R 5% | A | EA | - | |
| R143 | 012491 | RES MF 2K49 1% .12W 50PPM | MEC | H8 2K49 1% 50PPM | A | EA | - | |
| R144 | 050153 | RES MF 6R2 1% .5W 50PPM | WELWYN | MFR4 | A | EA | 2 | |
| R145 | 000221 | RES CF 220R 5% .25W | NEOHM | CFR25 220R 5% | A | EA | - | |
| R146 | 000221 | RES CF 220R 5% .25W | NEOHM | CFR25 220R 5% | A | EA | - | |

| DESIG | PART NO | DESCRIPTION | PRINC MANUF | MANUF PART NUMBER | CLASS | UM | QUANTITY | CHANGES |
|-------|---------|---------------------------|-------------|--------------------|-------|----|----------|---------|
| R147 | 000101 | RES CF 100K 5% .25W | NEOHM | CFR25 100K 5% | A | EA | - | |
| R148 | 000278 | RES CF 10K 5% .25W | NEOHM | CFR25 10K 5% | A | EA | 1 | |
| R149 | 013161 | RES MF 2K16 1% .12W 50PPM | MED | HB 3K16 1% 50PPM | A | EA | - | |
| R150 | 000471 | RES CF 470K 5% .25W | NEOHM | CFR25 470K 5% | A | EA | - | |
| R151 | 014751 | RES MF 4K75 1% .12W 50PPM | MED | HB 4K75 1% 50PPM | A | EA | - | |
| R152 | 015030 | RES MF 523R 1% .12W 50PPM | MED | HB 523R 1% 50PPM | A | EA | 1 | |
| R153 | 014320 | RES MF 432R 1% .12W 50PPM | MED | HB 432R 1% 50PPM | A | EA | 1 | |
| R154 | 014751 | RES MF 4K75 1% .12W 50PPM | MED | HB 4K75 1% 50PPM | A | EA | - | |
| R155 | 000472 | RES CF 4K7 5% .25W | NEOHM | CFR25 4K7 5% | A | EA | 3 | |
| R156 | 000472 | RES CF 4K7 5% .25W | NEOHM | CFR25 4K7 5% | A | EA | - | |
| R157 | 000471 | RES CF 470R 5% .25W | NEOHM | CFR25 470R 5% | A | EA | - | |
| R158 | 000150 | RES CF 10K 5% .25W | NEOHM | CFR25 10K 5% | A | EA | 1 | |
| R159 | 000472 | RES CF 4K7 5% .25W | NEOHM | CFR25 4K7 5% | A | EA | - | |
| R160 | 00000N | NOT FITTED | | | | | | |
| R161 | 000104 | RES CF 100K 5% .25W | NEOHM | CFR25 100K 5% | A | EA | - | |
| AN1 | 090131 | RES PACK 10K X 4 2% | BECKMAN | L08-3S-R10K | A | EA | 8 | |
| AN2 | 090131 | RES PACK 10K X 4 2% | BECKMAN | L08-3S-R10K | A | EA | - | |
| AN3 | 090131 | RES PACK 10K X 4 2% | BECKMAN | L08-3S-R10K | A | EA | - | |
| AN4 | 090132 | RES PACK 4K7 X 4 2% | BECKMAN | L08-3S-R4K7 | A | EA | 1 | |
| AN5 | 090140 | RES NTWK 22K X 9 2% | BECKMAN | L10-1S-R22K | A | EA | 2 | |
| AN6 | 090141 | RES NTWK 1M X 9 2% | BECKMAN | L10-1S-R1M | A | EA | 2 | |
| AN7 | 090131 | RES PACK 10K X 4 2% | BECKMAN | L08-3S-R10K | A | EA | - | |
| AN8 | 090140 | RES NTWK 22K X 9 2% | BECKMAN | L10-1S-R22K | A | EA | - | |
| AN9 | 090141 | RES NTWK 1M X 9 2% | BECKMAN | L10-1S-R1M | A | EA | - | |
| AN10 | 090131 | RES PACK 10K X 4 2% | BECKMAN | L08-3S-R10K | A | EA | - | |
| AN11 | 090131 | RES PACK 10K X 4 2% | BECKMAN | L08-3S-R10K | A | EA | - | |
| AN12 | 090086 | RES PACK 100K X 8 2% | AB | 761-3-100K | A | EA | 1 | |
| AN13 | 090131 | RES PACK 10K X 4 2% | BECKMAN | L08-3S-R10K | A | EA | - | |
| AN14 | 090142 | RES PACK 10K X 4 .5% | BECKMAN | 694-3-R10KD | A | EA | 1 | |
| AN15 | 090136 | RES PACK 2K X 8 .5% | BECKMAN | 698-3-R2KD | A | EA | 3 | |
| AN16 | 090136 | RES PACK 2K X 8 .5% | BECKMAN | 698-3-R2KD | A | EA | - | |
| AN17 | 090131 | RES PACK 10K X 4 2% | BECKMAN | L08-3S-R10K | A | EA | - | |
| AN18 | 090136 | RES PACK 2K X 8 .5% | BECKMAN | 698-3-R2KD | A | EA | - | |
| AN19 | 090143 | RES PACK 500R X 4 .5% | BECKMAN | 694-3-R500D | A | EA | 1 | |
| AN20 | 090168 | RES PACK 1K X 4 2% | AB | 770-83-1K | A | EA | 1 | |
| C1 | 100181 | CAP CP 180PF 2% 100V | PHILIPS | 2222 683 58181 | | EA | 1 | |
| C2 | 100561 | CAP CP 560PF 10% 100V | PHILIPS | 2222 630 19561 | | EA | 1 | |
| C3 | 100102 | CAP CP 1NF 10% 100V | PHILIPS | 2222 630 19102 | | EA | 15 | |
| C4 | 110027 | CAP PE 3N3F 20% 100V | WIMA | FKS2 3300 20% 100V | | EA | 1 | |
| C5 | 100121 | CAP CP 120PF 2% 100V | PHILIPS | 2222 683 34121 | | EA | 1 | |
| C6 | 150020 | CAP DT 10UF 20% 25V | AVX | TAP10M25F | A | EA | 15 | |
| C7 | 104026 | CAP CM 47NF +80%-20% 50V | AVX | SR175E4732AA | A | EA | 34 | |
| C8 | 150020 | CAP DT 10UF 20% 25V | AVX | TAP10M25F | A | EA | - | |
| C9 | 150020 | CAP DT 10UF 20% 25V | AVX | TAP10M25F | A | EA | - | |
| C10 | 104026 | CAP CM 47NF +80%-20% 50V | AVX | SR175E4732AA | A | EA | - | |

| DESIG | PART NO | DESCRIPTION | PRINC MANUF | MANUF PART NUMBER | CLASS | UM | QUANTITY | CHANGES |
|-------|---------|-------------------------------|-------------|--------------------|-------|----|----------|---------|
| C11 | 104026 | CAP CM 47NF +80%-20% 50V | AVX | SR175E4732AA | A | EA | - | |
| C12 | 104026 | CAP CM 47NF +80%-20% 50V | AVX | SR175E4732AA | A | EA | - | |
| C13 | 100102 | CAP CP 1NF 10% 100V | PHILIPS | 2222 630 19102 | | EA | - | |
| C14 | 110035 | CAP PE 220NF 20% 63V | WIMA | MKS2 0.12 20% 63V | | EA | 1 | |
| C15 | 110050 | CAP PE 22NF 10% 63V | WIMA | MKS2 0.022 10% 63V | | EA | 1 | |
| C16 | 104026 | CAP CM 47NF +80%-20% 50V | AVX | SR175E4732AA | A | EA | - | |
| C17 | 104026 | CAP CM 47NF +80%-20% 50V | AVX | SR175E4732AA | A | EA | - | |
| C18 | 104026 | CAP CM 47NF +80%-20% 50V | AVX | SR175E4732AA | A | EA | - | |
| C19 | 104026 | CAP CM 47NF +80%-20% 50V | AVX | SR175E4732AA | A | EA | - | |
| C20 | 102471 | CAP CD 470PF 20% 500V N4700 | BECK | CD10EM470PMSCR | A | EA | 1 | |
| C21 | 150020 | CAP DT 10UF 20% 25V | AVX | TAP10M25F | A | EA | - | |
| C22 | 150020 | CAP DT 10UF 20% 25V | AVX | TAP10M25F | A | EA | - | |
| C23 | 100102 | CAP CP 1NF 10% 100V | PHILIPS | 2222 630 19102 | | EA | - | |
| C24 | 104026 | CAP CM 47NF +80%-20% 50V | AVX | SR175E4732AA | A | EA | - | |
| C25 | 120034 | CAP PC 220NF 1% 63V | ASHCROFT | M2822101E | | EA | 2 | |
| C26 | 102100 | CAP CD 10PF 20% 500V NPC | BECK | CD08CG10PDMSCR | A | EA | 1 | |
| C27 | 00000N | NOT FITTED | | | | | | |
| C28 | 120035 | CAP PC 22NF 1% 400V | ASHCROFT | M2B22004E | | EA | 2 | |
| C29 | 102220 | CAP CD 22PF 10% 500V N150 | BECK | CD08PG22P0KSCR | A | EA | 3 | |
| C30 | 104017 | CAP CD 0P56P +/-0P1F 400V | BECK | GD08AG0P56BS | A | EA | 2 | |
| C31 | 102108 | CAP CD 1PF +/-0P5F 500V P100 | BECK | CD06AG01P0DSCR | A | EA | 2 | |
| C32 | 102188 | CAP CD 1P8F +/-5PF 500V | ITT | CD06AG1P8DSCR | A | EA | 2 | |
| C33 | 102398 | CAP CD 3P9F +/-0P5F 500V P100 | BECK | CD08AG03P9DSCR | A | EA | 2 | |
| C34 | 150020 | CAP DT 10UF 20% 25V | AVX | TAP10M25F | A | EA | - | |
| C35 | 100102 | CAP CP 1NF 10% 100V | PHILIPS | 2222 630 19102 | | EA | - | |
| C36 | 130083 | CAP PS 2NF 1% 160V | PHILIPS | 425 | | EA | 2 | |
| C37 | 110042 | CAP PE 100NF 20% 63V | WIMA | MKS2 0.1 20% 63V | | EA | 7 | |
| C38 | 00000N | NOT FITTED | | | | | | |
| C39 | 100101 | CAP CP 100PF 2% 100V | PHILIPS | 2222 683 34101 | | EA | 3 | |
| C40 | 100278 | CAP CP 2P7F +/-0P25F 100V | PHILIPS | 2222 683 09278 | | EA | 2 | |
| C41 | 130084 | CAP PS 110PF 1% 630V | PHILIPS | 427 | | EA | 2 | |
| C42 | 130042 | CAP PS 100PF 1% 630V | SUFLEX | HS | | EA | 2 | |
| C43 | 102478 | CAP CD 4P7F +/-5PF 500V NPC | BECK | CD08AGG4P7DSCR | A | EA | 2 | |
| C44 | 00000N | NOT FITTED | | | | | | |
| C45 | 104026 | CAP CM 47NF +80%-20% 50V | AVX | SR175E4732AA | A | EA | - | |
| C46 | 100102 | CAP CP 1NF 10% 100V | PHILIPS | 2222 630 19102 | | EA | - | |
| C47 | 150020 | CAP DT 10UF 20% 25V | AVX | TAP10M25F | A | EA | - | |
| C48 | 104026 | CAP CM 47NF +80%-20% 50V | AVX | SR175E4732AA | A | EA | - | |
| C49 | 00000N | NOT FITTED | | | | | | |
| C50 | 120034 | CAP PC 220NF 1% 63V | ASHCROFT | M2822101E | | EA | - | |
| C51 | 120035 | CAP PC 22NF 1% 400V | ASHCROFT | M2B22004E | | EA | - | |
| C52 | 104017 | CAP CD 0P56P +/-0P1F 400V | BECK | GD08AG0P56BS | A | EA | - | |
| C53 | 104026 | CAP CM 47NF +80%-20% 50V | AVX | SR175E4732AA | A | EA | - | |
| C54 | 00000N | NOT FITTED | | | | | | |
| C55 | 104026 | CAP CM 47NF +80%-20% 50V | AVX | SR175E4732AA | A | EA | - | |

| DESIGN | PART NO | DESCRIPTION | PRINC MANUF | MANUF PART NUMBER | CLASS | UM | QUANTITY | CHANGES |
|--------|---------|--------------------------------|-------------|----------------------|-------|----|----------|---------|
| C56 | 100109 | CAP CD 10PF +/-0.5PF 500V P100 | BECK | CD06AG01P000CR | A | EA | - | |
| C57 | 102149 | IND CD 100PF +/-0.5PF 500V | MT | CD06AG01P000CR | A | EA | - | |
| C58 | 102150 | CAP CD 10PF +/-0.5PF 500V P100 | BECK | CD06A100P000CR | A | EA | - | |
| C59 | 104026 | CAP CM 47NF +80%-20% 50V | AVX | SR175E473ZAA | A | EA | - | |
| C60 | 104026 | CAP CM 47NF +80%-20% 50V | AVX | SR175E473ZAA | A | EA | - | |
| C61 | 00000N | NOT FITTED | | | | EA | - | |
| C62 | 100093 | CAP PS 2NF 1% 160V | PHILIPS | 425 | | EA | - | |
| C63 | 104026 | CAP CM 47NF +80%-20% 50V | AVX | SR175E473ZAA | A | EA | - | |
| C64 | 100101 | CAP CP 100PF 2% 100V | PHILIPS | 2222 683 34101 | | EA | - | |
| C65 | 100102 | CAP CP 10PF +/-0.5PF 100V | PHILIPS | 2222 683 69279 | | EA | - | |
| C66 | 130094 | CAP PS 100PF 1% 630V | PHILIPS | 427 | | EA | - | |
| C67 | 130042 | CAP PS 100PF 1% 630V | SUFLEX | H5 | | EA | - | |
| C68 | 102478 | CAP CD 47PF +/-0.5PF 500V NPO | BECK | CD08AG04P70SCR | A | EA | - | |
| C69 | 00000N | NOT FITTED | | | | EA | - | |
| C70 | 104026 | CAP CM 47NF +80%-20% 50V | AVX | SR175E473ZAA | A | EA | - | |
| C71 | 100102 | CAP CP 1NF 10% 100V | PHILIPS | 2222 630 19102 | | EA | - | |
| C72 | 150020 | CAP DT 100PF 20% 25V | AVX | TAP10M25F | A | EA | - | |
| C73 | 00000N | NOT FITTED | | | | EA | - | |
| C74 | 102220 | CAP CD 22PF 10% 500V N150 | BECK | CD08PG22P0KSCR | A | EA | - | |
| C75 | 100102 | CAP CP 1NF 10% 100V | PHILIPS | 2222 630 19102 | | EA | - | |
| C76 | 110041 | CAP PE 10NF 20% 100V | WIMA | FKS2 0.01 20% 100V | | EA | 3 | |
| C77 | 102102 | CAP CD 1NF 10% 500V | BECK | CD10K101N0KSCR | A | EA | 1 | |
| C78 | 110041 | CAP PE 10NF 20% 100V | WIMA | FKS2 0.01 20% 100V | | EA | - | |
| C79 | 100102 | CAP CP 1NF 10% 100V | PHILIPS | 2222 630 19102 | | EA | - | |
| C80 | 110042 | CAP PE 100NF 20% 63V | WIMA | MKS2 0.1 20% 63V | | EA | - | |
| C81 | 100102 | CAP CP 1NF 10% 100V | PHILIPS | 2222 630 19102 | | EA | - | |
| C82 | 100182 | CAP CP 1NF 10% 100V | PHILIPS | 2222 630 19182 | | EA | 1 | |
| C83 | 100102 | CAP CP 1NF 10% 100V | PHILIPS | 2222 630 19102 | | EA | - | |
| C84 | 100102 | CAP CP 1NF 10% 100V | PHILIPS | 2222 630 19102 | | EA | - | |
| C85 | 100102 | CAP CP 1NF 10% 100V | PHILIPS | 2222 630 19102 | | EA | - | |
| C86 | 102221 | CAP CD 220PF 10% 500V N3300 | BECK | CD10DL220PKSCR | A | EA | 2 | |
| C87 | 104026 | CAP CM 47NF +80%-20% 50V | AVX | SR175E473ZAA | A | EA | - | |
| C88 | 104026 | CAP CM 47NF +80%-20% 50V | AVX | SR175E473ZAA | A | EA | - | |
| C89 | 110046 | CAP PE 10F 20% 50V | WIMA | MKS2 1.0 20% 50V | | EA | 1 | |
| C90 | 104026 | CAP CM 47NF +80%-20% 50V | AVX | SR175E473ZAA | A | EA | - | |
| C91 | 104026 | CAP CM 47NF +80%-20% 50V | AVX | SR175E473ZAA | A | EA | - | |
| C92 | 102351 | CAP CD 330PF 20% 500V K1 | BECK | CD08K1330PMSCR | A | EA | 1 | |
| C93 | 104026 | CAP CM 47NF +80%-20% 50V | AVX | SR175E473ZAA | A | EA | - | |
| C94 | 104026 | CAP CM 47NF +80%-20% 50V | AVX | SR175E473ZAA | A | EA | - | |
| C95 | 101103 | CAP CD 10NF +20-80% 250V | BECK | CD10K101N00SCR/SK250 | A | EA | 1 | |
| C96 | 150010 | CAP DT 330NF 20% 35V | AVX | TAPR33M35F | A | EA | 1 | |
| C97 | 100101 | CAP CP 100PF 2% 100V | PHILIPS | 2222 683 34101 | | EA | - | |
| C98 | 110042 | CAP PE 100NF 20% 63V | WIMA | MKS2 0.1 20% 63V | | EA | - | |
| C99 | 110042 | CAP PE 100NF 20% 63V | WIMA | MKS2 0.1 20% 63V | | EA | - | |
| C100 | 104026 | CAP CM 47NF +80%-20% 50V | AVX | SR175E473ZAA | A | EA | - | |

| DESIGN | PART NO | DESCRIPTION | PRINC MANUF | MANUF PART NUMBER | CLASS | UM | QUANTITY | CHANGES |
|--------|---------|--------------------------------|-------------|--------------------|-------|----|----------|---------|
| C101 | 104026 | CAP CM 47NF +80%-20% 50V | AVX | SR175E473ZAA | A | EA | - | |
| C102 | 150020 | CAP DT 100PF 20% 25V | AVX | TAP10M25F | A | EA | - | |
| C103 | 150020 | CAP DT 100PF 20% 25V | AVX | TAP10M25F | A | EA | - | |
| C104 | 00000N | NOT FITTED | | | | EA | - | |
| C105 | 104026 | CAP CM 47NF +80%-20% 50V | AVX | SR175E473ZAA | A | EA | - | |
| C106 | 100102 | CAP CP 1NF 10% 100V | PHILIPS | 2222 630 19102 | | EA | - | |
| C107 | 110042 | CAP PE 100NF 20% 63V | WIMA | MKS2 0.1 20% 63V | | EA | - | |
| C108 | 110015 | CAP PE 15NF 20% 63V | WIMA | MKS2 0.015 20% 63V | | EA | 1 | |
| C109 | 110041 | CAP PE 13NF 20% 100V | WIMA | FKS2 0.01 20% 100V | | EA | - | |
| C110 | 104064 | CAP CD 12PF 5% 50V | AVX | SR215A120JAA | | EA | 1 | |
| C111 | 110042 | CAP PE 100NF 20% 63V | WIMA | MKS2 0.1 20% 63V | | EA | - | |
| C112 | 102221 | CAP CD 220PF 10% 500V N3300 | BECK | CD10DL220PKSCR | A | EA | - | |
| C113 | 104026 | CAP CM 47NF +80%-20% 50V | AVX | SR175E473ZAA | A | EA | - | |
| C114 | 104026 | CAP CM 47NF +80%-20% 50V | AVX | SR175E473ZAA | A | EA | - | |
| C115 | 150015 | CAP DT 100PF 20% 35V | AVX | TAP10M35F | A | EA | 1 | |
| C116 | 00000N | NOT FITTED | | | | EA | - | |
| C117 | 100102 | CAP CP 1NF 10% 100V | PHILIPS | 2222 630 19102 | | EA | - | |
| C118 | 104026 | CAP CM 47NF +80%-20% 50V | AVX | SR175E473ZAA | A | EA | - | |
| C119 | 102338 | CAP CD 3P3P +/-0.5PF 500V P100 | BECK | CD08AG03P3DSCR | A | EA | 1 | |
| C120 | 104026 | CAP CM 47NF +80%-20% 50V | AVX | SR175E473ZAA | A | EA | - | |
| C121 | 150023 | CAP DT 330PF 20% 25V | AVX | TAP33M25F | A | EA | 3 | |
| C122 | 150023 | CAP DT 330PF 20% 25V | AVX | TAP33M25F | A | EA | - | |
| C123 | 150020 | CAP DT 100PF 20% 25V | AVX | TAP10M25F | A | EA | - | |
| C124 | 104026 | CAP CM 47NF +80%-20% 50V | AVX | SR175E473ZAA | A | EA | - | |
| C125 | 150020 | CAP DT 100PF 20% 25V | AVX | TAP10M25F | A | EA | - | |
| C126 | 150023 | CAP DT 330PF 20% 25V | AVX | TAP33M25F | A | EA | - | |
| C127 | 102220 | CAP CD 22PF 10% 500V N150 | BECK | CD08PG22P0KSCR | A | EA | - | |
| C128 | 104026 | CAP CM 47NF +80%-20% 50V | AVX | SR175E473ZAA | A | EA | - | |
| C129 | 150021 | CAP DT 220PF 20% 25V | AVX | TAP22M25F | A | EA | 1 | |
| C130 | 110042 | CAP PE 100NF 20% 63V | WIMA | MKS2 0.1 20% 63V | | EA | - | |
| C131 | 100102 | CAP CP 1NF 10% 100V | PHILIPS | 2222 630 19102 | | EA | - | |
| C132 | 00000N | NOT FITTED | | | | EA | - | |
| C134 | 120029 | CAP PC 6NF 20% 100V | WIMA | FKC2 6800 20% 100V | | EA | 1 | |
| C135 | 150020 | CAP DT 100PF 20% 25V | AVX | TAP10M25F | A | EA | - | |
| C136 | 104026 | CAP CM 47NF +80%-20% 50V | AVX | SR175E473ZAA | A | EA | - | |
| C137 | 150020 | CAP DT 100PF 20% 25V | AVX | TAP10M25F | A | EA | - | |
| C138 | 150020 | CAP DT 100PF 20% 25V | AVX | TAP10M25F | A | EA | - | |
| C139 | 104026 | CAP CM 47NF +80%-20% 50V | AVX | SR175E473ZAA | A | EA | - | |
| D2 | 210091 | DIODE 2N 9V1 400mW | PHILIPS | B2X79C9V1 | A | EA | 3 | |
| D3 | 210150 | DIODE 2N 15V 400mW | PHILIPS | B2X79C15 | A | EA | 1 | |
| D4 | 210091 | DIODE 2N 9V1 400mW | PHILIPS | B2X79C9V1 | A | EA | - | |
| D5 | 213009 | DIODE TS 15V 5/500W | UNITRODE | TVS515 | A | EA | 4 | |
| D6 | 213009 | DIODE TS 15V 5/500W | UNITRODE | TVS515 | A | EA | - | |
| D7 | 200001 | DIODE GP 75mA 75V | FAIRCHILD | 1N4148 | A | EA | 15 | |
| D8 | 200001 | DIODE GP 75mA 75V | FAIRCHILD | 1N4148 | A | EA | - | |

| DESIG | PART NO | DESCRIPTION | PRINC MANUF | MANUF PART NUMBER | CLASS | UM | QUANTITY | CHANGES |
|-------|---------|---------------------|-------------|-------------------|-------|----|----------|---------|
| D10 | 210043 | DIODE ZN 4V3 400MW | PHILIPS | B2X79C4V3 | A | EA | 4 | - |
| D11 | 200001 | DIODE GP 75mA 75V | FAIRCHILD | 1N4148 | | EA | - | - |
| D12 | 210043 | DIODE ZN 4V3 400MW | PHILIPS | B2X79C4V3 | A | EA | - | - |
| D13 | 200001 | DIODE GP 75mA 75V | FAIRCHILD | 1N4148 | | EA | - | - |
| D14 | 200001 | DIODE GP 75mA 75V | FAIRCHILD | 1N4148 | | EA | - | - |
| D15 | 200001 | DIODE GP 75mA 75V | FAIRCHILD | 1N4148 | | EA | - | - |
| D16 | 210043 | DIODE ZN 4V3 400MW | PHILIPS | B2X79C4V3 | A | EA | - | - |
| D17 | 200001 | DIODE GP 75mA 75V | FAIRCHILD | 1N4148 | | EA | - | - |
| D18 | 210043 | DIODE ZN 4V3 400MW | PHILIPS | B2X79C4V3 | A | EA | - | - |
| D19 | 210091 | DIODE ZN 5V1 400MW | PHILIPS | B2X79C9V1 | A | EA | - | - |
| D20 | 213011 | DIODE VR 1V4 250MW | PHILIPS | B2V86-1V4 | | EA | 2 | - |
| D21 | 200001 | DIODE GP 75mA 75V | FAIRCHILD | 1N4148 | | EA | - | - |
| D22 | 213011 | DIODE VR 1V4 250MW | PHILIPS | B2V86-1V4 | | EA | - | - |
| D23 | 200001 | DIODE GP 75mA 75V | FAIRCHILD | 1N4148 | | EA | - | - |
| D24 | 210056 | DIODE ZN 5V6 400MW | PHILIPS | B2X79C5V6 | A | EA | 2 | - |
| D25 | 210056 | DIODE ZN 5V6 400MW | PHILIPS | B2X79C5V6 | A | EA | - | - |
| D26 | 213023 | DIODE ZN 6V4 100PPM | PHILIPS | B2V10 | | EA | 2 | - |
| D27 | 213009 | DIODE TS 15V 5/500W | UNITRODE | TYS515 | A | EA | - | - |
| D28 | 220010 | DIODE SB | HP | 1N5711/1N6263 | A | EA | 3 | - |
| D29 | 220010 | DIODE SB | HP | 1N5711/1N6263 | A | EA | - | - |
| D30 | 213023 | DIODE ZN 6V4 100PPM | PHILIPS | B2V10 | | EA | - | - |
| D31 | 200001 | DIODE GP 75mA 75V | FAIRCHILD | 1N4148 | | EA | - | - |
| D32 | 200001 | DIODE GP 75mA 75V | FAIRCHILD | 1N4148 | | EA | - | - |
| D33 | 200001 | DIODE GP 75mA 75V | FAIRCHILD | 1N4148 | | EA | - | - |
| D34 | 213009 | DIODE TS 15V 5/500W | UNITRODE | TYS515 | A | EA | - | - |
| D35 | 200001 | DIODE GP 75mA 75V | FAIRCHILD | 1N4148 | | EA | - | - |
| D36 | 200006 | DIODE GP 1A 600V | FAIRCHILD | 1N4005 | | EA | 2 | - |
| D37 | 200006 | DIODE GP 1A 600V | FAIRCHILD | 1N4005 | | EA | - | - |
| D38 | 220010 | DIODE SB | HP | 1N5711/1N6263 | A | EA | - | - |
| D39 | 213012 | DIODE VR 2V0 250MW | PHILIPS | B2V86-2V0 | | EA | 2 | - |
| D40 | 210062 | DIODE ZN 6V2 400MW | PHILIPS | B2X79C6V2 | A | EA | 2 | - |
| D41 | 210062 | DIODE ZN 6V2 400MW | PHILIPS | B2X79C6V2 | A | EA | - | - |
| D42 | 213012 | DIODE VR 2V0 250MW | PHILIPS | B2V86-2V0 | | EA | - | - |
| D43 | 210068 | DIODE ZN 6V8 400MW | PHILIPS | B2X79C6V8 | A | EA | 1 | - |
| D44 | 200001 | DIODE GP 75mA 75V | FAIRCHILD | 1N4148 | | EA | - | - |
| Q1 | 230035 | TRAN JFET N-CHAN | TELEDYNE | U1897JF | | EA | 35 | - |
| Q2 | 230035 | TRAN JFET N-CHAN | TELEDYNE | U1897JF | | EA | - | - |
| Q3 | 230035 | TRAN JFET N-CHAN | TELEDYNE | U1897JF | | EA | - | - |
| Q4 | 230035 | TRAN JFET N-CHAN | TELEDYNE | U1897JF | | EA | - | - |
| Q5 | 250004 | TRAN PNP TO92 | MOTOROLA | 2N3906 | | EA | 6 | - |
| Q6 | 250004 | TRAN PNP TO92 | MOTOROLA | 2N3906 | | EA | - | - |
| Q7 | 240006 | TRAN NPN TO92 | MOTOROLA | 2N3904 | | EA | 4 | - |
| Q8 | 230035 | TRAN JFET N-CHAN | TELEDYNE | U1897JF | | EA | - | - |
| Q9 | 230035 | TRAN JFET N-CHAN | TELEDYNE | U1897JF | | EA | - | - |

| DESIG | PART NO | DESCRIPTION | PRINC MANUF | MANUF PART NUMBER | CLASS | UM | QUANTITY | CHANGES |
|-------|----------|-----------------------------|-------------|-------------------|-------|----|----------|---------|
| Q18 | 250004 | TRAN PNP TO92 | MOTOROLA | 2N3906 | | EA | - | - |
| Q19 | 230001 | TRAN JFET I LIM 1.4mA | SILICONIX | J506 | | EA | 3 | - |
| Q20 | 230035 | TRAN JFET N-CHAN | TELEDYNE | U1897JF | | EA | - | - |
| Q21 | 230035 | TRAN JFET N-CHAN | TELEDYNE | U1897JF | | EA | - | - |
| Q22 | 230035 | TRAN JFET N-CHAN | TELEDYNE | U1897JF | | EA | - | - |
| Q23 | 230035 | TRAN JFET N-CHAN | TELEDYNE | U1897JF | | EA | - | - |
| Q24 | 230035 | TRAN JFET N-CHAN | TELEDYNE | U1897JF | | EA | - | - |
| Q25 | 230035 | TRAN JFET N-CHAN | TELEDYNE | U1897JF | | EA | - | - |
| Q26 | 230035 | TRAN JFET N-CHAN | TELEDYNE | U1897JF | | EA | - | - |
| Q27 | 230035 | TRAN JFET N-CHAN | TELEDYNE | U1897JF | | EA | - | - |
| Q28 | 230035 | TRAN JFET N-CHAN | TELEDYNE | U1897JF | | EA | - | - |
| Q29 | 239060-1 | TRAN JFET N-CHAN DUAL - RES | DATRON | SEE DRG | | S2 | - | - |
| Q30 | 260060 | IC LIM I SOURCE | NATIONAL | LM334H | | EA | 1 | - |
| Q31 | 240043 | TRAN NPN TO92 RESERVE STOCK | MOTOROLA | 2N3904 | | EA | 2 | - |
| Q32 | 230035 | TRAN JFET N-CHAN | TELEDYNE | U1897JF | | EA | - | - |
| Q33 | 230035 | TRAN JFET N-CHAN | TELEDYNE | U1897JF | | EA | - | - |
| Q34 | 230035 | TRAN JFET N-CHAN | TELEDYNE | U1897JF | | EA | - | - |
| Q35 | 230035 | TRAN JFET N-CHAN | TELEDYNE | U1897JF | | EA | - | - |
| Q36 | 230035 | TRAN JFET N-CHAN | TELEDYNE | U1897JF | | EA | - | - |
| Q37 | 230035 | TRAN JFET N-CHAN | TELEDYNE | U1897JF | | EA | - | - |
| Q38 | 230035 | TRAN JFET N-CHAN | TELEDYNE | U1897JF | | EA | - | - |
| Q39 | 230035 | TRAN JFET N-CHAN | TELEDYNE | U1897JF | | EA | - | - |
| Q40 | 230035 | TRAN JFET N-CHAN | TELEDYNE | U1897JF | | EA | - | - |
| Q41 | 230046 | TRAN JFET N-CHAN DUAL | SILICONIX | VCR11N | | EA | 1 | - |
| Q42 | 230001 | TRAN JFET I LIM 1.4mA | SILICONIX | J506 | | EA | - | - |
| Q43 | 230001 | TRAN JFET I LIM 1.4mA | SILICONIX | J506 | | EA | - | - |
| Q44 | 240043 | TRAN NPN TO92 RESERVE STOCK | MOTOROLA | 2N3904 | | EA | - | - |
| Q45 | 250001 | TRAN PNP | MOTOROLA | BC214 | | EA | 3 | - |
| Q46 | 250001 | TRAN PNP | MOTOROLA | BC214 | | EA | - | - |
| Q47 | 230035 | TRAN JFET N-CHAN | TELEDYNE | U1897JF | | EA | - | - |
| Q48 | 230035 | TRAN JFET N-CHAN | TELEDYNE | U1897JF | | EA | - | - |
| Q49 | 230035 | TRAN JFET N-CHAN | TELEDYNE | U1897JF | | EA | - | - |
| Q50 | 230035 | TRAN JFET N-CHAN | TELEDYNE | U1897JF | | EA | - | - |
| Q51 | 230035 | TRAN JFET N-CHAN | TELEDYNE | U1897JF | | EA | - | - |
| Q52 | 230035 | TRAN JFET N-CHAN | TELEDYNE | U1897JF | | EA | - | - |
| Q53 | 230035 | TRAN JFET N-CHAN | TELEDYNE | U1897JF | | EA | - | - |
| Q54 | 250004 | TRAN PNP TO92 | MOTOROLA | 2N3906 | | EA | - | - |
| Q55 | 240017 | TRAN NPN | NATIONAL | LM394H | | EA | 6 | - |
| Q56 | 240017 | TRAN NPN | NATIONAL | LM394H | | EA | - | - |
| Q57 | 240017 | TRAN NPN | NATIONAL | LM394H | | EA | - | - |
| Q58 | 240017 | TRAN NPN | NATIONAL | LM394H | | EA | - | - |
| Q59 | 240017 | TRAN NPN | NATIONAL | LM394H | | EA | - | - |
| Q60 | 240017 | TRAN NPN | NATIONAL | LM394H | | EA | - | - |
| Q61 | 230050 | TRAN JFET I LIM 2mA | SILICONIX | J508 | | EA | 1 | - |
| Q62 | 240013 | TRAN NPN TO18 | MOTOROLA | BC184C | | EA | 4 | - |

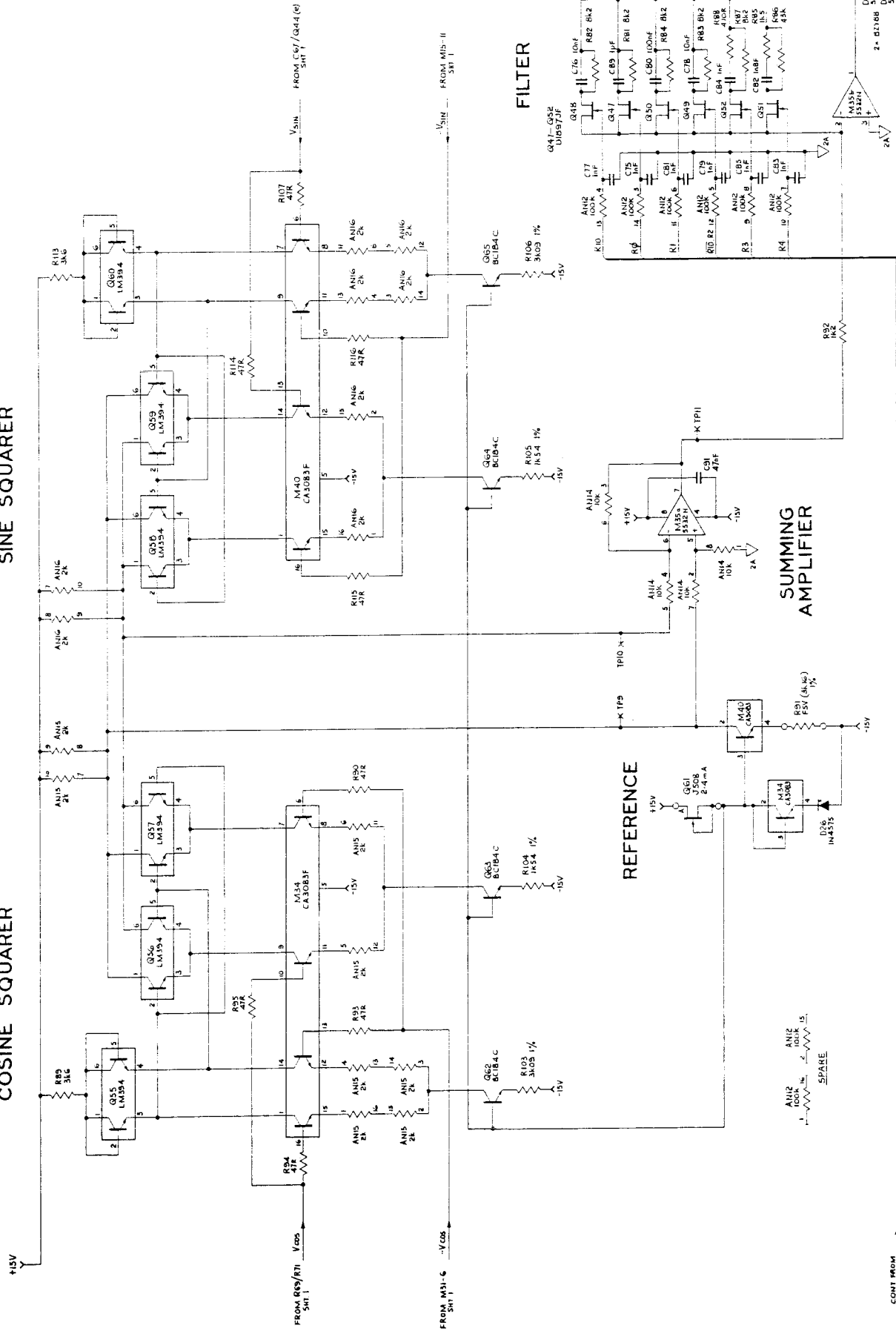
| DESIG | PART NO | DESCRIPTION | PRINC MANUF | MANUF PART NUMBER | CLASS | UM | QUANTITY | CHANGES |
|-------|----------|------------------------------|-------------|-------------------|-------|----|----------|---------|
| Q63 | 240013 | TRAN NPN TC18 | MOTOROLA | BC184C | EA | - | | |
| Q64 | 240013 | TRAN NPN TC18 | MOTOROLA | BC184C | EA | - | | |
| Q65 | 240013 | TRAN NPN TC18 | MOTOROLA | BC184C | EA | - | | |
| Q66 | 230042 | TRAN JFET I LIM 3mA | SILICONIX | J509 | EA | 6 | | |
| Q67 | 230035 | TRAN JFET N-CHAN | TELEDYNE | U1897JF | EA | - | | |
| Q68 | 230035 | TRAN JFET N-CHAN | TELEDYNE | U1897JF | EA | - | | |
| Q69 | 230035 | TRAN JFET N-CHAN | TELEDYNE | U1897JF | EA | - | | |
| Q70 | 240006 | TRAN NPN TC92 | MOTOROLA | 2N3904 | EA | 2 | | |
| Q71 | 250008 | TRAN PNP TC18 | MOTOROLA | BC214C | EA | - | | |
| Q72 | 250008 | TRAN PNP TC18 | MOTOROLA | BC214C | EA | - | | |
| Q73 | 230042 | TRAN JFET I LIM 3mA | SILICONIX | J509 | EA | - | | |
| Q74 | 230003 | TRAN JFET N-CHAN | TELEDYNE | U1899JF | EA | 1 | | |
| Q75 | 240006 | TRAN NPN TC92 | MOTOROLA | 2N3904 | EA | - | | |
| Q76 | 239059-1 | TRAN JFET N-CHAN DUAL X 2 | DATRON | SEE DRG | S2 | 1 | | |
| Q77 | 239059-1 | TRAN JFET N-CHAN DUAL X 2 | DATRON | SEE DRG | S2 | - | | |
| Q78 | 240032 | TRAN NPN | MOTOROLA | BF393 | EA | 4 | | |
| Q79 | 240032 | TRAN NPN | MOTOROLA | BF393 | EA | - | | |
| Q80 | 240032 | TRAN NPN | MOTOROLA | BF393 | EA | - | | |
| Q81 | 240032 | TRAN NPN | MOTOROLA | BF393 | EA | - | | |
| Q82 | 230042 | TRAN JFET I LIM 3mA | SILICONIX | J509 | EA | - | | |
| Q83 | 240001 | TRAN NPN | MOTOROLA | BC184 | EA | 2 | | |
| Q84 | 230042 | TRAN JFET I LIM 3mA | SILICONIX | J509 | EA | - | | |
| Q85 | 250001 | TRAN PNP | MOTOROLA | BC214 | EA | - | | |
| Q86 | 240031 | TRAN NPN | MOTOROLA | BD139 | EA | 2 | | |
| Q87 | 230042 | TRAN JFET I LIM 3mA | SILICONIX | J509 | EA | - | | |
| Q88 | 240006 | TRAN NPN TC92 | MOTOROLA | 2N3904 | EA | - | | |
| Q89 | 230042 | TRAN JFET I LIM 3mA | SILICONIX | J509 | EA | - | | |
| Q90 | 250004 | TRAN PNP TC92 | MOTOROLA | 2N3906 | EA | - | | |
| Q91 | 240001 | TRAN NPN | MOTOROLA | BC184 | EA | - | | |
| Q92 | 250004 | TRAN PNP TC92 | MOTOROLA | 2N3906 | EA | - | | |
| Q93 | 240031 | TRAN NPN | MOTOROLA | BD139 | EA | - | | |
| Q94 | 250021 | TRAN PNP | MOTOROLA | BD140 | EA | 1 | | |
| Q95 | 230035 | TRAN JFET N-CHAN | TELEDYNE | U1897JF | EA | - | | |
| M1 | 280101 | IC DIG COUNT DEC BIN PL X2 | MOTOROLA | MC14569BCP | EA | 3 | | |
| M2 | 280057 | IC DIG COUNT4 SYNC DEC PL UD | MOTOROLA | MC14510BCP | EA | 1 | | |
| M3 | 280008 | IC DIG NAND2 X4 | MOTOROLA | MC14011BCP | EA | 1 | | |
| M4 | 280011 | IC DIG FLIP FLOP D X2 | MOTOROLA | MC14013BCP | EA | 2 | | |
| M5 | 280101 | IC DIG COUNT DEC BIN PL X2 | MOTOROLA | MC14569BCP | EA | - | | |
| M6 | 280076 | IC DIG MUX 8TO1 ANALOG | MOTOROLA | MC14051BCL | A | EA | 2 | |
| M7 | 280079 | IC DIG OR2 X4 | MOTOROLA | MC14071BCP | EA | 1 | | |
| M8 | 280076 | IC DIG MUX 8TO1 ANALOG | MOTOROLA | MC14051BCL | A | EA | - | |
| M9 | 280101 | IC DIG COUNT DEC BIN PL X2 | MOTOROLA | MC14569BCP | EA | - | | |
| M10 | 280025 | IC DIG SWITCH QUAD CMOS | MOTOROLA | MC14066BCP | EA | 1 | | |
| M11 | 280197 | IC DIG PHASE LOCKED LOOP | PHILIPS | 74HCT4046AP | EA | 1 | | |
| M12 | 280125 | IC DIG PHASE DETECTOR | NATIONAL | MM74C932N | EA | 1 | | |

DATRON INSTRUMENTS LTD PARTS LIST 07-Jan-92 DESC: ASSY PCB SINE SOURCE 4700 DRG NO: LP400446-11 REV: 5 PAGE NO: 11

| DESIG | PART NO | DESCRIPTION | PRINC MANUF | MANUF PART NUMBER | CLASS | UM | QUANTITY | CHANGES |
|-------|----------|-----------------------------|-----------------|-------------------|-------|----|----------|---------|
| M13 | 280011 | IC DIG FLIP FLOP D X2 | MOTOROLA | MC14013BCP | EA | - | | |
| M14 | 280080 | IC DIG HEX SCHMITT TRIGGER | NATIONAL | 74C14N | EA | 2 | | |
| M15 | 260046 | IC LIN OP AMP | HARRIS | HA3 2525-5 | EA | 3 | | |
| M16 | 260076 | IC LIN I MIRROR 1:1 | TEXAS | TL011CLP | EA | 4 | | |
| M17 | 290090 | IC DIG DRIVER DARLINGTON X7 | EXAR | XR2202CP | A | EA | 4 | |
| M18 | 260076 | IC LIN I MIRROR 1:1 | TEXAS | TL011CLP | EA | - | | |
| M19 | 260134 | IC LIN OP AMP FET IP F/SET | ANALOG DEVICES | AD744JN | A | EA | 2 | |
| M20 | 290090 | IC DIG DRIVER DARLINGTON X7 | EXAR | XR2202CP | EA | - | | |
| M21 | 280080 | IC DIG HEX SCHMITT TRIGGER | NATIONAL | 74C14N | EA | - | | |
| M22 | 260087 | IC LIN OP AMP BIFET | MOTOROLA | MC34081P | EA | 5 | | |
| M23 | 260133 | IC LIN OP AMP | MOTOROLA | MC34080P | EA | 2 | | |
| M24 | 260087 | IC LIN OP AMP BIFET | MOTOROLA | MC34081P | EA | - | | |
| M25 | 260087 | IC LIN OP AMP BIFET | MOTOROLA | MC34081P | EA | - | | |
| M26 | 260076 | IC LIN I MIRROR 1:1 | TEXAS | TL011CLP | EA | - | | |
| M27 | 260076 | IC LIN I MIRROR 1:1 | TEXAS | TL011CLP | EA | - | | |
| M28 | 290090 | IC DIG DRIVER DARLINGTON X7 | EXAR | XR2202CP | A | EA | - | |
| M29 | 280035 | IC DIG DECODER BCDTODEC | MOTOROLA | MC14028BCP | EA | 1 | | |
| M30 | 260134 | IC LIN OP AMP FET IP F/SET | ANALOG DEVICES | AD744JN | EA | - | | |
| M31 | 260133 | IC LIN OP AMP | MOTOROLA | MC34080P | EA | - | | |
| M32 | 260057 | IC LIN OP AMP | SIGNETICS | NE5534N | EA | 1 | | |
| M33 | 290090 | IC DIG DRIVER DARLINGTON X7 | EXAR | XR2202CP | A | EA | - | |
| M34 | 290000 | TRAN NPN ARRAY X 5 | SILICON GENERAL | SG3083J | A | EA | 2 | |
| M35 | 260042 | IC LIN OP AMP DUAL | SIGNETICS | NE5532N | EA | 1 | | |
| M36 | 280023 | IC DIG NOR2 QUAD | MOTOROLA | MC14001UBCP | EA | 1 | | |
| M37 | 260078 | IC LIN V COMP DUAL | NATIONAL | LM393AN | EA | 1 | | |
| M38 | 280126 | IC DIG DAC | ANALOG DEVICES | AD7527LN | A | EA | 1 | |
| M39 | 260033 | IC LIN REG 5V .1A | MOTOROLA | MC78L05ACP | A | EA | 3 | |
| M40 | 290000 | TRAN NPN ARRAY X 5 | SILICON GENERAL | SG3083J | A | EA | - | |
| M41 | 260042 | IC LIN OP AMP DUAL | SIGNETICS | NE5532N | EA | - | | |
| M42 | 280127 | IC DIG DAC MULT 10BIT | ANALOG DEVICES | AD7533JN | EA | 2 | | |
| M43 | 280127 | IC DIG DAC MULT 10BIT | ANALOG DEVICES | AD7533JN | EA | - | | |
| M44 | 260087 | IC LIN OP AMP BIFET | MOTOROLA | MC34081P | EA | - | | |
| M45 | 260027 | IC LIN OP AMP | FAIRCHILD | UA714HC | A | EA | 1 | |
| M46 | 260046 | IC LIN OP AMP | HARRIS | HA3 2525-5 | EA | - | | |
| M47 | 260087 | IC LIN OP AMP BIFET | MOTOROLA | MC34081P | EA | - | | |
| M48 | 260046 | IC LIN OP AMP | HARRIS | HA3 2525-5 | EA | - | | |
| M49 | 260049 | IC LIN V COMP DUAL | NATIONAL | LM319N | EA | 1 | | |
| M50 | 260033 | IC LIN REG 5V .1A | MOTOROLA | MC78L05ACP | A | EA | - | |
| M51 | 260033 | IC LIN REG 5V .1A | MOTOROLA | MC78L05ACP | A | EA | - | |
| RL1 | 330012-3 | RELAY 1PNO REED GUARDED | HAMLIN | HE721A5134 TO DRG | EA | 8 | | |
| RL2 | 330012-3 | RELAY 1PNO REED GUARDED | HAMLIN | HE721A5134 TO DRG | EA | - | | |
| RL3 | 330012-3 | RELAY 1PNO REED GUARDED | HAMLIN | HE721A5134 TO DRG | EA | - | | |
| RL4 | 330012-3 | RELAY 1PNO REED GUARDED | HAMLIN | HE721A5134 TO DRG | EA | - | | |
| RL5 | 330012-3 | RELAY 1PNO REED GUARDED | HAMLIN | HE721A5134 TO DRG | EA | - | | |
| RL6 | 330012-3 | RELAY 1PNO REED GUARDED | HAMLIN | HE721A5134 TO DRG | EA | - | | |

COSINE SQUARER

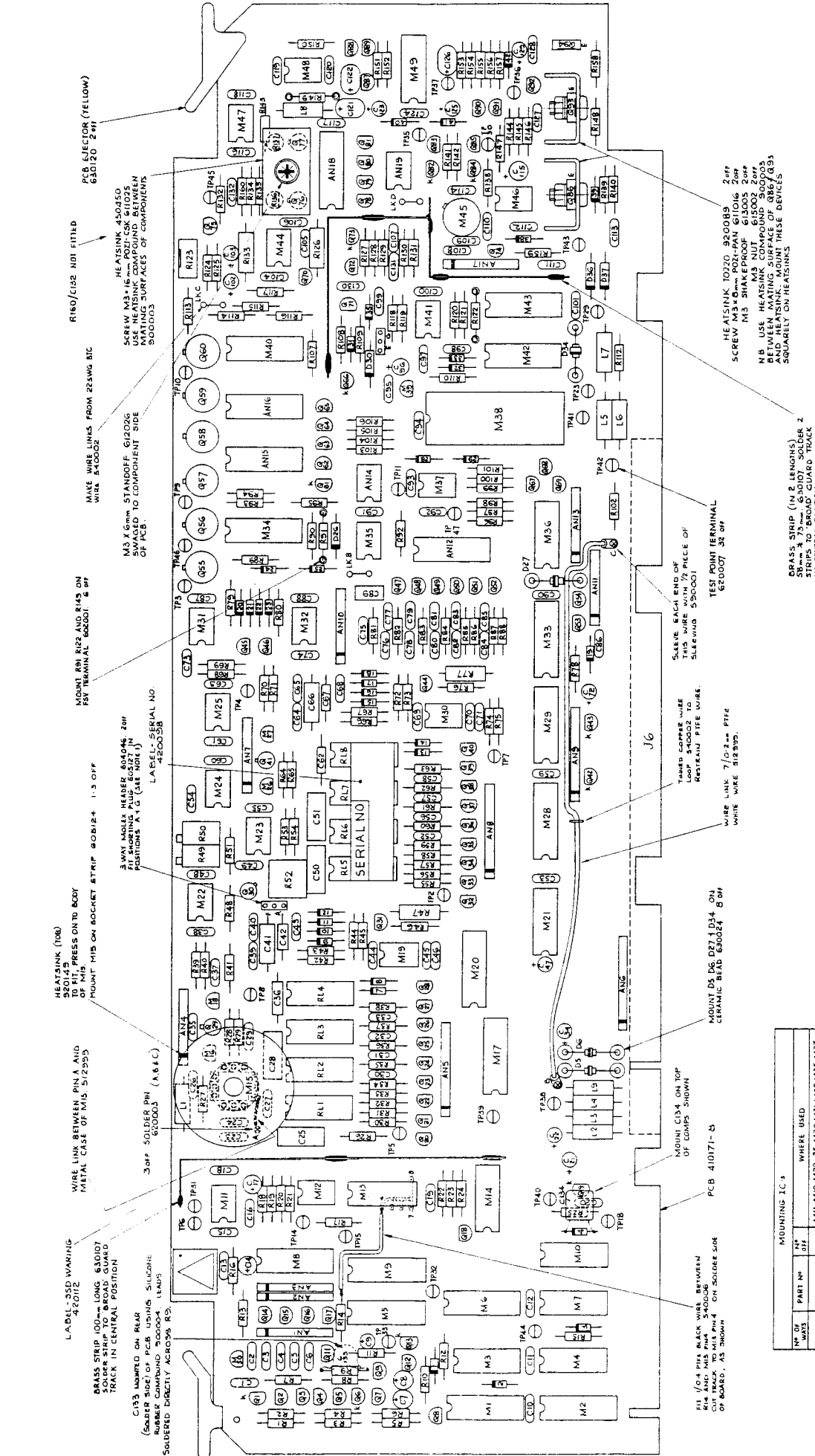
SINE SQUARER



SINE SOURCE ASSEMBLY
Oscillator Amplitude Detector and Reference
Circuit Diagram No. 430446-11.0 Sheet 2

SINE SOURCE ASSEMBLY

NOTE: FIT LINK 'E' AND LINK 'F' IN P
LINK 'A' AND LINK 'G' FOR T



HEATSINK (100)
220145
TO FIT, PRESS ON TO BODY
MOUNT HIS ON SOCKET STRIP 608124 1-3 OFF

HEATSINK (100)
220145
TO FIT, PRESS ON TO BODY
MOUNT HIS ON SOCKET STRIP 608124 1-3 OFF

WIRE LINK BETWEEN PIN A AND
METAL CASE OF M15 512955

WIRE LINK BETWEEN PIN A AND
METAL CASE OF M15 512955

3 OFF SOLDER PH
600035 (A B C)

3 OFF SOLDER PH
600035 (A B C)

LABEL-35D WARNING
42012

BRASS STRIP 100mm LONG 630107
USING TRACK IN CENTRAL POSITION

C133 MOUNTED ON REAR
(SOLDER SIDE) OF PCB USING SILICONE
RUBBER COMPOUND 500004. LEADS
SOLDERED DIRECTLY ACROSS RS.

2-WAY MOLEX HEADER 604046 20P
POSITIONS 'A' 'G' (SEE NOTE J)
LABEL-SERIAL NO.
420058

MOUNT R81 R82 AND R45 ON
FSV TERMINAL 600001 6 OFF

M3 X 0.6mm STANDOFF G12026
SWAGED TO COMPONENT SIDE
OF PCB.

USE HEATING COMPOUND BETWEEN
SURFACES OF COMPONENTS
500003

MAKE WIRE LINKS FROM 2214W BIC
WIRE 540002

R160/C128 NOT FITTED
PCB (SECTOR (YELLOW))

HEATSINK 10270 650088 2 OFF
SCREW M3 X 16mm PAN 613005 2 OFF
M3 SHAKEPROOF
M3 NUT 613002 2 OFF
M3 WASHERS 613001 2 OFF
N.B. USE HEATING COMPOUND
BETWEEN HEATING SURFACE OF M3
AND HEATSINK. MOUNT THESE DEVICES
SQUARELY ON HEATSINKS.

HEATSINK 10270 650088 2 OFF
SCREW M3 X 16mm PAN 613005 2 OFF
M3 SHAKEPROOF
M3 NUT 613002 2 OFF
M3 WASHERS 613001 2 OFF
N.B. USE HEATING COMPOUND
BETWEEN HEATING SURFACE OF M3
AND HEATSINK. MOUNT THESE DEVICES
SQUARELY ON HEATSINKS.

BRASS STRIP (IN 2 LENGTHS)
50mm X 75mm 630107 SOLDER 2
IN CENTRAL POSITION.
QUAD TRACK

SOLDER EACH END OF
THIS WIRE WITH 1/8" PIECE OF
SLEEVING 590001

TEST POINT TERMINAL
650007 32 OFF

THREE COPPER WIRE
REINFORCEMENT WIRE

WIRE LINK 7/10mm PTFE
WIRE WIRE SLEEVES.

MOUNT D5 D6 D7 D1 D44 ON
CERAMIC BEAD 604024 8 OFF

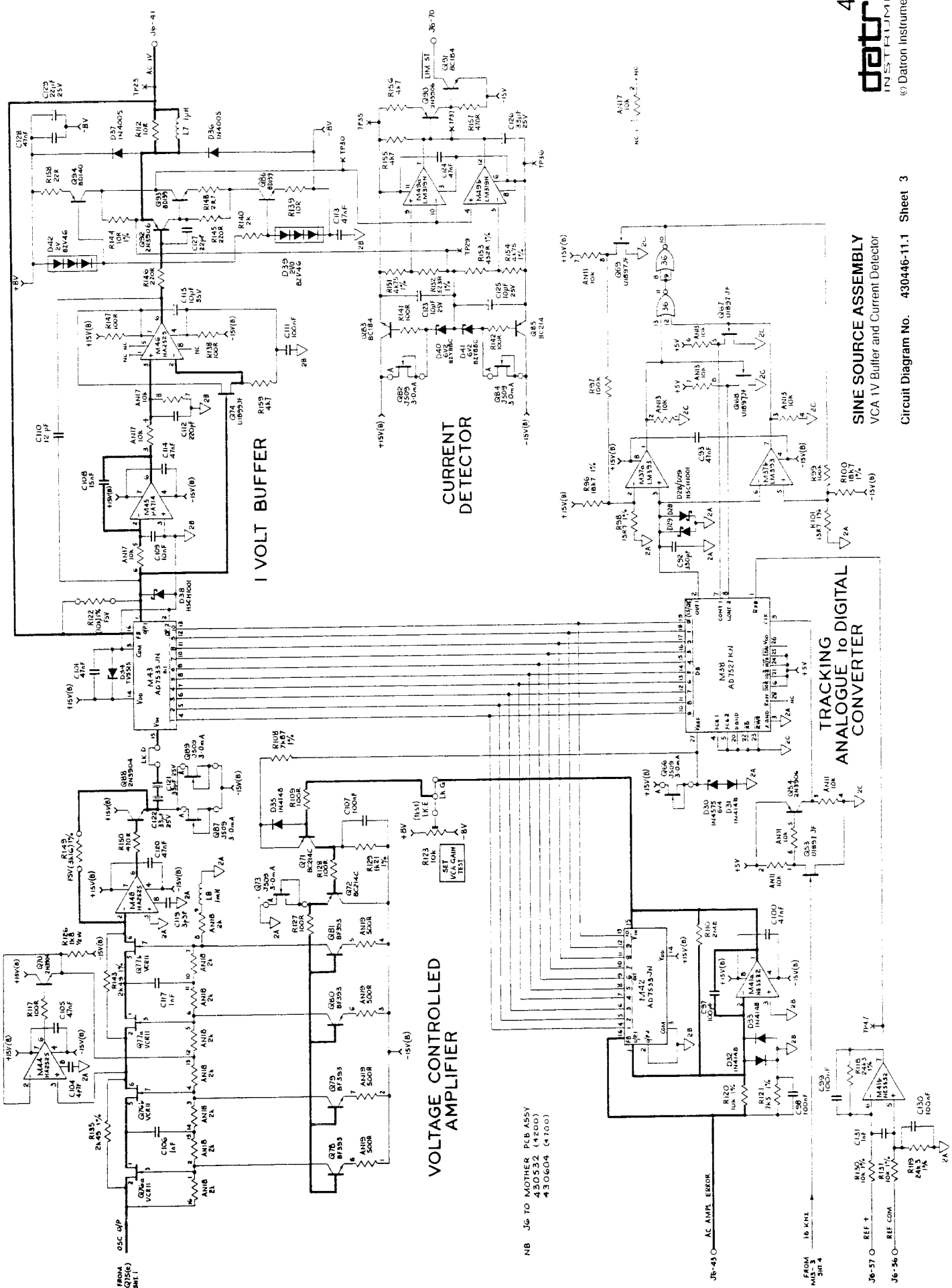
MONITOR G134 ON TOP
OF COILS SHOWN

PCB 410171-3

FIL 1/0.4 PHS BLACK WIRE BETWEEN
R14 AND M8 PH4 540006
ON BOARD. AS SHOWN

| MP NO. | PART NO. | QUANTITY | WHERE USED |
|--------|----------|----------|---|
| 8 | 605009 | 17 | M11, M19, M22-E5, M30, M31, M32, M33, M37 |
| 14 | 605060 | 5 | M3, M4, M7, M10, M14, M15, M16, M17, M18, M19 |
| 16 | 605061 | 5 | M1, M2, M5, M6, M9, M12, M13, M28, M38 |
| 26 | 605065 | 1 | M38 |

SINE SOURCE ASSEMBLY
 VCA TV Buffer and Current Detector



NB. J6 TO MOTHER PCB ASSY
 430532 (4200)
 430604 (4700)

16 K7E

FROM M1E-3 3H4

J6-57 O REF +

J6-56 O REF COM

J6-55 O REF GND

J6-54 O REF +

J6-53 O REF -

J6-52 O REF GND

J6-51 O REF +

J6-50 O REF -

J6-49 O REF GND

J6-48 O REF +

J6-47 O REF -

J6-46 O REF GND

J6-45 O REF +

J6-44 O REF -

J6-43 O REF GND

J6-42 O REF +

J6-41 O REF -

J6-40 O REF GND

J6-39 O REF +

J6-38 O REF -

J6-37 O REF GND

J6-36 O REF +

J6-35 O REF -

J6-34 O REF GND

J6-33 O REF +

J6-32 O REF -

J6-31 O REF GND

J6-30 O REF +

J6-29 O REF -

J6-28 O REF GND

J6-27 O REF +

J6-26 O REF -

J6-25 O REF GND

J6-24 O REF +

J6-23 O REF -

J6-22 O REF GND

J6-21 O REF +

J6-20 O REF -

J6-19 O REF GND

J6-18 O REF +

J6-17 O REF -

J6-16 O REF GND

J6-15 O REF +

J6-14 O REF -

J6-13 O REF GND

J6-12 O REF +

J6-11 O REF -

J6-10 O REF GND

J6-9 O REF +

J6-8 O REF -

J6-7 O REF GND

J6-6 O REF +

J6-5 O REF -

J6-4 O REF GND

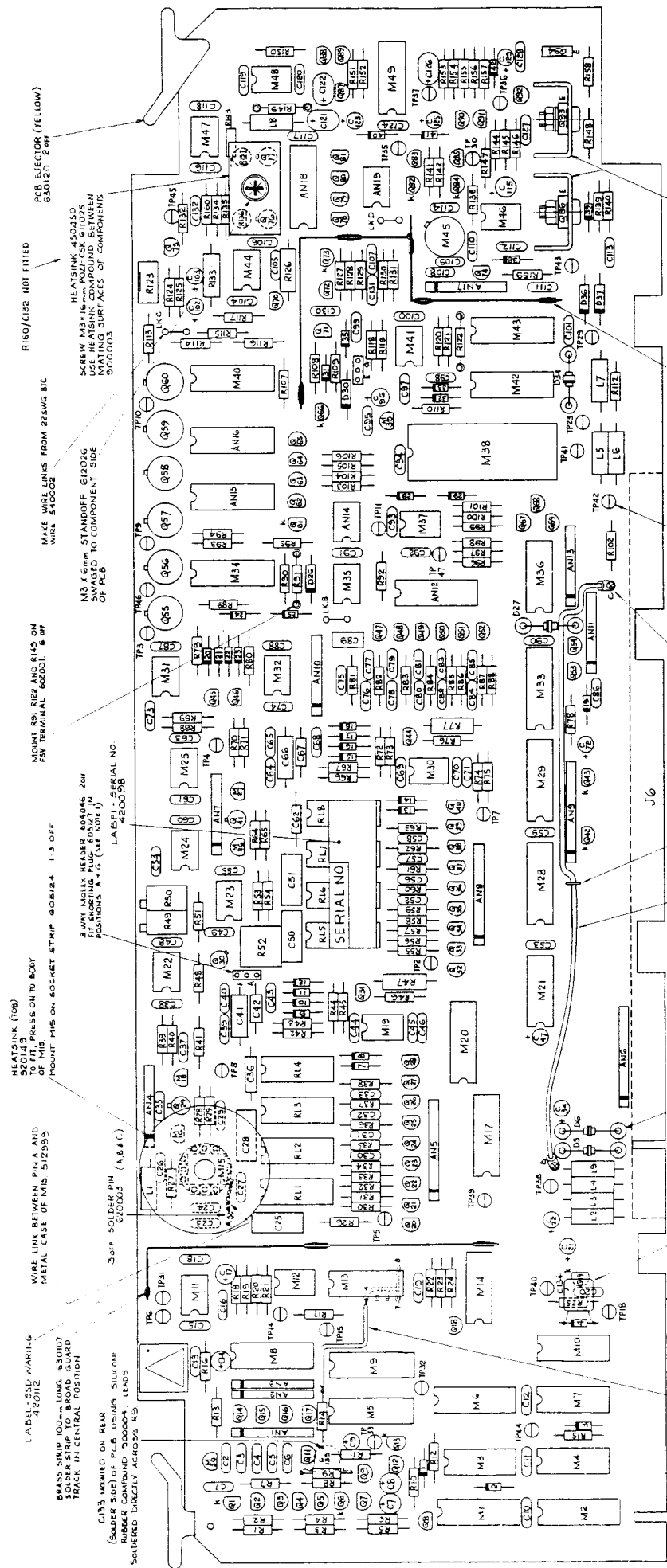
J6-3 O REF +

J6-2 O REF -

J6-1 O REF GND

SINE SOURCE ASSEMBLY

NOTE: FIT LINK P AND LINK F IN P LINK W AND LINK G FOR T



HEATSINK (YELLOW)
650120 2.47

HEATSINK 450140
USE HEATSINK COMPOUND BETWEEN MATING SURFACES OF COMPONENTS 500003

HEATSINK 450140
SCREW M3 X 0.5 PZ+CSK 501205
USE HEATSINK COMPOUND BETWEEN MATING SURFACES OF COMPONENTS 500003

M3 X 0.5mm STANDOFF 610206
SWAGED TO COMPONENT SIDE OF PCB

MAKE WIRE LINKS FROM 22AWG BIC WIRE 540002

MOUNT BRN R27 AND R145 ON FRY TERMINAL 620001 1.6 077

M3 X 0.5mm STANDOFF 610206 SWAGED TO COMPONENT SIDE OF PCB

3-WAY MOLEX HEADER 804046 20x FIT SHORTING PLUG 804027 IN POSITIONS A T G (SEE NOTE 1)

HEATSINK (108) 520145
MOUNT 108 IN SOCKET STRIP 608124 1.3 077
OF M15 PRESS ON TO BODY MOUNT THIS ON SOCKET STRIP 608124 1.3 077

WIRE LINK BETWEEN PH1A AND METAL CASE OF M15 512395

3-WAY MOLEX HEADER 804046 20x FIT SHORTING PLUG 804027 IN POSITIONS A T G (SEE NOTE 1)

WIRE LINK 7/0.2mm PTFE WIRE WIRE 512392

TEST POINT TERMINAL 620007 32 077

SLIP ON END OF THIS WIRE WITH 1/2 PIECE OF SLEEVING 550001

WIRE LINK 7/0.2mm PTFE WIRE WIRE 512392

MOUNT D5 D6 D7 1 D34 ON CERAMIC BEAD 630024 8 077

WIRE LINK 7/0.2mm PTFE WIRE WIRE 512392

HEATSINK 450140
SCREW M3 X 0.5 PZ+CSK 501205
USE HEATSINK COMPOUND BETWEEN MATING SURFACES OF COMPONENTS 500003

HEATSINK 10220 920083
SCREW M3 X 0.5 PZ+CSK 501205
M3 SHAKEN 613003 2.077
N.B. USE HEATSINK COMPOUND 500003 BETWEEN MATING SURFACES OF 9267 693. MOUNT THEM SQUARELY ON HEATSINKS

GLASS BEAD 630024 FITTED TO EACH LEG OF THE CERAMIC BEAD 630024
C15 C19 C24 C45 C48 C53 C55 C59 C60 C63 C70 C87 C89 C90 C93 C94 C100 C91 C105 C115 C116 C118 C119 C124 C128 D4

HEATSINK (108) 520145
MOUNT 108 IN SOCKET STRIP 608124 1.3 077
OF M15 PRESS ON TO BODY MOUNT THIS ON SOCKET STRIP 608124 1.3 077

WIRE LINK BETWEEN PH1A AND METAL CASE OF M15 512395

3-WAY MOLEX HEADER 804046 20x FIT SHORTING PLUG 804027 IN POSITIONS A T G (SEE NOTE 1)

WIRE LINK 7/0.2mm PTFE WIRE WIRE 512392

TEST POINT TERMINAL 620007 32 077

SLIP ON END OF THIS WIRE WITH 1/2 PIECE OF SLEEVING 550001

WIRE LINK 7/0.2mm PTFE WIRE WIRE 512392

MOUNT D5 D6 D7 1 D34 ON CERAMIC BEAD 630024 8 077

WIRE LINK 7/0.2mm PTFE WIRE WIRE 512392

HEATSINK 450140
SCREW M3 X 0.5 PZ+CSK 501205
USE HEATSINK COMPOUND BETWEEN MATING SURFACES OF COMPONENTS 500003

HEATSINK 10220 920083
SCREW M3 X 0.5 PZ+CSK 501205
M3 SHAKEN 613003 2.077
N.B. USE HEATSINK COMPOUND 500003 BETWEEN MATING SURFACES OF 9267 693. MOUNT THEM SQUARELY ON HEATSINKS

GLASS BEAD 630024 FITTED TO EACH LEG OF THE CERAMIC BEAD 630024
C15 C19 C24 C45 C48 C53 C55 C59 C60 C63 C70 C87 C89 C90 C93 C94 C100 C91 C105 C115 C116 C118 C119 C124 C128 D4

LABEL-552 MARKING 42012

BRASS STRIP 100mm LONG 530017
SOLDER STRIP TO BRASS GUARD TRACK IN CENTRAL POSITION

C133 MOUNTED ON REAR (SOLDER SIDE) OF PCB USING SILICONE BEAD COMPOUND 500003. LEADS SOLDERED DIRECTLY AGAINST PINS

WIRE LINK 7/0.2mm PTFE WIRE WIRE 512392

TEST POINT TERMINAL 620007 32 077

SLIP ON END OF THIS WIRE WITH 1/2 PIECE OF SLEEVING 550001

WIRE LINK 7/0.2mm PTFE WIRE WIRE 512392

MOUNT D5 D6 D7 1 D34 ON CERAMIC BEAD 630024 8 077

WIRE LINK 7/0.2mm PTFE WIRE WIRE 512392

HEATSINK 450140
SCREW M3 X 0.5 PZ+CSK 501205
USE HEATSINK COMPOUND BETWEEN MATING SURFACES OF COMPONENTS 500003

HEATSINK 10220 920083
SCREW M3 X 0.5 PZ+CSK 501205
M3 SHAKEN 613003 2.077
N.B. USE HEATSINK COMPOUND 500003 BETWEEN MATING SURFACES OF 9267 693. MOUNT THEM SQUARELY ON HEATSINKS

GLASS BEAD 630024 FITTED TO EACH LEG OF THE CERAMIC BEAD 630024
C15 C19 C24 C45 C48 C53 C55 C59 C60 C63 C70 C87 C89 C90 C93 C94 C100 C91 C105 C115 C116 C118 C119 C124 C128 D4

WIRE LINK 7/0.2mm PTFE WIRE WIRE 512392

TEST POINT TERMINAL 620007 32 077

SLIP ON END OF THIS WIRE WITH 1/2 PIECE OF SLEEVING 550001

WIRE LINK 7/0.2mm PTFE WIRE WIRE 512392

MOUNT D5 D6 D7 1 D34 ON CERAMIC BEAD 630024 8 077

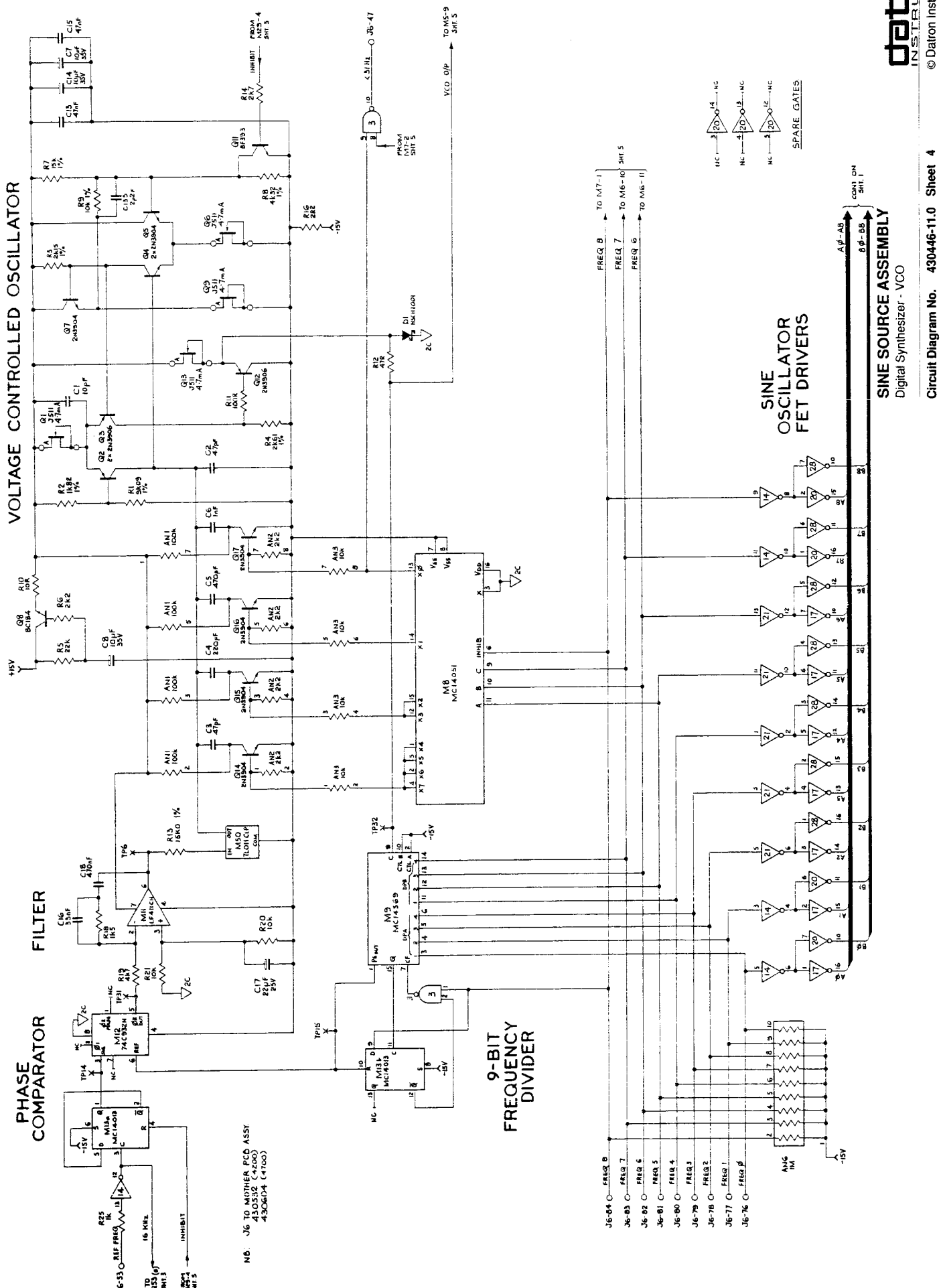
WIRE LINK 7/0.2mm PTFE WIRE WIRE 512392

| MOUNTING IC-1 | PART NO | WHERE USED |
|---------------|---------|--|
| 8 | 605059 | M11, M19, M22-25, M30, M31, M32, M35, M37 |
| 14 | 605060 | M41, M44, M45, M47, M48, M12 |
| 16 | 605061 | M1, M4, M7, M10, M13, M14, M21, M36, M49 |
| 28 | 605065 | M1, M2, M3, M6, M8, M15, M17, M20, M28, M29, M33, M34, M40, M42, M43 |

FIT 1/0.4 PTH BLACK WIRE BETWEEN R14 AND M15 PH4 340006. CUT TRACK TO M15 PH4 ON SOLDER SIDE OF BOARD. NO THROUGH

MOUNT C134 ON TOP OF COMPS SHOWN

PCB 410171-B



SINE SOURCE ASSEMBLY
 Digital Synthesizer - VCO
 Circuit Diagram No. 430446-11.0 Sheet 4

SINE SOURCE ASSEMBLY

NOTE: FIT LINK 'E' AND LINK 'F' IN P
LINK 'X' AND LINK 'G' FOR 1

LABEL-35D VARIATOR
470172

BRASS STRIP 100--LONG 630107
SOLDER STRIP TO BROAD GUARD
TRACK IN CENTRAL POSITION

C185 MOUNTED ON HEAT
SHIELDING (600000)
BARBER CODED PCB USHINS SILICONE
LEADS
SOLDERED DIRECTLY ACROSS RS.

WIRE LINK BETWEEN PIN A AND
METAL CASE OF M15 512953

3-0P 601005 PIN
620003 (A,B,C)

HEATSINK (108)
520149
PRESS ON TO BODY
OF M15

POINT THIS ON SOCKET STRIP
#08124 1-3 OFF

3-PIN WIRE: HEADER 654146
FIT SHORTEST PLUS 60527 IN
POSITIONS A, B, C (SEE NOT 1)
LABEL-SERIAL NO.
420058

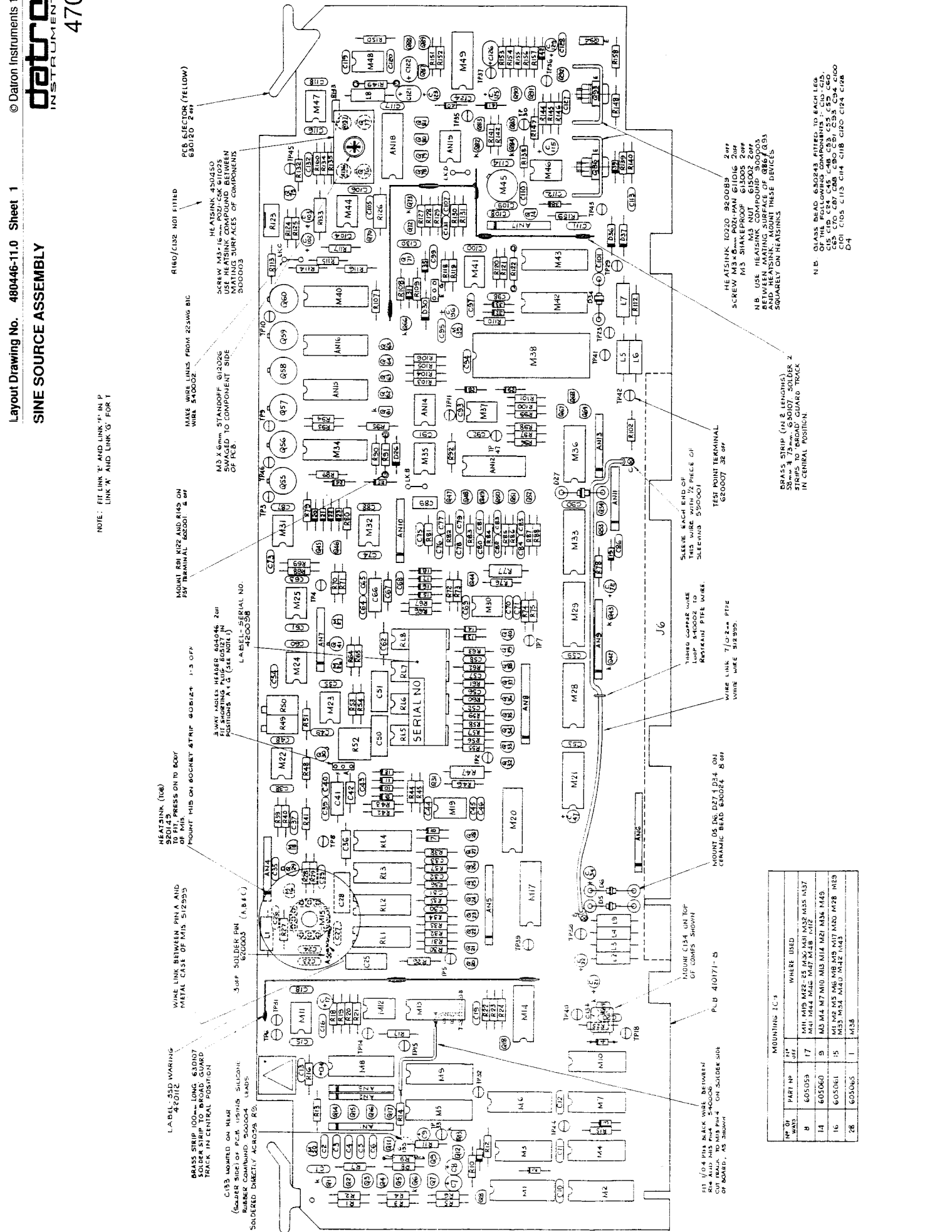
MOUNT RFI K122 AND R145 ON
TOP TERMINAL HEADS 8 OFF

M3 X 6mm STANDOFF 612026
MOUNTED TO COMPONENT SIDE
OF PCB

HEATSINK 430450
SCREW M3 X 6mm POSZ-CHK 61075
MOUNTED TO MATING SURFACES OF
COMPONENTS
300003

RIBO/C182 NOT FITTED

PCB SELECTOR (YELLOW)
630120 2-0H



HEATSINK TO BEAD 630243
FITTED TO EACH LEG
OF THE FOLLOWING COMPONENTS: C10, C15,
C16, C17, C18, C19, C20, C21, C22, C23, C24, C25,
C26, C27, C28, C29, C30, C31, C32, C33, C34, C35,
C36, C37, C38, C39, C40, C41, C42, C43, C44, C45,
C46, C47, C48, C49, C50, C51, C52, C53, C54, C55,
C56, C57, C58, C59, C60, C61, C62, C63, C64, C65,
C66, C67, C68, C69, C70, C71, C72, C73, C74, C75,
C76, C77, C78, C79, C80, C81, C82, C83, C84, C85,
C86, C87, C88, C89, C90, C91, C92, C93, C94, C95,
C96, C97, C98, C99, C100, C101, C102, C103, C104,
C105, C106, C107, C108, C109, C110, C111, C112, C113,
C114, C115, C116, C117, C118, C119, C120, C121, C122

HEATSINK 10220 930084
2-0H
SCREW M3 X 6mm POSZ-PAN 61016 2-0H
M3 SHAK-PROOF 61005 2-0H
M3 NUT 61502 2-0H
M3 WASHER 61503 2-0H
N.B. USE HEATSHIELDING STRIP
BETWEEN MATING SURFACE OF Q86/Q89
AND HEATSINK. MOUNT THESE DEVICES
SQUARELY ON HEATSINKS

N.B. GLASS BEAD 630243
FITTED TO EACH LEG
OF THE FOLLOWING COMPONENTS: C10, C15,
C16, C17, C18, C19, C20, C21, C22, C23, C24, C25,
C26, C27, C28, C29, C30, C31, C32, C33, C34, C35,
C36, C37, C38, C39, C40, C41, C42, C43, C44, C45,
C46, C47, C48, C49, C50, C51, C52, C53, C54, C55,
C56, C57, C58, C59, C60, C61, C62, C63, C64, C65,
C66, C67, C68, C69, C70, C71, C72, C73, C74, C75,
C76, C77, C78, C79, C80, C81, C82, C83, C84, C85,
C86, C87, C88, C89, C90, C91, C92, C93, C94, C95,
C96, C97, C98, C99, C100, C101, C102, C103, C104,
C105, C106, C107, C108, C109, C110, C111, C112, C113,
C114, C115, C116, C117, C118, C119, C120, C121, C122

GRASS STRIP (IN 2 LENGTHS)
50mm x 75mm 630007 SOLDER 2
IN CENTRAL POSITION

SLICER, EACH END OF
THIS WIRE WITH 1/2 PIECE OF
SLEEVING 550001

TEST POINT TERMINAL
620007 38 OFF

WIRE LINK 7132-20 PTFE
WIRE WIRE 512952

TRUNK WIRE
LOOP 840022 TO
RESTRAIN PIPE WIRE.

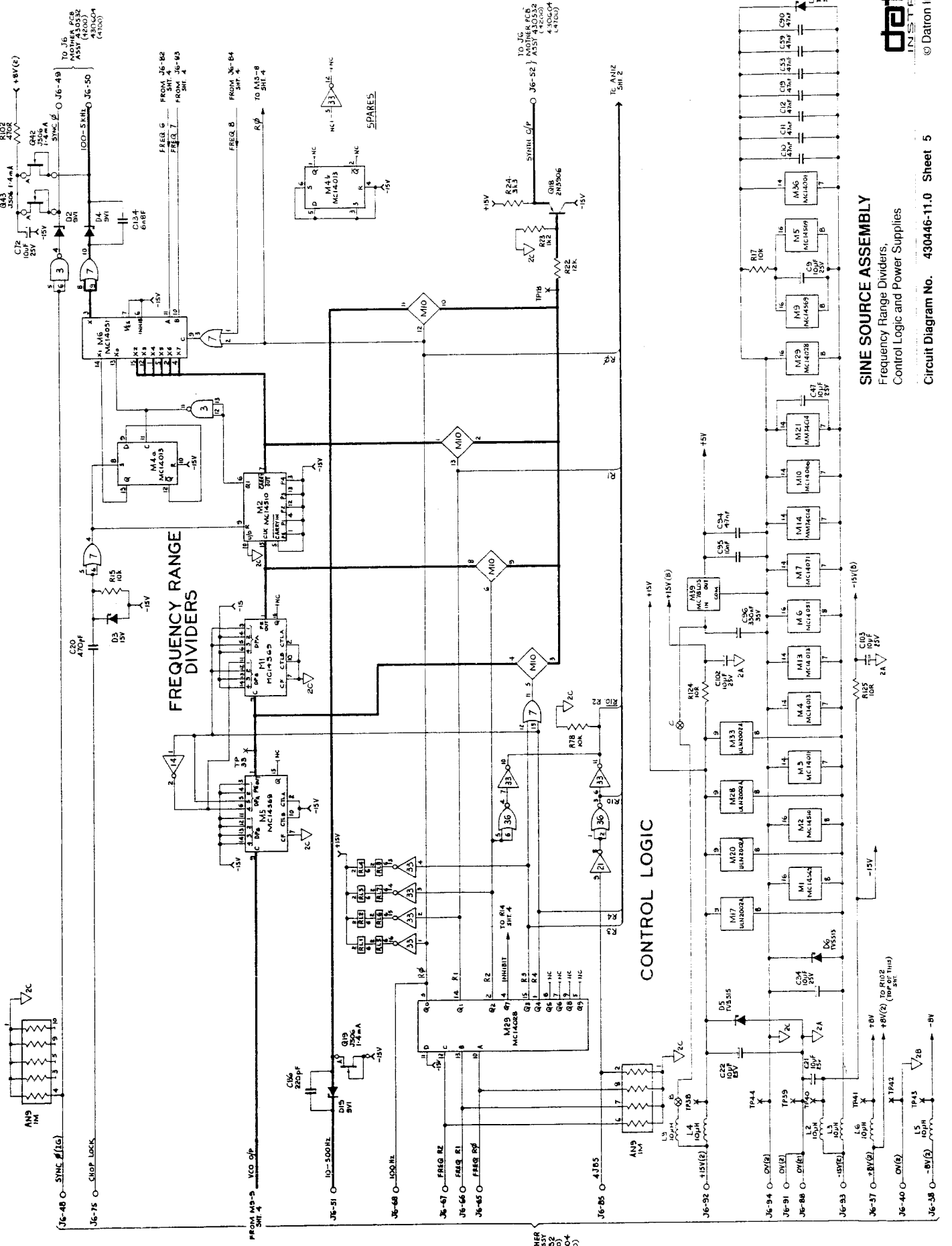
MOUNT D5 LK D27 1 D34 ON
CERAMIC BEAD 630024 8 OFF

MOUNT C134 ON TOP
OF COMPS SHOWN

PLB 410171-5

FIT 1/4 PHS BLACK WIRE BETWEEN
R16 AND M15 PER PIN 4 ON SOLDER SHI
OF BOARD, AS SHOWN

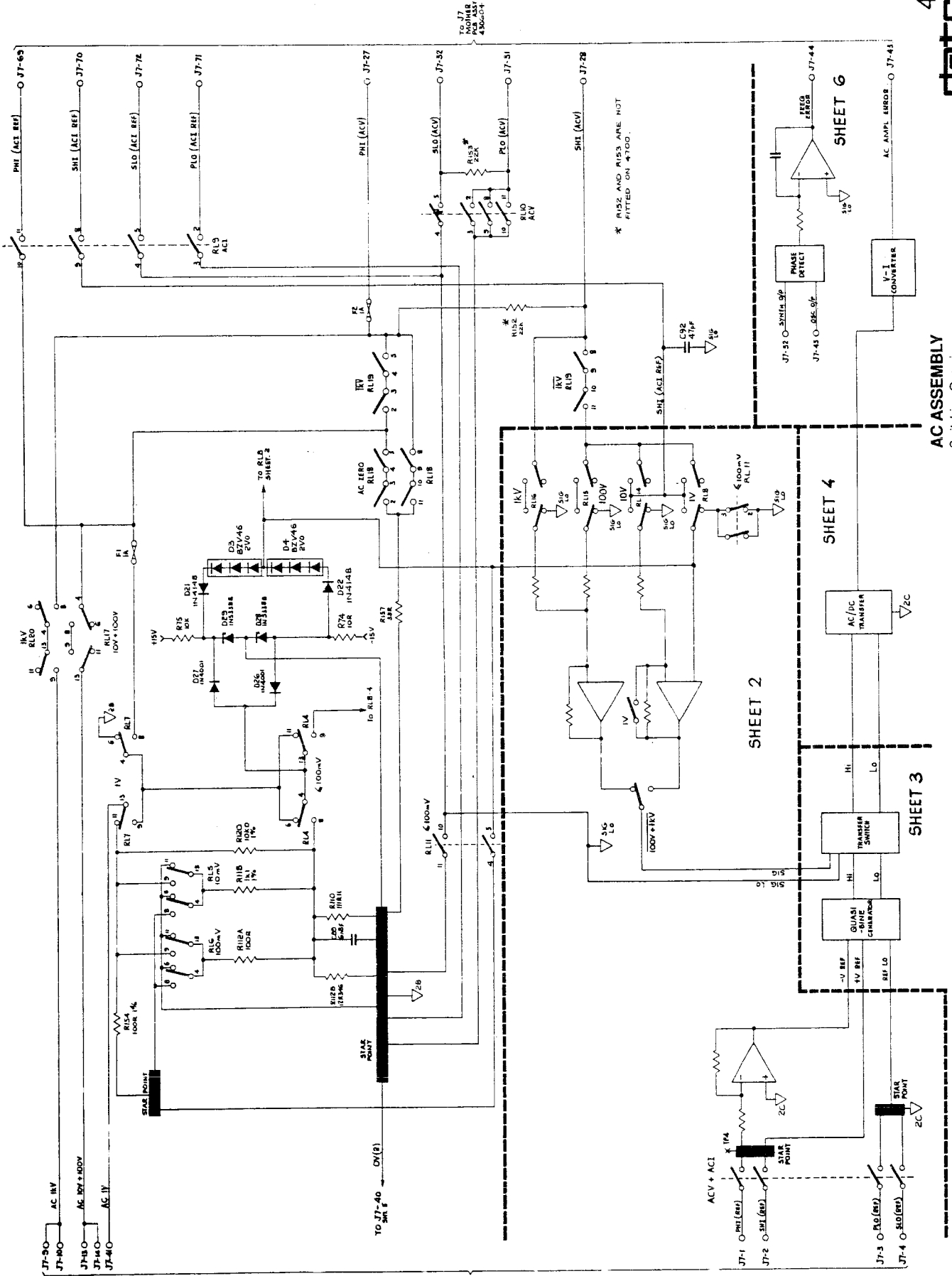
| MP TO WAS | PART NO | WHERE USED |
|--------------|---------|--|
| 8 | 605059 | M11, M15, M22-25, M30, M31, M32, M33, M37 |
| 14 | 605060 | M3, M4, M7, M10, M13, M14, M21, M36, M45 |
| 16 | 605061 | M1, M2, M5, M6, M8, M9, M17, M20, M28, M29 |
| 28 | 605065 | M35, M34, M40, M42, M43 |



SINE SOURCE ASSEMBLY
 Frequency Range Dividers,
 Control Logic and Power Supplies

Circuit Diagram No. 430446-11.0 Sheet 5

J6
 36 MOTHER
 PCB ASSY
 430446-11.0
 430446-11.0
 430446-11.0



TO J7
ADDRESS
430604

AC ASSEMBLY

N.B. GLASS BEAD RESISTS FITTED TO EACH LEG
C6, J1, J4, 20, 24, 27, 29, 35, 36, 40, 42, 43, 83, 84.

MS 14mm STAINLESS STEEL GROMMET
TO BE SWARDED TO 41017Z

USE HEADSHRINK SLEEVE
Ø 3.2 PART IN 500001

WELD WIRES TOGETHER
WITH SOLDER

INSERT LEG OF R111
INTO SWITCH MOUNTING
ENSURE ALL PINS UNDER
SOLDER

COB MARKED ON UNDER
SIDE OF PCB WITH WHITE
SILVER SLEEVE

COB MARKED ON UNDER
SIDE OF PCB WITH WHITE
SILVER SLEEVE

CUT TRACK AS SHOWN ABOVE
COMPARING PART SIZES
WITH MAIN PCB

BLUB OF SILICONE RUBBER
3000000 MOUNT SHUNTING
3000000 BETWEEN EX/103 &
2000000

DETAIL OF HEIGHT RESTRICTION
ON PIGTAIL-BACK AC RMS SENSE
PCB

INDICATES WIRE CONNECTIONS
FROM PIGTAIL BACK TO MAIN PCB
REFER MAIN PCB ONLY

AC RMS SENSE PCB ASSEMBLY
400B-42

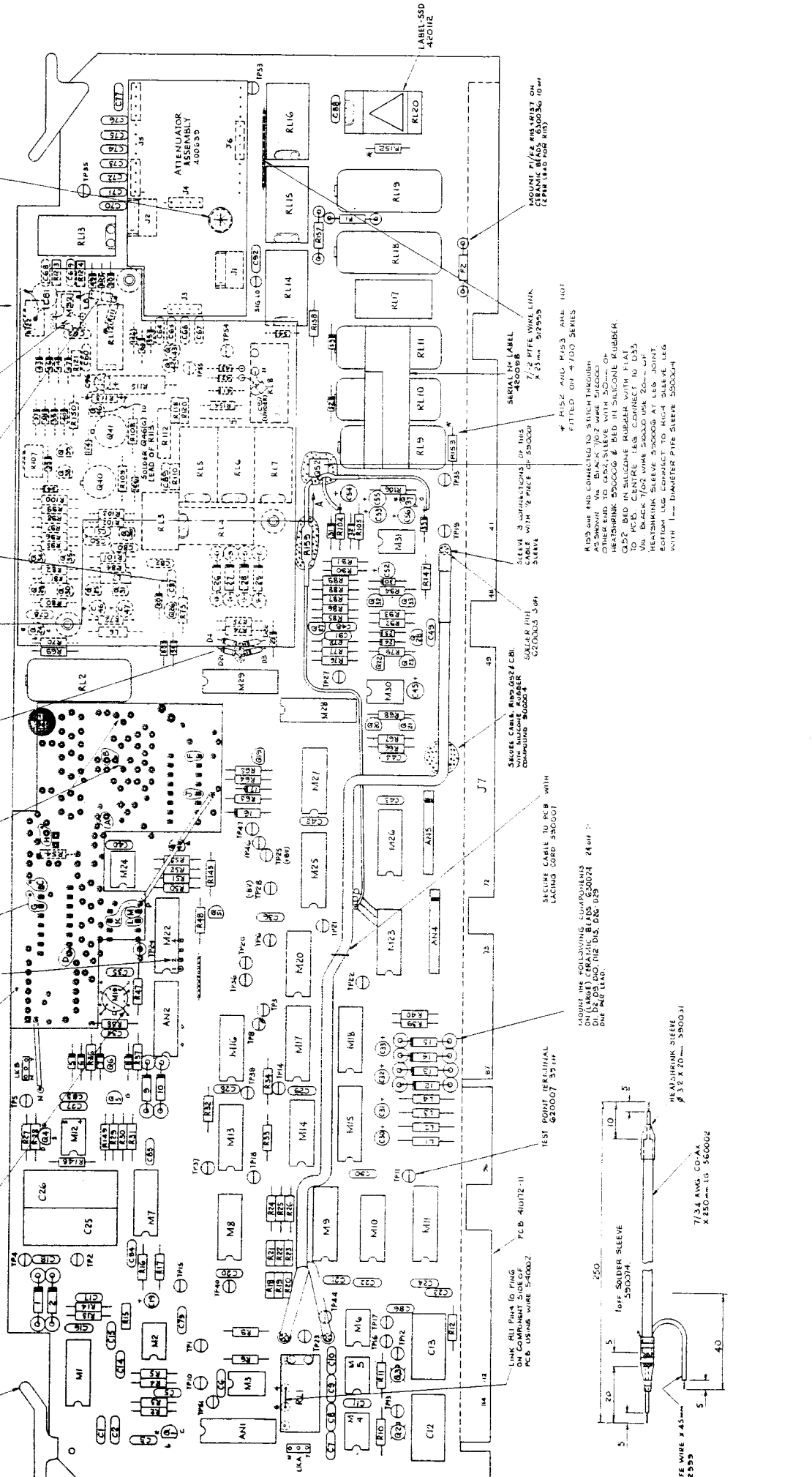
LINK ALL PINS TO PING
PCB USING WIRE 5-9000Z

PCB 41017Z-11

LINK ALL PINS TO PING
PCB USING WIRE 5-9000Z

HEADSHRINK SLEEVE
Ø 3.2 X 2.0mm 3900031

7/32" ANGLE COAXIAL
X 250mm LG 3600002



SECTION A-A

SLEEVE LEAD
390004

(GREEN) CIRCUIT BOARD EJECTOR
Ø 3.0127 204

LABEL 55D
420112

SERIAL TAG LABEL
4200008
7/2 PTFE WIRE LINK
X 25mm 92959

SLEEVE 3 COMPARE 2000 OF THIS
CABLE WITH 2 PICE OF 500001
SLEEVE

R103 AND R105 ARE NOT
FITTED FOR 4700 SERIES

R103 ARE NOT CONNECTED TO SWITCH THROUGH
AS SHOWN VIA BLANK 7/02 WIRE 510000
OTHER END TO CASE SLEEVE WITH 300000
OTHER END TO CASE SLEEVE WITH 300000
Ø 5.2 PART IN 50001 & RED SILICONE RUBBER
TO PCB CENTRE LEG CONTACT 10 D33
VIA BLACK 7/02 WIRE 50000 USE 20mm OF
HEADSHRINK SLEEVE 390003 AT LEG JOINT
BOTTOM LEG CONNECT TO HIGH SLEEVE LEG
WITH 1mm DIAMETER PIPE SLEEVE 390004

SOLDER CABLE 4000002 PCB
COMPARING 500001

SLEEVE CABLE NO. 509
LACKING CORD 390000

TEST POINT RESISTORIAL
Ø 2.0007 92716

LINK ALL PINS TO PING
PCB USING WIRE 5-9000Z

PCB 41017Z-11

HEADSHRINK SLEEVE
Ø 3.2 X 2.0mm 3900031

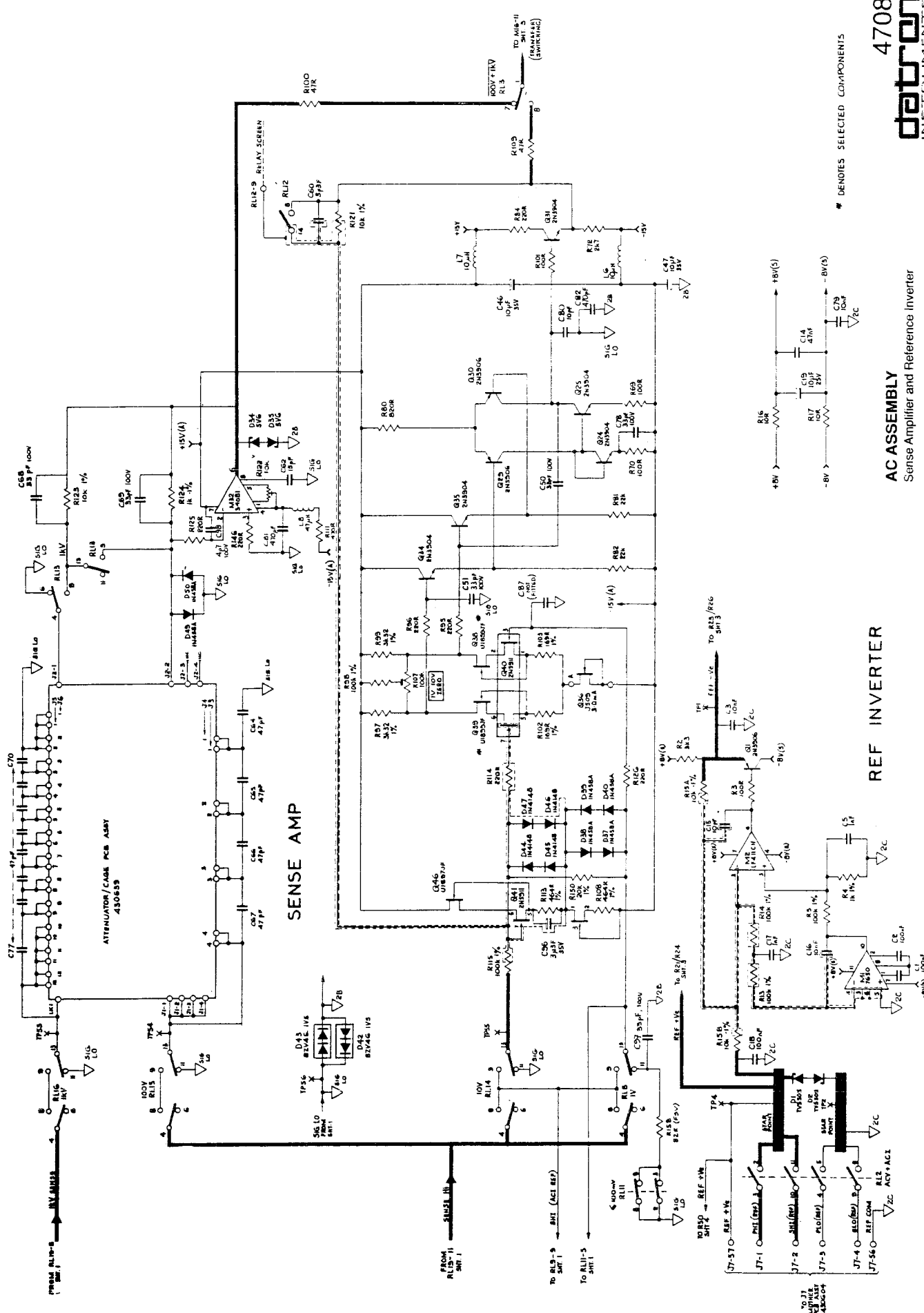
7/32" ANGLE COAXIAL
X 250mm LG 3600002

10FT SOLDER SLEEVE
390004

HEADSHRINK SLEEVE
Ø 3.2 X 2.0mm 3900031

7/32" ANGLE COAXIAL
X 250mm LG 3600002

MOUNT P1/2 PINS 41617 ON
CERAMIC BLADES 650030 (Ø 2mm
LEAD FOR 41617)

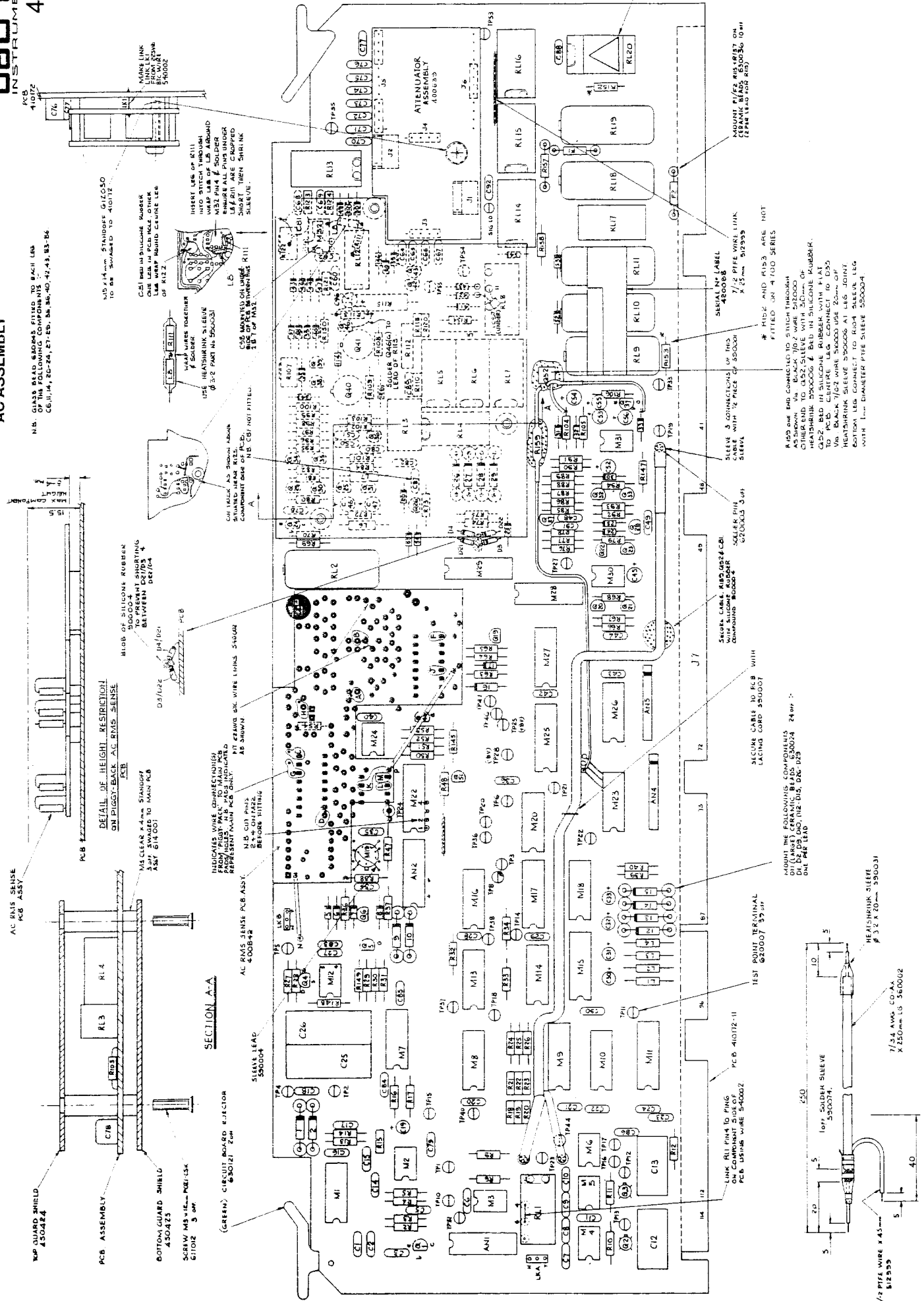


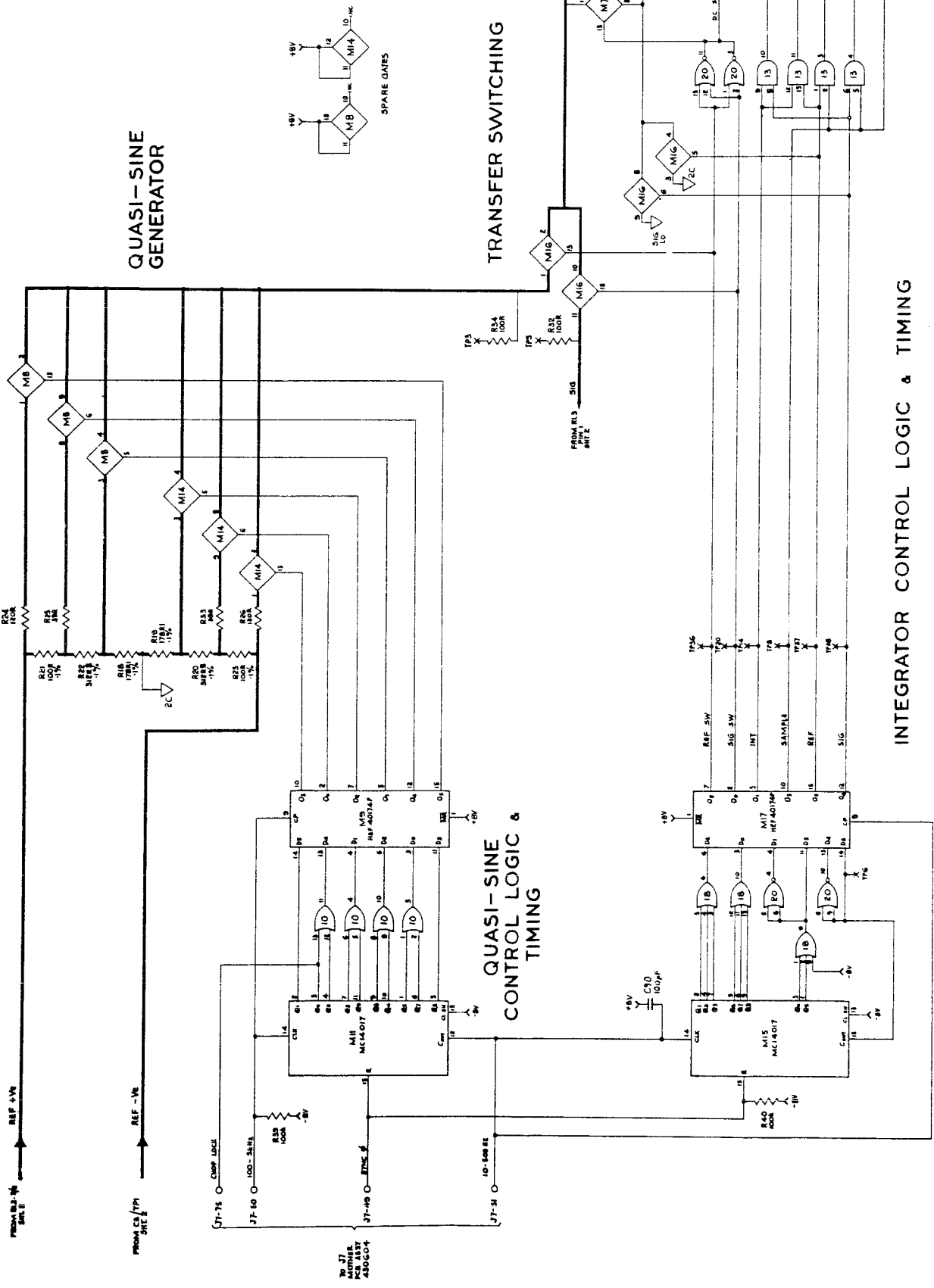
REF INVERTER

AC ASSEMBLY
Sense Amplifier and Reference Inverter

* DENOTES SELECTED COMPONENTS

AC ASSEMBLY

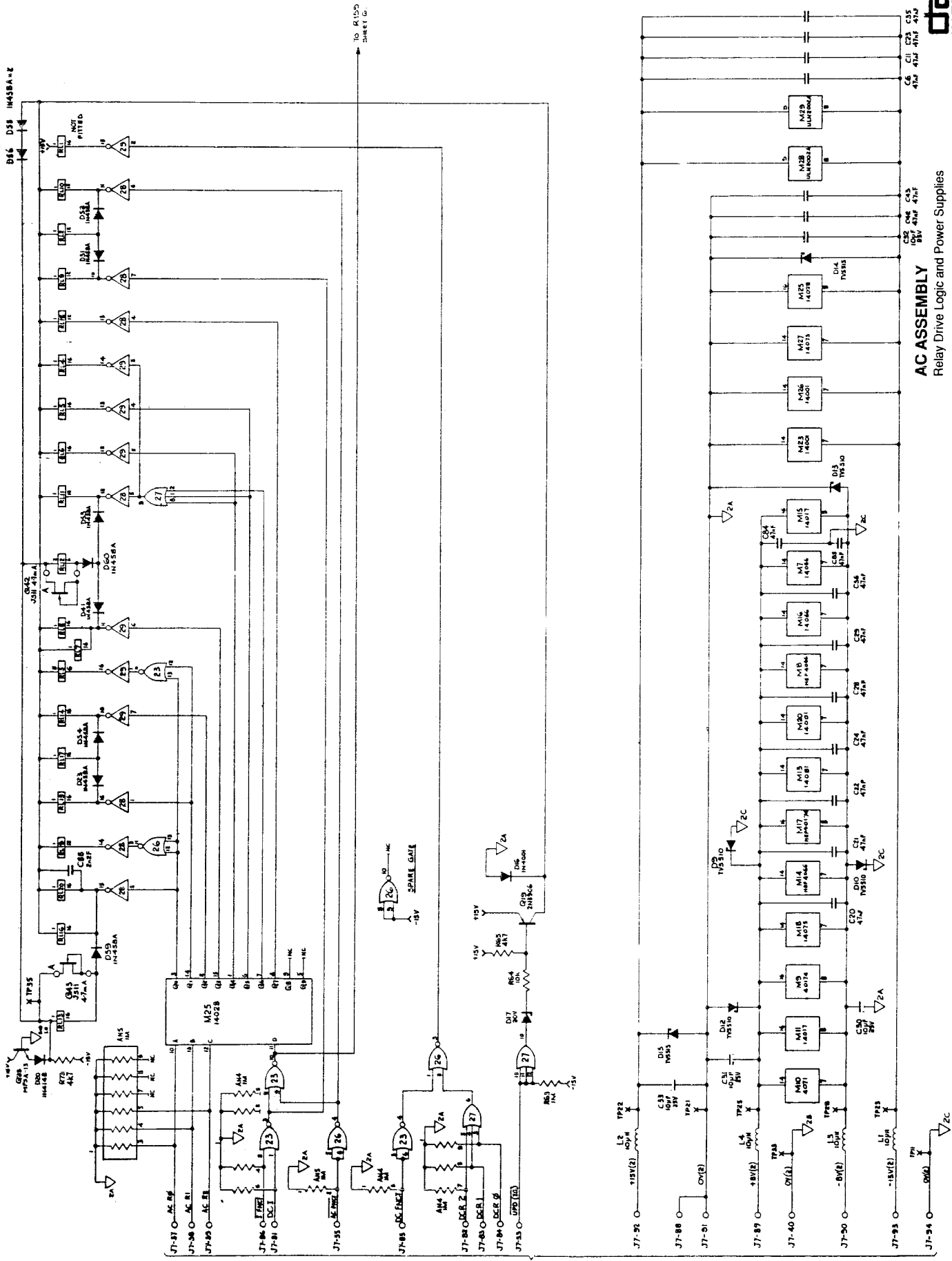




INTEGRATOR CONTROL LOGIC & TIMING

AC ASSEMBLY
Quasi-Sine Generator and Timing Logic

Circuit Diagram No. 430844-1.0 Sheet 3



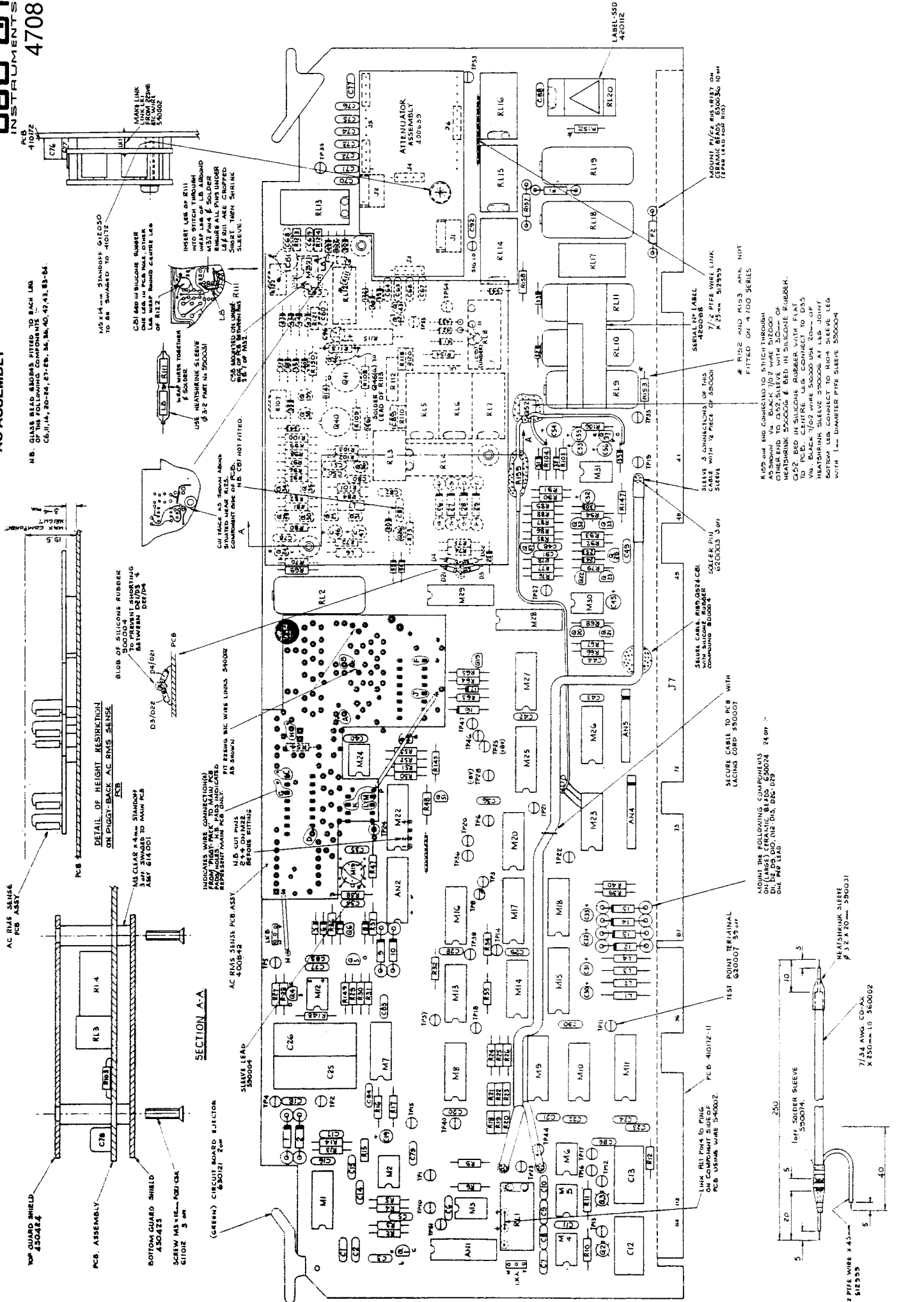
AC ASSEMBLY
 Relay Drive Logic and Power Supplies
 Circuit Diagram No. 430844-1.0 Sheet 5

TO J7
 MONTAGE
 PCB LAYOUT
 430844-1.0



4708

AC ASSEMBLY



N.B. GLASS BEAD BEADS FITTED TO EACH LEG OF THE FOLLOWING COMPONENTS: C6, J1, J4, J7, J8, J9, J10, J11, J12, J13, J14, J15, J16, J17, J18, J19, J20, J21, J22, J23, J24, J25, J26, J27, J28, J29, J30, J31, J32, J33, J34, J35, J36, J37, J38, J39, J40, J41, J42, J43, J44, J45, J46, J47, J48, J49, J50, J51, J52, J53, J54, J55, J56, J57, J58, J59, J60, J61, J62, J63, J64, J65, J66, J67, J68, J69, J70, J71, J72, J73, J74, J75, J76, J77, J78, J79, J80, J81, J82, J83, J84, J85, J86, J87, J88, J89, J90, J91, J92, J93, J94, J95, J96, J97, J98, J99, J100

MS24mm STANDOFF 410172 TO BE SWAGED TO 40172

USE HEATSHRINK SLEEVE # 30489 TO PROTECT SHORTING BETWEEN DET/DA AND PCB

INDICATES WIRE CONNECTIONS FROM MAIN PCB ONLY. FIT REMAINING WIRE LINGS 54000E AS SHOWN.

N.B. CUT PINS 544-01422 BEFORE FITTING

SECURE CABLE BENDS 40254C81 WITH SILICONE RUBBER GROUNDING BRIDGE

SECURE CABLE TO PCB WITH LACING CORD 450007

TEST POINT TERMINAL 620007 59 01

LINK ALL PINS TO PINS ON COMPACT SILENCE PCB USING WIRE 540002

MONITOR THE FOLLOWING COMPONENTS ON (LARGE) CERAMIC BEADS: 650074 24 01

MONUMENT PINS (LARGE CERAMIC BEADS 650074 24 01) (SEE LEAD FOR R/S)

4 R102 AND R103 ARE NOT FITTED ON 4100 SERIES

8100mm SMC CONNECTED TO SWITCH THROUGH AN 8100mm SILENCE SLEEVE 512000 OF OTHER END TO 0.02 SLEEVE WITH 2.0mm OF HEATSHRINK 550006 & BED IN SILICONE RUBBER. C622, BED IN SILICONE RUBBER WITH FLAT 1.0mm OF SILICONE RUBBER. VIB. BACK 1/62 WIRE 500000 USE 50mm OF HEATSHRINK SLEEVE 550006 AT LBS JOINT. BOTTOM LEG CONNECT TO RIGHT SLEEVE LEG WITH 1mm DIAMETER PTFE SLEEVE 550004

SLAVE 3 CONNECTIONS OF THIS SLEEVE WITH 1/2 PIECE OF 580000 SILENCE SLEEVE

SERIAL N° LABEL 480844-1.2 WIRE LINK X 0.25mm 502993

ATTENUATOR ASSEMBLY 4004639

WOP GUARD SHIELD 450424

PCB ASSEMBLY

AC RMS SENSE PCB ASSY

DETAIL OF HEIGHT RESTRICTION ON PIGGY-BACK AC RMS SENSE PCB

BLOB OF SILICONE RUBBER 540004 TO PREVENT SHORTING BETWEEN DET/DA AND PCB

MS CLEAR 4.4mm STANDOFF 3 017 SWAGED TO MAIN PCB (LWS 614 001)

MS24mm STANDOFF 410172 TO BE SWAGED TO 40172

CAN END IN SILICONE RUBBER ON LEGS IN PCB HOLE. OTHER LEGS MUST BE IN CENTRE LEG OF R122

INSERT LEGS OF R111 INTO SWITCH THROUGH WAF LEGS OF LBS AROUND PERIPHERY OF PCB. REMOVED LEGS UNDER LBS R111 ARE CRIMPED SHORT. THEN SHRINK SLEEVE.

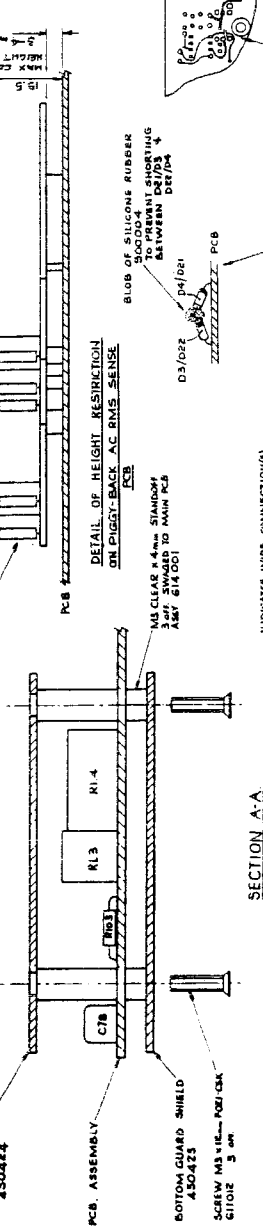
USE HEATSHRINK SLEEVE # 30489 TO PROTECT SHORTING BETWEEN DET/DA AND PCB

CAN END IN SILICONE RUBBER ON LEGS IN PCB HOLE. OTHER LEGS MUST BE IN CENTRE LEG OF R122

MARK LINK LINKER BEW/LEAD 540002

TOP GUARD SHIELD 450424

SECTION A-A



(GREEN) CIRCUIT BOARD SELECTOR 650121 20 01

SLEW LEAD 550004

AC RMS SENSE PCB ASSY 500542

INDICATES WIRE CONNECTIONS FROM MAIN PCB ONLY. FIT REMAINING WIRE LINGS 54000E AS SHOWN.

N.B. CUT PINS 544-01422 BEFORE FITTING

SECURE CABLE BENDS 40254C81 WITH SILICONE RUBBER GROUNDING BRIDGE

SECURE CABLE TO PCB WITH LACING CORD 450007

TEST POINT TERMINAL 620007 59 01

LINK ALL PINS TO PINS ON COMPACT SILENCE PCB USING WIRE 540002

MONITOR THE FOLLOWING COMPONENTS ON (LARGE) CERAMIC BEADS: 650074 24 01

MONUMENT PINS (LARGE CERAMIC BEADS 650074 24 01) (SEE LEAD FOR R/S)

4 R102 AND R103 ARE NOT FITTED ON 4100 SERIES

8100mm SMC CONNECTED TO SWITCH THROUGH AN 8100mm SILENCE SLEEVE 512000 OF OTHER END TO 0.02 SLEEVE WITH 2.0mm OF HEATSHRINK 550006 & BED IN SILICONE RUBBER. C622, BED IN SILICONE RUBBER WITH FLAT 1.0mm OF SILICONE RUBBER. VIB. BACK 1/62 WIRE 500000 USE 50mm OF HEATSHRINK SLEEVE 550006 AT LBS JOINT. BOTTOM LEG CONNECT TO RIGHT SLEEVE LEG WITH 1mm DIAMETER PTFE SLEEVE 550004

SLAVE 3 CONNECTIONS OF THIS SLEEVE WITH 1/2 PIECE OF 580000 SILENCE SLEEVE

SERIAL N° LABEL 480844-1.2 WIRE LINK X 0.25mm 502993

ATTENUATOR ASSEMBLY 4004639

WOP GUARD SHIELD 450424

PCB ASSEMBLY

AC RMS SENSE PCB ASSY

DETAIL OF HEIGHT RESTRICTION ON PIGGY-BACK AC RMS SENSE PCB

BLOB OF SILICONE RUBBER 540004 TO PREVENT SHORTING BETWEEN DET/DA AND PCB

MS CLEAR 4.4mm STANDOFF 3 017 SWAGED TO MAIN PCB (LWS 614 001)

MS24mm STANDOFF 410172 TO BE SWAGED TO 40172

CAN END IN SILICONE RUBBER ON LEGS IN PCB HOLE. OTHER LEGS MUST BE IN CENTRE LEG OF R122

INSERT LEGS OF R111 INTO SWITCH THROUGH WAF LEGS OF LBS AROUND PERIPHERY OF PCB. REMOVED LEGS UNDER LBS R111 ARE CRIMPED SHORT. THEN SHRINK SLEEVE.

USE HEATSHRINK SLEEVE # 30489 TO PROTECT SHORTING BETWEEN DET/DA AND PCB

CAN END IN SILICONE RUBBER ON LEGS IN PCB HOLE. OTHER LEGS MUST BE IN CENTRE LEG OF R122

MARK LINK LINKER BEW/LEAD 540002

TOP GUARD SHIELD 450424

PCB ASSEMBLY

AC RMS SENSE PCB ASSY

DETAIL OF HEIGHT RESTRICTION ON PIGGY-BACK AC RMS SENSE PCB

BLOB OF SILICONE RUBBER 540004 TO PREVENT SHORTING BETWEEN DET/DA AND PCB

MS CLEAR 4.4mm STANDOFF 3 017 SWAGED TO MAIN PCB (LWS 614 001)

MS24mm STANDOFF 410172 TO BE SWAGED TO 40172

CAN END IN SILICONE RUBBER ON LEGS IN PCB HOLE. OTHER LEGS MUST BE IN CENTRE LEG OF R122

INSERT LEGS OF R111 INTO SWITCH THROUGH WAF LEGS OF LBS AROUND PERIPHERY OF PCB. REMOVED LEGS UNDER LBS R111 ARE CRIMPED SHORT. THEN SHRINK SLEEVE.

USE HEATSHRINK SLEEVE # 30489 TO PROTECT SHORTING BETWEEN DET/DA AND PCB

CAN END IN SILICONE RUBBER ON LEGS IN PCB HOLE. OTHER LEGS MUST BE IN CENTRE LEG OF R122

MARK LINK LINKER BEW/LEAD 540002

TOP GUARD SHIELD 450424

PCB ASSEMBLY

AC RMS SENSE PCB ASSY

DETAIL OF HEIGHT RESTRICTION ON PIGGY-BACK AC RMS SENSE PCB

BLOB OF SILICONE RUBBER 540004 TO PREVENT SHORTING BETWEEN DET/DA AND PCB

MS CLEAR 4.4mm STANDOFF 3 017 SWAGED TO MAIN PCB (LWS 614 001)

MS24mm STANDOFF 410172 TO BE SWAGED TO 40172

CAN END IN SILICONE RUBBER ON LEGS IN PCB HOLE. OTHER LEGS MUST BE IN CENTRE LEG OF R122

INSERT LEGS OF R111 INTO SWITCH THROUGH WAF LEGS OF LBS AROUND PERIPHERY OF PCB. REMOVED LEGS UNDER LBS R111 ARE CRIMPED SHORT. THEN SHRINK SLEEVE.

USE HEATSHRINK SLEEVE # 30489 TO PROTECT SHORTING BETWEEN DET/DA AND PCB

CAN END IN SILICONE RUBBER ON LEGS IN PCB HOLE. OTHER LEGS MUST BE IN CENTRE LEG OF R122

MARK LINK LINKER BEW/LEAD 540002

TOP GUARD SHIELD 450424

PCB ASSEMBLY

AC RMS SENSE PCB ASSY

DETAIL OF HEIGHT RESTRICTION ON PIGGY-BACK AC RMS SENSE PCB

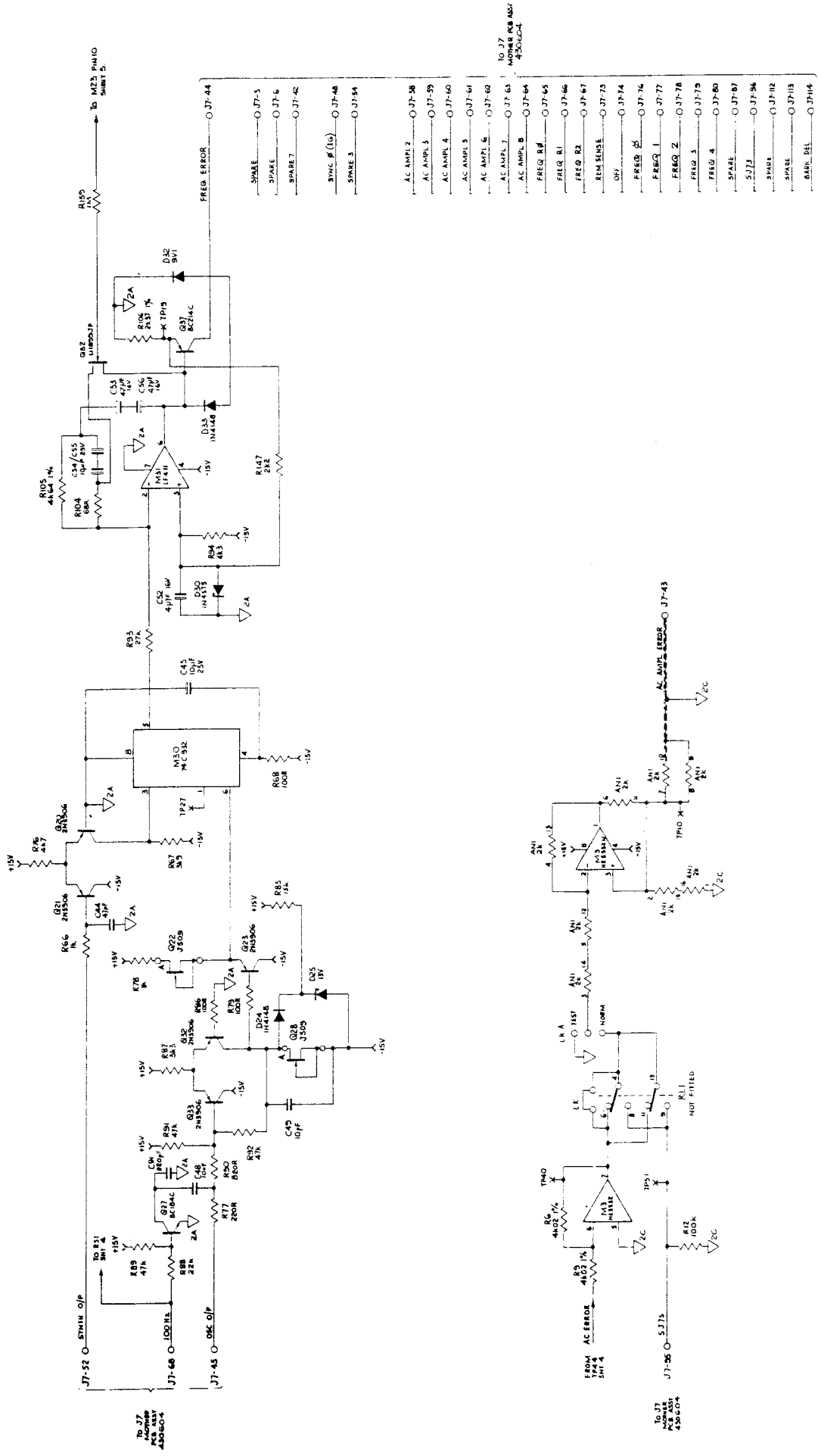
BLOB OF SILICONE RUBBER 540004 TO PREVENT SHORTING BETWEEN DET/DA AND PCB

MS CLEAR 4.4mm STANDOFF 3 017 SWAGED TO MAIN PCB (LWS 614 001)

MS24mm STANDOFF 410172 TO BE SWAGED TO 40172

CAN END IN SILICONE RUBBER ON LEGS IN PCB HOLE. OTHER LEGS MUST BE IN CENTRE LEG OF R122

7/32 PTFE WIRE X 4.3mm 512555 HEATSHRINK SLEEVE # 3.2 X 2.0mm 590031 7/32 AWG CO-AX X 250mm LG 560002



TO J7
PCB ASSY
4380604

TO J7
PCB ASSY
4380604

TO J7
MOTOR PCB ASSY
4380604

CURRENT / OHMS ASSEMBLY

| MP DE WAS | PART NO | MP OF | MP | MP NO | MP |
|-----------|---------|-------|-----|-------|-----|
| 14 | 605000 | 7 | M1 | M2 | M3 |
| 16 | 605001 | 3 | M12 | M13 | M14 |
| B | 605002 | 1 | M1 | M2 | M3 |
| ZO | 605010 | 2 | J13 | J14 | |

MOUNTING IS AS SHOWN IN FIG. 12.15.1
ON SMALL CERAMIC BEADS W-5002.26

NOTE: ALL CONNECTIONS TO SOLDER PINS TO BE SLEEVED USE 3189X 550001(02)

NOTE: ALL CONNECTIONS TO SOLDER PINS TO BE SLEEVED USE 3189X 550001(02)

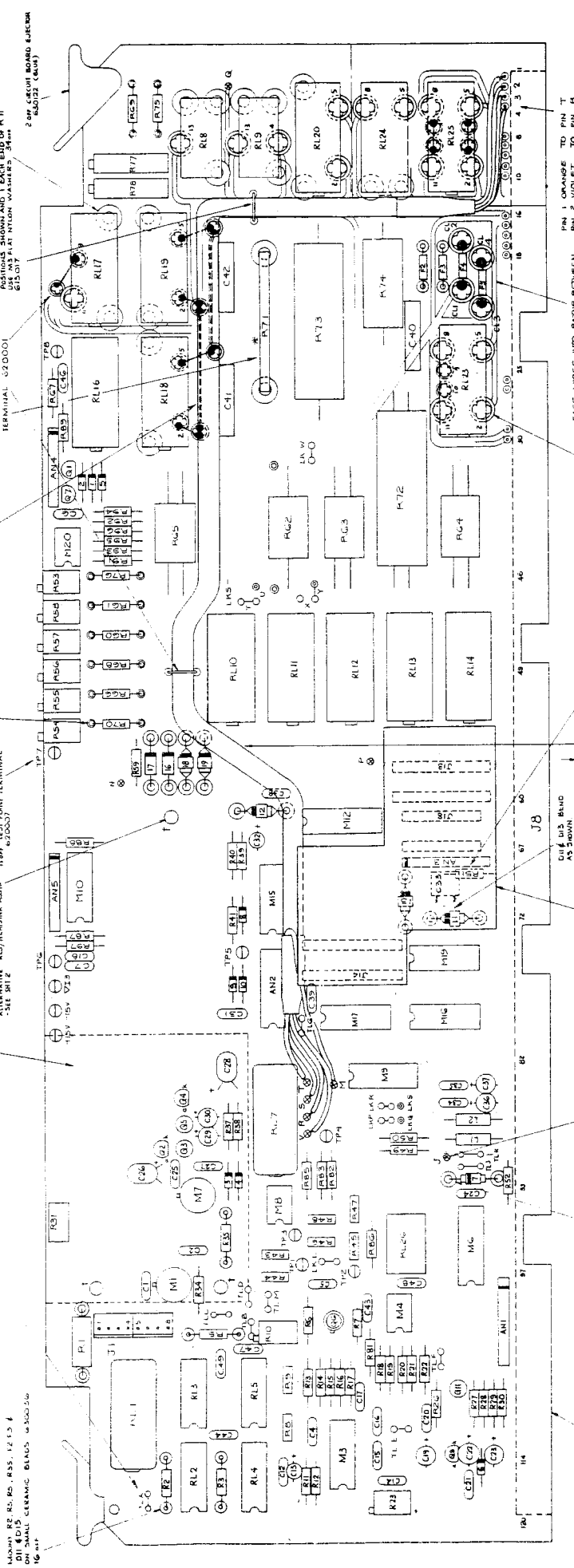
NOTE: ALL CONNECTIONS TO SOLDER PINS TO BE SLEEVED USE 3189X 550001(02)

NOTE: ALL CONNECTIONS TO SOLDER PINS TO BE SLEEVED USE 3189X 550001(02)

NOTE: ALL CONNECTIONS TO SOLDER PINS TO BE SLEEVED USE 3189X 550001(02)

NOTE: ALL CONNECTIONS TO SOLDER PINS TO BE SLEEVED USE 3189X 550001(02)

NOTE: ALL CONNECTIONS TO SOLDER PINS TO BE SLEEVED USE 3189X 550001(02)



NOTE: ALL CONNECTIONS TO SOLDER PINS TO BE SLEEVED USE 3189X 550001(02)

NOTE: ALL CONNECTIONS TO SOLDER PINS TO BE SLEEVED USE 3189X 550001(02)

NOTE: ALL CONNECTIONS TO SOLDER PINS TO BE SLEEVED USE 3189X 550001(02)

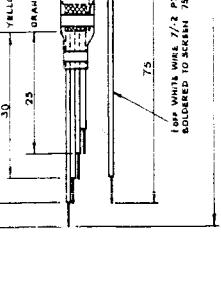
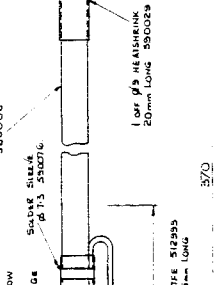
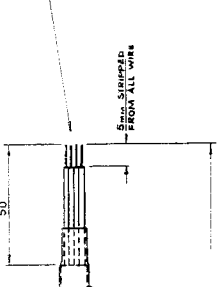
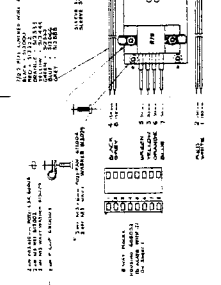
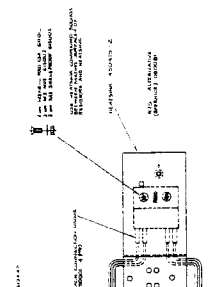
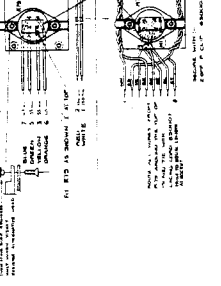
NOTE: ALL CONNECTIONS TO SOLDER PINS TO BE SLEEVED USE 3189X 550001(02)

NOTE: ALL CONNECTIONS TO SOLDER PINS TO BE SLEEVED USE 3189X 550001(02)

NOTE: ALL CONNECTIONS TO SOLDER PINS TO BE SLEEVED USE 3189X 550001(02)

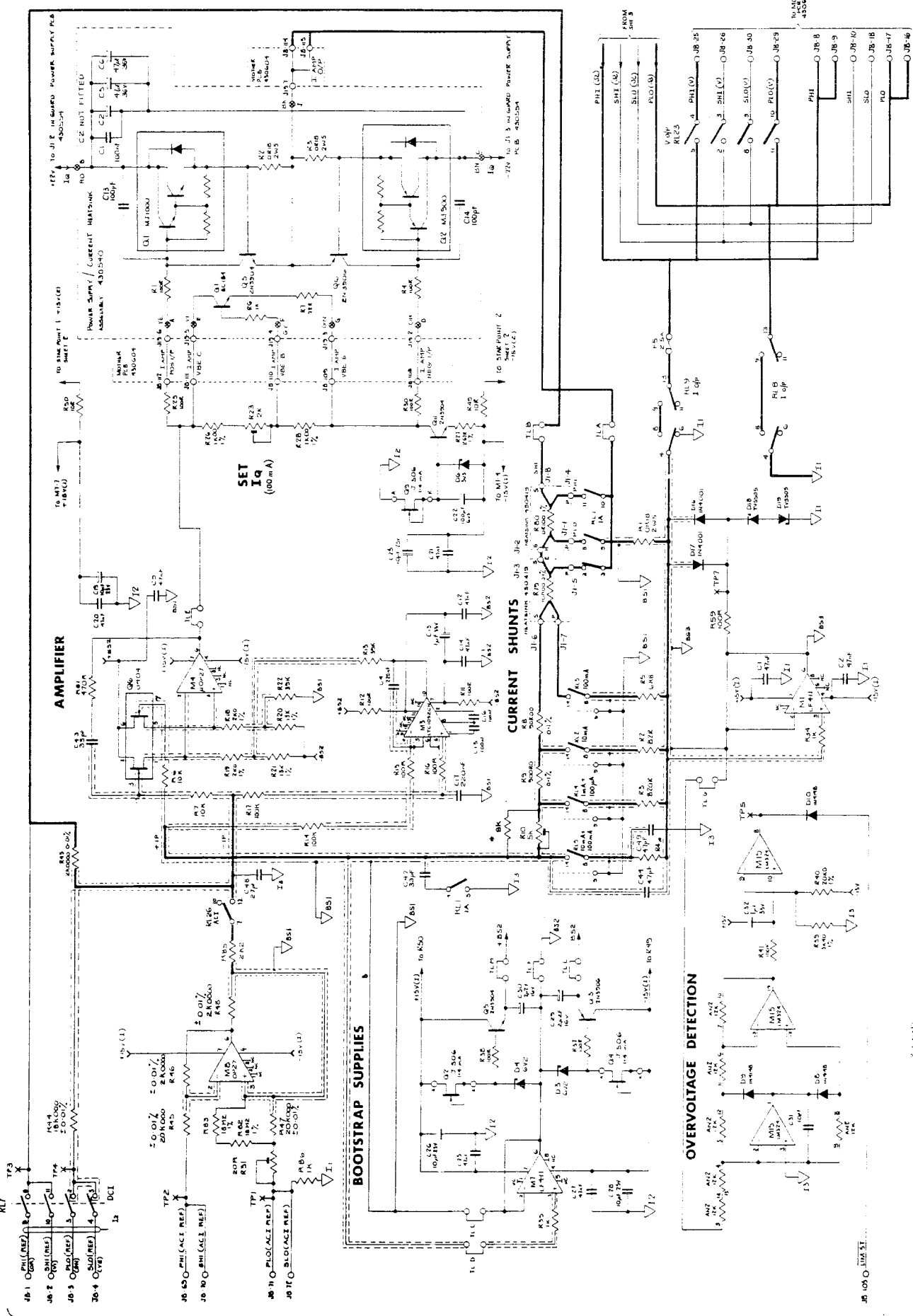
NOTE: ALL CONNECTIONS TO SOLDER PINS TO BE SLEEVED USE 3189X 550001(02)

NOTE: ALL CONNECTIONS TO SOLDER PINS TO BE SLEEVED USE 3189X 550001(02)



CURRENT / OHMS ASSEMBLY
 Voltage-to-Current Converter

Circuit Diagram No. 430614-1.1 Sheet 1



* INDICATES DEVICES NOT FITTED
 ON 4700

CURRENT / OHMS ASSEMBLY

| MOUNTING IC* | |
|-------------------|------------|
| WAFER WBS PART NO | IC PART NO |
| 14 | 605060 |
| 16 | 605061 |
| 8 | 605062 |
| 20 | 605063 |

MOUNT R2 R4 R5, R23, R24, R3
ON SMALL CERAMIC BRADS G-300236
16.875"

DATE LINES FROM 1
SINCE COPPER WIRE
SOLDERED TO SHOWN

COMPONENTS WITHIN THIS AREA DEFINED
BY DOTTED LINE, SHOULD BE IN HIGHER THAN
7mm

PIPING HOLE FOR MOUNTING
RESISTORS AND TRANSISTORS
-SEE SHEET 2

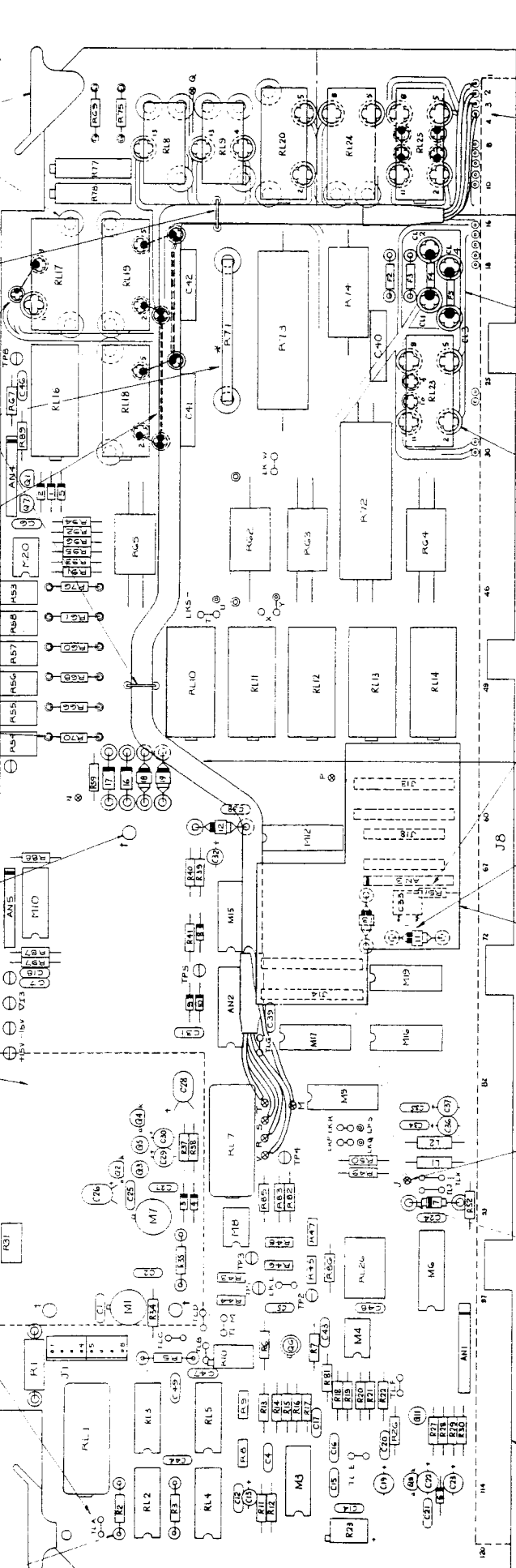
MOUNT R20 R21 R22 R24 R25 R26
R27 R28 R29 R30 R31 R32 R33
R34 R35 R36 R37 R38 R39 R40
R41 R42 R43 R44 R45 R46 R47
R48 R49 R50 R51 R52 R53 R54
R55 R56 R57 R58 R59 R60 R61
R62 R63 R64 R65 R66 R67 R68
R69 R70 R71 R72 R73 R74 R75
R76 R77 R78 R79 R80 R81 R82
R83 R84 R85 R86 R87 R88 R89
R90 R91 R92 R93 R94 R95 R96
R97 R98 R99 R100

1/4" DIA. BOLT TYPE
510006

16.875" SMALL LOCKWELF
TERMINAL G-20000

SECURE CABLE TO PCB
WITH LACING COND 550007

2.0" CIRC. BOARD JACKER
650132 (6UM)



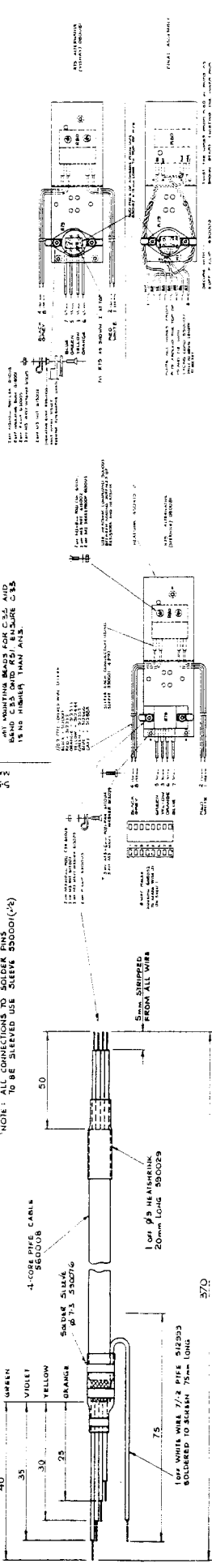
NOTE: ALL CONNECTIONS TO SOLDER PINS
TO BE SLEEVED USE SLEEVE 550001(2)

20.0" LARGE LOCKWELF
TERMINAL G-20000

1/8" CLAMP ASSY
400665

MOUNT R1, R1, R2
IN LARGE CERAMIC BRAD 650074
16.875"

41.0x17.1



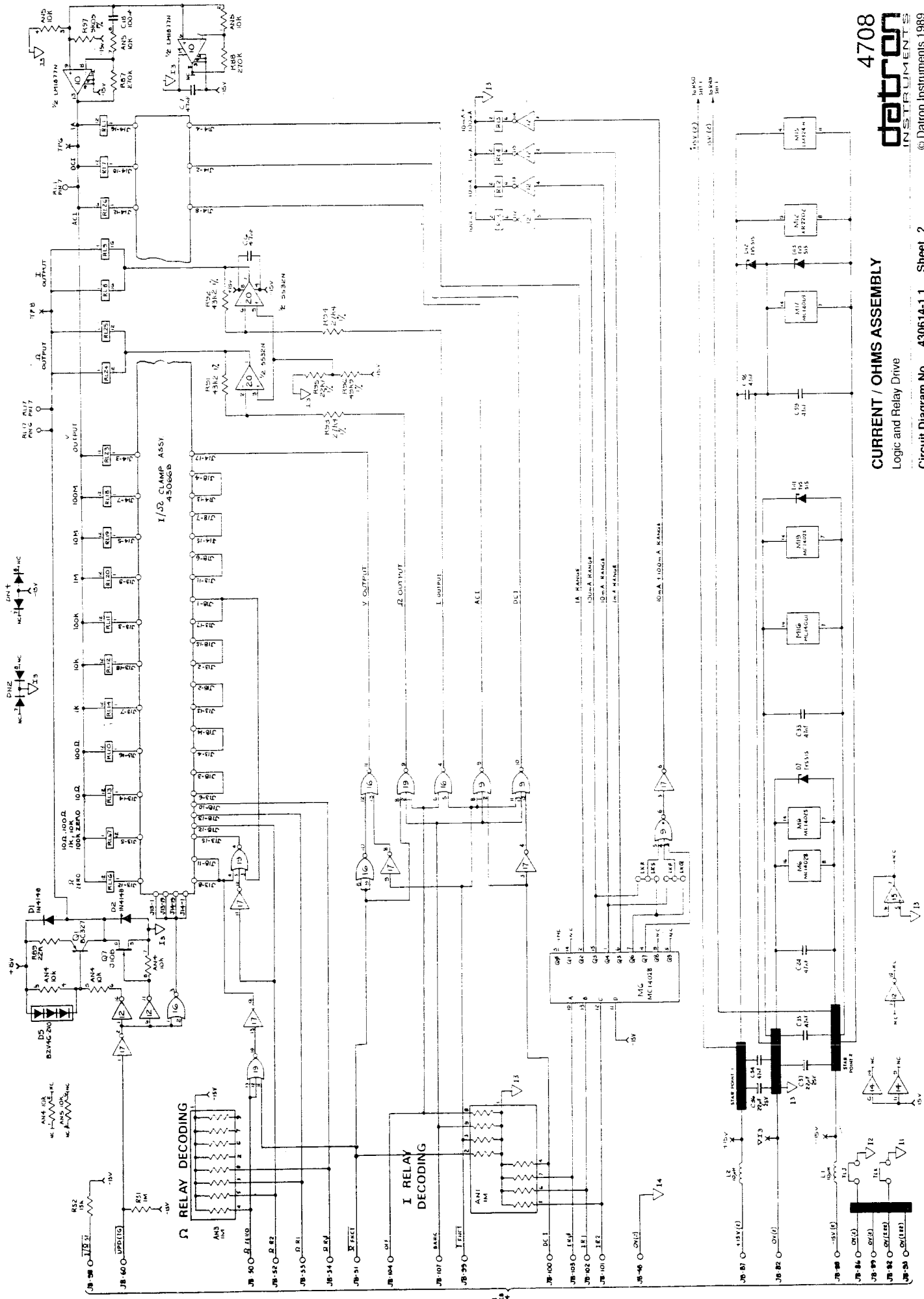
NOTE: PIN 1 ORANGE TO PIN T
PIN 2 VIOLET TO PIN T
PIN 3 GREEN TO PIN Y
PIN 4 YELLOW TO PIN 5

BASE WIRES INTO PADS BETWEEN
PINS 2, 3, 4, 5. SEE SHEET 2 FOR
POSSIBLE. POINT TO POINT WIRING SCHEDULE.

1.0" 9.5 HEATSHRINK
20mm LONG 550029

5mm STRIPPERS
FROM ALL WIRES

16.875" WIRE 17.2 PINS 610053
SOLDERED TO SHOWN 75mm LONG



CURRENT / OHMS ASSEMBLY
 Logic and Relay Drive
 Circuit Diagram No. 430614-1.1 Sheet 2

CURRENT / OHMS ASSEMBLY

| MOUNTING IC's | |
|---------------|--------|
| MP OR WMS | PART # |
| 14 | 605060 |
| 16 | 605061 |
| B | 605059 |
| 20 | 605070 |

ADAPT RE-55 RO, R55, F21.3 F
 ON SMALL CERAMIC BLANDS 6300356
 16 BIT

MAKE 1 PINS MOUNT
 ON SMALL CERAMIC BLAND
 3400302

COMPONENTS WITHIN THIS AREA OFFERED
 BY DOTTED LINE, SHOULD BE NO HIGHER THAN
 7mm

TP2G

TP2Z

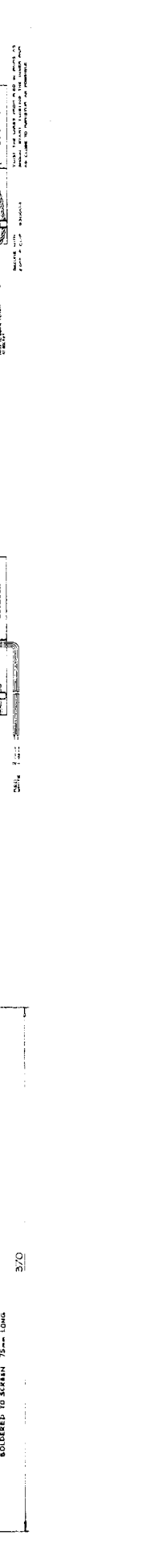
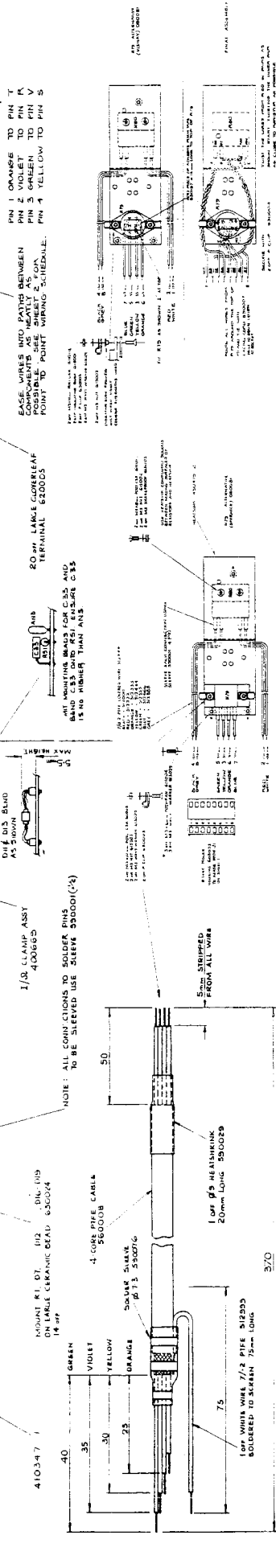
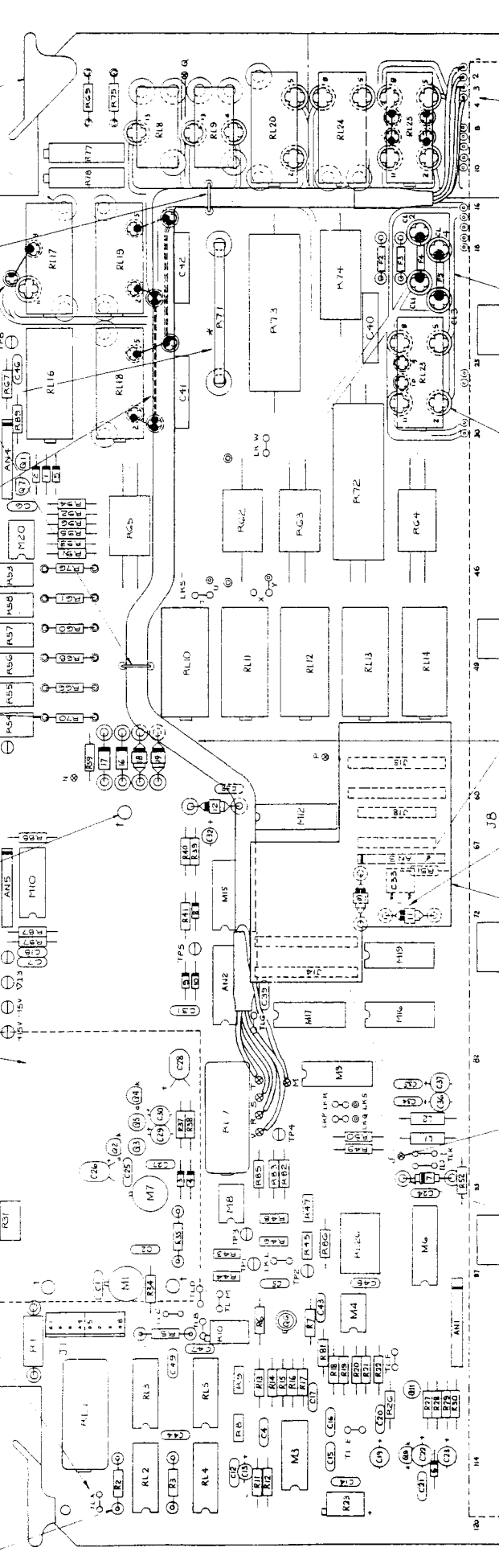
1/10-4 BLACK PTFE
 INSULATED WIRE
 3400000

16 OF SMALL CLOVERLEAF
 TERMINAL 6200031

SECURE CABLES TO PCB
 WITH LAKING COND 5300007

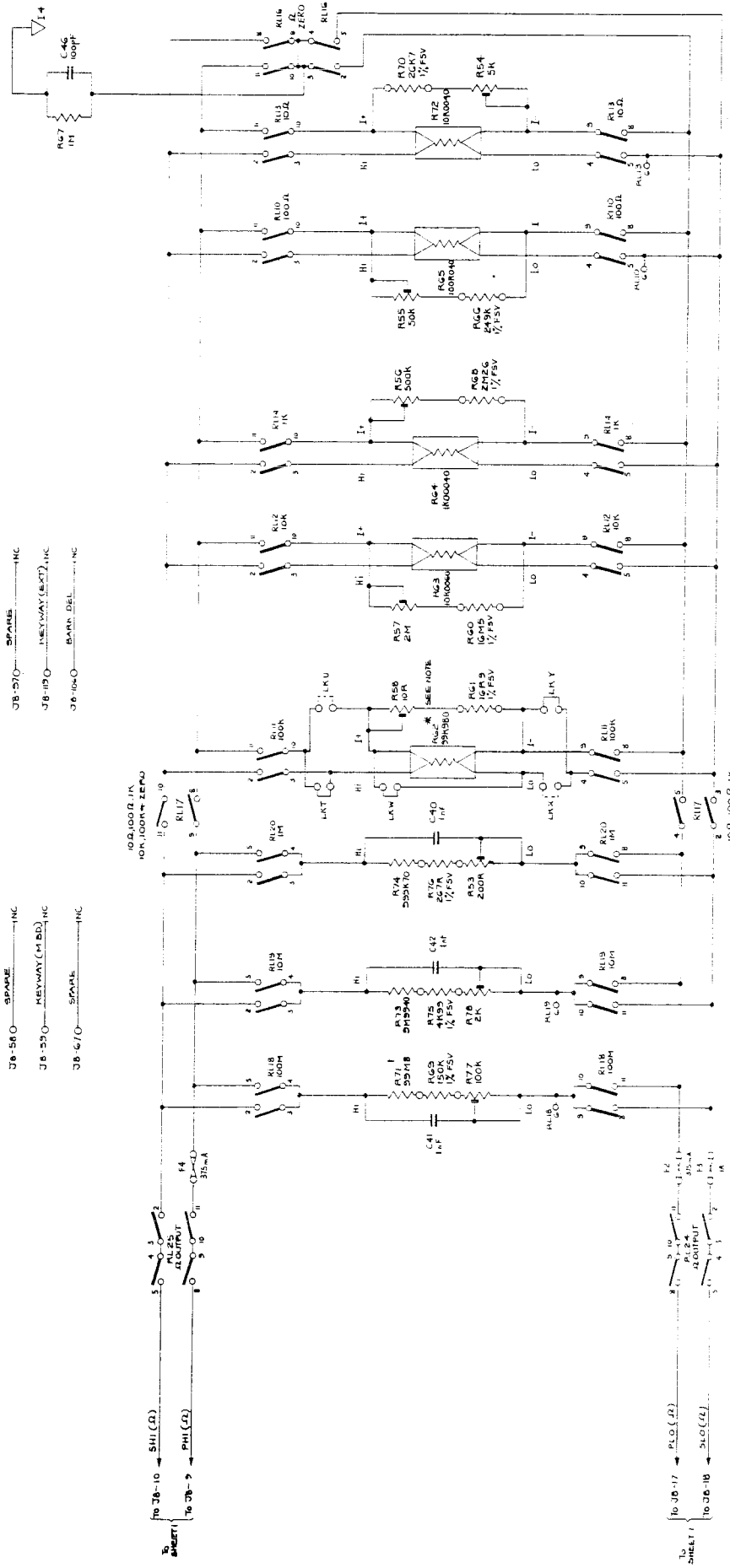
SET 2 WASHERS UNDER RELAYS IN
 ORDER TO PREVENT SHORTS FROM
 USING FLAT-NAILION WASHERS 5300007

2.5mm CEMENT BOARD 6300356



410347
 40
 35
 30
 25
 20
 15
 10
 5
 1.01 0.5 HEADSHANK
 20mm LONG 5800295
 SOLDERED TO STRIP 75mm LONG
 3/20

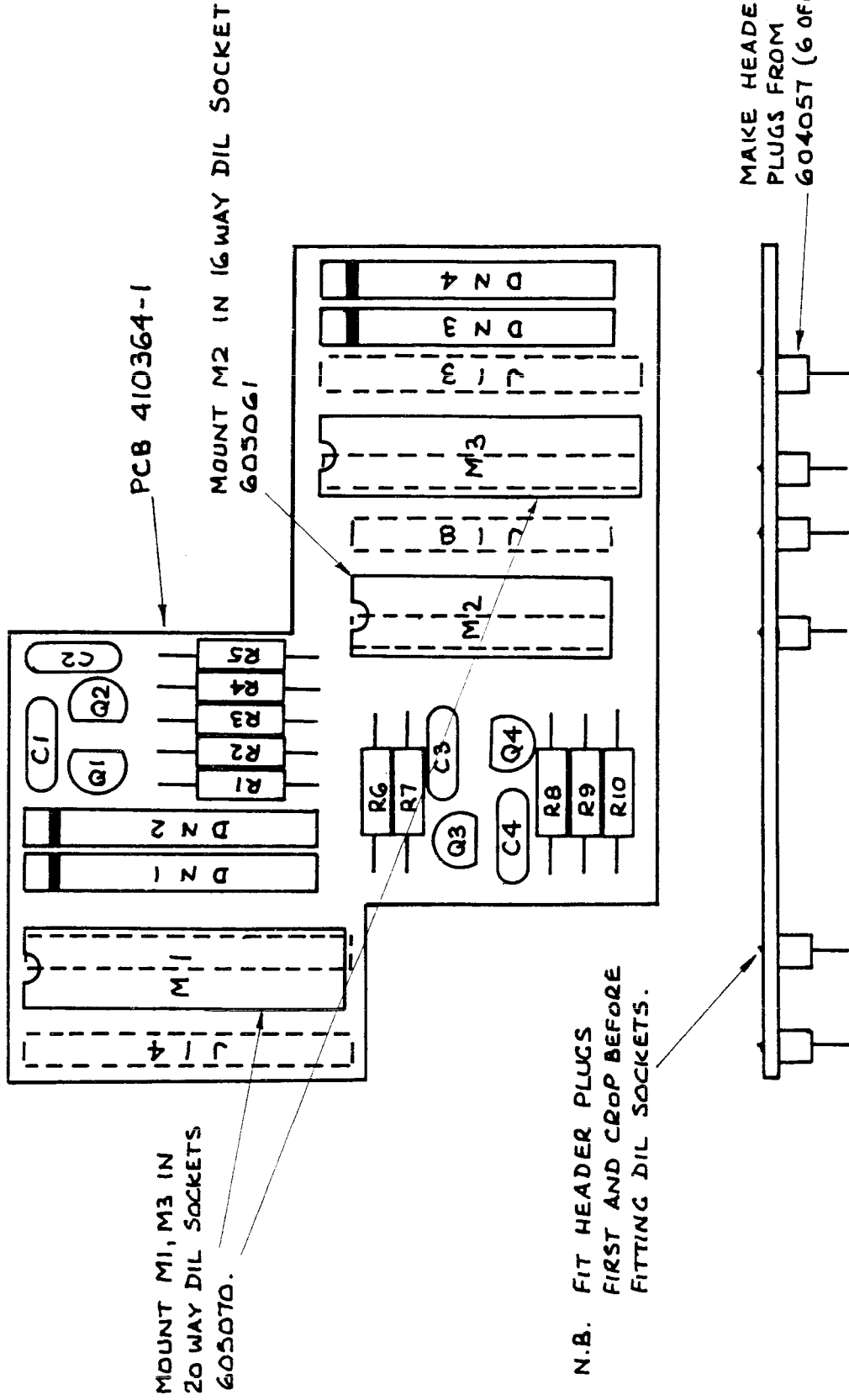
- J8-46 O SPARE INC
- J8-47 O SPARE INC
- J8-48 O SPARE INC
- J8-55 O REM SENSE INC
- J8-56 O POSITIVE INC
- J8-57 O SPARE INC
- J8-58 O SPARE INC
- J8-59 O KEYWAY (H.B.D) INC
- J8-67 O SPARE INC
- J8-68 O SPARE INC
- J8-63 O SPARE INC
- J8-64 O SPARE INC
- J8-65 O SPARE INC
- J8-90 O SPARE INC
- J8-91 O SPARE INC
- J8-97 O SPARE INC
- J8-100 O KEYWAY (EXT) INC
- J8-104 O BARR DEL INC



* NOTE R42 IS A 2-WIRE RESISTOR ON THE 4700.
 † ALTERNATIVE RESISTOR SET COMPRISES TWO 450'S IN SERIES.

CURRENT / OHMS ASSEMBLY
 Standard Resistors and Switching

NOTE. DN1 + DN3 ARE CODED RED
DN2 + DN4 ARE CODED BLUE

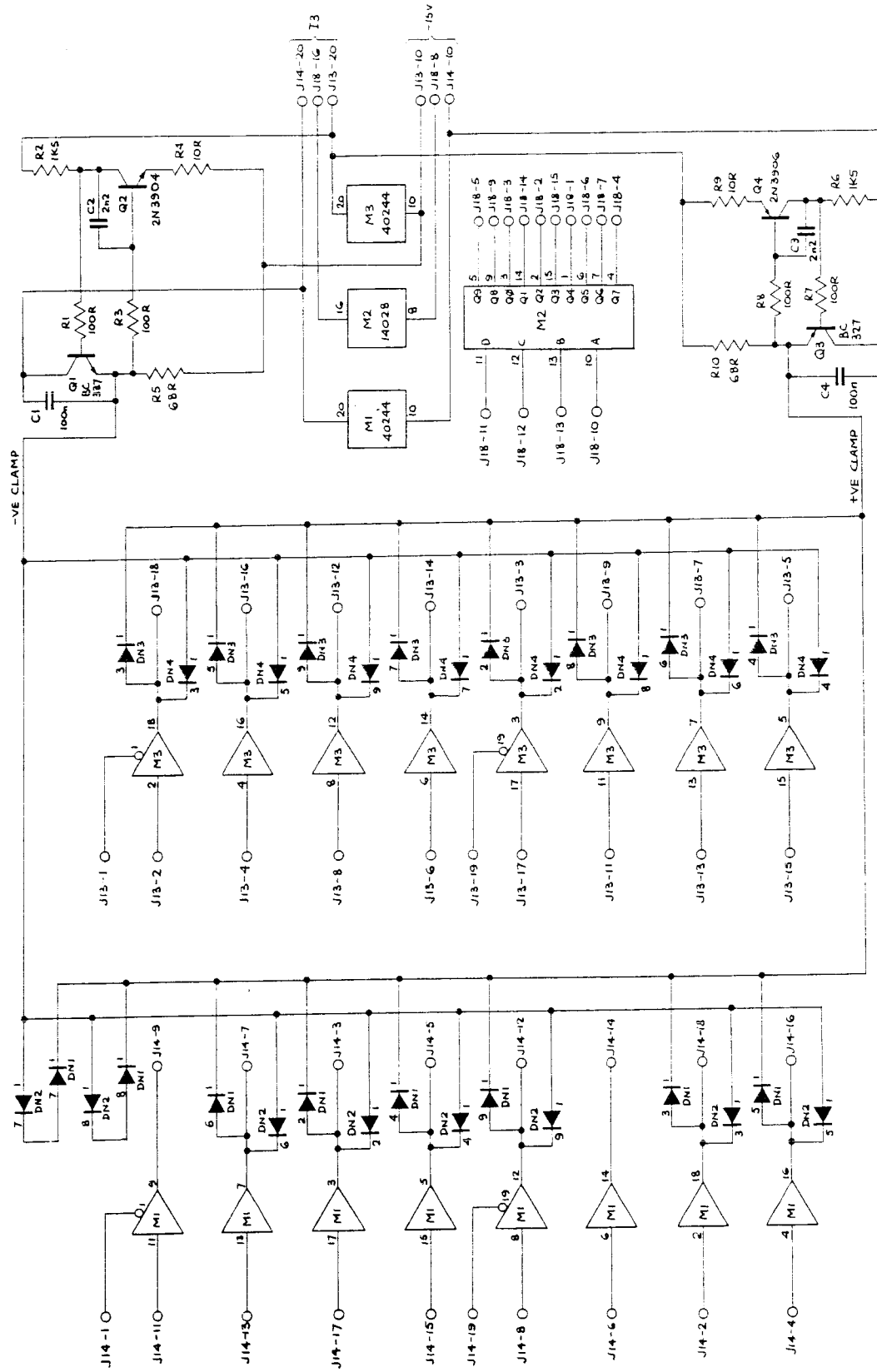


MOUNT M1, M3 IN
20 WAY DIL SOCKETS
605070.

N.B. FIT HEADER PLUGS
FIRST AND CROP BEFORE
FITTING DIL SOCKETS.

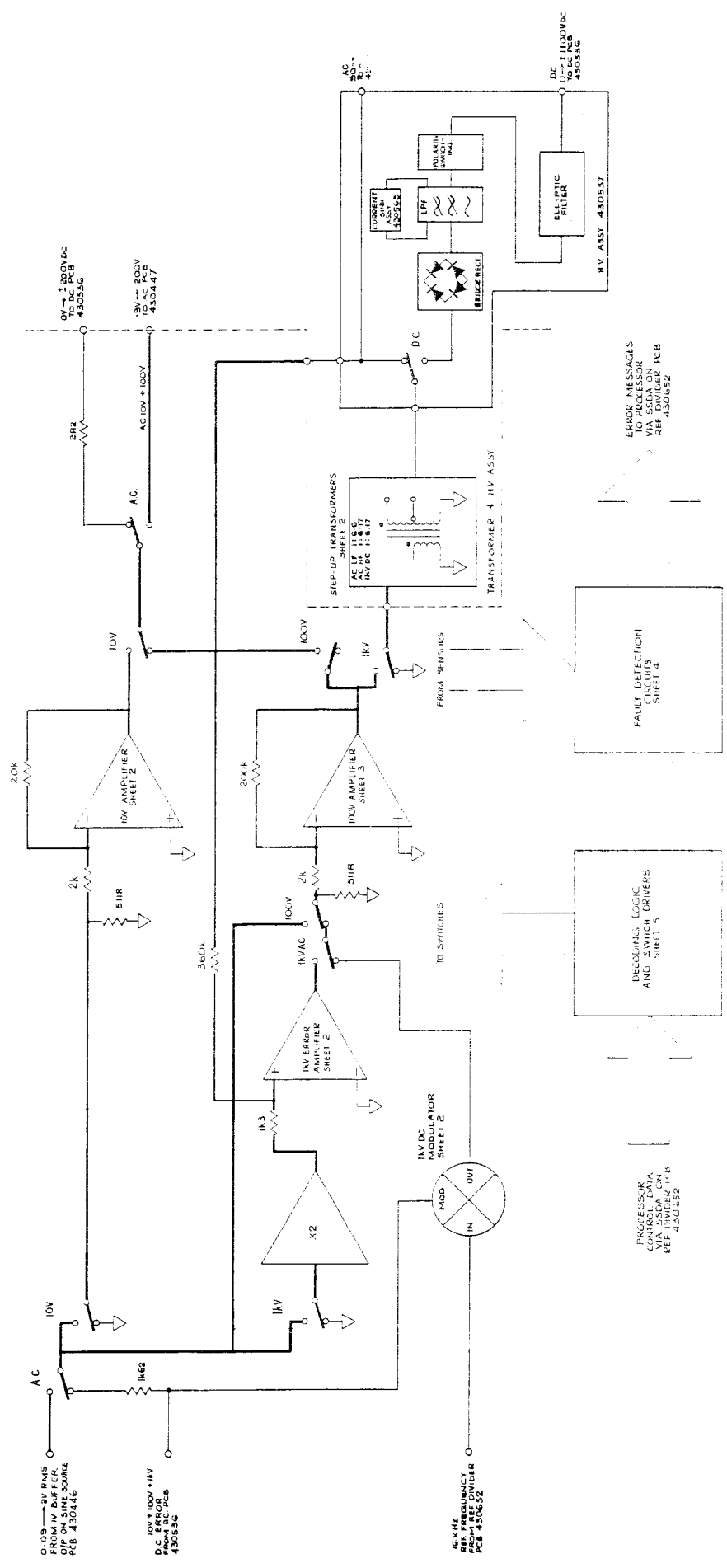
MAKE HEADER
PLUGS FROM
604057 (6 OFF)

DN1 AND DN3 ARE CC-IN414B
 DN2 AND DN4 ARE CA-IN414B



I/O CLAMP ASSEMBLY

Circuit Diagram No. 430669-1.0 Sheet 1



POWER AMPLIFIER ASSEMBLY
 Block Diagram
 Circuit Diagram No. 430618-5.0 Sheet 1

ERROR MESSAGES
 TO PROCESSOR
 VIA SSCA ON
 REF BOARD PCB
 430552

FAULT DETECTION
 CIRCUITS
 SHEET 4

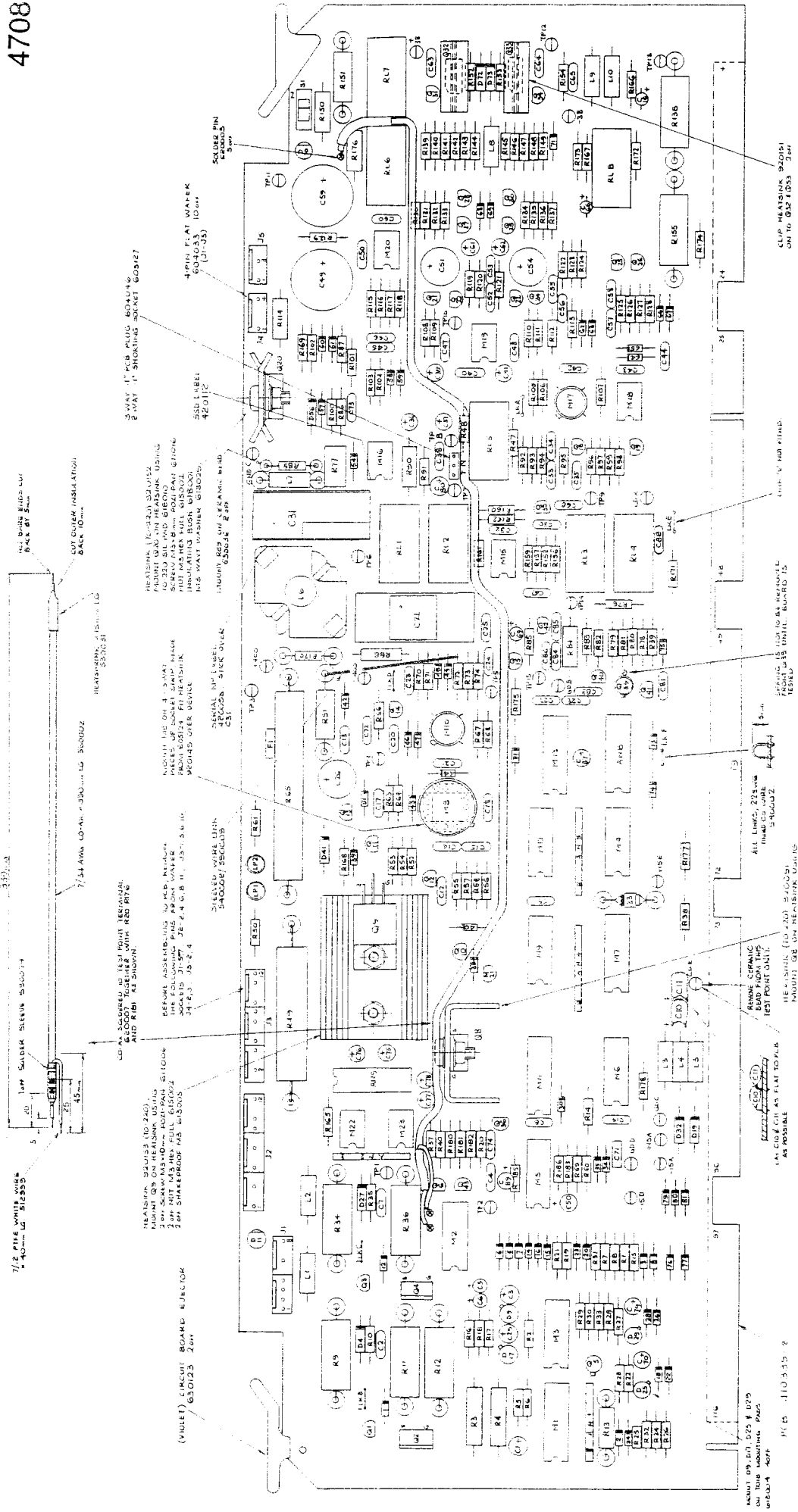
DECODING LOGIC
 AND SWITCH DRIVERS
 SHEET 5

PROCESSOR
 CONTROL DATA
 SHEET ON
 REF BOARD PCB
 430552

0.05 → 2V RMS
 FROM IV BUFFER
 ON BOARD PCB
 430446

10V + 100V + 1kV
 FROM 100V PCB
 430536

CLK HE
 REF FREQUENCY
 FROM DIVIDER
 PCB 430532



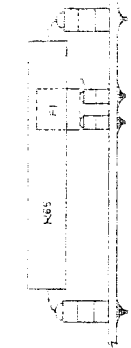
PLACING BEADS 630024 (50 WTS)

| BEAD | LOCATIONS |
|------|------------------------------------|
| 1 | R15, R51, R51A, R73A, C51, L7 |
| 2 | R5, R10, R34, R34A, R36, R36A, R55 |
| 3 | R19, R45 |

10. THE FOLLOWING MECHANICALS TO MAKE THE BEAD BOARD 630024 ON EACH LEG (TOTAL 60 BEADS)
 C 2, C5, C15, C19, C21, C21A, C26, C32, C32A, C43, C43A, C40 & C45

REWORK CERAMIC BOARD FOR THE HEATSHINK (TO 240) 500024

REWORK CERAMIC BOARD FOR THE HEATSHINK (TO 240) 500024



INSULATING J.C.

| PART NO. | QTY. | WHERE USED |
|----------|--------|------------|
| 8 | 500059 | 7 |
| 14 | 500060 | 7 |
| 16 | 600060 | 4 |

REWORK CERAMIC BOARD FOR THE HEATSHINK (TO 240) 500024

REWORK CERAMIC BOARD FOR THE HEATSHINK (TO 240) 500024

REWORK CERAMIC BOARD FOR THE HEATSHINK (TO 240) 500024

REWORK CERAMIC BOARD FOR THE HEATSHINK (TO 240) 500024

REWORK CERAMIC BOARD FOR THE HEATSHINK (TO 240) 500024

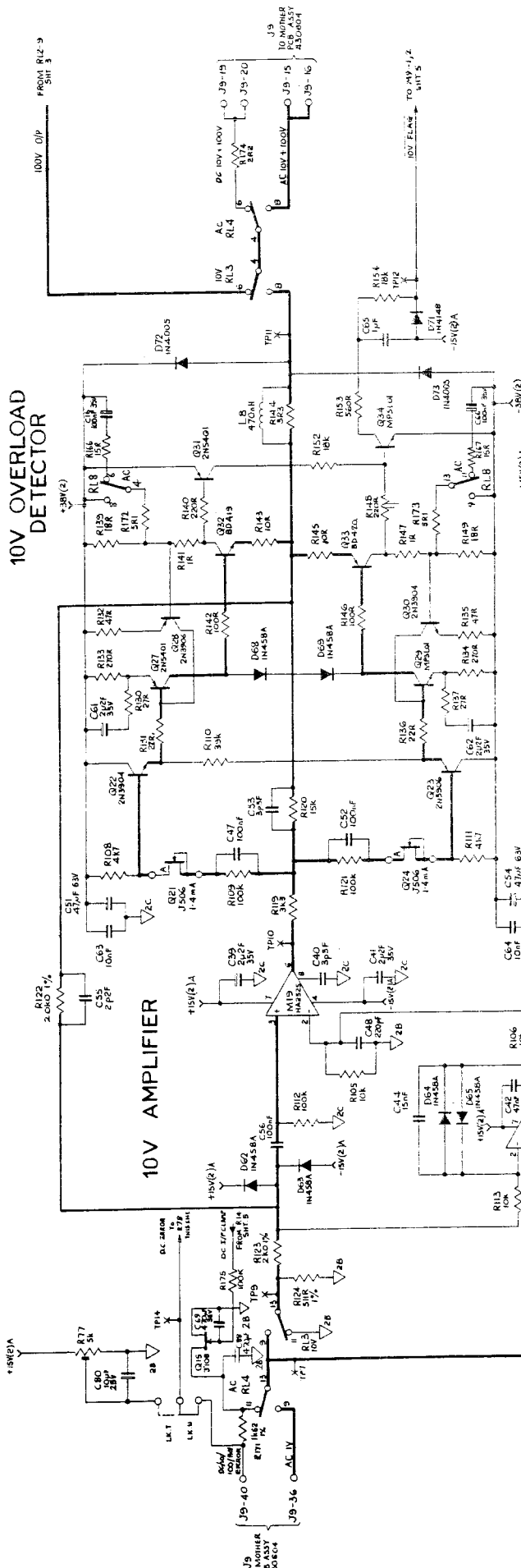
REWORK CERAMIC BOARD FOR THE HEATSHINK (TO 240) 500024

REWORK CERAMIC BOARD FOR THE HEATSHINK (TO 240) 500024

REWORK CERAMIC BOARD FOR THE HEATSHINK (TO 240) 500024

REWORK CERAMIC BOARD FOR THE HEATSHINK (TO 240) 500024

10V OVERLOAD DETECTOR



10V AMPLIFIER

SATURATION DETECTOR

1KV ERROR AMP

1KVDC MODULATOR

POWER AMPLIFIER ASSEMBLY

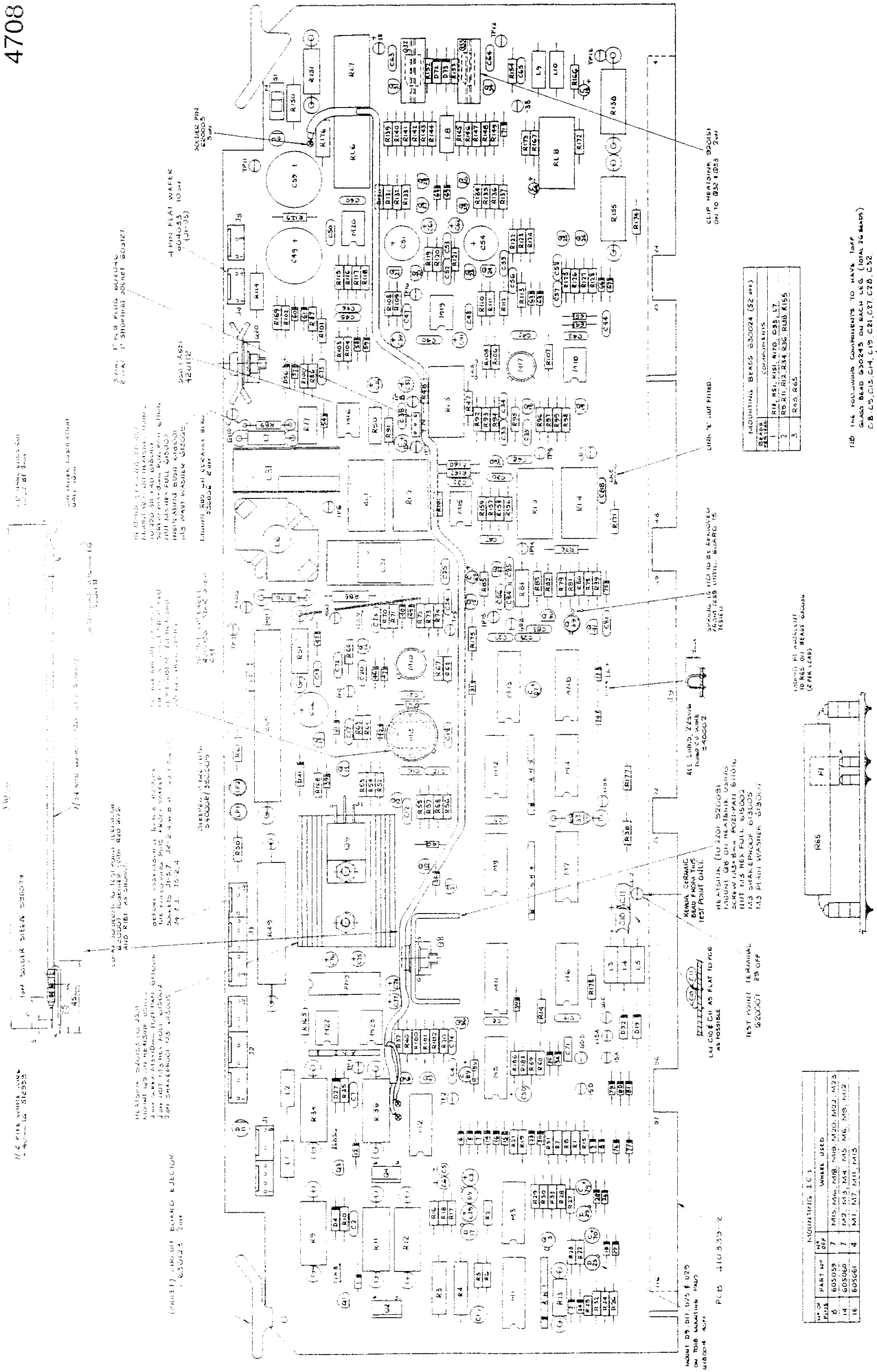
10V and 1KV Amplifiers

Circuit Diagram No. 430618-5.0 Sheet 2



© Datron Instruments 1989

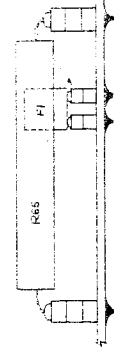
11.9-2



MOUNTING BEADS 630024 (32 OH)

| BEAD # | VALUES |
|--------|------------------------------|
| 1 | R1, R2, R11, R17, C23, L7 |
| 2 | R5, R11, R12, R24, R35, R105 |
| 3 | R20, R25 |

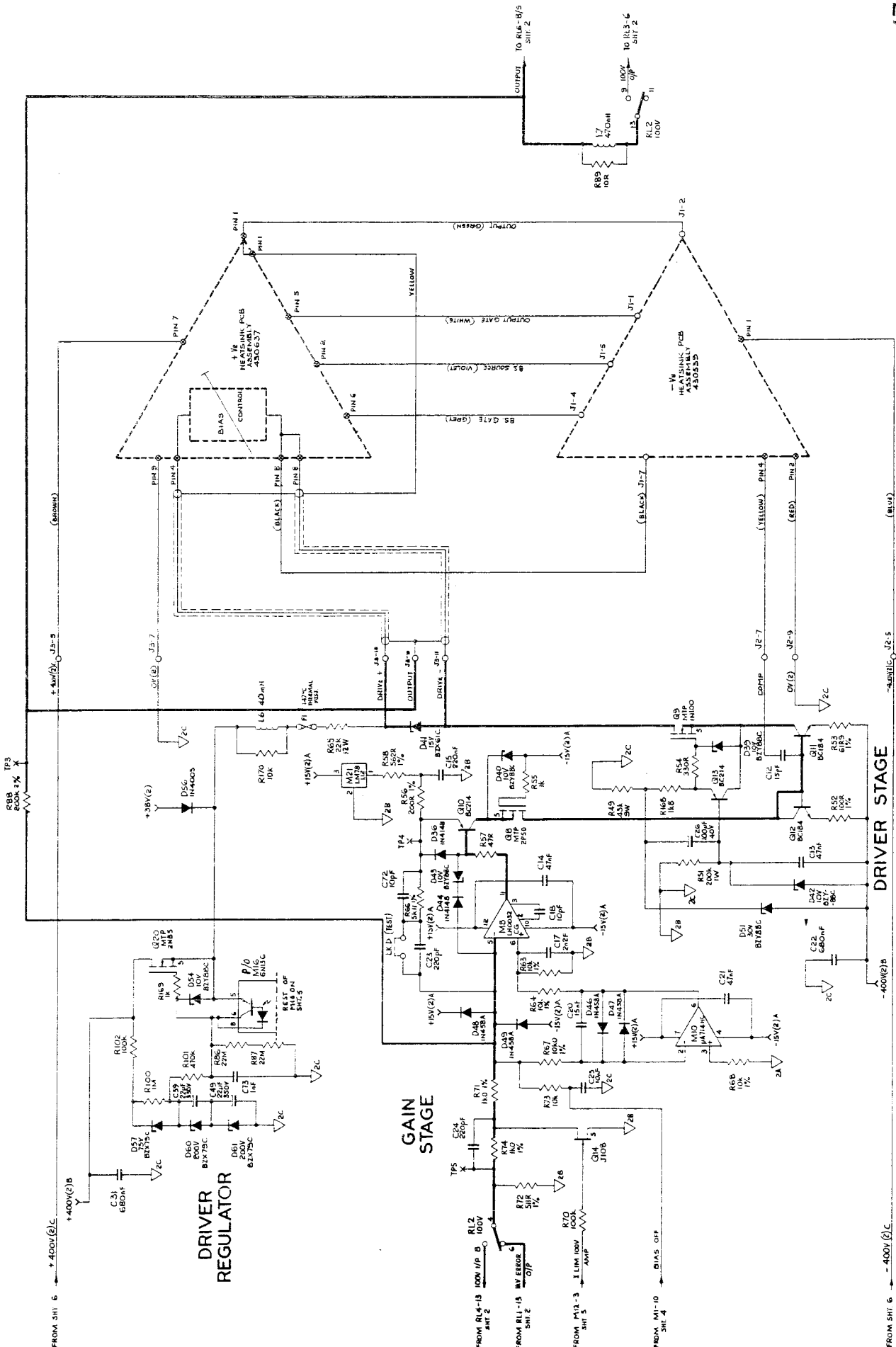
THE FOLLOWING COMMENTS TO HAVE LEFT
 BEAD 630024 ON EACH LEG (DON'T FORGET)
 C2, C3, C12, C14, C15, C16, C17, C20, C22,
 C24, C25, C40, C41, C42, C43, C44, C45



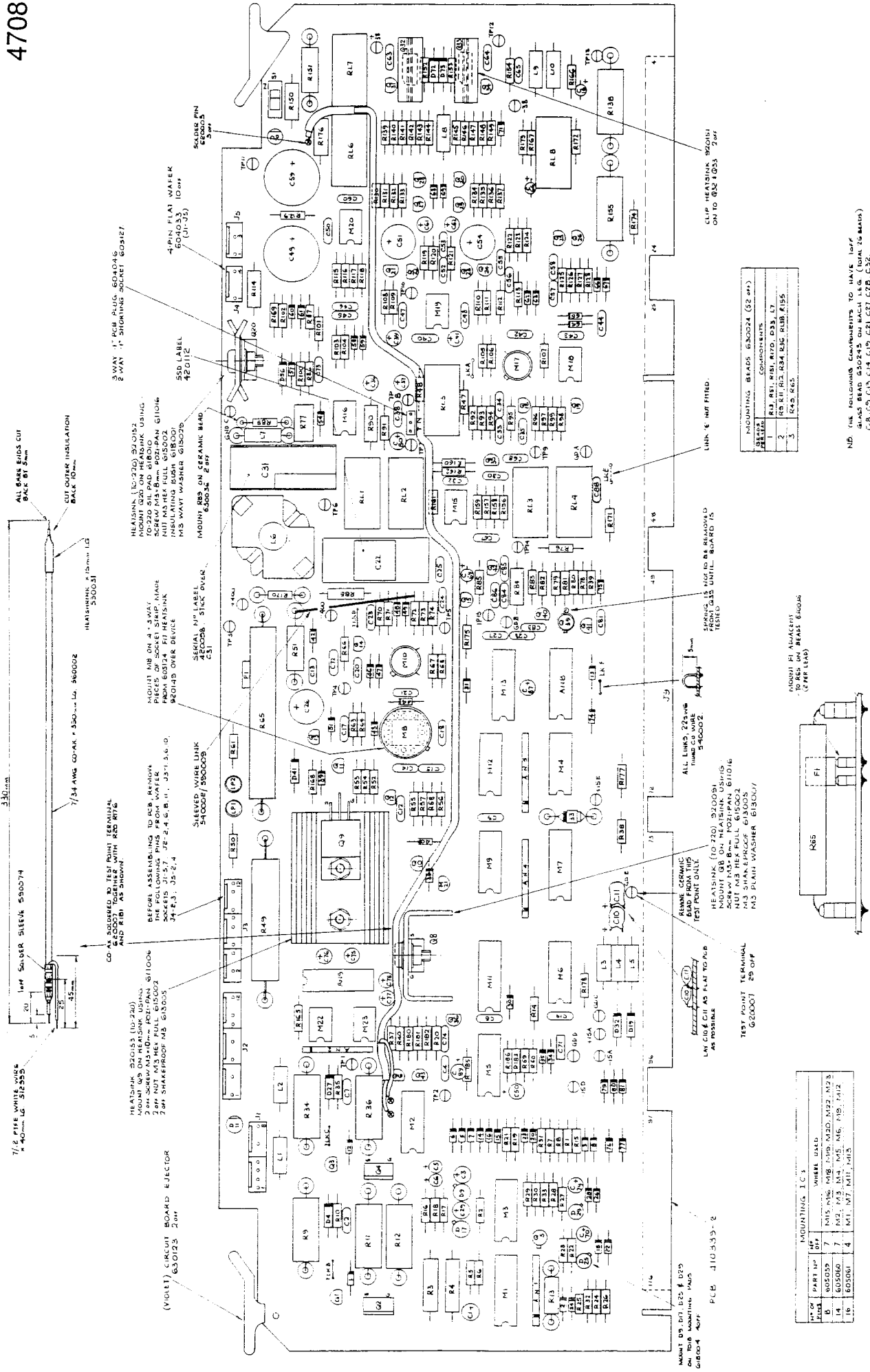
INQUIRIES 1 C 3

| W/ OF | PART NO | WHERE USED |
|-------|---------|-----------------------------------|
| 01 | 605039 | M15, M16, M18, M19, M20, M22, M23 |
| 02 | 605040 | M4, M5, M6, M7, M8, M9, M10 |
| 03 | 605061 | M1, M7, M11, M13 |

PCB 4103-33-2
 MOUNT DR DR DVS F 0029
 ON THE MOUNTING PAD
 GROUND NET



POWER AMPLIFIER ASSEMBLY
100V Amplifier



INDICATING BEADS: 630024 (52 Pcs)

| BEAD # | COMPONENTS |
|--------|------------------------------|
| 1 | R15, R17, M15, M16, D33, L7 |
| 2 | R5, R12, R34, R36, R10, R155 |
| 3 | C42, R65 |

NOTE: THE FOLLOWING COMPONENTS TO HAVE 100% BEAD READ 630024 ON EACH LEG (TOTAL 24 BEADS):
 C: C42, C43, C44, C24, C21, C20, C36, C42, C43, C44, C24, C21, C20, C36.

FRONT GAS LEAK BEAD READS TO BE TAKEN AT FRONT GAS LEAK UNTIL BEAD READ IS TESTED

FRONT FI MANIFEST TO R65 ON BEAD 630024 (OFF LEG)

TEST POINT TERMINAL 620001 29 OFF

INDICATING BEAD READS TO BE TAKEN AT FRONT GAS LEAK UNTIL BEAD READ IS TESTED

| MT OF PART # | WHEN USED |
|--------------|-----------------------------------|
| 0 | M15, M16, M15, M16, M20, M22, M23 |
| 1 | M2, M3, M4, M5, M6, M7, M12, M13 |
| 2 | M1, M7, M11, M13 |

PCB 1105333-2

3 WAY 1" PCB PLUG 604046
 2 WAY 1" SHORING SOCKET 603127

HEAT SINKS (10-220) 350183
 MOUNT ON HEAT SINK USING
 TO-220 SIL PAD 618100
 SCREW M3x8mm POSI-PAN 611016
 INSULATING WASHERS 618100
 M3 WASH WASHER 618029

HEAT SINK (10-220) 350183
 MOUNT ON HEAT SINK USING
 TO-220 SIL PAD 618100
 SCREW M3x8mm POSI-PAN 611016
 INSULATING WASHERS 618100
 M3 WASH WASHER 618029

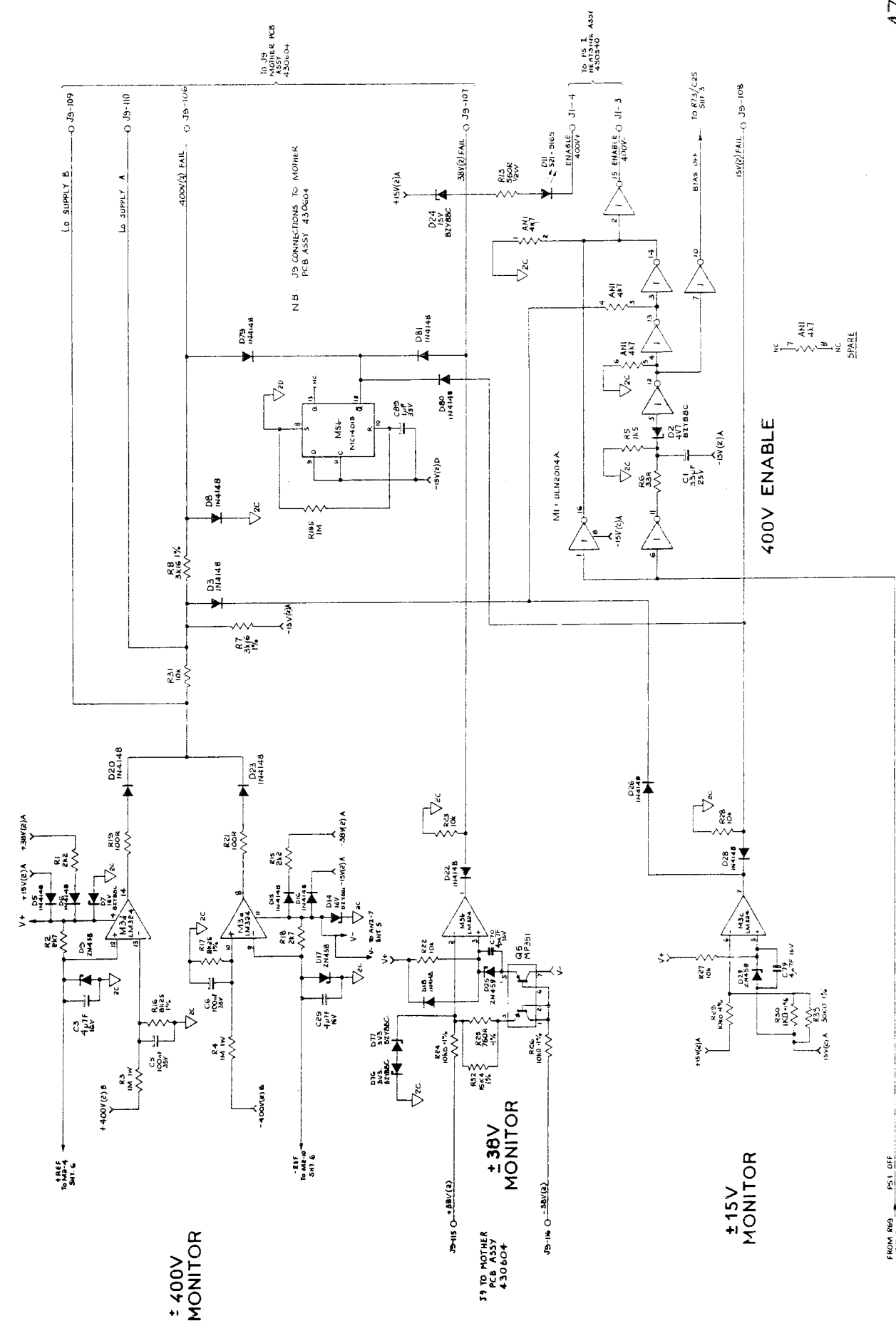
HEAT SINK (10-220) 350183
 MOUNT ON HEAT SINK USING
 TO-220 SIL PAD 618100
 SCREW M3x8mm POSI-PAN 611016
 INSULATING WASHERS 618100
 M3 WASH WASHER 618029

HEAT SINK (10-220) 350183
 MOUNT ON HEAT SINK USING
 TO-220 SIL PAD 618100
 SCREW M3x8mm POSI-PAN 611016
 INSULATING WASHERS 618100
 M3 WASH WASHER 618029

HEAT SINK (10-220) 350183
 MOUNT ON HEAT SINK USING
 TO-220 SIL PAD 618100
 SCREW M3x8mm POSI-PAN 611016
 INSULATING WASHERS 618100
 M3 WASH WASHER 618029

HEAT SINK (10-220) 350183
 MOUNT ON HEAT SINK USING
 TO-220 SIL PAD 618100
 SCREW M3x8mm POSI-PAN 611016
 INSULATING WASHERS 618100
 M3 WASH WASHER 618029

HEAT SINK (10-220) 350183
 MOUNT ON HEAT SINK USING
 TO-220 SIL PAD 618100
 SCREW M3x8mm POSI-PAN 611016
 INSULATING WASHERS 618100
 M3 WASH WASHER 618029



± 400V MONITOR

± 36V MONITOR

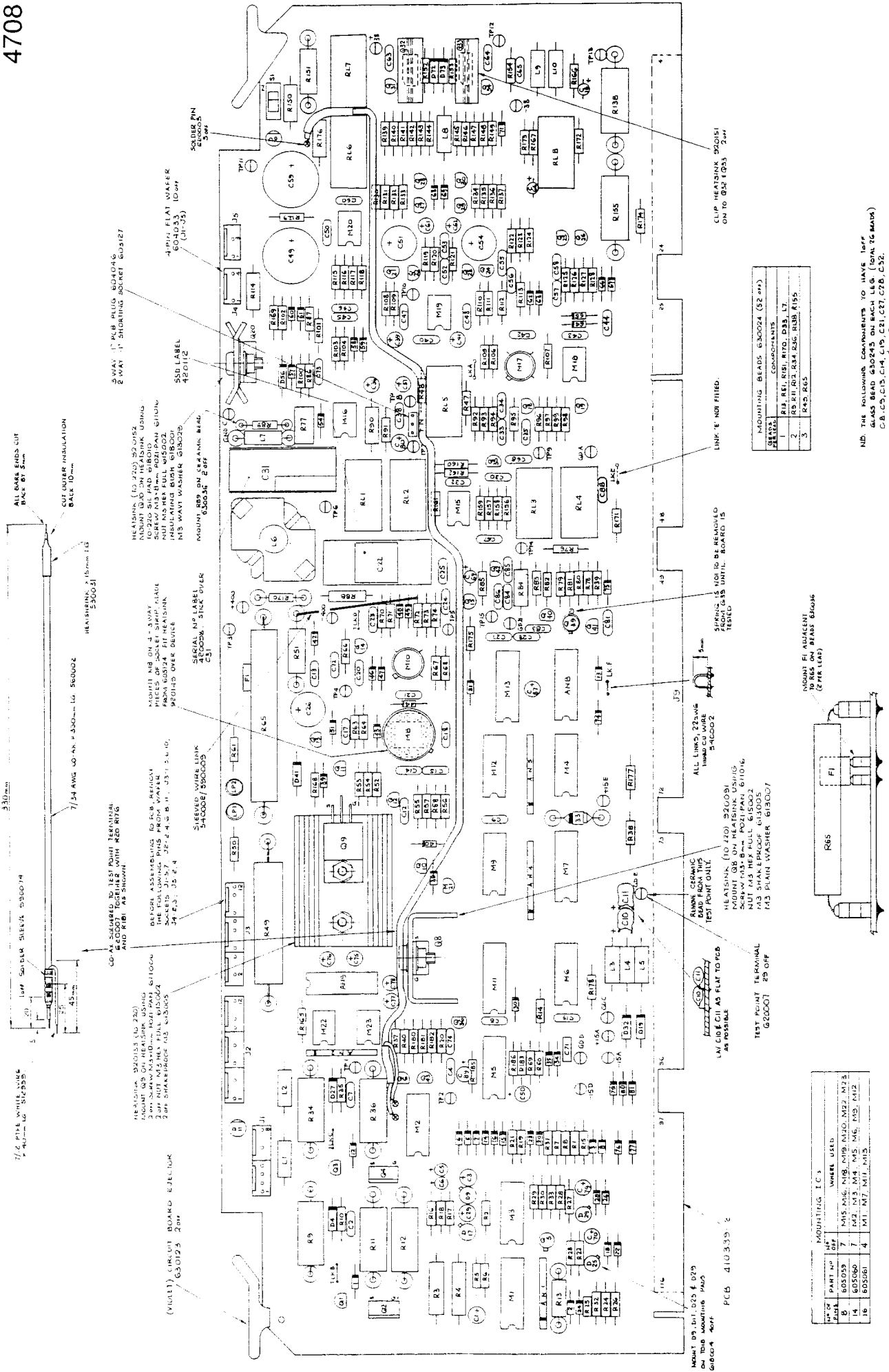
± 15V MONITOR

FIG. 206
SMT 5
PS 1 OFF

POWER AMPLIFIER ASSEMBLY
Power Supply Monitors

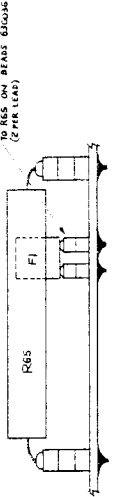
Circuit Diagram No. 430618-5.0 Sheet 4

POWER AMPLIFIER ASSEMBLY



| BEAD | COMPONENTS |
|------|-----------------------------------|
| 1 | R19, R21, R21, R170, D33, L7 |
| 2 | R2, R11, R12, R34, R36, R38, R155 |
| 3 | R43, R45 |

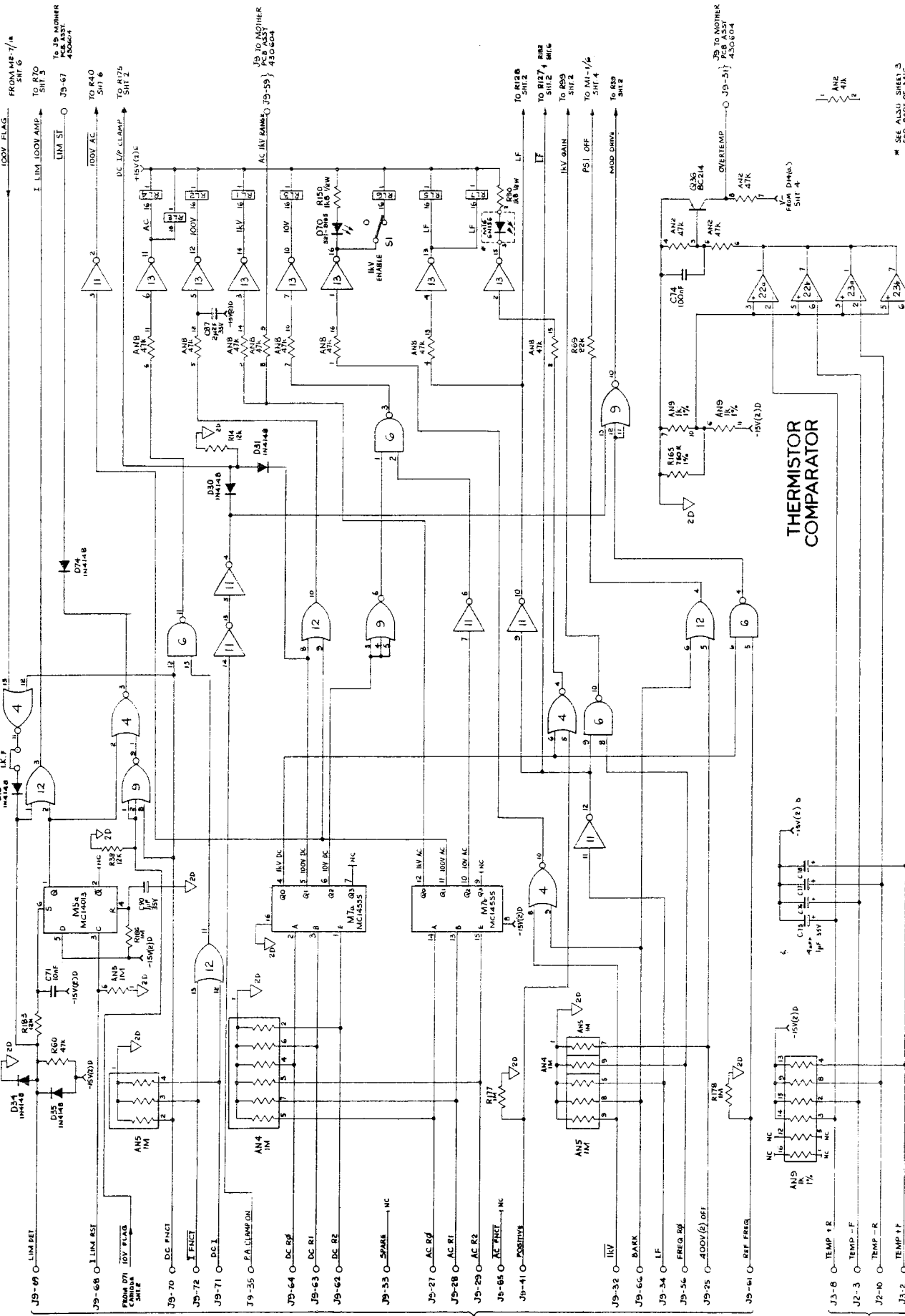
NOTE: THE FOLLOWING COMPONENTS TO HAVE LEAF GLASS BEAD 630024 ON EACH LEG (TOTAL 26 MAX):
 C-42, C-43, C-44, C-19, C-21, C-27, C-28, C-32, C-42, C-43, C-40 & C-45.



| QTY | PART NO | REF | WHERE USED |
|-----|---------|-----|-----------------------------------|
| 1 | 605035 | 7 | M15, M16, M18, M19, M20, M22, M23 |
| 1 | 605080 | 7 | M2, M3, M4, M5, M6, M8, M12 |
| 1 | 605061 | 4 | M1, M7, M11, M13 |

MOUNT D5, D1, D25 & D29 ON THIS MOUNTING PLATE GROUP 4 REF

PCB 410333-2



POWER AMPLIFIER ASSEMBLY
 Logic and Relay Drives

* SEE ALSO SHEET 3 FOR PART OF I/O

J2 TO NEG HEAT SINK ANS2 430618-5.0 SH1 3
 J3 TO POS HEAT SINK ANS3 430618-5.0 SH1 3
 J4 TO POS HEAT SINK ANS4 430618-5.0 SH1 3
 J5 TO POS HEAT SINK ANS5 430618-5.0 SH1 3

J6 TO NEG HEAT SINK ANS6 430618-5.0 SH1 3
 J7 TO POS HEAT SINK ANS7 430618-5.0 SH1 3
 J8 TO POS HEAT SINK ANS8 430618-5.0 SH1 3
 J9 TO POS HEAT SINK ANS9 430618-5.0 SH1 3

J10 TO NEG HEAT SINK ANS10 430618-5.0 SH1 3
 J11 TO POS HEAT SINK ANS11 430618-5.0 SH1 3
 J12 TO POS HEAT SINK ANS12 430618-5.0 SH1 3
 J13 TO POS HEAT SINK ANS13 430618-5.0 SH1 3

J14 TO NEG HEAT SINK ANS14 430618-5.0 SH1 3
 J15 TO POS HEAT SINK ANS15 430618-5.0 SH1 3
 J16 TO POS HEAT SINK ANS16 430618-5.0 SH1 3
 J17 TO POS HEAT SINK ANS17 430618-5.0 SH1 3

J18 TO NEG HEAT SINK ANS18 430618-5.0 SH1 3
 J19 TO POS HEAT SINK ANS19 430618-5.0 SH1 3
 J20 TO POS HEAT SINK ANS20 430618-5.0 SH1 3
 J21 TO POS HEAT SINK ANS21 430618-5.0 SH1 3

J22 TO NEG HEAT SINK ANS22 430618-5.0 SH1 3
 J23 TO POS HEAT SINK ANS23 430618-5.0 SH1 3
 J24 TO POS HEAT SINK ANS24 430618-5.0 SH1 3
 J25 TO POS HEAT SINK ANS25 430618-5.0 SH1 3

J26 TO NEG HEAT SINK ANS26 430618-5.0 SH1 3
 J27 TO POS HEAT SINK ANS27 430618-5.0 SH1 3
 J28 TO POS HEAT SINK ANS28 430618-5.0 SH1 3
 J29 TO POS HEAT SINK ANS29 430618-5.0 SH1 3

J30 TO NEG HEAT SINK ANS30 430618-5.0 SH1 3
 J31 TO POS HEAT SINK ANS31 430618-5.0 SH1 3
 J32 TO POS HEAT SINK ANS32 430618-5.0 SH1 3
 J33 TO POS HEAT SINK ANS33 430618-5.0 SH1 3

J34 TO NEG HEAT SINK ANS34 430618-5.0 SH1 3
 J35 TO POS HEAT SINK ANS35 430618-5.0 SH1 3
 J36 TO POS HEAT SINK ANS36 430618-5.0 SH1 3
 J37 TO POS HEAT SINK ANS37 430618-5.0 SH1 3

J38 TO NEG HEAT SINK ANS38 430618-5.0 SH1 3
 J39 TO POS HEAT SINK ANS39 430618-5.0 SH1 3
 J40 TO POS HEAT SINK ANS40 430618-5.0 SH1 3
 J41 TO POS HEAT SINK ANS41 430618-5.0 SH1 3

J42 TO NEG HEAT SINK ANS42 430618-5.0 SH1 3
 J43 TO POS HEAT SINK ANS43 430618-5.0 SH1 3
 J44 TO POS HEAT SINK ANS44 430618-5.0 SH1 3
 J45 TO POS HEAT SINK ANS45 430618-5.0 SH1 3

J46 TO NEG HEAT SINK ANS46 430618-5.0 SH1 3
 J47 TO POS HEAT SINK ANS47 430618-5.0 SH1 3
 J48 TO POS HEAT SINK ANS48 430618-5.0 SH1 3
 J49 TO POS HEAT SINK ANS49 430618-5.0 SH1 3

J50 TO NEG HEAT SINK ANS50 430618-5.0 SH1 3
 J51 TO POS HEAT SINK ANS51 430618-5.0 SH1 3
 J52 TO POS HEAT SINK ANS52 430618-5.0 SH1 3
 J53 TO POS HEAT SINK ANS53 430618-5.0 SH1 3

J54 TO NEG HEAT SINK ANS54 430618-5.0 SH1 3
 J55 TO POS HEAT SINK ANS55 430618-5.0 SH1 3
 J56 TO POS HEAT SINK ANS56 430618-5.0 SH1 3
 J57 TO POS HEAT SINK ANS57 430618-5.0 SH1 3

J58 TO NEG HEAT SINK ANS58 430618-5.0 SH1 3
 J59 TO POS HEAT SINK ANS59 430618-5.0 SH1 3
 J60 TO POS HEAT SINK ANS60 430618-5.0 SH1 3
 J61 TO POS HEAT SINK ANS61 430618-5.0 SH1 3

J62 TO NEG HEAT SINK ANS62 430618-5.0 SH1 3
 J63 TO POS HEAT SINK ANS63 430618-5.0 SH1 3
 J64 TO POS HEAT SINK ANS64 430618-5.0 SH1 3
 J65 TO POS HEAT SINK ANS65 430618-5.0 SH1 3

J66 TO NEG HEAT SINK ANS66 430618-5.0 SH1 3
 J67 TO POS HEAT SINK ANS67 430618-5.0 SH1 3
 J68 TO POS HEAT SINK ANS68 430618-5.0 SH1 3
 J69 TO POS HEAT SINK ANS69 430618-5.0 SH1 3

J70 TO NEG HEAT SINK ANS70 430618-5.0 SH1 3
 J71 TO POS HEAT SINK ANS71 430618-5.0 SH1 3
 J72 TO POS HEAT SINK ANS72 430618-5.0 SH1 3
 J73 TO POS HEAT SINK ANS73 430618-5.0 SH1 3

J74 TO NEG HEAT SINK ANS74 430618-5.0 SH1 3
 J75 TO POS HEAT SINK ANS75 430618-5.0 SH1 3
 J76 TO POS HEAT SINK ANS76 430618-5.0 SH1 3
 J77 TO POS HEAT SINK ANS77 430618-5.0 SH1 3

J78 TO NEG HEAT SINK ANS78 430618-5.0 SH1 3
 J79 TO POS HEAT SINK ANS79 430618-5.0 SH1 3
 J80 TO POS HEAT SINK ANS80 430618-5.0 SH1 3
 J81 TO POS HEAT SINK ANS81 430618-5.0 SH1 3

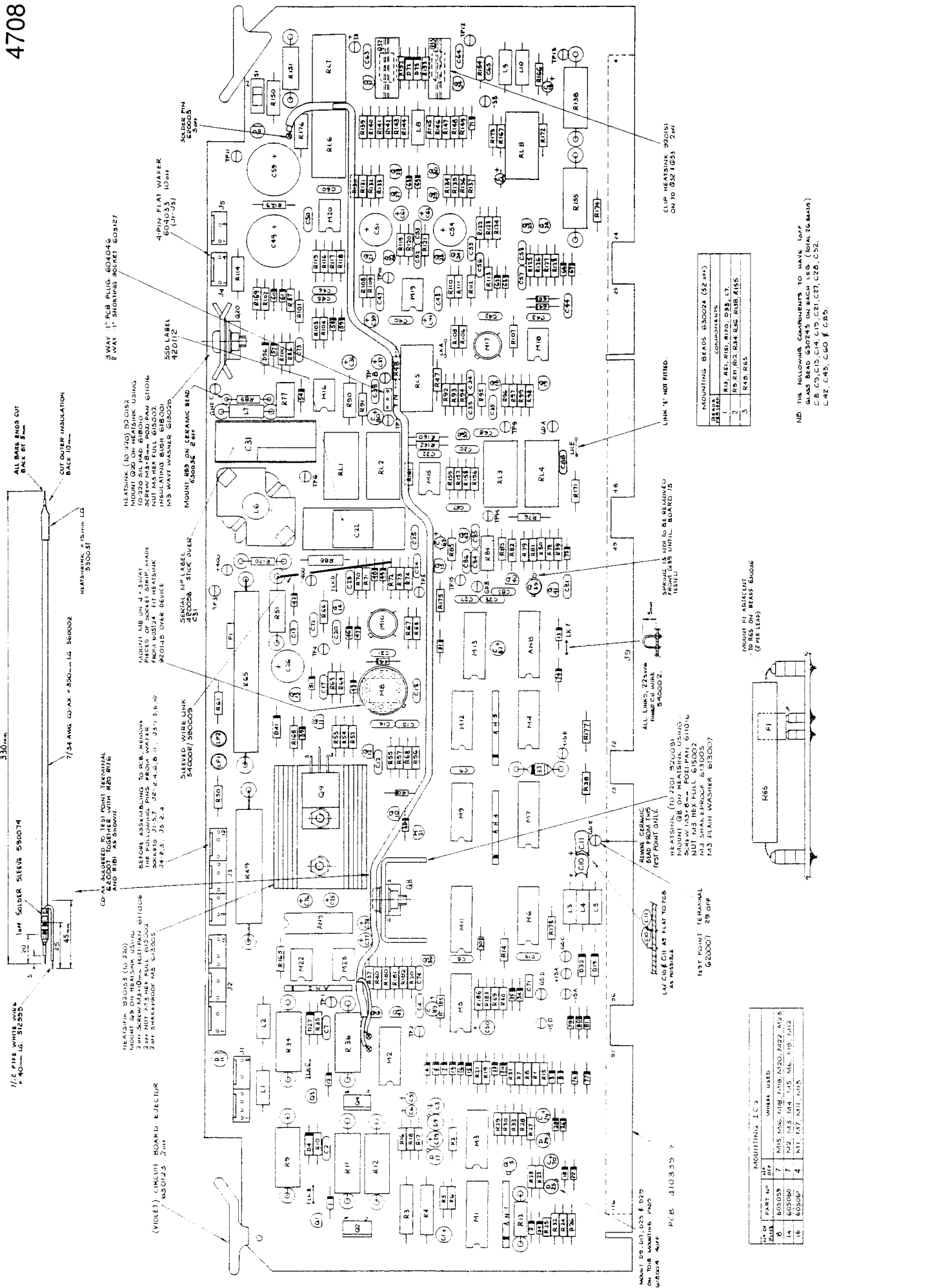
J82 TO NEG HEAT SINK ANS82 430618-5.0 SH1 3
 J83 TO POS HEAT SINK ANS83 430618-5.0 SH1 3
 J84 TO POS HEAT SINK ANS84 430618-5.0 SH1 3
 J85 TO POS HEAT SINK ANS85 430618-5.0 SH1 3

J86 TO NEG HEAT SINK ANS86 430618-5.0 SH1 3
 J87 TO POS HEAT SINK ANS87 430618-5.0 SH1 3
 J88 TO POS HEAT SINK ANS88 430618-5.0 SH1 3
 J89 TO POS HEAT SINK ANS89 430618-5.0 SH1 3

J90 TO NEG HEAT SINK ANS90 430618-5.0 SH1 3
 J91 TO POS HEAT SINK ANS91 430618-5.0 SH1 3
 J92 TO POS HEAT SINK ANS92 430618-5.0 SH1 3
 J93 TO POS HEAT SINK ANS93 430618-5.0 SH1 3

J94 TO NEG HEAT SINK ANS94 430618-5.0 SH1 3
 J95 TO POS HEAT SINK ANS95 430618-5.0 SH1 3
 J96 TO POS HEAT SINK ANS96 430618-5.0 SH1 3
 J97 TO POS HEAT SINK ANS97 430618-5.0 SH1 3

J98 TO NEG HEAT SINK ANS98 430618-5.0 SH1 3
 J99 TO POS HEAT SINK ANS99 430618-5.0 SH1 3
 J100 TO POS HEAT SINK ANS100 430618-5.0 SH1 3



| BEAD | COMPONENTS |
|------|----------------------------|
| 1 | R4, R1, R2, R3, R13 |
| 2 | R6, R7, R12, R14, R16, R15 |
| 3 | R10, R15 |

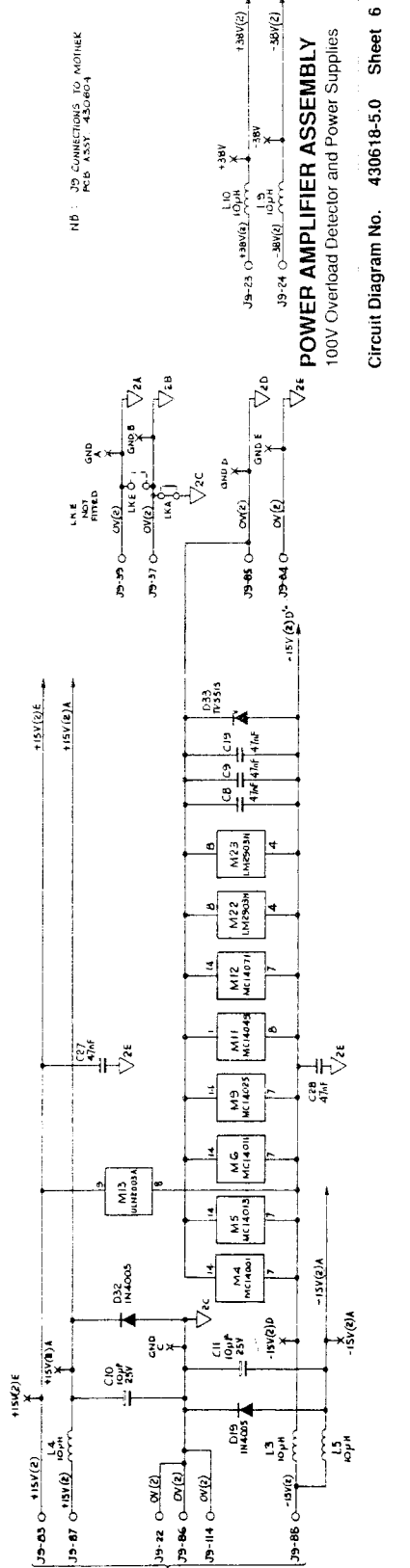
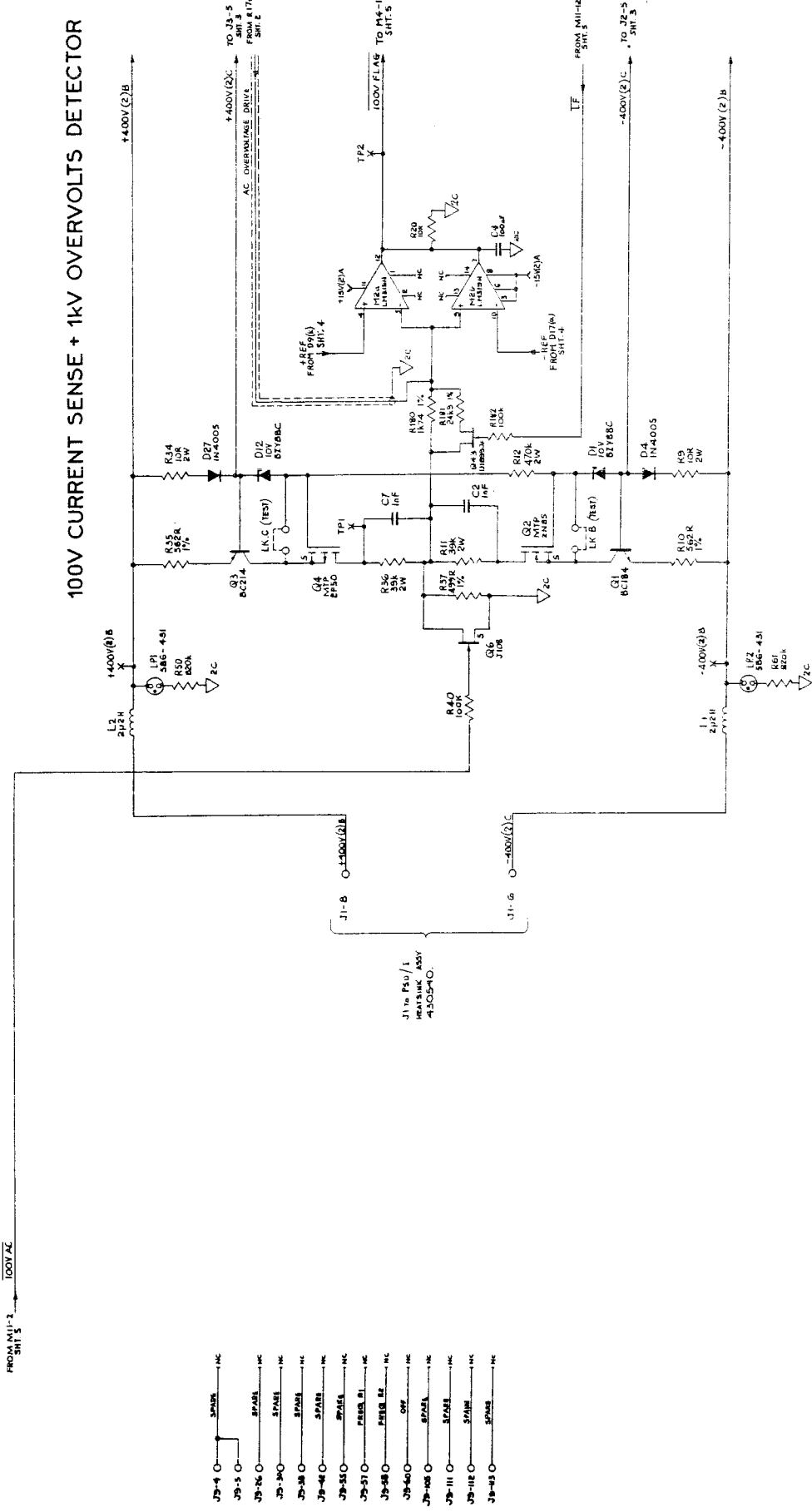
NOTE: THE FOLLOWING COMPONENTS TO BE ASSEMBLED ON THE BOARD: R15, R16, R17, R18, R19, R20, R21, R22, R23, R24, R25, R26, R27, R28, R29, R30, R31, R32, R33, R34, R35, R36, R37, R38, R39, R40, R41, R42, R43, R44, R45, R46, R47, R48, R49, R50, R51, R52, R53, R54, R55, R56, R57, R58, R59, R60, R61, R62, R63, R64, R65, R66, R67, R68, R69, R70, R71, R72, R73, R74, R75, R76, R77, R78, R79, R80, R81, R82, R83, R84, R85, R86, R87, R88, R89, R90, R91, R92, R93, R94, R95, R96, R97, R98, R99, R100, R101, R102, R103, R104, R105, R106, R107, R108, R109, R110, R111, R112, R113, R114, R115, R116, R117, R118, R119, R120, R121, R122, R123, R124, R125, R126, R127, R128, R129, R130, R131, R132, R133, R134, R135, R136, R137, R138, R139, R140, R141, R142, R143, R144, R145, R146, R147, R148, R149, R150, R151, R152, R153, R154, R155, R156, R157, R158, R159, R160, R161, R162, R163, R164, R165, R166, R167, R168, R169, R170.

| PART NO. | QTY | UNIT | USED |
|----------|-----|------|------|
| 6 | 1 | RES | 1 |
| 14 | 1 | RES | 1 |
| 16 | 1 | RES | 1 |
| 17 | 1 | RES | 1 |
| 18 | 1 | RES | 1 |
| 19 | 1 | RES | 1 |
| 20 | 1 | RES | 1 |
| 21 | 1 | RES | 1 |
| 22 | 1 | RES | 1 |
| 23 | 1 | RES | 1 |
| 24 | 1 | RES | 1 |
| 25 | 1 | RES | 1 |
| 26 | 1 | RES | 1 |
| 27 | 1 | RES | 1 |
| 28 | 1 | RES | 1 |
| 29 | 1 | RES | 1 |
| 30 | 1 | RES | 1 |
| 31 | 1 | RES | 1 |
| 32 | 1 | RES | 1 |
| 33 | 1 | RES | 1 |
| 34 | 1 | RES | 1 |
| 35 | 1 | RES | 1 |
| 36 | 1 | RES | 1 |
| 37 | 1 | RES | 1 |
| 38 | 1 | RES | 1 |
| 39 | 1 | RES | 1 |
| 40 | 1 | RES | 1 |
| 41 | 1 | RES | 1 |
| 42 | 1 | RES | 1 |
| 43 | 1 | RES | 1 |
| 44 | 1 | RES | 1 |
| 45 | 1 | RES | 1 |
| 46 | 1 | RES | 1 |
| 47 | 1 | RES | 1 |
| 48 | 1 | RES | 1 |
| 49 | 1 | RES | 1 |
| 50 | 1 | RES | 1 |
| 51 | 1 | RES | 1 |
| 52 | 1 | RES | 1 |
| 53 | 1 | RES | 1 |
| 54 | 1 | RES | 1 |
| 55 | 1 | RES | 1 |
| 56 | 1 | RES | 1 |
| 57 | 1 | RES | 1 |
| 58 | 1 | RES | 1 |
| 59 | 1 | RES | 1 |
| 60 | 1 | RES | 1 |
| 61 | 1 | RES | 1 |
| 62 | 1 | RES | 1 |
| 63 | 1 | RES | 1 |
| 64 | 1 | RES | 1 |
| 65 | 1 | RES | 1 |
| 66 | 1 | RES | 1 |
| 67 | 1 | RES | 1 |
| 68 | 1 | RES | 1 |
| 69 | 1 | RES | 1 |
| 70 | 1 | RES | 1 |
| 71 | 1 | RES | 1 |
| 72 | 1 | RES | 1 |
| 73 | 1 | RES | 1 |
| 74 | 1 | RES | 1 |
| 75 | 1 | RES | 1 |
| 76 | 1 | RES | 1 |
| 77 | 1 | RES | 1 |
| 78 | 1 | RES | 1 |
| 79 | 1 | RES | 1 |
| 80 | 1 | RES | 1 |
| 81 | 1 | RES | 1 |
| 82 | 1 | RES | 1 |
| 83 | 1 | RES | 1 |
| 84 | 1 | RES | 1 |
| 85 | 1 | RES | 1 |
| 86 | 1 | RES | 1 |
| 87 | 1 | RES | 1 |
| 88 | 1 | RES | 1 |
| 89 | 1 | RES | 1 |
| 90 | 1 | RES | 1 |
| 91 | 1 | RES | 1 |
| 92 | 1 | RES | 1 |
| 93 | 1 | RES | 1 |
| 94 | 1 | RES | 1 |
| 95 | 1 | RES | 1 |
| 96 | 1 | RES | 1 |
| 97 | 1 | RES | 1 |
| 98 | 1 | RES | 1 |
| 99 | 1 | RES | 1 |
| 100 | 1 | RES | 1 |
| 101 | 1 | RES | 1 |
| 102 | 1 | RES | 1 |
| 103 | 1 | RES | 1 |
| 104 | 1 | RES | 1 |
| 105 | 1 | RES | 1 |
| 106 | 1 | RES | 1 |
| 107 | 1 | RES | 1 |
| 108 | 1 | RES | 1 |
| 109 | 1 | RES | 1 |
| 110 | 1 | RES | 1 |
| 111 | 1 | RES | 1 |
| 112 | 1 | RES | 1 |
| 113 | 1 | RES | 1 |
| 114 | 1 | RES | 1 |
| 115 | 1 | RES | 1 |
| 116 | 1 | RES | 1 |
| 117 | 1 | RES | 1 |
| 118 | 1 | RES | 1 |
| 119 | 1 | RES | 1 |
| 120 | 1 | RES | 1 |
| 121 | 1 | RES | 1 |
| 122 | 1 | RES | 1 |
| 123 | 1 | RES | 1 |
| 124 | 1 | RES | 1 |
| 125 | 1 | RES | 1 |
| 126 | 1 | RES | 1 |
| 127 | 1 | RES | 1 |
| 128 | 1 | RES | 1 |
| 129 | 1 | RES | 1 |
| 130 | 1 | RES | 1 |
| 131 | 1 | RES | 1 |
| 132 | 1 | RES | 1 |
| 133 | 1 | RES | 1 |
| 134 | 1 | RES | 1 |
| 135 | 1 | RES | 1 |
| 136 | 1 | RES | 1 |
| 137 | 1 | RES | 1 |
| 138 | 1 | RES | 1 |
| 139 | 1 | RES | 1 |
| 140 | 1 | RES | 1 |
| 141 | 1 | RES | 1 |
| 142 | 1 | RES | 1 |
| 143 | 1 | RES | 1 |
| 144 | 1 | RES | 1 |
| 145 | 1 | RES | 1 |
| 146 | 1 | RES | 1 |
| 147 | 1 | RES | 1 |
| 148 | 1 | RES | 1 |
| 149 | 1 | RES | 1 |
| 150 | 1 | RES | 1 |
| 151 | 1 | RES | 1 |
| 152 | 1 | RES | 1 |
| 153 | 1 | RES | 1 |
| 154 | 1 | RES | 1 |
| 155 | 1 | RES | 1 |
| 156 | 1 | RES | 1 |
| 157 | 1 | RES | 1 |
| 158 | 1 | RES | 1 |
| 159 | 1 | RES | 1 |
| 160 | 1 | RES | 1 |
| 161 | 1 | RES | 1 |
| 162 | 1 | RES | 1 |
| 163 | 1 | RES | 1 |
| 164 | 1 | RES | 1 |
| 165 | 1 | RES | 1 |
| 166 | 1 | RES | 1 |
| 167 | 1 | RES | 1 |
| 168 | 1 | RES | 1 |
| 169 | 1 | RES | 1 |
| 170 | 1 | RES | 1 |

Mount D9, D1, D25 & D29 on the mounting pads 630014 407P

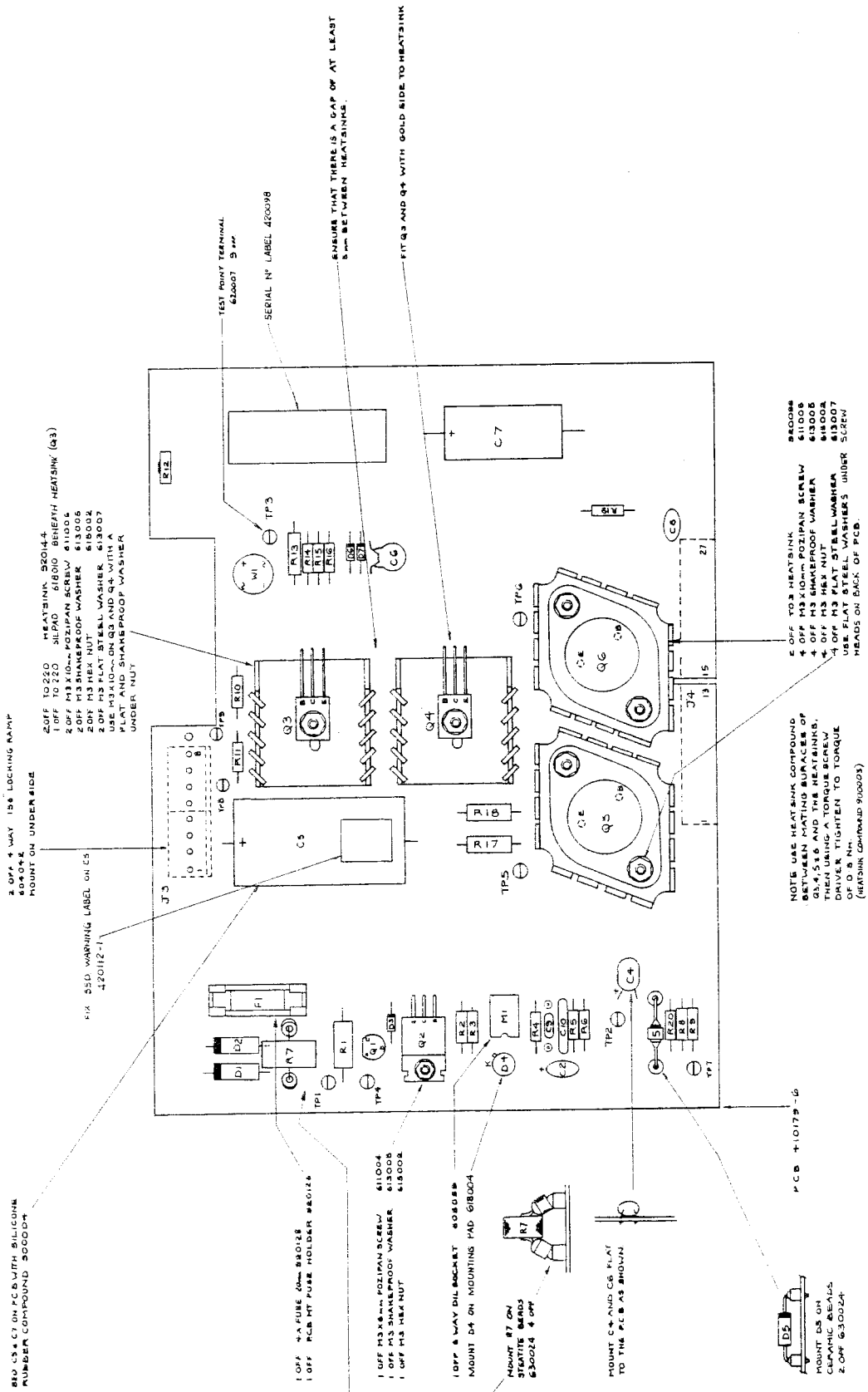
PCB 310335 2

100V CURRENT SENSE + 1kV OVERVOLTS DETECTOR



POWER AMPLIFIER ASSEMBLY

100V Overload Detector and Power Supplies
 Circuit Diagram No. 430618-5.0 Sheet 6



820 0.5A C7 ON PCB WITH SILICONE NUMBER COMPOUND 90000+

2 OFF 4 WAY 156 LOCKING RAMP 804042 POINT ON UNDER SIDE

2 OFF 10 220 5% 1/4W (RADIAL) HEATSINK (Q3)
 2 OFF M3 X 1.0mm POZIPAN SCREW 411004
 2 OFF M3 SHANKPROOF WASHER 410004
 2 OFF M3 FLAT STEEL WASHER 413007
 USE M3 X 1.0mm ON Q3 AND Q4 WITH A SHANKPROOF WASHER UNDER NUT

FIX 350 WARNING LABEL ON C5 420112-1

1 OFF 4X FUSE 20mm BR028
 1 OFF PCB MOUNT FUSE HOLDER 860124

1 OFF M3 X 1.0mm POZIPAN SCREW 411004
 1 OFF M3 SHANKPROOF WASHER 410004
 1 OFF M3 HEX NUT

1 OFF 4 WAY DIL SOCKET 808058
 MOUNT ON MOUNTING PAD 618004

MOUNT 87 ON MOUNTING PAD 618004 4 OFF

MOUNT C6 AND C6 FLAT TO THE PCB AS SHOWN

PCB 1-10179-6
 MOUNT D8 ON CERAMIC BEADS 2 OFF 630024

NOTE USE HEAT SINK COMPOUND BETWEEN MATING SURFACES OF Q3, Q4, S1 & THE HEAT SINKS. DRIVERS TIGHTEN TO TORQUE OF 0.8 Nm. (HEAT SINK COMPOND 910003)

2 OFF Q3 HEAT SINK
 4 OFF M3 X 1.0mm POZIPAN SCREW 411004
 4 OFF M3 SHANKPROOF WASHER 410004
 4 OFF M3 HEX NUT 410004
 4 OFF M3 FLAT STEEL WASHER 413007
 USE FLAT STEEL WASHERS UNDER SCREW HEADS ON BACK OF PCB.

ENSURE THAT THERE IS A GAP OF AT LEAST 8mm BETWEEN HEAT SINKS.

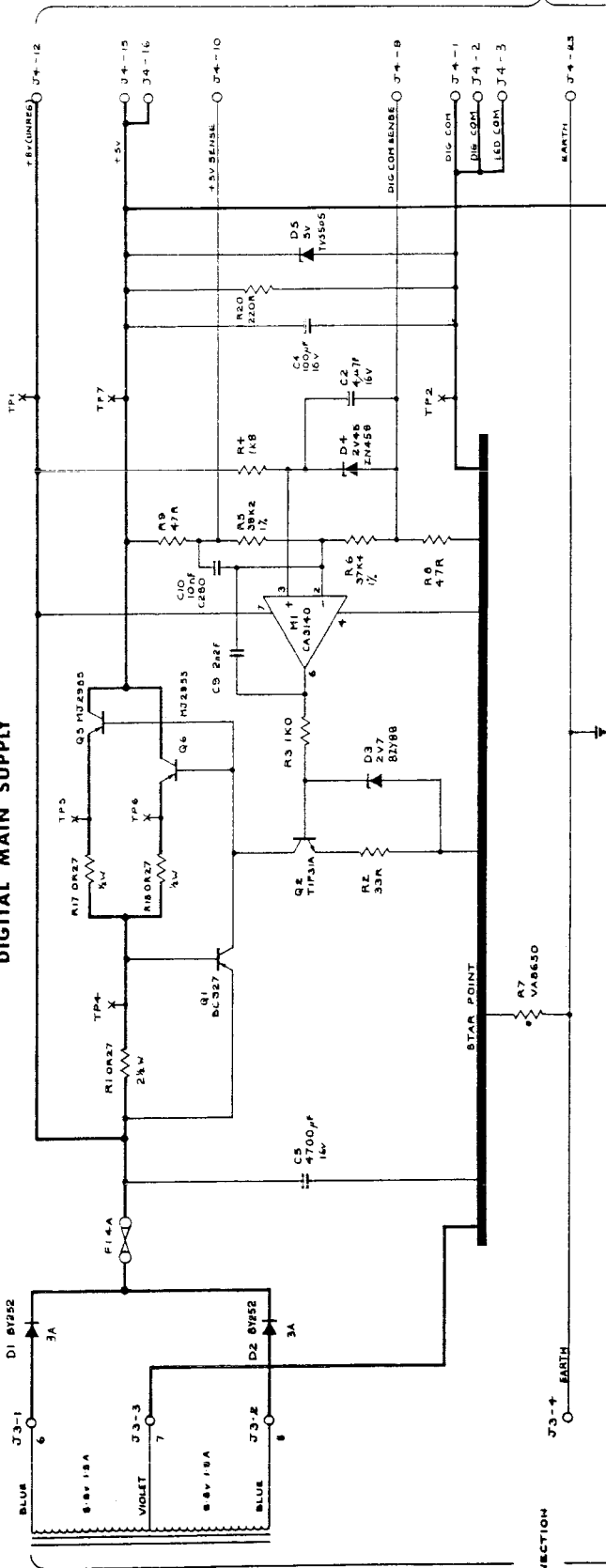
FIT Q3 AND Q4 WITH GOLD SIDE TO HEAT SINK

TEST POINT TERMINAL 610007 5 WIP

SERIAL N° LABEL 420098

MAINS TRANSFORMER

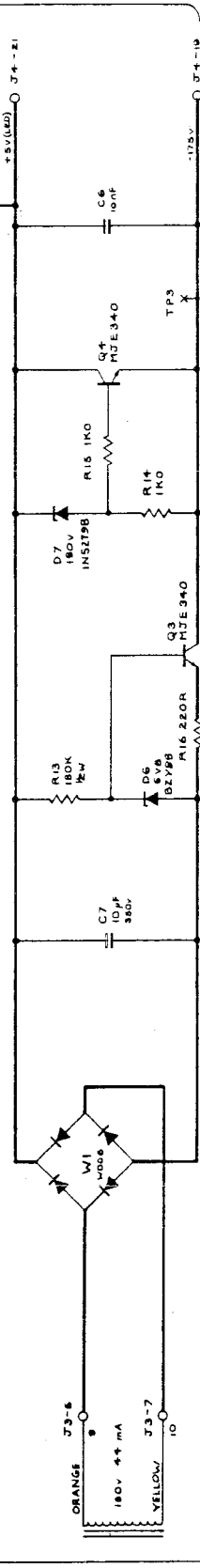
DIGITAL MAIN SUPPLY



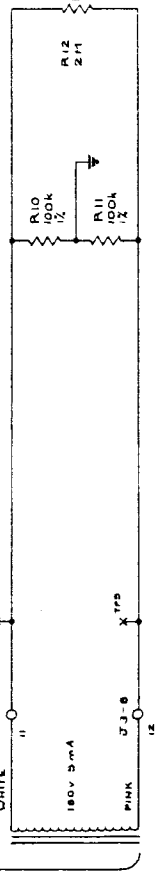
TO J20
 43053Z (4200)
 43050+ (4700)
 (J4-23 ALSO GOES
 TO REAR PANEL
 EARTH SCREW)

PRIMARY
 AND/OR
 INTERCONNECTION
 P.C.B.
 430-38

DISPLAY SUPPLY

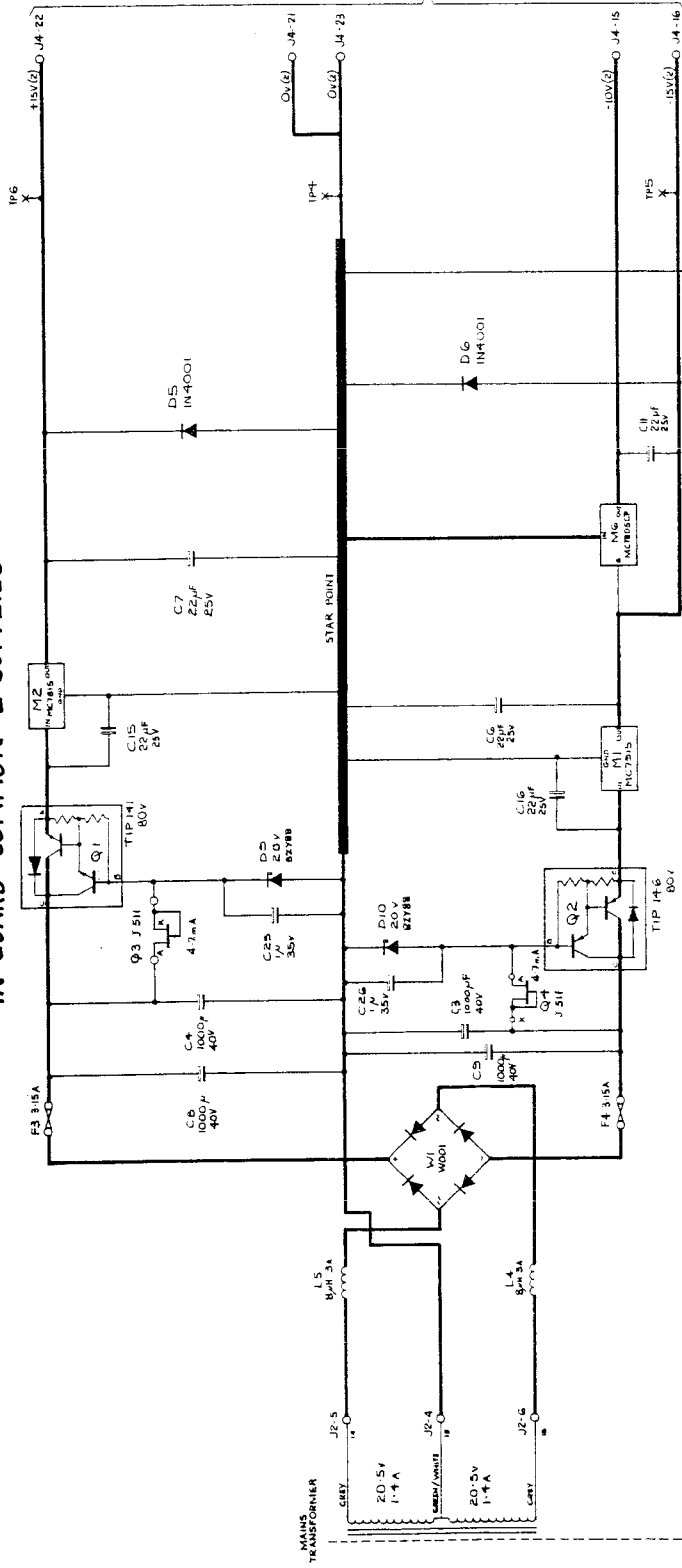


COMMON MODE NULL (O.G.)

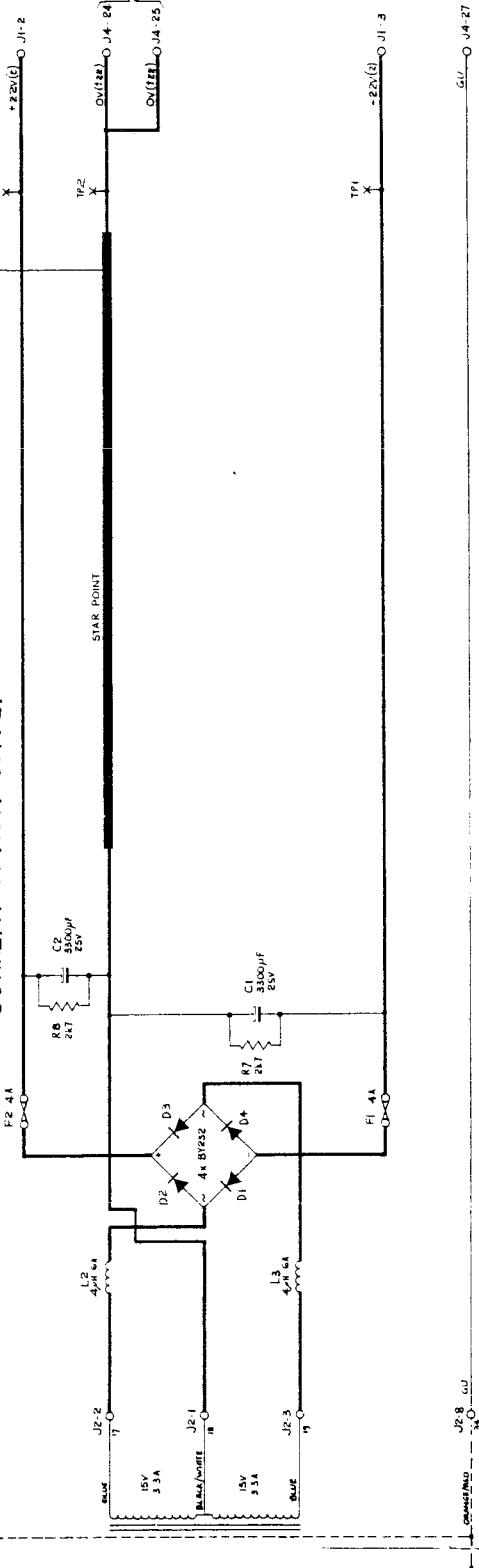


TO J4-27
 P5 (16) P.C.B.
 430554

IN GUARD COMMON 2 SUPPLIES



CURRENT OPTION SUPPLY



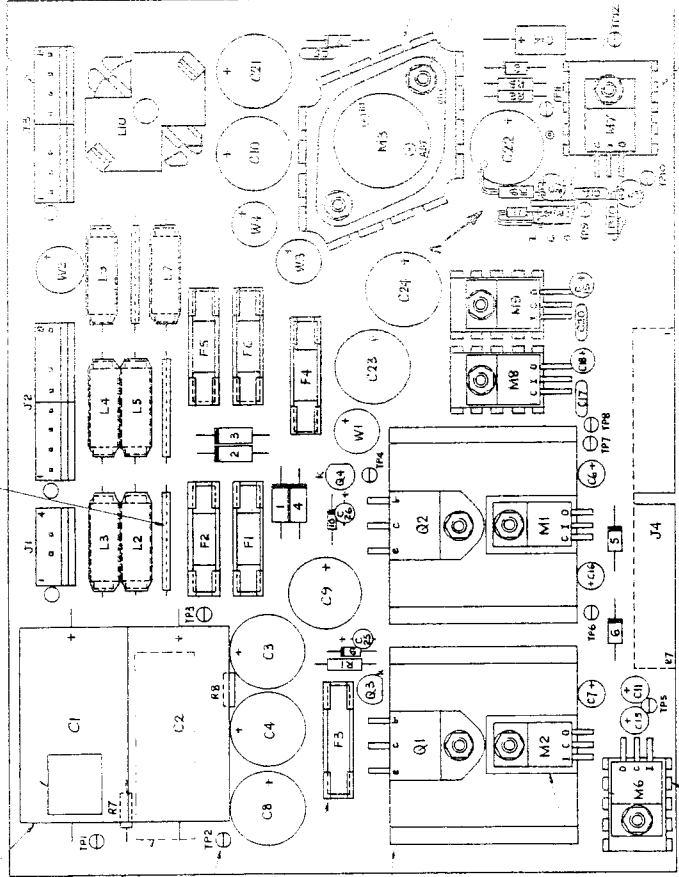
IN-GUARD POWER SUPPLY ASSEMBLY
Common-2 and Current Option Supplies
Circuit Diagram No. 430554-4.2 Sheet 1

REVISED DRAWING 6/10/74
BY WJ

LINKS, USE 3000002 THINDED CENTER LINK
SLEEVED WITH SHIM'S P/N 3000004

FIX SSD WARNING LABEL TO CI
450102-1

GLUE CI AND C2 IN SILICONE
RUBBER (3000004)



PC B 410282-2

FIX SERIAL PT LABEL
420098 ON REVERSE SIDE

TEST POINT TERMINAL
620007 1459

6 OFF FUSE HOLDERS 520126
2 OFF FUSE (1/4A 5B) 520143 P4
2 OFF FUSE (1/4A 5B) 520143 P4
2 OFF FUSE (1/4A 5B) 520143 P4
2 OFF FUSE (1/4A 5B) 520143 P4

2 OFF HEATSINK 520142

MOUNT M1 AND M2 ON TO HEATSINKS
WITH A SIL PAD 618010 2 OFF
SECURE WITH N3-1000000 NUT/PAN 618006
INSULATING BUSH (FOR UNDER SCREW) M3
SHAKEPROOF 613003
INSULATING BUSH 618001 2 OFF

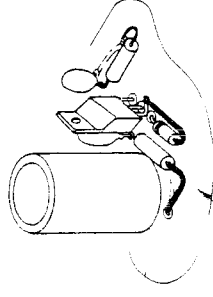
3 OFF HEATSINK (10202) 520105

81, 82, M3, M6-M9 FININGS
8 OFF M3 WASH 618007
8 OFF M3 WASH 618007
8 OFF M3 WASH 618007
8 OFF M3 WASH 618007

NOTE:
USE HEATSINK COMPOUND (800005) BETWEEN M9
AND THEIR RESPECTIVE HEATSINKS. A TORQUE OF
0.5-1.0 INCH SHOULD BE APPLIED TO TIGHTEN COMPONENT
FININGS
SELECT HEAD 620045 FITTED TO EACH LEG OF CIR 07 1020

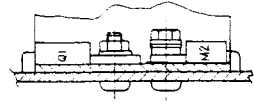
1 OFF HEATSINK (102) 520088

1 OFF M3 WASHER 618007
FIT UNDER SCREW HEAD

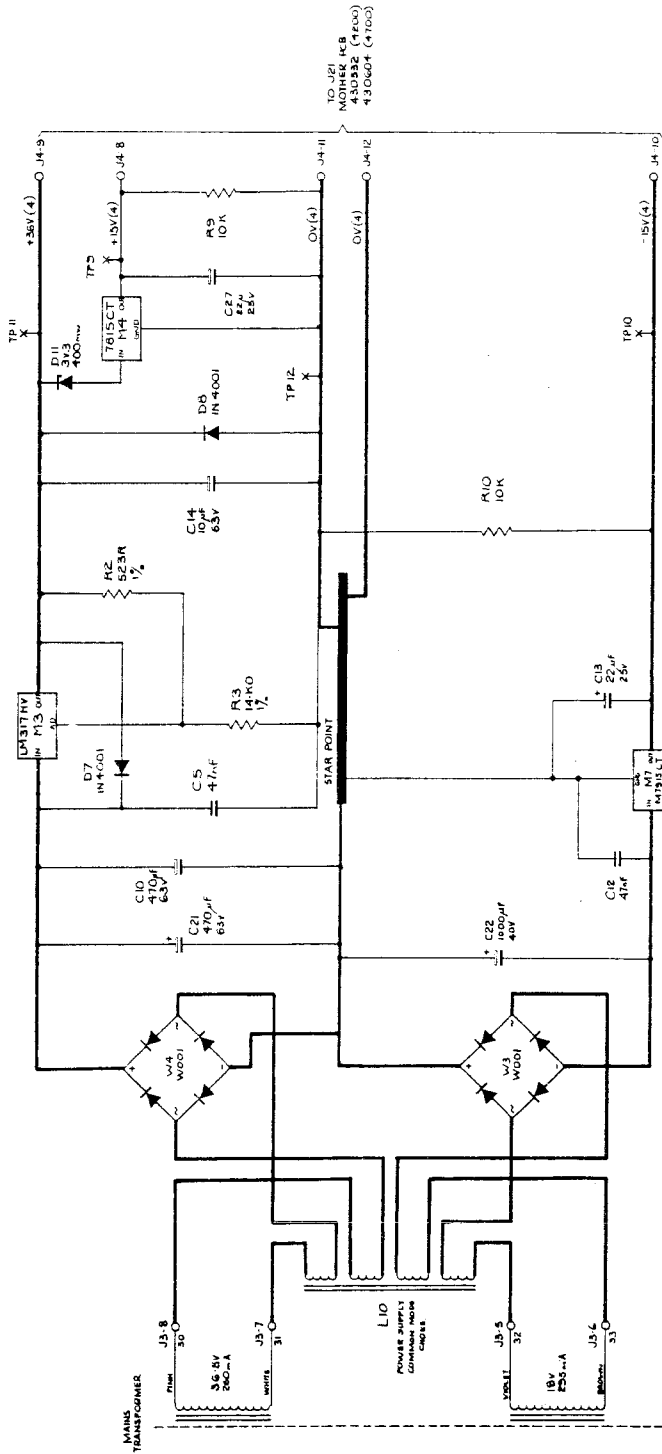


FIT CLUED COMPONENTS AS SHOWN
ABOVE. SLEEVE LEADS INDICATED
WITH 550004

VIEWED FROM DIRECTION OF ARROW A

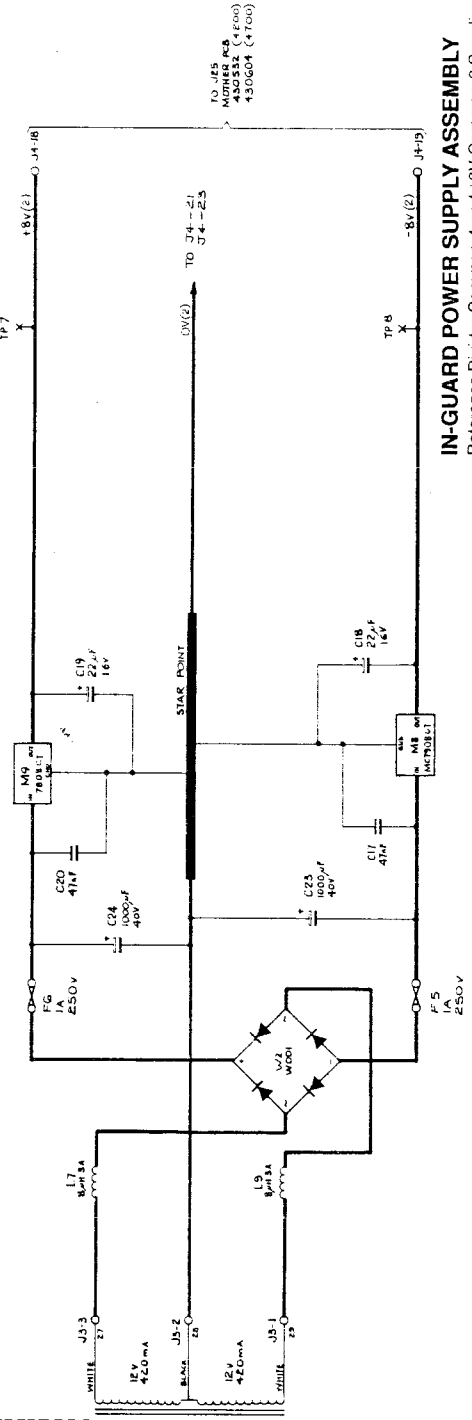


REFERENCE DIVIDER COMMON 4 SUPPLIES



TO J21
MOTHER PCB
430532 (+200)
430604 (+700)

IN GUARD COMMON 2 ±8V SUPPLY



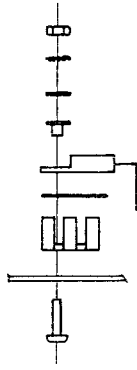
TO J55
MOTHER PCB
430532 (+200)
430604 (+700)

PRIMARYS
SHOWN ON
INTERCONNECTION PCB
430415

±8V GROUND SCREEN
CONNECTION SHOWN

IN-GUARD POWER SUPPLY ASSEMBLY
Reference Divider Common-4 and ±8V Common-2 Supplies

Circuit Diagram No. 430554-4.0 Sheet 2



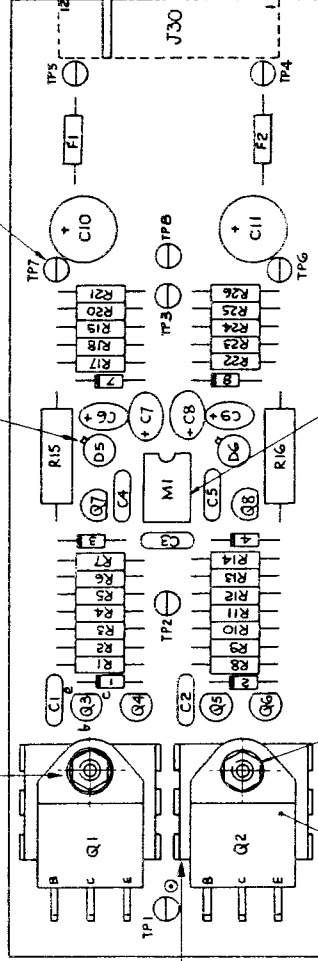
MOUNT Q1 USING THE FOLLOWING :-

- M3X10mm POZI-PAN SCREW G1000G 1 off.
- INSULATING PAD G18014 1 off.
- INSULATING BUSH G18001 1 off.
- M3 WASHER STEEL G15007 1 off.
- M3 INT SHAKE PROOF G15005 1 off.
- M3 NUT G15002 1 off.

MOUNT D5 & D6 ON MOUNTING PADS G18004 2 off.

TEST POINT PIN G20007 B off

PCB. 410254-2



HEATSINK (TOZZO) S20141 2 off.

USE HEATSINK COMPOUND S00003 BETWEEN MOUNTING SURFACES OF HEATSINK AND Q2.

M3X6mm POZI-PAN SCREW G11016 1 off (TO SECURE Q2)
M3 SHAKEPROOF G15005 1 off
M3 NUT G15002 1 off

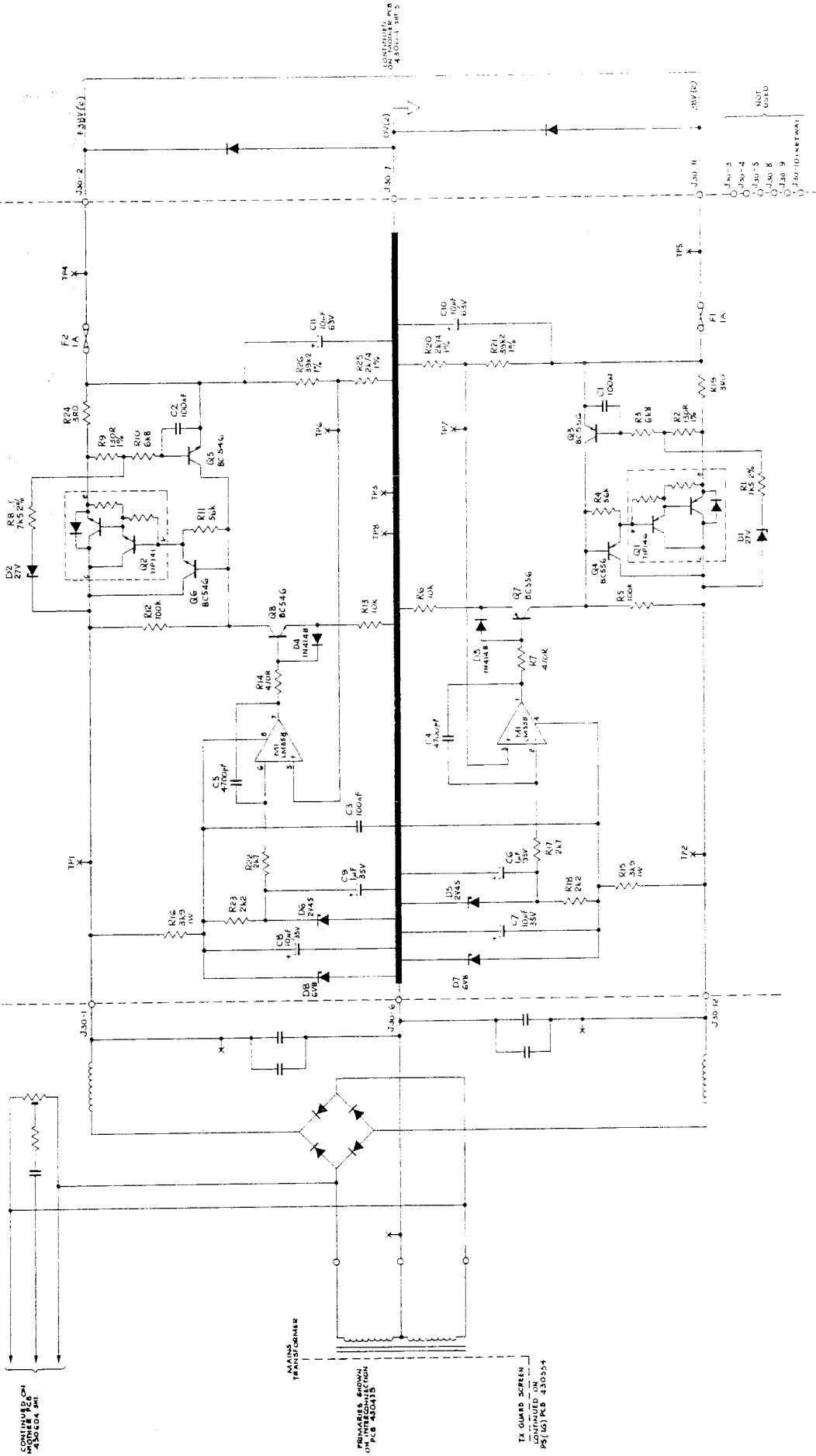
MOUNT M1 ON 8WAY DIL SRT G05059/A

PCB. 410254-2

MOTHER PCB ASSY
400604

PS (38V) PCB ASSY
400653

MOTHER PCB ASSY
400604



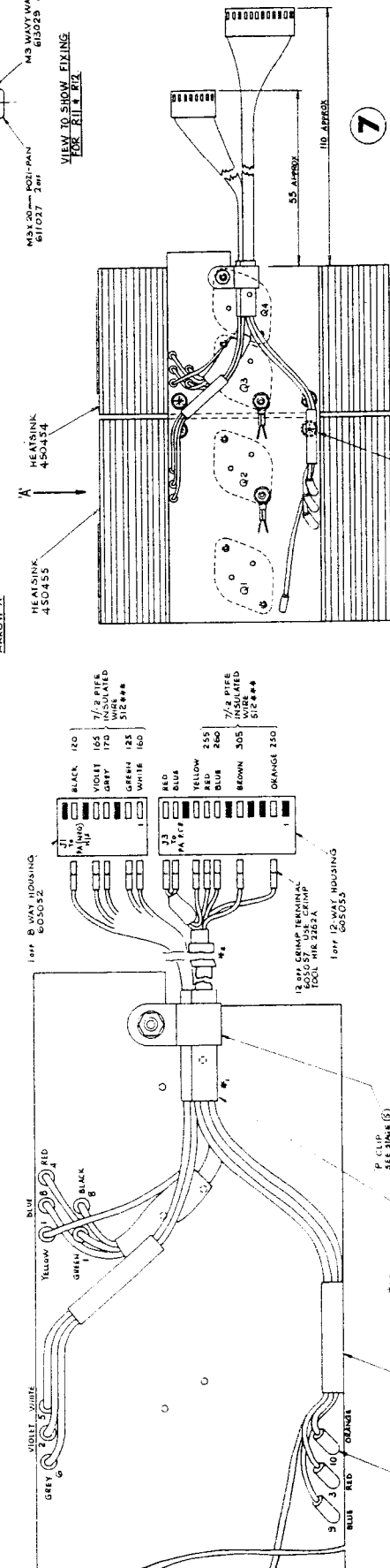
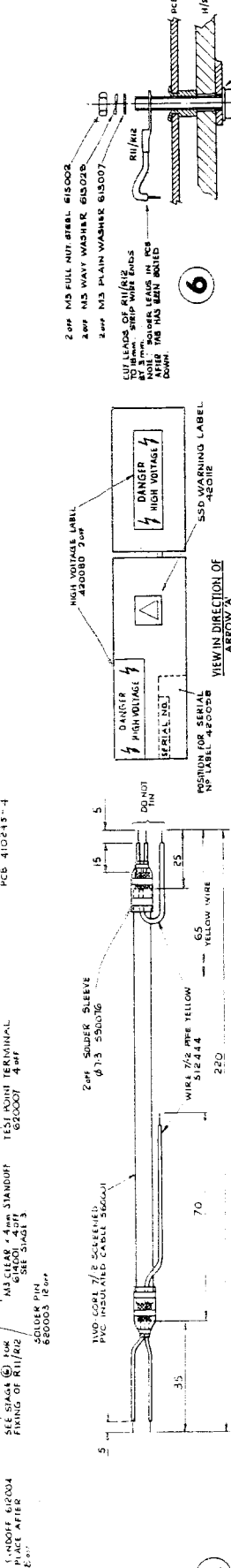
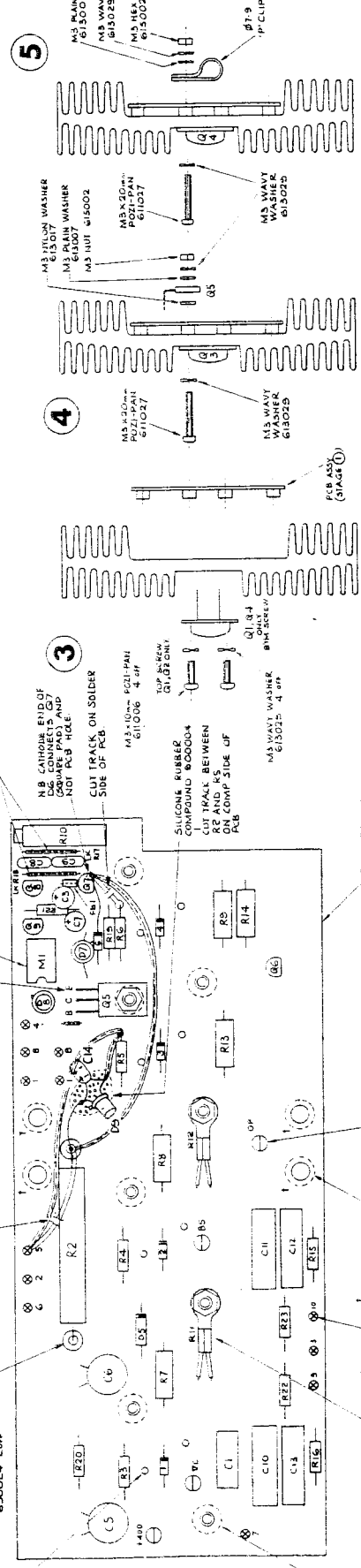
±38V POWER SUPPLY ASSEMBLY
±38V Power Supply with Mother Assembly Components

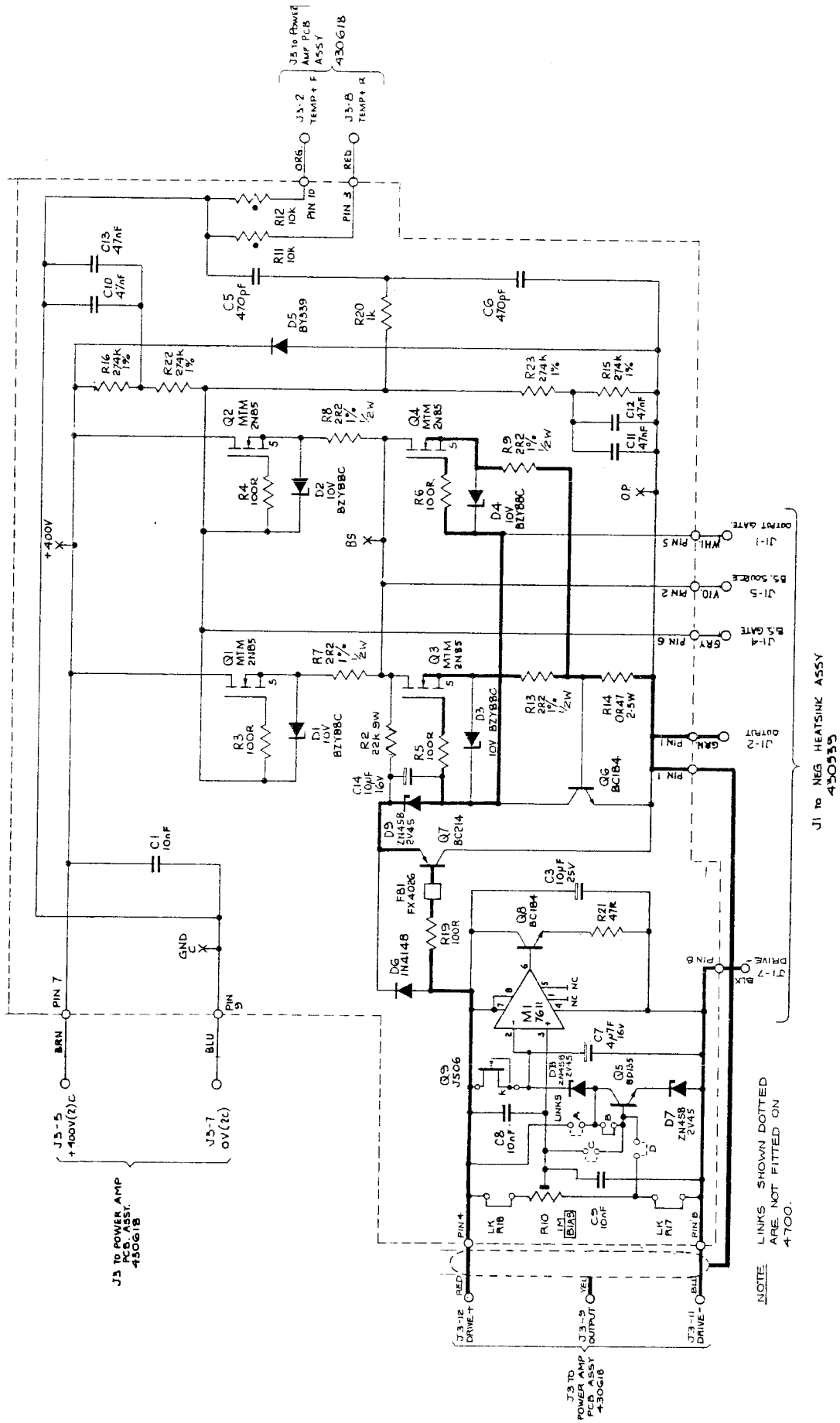
Circuit Diagram No. 430653-1.0 Sheet 1

POSITIVE HEATSINK ASSEMBLY

- ASSEMBLY NOTES:
- ASSEMBLY FIG. 1 TO STAGE 5 EXCEPT SCREW FINING FOR Q5 (SEE STAGE 6)
 - COMPLETE PCB ASSY BY FITTING WIRING LOOKS DO NOT FIT P CLIP (SEE STAGE 6)
 - ASSEMBLE PCB ASSY TO HEATSINKS, FITTED BY 4 MIDSIZE SCREWS (SEE STAGE 6)
 - MOUNT Q1-Q4 TO STAGE 3 ASSEMBLY IN THE POSITION SHOWN (STAGE 7); APPLY HEADSINK COMPOUND 800003 BETWEEN MATING SURFACES. USE A TORQUE SCREWDRIVER TO TIGHTEN ALL TRANSISTOR FIRING SCREWS TO TORQUE OF 0.8 MM.
 - SECURE WIRING WITH P CLIP (STAGE 6)

MAIN SINKS WITH PINS, BEG WIRE 840002 (45)





J3 TO POWER AMP PCB ASSY 430618

J3 TO POWER AMP PCB ASSY 430618

NOTE: LINKS SHOWN DOTTED ARE NOT FITTED ON 4-700.

J1 TO NEG HEATSINK ASSY 430635

POSITIVE HEATSINK ASSEMBLY
Output Power Amplifier (Positive Half)

Circuit Diagram No. 430637-1.2 Sheet 1

NEGATIVE HEATSINK ASSEMBLY

ASSEMBLY NOTES:

- 1 ASSEMBLE PCB TO STAGE ①
- 2 COMPLETE PCB ASSY BY FITTING WIRING LOOM. DO NOT FIT 'P' CLIP (SEE STAGE ⑤)
- 3 ASSEMBLE PCB ASSY TO HEATSINKS, FITTED BY 4 MIDDLE SCREWS (SEE STAGE ②)
- 4 MOUNT Q1-Q7 TO STAGE ③ ASSEMBLY IN THE POSITION SHOWN (STAGE ③), APPLY SILICONE RUBBER GROUT IN THE MOUNTING HOLES AS SHOWN IN STAGE ③, TIGHTEN SCREWS TO TIGHTEN ALL TRANSISTOR FIXING SCREWS TO A TORQUE OF 0.78 Nm.
- 5 SECURE WIRING WITH 'P' CLIP (STAGE ⑤)

1

MOUNT Q8 WITH FERRITE BEAD
SCREWS ON CENTER LEG, AS SHOWN

CUT FLACK ON COMP. SIDE
R5 BEFORE FITTING DIS C/5

GLUE CURE

SILICONE RUBBER
5900004

MOUNT R12 ON 16.5mm CER BEAD
630024 2 OFF

CUT FLACK ON COMP. SIDE
R5 BEFORE FITTING DIS C/5
GLUE CURE

CLIP FLACK ON COMP. SIDE
OF Q7 TO Q8
WITH 5900004

GLUE FLAT FACE
OF Q7 TO Q8
WITH 5900004

M2X10mm PZL-PAN
611027 7 OFF

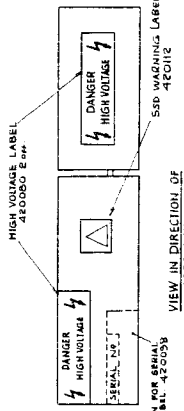
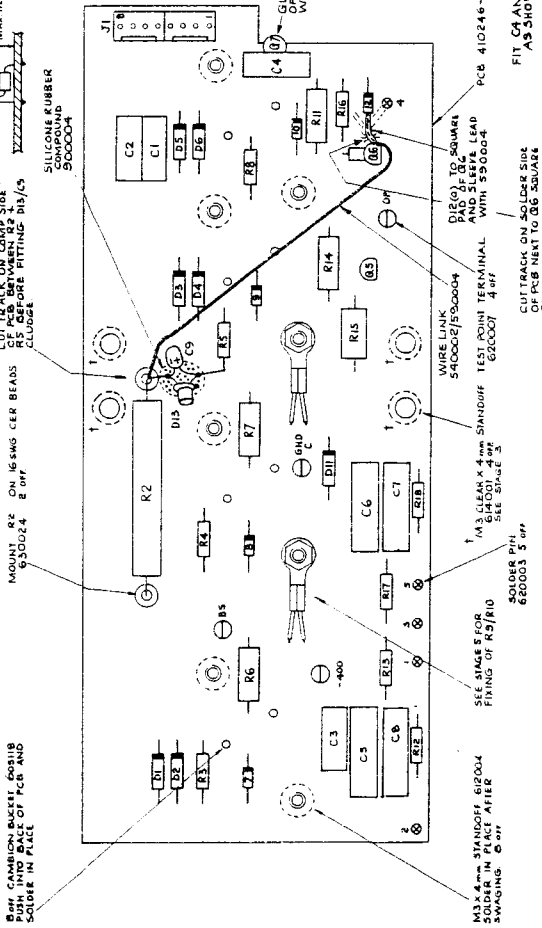
M3 WAVY WASHER
613029 7 OFF

Q1-Q7

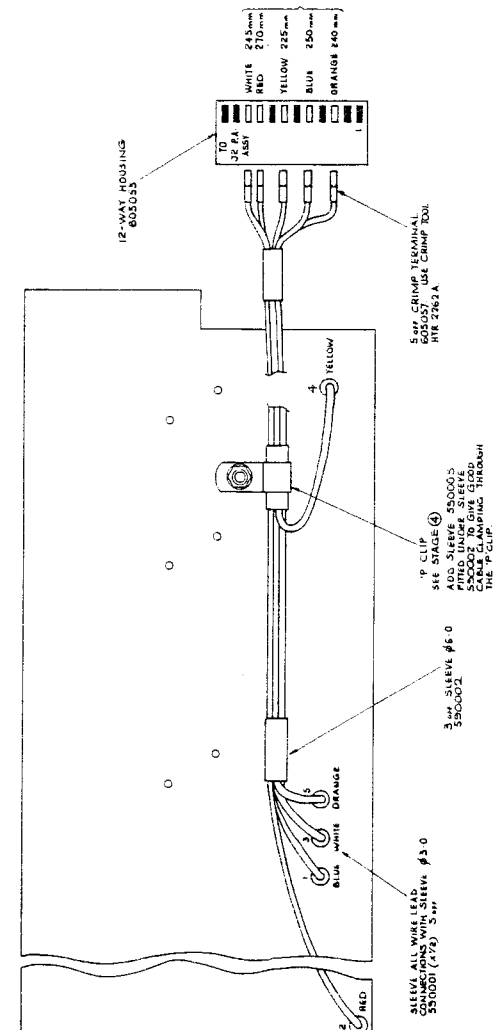
PCB ASSY
(STAGE ①)

M2X10mm PZL-PAN
611027 7 OFF

M3 WAVY WASHER
613029 7 OFF



2



MOUNT R12 ON 16.5mm CER BEAD
630024 2 OFF

CUT FLACK ON COMP. SIDE
R5 BEFORE FITTING DIS C/5
GLUE CURE

SILICONE RUBBER
5900004

MOUNT R12 ON 16.5mm CER BEAD
630024 2 OFF

CUT FLACK ON COMP. SIDE
R5 BEFORE FITTING DIS C/5
GLUE CURE

CLIP FLACK ON COMP. SIDE
OF Q7 TO Q8
WITH 5900004

GLUE FLAT FACE
OF Q7 TO Q8
WITH 5900004

M2X10mm PZL-PAN
611027 7 OFF

M3 WAVY WASHER
613029 7 OFF

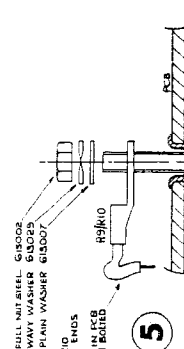
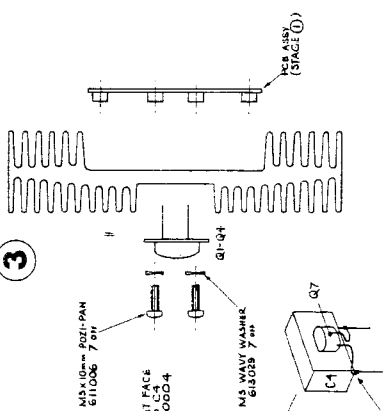
Q1-Q7

PCB ASSY
(STAGE ①)

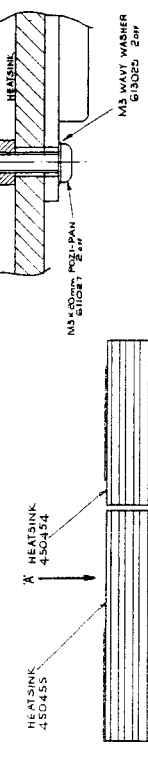
M2X10mm PZL-PAN
611027 7 OFF

M3 WAVY WASHER
613029 7 OFF

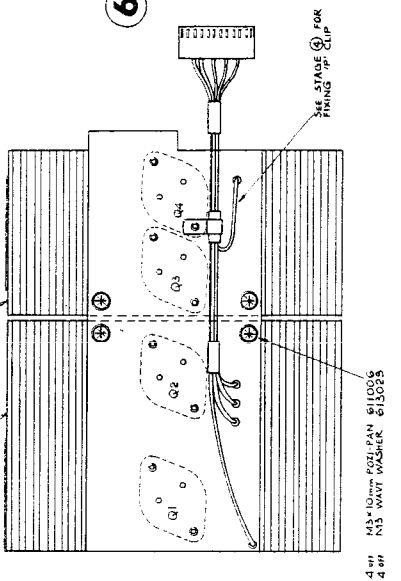
3



5



6



4 OFF M3x10mm PZL-PAN
611027

4 OFF M3 WAVY WASHER
613029

HEATSINK
450454

HEATSINK
450454

M3x10mm PZL-PAN
611027

M3 WAVY WASHER
613029

M3 WAVY WASHER
613029

M3 HEX NUT
613025

M3 PLAIN WASHER
613025

'P' CLIP 630003

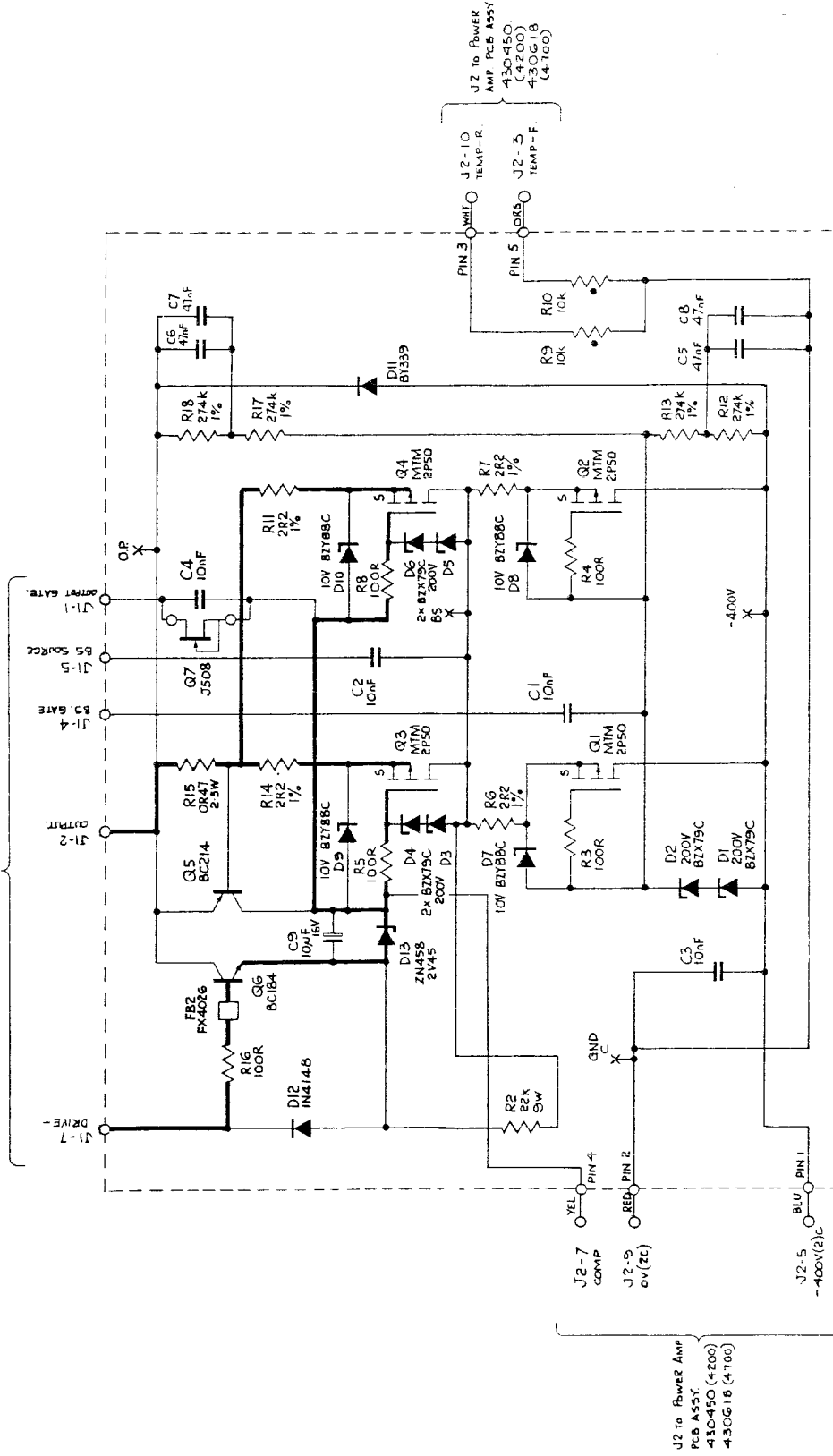
M3 WAVY WASHER
613029

M3 WAVY WASHER
613029

M3 HEX NUT
613025

M3 PLAIN WASHER
613025

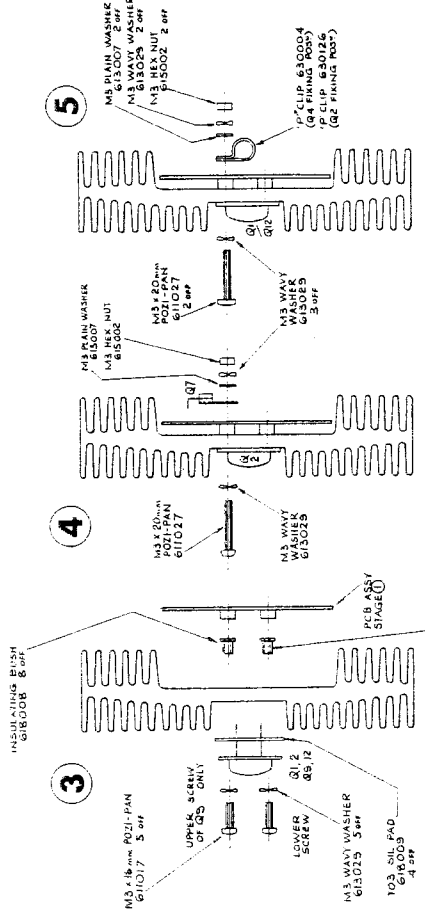
J1 To Pos. HEATSINK ASSY 430637 (4200/4700)



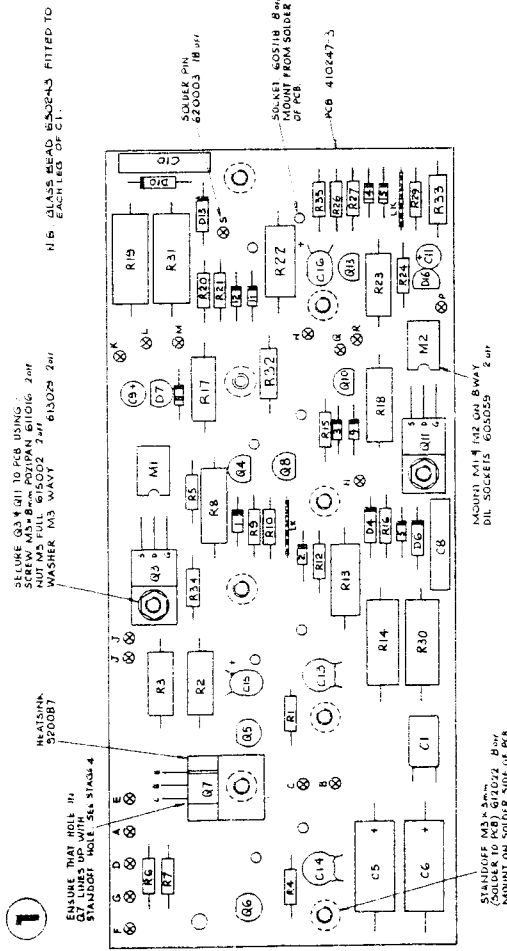
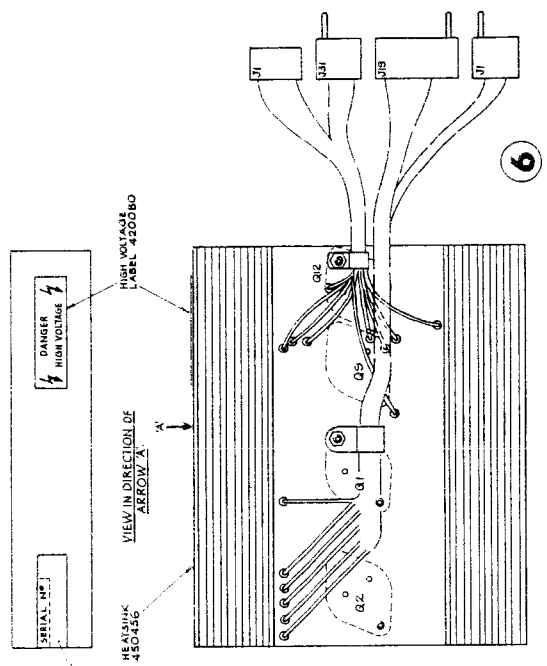
J2 TO POWER AMP PCB ASSY
430450 (4200)
430G18 (4700)

PS / I HEATSINK ASSEMBLY

- ASSEMBLY NOTES:
- 1 ASSEMBLE PCB TO STAGE ① EXCEPT SCREW FOR SECURING Q7 (SEE STAGE ④)
 - 2 COMPLETE PCB ASSY BY FITTING WIRING LOOKS DO NOT FIT P CLIPS (SEE STAGE ⑤)
 - 3 ASSEMBLE PCB ASSY TO HEATSINK BY FITTING Q12, Q19, Q12 (SEE STAGE ⑥)
 - 4 SECURE Q7 (STAGE ④) TO TIGHTEN ALL TRANSISTOR FIXING SCREWS TO A TORQUE OF 0.8 Nm
 - 5 SECURE WIRING WITH P CLIPS (SEE STAGES ② AND ③)



POSITION ALL INSULATING BUSHES INTO RESPECTIVE HOLES OF HEATSINK BEFORE POSITIONING PCB ASSY



1 ENSURE THAT HOLE IN Q7 LINES UP WITH STANDBY HOLE SEE STAGE ④

2 ENSURE Q3 & Q11 TO PCB USING SCREW M3-8mm POSI-PAN 611017 WASHER M3 WAVY WASHER 61025 2 off 61029 2 off

3 N16 GLASS HEAD B30P43 FITTED TO EACH LEG OF C1

4 SOLETS 20mm 610055 18 off

5 SOLETS 605118 8 off

6 SOLETS 605118 8 off

7 SOLETS 605118 8 off

8 SOLETS 605118 8 off

9 SOLETS 605118 8 off

10 SOLETS 605118 8 off

11 SOLETS 605118 8 off

12 SOLETS 605118 8 off

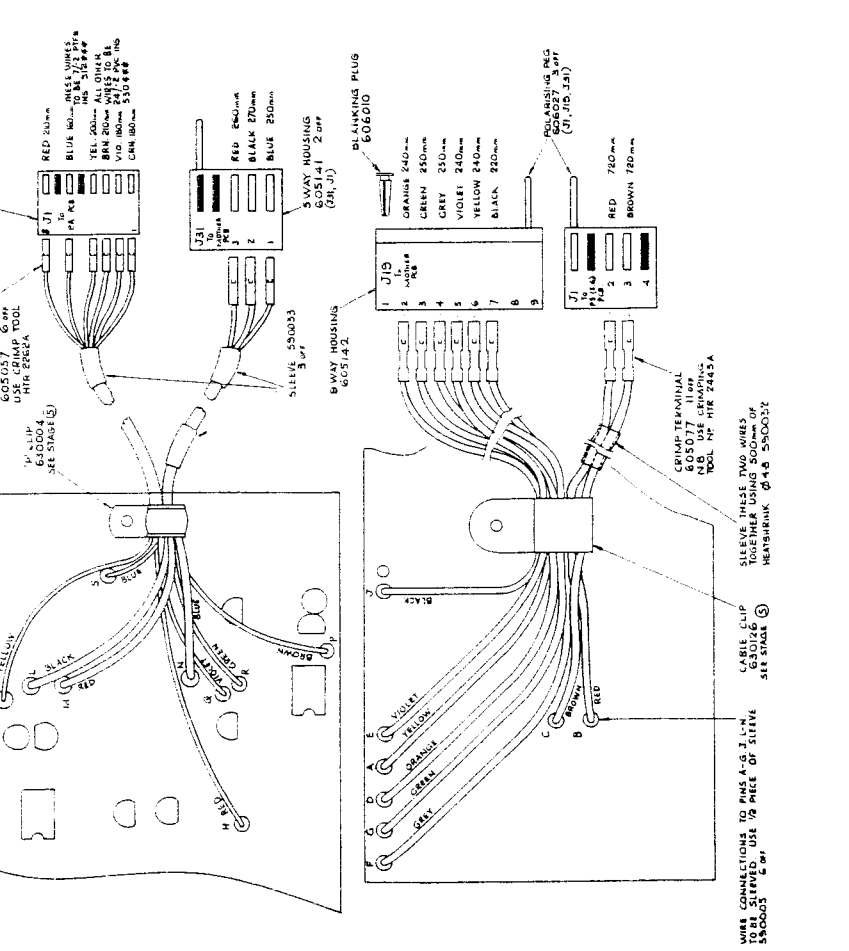
13 SOLETS 605118 8 off

14 SOLETS 605118 8 off

15 SOLETS 605118 8 off

16 WIRE CONNECTIONS TO PINS K & R 46 TO BE SLEEVED - USE 1/2 PEELE OF SLEEVE 590001 3 off

17 WIRE CONNECTIONS TO PINS A-G 31, C-N TO BE SLEEVED - USE 1/2 PEELE OF SLEEVE 590001 3 off



2 WIRE CONNECTIONS TO PINS K & R 46 TO BE SLEEVED - USE 1/2 PEELE OF SLEEVE 590001 3 off

3 WIRE CONNECTIONS TO PINS A-G 31, C-N TO BE SLEEVED - USE 1/2 PEELE OF SLEEVE 590001 3 off

4 CRIMP TERMINAL 605037 6 off

5 CRIMP TOOL HIR 27624

6 B-WAY HOUSING 605141 2 off

7 5-WAY HOUSING 605141 2 off

8 BLANKING PLUG 606010

9 POLARISING PIG 605141 2 off

10 CRIMP TERMINAL 605077 11 off

11 CRIMP TOOL HIR 27624

12 WIRE CONNECTIONS TO PINS A-G 31, C-N TO BE SLEEVED - USE 1/2 PEELE OF SLEEVE 590001 3 off

13 SLEEVE THESE TWO WIRES TOGETHER USING 500mm OF HEATSINK 6045 590032

14 CABLE CLIP 630126

15 SEE STAGE ⑤

16 SLEEVE THESE TWO WIRES TOGETHER USING 500mm OF HEATSINK 6045 590032

17 CABLE CLIP 630126

18 SEE STAGE ⑤

19 SLEEVE THESE TWO WIRES TOGETHER USING 500mm OF HEATSINK 6045 590032

20 CABLE CLIP 630126

21 SEE STAGE ⑤

22 SLEEVE THESE TWO WIRES TOGETHER USING 500mm OF HEATSINK 6045 590032

23 CABLE CLIP 630126

24 SEE STAGE ⑤

25 SLEEVE THESE TWO WIRES TOGETHER USING 500mm OF HEATSINK 6045 590032

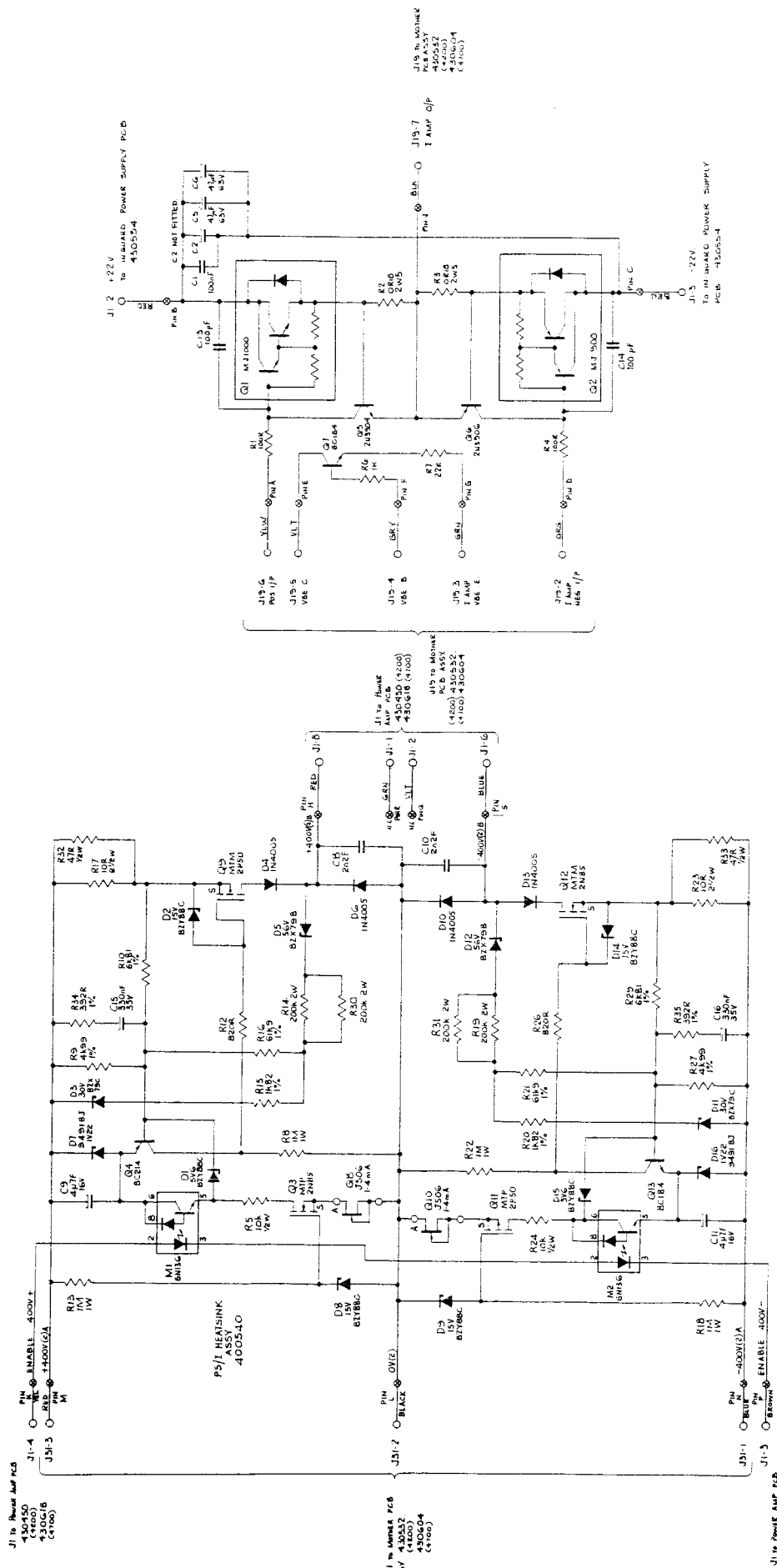
26 CABLE CLIP 630126

27 SEE STAGE ⑤

28 SLEEVE THESE TWO WIRES TOGETHER USING 500mm OF HEATSINK 6045 590032

29 CABLE CLIP 630126

30 SEE STAGE ⑤



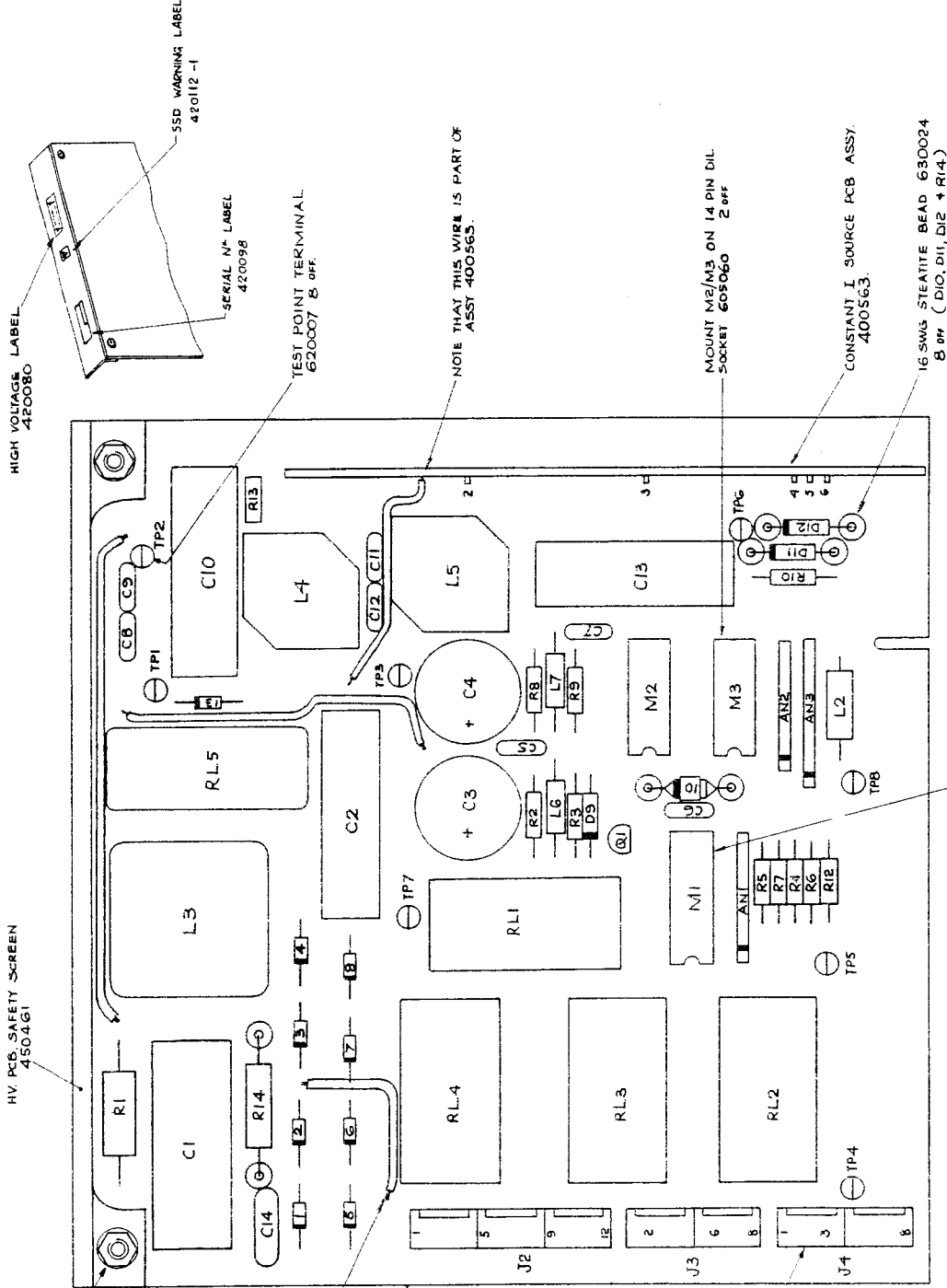
J1 to Heatsink PCB
 430550
 430552
 430554
 430618
 430619
 430620

J15 to Heatsink PCB
 430552
 430554
 430618
 430619
 430620

J1 to Power Amp PCB
 430550
 430552
 430618
 430619
 430620

HIGH VOLTAGE ASSEMBLY

1. R11 AND R13 NOT FITTED TO PCB
2. GLASS BEAD 630043 FITTED TO EACH LEG OF THE FOLLOWING COMPONENTS: C5-C7



HV PCB SAFETY SCREEN
450461

2 off SCREW M3X10mm POZI-PAN G1100G
2 off NUT M3 HEX FULL G1300Z
2 off WASHER M3 G1300Z
2 off SHAKEPROOF M3 G1300Z

3 off LINK MAKE BRCS 7/2 PTFE
1AS, WHITE 512039

PCB 4-10327-2

7 off 4WAY 1" PCB PLUS 604033
(J2, J3 AND J4)

HIGH VOLTAGE LABEL
420080

SSD WARNING LABEL
420112-1

SERIAL N° LABEL
420096

TEST POINT TERMINAL
620007 8 off

NOTE THAT THIS WIRE IS PART OF
ASSY 400563.

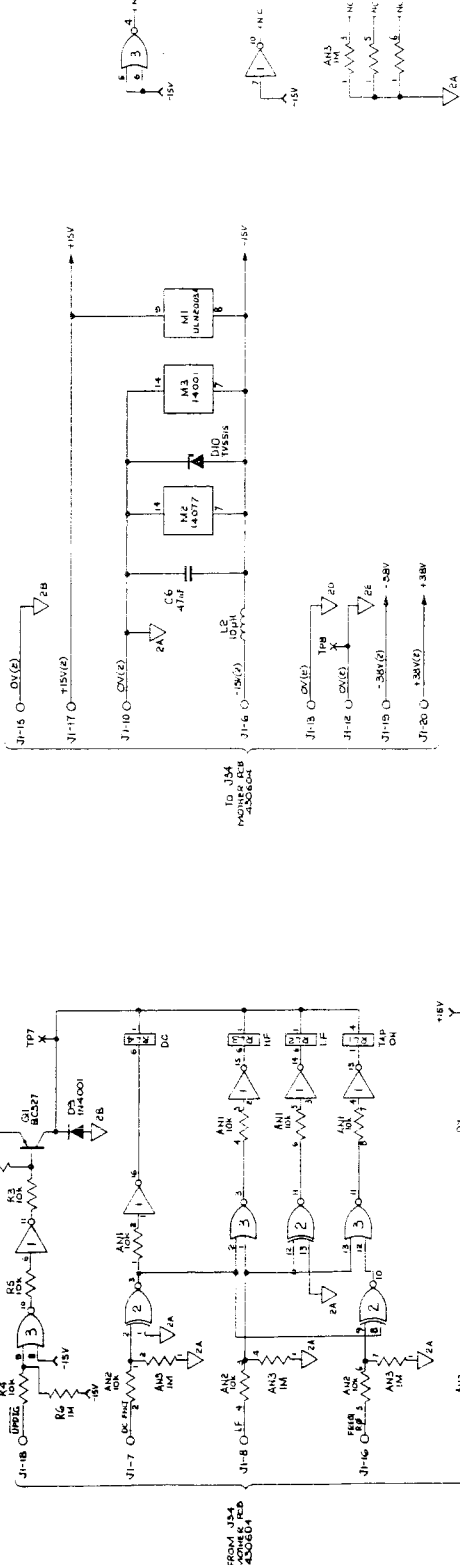
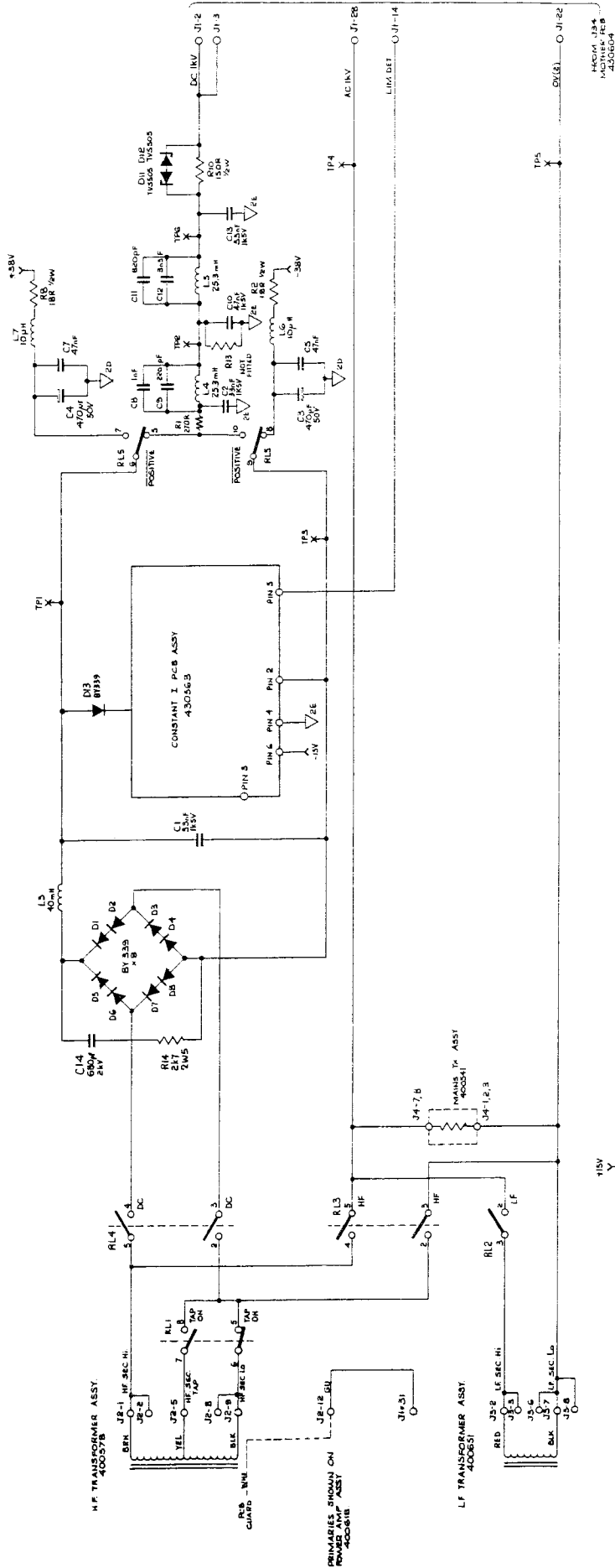
MOUNT M2/M3 ON 14 PIN DIL
SOCKET 605060 2 off

CONSTANT I SOURCE PCB ASSY
400563.

16 SWG STEARITE BEAD 630024
8 off (D10, D11, D12 + R14)

MOUNT M1 ON 16PIN DIL SOCKET
605061

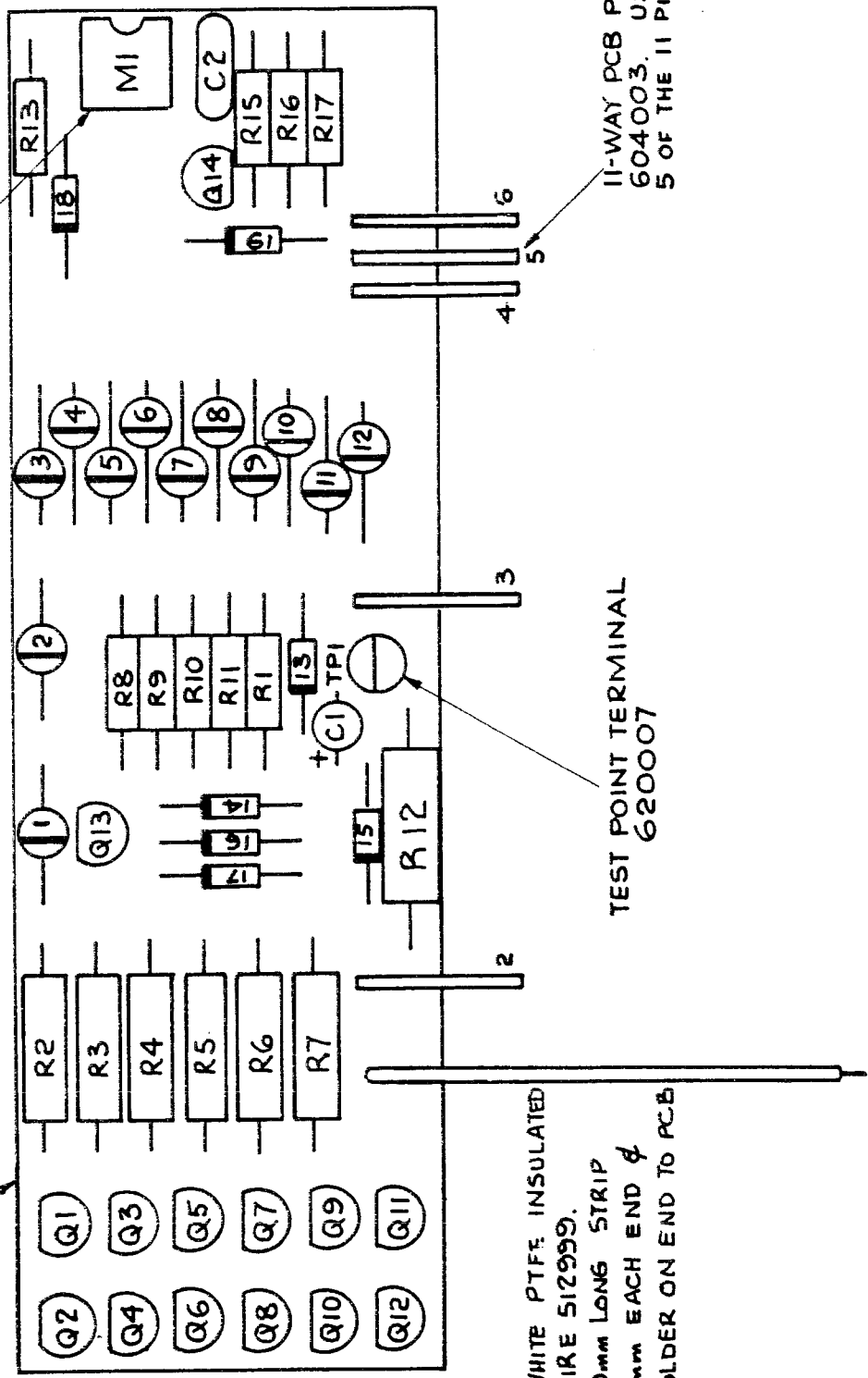
HIGH VOLTAGE ASSEMBLY
 High Voltage Switching and Logic



CONSTANT CURRENT SOURCE ASSEMBLY

MOUNT MI ON 6-WAY DIL
SOCKET 605066

PCB 410285-4

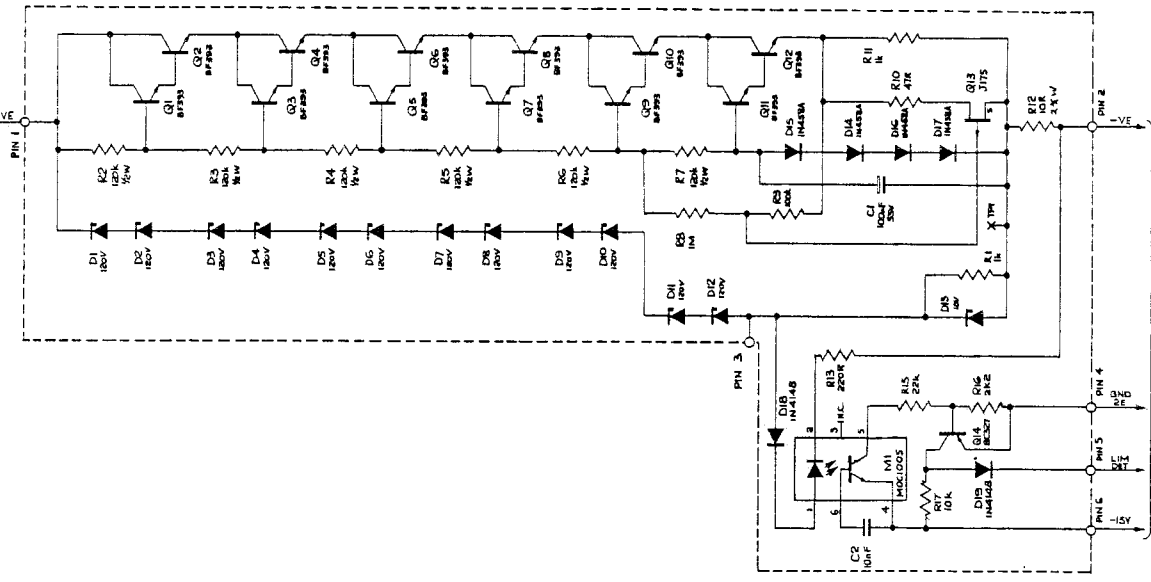


7/0.2 WHITE PTFE INSULATED
WIRE 512999.
50mm LONG STRIP
5mm EACH END ϕ
SOLDER ON END TO PCB

TEST POINT TERMINAL
620007

11-WAY PCB PLUG
604003. USE ONLY
5 OF THE 11 PINS HERE.

TO H.V. PCB ASSY
430537



CONSTANT CURRENT SOURCE ASSEMBLY
High Voltage Rectifier Bleed Chain

Circuit Diagram No. 430563-3.0 Sheet 1

For mains (line) transformer circuits refer to the following pages:

- 11.10-1 Main Digital Supply, Display Supply and Common Mode Null
- 11.11-1 Common-2 Supplies and Current Option Supply
- 11.11-2 Reference Divider Common-4 and 8V Common-2 Supplies
- 11.16-5 400V Power Supply, 38V Power Supply and Common Mode Null
- 11.17-2 Interconnections, Power Input Module and Mains Transformer Primary

CABLE TIE 590063 TO BE WRAPPED AROUND THE TRANSFORMER BODY HOLDING ALL THE WIRES AS A STRAIN RELIEF. ENSURE THIS SLEEVE IS UNDER THE CABLE TIE.

2 OFF CERAMIC BEADS G30024

RED WIRE 7/0-2 PTFE INSULATED 512222

BLUE WIRE 7/0-2 PTFE INSULATED 512666

1 OFF 4 WAY SOCKET G09091

5 OFF GOLD CLIPS G09097

RED - 1
BLACK - 2

350 mm

A A

B B

YELLOW WIRE 7/0-2 PTFE INSULATED 512444

250 mm

BLUE RED

M4 FULL NUT G15011

3.10 mm

M4 SHAKEPROOF WASHER G15021

260 mm

WHITE 7/0-2 PTFE INSULATED 512333, 210 mm

1 OFF 12 WAY SOCKET G09093

WHITE - 1
BLACK - 2
YELLOW - 3
BROWN - 6

2 OFF SLEEVES MARKED 'A' 590001

3 OFF SLEEVES MARKED 'B' 590005

4 OFF M3 X 12 mm STANDOFF G12025

2 OFF M4 PLAIN WASHER G13020

M4 X 40 mm BRASS SCREW G11055

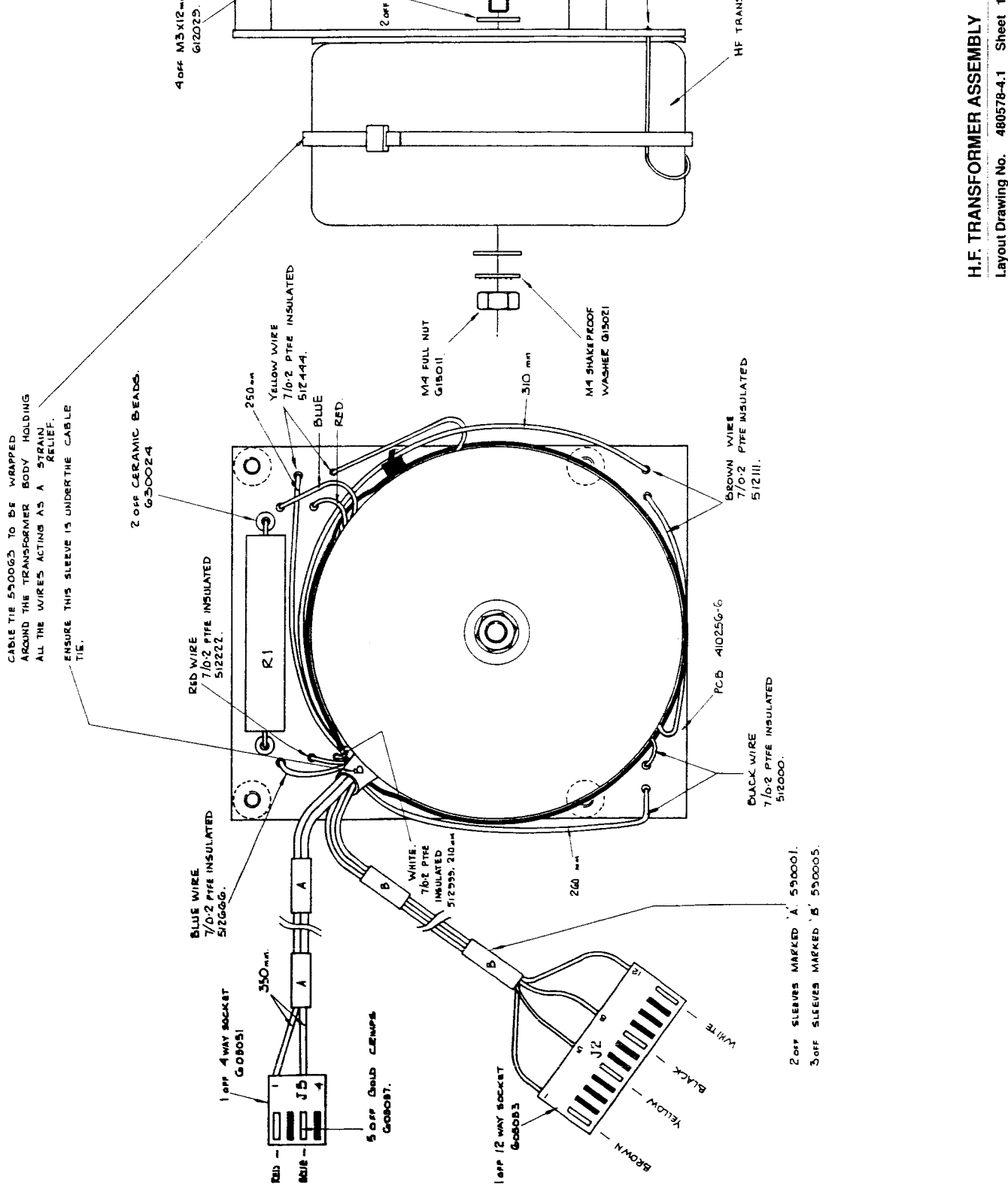
ALL WIRES ARE SOLDERED DIRECTLY TO PCB. NO SLEEVING REQUIRED.

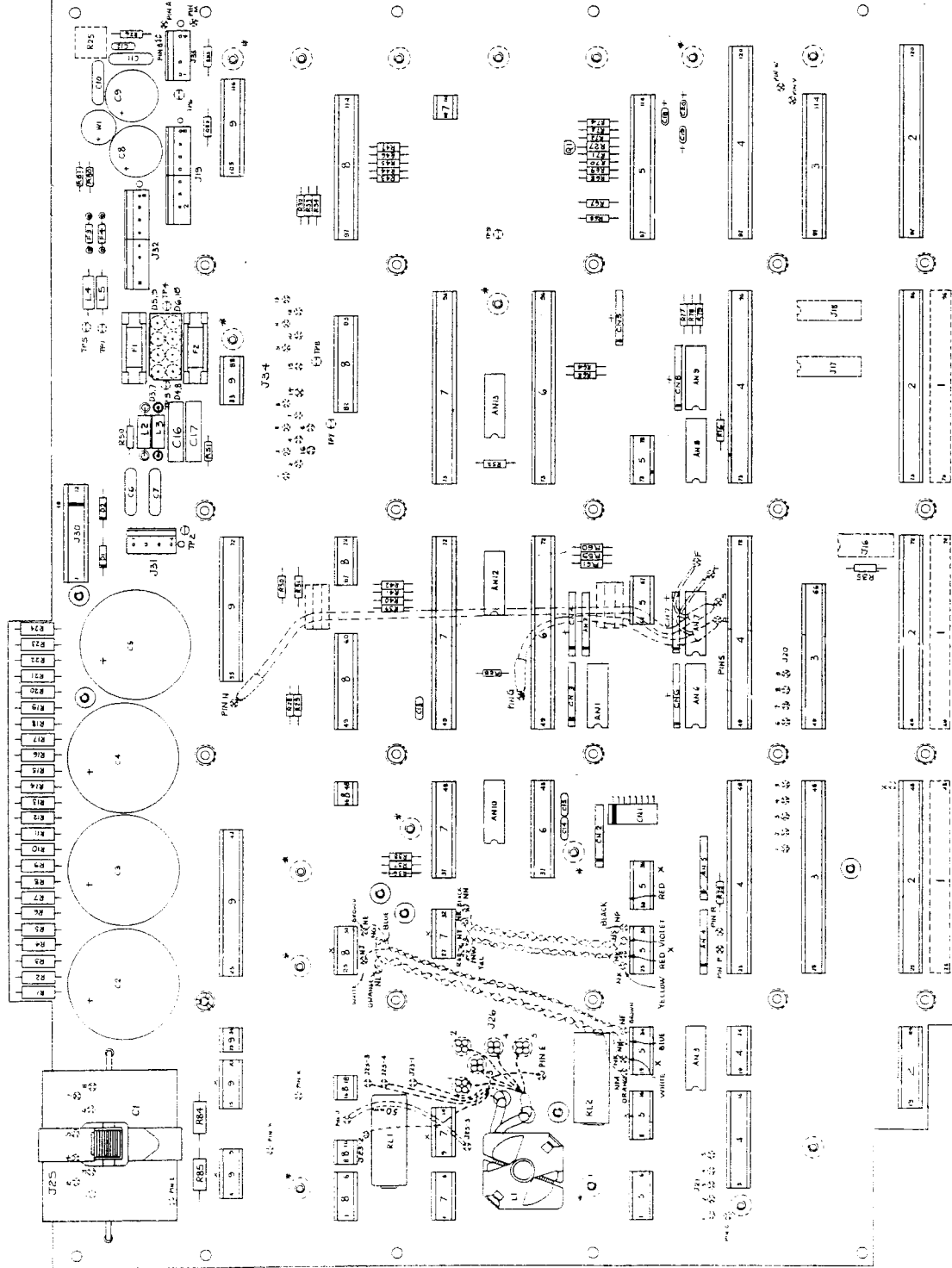
HF TRANSFORMER 300026

BROWN WIRE 7/0-2 PTFE INSULATED 512111

BLACK WIRE 7/0-2 PTFE INSULATED 512000

PCB 410256-6

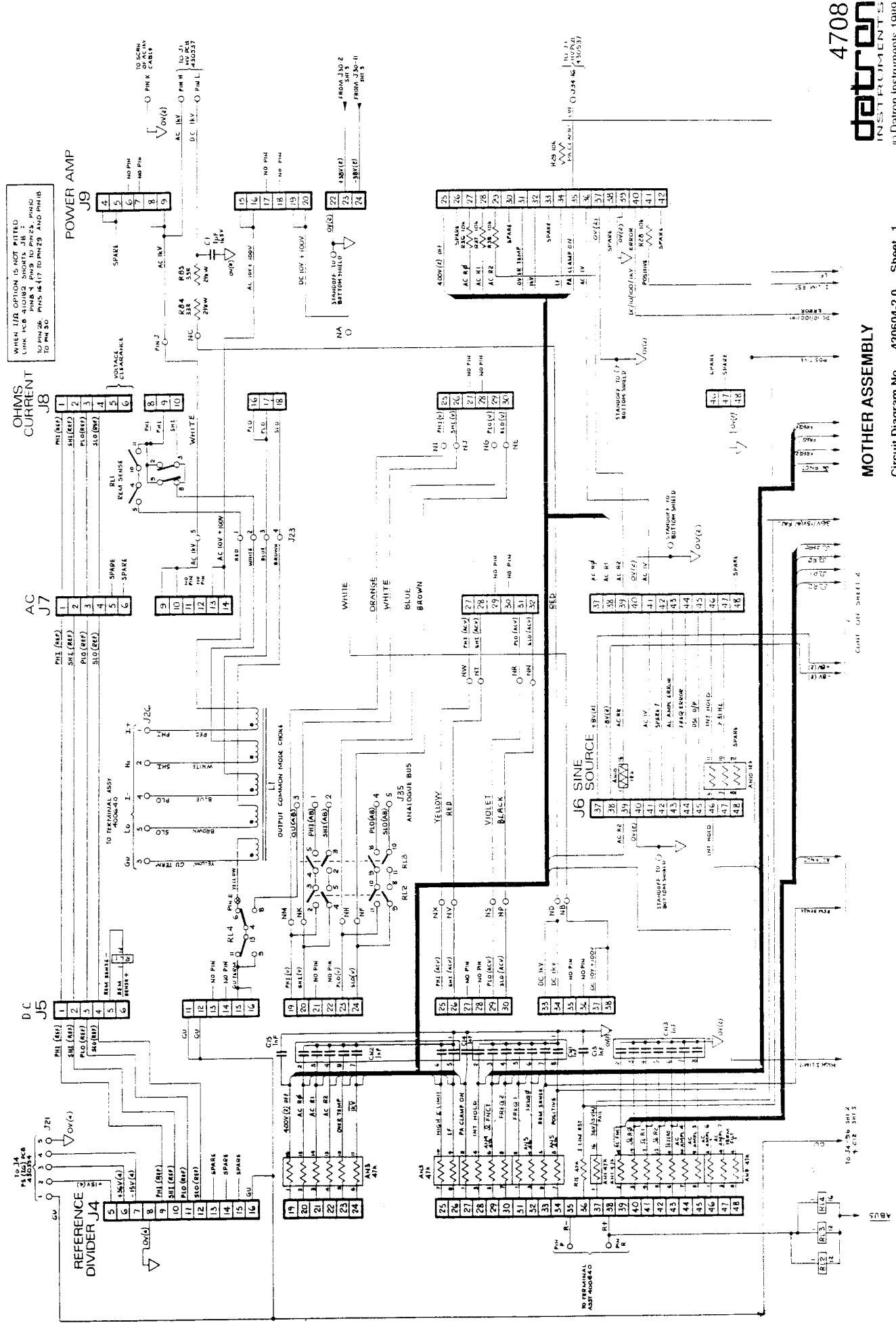




Connectors and Pin Numbers Page

| | | |
|-------------|------------------|---------|
| J1 | 25-96 | 11.16-4 |
| J2 | 13-120 | 11.16-4 |
| J3 | 25-66 | 11.16-4 |
| J4 | 5-16 | 11.16-1 |
| | 49-96 | 11.16-2 |
| | 97-120 | 11.16-4 |
| J5 | 1-6 | 11.16-1 |
| | 19-30 | 11.16-1 |
| | 62-67 | 11.16-2 |
| | 97-114 | 11.16-3 |
| J6 | 37-48 | 11.16-1 |
| | 49-96 | 11.16-2 |
| J7 | 1-6 | 11.16-1 |
| | 27-32 | 11.16-1 |
| | 49-96 | 11.16-2 |
| | 112-114 | 11.16-3 |
| J8 | 1-6 | 11.16-1 |
| | 16-18 | 11.16-1 |
| | 46-48 | 11.16-1 |
| | 49-60 | 11.16-2 |
| | 82-93 | 11.16-2 |
| | 97-114 | 11.16-3 |
| J9 | 4-9 | 11.16-1 |
| | 22-42 | 11.16-1 |
| | 55-72 | 11.16-2 |
| | 83-88 | 11.16-3 |
| J16/J17/J18 | 1-16 | 11.16-4 |
| J19 | 1-8 | 11.16-3 |
| J20 | 1-9 | 11.16-4 |
| J21/J23/J26 | 1-5 | 11.16-1 |
| J25 | 1-8 | 11.16-2 |
| J30 | 1-2 | 11.16-5 |
| | 6-7 | 11.16-5 |
| J31/33 | 1-4 | 11.16-5 |
| J32 | 1-8 | 11.16-5 |
| J34 | 1-2 | 11.16-5 |
| | 3-15 | 11.16-2 |
| | 16 | 11.16-1 |
| Pins | A; B; C; M | 11.16-5 |
| | D; E; G; N; S; T | 11.16-2 |
| | H; J; K; L; P; R | 11.16-1 |
| | V; W; X | 11.16-4 |

**MOTHER ASSEMBLY
EDGE CONNECTOR PIN INDEX**



WHEN IIA OPTION IS NOT FITTED
LINK PCB 410R2 SHORTS J8 1 OHMS
TO PIN 26 PINS 14,17,20,25 AND PIN 18
TO PIN 30

OHMS
CURRENT
J8

AC
J7

D.C.
J5

POWER AMP
J9

REFERENCE
DIVIDER
J4

J6 SINE
SOURCE

MOTHER ASSEMBLY

Circuit Diagram No. 430604-2.0 Sheet 1

4708

datron
INSTRUMENTS

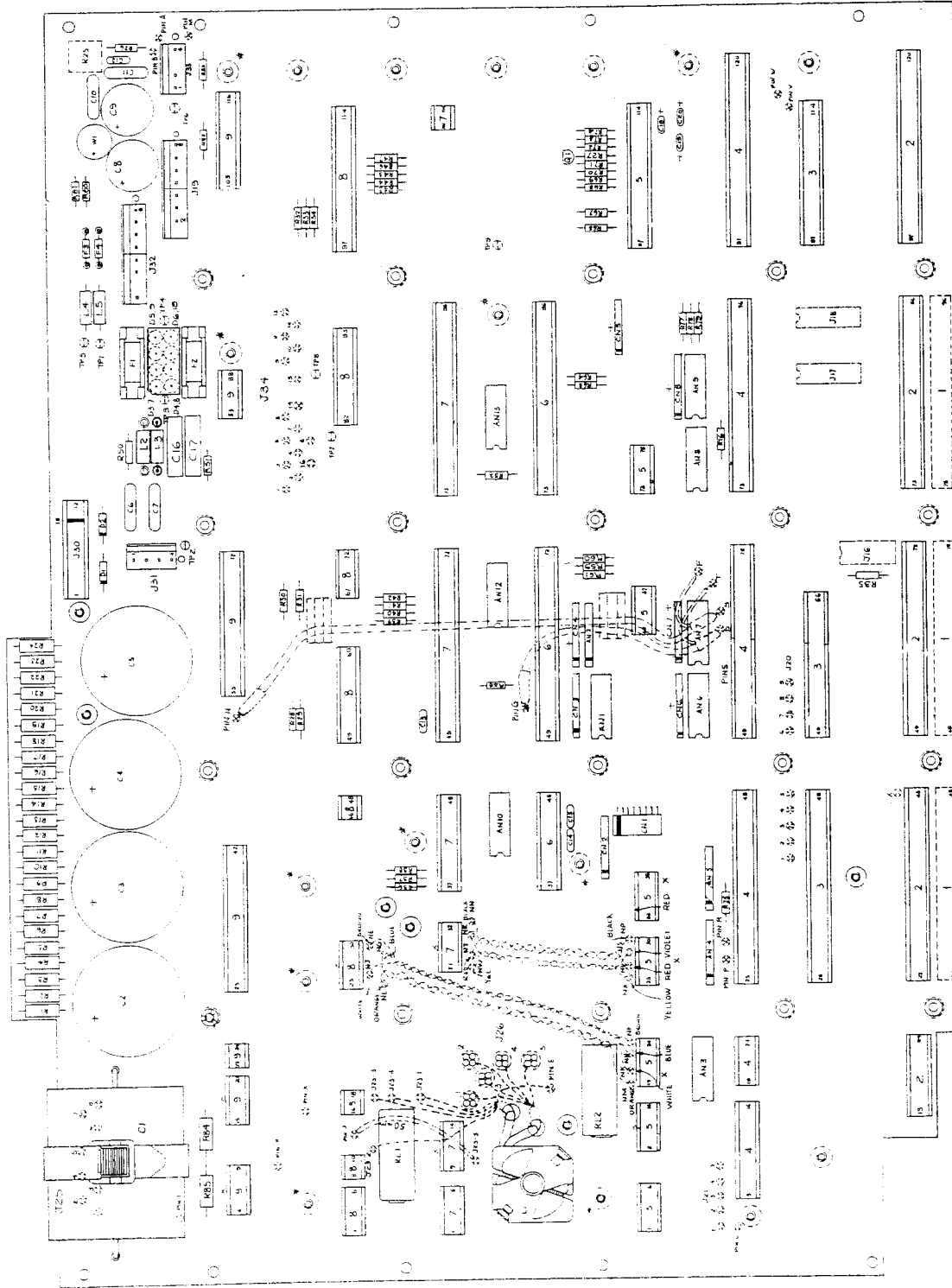
© Datron Instruments 1989

11.16-1

MOTHER ASSEMBLY

datron
INSTRUMENTS

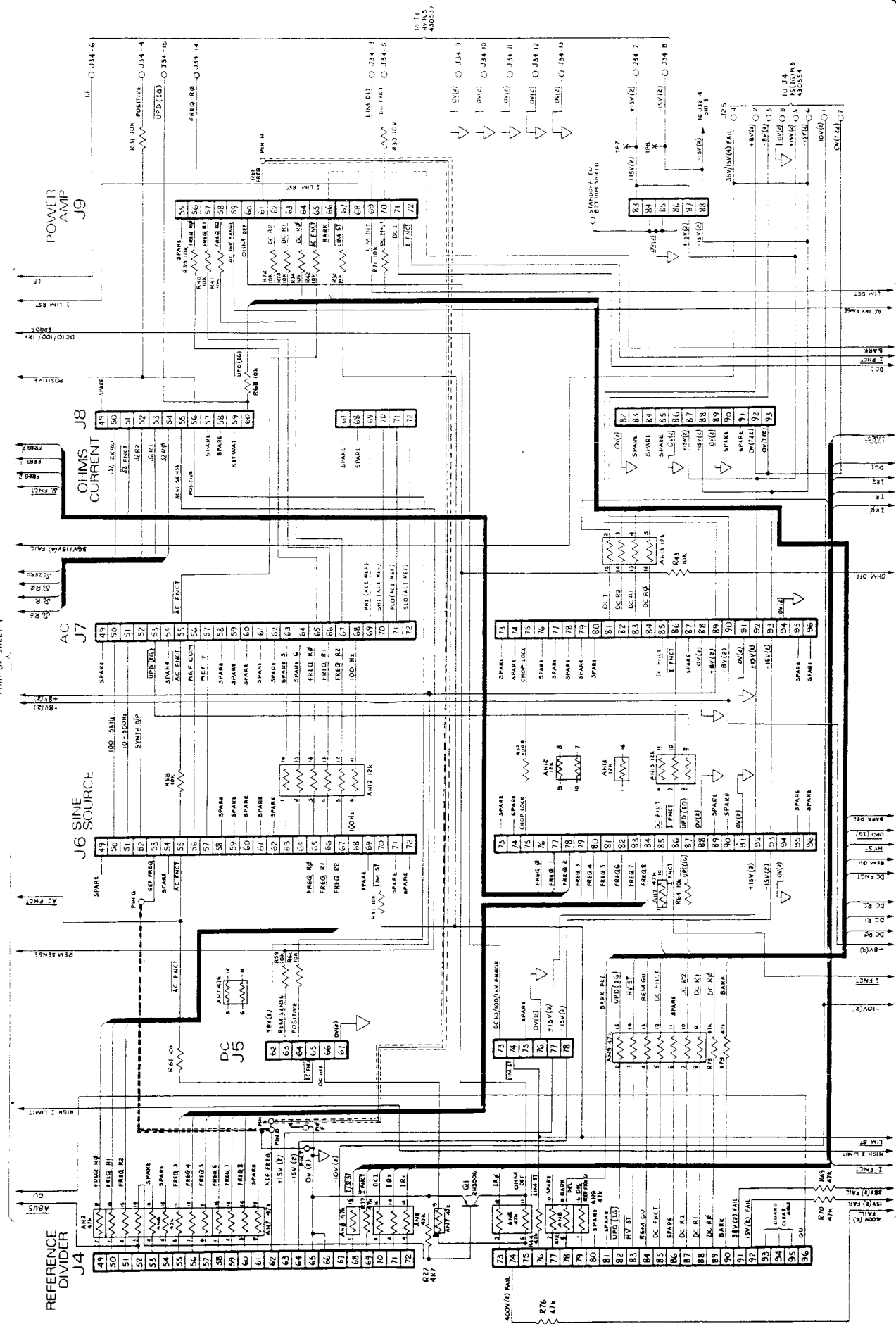
4708



Connectors and Pin Numbers Page

| | | |
|-------------|--|--|
| J1 | 25-96 | 11-16-4 |
| J2 | 13-120 | 11-16-4 |
| J3 | 25-66 | 11-16-4 |
| J4 | 5-16 49-96 97-120 | 11-16-1 11-16-2 11-16-4 |
| J5 | 1-6 19-30 62-67 97-114 | 11-16-1 11-16-1 11-16-2 11-16-3 |
| J6 | 37-48 49-96 | 11-16-1 11-16-2 |
| J7 | 1-6 27-32 49-96 112-114 | 11-16-1 11-16-1 11-16-2 11-16-3 |
| J8 | 1-6 16-18 46-48 49-60 82-93 97-114 | 11-16-1 11-16-1 11-16-1 11-16-2 11-16-2 11-16-3 |
| J9 | 4-9 22-42 55-72 105-116 | 11-16-1 11-16-1 11-16-2 11-16-3 |
| J16/J17/J18 | 1-16 | 11-16-4 |
| J19 | 1-8 | 11-16-3 |
| J20 | 1-9 | 11-16-4 |
| J21/J23/J26 | 1-5 | 11-16-1 |
| J25 | 1-8 | 11-16-2 |
| J30 | 1-2 11-12 | 11-16-5 11-16-5 |
| J31/J33 | 1-4 | 11-16-5 |
| J32 | 1-8 | 11-16-5 |
| J34 | 1-2 3-15 16 | 11-16-5 11-16-2 11-16-1 |
| Pins: | A: B; C; M D; F; G; N; S; T E; H; J; K; L; P; R V; W; X | 11-16-5 11-16-2 11-16-1 11-16-4 |

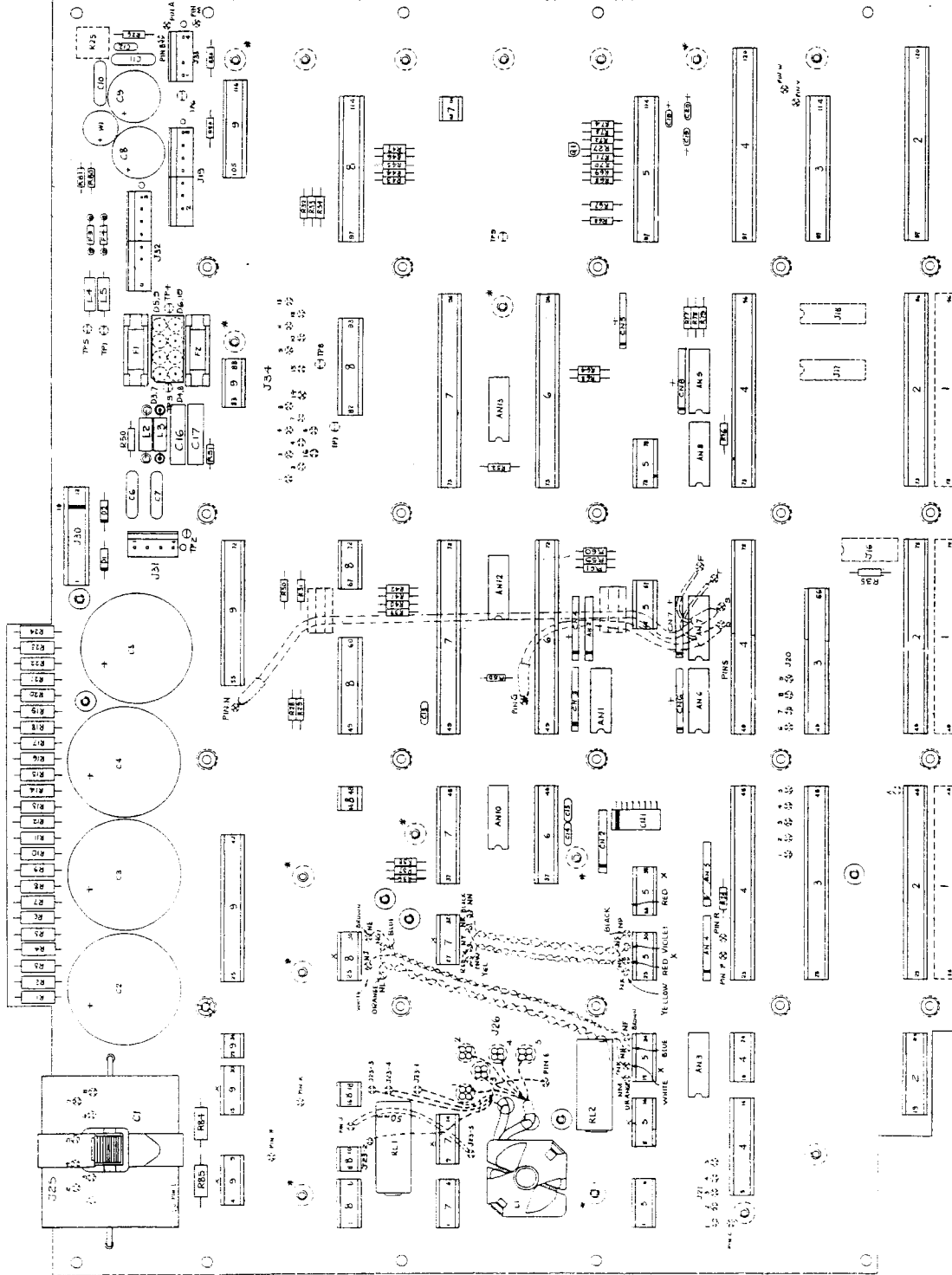
MOTHER ASSEMBLY
EDGE CONNECTOR PIN INDEX



CONT ON SHEET 1

CONT ON SHEET 3

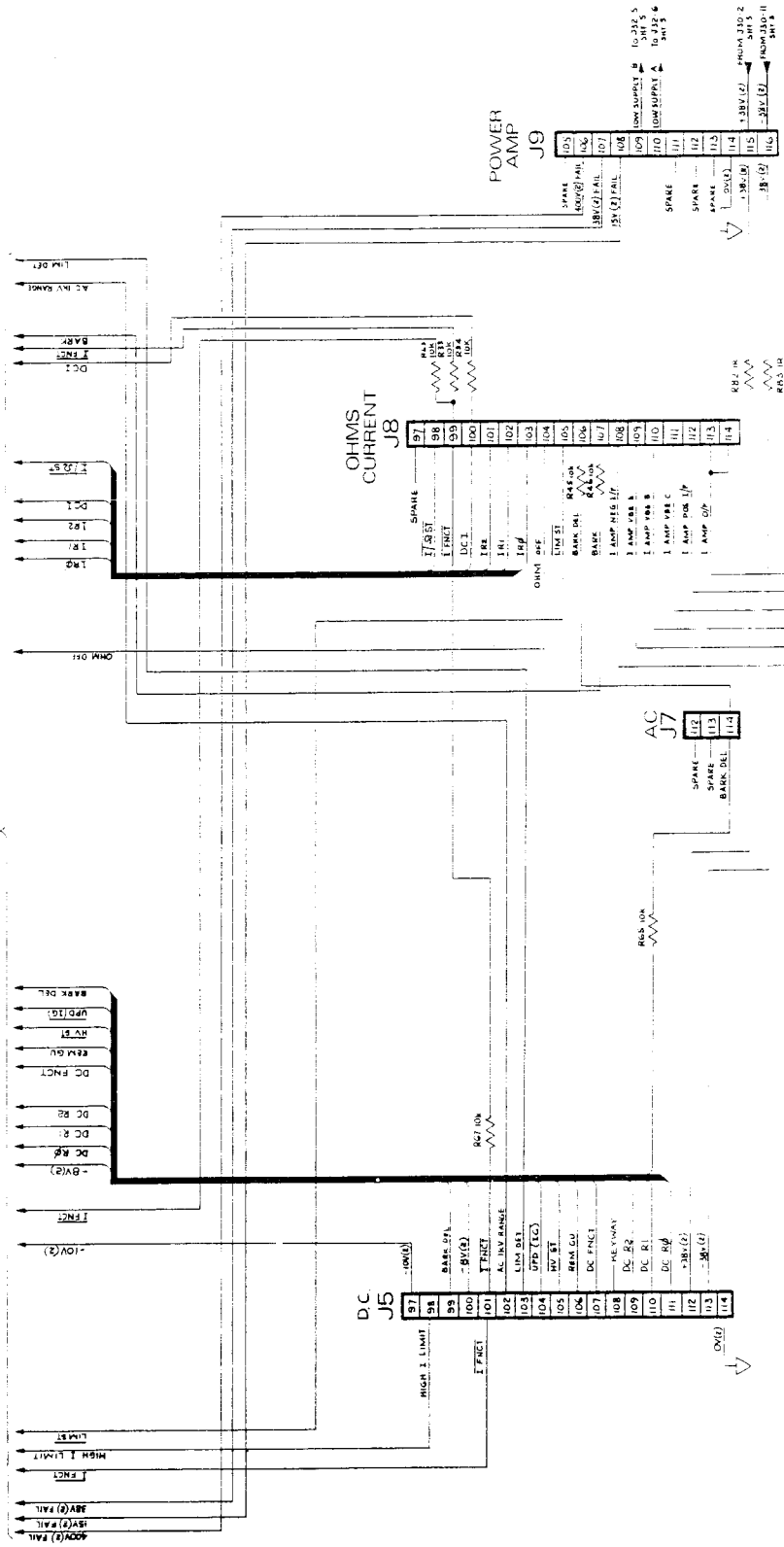
MOTHER ASSEMBLY



| Connectors and Pin Numbers | Page |
|----------------------------|--|
| J1 | 25-96 |
| J2 | 13-120 |
| J3 | 25-66 97-114 |
| J4 | 5-16 19-48 |
| J5 | 11-16 19-30 33-38 62-67 73-78 97-120 |
| J6 | 37-48 49-96 |
| J7 | 1-6 9-14 27-32 37-48 49-96 112-114 |
| J8 | 1-6 8-10 16-18 25-30 46-48 49-60 67-72 82-93 97-114 |
| J9 | 4-9 15-20 22-42 55-72 83-88 105-116 |
| J16/J17/J18 | 1-16 |
| J19 | 1-8 |
| J20 | 1-9 |
| J21/J23/J26 | 1-5 |
| J25 | 1-8 |
| J30 | 1-2 6-7 |
| J31/J33 | 1-4 |
| J32 | 1-8 |
| J34 | 1-2 3-15 16 |
| Pins: | A: B; C; M 11-16-5 D; F; G; N; S; T 11-16-2 E; H; J; K; L; P; R 11-16-1 V; W; X 11-16-4 |

**MOTHER ASSEMBLY
EDGE CONNECTOR PIN INDEX**

Cont on Sheet 2



CHS, CH2, CH3, CH4, CH5, CH6, CH7, CH8, CH9, CH10, CH11, CH12, CH13, CH14, CH15, CH16, CH17, CH18, CH19, CH20, CH21, CH22, CH23, CH24, CH25, CH26, CH27, CH28, CH29, CH30, CH31, CH32, CH33, CH34, CH35, CH36, CH37, CH38, CH39, CH40, CH41, CH42, CH43, CH44, CH45, CH46, CH47, CH48, CH49, CH50, CH51, CH52, CH53, CH54, CH55, CH56, CH57, CH58, CH59, CH60, CH61, CH62, CH63, CH64, CH65, CH66, CH67, CH68, CH69, CH70, CH71, CH72, CH73, CH74, CH75, CH76, CH77, CH78, CH79, CH80, CH81, CH82, CH83, CH84, CH85, CH86, CH87, CH88, CH89, CH90, CH91, CH92, CH93, CH94, CH95, CH96, CH97, CH98, CH99, CH100, CH101, CH102, CH103, CH104, CH105, CH106, CH107, CH108, CH109, CH110, CH111, CH112, CH113, CH114, CH115, CH116, CH117, CH118, CH119, CH120, CH121, CH122, CH123, CH124, CH125, CH126, CH127, CH128, CH129, CH130, CH131, CH132, CH133, CH134, CH135, CH136, CH137, CH138, CH139, CH140, CH141, CH142, CH143, CH144, CH145, CH146, CH147, CH148, CH149, CH150, CH151, CH152, CH153, CH154, CH155, CH156, CH157, CH158, CH159, CH160, CH161, CH162, CH163, CH164, CH165, CH166, CH167, CH168, CH169, CH170, CH171, CH172, CH173, CH174, CH175, CH176, CH177, CH178, CH179, CH180, CH181, CH182, CH183, CH184, CH185, CH186, CH187, CH188, CH189, CH190, CH191, CH192, CH193, CH194, CH195, CH196, CH197, CH198, CH199, CH200, CH201, CH202, CH203, CH204, CH205, CH206, CH207, CH208, CH209, CH210, CH211, CH212, CH213, CH214, CH215, CH216, CH217, CH218, CH219, CH220, CH221, CH222, CH223, CH224, CH225, CH226, CH227, CH228, CH229, CH230, CH231, CH232, CH233, CH234, CH235, CH236, CH237, CH238, CH239, CH240, CH241, CH242, CH243, CH244, CH245, CH246, CH247, CH248, CH249, CH250, CH251, CH252, CH253, CH254, CH255, CH256, CH257, CH258, CH259, CH260, CH261, CH262, CH263, CH264, CH265, CH266, CH267, CH268, CH269, CH270, CH271, CH272, CH273, CH274, CH275, CH276, CH277, CH278, CH279, CH280, CH281, CH282, CH283, CH284, CH285, CH286, CH287, CH288, CH289, CH290, CH291, CH292, CH293, CH294, CH295, CH296, CH297, CH298, CH299, CH300, CH301, CH302, CH303, CH304, CH305, CH306, CH307, CH308, CH309, CH310, CH311, CH312, CH313, CH314, CH315, CH316, CH317, CH318, CH319, CH320, CH321, CH322, CH323, CH324, CH325, CH326, CH327, CH328, CH329, CH330, CH331, CH332, CH333, CH334, CH335, CH336, CH337, CH338, CH339, CH340, CH341, CH342, CH343, CH344, CH345, CH346, CH347, CH348, CH349, CH350, CH351, CH352, CH353, CH354, CH355, CH356, CH357, CH358, CH359, CH360, CH361, CH362, CH363, CH364, CH365, CH366, CH367, CH368, CH369, CH370, CH371, CH372, CH373, CH374, CH375, CH376, CH377, CH378, CH379, CH380, CH381, CH382, CH383, CH384, CH385, CH386, CH387, CH388, CH389, CH390, CH391, CH392, CH393, CH394, CH395, CH396, CH397, CH398, CH399, CH400, CH401, CH402, CH403, CH404, CH405, CH406, CH407, CH408, CH409, CH410, CH411, CH412, CH413, CH414, CH415, CH416, CH417, CH418, CH419, CH420, CH421, CH422, CH423, CH424, CH425, CH426, CH427, CH428, CH429, CH430, CH431, CH432, CH433, CH434, CH435, CH436, CH437, CH438, CH439, CH440, CH441, CH442, CH443, CH444, CH445, CH446, CH447, CH448, CH449, CH450, CH451, CH452, CH453, CH454, CH455, CH456, CH457, CH458, CH459, CH460, CH461, CH462, CH463, CH464, CH465, CH466, CH467, CH468, CH469, CH470, CH471, CH472, CH473, CH474, CH475, CH476, CH477, CH478, CH479, CH480, CH481, CH482, CH483, CH484, CH485, CH486, CH487, CH488, CH489, CH490, CH491, CH492, CH493, CH494, CH495, CH496, CH497, CH498, CH499, CH500, CH501, CH502, CH503, CH504, CH505, CH506, CH507, CH508, CH509, CH510, CH511, CH512, CH513, CH514, CH515, CH516, CH517, CH518, CH519, CH520, CH521, CH522, CH523, CH524, CH525, CH526, CH527, CH528, CH529, CH530, CH531, CH532, CH533, CH534, CH535, CH536, CH537, CH538, CH539, CH540, CH541, CH542, CH543, CH544, CH545, CH546, CH547, CH548, CH549, CH550, CH551, CH552, CH553, CH554, CH555, CH556, CH557, CH558, CH559, CH560, CH561, CH562, CH563, CH564, CH565, CH566, CH567, CH568, CH569, CH570, CH571, CH572, CH573, CH574, CH575, CH576, CH577, CH578, CH579, CH580, CH581, CH582, CH583, CH584, CH585, CH586, CH587, CH588, CH589, CH590, CH591, CH592, CH593, CH594, CH595, CH596, CH597, CH598, CH599, CH600, CH601, CH602, CH603, CH604, CH605, CH606, CH607, CH608, CH609, CH610, CH611, CH612, CH613, CH614, CH615, CH616, CH617, CH618, CH619, CH620, CH621, CH622, CH623, CH624, CH625, CH626, CH627, CH628, CH629, CH630, CH631, CH632, CH633, CH634, CH635, CH636, CH637, CH638, CH639, CH640, CH641, CH642, CH643, CH644, CH645, CH646, CH647, CH648, CH649, CH650, CH651, CH652, CH653, CH654, CH655, CH656, CH657, CH658, CH659, CH660, CH661, CH662, CH663, CH664, CH665, CH666, CH667, CH668, CH669, CH670, CH671, CH672, CH673, CH674, CH675, CH676, CH677, CH678, CH679, CH680, CH681, CH682, CH683, CH684, CH685, CH686, CH687, CH688, CH689, CH690, CH691, CH692, CH693, CH694, CH695, CH696, CH697, CH698, CH699, CH700, CH701, CH702, CH703, CH704, CH705, CH706, CH707, CH708, CH709, CH710, CH711, CH712, CH713, CH714, CH715, CH716, CH717, CH718, CH719, CH720, CH721, CH722, CH723, CH724, CH725, CH726, CH727, CH728, CH729, CH730, CH731, CH732, CH733, CH734, CH735, CH736, CH737, CH738, CH739, CH740, CH741, CH742, CH743, CH744, CH745, CH746, CH747, CH748, CH749, CH750, CH751, CH752, CH753, CH754, CH755, CH756, CH757, CH758, CH759, CH760, CH761, CH762, CH763, CH764, CH765, CH766, CH767, CH768, CH769, CH770, CH771, CH772, CH773, CH774, CH775, CH776, CH777, CH778, CH779, CH780, CH781, CH782, CH783, CH784, CH785, CH786, CH787, CH788, CH789, CH790, CH791, CH792, CH793, CH794, CH795, CH796, CH797, CH798, CH799, CH800, CH801, CH802, CH803, CH804, CH805, CH806, CH807, CH808, CH809, CH810, CH811, CH812, CH813, CH814, CH815, CH816, CH817, CH818, CH819, CH820, CH821, CH822, CH823, CH824, CH825, CH826, CH827, CH828, CH829, CH830, CH831, CH832, CH833, CH834, CH835, CH836, CH837, CH838, CH839, CH840, CH841, CH842, CH843, CH844, CH845, CH846, CH847, CH848, CH849, CH850, CH851, CH852, CH853, CH854, CH855, CH856, CH857, CH858, CH859, CH860, CH861, CH862, CH863, CH864, CH865, CH866, CH867, CH868, CH869, CH870, CH871, CH872, CH873, CH874, CH875, CH876, CH877, CH878, CH879, CH880, CH881, CH882, CH883, CH884, CH885, CH886, CH887, CH888, CH889, CH890, CH891, CH892, CH893, CH894, CH895, CH896, CH897, CH898, CH899, CH900, CH901, CH902, CH903, CH904, CH905, CH906, CH907, CH908, CH909, CH910, CH911, CH912, CH913, CH914, CH915, CH916, CH917, CH918, CH919, CH920, CH921, CH922, CH923, CH924, CH925, CH926, CH927, CH928, CH929, CH930, CH931, CH932, CH933, CH934, CH935, CH936, CH937, CH938, CH939, CH940, CH941, CH942, CH943, CH944, CH945, CH946, CH947, CH948, CH949, CH950, CH951, CH952, CH953, CH954, CH955, CH956, CH957, CH958, CH959, CH960, CH961, CH962, CH963, CH964, CH965, CH966, CH967, CH968, CH969, CH970, CH971, CH972, CH973, CH974, CH975, CH976, CH977, CH978, CH979, CH980, CH981, CH982, CH983, CH984, CH985, CH986, CH987, CH988, CH989, CH990, CH991, CH992, CH993, CH994, CH995, CH996, CH997, CH998, CH999, CH1000.

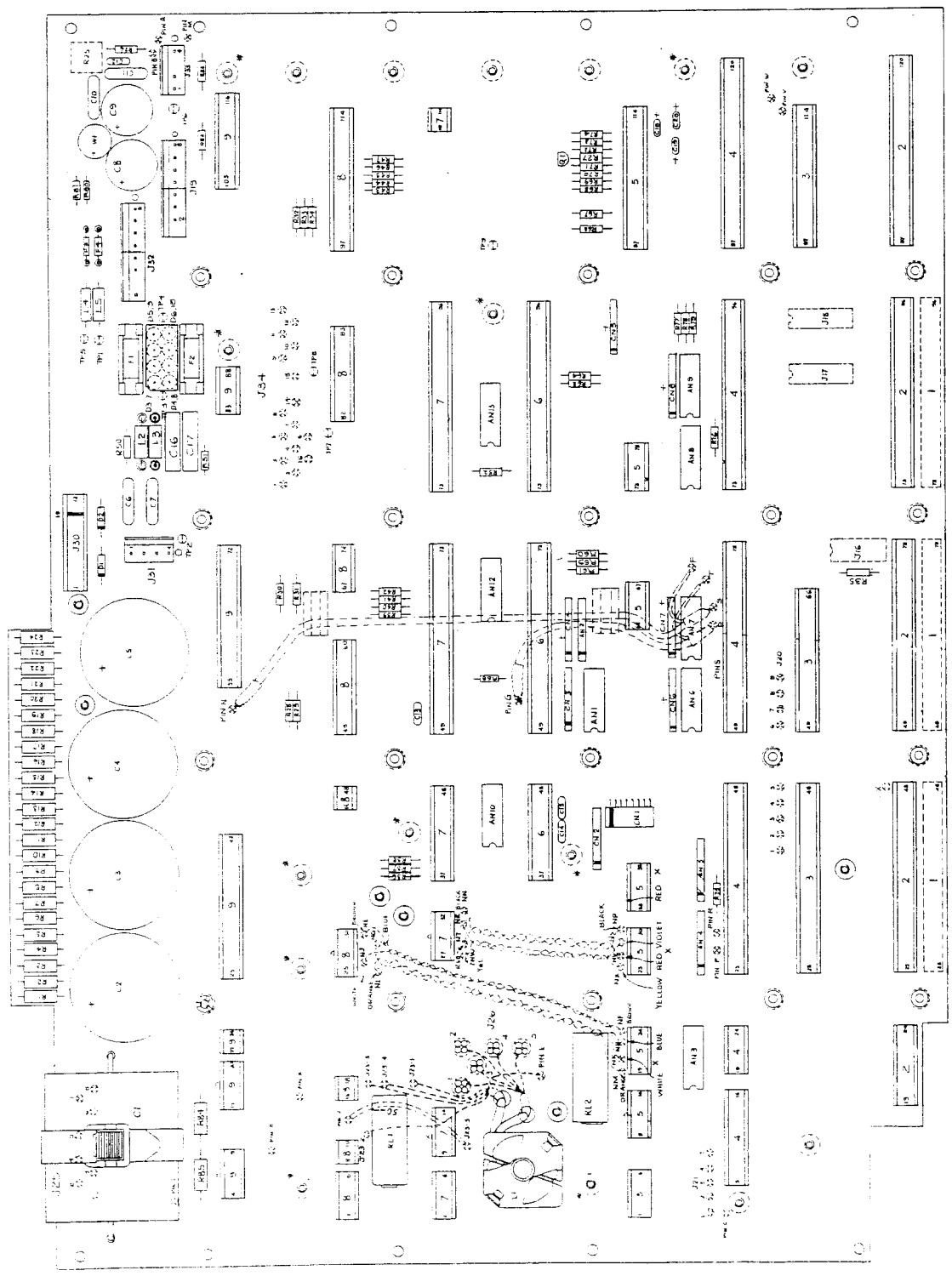
| CH4 | CH5 | CH6 | CH7 | CH8 |
|-----|---------------|--------|--------|--------|
| 1 | COMMON | COMMON | COMMON | COMMON |
| 2 | AN2-2 | AN2-15 | AN7-16 | AN8-5 |
| 3 | AN2-2 | AN2-15 | AN7-15 | AN8-15 |
| 4 | N.C. | AN8-14 | AN7-14 | AN8-14 |
| 5 | AN2-4 | AN8-13 | AN7-13 | AN8-13 |
| 6 | AN2-4 | AN8-12 | AN6-12 | AN8-12 |
| 7 | N.C. | AN8-11 | AN7-11 | AN8-11 |
| 8 | AN2-5 (50-50) | N.C. | AN6-10 | AN8-10 |
| 9 | N.C. | AN8-16 | AN5-16 | AN8-16 |

C18 - R77
C19 - R76
C20 - R75

MOTHER ASSEMBLY

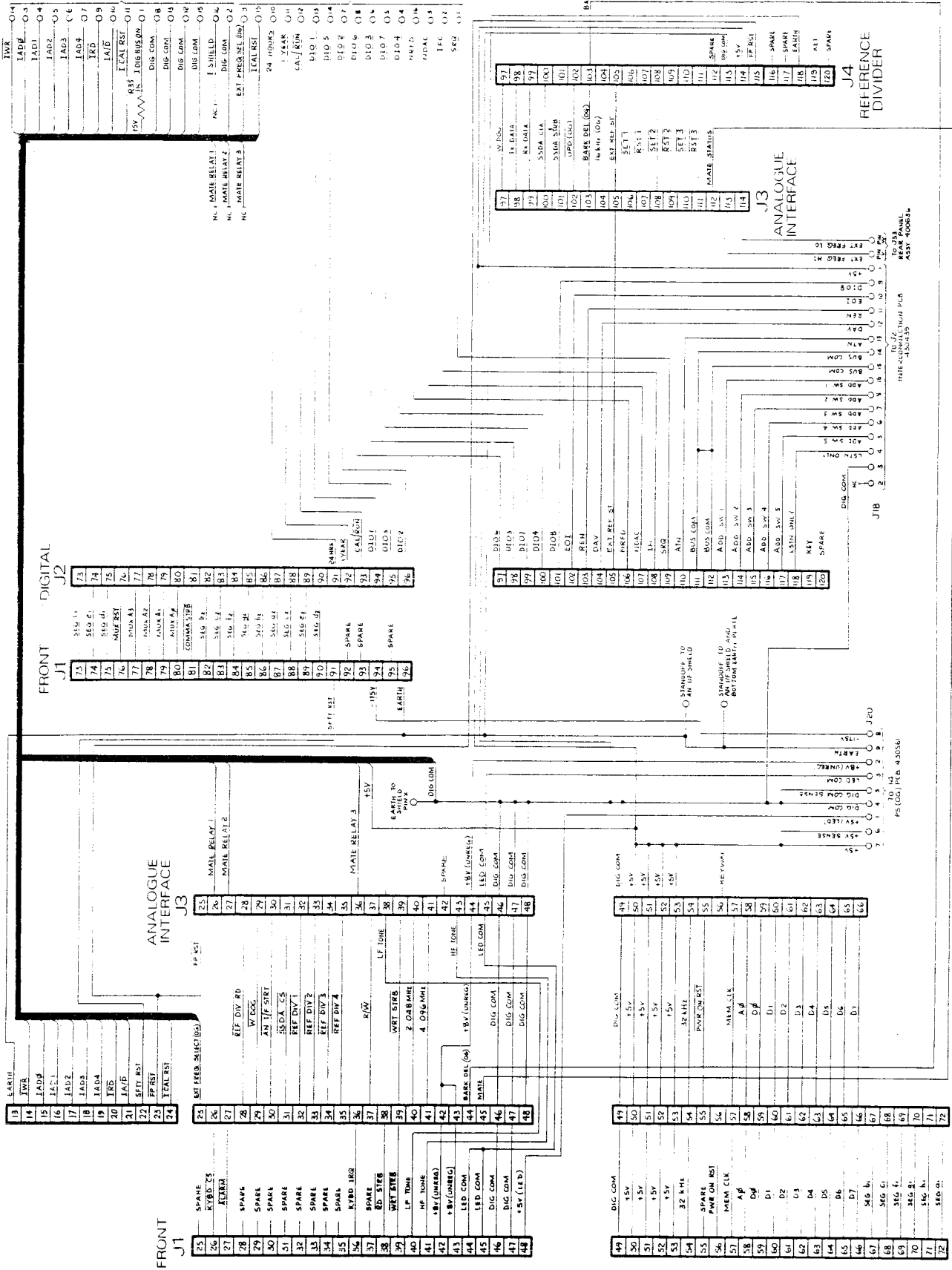
Circuit Diagram No. 430604-2.0 Sheet 3

MOTHER ASSEMBLY

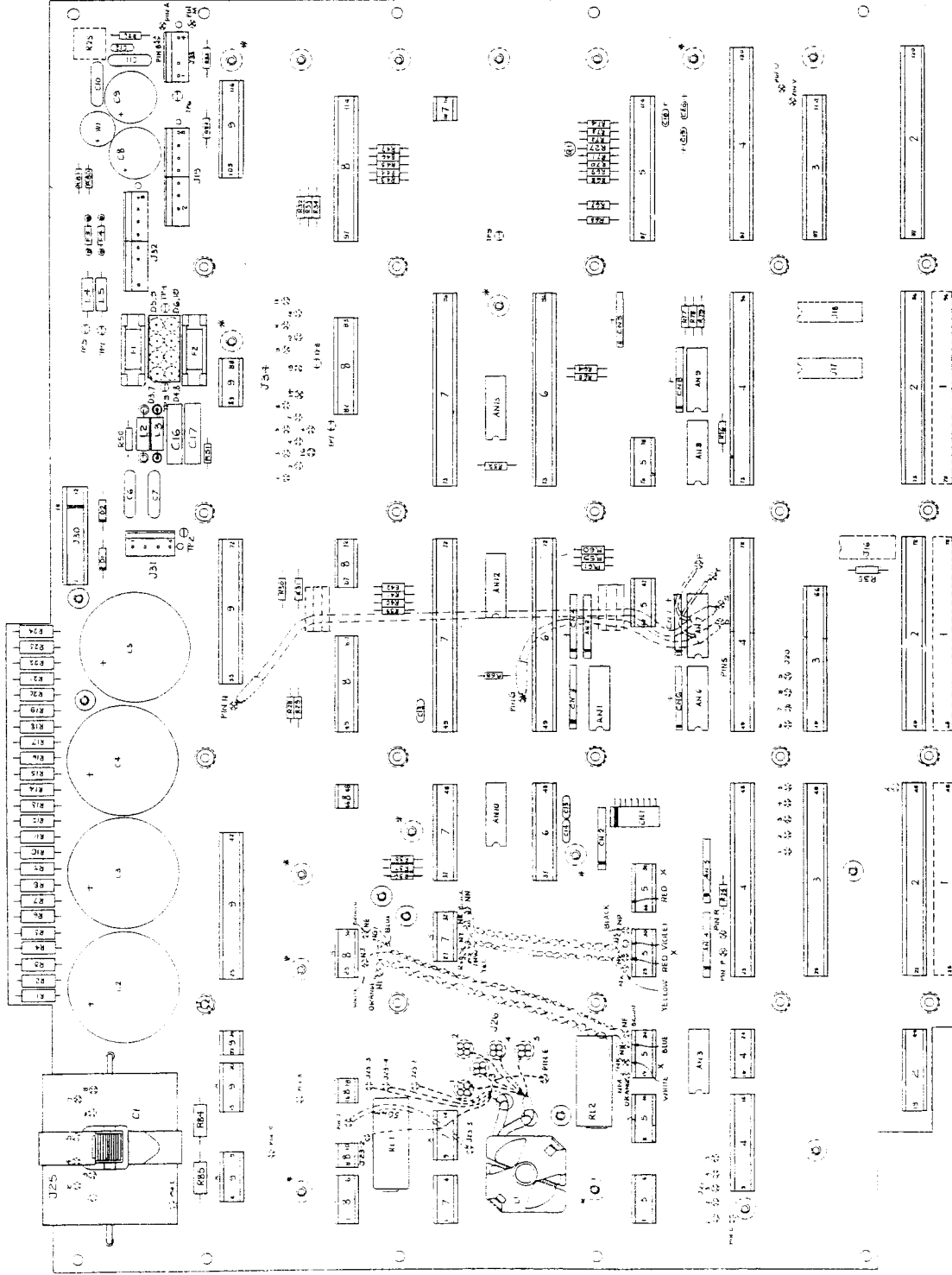


| Connectors and Pin Numbers | Page |
|----------------------------|--|
| J1 | 25-96 |
| J2 | 13-120 |
| J3 | 25-66 |
| J4 | 5-16 49-96 97-120 |
| J5 | 1-6 19-30 62-67 97-114 |
| J6 | 37-48 49-96 |
| J7 | 1-6 27-32 49-96 112-114 |
| J8 | 1-6 16-18 46-48 49-60 82-93 97-114 |
| J9 | 4-9 22-42 55-72 105-116 |
| J16/J17/J18 | 1-16 |
| J19 | 1-8 |
| J20 | 1-9 |
| J21/J23/J26 | 1-5 |
| J25 | 1-8 |
| J30 | 1-2 11-12 |
| J31/J33 | 1-4 |
| J32 | 1-8 |
| J34 | 1-2 3-15 16 |
| Plugs | A; B; C; M D; F; G; N; S; T E; H; J; K; L; P; R V; W; X |

**MOTHER ASSEMBLY
EDGE CONNECTOR PIN INDEX**

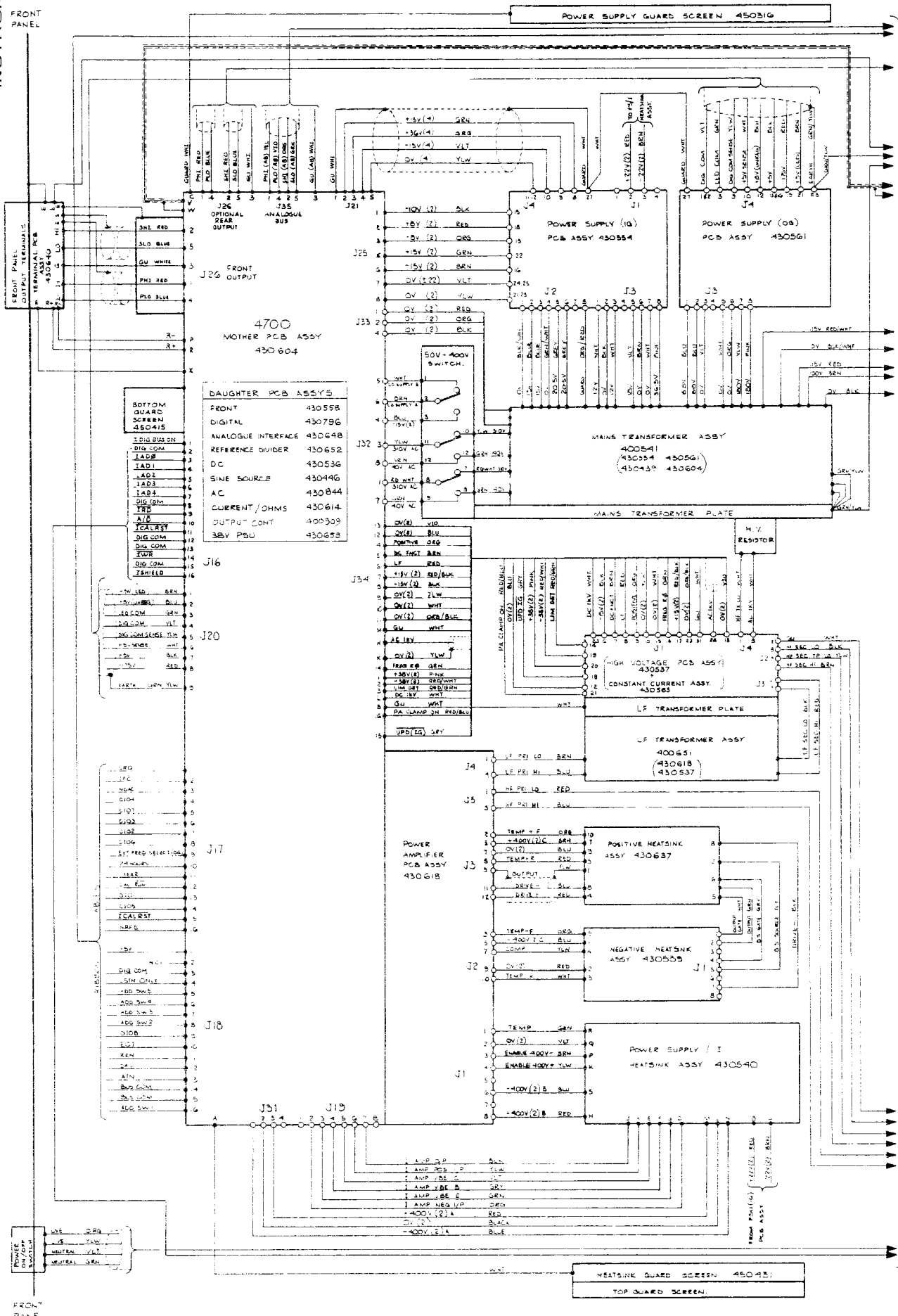


MOTHER ASSEMBLY



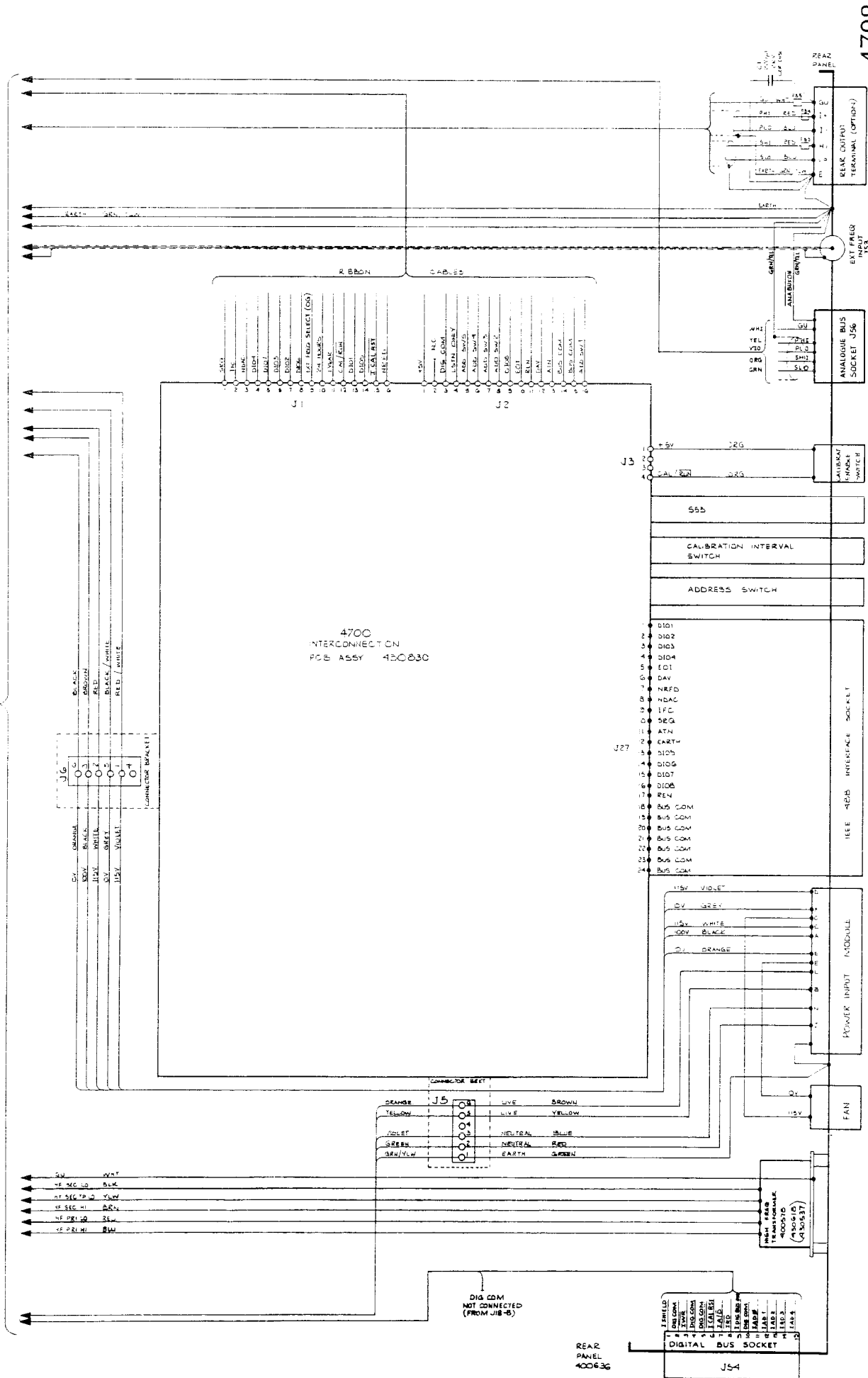
| Connectors and Pin Numbers | Page |
|----------------------------|---------------------|
| J1 | 25-96 |
| J2 | 13-120 |
| J3 | 25-66 |
| J4 | 5-16 |
| J5 | 11-16 |
| J6 | 37-48 |
| J7 | 1-6 |
| J8 | 1-6 |
| J9 | 4-9 |
| J16/J17/J18 | 1-16 |
| J19 | 1-8 |
| J20 | 1-9 |
| J21/J23/J26 | 1-5 |
| J25 | 1-8 |
| J30 | 1-2 |
| J31/J33 | 1-4 |
| J32 | 1-8 |
| J34 | 1-2 |
| Plns: | A: B; C; M |
| | D; F; G; N; S; T |
| | E; H; J; K; L; P; R |
| | V; W; X |

MOTHER ASSEMBLY
EDGE CONNECTOR PIN INDEX

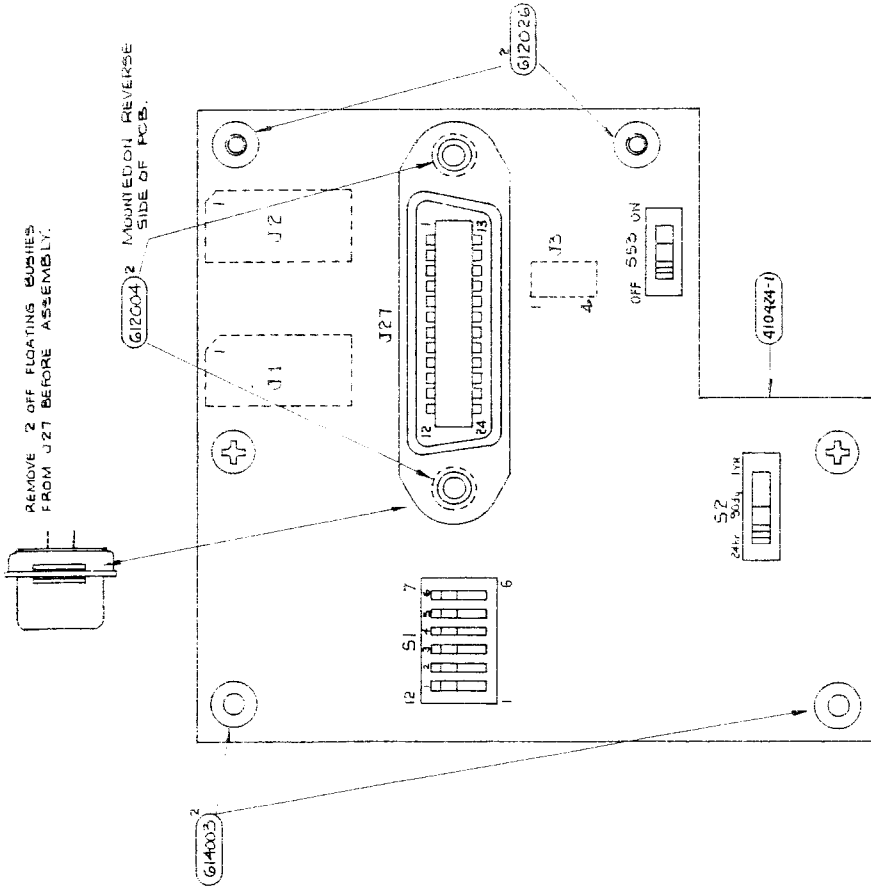
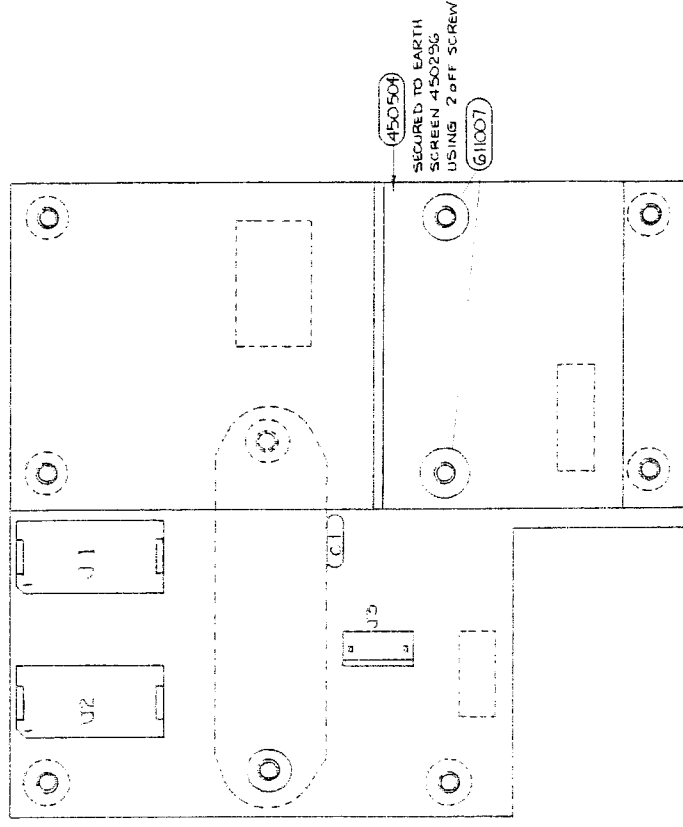
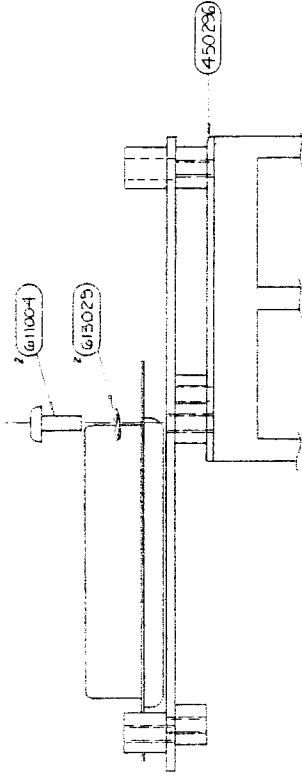


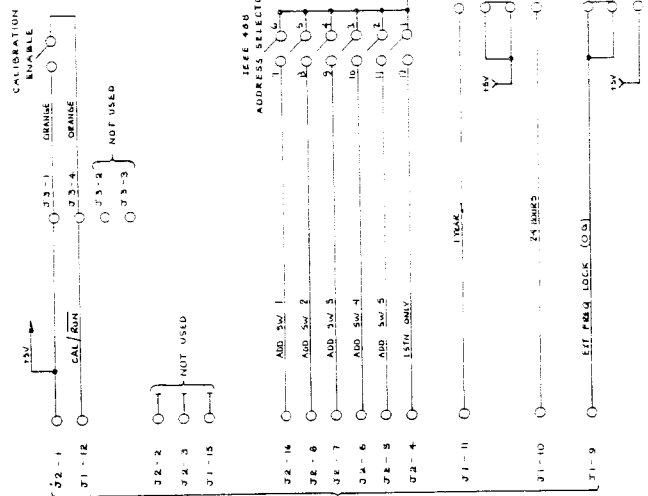
CONTINUED ON SHEET 2

CONTINUED ON SHEET 1

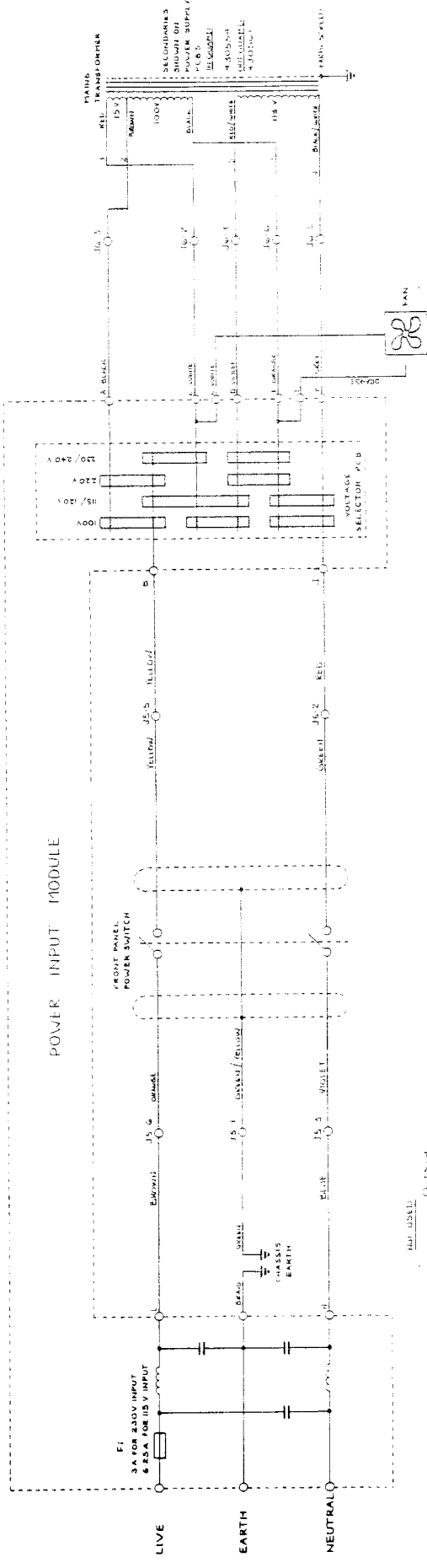


INTERCONNECTION ASSEMBLY





POWER INPUT MODULE



REV. 02812

Q J3-4

Q J3-5

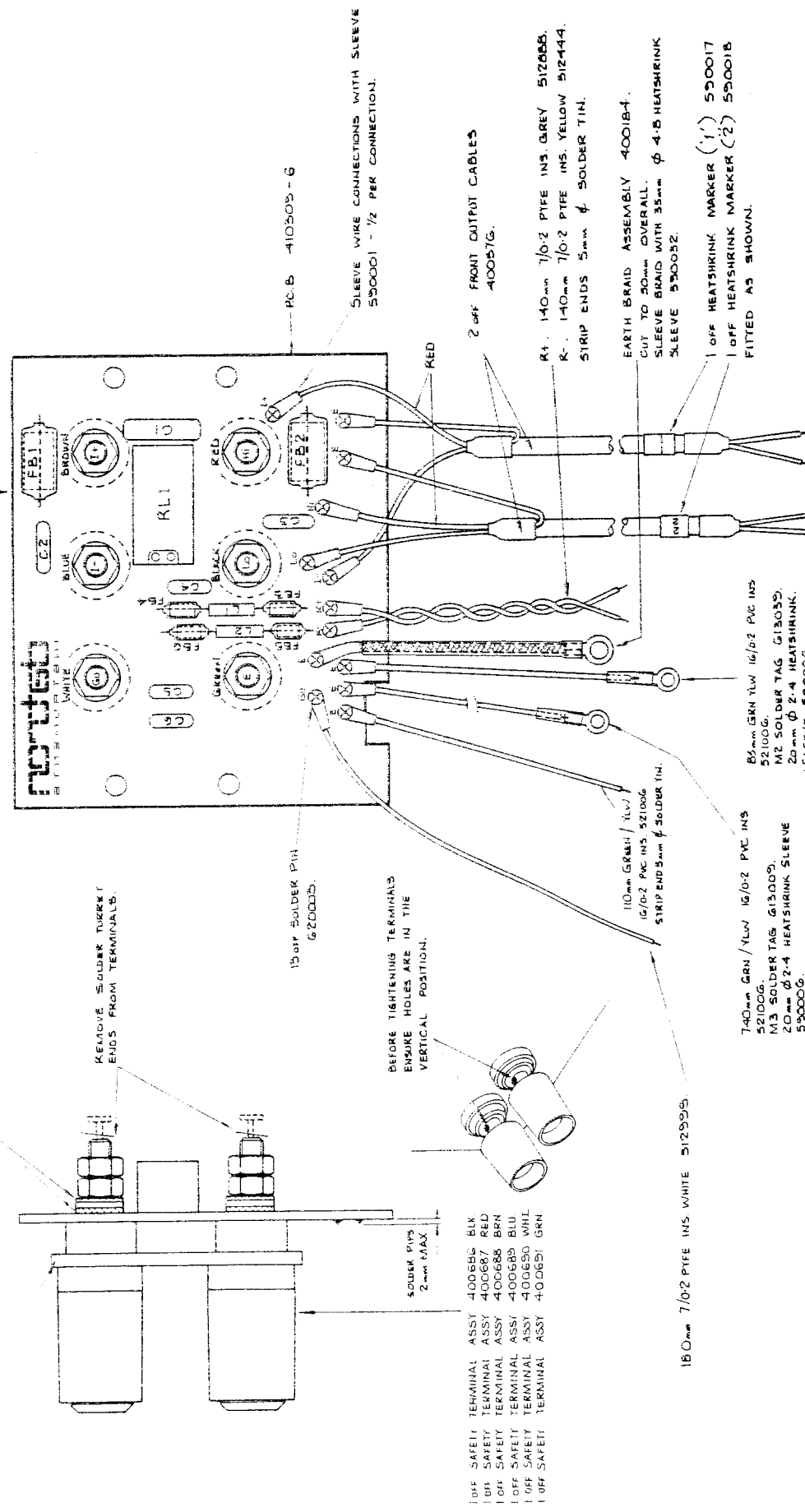
TERMINAL BOARD ASSEMBLY

SLEEVE ALL FERRITE BEADS
 FB1 & FB2 USE Ø 0.4 HEATSHRINK SLEEVE 550005.
 FB3, FB4, FB5 & FB6 USE Ø 4 HEATSHRINK SLEEVE 550032.
 ASSEMBLE FB3, FB4, FB5 & FB6 ON CHOICE LEADS AS SHOWN.
 FB1 & FB2 FITTED ON THINNED COPPER WIRE 540002.

WASHER SUPPLIED WITH TERMINAL IS NOT TO BE USED AS IT IS TOO LARGE.

SECURE TERMINAL USING:-
 2 OFF M4 SHAKEPROOF G13021 } PER TERMINAL
 1 OFF M4 PLAIN WASHER G13020 }
 USE NUTS AS SUPPLIED WITH TERMINALS.

TERMINAL PLATE
 4502 G5



- 1 OFF SAFETY TERMINAL ASSY 400656 BLK
- 1 OFF SAFETY TERMINAL ASSY 400667 RED
- 1 OFF SAFETY TERMINAL ASSY 400688 BRN
- 1 OFF SAFETY TERMINAL ASSY 400689 BLU
- 1 OFF SAFETY TERMINAL ASSY 400690 WHL
- 1 OFF SAFETY TERMINAL ASSY 400691 GRN

BEFORE TIGHTENING TERMINALS
 ENSURE HOLES ARE IN THE
 VERTICAL POSITION.

SOLDER PIPS
 2mm MAX

15 OFF SOLDER PIP
 G20005

REMOVE SOLDER TORQUE
 ENDS FROM TERMINALS.

SLEEVE WIRE CONNECTIONS WITH SLEEVE
 550001 - 1/2 PER CONNECTION.

2 OFF FRONT OUTPUT CABLES
 400576

R1. 140mm 7/0-2 PTFE INS. GREY 512655.
 R2. 140mm 7/0-2 PTFE INS. YELLOW 512444.
 STRIP ENDS 5mm Ø SOLDER TIN.

EARTH BRAID ASSEMBLY 400184.
 CUT TO 50mm OVERALL.
 SLEEVE BRAID WITH 35mm Ø 4-B HEATSHRINK
 SLEEVE 550052

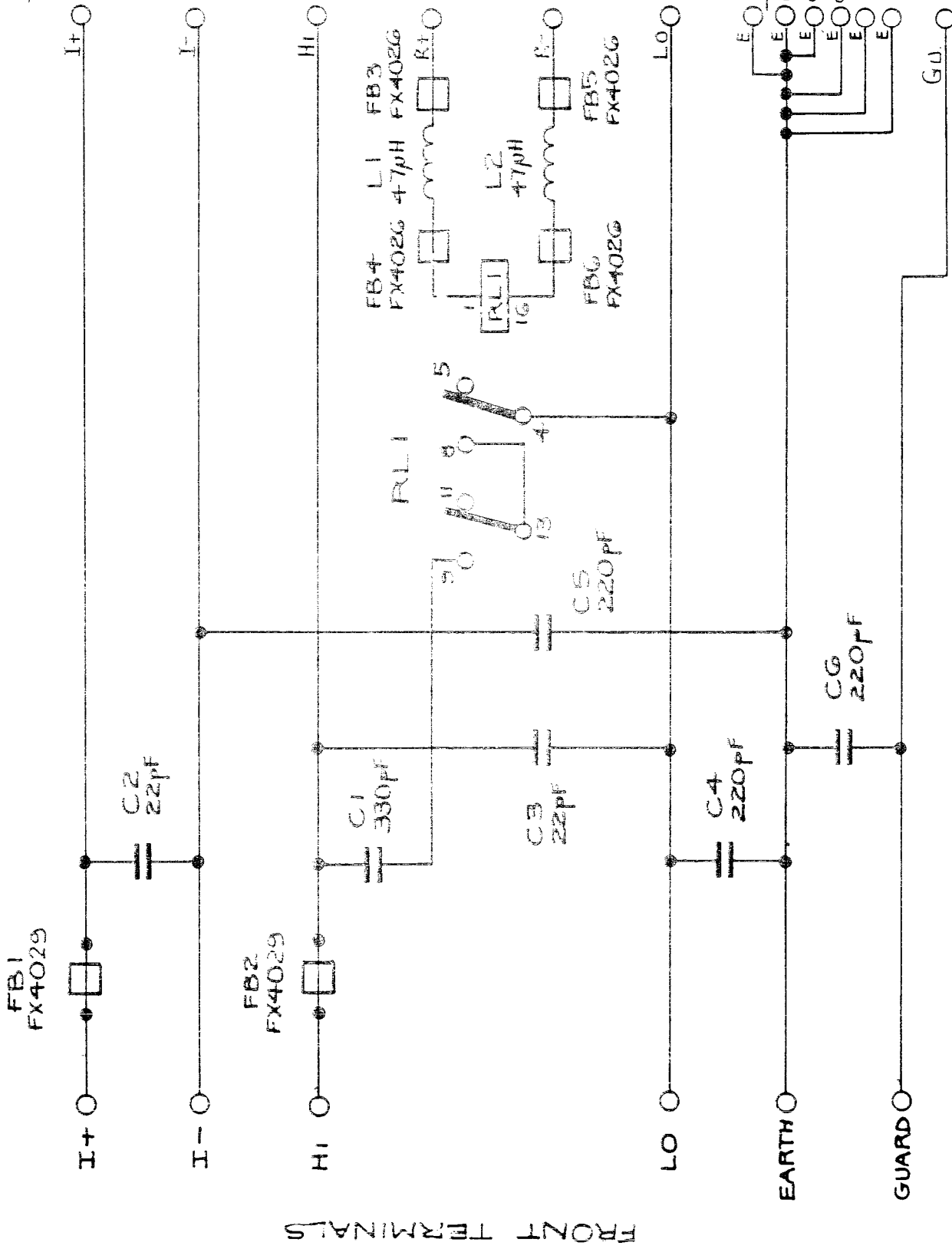
1 OFF HEATSHRINK MARKER (1) 550017
 1 OFF HEATSHRINK MARKER (2) 550018
 FITTED AS SHOWN.

85mm GRN YLW 16/02 PVC INS
 521006.
 M2 SOLDER TAG G13039.
 20mm Ø 2-A HEATSHRINK.
 SLEEVE 550006.

740mm GRN/YLW 16/02 PVC INS
 521006.
 M3 SOLDER TAG G13039.
 20mm Ø 2-A HEATSHRINK SLEEVE
 550006.

10mm GRN/YLW
 16/0-2 PVC INS 521006
 STRIP ENDS 5mm Ø SOLDER TIN.

180mm 7/0-2 PTFE INS. WHITE 512995



TO MOTHER BOARD ASSEMBLY

X M A D W U N I O ' 9 2 D

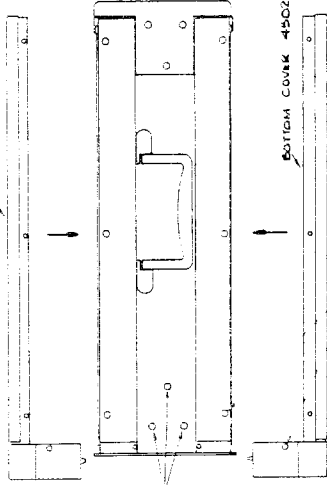
FRONT TERMINALS

INSTRUMENT ASSEMBLY

NOTES

1. FIT INTO CAL # SER# HANDBOOK:-
 1.1. LAY 3/32" DIA 1/4" ANTI-BURST FUSE.
 1.2. OFF GROUND 2.5mm A/P HEX KEY.
 2. OFF CAL SWITCH KEYS (FROM REAR PANEL ASSY).
 3. LINK K ON REF DIVIDER POW ASSY
 IS TO BE MADE FOR INSTRUMENTS
 WITH H.V. OPTIONS FITTED & SUI IF
 NOT FITTED.
 4. FOR ALL OPTION FITTING INSTRUCTIONS
 SEE DRAWING 4806003
- OVERLAY FITTING PROCEDURE**
1. CLEAN FRONT PANEL METALWORK
 2. FIT PANEL ALIGN & FIT OVERLAY BY
 USING ROLLER (FOR SIMILAR)
 3. TRIM OFF ANY EXCESS OVERLAY FROM OVERHANGS
 4. LEAVE THIS ASSEMBLED PANEL FOR 24 HOURS (MIN)
 5. RE-LOCATE OVERLAY TO ORIGINAL POSITION
 6. REPLACE THIS PANEL ON THE ORIGINAL INSTRUMENT.

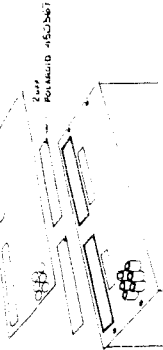
TOP COVER 450213



BOTTOM COVER 450214

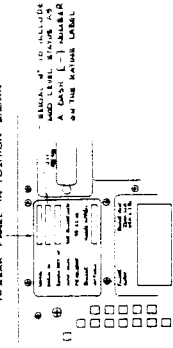
FIT 450212-- SECURE REAL C.S.K. SCREWS
 510336 IN IG POSITIONS

VARIABLE RESISTOR
 SEE NOTES

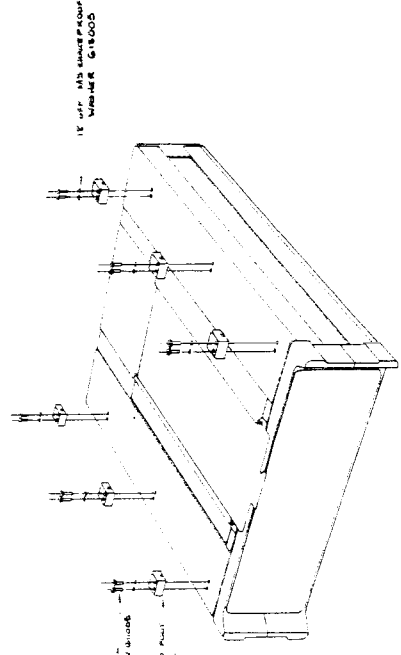


Fit the main wiring assembly into
 the main wiring assembly in the
 positions for the main wiring
 assembly on the main wiring
 assembly

STICK RAYING LABEL 450203
 TO REAR PANEL IN POSITION SHOWN

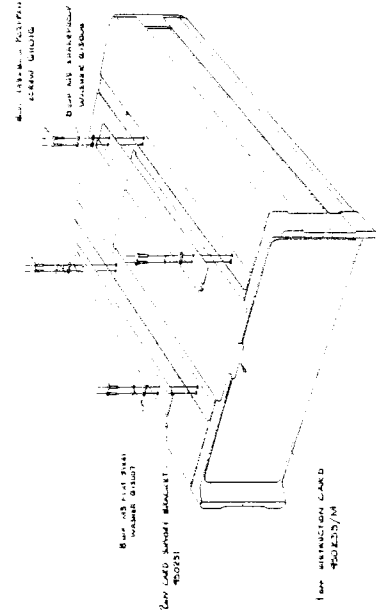


REAR PANEL TO INCLUDE
 A GASKET (L) UNDER
 AT THE RAYING LABEL



IF CAL. 1150 WIRE-PROOF
 WIRE-PROOF GROUND

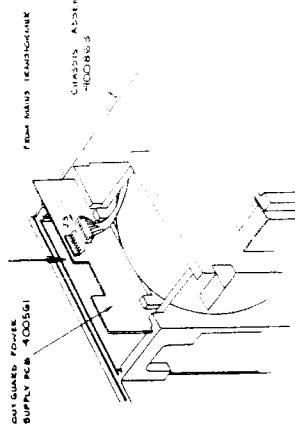
REAR PANEL-- SECURE REAL C.S.K. SCREWS
 510336 IN IG POSITIONS



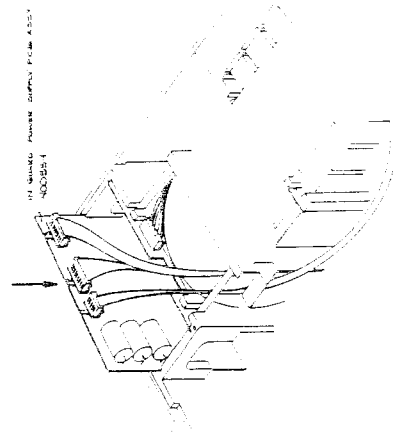
REAR PANEL-- SECURE REAL C.S.K. SCREWS
 510336 IN IG POSITIONS

FOR INSTRUCTION CABLE
 450203/14

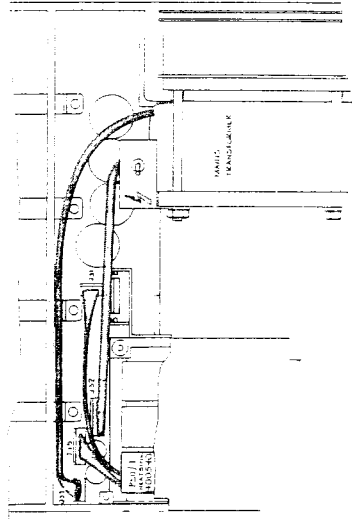
1



2



3



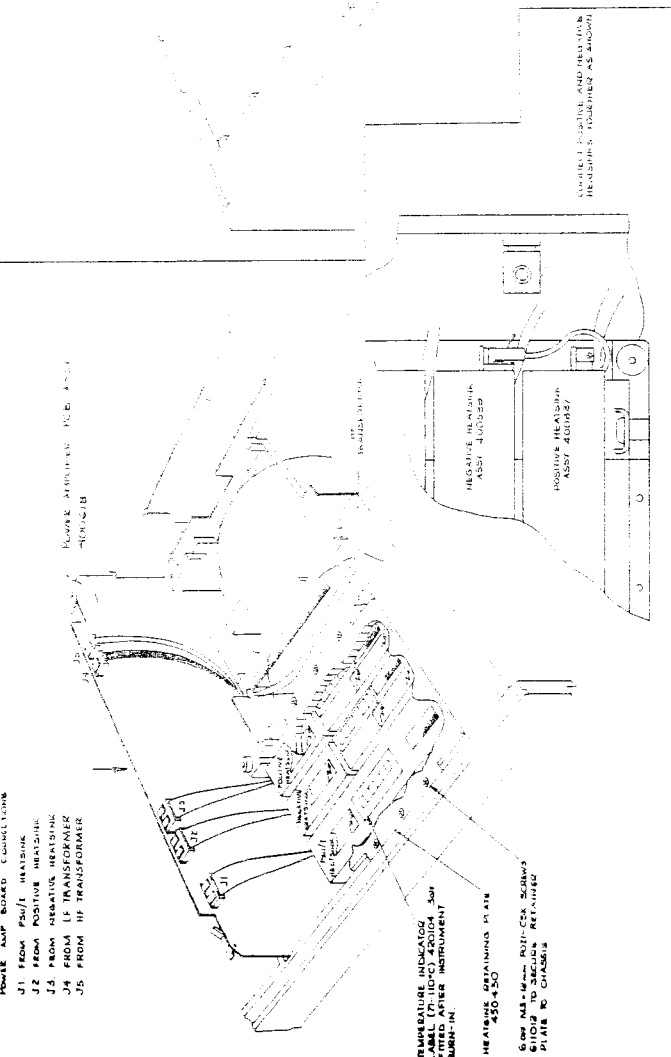
INWARD PCB CONNECTIONS
 J1 FROM POWER SUPPLY TRANSFORMER
 J2 FROM MAIN TRANSFORMER
 J3 FROM MAIN TRANSFORMER

NOTE
 CLEAN ALL PCB EDGE CONTACTS WITH
 CLEANING FLUID BEFORE DOING BRIDGE
 FINAL ASSEMBLY & AT FINAL INSPECTION
 STAGE
 STEPS 3 5 6 7

4

POWER AMP BOARD CONNECTIONS
 J1 FROM PAU/I HEATING
 J2 FROM POSITIVE HEATING
 J3 FROM NEGATIVE HEATING
 J4 FROM LF TRANSFORMER
 J5 FROM HF TRANSFORMER

5



TEMPERATURE INDICATOR LABEL (711010) 42004 50p
 HEATING RETAINING PLATE INSTRUMENT MOUNT
 HEATING RETAINING PLATE 430430
 50p MOUNTING INSTRUMENT MOUNTING PLATE TO CHASSIS

HIGH VOLTAGE WASHED CONNECTIONS
 J1 FROM HF TRANSFORMER
 J2 FROM LF TRANSFORMER
 J3 FROM LF TRANSFORMER
 J4 FROM ALTO LABO RESISTOR ON
 MAIN TRANSFORMER CORE

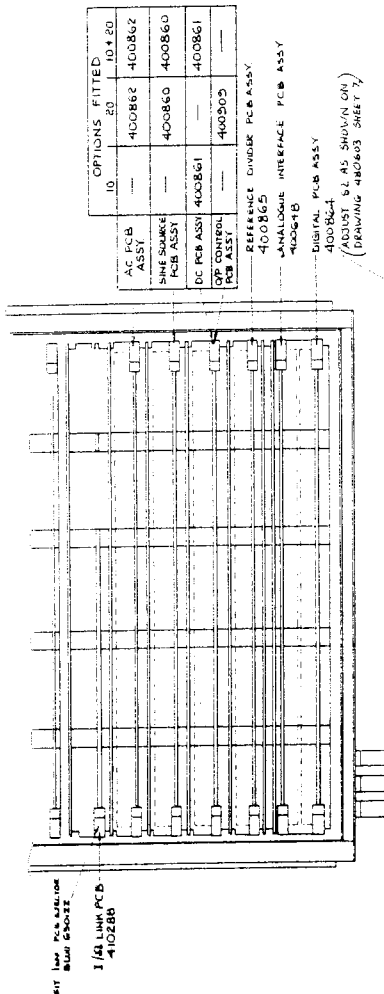
MAIN ASSEMBLY

Layout Drawing No. DA400859-1.1

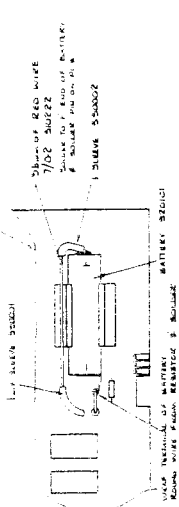
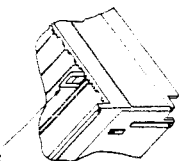
Sheet 1

6

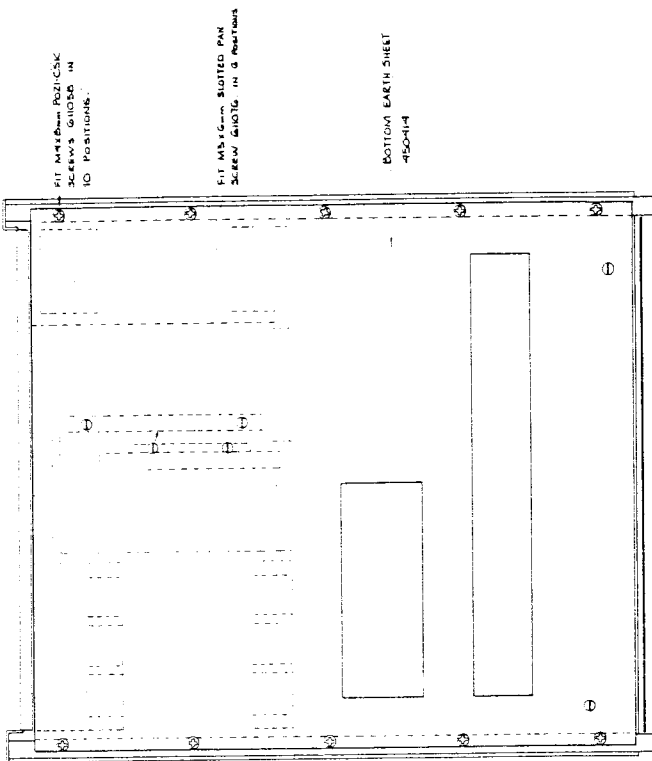
TEST
 CLEAN ALL PCB EDGE SURFACES WITH CLEANING
 FLUID. SOLDER GOTS BEFORE INITIAL ASSEMBLY
 AND AT FINAL INSPECTION STAGE.



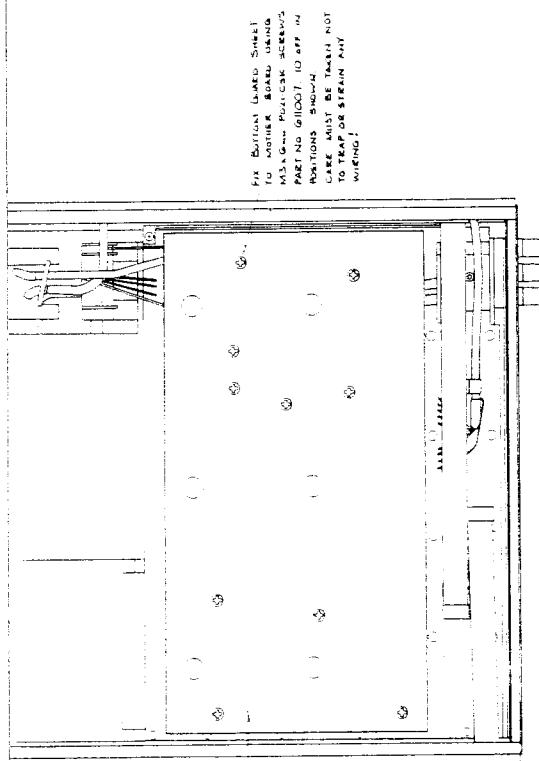
TRANSFER THE
 LABEL (7-45) 42008
 AFTER INSTRUMENT
 SERVICE

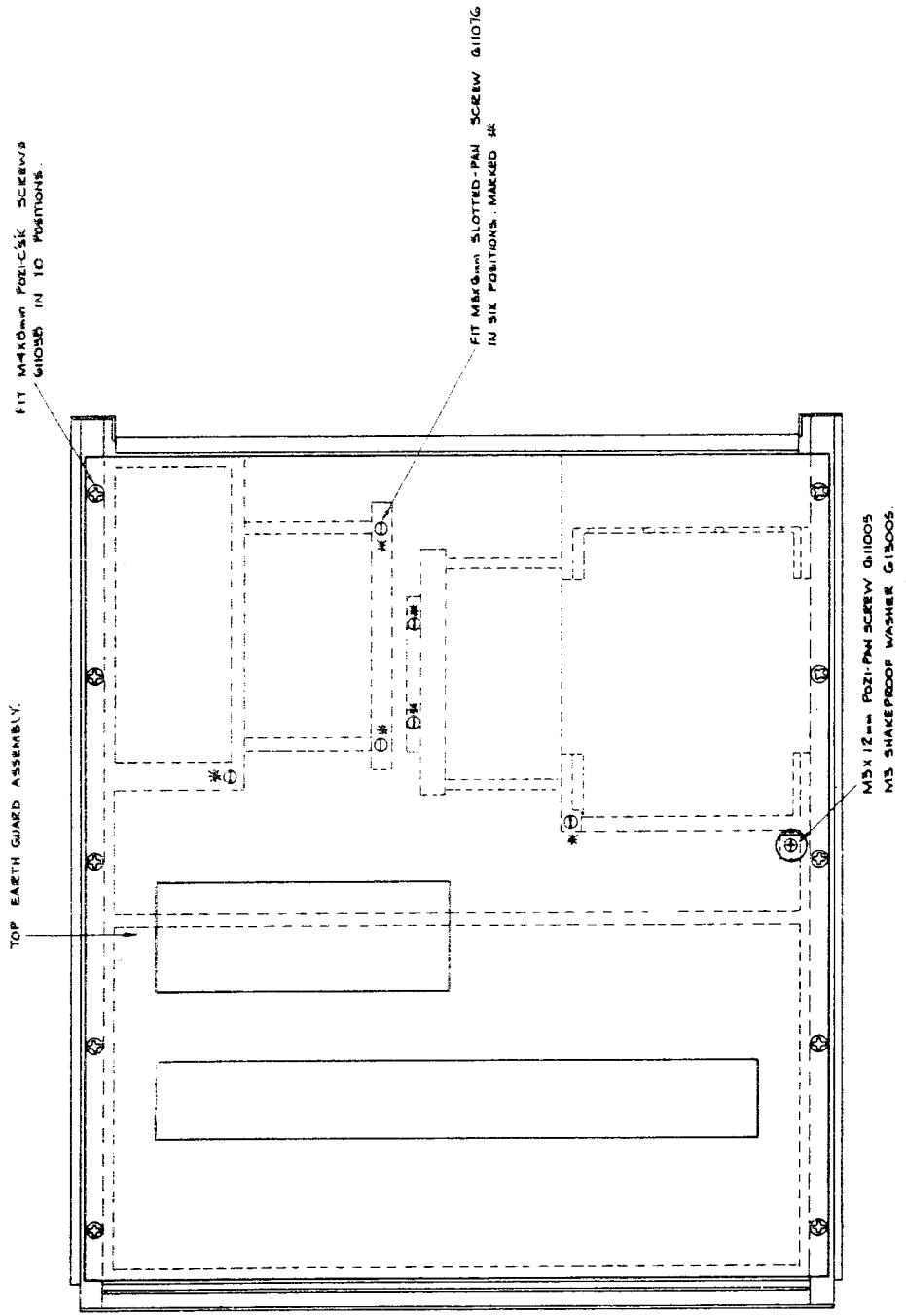


8



7



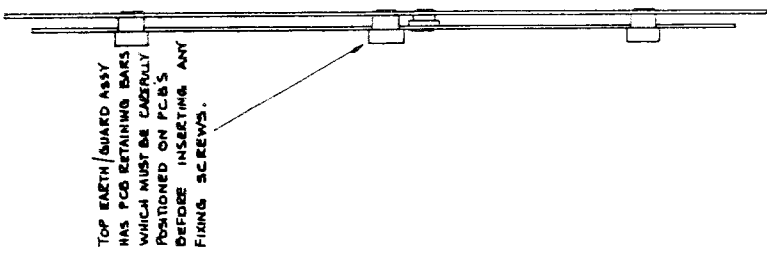


TOP EARTH GUARD ASSEMBLY.

FIT M4X6mm POZI-DRILL SCREWS G1035B IN 10 POSITIONS.

FIT M8X6mm SLOTTED-PAN SCREW G1107G IN SIX POSITIONS. MARKED #8

M3X 12mm POZI-PAN SCREW G1100S
M3 SHAKEPROOF WASHER G1300S

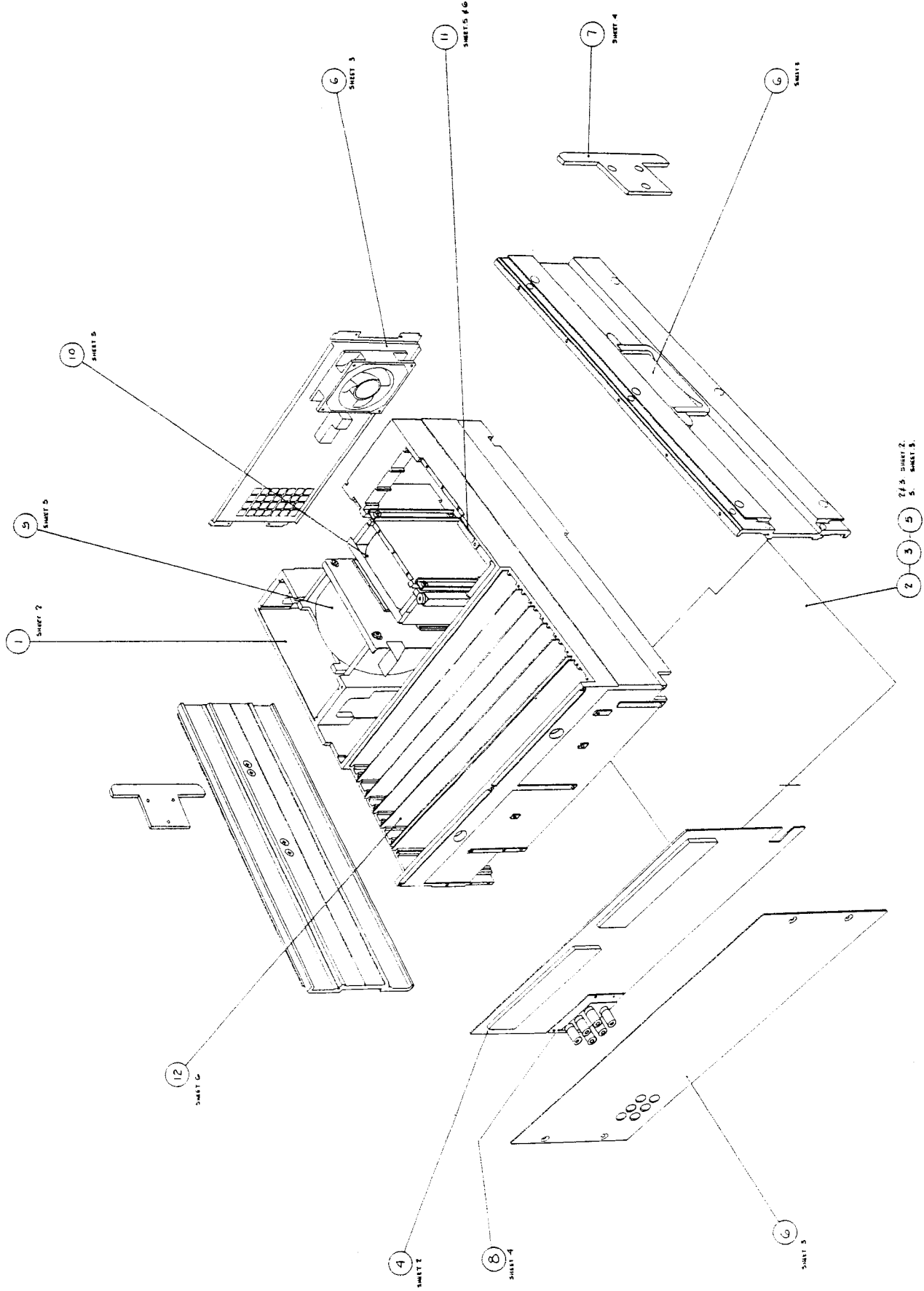


TOP EARTH GUARD ASSY HAS PCB RETAINING BARS WHICH MUST BE CAREFULLY POSITIONED ON PCB'S BEFORE INSERTING ANY FIXING SCREWS.

MAIN ASSEMBLY

Layout Drawing No. DA400659-1.0 Sheet 3

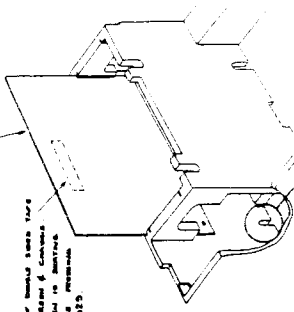
CHASSIS ASSEMBLY



1

FROM BERRY GAIN SCREEN GEOSIC

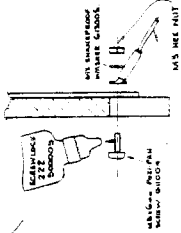
USE 30mm OF INSULATED THERM TUBE
 BETWEEN GAIN SCREEN AND CHASSIS.
 POSITION SCREEN FRAME BOARD INTO PLACE.
 CONNECTIVELY WIRING TO SCREEN.
 COVER TOP GEOSIC.



USE 30mm INS.
 GEOSIC

2mm ϕ 4 MOUNTING
 SCREW
 500993

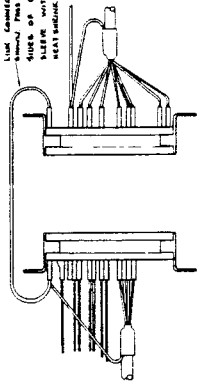
240mm



WASHER PER PART NO. 400604
 MS 100 NUT
 503002

2

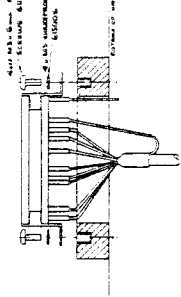
USE GEOSIC WITH TUBE AS
 SHOWN. INSULATE BETWEEN BERRY
 TUBE AND CONNECTION BOARD.
 SLITER WITH 15mm AT 5/16
 HEATSHIELD GEOSIC.



MS 100 NUT

503002

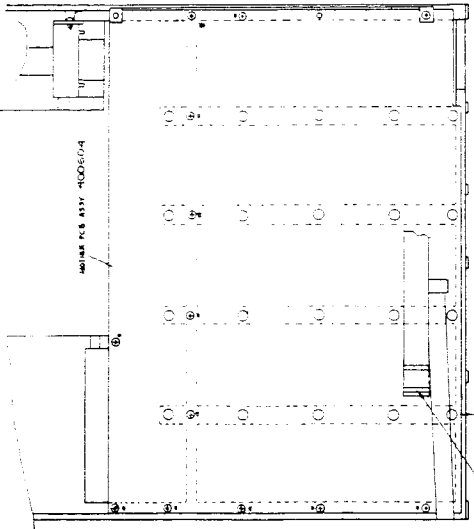
4mm 30mm PER PART
 NO. 400604



4mm 30mm PER PART
 NO. 400604

MS 100 NUT
 503002

3



MS 100 NUT

503002

1mm MS 100 PER PART NO. 400604
 1mm 30mm PER PART NO. 400604
 THE SECOND SCREW IS FITTED
 IN A LARGER SLOT.
 EARTH MOUNT
 400601

MS 100 NUT

503002

MS 100 NUT

503002

MS 100 NUT

503002

MS 100 NUT

503002

MS 100 NUT

503002

MS 100 NUT

503002

MS 100 NUT

503002

MS 100 NUT

503002

MS 100 NUT

503002

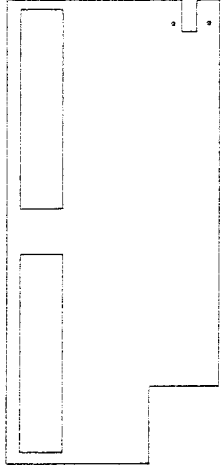
MS 100 NUT

503002

MS 100 NUT

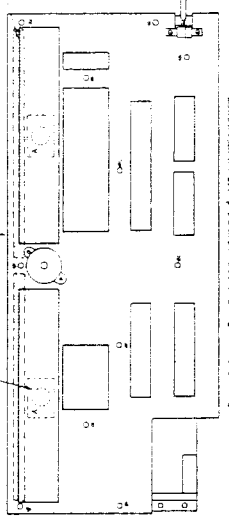
503002

4



GEOSIC POWER SUPPLY
 A 2 GEOSIC FITTED TO INSIDE OF CHASSIS COVER
 DISPLAY CLEARANCE 10mm

FRONT PER. ASSY 400608



FRONT PER. ASSY 400608
 FIT WITH BERRY PER. ASSY 400608 & MS WAXY WAXER
 GEOSIC IN 16 POSITIONS MARKED X

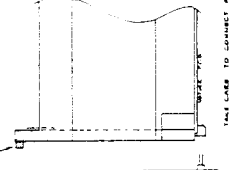
2mm MS 100 PER PART NO. 400604
 WASHER 503002

NOTE: ASSEMBLY WITH WAXER, PINS
 AT BOTTOM (AS SHOWN)

WASHER PER. ASSY 400608

2mm MS 100 PER PART NO. 400604
 WAXER PER. ASSY 400608

GEOSIC
 2 PIECES OF 6mm THICK
 BY 7mm WIDE FOAM TAPE



NOTE: USE TO CONNECT ALL PINS

FROM BERRY GAIN SCREEN GEOSIC

WHEN ATTACH WAXER PER TO CHASSIS CHECK THAT ALL WAXER ARE IN THE UP
 POSITION BEFORE FRAME BOARD INTO PLACE. DEFLECT ALL WAXER THEN FIT
 WAXER PER. ASSY 400608 & MS WAXY WAXER GEOSIC IN HAVE POSITIONS
 MARKED X

MS 100 NUT

503002

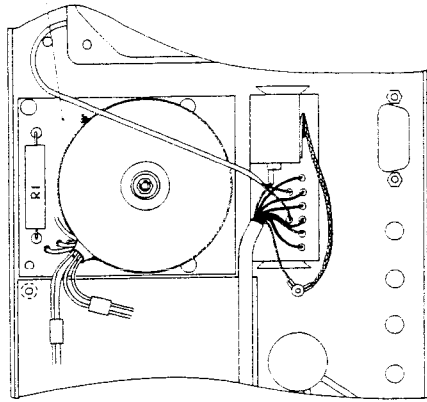
2mm ϕ 4 MOUNTING
 SCREW
 500993

WASHER PER. ASSY 400604
 MS 100 NUT
 503002

CHASSIS ASSEMBLY

Layout Drawing No. DA400863-1-0 Sheet 2

CHASSIS ASSEMBLY



HF TRANSFORMER ASSY
100-878

4 #12 M35 SHANKS
4 #12 M35 HEADS
4 #12 M35 HEADS
4 #12 M35 HEADS

1 #12 M35 IN ENGLISH
FITTED USING 2 #12 M35
2 #12 M35 HEADS
2 #12 M35 HEADS

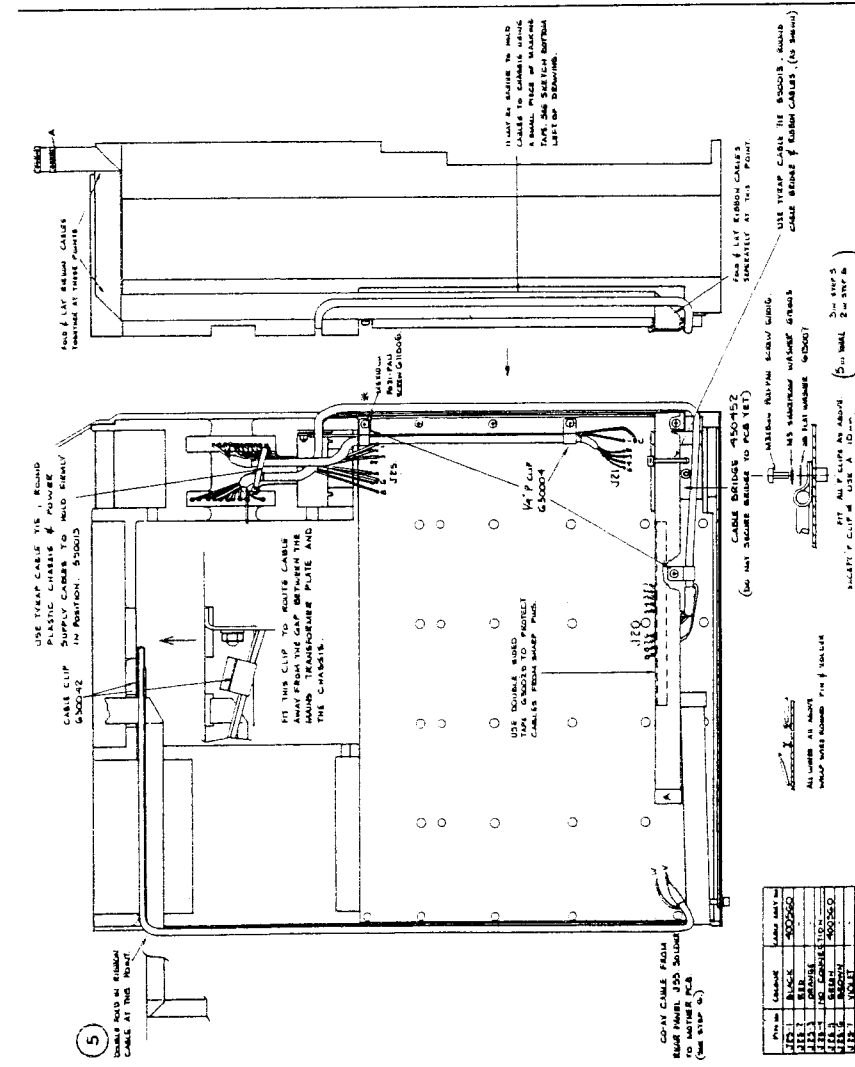
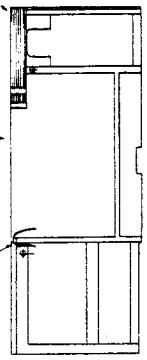
BEAR PAPER ASSY
400-310

2 #12 M35 SHANKS
2 #12 M35 HEADS

WIRE FITTING: MAKE SURE CABLE
WIRE IS PROPERLY SEATED
WIRE, ESPECIALLY SHIELDING
WIRE, IS PROPERLY SEATED
WIRE, ESPECIALLY SHIELDING
WIRE, IS PROPERLY SEATED

RIBBON CABLES LAY IN
RIBBON IN PLASTIC CHANNEL.

WIRE FROM PWB TO BE POSITIONED
WIRE FROM PWB TO BE POSITIONED
WIRE FROM PWB TO BE POSITIONED



USE TRAP CABLE VIS. ROUND
PLASTIC CHANNEL TO HOLD SERIAL
SUPPLY CABLES TO HOLD SERIAL
IN POSITION. 500-242

5

DOUBLE END OF RIBBON
CABLE AT THIS POINT

USE THIS CLIP TO SECURE CABLE
AWAY FROM THE GAP BETWEEN THE
BOARD TRANSFORMER PLATE AND
THE CHASSIS.

USE ROUND WIRE
CABLES FROM SHAFER PWB.

1/4" PCLIP
CABLES

1/2" PCLIP
CABLES

1/4" PCLIP
CABLES

1/2" PCLIP
CABLES

1/4" PCLIP
CABLES

1/2" PCLIP
CABLES

1/4" PCLIP
CABLES

1/2" PCLIP
CABLES

1/4" PCLIP
CABLES

1/2" PCLIP
CABLES

1/4" PCLIP
CABLES

1/2" PCLIP
CABLES

1/4" PCLIP
CABLES

1/2" PCLIP
CABLES

1/4" PCLIP
CABLES

1/2" PCLIP
CABLES

1/4" PCLIP
CABLES

1/2" PCLIP
CABLES

1/4" PCLIP
CABLES

1/2" PCLIP
CABLES

1/4" PCLIP
CABLES

1/2" PCLIP
CABLES

1/4" PCLIP
CABLES

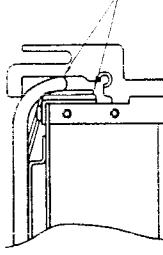
1/2" PCLIP
CABLES

1/4" PCLIP
CABLES

1/2" PCLIP
CABLES

| Part No. | Quantity | Part Name | Part No. |
|----------|----------|-----------|----------|
| 100-250 | 1 | BLACK | 100-250 |
| 100-251 | 1 | RED | 100-251 |
| 100-252 | 1 | GREEN | 100-252 |
| 100-253 | 1 | YELLOW | 100-253 |
| 100-254 | 1 | BLUE | 100-254 |
| 100-255 | 1 | BROWN | 100-255 |
| 100-256 | 1 | PURPLE | 100-256 |
| 100-257 | 1 | PINK | 100-257 |
| 100-258 | 1 | WHITE | 100-258 |
| 100-259 | 1 | GRAY | 100-259 |
| 100-260 | 1 | BLACK | 100-260 |
| 100-261 | 1 | RED | 100-261 |
| 100-262 | 1 | GREEN | 100-262 |
| 100-263 | 1 | YELLOW | 100-263 |
| 100-264 | 1 | BLUE | 100-264 |
| 100-265 | 1 | BROWN | 100-265 |
| 100-266 | 1 | PURPLE | 100-266 |
| 100-267 | 1 | PINK | 100-267 |
| 100-268 | 1 | WHITE | 100-268 |
| 100-269 | 1 | GRAY | 100-269 |
| 100-270 | 1 | BLACK | 100-270 |

6



POSITION OF WIRES IN SIDE EXTRUSION SHOULD
BE AS SHOWN SO AS TO AVOID TAPPING &
DAMAGING THE CABLE CASE TAPER AT THIS
POINT. WIRE FITTING MUST BE PRECISE
TO AVOID DAMAGE TO THE WIRE & FAST FITTING
OF FRONT & REAR PANELS.

FRONT PANEL
100-478

K.N. SIDE EXTRUSION
400-310

1.1 N SIDE EXTRUSION
400-311

WIRE FROM PWB TO BE POSITIONED
WIRE FROM PWB TO BE POSITIONED
WIRE FROM PWB TO BE POSITIONED

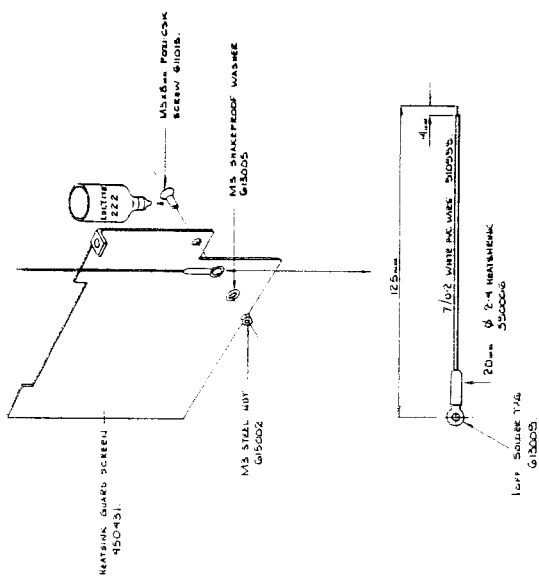
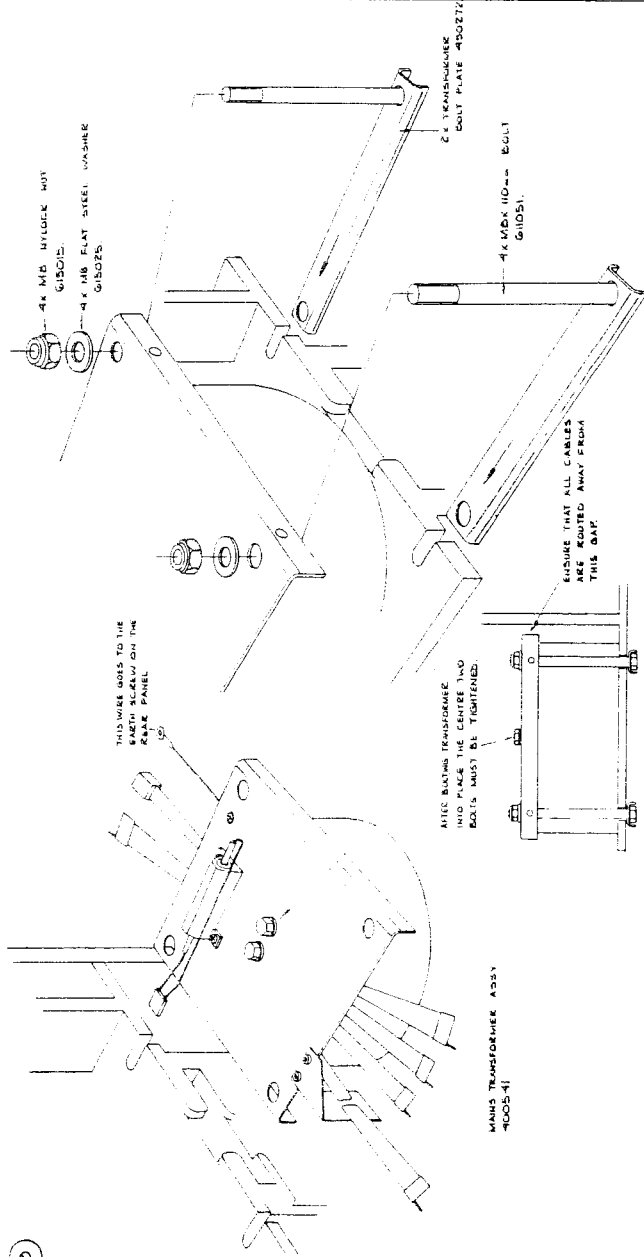
FRONT BARRET (SCHEM)
100-478

2.00 INCHES
WIRE

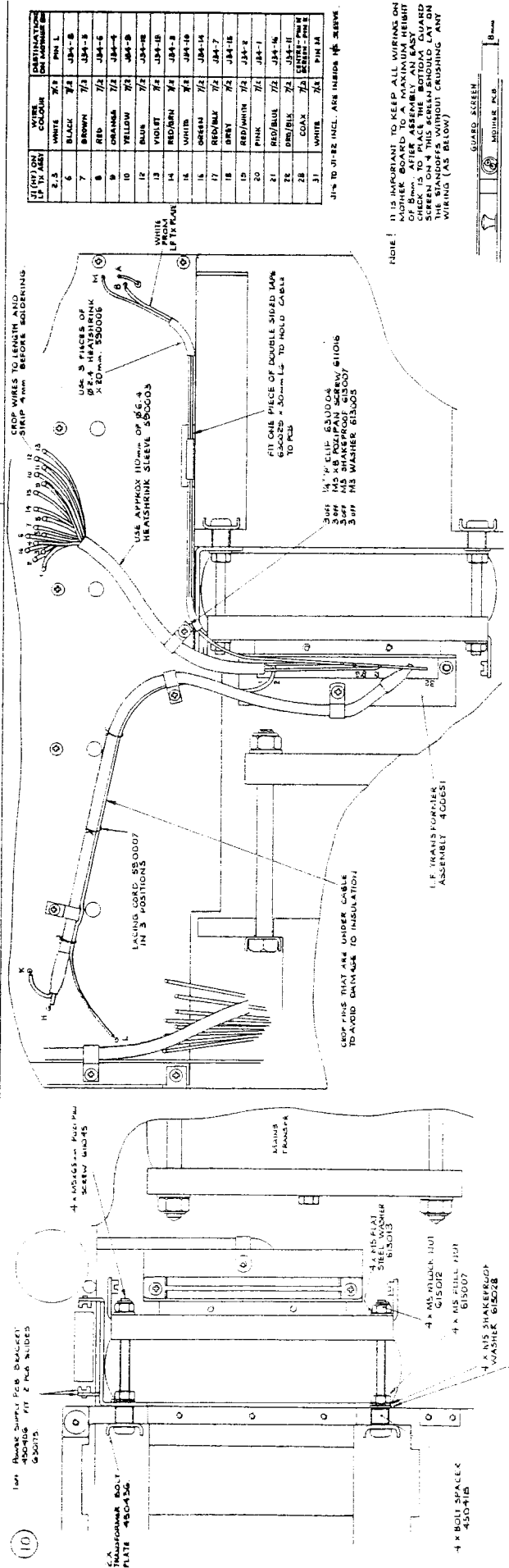
2.00 INCHES
WIRE

CHASSIS ASSEMBLY

11



9

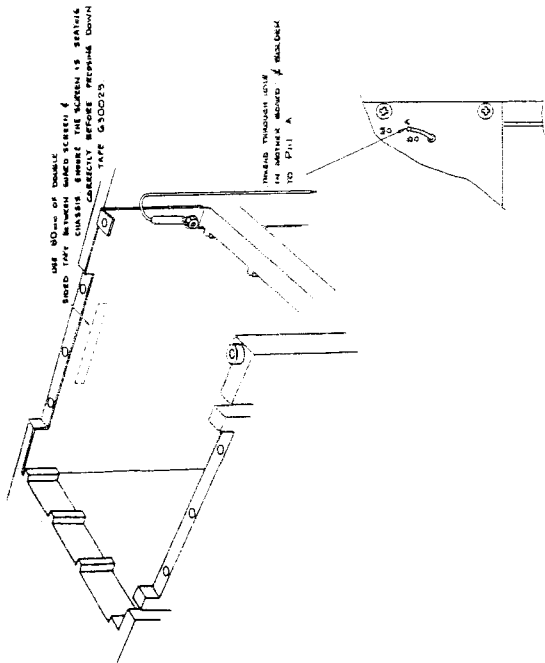


| LT (W) ON LEFT TO ASSEMBLY | WIRE COLOUR | WIRE PIN L. | WIRE ON MAINBOARD |
|----------------------------|-------------|-------------|-------------------|
| 2, 3 | WHITE | 7/8 | PH 1 |
| 6 | BLACK | 7/8 | JPA-8 |
| 7 | BROWN | 7/8 | JPA-3 |
| 8 | RED | 7/8 | JPA-5 |
| 9 | ORANGE | 7/8 | JPA-9 |
| 10 | YELLOW | 7/8 | JPA-5 |
| 12 | BLUE | 7/8 | JPA-18 |
| 13 | VIOLET | 7/8 | JPA-18 |
| 14 | RED/BRN | 7/8 | JPA-8 |
| 15 | WHITE | 7/8 | JPA-10 |
| 16 | GREEN | 7/8 | JPA-14 |
| 17 | RED/BLK | 7/8 | JPA-7 |
| 18 | GRY | 7/8 | JPA-16 |
| 19 | RED/WHN | 7/8 | JPA-2 |
| 20 | PINK | 7/8 | JPA-1 |
| 21 | RED/BLU | 7/8 | JPA-6 |
| 22 | DRY/BLK | 7/8 | JPA-11 |
| 23 | DRY/BLK | 7/8 | JPA-11 |
| 24 | DRY/BLK | 7/8 | JPA-11 |
| 25 | DRY/BLK | 7/8 | JPA-11 |
| 26 | DRY/BLK | 7/8 | JPA-11 |
| 27 | DRY/BLK | 7/8 | JPA-11 |
| 28 | DRY/BLK | 7/8 | JPA-11 |
| 29 | DRY/BLK | 7/8 | JPA-11 |
| 30 | DRY/BLK | 7/8 | JPA-11 |
| 31 | WHITE | 7/8 | PH 1 |

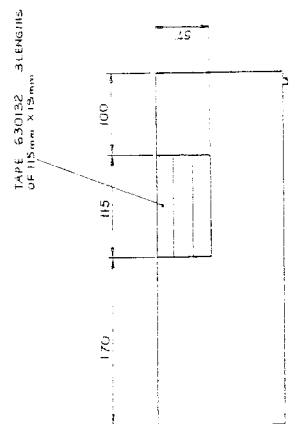
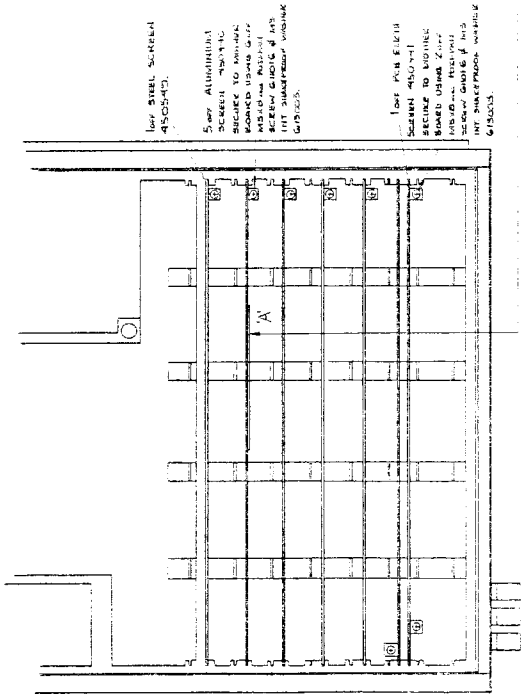
NOTE: IT IS IMPERATIVE TO KEEP ALL WIRING ON CHASSIS GUARD TO MAXIMUM HEIGHT OF 1/8\"/>



11



12



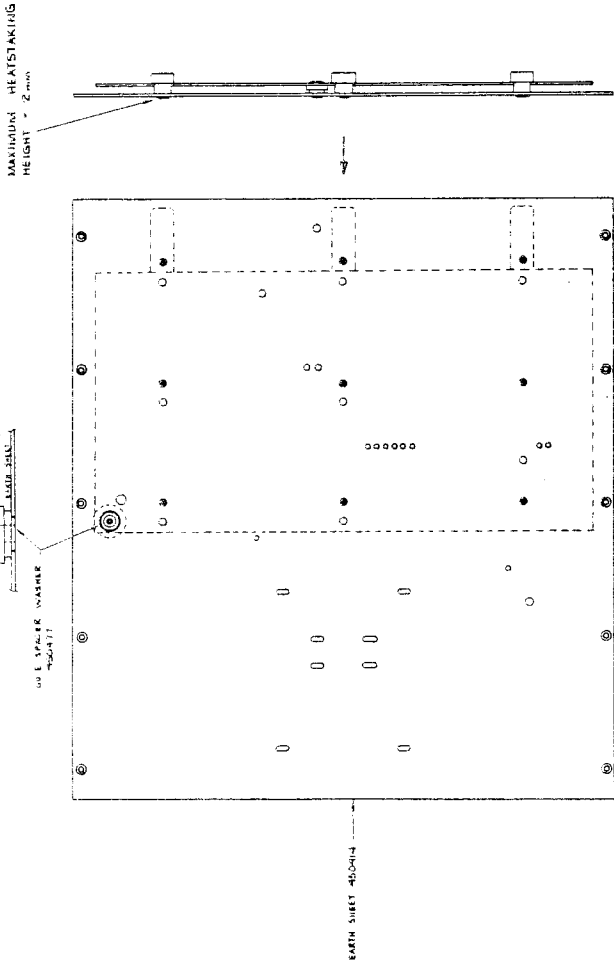
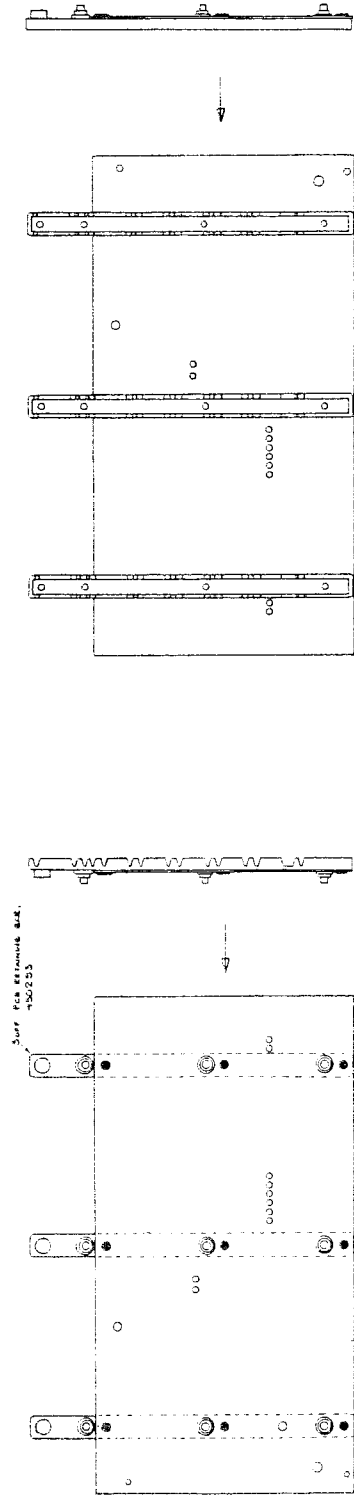
VIEW IN DIRECTION OF ARROW 'A' SHOWING ONLY GUARD SCREEN

CHASSIS ASSEMBLY

Layout Drawing No. DA400863-1.1

Sheet 6

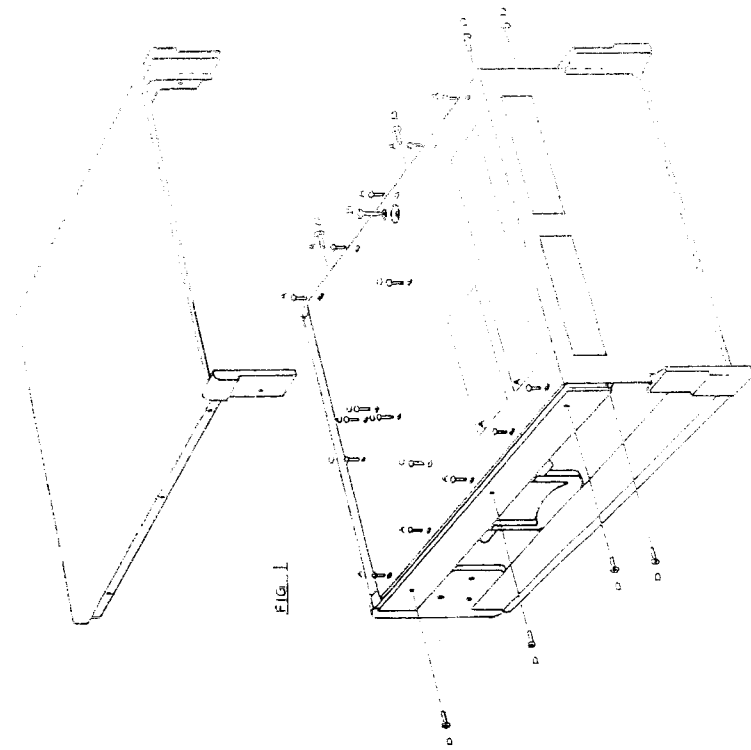
CHASSIS ASSEMBLY



WHEN THE CHASSIS ASSY IS COMPLETE CHECK THAT THE TOP EARTH GUARD SHEET ASSEMBLY, BOTTOM GUARD & EARTH SHEETS FIT.

OPTION FITTING INSTRUCTIONS

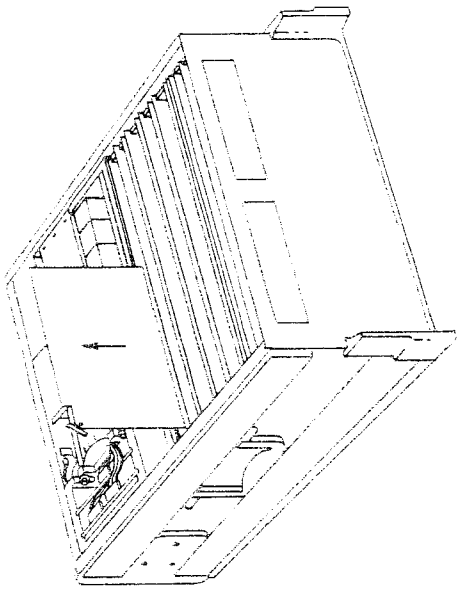
Option 30: Current / Ohms



CURRENT OHMS OPTION

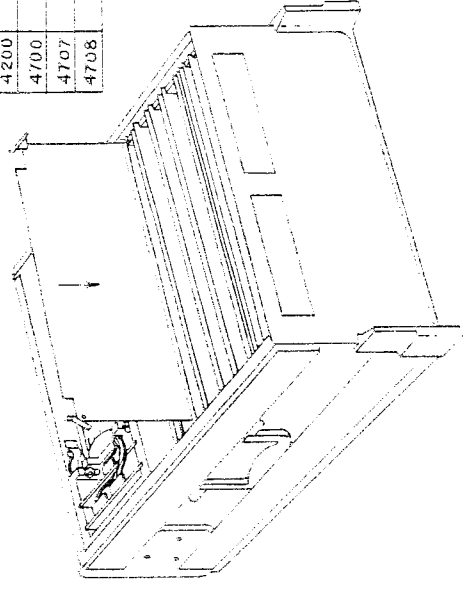
PROCEDURE:

- ① REMOVE THE 8 SCREWS WHICH SECURE THE LID IN POSITION. TO DO THIS LIFT THE LID OFF. THERE ARE 17 SCREWS TO REMOVE THROUGH THE GUARD SHIELD. CAN BE TAKEN AWAY.
- ② REPLACE THE GUARD SHIELD AND REFIT THE SCREWS IN THE POSITIONS SHOWN IN FIG. 1.
 - A 10 OFF M4 X 6MM POINT CSK SCREWS (GROUP)
 - B 1 OFF M3 X 12MM POINT PAN SCREWS (GROUP)
 - C 6 OFF M3 X 6MM SLOTTED PAN HD SCREWS (GROUP)
 - USE M3 SHAKEPROOF WASHER (H) SCREW (B) ONLY.
 - POSITION LID & SECURE WITH:
 - D 8 OFF M4 X 12MM SOCKET HD - CSK SCREW (GROUP)



- ② THE GREY PLASTIC INNER CHASSIS DIVIDES THE INTERNAL SPACE INTO TWO AREAS. THE LAST POSITION IN THE FRONT SECTION CONTAINS A HALF WIDTH PCB WHICH IS FITTED WHEN THE CURRENT OPTION IS NOT REQUIRED.
- ③ REMOVE THE LINK PCB AND REPLACE IT WITH THE CURRENT / OHMS BOARD - SEE TABLE.

| INSTR. | OPTION | ASSY N° |
|--------|--------|---------|
| 4200 | 30 | 400555 |
| 4700 | 20 | 400614 |
| 4707 | 27 | 400732 |
| 4708 | 30 | 400867 |



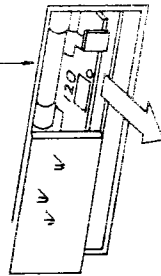
OPTION 80 115V 60HZ KIT OF PARTS 440094

PROCEDURE:

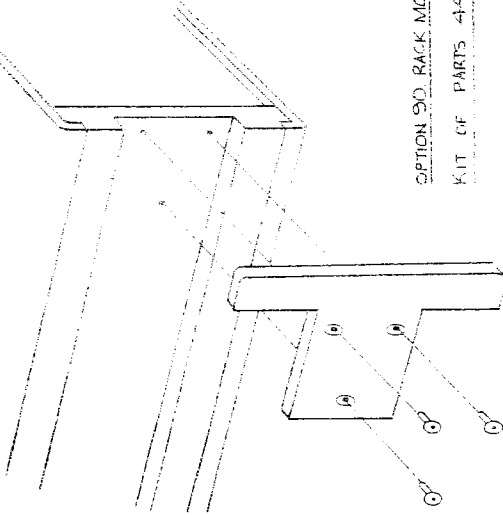
1. CHANGE MAINS FUSE
2. CHANGE VOLTAGE P.C.B.
3. ENSURE THAT CORRECT VOLTAGE AND FREQUENCY ARE STATED ON THE RATING LABEL.
4. ON FINAL CHECK, USE THE INST. INC. CERTIFICATE OF QUALITY CONFORMANCE FORM S3
5. REPLACE FUSE IN SERVICING MANUAL ACCESSORY VALLET WITH 6.25A 250V 1 1/4" SLO-4 FUSE.

CHANGE MAINS FUSE TO:
 6.25A 250V 1 1/4" SLO-4 FUSE.

DETAIL FROM
 REAR PANEL



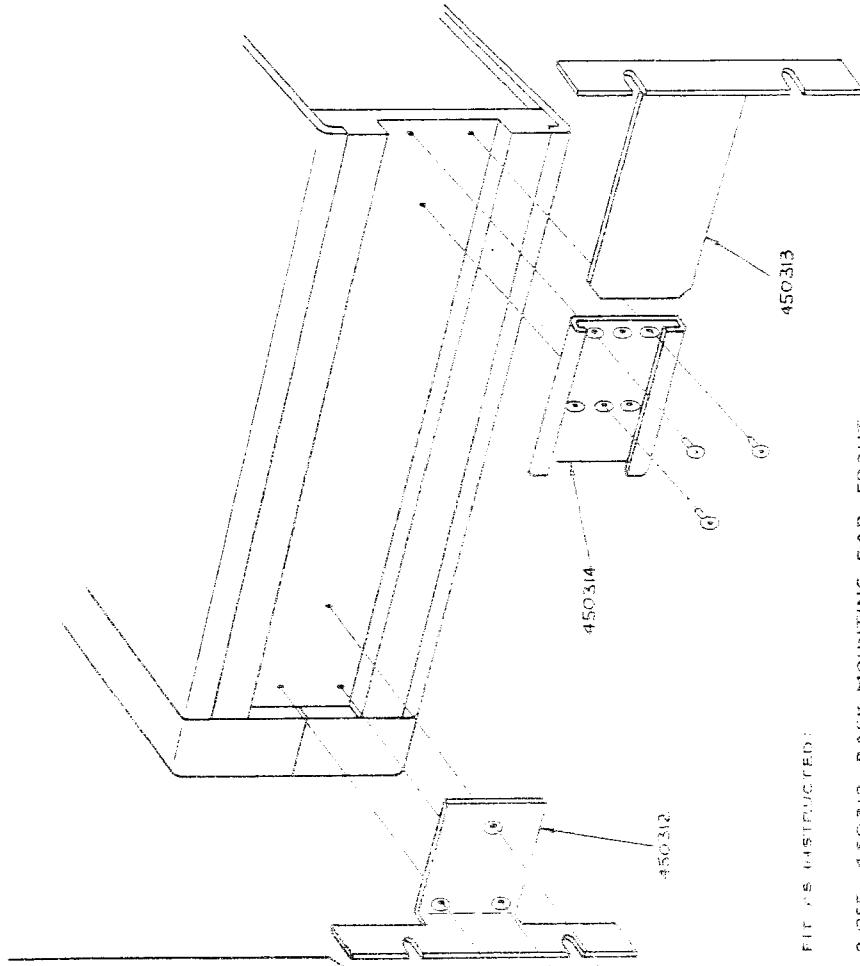
SLIDE P.C.B. FORWARD AND REMOVE FROM MAINS FILTER. INSERT SO THAT 120 IS VISIBLE AS ABOVE.



1

- REMOVE:
- 2 OFF 450300 REAR SPACERS.
 - 6 OFF 601038 M4x12mm SOCKET H.D. CSK SCREWS

OPTION 90 RACK MOUNTING
 KIT OF PARTS 440094



FIT AS INSTRUCTED:

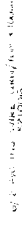
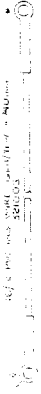
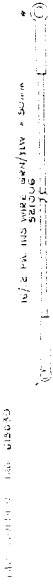
- 2 OFF 450312 RACK MOUNTING EAR FRONT
- 2 OFF 450313 RACK MOUNTING EAR REAR
- 2 OFF 450314 RACK MOUNTING SLIDE
- 12 OFF 611052 P.H.B. SOCKET H.D. CSK SCREWS

SUITABLE RACK DEPTHS

| RMT | DEPTH INCHES | NOTES |
|------------|--------------|---|
| 4535 | 4.25 | SHORTEN REAR RACK MOUNTING EARS. |
| 635 TO 735 | 25 TO 29 | FIT AS SHOWN BY DRAWING. |
| 735 TO 800 | 29 TO 31 1/2 | REVERSE RACK MOUNTING SLIDES TO EXTEND PAST REAR PANEL. |

OPTION FITTING INSTRUCTIONS

- Option 80: 115V 60Hz
- Option 90: Rack Mounting



DRIP WIRE END VIEW

REMOVE ALL SCREWS FROM SCREWS AND
 FROM BOTTOM SHEET FROM BOTTOM

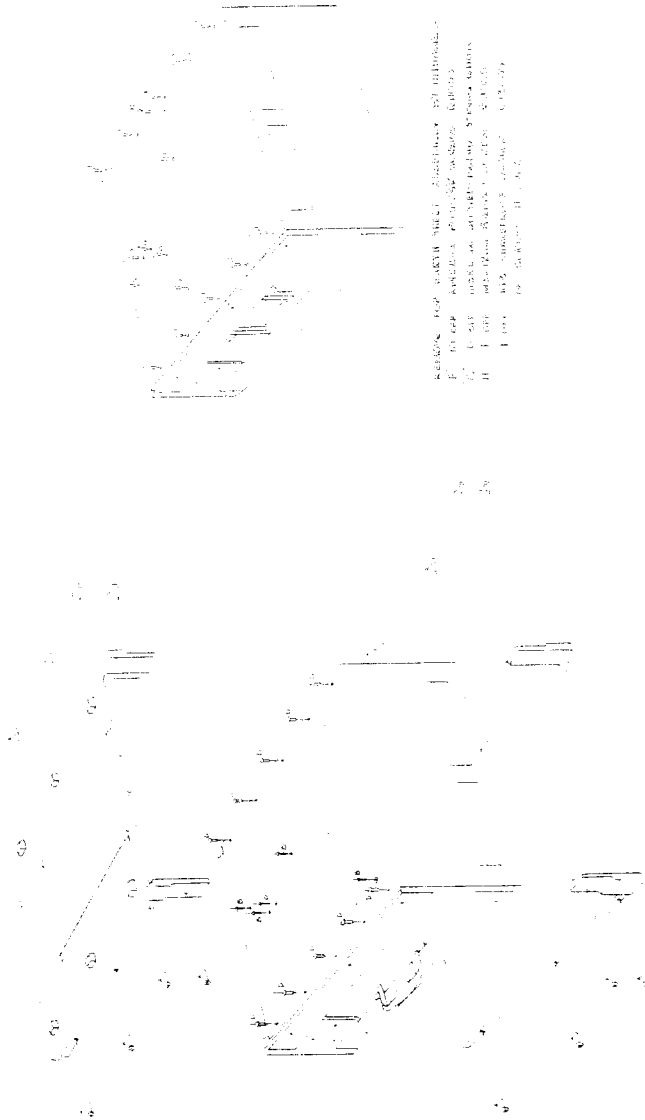
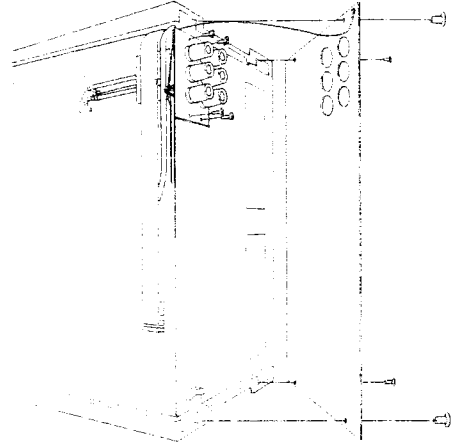
REMOVE ALL SCREWS FROM FRONT PANEL

REMOVE ALL SCREWS FROM FRONT PANEL
 FROM SCREWS FROM FRONT PANEL
 FROM SCREWS FROM FRONT PANEL
 FROM SCREWS FROM FRONT PANEL

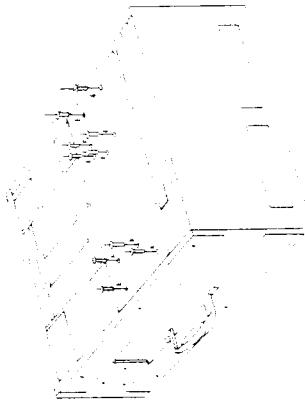
REMOVE ALL SCREWS FROM FRONT PANEL
 FROM SCREWS FROM FRONT PANEL
 FROM SCREWS FROM FRONT PANEL
 FROM SCREWS FROM FRONT PANEL

100mm diameter hole
 for 1/2 in. max. hole diameter
 on PN X on T44-4700 on
 scales to JE-4B on 4200

WITH CALCULATOR UPSIDE DOWN FACING FORWARD
 UNPLUG THE CABLES FROM TERMINALS
 TO THE CLOSURE ON THE MOTHER PCB. ALSO
 REMOVE THE 2 P CLIPS & FINISH SCREWS
 REMOVE THE FRONT PANEL FINISH SCREWS
 REMOVE TERMINAL PCB ASSY WITH ALL ITS WIRES
 REPLACE FRONT PANEL.



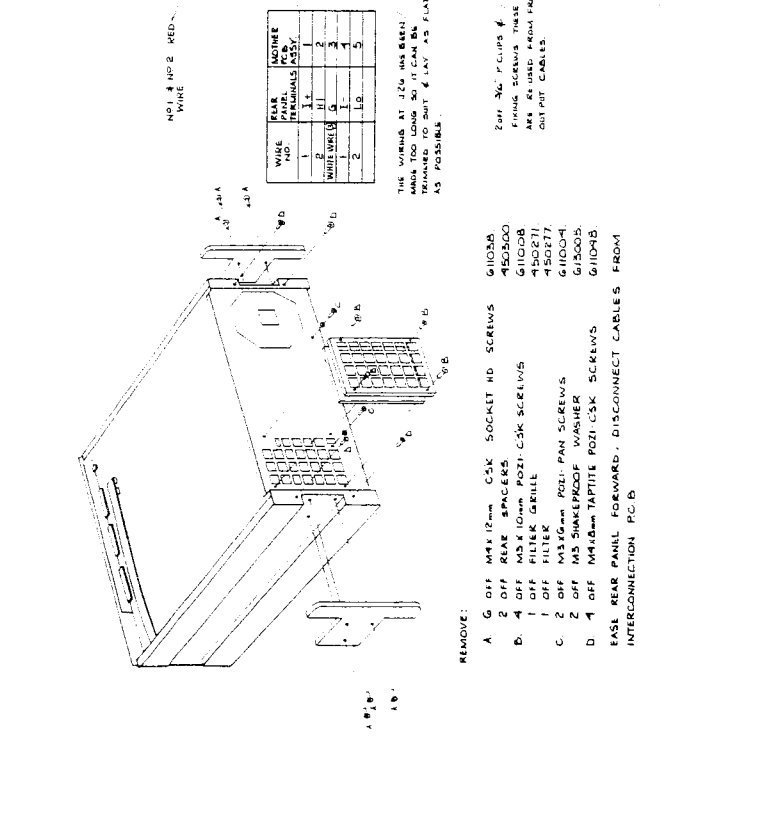
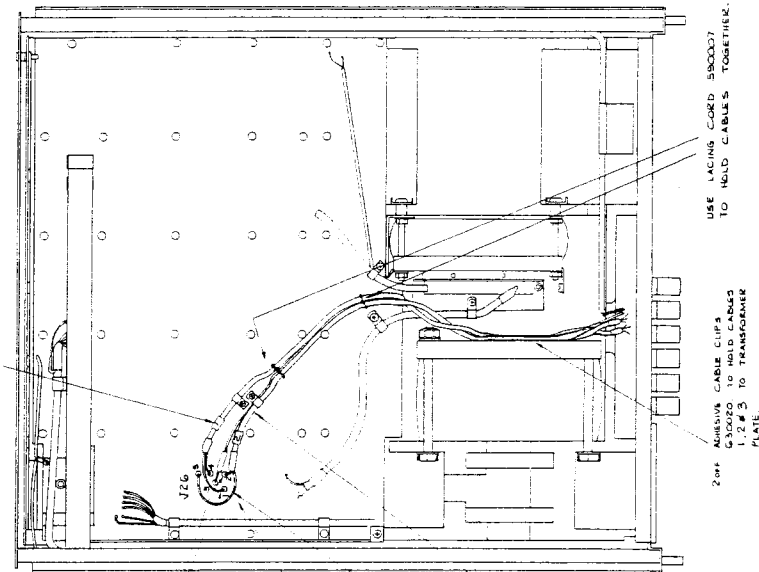
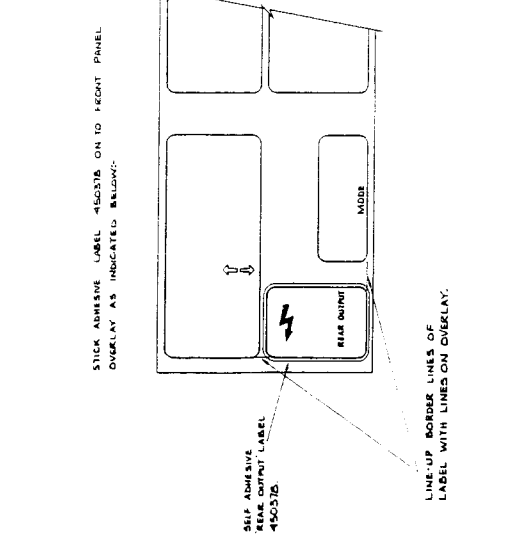
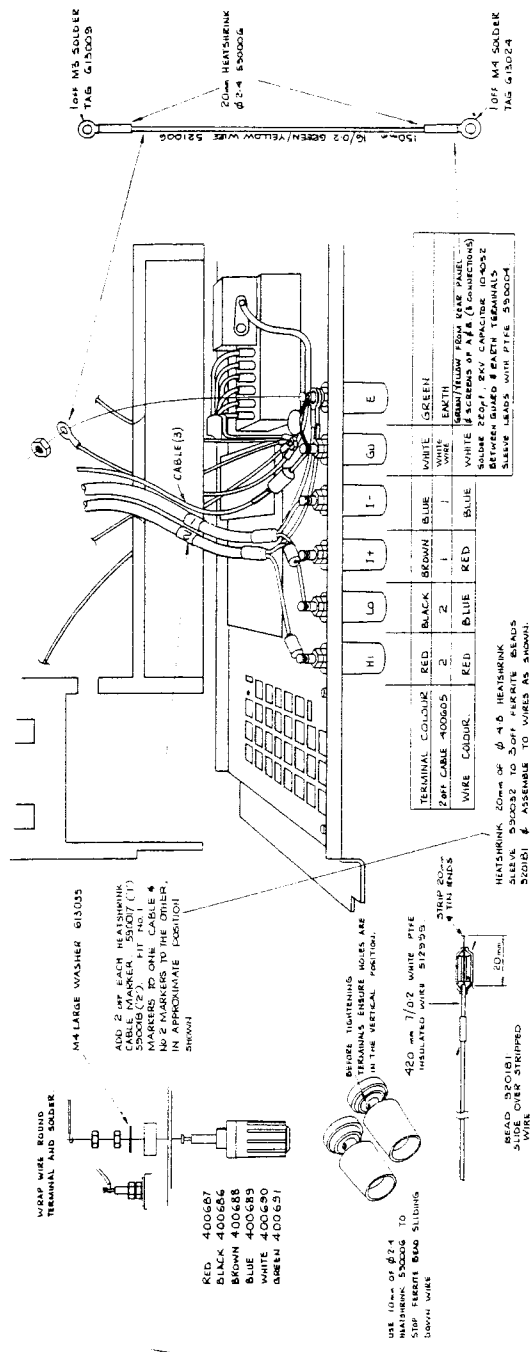
REMOVE TOP & BOTTOM COVERS BY REMOVING:
 A 10-011 10X12MM DIA. HEX. SCREWS - 4 UNITS
 REMOVE BOTTOM FRONT SHEET & THEN BOTTOM
 FRONT SHEET REMOVE FOLLOWING SCREWS FROM:
 B 5-001 10-011mm SLITTED TORX SCREWS - 10/10
 C 10-011 10-011mm TORX SCREWS - 10/10
 E 10-011 10-011mm TORX SCREWS - 10/10



OPTION FITTING INSTRUCTIONS

Option 42: Rear Output

Layout Drawing No. 480603-3.6 Sheet 4



WHEN THE REAR PANEL IS AWAY FROM THE CHASSIS REMOVE THE PUSH OUT PLUGS WHICH BLANK THE TERMINAL HOLES, AND FIT TERMINALS.

CONNECT REAR OUTPUT CABLES

FIT 150mm EARTH WIRE (SHOWN ABOVE) TO EARTH SCREW ON REAR PANEL M5 SOLDER TAG END.

PASS EARTH WIRE AROUND THE BACK OF, AND THEN INTO THE RECESS IN THE CHASSIS & CONNECT THE M4 SOLDER TAG OF EARTH WIRE TO THE EARTH TERMINAL.

SOLDER THE 220pf 2KV CAPACITOR 104032 BETWEEN GUARD & EARTH TERMINALS.

RECONNECT CABLES TO INTERCONNECTION PCB

EASE REAR PANEL BACK INTO PLACE.

REFIT REAR PANEL AS SHOWN IN PREVIOUS STEP.

SOLDER WHITE WIRE TO CLOVERLEAF

THEN SECURE WITH 7P CLIPS

TWIST CABLES 1 & 2 TOGETHER TWO COMPLETE TURNS

SOLDER WIRES FROM CABLES 1 & 2 TO CLOVERLEAF TERMINALS. TIE CABLES 1 & 2 TOGETHER USING 590007

SECURE CABLES 1, 2 & 3 TO THE TRANSFORMER PLATE USING CABLE CLIPS G30020. POSITION THE CLIPS PARALLEL TO THE EDGE OF THE TX PLATE AND AS CLOSE TO ITS CENTRE AS POSSIBLE, WITHOUT STRAINING THE CABLE

REPLACE GUARD SHIELDS & COVERS AS SHOWN IN PREVIOUS STEPS.

DIGITAL PCB ASSY
 ADJUST S2 TO SUIT
 OPTION MIX.

SWITCH POSITIONS

BLACK
 EJECTOR

1 2 3 4 5 6
 S2 ON OFF

AC 4 DC OPTIONS 4708.

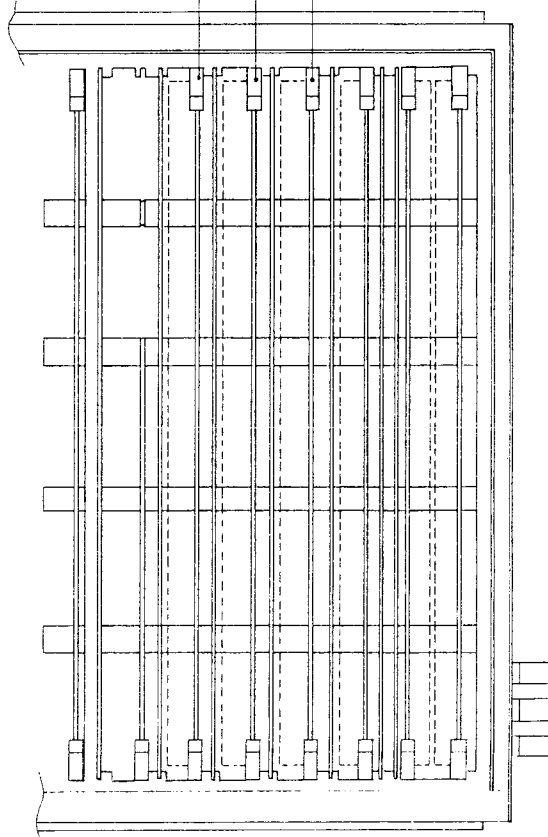
NOTE:
 CLEAN ALL PCB EDGE CONTACTS WITH CLEANING
 FLUID 900016 BOTH BEFORE INITIAL ASSEMBLY
 AND AT FINAL INSTRUMENT FINISHING.

4708

| OPTION MIX | S2 POSITIONS | | | | | |
|-----------------------|--------------|-----|-----|-----|-----|-----|
| | 1 | 2 | 3 | 4 | 5 | 6 |
| DCV | OFF | OFF | ON | ON | ON | OFF |
| ACV | OFF | OFF | ON | ON | OFF | ON |
| DCV, DCI, Ω | OFF | OFF | OFF | OFF | ON | OFF |
| ACV, RCI, Ω | OFF | OFF | OFF | OFF | OFF | ON |
| DCV, RCU | OFF | OFF | ON | ON | OFF | OFF |
| DCV, ACV, DCI, RCI, Ω | OFF | OFF | OFF | OFF | OFF | OFF |

4700, 4705, 4707

| OPTION MIX | S2 POSITIONS | | | | | |
|------------|--------------|-----|-----|-----|-----|-----|
| | 1 | 2 | 3 | 4 | 5 | 6 |
| I/R | OFF | ON | OFF | OFF | OFF | OFF |
| 1KV | OFF | OFF | ON | ON | OFF | OFF |
| I/J, 1KV | OFF | OFF | OFF | OFF | OFF | OFF |
| NO OPTIONS | OFF | ON | ON | ON | OFF | OFF |



AC OPTION 20
 400862 AC PCB ASSY

400860 SINE SOURCE
 PCB ASSY

DC OPTION 10
 REPLACE 400809 DIP
 CONTROL PCB ASSY
 WITH 400861 DC
 PCB ASSY.


OPTION FITTING INSTRUCTIONS

Option 10: DC Voltage
 Option 20: AC Voltage
 Digital Assembly: Switch Positions for Fitted Options
 Layout Drawing No. 480603-3.1 Sheet 7

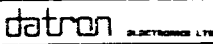
SECTION 12 4708 COMPONENT LISTS

Contents

| | |
|--|----------|
| Front Assembly | 400558 |
| Digital Assembly | 400796 |
| Analog Interface Assembly | 400648 |
| Reference Divider Assembly | 400652 |
| Reference Assembly | LP400761 |
| DC Assembly | 400536 |
| Output Control Assembly | LP400909 |
| Sine Source Assembly | 400446 |
| AC Assembly | 400844 |
| Current / Ohms Assembly | 400614 |
| Power Amplifier Assembly | 400618 |
| Out-guard Power Supply Assembly | 400561 |
| In-guard Power Supply Assembly | 400554 |
| ±38V Power Supply Assembly | 400653 |
| Power Amplifier Positive Heatsink Assembly | 400637 |
| Power Amplifier Negative Heatsink Assembly | 400539 |
| Power Supply / Current Heatsink Assembly | 400540 |
| High Voltage Assembly | 400537 |
| Constant Current Source Assembly | 400563 |
| Mains (Line) Transformer Assembly | 400541 |
| L.F. Transformer Assembly | 400651 |
| H.F. Transformer Assembly | 400578 |
| Mother Assembly | 400604 |
| Interconnection Assembly | 400830 |
| Terminal Board Assembly | 400640 |
| 4700 Instrument Assembly | LP400858 |
| Main Assembly | LP400859 |
| Chassis Assembly | LP400863 |
| Rear Panel Assembly | 400636 |
| Option Fitting Instructions | 400603 |

| | | | | | | |
|-----------------------------|----------------|---|--|--|-------------------------------|--|
| DRAWING No 400558 | | CHKD | 1.0 12/62 26.286/AR 1.1 25G 113.886/R 1.1 2386 12.2.87 1.1 275 129.2.87 | | | |
| REV. AM. | | DATE | | | | |
| | | ECO | | | | |
| | | REVISION | | | | |
| | | ISSUE | | | | |
| DESCR PTION | DRAWING NUMBER | SHEET NUMBER | ISSUE - REVISION | | | |
| COMPONENT LAYOUT | 480558 | 1 | 1.0 | 1.0 | | |
| SCHEMATIC | 430558 | 1 | 1.0 | 1.1 | | |
| SCHEMATIC | 430558 | 2 | 1.0 | 1.1 | | |
| FUNCTIONAL TEST PROC. | 460558/FT | 1-3 | 1.0 | 1.1 | | |
| FUNCT. TEST TICK LIST | 470558/FT | 1 | 1.0 | 1.1 | | |
| PCB | 410144 | 10-0 | | | | |
| NOTES | |  | | DRN <u>11</u> DATE 14. 8. 85 CHKD <u>R.K. COGGAN</u> DATE 3/3/85 APPD <u>[Signature]</u> RATE 33% | TITLE 4700 FRONT PCB ASSY. | DRAWING No 400558 SHEET 1 of 11 |

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No. USED Per Assy. |
|------------|-----------------|---------------------|------------------------|-------------------------|--------------------|
| R1 | 000334 | 330k 5% 1/4W CARBON | MULLARD | CR25 | 22 |
| R2 | 000334 | " " " " | " | " | - |
| R3 | 000334 | " " " " | " | " | - |
| R4 | 000334 | " " " " | " | " | - |
| R5 | 000334 | " " " " | " | " | - |
| R6 | 000334 | " " " " | " | " | - |
| R7 | 000334 | " " " " | " | " | - |
| R8 | 000334 | " " " " | " | " | - |
| R9 | 000334 | " " " " | " | " | - |
| R10 | 000334 | " " " " | " | " | - |
| R11 | 000334 | " " " " | " | " | - |
| R12 | 000334 | " " " " | " | " | - |
| R13 | 000334 | " " " " | " | " | - |
| R14 | 000334 | " " " " | " | " | - |
| R15 | 000334 | " " " " | " | " | - |
| R16 | 000334 | " " " " | " | " | - |
| R17 | 000334 | " " " " | " | " | - |
| R18 | 000334 | " " " " | " | " | - |
| R19 | 000334 | " " " " | " | " | - |
| R20 | 000334 | " " " " | " | " | - |
| R21 | 000334 | " " " " | " | " | - |
| R22 | 000334 | " " " " | " | " | - |
| R23 | 000102 | 1k " " " | " | " | 11 |

| | | | | | | | |
|------------------------------|-----|------|------|--|--|--|---|
| NOTES. | | | | | | DATE 7. 6. 85 |  ELECTRONICS LTD TITLE 4700 FRONT PCB. ASSY. |
| SEE SHEET 1 FOR LATEST ISSUE | | | | | | DRAWN <u>[Signature]</u> CHECKED APPROVED R.K. COGGAN DATE 18/6/85 | |
| NO. | ECO | DATE | CHKD | | | | SHEET 2 of 11 |

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No. USED Per Assy. |
|------------|-----------------|-------------------|------------------------|-------------------------|--------------------|
| R24 | 000102 | 1k 5% 1/3W CARBON | MULLARD | CR25 | - |
| R25 | 000102 | 1k " " " | " | " | - |
| R26 | 000104 | 100k " " " | " | " | 4 |
| R27 | 000102 | 1k " " " | " | " | - |
| R28 | 000102 | 1k " " " | " | " | - |
| R29 | 000102 | 1k " " " | " | " | - |
| R30 | 000102 | 1k " " " | " | " | - |
| R31 | 000102 | 1k " " " | " | " | - |
| R32 | 000102 | 1k " " " | " | " | - |
| R33 | 000102 | 1k " " " | " | " | - |
| R34 | 000102 | 1k " " " | " | " | - |
| R35 | 000103 | 10k " " " | " | " | 5 |
| R36 | 000103 | 10k " " " | " | " | - |
| R37 | 000103 | 10k " " " | " | " | - |
| R38 | 000103 | 10k " " " | " | " | - |
| R39 | 000472 | 4k7 " " " | " | " | 6 |
| R40 | 000680 | 68R " " " | " | " | 8 |
| R41 | 000680 | 68R " " " | " | " | - |
| R42 | 000680 | 68R " " " | " | " | - |
| R43 | 000272 | 2k7 " " " | " | " | 18 |
| R44 | 000272 | 2k7 " " " | " | " | - |
| R45 | 000472 | 4k7 " " " | " | " | - |
| R46 | 000272 | 2k7 " " " | " | " | - |

NOTES.

SEE SHEET 7 FOR LATEST ISSUE

| | | |
|----------|---|---|
| DATE | | datron ELECTRONICS LTD TITLE 4700 FRONT PCB. ASSY. DRAWING NUMBER 400558 SHEET 3 of 11 |
| DRAWN | L | |
| CHECKED | | |
| APPROVED | | |
| DATE | | |

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No. USED Per Assy. |
|------------|-----------------|--------------------|------------------------|-------------------------|--------------------|
| R47 | 000182 | 1k8 5% 1/3W CARBON | MULLARD | CR25 | 2 |
| R48 | 000272 | 2k7 " " " | " | " | - |
| R49 | 000272 | 2k7 " " " | " | " | - |
| R50 | 000222 | 2k2 " " " | " | " | 2 |
| R51 | 000222 | 2k2 " " " | " | " | - |
| R52 | 000272 | 2k7 " " " | " | " | - |
| R53 | 000272 | 2k7 " " " | " | " | - |
| R54 | 000472 | 4k7 " " " | " | " | - |
| R55 | 000272 | 2k7 " " " | " | " | - |
| R56 | 000272 | 2k7 " " " | " | " | - |
| R57 | 000272 | 2k7 " " " | " | " | - |
| R58 | 000182 | 1k8 " " " | " | " | - |
| R59 | 000272 | 2k7 " " " | " | " | - |
| R60 | 000272 | 2k7 " " " | " | " | - |
| R61 | 000272 | 2k7 " " " | " | " | - |
| R62 | 000272 | 2k7 " " " | " | " | - |
| R63 | 000272 | 2k7 " " " | " | " | - |
| R64 | 000272 | 2k7 " " " | " | " | - |
| R65 | 000272 | 2k7 " " " | " | " | - |
| R66 | 000272 | 2k7 " " " | " | " | - |
| R67 | 000680 | 68R " " " | " | " | - |
| R68 | 000680 | 68R " " " | " | " | - |
| R69 | 000680 | 68R " " " | " | " | - |

NOTES.

SEE SHEET 2 FOR LATEST ISSUE

| | | |
|----------|---|---|
| DATE | | datron ELECTRONICS LTD TITLE 4700 FRONT PCB. ASSY. DRAWING NUMBER 400558 SHEET 4 of 11 |
| DRAWN | L | |
| CHECKED | | |
| APPROVED | | |
| DATE | | |

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No. USED Per Assy. |
|---------------|-----------------|---|------------------------|-------------------------|--------------------|
| R70 | 000680 | 68R 5% 1/3W CARBON | MULLARD | CR25 | — |
| R71 | 000680 | 68R " " " | " | " | — |
| R72 | 000563 | 56k " " " | " | " | 1 |
| R73, R74, R75 | 000472 | 4k7 " " " | " | " | — |
| R76 | 000103 | 10k " " " | " | " | — |
| R77, R78, R79 | 000104 | 100k " " " | " | " | — |
| AN1, AN2 | 090017 | 100k x 7 2% NETWORK | BECKMAN | L08-1- R100k | 2 |
| AN3, AN4 | 090041 | 4k7 x 7 2% NETWORK | BECKMAN | L08-1- R4k7 | 2 |
| AN5, AN6 | 090121 | 100k x 8 2% NETWORK | BECKMAN | L09-1- R100k | 2 |
| C1 | 150002 | 10µF 20% 16V DIP TANT | UNION CARBIDE | K10E16 | 2 |
| C2 | 104026 | 47nF ⁺⁵⁰ / ₋₂₀ % 50V CER DISC | SIEMENS | B37449 | 3 |
| C3 | 104026 | 47nF ⁺⁵⁰ / ₋₂₀ % 50V CER DISC | SIEMENS | B37449 | — |
| C4 | 150001 | 22µF 20% 16V DIP TANT | UNION CARBIDE | K22E16 | 1 |
| C5 | 104026 | 47nF ⁺⁵⁰ / ₋₂₀ % 50V CER DISC | SIEMENS | B37449 | — |
| C6 | | NOT USED | | | — |
| C7 | | NOT USED | | | — |
| C8 | 110013 | 100nF 20% 250V POLYESTER | MULLARD | C280AEP100k | 19 |
| C9 | 110013 | " " " " " " | " | " | — |
| C10 | 110013 | " " " " " " | " | " | — |
| C11 | 110013 | " " " " " " | " | " | — |
| C12 | 110013 | " " " " " " | " | " | — |

NOTES:

SEE SHEET 2 FOR LATEST ISSUE

| | | |
|----------|--|---|
| DATE | | datron ELECTRONICS LTD TITLE 4700 FRONT PCB ASSY DRAWING NUMBER 400558 SHEET 5 OF 11 |
| DRAWN | | |
| CHECKED | | |
| APPROVED | | |
| DATE | | |

| IGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No. USED Per Assy. |
|---------|-----------------|--------------------------|------------------------|-------------------------|--------------------|
| | 110013 | 100nF 20% 250V POLYESTER | MULLARD | C280AEP100k | — |
| | 110013 | " " " " " " | " | " | — |
| | 110013 | " " " " " " | " | " | — |
| | 110013 | " " " " " " | " | " | — |
| | 110013 | " " " " " " | " | " | — |
| | 110013 | " " " " " " | " | " | — |
| | 110013 | " " " " " " | " | " | — |
| | 110013 | " " " " " " | " | " | — |
| | 110013 | " " " " " " | " | " | — |
| | 110013 | " " " " " " | " | " | — |
| | 110013 | " " " " " " | " | " | — |
| | 110013 | " " " " " " | " | " | — |
| | 110013 | " " " " " " | " | " | — |
| | 150002 | 10µF 20% 16V DIP TANT | UNION CARBIDE | K10E16 | — |
| | 150016 | 1µF 20% 35V DIP TANT | UNION CARBIDE | K10B35 | 1 |
| | 200001 | 75mA 75V GP. SI. DIODE | FAIRCHILD | 1N4148 | 18 |
| | 200001 | " " " " " " | " | " | — |
| | 200001 | " " " " " " | " | " | — |
| | 200001 | " " " " " " | " | " | — |
| | 200001 | " " " " " " | " | " | — |
| | 200001 | " " " " " " | " | " | — |
| | 200001 | " " " " " " | " | " | — |
| | 200001 | " " " " " " | " | " | — |

SHEET 2 FOR LATEST ISSUE

| | | |
|----------|--|---|
| DATE | | datron ELECTRONICS LTD TITLE 4700 FRONT PCB ASSY DRAWING NUMBER 400558 SHEET 6 OF 11 |
| DRAWN | | |
| CHECKED | | |
| APPROVED | | |
| DATE | | |

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No. USED Per Assy |
|------------|-----------------|----------------------|------------------------|-------------------------|-------------------|
| D8 | 200001 | 75mA 75V GP SI DIODE | FAIRCHILD | 1N4148 | — |
| D9 | 200001 | " " " " " | " | " | — |
| D10 | 200001 | " " " " " | " | " | — |
| D11 | 200001 | " " " " " | " | " | — |
| D12 | 200001 | " " " " " | " | " | — |
| D13 | 200001 | " " " " " | " | " | — |
| D14 | 200001 | " " " " " | " | " | — |
| D15 | 200001 | " " " " " | " | " | — |
| D16 | 200001 | " " " " " | " | " | — |
| D17 | 213005 | 75V 1/2W ZENER | MOTOROLA | BZX79C75 | 1 |
| D18 | 200001 | 75mA 75V GP SI DIODE | FAIRCHILD | 1N4148 | — |
| D19 | 200001 | 75mA 75V GP SI DIODE | FAIRCHILD | 1N4148 | — |
| D20 | 213006 | 5V1 5W ZENER | UNITRODE | TVS 505 | 1 |
| Q1 | | NOT USED | | | — |
| Q2 | 240009 | SI NPN TRANSISTOR | NATIONAL | MPSL01 / TO18 | 18 |
| Q3 | 240009 | " " " " | " | " | — |
| Q4 | 240009 | " " " " | " | " | — |
| Q5 | 240009 | " " " " | " | " | — |
| Q6 | 240009 | " " " " | " | " | — |
| Q7 | 240009 | " " " " | " | " | — |
| Q8 | 240009 | " " " " | " | " | — |

NOTES

SEE SHEET 2 FOR LATEST ISSUE

| | | |
|----------|--|---|
| DATE | | datron ELECTRONICS LTD TITLE 4700 FRONT PCB ASSY DRAWING NUMBER 400558 SHEET 7 OF 11 |
| DRAWN | | |
| CHECKED | | |
| APPROVED | | |
| DATE | | |

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No. USED Per Assy |
|------------|-----------------|-------------------|------------------------|-------------------------|-------------------|
| Q9 | 240009 | SI NPN TRANSISTOR | NATIONAL | MPSL01 / TO18 | — |
| Q10 | 250009 | SI PNP TRANSISTOR | NATIONAL | 2N5401 / TO18 | 11 |
| Q11 | 250009 | " " " " | " | " | — |
| Q12 | 250009 | " " " " | " | " | — |
| Q13 | 250009 | " " " " | " | " | — |
| Q14 | 250009 | " " " " | " | " | — |
| Q15 | 250009 | " " " " | " | " | — |
| Q16 | 250009 | " " " " | " | " | — |
| Q17 | 250009 | " " " " | " | " | — |
| Q18 | 250009 | " " " " | " | " | — |
| Q19 | 250009 | " " " " | " | " | — |
| Q20 | 250009 | " " " " | " | " | — |
| Q21 | 240025 | SI NPN TRANSISTOR | " | MPSA13 | 4 |
| Q22 | 240025 | " " " " | " | " | — |
| Q23 | 240025 | " " " " | " | " | — |
| Q24 | 240025 | " " " " | " | " | — |
| Q25 | 250011 | SI PNP TRANSISTOR | " | BC327 / TO18 | 8 |
| Q26 | 250011 | " " " " | " | " | — |
| Q27 | 250011 | " " " " | " | " | — |
| Q28 | 250011 | " " " " | " | " | — |
| Q29 | 250011 | " " " " | " | " | — |
| Q30 | 250011 | " " " " | " | " | — |
| Q31 | 250011 | " " " " | " | " | — |

NOTES

SEE SHEET 2 FOR LATEST ISSUE

| | | |
|----------|--|---|
| DATE | | datron ELECTRONICS LTD TITLE 4700 FRONT PCB ASSY DRAWING NUMBER 400558 SHEET 8 OF 11 |
| DRAWN | | |
| CHECKED | | |
| APPROVED | | |
| DATE | | |

| DESIGNATOR | DATRON PART No | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No | No. USED Per Assy |
|------------|----------------|----------------------------------|------------------------|------------------------|-------------------|
| Q32 | 250011 | SI PNP TRANSISTOR | NATIONAL | BC327/TO18 | - |
| Q33 | 240009 | SI NPN TRANSISTOR | " | MPSL01/TO18 | - |
| Q34 | 240009 | " " " | " | " | - |
| Q35 | 240009 | " " " | " | " | - |
| Q36 | 240009 | " " " | " | " | - |
| Q37 | 240009 | " " " | " | " | - |
| Q38 | 240009 | " " " | " | " | - |
| Q39 | 240009 | " " " | " | " | - |
| Q40 | 240009 | " " " | " | " | - |
| Q41 | 240009 | " " " | " | " | - |
| Q42 | 240009 | " " " | " | " | - |
| M1 | 280023 | QUAD 2-1/P NOR GATE | MOTOROLA | MC14001 BCP | 1 |
| M2 | 260005 | 5Y 1A REGULATOR | MOTOROLA | MC7805CP | 1 |
| M3 | 280043 | 4 BIT LATCH/4 TO 16 LINE DECODER | MOTOROLA | MC14515 BCP | 1 |
| M4 | 280090 | DUAL BINARY 1 of 4 DECODER | MOTOROLA | MC14555 BCP | 1 |
| M5 | 270071 | DUAL 1 of 4 DECODER LS | NATIONAL | DM74LS156N | 1 |
| M6 | 280103 | PROGRAMMABLE KEYBOARD/DSF | INTEL | 8279-S | 1 |

NOTES.

SEE SHEET 2 FOR LATEST ISSUE

| REV | DATE | BY | CHKD |
|-----|------|----|------|
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |

| | |
|----------|---|
| DATE | datron ELECTRONICS LTD TITLE: 4700 FRONT PCB. ASSY |
| DRAWN | |
| CHECKED | DRAWING NUMBER: 400558 SHEET 9 OF 11 |
| APPROVED | |
| DATE | |

| DESIGNATOR | DATRON PART No | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No | No. USED Per Assy |
|---------------|----------------|--|------------------------|------------------------|-------------------|
| S1-S27 | 700079 | KEYBOARD x 1/2 SWITCH . BLACK | NSF | K12/HALF KEY. BLACK | 28 |
| S29-S43 | 700061 | KEYBOARD SWITCH RED LED. | SCHADOW | SRL-RED LED | 25 |
| S23, S44, S45 | 700062 | KEYBOARD SWITCH GREEN LED | SCHADOW | SRL-GREEN LED | 3 |
| S46-S55 | 700061 | KEYBOARD SWITCH . RED LED | SCHADOW | SRL-RED LED | - |
| S56 | 700079 | KEYBOARD x 1/2 SWITCH . BLACK | NSF | K12/HALF KEY. BLACK | - |
| | 410144-10 | PCB | | | 1 |
| J1 | 604060 | 24+24 WAY .1" PCB. PLUG GOLD | AMP | 2-825440-4 | 3 |
| | 605098 | 40 PIN DIL. LOW PROFILE SKT. | CAMBION | 703-4340-01-06-00 | 1 |
| | 605060 | 14 WAY DIL. " " " | | | 1 |
| | 605061 | 16 WAY DIL. " " " | | | 2 |
| | 605097 | 24 WAY DIL. " " " | CAMBION | 703-4324-01-06-00 | 1 |
| | 612023 | STANDOFF M2.5 x #16. BRASS 1/8" x 1/4" | CAMBION | 350-5181-22-07 | 2 |
| | 800017-3 | 8 1/2 DIGIT DISPLAY WITH LEGEND | DALE | SEE DRG | 2 |
| | 920096 | BUZZER PIEZOELECTRIC | TOKO | PB 2720 | 1 |
| | 620003 | SOLDER PCB TERMINAL LUG | HARWIN | H2105A | 2 |

NOTES.

SEE SHEET 2 FOR LATEST ISSUE

| REV | DATE | BY | CHKD |
|-----|------|----|------|
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |

| | |
|----------|---|
| DATE | datron ELECTRONICS LTD TITLE: 4700 FRONT PCB. ASSY |
| DRAWN | |
| CHECKED | DRAWING NUMBER: 400558 SHEET 10 OF 11 |
| APPROVED | |
| DATE | |

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No. USED Per Assy. |
|------------|-----------------|--------------------------------|------------------------|-------------------------|--------------------|
| | 611054 | M2x6mm SLOT CSK STEEL | ZN PL | | 2 |
| | 611076 | M3x6mm SLOT PAN HEAD. | ZN PL | | 1 |
| | 613005 | M3 INT. SHAKEPROOF | | | 1 |
| | 613026 | M2 WASHER STEEL ZN PL | | | 2 |
| | 613027 | M2 INT SHAKEPROOF | | | 2 |
| | 615002 | M3 FULL NUT STEEL ZN PL | | | 1 |
| | 615016 | M2 FULL NUT STEEL ZN PL | | | 2 |
| | 620007 | TEST POINT TERMINAL | MICROVAR | C 30 | 9 |
| | 630029 | TAPE DOUBLE SIDED 1/4" x 1/32" | 3M | 4032 | 150mm |
| | 630242 | GLASS BEAD 2.4% x 0.8% x 1.8 | MANSOL (PREFORMS) | M5363B/3 | 6 |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |

| | | |
|------------------------------|----------|------------------------|
| NOTES. | DATE | DATRON ELECTRONICS LTD |
| SEE SHEET 2 FOR LATEST ISSUE | DRAWN JL | TITLE |
| | CHECKED | 4700 |
| | APPROVED | FRONT PCB ASSY |
| | DATE | DRAWING NUMBER |
| | | 400558 |
| | | SHEET 11 OF 11 |

| | | |
|-----------------------|-------------------|----------------|
| DRAWING No. 400796 | CHKD | 25 NOV 87 |
| DI WM | DATE | 25 NOV 87 |
| | ECC | 2858 @ 6.88 14 |
| | REVISION ISSUE | 1.0 |

| DESCRIPTION | DRAWING NUMBER | SHEET NUMBER | ISSUE / REVISION |
|-----------------------|----------------|--------------|------------------|
| COMPONENT LAYOUT | 480796 | 1 | A 1.0 |
| SCHEMATIC | 430796 | 1 | A 1.0 |
| SCHEMATIC | 430796 | 2 | A 1.0 |
| SCHEMATIC | 430796 | 3 | A 1.0 |
| SCHEMATIC | 430796 | 4 | A 1.0 |
| SCHEMATIC | 430796 | 5 | A 1.0 |
| FUNCTIONAL TEST PROC. | 460796/FT | 1-7 | N/R |
| FUNC. TEST TICK LIST | 470796/FT | 1 | N/R |
| PCB | 410248 | 1 | 3 4 |

| | | | | | | | |
|-------|---|---|---------------------------|------------------|-------------------------------|--|--|
| NOTES | <input type="checkbox"/> DENOTES NO CHANGE TO DOCS AT ISSUE LEVEL CHANGE N/R = NOT RELEASED. | datron ELECTRONICS LTD BORWICH ENGLAND | CHKD DATE 25 NOV 87 | DATE 7 JAN 88 | APPROVED DATE 25 NOV 87 | TITLE CALIBRATOR DIGITAL PCB ASSY. | DRAWING No. 400796 SHEET 1 of 12 |
|-------|---|---|---------------------------|------------------|-------------------------------|--|--|

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No. USED per Assy. |
|------------|-----------------|-----------------------|------------------------|-------------------------|--------------------|
| R1 | | NOT USED | | | |
| R2 | 000472 | 4k7 5% 1/4W C/P RES | MULLARD | CR25 | 11 |
| R3 | 000472 | 4k7 " " " | " | " | - |
| R4 | 000472 | 4k7 " " " | " | " | - |
| R5 | 000472 | 4k7 " " " | " | " | - |
| R6 | 000103 | 10k " " " | " | " | 5 |
| R7 | 000104 | 100k " " " | " | " | 9 |
| R8 | 000122 | 1k2 " " " | " | " | 2 |
| R9 | 000104 | 100k " " " | " | " | - |
| R10 | 000104 | 100k " " " | " | " | - |
| R11 | 000103 | 10k " " " | " | " | - |
| R12 | 000472 | 4k7 " " " | " | " | - |
| R13 | 000472 | 4k7 " " " | " | " | - |
| R14 | 000561 | 560R " " " | " | " | 2 |
| R15 | 000104 | 100k " " " | " | " | - |
| R16 | 000182 | 1k8 " " " | " | " | 1 |
| R17 | 014751 | 4k75 1% 1/8W 50ppm MF | HOLCO | H8C | 1 |
| R18 | 000122 | 1k2 5% 1/4W CARBON | MULLARD | CR25 | - |
| R19 | 012491 | 2k49 1% 1/8W 50ppm MF | HOLCO | H8C | 1 |
| R20 | 000102 | 1k 5% 1/4W CARBON | MULLARD | CR25 | 22 |
| R21 | 000472 | 4k7 " " " | " | " | - |
| R22 | 000223 | 22k " " " | " | " | 1 |
| R23 | 000103 | 10k " " " | " | " | - |

| | | | |
|--------|------------------------------|----------|-------------------------------|
| NOTES: | SEE SHEET 1 FOR LATEST ISSUE | DATE | datron ELECTRONICS LTD |
| CHKD | | DRAWN | TITLE |
| DATE | | CHECKED | CALIBRATOR |
| CHKD | | APPROVED | DIGITAL PCB ASSY |
| DATE | | DATE | DRAWING NUMBER |
| | | | 400796 |
| | | | SHEET 2 of 12 |

| DESIGNATOR | DATRON PART No | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No | No. USED Per Assy |
|------------|----------------|-----------------------|------------------------|------------------------|-------------------|
| R24 | 000332 | 3k3 5% 1/4W CARBON | MULLARD | CR25 | 2 |
| R25 | 011002 | 10k0 1% 1/8W 50ppm MF | HOLCO | H8C | 2 |
| R26 | 000104 | 100k 5% 1/4W CARBON | MULLARD | CR25 | — |
| R27 | 011002 | 10k0 1% 1/8W 50ppm MF | HOLCO | H8C | — |
| R28 | 000471 | 470R 5% 1/4W CARBON | MULLARD | CR25 | 3 |
| R29 | 000104 | 100k " " " | " | " | — |
| R30 | 000472 | 4k7 " " " | " | " | — |
| R31 | 000102 | 1k " " " | " | " | — |
| R32 | 000104 | 100k " " " | " | " | — |
| R33 | 000102 | 1k " " " | " | " | — |
| R34 | 000102 | 1k " " " | " | " | — |
| R35 | 000102 | 1k " " " | " | " | — |
| R36 | 000102 | 1k " " " | " | " | — |
| R37 | 000102 | 1k " " " | " | " | — |
| R38 | 000102 | 1k " " " | " | " | — |
| R39 | 000102 | 1k " " " | " | " | — |
| R40 | 000102 | 1k " " " | " | " | — |
| R41 | 000102 | 1k " " " | " | " | — |
| R42 | 000103 | 10k " " " | " | " | — |
| R43 | 000102 | 1k " " " | " | " | — |
| R44 | 000102 | 1k " " " | " | " | — |
| R45 | 000102 | 1k " " " | " | " | — |
| R46 | 000102 | 1k " " " | " | " | — |

NOTES

USE SHEET 2 FOR LATEST ISSUE

| | |
|----------|--|
| DATE | |
| DRAWN | |
| CHECKED | |
| APPROVED | |
| DATE | |

datron ELECTRONICS LTD
 TITLE: **CALIBRATOR DIGITAL PCB ASSY**
 DRAWING NUMBER: **400796** SHEET **3** OF **12**

| DESIGNATOR | DATRON PART No | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No | No. USED Per Assy |
|------------|----------------|-------------------|------------------------|------------------------|-------------------|
| R47 | 000102 | 1k 5% 1/4W CARBON | MULLARD | CR25 | — |
| R48 | 000102 | 1k " " " | " | " | — |
| R49 | 000102 | 1k " " " | " | " | — |
| R50 | 000102 | 1k " " " | " | " | — |
| R51 | 000102 | 1k " " " | " | " | — |
| R52 | 000472 | 4k7 " " " | " | " | — |
| R53 | 000104 | 100k " " " | " | " | — |
| R54 | 000104 | 100k " " " | " | " | — |
| R55 | 000103 | 10k " " " | " | " | — |
| R56 | 000471 | 470R " " " | " | " | — |
| R57 | 000471 | 470R " " " | " | " | — |
| R58 | 000102 | 1k " " " | " | " | — |
| R59 | 000391 | 390R " " " | " | " | 1 |
| R60 | 000472 | 4k7 " " " | " | " | — |
| R61 | 000472 | 4k7 " " " | " | " | — |
| R62 | 000561 | 560R " " " | " | " | — |
| R63 | | NOT USED | | | — |
| R64 | 000332 | 3k3 " " " | " | " | — |
| R65 | 000102 | 1k " " " | " | " | — |
| R66 | 000222 | 2k2 " " " | " | " | 3 |
| R67 | 000222 | 2k2 " " " | " | " | — |
| R68 | 000222 | 2k2 " " " | " | " | — |

NOTES

USE SHEET 2 FOR LATEST ISSUE

| | |
|----------|--|
| DATE | |
| DRAWN | |
| CHECKED | |
| APPROVED | |
| DATE | |

datron ELECTRONICS LTD
 TITLE: **CALIBRATOR DIGITAL PCB ASSY**
 DRAWING NUMBER: **400796** SHEET **4** OF **12**

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No. USED Per Assy. |
|------------|-----------------|-----------------------|------------------------|-------------------------|--------------------|
| AN1 | | NOT USED | | | - |
| AN2 | 090017 | 100k x7 2% NETWORK | BECKMAN | 764-1-R100k | 1 |
| AN3 | 090046 | 10k x7 2% NETWORK | BECKMAN | 764-1-R10k | 2 |
| AN4 | 090046 | 10k x7 2% NETWORK | BECKMAN | 764-1-R10k | - |
| AN5 | 090085 | 12k x8 2% NETWORK | AB | 761-3-12k | 1 |
| AN6 | 090177 | 3k3 x8 2% NETWORK | AB | 870-91-3k3 | 1 |
| C1 | 150002 | 10uF 20% 16V DIP TANT | UNION CARBIDE | K10E16 | 11 |
| C2 | 150002 | 10uF 20% 16V DIP TANT | UNION CARBIDE | K10E16 | - |

NOTES

SEE SHEET 2 FOR LATEST ISSUE

| | | | | | | | | | | | | | | | |
|------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ISS | | | | | | | | | | | | | | | |
| ECN | | | | | | | | | | | | | | | |
| DATE | | | | | | | | | | | | | | | |
| CHG | | | | | | | | | | | | | | | |

| | | |
|----------|----|---|
| DATE | | datron <small>ELECTRONICS LTD</small> TITLE CALIBRATOR DIGITAL PCB ASSY |
| DRAWN | 11 | |
| CHECKED | | |
| APPROVED | | |
| DATE | | DRAWING NUMBER 400796 SHEET 5 OF 12 |

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No. USED Per Assy. |
|------------|-----------------|---|------------------------|-------------------------|--------------------|
| C3 | 104026 | 47nF ^{+50%} / _{-20%} 50V CER DISC | SIEMENS | B37449 | 14 |
| C4 | 104026 | 47nF ^{+50%} / _{-20%} 50V CER DISC | SIEMENS | B37449 | - |
| C5 | 104026 | 47nF ^{+50%} / _{-20%} 50V CER DISC | SIEMENS | B37449 | - |
| C6 | 104026 | 47nF ^{+50%} / _{-20%} 50V CER DISC | SIEMENS | B37449 | - |
| C7 | 102681 | 680pF 10% 500V CER DISC | ITT | CD10 | 1 |
| C8 | 150016 | 1uF 20% 35V DIP TANT | UNION CARBIDE | K1R035 | 3 |
| C9 | 104026 | 47nF ^{+50%} / _{-20%} 50V CER DISC | SIEMENS | B37449 | - |
| C10 | 150002 | 10uF 20% 16V DIP TANT | UNION CARBIDE | K10E16 | - |
| C11 | 104026 | 47nF ^{+50%} / _{-20%} 50V CER DISC | SIEMENS | B37449 | - |
| C12 | 150002 | 10uF 20% 16V DIP TANT | UNION CARBIDE | K10E16 | - |
| C13 | 150002 | 10uF 20% 16V DIP TANT | UNION CARBIDE | K10E16 | - |
| C14 | 104026 | 47nF ^{+50%} / _{-20%} 50V CER DISC | SIEMENS | B37449 | - |
| C15 | 150002 | 10uF 20% 16V DIP TANT | UNION CARBIDE | K10E16 | - |
| C16 | 102102 | 1nF 10% 500V CER DISC | ITT | CD10 | 1 |
| C17 | 150002 | 10uF 20% 16V DIP TANT | UNION CARBIDE | K10E16 | - |
| C18 | 150016 | 1uF 20% 35V DIP TANT | UNION CARBIDE | K1R035 | - |
| C19 | 104026 | 47nF ^{+50%} / _{-20%} 50V CER DISC | SIEMENS | B37449 | - |
| C20 | 104026 | 47nF ^{+50%} / _{-20%} 50V CER DISC | SIEMENS | B37449 | - |
| C21 | 150002 | 10uF 20% 16V DIP TANT | UNION CARBIDE | K10E16 | - |
| C22 | 104026 | 47nF ^{+50%} / _{-20%} 50V CER DISC | SIEMENS | B37449 | - |
| C23 | 104026 | 47nF ^{+50%} / _{-20%} 50V CER DISC | SIEMENS | B37449 | - |
| C24 | 150002 | 10uF 20% 16V DIP TANT | UNION CARBIDE | K10E16 | - |
| C25 | 104026 | 47nF ^{+50%} / _{-20%} 50V CER DISC | SIEMENS | B37449 | - |

NOTES

SEE SHEET 2 FOR LATEST ISSUE

| | | | | | | | | | | | | | | | |
|------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ISS | | | | | | | | | | | | | | | |
| ECN | | | | | | | | | | | | | | | |
| DATE | | | | | | | | | | | | | | | |
| CHG | | | | | | | | | | | | | | | |

| | | |
|----------|----|---|
| DATE | | datron <small>ELECTRONICS LTD</small> TITLE CALIBRATOR DIGITAL PCB ASSY |
| DRAWN | 11 | |
| CHECKED | | |
| APPROVED | | |
| DATE | | DRAWING NUMBER 400796 SHEET 6 OF 12 |

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No. USED Per Assy |
|------------|-----------------|------------------------------|------------------------|-------------------------|-------------------|
| C26 | 101103 | 10nF 25% 250V CER DISC | ITT | CD10 | 3 |
| C27 | 104026 | 47nF $\pm 50\%$ 50V CER DISC | SIEMENS | B37449 | - |
| C28 | 150006 | 1uF 20% 16V DIP TANT | UNION CARBIDE | K47E16 | 1 |
| C29 | 150016 | 1uF 20% 35V DIP TANT | UNION CARBIDE | K10R35 | - |
| C30 | 150024 | 17uF 20% 16V DIP TANT | UNION CARBIDE | K47E16 | 1 |
| C31 | 101103 | 10nF 25% 250V CER DISC | ITT | CD10 | - |
| C32 | 104026 | 47nF $\pm 50\%$ 50V CER DISC | SIEMENS | B37449 | - |
| C33 | 150002 | 10uF 20% 16V DIP TANT | UNION CARBIDE | K10E16 | - |
| C34 | 150002 | 10uF 20% 16V DIP TANT | UNION CARBIDE | K10E16 | - |
| C35 | 101103 | 10nF 25% 250V CER DISC | ITT | CD10 | - |
| C36 | 100560 | 56pF 2% 100V CER PLATE | PHILIPS/MULLARD | 2222 683 34509 | 1 |
| D1 | 200001 | 75mA 75V GP Si DIODE | FAIRCHILD | IN4148 | 6 |
| D2 | 200001 | 75mA 75V GP Si DIODE | FAIRCHILD | IN4148 | - |
| D3 | 200001 | 75mA 75V GP Si DIODE | FAIRCHILD | IN4148 | - |
| D4 | 200001 | 75mA 75V GP Si DIODE | FAIRCHILD | IN4148 | - |
| D5 | 210047 | 4V7 400mw ZENER | MULLARD | BZY88C4V7 | 1 |
| D6 | 214012 | 2V45 30ppm ZENER | FERRANTI | ZN458 | 1 |
| D7 | 220010 | Si HOT CARRIER DIODE | H.P. | HSCH1001/IN6263 | 1 |
| D8 | 200001 | 75mA 75V GP Si DIODE | FAIRCHILD | IN4148 | - |
| D9 | 200001 | 75mA 75V GP Si DIODE | FAIRCHILD | IN4148 | - |

NOTES:

SEE SHEET 2 FOR LATEST ISSUE

| | | |
|----------|--|---|
| DATE | | datron ELECTRONICS LTD CALIBRATOR DIGITAL PCB ASSY |
| DRAWN | | |
| CHECKED | | |
| APPROVED | | |
| DATE | | DRAWING NUMBER 400796 SHEET 7 OF 12 |

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No. USED Per Assy |
|------------|-----------------|-------------------|------------------------|-------------------------|-------------------|
| D10 | 213006 | 5V SW ZENER | UNITRODE | TVS 505 | 1 |
| Q1 | 240001 | Si NPN TRANSISTOR | NATIONAL | BC184/TO18 | 2 |
| Q2 | 240001 | Si NPN TRANSISTOR | NATIONAL | BC184/TO18 | - |
| Q3 | 230031 | N-CHAN DUAL JFET | TELEDYNE | SU2656M | 1 |

NOTES:

SEE SHEET 2 FOR LATEST ISSUE

| | | |
|----------|--|---|
| DATE | | datron ELECTRONICS LTD CALIBRATOR DIGITAL PCB ASSY |
| DRAWN | | |
| CHECKED | | |
| APPROVED | | |
| DATE | | DRAWING NUMBER 400796 SHEET 8 OF 12 |

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No. USED Per Qty |
|------------|-----------------|-------------------------------|------------------------|-------------------------|------------------|
| M47 | 280024 | TRI-STATE HEX NON-INV BUFFER | MOTOROLA | MC14503 BCP | - |
| M48 | 280086 | BI-DIRECTIONAL BUS TRANSDUCER | MOTOROLA | MC3447 | - |
| M49 | 270048 | QUAD 2 I/P NAND LS | NATIONAL | DM74LS00N | - |
| M50 | 270050 | HEX. INVERTER | NATIONAL | 74LS04 | - |
| M51 | 270058 | DUAL 2 TO 4 LINE DEMUX. LS | NATIONAL | DM74LS155N | 2 |
| M52 | 270058 | DUAL 2 TO 4 LINE DEMUX. LS | NATIONAL | DM74LS155N | - |
| M53 | 280068 | DUAL PRECISION MONOSTABLE | MOTOROLA | MC14538 BCP | 1 |
| | 605059 | 8 WAY DIL SOCKET | | | 1 |
| | 410248-4 | PCB | | | 1 |
| | 605050 | 40 WAY DIL LOW PROFILE SKT. | | | 3 |
| | 605060 | 14 WAY DIL SOCKET | | | 14 |
| | 605061 | 16 WAY DIL SOCKET | | | 17 |
| | 605064 | 24 WAY DIL SOCKET | | | 6 |
| | 605066 | 6 WAY DIL SOCKET | | | 2 |
| | 620003 | SOLDER PCB TERMINAL LUG | HARWIN | H210SA | 1 |
| | 630098 | COMPONENT CLIP | RICHCO | KKU-8 | 1 |
| | 630112 | CIRCUIT BOARD EJECTOR | RICHCO | CBE BLACK | 2 |
| S1 | 700065 | SWITCH IPIW MOMENT. | LIPA + ISOSTAT | 532 000 007 | 1 |
| TP's | 620007 | TEST POINT TERMINAL | MICROVAR | C30 | 2 |

NOTES:

SEE SHEET 2 FOR LATEST ISSUE

| REV | DATE | DESCRIPTION | DATE | DESCRIPTION |
|-----|------|-------------|------|-------------|
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |

| | | |
|----------|-------------------------------|----------------|
| DATE | datron ELECTRONICS LTD | |
| DRAWN | TITLE: CALIBRATOR | |
| CHECKED | DIGITAL PCB ASSY | |
| APPROVED | DRAWING NUMBER: 400796 | SHEET 11 OF 12 |
| DATE | | |

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No. USED Per Qty |
|------------|-----------------|------------------------------------|------------------------|-------------------------|------------------|
| | 618004 | MOUNTING PAD TOIS | JERMYN | 7018-0080 | 1 |
| | 605065 | 28 WAY DIL SOCKET | | | 2 |
| | 630024 | STEATITE BEAD 1G SWG | PARK ROIAL PORCELAIN | No 2 | 2 |
| | 630243 | GLASS BEAD 2.4 o/d x 0.8 I/D x 1.8 | MANSOL (PREFORMS) LTD | M5363B/B | 28 |
| | 605070 | 20 WAY DIL SOCKET | | | 2 |
| S2 | 700114 | SWITCH 6X I/P DIL | A. B. | 206-006ST | 1 |

NOTES:

SEE SHEET 2 FOR LATEST ISSUE

| REV | DATE | DESCRIPTION | DATE | DESCRIPTION |
|-----|------|-------------|------|-------------|
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |

| | | |
|----------|-------------------------------|----------------|
| DATE | datron ELECTRONICS LTD | |
| DRAWN | TITLE: CALIBRATOR | |
| CHECKED | DIGITAL PCB ASSY | |
| APPROVED | DRAWING NUMBER: 400796 | SHEET 12 OF 12 |
| DATE | | |

| DRAWING No. 400648 | | CHKD WJE | DATE 4.3.86 | ECD | REVISION | ISSUE | | |
|---|-------------------|--|-----------------------|------------------------|---------------------|--------------------|------------------------|-----------------------|
| DWG. No. DIWM | | DATE 8.4.86 | ECD WJE | REVISION 1.1 | ISSUE 1.1 | | | |
| DATE 21.4.86 | ECD WJE | REVISION 1.2 | ISSUE 1.2 | | | | | |
| DATE 2.2.87 | ECD WJE | REVISION 1.3 | ISSUE 1.3 | | | | | |
| DATE 19.8.87 | ECD WJE | REVISION 1.4 | ISSUE 1.4 | | | | | |
| DATE 29.1.99 | ECD WJE | REVISION 1.5 | ISSUE 1.5 | | | | | |
| DATE 6.10.88 | ECD WJE | REVISION A | ISSUE A | | | | | |
| DESCRIPTION | DRAWING NUMBER | SHEET NUMBER | ISSUE - REVISION | | | | | |
| COMP. LAYOUT. | 480648 | 1 | 1.0 | 1.1 | 1.1 | 1.1 | 1.1 | 1.1 |
| SCHEMATIC | 430648 | 1 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 |
| SCHEMATIC | 430648 | 2 | 1.0 | 1.0 | 1.1 | 1.1 | 1.1 | 1.1 |
| SCHEMATIC | 430648 | 3 | 1.0 | 1.0 | 1.1 | 1.1 | 1.1 | 1.1 |
| SCHEMATIC | 430648 | 4 | 1.0 | 1.0 | 1.1 | 1.1 | 1.1 | 1.1 |
| FUNCTIONAL TEST PROC. | 460648/FT | | 1.0 | | | | | |
| FUNCT. TEST TICK LIST | 470648/FT | 1 | 1.0 | | | 1.1 | 1.1 | 1.2 |
| PCB | 410264 | 1 | 1.0 | | | | | |
| NOTES <input type="checkbox"/> INDICATES NO CHANGE TO DOCS AT ISSUE LEVEL CHANGE | | datron INSTRUMENTS NORWICH ENGLAND | | DRN B. JACKSON | CHKD R. COGGAN | APPD WJE | TITLE 4700 | DRAWING No. 400648 |
| | | | | DATE 9/1/86 | DATE 10/3/86 | DATE 11.7.86 | ANALOG. INTERFACE ASSY | SHEET 1 OF 9 |

| DESIGNATOR | DATRON PART No | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No | No. USED Per Assy. |
|------------|----------------|-----------------------|------------------------|------------------------|--------------------|
| R1 | 008031 | 100R 5% 1.6 W MF | MULLARD | PR37 | 2 |
| R2 | 000472 | 4k7 5% 1/4W CARBON | MULLARD | CR25 | 8 |
| R3 | 000472 | 4k7 5% 1/4W CARBON | MULLARD | CR25 | - |
| R4 | 000472 | 4k7 5% 1/4W CARBON | MULLARD | CR25 | - |
| R5 | 000472 | 4k7 5% 1/4W CARBON | MULLARD | CR25 | - |
| R6 | 000472 | 4k7 5% 1/4W CARBON | MULLARD | CR25 | - |
| R7 | 000474 | 470k 5% 1/4W CARBON | MULLARD | CR25 | 2 |
| R8 | 000472 | 4k7 5% 1/4W CARBON | MULLARD | CR25 | - |
| R9 | 000273 | 27k 5% 1/4W CARBON | MULLARD | CR25 | 1 |
| R10 | 000474 | 470k 5% 1/4W CARBON | MULLARD | CR25 | - |
| R11 | 011212 | 12k1 1% 1/8W 50ppm MF | HOLCO | H8C | 1 |
| R12 | 012492 | 24k9 1% 1/8W 50ppm MF | HOLCO | H8C | 1 |
| R13 | 000153 | 15k 5% 1/4W CARBON | MULLARD | CR25 | 1 |
| R14 | 000471 | 470R 5% 1/4W CARBON | MULLARD | CR25 | 8 |
| R15 | 008031 | 100R 5% 1.6 W MF | MULLARD | PR37 | - |
| R16 | 000104 | 100k 5% 1/4W CARBON | MULLARD | CR25 | 1 |
| R17 | | NOT USED | | | - |
| R18 | | NOT USED | | | - |
| R19 | 000821 | 820R 5% 1/4W CARBON | MULLARD | CR25 | 1 |
| R20 | 000471 | 470R 5% 1/4W CARBON | MULLARD | CR25 | - |
| R21 | 000471 | 470R 5% 1/4W CARBON | MULLARD | CR25 | - |
| R22 | 000471 | 470R 5% 1/4W CARBON | MULLARD | CR25 | - |
| R23 | 000471 | 470R 5% 1/4W CARBON | MULLARD | CR25 | - |

| | | | |
|------------------------------|------------------------|------------------------|---|
| NOTES | | DATE 9/1/86 | datron ELECTRONICS LTD |
| SEE SHEET 1 FOR LATEST ISSUE | DATE 31.5.84 | DRAWN WJE | TITLE 4700. ANALOG INTERFACE PCB ASSY. |
| | RELEASED | CHECK WJE | DRAWING NUMBER 400648 |
| | | APPROVED WJE | SHEET 2 OF 9 |
| | | DATE 9/1/86 | |

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No. USED Per Assy. |
|------------|-----------------|---------------------|------------------------|-------------------------|--------------------|
| R24 | 000471 | 470R 5% 1/4W CARBON | MULLARD | CR25 | - |
| R25 | 000331 | 330R 5% 1/4W CARBON | MULLARD | CR25 | 1 |
| R26 | 000471 | 470R 5% 1/4W CARBON | MULLARD | CR25 | - |
| R27 | 000102 | 1K 5% 1/4W CARBON | MULLARD | CR25 | 2 |
| R28 | 000102 | 1K 5% 1/4W CARBON | MULLARD | CR25 | - |
| R29 | 000561 | 560R 5% 1/4W CARBON | MULLARD | CR25 | 4 |
| R30 | 000561 | 560R 5% 1/4W CARBON | MULLARD | CR25 | - |
| R31 | 000561 | 560R 5% 1/4W CARBON | MULLARD | CR25 | - |
| R32 | 000561 | 560R 5% 1/4W CARBON | MULLARD | CR25 | - |
| R33 | 000103 | 10K 5% 1/4W CARBON | MULLARD | CR25 | 1 |
| R34 | 000154 | 150K 5% 1/4W CARBON | MULLARD | CR25 | 1 |
| R35 | 000472 | 4K7 5% 1/4W CARBON | MULLARD | CR25 | - |
| R36 | 000471 | 470R 5% 1/4W CARBON | MULLARD | CR25 | - |
| R37 | 000472 | 4K7 5% 1/4W CARBON | MULLARD | CR25 | - |
| AN1 | 090079 | 5kG x 8 2% NETWORK | AB | 850-91-5k6 | 2 |
| AN2 | 090079 | 5kG x 8 2% NETWORK | AB | 850-91-5k6 | - |

NOTES.

SEE SHEET 2 FOR LATEST ISSUE

| | | | |
|----------|--------|------------------------|----------------------------------|
| DATE | 9/1/86 | datron ELECTRONICS LTD | |
| DRAWN | JFA | TITLE | 4700 ANALOG INTERFACE PCB. ASSY. |
| CHECKED | | DRAWING NUMBER | 400648 |
| APPROVED | | SHEET | 3 OF 9 |
| DATE | | | |

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No. USED Per Assy. |
|------------|-----------------|-------------------------|------------------------|-------------------------|--------------------|
| C1 | 104026 | 47nF ±50% 50V CER DISC | SIEMENS | B37449 | 46 |
| C2 | 104026 | 47nF " " " " | " | " | - |
| C3 | 104026 | 47nF " " " " | " | " | - |
| C4 | 104026 | 47nF " " " " | " | " | - |
| C5 | 104026 | 47nF " " " " | " | " | - |
| C6 | 104026 | 47nF " " " " | " | " | - |
| C7 | 104026 | 47nF " " " " | " | " | - |
| C8 | 104026 | 47nF " " " " | " | " | - |
| C9 | 100221 | 220pF 2% 100V CER PLATE | MULLARD | 2222 683 221 | 1 |
| C10 | 100272 | 2n7F 10% 100V CER PLATE | MULLARD | 2222 630 19272 | 1 |
| C11 | 104026 | 47nF ±50% 50V CER DISC | SIEMENS | B37449 | - |
| C12 | 104026 | 47nF " " " " | " | " | - |
| C13 | 104026 | 47nF " " " " | " | " | - |
| C14 | 104026 | 47nF " " " " | " | " | - |
| C15 | 104026 | 47nF " " " " | " | " | - |
| C16 | 104026 | 47nF " " " " | " | " | - |
| C17 | 104026 | 47nF " " " " | " | " | - |
| C18 | 104026 | 47nF " " " " | " | " | - |
| C19 | 104026 | 47nF " " " " | " | " | - |
| C20 | 104026 | 47nF " " " " | " | " | - |
| C21 | 104026 | 47nF " " " " | " | " | - |
| C22 | 104026 | 47nF " " " " | " | " | - |
| C23 | 104026 | 47nF " " " " | " | " | - |

NOTES.

SEE SHEET 2 FOR LATEST ISSUE

| | | | |
|----------|--------|------------------------|----------------------------------|
| DATE | 9/1/86 | datron ELECTRONICS LTD | |
| DRAWN | JFA | TITLE | 4700 ANALOG INTERFACE PCB. ASSY. |
| CHECKED | | DRAWING NUMBER | 400648 |
| APPROVED | | SHEET | 4 OF 9 |
| DATE | | | |

| DESIGNATOR | DATRON PART No | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No | No. USED Per Assy. |
|------------|----------------|------------------------------|------------------------|------------------------|--------------------|
| C24 | 104026 | 47nF $\pm 50\%$ 50V CER DISC | SIEMENS | B37449 | - |
| C25 | 104026 | " " " " " " " " | " | " | - |
| C26 | 104026 | " " " " " " " " | " | " | - |
| C27 | 104026 | " " " " " " " " | " | " | - |
| C28 | 104026 | " " " " " " " " | " | " | - |
| C29 | 150016 | 1µF 20% 35V DIP TANT | UNION CARBIDE | KIROE35 | 2 |
| C30 | 100182 | 1nBF 10% 100V CER PLATE | MULLARD | 2222 630 19182 | 1 |
| C31 | 100331 | 330pF 2% 100V CER PLATE | MULLARD | 2222 681 331 | 2 |
| C32 | 150012 | 100nF 20% 35V DIP TANT | UNION CARBIDE | KRIOE35 | 1 |
| C33 | 104026 | 47nF $\pm 50\%$ 50V CER DISC | SIEMENS | B37449 | - |
| C34 | 104026 | " " " " " " " " | " | " | - |
| C35 | 104026 | " " " " " " " " | " | " | - |
| C36 | 104026 | " " " " " " " " | " | " | - |
| C37 | 104026 | " " " " " " " " | " | " | - |
| C38 | 104026 | " " " " " " " " | " | " | - |
| C39 | 102220 | 22pF 5% 500V CER DISC | ITT | CD10 | 1 |
| C40 | 102330 | 33pF 5% 500V CER DISC | ITT | CD10 | 1 |
| C41 | 104026 | 47nF $\pm 50\%$ 50V CER DISC | SIEMENS | B37449 | - |
| C42 | 104026 | " " " " " " " " | " | " | - |
| C43 | 104026 | " " " " " " " " | " | " | - |
| C44 | 104026 | " " " " " " " " | " | " | - |
| C45 | 104026 | " " " " " " " " | " | " | - |
| C46 | 104026 | " " " " " " " " | " | " | - |

NOTES

SEE SHEET 2 FOR LATEST ISSUE

| ISS | ECN | DATE | BY |
|-----|-----|------|----|
| | | | |
| | | | |
| | | | |
| | | | |

DATE 9/1/86

datron ELECTRONICS LTD

TITLE 4700. ANALOG INTERFACE PCB ASSY.

DRAWING NUMBER 400648

SHEET 5 OF 9

| DESIGNATOR | DATRON PART No | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No | No. USED Per Assy. |
|----------------|----------------|------------------------------|------------------------|------------------------|--------------------|
| C47 | 150024 | 47µF 20% 16V DIP TANT | UNION CARBIDE | K47E16 | 1 |
| C48, 51 | 104026 | 47nF $\pm 50\%$ 50V CER DISC | SIEMENS | B37449 | - |
| C49, 52-55, 61 | 104026 | 47nF $\pm 50\%$ 50V CER DISC | SIEMENS | B37449 | - |
| C50 | 100331 | 330pF 2% 100V CER PLATE | MULLARD | 2222 681 331 | - |
| C53 | 110042 | 100nF 20% 63V POLYESTER | WIMA | MKS2 | 1 |
| C60 | 150016 | 1µF 20% 35V DIP TANT | UNION CARBIDE | KIROE35 | - |
| C62 | 104041 | 10nF 25% 250V CER DISC | STC | CD10 | 1 |
| D1 | 200001 | 75mA 75v GP Si DIODE | FAIRCHILD | IN4148 | 2 |
| D2 | 200001 | 75mA 75v GP Si DIODE | FAIRCHILD | IN4148 | - |
| Q1 | 240014 | SI NPN TRANSISTOR | NATIONAL | BC337 | 1 |
| M1 | 270050 | HEX INVERTER LS | NATIONAL | DM74LS04N | 1 |
| M2 | 280008 | QUAD 2 1/P 'NAND' GATE | MOTOROLA | MC14011BCP | 1 |
| M3 | 280011 | DUAL D FLIP-FLOP | MOTOROLA | MC14013BCP | 2 |
| M4 | 280059 | DUAL BINARY UP COUNTER | MOTOROLA | MC14520BCP | 1 |
| M5 | 280037 | HEX BUFFER | MOTOROLA | MC14050BCP | 1 |
| M6 | 270048 | QUAD 2 1/P 'NAND' LS | NATIONAL | DM74LS00N | 2 |
| M7 | 270072 | QUAD 2 1/P 'NOR' LS | NATIONAL | DM74LS02N | 2 |
| M8 | 270002 | QUAD 2 1/P O/C NAND | NATIONAL | DM7401N | 2 |
| M9 | 270094 | DUAL LINE RECEIVER | TEXAS | SN75182N | 1 |
| M10 | 270076 | DUAL MONOSTABLE LS | NATIONAL | DM74LS123N | 1 |
| M11 | 270095 | DUAL DECADE COUNTER | NATIONAL | DM74LS390N | 2 |

NOTES

SEE SHEET 2 FOR LATEST ISSUE

| ISS | ECN | DATE | BY |
|-----|-----|------|----|
| | | | |
| | | | |
| | | | |
| | | | |

DATE 9/1/86

datron ELECTRONICS LTD

TITLE 4700. ANALOG INTERFACE PCB ASSY.

DRAWING NUMBER 400648

SHEET 6 OF 9

| REF. NO. | DATRON PART NO. | DESCRIPTION | MANUFACTURER | QTY. ORDERED | QTY. USED |
|----------|-----------------|---------------------------|--------------|--------------|-----------|
| | 270073 | QUAD 2 1/2 FLIP-FLOP LS | NATIONAL | DM74LS279N | 0 |
| M14 | 270075 | DUAL D FLIP-FLOP LS | NATIONAL | DM74LS279N | 0 |
| M15 | 280095 | 4BIT SYNC BINARY COUNTER | MULLARD | HEF401633P | 0 |
| M16 | 280095 | 4BIT SYNC BINARY COUNTER | MULLARD | HEF401633P | 0 |
| M17 | 280095 | 4BIT SYNC BINARY COUNTER | MULLARD | HEF401633P | 0 |
| M18 | 270096 | DUAL 4 TO 1 MULTIPLEXER | NATIONAL | DM74LS153N | 1 |
| M19 | 280093 | QUAD EXCLUSIVE-OR GATE | MOTOROLA | MC14070BCP | 0 |
| M20 | 280093 | QUAD EXCLUSIVE-OR GATE | MOTOROLA | MC14070BCP | 0 |
| | 270073 | QUAD 2 1/2 FLIP-FLOP LS | NATIONAL | DM74LS279N | 0 |
| | 270073 | QUAD 2 1/2 FLIP-FLOP LS | NATIONAL | DM74LS279N | 0 |
| | 270073 | QUAD 2 1/2 FLIP-FLOP LS | NATIONAL | DM74LS279N | 0 |
| | 270073 | QUAD 2 1/2 FLIP-FLOP LS | NATIONAL | DM74LS279N | 0 |
| | 270073 | QUAD 2 1/2 FLIP-FLOP LS | NATIONAL | DM74LS279N | 0 |
| | 270073 | QUAD 2 1/2 FLIP-FLOP LS | NATIONAL | DM74LS279N | 0 |
| M25 | 280093 | QUAD EXCLUSIVE-OR GATE | MOTOROLA | MC14070BCP | 0 |
| M26 | 280093 | QUAD EXCLUSIVE-OR GATE | MOTOROLA | MC14070BCP | 0 |
| M27 | 280093 | QUAD EXCLUSIVE-OR GATE | MOTOROLA | MC14070BCP | 0 |
| M28 | 270095 | DUAL DECADE COUNTER | NATIONAL | DM74LS390N | 0 |
| M29 | 280068 | DUAL PRECISION MONOSTABLE | MOTOROLA | MC14538BCP | 1 |
| M30 | 280145 | PHASE LOCKED LOOP | MOTOROLA | MC14046BCP | 1 |
| M31 | 280015 | QUAD LATCH | MOTOROLA | MC14076BCP | 7 |
| M32 | 280015 | QUAD LATCH | MOTOROLA | MC14076BCP | 0 |
| M33 | 280015 | QUAD LATCH | MOTOROLA | MC14076BCP | 0 |
| M34 | 280015 | QUAD LATCH | MOTOROLA | MC14076BCP | 0 |

NOTES.

SEE SHEET 2 FOR LATEST ISSUE

| ISS | ECO | DATE | CHKD | | | | | | | | |
|-----|-----|------|------|--|--|--|--|--|--|--|--|
| | | | | | | | | | | | |

| | | |
|----------------|----------|--|
| DATE 9/1/86 | | datron ELECTRONICS LTD TITLE 4700. ANALOG INTERFACE PCB. ASSY. |
| DRAWN | | |
| CHECKED | APPROVED | DRAWING NUMBER 400648 |
| DATE | | SHEET OF 7 OF 9 |

| DESIGNATOR | DATRON PART NO. | DESCRIPTION | MANUFACTURER | QTY. ORDERED | QTY. USED |
|------------|-----------------|--------------------------------|--------------|--------------|-----------|
| M35 | 270073 | QUAD 2 1/2 FLIP-FLOP LS | NATIONAL | DM74LS09N | 2 |
| M36 | 270073 | QUAD 2 1/2 FLIP-FLOP LS | NATIONAL | DM74LS09N | 0 |
| M37 | 280015 | QUAD LATCH | MOTOROLA | MC14076BCP | 0 |
| M38 | 280015 | QUAD LATCH | MOTOROLA | MC14076BCP | 0 |
| M39 | 280015 | QUAD LATCH | MOTOROLA | MC14076BCP | 0 |
| M40 | 270036 | MONOSTABLE | NATIONAL | DM74121N | 1 |
| M41 | 270057 | DUAL JK FLIP-FLOP LS | NATIONAL | DM74LS76N | 2 |
| M42 | 270057 | DUAL JK FLIP-FLOP LS | NATIONAL | DM74LS76N | 0 |
| M43 | 270048 | QUAD 2 1/2 NAND LS | NATIONAL | DM74LS00N | 0 |
| M44 | 280094 | SYNC SERIAL DATA ADAPTOR | MOTOROLA | MC6852P | 1 |
| M45 | 280024 | TRI-STATE HEX. NON-INV. BUFFER | MOTOROLA | MC14503BCP | 1 |
| M46 | 270002 | QUAD 2 1/2 O/C NAND | NATIONAL | DM7401N | 0 |
| M47 | 280038 | HEX D FLIP-FLOP | MOTOROLA | MC14174BCP | 4 |
| M48 | 280038 | HEX D FLIP-FLOP | MOTOROLA | MC14174BCP | 0 |
| M49 | 280011 | DUAL D FLIP-FLOP | MOTOROLA | MC14013BCP | 0 |
| M50 | 280105 | 8 1/2 NAND | MOTOROLA | MC14068BCP | 1 |
| M51 | 280038 | HEX D FLIP-FLOP | MOTOROLA | MC14174BCP | 0 |
| M52 | 280038 | HEX D FLIP-FLOP | MOTOROLA | MC14174BCP | 0 |
| M53 | 270086 | 4-BIT BINARY COUNTER | NATIONAL | DM74LS93N | 1 |
| M54 | 280023 | QUAD 2 1/2 NOR GATE | MOTOROLA | MC14001UBCP | 1 |
| M55 | 280149 | GEN. PURPOSE TIMER | INTERSIL | ICM75551PA | 1 |

NOTES.

SEE SHEET 2 FOR LATEST ISSUE

| ISS | ECO | DATE | CHKD | | | | | | | | |
|-----|-----|------|------|--|--|--|--|--|--|--|--|
| | | | | | | | | | | | |

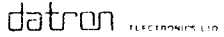

| | | |
|----------------|----------|--|
| DATE 9/1/86 | | datron ELECTRONICS LTD TITLE 4700. ANALOG INTERFACE PCB. ASSY. |
| DRAWN | | |
| CHECKED | APPROVED | DRAWING NUMBER 400648 |
| DATE | | SHEET OF 8 OF 9 |

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | Qty. USED (Per Assy) |
|------------|-----------------|-----------------------------|---------------------------|-------------------------|----------------------|
| | 410264-2 | PCB | | | 1 |
| | 605060 | 14 WAY DIL SOCKET | JERMYN | J23-18014 | 28 |
| | 605061 | 16 WAY DIL SOCKET | JERMYN | J23-18016 | 25 |
| | 605064 | 24 WAY DIL SOCKET | JERMYN | J23-18024 | 1 |
| | 630117 | CIRCUIT BD EJECTOR | RICHCO | CBE BROWN | 2 |
| XI | 800029 | CRYSTAL OSCILATOR | 4.096 MH ₂ IQD | IQXO-100 | 1 |
| | 620007 | TEST POINT TERMINAL | MICROVAR | C 30 | 27 |
| | 540002 | 22 SWG TINNED CU WIRE | RS | | A/R |
| | 630243 | GLASS BEAD 24% x 0.8% x 1.8 | MAN SOL (PREFORMS) | M5363B/3 | 92 |
| TI | 310003 | PULSE TRANSFORMER | NEWPORT | 76610/1 | 1 |
| | 605059 | 8 WAY DIL SOCKET | | | 1 |
| | 900004 | SILICONE RUBBER COMPOUND | RS | 555-588 | A/R |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |

NOTES

SEE SHEET 2 FOR LATEST ISSUE

| | | | | | | | | | | | |
|------|--|--|--|--|--|--|--|--|--|--|--|
| REV. | | | | | | | | | | | |
| DATE | | | | | | | | | | | |
| BY | | | | | | | | | | | |

| | | |
|--------------------|---|---|
| DATE | 3 3 86 |  ELECTRONICS LTD. |
| DRAWN |  | |
| CHECKED | | |
| APPROVED | | |
| TITLE | | 4700 ANALOG |
| INTERFACE PCB ASSY | | |
| DATE | 400648 | SHEET 9 OF 9 |

| DESCRIPTION | DRAWING NUMBER | SHEET NUMBER | ISSUE | REVISION |
|------------------------|----------------|--------------|-------|---|
| COMP. LAYOUT | 430652 | 1 | 1.0 | 1.1 2.0 2.1 3.0 4.0 4.1 4.2 |
| SCHMATIC | 430652 | 1 | 1.0 | 1.1 2.0 2.1 3.0 4.0 4.1 4.2 |
| SCHMATIC | 430652 | 6 | 1.0 | 1.1 2.0 2.1 3.0 4.0 4.1 4.2 |
| FUNCTIONAL TEST. PROC. | 460652/FT | 1-14 | 1.0 | 2.0 2.1 2.2 3.0 3.1 4.0 |
| FUNCT. TEST TICK LIST | 470652/FT | 1-2 | 1.0 | 2.0 2.1 2.2 3.0 3.1 4.0 |
| PCB | 410257 | | 4.0 | 4.0 4.0 4.0 |

NOTES: INDICATES NO CHANGE TO DOC AT ISSUE LEVEL CHANGE.

datron ELECTRONICS LTD. HORWICH ENGLAND

DATE: 12.2.86

CHKD: R.K. COFFMAN

APPR: *[Signature]*

TITLE: 4700 REF. DIVIDER PCB ASSY

DRAWING No. 400652 SHEET 1 OF 21

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No. USED Per Assy. |
|------------|-----------------|-----------------------|------------------------|-------------------------|--------------------|
| R1 | 000472 | 4k7 5% 1/4W CARBON | MULLARD | CR25 | 6 |
| R2 | 000561 | 560R 5% 1/4W CARBON | MULLARD | CR25 | 8 |
| R3 | 000622 | 6k2 5% 1/4W CARBON | MULLARD | CR25 | 4 |
| R4 | 000561 | 560R 5% 1/4W CARBON | MULLARD | CR25 | - |
| R5 | 000472 | 4k7 5% 1/4W CARBON | MULLARD | CR25 | - |
| R6 | 000472 | 4k7 5% 1/4W CARBON | MULLARD | CR25 | - |
| R7 | 000561 | 560R 5% 1/4W CARBON | MULLARD | CR25 | - |
| R8 | 000272 | 2k7 5% 1/4W CARBON | MULLARD | CR25 | 2 |
| R9 | 000561 | 560R 5% 1/4W CARBON | MULLARD | CR25 | - |
| R10 | 000472 | 4k7 5% 1/4W CARBON | MULLARD | CR25 | - |
| R11 | 000103 | 10k 5% 1/4W CARBON | MULLARD | CR25 | 9 |
| R12 | 000102 | 1k 5% 1/4W CARBON | MULLARD | CR25 | 5 |
| R13 | 000622 | 6k2 5% 1/4W CARBON | MULLARD | CR25 | - |
| R14 | 000102 | 1k 5% 1/4W CARBON | MULLARD | CR25 | - |
| R15 | 000103 | 10k 5% 1/4W CARBON | MULLARD | CR25 | - |
| R16 | 013161 | 3k16 1% 1/8W 50ppm MF | HOLCO | H8C | 4 |
| R17 | 000101 | 100R 5% 1/4W CARBON | MULLARD | CR25 | 12 |
| R18 (FSV) | 014750 | 475R 1% 1/8W 50ppm MF | HOLCO | H8C | 1 |
| R19 | 013161 | 3k16 1% 1/8W 50ppm MF | HOLCO | H8C | - |
| R20 | 000101 | 100R 5% 1/4W CARBON | MULLARD | CR25 | - |
| R21 | 013161 | 3k16 1% 1/8W 50ppm MF | HOLCO | H8C | - |
| R22 | 000101 | 100R 5% 1/4W CARBON | MULLARD | CR25 | - |
| R23 (FSV) | 012261 | 2k26 1% 1/8W 50ppm MF | HOLCO | H8C | 1 |

NOTES

SEE SHEET 1 FOR LATEST ISSUE

| | | | | |
|------|--------------------|--------------------|--------------------|--------------------|
| ISS | 2 | 3 | 4 | 5 |
| ECO | 1577 | 1603 | 1665 | 1707 |
| DATE | 7.2.87 | 5.4.84 | 8.9.84 | 21.3.84 |
| CHKD | <i>[Signature]</i> | <i>[Signature]</i> | <i>[Signature]</i> | <i>[Signature]</i> |

DATE: 12.2.86

datron ELECTRONICS LTD.

TITLE: 4700 REF DIVIDER PCB ASSY

DRAWING NUMBER: 400652 SHEET 2 OF 21

| DESIGNATOR | DATRŌN PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No. USED Per Assy. |
|------------|-----------------|-----------------------|------------------------|-------------------------|--------------------|
| R24 | 013161 | 3k16 1% 1/8W 50ppm MF | HOLCO | H8C | - |
| R25 | 000101 | 100R 5% 1/4W CARBON | MULLARD | CR25 | - |
| R26 | 000102 | 1k 5% 1/4W CARBON | MULLARD | CR25 | - |
| R27 | 000431 | 430R 5% 1/4W CARBON | MULLARD | CR25 | 2 |
| R28 | 000101 | 100R 5% 1/4W CARBON | MULLARD | CR25 | - |
| R29 (FSV) | 019538 | 95R3 1% 1/8W 50ppm MF | HOLCO | H8C | 4 |
| R30 | 000431 | 430R 5% 1/4W CARBON | MULLARD | CR25 | - |
| R31 | 000101 | 100R 5% 1/4W CARBON | MULLARD | CR25 | - |
| R32 | 000102 | 1k 5% 1/4W CARBON | MULLARD | CR25 | - |
| R33 (FSV) | 019538 | 95R3 1% 1/8W 50ppm MF | HOLCO | H8C | - |
| R34 | 000562 | 5k6 5% 1/4W CARBON | MULLARD | CR25 | 4 |
| R35 | 000561 | 560R 5% 1/4W CARBON | MULLARD | CR25 | - |
| R36 | 000622 | 6k2 5% 1/4W CARBON | MULLARD | CR25 | - |
| R37 | 000561 | 560R 5% 1/4W CARBON | MULLARD | CR25 | - |
| R38 | 000562 | 5k6 5% 1/4W CARBON | MULLARD | CR25 | - |
| R39 | 000562 | 5k6 5% 1/4W CARBON | MULLARD | CR25 | - |
| R40 | 000561 | 560R 5% 1/4W CARBON | MULLARD | CR25 | - |
| R41 | 000622 | 6k2 5% 1/4W CARBON | MULLARD | CR25 | - |
| R42 | 000561 | 560R 5% 1/4W CARBON | MULLARD | CR25 | - |
| R43 | 000562 | 5k6 5% 1/4W CARBON | MULLARD | CR25 | - |
| R44 | 000202 | 2k0 5% 1/4W CARBON | MULLARD | CR25 | 2 |
| R45 | 000222 | 2k2 5% 1/4W CARBON | MULLARD | CR25 | 3 |
| R46 | 014320 | 432R 1% 1/8W 50ppm MF | HOLCO | H8C | 4 |

NOTES:
SEE SHEET 2 FOR LATEST ISSUE

| | | | | | | | | | | | | | | | |
|------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ISS | | | | | | | | | | | | | | | |
| ECD | | | | | | | | | | | | | | | |
| DATE | | | | | | | | | | | | | | | |
| CHKD | | | | | | | | | | | | | | | |

| | | | |
|----------|---------|-------------------------------------|--|
| DATE | 12 2 86 | datron ELECTRONICS LTD | |
| DRAWN | JL | TITLE 4700 REF DIVIDER PCB ASSY. | |
| CHECKED | | DRAWING NUMBER 400652 | |
| APPROVED | | SHEET OF 21 | |
| DATE | | | |

W 1164

| DESIGNATOR | DATRŌN PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No. USED Per Assy. |
|------------|-----------------|-----------------------|------------------------|-------------------------|--------------------|
| R47 | 000101 | 100R 5% 1/4W CARBON | MULLARD | CR25 | - |
| R48 (FSV) | 019538 | 95R3 1% 1/8W 50ppm MF | HOLCO | H8C | - |
| R49 | 014320 | 432R 1% 1/8W 50ppm MF | HOLCO | H8C | - |
| R50 | 000101 | 100R 5% 1/4W CARBON | MULLARD | CR25 | - |
| R51 | 014320 | 432R 1% 1/8W 50ppm MF | HOLCO | H8C | - |
| R52 | 000101 | 100R 5% 1/4W CARBON | MULLARD | CR25 | - |
| R53 (FSV) | 019538 | 95R3 1% 1/8W 50ppm MF | HOLCO | H8C | - |
| R54 | 014320 | 432R 1% 1/8W 50ppm MF | HOLCO | H8C | - |
| R55 | 000101 | 100R 5% 1/4W CARBON | MULLARD | CR25 | - |
| R56 | 000474 | 470k 5% 1/4W CARBON | MULLARD | CR25 | 1 |
| R57 | 000184 | 180k 5% 1/4W CARBON | MULLARD | CR25 | 1 |
| R58 | 013742 | 37k4 1% 1/8W 50ppm MF | HOLCO | H8C | 1 |
| R59 | 000103 | 10k 5% 1/4W CARBON | MULLARD | CR25 | - |
| R60 | 000338 | 3R3 5% 1/4W CARBON | MULLARD | CR25 | 1 |
| R61 | 000104 | 100k 5% 1/4W CARBON | MULLARD | CR25 | 2 |
| R62 | 018872 | 88k7 1% 1/8W 50ppm MF | HOLCO | H8C | 1 |
| R63 | 017872 | 78k7 1% 1/8W 50ppm MF | HOLCO | H8C | 2 |
| R64 | 070144 | 36k0 .01% 5ppm WW | MANN | MX125B | 1 |
| R65 | 070142 | 12k0 .01% 5ppm WW | MANN | MX125B | 2 |
| R66 | 017872 | 78k7 1% 1/8W 50ppm MF | HOLCO | H8C | - |
| R67 | 000912 | 9k1 5% 1/4W CARBON | MULLARD | CR25 | 1 |
| R68 | | NOT USED | | | - |
| R69 | | NOT USED | | | - |

NOTES:
SEE SHEET 2 FOR LATEST ISSUE

| | | | | | | | | | | | | | | |
|------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ISS | | | | | | | | | | | | | | |
| ECD | | | | | | | | | | | | | | |
| DATE | | | | | | | | | | | | | | |
| CHKD | | | | | | | | | | | | | | |

| | | | |
|----------|---------|-------------------------------------|--|
| DATE | 12 2 86 | datron ELECTRONICS LTD | |
| DRAWN | JL | TITLE 4700 REF DIVIDER PCB ASSY. | |
| CHECKED | | DRAWING NUMBER 400652 | |
| APPROVED | | SHEET OF 21 | |
| DATE | | | |

W 1164

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No. USED Per Assy. |
|------------|-----------------|-----------------------|------------------------|-------------------------|--------------------|
| R116 | 000222 | 2k2 5% 1/3W CARBON | MULLARD | CR25 | - |
| R117 | | NOT USED | | | - |
| R118 | 006132 | 1k30 2% 1W MET-OX | ELECTROSIL | FPI | 2 |
| R119 | 006132 | 1k30 2% 1W MET-OX | ELECTROSIL | FPI | - |
| R120 | 000103 | 10k 5% 1/4W CARBON | MULLARD | CR25 | - |
| R121 | 000473 | 47k 5% 1/4W CARBON | MULLARD | CR25 | - |
| R122 | 000823 | 82k 5% 1/4W CARBON | MULLARD | CR25 | 1 |
| R123 | 000473 | 47k 5% 1/4W CARBON | MULLARD | CR25 | - |
| R124 | 000152 | 1k5 5% 1/4W CARBON | MULLARD | CR25 | 2 |
| R125 | 011002 | 10k0 1% 1/8W 50ppm MF | HOLCO | H8C | - |
| R126 | 011002 | 10k0 1% 1/8W 50ppm MF | HOLCO | H8C | - |
| R127 | 011002 | 10k0 1% 1/8W 50ppm MF | HOLCO | H8C | - |
| R128 | 012001 | 2k 1% 1/8W 50ppm MF | HOLCO | H8C | - |
| R129 | 011302 | 13k 1% 1/8W 50ppm MF | HOLCO | H8C | - |
| R130 | 012001 | 2k 1% 1/8W 50ppm MF | HOLCO | H8C | - |
| R131 | 011302 | 13k 1% 1/8W 50ppm MF | HOLCO | H8C | - |
| R132 | 000470 | 47R 5% 1/3W CARBON | MULLARD | CR25 | - |
| R133 | 000222 | 2k2 5% 1/3W CARBON | MULLARD | CR25 | - |
| R134 | 000821 | 820R 5% 1/3W CARBON | MULLARD | CR25 | 2 |
| R135 | 000821 | 820R 5% 1/3W CARBON | MULLARD | CR25 | - |
| R136 | 000393 | 39k 5% 1/3W CARBON | MULLARD | CR25 | - |
| R137 | 000393 | 39k 5% 1/3W CARBON | MULLARD | CR25 | - |
| R138 | 000220 | 22R 5% 1/3W CARBON | MULLARD | CR25 | 2 |

NOTES.

SEE SHEET 2 FOR LATEST ISSUE

| | | | | | | | | | | | | | | |
|------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ISS | | | | | | | | | | | | | | |
| ECO | | | | | | | | | | | | | | |
| DATE | | | | | | | | | | | | | | |
| CHKD | | | | | | | | | | | | | | |

| | | |
|-----------------|---------------------------------------|------------------|
| DATE 12.2.86 | datron ELECTRONICS LTD | |
| DRAWN | TITLE 4700 REF DIVIDER PCB ASSY | |
| CHECKED | | |
| APPROVED | DRAWING NUMBER 400652 | SHEET 7 OF 21 |
| DATE | | |

M. 1164

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No. USED Per Assy. |
|------------|-----------------|--------------------|------------------------|-------------------------|--------------------|
| R139 | 000220 | 22R 5% 1/3W CARBON | MULLARD | CR25 | - |
| R140 | 000152 | 1k5 5% 1/3W CARBON | MULLARD | CR25 | - |
| R141 | 000103 | 10k 5% 1/3W CARBON | MULLARD | CR25 | - |
| R142 | 000472 | 4k7 5% 1/3W CARBON | MULLARD | CR25 | - |
| R143 | 000473 | 47k 5% 1/3W CARBON | MULLARD | CR25 | - |
| R144 | 000103 | 10k 5% 1/3W CARBON | MULLARD | CR25 | - |
| R145 | 000202 | 2k 5% 1/3W CARBON | MULLARD | CR25 | - |
| R146 | 000303 | 30k 5% 1/3W CARBON | MULLARD | CR25 | 1 |
| R147 | 000155 | 1M5 5% 1/3W CARBON | MULLARD | CR25 | 1 |
| R148 | 000273 | 27k 5% 1/3W CARBON | MULLARD | CR25 | 1 |
| AN1 | 090031 | 1k x7 2% NETWORK | BECKMAN | L08-I-R1K | 1 |
| AN2 | 090096 | 1M x8 2% NETWORK | BECKMAN | L09-I-R1M | 2 |
| AN3 | 090096 | 1M x8 2% NETWORK | BECKMAN | L09-I-R1M | - |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |

NOTES.

SEE SHEET 2 FOR LATEST ISSUE

| | | | | | | | | | | | | | | |
|------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ISS | | | | | | | | | | | | | | |
| ECO | | | | | | | | | | | | | | |
| DATE | | | | | | | | | | | | | | |
| CHKD | | | | | | | | | | | | | | |

| | | |
|-----------------|---------------------------------------|------------------|
| DATE 12.2.86 | datron ELECTRONICS LTD | |
| DRAWN | TITLE 4700 REF DIVIDER PCB ASSY | |
| CHECKED | | |
| APPROVED | DRAWING NUMBER 400652 | SHEET 8 OF 21 |
| DATE | | |

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No. USED Per Assy. |
|------------|-----------------|---|------------------------|-------------------------|--------------------|
| 1 | 104026 | 47nf ^{+30%} / _{-20%} 50V CER DISC | SIEMENS | B37449 | 23 |
| 2 | 104026 | 47nf ^{+50%} / _{-20%} 50V CER DISC | SIEMENS | B37449 | - |
| 3 | 150003 | 47µF 20% 6Y3 DIP TANT | UNION CARBIDE | K47EGV3 | 1 |
| 4 | 150021 | 22µF 20% 25V DIP TANT | UNION CARBIDE | K22E25 | 1 |
| 5 | | NOT USED | | | - |
| 6 | 104026 | 47nf ^{+50%} / _{-20%} 50V CER DISC | SIEMENS | B37449 | - |
| 7 | 150016 | 1µF 20% 35V DIP TANT | UNION CARBIDE | K10E35 | 4 |
| 8 | 104026 | 47nf ^{+50%} / _{-20%} 50V CER DISC | SIEMENS | B37449 | - |
| 9 | 104026 | 47nf ^{+50%} / _{-20%} 50V CER DISC | SIEMENS | B37449 | - |
| 10 | 104026 | 47nf ^{+50%} / _{-20%} 50V CER DISC | SIEMENS | B37449 | - |
| 11 | 104026 | 47nf ^{+50%} / _{-20%} 50V CER DISC | SIEMENS | B37449 | - |
| 12 | 104026 | 47nf ^{+50%} / _{-20%} 50V CER DISC | SIEMENS | B37449 | - |
| 13 | 102101 | 100µF 10% 500V CER DISC | ITT | CD10 | 1 |
| 14 | 104026 | 47nf ^{+50%} / _{-20%} 50V CER DISC | SIEMENS | B37449 | - |
| 15 | 110013 | 100nf 20% 250V POLYESTER | MULLARD | C280AEP100K | 2 |
| 16 | 110013 | 100nf 20% 250V POLYESTER | MULLARD | C280AEP100K | - |
| 17 | 104026 | 47nf ^{+50%} / _{-20%} 50V CER DISC | SIEMENS | B37449 | - |
| 18 | 104026 | 47nf ^{+50%} / _{-20%} 50V CER DISC | SIEMENS | B37449 | - |
| 19 | 104026 | 47nf ^{+50%} / _{-20%} 50V CER DISC | SIEMENS | B37449 | - |
| 20 | 104026 | 47nf ^{+50%} / _{-20%} 50V CER DISC | SIEMENS | B37449 | - |
| 21 | 104026 | 47nf ^{+50%} / _{-20%} 50V CER DISC | SIEMENS | B37449 | - |
| 22 | 104026 | 47nf ^{+50%} / _{-20%} 50V CER DISC | SIEMENS | B37449 | - |
| 23 | 140016 | 470nf 10% 250V POLYPROP | RIFA | PHE402 HFK | 10 |

NOTES.

SEE SHEET 2 FOR LATEST ISSUE

| | | | | | | | | | | | | |
|------|--|--|--|--|--|--|--|--|--|--|--|--|
| ISS | | | | | | | | | | | | |
| ECD | | | | | | | | | | | | |
| DATE | | | | | | | | | | | | |
| CHKD | | | | | | | | | | | | |

| | | | |
|----------|---------|--|------------------------------|
| DATE | 12.2.86 | datron <small>ELECTRONICS LTD</small> | |
| DRAWN | LL | | TITLE |
| CHECKED | | | 4700 REF. DIVIDER PCB. ASSY. |
| APPROVED | | | DRAWING NUMBER |
| DATE | | 400652 | SHEET |
| | | | 10 OF 21 |

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No. USED Per Assy. |
|------------|-----------------|---|------------------------|-------------------------|--------------------|
| C24 | 102470 | 47pF 5% 500V CER DISC | ITT | CD10 | 3 |
| C25 | 104026 | 47nf ^{+50%} / _{-20%} 50V CER DISC | SIEMENS | B37449 | - |
| C26 | 102470 | 47pF 5% 500V CER DISC | ITT | CD10 | - |
| C27 | 104026 | 47nf ^{+50%} / _{-20%} 50V CER DISC | SIEMENS | B37449 | - |
| C28 | | NOT USED | | | - |
| C29 | 140016 | 470nf 10% 250V POLYPROP | RIFA | PHE402HFK | - |
| C30 | 102470 | 47pF 5% 500V CER DISC | ITT | CD10 | - |
| C31 | 140016 | 470nf 10% 250V POLYPROP | RIFA | PHE402 HFK | - |
| C32 | 104026 | 47nf ^{+50%} / _{-20%} 50V CER DISC | SIEMENS | B37449 | - |
| C33 | 150020 | 10µF 20% 25V DIP TANT | UNION CARBIDE | K10E25 | 8 |
| C34 | 180015 | 470µF 25V AL. ELECT. | MULLARD | 017-16471 | 1 |
| C35 | 150020 | 10µF 20% 25V DIP TANT | UNION CARBIDE | K10E25 | - |
| C36 | | NOT USED | | | - |
| C37 | | NOT USED | | | - |
| C38 | 110030 | 1nf 20% 100V POLYESTER | WIMA | FKS2 | 3 |
| C39 | 150020 | 10µF 20% 25V DIP TANT | UNION CARBIDE | K10E25 | - |
| C40 | 102270 | 27pF 5% 500V CER DISC | ITT | CD10 | 2 |
| C41 | 140016 | 470nf 10% 250V POLYPROP | RIFA | PHE 402 HFK | - |
| C42 | 140016 | 470nf 10% 250V POLYPROP | RIFA | PHE 402 HFK | - |
| C43 | 140016 | 470nf 10% 250V POLYPROP | RIFA | PHE 402 HFK | - |
| C44 | 140016 | 470nf 10% 250V POLYPROP | RIFA | PHE 402 HFK | - |
| C45 | 102270 | 27pF 5% 500V CER DISC | ITT | CD10 | - |
| C46 | 140016 | 470nf 10% 250V POLYPROP | RIFA | PHE 402 HFK | - |

NOTES.

SEE SHEET 2 FOR LATEST ISSUE

| | | | | | | | | | | | | |
|------|--|--|--|--|--|--|--|--|--|--|--|--|
| ISS | | | | | | | | | | | | |
| ECD | | | | | | | | | | | | |
| DATE | | | | | | | | | | | | |
| CHKD | | | | | | | | | | | | |

| | | | |
|----------|---------|--|------------------------------|
| DATE | 12.2.86 | datron <small>ELECTRONICS LTD</small> | |
| DRAWN | LL | | TITLE |
| CHECKED | | | 4700 REF. DIVIDER PCB. ASSY. |
| APPROVED | | | DRAWING NUMBER |
| DATE | | 400652 | SHEET |
| | | | 10 OF 21 |

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No. USED Per Assy. |
|------------|-----------------|------------------------|------------------------|-------------------------|--------------------|
| D1 | 210027 | 2V7 400mW ZENER | MULLARD | BZY88C2V7 | 4 |
| D2 | 210120 | 12V 400mW ZENER | MULLARD | BZY88C12 | 1 |
| D3 | 210027 | 2V7 400mW ZENER | MULLARD | BZY88C2V7 | - |
| D4 | 210043 | 4V3 400mW ZENER | MULLARD | BZY88C4V3 | 1 |
| D5 | 210027 | 2V7 400mW ZENER | MULLARD | BZY88C2V7 | - |
| D6 | 210027 | 2V7 400mW ZENER | MULLARD | BZY88C2V7 | - |
| D7 | 213009 | 15V 5W ZENER | UNITRODE | TVS 515 | 5 |
| D8 | 213009 | 15V 5W ZENER | UNITRODE | TVS 515 | - |
| D9 | 213009 | 15V 5W ZENER | UNITRODE | TVS 515 | - |
| D10 | 200008 | 200mA 125V LL Si DIODE | FAIRCHILD | IN458A | 1 |
| D11 | 213009 | 15V 5W ZENER | UNITRODE | TVS 515 | - |
| D12 | | NOT USED | | | - |
| D13 | | NOT USED | | | - |
| D14 | 210062 | 6V2 400mW ZENER | MULLARD | BZY88C6V2 | 2 |
| D15 | 210062 | 6V2 400mW ZENER | MULLARD | BZY88C6V2 | - |
| D16 | | NOT USED | | | - |
| D17 | | NOT USED | | | - |
| D18 | 200001 | 75mA 75V GP Si DIODE | FAIRCHILD | IN4148 | 9 |
| D19 | 200001 | 75mA 75V GP Si DIODE | FAIRCHILD | IN4148 | - |
| D20 | 200001 | 75mA 75V GP Si DIODE | FAIRCHILD | IN4148 | - |
| D21 | 200001 | 75mA 75V GP Si DIODE | FAIRCHILD | IN4148 | - |
| D22 | 200001 | 75mA 75V GP Si DIODE | FAIRCHILD | IN4148 | - |
| D23 | 210056 | 5V6 400mW ZENER | MULLARD | BZY88C5V6 | 2 |

NOTES.

SEE SHEET 2 FOR LATEST ISSUE

| ISS | E.C.O. | DATE | CHKD |
|-----|--------|------|------|
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |

| | | | |
|----------|---------|---------------------------------|--------|
| DATE | 12 2 86 | datron ELECTRONICS LTD | |
| DRAWN | | TITLE 4700 REF DIVIDER PCB ASSY | |
| CHECKED | | DRAWING NUMBER | 400652 |
| APPROVED | | SHEET 13 OF 21 | |
| DATE | | | |

W. 1164

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No. USED Per Assy. |
|------------|-----------------|----------------------|------------------------|-------------------------|--------------------|
| D24 | 210056 | 5V6 400mW ZENER | MULLARD | BZY88C5V6 | - |
| D25 | 213006 | 5V 5W ZENER | UNITRODE | TVS 505 | 1 |
| D26 | 200001 | 75mA 75V GP Si DIODE | FAIRCHILD | IN4148 | - |
| D27 | 200001 | 75mA 75V GP Si DIODE | FAIRCHILD | IN4148 | - |
| D28 | 200001 | 75mA 75V GP Si DIODE | FAIRCHILD | IN4148 | - |
| D29 | 213009 | 15V 5W ZENER | UNITRODE | TVS 515 | - |
| D30 | 200001 | 75mA 75V GP Si DIODE | FAIRCHILD | IN4148 | - |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |

NOTES.

SEE SHEET 2 FOR LATEST ISSUE

| ISS | E.C.O. | DATE | CHKD |
|-----|--------|------|------|
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |

| | | | |
|----------|---------|---------------------------------|--------|
| DATE | 12 2 86 | datron ELECTRONICS LTD | |
| DRAWN | | TITLE 4700 REF DIVIDER PCB ASSY | |
| CHECKED | | DRAWING NUMBER | 400652 |
| APPROVED | | SHEET 14 OF 21 | |
| DATE | | | |

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No. USED Per Assy. |
|------------|-----------------|-------------------|------------------------|-------------------------|--------------------|
| Q1 | 250004 | Si PNP TRANSISTOR | NATIONAL | 2N3906/TO18 | 13 |
| Q2 | 240006 | Si NPN | NATIONAL | 2N3904/TO18 | 14 |
| Q3 | 250004 | Si PNP | NATIONAL | 2N3906/TO18 | - |
| Q4 | 240006 | Si NPN | NATIONAL | 2N3904/TO18 | - |
| Q5 | 240006 | Si NPN | NATIONAL | 2N3904/TO18 | - |
| Q6 | 250004 | Si PNP | NATIONAL | 2N3906/TO18 | - |
| Q7 | 240006 | Si NPN | NATIONAL | 2N3904/TO18 | - |
| Q8 | 250004 | Si PNP | NATIONAL | 2N3906/TO18 | - |
| Q9 | 250004 | Si PNP | NATIONAL | 2N3906/TO18 | - |
| Q10 | 240006 | Si NPN | NATIONAL | 2N3904/TO18 | - |
| Q11 | 250004 | Si PNP | NATIONAL | 2N3906/TO18 | - |
| Q12 | 240006 | Si NPN | NATIONAL | 2N3904/TO18 | - |
| Q13 | | NOT USED | | | - |
| Q14 | | NOT USED | | | - |
| Q15 | | NOT USED | | | - |
| Q16 | | NOT USED | | | - |
| Q17 | | NOT USED | | | - |
| Q18 | | NOT USED | | | - |
| Q19 | 240006 | Si NPN | NATIONAL | 2N3904/TO18 | - |
| Q20 | 240006 | Si NPN | NATIONAL | 2N3904/TO18 | - |
| Q21 | 250004 | Si PNP | NATIONAL | 2N3906/TO18 | - |
| Q22 | 240006 | Si NPN | NATIONAL | 2N3904/TO18 | - |
| Q23 | 250004 | Si PNP | NATIONAL | 2N3906/TO18 | - |

NOTES.

SEE SHEET 2 FOR LATEST ISSUE

| | | | | | | | | | | | | | | | | | | | |
|------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ISS | | | | | | | | | | | | | | | | | | | |
| ECD | | | | | | | | | | | | | | | | | | | |
| DATE | | | | | | | | | | | | | | | | | | | |
| CHRD | | | | | | | | | | | | | | | | | | | |

| | | | |
|----------|---------|------------------------|------------------------------|
| DATE | 12.2.86 | datron ELECTRONICS LTD | |
| DRAWN | 11 | | |
| CHECKED | | TITLE | 4700 REF. DIVIDER PCB. ASSY. |
| APPROVED | | DRAWING NUMBER | 400652 |
| DATE | | SHEET | 15 OF 21 |

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No. USED Per Assy. |
|------------|-----------------|-------------------------|------------------------|-------------------------|--------------------|
| Q24 | 240006 | Si NPN TRANSISTOR | NATIONAL | 2N3904/TO18 | - |
| Q25 | 240006 | Si NPN | NATIONAL | 2N3904/TO18 | - |
| Q26 | 250004 | Si PNP | NATIONAL | 2N3906/TO18 | - |
| Q27 | 240006 | Si NPN | NATIONAL | 2N3904/TO18 | - |
| Q28 | 250004 | Si PNP | NATIONAL | 2N3906/TO18 | - |
| Q29 | 230039 | P-CHAN JFET | SILICONIX | J175 | 2 |
| Q30 | 230039 | P-CHAN JFET | SILICONIX | J175 | - |
| Q31 | 230038 | N-CHAN JFET | SILICONIX | J112 | 1 |
| Q32 | * 239037-1 | N-CHAN JFET SEL SET | DATRON (SEE DRG) | J108 (COLOUR) | 1 SET OF 4 |
| Q33 | 230048 | P-CHAN JFET | TELEDYNE | J174 | 2 |
| Q34 | * 239037-1 | N-CHAN JFET SEL SET | DATRON (SEE DRG) | J108 (COLOUR) | - |
| Q35 | * 239037-1 | N-CHAN JFET SEL SET | DATRON (SEE DRG) | J108 (COLOUR) | - |
| Q36 | 230048 | P-CHAN JFET | TELEDYNE | J174 | - |
| Q37 | * 239037-1 | N-CHAN JFET SEL SET | DATRON (SEE DRG) | J108 (COLOUR) | - |
| Q38 | | NOT USED | | | - |
| Q39 | | NOT USED | | | - |
| Q40 | 250004 | Si PNP | NATIONAL | 2N3906/TO18 | - |
| Q41 | 230031 | N-CHAN DUAL JFET | TELEDYNE | SU2656M | 4 |
| Q42 | 230031 | N-CHAN DUAL JFET | TELEDYNE | SU2656M | - |
| Q43 | 250004 | Si PNP | NATIONAL | 2N3906/TO18 | - |
| Q44 | 230031 | N-CHAN DUAL JFET | TELEDYNE | SU2656M | - |
| Q45 | 240006 | Si NPN | NATIONAL | 2N3904/TO18 | - |
| Q46 | 230042 | N-CHAN CURRENT LIM. 3mA | TELEDYNE | 12R 510 | 2 |

NOTES. * THESE 4 FETS MUST HAVE THE SAME COLOUR CODING

SEE SHEET 2 FOR LATEST ISSUE

| | | | | | | | | | | | | | | | | | | | |
|------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ISS | | | | | | | | | | | | | | | | | | | |
| ECD | | | | | | | | | | | | | | | | | | | |
| DATE | | | | | | | | | | | | | | | | | | | |
| CHRD | | | | | | | | | | | | | | | | | | | |

| | | | |
|----------|---------|------------------------|------------------------------|
| DATE | 12.2.86 | datron ELECTRONICS LTD | |
| DRAWN | 11 | | |
| CHECKED | | TITLE | 4700 REF. DIVIDER PCB. ASSY. |
| APPROVED | | DRAWING NUMBER | 400652 |
| DATE | | SHEET | 16 OF 21 |

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No. USED Per Assy. |
|------------|-----------------|------------------------|------------------------|-------------------------|--------------------|
| Q47 | 230042 | N-CHAN CURRENT LIM 3mA | TELEDYNE | TCR510 | — |
| Q48 | 250021 | Si PNP TRANSISTOR | MOTOROLA | BD140 | 1 |
| Q49 | 240031 | Si NPN TRANSISTOR | MOTOROLA | BD139 | 1 |
| Q50 | | NOT USED | | | — |
| Q51 | 230031 | N-CHAN DUAL JFET | TELEDYNE | SU2656M | — |
| Q52 | 250004 | Si PNP TRANSISTOR | NATIONAL | 2N3906/TO18 | — |
| Q53 | 240006 | Si NPN TRANSISTOR | NATIONAL | 2N3904/TO18 | — |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |

NOTES:

SEE SHEET 2 FOR LATEST ISSUE

| ISS | ECD | DATE | CHKD | DATE |
|-----|-----|------|------|------|
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |

| | | | |
|----------|---------|-------------------------------|-----------------------------|
| DATE | 12 2 86 | datron ELECTRONICS LTD | |
| DRAWN | | TITLE | 4700 REF. DIVIDER PCB ASSY. |
| CHECKED | | DRAWING NUMBER | 400652 |
| APPROVED | | SHEET | 17 OF 21 |
| DATE | | | |

V. 1164

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No. USED Per Assy. |
|------------|-----------------|---------------------------|------------------------|-------------------------|--------------------|
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| M1 | 220027 | HIGH CMR OPTO ISOL. | HP | HCPL-2601(5082-4361) | 7 |
| M2 | | NOT USED | | | — |
| M3 | 220027 | HIGH CMR OPTO ISOL. | HP | HCPL-2601(5082-4361) | — |
| M4 | 220017 | 2k5V DUAL OPTO ISOLATOR | FAIRCHILD | FCD 880 | 1 |
| M5 | | NOT USED | | | — |
| M6 | 220027 | HIGH CMR OPTO ISOL. | HP | HCPL-2601(5082-4361) | — |
| M7 | 220027 | HIGH CMR OPTO ISOL. | HP | HCPL-2601(5082-4361) | — |
| M8 | 220027 | HIGH CMR OPTO ISOL. | HP | HCPL-2601(5082-4361) | — |
| M9 | 220027 | HIGH CMR OPTO ISOL. | HP | HCPL-2601(5082-4361) | — |
| M10 | 280068 | DUAL PRECISION MONOSTABLE | MOTOROLA | MC14538 BCP | 1 |
| M11 | 280037 | HEX BUFFER | MOTOROLA | MC14050BCP | 1 |
| M12 | 260025 | 10I OP AMP | NATIONAL | LM101AH | 3 |
| M13 | 280011 | DUAL-D FLIP FLOP | MOTOROLA | MC14013 BCP | 2 |
| M14 | 280009 | HEX INVERTER/BUFFER | MOTOROLA | MC14049 BCP | 1 |
| M15 | 280089 | 8 BIT SHIFT REGISTER | MOTOROLA | MC14094 BCP | 6 |
| M16 | 260025 | 10I OP AMP | NATIONAL | LM101AH | — |
| M17 | | NOT USED | | | — |

NOTES:

SEE SHEET 2 FOR LATEST ISSUE

| ISS | ECD | DATE | CHKD | DATE |
|-----|-----|------|------|------|
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |

| | | | |
|----------|---------|-------------------------------|-----------------------------|
| DATE | 12 2 86 | datron ELECTRONICS LTD | |
| DRAWN | | TITLE | 4700 REF. DIVIDER PCB ASSY. |
| CHECKED | | DRAWING NUMBER | 400652 |
| APPROVED | | SHEET | 18 OF 21 |
| DATE | | | |

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No. USED Per Assy. |
|------------|-----------------|-----------------------------|------------------------|-------------------------|--------------------|
| M18 | 280088 | 8BIT STATIC SHIFT REGISTER | MOTOROLA | MC14021BCP | 2 |
| M19 | 280089 | 8 BIT STATIC SHIFT REGISTER | MOTOROLA | MC14094 BCP | - |
| M20 | 260025 | 101 OP AMP | NATIONAL | LM101AH | - |
| M21 | | NOT USED | | | - |
| M22 | 280088 | 8BIT STATIC SHIFT REGISTER | MOTOROLA | MC14021 BCP | - |
| M23 | 260027 | 714 OP AMP | FAIRCHILD | µA 714 HC | 5 |
| M24 | 280023 | QUAD 21/P NOR GATE | MOTOROLA | MC14001 BCP | 1 |
| M25 | 280089 | 8BIT STATIC SHIFT REGISTER | MOTOROLA | MC14094 BCP | - |
| M26 | 260057 | 5534 OP AMP | SIGNETICS | NE5534N | 2 |
| M27 | 280089 | 8BIT STATIC SHIFT REGISTER | MOTOROLA | MC14094 BCP | - |
| M28 | 260057 | 5534 OP AMP | SIGNETICS | NE5534N | - |
| M29 | 290090 | 7X DARLINGTON DRIVER | SPRAGUE/EXAR | ULN2002A/xR2202CP | 1 |
| M30 | 280089 | 8 BIT STATIC SHIFT REGISTER | MOTOROLA | MC14094 BCP | - |
| M31 | 280089 | 8BIT STATIC SHIFT REGISTER | MOTOROLA | MC14094 BCP | - |
| M32 | 260027 | 714 OP AMP | FAIRCHILD | µA 714 HC | - |
| M33 | 260083 | 1052 CHOPPER AMP | LINEAR TECHNOLOGY | LTC1052CN | 2 |
| M34 | 260027 | 714 OP AMP | FAIRCHILD | µA 714 HC | - |
| M35 | 260027 | 714 OP AMP | FAIRCHILD | µA 714 HC | - |
| M36 | 280106 | HEX LEVEL SHIFTER | MOTOROLA | MC14504 BCP | 1 |
| M37 | 280011 | DUAL D FLIP FLOP | MOTOROLA | MC14013 BCP | - |
| M38 | 260083 | 1052 CHOPPER AMP | LINEAR TECHNOLOGY | LTC1052CN | - |
| M39 | 260027 | 714 OP AMP | FAIRCHILD | µA 714 HC | - |
| M40 | 220027 | HIGH CMR OPTO ISOL. | HP | HCPL-2601 (5082-4361) | - |
| M41 | 290149 | CMOS 555 TIMER | INTERSIL | ICM7555 1PA | 1 |

| | | | | | | | | | | | | | | | |
|------------------------------|--|--|--|--|--|--|--|--|--|--|--|----------|-------------------------------------|------------------------|----------------------------|
| SEE SHEET 2 FOR LATEST ISSUE | | | | | | | | | | | | DATE | 12.2.86 | datron ELECTRONICS LTD | |
| ISS | | | | | | | | | | | | DRAWN | <input checked="" type="checkbox"/> | TITLE | 4700 REF DIVIDER PCB ASSY. |
| ECO | | | | | | | | | | | | CHECKED | | APPROVED | |
| DATE | | | | | | | | | | | | APPROVED | | DRAWING NUMBER | 400652 |
| CHG | | | | | | | | | | | | DATE | | SHEET OF | 21 |

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No. USED Per Assy. |
|------------|-----------------|-----------------------------------|------------------------|-------------------------|--------------------|
| RL1 | 330030 | RELAY 4P N/O | SDS | S4 24V | 2 |
| RL2 | 330030 | RELAY 4P N/O | SDS | S4 24V | - |
| RL3 | | NOT USED | | | - |
| LI-L9 | 370001 | 10 μ H 0.85 Ω RF CHOKE | PLESSEY | 58/10/0011/10 | 9 |
| | | | | | |
| | | | | | |
| TI-T5 | 310002-2 | PULSE TX | NEWPORT | 76616/4 HV | 5 |
| SI | 700070 | SLIDE SWITCH, EXTRA HI. LEVER | APR | 25446A H6 | 1 |
| | 410257-4 | PCB | | | 1 |
| | 540006 | 1/0.4 BLACK PTFE INS. WIRE | | | A/R |
| | 540002 | 22SWG BTC WIRE | | | A/R |
| | 590004 | Ø1.0 PTFE SLEEVE | | | A/R |
| | 602001 | FSV TERMINAL | MOLEX | 02-04-5114 | 14 |
| | 605059 | 8WAY DIL. SOCKET | | | 11 |
| | 605060 | 14WAY DIL. SOCKET | | | 5 |
| | 605061 | 16WAY DIL. SOCKET | | | 13 |
| | 604053 | 4WAY 1" PCB PLUG GD. PL. | MOLEX | 4030-04 AG (825" PINS) | 2 |
| | 612025-1 | STANDOFF M3X5mm BRASS | DATRON | SEE DRAWING. | 1 |

| | | | | | | | | | | | | | | | |
|------------------------------|--|--|--|--|--|--|--|--|--|--|--|----------|-------------------------------------|------------------------|---------------------------|
| NOTES. | | | | | | | | | | | | DATE | 12.2.86 | datron ELECTRONICS LTD | |
| SEE SHEET 2 FOR LATEST ISSUE | | | | | | | | | | | | DRAWN | <input checked="" type="checkbox"/> | TITLE | 400 REF DIVIDER PCB ASSY. |
| ISS | | | | | | | | | | | | CHECKED | | APPROVED | |
| ECO | | | | | | | | | | | | APPROVED | | DRAWING NUMBER | 400652 |
| DATE | | | | | | | | | | | | DATE | | SHEET OF | 21 |
| CHG | | | | | | | | | | | | | | | |

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No. USED Per Assy. |
|------------|-----------------|---|-------------------------|-------------------------|--------------------|
| | 630024 | STANDARD STEATITE INS. BEAD | PARK ROYAL PORCELAIN CO | TYPE No 2 (16SWG) | 20 |
| | 630118 | CIRCUIT BOARD EJECTOR | RICHCO | CBE RED | 2 |
| | 620007 | TEST POINT TERMINAL | MICROVAR | C30 | 32 |
| | 630243 | GLASS BEAD 2.4% _D x0.8% _D | MANSOL (PREFORMS)LTD. | M53638/3 | 46 |
| | 900004 | SILICONE RUBBER COMPOUND. | RS. | 555-588 | A/R. |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |

NOTES.



SEE SHEET 2 FOR LATEST ISSUE

| | | | | | | | | | | | | | | | |
|------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ISS | | | | | | | | | | | | | | | |
| ECD | | | | | | | | | | | | | | | |
| DATE | | | | | | | | | | | | | | | |
| CHKD | | | | | | | | | | | | | | | |

| | | |
|----------|---------|-------------------------------|
| DATE | 12.2.86 | datron ELECTRONICS LTD |
| DRAWN | | |
| CHECKED | | TITLE |
| APPROVED | | 4700 REF DIVIDER PCB. ASSY |
| DATE | | DRAWING NUMBER |
| | | 400652 |
| | | SHEET |
| | | 21 OF 21 |

| DESIG | PART NO | DESCRIPTION | PRINC MANUF | MANUF PART NUMBER | CLASS | QM | QUANTITY | CHANGES |
|-------|----------|-----------------------------|-----------------------|-------------------|-------|----|----------|---------|
| M3 | 260107 | IC LIM OP AMP | PRECISION MONOLITHIC | 940700 | | | EA 2 | |
| M4 | 260107 | IC LIM OP AMP | PRECISION MONOLITHIC | 940700 | | | EA 2 | |
| J1 | 605085 | SOCKET PCB 4 WAY | MOLEX | 02-17-2042 | | | EA 2 | |
| J2 | 605085 | SOCKET PCB 4 WAY | MOLEX | 02-17-2042 | | | EA 2 | |
| | 410420-1 | PCB | | SEE DRG | | | EA 1 | |
| | 450675-1 | INSULATION CAP TOP | | SEE DRG | | | EA 1 | |
| | 450676-1 | INSULATION CAP BOTTOM | | SEE DRG | | | EA 1 | |
| | 540002 | WIRE 1/2" TINNED COPPER | HEATER | 2550 | | | EA 1 | |
| | 602001 | TERMINAL PSM | MOLEX | 02-94-5114 | | | EA 1 | |
| | 612051-1 | STANDOFF M3 X 7 | DATCOM | SEE DRG | | | EA 1 | |
| | 613020 | WASHER M4 SDP | | | | | EA 2 | |
| | 614022-1 | SPACER M3 CLENB X 7 | | SEE DRG | | | EA 2 | |
| | 620007 | TEST POINT TERMINAL | MICROWAP | TYPE 120 | | | EA 1 | |
| | 630024 | BEAD CERAMIC 16 SPS | FARK ROYAL PORCELAIN | MS2 | | | EA 1 | |
| | 630291-1 | EXPANDED FOAM BLOCK OUTER | | SEE DRG | | | EA 2 | |
| | 630292-1 | EXPANDED FOAM BLOCK INNER | | SEE DRG | | | EA 1 | |
| | 630243 | BEAD GLASS 2.4 X 0.81 X 1.8 | MARCONI (PREFORMS) LT | MS163B/3 | | | EA 18 | |


End

| | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-----------------------------|----------------|--|------------------|---|------------------------------|---------------------------|------------------|--------------------|-------------------------------------|--|---------------------------------|--|-----------------|------------------|------------------|-----------------|------------------|------------------|------------------|------------------|------------------|-----------------|------------------|------------------|------------------|--|
| DRAWING No 400536 | | CHKD <i>AK</i> | DATE 17.3.86 | ECO <i>AK</i> | REVISION 1.0 2162 17.3.86 | ISSUE 1.1 2180 10.4.86 | 1.2 2208 15.4.86 | 1.3 2216 17.4.86 | 1.4 2221 18.4.86 | 1.5 2222 18.4.86 | 1.6 2223 18.4.86 | 1.7 2223 16.5.86 | 1.8 2275 9.6.86 | 2.0 2303 23.6.86 | 2.1 2256 25.6.86 | 2.2 2355 8.8.86 | 2.3 2307 13.8.86 | 3.0 2244 20.8.86 | 3.0 2386 30.1.87 | 3.1 2553 23.3.87 | 3.1 2560 26.3.87 | 3.1 2585 1.5.87 | 4.0 2714 3.12.87 | 4.1 2736 15.1.88 | 4.1 2751 29.2.88 | |
| DESCRIPTION | DRAWING NUMBER | SHEET NUMBER | ISSUE - REVISION | | | | | | | | | | | | | | | | | | | | | | | |
| COMPONENT LAYOUT | 480536 | 1 | 1.0 | | | | | | | | | | | | | | | | | | | | | | | |
| SCHEMATIC | 430536 | 1 | 1.0 | | | | | | | | | | | | | | | | | | | | | | | |
| SCHEMATIC | 430536 | 2 | | | | | | | | | | | | | | | | | | | | | | | | |
| SCHEMATIC | 430536 | 3 | | | | | | | | | | | | | | | | | | | | | | | | |
| SCHEMATIC | 430536 | 4 | | | | | | | | | | | | | | | | | | | | | | | | |
| FUNCTIONAL TEST PROC. | 460536/FT | ALL | 1.0 | | | | | | | | | | | | | | | | | | | | | | | |
| FUNC. TEST TICK LIST | 470536/FT | ALL | 1.0 | | | | | | | | | | | | | | | | | | | | | | | |
| P.C.B. | 410258 | 1 | 1.0 | | | | | | | | | | | | | | | | | | | | | | | |
| NOTES | | <input type="checkbox"/> INDICATES NO CHANGE TO DOC AT ISSUE LEVEL CHANGE. | |  | | | | DWN DATE 6.3.86 | CHKD R.K. COGGIN DATE 18/3/86 | APPD  DATE 8.3.86 | TITLE 4700 DC. PCB. ASSY. | DRAWING No. 400536 SHEET 1 OF 18 | | | | | | | | | | | | | | |

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No USED Per Assy. |
|------------|-----------------|------------------------|------------------------|-------------------------|-------------------|
| R1 | 000274 | 270k 5% 1/3W CARBON | | | 2 |
| R2 | 000472 | 4k7 5% 1/3W CARBON | | | 3 |
| R3 | 000274 | 270k 5% 1/3W CARBON | | | - |
| R4 | 019091 | 9k09 1% 1/8W 50ppm MF | HOLCO | H8C | 3 |
| R5 | 011002 | 10k0 1% 1/8W 50ppm MF | HOLCO | H8C | 3 |
| R6 | 000472 | 4k7 5% 1/3W CARBON | | | - |
| R7 | 014992 | 49k9 1% 1/8W 50ppm MF | HOLCO | H8C | 1 |
| R8 | 012212 | 22k1 1% 1/8W 50ppm MF | HOLCO | H8C | 1 |
| R9 | 014322 | 43k2 1% 1/8W 50ppm MF | HOLCO | H8C | 1 |
| R10 | 012742 | 27k4 1% 1/8W 50ppm MF | HOLCO | H8C | 3 |
| R11 | 012742 | 27k4 1% 1/8W 50ppm MF | HOLCO | H8C | - |
| R12 | 000133 | 13k 5% 1/3W CARBON | | | 2 |
| R13 | 012742 | 27k4 1% 1/8W 50ppm MF | HOLCO | H8C | - |
| R14 | 000105 | 1M 5% 1/3W CARBON | | | 2 |
| R15 | 041005 | 10M0 1% 1/2W 100ppm CF | ALLEN BRADLEY | CC | 10 |
| R16 | 041005 | 10M0 1% 1/2W 100ppm CF | ALLEN BRADLEY | CC | - |
| R17 | 090157-1 | GM ATTEN. SET | | SEE DRG | 1 |
| R18 | 000105 | 1M 5% 1/3W CARBON | | | - |
| R19 | 000244 | 240k 5% 1/3W CARBON | | | 1 |
| R20 | 000104 | 100k 5% 1/3W CARBON | | | 4 |
| R21 | 000103 | 10k 5% 1/3W CARBON | | | 5 |
| R22 | 000164 | 160k 5% 1/3W CARBON | | | 1 |
| R23 | 000104 | 100k 5% 1/3W CARBON | | | - |

NOTES

SEE SHEET 2 FOR LATEST ISSUE

| | | |
|----------|---------|--|
| DATE | 27.2.86 |  ELECTRONICS LTD TITLE 4700 DC. PCB. ASSY. DRAWING NUMBER 400536 |
| DRAWN | 11 | |
| CHECKED | | |
| APPROVED | | |
| DATE | | |
| | | SHEET 2 OF 18 |

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | Qty. USED Per Assy. |
|------------|-----------------|------------------------|------------------------|-------------------------|---------------------|
| R24 | 000104 | 100k 5% 1/3W CARBON | | | - |
| R25 | 041005 | 10M0 1% 1/8W 100ppm CF | ALLEN BRADLEY | CC | - |
| R26 | 041005 | 10M0 1% 1/8W 100ppm CF | ALLEN BRADLEY | CC | - |
| R27 | 090157-1 | 6M ATTEN. SET | | SEE DRG. | - |
| R28 | 090159-1 | 1k/111R11 ATTEN SET | | SEE DRG. | 1 |
| R29 | | NOT USED | | | - |
| R30 | 045623 | 562k 1% 1/8W 50ppm MF | ALLEN BRADLEY | CC | 2 |
| R31 | 017500 | 750R1% 1/8W 50ppm MF | HOLCO | H8C | 1 |
| R32 | 045623 | 562k 1% 1/8W 50ppm MF | ALLEN BRADLEY | CC | - |
| R33 | 013161 | 3k16 1% 1/8W 50ppm MF | HOLCO | H8C | 2 |
| R34 | 000153 | 15k 5% 1/3W CARBON | | | 2 |
| R35 | 000153 | 15k 5% 1/3W CARBON | | | - |
| R36 | 000472 | 4k7 5% 1/3W CARBON | | | - |
| R37 | 011001 | 1k00 1% 1/8W 50ppm MF | HOLCO | H8C | 2 |
| R38 | 011001 | 1k00 1% 1/8W 50ppm MF | HOLCO | H8C | - |
| R39 | 013161 | 3k16 1% 1/8W 50ppm MF | HOLCO | H8C | - |
| R40 | 000272 | 2k7 5% 1/3W CARBON | | | 1 |
| R41 | 000273 | 27k 5% 1/3W CARBON | | | 1 |
| R42 | 000155 | 1M5 5% 1/3W CARBON | | | 1 |
| R43 | 041005 | 10M0 1% 1/2W 100ppm CF | ALLEN BRADLEY | CC | - |
| R44 | 041005 | 10M0 1% 1/2W 100ppm CF | ALLEN BRADLEY | CC | - |
| R45 | 090157-1 | 6M ATTEN. SET | | SEE DRG. | - |
| R46 | 000103 | 10k 5% 1/3W CARBON | | | - |

NOTES.

SEE SHEET 2 FOR LATEST ISSUE

| | | | | | | | | | | |
|------|--|--|--|--|--|--|--|--|--|--|
| ISS | | | | | | | | | | |
| ECD | | | | | | | | | | |
| DATE | | | | | | | | | | |
| CHKD | | | | | | | | | | |

| | | |
|-----------------|----------------------------|------------------|
| DATE 25.2.86 | datron ELECTRONICS LTD | |
| DRAWN | TITLE 4700 DC PCB ASSY. | |
| CHECKED | APPROVED | |
| DATE | DRAWING NUMBER 400536 | SHEET 3 OF 18 |

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | Qty. USED Per Assy. |
|------------|-----------------|------------------------|------------------------|-------------------------|---------------------|
| R47 | 000202 | 2k0 5% 1/3W CARBON | | | 2 |
| R48 | 000183 | 18k 5% 1/3W CARBON | | | 1 |
| R49 | 011651 | 1k65 1% 1/8W 50ppm MF | HOLCO | H8C | 1 |
| R50 | 011002 | 10k 1% 1/8W 50ppm MF | HOLCO | H8C | 1 |
| R51 | 018450 | 845R 1% 1/8W 50ppm MF | HOLCO | H8C | 1 |
| R52 | 012002 | 20k 1% 1/8W 50ppm MF | HOLCO | H4C | 1 |
| R53 | 012491 | 2k49 1% 1/8W 50ppm MF | HOLCO | H8C | 1 |
| R54 | 000202 | 2k0 5% 1/3W CARBON | | | - |
| R55 | 012611 | 2k61 1% 1/8W 50ppm MF | HOLCO | H8C | 1 |
| R56 | 011008 | 10R0 1% 1/8W 50ppm MF | HOLCO | H8C | 1 |
| R57 | 000104 | 100k 5% 1/3W CARBON | | | - |
| R58 | 000102 | 1k 5% 1/3W CARBON | | | 2 |
| R59 | 012261 | 2k26 1% 1/8W 50ppm MF | HOLCO | H8C | 2 |
| R60 | 012261 | 2k26 1% 1/8W 50ppm MF | HOLCO | H8C | - |
| R61 | 017501 | 7k50 1% 1/8W 50ppm MF | HOLCO | H8C | 1 |
| R62 | 011002 | 10k0 1% 1/8W 50ppm MF | HOLCO | H8C | - |
| R63 | 018251 | 8k25 1% 1/8W 50ppm MF | HOLCO | H8C | 1 |
| R64 | 046813 | 681k 1% 1/2W 100ppm CF | ALLEN BRADLEY | CC | 2 |
| R65 | 012211 | 2k21 1% 1/8W 50ppm MF | HOLCO | H8C | 2 |
| R66 | 000683 | 68k 5% 1/3W CARBON | | | 2 |
| R67 | 008067 | 100R 5% 1W MF | VISHAY | SI05K | 1 |
| R68 | 017321 | 7k32 1% 1/8W 50ppm MF | HOLCO | H8C | 1 |
| R69 | 012211 | 2k21 1% 1/8W 50ppm MF | HOLCO | H8C | - |

NOTES.

SEE SHEET 2 FOR LATEST ISSUE

| | | | | | | | | | | |
|------|--|--|--|--|--|--|--|--|--|--|
| ISS | | | | | | | | | | |
| ECD | | | | | | | | | | |
| DATE | | | | | | | | | | |
| CHKD | | | | | | | | | | |

| | | |
|-----------------|----------------------------|------------------|
| DATE 25.2.86 | datron ELECTRONICS LTD | |
| DRAWN | TITLE 4700 DC PCB ASSY. | |
| CHECKED | APPROVED | |
| DATE | DRAWING NUMBER 400536 | SHEET 4 OF 18 |

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No. USED Per Assy. |
|------------|-----------------|------------------------|------------------------|-------------------------|--------------------|
| R70 | 046813 | 68k 1% 1/2W 100ppm CF | ALLEN BRADLEY | CC | - |
| R71 | 000683 | 68k 5% 1/3W CARBON | | | - |
| R72 | 000470 | 47R 5% 1/3W CARBON | | | 2 |
| R73 | 000330 | 33R 5% 1/3W CARBON | | | 1 |
| R74 | 041005 | 10M0 1% 1/2W 100ppm CF | ALLEN BRADLEY | CC | - |
| R75 | 041005 | 10M0 1% 1/2W 100ppm CF | | | - |
| R76 | 090157-1 | 6M ATTEN SET | | SEE DRG. | - |
| R77 | 019091 | 9k09 1% 1/8W 50ppm MF | HOLCO | H8C | - |
| R78 | 000470 | 47R 5% 1/3W CARBON | | | - |
| R79 | 000562 | 5k6 5% 1/3W CARBON | | | 1 |
| R80 | 000391 | 390R 5% 1/3W CARBON | | | 1 |
| R81 | 000222 | 2k2 5% 1/3W CARBON | | | 1 |
| R82 | 000133 | 13k 5% 1/3W CARBON | | | - |
| R83 | 050059 | 1M5 1% 2W 100ppm MF | HOLCO | H803RE | 1 |
| R84 | 013011 | 3k01 1% 1/8W 50ppm MF | HOLCO | H8C | 1 |
| R85 | 090157-1 | 1M MATCHED SET | | SEE DRG. | - |
| R86 | 041005 | 10M0 1% 1/2W 100ppm CF | ALLEN BRADLEY | CC | - |
| R87 | 000913 | 91k 5% 1/3W CARBON | | | 1 |
| R88 | 000912 | 9k1 5% 1/3W CARBON | | | 1 |
| R89 | 000102 | 1k 5% 1/3W CARBON | | | - |
| R90 | 041005 | 10M 1% 1/2W 100ppm CF | ALLEN BRADLEY | CC | - |
| R91 | 012001 | 2k00 1% 1/8W 50ppm MF | HOLCO | H8C | 2 |
| R92 | 000393 | 39k 5% 1/3W CARBON | | | 2 |

NOTES:

SEE SHEET 2 FOR LATEST ISSUE

| | | | | | | | | | | | | | | | | | |
|--------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ISS | | | | | | | | | | | | | | | | | |
| E.C.O. | | | | | | | | | | | | | | | | | |
| DATE | | | | | | | | | | | | | | | | | |
| CHKD | | | | | | | | | | | | | | | | | |

| | | |
|----------|---------------------|---------------------------|
| DATE | 25.2.86 | datron ELECTRONICS LTD |
| DRAWN | TITLE | |
| CHECKED | 4700 DC. PCB. ASSY. | |
| APPROVED | | |
| DATE | DRAWING NUMBER | 400536 |
| | SHEET | 5 OF 18 |

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No. USED Per Assy. |
|------------|-----------------|------------------------|------------------------|-------------------------|--------------------|
| R93 | 000152 | 1k5 5% 1/3W CARBON | | | 1 |
| R94 | 011302 | 13k0 1% 1/8W 50ppm MF | HOLCO | H8C | 2 |
| R95 | 000103 | 10k 5% 1/3W CARBON | | | - |
| R96 | 000103 | 10k 5% 1/3W CARBON | | | - |
| R97 | 090001 | PTC THERMISTOR | MULLARD | VA8650 | 1 |
| R98 | 012008 | 20R0 1% 1/8W 50ppm MF | HOLCO | H8C | 1 |
| R99 | 041825 | 18M2 1% 1/2W 100ppm MF | ALLEN BRADLEY | CC | 1 |
| R100 | 041824 | 1M82 1% 1/2W 100ppm MF | ALLEN BRADLEY | CC | 1 |
| R101 | 090157-1 | 6M ATTEN SET (100k) | | SEE DRG. | - |
| R102 | 012001 | 2k00 1% 1/8W 50ppm MF | HOLCO | H8C | - |
| R103 | 011302 | 13k0 1% 1/8W 50ppm MF | HOLCO | H8C | - |
| R104 | 000393 | 39k 5% 1/3W CARBON | | | - |
| R105 | 000473 | 47k 5% 1/3W CARBON | | | 2 |
| R106 | 000473 | 47k 5% 1/3W CARBON | | | - |
| R107 | 050062 | 51R0 1% 1W 250ppm M.O. | WELWYN | MRG | 1 |
| R108 | 021820 | 182R 1% 1/4W 50ppm MF | HOLCO | H4C | 1 |
| R109 | 000512 | 5k1 5% 1/3W CARBON | | | 2 |
| R110 | 000512 | 5k1 5% 1/3W CARBON | | | - |
| R111 | 011000 | 100R 1% 1/8W 50ppm MF | HOLCO | H8C | 2 |
| R112 | 011000 | 100R 1% 1/8W 50ppm MF | HOLCO | H8C | - |
| R113 | 019091 | 9k09 1% 1/8W 50ppm MF | HOLCO | H8C | - |
| R114 | 011002 | 10k0 1% 1/8W 50ppm MF | HOLCO | H8C | - |
| R115 | 019092 | 90k9 1% 1/8W 50ppm MF | HOLCO | H8C | 1 |

NOTES:

SEE SHEET 2 FOR LATEST ISSUE


| | | | | | | | | | | | | | | | | | |
|--------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ISS | | | | | | | | | | | | | | | | | |
| E.C.O. | | | | | | | | | | | | | | | | | |
| DATE | | | | | | | | | | | | | | | | | |
| CHKD | | | | | | | | | | | | | | | | | |

| | | |
|----------|---------------------|---------------------------|
| DATE | 25.2.86 | datron ELECTRONICS LTD |
| DRAWN | TITLE | |
| CHECKED | 4700 DC. PCB. ASSY. | |
| APPROVED | | |
| DATE | DRAWING NUMBER | 400536 |
| | SHEET | 6 OF 18 |

| DESIGNATOR | DATRON PART No | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No | QUANTITY USED |
|------------|----------------|------------------------------|------------------------|------------------------|---------------|
| C24 | 104026 | 47nF $\pm 50\%$ 50V CER DISC | SIEMENS | B37449 | - |
| C25 | 150023 | 33 μ F 20% 25V DIP TANT | UNION CARBIDE | K33E25 | - |
| C26 | 150020 | 10 μ F 20% 25V DIP TANT | UNION CARBIDE | K10E25 | 2 |
| C27 | 150020 | 10 μ F 20% 25V DIP TANT | UNION CARBIDE | K10E25 | - |
| C28 | 110055 | 68nF 10% 100V POLYESTER | WIMA | MKS4 | 1 |
| C29 | 100390 | 39pF 2% 100V CER PLATE | MULLARD | 2222 683 34339 | 1 |
| C30 | 120014 | 2 μ F 20% 63V POLYCARB | ASHCROFT | A28 | 1 |
| C31 | 100560 | 56pF 2% 100V CER PLATE | MULLARD | 2222 683 34563 | 1 |
| C32 | 104026 | 47nF $\pm 50\%$ 50V CER DISC | SIEMENS | B37449 | - |
| C33 | 150023 | 33 μ F 20% 25V DIP TANT | UNION CARBIDE | K33E25 | - |
| C34 | 104026 | 47nF $\pm 50\%$ 50V CER DISC | SIEMENS | B37449 | - |
| C35 | 150023 | 33 μ F 20% 25V DIP TANT | UNION CARBIDE | K33E25 | - |
| C36 | 104026 | 47nF $\pm 50\%$ 50V CER DISC | SIEMENS | B37449 | - |
| C37 | 104026 | 47nF $\pm 50\%$ 50V CER DISC | SIEMENS | B37449 | - |
| C38 | 104026 | 47nF $\pm 50\%$ 50V CER DISC | SIEMENS | B37449 | - |
| C39 | 101103 | 10nF 25% 250V CER DISC | ITT | CD10 | 1 |
| C40 | 140004 | 68nF 10% 400V POLYPROP | WIMA | MKP10 | 1 |
| C41 | 100101 | 100pF 2% 100V CER PLATE | MULLARD | 2222-683-34101 | - |
| C42 | 110051 | 470nF 10% 63V POLYESTER | WIMA | MKS2 | 1 |
| C43 | 100391 | 390pF 10% 100V CER PLATE | MULLARD | 2222-630-19391 | 1 |
| C44 | 100221 | 220pF 2% 100V CER PLATE | MULLARD | 2222-683-58221 | 1 |
| C45 | 100471 | 470pF 10% 100V CER PLATE | MULLARD | 222-630-19471 | 1 |
| C46 | 110042 | 100nF 20% 63V POLYESTER | WIMA | MKS2 | - |

NOTES

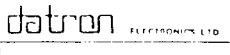
SEE SHEET 2 FOR LATEST ISSUE

| | | |
|----------|---------|---|
| DATE | 25.2.86 |  |
| DRAWN | | |
| CHECKED | | |
| APPROVED | | |
| DATE | | TITLE 4700 DC. PCB. ASSY. |
| | | DRAWING NUMBER 400536 |
| | | SHEET 9 OF 18 |

| DESIGNATOR | DATRON PART No | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No | QUANTITY USED |
|------------|----------------|------------------------------------|------------------------|------------------------|---------------|
| C47 | 110050 | 22nF 10% 63V POLYESTER | WIMA | MKS2 | - |
| C48 | 110050 | 22nF 10% 63V POLYESTER | WIMA | MKS2 | - |
| C49 | 130086 | 30nF 1% 63V POLYSTYRENE | MULLARD | 424 43003 | 1 |
| C50 | 150016 | 1 μ F 20% 35V DIP TANT | UNION CARBIDE | K1RE35 | - |
| C51 | 110042 | 100nF 20% 63V POLYESTER | WIMA | MKS2 | - |
| C52 | 110039 | 470nF 20% 63V POLYESTER | WIMA | MKS2 | 4 |
| C53 | 110039 | 470nF 20% 63V POLYESTER | WIMA | MKS2 | - |
| C54 | 110039 | 470nF 20% 63V POLYESTER | WIMA | MKS2 | - |
| C55 | 110039 | 470nF 20% 63V POLYESTER | WIMA | MKS2 | - |
| C56 | 120036 | 470pF 20% 160V POLYCARB | WIMA | FKC3 | 1 |
| C57 | 100220 | 22pF 2% 100V CER PLATE | MULLARD | 2222-683-34229 | 1 |
| C58 | 150001 | 22 μ F 20% 16V DIP TANT | UNION CARBIDE | K22E16 | 2 |
| C59 | 150001 | 22 μ F 20% 16V DIP TANT | UNION CARBIDE | K22E16 | - |
| C60 | 150002 | 10 μ F 20% 16V DIP TANT | UNION CARBIDE | K10E16 | 2 |
| C61 | 150002 | 10 μ F 20% 16V DIP TANT | UNION CARBIDE | K10E16 | - |
| C62 | 104032 | 220pF 10% 2KV CER DISC | ITT | HD09 | 1 |
| C63 | 110026 | 68nF 20% 100V POLYESTER | WIMA | FKS2 | 1 |
| C64 | 140071 | 470pF 1% 500V GLASS | CORNING ELECTROSIL | CYFM15 | 2 |
| C65 | 104045 | 1 μ F $\pm 20\%$ 50V CER PLATE | MULLARD | CZ30C 105Z | 2 |
| C66 | 104045 | 1 μ F $\pm 30\%$ 50V CER PLATE | MULLARD | CZ30C 105Z | - |
| C67 | 100270 | 27pF 2% 100V CER PLATE | MULLARD | 2222-683-34279 | 1 |
| C68 | 140071 | 470pF 1% 500V GLASS | CORNING ELECTROSIL | CYFM15 | - |

NOTES

SEE SHEET 2 FOR LATEST ISSUE

| | | |
|----------|---------|---|
| DATE | 25.2.86 |  |
| DRAWN | | |
| CHECKED | | |
| APPROVED | | |
| DATE | | TITLE 4700 DC. PCB. ASSY. |
| | | DRAWING NUMBER 400536 |
| | | SHEET 10 OF 18 |

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | Qty. USED Per Assy. |
|------------|-----------------|----------------------|------------------------|-------------------------|---------------------|
| D1 | 213009 | 15V 5W ZENER | UNITRODE | TVS515 | 3 |
| D2 | 213009 | 15V 5W ZENER | UNITRODE | TVS515 | 1 |
| D3 | 200001 | 75mA 75V GP Si DIODE | FAIRCHILD | IN4148 | 10 |
| D4 | 213006 | 5V 5W ZENER | UNITRODE | TVS505 | 4 |
| D5 | 213006 | 5V 5W ZENER | UNITRODE | TVS505 | - |
| D6 | 200001 | 75mA 75V GP Si DIODE | FAIRCHILD | IN4148 | - |
| D7 | 200001 | 75mA 75V GP Si DIODE | FAIRCHILD | IN4148 | - |
| D8 | 213009 | 15V 5W ZENER | UNITRODE | TVS515 | - |
| D9 | 200001 | 75mA 75V GP Si DIODE | FAIRCHILD | IN4148 | - |
| D10 | 200001 | 75mA 75V GP Si DIODE | FAIRCHILD | IN4148 | - |
| D11 | 213006 | 5V 5W ZENER | UNITRODE | TVS505 | - |
| D12 | 213006 | 5V 5W ZENER | UNITRODE | TVS505 | - |
| D13 | 213025 | 3V3 5W ZENER | SIEMENS | IN5333B | 2 |
| D14 | 210033 | 3V3 400mW ZENER | MULLARD | BZY88C3V3 | 3 |
| D15 | 200001 | 75mA 75V GP Si DIODE | FAIRCHILD | IN4148 | - |
| D16 | 200001 | 75mA 75V GP Si DIODE | FAIRCHILD | IN4148 | - |
| D17 | 214014 | 1V22 100ppm ZENER | TELEDYNE | 9491BJ | 6 |
| D18 | 214014 | 1V22 100ppm ZENER | TELEDYNE | 9491BJ | - |
| D19 | 213008 | 24V 5W ZENER | UNITRODE | TVS524 | 2 |
| D20 | 213008 | 24V 5W ZENER | UNITRODE | TVS524 | - |
| D21 | 200002 | 1A 50V GP Si DIODE | FAIRCHILD | IN4001 | 12 |
| D22 | 200002 | 1A 50V GP Si DIODE | FAIRCHILD | IN4001 | - |
| D23 | 200002 | 1A 50V GP Si DIODE | FAIRCHILD | IN4001 | - |

NOTES:

SEE SHEET 2 FOR LATEST ISSUE

| REV | DATE | BY | CHKD | APPD | DATE | BY | CHKD | APPD | DATE |
|-----|------|----|------|------|------|----|------|------|------|
| | | | | | | | | | |
| | | | | | | | | | |
| | | | | | | | | | |
| | | | | | | | | | |
| | | | | | | | | | |
| | | | | | | | | | |
| | | | | | | | | | |
| | | | | | | | | | |
| | | | | | | | | | |
| | | | | | | | | | |

| | | | | | |
|----------|---------|--|----------------|--------------------|--------|
| DATE | 25.2.86 | | TITLE | 4700 DC PCB. ASSY. | |
| DRAWN | | | DRAWING NUMBER | | 400536 |
| CHECKED | | | SHEET | | 11 |
| APPROVED | | | OF | | 18 |
| DATE | | | | | |

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | Qty. USED Per Assy. |
|------------|-----------------|------------------------|------------------------|-------------------------|---------------------|
| D24 | 200002 | 1A 50V GP Si DIODE | FAIRCHILD | IN4001 | - |
| D25 | 213025 | 3V3 5W ZENER | SIEMENS | IN5333B | - |
| D26 | 214014 | 1V22 100ppm ZENER | TELEDYNE | 9491BJ | - |
| D27 | 214014 | 1V22 100ppm ZENER | TELEDYNE | 9491BJ | - |
| D28 | 200001 | 75mA 75V GP Si DIODE | FAIRCHILD | IN4148 | - |
| D29 | 200001 | 75mA 75V GP Si DIODE | FAIRCHILD | IN4148 | - |
| D30 | 213011 | 1V5 250mW ZENER | MULLARD | BZY46-1V5 | 1 |
| D31 | 213001 | 10V 5W ZENER | MOTOROLA | IN5347B | 1 |
| D32 | 200002 | 1A 50V GP Si DIODE | FAIRCHILD | IN4001 | - |
| D33 | 200002 | 1A 50V GP Si DIODE | FAIRCHILD | IN4001 | - |
| D34 | 200002 | 1A 50V GP Si DIODE | FAIRCHILD | IN4001 | - |
| D35 | 200002 | 1A 50V GP Si DIODE | FAIRCHILD | IN4001 | - |
| D36 | 210033 | 3V3 400mW ZENER | MULLARD | BZY88C3V3 | - |
| D37 | 210033 | 3V3 400mW ZENER | MULLARD | BZY88C3V3 | - |
| D38 | 200008 | 200mA 125V LL Si DIODE | FAIRCHILD | IN458A | 2 |
| D39 | 200008 | 200mA 125V LL Si DIODE | FAIRCHILD | IN458A | - |
| D40 | 214014 | 1V22 100ppm ZENER | TELEDYNE | 9491BJ | - |
| D41 | 214014 | 1V22 100ppm ZENER | TELEDYNE | 9491BJ | - |
| D42 | 220020 | FET DIODE 100pA Ir | TELEDYNE | PAD100 | 2 |
| D43 | 220020 | FET DIODE 100pA Ir | TELEDYNE | PAD100 | - |
| D44 | 200002 | 1A 50V GP Si DIODE | FAIRCHILD | IN4001 | - |
| D45 | 200002 | 1A 50V GP Si DIODE | FAIRCHILD | IN4001 | - |
| D46 | 200002 | 1A 50V GP Si DIODE | FAIRCHILD | IN4001 | - |

NOTES:

SEE SHEET 2 FOR LATEST ISSUE

| REV | DATE | BY | CHKD | APPD | DATE | BY | CHKD | APPD | DATE |
|-----|------|----|------|------|------|----|------|------|------|
| | | | | | | | | | |
| | | | | | | | | | |
| | | | | | | | | | |
| | | | | | | | | | |
| | | | | | | | | | |
| | | | | | | | | | |
| | | | | | | | | | |
| | | | | | | | | | |
| | | | | | | | | | |
| | | | | | | | | | |

| | | | | | |
|----------|---------|--|----------------|--------------------|--------|
| DATE | 25.2.86 | | TITLE | 4700 DC PCB. ASSY. | |
| DRAWN | | | DRAWING NUMBER | | 400536 |
| CHECKED | | | SHEET | | 12 |
| APPROVED | | | OF | | 18 |
| DATE | | | | | |

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | QUANTITY |
|------------|-----------------|----------------------|------------------------|-------------------------|----------|
| D47 | 200002 | 1A 50V GP SI DIODE | FAIRCHILD | IN4001 | - |
| D48 | 210062 | 6V2 400mW ZENER | MULLARD | BZY88C6V2 | 2 |
| D49 | 210062 | 6V2 400mW ZENER | MULLARD | BZY88C6V2 | - |
| D50 | 210047 | 4V7 400mW ZENER | MULLARD | BZY88C4V7 | 2 |
| D51 | 210047 | 4V7 400mW ZENER | MULLARD | BZY88C4V7 | - |
| D52 | 200001 | 75mA 75V GP SI DIODE | FAIRCHILD | IN4148 | - |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| Q1 | 230036B | N-CHAN JFET | SILICONIX | J108 | 1 |
| Q2 | 230042 | N-CHAN I LIM 3.0mA | SILICONIX | J509 | 2 |
| Q3 | 230042 | N-CHAN I LIM 3.0mA | SILICONIX | J509 | - |
| Q4 | 240001 | SI NPN TRANSISTOR | NATIONAL | BC184 TO18 | 1 |
| Q5 | 230031 | N-CHAN DUAL JFET | TELEDYNE | U404 | 2 |
| Q6 | 240018 | SI NPN TRANSISTOR | MOTOROLA | MJE340 | 1 |
| Q7 | 250025 | SI PNP TRANSISTOR | MOTOROLA | MJE350 | 1 |

NOTES

SEE SHEET 2 FOR LATEST ISSUE

| | | | | | | | | | | | | | |
|------|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ISS | | | | | | | | | | | | | |
| REQ | | | | | | | | | | | | | |
| DATE | | | | | | | | | | | | | |
| APPD | | | | | | | | | | | | | |

DATE
25.2.86

DRAWN

CHECKED

APPROVED

DATE

datron ELECTRONICS LTD

TITLE
4700 DC PCB ASSY

DRAWING NUMBER 400536

13 SHEET OF 18

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | QUANTITY |
|------------|-----------------|----------------------|------------------------|-------------------------|----------|
| Q8 | 230001 | N-CHAN I LIM 1.4mA | SILICONIX | J506 | 2 |
| Q9 | 230001 | N-CHAN I LIM 1.4mA | SILICONIX | J506 | - |
| Q10 | 230031 | N-CHAN DUAL JFET | SILICONIX | U404 | - |
| | | | | | |
| | | | | | |
| M1 | 260086 | DUAL 2W AUDIO AMP | NATIONAL | LM1877N | 1 |
| M2 | 260042 | 5532 DUAL OP AMP | SIGNETICS | NE5532N | 3 |
| M3 | 280023 | QUAD 2 I/P OR | MOTOROLA | MC14001UBCP | 1 |
| M4 | 280045 | TRIPLE 3 I/P NDR | MOTOROLA | MC14025BCP | 1 |
| M5 | 280079 | QUAD 2 I/P OR | MOTOROLA | MC14071BCP | 2 |
| M6 | 280035 | BCD/DECIMAL DECODER | MOTOROLA | MC14028BCP | 1 |
| M7 | | NOT USED | | | - |
| M8 | | NOT USED | | | - |
| M9 | | NOT USED | | | - |
| M10 | 280079 | QUAD 2 I/P OR | MOTOROLA | MC14071BCP | - |
| M11 | 280009 | HEX INVERTER | MOTOROLA | MC14049UBCP | 1 |
| M12 | 280034 | DUAL MONOSTABLE | MOTOROLA | MC14528BCP | 1 |
| M13 | 260075 | 2903 DUAL COMPARATOR | NATIONAL | LM2903N | 1 |
| M14 | 260042 | 5532 DUAL OP AMP | SIGNETICS | NE5532N | - |
| M15 | 260042 | 5532 DUAL OP AMP | SIGNETICS | NE5532N | - |
| M16 | 260073 | 411 OP AMP | NATIONAL | LF411CN | 1 |
| M17 | 260049 | 319 DUAL COMPARATOR | NATIONAL | LM319N | 1 |

NOTES

SEE SHEET 2 FOR LATEST ISSUE

| | | | | | | | | | | | | | |
|------|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ISS | | | | | | | | | | | | | |
| REQ | | | | | | | | | | | | | |
| DATE | | | | | | | | | | | | | |
| APPD | | | | | | | | | | | | | |

DATE
25.2.86

DRAWN

CHECKED

APPROVED

DATE

datron ELECTRONICS LTD

TITLE
4700 DC PCB ASSY

DRAWING NUMBER 400536

14 SHEET OF 18

| DESIGNATOR | DATRON PART NO. | DESCRIPTION | PRINCIPAL MANUFACTURER | MATERIAL NUMBER'S PART NO. | Qty. USED In Assy |
|------------|-----------------|------------------------|------------------------|----------------------------|-------------------|
| M18 | 260080 | 311 COMPARATOR | NATIONAL | LM311N | 1 |
| M19 | 220027 | HIGH CMR OPTO ISOLATOR | HP | HCPL-2601 (5082-4361) | 1 |
| M20 | 260027 | 714 OP AMP. | FAIRCHILD | μ A 714 HC | 1 |
| M21 | 260082 | 1052 OP AMP. | LINEAR TECH. | LTC 1052 CN8 | 1 |
| M22 | 260081 | 5534A OP AMP. | SIGNETICS | NE5534 AN | 1 |
| M23 | 260059 | 0002 BUFFER AMP | NATIONAL | LH0002 CH | 1 |
| RL1 | 330040 | RELAY 1P 2W | SDS | DS1E-SL-6V | 5 |
| RL2 | 330039 | RELAY 4P N/O | SDS | S4-L-6V | 6 |
| RL3 | 330040 | RELAY 1P 2W | SDS | DS1E-SL-6V | - |
| RL4 | 330039 | RELAY 4P N/O | SDS | S4-L-6V | - |
| RL5 | 330041 | RELAY 2P 2W | SDS | DS2E-SL-6V | 2 |
| RL6 | 330041 | RELAY 2P 2W | SDS | DS2E-SL-6V | - |
| RL7 | 330039 | RELAY 4P N/O | SDS | S4-L-6V | - |
| RL8 | 330042-2 | RELAY 3P N/O ; 1P N/C | | SEE DRG | 1 |
| RL9 | 330038 | RELAY 2P N/O | SDS | S2-L-6V | 3 |
| RL10 | 330039 | RELAY 4P N/O | SDS | S4-L-6V | - |
| RL11 | 330039 | RELAY 4P N/O | SDS | S4-L-6V | - |
| RL12 | 330040 | RELAY 1P 2W | SDS | DS1E-SL-6V | - |

NOTES

SEE SHEET 2 FOR LATEST ISSUE

| | | | |
|-----|------|----|-------------|
| NO. | DATE | BY | DESCRIPTION |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |

| | | | |
|----------|-----------|------------------------|----------|
| DATE | 25. 2. 86 | datron ELECTRONICS LTD | |
| QUANTITY | | TITLE | |
| CHECKED | | 4700 DC PCB ASSY | |
| APPROVED | | DRAWING NUMBER | 400536 |
| DATE | | SHEET | 15 OF 18 |

| DESIGNATOR | DATRON PART NO. | DESCRIPTION | PRINCIPAL MANUFACTURER | MATERIAL NUMBER'S PART NO. | Qty. USED In Assy |
|------------|-----------------|-----------------------------------|------------------------|----------------------------|-------------------|
| RL13 | 330040 | RELAY 1P 2W | SDS | DS1E-SL-6V | - |
| RL14 | 330038 | RELAY 2P N/O | SDS | S2-L-6V | - |
| RL15 | 330030 | RELAY 4P N/O | SDS | S4-24V | 1 |
| RL16 | 330038 | RELAY 2P N/O | SDS | S1-L-6V | - |
| RL17 | 330040 | RELAY 1P 2W | SDS | DS1E-SL-6V | - |
| RL18 | 330039 | RELAY 4P N/O | SDS | S4-L-6V | - |
| L1 | 370001 | 10 μ H 0.85 Ω RF CHOKE | PLESSEY | 58/10/0011/10 | 7 |
| L2 | 370001 | 10 μ H 0.85 Ω RF CHOKE | PLESSEY | 58/10/0011/10 | - |
| L3 | 370001 | 10 μ H 0.85 Ω RF CHOKE | PLESSEY | 58/10/0011/10 | - |
| L4 | 370001 | 10 μ H 0.85 Ω RF CHOKE | PLESSEY | 58/10/0011/10 | - |
| L5 | 370001 | 10 μ H 0.85 Ω RF CHOKE | PLESSEY | 58/10/0011/10 | - |
| L6 | 370012 | 470nH 0.1 Ω RF CHOKE | SIGMA | SC10 | 1 |
| L7 | 370001 | 10 μ H 0.85 Ω RF CHOKE | PLESSEY | 58/10/0011/10 | - |
| L8 | 370001 | 10 μ H 0.85 Ω RF CHOKE | PLESSEY | 58/10/0011/10 | - |
| W1 | 209003 | 1A5 100V BRIDGE RECT. | MICRO-ELECTRONICS | W001 | 1 |

NOTES

SEE SHEET 2 FOR LATEST ISSUE

| | | | |
|-----|------|----|-------------|
| NO. | DATE | BY | DESCRIPTION |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |

| | | | |
|----------|---------|------------------------|----------|
| DATE | 25 2 86 | datron ELECTRONICS LTD | |
| QUANTITY | | TITLE | |
| CHECKED | | 4700 DC PCB ASSY | |
| APPROVED | | DRAWING NUMBER | 400536 |
| DATE | | SHEET | 16 OF 18 |

| DRAWING No 400909 | | TRKD | DATE | ECO | REVISION | ISSUE |
|----------------------|--|----------------|--------------|------------------|----------|-------|
| DOCUMENT LIST | | | | | | |
| DISTRIBUTION | | | | | | |
| PARTS LIST | | | | | | |
| ASSEMBLY DRAWING | | | | | | |
| CIRCUIT DIAGRAM | | | | | | |
| TEST PROCEDURE | | | | | | |
| TEST SPECIFICATION | | | | | | |
| PCB | | | | | | |
| DESCRIPTION | | DRAWING NUMBER | SHEET NUMBER | ISSUE . REVISION | | |
| PARTS LIST | | LP 400909 | 1 | 1.0 1.0 | | |
| ASSEMBLY DRAWING | | DA 400909 | 1 | 1.0 1.0 | | |
| CIRCUIT DIAGRAM | | DC 400909 | 1 | 1.0 1.0 | | |
| | | DC 400909 | 2 | 1.0 1.0 | | |
| | | DC 400909 | 3 | 1.0 1.0 | | |
| TEST PROCEDURE | | PT 400909 | ALL | | | |
| TEST SPECIFICATION | | | | | | |
| PCB | | 410258 | 1 | 2 | | |

NOTES
 DENOTES NO CHANGE TO DOCS AT ISSUE LEVEL CHANGE



DRN D.T. (TRYCO) DATE 20.2.89

CHKD RB DATE 10.3.89

APPR Ruk DATE 13/04/89

TITLE 4708 OUTPUT CONTROL P.C.B ASSY


DRAWING No 400909 SHEET 1 OF 1

DATRAN INSTRUMENTS LTD PARTS LIST 10-Mar-89 DESG: ASSY PCB OUTPUT CONTROL 4708 UPO NO: LP400-03-1 REF: 400909

| DESIG | PART NO | DESCRIPTION | PRINC MANUF | MANUF PART NUMBER | CLASS | QTY | UNIT | DATE |
|-------|---------|---------------------------|-------------|-------------------|-------|-----|------|------|
| R1 | 000274 | RES CF 270K 5% .25W | NEOHM | CFR25 | A | EA | 2 | |
| R2 | 000472 | RES CF 4K7 5% .25W | NEOHM | CFR25 | A | EA | 2 | |
| R3 | 000274 | RES CF 270K 5% .25W | NEOHM | CFR25 | A | EA | 2 | |
| R4 | 019091 | RES MF 9K09 1% .12W 50PPM | HOLSWORTHY | H8C | A | EA | 1 | |
| R5 | 011002 | RES MF 10K0 1% .12W 50PPM | HOLSWORTHY | H8C | A | EA | 1 | |
| R6 | 000472 | RES CF 4K7 5% .25W | NEOHM | CFR25 | A | EA | 2 | |
| R7 | 014992 | RES MF 49K9 1% .12W 50PPM | HOLSWORTHY | H8C | A | EA | 1 | |
| R8 | 012212 | RES MF 22K1 1% .12W 50PPM | HOLSWORTHY | H8C | A | EA | 1 | |
| R9 | 014322 | RES MF 43K2 1% .12W 50PPM | HOLSWORTHY | H8C | A | EA | 1 | |
| R10 | 012742 | RES MF 27K4 1% .12W 50PPM | HOLSWORTHY | H8C | A | EA | 1 | |
| R11 | 012742 | RES MF 27K4 1% .12W 50PPM | HOLSWORTHY | H8C | A | EA | 1 | |
| R12 | 000133 | RES CF 13K 5% .25W | NEOHM | CFR25 | A | EA | 2 | |
| R13 | 012742 | RES MF 27K4 1% .12W 50PPM | HOLSWORTHY | H8C | A | EA | 1 | |
| R14 | 000105 | RES CF 1M0 5% .25W | NEOHM | CFR21 | A | EA | 1 | |
| R18 | 000105 | RES CF 1M0 5% .25W | NEOHM | CFR25 | A | EA | 1 | |
| R19 | 000244 | RES CF 240K 5% .25W | NEOHM | CFR25 | A | EA | 1 | |
| R20 | 000104 | RES CF 100K 5% .25W | NEOHM | CFR25 | A | EA | 1 | |
| R21 | 000103 | RES CF 10K 5% .25W | NEOHM | CFR25 | A | EA | 1 | |
| R22 | 000164 | RES CF 160K 5% .25W | NEOHM | CFR25 | A | EA | 1 | |
| R23 | 000104 | RES CF 100K 5% .25W | NEOHM | CFR25 | A | EA | 1 | |
| R24 | 000104 | RES CF 100K 5% .25W | NEOHM | CFR25 | A | EA | 1 | |
| R61 | 017501 | RES MF 7K50 1% .12W 50PPM | HOLSWORTHY | H8C | A | EA | 1 | |
| R62 | 011002 | RES MF 10K0 1% .12W 50PPM | HOLSWORTHY | H8C | A | EA | 1 | |
| R63 | 018251 | RES MF 9K25 1% .12W 50PPM | HOLSWORTHY | H8C | A | EA | 1 | |
| R64 | 046813 | RES MF 681K 1% .12W 50PPM | HOLSWORTHY | H8C | A | EA | 1 | |
| R65 | 012211 | RES MF 22K1 1% .12W 50PPM | HOLSWORTHY | H8C | A | EA | 1 | |
| R66 | 000683 | RES CF 68K 5% .25W | NEOHM | CFR25 | A | EA | 1 | |
| R68 | 017321 | RES MF 7K32 1% .12W 50PPM | HOLSWORTHY | H8C | A | EA | 1 | |
| R69 | 012211 | RES MF 22K1 1% .12W 50PPM | HOLSWORTHY | H8C | A | EA | 1 | |
| R70 | 046813 | RES MF 681K 1% .12W 50PPM | HOLSWORTHY | H8C | A | EA | 1 | |
| R71 | 000683 | RES CF 68K 5% .25W | NEOHM | CFR25 | A | EA | 1 | |
| R72 | 000472 | RES CF 47R 5% .25W | NEOHM | CFR25 | A | EA | 1 | |
| R78 | 000470 | RES CF 47R 5% .25W | NEOHM | CFR25 | A | EA | 1 | |
| R79 | 000562 | RES CF 5K6 5% .25W | NEOHM | CFR21 | A | EA | 1 | |
| R80 | 000391 | RES CF 390R 5% .25W | NEOHM | CFR21 | A | EA | 1 | |
| R81 | 000222 | RES CF 2K2 5% .25W | NEOHM | CFR25 | A | EA | 1 | |
| R82 | 000133 | RES CF 13K 5% .25W | NEOHM | CFR25 | A | EA | 1 | |
| R83 | 050059 | RES TF 1M5 1% 2W 15K V | NEOHM | CFR21 | A | EA | 1 | |
| R84 | 013511 | RES MF 35K1 1% .12W 50PPM | HOLSWORTHY | H8C | A | EA | 1 | |
| R87 | 090001 | THERMISTOR PTC 50K | NEOHM | CFR21 | A | EA | 1 | |
| R99 | 012008 | RES MF 20R0 1% .12W 50PPM | HOLSWORTHY | H8C | A | EA | 1 | |
| R107 | 050060 | RES MO 51R 1% .1W | NEOHM | CFR21 | A | EA | 1 | |
| R108 | 021820 | RES MF 182R 1% .2W 50PPM | HOLSWORTHY | H8C | A | EA | 1 | |
| R121 | 000221 | RES CF 220R 5% .25W | NEOHM | CFR21 | A | EA | 1 | |
| R123 | 000474 | RES CF 470K 5% .25W | NEOHM | CFR21 | A | EA | 1 | |

| DESIG | PART NO | DESCRIPTION | FRING MANUF | MATERIAL NUMBER | CLASS | QTY | UNIT | QTY | UNIT |
|-------|---------|----------------------------|--------------------------|-----------------|-------|-----|------|-----|------|
| | 63004 | BEAD CERAMIC 1/8 DIA | LABE ROYAL PORCELAIN LTD | | EA | 10 | | | |
| | 63006 | BEAD CERAMIC 1/8 DIA | LABE ROYAL PORCELAIN LTD | | EA | 10 | | | |
| | 63011 | FOR MOTOR CRANK | RICHM | CBE | EA | 1 | | | |
| | 63023 | BEAD GLASS 1/4 X 1/8 X 1/8 | MANS L (PREFORMS) LTD | MFG-1 | EA | 1 | | | |

End


| | | | | | | | | | | | | | | | | | | | |
|-----------------------------|-----------|----------------|---|-------------------|------------------|---|------------------|------------------|------------------|------------------|------------------|---------------------------|------------------|-------------------|-------------------|-------------------|-------------------|-------------------|--|
| DRAWING NO 400446 | | CHKD | 8-0 1958 5.7.85 | 8-1 2045 29.10.85 | 9-0 2168 20.3.86 | 9-1 2283 5.6.86 | 9-1 2404 4.11.87 | 9-2 2386 23/1/87 | 9-3 2497 23/1/87 | 9-4 2561 25/5/87 | 10-0 2650 4.2.87 | 10-1 2650 19.8.87 | 10-1 2775 6.5.88 | 10-3 2902 19.5.88 | 10-4 2946 22.5.88 | 10-5 2987 16.8.88 | 10-6 3006 23.8.88 | 11-0 3287 20.3.89 | |
| DATE | | ECO | | | | | | | | | | | | | | | | | |
| REVISION | | ISSUE | | | | | | | | | | | | | | | | | |
| DESCRIPTION | | DRAWING NUMBER | SHEET NUMBER | ISSUE - REVISION | | | | | | | | | | | | | | | |
| COMPONENT LAYOUT | 480446 | 1 | 8-0 | | | | | | | | | | | | | | | | |
| L.P. | 400446 | ALL | | | | | | | | | | | | | | | | | |
| SCHEMATIC | 430446 | 1 | 8-0 | 8-0 | 8-0 | 8-0 | 8-0 | 8-0 | 8-0 | 8-0 | 8-0 | 8-0 | 8-0 | 8-0 | 8-0 | 8-0 | 8-0 | 8-0 | |
| SCHEMATIC | 430446 | 2 | | | | | | | | | | | | | | | | | |
| SCHEMATIC | 430446 | 3 | | | | | | | | | | | | | | | | | |
| SCHEMATIC | 430446 | 4 | | | | | | | | | | | | | | | | | |
| SCHEMATIC | 430446 | 5 | | | | | | | | | | | | | | | | | |
| FUNCTIONAL TEST PROC. | 460446/FT | 1-7 | 8-0 | | | | | | | | | | | | | | | | |
| FUNC. TEST TICK LIST | 470446/FT | 1 | 8-0 | | | | | | | | | | | | | | | | |
| NOTES | | | INDICATES NO CHANGE TO DOCS AT ISSUE LEVEL CHANGE | | |  | | | DRN | CHKD | APP | TITLE | | | DRAWING NO | | | | |
| | | | | | | | | | 11 | 130 | 57 | 4200 SINE SOURCE PCB ASSY | | | 400446 | | | | |
| | | | | | | | | | DATE | DATE | DATE | | | | SHEET 1 OF 27 | | | | |
| | | | | | | | | | 5.7.85 | 10.7.85 | 23.7.85 | | | | | | | | |

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No. USED Per Assy. |
|------------|-----------------|-----------------------|------------------------|-------------------------|--------------------|
| R1 | 019091 | 9k09 1% 1/8W 50ppm MF | HOLCO | H8C | 1 |
| R2 | 011821 | 1k82 1% 1/8W 50ppm MF | HOLCO | H8C | 1 |
| R3 | 012151 | 2k15 1% 1/8W 50ppm MF | HOLCO | H8C | 1 |
| R4 | 012611 | 2k61 1% 1/8W 50ppm MF | HOLCO | H8C | 1 |
| R5 | 000223 | 22k 5% 1/3W CARBON | MULLARD | CR25 | 1 |
| R6 | 000222 | 2k2 5% 1/3W CARBON | MULLARD | CR25 | 1 |
| R7 | 011502 | 15k 1% 1/8W 50ppm MF | HOLCO | H8C | 2 |
| R8 | 014321 | 4k32 1% 1/8W 50ppm MF | HOLCO | H8C | 2 |
| R9 | 011002 | 10k 1% 1/8W 50ppm MF | HOLCO | H8C | 7 |
| R10 | 000100 | 10R 5% 1/3W CARBON | MULLARD | CR25 | 6 |
| R11 | 000101 | 100R 5% 1/3W CARBON | MULLARD | CR25 | 10 |
| R12 | 000470 | 47R 5% 1/3W CARBON | MULLARD | CR25 | 9 |
| R13 | 011502 | 15k0 1% 1/8W 50ppm MF | HOLCO | H8C | - |
| R14 | 000272 | 2k7 5% 1/3W CARBON | MULLARD | CR25 | 2 |
| R15 | 000103 | 10k 5% 1/3W CARBON | MULLARD | CR25 | 8 |
| R16 | 000228 | 2R2 5% 1/3W CARBON | MULLARD | CR25 | 1 |
| R17 | 000100 | 10R 5% 1/3W CARBON | MULLARD | CR25 | - |
| R18 | 000152 | 1k5 5% 1/3W CARBON | MULLARD | CR25 | 4 |
| R19 | 000472 | 4k7 5% 1/3W CARBON | MULLARD | CR25 | 4 |
| R20 | 000103 | 10k 5% 1/3W CARBON | MULLARD | CR25 | - |
| R21 | 000103 | 10k 5% 1/3W CARBON | MULLARD | CR25 | - |
| R22 | 000123 | 12k 5% 1/3W CARBON | MULLARD | CR25 | 1 |
| R23 | 000122 | 1k2 5% 1/3W CARBON | MULLARD | CR25 | 2 |

NOTES

SEE SHEET 1 FOR LATEST ISSUE

| | | | | | | | | |
|------|---------|----------|----------|----------|---------|--------|---------|--------|
| ISS | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
| LCD | | 1725 | 1742 | 1770 | 1780 | 1801 | 1827 | 1839 |
| DATE | 26.9.84 | 10.10.84 | 31.10.84 | 22.11.84 | 4.12.84 | 2.1.85 | 13.2.85 | 9.4.85 |
| CHKD | | SD | MS | MS | MD | MP | MP | MP |

| | | | |
|----------|-------------|---|---------------------------|
| DATE | 24.7.84 |  | |
| DRAWN | | | |
| CHECKED | K.K. COGGAN | TITLE | 4200 SINE SOURCE PCB ASSY |
| APPROVED | ST | DRAWING NUMBER | 400446 |
| DATE | 29.9.84 | SHEET | 2 OF 27 |

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No USED Per Assy. |
|------------|-----------------|----------------------------|------------------------|-------------------------|-------------------|
| R24 | 000332 | 3k3 5% 1/3W CARBON | MULLARD | CR25 | 1 |
| R25 | 000102 | 1k 5% 1/3W CARBON | MULLARD | CR25 | 5 |
| R26 | 000272 | 2k7 5% 1/3W CARBON | MULLARD | CR25 | - |
| R27 | 011001 | 1k 1% 1/8W 50ppm MF | HOLCO | H8C | 2 |
| R28 | 012001 | 2k 1% 1/8W 50ppm MF | HOLCO | H8C | 1 |
| R29 | 011001 | 1k 1% 1/8W 50ppm MF | HOLCO | H8C | - |
| R30 | 047153 | 715k 1% 1/2W 100ppm CF | ALLEN BRADLEY | CC | 2 |
| R31 | 013573 | 357k 1% 1/8W 50ppm MF | HOLCO | H8C | 2 |
| R32 | 011783 | 178k 1% 1/8W 50ppm MF | HOLCO | H8C | 2 |
| R33 | 018872 | 88k7 1% 1/8W 50ppm MF | HOLCO | H8C | 2 |
| R34 | 014422 | 44k2 1% 1/8W 50ppm MF | HOLCO | H8C | 2 |
| R35 | 012262 | 22k6 1% 1/8W 50ppm MF | HOLCO | H8C | 2 |
| R36 | 011132 | 11k3 1% 1/8W 50ppm MF | HOLCO | H8C | 2 |
| R37 | 015621 | 5k62 1% 1/8W 50ppm MF | HOLCO | H8C | 2 |
| R38 | 012801 | 2k8 1% 1/8W 50ppm MF | HOLCO | H8C | 2 |
| R39 | 000152 | 1k5 5% 1/3W CARBON | MULLARD | CR25 | - |
| R40 | 000152 | 1k5 5% 1/3W CARBON | MULLARD | CR25 | - |
| R41 | | FSV (PART OF KIT WITH Q29) | | | - |
| R42 | 000103 | 10k 5% 1/3W CARBON | MULLARD | CR25 | - |
| R43 | 000103 | 10k 5% 1/3W CARBON | MULLARD | CR25 | - |
| R44 | 000102 | 1k 5% 1/3W CARBON | MULLARD | CR25 | - |
| R45 | 000102 | 1k 5% 1/3W CARBON | MULLARD | CR25 | - |
| R46 | 000221 | 220R 5% 1/3W CARBON | MULLARD | CR25 | 4 |

| | | | |
|------------------------------|-----------------|-------------------------------------|---------------|
| NOTES | DATE 24.7.84 | datron ELECTRONICS LTD | |
| SEE SHEET 2 FOR LATEST ISSUE | DRAWN L | TITLE 4200 SINE SOURCE PCB ASSY. | |
| ISS | CHECKED | DRAWING NUMBER 400446 | 3 SHEET OF 27 |
| ISS | APPROVED | | |
| ISS | DATE | | |

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No USED Per Assy. |
|------------|-----------------|------------------------|------------------------|-------------------------|-------------------|
| R47 | 001182 | 1k8 5% 1/2W CARBON | MULLARD | CR37 | 2 |
| R48 | 011823 | 182k 1% 1/8W 50ppm MF | HOLCO | H8C | 1 |
| R49 | 067503 | 50k POT 20 TURN CERMET | BECKMAN | 68X | 2 |
| R50 | 067503 | 50k POT 20 TURN CERMET | BECKMAN | 68X | - |
| R51 | 014990 | 499R 1% 1/8W 50ppm MF | HOLCO | H8C | 2 |
| R52 | 063100 | 10R POT 3/8 SQ CERMET | BECKMAN | 72P | 1 |
| R53 | 014751 | 4k75 1% 1/8W 50ppm MF | HOLCO | H8C | 3 |
| R54 | 012218 | 22R1 1% 1/8W 50ppm MF | HOLCO | H8C | 1 |
| R55 | 047153 | 715k 1% 1/2W 100ppm CF | ALLEN BRADLEY | CC | - |
| R56 | 013573 | 357k 1% 1/8W 50ppm MF | HOLCO | H8C | - |
| R57 | 011783 | 178k 1% 1/8W 50ppm MF | HOLCO | H8C | - |
| R58 | 018872 | 88k7 1% 1/8W 50ppm MF | HOLCO | H8C | - |
| R59 | 014422 | 44k2 1% 1/8W 50ppm MF | HOLCO | H8C | - |
| R60 | 012262 | 22k6 1% 1/8W 50ppm MF | HOLCO | H8C | - |
| R61 | 011132 | 11k3 1% 1/8W 50ppm MF | HOLCO | H8C | - |
| R62 | 015621 | 5k62 1% 1/8W 50ppm MF | HOLCO | H8C | - |
| R63 | 012801 | 2k8 1% 1/8W 50ppm MF | HOLCO | H8C | - |
| R64 | 013321 | 3k32 1% 1/8W 50ppm MF | HOLCO | H8C | 2 |
| R65 | 013321 | 3k32 1% 1/8W 50ppm MF | HOLCO | H8C | - |
| R66 | 000103 | 10k 5% 1/3W CARBON | MULLARD | CR25 | - |
| R67 | 000103 | 10k 5% 1/3W CARBON | MULLARD | CR25 | - |
| R68 | 011002 | 10k 1% 1/8W 50ppm MF | HOLCO | H8C | - |
| R69 | 011002 | 10k 1% 1/8W 50ppm MF | HOLCO | H8C | - |

| | | | |
|------------------------------|-----------------|-------------------------------------|---------------|
| NOTES | DATE 24.7.84 | datron ELECTRONICS LTD | |
| SEE SHEET 2 FOR LATEST ISSUE | DRAWN L | TITLE 4200 SINE SOURCE PCB ASSY. | |
| ISS | CHECKED | DRAWING NUMBER 400446 | 4 SHEET OF 27 |
| ISS | APPROVED | | |
| ISS | DATE | | |

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No. USED Per Assy. |
|------------|-----------------|-----------------------|------------------------|-------------------------|--------------------|
| R70 | 011501 | 1k5 1% 1/8W 50ppm MF | HOLCO | H8C | 2 |
| R71 | 011501 | 1k5 1% 1/8W 50ppm MF | HOLCO | H8C | - |
| R72 | 000102 | 1k 5% 1/3W CARBON | MULLARD | CR25 | - |
| R73 | 000102 | 1k 5% 1/3W CARBON | MULLARD | CR25 | - |
| R74 | 012743 | 274k 1% 1/8W 50ppm MF | HOLCO | H8C | 1 |
| R75 | 014990 | 499R 1% 1/8W 50ppm MF | HOLCO | H8C | - |
| R76 | 000221 | 220R 5% 1/3W CARBON | MULLARD | CR25 | - |
| R77 | 001182 | 1k8 5% 1/2W CARBON | MULLARD | CR37 | - |
| R78 | 000103 | 10k 5% 1/3W CARBON | MULLARD | CR25 | - |
| R79 | 012551 | 2k55 1% 1/8W 50ppm MF | HOLCO | H8C | 2 |
| R80 | 012551 | 2k55 1% 1/8W 50ppm MF | HOLCO | H8C | - |
| R81 | 000822 | 8k2 5% 1/3W CARBON | MULLARD | CR25 | 5 |
| R82 | 000822 | 8k2 5% 1/3W CARBON | MULLARD | CR25 | - |
| R83 | 000822 | 8k2 5% 1/3W CARBON | MULLARD | CR25 | - |
| R84 | 000822 | 8k2 5% 1/3W CARBON | MULLARD | CR25 | - |
| R85 | 000152 | 1k5 5% 1/3W CARBON | MULLARD | CR25 | - |
| R86 | 000433 | 43k 5% 1/3W CARBON | MULLARD | CR25 | 1 |
| R87 | 000822 | 8k2 5% 1/3W CARBON | MULLARD | CR25 | - |
| R88 | 000471 | 470R 5% 1/3W CARBON | MULLARD | CR25 | 4 |
| R89 | 000362 | 3k6 5% 1/3W CARBON | MULLARD | CR25 | 2 |
| R90 | 000470 | 47R 5% 1/3W CARBON | MULLARD | CR25 | - |
| R91 | 013161 | FSV (3k16 1% NOM) | HOLCO | H8C | 2 |
| R92 | 000122 | 1k2 5% 1/3W CARBON | MULLARD | CR25 | - |

NOTES

SEE SHEET 2 FOR LATEST ISSUE

| | |
|------|--|
| ISS | |
| EC'D | |
| DATE | |
| CHKD | |

| | |
|----------|---------|
| DATE | 24.7.84 |
| DRAWN | L |
| CHECKED | |
| APPROVED | |
| DATE | |

| | |
|----------------------------|--------|
| datron ELECTRONICS LTD | |
| TITLE | |
| 4200 SINE SOURCE PCB ASSY. | |
| DRAWING NUMBER | 400446 |
| SHEET | 5 |
| OF | 27 |

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No. USED Per Assy. |
|------------|-----------------|-----------------------|------------------------|-------------------------|--------------------|
| R93 | 000470 | 47R 5% 1/3W CARBON | MULLARD | CR25 | - |
| R94 | 000470 | 47R 5% 1/3W CARBON | MULLARD | CR25 | - |
| R95 | 000470 | 47R 5% 1/3W CARBON | MULLARD | CR25 | - |
| R96 | 011872 | 18k7 1% 1/8W 50ppm MF | HOLCO | H8C | 2 |
| R97 | 000104 | 100k 5% 1/3W CARBON | MULLARD | CR25 | 2 |
| R98 | 011378 | 13R7 1% 1/8W 50ppm MF | HOLCO | H8C | 2 |
| R99 | 000104 | 100k 5% 1/3W CARBON | MULLARD | CR25 | - |
| R100 | 011872 | 18k7 1% 1/8W 50ppm MF | HOLCO | H8C | - |
| R101 | 011378 | 13R7 1% 1/8W 50ppm MF | HOLCO | H8C | - |
| R102 | 000471 | 470R 5% 1/3W CARBON | MULLARD | CR25 | - |
| R103 | 013091 | 3k09 1% 1/8W 50ppm MF | HOLCO | H8C | 2 |
| R104 | 011541 | 1k54 1% 1/8W 50ppm MF | HOLCO | H8C | 2 |
| R105 | 011541 | 1k54 1% 1/8W 50ppm MF | HOLCO | H8C | - |
| R106 | 013091 | 3k09 1% 1/8W 50ppm MF | HOLCO | H8C | - |
| R107 | 000470 | 47R 5% 1/3W CARBON | MULLARD | CR25 | 4 |
| R108 | 017871 | 7k87 1% 1/8W 50ppm MF | HOLCO | H8C | 1 |
| R109 | 000101 | 100R 5% 1/3W CARBON | MULLARD | CR25 | - |
| R110 | 000225 | 2M210% 1/3W CARBON | MULLARD | CR25 | 1 |
| R111 | | NOT USED | | | - |
| R112 | 000100 | 10R 5% 1/3W CARBON | MULLARD | CR25 | - |
| R113 | 000362 | 3k6 5% 1/3W CARBON | MULLARD | CR25 | - |
| R114 | 000470 | 47R 5% 1/3W CARBON | MULLARD | CR25 | - |
| R115 | 000470 | 47R 5% 1/3W CARBON | MULLARD | CR25 | - |

NOTES

SEE SHEET 2 FOR LATEST ISSUE

| | |
|------|--|
| ISS | |
| EC'D | |
| DATE | |
| CHKD | |

| | |
|----------|---------|
| DATE | 24.7.84 |
| DRAWN | L |
| CHECKED | |
| APPROVED | |
| DATE | |

| | |
|---------------------------|--------|
| datron ELECTRONICS LTD | |
| TITLE | |
| 4200 SINE SOURCE PCB ASSY | |
| DRAWING NUMBER | 400446 |
| SHEET | 6 |
| OF | 27 |

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No. USED Per Assy |
|------------|-----------------|-----------------------------|------------------------|-------------------------|-------------------|
| R116 | 000470 | 47R 5% 1/8W CARBON | MULLARD | CR25 | - |
| R117 | 000101 | 100R 5% 1/8W CARBON | MULLARD | CR25 | - |
| R118 | 012432 | 24k3 1% 1/8W 50ppm MF | HOLCO | H8C | 2 |
| R119 | 012432 | 24k3 1% 1/8W 50ppm MF | HOLCO | H8C | - |
| R120 | 011002 | 10K 1% 1/8W 50ppm MF | HOLCO | H8C | - |
| R121 | 017501 | 7K5 1% 1/8W 50ppm MF | HOLCO | H8C | 1 |
| R122 | 011002 | FSV (10K 1% NOM) | HOLCO | H8C | - |
| R123 | 068103 | 10K POT 3/8 SQ VERT CERMIET | BECKMAN | 72XW | 1 |
| R124 | 000100 | 10R 5% 1/3W CARBON | MULLARD | CR25 | - |
| R125 | 000100 | 10R 5% 1/3W CARBON | MULLARD | CR25 | - |
| R126 | 001182 | 1K8 5% 1/2W CARBON | MULLARD | CR37 | 2 |
| R127 | 000101 | 100R 5% 1/3W CARBON | MULLARD | CR25 | - |
| R128 | 000101 | 100R 5% 1/3W CARBON | MULLARD | CR25 | - |
| R129 | 011211 | 1K21 1% 1/8W 50ppm MF | HOLCO | H8C | 1 |
| R130 | 011002 | 10K 1% 1/8W 50ppm MF | HOLCO | H8C | - |
| R131 | 011002 | 10K 1% 1/8W 50ppm MF | HOLCO | H8C | - |
| R132 | 000101 | 100R 5% 1/3W CARBON | MULLARD | CR25 | - |
| R133 | 001182 | 1K8 5% 1/2W CARBON | MULLARD | CR37 | - |
| R134 | 014321 | 4k32 1% 1/8W 50ppm MF | HOLCO | H8C | - |
| R135 | 012491 | 2k49 1% 1/8W 50ppm MF | HOLCO | H8C | 2 |
| R136 | 090063 | PTC THERMISTOR | TEXAS | TSPI02K | 2 |
| R137 | 090063 | PTC THERMISTOR | TEXAS | TSPI02K | - |
| R138 | 000101 | 100R 5% 1/3W CARBON | MULLARD | CR25 | - |

NOTES

SEE SHEET 2 FOR LATEST ISSUE

| | | | | | | | | | | | | | | | | | | |
|----------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| NO. | | | | | | | | | | | | | | | | | | |
| DATE | | | | | | | | | | | | | | | | | | |
| BY | | | | | | | | | | | | | | | | | | |
| CHECKED | | | | | | | | | | | | | | | | | | |
| APPROVED | | | | | | | | | | | | | | | | | | |
| DATE | | | | | | | | | | | | | | | | | | |

| | | | |
|----------|---------|------------------------------------|--------|
| DATE | 24.7.84 | datron ELECTRONICS LTD | |
| DRAWN | IL | TITLE 4200 SINE SOURCE PCB ASSY | |
| CHECKED | | DRAWING NUMBER | 400446 |
| APPROVED | | SHEET | 7 |
| DATE | | OF | 26 |

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No. USED Per Assy |
|------------|-----------------|-----------------------|------------------------|-------------------------|-------------------|
| R139 | 000100 | 10R 5% 1/3W CARBON | MULLARD | CR25 | - |
| R140 | 000202 | 2K 5% 1/3W CARBON | MULLARD | CR25 | 1 |
| R141 | 000101 | 100R 5% 1/3W CARBON | MULLARD | CR25 | - |
| R142 | 000101 | 100R 5% 1/3W CARBON | MULLARD | CR25 | - |
| R143 | 012491 | 2k49 1% 1/8W 50ppm MF | HOLCO | H8C | - |
| R144 | 011003 | 10R 1% 1/8W 50ppm MF | HOLCO | H8C | 1 |
| R145 | 000221 | 220R 5% 1/3W CARBON | MULLARD | CR25 | - |
| R146 | 000221 | 220R 5% 1/3W CARBON | MULLARD | CR25 | - |
| R147 | 000101 | 100R 5% 1/3W CARBON | MULLARD | CR25 | - |
| R148 | 000278 | 2R7 5% 1/3W CARBON | MULLARD | CR25 | 1 |
| R149 | 013161 | FSV (3K16 1% NOM) | HOLCO | H8C | - |
| R150 | 000471 | 470R 5% 1/3W CARBON | MULLARD | CR25 | - |
| R151 | 014751 | 4k75 1% 1/8W 50ppm MF | HOLCO | H8C | - |
| R152 | 015230 | 523R 1% 1/8W 50ppm MF | HOLCO | H8C | 1 |
| R153 | 014320 | 432R 1% 1/8W 50ppm MF | HOLCO | H8C | 1 |
| R154 | 014751 | 4k75 1% 1/8W 50ppm MF | HOLCO | H8C | - |
| R155 | 000472 | 4K7 5% 1/3W CARBON | MULLARD | CR25 | - |
| R156 | 000472 | 4K7 5% 1/3W CARBON | MULLARD | CR25 | - |
| R157 | 000471 | 470R 5% 1/3W CARBON | MULLARD | CR25 | - |
| R158 | 000220 | 22R 5% 1/3W CARBON | MULLARD | CR25 | 1 |
| R159 | 000472 | 4k7 5% 1/3W CARBON | MULLARD | CR25 | - |
| R160 | | NOT FITTED | | | - |

NOTES

SEE SHEET 2 FOR LATEST ISSUE

| | | | | | | | | | | | | | | | | | | |
|----------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| NO. | | | | | | | | | | | | | | | | | | |
| DATE | | | | | | | | | | | | | | | | | | |
| BY | | | | | | | | | | | | | | | | | | |
| CHECKED | | | | | | | | | | | | | | | | | | |
| APPROVED | | | | | | | | | | | | | | | | | | |
| DATE | | | | | | | | | | | | | | | | | | |

| | | | |
|----------|---------|------------------------------------|--------|
| DATE | 24.7.84 | datron ELECTRONICS LTD | |
| DRAWN | IL | TITLE 4200 SINE SOURCE PCB ASSY | |
| CHECKED | | DRAWING NUMBER | 400446 |
| APPROVED | | SHEET | 8 |
| DATE | | OF | 27 |

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No. USED Per Assy. |
|------------|-----------------|------------------------|------------------------|-------------------------|--------------------|
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| AN1 | 090017 | 100k x7 2% NETWORK | BECKMAN | L08-1-R100K | 1 |
| AN2 | 090139 | 2k2 x4 2% SIL. NETWORK | BECKMAN | L08-3-R2k2 | 1 |
| AN3 | 090131 | 10k x4 2% SIL. NETWORK | BECKMAN | L08-3-R10K | 6 |
| AN4 | 090132 | 4k7 x4 2% SIL. NETWORK | BECKMAN | L08-3-R4k7 | 1 |
| AN5 | 090140 | 22k x9 2% SIL. NETWORK | BECKMAN | L10-1-R22k | 2 |
| AN6 | 090141 | 1M x9 2% SIL. NETWORK | BECKMAN | L10-1-R1M | 2 |
| AN7 | 090131 | 10k x4 2% SIL. NETWORK | BECKMAN | L08-3-R10K | - |
| AN8 | 090140 | 22k x9 2% SIL. NETWORK | BECKMAN | L10-1-R22k | - |

| | | | | | | | | | | | | | |
|------------------------------|--|--|--|--|--|--|--|--|--|----------|---------|--|---|
| NOTES | | | | | | | | | | DATE | 24.7.84 | | <div style="text-align: center;"> datron ELECTRONICS LTD TITLE 4200 SINE SOURCE PCB ASSY DRAWING NUMBER 400446 SHEET 9 OF 27 </div> |
| SEE SHEET 2 FOR LATEST ISSUE | | | | | | | | | | DRAWN | IL | | |
| NO | | | | | | | | | | CHECKED | | | |
| DATE | | | | | | | | | | APPROVED | | | |
| TIME | | | | | | | | | | DATE | | | |
| | | | | | | | | | | | | | |

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No. USED Per Assy. |
|------------|-----------------|--------------------------|------------------------|-------------------------|--------------------|
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| AN9 | 090141 | 1M x9 2% SIL. NETWORK | BECKMAN | L10-1-R1M | - |
| AN10 | 090131 | 10k x4 2% SIL. NETWORK | BECKMAN | L08-3-R10K | - |
| AN11 | 090131 | 10k x4 2% SIL. NETWORK | BECKMAN | L08-3-R10K | - |
| AN12 | 090086 | 100k x8 2% NETWORK | AB | 761-3-100k | 1 |
| AN13 | 090131 | 10k x4 2% SIL. NETWORK | BECKMAN | L08-3-R10K | - |
| AN14 | 090142 | 10k x4 0.5% DIL NETWORK | BECKMAN | 694-3-R10KD | 1 |
| AN15 | 090136 | 2k x8 0.5% DIL NETWORK | BECKMAN | 698-3-R2kD | 3 |
| AN16 | 090136 | 2k x8 0.5% DIL NETWORK | BECKMAN | 698-3-R2kD | - |
| AN17 | 090131 | 10k x4 2% SIL. NETWORK | BECKMAN | L08-3-R10K | - |
| AN18 | 090136 | 2k x8 0.5% DIL NETWORK | BECKMAN | 698-3-R2kD | - |
| AN19 | 090143 | 500R x4 0.5% DIL NETWORK | BECKMAN | 694-3-R500D | 1 |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| C1 | 102100 | 10pF 5% 500V CER DISC | ITT | CD10 | 3 |
| C2 | 102470 | 47pF 5% 500V CER DISC | ITT | CD10 | 2 |
| C3 | 102470 | 47pF 5% 500V CER DISC | ITT | CD10 | - |
| C4 | 102221 | 220pF 10% 500V CER DISC | ITT | CD10 | 3 |
| C5 | 102471 | 470pF 10% 500V CER DISC | ITT | CD10 | 2 |

| | | | | | | | | | | | | | |
|------------------------------|--|--|--|--|--|--|--|--|--|----------|---------|--|--|
| NOTES | | | | | | | | | | DATE | 24.7.84 | | <div style="text-align: center;"> datron ELECTRONICS LTD TITLE 4200 SINE SOURCE PCB ASSY DRAWING NUMBER 400446 SHEET 10 OF 27 </div> |
| SEE SHEET 2 FOR LATEST ISSUE | | | | | | | | | | DRAWN | IL | | |
| NO | | | | | | | | | | CHECKED | | | |
| DATE | | | | | | | | | | APPROVED | | | |
| TIME | | | | | | | | | | DATE | | | |
| | | | | | | | | | | | | | |

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No. USED Per Assy. |
|------------|-----------------|------------------------------|------------------------|-------------------------|--------------------|
| C6 | 100102 | 1nF 2% 100V CER PLATE | MULLARD | 630 | 14 |
| C7 | 150015 | 10uF 20% 35V DIP TANT | UNION CARBIDE | K10E35 | 4 |
| C8 | 150015 | 10uF 20% 35V DIP TANT | UNION CARBIDE | K10E35 | - |
| C9 | 150020 | 10uF 20% 25V DIP TANT | UNION CARBIDE | K10E25 | 10 |
| C10 | 104026 | 47nF $\pm 50\%$ 50V CER DISC | SIEMENS | B37449 | 30 |
| C11 | 104026 | 47nF $\pm 50\%$ 50V CER DISC | SIEMENS | B37449 | - |
| C12 | 104026 | 47nF $\pm 50\%$ 50V CER DISC | SIEMENS | B37449 | - |
| C13 | 104026 | 47nF $\pm 50\%$ 50V CER DISC | SIEMENS | B37449 | - |
| C14 | 150015 | 10uF 20% 35V DIP TANT | UNION CARBIDE | K10E35 | - |
| C15 | 104026 | 47nF $\pm 50\%$ 50V CER DISC | SIEMENS | B37449 | - |
| C16 | 110040 | 33nF 20% 63V POLYESTER | WIMA | MKS2 | 1 |
| C17 | 150021 | 22uF 20% 25V DIP TANT | UNION CARBIDE | K22E25 | 2 |
| C18 | 110039 | 470nF 20% 63V POLYESTER | WIMA | MKS2 | 1 |
| C19 | 104026 | 47nF $\pm 50\%$ 50V CER DISC | SIEMENS | B37449 | - |
| C20 | 102471 | 470pF 10% 500V CER DISC | ITT | CD10 | - |
| C21 | 150020 | 10uF 20% 25V DIP TANT | UNION CARBIDE | K10E25 | - |
| C22 | 150020 | 10uF 20% 25V DIP TANT | UNION CARBIDE | K10E25 | - |
| C23 | 100102 | 1nF 2% 100V CER PLATE | MULLARD | 630 | - |
| C24 | 104026 | 47nF $\pm 50\%$ 50V CER DISC | SIEMENS | B37449 | - |
| C25 | 120034 | 220nF 1% 63V POLYCARB | ASHCROFT | A2B2201E | 2 |
| C26 | 102100 | 10pF 5% 500V CER DISC | ITT | CD10 | - |
| C27 | 102100 | 10pF 5% 500V CER DISC | ITT | CD10 | - |
| C28 | 120035 | 22nF 1% 400V POLYCARB | ASHCROFT | A2B22004E | 2 |

NOTES

SEE SHEET 2 FOR LATEST ISSUE

| | | |
|----------|-----------|--|
| DATE | 24. 7. 84 | datron ELECTRONICS LTD TITLE 4200 SINE SOURCE PCB ASSY. DRAWING NUMBER 400446 11 SHEET OF 27 |
| DRAWN | L | |
| CHECKED | | |
| APPROVED | | |
| DATE | | |

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No. USED Per Assy. |
|------------|-----------------|---------------------------------|------------------------|-------------------------|--------------------|
| C29 | 102220 | 22pF 5% 500V CER DISC | ITT | CD10 | 3 |
| C30 | 104017 | 0p56F $\pm 0.1pF$ 500V CER DISC | ITT | CD08 AGOP56BS | 2 |
| C31 | 102108 | 1pF $\pm 5pF$ 500V CER DISC | ITT | CD06 | 2 |
| C32 | 102188 | 1p8F $\pm 5pF$ 500V CER DISC | ITT | CD06 | 2 |
| C33 | 102398 | 3p9F $\pm 5pF$ 500V CER DISC | ITT | CD08 | 2 |
| C34 | 150020 | 10uF 20% 25V DIP TANT | UNION CARBIDE | K10E25 | - |
| C35 | 100102 | 1nF 2% 100V CER PLATE | MULLARD | 630 | - |
| C36 | 130083 | 2nF 1% 160V POLYSTYRENE | MULLARD | 425 | 2 |
| C37 | 110042 | 100nF 20% 63V POLYESTER | WIMA | MKS2 | 7 |
| C38 | 102478 | 4p7F $\pm 5pF$ 500V CER DISC | ITT | CD08 | 9 |
| C39 | 100101 | 100pF 2% 100V CER PLATE | MULLARD | 683 | 3 |
| C40 | 100278 | 2p7F 2% 100V CER PLATE | MULLARD | 683 | 2 |
| C41 | 130084 | 110pF 1% 630V POLYSTYRENE | MULLARD | 427 | 2 |
| C42 | 130042 | 100pF 1% 630V POLYSTYRENE | SUFLEX | HS | 2 |
| C43 | 102478 | 4p7F $\pm 5pF$ 500V CER DISC | ITT | CD08 | - |
| C44 | 102338 | 3p3F $\pm 5pF$ 500V CER DISC | ITT | CD08 | 3 |
| C45 | 104026 | 47nF $\pm 50\%$ 50V CER DISC | SIEMENS | B37449 | - |
| C46 | 100102 | 1nF 2% 100V CER PLATE | MULLARD | 630 | - |
| C47 | 150020 | 10uF 20% 25V DIP TANT | UNION CARBIDE | K10E25 | - |
| C48 | 104026 | 47nF $\pm 50\%$ 50V CER DISC | SIEMENS | B37449 | - |
| C49 | 102478 | 4p7F $\pm 5pF$ 500V CER DISC | ITT | CD08 | - |
| C50 | 120034 | 220nF 1% 63V POLYCARB | ASHCROFT | A2B2201E | - |
| C51 | 120035 | 22nF 1% 400V POLYCARB | ASHCROFT | A2B22004E | - |

NOTES

SEE SHEET 2 FOR LATEST ISSUE

| | | |
|----------|-----------|--|
| DATE | 24. 7. 84 | datron ELECTRONICS LTD TITLE 4200 SINE SOURCE PCB ASSY. DRAWING NUMBER 400446 11 SHEET OF 27 |
| DRAWN | L | |
| CHECKED | | |
| APPROVED | | |
| DATE | | |

| DESIGNATOR | DATRON PART No | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No. USED Per Assy. |
|------------|----------------|----------------------------|------------------------|-------------------------|--------------------|
| C52 | 104017 | 0p56F ±0.1pF 500V CER DISC | ITT | GDO8AGOP56BS | - |
| C53 | 104026 | 47nF ±50% 50V CER DISC | SIEMENS | B37449 | - |
| C54 | 102478 | 4p7F ±.5pF 500V CER DISC | ITT | CD08 | - |
| C55 | 104026 | 47nF ±50% 50V CER DISC | SIEMENS | B37449 | - |
| C56 | 102108 | 1pF ±.5pF 500V CER DISC | ITT | CD06 | - |
| C57 | 102188 | 1p8F ±.5pF 500V CER DISC | ITT | CD06 | - |
| C58 | 102398 | 3p9F ±.5pF 500V CER DISC | ITT | CD08 | - |
| C59 | 104026 | 47nF ±50% 50V CER DISC | SIEMENS | B37449 | - |
| C60 | 104026 | 47nF ±50% 50V CER DISC | SIEMENS | B37449 | - |
| C61 | 102478 | 4p7F ±.5pF 500V CER DISC | ITT | CD08 | - |
| C62 | 130083 | 2nF 1% 160V POLYSTYRENE | MULLARD | 425 | - |
| C63 | 104026 | 47nF ±50% 50V CER DISC | SIEMENS | B37449 | - |
| C64 | 100101 | 100pF 2% 100V CER PLATE | MULLARD | 683 | - |
| C65 | 100278 | 2p7F 2% 100V CER PLATE | MULLARD | 683 | - |
| C66 | 130084 | 110pF 1% 630V POLYSTYRENE | MULLARD | 427 | - |
| C67 | 130042 | 100pF 1% 630V POLYSTYRENE | SUFLEX | HS | - |
| C68 | 102478 | 4p7F ±.5pF 500V CER DISC | ITT | CD08 | - |
| C69 | 102338 | 3p3F ±.5pF 500V CER DISC | ITT | CD08 | - |
| C70 | 104026 | 47nF ±50% 50V CER DISC | SIEMENS | B37449 | - |
| C71 | 100102 | 1nF 2% 100V CER PLATE | MULLARD | 630 | - |
| C72 | 150020 | 10nF 20% 25V DIP TANT | UNION CARBIDE | K10E25 | - |
| C73 | 102478 | 4p7F ±.5pF 500V CER DISC | ITT | CD08 | - |
| C74 | 102220 | 22pF 5% 500V CER DISC | ITT | CD10 | - |

NOTES

SEE SHEET 2 FOR LATEST ISSUE

| | | | | | | | | | | | |
|------|--|--|--|--|--|--|--|--|--|--|--|
| DES | | | | | | | | | | | |
| ECO | | | | | | | | | | | |
| DATE | | | | | | | | | | | |
| BY | | | | | | | | | | | |

| | | | |
|----------|---------|----------------------------|----------|
| DATE | 24.7.84 | datron ELECTRONICS LTD | |
| DRAWN | | TITLE | |
| CHECKED | | 4200 SINE SOURCE PCB ASSY. | |
| APPROVED | | DRAWING NUMBER | 400446 |
| DATE | | SHEET | 13 OF 27 |

| DESIGNATOR | DATRON PART No | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No. USED Per Assy. |
|------------|----------------|-------------------------|------------------------|-------------------------|--------------------|
| C75 | 100102 | 1nF 2% 100V CER PLATE | MULLARD | 630 | - |
| C76 | 110041 | 10nF 20% 100V POLYESTER | WIMA | FKS2 | 3 |
| C77 | 102102 | 1nF 10% 500V CER DISC | ITT | CD10 | - |
| C78 | 110041 | 10nF 20% 100V POLYESTER | WIMA | FKS2 | - |
| C79 | 100102 | 1nF 2% 100V CER PLATE | MULLARD | 630 | - |
| C80 | 110042 | 100nF 20% 63V POLYESTER | WIMA | MKS2 | - |
| C81 | 100102 | 1nF 2% 100V CER PLATE | MULLARD | 630 | - |
| C82 | 100182 | 1n8F 2% 100V CER PLATE | MULLARD | 630 | 1 |
| C83 | 100102 | 1nF 2% 100V CER PLATE | MULLARD | 630 | - |
| C84 | 100102 | 1nF 2% 100V CER PLATE | MULLARD | 630 | - |
| C85 | 100102 | 1nF 2% 100V CER PLATE | MULLARD | 630 | - |
| C86 | 102221 | 220pF 10% 500V CER DISC | ITT | CD10 | - |
| C87 | 104026 | 47nF ±50% 50V CER DISC | SIEMENS | B37449 | - |
| C88 | 104026 | 47nF ±50% 50V CER DISC | SIEMENS | B37449 | - |
| C89 | 110046 | 1µF 20% 50V POLYESTER | WIMA | MKS2 | 1 |
| C90 | 104026 | 47nF ±50% 50V CER DISC | SIEMENS | B37449 | - |
| C91 | 104026 | 47nF ±50% 50V CER DISC | SIEMENS | B37449 | - |
| C92 | 102331 | 330pF 10% 500V CER DISC | ITT | CD10 | 1 |
| C93 | 104026 | 47nF ±50% 50V CER DISC | ITT | B37449 | - |
| C94 | 104026 | 47nF ±50% 50V CER DISC | ITT | B37449 | - |
| C95 | 101103 | 10nF 25% 250V CER DISC | ITT | CD10 | 1 |
| C96 | 150010 | 330nF 20% 35V DIP TANT | UNION CARBIDE | KR33E35 | 1 |
| C97 | 100101 | 100pF 2% 100V CER PLATE | MULLARD | 683 | - |

NOTES

SEE SHEET 2 FOR LATEST ISSUE

| | | | | | | | | | | | |
|------|--|--|--|--|--|--|--|--|--|--|--|
| DES | | | | | | | | | | | |
| ECO | | | | | | | | | | | |
| DATE | | | | | | | | | | | |
| BY | | | | | | | | | | | |

| | | | |
|----------|---------|----------------------------|----------|
| DATE | 24.7.84 | datron ELECTRONICS LTD | |
| DRAWN | | TITLE | |
| CHECKED | | 4200 SINE SOURCE PCB ASSY. | |
| APPROVED | | DRAWING NUMBER | 400446 |
| DATE | | SHEET | 14 OF 27 |

| DESIGNATOR | DATRON PART No | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No | No. USED Per Assy |
|------------|----------------|------------------------------|------------------------|------------------------|-------------------|
| C98 | 110042 | 100nF 20% 63V POLYESTER | WIMA | CD10 | - |
| C99 | 110042 | 100nF 20% 63V POLYESTER | WIMA | CD10 | - |
| C100 | 104026 | 47nF $\pm 50\%$ 50V CER DISC | SIEMENS | B37449 | - |
| C101 | 104026 | 47nF $\pm 50\%$ 50V CER DISC | SIEMENS | B37449 | - |
| C102 | 150020 | 10uF 20% 25V DIP TANT | UNION CARBIDE | K10E25 | - |
| C103 | 150020 | 10uF 20% 25V DIP TANT | UNION CARBIDE | K10E25 | - |
| C104 | 102478 | 4p7F $\pm 5\%$ 500V CER DISC | ITT | CD08 | - |
| C105 | 104026 | 47nF $\pm 50\%$ 50V CER DISC | SIEMENS | B37449 | - |
| C106 | 100102 | 1nF 2% 100V CER PLATE | MULLARD | 630 | - |
| C107 | 110042 | 100nF 20% 63V POLYESTER | WIMA | CD10 | - |
| C108 | 110015 | 15nF 20% 63V POLYESTER | WIMA | MKS2 | 1 |
| C109 | 110041 | 10nF 20% 100V POLYESTER | WIMA | FKS2 | - |
| C110 | 104064 | 12pF 5% 50V CER DISC | AVX | SR21A120JAA | 1 |
| C111 | 110042 | 100nF 20% 63V POLYESTER | WIMA | CD10 | - |
| C112 | 102221 | 220pF 10% 500V CER DISC | ITT | CD10 | - |
| C113, C114 | 104026 | 47nF $\pm 50\%$ 50V CER DISC | ITT | B37449 | - |
| C115 | 150015 | 10uF 20% 35V DIP TANT | UNION CARBIDE | K10E35 | - |
| C116 | 102478 | 4p7F $\pm 5\%$ 500V CER DISC | ITT | CD08 | - |
| C117 | 100102 | 1nF 2% 100V CER PLATE | MULLARD | 630 | - |
| C118 | 104026 | 47nF $\pm 50\%$ 50V CER DISC | SIEMENS | B37449 | - |
| C119 | 102338 | 3p3F $\pm 5\%$ 500V CER DISC | ITT | CD08 | - |
| C120 | 104026 | 47nF $\pm 50\%$ 50V CER DISC | SIEMENS | B37449 | - |
| C121 | 150023 | 33uF 20% 25V DIP TANT | UNION CARBIDE | K33E25 | 3 |

| | | | | | | | |
|------------------------------------|--|--|--|--|----------|------------------------------|---------------------------|
| NOTES | | | | | DATE | 24.7.84 | datron ELECTRONICS LTD |
| SEE SHEET 1 OF 27 FOR LATEST ISSUE | | | | | DRAWN | | |
| | | | | | TITLE | 4200 SINE SOURCE PCB ASSY | |
| | | | | | APPROVED | | DRAWING NUMBER |
| | | | | | DATE | | 400446 |
| | | | | | | | SHEET 15 OF 27 |

| DESIGNATOR | DATRON PART No | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No | No. USED Per Assy |
|------------|----------------|------------------------------|------------------------|------------------------|-------------------|
| C122 | 150023 | 33uF 20% 25V DIP TANT | UNION CARBIDE | K33E25 | - |
| C123 | 150020 | 10uF 20% 25V DIP TANT | UNION CARBIDE | K10E25 | - |
| C124 | 104026 | 47nF $\pm 50\%$ 50V CER DISC | SIEMENS | B37449 | - |
| C125 | 150020 | 10uF 20% 25V DIP TANT | UNION CARBIDE | K10E25 | - |
| C126 | 150023 | 33uF 20% 25V DIP TANT | UNION CARBIDE | K33E25 | - |
| C127 | 102220 | 22pF 5% 500V CER DISC | ITT | CD10 | - |
| C128 | 104026 | 47nF $\pm 50\%$ 50V CER DISC | SIEMENS | B37449 | - |
| C129 | 150021 | 22uF 20% 25V DIP TANT | UNION CARBIDE | K22E25 | - |
| C130 | 110042 | 100nF 20% 63V POLYESTER | WIMA | MKS2 | - |
| C131 | 100102 | 1nF 10% 500V CER PLATE | MULLARD | 630 | - |
| C132 | | NOT FITTED | | | - |
| C133 | 102221 | 2p2F 10% 500V CER DISC | ITT | CD08 | 1 |
| C134 | 100029 | 68pF 20% 100V POLYCARB | WIMA | FKC2 | 1 |

| | | | | | | | |
|-------|--|--|--|--|----------|------------------------------|---------------------------|
| NOTES | | | | | DATE | 24.7.84 | datron ELECTRONICS LTD |
| | | | | | DRAWN | | |
| | | | | | TITLE | 4200 SINE SOURCE PCB ASSY | |
| | | | | | APPROVED | | DRAWING NUMBER |
| | | | | | DATE | | 400446 |
| | | | | | | | SHEET 16 OF 27 |

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No. USED Per Assy. |
|------------|-----------------|----------------------|------------------------|-------------------------|--------------------|
| D1 | 220010 | Si HOT CARRIER DIODE | HP | HSCH1001/IN6263 | 4 |
| D2 | 210091 | 9V1 400mW ZENER | MULLARD | BZY88C9V1 | 3 |
| D3 | 210150 | 15V 400mW ZENER | MULLARD | BZY88C15 | 1 |
| D4 | 210091 | 9V1 400mW ZENER | MULLARD | BZY88C9V1 | - |
| D5 | 213009 | 15V 5W ZENER | UNITRODE | TV5515 | 4 |
| D6 | 213009 | 15V 5W ZENER | UNITRODE | TV5515 | - |
| D7 | 200001 | 75mA 75V GP Si DIODE | FAIRCHILD | IN4148 | 14 |
| D8 | 200001 | 75mA 75V GP Si DIODE | FAIRCHILD | IN4148 | - |
| D9 | 200001 | 75mA 75V GP Si DIODE | FAIRCHILD | IN4148 | - |
| D10 | 210043 | 4V3 400mW ZENER | MULLARD | BZY88C4V3 | 4 |
| D11 | 200001 | 75mA 75V GP Si DIODE | FAIRCHILD | IN4148 | - |
| D12 | 210043 | 4V3 400mW ZENER | MULLARD | BZY88C4V3 | - |
| D13 | 200001 | 75mA 75V GP Si DIODE | FAIRCHILD | IN4148 | - |
| D14 | 200001 | 75mA 75V GP Si DIODE | FAIRCHILD | IN4148 | - |
| D15 | 200001 | 75mA 75V GP Si DIODE | FAIRCHILD | IN4148 | - |
| D16 | 210043 | 4V3 400mW ZENER | MULLARD | BZY88C4V3 | - |
| D17 | 200001 | 75mA 75V GP Si DIODE | FAIRCHILD | IN4148 | - |
| D18 | 210043 | 4V3 400mW ZENER | MULLARD | BZY88C4V3 | - |
| D19 | 210091 | 9V1 400mW ZENER | MULLARD | BZY88C9V1 | - |
| D20 | 213011 | 1V5 250mW ZENER | MULLARD | BZV46-1V5 | 2 |
| D21 | 200001 | 75mA 75V GP Si DIODE | FAIRCHILD | IN4148 | - |
| D22 | 213011 | 1V5 250mW ZENER | MULLARD | BZV46-1V5 | - |
| D23 | 200001 | 75mA 75V GP Si DIODE | FAIRCHILD | IN4148 | - |

NOTES.

SEE SHEET 2 FOR LATEST ISSUE

| ISS | ECO | DATE | CHKED |
|-----|-----|------|-------|
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |

| | | | |
|----------|---------|---------------------------------------|--|
| DATE | 24.7.84 | datron ELECTRONICS LTD | |
| DRAWN | | TITLE 4200 SINE SOURCE PCB ASSY | |
| CHECKED | | DRAWING NUMBER 400446 | |
| APPROVED | | 17 SHEET OF 27 | |
| DATE | | | |

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No. USED Per Assy. |
|------------|-----------------|----------------------|------------------------|-------------------------|--------------------|
| D24 | 210056 | 5V6 400mW ZENER | MULLARD | BZY88C5V6 | 2 |
| D25 | 210056 | 5V6 400mW ZENER | MULLARD | BZY88C5V6 | - |
| D26 | 213023 | 6V4 100ppm ZENER | MOTOROLA | IN4575 | 2 |
| D27 | 213009 | 15V 5W ZENER | UNITRODE | TV5515 | - |
| D28 | 220010 | Si HOT CARRIER DIODE | HP | HSCH1001/IN6263 | - |
| D29 | 220010 | Si HOT CARRIER DIODE | HP | HSCH1001/IN6263 | - |
| D30 | 213023 | 6V4 100ppm ZENER | MOTOROLA | IN4575 | - |
| D31 | 200001 | 75mA 75V GP Si DIODE | FAIRCHILD | IN4148 | - |
| D32 | 200001 | 75mA 75V GP Si DIODE | FAIRCHILD | IN4148 | - |
| D33 | 200001 | 75mA 75V GP Si DIODE | FAIRCHILD | IN4148 | - |
| D34 | 213009 | 15V 5W ZENER | UNITRODE | TV5515 | - |
| D35 | 200001 | 75mA 75V GP Si DIODE | FAIRCHILD | IN4148 | - |
| D36 | 200006 | 1A 600V GP Si DIODE | FAIRCHILD | IN4005 | 2 |
| D37 | 200006 | 1A 600V GP Si DIODE | FAIRCHILD | IN4005 | - |
| D38 | 220010 | Si HOT CARRIER DIODE | HP | HSCH1001/IN6263 | - |
| D39 | 213012 | 2V0 250mW ZENER | MULLARD | BZV46-2V0 | 2 |
| D40 | 210062 | 6V2 400mW ZENER | MULLARD | BZY88C6V2 | 2 |
| D41 | 210062 | 6V2 400mW ZENER | MULLARD | BZY88C6V2 | - |
| D42 | 213012 | 2V0 250mW ZENER | MULLARD | BZV46-2V0 | - |

NOTES

SEE SHEET 2 FOR LATEST ISSUE

| ISS | ECO | DATE | CHKED |
|-----|-----|------|-------|
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |

| | | | |
|----------|---------|---------------------------------------|--|
| DATE | 24.7.84 | datron ELECTRONICS LTD | |
| DRAWN | | TITLE 4200 SINE SOURCE PCB ASSY | |
| CHECKED | | DRAWING NUMBER 400446 | |
| APPROVED | | 18 SHEET OF 27 | |
| DATE | | | |

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No. USED Per Assy. |
|------------|-----------------|---------------------|------------------------|-------------------------|--------------------|
| Q1 | * 239092-1 | J511x2 SELECTED FET | | SEE DRG | 1 of SET |
| Q2 | 250004 | Si PNP TRANSISTOR | NATIONAL | 2N3906/TO18 | 7 |
| Q3 | 250004 | Si PNP TRANSISTOR | NATIONAL | 2N3906/TO18 | - |
| Q4 | 240006 | Si NPN TRANSISTOR | NATIONAL | 2N3904/TO18 | 10 |
| Q5 | 240006 | Si NPN TRANSISTOR | NATIONAL | 2N3904/TO18 | - |
| Q6 | * 239092-1 | J511x2 SELECTED FET | | SEE DRG | 1 of SET |
| Q7 | 240006 | Si NPN TRANSISTOR | NATIONAL | 2N3904/TO18 | - |
| Q8 | 240013 | Si NPN TRANSISTOR | NATIONAL | BC184C/TO18 | 5 |
| Q9 | 230065 | N-CHAN I LIM 4.7mA | SILICONIX | J511 | 2 |
| Q10 | | NOT USED | | | - |
| Q11 | 240032 | Si NPN TRANSISTOR | MOTOROLA | BF393/TO18 | 5 |
| Q12 | 250004 | Si PNP TRANSISTOR | NATIONAL | 2N3906/TO18 | - |
| Q13 | 230065 | N-CHAN I LIM 4.7mA | SILICONIX | J511 | - |
| Q14 | 240006 | Si NPN TRANSISTOR | NATIONAL | 2N3904/TO18 | - |
| Q15 | 240006 | Si NPN TRANSISTOR | NATIONAL | 2N3904/TO18 | - |
| Q16 | 240006 | Si NPN TRANSISTOR | NATIONAL | 2N3904/TO18 | - |
| Q17 | 240006 | Si NPN TRANSISTOR | NATIONAL | 2N3904/TO18 | - |
| Q18 | 250004 | Si PNP TRANSISTOR | NATIONAL | 2N3906/TO18 | - |
| Q19 | 230001 | N-CHAN I LIM 1.4mA | SILICONIX | J506 | 3 |
| Q20 | 230035 | N-CHAN JFET | TELEDYNE | U1897JF | 28 |
| Q21 | 230035 | N-CHAN JFET | TELEDYNE | U1897JF | - |
| Q22 | 230035 | N-CHAN JFET | TELEDYNE | U1897 JF | - |
| Q23 | 230035 | N-CHAN JFET | TELEDYNE | U1897 JF | - |

NOTES

SEE SHEET 2 FOR LATEST ISSUE

| REV | DATE | BY | CHKD | DATE | BY | CHKD | DATE | BY | CHKD | DATE | BY | CHKD | DATE | BY | CHKD | DATE | BY | CHKD |
|-----|------|----|------|------|----|------|------|----|------|------|----|------|------|----|------|------|----|------|
| | | | | | | | | | | | | | | | | | | |

| | | | | | |
|----------------|---------|---|----|----|----|
| DATE | 24.7.84 | datron <small>ELECTRONICS LTD</small> 4200 SINE SOURCE PCB ASSY | | | |
| DRAWN | L. | | | | |
| CHECKED | | | | | |
| APPROVED | | | | | |
| DATE | | | | | |
| DRAWING NUMBER | 400446 | SHEET | 19 | OF | 27 |

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No. USED Per Assy. |
|------------|-----------------|----------------------------|------------------------|-------------------------|--------------------|
| Q24 | 230035 | N-CHAN JFET | TELEDYNE | U1897 JF | - |
| Q25 | 230035 | N-CHAN JFET | TELEDYNE | U1897 JF | - |
| Q26 | 230035 | N-CHAN JFET | TELEDYNE | U1897 JF | - |
| Q27 | 230035 | N-CHAN JFET | TELEDYNE | U1897 JF | - |
| Q28 | 230035 | N-CHAN JFET | TELEDYNE | U1897 JF | - |
| Q29 | 239060-1 | N-CHAN DUAL JFET + R41 | DATRON | VCR11 (COLOUR) + HB | 1 |
| Q30 | 260060 | 334 CURRENT SOURCE | NATIONAL | LM334H | 1 |
| Q31 | 240043 | TRAN NPN - (RESERVE STOCK) | MOTOROLA | 2N3904 | 2 |
| Q32 | 230035 | N-CHAN JFET | TELEDYNE | U1897 JF | - |
| Q33 | 230035 | N-CHAN JFET | TELEDYNE | U1897 JF | - |
| Q34 | 230035 | N-CHAN JFET | TELEDYNE | U1897 JF | - |
| Q35 | 230035 | N-CHAN JFET | TELEDYNE | U1897 JF | - |
| Q36 | 230035 | N-CHAN JFET | TELEDYNE | U1897 JF | - |
| Q37 | 230035 | N-CHAN JFET | TELEDYNE | U1897 JF | - |
| Q38 | 230035 | N-CHAN JFET | TELEDYNE | U1897 JF | - |
| Q39 | 230035 | N-CHAN JFET | TELEDYNE | U1897 JF | - |
| Q40 | 230035 | N-CHAN JFET | TELEDYNE | U1897 JF | - |
| Q41 | 230046-1 | N-CHAN DUAL JFET | | SEE DRG | 1 |
| Q42 | 230001 | N-CHAN I LIM 1.4mA | SILICONIX | J506 | - |
| Q43 | 230001 | N-CHAN I LIM 1.4mA | SILICONIX | J506 | - |
| Q44 | 240043 | TRAN NPN - (RESERVE STOCK) | MOTOROLA | 2N3904 | - |
| Q45 | 250001 | Si PNP TRANSISTOR | NATIONAL | BC214/TO18 | 3 |
| Q46 | 250001 | Si PNP TRANSISTOR | NATIONAL | BC214/TO18 | - |

NOTES

SEE SHEET 2 FOR LATEST ISSUE

| REV | DATE | BY | CHKD | DATE | BY | CHKD | DATE | BY | CHKD | DATE | BY | CHKD | DATE | BY | CHKD | DATE | BY | CHKD |
|-----|------|----|------|------|----|------|------|----|------|------|----|------|------|----|------|------|----|------|
| | | | | | | | | | | | | | | | | | | |

| | | | | | |
|----------------|---------|---|----|----|----|
| DATE | 24.7.84 | datron <small>ELECTRONICS LTD</small> 4200 SINE SOURCE PCB ASSY | | | |
| DRAWN | L. | | | | |
| CHECKED | | | | | |
| APPROVED | | | | | |
| DATE | | | | | |
| DRAWING NUMBER | 400446 | SHEET | 20 | OF | 27 |

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No. USED Per Assy. |
|------------|-----------------|------------------------|------------------------|-------------------------|--------------------|
| Q47 | 230035 | N-CHAN JFET | TELEDYNE | U1897JF | - |
| Q48 | 230035 | N-CHAN JFET | TELEDYNE | U1897JF | - |
| Q49 | 230035 | N-CHAN JFET | TELEDYNE | U1897JF | - |
| Q50 | 230035 | N-CHAN JFET | TELEDYNE | U1897JF | - |
| Q51 | 230035 | N-CHAN JFET | TELEDYNE | U1897JF | - |
| Q52 | 230035 | N-CHAN JFET | TELEDYNE | U1897JF | - |
| Q53 | 230035 | N-CHAN JFET | TELEDYNE | U1897JF | - |
| Q54 | 250004 | Si PNP TRANSISTOR | NATIONAL | 2N3906/TO18 | - |
| Q55 | 240017 | Si NPN DUAL TRANSISTOR | NATIONAL | LM394 | 6 |
| Q56 | 240017 | Si NPN DUAL TRANSISTOR | NATIONAL | LM394 | - |
| Q57 | 240017 | Si NPN DUAL TRANSISTOR | NATIONAL | LM394 | - |
| Q58 | 240017 | Si NPN DUAL TRANSISTOR | NATIONAL | LM394 | - |
| Q59 | 240017 | Si NPN DUAL TRANSISTOR | NATIONAL | LM394 | - |
| Q60 | 240017 | Si NPN DUAL TRANSISTOR | NATIONAL | LM394 | - |
| Q61 | 230050 | N-CHAN I LIM 2.4mA | SILICONIX | J508 | 1 |
| Q62 | 240013 | Si NPN TRANSISTOR | NATIONAL | BC184C/TO18 | - |
| Q63 | 240013 | Si NPN TRANSISTOR | NATIONAL | BC184C/TO18 | - |
| Q64 | 240013 | Si NPN TRANSISTOR | NATIONAL | BC184C/TO18 | - |
| Q65 | 240013 | Si NPN TRANSISTOR | NATIONAL | BC184C/TO18 | - |
| Q66 | 230042 | N-CHAN I LIM 3.0mA | SILICONIX | J509 | 6 |
| Q67 | 230035 | N-CHAN JFET | TELEDYNE | U1897JF | - |
| Q68 | 230035 | N-CHAN JFET | TELEDYNE | U1897JF | - |
| Q69 | 230035 | N-CHAN JFET | TELEDYNE | U1897JF | - |

| | | | | | | | | | |
|------------------------------|--|--|--|--|--|----------|---------|---------------------------|--|
| NOTES | | | | | | DATE | 24.7.84 | datron ELECTRONICS LTD | |
| SEE SHEET 2 FOR LATEST ISSUE | | | | | | DRAWN | | TITLE | |
| | | | | | | CHECKED | | 4200 SINE SOURCE PCB ASSY | |
| | | | | | | APPROVED | | DRAWING NUMBER | |
| | | | | | | DATE | | 400446 | |
| | | | | | | | | SHEET OF 27 | |

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No. USED Per Assy. |
|------------|-----------------|----------------------|------------------------|-------------------------|------------------------|
| Q70 | 240006 | Si NPN TRANSISTOR | NATIONAL | 2N3904/TO18 | - |
| Q71 | 250008 | Si PNP TRANSISTOR | NATIONAL | BC214C/TO18 | 2 |
| Q72 | 250008 | Si PNP TRANSISTOR | NATIONAL | BC214C/TO18 | - |
| Q73 | 230042 | N-CHAN I LIM 3.0mA | SILICONIX | J509 | - |
| Q74 | 230003 | N-CHAN JFET | TELEDYNE | U1899JF | 1 |
| Q75 | 240006 | Si NPN TRANSISTOR | NATIONAL | 2N3904/TO18 | - |
| Q76 | 239059-1 | N-CHAN DUAL JFET KIT | DATRON | VCR11 | } SAME COLOUR 1 KIT |
| Q77 | 239059-1 | N-CHAN DUAL JFET KIT | DATRON | VCR11 | |
| Q78 | 240032 | Si NPN TRANSISTOR | MOTOROLA | BF 393/TO18 | - |
| Q79 | 240032 | Si NPN TRANSISTOR | MOTOROLA | BF 393/TO18 | - |
| Q80 | 240032 | Si NPN TRANSISTOR | MOTOROLA | BF 393/TO18 | - |
| Q81 | 240032 | Si NPN TRANSISTOR | MOTOROLA | BF 393/TO18 | - |
| Q82 | 230042 | N-CHAN I LIM 3.0mA | SILICONIX | J509 | - |
| Q83 | 240001 | Si NPN TRANSISTOR | NATIONAL | BC184/TO18 | 2 |
| Q84 | 230042 | N-CHAN I LIM 3.0mA | SILICONIX | J509 | - |
| Q85 | 250001 | Si PNP TRANSISTOR | NATIONAL | BC214/TO18 | - |
| Q86 | 240031 | Si NPN TRANSISTOR | MOTOROLA | BD139 | 2 |
| Q87 | 230042 | N-CHAN I LIM 3.0mA | SILICONIX | J509 | - |
| Q88 | 240006 | Si NPN TRANSISTOR | NATIONAL | 2N3904/TO18 | - |
| Q89 | 230042 | N-CHAN I LIM 3.0mA | SILICONIX | J509 | - |
| Q90 | 250004 | Si PNP TRANSISTOR | NATIONAL | 2N3906/TO18 | - |
| Q91 | 240001 | Si NPN TRANSISTOR | NATIONAL | BC184/TO18 | - |
| Q92 | 250004 | Si PNP TRANSISTOR | NATIONAL | 2N3906/TO92 | - |

| | | | | | | | | | |
|------------------------------|--|--|--|--|--|----------|---------|---------------------------|--|
| NOTES | | | | | | DATE | 24.7.84 | datron ELECTRONICS LTD | |
| SEE SHEET 2 FOR LATEST ISSUE | | | | | | DRAWN | | TITLE | |
| | | | | | | CHECKED | | 4200 SINE SOURCE PCB ASSY | |
| | | | | | | APPROVED | | DRAWING NUMBER | |
| | | | | | | DATE | | 400446 | |
| | | | | | | | | SHEET OF 27 | |

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No. USED Per Assy. |
|------------|-----------------|-------------------------|------------------------|-------------------------|--------------------|
| Q93 | 240031 | Si NPN TRANSISTOR | MOTOROLA | BD139 | - |
| Q94 | 250021 | Si PNP TRANSISTOR | MOTOROLA | BD140 | 1 |
| M1 | 280101 | DUAL BCD/BINARY COUNTER | MOTOROLA | MC14569BCP | 3 |
| M2 | 280057 | BCD UP/DOWN COUNTER | MOTOROLA | MC14510BCP | 1 |
| M3 | 280008 | QUAD 2 I/P NAND | MOTOROLA | MC14011BCP | 1 |
| M4 | 280011 | DUAL D FLIP-FLOP | MOTOROLA | MC14013BCP | 2 |
| M5 | 280101 | DUAL BCD/BINARY COUNTER | MOTOROLA | MC14569BCP | - |
| M6 | 280076 | 8 CHANNEL AN MUX | MOTOROLA | MC14051BCL | 2 |
| M7 | 280079 | QUAD 2 I/P OR | MOTOROLA | MC14071BCP | 1 |
| M8 | 280076 | 8 CHANNEL AN MUX | MOTOROLA | MC14051BCL | - |
| M9 | 280101 | DUAL BCD/BINARY COUNTER | MOTOROLA | MC14569BCP | - |
| M10 | 280025 | QUAD ANALOG SWITCH | MOTOROLA | MC14066BCP | 1 |
| M11 | 260073 | 4 I I OP AMP | NATIONAL | LF411CN | 1 |
| M12 | 280125 | PHASE DETECTOR | NATIONAL | MM74C932N | 1 |
| M13 | 280011 | DUAL D FLIP-FLOP | MOTOROLA | MC14013BCP | - |
| M14 | 280080 | HEX SCHMITT TRIGGER | NATIONAL | MM74C14N | 2 |
| M15 | 260074 | LH0032C FAST FET OP AMP | NATIONAL | LH0032CG | 1 |

NOTES

SEE SHEET 2 FOR LATEST ISSUE

| | | |
|----------------|---------|--|
| DATE | 24.7.84 | datron ELECTRONICS LTD 4200 SINE SOURCE PCB ASSY |
| DRAWN | L | |
| CHECKED | | |
| APPROVED | | |
| DATE | | |
| DRAWING NUMBER | 400446 | SHEET 23 OF 27 |

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No. USED Per Assy. |
|------------|-----------------|----------------------|------------------------|-------------------------|--------------------|
| M16 | 260076 | CURRENT MIRROR 1:1 | TEXAS | TLO11CLP | 5 |
| M17 | 290090 | 7x DARLINGTON DRIVER | SPRAGUE/EXAR | ULN2002A/XR2202CP | 4 |
| M18 | 260076 | CURRENT MIRROR 1:1 | TEXAS | TLO11CLP | - |
| M19 | 260046 | 2525 OP AMP | HARRIS | HA32527-5 | 11 |
| M20 | 290090 | 7x DARLINGTON DRIVER | SPRAGUE/EXAR | ULN2002A/XR2202CP | - |
| M21 | 280080 | HEX SCHMITT TRIGGER | NATIONAL | MM74C14N | - |
| M22 | 260046 | 2525 OP AMP | HARRIS | HA32527-5 | - |
| M23 | 260046 | 2525 OP AMP | HARRIS | HA32527-5 | - |
| M24 | 260046 | 2525 OP AMP | HARRIS | HA32527-5 | - |
| M25 | 260046 | 2525 OP AMP | HARRIS | HA32527-5 | - |
| M26 | 260076 | CURRENT MIRROR 1:1 | TEXAS | TLO11CLP | 3 |
| M27 | 260076 | CURRENT MIRROR 1:1 | TEXAS | TLO11CLP | - |
| M28 | 290090 | 7x DARLINGTON DRIVER | SPRAGUE/EXAR | ULN2002A/XR2202CP | - |
| M29 | 280035 | BCD/DECIMAL DECODER | MOTOROLA | MC14028BCP | 1 |
| M30 | 260046 | 2525 OP AMP | HARRIS | HA32527-5 | - |
| M31 | 260046 | 2525 OP AMP | HARRIS | HA32527-5 | - |
| M32 | 260057 | 5534 OP AMP | SIGNETICS | NE5534N | 1 |
| M33 | 290090 | 7x DARLINGTON DRIVER | SPRAGUE/EXAR | ULN2002A/XR2202CP | - |
| M34 | 290000 | NPN TRANSISTOR ARRAY | RCA | CA3083F | 2 |
| M35 | 260042 | 5532 DUAL OP AMP | SIGNETICS | NE5532N | 2 |
| M36 | 280023 | QUAD 2 I/P NOR | MOTOROLA | MC14001UBCP | 1 |
| M37 | 260078 | DUAL COMPARATOR | NATIONAL | LM393AN | 1 |
| M38 | 280126 | D/A CONVERTER | ANALOG DEVICES | AD7527KN | 1 |

NOTES

SEE SHEET 2 FOR LATEST ISSUE

| | | |
|----------------|---------|--|
| DATE | 24.7.84 | datron ELECTRONICS LTD 4200 SINE SOURCE PCB ASSY |
| DRAWN | | |
| CHECKED | | |
| APPROVED | | |
| DATE | | |
| DRAWING NUMBER | 400446 | SHEET 24 OF 27 |

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No. USED Per Assy. |
|------------|-----------------|-------------------------------|------------------------|-------------------------|--------------------|
| M39 | 260033 | 5V V _{IOA} REGULATOR | MOTOROLA | MC78L05ACP | 1 |
| M40 | 290000 | NPN TRANSISTOR ARRAY | RCA | CA3083F | - |
| M41 | 260042 | 5532 DUAL OP AMP | SIGNETICS | NE5532N | - |
| M42 | 280127 | 10-BIT MULTIPLYING DAC | ANALOG DEVICES | AD7533JN | 2 |
| M43 | 280127 | 10-BIT MULTIPLYING DAC | ANALOG DEVICES | AD7533JN | - |
| M44 | 260046 | 2525 OP AMP | HARRIS | HA32527-5 | - |
| M45 | 260027 | 714 OP AMP | FAIRCHILD | UA714HC | 1 |
| M46 | 260046 | 2525 OP AMP | HARRIS | HA32527-5 | - |
| M47 | 260046 | 2525 OP AMP | HARRIS | HA32527-5 | - |
| M48 | 260046 | 2525 OP AMP | HARRIS | HA32527-5 | - |
| M49 | 260049 | 319 DUAL COMPARATOR | NATIONAL | LM319N | 1 |
| M50 | 260076 | CURRENT MIRROR 1:1 | TEXAS | TLO11 CLP | - |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| RL1 | 330012-3 | RELAY REED 1A GUARDED | HAMLIN | HE721A5134 | 8 |
| RL2 | 330012-3 | RELAY REED 1A GUARDED | HAMLIN | HE721A5134 | - |
| RL3 | 330012-3 | RELAY REED 1A GUARDED | HAMLIN | HE721A5134 | - |
| RL4 | 330012-3 | RELAY REED 1A GUARDED | HAMLIN | HE721A5134 | - |
| RL5 | 330012-3 | RELAY REED 1A GUARDED | HAMLIN | HE721A5134 | - |
| RL6 | 330012-3 | RELAY REED 1A GUARDED | HAMLIN | HE721A5134 | - |

NOTES

SEE SHEET 2 FOR LATEST ISSUE

| | | | | | | | | | | | | | | | | | | | | |
|-------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| DES | | | | | | | | | | | | | | | | | | | | |
| FILED | | | | | | | | | | | | | | | | | | | | |
| DATE | | | | | | | | | | | | | | | | | | | | |
| BY | | | | | | | | | | | | | | | | | | | | |

| | |
|-----------------|---|
| DATE 24.7.84 | datron ELECTRONICS LTD TITLE 4200 SINE SOURCE PCB ASSY DRAWING NUMBER 400446 |
| DRAWN | |
| CHECKED | |
| APPROVED | |
| DATE | |
| | 25 |

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No. USED Per Assy. |
|------------|-----------------|-----------------------|------------------------|-------------------------|--------------------|
| RL7 | 330012-3 | RELAY REED 1A GUARDED | HAMLIN | HE721A5134 | - |
| RL8 | 330012-3 | RELAY REED 1A GUARDED | HAMLIN | HE721A5134 | - |
| | | | | | |
| | | | | | |
| | | | | | |
| L1 | 370003 | 1mH 40Ω RF CHOKE | SIGMA | SC10 | 2 |
| L2 | 370001 | 10μH 0.85Ω RF CHOKE | PLESSEY | 58/10/0011/10 | 6 |
| L3 | 370001 | 10μH 0.85Ω RF CHOKE | PLESSEY | 58/10/0011/10 | - |
| L4 | 370001 | 10μH 0.85Ω RF CHOKE | PLESSEY | 58/10/0011/10 | - |
| L5 | 370001 | 10μH 0.85Ω RF CHOKE | PLESSEY | 58/10/0011/10 | - |
| L6 | 370001 | 10μH 0.85Ω RF CHOKE | PLESSEY | 58/10/0011/10 | - |
| L7 | 370026 | 1μH 880mA CHOKE | SIGMA | SC10 | 1 |
| L8 | 370003 | 1mH 40Ω RF CHOKE | SIGMA | SC10 | - |
| L9 | 370001 | 10μH 0.85Ω RF CHOKE | PLESSEY | 58/10/0011/10 | - |
| | 410171-8 | PCB | | | 1 |
| | 450450-1 | HEATSINK | | | 1 |
| | 540002 | 22 SWG BTC WIRE | | | A/R |
| | 512999 | 7/2 PTFE WIRE | | | A/R |
| | 602001 | FSV TERMINAL | MOLEX | 02-04-5114 | 6 |
| | 605059 | 8WAY DIL SOCKET | JERMYN | J23-18008 | 17 |
| | 605060 | 14WAY DIL SOCKET | JERMYN | J23-18014 | 9 |
| | 605061 | 16WAY DIL SOCKET | JERMYN | J23-18016 | 15 |

NOTES

SEE SHEET 2 FOR LATEST ISSUE

| | | | | | | | | | | | | | | | | | | | | |
|-------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| DES | | | | | | | | | | | | | | | | | | | | |
| FILED | | | | | | | | | | | | | | | | | | | | |
| DATE | | | | | | | | | | | | | | | | | | | | |
| BY | | | | | | | | | | | | | | | | | | | | |

| | |
|-----------------|---|
| DATE 24.7.84 | datron ELECTRONICS LTD TITLE 4200 SINE SOURCE PCB ASSY DRAWING NUMBER 400446 |
| DRAWN | |
| CHECKED | |
| APPROVED | |
| DATE | |
| | 26 |

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No. USED Per Assy. |
|------------|--------------------|------------------------------|---------------------------|----------------------------|-----------------------|
| | 605065 | 28 WAY DIL SOCKET | JERMYN | J23-18028 | 1 |
| | 604046 | 3-WAY .1" PCB PLUG GD.R. | MOLEX | 22-10-2031 | 2 |
| | 611016 | M3x8mm POZIPAN STEEL | ZN PL | | 2 |
| | 611025 | M3x16mm POZICK STEEL | ZN PL | | 1 |
| | 612026-1 | M3x6mm STANDOFF | DATRON | SEE DRG | 1 |
| | 613005 | M3 INT SHAKEPROOF | | | 2 |
| | 615002 | M3 FULL NUT STEEL ZN.PL. | | | 2 |
| | 620003 | SOLDER PIN | HARWIN | H2105A01 | 3 |
| | 620007 | TEST POINT TERMINAL | MICROVAR | TYPE C30 | 32 |
| | 630024 | STEATITE BEAD 16SWG | PARK ROYAL PORCELAIN | Nº2 | 8 |
| | 630107 | BRASS STRIP 15.5 x 38mm | RIGHTON | CZ108 1/2H | A/R |
| | 630120 | PCB EJECTOR (YELLOW) | RICHCO | CBE | 2 |
| | 900003 | HEATSINK COMPOUND | RS | 554-311 | A/R |
| | 920089-1 | HEATSINK TO-220 | | SEE DRG | 2 |
| | 920149 | HEATSINK TO8 | SCURIAU | TX8F 2-050-033B | 1 |
| | 605124 | 10 WAY SOCKET STRIP | AUGAT | 510-AG-910 | 1/3 |
| | 605127 | 2 WAY .1" SHORTING SKT | ASSMANN | AKSPL-G | 2 |
| | 590001 | 20mm RUBBER SLEEVE | HELLERMANN | 115x20 | 1 |
| | 540006 | 1/0.4 PTFE BLACK WIRE | | B5G210 TYPE A | A/R |
| | 630243 | GLASS BEAD 2.4% x 0.8% x 1.8 | MANSOL (PREFORMS) | M5363B/3 | 62 |
| | 900004 | SILICONE RUBBER | RS. | 555-558 | A/R |
| | 420098 | LABEL SERIAL NO | RS | 554-793 | 1 |
| | 420112-1 | LABEL SSD WARNING | | SEE DRG | 1 |

NOTES:

SEE SHEET 2 FOR LATEST ISSUE

| | | | | | | | | | | | | | | | |
|--------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ISS | | | | | | | | | | | | | | | |
| A.C.D. | | | | | | | | | | | | | | | |
| DATE | | | | | | | | | | | | | | | |
| CHKD | | | | | | | | | | | | | | | |

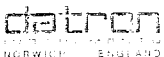
| | | |
|-----------------|-----------------------------|---------------------------------------|
| DATE 24.7.84 | | TITLE 4200 SINE SOURCE PCB ASSY |
| DRAWN IL. | | |
| CHECKED | | |
| APPROVED | | |
| DATE | DRAWING NUMBER 400446 | SHEET OF 27 |

LD400844

DOCUMENT LIST

I.O 3099 17/08/83
 I.1 3163 25/JAN/84
 I.2 3244 24/FEB/84

| REV | DRAWING NO | REVISION | DATE |
|-----|------------|----------|-----------|
| 1.0 | LD400844 | ALL | 17/08/83 |
| 1.1 | DA400844 | 1 | 25/JAN/84 |
| 1.2 | | | 24/FEB/84 |
| 1.0 | DC400844 | 1 | 17/08/83 |
| 1.0 | " | 2 | 17/08/83 |
| 1.0 | " | 3 | 17/08/83 |
| 1.0 | " | 4 | 17/08/83 |
| 1.0 | " | 5 | 17/08/83 |
| 1.0 | " | 6 | 17/08/83 |
| 1.0 | PT400844 | | |
| 1.0 | 410172 | | |

| | | | | | |
|--|--|--|--|---------------------------|--|
| <input type="checkbox"/> DENOTES NO CHANGE TO DOCS AT ISSUE LEVEL CHANGE |  datron <small>THE ELECTRONIC INSTRUMENTS GROUP</small> NGRWICH ENGLAND | ORG SRG DATE 17.10.83 | C.D. NO RS DATE 23.11.83? | TITLE AC. PCB ASSY | DRAWING NO LD400844 SHEET 1 OF 1 |
| | | DATE | DATE | DATE | |

DACRON INSTRUMENTS LTD PARTS LIST (REFERENCE) AC. PCB ASSY (FOR BOM USE) (DATE: 17/08/83) (DRAWING: LD400844)

| DESIG | PART NO | DESCRIPTION | PRIN MANUF | MATCH PART NUMBER | QTY | UNITS |
|-------|----------|---------------------|------------|-------------------|-----|-------|
| R2 | 006132 | RES CF 300 1% 12W | NEOHM | 1201 | 1 | EA |
| R3 | 006101 | RES CF 100R 5% 125W | NEOHM | 1201 | 1 | EA |
| R4 | 011001 | RES MF 1K 1% 1W | HELMSPHERE | 1201 | 1 | EA |
| R5 | 011003 | RES MF 100K 1% 1W | HELMSPHERE | 1201 | 1 | EA |
| R6 | 014001 | RES MF 4K7 1% 1W | HELMSPHERE | 1201 | 1 | EA |
| R9 | 014001 | RES MF 4K7 1% 1W | HELMSPHERE | 1201 | 1 | EA |
| R10 | 000104 | RES CF 100K 5% 125W | NEOHM | 1201 | 1 | EA |
| R11 | 000104 | RES CF 100K 5% 125W | NEOHM | 1201 | 1 | EA |
| R12 | 000104 | RES CF 100K 5% 125W | NEOHM | 1201 | 1 | EA |
| R13 | 011003 | RES MF 100K 1% 1W | HELMSPHERE | 1201 | 1 | EA |
| R14 | 011003 | RES MF 100K 1% 1W | HELMSPHERE | 1201 | 1 | EA |
| R15 | 020138-1 | RES FL 82K 1% 1/8" | VISHAY MGR | 1201 | 1 | EA |
| R16 | 000100 | RES CF 10R 5% 25W | NEOHM | 1201 | 1 | EA |
| R17 | 000100 | RES CF 10R 5% 25W | NEOHM | 1201 | 1 | EA |
| R18 | 080144 | RES FL 170R 0.1" | VISHAY MGR | 1201 | 1 | EA |
| R19 | 080144 | RES FL 170R 0.1" | VISHAY MGR | 1201 | 1 | EA |
| R20 | 080145 | RES FL 310R 0.1" | VISHAY MGR | 1201 | 1 | EA |
| R21 | 080143 | RES FL 100R 0.1" | VISHAY MGR | 1201 | 1 | EA |
| R22 | 080145 | RES FL 310R 0.1" | VISHAY MGR | 1201 | 1 | EA |
| R23 | 080143 | RES FL 100R 0.1" | VISHAY MGR | 1201 | 1 | EA |
| R24 | 000101 | RES CF 120R 5% 125W | NEOHM | 1201 | 1 | EA |
| R25 | 000100 | RES CF 10R 5% 25W | NEOHM | 1201 | 1 | EA |
| R26 | 000101 | RES CF 120R 5% 125W | NEOHM | 1201 | 1 | EA |
| R27 | 000103 | RES CF 1K 5% 125W | NEOHM | 1201 | 1 | EA |
| R28 | 000104 | RES CF 10K 5% 125W | NEOHM | 1201 | 1 | EA |
| R29 | 000104 | RES CF 10K 5% 125W | NEOHM | 1201 | 1 | EA |
| P30 | 000104 | RES CF 10K 5% 125W | NEOHM | 1201 | 1 | EA |
| P31 | 011002 | RES MF 10R 1% 1W | HELMSPHERE | 1201 | 1 | EA |
| P32 | 006101 | RES CF 100R 5% 125W | NEOHM | 1201 | 1 | EA |
| P33 | 000100 | RES CF 10R 5% 25W | NEOHM | 1201 | 1 | EA |
| R34 | 000101 | RES CF 120R 5% 125W | NEOHM | 1201 | 1 | EA |
| R36 | 000101 | RES CF 120R 5% 125W | NEOHM | 1201 | 1 | EA |
| R37 | 011002 | RES MF 10R 1% 1W | HELMSPHERE | 1201 | 1 | EA |
| R38 | 010451 | RES MF 22K 1% 1W | HELMSPHERE | 1201 | 1 | EA |
| R39 | 000104 | RES CF 10K 5% 125W | NEOHM | 1201 | 1 | EA |
| R40 | 000104 | RES CF 10K 5% 125W | NEOHM | 1201 | 1 | EA |
| R47 | 011001 | RES MF 100K 1% 1W | HELMSPHERE | 1201 | 1 | EA |
| R48 | 000220 | RES CF 10R 5% 25W | NEOHM | 1201 | 1 | EA |
| R50 | 016910 | RES MF 100K 1% 1W | HELMSPHERE | 1201 | 1 | EA |
| R51 | 000103 | RES CF 10K 5% 125W | NEOHM | 1201 | 1 | EA |
| R52 | 000103 | RES CF 10K 5% 125W | NEOHM | 1201 | 1 | EA |
| R53 | 000470 | RES CF 4K7 5% 125W | NEOHM | 1201 | 1 | EA |
| R54 | 011001 | RES MF 100K 1% 1W | HELMSPHERE | 1201 | 1 | EA |
| R55 | 000103 | RES CF 10K 5% 125W | NEOHM | 1201 | 1 | EA |
| P64 | 000103 | RES CF 10K 5% 125W | NEOHM | 1201 | 1 | EA |

Table with columns: DISPATCH, PART NO., INSTRUMENT, WINDMACHINE, MAKE, PART NUMBER, PLACE ON INSTRUMENT, COMMENTS. Contains multiple rows of instrument specifications.

Table with columns: DISPATCH, PART NO., INSTRUMENT, WINDMACHINE, MAKE, PART NUMBER, PLACE ON INSTRUMENT, COMMENTS. Contains multiple rows of instrument specifications, similar to the first table.

| DESIGN | PART NO | DESCRIPTION | PRINC MANUF | MANUF PART NUMBER | CLASS UM | QUANTITY | CHANGES |
|--------|---------|--------------------------|-------------|---------------------|----------|----------|---------|
| C19 | 104026 | CAP CD 10NF +50%-20% 50V | SIEMENS | B37449 | A | EA 2 | |
| C20 | 104026 | CAP CD 10NF +50%-20% 50V | SIEMENS | B37449 | A | EA 1 | |
| C21 | 104026 | CAP CD 10NF +50%-20% 50V | SIEMENS | B37449 | A | EA 1 | |
| C22 | 104026 | CAP CD 10NF +50%-20% 50V | SIEMENS | B37449 | A | EA 1 | |
| C23 | 104026 | CAP CD 10NF +50%-20% 50V | SIEMENS | B37449 | A | EA 1 | |
| C24 | 104026 | CAP CD 10NF +50%-20% 50V | SIEMENS | B37449 | A | EA 1 | |
| C25 | 104026 | CAP CD 10NF +50%-20% 50V | SIEMENS | B37449 | A | EA 1 | |
| C26 | 104026 | CAP CD 10NF +50%-20% 50V | SIEMENS | B37449 | A | EA 1 | |
| C27 | 104026 | CAP CD 10NF +50%-20% 50V | SIEMENS | B37449 | A | EA 1 | |
| C28 | 104026 | CAP CD 10NF +50%-20% 50V | SIEMENS | B37449 | A | EA 1 | |
| C29 | 104026 | CAP CD 10NF +50%-20% 50V | SIEMENS | B37449 | A | EA 1 | |
| C30 | 150020 | CAP CD 10NF +50%-20% 50V | AVX | TAF10M25F | A | EA 1 | |
| C31 | 150020 | CAP CD 10NF +50%-20% 50V | AVX | TAF10M25F | A | EA 1 | |
| C32 | 150020 | CAP CD 10NF +50%-20% 50V | AVX | TAF10M25F | A | EA 1 | |
| C33 | 150020 | CAP CD 10NF +50%-20% 50V | AVX | TAF10M25F | A | EA 1 | |
| C34 | 102150 | CAP CD 10PF +50%-20% 50V | BECK | CD10TH7P0M5CR/SK500 | A | EA 1 | |
| C35 | 104026 | CAP CD 10NF +50%-20% 50V | SIEMENS | B37449 | A | EA 1 | |
| C36 | 104026 | CAP CD 10NF +50%-20% 50V | SIEMENS | B37449 | A | EA 1 | |
| C37 | 104026 | CAP CD 10NF +50%-20% 50V | SIEMENS | B37449 | A | EA 1 | |
| C38 | 104026 | CAP CD 10NF +50%-20% 50V | SIEMENS | B37449 | A | EA 1 | |
| C39 | 102150 | CAP CD 10PF +50%-20% 50V | BECK | CD10TH7P0M5CR/SK500 | A | EA 1 | |
| C40 | 150020 | CAP CD 10NF +50%-20% 50V | AVX | TAF10M25F | A | EA 2 | |
| C41 | 150015 | CAP CD 10NF +50%-20% 50V | AVX | TAF10M25F | A | EA 2 | |
| C42 | 150015 | CAP CD 10NF +50%-20% 50V | AVX | TAF10M25F | A | EA 2 | |
| C43 | 101103 | CAP CD 10NF +50%-20% 50V | PHILIPS | 2222 683 34339 | A | EA 1 | |
| C44 | 101103 | CAP CD 10NF +50%-20% 50V | PHILIPS | 2222 683 34339 | A | EA 1 | |
| C45 | 100330 | CAP CD 10PF +50%-20% 50V | PHILIPS | 2222 683 34339 | A | EA 1 | |
| C46 | 100330 | CAP CD 10PF +50%-20% 50V | PHILIPS | 2222 683 34339 | A | EA 1 | |
| C47 | 150015 | CAP CD 10NF +50%-20% 50V | AVX | TAF10M25F | A | EA 1 | |
| C48 | 101103 | CAP CD 10NF +50%-20% 50V | PHILIPS | 2222 683 34339 | A | EA 1 | |
| C49 | 101103 | CAP CD 10NF +50%-20% 50V | PHILIPS | 2222 683 34339 | A | EA 1 | |
| C50 | 100330 | CAP CD 10PF +50%-20% 50V | PHILIPS | 2222 683 34339 | A | EA 1 | |
| C51 | 100330 | CAP CD 10PF +50%-20% 50V | PHILIPS | 2222 683 34339 | A | EA 1 | |
| C52 | 150015 | CAP CD 10NF +50%-20% 50V | AVX | TAF10M25F | A | EA 1 | |
| C53 | 150024 | CAP CD 10NF +50%-20% 50V | AVX | TAF10M25F | A | EA 2 | |
| C54 | 150020 | CAP CD 10NF +50%-20% 50V | AVX | TAF10M25F | A | EA 1 | |
| C55 | 150020 | CAP CD 10NF +50%-20% 50V | AVX | TAF10M25F | A | EA 1 | |
| C56 | 150024 | CAP CD 10NF +50%-20% 50V | AVX | TAF10M25F | A | EA 1 | |
| C57 | 102338 | CAP CD 10PF +50%-20% 50V | BECK | CD10TH7P0M5CR/SK500 | A | EA 1 | |
| C58 | 102150 | CAP CD 10PF +50%-20% 50V | BECK | CD10TH7P0M5CR/SK500 | A | EA 1 | |
| C59 | 102470 | CAP CD 10PF +50%-20% 50V | BECK | CD10TH7P0M5CR/SK500 | A | EA 1 | |
| C60 | 102470 | CAP CD 10PF +50%-20% 50V | BECK | CD10TH7P0M5CR/SK500 | A | EA 1 | |
| C61 | 102470 | CAP CD 10PF +50%-20% 50V | BECK | CD10TH7P0M5CR/SK500 | A | EA 1 | |
| C62 | 102470 | CAP CD 10PF +50%-20% 50V | BECK | CD10TH7P0M5CR/SK500 | A | EA 1 | |
| C63 | 102470 | CAP CD 10PF +50%-20% 50V | BECK | CD10TH7P0M5CR/SK500 | A | EA 1 | |
| C64 | 102470 | CAP CD 10PF +50%-20% 50V | BECK | CD10TH7P0M5CR/SK500 | A | EA 1 | |
| C65 | 102470 | CAP CD 10PF +50%-20% 50V | BECK | CD10TH7P0M5CR/SK500 | A | EA 1 | |
| C66 | 102470 | CAP CD 10PF +50%-20% 50V | BECK | CD10TH7P0M5CR/SK500 | A | EA 1 | |
| C67 | 102470 | CAP CD 10PF +50%-20% 50V | BECK | CD10TH7P0M5CR/SK500 | A | EA 1 | |
| C68 | 100330 | CAP CD 10PF +50%-20% 50V | PHILIPS | 2222 683 34339 | A | EA 1 | |
| C69 | 100330 | CAP CD 10PF +50%-20% 50V | PHILIPS | 2222 683 34339 | A | EA 1 | |
| C70 | 102470 | CAP CD 10PF +50%-20% 50V | BECK | CD10TH7P0M5CR/SK500 | A | EA 1 | |
| C71 | 102470 | CAP CD 10PF +50%-20% 50V | BECK | CD10TH7P0M5CR/SK500 | A | EA 1 | |
| C72 | 102470 | CAP CD 10PF +50%-20% 50V | BECK | CD10TH7P0M5CR/SK500 | A | EA 1 | |

| DESIGN | PART NO | DESCRIPTION | PRINC MANUF | MANUF PART NUMBER | CLASS UM | QUANTITY | CHANGES |
|--------|---------|---------------------------|-------------|---------------------|----------|----------|---------|
| C73 | 102470 | CAP CD 10PF +50%-20% 50V | BECK | CD10TH7P0M5CR/SK500 | A | EA 1 | |
| C74 | 102470 | CAP CD 10PF +50%-20% 50V | BECK | CD10TH7P0M5CR/SK500 | A | EA 1 | |
| C75 | 102470 | CAP CD 10PF +50%-20% 50V | BECK | CD10TH7P0M5CR/SK500 | A | EA 1 | |
| C76 | 102470 | CAP CD 10PF +50%-20% 50V | BECK | CD10TH7P0M5CR/SK500 | A | EA 1 | |
| C77 | 102470 | CAP CD 10PF +50%-20% 50V | BECK | CD10TH7P0M5CR/SK500 | A | EA 1 | |
| C78 | 100330 | CAP CD 10PF +50%-20% 50V | PHILIPS | 2222 683 34339 | A | EA 1 | |
| C79 | 101103 | CAP CD 10NF +50%-20% 50V | PHILIPS | 2222 683 34339 | A | EA 1 | |
| C80 | 102100 | CAP CD 10PF +50%-20% 50V | PHILIPS | 2222 683 34339 | A | EA 1 | |
| C81 | 100471 | CAP CD 10NF +50%-20% 50V | PHILIPS | 2222 683 34339 | A | EA 2 | |
| C82 | 100471 | CAP CD 10NF +50%-20% 50V | PHILIPS | 2222 683 34339 | A | EA 1 | |
| C83 | 104026 | CAP CD 10NF +50%-20% 50V | SIEMENS | B37449 | A | EA 1 | |
| C84 | 104026 | CAP CD 10NF +50%-20% 50V | SIEMENS | B37449 | A | EA 1 | |
| C85 | 104026 | CAP CD 10NF +50%-20% 50V | SIEMENS | B37449 | A | EA 1 | |
| C86 | 104026 | CAP CD 10NF +50%-20% 50V | SIEMENS | B37449 | A | EA 1 | |
| C87 | 100008 | CAP - 100008 FITTED | | | | EA 1 | |
| C88 | 100222 | CAP CD 20PF +50%-20% 50V | BECK | CD10K120M5CR/SK500 | A | EA 1 | |
| C89 | 100603 | CAP CD 60PF +50%-20% 50V | VISHAY | FNR2 | A | EA 1 | |
| C90 | 102101 | CAP CD 100PF +50%-20% 50V | BECK | CD10K120M5CR/SK500 | A | EA 1 | |
| C91 | 102221 | CAP CD 200PF +50%-20% 50V | BECK | CD10K120M5CR/SK500 | A | EA 1 | |
| C92 | 102470 | CAP CD 10PF +50%-20% 50V | BECK | CD10TH7P0M5CR/SK500 | A | EA 1 | |
| C93 | 150025 | CAP CD 10NF +50%-20% 50V | AVX | TAF10M25F | A | EA 1 | |
| C94 | 100330 | CAP CD 10PF +50%-20% 50V | PHILIPS | 2222 683 34339 | A | EA 1 | |
| C95 | 100418 | CAP CD 10PF +50%-20% 50V | PHILIPS | 2222 683 34339 | A | EA 1 | |
| D1 | 213006 | DIODE CN 5V 5W | UNITRODE | TVS505 | A | EA 2 | |
| D2 | 213006 | DIODE CN 5V 5W | UNITRODE | TVS505 | A | EA 1 | |
| D3 | 213012 | DIODE CR 2V0 250mW | PHILIPS | 82746-2V0 | A | EA 1 | |
| D4 | 213012 | DIODE CR 2V0 250mW | PHILIPS | 82746-2V0 | A | EA 1 | |
| D5 | 200008 | DIODE CP 200mA 100V | FAIRCHILD | 1N458A | A | EA 20 | |
| D6 | 200008 | DIODE CP 200mA 100V | FAIRCHILD | 1N458A | A | EA 1 | |
| D7 | 200008 | DIODE CP 200mA 100V | FAIRCHILD | 1N458A | A | EA 1 | |
| D8 | 200008 | DIODE CP 200mA 100V | FAIRCHILD | 1N458A | A | EA 1 | |
| D9 | 213022 | DIODE CN 10V 5W | UNITRODE | TVS510 | A | EA 4 | |
| D10 | 213022 | DIODE CN 10V 5W | UNITRODE | TVS510 | A | EA 1 | |
| D11 | 213022 | DIODE CN 10V 5W | UNITRODE | TVS510 | A | EA 1 | |
| D12 | 213022 | DIODE CN 10V 5W | UNITRODE | TVS510 | A | EA 1 | |
| D13 | 213022 | DIODE CN 10V 5W | UNITRODE | TVS510 | A | EA 1 | |
| D14 | 213009 | DIODE CN 15V 5W | UNITRODE | TVS515 | A | EA 1 | |
| D15 | 213009 | DIODE CN 15V 5W | UNITRODE | TVS515 | A | EA 1 | |
| D16 | 200002 | DIODE CP 1A 50V | FAIRCHILD | 1N4001 | A | EA 1 | |
| D17 | 213009 | DIODE CN 15V 500mW | PHILIPS | 82746-15V | A | EA 1 | |
| D20 | 200001 | DIODE CP 75mA 75V | FAIRCHILD | 1N4148 | A | EA 4 | |
| D21 | 200001 | DIODE CP 75mA 75V | FAIRCHILD | 1N4148 | A | EA 1 | |
| D22 | 200001 | DIODE CP 75mA 75V | FAIRCHILD | 1N4148 | A | EA 1 | |
| D23 | 200008 | DIODE CP 200mA 100V | FAIRCHILD | 1N458A | A | EA 1 | |
| D24 | 200001 | DIODE CP 75mA 75V | FAIRCHILD | 1N4148 | A | EA 1 | |
| D25 | 210130 | DIODE CN 10V 100mW | PHILIPS | 82746-10V | A | EA 1 | |

| DESIG | PART NO | DESCRIPTION | FRING MANUF | MANUF PART NUMBER | QUANTITY | UNIT PRICE | TOTAL |
|-------|---------|----------------------|-------------|-------------------|----------|------------|-------|
| D26 | 200032 | DIODE 20V 1A 50V | FAIRCHILD | 1N4148 | 1 | 0.10 | 0.10 |
| D27 | 200032 | DIODE 20V 1A 50V | FAIRCHILD | 1N4148 | 1 | 0.10 | 0.10 |
| D28 | 213023 | DIODE 20V 50V 50V | MOTOROLA | 1N4148 | 1 | 0.10 | 0.10 |
| D29 | 213023 | DIODE 20V 50V 50V | MOTOROLA | 1N4148 | 1 | 0.10 | 0.10 |
| D30 | 213023 | DIODE 20V 50V 400mA | MOTOROLA | 1N4148 | 1 | 0.10 | 0.10 |
| D31 | 200008 | DIODE 20V 200mA 125V | FAIRCHILD | 1N4001 | 1 | 0.10 | 0.10 |
| D32 | 210091 | DIODE 20V 200mA 125V | PHILIPS | 1N4001 | 1 | 0.10 | 0.10 |
| D33 | 200001 | DIODE 20V 75mA 75V | FAIRCHILD | 1N4148 | 1 | 0.10 | 0.10 |
| D34 | 210056 | DIODE 20V 50V 400mA | PHILIPS | 1N4001 | 1 | 0.10 | 0.10 |
| D35 | 210056 | DIODE 20V 50V 400mA | PHILIPS | 1N4001 | 1 | 0.10 | 0.10 |
| D37 | 200009 | DIODE 20V 200mA 125V | FAIRCHILD | 1N4001 | 1 | 0.10 | 0.10 |
| D38 | 200008 | DIODE 20V 200mA 125V | FAIRCHILD | 1N4001 | 1 | 0.10 | 0.10 |
| D39 | 200008 | DIODE 20V 200mA 125V | FAIRCHILD | 1N4001 | 1 | 0.10 | 0.10 |
| D40 | 200008 | DIODE 20V 200mA 125V | FAIRCHILD | 1N4001 | 1 | 0.10 | 0.10 |
| D41 | 200008 | DIODE 20V 200mA 125V | FAIRCHILD | 1N4001 | 1 | 0.10 | 0.10 |
| D42 | 213011 | DIODE 20V 125V 100mA | PHILIPS | 1N4001 | 1 | 0.10 | 0.10 |
| D43 | 213011 | DIODE 20V 125V 100mA | PHILIPS | 1N4001 | 1 | 0.10 | 0.10 |
| D44 | 200001 | DIODE 20V 75mA 75V | FAIRCHILD | 1N4148 | 1 | 0.10 | 0.10 |
| D45 | 200001 | DIODE 20V 75mA 75V | FAIRCHILD | 1N4148 | 1 | 0.10 | 0.10 |
| D46 | 200001 | DIODE 20V 75mA 75V | FAIRCHILD | 1N4148 | 1 | 0.10 | 0.10 |
| D47 | 200001 | DIODE 20V 75mA 75V | FAIRCHILD | 1N4148 | 1 | 0.10 | 0.10 |
| D49 | 200008 | DIODE 20V 200mA 125V | FAIRCHILD | 1N4001 | 1 | 0.10 | 0.10 |
| D50 | 200008 | DIODE 20V 200mA 125V | FAIRCHILD | 1N4001 | 1 | 0.10 | 0.10 |
| D52 | 200008 | DIODE 20V 200mA 125V | FAIRCHILD | 1N4001 | 1 | 0.10 | 0.10 |
| D53 | 200008 | DIODE 20V 200mA 125V | FAIRCHILD | 1N4001 | 1 | 0.10 | 0.10 |
| D54 | 200008 | DIODE 20V 200mA 125V | FAIRCHILD | 1N4001 | 1 | 0.10 | 0.10 |
| D55 | 200008 | DIODE 20V 200mA 125V | FAIRCHILD | 1N4001 | 1 | 0.10 | 0.10 |
| D56 | 200008 | DIODE 20V 200mA 125V | FAIRCHILD | 1N4001 | 1 | 0.10 | 0.10 |
| D59 | 200008 | DIODE 20V 200mA 125V | FAIRCHILD | 1N4001 | 1 | 0.10 | 0.10 |
| D60 | 200008 | DIODE 20V 200mA 125V | FAIRCHILD | 1N4001 | 1 | 0.10 | 0.10 |
| Q1 | 250004 | TRAN PNP T092 | NATIONAL | 2N3904 | 1 | 0.10 | 0.10 |
| Q2 | 230062 | TRAN JFET N-CHAN | SILICONIX | 2N3110 | 1 | 0.10 | 0.10 |
| Q3 | 230069 | TRAN JFET N-CHAN | SILICONIX | 2N3110 | 1 | 0.10 | 0.10 |
| Q4 | 230003 | TRAN JFET N-CHAN | TELETYPE | 11894JF | 1 | 0.10 | 0.10 |
| Q5 | 230003 | TRAN JFET N-CHAN | TELETYPE | 11894JF | 1 | 0.10 | 0.10 |
| Q6 | 230003 | TRAN JFET N-CHAN | TELETYPE | 11894JF | 1 | 0.10 | 0.10 |
| Q19 | 250004 | TRAN PNP T092 | NATIONAL | 2N3904 | 1 | 0.10 | 0.10 |
| Q20 | 250004 | TRAN PNP T092 | NATIONAL | 2N3904 | 1 | 0.10 | 0.10 |
| Q21 | 250004 | TRAN PNP T092 | NATIONAL | 2N3904 | 1 | 0.10 | 0.10 |
| Q22 | 230042 | TRAN JFET I LIM 3mA | SILICONIX | 2N3110 | 1 | 0.10 | 0.10 |
| Q23 | 250004 | TRAN PNP T092 | NATIONAL | 2N3904 | 1 | 0.10 | 0.10 |
| Q24 | 240006 | TRAN NPN T092 | MOTOROLA | 2N3904 | 1 | 0.10 | 0.10 |
| Q25 | 240006 | TRAN NPN T092 | MOTOROLA | 2N3904 | 1 | 0.10 | 0.10 |
| Q26 | 240025 | TRAN NPN DARL | MOTOROLA | 2N3904 | 1 | 0.10 | 0.10 |
| Q27 | 240013 | TRAN NPN T01A | NATIONAL | 2N3904 | 1 | 0.10 | 0.10 |

| DESIG | PART NO | DESCRIPTION | FRING MANUF | MANUF PART NUMBER | QUANTITY | UNIT PRICE | TOTAL |
|-------|----------|---------------------------|-------------|-------------------|----------|------------|-------|
| Q28 | 230042 | TRAN JFET I LIM 3mA | SILICONIX | 2N3110 | 1 | 0.10 | 0.10 |
| Q29 | 250004 | TRAN PNP T092 | NATIONAL | 2N3904 | 1 | 0.10 | 0.10 |
| Q30 | 250004 | TRAN PNP T092 | NATIONAL | 2N3904 | 1 | 0.10 | 0.10 |
| Q31 | 240006 | TRAN NPN T092 | MOTOROLA | 2N3904 | 1 | 0.10 | 0.10 |
| Q32 | 250004 | TRAN PNP T092 | NATIONAL | 2N3904 | 1 | 0.10 | 0.10 |
| Q33 | 250004 | TRAN PNP T092 | NATIONAL | 2N3904 | 1 | 0.10 | 0.10 |
| Q34 | 240006 | TRAN NPN T092 | MOTOROLA | 2N3904 | 1 | 0.10 | 0.10 |
| Q35 | 240006 | TRAN NPN T092 | MOTOROLA | 2N3904 | 1 | 0.10 | 0.10 |
| Q36 | 230042 | TRAN JFET I LIM 3mA | SILICONIX | 2N3110 | 1 | 0.10 | 0.10 |
| Q37 | 250008 | TRAN PNP T01A | NATIONAL | 2N3904 | 1 | 0.10 | 0.10 |
| Q38 | 239072-1 | TRAN JFET N-CHAN SELECTED | SILICONIX | 2N3110 | 1 | 0.10 | 0.10 |
| Q39 | 239072-1 | TRAN JFET N-CHAN SELECTED | SILICONIX | 2N3110 | 1 | 0.10 | 0.10 |
| Q40 | 230070 | TRAN JFET N-CHAN DARL | SILICONIX | 2N3110 | 1 | 0.10 | 0.10 |
| Q41 | 230070 | TRAN JFET N-CHAN DARL | SILICONIX | 2N3110 | 1 | 0.10 | 0.10 |
| Q42 | 230065 | TRAN JFET I LIM 3mA | SILICONIX | 2N3110 | 1 | 0.10 | 0.10 |
| Q43 | 230065 | TRAN JFET I LIM 3mA | SILICONIX | 2N3110 | 1 | 0.10 | 0.10 |
| Q46 | 230035 | TRAN JFET N-CHAN | TELETYPE | 11894JF | 1 | 0.10 | 0.10 |
| Q48 | 230029 | TRAN JFET N-CHAN | SILICONIX | 2N3110 | 1 | 0.10 | 0.10 |
| Q51 | 230029 | TRAN JFET N-CHAN | SILICONIX | 2N3110 | 1 | 0.10 | 0.10 |
| Q52 | 230003 | TRAN JFET N-CHAN | TELETYPE | 11894JF | 1 | 0.10 | 0.10 |
| M1 | 260073 | IC LIN OP AMP | INTEGRAL | LM311 | 1 | 0.10 | 0.10 |
| M2 | 260073 | IC LIN OP AMP | INTEGRAL | LM311 | 1 | 0.10 | 0.10 |
| M3 | 260042 | IC LIN OP AMP 1/2 | INTEGRAL | LM311 | 1 | 0.10 | 0.10 |
| M4 | 260108 | IC LIN OP AMP | INTEGRAL | LM311 | 1 | 0.10 | 0.10 |
| M5 | 260108 | IC LIN OP AMP | INTEGRAL | LM311 | 1 | 0.10 | 0.10 |
| M6 | 260075 | IC LIN OP AMP 2/2 | INTEGRAL | LM311 | 1 | 0.10 | 0.10 |
| M7 | 260025 | IC LIN OP AMP 2/2 | INTEGRAL | LM311 | 1 | 0.10 | 0.10 |
| M9 | 260025 | IC LIN OP AMP 2/2 | INTEGRAL | LM311 | 1 | 0.10 | 0.10 |
| M10 | 260124 | IC LIN OP AMP 1/2 | INTEGRAL | LM311 | 1 | 0.10 | 0.10 |
| M11 | 260075 | IC LIN OP AMP 2/2 | INTEGRAL | LM311 | 1 | 0.10 | 0.10 |
| M12 | 260124 | IC LIN OP AMP 1/2 | INTEGRAL | LM311 | 1 | 0.10 | 0.10 |
| M13 | 260124 | IC LIN OP AMP 1/2 | INTEGRAL | LM311 | 1 | 0.10 | 0.10 |
| M14 | 260124 | IC LIN OP AMP 1/2 | INTEGRAL | LM311 | 1 | 0.10 | 0.10 |
| M15 | 260124 | IC LIN OP AMP 1/2 | INTEGRAL | LM311 | 1 | 0.10 | 0.10 |
| M16 | 260124 | IC LIN OP AMP 1/2 | INTEGRAL | LM311 | 1 | 0.10 | 0.10 |
| M17 | 260124 | IC LIN OP AMP 1/2 | INTEGRAL | LM311 | 1 | 0.10 | 0.10 |
| M18 | 260124 | IC LIN OP AMP 1/2 | INTEGRAL | LM311 | 1 | 0.10 | 0.10 |
| M19 | 260124 | IC LIN OP AMP 1/2 | INTEGRAL | LM311 | 1 | 0.10 | 0.10 |
| M20 | 260124 | IC LIN OP AMP 1/2 | INTEGRAL | LM311 | 1 | 0.10 | 0.10 |
| M21 | 260124 | IC LIN OP AMP 1/2 | INTEGRAL | LM311 | 1 | 0.10 | 0.10 |
| M22 | 260124 | IC LIN OP AMP 1/2 | INTEGRAL | LM311 | 1 | 0.10 | 0.10 |
| M23 | 260124 | IC LIN OP AMP 1/2 | INTEGRAL | LM311 | 1 | 0.10 | 0.10 |
| M24 | 260124 | IC LIN OP AMP 1/2 | INTEGRAL | LM311 | 1 | 0.10 | 0.10 |
| M25 | 260124 | IC LIN OP AMP 1/2 | INTEGRAL | LM311 | 1 | 0.10 | 0.10 |
| M26 | 260124 | IC LIN OP AMP 1/2 | INTEGRAL | LM311 | 1 | 0.10 | 0.10 |
| M27 | 260124 | IC LIN OP AMP 1/2 | INTEGRAL | LM311 | 1 | 0.10 | 0.10 |
| M28 | 260124 | IC LIN OP AMP 1/2 | INTEGRAL | LM311 | 1 | 0.10 | 0.10 |
| M29 | 260124 | IC LIN OP AMP 1/2 | INTEGRAL | LM311 | 1 | 0.10 | 0.10 |
| M30 | 260124 | IC LIN OP AMP 1/2 | INTEGRAL | LM311 | 1 | 0.10 | 0.10 |

| DESIG | PART NO | DESCRIPTION | PRINC MANUF | MANUF PART NUMBER | CLASS | QM | QUANTITY | CHANGES |
|-------|-----------|-----------------------------|-------------|-------------------|-------|----|----------|---------|
| M27 | 280103 | IC DIS CR3 X3 | MOTOROLA | MC14018CP | EA | - | | |
| M28 | 280390 | IC DIS DRIVER EMULATING X1 | SGS | 88282CP | A | EA | 2 | |
| M29 | 280392 | IC DIS DRIVER EMULATING X2 | SGS | 88282CP | A | EA | 2 | |
| M30 | 280105 | IC DIS PHASE DETECTOR | NATIONAL | DM74C93DN | EA | 1 | | |
| M31 | 280073 | IC LIN OP AMP | NATIONAL | LM741CN | EA | - | | |
| M32 | 260087 | IC LIN OP AMP BIFET | MOTOROLA | MC14081P | EA | 1 | | |
| RL2 | 330030 | RELAY 4PNO | SGS | 64-24V | EA | 2 | | |
| RL3 | 330032 | RELAY 4PCN MINIATURE | YAMAWATA | MC1481 | EA | 1 | | |
| RL4 | 330029 | RELAY 2P2N | SGS | 652E-DC24V | EA | 11 | | |
| RL5 | 330029 | RELAY 2P2N | SGS | 652E-DC24V | EA | - | | |
| RL6 | 330029 | RELAY 2P2N | SGS | 652E-DC24V | EA | - | | |
| RL7 | 330029 | RELAY 2P2N | SGS | 652E-DC24V | EA | - | | |
| RL8 | 330029 | RELAY 2P2N | SGS | 652E-DC24V | EA | - | | |
| RL9 | 330033 | RELAY 4PNO | SGS | 64-24V | EA | - | | |
| RL10 | 330033 | RELAY 4PNO | SGS | 64-24V | EA | - | | |
| RL11 | 330031 | RELAY 4PNO 2P2N | SGS | 64-24V | EA | 1 | | |
| RL12 | 330011-3 | RELAY 4PNO REED SWITCH | HARWIN | SEE DRG | EA | 1 | | |
| RL13 | 330029 | RELAY 2P2N | SGS | 652E-DC24V | EA | - | | |
| RL14 | 330029 | RELAY 2P2N | SGS | 652E-DC24V | EA | - | | |
| RL15 | 330029 | RELAY 2P2N | SGS | 652E-DC24V | EA | - | | |
| RL16 | 330029 | RELAY 2P2N | SGS | 652E-DC24V | EA | - | | |
| RL17 | 330029 | RELAY 2P2N | SGS | 652E-DC24V | EA | - | | |
| RL18 | 330030 | RELAY 4PNO | SGS | 64-24V | EA | - | | |
| RL19 | 330030 | RELAY 4PNO | SGS | 64-24V | EA | - | | |
| RL20 | 330029 | RELAY 2P2N | SGS | 652E-DC24V | EA | - | | |
| L1 | 370001 | CHOKER RF 100H | SIGMA | SC10/25 | A | EA | 2 | |
| L2 | 370001 | CHOKER RF 100H | SIGMA | SC10/25 | A | EA | 1 | |
| L3 | 370001 | CHOKER RF 100H | SIGMA | SC10/25 | A | EA | 1 | |
| L4 | 370001 | CHOKER RF 100H | SIGMA | SC10/25 | A | EA | 1 | |
| L6 | 370001 | CHOKER RF 100H | SIGMA | SC10/25 | A | EA | - | |
| L7 | 370001 | CHOKER RF 100H | SIGMA | SC10/25 | A | EA | - | |
| L8 | 370027 | CHOKER RF 47UH 1/4 | SIC | SC30-10-2533-10 | EA | 1 | | |
| F1 | 220129 | FUSE 1A 125V TMC | LITTLEFUSE | 275-025 | EA | 2 | | |
| F2 | 220120 | FUSE 1A 125V TMC | LITTLEFUSE | 275-025 | EA | 1 | | |
| AKA | 604046 | PLUG PCB 3-WAY .1" | MOLEX | 22-10-2031 | EA | 2 | | |
| LNA | 605127 | SOCKET LINK 2-WAY .1" BLK | ASSMANN | AKSPL-6 | EA | 2 | | |
| LKB | 604046 | PLUG PCB 3-WAY .1" | MOLEX | 22-10-2031 | EA | - | | |
| LKB | 605127 | SOCKET LINK 2-WAY .1" BLK | ASSMANN | AKSPL-6 | EA | - | | |
| | 400639-1 | ASSY PCB ATTENUATOR TAPE | DATRON | SEE DRG | EA | 1 | | |
| | 400842-1 | ASSY PCB AC SENSE 4700 | DATRON | SEE DRG | EA | 1 | | |
| | 410170-11 | PCB AC 1000 | | SEE DRG | EA | 1 | | |
| | 420008 | LABEL SERIAL ASSY No. | RS | 554-730 | EA | 1 | | |
| | 420110-1 | LABEL SSC WARNING 10 X 12mm | | SEE DRG | EA | 1 | | |
| | 450424-1 | GUARD SHIELD TOP | | SEE DRG | EA | 1 | | |
| | 450425-1 | GUARD SHIELD BOTTOM | | SEE DRG | EA | 1 | | |

| DESIG | PART NO | DESCRIPTION | PRINC MANUF | MANUF PART NUMBER | CLASS | QM | QUANTITY | CHANGES |
|-------|----------|-----------------------------|----------------------|-------------------|-------|-----|----------|---------|
| | 512000 | WIRE 7/2 PTFE 1KV BLK | BSC210 | TYPE C | AR | 1 | | |
| | 512999 | WIRE 7/2 PTFE 1KV WHI | BSC210 | TYPE C | AR | 1 | | |
| | 540002 | WIRE 1/7 TINNED COPPER | BS4109 | 22SWG | AR | 1 | | |
| | 560002 | CABLE AX 2.54mm 1/34AWG | MIL-C170 | RGL74U | MM | 250 | | |
| | 590001 | SLEEVE NP 1.5 X 20MM BLK | HELLERMANN | H15 | EA | 2 | | |
| | 590004 | SLEEVE PTFE 1mm BLK | HELLERMAN | PE10 | AR | 1 | | |
| | 590006 | SLEEVE HS 2.4mm YLW | R.S.COMONENTS | 399-495 | AR | 1 | | |
| | 590007 | LACING TAPE 2.5MM | ALPHA | LC136 | AR | 1 | | |
| | 590031 | SLEEVE HS 3.2mm YLW | R.S.COMONENTS | 399-502 | AR | 1 | | |
| | 590074 | SLEEVE SOLDER DIAH.3.0 | RAYFAST | CWT-3 | EA | 1 | | |
| | 604056 | PLUG PCB 4-WAY .1" | MOLEX | 32-10-2041 | EA | 10 | | |
| | 605059 | SOCKET PCB 8-WAY DIL | JERMYN | J23-18008 | A | EA | 2 | |
| | 605060 | SOCKET PCB 14-WAY DIL | JERMYN | J23-18014 | A | EA | 12 | |
| | 605061 | SOCKET PCB 16-WAY DIL | JERMYN | J23-18016 | A | EA | 8 | |
| | 611004 | SCREW M3 X 6 POSIPAN SSP | | | EA | 1 | | |
| | 611012 | SCREW M3 X 12 POSICOR SSP | | | EA | 3 | | |
| | 612010-1 | STANDOFF M3 X 14 | DATRON | SEE DRG | EA | 1 | | |
| | 613029 | WASHER M3 WAVY SS | | | EA | 1 | | |
| | 614001-1 | SPACER M3 CLEAR X 4 | | SEE DRG | EA | 3 | | |
| | 620003 | SOLDER PIN | HARWIN | H2105A01 | EA | 3 | | |
| | 620007 | TEST POINT TERMINAL | MICROVAR | TYPE C30 | EA | 39 | | |
| | 630024 | BEAD CERAMIC 16 SWG | FARK ROYAL PORCELAIN | No2 | EA | 24 | | |
| | 630036 | BEAD CERAMIC 18 SWG | FARK ROYAL PORCELAIN | No1 | EA | 10 | | |
| | 630121 | PCB EJECTOR GREEN | RICRCD | DBE | EA | 2 | | |
| | 630243 | BEAD GLASS 2.4 X 2.81 X 1.5 | MAUSOL (PREFORMS) | LT M5363B/3 | EA | 4 | | |
| | 900004 | SILICONE RUBBER COMPOUND | RS | 555-588 | AR | 1 | | |

End

| | | | | | | |
|-----------------------------|--|-------|---------|----------|----------|-------|
| DRAWING No 400614 | | CHK'D | DATE | ECO | REVISION | ISSUE |
| L E W M | | | 10.3.85 | | | |
| | | 1.1 | 12193 | 11.7.86 | | |
| | | 1.2 | 2210 | 14.4.86 | | |
| | | 1.3 | 2235 | 28.4.86 | | |
| | | 1.4 | 2229 | 20.5.86 | | |
| | | 1.5 | 2256 | 25.6.86 | | |
| | | 1.6 | 2323 | 18.7.86 | | |
| | | 1.7 | 2365 | 29.8.86 | | |
| | | 1.8 | 2386 | 26.1.87 | | |
| | | 1.9 | 2497 | 26.1.87 | | |
| | | 1.10 | 2585 | 1.5.87 | | |
| | | 1.10 | 2591 | 12.6.87 | | |
| | | 1.10 | 2609 | 22.6.87 | | |
| | | 1.10 | 2676 | 30.04.87 | | |
| | | 1.10 | 2697 | 18.04.87 | | |
| | | 1.10 | 2749 | 2.2.88 | | |
| | | 1.11 | 2856 | 28.4.88 | | |
| | | 1.11 | 2810 | 19.6.88 | | |

| DESCRIPTION | DRAWING NUMBER | SHEET NUMBER | ISSUE | REVISION |
|-----------------------|----------------|--------------|-------|----------|
| COMPONENT LAYOUT | 480614 | 1 | 1.0 | 1.1 |
| COMPONENT LAYOUT | 480614 | 2 | 1.1 | 1.2 |
| SCHEMATIC | 430614 | 1 | 1.0 | 1.1 |
| SCHEMATIC | 430614 | 2 | 1.1 | 1.1 |
| SCHEMATIC | 430614 | 3 | 1.1 | 1.2 |
| FUNCTIONAL TEST PROC. | 460614/FT | 1-5 | 1.0 | 1.1 |
| FUNCT. TEST TICK LIST | 470614/FT | 1-2 | 1.0 | 1.1 |
| PCB | 410347 | | 1.0 | |

| | | | | | | | |
|-------|---|---|-----------------|----------------------|-----------------|-----------------------------------|---------------------------------------|
| NOTES | <input type="checkbox"/> INDICATES NO CHANGE TO DOC. AT ISSUE LEVEL CHANGE. | datron ELECTRONICS LTD NORWICH ENGLAND | DRN 1 | CHK'D R.H. COGGAN | APP'D W. | TITLE 4700 I/O PCB ASSEMBLY | DRAWING No 400614 SHEET 1 OF 15 |
| | | | DATE 13.8.85 | DATE 18/3/86 | DATE 18.3.86 | | |

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No. USED Per Assy. |
|------------|-----------------|------------------------|------------------------|-------------------------|--------------------|
| R1 | 008037 | OR18 10% 2W5 WIREWOUND | WELWYN | W21 | 1 |
| R2 | 000820 | 82R 5% 1/4W CARBON | MULLARD | CR25 | 1 |
| R3 | 000821 | 820R 5% 1/4W CARBON | MULLARD | CR25 | 1 |
| R4 | | NOT USED | | | |
| R5 | 000688 | 6R8 5% 1/4W CARBON | MULLARD | CR25 | 1 |
| R6 | 000103 | 10K 5% 1/4W CARBON | MULLARD | CR25 | 2 |
| R7 | 000103 | 10K 5% 1/4W CARBON | MULLARD | CR25 | - |
| R8 | 080084 | 90R00 -1% 3ppm M.FOIL | VISHAY | S102C | 1 |
| R9 | 080085 | 300R0 -1% 3ppm M.FOIL | VISHAY | S102C | 1 |
| R10 | 067502 | 5K POT 20TURN CERMET | BECKMAN | 68X | 2 |
| R11 | 000101 | 100R 5% 1/4W CARBON | MULLARD | CR25 | 9 |
| R12 | 000101 | 100R 5% 1/4W CARBON | MULLARD | CR25 | - |
| R13 | 000333 | 33K 5% 1/4W CARBON | MULLARD | CR25 | 2 |
| R14 | 000104 | 100K 5% 1/4W CARBON | MULLARD | CR25 | 3 |
| R15 | 000101 | 100R 5% 1/4W CARBON | MULLARD | CR25 | - |
| R16 | 000101 | 100R 5% 1/4W CARBON | MULLARD | CR25 | - |
| R17 | 000104 | 100K 5% 1/4W CARBON | MULLARD | CR25 | - |
| R18 | 012001 | 2K00 1% 1/8W 30ppm MF | HOLCO | H8C | 2 |
| R19 | 012001 | 2K00 1% 1/8W 50ppm MF | HOLCO | H8C | - |
| R20 | 011302 | 13K0 1% 1/8W 50ppm MF | HOLCO | H8C | 2 |
| R21 | 011302 | 13K0 1% 1/8W 50ppm MF | HOLCO | H8C | - |
| R22 | 000393 | 33K 5% 1/4W CARBON | MULLARD | CR25 | - |
| R23 | 067202 | 2K POT 20TURN CERMET | BECKMAN | 68X | 1 |

| | | | |
|--------|------|--------|-----------------------------------|
| ISSUED | DATE | 7.5.85 | datron ELECTRONICS LTD |
| CHK'D | | | |
| DATE | | | TITLE 4700 I/O PCB ASSEMBLY |
| CHK'D | | | DRAWING NUMBER 400614 |
| DATE | | | SHEET 2 OF 15 |

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No. USED Per Assy |
|------------|-----------------|----------------------------|------------------------|-------------------------|-------------------|
| R24 | | NOT USED | | | |
| R25 | | NOT USED | | | |
| R26 | 011001 | 1K00 1% 1/8W 50ppm MF | HOLCO | HBC | 2 |
| R27 | 012670 | 267R 1% 1/8W 50ppm MF | HOLCO | HBC | 1 |
| R28 | 011001 | 1K00 1% 1/8W 50ppm MF | HOLCO | HBC | - |
| R29 | 000101 | 100R 5% 1/4W CARBON | MULLARD | CR25 | - |
| R30 | 000101 | 100R 5% 1/4W CARBON | MULLARD | CR25 | - |
| R31 | 066200 | 20R POT 3/8 SQ VERT.CERMET | BECKMAN | 72XW | 1 |
| R32 | | NOT USED | | | |
| R33 | | NOT USED | | | |
| R34 | 000102 | 1K 5% 1/4W CARBON | MULLARD | CR25 | 3 |
| R35 | 000102 | 1K 5% 1/4W CARBON | MULLARD | CR25 | - |
| R36 | NOT USED | | | | |
| R37 | 000101 | 100R 5% 1/4W CARBON | MULLARD | CR25 | - |
| R38 | 000101 | 100R 5% 1/4W CARBON | MULLARD | CR25 | - |
| R39 | 013401 | 3K40 1% 1/8W 50ppm MF | HOLCO | HBC | 1 |
| R40 | 012002 | 20K0 1% 1/8W 50ppm MF | HOLCO | HBC | 1 |
| R41 | 000104 | 100K 5% 1/4W CARBON | MULLARD | CR25 | - |
| R42 | | NOT USED | | | |
| R43 | 080083 | 2K0000 .01% 3ppm M.FOIL | VISHAY | S102C | 3 |
| R44 | 080096 | 18K000 .01% 3ppm M.FOIL | VISHAY | S102C | 1 |
| R45 | 080082 | 20K000 .01% 3ppm M.FOIL | VISHAY | S102C | 2 |
| R46 | 080083 | 2K0000 .01% 3ppm M.FOIL | VISHAY | S102C | - |

NOTES.

SEE SHEET 1 FOR LATEST ISSUE

| | | | | | | | | | | | | | | | | | | | | |
|------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ISS | | | | | | | | | | | | | | | | | | | | |
| ECO | | | | | | | | | | | | | | | | | | | | |
| DATE | | | | | | | | | | | | | | | | | | | | |
| CHKD | | | | | | | | | | | | | | | | | | | | |

| | | |
|----------|----------|------------------------|
| DATE | 7. 5. 85 | datron ELECTRONICS LTD |
| DRAWN | LL | |
| CHECKED | | TITLE 4700 |
| APPROVED | | I/R PCB ASSEMBLY |
| DATE | | DRAWING NUMBER 400614 |
| | | 3 SHEET OF 15 |

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No. USED Per Assy |
|------------|-----------------|-------------------------|------------------------|-------------------------|-------------------|
| R47 | 080082 | 20K000 .01% 3ppm M.FOIL | VISHAY | S102C | - |
| R48 | 080083 | 2K0000 .01% 3ppm M.FOIL | VISHAY | S102C | - |
| R49 | 000100 | 10R 5% 1/4W CARBON | MULLARD | CR25 | 2 |
| R50 | 000100 | 10R 5% 1/4W CARBON | MULLARD | CR25 | - |
| R51 | 000105 | 1M 5% 1/4W CARBON | MULLARD | CR25 | 2 |
| R52 | 000153 | 15K 5% 1/4W CARBON | MULLARD | CR25 | 1 |
| R53 | 067201 | 200R POT 20TURN CERMET | BECKMAN | 68X | 1 |
| R54 | 067502 | 5K POT 20TURN CERMET | BECKMAN | 68X | - |
| R55 | 067503 | 50K POT 20TURN CERMET | BECKMAN | 68X | 1 |
| R56 | 067504 | 500K POT 20TURN CERMET | BECKMAN | 68X | 1 |
| R57 | 067205 | 2M POT 20TURN CERMET | BECKMAN | 68X | 1 |
| R58 | 067100 | 10R POT 20TURN CERMET | BECKMAN | 68X | 1 |
| R59 | 000101 | 100R 5% 1/4W CARBON | MULLARD | CR25 | - |
| R60 (FSV) | 041655 | 16M5 1% 1/2W 150ppm MF | MEPCO | 50S37L | 1 |
| R61 (FSV) | 011698 | 16R9 1% 1/8W 50ppm MF | HOLCO | HBC | 1 |
| R62 | 070134 - 3 | 99K980 50ppm WIREWOUND | MANN | SEE DRG. | 1 |
| R63 | 070133 - 3 | 10K0060 50ppm WIREWOUND | MANN | SEE DRG. | 1 |
| R64 | 070132 - 3 | 1K00040 50ppm WIREWOUND | MANN | SEE DRG. | 1 |
| R65 | 070131 - 3 | 100R040 50ppm WIREWOUND | MANN | SEE DRG. | 1 |
| R66 (FSV) | 012493 | 249K 1% 1/8W 50ppm MF | HOLCO | HBC | 1 |
| R67 | 000105 | 1M 5% 1/4W CARBON | MULLARD | CR25 | - |
| R68 (FSV) | 042264 | 2M26 1% 1/2W 100ppm CF | ALLEN BRADLEY | CC | 1 |
| R69 (FSV) | 011503 | 150K 1% 1/8W 50ppm MF | HOLCO | HBC | 1 |

NOTES.

SEE SHEET 2 FOR LATEST ISSUE

| | | | | | | | | | | | | | | | | | | | | |
|------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ISS | | | | | | | | | | | | | | | | | | | | |
| ECO | | | | | | | | | | | | | | | | | | | | |
| DATE | | | | | | | | | | | | | | | | | | | | |
| CHKD | | | | | | | | | | | | | | | | | | | | |

| | | |
|----------|----------|------------------------|
| DATE | 7. 5. 85 | datron ELECTRONICS LTD |
| DRAWN | LL | |
| CHECKED | | TITLE 4700 |
| APPROVED | | I/R PCB ASSEMBLY. |
| DATE | | DRAWING NUMBER 400614 |
| | | 4 SHEET OF 15 |

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No. USED Per Assy. |
|------------|-----------------|-------------------------|------------------------|-------------------------|--------------------|
| R70 (FSV) | 012672 | 26K7 1% 1/8W 50ppm MF | HOLCO | H8C | 1 |
| R71 * | 080097-1 | 99M8 0.1% 15ppm MF | CADDOCK | SEE DRG. | 1 |
| R72 | 070130-3 | 10R0040 50ppm WIREWOUND | MANN | SEE DRG. | 1 |
| R73 | 070136-3 | 9M9940 50ppm WIREWOUND | MANN | SEE DRG. | 1 |
| R74 | 070196-1 | 999K70 50ppm WIREWOUND | MANN | SEE DRG. | 1 |
| R75 (FSV) | 014991 | 4K99 1% 1/8W 50ppm MF | HOLCO | H8C | 1 |
| R76 (FSV) | 012670 | 267R 1% 1/8W 50ppm MF | HOLCO | H8C | 1 |
| R77 | 064104 | 100K POT 15TURN CERMET | BECKMAN | 89P | 1 |
| R78 | 064202 | 2K POT 15TURN CERMET | BECKMAN | 89P | 1 |
| R79 | 080081-1 | 10R00 0.1% | VISHAY | SEE DRG. | 1 |
| R80 | 080022-1 | 0R100 1% | ISABELLENHUTE | SEE DRG. | 1 |
| R81 | 000471 | 470R 5% 1/4W CARBON | MULLARD | CR25 | 1 |
| R82 | 041825 | 18M2 1% 1/2W 100ppm CF | ALLEN BRADLEY | CC | 2 |
| R83 | 041825 | 18M2 1% 1/2W 100ppm CF | ALLEN BRADLEY | CC | - |
| R84 | | NOT USED | | | |
| R85 | 000222 | 2k2 5% 1/4W CARBON | MULLARD | CR25 | 1 |
| R86 | 000102 | 1k 5% 1/4W CARBON | MULLARD | CR25 | - |
| AN1 | 090096 | 1MX8 2% NETWORK | AB | 850-91-1M | 2 |
| AN2 | 090085 | 12KX8 2% NETWORK | AB | 761-3-12K | 1 |
| AN3 | 090096 | 1MX8 2% NETWORK | AB | 850-91-1M | - |
| AN4 | 090131 | 10K X4 2% NETWORK | AB | L08-3-R10K | 2 |
| AN5 | 090131 | 10K X4 2% NETWORK | AB | L08-3-R10K | - |

NOTES: * R71 ALTERNATIVE R71 A AND B 49M9 0.1% 25ppm 2 OFF 080098-1

SEE SHEET 2 FOR LATEST ISSUE

| | | | | | | | | | | |
|------|--|--|--|--|--|--|--|--|--|--|
| ISS | | | | | | | | | | |
| ECO | | | | | | | | | | |
| DATE | | | | | | | | | | |
| CHKD | | | | | | | | | | |

| | | | |
|----------|--------|------------------------|---------|
| DATE | 7 5 85 | datron ELECTRONICS LTD | |
| DRAWN | IL | TITLE | 4700 |
| CHECKED | | I/O PCB ASSEMBLY | |
| APPROVED | | DRAWING NUMBER | 400614 |
| DATE | | SHEET | 5 OF 15 |

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No. USED Per Assy. |
|------------|-----------------|-----------------------|------------------------|-------------------------|--------------------|
| R87 | 000274 | 270k 5% 1/4W CARBON | MULLARD | CR25 | 2 |
| R88 | 000274 | 270k 5% 1/4W CARBON | MULLARD | CR25 | - |
| R89 | 000220 | 22R 5% 1/4W CARBON | MULLARD | CR25 | 1 |
| R90 | | NOT USED | | | - |
| R91 | 014322 | 43K2 1% 1/8W 50ppm MF | HOLCO | H8C | 2 |
| R92 | 014322 | 43K2 1% 1/8W 50ppm MF | HOLCO | H8C | - |
| R93 | 012742 | 27K4 1% 1/8W 50ppm MF | HOLCO | H8C | 2 |
| R94 | 012742 | 27K4 1% 1/8W 50ppm MF | HOLCO | H8C | - |
| R95 | 012212 | 22K1 1% 1/8W 50ppm MF | HOLCO | H8C | 1 |
| R96 | 014992 | 49K9 1% 1/8W 50ppm MF | HOLCO | H8C | 1 |
| R97 | 019091 | 9K09 1% 1/8W 50ppm MF | HOLCO | H8C | 1 |

NOTES

SEE SHEET 2 FOR LATEST ISSUE

| | | | | | | | | | | |
|------|--|--|--|--|--|--|--|--|--|--|
| ISS | | | | | | | | | | |
| ECO | | | | | | | | | | |
| DATE | | | | | | | | | | |
| CHKD | | | | | | | | | | |

| | | | |
|----------------|---------|------------------------|---------|
| DATE | 10 3 86 | datron ELECTRONICS LTD | |
| TITLE | 4700 | I/O PCB ASSEMBLY | |
| DRAWING NUMBER | 400614 | SHEET | 6 OF 15 |

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No. USED Per Assy. |
|------------|-----------------|------------------------------|------------------------|-------------------------|--------------------|
| C1 | 104026 | 47nF $\pm 50\%$ 50V CER DISC | SIEMENS | B37449 | 17 |
| C2 | 104026 | 47nF $\pm 50\%$ 50V CER DISC | SIEMENS | B37449 | - |
| C3 | | NOT USED | | | - |
| C4 | 110035 | 220nF 20% 63V POLYESTER | WIMA | MK52 | 2 |
| C5 | 104026 | 47nF $\pm 50\%$ 50V CER DISC | SIEMENS | B37449 | - |
| C6 | 104026 | 47nF $\pm 50\%$ 50V CER DISC | SIEMENS | B37449 | - |
| C7 | 104026 | 47nF $\pm 50\%$ 50V CER DISC | SIEMENS | B37449 | - |
| C8 | NOT USED | | | | - |
| C9 | NOT USED | | | | - |
| C10 | NOT USED | | | | - |
| C11 | NOT USED | | | | - |
| C12 | 104026 | 47nF $\pm 50\%$ 50V CER DISC | SIEMENS | B37449 | - |
| C13 | 150016 | 1μF 20% 35V DIP TANT | UNION CARBIDE | K10E35 | 2 |
| C14 | 104026 | 47nF $\pm 50\%$ 50V CER DISC | SIEMENS | B37449 | - |
| C15 | 110042 | 100nF 20% 63V POLYESTER | WIMA | MK52 | 3 |
| C16 | 110042 | 100nF 20% 63V POLYESTER | WIMA | MK52 | - |
| C17 | 110035 | 220nF 20% 63V POLYESTER | WIMA | MK52 | - |
| C18 | 110042 | 100nF 20% 63V POLYESTER | WIMA | MK52 | - |
| C19 | 150020 | 10μF 20% 25V DIP TANT | UNION CARBIDE | K10E25 | 4 |
| C20 | 104026 | 47nF $\pm 50\%$ 50V CER DISC | SIEMENS | B37449 | - |
| C21 | 104026 | 47nF $\pm 50\%$ 50V CER DISC | SIEMENS | B37449 | - |
| C22 | 150004 | 100μF 20% 6V3 DIP TANT | UNION CARBIDE | K100E6V3 | 1 |
| C23 | 150020 | 10μF 20% 25V DIP TANT | UNION CARBIDE | K10E25 | - |

NOTES.

SEE SHEET 2 FOR LATEST ISSUE

| ISS | ECO | DATE | CHKD |
|-----|-----|------|------|
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |

| DATE | TITLE | DRAWING NUMBER | SHEET OF |
|--------|--------------------------------|------------------|----------|
| 7 5 85 | datron ELECTRONICS LTD 4700 | I/Ω PCB ASSEMBLY | 7 OF 15 |

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No. USED Per Assy. |
|------------|-----------------|------------------------------|------------------------|-------------------------|--------------------|
| C24 | 104026 | 47nF $\pm 50\%$ 50V CER DISC | SIEMENS | B37449 | - |
| C25 | 104026 | 47nF $\pm 50\%$ 50V CER DISC | SIEMENS | B37449 | - |
| C26 | 150020 | 10μF 20% 25V DIP TANT | UNION CARBIDE | K10E25 | - |
| C27 | 104026 | 47nF $\pm 50\%$ 50V CER DISC | SIEMENS | B37449 | - |
| C28 | 150020 | 10μF 20% 25V DIP TANT | UNION CARBIDE | K10E25 | - |
| C29 | 150005 | 2μ2F 20% 16V DIP TANT | UNION CARBIDE | K2R2E16 | 2 |
| C30 | 150005 | 2μ2F 20% 16V DIP TANT | UNION CARBIDE | K2R2E16 | - |
| C31 | 102100 | 10pF 5% 500V CER DISC | ITT | CD10 | 1 |
| C32 | 150016 | 1μF 20% 35V DIP TANT | UNION CARBIDE | K10E35 | - |
| C33 | 104026 | 47nF $\pm 50\%$ 50V CER DISC | SIEMENS | B37449 | - |
| C34 | 104026 | 47nF $\pm 50\%$ 50V CER DISC | SIEMENS | B37449 | - |
| C35 | 104026 | 47nF $\pm 50\%$ 50V CER DISC | SIEMENS | B37449 | - |
| C36 | 150021 | 22μF 20% 25V DIP TANT | UNION CARBIDE | K22E25 | 2 |
| C37 | 150021 | 22μF 20% 25V DIP TANT | UNION CARBIDE | K22E25 | - |
| C38 | 104026 | 47nF $\pm 50\%$ 50V CER DISC | SIEMENS | B37449 | - |
| C39 | 104026 | 47nF $\pm 50\%$ 50V CER DISC | SIEMENS | B37449 | - |
| C40 | 140054 | 1nF 20% 400V AC POLYPROP | WIMA | FKP1 | 3 |
| C41 | 140054 | 1nF 20% 400V AC POLYPROP | WIMA | FKP1 | - |
| C42 | 140054 | 1nF 20% 400V AC POLYPROP | WIMA | FKP1 | - |
| C43 | 102330 | 33pF 5% 500V CER DISC | ITT | CD10 | 2 |
| C44 | 102470 | 47pF 5% 500V CER DISC | ITT | CD10 | 2 |
| C45 | | NOT USED | | | - |
| C46 | 102101 | 100pF 10% 500V CER DISC | ITT | CD10 | 1 |

NOTES.

SEE SHEET 2 FOR LATEST ISSUE

| ISS | ECO | DATE | CHKD |
|-----|-----|------|------|
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |

| DATE | TITLE | DRAWING NUMBER | SHEET OF |
|--------|--------------------------------|------------------|----------|
| 7 5 85 | datron ELECTRONICS LTD 4700 | I/Ω PCB ASSEMBLY | 8 OF 15 |

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No. USED Per Assy. |
|------------|-----------------|-----------------------|------------------------|-------------------------|--------------------|
| C47 | 102330 | 33pF 5% 500V CER DISC | ITT | CD10 | - |
| C48 | 102270 | 27pF 5% 500V CER DISC | ITT | CD10 | 1 |
| C49 | 102470 | 47pF 5% 500V CER DISC | ITT | CD10 | - |
| D1 | 200001 | 75mA 75V GP SI DIODE | FAIRCHILD | IN4148 | 5 |
| D2 | 200001 | 75mA 75V GP SI DIODE | FAIRCHILD | IN4148 | - |
| D3 | 210062 | 6V2 400mW ZENER | MULLARD | BZY88C | 2 |
| D4 | 210062 | 6V2 400mW ZENER | MULLARD | BZY88C | - |
| D5 | 213012 | 2V0 250mW REG DIODE | MULLARD | BZV46-2V0 | 1 |
| D6 | 210033 | 3V3 400mW ZENER | MULLARD | BZY88C3V3 | 1 |
| D7 | 213009 | 15V 5W ZENER | UNITRODE | TV5515 | 4 |
| D8 | 200001 | 75mA 75V GP SI DIODE | FAIRCHILD | IN4148 | - |
| D9 | 200001 | 75mA 75V GP SI DIODE | FAIRCHILD | IN4148 | - |
| D10 | 200001 | 75mA 75V GP SI DIODE | FAIRCHILD | IN4148 | - |
| D11 | 213009 | 15V 5W ZENER | UNITRODE | TV5515 | - |
| D12 | 213009 | 15V 5W ZENER | UNITRODE | TV5515 | - |
| D13 | 213009 | 15V 5W ZENER | UNITRODE | TV5515 | - |
| D14 | NOT USED | | | | - |
| D15 | NOT USED | | | | - |
| D16 | 200002 | 1A 50V GP SI DIODE | FAIRCHILD | IN4001 | 2 |
| D17 | 200002 | 1A 50V GP SI DIODE | FAIRCHILD | IN4001 | - |
| D18 | 213006 | 5V 5W ZENER | UNITRODE | TV5505 | 2 |

NOTES

SEE SHEET 2 FOR LATEST ISSUE

| REV | DATE | BY | CHKD |
|-----|------|----|------|
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |

| | |
|----------------|---------------------------|
| DATE 7 5 85 | datron ELECTRONICS LTD |
| DRAWN | |
| CHECKED | TITLE 4700 |
| APPROVED | I/O PCB ASSEMBLY |
| DATE | DRAWING NUMBER 400614 |
| | SHEET 9 of 15 |

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No. USED Per Assy. |
|------------|-----------------|--------------------|------------------------|-------------------------|--------------------|
| D19 | 213006 | 5V 5W ZENER | UNITRODE | TV5505 | - |
| | | | | | - |
| | | | | | - |
| | | | | | - |
| Q1 | 250011 | SI PNP TRANSISTOR | NATIONAL | BC327/T018 | 1 |
| Q2 | 230001 | N-CHAN I LIM 1.4mA | SILICONIX | J506 | 3 |
| Q3 | 250004 | SI PNP TRANSISTOR | NATIONAL | 2N3906/T092 | 1 |
| Q4 | 230001 | N-CHAN I LIM 1.4mA | SILICONIX | J506 | - |
| Q5 | 240006 | SI NPN TRANSISTOR | NATIONAL | 2N3904/T092 | 2 |
| Q6 | 230031 | N-CHAN DUAL J FET | SILICONIX | U404 | 1 |
| Q7 | 230036 | N-CHAN J FET | SILICONIX | J108 | - |
| Q8 | | NOT USED | | | - |
| Q9 | 230001 | N-CHAN I LIM 1.4mA | | J506 | - |
| Q10 | | NOT USED | | | - |
| Q11 | 240006 | SI NPN TRANSISTOR | NATIONAL | 2N3904/T092 | - |

NOTES

SEE SHEET 2 FOR LATEST ISSUE

| REV | DATE | BY | CHKD |
|-----|------|----|------|
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |

| | |
|----------------|---------------------------|
| DATE 7 5 85 | datron ELECTRONICS LTD |
| DRAWN | |
| CHECKED | TITLE 4700 |
| APPROVED | I/O PCB ASSEMBLY |
| DATE | DRAWING NUMBER 400614 |
| | SHEET 10 of 15 |

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No. USED Per Assy. |
|------------|-----------------|----------------------|------------------------|-------------------------|--------------------|
| M1 | 260069 | 4II OP AMP | NATIONAL | LF411CH | 2 |
| M2 | NOT USED | | | | - |
| M3 | 260083 | LTC1052CN OP AMP | LINEAR TECHNOLOGY | LTC 1052 CN | 1 |
| M4 | 260065 | OP27 OP AMP | PMI | OP27FZ | 2 |
| M5 | NOT USED | | | | - |
| M6 | 280035 | BCD/DECIMAL DECODER | MOTOROLA | MC14023 BCP | 2 |
| M7 | 260069 | 4II OP AMP | NATIONAL | LF411CH | - |
| M8 | 260065 | OP27 OP AMP | PMI | OP27FZ | - |
| M9 | 280045 | TRIPLE 3 I/P NOR | MOTOROLA | MC14025 BCP | 2 |
| M10 | 260086 | DUAL POWER AUDIO AMP | NATIONAL | LM1877N | 1 |
| M11 | NOT USED | | | | - |
| M12 | 280050 | 7X DARLINGTON DRIVER | SPRAGUE / EXAR | ULN2002A / XR2202CP | 1 |
| M13 | NOT USED | | | | - |
| M14 | NOT USED | | | | - |
| M15 | 260039 | 321 QUAD OP AMP | NATIONAL | LM324N | 1 |
| M16 | 280023 | QUAD 2 I/P NOR | MOTOROLA | MC14001UBCP | 1 |
| M17 | 280017 | HEX INVERTER | MOTOROLA | MC14069UBCP | 1 |
| M18 | NOT USED | | | | - |
| M19 | 280045 | TRIPLE 3 I/P NOR | MOTOROLA | MC14025 BCP | - |
| M20 | 260042 | 5532 DUAL OP AMP | SIGNETICS | NE5532N | 1 |

NOTES

SEE SHEET 2 FOR LATEST ISSUE

| | | | | | | | | | | | | | | | | | | | | |
|------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ISS | | | | | | | | | | | | | | | | | | | | |
| ECN | | | | | | | | | | | | | | | | | | | | |
| DATE | | | | | | | | | | | | | | | | | | | | |
| CHKD | | | | | | | | | | | | | | | | | | | | |

| | | |
|----------|--------|------------------------|
| DATE | 7.5.85 | datron ELECTRONICS LTD |
| DRAWN | L | |
| CHECKED | | TITLE 4700 |
| APPROVED | | I/Ω PCB ASSEMBLY |
| DATE | | DRAWING NUMBER 400614 |
| | | SHEET 11 OF 15 |

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No. USED Per Assy. |
|------------|-----------------|-----------------------|------------------------|-------------------------|--------------------|
| RL1 | 330042-2 | RELAY 3P N/O 1P N/C | | SEE DRG | 1 |
| RL2 | 330012-3 | RELAY REED 1A GUARDED | HAMLIN | HE721A5134 | 4 |
| RL3 | 330012-3 | RELAY REED 1A GUARDED | HAMLIN | HE721A5134 | - |
| RL4 | 330012-3 | RELAY REED 1A GUARDED | HAMLIN | HE721A5134 | - |
| RL5 | 330012-3 | RELAY REED 1A GUARDED | HAMLIN | HE721A5134 | - |
| RL6 | | NOT USED | | | - |
| RL7 | 330039 | RELAY 4POLE N/O | SDS | S4-L-6V | 12 |
| RL8 | 330029 | RELAY 2P2W | SDS | DS2E-M-DC24V | 2 |
| RL9 | 330029 | RELAY 2P2W | SDS | DS2E-M-DC24V | - |
| RL10 | 330039 | RELAY 4P N/O | SDS | S4-L-6V | - |
| RL11 | 330039 | RELAY 4P N/O | SDS | S4-L-6V | - |
| RL12 | 330039 | RELAY 4P N/O | SDS | S4-L-6V | - |
| RL13 | 330039 | RELAY 4P N/O | SDS | S4-L-6V | - |
| RL14 | 330039 | RELAY 4P N/O | SDS | S4-L-6V | - |
| RL15 | | NOT USED | | | - |
| RL16 | 330039 | RELAY 4P N/O | SDS | S4-L-6V | - |
| RL17 | 330039 | RELAY 4P N/O | SDS | S4-L-6V | - |
| RL18 | 330039 | RELAY 4P N/O | SDS | S4-L-6V | - |
| RL19,20,23 | 330039 | RELAY 4P N/O | SDS | S4-L-6V | - |
| RL24,25 | 330030 | RELAY 4P N/O | SDS | S4-24V | 2 |
| RL26 | 330040 | RELAY 1P 2W | SDS | DS1E-SL-6V | 1 |

NOTES

SEE SHEET 2 FOR LATEST ISSUE

| | | | | | | | | | | | | | | | | | | | | |
|------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ISS | | | | | | | | | | | | | | | | | | | | |
| ECN | | | | | | | | | | | | | | | | | | | | |
| DATE | | | | | | | | | | | | | | | | | | | | |
| CHKD | | | | | | | | | | | | | | | | | | | | |

| | | |
|----------|--------|------------------------|
| DATE | 7.5.85 | datron ELECTRONICS LTD |
| DRAWN | L | |
| CHECKED | | TITLE 4700 |
| APPROVED | | I/Ω PCB ASSEMBLY |
| DATE | | DRAWING NUMBER 400614 |
| | | SHEET 12 OF 15 |

| DESIGNATOR | DATRON PART No | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No | |
|------------|----------------|--|------------------------|------------------------|-------|
| L1 | 370001 | 10 μ H 0.85 Ω RF CHOKE | PLESSEY | 58/10/0011/10 | 2 |
| L2 | 370001 | 10 μ H 0.85 Ω RF CHOKE | PLESSEY | 58/10/0011/10 | - |
| | 400669-1 | I/ Ω CLAMP ASSY | DATRON | | 1 |
| | 410347-1 | I/ Ω PRINTED CIRCUIT BOARD | | | 1 |
| | 450419-2 | CURRENT HEATSINK | | | 1 |
| | 512000 | 7/0.2 PTFE WIRE BLACK | | | A/R |
| | 512222 | 7/0.2 PTFE WIRE RED | | | A/R |
| | 512333 | 7/0.2 PTFE WIRE ORANGE | | | A/R |
| | 512444 | 7/0.2 PTFE WIRE YELLOW | | | A/R |
| | 512555 | 7/0.2 PTFE WIRE GREEN | | | A/R |
| | 512666 | 7/0.2 PTFE WIRE BLUE | | | A/R |
| | 512888 | 7/0.2 PTFE WIRE GREY | | | A/R |
| | 540002 | 22SWG TINNED COPPER WIRE. | | | A/R |
| | 512999 | 7/0.2 WHITE PTFE INSULATED WIRE | | | A/R |
| | 540006 | 1/0.4 BLK. PTFE INST WIRE | | TO 850210 TYPEA | A/R |
| | 560008 | 4 CORE PTFE SCREENED 19/0.15 CABLE | | SEE DRG. | 370mm |
| | 590001 | SLEEVE ϕ 3 MAX CABLE | HELLERMANN ELECTRIC | H15 x 20mm BLK | 12 |
| | 590029 | HEATSHRINK SLEEVE ^{POLYOLEFIN} ϕ 3 | HELLERMANN ELECTRIC | SFM9-3BK | 20mm |
| | 590076 | SOLDER SLEEVE ϕ 7.3 | RAYFAST | CWT-7 | 1 |
| | 590007 | LACING CORD | | | A/R |

NOTES.

SEE SHEET 2 FOR LATEST ISSUE

| | | | | | | | | | | | | | | | | | | | |
|-------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ISS | | | | | | | | | | | | | | | | | | | |
| E.C.D | | | | | | | | | | | | | | | | | | | |
| DATE | | | | | | | | | | | | | | | | | | | |
| CHKD | | | | | | | | | | | | | | | | | | | |

| | | | |
|----------|--------|--------------------------|----------|
| DATE | 7.5.85 | datron ELECTRONICS LTD | |
| DRAWN | L | TITLE | 4700 |
| CHECKED | | I/ Ω PCB ASSEMBLY | |
| APPROVED | | DRAWING NUMBER | 400614 |
| DATE | | SHEET | 13 OF 15 |

| DESIGNATOR | DATRON PART No | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No | No USED For Assy |
|------------|----------------|--------------------------|------------------------|------------------------|------------------|
| J1 | 604033 | 4WAY .1" PCB PLUG GD.PL. | MOLEX | 22-29-2041 | 2 |
| | 602001 | FSV TERMINAL | MOLEX | 0204-5114 | 16 |
| | 605059 | 8WAY DIL SOCKET | | | 3 |
| | 605060 | 14WAY DIL SOCKET | | | 7 |
| | 605061 | 16WAY DIL SOCKET | | | 3 |
| | 605052 | 8WAY .1" HOUSING | MOLEX | 22-01-2085 | 1 |
| | 611008 | M3X10mm POZI-CSK STEEL | ZN PL | | 2 |
| | 611004 | M3X6mm POZI-PAN STEEL | ZN PL | | 3 |
| | 611015 | M3X8mm POZI-CSK STEEL | ZN PL | | 2 |
| | 605057 | CRIMP TERMINAL GD.PL. | MOLEX | 4809-GL | 8 |
| | 605070 | 20WAY DIL SOCKET | | | 2 |
| | 613029 | M3 WAVY WASHER SS | | | 5 |
| | 613017 | M3 FLAT WASHER NYLON | | | 34 |
| | 615002 | M3 FULL NUT STEEL ZN.PL. | | | 4 |
| * | 618001 | INSULATING BUSH TO 220 | MULLARD | 56359C | 2 |
| | 620001 | CLOVERLEAF PTFE INSUL. | SEAELECTRO | FTE12P59 | 16 |
| | 620003 | SOLDER PIN | HARWIN | H 2105 A01 | 9 |
| | 620005 | CLOVERLEAF PTFE INSUL. | SEAELECTRO | FTE15P59 | 20 |
| | 620007 | TEST POINT TERMINAL | MICROYAR | TYPE C30 | 11 |
| ** | 620005 | CLOVERLEAF PTFE INSU | SEAELECTRO | FTE15P59 | 1 |

NOTES: * INSULATING BUSH REQUIRED ONLY WHEN VISHAY RESISTOR ALTERNATIVE USED. (R79)
 ** CLOVERLEAF REQUIRED ONLY WHEN R71 'A' AND 'B' ALTERNATIVE USED

| | | | | | | | | | | | | | | | | | | | |
|-------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ISS | | | | | | | | | | | | | | | | | | | |
| E.C.D | | | | | | | | | | | | | | | | | | | |
| DATE | | | | | | | | | | | | | | | | | | | |
| CHKD | | | | | | | | | | | | | | | | | | | |

| | | | |
|----------|--------|--------------------------|----------|
| DATE | 7.5.85 | datron ELECTRONICS LTD | |
| DRAWN | L | TITLE | 4700 |
| CHECKED | | I/ Ω PCB ASSEMBLY | |
| APPROVED | | DRAWING NUMBER | 400614 |
| DATE | | SHEET | 14 OF 15 |

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No. USED Per Assy. |
|------------|-----------------|------------------------------|------------------------|-------------------------|--------------------|
| | 630003 | P CLIP ϕ 4.8 mm | SES | CNS | 2 |
| | 630024 | STEATITE BEAD 16 SWG | PARK ROYAL PORCELAIN | Nº2 | 14 |
| | 630036 | STEATITE BEAD 18 SWG | PARK ROYAL PORCELAIN | Nº1 | 16 |
| | 630122 | PCB EJECTOR BLUE | RICHCO | CBE | 2 |
| | 630167 | FOAM TAPE 6mmT x 9mm W | TESA | TESAMOLL 761/4763 | A/R |
| | 630243 | GLASS BEAD 2.4% x 0.8' x 1.8 | MANSOL (PREFORMS) | M5363B/3 | 32 |
| | 900003 | HEAT SINK COMPOUND | RS | 554-311 | A/R |
| | | | | | |
| F1 | | NOT USED | | | |
| F2 | 920124 | FUSE 375mA 125V 7mm | LITTLE FUSE | 275-375 | 2 |
| F3 | 920120 | FUSE 1A 125V 7mm | LITTLE FUSE | 275 001 | 1 |
| F4 | 920124 | FUSE 375mA 125V 7mm | LITTLE FUSE | 275-375 | - |
| F5 | 920125 | FUSE 2 1/2 A 125V 7mm | LITTLE FUSE | 275 02.5 | 1 |
| | | | | | |
| | 613005 | M3 SHAKEPROOF WASHER | STEEL | | 2 |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |

NOTES.

SEE SHEET 2 FOR LATEST ISSUE

| | | | | | | | | | | | | | | | | | | | | |
|------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ISS | | | | | | | | | | | | | | | | | | | | |
| E CD | | | | | | | | | | | | | | | | | | | | |
| DATE | | | | | | | | | | | | | | | | | | | | |
| CHKD | | | | | | | | | | | | | | | | | | | | |

| | | | |
|----------|--------|------------------------|----------|
| DATE | 7.5.85 | datron ELECTRONICS LTD | |
| DRAWN | | TITLE | 4700 |
| CHECKED | | I/Ω PCB ASSEMBLY | |
| APPROVED | | DRAWING NUMBER | 400614 |
| DATE | | SHEET | 15 OF 15 |

| DRAWING No | | CHKD | DATE | ECO | REVISION | ISSUE |
|----------------------|----------------|--------------|------------------|-----|----------|-------|
| 400618 | | | | | | |
| CEWM | | | | | | |
| | | 1.0 | 21.06.86 | AKC | | |
| | | 2.0 | 22.11.86 | | | |
| | | 2.1 | 21.7.86 | | | |
| | | 2.2 | 23.05.86 | | | |
| | | 2.3 | 23.06.86 | | | |
| | | 3.0 | 23.09.86 | | | |
| | | 3.1 | 24.6.86 | | | |
| | | 4.0 | 26.03.87 | | | |
| | | 4.1 | 25.12.87 | | | |
| | | 4.2 | 26.42.87 | | | |
| | | 4.3 | 26.03.88 | | | |
| | | 4.3 | 27.3.88 | | | |
| | | 4.4 | 27.15.88 | | | |
| | | 4.4 | 29.6.88 | | | |
| | | 4.5 | 29.55.88 | | | |
| | | 4.6 | 30.08.88 | | | |
| | | 5.0 | 32.15.88 | | | |
| | | 5.1 | 32.73.88 | | | |
| DESCRIPTION | DRAWING NUMBER | SHEET NUMBER | ISSUE - REVISION | | | |
| COMPONENT LAYOUT | 480618 | 1 | 1.0 | 2.0 | | |
| L.P. | 400618 | ALL | | | | |
| SCHEMATIC | 430618 | 1 | 1.0 | 2.0 | | |
| SCHEMATIC | 430618 | 2 | | | | |
| SCHEMATIC | 430618 | 3 | | | | |
| SCHEMATIC | 430618 | 4 | | | | |
| SCHEMATIC | 430618 | 5 | | | | |
| SCHEMATIC | 430618 | 6 | | | | |
| FUNCTIONAL TEST PROC | 460618/FT | ALL | 1.0 | 2.0 | | |
| FUNC. TEST TICK LIST | 470618/FT | ALL | 1.0 | 2.0 | | |
| PCB | 410339 | | 1.0 | 2.0 | | |

NOTES

DENOTES NO CHANGE TO DOC AT ISSUE LEVEL CHANGE.

datron ELECTRONICS LTD NORWICH ENGLAND

DRN: 11 DATE: 11.3.86

CHKD: R.M. COGGAN DATE: 17/3/86

APPD: [Signature] DATE: 18.3.86

TITLE: 4700 PA PCB ASSY

DRAWING No: 400618 SHEET 1 OF 24

| DESIGNATOR | DATRON PART No | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No | No USED Per Assy |
|------------|----------------|-----------------------|------------------------|------------------------|------------------|
| R1 | 000222 | 2k2 5% 1/3W CARBON | MULLARD | CR25 | 3 |
| R2 | 000272 | 2k7 5% 1/3W CARBON | MULLARD | CR25 | 2 |
| R3 | 006105 | 1M 2% 1W MET-OX | ELECTROSIL | FPI | 2 |
| R4 | 006105 | 1M 2% 1W MET-OX | ELECTROSIL | FPI | - |
| R5 | 000152 | 1k5 5% 1/3W CARBON | MULLARD | CR25 | 1 |
| R6 | 000330 | 33R 5% 1/3W CARBON | MULLARD | CR25 | 1 |
| R7 | 013161 | 3k16 1% 1/8W 50ppm MF | HOLCO | H8C | 2 |
| R8 | 013161 | 3k16 1% 1/8W 50ppm MF | HOLCO | H8C | - |
| R9 | 007100 | 10R 2% 2W MET-OX | ELECTROSIL | FP2 | 2 |
| R10 | 015620 | 562R 1% 1/8W 50ppm MF | HOLCO | H8C | 3 |
| R11 | 007393 | 39k 2% 2W MET-OX | ELECTROSIL | FP2 | 2 |
| R12 | 007474 | 470k 2% 2W MET-OX | ELECTROSIL | FP2 | 1 |
| R13 | 001561 | 560R 5% 1/2W CARBON | MULLARD | CR37 | 1 |
| R14 | 000123 | 12k 5% 1/3W CARBON | MULLARD | CR25 | 3 |
| R15 | 000222 | 2k2 5% 1/3W CARBON | MULLARD | CR25 | - |
| R16 | 018251 | 8k25 1% 1/8W 50ppm MF | HOLCO | H8C | 2 |
| R17 | 018251 | 8k25 1% 1/8W 50ppm MF | HOLCO | H8C | - |
| R18 | 000272 | 2k7 5% 1/3W CARBON | MULLARD | CR25 | - |
| R19 | 000101 | 100R 5% 1/3W CARBON | MULLARD | CR25 | 4 |
| R20 | 000103 | 10k 5% 1/3W CARBON | MULLARD | CR25 | 15 |
| R21 | 000101 | 100R 5% 1/3W CARBON | MULLARD | CR25 | - |
| R22 | 000103 | 10k 5% 1/3W CARBON | MULLARD | CR25 | - |
| R23 | 000103 | 10k 5% 1/3W CARBON | MULLARD | CR25 | - |

NOTES

SEE SHEET 1 FOR LATEST ISSUE

datron ELECTRONICS LTD

TITLE: 4700 PA PCB ASSY

DRAWING NUMBER: 400618 SHEET 2 OF 24

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No. USED Per Assy. |
|------------|-----------------|-----------------------|------------------------|-------------------------|--------------------|
| R24 | 070066 | 10k0 0.1% 5ppm W/W | MANN | MX125B | 3 |
| R25 | 080041 | 750R 0.1% 50ppm MF | VISHAY | VSRC1 | 1 |
| R26 | 070066 | 10k0 0.1% 5ppm WW | MANN | MX125B | - |
| R27 | 000103 | 10k 5% 1/3W CARBON | MULLARD | CR25 | - |
| R28 | 000103 | 10k 5% 1/3W CARBON | MULLARD | CR25 | - |
| R29 | 070066 | 10k0 0.1% 5ppm WW | MANN | MX125B | - |
| R30 | 070170 | 1k0 0.1% 5ppm WW | MANN | MX125B | 1 |
| R31 | 000103 | 10k 5% 1/3W CARBON | MULLARD | CR25 | - |
| R32 | 011542 | 15k4 1% 1/8W 50ppm MF | HOLCO | H8C | 1 |
| R33 | 013002 | 30k0 1% 1/8W 50ppm MF | HOLCO | H8C | 1 |
| R34 | 007100 | 10R 2% 2W MET-OX | ELECTROSIL | FP2 | - |
| R35 | 015620 | 562R 1% 1/8W 50ppm MF | HOLCO | H8C | - |
| R36 | 007393 | 39k 2% 2W MET-OX | ELECTROSIL | FP2 | - |
| R37 | 014990 | 499R 1% 1/8W 50ppm MF | HOLCO | H8C | 1 |
| R38 | 000123 | 12k 5% 1/3W CARBON | MULLARD | CR25 | - |
| R39 | 000103 | 10k 5% 1/3W CARBON | MULLARD | CR25 | - |
| R40 | 000104 | 100k 5% 1/3W CARBON | MULLARD | CR25 | 16 |
| R41 | | NOT USED | | | - |
| R42 | | NOT USED | | | - |
| R43 | | NOT USED | | | - |
| R44 | | NOT USED | | | - |
| R45 | | NOT USED | | | - |
| R46 | | NOT USED | | | - |

NOTES

SEE SHEET 2 FOR LATEST ISSUE

| | | | | | | | | | | | | | | | | | | | |
|------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ISS | | | | | | | | | | | | | | | | | | | |
| ECU | | | | | | | | | | | | | | | | | | | |
| DATE | | | | | | | | | | | | | | | | | | | |
| CHKD | | | | | | | | | | | | | | | | | | | |

| | | |
|----------------|--|------------------------|
| DATE | | datron ELECTRONICS LTD |
| DRAWN | | |
| CHECKED | | |
| APPROVED | | |
| DATE | | |
| TITLE | | 4700 PA PCB ASSY |
| DRAWING NUMBER | | 400618 |
| SHEET | | 3 |
| OF | | 24 |

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No. USED Per Assy. |
|------------|-----------------|-----------------------|------------------------|-------------------------|--------------------|
| R47 | 000473 | 47k 5% 1/3W CARBON | MULLARD | CR25 | 3 |
| R48 | 000473 | 47k 5% 1/3W CARBON | MULLARD | CR25 | - |
| R49 | 008051 | 43k 5% 3W W.W. | WELWYN | W23 | 1 |
| R50 | 000824 | 820k 5% 1/3W CARBON | MULLARD | CR25 | 2 |
| R51 | 006204 | 200k 2% 1W MET-OX | ELECTROSIL | FP1 | 1 |
| R52 | 011000 | 100R 1% 1/8W 50ppm MF | HOLCO | H8C | 1 |
| R53 | 016198 | 619R 1% 1/8W 50ppm MF | HOLCO | H8C | 1 |
| R54 | 000331 | 330R 5% 1/3W CARBON | MULLARD | CR25 | 1 |
| R55 | 000102 | 1k 5% 1/3W CARBON | MULLARD | CR25 | 6 |
| R56 | 012000 | 200R 1% 1/8W 50ppm MF | HOLCO | H8C | 1 |
| R57 | 000470 | 47R 5% 1/3W CARBON | MULLARD | CR25 | 3 |
| R58 | 015620 | 562R 1% 1/8W 50ppm MF | HOLCO | H8C | - |
| R59 | | NOT USED | | | - |
| R60 | 000473 | 47k 5% 1/3W CARBON | MULLARD | CR25 | - |
| R61 | 000824 | 820k 5% 1/3W CARBON | MULLARD | CR25 | - |
| R62 | | NOT USED | | | - |
| R63 | 011002 | 10k0 1% 1/8W 50ppm MF | HOLCO | H8C | 4 |
| R64 | 011002 | 10k0 1% 1/8W 50ppm MF | HOLCO | H8C | - |
| R65 | 008058 | 22k 5% 1/2W W.W. | WELWYN | W24 | 1 |
| R66 | 015111 | 5k11 1% 1/8W 50ppm MF | HOLCO | H8C | 1 |
| R67 | 011002 | 10k0 1% 1/8W 50ppm MF | HOLCO | H8C | - |
| R68 | 011002 | 10k0 1% 1/8W 50ppm MF | HOLCO | H8C | - |
| R69 | 000223 | 22k 5% 1/3W CARBON | MULLARD | CR25 | 1 |

NOTES

SEE SHEET 2 FOR LATEST ISSUE

| | | | | | | | | | | | | | | | | | | | |
|------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ISS | | | | | | | | | | | | | | | | | | | |
| ECU | | | | | | | | | | | | | | | | | | | |
| DATE | | | | | | | | | | | | | | | | | | | |
| CHKD | | | | | | | | | | | | | | | | | | | |

| | | |
|----------------|--|------------------------|
| DATE | | datron ELECTRONICS LTD |
| DRAWN | | |
| CHECKED | | |
| APPROVED | | |
| DATE | | |
| TITLE | | 4700 PA. PCB ASSY |
| DRAWING NUMBER | | 400618 |
| SHEET | | 4 |
| OF | | 24 |

| DESIGNATOR | DATRON PART No | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No | No. USED Per Assy |
|------------|----------------|--------------------------|------------------------|------------------------|-------------------|
| R70 | 000104 | 100k 5% 1/3W CARBON | MULLARD | CR25 | - |
| R71 | 011001 | 1k 1% 1/8W 50ppm MF | HOLCO | H8C | 2 |
| R72 | 015110 | 511R 1% 1/8W 50ppm MF | HOLCO | H8C | 2 |
| R73 | 000103 | 10k 5% 1/3W CARBON | MULLARD | CR25 | - |
| R74 | 011001 | 1k 1% 1/8W 50ppm MF | HOLCO | H8C | - |
| R75 | | NOT USED | | | - |
| R76 | 000103 | 10k 5% 1/3W CARBON | MULLARD | CR25 | - |
| R77 | 066502 | 5K POT 3/8sq VERT CERMET | BECKMAN | 72XW | 1 |
| R78 | 000621 | 620R 5% 1/3W CARBON | MULLARD | CR25 | 1 |
| R79 | 000104 | 100k 5% 1/3W CARBON | MULLARD | CR25 | - |
| R80 | 000105 | 1M 5% 1/3W CARBON | MULLARD | CR25 | 6 |
| R81 | 000222 | 2k2 5% 1/3W CARBON | MULLARD | CR25 | - |
| R82 | 000102 | 1k 5% 1/3W CARBON | MULLARD | CR25 | - |
| R83 | 000472 | 4k7 5% 1/3W CARBON | MULLARD | CR25 | 3 |
| R84 | 001182 | 1k8 5% 1/2W CARBON | MULLARD | CR37 | 3 |
| R85 | 000104 | 100k 5% 1/3W CARBON | MULLARD | CR25 | - |
| R86 | 000226 | 22M 5% 1/3W CARBON | MULLARD | CR25 | 2 |
| R87 | 000226 | 22M 5% 1/3W CARBON | MULLARD | CR25 | - |
| R88 | 005204 | 200k 2% 1/2W CARBON | ELECTROSIL | TR5 | 2 |
| R89 | 000100 | 10R 5% 1/3W CARBON | MULLARD | CR25 | 3 |
| R90 | 001182 | 1k8 5% 1/2W CARBON | MULLARD | CR37 | - |
| R91 | 000104 | 100k 5% 1/3W CARBON | MULLARD | CR25 | - |
| R92 | 000103 | 10k 5% 1/3W CARBON | MULLARD | CR25 | - |

NOTES

SEE SHEET 2 FOR LATEST ISSUE

| | | | | | | | | | | | | | | |
|------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ISS | | | | | | | | | | | | | | |
| ECO | | | | | | | | | | | | | | |
| DATE | | | | | | | | | | | | | | |
| CHKD | | | | | | | | | | | | | | |

| | | |
|----------|--|------------------------|
| DATE | | datron ELECTRONICS LTD |
| DRAWN | | |
| CHECKED | | |
| APPROVED | | |
| DATE | | |

FILE: 4700 PA PCB ASSY.

DRAWING NUMBER: 400618 5 SHEET OF 24

| DESIGNATOR | DATRON PART No | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No | No. USED Per Assy |
|------------|----------------|-----------------------|------------------------|------------------------|-------------------|
| R93 | 016190 | 619R 1% 1/8W 50ppm MF | HOLCO | H8C | 3 |
| R94 | 013320 | 332R 1% 1/8W 50ppm MF | HOLCO | H8C | 1 |
| R95 | 012800 | 280R 1% 1/8W 50ppm MF | HOLCO | H8C | 1 |
| R96 | 019090 | 909R 1% 1/8W 50ppm MF | HOLCO | H8C | 1 |
| R97 | 012211 | 2k21 1% 1/8W 50ppm MF | HOLCO | H8C | 1 |
| R98 | 014421 | 4k42 1% 1/8W 50ppm MF | HOLCO | H8C | 1 |
| R99 | 000104 | 100k 5% 1/3W CARBON | MULLARD | CR25 | - |
| R100 | 000105 | 1M 5% 1/3W CARBON | MULLARD | CR25 | - |
| R101 | 000474 | 470k 5% 1/3W CARBON | MULLARD | CR25 | 1 |
| R102 | 000104 | 100k 5% 1/3W CARBON | MULLARD | CR25 | - |
| R103 | 000104 | 100k 5% 1/3W CARBON | MULLARD | CR25 | - |
| R104 | 000102 | 1k 5% 1/3W CARBON | MULLARD | CR25 | - |
| R105 | 000103 | 10k 5% 1/3W CARBON | MULLARD | CR25 | - |
| R106 | 000103 | 10k 5% 1/3W CARBON | MULLARD | CR25 | - |
| R107 | 000103 | 10k 5% 1/3W CARBON | MULLARD | CR25 | - |
| R108 | 000472 | 4k7 5% 1/3W CARBON | MULLARD | CR25 | - |
| R109 | 000104 | 100k 5% 1/3W CARBON | MULLARD | CR25 | - |
| R110 | 000393 | 39k 5% 1/3W CARBON | MULLARD | CR25 | 1 |
| R111 | 000472 | 4k7 5% 1/3W CARBON | MULLARD | CR25 | - |
| R112 | 000104 | 100k 5% 1/3W CARBON | MULLARD | CR25 | - |
| R113 | 000103 | 10k 5% 1/3W CARBON | MULLARD | CR25 | - |
| R114 | 001278 | 2R7 5% 1/2W CARBON | MULLARD | CR37 | 1 |
| R115 | 011302 | 13k 1% 1/8W 50ppm MF | HOLCO | H8C | 2 |

NOTES

SEE SHEET 2 FOR LATEST ISSUE

| | | | | | | | | | | | | | | |
|------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ISS | | | | | | | | | | | | | | |
| ECO | | | | | | | | | | | | | | |
| DATE | | | | | | | | | | | | | | |
| CHKD | | | | | | | | | | | | | | |

| | | |
|----------|--|------------------------|
| DATE | | datron ELECTRONICS LTD |
| DRAWN | | |
| CHECKED | | |
| APPROVED | | |
| DATE | | |

FILE: 4700 PA PCB ASSY.

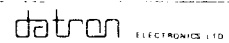
DRAWING NUMBER: 400618 6 SHEET OF 24

| DESIGNATOR | DATRON PART No | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No | No USED Per Assy |
|------------|----------------|-----------------------|------------------------|------------------------|------------------|
| R116 | 011101 | 1k1 1% 1/8W 50ppm MF | HOLCO | H8C | 2 |
| R117 | 011302 | 13k0 1% 1/8W 50ppm MF | HOLCO | H8C | - |
| R118 | 011101 | 1k1 1% 1/8W 50ppm MF | HOLCO | H8C | - |
| R119 | 000332 | 3k3 5% 1/3W CARBON | MULLARD | CR25 | 2 |
| R120 | 000153 | 15k 5% 1/3W CARBON | MULLARD | CR25 | 1 |
| R121 | 000104 | 100k 5% 1/3W CARBON | MULLARD | CR25 | - |
| R122 | 012002 | 20k0 1% 1/8W 50ppm MF | HOLCO | H8C | 1 |
| R123 | 012001 | 2k0 1% 1/8W 50ppm MF | HOLCO | H8C | 2 |
| R124 | 015110 | 511R 1% 1/8W 50ppm MF | HOLCO | H8C | - |
| R125 | 016190 | 619R 1% 1/8W 50ppm MF | HOLCO | H8C | - |
| R126 | 016190 | 619R 1% 1/8W 50ppm MF | HOLCO | H8C | - |
| R127 | 000104 | 100k 5% 1/3W CARBON | MULLARD | CR25 | - |
| R128 | 000104 | 100k 5% 1/3W CARBON | MULLARD | CR25 | - |
| R129 | 000102 | 1k 5% 1/3W CARBON | MULLARD | CR25 | - |
| R130 | 000270 | 27R 5% 1/3W CARBON | MULLARD | CR25 | 2 |
| R131 | 000220 | 22R 5% 1/3W CARBON | MULLARD | CR25 | 2 |
| R132 | 000470 | 47R 5% 1/3W CARBON | MULLARD | CR25 | - |
| R133 | 000271 | 270R 5% 1/3W CARBON | MULLARD | CR25 | 2 |
| R134 | 000271 | 270R 5% 1/3W CARBON | MULLARD | CR25 | - |
| R135 | 000470 | 47R 5% 1/3W CARBON | MULLARD | CR25 | - |
| R136 | 000220 | 22R 5% 1/3W CARBON | MULLARD | CR25 | - |
| R137 | 000270 | 27R 5% 1/3W CARBON | MULLARD | CR25 | - |
| R138 | 007184 | 180k 2% 2W MET-OX | ELECTROSIL | FP2 | 2 |

NOTES

SEE SHEET 2 FOR LATEST ISSUE

| | |
|------|--|
| ISS | |
| ECN | |
| DATE | |
| CHKD | |



 4700 PA. PCB ASSY
 DRAWING NUMBER 400618 7 of 24

| DESIGNATOR | DATRON PART No | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No | No USED Per Assy |
|------------|----------------|-----------------------|------------------------|------------------------|------------------|
| R139 | 000130 | 18R 5% 1/3W CARBON | MULLARD | CR25 | 2 |
| R140 | 000221 | 220R 5% 1/3W CARBON | MULLARD | CR25 | 2 |
| R141 | 000108 | 1R 5% 1/3W CARBON | MULLARD | CR25 | 2 |
| R142 | 000101 | 100R 5% 1/3W CARBON | MULLARD | CR25 | - |
| R143 | 000100 | 10R 5% 1/3W CARBON | MULLARD | CR25 | - |
| R144 | 000333 | 3R3 5% 1/3W CARBON | MULLARD | CR25 | 1 |
| R145 | 000100 | 10R 5% 1/3W CARBON | MULLARD | CR25 | - |
| R146 | 000101 | 100R 5% 1/3W CARBON | MULLARD | CR25 | - |
| R147 | 000108 | 1R 5% 1/3W CARBON | MULLARD | CR25 | - |
| R148 | 000221 | 220R 5% 1/3W CARBON | MULLARD | CR25 | - |
| R149 | 000130 | 18R 5% 1/3W CARBON | MULLARD | CR25 | - |
| R150 | 001132 | 1k8 5% 1/2W CARBON | MULLARD | CR37 | - |
| R151 | 008005 | 1R 5% 2 1/2W W.W. | WELWYN | W21 | 1 |
| R152 | 000183 | 18k 5% 1/3W CARBON | MULLARD | CR25 | 2 |
| R153 | 000561 | 560R 5% 1/3W CARBON | MULLARD | CR25 | 1 |
| R154 | 000183 | 18k 5% 1/3W CARBON | MULLARD | CR25 | - |
| R155 | 007184 | 180k 2% 2W MET-OX | ELECTROSIL | FP2 | - |
| R156 | 018250 | 825R 1% 1/3W 50ppm MF | HOLCO | H8C | 1 |
| R157 | 016811 | 6k81 1% 1/8W 50ppm MF | HOLCO | H8C | 2 |
| R158 | 000104 | 100k 5% 1/3W CARBON | MULLARD | CR25 | - |
| R159 | 012001 | 2k0 1% 1/8W 50ppm MF | HOLCO | H8C | - |
| R160 | 000332 | 3k3 5% 1/3W CARBON | MULLARD | CR25 | - |
| R161 | 016811 | 6k81 1% 1/8W 50ppm MF | HOLCO | H8C | - |

NOTES

SEE SHEET 2 FOR LATEST ISSUE

| | |
|------|--|
| ISS | |
| ECN | |
| DATE | |
| CHKD | |


 4700 PA. PCB ASSY
 DRAWING NUMBER 400618 8 of 24

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No. USED Per Assy. |
|------------|-----------------|------------------------------|------------------------|-------------------------|--------------------|
| C1 | 150023 | 33µF 20% 25V DIP TANT | UNION CARBIDE | K33E25 | 1 |
| C2 | 104018 | 1nF 20% 1KV CER DISC | ITT | HDI0K101NOMS-SSIK0DSC | 2 |
| C3 | 150006 | 4µF 20% 16V DIP TANT | UNION CARBIDE | K4R7E16 | 4 |
| C4 | 110042 | 100nF 20% 63V POLYESTER | WIMA | MKS2 | 6 |
| C5 | 150012 | 100nF 20% 35V DIP TANT | UNION CARBIDE | KR10E35 | 4 |
| C6 | 150012 | 100nF 20% 35V DIP TANT | UNION CARBIDE | KR10E35 | - |
| C7 | 104018 | 1nF 20% 1KV CER DISC | ITT | HDI0K101NOMS-SSIK0DSC | - |
| C8 | 104026 | 47nF $\pm 50\%$ 50V CER DISC | SIEMENS | B37449 | 13 |
| C9 | 104026 | 47nF $\pm 50\%$ 50V CER DISC | SIEMENS | B37449 | - |
| C10 | 150020 | 10µF 20% 25V DIP TANT | UNION CARBIDE | K10E25 | 5 |
| C11 | 150020 | 10µF 20% 25V DIP TANT | UNION CARBIDE | K10E25 | - |
| C12 | 104021 | 15pF 20% 1KV NPO CD | ITT | HDI0CG15POMS-SSIK0DSC | 1 |
| C13 | 104026 | 47nF $\pm 50\%$ 50V CER DISC | SIEMENS | B37449 | - |
| C14 | 104026 | 47nF $\pm 50\%$ 50V CER DISC | SIEMENS | B37449 | - |
| C15 | 110035 | 220nF 20% 63V POLYESTER | WIMA | MKS2 | 2 |
| C16 | 150012 | 100nF 20% 35V DIP TANT | UNION CARBIDE | KR10E35 | - |
| C17 | 102222 | 2n2F 10% 500V CER DISC | ITT | CD10 | 1 |
| C18 | 102100 | 10pF 5% 500V CER DISC | ITT | CD10 | 2 |
| C19 | 104026 | 47nF $\pm 50\%$ 50V CER DISC | SIEMENS | B37449 | - |
| C20 | 110015 | 15nF 20% 63V POLYESTER | WIMA | MKS2 | 3 |
| C21 | 104026 | 47nF $\pm 50\%$ 50V CER DISC | SIEMENS | B37449 | - |
| C22 | 110044 | 680nF 20% 630V POLYESTER | WIMA | MKS4 | 2 |
| C23 | 102221 | 220pF 10% 500V CER DISC | ITT | CD10 | 3 |

NOTES

SEE SHEET 2 FOR LATEST ISSUE

| | | | | | | | | | | | |
|--------|--|--|--|--|--|--|--|--|--|--|--|
| ISS | | | | | | | | | | | |
| E.C.O. | | | | | | | | | | | |
| DATE | | | | | | | | | | | |
| CHKD | | | | | | | | | | | |

| | | |
|----------|--|---|
| DATE | | datron ELECTRONICS LTD 4700 PA. PCB. ASSY. |
| DRAWN | | |
| CHECKED | | |
| APPROVED | | |
| DATE | | DRAWING NUMBER 400618 SHEET 11 OF 24 |

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No. USED Per Assy. |
|------------|-----------------|------------------------------|------------------------|-------------------------|--------------------|
| C24 | 102221 | 220pF 10% 500V CER DISC | ITT | CD10 | - |
| C25 | 110041 | 10nF 20% 100V POLYESTER | WIMA | FKS2 | 3 |
| C26 | 180041 | 100µF 40V AL ELECT | STEATITE | EKM 00FD 310G | 1 |
| C27 | 104026 | 47nF $\pm 50\%$ 50V CER DISC | SIEMENS | B37449 | - |
| C28 | 104026 | 47nF $\pm 50\%$ 50V CER DISC | SIEMENS | B37449 | - |
| C29 | 150006 | 4µF 20% 16V DIP TANT | UNION CARBIDE | K4R7E16 | - |
| C30 | 102471 | 470pF 10% 500V CER DISC | ITT | CD10 | 2 |
| C31 | 110044 | 680nF 20% 630V POLYESTER | WIMA | MKS4 | - |
| C32 | 104026 | 47nF $\pm 50\%$ 50V CER DISC | SIEMENS | B37449 | - |
| C33 | 100182 | 1n8F 2% 100V CER DISC | MULLARD | 2222 683 | 1 |
| C34 | 110015 | 15nF 20% 63V POLYESTER | WIMA | MKS2 | - |
| C35 | 110042 | 100nF 20% 63V POLYESTER | WIMA | MKS2 | - |
| C36 | 150020 | 10µF 20% 25V DIP TANT | UNION CARBIDE | K10E25 | - |
| C37 | 150020 | 10µF 20% 25V DIP TANT | UNION CARBIDE | K10E35 | - |
| C38 | 110035 | 220nF 20% 63V POLYESTER | WIMA | MKS2 | - |
| C39 | 150022 | 2µ2F 20% 35V DIP TANT | UNION CARBIDE | K2R2E35 | 5 |
| C40 | 102338 | 3p3F $\pm 5\%$ 500V CER DISC | ITT | CD08 | 1 |
| C41 | 150022 | 2µ2F 20% 35V DIP TANT | UNION CARBIDE | K2R2E35 | - |
| C42 | 104026 | 47nF $\pm 50\%$ 50V CER DISC | SIEMENS | B37449 | - |
| C43 | 104026 | 47nF $\pm 50\%$ 50V CER DISC | SIEMENS | B37449 | - |
| C44 | 110015 | 15nF 20% 63V POLYESTER | WIMA | MKS2 | - |
| C45 | 101103 | 10nF 25% 250V CER DISC | ITT | CD10 | 4 |
| C46 | 101103 | 10nF 25% 250V CER DISC | ITT | CD10 | - |

NOTES

SEE SHEET 2 FOR LATEST ISSUE

| | | | | | | | | | | |
|--------|--|--|--|--|--|--|--|--|--|--|
| ISS | | | | | | | | | | |
| E.C.O. | | | | | | | | | | |
| DATE | | | | | | | | | | |
| CHKD | | | | | | | | | | |

| | | |
|----------|--|---|
| DATE | | datron ELECTRONICS LTD 4700 PA. PCB. ASSY. |
| DRAWN | | |
| CHECKED | | |
| APPROVED | | |
| DATE | | DRAWING NUMBER 400618 SHEET 12 OF 24 |

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No. USED Per Assy |
|------------|-----------------|---------------------------|------------------------|-------------------------|-------------------|
| C47 | 110042 | 100nF 20% 63V POLYESTER | WIMA | MKS2 | - |
| C48 | 102221 | 220pF 10% 500V CER DISC | ITT | CD10 | - |
| C49 | 180051 | 22µF 20% 350V AL. ELECT | ECC | SMVB | 2 |
| C50 | 100101 | 100pF 2% 100V CER DISC | MULLARD | 2222 683 | 2 |
| C51 | 180045 | 47µF 63V AL. ELECT. | MULLARD | 031-38479 | 2 |
| C52 | 110042 | 100nF 20% 63V POLYESTER | WIMA | MKS2 | - |
| C53 | 100338 | 3p3F ±.25pF 100V CER DISC | MULLARD | 2222 683 | 1 |
| C54 | 180045 | 47µF 63V AL. ELECT. | MULLARD | 031-38479 | - |
| C55 | 102228 | 2p2F ±.5pF 500V CER DISC | ITT | CDO8 | 1 |
| C56 | 110042 | 100nF 20% 63V POLYESTER | WIMA | MKS2 | - |
| C57 | 100101 | 100pF 2% 100V CER DISC | MULLARD | 2222-683 | - |
| C58 | 100332 | 3n3F 2% 100V CER DISC | MULLARD | 2222-63019 | 1 |
| C59 | 180051 | 22µF 20% 350V AL. ELECT | ECC | SMVB | - |
| C60 | 104026 | 47nF ±20% 50V CER DISC | SIEMENS | B37449 | - |
| C61 | 150022 | 2µ2F 20% 35V DIP TANT | UNION CARBIDE | K2R2E35 | - |
| C62 | 150022 | 2µ2F 20% 35V DIP TANT | UNION CARBIDE | K2R2E35 | - |
| C63 | 101103 | 10nF 25% 250V CER DISC | ITT | CD10 | - |
| C64 | 101103 | 10nF 25% 250V CER DISC | ITT | CD10 | - |
| C65 | 110046 | 1µF 20% 50V POLYESTER | WIMA | MKS2 | 1 |
| C66 | 150012 | 100nF 20% 35V DIP TANT | UNION CARBIDE | KR10E35 | - |
| C67 | 100102 | 1nF 2% 100V CER DISC | MULLARD | 2222 63019 | 3 |
| C68 | 110026 | 6n8F 20% 100V POLYESTER | WIMA | FKS2 | 1 |
| C69 | 150008 | 470nF 20% 35V DIP TANT | UNION CARBIDE | KR47E35 | 1 |

| | | | | | | | | | | | | | |
|------------------------------|--|--|--|--|--|--|--|--|--|--------------------|----------------|------------------------|----------|
| NOTES | | | | | | | | | | DATE | | datron ELECTRONICS LTD | |
| SEE SHEET 2 FOR LATEST ISSUE | | | | | | | | | | DRAWN | | TITLE | |
| ISS | | | | | | | | | | 4700 PA. PCB. ASSY | | | |
| ECG | | | | | | | | | | | | | |
| DATE | | | | | | | | | | | | | |
| CHECK | | | | | | | | | | APPROVED | DRAWING NUMBER | | SHEET |
| | | | | | | | | | | | 400618 | | 13 of 24 |

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No. USED Per Assy |
|------------|-----------------|-------------------------|------------------------|-------------------------|-------------------|
| C70 | 150006 | 4µ7F 20% 16V DIPTANT | UNION CARBIDE | K4R7E16 | - |
| C71 | 110041 | 10nF 20% 100V POLYESTER | WIMA | FKS2 | - |
| C72 | 102100 | 10pF 5% 500V CER DISC | ITT | CD10 | - |
| C73 | 102102 | 1nF 10% 500V CER DISC | ITT | CD10 | 1 |
| C74 | 110042 | 100nF 20% 63V POLYESTER | WIMA | MKS2 | - |
| C75 | 150016 | 1µF 20% 35V DIP TANT | UNION CARBIDE | K10E35 | 6 |
| C76 | 150016 | 1µF 20% 35V DIP TANT | UNION CARBIDE | K10E35 | - |
| C77 | 150016 | 1µF 20% 35V DIP TANT | UNION CARBIDE | K10E35 | - |
| C78 | 150016 | 1µF 20% 35V DIP TANT | UNION CARBIDE | K10E35 | - |
| C79 | 150006 | 4µ7F 20% 16V DIP TANT | UNION CARBIDE | K4R7E16 | - |
| C80 | 150020 | 10µF 20% 25V DIP TANT | UNION CARBIDE | K10E25 | - |
| C81 | 110041 | 10nF 20% 100V POLYESTER | WIMA | FKS2 | - |
| C82 | | NOT USED | | | - |
| C83 | 100102 | 1nF 2% 100V CER DISC | MULLARD | 2222 63019 | - |
| C84 | 100102 | 1nF 2% 100V CER DISC | MULLARD | 2222 63019 | - |
| C85 | 104026 | 47nF ±20% 50V CER DISC | SIEMENS | B37449 | - |
| C86 | 110020 | 47nF 20% 63V POLYESTER | WIMA | MKS2 | 1 |
| C87 | 150022 | 2µ2F 20% 35V DIP TANT | UNION CARBIDE | K2R2E35 | - |
| C88 | 102471 | 470pF 5% 500V CER DISC | ITT | CD10 | - |
| C89 | 150016 | 1µF 20% 35V DIP TANT | UNION CARBIDE | K10E35 | - |
| C90 | 150016 | 1µF 20% 35V DIP TANT | UNION CARBIDE | K10E35 | - |

| | | | | | | | | | | | | | |
|------------------------------|--|--|--|--|--|--|--|--|--|------------------|----------------|------------------------|----------|
| NOTES | | | | | | | | | | DATE | | datron ELECTRONICS LTD | |
| SEE SHEET 2 FOR LATEST ISSUE | | | | | | | | | | DRAWN | | TITLE | |
| ISS | | | | | | | | | | 4700 PA PCB ASSY | | | |
| ECG | | | | | | | | | | | | | |
| DATE | | | | | | | | | | | | | |
| CHECK | | | | | | | | | | APPROVED | DRAWING NUMBER | | SHEET |
| | | | | | | | | | | | 400618 | | 14 of 24 |

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | Qty. USED Per Assy. |
|------------|-----------------|------------------------|------------------------|-------------------------|---------------------|
| D47 | 200008 | 200mA 125V LL Si DIODE | FAIRCHILD | IN458A | - |
| D48 | 200008 | 200mA 125V LL Si DIODE | FAIRCHILD | IN458A | - |
| D49 | 200008 | 200mA 125V LL Si DIODE | FAIRCHILD | IN458A | - |
| D50 | | NOT USED | | | - |
| D51 | 210300 | 30V 400mW ZENER | MULLARD | BZY88C30 | 1 |
| D52 | | NOT USED | | | - |
| D53 | | NOT USED | | | - |
| D54 | 210100 | 10V 400mW ZENER | MULLARD | BZY88C10 | - |
| D55 | | NOT USED | | | - |
| D56 | 200006 | 1A 600V GP Si DIODE | FAIRCHILD | IN4005 | - |
| D57 | 213005 | 75V 1/2W ZENER | MOTOROLA | BZX79C75 | 1 |
| D58 | 200001 | 75mA 75V GP Si DIODE | FAIRCHILD | IN4148 | - |
| D59 | 200001 | 75mA 75V GP Si DIODE | FAIRCHILD | IN4148 | - |
| D60 | 213019 | 200V 5% 1/2W ZENER | MULLARD | BZX79C200 | 2 |
| D61 | 213019 | 200V 5% 1/2W ZENER | MULLARD | BZX79C200 | - |
| D62 | 200008 | 200mA 125V LL Si DIODE | FAIRCHILD | IN458A | - |
| D63 | 200008 | 200mA 125V LL Si DIODE | FAIRCHILD | IN458A | - |
| D64 | 200008 | 200mA 125V LL Si DIODE | FAIRCHILD | IN458A | - |
| D65 | 200008 | 200mA 125V LL Si DIODE | FAIRCHILD | IN458A | - |
| D66 | 200008 | 200mA 125V LL Si DIODE | FAIRCHILD | IN458A | - |
| D67 | 200008 | 200mA 125V LL Si DIODE | FAIRCHILD | IN458A | - |
| D68 | 200008 | 200mA 125V LL Si DIODE | FAIRCHILD | IN458A | - |
| D69 | 200008 | 200mA 125V LL Si DIODE | FAIRCHILD | IN458A | - |

NOTES

SEE SHEET 2 FOR LATEST ISSUE

| | |
|------|--|
| ISS | |
| ECO | |
| DATE | |
| CHKD | |

| | | |
|----------|------------------------|----------|
| DATE | datron ELECTRONICS LTD | |
| DRAWN | FILE | |
| CHECKED | 4700 P.A. PCB. ASSY. | |
| APPROVED | DRAWING NUMBER | SHEET |
| DATE | 400618 | 17 OF 24 |

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | Qty. USED Per Assy. |
|------------|-----------------|----------------------|------------------------|-------------------------|---------------------|
| D70 | 220008 | L.E.D. RED. | PYE - TMC | 521-9165 | - |
| D71 | 200001 | 75mA 75V GP Si DIODE | FAIRCHILD | IN4148 | - |
| D72 | 200006 | 1A 600V GP Si DIODE | FAIRCHILD | IN4005 | - |
| D73 | 200006 | 1A 600V GP Si DIODE | FAIRCHILD | IN4005 | - |
| D74 | 200001 | 75mA 75V GP Si DIODE | FAIRCHILD | IN4005 | - |
| D75 | 210120 | 12V 400mW ZENER | MULLARD | BZY88C12 | 1 |
| D76 | 210033 | 3V3 400mW ZENER | MULLARD | BZY88C3V3 | 2 |
| D77 | 210033 | 3V3 400mW ZENER | MULLARD | BZY88C3V3 | - |
| D78 | | NOT USED | | | - |
| D79 | 200001 | 75mA 75V GP Si DIODE | FAIRCHILD | IN4148 | - |
| D80 | 200001 | 75mA 75V GP Si DIODE | FAIRCHILD | IN4148 | - |
| D81 | 200001 | 75mA 75V GP Si DIODE | FAIRCHILD | IN4148 | - |

NOTES

SEE SHEET 2 FOR LATEST ISSUE

| | |
|------|--|
| ISS | |
| ECO | |
| DATE | |
| CHKD | |

| | | |
|----------|------------------------|----------|
| DATE | datron ELECTRONICS LTD | |
| DRAWN | FILE | |
| CHECKED | 4700 P.A. PCB. ASSY. | |
| APPROVED | DRAWING NUMBER | SHEET |
| DATE | 400618 | 18 OF 24 |

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No. USED Per Assy |
|------------|-----------------|------------------------|------------------------|-------------------------|-------------------|
| Q1 | 240001 | Si NPN TRANSISTOR | NATIONAL | BC184/TO18 | 4 |
| Q2 | 230063 | N-CHAN TMOS JFET | MOTOROLA | MTP2N85 | 2 |
| Q3 | 250001 | Si PNP TRANSISTOR | NATIONAL | BC214/TO18 | 4 |
| Q4 | 230064 | P-CHAN TMOS JFET | MOTOROLA | MTP2P50 | 2 |
| Q5 | 250027 | Si PNP DUAL TRANSISTOR | MICRO POWER SYSTEMS | MP351 | 1 |
| Q6 | 230036 | N-CHAN JFET | SILICONIX | J108 | 4 |
| Q7 | | NOT USED | | | - |
| Q8 | 230064 | P-CHAN TMOS JFET | MOTOROLA | MTP2P50 | - |
| Q9 | 230073 | N-CHAN TMOS JFET | MOTOROLA | MTPIN100 | 1 |
| Q10 | 250001 | Si PNP TRANSISTOR | NATIONAL | BC214/TO18 | - |
| Q11 | 240001 | Si NPN TRANSISTOR | NATIONAL | BC184/TO18 | - |
| Q12 | 240001 | Si NPN TRANSISTOR | NATIONAL | BC184/TO18 | - |
| Q13 | 250001 | Si PNP TRANSISTOR | NATIONAL | BC214/TO18 | - |

NOTES:
SEE SHEET 2 FOR LATEST ISSUE

| | | | | | | | | | | | | | | | | | | | | |
|------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ISS | | | | | | | | | | | | | | | | | | | | |
| EC'D | | | | | | | | | | | | | | | | | | | | |
| DATE | | | | | | | | | | | | | | | | | | | | |
| CHKD | | | | | | | | | | | | | | | | | | | | |

| | | | |
|----------|--|------------------------|--------|
| DATE | | datron ELECTRONICS LTD | |
| DRAWN | | TITLE | |
| CHECKED | | 4700 P.A. PCB. ASSY. | |
| APPROVED | | DRAWING NUMBER | 400618 |
| DATE | | SHEET 19 OF 24 | |

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No. USED Per Assy |
|------------|-----------------|---------------------|------------------------|-------------------------|-------------------|
| Q14 | 230036 | N-CHAN JFET | SILICONIX | J108 | - |
| Q15 | 230036 | N-CHAN JFET | SILICONIX | J108 | - |
| Q16 | | NOT USED | | | - |
| Q17 | | NOT USED | | | - |
| Q18 | 230036 | N-CHAN JFET | SILICONIX | J108 | - |
| Q19 | 230003 | N-CHAN JFET | TELEDYNE | U1899JF | 6 |
| Q20 | 230063 | N-CHAN TMOS JFET | MOTOROLA | MTP2N85 | - |
| Q21 | 230001 | N-CHAN I LIM 1.4 mA | SILICONIX | J506 | 2 |
| Q22 | 240006 | Si NPN TRANSISTOR | NATIONAL | 2N3904/TO18 | 2 |
| Q23 | 250004 | Si PNP TRANSISTOR | NATIONAL | 2N3906/TO18 | 2 |
| Q24 | 230001 | N-CHAN I LIM 1.4 mA | SILICONIX | J506 | - |
| Q25 | 230003 | N-CHAN JFET | TELEDYNE | U1899JF | - |
| Q26 | 230003 | N-CHAN JFET | TELEDYNE | U1899JF | - |
| Q27 | 250009 | Si PNP TRANSISTOR | NATIONAL | 2N5401/TO18 | 2 |
| Q28 | 250004 | Si PNP TRANSISTOR | NATIONAL | 2N3906/TO18 | - |
| Q29 | 240009 | Si NPN TRANSISTOR | NATIONAL | MPSL01/2N5550 TO18 | 2 |
| Q30 | 240006 | Si NPN TRANSISTOR | NATIONAL | 2N3904/TO18 | - |
| Q31 | 250009 | Si PNP TRANSISTOR | NATIONAL | 2N5401/TO18 | - |
| Q32 | 240039 | Si NPN TRANSISTOR | MOTOROLA | BD419 | 1 |
| Q33 | 250028 | Si PNP TRANSISTOR | MOTOROLA | BD420 | 1 |
| Q34 | 240009 | Si NPN TRANSISTOR | NATIONAL | MPSL01/2N5550 TO18 | - |
| Q35 | 230003 | N-CHAN JFET | TELEDYNE | U1899JF | - |
| Q36 | 250001 | Si PNP TRANSISTOR | NATIONAL | BC214/TO18 | - |

NOTES:
SEE SHEET 2 FOR LATEST ISSUE

| | | | | | | | | | | | | | | | | | | | | |
|------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ISS | | | | | | | | | | | | | | | | | | | | |
| EC'D | | | | | | | | | | | | | | | | | | | | |
| DATE | | | | | | | | | | | | | | | | | | | | |
| CHKD | | | | | | | | | | | | | | | | | | | | |

| | | | |
|----------|--|------------------------|--------|
| DATE | | datron ELECTRONICS LTD | |
| DRAWN | | TITLE | |
| CHECKED | | 4700 P.A. PCB. ASSY. | |
| APPROVED | | DRAWING NUMBER | 400618 |
| DATE | | SHEET 20 OF 23 | |

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No. USED Per Assy |
|------------|-----------------|-------------------------|------------------------|-------------------------|-------------------|
| Q37 | | NOT USED | | | - |
| Q38 | | NOT USED | | | - |
| Q39 | 230019 | PMOS ENH FET | G.I. | MEM806 | 1 |
| Q40 | 230035 | NCHAN JFET | TELEDYNE | U1899JF | 1 |
| Q41 | 240001 | SI NPN TRANSISTOR | NATIONAL | BC184/TO18 | - |
| Q42 | 230003 | N-CHAN JFET | TELEDYNE | U1899JF | - |
| Q43 | 230003 | N-CHAN JFET | TELEDYNE | U1899JF | - |
| M1 | 290077 | 7X DARLINGTON DRIVER | SPRAGUE/EXAR | ULN2004A/XR2204CP | 1 |
| M2 | 260049 | 319 DUAL COMPARATOR | NATIONAL | LM319N | 1 |
| M3 | 260039 | 324 QUAD OP AMP | NATIONAL | LM324N | 1 |
| M4 | 280023 | QUAD 2 I/P NOR | MOTOROLA | MC14001UBCP | 1 |
| M5 | 280011 | DUAL D FLIP-FLOP | MOTOROLA | MC14013BCP | 1 |
| M6 | 280008 | QUAD 2 I/P NAND | MOTOROLA | MC14011BCP | 1 |
| M7 | 280090 | DUAL BINARY DECODER | MOTOROLA | MC14555BCP | 1 |
| M8 | 260074 | LH0032C FAST FET OP AMP | NATIONAL | LH0032 CG | 1 |
| M9 | 280045 | TRIPLE 3 I/P NOR | MOTOROLA | MC14025BCP | 1 |
| M10 | 260027 | 714 OP AMP | FAIRCHILD | JA 714 HC | 2 |
| M11 | 280009 | HEX INVERTER | MOTOROLA | MC14049UBCP | 1 |
| M12 | 280079 | QUAD 2 I/P OR | MOTOROLA | MC14071BCP | 1 |
| M13 | 290089 | 7X DARLINGTON DRIVER | SPRAGUE/EXAR | ULN2003A/XR2203CP | 1 |
| M14 | | NOT USED | | | - |
| M15 | 260046 | 2525 OP AMP | HARRIS | HA32525-5 | 2 |
| M16 | 220018 | HI-SPEED OPTO ISOLATOR | HP | 6N136 | 1 |

NOTES:

SEE SHEET 2 FOR LATEST ISSUE

| | | | | | | | | | | | | | |
|------|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ISS | | | | | | | | | | | | | |
| EC'D | | | | | | | | | | | | | |
| DATE | | | | | | | | | | | | | |
| BY | | | | | | | | | | | | | |

| | | | |
|----------|--|------------------------|----------|
| DATE | | datron ELECTRONICS LTD | |
| DRAWN | | TITLE | |
| CHECKED | | 4700 PA PCB ASSY | |
| APPROVED | | DRAWING NUMBER | 400618 |
| DATE | | SHEET | 21 OF 24 |

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No. USED Per Assy |
|------------|-----------------|----------------------|------------------------|-------------------------|-------------------|
| M17 | 260027 | 714 OP AMP | FAIRCHILD | JA714HC | - |
| M18 | 260042 | 5532 DUAL OP AMP | SIGNETICS | NESS32N | 1 |
| M19 | 260046 | 2525 OP AMP | HARRIS | HA32525-5 | - |
| M20 | 260028 | 1458 DUAL OP AMP | FAIRCHILD | JA1458CTC | 1 |
| M21 | 260079 | 12V REGULATOR | NATIONAL | LM78L12 | 1 |
| M22 | 260075 | 2903 DUAL COMPARATOR | NATIONAL | LM2903N | 2 |
| M23 | 260075 | 2903 DUAL COMPARATOR | NATIONAL | LM2903N | - |
| RL1 | 330029 | RELAY 2P2W | SDS | DS2E-DC24V | 8 |
| RL2 | 330029 | RELAY 2P2W | SDS | DS2E-DC24V | - |
| RL3 | 330029 | RELAY 2P2W | SDS | DS2E-DC24V | - |
| RL4 | 330029 | RELAY 2P2W | SDS | DS2E-DC24V | - |
| RL5 | 330029 | RELAY 2P2W | SDS | DS2E-DC24V | - |
| RL6 | 330029 | RELAY 2P2W | SDS | DS2E-DC24V | - |
| RL7 | 330029 | RELAY 2P2W | SDS | DS2E-DC24V | - |
| RL8 | 330029 | RELAY 2P2W | SDS | DS2E-DC24V | - |
| L1 | 370025 | 2μ2H 665mA CHOKE | SIGMA | SC30 | 2 |
| L2 | 370025 | 2μ2H 665mA CHOKE | SIGMA | SC30 | - |
| L3 | 370001 | 10μH 0.85Ω RF CHOKE | PLESSEY | 58/10/0011/10 | 3 |
| L4 | 370001 | 10μH 0.85Ω RF CHOKE | PLESSEY | 58/10/0011/10 | - |
| L5 | 370001 | 10μH 0.85Ω RF CHOKE | PLESSEY | 58/10/0011/10 | - |
| L6 | 370007-1 | 40mH CHOKE | SIGA | SEE DRG | 1 |
| L7 | 370012 | 470nH 0.1Ω RF CHOKE | SIGMA | SC10 | 2 |
| L8 | 370012 | 470nH 0.1Ω RF CHOKE | SIGMA | SC10 | - |

NOTES:

SEE SHEET 2 FOR LATEST ISSUE

| | | | | | | | | | | | | | |
|------|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ISS | | | | | | | | | | | | | |
| EC'D | | | | | | | | | | | | | |
| DATE | | | | | | | | | | | | | |
| BY | | | | | | | | | | | | | |

| | | | |
|----------|--|------------------------|----------|
| DATE | | datron ELECTRONICS LTD | |
| DRAWN | | TITLE | |
| CHECKED | | 4700 PA PCB ASSY | |
| APPROVED | | DRAWING NUMBER | 400618 |
| DATE | | SHEET | 22 OF 24 |

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | Qty. USED Per Assy |
|------------|-----------------|-----------------------------------|------------------------|-------------------------|--------------------|
| L9 | 370001 | 10 μ H 0.85 Ω RF CHOKE | PLESSEY | 58/10/0011/10 | - |
| L10 | 370001 | 10 μ H 0.85 Ω RF CHOKE | PLESSEY | 58/10/0011/10 | - |
| LPI | 920148 | NEON 200/250V T1/4 BI-PIN | RS | 586-431 | 2 |
| LP2 | 920148 | NEON 200/250V T1/4 BI-PIN | RS | 586-431 | - |
| | 410339-2 | PCB | | | 1 |
| | 540002 | 22SWG B.T.C. WIRE | | | A/R |
| | 540006 | 1/0.4 BLACK PTFE INSULATED WIRE | | | A/R |
| | 420112-1 | LABEL SSD WARNING- | SEE DRG- | | 1 |
| J1-J5 | 604033 | 4-WAY .1" PCB PLUG GD.PL. | MOLEX | 22-29-2041 | 10 |
| | 605059 | 8-WAY DIL SOCKET | JERMYN | J23-18008 | 7 |
| | 605060 | 14-WAY DIL SOCKET | JERMYN | J23-18014 | 7 |
| | 605061 | 16-WAY DIL SOCKET | JERMYN | J23-18016 | 4 |
| | 611006 | M3x10mm POZI-PAN STEEL | ZN.PL. | | 2 |
| | 611016 | M3x8mm POZI-PAN STEEL | ZN.PL. | | 2 |
| | 613005 | M3 INT. SHAKEPROOF | ZN.PL. | | 3 |
| | 613007 | M3 WASHER STEEL | ZN.PL. | | 1 |
| | 615002 | M3 FULL NUT STEEL | ZN.PL. | | 4 |
| | 618001 | INSULATING BUSH TO-220 | MULLARD | 56359C | 1 |
| | 613029 | M3 WAVY WASHER | | | 1 |
| | 620007 | TEST POINT TERMINAL | MICROVAR | TYPE C30 | 29 |

NOTES

SEE SHEET 2 FOR LATEST ISSUE

| | | | | | | | | | | | | | | | | | | | | |
|--------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ISS | | | | | | | | | | | | | | | | | | | | |
| ECN | | | | | | | | | | | | | | | | | | | | |
| DATE | | | | | | | | | | | | | | | | | | | | |
| APPROV | | | | | | | | | | | | | | | | | | | | |

| | | |
|----------|--|---|
| DATE | | datron ELECTRONICS LTD TITLE 4700 PA. PCB ASSY DRAWING NUMBER 400618 SHEET 23 OF 24 |
| DRAWN | | |
| CHECKED | | |
| APPROVED | | |
| DATE | | |


| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | Qty. USED Per Assy |
|------------|-----------------|--------------------------------|------------------------|-------------------------|--------------------|
| | 630024 | STEATITE BEAD 16SWG | PARK ROYAL PORCELAIN | Nº2 | 52 |
| | 630123 | PCB EJECTOR - VIOLET | RICHCO | CBE | 2 |
| S1 | 700081 | SWITCH IP 2POS* SLIDE | ALCO | SLS-121-PC | 1 |
| | 920091-1 | HEATSINK TO220 | SEE DRG | | 1 |
| | 920151 | HEATSINK TO202 SLIP CLIP | THERMALLOY | 6046 PB | 2 |
| | 920152 | HEATSINK TO220 | AAVID | 5425B-TT | 1 |
| | 920153 | HEATSINK TO220 | ASSMANN | V4330 | 1 |
| | 630036 | STEATITE BEAD 18SWG | PARK ROYAL PORCELAIN | Nº1 | 6 |
| | 630243 | GLASS BEAD 2.40D x 0.81D x 0.8 | MANSOL (PREFORMS) LTD | M5363B/3 | 26 |
| | 620003 | SOLDER PIN | HARWIN | H2105A01 | 3 |
| | 618004 | TO18 MOUNTING PAD | JERMYN | TO18-008D | 4 |
| | 618010 | SIL PAD TO220 | | | 1 |
| | 605124 | 10 WAY SOCKET STRIP | AUGAT | S10-AG91D | 1.33 |
| | 920149 | HEATSINK TO8 | SOURIAU | TXBF 2-050-033 B | 1 |
| | 604046 | 3WAY .1" PCB PLUG GD.PL | MOLEX | 22-10-2031 | 1 |
| | 605127 | 2WAY .1" SHORTING LINK | ASSMANN | AKS PL-G | 1 |
| | 590031 | HEATSHRINK Ø3.2 | RS | | 15mm |
| | 590004 | SLEEVE Ø1.0 PTFE | HELLERMANN | FE10 | A/R |
| | 590074 | SOLDER SLEEVE Ø3.0 | RAYFAST | CWT-3 | 1 |
| | 420098 | LABEL SERIAL N° | | | 1 |
| | 512999 | 7/2 PTFE WHITE WIRE | | | 40mm |
| | 560002 | 7/34 AWG CO-AX | | | 330mm |
| F1 | 920191 | THERMAL FUSE 147°C | UMI | X150 | 1 |

NOTES

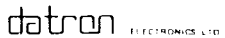
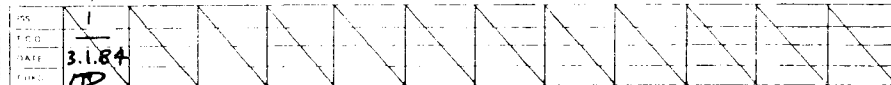
SEE SHEET 2 FOR LATEST ISSUE

| | | | | | | | | | | | | | | | | | | | | |
|--------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ISS | | | | | | | | | | | | | | | | | | | | |
| ECN | | | | | | | | | | | | | | | | | | | | |
| DATE | | | | | | | | | | | | | | | | | | | | |
| APPROV | | | | | | | | | | | | | | | | | | | | |

| | | |
|----------|--|---|
| DATE | | datron ELECTRONICS LTD TITLE 4700 PA. PCB ASSY DRAWING NUMBER 400618 SHEET 24 OF 24 |
| DRAWN | | |
| CHECKED | | |
| APPROVED | | |
| DATE | | |

| DRAWING No. | | CHK'D | DATE | ISSUE | REVISION | ISSUE | SHEET NUMBER |
|---|-----------|-------------------|-----------------|------------------|--------------------|-------|-----------------------|
| 400561 | | | | | | | |
| DESCRIPTION | | DRAWING NUMBER | SHEET NUMBER | ISSUE - REVISION | | | |
| COMP LAYOUT | 480561 | 1 | 2.0 | 2.1 | 2.2 | | |
| SCHEMATIC | 430561 | 1 | 2.0 | | | | |
| FUNCTIONAL TEST PROC. | 460561/FT | 1-3 | 2.0 | 2.1 | | | |
| FUNCT. TEST TICK LIST | 470561/FT | 1 | 2.0 | 2.1 | | | |
| NOTES | | | | | | | |
|  | | DRN B. JACKSON | CHK'D MSD | APP'D MSD | TITLE 4200 | | DRAWING No. 400561 |
| NORWICH ENGLAND | | DATE 4-7-85 | DATE 10.7.85 | DATE 23.7.85 | OUT GUARD PSU ASSY | | SHEET 1 OF 5 |

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No. USED Per Assy |
|------------|-----------------|----------------------------|------------------------|-------------------------|-------------------|
| R1 | 008024 | OR27 10% 1/2W WIREWOUND | WELWYN | W21 | 1 |
| R2 | 000330 | 33R 5% 1/3W CARBON | MULLARD | CR25 | 1 |
| R3 | 000102 | 1k 5% 1/3W CARBON | MULLARD | CR25 | 3 |
| R4 | 000182 | 1k 5% 1/3W CARBON | MULLARD | CR25 | 1 |
| R5 | 013922 | 39k2 1% 1/8W 50ppm MF | HOLCO | H8C | 1 |
| R6 | 013742 | 37k4 1% 1/8W 50ppm MF | HOLCO | H8C | 1 |
| R7 | 090001 | PTC THERMISTOR | MULLARD | VAR650 | 1 |
| R8 | 000470 | 47R 5% 1/3W CARBON | MULLARD | CR25 | 2 |
| R9 | 000470 | 47R 5% 1/3W CARBON | MULLARD | CR25 | - |
| R10 | 011003 | 100k 1% 1/8W 50ppm MF | HOLCO | H8C | 2 |
| R11 | 011003 | 100k 1% 1/8W 50ppm MF | HOLCO | H8C | - |
| R12 | 066205 | 2M POT 3/8 SQ VERT. CERMET | BECKMAN | 72XW | 1 |
| R13 | 008069 | 180k 5% 1/2W CARBON | AB | EB | 1 |
| R14 | 000102 | 1k 5% 1/3W CARBON | MULLARD | CR25 | - |
| R15 | 000102 | 1k 5% 1/3W CARBON | MULLARD | CR25 | - |
| R16 | 000221 | 220R 5% 1/3W CARBON | MULLARD | CR25 | 2 |
| R17 | 008022 | OR27 10% 1/2W MF | ITT | RN05 | 2 |
| R18 | 008022 | OR27 10% 1/2W MF | ITT | RN05 | - |
| R19 | 000104 | 100k 5% 1/3W CARBON | MULLARD | CR25 | 1 |
| R20 | 000221 | 220R 5% 1/3W CARBON | MULLARD | CR25 | - |

| | | | | |
|--|--|-----------------------------|---|--|
| NOTES | | DATE 29.2.84 |  | |
| SEE SHEET 1 FOR LATEST ISSUE | | DRAWN | TITLE 4200 P5 (0G) PCB ASSY | |
|  | | CHECKED | DRAWING NUMBER 400561 | |
| DATE 3.1.84 | | APPROVED <i>J. Stone</i> | SHEET 2 OF 5 | |
| DATE 10 | | DATE 6.3.89 | | |

| DESIGNATOR | DATRON PART No | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No. USED Per Assy. |
|------------|----------------|------------------------------|------------------------|-------------------------|--------------------|
| C1 | | NOT USED | | | - |
| C2 | 150006 | 4 μ F 20% 16V DIP TANT | UNION CARBIDE | K4R7E16 | 1 |
| C3 | | NOT USED | | | - |
| C4 | 150017 | 100 μ F 20% 16V DIP TANT | UNION CARBIDE | K100E16 | 1 |
| C5 | 180004 | 4700 μ F 16V AL. ELECT | WIMA | PRINTILYT 1 | 1 |
| C6 | 101103 | 10nF 25% 250V CER DISC | ITT | CD10 | 1 |
| C7 | 180026 | 10 μ F 350V AL. ELECT | ITT | EN12.12 10/350 | 1 |
| C8 | 104030 | 100pF 10% 4kV CER DISC | ITT | HD16 | 1 |
| C9 | 102222 | 2n2F 20% 500V CER DISC | ITT | CD10 | 1 |
| C10 | 110005 | 10nF 20% 250V POLYESTER | MULLARD | C280AE P10K | 1 |
| D1 | 200022 | 3A 400V GP Si DIODE | MOTOROLA | BY252 | 2 |
| D2 | 200022 | 3A 400V GP Si DIODE | MOTOROLA | BY252 | - |
| D3 | 210027 | 2V7 400mW ZENER | MULLARD | BZY88C2V7 | 1 |
| D4 | 214012 | 2V45 30ppm ZENER | FERRANTI | ZN458 | 1 |
| D5 | 213006 | 5V 5W ZENER | UNITRODE | TV5505 | 1 |
| D6 | 210068 | 6V8 400mW ZENER | MULLARD | BZY88C6V8 | 1 |
| D7 | 213004 | 180V 1/2 W ZENER | MOTOROLA | IN5279B | 1 |

NOTES

SEE SHEET 2 FOR LATEST ISSUE

| | | | | | | | | | | | | |
|------|--|--|--|--|--|--|--|--|--|--|--|--|
| ISS | | | | | | | | | | | | |
| ECCO | | | | | | | | | | | | |
| DATE | | | | | | | | | | | | |
| CHKD | | | | | | | | | | | | |

| | | |
|-----------------|-------------------------------|--------------------|
| DATE 29.2.84 | datron ELECTRONICS LTD | |
| DRAWN J.L. | TITLE 4200 PS(OG) PCB ASSY | |
| CHECKED | APPROVED | |
| DATE | DRAWING NUMBER 400561 | SHEET OF 3 OF 5 |

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No. USED Per Assy. |
|------------|-----------------|--------------------------|------------------------|-------------------------|--------------------|
| W1 | 209013 | 1A5 600V BRIDGE RECT | MICRO-ELECTRONICS | W006 | 1 |
| Q1 | 250011 | Si PNP TRANSISTOR | NATIONAL | BC327/TO18 | 1 |
| Q2 | 240024 | Si NPN TRANSISTOR | NATIONAL | TIP31A | 1 |
| Q3 | 240018 | Si NPN TRANSISTOR | MOTOROLA | MJE340 | 2 |
| Q4 | 240018 | Si NPN TRANSISTOR | MOTOROLA | MJE340 | - |
| Q5 | 250016 | Si PNP TRANSISTOR | MOTOROLA | MJ2955 | 2 |
| Q6 | 250016 | Si PNP TRANSISTOR | MOTOROLA | MJ2955 | - |
| M1 | 260061 | 3140 OP AMP | RCA | CA3140E | 1 |
| | 410179-G | PCB | | | 1 |
| | 604042 | 4WAY WAFER PIN .156" | MOLEX | 09-72-2041 | 2 |
| | 605059 | 8WAY DIL SOCKET | JERMYN | J23-18008 | 1 |
| | 611006 | M3X10mm POZIPAN STEEL | ZN PL | | 6 |
| | 611004 | M3X6mm POZIPAN STEEL | ZN PL | | 1 |
| | 613005 | M3 INT. SHAKEPROOF | ZN PL | | 7 |
| | 613007 | M3 WASHER STEEL | ZN PL | | 6 |
| | 615002 | M3 FULL NUT STEEL | ZN PL | | 7 |
| | 618004 | MOUNTING PAD TO18 | JERMYN | TO18-008D | 1 |
| | 620007 | TEST POINT TERMINAL | MICROVAR | TYPE C30 | 9 |
| | 630024 | STEATITE BEAD 16 SWG | PARK ROYAL PORCELAIN | No 2 (LARGE) | 6 |
| | 900003 | HEATSINK COMPOUND | RS | 554-311 | A/R |
| | 900004 | SILICONE RUBBER COMPOUND | RS | 555-588 | A/R |

NOTES



SEE SHEET 2 FOR LATEST ISSUE

| | | | | | | | | | | | | |
|------|--|--|--|--|--|--|--|--|--|--|--|--|
| ISS | | | | | | | | | | | | |
| ECCO | | | | | | | | | | | | |
| DATE | | | | | | | | | | | | |
| CHKD | | | | | | | | | | | | |

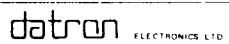



| | | |
|-----------------|--------------------------------|--------------------|
| DATE 29.2.84 | datron ELECTRONICS LTD | |
| DRAWN J.L. | TITLE 4200 PS (OG) PCB ASSY | |
| CHECKED | APPROVED | |
| DATE | DRAWING NUMBER 400561 | SHEET OF 4 OF 5 |

| DRAWING No | DATE | ISSUE | REVISION | ISSUE |
|------------|--------------|-------|----------|-------|
| 400554 | 4-7-85 | 4-0 | | |
| | 1981 11.9.85 | 4-1 | | |
| | 21.3.95 | 4-2 | | |
| | 23.8.96 | 4-2 | | |
| | 16.5.88 | 4-2 | | |
| | 14.2.89 | 4-3 | | |

| DESCRIPTION | DRAWING NUMBER | SHEET NUMBER | ISSUE | REVISION |
|------------------------|----------------|--------------|-------|----------|
| COMP LAYOUT | 480554 | 1 | 4-0 | 4-1 |
| | | | 4-1 | 4-2 |
| SCHEMATIC | 430554 | 1 | 4-0 | 4-1 |
| SCHEMATIC | 430554 | 2 | 4-0 | 4-2 |
| FUNCTIONAL TEST. PROC. | 460554/FT | 1-2 | 4-0 | 4-1 |
| FUNCT. TEST TICK LIST | 470554/FT | 1 | 4-0 | 4-1 |

| | | | | | | | |
|-------|---|--|-------------------------------------|------------------------------------|--|--|--------------------------------------|
| NOTES |  | | DRN B. JACKSON DATE 4-7-85 | DESIGNED MSD DATE 10.7.85 | APPROVED  DATE 23.7.85 | TITLE 4200 PART No. PS(IG) PCB ASSY | DRAWING No 400554 SHEET 1 OF 7 |
|-------|---|--|-------------------------------------|------------------------------------|--|--|--------------------------------------|

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | Qty USED Per Assy |
|------------|-----------------|------------------------|------------------------|-------------------------|-------------------|
| R1 | 000102 | 1k 5% 1/3W CARBON | MULLARD | CR25 | 1 |
| R2 | 015230 | 523R 1% 1/8W 50ppm MF | HOLCO | H8C | 1 |
| R3 | 021402 | 14k 1% 1/4W 50ppm MF | HOLCO | H4C | 1 |
| R4 | | NOT USED | | | - |
| R5 | | NOT USED | | | - |
| R6 | | NOT USED | | | - |
| R7 | 000272 | 2k7 5% 1/3W CARBON | MULLARD | CR25 | 2 |
| R8 | 000272 | 2k7 5% 1/3W CARBON | MULLARD | CR25 | - |
| R9 | 000103 | 10k 5% 1/3W CARBON | MULLARD | CR25 | 2 |
| R10 | 000103 | 10k 5% 1/3W CARBON | MULLARD | CR25 | - |
| C1 | 180042 | 3300µF 25V AL ELECT | STEATITE | EG. OOMG. 433E | 2 |
| C2 | 180042 | 3300µF 25V AL ELECT | STEATITE | EG. OOMG. 433E | - |
| C3 | 180047 | 1000µF 40V AL ELECT | ECC | SMVB | 7 |
| C4 | 180047 | 1000µF 40V AL ELECT | ECC | SMVB | - |
| C5 | 110020 | 47nF 20% 63V POLYESTER | WIMA | MKS2 | 1 |
| C6 | 150021 | 22µF 20% 25V DIP TANT | UNION CARBIDE | K22E25 | 7 |
| C7 | 150021 | 22µF 20% 25V DIP TANT | UNION CARBIDE | K22E25 | - |
| C8 | 180047 | 1000µF 40V AL ELECT | ECC | SMVB | - |
| C9 | 180047 | 1000µF 40V AL ELECT | ECC | SMVB | - |
| C10 | 180048 | 470µF 63V AL ELECT | ECC | SMVB | 2 |

| | | | | |
|--------|---|---|---|---|
| NOTES | SEE SHEET 1 FOR LATEST ISSUE | | DATE 29.2.84 |  |
| ISS | 2 | 3 | 4 | DRAWN CHECKED APPROVED DATE 6.3.84 |
| E.C.O. | 1576 | 1647 | 1743 | |
| DATE | 7.2.84 | 11.6.84 | 24.10.84 | |
| BY |  |  |  | |
| | | | | TITLE 4200 PS(IG) PCB ASSY |
| | | | | DRAWING NUMBER 400554 |
| | | | | SHEET 2 OF 7 |

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No. USED Per Assy. |
|------------|-----------------|-----------------------------|------------------------|-------------------------|--------------------|
| C11 | 150021 | 22 μ F 20% 25V DIP TANT | UNION CARBIDE | K22E25 | - |
| C12 | 104026 | 47nF 50% 50V CER DISC | SIEMENS | B37449 | 3 |
| C13 | 150021 | 22 μ F 20% 25V DIP TANT | UNION CARBIDE | K22E25 | - |
| C14 | 180024 | 10 μ F 63V AL ELECT | MULLARD | O16-18109 | 1 |
| C15 | 150021 | 22 μ F 20% 25V DIP TANT | UNION CARBIDE | K22E25 | - |
| C16 | 150021 | 22 μ F 20% 25V DIP TANT | UNION CARBIDE | K22E25 | - |
| C17 | 104026 | 47nF 50% 50V CER DISC | SIEMENS | B37449 | - |
| C18 | 150001 | 22 μ F 20% 16V DIP TANT | UNION CARBIDE | K22E1G | 2 |
| C19 | 150001 | 22 μ F 20% 16V DIP TANT | UNION CARBIDE | K22E1G | - |
| C20 | 104026 | 47nF 50% 50V CER DISC | SIEMENS | B37449 | - |
| C21 | 180048 | 470 μ F 63V AL ELECT | ECC | SMVB | - |
| C22 | 180047 | 1000 μ F 40V AL ELECT | ECC | SMVB | - |
| C23 | 180047 | 1000 μ F 40V AL ELECT | ECC | SMVB | - |
| C24 | 180047 | 1000 μ F 40V AL ELECT | ECC | SMVB | - |
| C25 | 150016 | 1 μ F 20% 35V DIP TANT | UNION CARBIDE | K1R0E35 | 2 |
| C26 | 150016 | 1 μ F 20% 35V DIP TANT | UNION CARBIDE | K1R0E35 | - |
| C27 | 150021 | 22 μ F 20% 25V DIP TANT | UNION CARBIDE | K22E25 | - |
| D1 | 200022 | 3A 400V GP SI DIODE | MOTOROLA | BY252 | 4 |
| D2 | 200022 | 3A 400V GP SI DIODE | MOTOROLA | BY252 | - |
| D3 | 200022 | 3A 400V GP SI DIODE | MOTOROLA | BY252 | - |

NOTES

SEE SHEET 2 FOR LATEST ISSUE

| | | | | | | | | | | | | | | | | | | | | |
|------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| DES | | | | | | | | | | | | | | | | | | | | |
| ECN | | | | | | | | | | | | | | | | | | | | |
| DATE | | | | | | | | | | | | | | | | | | | | |
| CHKD | | | | | | | | | | | | | | | | | | | | |

| | | |
|-----------------|--------------------------------|--|
| DATE 29.2.84 | datron ELECTRONICS LTD | |
| DRAWN 11 | TITLE 4200 PS (IG) PCB ASSY | |
| CHECKED | DRAWING NUMBER 400554 | |
| APPROVED | SHEET OF 3 OF 7 | |
| DATE | | |

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No. USED Per Assy. |
|------------|-----------------|----------------------|------------------------|-------------------------|--------------------|
| D4 | 200022 | 3A 400V GP SI DIODE | MOTOROLA | BY252 | - |
| D5 | 200002 | 1A 50V GP SI DIODE | FAIRCHILD | IN4001 | 4 |
| D6 | 200002 | 1A 50V GP SI DIODE | FAIRCHILD | IN4001 | - |
| D7 | 200002 | 1A 50V GP SI DIODE | FAIRCHILD | IN4001 | - |
| D8 | 200002 | 1A 50V GP SI DIODE | FAIRCHILD | IN4001 | - |
| D9 | 210200 | 20V 400mW ZENER | MULLARD | BZY88C20 | 2 |
| D10 | 210200 | 20V 400mW ZENER | MULLARD | BZY88C20 | - |
| D11 | 210033 | 3V3 400mW ZENER | MULLARD | BZY88C3V3 | 1 |
| W1 | 209003 | 1A5 100V BRIDGE RECT | MICRO-ELECTRONICS | W001 | 4 |
| W2 | 209003 | 1A5 100V BRIDGE RECT | MICRO-ELECTRONICS | W001 | - |
| W3 | 209003 | 1A5 100V BRIDGE RECT | MICRO-ELECTRONICS | W001 | - |
| W4 | 209003 | 1A5 100V BRIDGE RECT | MICRO-ELECTRONICS | W001 | - |
| Q1 | 240037 | Si NPN TRANSISTOR | MOTOROLA | TIPI41 | 1 |
| Q2 | 250026 | Si PNP TRANSISTOR | MOTOROLA | TIPI46 | 1 |
| Q3 | 230065 | J FET 1 LIM 4.7mA | SILICONIX | J511 | 2 |
| Q4 | 230065 | J FET 1 LIM 4.7mA | SILICONIX | J511 | - |
| M1 | 260051 | -15V 1A REGULATOR | MOTOROLA | MC7915CT | 2 |
| M2 | 260006 | 15V 1A REGULATOR | MOTOROLA | MC7815CT | 2 |

NOTES

SEE SHEET 2 FOR LATEST ISSUE

| | | | | | | | | | | | | | | | | | | | | |
|------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| DES | | | | | | | | | | | | | | | | | | | | |
| ECN | | | | | | | | | | | | | | | | | | | | |
| DATE | | | | | | | | | | | | | | | | | | | | |
| CHKD | | | | | | | | | | | | | | | | | | | | |

| | | |
|-----------------|--------------------------------|--|
| DATE 29.2.84 | datron ELECTRONICS LTD | |
| DRAWN 11 | TITLE 4200 PS (IG) PCB ASSY | |
| CHECKED | DRAWING NUMBER 400554 | |
| APPROVED | SHEET OF 4 OF 7 | |
| DATE | | |

| DESIGNATOR | DATRON PART No | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No | No. USED Per Assy |
|------------|----------------|-------------------------|------------------------|------------------------|-------------------|
| M3 | 260070 | 317 ADJ. REGULATOR | NATIONAL | LM317 HVK | 1 |
| M4 | 260006 | 15V 1A REGULATOR | MOTOROLA | MC7815CT | - |
| M5 | | NOT USED | | | - |
| M6 | 260005 | 5V 1A REGULATOR | MOTOROLA | MC7805CT | 1 |
| M7 | 260051 | -15V 1A REGULATOR | MOTOROLA | MC7915CT | - |
| M8 | 260072 | -8V 1A REGULATOR | NATIONAL | LM7809CT | 1 |
| M9 | 260071 | 8V 1A REGULATOR | NATIONAL | LM7808CT | 1 |
| | | | | | |
| L1 | | NOT USED | | | |
| L2 | 370013 | 4 μ H 6A RF CHOKE | ERO | F1756-004-601 | 2 |
| L3 | 370013 | 4 μ H 6A RF CHOKE | ERO | F1756-004-601 | - |
| L4 | 370014 | 8 μ H 3A RF CHOKE | ERO | F1756-008-301 | 4 |
| L5 | 370014 | 8 μ H 3A RF CHOKE | ERO | F1756-008-301 | - |
| L6 | | NOT USED | | | |
| L7 | 370014 | 8 μ H 3A RF CHOKE | ERO | F1756-008-301 | - |
| L8 | | NOT USED | | | |
| L9 | 370014 | 8 μ H 3A RF CHOKE | ERO | F1756-008-301 | - |
| L10 | 370019 | PS COMMON MODE CHOKE | SIGA | SEE DRG | 1 |
| | | | | | |
| F1 | 920128 | FUSE 4A 250V 20mm SLO-B | BELLING LEE | L2080A/4 | 2 |
| F2 | 920128 | FUSE 4A 250V 20mm SLO-B | BELLING LEE | L2080A/4 | - |

NOTES

SEE SHEET 2 FOR LATEST ISSUE

| | | | | | | | | | | | | | | | | | | | |
|------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ISS | | | | | | | | | | | | | | | | | | | |
| ECO | | | | | | | | | | | | | | | | | | | |
| DATE | | | | | | | | | | | | | | | | | | | |
| CHKD | | | | | | | | | | | | | | | | | | | |

| | | |
|----------|-----------------------|---------------------------|
| DATE | 29.2.84 | datron ELECTRONICS LTD |
| TITLE | 4200 PS (IG) PCB ASSY | |
| DRAWN | IL | DRAWING NUMBER 400554 |
| CHECKED | | |
| APPROVED | | SHEET 5 OF 7 |
| DATE | | |


| DESIGNATOR | DATRON PART No | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No | No. USED Per Assy |
|------------|----------------|------------------------------|------------------------|------------------------|-------------------|
| F3 | 920143 | FUSE 3.15A 250V 20mm SLO-B | BELLING LEE | L2080A/3-15 | 2 |
| F4 | 920143 | FUSE 3.15A 250V 20mm SLO-B | BELLING LEE | L2080A/3-15 | - |
| F5 | 920116 | FUSE 1A 250V 20mm SLO-B | BELLING LEE | L2080A/1 | 2 |
| F6 | 920116 | FUSE 1A 250V 20mm SLO-B | BELLING LEE | L2080A/1 | - |
| | 540002 | 22 SWG TINNED COPPER WIRE | | | A/R |
| | 410282-2 | PCB | | | 1 |
| | 590004 | SLEEVE - PTFE | HELLERMANN ELECTRIC | FE10 | A/R |
| | 604042 | 4WAY .156" PLUG GD. PL. | MOLEX | 09-72-2041 | 5 |
| | 611006 | M3x10mm POZIPAN STEEL | ZN PL | | 10 |
| | 630243 | GLASS BEAD 2.4% x 0.8% x 1.8 | MANSOL (PREFORMS) | M5363B/3 | 6 |
| | 613005 | M3 INT SHAKEPROOF | ZN PL | | 10 |
| | 613007 | M3 WASHER STEEL | ZN PL | | 3 |
| | 615002 | M3 FULL NUT STEEL | ZN PL | | 10 |
| | 618010 | INSULATING PAD SIL TO-220 | WARTH | 3223-07FR-54 | 2 |
| | 618001 | INSULATING BUSH TO-220 | MULLARD | 56359C | 2 |
| | 620007 | TEST POINT TERMINAL | MICROVAR | TYPE C30 | 12 |
| | 900003 | HEATSINK COMPOUND | RS | 554-311 | A/R |
| | 900004 | SILICONE RUBBER COMPOUND | RS | 555-588 | A/R |
| | 920088-1 | HEATSINK TO-3 | SEE DRG | | 1 |
| | 920089-1 | HEATSINK TO-220 | SEE DRG | | 1 |
| | 920105-1 | HEATSINK TO-202 | SEE DRG | | 3 |
| | 920126 | FUSE HOLDER 20mm PCB | BELLING LEE | L1426 | 6 |
| | 920142 | HEATSINK 2 X TO-220 | REDPOINT | TY35HI9 | 2 |

NOTES

SEE SHEET 2 FOR LATEST ISSUE

| | | | | | | | | | | | | | | | | | | | |
|------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ISS | | | | | | | | | | | | | | | | | | | |
| ECO | | | | | | | | | | | | | | | | | | | |
| DATE | | | | | | | | | | | | | | | | | | | |
| CHKD | | | | | | | | | | | | | | | | | | | |

| | | |
|----------|-----------------------|---------------------------|
| DATE | 29.2.84 | datron ELECTRONICS LTD |
| TITLE | 4200 PS (IG) PCB ASSY | |
| DRAWN | IL | DRAWING NUMBER 400554 |
| CHECKED | | |
| APPROVED | | SHEET 6 OF 7 |
| DATE | | |

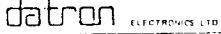
| | | | | | | | |
|------------------------------|----------------|--|------------------|-----------------|---------------------|------------------------------|----------------------------|
| DRAWING No. 400653 | | CHAD | 26.2.86 | 21.4.86 | 27.5.87 | 22.6.87 | 29.2.88 |
| TITLE LT WA1 | | DATE | 26.2.86 | 21.4.86 | 27.5.87 | 22.6.87 | 29.2.88 |
| | | ECO | 1.0 | 1.1 | 1.2 | 1.2 | 1.2 |
| | | REVISION | 1.0 | 1.1 | 1.2 | 1.2 | 1.2 |
| | | ISSUE | 1.0 | 1.1 | 1.2 | 1.2 | 1.2 |
| DESCRIPTION | DRAWING NUMBER | SHEET NUMBER | ISSUE / REVISION | | | | |
| COMP LAYOUT | 480653 | 1 | 1.0 | 1.1 | 1.2 | | |
| SCHEMATIC | 430653 | 1 | 1.0 | | | | |
| FUNCTIONAL TEST PROC. | 460653/FT | 1-4 | 1.0 | | 1.1 | | |
| FUNCT. TEST TICK LIST | 470653/FT | 1 | 1.0 | | | | |
| P.C.B. | 410254 | - | 2.0 | | | | |
| NOTES | |  | | DRN 11 | CHKD R.H. COGGAN | APPD [Signature] | TITLE 4700 |
| | | | | DATE 12.2.86 | DATE 3/3/86 | DATE 3.3.86 | TITLE PS (38V) PCB ASSY |
| | | | | | | DRAWING No. 400653 | |
| | | | | | | SHEET 1 OF 5 | |

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No. USED Per Assy. |
|------------|-----------------|-----------------------|------------------------|-------------------------|--------------------|
| R1 | 004752 | 7k5 2% 1/4W MET-OX | ELECTROSIL | TR4 | 2 |
| R2 | 011300 | 130R 1% 1/8W 50ppm MF | HOLCO | H8C | 2 |
| R3 | 000682 | 6k8 5% 1/3W CARBON | MULLARD | CR25 | 2 |
| R4 | 000563 | 56k 5% 1/3W CARBON | MULLARD | CR25 | 2 |
| R5 | 000104 | 100k 5% 1/3W CARBON | MULLARD | CR25 | 2 |
| R6 | 000103 | 10k 5% 1/3W CARBON | MULLARD | CR25 | 2 |
| R7 | 000471 | 470R 5% 1/3W CARBON | MULLARD | CR25 | 2 |
| R8 | 004752 | 7k5 2% 1/4W MET-OX | ELECTROSIL | TR4 | - |
| R9 | 011300 | 130R 1% 1/8W 50ppm MF | HOLCO | H8C | - |
| R10 | 000682 | 6k8 5% 1/3W CARBON | MULLARD | CR25 | - |
| R11 | 000563 | 56k 5% 1/3W CARBON | MULLARD | CR25 | - |
| R12 | 000104 | 100k 5% 1/3W CARBON | MULLARD | CR25 | - |
| R13 | 000103 | 10k 5% 1/3W CARBON | MULLARD | CR25 | - |
| R14 | 000471 | 470R 5% 1/3W CARBON | MULLARD | CR25 | - |
| R15 | 006392 | 3k9 % 1W MET-OX | ELECTROSIL | FPI | 2 |
| R16 | 006392 | 3k9 % 1W MET-OX | ELECTROSIL | FPI | - |
| R17 | 000272 | 2k7 5% 1/3W CARBON | MULLARD | CR25 | 2 |
| R18 | 000222 | 2k2 5% 1/3W CARBON | MULLARD | CR25 | 2 |
| R19 | 000308 | 3R0 5% 1/3W CARBON | MULLARD | CR25 | 2 |
| R20 | 012741 | 2k74 1% 1/8W 50ppm MF | HOLCO | H8C | 2 |
| R21 | 013922 | 39k2 1% 1/8W 50ppm MF | HOLCO | H8C | 2 |
| R22 | 000272 | 2k7 5% 1/3W CARBON | MULLARD | CR25 | - |
| R23 | 000222 | 2k2 5% 1/3W CARBON | MULLARD | CR25 | - |

NOTES:

SEE SHEET 1 FOR LATEST ISSUE

| | | | | | | | | | | | |
|------|---------|--------|--------|----------|--|--|--|--|--|--|--|
| ISS | 1 | 2 | 3 | 4 | | | | | | | |
| ECO | | 1684 | 1694 | 1776 | | | | | | | |
| DATE | 7.12.83 | 1.8.84 | 5.9.84 | 30.11.84 | | | | | | | |
| CHMD | MD | MD | MD | MD | | | | | | | |

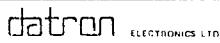
| | | |
|----------------|------------------------|---|
| DATE | 12.2.86 |  |
| DRAWN | 11 | |
| CHECKED | | |
| APPROVED | | |
| TITLE | 4700 PS (38V) PCB ASSY | |
| DRAWING NUMBER | 400653 | |
| SHEET | 2 | OF 5 |

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No. USED Per Assy. |
|------------|-----------------|-------------------------|------------------------|-------------------------|--------------------|
| R24 | 000308 | 3R0 5% 1/3W CARBON | MULLARD | CR25 | - |
| R25 | 012741 | 2k74 1% 1/8W 50ppm MF | HOLCO | H8C | - |
| R26 | 013922 | 39k2 1% 1/8W 50ppm MF | HOLCO | H8C | - |
| | | | | | |
| | | | | | |
| C1 | 110042 | 100nF 20% 63V POLYESTER | WIMA | MKS2 | 3 |
| C2 | 110042 | 100nF 20% 63V POLYESTER | WIMA | MKS2 | - |
| C3 | 110042 | 100nF 20% 63V POLYESTER | WIMA | MKS2 | - |
| C4 | 120028 | 4n7F 20% 100V POLYCARB | WIMA | FKC2 | 2 |
| C5 | 120028 | 4n7F 20% 100V POLYCARB | WIMA | FKC2 | - |
| C6 | 150016 | 1uF 20% 35V DIP TANT | UNION CARBIDE | K10E35 | 2 |
| C7 | 150015 | 10uF 20% 35V DIP TANT | UNION CARBIDE | K10E35 | 2 |
| C8 | 150015 | 10uF 20% 35V DIP TANT | UNION CARBIDE | K10E35 | - |
| C9 | 150016 | 1uF 20% 35V DIP TANT | UNION CARBIDE | K10E35 | - |
| C10 | 180040 | 10uF 100V AL ELECT | ECC | SMVB | 2 |
| C11 | 180040 | 10uF 100V AL ELECT | ECC | SMVB | - |

NOTES:

SEE SHEET 2 FOR LATEST ISSUE

| | |
|----------|---------|
| DATE | 12.2.86 |
| DRAWN | |
| CHECKED | |
| APPROVED | |
| DATE | |



TITLE
4700 PS (38V) PCB ASSY

DRAWING NUMBER 400653


SHEET 3 OF 5

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No. USED Per Assy. |
|------------|-----------------|----------------------|------------------------|-------------------------|--------------------|
| D1 | 210270 | 27V 400mW ZENER | MULLARD | BZY88C27 | 2 |
| D2 | 210270 | 27V 400mW ZENER | MULLARD | BZY88C27 | - |
| D3 | 200001 | 75mA 75V GP Si DIODE | FAIRCHILD | IN4148 | 2 |
| D4 | 200001 | 75mA 75V GP Si DIODE | FAIRCHILD | IN4148 | - |
| D5 | 214012 | 2V45 30ppm ZENER | FERRANTI | ZN458 | 2 |
| D6 | 214012 | 2V45 30ppm ZENER | FERRANTI | ZN458 | - |
| D7 | 210068 | 6V8 400mW ZENER | MULLARD | BZY88C6V8 | 2 |
| D8 | 210068 | 6V8 400mW ZENER | MULLARD | BZY88C6V8 | - |
| | | | | | |
| | | | | | |
| Q1 | 250026 | Si PNP TRANSISTOR | MOTOROLA | TIPI46 | 1 |
| Q2 | 240037 | Si NPN TRANSISTOR | MOTOROLA | TIPI41 | 1 |
| Q3 | 250018 | Si PNP TRANSISTOR | MOTOROLA | BC556/TO18 | - |
| Q4 | 250018 | Si PNP TRANSISTOR | MOTOROLA | BC556/TO18 | 3 |
| Q5 | 240029 | Si NPN TRANSISTOR | MOTOROLA | BC546/TO18 | - |
| Q6 | 240029 | Si NPN TRANSISTOR | MOTOROLA | BC546/TO18 | 3 |
| Q7 | 250018 | Si PNP TRANSISTOR | MOTOROLA | BC556/TO18 | - |
| Q8 | 240029 | Si NPN TRANSISTOR | MOTOROLA | BC546/TO18 | - |

NOTES:

SEE SHEET 2 FOR LATEST ISSUE

| | |
|----------|---------|
| DATE | 12.2.86 |
| DRAWN | |
| CHECKED | |
| APPROVED | |
| DATE | |



TITLE
4700 PS (38V) PCB ASSY

DRAWING NUMBER 400653

SHEET 4 OF 5


| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No. USED Per Assy. |
|------------|-----------------|------------------------|------------------------|-------------------------|--------------------|
| MI | 260043 | 358 DUAL OP AMP | NATIONAL | LM358N | 1 |
| F1 | 920120 | FUSE 1A 125V 7mm | LITTLEFUSE | 275 001 | 2 |
| F2 | 920120 | FUSE 1A 125V 7mm | LITTLEFUSE | 275 001 | - |
| | 410254-2 | PCB | | | 1 |
| | 605059/A | 8 WAY DIL SOCKET | | | 1 |
| | 611016 | M3x8mm POZIPAN STEEL | ZN.PL. | | 1 |
| | 613005 | M3 INT. SHAKEPROOF | ZN. PL. | | 2 |
| | 613007 | M3 WASHER STEEL | ZN. PL. | | 1 |
| | 615002 | M3 FULL NUT STEEL | ZN. PL. | | 2 |
| | 620007 | TEST POINT TERMINAL | MICROVAR | TYPE C30 | 8 |
| | 900003 | HEATSINK COMPOUND | RS | 554-311 | A/R |
| | 920141 | HEATSINK TO-220 | AAVID | 50418 | 2 |
| | 611006 | M3x10mm POZI-PAN STEEL | ZN. PL. | | 1 |
| | 618001 | INSULATING BUSH TO220 | MULLARD | 56359C | 1 |
| | 618014 | INSULATING PAD TIP36 | WARTH | 4177-NA-53 | 1 |
| | 618004 | MOUNTING PAD TO18 | JERMYN | TO18-008D | 2 |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |

NOTES.

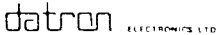
SEE SHEET 2 FOR LATEST ISSUE

| | | | | | | | | | | | | | | | | | | | | |
|------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ISS | | | | | | | | | | | | | | | | | | | | |
| ECO | | | | | | | | | | | | | | | | | | | | |
| DATE | | | | | | | | | | | | | | | | | | | | |
| TOP | | | | | | | | | | | | | | | | | | | | |

| | | | |
|----------|---------|------------------------|--------|
| DATE | 12.2.86 | datron ELECTRONICS LTD | |
| DRAWN | | TITLE | |
| CHECKED | | 4700 PS(38V)PCB ASSY | |
| APPROVED | | DRAWING NUMBER | 400653 |
| DATE | | SHEET | 5 OF 5 |

| | | | | |
|---|----------------|--|-------------------------|---|
| DRAWING No 400637 | | CHKD R.K. COGGAN | DATE 20.12.85 | ECO 1.0 2162.4.3.86 1.1 2220 22.4.86 1.2 2276 13.6.86 1.2 2253 15.3.87 1.3 2259 12.6.87 1.3 2266 12.8.87 1.3 2724 10.12.87 1.3 2751 29.2.88 1.4 2956 12.7.88 1.5 3015 15.2.88 1.6 3272 16.04.89 |
| DLWM | | REVISION ISSUE | | |
| DESCRIPTION | DRAWING NUMBER | SHEET NUMBER | ISSUE - REVISION | |
| COMPONENT LAYOUT | 480637 | 1 | 1.0 | 1.1 |
| SCHEMATIC | 430637 | 1 | 1.0 | 1.1 |
| FUNCTIONAL TEST PROC. | 460637/FT | 1-2 | 1.0 | 1.1 |
| FUNCT. TEST TICK LIST | 470637/FT | 1 | 1.0 | 1.1 |
| PCB | 410245 | 4-0 | | |
| NOTES <input type="checkbox"/> DENOTES NO CHANGE TO DOC AT ISSUE LEVEL CHANGE. | |  | | DRN 11 DATE 20.12.85 |
| | | CHKD R.K. COGGAN DATE 5/3/86 | | APPR [Signature] DATE 4.3.88 |
| | | TITLE 4700 PA (POS) H/S ASSY. | | DRAWING No. 400637 SHEET 1 OF 7 |

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No. USED Per Assy. |
|------------|-----------------|-----------------------|------------------------|-------------------------|--------------------|
| R1 | | NOT USED | | | - |
| R2 | 008057 | 22k 5% 9W WW RES | WELWYN | W23 | 1 |
| R3 | 000101 | 100R 5% 1/3W CF RES | MULLARD | CR25 | 5 |
| R4 | 000101 | 100R 5% 1/3W CF RES | MULLARD | CR25 | - |
| R5 | 000101 | 100R 5% 1/3W CF RES | MULLARD | CR25 | - |
| R6 | 000101 | 100R 5% 1/3W CF RES | MULLARD | CR25 | - |
| R7 | 008055 | 2R2 1% 1/2W MET GLAZE | NEOHM | RGPO207 | 4 |
| R8 | 008055 | 2R2 1% 1/2W MET GLAZE | NEOHM | RGPO207 | - |
| R9 | 008055 | 2R2 1% 1/2W MET GLAZE | NEOHM | RGPO207 | - |
| R10 | 064105 | 1M 15 TURN V CM POT | BECKMAN | 89P | 1 |
| R11 | 090155 - 1 | 10K NTC THERMISTOR | DALE ELECTRONICS | SEE DRG | 2 |
| R12 | 090155 - 1 | 10K NTC THERMISTOR | DALE ELECTRONICS | SEE DRG | - |
| R13 | 008055 | 2R2 1% 1/2W MET GLAZE | NEOHM | RGPO207 | - |
| R14 | 008021 | 0R47 5% 2.5W WW RES | WELWYN | W21 | 1 |
| R15 | 012743 | 274k 1% 1/8W 50ppm MF | HOLCO | H8C | 4 |
| R16 | 012743 | 274k 1% 1/8W 50ppm MF | HOLCO | H8C | - |
| R17 | | NOT USED | | | - |
| R18 | | NOT USED | | | - |
| R19 | 000101 | 100R 5% 1/3W CF RES | MULLARD | CR25 | - |
| R20 | 000102 | 1K 5% 1/3W CF RES | MULLARD | CR25 | 1 |
| R21 | 000470 | 47R 5% 1/3W CF RES | MULLARD | CR25 | 1 |
| R22 | 012743 | 274k 1% 1/8W 50ppm MF | HOLCO | H8C | - |
| R23 | 012743 | 274k 1% 1/8W 50ppm MF | HOLCO | H8C | - |

| | | | | | | | | | | | | |
|------------------------------|---------|---------|---------|---------|----------|----------|---------|---------|---------|------------------|---|--------------------------|
| NOTES | | | | | | | | | | DATE 20.12.85 |  | |
| SEE SHEET 1 FOR LATEST ISSUE | | | | | | | | | | DRAWN L. | TITLE 4700 PA (POS) H/S ASSY | |
| ECO | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | | APPROVED | DRAWING NUMBER 400637 |
| DATE | 29.5.84 | 25.7.84 | 20.9.84 | 4.10.84 | 25.10.84 | 28.11.84 | 14.1.85 | 29.1.85 | 19.4.85 | | DATE | SHEET 2 OF 7 |
| CHKD | M | MD | MD | MD | MD | MD | MD | MD | MD | | DATE | |

| DESIGNATOR | DATRON PART No | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No | No USED In Assy |
|------------|----------------|----------------------------|------------------------|------------------------|-----------------|
| | 612004-1 | M3 x 4mm STANDOFF | HARWIN | CS2116/B | 8 |
| | 613029 | M3 WAVY WASHER SS | | | 16 |
| | 615002 | M3 FULL NUT STEEL ZN PL. | | | 4 |
| | 620003 | SOLDER PIN | HARWIN | H2105A01 | 12 |
| | 620007 | TEST POINT TERMINAL | MICROVAR | TYPE C30 | 4 |
| | 630024 | STEATITE BEAD 16 SWG | PARK ROYAL PORCELAIN | Nº2 | 2 |
| | 630126 | 'P' CLIP ϕ 7.9mm | RICHCO | N5 | 1 |
| | 613017 | M3 WASHER NYLON | | | 1 |
| | 900003 | HEATSINK COMPOUND | RS | 554-311 | A/R |
| FBI | 920145 | FERROXCUBE BEAD | MULLARD | FX4026 | 1 |
| | 590033 | SLEEVE MAX CABLE ϕ 10 | HELLERMANN ELECTRIC | H50 x 25mm BLK. HELSYN | 2 |
| | 420098 | LABEL SERIAL Nº | RS | 554-793 | 1 |
| | 420112-1 | LABEL SSD WARNING | SEE DRG | | 1 |
| | 605059 | 8 WAY DIL SOCKET | | | 1 |
| J3 | 605053 | 12-WAY .1" HOUSING | MOLEX | 22-01-2125 | 1 |
| | 613007 | M3 WASHER STEEL ZN PL | | | 4 |
| | 614001 | M3 CLEAR x 4mm STANDOFF | HARWIN | CS2117B | 4 |
| | 540002 | 22 SWG B.T.C. WIRE | | | A/R |
| | 590004 | SLEEVE ϕ 1.0 PTFE | HELLERMANN | FE10 | A/R |
| | 900004 | SILICONE RUBBER COMP. | RS | 555-588 | A/R |

NOTES.

SEE SHEET 2 FOR LATEST ISSUE

| | | | | | | | | | | | | | | | | | | | | |
|------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ISS | | | | | | | | | | | | | | | | | | | | |
| ECD | | | | | | | | | | | | | | | | | | | | |
| DATE | | | | | | | | | | | | | | | | | | | | |
| CHKD | | | | | | | | | | | | | | | | | | | | |

| | | |
|----------|----------|---------------------------|
| DATE | 20.12.85 | datron ELECTRONICS LTD |
| DRAWN | IL | |
| CHECKED | | TITLE |
| APPROVED | | 4700.PA (POS) H/S ASSY |
| DATE | | DRAWING NUMBER |
| | | 400637 |
| | | SHEET |
| | | 7 of 7 |

| | | | | | | | | | | | | |
|-----------------------------|-----------|---------------------|-----|------------------------|-----|------------------|-----|----------|-----|-------|-----|-----|
| DRAWING No 400539 | | CHK D WJD | | DATE 12.7.85 | | E.C.O. | | REVISION | | ISSUE | | |
| DESCRIPTION | | DRAWING NUMBER | | SHEET NUMBER | | ISSUE + REVISION | | | | | | |
| COMPONENT LAYOUT | 480539 | 1 | 7.0 | 7.1 | 7.2 | 7.3 | 7.4 | 7.5 | 7.6 | 7.7 | 7.8 | 7.9 |
| SCHMATIC | 430539 | 1 | 7.0 | 7.1 | 7.2 | 7.3 | 7.4 | 7.5 | 7.6 | 7.7 | 7.8 | 7.9 |
| FUNCTIONAL TEST PROC | 460539/FT | 1-2 | 7.0 | | | | | | 7.1 | 7.2 | | |
| FUNC. TEST TICK LIST | 470539/FT | 1 | 7.0 | | | | | | 7.1 | 7.2 | | |
| PCB | 410246 | 1 | | | | 4 | | | | | | |

| | | | | | | | |
|-------|---|---|------------------------|------------------------|------|--|------------------------------|
| NOTES | <input type="checkbox"/> DENOTES NO CHANGE TO DOC AT ISSUE LEVEL CHANGE | datron INTEGRATED COMPONENTS NORWICH ENGLAND | DRN IL | CHK D WJD | APPD | FILE 4200 PA (NEG) H/S ASSY. | DRAWING No. 400539 |
| | | | DATE 10.7.85 | DATE 12.7.85 | DATE | | SHEET 1 OF 6 |

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No. USED Per Assy |
|------------|-----------------|-------------------------|------------------------|-------------------------|-------------------|
| R1 | | NOT USED | | | - |
| R2 | 008057 | 22k 5% 9W WW RES | WELWYN | W23 | - |
| R3 | 000101 | 100R 5% 1/3W CF RES | MULLARD | CR25 | 5 |
| R4 | 000101 | 100R 5% 1/3W CF RES | MULLARD | CR25 | - |
| R5 | 000101 | 100R 5% 1/3W CF RES | MULLARD | CR25 | - |
| R6 | 008055 | 2R2 1% 1/2W MET-GLAZE | NEOHM | RGPO207 | 4 |
| R7 | 008055 | 2R2 1% 1/2W MET-GLAZE | NEOHM | RGPO207 | - |
| R8 | 000101 | 100R 5% 1/3W CF RES | MULLARD | CR25 | - |
| R9 | 090155-1 | 10K NTC THERMISTOR | DALE ELECTRONICS | SEE DRG | 2 |
| R10 | 090155-1 | 10K NTC THERMISTOR | DALE ELECTRONICS | SEE DRG | - |
| R11 | 008055 | 2R2 1% 1/2W MET-GLAZE | NEOHM | RGPO207 | - |
| R12 | 012743 | 274k 1% 1/8W 50ppm MF | HOLCO | H8C | 4 |
| R13 | 012743 | 274k 1% 1/8W 50ppm MF | HOLCO | H8C | - |
| R14 | 008055 | 2R2 1% 1/2W MET-GLAZE | NEOHM | RGPO207 | - |
| R15 | 008021 | 0R47 5% 2-SW WW RES | WELWYN | W21 | 1 |
| R16 | 000101 | 100R 5% 1/3W CF RES | MULLARD | CR25 | - |
| R17 | 012743 | 274k 1% 1/8W 50ppm MF | HOLCO | H8C | - |
| R18 | 012743 | 274k 1% 1/8W 50ppm MF | HOLCO | H8C | - |
| C1 | 110043 | 10nF 20% 630V POLYESTER | WIMA | MKS4 | 4 |
| C2 | 110043 | 10nF 20% 630V POLYESTER | WIMA | MKS4 | - |
| C3 | 110043 | 10nF 20% 630V POLYESTER | WIMA | MKS4 | - |
| C4 | 110043 | 10nF 20% 630V POLYESTER | WIMA | MKS4 | - |

| | | | |
|-------|---|------------------------|---------------------------------|
| NOTES | SEE SHEET 1 FOR LATEST ISSUE | DATE 22.2.84 | datron ELECTRONICS LTD |
| ISS | 1 2 3 4 5 6 7 | DATE 29.5.84 | 4200 PA (NEG) H/S ASSY |
| DATE | 29.5.84 24.7.84 4.10.84 25.10.84 28.11.84 14.1.85 19.4.85 | DATE | DRAWING NUMBER 400539 |
| | | | SHEET 2 OF 6 |

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No. USED Per Assy. |
|------------|-----------------|------------------------------|------------------------|-------------------------|--------------------|
| | 410246-1 | PCB | | | 1 |
| | 420080-1 | LABEL 'DANGER HIGH VOLTAGE' | | | 2 |
| | 450454-1 | HEATSINK 64mm | | | 1 |
| | 450455-1 | HEATSINK 91mm | | | 1 |
| | 605118-1 | SOCKET ϕ 1.02 | CAMBION | SEE DRAWING. A4. | 8 |
| | 590005 | SLEEVE MAX. CABLE ϕ 4.0 | HELLERMANN ELECTRIC | H20 x 20mm BLACK HELSYN | 1 |
| | 590001 | SLEEVE MAX. CABLE ϕ 3.0 | HELLERMANN ELECTRIC | H15 x 20mm BLACK HELSYN | 3 |
| | 590002 | SLEEVE MAX. CABLE ϕ 6.0 | HELLERMANN ELECTRIC | H15 x 25mm BLACK HELSYN | 3 |
| FB2 | 920145 | FERROXUBE BEAD | MULLARD | FX 4026 | 1 |
| J1 | 604033 | 4 WAY .1" PCB PLUG GD. PL. | MOLEX | 22-29-2041 | 2 |
| J2 | 605053 | 12 WAY .1" HOUSING | MOLEX | 22-01-2125 | 1 |
| | 605057 | CRIMP TERMINAL GD. PL. | MOLEX | 4809-GL | 5 |
| | 590004 | SLEEVE ϕ 1.0 PTFE | HELLERMANN | FE10 | A/R |
| | 611006 | M3 x 10mm POZIPAN STEEL | ZN PL | | 9 |
| | 611027 | M3 x 20mm POZIPAN STEEL | ZN PL | | 3 |
| | 612004-1 | M3 x 4mm STANDOFF | HARWIN | CS2116/B | 8 |
| | 613029 | M3 WAY WASHER SS | | | 15 |
| | 613007 | M3 WASHER STEEL | ZN PL | | 3 |
| | 615002 | M3 FULL NUT STEEL | ZN PL | | 3 |
| | 620003 | SOLDER PIN | HARWIN | H2105A01 | 5 |
| | 620007 | TEST POINT TERMINAL | MICROVAR | TYPE C30 | 4 |
| | 630003 | 'P' CLIP ϕ 4.8mm | SES | CN5 | 1 |
| | 900003 | HEATSINK COMPOUND | RS | 554-311 | A/R |

NOTES:

SEE SHEET 2 FOR LATEST ISSUE

| | | |
|----------|----------|------------------------|
| DATE | 23.2.84. | datron ELECTRONICS LTD |
| DRAWN | 11 | |
| CHECKED | | TITLE |
| APPROVED | | 4200 PA (NEG) H/S ASSY |
| DATE | | DRAWING NUMBER |
| | | 400539 |
| | | SHEET |
| | | 5 OF 6 |

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No. USED Per Assy. |
|------------|-----------------|---------------------------------|------------------------|-------------------------|--------------------|
| | 512222 | 7/2 PTFE INSULATED (RED) WIRE | | | A/R |
| | 512444 | 7/2 PTFE INSULATED (YEL) WIRE | | | A/R |
| | 512666 | 7/2 PTFE INSULATED (BLUE) WIRE | | | A/R |
| | 512999 | 7/2 PTFE INSULATED (WHITE) WIRE | | | A/R |
| | 512333 | 7/2 PTFE INSULATED (OR) WIRE | | | A/R |
| | 420098 | LABEL SERIAL No | RS | 554-793 | 1 |
| | 420112-1 | LABEL SSD WARNING | SEE DRG | | 1 |
| | 630024 | STEATITE BEAD 16SWG | PARK ROYAL PORCELAIN | Nº 2 | 2 |
| | 614001 | M3 CLEAR x 4mm STANDOFF | HARWIN | CS2117B | 4 |

NOTES:

SEE SHEET 2 FOR LATEST ISSUE

| | | |
|----------|---------|------------------------|
| DATE | 22.2.84 | datron ELECTRONICS LTD |
| DRAWN | | |
| CHECKED | | TITLE |
| APPROVED | | 4200 PA (NEG) H/S ASSY |
| DATE | | DRAWING NUMBER |
| | | 400539 |
| | | SHEET |
| | | 6 OF 6 |

| | | | | | | |
|------------------------------|--|--------------------|------------------------|---------|----------|-------|
| DRAWING No. 400540 | | CHK'D MD | DATE 10.7.85 | ECO | REVISION | ISSUE |
| TITLE HW | | 6.0 | 1958 | 10.7.85 | MD | |
| | | 6.1 | 2048 | 21.0.85 | AD | |
| | | 6.1 | 2069 | 3.12.85 | AD | |
| | | 6.2 | 2219 | 22.4.86 | AD | |
| | | 6.3 | 2315 | 11.7.86 | AD | |
| | | 6.4 | 2366 | 7.11.86 | AD | |
| | | 6.5 | 2444 | 7.11.86 | AD | |
| | | 6.6 | 2535 | 5.3.87 | AD | |
| | | 6.6 | 2560 | 26.3.87 | AD | |
| | | 6.6 | 2609 | 22.6.87 | AD | |
| | | 6.6 | 2651 | 25.8.87 | AD | |
| | | 6.6 | 2751 | 29.2.88 | AD | |
| | | 6.7 | 3015 | 5.9.88 | AD | |

| DESCRIPTION | DRAWING NUMBER | SHEET NUMBER | ISSUE - REVISION | | | | | | | | |
|-----------------------|----------------|--------------|------------------|-----|-----|-----|-----|-----|-----|-----|-----|
| COMPONENT LAYOUT | 480540 | 1 | 6.0 | 6.1 | 6.2 | 6.3 | 6.4 | 6.5 | 6.6 | 6.7 | 6.8 |
| SCHEMATIC | 430540 | 1 | 6.0 | | | | | 6.1 | | | |
| FUNCTIONAL TEST PROC. | 460540/FT | 1-5 | 6.0 | | | | | | | 6.1 | |
| FUNC. TEST TICK LIST | 470540/FT | 1 | 6.0 | | | | | | | 6.1 | |

| | | | | | | | |
|-------|---|---|------------------------------|---------------------------------|-------------------------------|-----------------------------|---------------------------------------|
| NOTES | <input type="checkbox"/> DENOTES NO CHANGE TO DOC AT ISSUE LEVEL CHANGE | datron INSTRUMENTS LTD NORWICH ENGLAND | DRN DATE 11 10.7.85 | CHK'D DATE 150 12.7.85 | APPR DATE 57 23.7.85 | TITLE 4200 PS/I H/S ASSY | DRAWING No. 400540 SHEET 1 OF 8 |
|-------|---|---|------------------------------|---------------------------------|-------------------------------|-----------------------------|---------------------------------------|

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No. USED Per Assy |
|------------|-----------------|-----------------------|------------------------|-------------------------|-------------------|
| R1 | 000101 | 100R 5% 1/3W CF RES | MULLARD | CR25 | 2 |
| R2 | 008037 | OR18 10% 2.5W WW RES | WELWYN | W21 | 2 |
| R3 | 008037 | OR18 10% 2.5W WW RES | WELWYN | W21 | - |
| R4 | 000101 | 100R 5% 1/3W CF RES | MULLARD | CR25 | - |
| R5 | 008045 | 10K 1% 1/2W MET-GLAZE | NEOHM | RGPO207 | 2 |
| R6 | 000102 | 1K 5% 1/3W CF RES | MULLARD | CR25 | 1 |
| R7 | 000220 | 22R 5% 1/3W CF RES | MULLARD | CR25 | 1 |
| R8 | 006105 | 1M 2% 1W MET-OX | ELECTROSIL | FPI | 4 |
| R9 | 014991 | 4K99 1% 1/8W 50ppm MF | HOLCO | H8C | 2 |
| R10 | 016811 | 6k81 1% 1/8W 50ppm MF | HOLCO | H8C | 2 |
| R11 | | NOT USED | | | - |
| R12 | 000821 | 820R 5% 1/3W CF RES | MULLARD | CR25 | 2 |
| R13 | 006105 | 1M 2% 1W MET-OX | ELECTROSIL | FPI | - |
| R14 | 007204 | 200k 2% 2W MET-OX | ELECTROSIL | FP2 | 4 |
| R15 | 011821 | 1k82 1% 1/8W 50ppm MF | HOLCO | H8C | 2 |
| R16 | 016192 | 61k9 1% 1/8W 50ppm MF | HOLCO | H8C | 2 |
| R17 | 008062 | 10R 1% 2 1/2W WW RES | WELWYN | W21 | 2 |
| R18 | 006105 | 1M 2% 1W MET-OX | ELECTROSIL | FPI | - |
| R19 | 007204 | 200k 2% 2W MET-OX | ELECTROSIL | FP2 | - |
| R20 | 011821 | 1k82 1% 1/8W 50ppm MF | HOLCO | H8C | - |
| R21 | 016192 | 61k9 1% 1/8W 50ppm MF | HOLCO | H8C | - |
| R22 | 006105 | 1M 2% 1W MET-OX | ELECTROSIL | FPI | - |
| R23 | 008062 | 10R 1% 2 1/2W WW RES | WELWYN | W21 | - |

| | | | | | | | |
|------------------------------|---------|---------|----------|--------|---------|-----------------|-------------------------------|
| NOTES | | | | | | DATE 23.2.84 | datron ELECTRONICS LTD |
| SEE SHEET 1 FOR LATEST ISSUE | | | | | | DRAWN 11 | TITLE 4200 PS/I H/S ASSY |
| ISS | 1 | 2 | 3 | 4 | 5 | 6 | CHECKED OC |
| ECO | 1691 | 1731 | 1740 | 1775 | 1805 | 1869 | APPROVED 57 |
| DATE | 29.5.84 | 20.8.84 | 18.10.84 | 9.1.85 | 19.4.85 | 30.4.85 | DATE 29.5.84 |
| CHK'D | MD | AD | AD | AD | AD | AD | DRAWING NUMBER 400540 |
| | | | | | | SHEET 2 OF 8 | |

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No. USED Per Assy |
|------------|-----------------|-------------------------------|------------------------|-------------------------|-------------------|
| R24 | 008045 | 10k 1% 1/2W MET-GLAZE | NEOHM | RGPO207 | - |
| R25 | | NOT USED | | | - |
| R26 | 000821 | 820R 5% 1/3W CF RES | MULLARD | CR25 | - |
| R27 | 014991 | 4k99 1% 1/8W 50ppm MF | HOLCO | H8C | - |
| R28 | | NOT USED | | | - |
| R29 | 016811 | 6k81 1% 1/8W 50ppm MF | HOLCO | H8C | - |
| R30 | 007204 | 200k 2% 2W MET-OX | ELECTROSIL | FP2 | - |
| R31 | 007204 | 200k 2% 2W MET-OX | ELECTROSIL | FP2 | - |
| R32 | 005470 | 47R 2% 1/2W MET-OX | ELECTROSIL | TR5 | 2 |
| R33 | 005470 | 47R 2% 1/2W MET-OX | ELECTROSIL | TR5 | - |
| R34 R35 | 013920 | 392R 1% 1/8W 50ppm MF | HOLCO | H8C | 2 |
| C1 | 104025 | 100nF $\pm 20\%$ 50V CER DISC | SIEMENS | B37449 | 1 |
| C2 | | NOT USED | | | - |
| C3 | | NOT USED | | | - |
| C4 | | NOT USED | | | - |
| C5 | 180045 | 47 μ F 63V AL. ELECT. | MULLARD | 031-38479 | 2 |
| C6 | 180045 | 47 μ F 63V AL. ELECT. | MULLARD | 031-38479 | - |
| C7 | | NOT USED | | | - |
| C8 | 120033 | 2n2F 20% 1kV POLYCARB | WIMA | FKC3 | 2 |
| C9 | 150006 | 4 μ 7F 20% 16V DIP TANT | UNION CARBIDE | K4R7E1G | 2 |
| C10 | 120033 | 2n2F 20% 1kV POLYCARB | WIMA | FKC3 | - |
| C11 | 150006 | 4 μ 7F 20% 16V DIP TANT | UNION CARBIDE | K4R7E1G | - |
| C12 | | NOT USED | | | - |

NOTES:

SEE SHEET 2 FOR LATEST ISSUE

| | | | | | | | | | | | | | | |
|------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ISS | | | | | | | | | | | | | | |
| PCD | | | | | | | | | | | | | | |
| DATE | | | | | | | | | | | | | | |
| CHRD | | | | | | | | | | | | | | |

| | | | |
|-----------------|------------------------------|--------------------|--|
| DATE 23.2.84 | datron ELECTRONICS LTD | | |
| DRAWN L. | TITLE 4200. PS/I H/S ASSY | | |
| CHECKED | APPROVED | | |
| DATE | DRAWING NUMBER 400540 | SHEET OF 3 OF 8 | |

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No. USED Per Assy |
|------------|-----------------|-------------------------|------------------------|------------------------------------|-------------------|
| C13 | 104043 | 100pF 10% 500V CER DISC | STC | CD10KWK100PMS ^{65C} SS500 | 2 |
| C14 | 104043 | 100pF 10% 500V CER DISC | STC | CD10KWK100PMS ^{65C} SS500 | - |
| C15 | 150010 | 330nF 20% 35V DIP TANT | UNION CARBIDE | KR33E35 | 2 |
| C16 | 150010 | 330nF 20% 35V DIP TANT | UNION CARBIDE | KR33E35 | - |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |

NOTES:

SEE SHEET 2 FOR LATEST ISSUE

| | | | | | | | | | | | | | | |
|------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ISS | | | | | | | | | | | | | | |
| PCD | | | | | | | | | | | | | | |
| DATE | | | | | | | | | | | | | | |
| CHRD | | | | | | | | | | | | | | |

| | | | |
|------------------|------------------------------|--------------------|--|
| DATE 18.10.84 | datron ELECTRONICS LTD | | |
| DRAWN | TITLE 4200. PS/I H/S ASSY | | |
| CHECKED | APPROVED | | |
| DATE | DRAWING NUMBER 400540 | SHEET OF 4 OF 8 | |

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No. USED Per Assy |
|------------|-----------------|------------------------|------------------------|-------------------------|-------------------|
| D1 | 210056 | 5V6 400mW ZENER | MULLARD | BZY88C5V6 | 2 |
| D2 | 210150 | 15V 400mW ZENER | MULLARD | BZY88C15 | 4 |
| D3 | 213020 | 30V 5% 1/2W ZENER | MULLARD | BZX79C30 | 2 |
| D4 | 200006 | 1A 600V GP Si DIODE | FAIRCHILD | IN4005 | 4 |
| D5 | 213021 | 56V 2% 400mW ZENER | MULLARD | BZX79B56 | 2 |
| D6 | 200006 | 1A 600V GP Si DIODE | FAIRCHILD | IN4005 | - |
| D7 | 214014 | 1V22 100ppm ZENER | TELEDYNE | 9491BJ | 2 |
| D8 | 210150 | 15V 400mW ZENER | MULLARD | BZY88C15 | - |
| D9 | 210150 | 15V 400mW ZENER | MULLARD | BZY88C15 | - |
| D10 | 200006 | 1A 600V GP Si DIODE | FAIRCHILD | IN4005 | - |
| D11 | 213020 | 30V 5% 1/2W ZENER | MULLARD | BZX79C30 | - |
| D12 | 213021 | 56V 2% 400mW ZENER | MULLARD | BZX79B56 | - |
| D13 | 200006 | 1A 600V GP Si DIODE | FAIRCHILD | IN4005 | - |
| D14 | 210150 | 15V 400mW ZENER | MULLARD | BZY88C15 | - |
| D15 | 210056 | 5V6 400mW ZENER | MULLARD | BZY88C5V6 | - |
| D16 | 214014 | 1V22 100ppm ZENER | TELEDYNE | 9491BJ | - |
| Q1 | 240036 | Si NPN DARL TRANSISTOR | MOTOROLA | MJ1000 | 1 |
| Q2 | 250024 | Si PNP DARL TRANSISTOR | MOTOROLA | MJ900 | 1 |
| Q3 | 230063 | N-CHAN TMOS JFET | MOTOROLA | MTP2N85 | 1 |
| Q4 | 250001 | Si PNP TRANSISTOR | NATIONAL | BC214/TO18 | 1 |
| Q5 | 240006 | Si NPN TRANSISTOR | NATIONAL | 2N3904/TO18 | 1 |

NOTES:

SEE SHEET 2 FOR LATEST ISSUE

| ISS | F.C.O | DATE | CHKD |
|-----|-------|------|------|
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |

| | | |
|-----------------|------------------------------|--------------------|
| DATE 23.2.84 | datron ELECTRONICS LTD | |
| DRAWN L | TITLE 4200. PS/I H/S ASSY | |
| CHECKED | APPROVED | |
| DATE | DRAWING NUMBER 400540 | SHEET OF 5 of 8 |

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No. USED Per Assy |
|------------|-----------------|-------------------------------|------------------------|-------------------------|-------------------|
| Q6 | 250004 | Si PNP TRANSISTOR | NATIONAL | 2N3906/TO92 | 1 |
| Q7 | 240001 | Si NPN TRANSISTOR | NATIONAL | BC184/TO92 | 2 |
| Q8 | 230001 | N-CHAN I LIM 1.4 mA | TELEDYNE | TCR506 | 2 |
| Q9 | 230062 | P-CHAN T.MOS JFET | MOTOROLA | MTM2P50 | 1 |
| Q10 | 230001 | N-CHAN I LIM 1.4 mA | TELEDYNE | TCR506 | - |
| Q11 | 230064 | P-CHAN T.MOS JFET | MOTOROLA | MTP2P50 | 1 |
| Q12 | 230061 | N-CHAN T.MOS JFET | MOTOROLA | MTM2N85 TO3 | 1 |
| Q13 | 240001 | Si NPN TRANSISTOR | NATIONAL | BC184/TO18 | - |
| M1 | 220018 | Hi-SPEED OPTO ISOLATOR | HP | 6N136 | 2 |
| M2 | 220018 | Hi-SPEED OPTO ISOLATOR | HP | 6N136 | - |
| | 410247-3 | PCB | | | 1 |
| | 420080-1 | LABEL 'DANGER HIGH VOLTAGE' | | | 1 |
| | 450456-1 | HEATSINK | | | 1 |
| | 512111 | 7/2 PTFE INSULATED (BRN) WIRE | RS | | A/R |
| | 512222 | 7/2 PTFE INSULATED (RED) WIRE | RS | | A/R |
| | 512444 | 7/2 PTFE INSULATED (YEL) WIRE | RS | | A/R |
| | 512555 | 7/2 PTFE INSULATED (GRN) WIRE | RS | | A/R |
| | 512666 | 7/2 PTFE INSULATED (BLU) WIRE | RS | | A/R |

NOTES:

SEE SHEET 2 FOR LATEST ISSUE

| ISS | F.C.O | DATE | CHKD |
|-----|-------|------|------|
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |

| | | |
|-----------------|------------------------------|--------------------|
| DATE 23.2.84 | datron ELECTRONICS LTD | |
| DRAWN L | TITLE 4200. PS/I H/S ASSY | |
| CHECKED | APPROVED | |
| DATE | DRAWING NUMBER 400540 | SHEET OF 6 of 8 |

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No. USED Per Assy. |
|------------|-----------------|------------------------------|------------------------|-------------------------|--------------------|
| AN1 | 090131 | 10K x 4 2% SIL NETWORK | BECKMAN | LO8-3-R10K | 2 |
| AN2 | 090131 | 10k x 4 2% SIL NETWORK | BECKMAN | LO8-3-R10K | - |
| AN3 | 090096 | 1M x 8 2% NETWORK | BECKMAN | LO9-1-R1M | 1 |
| C1 | 140047 | 33nF 10% 1k5V POLYPROP | STEATITE | MKP1841 | 3 |
| C2 | 140047 | 33nF 10% 1k5V POLYPROP | STEATITE | MKP1841 | - |
| C3 | 180048 | 470uF 50V AL. ELEC. | ECC | SMVB | 2 |
| C4 | 180048 | 470uF 50V AL. ELEC. | ECC | SMVB | - |
| C5 | 104026 | 47nF $\pm 50\%$ 50V CER DISC | SIEMENS | B37449 | 3 |
| C6 | 104026 | 47nF $\pm 50\%$ 50V CER DISC | SIEMENS | B37449 | - |
| C7 | 104026 | 47nF $\pm 50\%$ 50V CER DISC | SIEMENS | B37449 | - |
| C8 | 102102 | 1nF 10% 500V CER DISC | ITT | CD10 | 1 |

NOTES.

SEE SHEET 2 FOR LATEST ISSUE

| | | | | | | | | | | |
|------|--|--|--|--|--|--|--|--|--|--|
| ISS | | | | | | | | | | |
| ECO | | | | | | | | | | |
| DATE | | | | | | | | | | |
| CHKD | | | | | | | | | | |

| | | |
|----------|--------|---------------------|
| DATE | 3.6.85 | |
| DRAWN | IL | |
| CHECKED | | TITLE |
| APPROVED | | 4700 HV. PCB. ASSY. |
| DATE | | DRAWING NUMBER |
| | | 400537 |
| | | SHEET |
| | | 3 |
| | | OF |
| | | 6 |

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No. USED Per Assy. |
|------------|-----------------|-------------------------|------------------------|-------------------------|--------------------|
| C9 | 102221 | 220pF 10% 500V CER DISC | ITT | CD10 | 1 |
| C10 | 140048 | 47nF 10% 1k5V POLYPROP | STEATITE | MKP1841 | 1 |
| C11 | 102821 | 820pF 10% 500V CER DISC | ITT | CD10 | 1 |
| C12 | 102332 | 3n3F 20% 500V CER DISC | ITT | CD10 | 1 |
| C13 | 140047 | 33nF 10% 1k5V POLYPROP | STEATITE | MKP1841 | - |
| C14 | 104044 | 680pF 10% 2kV CER DISC | ITT | HD09 | 1 |
| D1 | 200020 | 1A 1k5V FR Si DIODE | MOTOROLA | BY339 | 3 |
| D2 | 200020 | 1A 1k5V FR Si DIODE | MOTOROLA | BY339 | - |
| D3 | 200020 | 1A 1k5V FR Si DIODE | MOTOROLA | BY339 | - |
| D4 | 200020 | 1A 1k5V FR Si DIODE | MOTOROLA | BY339 | - |
| D5 | 200020 | 1A 1k5V FR Si DIODE | MOTOROLA | BY339 | - |
| D6 | 200020 | 1A 1k5V FR Si DIODE | MOTOROLA | BY339 | - |
| D7 | 200020 | 1A 1k5V FR Si DIODE | MOTOROLA | BY339 | - |
| D8 | 200020 | 1A 1k5V FR Si DIODE | MOTOROLA | BY339 | - |
| D9 | 200002 | 1A 50V GP Si DIODE | FAIRCHILD | IN4001 | 1 |
| D10 | 213009 | 15V 5W ZENER | UNITRODE | TVS515 | 1 |
| D11 | 213006 | 5V 5W ZENER | UNITRODE | TVS505 | 2 |
| D12 | 213006 | 5V 5W ZENER | UNITRODE | TVS505 | - |
| D13 | 200020 | 1A 1k5V FR Si DIODE | MOTOROLA | BY339 | - |

NOTES

SEE SHEET 2 FOR LATEST ISSUE

| | | | | | | | | | | |
|------|--|--|--|--|--|--|--|--|--|--|
| ISS | | | | | | | | | | |
| ECO | | | | | | | | | | |
| DATE | | | | | | | | | | |
| CHKD | | | | | | | | | | |

| | | |
|----------|--------|---------------------|
| DATE | 3.6.85 | |
| DRAWN | IL | |
| CHECKED | | TITLE |
| APPROVED | | 4700 HV. PCB. ASSY. |
| DATE | | DRAWING NUMBER |
| | | 400537 |
| | | SHEET |
| | | 3 |
| | | OF |
| | | 6 |

| DESIGNATOR | DATRON PART No | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No | No. USED Per Assy |
|------------|----------------|-----------------------------------|------------------------|------------------------|-------------------|
| Q1 | 250011 | Si PNP TRANSISTOR | NATIONAL | BC327/TO18 | 1 |
| M1 | 290089 | 7 X DARLINGTON DRIVER | SPRAGUE/EXAR | ULN2003A/XR2203CP | 1 |
| M2 | 280039 | QUAD EXCLUSIVE NOR | MOTOROLA | MC14077BCP | 1 |
| M3 | 280023 | QUAD 2 I/P NOR | MOTOROLA | MC14001U BCP | 1 |
| RL1 | 330035 | RELAY 2P 24V | SDS | ST1-24V | 1 |
| RL2 | 330033 | RELAY 2P N/O 5A 2kV | SDS | JC2a DC24V | 3 |
| RL3 | 330033 | RELAY 2P N/O 5A 24V | SDS | JC2a DC24V | - |
| RL4 | 330033 | RELAY 2P N/O 5A 24V | SDS | JC2a DC24V | - |
| RL5 | 330044 | RELAY 2P2W 5A | DATRON | | 1 |
| L1 | | NOT USED | | | - |
| L2 | 370001 | 10 μ H 0.85 Ω RF CHOKE | PLESSEY | 58/10/0011/10 | 3 |
| L3 | 370007-1 | 40mH CHOKE | SIGA | SEE DRG | 1 |
| L4 | 370015-2 | 25.3mH CHOKE | SIGA | SEE DRG | 2 |
| L5 | 370015-2 | 25.3mH CHOKE | SIGA | SEE DRG | - |
| L6 | 370001 | 10 μ H 0.85 Ω RF CHOKE | PLESSEY | 58/10/0011/10 | - |
| L7 | 370001 | 10 μ H 0.85 Ω RF CHOKE | PLESSEY | 58/10/0011/10 | - |

NOTES.

SEE SHEET 2 FOR LATEST ISSUE

| | | | | | | | | | | | | | | | | | | | | |
|------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ISS | | | | | | | | | | | | | | | | | | | | |
| ECD | | | | | | | | | | | | | | | | | | | | |
| DATE | | | | | | | | | | | | | | | | | | | | |
| CHKD | | | | | | | | | | | | | | | | | | | | |

| | | | |
|----------|--------|------------------------|------------|
| DATE | 3.6.85 | datron ELECTRONICS LTD | |
| DRAWN | IL | TITLE 4700 HV PCB ASSY | |
| CHECKED | | | |
| APPROVED | | | |
| DATE | | DRAWING NUMBER 400537 | SHEET OF 6 |



| DESIGNATOR | DATRON PART No | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No | No. USED Per Assy |
|------------|----------------|------------------------------|------------------------|------------------------|-------------------|
| | 400563-3 | CONSTANT I PCB ASSY | | | 1 |
| | 410327-2 | H.V. PCB | | | 1 |
| | 420080-1 | HIGH VOLTAGE LABEL | | | 1 |
| | 450461-3 | H.V. PCB SAFETY SCREEN | DATRON | | 1 |
| | 512999 | 7/0-2 PTFE INS. WHITE WIRE | RS | | A/R |
| | 420112-1 | SSD WARNING LABEL | | SEE DRG | 1 |
| | 420098 | SERIAL NO LABEL | | RS 554-793 | 1 |
| J2, J3, J4 | 604033 | 4WAY .1" PCB PLUG GD.PL | MOLEX | 22-29-2041 | 7 |
| | 611006 | M3x10mm SCREW POZIPAN ST. | ZN.PL. | GKN | 2 |
| | 613029 | M3 WAVY WASHER SS. | | | 2 |
| | 615002 | M3 FULL NUT STEEL ZN.PL. | | | 2 |
| | 613005 | M3 SHAKERPROOF WASHER | ZN.PL. | | 2 |
| | 630243 | GLASS BEAD 24% x 0.8/0 x 1.8 | MAN SOL (PREFORMS) | M53638/3 | 6 |
| | 620007 | TEST POINT TERMINAL | MICROVAR | TYPE C30 | 8 |
| | 630024 | 16SWG STEATITE BEAD | PARK ROYAL PORCELAIN | NO 2 | 8 |
| | 605060 | 14 PIN DIL SOCKET | JERMYN | J23-18014 | 2 |
| | 605061 | 16 PIN DIL SOCKET | JERMYN | J23-18016 | 1 |

NOTES.

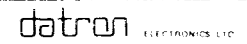
SEE SHEET 2 FOR LATEST ISSUE

| | | | | | | | | | | | | | | | | | | | | |
|------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ISS | | | | | | | | | | | | | | | | | | | | |
| ECD | | | | | | | | | | | | | | | | | | | | |
| DATE | | | | | | | | | | | | | | | | | | | | |
| CHKD | | | | | | | | | | | | | | | | | | | | |

| | | | |
|----------|--------|------------------------|------------|
| DATE | 3.6.85 | datron ELECTRONICS LTD | |
| DRAWN | IL | TITLE 4700 HV PCB ASSY | |
| CHECKED | | | |
| APPROVED | | | |
| DATE | | DRAWING NUMBER 400537 | SHEET OF 6 |

| | | | | | | | | | | | |
|---|----------------|-------------------|--|------------------|------------------------|-----------------------|-----------------------|-------------------------|-----------------------------|------------------|-----|
| DRAWING No 400563 | | CHKD AK | DATE 15.8.85 | ECS AK | | REVISION AK | | ISSUE AK | | ISSUE - REVISION | |
| DESCRIPTION | DRAWING NUMBER | SHEET NUMBER | 1-0 | 2-0 | 2-1 | 2-2 | 2-3 | 3-0 | 3-1 | 3-0 | 3-1 |
| COMPONENT LAYOUT | 480563 | 1 | 1-0 | 2-0 | 2-1 | 2-2 | 2-3 | 3-0 | 3-1 | | |
| SCHEMATIC | 430563 | 1 | 1-0 | 2-0 | | | | 3-0 | | | |
| FUNC TEST PROC. | 460563/FT | ALL | 1-0 | 2-0 | | | | 3-0 | 3-1 | | |
| FUNC TEST TICK LIST | 470563/FT | ALL | 1-0 | 2-0 | | | | 3-0 | 3-1 | | |
| PCB | 410285 | - | 3-0 | 3-0 | | | | 4-0 | | | |
| NOTES <input type="checkbox"/> INDICATES NO CHANGE TO DOCS AT ISSUE LEVEL CHANGE | | |  | | DRN AK | CHKD AK | APPR AK | TITLE 4700 | DRAWING No 400563 | | |
| | | |  | | DATE 15.8.85 | DATE 5/3/86 | DATE 6.3.86 | CONSTANT I ASSY. | | SHEET 1 of 4 | |

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No. USED Per Assy. |
|------------|-----------------|-------------------------|------------------------|-------------------------|--------------------|
| R1 | 000102 | 1K 5% 1/4W CARBON | MULLARD | CR25 | 2 |
| R2 | 005124 | 120K 2% 1/2W MET-OX | ELECTROSIL | TR5 | 6 |
| R3 | 005124 | 120K 2% 1/2W MET-OX | ELECTROSIL | TR5 | - |
| R4 | 005124 | 120K 2% 1/2W MET-OX | ELECTROSIL | TR5 | - |
| R5 | 005124 | 120K 2% 1/2W MET-OX | ELECTROSIL | TR5 | - |
| R6 | 005124 | 120K 2% 1/2W MET-OX | ELECTROSIL | TR5 | - |
| R7 | 005124 | 120K 2% 1/2W MET-OX | ELECTROSIL | TR5 | - |
| R8 | 000105 | 1M 5% 1/4W CARBON | MULLARD | CR25 | 1 |
| R9 | 000104 | 100K 5% 1/4W CARBON | MULLARD | CR25 | 1 |
| R10 | 000470 | 47R 5% 1/4W CARBON | MULLARD | CR25 | 1 |
| R11 | 000102 | 1k 5% 1/4W CARBON | MULLARD | CR25 | - |
| R12 | 000046 | 10R 5% 2 1/4W WIREWOUND | WELWYN | W11 | 1 |
| R13 | 000221 | 220R 5% 1/4W CARBON | MULLARD | CR25 | 1 |
| R14 | | NOT USED | | | - |
| R15 | 000223 | 22k 5% 1/4W CARBON | MULLARD | CR25 | 1 |
| R16 | 000222 | 2k2 5% 1/4W CARBON | MULLARD | CR25 | 1 |
| R17 | 000103 | 10k 5% 1/4W CARBON | MULLARD | CR25 | 1 |
| C1 | 150012 | 100nF 20% 35V DIP TANT | UNION CARBIDE | KR10E35 | 1 |
| C2 | 101103 | 10nF 25% 250V CER DISC | ITT | CD10 | 1 |

| | | | | |
|----------------------------|--|------------------------|---|--|
| NOTES | | DATE 4.10.85 |  | |
| SEE SHEET FOR LATEST ISSUE | | DRAWN L | 4700 CONSTANT CURRENT SOURCE PCB ASSY | |
| | | CHECKED | DRAWING NUMBER 400563 | |
| | | APPROVED | SHEET 2 of 4 | |
| | | DATE | | |


| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No. USED In Assy. |
|------------|-----------------|----------------------------|------------------------|-------------------------|-------------------|
| | 605136 | 0.093" MALE CRIMP TERM.GD. | MOLEX | 02-09-6123 | 5 |
| | 606010 | POLARISING KEY | MOLEX | 15-04-0219 | 4 |
| | 604068 | GWAY 0.093" PLUG | MOLEX | 03-09-2062 | 1 |
| | 606027 | POLARISING PIN | MOLEX | 15-04-0220 | 5 |
| | 611015 | M3x 8mm POZI-CSK STEEL | ZN PL | | 5 |
| | 611081-2 | M5x12mm STEEL SCREW. | | SEE DRAWING | 2 |
| | 613005 | M3 INT SHAKEPROOF | | | 3 |
| | 613009 | 4BA SOLDER TAG BRASS | TIN PL | | 5 |
| | 613013 | M5 FLAT WASHER | | | 2 |
| | 615002 | M3 FULL NUT STEEL | ZN PL | | 3 |
| | 700093 | SWITCH 4P 2P C/O. | ARROW-HART | CTS12 BP4 | 1 |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |

NOTES.

SEE SHEET 1 FOR LATEST ISSUE

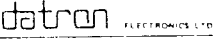
| | | | | | | | | | | | | | | | | | | | | |
|--------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ISS | | | | | | | | | | | | | | | | | | | | |
| E.C.O. | | | | | | | | | | | | | | | | | | | | |
| DATE | | | | | | | | | | | | | | | | | | | | |
| CHKD | | | | | | | | | | | | | | | | | | | | |

| | | | |
|----------|------------|------------------------|--------|
| DATE | 6th MAR 84 | | |
| DRAWN | B. JACKSON | | |
| CHECKED | | TITLE | 4200 |
| APPROVED | | MAINS TRANSFORMER ASSY | |
| DATE | | DRAWING NUMBER | 400541 |
| | | SHEET | 3 |
| | | OF | 3 |

| | | | | |
|--|----------------|---------------------------------------|-----------------------|----------------|
| DRAWING NO. 400651 | | CHK D | 1-0 12162-7-3 86/NO | |
| DATE | | DATE | 1-1 12575 21/4 87/NO | |
| ECO | | ECO | 1-2 2607 23/6 87/NO | |
| REV. HISTORY | | REV. HISTORY | 1-3 2683 10/00 87/NO | |
| ISSUE | | ISSUE | 1-4 3004 23/AUG 88/NO | |
| DESCRIPTION | DRAWING NUMBER | SHEET NUMBER | ISSUE / REVISION | |
| COMP LAYOUT | 400651 | 1 | 1-0 | 1-1 |
| | | | 1-2 | 1-3 |
| NOTES | | | | |
|  | | DATE 22.1.86 | DATE 4.3.86 | DATE 4.3.86 |
| TITLE 4700 LF TRANSFORMER ASSY | | DRAWING NO. 400651 SHEET 1 of 3 | | |

400651

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No USED Per Assy |
|------------|-----------------|-------------------------------|---------------------------|-------------------------|------------------|
| | 300025-2 | L.F. TRANSFORMER | SIGA | | 1 |
| | 450402-2 | 4200 LF. TX MTG. PLATE | | | 1 |
| | 450405-1 | 4200 LF. TX PLATE SUPPT. BAR. | | | 2 |
| | 450408-1 | 4200 CONN. MTG. BRKT. | | | 1 |
| | 540002 | BTC WIRE | | | A/R |
| | 512000 | WIRE 7/2 BLACK PTFE | 1KV TYPE 'C' INSULATION. | | A/R |
| | 512111 | WIRE 7/2 BROWN PTFE | 1KV TYPE 'C' INSULATION. | | A/R |
| | 512220 | WIRE 7/2 RD/BK PTFE | 1KV TYPE 'C' INSULATION. | | A/R |
| | 512330 | WIRE 7/2 OE/BK PTFE | 1KV TYPE 'C' INSULATION. | | A/R |
| | 512333 | WIRE 7/2 ORANGE PTFE | 1KV TYPE 'C' INSULATION. | | A/R |
| | 512444 | WIRE 7/2 YELLOW PTFE | 1KV TYPE 'C' INSULATION. | | A/R |
| | 512555 | WIRE 7/2 GREEN PTFE | 1KV TYPE 'C' INSULATION. | | A/R |
| | 512888 | WIRE 7/2 GREY PTFE | 1KV TYPE 'C' INSULATION. | | A/R |
| | 512999 | WIRE 7/2 WHITE PTFE | 1KV TYPE 'C' INSULATION. | | A/R |
| | 512666 | WIRE 7/2 BLUE PTFE | 1KV TYPE 'C' INSULATION. | | A/R |
| | 512777 | WIRE 7/2 VIOLET PTFE | 1KV TYPE 'C' INSULATION. | | A/R |
| | 560012 | 1 CORE 1/0.64 CO-AX | | | A/R |
| | 590003 | SLEEVE HEATSHRINK $\phi 6.4$ | RS OR HELLERMANN ELECTRIC | 399-524 OR LVR 64 | A/R |
| | 590006 | SLEEVE HEATSHRINK $\phi 2.4$ | RS OR HELLERMANN ELECTRIC | 399-495 OR LVR 24 | A/R |
| | 590032 | SLEEVE HEATSHRINK $\phi 4.8$ | | | A/R |
| | 512222 | WIRE 7/2 RED PTFE | 1KV TYPE 'C' INSULATION. | | A/R |
| | 605051 | 4WAY 0.1" HOUSING | MOLEX | 22-01-2045 | 1 |
| | 605052 | 8WAY 0.1" HOUSING | MOLEX | 22-01-2085 | 1 |

| | | | | | |
|---------------------------|------|------|------|-----------------|---|
| NOTES | | | | DATE 22.1.86 |  |
| SHEET 1 OF 3 LATEST ISSUE | | | | DATE 22.1.86 | TITLE 4700 LF TRANSFORMER ASSY |
| 1 | 2 | 3 | 4 | | DRAWING NUMBER 400651 |
| 22 244 | 1394 | 1030 | 1031 | | SHEET 2 of 3 |
| MD | MD | MD | MD | | |


| DESIGNATOR | DATRON PART No | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No | No. USED Per Assy. |
|------------|----------------|--------------------------|--------------------------|------------------------|--------------------|
| | G05057 | CRIMP TERMINAL GD PL | MOLEX | 4089-GL | 4 |
| | G05116-2 | 32x32WAY PCB EDGE SKT. | | SEE DRG. A4. | 1 |
| | G11007 | M3x6mm POZI-CSK STEEL | ZN PL | | 7 |
| | G11016 | M3x 8mm POZI-PAN STEEL | ZN PL | | 3 |
| | G11081-2 | M5X 12mm TUF LOK HEX HD. | | SEE DRG- | 2 |
| | G13005 | M3 INTERNAL SHAKE PROOF | | | 4 |
| | G13007 | M3 WASHER STEEL | ZN PL | | 1 |
| | G13009 | 4BA SOLDER TAG BRASS | TIN PL | | 1 |
| | G13028 | M5 INTERNAL SHAKE PROOF | | | 2 |
| | G15002 | M3 FULL NUT STEEL | ZN PL | | 1 |
| | G30004 | P CLIP ϕ 6.4mm | SES | CNG | 1 |
| | G30170 | PCB GUIDE | RICHCO | RCG2 | 2 |
| | 900009 | LOCKING COMPOUND | LOCTITE | 222 | A/R |
| | 512992 | WIRE 7/2 WH/RED PTFE | 1KV TYPE 'C' INSULATION. | | A/R |
| | 513001 | WIRE 7/2 PINK PTFE | 1KV TYPE 'C' INSULATION. | | A/R |
| | 512225 | WIRE 7/2 RED/GRN PTFE | 1KV TYPE 'C' INSULATION. | | A/R |
| | 512999 | WIRE 7/2 WHITE PTFE | 1KV TYPE 'C' INSULATION. | | A/R |
| | 512226 | WIRE 7/2 RED/BLUE PTFE | 1KV TYPE 'C' INSULATION. | | A/R |

NOTES.

SEE SHEET 1 FOR LATEST ISSUE

| | | | | | | | | | | | | | | | | | | | |
|-------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ISS | | | | | | | | | | | | | | | | | | | |
| EC'D | | | | | | | | | | | | | | | | | | | |
| DATE | | | | | | | | | | | | | | | | | | | |
| CHK'D | | | | | | | | | | | | | | | | | | | |

| | | | |
|----------|-----------|------------------------|--------|
| DATE | 22. 1. 86 | datron ELECTRONICS LTD | |
| DRAWN | JL | TITLE | 4700 |
| CHECKED | | L.F. TRANSFORMER ASSY | |
| APPROVED | | DRAWING NUMBER | 400651 |
| DATE | | SHEET | 3 OF 3 |

| DRAWING No. | | CHKD | DATE | ECO | REVISION | ISSUE | | |
|-----------------------|----------------|--|------------------|--|--------------------------------------|------------------|-------------------------------|---------------------------------------|
| 400578 | | | | | | | | |
| HI WA | | | | | | | | |
| | | 4.0 | 1988.3.7.95 MD | | | | | |
| | | 4.1 | 1993.19.7.86 R | | | | | |
| | | 4.1 | 2775.6.5.88 LC | | | | | |
| DESCRIPTION | DRAWING NUMBER | SHEET NUMBER | ISSUE - REVISION | | | | | |
| COMP LAYOUT | 480578 | 1 | 4.0 | 4.1 | | | | |
| FUNCTIONAL TEST PROC. | 460578/FT | 1 | 4.0 | 4.1 | | | | |
| FUNCT. TEST TICK LIST | 470578/FT | 1 | 4.0 | 4.1 | | | | |
| NOTES | |  | | DNN B. JACKSON DATE 3-7-85 | CHKD MJD DATE 9.7.85 | APPD DATE | TITLE 4200. HF. TX ASSY | DRAWING No. 400578 SHEET 1 OF 3 |

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No. USED Per Assy |
|------------|-----------------|------------------------|------------------------|-------------------------|-------------------|
| R1 | 008042 | GRB 5% SW WIREWOUND | WELWYN | W 23 | 1 |
| | 300026-2 | HF TRANSFORMER | SIGA | SEE DRG. | 1 |
| | 410256-6 | HF TX MOUNTING PCB. | | | 1 |
| | 512222 | 7/0.2 PTFE INSUL. WIRE | RED | | 0.35M |
| | 512666 | 7/0.2 PTFE INSUL. WIRE | BLUE | | 0.35M |
| | 512000 | 7/0.2 PTFE INSUL. WIRE | BLACK | | 0.26M |
| | 512111 | 7/0.2 PTFE INSUL. WIRE | BROWN | | 0.31M |
| | 512444 | 7/0.2 PTFE INSUL. WIRE | YELLOW | | 0.25M |
| | 512999 | 7/0.2 PTFE INSUL. WIRE | WHITE | | 0.21M |
| | 590001 | SLEEVING H15x20 BLACK | | | 2 |
| | 590005 | SLEEVING H20x20 BLACK | | | 3 |
| | 590063 | 295mm CABLE TIE | PANDUIT | PLT 31 | 1 |
| | 605051 | 4WAY 0.1" HOUSING | MOLEX | 22-01-2045 | 1 |
| | 605053 | 12WAY 0.1" HOUSING | MOLEX | 22-01-2125 | 1 |
| | 605057 | CRIMP TERMINAL GD. PL | MOLEX | 4809-GL | 6 |
| | 611055 | M4x40mm SLOT-PAN BRASS | Ni PL | | 1 |
| | 612029-1 | M3x12mm STANDOFF | HARWIN | SEE DRG G12***. | 4 |

NOTES

SEE SHEET 1 FOR PARTS LIST

| | | | |
|-----------|-----------|---------|--------|
| 1 | 2 | 3 | 4 |
| RELEASED | 1757 | 1828 | 1934 |
| 28 SEP 84 | 15 NOV 84 | 25 1 85 | 4 6 85 |
| MD | MD | K. | RP |

DATE: 26 APR 84

DRAWN BY: B. JACKSON


CHECKED BY: MJD

DATE: 28.9.84

datron ELECTRONICS LTD

TITLE: 4200 HF TRANSFORMER ASSY

DRAWING No.: 400578 SHEET 2 OF 3

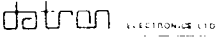
| | | | | | |
|-----------------------|--------|---|---|--|----------|
| DRAWING No. 400604 | | CHKD DATE | 1-0 2162 26 2 86 1-1 2279 10 6 86 1-2 2333 24 7 86 1-2 2334 30 9 86 1-3 2469 12 26 86 1-3 2539 16 3 87 1-4 2591 11 6 87 1-5 2614 10 7 87 1-6 2623 10 7 87 1-7 2641 19 8 87 2-0 2858 16 6 88 2-1 2955 20 7 88 2-2 2983 27 7 88 2-3 3009 26 8 88 | | |
| DESCRIPTION | | DRAWING NUMBER | REVISION NUMBER | ISSUE | REVISION |
| COMPONENT LAYOUT | 480604 | 1 | 1-0 1-1 | | |
| COMPONENT LAYOUT | 480604 | 2 | 1-1 1-2 1-3 1-4 1-5 1-6 1-7 1-8 1-9 | | |
| L.P. | 400604 | ALL | | | |
| SCHEMATIC | 430604 | 1 | 1-0 1-1 1-2 1-3 1-4 1-5 1-6 1-7 1-8 1-9 | | |
| SCHEMATIC | 430604 | 2 | | | |
| SCHEMATIC | 430604 | 3 | | | |
| SCHEMATIC | 430604 | 4 | | | |
| SCHEMATIC | 430604 | 5 | | | |
| PCB | 410361 | | 1-0 | | |
| PCB | 410348 | | 2-0 | | |
| NOTES | | DENOTES NO CHANGE TO DOC'S AT ISSUE LEVEL CHANGE. | |  DYN DATE 13.8.85 CHKD A.K. COGGIN DATE 6/3/86 APPD DATE 7.3.86 TITLE 4700 MOTHER PCB. ASSY. DRAWING No. 400604 SHEET 1 OF 10 | |

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No. USED Per Assy |
|------------|-----------------|--------------------|------------------------|-------------------------|-------------------|
| R1 | 001822 | 8k2 5% 1/2W CARBON | MULLARD | CR37 | 24 |
| R2 | 001822 | 8k2 5% 1/2W CARBON | MULLARD | CR37 | - |
| R3 | 001822 | 8k2 5% 1/2W CARBON | MULLARD | CR37 | - |
| R4 | 001822 | 8k2 5% 1/2W CARBON | MULLARD | CR37 | - |
| R5 | 001822 | 8k2 5% 1/2W CARBON | MULLARD | CR37 | - |
| R6 | 001822 | 8k2 5% 1/2W CARBON | MULLARD | CR37 | - |
| R7 | 001822 | 8k2 5% 1/2W CARBON | MULLARD | CR37 | - |
| R8 | 001822 | 8k2 5% 1/2W CARBON | MULLARD | CR37 | - |
| R9 | 001822 | 8k2 5% 1/2W CARBON | MULLARD | CR37 | - |
| R10 | 001822 | 8k2 5% 1/2W CARBON | MULLARD | CR37 | - |
| R11 | 001822 | 8k2 5% 1/2W CARBON | MULLARD | CR37 | - |
| R12 | 001822 | 8k2 5% 1/2W CARBON | MULLARD | CR37 | - |
| R13 | 001822 | 8k2 5% 1/2W CARBON | MULLARD | CR37 | - |
| R14 | 001822 | 8k2 5% 1/2W CARBON | MULLARD | CR37 | - |
| R15 | 001822 | 8k2 5% 1/2W CARBON | MULLARD | CR37 | - |
| R16 | 001822 | 8k2 5% 1/2W CARBON | MULLARD | CR37 | - |
| R17 | 001822 | 8k2 5% 1/2W CARBON | MULLARD | CR37 | - |
| R18 | 001822 | 8k2 5% 1/2W CARBON | MULLARD | CR37 | - |
| R19 | 001822 | 8k2 5% 1/2W CARBON | MULLARD | CR37 | - |
| R20 | 001822 | 8k2 5% 1/2W CARBON | MULLARD | CR37 | - |
| R21 | 001822 | 8k2 5% 1/2W CARBON | MULLARD | CR37 | - |
| R22 | 001822 | 8k2 5% 1/2W CARBON | MULLARD | CR37 | - |
| R23 | 001822 | 8k2 5% 1/2W CARBON | MULLARD | CR37 | - |

NOTES

SEE SHEET 1 FOR LAYER 1000

| | | | | | | | |
|------|------|------|------|------|------|------|------|
| DATE | DATE | DATE | DATE | DATE | DATE | DATE | DATE |
| | | | | | | | |



4700 MOTHER PCB ASSY

400604 2 10

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No. USED Per Assy |
|------------|-----------------|----------------------|------------------------|-------------------------|-------------------|
| R24 | 001822 | 8k2 5% 1/2W CARBON | MULLARD | CR37 | - |
| R25 | 063205 | 2M POT 3/8 SQ CERMET | BECKMAN | 72P | 1 |
| R26 | 000104 | 100k 5% 1/3W CARBON | MULLARD | CR25 | 1 |
| R27 | 000472 | 4k7 5% 1/3W CARBON | MULLARD | CR25 | 1 |
| R28 | 000103 | 10k 5% 1/3W CARBON | MULLARD | CR25 | 33 |
| R29 | 000103 | 10k 5% 1/3W CARBON | MULLARD | CR25 | - |
| R30 | 000103 | 10k 5% 1/3W CARBON | MULLARD | CR25 | - |
| R31 | 000103 | 10k 5% 1/3W CARBON | MULLARD | CR25 | - |
| R32 | 000103 | 10k 5% 1/3W CARBON | MULLARD | CR25 | - |
| R33 | 000103 | 10k 5% 1/3W CARBON | MULLARD | CR25 | - |
| R34 | 000103 | 10k 5% 1/3W CARBON | MULLARD | CR25 | - |
| R35 | 000102 | 1k 5% 1/3W CARBON | MULLARD | CR25 | 1 |
| R36 | 000103 | 10k 5% 1/3W CARBON | MULLARD | CR25 | - |
| R37 | 000103 | 10k 5% 1/3W CARBON | MULLARD | CR25 | - |
| R38 | 000103 | 10k 5% 1/3W CARBON | MULLARD | CR25 | - |
| R39 | 000103 | 10k 5% 1/3W CARBON | MULLARD | CR25 | - |
| R40 | 000103 | 10k 5% 1/3W CARBON | MULLARD | CR25 | - |
| R41 | 000103 | 10k 5% 1/3W CARBON | MULLARD | CR25 | - |
| R42 | 000103 | 10k 5% 1/3W CARBON | MULLARD | CR25 | - |
| R43 | 000103 | 10k 5% 1/3W CARBON | MULLARD | CR25 | - |
| R44 | 000473 | 47k 5% 1/3W CARBON | MULLARD | CR25 | 8 |
| R45 | 000103 | 10k 5% 1/3W CARBON | MULLARD | CR25 | - |
| R46 | 000103 | 10k 5% 1/3W CARBON | MULLARD | CR25 | - |

NOTES.

SEE SHEET 2 FOR LATEST ISSUE

| | | | | | | | | | | | |
|--------|--|--|--|--|--|--|--|--|--|--|--|
| ISS | | | | | | | | | | | |
| E.C.O. | | | | | | | | | | | |
| DATE | | | | | | | | | | | |
| CHKD | | | | | | | | | | | |

| | | |
|----------------|----|----------------------------------|
| DATE | | datron ELECTRONICS LTD |
| DRAWN | JL | |
| CHECKED | | |
| APPROVED | | |
| DATE | | |
| TITLE | | 4700 MOTHER PCB ASSY |
| DRAWING NUMBER | | 400604 |
| SHEET | | 3 OF 10 |

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No. USED Per Assy |
|------------|-----------------|---------------------|------------------------|-------------------------|-------------------|
| R47 | 000103 | 10k 5% 1/3W CARBON | MULLARD | CR25 | - |
| R48 | | NOT USED | | | - |
| R49 | | NOT USED | | | - |
| R50 | 000820 | 82R 5% 1/3W CARBON | MULLARD | CR25 | 2 |
| R51 | 000820 | 82R 5% 1/3W CARBON | MULLARD | CR25 | - |
| R52 | 000101 | 100R 5% 1/3W CARBON | MULLARD | CR25 | 1 |
| R53 | | NOT USED | | | - |
| R54 | | NOT USED | | | - |
| R55 | | NOT USED | | | - |
| R56 | | NOT USED | | | - |
| R57 | | NOT USED | | | - |
| R58 | 000103 | 10k 5% 1/3W CARBON | MULLARD | CR25 | - |
| R59 | 000103 | 10k 5% 1/3W CARBON | MULLARD | CR25 | - |
| R60 | 000103 | 10k 5% 1/3W CARBON | MULLARD | CR25 | - |
| R61 | 000103 | 10k 5% 1/3W CARBON | MULLARD | CR25 | - |
| R62 | | NOT USED | | | - |
| R63 | 000103 | 10k 5% 1/3W CARBON | MULLARD | CR25 | - |
| R64 | 000103 | 10k 5% 1/3W CARBON | MULLARD | CR25 | - |
| R65 | 000103 | 10k 5% 1/3W CARBON | MULLARD | CR25 | - |
| R66 | | NOT USED | | | - |
| R67 | 000103 | 10k 5% 1/3W CARBON | MULLARD | CR25 | - |
| R68 | 000103 | 10k 5% 1/3W CARBON | MULLARD | CR25 | - |
| R69 | 000473 | 47k 5% 1/3W CARBON | MULLARD | CR25 | - |

NOTES.

SEE SHEET 2 FOR LATEST ISSUE

| | | | | | | | | | | | |
|--------|--|--|--|--|--|--|--|--|--|--|--|
| ISS | | | | | | | | | | | |
| E.C.O. | | | | | | | | | | | |
| DATE | | | | | | | | | | | |
| CHKD | | | | | | | | | | | |

| | | |
|----------------|----|----------------------------------|
| DATE | | datron ELECTRONICS LTD |
| DRAWN | JL | |
| CHECKED | | |
| APPROVED | | |
| DATE | | |
| TITLE | | 4700 MOTHER PCB ASSY |
| DRAWING NUMBER | | 400604 |
| SHEET | | 4 OF 10 |

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No. USED Per Assy. |
|---------------|-----------------|------------------------|------------------------|-------------------------|--------------------|
| C12 | 104032 | 220pF 10% 2KV CER DISC | ITT | HD09 | 1 |
| C13 | 102102 | 1nF 10% 500V CER DISC | ITT | CD10 | 3 |
| C14 | 102102 | 1nF 10% 500V CER DISC | ITT | CD10 | - |
| C15 | 102102 | 1nF 10% 500V CER DISC | ITT | CD10 | - |
| C16 | 140090 | 100n 20% 400V POLYPROP | ROEDERSTEIN | MKP 1844-410-4000 | 3 |
| C17 | 140090 | 100n 20% 400V POLYPROP | ROEDERSTEIN | MKP 1844-410-4000 | - |
| C18 | | NOT FITTED | | | |
| C19 | | NOT FITTED | | | |
| C20 | | NOT FITTED | | | |
| CN1 | 104033 | 1nF x7 20% 50V CAP NWK | SPRAGUE | 470C7X7R102M5DG | 3 |
| CN2 | 104033 | 1nF x7 20% 50V CAP NWK | SPRAGUE | 470C7X7R102M5DG | - |
| CN3 | 104033 | 1nF x7 20% 50V CAP NWK | SPRAGUE | 470C7X7R102M5DG | - |
| CN4, CN5, CN6 | | NOT FITTED | | | |
| CN7, CN8 | | NOT FITTED | | | |
| D1 | 200002 | 1A 50V GP Si DIODE | FAIRCHILD | IN4001 | 2 |
| D2 | 200002 | 1A 50V GP Si DIODE | FAIRCHILD | IN4001 | - |
| D3 | 200024 | 3A 1k3V GP Si DIODE | MOTOROLA | BY255 | 8 |
| D4 | 200024 | 3A 1k3V GP Si DIODE | MOTOROLA | BY255 | - |
| D5 | 200024 | 3A 1k3V GP Si DIODE | MOTOROLA | BY255 | - |
| D6 | 200024 | 3A 1k3V GP Si DIODE | MOTOROLA | BY255 | - |
| D7-D10 | 200024 | 3A 1k3V GP Si DIODE | MOTOROLA | BY255 | - |

NOTES

SEE SHEET 2 FOR LATEST ISSUE

| | | | | | | | | | |
|------|--|--|--|--|--|--|--|--|--|
| ISS | | | | | | | | | |
| ECO | | | | | | | | | |
| DATE | | | | | | | | | |
| CHKD | | | | | | | | | |

| | |
|----------|--|
| DATE | |
| DRAWN | |
| CHECKED | |
| APPROVED | |
| DATE | |

| | |
|------------------------|---------|
| datron ELECTRONICS LTD | |
| TITLE | |
| 4700 MOTHER PCB ASSY | |
| DRAWING NUMBER | 400604 |
| SHEET | 7 OF 10 |

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No. USED Per Assy. |
|------------------------|-----------------|------------------------------|------------------------|-------------------------|--------------------|
| W1 | 209014 | 1A5 400V BRIDGE RECT | MICRO-ELECTRONICS | W004 | 1 |
| Q1 | 250004 | Si PNP TRANSISTOR | NATIONAL | 2N3906/1092 | 1 |
| RL1 | 330038 | RELAY 2P N/O 2P N/C | SDS | S2-L-6V | 1 |
| RL2, RL3 | 330030 | RELAY 4P N/O | SDS | S4-24V | 2 |
| RL4 | 330029 | RELAY 2P2W | SDS | DS2E-DC24V | 1 |
| L1 | 370024-1 | COMMON MODE CHOKE 5W | SIGA | SEE DRG | 1 |
| L2, L3 | 370014 | 8uH 3A RF CHOKE | ERO | F1756-008-301 | 2 |
| L4 | 370001 | 10uH 0.85u RF CHOKE | PLESSEY | 58/10/0011/10 | 2 |
| L5 | 370001 | 10uH 0.85u RF CHOKE | PLESSEY | 58/10/0011/10 | - |
| | 410361-1 | DIODE LINK BOARD | | | 1 |
| J4, J5, J7, J8, J9 | 605090-2 | 6+6 WAY PCB EDGE SKT | SEE DRG | | 8 |
| | 410348-4 | PCB | | | 1 |
| | 512999 | 7/2 WHITE PTFE INS 1kV rms | | TO BSG210 TYPE C | A/R |
| | 560002 | 7/34AWG CU. COV. STEEL CO-AX | | | A/R |
| | 590031 | HEATSHRINK SLEEVE ø 3.2 | | | A/R |
| J19, J31, J32, J33 | 604042 | 4WAY 15G' PLUG GD PL | MOLEX | 09-72-2041 | 6 |
| J2, J3, J4, J6, J7 | 605087-2 | 24+24 WAY PCB EDGE SKT | SEE DRG | | 13 |
| J3, J5, J8, J9 | 605088-2 | 18+18 WAY PCB EDGE SKT | SEE DRG | | 6 |
| J2, J4, J6, J7, J8, J9 | 605089-2 | 12+12 WAY PCB EDGE SKT | SEE DRG | | 7 |
| J5, J7, J8, J9 | 605091-2 | 6+6 WAY PCB EDGE SKT | SEE DRG | | 9 |
| J7, J8, J9 | 605092-2 | 3+3 WAY PCB EDGE SKT | SEE DRG | | 5 |
| J30 | 605114-2 | 12+12 WAY PCB EDGE SKT | SEE DRG | | 1 |

NOTES

SEE SHEET 2 FOR LATEST ISSUE

| | | | | | | | | | |
|------|--|--|--|--|--|--|--|--|--|
| ISS | | | | | | | | | |
| ECO | | | | | | | | | |
| DATE | | | | | | | | | |
| CHKD | | | | | | | | | |

| | |
|----------|--|
| DATE | |
| DRAWN | |
| CHECKED | |
| APPROVED | |
| DATE | |

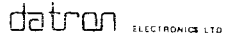
| | |
|------------------------|---------|
| datron ELECTRONICS LTD | |
| TITLE | |
| 4700 MOTHER PCB ASSY | |
| DRAWING NUMBER | 400604 |
| SHEET | 8 OF 10 |

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | Qty. USED Per Assy. |
|------------|-----------------|----------------------------------|------------------------|-------------------------|---------------------|
| | 612004-1 | M3 x 4mm STANDOFF | DATRON | SEE DRG | 12 |
| | 612027-1 | M3 x 8mm STANDOFF | DATRON | SEE DRG | 10 |
| | 617010 | NYLATCH PLUNGER 3/16" | HARTWELL CORP | HN3P-32-4-1 | 20 |
| | 617011 | NYLATCH GROMMET 3/16" | HARTWELL CORP | HN3G-32-1 | 20 |
| J26 | 620005 | CLOVERLEAF PTFE INSUL. | SEAELECTRO | FTE1SP59 | 5 |
| | 620006 | SOLDER TURRET | HARWIN | H9001-01 | 86 |
| | 620007 | TEST POINT TERMINAL | MICROVAR | TYPE C30 | 9 |
| | 630036 | STEATITE BEAD 18 SWG | PARK ROYAL PORCELAIN | Nº 1 (SMALL) | 4 |
| F1 | 920116 | FUSE 1A 250V 20mm SLO-B | BELLING LEE | L2080A/1 | 2 |
| F2 | 920116 | FUSE 1A 250V 20mm SLO-B | BELLING LEE | L2080A/1 | - |
| F3 | 920125 | FUSE 2.5A 125V 7mm | LITTLEFUSE | 275 02.5 | 2 |
| F4 | 920125 | FUSE 2.5A 125V 7mm | LITTLEFUSE | 275 02.5 | - |
| | 920126 | FUSE HOLDER 20mm PCB | BELLING LEE | L1426 | 2 |
| J1 | 605111 | 24 + 24 WAY .1" PCB SKT | AMP | 2-141592-4 | 3 |
| | 612024-1 | M3 X 12.7mm STANDOFF | DATRON | SEE DRG | 1 |
| | 630024 | STEATITE BEAD 16 SWG | PARK ROYAL PORCELAIN | Nº 2 (LARGE) | 4 |
| | 512333 | 7/0.2 PTFE INSULATED ORANGE WIRE | WIRE | | A/R |
| | 512444 | 7/0.2 PTFE INSULATED YELLOW WIRE | WIRE | | A/R |
| | 512000 | 7/0.2 PTFE INSULATED BLACK WIRE | WIRE | | A/R |
| | 512111 | 7/0.2 PTFE INSULATED BROWN WIRE | WIRE | | A/R |
| | 512222 | 7/0.2 PTFE INSULATED RED WIRE | WIRE | | A/R |

NOTES

SEE SHEET 2 FOR LATEST ISSUE

| | | | | | | | | | | | | | | | | | | | | |
|------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ISS | | | | | | | | | | | | | | | | | | | | |
| ECO | | | | | | | | | | | | | | | | | | | | |
| DATE | | | | | | | | | | | | | | | | | | | | |
| CHKD | | | | | | | | | | | | | | | | | | | | |


| | | |
|----------|----|---|
| DATE | |  |
| DRAWN | /L | |
| CHECKED | | TITLE |
| APPROVED | | 4700 MOTHER PCB ASSY |
| DATE | | DRAWING NUMBER |
| | | 400604 |
| | | SHEET |
| | | 9 OF 10 |

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | Qty. USED Per Assy. |
|------------|-----------------|--------------------------------|-------------------------|-------------------------|---------------------|
| | 512666 | 7/0.2 PTFE INSULATED BLUE WIRE | WIRE | | A/R |
| | 512777 | 7/0.2 PTFE INSULATED VID WIRE | WIRE | | A/R |
| | 611016 | M3 x 8mm POZI-PAN STEEL | ZN PL | | 1 |
| | 613005 | M3 INT. SHAKEPROOF | | | 1 |
| | 613029 | M3 WAVEY WASHER SS | | | 1 |
| | 613019 | M3 LARGE WASHER STEEL | ZN PL | | 1 |
| | 615002 | M3 FULL NUT STEEL ZN PL | | | 1 |
| | 590001 | SLEEVE MAX CABLE Ø3 | HELLERMANN ELECTRIC | H15 x 20mm BLK HELSYN | 2 |
| | 620003 | SOLDER PIN | HARWIN | H210SA01 | 2 |
| | 630250 | CABLE CLIP | RICHCO | SFCC 4A-01 | 3 |
| | 590074 | SOLDER SLEEVE Ø 3.0 | RAYFAST | CWT-3 | 2 |
| | 630243 | GLASS BEAD | MAN SOL (PREFORMS) LTD. | M5363B/3 | 4 |
| | 630270 | CABLE TIE MTG. BLOCK | PANDUIT | TMEH-S8-0 | 1 |
| | 630271 | HEAVY DUTY CABLE TIE | PANDUIT | PRT2EH | 1 |

NOTES

SEE SHEET 2 FOR LATEST ISSUE


| | | | | | | | | | | | | | | | | | | | | |
|------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ISS | | | | | | | | | | | | | | | | | | | | |
| ECO | | | | | | | | | | | | | | | | | | | | |
| DATE | | | | | | | | | | | | | | | | | | | | |
| CHKD | | | | | | | | | | | | | | | | | | | | |

| | | |
|----------|----|---|
| DATE | |  |
| DRAWN | /L | |
| CHECKED | | TITLE |
| APPROVED | | 4700 MOTHER PCB ASSY |
| DATE | | DRAWING NUMBER |
| | | 400604 |
| | | SHEET |
| | | 10 OF 10 |

| | | | | | |
|--|-----------------|-------------------------|----------------|---|--|
| Doc No. 400830 | | DOCUMENT LIST. DI/wm | | 1.0 2858 8.6.88 1.1 3023 27.10.88 1.2 3227 18FE88 | |
| EX-DESCRIPTION | QUANTITY NUMBER | SHEET 1 OF 2 | DATE / VERSION | | |
| 4700 INTERCONNECTION PCB | 400830 ALL | 1.0 | 1.0 | 1.1 | 1.2 |
| 480830 | 1 | 1.0 | 1.1 | 1.1 | 1.2 |
| 430830 | 1 | 1.0 | 1.0 | | |
| 410424 | ALL | C | 1.0 | | |
| <input type="checkbox"/> DENOTES NO CHANGE TO EXCS AT ISSUE LEVEL CHANGE | | | | DATE 25.MAY.88 BY B.S.J. CHECKED A.S. APPROVED DATE 20 JUN 88 | TITLE 4700 INTERCONNECTION PCB DRAWING NO. 400830 SHEET 1 OF 2 |

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No. USED Per Assy. |
|------------|-----------------|---------------------------------|------------------------|-------------------------|--------------------|
| | 410424-1 | PCB | | | 1 |
| | 450540-1 | CONNECTOR SUPPT. BRACKET | | | 1 |
| | 450296-1 | EARTH SCREEN | | | 1 |
| Q1 | 101103 | 10K 25% 250V CER DISC | ITT | CD10 | 1 |
| R3 | 604033 | 4 CCT POLARISING WAFER | MOLEX | 22-29-2041 GOLD | 1 |
| J1, J2 | 605002 | 16 WAY DIL SOCKET | CA | CA-105-1050 | 2 |
| J27 | 605085 | 24 WAY PCB MNT RECEPTACLE | AMPHENOL | 57-20240-8 | 1 |
| | 612001 | M3X6 POZIFAN SCREW | GKN | ZINC PLATED | 2 |
| | 612004 | M3X4 STANDOFF 1/16 PCB | HARWIN | CS 2110-B | 2 |
| | 612026-1 | M3X6 STANDOFF 1/16 PCB | | SEE DRG. | 2 |
| | 613023 | M3 CRINKLE WASHER | | | 2 |
| S1 | 700114 | SWITCH 6X1P. DIL | A.B. | 706-00651 | 1 |
| S2 | 700060 | SP3P SLIDE PCB MNT | ALCO | SLS-131-PC | 1 |
| S33 | 700061 | EPDT SLIDE PCB MNT | ALCO | SLS-121-PC | 1 |
| | 611003 | STANDOFF 3-3 CLEAR X GIMM BRASS | HARWIN | CS 2117-A | 2 |
| | 611007 | M3X6mm POZI-C5K SCREW | ZN. PL. | | 2 |

| | | | | |
|------------------------------|---------|----------------|-------------------------------------|--|
| NOTES. | | DATE 25.MAY.88 | datron ELECTRONICS LTD | |
| SEE SHEET 1 FOR LATEST ISSUE | | BY B.S.JACKSON | TITLE 4700 INTERCONNECTION PCB ASSY | |
| ISS 1 | 2 | CHECKED A.S. | DRAWING NUMBER 400830 | |
| DATE 5-8-81 | 25-3-82 | APPROVED | SHEET 2 OF 2 | |
| ISS 1 | 2 | DATE | | |

| | | | | | | | | |
|----------------------|----------------|--|------------------|---|--|------------------------------|------------------------------------|---------------------------------------|
| DRAWING NO 400640 | | CH/D | | | | | | |
| DATE | | 1.0 2162 25286 R/S | | | | | | |
| ECO | | 1.1 2301 18766 R/S | | | | | | |
| REVISION | | 1.2 2324 24786 R/S | | | | | | |
| ISSUE | | | | | | | | |
| DESCRIPTION | DRAWING NUMBER | SHEET NUMBER | ISSUE - REVISION | | | | | |
| COMP LAYOUT | 480640 | 1 | 1.0 | 1.1 1.2 | | | | |
| SCHEMATIC | 430640 | 1 | 1.0 | | | | | |
| PCB | 410309 | - | 5.0 | 6.0 | | | | |
| NOTES | |  | | DRN B.S. JACKSON DATE 12 FEB. 86 | CH/D A.K. COGGAN DATE 25/2/86 | APP'D 27 DATE 33.86 | TITLE 4700 TERMINAL PCB ASSY | DRAWING No. 400640 SHEET 1 OF 3 |

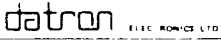
400640

| SIGNATOR | DATRON PART No | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No | No USED Per Assy |
|----------|----------------|-------------------------|------------------------|------------------------|------------------|
| 1 | 120037 | 330pF 20% 400V POLYCARB | WIMA | FKC3 | 1 |
| 2 | 104037 | 22pF 10% 2KV CER DISC | STC | HD10 | 2 |
| 3 | 104037 | 22pF 10% 2KV CER DISC | STC | HD10 | - |
| 4 | 104032 | 220pF 10% 2KV CER DISC | STC | HD10 | 3 |
| 5 | 104032 | 220pF 10% 2KV CER DISC | STC | HD10 | - |
| 6 | 104032 | 220pF 10% 2KV CER DISC | STC | HD10 | - |
| 1 | 370027 | 47µH RF CHOKE | SIGMA | SC30-10-2533-10 | 2 |
| 2 | 370027 | 47µH RF CHOKE | SIGMA | SC30-10-2533-10 | - |
| L1 | 330029 | RELAY 2P2W | SDS | DS2E DC 24V | - |
| | 400576-2 | FRONT OUTPUT CABLE ASSY | | | 2 |
| B1 | 920181 | FERRITE BEAD | MULLARD | FX4029 | 2 |
| B2 | 920181 | FERRITE BEAD | MULLARD | FX4029 | - |
| B3 | 920145 | FERRITE BEAD | MULLARD | FX4026 | 4 |
| B4 | 920145 | FERRITE BEAD | MULLARD | FX4026 | - |
| B5 | 920145 | FERRITE BEAD | MULLARD | FX4026 | - |
| B6 | 920145 | FERRITE BEAD | MULLARD | FX4026 | - |
| | 410309 | P.C.B. | | | 1 |
| | 450269-1 | TERMINAL PLATE | DATRON | SEE DRAWING A4 | 1 |
| | 540002 | 22 SWG TINNED CU WIRE | | | A/R |
| | 590032 | HEATSHRINK SLEEVING | 4 BØ | | A/R |
| | 620003 | SOLDER PIN | HARWIN | H2105A01 | 13 |

NOTES

SEE SHEET 2 FOR LATEST ISSUE



| | |
|----------------------------------|---|
| DATE 12 FEB 86 |  |
| CHECKED B.S. JACKSON | |
| APPROVED | |
| DATE | |
| TITLE TERMINAL BOARD ASSEMBLY | DRAWING NUMBER 400640 |
| SHEET 2 OF 3 | |


| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No. USED Per Assy. |
|------------|-----------------|-------------------------------|------------------------|-------------------------|--------------------|
| | 400686-1 | SAFETY TERMINAL ASSY. BLACK | DATRON | SEE DRAWING A4 | 1 |
| | 400687-1 | SAFETY TERMINAL ASSY. RED | DATRON | SEE DRAWING A4 | 1 |
| | 400688-1 | SAFETY TERMINAL ASSY. BRN | DATRON | SEE DRAWING A4 | 1 |
| | 400689-1 | SAFETY TERMINAL ASSY. BLU. | DATRON | SEE DRAWING A4 | 1 |
| | 400690-1 | SAFETY TERMINAL ASSY. WHI | DATRON | SEE DRAWING A4 | 1 |
| | 400691-1 | SAFETY TERMINAL ASSY. GRN. | DATRON | SEE DRAWING A4 | 1 |
| | 613009 | M3 SOLDER TAG. | | | 1 |
| | 613021 | M4 SHAKEPROOF WASHER. | | | 12 |
| | 613020 | M4 WASHER STEEL | ZN PL | | 6 |
| | 613039 | M2 SOLDER TAG. | ROSS COURTNEY | 201002 | 1 |
| | 400184 | EARTH BRAID ASSY | DATRON | | 1 |
| | 512999 | 7/0.2 PTFE INSUL. WHITE | WIRE | | 0.18M |
| | 521006 | 16/0.2 PVC INS. GRN/YLW | WIRE | | A/R |
| | 590001 | SLEEVE ϕ 3.0 | HELLERMANN. | H15 X 20 | 7 |
| | 590006 | HEATSHRINK SLEEVE ϕ 2.4 | | | A/R |
| | 512444 | 7/0.2 PTFE INSUL. YELLOW | WIRE | | 0.14M |
| | 512838 | 7/0.2 PTFE INSUL. GREY. | WIRE. | | 0.14M |
| | 590003. | HEATSHRINK SLEEVE ϕ 6.4 | | | A/R |
| | 590017 | HEATSHRINK CABLE MARKER ('1') | | | 1 |
| | 590018 | HEATSHRINK CABLE MARKER ('2') | | | 1 |

NOTES.

SEE SHEET 2 FOR LATEST ISSUE

| | | | | | | | | | | | | | | | | | | | | |
|------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ISS | | | | | | | | | | | | | | | | | | | | |
| ECO. | | | | | | | | | | | | | | | | | | | | |
| DATE | | | | | | | | | | | | | | | | | | | | |
| CHKD | | | | | | | | | | | | | | | | | | | | |

| | | | |
|----------|--------------|--------------------------|--------|
| DATE | 12. FEB. 86. | datron ELECTRONICS LTD | |
| DRG. BY | B.S. JACKSON | TITLE | |
| CHECKED | | TERMINAL BOARD ASSEMBLY. | |
| APPROVED | | DRAWING NUMBER | 400640 |
| DATE | | SHEET 3 OF 3 | |

| | | | | |
|--|--|---|---|---|
| DRAWING NO. LD 400859 | | ISSUE | DATE | BY |
| DOCUMENT LIST | | ISSUE | DATE | BY |
| DESCRIPTION | | ISSUE | DATE | BY |
| DRAWING NUMBER | | SHEET NUMBER | DATE | |
| PARTS LIST | | SHEET NUMBER | DATE | |
| ASSEMBLY DRAWING | | SHEET NUMBER | DATE | |
| TEST PROCEDURE | | SHEET NUMBER | DATE | |
| TEST SPECIFICATION | | SHEET NUMBER | DATE | |
| PCB | | SHEET NUMBER | DATE | |
| TITLE | | DRAWING NO. | | |
| <input type="checkbox"/> DENOTES NO CHANGE TO EXCS AT ISSUE LEVEL CHANGE | |  | | DATE: 2.SEP.88 TIME: 12.40 BY: ZS |
| | | DATE: 2.SEP.88 TIME: 12.40 BY: ZS | DATE: 2.SEP.88 TIME: 12.40 BY: ZS | TITLE: 4708 MAIN ASSY |
| | | | | DRAWING NO: LD 400859 SHEET 1 OF 1 |

DATRON INSTRUMENTS LTD PARTS LIST 06-Mar-89 DESC: ASSY MAIN 4708 DRG NO: LP400859-1 REV: 2 PAGE 001 OF 01

| DESIG | PART NO | DESCRIPTION | PRINC MANUF | MANUF PART NUMBER | CLASS | UM | QUANTITY | CHANGES |
|-------|----------|------------------------------|---------------|-------------------|-------|----|----------|---------|
| | 400537-2 | ASSY PCB HV | DATRON | SEE DRG | | | EA 1 | |
| | 400539-7 | ASSY HS PA NEG 4200 | DATRON | SEE DRG | | | EA 1 | |
| | 400540-6 | ASSY HS PSU/I 4200 | DATRON | SEE DRG | | | EA 1 | |
| | 400554-4 | ASSY PCB P/S IN GUARD 4200 | DATRON | SEE DRG | | | EA 1 | |
| | 400561-2 | ASSY PCB P/S OUT GUARD 4200 | DATRON | SEE DRG | | | EA 1 | |
| | 400618-5 | ASSY PCB PA 4XXX | DATRON | SEE DRG | | | EA 1 | |
| | 400637-1 | ASSY HS PA POS 4700 | DATRON | SEE DRG | | | EA 1 | |
| | 400648-1 | ASSY PCB ANALOGUE INTF 4700 | DATRON | SEE DRG | | | EA 1 | |
| | 400653-1 | ASSY PCB JBY PSU 4700 | DATRON | SEE DRG | | | EA 1 | |
| | 400860-1 | ASSY SINE SOURCE 4708 | DATRON | SEE DRG | | | AR 1 | |
| | 400861-1 | ASSY DC 4708 | DATRON | SEE DRG | | | AR 1 | |
| | 400862-1 | ASSY AC 4708 | DATRON | SEE DRG | | | AR 1 | |
| | 400863-1 | ASSY CHASSIS 4708 | DATRON | SEE DRG | | | EA 1 | |
| | 400864-1 | ASSY DIGITAL 4708 | DATRON | SEE DRG | | | EA 1 | |
| | 400865-1 | ASSY REFERENCE DIVIDER 4708 | DATRON | SEE DRG | | | EA 1 | |
| | 400909-1 | ASSY PCB OUTPUT CONTROL 4708 | DATRON | SEE DRG | | | AR 1 | |
| | 410288-1 | PCB CURRENT/OHMS LINK | | SEE DRG | | | EA 1 | |
| | 420103 | TEMP IND LABEL 37-65 DEG C | THERMOGRAPHIC | RANGE A | | A | EA 1 | |
| | 420104 | TEMP IND LABEL 71-110 DEG C | THERMOGRAPHIC | THERMAX RANGE B | | A | EA 1 | |
| | 450414-2 | EARTH SHEET | | SEE DRG | | | EA 1 | |
| | 450415-2 | GUARD SHEET ALUM | | SEE DRG | | | EA 1 | |
| | 450430-2 | HEATSINK RETAINER 4200 | | SEE DRG | | | EA 1 | |
| | 510222 | WIRE 7/0.2 PVC INSULATED RED | | | | | AR 1 | |
| | 590001 | SLEEVE NP 1.5 X 20MM BLK | HELLERMANN | H15 | | | EA 1 | |
| | 590002 | SLEEVE NP 3 X 25MM BLK | HELLERMANN | H30 | | | EA 1 | |
| | 611005 | SCREW M3 X 13 POSIPAN SZP | | | | | EA 1 | |
| | 611007 | SCREW M3 X 6 POSIPAN SZP | | | | | EA 1 | |
| | 611012 | SCREW M3 X 12 POSIPAN SZP | | | | | EA 6 | |
| | 611058 | SCREW M4 X 8 POSIPAN SZP | | | | | EA 20 | |
| | 611076 | SCREW M3 X 6 SLOT PAN SZP | | | | | EA 12 | |
| | 613005 | WASHER M3 INT SHAKERPROOF | | | | | EA 1 | |
| | 630122 | PCB EJECTOR BLUE | RICHCO | CBE | | | EA 1 | |
| | 900016 | CLEANING FLUID | RS | 556-654 | | | AR 1 | |
| | 920101-1 | BATTERY LITHIUM AA | DATRON | SEE DRG | | A | EA 1 | |

End

LD400863

DATE

DATE

DATE

DATE

DATE

DATE

DATE

DATE

DATE

DATE

DATE

DATE

DATE

DATE

DATE

DATE

DATE

DATE

DATE

DATE

DATE

DATE

DATE

DATE

DATE

DATE

DATE

DATE

DATE

DATE

DATE

DATE

DATE

DATE

DATE

DATE

DATE

DATE

DATE

DATE

DATE

DATE

DATE

DATE

DATE

DATE

DATE

DATE

DATE

DATE

DATE

DATE

DATE

DATE

DATE

DATE

DATE

DATE

1.0 3205 8 MAR 89
1.1 3244 8 MAR 89

| ISSUE NO | ISSUE DATE | ISSUE DESCRIPTION |
|----------|------------|-------------------|
| 1 | 1.0 | 1.0 |
| 2 | 1.1 | 1.1 |
| 3 | 1.0 | 1.0 |
| 4 | 1.0 | 1.0 |
| 5 | 1.0 | 1.0 |
| 6 | 1.0 | 1.0 |
| 7 | 1.0 | 1.0 |




DATE 6 JAN 89
DATE 8 MAR 89

TITLE 4708 CHASSIS ASSY

DRAWING NO LD 400863
SHEET 1 OF 1

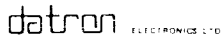
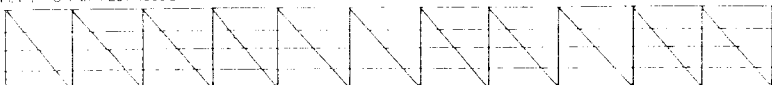
DATRON INSTRUMENTS LTD PARTS LIST 08-Mar-89 DESC: ASSY CHASSIS 4708

| DESIGN | PART NO | DESCRIPTION | PRINC MANUF | MANUF PART NUMBER | CLASS | UN | QUANTITY | ISSUED |
|--------|----------|-----------------------------|--------------------|-------------------|-------|----|----------|--------|
| | 400462-4 | ASSY CABLE MAINS SWITCH | DATRON | SEE DR 1 | | | 1 | |
| | 400463-2 | ASSY CABLE DIGITAL PSU | DATRON | SEE DR 1 | | | 1 | |
| | 400471-1 | ASSY RIBBON CABLE | DATRON | SEE DR 1 | | | 1 | |
| | 400541-4 | ASSY MAINS TRANSF | DATRON | SEE DR 1 | | | 1 | |
| | 400558-1 | ASSY PCB FRONT 4700 | DATRON | SEE DR 1 | | | 1 | |
| | 400560-1 | ASSY CABLE IN/OU PSU 4200 | DATRON | SEE DR 1 | | | 1 | |
| | 400578-4 | ASSY HF TRANSF | DATRON | SEE DR 1 | | | 1 | |
| | 400604-2 | ASSY PCB MOTHER 4700 | DATRON | SEE DR 1 | | | 1 | |
| | 400636-2 | ASSY REAR PANEL 4700 | DATRON | SEE DR 1 | | | 1 | |
| | 400640-1 | ASSY PCB TERMINAL 47XX | DATRON | SEE DR 1 | | | 1 | |
| | 400651-1 | ASSY LF TRANSF | DATRON | SEE DR 1 | | | 1 | |
| | 450265-4 | CHASSIS MOULDED | | SEE DR 1 | | | 1 | |
| | 450271-1 | FILTER GRILLE | | SEE DR 1 | | | 1 | |
| | 450272-1 | TRANSF BOLT PLATE | | SEE DR 1 | | | 1 | |
| | 450277-1 | FOAM FILTER | | SEE DR 1 | | | 1 | |
| | 450280-1 | HANDLE | | SEE DR 1 | | | 1 | |
| | 450293-1 | PCB SUPPORT | | SEE DR 1 | | | 1 | |
| | 450300-1 | REAR SPACE | | SEE DR 1 | | | 1 | |
| | 450301-2 | EARTH BRACKET | | SEE DR 1 | | | 1 | |
| | 450310-1 | SIDE EXTRUSION RH | | SEE DR 1 | | | 1 | |
| | 450311-1 | SIDE EXTRUSION LH | | SEE DR 1 | | | 1 | |
| | 450316-1 | P.S. GUARD SCREEN | | SEE DR 1 | | | 1 | |
| | 450406-1 | 40V PSU BRACKET | | SEE DR 1 | | | 1 | |
| | 450414-2 | EARTH SHEET | | SEE DR 1 | | | 1 | |
| | 450418-1 | SPACER M5 BOLT | | SEE DR 1 | | | 1 | |
| | 450431-1 | HEATSINK GUARD SCREEN 4200 | | SEE DR 1 | | | 1 | |
| | 450436-1 | PLATE TRANSFORMER ROLT | | SEE DR 1 | | | 1 | |
| | 450446-1 | PCB GUARD SCREEN ALUM | | SEE DR 1 | | | 1 | |
| | 450447-1 | PCB EARTH SCREEN | | SEE DR 1 | | | 1 | |
| | 450452-1 | CABLE BRIDGE | | SEE DR 1 | | | 1 | |
| | 450467-1 | FOAM GASKET | | SEE DR 1 | | | 1 | |
| | 450477-1 | PCB EARTH SCREEN | | SEE DR 1 | | | 1 | |
| | 450478-1 | FRONT PANEL 4700 | | SEE DR 1 | | | 1 | |
| | 450542-1 | MADE IN ENGLAND BADGE | | SEE DR 1 | | | 1 | |
| | 450549-1 | PCB GUARD SCREEN STEEL | | SEE DR 1 | | | 1 | |
| | 450550-1 | GUARD SHEET STEEL | | SEE DR 1 | | | 1 | |
| | 510999 | WIRE 2x PVC INSULATED WHITE | | SEE DR 1 | | | 1 | |
| | 540009 | WIRE BRAID 1/8" TINNED CN | REAR SHIELDING KIT | 11 5 11 11 | | | 1 | |
| | 590002 | SLEEVE HS. 6.4mm I.D.W | R.S.D. MICHIGAN | 145 145 | | | 1 | |
| | 590026 | SLEEVE HS. 2.4mm I.D.W | R.S.D. MICHIGAN | 145 145 | | | 1 | |
| | 590007 | LACING TAPE 2.5MM | ALPHA | 145 145 | | | 1 | |
| | 590013 | STU CABLE TIE 32mm | MS | 145 145 | | | 1 | |
| | 590032 | SLEEVE HS. 4.3mm I.D.W | R.S.D. MICHIGAN | 145 145 | | | 1 | |
| | 606005 | SOCKET CLIP PH. 16-WAY | MS | 145 145 | | | 1 | |
| | 611094 | SCREW M3 X 6 POZIHAN RCP | | 145 145 | | | 1 | |

| | | | | | | | | | | | | | | | | | | | | |
|-----------------------------|----------------|----------------------|--|----------------------|----------------------|-----------------------|----------------------|-------------------------------|------------------------|--------------|--|--|--|--|--|--|--|--|--|--|
| DRAWING No 400636 | | CHKD | DATE | ECC | REVISION | ISSUE | | | | | | | | | | | | | | |
| | | 1-012162 25.2.86 (P) | 1.1 2472 8.12.86 (S) | 1.2 2577 21.4.87 (S) | 1.3 2591 11.6.87 (S) | 2.0 2858 8.6.88 (S) | 2.1 2955 20.7.88 (S) | 2.2 2978 23.8.88 (S) | 2.3 3157 13.JAN.89 (S) | | | | | | | | | | | |
| DESCRIPTION | DRAWING NUMBER | SHEET NUMBER | ISSUE - REVISION | | | | | | | | | | | | | | | | | |
| COMPONENT LAYOUT | 480636 | 1 | 1-0 | 1-1 | 1-2 | 1-3 | 2-0 | 2-1 | 2-1.2.2 | 2-2 | | | | | | | | | | |
| L.P. | 400636 | ALL | | | | | | | | | | | | | | | | | | |
| NOTES | | |  | | DPN DATE 13.8.85 | CHKD DATE 24.12.85 | APPD DATE 7.3.86 | TITLE 4700 REAR PANEL ASSY | DRAWING No 400636 | SHEET 1 of 4 | | | | | | | | | | |

400636

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | Qty USED Dir Assy |
|------------|-----------------|--|------------------------|-------------------------|-------------------|
| | 400184-2 | TAG + BRAID ASSY | | | 1 |
| | 400830-1 | INTERCONNECTION PCB ASSY | DATRON | | 1 |
| | 400641-1 | CAL. I/O PORT CABLE ASSY | DATRON | | 1 |
| | 450682-1 | REAR PANEL | | | 1 |
| | 450309-2 | IEEE MOUNTING SCREW | | | 2 |
| | 512333 | 7/2 PTFE INS (ORANGE) WIRE | | | 450mm |
| | 512555 | 7/2 PTFE INS (GREEN) WIRE | | | 180mm |
| | 512999 | 7/2 PTFE INS (WHITE) WIRE | | | 770mm |
| | 530000 | 24/2 PVC INS (BLACK) WIRE | | | 100mm |
| | 530111 | 24/2 PVC INS (BROWN) WIRE | | | 110mm |
| | 530222 | 24/2 PVC INS (RED) WIRE | | | 120mm |
| | 530333 | 24/2 PVC INS (ORANGE) WIRE | | | 120mm |
| | 530444 | 24/2 PVC INS (YELLOW) WIRE | | | 110mm |
| | 530555 | 24/2 PVC INS (GREEN) WIRE | | | 130mm |
| | 530666 | 24/2 PVC INS (BLUE) WIRE | | | 110mm |
| | 530777 | 24/2 PVC INS (VIOLET) WIRE | | | 115mm |
| | 530888 | 24/2 PVC INS (GREY) WIRE | | | 120mm |
| | 530999 | 24/2 PVC INS (WHITE) WIRE | | | 110mm |
| | 560002 | Ø2.5 7/34 ANG COPPER COVERED STEEL CO-AX | | | 800mm |

| | | | | |
|---|--|---------------|---|--|
| NOTES | | DATE 22.11.85 |  | |
| SEE SHEET 1 FOR LATEST ISSUE | | DRAWN L | TITLE 4700 REAR PANEL ASSY | |
|  | | CHECKED MD | DRAWING NUMBER 400636 | |
| | | APPROVED | SHEET 2 of 4 | |
| | | DATE | | |

400636

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No. USED Per Assy. |
|------------|-----------------|---------------------------------|------------------------|-------------------------|--------------------|
| | 590001 | SLEEVE MAX. CABLE Ø3.0 | HELLERMANN ELECTRIC | HIS x20 BLK. HELSYN | 5 |
| | 590029 | HEATSHRINK SLEEVE. POLYOLEFIN 3 | HELLERMANN | SFM9-3BK | 55 mm |
| | 590031 | HEATSHRINK Ø3.2 YELLOW | | | 290 mm |
| | 590005 | SLEEVE MAX CABLE Ø4.0 | HELLERMANN ELECTRIC | H20x20 BLK. HELSYN. | 5 |
| | 601001 | BNC 50Ω BULKHEAD SKT. | GREENPAR | GE35027S | 1 |
| | 590006 | HEATSHRINK SLEEVE Ø2.4 | | | A/R. |
| | 605051 | 4-WAY POLARISED SOCKET | MOLEX | 22-01-2045 | 1 |
| | 605057 | CRIMP TERMINAL | MOLEX | 4809-GL | 2 |
| | 605135 | 6-WAY CHASSIS MNT. 0.093" SKT. | MOLEX | 03-09-1061 | 2 |
| | 605136 | 0.093" MALE CRIMP TERM. GD. | MOLEX | 02-09-6123 | 5 |
| | 605137 | 0.093" FEMALE CRIMP TERM. GD. | MOLEX | 02-09-5123 | 5 |
| | 590074 | SOLDER SLEEVE Ø3.0 | RAYFAST | CWT-3 | 2 |
| | 606013 | 'D' CONN. JACKSCREW | T+B ANSLEY | 609-004 | 2 |
| | 606014 | 'D' CONN. JACK SOCKET | T+B ANSLEY | 609-006 | 2 |
| | 611005 | SCREW M3x12mm STEEL | POZIPAN ZINC PLATED | GKN | 1 |
| | 611016 | SCREW M3x8mm STEEL | POZIPAN ZINC PLATED | GKN | 2 |
| | 611017 | SCREW M3x16mm STEEL | POZIPAN ZINC PLATED | GKN | 2 |
| | 611049 | SCREW M4x20mm STEEL | POZIPAN ZINC PLATED | GKN | 4 |
| | 613005 | WASHER M3 INT./SHAKEPROOF | STEEL ZINC PLATED | GKN | 5 |
| | 613009 | SOLDER TAG 48A | | | 3 |

NOTES.

SEE SHEET 2 FOR LATEST ISSUE

| | | | | | | | | | | | | | | | | | | | |
|------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ISS | | | | | | | | | | | | | | | | | | | |
| ECD | | | | | | | | | | | | | | | | | | | |
| DATE | | | | | | | | | | | | | | | | | | | |
| CHKD | | | | | | | | | | | | | | | | | | | |

| | | | |
|----------|----------|------------------------|----------------------|
| DATE | 22.11.85 | datron ELECTRONICS LTD | |
| DRAWN | IL | TITLE | 4700 REAR PANEL ASSY |
| CHECKED | ID | DRAWING NUMBER | 400636 |
| APPROVED | | SHEET | 3 OF 4 |
| DATE | | | |

400636

| DESIGNATOR | DATRON PART No. | DESCRIPTION | PRINCIPAL MANUFACTURER | MANUFACTURER'S PART No. | No. USED Per Assy. |
|------------|-----------------|----------------------------|------------------------|-------------------------|--------------------|
| | 560008-3 | 4 CORE PTFE SCREENED CABLE | | SEE DRG | 0.47M |
| | 613021 | M4 INT. SHAKEPROOF | | | 4 |
| | 590076 | SOLDER SLEEVE Ø7.3 | RAYFAST | CWT-7 | 1 |
| | 615002 | M3 FULL NUT STEEL ZN PL | | | 1 |
| | 615011 | M4 FULL NUT STEEL ZN PL | | | 4 |
| | 630099 | MASKING TAPE 25mm | 3M | N230 | A/R. |
| | 630133 | HOLE PLUG 1/4" BLACK | HEYCO | DP250 | 6 |
| | 700071-1 | SWITCH 1POLE KEY | | SEE DRG | 1 |
| | 900009 | LOCKING COMPOUND | LOCTITE | 270 | A/R |
| | 920150 | FAN 119mm 115V BALL-B | REDPOINT. | RCF 162/115 | 1 |
| | 920086 | POWER INPUT MODULE | POTTER | 7100-0002 | 1 |
| | 920098 | FUSE 3A 250V 1/4" SLO-B | LITTLEFUSE | 313 003 | 1 |
| J56 | 605181 | 6-WAY CHASSIS MTG. SOCKET | LEMO | EGG-2B-306CNL | 1 |
| J56 | 606034 | CHASSIS MTG. DUST COVER | LEMO | BRR-2S-200PZSG | 1 |

NOTES.


SEE SHEET 2 FOR LATEST ISSUE

| | | | | | | | | | | | | | | | | | | | |
|------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ISS | | | | | | | | | | | | | | | | | | | |
| ECD | | | | | | | | | | | | | | | | | | | |
| DATE | | | | | | | | | | | | | | | | | | | |
| CHKD | | | | | | | | | | | | | | | | | | | |

| | | | |
|----------|----------|------------------------|----------------------|
| DATE | 22.11.85 | datron ELECTRONICS LTD | |
| DRAWN | IL | TITLE | 4700 REAR PANEL ASSY |
| CHECKED | ID | DRAWING NUMBER | 400636 |
| APPROVED | | SHEET | 4 OF 4 |
| DATE | | | |

| DRAWING NO | | CHK'D | | | | | | |
|------------|--|----------|-----|------|----------|---|--|--|
| 400603 | | | 3.0 | 1958 | 11.7.85 | W | | |
| DIWN | | DATE | 3.1 | 2150 | 21.5.86 | | | |
| | | ECO | 3.2 | 2318 | 11.7.86 | | | |
| | | REVISION | 3.3 | 2301 | 18.7.86 | | | |
| | | ISSUE | 3.4 | 2465 | 19.11.86 | | | |
| | | | 3.5 | 2707 | 17.1.88 | | | |
| | | | 3.6 | 3205 | 23.8.89 | W | | |

| DESCRIPTION | DRAWING NUMBER | SHEET NUMBER | ISSUE - REVISION | | | | | | | | | |
|--------------|----------------|--------------|------------------|-----|-----|-----|--|--|--|--|--|--|
| COMP LAYOUT. | 480603 | 1 | 3.0 | 3.0 | 3.0 | 3.0 | | | | | | |
| COMP LAYOUT. | 480603 | 2 | | | | | | | | | | |
| COMP LAYOUT. | 480603 | 3 | | | | | | | | | | |
| COMP LAYOUT. | 480603 | 4 | | | | | | | | | | |
| COMP LAYOUT. | 480603 | 5 | | | | | | | | | | |
| COMP LAYOUT. | 480603 | 6 | | | | | | | | | | |
| COMP LAYOUT. | 480603 | 7 | | | | | | | | | | |

| | | | | | | |
|-------|--|---|--------------------------------|---------------------------------|--|--------------------------------------|
| NOTES |  | DRN B. JACKSON DATE 11 JULY 85 | CHK'D MS DATE 26.7.85 | APP'D MS DATE 22.12.84 | TITLE 4200/4700/4705/4707 OPTION FITTING | DRAWING NO 400603 SHEET 1 of 1 |
|-------|--|---|--------------------------------|---------------------------------|--|--------------------------------------|

TERMS AND CONDITIONS OF SALE

1. GENERAL

The acceptance of a quotation, of any goods supplied, advice given or service rendered includes the acceptance of the following terms and conditions and no variation of or addition to the same shall be binding upon us unless expressly agreed in writing by us. Any order shall be subject to our written acceptance.

2. QUOTATION

Unless previously withdrawn our quotation is open to acceptance in writing within the period stated or where no period is stated within thirty (30) days after its date. We reserve the right to correct any errors or omissions in our quotation. Unless otherwise stated all quotations are firm and fixed. The prices quoted are based on manufacture of the quantity and type ordered and are subject to revision when interruptions, engineering changes or changes in quantity are caused or requested by the customer.

3. LIABILITY FOR DELAY

Any delivery times quoted are from the date of our written acceptance of any order and on receipt of all information and drawings to enable us to put the work in hand. Where delivery is to take place by instalments each such instalment shall constitute a separate contract. We will use our best endeavours to complete delivery of the goods or services in the period stated but accept no liability in damages or otherwise for failure to do so for any cause whatsoever. In all cases of delay the delivery time shall be extended by reasonable period having regard to the cause of delay.

4. PAYMENT

Payment shall be made net cash within thirty (30) days of delivery or in accordance with the payment terms set out in the quotation. Unless specifically stated to the contrary payment shall be in pounds sterling. In the event of any payment to us being overdue we may without prejudice to any other right suspend delivery to you or terminate the contract and/or charge you simple interest on overdue amounts at the rate of 2.5% above the ruling Bank of England Minimum Lending Rate. No payment to us shall in any circumstance be offset against any sum owing by us to you whether in respect of the present transaction or otherwise.

5. INSPECTION & TEST

All goods are fully inspected at our works and where practicable subjected to our standard tests before despatch. If tests are required to be witnessed by your representative notice of this must be given at the time of placing the order and notice of readiness will then be given to you seven (7) days in advance of such tests being carried out. In the event of any delay on your part in attending such tests or in carrying out inspection by you after seven (7) days notice of readiness the tests will proceed in your absence and shall be deemed to have been made in your presence and the inspection deemed to have been made by you. In any event you shall be required promptly after witnessing a test or receiving test results of witnessed or unwitnessed tests to notify us in writing of any claimed defects in the goods or of any respect in which it is claimed that the goods do not conform with the contract. Before you become entitled to reject any goods we are to be given reasonable time and opportunity to rectify them. You assume the responsibility that the goods stipulated by you are sufficient and suitable for your purpose and take all steps to ensure that the goods will be safe and without risk to health when properly used. Any additional certification demanded may incur extra cost for which a special quotation will be issued.

6. DELIVERY AND PACKING

All shipments are, unless otherwise specifically provided, Ex-works which is the address given on the invoice. An additional charge will be made for carriage and insurance as necessary with the provision that all shipments shall be insured and this insurance expense shall be paid by the purchaser. Where special domestic or export packing is specified a charge will be made to cover the extra expense involved.

7. DAMAGE IN TRANSIT

Claims for damage in transit or loss in delivery of the goods will only be considered if the carriers and ourselves receive notice of such damage within seven (7) days of delivery or in the event of loss of goods in transit within fourteen (14) days of consignment.

8. TRANSFER OF PROPERTY & RISK

Title and property of the goods shall pass when full payment has been received of all sums due to us whether in respect of the present transaction or not. The risk in the goods shall be deemed to have passed on delivery.

9. WARRANTY

We agree to correct, either by repair, or at our election, by replacement, any defects of material or workmanship which develop within the warranty period specified in the sales literature or quotation after delivery to the original purchaser. All items claimed defective must be promptly returned to us carriage paid unless otherwise arranged and will be returned to you free of charge. Unless otherwise agreed no warranty is made concerning components or accessories not manufactured by us. We will be released from all obligations under warranty in the event of repairs or modifications made by persons other than our own authorised service personnel unless such repairs are made with our prior written consent.

10. PATENTS

We will indemnify you against any claim of infringement of Letters Patent, Registered Design, Trade Mark or Copyright (published at the date of the contract) by the use or sale of any goods supplied or service rendered by us to you and against all costs and damages which you may incur and for which you may become liable in any action for such infringement. Provided always that this indemnity shall not apply to any infringement which is due to our having followed a design or instruction furnished or given by you or to the use of such goods or service in association or combination with any other article, material or service not supplied by us. This indemnity is conditional on your giving to us the earliest possible notice in writing of any claim being made or action threatened or brought against you and on your permitting us at our own expense to conduct litigation that may ensue and all negotiations for a settlement of the claim or action. You on your part warrant that any design or instruction furnished or given by you shall not cause us to infringe any Letter Patent, Registered Design, Trade Mark or Copyright in the execution of your order.

11. DOCUMENTATION

All drawings, plans, designs, software specifications, manuals and technical documents and information supplied by us for your use or information shall remain at all times our exclusive property and must not be copied, reproduced, transmitted or communicated to a third party without our prior written consent.

12. FRUSTRATION

If any contract or any part of it shall become impossible of performance or otherwise frustrated we shall be entitled to a fair and reasonable proportion of the price in respect of the work done up to the date thereof. For this purpose any monies previously paid by you shall be retained against the sum due to us under this provision. We may dispose of the goods as we think fit due allowance being made to you for the net proceeds thereof.

13. BANKRUPTCY

If the purchaser shall become bankrupt or insolvent, or being a Limited Company commence to be wound up or suffer a Receiver to be appointed, we shall be at liberty to treat the contract as terminated and be relieved of further obligations. This shall be without prejudice to our right to claim for damages for breach of contract.

14. LEGAL INTERPRETATION

Any contract will be deemed to be made in England and shall be governed and construed for all purposes and in all respects in accordance with English Law and only the Courts of England shall have jurisdiction.

| COUNTRY and REPRESENTATIVE | Telephone | Telex | Fax |
|--|----------------|-----------------------|----------------|
| UNITED KINGDOM | | | |
| Datron Instruments Ltd Hurricane Way, Norwich Airport, Norwich, Norfolk NR6 6JB, England | 0603 404824 | 975173 | 0603 483670 |
| UNITED STATES of AMERICA | | | |
| Datron Instruments Inc c/o Wavetek RF Products Inc. 5808 Churchman Bypass, Indianapolis, Indiana 46203 | (317) 787 3915 | TWX (810) 341 3226 | (317) 788 5999 |
| Wavetek Northeast Area Sales 1 Executive Blvd. Suite 206, Suffern New York 10901 | (914) 357 5544 | | (914) 357 5609 |
| Wavetek Western Area Sales 9045 Balboa Avenue, San Diego, California 92123 | (619) 565 9234 | TWX (910) 335 2007 | (619) 565 9558 |

For customers in countries not listed please contact DATRON INSTRUMENTS in the United Kingdom:

| | | | |
|---|-------------|--------|-------------|
| Datron Instruments Ltd Hurricane Way, Norwich Airport, Norwich, Norfolk NR6 6JB, England | 0603 404824 | 975173 | 0603 483670 |
|---|-------------|--------|-------------|

| DESIG | PART NO | DESCRIPTION | PRINC MANUF | MANUF PART NUMBER | CLASS | UM | QUANTITY | CHANGES |
|-------|---------|---------------------------|-------------|-------------------|-------|----|----------|---------|
| R56 | 013573 | RES MF 357K 1% .12W 50PPM | MEC | H8 357K 1% 50PPM | A | EA | - | |
| R57 | 011780 | RES MF 178K 1% .12W 50PPM | MEC | H8 178K 1% 50PPM | A | EA | - | |
| R58 | 012872 | RES MF 287K 1% .12W 50PPM | MEC | H8 287K 1% 50PPM | A | EA | - | |
| R59 | 014422 | RES MF 442K 1% .12W 50PPM | MEC | H8 442K 1% 50PPM | A | EA | - | |
| R60 | 012262 | RES MF 226K 1% .12W 50PPM | MEC | H8 226K 1% 50PPM | A | EA | - | |
| R61 | 011132 | RES MF 11K3 1% .12W 50PPM | MEC | H8 11K3 1% 50PPM | A | EA | - | |
| R62 | 015621 | RES MF 5K62 1% .12W 50PPM | MEC | H8 5K62 1% 50PPM | A | EA | - | |
| R63 | 012801 | RES MF 2K80 1% .12W 50PPM | MEC | H8 2K80 1% 50PPM | A | EA | 2 | |
| R64 | 013321 | RES MF 3K32 1% .12W 50PPM | MEC | H8 3K32 1% 50PPM | A | EA | - | |
| R65 | 013321 | RES MF 3K32 1% .12W 50PPM | MEC | H8 3K32 1% 50PPM | A | EA | - | |
| R66 | 000103 | RES CF 10K 5% .25W | NEOHM | CFR25 10K 5% | A | EA | - | |
| R67 | 000103 | RES CF 10K 5% .25W | NEOHM | H8 10K0 1% 50PPM | A | EA | - | |
| R68 | 011002 | RES MF 10K0 1% .12W 50PPM | MEC | H8 10K0 1% 50PPM | A | EA | - | |
| R69 | 011002 | RES MF 10K0 1% .12W 50PPM | MEC | H8 1K50 1% 50PPM | A | EA | - | |
| R70 | 011501 | RES MF 1K50 1% .12W 50PPM | MEC | H8 1K50 1% 50PPM | A | EA | - | |
| R71 | 011501 | RES MF 1K50 1% .12W 50PPM | NEOHM | CFR25 1K0 5% | A | EA | - | |
| R72 | 000102 | RES CF 1K0 5% .25W | NEOHM | CFR25 1K0 5% | A | EA | 1 | |
| R73 | 000102 | RES CF 1K0 5% .25W | MEC | H8 274K 1% 50PPM | A | EA | - | |
| R74 | 012743 | RES MF 274K 1% .12W 50PPM | MEC | H8 499R 1% 50PPM | A | EA | - | |
| R75 | 014990 | RES MF 499R 1% .12W 50PPM | MEC | | | | | |
| R76 | 000470 | RES CF 47R 5% .25W | NEOHM | CFR25 47R 5% | A | EA | - | |
| R77 | 001182 | RES CF 1K8 5% .5W | NEOHM | CFR50 1K8 5% | A | EA | - | |
| R78 | 000103 | RES CF 10K 5% .25W | NEOHM | CFR25 10K 5% | A | EA | 2 | |
| R79 | 012551 | RES MF 2K55 1% .12W 50PPM | MEC | H8 2K55 1% 50PPM | A | EA | - | |
| R80 | 012551 | RES MF 2K55 1% .12W 50PPM | MEC | H8 2K55 1% 50PPM | A | EA | - | |
| R81 | 000822 | RES CF 8K2 5% .25W | NEOHM | CFR25 8K2 5% | A | EA | 5 | |
| R82 | 000822 | RES CF 8K2 5% .25W | NEOHM | CFR25 8K2 5% | A | EA | - | |
| R83 | 000822 | RES CF 8K2 5% .25W | NEOHM | CFR25 8K2 5% | A | EA | - | |
| R84 | 000822 | RES CF 8K2 5% .25W | NEOHM | CFR25 8K2 5% | A | EA | - | |
| R85 | 000152 | RES CF 1K5 5% .25W | NEOHM | CFR25 1K5 5% | A | EA | - | |
| R86 | 000433 | RES CF 43K 5% .25W | NEOHM | CFR25 43K 5% | A | EA | 1 | |
| R87 | 000822 | RES CF 8K2 5% .25W | NEOHM | CFR25 8K2 5% | A | EA | - | |
| R88 | 000471 | RES CF 470R 5% .25W | NEOHM | CFR25 470R 5% | A | EA | 4 | |
| R89 | 000362 | RES CF 3K6 5% .25W | NEOHM | CFR25 3K6 5% | A | EA | 2 | |
| R90 | 000470 | RES CF 47R 5% .25W | NEOHM | CFR25 47R 5% | A | EA | - | |
| R91 | 013161 | RES MF 3K16 1% .12W 50PPM | MEC | H8 3K16 1% 50PPM | A | EA | 2 | |
| R92 | 000122 | RES CF 1K2 5% .25W | NEOHM | CFR25 1K2 5% | A | EA | - | |
| R93 | 000470 | RES CF 47R 5% .25W | NEOHM | CFR25 47R 5% | A | EA | - | |
| R94 | 000470 | RES CF 47R 5% .25W | NEOHM | CFR25 47R 5% | A | EA | - | |
| R95 | 000470 | RES CF 47R 5% .25W | NEOHM | CFR25 47R 5% | A | EA | - | |
| R96 | 011872 | RES MF 18K7 1% .12W 50PPM | MEC | H8 18K7 1% 50PPM | A | EA | 3 | |
| R97 | 000104 | RES CF 100K 5% .25W | NEOHM | CFR25 100K 5% | A | EA | 2 | |
| R98 | 011378 | RES MF 13R7 1% .12W 50PPM | MEC | H8 13R7 1% 50PPM | A | EA | - | |
| R99 | 000104 | RES CF 100K 5% .25W | NEOHM | CFR25 100K 5% | A | EA | - | |
| R100 | 011872 | RES MF 18K7 1% .12W 50PPM | MEC | H8 18K7 1% 50PPM | A | EA | - | |

| DESIG | PART NO | DESCRIPTION | PRINC MANUF | MANUF PART NUMBER | CLASS | UM | QUANTITY | CHANGES |
|-------|---------|---------------------------|-------------|-------------------|-------|----|----------|---------|
| R101 | 011378 | RES MF 13R7 1% .12W 50PPM | MEC | H8 13R7 1% 50PPM | A | EA | - | |
| R102 | 000471 | RES CF 470R 5% .25W | NEOHM | CFR25 470R 5% | A | EA | - | |
| R103 | 013091 | RES MF 3K09 1% .12W 50PPM | MEC | H8 3K09 1% 50PPM | A | EA | 2 | |
| R104 | 011541 | RES MF 1K54 1% .12W 50PPM | MEC | H8 1K54 1% 50PPM | A | EA | 2 | |
| R105 | 011541 | RES MF 1K54 1% .12W 50PPM | MEC | H8 1K54 1% 50PPM | A | EA | - | |
| R106 | 013091 | RES MF 3K09 1% .12W 50PPM | MEC | H8 3K09 1% 50PPM | A | EA | - | |
| R107 | 000470 | RES CF 47R 5% .25W | NEOHM | CFR25 47R 5% | A | EA | - | |
| R108 | 017871 | RES MF 7K87 1% .12W 50PPM | MEC | H8 7K87 1% 50PPM | A | EA | 1 | |
| R109 | 000101 | RES CF 100R 5% .25W | NEOHM | CFR25 100R 5% | A | EA | 9 | |
| R110 | 000225 | RES CF 2M2 5% .25W | NEOHM | CFR25 2M2 5% | A | EA | 1 | |
| R112 | 000100 | RES CF 10R 5% .25W | NEOHM | CFR25 10R 5% | A | EA | - | |
| R113 | 000362 | RES CF 3K6 5% .25W | NEOHM | CFR25 3K6 5% | A | EA | - | |
| R114 | 000470 | RES CF 47R 5% .25W | NEOHM | CFR25 47R 5% | A | EA | - | |
| R115 | 000470 | RES CF 47R 5% .25W | NEOHM | CFR25 47R 5% | A | EA | - | |
| R116 | 000470 | RES CF 47R 5% .25W | NEOHM | CFR25 47R 5% | A | EA | - | |
| R117 | 000101 | RES CF 100R 5% .25W | NEOHM | CFR25 100R 5% | A | EA | - | |
| R118 | 012432 | RES MF 24K3 1% .12W 50PPM | MEC | H8 24K3 1% 50PPM | A | EA | 2 | |
| R119 | 012432 | RES MF 24K3 1% .12W 50PPM | MEC | H8 24K3 1% 50PPM | A | EA | - | |
| R120 | 011002 | RES MF 10K0 1% .12W 50PPM | MEC | H8 10K0 1% 50PPM | A | EA | - | |
| R121 | 017501 | RES MF 7K50 1% .12W 50PPM | MEC | H8 7K50 1% 50PPM | A | EA | 1 | |
| R122 | 011002 | RES MF 10K0 1% .12W 50PPM | MEC | H8 10K0 1% 50PPM | A | EA | - | |
| R123 | 066103 | RES CT 10K SIDE ADJ S/T | BECKMAN | 72XW | A | EA | 1 | |
| R124 | 000100 | RES CF 10R 5% .25W | NEOHM | CFR25 10R 5% | A | EA | - | |
| R125 | 000100 | RES CF 10R 5% .25W | NEOHM | CFR25 10R 5% | A | EA | - | |
| R126 | 001182 | RES CF 1K8 5% .5W | NEOHM | CFR50 1K8 5% | A | EA | - | |
| R127 | 000101 | RES CF 100R 5% .25W | NEOHM | CFR25 100R 5% | A | EA | - | |
| R128 | 000101 | RES CF 100R 5% .25W | NEOHM | CFR25 100R 5% | A | EA | - | |
| R129 | 011211 | RES MF 1K21 1% .12W 50PPM | MEC | H8 1K21 1% 50PPM | A | EA | 1 | |
| R130 | 011002 | RES MF 10K0 1% .12W 50PPM | MEC | H8 10K0 1% 50PPM | A | EA | - | |
| R131 | 011002 | RES MF 10K0 1% .12W 50PPM | MEC | H8 10K0 1% 50PPM | A | EA | - | |
| R132 | 000101 | RES CF 100R 5% .25W | NEOHM | CFR25 100R 5% | A | EA | - | |
| R133 | 001182 | RES CF 1K8 5% .5W | NEOHM | CFR50 1K8 5% | A | EA | - | |
| R134 | 014321 | RES MF 4K32 1% .12W 50PPM | MEC | H8 4K32 1% 50PPM | A | EA | 2 | |
| R135 | 012491 | RES MF 2K49 1% .12W 50PPM | MEC | H8 2K49 1% 50PPM | A | EA | 2 | |
| R136 | 090063 | THERMISTOR PTC | PHILIPS | KTY81-120 | A | EA | - | |
| R137 | 090063 | THERMISTOR PTC | PHILIPS | KTY81-120 | A | EA | - | |
| R138 | 000101 | RES CF 100R 5% .25W | NEOHM | CFR25 100R 5% | A | EA | - | |
| R139 | 050153 | RES MF 6R2 1% .5W 50PPM | WELWYN | MFR4 | A | EA | 1 | |
| R140 | 000202 | RES CF 2K0 5% .25W | NEOHM | CFR25 2K0 5% | A | EA | - | |
| R141 | 000101 | RES CF 100R 5% .25W | NEOHM | CFR25 100R 5% | A | EA | - | |
| R142 | 000101 | RES CF 100R 5% .25W | NEOHM | CFR25 100R 5% | A | EA | - | |
| R143 | 012491 | RES MF 2K49 1% .12W 50PPM | MEC | H8 2K49 1% 50PPM | A | EA | - | |
| R144 | 050153 | RES MF 6R2 1% .5W 50PPM | WELWYN | MFR4 | A | EA | - | |
| R145 | 000221 | RES CF 220R 5% .25W | NEOHM | CFR25 220R 5% | A | EA | 2 | |
| R146 | 000221 | RES CF 220R 5% .25W | NEOHM | CFR25 220R 5% | A | EA | - | |

| DESIG | PART NO | DESCRIPTION | PRINC MANUF | MANUF PART NUMBER | CLASS | UM | QUANTITY | CHANGES |
|-------|---------|---------------------------|-------------|--------------------|-------|----|----------|---------|
| R147 | 090101 | RES CF 100K 5% .25W | NECHM | CPR25 100R 5% | A | EA | - | |
| R148 | 090278 | RES CF 2R 5% .25W | NECHM | CPR25 2R7 5% | A | EA | 1 | |
| R149 | 013161 | RES MF 3K16 1% .12W 50PPM | MED | H8 3K16 1% 50PPM | A | EA | - | |
| R150 | 000471 | RES CF 470R 5% .25W | NECHM | CPR25 470R 5% | A | EA | - | |
| R151 | 014751 | RES MF 4K75 1% .12W 50PPM | MED | H8 4K75 1% 50PPM | A | EA | - | |
| R152 | 015230 | RES MF 523R 1% .12W 50PPM | MED | H8 523R 1% 50PPM | A | EA | 1 | |
| R153 | 014320 | RES MF 432R 1% .12W 50PPM | MED | H8 432R 1% 50PPM | A | EA | 1 | |
| R154 | 014751 | RES MF 4K75 1% .12W 50PPM | MED | H8 4K75 1% 50PPM | A | EA | - | |
| R155 | 000472 | RES CF 4K7 5% .25W | NECHM | CPR25 4K7 5% | A | EA | 3 | |
| R156 | 000472 | RES CF 4K7 5% .25W | NECHM | CPR25 4K7 5% | A | EA | - | |
| R157 | 000471 | RES CF 470R 5% .25W | NECHM | CPR25 470R 5% | A | EA | - | |
| R158 | 000150 | RES CF 15R 5% .25W | NECHM | CPR25 15R 5% | A | EA | 1 | |
| R159 | 000472 | RES CF 4K7 5% .25W | NECHM | CPR25 4K7 5% | A | EA | - | |
| R160 | 00000N | NOT FITTED | | | | EA | 12 | |
| R161 | 000104 | RES CF 100K 5% .25W | NECHM | CPR25 100K 5% | A | EA | - | |
| AN1 | 090131 | RES PACK 10K X 4 2% | BECKMAN | L08-3S-R10K | A | EA | 8 | |
| AN2 | 090131 | RES PACK 10K X 4 2% | BECKMAN | L08-3S-R10K | A | EA | - | |
| AN3 | 090131 | RES PACK 10K X 4 2% | BECKMAN | L08-3S-R10K | A | EA | - | |
| AN4 | 090132 | RES PACK 4K7 X 4 2% | BECKMAN | L08-3S-R4K7 | A | EA | 1 | |
| AN5 | 090140 | RES NTWK 22K X 9 2% | BECKMAN | L10-1S-R22K | A | EA | 2 | |
| AN6 | 090141 | RES NTWK 1M X 9 2% | BECKMAN | L10-1S-R1M | A | EA | 2 | |
| AN7 | 090131 | RES PACK 10K X 4 2% | BECKMAN | L08-3S-R10K | A | EA | - | |
| AN8 | 090140 | RES NTWK 22K X 9 2% | BECKMAN | L10-1S-R22K | A | EA | - | |
| AN9 | 090141 | RES NTWK 1M X 9 2% | BECKMAN | L10-1S-R1M | A | EA | - | |
| AN10 | 090131 | RES PACK 10K X 4 2% | BECKMAN | L08-3S-R10K | A | EA | - | |
| AN11 | 090131 | RES PACK 10K X 4 2% | BECKMAN | L08-3S-R10K | A | EA | - | |
| AN12 | 090086 | RES PACK 100K X 8 2% | AB | 761-3-100K | A | EA | 1 | |
| AN13 | 090131 | RES PACK 10K X 4 2% | BECKMAN | L08-3S-R10K | A | EA | - | |
| AN14 | 090142 | RES PACK 10K X 4 .5% | BECKMAN | 694-3-R10KD | A | EA | 1 | |
| AN15 | 090136 | RES PACK 2K X 8 .5% | BECKMAN | 698-3-R2KD | A | EA | 3 | |
| AN16 | 090136 | RES PACK 2K X 8 .5% | BECKMAN | 698-3-R2KD | A | EA | - | |
| AN17 | 090131 | RES PACK 10K X 4 2% | BECKMAN | L08-3S-R10K | A | EA | - | |
| AN18 | 090136 | RES PACK 2K X 8 .5% | BECKMAN | 698-3-R2KD | A | EA | - | |
| AN19 | 090143 | RES PACK 500R X 4 .5% | BECKMAN | 694-3-R500D | A | EA | 1 | |
| AN20 | 090168 | RES PACK 1K X 4 2% | AB | 770-83-1K | A | EA | 1 | |
| C1 | 100181 | CAP CP 180PF 2% 100V | PHILIPS | 2222 683 58181 | | EA | 1 | |
| C2 | 100561 | CAP CP 560PF 10% 100V | PHILIPS | 2222 630 19561 | | EA | 1 | |
| C3 | 100102 | CAP CP 1NF 10% 100V | PHILIPS | 2222 630 19102 | | EA | 15 | |
| C4 | 110027 | CAP PE 330F 20% 100V | WIMA | FKS2 3300 20% 100V | | EA | 1 | |
| C5 | 100121 | CAP CP 120PF 2% 100V | PHILIPS | 2222 683 34121 | | EA | 1 | |
| C6 | 150020 | CAP DT 10UF 20% 25V | AVX | TAP10M25F | A | EA | 15 | |
| C7 | 104026 | CAP CM 47NF +80%-20% 50V | AVX | SR175E473ZAA | A | EA | 34 | |
| C8 | 150020 | CAP DT 10UF 20% 25V | AVX | TAP10M25F | A | EA | - | |
| C9 | 150020 | CAP DT 10UF 20% 25V | AVX | TAP10M25F | A | EA | - | |
| C10 | 104026 | CAP CM 47NF +80%-20% 50V | AVX | SR175E473ZAA | A | EA | - | |

| DESIG | PART NO | DESCRIPTION | PRINC MANUF | MANUF PART NUMBER | CLASS | UM | QUANTITY | CHANGES |
|-------|---------|-------------------------------|-------------|--------------------|-------|----|----------|---------|
| C11 | 104026 | CAP CM 47NF +80%-20% 50V | AVX | SR175E473ZAA | A | EA | - | |
| C12 | 104026 | CAP CM 47NF +80%-20% 50V | AVX | SR175E473ZAA | A | EA | - | |
| C13 | 100102 | CAP CP 1NF 10% 100V | PHILIPS | 2222 630 19102 | | EA | - | |
| C14 | 110035 | CAP PE 220NF 20% 63V | WIMA | MKS2 0.22 20% 63V | | EA | 1 | |
| C15 | 110050 | CAP PE 22NF 10% 63V | WIMA | MKS2 0.022 10% 63V | | EA | 1 | |
| C16 | 104026 | CAP CM 47NF +80%-20% 50V | AVX | SR175E473ZAA | A | EA | - | |
| C17 | 104026 | CAP CM 47NF +80%-20% 50V | AVX | SR175E473ZAA | A | EA | - | |
| C18 | 104026 | CAP CM 47NF +80%-20% 50V | AVX | SR175E473ZAA | A | EA | - | |
| C19 | 104026 | CAP CM 47NF +80%-20% 50V | AVX | SR175E473ZAA | A | EA | - | |
| C20 | 102471 | CAP CD 470PF 20% 500V N4700 | BECK | CD10EM470PMSCR | A | EA | 1 | |
| C21 | 150020 | CAP DT 10UF 20% 25V | AVX | TAP10M25F | A | EA | - | |
| C22 | 150020 | CAP DT 10UF 20% 25V | AVX | TAP10M25F | A | EA | - | |
| C23 | 100102 | CAP CP 1NF 10% 100V | PHILIPS | 2222 630 19102 | | EA | - | |
| C24 | 104026 | CAP CM 47NF +80%-20% 50V | AVX | SR175E473ZAA | A | EA | - | |
| C25 | 120034 | CAP PC 220NF 1% 63V | ASHCROFT | M2B22101E | | EA | 2 | |
| C26 | 102100 | CAP CD 10PF 20% 500V NPO | BECK | CD08CG10PCHMSCR | A | EA | 1 | |
| C27 | 00000N | NOT FITTED | | | | EA | - | |
| C28 | 120035 | CAP PC 22NF 1% 400V | ASHCROFT | M2B22004E | | EA | 2 | |
| C29 | 102220 | CAP CD 22PF 10% 500V N150 | BECK | CD08PG22P0KMSCR | A | EA | 3 | |
| C30 | 104017 | CAP CD 0P56F +/-0P1F 400V | BECK | GD08AG0P56BS | A | EA | 2 | |
| C31 | 102108 | CAP CD 1PF +/-0P5F 500V P100 | BECK | CD06AG01P0DMSCR | A | EA | 2 | |
| C32 | 102128 | CAP CD 1P8F +/-0P5F 500V | ITT | CD06AG01P8DMSCR | A | EA | 2 | |
| C33 | 102358 | CAP CD 3P9F +/-0P5F 500V P100 | BECK | CD08AG03P9DMSCR | A | EA | 2 | |
| C34 | 150020 | CAP DT 10UF 20% 25V | AVX | TAP10M25F | A | EA | - | |
| C35 | 100102 | CAP CP 1NF 10% 100V | PHILIPS | 2222 630 19102 | | EA | - | |
| C36 | 130083 | CAP PS 2NF 1% 160V | PHILIPS | 425 | | EA | 2 | |
| C37 | 110042 | CAP PE 100NF 20% 63V | WIMA | MKS2 0.1 20% 63V | | EA | 7 | |
| C38 | 00000N | NOT FITTED | | | | EA | - | |
| C39 | 100101 | CAP CP 100PF 2% 100V | PHILIPS | 2222 683 34101 | | EA | 3 | |
| C40 | 100278 | CAP CP 2P7F +/-0P25F 100V | PHILIPS | 2222 683 09278 | | EA | 2 | |
| C41 | 130084 | CAP PS 110PF 1% 630V | PHILIPS | 427 | | EA | 2 | |
| C42 | 130042 | CAP PS 100PF 1% 630V | SUFLEX | HS | | EA | 2 | |
| C43 | 102478 | CAP CD 4P7F +/-0P5F 500V NPO | BECK | CD08AG04P7DMSCR | A | EA | 2 | |
| C44 | 00000N | NOT FITTED | | | | EA | - | |
| C45 | 104026 | CAP CM 47NF +80%-20% 50V | AVX | SR175E473ZAA | A | EA | - | |
| C46 | 100102 | CAP CP 1NF 10% 100V | PHILIPS | 2222 630 19102 | | EA | - | |
| C47 | 150020 | CAP DT 10UF 20% 25V | AVX | TAP10M25F | A | EA | - | |
| C48 | 104026 | CAP CM 47NF +80%-20% 50V | AVX | SR175E473ZAA | A | EA | - | |
| C49 | 00000N | NOT FITTED | | | | EA | - | |
| C50 | 120034 | CAP PC 220NF 1% 63V | ASHCROFT | M2B22101E | | EA | - | |
| C51 | 120035 | CAP PC 22NF 1% 400V | ASHCROFT | M2B22004E | | EA | - | |
| C52 | 104017 | CAP CD 0P56F +/-0P1F 400V | BECK | GD08AG0P56BS | A | EA | - | |
| C53 | 104026 | CAP CM 47NF +80%-20% 50V | AVX | SR175E473ZAA | A | EA | - | |
| C54 | 00000N | NOT FITTED | | | | EA | - | |
| C55 | 104026 | CAP CM 47NF +80%-20% 50V | AVX | SR175E473ZAA | A | EA | - | |

| DESIG | PART NO | DESCRIPTION | PRINC MANUF | MANUF PART NUMBER | CLASS | UM | QUANTITY | CHANGES |
|-------|---------|-------------------------------|-------------|----------------------|-------|----|----------|---------|
| 156 | 101148 | CAP CD 10PF +/-0.05% 50V P100 | BECK | CD08A101P05SCR | A | EA | - | |
| 157 | 101148 | CAP CD 10PF +/-0.05% 50V | ITT | CD08A101P05SCR | A | EA | - | |
| 158 | 101148 | CAP CD 10PF +/-0.05% 50V P100 | BECK | CD08A101P05SCR | A | EA | - | |
| 159 | 104026 | CAP CM 47NF +80%-20% 50V | AVX | SR175E473ZAA | A | EA | - | |
| 160 | 104026 | CAP CM 47NF +80%-20% 50V | AVX | SR175E473ZAA | A | EA | - | |
| C61 | 00000N | NOT FITTED | | | | | | EA - |
| C62 | 130083 | CAP PS 2NF 1% 160V | PHILIPS | 425 | | EA | - | |
| C63 | 104026 | CAP CM 47NF +80%-20% 50V | AVX | SR175E473ZAA | A | EA | - | |
| C64 | 100102 | CAP CP 10PF 10% 100V | PHILIPS | 2222 683 34101 | | EA | - | |
| C65 | 100102 | CAP CP 10PF +/-0.05% 100V | PHILIPS | 2222 683 09278 | | EA | - | |
| C66 | 130084 | CAP PS 100PF 1% 630V | PHILIPS | 427 | | EA | - | |
| C67 | 130042 | CAP PS 100PF 1% 630V | SUFLEX | HS | | EA | - | |
| C68 | 102478 | CAP CD 47PF +/-0.5% 500V NPO | BECK | CD08AG04P7DSCR | A | EA | - | |
| C69 | 00000N | NOT FITTED | | | | | | EA - |
| C70 | 104026 | CAP CM 47NF +80%-20% 50V | AVX | SR175E473ZAA | A | EA | - | |
| C71 | 100102 | CAP CP 1NF 10% 100V | PHILIPS | 2222 630 19102 | | EA | - | |
| C72 | 150020 | CAP DT 10UF 20% 25V | AVX | TAP10M25F | A | EA | - | |
| C73 | 00000N | NOT FITTED | | | | | | EA - |
| C74 | 102220 | CAP CD 22PF 10% 500V N150 | BECK | CD08PG22P0KSCR | A | EA | - | |
| C75 | 100102 | CAP CP 1NF 10% 100V | PHILIPS | 2222 630 19102 | | EA | - | |
| C76 | 110041 | CAP PE 10NF 20% 100V | WIMA | FKS2 0.01 20% 100V | | EA | 3 | |
| C77 | 102102 | CAP CD 1NF 10% 500V | BECK | CD10K101N0KSCR | A | EA | 1 | |
| C78 | 110041 | CAP PE 10NF 20% 100V | WIMA | FKS2 0.01 20% 100V | | EA | - | |
| C79 | 100102 | CAP CP 1NF 10% 100V | PHILIPS | 2222 630 19102 | | EA | - | |
| C80 | 110042 | CAP PE 100NF 20% 63V | WIMA | MKS2 0.1 20% 63V | | EA | - | |
| C81 | 100102 | CAP CP 1NF 10% 100V | PHILIPS | 2222 630 19102 | | EA | - | |
| C82 | 100182 | CAP CP 1NF 10% 100V | PHILIPS | 2222 630 19182 | | EA | 1 | |
| C83 | 100102 | CAP CP 1NF 10% 100V | PHILIPS | 2222 630 19102 | | EA | - | |
| C84 | 100102 | CAP CP 1NF 10% 100V | PHILIPS | 2222 630 19102 | | EA | - | |
| C85 | 100102 | CAP CP 1NF 10% 100V | PHILIPS | 2222 630 19102 | | EA | - | |
| C86 | 102221 | CAP CD 220PF 10% 500V N3300 | BECK | CD10DL220PKSCR | A | EA | 2 | |
| C87 | 104026 | CAP CM 47NF +80%-20% 50V | AVX | SR175E473ZAA | A | EA | - | |
| C88 | 104026 | CAP CM 47NF +80%-20% 50V | AVX | SR175E473ZAA | A | EA | - | |
| C89 | 110046 | CAP PE 10UF 20% 50V | WIMA | MKS2 1.0 20% 50V | | EA | 1 | |
| C90 | 104026 | CAP CM 47NF +80%-20% 50V | AVX | SR175E473ZAA | A | EA | - | |
| C91 | 104026 | CAP CM 47NF +80%-20% 50V | AVX | SR175E473ZAA | A | EA | - | |
| C92 | 102331 | CAP CD 330PF 20% 500V K1 | BECK | CD08K1330PKSCR | A | EA | 1 | |
| C93 | 104026 | CAP CM 47NF +80%-20% 50V | AVX | SR175E473ZAA | A | EA | - | |
| C94 | 104026 | CAP CM 47NF +80%-20% 50V | AVX | SR175E473ZAA | A | EA | - | |
| C95 | 101103 | CAP CD 10NF -20%-80% 250V | BECK | CD10K310N02SCR/SK250 | | EA | 1 | |
| C96 | 150010 | CAP DT 330NF 20% 35V | AVX | TAP33M35F | A | EA | 1 | |
| C97 | 100101 | CAP CP 100PF 20% 100V | PHILIPS | 2222 683 34101 | | EA | - | |
| C98 | 110042 | CAP PE 100NF 20% 63V | WIMA | MKS2 0.1 20% 63V | | EA | - | |
| C99 | 110042 | CAP PE 100NF 20% 63V | WIMA | MKS2 0.1 20% 63V | | EA | - | |
| C100 | 104026 | CAP CM 47NF +80%-20% 50V | AVX | SR175E473ZAA | A | EA | - | |

GATRON INSTRUMENTS LTD PARTS LIST 07-Jan-92 DESIG: ASSY PCB SINE SOURCE 4700 DRG NO: LP400446-11 REV: 5 PAGE NO: 7

| DESIG | PART NO | DESCRIPTION | PRINC MANUF | MANUF PART NUMBER | CLASS | UM | QUANTITY | CHANGES |
|-------|---------|-------------------------------|-------------|--------------------|-------|----|----------|---------|
| C101 | 104026 | CAP CM 47NF +80%-20% 50V | AVX | SR175E473ZAA | A | EA | - | |
| C102 | 150020 | CAP DT 10UF 20% 25V | AVX | TAP10M25F | A | EA | - | |
| C103 | 150020 | CAP DT 10UF 20% 25V | AVX | TAP10M25F | A | EA | - | |
| C104 | 00000N | NOT FITTED | | | | | | EA - |
| C105 | 104026 | CAP CM 47NF +80%-20% 50V | AVX | SR175E473ZAA | A | EA | - | |
| C106 | 100102 | CAP CP 1NF 10% 100V | PHILIPS | 2222 630 19102 | | EA | - | |
| C107 | 110042 | CAP PE 100NF 20% 63V | WIMA | MKS2 0.1 20% 63V | | EA | 1 | |
| C108 | 110015 | CAP PE 15NF 20% 63V | WIMA | MKS2 0.015 20% 63V | | EA | - | |
| C109 | 110041 | CAP PE 10NF 20% 100V | WIMA | FKS2 0.01 20% 100V | | EA | 1 | |
| C110 | 104064 | CAP CD 12PF 5% 50V | AVX | SR215A120JAA | | | | |
| C111 | 110042 | CAP PE 100NF 20% 63V | WIMA | MKS2 0.1 20% 63V | | EA | - | |
| C112 | 102221 | CAP CD 220PF 10% 500V N3300 | BECK | CD10DL220PKSCR | A | EA | - | |
| C113 | 104026 | CAP CM 47NF +80%-20% 50V | AVX | SR175E473ZAA | A | EA | - | |
| C114 | 104026 | CAP CM 47NF +80%-20% 50V | AVX | SR175E473ZAA | A | EA | - | |
| C115 | 150015 | CAP DT 10UF 20% 35V | AVX | TAP10M35F | A | EA | 1 | |
| C116 | 00000N | NOT FITTED | | | | | | EA - |
| C117 | 100102 | CAP CP 1NF 10% 100V | PHILIPS | 2222 630 19102 | | EA | - | |
| C118 | 104026 | CAP CM 47NF +80%-20% 50V | AVX | SR175E473ZAA | A | EA | - | |
| C119 | 102338 | CAP CD 3P3F +/-0.5% 500V P100 | BECK | CD08AG03P3DSCR | A | EA | 1 | |
| C120 | 104026 | CAP CM 47NF +80%-20% 50V | AVX | SR175E473ZAA | A | EA | - | |
| C121 | 150023 | CAP DT 33UF 20% 25V | AVX | TAP33M25F | A | EA | 3 | |
| C122 | 150023 | CAP DT 33UF 20% 25V | AVX | TAP33M25F | A | EA | - | |
| C123 | 150020 | CAP DT 10UF 20% 25V | AVX | TAP10M25F | A | EA | - | |
| C124 | 104026 | CAP CM 47NF +80%-20% 50V | AVX | SR175E473ZAA | A | EA | - | |
| C125 | 150020 | CAP DT 10UF 20% 25V | AVX | TAP10M25F | A | EA | - | |
| C126 | 150023 | CAP DT 33UF 20% 25V | AVX | TAP33M25F | A | EA | - | |
| C127 | 102220 | CAP CD 22PF 10% 500V N150 | BECK | CD08PG22P0KSCR | A | EA | - | |
| C128 | 104026 | CAP CM 47NF +80%-20% 50V | AVX | SR175E473ZAA | A | EA | - | |
| C129 | 150021 | CAP DT 22UF 20% 25V | AVX | TAP22M25F | A | EA | 1 | |
| C130 | 110042 | CAP PE 100NF 20% 63V | WIMA | MKS2 0.1 20% 63V | | EA | - | |
| C131 | 100102 | CAP CP 1NF 10% 100V | PHILIPS | 2222 630 19102 | | EA | - | |
| C132 | 00000N | NOT FITTED | | | | | | EA - |
| C134 | 120029 | CAP PC 6N8F 20% 100V | WIMA | FKC2 6800 20% 100V | | EA | 1 | |
| C135 | 150020 | CAP DT 10UF 20% 25V | AVX | TAP10M25F | A | EA | - | |
| C136 | 104026 | CAP CM 47NF +80%-20% 50V | AVX | SR175E473ZAA | A | EA | - | |
| C137 | 150020 | CAP DT 10UF 20% 25V | AVX | TAP10M25F | A | EA | - | |
| C138 | 150020 | CAP DT 10UF 20% 25V | AVX | TAP10M25F | A | EA | - | |
| C139 | 104026 | CAP CM 47NF +80%-20% 50V | AVX | SR175E473ZAA | A | EA | - | |
| D2 | 210091 | DIODE 2N 9V1 400mW | PHILIPS | B2X79C9V1 | A | EA | 3 | |
| D3 | 210150 | DIODE 2N 15V 400mW | PHILIPS | B2X79C15 | A | EA | 1 | |
| D4 | 210091 | DIODE 2N 9V1 400mW | PHILIPS | B2X79C9V1 | A | EA | - | |
| D5 | 213009 | DIODE TS 15V 5/500W | UNITRODE | TVS515 | A | EA | 4 | |
| D6 | 213009 | DIODE TS 15V 5/500W | UNITRODE | TVS515 | A | EA | - | |
| D7 | 200001 | DIODE GP 75mA 75V | FAIRCHILD | 1N4148 | | EA | 15 | |
| D8 | 200001 | DIODE GP 75mA 75V | FAIRCHILD | 1N4148 | | EA | - | |

| DESIG | PART NO | DESCRIPTION | PRINC MANUF | MANUF PART NUMBER | CLASS | UM | QUANTITY | CHANGES |
|-------|---------|---------------------|-------------|-------------------|-------|----|----------|---------|
| D10 | 210001 | DIODE 1N 473 400mW | FAIRCHILD | 1N4148 | | EA | - | |
| D11 | 210043 | DIODE 1N 473 400mW | PHILIPS | BZX79C4V3 | A | EA | 4 | |
| D12 | 200001 | DIODE GP 75mA 75V | FAIRCHILD | 1N4148 | | EA | - | |
| D13 | 210043 | DIODE 1N 473 400mW | PHILIPS | BZX79C4V3 | A | EA | - | |
| D13 | 200001 | DIODE GP 75mA 75V | FAIRCHILD | 1N4148 | | EA | - | |
| D14 | 200001 | DIODE GP 75mA 75V | FAIRCHILD | 1N4148 | | EA | - | |
| D15 | 200001 | DIODE GP 75mA 75V | FAIRCHILD | 1N4148 | | EA | - | |
| D16 | 210043 | DIODE 1N 473 400mW | PHILIPS | BZX79C4V3 | A | EA | - | |
| D17 | 200001 | DIODE GP 75mA 75V | FAIRCHILD | 1N4148 | | EA | - | |
| D18 | 210043 | DIODE 1N 473 400mW | PHILIPS | BZX79C4V3 | A | EA | - | |
| D19 | 210091 | DIODE 1N 9V1 400mW | PHILIPS | BZX79C9V1 | A | EA | - | |
| D20 | 213011 | DIODE VR 1V4 250mW | PHILIPS | BZV86-1V4 | | EA | 2 | |
| D21 | 200001 | DIODE GP 75mA 75V | FAIRCHILD | 1N4148 | | EA | - | |
| D22 | 213011 | DIODE VR 1V4 250mW | PHILIPS | BZV86-1V4 | | EA | - | |
| D23 | 200001 | DIODE GP 75mA 75V | FAIRCHILD | 1N4148 | | EA | - | |
| D24 | 210056 | DIODE 1N 5V6 400mW | PHILIPS | BZX79C5V6 | A | EA | 2 | |
| D25 | 210056 | DIODE 1N 5V6 400mW | PHILIPS | BZX79C5V6 | A | EA | - | |
| D26 | 213023 | DIODE 1N 6V4 100PPM | PHILIPS | BZV10 | | EA | 2 | |
| D27 | 213009 | DIODE TS 15V 5/500W | UNITRODE | TVS515 | A | EA | - | |
| D28 | 220010 | DIODE SB | HP | 1N5711/1N6263 | A | EA | 3 | |
| D29 | 220010 | DIODE SB | HP | 1N5711/1N6263 | A | EA | - | |
| D30 | 213023 | DIODE 1N 6V4 100PPM | PHILIPS | BZV10 | | EA | - | |
| D31 | 200001 | DIODE GP 75mA 75V | FAIRCHILD | 1N4148 | | EA | - | |
| D32 | 200001 | DIODE GP 75mA 75V | FAIRCHILD | 1N4148 | | EA | - | |
| D33 | 200001 | DIODE GP 75mA 75V | FAIRCHILD | 1N4148 | | EA | - | |
| D34 | 213009 | DIODE TS 15V 5/500W | UNITRODE | TVS515 | A | EA | - | |
| D35 | 200001 | DIODE GP 75mA 75V | FAIRCHILD | 1N4148 | | EA | - | |
| D36 | 200006 | DIODE GP 1A 600V | FAIRCHILD | 1N4005 | | EA | 2 | |
| D37 | 200006 | DIODE GP 1A 600V | FAIRCHILD | 1N4005 | | EA | - | |
| D38 | 220010 | DIODE SB | HP | 1N5711/1N6263 | A | EA | - | |
| D39 | 213012 | DIODE VR 2V0 250mW | PHILIPS | BZV86-2V0 | | EA | 2 | |
| D40 | 210062 | DIODE 1N 6V2 400mW | PHILIPS | BZX79C6V2 | A | EA | 2 | |
| D41 | 210062 | DIODE 1N 6V2 400mW | PHILIPS | BZX79C6V2 | A | EA | - | |
| D42 | 213012 | DIODE VR 2V0 250mW | PHILIPS | BZV86-2V0 | | EA | - | |
| D43 | 210068 | DIODE 1N 6V8 400mW | PHILIPS | BZX79C6V8 | A | EA | 1 | |
| D44 | 200001 | DIODE GP 75mA 75V | FAIRCHILD | 1N4148 | | EA | - | |
| Q1 | 230035 | TRAN JFET N-CHAN | TELEDYNE | U1897JF | | EA | 35 | |
| Q2 | 230035 | TRAN JFET N-CHAN | TELEDYNE | U1897JF | | EA | - | |
| Q3 | 230035 | TRAN JFET N-CHAN | TELEDYNE | U1897JF | | EA | - | |
| Q4 | 230035 | TRAN JFET N-CHAN | TELEDYNE | U1897JF | | EA | - | |
| Q5 | 250004 | TRAN PNP TO92 | MOTOROLA | 2N3906 | | EA | 6 | |
| Q6 | 250004 | TRAN PNP TO92 | MOTOROLA | 2N3906 | | EA | - | |
| Q7 | 240006 | TRAN NPN TO92 | MOTOROLA | 2N3904 | | EA | 4 | |
| Q8 | 230035 | TRAN JFET N-CHAN | TELEDYNE | U1897JF | | EA | - | |
| Q9 | 230035 | TRAN JFET N-CHAN | TELEDYNE | U1897JF | | EA | - | |

| DESIG | PART NO | DESCRIPTION | PRINC MANUF | MANUF PART NUMBER | CLASS | UM | QUANTITY | CHANGES |
|-------|----------|-----------------------------|-------------|-------------------|-------|----|----------|---------|
| Q18 | 250004 | TRAN PNP TO92 | MOTOROLA | 2N3906 | | EA | - | |
| Q19 | 230001 | TRAN JFET I LIM 1.4mA | SILICONIX | J506 | | EA | 3 | |
| Q20 | 230035 | TRAN JFET N-CHAN | TELEDYNE | U1897JF | | EA | - | |
| Q21 | 230035 | TRAN JFET N-CHAN | TELEDYNE | U1897JF | | EA | - | |
| Q22 | 230035 | TRAN JFET N-CHAN | TELEDYNE | U1897JF | | EA | - | |
| Q23 | 230035 | TRAN JFET N-CHAN | TELEDYNE | U1897JF | | EA | - | |
| Q24 | 230035 | TRAN JFET N-CHAN | TELEDYNE | U1897JF | | EA | - | |
| Q25 | 230035 | TRAN JFET N-CHAN | TELEDYNE | U1897JF | | EA | - | |
| Q26 | 230035 | TRAN JFET N-CHAN | TELEDYNE | U1897JF | | EA | - | |
| Q27 | 230035 | TRAN JFET N-CHAN | TELEDYNE | U1897JF | | EA | - | |
| Q28 | 230035 | TRAN JFET N-CHAN | TELEDYNE | U1897JF | | EA | - | |
| Q29 | 239060-1 | TRAN JFET N-CHAN DUAL - RES | DATRON | SEE DRG | | S2 | - | |
| Q30 | 260060 | IC LIM I SOURCE | NATIONAL | LM334H | | EA | 1 | |
| Q31 | 240043 | TRAN NPN TO92 RESERVE STOCK | MOTOROLA | 2N3904 | | EA | 2 | |
| Q32 | 230035 | TRAN JFET N-CHAN | TELEDYNE | U1897JF | | EA | - | |
| Q33 | 230035 | TRAN JFET N-CHAN | TELEDYNE | U1897JF | | EA | - | |
| Q34 | 230035 | TRAN JFET N-CHAN | TELEDYNE | U1897JF | | EA | - | |
| Q35 | 230035 | TRAN JFET N-CHAN | TELEDYNE | U1897JF | | EA | - | |
| Q36 | 230035 | TRAN JFET N-CHAN | TELEDYNE | U1897JF | | EA | - | |
| Q37 | 230035 | TRAN JFET N-CHAN | TELEDYNE | U1897JF | | EA | - | |
| Q38 | 230035 | TRAN JFET N-CHAN | TELEDYNE | U1897JF | | EA | - | |
| Q39 | 230035 | TRAN JFET N-CHAN | TELEDYNE | U1897JF | | EA | - | |
| Q40 | 230035 | TRAN JFET N-CHAN | TELEDYNE | U1897JF | | EA | - | |
| Q41 | 230046 | TRAN JFET N-CHAN DUAL | SILICONIX | VCR11N | | EA | 1 | |
| Q42 | 230001 | TRAN JFET I LIM 1.4mA | SILICONIX | J506 | | EA | - | |
| Q43 | 230001 | TRAN JFET I LIM 1.4mA | SILICONIX | J506 | | EA | - | |
| Q44 | 240043 | TRAN NPN TO92 RESERVE STOCK | MOTOROLA | 2N3904 | | EA | - | |
| Q45 | 250001 | TRAN PNP | MOTOROLA | BC214 | | EA | 3 | |
| Q46 | 250001 | TRAN PNP | MOTOROLA | BC214 | | EA | - | |
| Q47 | 230035 | TRAN JFET N-CHAN | TELEDYNE | U1897JF | | EA | - | |
| Q48 | 230035 | TRAN JFET N-CHAN | TELEDYNE | U1897JF | | EA | - | |
| Q49 | 230035 | TRAN JFET N-CHAN | TELEDYNE | U1897JF | | EA | - | |
| Q50 | 230035 | TRAN JFET N-CHAN | TELEDYNE | U1897JF | | EA | - | |
| Q51 | 230035 | TRAN JFET N-CHAN | TELEDYNE | U1897JF | | EA | - | |
| Q52 | 230035 | TRAN JFET N-CHAN | TELEDYNE | U1897JF | | EA | - | |
| Q53 | 230035 | TRAN JFET N-CHAN | TELEDYNE | U1897JF | | EA | - | |
| Q54 | 250004 | TRAN PNP TO92 | MOTOROLA | 2N3906 | | EA | - | |
| Q55 | 240017 | TRAN NPN | NATIONAL | LM394H | | EA | 6 | |
| Q56 | 240017 | TRAN NPN | NATIONAL | LM394H | | EA | - | |
| Q57 | 240017 | TRAN NPN | NATIONAL | LM394H | | EA | - | |
| Q58 | 240017 | TRAN NPN | NATIONAL | LM394H | | EA | - | |
| Q59 | 240017 | TRAN NPN | NATIONAL | LM394H | | EA | - | |
| Q60 | 240017 | TRAN NPN | NATIONAL | LM394H | | EA | - | |
| Q61 | 230050 | TRAN JFET I LIM 2mA | SILICONIX | J508 | | EA | 1 | |
| Q62 | 240013 | TRAN NPN TO18 | MOTOROLA | BC184C | | EA | 4 | |

| DESIG | PART NO | DESCRIPTION | PRINC MANUF | MANUF PART NUMBER | CLASS | UM | QUANTITY | CHANGES |
|-------|----------|------------------------------|-------------|-------------------|-------|----|----------|---------|
| Q63 | 240013 | TRAN NPN TO18 | MOTOROLA | BC184C | EA | - | | |
| Q64 | 240013 | TRAN NPN TO18 | MOTOROLA | BC184C | EA | - | | |
| Q65 | 240013 | TRAN NPN TO18 | MOTOROLA | BC184C | EA | - | | |
| Q66 | 230042 | TRAN JFET I LIM 3mA | SILICONIX | J509 | EA | 6 | | |
| Q67 | 230035 | TRAN JFET N-CHAN | TELEDYNE | U1897JF | EA | - | | |
| Q68 | 230035 | TRAN JFET N-CHAN | TELEDYNE | U1897JF | EA | - | | |
| Q69 | 230035 | TRAN JFET N-CHAN | TELEDYNE | U1897JF | EA | - | | |
| Q70 | 240006 | TRAN NPN TO92 | MOTOROLA | 2N3904 | EA | 2 | | |
| Q71 | 250009 | TRAN PNP TO18 | MOTOROLA | BC214C | EA | - | | |
| Q72 | 250008 | TRAN PNP TO18 | MOTOROLA | BC214C | EA | - | | |
| Q73 | 230042 | TRAN JFET I LIM 3mA | SILICONIX | J509 | EA | - | | |
| Q74 | 230033 | TRAN JFET N CHAN | TELEDYNE | U1899JF | EA | 1 | | |
| Q75 | 240026 | TRAN NPN TO92 | MOTOROLA | 2N3904 | EA | - | | |
| Q76 | 239059-1 | TRAN JFET N-CHAN DUAL X 2 | DATRON | SEE DRG | S2 | 1 | | |
| Q77 | 239059-1 | TRAN JFET N-CHAN DUAL X 2 | DATRON | SEE DRG | S2 | - | | |
| Q78 | 240032 | TRAN NPN | MOTOROLA | BF393 | EA | 4 | | |
| Q79 | 240032 | TRAN NPN | MOTOROLA | BF393 | EA | - | | |
| Q80 | 240032 | TRAN NPN | MOTOROLA | BF393 | EA | - | | |
| Q81 | 240032 | TRAN NPN | MOTOROLA | BF393 | EA | - | | |
| Q82 | 230042 | TRAN JFET I LIM 3mA | SILICONIX | J509 | EA | - | | |
| Q83 | 240001 | TRAN NPN | MOTOROLA | BC184 | EA | 2 | | |
| Q84 | 230042 | TRAN JFET I LIM 3mA | SILICONIX | J509 | EA | - | | |
| Q85 | 250001 | TRAN PNP | MOTOROLA | BC214 | EA | - | | |
| Q86 | 240031 | TRAN NPN | MOTOROLA | BD139 | EA | 2 | | |
| Q87 | 230042 | TRAN JFET I LIM 3mA | SILICONIX | J509 | EA | - | | |
| Q88 | 240006 | TRAN NPN TO92 | MOTOROLA | 2N3904 | EA | - | | |
| Q89 | 230042 | TRAN JFET I LIM 3mA | SILICONIX | J509 | EA | - | | |
| Q90 | 250004 | TRAN PNP TO92 | MOTOROLA | 2N3906 | EA | - | | |
| Q91 | 240001 | TRAN NPN | MOTOROLA | BC184 | EA | - | | |
| Q92 | 250004 | TRAN PNP TO92 | MOTOROLA | 2N3906 | EA | - | | |
| Q93 | 240031 | TRAN NPN | MOTOROLA | BD139 | EA | - | | |
| Q94 | 250021 | TRAN PNP | MOTOROLA | BD140 | EA | 1 | | |
| Q95 | 230035 | TRAN JFET N-CHAN | TELEDYNE | U1897JF | EA | - | | |
| M1 | 280101 | IC DIG COUNT DEC BIN PL X2 | MOTOROLA | MC14569BCP | EA | 3 | | |
| M2 | 280057 | IC DIG COUNT4 SYNC DEC PL UD | MOTOROLA | MC14510BCP | EA | 1 | | |
| M3 | 280008 | IC DIG NAND2 X4 | MOTOROLA | MC14011BCP | EA | 1 | | |
| M4 | 280011 | IC DIG FLIP FLOP D X2 | MOTOROLA | MC14013BCP | EA | 2 | | |
| M5 | 280101 | IC DIG COUNT DEC BIN PL X2 | MOTOROLA | MC14569BCP | EA | - | | |
| M6 | 280076 | IC DIG MUX 8TO1 ANALOG | MOTOROLA | MC14051BCL | A | EA | 2 | |
| M7 | 280079 | IC DIG OR2 X4 | MOTOROLA | MC14071BCP | EA | 1 | | |
| M8 | 280076 | IC DIG MUX 8TO1 ANALOG | MOTOROLA | MC14051BCL | A | EA | - | |
| M9 | 280101 | IC DIG COUNT DEC BIN PL X2 | MOTOROLA | MC14569BCP | EA | - | | |
| M10 | 280025 | IC DIG SWITCH QUAD CMOS | MOTOROLA | MC14066BCP | EA | 1 | | |
| M11 | 280197 | IC DIG PHASE LOCKED LOOP | PHILIPS | 74HCT4046AP | EA | 1 | | |
| M12 | 280125 | IC DIG PHASE DETECTOR | NATIONAL | MM74C932N | EA | 1 | | |

DATRON INSTRUMENTS LTD PARTS LIST 07-Jan-92 DESC: ASSY PCB SINE SOURCE 4700 DRG NO: LP400446-11 REV: 5 PAGE NO: 11

| DESIG | PART NO | DESCRIPTION | PRINC MANUF | MANUF PART NUMBER | CLASS | UM | QUANTITY | CHANGES |
|-------|----------|-----------------------------|-----------------|-------------------|--------|----|----------|---------|
| M13 | 280011 | IC DIG FLIP FLOP D X2 | MOTOROLA | MC14013BCP | EA | - | | |
| M14 | 280080 | IC DIG HEX SCHMITT TRIGGER | NATIONAL | 74C14N | EA | 2 | | |
| M15 | 260046 | IC LIN OP AMP | HARRIS | HA3 2525-5 | EA | 3 | | |
| M16 | 260076 | IC LIN I MIRROR 1:1 | TEXAS | TL011CLP | EA | 4 | | |
| M17 | 290090 | IC DIG DRIVER DARLINGTON X7 | EXAR | XR2202CP | A | EA | 4 | |
| M18 | 260076 | IC LIN I MIRROR 1:1 | TEXAS | TL011CLP | EA | - | | |
| M19 | 260134 | IC LIN OP AMP FET IP F/SET | ANALOG DEVICES | AD744JN | A | EA | 2 | |
| M20 | 290090 | IC DIG DRIVER DARLINGTON X7 | EXAR | XR2202CP | EA | - | | |
| M21 | 280080 | IC DIG HEX SCHMITT TRIGGER | NATIONAL | 74C14N | EA | - | | |
| M22 | 260087 | IC LIN OP AMP BIFET | MOTOROLA | MC34081P | EA | 5 | | |
| M23 | 260133 | IC LIN OP AMP | MOTOROLA | MC34080P | EA | 2 | | |
| M24 | 260087 | IC LIN OP AMP BIFET | MOTOROLA | MC34081P | EA | - | | |
| M25 | 260087 | IC LIN OP AMP BIFET | MOTOROLA | MC34081P | EA | - | | |
| M26 | 260076 | IC LIN I MIRROR 1:1 | TEXAS | TL011CLP | EA | - | | |
| M27 | 260076 | IC LIN I MIRROR 1:1 | TEXAS | TL011CLP | EA | - | | |
| M28 | 290090 | IC DIG DRIVER DARLINGTON X7 | EXAR | XR2202CP | A | EA | - | |
| M29 | 280035 | IC DIG DECODER BCDTODEC | MOTOROLA | MC14028BCP | EA | 1 | | |
| M30 | 260134 | IC LIN OP AMP FET IP F/SET | ANALOG DEVICES | AD744JN | EA | - | | |
| M31 | 260133 | IC LIN OP AMP | MOTOROLA | MC34080P | EA | - | | |
| M32 | 260057 | IC LIN OP AMP | SIGNETICS | NE5534N | EA | 1 | | |
| M33 | 290090 | IC DIG DRIVER DARLINGTON X7 | EXAR | XR2202CP | A | EA | - | |
| M34 | 290000 | TRAN NPN ARRAY X 5 | SILICON GENERAL | SG3083J | A | EA | 2 | |
| M35 | 260042 | IC LIN OP AMP DUAL | SIGNETICS | NE5532N | EA | 2 | | |
| M36 | 280023 | IC DIG NOR2 QUAD | MOTOROLA | MC14001UBCP | EA | 1 | | |
| M37 | 260078 | IC LIN V COMP DUAL | NATIONAL | LM393AN | EA | 1 | | |
| M38 | 280126 | IC DIG DAC | ANALOG DEVICES | AD7527LN | A | EA | 1 | |
| M39 | 260033 | IC LIN REG 5V .1A | MOTOROLA | MC78L05ACP | A | EA | 3 | |
| M40 | 290000 | TRAN NPN ARRAY X 5 | SILICON GENERAL | SG3083J | A | EA | - | |
| M41 | 260042 | IC LIN OP AMP DUAL | SIGNETICS | NE5532N | EA | - | | |
| M42 | 280127 | IC DIG DAC MULT 10BIT | ANALOG DEVICES | AD7533JN | EA | 2 | | |
| M43 | 280127 | IC DIG DAC MULT 10BIT | ANALOG DEVICES | AD7533JN | EA | - | | |
| M44 | 260087 | IC LIN OP AMP BIFET | MOTOROLA | MC34081P | A | EA | - | |
| M45 | 260027 | IC LIN OP AMP | FAIRCHILD | UA714HC | EA | 1 | | |
| M46 | 260046 | IC LIN OP AMP | HARRIS | HA3 2525-5 | EA | - | | |
| M47 | 260087 | IC LIN OP AMP BIFET | MOTOROLA | MC34081P | EA | - | | |
| M48 | 260046 | IC LIN OP AMP | NATIONAL | LM319N | EA | 1 | | |
| M49 | 260049 | IC LIN V COMP DUAL | MOTOROLA | MC78L05ACP | A | EA | - | |
| M50 | 260033 | IC LIN REG 5V .1A | MOTOROLA | MC78L05ACP | A | EA | - | |
| M51 | 260033 | IC LIN REG 5V .1A | MOTOROLA | MC78L05ACP | EA | - | | |
| RL1 | 330012-3 | RELAY 1PNO REED GUARDED | HAMLIN | HE721A5134 | TO DRG | EA | 8 | |
| RL2 | 330012-3 | RELAY 1PNO REED GUARDED | HAMLIN | HE721A5134 | TO DRG | EA | - | |
| RL3 | 330012-3 | RELAY 1PNO REED GUARDED | HAMLIN | HE721A5134 | TO DRG | EA | - | |
| RL4 | 330012-3 | RELAY 1PNO REED GUARDED | HAMLIN | HE721A5134 | TO DRG | EA | - | |
| RL5 | 330012-3 | RELAY 1PNO REED GUARDED | HAMLIN | HE721A5134 | TO DRG | EA | - | |
| RL6 | 330012-3 | RELAY 1PNO REED GUARDED | HAMLIN | HE721A5134 | TO DRG | EA | - | |

| DESIGN | PART NO | DESCRIPTION | PRINC MANUF | MANUF PART NUMBER | CLASS | UM | QUANTITY | CHANGES |
|--------|-----------|-----------------------------|----------------------|-------------------|-------|----|----------|---------|
| R17 | 330012-3 | RELAY 1P4C REED GUARDED | HAMLIN | HE721AS134 TO DRG | EA | - | | |
| R18 | 330012-3 | RELAY 1P4C REED GUARDED | HAMLIN | HE721AS134 TO DRG | EA | - | | |
| L1 | 370003 | CHCKE RF 1mH 43R | SIGMA | SC10 | EA | 2 | | |
| L2 | 370001 | CHCKE RF 10UH | SIGMA | SC10/25 | A | EA | 6 | |
| L3 | 370001 | CHCKE RF 10UH | SIGMA | SC10/25 | A | EA | - | |
| L4 | 370001 | CHCKE RF 10UH | SIGMA | SC10/25 | A | EA | - | |
| L5 | 370001 | CHCKE RF 10UH | SIGMA | SC10/25 | A | EA | - | |
| L6 | 370001 | CHCKE RF 10UH | SIGMA | SC10/25 | A | EA | - | |
| L7 | 370026 | CHCKE RF 1UH 990MA | SIGMA | SC10 | EA | 1 | | |
| L8 | 370003 | CHCKE RF 1mH 43R | SIGMA | SC10 | EA | - | | |
| L9 | 370001 | CHCKE RF 10UH | SIGMA | SC10/25 | A | EA | - | |
| | 410171-12 | PCB SINE SOURCE 4000 | | SEE DRG | EA | 1 | | |
| | 420098 | LABEL SERIAL/ASSY No | RS COMPONENTS | 554-793 | EA | 1 | | |
| | 420112-1 | LABEL SSD WARNING 12 X 12mm | TEKNIS | LN1212 | A | EA | 1 | |
| | 450450-1 | HEATSINK SINE SOURCE 4200 | | SEE DRG | EA | 1 | | |
| | 450841-1 | SCREEN SINE SOURCE 4700 | | SEE DRG | EA | 1 | | |
| | 512999 | WIRE 7/2 PTFE 1KV WHT | BSG210 | TYPE C | AR | 1 | | |
| | 540002 | WIRE 1/.7 TINNED COPPER | BS4109 | 22SWG | AR | 1 | | |
| | 590001 | SLEEVE NP 1.5 X 20MM BLK | HELLERMANN | H15 X 20MM BLK | EA | 1 | | |
| | 602001 | TERMINAL FSV | MILL-MAX | 1165015013002102 | A | EA | 8 | |
| | 604046 | PLUG PCB 3-WAY .1" | MOLEX | 22-10-2031 | EA | 2 | | |
| | 605059 | SOCKET PCB 9-WAY DIL | JERMYN | J23-18008 | A | EA | 17 | |
| | 605060 | SOCKET PCB 14-WAY DIL | JERMYN | J23-18014 | A | EA | 9 | |
| | 605061 | SOCKET PCB 16-WAY DIL | JERMYN | J23-18016 | A | EA | 16 | |
| | 605065 | SOCKET PCB 28-WAY DIL | JERMYN | J23-18028 | A | EA | 1 | |
| | 605127 | SOCKET LINK 2-WAY .1" BLK | ASSMANN | AKSPL-G | EA | 2 | | |
| | 611007 | SCREW M3 X 6 PCZ1CSK SZP | | | EA | 4 | | |
| | 611016 | SCREW M3 X 8 PCZ1PAN SZP | | | EA | 2 | | |
| | 611025 | SCREW M3 X 16 PCZ1CSK SZP | | | EA | 1 | | |
| | 612004-1 | STANDOFF M3 X 4 | | SEE DRG | EA | 4 | | |
| | 612026-1 | STANDOFF M3 X 6 | | SEE DRG | EA | 1 | | |
| | 613005 | WASHER M3 INT SHAKP SZP | | | EA | 2 | | |
| | 615002 | NUT FULL M3 SZP | | | EA | 2 | | |
| | 620003 | PIN SOLDER | MILL-MAX | 3130200010000080 | EA | 2 | | |
| | 620007 | TEST POINT TERMINAL | MICROVAR | TYPE C30 | EA | 31 | | |
| | 630024 | BEAD CERAMIC 16 SWG | PARK ROYAL PORCELAIN | No2/D0006 | EA | 8 | | |
| | 630107 | STRIP BRASS 15.5 X 0.38mm | RIGHTON | CZ108 1/2H | AR | 1 | | |
| | 630120 | PCB EJECTOR YELLOW | RICHCO | CBE | EA | 2 | | |
| | 900003 | HEATSINK COMPOUND | RS COMPONENTS | 554-311 | AR | 1 | | |
| | 920089-1 | HEATSINK TO220 | THERMALLOY | 6073B | EA | 2 | | |

End

| DESIG | PART NO | DESCRIPTION | PRINC MANUF | MANUF PART NUMBER | CLASS | UM | QUANTITY | CHANGES |
|-------|-----------|-----------------------------|----------------------|-------------------|-------|----|----------|---------|
| R17 | 330012-3 | RELAY 1PNC REED GUARDED | HAMLIN | HE721A5134 TO DRG | | | | EA - |
| R18 | 330012-3 | RELAY 1PNC REED GUARDED | HAMLIN | HE721A5134 TO DRG | | | | EA - |
| L1 | 370003 | CHCKE RF 1mH 40R | SIGMA | SC10 | | | | EA 2 |
| L2 | 370001 | CHCKE RF 10UH | SIGMA | SC10/25 | A | | | EA 6 |
| L3 | 370001 | CHCKE RF 10UH | SIGMA | SC10/25 | A | | | EA - |
| L4 | 370001 | CHCKE RF 10UH | SIGMA | SC10/25 | A | | | EA - |
| L5 | 370001 | CHCKE RF 10UH | SIGMA | SC10/25 | A | | | EA - |
| L6 | 370001 | CHCKE RF 10UH | SIGMA | SC10/25 | A | | | EA - |
| L7 | 370026 | CHCKE RF 1UH 890mA | SIGMA | SC10 | | | | EA 1 |
| L8 | 370003 | CHCKE RF 1mH 40R | SIGMA | SC10 | | | | EA - |
| L9 | 370001 | CHCKE RF 10UH | SIGMA | SC10/25 | A | | | EA - |
| | 410171-12 | PCB SINE SOURCE 4300 | | SEE DRG | | | | EA 1 |
| | 420098 | LABEL SERIAL/ASSY No | RS COMPONENTS | 534-793 | | | | EA 1 |
| | 420112-1 | LABEL SSD WARNING 12 X 12mm | TEKNIS | LN1212 | A | | | EA 1 |
| | 450450-1 | HEATSINK SINE SOURCE 4200 | | SEE DRG | | | | EA 1 |
| | 450841-1 | SCREEN SINE SOURCE 4700 | | SEE DRG | | | | EA 1 |
| | 512999 | WIRE 7/.2 PTFE 1KV WHT | BSG210 | TYPE C | | | | AR 1 |
| | 540002 | WIRE 1/.7 TINNED COPPER | BS4109 | 22SWG | | | | AR 1 |
| | 590001 | SLEEVE NP 1.5 X 20MM BLK | HELLERMANN | H15 X 20MM BLK | | | | EA 1 |
| | 620001 | TERMINAL PSV | MILL-MAX | 1065015013002102 | A | | | EA 8 |
| | 604046 | PLUG PCB 3-WAY .1" | MOLLEX | 22-10-2031 | | | | EA 2 |
| | 605059 | SOCKET PCB 3-WAY DIL | JERMYN | J23-18008 | A | | | EA 17 |
| | 605060 | SOCKET PCB 14-WAY DIL | JERMYN | J23-18014 | A | | | EA 9 |
| | 605061 | SOCKET PCB 16-WAY DIL | JERMYN | J23-18016 | A | | | EA 16 |
| | 605065 | SOCKET PCB 28-WAY DIL | JERMYN | J23-18028 | A | | | EA 1 |
| | 605127 | SOCKET LINK 2-WAY .1" BLK | ASSMANN | AKSPL-G | | | | EA 2 |
| | 611007 | SCREW M3 X 6 POZICSK SZP | | | | | | EA 4 |
| | 611016 | SCREW M3 X 8 POZIPAN SZP | | | | | | EA 2 |
| | 611025 | SCREW M3 X 16 POZICSK SZP | | | | | | EA 1 |
| | 612004-1 | STANDOFF M3 X 4 | | SEE DRG | | | | EA 4 |
| | 612026-1 | STANDOFF M3 X 6 | | SEE DRG | | | | EA 1 |
| | 613005 | WASHER M3 INT SHAKP SZP | | | | | | EA 2 |
| | 615002 | NUT FULL M3 SZP | | | | | | EA 2 |
| | 620003 | PIN SOLDER | MILL-MAX | 3130200010000080 | | | | EA 2 |
| | 620007 | TEST POINT TERMINAL | MICROVAR | TYPE C30 | | | | EA 31 |
| | 630024 | BEAD CERAMIC 16 SWG | PARK ROYAL PORCELAIN | №2/D0006 | | | | EA 8 |
| | 630107 | STRIP BRASS 15.5 X 0.38mm | RIGHTON | C2108 1/2H | | | | AR 1 |
| | 630120 | PCB EJECTOR YELLOW | RICHCO | CBE | | | | EA 2 |
| | 900003 | HEATSINK COMPOUND | RS COMPONENTS | 554-311 | | | | AR 1 |
| | 920089-1 | HEATSINK TO220 | THERMALLOY | 6073B | | | | EA 2 |

End

