SECTION 3
CIRCUIT DESCRIPTIONS

3.1 INTRODUCTION

This section discusses the four major circuits that make up the Model 2100/2110. These four circuits are: measurement, motherboard, CRT, and power supply. Each of the discussions that follow, start by presenting a block diagram, then continue with a discussion of the operation of the major blocks within each diagram.

3.2 MEASUREMENT OVERVIEW

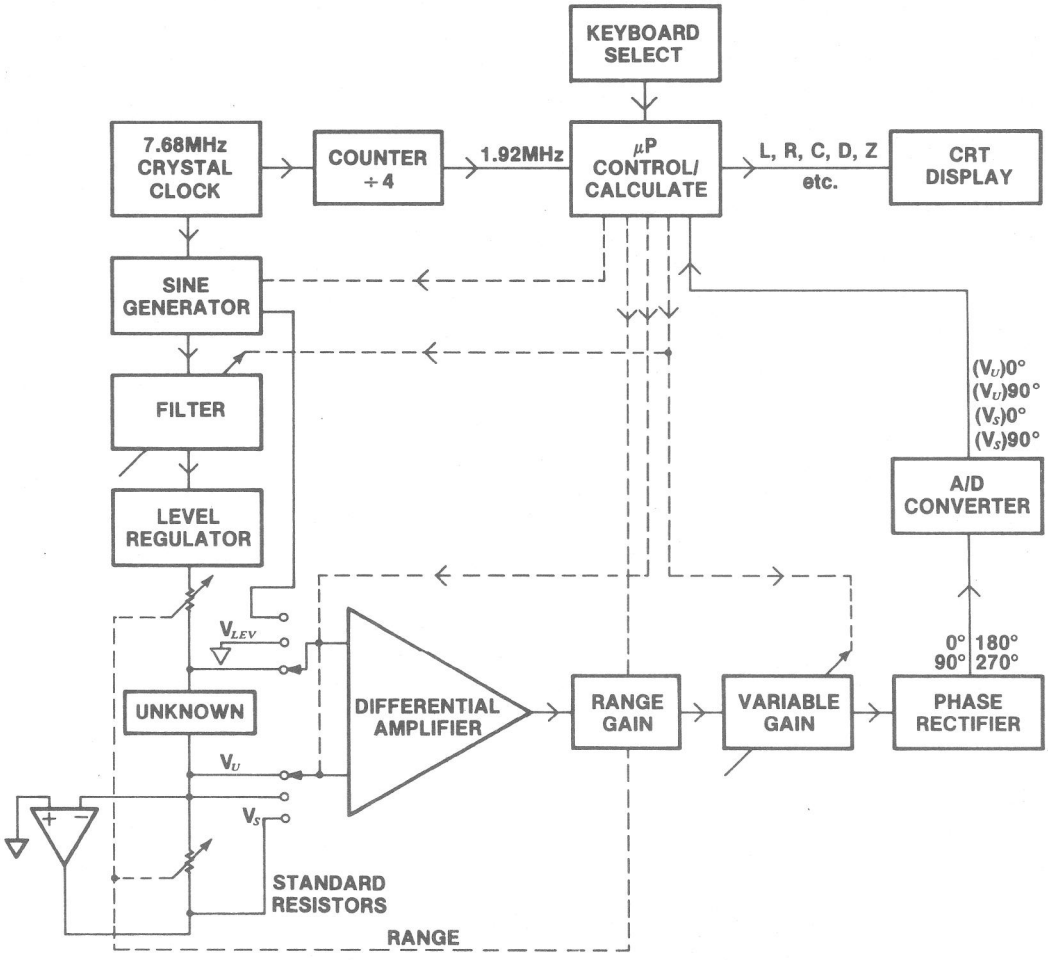


Figure 3-1. Block Diagram

The microcomputer control/calculate block is the command center for all instrument operations. It accepts input from the keyboard and coordinates all phases of a measurement sequence. It also performs all calculations required to arrive at the desired measured quantities and displays them.

Model 2100/2110 operation essentially starts with the 7.68MHz clock. This clock is divided by 4 to obtain the 1.9MHz processor clock and divided by N (3-3000) to develop the sinewave measurement signal.

The sinewave generator is frequency programmable (20Hz to 20kHz). It produces a digitally-stairstepped, sinewave output that is band limited by the filter block, then passed through the programmable level regulator. The result is a sinewave signal of specified frequency within a specified voltage range, in the mV mode, or current range, in the mA mode. This sinewave is applied to the unknown component being measured, and the standard (range) resistor.

A differential amplifier sequentially measures the voltages across the unknown component and the standard resistor. These voltages are passed through the range gain and variable gain amplifiers to the phase rectifier. The phase sensitive voltmeter (phase rectifier) compares the vector relationships of the measured signals to determine which portions are in phase and which are in quadrature. The phase rectifier outputs the following four DC voltages:

V_0 or $V_{\text{unknown } 0°}$
V_1 or $V_{\text{unknown } 90°}$
V_2 or $V_{\text{standard } 0°}$
V_3 or $V_{\text{standard } 90°}$

These voltages are serially processed by the A/D converter with resistance (R) and reactance (X), when in the mA mode, or conductance (G) and susceptance (B), when in the mV mode, computed by the Z8Ø CPU.

mV MODE

$$G_{unknown} = \frac{V_{\emptyset}\ V_2 + V_1\ V_3}{(V_{\emptyset})^2 + (V_1)^2} \times R_{standard}$$

$$B_{unknown} = \frac{V_{\emptyset}\ V_3 - V_1\ V_2}{(V_{\emptyset})^2 + (V_1)^2} \times R_{standard}$$

mA MODE

$$R_{unknown} = \frac{V_{\emptyset}\ V_2 + V_1\ V_3}{(V_2)^2 + (V_3)^2} \times R_{standard}$$

$$X_{unknown} = \frac{V_1\ V_2 - V_{\emptyset}\ V_3}{(V_2)^2 + (V_3)^2} \times R_{standard}$$

All other impedance parameters are computed using the results of these measurements, the test frequency, and the formulas in Figure 1-1.

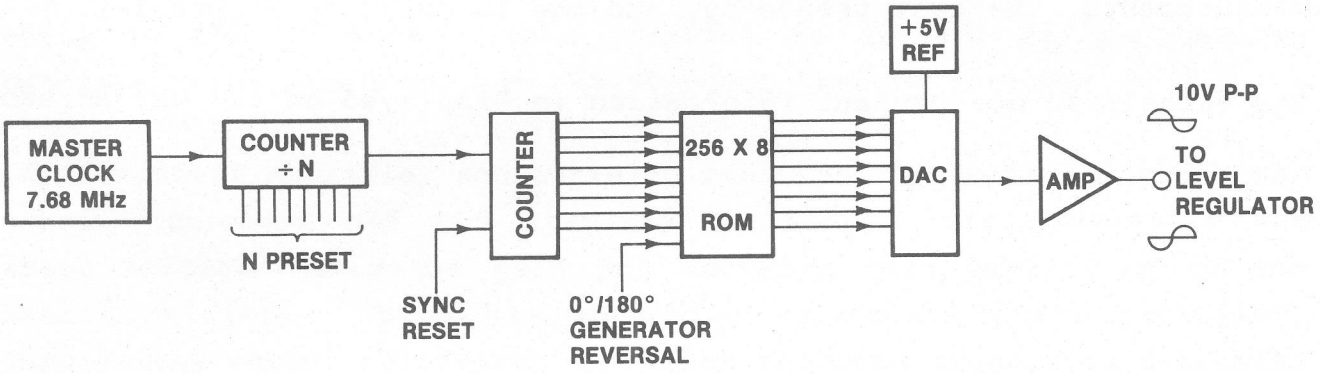
The calculated measurement information is displayed on the CRT screen.

3.3 MEASUREMENT CIRCUITRY

The electronics involved with the actual measuring of a component is contained on two circuit cards. The Digital circuit card performs two basic functions: sinewave generation, and analog-to-digital conversion. The Analog circuit card holds all other measurement circuitry, i.e. level regulator, standard (range) resistors, amplifiers, phase rectifier, etc., needed to make a measurement.

3.3.1 Digital Circuit Card (P/N 45237)

3.3.1.1 Sine Generator



$$\text{FREQUENCY} = \frac{60{,}000\ \text{Hz}}{N}$$

N = 3 ⇒ 3000
N = 1 F = 60,000 Hz
N = 3 F = 20,000 Hz
N = 3000 F = 20 Hz

$$\frac{7.68\text{MHz}}{128\ (\text{STEPS IN ONE COMPLETE SINEWAVE})} = 60{,}000\text{Hz}$$

Figure 3-2. Sine Generator Block Diagram

Measurement begins when a sinewave signal at a specified frequency is applied to the unknown component. The origin of this sinewave signal is the sine generator (Figure 3-2) which consists of a preset counter chain, a second counter, a 256 x 8 bit preprogrammed ROM, a digital-to-analog converter (DAC), and a current-to-voltage buffer amplifier. The preset counter chain (U22, U24, U25) is a set of three chips configured to perform a divide-by-N function. It divides the 7.68MHz master clock into one of the 2998 frequencies that are presettable by the microcomputer. The new frequency, actually a squarewave signal, goes into a second counter chain made of U16 and U19. The second counter is connected to U17, a read only memory (ROM), in such a way that as the counter's output lines toggle, they ripple through all the addresses on the ROM. For each address the ROM outputs 8 bits of information which are fed to the D/A converter.

Two complete sinewave signals are stored in the 74S471 ROM. The 256 x 8 bit memory block reserves 128 address locations for the Ø° sinewave and 128 locations for the 18Ø° sinewave. Each address location contains 8 bits of information.

NOTE: 7.68MHz divided by 128 sinewave address locations equals the 6ØkHz base frequency used to determine test frequency.

$$\frac{6ØkHz}{N} = \text{Test Frequency}$$

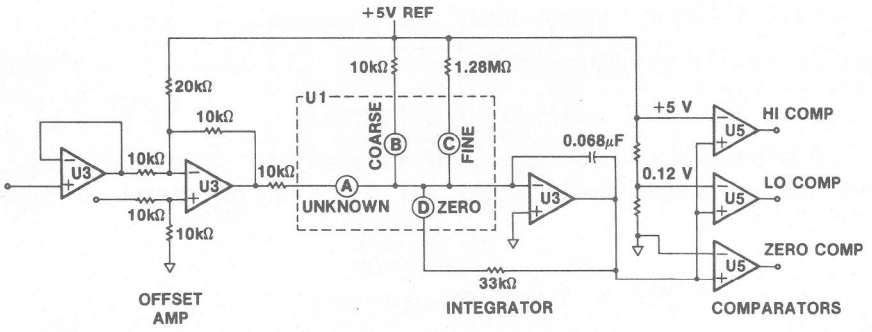
Where: N = 3 to 3ØØØ

Notice in Figure 3-2 that the counter and the ROM each have an input line coming from outside the sine generator electronics. The Ø°/18Ø° line to the ROM, under microcomputer control, selects the polarity of the ROM's output sinewave, Ø° or 18Ø°. This is the generator reversal routine where the sinewave polarity is reversed for a second series of measurements. The two series of measurements, made with opposite polarities, are algebraically added to cancel offset voltages and synchronized line related pick-up.

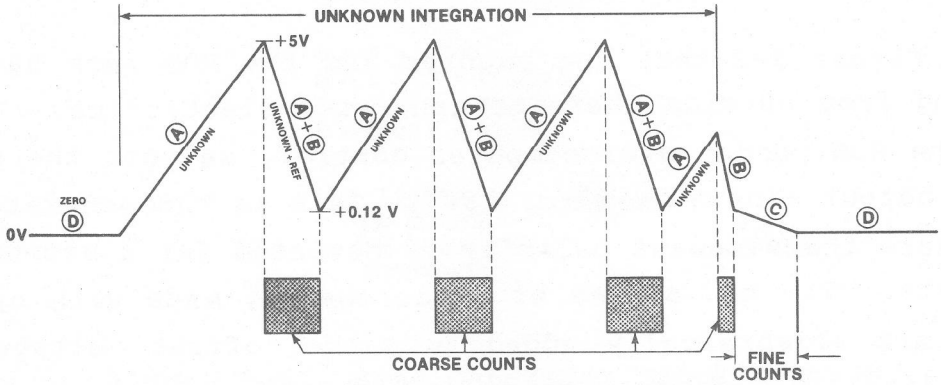
The sync reset line to the counter is use to synchronize the 2100/2110 sinewave to the power line. At frequencies below 200Hz, the 2100/2110 detects power line zero crossings and starts its sinewave at these exact points. This is accomplished by resetting the counter at the first power line zero crossing after a completed measurement cycle. Test signal/power line synchronization maximizes rejection of line related EMI coupled to the measurement circuit.

The digital-to-analog converter (DAC) is the analog device that produces the actual waveform. It works with operational amplifier U14 to transform the DAC's current output into a voltage waveform. The sinewave output from the sine generator is 10V peak-to-peak and is symmetrical around zero.

3.3.1.2 Analog-to-Digital Converter



SIMPLIFIED A/D CONVERTER



TOTAL COUNT = 1024 = COARSE COUNTS + FINE COUNTS

INTEGRATOR WAVEFORM

Figure 3-3. A/D Converter Simplified Diagram

The analog-to-digital converter is called a "charge balancing" A/D converter (see Figure 3-3). Moving from left to right on the diagram, the offset amplifier, two sections of quad-amplifier U3, offsets the DC input voltages, from the phase rectifier, so they always remain one polarity. Solid state switch, U1, selects inputs, i.e. unknown signal, standard signal, coarse reference, fine reference, or zero, to the third section of U3, the integrator. Three comparator sections of U5, and logic U7, U8, U6, and U11 (see schematic diagram in Section 5 of this manual), synchronize the turning ON and OFF of coarse and fine counters with the switching of coarse and fine reference inputs to the integrator. Counter timer, U29, has 3 channels: two channels are counters, one for coarse counts, and one for fine counts during A/D conversion, and the third channel sets up, through the bus system, the number of multiples of test frequency over which the integrator will integrate. The 2100/2110 is locked into exact multiples of the test cycle or test frequency because it is the test frequency that determines the actual integration time. The Digital assembly also contains support logic for the A/D converter. The support logic interfaces the A/D converter's output to the microcomputer, and performs level shifting for the drive signals to the input (reference) switches on the integrator. The easiest way to step through the A/D conversion sequence is to follow the integrator waveform (in Figure 3-3). The circled letters on the waveform correspond to the input (reference) switches in the simplified diagram.

The integrator waveform starts from the ØV level. When switch A is turned ON, the integrator starts ramping toward the +5V level. (Switch A allows the unknown signal, a DC voltage from the phase rectifier, to pass to the integrator.) Upon reaching the +5V level a comparator, called "HI COMP", causes the logic to turn switch B, the coarse reference, ON. With both switches ON, the integrator ramps back down toward zero. It ramps down to approximately +Ø.12V where the "LO COMP" comparator trips turning the B switch OFF. With the A switch ON by itself again, the integrator ramps back up toward +5V. Switch B comes back ON at the +5V level, and the integrator ramps down toward zero. The object of this switching technique is to keep the integrator in bounds, between +5V and +Ø.12V, for the duration of the unknown integration. This allows longer integration times without the integrator going out of range and provides a wide choice of integration times and also provides shorter total integration time due to the overlap of the reference signal with the unknown integration.

At the end of the unknown integration, switch A is turned OFF. (It remained ON during the unknown integration.) Now, since the integrator is still above the ØV level, switch B is turned ON driving the integrator to the Ø.12V level, then is turned OFF and switch C is turned ON. Switch C is called "fine" reference. The fine reference brings the integrator back to ØV.

The relationship between coarse and fine reference levels lies in the fact that they each have an associated counter. Each time the B switch is turned ON, a counter is being gated to keep track, by accumulating counts, of how long switch B was on. (In Figure 3-3, the waveform has four bursts of coarse counts, three of which are roughly the same level, the fourth is a finish off of the coarse counts.) The fine counter also accumulates counts when switch C is turned ON. The relationship, for counts, is one coarse count equals 1,Ø24 fine counts.

Where does this 1,Ø24 count relationship come from?

Looking carefully at the coarse and fine reference levels, you find that the coarse and fine differ by only 128 counts, not by 1,Ø24. The clocks associated with the coarse counter and the fine counter are not the same, one clock is 12Ø kHz, that is the coarse count clock, and the fine clock is 8 times that or 96Ø kHz. As a result there is a factor-of-8 difference, and 8 times 128 equals 1,Ø24 counts.

The total of all coarse and fine counts constitutes a measured value. Accumulated counts for each of the four measured values ($V_{unknown\ Ø°}$, $V_{unknown\ 9Ø°}$, $V_{standard\ Ø°}$, $V_{standard\ 9Ø°}$) are sent to the microcomputer.

3.3.2 Analog Circuit Card (P/N 45239)

3.3.2.1 Signal to the Unknown

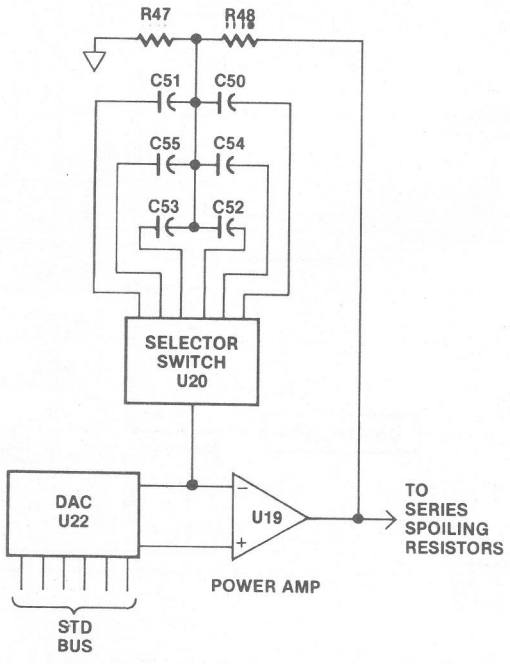


Figure 3-4. Level set, Filter, and Power Amplifier Block Diagram

As the sinewave from the sine generator comes onto the Analog circuit card, it goes through a level-setting DAC. The level-set DAC is under microcomputer control and can reduce the test signal to any one of 256 predetermined test levels. Level-set DAC, U22, is ganged with U17, the variable gain DAC, so that as the test signal level is reduced, the measured signal can be amplified by the same amount for further processing.

The level-set DAC outputs a stairstepped sinewave that must be filtered before it can be used. The Analog assembly has three filters that can be selected for this job. Filter selection is dependent on the test signal frequency such that C50 and C51 are selected at frequencies between 20Hz and 200Hz, C54 and C55 between 200Hz and 2kHz, and C52 and C53 between 2kHz and 20kHz. The filtered sinewave is sent to the power amplifier.

Power amplifier U19 is designed to supply enough current out through the HI DRIVE port to the unknown that a measurement can be made. The power amplifier also supplies a signal to the high side of the standard (range) resistors.

3.3.2.2 Range Switching

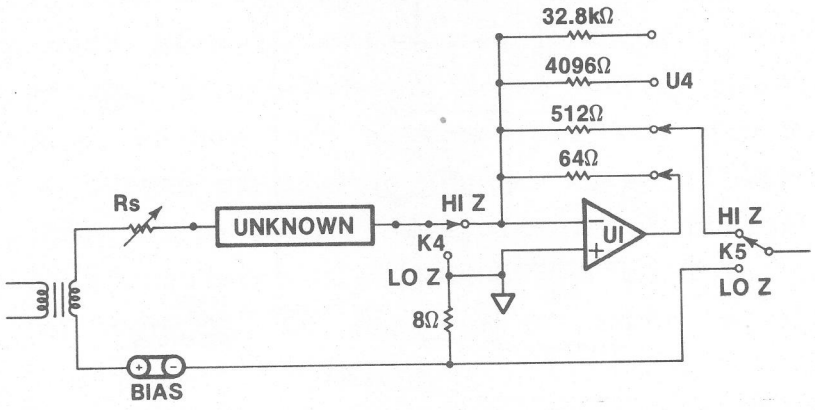


Figure 3-5. Range Switching Block Diagram

Figure 3-5 illustrates the range switching used in the 2100/2110. The diagram shows, basically, two bridge configurations or two measurement configurations, a HI Z and a LO Z configuration. Anytime the 8Ω standard resistor (measuring unknowns from 0Ω to about 32Ω) is used, relay K4 switches to the LO Z configuration. All measurements above 32Ω use the other standard resistors or the HI Z configuration. Standard resistors used in the HI Z configuration are 64Ω, 512Ω, 4.096kΩ, and 32.8kΩ. The 64Ω standard resistor is switched in/out of the circuit by relay K5, while the 512Ω, 4.096kΩ, and 32.8kΩ resistors are switched by solid state switch U4. Any ranges beyond those represented by actual resistors are the result of a range gain multiplier.

3.3.2.3 Range Gain

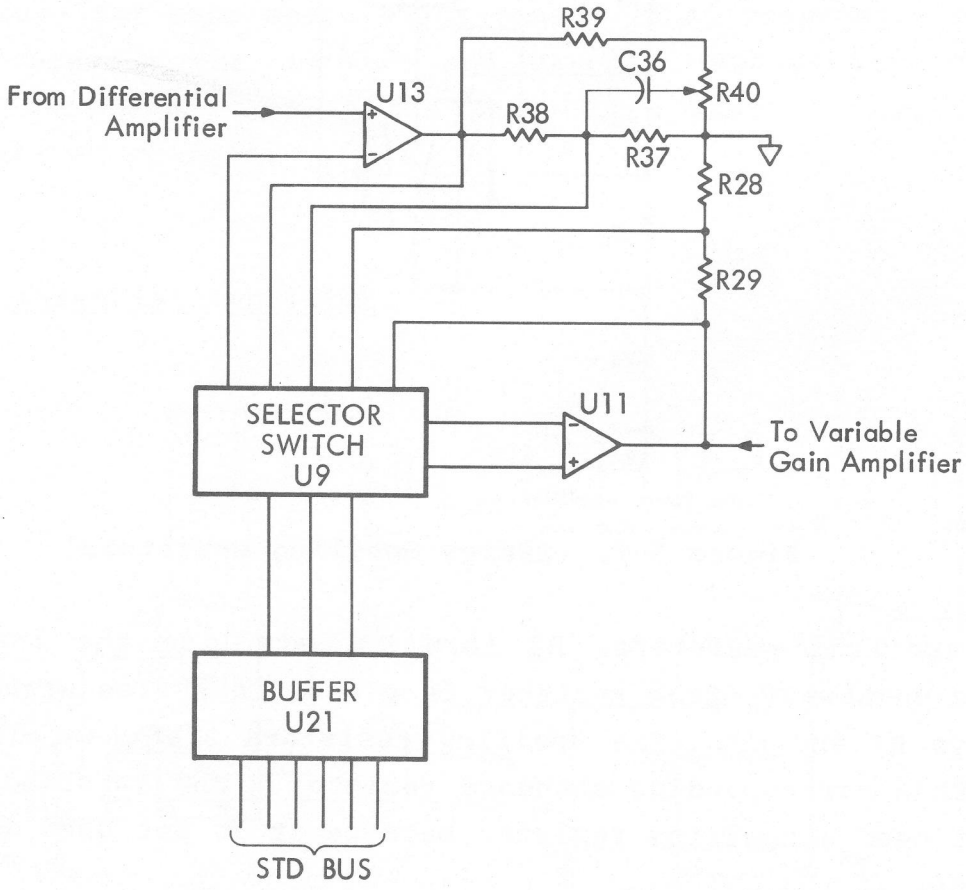


Figure 3-6. Range Gain Amplifier

The range gain amplifier, U11, U13, and U9, sets up gains of 1/8, 8, or 64 in conjunction with the range resistors to produce the 2100/2110's eight measurement ranges. Each multiplier is an exact power of 8 so that when combined with a standard resistor it provides measurement ranges between 0.125Ω and 262kΩ. The range gain amplifier is bus connected thru buffer U21 and receives programmed instructions from the microcomputer.

3.3.2.4 Series Spoiling Resistors

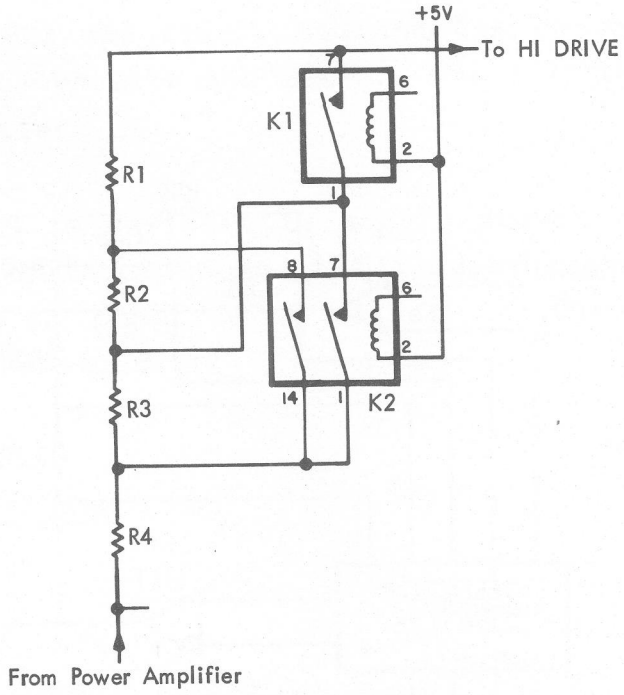


Figure 3-7. Series Spoiling Resistors

Series spoiling resistors, R1 thru R4, stablize the instrument for reactive unknowns. Each resistor is placed in series with the unknown by relays K1 and K2. The spoiling resistors are changed in conjunction with a corresponding standard resistor. The 8Ω standard resistor does not need a spoiling resistor because it is not used in U1's feedback loop.

3.3.2.5 Phase Trims

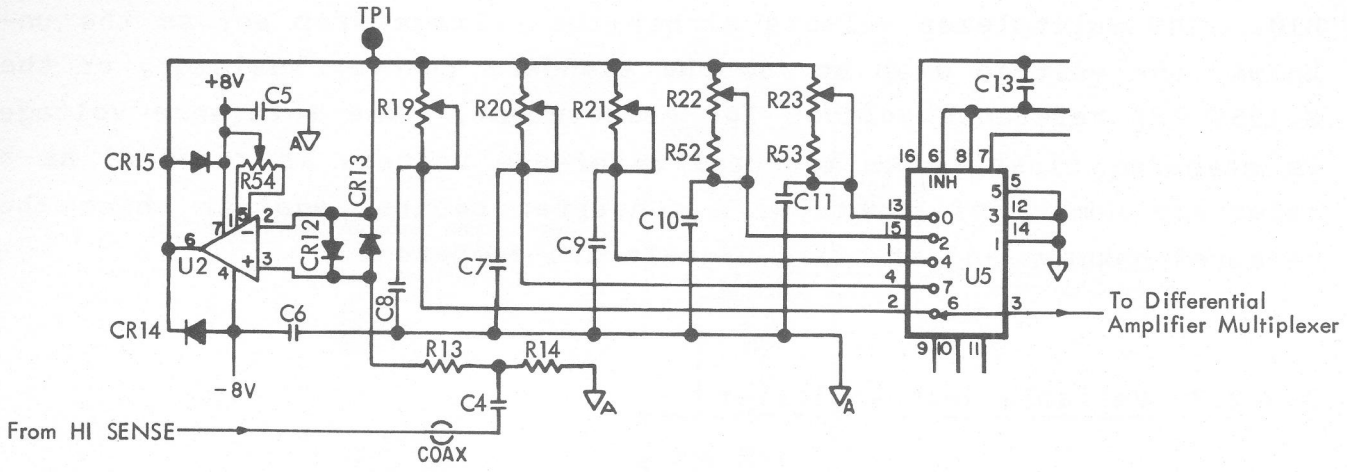


Figure 3-8. Phase Trims

Phase calibration trimmers R19 thru R23 and R40 calibrate dissipation factor accuracy for each measurement range. They compensate for phase differences between the unknown and standard measurement channels. Solid state switch U5 changes the phase trim when the corresponding range resistor is changed.

3.3.2.6 Differential Amplifier

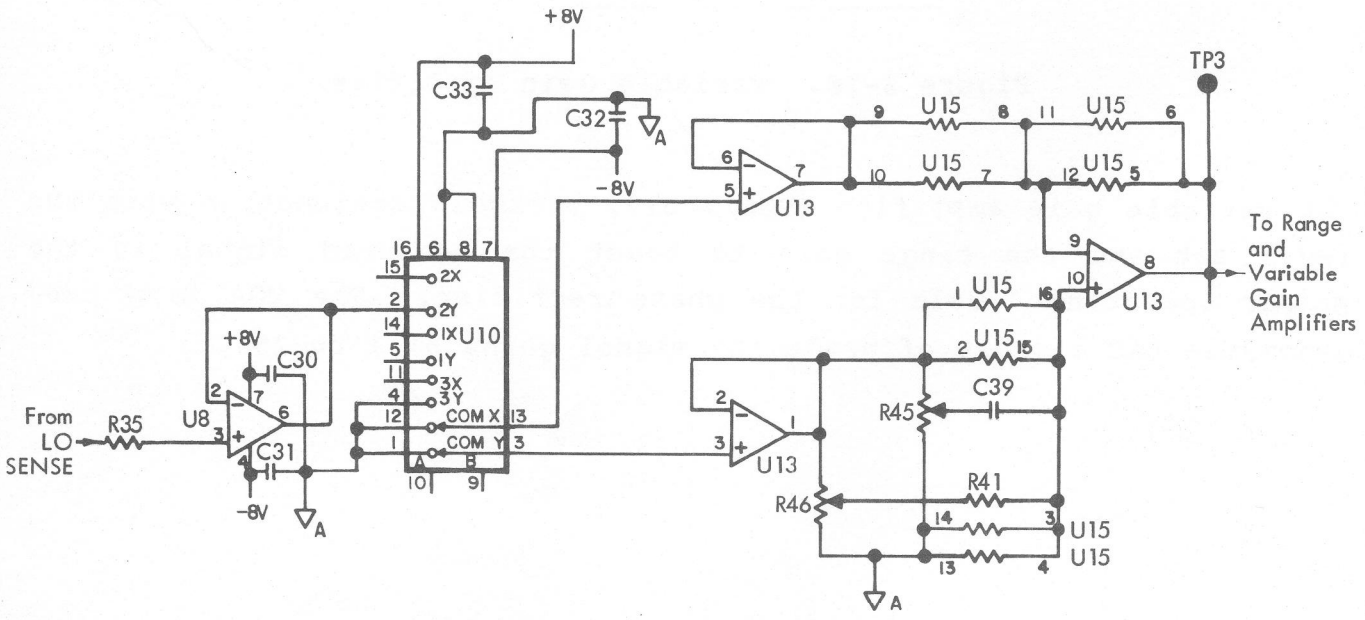


Figure 3-9. Differential Amplifier

The differential amplifier consists of 3 sections of quad-amplifier U13. It's input is sequentially selected by the input multiplexer U10. The mulitplexer selects either the voltage drop across the unknown, the voltage drop across the standard (range) resistor, or the 0.125V RMS reference voltage for measurement. The reference voltage is measured first. The measured reference voltage is recorded as a reference number of counts (A/D converter counts) against which the measured unknown and standard signals are compared.

3.3.2.7 Variable Gain Amplifier

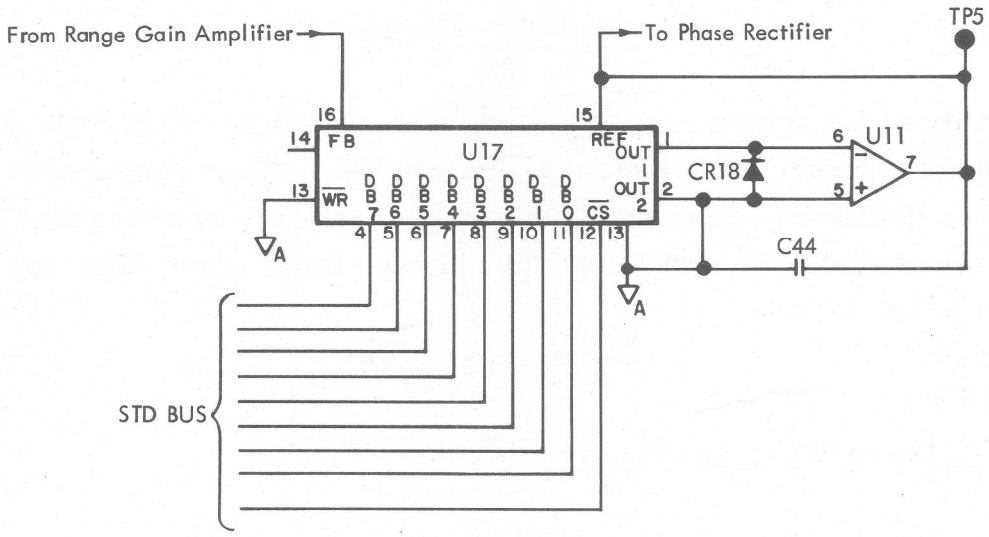


Figure 3-10. Variable Gain Amplifier

The variable gain amplifier (VGA), U17, works in conjunction with the level set and the range gain to boost the measured signal to the proper operating levels for the phase rectifier. The VGA is a programmable DAC capable of producing signal gains of 1 to 256.

3.3.2.8 Overload Detector

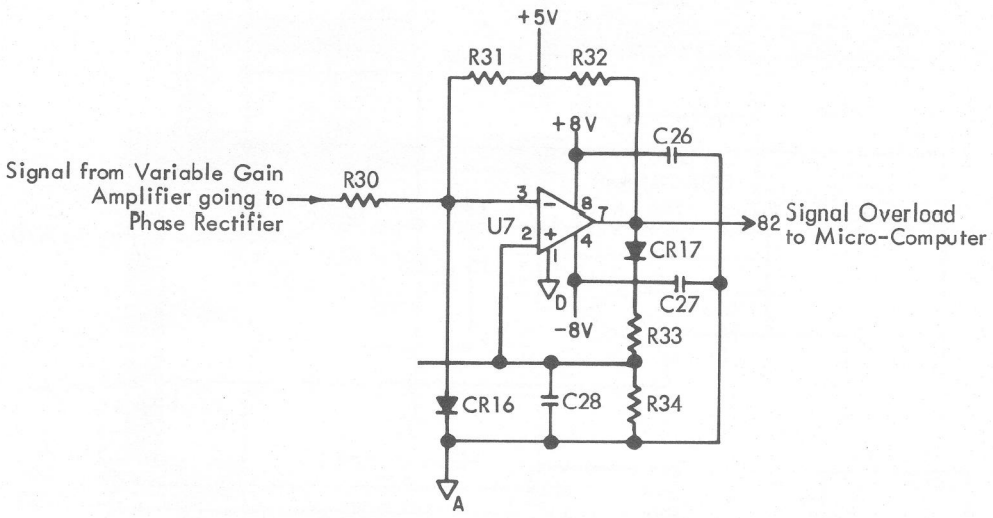


Figure 3-11. Overload Detector

Overload detector U7 monitors the signal going from the output of the variable gain amplifier to the phase rectifier. This peak detector indicates overload when the signal is too high. The detector's output goes HI when an overload occurs.

3.3.2.9 Phase Rectifier

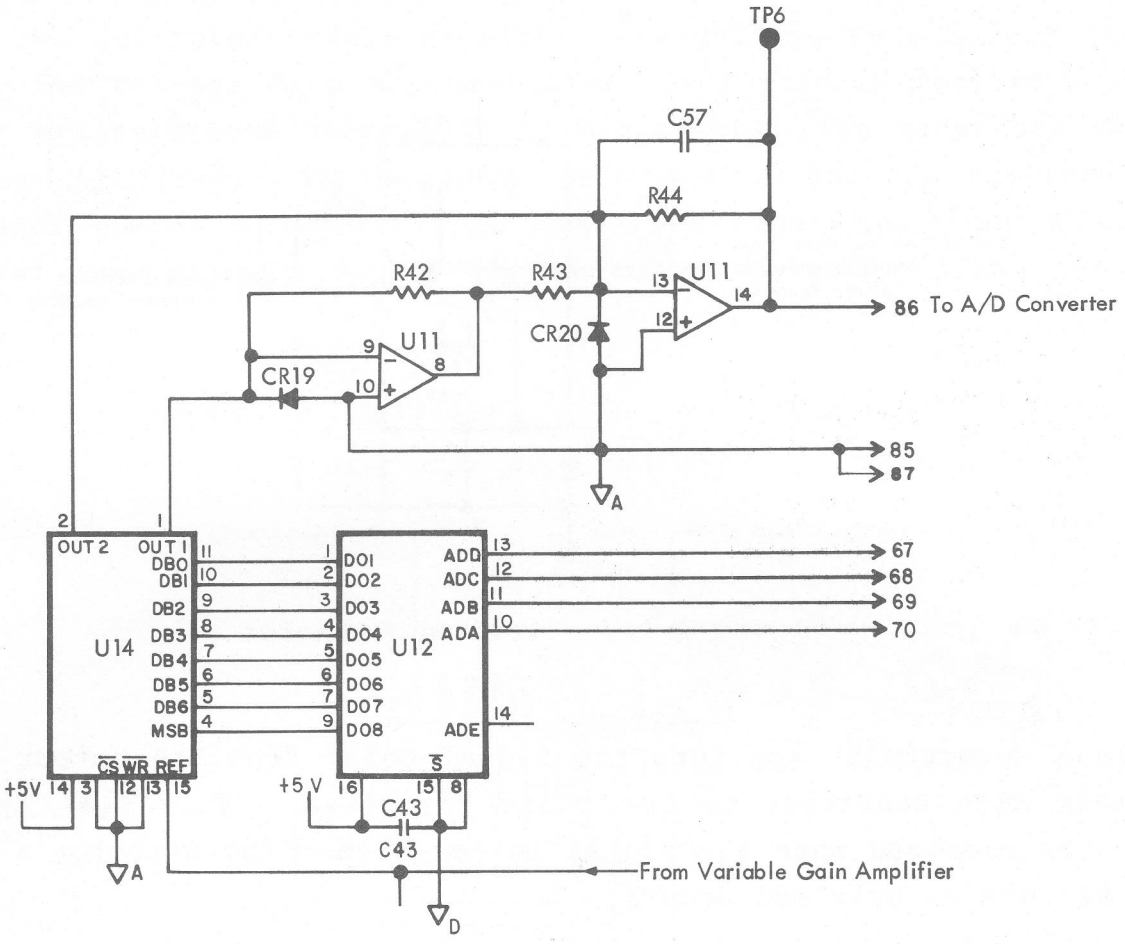


Figure 3-12. Phase Rectifier

The phase rectifier, shown in the Block Diagram, resides in U14, U12, and U11; a four quadrant, CMOS digital-to-analog converter. The phase rectifier is driven by a 32 x 8 bit PROM which does the synchronous gating needed to give a DC output. The PROM is driven by four input lines that are harmonics of the test frequency. A fifth input line is the 0°/90° bit. This circuit provides a multiplier type action of phase detection. It takes the product of the sinewave (measured signal) coming in and the digitally related sinewave (from the PROM) to produce a DC current output. The current output of U14 is summed by two sections of operational amplifier U11 to produce a full wave voltage output.

3.4 MOTHERBOARD

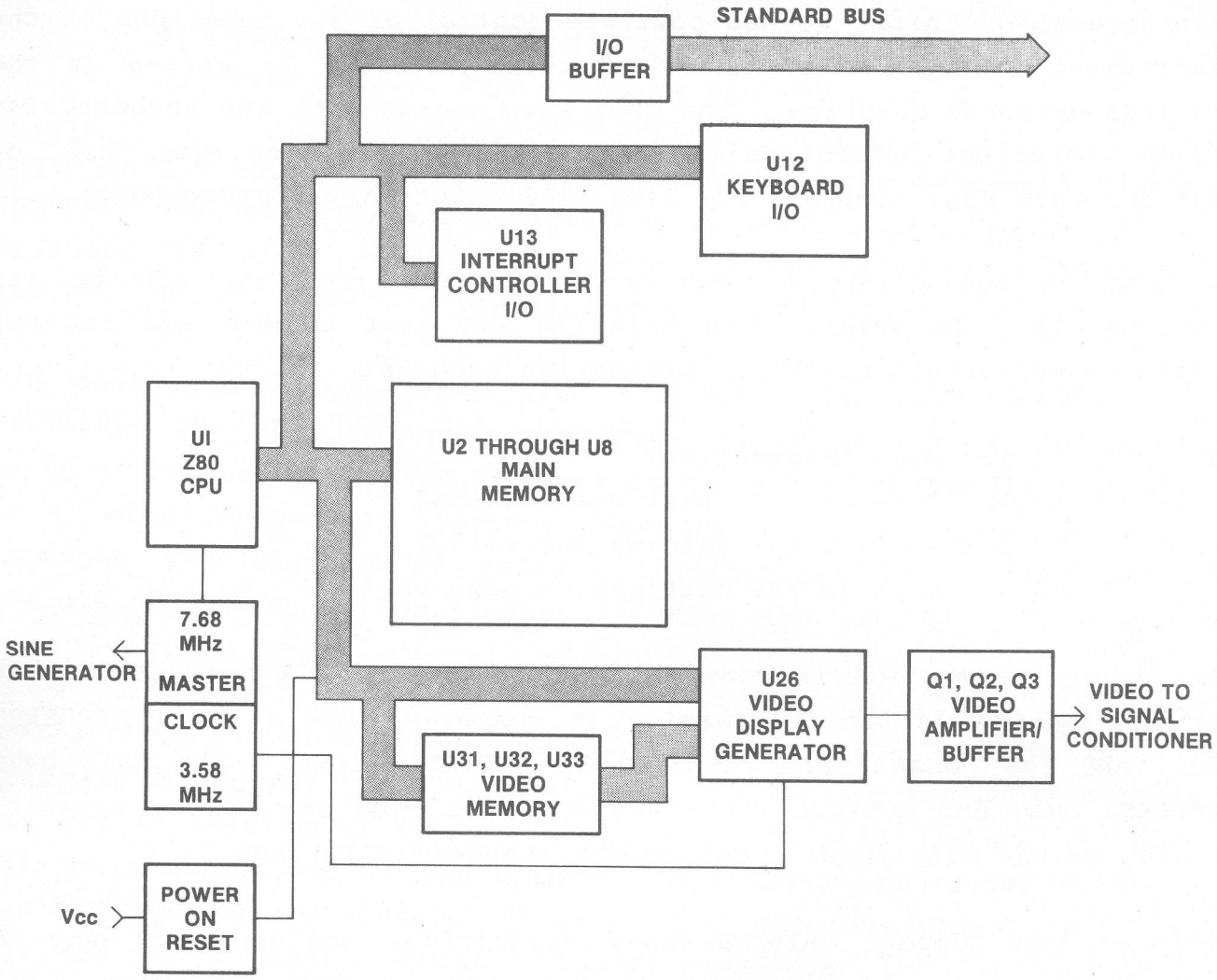


Figure 3-13. Motherboard Simplified Diagram

A simplified diagram of the motherboard is shown in Figure 3-8. The motherboard architecture centers on its standard communication bus which has 6 slots for plugging in circuit cards containing measurement circuitry, IEEE-488 interfacing circuitry, RS232 interfacing circuitry, and other bus compatable devices. The motherboard holds the Z80 CPU chip and its memory, the video generator and its memory, the master clock, and associated control logic.

3.4.1 CPU

The central processing unit (CPU) used in the 2100/2110 is a Z80 microprocessor chip. It has complete control of all functions of the instrument and does all the calculations required to arrive at the desired measured quantity. The CPU, when joined with the keyboard I/O (U12), interrupt controller I/O (U13), and main memory PROM, ROM, or RAM (U2 thru U8), comprise the 2100/2110's internal microcomputer.

A computer bus exists to convey information from the CPU to its peripherals. In order to do this the CPU must supply, and the bus must convey certain specific information such as:

1. What information?
2. To whom? To what destination?
3. When is the information valid?
4. When is the destination name valid?

The exact information is conveyed over an 8 bit DATA bus, the source or destination of the information is conveyed over a 16 bit ADDRESS bus, and the "whens" are resolved by CONTROL lines. The DATA bus, ADDRESS bus, and CONTROL lines are combined into one set of parallel lines, on the motherboard, called the standard (STD) bus.

Any CPU can support only so many capacitive, and only so many DC loads. Expansion beyond these load limits requires buffering. All ADDRESS, DATA, and CONTROL lines are buffered before they are routed to the standard (STD) bus. Thus, all things that talk to the CPU can be divided into two groups: those that exist on one side of the buffers (that talk directly to the CPU), and those that exist on the other side of the buffers (that talk to the CPU through the buffers). It is the job of the motherboard's logic to decide on which side of the buffers a device is and whether or not to enable those buffers. If an addressed device is on the CPU side of the buffers (INTERNAL), it needs to be singled out (SELECTED) before it can speak or be spoken to. Devices that are INTERNAL are:

1. Keyboard I/O, KDI18279, U12
2. Interrupt controller I/O, CTC3882, U13
3. Video display generator control, MC6847, U26
4. Video memory, RAM, U31 thru U33
5. Main memory, PROM, ROM, or RAM, U2 thru U8

Logic on the motherboard is programmed to know the addresses of these INTERNAL devices. For all devices not INTERNAL, the motherboard logic presumes that they reside somewhere on the far side of the buffer, on the STD bus, in this case the appropriate buffers are enabled.

I/O decode is accomplished with two MSI devices, a DM8131 and a 74LS139. The 8131 is a hex comparator which is set to recognize a range of I/O addresses. This range is subdivided by the 74LS139 which is a 2:4 line decoder/selector. When the DM8131 recognizes a valid INTERNAL I/O address it selects the decoder which resolves the address, allowing one particular INTERNAL I/O device to communicate with the CPU.

Memory decode is accomplished with the MSI device, a 74LS288, which is a 32 x 8 bit fused link ROM. The inputs to the ROM are address lines, the ROM is programmed to do a table lookup: "this address in, means this chip select out". The chip-select outputs are routed to one of the INTERNAL memory sockets (U2 thru U8). The same technique is used for the video memory matrix. Please note that the 74LS288 ROM is doing the same job for the memory as the comparator and selector are for the I/O.

It may be interesting to note that these are more than just address lines entering the comparator chips in both of the previous circuits, these are the CONTROL lines that tell the comparator when the address is valid and when a chip select can be output.

3.4.2 Standard Communications Bus

When the CPU addresses a device on the output side (EXTERNAL) of the CPU buffers, it also needs to be singled out (SELECTED) before it can speak or be spoken to. There are a number of lines, called the standard (STD) bus, that are dedicated to conveying address information, control signals, and data to and from these EXTERNAL devices. The STD bus has six locations for plugging in measurement and I/O dedicated devices. Standard bus signals and card edge connections are identified in Table 3-1. Devices that are serviced by the STD bus are:

1. Digital and Analog Measurement circuit assemblies.
2. IEEE-488 Interface circuit assembly (optional).
3. RS232 Interface circuit assembly (optional).
4. Cassette tape interface (Model 2110 only).
5. External Memory circuit assembly.

	PIN	MNEMONIC	SIGNAL FLOW	DESCRIPTION	PIN	MNEMONIC	SIGNAL FLOW	DESCRIPTION
LOGIC POWER BUS	1	+5V	In	+5 Volts DC (Bussed)	2	+5V	In	+5 Volts DC (Bussed)
	3	GND	In	Digital Ground (Bussed)	4	GND	In	Digital Ground (Bussed)
	5	-5V	In	-5 Volts DC	6	-5V	In	-5 Volts DC
DATA BUS	7	D3	In/Out	Low Order Data Bus	8	D7	In/Out	High Order Data Bus
	9	D2	In/Out	Low Order Data Bus	10	D6	In/Out	High Order Data Bus
	11	D1	In/Out	Low Order Data Bus	12	D5	In/Out	High Order Data Bus
	13	D0	In/Out	Low Order Data Bus	14	D4	In/Out	High Order Data Bus
ADDRESS BUS	15	A7	Out	Low Order Address Bus	16	A15	Out	High Order Address Bus
	17	A6	Out	Low Order Address Bus	18	A14	Out	High Order Address Bus
	19	A5	Out	Low Order Address Bus	20	A13	Out	High Order Address Bus
	21	A4	Out	Low Order Address Bus	22	A12	Out	High Order Address Bus
	23	A3	Out	Low Order Address Bus	24	A11	Out	High Order Address Bus
	25	A2	Out	Low Order Address Bus	26	A10	Out	High Order Address Bus
	27	A1	Out	Low Order Address Bus	28	A9	Out	High Order Address Bus
	29	A0	Out	Low Order Address Bus	30	A8	Out	High Order Address Bus
CONTROL BUS	31	WR*	Out	Write to Memory or I/O	32	RD*	Out	Read to Memory or I/O
	33	IORQ*	Out	I/O Address Select	34	MEMRQ*	Out	Memory Address Select
	35	IOEXP*	In/Out	I/O Expansion	36	MEMEX*	In/Out	Memory Expansion
	37	REFRESH*	Out	Refresh Timing	38	MCSYNC*	NA	CPU Machine Cycle Sync
	39	STATUS 1*	Out	CPU Status (Z80-M1)	40	SATUS 0*	Out	CPU Status
	41	BUSAK*	Out	Bus Acknowledge	42	BUSRQ*	In	Bus Request
	43	INTAK*	Out	Interrupt Acknowledge	44	INTRQ*	In	Interrupt Request
	45	WAITRQ*	In	Wait Request	46	NMIRQ*	In	Non-Maskable Interrupt
	47	SYSRESET*	Out	System Reset	48	PBRESET*	In	Push Button Reset
	49	CLOCK*	Out	Clock Processor (1.92MHz)	50	CNTRL*	In	2 x CPU Clock (3.84MHz)
	51	PCO*	Out	Priority Chain Out	52	PCI*	In	Priority Chain In
POWER BUS	53	AUX GND	In	AUX Ground (Bussed)	54	AUX GND	In	AUX Ground (Bussed)
	55	AUX + V	In	AUX Positive (+12 Volts DC)	56	AUX - V	In	AUX Negative (-12 Volts DC)

*Low Level Active Indicator

Table 3-1. Standard Bus Signals and Card Edge Connections

3.4.3 Extra Bus

Some EXTERNAL devices used in the 2100/2110 communicate with signals that are not compatible with the STD bus. For these devices, a second proprietary bus called the extra bus is used. The extra bus is designed to carry analog signals as well as digital information. The extra bus transmits the following major signal categories, see Table 3-2 for a further breakdown of signals.

1. 7.68MHz master clock
2. Sinewave test signals
3. Chip select signals
4. Measurement cycle and zero crossing information
5. Remote start

PIN	MNEMONIC	DESCRIPTION	PIN	MNEMONIC	DESCRIPTION
57	AUX GND	AUX Ground (Bussed)	58	AUX GND	AUX Ground (Bussed)
59	AUX +V	AUX Positive (+12VDC)	60	AUX -V	AUX Negative (-12VDC)
61	IO1	I/O Select	62	IO2	I/O Select
63	IO3	I/O Select	64	IO4	I/O Select
65	60Hz	60Hz Square Wave	66	7.68MHz	128 x 60kHz
67	F0	Test Frequency Square Wave	68	F1	2 x F0 (F0→F6 connect to sine ROM Address Pins)
69	F2	4 x F0 (F0→F6 connect to sine ROM Address Pins)	70	F3	8 x F0
71	F4	16 x F0	72	F5	32 x F0
73	F6	64 x F0	74	$\overline{\text{FINE GATE}}$	Analog Gate Control
75	$\overline{\text{HI GATE}}$	Analog Gate Control	76	$\overline{\text{LO GATE}}$	Analog Gate Control
77	$\overline{\text{Z GATE}}$	Analog Gate Control	78	$\overline{\text{JNK}}$	Analog Gate Control
79	HI CMP	Comparator Contol	80	LO CMP	Comparator Control
81	Z CMP	Comparator Control	82	SIG OVERLOAD	Comparator Control
83	SINE GND	Ground	84	SINEWAVE	Buffered Sinewave
85	LO-V_{IN}	A/D Converter Control	86	HI-V_{IN}	A/D Converter Control
87			88		
89			90		
91			92		
93			94		
95	$\overline{\text{CPU BUSY}}$	Indicates Internal Process	96	$\overline{\text{START}}$	Start Measurement
97	-7.5V	500mA CMOS Switches	98	+7.5V	500mA CMOS Switches
99	GND	Ground	100	GND	Ground

Table 3-2. Extra Bus Signals and Card Edge Connections

3.4.4 Master Clock

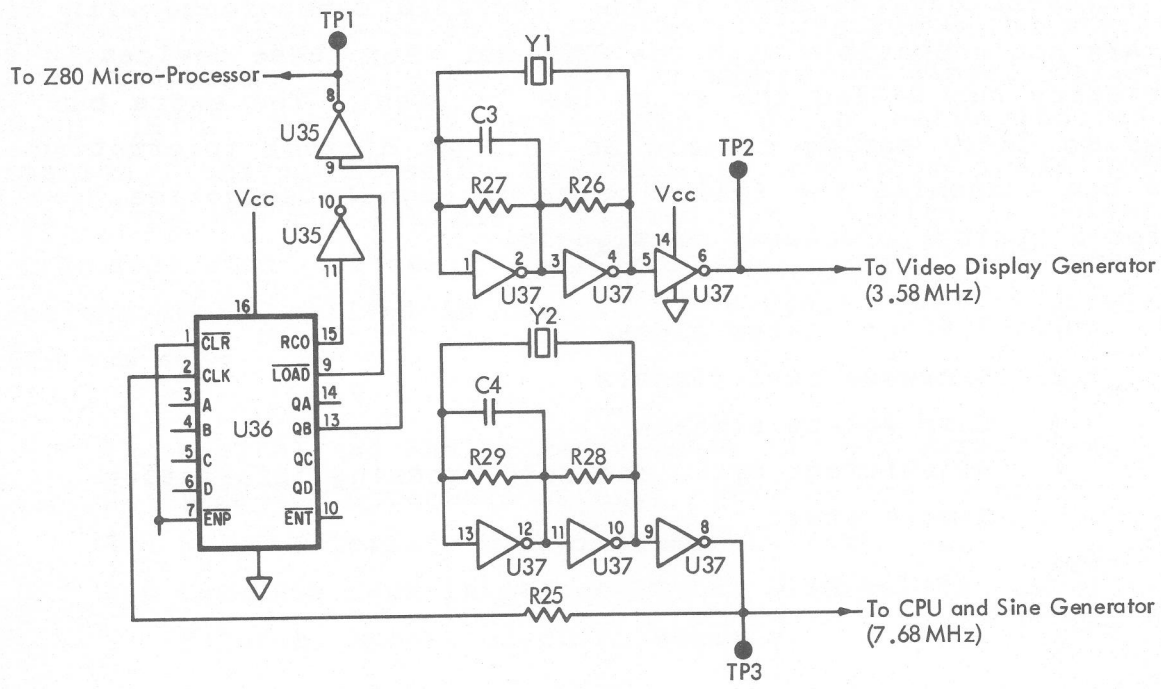


Figure 3-14. Master Clock

The master clock is actually two clock oscillators which support the motherboard. One clock is 7.68MHz for the CPU and projected analog applications. This clock is divided by 4 to produce the 1.92MHz clock signal which sets processor speed, and it is divided by 128 to provide the 60kHz base frequency used by the sine generator. The other clock is a "color burst" frequency (3.58MHz) and is the required clock for the video display generator.

3.4.5 Power ON Reset

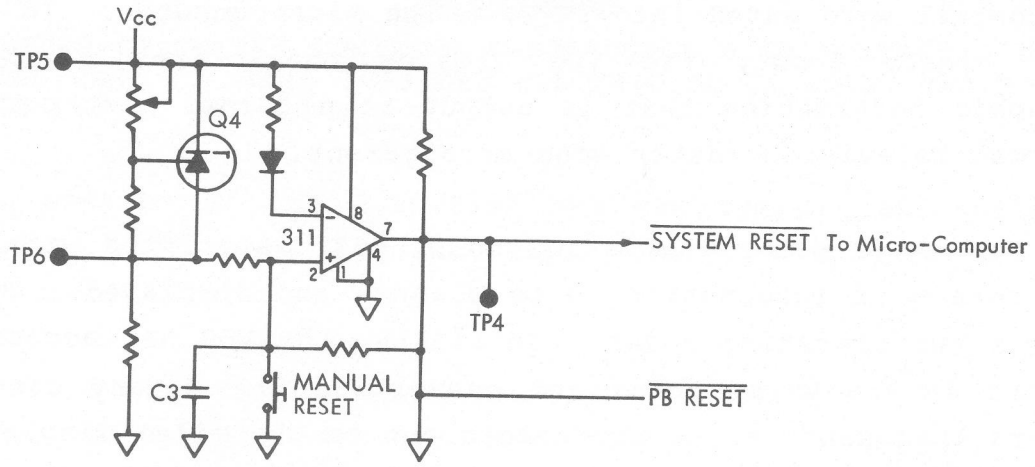


Figure 3-15. Power ON Reset

The power ON reset circuitry is necessary because of the long power-up and power-down time of the switching power supply. It keeps all logic, on the motherboard, reset until V_{cc} reaches 4.75 volts and it keeps the logic operating until V_{cc} drops below 4.75 volts, during power down. If V_{cc} is below 4.75 volts, the power ON reset circuit holds the reset line low. When V_{cc} crosses the 4.75 volt threshold, the power ON reset circuit integrates for 1/10 second, then releases the reset line.

3.4.6 Video Display Generator

The video display generator (VDG) is a Motorola MC6847 which accepts a binary control word gated into it from the microcomputer. In response to that binary input, the VDG creates characters, graphic, and semi-graphic information that is output in a format that corresponds to a normal television raster scan arrangement.

The VDG has three memory chips (U3, U32, U33) associated with it that store a screen of information to be scanned and displayed. The video memory has two operating modes. Initially, the VDG has access to the memory and is always scanning and converting the memory contents to characters then sends those characters out to the video display. When the processor is ready to read or write a character into that memory, it goes through a piece of arbitration logic that says, if the video display generator is doing a horizontal sync, a horizontal retrace, or a vertical sync then grant the processor access to the memory. However, if the VDG is not doing horizontal sync or vertical sync then it is putting video out and must not be interrupted. At that point the processor is told to wait, treating the video memory like slow memory. The processor will wait, keeping the address, data, and control lines activated, until a horizontal sync or a vertical sync is output, then the memory returns to normal operation and readily accepts new inputs from the processor.

The composite video, as it comes out of the VDG chip, is a very low level signal. The signal is high impedance in nature and is very susceptible to noise and interference. To counteract these undesirable qualities, there is a three transistor amplifier/buffer (Q1, Q2, Q3) that transforms the VDG output signal into a higher level, low impedance output signal. This output signal then drives the video section of the 2100/2110.

3.5 VIDEO CIRCUITRY

DANGER

THE VIDEO CIRCUITRY CONTAINS DANGEROUSLY HIGH VOLTAGE. EXERCISE EXTREME CARE TO AVOID POSSIBLE ELECTRIC SHOCK WHICH MAY RESULT IN SEVERE INJURY OR DEATH.

The video section of the 2100/2110 has two circuit assemblies that deal directly with processing and displaying video information. These circuit assemblies are:

1. Signal Conditioner Assembly (P/N 45468)
2. Deflection Assembly (P/N 45470)

The operation of the video circuitry located on these assemblies is discussed in the following paragraphs.

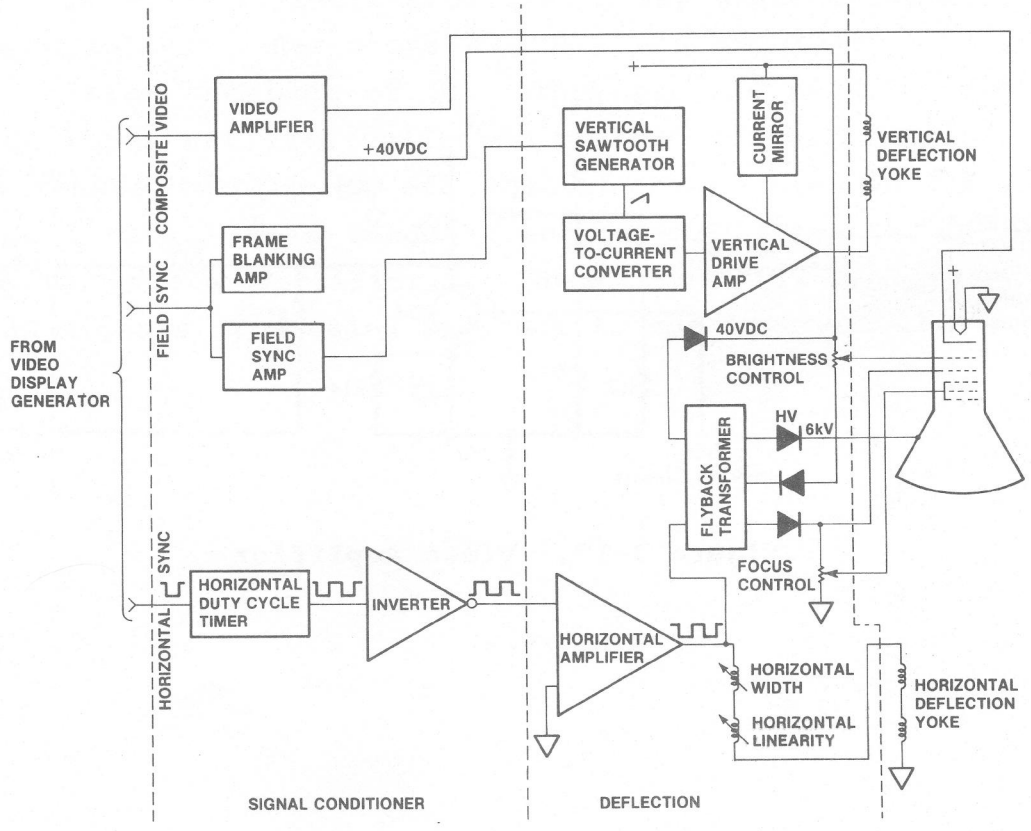


Figure 3-16. Video Circuit Block Diagram

3.5.1 Signal Conditioner Circuitry (P/N 45468)

The Signal Conditioner Assembly receives a number of input signals and operating voltages on input connector P301. Composite video, field sync, and horizontal sync signals come from the video display generator, U26, located on the motherboard.

The video display generator is a Motorola MC6847 which accepts sequences of binary words from the microcomputer. In response to that binary input it creates characters, graphic, and semi-graphic outputs in a format that corresponds to a normal raster scan arrangement. The MC6847 also provides separate field sync and horizontal sync signals which are usable directly without having to strip them from the composite video input.

3.5.2 Video Amplifier

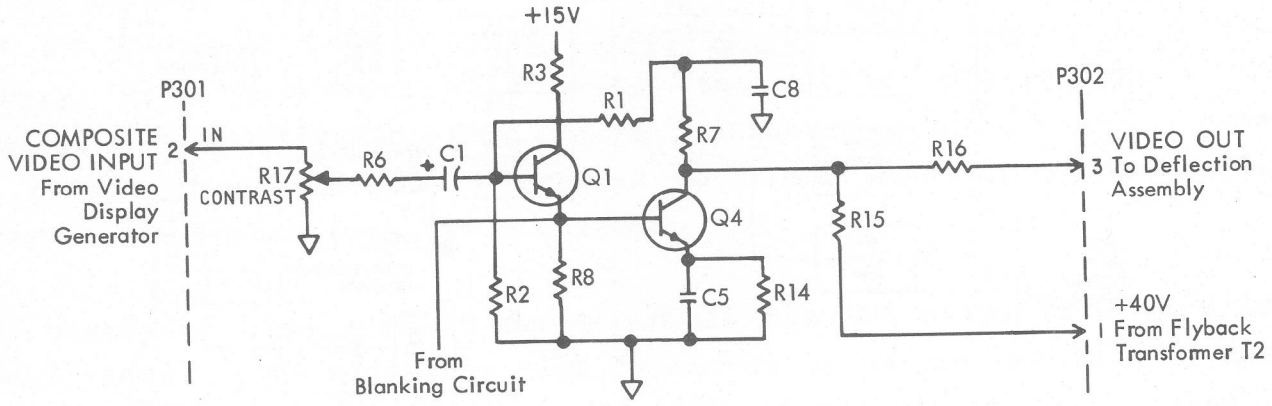


Figure 3-17. Video Amplifier

The composite video signal comes first to potentiometer R17, the contrast control. The contrast control adjusts the level of the composite video signal going to the CRT. The signal passes through RC shaping network R6 and C1 into the base of Q1. Buffer/amplifier Q1 is an emitter follower that drives the base of inverting amplifier Q4 whose collector in turn drives, through R16, to the cathode (pin 2) of the CRT. The collector of Q1 is pulled up to +15V by R3 while the emitter resistor R8 is used to develop the signal as well as for biasing the base of Q4, a 2N3053. The emitter of Q4 uses R14 and C5 to increase the high frequency gain of the Q4 stage. The collector of Q4 and base of Q1 are DC biased through R15 and the +40V source located on the Deflection Assembly. (This 40V source also, through R15 and R16 provides bias for the cathode of the CRT.) The collector of Q4 can have voltage swings in the vicinity of 20 to 30V peak-to-peak which are the levels required when composite video is applied to the cathode of the CRT. These voltage swings will turn the CRT from full-on to full-off providing crisp black and white and some half-tone displays. Resistors R1, R7, and capacitor C8 provide DC feedback to bias the base of Q1. They provide negative feedback so that as Q4 turns off it's collector voltage rises. The base voltage on Q1 increases turning Q4 off through the action of Q1's emitter driving Q4's base. This feedback action stabilizes the DC operating point of the video amplifier. Capacitor C8 is a large value to prevent AC signals from being fed back to the input of Q1.

3.5.3 Frame Blanking

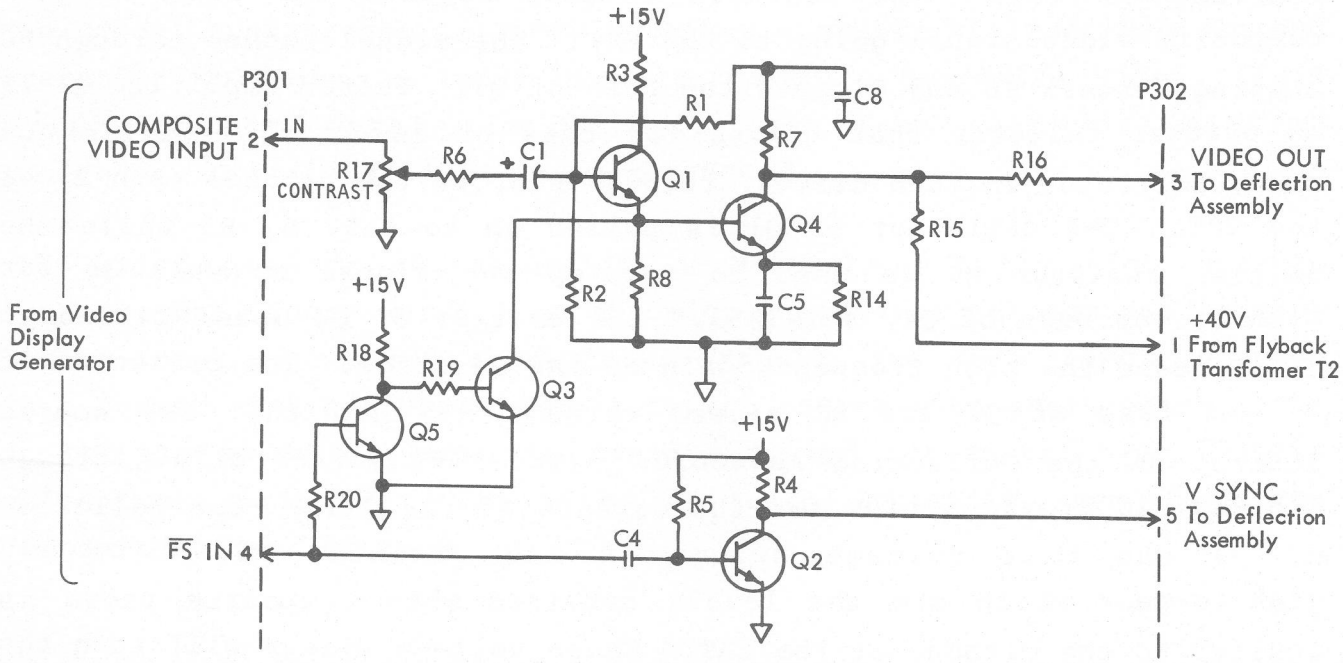


Figure 3-18. Video Amplifier with Blanking

One of the requirements of a video circuit such as the one used in the 2100/2110 is blanking the electron beam whenever one field has been completed and the electron beam is going to be retraced from the end of one field up to the beginning of the next one. The field sync (FS) input at pin 4 of P301 in addition to going through C4, a coupling capacitor, and Q2 out to the vertical sync output of this card, also comes up through Q5 and Q3, another set of DC amplifiers. Basically, this is a logic circuit made of two transistors Q5 and Q3 and resistors R18, R19, and R20, which pulls down the emitter of Q1 to shut off the video output during the retrace. When the emitter of Q1 is pulled down, which will essentially short the base of Q4 to ground, Q4's collector will go positive which is a turn off condition for the electron beam in the CRT. Positive voltages to the CRT produce black displays, near zero voltages produce white displays.

3.5.4 Horizontal Sync

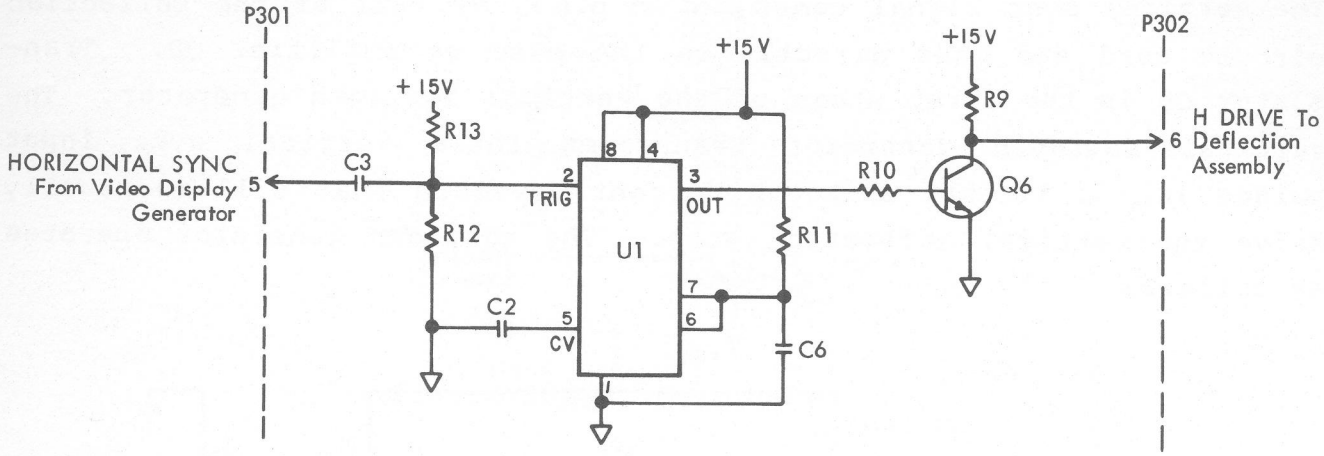


Figure 3-19. Horizontal Sync Circuitry

The horizontal, signal conditioning circuitry sets the duty cycle of the horizontal sync signal to ≈25%. The short horizontal sync (HS) pulse (negative going pulses) are coupled to the input of U1, a NE-555 timer chip, via blocking capacitor C3. Resistors R13 and R12 bias input pin 2 of U1 to trigger at 3.5VDC. The duty cycle of U1 is determined by the RC time constant set up by R11 and C6. The rectangular wave output of U1 is inverted by Q5 and sent to the Deflection assembly H DRIVE input.

3.5.5 Deflection Circuitry (P/N 45470)

The video deflection assembly passes, with no further processing, the amplified composite video signal from the Signal Conditioner assembly directly to the cathode of the CRT.

3.5.6 Vertical Sync

The vertical sync signal comes in on pin 5 of P401 of the Deflection circuit card and goes directly to the base of amplifier Q8. Transistor Q8 is the first stage of the vertical sawtooth generator. The vertical sawtooth generator transforms these vertical sync input pulses into a linear, sawtooth current waveform that will eventually drive the vertical deflection yoke. The sawtooth generator operates as follows:

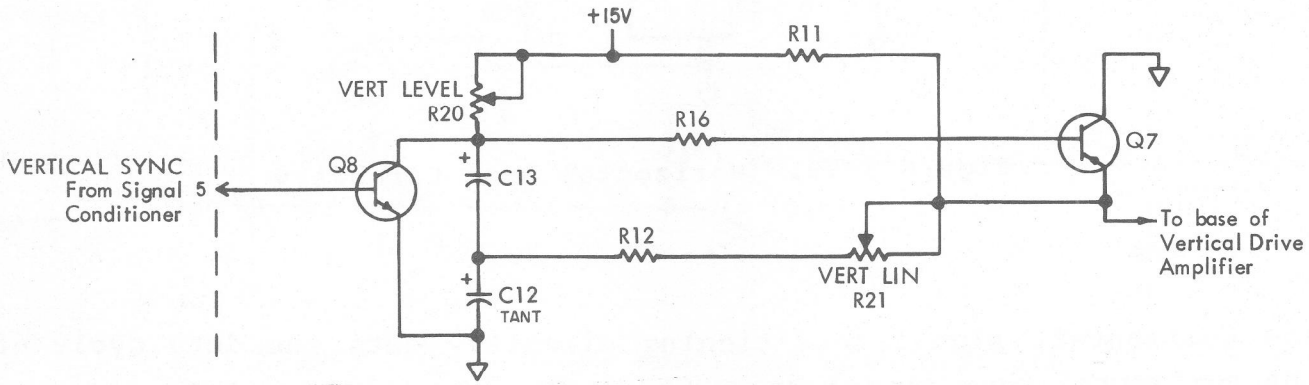


Figure 3-20. Vertical Sawtooth Generator

Resistor R20, the ramp level adjust, controls the slope of the sawtooth waveform. It sets the rate at which capacitors C12 and C13 will charge. These capacitors charge in a positive direction until a vertical sync pulse is received at Q8. The vertical sync pulse turns transistor Q8 ON allowing C12 and C13 to rapidly discharge. The result of the slow charge/fast discharge action is a sawtooth waveform at the base of amplifier Q7.

The voltage-to-current converter, Q7, is a PNP transistor connected as an emitter follower. It transforms the sawtooth voltage waveform on its base to a sawtooth current at its collector. A portion of Q7's collector current is picked off by resistors R21 and R12, the vertical linearity control, and fed back to the center of C12 and C13 to provide vertical linearity adjustment. Resistor R19, the vertical drive control, sets the amount of sawtooth collector current passed to the vertical drive amplifier Q6.

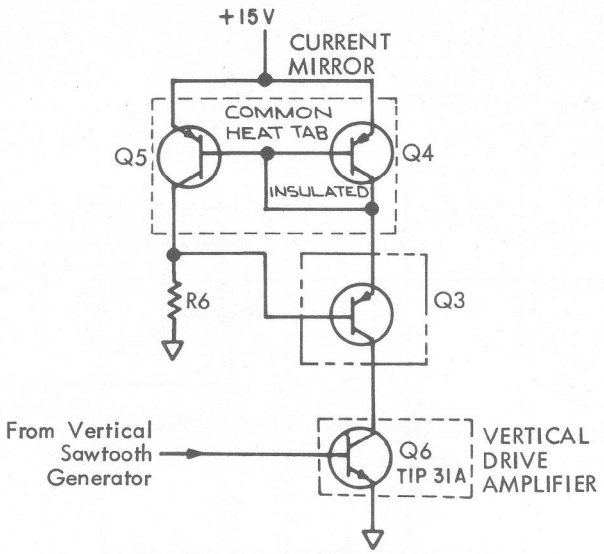


Figure 3-21. Current Mirror

The vertical drive amplifier's collector is coupled to a constant current source called a current mirror. The current mirror is designed to keep the vertical drive amplifier's current at a constant level despite changing loads on its output. This provides a low DC and a high AC impedance path for the vertical drive signal. Capacitor C11 couples vertical drive to the vertical deflection yoke which in turn moves the electron beam up/down on the CRT screen. Components C10 and R14 give feedback to the base of Q6 to provide vertical gain stability.

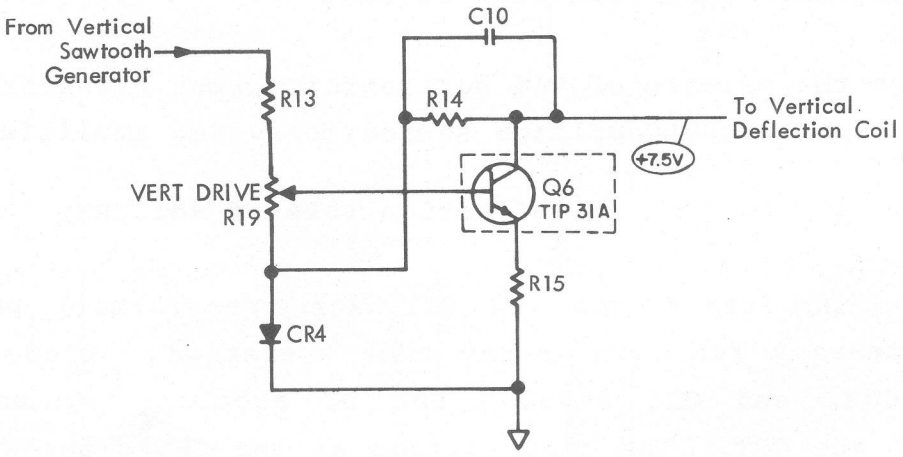


Figure 3-22. Vertical Drive Amplifier

3.5.7 Horizontal Sync

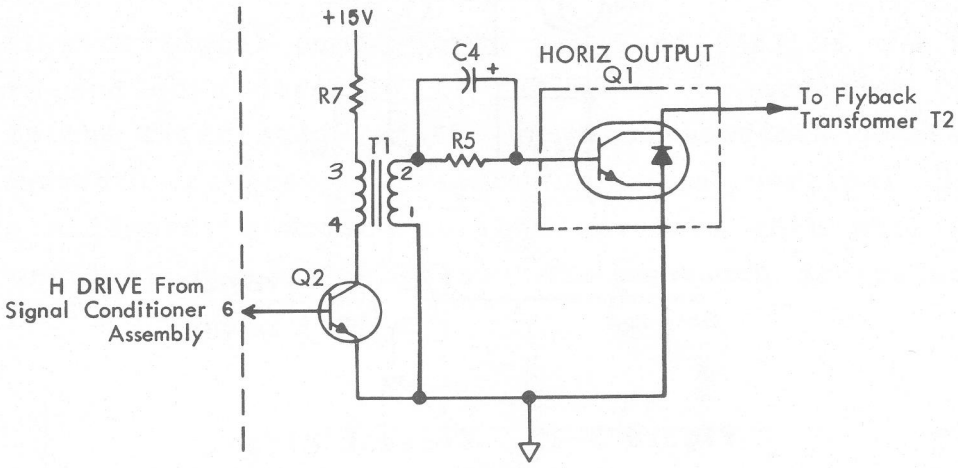


Figure 3-23. Horizontal Drive Amplifier

The horizontal sync signal, from input connector pin 6, feeds the base of transistor Q2. It is basically a digital signal which is pulled up to +15V or pulled down to ØV. Transistor Q2's collector is connected to the primary of coupling transformer T1, and also through resistor R7 to +15V. This combination, Q2, R7, T1, produces a snap action in the horizontal output transistor Q1. When transistor Q2 is shut-off, all the magnetic energy stored in T1 is coupled through C4 into the base of the horizontal output transistor. The horizontal output transistor produces base-collector current to:

1. Drive the primary of the horizontal output transformer (T2).
2. Develop the 4ØVDC voltage source for video amplifier and CRT cathode biasing.
3. Drive the horizontal deflection yoke of the CRT.

Horizontal output transformer T2 (flyback transformer) provides the voltages necessary for cathode-ray tube operation. Diode rectifiers CR1, CR2, CR3, and CR5 develop the DC accelerating and focusing voltages for the CRT. The high voltage at the CRT's anode, for final electron acceleration, is 6kVDC. Display brightness and focus are contolled by R18 and R17 respectively.

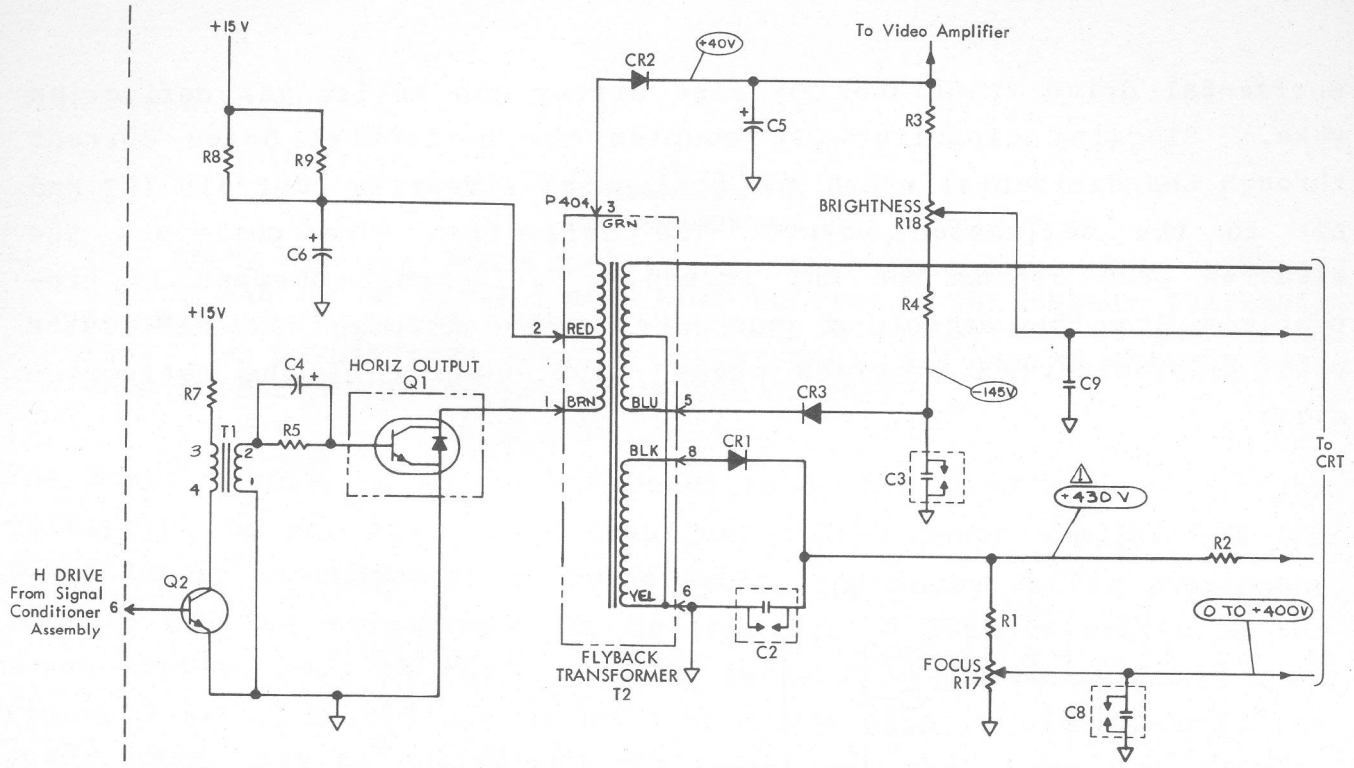


Figure 3-24. Horizontal Drive and Flyback Transformer

Diode rectifier CR2 and filter capacitor C5 develop a noise free 40VDC to bias the video amplifier's cathode drive transistor Q4, located on the Signal Conditioner circuit card.

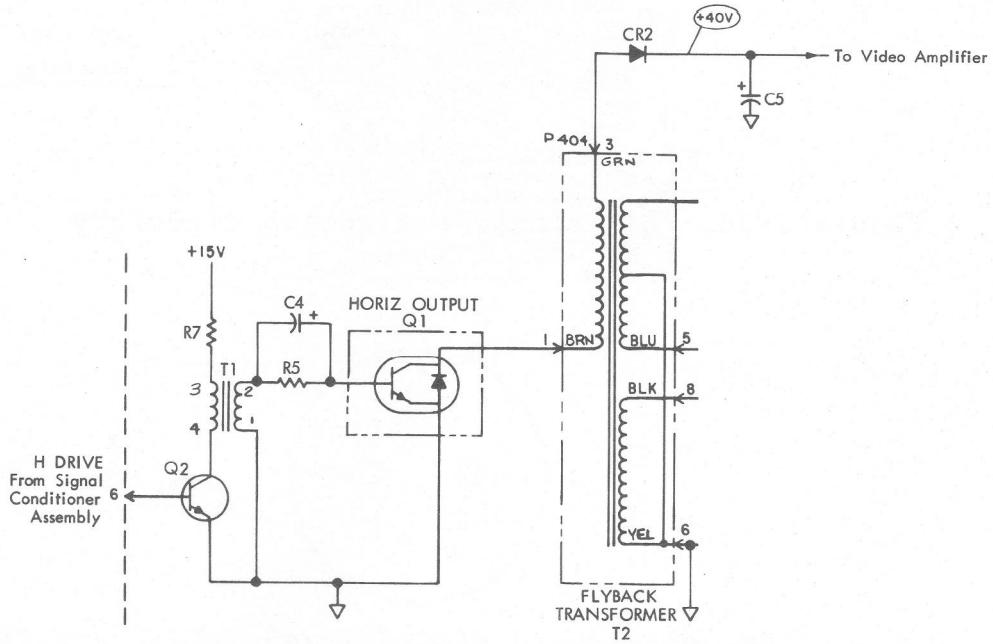


Figure 3-25. 40VDC Power Supply

Horizontal drive transistor Q1 also drives the horizontal deflection yoke. Blocking capacitor C14 couples the horizontal drive current through the horizontal width and horizontal linearity controls (L1 and L2) to the deflection yoke. The deflection yoke positions the electron beam across the CRT screen. Horizontal movement is proportional to the amount of current flowing through the deflection yoke. Capacitor C1 provides proper wave shaping of the deflection signal.

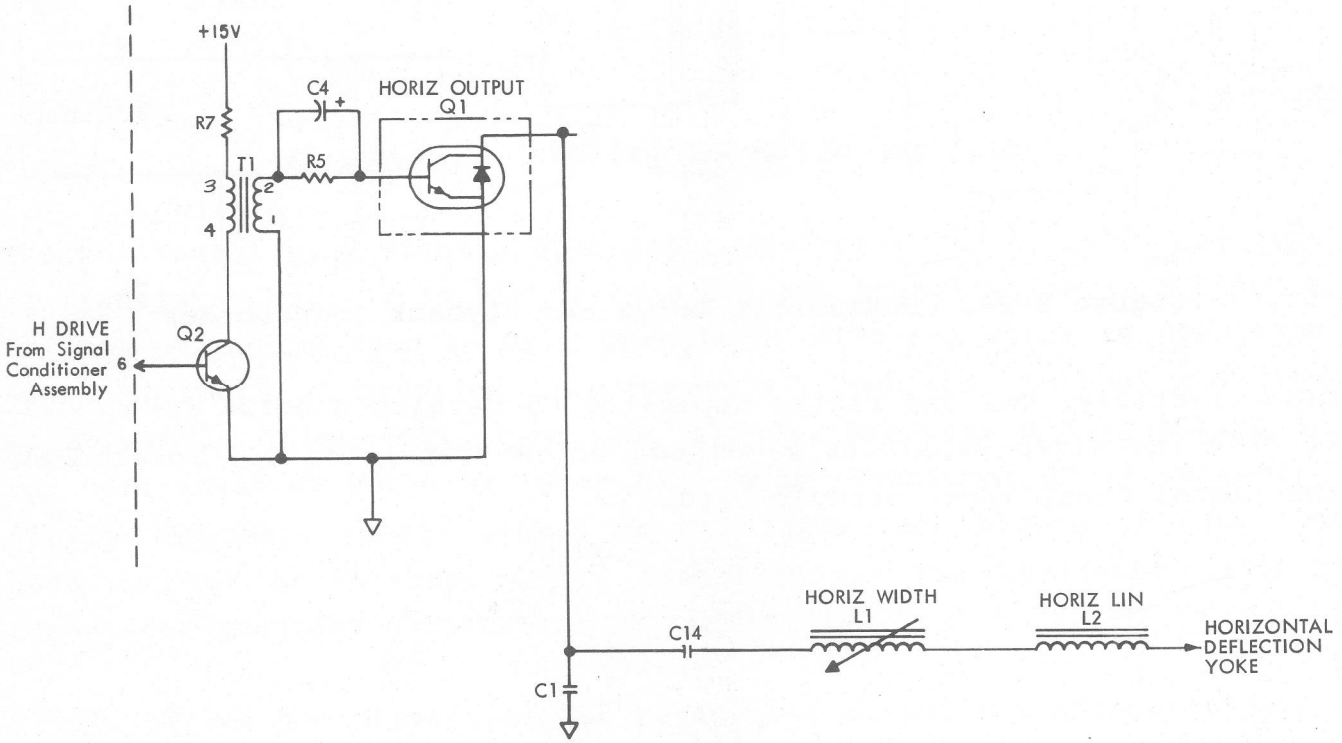


Figure 3-26. Horizontal Deflection Circuitry

3.6 POWER SUPPLY

WARNING

ALL PARTS OF THE POWER SUPPLY ASSEMBLY INCLUDING INPUT CIRCUIT COMMON ARE AT OR ABOVE POWER LINE VOLTAGE. THE ENERGY AVAILABLE AT ANY POINT ON THE ASSEMBLY MAY BE LIMITED ONLY BY THE INPUT FUSE. DO NOT ATTEMPT SERVICE OPERATIONS. FAILURE TO OBSERVE THIS WARNING MAY RESULT IN SEVERE INJURY OR DEATH.

The Power Supply, under normal conditions, has very dangerous, high voltages. Do not attempt to troubleshoot the power supply. If the power supply is suspected of being faulty, send the entire instrument back to ESI for servicing. To determine if a problem exists in the power supply, look at the five LEDs located on the motherboard (see Figure 3-27). Should one or more of these LEDs be dim or dark, the power supply may be faulty and the instrument should be sent to ESI. If all five LEDs are illuminated, the trouble is not in the power supply and normal troubleshooting procedures should be continued.
THIS IS BULLSHIT. +15V IS NOT A LED! BUT IT CAN BE DEFECT!

NOTE: Detailed service procedures on this switching power supply will be available from ESI on request at a future date.

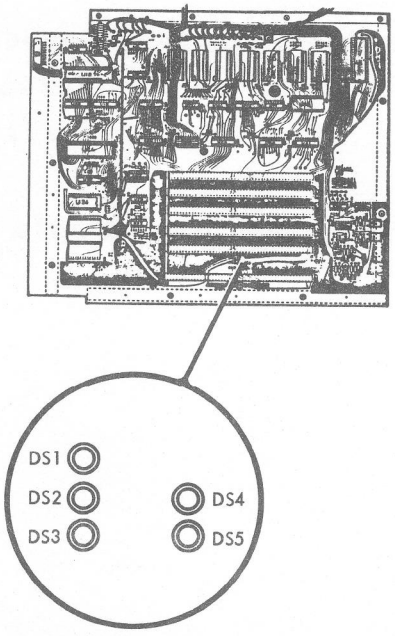


Figure 3-27. Power Supply Diagnostic LED Locations