Section 3
Theory of Operation

3-1. INTRODUCTION

3-2. This section of the manual contains the theory of operation for the 8860A. The theory is presented in two parts, an overall block diagram description followed by a detailed block diagram description. The theory of operation for the options is covered in Section 6 in this manual.

3-3. OVERALL BLOCK DIAGRAM DESCRIPTION

3-4. The overall block diagram description of the 8860A is keyed to the simplified block diagram shown in Figure 3-1. The description concentrates on the guard and measurement circuits.

3-5. Guard Circuit

3-6. The guard circuit establishes a physical and electrical separation between the analog measurement (in-guard) circuits of the 8860A and the control, display, and power supply (out-guard) circuits. The separation provides the shielding and isolating qualities required to enable accurate low-level measurements in the presence of common mode voltages. Since the guard forms a natural division of the 8860A circuitry, circuit functions and components are hereafter referred to as being in-guard or out-guard circuitry.

3-7. In-Guard and Out-Guard Processors

3-8. The 8860A uses two 8-bit microprocessors, one inside the guard (in-guard) and the other outside the guard (out-guard). The in-guard microprocessor implements function and range selection (including autoranging), controls the measurement cycle, and communicates with the out-guard microprocessor via optical couplers.

3-9. When the out-guard microprocessor receives the measurement data, it can modify or analyze the data if an offset, limits, or peak to peak function is selected. The resulting data is then sent to the display. In addition, the out-guard microprocessor monitors and responds to front-panel key selection (function, range, etc.), initiates each A/D conversion cycle, and controls the operation of either of two digital options.

3-10. Voltage Measurements

3-11. When the VDC, VAC, or VAC+VDC function is selected, the unknown voltage applied to the HI and LO INPUT terminals is directed through the input protection circuit to the AC/DC scaling and filtering circuit. AC measurements are either capacitively coupled (VAC) or directly coupled (VAC+VDC) into the scaling amplifier. Here the input voltage is either amplified by 10 (200 mV range), passed unscaled (2V range), or divided by 100 or 1000 (20V, 200V, 1000V ranges). A full-range input on any range is scaled to $\pm$2V dc or 2V rms (see Table 3-1). Measurements which are strictly dc (VDC, Ω2T, and Ω4T functions) continue directly from the scaling amplifier to the A/D Converter. All ac measurements (VAC and VAC+VDC functions) pass through the RMS-to-DC Converter where they are converted to a dc voltage.

3-12. Resistance Measurements

3-13. When the Ω2T or Ω4T function is selected, two operations occur concurrently at the input terminals:

1. A precision current is applied to the unknown resistor via the HI and LOW INPUT terminals. This current is generated by the Ohms Converter (also known as the Ohms Source). The value of source current for each range (except the 200 ohm range) is established at a level that will generate a two volt full-scale voltage for the 200 ohm range is 200 mV.

2. The voltage generated across the unknown resistor is sensed at the HI and LO INPUT terminals (for Ω2T), or at the Ω4T SENSE HI and LO terminals (for Ω4T). This voltage passes unscaled into the A/D Converter (except on the 200Ω range where it is first amplified by a factor of 10).

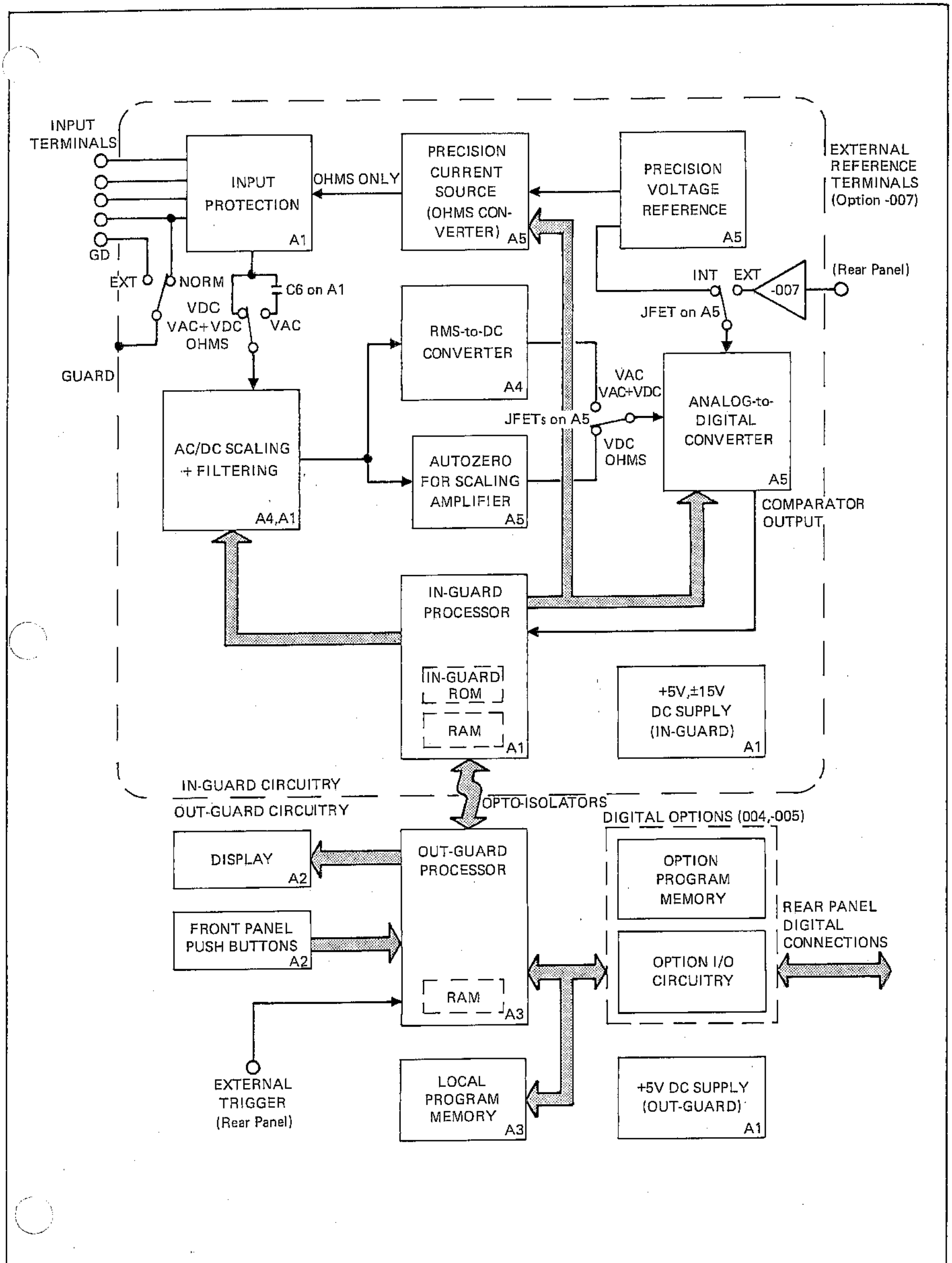


Figure 3-1. 8860A Block Diagram

Table 3-1. Scaling of Input Signals

FUNCTION	RANGE (FULL-SCALE INPUT)	OHMS CONVERTER SOURCE CURRENT (OHMS ONLY	AC/DC SSCALING		FULL-SCALE OUTPUT OF AC/DC SCALING
			INPUT DIVIDER	SCALING AMPLIFIER	
Volts VDC, VAC, VAC + VDC	200 mV 2V 20V 200V 1000VDC 700 VAC	— — — — —	÷1 ÷1 ÷100 ÷100 ÷1000	X10 X1 X10 X1 X1	±2V dc (VDC) or 2V rms (VAC, VAC + VDC)
Ohms Ω2T, Ω4T	200 Ω 2 KΩ 20 KΩ 200 KΩ 2 MΩ 20 MΩ	1 mA 1 mA 100 μA 10 μA 1 μA .1 μA	NOT CONNECTED	X10 X1 X1 X1 X1 X1	+2V dc

3-14. A/D Converter

3-15. The input to the A/D Converter is a scaled dc voltage (2V max) proportional to the 8860A input voltage or resistance. In conjunction with the in-guard microprocessor, the A/D Converter uses a dual-slope integration technique to convert the analog value to a digital representation.

3-16. DETAILED BLOCK DIAGRAM DESCRIPTION

3-17. The following paragraphs describe each of the blocks appearing in the 8860A block diagram, Figure 3-1. The description covers the power supply first, then traces the measurement signal path starting at the input terminals and ending at the display.

3-18. Drawing numbers for the applicable schematic diagrams are shown in parentheses following the description headings. The schematics are located in Section 8 of this manual.

3-19. Circuit descriptions often refer to IC and connector pin-numbers. ICs mentioned in the text are identified by U-numbers, e.g., U6. An IC pin number is identified by a dash and a number following the U-number. For example, U6-1 identifies pin 1 of IC U6. Pin 1 of each integrated circuit is identified on the pcb by a square solder pad. To identify a signal path through a series of connectors, refer to the Interconnect Diagram located in the schematic section. When two boards are connected, the pin numbers on both boards match, although the connector identification numbers (the J and P numbers) may not match. For example, pin J3-42 (Main board) mates to P1-42 (Controller board).

3-20. Power Supply (Schematic 8860-1001)

3-21. The operating voltages for the 8860 are generated on the A1 Main PCB. Operating voltages for the in-guard circuitry include +5, +15, and -15 volts. A separate +5 volt supply provides the operating voltage for the out-guard circuitry. Elsewhere, +9, -9 and -4 volt supplies are derived from the main operating voltages. Table 4-2 lists the circuitry powered by each supply.

3-22. As a troubleshooting aid, the ± 15 volt supplies for the RMS-to-DC Converter and the Ohms Converter can be disconnected by removing jumper wires on the appropriate plug-in board. Refer to Troubleshooting in Section 4 for detailed procedures.

3-23. FUSING

3-24. The replaceable fuse located on the rear panel protects against excessive current in the power supply due to a short circuit. An additional non-replaceable thermal fuse, located inside the transformer, protects the 8860A against fire hazard.

3-25. +5 VOLT SUPPLIES

3-26. Functionally, the +5 volt supplies for the in-guard and the out-guard circuitry are nearly identical. Each has a full-wave rectifier (CR10-13), a filter (C1, C2, C7), and a 5-volt regulator (VR1, VR3).

3-27. +/-15 VOLT SUPPLIES

3-28. The +15 volt supply is regulated by a 15-volt regulator (VR2). The -15 volt supply uses the output of the +15 volt supply as a reference. That is, as the output of the +15 volt supply becomes more positive, the -15 volt output becomes more negative. The tracking is accomplished by a precision inverter (U1, Ω6, R12, and R13) in which the voltage across R13 is equal to the voltage across R12. Power transistor Q6 is not short-circuit protected. Therefore, care must be taken to avoid shorting the -15 volt output to ground.

3-29. Notice the -15 volt supply requires that the +5 volt in-guard supply be working, since U1 is supplied by the +5 volt supply. The +15 volt supply is unaffected by the +5 volt supply.

3-30. CIRCUIT COMMON AND THE GUARD

3-31. The 8860A is capable of making fully floating measurements since its LO INPUT terminal is not internally connected to earth ground. To isolate the sensitive analog circuitry from the digital circuits, a guard is used. The circuitry outside the guard must interact with the outside world via the IEEE-488 option and external trigger BNC jack. Therefore, its common must sit at or close to earth ground. Thus, there are two electrically separate circuit commons: the in-guard common (also referred to as analog common), and the out-guard common (referred to as digital common). The out-guard common is connected through a 10 MΩ resistor to the center pin of the ac line cord, and thereby grounded to earth. The in-guard common is connected to the LO INPUT terminal; it is left floating, and can rise up to ± 500 volts peak above the out-guard common (earth).

3-32. The guard is a separate metal shield which encloses the analog circuitry and in-guard microprocessor. By use of the GUARD switch, the guard may be connected to the in-guard common, or to an external common via the front panel GD terminal. Use of the guard switch and terminal is described in the 8860A Operator Manual.

3-33. Input Protection (Schematic 8860A-1001)

3-34. The input protection circuit, located on the A1 Main PCB Assembly, protects the 8860A against sustained input voltages within its maximum input rating. The circuit also provides protection against voltage transients beyond this range. Sustained voltages beyond the rated range may damage the instrument.

3-35. The input protection description which follows is sectioned according to the various input paths:

1. DC and AC Voltage Sense
2. Ohms Source
3. Ω4T Sense
4. Guard

3-36. The relays located on the A1 Main PCB Assembly are not part of the input protection circuitry. Instead, they route the input signal according to the selected range and function. Additional relay details are provided later in this section under Scaling and Filtering.

3-37. PROTECTION FOR DC AND AC VOLTAGE SENSE

3-38. For dc or ac input signals the sense path is from the INPUT HI terminal through R7 (2 kΩ, 7W resistor). At the junction of R7 and R10, four metal oxide varistors (MOV) RV1 through RV4 are connected to analog LO. These bipolar MOVs limit high voltage transients to ±2 kV at point E3. If the MOVs overheat and fail, they short circuit and thereby continue to provide protection for the scaling circuitry.

3-39. Coils L1 and L2 suppress arcing when the contacts of K1 are switching high voltages. The individual switches on K1, K2, and K4 are wired in series to obtain the 1000V isolation required for input switching. Resistors R10 and R11 protect the contacts of relay K3 from current surges when capacitor C6 discharges through K3.

3-40. OHMS SOURCE PROTECTION

3-41. The protection path for the ohms source is through R6. Varistors RV5 through RV8 limit high voltage transients to ± 2 kV, as described previously. The thermistor RT1 (nominally 1 kΩ) protects against high sustained voltages up to 300V peak. As the temperature of RT1 rises, its resistance increases and effectively isolates the ohms source circuitry from the HI INPUT terminal. The clamp circuit (Q8, Q9, Q10, CR6, R14, and R15) serves two purposes: first, it clamps the open-circuit voltage of the current source (point E8) to about 5V; second it protects the Ohms Converter from voltage spikes at the input by limiting positive spikes to +5V (via Q8 and Q10) and negative spikes to -2V (via CR6 and Q9). Capacitor C16 helps to shunt transient voltages to ground.

3-42. FOUR-TERMINAL OHMS SENSE PROTECTION

3-43. Resistors R8 and R9 provide protection for the 4-terminal ohms sense circuitry. To prevent ac cross talk, FET Q13 grounds the Ω4T input line when VAC or VAC+VDC is selected. Transistor Q7 keeps the Ω4T SENSE LO line within -.7V to +9V of the in-guard common. This clamping of the sense inputs protects JFET A1-E on the AC/DC Scaling circuit.

3-44. GUARD PROTECTION

3-45. Components R25, C17, and R29 prevent the guard from making fast voltage transitions. As a result, voltage spikes at the GD terminal do not reach the guard itself.

3-46. Scaling and Filtering (Schematic 8860A-1004, Sheet 1 of 2)

3-47. The ranging and filtering for the selected function takes place on the AC/DC Scaling PCB (A4). When a range is selected, either manually or automatically, the AC/DC scaling circuitry conditions the input signal to produce a ±2V dc or 2V rms signal for a full-range input.

3-48. AC/DC SCALING

3-49. The amount of scaling for each range and function is given in Tables 3-1. Figure 3-2 shows how the scaling takes place. Either JFET switch A1-A, A1-B, or Q13 is ON to divide by 1, 100, or 1000. FETs Q12 and Q18 configure the scaling amplifier for a gain of either 1 or 10. For both voltage resistance measurements, a conditioned signal of 2 volts dc at the A/D Converter is recognized as a full scale-input for all ranges.

3-50. For all resistance measurements (except on the 200Ω range) the sense voltage generated across the unknown resistor is scaled to the 2V range by the current source (Ohms Converter). The 200Ω range has a full-scale sense voltage of 200 mV. Consequently, the AC/DC Scaling amplifier multiplies this voltage by 10 to establish the required 2V dc at full scale. The JFET state tables are located with the AC/DC Scaling schematic in Section 8.

3-51. The scaling amplifier (Q17 and U14) is the first amplifier an input signal encounters. In VDC, the differential JFET input stage Q17 provides an input resistance greater than 10,000 MΩ for the 200 mV and 2V ranges. The input divider presents a 10 MΩ input resistance for the higher voltage ranges. Capacitors C2 through C7, connected to the resistive divider, are adjusted to maintain a flat frequency response for the divider ranges.

3-52. The voltage clamp (Q2, Q3, Q7, Q8, VR1, VR2) limits the voltage applied to the scaling amplifier to ±10V peak on the two lowest voltage ranges (both ac and dc) and all ranges of ohms. The other voltage ranges do not require clamping since the largest voltage that can appear at the scaling amplifier is 10V (1000V divided by 100).

3-53. JFET BIAS AMPLIFIERS

3-54. The high-impedance, unity-gain, JFET amplifier, Q16 and U5, follows the input voltage to pull up the gate of each conducting JFET in the scaling circuit. Amplifier U6A performs the same bias function for JFET switches A1-G, Q12, and Q18.

3-55. FILTERING

3-56. A passive and an active filter are a part of the AC/DC Scaling network. Both are shown in simplified form in Figure 3-2.

3-57. If either the Calculating Controller Option (-004) or the IEEE-488 Interface Option (-005) is installed, a settling delay (Modifier A4) may be enabled. In this case, each measurement is initiated only after the filter voltages have settled. The amount of delay is controlled by the in-guard processor.

3-58. Passive Filtering

3-59. The passive filter consists of capacitor C9, JFET Q15, and the resistive component (approximately 100 kilohms) of the input divider. The VDC and the ohms functions allow the filter to be selected using the front panel filter switch. If the filter is not selected, its state is conditional as described in the state table (see schematic). Selecting either the VAC or the VAC+VDC functions disables both filters regardless of other operating conditions.

3-60. 3-Pole Active Filtering

3-61. The front panel FILTER modifier, for certain functions and ranges, inserts a low-pass 3-pole Butterworth filter (U3) with a corner frequency of approximately 7 Hz. It provides additional noise rejection in VDC, Ω2T, and Ω4T.

3-62. AUTOZERO

3-63. The scaling amplifier (Q17 & U14) has an inherent input offset voltage which drifts with time and temperature. In the VDC and ohms functions the autozero circuitry eliminates the effect of this error at the start of every VDC or ohms measurement cycle. (In VAC and VAC+VDC the autozero routine is not performed.) Functionally, the auto zero circuit may be divided into the following three groups:

1. Components to momentarily short the input of Q17 to ground through A1-G and either JFET A1-D (for VDC and Ω2T), or A1-E (for Ω4T). The drive signal for A1-G is $\overline{\text{INT}}$.
2. Components to store and subtract the offset voltage from the output of U14: C15 and Q10 located on the A/D Converter board.
3. Components to correct for charge injection during the measurement cycle: C1, R5, C44.

3-64. A functional grouping of the autozero components is shown in Figure 3-3. The auto zero sequence is performed under the control of the in-guard microprocessor as follows: FETs Q10 and A1-G close simultaneously. The input of Q17 is grounded causing capacitor C15 to charge to the combined offset voltage of Q17 and U14. Then Q10 and A1-G open causing the corrected input signal to be applied to the input buffer of the A/D Converter, A2-J.

3-65. In the four-terminal ohms function, the DMM autozeros through JFET A1-E to the Ω4T SENSE LO terminal. This terminal is the measurement reference, giving true four-terminal sense.

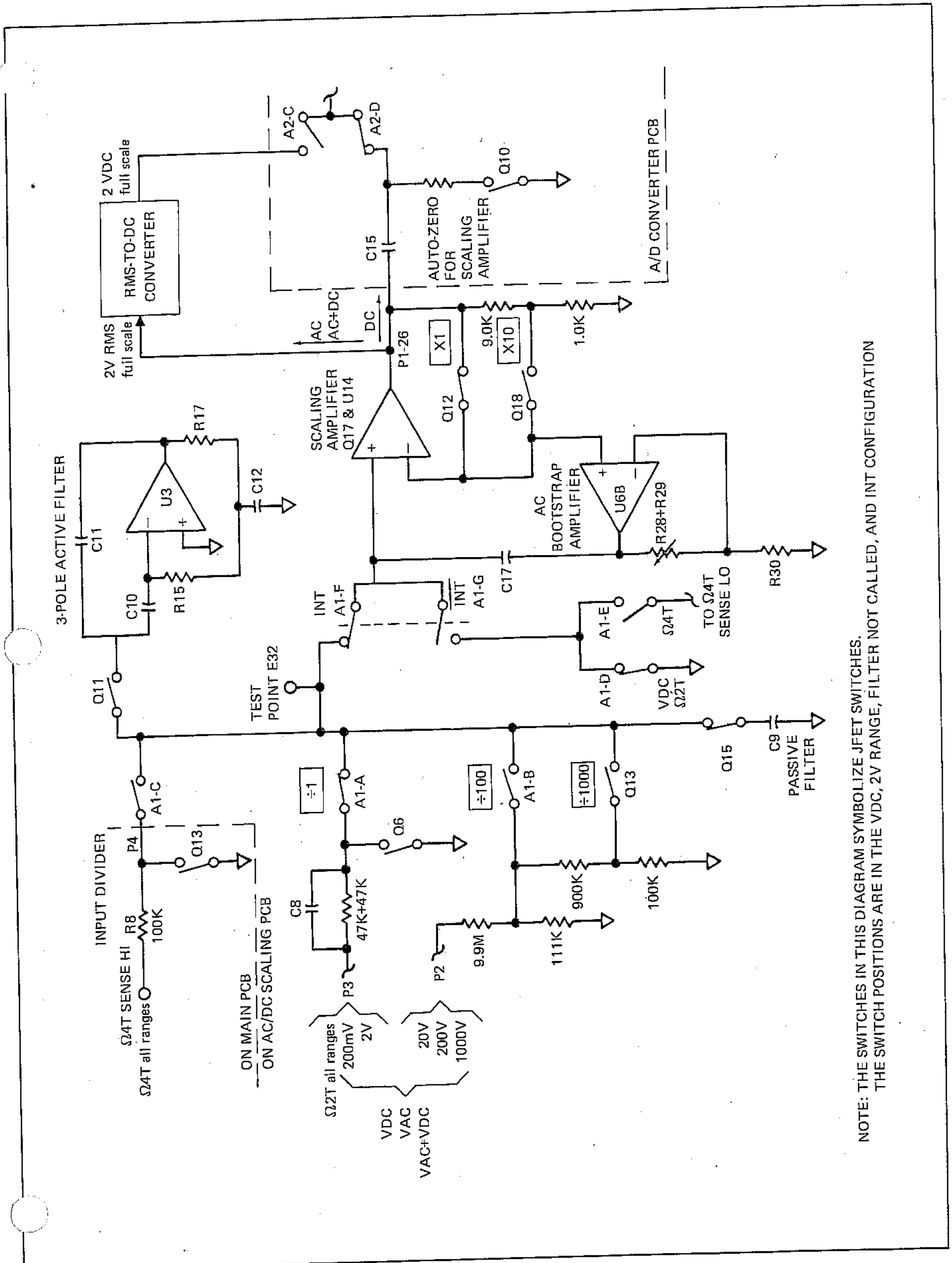


Figure 3-2. AC/DC Scaling

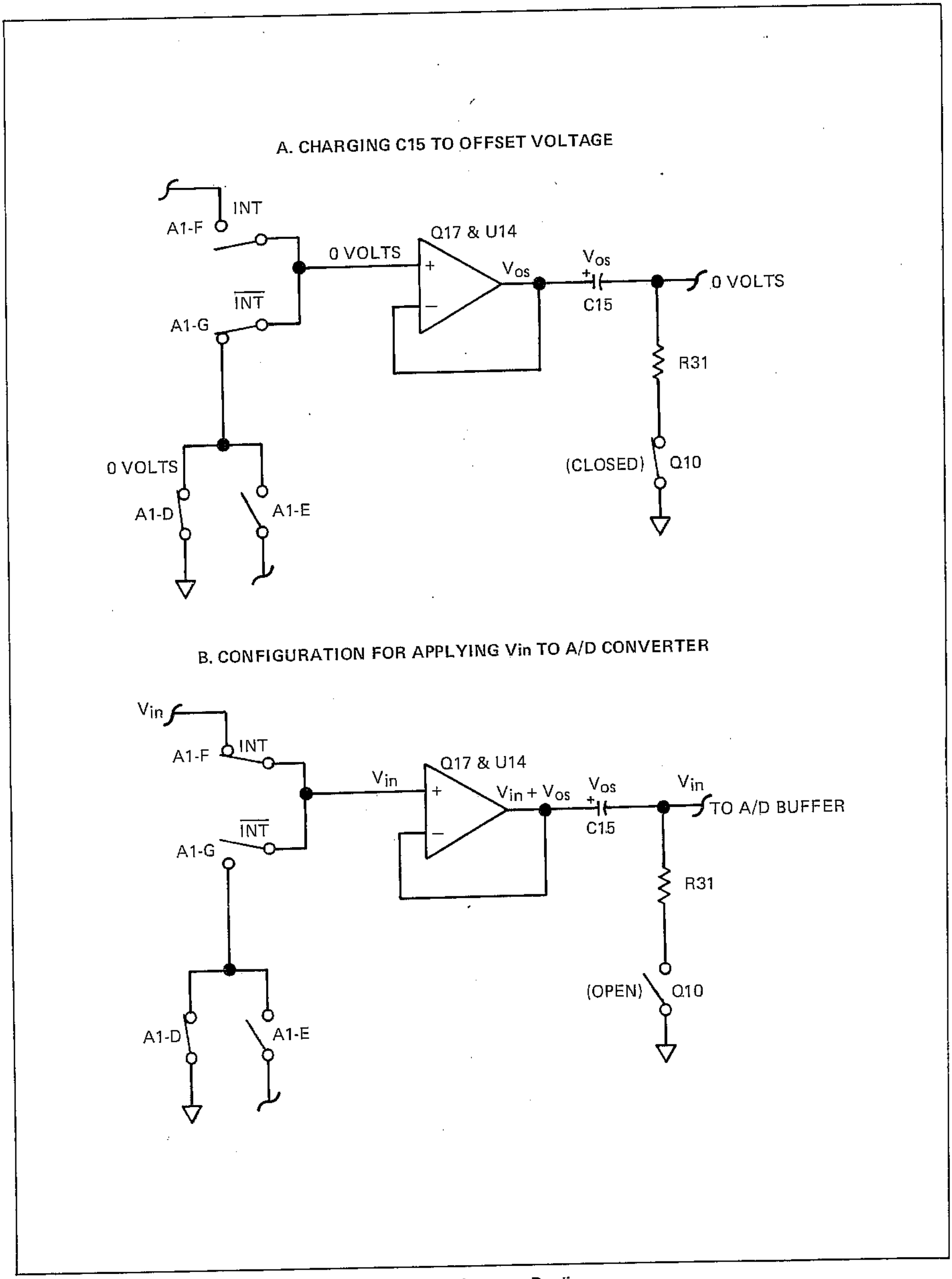


Figure 3-3. Autozero Routine

3-66. During the measurement cycle, switching signals are capacitively coupled into the input node of Q17. Capacitor C1 is driven with the $\overline{INT}$ signal to correct for charge injection errors.

3-67. AC BOOTSTRAP AMPLIFIER

3-68. Operational amplifier U6B is capacitively coupled to the non-inverting input of Q17. At higher frequencies U6B operates as a bootstrap to compensate for the high frequency rolloff of ac signals in the 200 mV and 2V ranges. The rolloff is due to the parasitic capacitance of the JFET switches connected to pin 17 of A1. Amplifier U6B has a gain of 1.75 to 2.00 (depending on how R29 is set). JFET Q19 is turned on for VDC and ohms measurements to reduce the gain of U6B. This gain reduction eliminates charge transfer through C17 during the autozero process, and keeps input bias current to a minimum. The charge transfer is especially evident when making high resistance (greater than 10 megohm) measurements.

3-69. RMS-to-DC Converter (Schematic 8860A-1004, Sheet 2 of 2)

3-70. The RMS-to-DC Converter, hereafter referred to as the RMS Converter, is located on the AC/DC Scaling PCB. For the VAC and the VAC+VDC functions the converter generates a positive dc voltage with a magnitude equal to the true rms value of the input (up to crest factor of 3). The RMS Converter, shown in Figure 3-4, computes the rms voltage using a log-antilog circuit.

3-71. The following description of the RMS Converter is divided into four separate sections:

1. Absolute Value Converter
2. 2X Log Amplifier
3. Log Feedback Amplifier
4. Antilog Amplifier

3-72. The absolute value converter, composed of U8 and its associated components, forms a full-wave rectifier which converts a bipolar voltage to a positive collector current at U17A. A positive input voltage (Vin) causes a collector current of Vin/40k (I_1 in Figure 3-4). When Vin is positive, I_2 is zero since CR6 is off; diode CR7 is turned on.

3-73. A negative input voltage (Vin) produces the same U17A collector current, but in a different manner. Diode CR6 is turned on, and CR7 is turned off. The negative input voltage appears at the cathode of CR6, inverted (with unity gain). Half of current I_2 flows through the 40 kilohm resistor and the other half (Vin/40k) flows into the collector of U17A.

3-74. The offset compensation amplifier U15 corrects for the dc offset of U8. The correction improves the dc stability of U8 over the operating temperature range of the 8860A.

3-75. The 2X Log Amplifier takes the logarithm of the U17A collector current and multiplies the logarithm by 2. Transistors U17A and U20A are the logarithmic elements in the amplifier. The logarithmic function is derived from the relationship of base-emitter voltage to collector current of a bipolar transistor.

3-76. A few components in the 2X Log Amplifier help to improve stability and high frequency response. For example, Q14, a transconductance amplifier, assures loop stability; RC network R75 and C41 provide ac compensation; and R61 adjusts the loop gain of the circuit to improve high frequency response. Low voltage power supplies are used with U16 to ensure low power dissipation and improved stability.

3-77. The amplifier consisting of U19A and U20B performs the antilog function of the RMS Converter. The collector current of U20B (V3/400 kΩ) is logarithmically related to the difference between its base and emitter voltages (V2 and V1). Capacitor C34 operates as a filter and U19B operates as the log feedback amplifier.

3-78. In operation the output of U19A is a dc voltage equal to five times the rms value of the input to the RMS Converter. At full scale, its output is 10V. Resistive divider network U18 divides the output of U19A by five to obtain a full scale output of 2 volts. Jumper wires W5 through W8 are removed as necessary during factory calibration to bring the divider output within the adjustment range of R67. The output is filtered by R59 and C32 before being applied to the A/D Converter.

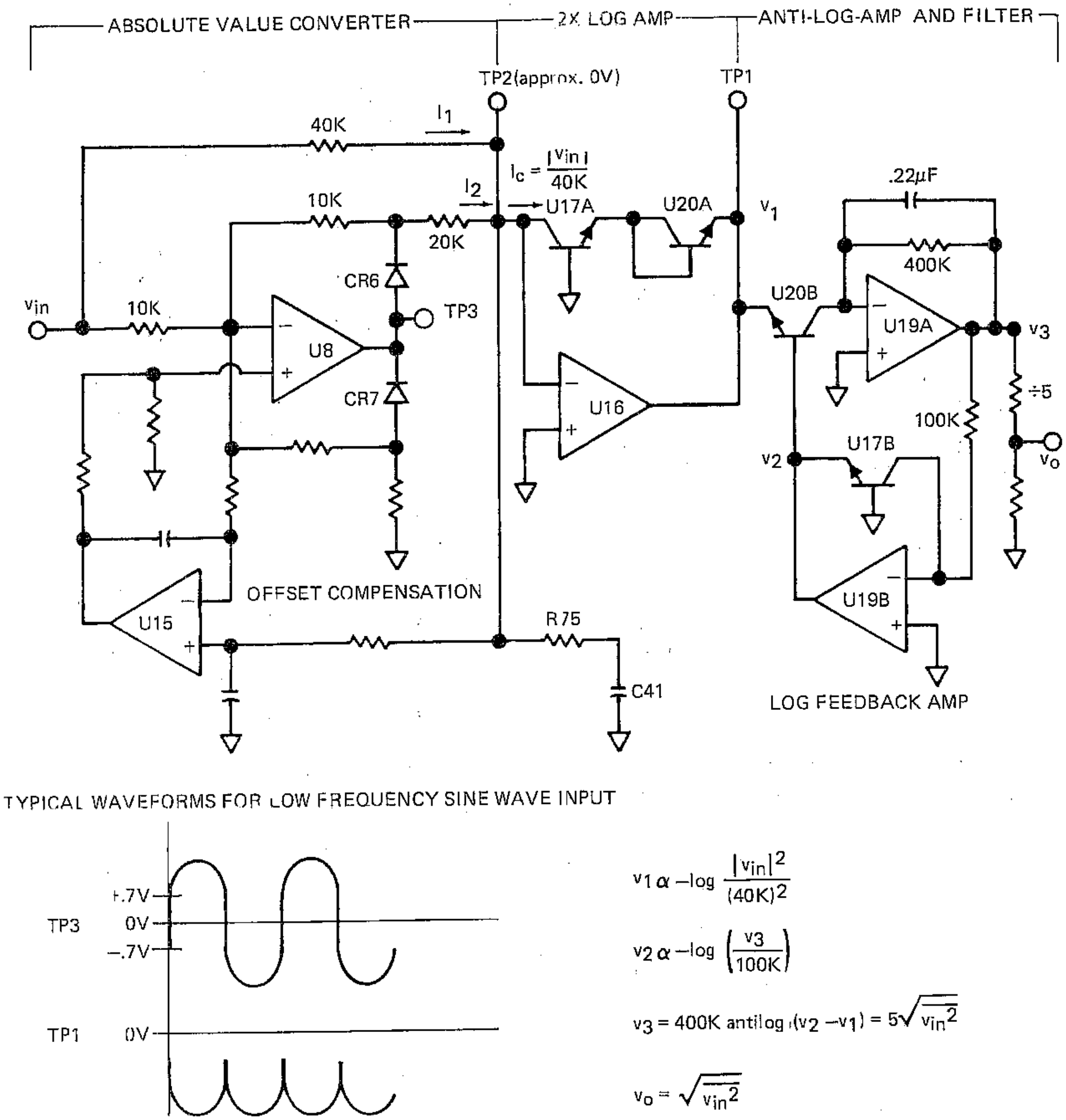
3-79. Jumpers W5 through W8 are selectively cut at the factory during pre-calibration, and should not be altered unless the U17 or U20 transistor arrays are replaced. See Table 4-5 for the jumper selection guide.

3-80. Ohms Converter (Schematic 8860A-1005, Sheet 1 of 2)

3-81. The Ohms Converter is physically located at the forward end of the A/D and Ohms Converter PCB. The Ohms Converter is enabled when the Ω2T or Ω4T function is selected. Circuit operation is the same for both functions. The Ohms Converter supplies a source current through the unknown resistance (Rx), generating a dc voltage proportional to Rx. This voltage is sensed and measured in the same way as a dc input voltage, but is displayed in ohms.

3-82. SOURCE CURRENT

3-83. Figure 3-5 shows a simplified schematic of the Ohms Converter. Source current for Rx flows through relay K4, to the front panel terminal labeled INPUT HI, through Rx (the resistor being measured), and returns to the source through the INPUT LO terminal. This current is scaled according to the selected resistance range. The scaled values for each range are shown in Table 3-1. The 200Ω range has a 1 mA source current and produces a full-range voltage of 200 mV. All other ranges produce a 2 volt output at full-range.



$$v_1 \alpha -\log \frac{|v_{in}|^2}{(40K)^2}$$

$$v_2 \alpha -\log \left(\frac{v_3}{100K}\right)$$

$$v_3 = 400K \text{ antilog } (v_2 - v_1) = 5\sqrt{\overline{v_{in}^2}}$$

$$v_o = \sqrt{\overline{v_{in}^2}}$$

Figure 3-4. RMS-to-DC Converter — Simplified Schematic

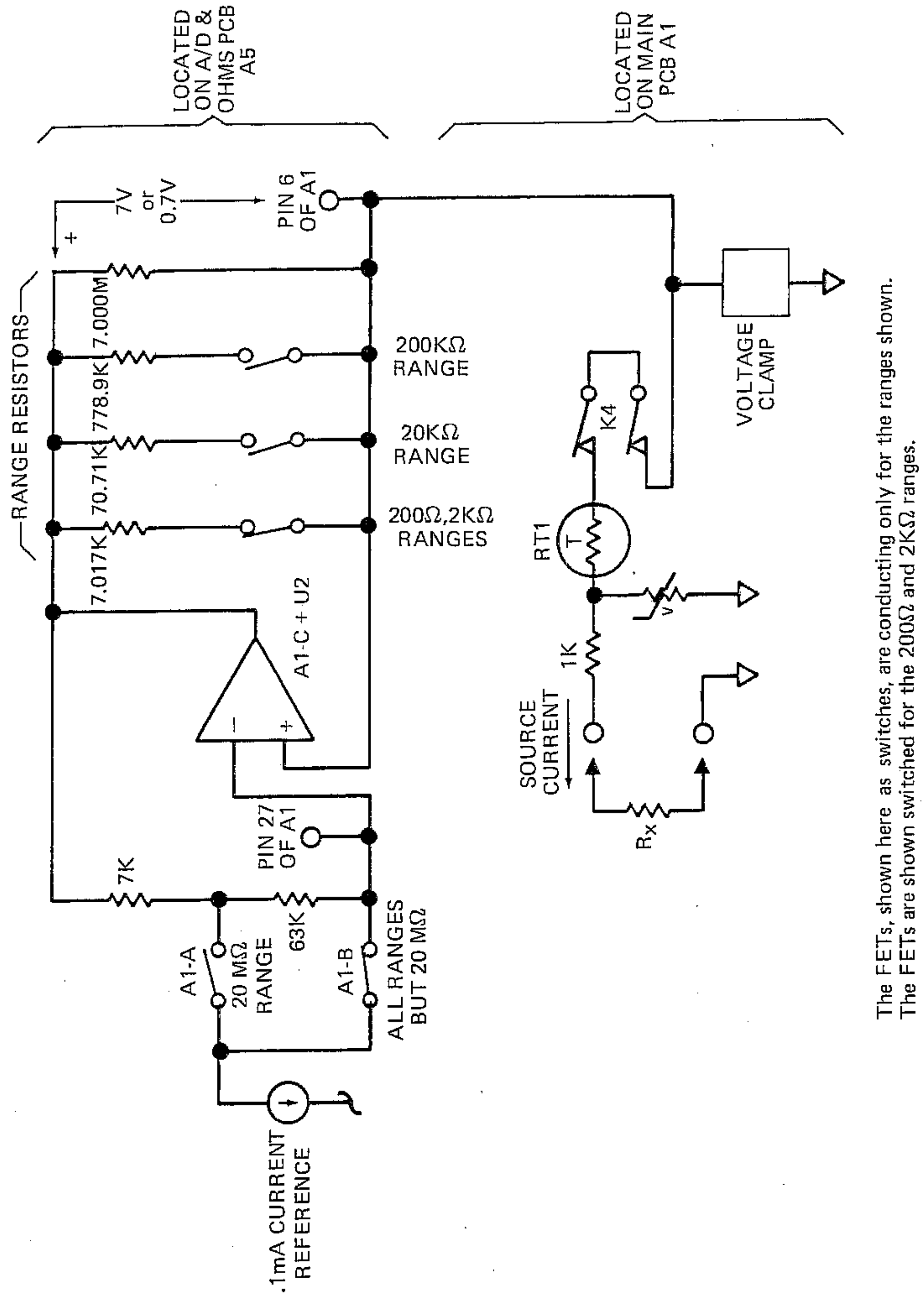


Figure 3-5. Ohms Converter—Simplified Schematic

3-84. RANGING VIA JFET SWITCHING

3-85. The ranging resistors are switched into the circuit by a series of JFETs located on the A1 hybrid assembly. ICs U6 and U7 are quad comparators with open-collector outputs. They translate digital control signals to voltage levels suitable for driving JFET switches. The JFET gate voltage requirements are -15 volts for turn off and a value equal to the channel voltage for turn on. The 2 to 4 decoder, U21, controls (through U6 and U7) the selection of four precision range resistors. The U21 truth table is given in Section 8, Ohms Converter.

3-86. On the lowest five resistance ranges, the 0.1 mA reference current flows through 70 kΩ (R9 + 63K + 7K) to produce a constant +7 volt drop across the enabled range resistor. Holding the voltage across the selected range resistors produces the constant source current for Rx. For example, on the 200Ω range, +7 volts across 7 kilohms produces a 1 mA source current. On the 20 MΩ range, JFETs A1-A and A1-B switch the 0.1 mA through the 7 kilohm reference resistor, producing a +0.7 volts drop across the 7 megohm reference resistor. The 0.7 volt drop maintains the 0.1 μA source current for Rx.

3-87. Amplifier U4, configured as a unity-gain amplifier, tracks the channel voltage of the A1 switching FETs. The output of U4 is used to supply the on-state gate bias voltage for all of the A1 switching JFETs. By tracking the voltage at pin 6 of A1, U4 maintains a constant, low junction voltage for all input voltages, thus keeping leakage effects constant. U4 also bootstraps the protection circuit on the main board to minimize leakage errors.

3-88. A/D Converter (Schematic 8860A-1005, Sheet 2 of 2)

3-89. The A/D Converter is located on the A/D and Ohms Converter PCB. Its purpose is to convert a measured quantity from analog to digital form for the purpose of display. Figure 3-6 is a simplified circuit diagram of the A/D Converter. The entire A/D conversion process, including timing, is under the control of the in-guard microprocessor. The A/D Converter indicates the polarity of the input (for selection of the reference) and signals the processor when the correct count has been reached.

3-90. The A/D Converter uses a dual-slope conversion technique and operates in both polarities. The dc voltage input to the A/D Converter represents the unknown resistance or voltage at the 8860A input terminals. This dc voltage is integrated (charges C7) for a fixed amount of time, called the integration period; see Figure 3-7. At the end of this period the input of the A/D converter switches to either an internal or an external reference voltage with a polarity that is opposite that of the input voltage. This discharges capacitor C7 at a controlled rate. A comparator interrupts the microprocessor and ends the discharge period when the charge remaining on C7 is equal to the charge that was present just prior to integration.

3-91. Figure 3-7 illustrates and describes the various periods within a measurement cycle. Figures 4-4 and 4-5 in Section 4 of this manual give the associated JFET timing diagrams and signal waveforms.

3-92. The in-guard microprocessor derives the digital readout by counting at a 1 MHz rate during the discharge cycle. If the counter reached 199,999 counts without being interrupted (in the 5-1/2 digit mode), the display will indicate overrange.

3-93. PRECISION VOLTAGE REFERENCE

3-94. The Precision Voltage Reference, Figure 3-8, provides the voltage standard for all 8860A measurements by establishing a precise discharge rate for C7. Reference amplifier U22 is a temperature compensated 6.5 volt zener reference. Op amp U23A is connected in a bootstrap configuration to supply a very stable +11 volt output to R40 and R41, assuring highly stable currents for U22. Resistor R40 sets the zener current. Resistors R41 and R42 are selected to set the correct temperature compensation current for the reference amplifier.

3-95. Amplifier U23B fixes the collector of U22 at zero volts and buffers the output of U22 for use by the reference divider network, U10. Jumper wires W4-W8 are removed as necessary during factory calibration to bring the reference divider output voltage within the adjustment range of R17. Diode CR11 and R44 assure that the reference circuit always powers up to the correct polarity.

3-96. PRECISION CURRENT REFERENCE

3-97. Amplifier U5 taps 5.480V dc from U10 and applies it to R11 and R12 to generate a precise 0.1 mA dc reference current for the Ohms Converter. JFET Q3 assures a constant output current over the entire compliance voltage range of the Ohms Converter.

3-98. A/D SWITCHING NETWORK

3-99. Hybrid A2 on the A/D Converter PCB contains a series of JFET switches. These switches are used to perform the following functions:

1. Select the VDC, Ohms (via A2-C), or VAC (via A2-D) functions for processing during the integrate period.
2. Enables the internal reference (via A2-B) or the external reference (via A2-A) for use during the counting period. (This selection is made from the front panel.)
3. Switches the polarity of the 1V reference (via A2-F, G, H, and C14) for the A/D Converter.

3-100. Items 2 and 3 are described further under Internal/External Reference.

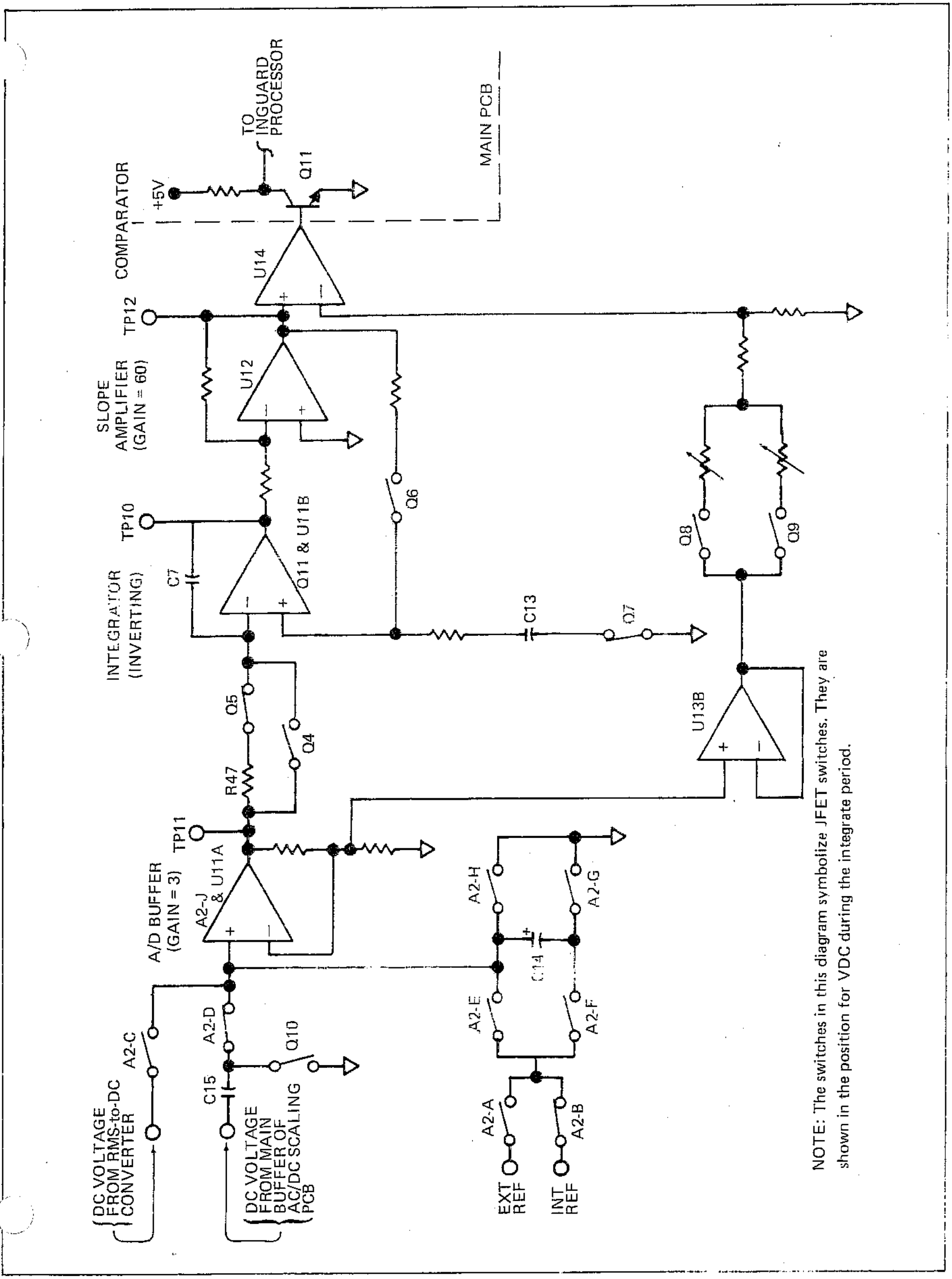
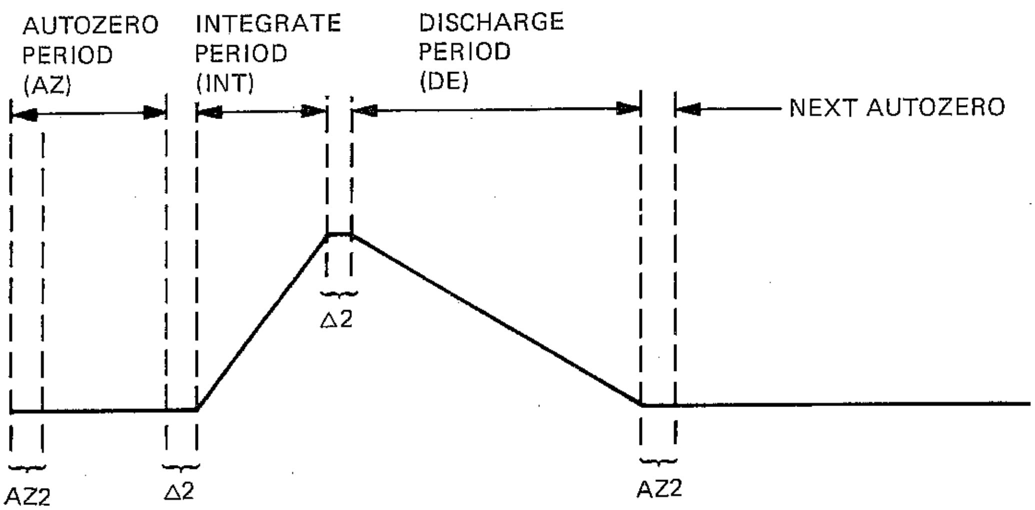


Figure 3-6. A/D Converter—Simplified Schematic



AUTOZERO PERIOD (AZ)

The initial small voltages on C7 and C13 are established during this period with Q6 switched on and the A/D buffer input grounded through A2-H. AZ2 assures fast recovery from overloads.

TIME-OUT PERIODS (Delta-2)

Each of these .5 ms periods allows the A/D buffer to respond to the switched-in voltage and settle, before the voltage is applied to the integrator.

INTEGRATE PERIOD (INT)

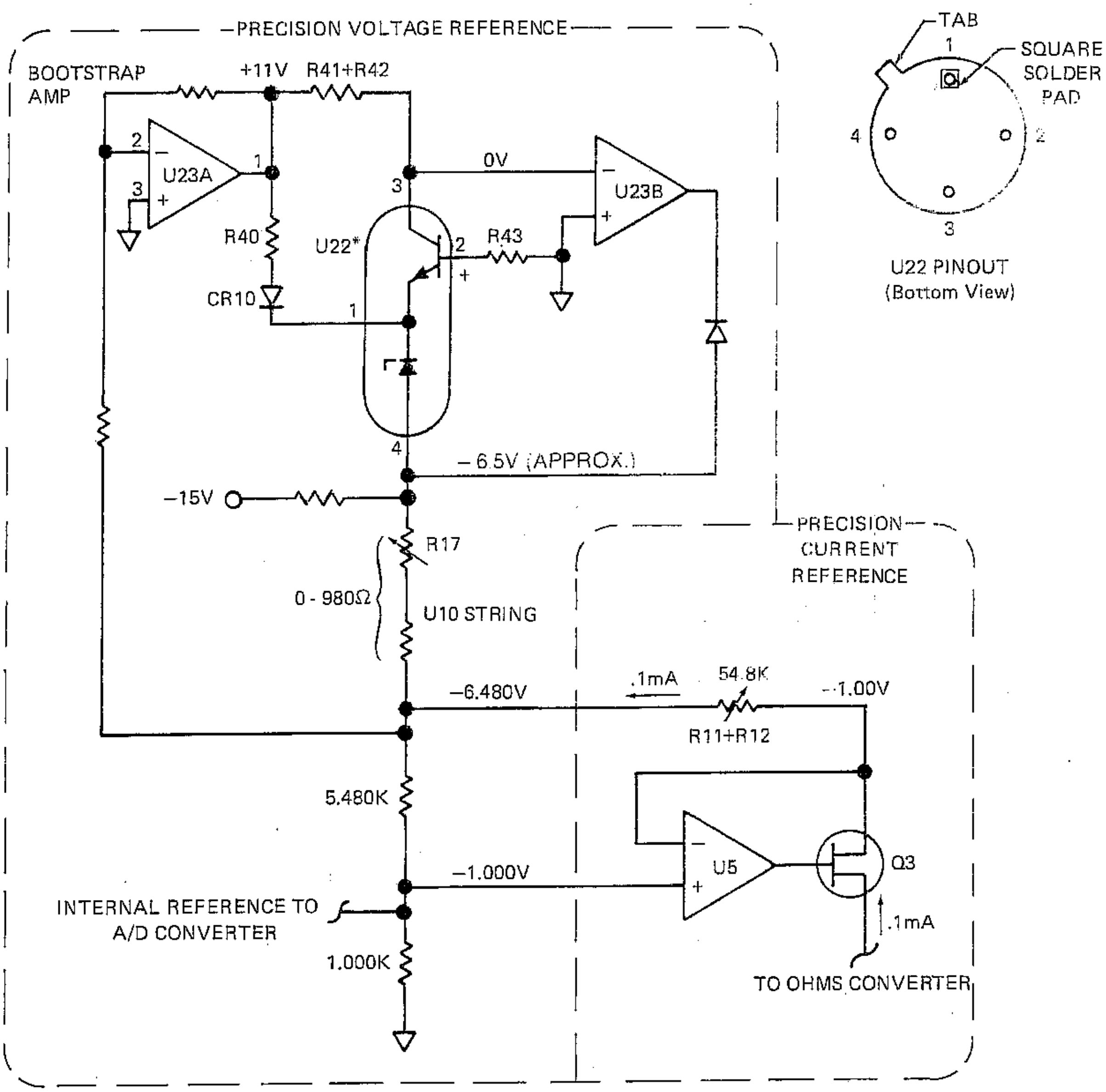
C7 charges to a voltage proportional to the applied input. The length of the integrate period depends on the sample rate chosen, as follows:

RESOLUTION	AC LINE FREQUENCY	INTEGRATION PERIOD (INT)	MEASUREMENT CYCLE (approximate)
5½ digit	50 Hz or 60 Hz	100 ms	400 ms
4½ digit	50 Hz 60 Hz	20 ms 16-2/3 ms	66.7 ms
3½ digit	50 Hz or 60 Hz	2 ms	20 to 50 ms

DISCHARGE PERIOD (DE)

C7 discharges for a length of time proportional to the applied input, during which digital counts accumulate. This count represents the value of the input resistance or voltage being measured. The rate of discharge is the same for all A/D conversion speeds when the internal reference is chosen.

Figure 3-7. A/D Converter Measurement Cycle



*R41, R42, and U22 are replaced only as a set.

Figure 3-8. Precision Voltage and Current References—Simplified Schematic

3-101. The JFET switches of A2 are controlled by comparators U15 through U18, which in turn are controlled by the in-guard microprocessor. The timing for the JFET switches is shown in Figure 4-4. IC U21 decodes two lines from the microprocessor into a 1-of-4 output.

3-102. Amplifiers U13A and U13B supply gate bias to JFET switches which must conduct non-zero voltages. This bias arrangement assures a constant switch resistance for all voltage levels.

3-103. A/D BUFFER

3-104. The A/D buffer, as shown in Figure 3-6, consists of dual JFET A2-J and amplifier U11A. The buffer receives a scaled dc input from the AC/DC scaling circuits, amplifies the input by a factor of 3, and provides the integrator with the amplified signal.

3-105. INTEGRATOR AMPLIFIER

3-106. The integrator consists of Q11, U11B, R47 and C7. JFET Q5 is on during the integrate and discharge periods to allow C7 to charge and discharge. JFET Q5 is switched off for 0.5 ms (Delta-2) before the charge and discharge periods. Clamp transistor Q12 ensures that Q5 does not conduct current during these off times. The Delta-2 periods serve to isolate the integrator from transient voltages due to switching of the A/D buffer input. In addition, input polarity is sensed during the second Delta-2 so that the appropriate reference can be applied to the A/D buffer.

3-107. JFET Q4 is normally off and Q7 is normally on. However, they change state simultaneously for a short time (called AZ2) at the beginning of the autozero period. Q4 switches on during AZ2 to rapidly remove any residual charge on C7. Q7 switches off to minimize disturbance of the charge stored on C13 during the previous autozero. The AZ2 period is the key to high-speed operation of the A/D Converter (4-1/2 and 3-1/2 digit modes). AZ2 also assures rapid overload recovery. Resistors R22 and R23 provide a small amount of linearity correction.

3-108. INTERNAL/EXTERNAL REFERENCE

3-109. The selected reference, internal or external, is applied to the A/D Buffer during the discharge period. The internal reference is a precise +1 or -1 volt level. It is applied with a polarity opposite the scaled dc input voltage in order to discharge C7. The precision -1 volt internal reference is available via JFET A2-B.

3-110. The +1 volt reference is derived by storing the precision -1 volt level on capacitor C14 and then reversing the capacitor's connections. JFETs A2-F and A2-H are switched on for the duration of the autozero period to charge C14. When the positive reference is required, A2-G is switched on during the discharge period.

3-111. An external reference voltage may be of either polarity since the A/D Converter incorporates a precision inversion circuit. The inversion is accomplished by connecting C14 to the reference voltage during autozero and reversing the capacitor's connections during the discharge period.

3-112. SLOPE AMPLIFIER AND COMPARATOR

3-113. Op amp U12 is configured as an inverting amplifier with a gain of 60. Its output is used to improve the accuracy of zero-crossing detection (via U14) at the end of the discharge period, and to assure accurate and repeatable autozeroing of the integrator during the autozero period (via Q6). JFET Q6 conducts during the autozero period to close the loop which initializes the voltages on C7 and C13.

3-114. The comparator is composed primarily of U14, and includes Q11 on the Main PCB. The output of the comparator indicates polarity during the second Delta-2, and interrupts the counter at the end of the discharge period.

3-115. Diodes CR5, 6, 8, and 9 limit the slope amplifier output to ensure pinchoff of Q6 during the integrate and discharge periods. A dc voltage (70 mV to 120 mV) determined by R29 and R30 is applied to U14-4 during the discharge period. When the output of the slope amplifier reaches the same voltage as U14-4, the comparator changes state and interrupts the in-guard microprocessor. Q9 is enabled for positive inputs, and Q8 for negative inputs.

3-116. In-Guard Microprocessor (Schematic 8860A-1001)

3-117. The in-guard controller is an 8-bit microprocessor, complete with RAM and ROM. It plugs into a socket on the Main PCB Assembly and controls the entire measurement cycle. Measurement cycle control includes:

1. Implementing front panel selections: function, range, autoranging, zero, filter, sample rate, external reference, and trigger arm.
2. Timing the JFET switching associated with the A/D Converter.
3. Transmitting the measured value to the out-guard microprocessor at the end of every measurement cycle.

3-118. The in-guard microprocessor controls autoranging. When autoranging is selected, the 8860A begins in the highest range and downranges. If the input signal represents less than 18000 counts (in the 5-1/2 digit mode), the 8860A switches to the next lower range. If at any time the input signal represents more than 199999 counts, the 8860A upranges.

3-119. The front panel ZERO function allows the in-guard microprocessor to store an offset value for the

VDC and resistance measurement functions (2- or 4-terminal). The value is stored in three separate and independent RAM locations, and is subtracted from measured value before sending it to the out-guard microprocessor.

3-120. The in-guard microprocessor is powered by the +5V in-guard supply. A reset circuit at U6-39 momentarily holds the microprocessor in the reset state during power-up to initialize internal conditions.

3-121. Guard-Crossing Circuitry (Schematic 8860A-1001)

3-122. The guard-crossing, located on the Main PCB Assembly, is an optically coupled data transmission path for communication between the in-guard and out-guard microprocessors. The use of opto-isolators allows a differential of up to ± 500 volts between out-guard common and in-guard common.

3-123. Communication between the microprocessors employs detection and correction, and is fully self-restarting when data is lost or incorrectly transmitted. Inadvertent loss of data is usually indicated by an error message on the display.

3-124. In each direction there are two transmission paths, clock and data, which carry parallel signals. Transmissions either direction, out-guard to in-guard (through U9 and U10) or in-guard to out-guard (through U7 and U8), are fully symmetrical. The following description of one of the guard-crossing data paths applies to all four.

3-125. A digital signal from J3-15 (Controller PCB connector) drives the inverting input of a comparator in U2. The output of the comparator drives the input of optoisolator U10. A low input to U10 produces an isolated high output level (+0.42 to +0.6V dc). This signal drives the inverting input of another comparator (contained in U5) that has a switching threshold of +0.2 volts to 0.35 volts. The output of this comparator (pin 14) drives U6-14, the Receive Clock input to the in-guard microprocessor. The signal is inverted three times in crossing the guard, resulting in a net signal inversion.

3-126. Out-Guard Microprocessor (Schematic 8860A-1003)

3-127. The out-guard controller U2 is an 8-bit microprocessor which plugs into a socket on the A3 Controller PCB Assembly. It is supported with external ROM and expanded I/O capability.

3-128. OUT-GUARD MICROPROCESSOR SOFTWARE

3-129. The out-guard microprocessor (U2) has an external program ROM (U9). This ROM contains the program which operates the 8860A in the local mode; another ROM takes over in the remote mode. From local ROM, the out-guard microprocessor:

1. Reads the front panel keys and internal switches.
2. Communicates front panel selections to the in-guard microprocessor.
3. Passes all triggers to the in-guard microprocessor, including continuous triggers and those from manual, external, and bus sources.
4. Receives measurements from the in-guard microprocessor.
5. Processes numerical data entered from the front panel.
6. Performs limits and peak to peak comparisons.
7. Performs offset subtraction.
8. Controls the display and front panel LEDs.
9. Performs self-diagnostic error checks.
10. Interfaces with the two digital options: the Calculating Controller (-004) and the IEEE-488 Interface (-005).

3-130. Table 3-2 shows how the various ROMs are sectioned into four address spaces, and how each section is accessed using ports P23, P26, and P50. The table also shows the state of the control lines for each ROM device. The RAM internal to the out-guard microprocessor holds the three stored values for offset, high limit, and low limit.

3-131. OUT-GUARD MICROPROCESSOR HARDWARE

3-132. The four major components which suport the operations listed previously are located on the Controller PCB. They are:

1. U2, Out-Guard Microprocessor
2. U9, Local Program Memory (ROM)
3. U10, 8-Bit Latch
4. U3, I/O Expander

3-133. Operating power for the Controller PCB Assembly comes from the +5 volt out-guard supply. At power-up, capacitor C1 charges slowly through an internal resistor in U2 to release the reset line (pin 4) after a delay. This initial delay sets the logic on the Controller PCB Assembly to a known state on power-up.

Table 3-2. Out-Guard ROM Selection

	ROM DEVICE (IEEE)	ROM DEVICE (CALC.)	ROM ADDRESS	PORT NO. P23 U2-24	PORT NO. P26 U2-37	PORT NO. P50 U3-1
BASIC INSTRUMENT (LOCAL ROM)	U9		0-2047	0	X	0
			2048-4095	0	X	1
OPTION (OPTION ROM)	IEEE	CALC.				
	U4	U10	0-2047	1	0	X
		U19	2048-4095	1	1	X

X = don't care

Device/pin numbers refer to schematic 8860A-1003, Controller circuit board; U2-24, for example, means device U2, pin 24.

3-134. The out-guard microprocessor communicates with the other ICs (U9, U10, and the two digital options) by way of the data bus, lines D80 through D87. This bus is multiplexed; the data and the eight lower-order address bits appear at different times on these lines. The eight-bit latch (U10) holds the address at its output for the local program memory (U9). The address is latched from the data bus by a signal called ALE (Address Latch Enable). ALE is generated by the out-guard microprocessor.

3-135. The local ROM U9 actually requires a total of 12 address bits. The upper four bits of U9 are static during program memory read operations; the processor outputs them directly to U9 on lines P20 to P23.

3-136. The I/O Expander U3 expands lines P20 through P23 to 16 bits. Table 3-3 shows the functions that are assigned to each pin of U3. Notice that most of the pin assignments are bidirectional (input and output data). This expanded I/O operates the multiplexed display, reads the option identification, and reads the three slide switches S1, S2, and S3. The pin labeled PROG controls the timing of U3.

3-137. The display receives its control from the output ports of U2 and U3. Non-inverting drivers U4, U5 and U7 buffer the port outputs. Resistor network U6, and resistors R4, R5, and R6 are series resistors to limit the drive current to the display LEDs.

3-138. The two D-type flip-flops of U1 operate as signal conditioners for the out-guard microprocessor. The first flip-flop (pins 1-5) is part of the external trigger circuitry. The second (pins 9-13) conditions signals arriving from the installed digital option. The IEEE-488 option uses this line to interrupt the out-guard microprocessor. The Calculating Controller option, however, uses this line as simply another input to the out-guard microprocessor.

3-139. EXTERNAL TRIGGER CIRCUITRY

3-140. The external trigger circuit is designed to trigger from either a switch opening or a rising TTL signal. The signal passes through two stages of conditioning. One-shot U11, when triggered, eliminates switch bounce by producing a positive output pulse of approximately 40 ms. This pulse sets D-type flip-flop U1 to signal the microprocessor that a trigger has been received. The microprocessor clears the flip-flop after it detects the set condition.

3-141. Front Panel Push Buttons (Schematic 8860A-1002)

3-142. The front panel push buttons are scanned by the out-guard microprocessor at the rate of two keys every 2.5 ms (regardless of the A/D sample rate). The out-guard microprocessor interrupts whatever it is doing to perform this function. (The IEEE-488 option causes the scan rate to slow when certain bus interrupts occur. This is because data communication between the GPIA and the out-guard microprocessor has priority over the 2.5 ms scan interrupts.)

3-143. A binary sequence at the input of U1 (pins 13, 14 and 15) sets each of the eight output lines of U1 low, one at a time. In this way the sixteen keys are strobed a column at a time through diodes CR1 through CR8. The two strobed keys are read simultaneously via pins 16 and 17 of J1. A line is low (at zero volts) only if the corresponding key is depressed. Thus the entire keyboard is read over a 20 ms interval.

3-144. Display (Schematic 8860A-1002)

.45. The same U1 strobe lines that scan the front panel push-buttons also strobe the eight display digits, 6 decimal points, 2 units annunciators, and 15 indicator lights. When pin 1 of U1 goes low, Q1 turns on, activating the first seven segment readout and three indicator lights. Signals applied to the cathodes of the segments determine which segments will light. As this first column of lights is lit, all other columns (transistors Q2 through Q8 and their display lights) are turned off. The eight columns are strobed one at a time, at a rate high enough to make all digits appear to be on at the same time. A timer interrupt occurs every 2.5 ms (except with IEEE-488 Interface) to advance columns. The sequence continues in an unending loop, completing a full cycle once every 20 ms.

Table 3-3. I/O Expander (U3) Pin Assignments

PORT	U3 PIN NO.	OUTPUT FUNCTION	INPUT FUNCTION
P40	2	Send data } Guard crossing bit	Test Mode 0 switch (S3)
P41	3	Send clock } Guard crossing bit	Test Mode 1 switch (S1)
P42	—	(not used)	(not used)
P43	—	(not used)	(not used)
P50	1	ROM bank switch control	(pulled to logic 0)
P51	23	LSB } Annunciator data	50/60 Hz switch (S2)
P52	22	middle bit } Annunciator data	(not used)
P53	21	MSB } Annunciator data	(not used)
P60	20	LSB } Front panel scan data	ID0 } Option Identification
P61	19	middle bit } Front panel scan data	ID1 } Option Identification
P62	18	MSB } Front panel scan data	ID2 } Option Identification
P63	17	(not used)	ID3 } Option Identification
P70	13	(not used)	Receive data } Guard crossing bit
P71	14	(not used)	Receive clock } Guard crossing bit
P72	15	(not used)	Bottom row } Front panel keyboard
P73	16	(not used)	Top row } Front panel keyboard