Errata

Title & Document Type: **8170A Logic Pattern Generator Operating and Service Manual**

Manual Part Number: **08170-90001**

Revision Date: **November 1978**

About this Manual

We've added this manual to the Agilent website in an effort to help you support your product. This manual provides the best information we could find. It may be incomplete or contain dated information, and the scan quality may not be ideal. If we find a better copy in the future, we will add it to the Agilent website.

HP References in this Manual

This manual may contain references to HP or Hewlett-Packard. Please note that Hewlett-Packard's former test and measurement, life sciences, and chemical analysis businesses are now part of Agilent Technologies. The HP XXXX referred to in this document is now the Agilent XXXX. For example, model number HP8648A is now model number Agilent 8648A. We have made no changes to this manual copy.

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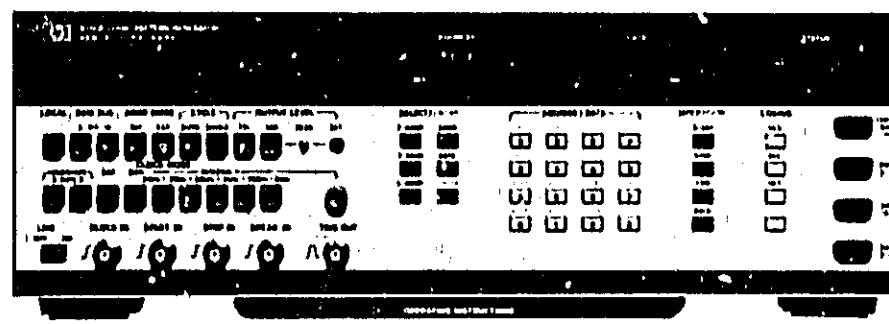
Agilent Technologies

HP8170A

OPERATING AND SERVICE MANUAL

8170A

LOGIC PATTERN GENERATOR



HEWLETT hp PACKARD

HP 8170A

SAFETY

This product has been designed and tested according to International Safety Requirements. To ensure safe operation and to keep the product safe, the information, cautions, and warnings in this manual must be heeded. Refer to Section I for general safety considerations applicable to this product.

CERTIFICATION

Hewlett-Packard Company certifies that this product met its published specifications at the time of shipment from the factory. Hewlett-Packard further certifies that its calibration measurements are traceable to the United States National Bureau of Standards, to the extent allowed by the Bureau's calibration facility, and to the calibration facilities of other International Standards Organization members.

WARRANTY

This Hewlett-Packard product is warranted against defects in material and workmanship for a period of one year from date of shipment. During the warranty period, Hewlett-Packard Company will, at its option, either repair or replace products which prove to be defective.

For warranty service or repair, this product must be returned to a service facility designated by HP. However, warranty service for products installed by HP and certain other products designated by HP will be performed at Buyer's facility at no charge within the HP service travel area. Outside HP service travel areas, warranty service will be performed at Buyer's facility only upon HP's prior agreement and Buyer shall pay HP's round trip travel expenses.

For products returned to HP for warranty service, Buyer shall prepay shipping charges to HP and HP shall pay shipping charges to return the product to Buyer. However, Buyer shall pay all shipping charges, duties, and taxes for products returned to HP from another country.

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THE REMEDIES PROVIDED HEREIN ARE BUYER'S SOLE AND EXCLUSIVE REMEDIES. HP SHALL NOT BE LIABLE FOR ANY DIRECT, INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES, WHETHER BASED ON CONTRACT, TORT, OR ANY OTHER LEGAL THEORY.

ASSISTANCE

Product maintenance agreements and other customer assistance agreements are available for Hewlett-Packard products.

For any assistance, contact your nearest Hewlett-Packard Sales and Service Office. Addresses are provided at the back of this manual.

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OPERATING AND SERVICE MANUAL

8170A

LOGIC PATTERN GENERATOR

(Including Options 001, 002 and 907 to 910)

SERIAL NUMBERS

This manual applies directly to instruments with serial number 1739G00116 and higher. Any changes made in instruments having serial numbers higher than the above number will be found in a "Manual Changes" supplement supplied with this manual. Be sure to examine this supplement for any changes which apply to your instrument and record these changes in the manual.

D-7030 BÖBLINGEN, HERRENBERGER STR. 110
FEDERAL REPUBLIC OF GERMANY

MANUAL PART NO. 08170-90001
Microfiche Part No. 08170-95001

Printed: November 1978

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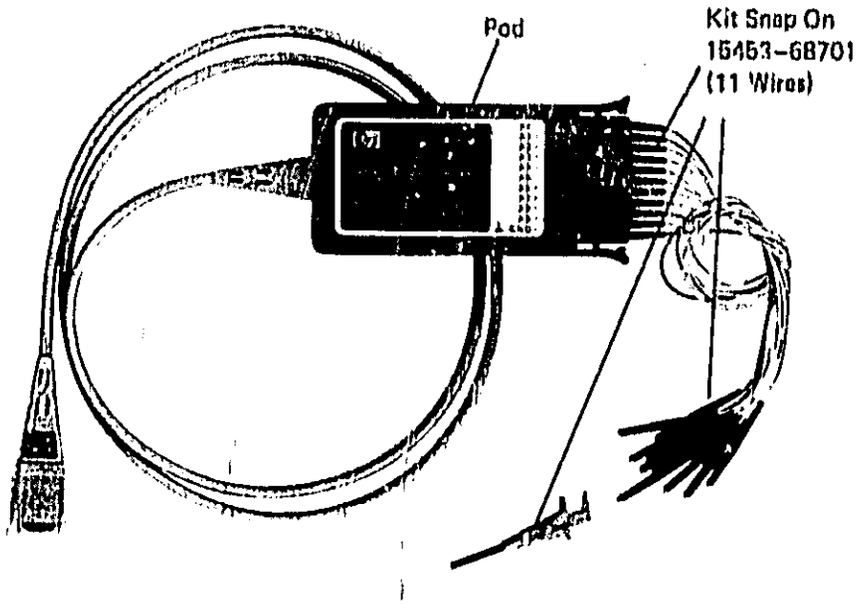
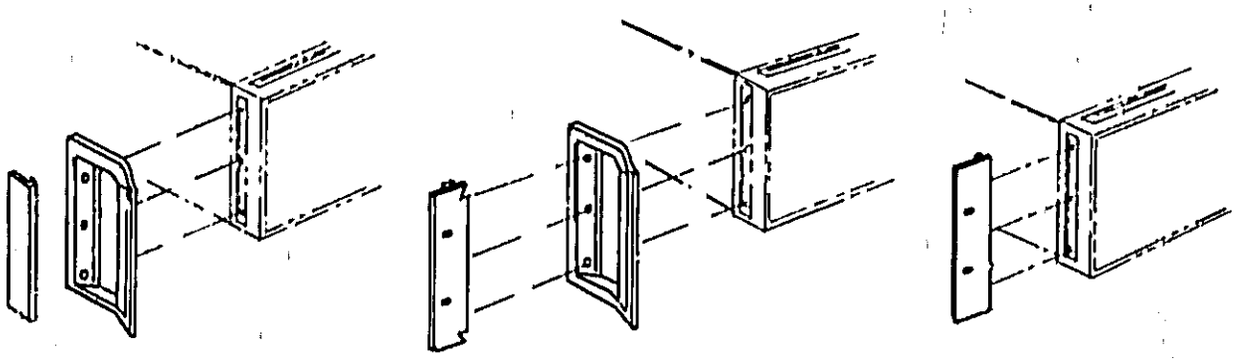


16462A ADDRESS DRIVER (OUTPUT) POD

Figure 1-2. Additional Supplied Accessory for 8170A Option 002

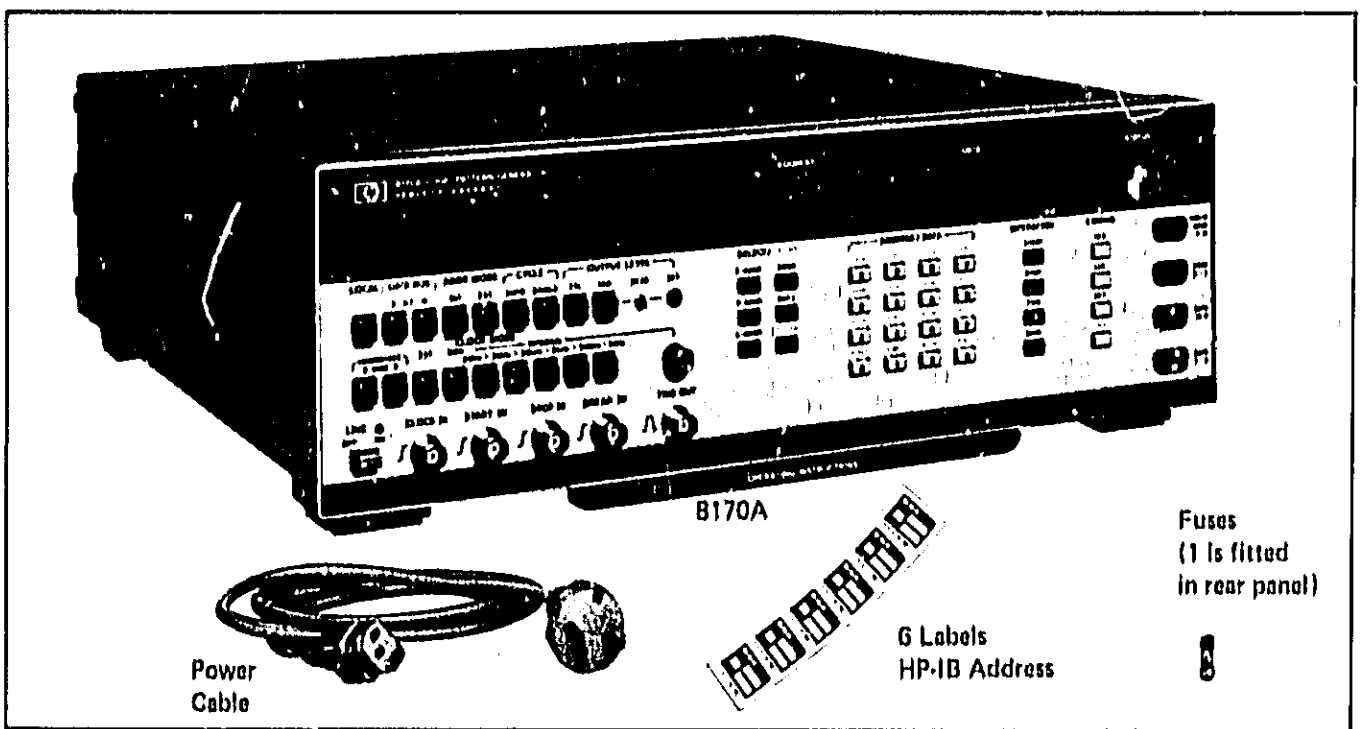


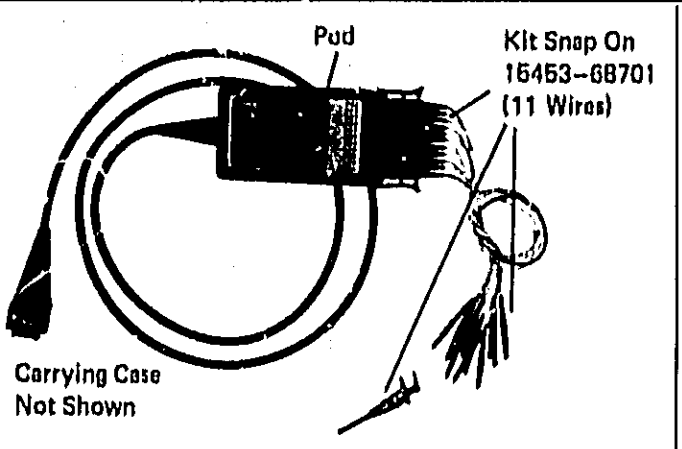
Front handle
Order Option 907
(HP Part No.
5061-0089)

Rack flange with front handle
Order Option 908
(HP Part No.
5061-0083)

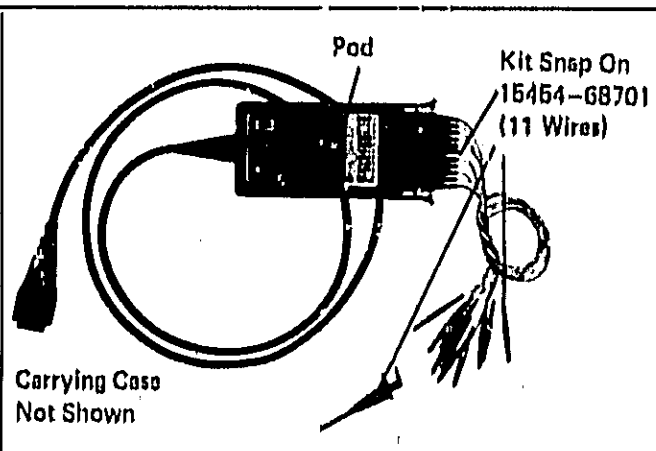
Rack flange
Order Option 908
(HP Part No.
5061-0077)

Figure 1-3. Available Rack Mounting Options/Accessories

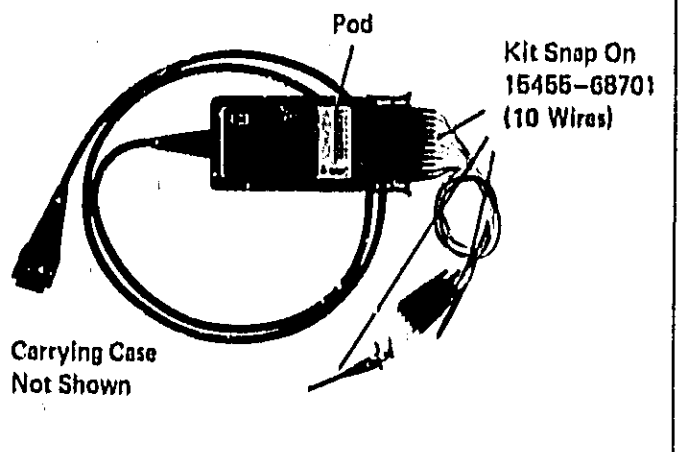




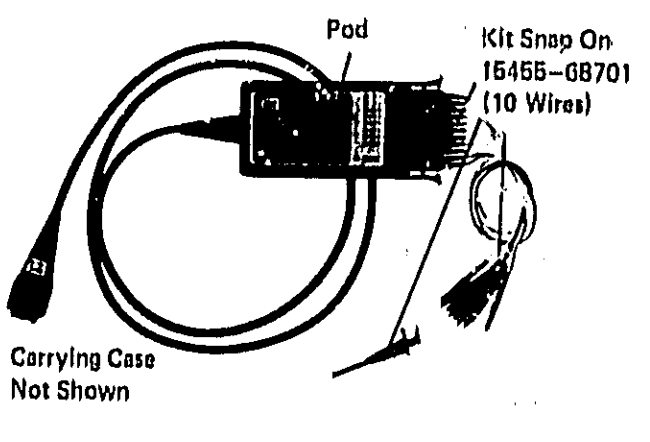
15453A ADDRESS INPUT POD



15454A CONTROL POD



15455A DATA OUTPUT D7-D0 POD



15456A DATA OUTPUT D15-D8 POD

Figure 1-1. 8170A and Supplied Accessories

SECTION I
GENERAL INFORMATION

1–1 INTRODUCTION

1–2 This Operating and Service Manual contains information required to install, operate, test, adjust and service the Hewlett-Packard Model 8170A. Figure 1–1 shows the mainframe and accessories supplied. This section covers instrument identification, description, accessories, specifications, and other basic information.

1–3 A Microfiche version of this manual is available on 4 x 6 inch microfilm transparencies (order number on title page). Each microfilm contains up to 60 photoduplicates of the manual pages. The microfiche package also includes the latest Manual Changes supplement as well as all pertinent Service Notes.

1–4 SPECIFICATIONS

1–5 Instrument specifications are listed in Table 1–2. These specifications are the limits against which the instrument is tested.

1–6 SAFETY CONSIDERATIONS

1–7 The Model 8170A is a Safety Class 1 instrument (it has an exposed metal chassis that is directly connected to earth via the power supply cable).

1–8 This operating and service manual contains information, cautions, and warnings which must be followed by the user to ensure safe operation and to maintain the instrument in a safe condition.

1–9 INSTRUMENTS COVERED BY MANUAL

1–10 Attached to the rear of this instrument is a serial number plate (Figure 1–4). The first four digits of the serial number only change when there is a significant change to the instrument. The last five digits are assigned to instruments sequentially. The contents of this manual apply directly to the instrument serial number quoted on the title page. For instruments with lower serial numbers, refer to the backdating information in Section VII of this manual. For instruments with higher serial numbers, refer to the Manual Change sheets at the end of this manual. In addition to change information, the Manual Change sheets may contain information for correcting errors in the manual. To keep this manual as up-to-date and accurate as possible, Hewlett-Packard recommends that you periodically request the latest Manual Change supplement. The supplement for this manual is identified with this manual's print date and part number, both of which appear on this manual's title page. Complimentary copies of the supplement are available from Hewlett-Packard.

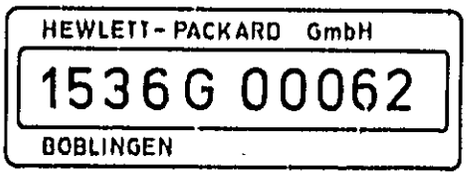


Figure 1–4. Serial Number Plate

1–11 DESCRIPTION

1–12 The HP Model 8170A Logic Pattern Generator is a real time test stimulus for functional checkout of multi-channel logic devices. Data output, suitable for 8- or 16-bit data busses, is generated from the 1024 x 8 bit freely-programmable memory. Data rate may be determined by internal or external clock, for functional testing, or by a 2- or 3 wire handshake for real time data traffic simulation. ROM's can be emulated by addressing the 8170A's keyboard-programmable memory externally. 16-line addressing is feasible. Manual address-shift is available in all modes. Auto or single cycle modes allow continuous or single generation of data between operator-defined first and last addresses. A trigger address, also operator-defined, provides a qualifier. Data output is TTL-compatible or variable CMOS selectable, and has 3-state (high impedance, 'transparent' to connected devices) capability. 3-State is invoked at the end of a single cycle, or on the application of an external stop signal. When programming the memory, data may be entered in binary, octal or hexadecimal codes. The 8170A is remote-programmable via HP-IB* and RS 232C.

* *Hewlett-Packard Interface Bus, Hewlett-Packard's implementation of IEEE Standard 488 "Standard Digital Interface for Programmable Instrumentation".*

1–13 **8170A Option 001 Extended Memory.** This option provides a total freely-programmable memory capacity of 4096 x 8 bit (2048 x 16 bit).

1–14 8170A Option 002 Address Driver Pod 15452A. Provides 10 address lines which output the 8170A's internally-generated address (memory comparison applications). Supplied complete with accessories as other pods, see § 1–19.

1–15 8170A Options 907, 908 and 909 provide handles and/or rack mounting accessories. Refer to Figure 1–3.

1–16 8170A Option 910 provides an additional manual.

1–17 All options will be delivered with the instrument if ordered at the same time as the instrument.

1–18 ACCESSORIES SUPPLIED

1–19 The 8170A is supplied complete with the following items (see Figure 1–1).

ITEM	HP PART NUMBER
500mA Fuse for 230 V operation	2110–0202
1 A Fuse for 115 V operation	2110–0007
Power Cable	See Figure 2–2
Label HP-IB address(6)	7120–6853
User's Reference (inserted in pull-out under instrument)	08170–90011
Data Output Pod 7–0	15455A
Data Output Pod 15–8	15456A
Address Pod	15453A
Control Pod	15454A
Pods are complete with:	
Carrying Case	1540–0320
Snap-on Kit	See Fig. 1–1, 1–2
The kits consist of:	
Clip connector	5040–0563
Hook-on clips (11/10)	10230–62101
and the following wires with terminations:	
Wire Black	5061–1216
Wire White/Black	5061–1217
Wire White/Brown	5061–1218
Wire White/Red	5061–1219
Wire White/Orange	5061–1220
Wire White/Yellow	5061–1221
Wire White/Green	5061–1222
Wire White/Blue	5061–1223
Wire White/Violett	5061–1224

1–20 ACCESSORIES AVAILABLE

1–21 Card Reader Model 16263A provides rapid memory loading from marked or punched cards.

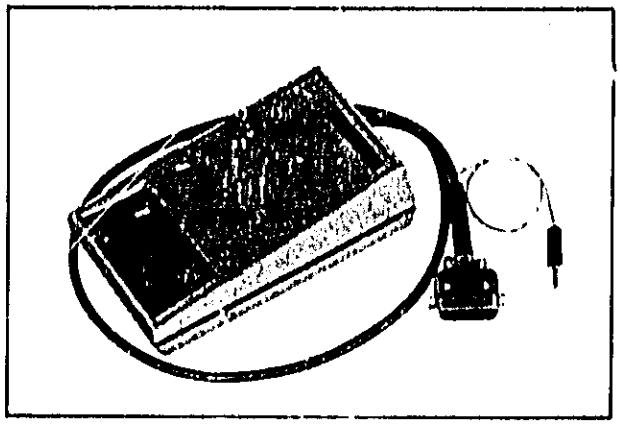


Figure 1–5. Card Reader

1–22 Pod Connector Model 15457A. This connector assembly is for permanent installation in a system. The 8170A's pods are then simply plugged in as occasion demands.

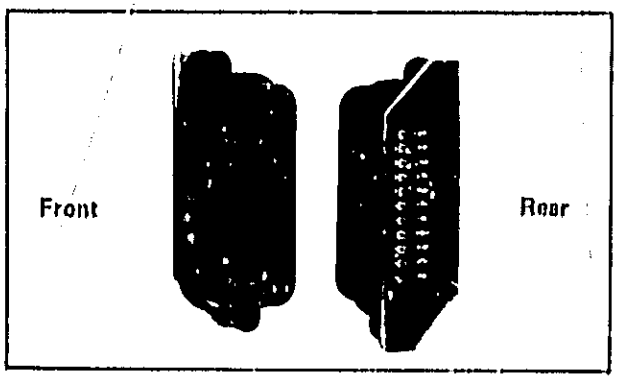


Figure 1–6. Pod Connector

1–23 Front Handle and Rack Mounting Accessories. Available as accessories or, if ordered same time as instrument, as options. Refer to Figure 1–3.

1–24 Remote Programming Connectors. Refer to Section II.

1–25 RECOMMENDED TEST EQUIPMENT

1–26 Equipment required to maintain the model 8170A is listed in Table 1–1. Other equipment can be substituted if it meets or exceeds the critical specifications listed in the table.

Table 1–1. Recommended Test Equipment

INSTRUMENT	RECOMMENDED MODEL	REQUIRED CHARACTERISTICS	USE*
Counter	HP5346A	50 μHz to 50 MHz, 8-digit display	A
Digital voltmeter	HP 3456A	0.1–20V, ac rms and dc, 0.004 % accuracy	A
Scope with probes	HP1740A	100 MHz bandwidth, 2-channel	F, A
Pulse generator	HP8012B	1 Hz – 2 MHz pulse,	F, A
Digital Signature Analyzer	HP 5004A		T
Cable assembly (3)	HP11170B	50 Ω, 61cm (24 in), BNC	F, A
Cable assembly (2)	HP11170A	50 Ω, 30cm (12 in), BNC	F,
Feedthrough termination	HP10100C	50 Ω, BNC	A
Resistor		2.5 Ω, 10 W	A
Extender board (2)	HP 5061–2160	26 pin	A, T

* F = Function Test; A = Adjustments; T = Troubleshooting

Table 1-2. Specifications

MEMORY

CAPACITY: 8192 bit.

Data bus format: 8 bit x 1024 words or 16 bit x 512 words.

POWER-OFF STORAGE: Internal battery provides memory retention for approx. 3 weeks at room temperature. Battery recharges when 8170A is switched on.

OPERATING STATES

IDLE: Permits entry of address, data and operating parameters. Data and DAV output in 3-state.

ACTIVE: Continuous data output.

BREAK: Static data output. FWD/BACK enables data change by stepping address.

ADDRESS MODES

INTERNAL: Data generation in ascending address sequence from First to Last Address. Rate governed by clock (see 'Clocking').

EXTERNAL: Data output follows external address and enable signals. DAV generated at each new address. Data and DAV in 3-state when instrument not enabled. Clock and cycle modes disabled.

Address to output delay: 550 ns max.
Enable to output delay: 100 ns typ., 130 ns max. DAV at min. delay.

CLOCKING

INTERNAL: 20 Hz to 2 MHz in 5 decade ranges, adjustable by vernier.

Rate jitter: < 0.2%.

EXTERNAL: dc to 2 MHz. For input specs, see 'Auxiliary Inputs'.

MANUAL: Operated by FWD and BACK key.

HANDSHAKE: 2-wire/3-wire handshake capability selectable. Ext handshake signals determine timing of data readout. If MAN and Handshake selected, FWD/BACK provides trigger for next handshake cycle.

CYCLE MODES

AUTO CYCLE: Data is continuously generated between first address (F-ADDR) and last address (L-ADDR).

SINGLE CYCLE: Data is generated once between F- and L-ADDR. After cycle completion, 8170A returns to IDLE state.

OUTPUT SIGNALS

DATA: Pods provide 16 output lines D0 to D7 (Model 15455A), and D8 to D15 (Model 15456A). Pos /neg true selectable on rear panel.

CONTROL: Data valid (DAV) generated with each word. Pos /neg true selectable on rear panel. DAV line via Control Pod Model 15454A.

DAV delay: (adjustable on rear panel).
Non-handshake: 100 ns to 700 ns.
2- or 3-wire handshake: 300 ns to 800 ns.
DAV width (at +1.3 V): See following table:

Clock Mode	DAV Width:
Int. Clock	Clock period/2 ± 50 ns
Man. Clock	10 μs (typical)
Ext. Clock:	
Width 40 ns - 200 ns	250 ns (typical)
Width > 200 ns	Ext width ± 50 ns

STATUS: Idle, Active and Break states indicated on lines ACS and BRS -- fed via Control Pod Model 15454A:

Status	ACS	BRS
Idle	LO	HI
Active	HI	HI
Break	LO	LO

POD OUTPUT CHARACTERISTICS

TTL setting
Fan out: 5 standard TTL max.
Levels: high +4.5 V to +5 V; low −0.5 V to +0.4 V.
Signal characteristics (1 standard TTL load):
Transition times (+0.4 V to +2.4V): 25 ns typ, 50 ns max.
Distorted high level: ≥ +3.5 V (i.e. preshoot, overshoot, ringing lie above this level).
Distorted low level: ≤ + 0.8 V (i.e. preshoot, overshoot, ringing lie below this level).

Variable setting (CMOS)
Maximum load: 50 pF (high impedance).
Levels: high +3 V to +15 V adj , low −0.5 V to +0.4 V.
High level to measurement pin voltage tracking: ± 0.2 V typ , ± 0.5 V max.
Signal characteristics (50 pF, +15 V):

Table 1–2. Specifications

Transition times (20% to 80%): 35 ns typ., 60 ns max.
Distorted low level: ⩽ + 2.5 V
Distorted high level: ⩾ +12.0 V.

Output protection: all outputs protected against short circuit and ext. voltages from −1.0 V to +18 V.

AUXILIARY OUTPUTS

TRIGGER: Generated at trigger address (T-ADDR).

Format: NRZ.
Level: standard TTL.
Fan out: 5 standard TTL max.

PROBE: +5 V dc, 400 mA max.

POD INPUT SIGNALS

ADDRESS: 12 lines (positive true), A0 to A9 via Address Pod Model 15453A; A10, A11 (for Option 001 Extended Memory) via Control Pod Model 15454A. Additional enable lines (EN1, EN2 via Control Pod; EN3, EN4 via rear panel) allow a number of 8170A's to be addressed from a 16-bit bus; selectable levels pos/neg/don't care.

CONTROL (Model 15454A): Ready for Data (RFD) and Data Accepted (DAC). In 2-wire handshake, RFD level pos/neg selectable. In 3-wire handshake, RFD and DAC conform to IEEE 488-1975.

POD INPUT CHARACTERISTICS

Input Impedance: > 10 kΩ parallel ⩽ 25 pF.
Levels: high ⩾ +2.0 V; low ⩽ +0.8 V.
Max. External Voltage: ± 18 V.

AUXILIARY INPUTS

CLOCK IN: For external clock signal input.

START IN: External signal starts data generation. Prompts 8170A transition from Idle/Break to Active state.

STOP IN: External signal stops data generation. Prompts 8170A transition from Active/Break state to Idle state.

BREAK IN: External signal halts 8170A at current address, outputs remain active. Prompts 8170A transition from Active to Break state.

INPUT CHARACTERISTICS (all positive edge triggered)

Input Impedance: > 10 kΩ parallel ⩽ 25 pF.
Levels: high ⩾ +2.0 V, low ⩽ +0.8 V.
Min. Width (at +1.3 V): 40 ns.
Max. external voltage: ± 18 V.

HP-IB CAPABILITY

Following interface functions implemented: SH1, AH1, L4, SR1, RL1, T5, PP0, DC0, DT0, C0.

KEYBOARD MODE: Remote programming of all front panel keys and functions. Coded loading and readout of data.

DATA MODE: Fast binary loading and readout of data only.

RS 232C/CCITT V24 CAPABILITY

Remote programming and listing of memory content, and display of current data bus format and address/data coding. ASCII 7, parity even.

BAUD RATE: 110, 150, 300, 600, 1200, 2400, 4800, 9600 selectable. Automatic generation of 2 stop-bits for 110 baud, one stop-bit for others.

GENERAL

POWER: 100, 120, 220 or 240 V, +5% −10%; 48 – 66 Hz, 110 VA max.

ENVIRONMENTAL: 0 to 55°C, with rel humidity to 95% at 40°C.

WEIGHT: net 11 kg (24.3 lbs), shipping 15 kg (33.2 lbs).

DIMENSIONS: 133 mm high x 426 mm wide x 422 mm deep (5.2 x 16.8 x 16.6 in.).

ACCESSORIES SUPPLIED

2 data output pods (Models 15455A, 15456A)

1 address input pod (Model 15453A)

1 control pod (Model 15454A)

Pods complete with Snap-on Assembly, wires, hook-on clips and carrying case.

2-m power cord, Operating and Service Manual.

OPTIONS

001 ADDITIONAL 24 K BIT MEMORY
for output format 8 bit x 4096 words, or 16 bit x 2048 words

Continued.

Table 1–2, Specifications

002 ADDRESS DRIVER (MODEL 15452A)

Provides 10 address output lines A0 to A9, positive true, 3-state capability in idle state.
Fan out: 10 standard TTL max.
Levels: high ≥ +2.4 V, low ≤ +0.5 V.
Signal characteristics (into 1 standard TTL):
Transition times (+0.5 V to +2.4 V): ≤ 50 ns.
Distorted high level: ≥ +2.4 V.
Distorted low level: ≤ +0.8 V.

907 Front Handle Kit (Part No 5061-0089)
908 Rack Flange Kit (Part No. 5061-0077)
909 Rack Flange and Front Handle Combination Kit (Part No. 5061-0083)
910 Additional Operating and Service Manual

SECTION II
INSTALLATION

2–1 INTRODUCTION

2–2 This section provides installation instructions for the instrument and its accessories. It also includes information about initial inspection and damage claims, preparation for use, and packaging, storage and shipment.

2–3 INITIAL INSPECTION

2–4 Inspect the shipping container for damage. If the container or cushioning material is damaged, it should be kept until the contents of the shipment have been checked for completeness and the instrument has been checked mechanically and electrically. The contents of the shipment should be as shown in Figure 1–1 plus any accessories that were ordered with the instrument. Procedures for checking the electrical operation are given in Section IV. If the contents are incomplete, if there is mechanical damage or defect, or if the instrument does not pass the operator's check, notify the nearest Hewlett-Packard office. Keep the shipping materials for carrier's inspection. The HP office will arrange for repair or replacement without waiting for settlement.

2–5 PREPARATION FOR USE

2–6 Power Requirements

2–7 The instrument requires a power source of 100V, 120V, 220V or 240V (+5%, –10%) at a frequency of 48 to 66 Hz single phase. The maximum power consumption is 110 VA.

2–8 Line Voltage Selection

CAUTION

BEFORE SWITCHING ON THIS INSTRUMENT OR CONNECTING TO THE SUPPLY, make sure that the instrument is set to the local line voltage.

2–9 Figure 2–1 provides information for line voltage and fuse selection:

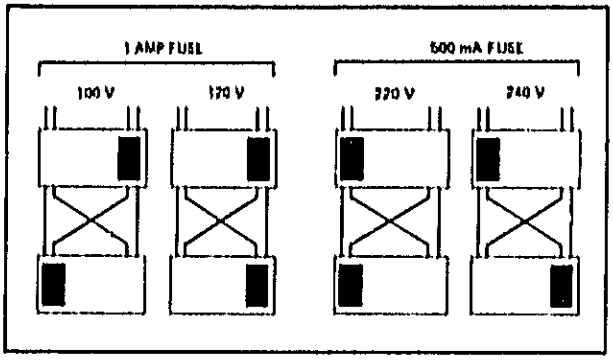


Figure 2–1. Switch Settings for the various Nominal Powerline Voltages

2–10 Power Cable

WARNING

To avoid the possibility of injury or death, the following precautions must be followed before the instrument is switched on:

a. If this instrument is to be energized via an autotransformer for voltage reduction, make sure that the common terminal is connected to the neutral pole of the power source (non-symmetrical supplies). Ensure that the ground connection is preserved.
b. The power cable plug shall only be inserted into a socket outlet provided with a protective ground contact. The protective action must not be negated by the use of an extension cord without a protective conductor.

c. Before switching on the instrument, the protective ground terminal of the instrument must be connected to a protective conductor of the power cable. This is verified by checking that the resistance between the instrument chassis and the front panel and the ground pin of the power cable plug is zero ohms.

2–11 In accordance with international safety standards, this instrument is equipped with a three-wire power cable. When connected to an appropriate ac power receptacle, this cable grounds the instrument cabinet. The type

of power cable shipped with each instrument depends on the country of destination. Refer to Figure 2–2 for the part number of the power cords available.

2–12 If the plug on the cable supplied does not fit your power outlet, then cut the cable at the plug end and connect a suitable plug. The plug should meet local safety requirements and include the following features:

Minimum current rating of 2A
Ground connection
Cable clamp.

The colour coding used in the cable will depend on the cable supplied (see Figure 2–2).

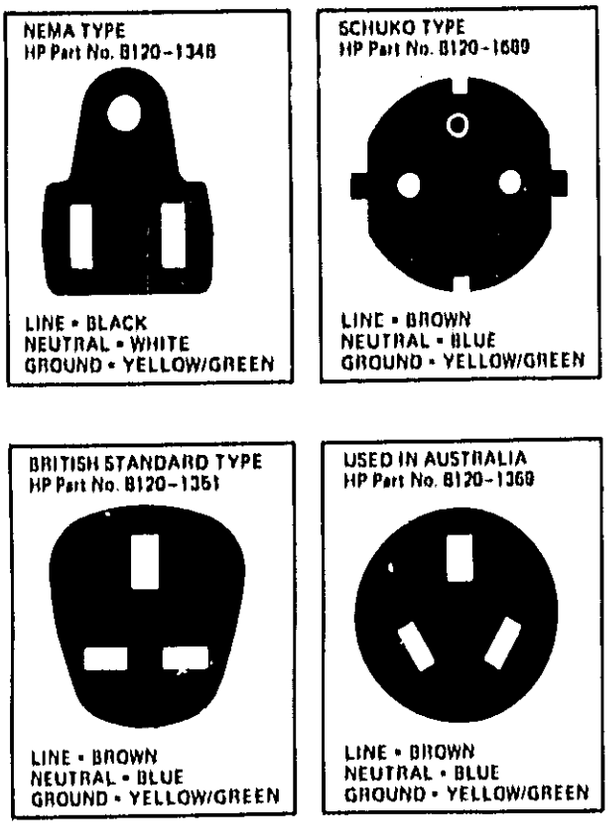


Figure 2–2. Power Cables Available: Plug Identification

2–13 HP-IB Connector

2–14 The rear panel HP-IB connector (Figure 2–3) is compatible with the connectors on Cable Assemblies 10631A, B, C and D. If a cable is to be locally-manufactured, use connector male, HP Part Number 1251–0293.

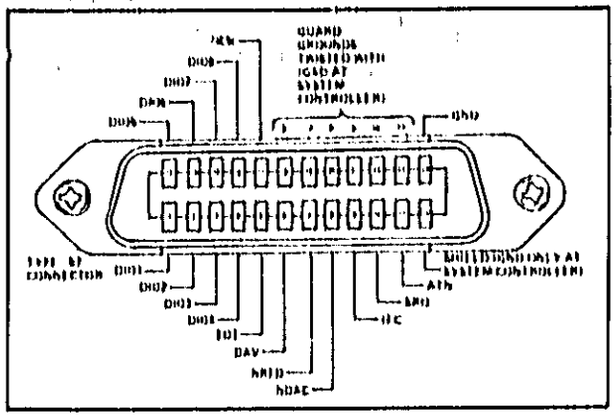


Figure 2–3. HP-IB Connector

2–15 HP-IB Logic Levels

2–16 The 8170A HP-IB lines use standard TTL logic. Logic levels are as follows:

True = low = digital ground or 0 V dc to +0.4 V dc,
False = high = open or +2.5 V dc to +5 V dc.

All HP-IB lines have LOW assertion ("1") states. High states are held at +3 V dc by pullups within the instrument. When a line functions as an input, approximately 3.2 mA of current is required to pull it low through a closure to digital ground. When a line functions as an output, it will sink up to 48 mA in the low state and approximately 0.6 mA in the high state.

CAUTION

Isolation. The HP-IB line screens are not isolated from outer chassis (frame) ground.

2–17 RS 232C Connector

2–18 Connections used in the 8170A are shown in Figure 2–4. If the RS 232C device to which the 8170A is to be connected does not have a free-end cable, use Cable Assembly, HP part number 07221–60157.

Note: The 8170A is wired as a DCE (Data Communication Equipment, EIA Std RS 232C/CCITT V.24.

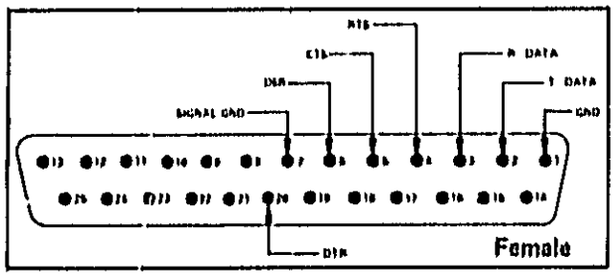


Figure 2–4. RS 232C Connector

2–19 RS 232C Logic Levels

From 8170A	True	False
DSR	+12 V	−12 V
RDATA	−12 V	+12 V
CTS (= RTS)	+12 V	−12 V

To 8170A		
DTR	Open	< −3 V
TDATA	Open	> +3 V
RTS	Open	< −3 V

2–20 Operating Environment

2–21 The instrument will operate within specifications when the ambient temperature is between 0°C and 55°C.

2–22 FRONT HANDLE/RACK MOUNTING

2–23 Figure 1–2 shows the possible handle/rack mounting configurations. If handles are fitted and subsequently need to be removed, the plastic trim must first be taken off as shown in Figure 2–5.

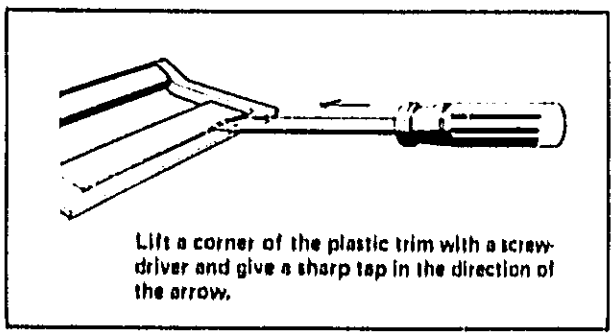


Figure 2–5. Removing Plastic Trim

2–24 CLAIMS AND REPACKAGING

2–25 Claims for Damage

2–26 If physical damage is evident or if the instrument does not meet specification when received, notify the carrier and the nearest Hewlett-Packard Sales /Service Office. The Sales/Service Office will arrange for repair or replacement of the unit without waiting for settlement of the claim against the carrier.

2–27 Storage and shipment

2–28 The instrument can be stored or shipped at temperatures between −20°C and 70°C. The instrument should be protected from temperature extremes which cause condensation within the instrument.

2–29 If the instrument is to be shipped to a Hewlett-Packard Sales/Service Office, attach a tag showing owner, return address, model number and full serial number and the type of service required. The original shipping carton and packaging material may be re-usable but the Hewlett-Packard Sales/Service Office will also provide information and recommendations on materials to be used if the original packing is not available or reusable. General instructions for re-packing are as follows:

1. Wrap instrument in heavy paper or plastic.

2. Use strong shipping container. A double wall carton made of 350-pound test material is adequate.

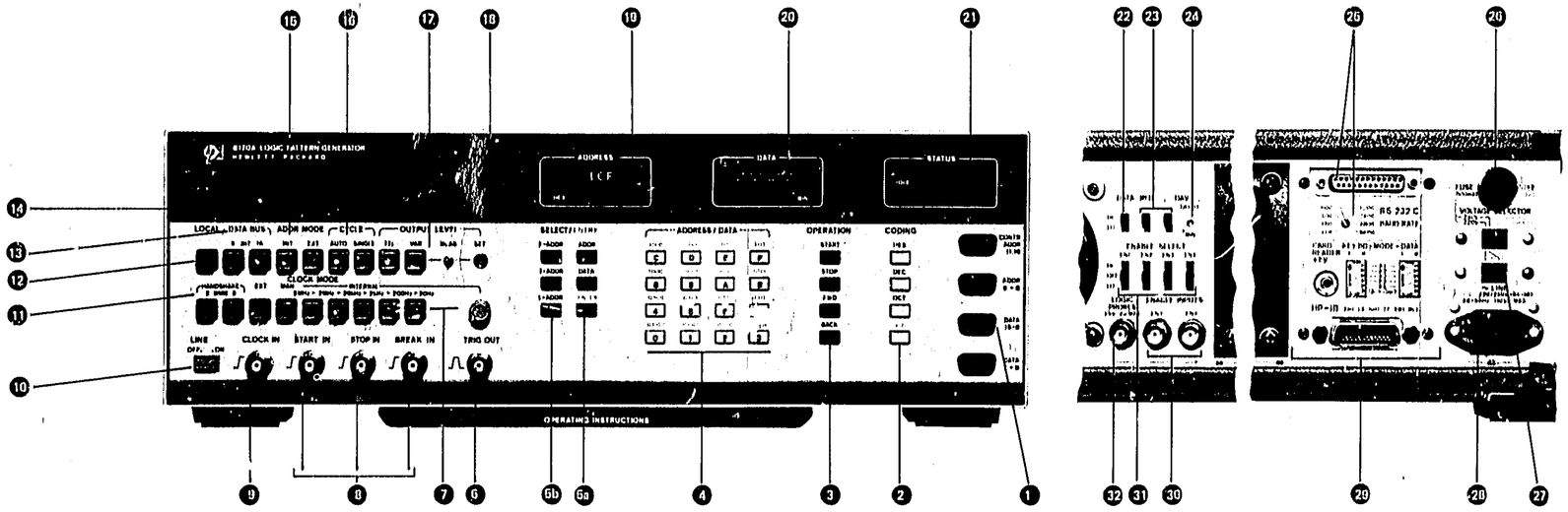
3. Use enough shock-absorbing material (3 to 4-inch layer) around all sides of instrument to provide firm cushion and prevent movement inside the container. Protect control panel with cardboard.

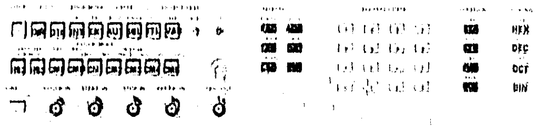
4. Seal shipping container securely.

5. Mark shipping container FRAGILE to encourage careful handling.

6. In any correspondence, refer to instrument by model number and serial number.

OPERATION AND PROGRAMMING





HP-IB Codes

1 Connectors for Pod Assemblies. From top to bottom: **Control Pod**, carrying: DAV, RFD, DAC, ACS, BRS, EN1, EN2, and address lines A10, A11.
Address (Input) Pod or Option Address Driver (Output) Pod, carrying address lines A0 – A9.
Data Pod 15–8, carrying MS Byte D8 – D15 in 16-bit bus mode. Lines in 3-state in 8-bit bus mode (except 3-wire handshake) and Idle State (§ 3–35).
Data Pod 0–7, carrying data lines D0 to D7. Lines in 3-state in Idle State.

2 Selectors for the codes used in entry/display of address and data. Addresses may be entered in octal, decimal or hexadecimal. Data in binary, octal or hexadecimal. These codes do not affect the data output.

3 Manual implementation of the 'Active State' (See § 3–35) by the START key, and of the 'Idle State' by the STOP key. FWD and BACK keys step the address when the 8170A is: in the 'Active State' with Man Clock mode, in the 'Break State'.
Keeping the FWD or BACK key depressed causes rapid address and data stepping.

4 Value keys for data and address. When entering in binary (data only) use the binary notation on the panel.
For other codes, use the notation on the keys themselves, as follows: octal: keys 0 – 7
decimal (address only): keys 0 – 9
hexadecimal: keys 0 – F
Commence value entry with the most significant digit/byte.

6a Address selection and data recall/entry. These keys are for:
a) defining the address and data codes for entry/display,
b) defining the address at which data recall/entry shall commence.
Syntax for code definition, e.g.:
<ADDR> <DEC> <DATA> <HEX>
(< > = press key)
The displays 19 20 will show DEC, HEX respectively. Address can be coded in OCT, DEC, HEX; data in BIN, OCT, HEX.
Syntax for data recall, e.g.:
<ADDR> <38> <DATA> Displays **19** **20** then show address and data as well as the respective codes. Data at the previous address, or next address, can then be accessed by
< BACK > or < FWD > . Keeping the key depressed causes rapid address and data stepping.
Syntax for changing data , e.g..
<ADDR> <12 > <DATA > < 2 ><A >
< ENTER >
The display changes to the new data when (in this example) the keys 2 and A are pressed. If leading digit is zero this need not be pressed. When ENTER key is pressed, new data overwrites old data and the 8170A automatically goes to the next address. Multiple data entries can be made by keeping the ENTER button depressed.

6b Special addresses
F–ADDR (first address): the address at which data generation is to start.
L–ADDR (last address): the address at which data generation is to end.
T–ADDR (trigger address): the address at which a trigger pulse (TRIG OUT **6**) is generated.
By pressing, for example, F–ADDR, the display **19** shows the current first address. This may be changed by entering the desired address value. The following example selects the trigger address, defines hexadecimal code and defines a T–ADDR value of A4:
<T–ADDR> <HEX> <A > <4> <ENTER>
A typical sequence for setting F–ADDR and entering data from that address on, would be:
<F–ADDR><DEC><2><5 ><ENTER>
<DATA> < HEX> <1> <2 > <ENTER>
<A > <3 > < ENTER > <E> <8 > < ENTER> ...
(< DEC> , < HEX> may be omitted if desired codes are already selected).

6 Trigger output. See **6b** T-ADDR.

7 Int/ext/man clock mode selector buttons. Vernier provides continuous adjustment within internal ranges.

8 Input signals for the implementation of Active, Idle and Break states (see § 3–34).

9 Input for external clock mode.

10 Line on/off.

11 Selectors for 2- or 3-wire handshake. Int and ext clock modes are inhibited.

12 Re-instates front panel control unless LLO (local lock out) has been programmed.

13 Selects 8/16-bit output data. Affects maximum address and maximum data values as follows:

HIGHEST ADDRESS			
8170A	OCT	DEC	HEX
8-bit	1777	1023	3FF
16-bit	777	511	1FF
8170A Option 001			
8-bit	7777	4095	FFF
16-bit	3777	2047	7FF

MAX DATA VALUE		
BIN	OCT	HEX
8 bits set to 1	377	FF
16 bits set to 1	177777	FFFF

14 Remote Control status indicators: remote, talk, listen, SRQ (service request – see § 3–72).

15 Selection of internal address mode means that the 8170A generates addresses in an ascending order at a rate (data rate) determined by int/ext clock or 2-/3-wire handshake.
Selection of external address causes the 8170A to operate like a PROM; the 8170A outputs the content of locations addressed from an external source. Clock and handshake inhibited. External address lines A9–A0 are fed via the Address Input Pod and lines A11, 10 (required for the Option 001 Extended Memory) are fed via the Control Pod. Note that, the Control Pod must always be connected to the 8170A for correct operation in the external address mode.

16 Data may be cycled continuously or just once from F–ADDR to L–ADDR (see § 3–48).

17 With the exception of TRIG OUT and Option 002 Address Driver Pod outputs (which are always TTL-compatible) all outputs can be selected TTL-compatible or variable high level from +3 V to +15 V. This adjustment can be made by attaching a DVM to the testpoint MEAS and adjusting the screwdriver slot SET.

18 'ERROR' is indicated if syntax or value errors are made.

19 Address display – indicates value and code.

20 Data display – indicates value and code. In binary (as in picture), bit high represents true, bit low represents false.

24 Status display – Idle, Active, Break (§ 3–35).

22 Selects data pod outputs as low true or high true. Logic change first effective on following clock pulse or address change.

23 Sets RFD and DAV lines low true or high true. In 3-wire handshake, convention is IEEE 488 (not selectable).

24 Adjustable DAV delay. Factory setting is minimum. See Figure 3–8, 3–10.

25 Connector and baud-rate selector for RS 232C instruments.

26 Fuse.

27 Input Voltage Selector.

28 Line receptacle.

29 HP-IB connector, address selectors and 5 V supply for Card Reader 16263A.

30 Enable Lines 3 and 4. With Control Pod's enable lines 1 and 2, 16-line addressing of several 8170A's is feasible.

31 True high/low and off selectors for the enable lines.

32 Logic probe supply.

Figure 3–1. Controls, Connectors and Indicators

SECTION III
OPERATION AND PROGRAMMING

3–1 INTRODUCTION

3–2 This section explains the functions of control, connectors and indicators, and provides operating and programming information. The Extended Memory Option 001 and Address Driver Pod Option 002 are included.

3–3 SPECIAL OPERATING CONSIDERATIONS

3–4 The following steps must be taken before applying power to the Model 8170A:

a) Read the safety summary at the front of this manual.

b) Be sure the power selector switches are set properly for the power source being used to avoid instrument damage (Section II).

CAUTION

Do not change the LINE SELECTOR Switch setting with the instrument on or with power connected to the rear panel.

3–5 OPERATOR'S CHECKS

3–6 Verify that all displays light briefly on switching on. The displays, special addresses and controls will then revert to the condition prevalent at switch-off. Exception: 8170A automatically adopts Idle State (§ 3–35).

Note. Operating modes, parameters and data are retained in a CMOS memory with battery back-up. If the batteries are allowed to run down, the information must be re-entered. If the instrument has not been used for several weeks, leave it switched on so that the batteries can recharge. A full charge requires 16 hours.

3–7 Use the performance checks in Section IV to fully verify operation.

3–8 CONTROLS, CONNECTORS AND INDICATORS

3–9 Refer to Figure 3–1.

3–10 OPERATING INSTRUCTIONS

3–11 General

3–12 The 8170A generates 1024 words (8 BIT DATA BUS selected) or 512 words (16 BIT DATA BUS selected). Option 001 Extended Memory increases the RAM depth to 4096 or 2048 words respectively. The memory is non-volatile (battery back-up), and is programmable from the front panel or remotely.

3–13 An ascending-address generator accesses the RAM and hence determines the data output. The address generator operates between first and last addresses (F-ADDR and L-ADDR), which are determined by the operator. A trigger address (T-ADDR) allows a trigger pulse to be generated when this address is reached. Data can be continuous- or single-cycled between F- and L-ADDR.

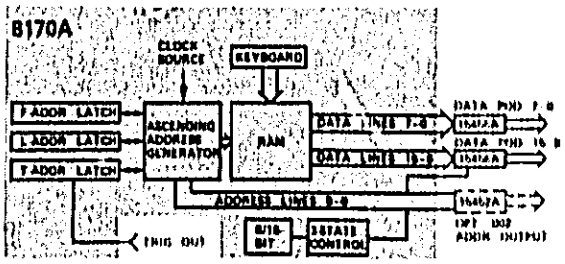


Figure 3–2. Block Diagram: Internal Address Mode Configuration

3–14 Data outputs are fed via active line driver pods. These are supplied accessories which provide easy connection to a device-under-test.
Option 002 provides a line driver pod for the address lines.

3–15 Bit rate can be determined by internal or external clock, manually or by a 2- or 3-wire handshake (Figure 3–3).

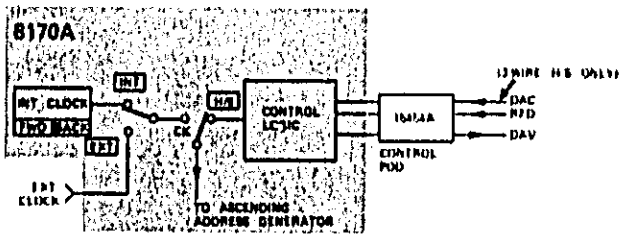


Figure 3–3. Block Diagram: Synch/Asynch Bit Rate Generation (Internal Address Mode)

3–16 External addressing is feasible using the address input pod. This is an active line receiver for ten address lines. If the extended memory is used, two more address lines are available using the control pod. Four enable lines facilitate 8170A selection so that one or more 8170A's may be addressed from a 16 address line bus. Two enable lines are routed through the control pod; and two are brought out on the rear panel. The control pod must always be connected to the 8170A.

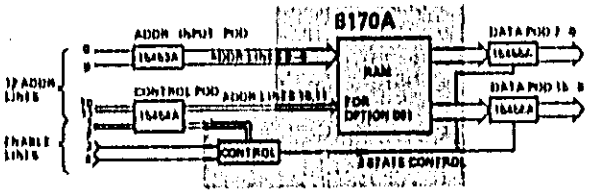


Figure 3–4. Block Diagram: External Address Mode Configuration

3–17 Addressing

3–18 Coding

3–19 Memory addresses may be entered and displayed in decimal, octal or hexadecimal codes. The desired code is selected by pressing the ADDR key (SELECT keys) and then the desired HEX, DEC or OCT key (CODING keys) e.g.:

<ADDR> <DEC>

The selected code will then appear in the display's ADDRESS field. BIN code is not admissible and will cause an ERROR display if selection is attempted. The address code may also be selected by using either F-, T-, or L-ADDR keys, e.g.:

<F–ADDR> <OCT>

The selected address code remains effective until redefined. Consequently, there is no need to define code if the desired code is already active. Changing the address code merely changes the values entered and displayed. It does not change the location.

3–20 Defining First, Last and Trigger Addresses

3–21 Commence by selecting the desired 8-bit/16-bit data bus. F-, T- and L-ADDR are then defined by pressing the appropriate -ADDR key, setting up a value on the ADDRESS/DATA keys and pressing ENTER, e.g.:

<F–ADDR><2> <1> <7>
<ENTER>

Make sure the address does not exceed the value set out in Table 3–1. If a higher address is attempted, the ERROR display will light when the ENTER key is pressed. Also, L-ADDR must be higher than T-ADDR, if a trigger pulse is required.

If the address commences with zeroes, e.g. 004, these may be omitted from the entry. The 8170A automatically inserts the zeroes when ENTER is pressed. F-, T- and L-ADDR storage is non-volatile and can consequently be used and recalled even if power has been removed in the meantime. Recall into the address display is made by pressing the appropriate -ADDR key, e.g.:

<T–ADDR>

If the Bus Mode is changed from 8- to 16-bit, the existing F-, T- and L-ADDR will be retained provided that they lie within the address limits of Table 3–1. Those outside are set to zero (F- and T-), or highest permissible address (L-). Refer also to § 3–33.

Table 3–1. Address Limits

Highest Address:

	8170A		8170A Opt. 001	
	16 BIT	8 BIT	16 BIT	8 BIT
HEX	1FF	3FF	7FF	FFF
DEC	511	1023	2047	4095
OCT	777	1777	3777	7777

Lowest Address: Zero

3–22 Data Storing

3–23 Coding

3–24 Data may be entered in binary, octal and hexadecimal codes. The desired code is selected by pressing the DATA key and then the desired BIN, OCT or HEX key, e.g.:

<DATA> <HEX>

The selected code will then appear in the display's DATA field. DEC code is not admissible and will cause an ERROR display if selection is attempted. Note that, if neither address nor data fields are selected, the coding keys are operative on the data display. Thus, pressing a code key then causes the data code indicator to change. The value displays remain blank.

The selected data code remains effective until redefined, consequently there is no need to enter a code if the desired code is already active.

Changing the data code merely changes the values entered and displayed. It does not change the location contents.

3–25 Loading

3–26 Commence by selecting the required 8-bit/16-bit data bus. Loading data into a specified memory location is then achieved by calling an address (press ADDR, set-up desired address value), pressing the DATA key, setting up the desired data in the selected code, and pressing the ENTER key e.g.:

< ADDR > <2> < 0 > < 0 >

< DATA> < 2> < E > <ENTER >

After pressing ENTER, the 8170A moves automatically to the next address. Data is loaded into this new address simply by setting up a value and pressing ENTER e.g.:

<F > <1 > <ENTER >
<6 > <8> <ENTER >

and so on. Holding the ENTER key down causes multiple entry of value last entered or fetched.

3–27 Loading Binary. When loading binary, the desired bit pattern is entered e.g. (for 8-bit word length):

< DATA ><0 > <1> < 0> <0> < 0 >
BIT D7
<0 > <1> <1 > < ENTER >
BIT D0

In this example, the initial digit is zero. This need not be written by the operator. The 8170A will automatically insert leading zeroes when ENTER is pressed.

3–28 Loading Octal. When loading octal, the desired bit pattern must be converted, e.g.:

8-bit pattern 1 1 1 0 1 0 1 0
BIT D7
Octal equivalent 3 5 2

Note, first octal character may not exceed 3. If first significant digit exceeds this value, leading zeroes must be entered.

Keystroke sequence

<DATA><3> <5> <2> <ENTER >

16-Bit pattern

1 0 1 1 1 0 1 1 0 0 1 0 1 1 1 0
BIT D15

Octal equivalent

1 3 5 4 5 6

Note, first octal character may not exceed 1. If first significant digit exceeds this value, leading zeroes must be entered.

Keystroke sequence

<DATA><1> <3> <5>
<4> <5> <6 > < ENTER >

3–29 Loading Hexadecimal. Examples for binary/hexadecimal conversion:

8-Bit pattern 1 1 1 0 1 0 1 0
BIT D7

Hexadecimal equivalent E A

Keystroke sequence

<DATA> <E> < A> <ENTER >

16-Bit pattern

1 0 1 1 1 0 1 1 0 0 1 0 1 1 1 0
BIT D15

Hexadecimal equivalent

B B 2 E

Keystroke sequence

< DATA > <B> <B> <2> <E> <ENTER >

3–30 Fixed Data Pattern Entry. Fixed data patterns may be loaded into memory using a special keystroke

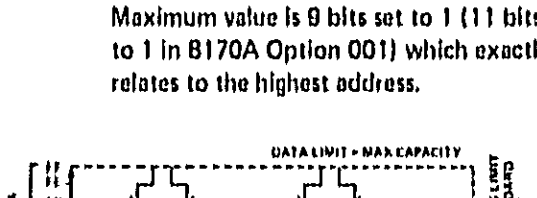
procedure. The data patterns available and their associated keys are:

0	Memory reset (all zeroes),
1	Memory set (all ones),
E	Pseudo random pattern,
C	Sequence C
D	Sequence D

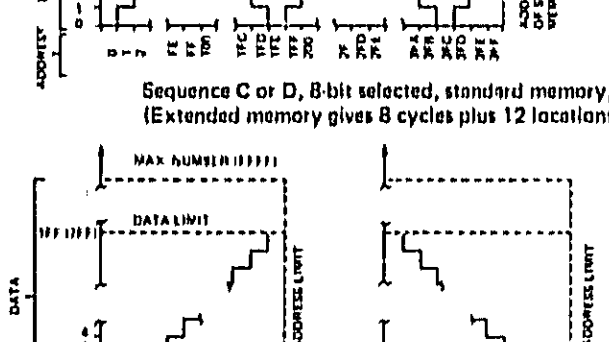
Sequences C and D increment and decrement data as follows:

If 8-BIT DATA BUS is selected, C and D sequences generate an identical pattern. This starts at zero and increments by 1 per memory location until all 8 bits are true (FF in HEX), and then decrements to zero in the same way. This cycle repeats until the whole memory is loaded (2 cycles with 8170A, 8 cycles for 8170A Option 001). Up or down sequences can be accessed by appropriate definition of F-ADDR and L-ADDR, e.g., 0 and FF respectively for up, FF and 1FE respectively for down.

If 16-BIT DATA BUS is selected, Sequence C generates a progression, Sequence D a regression. Maximum value is 9 bits set to 1 (11 bits set to 1 in 8170A Option 001) which exactly relates to the highest address.



Sequence C or D, 8-bit selected, standard memory, (Extended memory gives 8 cycles plus 12 locations).



Sequence C, 16-bit selected, standard memory (extended memory in brackets).

Sequence D, 16-bit selected, standard memory (extended memory in brackets).

Figure 3–5. Data Patterns C and D

To load a fixed data pattern, press the DATA key, keep held down, and press the pattern selector key for 2 seconds. The data display will show:

Mem Chg ?

If memory change is not required (e.g., inadvertent selection), press the 0 key (or any other value key except 1). These keys (except 0) operate in the normal way, including ERROR indication. The display then reverts for normal operation. If memory change is required, press the 1 key. Data display changes to

Mem Chg !

When loading is complete, the exclamation mark is replaced by the pattern identifier. As an example, the pseudo random pattern is entered as follows:

< DATA / E > [(DATA first, then simultaneously for 2 s)
Mem Chg ?
< 1 >
Mem Chg !
Mem Chg E

The next keystroke causes the display to revert to it's normal function.

3–31 Recall

3–32 The contents of a specific address can be displayed by a keystroke sequence similar to the following example:

<ADDR> <4> <5> <DATA>

The contents of the next (or previous) address can then be displayed by pressing the FWD (or BACK) key. Holding the FWD (or BACK) key down causes consecutive recall.

3–33 Data Bus (8 bit/16 bit) Change

3–34 This paragraph only applies if, contrary to the procedures already described, it is desired to change the 8-bit/16-bit bus selection without reprogramming the memory.
If the bus selection is changed from 8-bit to 16-bit, address 512 (of the 8-bit word) becomes the MS Byte of address 0 (of the 16-bit word), address 513 becomes MS Byte of address 1 and so-on up to address 1023 which becomes the MS Byte of address 511.
In the 8170A Option, each 1 k segment of memory behaves the same way. The effect is shown in Figure 3–6.

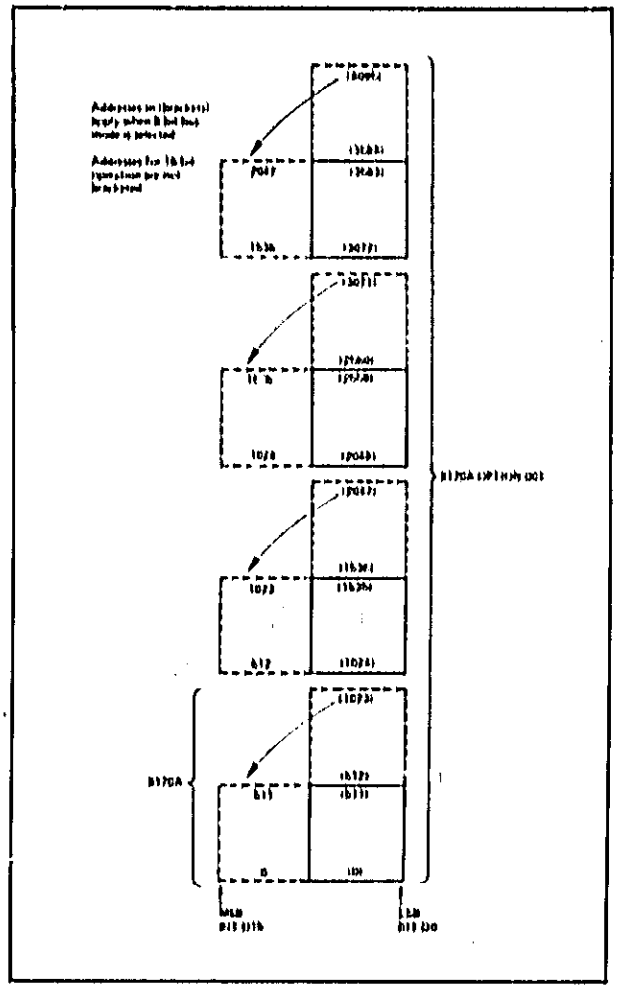


Figure 3–6. Memory Organization

3–35 Operating States

3–36 The B170A resides in one of three states:

idle – outputs inactive (high-impedance 3-state)

active – outputs active

break – outputs active (static).

State transitions are initiated by control signals applied at the front panel or by the B170A's keyboard. Current status is indicated by status signals (via the control pod) and front panel indicators.

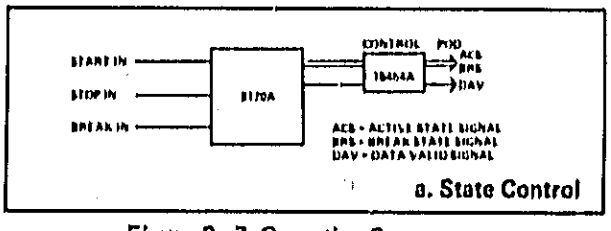
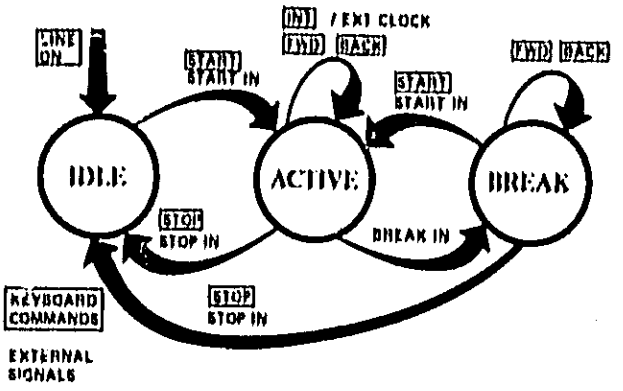


Figure 3–7. Operating States



b. State Diagram

Figure 3–7. Operating States (cont'd)

3–37 Idle State

3–38 Idle state is entered after:

power on,

manual STOP,

STOP IN signal,

at the end of a SINGLE CYCLE.

The operator can set operating modes and load, fetch and change address and data. All front panel controls and keys are operative. No output signals (except ACS low and BRS high) are generated. DAV and all data lines are high impedance (3-state). The B170A will only respond to an external or manual start signal.

3–39 Active State

3–40 Active state can be entered from Idle or Break States by an external or manual start signal. The B170A responds to all external signals according to the selected mode of operation. With the exception of LOCAL, STOP and (in manual clock mode) FWD and BACK, all front panel keys are disabled. All outputs are active. ACS is high, BRS high.

3–41 Break State

3–42 Break state can only be entered from Active State with the BREAK IN signal. With the exception of LOCAL, STOP, START and (independent of clock mode setting) FWD and BACK, all front panel keys are disabled. Data Outputs are active, but are static at the address which was effective at the incidence of the BREAK IN signal. By using the FWD or BACK keys, data can be stepped at manual rates. Feeding TRIG OUT to BREAK IN activates the Break

state when the T-DDR is reached. ACS and BRS are low. The 8170A will respond to external or manual start and stop signals.

3–43 Signal Levels

3–44 Input Signals

3–45 All input signals are TTL-compatible. Enable lines can be selected positive true, negative true or off (rear panel). RFD can be selected positive true or negative true for 2-wire handshake; for 3-wire handshake it is always in accordance with IEEE 488 (high level = ready for data). All other inputs are effective on the positive-going edge.

3–46 Output Signals

3–47 TRIG OUT and Option 002 Address Driver Pod outputs are TTL-compatible positive pulse. All other outputs are TTL-compatible (TTL selected or CMOS-compatible (VAR selected). When VAR is selected, high level is adjustable from +3 V to +15 V (test point MEAS and screwdriver trimmer SET). Data outputs and DAV are positive/negative true selectable (rear panel) and have 3-state capability. For 3-wire handshake, DAV is always in accordance with IEEE 488 (low level = data valid). Trigger and data outputs are NRZ.

3–48 Operating Modes

3–49 Internal Address Mode

3–50 Clock Mode. Data rate can be determined by the internal 20 Hz to 2 MHz clock, external CLOCK IN signal or manually (MAN button lit, press FWD/BACK keys). At slow clock rates, addresses and data are displayed. When AUTO CYCLE is selected, data between F-ADDR and L-ADDR will be continuously recycled so long as the active state prevails. In SINGLE CYCLE, the 8170A automatically returns to the idle state when L-ADDR is reached. A timing diagram appears in Figure 3–8. Note that, in break state with external clock selected, the data may be stepped manually with the FWD or BACK key.

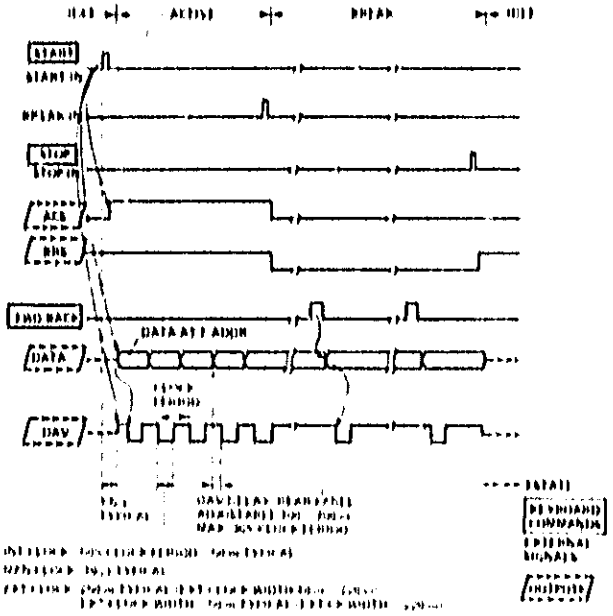


Figure 3–8. Clock Mode Timing

Note that, when changing from ext clock to int clock, AUTO CYCLE is automatically selected.

3–51 Handshake Modes. In the active state, timing is determined by the handshake lines DAV, RFD and (3-wire handshake only) DAC. When 2- or 3-wire handshake is selected, the internal and external (but not manual) clock modes are disabled. Auto or single cycle may be selected. A rear panel DAV delay adjustment is provided for handshake timing investigation. In the event of apparent handshake malfunction, verify that this control is set to minimum (factory setting), and that the RFD and DAV are set to the appropriate logic convention (in 3-wire handshake the convention is fixed: IEEE 488).
In 3-wire handshake, data bits 8 -15 are active even of 8-bit bus is selected. This allows the control lines of the IEEE bus Std 488 to be simulated as well as the data and handshake lines.

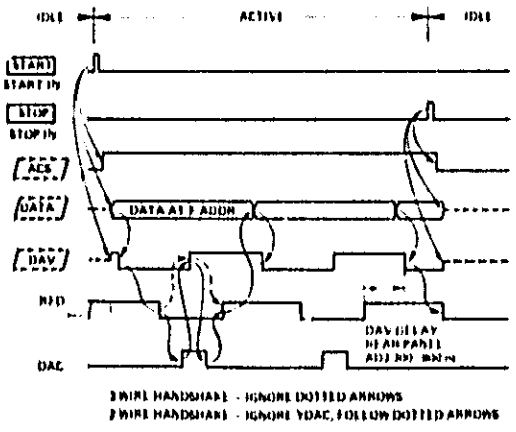


Figure 3–9. Handshake Mode Timing

3–52 Bus traffic can be slowed to manual speeds either by initiating break state or by selecting manual. Both methods operate by preventing the 8170A from stepping the address until the FWD or BACK key is pressed. Note that, should RFD be false when the key is pressed, an error condition will be indicated on the display.

3–53 Optional Address Output Capability. The addresses generated by the 8170A can be applied to an external device by means of the Address Driver Pod Model 15462A (8170A Option 002). Applied to the ADDR 9–0 connector, 10 address lines are available which provide complete addressing for the standard memory. If using the 8170A Option 001 Extended Memory, the address sequence repeats four times for a complete data read-out.

3–54 External Address Mode

3–55 When external address mode is selected, addresses applied to the 8170A via the Address Pod Model 15463A (connector ADDR 9–0) will cause the corresponding data to be accessed and output. Qualifiers EN1, EN2 (via control pod) and EN3, EN4 (via rear panel) must be true or switched off (rear panel HI/OFF/LO switches). These qualifiers allow the use of several 8170A's in parallel and permit 16-line addressing. With external address mode selected, cycle and clock modes are inhibited.

In the break state, the FWD key can be used to pull the BRS signal (can be used as system halt). When using the 8170A Option 001 Exteded Memory, the address lines (A10, A11) of the control pod are required as well.

Note that, whether or not the A 10, A 11 lines are required, the control pod must always be connected to the 8170A.

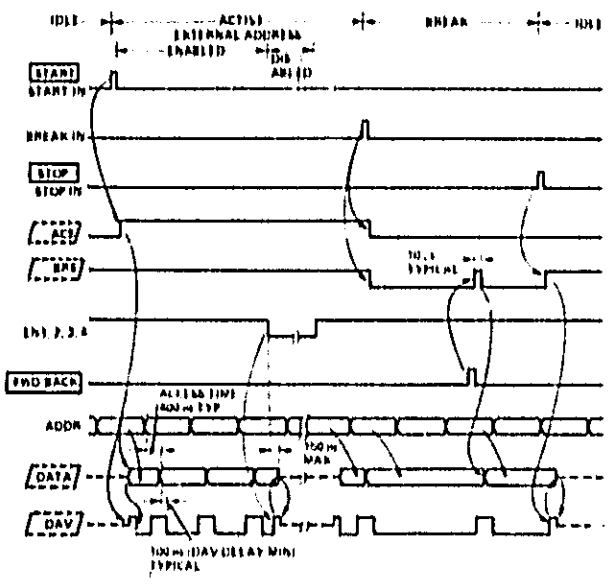


Figure 3–10. External Address Mode Timing

3–56 HP-IB PROGRAMMING INSTRUCTIONS

3–57 The following program modes can be chosen by appropriate addressing:

Keyboard Mode

Listen – all front panel keys (data, address, parameter and mode) can be programmed from the system controller.

Talk – memory content or error message can be communicated to the HP-IB.

Talk only – for memory content reporting, in the selected code, to a non-controlling peripheral (e.g. printer). No system controller required.

Data Mode

Listen – fast memory loading (in binary bytes only). No mode control.

Talk – fast memory content communication (in binary bytes only) or error message (same as keyboard mode) to the HP-IB.

Talk only – for memory content reporting, in binary, to a non-controlling, serial storing/reporting, peripheral (e.g. tape punch). No system control required.

3–58 Control Lines

3–59 The bus lines available at the rear panel HP-IB connector are as follows (all use negative logic):

8-bit data bus (lines DIO 1 to 8);

handshake lines DAV (data valid), NRFD (not read for data), NDAC (not data accepted);

control lines IFC (interface clear), ATN (attention), SRQ (service request), REN (remote enable), EIO (end or indentify).

The 8170A uses all lines except EOI. Terminations, logic levels and pinouts are described in Section II. In this manual, bus information will generally be restricted to 8170A specifics, for this reason, the handshake lines will not be discussed and the control lines will only be mentioned in connection with 8170A activity. Permissible codes are

presented in Table 3–3. For more bus information, refer to the condensed description in HP publication 59401–90030 and to IEEE Standard 488.

3–60 To use the 8170A on the bus, remote control must be implemented. This is done by setting the REN line true. A return to local control can be made manually (LOCAL button), by sending the command GTL (go to local), or by setting REN false.

3–61 Addressing the 8170A

3–62 Talk and listen addresses are transmitted by the system controller over the data bus with the ATN line true. When an instrument recognizes its address, it will adopt the appropriate bus mode. The 8170A has two sets of address selectors, one for the keyboard mode and the other for the Data Mode. They are situated on the rear panel, and their possible settings are summarized in Table 3–2. When allocating addresses, make sure all selectors in the system have a unique setting. Supplied accessory 7120–6853 peel-off HP-IB labels provide a convenient record, see Figure 3–11.

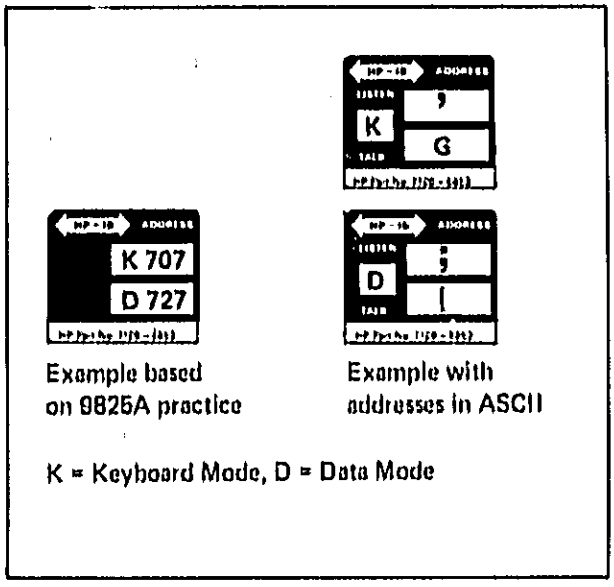


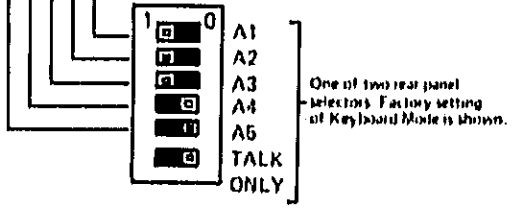
Figure 3–11. HP-IB Address Labels

3–63 For operation in Talk only, it is immaterial what setting the A1 to A5 selectors have. Important is, that the appropriate 8170A TALK ONLY selector be set to 1, and that the listener (printer, punch) be set to 'Listen Only'. Note that, first and last addresses must be defined on front panel or remotely in keyboard mode.

3–64 When the 8170A is addressed, REMOTE LISTEN or TALK or REMOTE TALK will appear in the display (REMOTE TALK appears if the 8170A was previously listen addressed). Front panel operations are protected against interruption from the HP-IB. Thus, if a manually-invoked operation is in progress, the 8170A will not respond to the talk or listen address until that operation is completed.

Table 3–2. Available HP-IB Addresses

Data bus (DIO lines)		Address in ASCII		8170A Factory Settings/ Comments
8 7 6	Selectable 5 4 3 2 1	Talk	Listen	
0 T L	0 0 0 0 0	@	Space	
0 T L	0 0 0 0 1	A	!	
0 T L	0 0 0 1 0	B	"	
0 T L	0 0 0 1 1	C	#	
0 T L	0 0 1 0 0	D	$	
0 T L	0 0 1 0 1	E	%	
0 T L	0 0 1 1 0	F	&	
0 T L	0 0 1 1 1	G	'	Keyboard Mode
0 T L	0 1 0 0 0	H	(	
0 T L	0 1 0 0 1	I	)	
0 T L	0 1 0 1 0	J	*	
0 T L	0 1 0 1 1	K	+	
0 T L	0 1 1 0 0	L	,	
0 T L	0 1 1 0 1	M	-	
0 T L	0 1 1 1 0	N	.	
0 T L	0 1 1 1 1	O	/	
0 T L	1 0 0 0 0	P	0	
0 T L	1 0 0 0 1	Q	1	
0 T L	1 0 0 1 0	R	2	
0 T L	1 0 0 1 1	S	3	
0 T L	1 0 1 0 0	T	4	
0 T L	1 0 1 0 1	U	5	Usually controller address
0 T L	1 0 1 1 0	V	6	
0 T L	1 0 1 1 1	W	7	
0 T L	1 1 0 0 0	X	8	
0 T L	1 1 0 0 1	Y	9	
0 T L	1 1 0 1 0	Z	:	
0 T L	1 1 0 1 1	[	;	Data Mode
0 T L	1 1 1 0 0	\	<	
0 T L	1 1 1 0 1	]	=	
0 T L	1 1 1 1 0	^	>	
0 T L	1 1 1 1 1	_	?	Forbidden setting ! UNT, UNL



L = 1 for listen address, 0 for talk address.
T = 1 for talk address, 0 for listen address.

3–65 HP-IB Keyboard Mode

3–66 Listen

3–67 The syntax is identical to that used via the keyboard. The program codes are mnemonics of the front panel inscription or the inscriptions themselves. Refer to Figure 3–1.

3–68 In addition to First and Last Addresses (FAD, LAD), Start Address (SAD) and End Address (EAD) are programmable. SAD and EAD are limits for memory reporting in Keyboard Talk and Data Talk modes. These are distinct from FAD and LAD which are the limits for the front panel output data (§ 3–13). SAD also defines the first location for data read into the 8170A in the Data Listen mode. SAD increments as data is loaded/reported so that, if a data transmission is interrupted, it can be automatically resumed at the next address. In the Talk Only modes, FAD and LAD provide the limits for loading and reporting.

3–69 The following examples illustrate some typical program steps. The Model 9825A Desktop Computer with HP-IB Interface Model 98034A is used as system controller. In the examples, the 98034A's address is assumed to be 7, thus the address of an instrument on the HP-IB is 7XX where XX is the decimal equivalent of the five least significant bits of the bus address. As 8170A address selector settings of 00111 and 11011 (decimal 7, 27) are assumed, the 9825A address codes are 707 and 727 respectively. Talk or listen addresses (more specifically, bits 6 and 7 of the HP-IB address) are automatically specified by the kind of statement governing the 9825A's activity, e.g., the statement red 707 tells the 9825A to read from the bus and tells the 8170A to talk (in keyboard) mode; the statement wrt 707 tells the 9825A to output to the bus and tells the 8170A to listen (in keyboard mode). Similarly rdb 727 and wrb 727 for the data mode talk and listen addresses.

3–70 Selection of operating mode and codes for address and data. The following example programs 8-bit bus, int addr mode, auto cycle, TTL output level, 20–200 Hz int clock, decimal addr code, hexadecimal data code:

```
wrt 707, "D08 INT AUT TTL CM5 ADR DEC DAT HEX"
```

The string within the quotes represents the actual ASCII characters transmitted over the bus. The spaces have been inserted for optical clarity and may be omitted or replaced by ASCII NUL if desired; any number of such characters may be inserted. Small letters may be used instead of capitals.

3–71 SAD/EAD entry, e.g.:

```
wrt 707, "SAD, 0, ent ead, 12, ent"
```

Space(s) between ent and ead optional. Commas inside the string may be replaced by any sign in ASCII column 010 (= . ! ? + – etc.) except space.

3–72 Data entry, e.g.:

```
wrt 707, "adr, 6, dat, 12, ent, 34, ent, 56,
ent, 78, ent, 9a, ent"
```

where data is stored at consecutive locations from address 6.

3–73 Short-form entry. The line length may be shortened by making the following substitution:

Long form	Short form
, ent	;,
, ent ,	;

Thus the data entry line reduces to:
wrt 707, "adr, 6, dat, 12; 34; 56; 78; 9a;"

SAD/EAD entry becomes:
wrt 707, "sad, 0; , ead, 12; , "

The following example combines SAD and data entry: wrt 707, "sad, 10, dat, 12; 34; 4e; 74; 68;, ". Where data is loaded consecutively from start address 10.

3–74 Data entry: coding. The format (over the bus) of the data entry is the chosen code (HEX, OCT, BIN) translated digit-by-digit into ASCII. The following examples illustrate the different codes.

Data formatting example, 8-bit word selected:

Desired bit pattern 1 1 1 1 1 1 1 0 (= 376 OCT, FE HEX)
BIT D7 BIT D0

ASCII string:

...; 376; . . . . . (if OCT programmed)

...; FE; . . . . . (if HEX programmed)

...; 11111110; . . . . . (if BIN programmed)

Data formatting example, 16-bit word selected:

Desired bit pattern 0001000010001000 (= 010421 OCT, 1111 HEX)
BIT D15 BIT D0

ASCII string:

...; 010421; . . . . . (if OCT programmed)

...; 1111; . . . . . (if HEX programmed)

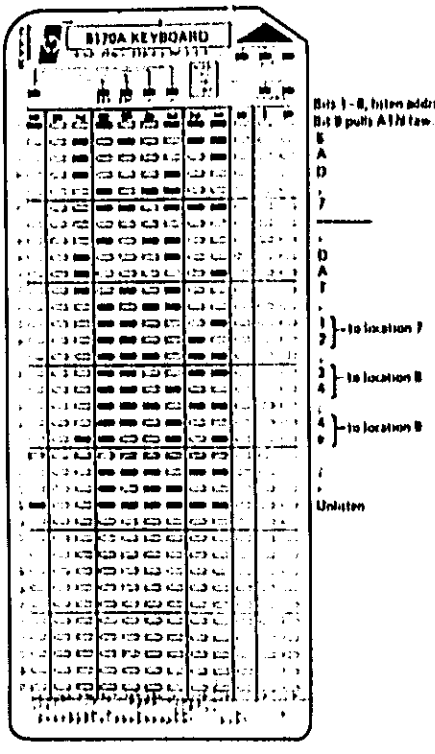
...; 0001000100010001; . . . (if BIN programmed)

Initial zeroes may be omitted.

3–75 Using the Card Reader

3–76 General instructions for using the Card Reader 15263A are contained in its manual. The following marked card example illustrates a combined SAD and data entry:

wrt 707, "SAD,7,DAT,12;34;4e;,"



3–77 Error Messages

3–78 If data is given incorrectly, the 8170A will issue a Service Request, display SRQ and remain in its previous operating condition. To obtain the error code, the system controller must serial poll and arrange to store the response e.g. (for the 9825A):
rds (707) → A.

One of the following codes will then be transferred from the 8170A to (in this example) the 9825A's A register:

HP-IB DIO Lines 8 7 6 5 4 3 2 1	9825A A register	Meaning
0 1 0 0 0 0 0 0	64	Address error (keyboard Mode addr Data Mode addr)
0 1 0 0 0 0 0 1	65	Status error (Syntax error in Idle state becomes status error in Active or Break states)
0 1 0 0 0 0 1 0	66	Mnemonic error
0 1 0 0 0 0 1 1	67	Syntax error
0 1 0 0 0 1 0 0	68	ATN timing error

3–79 Talk

3–80 Talk addressing the 8170A (in the absence of a service request) causes the memory contents from SAD to EAD to appear on the bus. The format of the data for each location is the chosen code (HEX, OCT, BIN) translated digit-by-digit into ASCII. Most-significant-byte leads. There are no separators. The last location (LAD) is terminated by CRLF.

Example: HEX code selected, 8-bit word selected, data incrementing from 9 at SAD to FB at EAD

Bit pattern at SAD 00001001 (= 9 HEX),

bit pattern at EAD 11111001 (= FB HEX)

ASCII string transmitted over bus:

090A0B0C0D0F10 ..... F9FAFBCRLF

Example: OCT code selected, 16-bit word selected

Bit pattern at SAD 0000 0000 0001 0001 (= 21 OCT),

bit pattern at EAD 0001 0001 0001 0001 (= 10421 OCT),

ASCII string transmitted over bus:

000021 ..... 010421 CRLF

A program to read out the memory contents after data storing would typically be organized somewhat as the following example:

```
wrt 707,"sad, 0;, dat, 0; 1; 2; 3; 4;, ead, 3; ,"
< Define buffer for 8170A data >
red 707, < read-in and store routine >
```

Note that, SAD is incremented as each memory location is transmitted. Consequently, if the 8170A is de-addressed then re-addressed, the data transmission will be interrupted and then continued from where it left off. SAD must be redefined if the data is to be transmitted in a single string.

3-81 Talk Only

3-82 The 8170A transmits memory content between FAD and LAD (as opposed to SAD EAD in bus-addressed talk).

Example: HEX code selected, 8-bit word selected, data incrementing from 9 at FAD to FB at LAD

Bit pattern at FAD 00001001 (= 9 HEX),

bit pattern at LAD 11111001 (= FE HEX)

ASCII string transmitted over bus:

```
CRLF ———— to ensure print head
          is at left margin.

09CRLF
0ACRLF
0BCRLF
0DCRLF
0ECRLF
0FCRLF
10CRLF
  .   .
  .   .
  .   .
FBCRLF
FACRLF
FBCRLF
CRLF ———— second CRLF to
          separate consecutive
          print outs.
```

3-83 HP-IB Data Mode

3-84 Listen

3-85 Data is taken from the bus and filed in SAD up. Each word on the HP-IB represents a binary byte. If 16-bit word is selected on the 8170A, high-order byte is transmitted first. The following program, which defines the SAD as 41 in the keyboard mode, then louds a data string from this address on, is typical:

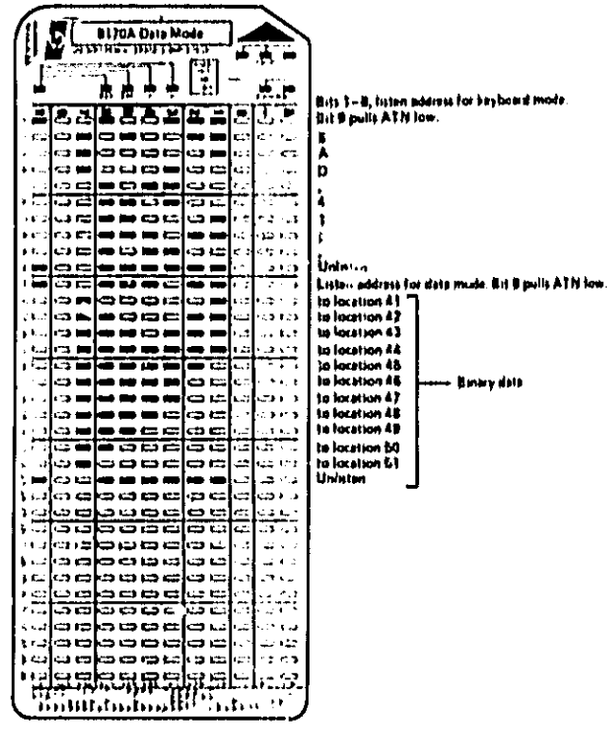
```
wrt 707, "sad, 41;"      Note: Keyboard Mode
                         address.

wrb 727, <binary string> Note: Data
                         Mode address.
```

If the controller must fetch or generate more data before the field is complete, the 8170A should be de-addressed while the controller attends to these tasks. To complete the field, the 8170A should be re-addressed and the data transmission continued from the word (or byte, if 16-bit word is selected) at which the transmission was interrupted.

3-86 Using the Card Reader

3-87 General instructions for using the Card Reader 15263A are contained in its manual. The following marked card example is based on the program in the previous paragraph.



3-88 Error Messages

3-89 Same as in Keyboard Mode (but use Data Mode talk address).

3-90 Talk and Talk Only

3-91 Data is output in binary (same format as in Listen) between SAD/EAD (talk) or FAD/LAD (talk only). Note that, SAD is incremented as words are transmitted. Consequently, if the 8170A is de-addressed then re-addressed, the data transmission will be interrupted and then continued from where it left off. If the entire data is to be transmitted in a single string, SAD must be redefined.

3-92 Code Assignments

3-93 Refer to Table 3-3.

Table 3–3. HP-IB Code Assignments (ASCII) for the 8170A

APPLIES ONLY IN COMMAND MODE (ATN TRUE)

THESE CHARACTERS CAUSE SRQ

THESE CHARACTERS ARE IGNORED

SAME INTERPRETATION

SAME INTERPRETATION

HP-IB DATA LINES	7	0	0	0	0	1	1	1
	6	0	0	1	1	0	1	1
	5	0	1	0	1	0	1	0	1
4 3 2 1									
0 0 0 0	0	NUL		DLE		SP	0	@	P	`	p
0 0 0 1	1	SOH	GTL	DC1	LLO	!	1	A	Q	a	q
0 0 1 0	2	STX		DC2		"	2	B	R	b	r
0 0 1 1	3	ETX		DC3		#	3	C	S	c	s
0 1 0 0	4	EOT		DC4		$	4	D	T	d	t
0 1 0 1	5	ENQ		NAK		%	5	E	U	e	u
0 1 1 0	6	ACK		SYN		&	6	F	V	f	v
0 1 1 1	7	BEL		ETB		'	7	G	W	g	w
1 0 0 0	8	BS		CAN	SPE	(	8	H	X	h	x
1 0 0 1	9	HT		EM	SPD	)	9	I	Y	i	y
1 0 1 0	10	LF		SUB		*	:	J	Z	j	z
1 0 1 1	11	VT		ESC		+	;	K	[	k	{
1 1 0 0	12	FF		FS		,	<	L	\	l	|
1 1 0 1	13	CR		GS		-	=	M	]	m	}
1 1 1 0	14	SO		RS		.	>	N	^	n	~
1 1 1 1	15	SI		US		/	?	O	_	o	DEL

MLA ASSIGNED TO DEVICE — MTA ASSIGNED TO DEVICE — UNL — UNT

3–94 RS 232C PROGRAMMING INSTRUCTIONS

3–95 The following 8170A activities can be directed from a data terminal using this interface:

status message,

memory examination,

memory change,

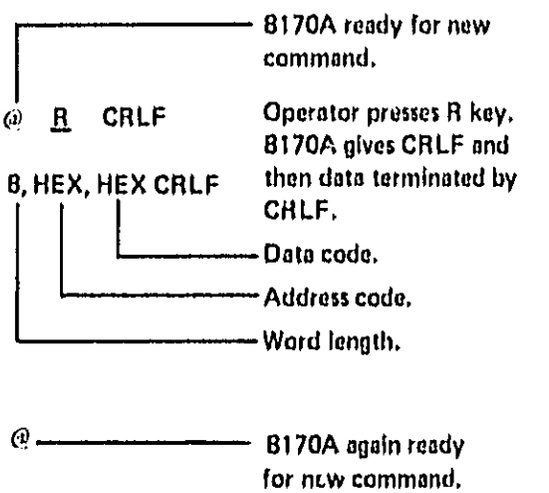
memory listing

Note: The 8170A is wired as a DCE (Data Communication Equipment), EIA Std RS 232C/CCITT V.24.

The bus lines used, terminations, logic levels and pinouts are described in Section II. Front panel operations are protected against interruption from the RS 232C. Thus, if a manually-invoked operation is in progress, the 8170A will not respond to a data terminal until that operation is completed.

3–96 Status Message

3–97 Data bus (8/16 bit), address code and data code are displayed on the screen when the terminal's R key is pressed:



Note: Underlined characters are entered by operator on the terminal keyboard. They are accepted by the 8170A and are then returned to the terminal for display (full duplex). Characters not underlined originate from the 8170A. The underline does not appear on the display.

3–98 Memory Examination and Change

3–99 A memory location can be examined by entering M and the required address at the terminal:

@	M	CRLF	Operator presses M, 8170A gives CRLF.
1 2 3	1 F		Operator types 1 2 3. 8170A responds with two spaces, followed by address 1 2 3's data followed by two spaces.

From this point, the operator may:
end operation (. key),
go on to next address (CR),
or change the data.

For example

@	M		
1 2 3	1 F	6 A	Operator changes address 123 data to 6 A. System automatically goes to next address.
1 2 4	A A	1 CR	Operator changes data from AA to 01. CR signals that there is no further data entry. Line is overwritten with complete data. System goes to next address.
1 2 5	0 6	CR	No change to data. System goes to next address.
1 2 6	D C	.	Operation ends.
@			

Leading zeroes need not be entered by the operator. In the case of an address, the line is overwritten with a space for each omitted leading zero – the digits consequently occupy the vertical column appropriate to its weighting. With data, the omitted leading zeroes are regenerated. In the above example (address 124, data change from AA to 01) the overwritten line would appear as:

1 2 4 A A 0 1

When 110 baud is selected (for teleprinter), the 8170A's control logic automatically causes a new line to be generated instead of overwriting.

3–100 Memory Listing

3–101 A dialog to define start and end of the list is called up using the P key:

@	P	
S T A R T A D D R . :	1 0 ▲	8170A demands the start address. Because, in this example, the address is incomplete (only 2 digits), the operator inserts a space (▲) after the address
S T O P A D D R . :	1 6 A	8170A demands stop address.
1 0	1 F	Display of address and corresponding data follows automatically. Space is transmitted instead of initial zeroes. Double space between address and data. CRLF follows each data.
1 1	2 E	
1 2	3 D	
.		
.		
.		
1 6 9	7 8	
1 6 A	A F	Read-out terminates at stop address. 8170A again ready for a new command.
@		

The listing may be discontinued at any time by pressing the terminal's space bar. Pressing a second time allows the list to continue from where it left off. The terminal's period (.) key can be used to terminate the listing before the stop address is reached.

3–102 Having discontinued the listing, a line may be changed by pressing the terminal's M key and writing new data. Subsequently, the M operation may be discontinued and the listing continued by pressing the period (.) key.

SECTION

IV

SECTION IV
FUNCTION TESTS

4–1 INTRODUCTION

4–2 The procedures in this section test the instrument using the specifications of Table 1–2 as standards. All tests can be performed without access to the interior of the instrument.

4–3 EQUIPMENT REQUIRED

4–4 Equipment required for the function tests is listed in Table 1–1 Recommended Test Equipment. Any equipment that satisfies the critical specifications given in the table may be substituted for the recommended model(s).

4–5 TEST RECORD

4–6 Results of the function tests may be tabulated on the test procedures. Test results recorded at incoming inspection can be used for comparison in periodic maintenance, troubleshooting, and after repairs or adjustments.

4–7 FUNCTION TESTS

4–8 The function tests given in this section are suitable for incoming inspection, troubleshooting, or preventive maintenance. During any function test, all shields and connecting hardware must be in place. The tests are designed to verify the published instrument specifications. Perform the tests in the order given and record the data in the data spaces provided at the end of each procedure.

4–9 Each test is arranged so that the specification is written as it appears in Table 1–2. Next, a description of the test and any special instructions or problem areas are included. Each test that requires test equipment has a setup drawing and a list of the required equipment. The initial steps of each procedure give control settings required for that particular test.

FUNCTION TESTS

4–10 DATA OUTPUT FUNCTION TEST

SPECIFICATION

Data pods provide 16 output lines (Model 16455A D0 to D7, Model 16456A D8 to D15), pos/neg true selectable on rear panel. Data generation in ascending address sequence from First to Last Address.

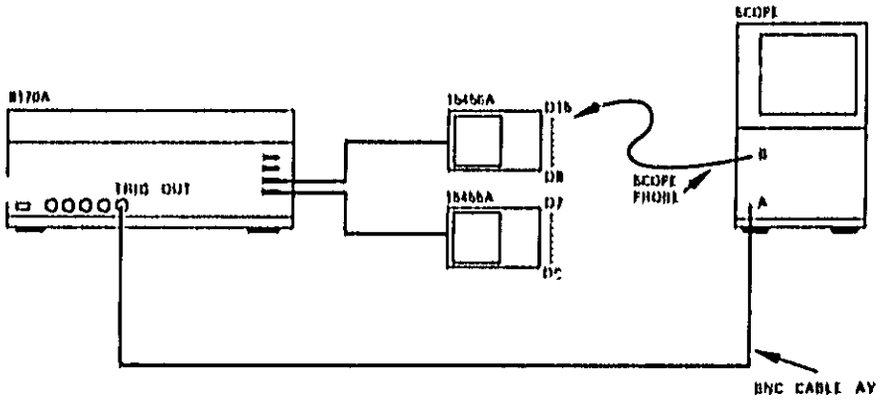


Figure 4–1. Test Setup for Data Output Function Test

EQUIPMENT

Oscilloscope with probe
BNC cable assembly, 61 cm

PROCEDURE

1. Connect the equipment as shown in Figure 4–1.

2. Set the 8170A as follows:

DATA BUS	16 BIT
ADDR MODE	INT
CYCLE	AUTO
OUTPUT LEVEL	TTL
CLOCK MODE	INTERNAL .2 MHz – 20 kHz
Vernier	CCW
DATA (required)	HI
ADDR CODE	HEX

3. Load:

F-ADDR	zero
T-ADDR	zero
L-ADDR	7FF

FUNCTION TESTS

4. Set memory (all ones), see § 3–30.

5. Press START key.

6. Adjust oscilloscope so that two TRIG OUT pulses are displayed on the A trace.

7. Check each data line (pod outputs D0 to D15) in turn with the scope probe. A continuous high level should be displayed by the B trace ..... YES/NO

NOTE: If any bit is incorrect, a narrow negative pulse will be observed. To find the address of the faulty bit:
connect data line concerned to BREAK IN,
set DATA switch to LO.

The faulty bit stops data generation and its address is then one less than that displayed. Disconnect BREAK IN. Return DATA switch to HI. Press START key.

8. Reset memory (all zeroes), see § 3–30.

9. Check each data line (pod outputs D0 to D15) in turn with the scope probe. A continuous low level should be displayed by the B trace ..... YES/NO

NOTE: If any bit is incorrect, a narrow positive pulse will be observed. To find the address of the faulty bit, connect the data line concerned to BREAK IN. The faulty bit stops data generation and its address is then one less than that displayed. Disconnect BREAK IN. Press START key.

10. Press the STOP key.

11. Check each data line (pod outputs D0 to D15) in turn with the scope probe to verify 3-state (+1.4 V, high impedance) ..... YES/NO

FUNCTION TESTS

4–11 EXTERNAL ADDRESS AND DAV FUNCTION TEST

SPECIFICATION

Data generation follows external address and enable signals. DAV generated at each new address, pos/neg true selectable on rear panel. 12 address lines (positive true) A0 to A9 via Address Input Pod Model 15453A; A10, A11 and DAV via Control Pod Model 15454A. Enable signals (EN1, EN2 via Control Pod; EN3, EN4 via rear panel) pos/neg true/don't care selectable.

DESCRIPTION

This test verifies that the displayed address corresponds to the applied external address. DAV and the 8170A selector lines EN1–4 are then mutually checked using static logic levels.

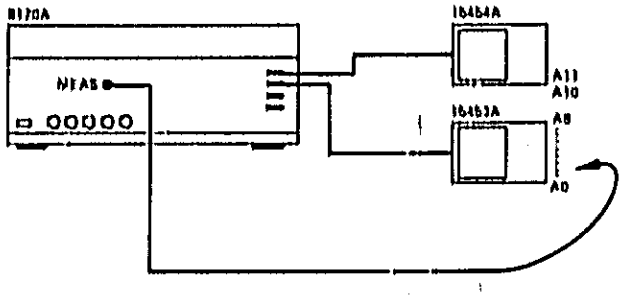


Figure 4–2. Test Setup for External Address Test

EQUIPMENT

Figure 4–2	Figure 4–3
none	Oscilloscope with probe

PROCEDURE

1. Connect the 8170A and pods as shown in Figure 4–2.

2. Set the 8170A as follows:

DATA BUS	8 BIT
ADDR MODE	EXT
OUTPUT LEVEL	TTL
SET	CW
DATA (rear panel)	HI
EN1 to EN4 (rear panel)	OFF
DAV (rear panel)	HI

3. Press ADDR then DEC keys. Verify that DEC appears in the address display window.

4 Press START key.

FUNCTION TESTS

5. In turn, connect each address line to the MEAS test point on the front panel. Verify the displayed address:

Address line connected to MEAS	Address display DEC	YES/NO
15453A		
A 0	0 0 0 1	
A 1	0 0 0 2	
A 2	0 0 0 4	
A 3	0 0 0 8	
A 4	0 0 1 6	
A 5	0 0 3 2	
A 6	0 0 6 4	
A 7	0 1 2 8	
A 8	0 2 5 6	
A 9	0 5 1 2	
15454A		
A 10	1 0 2 4	
A 11	2 0 4 8	

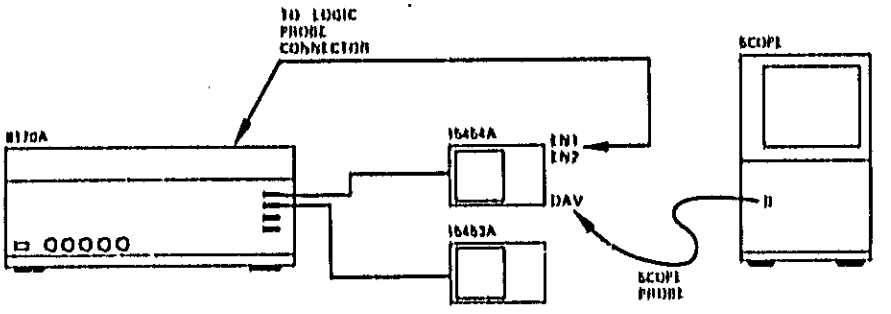


Figure 4–3 Test Setup for DAV/EN Function Test

6. Connect the equipment as shown in Figure 4–3.

7. Set EN 1 switch (rear panel) to HI, verify that DAV line is in tri-state ..... YES / NO

8. Apply +5 V from LOGIC PROBE connector (rear panel) to the EN1 line (Control Pod). Verify DAV line is low ..... YES/NO

9. Set EN1 switch to LO, Verify DAV line is in 3-state. ..... YES/NO

10. Remove EN1 line from LOGIC PROBE connector. Verify DAV line is low ..... YES/NO

11. Set EN1 switch to OFF.

12. Repeat steps 7 to 11 for EN2, EN3 and EN4 (EN3, EN4 lines on rear panel) ..... YES/NO

13. Set DAV switch (rear panel) to LO. Repeat steps 7–10, verify DAV line goes high in steps 8 and 10 ..... YES/NO

FUNCTION TESTS

4–12 EXT CLOCK AND STATE FUNCTION TEST

SPECIFICATION

External Clock dc to 2 MHz.
Operating states:

Idle: permits entry of address, data and operating parameters, Data and DAV in tri-state, ACS low, BRS high.

Active: continuous data output, ACS high, BRS high.

Break: static data output, ACS low, BRS low.

Input characteristics: high level ≥ + 2.0 V , low level ≤ + 0.8 V, min width (at + 1.3 V) 40 ns.

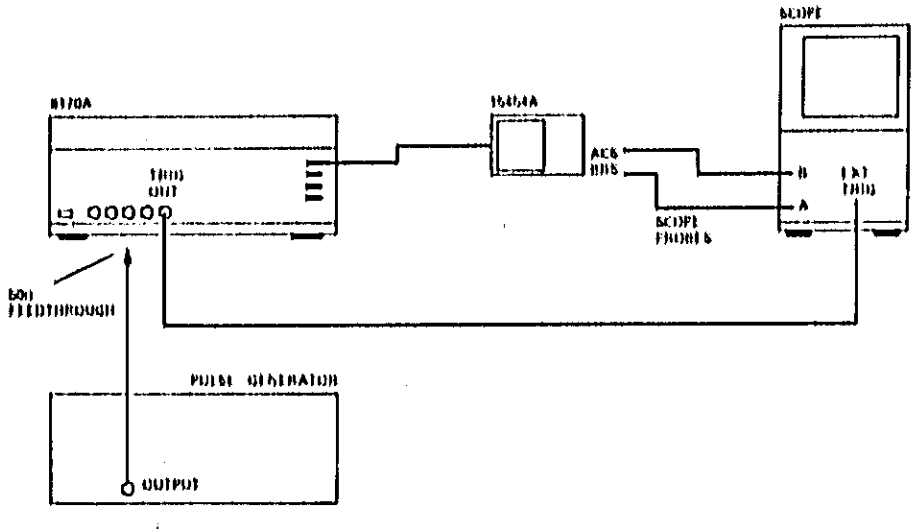


Figure 4–4. Test Setup for Ext Clock and State Function Test

EQUIPMENT

Pulse generator
Oscilloscope with 2 probes
BNC cable assembly, 30 cm
BNC cable assembly, 61 cm

PROCEDURE

1. Connect the equipment as shown in Figure 4–4.

FUNCTION TESTS

2. Set the 8170A as follows:

DATA BUS	8 BIT
ADDR MODE	INT
CYCLE	AUTO
OUTPUT LEVEL	TTL
CLOCK MODE	EXT

3. Load:

F-ADDR	zero
T-ADDR	zero
L-ADDR	zero

4. Press START key.

5. Set pulse generator for a 2 V pulse, width ≥ 40 ns, and apply to CLOCK IN. Verify TRIG OUT pulses ..... YES/NO

6. Transfer pulse generator connection from CLOCK IN to STOP IN. Verify that 8170A goes to Idle state and that ADDRESS and DATA value displays are blanked ..... YES/NO

   Verify ACS low, BRS high: ..... YES/NO

7. Transfer pulse generator from STOP IN to START IN

   Verify that the 8170A goes to Active State. Verify ACS high, BRS high ..... YES/NO

8. Transfer pulse generator from START IN to BREAK IN. Verify that the 8170A goes to Break state ..... YES/NO

   Verify ACS low, BRS low ..... YES/NO

FUNCTION TESTS

4–13 ADDRESS OUTPUT (OPTION 002) FUNCTION TEST

SPECIFICATION

Data generation in ascending address sequence from First to Last Address. Option 002 Address Output Pod Model 16452A provides 10 address output lines, A0 to A9, positive true, 3-state capability.

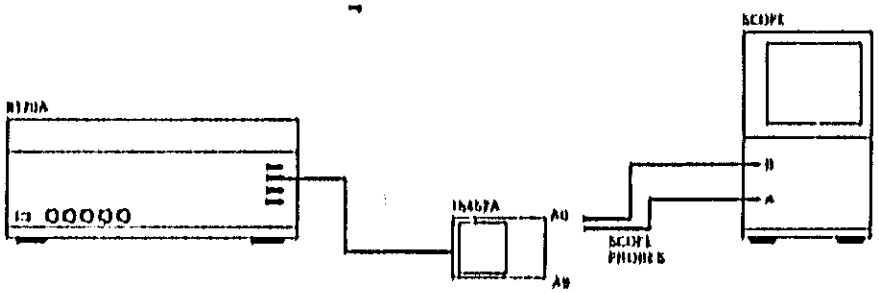


Figure 4–5. Test Setup for Address Output Function Test

EQUIPMENT

Oscilloscope with 2 probes.

PROCEDURE

1. Connect equipment as shown in Figure 4–5.

2. Set the 8170A as follows:

   DATA BUS ..... 8 BIT
   ADDR MODE ..... INT
   CYCLE ..... AUTO
   OUTPUT LEVEL ..... TTL
   CLOCK MODE ..... INTERNAL 2 M – .2 M
   Vernier ..... CCW
   ADDR CODE ..... HEX

3. Load:

   F-ADDR ..... zero
   L-ADDR 3FF

4. Press START key.

5. Start with A0 and A1 lines connected to the scope's A and B channels.
   Change connections so that lines A1, A2 then A2, A3 and so-on are displayed.
   Verify that the frequency doubles between adjacent lines ..... YES/NO

ADJUSTMENTS

SECTION V
ADJUSTMENTS

5–1 INTRODUCTION

5–2 This section describes the adjustments which will return the instrument to peak operating condition after repairs are completed.

5–3 SAFETY CONSIDERATIONS

5–4 Although this instrument has been designed in accordance with international safety standards, this manual contains information, cautions, and warnings which must be followed to ensure safe operation and to retain the instrument in safe condition (see Sections II and III). Service and adjustments should be performed only by qualified service personnel. Safety checks are presented in Section VIII.

WARNING

Any interruption of the protective (grounding) conductor (inside or outside the instrument) or disconnection of the protective earth terminal is likely to make the instrument dangerous. Intentional interruption is prohibited.

5–5 Any adjustment, maintenance, and repair of the opened instrument with voltage applied should be avoided as much as possible, and, when inevitable, should be carried out only by a skilled person who is aware of the hazard involved.

5–6 Capacitors inside the instrument may still be charged even if the instrument has been disconnected from its source of supply.

5–7 Make sure that only fuses with the required rated current and of the specified type (normal blow, time delay, etc.) are used for replacement. The use of repaired fuses and the shortcircuiting of fuseholders must be avoided.

5–8 Whenever it is likely that the protection offered by fuses has been impaired, the instrument must be made inoperative and secured against any unintended operation.

WARNING

Adjustments described herein are performed with power supplied to the instrument while protective covers are removed. Energy available at many points may, if contacted, result in personal injury.

5–9 EQUIPMENT REQUIRED

5–10 The test equipment required for the adjustment procedures is listed in Table 1–1, Recommended Test Equipment. The critical specifications of substitute test instruments must meet or exceed the standards listed in the table if the instrument is to meet the standards set forth in Table 1–2, Specifications.

5–11 ADJUSTMENT PROCEDURE

5–12 Allow a 15-minute warm-up time before starting the adjustments. During adjustments, keep the covers in place as far as is possible so that the instrument's temperature remains steady. Refer to Figure 6–1 for removal of top cover and assembly location; all other covers should remain fitted.

5–13 POWER SUPPLY ADJUSTMENT

EQUIPMENT

DVM
2,5 ohm, 10 W resistor
Extender boards

PROCEDURE

1. Connect the Control, Address Input and both Data Pods to the 8170A.

2. Set the 8170A as follows:

DATA BUS	16 BIT
ADDR MODE	INT
CYCLE	AUTO
OUTPUT LEVEL	VAR
SET	CW
CLOCK MODE	INTERNAL 2 MHz – .2 MHz
Vernier	CCW
ADDR CODE	HEX

3. Set memory (all ones), see 5 3–30.

4. Press START key.

5. Set A7R3 (see Service Sheet 7) CW.

6. Adjust A7R14 for a DVM reading of + 5,00 V at the + 5 V testpoint.

7. Connect the 2,5 Ohm resistor between the + 5 V testpoint and chassis.

8. Set the max. current limit by rotating A7R3 slowly CCW until the voltage at the + 5 V testpoint just begins to decrease.

9. Remove the resistor.

10. Check and adjust the following voltages:

Location	Testpoint	Adjust	Result
A7	+ 0,6 V	A7R17	+ 0,59 V to + 0,61 V
	– 3 V	A7R21	– 2,97 V to – 3,03 V
	+ 12 V	–	+ 11,94 V to + 12,03 V
	– 12 V	–	–11,94 V to – 12,06 V
Front panel	MEAS	SET	+ 15,0 V
Data pod	any data line	A7R16	+ 15,0 V (VAR selected)
		A7R40	+ 4,75 V (TTL selected)

5–14 CLOCK RATE ADJUSTMENT

EQUIPMENT

Counter
Extender boards

PROCEDURE

1. Set the 8170A as follows:

   DATA BUS ..... 8 BIT
   ADDRESS MODE ..... INT
   CYCLE ..... AUTO
   CLOCK MODE ..... INTERNAL 2 MHz – .2 MHz
   Vernier ..... CCW
   DAV DELAY (rear panel) ..... MIN

2. Press START key.

3. Connect high impedance counter to A4TP1 and check frequency ≥ 2.1 MHz.

4. Turn vernier CW and adjust A4R14 for a counter reading of 175 kHz to 188 kHz.

5. Check that the frequencies at the extremities of each range extend at least as far as the nominal.

6. Select lowest frequency range (200 Hz – 20 Hz) and set vernier CW. Verify that ADDRESS and DATA value displays operate.

7. Slowly increase frequency and check that the displays blank at approx 25 Hz.

5–16 EXT START ADJUSTMENT

EQUIPMENT

Oscilloscope with probe
Pulse generator
50 Ohm feedthrough termination
BNC cable assembly, 30 cm
Extender boards

PROCEDURE

1. Set 8170A as follows:

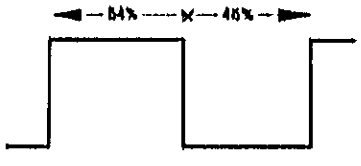
DATA BUS	8 BIT
ADDR MODE	INT
CYCLE	SINGLE
CLOCK MODE	INTERNAL 2 MHz – .2 MHz
Vernier	CCW
ADDR CODE	DEC
DAV DELAY (rear panel)	MIN

2. Load :

F-ADDR	zero
T-ADDR	6
L-ADDR	10

3. Apply a 2 V pulse (width ≥ 40 ns, approx 10 kHz rep rate) to START IN via the 50-ohm feedthrough.

4. Connect oscilloscope to A4TP1 with probe and adjust A4R15 for 54% duty cycle.



PARTS LIST

SECTION VI
REPLACEABLE PARTS

6–1 INTRODUCTION

6–2 This section contains information for ordering parts. Table 6–1 lists abbreviations used in the parts lists and elsewhere in the manual. Table 6–2 lists all replaceable parts in reference designator order.

6–3 ABBREVIATIONS

6–4 Table 6–1 lists abbreviations used in the parts lists, schematics and elsewhere in the manual. In some cases two forms of the abbreviation are used, one all in capital letters, and one partial or no capitals. This occurs because the abbreviations in the parts lists are always all capitals. However, in the schematics and other parts of the manual, the same abbreviations may have upper and lower case letters.

6–5 REPLACEABLE PARTS

6–6 Table 6–2 is the list of replaceable parts and is organised as follows:

a. Mainframe (chassis) parts in alphanumerical order by reference designation.

b. Electrical assemblies and their components in alpha-numerical order by reference designation.

Reference designators are of the form A5R9 i.e. resistor 9 on assembly 5.

6–7 The information given for each part consists of the following:

a. The Hewlett-Packard part number.

b. The description of the part.

6–8 ORDERING INFORMATION

6–9 To order a part listed in the replaceable parts table, quote the Hewlett-Packard part number, indicate the quantity required, and address the order to the nearest Hewlett-Packard office (list of Sales/Service offices at the rear of this manual).

6–10 To order a part that is not listed in the replaceable parts table, include the instrument model number, instrument serial number, the description and function of the part, and the number of parts required, address the order to the nearest Hewlett-Packard office.

Table 6–1. Reference Designators and Abbreviations

REFERENCE DESIGNATIONS

A . . . . . assembly
AT . . . attenuator; isolator; termination
B . . . . . fan; motor
BT . . . . . battery
C . . . . . capacitor
CP . . . . . coupler
CR . . . . . diode; diode thyristor; varactor
DC . . . directional coupler
DL . . . . . delay line
DS . . . . . annunciator; signaling device (audible or visual); lamp; LED
E . . . . . miscellaneous electrical part
F . . . . . fuse
FL . . . . . filter
H . . . . . hardware
HY . . . . . circulator
J . . . . . electrical connector (stationary portion); jack
K . . . . . relay
L . . . . . coil; inductor
M . . . . . meter
MP . . . . . miscellaneous mechanical part
P . . . . electrical connector (movable portion); plug
Q . . . . . transistor; SCR; triode thyristor
R . . . . . resistor
RT . . . . . thermistor
S . . . . . switch
T . . . . . transformer
TB . . . . . terminal board
TC . . . . . thermocouple
TP . . . . . test point
U . . . . . integrated circuit; microcircuit
V . . . . . electron tube
VR . . . voltage regulator; breakdown diode
W . . . . cable; transmission path; wire
X . . . . . socket
Y . . . . crystal unit (piezoelectric or quartz)
Z . . . . tuned cavity; tuned circuit

ABBREVIATIONS

A . . . . . ampere
ac . . . . alternating current
ACCESS . . . . . accessory
ADJ . . . . . adjustment
A/D. . . . . analog-to digital
AF . . . . . audio frequency
AFC . . . . . automatic frequency control
AGC . . . . . automatic gain control
AL . . . . . aluminum
ALC . . . . automatic level control
AM . . . amplitude modulation
AMPL . . . . . amplifier
APC . . . . automatic phase control
ASSY. . . . . assembly
AUX . . . . . auxiliary
avg . . . . . average
AWG . . . . . American wire gauge
BAL . . . . . balance
BCD . . . . . binary coded decimal
BD . . . . . board
BE CU . . . . . beryllium copper
BFO . . . . beat frequency oscillator
BH . . . . . binder head
BKDN . . . . . breakdown
BP . . . . . bandpass
BPF. . . . . bandpass filter
BRS . . . . . brass
BWO . . . . backward-wave oscillator
CAL . . . . . calibrate
ccw . . . . counter-clockwise
CER . . . . . ceramic
CHAN . . . . . channel
cm . . . . . centimeter
CMO . . cabinet mount only
COAX . . . . . coaxial
COEF . . . . . coefficient
COM . . . . . common
COMP . . . . composition
COMPL . . . . . complete
CONN . . . . . connector
CP . . . . . cadmium plate
CRT . . . cathode-ray tube
CTL . . . . complementary transistor logic
CW . . . . continuous wave
cw . . . . . clockwise
cm . . . . . centimeter
D/A. . . . . digital-to-analog
dB . . . . . decibel
dBm . . . . decibel referred to 1 mW
dc. . . . . direct current
deg . . . degree (temperature interval or difference)
. . . degree (plane angle)
°C . . . . . degree Celsius (centigrade)
°F . . . . degree Fahrenheit
°K . . . . . degree Kelvin
DEPC . . deposited carbon
DET . . . . . detector
diam . . . . . diameter
DIA . . . diameter (used in parts list)
DIFF AMPL . . . differential amplifier
div . . . . . division
DPDT . . . . double pole, double-throw
DR . . . . . drive
DSB . . . double sideband
DTL . . . diode transistor logic
DVM . . . . digital voltmeter
ECL . . . . emitter coupled logic
EMF . . electromotive force
EDP . . . . electronic data processing
ELECT. . . . . electrolytic
ENCAP. . . . . encapsulated
EXT . . . . . external
F . . . . . farad
FET . . . . . field-effect transistor
F/F . . . . . flip-flop
FH . . . . . flat head
FIL H . . . . . fillister head
FM . frequency modulation
FP . . . . . front panel
FREQ . . . . . frequency
FXD . . . . . fixed
g . . . . . gram
GE . . . . . germanium
GHz . . . . . gigahertz
GL . . . . . glass
GRD . . . . . ground(ed)
H . . . . . henry
h . . . . . hour
HET . . . . . heterodyne
HEX . . . . . hexagonal
HD . . . . . head
HDW . . . . . hardware
HF . . . . . high frequency
HG . . . . . mercury
HI . . . . . high
HP . . . . Hewlett-Packard
HPF. . . . . high pass filter
HR . . . . . hour (used in parts list)
HV . . . . . high voltage
Hz . . . . . Hertz
IC. . . . . integrated circuit
ID. . . . . inside diameter
IF . . . . . intermediate frequency
IMPG. . . . . impregnated
in . . . . . inch
INCD. . . . . incandescent
INCL . . . . . included(s)
INP. . . . . input
INS. . . . . insulation
INT. . . . . internal
kg . . . . . kilogram
kHz . . . . . kilohertz
kΩ . . . . . kilohm
kV . . . . . kilovolt
lb . . . . . pound
LC . . . . . inductance-capacitance
LED . . light-emitting diode
LF . . . . . low frequency
LG . . . . . long
LH . . . . . left hand
LIM. . . . . limit
LIN. . . . linear taper (used in parts list)
lin . . . . . linear
LK WASH . . . lock washer
LO . . . low; local oscillator
LOG . . . logarithmic taper (used in parts list)
log . . . . . logarithm(ic)
LPF. . . . . low pass filter
LV . . . . . low voltage
m . . . . . meter (distance)
mA . . . . . milliampere
MAX . . . . . maximum
MΩ . . . . . megohm
MEG . . . . meg (10^6) (used in parts list)
MET FLM . . . . metal film
MET OX . . . metallic oxide
MF . . . medium frequency; microfarad (used in parts list)
MFR . . . . . manufacturer
mg . . . . . milligram
MHz . . . . . megahertz
mH . . . . . millihenry
mho . . . . . mho
MIN . . . . . minimum
min . . . . . minute (time)
' . . . . . minute (plane angle)
MINAT. . . . . miniature
mm . . . . . millimeter
MOD . . . . . modulator
MOM . . . . . momentary
MOS . . . . . metal-oxide semiconductor
ms . . . . . millisecond
MTG . . . . . mounting
MTR . . . meter (indicating device)
mV . . . . . millivolt
mVac. . . . . millivolt, ac
mVdc . . . . millivolt, dc
mVpk . . . . millivolt, peak
mVp-p . . . millivolt, peak to peak
mVrms . . . . millivolt, rms
mW . . . . . milliwatt
MUX . . . . . multiplex
MY . . . . . mylar
μA . . . . . microampere
μF. . . . . microfarad
μH . . . . . microhenry
μmho. . . . . micromho
μs . . . . . microsecond
μV . . . . . microvolt
μVac . . . . microvolt, ac
μVdc . . . . microvolt, dc
μVp-p . . . microvolt, peak-to peak
μVrms . . . microvolt, rms
μW . . . . . microwatt
nA . . . . . nanoampere
NC . . . . . no connection
N/C. . . . normally closed
NE . . . . . neon
NEG . . . . . negative
nF . . . . . nanofarad
NI PL . . . . . nickel plate
N/O . . . . normally open
NOM . . . . . nominal

NOTE

All abbreviations in the parts list will be in upper-case.

Table 6-1. Reference Designators and Abbreviations (cont'd)

NORM . . . . . normal
NPN . . . negative positive negative
NPO . . . . negative positive zero (zero temperature coefficient)
NRFR . . not recommended for field replacement
NSR . . . . . not separately replaceable
ns . . . . . nanosecond
nW . . . . . nanowatt
OBD . order by description
OD . . . . outside diameter
OH . . . . . oval head
OP AMPL . . . . operational amplifier
OPT . . . . . option
OSC . . . . . oscillator
OX . . . . . oxide
oz . . . . . ounce
Ω . . . . . ohm
P . . . . peak (used in parts list)
PAM . . . . pulse amplitude modulation
PC . . . . . printed circuit
PCM . . pulse code modulation; pulse count modulation
PDM . . . . . pulse duration modulation
pF . . . . . picofarad
PH BRZ . phosphor bronze
PHL . . . . . Phillips
PIN . . . . positive intrinsic negative
PIV . . . . . peak inverse voltage
pk . . . . . peak
PL . . . . . phase lock
PLO . . . . . phase lock oscillator
PM . . . . phase modulation
PNP . . . . positive negative positive
P/O . . . . . part of
POLY . . . . . polystyrene
PORC . . . . . porcelain
POS . . positive; position(s) (used in parts list)
POSN . . . . . position
POT . . . potentiometer
p p . . . . peak to peak
PP . . . peak to peak (used in parts list)
PPM . . . . pulse position modulation
PREAMPL . . . preamplifier
PRF . . . pulse repetition frequency
PRR . . . pulse repetition rate
ps . . . . picosecond
PT . . . . . point
PTM . . . pulse time modulation
PWM . . . pulse width modulation
PWV . . . . peak working voltage
RC . resistance capacitance
RECT . . . . . rectifier
REF . . . . . reference
REG . . . . . regulated
REPL . . . . . replaceable
RF . . . . radio frequency
RFI . . . . radio frequency interference
RH . . . round head; right hand
RLC . . . . . resistance inductance capacitance
RMO . . . rack mount only
rms . . . . root mean square
RND . . . . . round
ROM . . read only memory
R&P . . . . rack and panel
RWV . . . reverse working voltage
S . . . scattering parameter
s . . . . . second (time)
" . . second (plane angle)
SB . . . . slow blow (fuse) (used in parts list)
SCR . . . silicon controlled rectifier; screw
SE . . . . . selenium
SECT . . . . . sections
SEMICON . . . . semiconductor
SHF . . . . superhigh frequency
SI . . . . . silicon
SIL . . . . . silver
SL . . . . . slide
SNR . signal to noise ratio
SPDT . . . . single pole, double throw
SPG . . . . . spring
SR . . . . . split ring
SPST . . . . single pole, single throw
SSB . . . . single sideband
SST . . . . stainless steel
STL . . . . . steel
SQ . . . . . square
SWR . . standing wave ratio
SYNC . . . . synchronize
T . . timed (slow blow fuse)
TA . . . . . tantalum
TC . . . . . temperature compensating
TD . . . . . time delay
TERM . . . . . terminal
TFT . . thin film transistor
TGL . . . . . toggle
THD . . . . . thread
THRU . . . . . through
TI . . . . . titanium
TOL . . . . . tolerance
TRIM . . . . trimmer
TSTR . . . . . transistor
TTL . . transistor transistor logic
TV . . . . . television
TVI . television interference
TWT . . travelling wave tube
U . . . . micro (10^{-6}) (used in parts list)
UF . . . microfarad (used in parts list)
UHF . . ultrahigh frequency
UNREG . . . . unregulated
V . . . . . volt
VA . . . . . voltampere
Vac . . . . . volts, ac
VAR . . . . . variable
VCO . voltage controlled oscillator
Vdc . . . . . volts, dc
VDCW . . volts, dc, working (used in parts list)
V(F) . . . . volts, filtered
VFO . . variable frequency oscillator
VHF . . . . very high frequency
Vpk . . . . . volts, peak
Vp p . . volts, peak to peak
Vrms . . . . . volts, rms
VSWR . . voltage standing wave ratio
VTO . . . . voltage tuned oscillator
VTVM . . . . Vacuum tube voltmeter
V(X) . . . . volts, switched
W . . . . . watt
W . . . . . with
WIV . . . . working inverse voltage
WW . . . . . wirewound
W/O . . . . . without
YIG . . yttrium iron garnet
Z_0 . . . . characteristic impedance

MULTIPLIERS

Abbreviation	Prefix	Multiple
T	tera	10^{12}
G	giga	10^{9}
M	mega	10^{6}
k	kilo	10^{3}
da	deka	10
d	deci	10^{-1}
c	centi	10^{-2}
m	milli	10^{-3}
μ	micro	10^{-6}
n	nano	10^{-9}
p	pico	10^{-12}
f	femto	10^{-15}
a	atto	10^{-18}

NOTE

All abbreviations in the parts list will be in upper case.

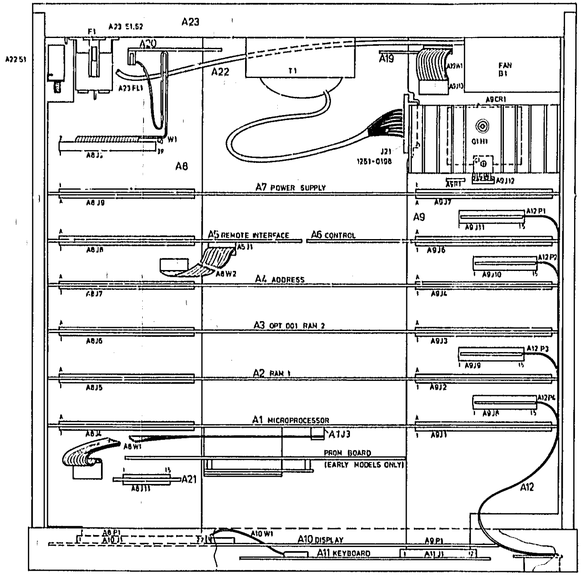


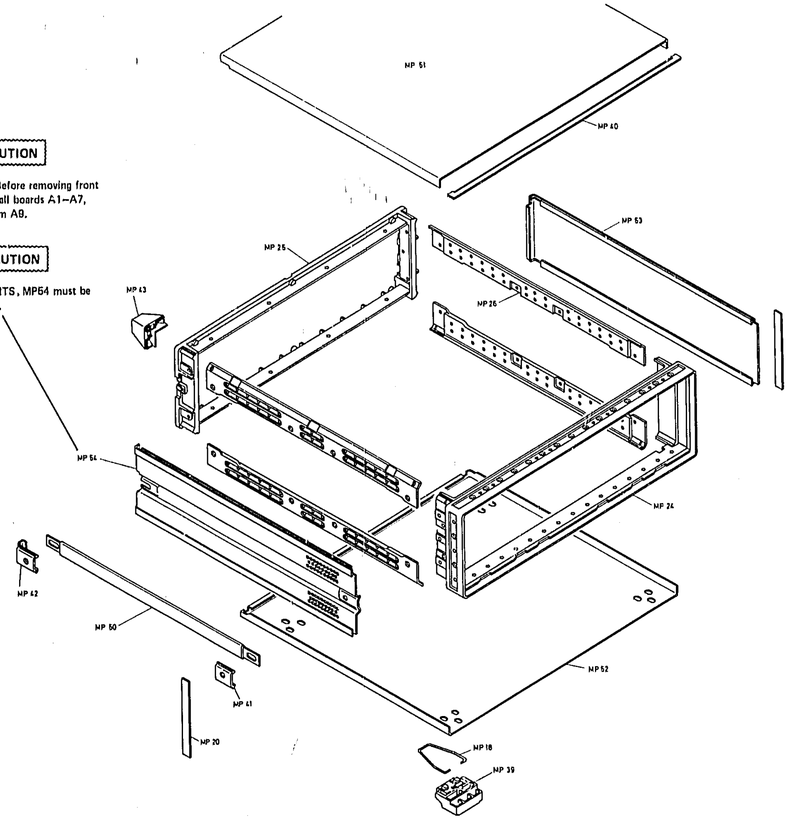
Figure 6–1. Mainframe Parts

CAUTION

A12 is fragile. Before removing front panel: Remove all boards A1–A7, unplug A12 from A9.

CAUTION

COOLING VENTS, MP64 must be fitted as shown.



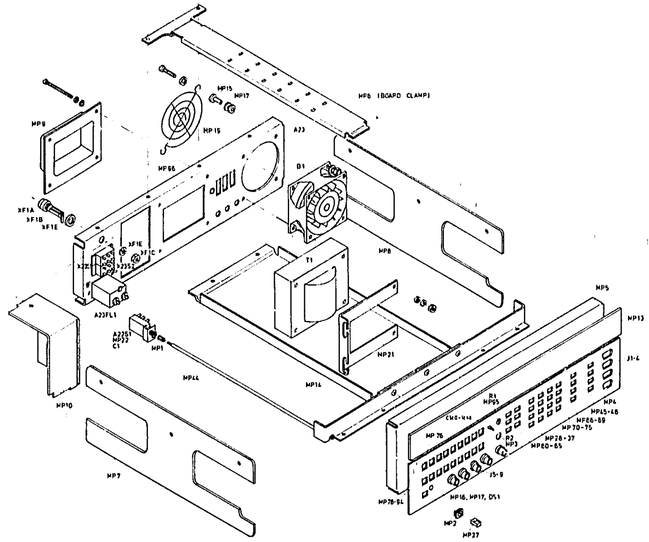


Table 6-2. Replaceable Parts

Mainframe

REFERENCE DESIGNATOR	H-P PART NUMBER	DESCRIPTION
A1	08170-66501	BD AY M. PROC.
A2	08170-66502	BD AY RAM 1
A3	08170-66503	BD AY RAM 2 (OPTION 001 ONLY)
A4	08170-66504	BD AY ADDRESS
A5	08170-66505	BD AY UP-IO
A6	08170-66506	BD AY CONTROL
A7	08170-66507	BD AY PWR SPLY
A8	08170-66508	BD AY MOTHER 1
A9	08170-66509	BD AY MOTHER 2
A10	08170-66510	BD AY DISPLAY
A11	08170-66511	BD AY KEY
A12	NOT AVAILABLE COMPLETE, ORDER W1 AND J1-4.	
A13	08170-66513	BD AY PROM (EARLIER MODELS ONLY)
A19	08170-66519	BD AY SWITCH
A20	08170-66520	I/F CONN
A21	08170-66521	BD AY TRIGGER
A22	08170-61601	CBL AY-POWER SW
A23	08170-60203	PANEL AY-REAR
B1	3160-0209	FAN
C1	0160-4323	C-F 0.047UF 20%
DS1	2140-0352	LAMP-INCD T1-1/8V
	2110-0007	FUSE 1 AMP
	2110-0202	FUSE 250V .5A SB
J1	08170-67601	CONN AY-FRNT PNL
J2	08170-67601	CONN AY-FRNT PNL
J3	08170-67601	CONN AY-FRNT PNL
J4	08170-67601	CONN AY-FRNT PNL
J5	1250-0118	CONN BNC BLKHD
J6	1250-0118	CONN BNC BLKHD
J7	1250-0118	CONN BNC BLKHD
J8	1250-0118	CONN BNC BLKHD
J9	1250-0118	CONN BNC BLKHD
J21	1251-0198	CONN PC 12CONT
MP1	01830-23201	COUPLER SW 10-24
MP2	0370-0914	BEZEL-PB KNOB
MP3	0370-2512	KNOB CONCENTRIC
MP4	08170-00201	PANEL FRONT
MP5	08170-00202	PANEL SUB
MP6	08170-01203	BRACKET TOP
MP7	08170-04102	PLAT SIDE LH
MP8	08170-04103	PLAT SIDE RH
MP9	5000-8915	CVR XFMR OLV BLK
MP10	08170-04107	COVER HIGH VOLT
MP13	08170-28101	WINDOW
MP14	08170-60101	CHASSIS
MP15	0380-0599	SPACER
MP16	1450-0404	LENS PILOT LIGHT
MP17	00183-67701	BASE PILTLT
MP17	0400-0193	GROMMET SHOCK
MP18	1460-1345	TILT STAND
MP19	3160-0290	FINGER GUARD
MP20	5001-0439	TRIM SIDE 5.25
MP21	5001-1206	PLATE SAFETY PWR
MP22	5001-1207	INSULATOR PWR SW
MP24	5020-8803	FRAME-FRONT
MP25	5020-8804	FRAME-REAR
MP26	5020-8836	CORNER STRUT LO
MP27	5040-1124	KNOB-PBIN PUWER
MP28	5040-6010	KEY CAP 0
MP29	5040-6011	KEY CAP 1
MP30	5040-6012	KEY CAP 2
MP31	5040-6013	KEY CAP 3
MP32	5040-6014	KEY CAP 4
MP33	5040-6015	KEY CAP 5
MP34	5040-6016	KEY CAP 6
MP35	5040-6017	KEY CAP 7
MP36	5040-6018	KEY CAP 8
MP37	5040-6019	KEY CAP 9
MP39	5040-7201	FOOT
MP40	5040-7202	TRIM STRIP-TOP

REFERENCE DESIGNATOR	H-P PART NUMBER	DESCRIPTION
MP41	5040-7219	CAP,HANDLE-FRONT
MP42	5040-7220	CAP,HANDLE-REAR
MP43	5040-7221	FOOT REAR
MP44	5040-7756	EXTENDER ROD PBT
MP45	5040-9305	KEY LARGE OLVBEI
MP46	5040-9305	KEY LARGE OLVBEI
MP47	5040-9305	KEY LARGE OLVBEI
MP48	5040-9305	KEY LARGE OLVBEI
MP50	5060-9803	STRAP-HANDLE
MP51	5060-9834	COVER AY TOP
MP52	08170-64111	COVER AY-BOTTOM
MP53	5060-9856	COVER-SIDE
MP54	08170-04110	COVER SIDE HNDL
MP60	5040-9306	KEY LARGE OLVGRY
MP61	5040-9306	KEY LARGE OLVGRY
MP62	5040-9306	KEY LARGE OLVGRY
MP63	5040-9306	KEY LARGE OLVGRY
MP64	5040-9306	KEY LARGE OLVGRY
MP65	5040-9306	KEY LARGE OLVGRY
MP66	5040-9306	KEY LARGE OLVGRY
MP67	5040-9306	KEY LARGE OLVGRY
MP68	5040-9306	KEY LARGE OLVGRY
MP69	5040-9306	KEY LARGE OLVGRY
MP70	5040-9308	KEY CAP A
MP71	5040-9309	KEY CAP B
MP72	5040-9310	KEY CAP C
MP73	5040-9311	KEY CAP D
MP74	5040-9312	KEY CAP E
MP75	5040-9313	KEY CAP F
MP76	5041-0309	CAP KEY QUARTER
MP78	5041-0318	LK CAP PTV GRAY
MP79	5041-0318	LK CAP PTV GRAY
MP80	5041-0318	LK CAP PTV GRAY
MP81	5041-0318	LK CAP PTV GRAY
MP82	5041-0318	LK CAP PTV GRAY
MP83	5041-0318	LK CAP PTV GRAY
MP84	5041-0318	LK CAP PTV GRAY
MP85	5041-0318	LK CAP PTV GRAY
MP86	5041-0318	LK CAP PTV GRAY
MP87	5041-0318	LK CAP PTV GRAY
MP88	5041-0318	LK CAP PTV GRAY
MP89	5041-0318	LK CAP PTV GRAY
MP90	5041-0318	LK CAP PTV GRAY
MP91	5041-0318	LK CAP PTV GRAY
MP92	5041-0318	LK CAP PTV GRAY
MP93	5041-0318	LK CAP PTV GRAY
MP94	5041-0318	LK CAP PTV GRAY
MP95	1410-0069	BUSHING PANEL
MP96	1410-0069	BUSHING PANEL
Q1	1853-0324	XSTR PNP SI TO39
XHT1	08170-21101	HEAT SINK
R1	2100-2492	R-VAR 5K 20% .5W
R2	2100-3436	R-VAR 10K 10%
T1	08170-61101	XFMR PWR
W1	08170-67601	CONDUCTOR AY FLAT FLEX
XF1A	2110-0565	FUSE CARRIER
XF1B	2110-3566	FUSEHOLDER
XF1C	2110-0569	NUT HEX
XF1E	1400-0090	WASHER NEOPRENE

Table 6–2. Replaceable Parts (cont'd)

Assembly A1

REFERENCE DESIGNATOR		H-P PART NUMBER		DESCRIPTION
A1	C1	0160-4386		C-F 33PF 5% 200V
A1	C2	0160-4386		C-F 33PF 5% 200V
A1	C3	0160-4320		C-F 68PF 200V
A1	C4	0160-4320		C-F 68PF 200V
A1	C5	0160-4389		C-F 100PF
A1	C6	0160-4389		C-F 100PF
A1	C7	0160-3872		C-F 2200PF 100V
A1	C8	0160-3879		C-F .01UF 100V
A1	C9	0160-3879		C-F .01UF 100V
A1	C10	0160-3879		C-F .01UF 100V
A1	C11	0160-4387		C-F 47PF 200V
A1	C12	0160-4387		C-F 47PF 200V
A1	C13	0160-4387		C-F 47PF 200V
A1	C14	0160-0174		C-F .47UF 25V
A1	C15	0160-0570		C-F 220PF +-20%
A1	C16	0160-0174		C-F .47UF 25V
A1	C17	0160-0174		C-F .47UF 25V
A1	C18	0160-0174		C-F .47UF 25V
A1	C19	0160-0174		C-F .47UF 25V
A1	C20	0160-0174		C-F .47UF 25V
A1	C21	0160-0174		C-F .47UF 25V
A1	C22	0160-0174		C-F .47UF 25V
A1	C23	0160-0174		C-F .47UF 25V
A1	C24	0160-0174		C-F .47UF 25V
A1	C25	0180-1715		C-F 150UF 6V
A1	C26	0180-1715		C-F 150UF 6V
A1	C27	0180-1747		C-F 47UF 15V
A1	C28	0180-1704		C-F 47UF 6V
A1	C29	0180-1704		C-F 47UF 6V
A1	C30	0160-3879		C-F .01UF 100V
A1	C31	0160-0576		C-F .1UF 20% 50V
A1	C32	0160-0576		C-F .1UF 20% 50V
A1	C33	0160-0576		C-F .1UF 20% 50V
A1	C34	0160-0576		C-F .1UF 20% 50V
A1	C35	0160-0576		C-F .1UF 20% 50V
A1	C36	0160-3878		C-F .001UF 100V
A1	CR1	1901-1068		DIU SCHOTTKY
A1	CR2	1901-1098		DIO-SWIT-1N4150
A1	CR3	1901-1098		DIO-SWIT-1N4150
A1	CR4	1901-1098		DIO-SWIT-1N4150
A1	CR5	1901-1098		DIO-SWIT-1N4150
A1	CR6	1901-1098		DIO-SWIT-1N4150
A1	CR7	1901-1098		DIO-SWIT-1N4150
A1	CR8	1901-1068		DIU SCHOTTKY
A1	CR9	1901-1068		DIU SCHOTTKY
A1	CR10	1901-1068		DIU SCHOTTKY
A1	CR11	1901-1068		DIU SCHOTTKY
A1	CR12	1901-1068		DIU SCHOTTKY
A1	CR13	1901-1068		DIU SCHOTTKY
A1	CR14	1901-1068		DIU SCHOTTKY
A1	CR15	1901-1068	(00116)	DIU SCHOTTKY
A1	J3	1200-0588		SOCKET IC
A1	J4	1251-4215		CONN 6 PIN (QTY 4)
A1	J5	1251-4215		CONN 6 PIN (QTY 1)
A1	Q1	1853-0086		XSTR SI 2N5087
A1	Q2	1853-0086		XSTR SI 2N5087
A1	Q3	1853-0086		XSTR SI 2N5087
A1	Q4	1853-0086		XSTR SI 2N5087
A1	Q5	1853-0086		XSTR SI 2N5087
A1	Q6	1854-0633		XSTR NPN SI DARL
A1	Q7	1854-0633		XSTR NPN SI DARL
A1	Q8	1854-0633		XSTR NPN SI DARL
A1	Q9	1854-0633		XSTR NPN SI DARL
A1	Q10	1854-0633		XSTR NPN SI DARL
A1	R1	0757-0433		R-F 3.32K1%
A1	R3	0757-0283		R-F 2K1% .125W F
A1	R4	0757-0433		R-F 3.32K1%
A1	R5	0698-0082		R-F 464 1% .125W
A1	R6	0698-0082		R-F 464 1% .125W
A1	R7	0757-0280		R-F 1K1% .125W F
A1	R8	0757-0280		R-F 1K1% .125W F
A1	R9	0757-0437		R-F 4.75K1%
A1	R10	0757-0437		R-F 4.75K1%
A1	R11	0757-0385		R-F 22.1 1%

REFERENCE DESIGNATOR		H-P PART NUMBER		DESCRIPTION
A1	R12	0757-0346		R-F 10 1% .125W
A1	R13	0757-0346		R-F 10 1% .125W
A1	R14	0757-0385		R-F 22.1 1%
A1	R15	0757-0442		R-F 10K1% .125W
A1	R16	0757-0442		R-F 10K1% .125W
A1	R17	0757-0440		R-F 7.5K1% .125W
A1	R18	0698-3136		R-F 17.8K1%
A1	R19	0757-0449		R-F 20K1% .125W
A1	R20	0698-3700		R-F 715 1% .125W
A1	R21	0698-4429		R-F 1.87K1%
A1	R22	0698-4429		R-F 1.87K1%
A1	R23	0698-4453		R-F 402 1% .125W
A1	R24	0698-4453		R-F 402 1% .125W
A1	R25	0698-4453		R-F 402 1% .125W
A1	R26	0698-4453		R-F 402 1% .125W
A1	R27	0698-4453		R-F 402 1% .125W
A1	R28	0757-0280		R-F 1K1% .125W F
A1	R29	0757-0280		R-F 1K1% .125W F
A1	R30	0698-4418		R-F 205 1% .125W
A1	R31	0698-3486		R-F 442 1% .125W
A1	R32	0757-0465		R-F 100K1% .125W
A1	R33	0757-0465		R-F 100K1% .125W
A1	R34	0757-0458		R-F 51.1K1%
A1	R35	0757-0458		R-F 51.1K1%
A1	R36	0757-0458		R-F 51.1K1%
A1	R37	0757-0280		R-F 1K1% .125W F
A1	R39	0757-0465		R-F 100K1% .125W
A1	R40	0757-0465		R-F 100K1% .125W
A1	R41	0757-0280		R-F 1K1% .125W F
A1	R42	0757-0280		R-F 1K1% .125W F
A1	R43	0757-0280		R-F 1K1% .125W F
A1	R44	0757-0280		R-F 1K1% .125W F
A1	R45	0757-0280		R-F 1K1% .125W F
A1	R46	0757-0437		R-F 4.75K1%
A1	R47	0757-0453		R-F 30.1K1% .125W
A1	R48	0698-3136		R-F 17.8K1%
A1	R49	0757-0280		R-F 1K1% .125W F
A1	R50	0757-0442		R-F 10K1% .125W
A1	R51	0757-0442		R-F 10K1% .125W
A1	R52	0757-0442		R-F 10K1% .125W
A1	R53	0757-0283		R-F 2K1% .125W F
A1	R54	0757-0280		R-F 1K1% .125W F
A1	R55	0757-0280		R-F 1K1% .125W F
A1	R57	0757-0289		R-F 3.1K1%
A1	R58	0698-7253	(00116)	R-F 3.11K 1% .05
A1	R71	1810-0204		NETWORK RES SIP
A1	R72	1810-0206		NETWORK-RES SIP
A1	R91	1810-0280		R-NETWORK BLP
A1	R92	1810-0280		R-NETWORK BLP
A1	R93	1810-0280		R-NETWORK BLP
A1	R94	1810-0280		R-NETWORK BLP
A1	R101	8159-0005		WIRE 22GA W PVC
A1	R102	8159-0005		WIRE 22GA W PVC
A1	R105	8159-0005		WIRE 22GA W PVC
A1	R106	8159-0005		WIRE 22GA W PVC
A1	R107	8159-0005		WIRE 22GA W PVC
A1	R108	8159-0005	(00116)	WIRE 22GA W PVC
A1	S1	3101-2125		SW SLD 5POT
A1	S2	3101-2030		SW-TGL SPDT
A1	U7	1818-0319		IC-MEMORY CMOS
A1	U8	1818-0319		IC-MEMORY CMOS
A1	U9	1820-1481		IC-PIA
A1	U10	1820-1481		IC-PIA
A1	U11	1820-1481		IC-PIA
A1	U12	1820-1918		IC SN74LS 241N
A1	U13	1820-1918		IC SN74LS 241N
A1	U14	1820-1918		IC SN74LS 241N
A1	U15	1820-1918		IC SN74LS 241N
A1	U16	1820-1918		IC SN74LS 241N
A1	U17	1820-1918		IC SN74LS 241N
A1	U18	1820-1427		IC-SN74LS156
A1	U19	1820-1216		IC-SN74LS138
A1	U20	1820-1217		IC DUTL
A1	U21	1820-1426		IC-SN74LS145

(00116) = serial numbers 00116 and below
(00116) = serial numbers 00116 and above

Table 6–2. Replaceable Parts (cont'd)

REFERENCE DESIGNATOR		H-P PART NUMBER	DESCRIPTION
A1	U22	1820-1197	IC SN74LS00
A1	U23	1820-1197	IC SN74LS00
A1	U24	1820-1144	IC SN74LS02N
A1	U25	1820-1201	IC-SN74LS08N
A1	U26	1818-0320	MOS 1024-BIT RAM
A1	U27	1818-0320	MOS 1024-BIT RAM
A1	U28	1820-2031	IC MC 14021UPL
A1	U29	1820-1114	IC MC14516 CMOS
A1	U30	1820-1387	IC MC14519CP
A1	U31	1820-1387	IC MC14519CP
A1	U32	1820-1150	CMOS CTRMC14520CP
A1	U33	1820-1462	IC DIG 140280
A1	U34	1820-1483	IC DGIL 74L 221
A1	U35	1820-1199	IC SN74LS 04
A1	U36	1820-1965	IC MC 14025BCP
A1	U37	1820-1425	IC SN74LS132
A1	U38	1820-2014	IC 140698 HEX
A1	U39	1820-1208	IC-SN74LS32
A1	U40	1820-0068	IC-SN7407
A1	U41	1820-1633	IC DIG SN74 S240
A1	U42	1820-1196	IC SN74LS174N
A1	U43	1820-1196	IC SN74LS174N
A1	U44	1820-1451	IC SN74 S38
A1	U45	1820-1451	IC SN74 S38
A1	U46	1820-1451	IC SN74 S38
A1	U47	1820-1451	IC SN74 S38
A1	U48	1820-1211	IC-SN74LS 86N
A1	U49	1820-1480	IC-MPU
A1	U50	1820-1437	IC-SN74LS221
A1	U51	1820-1804	IC-DIGITAL 6842

Table 6–2. Replaceable Parts (cont'd)

Assembly A2

REFERENCE DESIGNATOR		H-P PART NUMBER	DESCRIPTION
A2	BT1	1420-0574	BATTERIE
A2	BT2	1420-0574	BATTERIE
A2	C1	0160-0576	C-F .1UF 20% 50V
A2	C2	0160-0174	C-F .47UF 25V
A2	C3	0180-0228	C-F 22UF 15V
A2	C4	0160-0576	C-F .1UF 20% 50V
A2	C4	0180-1704	C-F 47UF 6V
A2	C5	0160-0576	C-F .1UF 20% 50V
A2	C6	0160-0576	C-F .1UF 20% 50V
A2	C7	0160-0576	C-F .1UF 20% 50V
A2	C8	0160-0576	C-F .1UF 20% 50V
A2	C9	0160-0576	C-F .1UF 20% 50V
A2	CR3	1901-0731	DIO-PWR 400V 1A
A2	CR4	1901-1098	DIO-SWIT.1N4150
A2	CR5	1901-1098	DIO-SWIT.1N4150
A2	CR6	1901-1098	DIO-SWIT.1N4150
A2	CR7	1901-0539	DIODE-SCHOTTKY
A2	CR8	1901-1098	DIO-SWIT.1N4150
A2	L1	9100-2264	COIL MLD 6.8UH
A2	L2	9100-2264	COIL MLD 6.8UH
A2	L3	9100-2264	COIL MLD 6.8UH
A2	L4	9100-2264	COIL MLD 6.8UH
A2	L5	9100-2264	COIL MLD 6.8UH
A2	L6	9100-2264	COIL MLD 6.8UH
A2	L7	9100-2264	COIL MLD 6.8UH
A2	L8	9100-2264	COIL MLD 6.8UH
A2	L9	9100-2264	COIL MLD 6.8UH
A2	L10	9100-2264	COIL MLD 6.8UH
A2	L11	9100-2264	COIL MLD 6.8UH
A2	L12	9100-2264	COIL MLD 6.8UH
A2	L13	9100-2264	COIL MLD 6.8UH
A2	L14	9100-2264	COIL MLD 6.8UH
A2	L15	9100-2264	COIL MLD 6.8UH
A2	L16	9100-2264	COIL MLD 6.8UH
A2	MP1	4040-0750	PC EXTR BD RED
A2	MP3	1205-0011	HT-SINK XSTR
A2	Q1	1854-0637	XSTR SI 2219A
A2	Q2	1853-0086	XSTR SI 2N5087
A2	Q3	1853-0036	XSTR SI 2N3906
A2	Q4	1853-0036	XSTR SI 2N3906
A2	Q5	1853-0036	XSTR SI 2N3906
A2	Q6	1854-0477	XSTR NPN 2N2222A
A2	Q7	1854-0477	XSTR NPN 2N2222A
A2	R4	0811-3069	R-F 1 OHM 5%
A2	R5	0757-0417	R-F 562 1% .125W
A2	R6	0757-0291	R-F 24.9 1%
A2	R7	0757-0401	R-F 100 1% .125W
A2	R8	0757-0438	R-F 5.11K1%
A2	R9	0757-0439	R-F 6.81K1%
A2	R10	0698-3488	R-F 442 1% .125W
A2	R11	0698-3488	R-F 442 1% .125W
A2	R12	0698-4458	R-F 590 1% .125W
A2	R13	0757-0280	R-F 1K1% .125W F
A2	R14	0757-0438	R-F 5.11K1%
A2	R15	0757-0465	R-F 100K1% .125W
A2	R16	0757-0280	R-F 1K1% .125W F
A2	R17	0757-0280	R-F 1K1% .125W F
A2	R18	0757-0280	R-F 1K1% .125W F
A2	R19	0757-0453	R-F 30.1K1% .125W
A2	R20	0757-0453	R-F 30.1K1% .125W
A2	R21	0757-0280	R-F 1K1% .125W F
A2	R22	0757-0280	R-F 1K1% .125W F
A2	R24	0698-7212	R-F 100 1% .05W
A2	R25	0698-7212	R-F 100 1% .05W
A2	R26	0698-7212	R-F 100 1% .05W
A2	R27	0698-7212	R-F 100 1% .05W
A2	R28	0698-7212	R-F 100 1% .05W
A2	R29	0698-7212	R-F 100 1% .05W
A2	R30	0698-7212	R-F 100 1% .05W
A2	R31	0698-7212	R-F 100 1% .05W
A2	R32	0698-7212	R-F 100 1% .05W
A2	R33	0698-7212	R-F 100 1% .05W
A2	R34	0698-7212	R-F 100 1% .05W

REFERENCE DESIGNATOR		H-P PART NUMBER	DESCRIPTION
A2	R35	0698-7212	R-F 100 1% .05W
A2	R36	0698-7212	R-F 100 1% .05W
A2	R37	0698-7212	R-F 100 1% .05W
A2	R38	0698-7212	R-F 100 1% .05W
A2	R39	0698-7212	R-F 100 1% .05W
A2	RT23	0837-0050	THMS 1K DIS
A2	U1	1820-1491	IC-SN74LS367N
A2	U2	1820-1491	IC-SN74LS367N
A2	U3	1820-1491	IC-SN74LS367N
A2	U4	1820-1491	IC-SN74LS367N
A2	U5	1820-1216	IC-SN74LS138
A2	U6	1820-2053	IC DM74LS154N
A2	U7	1820-1216	IC-SN74LS138
A2	U8	1820-1491	IC-SN74LS367N
A2	U9	1820-1491	IC-SN74LS367N
A2	U10	1820-0605	IC-SN74S10N
A2	U11	1820-1130	IC SN745 133 N
A2	U12	1820-1211	IC-SN74LS 86N
A2	U13	1820-1211	IC-SN74LS 86N
A2	U14	1820-1211	IC-SN74LS 86N
A2	U15	1820-1211	IC-SN74LS 86N
A2	U16	1820-1997	IC SN74LS374CP
A2	U17	1820-1997	IC SN74LS374CP
A2	U21	1818-0695	IC-MEM CMOS 5101
A2	U22	1818-0695	IC-MEM CMOS 5101
A2	U23	1818-0695	IC-MEM CMOS 5101
A2	U24	1818-0695	IC-MEM CMOS 5101
A2	U25	1818-0695	IC-MEM CMOS 5101
A2	U26	1818-0695	IC-MEM CMOS 5101
A2	U27	1818-0695	IC-MEM CMOS 5101
A2	U28	1818-0695	IC-MEM CMOS 5101
A2	U29	1820-1491	IC-SN74LS367N
A2	U30	1820-1491	IC-SN74LS367N
A2	U31	1820-1425	IC SN74LS132
A2	VR1	1902-0048	DIO 6.81V 5% .4W

Assembly A3 (Option 001 only)

REFERENCE DESIGNATOR		H-P PART NUMBER	DESCRIPTION
A3	C1	0160-3576	C-F .1UF 20% 50V
A3	C2	0160-0576	C-F .1UF 20% 50V
A3	C3	0160-3576	C-F .1UF 20% 50V
A3	C4	0160-0576	C-F .1UF 20% 50V
A3	C5	0160-3576	C-F .1UF 20% 50V
A3	U1	1818-0695	IC-MEM CMOS 5101
A3	U2	1818-0695	IC-MEM CMOS 5101
A3	U3	1818-0695	IC-MEM CMOS 5101
A3	U4	1818-0695	IC-MEM CMOS 5101
A3	U5	1818-3695	IC-MEM CMOS 5101
A3	U6	1818-0695	IC-MEM CMOS 5101
A3	U7	1818-0695	IC-MEM CMOS 5101
A3	U8	1818-0695	IC-MEM CMOS 5101
A3	U9	1818-0695	IC-MEM CMOS 5101
A3	U10	1818-0695	IC-MEM CMOS 5101
A3	U11	1818-0695	IC-MEM CMOS 5101
A3	U12	1818-0695	IC-MEM CMOS 5101
A3	U13	1818-3695	IC-MEM CMOS 5101
A3	U14	1818-0695	IC-MEM CMOS 5101
A3	U15	1818-3695	IC-MEM CMOS 5101
A3	U16	1818-0695	IC-MEM CMOS 5101
A3	U17	1818-3695	IC-MEM CMOS 5101
A3	U18	1818-0695	IC-MEM CMOS 5101
A3	U19	1818-0695	IC-MEM CMOS 5101
A3	U20	1818-3695	IC-MEM CMOS 5101
A3	U21	1818-0695	IC-MEM CMOS 5101
A3	U22	1818-3695	IC-MEM CMOS 5101
A3	U23	1818-0695	IC-MEM CMOS 5101
A3	U24	1818-3695	IC-MEM CMOS 5101

Table 6-2. Replaceable Parts (cont'd)

Assembly A4

REFERENCE DESIGNATOR		H-P PART NUMBER	DESCRIPTION
A4	C1	0160-0576	C-F .1UF 20% 50V
A4	C2	0160-0576	C-F .1UF 20% 50V
A4	C3	0160-0576	C-F .1UF 20% 50V
A4	C4	0160-0576	C-F .1UF 20% 50V
A4	C5	0160-0576	C-F .1UF 20% 50V
A4	C6	0160-0576	C-F .1UF 20% 50V
A4	C7	0160-3793	C-F 680PF 100V
A4	C8	0180-2690	C-F 3.3UF 15V
A4	C9	0160-0576	C-F .1UF 20% 50V
A4	C10	0180-0374	C-F 10UF 20V
A4	C11	0160-2204	C-F 100PF 300V
A4	C13	0180-3197	C-F 2.2UF 20V
A4	C14	0160-0573	C-F 4700 PF 20%
A4	C15	0160-3878	C-F .001UF 100V
A4	C16	0160-3878	C-F .001UF 100V
A4	C17	0160-3878	C-F .001UF 100V
A4	C18	0160-3878	C-F .001UF 100V
A4	C19	0160-3878	C-F .001UF 100V
A4	C20	0160-3878	C-F .001UF 100V
A4	C21	0160-3878	C-F .001UF 100V
A4	C22	0160-3878	C-F .001UF 100V
A4	C23	0160-3878	C-F .001UF 100V
A4	C24	0160-3878	C-F .001UF 100V
A4	C25	0160-3878	C-F .001UF 100V
A4	C26	0160-3878	C-F .001UF 100V
A4	C27	0160-0197	C-F 2.2UF 20V
A4	C28	0180-1714	C-F 330UF 6V
A4	C29	0160-0573	C-F 4700 PF 20%
A4	C30	0180-0374	C-F 10UF 20V
A4	C31	0180-0374	C-F 10UF 20V
A4	C32	0160-0576	C-F .1UF 20% 50V
A4	CR1	1901-0539	DIODE-SCHOTTKY
A4	CR2	1901-0539	DIODE-SCHOTTKY
A4	CR3	1901-1098	DIO-SWIT.1N4150
A4	MP1	4040-0752	PC EXTR BD YEL
A4	MP6	1460-0579	WIREFORM
A4	MP7	1460-0579	WIREFORM
A4	Q1	1854-0392	XSTR ST 2N 5088
A4	Q2	1853-0036	XSTR ST 2N3906
A4	Q3	1853-0036	XSTR ST 2N3906
A4	Q4	1853-0281	XSTR ST 2907A
A4	Q50	1858-0021	XSTR ARRAY
A4	R1	0757-0428	R-F 1.62K1%
A4	R2	0757-0428	R-F 1.62K1%
A4	R3	0757-0428	R-F 1.62K1%
A4	R4	0757-0407	R-F 200 1% .125W
A4	R5	0757-0411	R-F 332 1% .125W
A4	R7	0698-3431	R-F 23.7 1%
A4	R10	0757-0422	R-F 909 1% .125W
A4	R11	0757-0422	R-F 909 1% .125W
A4	R12	0757-0422	R-F 909 1% .125W
A4	R13	0757-0394	R-F 51.1 1%
A4	R14	0757-0407	R-F 200 1% .125W
A4	R15	2100-3351	R-VAR 500 10%
A4	R16	0757-0437	R-F 4.75K1%
A4	R17	2100-3351	R-VAR 500 10%
A4	R18	0698-4460	R-F 649 1% .125W
A4	R19	0698-4460	R-F 649 1% .125W
A4	R20	0757-0280	R-F 1K1% .125W F
A4	R21	0698-7229	R-F 511 1% .05W
A4	R22	0757-0438	R-F 5.11K1%
A4	R23	0698-7249	R-F 3.48K 1%.05
A4	R24	0698-7260	R-F 10K 1% .05W
A4	R25	0698-7212	R-F 100 1% .05W
A4	R26	0698-7212	R-F 100 1% .05W
A4	R27	0698-7212	R-F 100 1% .05W
A4	R28	0698-7212	R-F 100 1% .05W
A4	R29	0698-7212	R-F 100 1% .05W
A4	R30	0698-7212	R-F 100 1% .05W
A4	R31	0698-7212	R-F 100 1% .05W
A4	R32	0698-7212	R-F 100 1% .05W
A4	R33	0698-7212	R-F 100 1% .05W
A4	R34	0698-7212	R-F 100 1% .05W
A4	R35	0698-7212	R-F 100 1% .05W
A4	R36	0698-7212	R-F 100 1% .05W
A4	R37	0757-0437	R-F 4.75K1%

REFERENCE DESIGNATOR		H-P PART NUMBER	DESCRIPTION
A4	U1	1820-2078	IC SN74LS490N
A4	U2	1820-2078	IC SN74LS490N
A4	U3	1820-1216	IC-SN74LS138
A4	U4	1820-1225	IC SN74LS132
A4	U5	1820-1212	IC SN74LS112
A4	U6	1820-1568	IC SN74LS125N
A4	U7	1820-1568	IC SN74LS125N
A4	U8	1820-1199	IC SN74LS 04
A4	U9	1820-1202	IC DGTL SN74LS10
A4	U10	1820-1195	IC 74LS175
A4	U11	1820-1195	IC 74LS175
A4	U12	1820-1195	IC 74LS175
A4	U13	1820-1195	IC 74LS175
A4	U14	1820-1195	IC 74LS175
A4	U15	1820-1195	IC 74LS175
A4	U16	1820-1211	IC-SN74LS 86N
A4	U17	1820-1211	IC-SN74LS 86N
A4	U18	1820-1211	IC-SN74LS 86N
A4	U19	1820-1211	IC-SN74LS 86N
A4	U20	1820-1211	IC-SN74LS 86N
A4	U21	1820-1211	IC-SN74LS 86N
A4	U22	1820-1641	IC 74LS365N
A4	U23	1820-1641	IC 74LS365N
A4	U24	1820-1641	IC 74LS365N
A4	U25	1820-1641	IC 74LS365N
A4	U26	1820-1130	IC SN745 133 N
A4	U27	1820-1130	IC SN745 133 N
A4	U28	1820-1130	TTL UCTFF74LS273
A4	U29	1820-1216	IC-SN74LS138
A4	U30	1820-1208	IC-SN74LS32
A4	U31	1820-1144	IC SN74LS02N
A4	U32	1820-1196	IC SN74LS174N
A4	U33	1820-1196	IC SN74LS174N
A4	U34	1820-1641	IC 74LS365N
A4	U35	1820-1641	IC 74LS365N
A4	U36	1820-1641	IC 74LS365N
A4	U37	1820-1641	IC 74LS365N
A4	U38	1820-1278	IC 74LS 191
A4	U39	1820-1278	IC 74LS 191
A4	U40	1820-1278	IC 74LS 191
A4	U41	1820-1492	IC-SN74LS 368N
A4	U41	1820-1641	IC 74LS365N
A4	U42	1820-1492	IC-SN74LS 368N
A4	U43	1820-1641	IC 74LS365N
A4	U44	1820-1208	IC-SN74LS32
A4	U45	1820-1423	TTL SN74LS123N
A4	U46	1820-1197	IC SN74LS00
A4	U47	1820-1297	IC DGTL 74LS266N
A4	U48	1820-1297	IC DGTL 74LS266N
A4	U49	1820-1297	IC DGTL 74LS266N
A4	U51	1820-1441	IC 74LS283
A4	U52	1820-1441	IC 74LS283
A4	U53	1820-1441	IC 74LS283
A4	U54	1820-1997	IC SN74LS374CP
A4	U55	1820-1997	IC SN74LS374CP
A4	U56	1820-1470	IC SN74LS157
A4	U57	1820-1217	IC DGTL

Table 6-2. Replaceable Parts (cont'd)

Assembly A5

REFERENCE DESIGNATOR		H-P PART NUMBER	DESCRIPTION
A5	C1	0160-0174	C-F .47UF 25V
A5	C2	0160-0174	C-F .47UF 25V
A5	C3	0160-0174	C-F .47UF 25V
A5	C4	0160-0174	C-F .47UF 25V
A5	C5	0180-1746	C-F 15UF 20V
A5	C6	0180-1746	C-F 15UF 20V
A5	C7	0160-4031	C-F 330PF
A5	C8	0160-4031	C-F 330PF
A5	C9	0160-4031	C-F 330PF
A5	C10	0180-3291	C-F 1UF 35V
A5	C11	0160-0174	C-F .47UF 25V
A5	C12	0160-0174	C-F .47UF 25V
A5	C13	0160-0174	C-F .47UF 25V
A5	C14	0180-1714	C-F 330UF 6V
A5	C15	0160-3879	C-F .01UF 100V
A5	C16	0160-3879	C-F .01UF 100V
A5	C17	0160-3879	C-F .01UF 100V
A5	CR1	1901-0731	DIO-PWR 400V 1A
A5	CR2	1901-0731	DIO-PWR 400V 1A
A5	MP4	1460-0579	WIREFORM
A5	MP4	4040-0753	PC EXTR BD GRN
A5	MP5	1460-0579	WIREFORM
A5	R1	1810-0136	R-SETB-3K,8-0.2K
A5	R2	1810-0136	R-SETB-3K,8-0.2K
A5	R3	1810-0205	R-NETWORK 4.7K
A5	R4	0757-0442	R-F 10K1% .125W
A5	R5	0683-1565	R-F 15M 5% .174W
A5	R6	0757-0442	R-F 10K1% .125W
A5	R7	0757-0442	R-F 10K1% .125W
A5	R8	0757-0442	R-F 10K1% .125W
A5	R9	8159-0005	WIRE 22GA N FVL
A5	R10	0757-0452	R-F 27.4K1%
A5	R11	0698-3279	R-F 4.99K1%
A5	R12	0698-3279	R-F 4.99K1%
A5	U1	1820-1481	IC-PIA
A5	U2	1820-1481	IC-PIA
A5	U3	1820-1918	IC SN74LS 241N
A5	U4	1820-1624	IC-SN74S241N
A5	U5	1820-1451	IC SN74 538
A5	U6	1820-1197	IC SN74LS00
A5	U7	1820-1197	IC SN74LS00
A5	U8	1820-1416	TTL SN74LS14N
A5	U9	1820-1690	IC MC6850
A5	U10	1820-1779	BIT RATE GEN
A5	U11	1820-0509	IC DGTL-MC1488L
A5	U12	1820-0990	IC MC 1489 AL
A5	U13	1820-1217	IC DGTL
A5	U14	1820-1202	IC DGTL SN74LS10
A5	U15	1820-1568	IC SN74LS125N
A5	Y1	0410-1304	XTAL

Assembly A6

REFERENCE DESIGNATOR		H-P PART NUMBER	DESCRIPTION
A6	C1	0160-3877	C-F 100PF 200V
A6	C2	0160-4386	C-F 33PF 5% 200V
A6	C3	0160-4386	C-F 33PF 5% 200V
A6	C4	0160-0571	C-F 470 PF
A6	C5	0160-0571	C-F 470 PF
A6	C6	0160-0570	C-F 220PF +-20%
A6	C7	0160-3877	C-F 100PF 200V
A6	C8	0160-0573	C-F 4700 PF 20%
A6	C9	0180-0374	C-F 10UF 20V
A6	C10	0160-2204	C-F 100PF 300V
A6	C11	0160-0570	C-F 220PF +-20%
A6	C12	0160-0570	C-F 220PF +-20%
A6	C13	0160-2204	C-F 100PF 300V
A6	C14	0160-0576	C-F .1UF 20% 50V
A6	C15	0160-0576	C-F .1UF 20% 50V
A6	C16	0160-0576	C-F .1UF 20% 50V
A6	C17	0160-0576	C-F .1UF 20% 50V
A6	C18	0160-0576	C-F .1UF 20% 50V
A6	C19	0160-3877	C-F 100PF 200V
A6	C21	0160-0571	C-F 470 PF
A6	L22	0140-0196	C-F 150PF 300V
A6	L24	0160-0570	C-F 220PF +-20%
A6	MP1	4040-0754	PC EXTR BD BLU
A6	CR1	1901-0636	DIO SHOTTKY
A6	Q1	1854-0477	XSTR NPN 2N2222A
A6	R1	0757-0416	R-F 511 1% .125W
A6	R2	0757-0280	R-F 1K1% .125W F
A6	R3	0757-0280	R-F 1K1% .125W F
A6	R4	0757-0283	R-F 2K1% .125W F
A6	R5	0757-0438	R-F 5.11K1%
A6	R6	0757-0280	R-F 1K1% .125W F
A6	R7	0757-0283	R-F 2K1% .125W F
A6	R8	0757-0416	R-F 511 1% .125W
A6	R9	0757-0283	R-F 2K1% .125W F
A6	R10	0757-0416	R-F 511 1% .125W
A6	R11	0757-0416	R-F 511 1% .125W
A6	R13	0757-0438	R-F 5.11K1%
A6	R14	0757-0401	R-F 100 1% .125W
A6	R15	0757-0283	R-F 2K1% .125W F
A6	R16	0757-0407	R-F 200 1% .125W
A6	R17	0757-0407	R-F 200 1% .125W
A6	R18	0757-0407	R-F 200 1% .125W
A6	R27	0757-0394	R-F 51.1 1%
A6	U1	1820-1199	IC SN74LS 04
A6	U2	1820-1201	IC-SN74LS08N
A6	U3	1820-1112	IC DGTL SN74LS74
A6	U4	1820-1112	IC DGTL SN74LS74
A6	U5	1820-1208	IC-SN74LS32
A6	U6	1820-1199	IC SN74LS 04
A6	U7	1820-0693	IC SN74S74N TTL
A6	U8	1820-1201	IC-SN74LS08N
A6	U9	1820-1112	IC DGTL SN74LS74
A6	U10	1820-1112	IC DGTL SN74LS74
A6	U11	1820-1199	IC SN74LS 04
A6	U12	1820-1199	IC SN74LS 04
A6	U13	1820-1201	IC-SN74LS08N
A6	U14	1820-1197	IC SN74LS00
A6	U15	1820-1206	IC SN74LS 27N
A6	U16	1820-1194	IC SN74LS02N
A6	U17	1820-1208	IC-SN74LS32
A6	U18	1820-1201	IC-SN74LS08N
A6	U19	1820-1367	IC SN 74S38
A6	U20	1820-1211	IC-SN74LS 86N
A6	U21	1820-1112	IC DGTL SN74LS74
A6	U22	1820-1437	IC-SN74LS221
A6	U23	1820-1204	IC 2A4 INP NAND
A6	U24	1820-1199	IC SN74LS 04
A6	U25	1820-1437	IC-SN74LS221
A6	U26	1820-1568	IC SN74LS125N
A6	U27	1820-1144	IC SN74LS02N
A6	U28	1820-1196	IC SN74LS174N
A6	U29	1820-1196	IC SN74LS174N
A6	U30	1820-1568	IC SN74LS125N
A6	U31	1820-1437	IC-SN74LS221
A6	U32	1820-1568	IC SN74LS125N

Table 6-2. Replaceable Parts (cont'd)

Assembly A7

REFERENCE DESIGNATOR		H-P PART NUMBER	DESCRIPTION
A7	C1	0180-2093	C-F 8000UF 15V
A7	C2	0180-2635	CF 1000UF 35WVDC
A7	C3	0180-0374	C-F 10UF 20V
A7	C4	0160-2055	C-F .01UF 100V
A7	C6	0180-2207	C-F 100UF 10V
A7	C7	0160-3878	C-F .001UF 100V
A7	C8	0180-0291	C-F 1UF 35V
A7	C9	0180-0291	C-F 1UF 35V
A7	C10	0180-2635	CF 1000UF 35WVDC
A7	C11	0180-2635	CF 1000UF 35WVDC
A7	C12	0160-3174	C-F .47UF 25V
A7	C13	0160-0174	C-F .47UF 25V
A7	C14	0180-0291	C-F 1UF 35V
A7	C15	0180-0291	C-F 1UF 35V
A7	C16	0180-2635	CF 1000UF 35WVDC
A7	C17	0180-0374	C-F 10UF 20V
A7	C18	0180-0374	C-F 10UF 20V
A7	C19	0160-3878	C-F .001UF 100V
A7	C20	0180-0291	C-F 1UF 35V
A7	C21	0180-0374	C-F 10UF 20V
A7	C22	0160-3878	C-F .001UF 100V
A7	C23	0180-0291	C-F 1UF 35V
A7	C24	0180-0291	C-F 1UF 35V
A7	C25	0180-0291	C-F 1UF 35V
A7	C26	0160-2055	C-F .01UF 100V
A7	C31	0180-2093	C-F 8000UF 15V
A7	CR2	1901-0731	DIU-PWR 400V 1A
A7	CR3	1901-0731	DIO-PWR 400V 1A
A7	CR4	1901-0731	DIU-PWR 400V 1A
A7	CR5	1901-0731	DIU-PWR 400V 1A
A7	CR6	1901-0365	DIO SI ASSY 100V
A7	CR7	1901-1098	DIU-SWIT-1N4150
A7	CR9	1901-1098	DIU-SWIT-1N4150
A7	CR10	1901-1098	DIO-SWIT-1N4150
A7	F1	2110-0342	FUSE 8 FER
A7	MP1	1205-0309	HEAT SK-60388-FT
A7	MP1	4040-0755	PC EXTR BD VIO
A7	MP2	0360-0235	TERM-TEST POINT
A7	MP2	4040-0755	PC EXTR BD VIO
A7	U1	1853-0409	XSTR PNP SI
A7	U3	1854-0456	XSTR NPN SI
A7	R1	0812-0086	R-F 5.5K 3W PW
A7	R2	0698-3242	R-F 357 1% .125W
A7	R3	2100-3351	R-VAR 500 10%
A7	R4	0757-0276	R-F 1.78K1%
A7	R5	0757-0283	R-F 2K1% .125W F
A7	R6	0757-0283	R-F 2K1% .125W F
A7	R7	0757-0283	R-F 2K1% .125W F
A7	R8	0757-0178	R-F 100 1% .25W
A7	R9	0698-3445	R-F 1.54K1%
A7	R10	0757-0472	R-F 200K1% .125W
A7	R11	0757-0453	R-F 30.1K1% .125W
A7	R12	0757-0992	R-F 22.1 1% .5W
A7	R13	0757-0992	R-F 22.1 1% .5W
A7	R14	2100-3352	R-VAR 1K .5W
A7	R15	0698-3134	R-F 4.22K1%
A7	R16	0757-0274	R-F 1.21K1%
A7	R16	2100-3351	R-VAR 20K .5W
A7	R17	2100-3351	R-VAR 500 10%
A7	R18	0698-4421	R-F 249 1% .125W
A7	R19	0757-0280	R-F 1K1% .125W F
A7	R20	0757-0280	R-F 1K1% .125W F
A7	R21	2100-3351	R-VAR 500 10%
A7	R22	0757-0280	R-F 1K1% .125W F
A7	R23	0757-0433	R-F 3.32K1%
A7	R24	0698-3499	R-F 40.2K1%
A7	R25	0757-0453	R-F 30.1K1% .125W
A7	R26	0698-4428	R-F 1.69K1%
A7	R27	0698-7521	R-F 5.11 5% 1/4W
A7	R28	0698-4428	R-F 1.69K1%
A7	R29	0757-0280	R-F 1K1% .125W F
A7	R30	0757-0442	R-F 10K1% .125W
A7	R31	0757-0442	R-F 10K1% .125W
A7	R32	0757-0442	R-F 10K1% .125W
A7	R33	0757-0442	R-F 10K1% .125W

REFERENCE DESIGNATOR		H-P PART NUMBER	DESCRIPTION
A7	R34	0757-0442	R-F 10K1% .125W
A7	R35	0757-0449	R-F 20K1% .125W
A7	R36	0757-0338	R-F 1K1% .25W F
A7	R37	0698-3155	R-F 9.09K1%
A7	R38	0757-0453	R-F 30.1K1% .125W
A7	R39	0757-0280	R-F 1K1% .125W F
A7	R40	2100-3354	R-VAR 50K 10%
A7	R41	0698-7521	R-F 5.11 5% 1/4W
A7	R42	0757-0280	R-F 1K1% .125W F
A7	R43	0698-3358	R-F 4.02K1%
A7	R44	0757-0407	R-F 200 1% .125W
A7	R45	0757-0283	R-F 2K1% .125W F
A7	R46	0757-0178	R-F 100 1% .25W
A7	R47	0757-0280	R-F 1K1% .125W F
A7	U1	1820-1202	IC SN74LS 38 N
A7	U2	1820-1958	IC 14D108 ANAL
A7	U3	1820-0049	IC V RGLTR
A7	U4	1826-0147	IC V RGLTR
A7	U5	1826-0221	IC V-RGLTR 7912C
A7	U6	1826-0043	IC LM307H
A7	U7	1826-0049	IC V RGLTR
A7	U8	1826-0393	IC-LINEAR LM317T
A7	U9	1826-0049	IC V RGLTR
A7	U10	1826-0122	IC LM340-15
A7	VR9	1902-3209	DIU 15.4V 2% .4W
A7	VR10	1902-0522	DIU 6V 5% 5W
A7	VR12	1902-3139	DIO 8.25V 5% .4W

Table 6–2. Replaceable Parts (cont'd)

Assembly A8

REFERENCE DESIGNATOR		H-P PART NUMBER	DESCRIPTION
A8	J1	1251-2915	CONNPC50 (2X25)
A8	J2	1251-2915	CONNPC50 (2X25)
A8	J3	1251-2915	CONNPC50 (2X25)
A8	J4	1251-2915	CONNPC50 (2X25)
A8	J5	1251-2915	CONNPC50 (2X25)
A8	J6	1200-0588	SOCKET IC
A8	J7	1251-2915	CONNPC50 (2X25)
A8	J8	1251-3004	CONNECTOR
A8	J9	1251-3712	CONN-POST 15F

Assembly A9

REFERENCE DESIGNATOR		H-P PART NUMBER	DESCRIPTION
A9	CR1	1906-0093	DIO BRDG 100V35A
A9	J1	1251-2915	CONNPC50 (2X25)
A9	J2	1251-2915	CONNPC50 (2X25)
A9	J3	1251-2915	CONNPC50 (2X25)
A9	J4	1251-2915	CONNPC50 (2X25)
A9	J5	1200-0588	SOCKET IC
A9	J6	1251-2915	CONNPC50 (2X25)
A9	J7	1251-2915	CONNPC50 (2X25)
A9	J8	1251-3246	CONN 3-PIN F
A9	J9	1251-3365	CONN-PC EDGE
A9	J10	1251-3365	CONN-PC EDGE
A9	J11	1251-3365	CONN-PC EDGE
A9	J12	1251-3365	CONN-PC EDGE
A9	J13	1251-3600	PIN, CONNECTOR
A9	J14	1251-3600	PIN, CONNECTOR
A9	R1	0811-1826	R-WW 05 10E 3W

Assembly A11

REFERENCE DESIGNATOR		H-P PART NUMBER	DESCRIPTION
A11	J1	1251-1929	CONN PC 12CONT
A11	J2	1200-0588	SOCKET IC

Assembly A10

REFERENCE DESIGNATOR		H-P PART NUMBER	DESCRIPTION
A10	DS1	1990-0553	DISPLAY-AN .15-H
A10	DS2	1990-0553	DISPLAY-AN .15-H
A10	DS3	1990-0553	DISPLAY-AN .15-H
A10	DS4	1990-0487	LED YEL MIN;DIUD
A10	DS5	1990-0487	LED YEL MIN;DIUD
A10	DS6	1990-0487	LED YEL MIN;DIUD
A10	DS7	1990-0487	LED YEL MIN;DIUD
A10	DS8	1990-0487	LED YEL MIN;DIUD
A10	DS9	1990-0487	LED YEL MIN;DIUD
A10	DS10	1990-0487	LED YEL MIN;DIUD
A10	DS11	1990-0487	LED YEL MIN;DIUD
A10	DS12	1990-0487	LED YEL MIN;DIUD
A10	DS13	1990-0487	LED YEL MIN;DIUD
A10	DS14	1990-0487	LED YEL MIN;DIUD
A10	DS15	1990-0487	LED YEL MIN;DIUD
A10	DS16	1990-0487	LED YEL MIN;DIUD
A10	DS17	1990-0487	LED YEL MIN;DIUD
A10	DS18	1990-0487	LED YEL MIN;DIUD
A10	DS19	1990-0487	LED YEL MIN;DIUD
A10	DS20	1990-0487	LED YEL MIN;DIUD
A10	DS21	2140-0016	LAMP INCD 5V.06A
A10	DS22	2140-0016	LAMP INCD 5V.06A
A10	DS23	2140-0016	LAMP INCD 5V.06A
A10	DS24	2140-0016	LAMP INCD 5V.06A
A10	DS25	2140-0016	LAMP INCD 5V.06A
A10	DS26	2140-0016	LAMP INCD 5V.06A
A10	DS27	2140-0016	LAMP INCD 5V.06A
A10	DS28	2140-0016	LAMP INCD 5V.06A
A10	DS29	2140-0016	LAMP INCD 5V.06A
A10	DS30	2140-0016	LAMP INCD 5V.06A
A10	DS31	2140-0016	LAMP INCD 5V.06A
A10	DS32	2140-0016	LAMP INCD 5V.06A
A10	DS33	2140-0016	LAMP INCD 5V.06A
A10	DS34	2140-0016	LAMP INCD 5V.06A
A10	J1	1251-1365	CONN PC 44CONT R
A10	J2	1200-0424	SKT IC 14-CON
A10	J3	1200-0424	SKT IC 14-CON
A10	J4	1200-0424	SKT IC 14-CON
A10	R1	0757-0384	R-F 20 1% .125W
A10	R2	0757-0384	R-F 20 1% .125W
A10	R3	0757-0384	R-F 20 1% .125W
A10	R4	0757-0384	R-F 20 1% .125W
A10	R5	0757-0384	R-F 20 1% .125W
A10	R6	0757-0384	R-F 20 1% .125W
A10	R7	0757-0384	R-F 20 1% .125W
A10	R8	0757-0274	R-F 1.21K1%
A10	R9	0757-0260	R-F 1K1% .125W F
A10	R10	0757-0438	R-F 5.11K1%
A10	S1	5060-9436	SW P-BTN SINGLE
A10	S2	5060-9436	SW P-BTN SINGLE
A10	S3	5060-9436	SW P-BTN SINGLE
A10	S4	5060-9436	SW P-BTN SINGLE
A10	S5	5060-9436	SW P-BTN SINGLE
A10	S6	5060-9436	SW P-BTN SINGLE
A10	S7	5060-9436	SW P-BTN SINGLE
A10	S8	5060-9436	SW P-BTN SINGLE
A10	S9	5060-9436	SW P-BTN SINGLE
A10	S10	5060-9436	SW P-BTN SINGLE
A10	S11	5060-9436	SW P-BTN SINGLE
A10	S12	5060-9436	SW P-BTN SINGLE
A10	S13	5060-9436	SW P-BTN SINGLE
A10	S14	5060-9436	SW P-BTN SINGLE
A10	S15	5060-9436	SW P-BTN SINGLE
A10	S16	5060-9436	SW P-BTN SINGLE
A10	S17	5060-9436	SW P-BTN SINGLE
A10	S18	5060-9436	SW P-BTN SINGLE
A10	VR1	1902-3070	DIO 4.22V 5% .4W

Table 6-2. Replaceable Parts (cont'd)

Assembly A19

REFERENCE DESIGNATOR		H-P PART NUMBER	DESCRIPTION
A19	C1	0160-3874	C-F 10PF 200V
A19	C1	0160-4386	C-F 33PF 5% 200V
A19	C2	0160-3874	C-F 10PF 200V
A19	C2	0160-4386	C-F 33PF 5% 200V
A19	C3	0160-0576	C-F .1UF 20% 50V
A19	C4	0160-0576	C-F .1UF 20% 50V
A19	C5	0160-0576	C-F .1UF 20% 50V
A19	C6	0160-0576	C-F .1UF 20% 50V
A19	CR1	1901-1098	DIO-SWIT:1N4150
A19	CR2	1901-1098	DIO-SWIT:1N4150
A19	J1	1250-1163	CONN RF BNC
A19	J2	1250-1163	CONN RF BNC
A19	J3	1250-1163	CONN RF BNC
A19	MP12	2190-0084	WASH-LOCK INT1/4
A19	Q1	1854-0215	XSTR SI 2N3904
A19	Q2	1854-0215	XSTR SI 2N3904
A19	R1	0757-0458	R-F 51.1K1%
A19	R2	0757-0458	R-F 51.1K1%
A19	R3	0757-0442	R-F 10K1% .125W
A19	R4	0757-0442	R-F 10K1% .125W
A19	R5	0757-0280	R-F 1K1% .125W F
A19	R6	0757-0280	R-F 1K1% .125W F
A19	R7	0757-0437	R-F 4.75K1%
A19	R8	0757-0437	R-F 4.75K1%
A19	R9	0698-4454	R-F 523 1%
A19	R10	0698-7212	R-F 100 1% .05W
A19	R12	2100-2488	R-VAR 10K
A19	R11	0698-7212	R-F 100 1% .05W
A19	R13	0698-4454	R-F 523
A19	S1	3101-1598	SW SLIDE DP3T
A19	S2	3101-1598	SW SLIDE DP3T
A19	S3	3101-1598	SW SLIDE DP3T
A19	S4	3101-1598	SW SLIDE DP3T
A19	S5	3101-1596	SW SLIDE DPDT
A19	S6	3101-1596	SW SLIDE DPDT
A19	S7	3101-1596	SW SLIDE DPDT
A19	U1	1820-1624	IC SN 74S241
A19	U2	1820-1297	IC DGTL 74LS266N

Assembly A20

REFERENCE DESIGNATOR		H-P PART NUMBER	DESCRIPTION
A20	J1	1251-4040	CONN 24F MCR RIB
A20	J2	1251-3504	CONNECTOR
A20	J3	1251-4946	CONN 25CONT DIP
A20	S1	3101-2158	SW-SL .1A
A20	S2	3101-2158	SW-SL .1A
A20	S3	3100-3440	SW ROT BCD CODED

Assembly A21

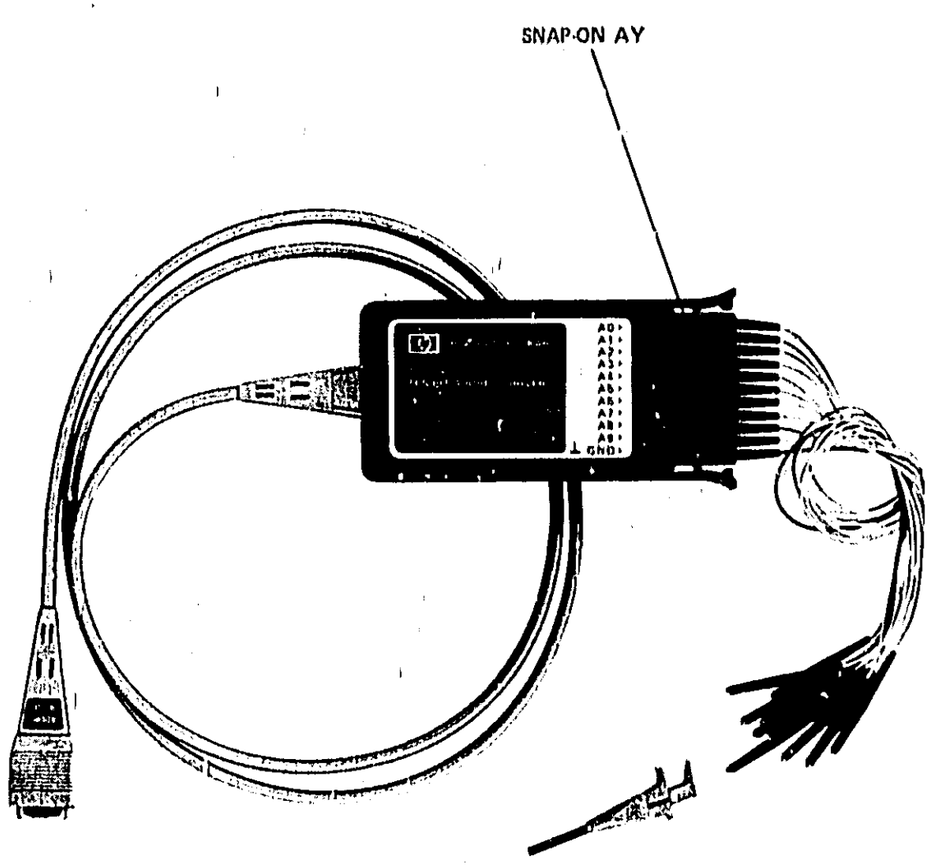
REFERENCE DESIGNATOR		H-P PART NUMBER	DESCRIPTION
A21	C1	0160-4386	C-F 33PF 5% 200V
A21	C2	0160-4386	C-F 33PF 5% 200V
A21	C3	0160-4386	C-F 33PF 5% 200V
A21	C4	0160-4386	C-F 33PF 5% 200V
A21	C5	0160-0576	C-F .1UF 20% 50V
A21	C6	0160-0576	C-F .1UF 20% 50V
A21	CR1	1901-1098	DIO-SWIT:1N4150
A21	CR2	1901-1098	DIO-SWIT:1N4150
A21	CR3	1901-1098	DIO-SWIT:1N4150
A21	CR4	1901-1098	DIO-SWIT:1N4150
A21	J1	1251-3707	CONN-POST 15M
A21	Q1	1854-0215	XSTR SI 2N3904
A21	Q2	1854-0215	XSTR SI 2N3904
A21	Q3	1854-0215	XSTR SI 2N3904
A21	Q4	1854-0215	XSTR SI 2N3904
A21	R1	0757-0458	R-F 51.1K1%
A21	R2	0757-0458	R-F 51.1K1%
A21	R3	0757-0458	R-F 51.1K1%
A21	R4	0757-0458	R-F 51.1K1%
A21	R5	0757-0442	R-F 10K1% .125W
A21	R6	0757-0442	R-F 10K1% .125W
A21	R7	0757-0442	R-F 10K1% .125W
A21	R8	0757-0442	R-F 10K1% .125W
A21	R9	0757-0280	R-F 1K1% .125W F
A21	R10	0757-0280	R-F 1K1% .125W F
A21	R11	0757-0280	R-F 1K1% .125W F
A21	R12	0757-0280	R-F 1K1% .125W F
A21	R13	0757-0437	R-F 4.75K1%
A21	R14	0757-0437	R-F 4.75K1%
A21	R15	0757-0437	R-F 4.75K1%
A21	R16	0757-0437	R-F 4.75K1%
A21	R17	0757-0394	R-F 51.1 1%
A21	R18	0698-7212	R-F 100 1% .05W
A21	R19	0698-7212	R-F 100 1% .05W
A21	R20	0698-7212	R-F 100 1% .05W
A21	R21	0698-7212	R-F 100 1% .05W
A21	U1	1820-1918	IC SN74LS 241N

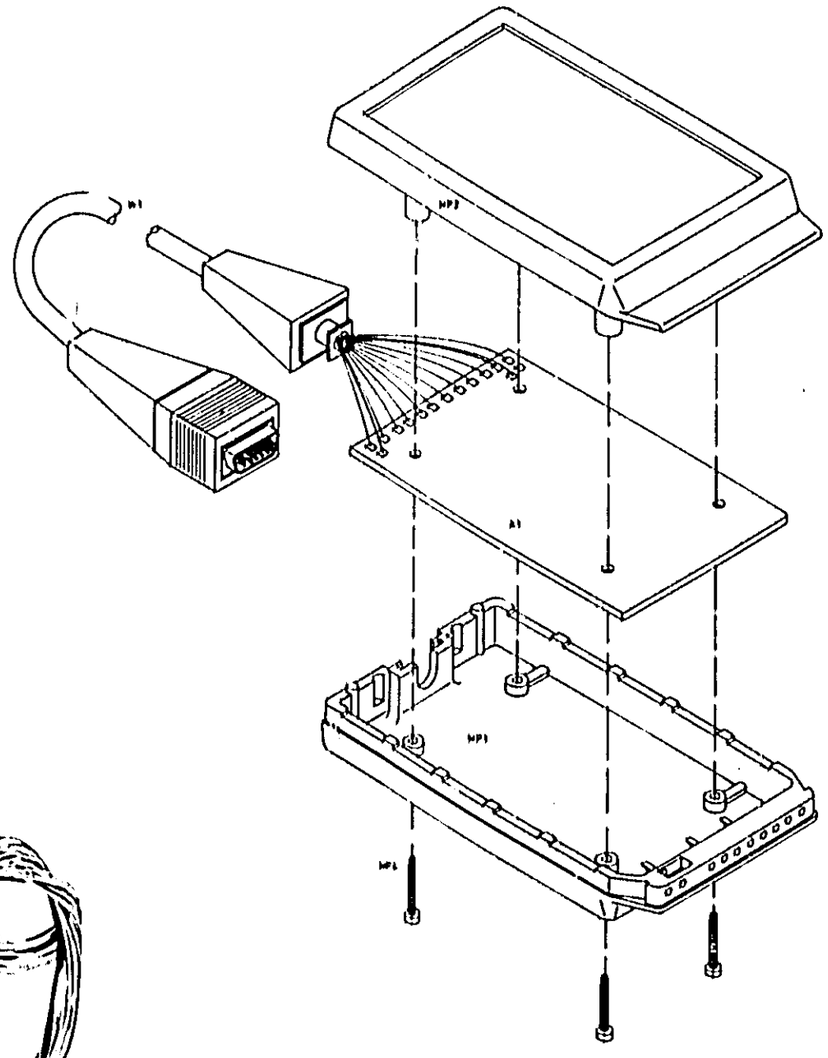
Assembly A22

REFERENCE DESIGNATOR		H-P PART NUMBER	DESCRIPTION
A22	S1	3101-1720	SW PBTN DPDT

Assembly A23

REFERENCE DESIGNATOR		H-P PART NUMBER	DESCRIPTION
A23	FL1	9135-0035	FILTER LINE
A23	S1	3101-2298	SWITCH-SLIDE
A23	S2	3101-2298	SWITCH-SLIDE





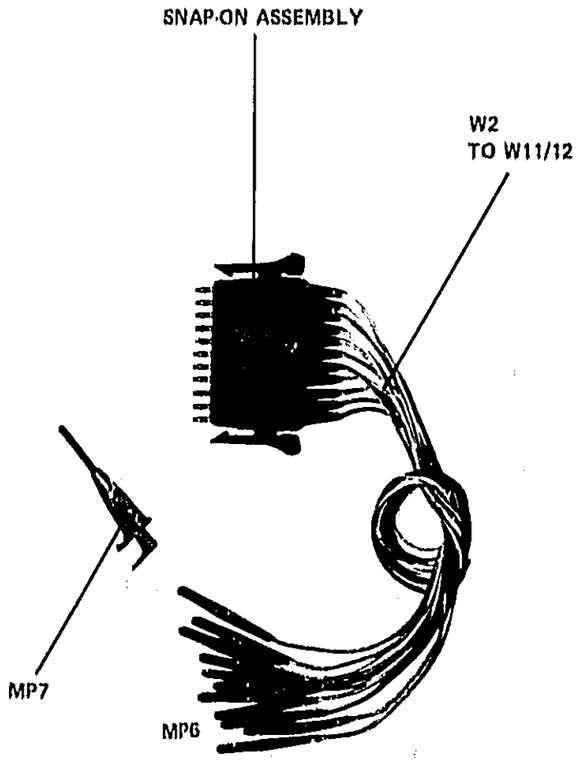


Figure 6-2. Typical Pod Assembly

Table 6-2. Replaceable Parts (cont'd)

15452A (8170A Option 002 only)

REFERENCE DESIGNATOR	H-P PART NUMBER	DESCRIPTION
A1	15452-66501	BD AY ADDR DRVR
MP1	5040-0012	HOUSING BUTTON
MP2	5040-8125	HOUSING TOP
MP4	0624-0306	SCR FPD 2-28 PH
MP6	1U230-62101	CLIP CBL ADAP
MP7	5040-0563	CLIP CONN
W1	08170-61603	CBL AY-15CONN
W2	5061-1215	CBL ADAP BLK
W3	5061-1217	CBL ADAP WHT/BLK
W4	5061-1217	CBL ADAP WHT/BLK
W5	5061-1218	CBL ADAP WHT/BRN
W6	5061-1218	CBL ADAP WHT/BRN
W7	5061-1219	CBL ADAP WHT/RED
W8	5061-1220	CBL ADAP WHT/ORN
W9	5061-1221	CBL ADAP WHT/YEL
W10	5061-1222	CBL ADAP WHT/GRN
W11	5061-1223	CBL ADAP WHT/BLV
W12	5061-1224	CBL ADAP WHT/VIO

REFERENCE DESIGNATOR		H-P PART NUMBER	DESCRIPTION
A1	C1	0160-3174	C-F .47UF 25V
A1	C2	0160-0174	C-F .47UF 25V
A1	C3	0180-1745	C-F 1.5UF 20V
A1	C4	0160-0571	C-F 470 PF
A1	C5	0160-0571	C-F 470 PF
A1	C6	0160-0571	C-F 470 PF
A1	C7	0160-0571	C-F 470 PF
A1	C8	0160-0571	C-F 470 PF
A1	C9	0160-0571	C-F 470 PF
A1	C10	0160-0571	C-F 470 PF
A1	C11	0160-0571	C-F 470 PF
A1	C12	0160-0571	C-F 470 PF
A1	C13	0160-0571	C-F 470 PF
A1	C14	0160-0571	C-F 470 PF
A1	C15	0160-0571	C-F 470 PF
A1	C16	0160-0571	C-F 470 PF
A1	C17	0160-0571	C-F 470 PF
A1	C18	0160-0571	C-F 470 PF
A1	C19	0160-0571	C-F 470 PF
A1	C20	0160-0571	C-F 470 PF
A1	C21	0160-0571	C-F 470 PF
A1	C22	0160-0571	C-F 470 PF
A1	C23	0160-0571	C-F 470 PF
A1	R1	0757-0346	R-F 10 1% .125W
A1	R2	0757-0346	R-F 10 1% .125W
A1	R3	0757-0346	R-F 10 1% .125W
A1	R5	0757-0346	R-F 10 1% .125W
A1	R5	0757-0346	R-F 10 1% .125W
A1	R6	0757-0346	R-F 10 1% .125W
A1	R7	0757-0346	R-F 10 1% .125W
A1	R8	0757-0346	R-F 10 1% .125W
A1	R9	0757-0346	R-F 10 1% .125W
A1	R10	0757-0346	R-F 10 1% .125W
A1	R11	0757-0417	R-F 4.75K 1%
A1	R12	0757-0417	R-F 4.75K 1%
A1	R13	0757-0417	R-F 4.75K 1%
A1	R14	1810-0125	R-NETWORK 4.7K
A1	U1	1820-1918	IC SN74LS 241N
A1	U2	1820-1918	IC SN74LS 241N
A1	U3	1820-1199	IC SN74LS 04

Table 6-2. Replaceable Parts (cont'd)

15453A

REFERENCE DESIGNATOR	H-P PART NUMBER	DESCRIPTION
A1	15453-66501	BD AY ADDR PUD
MP1	5040-4012	HOUSING BOTTOM
MP2	5040-4125	HOUSING TOP
MP4	0624-3306	SCR TPG 2-28 PH
MP6	1023J-62101	CLIP CBL ADAP
MP7	5040-0563	CLIP CONN
W1	08173-61603	CBL AY-15CONN
W2	5061-1215	CBL ADAP BLK
W3	5061-1217	CBL ADAP WHT/BLK
W4	5061-1217	CBL ADAP WHT/BLK
W5	5061-1218	CBL ADAP WHT/BRN
W6	5061-1218	CBL ADAP WHT/BRN
W7	5061-1219	CBL ADAP WHT/RED
W8	5061-1220	CBL ADAP WHT/ORN
W9	5061-1221	CBL ADAP WHT/YEL
W10	5061-1222	CBL ADAP WHT/GRN
W11	5061-1223	CBL ADAP WHT/BLV
W12	5061-1224	CBL ADAP WHT/VIO

REFERENCE DESIGNATOR	H-P PART NUMBER	DESCRIPTION
A1 C1	0160-4386	C-F 33PF 5% 200V
A1 C2	0160-4386	C-F 33PF 5% 200V
A1 C3	0160-4386	C-F 33PF 5% 200V
A1 C4	0160-4386	C-F 33PF 5% 200V
A1 C5	0160-4386	C-F 33PF 5% 200V
A1 C6	0160-4386	C-F 33PF 5% 200V
A1 C7	0160-4386	C-F 33PF 5% 200V
A1 C8	0160-4386	C-F 33PF 5% 200V
A1 C9	0160-4386	C-F 33PF 5% 200V
A1 C10	0160-4386	C-F 33PF 5% 200V
A1 C11	0160-3576	C-F .1UF 20% 50V
A1 C12	0160-3576	C-F .1UF 20% 50V
A1 CR1	1901-1098	DIU-SWIT.IN4150
A1 CR2	1901-1098	DIU-SWIT.IN4150
A1 CR3	1901-1098	DIU-SWIT.IN4150
A1 CR4	1901-1098	DIU-SWIT.IN4150
A1 CR5	1901-1098	DIU-SWIT.IN4150
A1 CR6	1901-1098	DIU-SWIT.IN4150
A1 CR7	1901-1098	DIU-SWIT.IN4150
A1 CR8	1901-1098	DIU-SWIT.IN4150
A1 CR9	1901-1098	DIU-SWIT.IN4150
A1 CR10	1901-1098	DIU-SWIT.IN4150
A1 Q1	1854-0215	XSTR SI 2N3904
A1 Q2	1854-0215	XSTR SI 2N3904
A1 Q3	1854-0215	XSTR SI 2N3904
A1 Q4	1854-0215	XSTR SI 2N3904
A1 Q5	1854-0215	XSTR SI 2N3904
A1 Q6	1854-0215	XSTR SI 2N3904
A1 Q7	1854-0215	XSTR SI 2N3904
A1 Q8	1854-0215	XSTR SI 2N3904
A1 Q9	1854-0215	XSTR SI 2N3904
A1 Q10	1854-0215	XSTR SI 2N3904
A1 R1	0698-7260	R-F 10K 1% .05W
A1 R2	0698-7260	R-F 10K 1% .05W
A1 R3	0698-7260	R-F 10K 1% .05W
A1 R4	0698-7260	R-F 10K 1% .05W
A1 R5	0698-7260	R-F 10K 1% .05W
A1 R6	0698-7260	R-F 10K 1% .05W
A1 R7	0698-7260	R-F 10K 1% .05W
A1 R8	0698-7260	R-F 10K 1% .05W
A1 R9	0698-7260	R-F 10K 1% .05W
A1 R10	0698-7260	R-F 10K 1% .05W
A1 R11	0757-0280	R-F 1K1% .125W F
A1 R12	0757-0280	R-F 1K1% .125W F
A1 R13	0757-0280	R-F 1K1% .125W F
A1 R14	0757-0280	R-F 1K1% .125W F
A1 R15	0757-0280	R-F 1K1% .125W F
A1 R16	0757-0280	R-F 1K1% .125W F
A1 R17	0757-0280	R-F 1K1% .125W F
A1 R18	0757-0280	R-F 1K1% .125W F
A1 R19	0757-0280	R-F 1K1% .125W F
A1 R20	0757-0280	R-F 1K1% .125W F
A1 R21	0698-7277	R-F 51.1K 1% .05
A1 R22	0698-7277	R-F 51.1K 1% .05
A1 R23	0698-7277	R-F 51.1K 1% .05
A1 R24	1810-0378	R-NETWORK 47K
A1 R31	0698-7252	R-F 4.64K 1% .05
A1 R32	0698-7252	R-F 4.64K 1% .05
A1 R33	0698-7252	R-F 4.64K 1% .05
A1 R34	0698-7252	R-F 4.64K 1% .05
A1 R35	0698-7252	R-F 4.64K 1% .05
A1 R36	0698-7252	R-F 4.64K 1% .05
A1 R37	0698-7252	R-F 4.64K 1% .05
A1 R38	0698-7252	R-F 4.64K 1% .05
A1 R39	0698-7252	R-F 4.64K 1% .05
A1 R40	0698-7252	R-F 4.64K 1% .05
A1 R41	0698-7212	R-F 100 1% .05W
A1 R42	0698-7212	R-F 100 1% .05W
A1 R43	0698-7212	R-F 100 1% .05W
A1 R44	0698-7212	R-F 100 1% .05W
A1 R45	0698-7212	R-F 100 1% .05W
A1 R46	0698-7212	R-F 100 1% .05W
A1 R47	0698-7212	R-F 100 1% .05W
A1 R48	0698-7212	R-F 100 1% .05W
A1 R49	0698-7212	R-F 100 1% .05W
A1 R50	0698-7212	R-F 100 1% .05W
A1 U1	1820-1918	IC SN74LS 241N
A1 U2	1820-1918	IC SN74LS 241N

Table 6-2. Replaceable Parts (cont'd)

16464A

REFERENCE DESIGNATOR	H-P PART NUMBER	DESCRIPTION
A1	15451-66501	BD AY CONTR POD
MP1	5040-8012	HOUSING BUTTON
MP2	5040-8125	HOUSING TOP
MP4	0624-0306	SCR TPG 2-28 PH
MP6	10213-62101	CLIP CBL ADAP
MP8	5040-0563	CLIP CONN
W1	08170-61603	CBL AY-15CONN
W2	5061-1215	CBL ADAP BLK
W3	5061-1215	CBL ADAP BLK
W4	5061-1217	CBL ADAP WHT/BLK
W5	5061-1217	CBL ADAP WHT/BLK
W6	5061-1218	CBL ADAP WHT/BRN
W7	5061-1219	CBL ADAP WHT/RED
W8	5061-1220	CBL ADAP WHT/ORN
W9	5061-1221	CBL ADAP WHT/YEL
W10	5061-1222	CBL ADAP WHT/GRN
W11	5061-1223	CBL ADAP WHT/BLV
W12	5061-1224	CBL ADAP WHT/VIO

REFERENCE DESIGNATOR	H-P PART NUMBER	DESCRIPTION
A1	C1	0160-0570 C-F 220PF +-20%
A1	C2	0160-0570 C-F 220PF +-20%
A1	C3	0160-0570 C-F 220PF +-20%
A1	C4	0160-4386 C-F 33PF 5% 200V
A1	C5	0160-4386 C-F 33PF 5% 200V
A1	C6	0160-4386 C-F 33PF 5% 200V
A1	C7	0160-4386 C-F 33PF 5% 200V
A1	C8	0160-4386 C-F 33PF 5% 200V
A1	C9	0160-4386 C-F 33PF 5% 200V
A1	C10	0160-0576 C-F .1UF 20% 50V
A1	C11	0160-0576 C-F .1UF 20% 50V
A1	C12	0160-0576 C-F .1UF 20% 50V
A1	C13	0160-0576 C-F .1UF 20% 50V
A1	CR1	1901-1098 DIU-SWIT.IN4150
A1	CR2	1901-1098 DIU-SWIT.IN4150
A1	CR3	1901-1098 DIU-SWIT.IN4150
A1	CR4	1901-0033 DIODE-SCHOTTKY
A1	CR5	1901-1098 DIU-SWIT.IN4150
A1	CR6	1901-1098 DIU-SWIT.IN4150
A1	CR7	1901-1098 DIU-SWIT.IN4150
A1	CR8	1901-1098 DIU-SWIT.IN4150
A1	CR9	1901-1098 DIU-SWIT.IN4150
A1	CR10	1901-1098 DIU-SWIT.IN4150
A1	L1	9100-2264 COIL MLD 6.8UH
A1	L2	9100-2264 COIL MLD 6.8UH
A1	L3	9100-2264 COIL MLD 6.8UH
A1	MP2	1460-1473 SPRING
A1	Q1	1854-0215 XSTR SI 2N3904
A1	Q2	1854-0215 XSTR SI 2N3904
A1	Q3	1854-0215 XSTR SI 2N3904
A1	Q4	1854-0215 XSTR SI 2N3904
A1	Q5	1854-0215 XSTR SI 2N3904
A1	Q6	1854-0215 XSTR SI 2N3904
A1	Q7	1855-0081 XSTR FET 2N5245
A1	R1	0698-7252 R-F 4.64K 1% .05
A1	R2	0698-7252 R-F 4.64K 1% .05
A1	R3	0698-7252 R-F 4.64K 1% .05
A1	R4	0698-7212 R-F 100 1% .05W
A1	R5	0698-7212 R-F 100 1% .05W
A1	R6	0698-7212 R-F 100 1% .05W
A1	R7	0699-0120 R-F 100 5% 8.5W
A1	R8	0699-0120 R-F 100 5% 8.5W
A1	R9	0699-0120 R-F 100 5% 8.5W
A1	R10	0698-7236 R-F 1K 1% .05W
A1	R11	0698-7260 R-F 10K 1% .05W
A1	R12	0698-7260 R-F 10K 1% .05W
A1	R13	0698-7260 R-F 10K 1% .05W
A1	R14	0698-7260 R-F 10K 1% .05W
A1	R15	0698-7260 R-F 10K 1% .05W
A1	R16	0698-7260 R-F 10K 1% .05W
A1	R17	1810-0030 NETWORK 7 RES
A1	R23	1810-0125 R-NETWORK 4.7K
A1	R35	0698-7212 R-F 100 1% .05W
A1	R29	1810-0395 R-NETW 47K 7X
A1	R36	0698-7212 R-F 100 1% .05W
A1	R37	0698-7212 R-F 100 1% .05W
A1	R38	0698-7212 R-F 100 1% .05W
A1	R39	0698-7212 R-F 100 1% .05W
A1	R40	0698-7212 R-F 100 1% .05W
A1	R41	0698-7236 R-F 1K 1% .05W
A1	R42	0698-7205 R-F 51.1 1% .05W
A1	U1	1820-1887 IC DGTL SN75361
A1	U2	1820-1887 IC DGTL SN75361
A1	U3	1820-1887 IC DGTL SN75361
A1	U4	1820-1918 IC SN74LS 241N
A1	U5	1820-1887 IC DGTL SN75361

Table 6-2. Replaceable Parts (cont'd)

15455/56A

REFERENCE DESIGNATOR	H-P PART NUMBER	DESCRIPTION
A1	15455-66501	BD AY DATA PUD
MP1	5040-4012	HOUSING BUTTON
MP2	5040-8125	HOUSING TOP
MP4	0624-0306	SCR PPH 2-28 PH
MP6	1021-0201	CLIP CBL ADAP
MP7	5040-3563	CLIP CONN
W1	08170-61603	CBL AY-15CONN
W2	5061-1215	CBL ADAP BLK
W3	5061-1215	CBL ADAP BLK
W4	5061-1217	CBL ADAP WHT/BLK
W5	5061-1218	CBL ADAP WHT/BRN
W6	5061-1219	CBL ADAP WHT/RED
W7	5061-1220	CBL ADAP WHT/ORN
W8	5061-1221	CBL ADAP WHT/YEL
W9	5061-1222	CBL ADAP WHT/GRN
W10	5061-1223	CBL ADAP WHT/BLV
W11	5061-1224	CBL ADAP WHT/VIO

REFERENCE DESIGNATOR		H-P PART NUMBER	DESCRIPTION
A1	C1	0160-0570	C-F 220PF +-20%
A1	C2	0160-0570	C-F 220PF +-20%
A1	C3	0160-0570	C-F 220PF +-20%
A1	C4	0160-0570	C-F 220PF +-20%
A1	C5	0160-0570	C-F 220PF +-20%
A1	C6	0160-0570	C-F 220PF +-20%
A1	C7	0160-0570	C-F 220PF +-20%
A1	C8	0160-0570	C-F 220PF +-20%
A1	C9	0160-0576	C-F .1UF 20% 50V
A1	C10	0160-0576	C-F .1UF 20% 50V
A1	C11	0160-0576	C-F .1UF 20% 50V
A1	C12	0160-0576	C-F .1UF 20% 50V
A1	C13	0160-0576	C-F .1UF 20% 50V
A1	C14	0160-0576	C-F .1UF 20% 50V
A1	C15	0160-0576	C-F .1UF 20% 50V
A1	C16	0160-0576	C-F .1UF 20% 50V
A1	C17	0160-0576	C-F .1UF 20% 50V
A1	C18	0160-0576	C-F .1UF 20% 50V
A1	C19	0160-0576	C-F .1UF 20% 50V
A1	C20	0160-0576	C-F .1UF 20% 50V
A1	C21	0160-0576	C-F .1UF 20% 50V
A1	CR1	1901-1098	DIO-SWIT.IN4150
A1	CR2	1901-1098	DIO-SWIT.IN4150
A1	CR3	1901-1098	DIO-SWIT.IN4150
A1	CR4	1901-1098	DIO-SWIT.IN4150
A1	CR5	1901-1098	DIO-SWIT.IN4150
A1	CR6	1901-1098	DIO-SWIT.IN4150
A1	CR7	1901-1098	DIO-SWIT.IN4150
A1	CR8	1901-1098	DIO-SWIT.IN4150
A1	CR9	1901-0539	DIODE-SCHOTTKY
A1	L1	9100-2264	COIL MLD 6.8UH
A1	L2	9100-2264	COIL MLD 6.8UH
A1	L3	9100-2264	COIL MLD 6.8UH
A1	L4	9100-2264	COIL MLD 6.8UH
A1	L5	9100-2264	COIL MLD 6.8UH
A1	L6	9100-2264	COIL MLD 6.8UH
A1	L7	9100-2264	COIL MLD 6.8UH
A1	L8	9100-2264	COIL MLD 6.8UH
A1	MP1	1460-1473	SPRING
A1	Q1	1855-0081	XSTR FET 2N5245
A1	Q2	1855-0081	XSTR FET 2N5245
A1	Q3	1855-0081	XSTR FET 2N5245
A1	Q4	1855-0081	XSTR FET 2N5245
A1	Q5	1855-0081	XSTR FET 2N5245
A1	Q6	1855-0081	XSTR FET 2N5245
A1	Q7	1855-0081	XSTR FET 2N5245
A1	Q8	1855-0081	XSTR FET 2N5245
A1	R1	0698-7212	R-F 100 1% .05W
A1	R2	0698-7212	R-F 100 1% .05W
A1	R3	0698-7212	R-F 100 1% .05W
A1	R4	0698-7212	R-F 100 1% .05W
A1	R5	0698-7212	R-F 100 1% .05W
A1	R6	0698-7212	R-F 100 1% .05W
A1	R7	0698-7212	R-F 100 1% .05W
A1	R8	0698-7212	R-F 100 1% .05W
A1	R9	0699-0120	R-F 100 548.5W
A1	R10	0699-0120	R-F 100 548.5W
A1	R11	0699-0120	R-F 100 548.5W
A1	R12	0699-0120	R-F 100 548.5W
A1	R13	0699-0120	R-F 100 548.5W
A1	R14	0699-0120	R-F 100 548.5W
A1	R15	0699-0120	R-F 100 548.5W
A1	R16	0699-0120	R-F 100 548.5W
A1	R17	0757-0417	R-F 4.75K1%
A1	R18	0757-0274	R-F 1.21K1%
A1	R19	0757-0274	R-F 1.21K1%
A1	R21	1810-0125	R-NETWORK 4.7K
A1	U1	1820-1887	IC DGTL SN75361
A1	U2	1820-1887	IC DGTL SN75361
A1	U3	1820-1887	IC DGTL SN75361
A1	U4	1820-1887	IC DGTL SN75361
A1	U5	1820-1237	IC DGTL SN75361
A1	U6	1820-1887	IC DGTL SN75361
A1	U7	1820-1887	IC DGTL SN75361
A1	U8	1820-1887	IC DGTL SN75361
A1	U9	1820-1887	IC DGTL SN75361

BACK DATING MANUAL CHANGES

SECTION VII
BACKDATING

7–1 EARLIER MODELS

7–2 Earlier models are equipped with A13 Bd Ay PROM (Service Sheet 1F) instead of ROMs on A1. In the event of failure, replace A13. The individual PROM's are not replaceable.

7–3 SERIAL NUMBERS 1739G00101 TO 115

7–4 These models are fitted with A1 Bd Ay Microprocessor 08170-66501 Rev. A instead of Rev. B. Display blanking may occur at critical frequencies of the external BREAK IN, START IN and HP-IB addressing/de-addressing.

SERVICE INFORMATION

SECTION VIII
SERVICE

8–1 INTRODUCTION

8–2 This section contains component layouts, schematic diagrams, principles of operation and service information. These are organized as 'Service Sheets', which are identified by a large number within a square in the lower corners. Service Sheet 0 contains information for the instrument as a whole, and assists troubleshooting to board level. Other service sheets concern specific boards, see Tables 8–1 and 8–2. Schematic Diagram symbols are summarized in Table 8–3. Diagnostic test procedures are summarized under § 8–11.

Table 8–1. Index to Assemblies

	Service Sheet
Block diagram	0
A1 μP	1
A2 RAM	2
A3 RAM Opt	3
A4 Addr	4
A5 HP-IB/RS 232	5
A6 Control	6
A7 PS	7
A8 Mother 1	Layout: 7
A9 Mother 2	Wiring: 1–7
A10 Display	1
A11 Keyboard	1
A12 Conn Bd	2,6,7
A13 PROM	1
A19 Switch	6
A20 I/F Conn	5
A21 Trigger	4
A22 Cable Ay Power Switch	7
16453A Addr Pod	4
16454A Control Pod	6
16455A Data Pod 0–7	2
16456A Data Pod 15–8	2
Mainframe	Figure 6–1
Pods	Figure 6–2

8–3 SAFETY CONSIDERATIONS

8–4 Although this instrument has been designed in accordance with international safety standards, this manual contains information, cautions, and warnings which must be followed to ensure safe operation and to retain the instrument in safe condition (see Sections II and III). Service and adjustments should be performed only by qualified service personnel. After repair, the After Service Safety Check (§ 8–27) must be performed.

WARNING

Any interruption of the protective (grounding) conductor (inside or outside the instrument) or disconnection of the protective earth terminal is likely to make the instrument dangerous. Intentional interruption is prohibited.

8–5 Any adjustment, maintenance, and repair of the opened instrument with voltage applied should be avoided as much as possible and, when inevitable, should be carried out only by a skilled person who is aware of the hazard involved.

8–6 Capacitors inside the instrument may still be charged even if the instrument has been disconnected from its source of supply.

8–7 Make sure that only fuses with the required rated current and of the specified type (normal blow, time delay, etc.) are used for replacement. The use of repaired fuses and the shortcircuiting of fuseholders must be avoided.

8–8 Whenever it is likely that the protection offered by the fuses has been impaired, the instrument must be made inoperative and secured against any unintended operation.

WARNING

Adjustments described herein are performed with power supplied to the instrument while protective covers are removed. Energy available at many points may, if contacted, result in personal injury.

8–9 PRINCIPLES OF OPERATION

8–10 A description how the instrument works in general is contained in Service Sheet 0. More detailed circuit descriptions are contained in subsequent service sheets. The symbology used in block and circuit diagrams is explained in Table 8–3.

8–11 TROUBLESHOOTING

IMPORTANT NOTE

If boards A1 or A2 are removed, the 8170A will power-up with the following parameters:
8-BIT DATA BUS, INT ADDR MODE,
AUTO CYCLE, TTL OUTPUT,
MAN CLOCK MODE.

In the Extended Memory Option 001, removal of A2 or A3 causes loss of A3 data (A3 uses A2's battery back-up and has no batteries of its own).

Removal of A3 may mean that the F-, T-, and L-address are out of address range, F- and T-ADDR will then be automatically set to zero, and L-ADDR to the highest available address.

8–12 The 8170A is equipped with a number of built-in troubleshooting aids:

Go/No Go Tests for:
Indicators,
ROMs.
Digital Signature Analysis (DSA) routines which help verify a suspect sub-assembly and assist in troubleshooting to component level.

Before commencing any of these tests, verify the power supplies in accordance with Service Sheet 7 and the adjustments in Section V.

8–13 Indicator Test

8–14 If all lamps do not light briefly at switch-on (§ 3–6), procede as follows:

Set A1S1 to T (Figure 8–1).
Press A1S2 to [illegible] – all LED's should light for approx. 1 s.
Press the zero key (0) on the front panel – all indicators should light for approx 3 s.

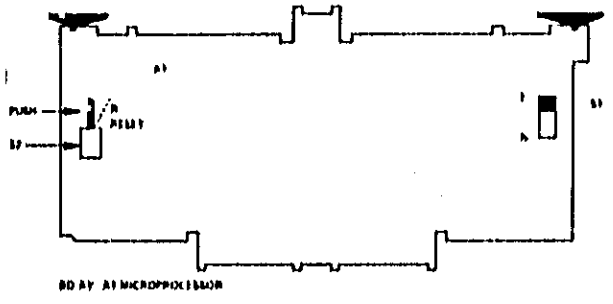


Figure 8–1. Location of Internal Switches

8–15 ROM Test

8–16 This test establishes that the stored μP program is correct. Each part checks a specific ROM, correct function being indicated by a specific display. To access each part of the test:

Set A1S1 to T (if not already selected),

Press the ADDRESS/DATA value key shown below:

ADDRESS/DATA Value Key	ROM Tested	DISPLAY Data Code Selected → BIN	OCT	HEX
1	A1U1		1 → 377	1 → 3FF
2	A1U2	A11	2 → 377	2 → 3FF
3	A1U3	bits	3 → 377	3 → 3FF
4	A1U4	high	4 → 377	4 → 3FF
5	A1U5		5 → 377	5 → 3FF
6	A1U6		6 → 377	6 → 3FF

8–17 DSA Test Routines

8–18 The following test routines are available for DSA using the HP Model 5004A Digital Signature Analyzer:

Test Routine and designator		Documentation Service Sheet
Address Board	A	4
HP-IB RS 232C	B	5
Control Board	C	6
Display	D	1
Operational RAM	E	1
User RAM	F	2,3
Address Counter	1	4
Microprocessor	2	1
Keyboard	3	1

The DSA concept is presented in the Model 5004A's Manual.

8–19 Signature documentation in this manual is organized as follows:

In the following paragraphs, The complete procedure is explained.

On the component layouts, To permit rapid location of the 5004A probe and fast signature verification, the signatures are shown within the IC outline adjacent to the pin concerned. The corresponding test routine is indicated next to the title, bottom left of page. Test-set-up, procedure and reference signature values are given here.

On the schematics, All points with a signature are identified by the designator of the test routine concerned. This allows rapid appraisal of the circuit between adjacent 'good' and 'bad' signatures once these have been established.

8–20 As the signature obtained at any point depends on the DSA routine and 5004A connections, always check the selection procedure each time a new test routine is required:

Set A1S1 to T (if not already selected),
Press A1S2 to R (when initially selecting a test routine and when changing test routines),
Press the ADDRESS/DATA value key shown,

and verify the reference signatures:

Reference signature	Example of actual signal	5004A lamp	Signature value
SH (signature, high level)	+5 V supply.	Bright	See Service Sheet
	5004A probe input floating, RESET button pressed .	Glows	
SHF (signature, high level, flashing)	Clock signal	Flashing	Same as SH
SL (signature, low level)	Ground	Off	0000
SLF (signature, low level, flashing)	Clock signal	Flashing	0000

8–21 Address Board Routine (DSA Routine A)

8–22 Connect as follows:

5004A	8170A BD AY A1 Testpoint
START,STOP	G/H
CLOCK	CLK
GROUND	GND

Release all 5004A pushbuttons and set the 8170A as follows:

all jumpers in the NORMAL position,
set A1S1 to T,
press A1S2 to R,
press the A key on the front panel.

Verify that the SH reference signature (see A4 Component Layout, DSA Routine A) is H3UH. Proceed by taking and comparing signatures shown on the layout.

8–23 HP-IB/RS 232C Board Routine (DSA Routine B)

8–24 Connect as follows:

5004A	8170A BD AY A1 Testpoint
START, STOP	G/H
CLOCK	CLK
GROUND	GND

Release all 5004A pushbuttons and set the 8170A as follows:

jumpers A5W4, A5W5 to DSA,
both Address selectors (rear panel) to 111 111,
set BAUD RATE (rear panel) to 150,
set A1S1 to T,
press A1S2 to R,
press the B key on the front panel.

Verify that the SH reference signature (see A5 Component Layout, DSA Routine B) is 3374. Proceed by taking and comparing signatures shown on the layout. When completed, put back jumpers A5W4, A5W5.

In earlier models, it may be necessary to switch the instrument off (as well as setting A1S1 to NORMAL) in order to leave this routine.

8–25 Control Board Routine (DSA Routine C)

8–26 Connect as follows:

5004A	8170A BD AY A1 Testpoint
START, STOP	G/H
CLOCK	CLK
GROUND	GND

Release all 5004A pushbuttons and set the 8170A as follows:

jumpers A4W6, A4W7 to DSA,
ENable switches 1, 2, 3, 4 (rear panel) to OFF,
RFD switch to LOW,
DAV switch to HIGH,
DELAY ADJ to MIN,
Control Pod 15464A connected,
Set A1S1 to T,
press A1S2 to R,
press the C key on the front panel.

Verify that the SH signature (see A6 Component Layout, DSA Routine C) is 1668. Proceed by taking and comparing all signatures shown on the layouts. When completed, put back jumpers A4W6, A4W7.

8–27 Display Routine (DSA Routine D)

8–28 Connect as follows:

5004A	8170A BD AY A1 Testpoint
START, STOP	G/H
CLOCK	CLK
GROUND	GND

Depress 5004A's clock button (⌥) and release all other pushbuttons.

Set the 8170A as follows:

Jumper A1W3 to DSA (serial numbers 1739G00116 and higher), alternatively lift U36 pin 11 from socket and connect to +5 V at U36 pin 14 (serial numbers 1739G00115 and below),
set A1S1 to T,
press A1S2 to R,
press the D key on the front panel.

Verify that the SH reference signature (see A1 Component Layout, DSA Routine D) is AH7P. Proceed by taking and comparing signatures shown on the layout. When completed, put back the jumper A1W3/U36 pin 14.

8–29 Operational RAM Routine (DSA Routine E)

8–30 Connect as follows:

5004A	8170A BD AY A1 Testpoint
START, STOP	G/H
CLOCK	CLK
GROUND	GND

Release all 5004A's pushbuttons and set the 8170A as follows:

all jumpers in NORMAL position,
set A1S1 to T,
press A1S2 to R,
press the E key on the front panel.

Verify that the SH reference signature (see A1 Component Layout, DSA Routine E) is 2 PP4. Proceed by taking and comparing signatures shown on A1 layout for DSA Routine E.

8–31 User RAM Routine (DSA Routine F)

8–32 Connect 5004A as above and release all buttons. Set the 8170A as follows:

remove A3 Extended Memory Board (applies to Option 001 only),
remove A5 HP-IB/RS 232C,
set DATA switch on rear panel to high,
set A1S1 to T,
press A1S2 to R,
press the F key on the front panel.

Verify that the SH reference signature (see A2 Component Layout, DSA Routine F, 1 k Memory) is 2C5A. Proceed by taking and comparing signatures shown on the layout.

8–33 For the 8170A Option 001 only, replace A3 Extended Memory Board and verify that the SH reference signature (see A3 Component Layout, DSA Routine F, 4 k Memory) is now 95P7. Proceed by taking and comparing signatures shown on the layout. Note that, for the extended memory, the 5004A's CLOCK button must be depressed (⌥) when taking signatures from the RAM data outputs (pins 9 to 16 on each RAM IC).

8–34 Address Counter Routine (DSA Routine 1)

8–35 Connect as follows:

5004A	8170A BD AY A1 Testpoint
START, STOP	U40 pin 2
CLOCK	U7 pin 6
GROUND	Chassis

Check all 5004A pushbuttons are released. Then procede as follows:

remove A3 Extended Memory Board (applies to Option 001 only),
set A1S1 to N,
on front panel, select: 8-BIT, AUTO, INT ADDR MODE, INT CLOCK 0.2 MHz – 2 MHz,
Load F-ADDR zero
Load L-ADDR 3FF (HEX address code)
press START (for active state).

Verify that the SH reference signature (see A4 Component Layout, DSA Routine 1, 1 k Memory) is 8P54. Proceed by taking and comparing signatures shown on the layout.

8–36 The following is for 8170A Option 001 only:

replace A3 Extended Memory Board,
change L-ADDR to FFF.

Connect as follows:

5004A	8170A BD AY A4 Testpoint
START, STOP	U40 pin 7
CLOCK	U7 pin 6
GROUND	Chassis

Check that all 5004A pushbuttons are released. Verify that the SH reference signature (see A4 Component Layout, DSA Routine 1, 4 k Memory) is 826P. Proceed by taking and comparing signatures shown on the layout.

8–37 Microprocessor Routine (DSA Routine 2)

8–38 Connect as follows:

5004A	8170A BD AY A1 Testpoint
START, STOP	Address Bit A15
CLOCK	CLK
GROUND	GND

Check that all 5004A pushbuttons are released. Set the 8170A as follows:

Set jumper A1W1 to DSA,
remove jumper A1W2 (later models, set to DSA),
set A1S1 to T,
press A1S2 to R.

Verify that the SH reference signature (see A1 Component Layout, DSA Routine 2) is 0003. Proceed by taking and comparing all signatures shown on the layout. When completed, put back jumpers A1W1, A1W2. If instrument is fitted with A13 Bd Ay PROM instead of ROMs A1U1 to U6, use A13 Component Layout, DSA Routine 2 as well.

8–39 Keyboard Routine (DSA Routine 3)

8–40 Connect and set the 5004A as follows:

5004A	8170A BD AY A1 Testpoint
START, STOP	G/H
CLOCK	CLK
GROUND	GND

Check that all 5004A pushbuttons are released. Set the 8170A as follows:

all jumpers in the NORMAL position,
set A1S1 to T,
press A1S2 to DSA11.

Verify that the SH reference signature (A1U20 pin 6) is C788. Connect the 5004A's data probe to A1U20 pin 6. Press each front panel control in turn and verify the signature obtained:

KEY	SIGNATURE	KEY	SIGNATURE	KEY	SIGNATURE
8 BIT	8 0 5 H	F ADDR	6 3 7 P	A	C P 0 1
16 BIT	U 0 6 7	T ADDR	8 7 6 1	B	A P 0 1
INT ADDR	C 4 0 P	L ADDR	F 1 6 P	C	A 6 1 6
EXT ADDR	0 3 0 A	ADDR	6 1 6 C	D	U 3 3 A
AUTO	7 7 C 6	DATA	4 H H P	E	1 4 P U
SINGLE	5 H 7 A	ENTER	A 2 F 3	F	U U 0 6
TTL	0 3 U 9				
VAR	D 9 4 C	0	6 6 U 8	START	0 P C H
2 WIRE	4 7 0 7	1	0 6 8 3	STOP	P U 0 0
3 WIRE	P H 6 0	2	8 6 1 1	FWD	7 0 H P
EXT (clock)	3 6 6 1	3	6 U 7 2	BACK	5 7 0 P
MAN	P F 0 8	4	4 F C A		
2 MHz – .2 MHz	1 F 7 3	5	5 7 8 F	HEX	8 3 0 7
.2 MHz – 20 kHz	8 2 6 4	6	7 8 6 H	DEC	4 H 3 7
20 kHz – 2 kHz	2 U 6 0	7	8 0 0 8	OCT	C 6 0 1
2 kHz – 200 Hz	P 2 H 6	8	4 6 6 U	BIN	P 7 U P
200 Hz – 20 Hz	0 4 5 1	9	P 4 7 3		

8–41 RECOMMENDED TEST EQUIPMENT

8–42 Refer to Table 1–1.

8–43 REPAIR

8–44 Any necessary repair procedures are described on the appropriate service sheet. Board layouts include a component locator (grid reference with index). Mainframe structure and components are illustrated in Figure 6–1. Reference designators and abbreviations are listed in Table 6–1.

8–45 Service Aids

8–46 25-pin extender boards are available under HP part number 5061–2160.

8–47 After-Service Safety Check

8–48 Execute the following checks when servicing is completed.

8–49 Disconnect power cord from line. Visually inspect interior of instrument for any sign of abnormal internally generated heat, such as discolored printed

circuit boards or components, damaged insulation, or evidence of arcing. Determine cause and remedy.

8-50 Check cabinet/ground pin continuity in accordance with IEC/VDE. Flex the power cord while making the measurement to detect any intermittent discontinuity. Check internal ground connections on boards and frame. Also check resistance of any front or rear panel ground terminals marked ⏚ .

8-51 Check cabinet/line isolation in accordance with IEC/VDE. Replace any component which results in a failure or refer to production Memo or Service Note issued by product division for alternate action.

8-52 Check line fuse to verify that the proper value is installed.

8-53 Check that safety covers are installed (Figure 6-1, MP10).

8-54 Check that all coaxial and flat cables inside are properly connected. Check that all boards and the heatsink on the chassis are properly connected. Verify that the board clamp (Figure 6-1 MP6) is fitted).

8-55 Inform Hewlett-Packard (internally, the responsible product division) of any repeated failures in the above tests or any other safety features.

Table 8-2. Service Sheet Index

Service Sheet		
0		Block diagram
1A	A1, A10, A11	Keyboard, Control Port
1B	A1	Microprocessor I/O Ports
1C	A1	Microprocessor, Operational Memory
1D	A1	Display Logic, μP Supplies
1E	A1, A10	Displays
1F	A13	PROMS.
2A	A2	Battery back-up
2B	A2, A19	1 K byte User RAM
2C	A12, 15455A/56A	Data Output
3	A3	3 K byte User RAM (Option 001)
4A	A4, A10, A21	Rate Generator, Address Logic Control
4B	A4, A21	Address Logic
4C	A12, 15453A	Address Input (Bits 0-9)
4D	A12, 15452A	Address Output (Option 002)
5A	A5, A10, A20	HP-IB Interface
5B	A5, A20	RS 232C Interface
6A	A6	Control Logic
6B	A6, A19	Control Logic, EN Inputs
6C	A12, 15454A	Control I/O, Address Input (Bits 10, 11)
7	A7, A9, A10	Power Supplies

Table 8–3. Schematic Diagram Notes (1 of 2)

The following symbols conform, as far as possible, with ANSI Y 32.2, IEEE No. 315 and ANSI Y32.14 (for the logic symbols). These standards should be consulted when further informations is required.

General

Units — Resistance values are in ohms, capacitance values in microfarads and inductance values in microhenries unless otherwise noted.

P/O — Part of

✳ — Asterisk denotes a factory selected value. The value shown is the nominal value.

Encloses front panel nomenclature.

Encloses rear panel nomenclature.

Heavy line indicates signal path.

Heavy dashed line indicates primary feedback path.

Q47 — Wire colour code. Same as resistor colour code. First number is wire body colour.

Wire or plug used as link.

Test point in a circuit. Point may/may not be identified on P.C. board.

Used with trimmer potentiometers or capacitors to indicate screwdriver adjustment.

Direct connection to earth.

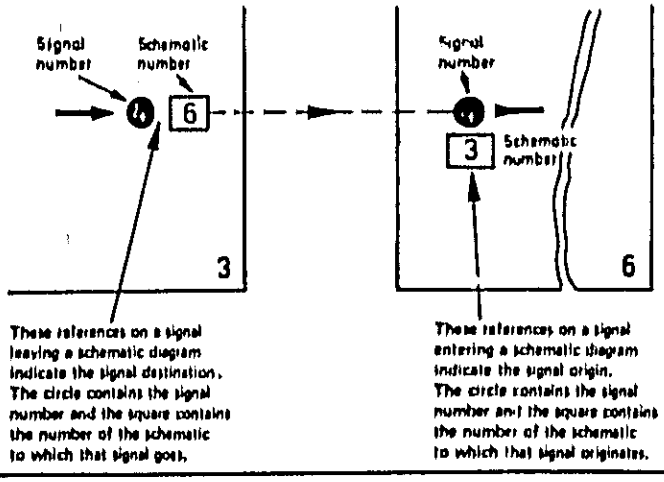
Ground connection to instrument chassis or frame.

Used when a number of common return connections are at the same potential. If there is more than one such system in the same circuit, numbers are written in the triangles so that all connections with the same potential have the same number.

xV — Specific potential difference with respect to a potential reference level, eg.

+10 V

Schematic Referencing



These references on a signal leaving a schematic diagram indicate the signal destination. The circle contains the signal number and the square contains the number of the schematic to which that signal goes.

These references on a signal entering a schematic diagram indicate the signal origin. The circle contains the signal number and the square contains the number of the schematic to which that signal originates.

Components

Normally open toggle switch. Circles (O) are used for the contacts to indicate a locking type switch.

Spring return, 2 position transfer switch. Triangle (▲) are used for the contacts to indicate a non locking type switch.

2 position, 2 pole slide switch.

Air cored inductor.

Air cored transformer. The dot (●) is used, when necessary, to indicate instantaneous polarity.

Iron core

Ferrite core

bead — Ferrite bead

Varactor diode

Multi-junction diode

Diode

Zener diode

Schottky diode

Light Emitting Diode (LED)

Photodiode

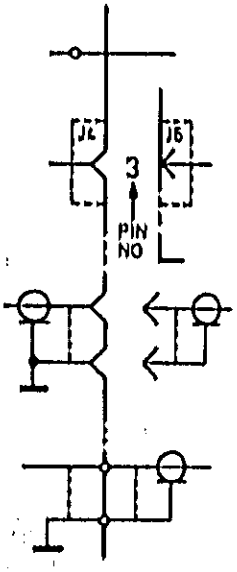
Fuse

Neon

Filament lamp

Table 8–3. Schematic Diagram Notes (2 of 2)

Terminals and Connectors



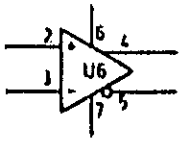
Soldered connection.

Example of board male and female connectors with plug and socket and contact designators, eg. P.C. board edge connector and socket.

example of bulkhead mounted coaxial socket with free coaxial plug and cable.

example of coaxial cable with termination soldered to P.C. board.

Analog Symbols



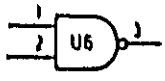
Operational amplifier

Voltage source

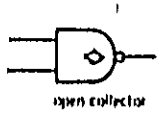
Current source

Logic Symbols

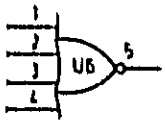
Positive logic is used unless otherwise specified.



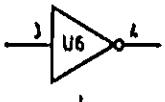
2 input NAND gate



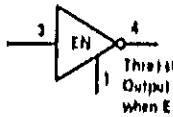
open collector



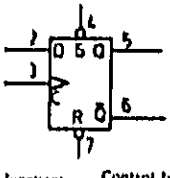
4 input NOR gate



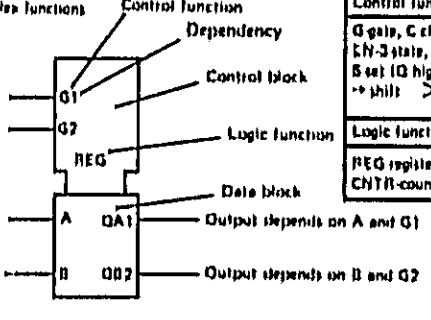
Inverter



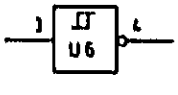
Three state device. Output is high impedance when EN is false, irrespective of input. Normal operation when EN is true.



Flip flop



Control functions:
G-gate, C clock EN-3 state, R-reset (Q low) S-set (Q high), ↑ (↓) count up (down) → shift > edge triggered.
Logic functions:
REG register, SEL-selector CNTR-counter, (DE)MUX (de)multiplexer

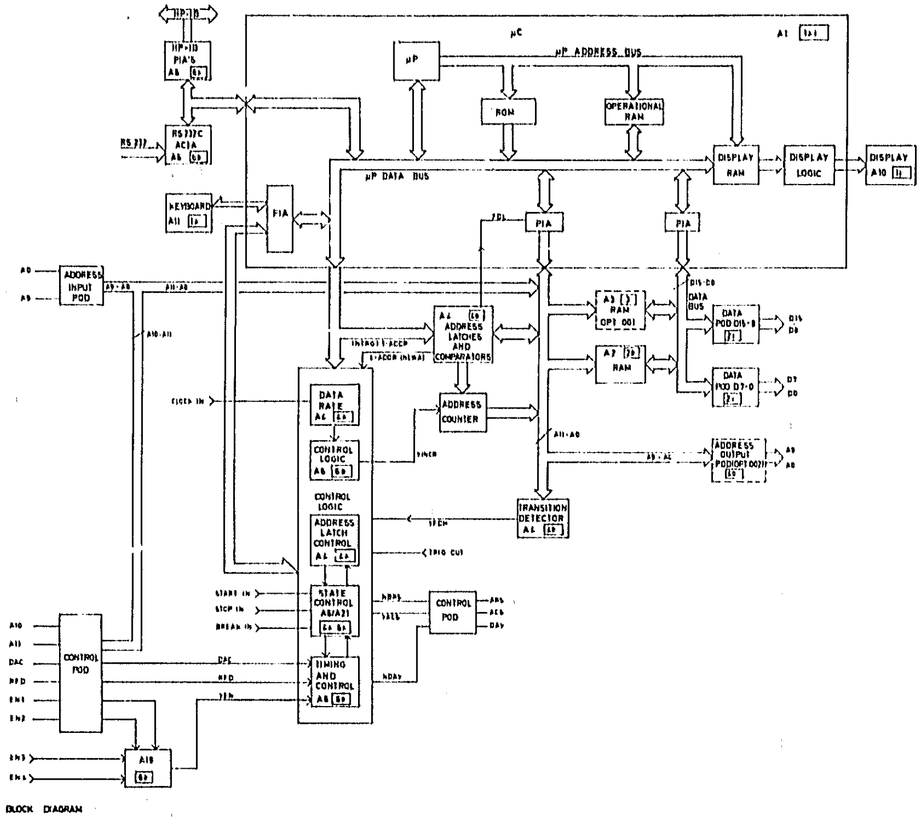


Schmitt trigger

Wired AND connection

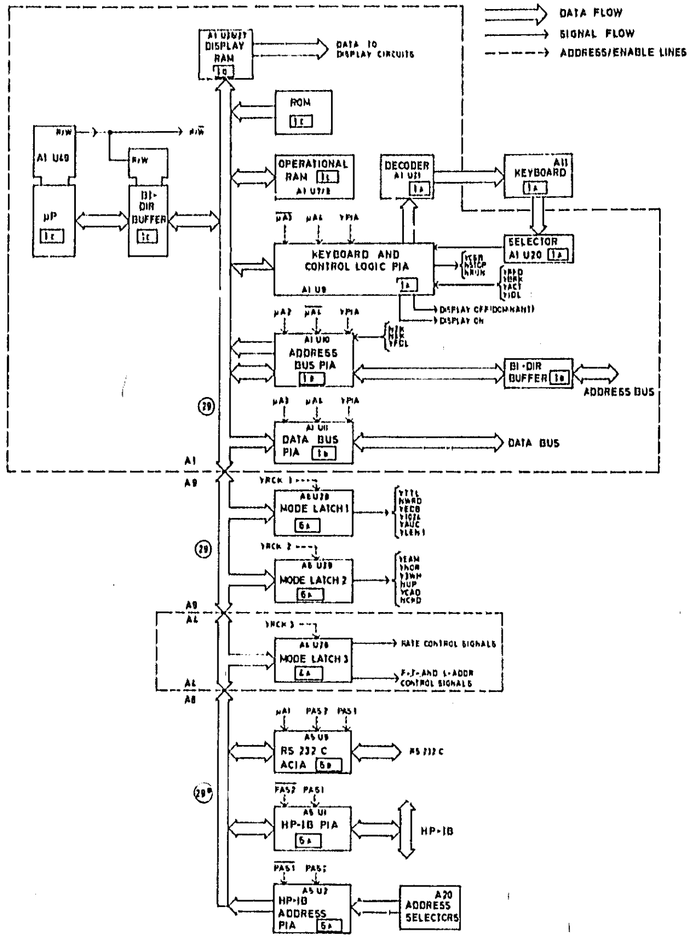
Wired OR connection

BLOCK DIAGRAM 8170A

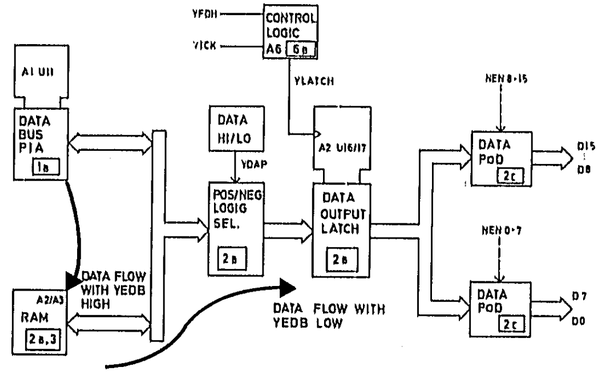


BLOCK DIAGRAM

µP DATA BUS DETAIL

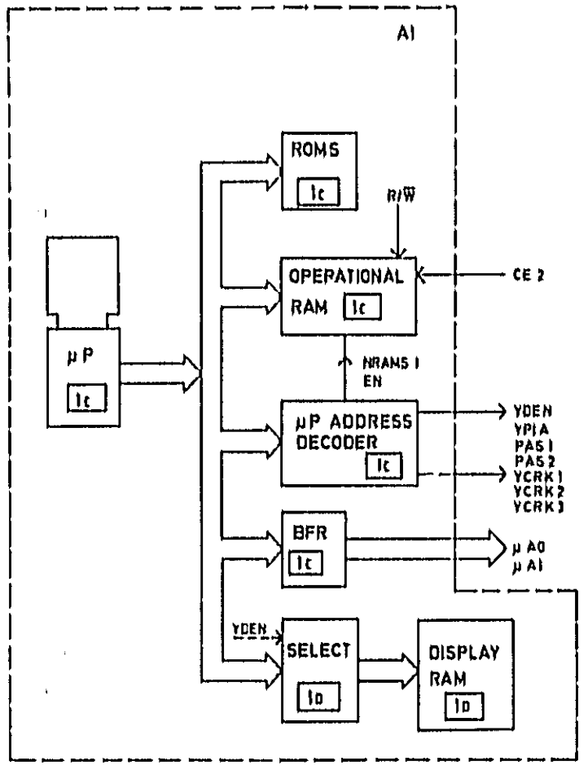


DATA BUS DETAIL

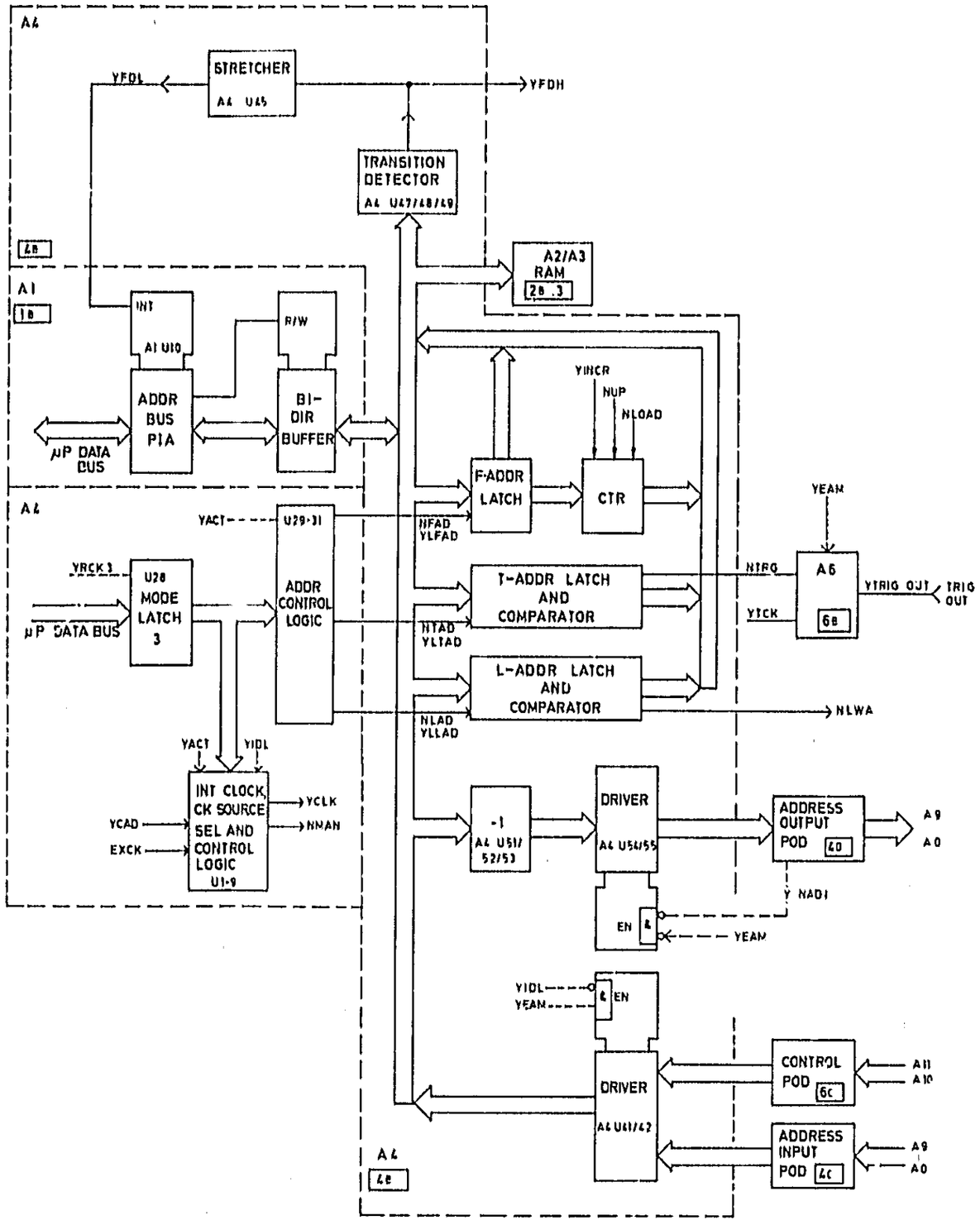


0 –1 BLOCK DIAGRAMS
8170A Overall
µP Data Bus
Data Bus

µP ADDRESS BUS DETAIL



ADDRESS BUS DETAIL



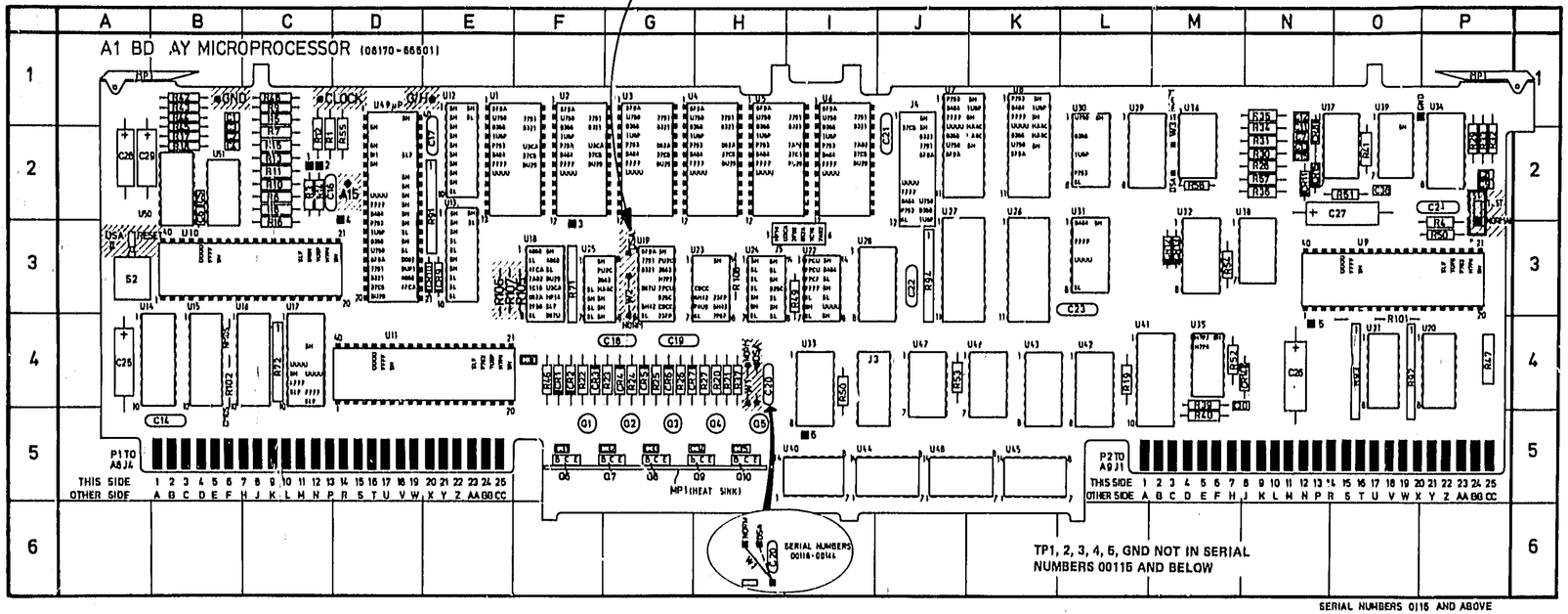
0–2 BLOCK DIAGRAMS
µP Address Bus
Address Bus

Table 8-0-1. Index of Internal Control Signals

1. For easy reference, the prefixes (Y = high level true, N = low level true) are ignored for purposes of alphabetical order, e.g., YEAM appears under the letter 'E'.
2. bus lines are abbreviated e.g., μD3 = microprocessor data bus bit 3, A2 is address bus bit 2.

SIGNAL TITLE	Nº	MEANING	ORIGIN SERVICE SHEET	COMP.	DEPENDENCY	DESTINATION SERV. SHEET	COMPONENT	PURPOSE
YACT	6	Active state	6A	AGU7 pin 6	YACT = EXT START + INRUN, EXT BREAK + NRUN, EX STOP)	6C 4A 4A 1A	1645AA U3 pin 3 A4 U20 pin 5 A4 U4 pins 4,5,13 A1 U9 pin 3	ACS o/p signal. Disables addr logic. Enables rate. μP port.
NADI	64	Enable internal address transmission to device	4D	1645ZA GND	Option 002 Address Driver Pod connected	4B	A4U44 pin 5	Enables address output latch
NADR		Address recall	4A	A4 U28 pin 12	μD4 latched by by YRCK3	4A	A4 U30 pins 1,4,12	NFAD, NLAD, NTAD logic
ADS1	–	Address select 1	4A	A4 U28 pin 2	μD0 latched by YRCK3	4A	A4 U20 pin 1	Address logic
ADS2	–	Address select 2	4A	A4 U28 pin 5	μD1 latched by YRCK3	4A	A4 U20 pin 2	Address logic
ADS3	–	Address select 3	4A	A4 U28 pin 6	μD2 latched by YRCK3	4A	A4 U20 pin 3	Address logic
YAUC	–	Auto cycle	6A	A6 U28 pin 12	μD5 latched by YRCK1	6B	A6 U11 pin 1	NSCR, YINC, NLOAD logic
YAVA	–	Address valid	4A	A4 U28 pin 9	μD3 latched by YRCK3	4A	A4 U8 pin 9	YLFAD, YLLAD YLTAD logic
YBRK	5	Break state	6A	A6 U7 pin 9	EXBREAK, YCSB, YEDB	6B 1A	A6 U20 pin 12 A1 U9 pin 4	YBRS logic, μP port.
NBRK	–	Break state	6A	A6 U7 pin 8	$\overline{\text{YBRK}}$	6B	A6 U18 pin 5	YACK, YDAV, YLEN logic.
NBPE	–	Base page enable	1C	A1 U25 pin 11	$\overline{\mu A0}$. $\overline{\mu A8}$	1C	A1 U7/8 pins 18,10	Enables operational RAMs
YCAD	63	Clock address i.e, Manual (FWD/BACK) clock for Ext Adr and Handshake modes	6A	A6 U20 pin 12	μD5 latched by YRCK2	6B	A6 U9 pin 3 A6 U17 pin 2 A6 U13 pin 13	YAC, YDAV logic YBRS logic
						4A	A4 U6 pin 12	YCLK logic
CE2	36	Chip enable signal for memory and operational RAMs	2A	A2 Q7 collector	Power up	2B 3 1C	A2 U21-28 pin 17 A3 U1-24 pin 17 A1 U7/8 pin 17	Memory enable Extended mem en. Operational RAM enable.
NCKD	–	Clock disabled	6A	A6 U20 pin 15	μD6 latched by YRCK2	6B 6B	A6 U18 pin 10 A6 U16 pin 9	YLATCH logic NLOAD logic
YCLK	50	Internal clock (Variable data rate, Internal/ man clock)	4A	A4 U7/6	EXT., CAD, IDL, ACT, CSI 1/2/3, rate gen.	6B	A6 U14 pin 13	YACK logic
YCSB	4	Clock state binary	1A	A1 U9 pin 6	μP	6A	A6 U12 pin 11	State logic
CSL1	–	Clock select 1	4A	A4 U28 pin 15	μD7 latched by YRCK3	4A	A4 U3 pin 1	Rate code to rate selector
CSL2	–	Clock select 2	4A	A4 U28 pin 16	μD6 latched by YRCK3	4A	A4 U3 pin 2	
CSL3	–	Clock select 3	4A	A4 U28 pin 10	μD5 latched by YRCK3	4A	A4 U3 pin 3	
NDAC	75	Data accepted (by device)	6C	1645AA U4 pin 12	Control pod input	6B	A6 Q1	DAV circuit enable
YDAV	72	Data valid	6B	A6 U20 pin 8	LATCH, NOR, 3WH. DAC, PDAV, DAV delay setting	6C	1645AA U1 pin 1	Control pod output
YDEN	27	Display enable	1C	A1 U10 pin 12	$\overline{\mu A6}$. $\overline{\mu A8}$. $\overline{\mu A7}$	1C 1D	A1 R48/45 A1 U22 pins 1, 2	Slows control clock Enables display
YEAM	61	External address mode selected	6A	A6 U21 pin 2	μD0 latched by YRCK2	6B 4B	A6 U11 pin 11, U23 pins 1,2 A6 U32 pin 4 A6 U30 pin 1 A6 U13 pin 12 A4 U44 pin 4 A4 U8 pin 3 A4 U30 pin 10	NEN 0–7 logic YLATCH logic YTRGOUT logic YBRS logic Disables address o/p latch Enables ext addr buffer Enables addr counter
YEDB	69	Enable data bus	6A	A6 U28 pin 7	μD0 latched by YRCK1	2B 3 6A	A2 U30 pins 9,10 A3 U1-24 pin 18 A6 U16 pin 1	Inhibits 8 bit data byte overwrite Inhibits memory outputs Resets signal latches in State Logic.
YEN	–	Enable data	6B	A10 U1 pin 5	EN1, EN2 (from control pod), EN3, Ext.4 (from rear panel)	6B	A6 U23 pin 5	NEN 0–7, NEN 8–15 logic
NEN 0–7	71	Enable data lines 7–0	6B	A6 U18 pin 11	EN, ACK, EAM, IDL, NOR	6B 6C 4D 4C 2C	A6 U17 pin 6, 27 pin 6 1645AA U6 pin 1, 2 1645ZA U17 pin 1 N.C. 1645A U1 pin 1, 2	NEN 8–15, YDAV logic DAV enable Address lines o/p enable – Data lines D0–7 o/p enable
NEN 8–15	73	Enable data lines 8–15	6B	A6 U17 pin 6	EN 0–7, 1024, 3WH	2C	1645A U1 pin 1, 2	Data lines D8–15 o/p enable
YEXCK	–	Ext CLOCK IN signal (filtered)	4A	A21 U1 pin 18	CLOCK IN	4A	A4 U46 pin 2	YCLK logic
EXBREAK	42	Ext BREAK IN signal (filtered)	4A	A21 U1 pin 12	BREAK IN	6A	A6 U2 pin 10	YBRK logic
EXSTART	40	Ext START IN signal (filtered)	4A	A21 U1 pin 14	START IN	6A	A6 U2 pin 1	YACT logic
EXSTOP	41	Ext STOP IN signal (filtered)	4A	A21 U1 pin 16	STOP IN	6A	A6 U8 pin 12	YIDL logic
NFAD	43	Fetch F-ADDR	4A	A4 U30 pin 3	NFAD = $\overline{\text{ADS3}}$.ADS2 ADS1 . NADR	4B	A4 U34/35 pins 1, 15	Enables F-ADDR bus driver
YFDH	52	Frequency different, high	4B	A4 U46 pin 8	Level change in any line of address bus (i.e. address change detection)	6B	A6 U31 pin 2	YLATCH logic
YFDL	53	Frequency different, low	4B	A4 U44 pin 8	NFDH stretched, low level if address changes at rates above 27 Hz	1B	A1 U pin 40	Interrupts addr bus PIA.
YICK	–	Internal clock	6B	A6 U14 pin 8	NOR, CLK, FDL, 3WH, RFD, CAD, BRK, MAN	6B	A6 U18 pin 9 A6 U10 pin 11 A6U16 pin 9 A6 U11 pin 3	YLATCH, YTRG OUT NSCR NLOAD NSCR, YINCR, YTRG OUT
YIDL	7	Idle state	6A	A6 U4 pin 9	EXSTOP, NSTOP, YEDB, YCSB, NSCR	6B 4B 4A 1A	A6U11 pin 5 A4 U31 pin 2 A4 U8 pin 13 A1 U9 pin 2	YACK, ENO–7, NSCR, NLOAD, YTRGOUT logic Disables ext addr buffer YCLK logic
YINCR	60	Increment address counter	6B	A6 U16 pin 4	YINCR = YICK. YLEN,YAUC,YLWAR	4B	A4 U38/39/40 pin 14	Clocks address counter
NIRQ	56	Interrupt request	1C	A1 U40 pin 4	Programming or operating error causes software to generate IRQ.	5B 6A	A5 U9 pin 7 A6 U1/2 pins 37, 38	
NLAD	44	Fetch L-ADDR	4A	A4 U30 pin 6	NLAD = $\overline{\text{ADS3}}$.ADS2 ADS1. $\overline{\text{NADR}}$	4B	A4 U24/25 pins 1, 15	Enables L-ADDR bus driver
YLATCH	70	Clock for output latches	6B	A6 U32 pins 3, 6	EAM, CKD, ICK, FDH	4B 2B	A4 U54/55, pin 11 A2 U16/17, pin 11	Clocks address output latch Clocks data output latch
YLEN[1]	–	Latch enable	6A	A6 U28 pin 15	μD6 latched by YRCK1	6B	A6 U30 pin 12	YLEN logic
YLEN	–	Latch enable	6B	A6 U30 pin 11	YLEN = YLEN[1], (NBRK + NMAN)	6B 6B 6B 6B	A6 U23 pin 10 A6 U13 pin 9 A6 U13 pin 4 A6 U10 pin 10	NSCR logic YINCR logic NLOAD logic NLOAD logic
YLFAD	46	Load F-ADDR latch	4A	A4 U31 pin 4	YLFAD = YAVA. $\overline{\text{ADS3}}$. ADS2. ADS1	4B	A4 U32/33 pin 9	Clocks F-ADDR latch
YLLAD	47	Load L-ADDR latch	4A	A4 U31 pin 10	YLLAD = YAVA $\overline{\text{ADS3}}$. ADS2. ADS1	4B	A4 U13/14/15 pin 9	Clocks L-ADDR latch
NLOAD	68	Load address counter	6B	A6 U10 pin 6	CKD, LEN, IDL, AUC LWA, ICK	4B	A4 U38/39/40 pin 11	Loads F-ADDR into addr counter
YLTAD	48	Load T-ADDR latch	4A	A4 U31 pin 13	YLTAD = YAVA, ADS3. ADS2. ADS1	4B	A4 U10/11/12 pin 9	Clocks T-ADDR latch
NLWA	54	Last word address (L-ADDR reached)	4B	A4 U27 pin 9	Address bus/L-ADDR co-incidence	6B 6B 6B	A6 U30 pin 8 A6 U16 pin 7 A6 U16 pin 11	NSCR logic YINCR logic NLOAD logic
NMAN	61	Manual clock Hi in Int. Addr Manual clock	4A	A4 U3 pin 5	NMAN = YACT + (CSL3. CSL2.CSL1)	6B	A6 U24 pin 1[1] U26 pin 1 U18 pin 4 U18 pin 2	YACK, YDAV logic NMAN enables YLEN
YNOR	–	"Normal mode" Hi in Int Addr (ext, man, Int clock) low in 2-/3-wire HS and external address	6A	A6 U20 pin 5	μD1 latched by YRCK2	6B	A6 U14 pin 12, U12 pin 1	YACK, YDAV logic
PAS 1	24		1C	A1 U23 pin 6	PAS 1 = μA (0,7,12,11,13).ϕ_2	5B 5A 5A	A5 U9 pin 6 A1 U1 pins 24, 22 A5 U2 pin 23	Enables RS 232C ACIA Enables HP-IB Interface PIA Inhibits HP-IB address PIA
PAS 2	23		1C	A1 U23 pin 8	μA(0,8,12,11,13).ϕ_2	5B 5A 5A	A5 U9 pin 10 A1 U1 pin 23 A5 U2 pins 22, 24	Enables RS 232C ACIA Inhibits HP-IB Interface PIA Enables HP-IB address PIA.
YPIA	28		1C	A1 U35 pin 2	YPIA=$\overline{\mu A0}$.$\overline{\mu A8}$.$\overline{\mu A7}$	1B 1A	A1 U11 pin 22 A1 U10 pin 22 A1 U9 pin 22	Enables data bus PIA Enables addr bus PIA Enables keyboard PIA
YRCK1	20	Register clock 1	1C	A1 U22 pin 8	YRCK1 = R/$\overline{W}$.A0. A9,A8,A7	6A	A6 U28 pin 9	Clocks latch for: YTTL, NWRD, YEDB, Y1024, YAUC, YLEN[1],
YRCK2	21	Register clock 2	1C	A1 U22 pin 6	YRCK2 = R/$\overline{W}$.A1. A9,A8,A7	6A	A6 U29 pin 9	Clocks latch for: YEAM, YNOR, Y3WH, NUP, YCAD, NCKD.
YRCK3	22	Register clock 3	1C	A1 U22 pin 11	YRCK3 = R/W.A2. A9,A8,A7	4A	A4 U28 pin 11	Clocks latch for data rate and address logic
NREST	35	Restart from power down	2A	A2 U31 pin 6	Negative pulse generated at switch on	1C	A1 U26 pin 1	Resets μP, and PIAs U9, 10, 11.
RFD	74	Device ready for data (input)	6C	1645AA U4 pin 9	Control pod input	6B	A6 U20 pin 4	YRFD logic
YRFD	1	Device ready for data	6B	A6 U20 pin 6	YRFD = RFD ⊗ PRFD	1A	A1 U9 pin 8	μP port
YRUN	2	Internal active state signal	1A	A1 U9 pin 7	μP	6A	A6 U2, pin 12	YACT logic
R/$\overline{W}_1$	26	Read (active high), write (active low)	1C	A1 U49 pin 34	μP	1C 1C 1B 1B	A1 U25 pin 9, 10 A1 U17 pin 13 A1 U11 pin 21 A1 U10 pin 21	Generates R/$\overline{W}_2$ Generates R/$\overline{W}_3$ Data bus PIA R/W Addrbus PIA R/W
R/$\overline{W}_2$	26	R/$\overline{W}_1$ buffered	1C	A1 U26 pin 8	R/$\overline{W}_2$ = R/$\overline{W}_1$	1C 1D 1A	A1 U7/8 pin 20 A1 U26/27 pin 20 A1 U9 pin 21	Operational RAM R/W Display RAM R/W Keyboard/Control PIA R/W
R/$\overline{W}_3$	17	R/$\overline{W}_1$ buffered	1C	A1 U17 pin 7	R/$\overline{W}_3$ = R/$\overline{W}_1$	5B 5A 5A	A5 U9 pin 13 A5 U1 pin 21 A5 U2 pin 21	RS 232C ACIA R/W HP-IB Interface PIA R/W HP-IB Address PIA R/W
YSTOP	3	Internal stop	1A	A1 U9 pin 6	μP	6A	A6 U8 pin 4	YIDL logic
NSCR	–	Single cycle ready	6B	A6 U29 pin 8	ICK, AUC, LWA, UP, LEN, IDL	6A	A6 U5 pin 9	YIDL hold-off
NTAD	45	Fetch T-ADDR	4A	A4 U30 pin 11	NTAD = ADS3.$\overline{\text{ADS2}}$. ADS1.NADR	4B	A4 U22/23 pins 1, 15	Enables T-ADDR bus driver
NTRG	55	Trigger (T-ADDR)	4B	A4 U20 pin 9	Address bus/T-ADDR fetch coincidence	6B	A6 U11 pin 13	YTRG OUT logic
YTRGOUT	67	Input to TRIG OUT Buffer	6B	A6 U30 pins 3, 6	TRG, EAM, IDL, ICK, LATCH	4A	A21 U1 pin 11	TRIG OUT buffer input
YTTL	57	TTL output levels	6A	A6 U28 pin 2	μD0 latched by YRCK1	7	A7 U1 pins 1, 2	Applies TTL level to V_{IL}, V_{IH} regulators.
UAO	18	Buffered μP Addr Bus Bit 0	1C	A1 U17 pin 14	μA0	5B 5A	A5 U9 pin 11 A6 U1/2 pin 36	Puts RS 232C ACIA from Control/Status Mode to send/Receive Mode Selects control registers in HP-IB PIA's.
UA1	19	Buffered μP Addr Bus Bit 1	1C	A1 U17 pin 12	μA1	6B 5A	A6 U9 pin 9 A6 U1/2 pin 35	Inhibits RS 232C ACIA Selects B in HP-IB PIA's.
NUP	62	Address counter up	6A	A6 U29 pin 10	μD4 latched by YRCK2	4B 6B	A4 U38/39/40 pin 5 A6 U30 pin 10	Switches address counter to count up. Enables NLWA in NSCR logic.
NWRD	58	Write data	6A	A6 U29 pin 6	μD1 latched by YRCK1	3 2B	A3 U1-24 pin 20 A2 U21-28 pin 20	Puts memory into write mode
Y1024	60	1024 x 8 bit operation (4096 x 8 bit with Opt. 001) i.e. 8-bit data bus selected.	6A	A6 U28 pin 10	μD4 latched by YRCK1	6B 2B	A6 U1 pin 0 A2 U10 pin 11	Inhibits NEN 8–15 (if Y3WH low) Switches terminator for 8 bit operation
N2K	11	2 K memory (not used)	3	A3 R1	Wire link	1B	A1 U10 pin 16	μP port
N4K	12	4 K memory (Option 001)	3	A3 R1	Wire link	1B	A1 U10 pin 17	μP port
Y3WH	–	3-wire handshake	6A	A6 U29 pin 7	μD2 latched by YRCK2	6B 6B	A6 U25 pin 11 A6 U16 pin 11 A6 U27 pins 3, 12 A6 U8 pin 10 A6 U16 pin 8	YACK logic YDAV logic NEN 8–15 logic
ϕ_2	15	Control clock	1C	A1 U50 pin 5	Y DEN	1C 1C 1A, B	A1 U49 pin 36 A1 U15 pin 6 A1 U9/10/11 pin 26	Enables μP data bus Enables μP addr, bus decoder Enables control/key board PIA, addr bus PIA, data bus PIA
ϕ_2'	16	Control clock buffered	1C	A1 U17 pin 9	ϕ_2	6B 5A	A6 U9 pin 14 A6 U1/2 pin 25	Enables RS 232C ACIA Enables HP-IB PIA's.

SERIAL NUMBERS 00110–00144: W2 NOT FITTED, FOR DSA,
REMOVE WIRED CONNECTION ON BACK OF BOARD FROM U19 PIN 6.



DSA Routine 2 SH = 0003	
5004A	8170A BD AY A1 Testpoint
START, STOP	Address Bit A15
CLOCK	CLK
GROUND	GND

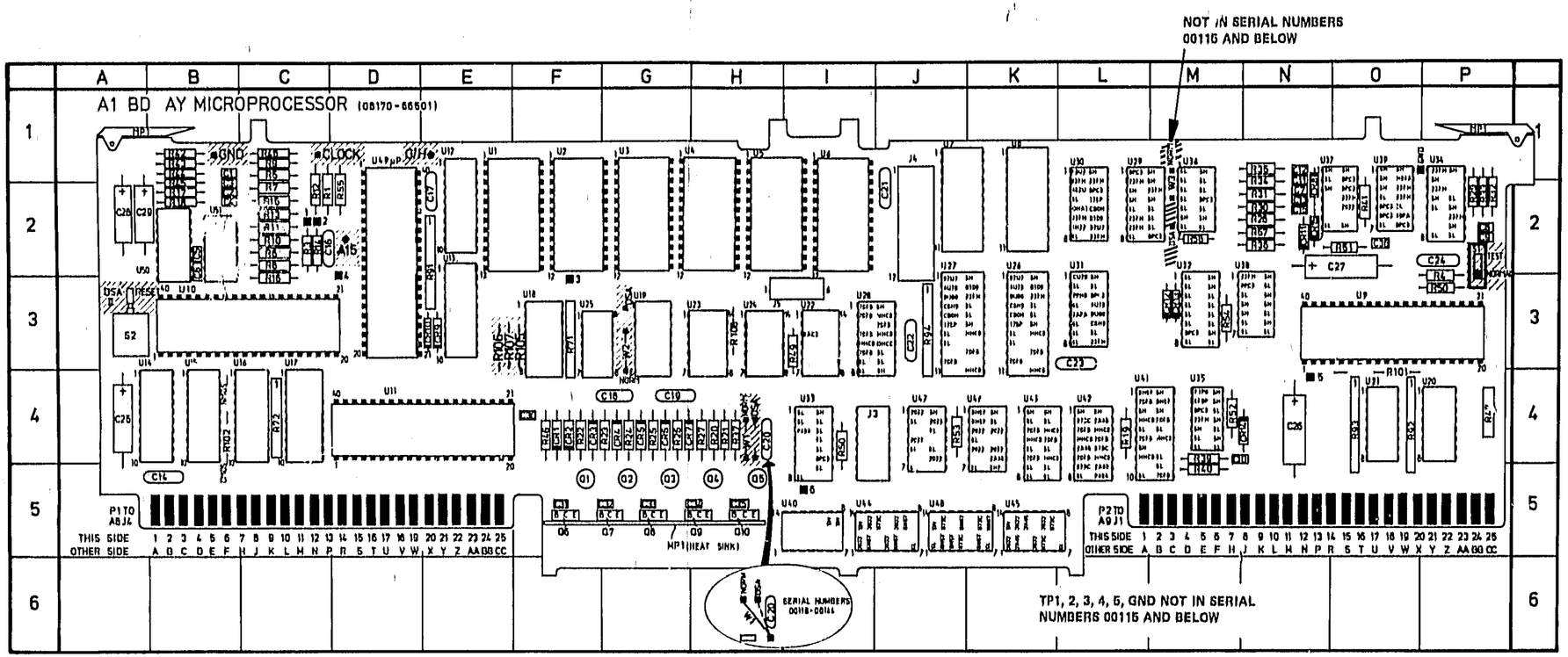
Set the 8170A as follows:

Set jumper A1W1 to DSA, remove jumper A1W2 (serial numbers 00115 and below) or set to DSA (serial numbers 00116 and above), set A1S1 to T, press A1S2 to R.

1A-1

A1 BD AY MICROPROCESSOR (FOR A10, A11 SEE SERVICE SHEET 1E)

REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC
C1	B-1	C17	E-2	C33	G-5	CR13	M-3	Q10	H-5	R17	B-2	R33	P-2	R50	I-4	R106	E-3	U12	E-2	U28	J-3	U44	J-4
C2	B-2	C18	G-4	C34	H-5	CR14	M-4	R1	C-2	R18	B-2	R34	N-2	R51	O-.	R107	E-3	U13	E-3	U29	L-2	U45	K-5
C3	B-1	C19	G-4	C35	H-5	CR15	N-2	R3	C-2	R19	L-4	R35	N-1	R52	M-4	R108	H-3	U14	B-4	U30	L-2	U46	K-4
C4	B-2	C20	H-4	C36	O-2	J3	J-4	R4	P-2	R20	H-4	R36	N-2	R53	J-4	S1	P-2	U15	B-4	U31	L-3	U47	J-4
C5	B-2	C21	J-2	CR1	F-4	J4	J-2	R5	C-1	R21	H-4	R37	H-4	R54	M-3	S2	A-3	U16	C-4	U32	M-3	U48	J-4
C6	B-2	C22	J-3	CR2	F-4	J5	I-3	R6	C-2	R22	F-4	R39	M-4	R55	D-2	U1	E-2	U17	C-4	U33	I-4	U49	D-2
C7	N-2	C23	L-3	CR3	F-4	MP1	A-1	R7	C-2	R23	F-4	R40	M-5	R57	N-2	U2	F-2	U18	F-3	U34	P-2	U50	B-2
C8	P-2	C24	P-2	CR4	G-4	Q1	F-5	R8	C-2	R24	G-4	R41	O-2	R71	F-3	U3	G-2	U19	G-3	U35	M-4	U51	B-2
C9	P-2	C25	A-4	CR5	G-4	Q2	G-5	R9	C-1	R25	G-4	R42	B-1	R72	C-4	U4	H-2	U20	P-4	U36	M-2	W1	H-4
C10	M-4	C26	N-4	CR6	G-4	Q3	G-5	R10	C-2	R26	G-4	R43	B-1	R91	E-2	U5	H-2	U21	O-4	U37	O-2	W2	G-3
C11	N-2	C27	O-2	CR7	G-4	Q4	H-5	R11	C-2	R27	H-4	R44	B-1	R92	O-4	U6	I-2	U22	I-3	U38	N-3		
C12	N-1	C28	A-2	CR8	N-2	Q5	H-5	R12	C-2	R28	N-2	R45	B-2	R93	O-4	U7	J-2	U23	H-3	U39	O-2		
C13	N-2	C29	A-2	CR9	E-3	Q6	F-5	R13	C-2	R29	P-2	R46	F-4	R94	J-3	U8	K-2	U24	H-3	U40	I-5		
C14	B-5	C30	F-4	CR10	E-3	Q7	G-5	R14	C-2	R30	N-2	R47	P-4	R101	O-4	U9	O-3	U25	F-3	U41	L-4		
C15	N-2	C31	F-5	CR11	N-2	Q8	G-5	R15	C-2	R31	N-2	R48	C-1	R102	B-4	U10	B-3	U26	K-3	U42	L-4		
C16	C-2	C32	G-5	CR12	M-3	Q9	H-5	R16	C-3	R32	P-2	R49	I-3	R105	F-3	U11	D-4	U27	J-3	U43	K-4		

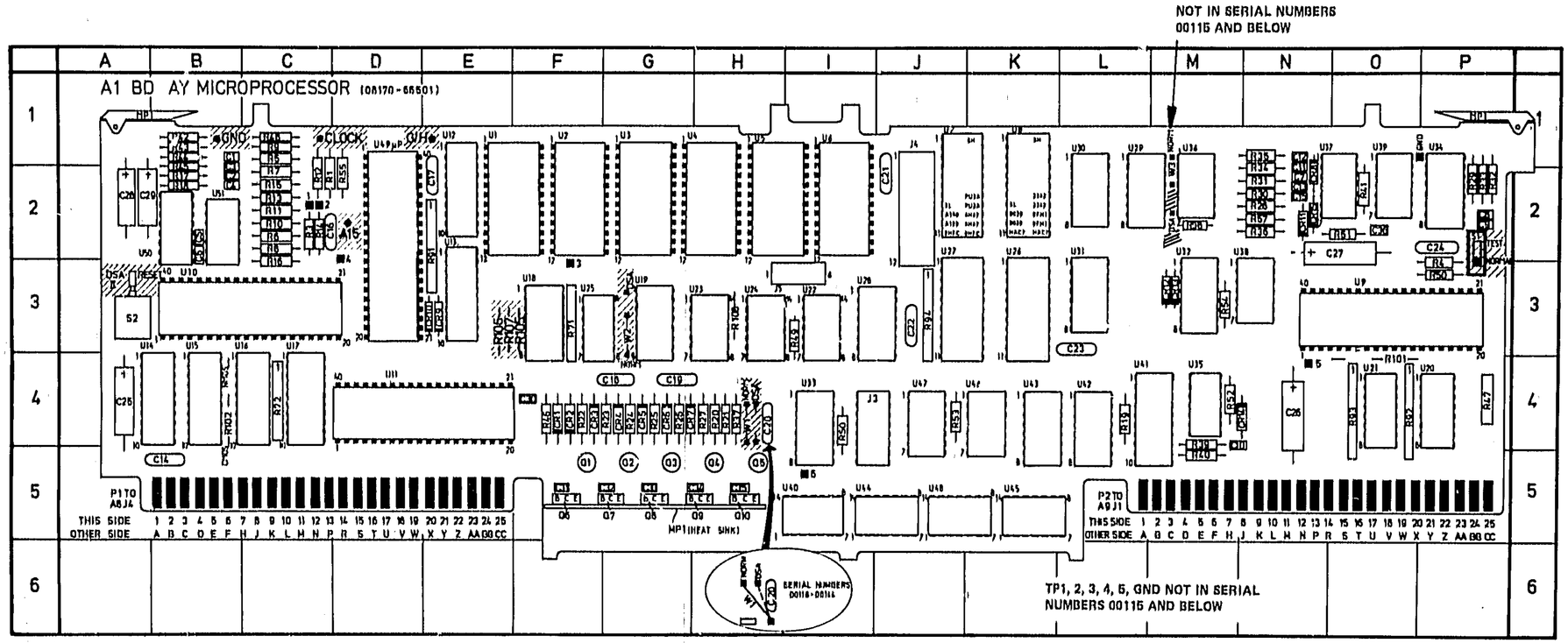


DSA Routine D SH = AH7P	
5004A	8170A BD AY A1 Testpoint
START, STOP	G/H
CLOCK	CLK
GROUND	GND

Set the 8170A as follows:

Jumper A1W3 to DSA (serial numbers 1738G00116 and higher), alternatively lift U36 pin 11 from socket and connect to + 5 V at U36 pin 14 (serial numbers 1738G00115 and below),
Set A1 S1 to T,
press A1 S2 to R,
press the D key on the front panel.

REF DESIG	GRID LOC
C1	B-1
C2	B-2
C3	B-1
C4	B-2
C5	B-2
C6	B-2
C7	N-2
C8	P-2
C9	P-2
C10	M-4
C11	N-2
C12	N-1
C13	N-2
C14	B-5
C15	N-2
C16	C-2
C17	E-2
C18	G-4
C19	G-4
C20	H-4
C21	J-2
C22	J-3
C23	L-3
C24	P-2
C25	A-4
C26	N-4
C27	O-2
C28	A-2
C29	A-2
C30	F-4
C31	F-5
C32	G-5
C33	G-5
C34	H-5
C35	H-5
C36	O-2
CR1	F-4
CR2	F-4
CR3	F-4
CR4	G-4
CR5	G-4
CR6	G-4
CR7	G-4
CR8	N-2
CR9	E-3
CR10	E-3
CR11	N-2
CR12	M-3
CR13	M-3
CR14	M-4
CR15	N-2
J3	J-4
J4	J-2
J5	I-3
MP1	A-1
Q1	F-5
Q2	G-5
Q3	G-5
Q4	H-5
Q5	F-5
Q6	F-5
Q7	G-5
Q8	G-5
Q9	H-5
Q10	H-5
R17	B-2
R18	B-2
R19	L-4
R20	H-4
R21	H-4
R22	F-4
F23	F-4
R24	G-4
R25	G-4
R26	G-4
R27	H-4
R28	N-2
R29	P-2
R30	N-2
R31	N-2
R32	P-2
R33	P-2
R34	N-2
R35	N-1
R36	N-2
R37	H-4
R39	M-4
R40	M-5
R41	O-2
R42	B-1
R43	B-1
R44	B-1
R45	B-2
R46	F-4
R47	P-4
R48	C-1
R49	I-3
R50	I-4
R51	O-2
R52	M-4
R53	N-1
R54	J-4
R55	M-3
R56	D-2
R57	N-2
R71	F-3
R72	C-4
R91	E-2
R92	O-4
R93	O-4
R94	J-3
R101	O-4
R102	B-4
R105	F-3
R106	E-3
R107	E-3
R108	H-3
S1	P-2
S2	A-3
U1	E-2
U2	F-2
U3	G-2
U4	H-2
U5	H-2
U6	I-2
U7	J-2
U8	K-2
U9	O-3
U10	B-3
U11	D-4
U12	E-2
U13	E-3
U14	B-4
U15	B-4
U16	C-4
U17	C-4
U18	F-3
U19	G-3
U20	P-4
U21	O-4
U22	I-3
U23	H-3
U24	H-3
U25	F-3
U26	K-3
U27	J-3
U28	J-3
U29	L-2
U30	L-2
U31	L-3
U32	M-3
U33	I-4
U34	P-2
U35	M-4
U36	M-2
U37	O-2
U38	N-3
U39	O-2
U40	I-5
U41	L-4
U42	L-4
U43	K-4
U44	J-4
U45	K-5
U46	K-4
U47	J-4
U48	J-4
U49	D-2
U50	B-2
U51	B-2
W1	H-4
W2	G-3



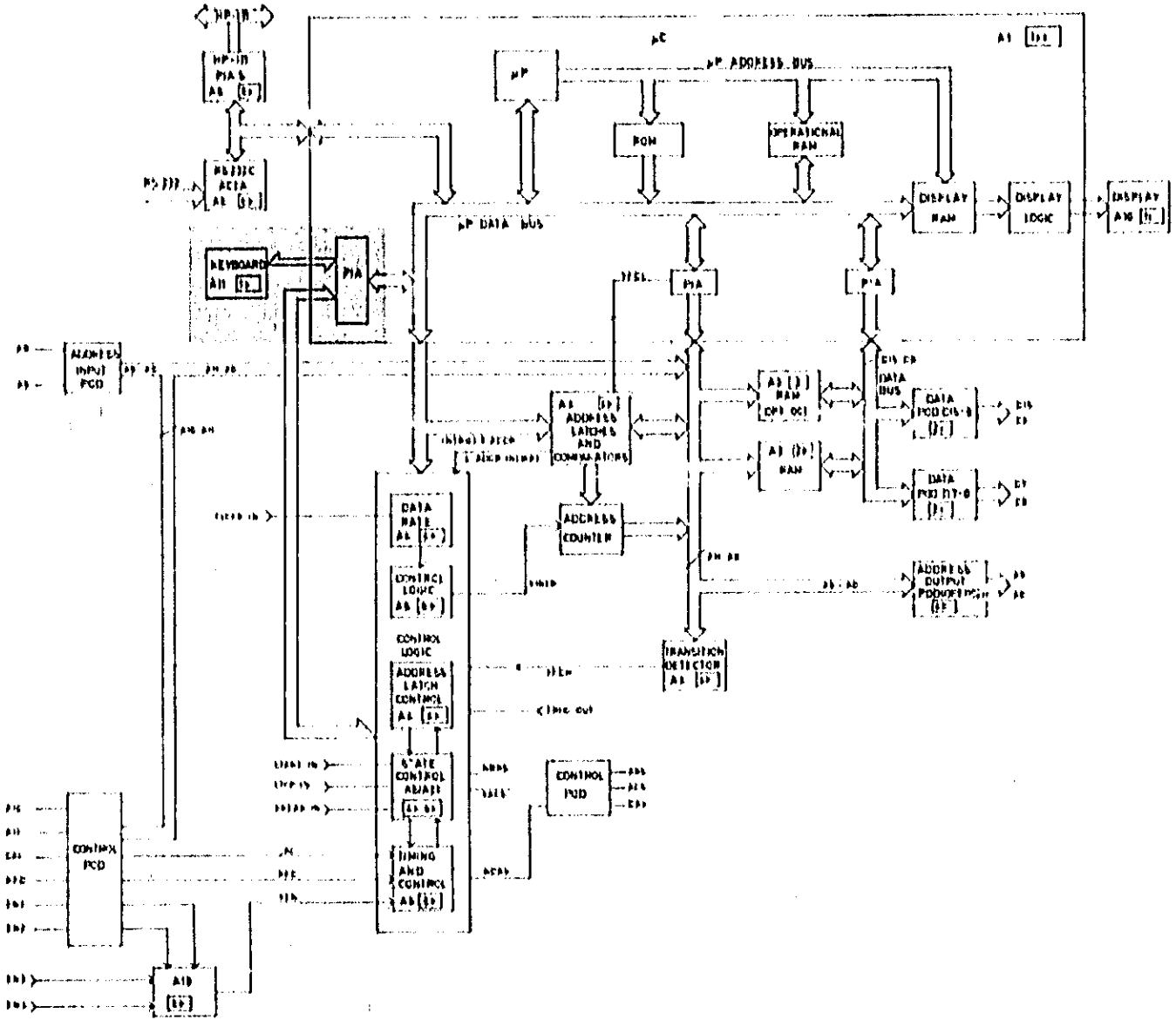
DSA Routine E SH = 2PP4	Set the 8170A as follows:
6004A 8170A BD AY A1 Testpoint	all jumpers in NORMAL position, set A1S1 to T, press A1S2 to R, press the E key on the front panel.
START, STOP — G/H	
CLOCK — CLK	
GROUND — GND	

1A-3

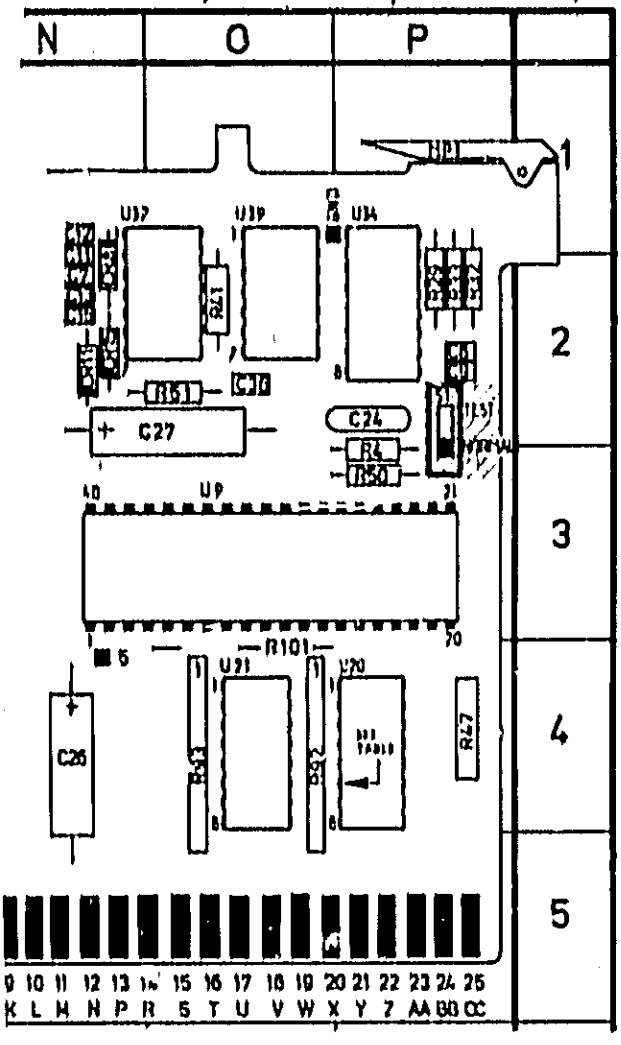
A1 BD AY MICROPROCESSOR (FOR A10, A11 SEE SERVICE SHEET 1E)

REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC
C1	B-1	C17	E-2	C33	G-5	CR13	M-3	Q10	H-5	R17	B-2	R33	P-2	R60	I-4	R106	E-3	U12	E-2	U28	J-3	U44	J-4
C2	B-2	C18	G-4	C34	H-5	CR14	M-4	R1	C-2	R18	B-2	R34	N-2	R61	O-2	R107	E-3	U13	E-3	U29	L-2	U45	K-5
C3	B-1	C19	G-4	C35	H-5	CR15	N-2	R3	C-2	R19	L-4	R35	N-1	R62	M-4	R108	H-3	U14	B-4	U30	L-2	U46	K-4
C4	B-2	C20	H-4	C36	O-2	J3	J-4	R4	P-2	R20	H-4	R36	N-2	R63	J-4	S1	P-2	U15	B-4	U31	L-3	U47	J-4
C5	B-2	C21	J-2	CR1	F-4	J4	J-2	R5	C-1	R21	H-4	R37	H-4	R64	M-3	S2	A-3	U16	C-4	U32	M-3	U48	J-4
C6	B-2	C22	J-3	CR2	F-4	J5	I-3	R6	C-2	R22	F-4	R38	M-4	R65	D-2	U1	E-2	U17	C-4	U33	I-4	U49	D-2
C7	N-2	C23	L-3	CR3	F-4	MP1	A-1	R7	C-2	F23	F-4	R40	M-5	R67	N-2	U2	F-2	U18	F-3	U34	P-2	U50	B-2
C8	P-2	C24	P-2	CR4	G-4	Q1	F-5	R8	C-2	R24	G-4	R41	O-2	R71	F-3	U3	G-2	U19	G-3	U35	M-4	U51	B-2
C9	P-2	C25	A-4	CR5	G-4	Q2	G-5	R9	C-1	R25	G-4	R42	B-1	R72	C-4	U4	H-2	U20	P-4	U36	M-2	W1	H-4
C10	M-4	C26	N-4	CR6	G-4	Q3	G-5	R10	C-2	R26	G-4	R43	B-1	R91	E-2	U5	H-2	U21	O-4	U37	O-2	W2	G-3
C11	N-2	C27	O-2	CR7	G-4	Q4	H-5	R11	C-2	R27	H-4	R44	B-1	R92	O-4	U6	I-2	U22	I-3	U38	N-3		
C12	N-1	C28	A-2	CR8	N-2	Q5	H-5	R12	C-2	R28	N-2	R45	B-2	R93	O-4	U7	J-2	U23	H-3	U39	O-2		
C13	N-2	C29	A-2	CR9	E-3	Q6	F-5	R13	C-2	R29	P-2	R46	F-4	R94	J-3	U8	K-2	U24	H-3	U40	I-5		
C14	B-5	C30	F-4	CR10	E-3	Q7	G-5	R14	C-2	R30	N-2	R47	P-4	R101	O-4	U9	O-3	U25	F-3	U41	L-4		
C15	N-2	C31	F-5	CR11	N-2	Q8	G-5	R15	C-2	R31	N-2	R48	C-1	R102	B-4	U10	B-3	U26	K-3	U42	L-4		
C16	C-2	C32	G-5	CR12	M-3	Q9	H-5	R16	C-3	R32	P-2	R49	I-3	R105	F-3	U11	D-4	U27	J-3	U43	K-4		

SERVICE SHEET 1A LOCALIZER



A1 BD AY MICROPROCESSOR

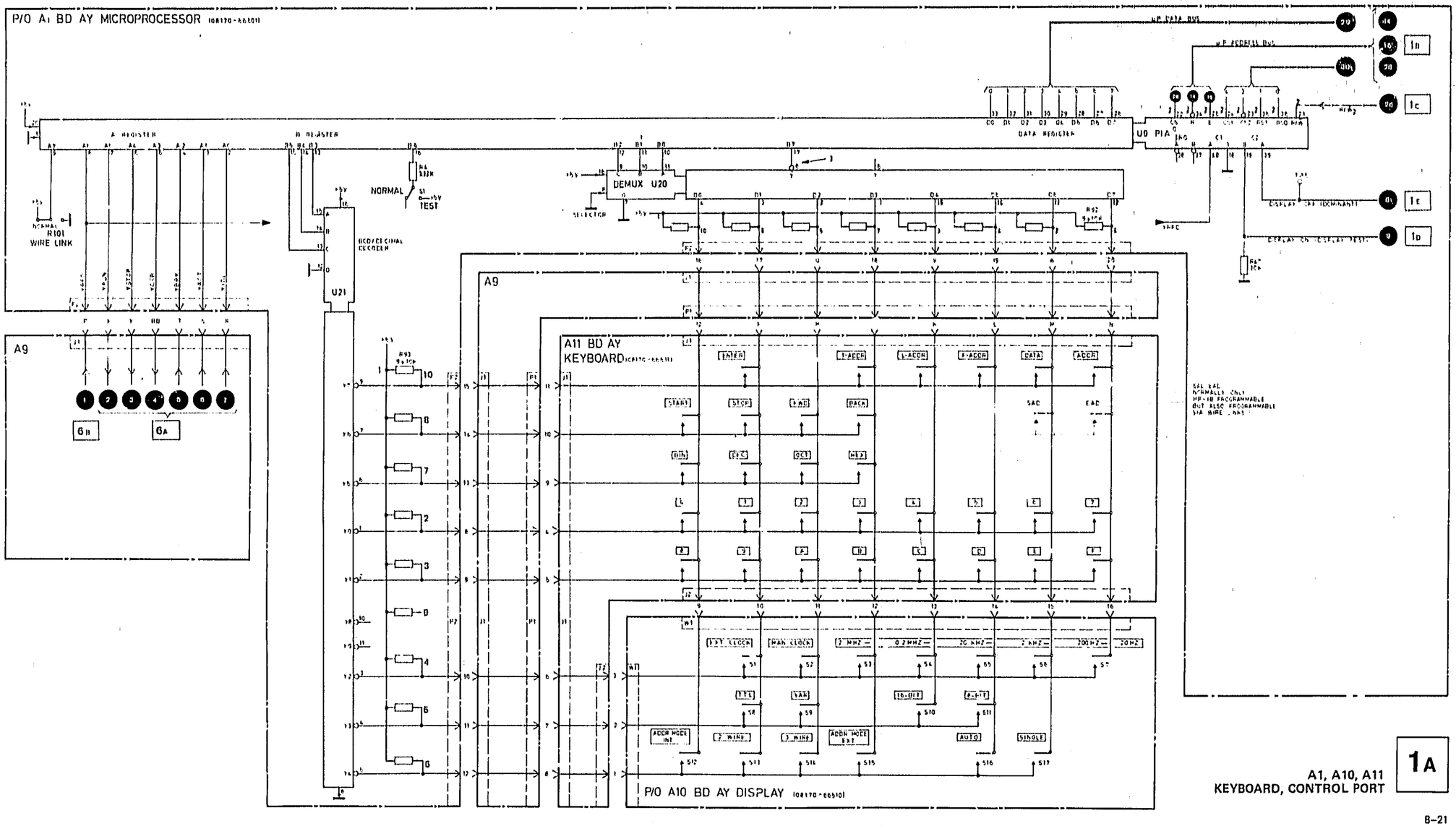


KEY	SIGNATURE	KEY	SIGNATURE	KEY	SIGNATURE
RUN	H96H	F ADDR	832P	A	CP01
16 BIT	U967	F ADDR	H761	B	AP01
INT ADDR	C48P	L ADDR	F16P	C	A616
EXT ADDR	830A	ADDR	616C	D	U33A
AUTO	77C6	DATA	AHHP	E	14PU
SINGLE	6H7A	ENTER	A2F3	F	U96C
TTL	0309				
VAR	904C	0	66U0	START	OPCH
2WIRE	4707	1	U6H3	STOP	P000
3WIRE	PH60	2	8611	FWD	70HP
EXT (clock)	3661	3	6U77	BACK	670P
MAN	7F0H	4	4FCA		
2 MHz	1F73	5	6781	HEX	H307
2 MHz					
2 MHz	H264	6	78611	DEC	4U37
20 kHz					
20 kHz	2U69	7	89CH	OCT	C501
2 kHz					
2 kHz	P2H6	8	4667	BIN	P7UP
200 Hz					
200 Hz	0461	9	P473		
20 Hz					

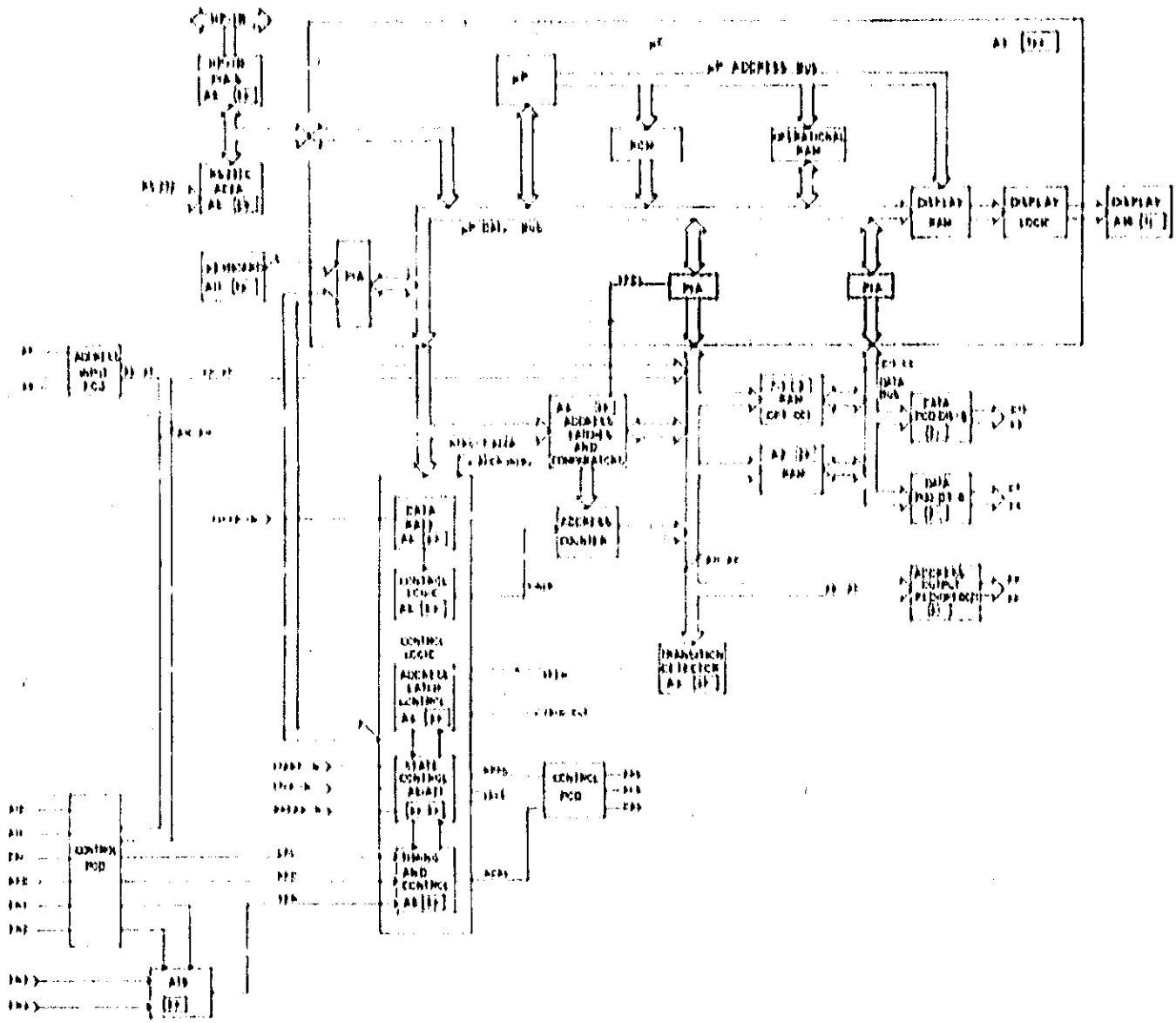
DSA Routine 3 SH = C788	Set the 8170A as follows:
5004A 8170A BD AY A1 Testpoint START, STOP — G/H CLOCK — CLK GROUND — GND	all jumpers in the NORMAL position, set A1 S1 to T, press A1 S2 to DSAII. Connect the 5004A's data probe to A1U20 pin 6 Press each front panel control in turn and verify the signatures listed in the table.

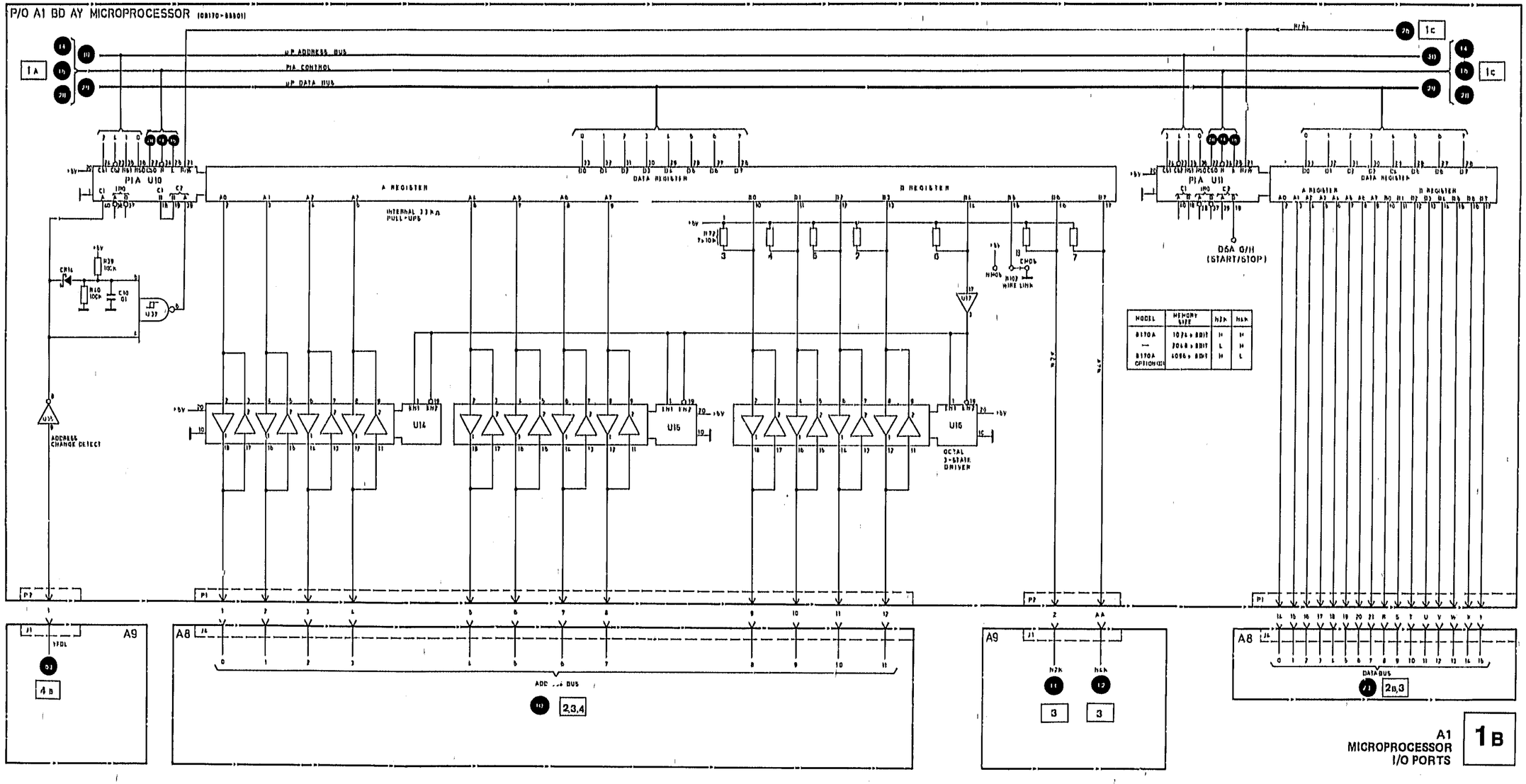
1A-4

A1 BD AY MICROPROCESSOR

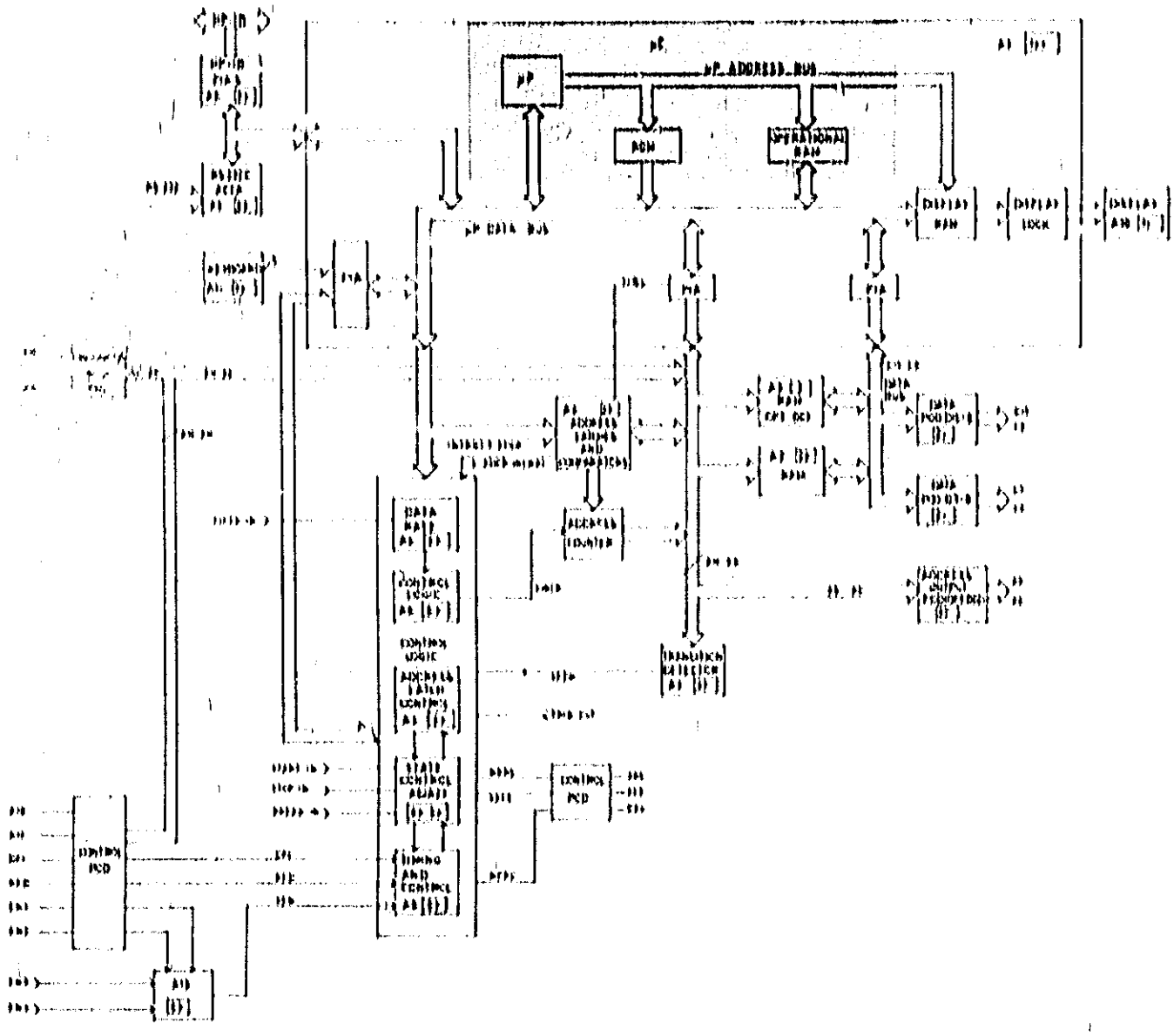

P/O A1 BD AY MICROPROCESSOR
A REGISTER
B REGISTER
R101
WIRE LINK
NORMAL
TEST
BCD/DECIMAL DECODER
U21
DEMUX U20
DATA REGISTER
U9 PIA
A9
A11 BD AY
KEYBOARD
P/O A10 BD AY DISPLAY
6B
6A
1A
A1, A10, A11
KEYBOARD, CONTROL PORT

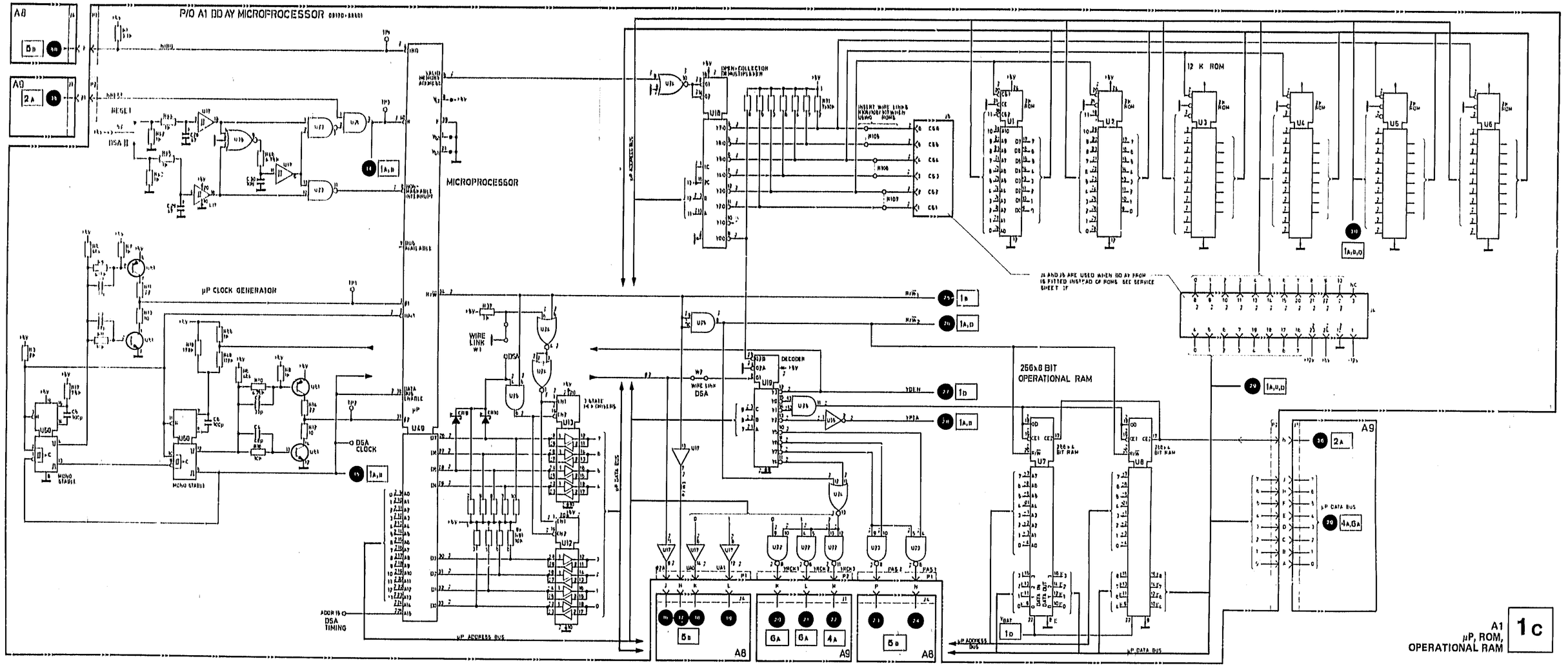
SERVICE SHEET 1b LOCALIZER



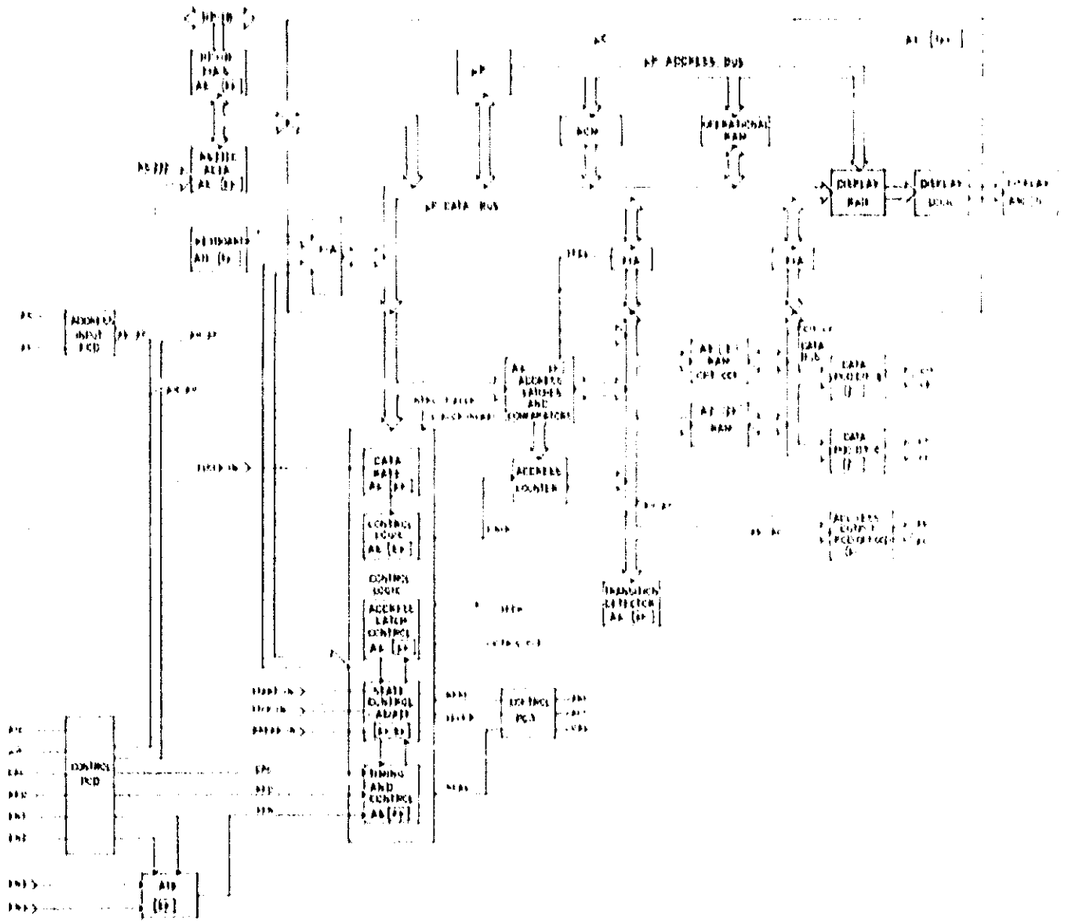

P/O A1 BD AY MICROPROCESSOR (08170-66501)
µP ADDRESS BUS
PIA CONTROL
µP DATA BUS
PIA U10
PIA U11
DATA REGISTER
A REGISTER
B REGISTER
INTERNAL 33KΩ PULL-UPS
D6A O/H (START/STOP)
ADDRESS CHANGE DETECT
OCTAL 3-STATE DRIVER
U14
U15
U16
U17
MODEL
MEMORY SIZE
8170A
8170A OPTION 020
A9
A8
DATA BUS
ADDRESS BUS
A1 MICROPROCESSOR I/O PORTS
1B
8-23

SERVICE SHEET 1a LOCALIZER




P/O A1 DD AY MICROPROCESSOR
MICROPROCESSOR
μP CLOCK GENERATOR
WIRE LINK W1
WIRE LINK DSA
DECODER
256 x 8 BIT OPERATIONAL RAM
12 K ROM
OPEN-COLLECTOR MULTIPLEXER
INSERT WIRE LINKS WHEN ROMS FITTED
JA AND JB ARE USED WHEN DD AY PROM IS FITTED INSTEAD OF ROMS SEE SERVICE SHEET 1F
DSA CLOCK
DSA TIMING
μP ADDRESS BUS
μP DATA BUS
μP ADDRESS BUS
μP DATA BUS
A8
A9
A8
A9
A1
μP, ROM, OPERATIONAL RAM
1c
DSA ROUTINE
8–26

SERVICE SHEET 1b LOCALIZER

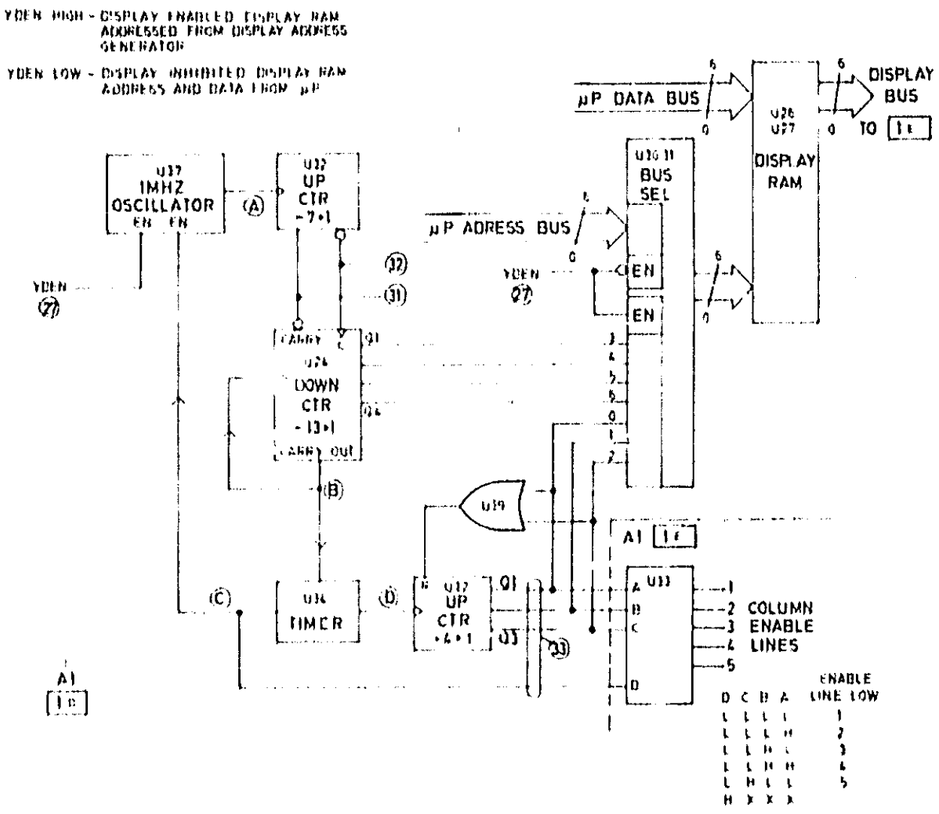


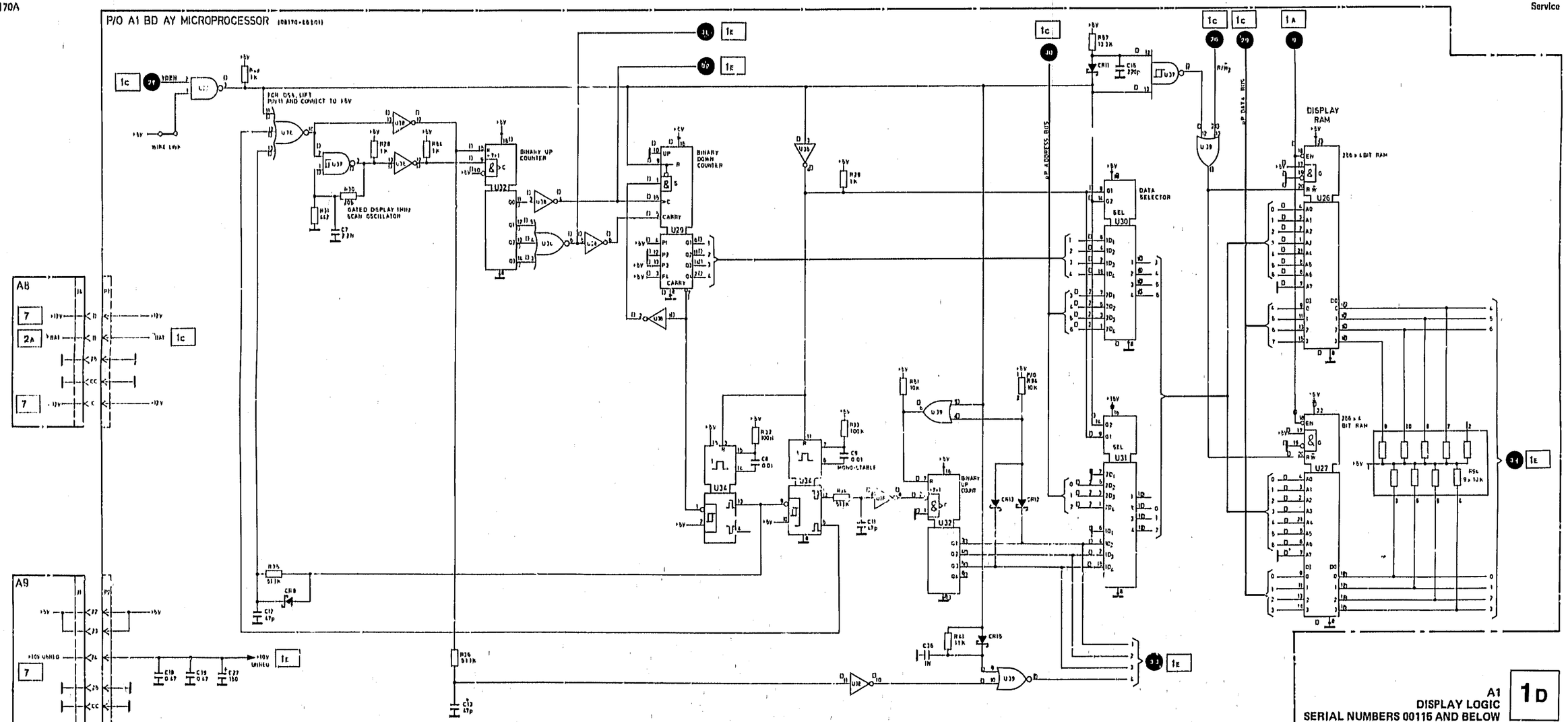
8-1D-1 DISPLAY LOGIC

8-1D-2 Data for the display is written into the display RAM U26, 27 from the μP. Signal YDEN is false during this operation so that the RAM is addressed and in the read state during this activity. When YDEN is true, the RAM address is generated by the circuitry on this schematic, and the RAM outputs is data onto the display bus. At the same time, Column Enable signals are generated so that appropriate parts of the display are activated synchronously with the data.

YDEN HIGH - DISPLAY ENABLED DISPLAY RAM ADDRESSED FROM DISPLAY ADDRESS GENERATOR

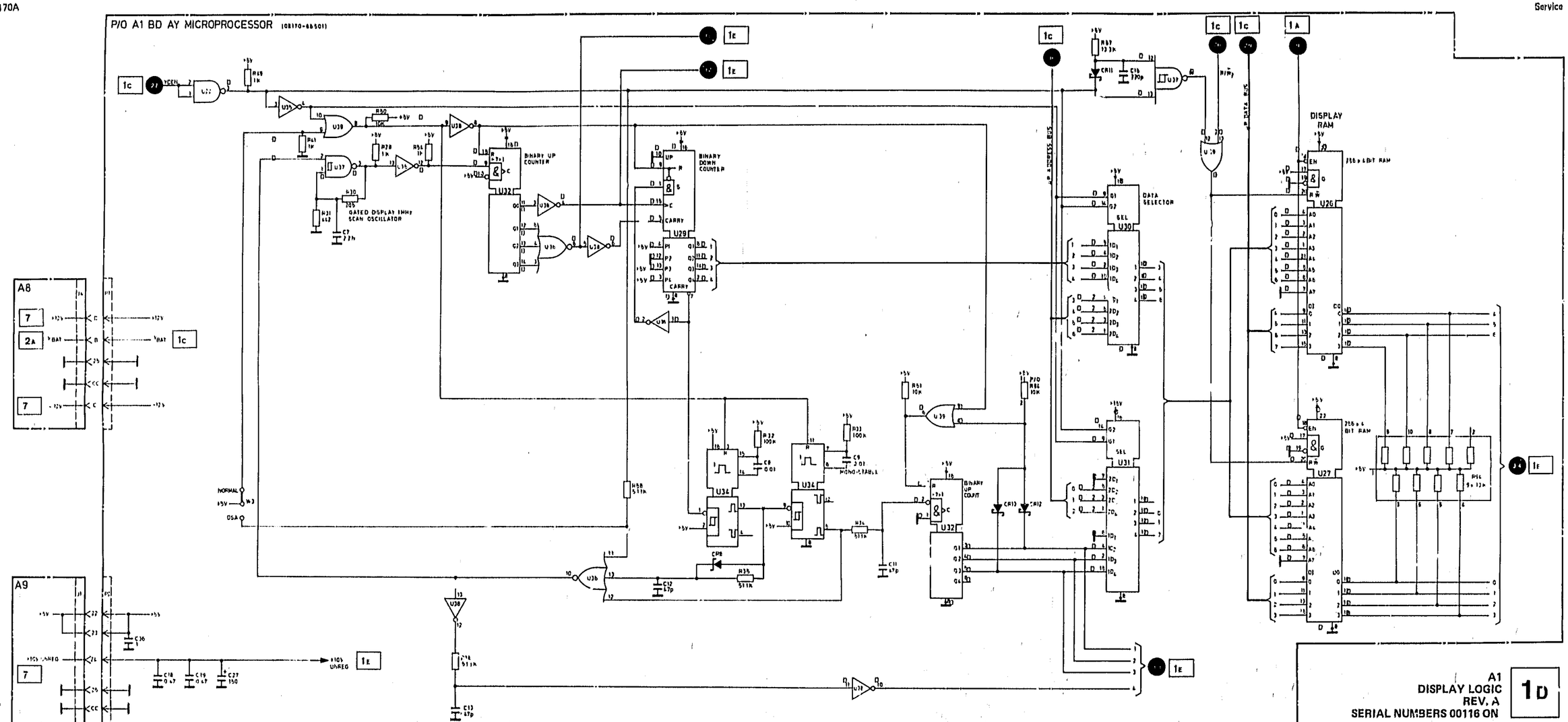
YDEN LOW - DISPLAY INHIBITED DISPLAY RAM ADDRESS AND DATA FROM μP





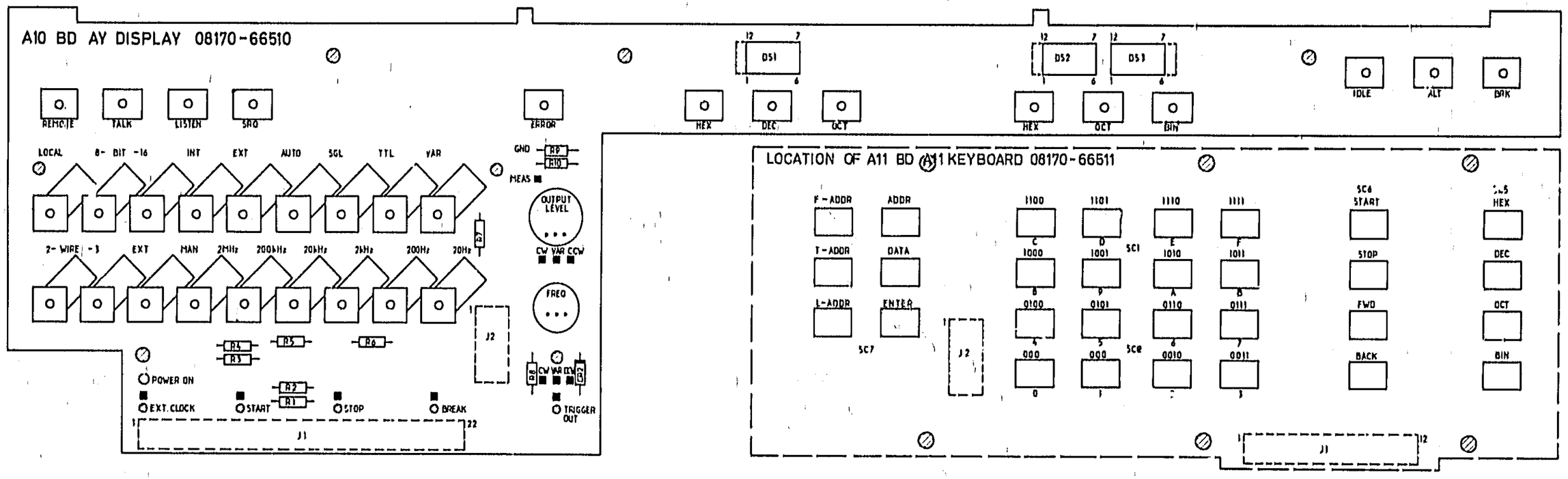
A1
DISPLAY LOGIC
SERIAL NUMBERS 00115 AND BELOW

1D

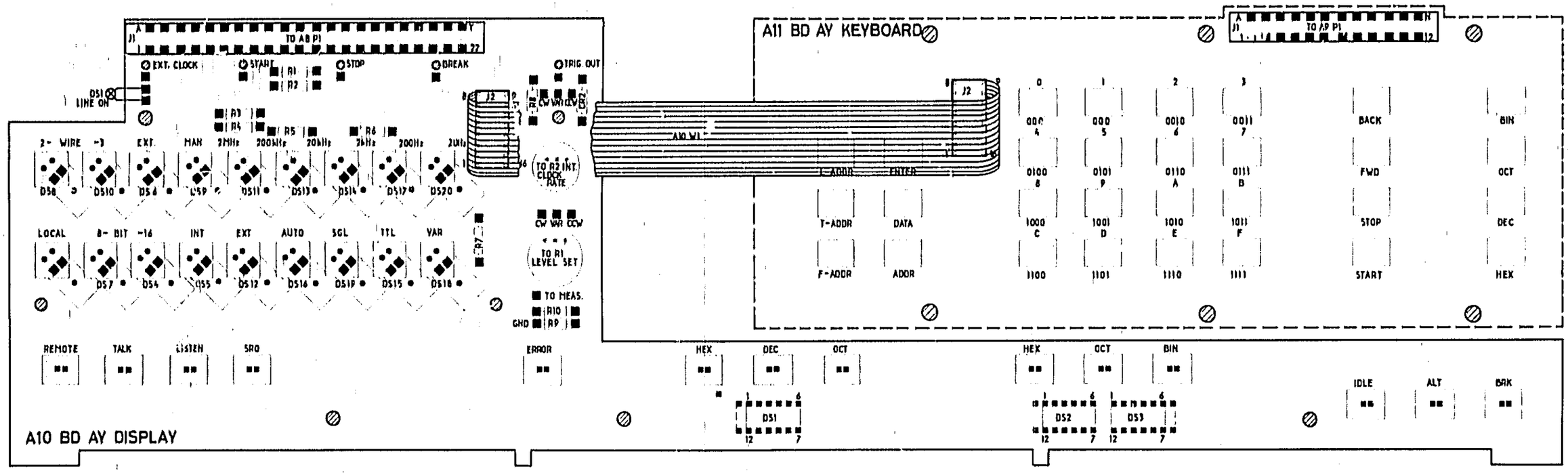


A1
DISPLAY LOGIC
REV. A
SERIAL NUMBERS 00116 ON

1D

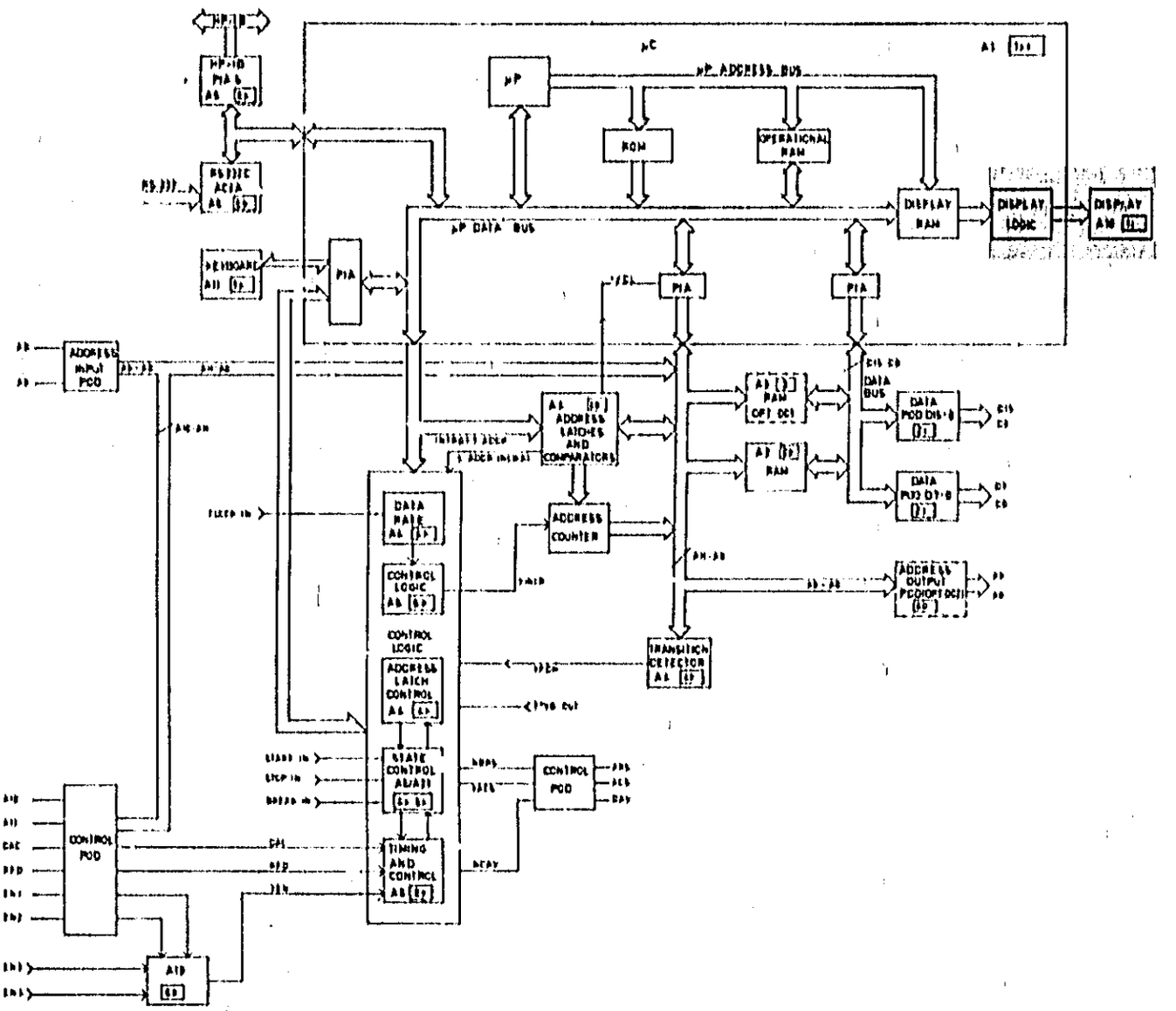


1E-1 A10 BD AY DISPLAY, A11 BD AY KEYBOARD
AS SEEN WITH FRONT PANEL REMOVED



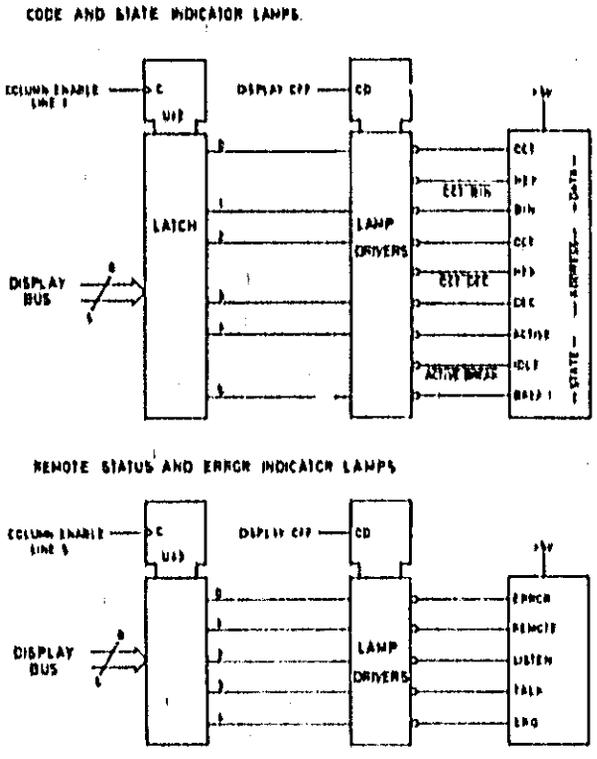
1E-2 A10 BD AY DISPLAY, A11 BD AY KEYBOARD
AS SEEN FROM INSIDE INSTRUMENT

SERVICE SHEET 1E LOCALIZER



8–1E–1 CODE AND STATE INDICATOR LAMPS

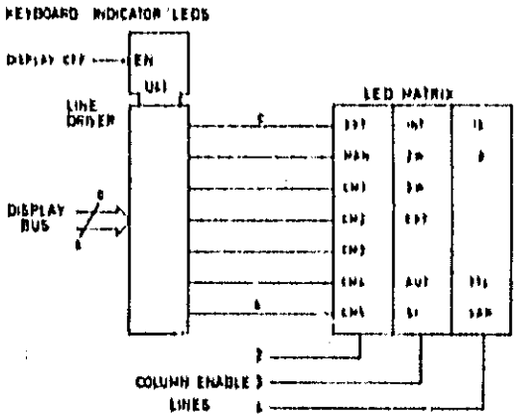
8–1E–2 Code and state indicator lamps depend on the status of the display bus at the low/high transition of Column Enable lines 1 or 5, as shown below:



As the display bus has only six lines, the switching signals for the HEX lamps and IDLE lamp are generated by the NOR function of OCT/BIN and ACTIVE/IDLE.

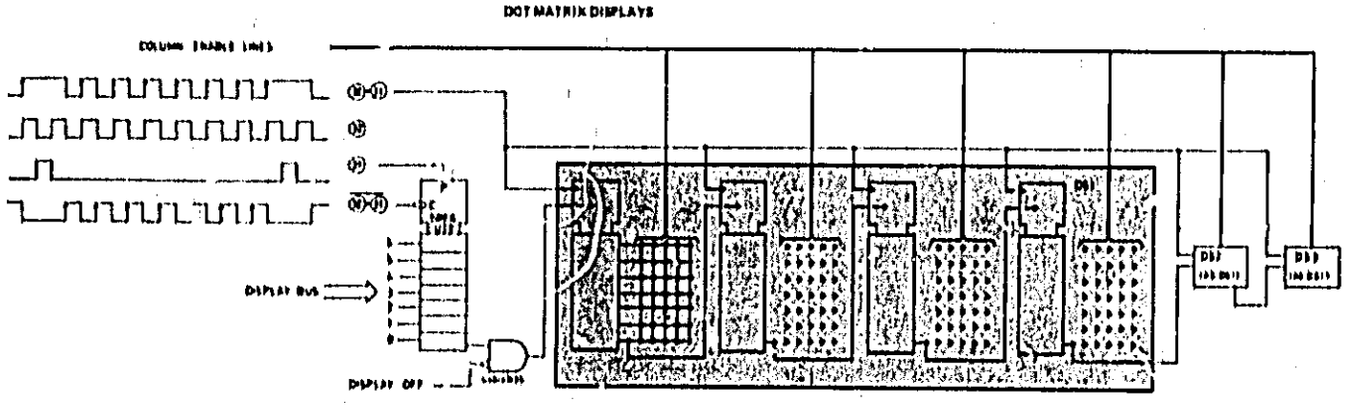
8–1E–3 KEYBOARD INDICATOR LEDS

8–1E–4 As shown below, the LEDs are arranged in a matrix. The three columns are tied to Column Enable lines 2, 3 and 4, and the rows are selected by the display bus status.

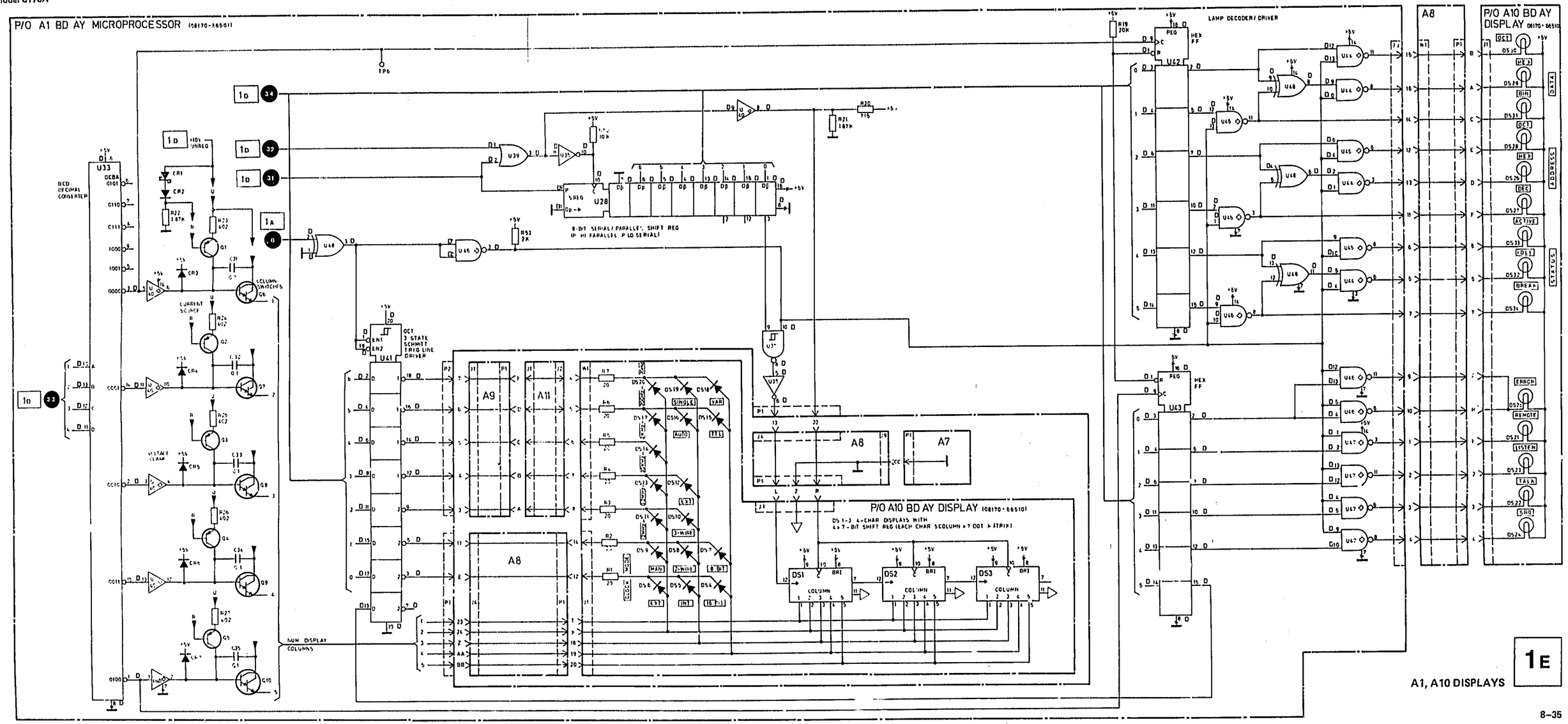


8–1E–5 DOT-MATRIX ALPHA/NUMERIC DISPLAY

8–1E–6 The displays DS1, DS2, DS3 each consists of four 7x5 dot matrices and four 7-bit shift registers. A particular point illuminates when its Column Enable line is true and when a logic 1 exists at its row. The necessary serial data shift is provided by shift register U28 as shown below.

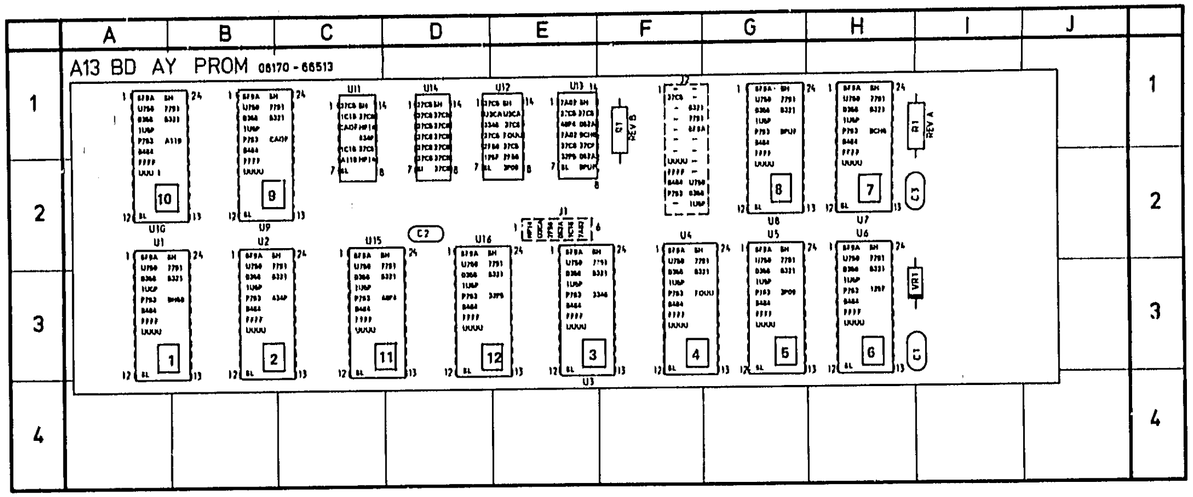


SERVICE INFORMATION CON'T



1E

A1, A10 DISPLAYS



DSA Routine 2	SH = 0003
5004A	8170A BD AY A1 Testpoint
START, STOP	Address Bit A15
CLOCK	CLK
GROUND	GND

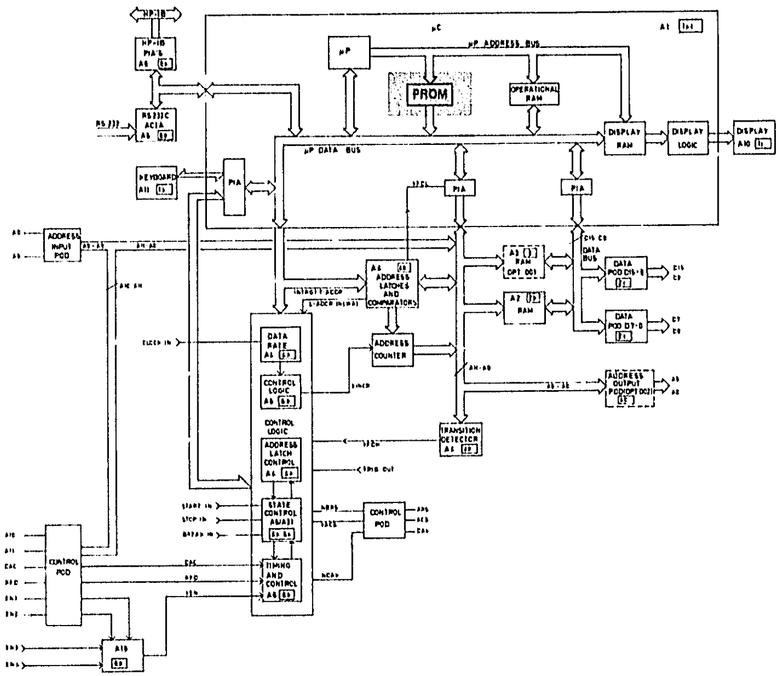
Set the 8170A as follows:

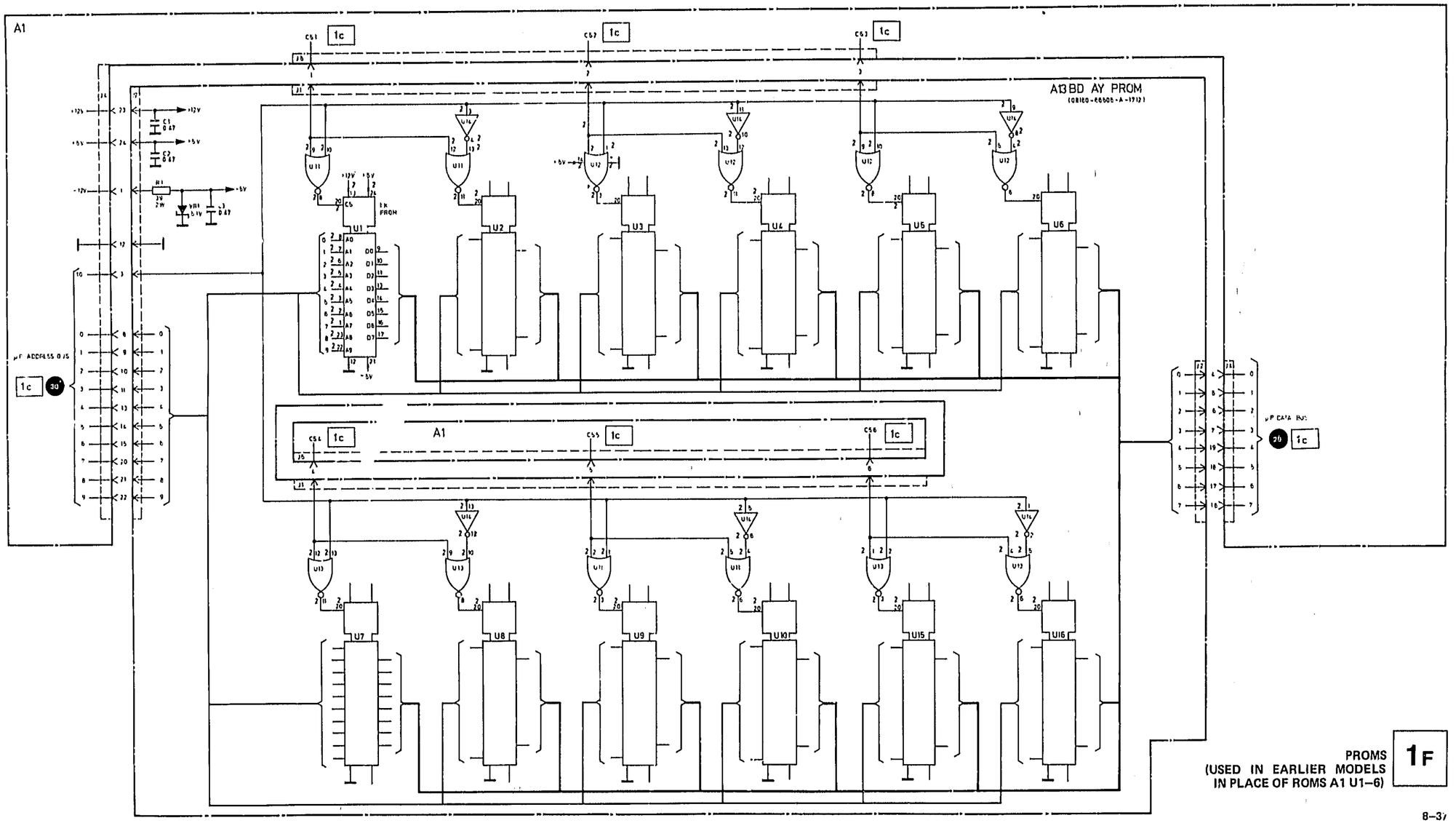
Set jumper A1W1 to DSA,
remove jumper A1W2 (serial numbers 00115 and below) or set to DSA (serial numbers 00116 and above),
set A1S1 to T,
press A1S2 to R.

1F

A13 BD AY PROM

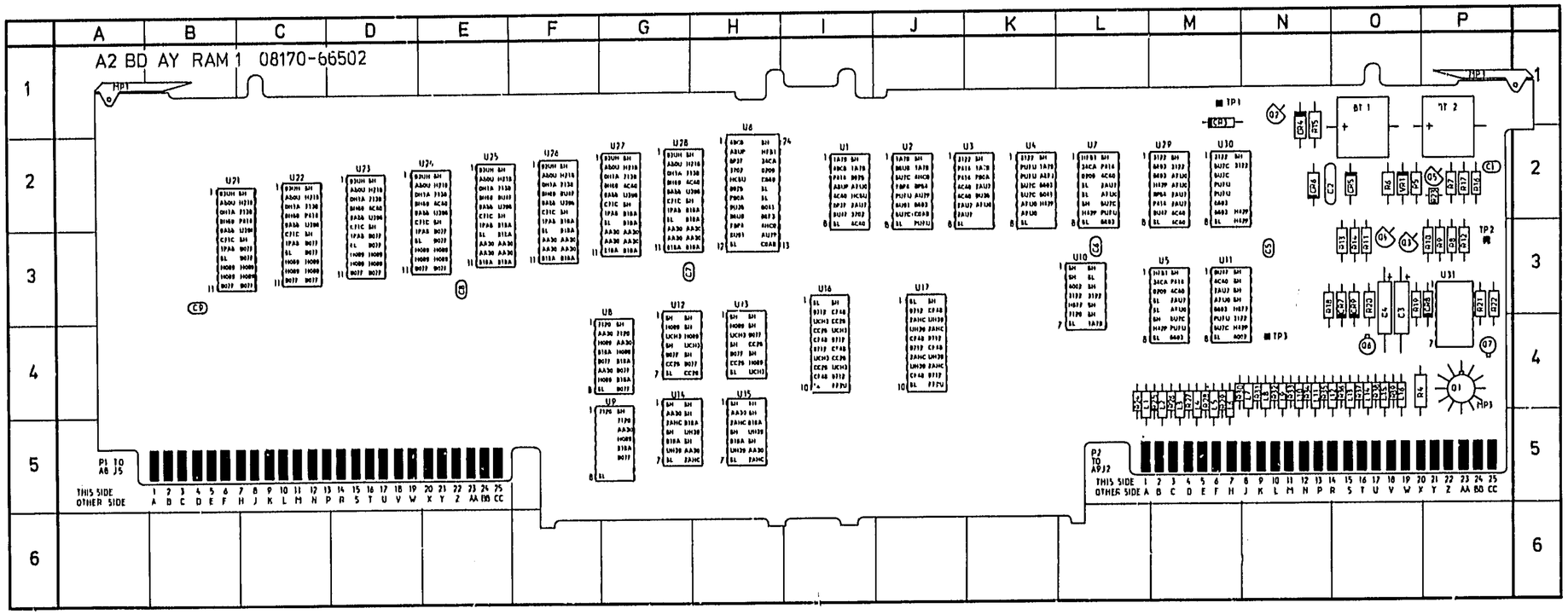
SERVICE SHEET 1F LOCALIZER





PROMS (USED IN EARLIER MODELS IN PLACE OF ROMS A1 U1–6) **1F**

DSA ROUTINE



DSA Routine F SH = 2C5A	
5004A	8170A BD AY A1 Testpoint
START, STOP	G/H
CLOCK	CLK
GROUND	GND

Set the 8170A as follows:

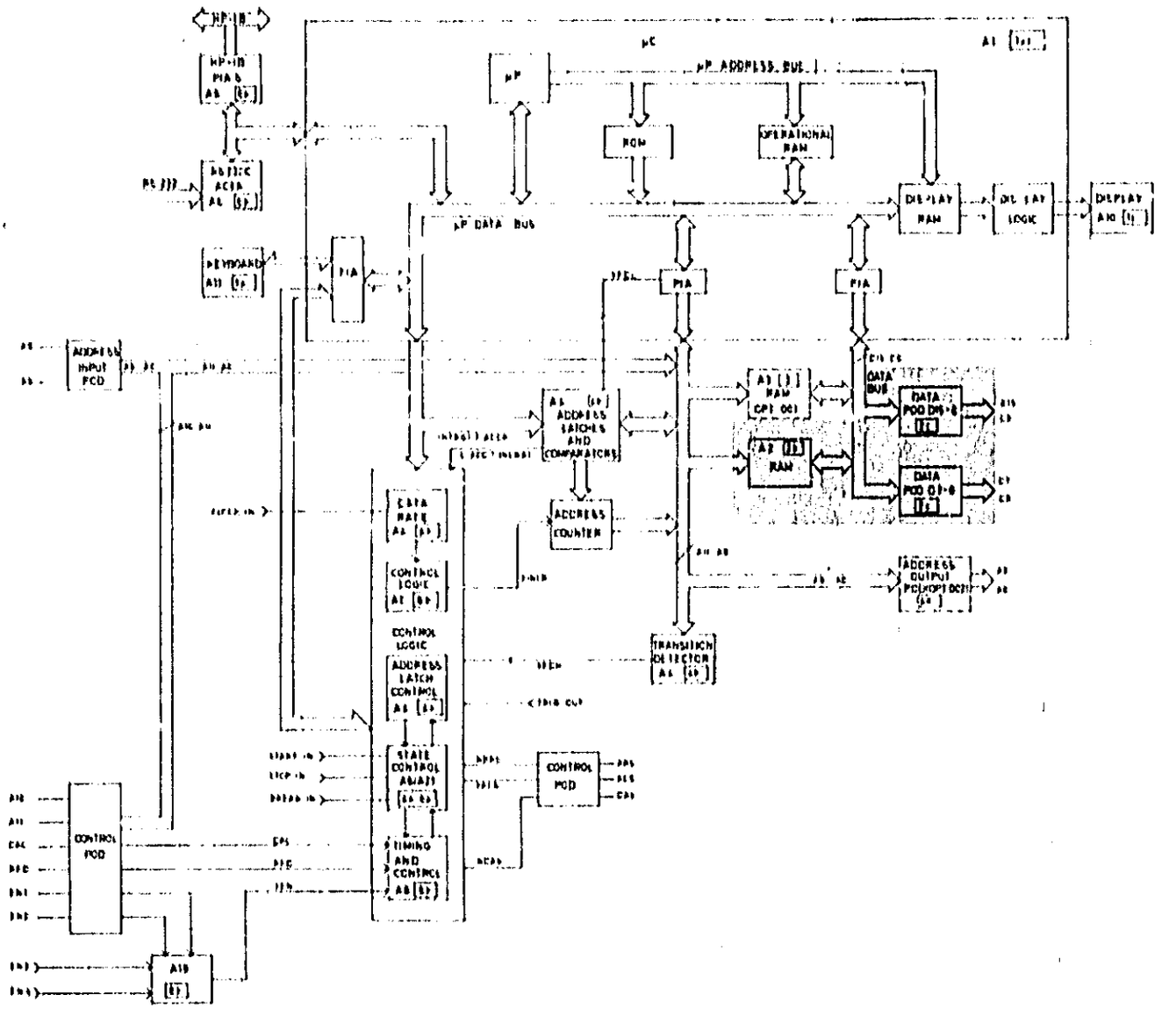
all jumpers in NORMAL position,
remove A2 Extended Memory Board (applies to Option 001 only),
remove A5 HP-IB/RS 232C,
set DATA switch on rear panel to high,
Set A1 S1 to T,
press A1 S2 to R,
press the F key on the front panel.

REF DESIG	GRID LOC
BT1	O-1
BT2	P-1
C1	P-2
C2	N-2
C3	O-3
C4	O-3
C5	N-3
C6	L-3
C7	G-3
C8	E-3
C9	B-3
CR3	M-2
CR4	N-1
CR5	O-2
CR6	N-2
CR7	O-3
CR8	P-3
CR9	O-3
L1	M-4
L2	M-4
L3	M-4
L4	M-4
L5	M-4
L6	M-4
L7	N-4
L8	N-4
L9	N-4
L10	N-4
L11	N-4
L12	N-4
L13	O-4
L14	O-4
L15	O-4
L16	O-4
MP1	A-1
MP2	P-1
MP3	P-4
Q1	P-4
Q2	N-1
Q3	O-3
Q4	O-3
Q5	P-2
Q6	O-4
Q7	P-4
R4	O-4
R5	O-2
R6	O-2
R7	P-2
R8	P-3
R9	P-3
R10	P-3
R11	O-3
R12	P-3
R13	O-3
R14	O-3
R15	N-1
R16	P-2
R17	P-2
R18	N 3
R19	O-3
R20	O-3
R21	P-3
R22	P-3
R24	L-4
R25	M-4
R26	M-4
R27	M-4
R28	M-4
R29	M-4
R30	N-4
R31	N-4
R32	N-4
R33	N-4
R34	N-4
R35	N-4
R36	O-4
R37	O-4
R38	O-4
R39	O-4
RT23	P-2
U1	I-2
U2	J-2
U3	K-2
U4	K-2
U5	M-3
U6	H-2
U7	L-2
U8	G-4
U9	G-5
U10	L-3
U11	M-3
U12	G-4
U13	H-4
U14	G-5
U15	H-5
U16	I-4
U17	S-4
U21	C-2
U22	C-2
U23	D-2
U24	E-2
U25	E-2
U26	F-2
U27	G-2
U28	G-2
U29	M-2
U30	M-2
U31	P-3
VR1	O-2

2A

A2 BD AY RAM 1 (FOR A19, SEE SERVICE SHEET 6B)

SERVICE SHEET 2A LOCALIZER



8–2–1 RAM POWER SUPPLY

8–2–2 Non-volatility of the stored data is ensured by the supply from the batteries BT1 and BT2. These are charged by the circuit Q5, R23 preventing charging below 0°C. Power switch-off is recognized when the +5 V supply falls to 4.7 V. This causes CE2 to go low, and the RAMs are disabled. At the same time, NREST goes low so that the μP goes into a power down status. Subsequently, the Q2 hold-off current via CR4 disappears and the RAMs are supplied from the batteries. At switch-on, Q2 is switched off and the RAMs are supplied via CR3 from the voltage regulator circuit of Q1. After an interval, NREST and CE2 are pulled high.

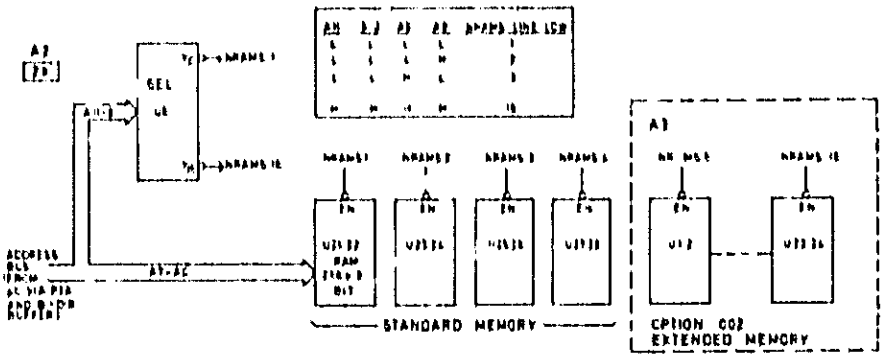
8–2–3 RAM SEGMENT SELECTION

8–2–4 The user-programmable RAM is addressed by 12 address lines (the address bus). However, the RAM is not a single chip but consists of 8 separate IC's (32 in Option 001) with 8 address lines. Consequently, the four most significant address lines are decoded so that the appropriate IC is enabled.

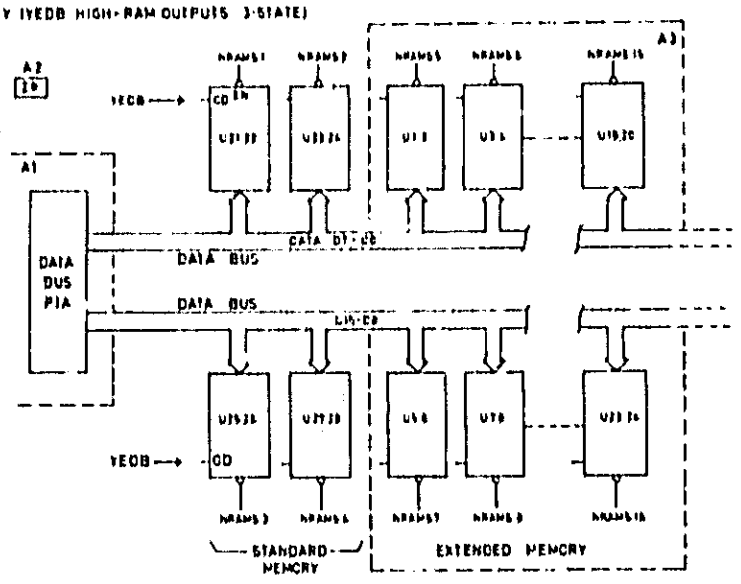
8–2–5 Decoding is dependent on whether 8-or 16-bit DATA BUS mode is selected. If 8-bit is selected, decoder U6 is used and the IC's are enabled in pairs so that an 8-bit width is obtained from two 4-bit IC's. If 16-bit is selected, decoders U5 and U7 enable the IC's in sets of four so that a 16-bit width is realized. In 8-bit operation, the data outputs of the RAM IC's which normally supply data lines 15–8 are strapped to data lines 7–0 so that the data depth is doubled (the basic 16-bit data bus organization is, however, retained when the μP writes into memory). The following diagrams outline the different configurations.

RAM ORGANIZATION – 8-BIT DATA BUS SELECTED (Y1076 HIGH)

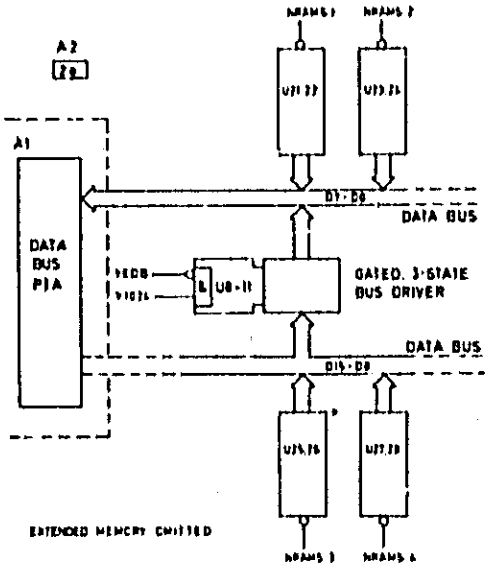
ADDRESSING



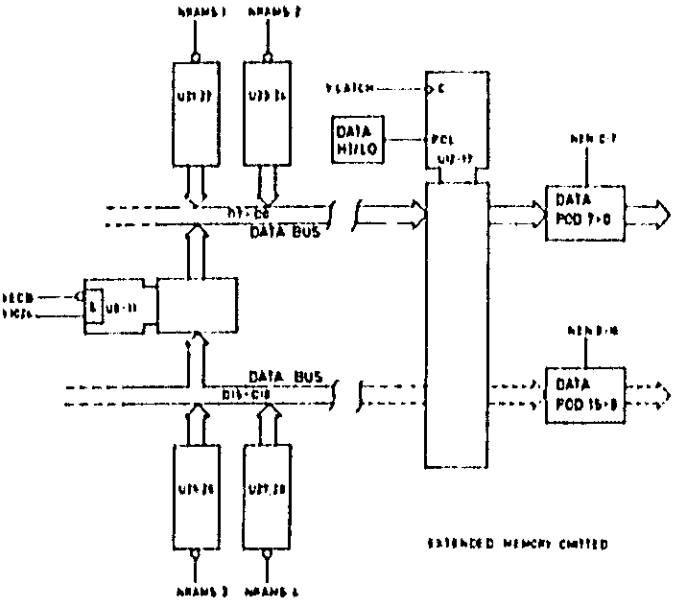
DATA ENTRY (YEOB HIGH – RAM OUTPUTS 3-STATE)



DISPLAY DATA (YEOB LOW – RAM OUTPUTS ENABLED)

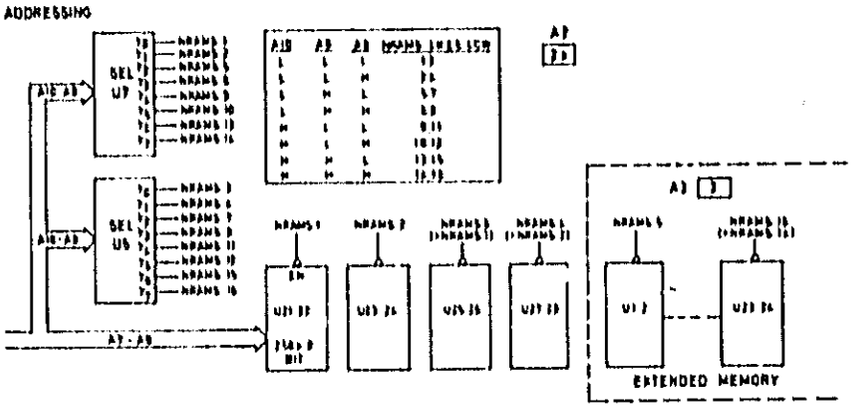


OUTPUT DATA (YEOB LOW – RAM OUTPUTS ENABLED, NEN 0-7 LOW, NEN 8-15 LOW WITH 3-WIRE HANDSHAKE, YLATCH ENABLED)

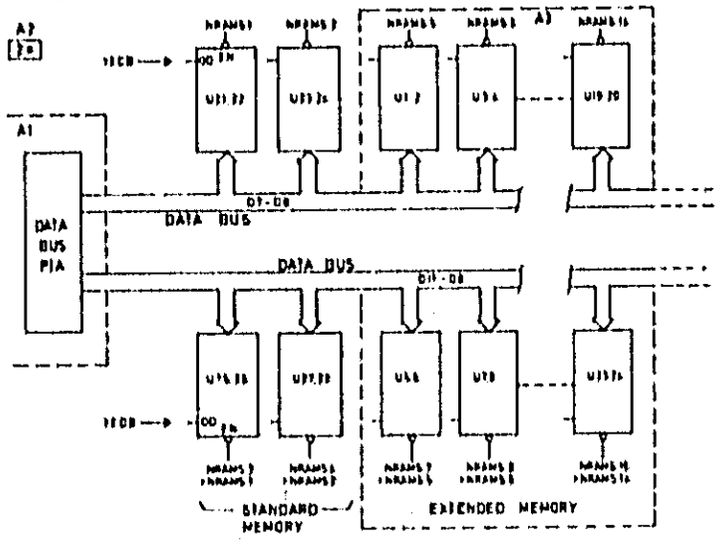


RAM ORGANIZATION—16-BIT DATA BUS SELECTED (Y10)A LOW)

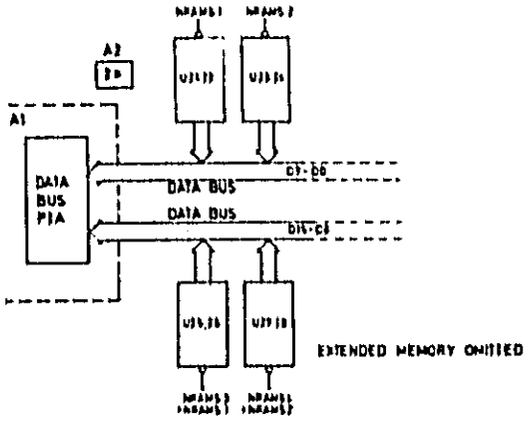
ADDRESSING



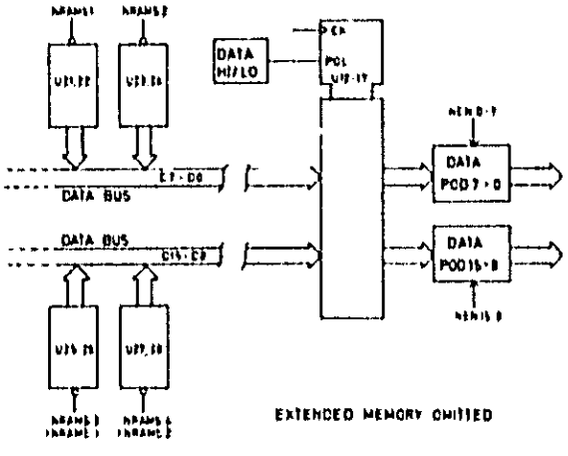
DATA ENTRY (YEDB HIGH - RAM OUTPUTS 3-STATE)

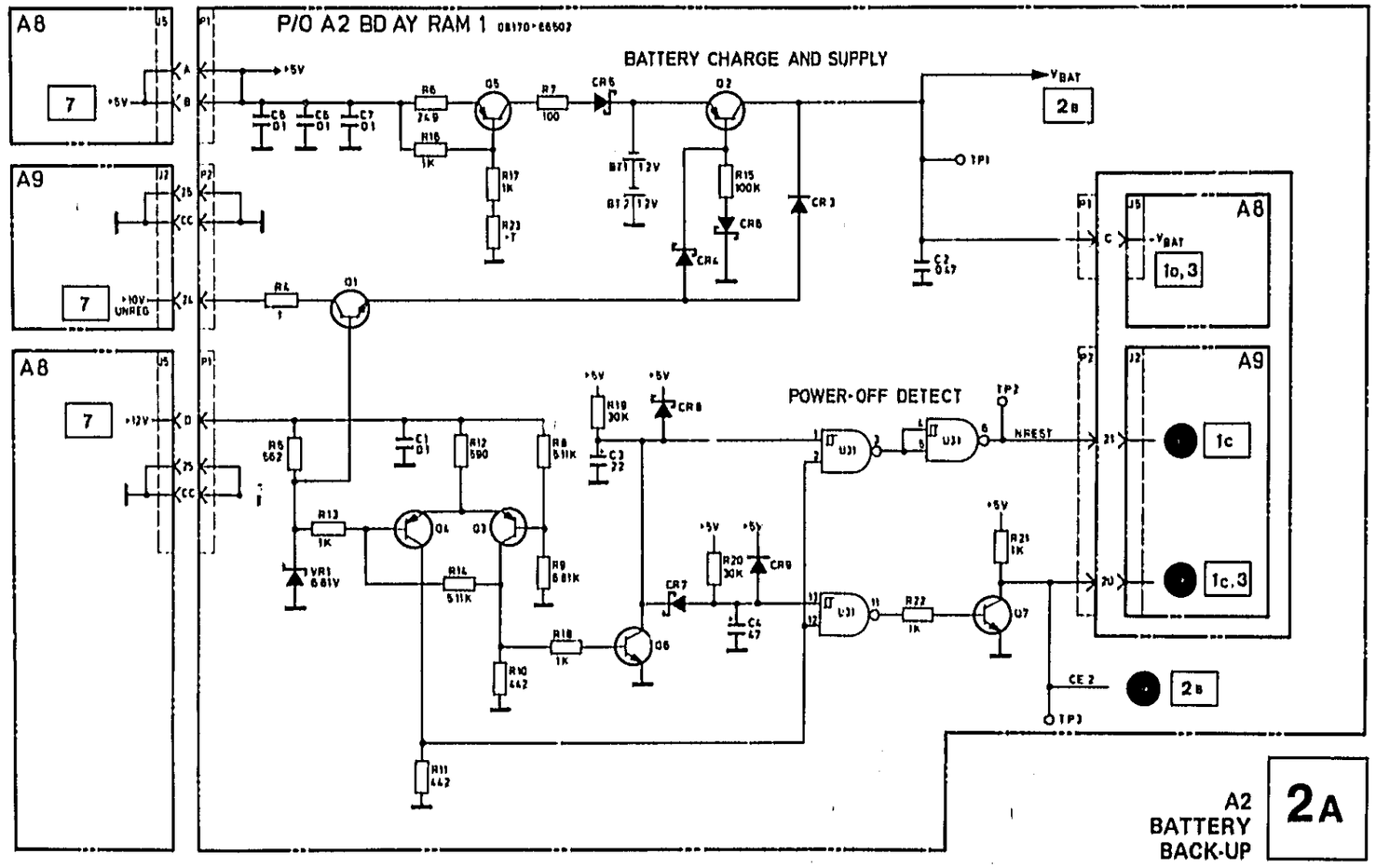


DISPLAY DATA (YEDB LOW - RAM OUTPUTS ENABLED)



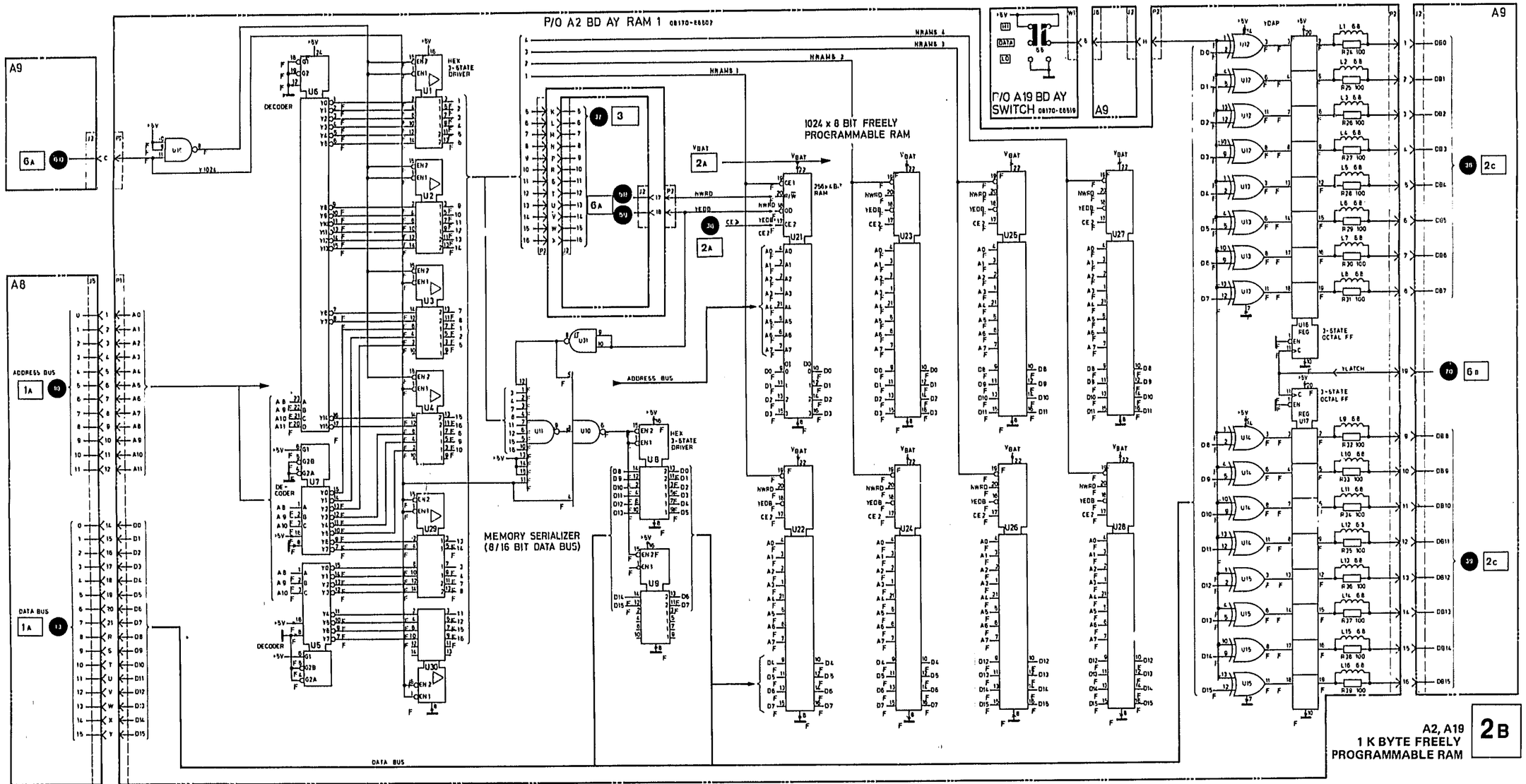
OUTPUT DATA



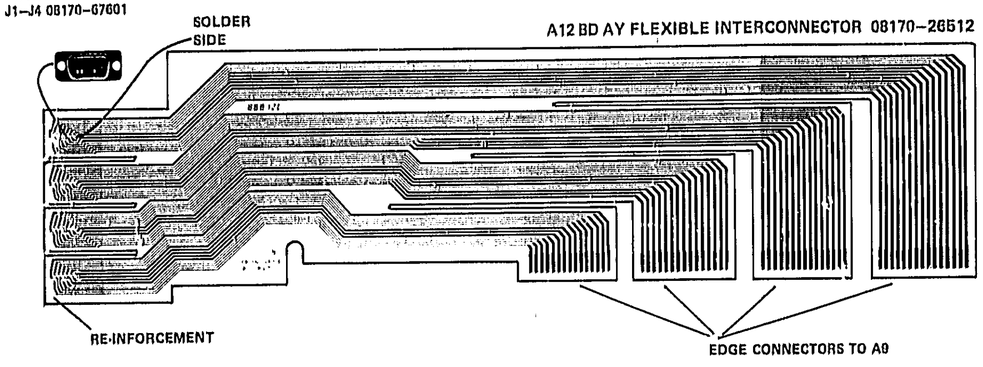


A2
BATTERY
BACK-UP

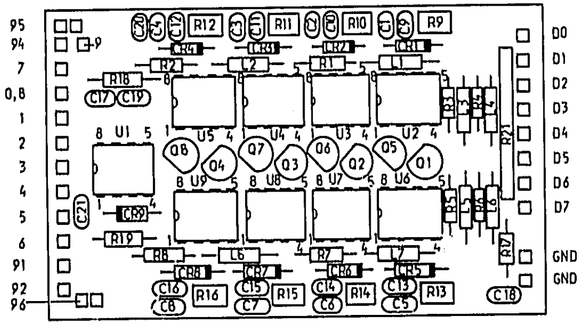
2A


P/O A2 BD AY RAM 1 08170-66507
A9
A8
ADDRESS BUS
DATA BUS
DECODER
HEX 3-STATE DRIVER
MEMORY SERIALIZER (8/16 BIT DATA BUS)
1024 x 8 BIT FREELY PROGRAMMABLE RAM
256 x 4 B.T. RAM
3-STATE OCTAL FF
YLATCH
YDAP
NRAMS 4
NRAMS 3
NRAMS 2
NRAMS 1
NWRD
YEDB
VBAT
P/O A19 BD AY SWITCH 08170-66519
A2, A19 1 K BYTE FREELY PROGRAMMABLE RAM
2B

FRONT PANEL CONNECTOR (1 OF 4)
J1–J4 08170–67601



BD AY DATA POD 15455-66501



2c A12 BD AY FLEXIBLE INTERCONNECTOR
BD AY DATA POD

8–2C–1 REPAIR PROCEDURES

8–2C–2 Flexible Interconnector A12/ Front Panel Connectors J1–4

8–2C–3 The flexible interconnector A12 links the front panel multi-pin DATA/CONTROL/ADDRESS connectors J1–4 to the mother board A9 (see Figure 6–1). A12 includes the edge connectors which plug into A1J8, 9, 10, 11 and a re-inforced part for soldering to J1–4, but excludes J1–4 which must be ordered separately. To gain access to A12, remove the front panel as follows:

Remove all boards A1–A7.

CAUTION

A12 is fragile. Do not attempt to unplug A12 from A9 with the boards A1–A7 in place.

Unplug A12 from A9J8, 9, 10, 11.

Remove screws from front frame (MP24 in Figure 6–1).

Withdraw front panel so that the connectors on A10 and A11 disengage from the mother boards.

8–2C–4 To replace J1, 2, 3 or 4, extreme care must be taken in unsoldering as well as resoldering A12.

CAUTION

The combined action of heat and solder removal by suction tends to loosen the printed circuit from A12 (no through-plated holes). Do not use a solder pump until the connector (J1, 2, 3 or 4, as required) has been removed. Avoid excessive heat.

Heat all pins of connector (J1, 2, 3 or 4, as required) together by flowing solder over all pins.

Lift A12 reinforcement away from the connector.

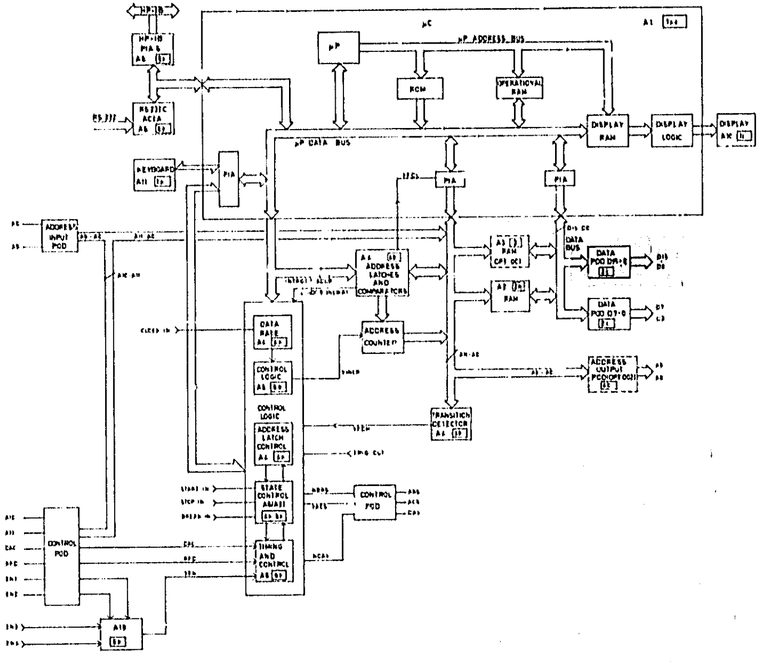
Remove solder from A12.

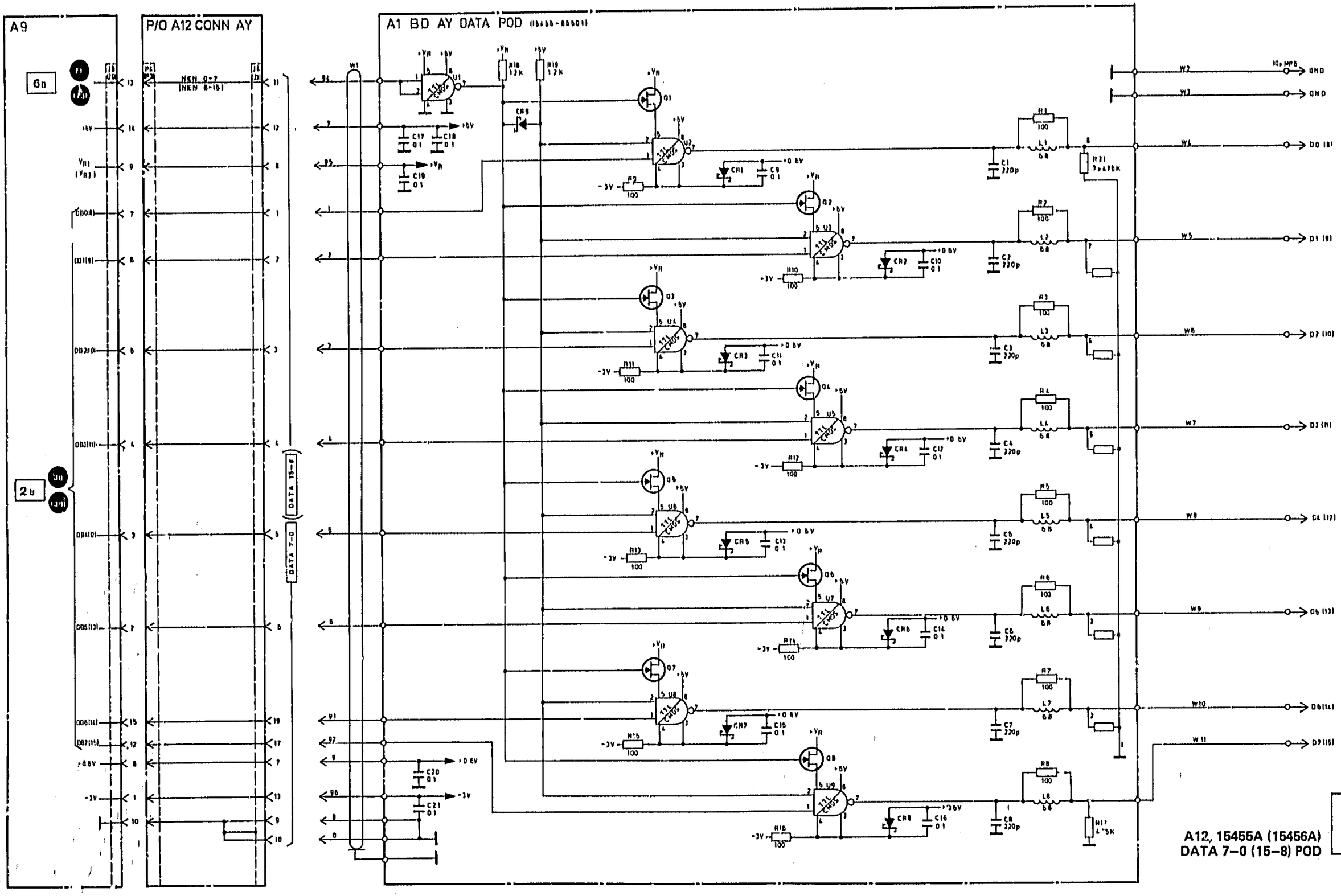
Replace faulty connector in front panel.

Reroider A12 to new connector. Use an extremely thin soldering iron.

8–2C–5 When replacing A12, observe similar precautions when soldering the new A12 to J1, 2, 3 and 4.

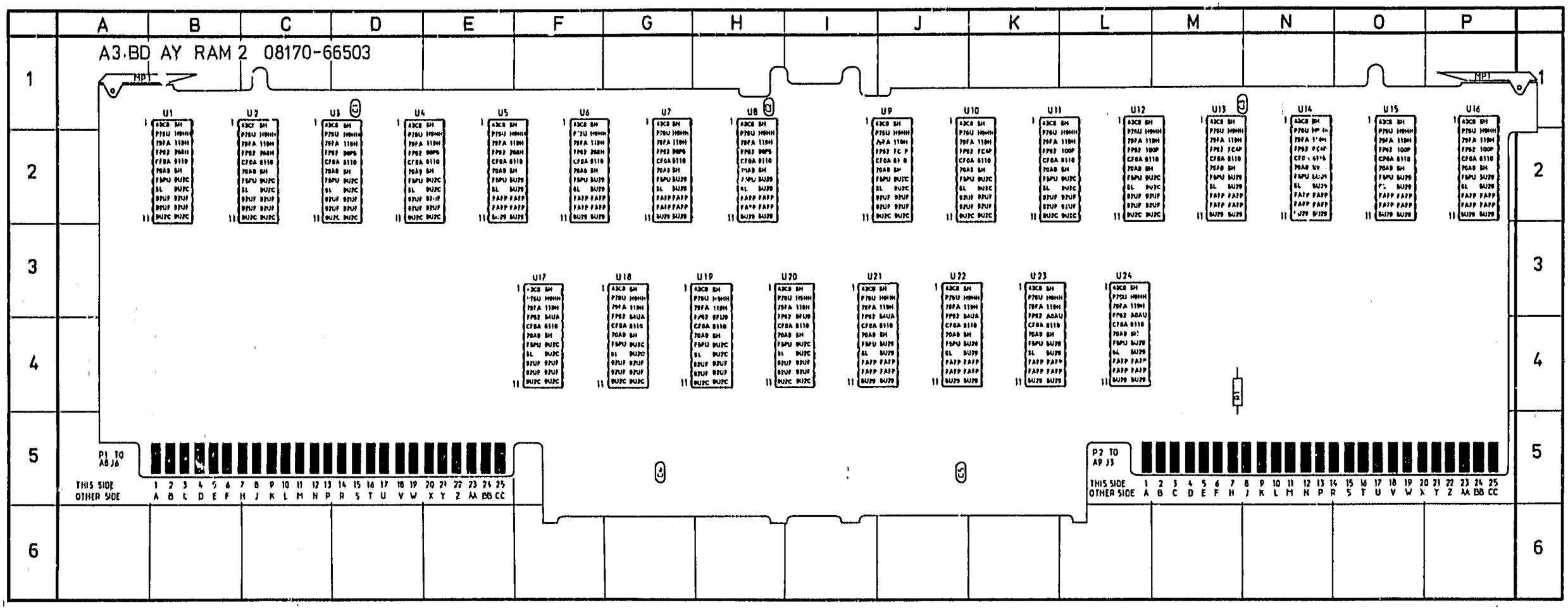
SERVICE SHEET 2c LOCALIZER





A12, 15455A (15456A)
DATA 7–0 (15–8) POD

2c



DSA Routine F SH = 95P7	
5004A	8170A BD AY A1 Testpoint
START, STOP	G,H
CLOCK	CLK
GROUND	GND

Set the 8170A as follows:

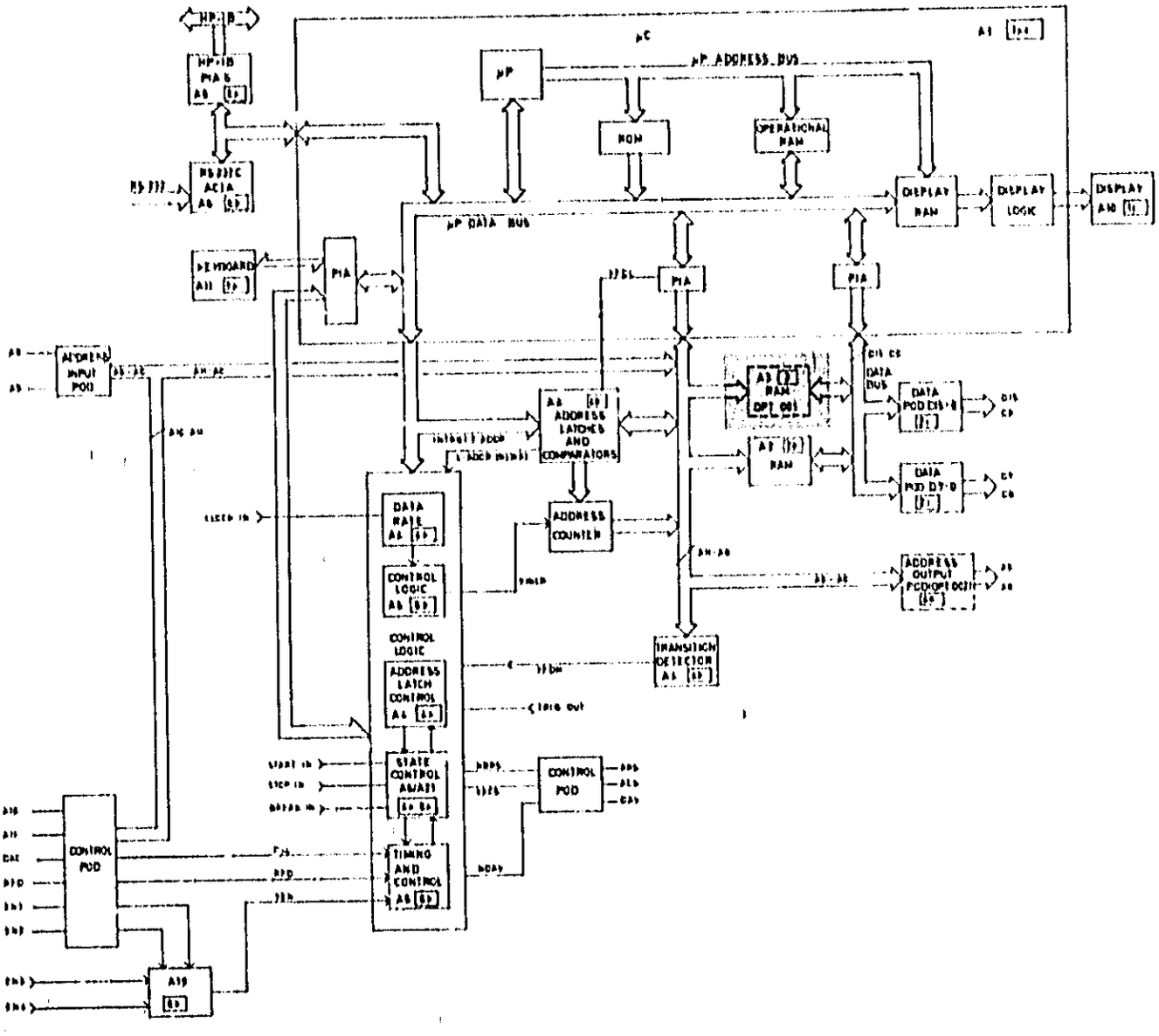
all jumpers in NORMAL position,
install A3 Extended Memory Board (applies to Option 001 only),
remove A6 HP-IB/RS 232C,
set DATA switch on rear panel to high (I),
set A1 S1 to T,
press A1 S2 to R,
press the F key on the front panel.

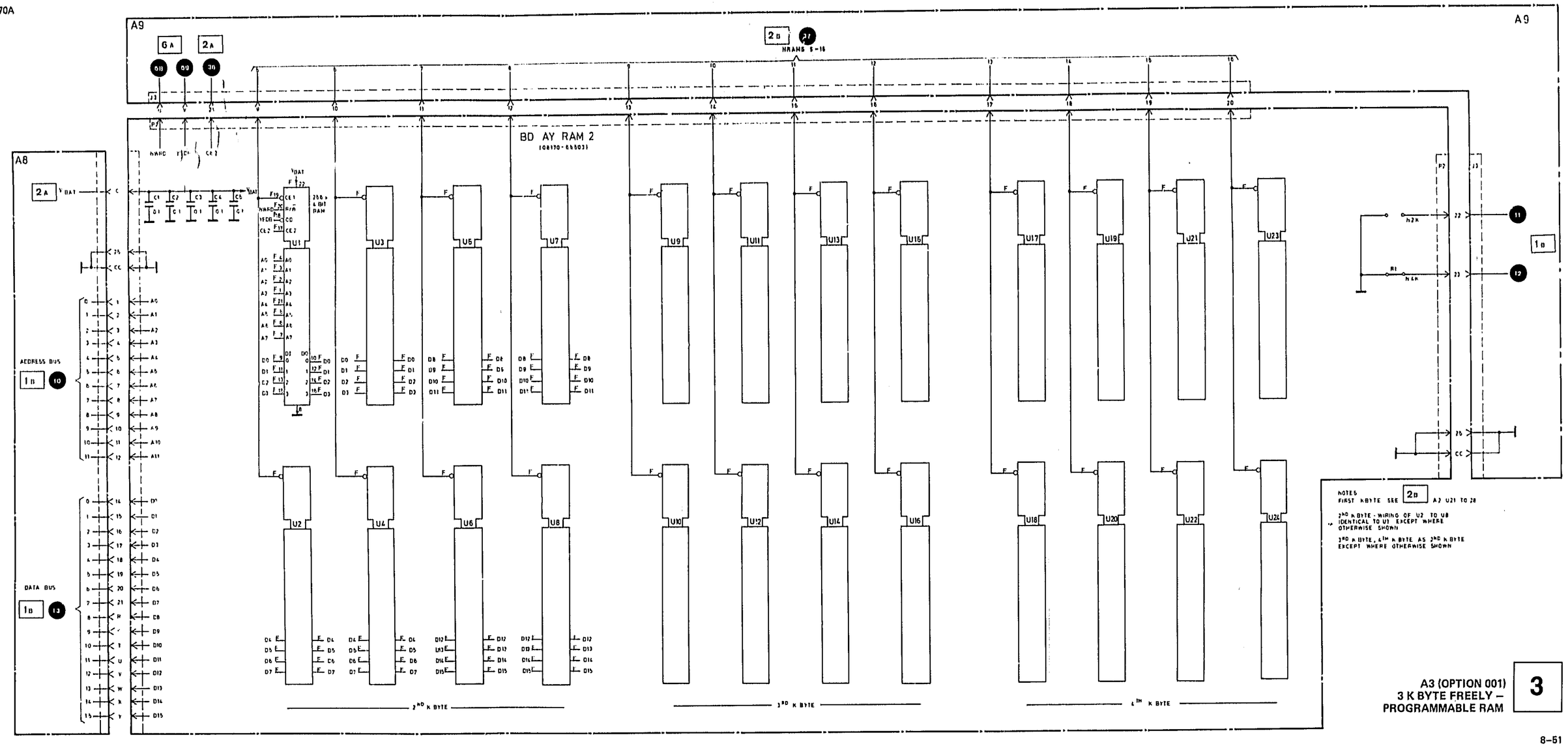
REF DESIG	GRID LOC	REF DESIG	GRID LOC
C1	D-1	U9	J-2
C2	H-1	U10	K-2
C3	M-1	U11	K-2
C4	G-5	U12	L-2
C5	J-5	U13	M-2
MP1	P1	U14	N-2
MP1	A-1	U15	O-2
R1	M-4	U16	P-2
U1	B-2	U17	F-3
U2	C-2	U18	G-3
U3	D-2	U19	H-3
U4	D-2	U20	I-3
U5	E-2	U21	J-3
U6	F-2	U22	J-3
U7	G-2	U23	K-3
U8	H-2	U24	L-3

3

A3 BD AY RAM 2 (OPTION 001)

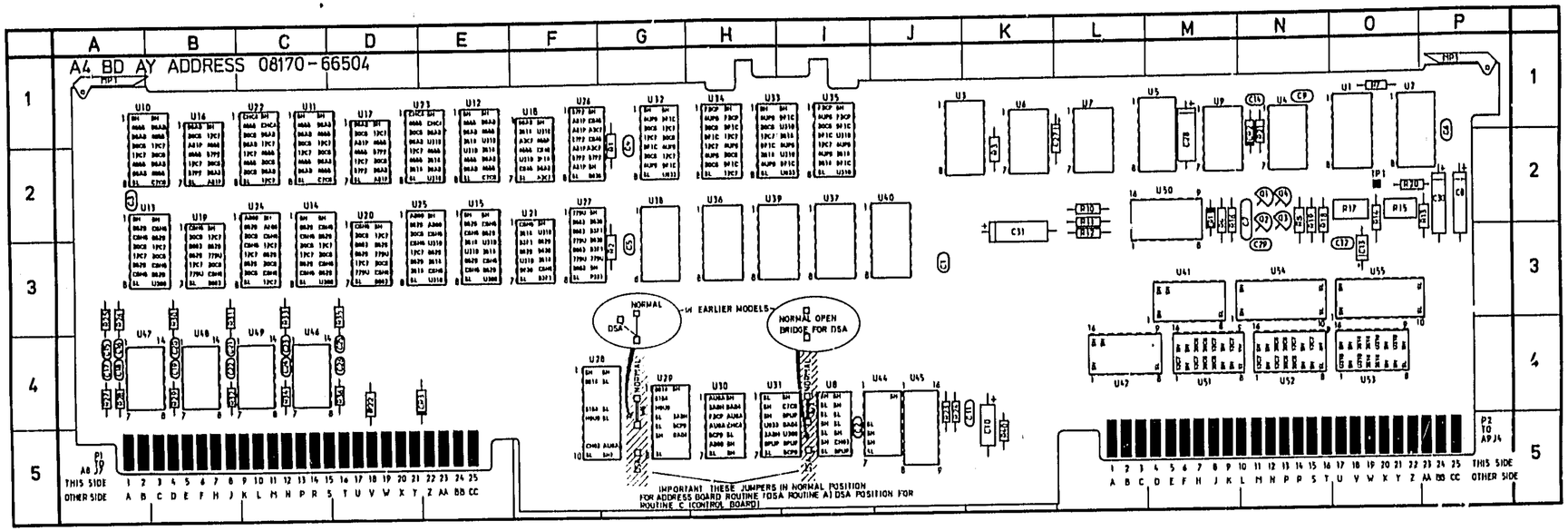
SERVICE SHEET 3 LOCALIZER





A3 (OPTION 001)
3 K BYTE FREELY – PROGRAMMABLE RAM

3



REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC
C1	J-3	C18	A-4	CR2	N-1	R14	O-2	R30	B-3	U9	M-1	U26	E-2	U41	M-3
C2	I-5	C19	B-4	CR3	D-4	R15	O-2	R31	B-3	U10	A-1	U26	F-1	U42	L-4
C3	A-2	C20	B-4	Q1	N-2	R16	M-2	R32	B-4	U11	C-1	U27	F-2	U44	J-4
C4	G-2	C21	B-4	Q2	N-2	R17	O-2	R33	C-3	U12	E-1	U28	F-4	U45	J-5
C5	G-3	C22	B-4	Q3	N-2	R18	N-2	R34	C-4	U13	A-2	U29	G-4	U46	C-4
C6	P-1	C23	C-4	Q4	N-2	R19	N-2	R35	D-3	U14	C-2	U30	H-4	U47	A-4
C7	N-2	C24	C-4	R1	G-2	R20	O-2	R36	D-4	U15	E-2	J31	H-4	U48	B-4
C8	P-2	C25	D-4	R2	G-3	R21	N-1	R40	K-4	U16	B-2	J32	G-1	U49	C-4
C9	N-1	C26	D-4	R3	K-2	R22	D-4	U1	O-1	U17	D-2	U33	H-1	U50	M-2
C10	K-4	C27	L-1	R4	M-2	R23	J-4	U2	O-1	U18	F-2	U34	H-1	U51	M-4
C11	K-4	C28	M-2	R5	N-2	R24	J-4	U3	J-1	U19	B-3	U35	I-1	U52	N-4
C13	O-3	C29	N-3	R7	O-1	R25	A-3	U4	N-1	U20	D-3	U36	H-2	U53	O-4
C14	N-1	C30	P-2	R10	L-2	R26	A-3	U5	M-1	U21	F-3	U37	I-2	U54	N-3
C15	A-4	C31	K-3	R11	L-2	R27	A-4	U6	K-1	U22	C-1	U38	G-2	U55	O-3
C16	A-4	C32	O-3	R12	L-2	R28	A-4	U7	L-1	U23	E-1	U39	H-2	W6	G-5
C17	A-4	CR1	M-2	R13	P-2	R29	B-4	U8	I-4	U24	C-2	U40	J-2	W7	I-5

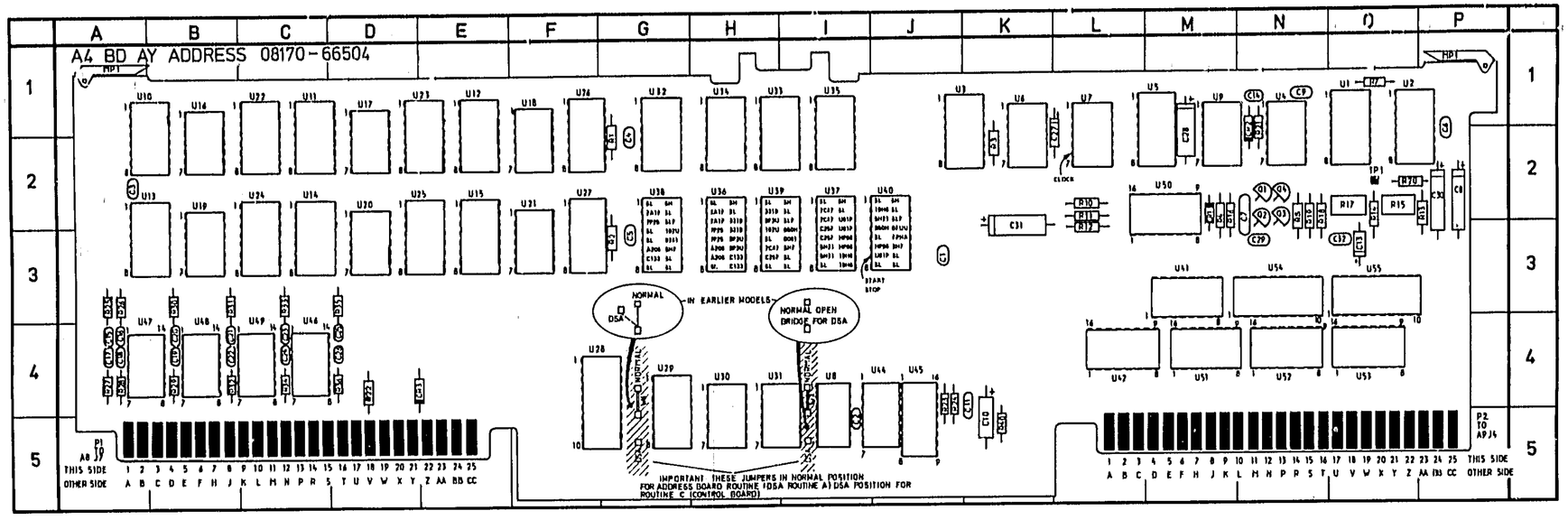
DSA Routine A	SH = H3UH
5004A	8170A BD AY A1 Testpoint
START, STOP	G/H
CLOCK	CLK
GROUND	GND

Set the 8170A as follows:

all jumpers in the NORMAL position,
set A1 S1 to T,
press A1 S2 to R,
press the A key on the front panel.

4A-1

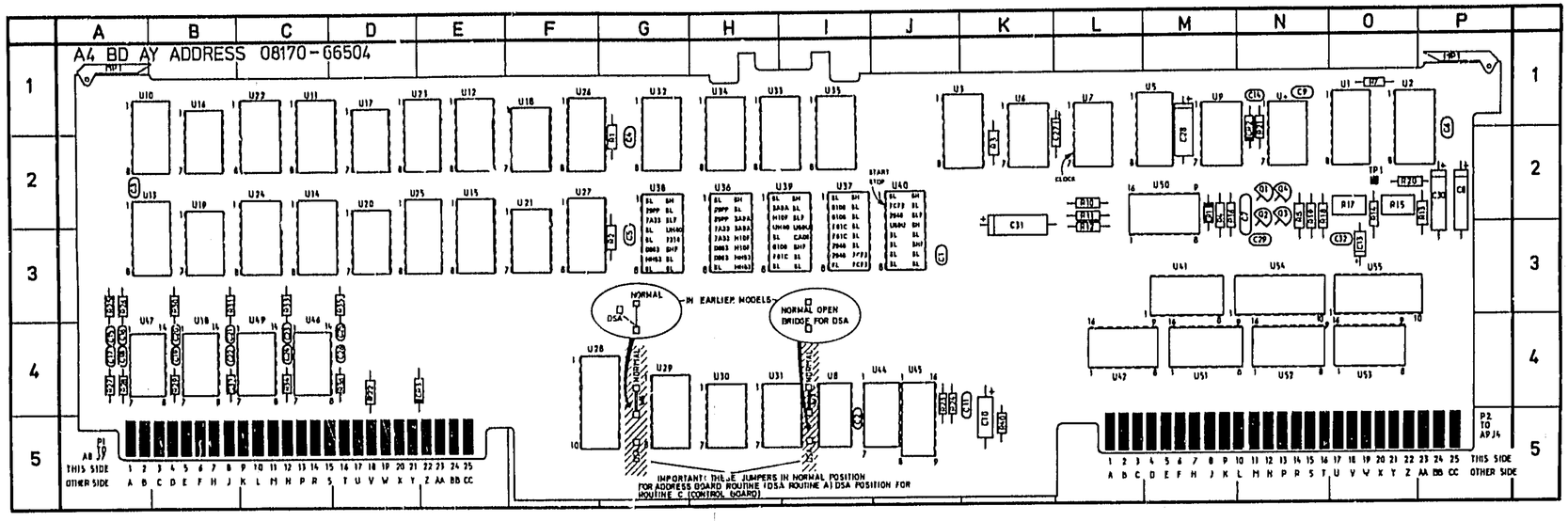
A4 BD AY ADDRESS



DSA Routine 1 SH = 826P	Set the 8170A as follows:
5004A (4 k memory) 8170A BD AY A4 Testpoint	all jumpers in NORMAL position,
START, STOP — U40 pin 7	install A3 Extended Memory Board (applies to Option 001 only),
CLOCK — U7 pin 6	set A1 S1 to N,
GROUND — Chassis	on front panel, select: 8-BIT, AUTO, INT, ADDR MODE, INT CLOCK 0.2 MHz – 2 MHz,
	Load F-ADDR zero,
	Load L-ADDR FFF (HEX address code)
	press START (for active state).

REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC
C1	J-3	C18	A-4	CR2	N-1	R14	O-2	R30	B-3	U9	M-1	U25	E-2	U41	M-3
C2	I-5	C19	B-4	CR3	D-4	R15	O-2	R31	B-3	U10	A-1	U26	F-1	U42	L-4
C3	A-2	C20	B-4	Q1	N-2	R16	M-2	R32	B-4	U11	C-1	U27	F-2	U44	J-4
C4	G-2	C21	B-4	Q2	N-2	R17	O-2	R33	C-3	U12	E-1	U28	F-4	U45	J-5
C5	G-3	C22	B-4	Q3	N-2	R18	N-2	R34	C-4	U13	A-2	U29	G-4	U46	C-4
C6	P-1	C23	C-4	Q4	N-2	R19	N-2	R35	D-3	U14	C-2	U30	H-4	U47	A-4
C7	N-2	C24	C-4	R1	G-2	R20	O-2	R36	D-4	U15	E-2	U31	H-4	U48	B-4
C8	P-2	C25	D-4	R2	G-3	R21	N-1	R40	K-4	U16	B-2	U32	G-1	U49	C-4
C9	N-1	C26	D-4	R3	K-2	R22	D-4	U1	O-1	U17	D-2	U33	H-1	U50	M-2
C10	K-4	C27	L-1	R4	M-2	R23	J-4	U2	O-1	U18	F-2	U34	H-1	U51	M-4
C11	K-4	C28	M-2	R5	N-2	R24	J-4	U3	J-1	U19	B-3	U35	I-1	U52	N-4
C13	O-3	C29	N-3	R7	O-1	R25	A-3	U4	N-1	U20	D-3	U36	H-2	U53	O-4
C14	N-1	C30	P-2	R10	L-2	R26	A-3	U5	M-1	U21	F-3	U37	I-2	U54	N-3
C15	A-4	C31	K-3	R11	L-2	R27	A-4	U6	K-1	U22	C-1	U38	G-2	U55	O-3
C16	A-4	C32	O-3	R12	L-2	R28	A-4	U7	L-1	U23	E-1	U39	H-2	W6	G-6
C17	A-4	CR1	M-2	R13	P-2	R29	B-4	U8	I-4	U24	C-2	U40	J-2	W7	I-5

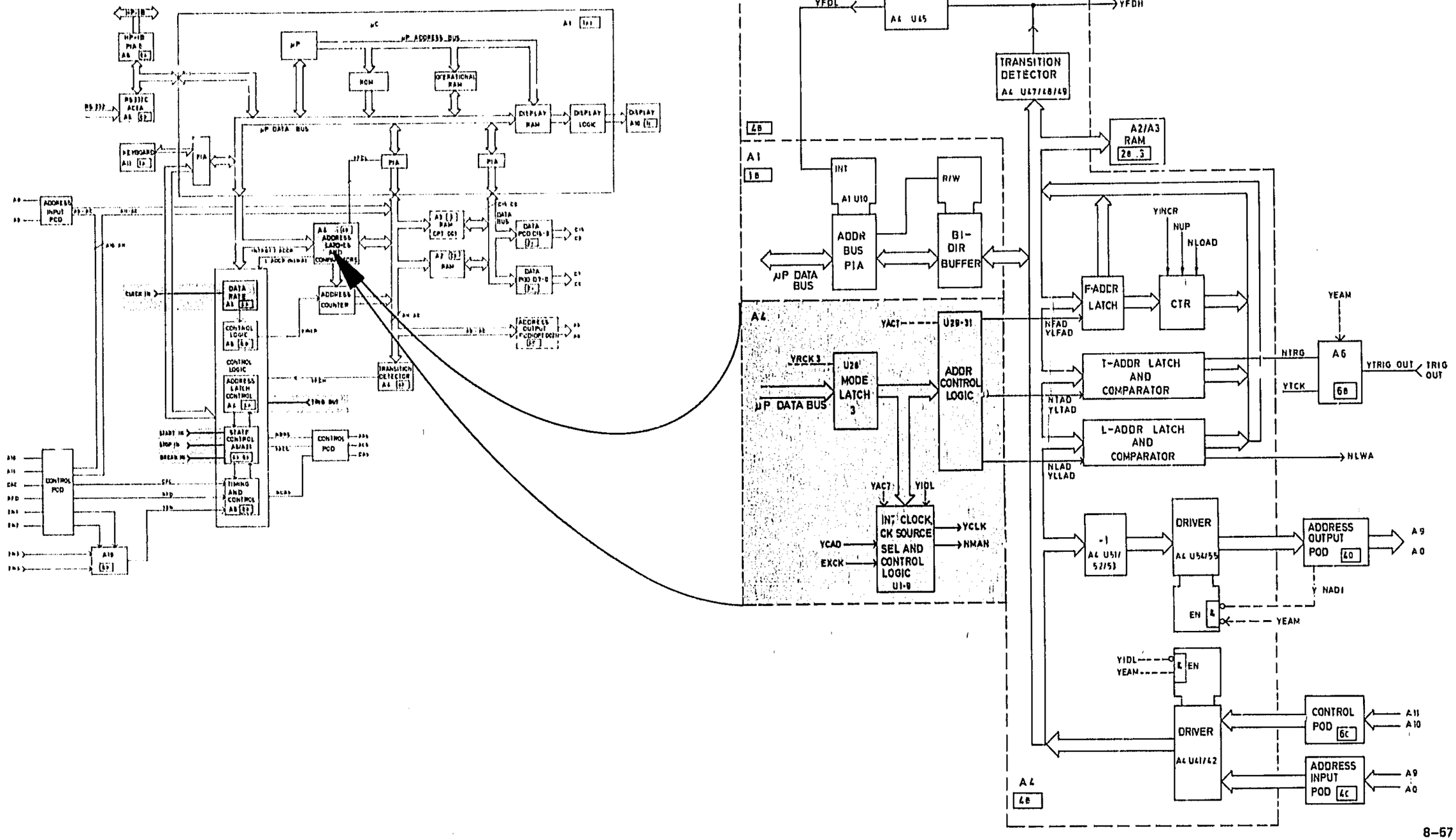
4A-2 **A4 BD AY ADDRESS**
(Use this diagram only for 8170A Option 001, Extended Memory)



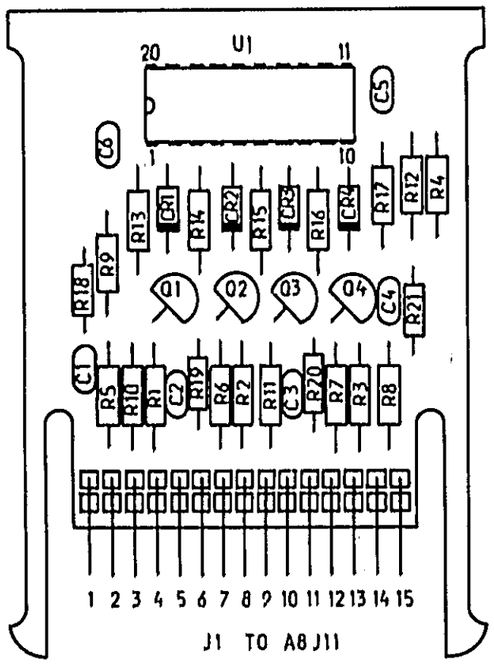
DSA Routine 1 (1 k memory) SH = 8P54	Set the 8170A as follows:
6004A 8170A BD AY A1 Testpoint	all jumpers in NORMAL position,
START, STOP — U40 pin 2	remove A3 Extended Memory Board (applies to Option 001 only),
CLOCK — U7 pin 6	set A1 S1 to N,
GROUND — Chassis	on front panel, select: 8-BIT, AUTO, INT ADDR MODE, INT CLOCK 0.2 MHz – 2 MHz,
	Load F-ADDR zero
	Load L-ADDR 3FF (HEX address code)
	press START (for active state).

REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC
C1	J-3	C18	A-4	CR2	N-1	R14	O-2	R30	B-3	U9	M-1	U25	E-2	U41	M-3
C2	I-5	C19	B-4	CR3	O-4	R15	O-2	R31	B-3	U10	A-1	U26	F-1	U42	L-4
C3	A-2	C20	B-4	Q1	N-2	R16	M-2	R32	B-4	U11	C-1	U27	F-2	U44	J-4
C4	G-2	C21	B-4	Q2	N-2	R17	O-2	R33	C-3	U12	E-1	U28	F-4	U45	J-5
C5	G-3	C22	B-4	Q3	N-2	R18	N-2	R34	C-4	U13	A-2	U29	G-4	U46	C-4
C6	P-1	C23	C-4	Q4	N-2	R19	N-2	R35	D-3	U14	C-2	U30	H-4	U47	A-4
C7	N-2	C24	C-4	R1	G-2	R20	O-2	R36	D-4	U15	E-2	U31	H-4	U48	B-4
C8	P-2	C25	D-4	R2	G-3	R21	N-1	R40	K-4	U16	B-2	U32	G-1	U49	C-4
C9	N-1	C26	D-4	R3	K-2	R22	O-4	U1	O-1	U17	D-2	U33	H-1	U50	M-2
C10	K-4	C27	L-1	R4	M-2	R23	J-4	U2	O-1	U18	F-2	U34	H-1	U51	M-4
C11	K-4	C28	M-2	R5	N-2	R24	J-4	U3	J-1	U19	B-3	U35	I-1	U52	N-4
C13	O-3	C29	N-2	R7	O-1	R25	A-3	U4	N-1	U20	D-3	U36	H-2	U53	O-4
C14	N-1	C30	P-2	R10	L-2	R26	A-3	U5	M-1	U21	F-3	U37	I-2	U54	N-3
C15	A-4	C31	K-3	R11	L-2	R27	A-4	U6	K-1	U22	C-1	U38	G-2	U55	O-3
C16	A-4	C32	O-3	R12	L-2	R28	A-4	U7	L-1	U23	E-1	U39	H-2	W6	G-5
C17	A-4	CR1	M-2	R13	P-2	R29	B-4	U8	I-4	U24	C-2	U40	J-2	W7	I-5

SERVICE SHEET 4A LOCALIZER

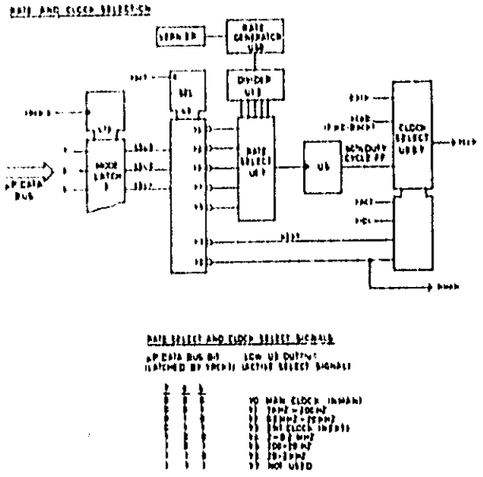


A21 BD AY TRIGGER 08170-66521

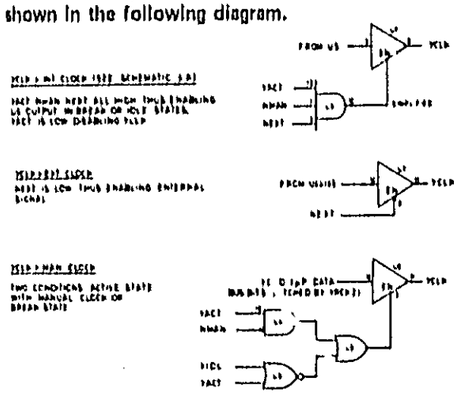


8-4A-1 RATE CONTROL AND CLOCK SOURCE SELECTION

8-4A-2 The internal clock rate is determined by the lines CSL1, 2 and 3 from Mode Latch 3. Depending on the status of these lines, one or other of the counter outputs are enabled, these outputs being a particular division of the rate generator's frequency. The rate generator runs continuously at a frequency between 0.2 MHz and 2 MHz, depending on the front panel vernier setting.

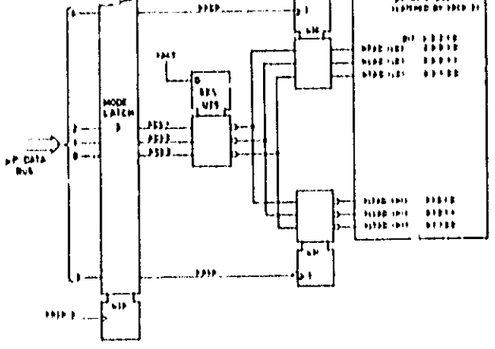


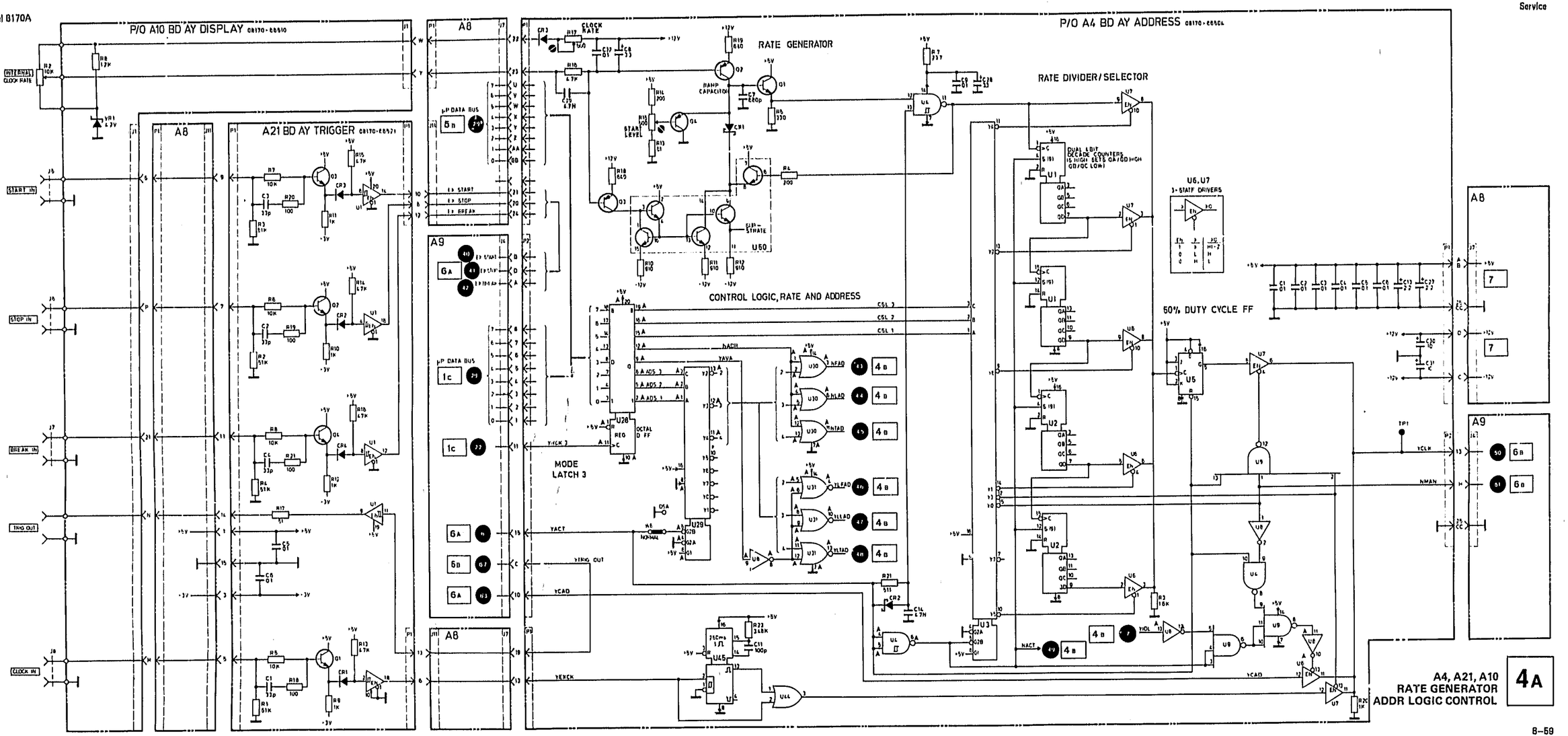
8-4A-3 Depending on the B170A's operating mode and state, the system clock signal (YCLK) is selected from the internal rate, external clock (CLOCK IN buffered in A21 and shaped by A4U45) or from manual impulses from the FWD or BACK keys (these impulses are processed by the μC and appear as the signal YCAD). The operation of the clock select circuit is shown in the following diagram.



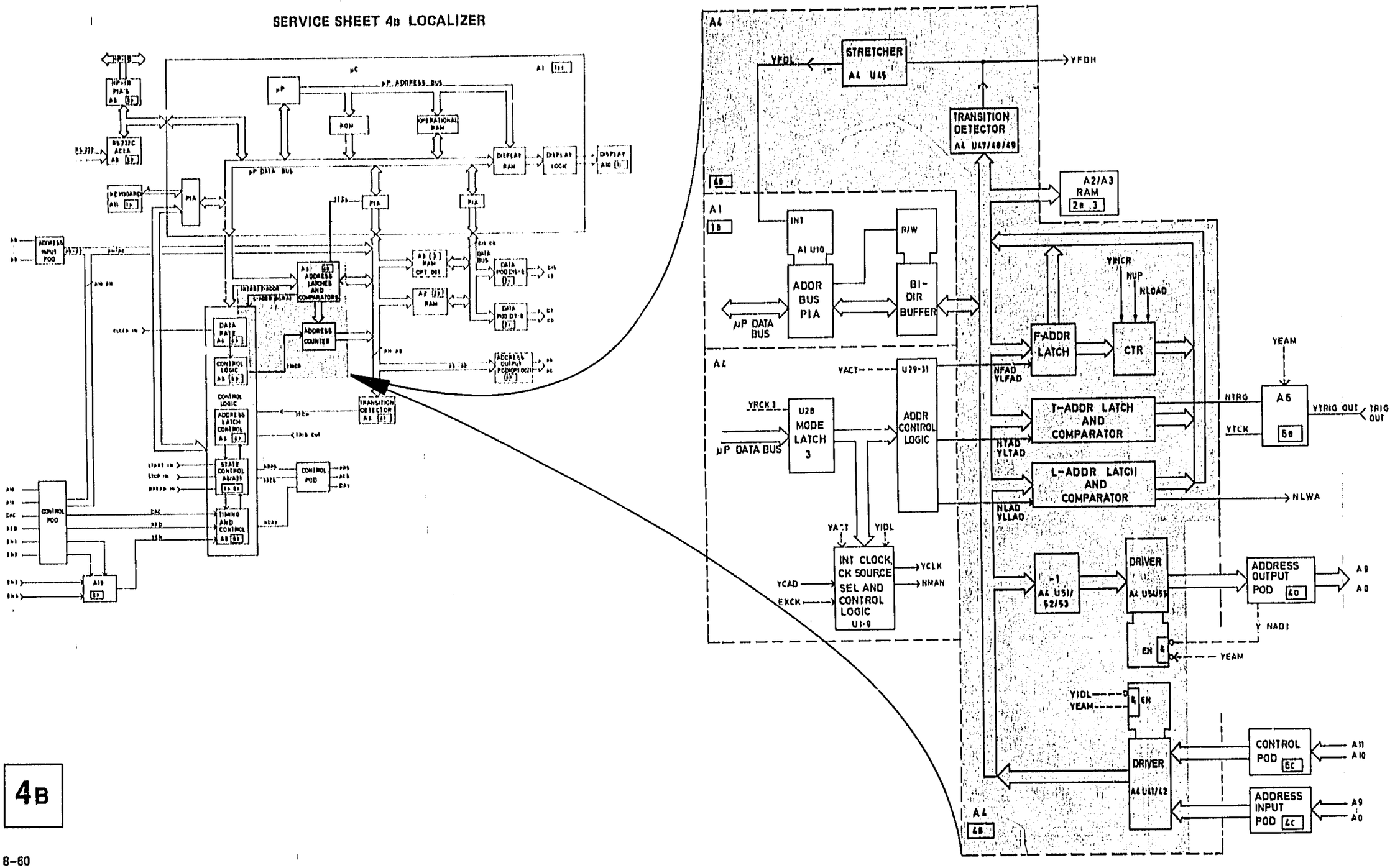
8-4A-4 MODE LATCH 3

8-4A-5 In addition to the clock select signals, Mode Latch 3 status also determines the special address (F-, T- and L-ADDR) control signals as shown below.




P/O A10 BD AY DISPLAY 08170-66510
A8
A21 BD AY TRIGGER 08170-66521
A9
P/O A4 BD AY ADDRESS 08170-66504
RATE GENERATOR
RATE DIVIDER/SELECTOR
CONTROL LOGIC, RATE AND ADDRESS
MODE LATCH 3
U6, U7 3-STATE DRIVERS
50% DUTY CYCLE FF
DUAL 4 BIT DECADE COUNTERS IS HIGH SETS QA/QD HIGH QB/QC LOW)
INTERNAL CLOCK RATE
START IN
STOP IN
BREAK IN
TRIG OUT
CLOCK IN
CLOCK RATE
RAMP CAPACITOR
START LEVEL
OCTAL D FF
DSA ROUTINE
A4, A21, A10
RATE GENERATOR
ADDR LOGIC CONTROL
4A
8-59

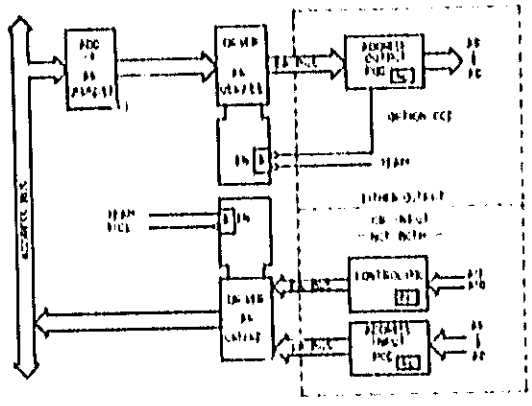
SERVICE SHEET 4B LOCALIZER



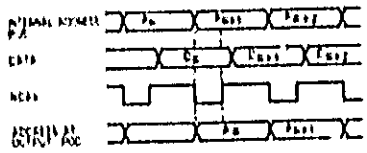
4B

8–4B–1 ADDRESS INPUT (EXT ADDRESS MODE) AND ADDRESS OUTPUT (OPTION 002) INTERNAL ADDRESS MODE

8–4B–2 The EA bus lines are common to both input and output drivers, the data flow, however, is to or from the respective pods and never from one driver to the other. This is ensured by the fact that the input driver is enabled only in external address mode (and active or idle states) and that the output driver is enabled only in internal address mode. Note that, for address input, control pod as well as address input pod must be connected to the 8170A so that all lines are defined.

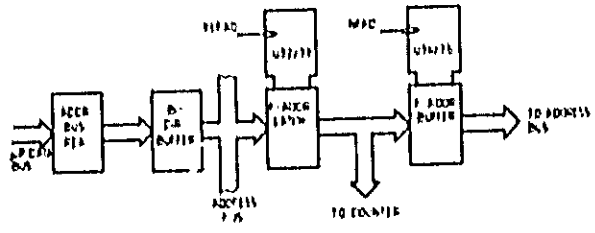


The address adder (U51–53) shifts the address by −1 so that the address appearing at the output corresponds to the data during the interval that DAV is true (low).

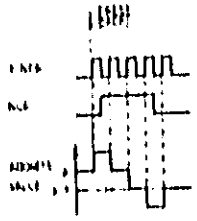


8–4B–3 F·ADDR LATCH AND ADDRESS COUNTER

8–4B–4 F·ADDR is stored on the leading edge of YLFAD, the value being determined by the status of the address bus PIA and buffer. F·ADDR is recalled on the leading (negative-going) edge of NFAD.



8–4B–5 The counter is responsible for putting the required address on the address bus. Starting at the stored F·ADDR, the counter increments by one for each int/ext/man (FWD) clock pulse or handshake. This activity is governed by the YINCR signal which is derived on the Control Board from the appropriate trigger source. Manual BACK effectively decrements the counter. Due to counter type, a decrement of one is achieved indirectly by counting up one, down three, then up one. The necessary clock pulses are inserted into the YINCR signal on the Control Board, the count direction signal (NUP) being derived from the μP data bus.



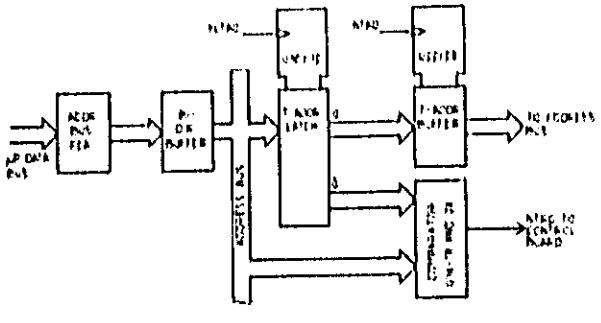
8–4B–6 In the idle state, and at the end of each SINGLE CYCLE, the counter is loaded with the contents of the F·ADDR latch (NLOAD signal).

8–4B–7 T·ADDR LATCH AND COMPARATOR

8–4B–8 T·ADDR is stored on the leading edge of YLTAD and recalled on the leading (negative-going) edge of NTAD. A comparator monitors the address bus and the latch's Q outputs, pulling NTRG low at co-incidence. The comparator consist of EX·NOR gates, the outputs of which are normally low. At co-incidence, all outputs go high and the output (NLWA) of NAND gate U26 is pulled low.

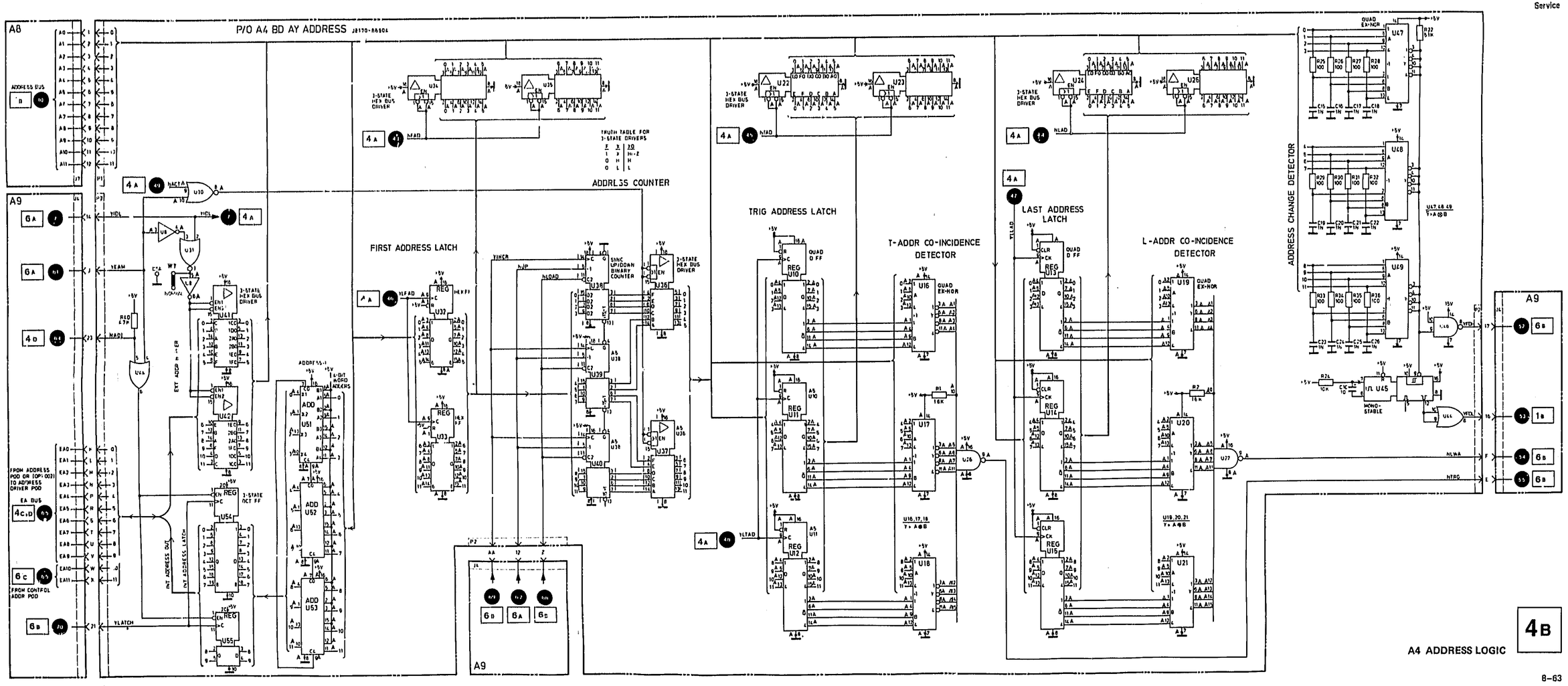
8–4B–9 L·ADDR LATCH AND COMPARATOR

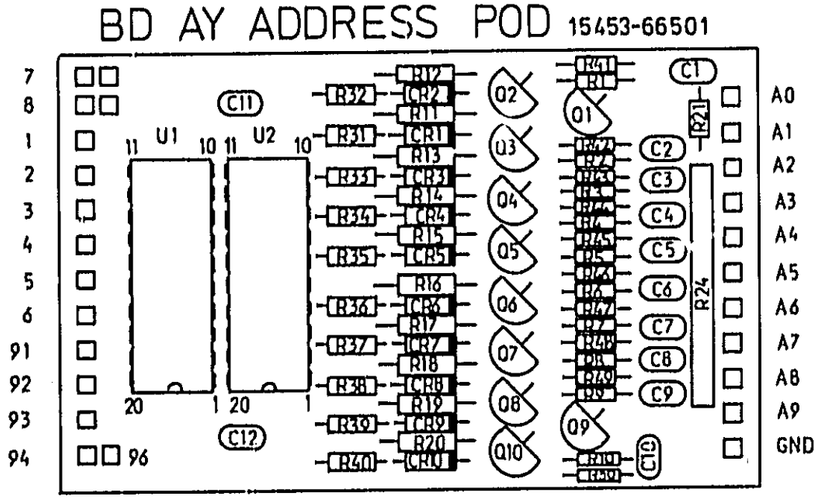
8–4B–10 These operate similary to the T·ADDR latch and comparator.

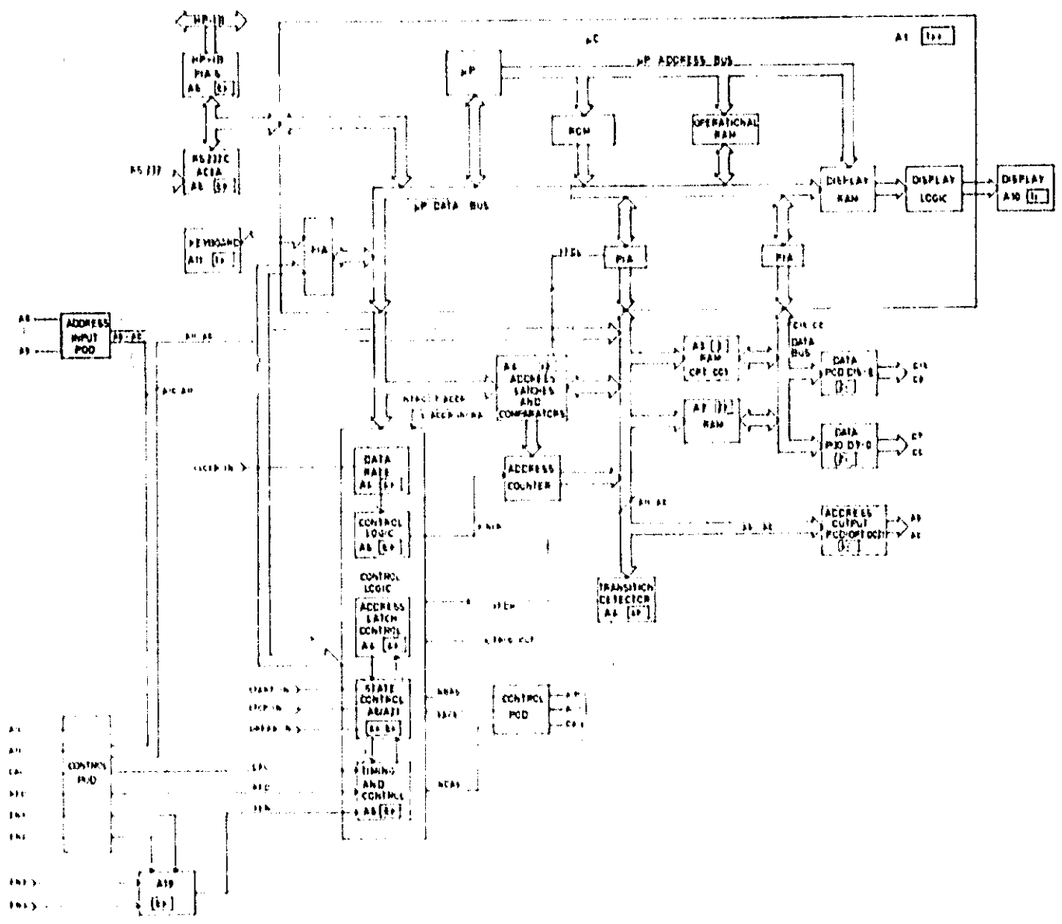


8–4B–11 ADDRESS CHANGE DETECTOR

8–4B–12 In all modes, the address change detector senses transitions on the address bus. The μP is informed of such changes by the stretched YFDL signal. The (unstretched) YFDH signal is used in the External Address mode to generate the data output latch signals. At change rates above 27 Hz, YFDL cannot return to the lowest state. This ensures that the display is blanked at speeds which exceed visual perception.


P/O A4 BD AY ADDRESS
A8
A9
ADDRESS BUS
FROM ADDRESS POD OR TOP (-002) TO ADDRESS DRIVER POD
EA BUS
FROM CONTROL ADDR POD
EXT ADDR REG
INT ADDRESS BUS
INT ADDRESS LATCH
3-STATE HEX BUS DRIVER
3-STATE OCT FF
FIRST ADDRESS LATCH
ADDRESS COUNTER
SYNC UP/DOWN BINARY COUNTER
16-BIT ADDR ADDERS
TRIG ADDRESS LATCH
T-ADDR CO-INCIDENCE DETECTOR
LAST ADDRESS LATCH
L-ADDR CO-INCIDENCE DETECTOR
ADDRESS CHANGE DETECTOR
QUAD EX-NOR
QUAD D FF
MONO-STABLE
TRUTH TABLE FOR 3-STATE DRIVERS
E S | I/O
1 1 | H-Z
0 H | H
0 L | L
A4 ADDRESS LOGIC
4B
DSA ROUTINE
8-63





4c BD AY ADDRESS INPUT POD

8–4C–1 REPAIR PROCEDURES

8–4C–2 Refer to § 8–2C–1 for replacement of A12 or associated front panel connectors.

A9

P/O A12 CONN AY

A1 BD AY ADDRESS RECEIVER PROBE (18453-66501)

6B

4B

4B

EA BUS

NEN 0-7

ADDR 0-9

NADJ

W1

NC

NC

+5V

-3V

C11 0.1

C12 0.1

U1

U2

CR1

CR2

CR3

CR4

CR5

CR6

CR7

CR8

CR9

CR10

Q1

Q2

Q3

Q4

Q5

Q6

Q7

Q8

Q9

Q10

R1 10K

R2 10K

R3 10K

R4 10K

R5 10K

R6 10K

R7 10K

R8 10K

R9 10K

R10 10K

R11 1K

R12 1K

R13 1K

R14 1K

R15 1K

R16 1K

R17 1K

R18 1K

R19 1K

R20 1K

R21 61.1K

R22 9.47K

R31 4.64K

R32 4.64K

R33 4.64K

R34 4.64K

R35 4.64K

R36 4.64K

R37 4.64K

R38 4.64K

R39 4.64K

R40 4.64K

R41 100

R42 100

R43 100

R44 100

R45 100

R46 100

R47 100

R48 100

R49 100

R50 100

C1 33p

C2 33p

C3 33p

C4 33p

C5 33p

C6 33p

C7 33p

C8 33p

C9 33p

C10 33p

W2 11xMPB GND

W3 A0

W4 A1

W5 A2

W6 A3

W7 A4

W8 A5

W9 A6

W10 A7

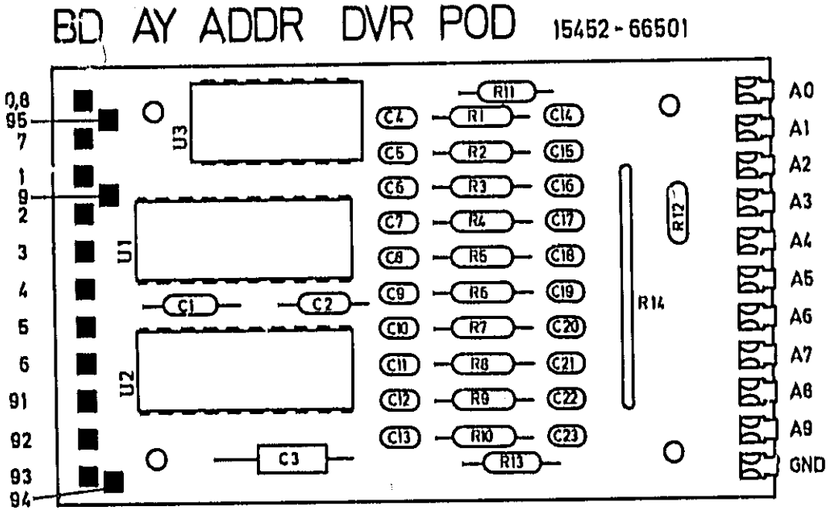
W11 A8

W12 A9

INPUTS

A12, 15453A
ADDRESS POD

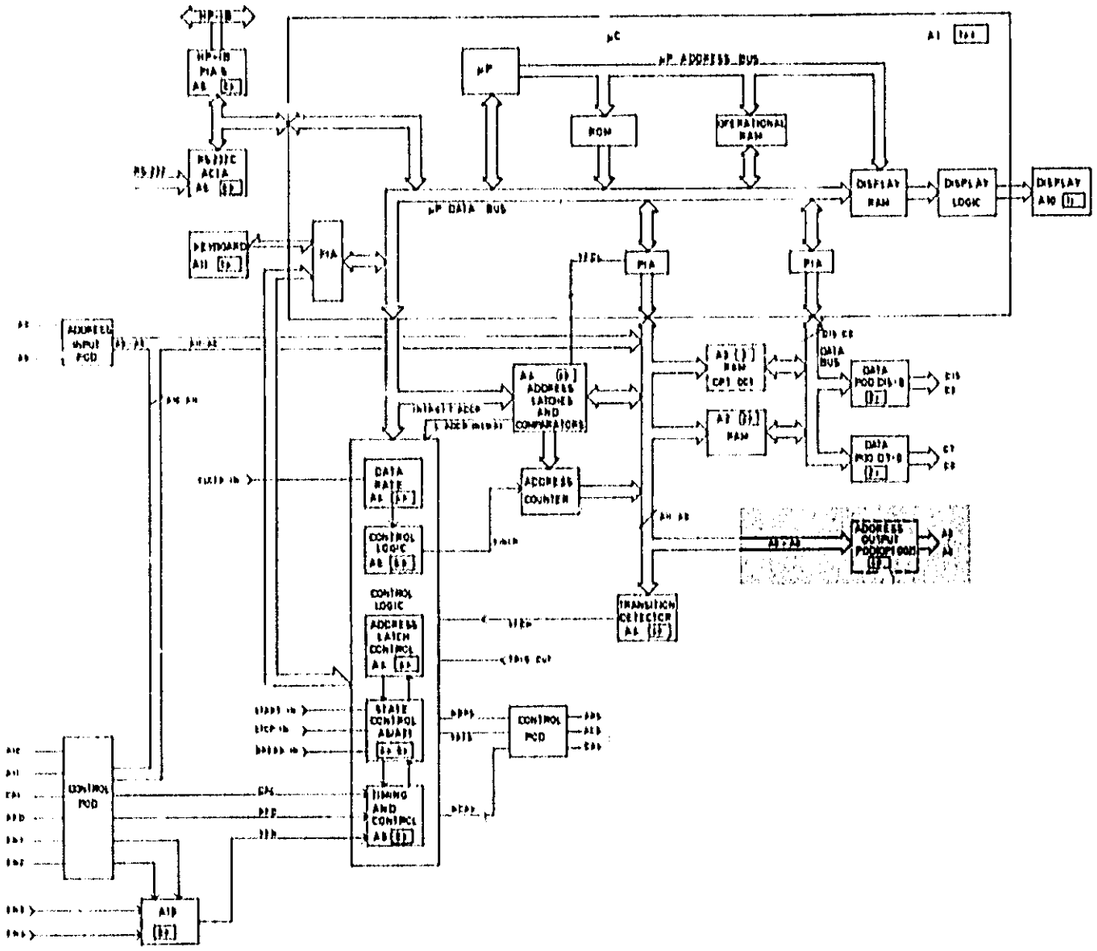
4C



4D

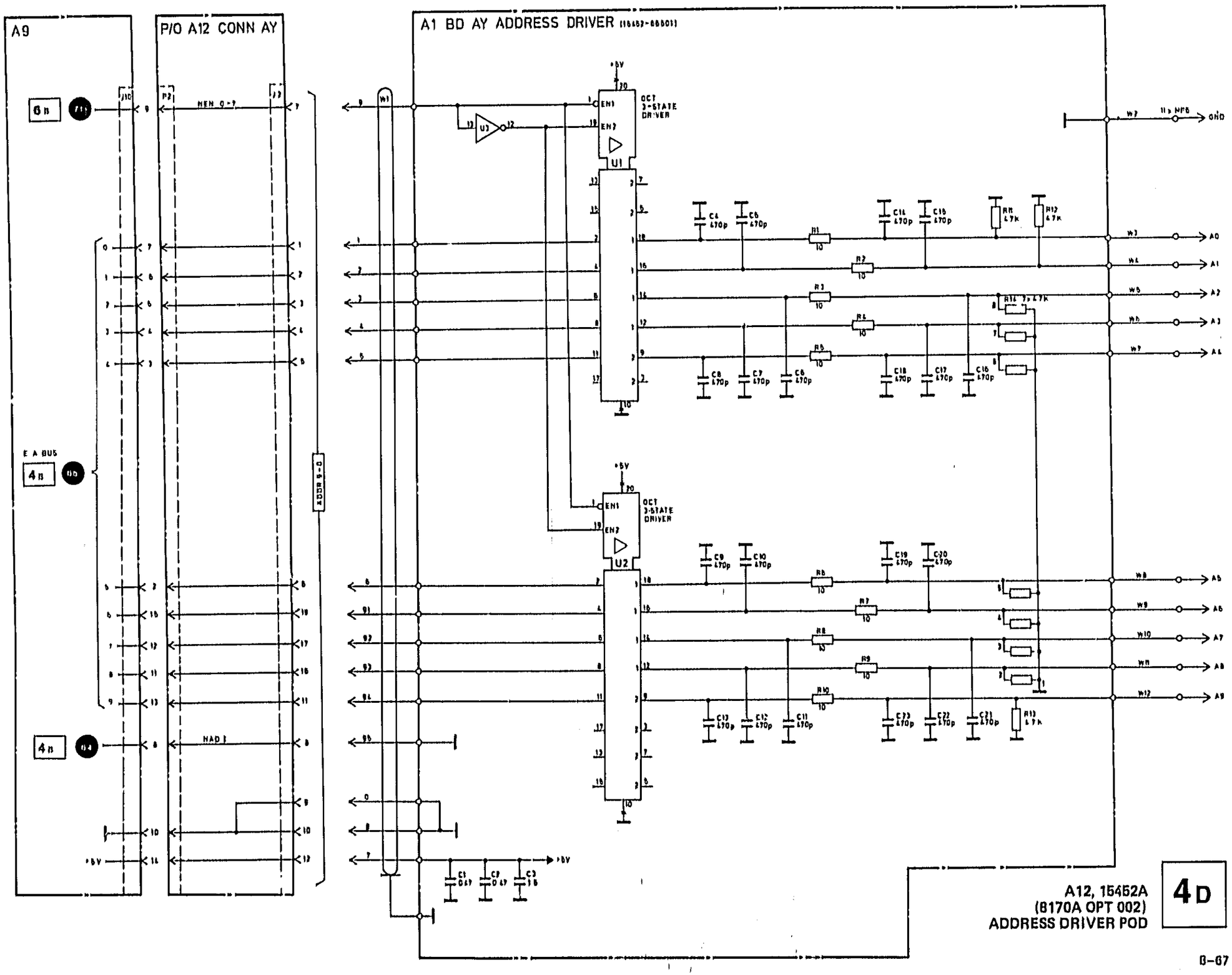
BD AY ADDRESS OUTPUT POD

SERVICE SHEET 4D LOCALIZER



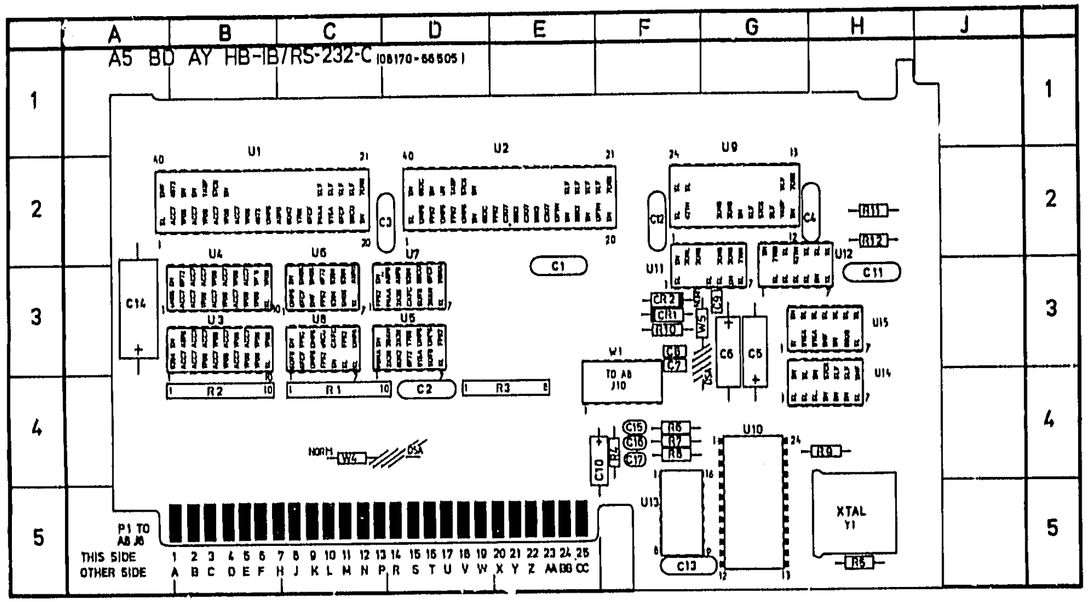
8-4D-1 REPAIR PROCEDURES

8-4D-2 Refer to § 8-2C-1 for replacement of A12 or associated front panel connectors.

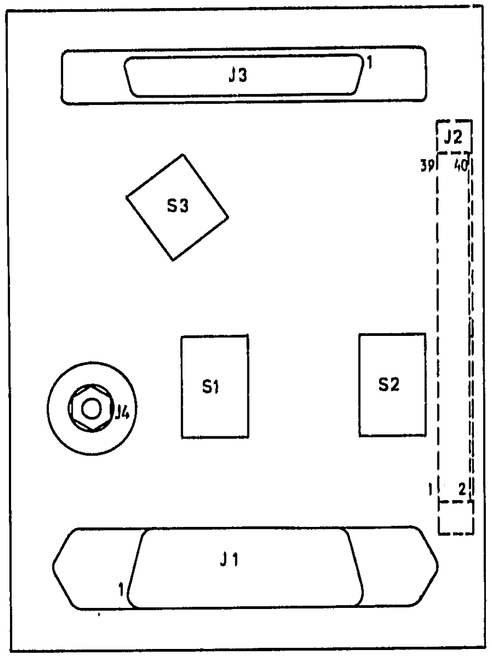


A12, 15452A
(8170A OPT 002)
ADDRESS DRIVER POD

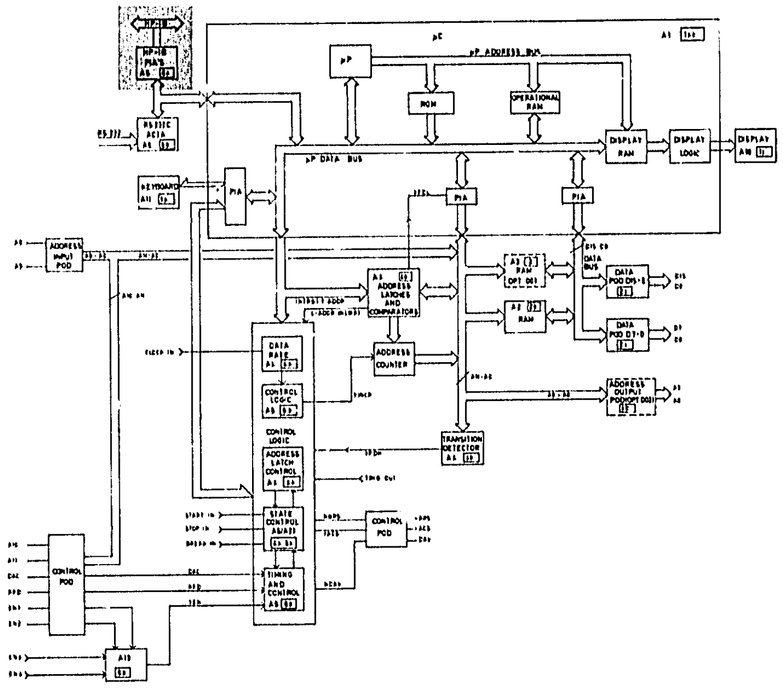
4D



A20 BD AY INTERFACE CONNECTOR 08170-66520



SERVICE SHEET 5A LOCALIZER



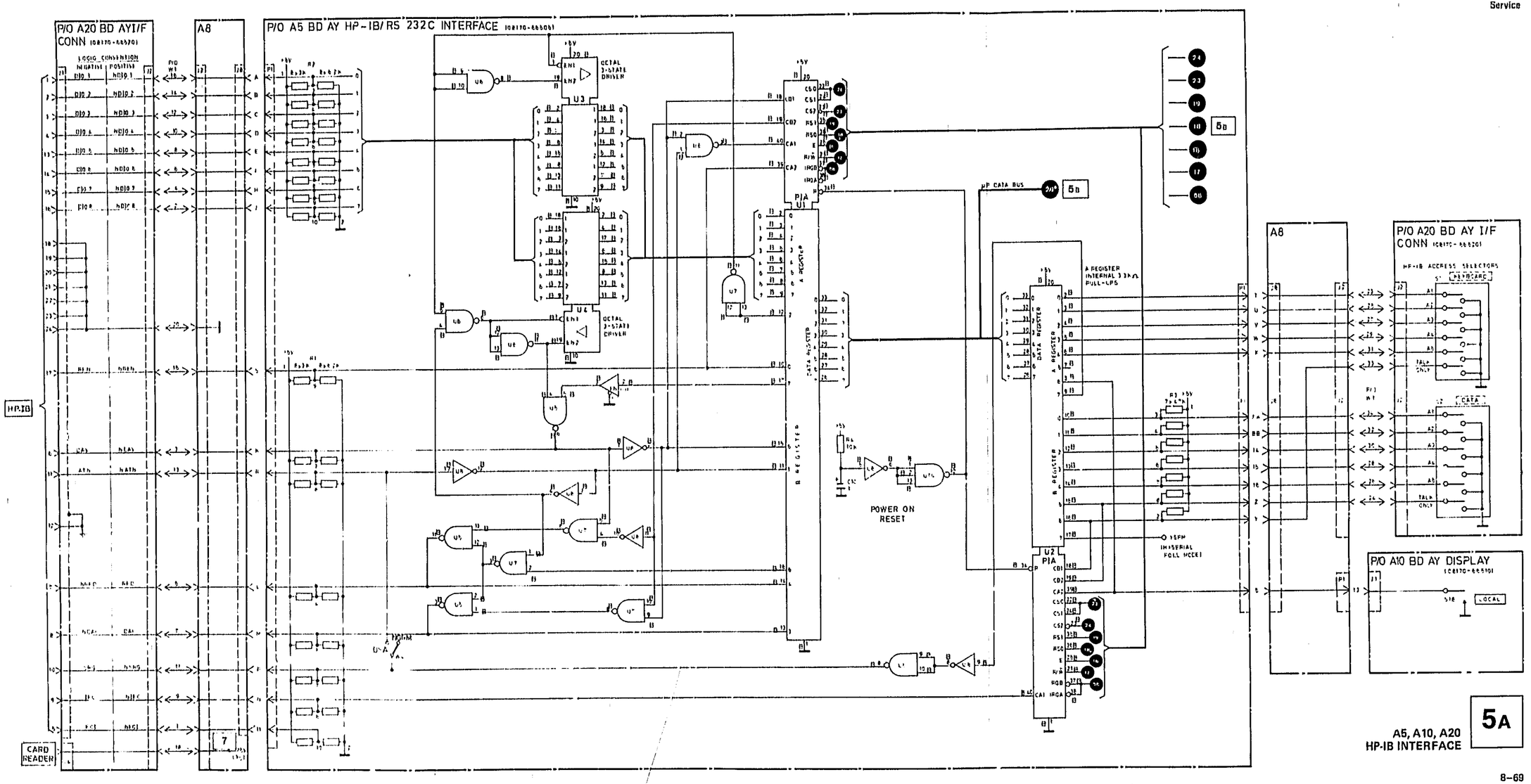
DSA Routine B	SH = 3374
5004A	8170A BD AY A1 Testpoint
START, STOP	G/H
CLOCK	CLK
GROUND	GND

Set the 8170A as follows:
Jumpers A5W4, A5W5 to DSA,
both Address Selectors (rear panel to III III
set BAUD RATE to 150 (rear panel),
set A1S1 to T,
press A1S2 to R,
press the B key on the front panel.
In serial numbers 00115 and below, it may be necessary to switch the instrument off (as well as setting A1S1 to NORMAL) in order to leave DSA routine B.

REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC
C1	E-3	R1	C-4	U4	B-3
C2	D-4	R2	B-4	U5	D-3
C3	C-2	R3	E-4	U6	C-3
C4	H-2	R4	F-4	U7	D-3
C5	G-3	R5	H-5	U8	C-3
C6	G-3	R6	F-4	U9	G-2
C7	F-4	R7	F-4	U10	G-4
C8	F-3	R8	F-4	U11	G-3
C9	G-3	R9	H-4	U12	G-3
C10	E-4	R10	F-3	U13	F-5
C11	H-3	R11	H-2	U14	H-4
C12	F-2	R12	H-2	U15	H-3
C13	F-5	W4	C-4	U16	H-5
C14	A-3	W5	F-3	Y1	F-4
CR1	F-3	U1	B-2	W1	F-4
CR2	F-3	U2	E-2		
MP4		U3	B-3		

5A

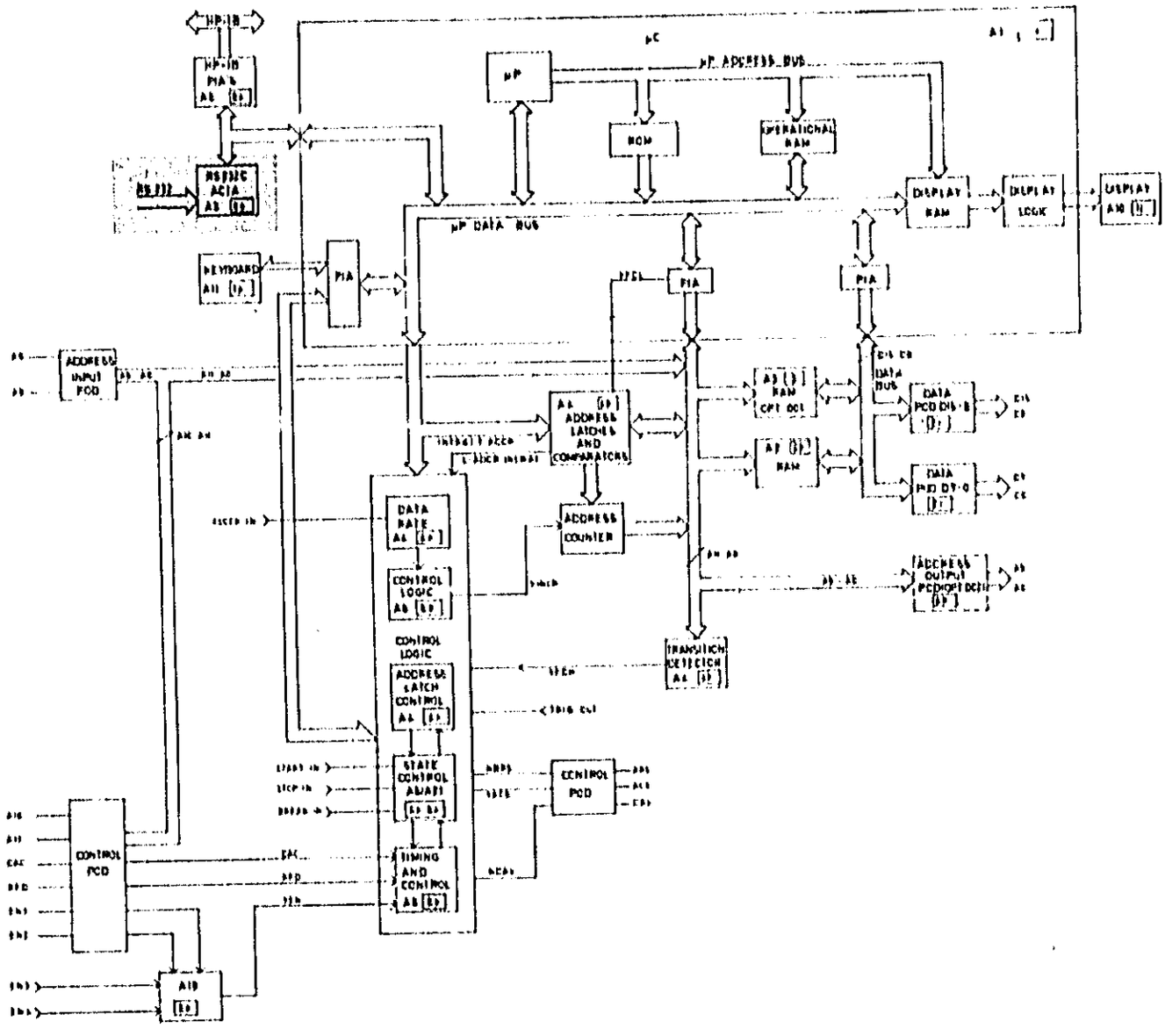
A5 BD AY HP-IB/RS-232-C, A20 BD AY I/F CONN



5A

A5, A10, A20 HP-IB INTERFACE

SERVICE SHEET 5B LOCALIZER



5 B

P/O A20 BD AY I/F CONNECTOR (08170-66670)

P/O A5 BD AY HP-IB/RS 232C INTERFACE (08170-66506)

A8

A8

5A

1C

4A

BAUD RATE

110
150
300
600
1200
2400
4800
9600

NOT USED

SIGNAL GROUND

DTR

T DATA

R DA

CTS

DSR

R DATA

RS 232C

BAUD-RATE GENERATOR

RATE SELECT

SEL

U13

U10

U11

U9

ACIA

SER/PAR CONN I/F ADAPTER

LINE RCVR LEVEL CONV

LINE DRIVER

CLEAR TO SEND (LOW WHEN INPUT OPEN)

SIGNAL DATA IN (HIGH WHEN INPUT OPEN)

LOW WHEN INPUT OPEN

REQUEST TO SEND

SERIAL DATA OUT

NORMAL

DSA

W5

BAUD RATE DETECT FOR 1 BIT START BIT

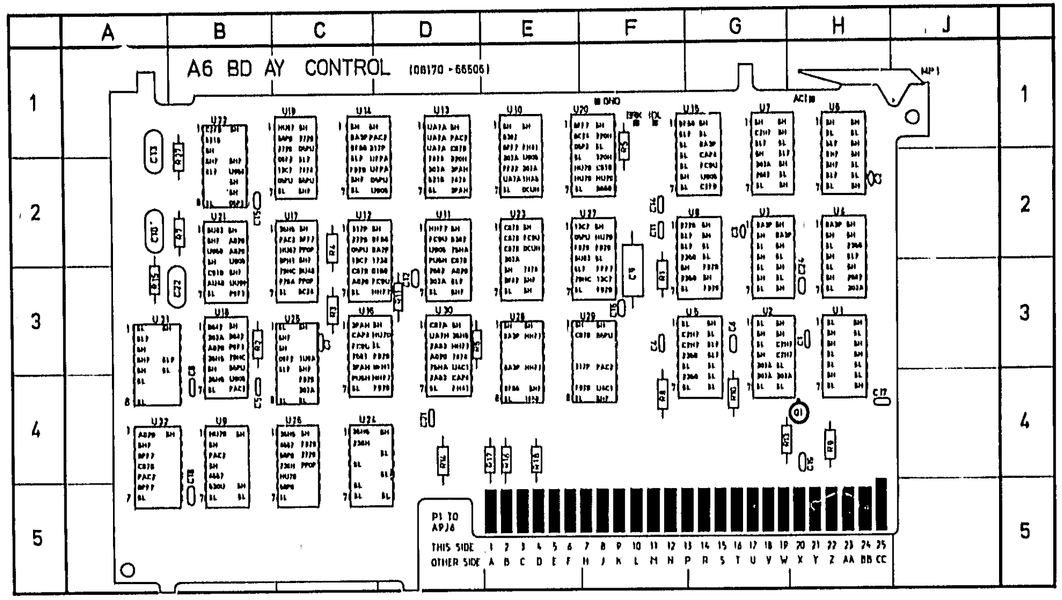
P DATA BUS

D0 D1 D2 D3 D4 D5 D6 D7

DSA ROUTINE

A5, A20
RS 232C INTERFACE

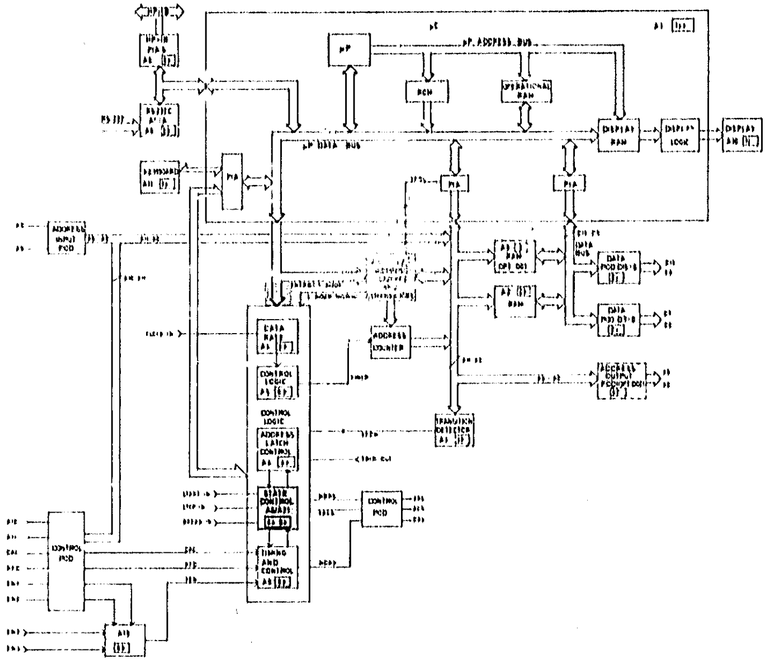
5B



DSA Routine C SH = 1658	follows:
5004A 8170A BD AY A1 Testpoint START, STOP — G/H CLOCK — CLK GROUND — GND	Jumpers A4W6, A4W7 to DSA, ENable switches 1, 2, 3, 4 (rear panel) to OFF, RFD switch to LOW, DAV switch to HIGH, DELAY ADJ to MIN, Control Pod 15454A connected, Set A1S1 to T, press A1 S2 to R, press the C key on the front panel.

REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC
C1	H-3	C21	D-4	R27	B-1	U19	C-1
C2	H-2	C22	B-3	U1	H-3	U20	F-1
C3	G-2	C24	H-3	U2	G-3	U21	B-2
C4	F-3	C25	B-4	U3	G-2	U22	B-1
C5	B-4	C1	H-4	U4	H-2	U23	E-2
C6	G-3	R1	F-3	U5	G-3	U24	C-4
C7	C-3	R2	B-3	U6	H-1	U25	C-3
C8	B-4	R3	C-3	U7	G-1	U26	C-4
C9	F-3	R4	C-2	U8	G-2	U27	F-2
C10	A-2	R5	F-1	U9	B-4	U28	E-3
C11	F-2	R6	D-3	U10	E-1	U29	F-3
C12	D-3	R7	B-2	U11	D-2	U30	D-3
C13	A-1	R8	F-4	U12	C-2	U31	A-3
C14	F-2	R9	H-4	U13	D-1	U32	A-4
C15	B-2	R10	G-4	U14	C-1	MP1	J-1
C16	F-3	R11	D-3	U15	G-1		
C17	H-4	R13	H-4	U16	C-3		
C18	B-5	R14	D-4	U17	C-2		
C19	H-4	R15	A-3	U18	B-3		

SERVICE SHEET 6A LOCALIZER



6A

A6 BD AY CONTROL

8-6A-1 STATE CONTROL

8-6A-2 At power on, idle state is automatically implemented, R5 and C9 generate a pulse so that the Active and Break state latches are reset (YACT and YBRK low) and that the Idle state latch is set (YIDL high). The Signal latches are also reset. Entry into Break state from Idle state is prevented by the Q output of the Idle state latch which inhibits the EXBREAK signal.

8-6A-3 Incoming EX START, EX BREAK, EX STOP signals clock the corresponding Signal latch, causing one of the Q outputs to go high. This transition clocks the State latches, and the corresponding State signal goes high. At the same time the Signal latches are reset.

8-6A-4 Keyboard-generated State changes are executed by the YRUN and YSTOP signals clocked by YCSB.

8-6A-5 YEDB holds the reset line of the Signal latches low during data transfer from μP to RAMs so that the operating state cannot be changed while this is taking place.

8-6A-6 At the end of a single cycle, the NSCR signal returns the 8170A to the Idle state.

8-6A-7 MODE LATCHES 1 AND 2

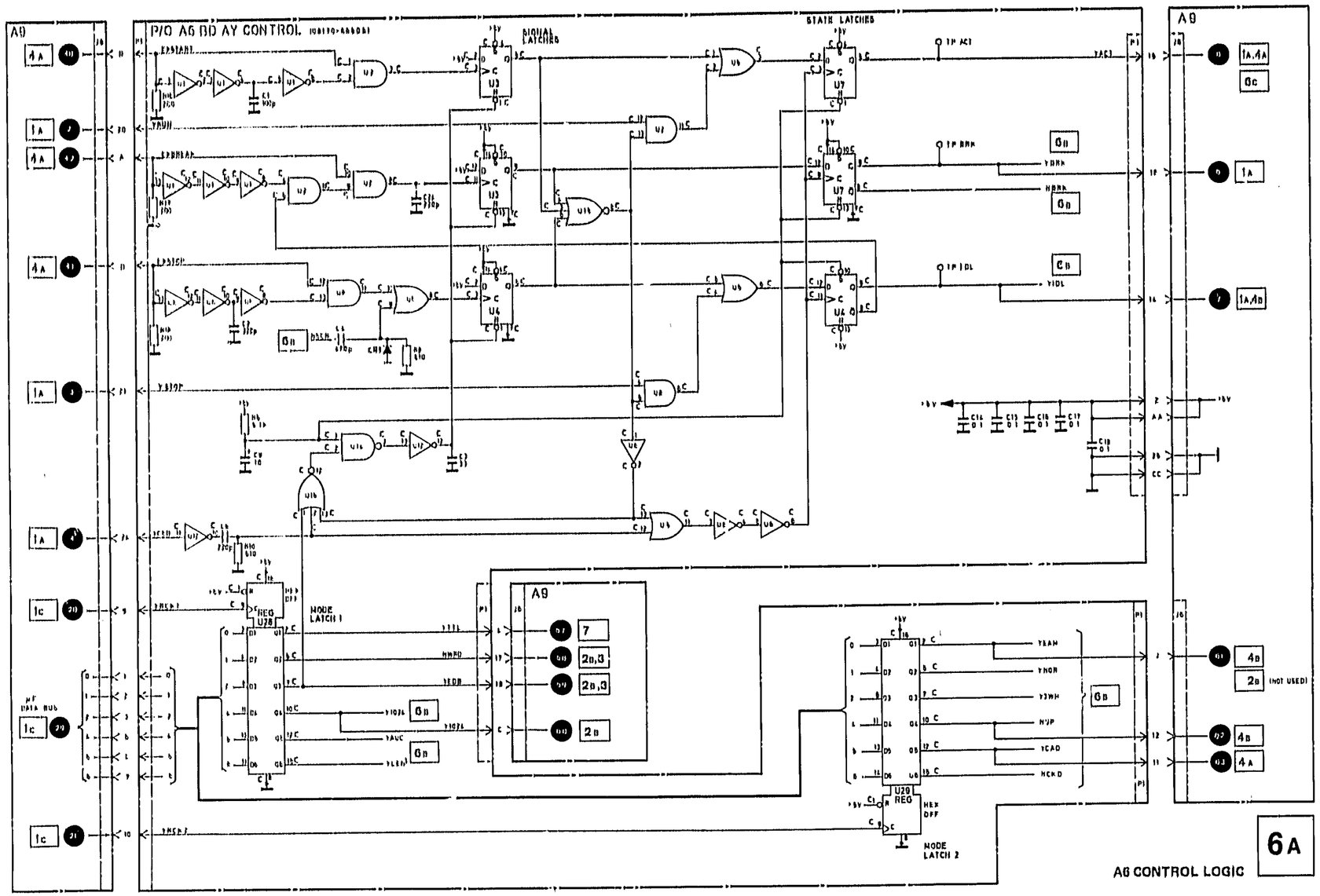
8-6A-8 Refer to the following tables.

MODE LATCH 1

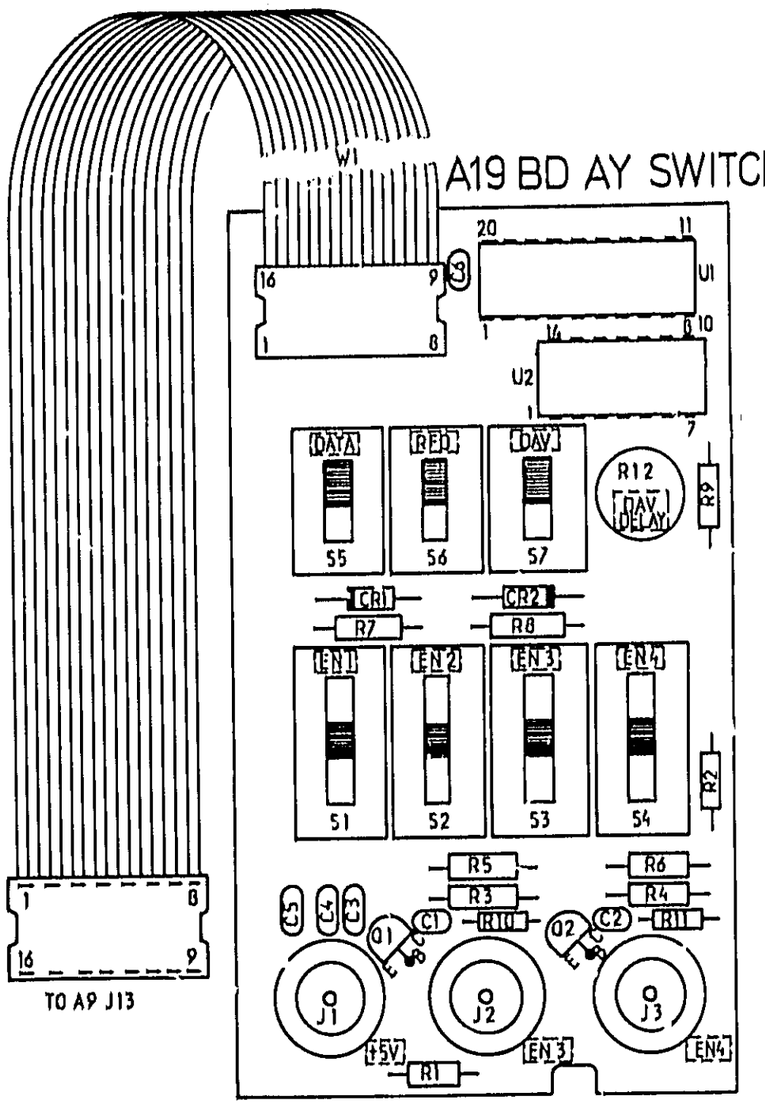
Signal	μP Data Bus Bit (Latched by YRCK1)	Condition
YTTL	0	HI=TTL OUTPUT selected.
NWRD	1	HI=μP writes into freely programmable RAM; LO=RAM writes into data bus.
YEDB	2	HI=enables RAM output.
Y1024	4	HI=8 BIT BUS selected.
YAUC	5	HI=AUTO CYCLE selected.
YLEN'	6	Address count forward: LO=address change from L.ADDR minus 1 to L.ADDR, Address count back (MAN BACK): LO=decrement address counter, HI=increment address counter.

MODE LATCH 2

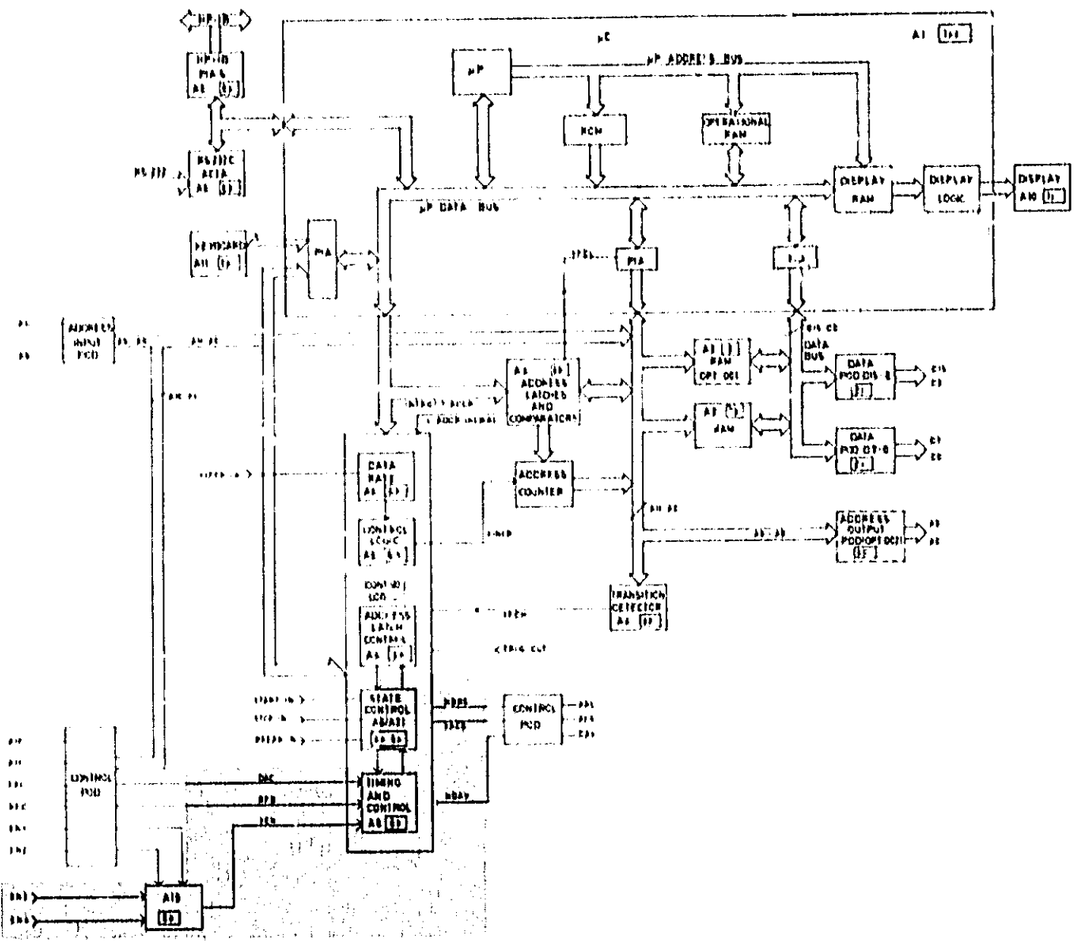
Signal	μP Data Bus Bit (Latched by YRCK2)	Condition
YEAM	0	HI=EXT ADDR mode selected.
YNOR	1	HI=INT ADDR mode, INT/EXT/MAN clock selected, LO=EXT ADDR or HANDSHAKE mode selected.
Y3WH	2	HI=3-WIRE HANDSHAKE selected.
NUP	4	HI=Decrement address counter.
YCAD	5	INT/EXT ADDR mode, man FWD: HI=FWD key pressed, INT ADDR mode, man BACK: 5 pulses for address counter increment/decrement/increment.
NCKD	6	LO=Gate during first four YCAD pulses



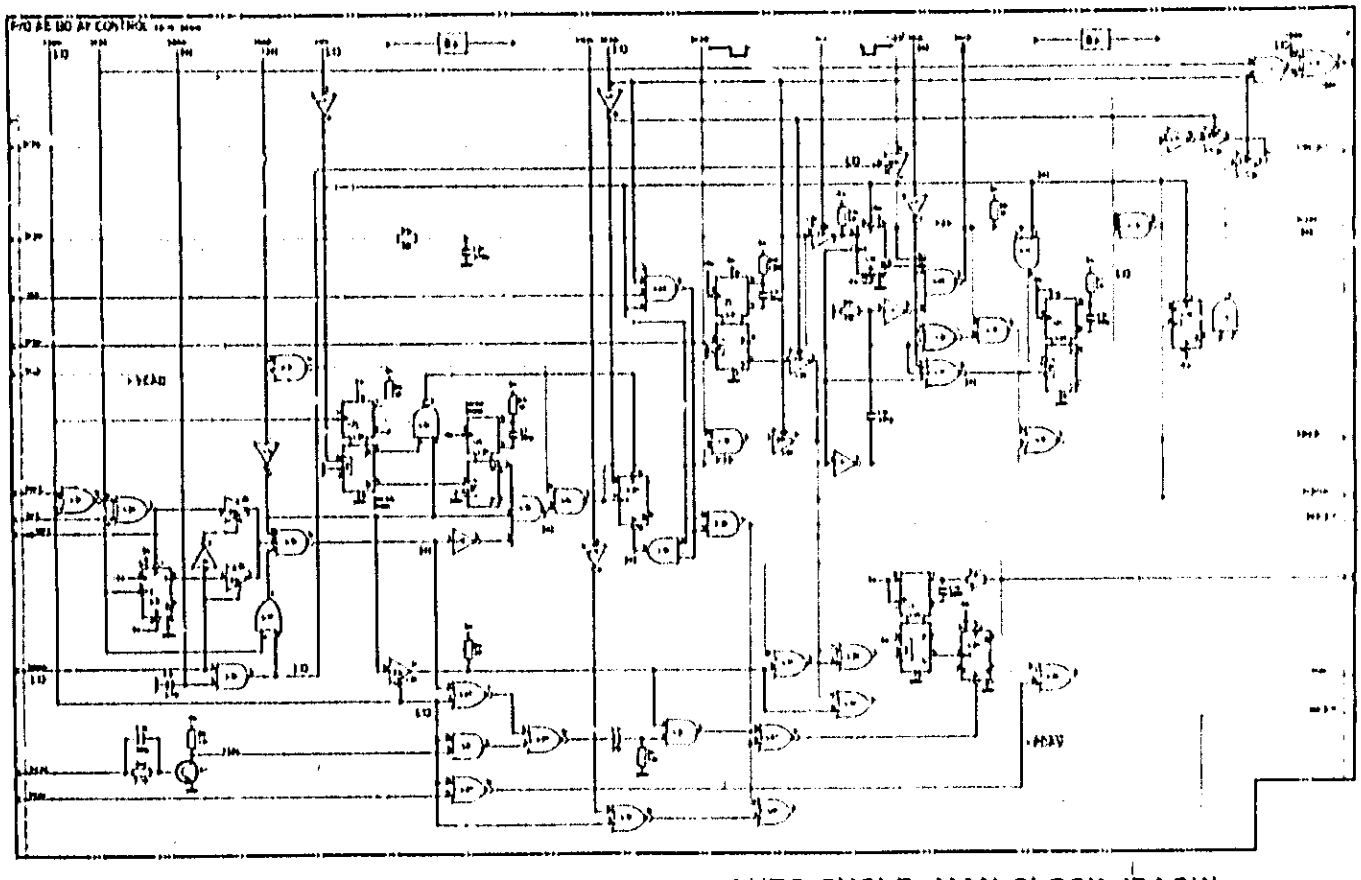
A19 BD AY SWITCH



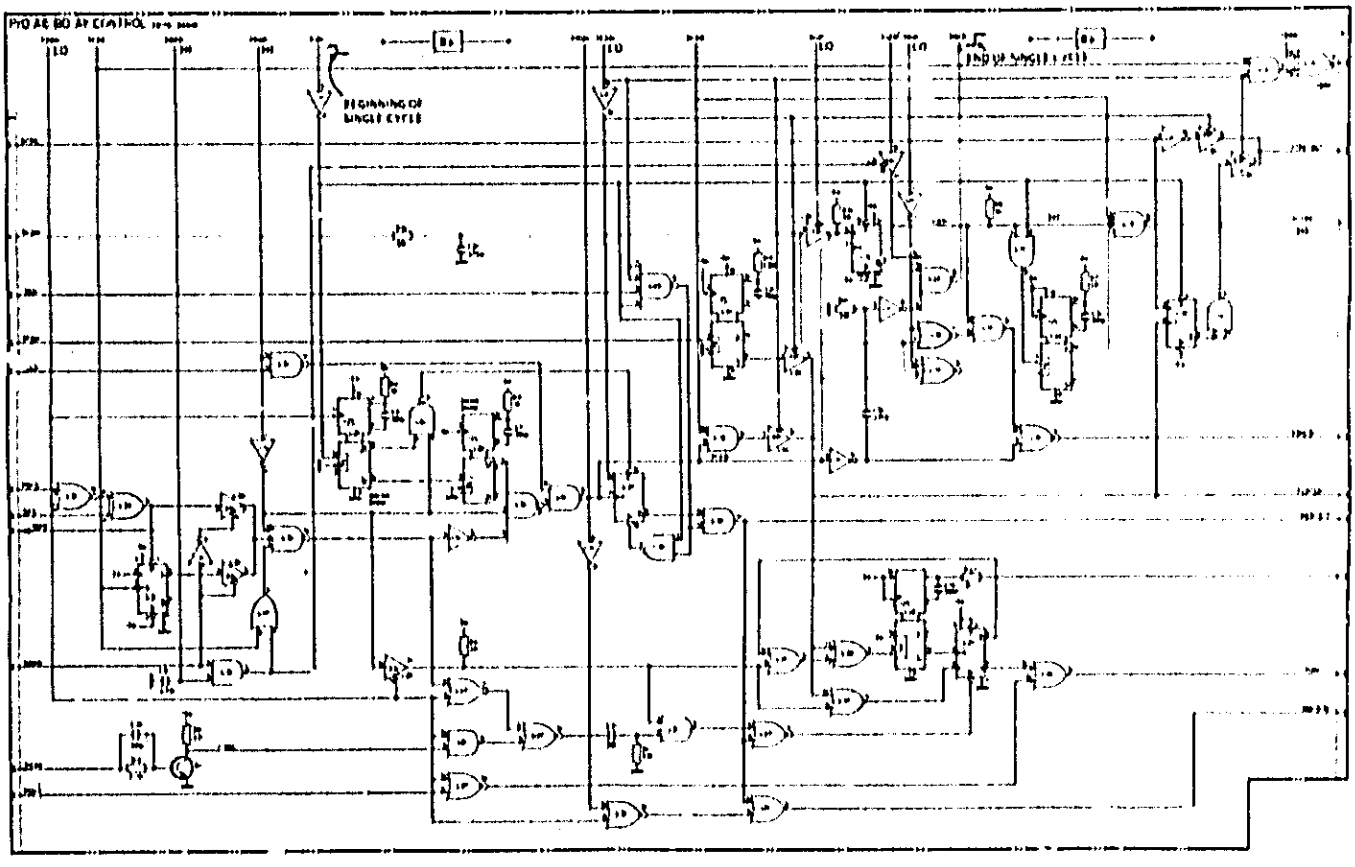
SERVICE SHEET 6B LOCALIZER



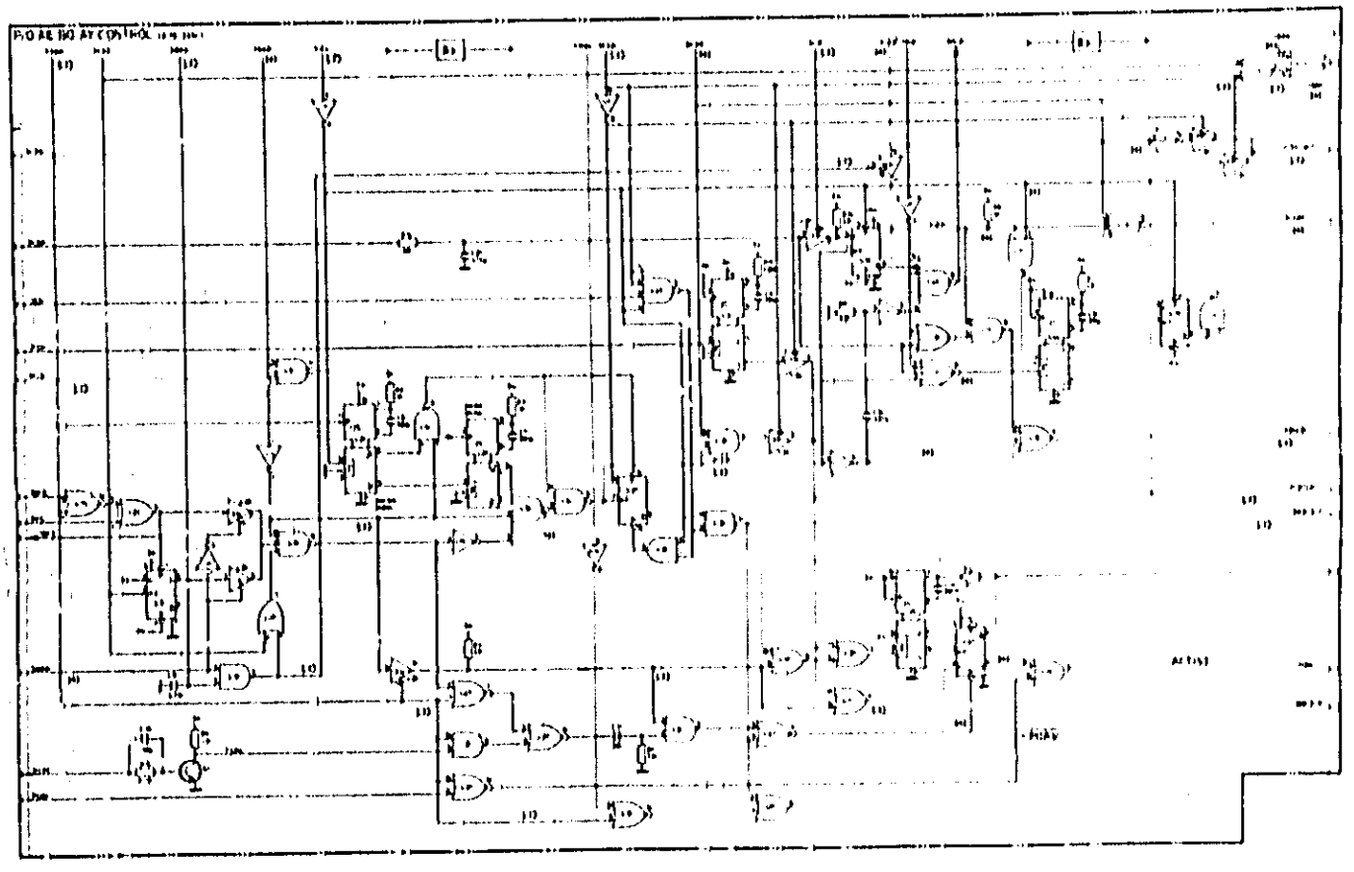
6B



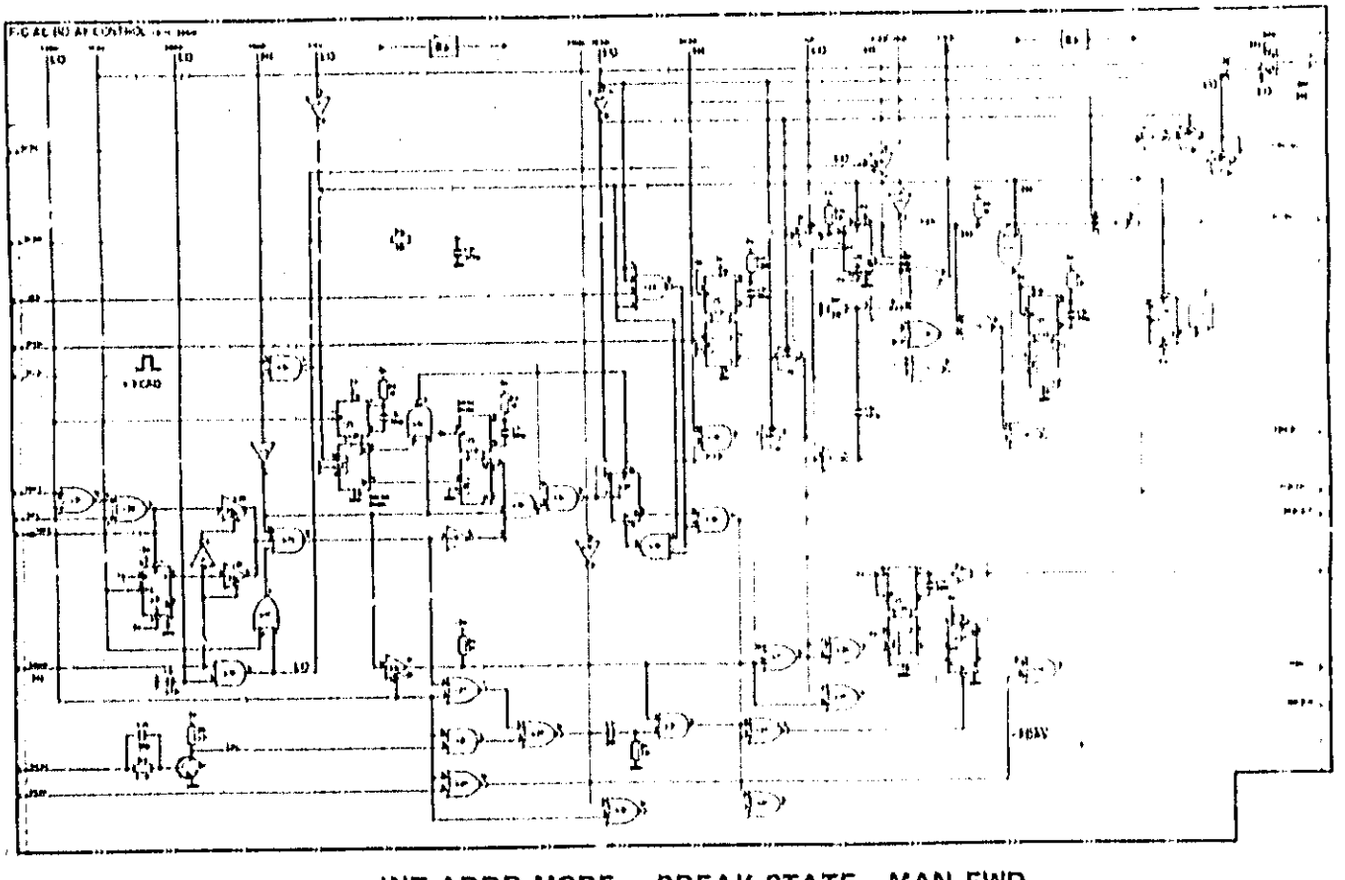
INT ADDR MODE ACTIVE STATE AUTO CYCLE MAN CLOCK (BACK)



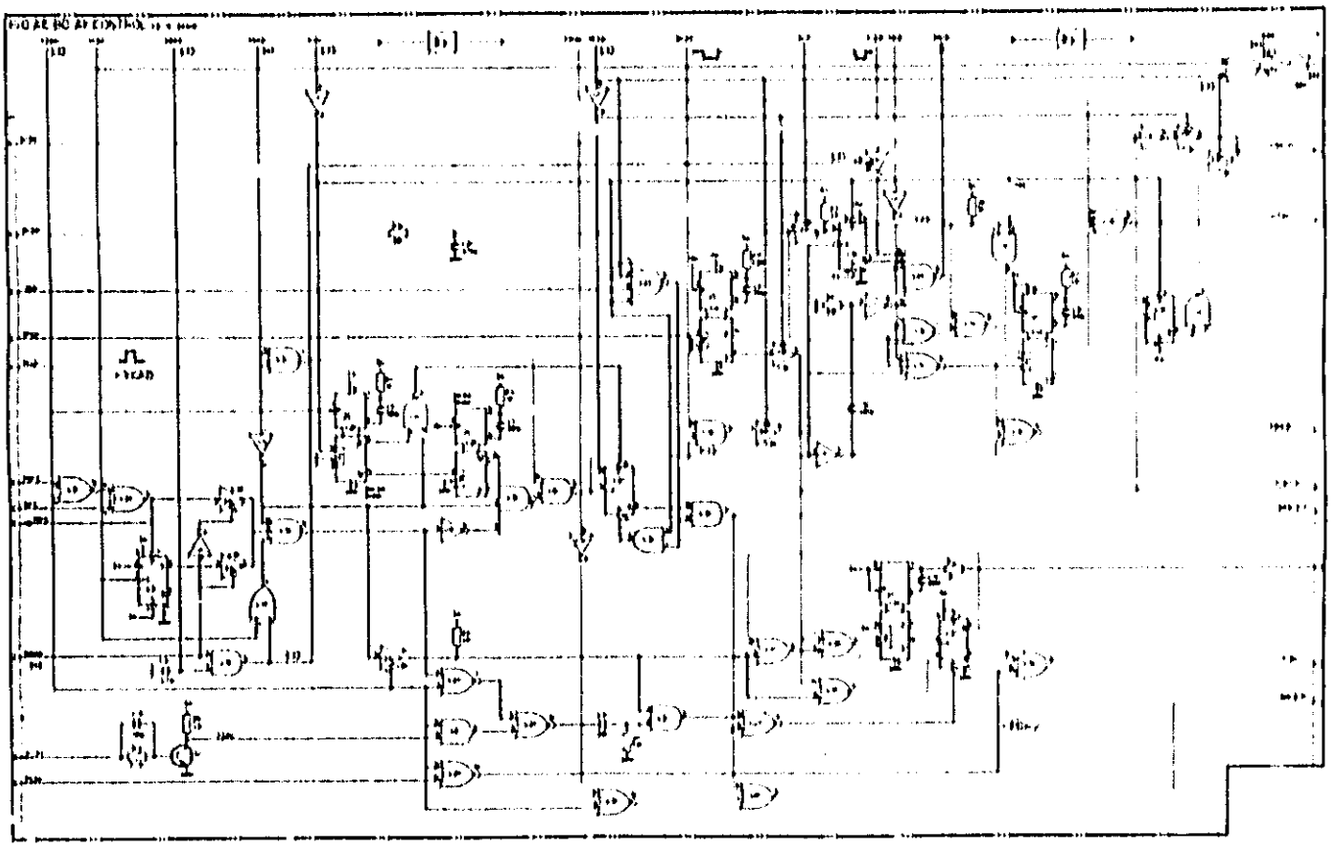
INT ADDR MODE SINGLE CYCLE



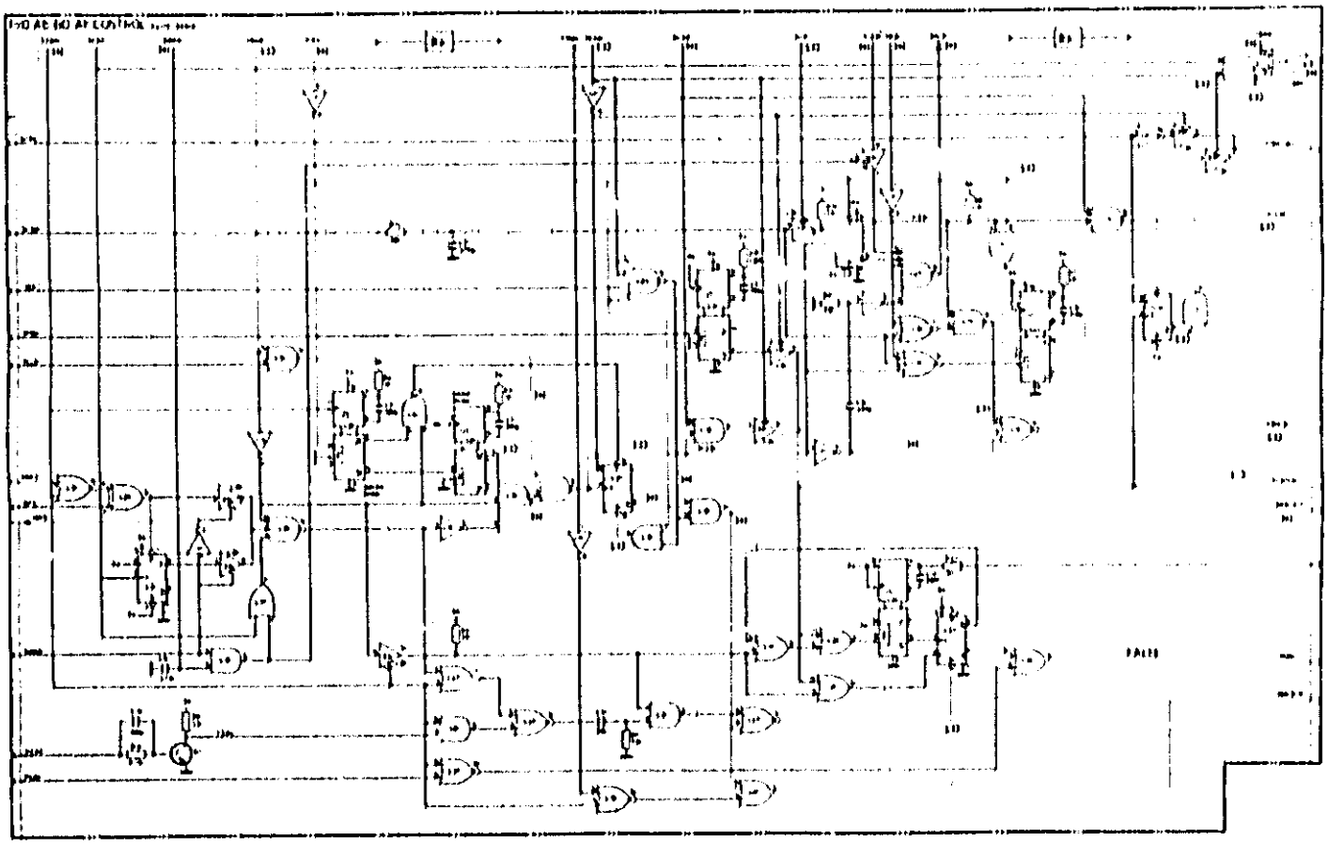
INT ADDR MODE BREAK STATE



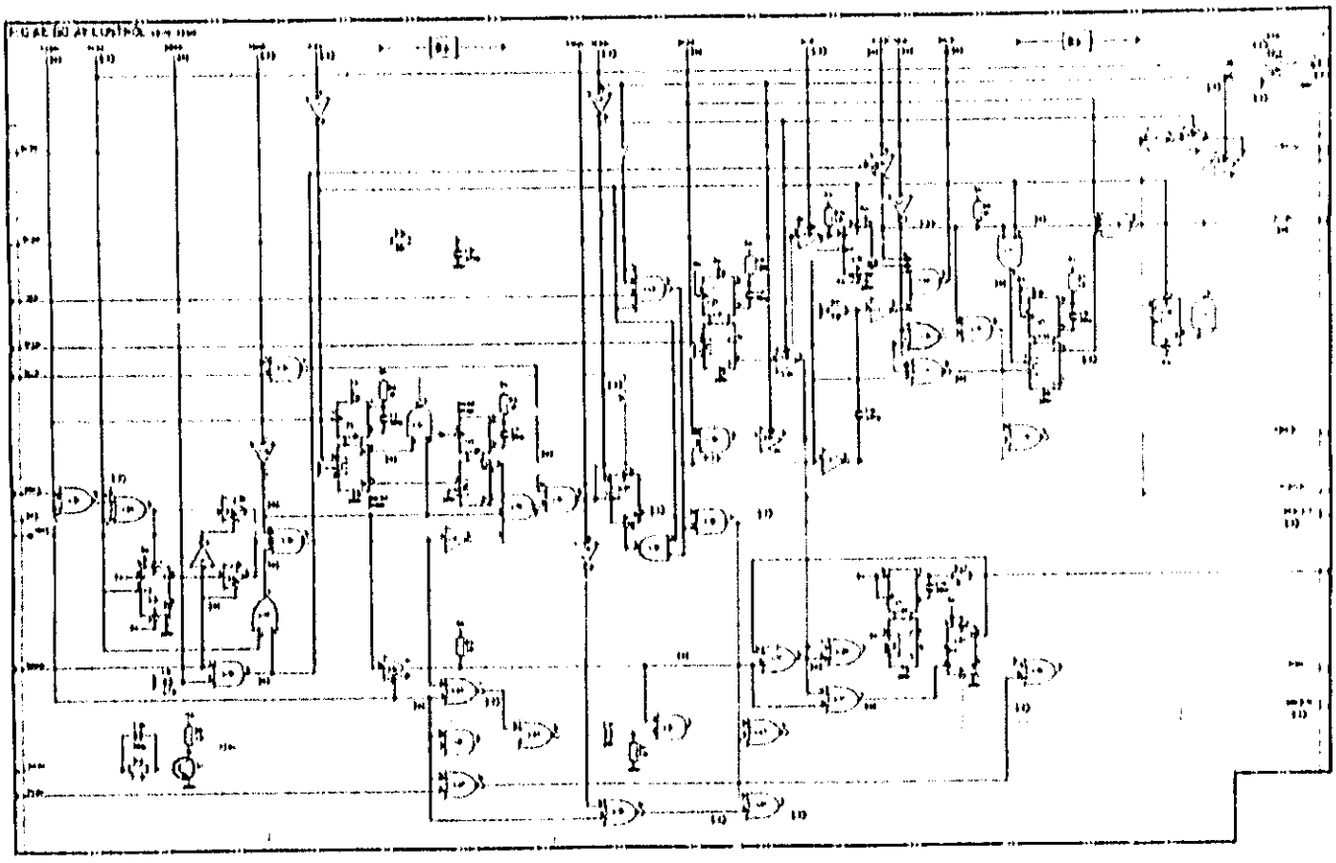
INT ADDR MODE BREAK STATE MAN FWD



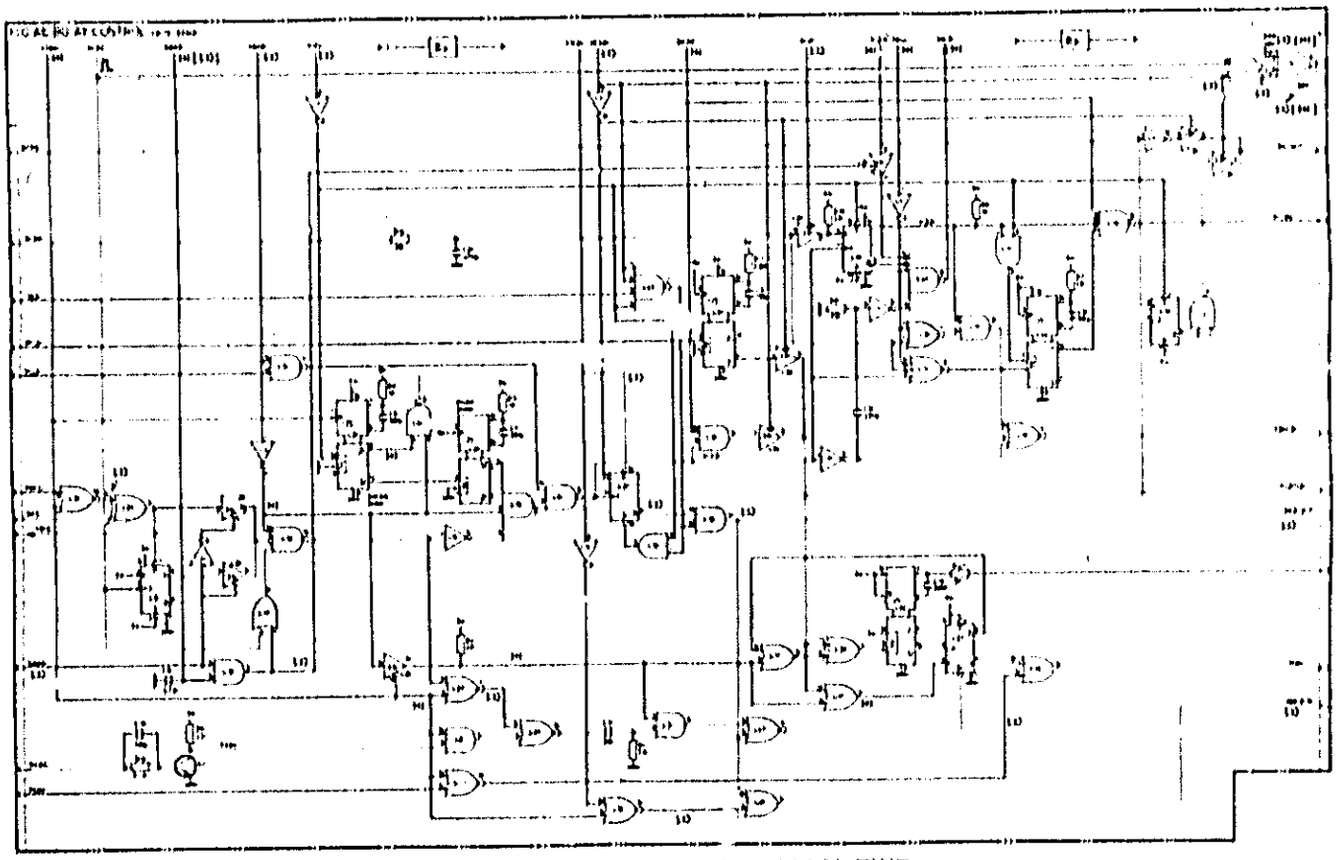
INT ADDR MODE BREAK STATE MAN BACK



3-WIRE HANDSHAKE IDLE STATE

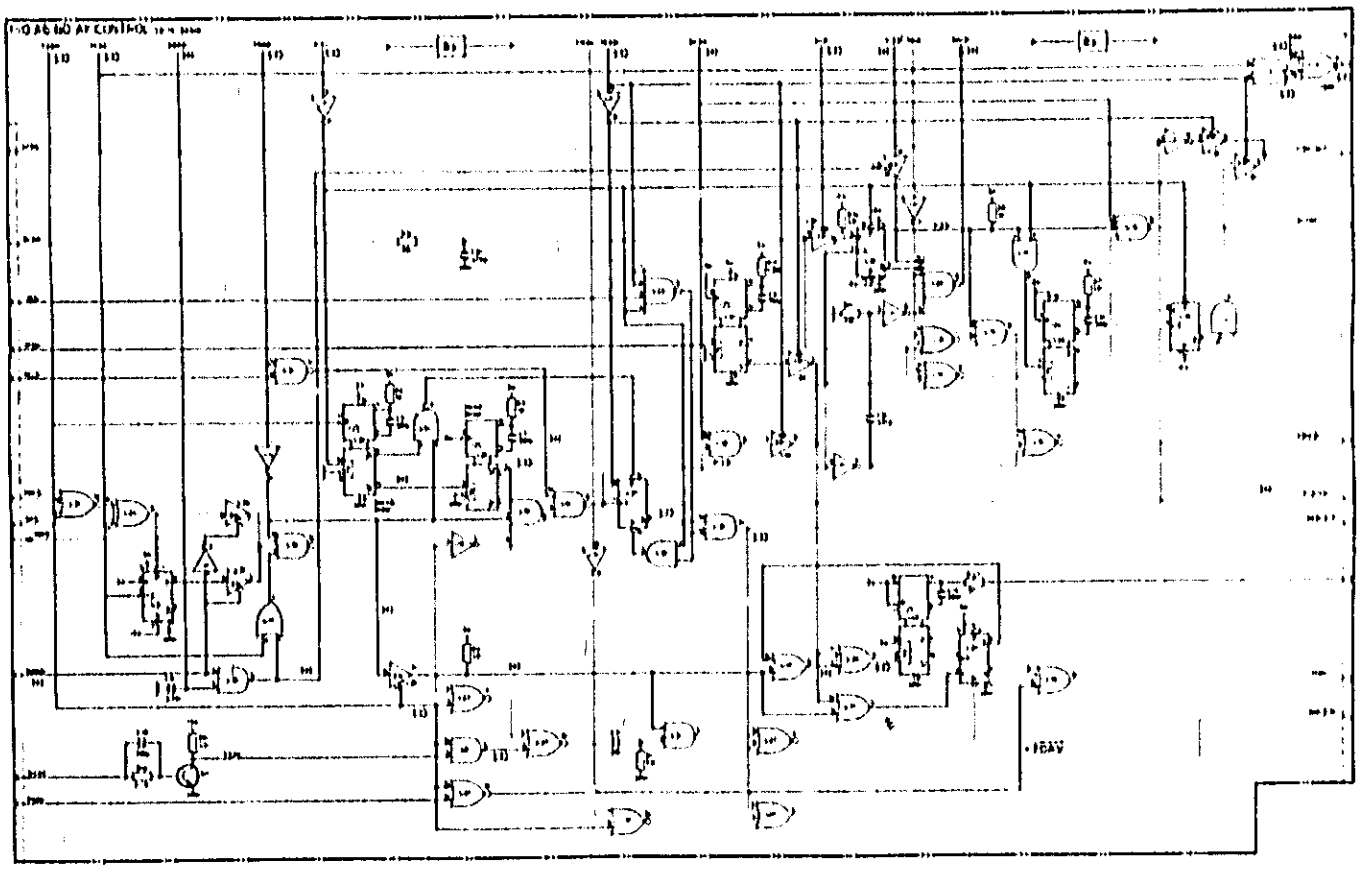


3-WIRE HANDSHAKE ACTIVE STATE

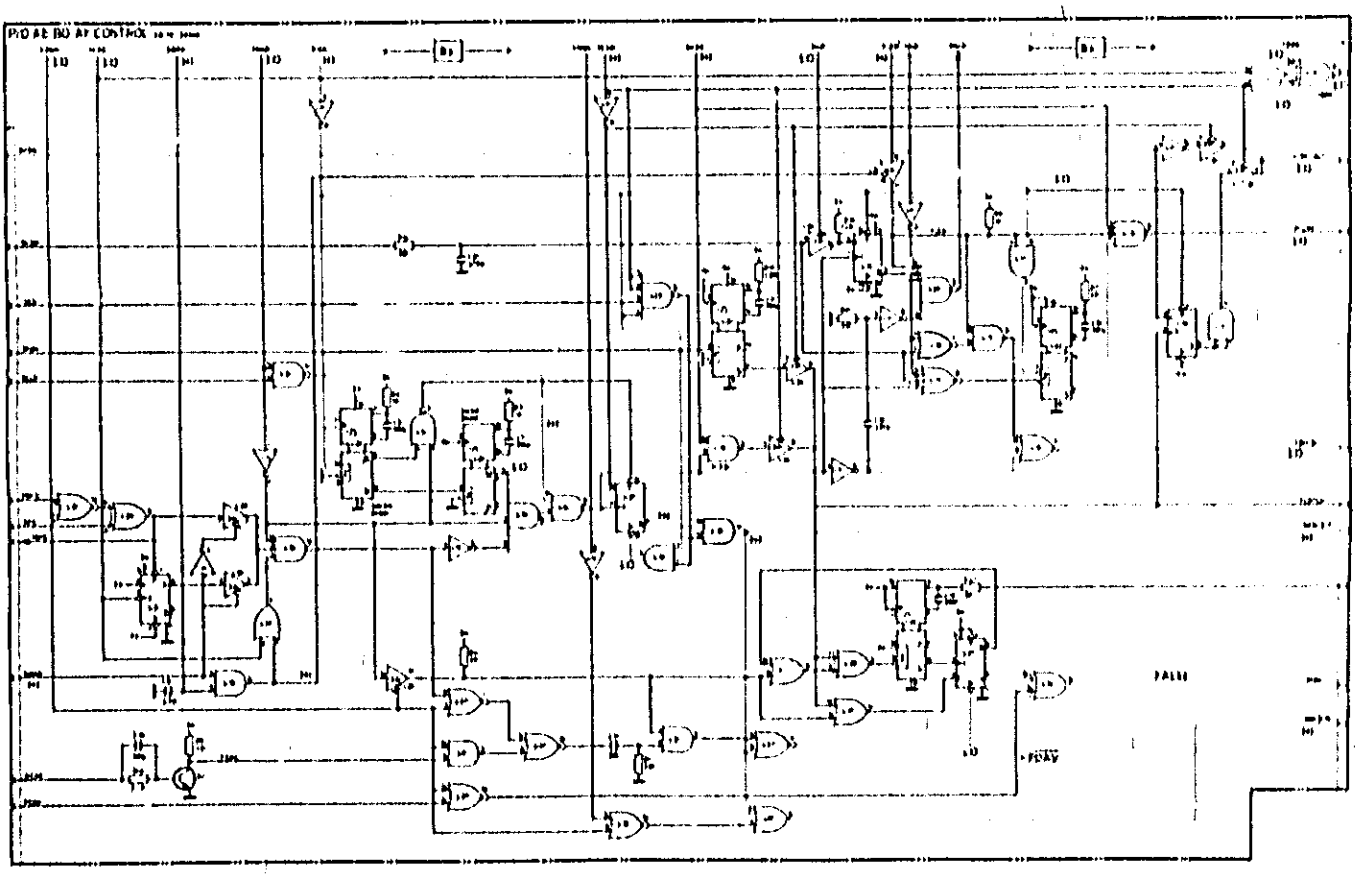


3-WIRE HANDSHAKE MAN FWD

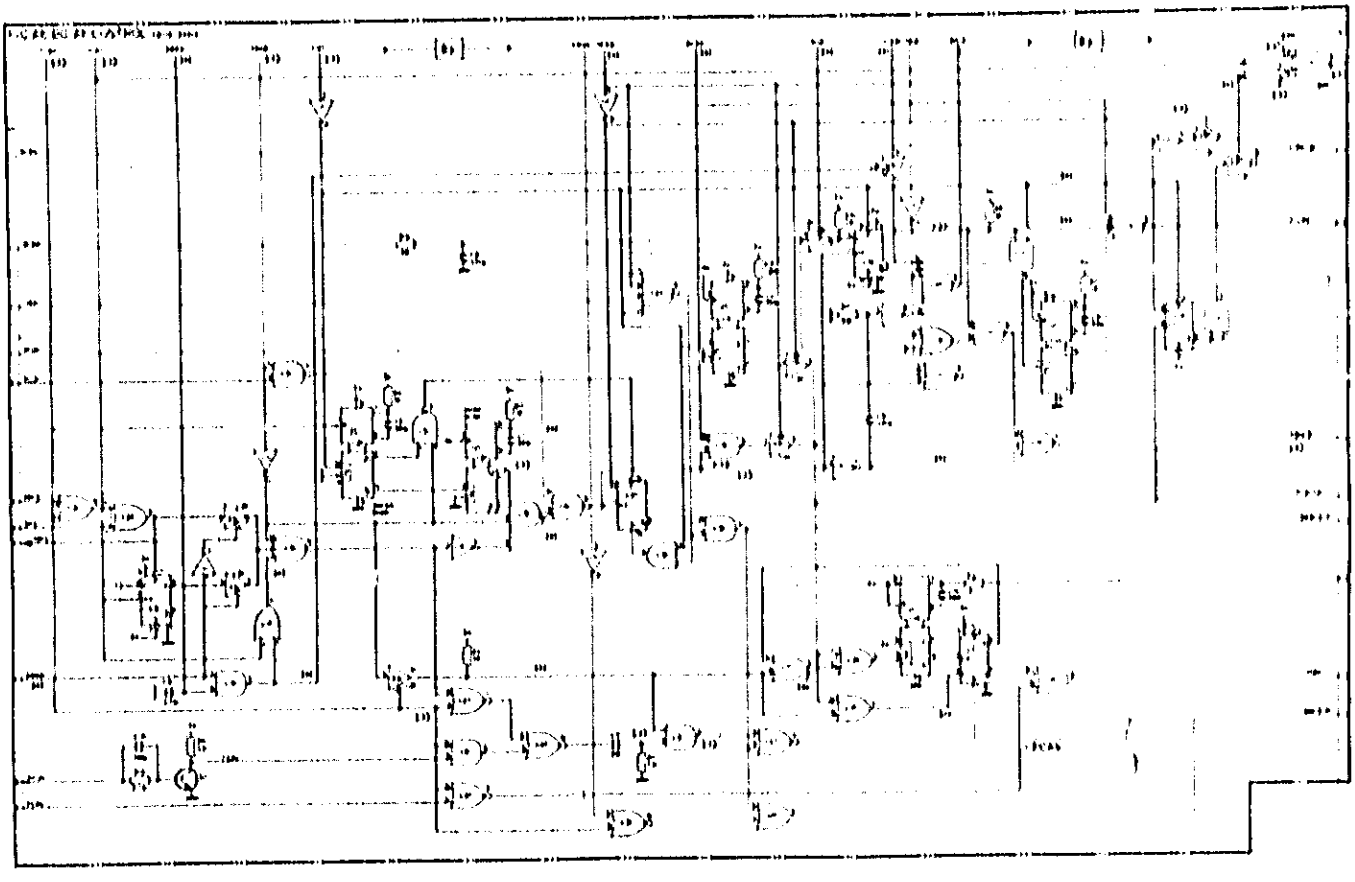
OR [BREAK STATE MAN FWD]. For NCKD, NUP, YLEN activity for MAN BACK, refer to INT MODE.



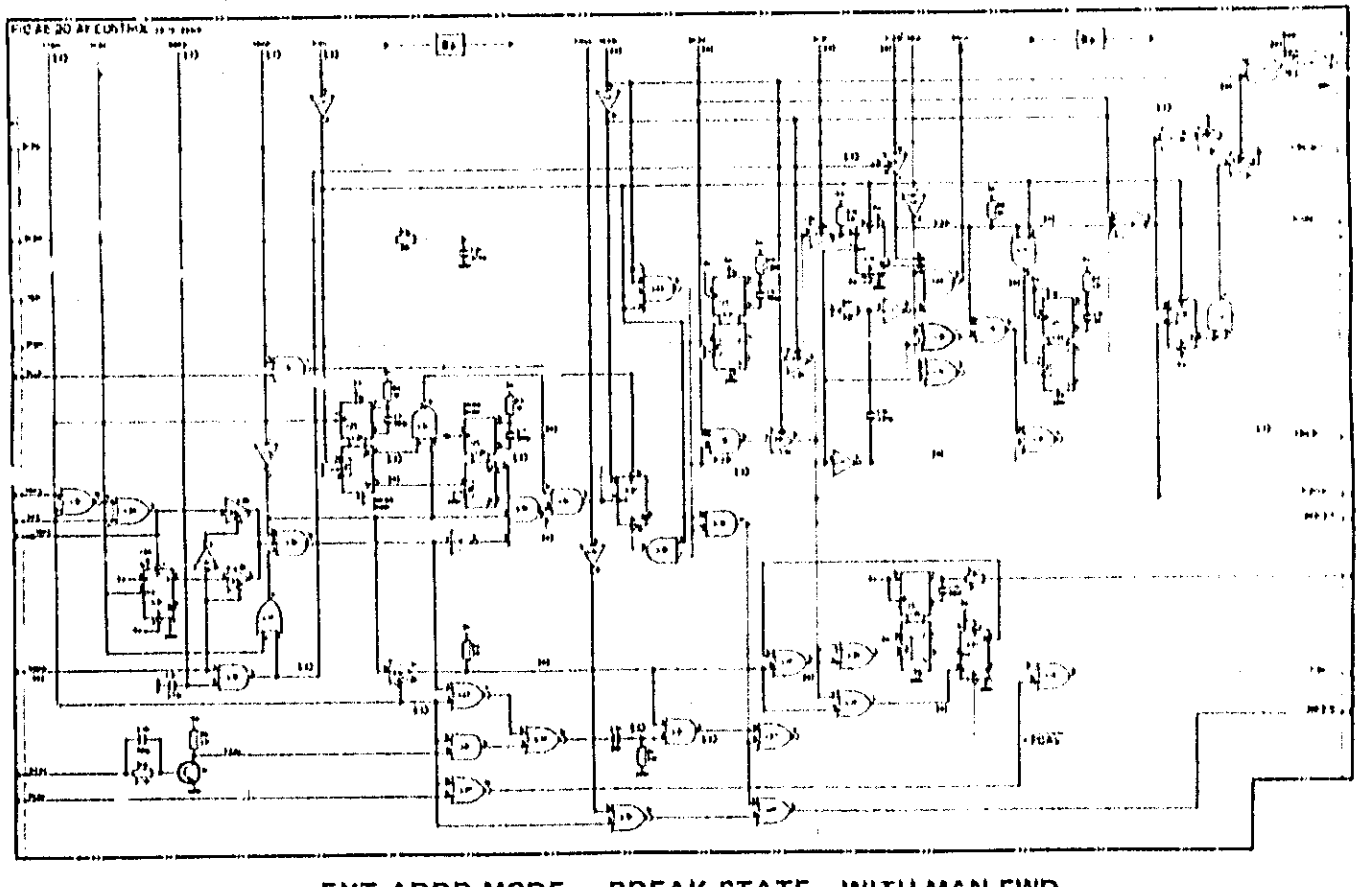
2-WIRE HANDSHAKE
(Refer to 3-WIRE HANDSHAKE for MAN FWD / BACK and IDLE STATE)



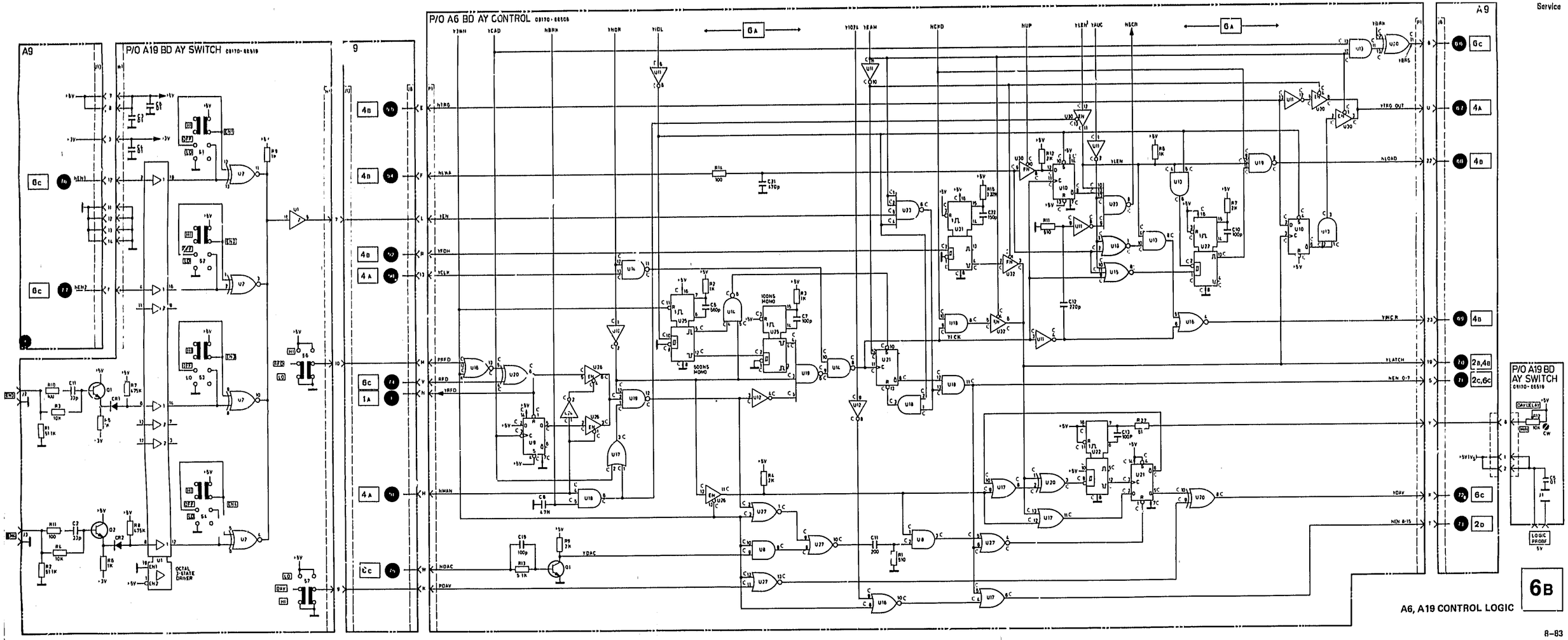
EXT ADDR MODE IDLE STATE



EXT ADDR MODE ACTIVE STATE



EXT ADDR MODE BREAK STATE WITH MAN FWD

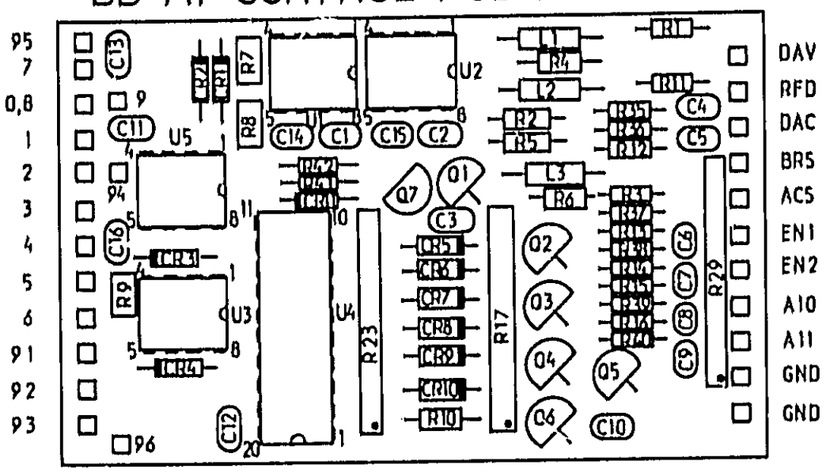


A6, A19 CONTROL LOGIC

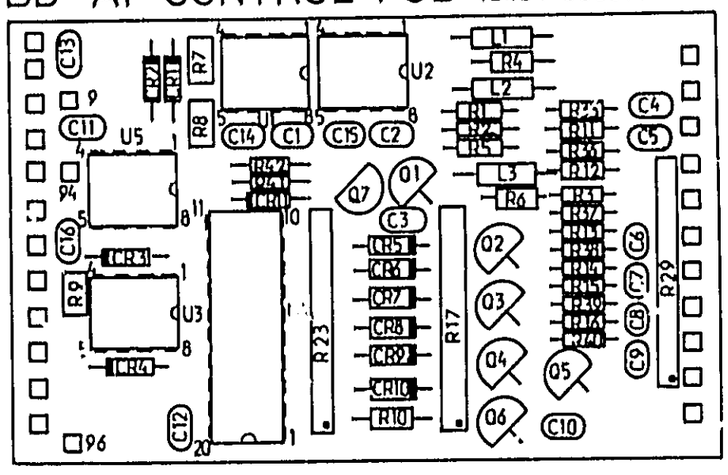
6B

DSA ROUTINE

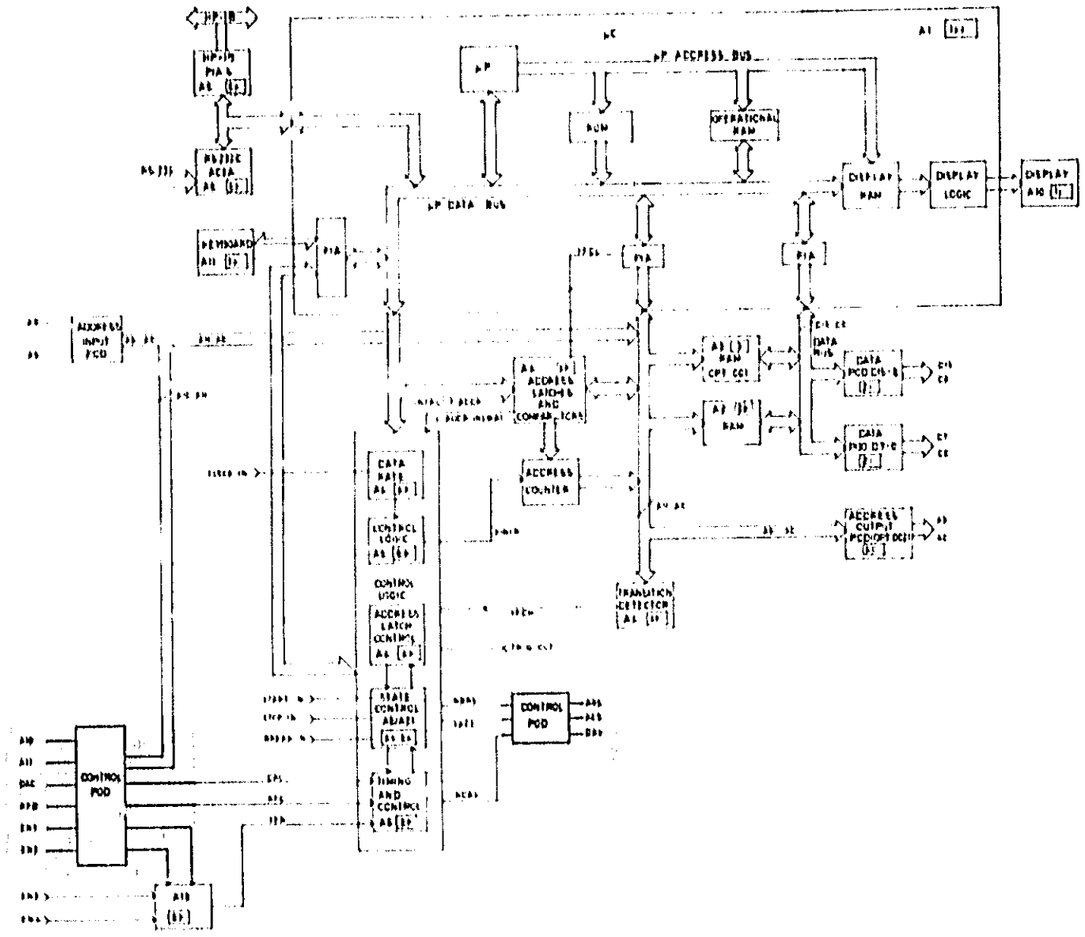
BD AY CONTROL POD 15454-66501A EARLIER MODELS



BD AY CONTROL POD 15454-66501B LATER MODELS



SERVICE SHEET 6c LOCALIZER



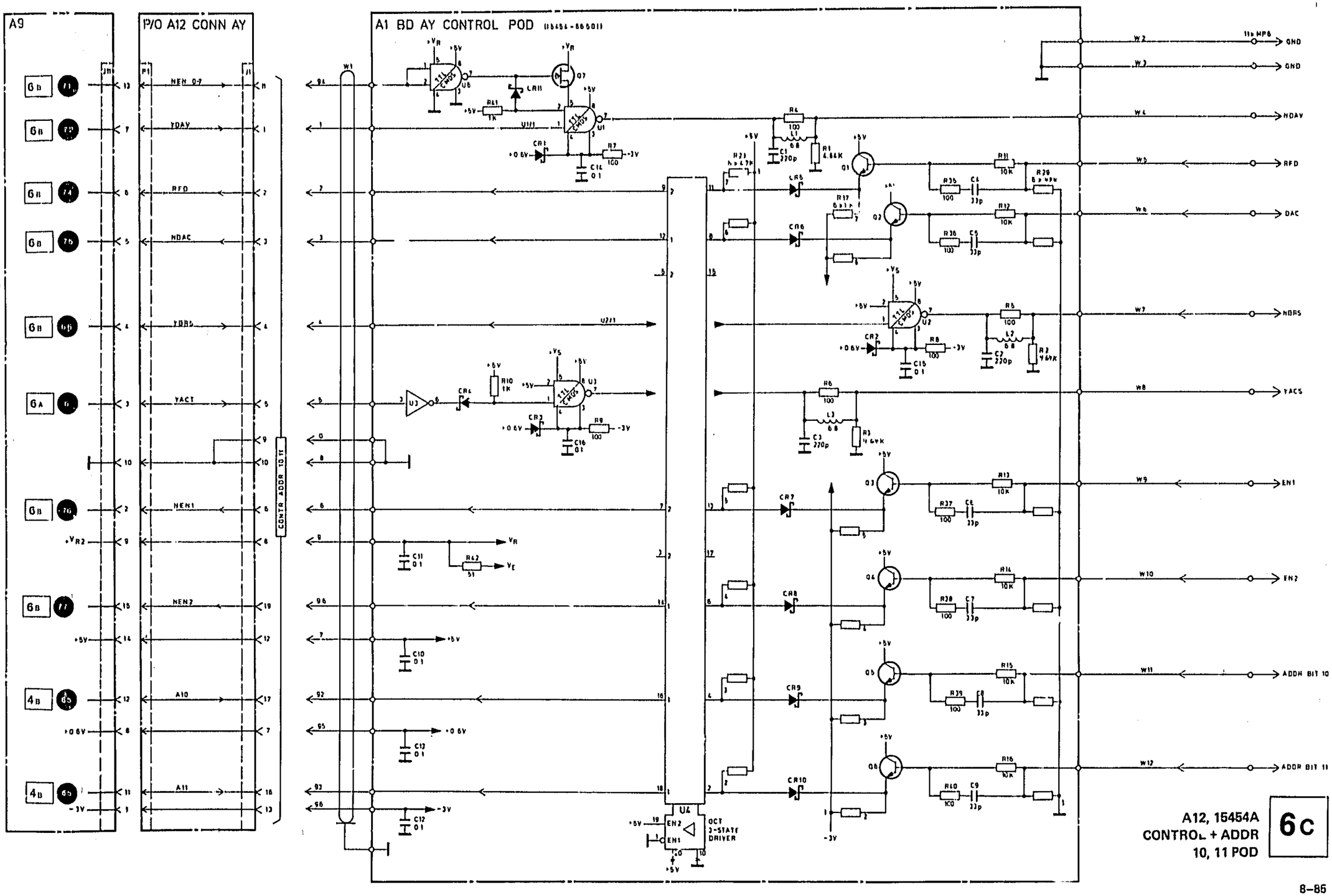
6c

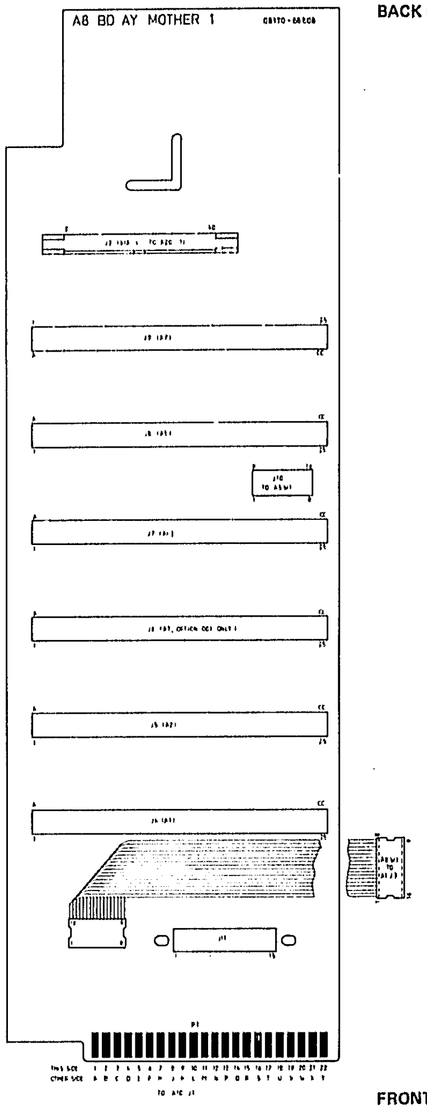
BD AY CONTROL POD

8-6C-1 REPAIR PROCEDURES

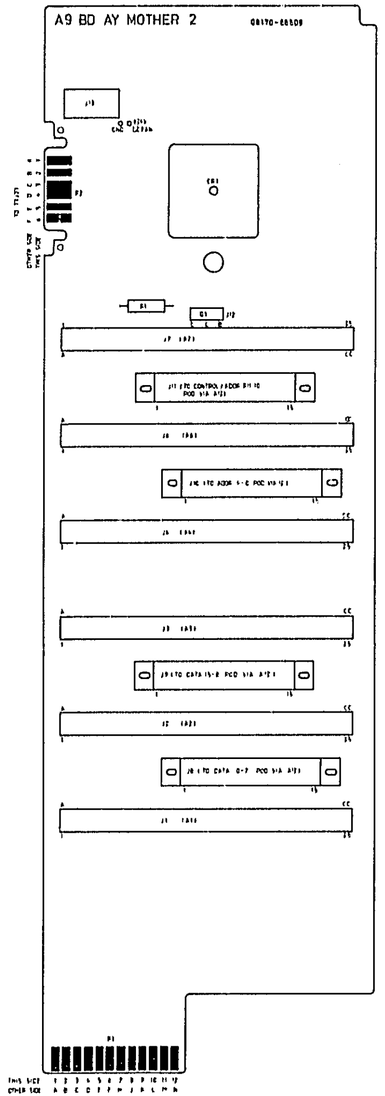
8-6C-1 Refer to 5 8-2C-1 for replacement of A12 or associated front panel connectors.

SERVICE INFORMATION CON'T


A9
P/O A12 CONN AY
A1 BD AY CONTROL POD 08454-66501
NEN 0-7
YDAV
RFD
NDAC
YDAS
YACT
HEN1
NEN2
A10
A11
CONTR ADDR 10 11
GND
GND
NDAV
RFD
DAC
NDAS
YACS
EN1
EN2
ADDR BIT 10
ADDR BIT 11
OCT 3-STATE DRIVER
A12, 15454A CONTROL + ADDR 10, 11 POD
6C



BACK OF INSTRUMENT

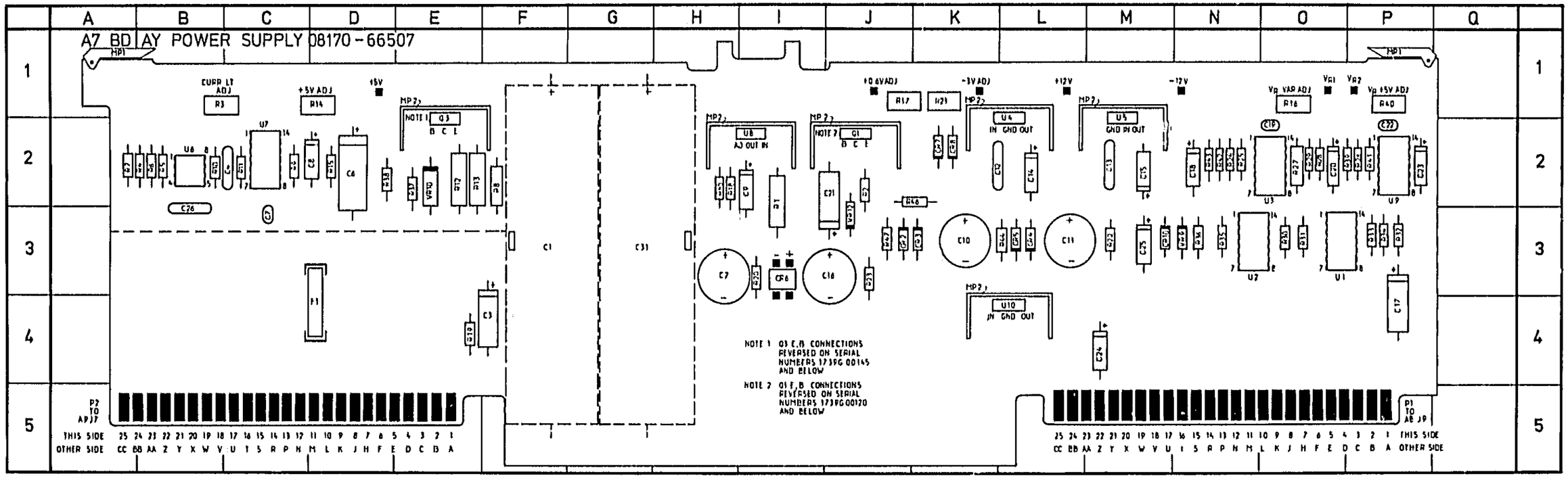


FRONT OF INSTRUMENT

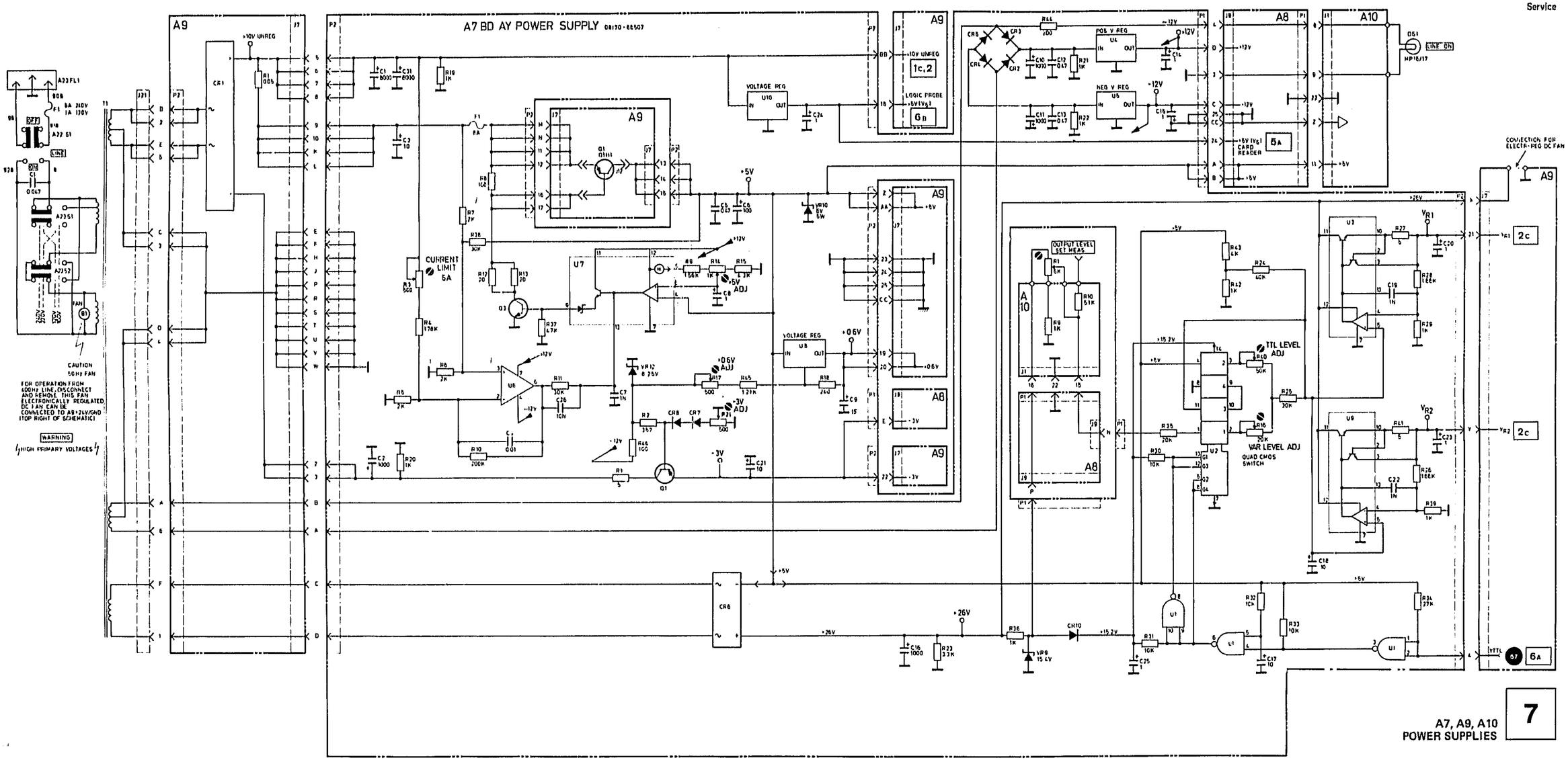
7-1

A8 BD AY MOTHER 1

A9 BD AY MOTHER 2



REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC
C1	F-3	C20	O-2	MP2	E-2	R16	O-1	R33	P-2	U4	L-1
C2	H-3	C21	J-2	Q1	J-2	R17	J-1	R34	P-2	U5	M-1
C3	F-4	C22	P-2	Q3	E-2	R18	H-2	R35	N-3	U6	B-2
C4	C-2	C23	P-2	R1	I-2	R19	E-4	R36	N-3	U7	C-2
C6	D-2	C25	M-3	R2	J-2	R20	I-3	R37	E-2	U8	I-2
C7	C-3	C26	B-3	R3	B-1	R21	J-3	R38	D-2	U9	P2
C8	D-2	C31	G-3	R4	B-2	R22	M-3	R39	P-2	U10	L4
C9	I-2	CR2	J-3	R5	B-2	R23	J-3	R40	P-1	VR9	N-3
C10	K-3	CR3	K-3	R6	B-2	R24	N-2	R41	P-2	VR10	E-2
C11	L-3	CR4	L-3	R7	A-2	R25	N-2	R42	N-2	VR12	J-2
C12	K-2	CR5	L-3	R8	F-2	R26	P-2	R43	N-2		
C13	M-2	CR6	I-3	R9	C-2	R6	O-1	R44	L-3		
C14	L-2	CR7	K-2	R10	B-2	R27	O-2	R45	H-2		
C15	M-2	CR8	K-2	R11	C-2	R28	O-2	R46	K-2		
C16	J-3	CR10	M-3	R12	E-2	R29	O-2	R47	K-1		
C17	P-4	C24	N-4	R13	E-2	R30	O-3	U1	O-3		
C18	N-2	F1	D-4	R14	D-1	R31	O-3	U2	N-3		
C19	O-2	MP1	A-1	R15	D-2	R32	P-2	U3	O-2		


A7 BD AY POWER SUPPLY 08170-66507
A9
A8
A10
CURRENT LIMIT 5A
+5V ADJ
-3V ADJ
+06V ADJ
VOLTAGE REG
POS V REG
NEG V REG
OUTPUT LEVEL SET MEAS
TTL LEVEL ADJ
VAR LEVEL ADJ
QUAD CMOS SWITCH
CONNECTION FOR ELECTA-REG DC FAN
CAUTION 50Hz FAN
FOR OPERATION FROM 400Hz LINE, DISCONNECT AND REMOVE THIS FAN. ELECTRONICALLY REGULATED DC FAN CAN BE CONNECTED TO A8 +12V/GND (TOP RIGHT OF SCHEMATIC)
WARNING
HIGH PRIMARY VOLTAGES
A7, A9, A10
POWER SUPPLIES
7

MANUAL CHANGES

HEWLETT hp PACKARD

MANUAL CHANGES

Manual for Model Number	8170A
Manual printed on	November 1978
Manual Part Number	08170-90001

Make all ERRATA corrections.

Check the following table for your instrument serial prefix/serial number and make the listed changes to your manual.

▶ New item

Serial Prefix or Serial Number		Manual Changes
ERRATA		
1739G00101	and above	1
1739G00156	and above	1-2
1915G00216	and above	1-3

Serial Prefix or Serial Number	Manual Changes

MODEL R1208A

INDEX OF MANUAL CHANGES

MANUAL CHANGE	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A19	A20	A21	A22	A23	MAINFRAME	MISCELL
ERRATA	R101,102, R105-108			U36,37,41 U42,56,57	MP4	R19*,U18 U19,31	MP1,2 R46					C1,2 A9,13					P1,MP12	Fig.6- MP1 Page 3-
1	CR16						C9											
2					C18													
3	U1,2,3,4, U5,6,34,6																	

MODEL B170A

INDEX OF MANUAL CHANGES

MANUAL CHANGE	16452A FRAME	16452A A1	16453A FRAME	16453A A1	16454A FRAME	16454A A1	16455/56A FRAME	16455/56A A1			
ERRATA				A1&22,23				C22			
1		U3									

ERRATA

Figure 6-1, Page 6-4 :

MP17 located to MP16 should read MP12.

On Table 6-2, change the Table of Replaceable Parts to read :

F1	2110-0007	FUSE 1A 110V
MP17	0400-0193	should read MP12
A2C3	0180-1704	C-FXD 47UF 6V
A2C4	0180-0228	C-FXD 22UF 16V
A4U36,37,41,42	1820-1049	IC-DM8097
A6MP4	4040-0763	should read A6MP3
A6R16*	0757-0433	R-FXD 3.32K 1%
A6U18	1820-1367	IC-SN74S08
A6U19	1820-1202	IC-DGTL SN74LS10
A6U31	1820-1423	IC-SN74LS123N
A7MP2	1205-0309	HEAT SINK-6030B
A19R9	0757-0280	R-FXD 1K 1% .125W F

Delete : A1R101,102,105-108
A2C4 0160-0576
A4U41,42 1820-1492
A4U56,67
A7MP1 1205-0309
A7MP2 0360-0535
A7R45
A19C1,2 0160-3874
A19R13

On Table 6-2, 15465A :

Delete : A1R22,23

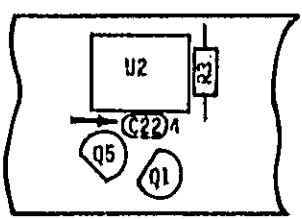
On Table 6-2, 15465/66A :

Add,: A1C22 0160-0576 C-FXD .1UF 20% 50V

Page 8-43, Service Sheet 2A to read :

A2C3 47UF
A2C4 22UF

Page 8-46, Service Sheet 2c, change the layout as shown below :

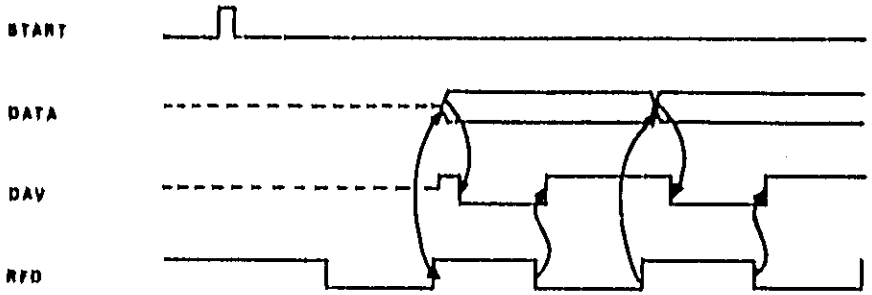


Page 8-47, Service Sheet 2c :

Add C22 connected between U2 Pin 3,4 to ground.

ERRATA (Cont.)

Page 3-6, Figure 3-9, change the diagram for 2-wire handshake as shown below :



Timing shown with
DAV = neg.true
RFD = pos.true

MANUAL CHANGE 1

On Table 6-2, change the Table of Replaceable Parts to read :

A7C9	0180-0686	C-FXD 15UF 6V 10%

Delete : A1CR15

On Table 6-2, 15452A, change the Table of Replaceable Parts to read :

A1U3	1820-1416	IC-SN74LS14N

MANUAL CHANGE 2

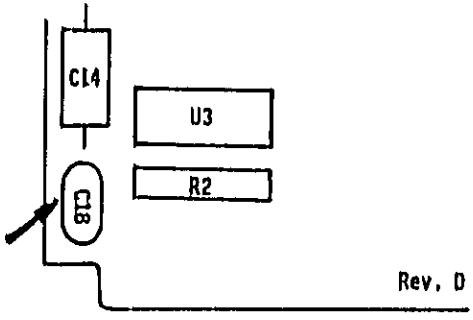
On Table 6-2, Replaceable Parts :

Add.:	A5C18	0160-3878	C-FXD .001UF 100V

On Page 8-69, Service Sheet 8A :

Add.: A5C18 connected between U1 Pin 10 and ground.

On Page 8-68, change the component layout as shown below :



MANUAL CHANGE 3

On Table 6-2, Replaceable Parts :

Add:	A1U1	1818-0914	IC ROM 2Kx8 NMOS
	A1U2	1818-0915	IC ROM 2Kx8 NMOS
	A1U3	1818-0916	IC ROM 2Kx8 NMOS
	A1U4	1818-0917	IC ROM 2Kx8 NMOS
	A1U5	1818-0918	IC ROM 2Kx8 NMOS
	A1U6	1818-0919	IC ROM 2Kx8 NMOS

Delete : A1J4,5
