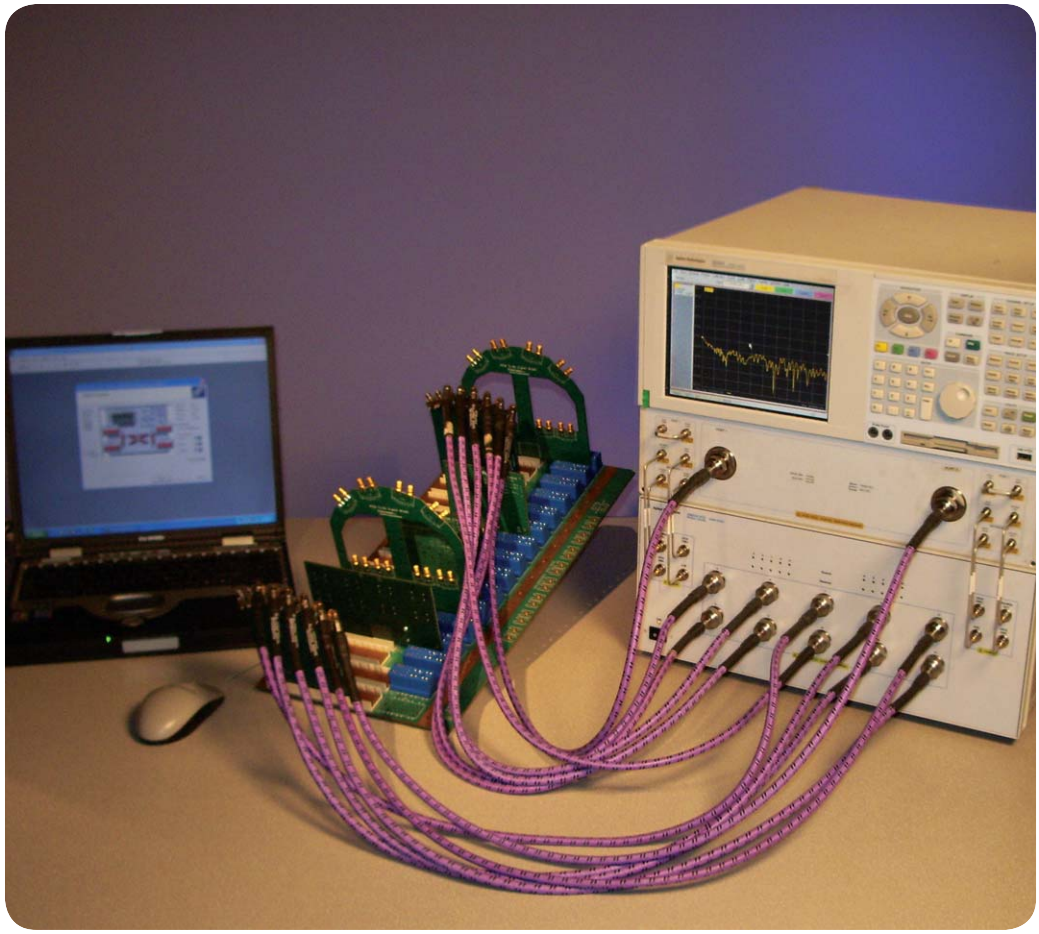
Data Mining 12-Port S-Parameters

Application Note



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Introduction

12-port differential S-parameters contain the complete behavior of up to three independent differential channels in a high-speed serial interconnect. Though there are 78 unique elements, when including magnitude and phase information, single-ended and differential forms, and the frequency and time domain descriptions, there are more than 400 different elements. This application note puts into perspective the most important terms and the valuable information that can be extracted about the interconnect performance of these measurements. In particular, we will show how the information about coupling regions can be mined from 12-port measurements.

High-Speed Serial Links and the Bandwidth Of Interconnects

High-speed serial links proliferate in data centers between servers, in backplanes between plug-in cards and between devices on a board. Each protocol, such as Infiniband, PCI-express and SATA, undergoes generational advances, with typically a factor of two increase in bit rate per channel. For example, Infiniband was introduced at 2.5 Gbps, with a second generation announced as double data rate (DDR) at 5 Gbps, and a quad data rate (QDR) at 10 Gbps.

The bandwidth of the signal components that make up the bit stream is difficult to quantify because it changes as it propagates down the channel. The signal with the highest bit transition density looks like a clock with a clock frequency of half the data rate. If the rise time of the signal were about 7% of the clock period, the bandwidth of this bit pattern would be the fifth harmonic, or 5 x 0.5 x bit rate or 2.5 x the bit rate.

While this might be the bandwidth of the signal at the transmitter, as it propagates down the interconnect, high frequencies are attenuated and the bandwidth reduces. In the typical case of a lossy line, only the first harmonic is left and the bandwidth is close to the clock frequency, or 0.5 x the bit rate at the receiver.

This is why the bandwidth of a serial data stream is typically reported as anywhere between 0.5 and 2.5 times the bit rate. This is a factor of five difference between different values. As a safe estimate, with bit rates in volume production of 5 Gbps, the signal bandwidth is in excess of 10 GHz and interconnects should be designed to support bandwidths in excess of 10 GHz.

In this Gigahertz frequency regime, interconnects contribute four important signal integrity problems, above and beyond the lower bandwidth problems such as terminations, switching noise, ground bounce and power distribution noise. These are losses, reflection noise from vias, mode conversion and crosstalk. Any one of these problems can cause failures in the channel if they are not specifically identified and designed out of the system right at the beginning.

Once built, the next step is evaluating the performance of the interconnect to a specification or compliance standard. If it does not pass, it is critical to identify the root cause of the performance limitation so it can be redesigned. Measurements based on S-Parameters can be a powerful tool to describe the measured electrical properties of the interconnect and by manipulating the information into various formats, can almost at a glance provide a first order estimate of the source of the design limitation.

4-Port S-Parameters

S-Parameters are defined in terms of how sine waves interact with a device. A sine wave with an amplitude, phase and frequency is incident on a port of the device, coming from a 50 ohm environment. The change in the amplitude and phase of the scattered wave has information about the device. Each port of the device under test is labeled with an index number and the ratio of the sine wave scattered to the sine wave incident is tracked by the index numbers.

To interpret the various S-Parameters the same way, everyone has to agree on the same port assignments. Unfortunately, there is no standardization and this is a source of confusion. When multiple channels are described, the port assignment that provides the greatest flexibility and scaling is shown in Figure 1.

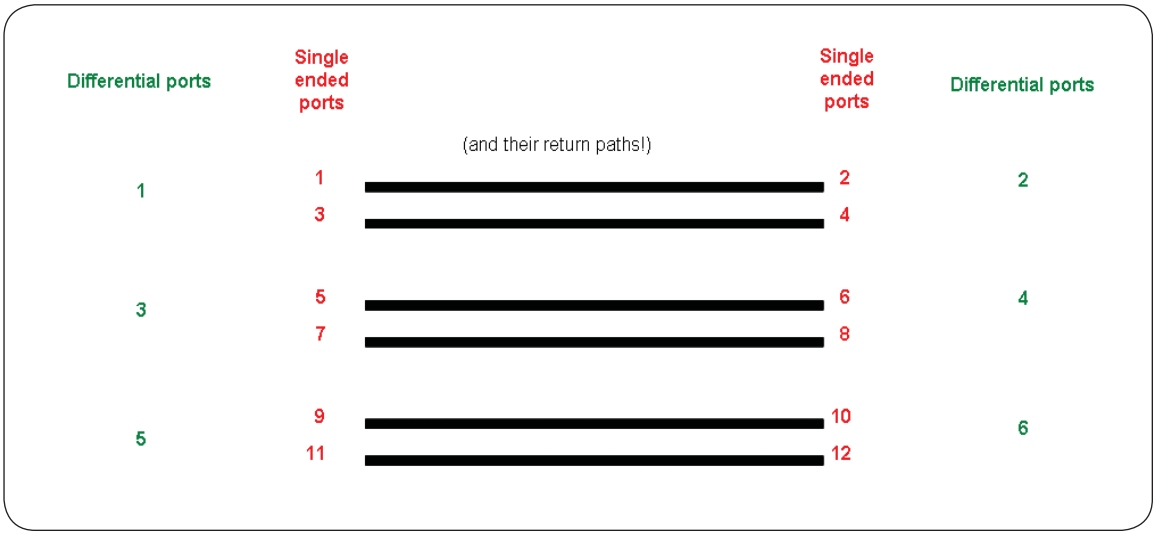

Figure 1. Port assignments for single ended and differential channels.

The first port is labeled as port 1, with its far end labeled as port 2. A second, single ended channel would have its ends labeled as port 3 and port 4. In this way, additional interconnect channels can be added while maintaining a consistent labeling scheme. An odd number port always has an even numbered port connected to it. This approach can be scaled to label an unlimited number of ports.

With this approach, the return loss of the first channel is S11 or S22 and the transmitted signal would be S21. The near end crosstalk, from a sine wave going into port 1 and coming out port 3, would be S31, while far end noise from one line to the adjacent would be labeled with S41.

The near end crosstalk between adjacent lines that makeup a parallel bus, for example, would be labeled as S31, S53, S75, etc. The near end crosstalk from the first line to all other lines in the bus would be S31, S51, S71, etc. It would be expected that the magnitudes of these terms drop off with spacing, if the coupling were due to short-range effects.

This labeling scheme can be applied to the same interconnects if adjacent traces are grouped as one differential pair. Two separate traces, with four single-ended ports, would have just two differential ports. In the same labeling scheme, an odd numbered differential port would connect to an even numbered differential port.

4-Port S-Parameters (cont'd.)

While the complete description of a collection of interconnects is contained in their single ended S-parameters, when describing the behavior of differential signals and common signals on a differential pair, it is convenient to convert the single ended S-Parameters into the balanced S-Parameters. This balanced S-Parameter format is also called the mixed mode or differential S-Parameters. These are three names used interchangeably in the industry for the same S-Parameters.

The balanced S-Parameters describe the behavior of differential and common signals on the differential pairs. In addition to the standard responses of a differential signal reflected and transmitted through the channel, or a common signal reflected or transmitted through the channel, the balanced S-Parameters can describe how a differential signal is converted into a common signal and visa versa.

When describing the interactions of differential and common sine waves with each differential port, a D or C suffix is used in addition to the port index to describe the nature of the signal going in and coming out. In the normal S-Parameter notion, the first letter or index is the coming out signal while the second letter or index is the going in signal.

In this formalism, SCD21 refers to the ratio of the common sine wave signal coming out of port 2 to the differential sine wave going into port 1. In a single differential pair channel, there is port 1 on the left and port 2 on the right. Differential and common signals can interact with this channel in four different combinations. The S-Parameters associated with each combination of differential or common signal going in or out are grouped into four quadrants. These quadrants, shown in Figure 2, are: differential in differential out (DD), common in and common out (CC) and the mode conversion terms, differential in and common out (CD) and common in and differential out (DC).

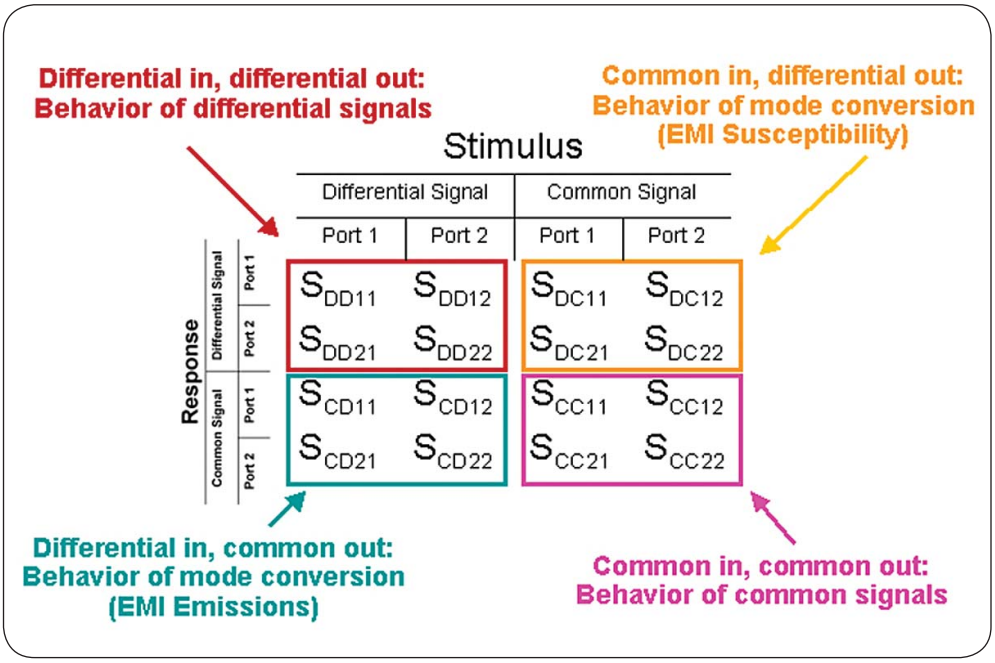

Figure 2. Four quadrants of the differential S-Parameters.

Within each quadrant are the return and insertion loss elements. This is a total of 16 different elements. All the electrical properties of a differential channel are contained in these 16 matrix elements. Also, all the electrical properties of the two interconnects as single-ended channels are contained in their 16 single-ended S-Parameter elements.

Both of these matrices are equivalent ways of describing the same interconnects. The information is the same between them, they are just in different forms. They can be converted back and forth between each form using linear combinations of one matrix element to describe the other.

Though the S-Parameter formalism is defined in terms of the frequency domain and the behavior of sine waves, the information about the frequency domain behavior of interconnects can be transformed into the time domain using Fourier transforms. When viewed in the time domain, the S-Parameters define the way time domain waveforms reflect from and transmit through the interconnect.

When the time domain waveform is a step edge wave, the response is identical to the Time Domain Reflectometer (TDR) response. The transmitted response is the Time Domain Transmitted (TDT) response of the interconnect. These two time domain responses can be either as single-ended or differential responses.

The simple single-ended S-Parameter matrix has information that can be converted into a variety of other forms. By re-defining the interconnect as a single differential pair, the single-ended matrix and be converted into the differential matrix. By converting either of the waveforms into the time domain response, they can display the TDR and TDT response of the interconnect. This transparency of the same information in each format, just displayed differently, is illustrated in Figure 3.

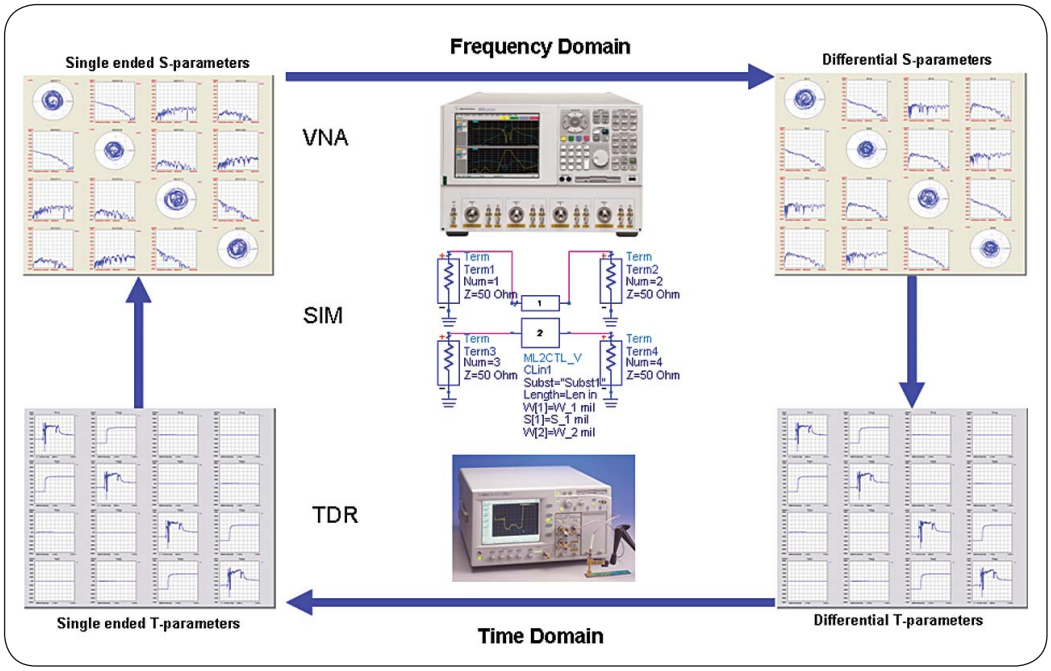

Figure 3. Originating from a time or frequency measurement or a simulation, the S-parameters can be transformed between single ended, differential and frequency, and time domains.

The information is the same in each format, just displayed differently. Each element in each format reveals a different behavior more clearly than another element. All the important electrical properties of a differential channel are contained in these 4-port single-ended or 2-port differential S-Parameter elements.

12-Port S-Parameters and Information Overload

Crosstalk between differential channels is an important interconnect property that is not included in the 2-port differential S-Parameters of a single differential channel. However, the interactions between two or more differential channels can easily be described with the same S-Parameter formalism, just expanded to incorporate the additional channels.

Each differential channel has two ports, an odd number on the left side and an even number on the right side. In the case of three differential channels, there are six differential ports.

As differential S-parameters, there are still four quadrants describing the interactions of each combination of differential and common signal. Within each quadrant, there is a 6 x 6 element matrix, corresponding to every combination of going in and coming out ports. This is a total of 36 x 4 = 144 different matrix elements in the differential S-Parameter matrix.

If the three differential channels were described by their single ended S-Parameters, there would be six different interconnects each with two, single-ended ports, or 12 ports. The S-Parameter matrix would be 12 x 12, to describe each combination of a going in port and a coming out port. This is also 144 elements. However, of these 144 elements, only (13 x 12)/2 = 78 of them are unique. Between these two matrices, there are 156 different unique terms.

Each matrix element in the single ended and differential form has two sets of data: a magnitude verses frequency and a phase verses frequency. This means that there are really 156 x 2 = 312 different sets of data in a 12-port S-Parameter matrix.

The 156 unique S-Parameter matrix elements describe the behavior of sine waves interacting with the interconnect. Each of these elements can be transformed into the time domain step response. In addition, another useful time domain response is the impulse response, also referred to as the Green's function response.

The impulse response of an interconnect describes how a unit pulse of input voltage is scattered by the interconnect over a period of time. The reflected or transmitted behavior of any arbitrary incident waveform, like a pseudo random bit sequence (PRBS), can be simulated by taking the convolution integral of the impulse response and the incident waveform.

The 156 frequency domain elements, displayed in the time domain as either a step edge response or an impulse response, result in 156 x 2 = 312 additional elements. Add to this the 156 phase terms, and there are really 624 different elements contained in the single ended S-Parameter matrix. Each element displays its information in a slightly different way.

Of these 624 elements, nine of them are especially useful in answering high-speed serial link performance questions almost by inspection. Focusing on these nine most useful elements, and not being distracted by the other 615 elements, will dramatically improve productivity.

Serial Link Performance Analysis

To measure the 12-port S-Parameters of three channels, an instrument capable of at least 2-port measurements is required. Each matrix element would be measured one at a time. While the two ports of the instrument are connected to two of the 12 ports, the other 10 ports would have to be terminated in 50 ohms. For a 12 port single ended system, a total of 72 different pairs of connections and re-connections would have to be done to cover all 78 unique elements in the single-ended S-Parameter matrix. Measuring the 12 different diagonal elements would only require six pairs of connections.

A much simpler process is possible if a 12-port instrument is used, as shown in Figure 4.

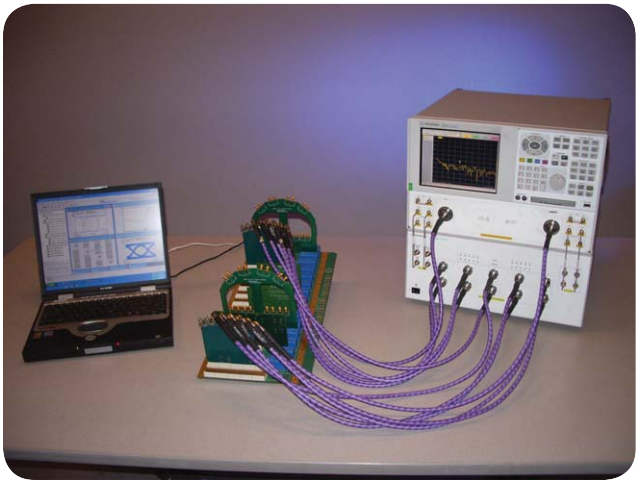

Figure 4. Example of typical 12-port VNA measurement system.

Regardless of how the initial measurements of the 12-port S-Parameters are performed, they can be transformed into any of the formats with straightforward mathematical operations.

The most important question to answer is the performance of each measured channel. For high-speed serial data channels, the shape and features of the eye diagram can directly assess performance.

A measurement of the SDD21 time domain impulse response contains information about how any arbitrary waveform will propagate through the channel. To turn this into an eye diagram, a PRBS signal at the test bit rate is synthesized and the convolution integral between the waveform and the impulse response is calculated. The resulting time domain waveform is well correlated to what appears at the receiver on an oscilloscope when a signal generator is input into the device under test. This is sliced synchronous with the clock and each consecutive pair of bits is superimposed to create an eye diagram.

Serial Link Performance Analysis (cont'd.)

Figure 5 is an example of the measured impulse response of a backplane channel and the resulting eye diagram at 2.5 Gbps and 5 Gbps.

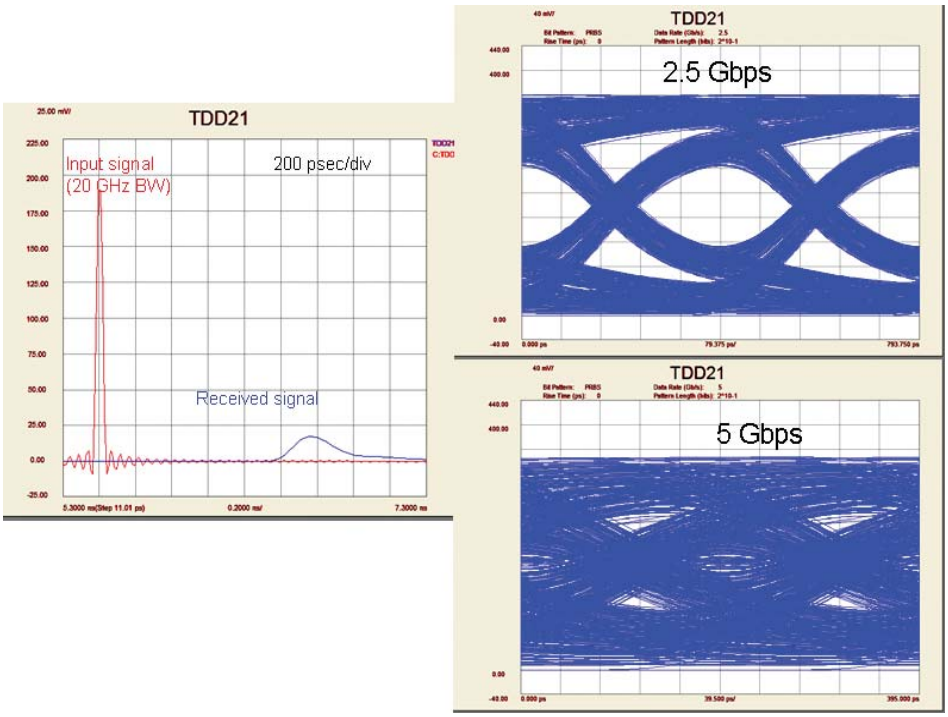

Figure 5. Impulse response of the SDD21 element and resulting simulated eye diagrams for synthesized 2.5 Gbps and 5 Gbps PRBS signals.

The impulse response provides an immediate view of the inter symbol interference (ISI) which will arise in the interconnect. With a 20 GHz measurement bandwidth, the impulse response is about 20 psec. As this impulse propagates through the interconnect, the losses and impedance discontinuities remove the higher frequency components of the signal causing it to spread out.

The time base in this example is 200 psec/div. This is one unit interval for a 5 Gbps signal. It is apparent how a single bit would spread out over at least 2 bit intervals. This is for a 20 psec wide impulse response. If the input signal were a 200 psec wide bit, the transmitted bit would have spread out even more. With this much ISI, we would expect the eye diagram at 5 Gbps to show considerable collapse and deterministic jitter. This is apparent in the synthesized eye diagrams.

While the eye diagram describes the performance of the interconnect, there is no information about why the interconnect has such poor 5 Gbps performance. The first step in optimizing performance is identifying the root cause of the limitation.

Losses

In the gigabit regime of high-speed serial links, interconnects are not transparent due to four families of problems: losses, impedance discontinuities from vias, mode conversion and channel-to-channel crosstalk. The impact each problem has on interconnect performance can be mined from specific S-Parameters.

The differential insertion loss, SDD21 in the frequency domain, has information about the nature of the losses. Figure 6 shows an example of SDD21 for three different channels measured in the same backplane.

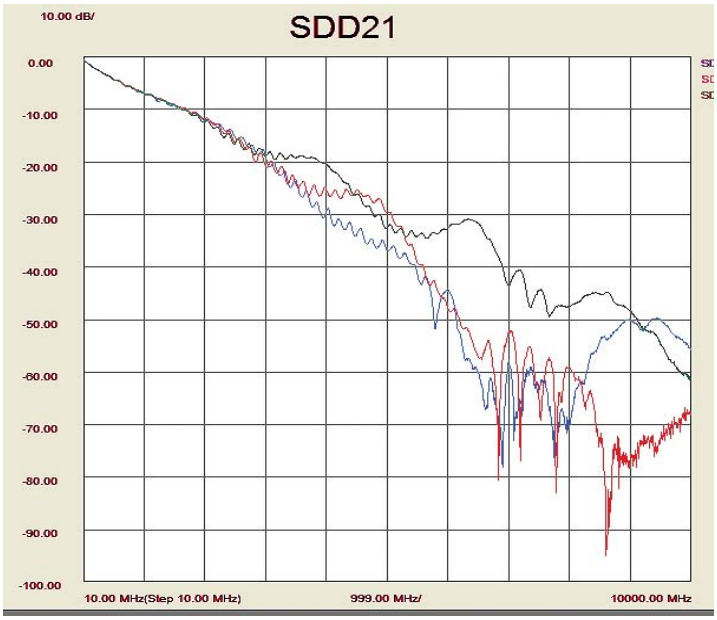

Figure 6. Measured SDD21 of three channels in the same backplane.

Below 3 GHz, the insertion loss is monotonic, suggesting the drop is dominated by conductor and dielectric losses. The slope is about 20 dB/3 GHz or 6.7 dB/GHz. In this example, the total interconnect length is about 40 inches long, so the normalized loss is about 0.17 dB/inch/GHz. This is to be compared with the rough rule of thumb for a 5 mil wide line in FR4 of about 0.15 dB/inch/GHz.

Below a bandwidth of 3 GHz, the behavior suggests losses dominate performance. This would apply to bit rates as high as 6 Gbps. This suggests that the dominant root cause of the collapse of the eye at 5 Gbps is probably due to losses.

Above 3 GHz, the variations in SDD21 suggest the presence of impedance discontinuities. Even though these three channels are adjacent in the same backplane, they have very different insertion loss above 3 GHz, suggesting specific structural differences in the channels.

Impedance Discontinuities

The details of the impedance discontinuities which might be giving rise to the insertion loss behavior above 3 GHz can be explored from the return loss measurements, displayed in the time domain for a step response. This is sometimes referred to as the SDD11 time domain or TDD11 differential response. Figure 7 shows the measured TDD11 response for these same three channels.

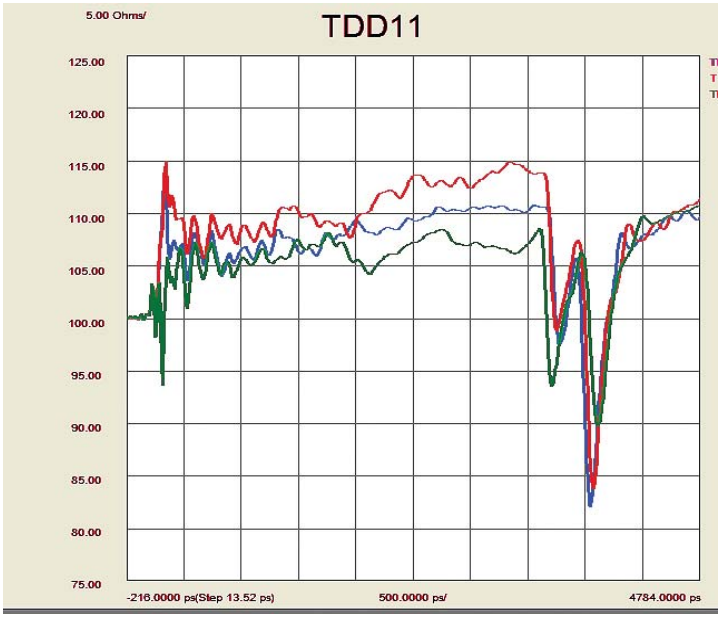

Figure 7. Measured differential TDR response of three differential channels..

The differential TDR response immediately identifies the impedance discontinuities from the 100 ohm differential source. Though there are small variations in the differential impedance of the daughter card, including the launch, the dominant discontinuities are from the vias on the daughter card side and then on the backplane side.

While much focus is placed on the connectors between the daughter card and motherboard, the connectors themselves are often very well matched to the 100 ohm environment. Rather, the biggest source of discontinuity is the vias. In this example, the variation in the magnitude of the via reflections probably are the source of the insertion loss variation.

Improving performance for bandwidths greater than 3 GHz would require improving the vias. They appear as low impedance discontinuities because of the stubs on the top and bottom of the signal transition layers. By reducing the capacitance of the vias and minimizing their length, their impedance can be greatly reduced to the point where they do not influence performance well into the 10 GHz region.

Mode Conversion

Another source of differential insertion loss is from mode conversion of some differential signal into common signal. Any asymmetry between the two lines that make up a differential pair will contribute to mode conversion. Mode conversion will cause two problems. First is the reduction in differential signal quality. This will increase the differential insertion loss. The second problem is the creation of the common signal.

Most differential receivers have a high threshold for common signal rejection so the common signal by itself may not cause a problem. However, if the common signal were to reflect from common impedance variations, and encounter the asymmetry again, it could re-convert back into a differential signal, but with an added skew. This will further distort the differential signal, increase ISI and ultimately cause a higher bit error rate.

If any of the common signal were to get out of the system, especially on twisted pairs, it can contribute to radiated emissions and possibly cause an EMI failure. It only takes about 3 micro amps of common current on an external cable to fail an FCC Class B test. Even if the common impedance were as high as 300 ohms, it only takes a common signal of about 1 mV to fail an FCC test. When the typical high-speed serial link signal is at least 100 mV, only 1% conversion is required to fail an FCC test.

Mode conversion by asymmetries in the interconnect is characterized by the SCD21 term. This is a measure of how much common signal emerges on port 2 from a differential signal incident on port 1. Figure 8 is an example of the measured SCD21 signal in the time domain, using a 400 mV incident differential signal.

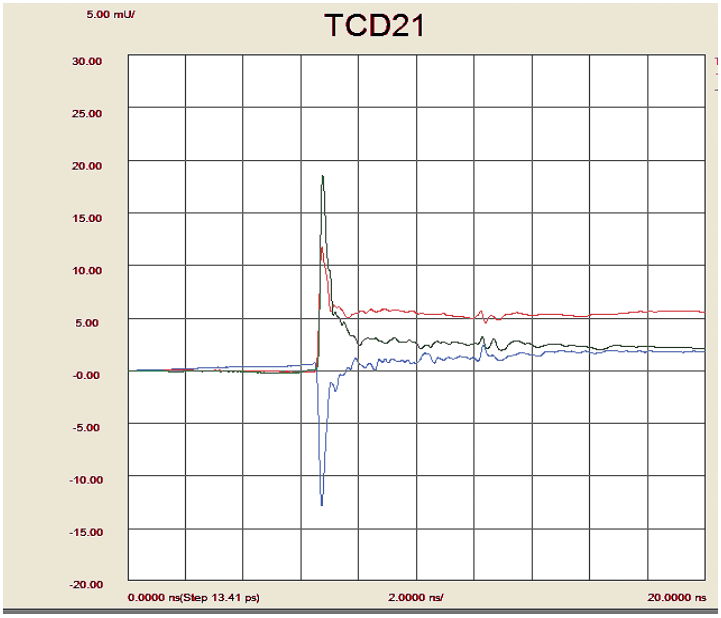

Figure 8. Measured SCD21 in the time domain for three different channels on a scale of 5 mV/div.

In this example, the three channels have about the same mode conversion, about 15 mV out of 400 mV or 4 percent. The difference in the sign between the three channels is an indication that the slow line in the pair varies between the three channels.

While this amount of common signal might cause a problem if it were to escape onto external twisted pairs, if would not cause a problem if it were confined to the backplane interconnect.

Mode Conversion (cont'd.)

If a common signal poses a problem, the first step to reduce it is to determine where the asymmetry is that causes the problem. This can be deduced by observing the SCD11 term, also in the time domain. This term is the common signal coming out of port 1 when a differential signal goes into port 1. When viewed in the time domain from a step response, the instant in time when the common signal comes back out is a measure of where it might have been produced. Figure 9 is an example of the SCD11 time domain response compared to the SDD11 response of the same backplane.

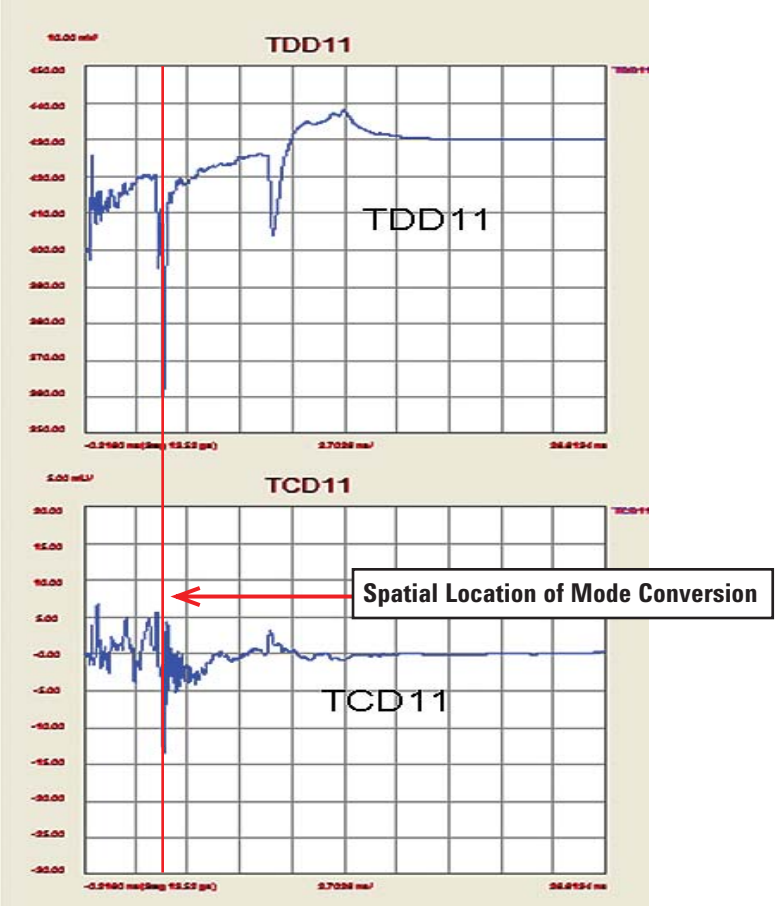

Figure 9. Measured SCD11 displayed in the time domain from a step response showing the possible spatial location of the mode conversion as the connector and via field.

In this example, most of the common signal reflected back seems to occur coincident with the reflection from the connector and the via field. A possible fix might be to select different paths in the connector, match the vias structures or better match the escapes from the via field. The root cause of mode conversion is only suggested by the SCD11 response, as not all conversion processes result in a reflection of the converted common signal back to the source.

It is not possible to further refine the location directly from the front screen. The only way to refine the source of the mode conversion would be to model various possible mechanisms and compare the simulated responses with the measured behavior, comparing the SCD11, SCD21, SDD11 and SDD21 responses.

Of course, it is almost impossible to eliminate mode conversion in any real interconnect. In addition to reducing it, all external connections must use common choke filters to attenuate the common signal before it can launch on an external cable. However the more it can be reduced at the source the further reduction there is through the filter and the more robust the product is to EMI problems.

Channel to Channel Crosstalk

The final high-speed serial link problem from the interconnect is channel-to-channel crosstalk between any two channels. The noise on one pair from a signal on the other pair will be picked up at either the near end or far end of the quiet pair. The magnitude and shape of the noise signature at the near end and far end of the quiet pair will be different. The differential near end noise between adjacent channels is described by SDD31, while the far end noise is described by SDD41. Likewise, in the channel two away from the active line, the near end noise is SDD51 and the far end noise is SDD61. An example of the measured noise is shown in Figure 10.

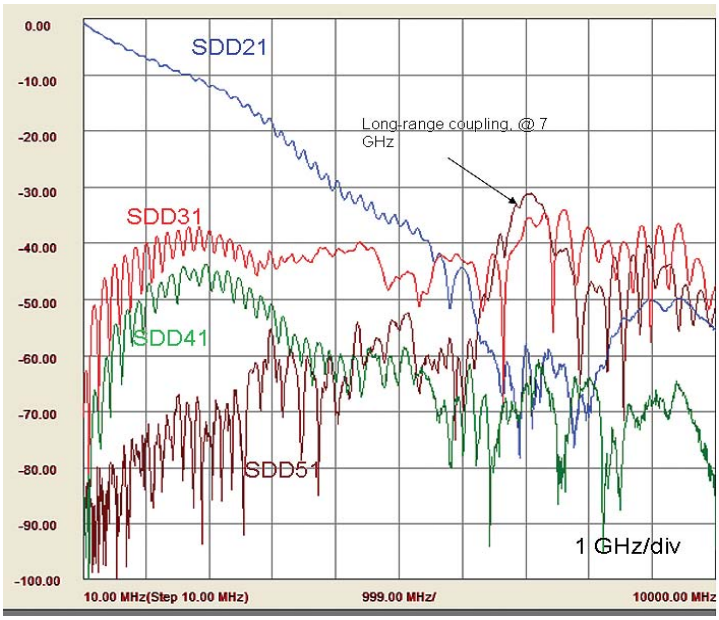

Figure 10. Measured differential NEXT and FEXT in a backplane system.

For comparison, the SDD21 response is also shown on the same scale. As expected, in this stripline based interconnect system, the far end noise, SDD41, is much less than the near end noise, SDD31. In fact, the presence of any far end noise in a stripline system is usually due not to noise generated propagating in the forward direction, but to the backward propagating noise reflected into the forward direction by impedance discontinuities. In general, the far end noise is typically about 10 dB lower than the near end noise.

When the crosstalk is dominated by the distributed coupling between the transmission lines that make up each differential pair, the near end noise to a channel two lanes distant is expected to be lower and is shown in this example to be more than 30 dB lower than to an adjacent channel. However, at about 7 GHz, the near end noise between the active channel and the adjacent and two away channel are almost the same. This is usually an indication of coupling in the connector or via field and can be a longer-range coupling.

Channel to Channel Crosstalk (cont'd.)

One way of identifying the dominant source of the coupling is by observing the SDD31 response in the time domain, as illustrated in Figure 11.

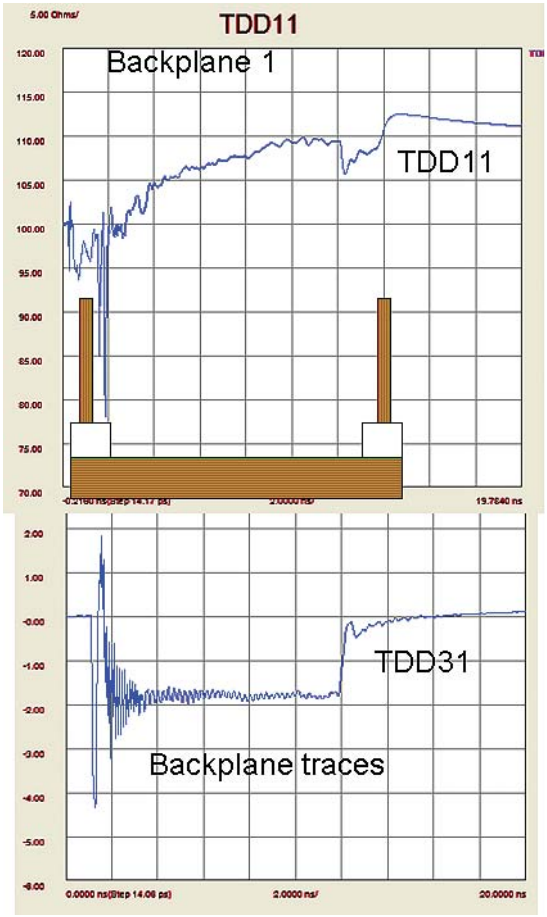

Figure 11. Measured SDD31, NEXT response, displayed in the time domain compared with the SDD11 response.

The SDD11 response, displayed in the time domain, shows the impedance profile of the backplane system. It identifies the time at which the reflection from each physical feature is received at port 1. This timing can be used to interpret the near end noise, SDD31 on the second channel.

There is a large NEXT noise pulse picked up in the quiet channel right when the incident signal reflects from the connector and via field. This is probably the origin of the 7 GHz noise.

After the connector, a large amount of near end noise can be seen as the incident signal is propagating down the backplane trace. This suggests that most of the noise, especially at lower frequency is due to pair-to-pair coupling in the backplane interconnect. To reduce this noise would require increasing the spacing between the differential pairs in the backplane.

Conclusion

All the electrical properties of three differential channels are contained in the 12-port S-Parameters matrix elements. These can be seamlessly transformed to the differential format, and between the frequency and time domains. Each different element in each different form tells a slightly different story about the behavior of the interconnects.

The first step in any interconnect characterization is to use the information as presented on the front screen to quickly and routinely obtain a first order analysis of the interconnect. This does not require any model building. Nine important elements carry more valuable information than the others, from which can be obtained the intrinsic performance limitations of the interconnect and indications of the root causes of these limitations.

It is important to note that additional information about the interconnect performance is also buried in the 12-port S-parameters. However, this information cannot be as easily mined by simply observing the measured response. Rather, to dig deeper, specific models would have to be constructed and then fitted to the measured responses. In this way, all the secrets of the interconnect can be revealed. By identifying the details of the root causes of performance limitations, the design knobs that influence performance can be adjusted to find the optimized cost-performance balance to interconnect performance.

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