



Digital Pre-distortion and Hardware Verification using SystemVue

Application Note

by Jinbiao Xu, Agilent Technologies Inc., EEs of EDA

Introduction

Power amplifier (PA) linearization using digital pre-distortion (DPD) techniques is critical for designers transitioning 3G systems to 3.9G and 4G. This application note introduces the concept behind DPD, as well as how to use the Agilent W1716 SystemVue DPD builder to do hardware verification. This software module implements memory polynomial algorithms to correct wireless components that have analog memory effects. Both simulation-based and test equipment-based extraction and verification are possible. For the purposes of this application note, SystemVue will be used with various Agilent test equipment, including the ESG/PSG/MXG family of signal sources and PSA/MXA/PXA family of analyzers.

Digital pre-distortion

Power amplifiers are essential components in the overall performance and throughput of communication systems, but they are inherently nonlinear. The nonlinearity generates spectral re-growth, which leads to adjacent channel interference and violations of the out-of-band emissions standards mandated by regulatory bodies. It also causes in-band distortion, which degrades the bit-error-rate (BER) and data throughput of the communication system.

To reduce the nonlinearity, the power amplifier can be operated at a lower power (that is, "backed off") so that it operates within the linear portion of its operating curve. However, newer transmission formats, such as wideband code division multiple access (WCDMA) and orthogonal frequency division multiplexing (OFDM, 3GPP LTE), have high peak-to-average power ratios (PAPR); that is, large fluctuations in their signal envelopes. This means that the power amplifier needs to be backed off well below its maximum saturated output power in order to handle infrequent peaks, which result in very low efficiencies (typically less than 10%). With greater than 90% of the DC power being lost and turning into heat, the amplifier performance, reliability and ongoing operating expenses (OPEX) are all degraded.

To maintain linearity and efficiency, one can apply linearization to the PA through several techniques such as feedback, feed-forward and DPD.



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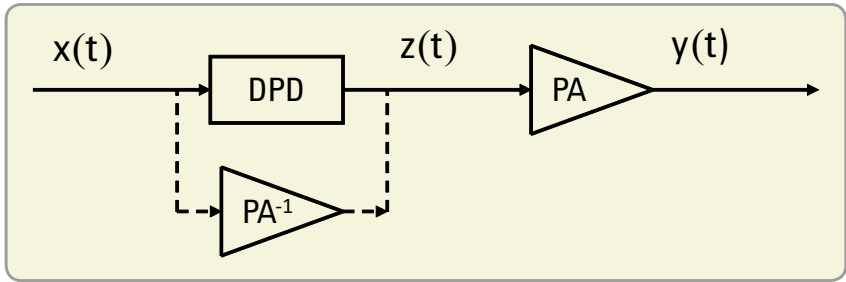


Figure 1. DPD-PA cascade

DPD is one of the most cost-effective linearization techniques. Compared with feedback and feed-forward linearization techniques, DPD has several advantages. It features an excellent linearization capability, the ability to preserve overall efficiency, and it takes full advantage of advances in digital signal processors and A/D converters. The technique adds an expanding nonlinearity in the baseband that complements the compressing characteristic of the RF power amplifier (Figure 1). Ideally, the cascade of the pre-distorter and the power amplifier becomes linear and the original input is amplified by a constant gain. With the pre-distorter, the power amplifier can be utilized up to its saturation point while still maintaining good linearity, thereby significantly increasing its efficiency. From Figure 1, the DPD can be seen as an “inverse” of the PA. The DPD algorithm needs to model the PA behavior accurately and efficiently for successful DPD deployment.

The DPD-PA cascade attempts to combine two nonlinear systems into one linear result, which allows the PA to operate closer to saturation. Figure 2 shows the amplitude response of the DPD network, the PA and the DPD-PA cascade, respectively.

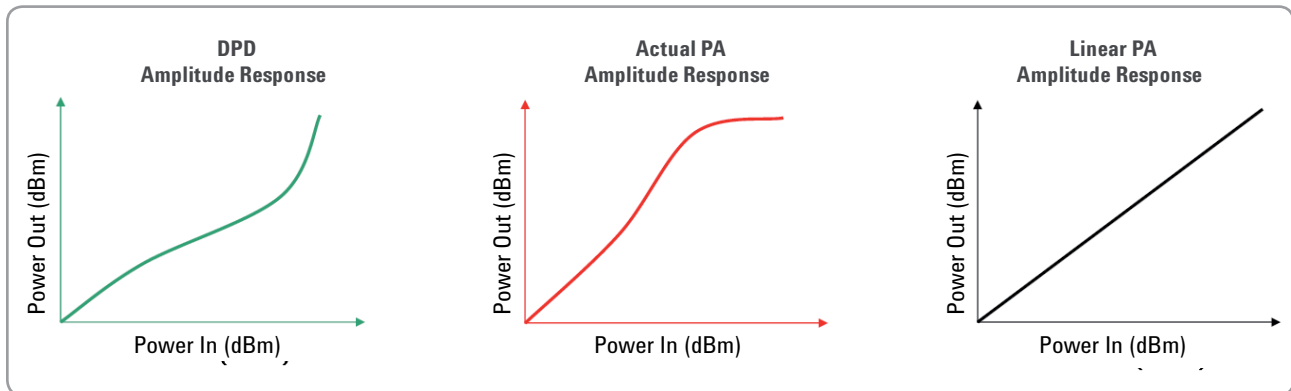


Figure 2. Amplitude response of DPD, PA and DPD-PA linearized cascade

DPD implementations can be classified into memoryless models and models with memory.

Memoryless models focus on power amplifiers where the output depends only on the instantaneous input, amplified through a nonlinear mechanism. The complex values of this nonlinear transfer function are usually characterized by the AM-AM and AM-PM responses of the power amplifier, where the output signal amplitude and phase deviation are given as functions of the amplitude of the current input value. The memoryless polynomial algorithm and the Look-Up Table (LUT) based algorithm are two key algorithms for memoryless models.

Memory effects begin to be significant as the signal bandwidth widens. This is especially true for high power amplifiers used in wireless base stations and for modulation formats with high PAPR such as WCDMA, mobile WiMAX™ and 3GPP LTE. Some of the causes of memory effects include the thermal constants of the active devices and components in the biasing network that have frequency dependent behaviors. As a result, the current output value of the power amplifier starts to depend on a history of past input values, thus existing “memory.” Memoryless linearization techniques that cannot account for these effects can only offer a limited amount of performance improvement. Therefore, practical DPD algorithms generally include memory structures.

There are two main categories of DPD algorithms that account for memory effects. The first is based on Artificial Neural Networks or Real-Valued Time Delay Neural Networks. The second DPD algorithm family is based on the Volterra series and its derivatives, with Volterra algorithms being the more general of the two approaches. However, the large number of coefficients of the Volterra series makes it unattractive for practical applications. In order to make the pre-distortion more computationally efficient, several algorithms based on Volterra have been developed, including Wiener, Hammerstein, Wiener–Hammerstein, parallel Wiener structures, and memory polynomial models. The “memory polynomial” used in the Agilent W1716 SystemVue DPD module is a special case of a generalized Hammerstein model with elements of the Wiener model added in.

After the DPD model has been chosen, the model coefficients need to be extracted. Construction of digital pre-distorters in the presence of memory effects can be difficult, and falls into two main categories:

- The first approach is to model the power amplifier and then find its inverse. However, obtaining the inverse of a nonlinear system with memory is generally a difficult task.
- Another approach is to use the indirect learning architecture to design the pre-distorter directly. The advantage of this approach is that it eliminates assumptions about the model and parameter estimation of the power amplifier.

The architecture for the digital pre-distorter uses a two-step modeling process. Step 1 is to understand the physical mechanisms behind the PA’s behavior. Step 2 is to construct a model to accurately capture both the static nonlinearity and the memory effects based on Step 1. The feedback path labeled “Pre-distorter Training” (block A) has $y(n)/G$ as its input, where G is the intended power amplifier small signal gain and $\hat{z}(n)$ is its output. The actual pre-distorter is an exact copy of the feedback path (copy of A); it has $x(n)$ as its input and $z(n)$ as its output. Ideally, we would like $y(n) = Gx(n)$, which renders $z(n) = \hat{z}(n)$ and the error term $e(n) = 0$. Given $y(n)$ and $z(n)$, this structure enables us to find the parameters of block A directly, which yields the pre-distorter. The algorithm converges when the error energy $\|e(n)\|^2$ is minimized.

In the SystemVue W1716 Digital Pre-Distortion builder, the memory polynomial algorithm is implemented. The next section describes this algorithm in more detail.

Memory Polynomial Pre-distorter

In the DPD architecture, $x(n)$ is the input signal to the pre-distortion unit, whose output $z(n)$ feeds the power amplifier to produce output $y(n)$. The most general form of nonlinearity with $Q+1$ taps of memory is described by the Volterra series, which consists of a sum of multidimensional convolutions. In the training branch, the Volterra series pre-distorter can be described by:

$$z(n) = \sum_{k=1}^K z_k(n) \quad (1)$$

where

$$z_k(n) = \sum_{m_1=0}^Q \cdots \sum_{m_k=0}^Q h_k(m_1, \dots, m_k) \prod_{l=1}^k y(n-m_l) \quad (2)$$

is the k -dimensional convolution of the input with Volterra kernel h_k . This is a generalization of a power series representation with a finite memory of length $Q+1$. The $z(n)$ also can be written as follows:

$$z(n) = h_0 + \sum_{m_1=0}^Q h_1(m_1)y(n-m_1) + \sum_{m_1=0}^Q \sum_{m_2=0}^Q h_2(m_1, m_2)y(n-m_1)y(n-m_2) + \dots \quad (3)$$

A memory polynomial pre-distorter uses the diagonal kernels of the Volterra series and can be viewed as a generalization of the Hammerstein pre-distorter. It is constructed using the indirect learning architecture, thereby eliminating the need for a model assumption and parameter estimation of the power amplifier. Compared to the Hammerstein pre-distorter, the memory polynomial pre-distorter has slightly more terms, but it is much more robust and its parameters can be easily estimated using a least-squares algorithm.

In the training branch, the memory polynomial pre-distorter can be described by:

$$z(n) = \sum_{k=1}^K \sum_{q=0}^Q a_{kq} y(n-q) |y(n-q)|^{k-1} \quad (4)$$

where $y(n)$ and $z(n)$ are the input and output of the pre-distorter in the training branch, respectively, and a_{kq} are the coefficients of the pre-distorter.

If $Q=0$, the structure in the equation degenerates to a memoryless polynomial. Since the model in equation 4 is linear with respect to its coefficients, the pre-distorter coefficients a_{kq} can be directly obtained using a least-squares algorithm by defining a new sequence:

$$u_{kq}(n) = \frac{y(n-q)}{G} \left| \frac{y(n-q)}{G} \right|^{k-1} \quad (5)$$

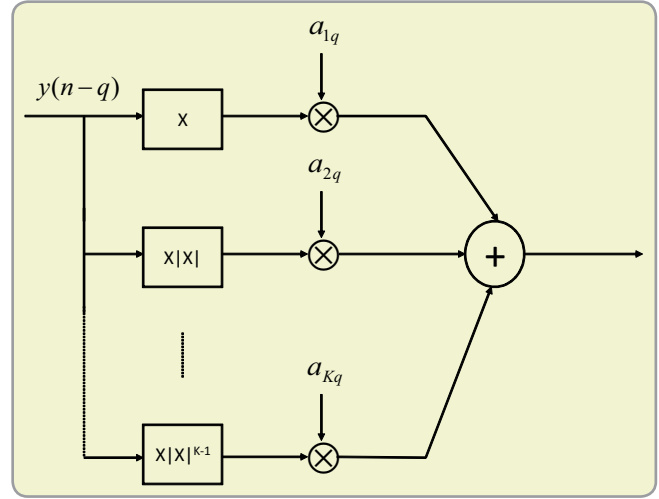


Figure 5. The architecture of the nonlinear polynomial

At convergence, we should have

$$z = Ua \quad (6)$$

where

$$\begin{aligned} z &= [z(0), z(1), \dots, z(N-1)]^T \\ U &= [u_{10}, \dots, u_{K0}, \dots, u_{1Q}, \dots, u_{KQ}], \\ u_{kq} &= [u_{kq}(0), u_{kq}(1), \dots, u_{kq}(N-1)]^T, \\ a &= [a_{10}, \dots, a_{K0}, \dots, a_{1Q}, \dots, a_{KQ}]^T. \end{aligned}$$

The least-squares solution for (6) is

$$\hat{a} = (U^H U)^{-1} U^H z \quad (7)$$

where $(U)^H$ denotes the complex conjugate transpose matrix. In the Agilent W1716 SystemVue DPD software, SVD and QR algorithms are used to decompose this matrix.

After getting memory polynomial coefficients $\hat{a} = [\hat{a}_{10}, \dots, \hat{a}_{K0}, \dots, \hat{a}_{1Q}, \dots, \hat{a}_{KQ}]^T$ and loading these coefficients into a nonlinear filter, the memory polynomial pre-distorter is able to function properly. In the Agilent W1716 SystemVue DPD, we output the DPD coefficients into two files, representing the real and imaginary parts of \hat{a} . Typical DPD coefficients are shown in Table 1 and were obtained from real measurements of a commercially available PA. The memory order is $Q=3$ and the nonlinear order is $K=9$, resulting in $K \times (Q+1)$ real and imaginary coefficients (for a total of 36).

Table 1. DPD coefficients for (memory order $Q=3$, nonlinearity order $K=9$)

Real part of DPD coefficients	Imaginary part of DPD coefficients
46015.273	8377.365
-20088.810	-2105.313
3609.907	155.622
-339.519	4.767
18.224	-1.188
-0.540	0.096
0.011	-0.000
1.80E-4	0.000
1.51E-5	1.69E-5
-4801.443	-9282.890
1681.593	4464.251
-206.216	-870.800
8.107	88.890
0.291	-5.238
-0.034	0.185
0.001	-0.004
-7.24E-6	4.56E-5
5.84E-7	2.69E-7
1456.304	-354.653
-668.183	323.138
121.485	-105.966
-11.511	17.054
0.647	-1.477
-0.025	0.067
0.001	-0.002
-1.54E-5	8.86E-6
-2.12E-7	-3.04E-7
-2121.749	-4666.219
1235.933	2611.859
-287.945	-581.543
35.090	66.952
-2.452	-4.363
0.100	0.165
-0.002	-0.004
2.59E-5	4.31E-5
1.15E-7	-2.08E-8

DPD Hardware Verification Flowchart

The Agilent W1716 SystemVue DPD builder goes beyond DPD simulation to provide a hardware verification platform for custom DPD algorithms. The following sections describe the hardware verification process.

The hardware extraction and verification process consists of five steps (Figure 6) and only takes a few minutes to perform, once the equipment has been configured:

- 1. Create DPD Stimulus** – Download the waveform (LTE, WCDMA or user defined) into the Agilent ESG/MXG signal generator.
- 2. Capture DUT Response** – Capture both the input and output of the DUT from the Agilent PSA/MXA analyzer using Agilent’s 89600 Vector Signal Analysis (VSA) software.
- 3. DUT Model Extraction** – Extract the DPD model based on the captured waveforms
- 4. Measurement Verification of DPD Response** – Apply the extracted DPD model to calculate a pre-distorted waveform and then re-download the new waveform into the Agilent signal source. The linearized PA response is captured from the Agilent signal analyzer using the 89600 VSA software.
- 5. Visualize the DPD response data** – The actual DPD performance improvements are plotted.

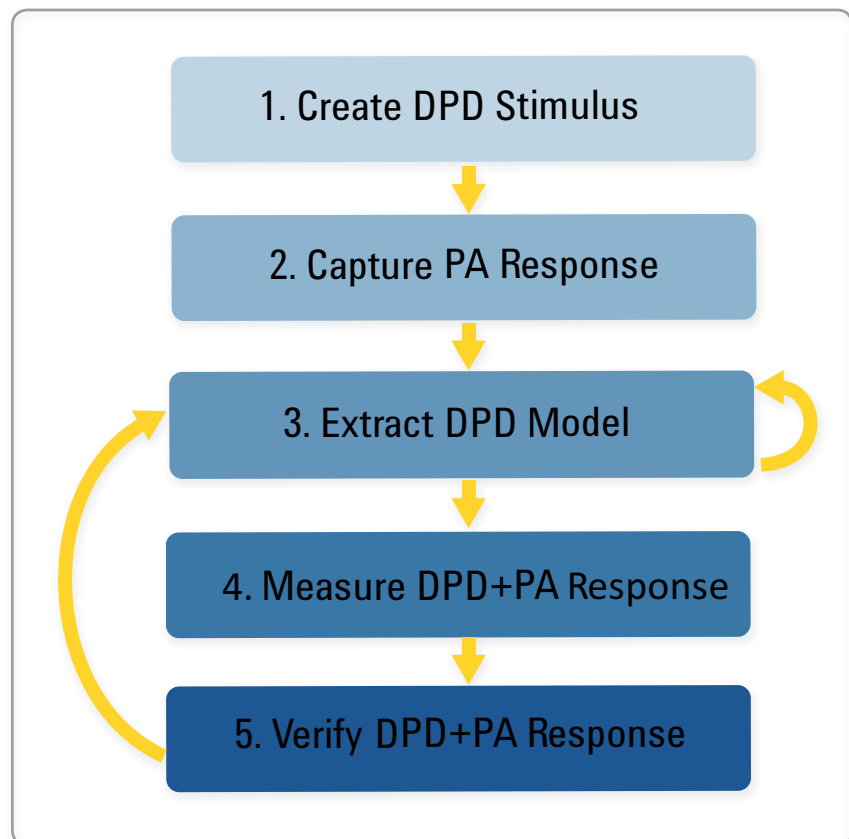


Figure 6. Flowchart of DPD hardware verification

The hardware verification platform needs an Agilent signal generator (ESG/PSG/MXG), an Agilent signal analyzer (PSA/MXA/PXA) and the power amplifier DUT. The Agilent 89600 VSA software is also needed to capture the PA input and output waveforms with DPD. Figure 7 shows the hardware verification process flow.

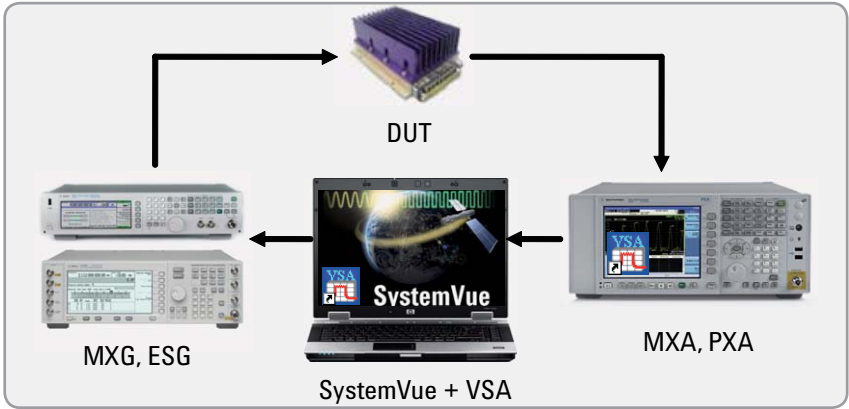


Figure 7. Hardware verification process flow

The connection with the Agilent ESG/PSG/MXG, PSA/MXA/PXA and the PA device-under-test (DUT) is shown in Figure 8. The “10 MHz OUT” of the Agilent signal generator should be connected to the “EXT REF IN” input on the signal analyzers. Also, the “EVENT1” output of the signal generator should be connected with “EXT Trigger” input 1 of the signal analyzer.

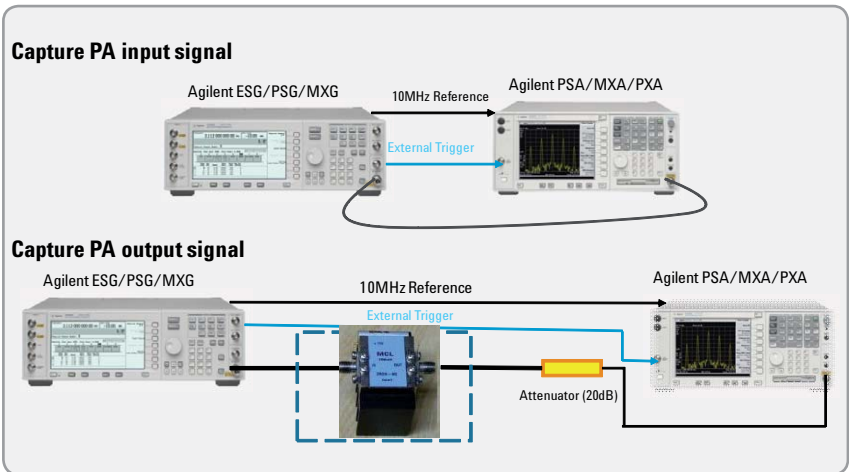


Figure 8. Connection of the Agilent MXG, Agilent PSA and the amplifier device under test

In the next section, we will elaborate on each step of the hardware verification flowchart. A 3GPP LTE downlink 10-MHz signal is used as the DPD stimulus. The DUT is an off-the-shelf PA from a major RF component manufacturer.

Step 1

Create DPD Stimulus

The first step is to download a baseband sampled I/Q waveform into the arbs of the RF signal generator. It will be used as the DPD stimulus. A choice of several waveform sources are available, including a parameterized LTE source with crest-factor reduction, a WCDMA source with up to four carriers, and a custom waveform created with the user's live SystemVue simulation blocks. The schematic of the parameterized LTE source is shown in Figure 9.

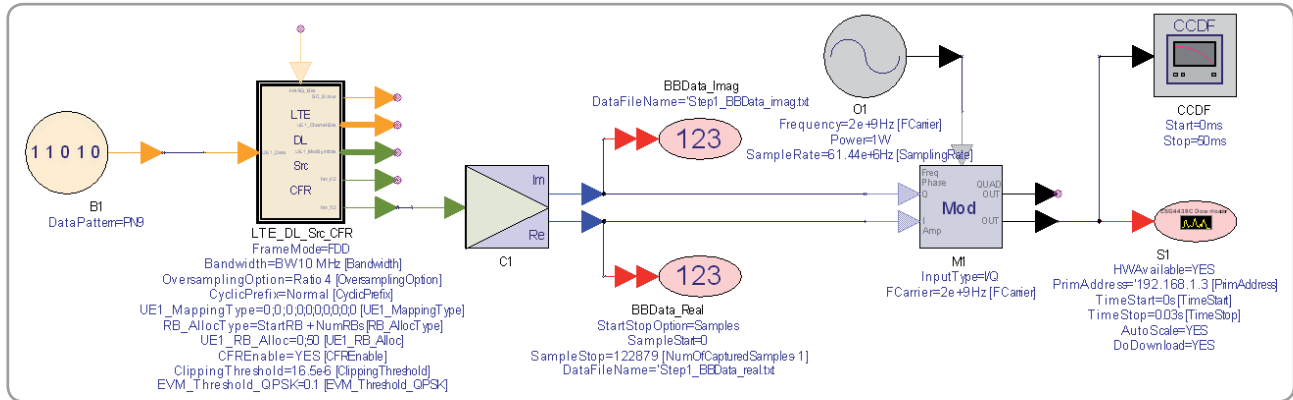


Figure 9. Schematic to create the DPD stimulus in Step 1

A tabbed graphical user interface (GUI), as shown in Figure 10, is available to help organization and configure the LTE parameters in Figure 9. LTE downlink parameters (e.g., FCarrier, Bandwidth, Cyclic Prefix, UE Resource Block allocation, and CFR threshold) can be configured in this GUI. The values of these parameters continue forward in subsequent steps of this process.

Instrument control parameters for the MXG/ESG download, such as RFPower, PrimAddress, TimeStart and TimeStop may also be set. RFPower defines the “RF output power level in dBm” of the ESG/MXG RF output waveform. Since the signal generator output is also the PA input waveform, its value should be set close to the PA saturation power for the purposes of this DPD application. PrimAddress is to set the instrument IP address (LAN) or GPIB address (GPIB). TimeStart and TimeStop determine the start and stop times of the waveform recording. After setting all of the above parameters, we can click the “Download Waveform” button in the GUI to download the waveform into the ESG/MXG. Once downloading the waveform into the ESG/MXG, we can click to see both the CCDF and PAPR of the downloaded waveform (Figure 11).

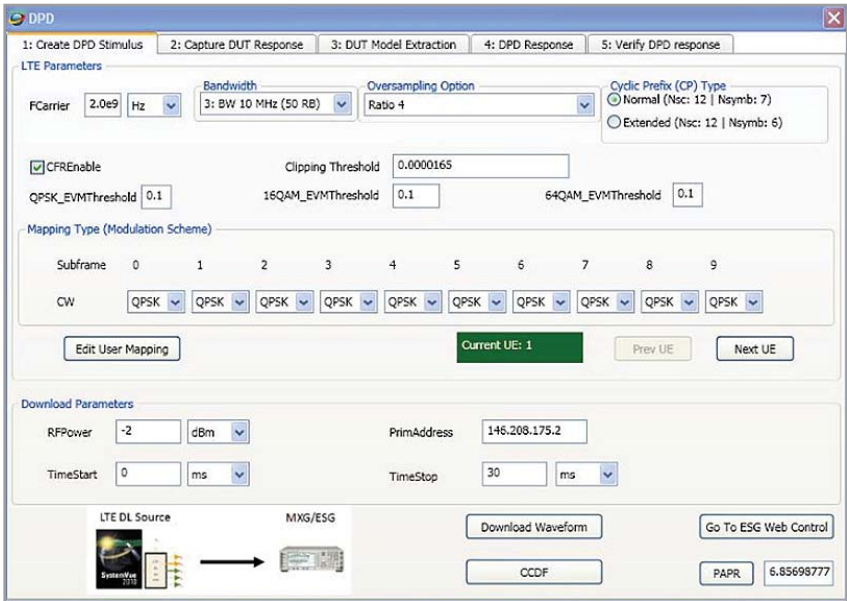


Figure 10. GUI of Step 1

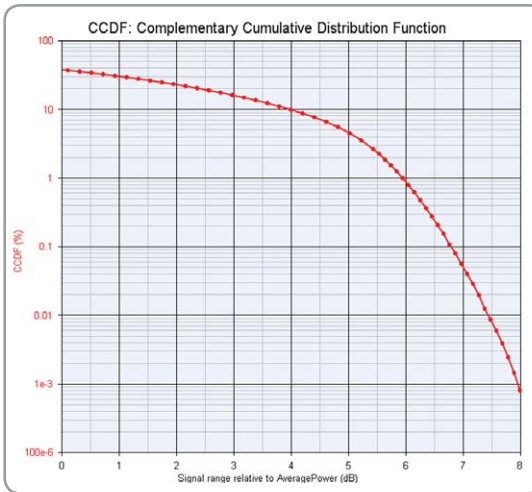


Figure 11. CCDF of LTE with CFR enabled

Two ASCII text files (Step1_BBData_real.txt and Step1_BBData_imag.txt) are generated in this and other DPD steps. They represent the IQ waveforms used for the initial signal generator training sequence. In the W1716 SystemVue DPD builder software, the IQ test vectors at each of the process steps are archived for later usage and analysis. Although the files can sometimes be large, they allow DPD simulations to be explored further offline, after the test equipment has been removed.

One practical consideration when linearizing real power amplifiers is the ability of the signal generator to drive the DUT hard enough, particularly for high crest-factor modulation formats such as LTE. A signal generator operating at its rated power (about +25 dBm for ESG/MXG) may not have the dynamic range to reproduce the intended peak values that are 7-10 dB above the average power levels. Therefore, crest factor reduction (CFR) should be enabled in SystemVue prior to download. This pre-conditions the test waveform to have a lower PAPR, with minimal impact to in-band EVM. In practice, CFR turns out to be essential to successful DPD of LTE signals, which is also true of the broader class of OFDM waveforms.

Step 2

Capture DUT Response

After downloading the waveform into the ESG/MXG in Step 1, we capture the PA input and output waveforms using the 89600 VSA software. The parameter `NumOfCapturedSamples` defines the length of the captured waveform. The Setup File sets the 89600 VSA .set file to control the 89600 VSA software's capture of waveforms from the PXA/PSA. VSATrace controls which channel will capture waveforms in the 89600 VSA software.

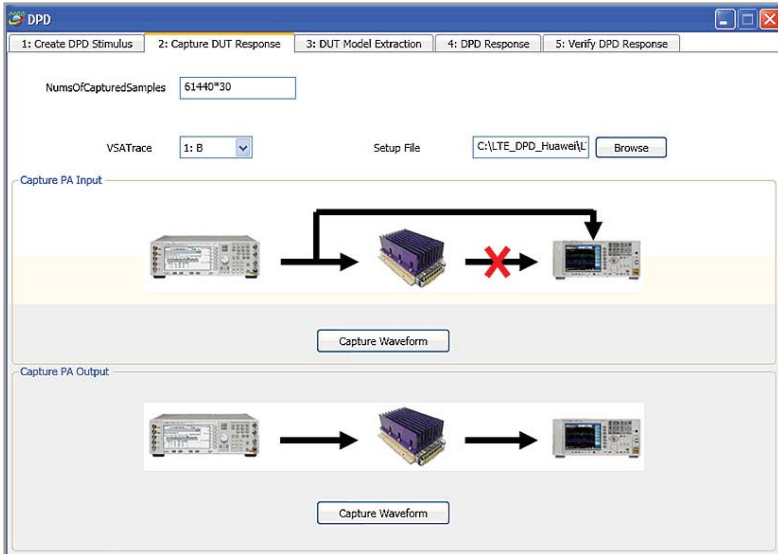


Figure 12. GUI of Step 2

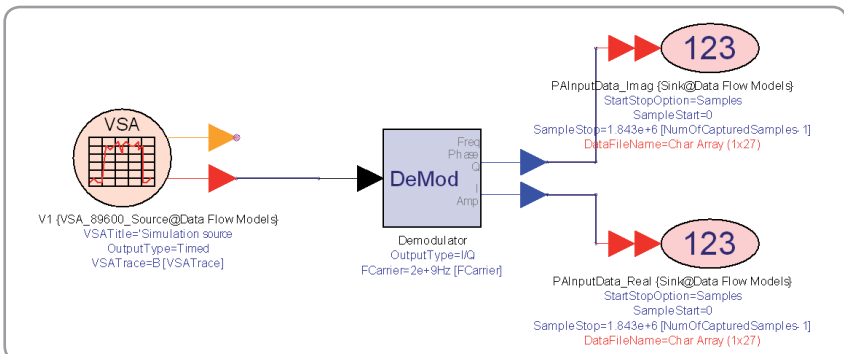


Figure 13. Schematic to capture waveform

First, connect the ESG directly with the PSA/PXA and click the “Capture Waveform” button in the “Capture PA Input” panel in the GUI (Figure 12). The captured signal is the input of the PA DUT (Figure 13).

Next, connect the ESG with the DUT and connect the DUT with the PSA. Click the “Capture Waveform” button in the “Capture PA Output” panel in the GUI. The captured signal is the output of the PA DUT.

These I/Q files are stored for further usage. Four text files (`Step2_PAInputdata_real.txt`, `Step2_PAInputdata_imag.txt`, `Step2_PAOutputdata_real.txt`, and `Step2_PAOutputdata_imag.txt`) are generated in this step. `Step2_PAInputdata_real.txt` and `Step2_PAInputdata_imag.txt` are the saved real and imaginary of the captured PA input waveform, respectively. `Step2_PAOutputdata_real.txt` and `Step2_PAOutputdata_imag.txt` are the saved real and imaginary of the captured PA input waveform, respectively.

Step 3

DUT Model Extraction

Step 3 is the most critical step and involves extracting DPD coefficients by using the PA input and output waveforms. Before clicking the DPD Model Extraction panel, we need to set the following parameters: NumOfInputSamples, ModelType, MemoryOrder, NonlinearOrder, and Model Identification Algorithm (Figure 14). The parameter ModelType can only be set to Memory Polynomial because only the Memory Polynomial algorithm is currently provided. The Model Identification Algorithm can be set to LSE using QR or LSE using SVD. The parameter NumOfInputSamples defines the length of the input waveform to be used to extract DPD coefficients. Both of the parameters MemoryOrder and NonlinearOrder define the memory depth and nonlinear order, respectively, in the memory polynomial algorithm (Figure 15).

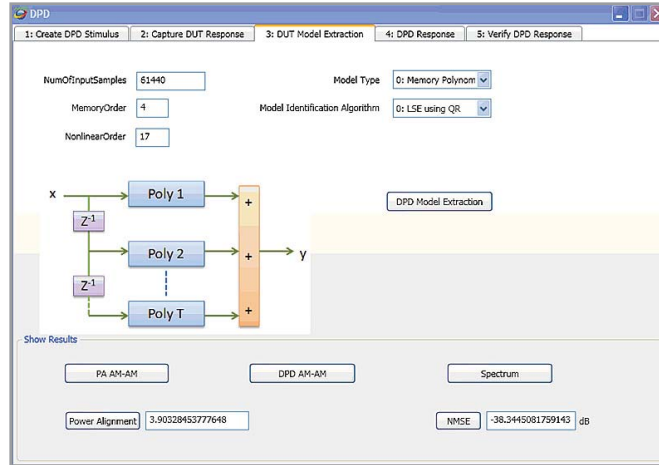


Figure 14. GUI of Step 3

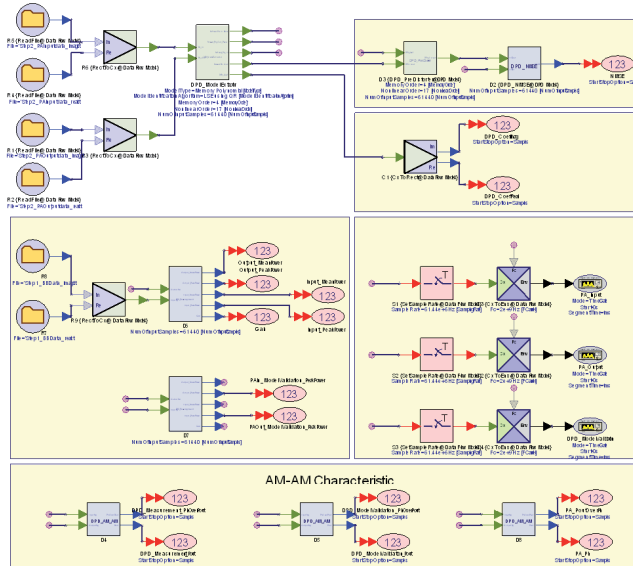


Figure 15. Schematic of Step 3

Following completion of the DPD Model Extraction, we can see the verification results of DPD. By clicking the PA AM-AM panel, the PA AM-AM characteristic becomes apparent (Figure 16). The DPD AM-AM shows the DPD AM-AM characteristic in terms of two curves in Figure 17. (Figure 17). The red curve is the AM-AM of the samples that are used to do model extraction. The blue curve is the AM-AM of the samples that are not used for model extraction. The spectrum shows the PA input, PA output and inverse PA spectrum, respectively (Figure 18).

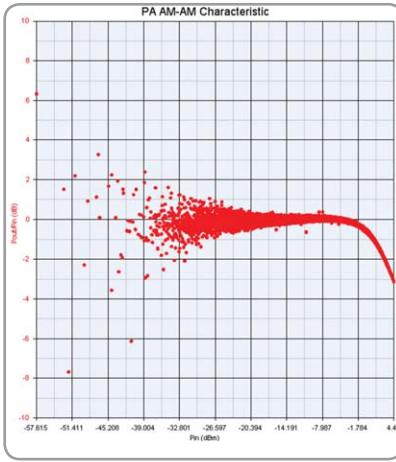


Figure 16. PA AM-AM

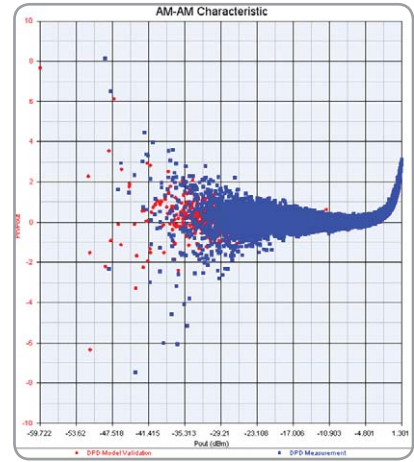


Figure 17. DPD AM-AM

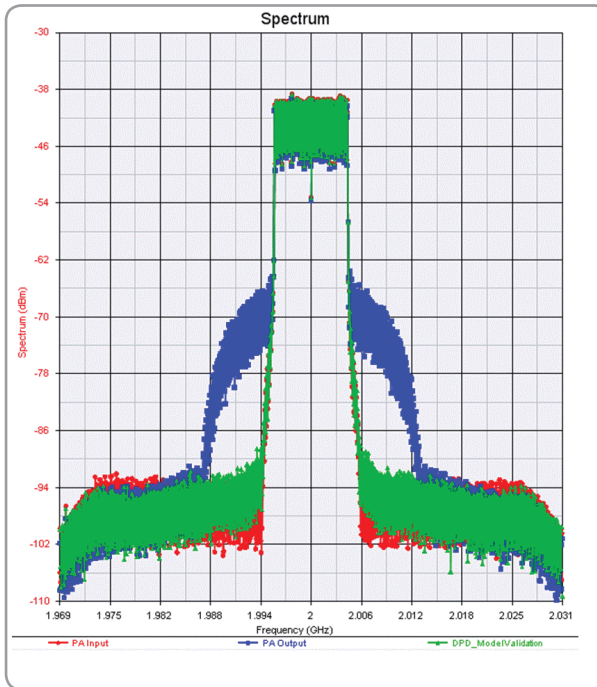


Figure 18. Spectrums of PA input, PA output and inverse PA

The power alignment value (for example, 3.90) can be obtained by clicking the Power Alignment panel. This value calculates back-off power and is used in Step 4. The NMSE value (for example, -38.34 dB) can also be obtained by clicking the NMSE panel.

After completing Step 3, we need to decide whether or not to go Step 4. To do this, it is necessary to first look at the NMSE value and then the DPD spectrum. If NMSE is small (≤ 35 dB) and DPD spectrum is reasonable, we can continue onto the next Step. Otherwise, we need to go back Step 1 to adjust RFPower and then proceed to Steps 2 and 3.

Two text files for DPD coefficients (Step3_DPD_Coefficients_Real.txt and Step3_DPD_Coefficients_Imag.txt) are generated in this step. Both files are saved real and imaginary of the DPD coefficients, respectively. The length of both text files is determined by MemoryOrder and NonlinearOrder ($\text{length} = (\text{MemoryOrder} + 1) \times \text{NonlinearOrder}$).

Step 4

DPD Response

This fourth step is to apply the DPD model extracted in Step 3. The generated LTE downlink signal is first pre-distorted by the extracted model, and then downloaded into the ESG. The RF power should also be set carefully to make sure the power of the baseband signal and the input signal of the extracted DPD model are in the same level. This step consists of three substeps.

The first substep is to “Do power Alignment” (Figure 19). The schematic for this substep is shown in Figure 20. Before “Do power Alignment,” we need to get the power alignment value. If we click the Default panel, the value (for example, 3.90) in Step 3 is displayed. The user also can change values if he considers the default unreasonable. Following “Do power Alignment,” we can see the DPD AM-AM characteristic after power alignment. Compared with Figure 21 and Figure 17, the maximum of Pin is the same in both figures.

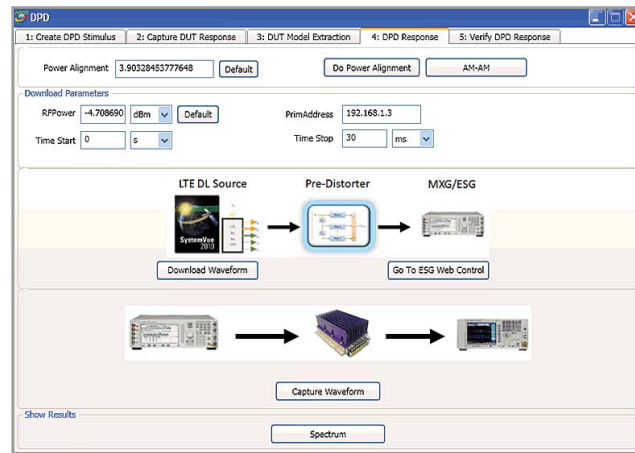


Figure 19. GUI of Step 4

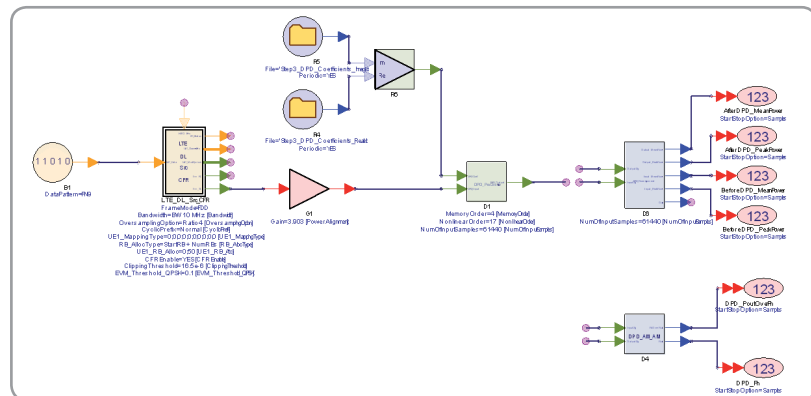


Figure 20. Schematic of power alignment

The second substep is to pass the waveform through the digital pre-distorter in simulation, using the coefficients in Step 3, and then download this DPD waveform into the Agilent ESG/MXG. The signal generator download parameters (RFPower, PrimAddress, TimeStart and TimeStop) also can be configured. RFPower can be calculated automatically. In this example, the value is -6.09 after clicking Default panel. The value of RFPower should add 1.0-1.3 dB gain to account for cable loss in the real PA measurement. Since this cable loss is not present in the original “thru” measurement of Step 1, it is important to account for it here in order to match the actual power levels incident to the DUT. The value is -4.79 after adding 1.3 dB of cable loss. For better DPD results, be certain to set the ESG/MXG RF output waveform close to the PA saturation power level (input referred).

PrimAddress sets the instrument IP address (LAN) or GPIB address (GPIB). TimeStart and TimeStop determine time start/stop waveform recording. After setting these parameters, we can click the “Download Waveform” button in the GUI to download the waveform into the ESG/MXG (Figure 22). The spectrums before DPD and after DPD are shown in Figure 23.

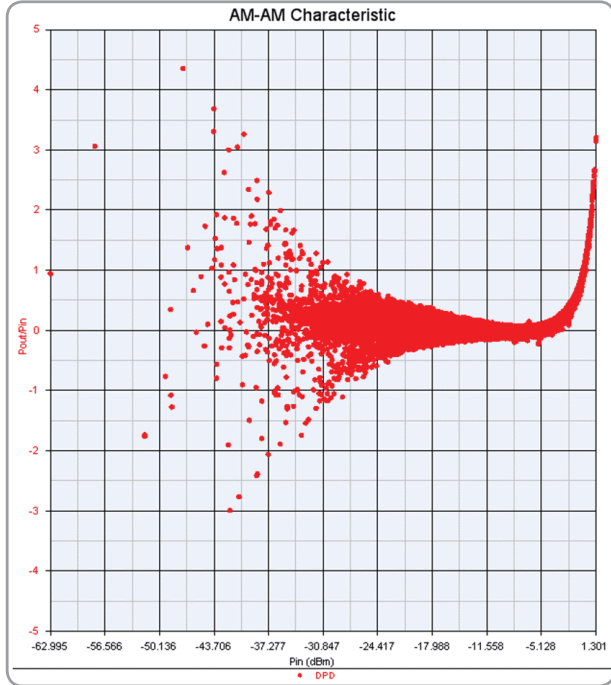


Figure 21. DPD AM-AM after power alignment

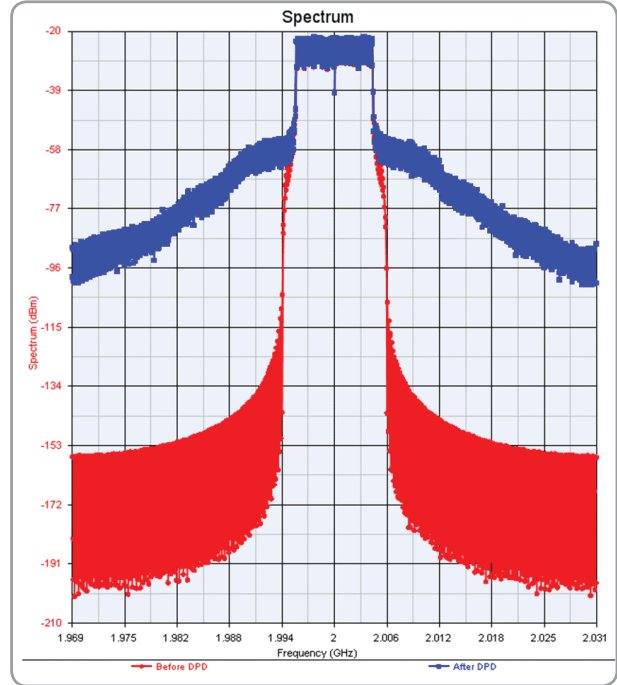


Figure 23. Spectrums before and after DPD

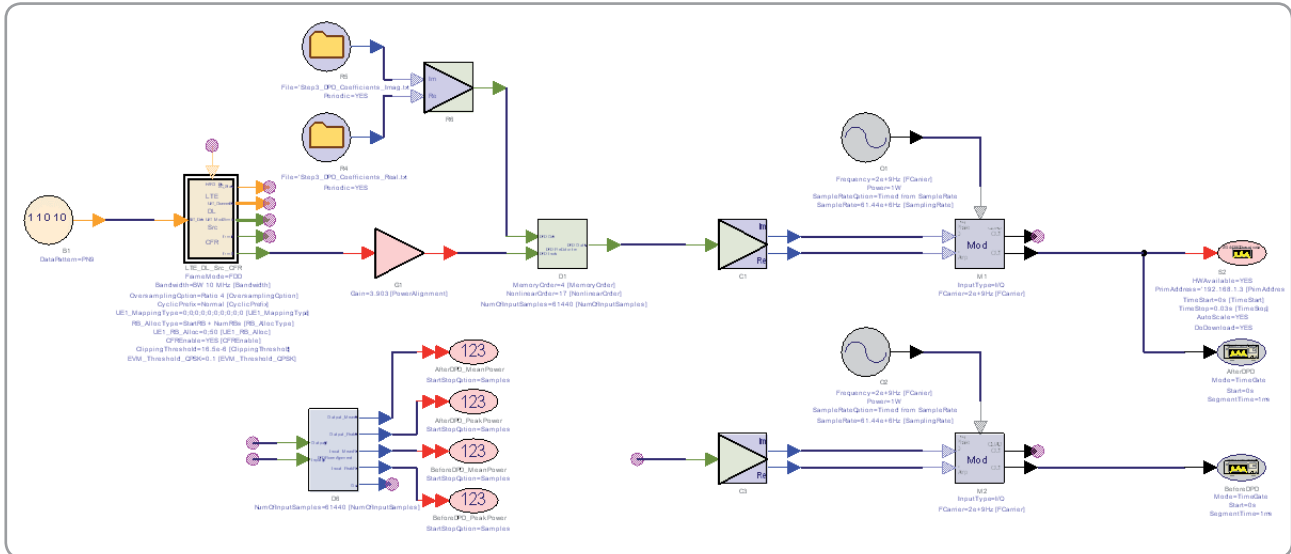


Figure 22. Download waveform with DPD into ESG/MXG

The third substep is to capture DPD waveform from the Agilent PSA/PXA using Agilent's 89600 VSA software. Its parameters (e.g., capture waveform and .set file) were set in Step 2. Please note that the power search must be performed in MXG/ESG because the digital pre-distorted waveform is not the standard waveform.

In the ESG/MXG signal generator, click the Amplitude panel, Power Search, Manual, and Modulated. After that, click the Amplitude panel again followed by the Do Power Search panel.

Figure 24 shows the spectrum, waveform and trace power without performing "Do Power Search." Note that the spectrum is not correct and the power of trace A is -24.241 dBm, which is also not correct because the RFPower is about -5 dBm.

Figure 25 shows the spectrum, waveform and Trace Power after doing "Do Power Search." Here the spectrum is correct and the power of trace A is -6.159 dBm, which is also correct and close to the RFPower equals about -5 dBm in the previous case.

Two text files for the DPD-PA waveform (Step4_DPD_PAOutputdata_real.txt and Step4_DPD_PAOutputdata_imag.txt) are generated in this step. Both files are saved real and imaginary of the DPD-PA waveform, respectively.

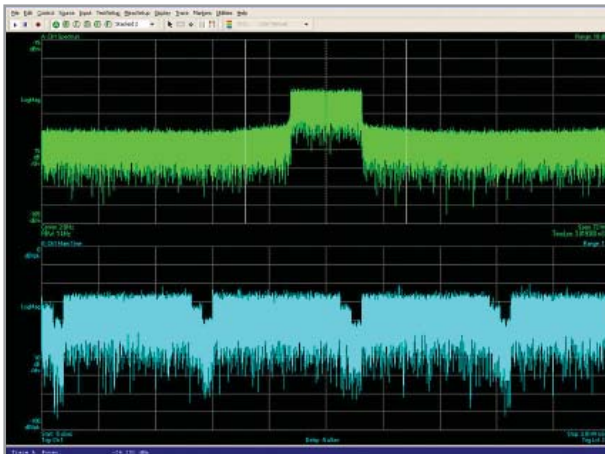


Figure 24. Spectrum and waveform of 89600 VSA without "Do Power Search"

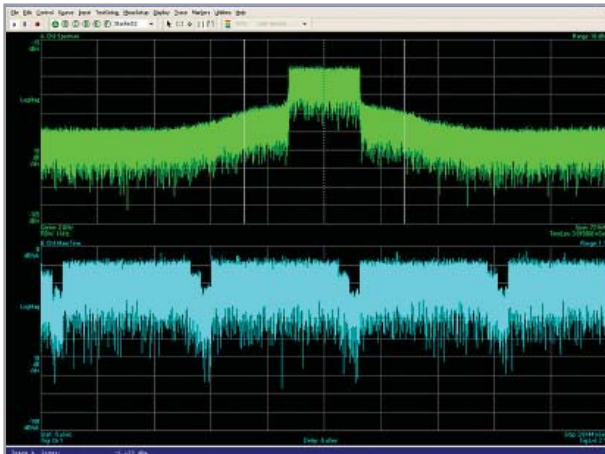


Figure 25. Spectrum and waveform of 89600 VSA after doing "Do Power Search"

Step 5

Verify DPD Response

The fifth step is to verify performance (e.g., EVM, ACLR and spectrum) after DPD, including the PA (Figures 26). In order to compare spectrums with and without DPD, the original signal should be re-downloaded into ESG/MXG after setting the same RF power as Step 4. We also can use the downloaded waveform in Step 1 and change the power in the MXG/ESG (Figure 27).

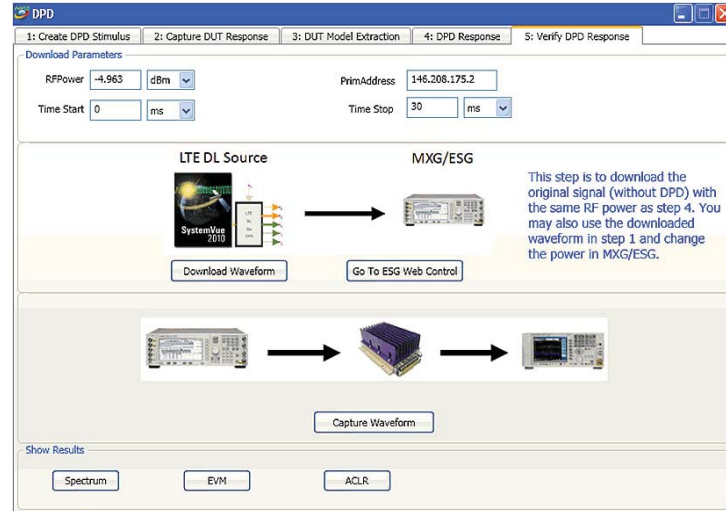


Figure 26. GUI of Step 5

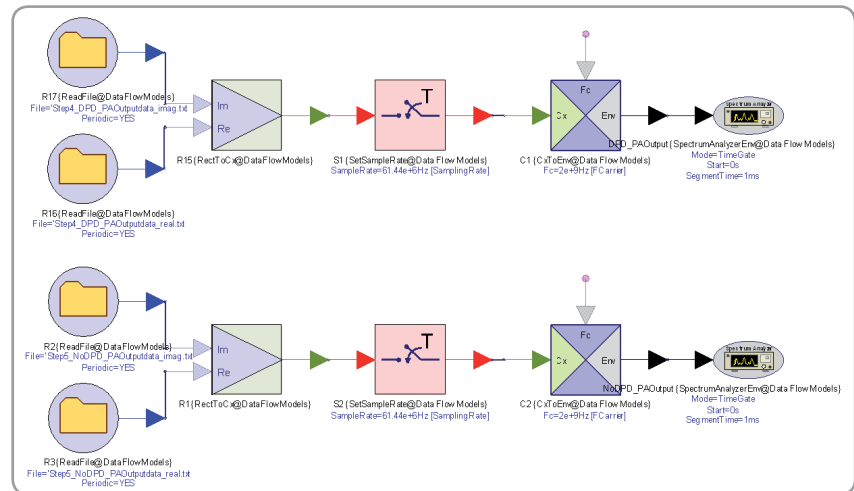


Figure 27. Schematic of spectrum

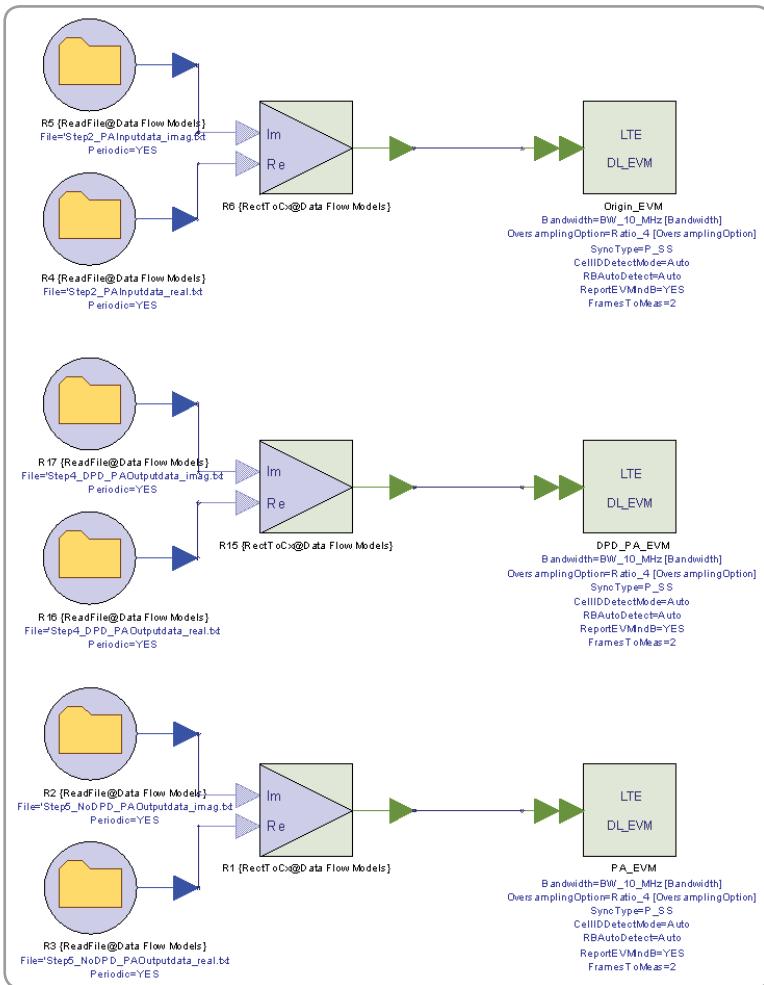


Figure 28. Schematic of EVM

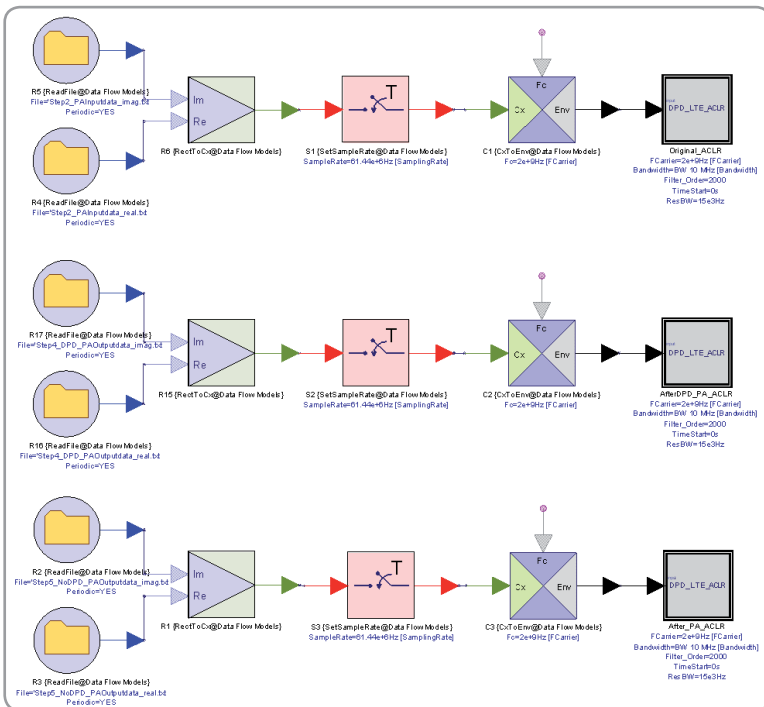


Figure 29. Schematic of ACLR

The setting of `RFPower` should be the same as Step 4. After capturing the waveform from the PA output, we can click the Spectrum, EVM and ACLR panels to run schematics for the spectrum comparison, EVM comparison and ACLR comparison, respectively (Figures 28, 29 and 30, and Table 2).

Two text files (`Step5_NoDPD_PAOutputdata_real.txt` and `Step5_NoDPD_PAOutputdata_imag.txt`) are generated in this step. Both files are saved real and imaginary of the PA without the DPD waveform, respectively.

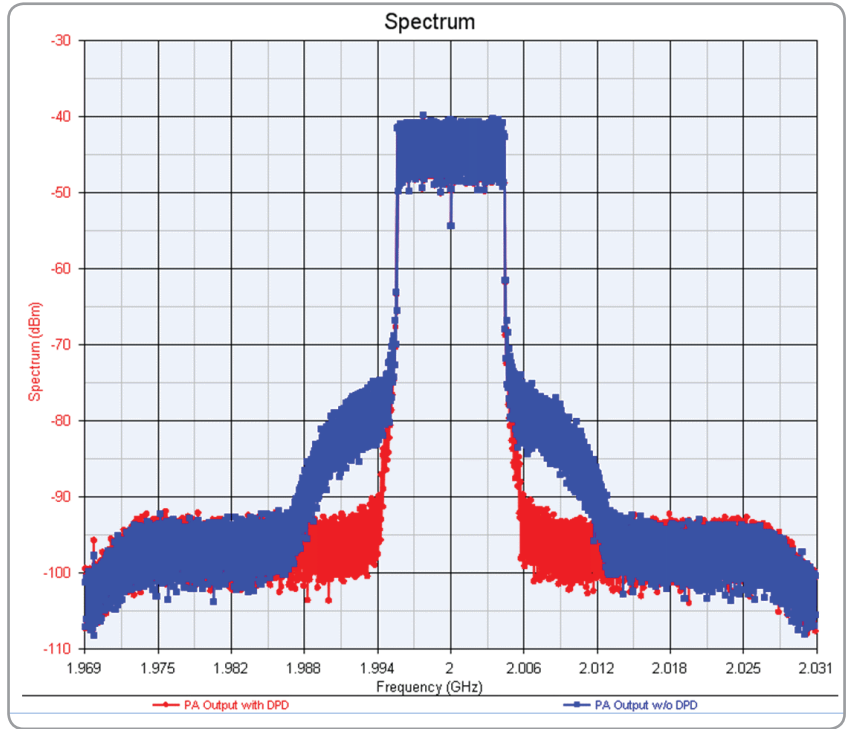


Figure 30. Spectrum of PA and DPD-PA

Table 2. LTE ACLR and EVM results of with and without DPD

ACLR	-2BW Lower	-1BW Lower	+1BW Upper	+2BW Upper	EVM (dB)
Raw signal	52.826	50.606	51.036	53.102	-20.689
PA output	51.687	38.224	38.484	51.997	-19.002
DPD+PA output	51.224	48.705	48.991	50.715	-20.585

Summary

Power amplifier linearization is a very important consideration in communication systems. The W1716 SystemVue Digital Pre-Distortion builder provides a memory polynomial algorithm for DPD simulation and hardware verification using Agilent test equipment. This application note discussed how to use SystemVue to do DPD hardware verification. Following the steps it outlined will help you prepare your amplifier to achieve the level of RF performance required by next-generation systems designs.

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