Combining Simulation and Test to Accelerate SDR Development

Software-defined capabilities create versatile test platforms that enhance design and test

Application Note

The goal of software-defined radio (SDR) technology is to provide a foundation for seamless interoperation between diverse communication systems. This level of interoperation is easy to envision but difficult to achieve. For example, the hardware and software elements required to enable greater flexibility introduce major challenges that reach back to the earliest stages of the design process. Later, as prototypes or end-user devices become available, interoperation introduces challenges and tradeoffs in testing methods and test systems.

In SDR design, development and test, tracing an issue back to its root cause can be a complex endeavor. This is often due to differences between the baseband and radio frequency (RF) sections of the design. The complexity is often compounded by three organizational factors: any separation between the baseband, RF and digital design teams; the divergent skill sets of analog and digital designers; and differences in the design and test tools used by each type of engineer. Addressing these issues early in the design process will help ensure timely completion and introduction of the end-user device.

This application note reviews the major attributes of SDRs then looks at three key topics: the use of multiple waveforms during SDR design, the use of simulation to add flexibility to SDR testing, and the use of logic analyzers and digital oscilloscopes to address baseband/RF testing challenges. These techniques can create a common ground that helps mitigate the risks caused by literal and figurative disconnects between baseband, RF and digital design teams and their designs.

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Reviewing SDR characteristics and Their implications

As context, let's define an SDR as follows: It's a radio in which the baseband processing—the physical or PHY layer—is implemented in re-configurable hardware and software. The PHY layer includes field-programmable gate arrays (FPGAs), as well as RF hardware such as mixers, filters, modulators, demodulators, and amplifiers. The software that emulates these devices may be a C program running in a digital signal processing (DSP) or general-purpose processor (GPP) chip, or could be VHDL code for an FPGA design

To the outside world, the result is a receiver/transmitter that can handle multiple types of formats and modulation schemes. This has two key benefits: flexibility and portability. An SDR offers greater flexibility through interoperation, which comes from the ability to support multiple waveforms, legacy formats, and new or future formats. Said another way, an SDR can be a backward-compatible and future-ready device. The technology provides portability by ensuring the ability to use an SDR waveform across platforms from a single vendor, or across platforms from multiple vendors. From a design perspective, portability also includes the ability to reuse waveform components across multiple devices or platforms.

Within the SDR, there is a technology shift: the amount of analog circuitry is decreasing while the quantity of digital technology is increasing. As a result, the digital circuitry is getting ever-closer to the antenna—and this transformation has important implications for both design and test.

Outlining the implications for design and test

In an SDR, RF performance is determined by not just the hardware but also the software elements. For example, a seemingly trivial bug fix in software could have a ripple effect that changes the radio's RF performance. On the hardware side, platforms from different vendors may offer different levels of functionality and performance. As a result, the hoped-for outcome of "write once, run anywhere" is not yet true in practice.

Within an SDR's mixed-signal path, there can be a mix of analog, RF, and digital probe points. Traditionally, digital and analog/RF teams have had their own design and test methodologies and tools, making it difficult to test along the SDR's mixed-signal path and introducing system integration risks. Addressing this issue has a two-pronged implication: designers need multiple ways to probe the signal path; however, to ensure valid comparisons, they also need a consistent way to measure the signals, both in design and test.

An SDR's actual RF performance depends on three aspects: baseband processing, radio configuration and the RF hardware. As a result, it can be difficult to isolate the root cause of a performance problem. This suggests the need for a consistent way to quantify RF performance in hardware and software.

To create a consistent approach to testing, practical experience suggests the use of three main elements: simulation software digital/baseband, and RF/IF test instruments. Specifically, the measuring instruments would be a logic analyzer, an oscilloscope, and vector signal analyzer (VSA) software. Additionally, a vector signal generator (VSG) with arbitrary waveform capabilities can be used to produce input signals.

Supporting future waveforms

In many instances, an SDR design will be expected to support field upgrades of radio functionality. This raises an issue: What can be done in the present—in design and manufacturing—to ensure confidence that the SDR will deliver sufficient performance with future waveforms and configurations?

Certainly, a different test strategy is needed, and there are two key elements to consider. First is the need to test not just supported waveforms but also possible radio configurations that might be used with future waveforms. Second is the need to identify a consistent set of tests that may include measurements such as adjacent-channel power (ACP), bit error ratio (BER), error vector magnitude (EVM), spurious and noise figure.

Focusing on possible waveforms, three approaches will be useful. One is to test the SDR with real, present-day waveforms and the required radio configurations. The next is to test with a broad selection of representative waveforms such as 64QAM. The third approach is to create custom waveforms that exercise different hardware configurations and make it easier to observe and characterize performance metrics such as phase noise and intermodulation distortion (IMD).

During the design process, simulation is an ideal vehicle for this test strategy. For example, a transmitter design could be tested with a variety of waveforms, defects, and impairments such as noise, DC offset, quadrature error, delay mismatch and distortion. The results of these simulations can be used to set the test limits used during actual measurements on prototype or final-article SDRs.

Figure 1 shows a consistent and seamless approach to evaluate a mixed-signal design in simulation and when testing the SDR hardware. VSA measurement elements can be used in simulation to evaluate the SDR design along the mixed-signal path. The VSA software can also be used with logic analyzers, oscilloscopes, and RF signal analyzers to evaluate the SDR hardware performance along the mixed-signal path during the hardware system integration testing phase.

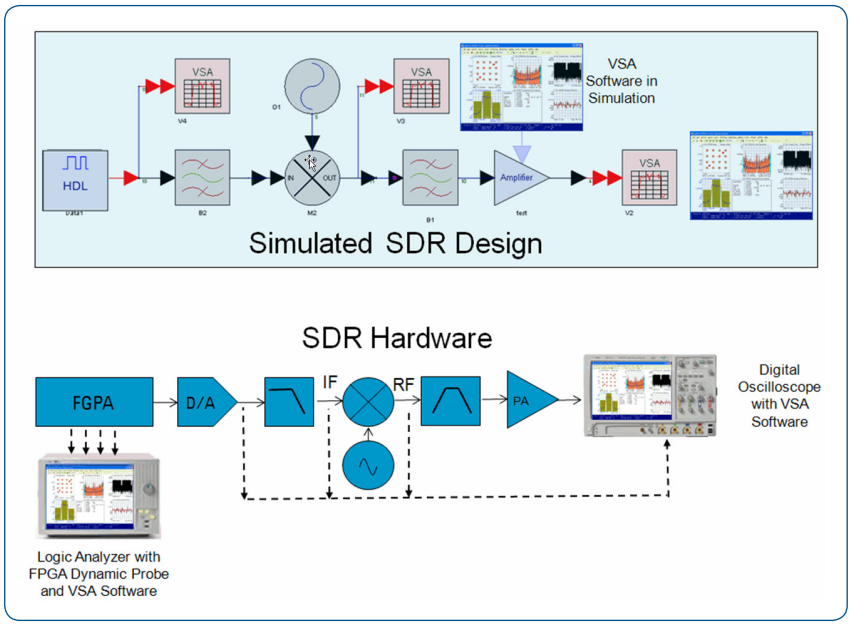

Figure 1. Using VSA software in design and test to evaluate SDR mixed-signal performance

Considering the longer-term implications

Stepping back to view the larger intent of SDR, there is a more imposing challenge: The need to design—and ultimately test—hardware capable of supporting waveforms and algorithms that are yet to be realized. As discussed in the sidebar "Supporting future waveforms," it is possible to use representative and custom waveforms and to exercise a variety of radio configurations and assess relevant performance characteristics. This technique can be used during development, diagnosis and manufacturing test.

Looking inside with FPGA dynamic probe

FPGA Dynamic Probe is a flexible tool that allows you to look inside an FPGA and view internal design signals. Virtual access is accomplished by connecting one or more actual FPGA pins to a logic analyzer. This approach has three important benefits:

- Increased visibility: Traditional logic analyzer probes limit measurements to signals at the periphery of the FPGA. With dynamic probe, you can measure up to 256 internal FPGA signals for each external FPGA pin dedicated to debug.
- Faster probing changes: With Agilent's dynamic probe, moving an FPGA-internal point is as easy as a mouse click. Neither design changes nor timing changes are required.
- More accurate set up: The dynamic probe automatically maps internal signal names from your FPGA design tool to the logic analyzer. Compared to manual methods, this capability saves time and eliminates potential mistakes.

Combining this capability with advanced logic analysis, physical probing and sophisticated triggering provides a powerful way to find the toughest bugs. For more information, please visit **www.agilent.com/find/fpga.**

Using a variety of waveforms in SDR design

To illustrate the preceding ideas, let's look at how different types of waveforms and waveform sources can be used in the design of an SDR RF transmitter. The waveforms will be either new or legacy formats. The four waveform sources are HDL code, FPGA hardware, simulation models and algorithm code.

The block diagram in Figure 2 applies to Examples 1 and 2. Using Agilent SystemVue electronic system-level (ESL) design software, the RF transmitter design was constructed using RF models of filters, mixers, local oscillators (LOs) and amplifiers. SystemVue also supports the simulation of potential issues such as amplifier gain compression, filter impairments and LO phase noise.

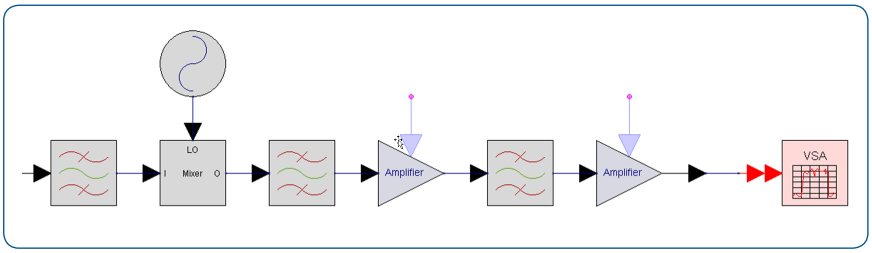

Figure 2. Block diagram for a SystemVue simulation of an RF transmitter design

Example 1: HDL-based WiMAX™ waveform

The first example uses HDL code being written for a new FPGA implementation. Because the SystemVue software supports HDL co-simulation, the HDL code can be used as a signal source to begin the transmitter design. In this case the co-simulated code is generating a Mobile WiMAX™ 64QAM signal, which is used as the input to the simulation of the transmitter design.

To provide a consistent measurement platform, the simulation output of the transmitter design can be analyzed with the Agilent 89600B VSA software. This software can run on a PC and inside certain Agilent signal analyzers, logic analyzers and oscilloscopes.

If the output of the simulated transmitter is distorting the waveform, it will show up in a constellation diagram (Figure 3) and will affect EVM measurements. It's important to note that EVM values will also be affected by any baseband fixed-point impairments from the co-simulated HDL code.

With these simulation and measurement capabilities, it's possible to evaluate the simulated RF design for interoperability by applying different waveforms. These tests can be performed by varying the values in parameterized HDL code or by applying other HDL-based waveforms.

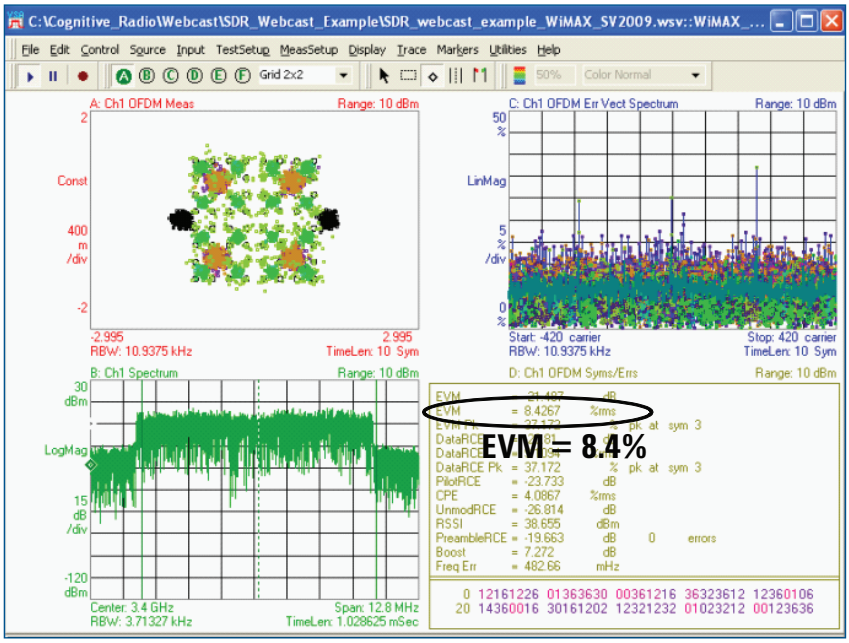

Figure 3. VSA measurement results from the simulated RF transmitter design

Example 2: FPGA-based legacy waveform

To test backward compatibility, legacy waveforms can be used as inputs to the simulated transmitter design. The first step is to capture the appropriate output signal from an FPGA development board—and the signal can be in either analog or digital format.

The analog output comes from the digital-to-analog converter (DAC) that converts an FPGA-based waveform into an analog modulated IF signal. This analog waveform can be captured with an Agilent Infiniium oscilloscope then transferred to SystemVue, which can use the waveform as a signal source input to the simulation of the transmitter.

Digital signals can be captured with a logic analyzer equipped with "FPGA dynamic probe." The dynamic probe capability is used to make measurements at various points inside the FPGA, thereby locating and capturing the appropriate digital signal (see sidebar). This signal can be transferred to SystemVue and used as the input to the transmitter.

With either analog or digital signals, testing the design for interoperability with a variety of legacy waveforms is a matter of reconfiguring the FPGA board to produce another waveform, capturing the signal with a scope or logic analyzer, and then transferring the analog or digital signal to SystemVue.

Example 3: Simulation-based WiMAX waveform

In transmitter design, EVM is an essential measure of signal quality. For receiver designs and receiver hardware, coded BER is typically a key metric. Measuring coded BER requires baseband coding and decoding functionality, and this is a challenge—and potential barrier—in receiver design and test. We can overcome this by using simulation models to provide baseband coding and decoding.

The block diagram in Figure 4 shows the SystemVue simulation of the RF receiver. The model includes an RF/IF downconverter with filters, a mixer, an LO and amplifiers as well as an analog-to-digital converter (ADC). ADCs are critical to SDR receiver performance and SystemVue includes a variety of device models.

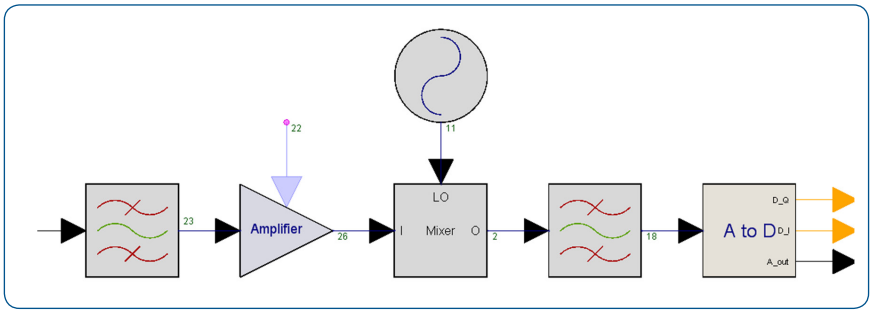

Figure 4. Block diagram for a SystemVue simulation of an RF receiver design

One key measure of receiver performance is the effect of ADC jitter on BER. Figure 5 shows three simulation results for the SDR receiver using WiMAX signals: QPSK (left), 16QAM (middle) and 64QAM (right). The plots show coded BER versus E_b/N_0 versus swept ADC jitter. Here, jitter is defined as a percentage of the simulation time step.[1]

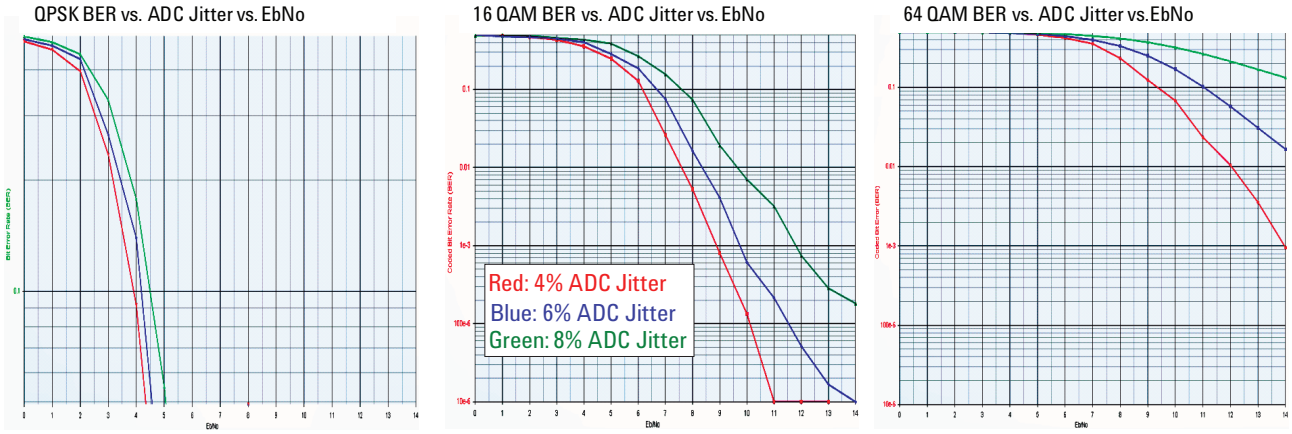

Figure 5. Results from an SDR receiver simulation with three WiMAX signals (QPSK, 16QAM and 64QAM)

Within each chart the left-most trace corresponds to 4 percent ADC jitter, the middle trace to 6 percent and the right-most trace to 8 percent. As shown, ADC jitter has a stronger impact on 64QAM than on QPSK, and this may be expected due to the closer constellation states in 64QAM. For SDR system engineers, this may suggest the need for stringent design requirements that support the higher data rates associated with 64QAM relative to QPSK.

1. *E_b/N_0, sometimes written "EbNo," is the ratio of (energy per bit) to (noise power spectral density).*

This approach can also be used to evaluate interoperability: First delete the existing waveform source and receiver and then replace them with the new waveform and receiver. In this case the WiMAX waveform was replaced with an LTE waveform and the resulting BER simulation is shown in Figure 6.

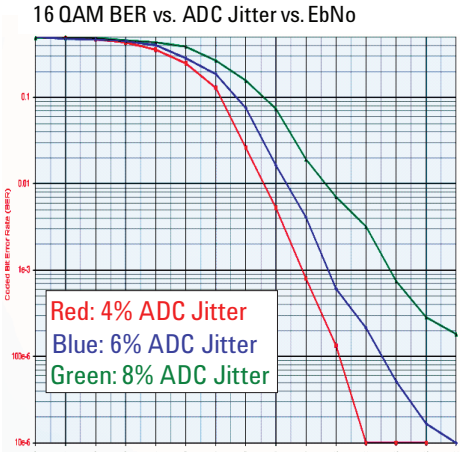

Figure 6. Results from an SDR receiver simulation with an LTE signal (64QAM)

Ideally, an SDR will use the same RF transceiver design to support a variety of waveforms. This typically requires changes to operating parameters such as filtering, gain, ADC settings, and so on. Simulation can be used to determine the optimum settings for each type of waveform.

Example 4: Algorithm-coded waveform

The final example uses algorithm code. The Mobile WiMAX and LTE models used in Examples 1-3 consist of preconfigured algorithm blocks that have been written in accordance with the respective standards.

Starting with the commercial representation as a baseline, the PHY-layer waveform algorithm code can be modified to create custom or proprietary OFDMA waveforms. Once modified, the customized algorithm code can be used during the design process and for SDR testing.

Using simulation to add flexibility to SDR testing

The inherent flexibility of an SDR provides functionality equal to that of multiple single-format radios—and this in turn demands a significant amount of RF testing. Those demands grow if the design is expected to support unknown radio formats without being retested in the future. The difficulty continues to increase if the design uses custom or proprietary waveforms that are not directly supported by commercial off-the-shelf (COTS) test equipment.

In such cases, a tightly linked combination of test equipment and simulation software can provide the flexibility needed to perform thorough, rigorous testing of SDR designs and devices. This approach has three important dimensions:

- Simulation enables customization of COTS equipment to support the creation, generation, measurement and analysis of custom or proprietary waveforms.
- Simulation makes it possible to support tomorrow's waveforms with today's test platforms.
- Common test tools applied to both design and test can also be used to help debug the hardware- and software-based elements of an SDR.

Two examples will help illustrate these concepts

Example 5: SDR FPGA testing with logic analyzer and FPGA dynamic probe

Figure 7 shows an FPGA development board being tested with a logic analyzer and VSA software. The FPGA implementation was designed using fixed-point schematic elements in SystemVue and HDL code generation. Xilinx Chipscope Pro is used to configure a debug mux core called ATC2 (Agilent Trace Core second generation). The core allows you to quickly access incremental sets of internal signals with a mouse click. For this example, we've configured the core with four banks of pre-selected signals.

Each of the probe banks are selected, then demodulated using the VSA software in the Logic Analyzer. Figure 7 shows the demodulation results at FIR inputs with 1X oversampling (left), FIR outputs with 4X oversampling (middle), and multiplexed digital Fs/4 IF output (DAC inputs) with 4X oversampling (right).

Because the VSA software can also be used in simulation (Figure 1), hardware test results can be compared with VSA simulation results from either a fixed-point simulation with the VSA software or an HDL co-simulation with the VSA software.

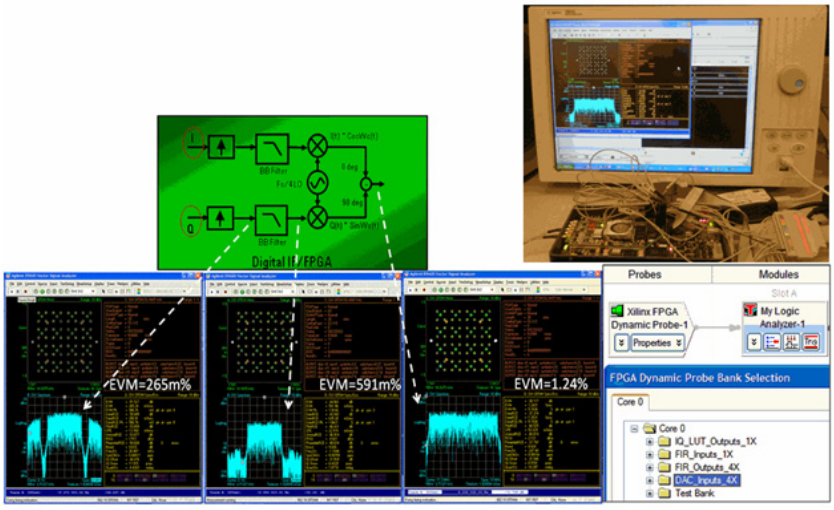

Figure 7. FPGA dynamic probe with the logic analyzer and VSA software

Example 6: Using simulation to add flexibility to SDR receiver testing

The next example shows how coded BER can be tested on an RF in/digital out mixed-signal receiver. To illustrate this process, the DUT was a 14-bit ADC similar to the one used in Example 3. The test system included a logic analyzer, a signal generator and the SystemVue simulation software.

SystemVue was installed in the logic analyzer where it provided the baseband coding and decoding necessary to perform a coded BER measurement on the hardware DUT. The simulated signal, which simulated the baseband coding, was downloaded to an Agilent MXG signal generator with an arbitrary waveform generator.

The MXG turned the simulated signal into a real-world waveform that was fed into the analog input of the ADC. The DUT's digital output was captured with the logic analyzer and read into SystemVue, which performed the simulated baseband decoding so the logic analyzer could measure the coded BER .

Using this configuration, multiple BER curves were measured by sweeping the RF output power of the signal generator. The results were plotted as measured BER versus IF input power, as shown in Figure 8. The figure shows results for QPSK, 16QAM and 64QAM (left, middle and right traces, respectively) SystemVue could also be used to set the DUT biases to generate additional BER curves under a range of possible operating conditions.

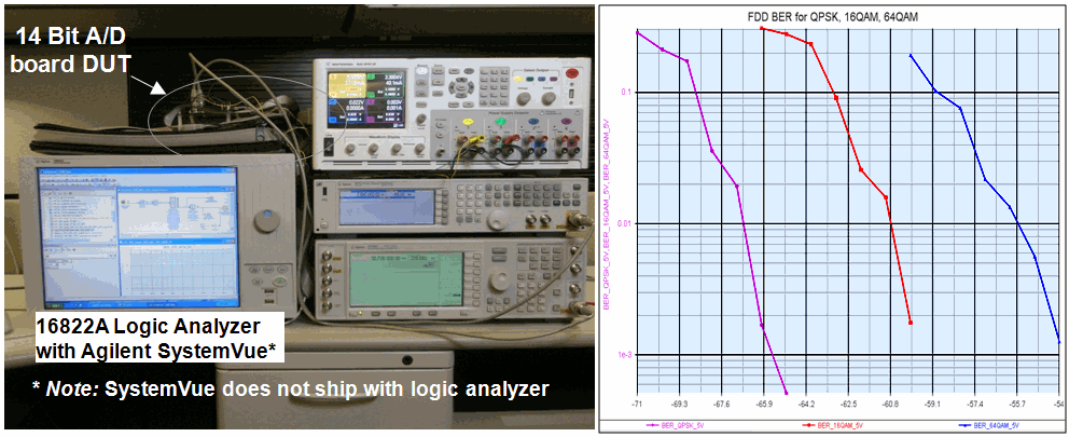

Figure 8. Measurements of BER vs. IF input power from a 14-bit ADC (QPSK, 16QAM and 64QAM signals) using logic analyzer and SystemVue

Note that this is a software-defined test setup: The test waveform is being generated and analyzed by the simulation software that's running inside the logic analyzer. Because simulation tools are being used, the coding and decoding of PHY-layer algorithms can be customized. In fact, the different types of waveform sources discussed in the earlier examples can all be applied to SDR hardware testing.

This enables the creation and analysis of custom test waveforms: proprietary OFDMA waveforms; waveforms with impairments such as multipath fading or phase noise; and more. The net result is a highly flexible SDR test platform.

Conclusion

Seamless interoperation of SDRs is easy to envision, and it becomes easier to achieve with the techniques described here. The ability to probe—physically or virtually—at multiple points along and inside the simulated receiver and transmitter and hardware mixed-signal paths makes it easier to trace an issue back to its root cause. The decision to adopt a common set of measurement tools—logic analyzer, oscilloscope, VSA software and simulation software—provides a consistent basis of comparison for baseband, RF and digital design teams.

The enabling technology is digital signal processing. Many of today's highly advanced test instruments contain the same types of software-defined DSP capabilities that are being used inside SDRs. Combined with simulation, this creates highly versatile test platforms that can be utilized in the design, development and testing of present and future waveforms and SDRs.

Related products

- Agilent 89600B VSA software, **www.agilent.com/find/89600B**
- Agilent SystemVue ESL design software, **www.agilent.com/find/SystemVue**
- Agilent Infiniium 90000 oscilloscopes, **www.agilent.com/find/90000X-series**
- Agilent 16800 Series portable logic analyzers, **www.agilent.com/find/16800**
- Agilent X-Series signal analyzers, **www.agilent.com/find/X-Series**

Related information

- *Software Defined Radio Measurement Solutions*, Application Note 5989-6931EN
- *Making RF Measurements on Digital Serial Data with Agilent's Signal Extractor and the 89601A Vector Signal Analyzer* , Application Note 5989-5290EN

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