HP 3589A Service Guide

(Includes HP 35689A/B)

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HEWLETT PACKARD

Safety Summary

The following general safety precautions must be observed during all phases of operation, service, and repair of this instrument. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of the instrument. Hewlett-Packard Company assumes no liability for the customer's failure to comply with these requirements. This is a Safety Class 1 instrument.

Ground The Instrument

To minimize shock hazard, the instrument chassis and cabinet must be connected to an electrical ground. The instrument is equipped with a three-conductor ac power cable. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet. The power jack and mating plug of the power cable meet International Electrotechnical Commission (IEC) safety standards.

Do Not Operate In An Explosive Atmosphere

Do not operate the instrument in the presence of flammable gases or fumes. Operation of any electrical instrument in such an environment constitutes a definite safety hazard.

Keep Away From Live Circuits

Operating personnel must not remove instrument covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

Do Not Service or Adjust Alone

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

Do Not Substitute Parts or Modify Instrument

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification to the instrument. Return the instrument to a Hewlett-Packard Sales and Service Office for service and repair to ensure the safety features are maintained.

Dangerous Procedure Warnings

Warnings, such as the example below, precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

Warning 

Dangerous voltages, capable of causing death, are present in this instrument. Use extreme caution when handling, testing, and adjusting.

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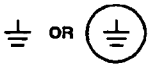
Safety Symbols

The following safety symbols are used throughout this manual and in the instrument. Familiarize yourself with each symbol and its meaning before operating this instrument.

General Definitions of Safety Symbols Used On Equipment or In Manuals.

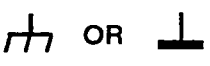
Instruction manual symbol: the product will be marked with this symbol when it is necessary for the user to refer to the instruction manual in order to protect against damage to the instrument.

Indicates dangerous voltage (terminals fed from the interior by voltage exceeding 1000 volts must be so marked.)



Protective conductor terminal. For protection against electrical shock in case of a fault. Used with field wiring terminals to indicate the terminal which must be connected to ground before operating equipment.

Low-noise or noiseless, clean ground (earth) terminal. Used for a signal common, as well as providing protection against electrical shock in case of a fault. A terminal marked with this symbol must be connected to ground in the manner described in the installation (operating) manual, and before operating the equipment.



Frame or chassis terminal. A connection to the frame (chassis) of the equipment which normally includes all exposed metal structures.

Alternating current (power line).

Direct current (power line).

Alternating or direct current (power line).

Warning

The WARNING sign denotes a hazard. It calls attention to a procedure, practice, condition or the like, which if not correctly performed or adhered to, could result in injury or death to personnel.

Caution

The CAUTION sign denotes a hazard. It calls attention to an operating procedure, practice, condition or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product.

Note

The NOTE sign denotes important information. It calls attention to procedure, practice, condition or the like, which is essential to highlight.

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Introducing the HP 3589A and HP 35689A/B

Instrument Description

The HP 3589A Spectrum/Network Analyzer is a high performance, 10 Hz to 150 MHz, synthesized network/spectrum analyzer offering swept spectrum, narrow band zoom, and vector network measurements. Swept spectrum mode uses digital IF filters that allow increased measurement speed (up to four times faster than conventional swept-tuned analyzers for comparable measurements) with no additional amplitude error or resolution loss. Narrow band zoom mode uses an implementation of the Fast Fourier Transform to provide even faster measurements (up to 350 times faster than conventional swept-tuned analyzers for comparable measurements) with even greater resolving power. Narrow band zoom mode can be used for spans of 40 kHz and less. Vector network mode provides complete frequency-domain characterization. With the addition of the HP 35689A/B S-Parameter Test Set, the HP 3589A can do complete one-port or two-port vector network analysis. The HP 35689A is a 50Ω S-Parameter test set and the HP 35689B is a 75Ω S-Parameter test set.

The HP 3589A Spectrum/Network Analyzer has a built-in source with programmable amplitude. Measurements can be saved using the internal non-volatile memory or the internal 3.5-inch flexible disk drive. Plots and prints of the measurements can be made directly to HP-IB printers and plotters. Options include time-gated spectrum analysis, HP Instrument BASIC programming language (IBASIC), and PC-compatible keyboards.

Safety Considerations

The HP 3589A Spectrum/Network Analyzer and the HP 35689A/B S-Parameter Test Set are Safety Class 1 instruments (provided with a protective earth terminal). Although these instruments have been designed in accordance with international safety standards, this manual contains information, cautions and warnings that must be followed to ensure safe operation and retain the instruments in safe operating condition. Service must be performed by trained service personnel who are aware of the hazards involved (such as fire and electrical shock).

Options

The following options are available to upgrade your HP 3589A Spectrum/Network Analyzer. Order HP 3589U followed by the option number below:

- 1D5 High Stability Frequency Reference
- 1D6 Time-Gated Spectrum Analysis
- 1C1 Additional 2 Mbyte RAM
- 1C2 HP Instrument BASIC
- 1D7 50/75 Ohm Minimum Loss Pad(s)

Accessories

The accessories are listed in four tables — table 1-1 lists accessories supplied with the HP 3589A Spectrum/Network Analyzer, table 1-2 lists accessories supplied with the HP 35689A/B S-Parameter Test Set, table 1-3 lists accessories available for the HP 3589A Spectrum/Network Analyzer, and table 1-4 lists accessories available for the HP 35689A/B S-Parameter Test Set.

Table 1-1. Accessories Supplied with the HP 3589A

Accessory	Part Number
Line Power Cable	See figure 2-3
Plastic Transportation Disk	HP 5061-2819
25Ω BNC feedthrough series resistors (2)	HP 1250-2275
Nylon mounting clips for BNC feedthrough series resistor (2)	HP 1400-1356
N-to-BNC adapters (2)	HP 1250-0780
Standard Data Format Utilities Includes *Standard Data Format Utilities Disk, 3 1/2 inch, 1 Of 2* *Standard Data Format Utilities Disk, 3 1/2 inch, 2 Of 2* *Standard Data Format Utilities Disk, 5 1/4 inch, 1 Of 2* *Standard Data Format Utilities Disk, 5 1/4 inch, 2 Of 2* *Standard Data Format Utilities User's Guide* *Standard Data Format Utilities Quick Reference*	HP 5061-8037 HP 5010-3316 HP 5010-3317 HP 5010-3318 HP 5010-3319 HP 5959-5791 HP 5959-5790
HP 3589A Performance Test Guide Includes: *HP 3589A Semiautomated Performance Test Disk* *HP 35689A/B Semiautomated Performance Test Disk*	HP 03589-90001 HP 03589-19407 HP 35689-19402
HP 3589A Quick Start Guide	HP 03589-90002 in English or HP 03589-90005 in Japanese
HP 3589A Operator's Guide	HP 03589-90021
HP 3589A Programmer's Reference	HP 03589-90020
With option 1D5 Coax BNC (m)-to-coax BNC(m) connector	 HP 1250-1499

Table 1-2. Accessories Supplied with the HP 35689A/B

Accessory	Part Number
Line Power Cable	See figure 2-3
RF Connecting Cables (2)	HP 8120-4387
Interconnect Cable	HP 35689-61612

Table 1-3. Available Accessories for the HP 3589A

Accessory	Part Number
Active probe	HP 41800A
50 to 75 ohm minimum loss pad	HP 11852B #004
Rack mount kit	HP 35660-86010
Box of ten 3.5-inch double-sided, double-density disks	HP 92192A
HP 3589A Operator's Reference	HP 03589-90000
HP Instrument BASIC User's Handbook	HP E2083-90000
Using HP Instrument BASIC with the HP 3589A	HP 03589-90009
Sample IBASIC Programs Disk	HP 5959-5710
Service kit	HP 03588-84401
HP 3589A Service Guide Includes. *HP 3589A Semiautomated Performance Test Disk* *HP 35689A Semiautomated Performance Test Disk*	HP 03589-90010 HP 03589-19407 HP 35689-19402
PC Style 101-key keyboard U.S. ASCII U.K. English German French Italian Spanish Swedish Keyboard cable	 HP C1405A #ABA HP C1405A #ABU HP C1405A #ABD HP C1405A #ABF HP C1405A #ABZ HP C1405A #ABE HP C1405A #ABS HP 5081-2249
Transit case	HP 9211-2663

Table 1-4. Available Accessories for the HP 35689A/B

Accessory	Part Number
Handle kit	HP 5062-3988
Rack mount kit	HP 5062-3974
Rack mount and handle kit	HP 5062-3975

Firmware Version Code

As with changes to the instrument hardware, Hewlett-Packard also makes changes to its firmware. To determine which version of firmware is in your analyzer, press the following keys:

[**Special Fctn**]
[NON-VOL SETUP]
[VERSION]

An information block appears on the screen for about five seconds (pressing [VERSION] repeats the information).

Serial Numbers

Hewlett-Packard makes frequent improvements to its products to enhance their performance, usability, or reliability, and to control costs. HP service personnel have access to complete records for each instrument model, based on the equipment's serial number. Whenever you contact HP about your analyzer, have the complete serial number available to ensure obtaining the most complete and accurate information possible.

A serial number label is attached to the rear of the analyzer. The serial number has two parts — the prefix (the first four numbers and a letter) and the suffix (the last five numbers).

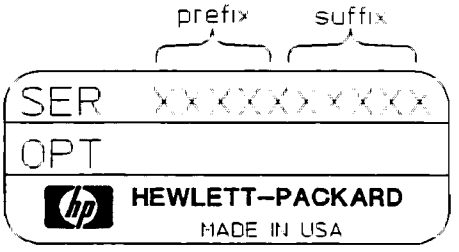


Figure 1-1. Serial Number Label

You can also access the serial number from the front panel by pressing the following keys:

[**Special Fctn**]
[NON-VOL SETUP]
[SERIAL NUMBER]

An information block appears on the screen for about five seconds (pressing [SERIAL NUMBER] repeats the information).

Recommended Test Equipment

The recommended test equipment is listed in six tables. Tables 1-5, 1-6, and 1-7 list the equipment needed to verify specifications for the HP 3589A, HP 35689A, and HP 35689B. Tables 1-8, 1-9, and 1-10 list the additional equipment needed to adjust or troubleshoot the HP 3589A, HP 35689A, and HP 35689B. Other equipment may be substituted for the recommended model if it meets or exceeds the listed critical specifications. When substitutions are made, you may have to modify the procedures to accommodate the different operating characteristics.

Table 1-5. Recommended Test Equipment for the HP 3589A

Instrument	Critical Specifications	Recommended Model
Attenuator	(2) 10 dB 20 to 30 MHz	HP 8491A Opt 010
Digital Multimeter	Frequency Range: 10 Hz to 300 kHz AC Range 2 mV to 20V Amplitude Accuracy: ± 0 1% dBm Math Mode	HP 3458A
Frequency Standard	Frequency Accuracy: ±0.0025 ppm	HP 5061B
Milliwatt Power Meter	Power Range: ± 0.2 dBm 10 Hz to 100 Hz. ± 0.4 dB 100 Hz to 30 kHz: ± 0.27 dB 300 kHz: ± 0.035 dB 30 kHz to 150 MHz. ± 0.13 dB Input Impedance: 50Ω 0 dBm Control Voltage Output	W & G EPM-1†
Power Meter	Frequency Range: 100 kHz to 150 MHz Input Range: 100 kHz to 150 MHz Amplitude Accuracy (with power sensor): ± 0.27 dB	HP 438A Alternate HP 436A
Power Sensor	SWR: ≤ 1.20 Impedance: 50Ω	HP 8482A
Power Splitter	SWR: ≤ 1.10 Input Impedance: 50Ω Two Outputs	HP 11667A
Power Supply	Volts: +20 Vdc Amps: 0.5	HP 6236B
Spectrum Analyzer	Frequency Range: 100 Hz to 150 MHz Amplitude Range: –100 to 20 dBm Dynamic Range: ≤ –52 dBc Phase Noise: <–86 dBm/Hz at 500 Hz offset Marker Noise Function	HP 8568B

† This equipment is only used in the "Input Amplitude Accuracy and Flatness" test. The "Alternate Input Amplitude Accuracy and Flatness" test does not require this equipment. To order this equipment contact Wandel & Goltermann, Inc., 1800 Wyatt Drive Suite 2, Santa Clara, CA 95054 (408) 988-7622.

Table 1-5. Recommended Test Equipment for the HP 3589A (continued)

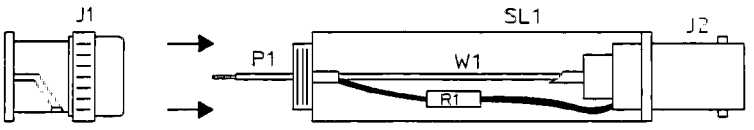
Instrument	Critical Specifications	Recommended Model
Synthesized Signal Generator	Dynamic Range: <–92 dBc Frequency Range: 1 MHz to 150 MHz Impedance: 50Ω Resolution: 0.1 Hz External Reference Input	HP 8663A Alternate HP 8662A
Step Attenuator (with calibration data at 100 kHz and 300 kHz)	0 to 70 dB: ± 0.02 dB	HP 355D Alternate HP 8495A HP 8495B
Synthesizer	Frequency Range: 10 Hz to 10 MHz Impedance: 50Ω	HP 3326A Alternate HP 3325A HP 3325B
Synthesizer/Level Generator	Frequency Range: 10 MHz to 25 MHz Harmonic Distortion: ≤ –32 dBc	HP 3335A
21 MHz Low Pass Filter	Filter Rejection: ≤ –60 dB Impedance: 50Ω	TTE # J87-21M-50-613B †
50 MHz Low Pass Filter	Filter Rejection: ≤ –60 dB Impedance: 50Ω	TTE # J87-50M-50-613B †
10 dB Amplifier	(2) Frequency Range: 10 kHz to 150 MHz	QB-210 ‡
50Ω Directional Bridge	Directivity: >40 dB Impedance: 50Ω Frequency Range: 50 to 150 MHz	HP 35677-63502
50Ω Feedthrough Termination	± 0.2% at dc	HP 11048C
100 kΩ Feedthrough Termination	± 0.2% at dc	see figure 1-2
Adapters	(5) N(m)-to-BNC(f) (4) SMA(m)-to-BNC(f) BNC(f)-to-Dual Banana Plug (2) N(f)-to-BNC(m) N(f)-to-BNC(f) N(m)-to-N(m) (2) SMA(m)-to-BNC(m) BNC Tee (2) BNC(f)-to-Alligator Clip	HP 1250-0780 HP 1250-1200 HP 1251-2277 HP 1250-0077 HP 1250-1536 †† HP 1250-1475 HP 1250-1787 HP 1250-0781 Pomona model 2630 ‡‡
Cables	(7) BNC-to-BNC 122 cm Error Correction Cable	HP 8120-1840 HP 03588-61630 ††

† To order this equipment contact TTE, Inc. 2214 S. Benny Avenue, Los Angeles, CA 90064.

‡ To order this equipment contact Q-Bit Corp. PO Box 2208, Melbourne, FL 32901 (407) 727-1838.

†† This equipment is only used in the "Input Amplitude Accuracy and Flatness" test. The "Alternate Input Amplitude Accuracy and Flatness" test does not require this equipment.

‡‡ To order this equipment contact ITT Pomona Electronics, 1500 East Ninth Street, Pomona, CA 91769 (714) 623-3463.



MATERIALS

Item	Qty	Description	HP Part Number
J1	1	Connector BNC male	1250-0052
J2	1	Connector BNC female	1250-0083
P1	1	Pin	1250-0089
SL1	1	Sleeve	1531-0246
R1	1	Resistor 100 kΩ	0757-0465
W1	2cm	Wire 24 AWG	8150-0295

Figure 1-2. 100 kΩ Feedthrough Termination

Table 1-6. Recommended Test Equipment for the HP 35689A

Instrument	Critical Specifications	Recommended Model
Spectrum/Network Analyzer	HP 35689A/B interface	HP 3589A
Short	50Ω, N(m)	HP 11512A
Z0 Terminations	(2) Precision 50Ω, N(m), ≥ 52 dB return loss 50Ω, N(m), ≥ 26 dB return loss	HP 909C HP 909A
Cables	(2) 50Ω, N(m)-to-N(m) (2) BNC-to-BNC 122 cm	HP 8120-4666 HP 8120-1840
Adapters	50Ω, N(f)-to-N(f) (5) 50Ω, N(m)-to-BNC(f) (2) SMA(m)-to-BNC(f) 50Ω, N(m)-to-N(m)	HP 1250-1472 HP 1250-0780 HP 1250-1200 HP 1250-1475
50Ω Directional Bridge	Directivity: >40 dB, Impedance: 50Ω Frequency Range: 50 to 150 MHz	HP 35677-63502

Table 1-7. Recommended Test Equipment for the HP 35689B

Instrument	Critical Specifications	Recommended Model
Spectrum/Network Analyzer	HP 35689A/B interface	HP 3589A
Shorts	75Ω, N(m) 50Ω, N(m)	HP1250-1530 HP 11512A
Z0 Terminations	(2) Precision 75Ω, N(m), ≥ 52 dB return loss 50Ω, N(m), ≥ 26 dB return loss	HP 909E HP 909A
Cables	(2) 75Ω, N(m)-to-N(m) (2) BNC-to-BNC 122 cm	HP 8120-4667 HP 8120-1840
Adapters	75Ω, N(f)-to-N(f) (5) 50Ω, N(m)-to-BNC(f) (2) SMA(m)-to-BNC(f) 50Ω, N(m)-to-N(m)	HP 1250-1529 HP 1250-0780 HP 1250-1200 HP 1250-1475
50Ω Directional Bridge	Directivity: >40 dB, Impedance: 50Ω Frequency Range: 50 to 150 MHz	HP 35677-63502

Table 1-8. Additional Recommended Test Equipment for the HP 3589A †

Instrument	Critical Specifications	Recommended Model
Frequency Counter	Frequency Range: 10 to 500 MHz Resolution: <1 Hz at 10 MHz Frequency Accuracy: $\pm 25 \times 10^{-3}$ Hz Sensitivity: –28 dBm Impedance: 1 MΩ	HP 5334B Opt 030 Alternate HP 5343A
Logic Probe	TTL/CMOS Maximum Clock: >25 MHz	HP 545A Alternative HP 5006A HP 5005A/B
Oscilloscope	Bandwidth: ≥ 150 MHz Vertical Sensitivity: 10 mV/div Input Coupling: AC, DC, 50Ω Waveform Math: A-B Trigger: Ext, Int, Chop	HP 54111D
Oscilloscope Probe	Input R: ≥ 1 MΩ Division Ratio: 10:1	HP 10431A
Oscilloscope Probe	Input R: ≥ 1 MΩ Division Ratio: 1:1	HP 10438A
Resistive Divider Probe Kit	Impedance: 50Ω Division Accuracy: ± 3% Input Capacitance: <0.7 pF Division Ratio: 1:1, 5:1, 10:1, 20:1, 50:1, 100:1	HP 10020A
Ball Driver Hex Tool	Size 3/32	Bondhus ‡
Spectrum Analyzer	Impedance: 1 MΩ Frequency Range: 20 Hz to 200 kHz Amplitude Accuracy: ± 1dB	HP 3585B
Adapter	SMB(f)-to-Coax BNC(f)	HP 1250-1236
HP 3589A Service Kit	Includes: Power Supply Test Board SMB Extender Cables (7) Extender Board, 12 pin Extender Board, 48 pin Fast Bus Extender Cable BNC-to-SMB Cable (2) Capacitive Load SMB-to-SMB Adapter (2) Flat -Edge Adjustment Tool Small Adjustment Tool Service Disks	HP 03589-84401 Includes: HP 35672-66590 HP 03585-61610 HP 03588-66595 HP 03588-66596 HP 35660-61621 HP 03585-61616 HP 35660-64401 HP 1250-0669 HP 8710-1928 HP 8710-1514 HP 03589-69401

† Not required for performance tests—only required for adjustment and troubleshooting procedures.

‡ To order this equipment contact Tool Kit Specialist Inc. Sunnyvale, CA (408) 745-6020.

Table 1-9. Additional Recommended Test Equipment for the HP 35689A †

Instrument	Critical Specifications	Recommended Model
Cables	(3) 50 Ω, N(m)-to-N(m), 183 cm 50 Ω, SMA(m)-to-Right Angle SMA(m)	HP 11500A Pomona 4814-BB-48
Adapter	N(m)-to-SMA(f)	HP 1250-1250

† Not required for performance tests—only required for troubleshooting procedures.

Table 1-10. Additional Recommended Test Equipment for the HP 35689B †

Instrument	Critical Specifications	Recommended Model
Cables	(2) 50 Ω, N(m)-to-N(m), 183 cm 50 Ω, SMA(m)-to-Right Angle SMA(m) 75 Ω, BNC(m)-to-BNC(m)	HP 11500A Pomona 4814-BB-48 HP 11652-60013
Cable Kit	Cables (2) 75 Ω, N(m)-to-N(m), 610 mm Adapter 75 Ω, N(f)-to-N(f)	HP 35679B
Adapters	N(m)-to-SMA(f) 75 Ω, N(m)-to-BNC(f) 75 Ω, N(f)-to-BNC(m)	HP 1250-1250 HP 1250-1535 HP 1250-1534
Feedthrough Series Resistor	25Ω BNC	HP 1250-2275

† Not required for performance tests—only required for troubleshooting procedures.

HP 3589A Specifications

General Specifications

Note: All specifications apply from 10 Hz to 150 MHz and include 30 minute warm-up from ambient conditions unless otherwise noted. Supplemental characteristics (identified as characteristic only) are non-warranted functional and feature information.

The general specifications apply independent of the measurement type selected. Refer to the spectrum measurements and network measurements for specifications that are measurement type dependent.

Frequency Specifications

Frequency range
Tuning range: 0 Hz to 150 MHz
Specifications for 50 and 75Ω apply over the frequency range 10 Hz to 150 MHz. The 1 MΩ input operates over the full span and is specified from 10 Hz to 40 MHz.

Frequency accuracy
Frequency accuracy is specified using the frequency counter marker function and is the sum of initial accuracy, aging, and frequency counter resolution.

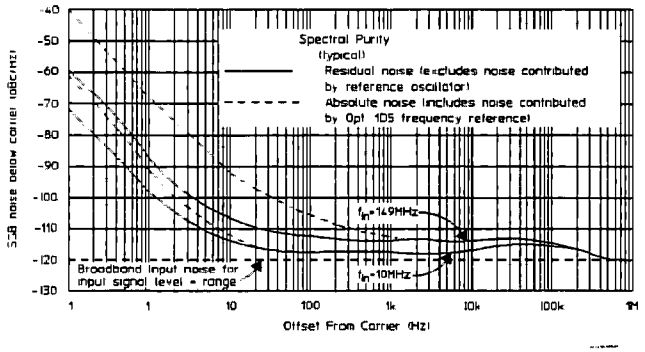
Initial accuracy:

	Without opt 1D5	With opt 1D5‡
20 ° to 30 °C	± 0.5 ppm	± 0.01 ppm
0 ° to 55 °C	± 3.0 ppm	± 0.07 ppm
Aging†	± 0.25 ppm/mo	± 0.125 ppm/mo

† Referenced to the most recent reference calibration at 23 °C
‡ Add ± 0.1 ppm if the instrument has been continually powered < 48 hours.

Frequency counter resolution: 0.1 Hz

Stability
Spectral Purity: See chart below.
Noise sidebands: less than -105 dBc when measured at a 1 kHz offset from CW signal and normalized to a 1 Hz noise-power bandwidth.



Note: Equivalent noise bandwidth is narrower than 1 Hz for spans below 150 Hz with the narrowband zoom measurement type, providing additional reduction in phase noise from that shown. This maintains good dynamic range, even for extremely small offset frequencies in narrow spans. Noise is reduced by 10*Log[1/noise bandwidth] dBc relative to the previous graph.

Drift/residual FM
The HP 3589A uses a fully synthesized local oscillator and is phase-locked to the frequency reference throughout the sweep. Refer to the frequency accuracy specifications stated earlier for the resulting accuracy.

Amplitude Specifications

Amplitude measurement range:

Maximum Safe Input Level

	50Ω	75Ω	1 MΩ
Avg Continuous Power: (10 Hz to 150 MHz)	26 dBm	28 dBm	13 dBV
dc Voltage:	± 4V	± 4V	± 25V
Combined ac/dc:	± 4 Vpk	± 4 Vpk	± 25 Vpk

Maximum Without Degrading Performance

	50Ω	75Ω	1 MΩ
Input dc:	± 3 Vdc	± 3 Vdc	± 25 Vdc
Measured input	20 dBm	22 dBm† 26 dBm‡	± 7 dBV

† With included BNC adapter
‡ With minimum loss pad (optional)

Input range settings
(characteristic only)
50Ω input (in 10 dB steps): +20 dBm to -20 dBm
75Ω input (in 10 dB steps) +21.76 dBm to -18.24 dBm, with included BNC adapter and automatic corrections.
+25.72 dBm to -14.28 dBm, with minimum loss pad (option) and automatic corrections
1 MΩ input (in 10 dB steps): +7 dBV to -33 dBV

Amplitude display range
Reference level: -1000 to +1000 dBm, dB
Display resolution: 0.001 to 100 dB/div
Marker resolution: 0.01 dB
Display units: dBm, dBV, Vrms

Normalization
Normalization routines allow the single receiver channel to accurately measure scalar network parameters when swept spectrum measurement type is selected, or vector network parameters when swept network measurement type is selected. Measurement normalizations require the reference measurement to be taken first, using either quick normalization, which uses an internal source to receiver path, or transmission normalization, which can correct for additional cable, adapter, and fixture effects. Measurements are then referenced to that measurement as a ratio.

Input port
Input channels: 1
Return loss: >20 dB
Impedance: 50Ω, 1 MΩ (<60 pF shunt capacitance)
(75Ω with included BNC adapter or optional minimum loss pad)
Connector: Type-N

Source Specifications

Frequency specifications
(characteristic only)
Frequency range: 10 Hz to 150 MHz

Amplitude specifications
Amplitude range 50Ω output +15 dBm to -54.9 dBm and off
Amplitude range 75Ω output +13.2 dBm to -56 7 dBm and off, with included BNC adapter.
+9.3 dBm to -60.6 dBm and off, with minimum loss pad (option).

Amplitude resolution 0.1 dB

Accuracy: Output amplitude accuracy is determined by the sum of absolute accuracy, dynamic accuracy, and frequency response.

Absolute amplitude accuracy: ± 1 dB
(at 300 kHz, +15 dBm output level)
Dynamic accuracy Add 0.02 dB/dB below 15 dBm
(add to absolute accuracy)
Frequency response: ± 1 dB
(Variations relative to the level at 300 kHz)

Spurious products:
Harmonic products: < -28 dBc
Non-harmonic products: < -40 dBc

Noise: < -80 dBc/Hz
(for offsets greater than 500 Hz from the carrier)

Source port:
Return loss: > 20 dB
Impedance: 50Ω
(75Ω with included BNC adapter or optional minimum loss pad)
Connector: Type-N

Spectrum Measurements

All specifications apply from 10 Hz to 150 MHz and include 30 minute warm-up from ambient conditions unless otherwise noted. Typical performance is applicable over ± 5 °C from the temperature during the most recent autocalibration and is not warranted. Supplemental characteristics (identified as characteristic only) are non-warranted functional and feature information.

All spectrum measurement specifications apply when swept spectrum or narrowband zoom measurement type is selected and with the source turned off and low-distortion mode off unless otherwise noted.

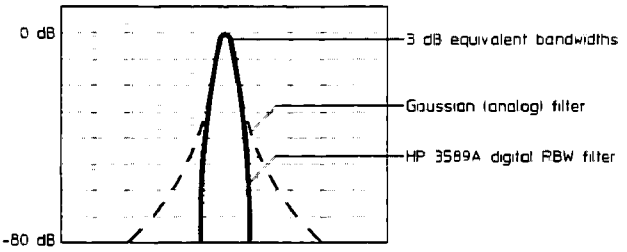
Frequency Specifications

Frequency span
(characteristic only)
Swept spans
Range: 10 Hz to 150 MHz, and zero span
Resolution: 0.1 Hz
Accuracy: Greater of 0.1 Hz or 0.125% of span
Start/stop frequency: 0 Hz to 150 MHz

Narrowband zoom spans:
Range: 1.23 Hz to 40 kHz in x2 steps
Accuracy: ± 0.001% of span

Resolution bandwidth
Swept spectrum: 1.1 Hz to 17 kHz ± 10%

Narrowband zoom
High-accuracy mode: 0.90% of span (11 mHz - 360 Hz)
High-resolution mode 0.37% of span (4 5 mHz - 148 Hz)



HP 3589A digital RBW filter shape (solid line) compared with a standard (Gaussian) analog RBW filter of equivalent 3 dB bandwidth. Shape factor of the analog filter is approximately 11:1.

Bandwidth selectivity
(shape factor or ratio of -60 dB to -3 dB bandwidths)

Swept spectrum mode:
(see also filter comparison graph)
Manual sweep: < 4.0:1
Auto-coupled sweep: 4 3:1 (typical)
Auto-coupled oversweep: 5.1:1 (typical)

Narrowband zoom:
High-accuracy mode: 2.6:1
High-resolution mode: 9.1:1

Equivalent noise bandwidth
The equivalent noise bandwidth and 1 Hz normalization factor are available for the current RBW filter in the state setup table.

Narrowband zoom:
High-accuracy mode: 0.955% of span
High-resolution mode: 0.375% of span

Video bandwidth
Entered in frequency values which are coupled to the current RBW and are from (1.54 * RBW) to (0.012 * RBW) in seven steps, and off.

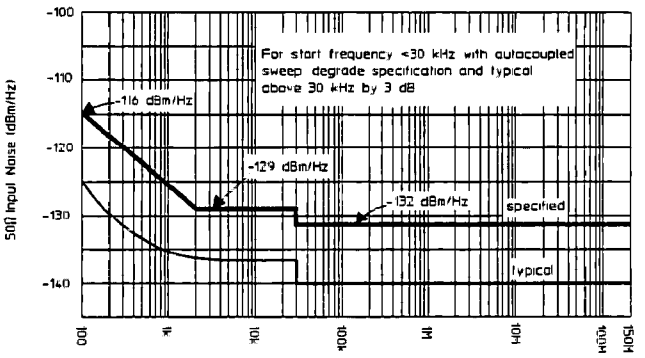
Amplitude Specifications

Dynamic range
Note: Spectrum dynamic range specifications apply with the source off.

A/D overload level > 2 dB (relative to selected range)

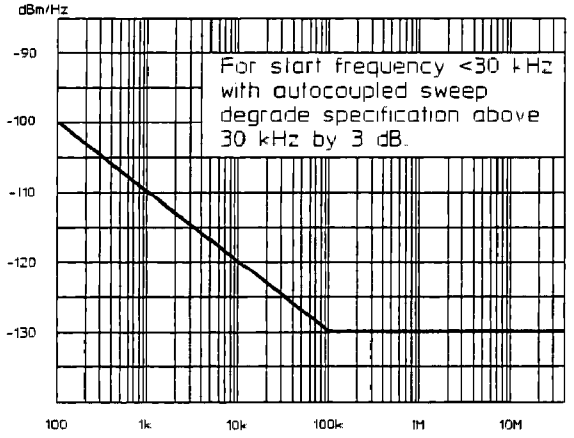
Noise level: (dBm/Hz using the noise marker function)

50Ω Input Noise



Specified for swept spectrum mode, with 50Ω input, range set to -20 dBm and low-distortion mode off. Degrade 10 dB if in low-distortion mode. For 75Ω input with included BNC adapter barrel degrade 2 dB, or with minimum loss pad degrade 6 dB.

1 MΩ Input Noise



Specified for swept spectrum mode with 1 MΩ input, range set to -33 dBV (100 kΩ termination) and low-distortion mode off. Degrade 10 dB if in low-distortion mode.

For narrowband zoom spans > 10 kHz, input noise is degraded by 4 dB.

Note: Equivalent noise bandwidth is narrower than 1 Hz for spans below 150 Hz with the narrowband zoom measurement type, providing additional reduction in noise from that shown. Noise is reduced by 10*Log[1/noise bandwidth] dBc relative to the graph.

Spurious responses

General spurious

Unless specifically mentioned in other spurious specifications, spurious responses are < -70 dBc (< -80 dBc typical) for signal levels equal to input range.

Harmonic distortion†

Harmonic distortion products are for a spectrally pure input signal with total input power level equal to the range and low distortion mode on.

50Ω and 75Ω inputs: < -80 dBc (< -90 dBc typical)
1 MΩ input: < -75 dBc (< -80 dBc typical)

Intermodulation distortion†

Intermodulation distortion products are with respect to two tones 6 dB below range and low-distortion mode on
50 and 75Ω inputs: < -80 dBc (< -90 dBc typical)
1 MΩ input: < -75 dBc (< -80 dBc typical)

† Degrade distortion specification by 10 dB (5 dB for 1 MΩ input) when input frequency is less than 30 kHz. Degrade specification by 10 dB when low-distortion mode is off.

Residual responses

Residual responses are less than -110 dBm on the -20 dBm range. Degrade specification by 10 dB when low-distortion mode is on. Degrade 10 dB for 40 kHz spans in narrowband zoom mode.

Image, multiple, and out-of-band responses: < -70 dBc (< -80 dBc typical) where applied signal level = range.

Local oscillator feedthrough

Local oscillator feedthrough (appears as signal at dc) is >20 dB below range. Degrade specification by 10 dB when low-distortion mode is on.

Amplitude accuracy

Measurement accuracy is determined by the sum of full-scale absolute accuracy and scale fidelity (linearity). For measurements made at full-scale (signal level = range), only full-scale accuracy need be considered. Recalibration due to change in center or manual frequency is not required for the accuracy shown.

Example: To compute the typical cumulative accuracy for a signal of -45 dBm at 100 MHz with 50Ω full-scale range of -20 dBm and manual sweep, sum the typical full-scale absolute accuracy and scale fidelity, i.e., (0.2 dB + 0.02 dB) = 0.22 dB.

Full scale absolute accuracy

(applies over entire 0 ° to 55 °C temperature range)

Full scale absolute accuracy

	50Ω Input [dB]	50Ω Typical [dB]	75Ω Input† [dB]	1 MΩ Input [dB]
10 Hz - 100 Hz	± 2.5	± 1.0	± 2.5	± 2.5
100 Hz - 30 kHz	± 1.0	± 0.5	± 1.0	± 1.25
30 kHz - 300 kHz	± 0.5	± 0.2	± 0.8	± 0.6
300 kHz - 40 MHz	± 0.4	± 0.2	± 0.8	± 0.6
40 MHz - 150 MHz	± 0.5	± 0.2	± 0.8	—

Full-scale absolute accuracy at 300 kHz is ± 0.3 dB (0.1 dB typical) when input level is equal to the range.

† Using either included BNC adapter or optional minimum loss pad.

Accuracy is specified for manual frequency or for sweeps where sweep time is increased by a factor of four. Add ± 0.1 dB for autocoupled sweep times.

Narrowband zoom: Add the following errors to the full-scale absolute accuracy specifications when in narrowband zoom mode. (This compensates for "window flatness" errors that result from windowing during the FFT operation):

High-accuracy mode (flat-top window): ± 0.005 dB
High-resolution mode (Hanning window): +0, -1.5 dB

Scale fidelity

(linearity) maximum cumulative error of log scale:

Level†	Incremental‡	Typical
0 to -30 dB	<0.05 dB	0.02 dB
-30 to -40 dB	<0.1 dB	0.03 dB
-40 to -50 dB	<0.3 dB	0.05 dB
-50 to -60 dB	<0.5 dB	0.10 dB
-60 to -70 dB	<0.7 dB	0.10 dB
-70 to -80 dB	—	0.25 dB
-80 to -90 dB	—	0.25 dB
-90 to -100 dB	—	0.40 dB
-100 to -110 dB	—	0.70 dB
-110 to -120 dB	—	4.00 dB

Specified for frequencies >200 kHz.
† Relative to the specified range.
‡ Incremental deviation must be added to the other reference level accuracy specifications to obtain the total cumulative error.

Automatic calibration

Calibrations, which may be turned off, are periodically performed to compensate for time and temperature drift effects. No recalibration is necessary for changes in frequency parameters.

Sweep Characteristics

Trigger
(characteristic only)
HP-IB, internal free run, or external triggering is available for linear sweep and narrowband zoom. Trigger arming is manual or automatic.

Trigger latency (uncertainty between the trigger input and internal trigger identification):
Zero span and manual sweep: 4 μs (for 17 kHz RBW, increasing by factor of 2 for each lower RBW)
Narrowband zoom: $8 * 2^{40000/span}$ μs
Linear sweep: 20 μs (for 17 kHz RBW, increasing by factor of 2 for each lower RBW)

Trigger delay (HP-IB or external trigger only): 0 ms to the maximum gate length indicated for gated sweep (See the gate length and trigger delay table in the gated sweep characteristics.)

Linear sweep
Measurement speed: (characteristic only)
Sweep rate, oversweep off: $RBW^2/2$ Hz/s
Sweep rate, oversweep on: $4 * (RBW^2/2)$ Hz/s

Note: Analog Gaussian RBW filters are usually swept at $RBW^2/2$ Hz/s (or slower) to limit the amplitude errors due to sweeping to <0.1 dB. The oversweep mode of the HP 3589A provides four times faster sweep time without increased error. To calculate sweep time, compute span/sweep rate.

Narrowband zoom
Measurement speed: >7 measurements/s (for spans ≥ 10 kHz)

Time record length: 400/span (Hz) second

Gated sweep
(with option 1D6) (characteristic only)
Gated sweep is not available in narrowband zoom mode

Gate length and trigger delay:

RBW [Hz]	Gate length minimum [ms]	Gate length maximum [ms]	Edge trigger default delay † [ms]
17000	0.02	131	0.13
9100	0.04	131	0.2
4600	0.08	131	0.38
2300	0.16	131	0.76
1200	0.32	131	1.5
580	0.64	131	3.1
290	1.28	665	6.25
150	2.56	1,311	12.5
73	5.12	2,621	25
36	10.24	5,243	50
18	20.48	10,486	100
9.1	40.96	20,972	200
4.5	81.92	41,861	400
2.3	163.84	83,886	800
1.1	327.68	167,772	1600

† Filter settling time required to achieve accurate noise and amplitude measurements. Delay range is from 0 ms to the maximum gate length indicated (10 μs steps for 17 kHz RBW) Level trigger default delay is approximately 20% larger than the edge trigger default delay

Edge trigger latency (uncertainty between the gate trigger input and internal trigger identification) is 10 μs (for 17 kHz to 580 kHz, increasing by factor of 2 for bandwidths below 580 kHz). Level trigger latency is equal to the minimum gate length indicated.

Network Measurements

Note: All specifications apply from 10 Hz to 150 MHz and include 30 minute warm-up from ambient conditions unless otherwise noted. Typical performance is applicable over ± 5 °C from the temperature during the most recent reference measurement and is not warranted. Supplemental characteristics (identified as characteristic only) are non-warranted functional and feature information.

All network measurement specifications apply when swept network measurement type is selected. Specifications apply to 50Ω to 75Ω only, unless otherwise noted.

Frequency Specification

Frequency span
(characteristic only)

Linear sweep:
Range: 10 Hz to 150 MHz, and zero span
Resolution: 0.1 Hz
Accuracy: Greater of 0.1 Hz or 0.125 % of span
Start/stop frequency 0 Hz to 150 MHz

Log sweep:
Range: 10 Hz to 149.99999 MHz
Resolution: 0.1 Hz
Accuracy: 3%
Start/stop frequency: 10 Hz to 150 MHz

Resolution bandwidth
Range: 1.1 Hz to 17 kHz ± 10%

Bandwidth selectivity
(shape factor or ratio of -60 dB to -3 dB bandwidths)
Manual sweep: < 4.0:1

Amplitude Specifications

Dynamic range
A/D overload level: > 2 dB (relative to the selected range)

Sensitivity
Sensitivity is the dynamic range limitation due to noise level (measured in a 1 Hz bandwidth) and internal crosstalk between the source and receiver: (75Ω with included BNC adapter or optional minimum loss pad)

Impedance	10 Hz - 30 kHz	30 kHz - 40 MHz	40 MHz - 150 MHz
50/75Ω	80 dB	100 dB	100 dB
50/75Ω typical	85 dB	110 dB	110 dB
1 MΩ	75 dB	100 dB	—

General spurious
Unless specifically mentioned in other spurious specifications, spurious responses are < -80 dBc for signal levels equal to range

Residual responses
Residual responses are less than -110 dBm on the -20 dBm range.

Local oscillator feedthrough
Local oscillator feedthrough (appears as signal at dc) is >20 dB below range.

Ratio Amplitude and Phase Specifications

Display range
Amplitude reference level: -1000 to +1000 dB
Amplitude display resolution: 0.001 to 100 dB/div
Amplitude marker resolution: 0.01 dB
Amplitude display units: dB
Phase reference level: -72000 deg to +72000 deg
Phase display resolution: 0.001 deg to 7200 deg/div
Phase marker resolution: 0.01 deg
Phase display units: deg

Accuracy
Dynamic accuracy:

Level†	Accuracy‡		Typical††	
[dB]	[dB]	[deg]	[dB]	[deg]
0 to -5 dB	<0.05	<1.0	0.05	0.2
-5 to -30	<0.10	<1.5	0.10	0.5
-30 to -40	<0.15	<2.0	0.10	1.0
-40 to -50	<0.35	<3.0	0.10	1.0
-50 to -60	<0.55	<4.0	0.15	1.5
-60 to -70	<0.75	<6.0	0.15	2.5
-70 to -80	—	—	0.30	—
-80 to -90	—	—	0.30	—
-90 to -100	—	—	0.45	—
-100 to -110	—	—	0.75	—
-110 to -120	—	—	4.00	—

Specified for frequencies >200 kHz.
† Relative to the specified range.
‡ At stable temperature following a 2 hour warm-up, and within 5 minutes of normalization.
†† Typical within one minute of normalization.

Note: Drift due to changes in ambient temperature is less than ± 0.2 dB/°C and ± 2 °/°C. Time and temperature errors are periodically compensated for, with calibration intervals between 5 and 20 minutes. Calibration will not interrupt the current measurement.

Group Delay Specifications

(Group delay is not available with log sweep)

Group delay reference level: 0 s to ± 10 s
Group delay display resolution: 1 ps/div to 1 s/div
Group delay marker resolution: 0.01 ns
Group delay display units: seconds

Aperture frequency: 0.5% to 16% of span in 2x steps

Group delay accuracy:
Group delay accuracy = dynamic phase accuracy/(360*aperture frequency) ± 1 ns.

Sweep Characteristics

Trigger
(characteristic only)
HP-IB, internal free run, or external triggering is available for linear sweep. Trigger arming is manual or automatic.

Trigger latency (uncertainty between the trigger input and internal trigger identification):
Zero span and manual sweep 16 μs (for 17, 9.1, and 4.6 kHz, increasing by factor of 2 for each lower RBW)
Linear and log sweep: 80 μs (for 17, 9.1, and 4.6 kHz, increasing by factor of 2 for each lower RBW)

Trigger delay (HP-IB or external trigger only): 0 ms to the maximum gate length indicated for gated sweep. (See the gate length and trigger delay table in the gated sweep characteristics.)

Linear sweep
Sweep time is uncoupled from the span and resolution bandwidth.

Log sweep
Log sweep uses a linear approximation to perform a log frequency sweep. Resolution bandwidths are selected automatically or manually

Manual sweep
Measurements of data between display points use reference data that is the interpolated reference value obtained from the two adjacent display points. Display points (N) are at frequencies = start frequency + span/400 × N.

Gated sweep
(with option 1D6)(characteristic only)
Gating is available only with linear frequency sweep or manual frequency selected.

Gate length and trigger delay:

RBW [Hz]	Gate length minimum [ms]	Gate length maximum [ms]	Edge trigger default delay † [ms]
17000	0.08	131	0.13
9100	0.08	131	0.2
4600	0.08	131	0.38
2300	0.16	131	0.76
1200	0.32	131	1.5
580	0.64	131	3.1
290	1.28	665	6.25
150	2.56	1,311	12.5
73	5.12	2,621	25
36	10.24	5,243	50
18	20.48	10,486	100
9.1	40.96	20,972	200
4.5	81.92	41,861	400
2.3	163.84	83,886	800
1.1	327.68	167,772	1600

† Filter settling time required to achieve accurate noise and amplitude measurements. Delay range is from 0 ms to the maximum gate length indicated. Level trigger default delay is approximately 20% larger than the edge trigger default delay.

Edge and level trigger latency (uncertainty between the gate trigger input and internal trigger identification) is equal to the minimum gate length indicated

General Characteristics

Note: All specifications apply from 10 Hz to 150 MHz and include 30 minute warm-up from ambient conditions unless otherwise noted. Supplemental characteristics (identified as characteristic only) are non-warranted functional and feature information.

Safety and environmental
Safety standards: CSA certified for Electronic Test and Measurement Equipment per CSA 22.2, no. 231

This product is designed for compliance to: UL1244, 2nd Edition and IEC348, 2nd Edition, 1978.

EMI/RFI standards: FTZ527 - Germany

Acoustics: LpA <70 dB

Temperature:
Operating: 5 ° to 50 °C
Storage (no disk in drive): -20 ° to 60 °C

Humidity, non-condensing:
Operating: 8% to 80% at 30 °C
Storage (no disk in drive): 5% to 95%

Altitude:
Operating: 2150 m (7,000 ft)
Storage: 4570 m (15,000 ft)

Calibration Interval: 1 year

Warm-up Time: 30 minutes

Power Requirements:
115 VAC operation: 90 - 132 Vrms, 47 - 440 Hz
230 VAC operation: 198 - 264 Vrms, 47 - 66 Hz
Maximum power dissipation: 450 VA

Weight:
Net: 28 kg (61 lbs)
Shipping: 38 kg (81 lbs)

Dimensions:
Height: 222 mm (8.75 in)
Width: 425.5 mm (16.75 in)
Depth: 630 mm (24.8 in)

Trigger/gate
(characteristic only)
Trigger/gate input:
Triggers on positive or negative TTL transition or contact closure or release from ground. For gated sweep (option 1D6) polarity is selectable for TTL edge or level

Trigger/gate output: Produces a negative TTL transition at the internal trigger identification. For gated sweep (option 1D6) produces a high TTL level during the active gate window. Fanout is 3 TTL LS loads.

Reference
(characteristic only)
Reference output: 10 MHz at +3 dBm (nominal) 50Ω

External reference input: 1 MHz, 2 MHz, 5 MHz, or 10 MHz between -5 dBm and +10 dBm into 50Ω (nominal)

High stability reference oven output (option 1D5): 10 MHz at +10 dBm into 50Ω

Display
(characteristic only)
Number of horizontal axis points: 401
Formats: single, upper/lower, front/back, setup state
Display blanking: annotation, full

Frequency axis mirror and frequency and amplitude annotation correction for use with external down-converters and receivers.

Trace math
(characteristic only)
Operators: +, -, *, /, SQRT, CONJ
Operands: input, network function, data registers, constants, other functions, SQRT(NBW), $j\omega$

Trace math can be used to correct the data on each measurement. Uses include user units correction and normalizations. Noise data is automatically referred to a 1 Hz bandwidth by displaying a function defined as SPECT/SQRT(NBW) or to any desired bandwidth by displaying a function defined as (SPECT/SQRT(NBW))*SQRT(K1), where K1 is set to the desired bandwidth. SQRT(NBW) is a trace math argument that automatically uses the equivalent noise bandwidth of the current resolution bandwidth filter.

Corrected data for use with divider probes can be displayed by displaying a function defined as SPECT*K1, where K1 is set to the probe division ratio.

External keyboard
(characteristic only)
Compatible with PC-style 101 key keyboard model number HP C1405A and HP Keyboard cable part number 5081-2249 (DIN connector).

Interfaces
Active probe power: +15 Vdc, -12.6 Vdc; 150 mA maximum, suitable for HP probes

HP-IB:
HP-IB implementation of IEEE Std 488.1 and 488.2
SH1, AH1, T6, TE0, L4, LE0, SR1, RL1, PP0, DC1, DT1, C1, C2, C3, C12, E2

Benchmarks (characteristic only)
Binary trace output: 120 ms/trace typical

Peripherals
HP-IB graphics printers (raster output only)
HP-IB plotters using HP-GL

Memory and data storage
(characteristic only)
Standard internal memory:
Non-volatile RAM: 64 Kbyte
Volatile RAM 1 Mbyte (partitionable between HP Instrument BASIC program space and RAM disk)

Optional memory:
Volatile RAM Option 1C1: additional 2 Mbyte RAM

Disk drive: (Only internal disk drive supported).
The HP 3589A's internal disk drive can format only double-sided, double-density disks (720 Kbyte). It can also read and write single-sided disks that were formatted in a double-sided drive It does not read, write or format high density (1.44 Mbyte) disks.

Benchmarks (characteristic only):
Trace memory size: 2850 bytes
State memory size: 3100 bytes

Standard data format utilities
(characteristic only)
Included on two 3 1/2-inch high-density (1.44 Mbyte) and two 5 1/4-inch high-density (1.2 Mbyte) floppy disks. The utilities run in MS-DOS 2.1 or greater on an IBM PC (AT or higher) or compatible The utilities include LIF to DOS format conversions, conversion to standard data format (SDF), displaying data and instrument state information, and utilities for conversion to PC-MATLAB, MATRIXx, data set 58, and ASCII format.

HP 35689A/B Specifications

Note: All specifications apply from 100 kHz to 150 MHz and include 30 minute warm-up from ambient conditions unless otherwise noted. Typical performance is applicable over ± 5 °C from the temperature during the most recent reference measurement and is not warranted. All specifications apply without bias signals. Degrees are specified as deviation from linear phase. All ratio measurements require a valid reference measurement be taken.

Frequency range: 100 kHz to 150 MHz

Test port impedance:
HP 35689A: 50 Ω
HP 35689B: 75 Ω

Directivity: >40 dB

Frequency response:
Transmission (S21, S12): ± 1 dB, ± 5 deg
Reflection (S11, S22): ± 1 dB, ± 5 deg

Port match:
Return loss input/output port: > 20 dB
Equivalent test port (1, 2) match:
HP 35689A: 26 dB
HP 35689B: 24 dB

Reference path match:
Magnitude. typically ± 0.5 dB
Phase: typically ± 5 deg

Test port isolation: > 90 dB

Insertion loss:
RF input to test port 1 or 2:
HP 35689A: typically 13 dB
HP 35689B: typically 19 dB
RF input to output:
HP 35689A: typically 19 dB
HP 35689B: typically 31 dB

Test port reciprocity:
Transmission (S21, S12): typically ± 0.5 dB, ± 5 deg
Reflection (S11, S22): typically ± 0.5 dB, ± 5 deg

RF input maximum operating level: +25 dBm or 30 Vdc

RF input damage level: +27 dBm or ± 30 Vdc

Port 1 or 2 damage level: +27 dBm or ± 30 Vdc

DC bias range:
Typically ± 30 Vdc and ± 20 mA with some degradation of RF specifications; 200 mA damage level.

Spectrum port:
The spectrum port is provided as a convenient input when the HP 3589A is connected to the HP 35689A/B. For specified HP 3589A measurement performance, direct connection to the HP 3589A input connector is required.

Spectrum port damage level:
HP 35689A: See HP 3589A specifications
HP 35689B: Add 6 dB to HP 3589A specifications

Spectrum port insertion loss:
HP 35689A: <0.5 dB typical
HP 35689B: 5 7 dB typical (due to included minimum loss pad)

Programming: The HP 35689A/B are completely controlled through the HP 3589A using the HP 3589A interconnecting cable.

Power:
110/120 VAC operation:
90 - 132 Vrms, 47 - 440 Hz
220/240 VAC operation: 198 - 264 Vrms, 47 - 66 Hz
Maximum power dissipation: 70 VA

Weight:
Net: 7.8 kg (17 lb)
Shipping: 11.5 kg (25 lb)

Dimensions:
Height: 90 mm (3.5 in)
Width: 426 mm (16 75 in)
Depth: 584 mm (22.75 in)

Accessories included:
2 ea 190 mm (7.5 in) 50Ω cables with Type-N male connectors for connection to the HP 3589A (HP P/N 8120-4387)

1 ea Test set interconnect cable to HP 3589A
(HP P/N 35689-61612)

1 ea power cord

2

Preparing the HP 3589A and HP 35689A/B for Use

How to Use This Chapter

This chapter contains power requirements and operating environment information needed to install the HP 3589A Spectrum/Network Analyzer and the HP 35689A/B S-Parameter Test Set. Also included in this chapter are instructions for connecting the test set and keyboard to the analyzer, cleaning the screen, and information on storage and shipment.

Incoming Inspection

The HP 3589A Spectrum/Network Analyzer and HP 35689A/B S-Parameter Test Set were carefully inspected both mechanically and electrically before shipment. The instrument should be free of marks or scratches and, it should meet its published specifications upon receipt. For a list of the accessories shiped with each instrument see "Accessories" in chapter 1.

Inspect the instrument for physical damage incurred in transit. If the instrument was damaged in transit, save all packing materials, file a claim with the carrier, and call your Hewlett-Packard sales and service office.

Warning

If the instrument is mechanically damaged, the integrity of the protective earth ground may be interrupted. Do not connect the instrument to power if it is damaged.

Incoming Tests

Finish incoming inspection by testing the electrical performance of the instrument using the operation verification or performance tests in chapter 3, "Verifying Specifications." The performance tests verify that the instrument meets its performance specifications. The operation verification tests are a subset of the performance tests and verify the basic operating integrity of the instrument.

HP 3589A Power Requirements

The HP 3589A Spectrum/Network Analyzer can operate from a single-phase ac power source supplying voltages as shown in table 2-1. With all options installed, the analyzer's power consumption is less than 450 VA.

The line-voltage selector switch is set at the factory to match the most commonly used line voltage of the country of destination; the appropriate fuse is also installed. To check or change either the line-voltage selector switch or the fuse, see figure 2-1, table 2-1, and the following procedures.

Caution

Before applying ac line power to the HP 3589A Spectrum/Network Analyzer, ensure that the line-voltage selector switch (on the rear panel) is set for the proper line voltage and the correct line fuse is installed in the fuse holder.

Warning

Only a qualified service person, aware of the hazards involved, should measure the line voltage.

Table 2-1. Analyzer Line Voltage and Fuse Selection

AC Line Voltage		Selector Switch	Fuse	
Range	Frequency		HP Part Number	Type
90-132 Vrms	47-440	115	2110-0056	6A 250V Fast Acting
198-264 Vrms	47-66	230	2110-0003	3A 250V Fast Acting

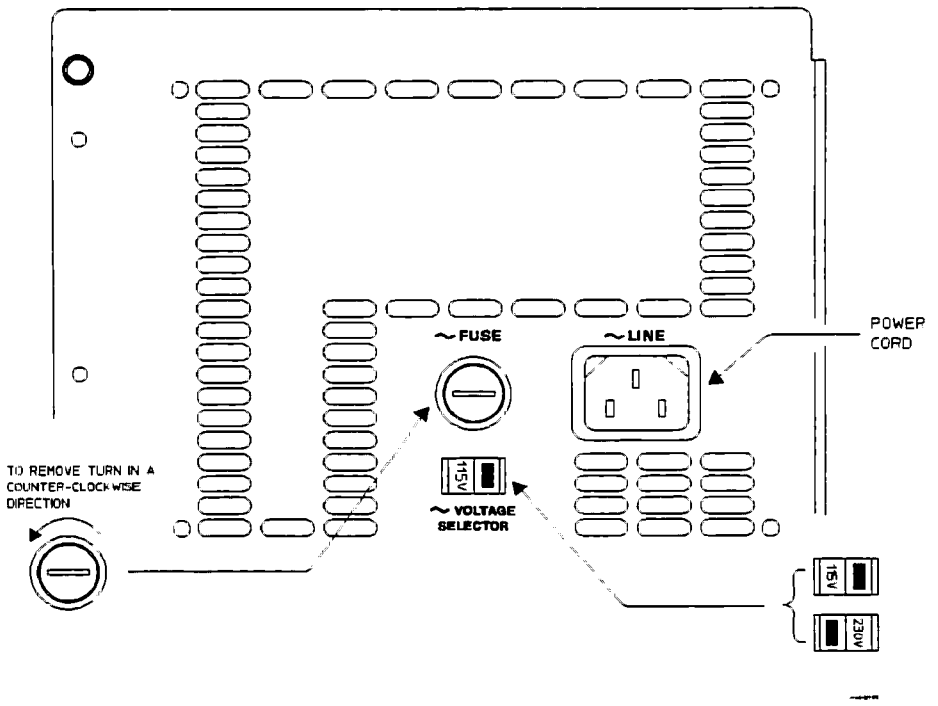


Figure 2-1. Analyzer Voltage Selection and Fuse Replacement

To change the line voltage selector switch:

1. Unplug the power cord from the analyzer.
2. Slide the line voltage selector switch (see figure 2-1) to the proper voltage (see table 2-1) and install the proper fuse for the voltage selected.

To change the fuse:

1. Unplug the power cord from the analyzer.
2. Using a coin or screw driver, turn the fuse holder cap counter-clockwise and remove when the fuse cap is free from the housing (see figure 2-1).
3. Pull the fuse from the fuse holder cap.
4. To reinstall, select the proper fuse (see table 2-1) and place in the fuse holder cap. Place the fuse holder cap in the housing and turn clockwise while pressing in.

HP 35689A/B Power Requirements

The HP 35689A/B S-Parameter Test Set can operate from a single-phase ac power source supplying voltages as shown in table 2-2. The test set's power consumption is less than 70 VA.

The line-voltage selector switch is set at the factory to match the most commonly used line voltage of the country of destination; the appropriate fuse is also installed. To check or change either the line-voltage selector switch or the fuse, see figure 2-2, table 2-2, and the following procedures.

Caution

Before applying ac line power to the HP 35689A/B S-Parameter Test Set, ensure that the line-voltage selector switch (on the rear panel) is set for the proper line voltage and the correct line fuse is installed in the fuse holder.

Warning

Only a qualified service person, aware of the hazards involved, should measure the line voltage.

Table 2-2. Test Set Line Voltage and Fuse Selection

AC Line Voltage		Selector Switch	Fuse	
Range	Frequency		HP Part Number	Type
90-132 Vrms	47-440	100/120	2110-0001	1A (normal blow) 250 VAC
198-264 Vrms	47-66	220/240	2110-0012	500 mA (normal blow) 250 VAC

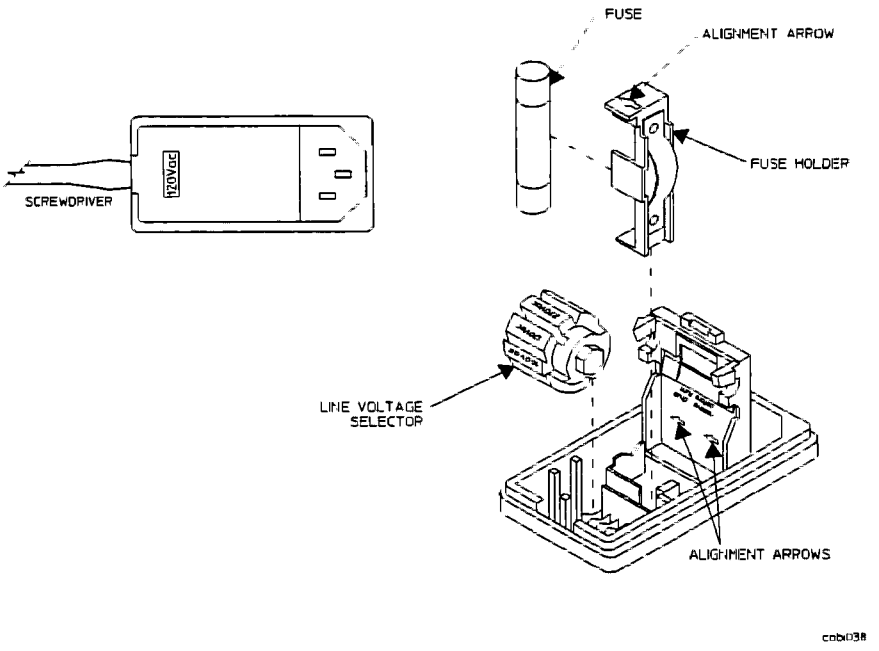


Figure 2-2. Test Set Voltage Selection and Fuse Replacement

To change the fuse or line voltage selector switch:

1. Unplug the power cord from the test set.
2. Using a small screw driver, pry open the power selector cover (see figure 2-2).
3. To change the fuse:
   a. Pull the white fuse holder out of the power selector and remove the fuse from the fuse holder.
   b. To reinstall, select the proper fuse (see table 2-2), and place in the fuse holder. Align the white arrow on top of the fuse holder with the white arrow on the power selector cover. All three arrows should point in the same direction. Install the fuse holder in the top slot. Push the fuse holder into the power selector.
4. To change the line voltage selector switch:
   a. Remove the cylindrical line voltage selector.

Caution Do not rotate the cylindrical line voltage selector without first removing from the power selector. The selector will be damaged if it is rotated while installed.

b. Position the cylindrical line voltage selector so the required voltage will be facing out of the power selector, then reinstall.

5. Close the power selector by pushing firmly on the black cover.
6. Check that the correct line voltage appears through the power selector cover.

Power Cable and Grounding Requirements

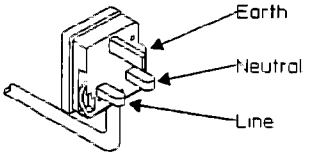
On the analyzer's HP-IB connector, pin 12 and pins 18 through 24 are tied to earth ground and the HP-IB cable shield. The instrument's frame, chassis, covers, all exposed metal surfaces including the connectors' outer shell are connected to protective earth ground.

Warning  **DO NOT interrupt the protective earth ground or "float" the instrument. This action could expose the operator to potentially hazardous voltages.**

The instrument is equipped with a three-conductor power cord that grounds the instrument when plugged into an appropriate receptacle. The type of power cable plug shipped with each instrument depends on the country of destination. See figure 2-3 for the available power cables and plug configurations.

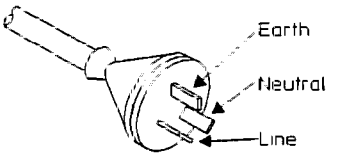
Warning  **The power cable plug must be inserted into an outlet provided with a protective earth terminal. Defeating the protection of the grounded instrument cabinet can subject the operator to lethal voltages.**

United Kingdom
Option 900



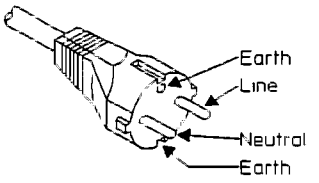
PLUG* BS 1363A
CABLE* HP 8120-1351
220V-5A
OPERATION

Australia/New Zealand
Option 901



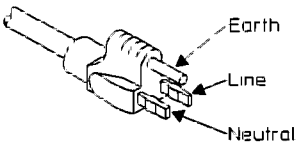
PLUG* NZSS 198/AS C112
CABLE* HP 8120-1369
220V-6A
OPERATION

Continental Europe
Option 902



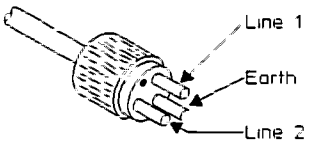
PLUG* CEE7-V11
CABLE* HP 8120-1689
220V-6A
OPERATION

North America
Option 903



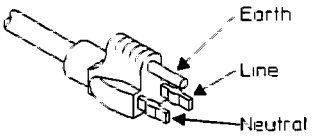
PLUG* NEMA 5-15P
CABLE* HP 8120-1378
125V-10A**
OPERATION

North America
Option 904



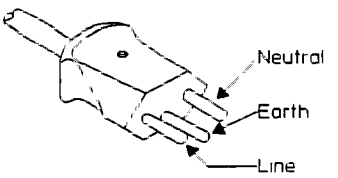
PLUG* NEMA-G-15P
CABLE* HP 8120-0698
250V-5A**
OPERATION

Japan
Option 918



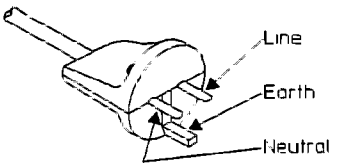
PLUG* MITI 41-9692
CABLE* HP 8120-4753
125V-12A
OPERATION

Switzerland
Option 906



PLUG* SEV 1011.1959-24507
TYPE 12
CABLE* HP 8120-2104
220V-6A
OPERATION

Denmark
Option 912



PLUG* DHCP 107
CABLE* HP 8120-2956
220V-6A
OPERATION

Figure 2-3. Power Cables

Operating Environment

The operating and storage environment specifications for the instrument are listed in chapter 1, "Introducing the HP 3589A and HP 35689A/B."

Warning 

To prevent potential fire or shock hazard, do not expose the instrument to rain or other excessive moisture.

Protect the instrument from moisture and temperatures or temperature changes that cause condensation within the instrument.

Caution 

Use of the HP 3589A Spectrum/Network Analyzer in an environment containing dirt, dust, or corrosive substances will drastically reduce the life of the disk drive and the flexible disks. The disks should be stored in a dry, static-free environment.

Instrument Cooling

Cooling air enters the HP 3589A Spectrum/Network Analyzer through both sides and exhausts through the rear panel. Install the analyzer to allow free circulation of cooling air.

HP-IB System Interface Connections

The HP 3589A Spectrum/Network Analyzer is compatible with the Hewlett-Packard Interface Bus (HP-IB). The HP-IB is Hewlett-Packard's implementation of IEEE Standard 488.2. The analyzer is connected to the HP-IB by connecting an HP-IB interface cable to the connector located on the rear panel. Total allowable transmission path length is 2 meters times the number of devices or 20 meters, whichever is less. Operating distances can be extended using an HP-IB Extender.

For additional HP-IB programming information, see the *HP 3589A HP-IB Programmer's Reference*.

Caution

The analyzer contains metric threaded HP-IB cable mounting studs as opposed to English threads. Use only metric threaded HP-IB cable lockscrews to secure the cable to the analyzer. Metric threaded fasteners are black, while English threaded fasteners are silver.

Installation

The HP 3589A Spectrum/Network Analyzer and HP 35689A/B S-Parameter Test Set are shipped with plastic feet in place, ready for use as portable bench instruments. The plastic feet are shaped to make full-width modular instruments self-align when they are stacked. To install the analyzer in an equipment cabinet, follow the instructions shipped with its rack mount kit, HP part number 35660-86010. To install the test set in an equipment cabinet, follow the instructions shipped with its rack mount kit, HP part number 5062-3975.

Connecting an External Frequency Reference

The analyzer may be connected to an external 1, 2, 5, or 10 MHz frequency reference. The frequency reference's amplitude must be greater than –5 dBm and less than +10 dBm. The analyzer's frequency reference input is labeled EXT REF IN and is located on the analyzer's rear panel. If EXT REF IN is not connected to a frequency reference, the analyzer uses its internal 10 MHz reference. To connect an external frequency reference to the analyzer, connect the frequency reference to EXT REF IN using a BNC cable.

Connecting the Optional High Stability Frequency Reference

Analyzers with the optional high stability frequency reference have a BNC connector on the rear panel labeled OVEN REF OUT. If OVEN REF OUT is not connected to EXT REF IN, the analyzer uses its internal 10 MHz reference. To connect the high stability frequency reference to the analyzer, connect OVEN REF OUT to EXT REF IN using the supplied coax BNC-to-coax BNC connector (HP part number 1250-1499). See figure 2-4.

Note

The high stability frequency reference requires approximately fifteen minutes to warm up. During this warm-up period, the output of the high stability frequency reference is turned off and the analyzer uses its internal 10 MHz reference.

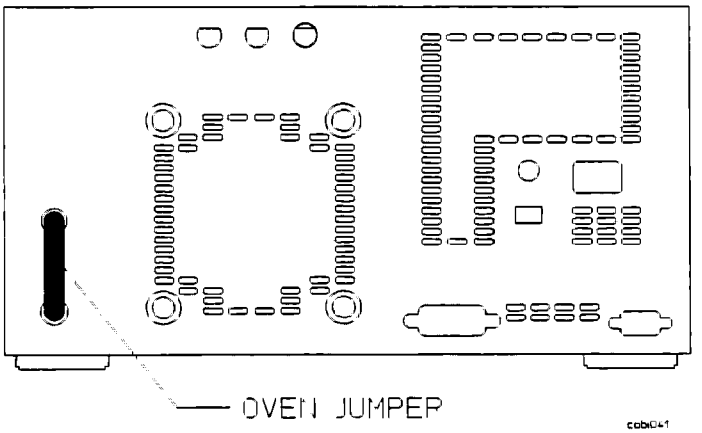


Figure 2-4. Connecting the High Stability Frequency Reference

Connecting the Optional Keyboard

To connect the PC Style Keyboard to the HP 3589A Spectrum/Network Analyzer do the following:

1. Set the analyzer's power switch to STANDBY (⏻).
2. Connect the round plug on the keyboard cable to the KEYBOARD connector on the analyzer's front panel. Make sure to align the plug with the connector pins (see figure 2-5).
3. Connect the other end of the keyboard cable to the keyboard.

Caution

Do not connect or disconnect the keyboard cable with the line power turned ON (I). Connecting or disconnecting the keyboard while power is applied may damage the keyboard or the analyzer.

In addition to the U.S. English keyboard, the HP 3589A Spectrum/Network Analyzer supports U.K. English, German, French, Italian, Spanish, and Swedish. Use only the Hewlett-Packard approved keyboard for this product. Hewlett-Packard does not warrant damage or performance loss caused by a non-approved keyboard. See table 1-3 for part numbers of approved Hewlett-Packard keyboards.

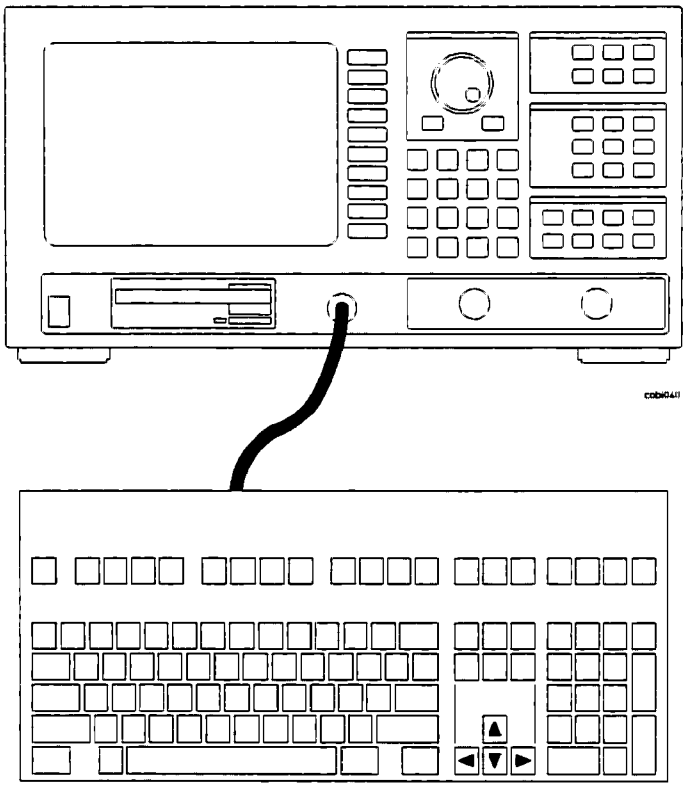


Figure 2-5. Connecting the Keyboard

4. To configure your analyzer for a keyboard other than U.S. English, press [**Special Fctn**], [NON-VOL SETUP], [KEYBOARD SETUP]. Then press the appropriate softkey to select the language.

Note

Configuring your analyzer to use a different keyboard only ensures that the analyzer recognizes the proper keys for that particular keyboard. Configuring your analyzer to use another keyboard *does not* localize the on-screen annotation or the analyzer's online HELP facility.

The keyboard remains active *even when the analyzer is not in alpha entry mode*. This means that you can operate the analyzer using the external keyboard rather than the front panel. Pressing the appropriate keyboard key does the same thing as pressing a hardkey or a softkey on the analyzer's front panel.

Connecting the S-Parameter Test Set

To connect the HP 35689A/B S-Parameter Test Set to the HP 3589A Spectrum/Network Analyzer do the following:

1. Set the power switch on both instruments to STANDBY (⏻).
2. Place the analyzer on top of the test set (see figure 2-6).
3. Using the interconnect cable, connect PORT 1 (analyzer's rear panel) to 3589 INTERCONNECT (test set's rear panel).

Caution

Do not connect or disconnect the interconnect cable with the line power turned ON (I). Connecting or disconnecting the analyzer from the test set while power is applied may damage the analyzer or test set.

---

4. Using one of the RF connecting cables, connect OUTPUT (test set's front panel) to INPUT (analyzer's front panel).
5. Using the other RF connecting cable, connect INPUT (test set's front panel) to SOURCE (analyzer's front panel).

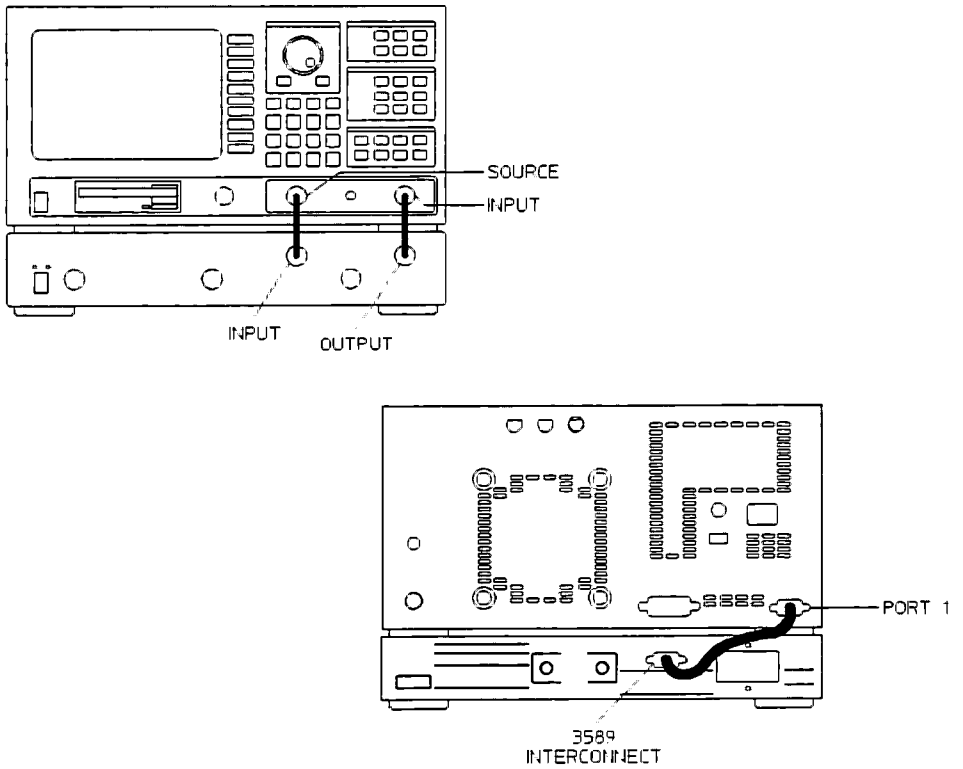


Figure 2-6. S-Parameter Test Set Connections

Turning the Instrument On

First, apply proper line power to the instrument, then press the rocker-switch in the lower left-hand corner of the instrument to ON (I). The analyzer requires about 35 seconds to test memory and self-calibrate.

For measurement specific information or other operating information, see the *HP 3589A Operator's Guide* or other appropriate manual. See the documentation map included with the analyzer for information on which document contains the information you need.

Screen (CRT) Cleaning

The HP 3589A Spectrum/Network Analyzer's screen is covered with a plastic diffuser screen (this is not removable by the operator). Under normal operating conditions, the only cleaning required will be an occasional dusting. However, if a foreign material adheres itself to the screen, set the power switch to STANDBY (⏻), remove the power cord, dampen a soft, lint-free cloth with a mild detergent mixed in water, and carefully wipe the screen.

Caution

Do not apply any water mixture directly to the screen or allow moisture to go behind the front panel. Moisture behind the front panel will severely damage the instrument.

To prevent damage to the screen, do not use cleaning solutions other than the above.

Need Assistance?

If you need assistance, contact your nearest Hewlett-Packard Sales and Service Office listed in the HP Catalog, or contact your nearest regional office listed at the back of this guide. If you are contacting Hewlett-Packard about a problem with your instrument, please provide the following information:

- Model number:
- Serial number:†
- Options:
- Firmware version:‡
- Date the problem was first encountered:
- Circumstances in which the problem was encountered:
- Can you reproduce the problem?
- What effect does this problem have on you?

† Press [**Special Fctn**], [NON-VOL SETUP], [SERIAL NUMBER] to display this information for the HP 3589A Spectrum/Network Analyzer.

‡ Press [**Special Fctn**], [NON-VOL SETUP], [VERSION] to display this information for the HP 3589A Spectrum/Network Analyzer

Storage and Shipment

Storage

Store the instrument in a clean, dry, and static free environment. For other requirements, see environmental specifications in chapter 1, "Introducing the HP 3589A and HP 35689A/B."

Shipment

Caution

When transporting the HP 3589A Spectrum/Network Analyzer, insert the plastic disk protector, part number HP 5061-2819, into the disk drive to prevent damage.

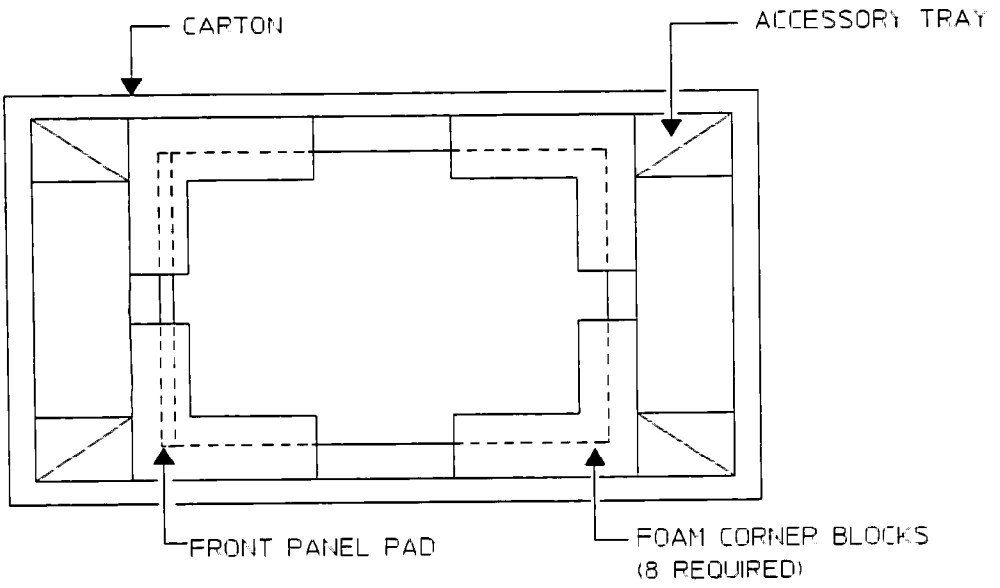


Figure 2-7. Repacking for Shipment

- Containers and materials identical to those used in factory packaging are available through Hewlett-Packard offices, see figure 2-7. If the instrument is being returned to Hewlett-Packard for service, attach a tag describing the type of service required, the return address, model number, and full serial number. Also, mark the container FRAGILE to ensure careful handling. In any correspondence, refer to the instrument by model number and full serial number.

- If it is necessary to package the instrument in a container other than original packaging, observe the following (use of other packaging is not recommended):

  - Protect the front panel with cardboard and wrap the instrument in heavy paper or anti-static plastic.

  - Use a double-wall carton made of at least 350-pound test material and cushion the instrument to prevent damage.

  - Identify the shipment as above and mark FRAGILE.

Caution

Do not use styrene pellets in any shape as packing material for the instrument. The pellets do not adequately cushion the instrument and do not prevent the instrument from shifting in the carton. In addition, the pellets create static electricity that can damage electronic components.

3

Verifying Specifications

How to Use This Chapter

This chapter tells you how to use the *HP 3589A Semiautomated Performance Test Disk* and the *HP 35689A/B Semiautomated Performance Test Disk.* These performance test disks contain programs that semiautomate the operation verification tests and performance tests for the HP 3589A Spectrum/Network Analyzer and the HP 35689A/B S-Parameter Test Set.

First review this chapter, then follow the directions in "Testing the HP 3589A" (starting on page 3-8) or "Testing the HP 35689A/B" (starting on page 3-45).

Safety Considerations

Although the HP 3589A Spectrum/Network Analyzer and HP 35689A/B S-Parameter Test Set are designed in accordance with international safety standards, this manual contains information, cautions, and warnings that must be followed to ensure safe operation and to keep the instrument in safe condition. The operation verification and performance test procedures must be performed by trained service personnel who are aware of the hazards involved (such as fire and electrical shock).

Warning

Any interruption of the protective (grounding) conductor inside or outside the instrument, or disconnection of the protective earth terminal can expose operators to potentially dangerous voltages.

Under no circumstances should an operator remove any covers, screws, shields or in any other way access the interior of the HP 3589A Spectrum/Network Analyzer or HP 35689A/B S-Parameter Test Set. There are no operator controls inside the instrument.

Overview

The *HP 3589A Semiautomated Performance Test Disk* contains a program (ITM_3589A) and four procedure files (OP_VERIFY, ALT_OPVER, PERFORMAN, and ALT_PERF) that are used to verify the performance of the HP 3589A Spectrum/Network Analyzer. ITM_3589A is the test manager program. OP_VERIFY and ALT_OPVER are the operation verification procedure files. PERFORMAN and ALT_PERF are the performance test procedure files. OP_VERIFY and PERFORMAN require a milliwatt power meter to do the amplitude accuracy and flatness test. ALT_OPVER and ALT_PERF are the alternate procedure files and do not require a milliwatt power meter.

The *HP 35689A/B Semiautomated Performance Test Disk* contains a program (ITM_35689) and four procedure files (A_OPVER, B_OPVER, A_PERF, and B_PERF) that are used to verify the performance of the HP 35689A/B S-Parameter Test Set. ITM_35689 is the test manager program. A_OPVER is the operation verification procedure file for the HP 35689A, and B_OPVER is the operation verification procedure file for the HP 35689B. A_PERF is the performance test procedure file for the HP 35689A, and B_PERF is the performance test procedure file for the HP 35689B.

The procedure files contain an ordered list of tests, and each test contains one or more measurements. Since the program reads the procedure files, the disk must remain in the disk drive during testing.

There are two types of keys on the HP 3589A Spectrum/Network Analyzer — hardkeys and softkeys.

- Hardkeys are front-panel buttons whose functions are always the same. Hardkeys have a label printed directly on the key itself. Throughout this guide, they are printed like this: [**Hardkey**]

- Softkeys are keys whose functions change with the analyzer's current menu selection. A softkey's function is indicated by a video label to the left of the key (on the edge of the analyzer's screen). Throughout this guide, softkeys are printed like this: [SOFTKEY]

- Some softkeys toggle through different settings. Toggle softkeys have a highlighted word in their label that changes with each press of the softkey. Throughout this guide, toggle softkeys are depicted as they appear after you press the softkey. For example, [AUTO CAL **ON** OFF] means to press [AUTO CAL ON OFF] until the word ON is highlighted.

If you do not have a keyboard connected to the analyzer, use the numeric key pad and the alpha keys when the program prompts you to type in information. See the analyzer's help text for a description of the alpha keys.

If a test fails, contact your local Hewlett-Packard sales and service office or have a qualified service technician see chapter 4, "Troubleshooting the HP 3589A and HP 35689A/B," in the *HP 3589A Service Guide.*

Features of the Program

- The program can automatically create a printout similar to the test records at the back of this chapter.
- The program can beep when equipment connections need to be changed.
- The program can start the test sequence at any test in the operation verification or performance test list.
- The program can stop after each measurement or alternatively, only if a failure occurs.
- The program can be run in manual mode.

Test Duration

For the HP 3589A Spectrum/Network Analyzer, the operation verification tests require approximately 1 hour to complete and the performance tests require approximately 3 hours to complete in semiautomated mode.

For the HP 35689A/B S-Parameter Test Set, the operation verification tests require approximately 45 minutes to complete and the performance tests require approximately 1 hour to complete in semiautomated mode.

Caution

Before applying line power to the instrument or testing its electrical performance, see chapter 2, "Preparing the HP 3589A and HP 35689A/B for Use."

Calibration Cycle

To verify that the HP 3589A Spectrum/Network Analyzer and HP 35689A/B S-Parameter Test Set are meeting their published specifications, do the performance tests every 12 months.

Recommended Test Equipment

The equipment needed for operation verification and performance tests is listed in table 1-5, 1-6 and 1-7. Other equipment may be substituted for the recommended model if it meets or exceeds the listed critical specifications.

Also, if you want the test record to be automatically printed, you need an HP-IB printer. If you do not have an HP-IB printer you must record the results of each test in the test records located near the end of this chapter. These test records may be reproduced without written permission of Hewlett-Packard.

Note

If you want the printer to automatically leave top and bottom margins on every page, enable perforation skip mode (see your printer's manual for directions).

Program Controlled Test Equipment

This program automatically controls the following instruments using HP-IB commands. If you use a test instrument other than those shown here, the program prompts you to set the instrument state during testing.

Table 3-1. Program Controlled Test Equipment

Test Equipment	Recommended Model
Synthesizer	HP 3326A HP 3325A (alternate) HP 3325B (alternate)
Synthesizer/Level Generator	HP 3335A
Digital Multimeter	HP 3458A
Synthesized Signal Generator	HP 8663A HP 8662A (alternate)
Spectrum Analyzer	HP 8568B HP 8568A (alternate)
Power Meter	HP 438A HP 436A (alternate)

Measurement Uncertainty

A table starting on page 3-72 lists the measurement uncertainty and ratio for each performance test using the recommended test equipment. The ratios listed for the recommended test equipment meet the requirements of U.S. MIL-STD-45662A. The table also provides a place to record the measurement uncertainty and ratio for each performance test using equipment other than the recommended test equipment. The table may be reproduced without written permission of Hewlett-Packard.

Operation Verification and Performance Tests

The operation verification tests give a high confidence level (>90%) that the instrument is operating properly and within specifications. The operation verification tests are a subset of the performance tests. The operation verification tests should be used for incoming and after-repair inspections. The performance tests provide the highest level of confidence and are used to verify that the instrument conforms to its published specifications. Some repairs require a performance test to be done after the repair (see chapter 6, "Replacing Assemblies" in the *HP 3589A and HP 35689A/B Service Guide* for this information). The following table lists all the tests and shows which tests are included in each semiautomated procedure file.

Table 3-2. Tests Used in Semiautomated Procedure Files

HP 3589A Tests	PERFORMAN	ALT_PERF	OP_VERIFY	ALT_OPVER
Local Oscillator Feedthrough	YES	YES	YES	YES
Phase Noise	YES	YES	YES	YES
Residual Responses	YES	YES	YES	YES
Noise Level	YES	YES	YES	YES
Frequency Accuracy	YES	YES	YES	YES
Spurious Responses	YES	YES	YES	YES
Image Responses	YES	YES	YES	YES
Input Harmonic Distortion	YES	YES	YES	YES
Intermodulation Distortion	YES	YES	no	no
Source Response	YES	no	YES	no
Amplitude Accuracy and Flatness	YES	no	YES	no
Alt_Amp Accuracy and Flatness	no	YES	no	YES
Reference Level Accuracy	YES	YES	YES	YES
Dynamic Accuracy	YES	YES	no	no
Source Dynamic Accuracy	YES	YES	YES	YES
Input Return Loss	YES	YES	no	no
Source Return Loss	YES	YES	no	no
Source Harmonic Distortion	YES	YES	YES	YES
Source Spurious Responses	YES	YES	YES	YES
Source Noise	YES	YES	YES	YES
HP 35689A/B Tests	**A_PERF**	**B_PERF**	**A_OPVER**	**B_OPVER**
Directivity and Source Match	YES	YES	YES	YES
Reflection	YES	YES	YES	YES
Transmission	YES	YES	YES	YES
Isolation	YES	YES	no	no
Return Loss	YES	YES	no	no

Specifications and Performance Tests

The following tables list specifications and the performance test or tests that verify each specification.

Table 3-3. HP 3589A Specifications and Performance Tests

Specification	Performance Test
General Specifications	
Frequency Specifications	
Frequency Accuracy	Frequency Accuracy
Stability	Phase Noise
Amplitude Specifications	
Input port	Input Return Loss
Source Specifications	
Amplitude specifications	Source Dynamic Accuracy
	Source Response
	Source Harmonic Distortion
	Source Spurious Responses
	Source Noise
	Source Return Loss
Spectrum Measurements	
Amplitude Specifications	
Dynamic range	Noise Level
Spurious responses	
General spurious	Spurious Responses
Harmonic distortion	Input Harmonic Distortion
Intermodulation distortion	Intermodulation Distortion
Residual responses	Residual Responses
	Image Responses
Local oscillator feedthrough	Local Oscillator Feedthrough
Full scale amplitude accuracy	Amplitude Accuracy and Flatness
	Alt_Amp Accuracy and Flatness
	Reference Level Accuracy
Network Measurements	
Ratio Amplitude and Phase Specifications	
Accuracy	Dynamic Accuracy

Table 3-4. HP 35689A/B Specifications and Performance Tests

Specification	Performance Test
Directivity	Directivity and Source Match
Frequency response	
Transmission	Transmission
Reflection	Reflection
Port match	
Return loss input/output port	Return Loss
Equivalent test port match	Directivity and Source Match
Test port isolation	Isolation

Testing the HP 3589A

To test the HP 3589A Spectrum/Network Analyzer, follow the directions in "How to Load the ITM_3589A Program" then continue with one of the following:

- "How to Run the ITM_3589A Program in Semiautomated Mode"
- "How to Run the ITM_3589A Program Without a Printer"
- "How to Run the ITM_3589A Program in Manual Mode"

How to Load the ITM_3589A Program

1. Set the HP 3589A Spectrum/Network Analyzer's power switch to STANDBY (⏻), then connect the analyzer, test instruments, and printer using HP-IB cables.
2. If you have the PC Style Keyboard, connect the keyboard to the analyzer using the keyboard cable (see "Connecting the Optional Keyboard" in chapter 2).

Caution 

Do not connect or disconnect the keyboard cable with the line power turned ON (I). Connecting or disconnecting the keyboard while power is applied may damage the keyboard or the analyzer.

3. Insert the *HP 3589A Semiautomated Performance Test Disk* into the analyzer's disk drive, then set the power switch to ON (I).
4. After the analyzer finishes its power-up calibration routine, press the following keys:

   [**Local/HP-IB**]
   [SYSTEM CONTROLLR]
   [**Save/Recall**]
   [DEFAULT DISK]
   [INTERNAL DISK]
   [CANCEL/RETURN]
   [CATALOG **ON** OFF]

5. Using the marker knob, highlight the line that reads ITM_3589A.
6. Press the following keys:

   [RECALL MORE]
   [RECALL PROGRAM]
   [ENTER]

7. After the recall program is done, press the following keys:

   [**BASIC**]

   [RUN]

8. Now go to one of the following procedures to continue.

   "How to Run the ITM_3589A Program in Semiautomated Mode" (see page 3-10)
   "How to Run the ITM_3589A Program Without a Printer" (see page 3-13)
   "How to Run the ITM_3589A Program in Manual Mode" (see page 3-15)

How to Run the ITM_3589A Program in Semiautomated Mode

Note

You must have an HP-IB printer connected to your system to run the program in semiautomated mode. If you do not have a printer, see "How to Run the ITM_3589A Program Without a Printer" later in this chapter.

For information about the program's softkeys, see "Softkey Descriptions" starting on page 3-65.

1. Press the following keys and when the program prompts you, type in the information for the title page of the test record and press [ENTER]:

   [TITLE PAGE]
   [TEST FACILITY]
   [FACILITY ADDRESS]
   [TESTED BY]
   [REPORT NUMBER]
   [CUSTOMER]
   [MORE]
   [OPTIONS]
   [DATE]
   [TEMP]
   [HUMIDITY]
   [LINE FREQUENCY]
   [RETURN]

2. Press the following keys and when the program prompts you, type in the equipment configuration information.

Note

Use the following to determine HP-IB addresses:

100 × (interface select code) + (primary address)

The interface select code for the test equipment and printer is 7 (for example, if the primary address is 8, the HP-IB address is 708).

Note When entering the calibration due date, only four characters are displayed on the screen. However, you can enter up to nine characters and they will be printed.

[EQUIP CONFIG]
[SIGNAL GEN]
[SYNTH]
[SYNTH/LVL GEN]
[ANALYZER]
[MORE]
[MULTIMETER]
[POWER METER]
[POWER SENSOR]
[DIR BRIDGE]
[STEP ATTEN]
[MORE]
[FREQ STD]
[mW-POWER METER]
[21 MHz FILTER]
[50 MHz FILTER]
[RETURN]

3. Press the following keys and type in the printer address when the program prompts you:

[TEST CONFIG]
[PRINTER ADDRESS]
[PROCEDURE]
[OP_VERIFY], [ALT_OPVER], [PERFORMAN] or [ALT_PERF]
[STOP AFTER]
[LIMIT FAILURE] or [NONE]
[RETURN]

4. Press the following keys to start the test:

[START TESTING]
[START BEGINNING]

Note When you select [START BEGINNING], the data is written to a file on the disk and printed only after all tests are done. When you select [START MIDDLE] or [ONE TEST], the data is printed immediately after each measurement.

5. Now follow the directions on the display.

Note

The directions on the display briefly tell you how to connect test equipment. For a description of each test and detailed illustrations of equipment setup, see "HP 3589A Test Descriptions and Equipment Setup" starting on page 3-17.

If you want to pause the program and return the HP 3589A Spectrum/Network Analyzer to front panel control, press [**BASIC**]. To continue the program, press [**BASIC**] [CONTINUE]. If you changed any instrument setup states, press [RESTART TEST] to ensure accurate measurement results.

How to Run the ITM_3589A Program Without a Printer

1. Write in the information needed on the title page of the "HP 3589A Performance Test Record" or the "HP 3589A Operation Verification Test Record" (located near the end of this chapter).
2. Press the following keys and when the program prompts you, type in the model number and HP-IB address:

Note

Use the following to determine HP-IB addresses:

100 × (interface select code) + (primary address)

The interface select code for the test equipment is 7 (for example, if the primary address is 8, the HP-IB address is 708).

[EQUIP CONFIG]
[SIGNAL GEN]
[SYNTH]
[SYNTH/LVL GEN]
[ANALYZER]
[MULTIMETER]
[POWER METER]
[MORE]
[STEP ATTEN]
[RETURN]

3. Press the following keys:

[TEST CONFIG]
[PROCEDURE]
[OP_VERIFY], [ALT_OPVER], [PERFORMAN] or [ALT_PERF]
[STOP AFTER]
[EACH MEASUREMENT]
[RETURN]

4. Press the following keys to start the test:

[START TESTING]
[START BEGINNING]

5. Now follow the directions on the display and record every measurement result in the "HP 3589A Performance Test Record" or the "HP 3589A Operation Verification Test Record."

Note

The directions on the display briefly tell you how to connect test equipment. For a description of each test and detailed illustrations of equipment setup, see "HP 3589A Test Descriptions and Equipment Setup" starting on page 3-17.

If you want to pause the program and return the HP 3589A Spectrum/Network Analyzer to front panel control, press [**BASIC**]. To continue the program, press [**BASIC**] [CONTINUE]. If you changed any instrument setup states, press [RESTART TEST] to ensure accurate measurement results.

How to Run the ITM_3589A Program in Manual Mode

Note

Use this procedure if you want to run the program in manual mode. You will be prompted to setup all test equipment and you can check the analyzer's setup state after each measurement.

1. Press the following keys and when the program prompts you, set all HP-IB addresses to 0:

   [EQUIP CONFIG]
   [SIGNAL GEN]
   [SYNTH]
   [SYNTH/LVL GEN]
   [ANALYZER]
   [MULTIMETER]
   [POWER METER]
   [MORE]
   [STEP ATTEN]
   [RETURN]

2. Press the following keys:

   [TEST CONFIG]
   [PROCEDURE]
   [OP_VERIFY], [ALT_OPVER], [PERFORMAN] or [ALT_PERF]
   [STOP AFTER]
   [EACH MEASUREMENT]
   [RETURN]

3. Press the following keys to start the test:

   [START TESTING]
   [START BEGINNING]

4. Now follow the directions on the display and after every measurement do the following:

   a. Record the measurement result in the "HP 3589A Performance Test Record" or the "HP 3589A Operation Verification Test Record" (located near the end of this chapter).

   b. If you want to view the analyzer's setup state, press [**Format**] [SETUP STATE]. To continue the program, press [**BASIC**] [CONTINUE].

Note

If you changed any instrument setup states, press [RESTART TEST] instead of [CONTINUE] to ensure accurate measurement results.

Note

The directions on the display briefly tell you how to connect test equipment. For a description of each test and detailed illustrations of equipment setup, see "HP 3589A Test Descriptions and Equipment Setup."

HP 3589A Test Descriptions and Equipment Setup

Local Oscillator Feedthrough

Operation Verification — Yes

For Operation Verification, this test is the same as the Performance Test.

This test verifies that the HP 3589A Spectrum/Network Analyzer meets its spurious responses specification for local oscillator (LO) feedthrough. In this test, the analyzer measures the LO feedthrough, which appears as a signal at 0 Hz. This test requires no external equipment.

Phase Noise

Operation Verification – Yes

For Operation Verification, this test is the same as the Performance Test.

This test verifies that the HP 3589A Spectrum/Network Analyzer meets its frequency stability specification for noise sidebands. In this test, the analyzer uses its internal 10 MHz calibration signal as a clean signal source for measuring phase noise. This test requires no external equipment.

Residual Responses

Operation Verification – Yes

For Operation Verification, this test is the same as the Performance Test.

This test verifies that the HP 3589A Spectrum/Network Analyzer meets its spurious responses specification for residual responses. In this test, the analyzer measures the residual responses of the power line frequency and its harmonics, the power supply switching frequency, the reference frequencies, and the oscillator harmonics.

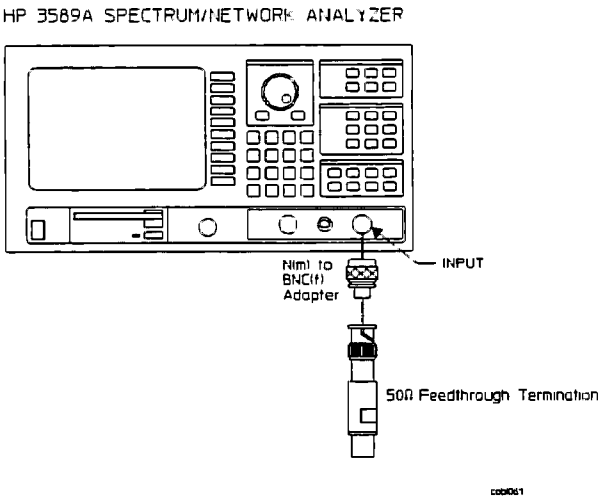


Figure 3-1. Residual Responses Test Setup

Noise Level

Operation Verification -- Yes

For Operation Verification, this test checks fewer frequencies than the Performance Test.

This test verifies that the HP 3589A Spectrum/Network Analyzer meets its dynamic range specification for noise level. In this test, the analyzer's noise level marker function measures the noise level. The noise level is measured using the receiver's 50Ω input path, with low distortion mode on and off, and using the 1 MΩ input path.

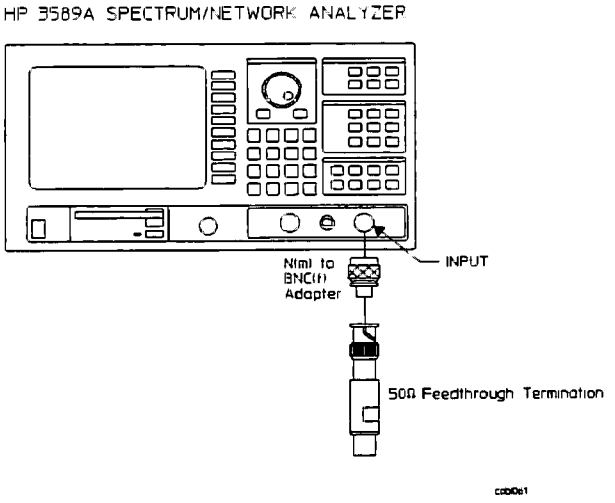


Figure 3-2. Noise Level Test Setup #1

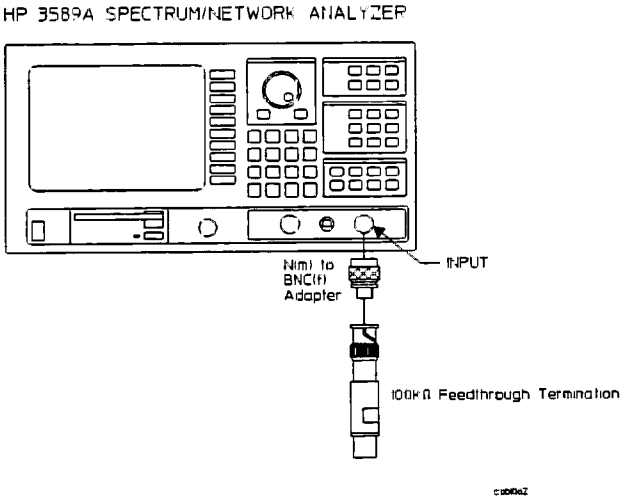


Figure 3-3. Noise Level Test Setup #2

Frequency Accuracy

Operation Verification -- Yes

For Operation Verification, this test is the same as the Performance Test.

This test verifies that the HP 3589A Spectrum/Network Analyzer meets its frequency accuracy specification. In this test, the analyzer's counter function measures an accurate 100 MHz signal. The frequency limits are then calculated using the number of days since the last frequency reference adjustment.

Note

The HP 3589A Spectrum/Network Analyzer must be on for 48 hours before performing this test.

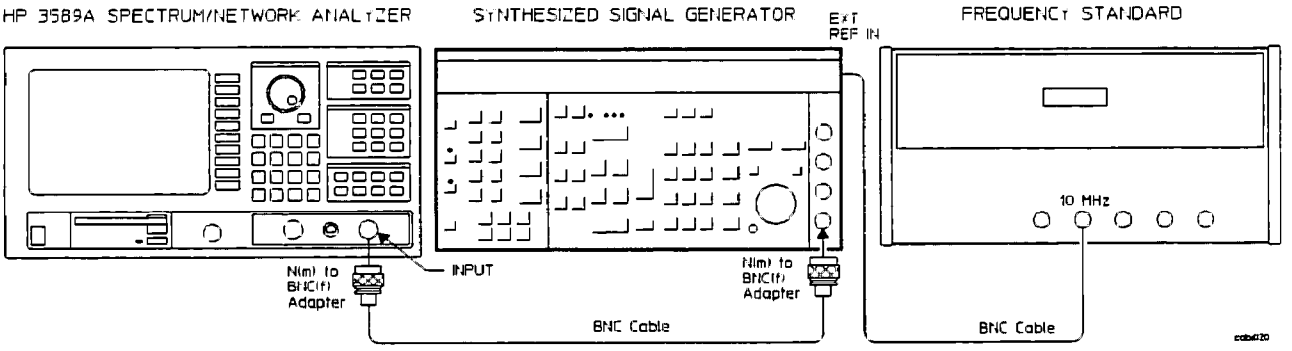


Figure 3-4. Frequency Accuracy Test Setup

Spurious Responses

Operation Verification – Yes

For Operation Verification, this test is the same as the Performance Test.

This test verifies that the HP 3589A Spectrum/Network Analyzer meets its general spurious responses specification. In this test, the analyzer measures spurious responses such as, API spurs, step loop spurs, sum loop spurs, and LO sideband spurs. The analyzer first measures a signal from the signal generator, establishing a reference level. Then, using its offset marker, the analyzer measures the spur.

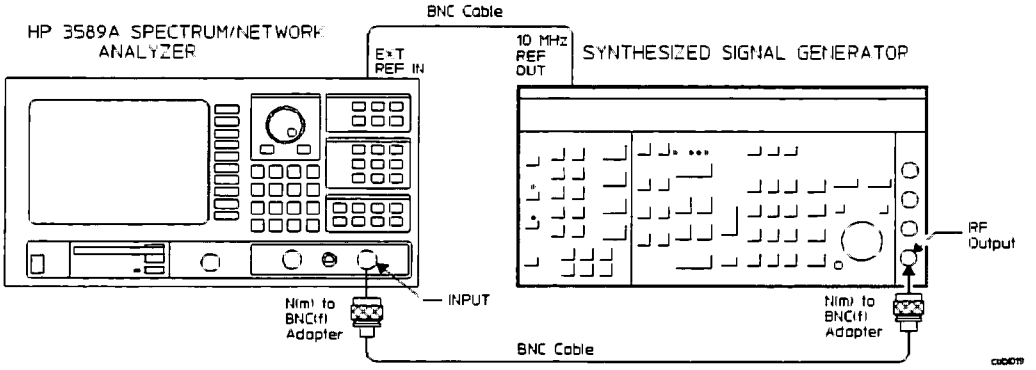


Figure 3-5. Spurious Responses Test Setup

Image Responses

Operation Verification -- Yes

For Operation Verification, this test is the same as the Performance Test.

This test verifies that the HP 3589A Spectrum/Network Analyzer meets its spurious responses specification for image responses. In this test, the analyzer measures the IF image spurs. The analyzer first measures a signal from the signal generator, establishing a reference level. Then, using its offset marker, the analyzer measures the image spurs.

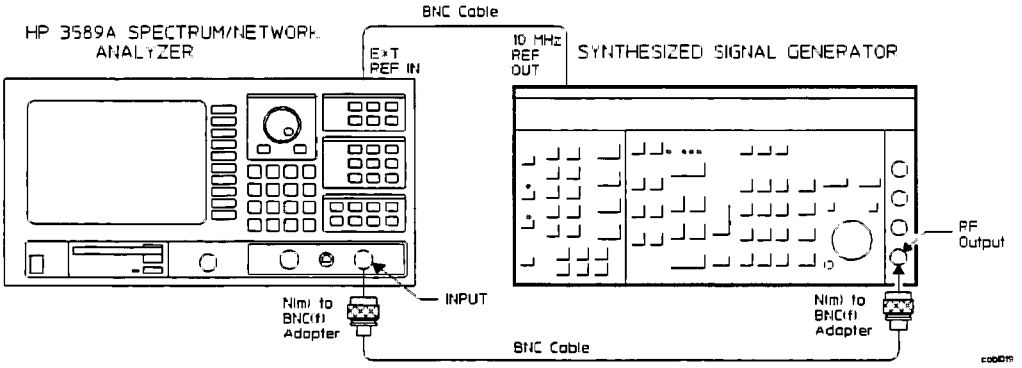


Figure 3-6. Image Responses Test Setup

Input Harmonic Distortion

Operation Verification – Yes

For Operation Verification, this test checks harmonic distortion using only the receiver's 50Ω input path with low distortion mode on.

This test verifies that the HP 3589A Spectrum/Network Analyzer meets its spurious responses specification for harmonic distortion. In this test, a low pass filter attenuates the harmonics of a signal from the synthesizer/level generator. The analyzer then measures the signal, establishing a reference level. Then, using its offset marker, the analyzer measures the second and third harmonics. Harmonic distortion is measured using the receiver's 50Ω input path, with low distortion mode on and off, and using the 1 MΩ input path.

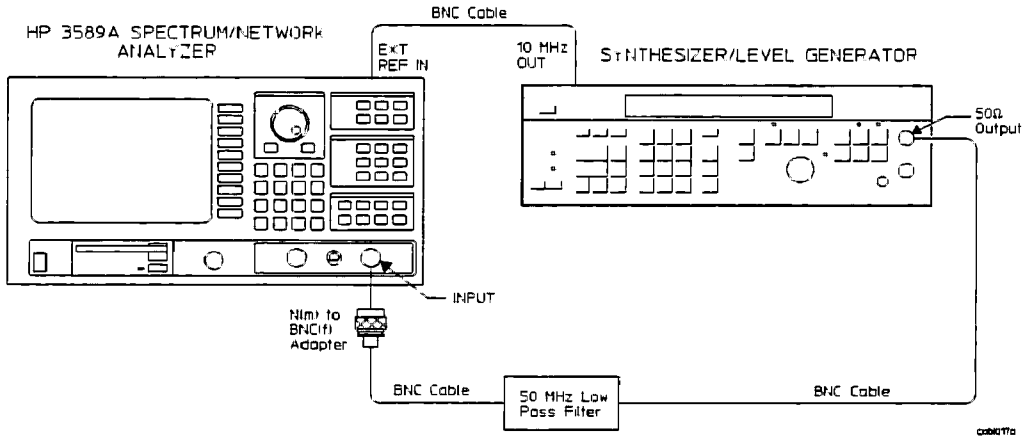


Figure 3-7. Input Harmonic Distortion Test Setup #1

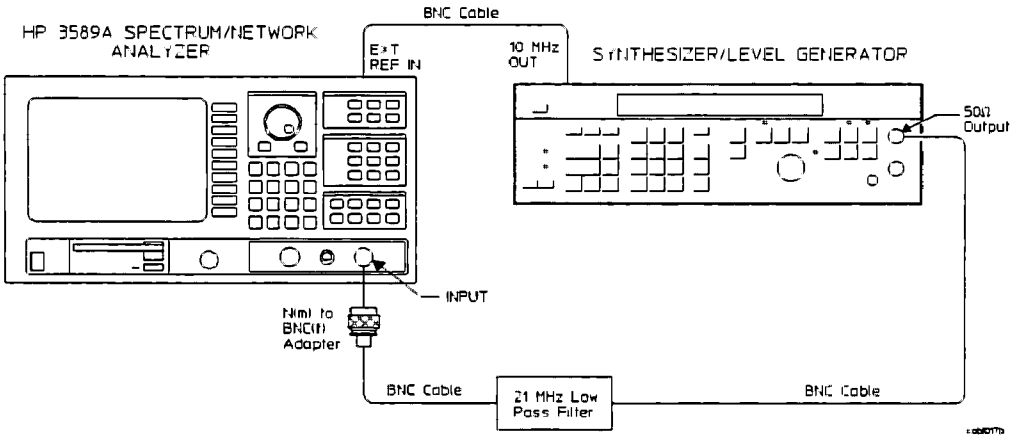


Figure 3-8. Input Harmonic Distortion Test Setup #2

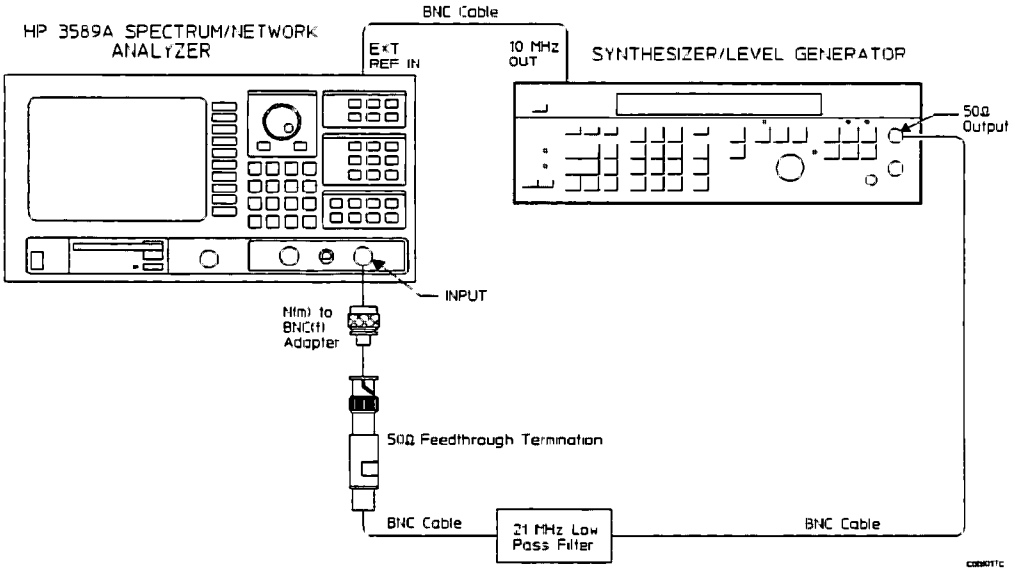


Figure 3-9. Input Harmonic Distortion Test Setup #3

Intermodulation Distortion

Operation Verification – No

This test is not required for Operation Verification.

This test verifies that the HP 3589A Spectrum/Network Analyzer meets its spurious responses specification for intermodulation distortion. In this test, a 50Ω directional bridge mixes two signals. The 10 dB amplifiers and the 10 dB attenuators are used to isolate the synthesizer/level generator from the synthesized signal generator. The resulting modulated signal is measured by the analyzer, establishing a reference level. Then, using its offset marker, the analyzer measures the second and third order intermodulation products (the sum and difference frequencies). Intermodulation distortion is measured using the receiver's 50Ω input path, with low distortion mode on and off, and using the 1 MΩ input path.

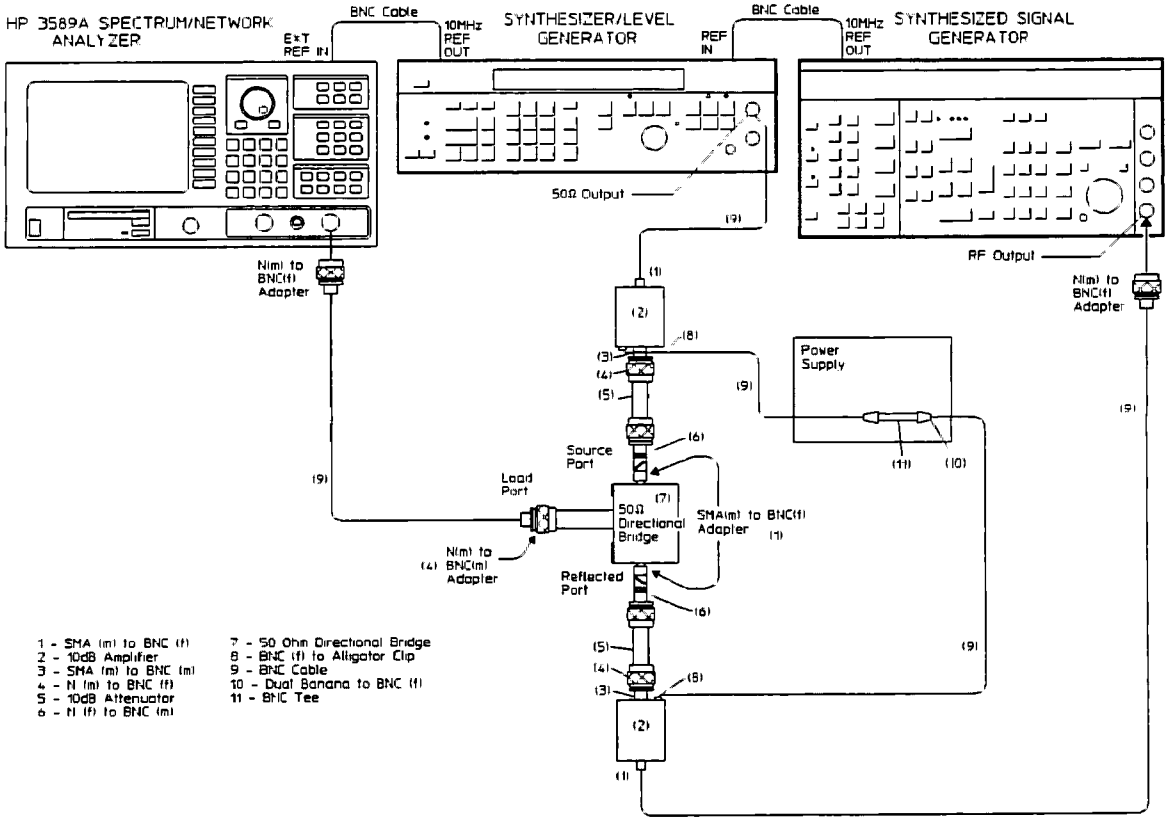


Figure 3-10. Intermodulation Distortion Test Setup #1

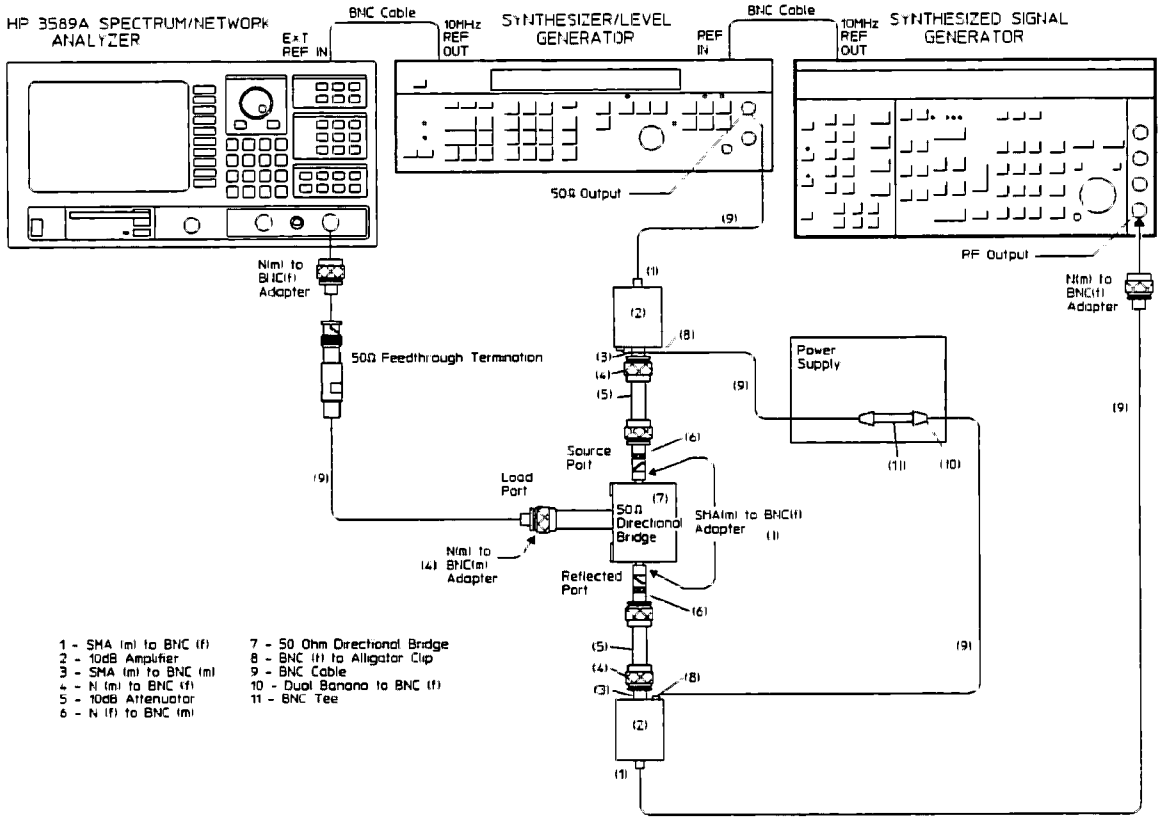


Figure 3-11. Intermodulation Distortion Test Setup #2

Source Response

Operation Verification – Yes

For Operation Verification, this test checks fewer frequencies than the Performance Test.

This test verifies that the HP 3589A Spectrum/Network Analyzer meets its source amplitude specifications for absolute amplitude accuracy and frequency response. In this test, a multimeter measures the analyzer's source from 10 Hz to 100 kHz and a power meter measures the analyzer's source from 300 kHz to 150 MHz. The value measured at 300 kHz is used to calculate the lower and upper limit specifications for all frequencies, except 300 kHz.

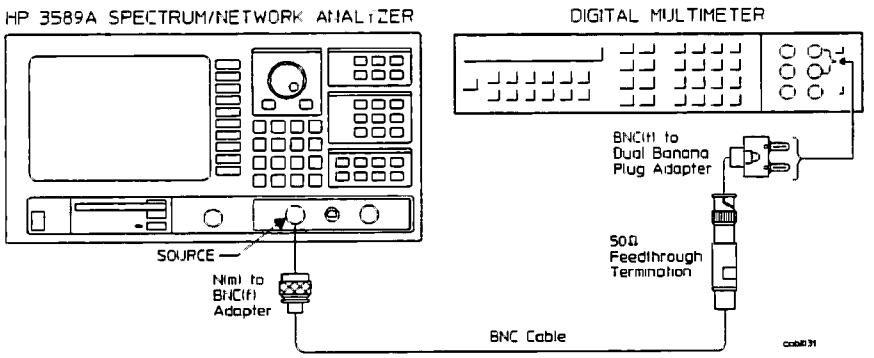


Figure 3-12. Source Response Test Setup #1

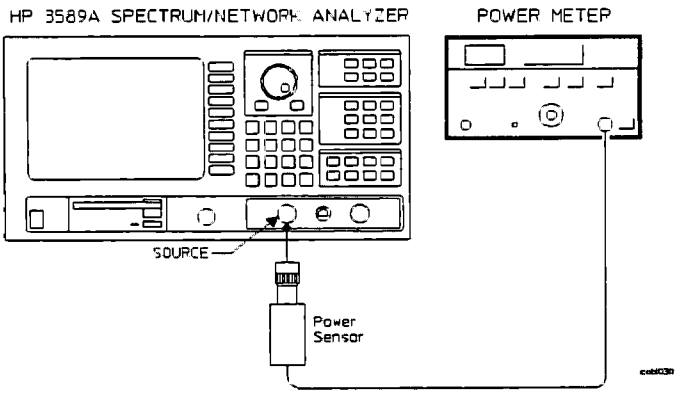


Figure 3-13. Source Response Test Setup #2

Amplitude Accuracy and Flatness

Operation Verification – Yes

For Operation Verification, this test checks input flatness using only the receiver's 50Ω input path.

Warning

This procedure requires the covers to be removed and must be performed by trained service personnel who are aware of the hazards involved (such as fire and electrical shock).

The HP 3589A Spectrum Analyzer is a Safety Class 1 instrument (provided with a protective earth terminal). Although this instrument has been designed in accordance with international safety standards, this procedure contains information, cautions and warnings that must be followed to ensure safe operation and retain the HP 3589A Spectrum/Network Analyzer in safe operating condition.

This test verifies that the HP 3589A Spectrum/Network Analyzer meets its amplitude specifications for full scale absolute accuracy. In this test, the analyzer measures the power splitter and cable errors at four spans and stores the results in its internal data registers. A milliwatt power meter provides correction to the source, maintaining 0 dBm at the power sensor input. Then the analyzer measures the flatness of each frequency span. Using its internal math functions, the analyzer corrects for any errors caused by the power splitter and cables. This test checks the input flatness from 10 Hz to 150 MHz in the 50Ω input path and from 10 Hz to 40 MHz in the 1 MΩ input path.

Note

The "Alt_Amp Accuracy and Flatness" test does not require a milliwatt power meter. Perform either this test and "Source Response" or "Alt_Amp Accuracy and Flatness."

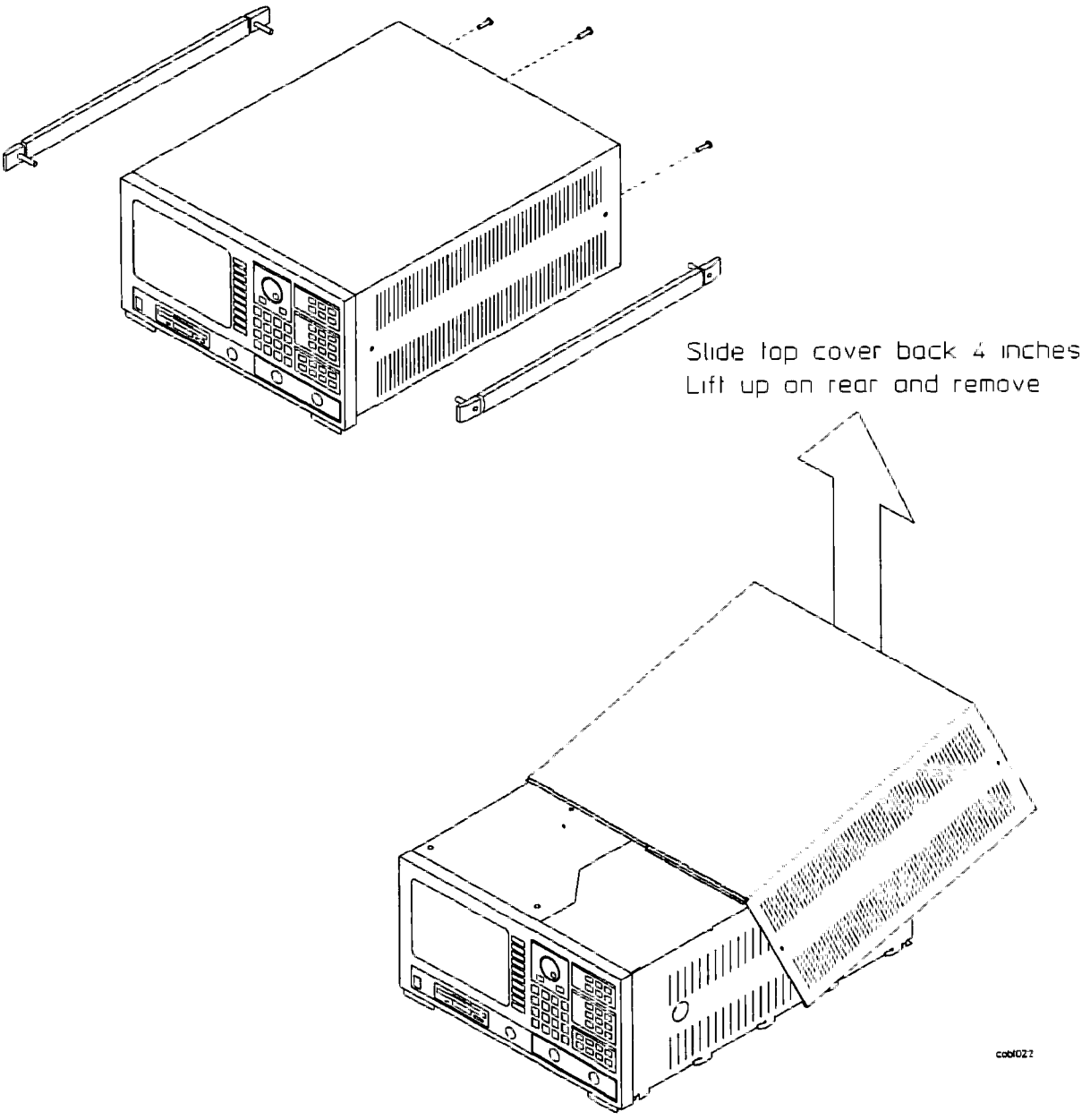


Figure 3-14. Removing Top Cover

Warning **When replacing the handle assemblies, be careful to position properly and attach firmly. If improperly attached, the handles could come off when lifting the analyzer, causing personal injury.**

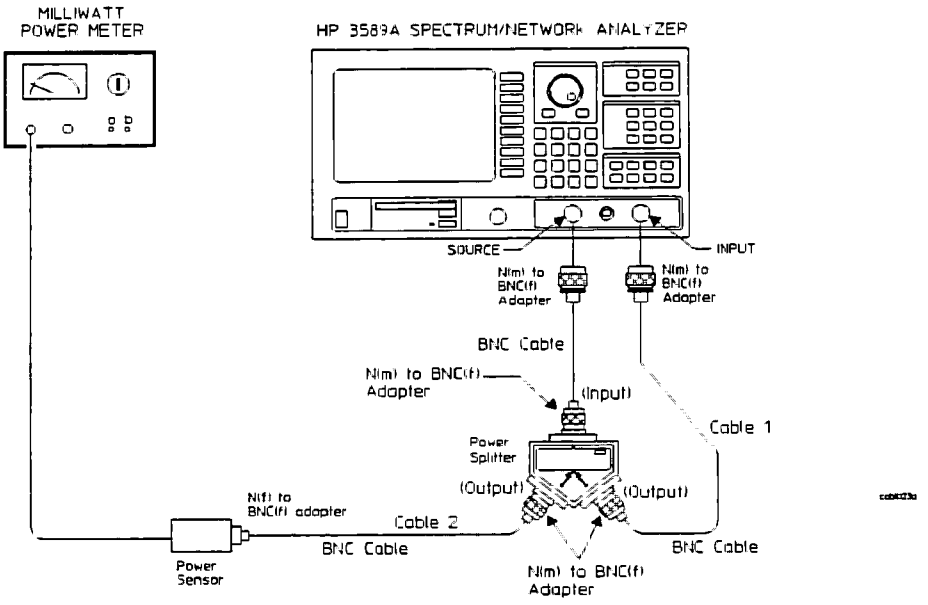


Figure 3-15. Amplitude Accuracy and Flatness Test Setup #1

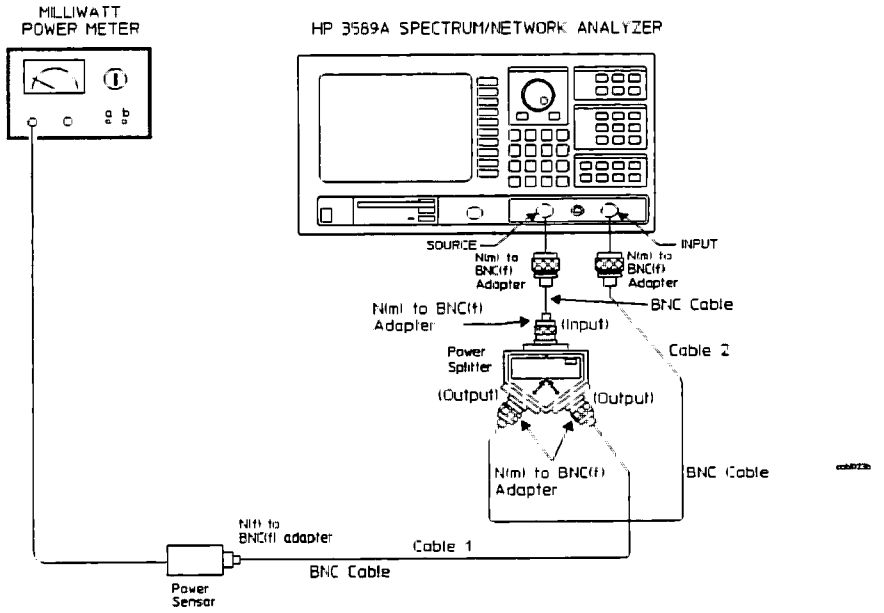


Figure 3-16. Amplitude Accuracy and Flatness Test Setup #2

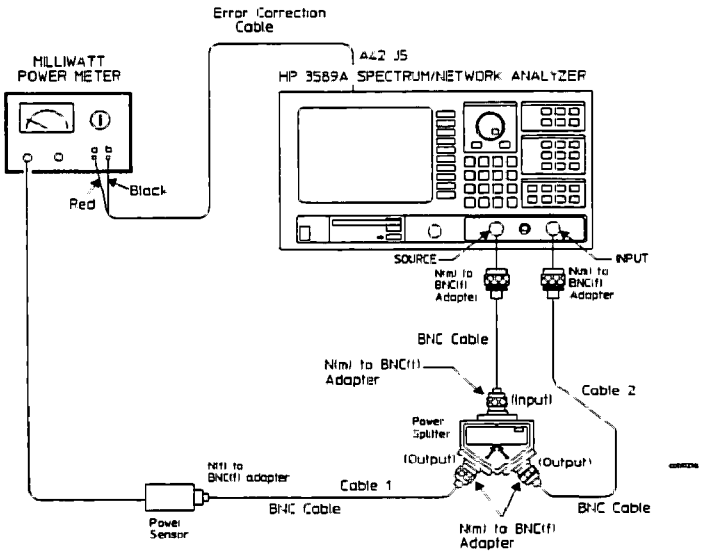


Figure 3-17. Amplitude Accuracy and Flatness Test Setup #3

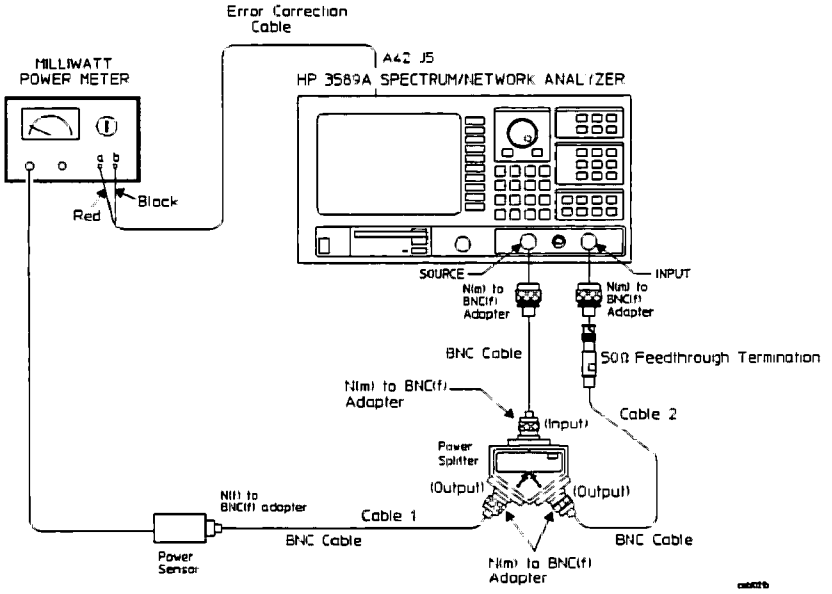


Figure 3-18. Amplitude Accuracy and Flatness Test Setup #4

Note

A calibration failure will occur if the HP 3589A Spectrum/Network Analyzer does an internal calibration while the error correction cable is connected to A42 J5. Make sure to disconnect the error correction cable before pressing [**Preset**], [SINGLE CAL], [AUTO CAL **ON** OFF], or before cycling power.

Alt_Amp Accuracy and Flatness

Operation Verification – Yes

For Operation Verification, this test checks input flatness using only the receiver's 50Ω input path.

This test verifies that the HP 3589A Spectrum/Network Analyzer meets its amplitude specification for full scale absolute accuracy and its source amplitude specification for absolute amplitude accuracy and frequency response. In this test, the analyzer generates and measures a signal from 10 Hz to 150 MHz using the receiver's 50Ω input path and from 10 Hz to 40 MHz using the 1 MΩ input path. The source amplitude levels measured in the Source Response test are subtracted from the levels measured in this test for the 50Ω input path. These levels are subtracted from the levels measured for the 1 MΩ input path. Then for specified frequency ranges in both the 50Ω and 1 MΩ input paths, the largest negative error is subtracted from the largest positive error, resulting in the frequency response error.

Note

This test is an alternate for the "Source Response" and "Amplitude Accuracy and Flatness" tests. Perform either this test or both the "Source Response" and "Amplitude Accuracy and Flatness" tests.

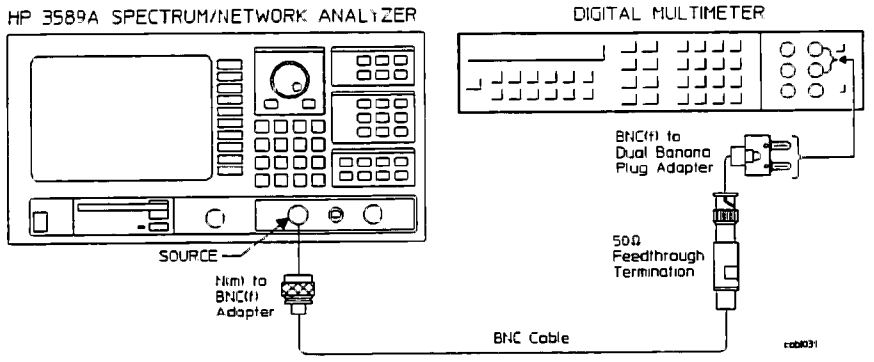


Figure 3-19. Alt_Amp Accuracy and Flatness Test Setup #1

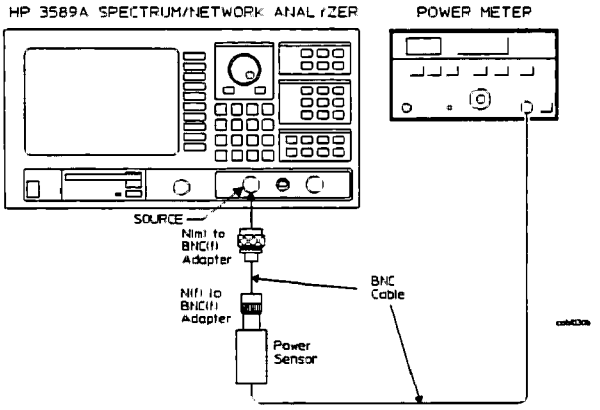


Figure 3-20. Alt-Amp Accuracy and Flatness Test Setup #2

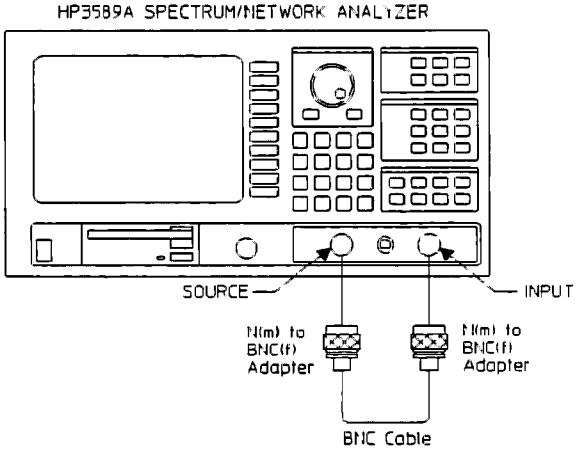


Figure 3-21. Alt-Amp Accuracy and Flatness Test Setup #3

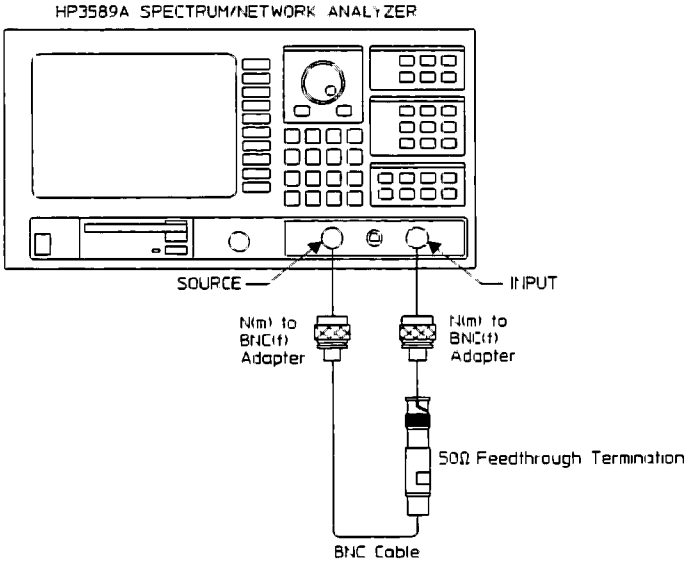


Figure 3-22. Alt-Amp Accuracy and Flatness Test Setup #4

Reference Level Accuracy

Operation Verification – Yes

For Operation Verification, this test is the same as the Performance Test.

This test verifies that the HP 3589A Spectrum/Network Analyzer meets its amplitude specification for full scale absolute accuracy. In this test, the synthesizer is adjusted to an exact amplitude level at 300 kHz. The analyzer's range is set to the amplitude level and the signal is measured. Then the receiver's input range is subtracted from the measured value. This test checks the calibrated level accuracy at five levels from –20 to +20 dBm.

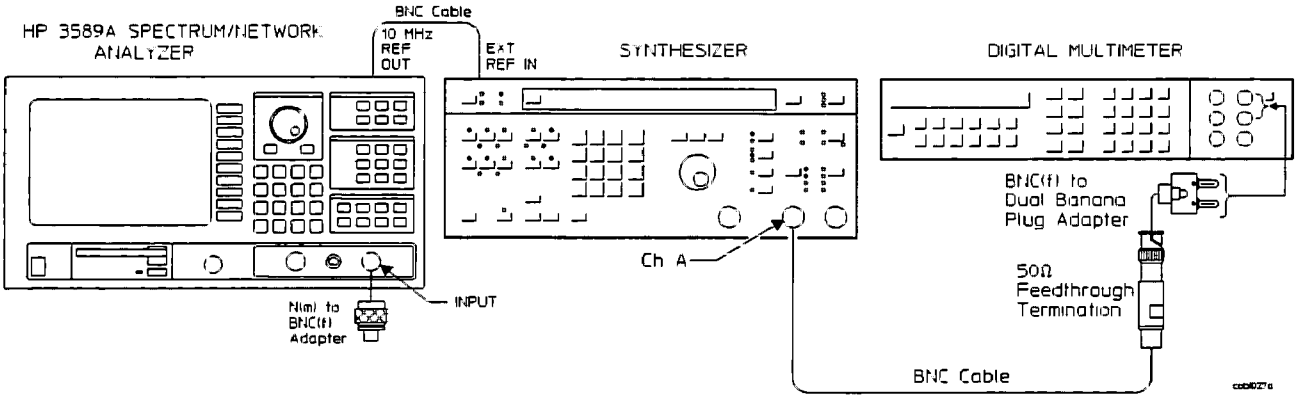


Figure 3-23. Reference Level Accuracy Test Setup #1

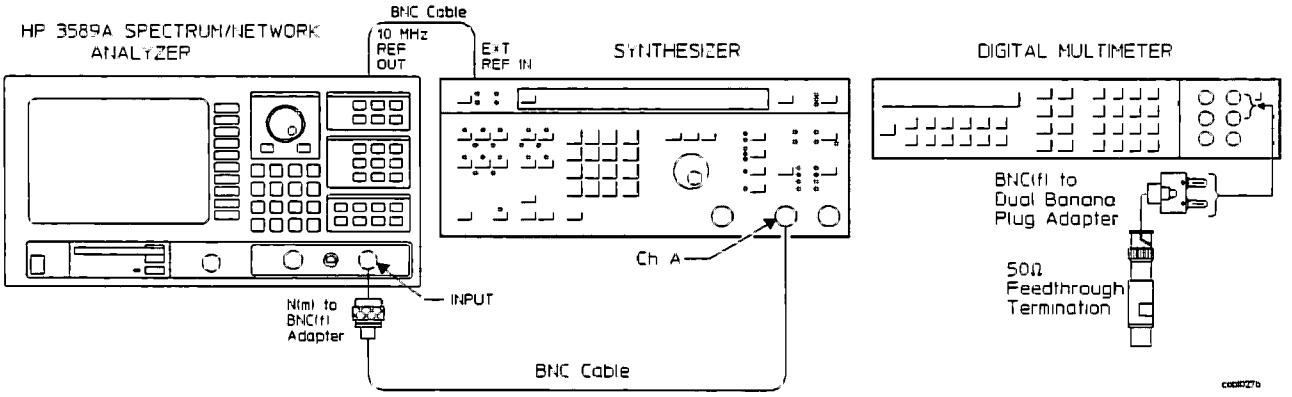


Figure 3-24. Reference Level Accuracy Test Setup #2

Dynamic Accuracy

Operation Verification – No

This test is not required for Operation Verification.

This test verifies that the HP 3589A Spectrum/Network Analyzer meets its ratio amplitude and phase specification for dynamic accuracy. This test checks dynamic accuracy at 7 amplitude levels at 300 kHz.

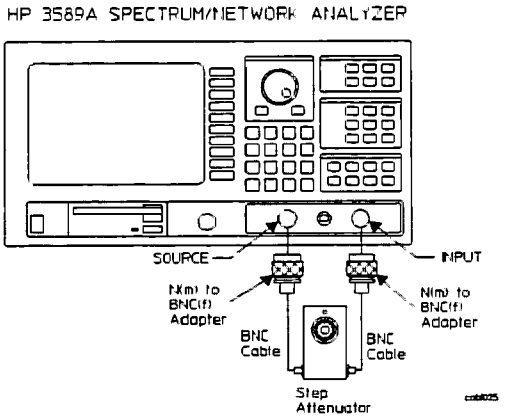


Figure 3-25. Dynamic Accuracy Test Setup

Source Dynamic Accuracy

Operation Verification – Yes

For Operation Verification, this test is the same as the Performance Test.

This test verifies that the HP 3589A Spectrum/Network Analyzer meets its source amplitude specification for dynamic accuracy. In this test, a step attenuator attenuates the source output by 20 dB, establishing a reference level. Then, the source internally attenuates the output, and the step attenuator's attenuation is decreased by the same amount. Using the offset marker, the analyzer measures the source output again. This value minus the correction for the step attenuator error is the source dynamic accuracy. This test checks dynamic accuracy at 300 kHz for all of the fixed attenuation pads and two attenuation levels in the variable attenuation circuit.

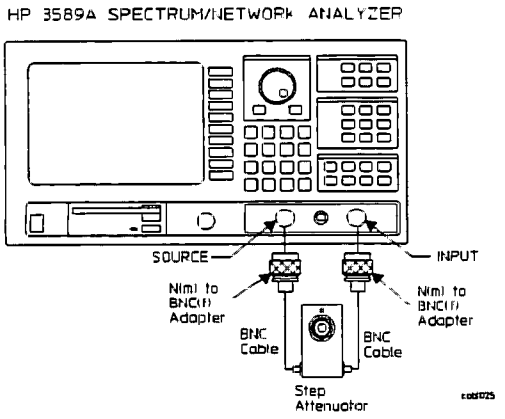


Figure 3-26. Source Dynamic Accuracy Test Setup

Input Return Loss

Operation Verification – No

This test is not required for Operation Verification.

This test verifies that the HP 3589A Spectrum/Network Analyzer meets its amplitude input port specification for return loss. In this test, a signal generator provides a signal to the source port of the 50Ω directional bridge. A spectrum analyzer measures the change that occurs to the directional bridge's reflected port when the HP 3589A analyzer's input is connected to the directional bridge's load port. This test checks the input return loss at all attenuator settings at 100 MHz and 150 MHz.

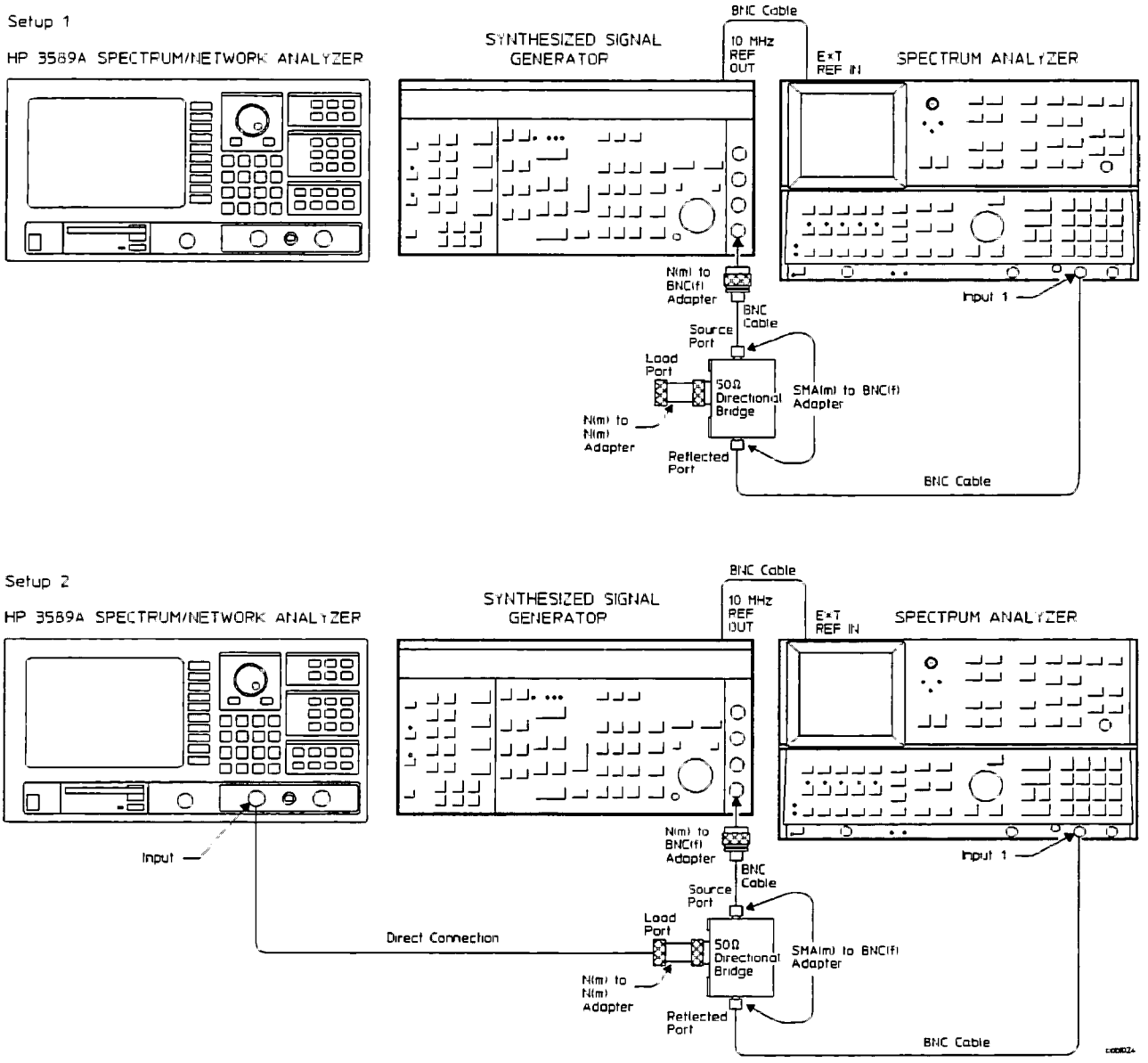


Figure 3-27. Input Return Loss Setups

Source Return Loss

Operation Verification – No

This test is not required for Operation Verification.

This test verifies that the HP 3589A Spectrum/Network Analyzer meets its source amplitude specification for return loss. In this test, a signal generator provides a signal to the source port of a 50Ω directional bridge. A spectrum analyzer measures the change that occurs to the directional bridge's reflected port when the HP 3589A analyzer's source is connected to the directional bridge's load port. This test checks the source return loss for 6 source amplitudes at 60 MHz, 120 MHz, and 150 MHz.

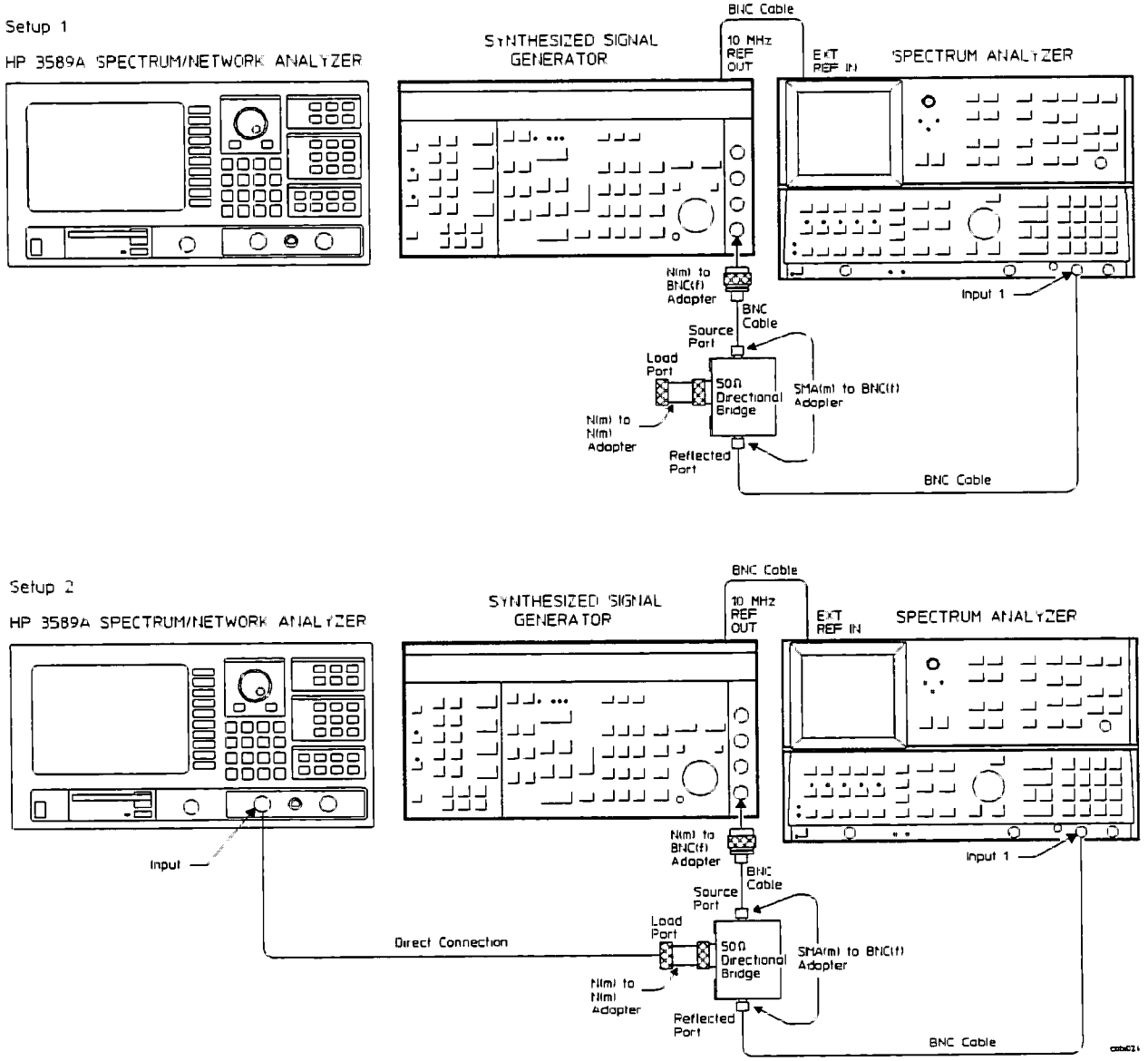


Figure 3-28. Source Return Loss Test Setups

Source Harmonic Distortion

Operation Verification – Yes

For Operation Verification, this test checks fewer frequencies than the Performance Test.

This test verifies that the HP 3589A Spectrum/Network Analyzer meets its source amplitude specification for harmonic products. In this test, a spectrum analyzer measures the source output, establishing a reference level. The spectrum analyzer then measures the second and third harmonic relative to the reference level.

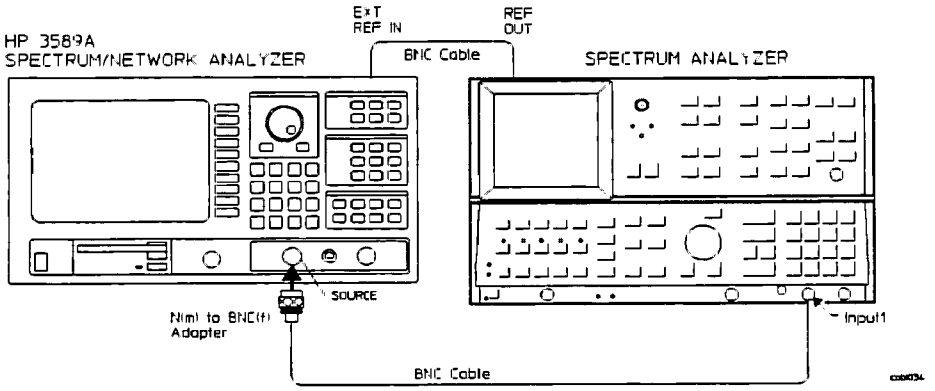


Figure 3-29. Source Harmonic Distortion Test Setup

Source Spurious Responses

Operation Verification -- Yes

For Operation Verification, this test is the same as the Performance Test.

This test verifies that the HP 3589A Spectrum/Network Analyzer meets its source amplitude specification for non-harmonic products. In this test, a spectrum analyzer measures the source's output, establishing a reference level. The spectrum analyzer then measures a spur relative to the reference level.

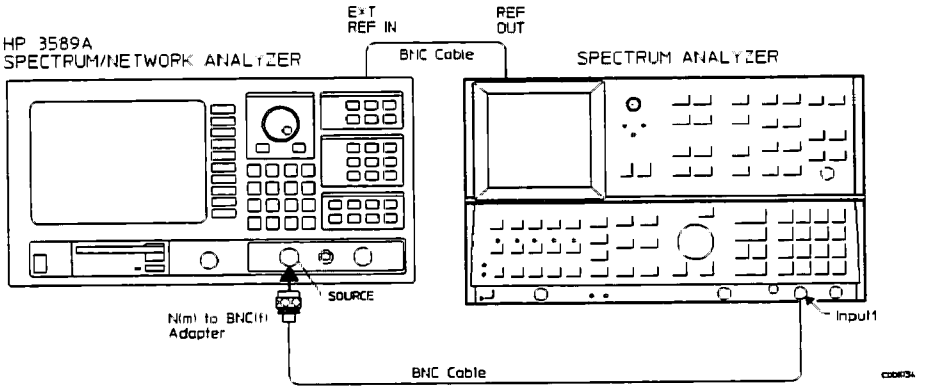


Figure 3-30. Source Spurious Responses Test Setup

Source Noise

Operation Verification – Yes

For Operation Verification, this test checks fewer frequencies than the Performance Test.

This test verifies that the HP 3589A Spectrum/Network Analyzer meets its source amplitude specification for noise. In this test, a spectrum analyzer measures the HP 3589A analyzer's source, establishing a reference level. Then, using its noise marker function, the spectrum analyzer measures the source at six offset frequencies. The spectrum analyzer's noise marker function normalizes the marker value to a 1 Hz bandwidth.

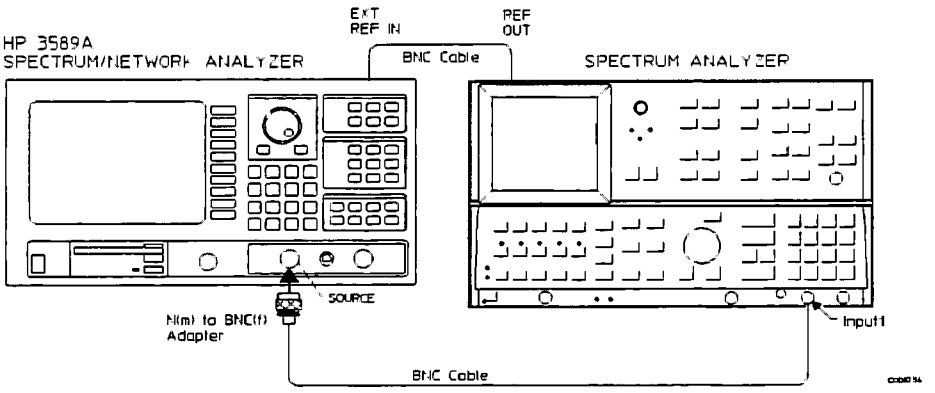


Figure 3-31. Source Noise Test Setup

Testing the HP 35689A/B

To test the HP 35689A/B S-Parameter Test Set, follow the directions in "How to Load the ITM_35689 Program" then continue with one of the following:

- "How to Run the ITM_35689 Program in Semiautomated Mode" (see page 3-47)
- "How to Run the ITM_35689 Program Without a Printer" (see page 3-49)
- "How to Run the ITM_35689 Program in Manual Mode" (see page 3-50)

Note

The HP 35689A/B S-Parameter Test Set is tested using a calibrated HP 3589A Spectrum/Network Analyzer.

How to Load the ITM_35689 Program

1. Set the power switch on the HP 35689A/B S-Parameter Test Set and HP 3589A Spectrum/Network Analyzer to STANDBY (⏻). Connect the analyzer, and printer using HP-IB cables. Connect the HP 35689A/B to the HP 3589A (see "Connecting the S-Parameter Test Set" in chapter 2).
2. If you have the PC Style Keyboard, connect the keyboard to the analyzer using the keyboard cable (see "Connecting the Optional Keyboard" in chapter 2).

Caution

Do not connect or disconnect the keyboard cable with the line power turned ON (I). Connecting or disconnecting the keyboard while power is applied may damage the keyboard or the analyzer.

3. Insert the *HP 35689A/B Semiautomated Performance Test Disk* into the analyzer's disk drive, then set the analyzer's power switch to ON (I).
4. After the analyzer finishes its power-up calibration routine, press the following keys:

   [**Local/HP-IB**]
   [SYSTEM CONTROLLR]
   [**Save/Recall**]
   [DEFAULT DISK]
   [INTERNAL DISK]
   [CANCEL/RETURN]
   [CATALOG **ON** OFF]

5. Using the marker knob, highlight the line that reads ITM_35689.

6. Press the following keys:

   [RECALL MORE]
   [RECALL PROGRAM]
   [ENTER]

7. After the recall program is done, press the following keys:

   [**BASIC**]
   [RUN]

8. Now go to one of the following procedures to continue.

   "How to Run the ITM_35689 Program in Semiautomated Mode" (see page 3-47)
   "How to Run the ITM_35689 Program Without a Printer" (see page 3-49)
   "How to Run the ITM_35689 Program in Manual Mode" (see page 3-50)

How to Run the ITM_35689 Program in Semiautomated Mode

Note

You must have an HP-IB printer connected to your system to run the program in semiautomated mode. If you do not have a printer, see "How to Run the ITM_35689 Program Without a Printer" later in this chapter.

For information about the program's softkeys, see "Softkey Descriptions" starting on page 3-65.

1. Press the following keys and when the program prompts you, type in the information for the title page of the test record and press [ENTER]:

   [TITLE PAGE]
   [TEST FACILITY]
   [FACILITY ADDRESS]
   [TESTED BY]
   [REPORT NUMBER]
   [CUSTOMER]
   [MORE]
   [OPTIONS]
   [DATE]
   [TEMP]
   [HUMIDITY]
   [LINE FREQUENCY]
   [RETURN]

2. Press the following keys and when the program prompts you, type in the equipment configuration information.

Note

Use the following to determine HP-IB addresses:

100 × (interface select code) + (primary address)

The interface select code for the test equipment and printer is 7 (for example, if the primary address is 8, the HP-IB address is 708).

Note

When entering the calibration due date, only four characters are displayed on the screen. However, you can enter up to nine characters and they will be printed.

[EQUIP CONFIG]
[NETWORK ANALYZER]
[Z0 TERMINATI]
[DIR BRIDGE]
[RETURN]

3. Press the following keys and type in the printer address when the program prompts you:

   [TEST CONFIG]
   [PRINTER ADDRESS]
   [PROCEDURE]
   [A_OPVER], [B_OPVER], [A_PERF], or [B_PERF]
   [STOP AFTER]
   [LIMIT FAILURE] or [NONE]
   [RETURN]

4. Press the following keys to start the test:

   [START TESTING]
   [START BEGINNING]

Note

When you select [START BEGINNING], the data is written to a file on the disk and printed only after all tests are done. When you select [START MIDDLE] or [ONE TEST], the data is printed immediately after each measurement.

5. Now follow the directions on the display.

Note

The directions on the display briefly tell you how to connect test equipment. For a description of each test and detailed illustrations of equipment setup, see "HP 35689A/B Test Descriptions and Equipment Setup" starting on page 3-51.

If you want to pause the program and return the HP 3589A Spectrum/Network Analyzer to front panel control, press [**BASIC**]. To continue the program, press [**BASIC**] [CONTINUE]. If you changed any instrument setup states, press [RESTART TEST] to ensure accurate measurement results.

How to Run the ITM_35689 Program Without a Printer

1. Write in the information needed on the title page of the "HP 35689A/B Performance Test Record" or the "HP 35689A/B Operation Verification Test Record" (located near the end of this chapter).
2. Press the following keys:

   [TEST CONFIG]
   [PROCEDURE]
   [A_OPVER], [B_OPVER], [A_PERF], or [B_PERF]
   [STOP AFTER]
   [EACH MEASUREMENT]
   [RETURN]

3. Press the following keys to start the test:

   [START TESTING]
   [START BEGINNING]

4. Now follow the directions on the display and record every measurement result in the "HP 35689A/B Performance Test Record" or the "HP 35689A/B Operation Verification Test Record."

Note

The directions on the display briefly tell you how to connect test equipment. For a description of each test and detailed illustrations of equipment setup, see "HP 35689A/B Test Descriptions and Equipment Setup" starting on page 3-51.

If you want to pause the program and return the HP 3589A Spectrum/Network Analyzer to front panel control, press [**BASIC**]. To continue the program, press [**BASIC**] [CONTINUE]. If you changed any instrument setup states, press [RESTART TEST] to ensure accurate measurement results.

How to Run the ITM_35689 Program in Manual Mode

Note

Use this procedure if you want to run the program in manual mode. You will be prompted to setup all test equipment and you can check the analyzer's setup state after each measurement.

1. Press the following keys:

   [TEST CONFIG]
   [PROCEDURE]
   [A_OPVER], [B_OPVER], [A_PERF], or [B_PERF]
   [STOP AFTER]
   [EACH MEASUREMENT]
   [RETURN]

2. Press the following keys to start the test:

   [START TESTING]
   [START BEGINNING]

3. Now follow the directions on the display and after every measurement do the following:

   a. Record the measurement result in the "HP 35689A/B Performance Test Record" or the "HP 35689A/B Operation Verification Test Record" (located near the end of this chapter).

   b. If you want to view the analyzer's setup state, press [**Format**] [SETUP STATE]. To continue the program, press [**BASIC**] [CONTINUE].

Note

If you changed any instrument setup states, press [RESTART TEST] to ensure accurate measurement results.

The directions on the display briefly tell you how to connect test equipment. For a description of each test and detailed illustrations of equipment setup, see "HP 35689A/B Test Descriptions and Equipment Setup" starting on page 3-51.

HP 35689A/B Test Descriptions and Equipment Setup

Directivity and Source Match

Operation Verification — Yes

For Operation Verification, this test is the same as the Performance Test.

This test verifies that the HP 35689A/B S-Parameter Test Set meets its directivity and port source match specifications. In this test, the test set is connected to the network analyzer. The network analyzer measures the Port 1 and Port 2 reflections from open, short, and Z_0 terminations for both magnitude and phase. Source match is then calculated using the following equation:

$$\text{ell} = \frac{\Gamma_{open} + \Gamma_{short} - 2\ (\ \Gamma_{z0}\ )}{\Gamma_{open} - \Gamma_{short}}$$

Directivity is calculated using the following equation:

$$\text{directivity} = \frac{\Gamma_{z0}}{\Gamma_{short}}$$

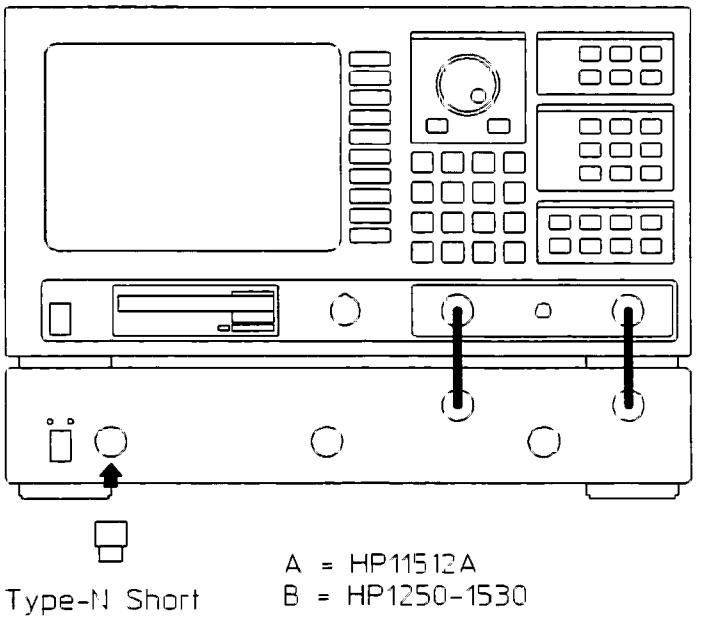


Figure 3-32. Directivity and Source Match Test Setup #1

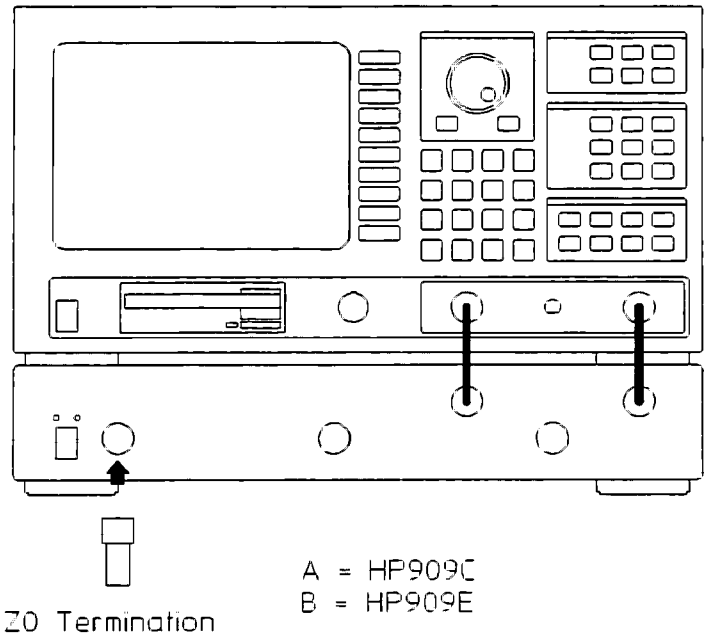


Figure 3-33. Directivity and Source Match Test Setup #2

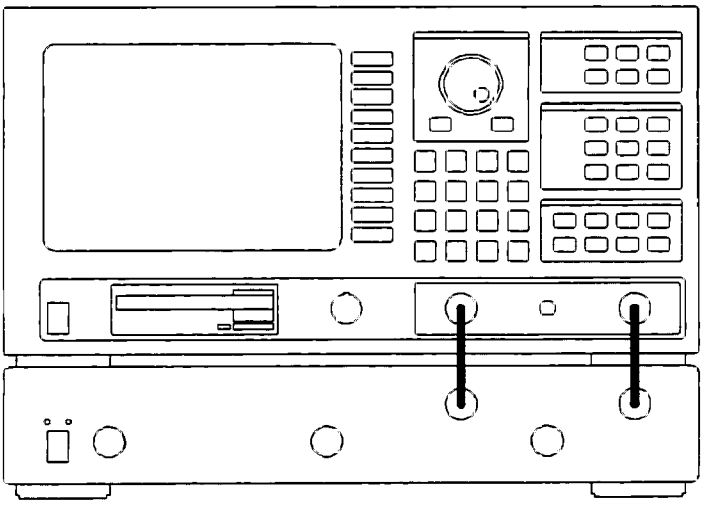


Figure 3-34. Directivity and Source Match Test Setup #3

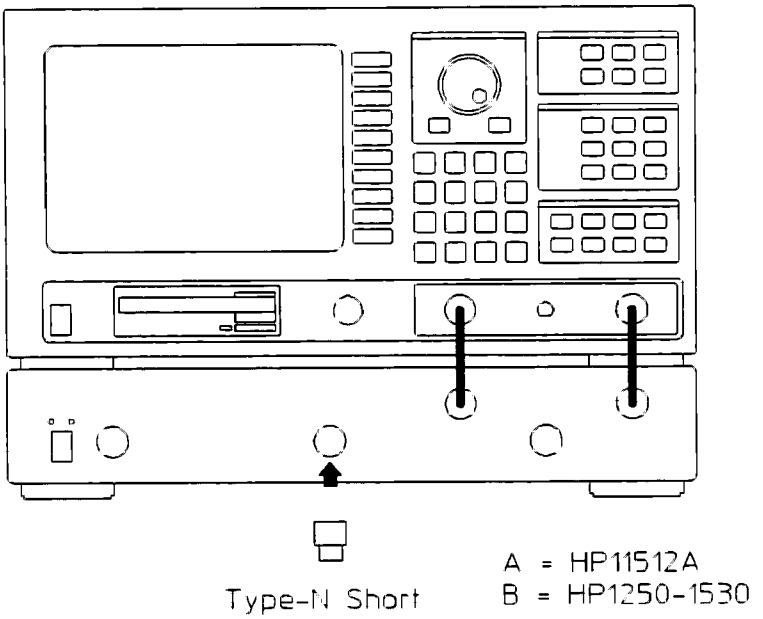


Figure 3-35. Directivity and Source Match Test Setup #4

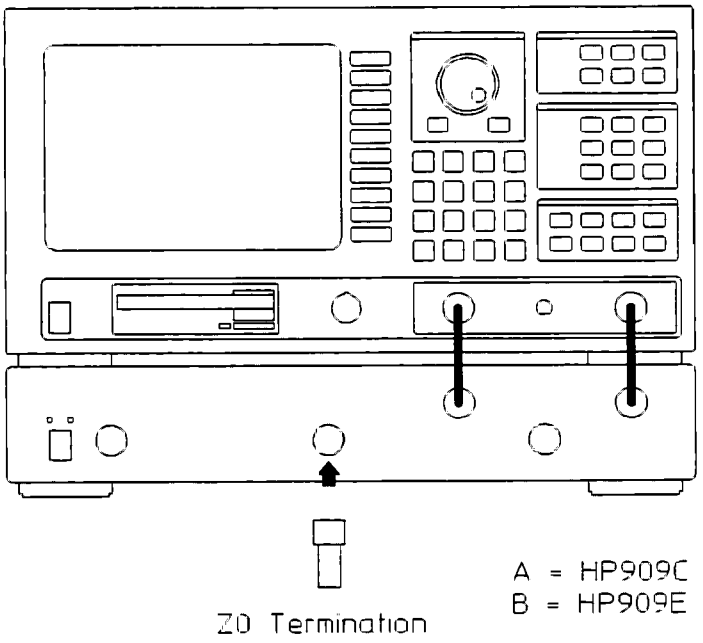


Figure 3-36. Directivity and Source Match Test Setup #5

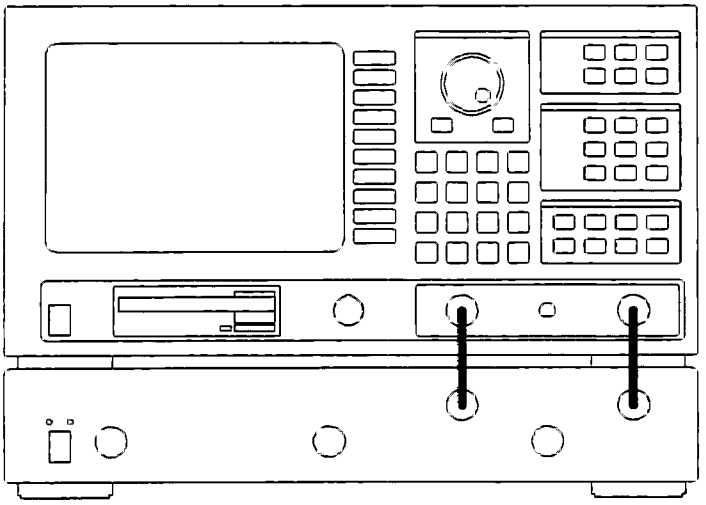


Figure 3-37. Directivity and Source Match Test Setup #6

Reflection

Operation Verification -- Yes

For Operation Verification, this test is the same as the Performance Test.

This test verifies that the HP 35689A/B S-Parameter Test Set meets its reflection specification for frequency response. In this test, the test set is connected to the network analyzer. The network analyzer measures the return loss of a short.

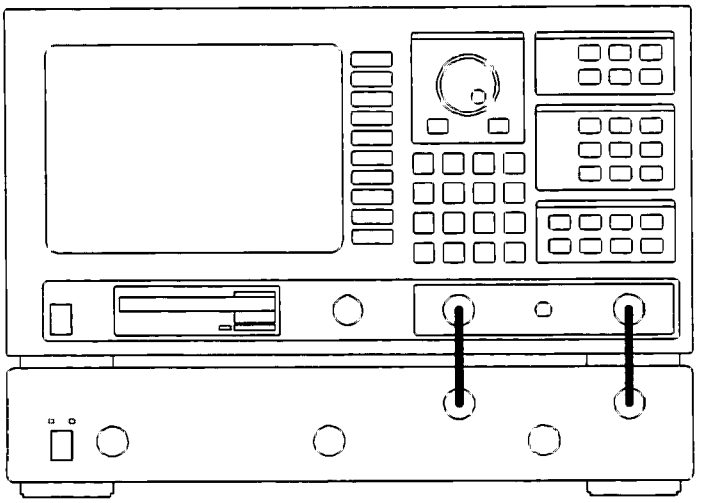


Table 3-38. Reflection Test Setup #1

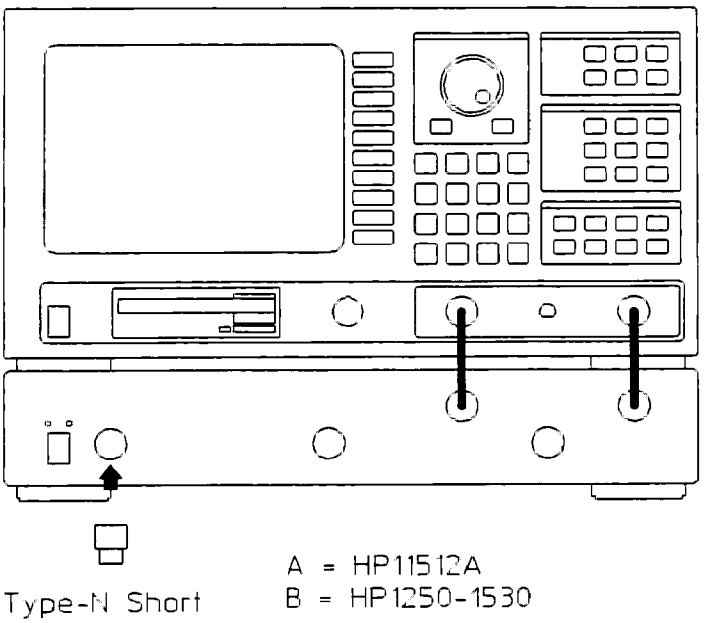


Table 3-39. Reflection Test Setup #2

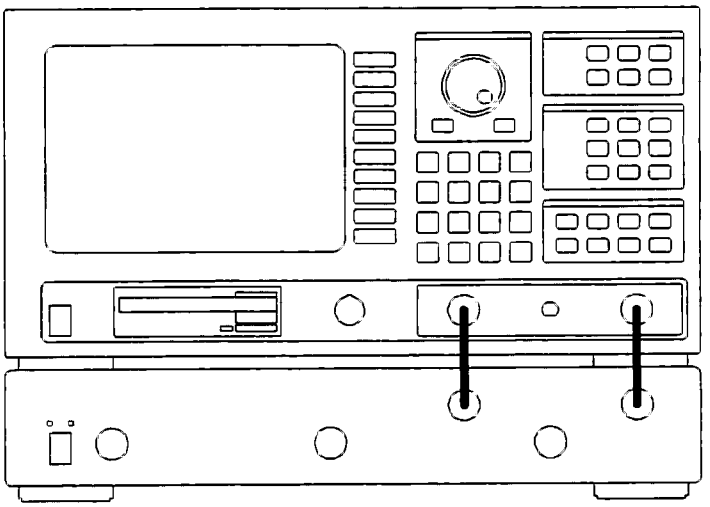


Table 3-40. Reflection Test Setup #3

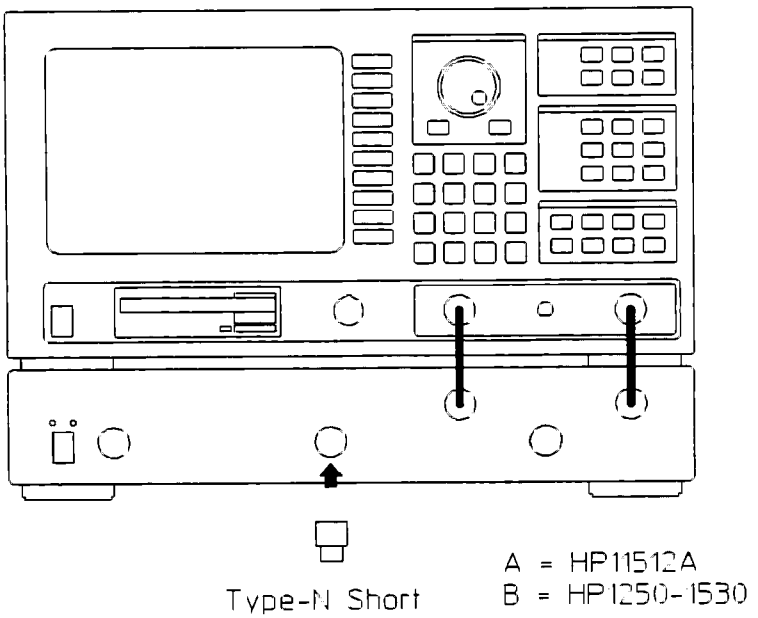


Table 3-41. Reflection Test Setup #4

Transmission

Operation Verification – Yes

For Operation Verification, this test is the same as the Performance Test.

This test verifies that the HP 35689A/B S-Parameter Test Set meets its transmission specification for frequency response. In this test, the test set is connected to the network analyzer and a cable is connected between the test ports. The netwok analyzer measures the response of the cable connected between the test ports. Another cable is connected between the test ports and the network analyzer measures the response of both cables. This results in a calibrated cable which is connected to the test ports. The network analyzer then measures the frequency response of both S_{21} and S_{12} modes.

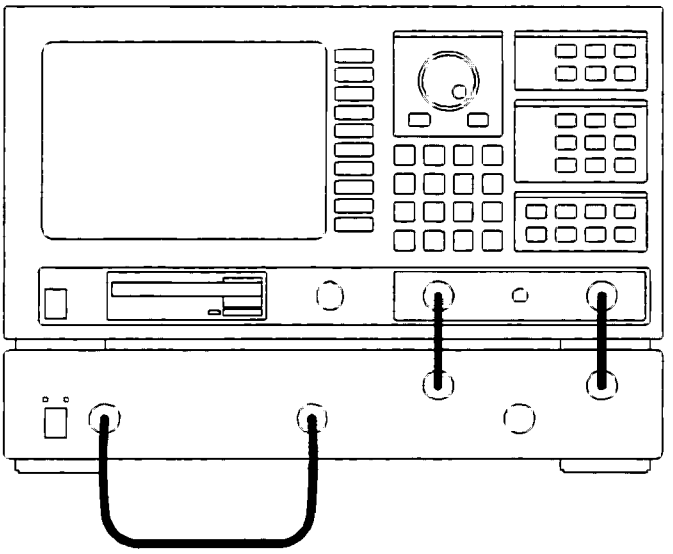


Figure 3-42. Transmission Test Setup #1

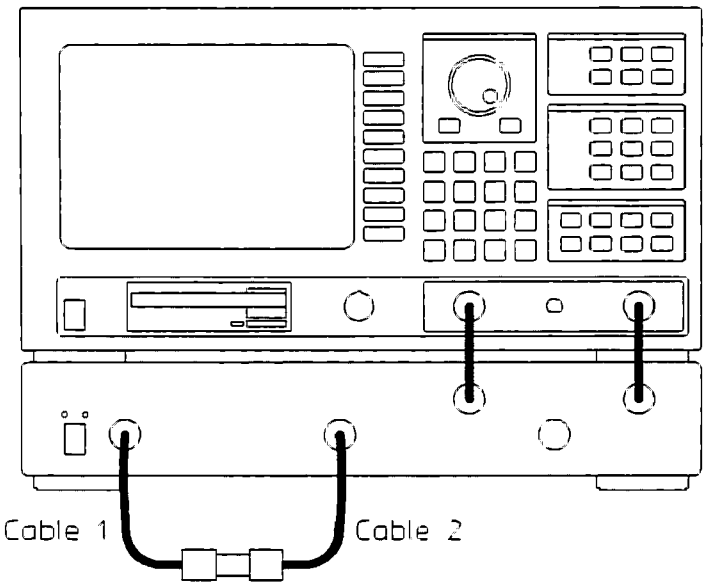


Figure 3-43. Transmission Test Setup #2

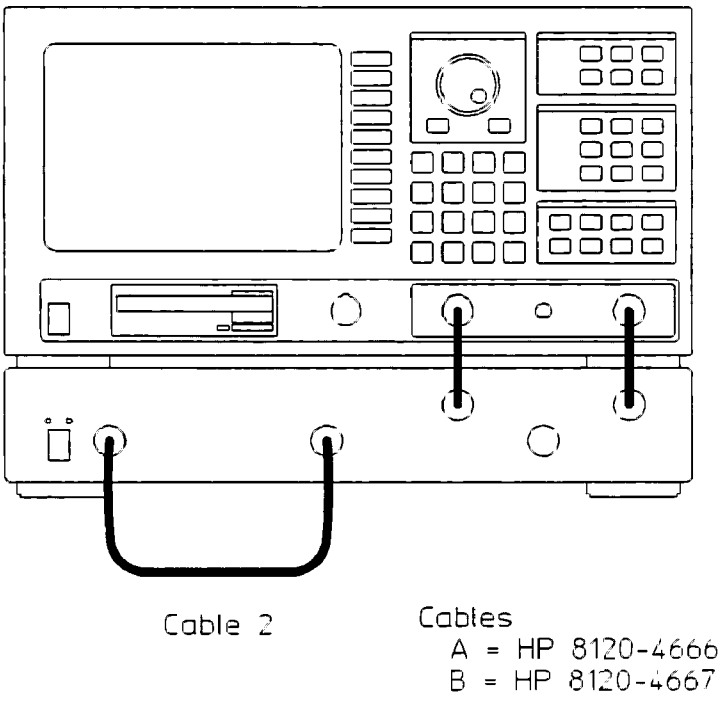


Figure 3-44. Transmission Test Setup #3

Isolation

Operation Verification – No

This test is not required for Operation Verification.

This test verifies that the HP 35689A/B S-Parameter Test Set meets its test port isolation specification. In this test, the test set is connected to the network analyzer and a cable is connected between the test ports. The network analyzer makes a transmission measurement and stores it as a reference. The two test ports are then terminated in a Z_0 load and the network analyzer makes another transmission measurement. The ratio of the reference measurement to the Z_0 measurement is a measure of test port isolation.

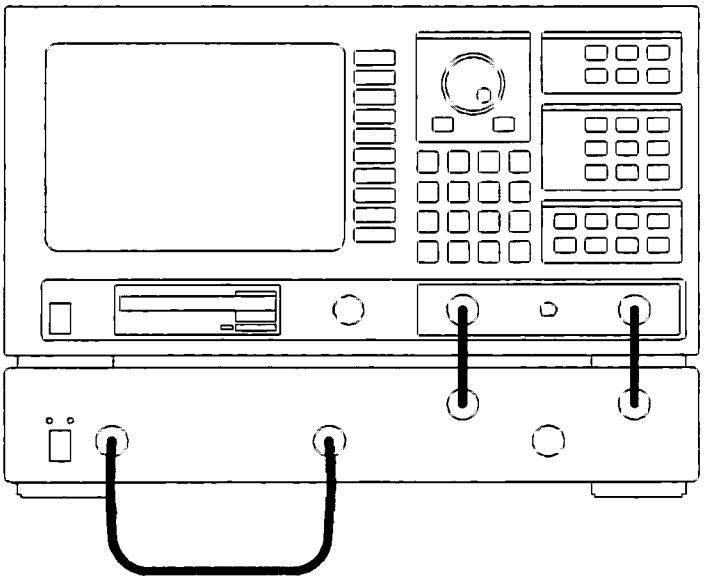


Figure 3-45. Isolation Test Setup #1

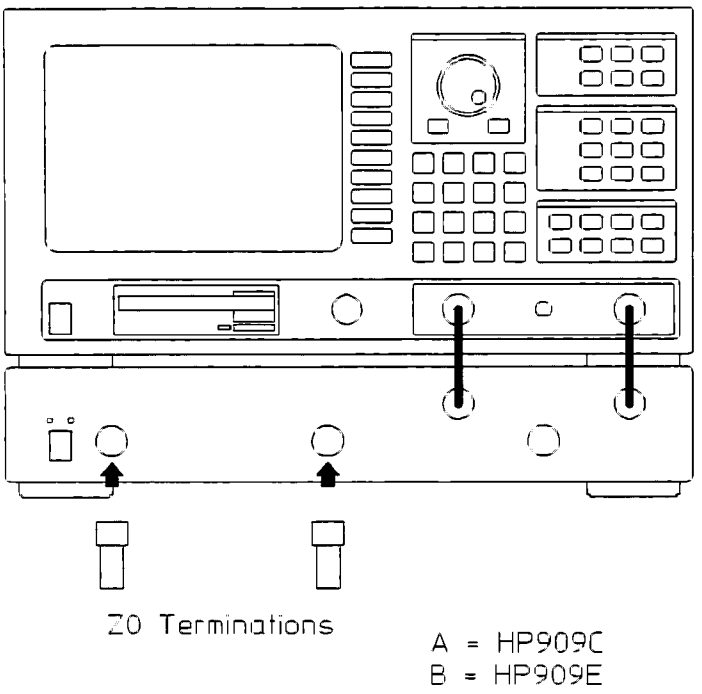


Figure 3-46. Isolation Test Setup #2

Return Loss

Operation Verification – No

This test is not required for Operation Verification.

This test verifies that the HP 35689A/B S-Parameter Test Set meets its port match return loss specification. In this test, all critical ports on the test set are terminated in their characteristic impedance. The network analyzer then measures the input and output port return loss using a directional bridge.

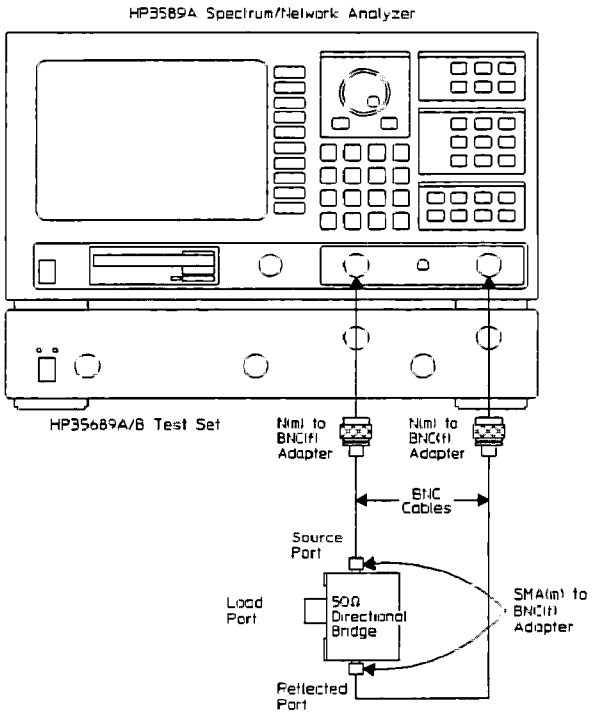


Figure 3-47. Return Loss Test Setup #1

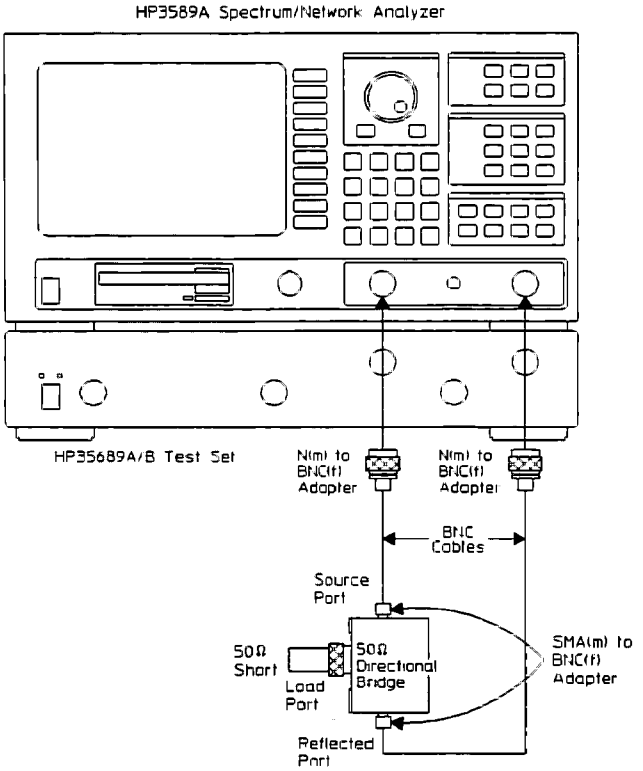


Figure 3-48. Return Loss Test Setup #2

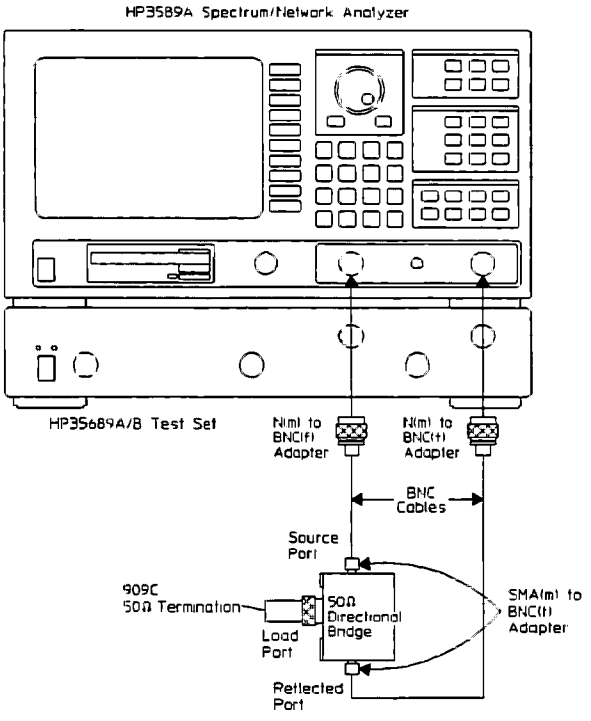


Figure 3-49. Return Loss Test Setup #3

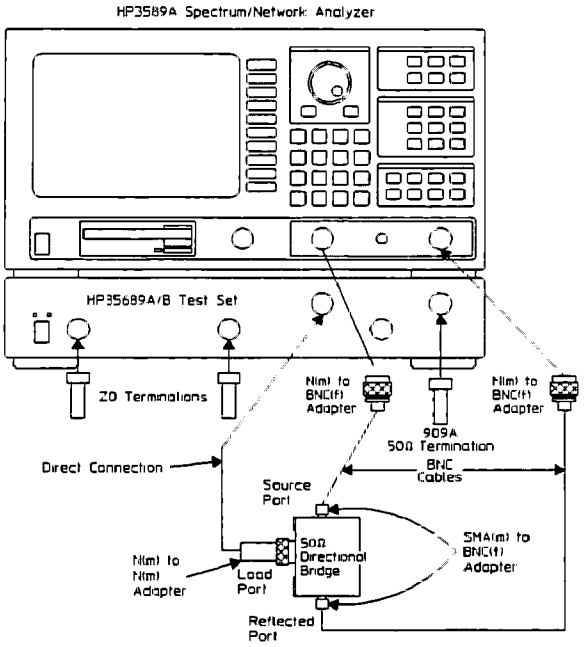


Figure 3-50. Return Loss Test Setup #4

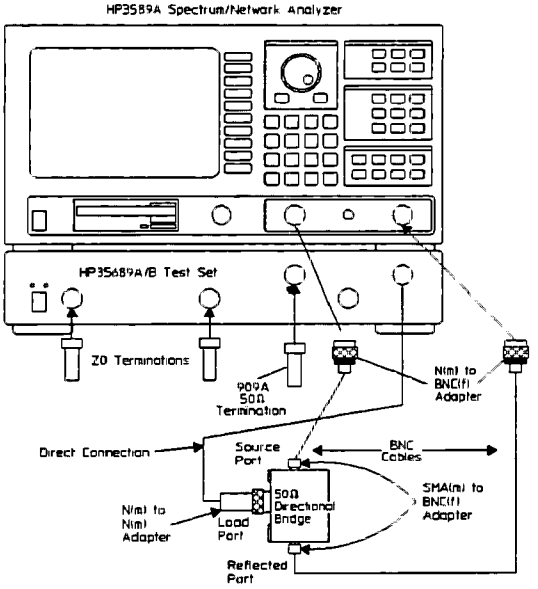


Figure 3-51. Return Loss Test Setup #5

Softkey Descriptions

Note

If you do not have a keyboard connected to the analyzer, use the numeric key pad and the alpha keys to enter names or numbers. See the analyzer's help text for a description of the alpha keys.

Main Menu

Load and run the ITM_3589A or ITM_35689 program to display the following softkeys:

[START TESTING]	Press [START TESTING] to display a menu that allows you to start testing with any test or to select just one test in the list. Before pressing this softkey, use [TEST CONFIG] and [EQUIP CONFIG].
[TEST CONFIG]	Press [TEST CONFIG] to display the test configuration and a menu that allows you to enter the procedure, stop conditions, beeper prompt, and HP-IB address for the analyzer and printer.
[EQUIP CONFIG]	Press [EQUIP CONFIG] to display the test equipment configuration and a menu that allows you to enter the model number, calibration due date, serial number, and HP-IB address for each test instrument.
[TITLE PAGE]	Press [TITLE PAGE] to display the test record title page information and a menu that allows you to enter information for the instrument.
[STOP ITM]	Press [STOP ITM] to stop the program.

Start Testing Menu

In the main menu of either the ITM_3589A or ITM_35689 program press [START TESTING] to display the following softkeys:

Note

When you select [START BEGINNING], the data is written to a file on the disk and printed only after all tests are done. When you select [START MIDDLE] or [ONE TEST], the data is printed immediately after each measurement.

[START BEGINNING] Press [START BEGINNING] to print the test record title page information and to start the selected test procedure at the beginning.

[START MIDDLE] Press [START MIDDLE] to display a list of all the tests in the selected procedure. Testing starts with the test you select and continues through the remainder of the tests in the list.

[ONE TEST] Press [ONE TEST] to display all the tests in the selected procedure. The test you select is the only test performed.

[RETURN] Press [RETURN] to return to the main menu.

Start a test to display the following softkeys:

[STOP TESTING] Press [STOP TESTING] to stop the test and return to the main menu.

[RESTART TEST] Press [RESTART TEST] to start the current test over. Any connection prompts are repeated.

[RESTART MEAS] Press [RESTART MEAS] to start the current measurement over.

The following softkeys also appear when the program is waiting for you to press [CONTINUE]:

[STOP BEEPING] Press [STOP BEEPING] to turn off the beeper prompt for the remainder of this measurement.

[CONTINUE] Press [CONTINUE] to continue testing after following the directions on the display.

Test Configuration Menu

Note

Use the following to determine HP-IB addresses:

100 × (interface select code) + (primary address)

The interface select code for the printer and test equipment is 7 (for example, if the primary address is 8, the HP-IB address is 708).

In the main menu of the ITM_3589A program press [TEST CONFIG] to display the test configuration and the following softkeys:

[HP 3589A ADDRESS] Press [HP 3589A ADDRESS] to enter the HP-IB address for the HP 3589A Spectrum/Network Analyzer.

[PRINTER ADDRESS] Press [PRINTER ADDRESS] to enter the HP-IB address for the printer. To disable the printer, set the printer address to 0.

[PROCEDURE] Press [PROCEDURE] to select the operation verification procedure (OP_VERIFY), the alternate operation verification procedure (ALT_OPVER), the performance test procedure (PERFORMAN), or the alternate performance test procedure (ALT_PERF).

[STOP AFTER] Press [STOP AFTER] to select stop after limit failure, stop after each measurement, or do not stop after a limit failure or measurement. If [LIMIT FAILURE] is selected, the program stops after the failing measurement is displayed, but before it is printed. At this point you can continue on and print the failing measurement or restart the measurement.

[BEEPER] Press [BEEPER] to toggle the beeper on the off. When the beeper is on, the program beeps approximately every 2 minutes while waiting for you to follow the directions on the display and press [CONTINUE].

[RETURN] Press [RETURN] to return to the main menu.

In the main menu of the ITM_35689 program press [TEST CONFIG] to display the test configuration and the following softkeys:

[PRINTER ADDRESS] Press [PRINTER ADDRESS] to enter the HP-IB address for the printer. To disable the printer, set the printer address to 0.

[PROCEDURE] Press [PROCEDURE] to select the HP 35689A operation verification procedure (A_OPVER), the HP 35689B operation verification procedure (B_OPVER), the HP 35689A performance test procedure (A_PERF), or the HP 35689B performance test procedure (B_OPVER).

[STOP AFTER] Press [STOP AFTER] to select stop after limit failure, stop after each measurement, or do not stop after a limit failure or measurement. If [Limit Failure] is selected, the program stops after the failing measurement is displayed, but before it is printed. At this point you can continue on and print the failing measurement or restart the measurement.

[BEEPER] Press [BEEPER] to toggle the beeper on the off. When the beeper is on, the program beeps approximately every 2 minutes while waiting for you to follow the directions on the display and press [CONTINUE].

[RETURN] Press [RETURN] to return to the main menu.

Equipment Configuration Menu

In the main menu of the ITM_3589A program press [EQUIP CONFIG] to display the test equipment configuration and the following softkeys:

Note

If you select [Other] for model, the program prompts you to type in a model, serial number, and calibration due date but not an HP-IB address.

When entering the calibration due date, only four characters are displayed on the screen. However, you can enter up to nine characters and they will be printed.

[SIGNAL GEN]	Press [SIGNAL GEN] to enter the model, serial number, HP-IB address, and calibration due date for the signal generator.
[SYNTH]	Press [SYNTH] to enter the model, serial number, HP-IB address, and calibration due date for the frequency synthesizer.
[SYNTH/LVL GEN]	Press [SYNTH/LVL GEN] to enter the model, serial number, HP-IB address, and calibration due date for the synthesizer/level generator.
[ANALYZER]	Press [ANALYZER] to enter the model, serial number, HP-IB address, and calibration due date for the analyzer.
[SAVE SETUP]	Press [SAVE SETUP] to save the current equipment configuration to a file for future recall.
[RECALL SETUP]	Press [RECALL SETUP] to recall an equipment configuration that was previously saved using [SAVE SETUP].
[MORE]	Press [MORE] to display the next page.
[RETURN]	Press [RETURN] to return to the main menu.
[MULTIMETER]	Press [MULTIMETER] to enter the model, serial number, HP-IB address, and calibration due date for the voltmeter.
[POWER METER]	Press [POWER METER] to enter the model, serial number, HP-IB address, and calibration due date for the power meter.
[POWER SENSOR]	Press [POWER SENSOR] to enter the model, serial number, and calibration due date for the power sensor.
[DIR BRIDGE]	Press [DIR BRIDGE] to enter the model, serial number, and calibration due date for the directional bridge.

[STEP ATTEN] Press [STEP ATTEN] to enter the model, serial number, calibration due date, and error correction data for the step attenuator.

[MORE] Press [MORE] to display the next page.

[RETURN] Press [RETURN] to return to the main menu.

[FREQ STD] Press [FREQ STD] to enter the model, serial number, and calibration due date for the frequency standard.

[mW-POWER METER] Press [mW-POWER METER] to enter the model, serial number, and calibration due date for the milliwatt power meter. This test instrument is not used in the alternate operation verification or alternate performance test procedures.

[21 MHz FILTER] Press [21 MHz FILTER] to enter the model, serial number, and calibration due date for the 21 MHz low pass filter.

[50 MHz FILTER] Press [50 MHz FILTER] to enter the model, serial number, and calibration due date for the 50 MHz low pass filter.

[MORE] Press [MORE] to display the first page.

[RETURN] Press [RETURN] to return to the main menu.

In the main menu of the ITM_35689 program press [EQUIP CONFIG] to display the test equipment configuration and the following softkeys:

[NETWORK ANALYZER] Press [NETWORK ANALYZER] to enter the model, serial number, and calibration due date for the HP 3589A Spectrum/Network Analyzer.

[Z0 TERMINATI] Press [Z0 TERMINATI] to enter the model, serial number, and calibration due date for the Z0 Termination.

[DIR BRIDGE] Press [DIR BRIDGE] to enter the model, serial number, and calibration due date for the directional bridge.

Title Page Menu

In the main menu of either the ITM_3589A or ITM_35689 program press [TITLE PAGE] to display the title page information and the following softkeys:

Note The title page information is printed at the beginning of the test procedure.

[TEST FACILITY]	Press [TEST FACILITY] to enter the name or number of the testing entity.
[FACILITY ADDRESS]	Press [FACILITY ADDRESS] to enter the address of the testing entity.
[TESTED BY]	Press [TESTED BY] to enter the name or number of the person performing the test.
[REPORT NUMBER]	Press [REPORT NUMBER] to enter the analyzer's report number.
[CUSTOMER]	Press [CUSTOMER] to enter the name or number of the person requesting the test.
[SERIAL NUMBER]	Press [SERIAL NUMBER] to enter the analyzer's serial number.
[MORE]	Press [MORE] to display the next page.
[RETURN]	Press [RETURN] to return to the main menu.
[OPTIONS]	Press [OPTIONS] to enter the analyzer's options.
[DATE]	Press [DATE] to enter the test date.
[TEMP]	Press [TEMP] to enter the temperature of the environment during the test.
[HUMIDITY]	Press [HUMIDITY] to enter the humidity of the environment during the test.
[LINE FREQUENCY]	Press [LINE FREQUENCY] to enter the power line frequency.
[MORE]	Press [MORE] to display the first page.
[RETURN]	Press [RETURN] to return to the main menu.

Measurement Uncertainty

Table 3-5. HP 3589A Measurement Uncertainty

Performance Test	Using Recommended Test Equipment		Using Other Test Equipment	
	Measurement Uncertainty	Ratio	Measurement Uncertainty	Ratio
Local Oscillator Feedthrough	NA[1]	NA[1]	NA[1]	NA[1]
Phase Noise	NA[1]	NA[1]	NA[1]	NA[1]
Residual Responses	NA[1]	NA[1]	NA[1]	NA[1]
Noise Level	NA[1]	NA[1]	NA[1]	NA[1]
Frequency Accuracy (following adjustment)	± 0.000003 ppm	>10:1		
Spurious Responses Typical scale fidelity Test signal spurious responses <120 MHz 120 to 150 MHz	 ± 0.25 dB <–90 dBc <–100 dBc	NA[2]		NA[2]
Image Responses Typical scale fidelity Test signal spurious responses <120 MHz 120 to 150 MHz	 ± 0.25 dB <–90 dBc <–100 dBc	NA[2]		NA[2]
Input Harmonic Distortion Typical scale fidelity Test signal harmonics	 ± 0.25 dB <–100 dBc	NA[2]		NA[2]
Intermodulation Distortion Typical scale fidelity Typical test signals distortion	 ± 0.25 dB <–86 dBc	NA[2]		NA[2]

[1] internal test
[2] open-ended specification
[3] root-sum-squares calculation method

Table 3-5. HP 3589A Measurement Uncertainty (continued)

Performance Test	Using Recommended Test Equipment		Using Other Test Equipment	
	Measurement Uncertainty	Ratio	Measurement Uncertainty	Ratio
Source Response				
10 Hz				
100 Hz	± 0.011 dB	>10:1		
1 kHz	± 0.010 dB	>10:1		
10 kHz	± 0.010 dB	>10:1		
30 kHz	± 0.011 dB	>10:1		
100 kHz	± 0.012 dB	>10:1		
300 kHz	± 0.017 dB	>10:1		
500 kHz	± 0.109 dB[3]	8.1:1		
1 MHz	± 0.109 dB[3]	8.1:1		
2 MHz	± 0.109 dB[3]	8.1:1		
5 MHz	± 0.109 dB[3]	8.1:1		
10 MHz	± 0.087 dB[3]	10:1		
25 MHz	± 0.089 dB[3]	9.9:1		
40 MHz	± 0.089 dB[3]	9.9:1		
55 MHz	± 0.092 dB[3]	9.6:1		
70 MHz	± 0.092 dB[3]	9.6:1		
85 MHz	± 0.092 dB[3]	9.6:1		
100 MHz	± 0.092 dB[3]	9.6:1		
120 MHz	± 0.098 dB[3]	9.1:1		
135 MHz	± 0.098 dB[3]	9.1:1		
150 MHz	± 0.098 dB[3]	9.1:1		
	± 0.098 dB[3]	9.1:1		
Amplitude Accuracy and Flatness				
50Ω				
10 to 100 Hz	± 0.035 dB	>10:1		
100 Hz to 30 kHz	± 0.035 dB	>10:1		
30 kHz to 50 MHz	± 0.035 dB	>10:1		
50 MHz to 100 MHz	± 0.045 dB	10:1		
100 MHz to 150 MHz	± 0.060 dB	>10:1		
1 MΩ				
10 to 100 Hz	± 0.035 dB	>10:1		
100 Hz to 30 kHz	± 0.035 dB	>10:1		
30 kHz to 40 MHz	± 0.035 dB	>10:1		

[1] internal test
[2] open-ended specification
[3] root-sum-squares calculation method

Table 3-5. HP 3589A Measurement Uncertainty (continued)

Performance Test	Using Recommended Test Equipment		Using Other Test Equipment	
	Measurement Uncertainty	Ratio	Measurement Uncertainty	Ratio
Alt_Amp Accuracy and Flatness				
50Ω				
10 Hz	± 0.011 dB	>10:1		
100 Hz	± 0.010 dB	>10:1		
1 kHz	± 0.010 dB	>10:1		
10 kHz	± 0.011 dB	>10:1		
30 kHz	± 0.012 dB	>10:1		
100 kHz	± 0.017 dB	>10:1		
300 kHz	± 0.109 dB[3]	3.5:1		
500 kHz	± 0.109 dB[3]	3.5:1		
1 MHz	± 0.109 dB[3]	3.5:1		
2 MHz	± 0.109 dB[3]	3.5:1		
5 MHz	± 0.097 dB[3]	3.9:1		
10 MHz	± 0.089 dB[3]	4.2:1		
25 MHz	± 0.089 dB[3]	4.1:1		
40 MHz	± 0.092 dB[3]	5.1:1		
55 MHz	± 0.092 dB[3]	5.1:1		
70 MHz	± 0.092 dB[3]	5.1:1		
85 MHz	± 0.092 dB[3]	4.8:1		
100 MHz	± 0.098 dB[3]	4.8 1		
120 MHz	± 0.098 dB[3]	4.8.1		
135 MHz	± 0.098 dB[3]	4.8:1		
150 MHz	± 0.098 dB[3]			
1 MΩ		>10:1		
10 Hz	± 0.011 dB	>10:1		
100 Hz	± 0.010 dB	>10:1		
1 kHz	± 0.010 dB	>10:1		
10 kHz	± 0.011 dB	>10:1		
30 kHz	± 0.012 dB	>10:1		
100 kHz	± 0.017 dB	5.1:1		
300 kHz	± 0.109 dB[3]	5.1:1		
500 kHz	± 0.109 dB[3]	5.1:1		
1 MHz	± 0.109 dB[3]	5.1:1		
2 MHz	± 0.109 dB[3]	6.4:1		
5 MHz	± 0.097 dB[3]	6.2:1		
10 MHz	± 0.089 dB[3]	6.2:1		
25 MHz	± 0.089 dB[3]	6.0:1		
40 MHz	± 0.092 dB[3]			
Reference Level Accuracy	± 0.036 dB	8:1		

[1] internal test
[2] open-ended specification
[3] root-sum-squares calculation method

Table 3-5. HP 3589A Measurement Uncertainty (continued)

Performance Test	Using Recommended Test Equipment		Using Other Test Equipment	
	Measurement Uncertainty	Ratio	Measurement Uncertainty	Ratio
Dynamic Accuracy –10 to –30 dB –40 dB –50 dB –60 dB –70 dB	 ± 0.02 dB ± 0.02 dB ± 0.03 dB ± 0.03 dB ± 0.03 dB	 4.9:1 7.4:1 >10:1 >10:1 >10:1		
Source Dynamic Accuracy 10 dB pad 20 dB pad	 ± 0.02 dB ± 0.02 dB	 9.8:1 >10:1		
Input Return Loss	± 0.9 dB	NA[2]		NA[2]
Source Return Loss	± 0.9 dB	NA[2]		NA[2]
Source Harmonic Distortion	± 2.5 dB	NA[2]		NA[2]
Source Spurious Responses	± 1.5 dB[3]	NA[2]		NA[2]
Source Noise	± 1.65 dB[3]	NA[2]		NA[2]

[1] internal test
[2] open-ended specification
[3] root-sum-squares calculation method

Table 3-6. HP 35689A/B Measurement Uncertainty

Performance Test	Using Recommended Test Equipment		Using Other Test Equipment	
	Measurement Uncertainty	Ratio	Measurement Uncertainty	Ratio
Directivity and Source Match	± 0 15dB	NA[1]		
Reflection	Magnatude ± 0.05dB Phase ± 1.0 deg	>10:1 5:1		
Transmission	Magnatude ± 0.05dB Phase ± 1.0 deg	>10:1 5:1		
Isolation	± 0.7dB	NA[1]		
Return Loss	± 0.9dB	NA[1]		

[1] open ended specification

HP 3589A Performance Test Record

Test Facility_____

Facility Address_____

Tested By_____

Report Number_____

Customer Name_____

Serial Number_____

Installed Options_____

Date_____

Temperature_____

Humidity_____

Power Line Frequency_____

Serial Number:_____Report Number:_____Test Date:__/__/__

Test Instruments Used

Instrument	Model	Trace Number	Cal Due
Signal Generator			
Synthesizer			
Synthesizer/Level Generator			
Analyzer			
Multimeter			
Power Meter			
Power Sensor			
Step Attenuator			
Directional Bridge			
21 MHz Filter			
50 MHz Filter			
Frequency Standard			
Milliwatt Power Meter			

Serial Number:_____ Report Number:_____ Test Date:___/___/___

Local Oscillator Feedthrough

Measurement	Upper Limit (dBm)	Measured Value (dBm)	Pass/Fail
Feedthrough, –20 dBm range	–40		

Phase Noise

Measurement	Upper Limit (dB/Hz)	Measured Value (dB/Hz)	Pass/Fail
1 kHz Offset	–105		

Residual Responses

Measurement	Upper Limit (dBm)	Measured Value (dBm)	Pass/Fail
60 Hz	–110		
120 Hz	–110		
180 Hz	–110		
12.5 kHz	–110		
24 7623 kHz	–110		
35 7134 kHz	–110		
100 kHz	–110		
187.5 kHz	–110		
250 kHz	–110		
10 MHz	–110		

Serial Number:_____Report Number:_____Test Date:__/__/__

Noise Level

Measurement	Upper Limit (dBm/Hz)	Measured Value (dBm/Hz)	Pass/Fail
50 ohm, 150 MHz	–132		
50 ohm, 140 MHz	–132		
50 ohm, 120 MHz	–132		
50 ohm, 71 MHz	–132		
50 ohm, 19 MHz	–132		
50 ohm, 5 3 MHz	–132		
50 ohm, 53 kHz	–132		
50 ohm, 5 3 kHz	–129		
50 ohm, 530 Hz	–124		
50 ohm, low distortion, 150 MHz	–122		
50 ohm, low distortion, 140 MHz	–122		
50 ohm, low distortion, 120 MHz	–122		
50 ohm, low distortion, 71 MHz	–122		
50 ohm, low distortion, 19 MHz	–122		
50 ohm, low distortion, 5 3 MHz	–122		
50 ohm, low distortion, 53 kHz	–122		
50 ohm, low distortion, 5.3 kHz	–119		
50 ohm, low distortion, 530 Hz	–114		
1 Mohm, 40 MHz	–110		
1 Mohm, 10.1 MHz	–110		
1 Mohm, 101 kHz	–110		
1 Mohm, 10.1 kHz	–100		
1 Mohm, 1.1 kHz	–90		
1 Mohm, 110 Hz	–80		

Frequency Accuracy

Measurement	Lower Limit (MHz)	Upper Limit (MHz)	Measured Value (MHz)	Pass/Fail
Accuracy @ 100 MHz				

Serial Number:_____ Report Number:_____ Test Date:__/__/__

Spurious Responses

Measurement	Upper Limit (dBc)	Measured Value (dBc)	Pass/Fail
Sum Reference, 10.8 MHz	–70		
Step combiner, 9 8 MHz	–70		
Step combiner, 149.8 MHz	–70		
API 1, 95.8125 MHz	–70		
API 1, 95.8129 MHz	–70		
API 1, 100.7925 MHz	–70		
API 1, 100 7929 MHz	–70		
API 2, 100.7925 MHz	–70		
API 3, 100.7925 MHz	–70		
API 4, 100.7925 MHz	–70		
Upper 3 MHz Sum Loop Sideband	–70		
Lower 3 MHz Sum Loop Sideband	–70		
Upper 10.123 kHz Sideband	–70		
Lower 10.123 kHz Sideband	–70		
100 kHz Sideband	–70		

Image Responses

Measurement	Upper Limit (dBc)	Measured Value (dBc)	Pass/Fail
40 MHz	–70		
60 MHz	–70		
61 MHz	–70		

Serial Number:_____Report Number:_____Test Date:__/__/__

Input Harmonic Distortion

Measurement	Upper Limit (dBc)	Measured Value (dBc)	Pass/Fail
47.265018 MHz, 2nd harmonic	–70		
47.265018 MHz, 3rd harmonic	–70		
47.265018 MHz, 2nd harmonic, low dist	–80		
47.265018 MHz, 3rd harmonic, low dist.	–80		
18.816541 MHz, 2nd harmonic	–70		
18.816541 MHz, 3rd harmonic	–70		
18.816541 MHz, 2nd harmonic, low dist.	–80		
18.816541 MHz, 3rd harmonic, low dist.	–80		
18.816541 MHz, 2nd harmonic, 1 Mohm	–65		

Serial Number:_____Report Number:_____Test Date:__/__/__

Intermodulation Distortion

Measurement	Upper Limit (dBc)	Measured Value (dBc)	Pass/Fail
2nd order sum, 134 Hz offset	–70		
2nd order difference, 134 Hz offset	–70		
3rd order, 134 Hz offset	–70		
2nd order sum, 2.841 kHz offset	–70		
2nd order difference, 2.841 kHz offset	–70		
3rd order, 2 841 kHz offset	–70		
2nd order sum, 60 kHz offset	–70		
2nd order difference, 60 kHz offset	–70		
3rd order, 60 kHz offset	–70		
2nd order sum, 134 Hz offset, low dist.	–80		
2nd order diff, 134 Hz offset, low dist.	–80		
3rd order, 134 Hz offset, low dist.	–80		
2nd order sum, 2.841 kHz offset, low dist.	–80		
2nd order diff, 2.841 kHz offset, low dist.	–80		
3rd order, 2.841 kHz offset, low dist	–80		
2nd order sum, 60 kHz offset, low dist.	–80		
2nd order diff, 60 kHz offset, low dist.	–80		
3rd order, 60 kHz offset, low dist.	–80		
2nd order, 134 Hz offset, 1 Meg Input	–65		
3rd order, 134 Hz offset, 1 Meg Input	–65		
2nd order, 2.841 kHz offset, 1 Meg Input	–65		
3rd order, 2.841 kHz offset, 1 Meg Input	–65		
2nd order, 60 kHz offset, 1 Meg Input	–65		
3rd order, 60 kHz offset, 1 Meg Input	–65		

Serial Number:_____Report Number:_____Test Date:__/__/__

Source Response †

Measurement	Lower Limit	Upper Limit	Measured Value	Pass/Fail
Source Accuracy @ 300 kHz	14 dBm	16 dBm	dBm	
Source Min. from 300 kHz	–1 dB	1 dB	dB	
Source Max. from 300 kHz	–1 dB	1 dB	dB	

† This test is not included in the ALT_PERF or ALT_OPVER procedure files.

Amplitude Accuracy and Flatness†

Measurement	Lower Limit (dBm)	Upper Limit (dBm)	Measured Value (dBm)	Pass/Fail
50 Ohm 30 kHz to 150 MHz maximum	–0.5	0.5		
50 Ohm 30 kHz to 150 MHz minimum	–0.5	0.5		
50 Ohm 300 kHz to 40 MHz maximum	–0.4	0.4		
50 Ohm 300 kHz to 40 MHz minimum	–0.4	0.4		
50 Ohm 100 Hz to 30 kHz maximum	–1	1		
50 Ohm 100 Hz to 30 kHz minimum	–1	1		
50 Ohm 10 Hz to 100 Hz maximum	–2.5	2.5		
50 Ohm 10 Hz to 100 Hz minimum	–2.5	2.5		
1 MOhm 30 kHz to 40 MHz maximum	–0.6	0.6		
1 MOhm 30 kHz to 40 MHz minimum	–0.6	0.6		
1 MOhm 100 Hz to 30 kHz maximum	–1.25	1.25		
1 MOhm 100 Hz to 30 kHz minimum	–1.25	1.25		
1 MOhm 10 Hz to 100 Hz maximum	–2.5	2.5		
1 MOhm 10 Hz to 100 Hz minimum	–2.5	2.5		

† This test is not included in the ALT_PERF or ALT_OPVER procedure files.

Serial Number:_____Report Number:_____Test Date:___/___/___

Alt_Amp Accuracy and Flatness†

Measurement	Lower Limit (dBm)	Upper Limit (dBm)	Measured Value (dBm)	Pass/Fail
Source Accuracy @ 300 kHz	14	16		
Source Min. from 300 kHz	–1	1		
Source Max. from 300 kHz	–1	1		
50 Ohm 30 kHz to 150 MHz maximum	–0.5	0 5		
50 Ohm 30 kHz to 150 MHz minimum	–0.5	0 5		
50 Ohm 300 kHz to 40 MHz maximum	–0.4	0 4		
50 Ohm 300 kHz to 40 MHz minimum	–0.4	0 4		
50 Ohm 100 Hz to 30 kHz maximum	–1	1		
50 Ohm 100 Hz to 30 kHz minimum	–1	1		
50 Ohm 10 Hz to 100 Hz maximum	–2 5	2 5		
50 Ohm 10 Hz to 100 Hz minimum	–2.5	2 5		
1 MOhm 30 kHz to 40 MHz maximum	–0 6	0.6		
1 MOhm 30 kHz to 40 MHz minimum	–0.6	0.6		
1 MOhm 100 Hz to 30 kHz maximum	–1.25	1 25		
1 MOhm 100 Hz to 30 kHz minimum	–1.25	1 25		
1 MOhm 10 Hz to 100 Hz maximum	–2.5	2.5		
1 MOhm 10 Hz to 100 Hz minimum	–2.5	2 5		

† This test is not included in the PERFORM or OP_VERIFY procedure files.

Reference Level Accuracy

Measurement	Lower Limit (dBm)	Upper Limit (dBm)	Measured Value (dBm)	Pass/Fail
–20 dBm range	–20.3	–19.7		
–10 dBm range	–10 3	–9.7		
0 dBm range	–0 3	0.3		
10 dBm range	9.7	10.3		
20 dBm range	19.7	20.3		

Serial Number:_____Report Number:_____Test Date:__/__/__

Dynamic Accuracy

Measurement	Lower Limit	Upper Limit	Measured Value	Pass/Fail
Amplitude @ –10 dB	–0 1 dB	0.1 dB	dB	
Phase @ –10 dB	–1 5 deg	1.5 deg	deg	
Amplitude @ –20 dB	–0 1 dB	0.1 dB	dB	
Phase @ –20 dB	–1 5 deg	1.5 deg	deg	
Amplitude @ –30 dB	–0 1 dB	0.1 dB	dB	
Phase @ –30 dB	–1.5 deg	1.5 deg	deg	
Amplitude @ –40 dB	–0 15 dB	0.15 dB	dB	
Phase @ –40 dB	–2 deg	2 deg	deg	
Amplitude @ –50 dB	–0 35 dB	0.35 dB	dB	
Phase @ –50 dB	–3 deg	3 deg	deg	
Amplitude @ –60 dB	–0.55 dB	0.55 dB	dB	
Phase @ –60 dB	–4 deg	4 deg	deg	
Amplitude @ –70 dB	–0 75 dB	0.75 dB	dB	
Phase @ –70 dB	–6 deg	6 deg	deg	

Serial Number:_____Report Number:_____Test Date:___/___/___

Source Dynamic Accuracy

Measurement	Lower Limit (dB)	Upper Limit (dB)	Measured Value (dB)	Pass/Fail
10 dB attenuator	–0.2	0.2		
10 dB DAC attenuator	–0.2	0.2		
20 dB A attenuator	–0.4	0.4		
20 dB B attenuator	–0.4	0.4		
20 dB DAC attenuator	–0.4	0.4		

Input Return Loss

Measurement	Upper Limit (dB)	Measured Value (dB)	Pass/Fail
20 dBm range, 100 MHz	–20		
10 dBm range, 100 MHz	–20		
0 dBm range, 100 MHz	–20		
-10 dBm range, 100 MHz	–20		
-20 dBm range, 100 MHz	–20		
20 dBm range, 150 MHz	–20		
10 dBm range, 150 MHz	–20		
0 dBm range, 150 MHz	–20		
-10 dBm range, 150 MHz	–20		
-20 dBm range, 150 MHz	–20		

Serial Number:_____ Report Number:_____ Test Date:___/___/___

Source Return Loss

Measurement	Upper Limit (dB)	Measured Value (dB)	Pass/Fail
15 dBm output, 60 MHz	–20		
5 dBm output, 60 MHz	–20		
-5 dBm output, 60 MHz	–20		
-15 dBm output, 60 MHz	–20		
-25 dBm output, 60 MHz	–20		
-35 dBm output, 60 MHz	–20		
15 dBm output, 120 MHz	–20		
5 dBm output, 120 MHz	–20		
-5 dBm output, 120 MHz	–20		
-15 dBm output, 120 MHz	–20		
-25 dBm output, 120 MHz	–20		
-35 dBm output, 120 MHz	–20		
15 dBm output, 150 MHz	–20		
5 dBm output, 150 MHz	–20		
-5 dBm output, 150 MHz	–20		
-15 dBm output, 150 MHz	–20		
-25 dBm output, 150 MHz	–20		
-35 dBm output, 150 MHz	–20		

Serial Number:_____Report Number:_____Test Date:___/___/___

Source Harmonic Distortion

Measurement	Upper Limit (dBc)	Measured Value (dBc)	Pass/Fail
100 kHz, 2nd harmonic	–28		
100 kHz, 3rd harmonic	–28		
1 MHz, 2nd harmonic	–28		
1 MHz, 3rd harmonic	–28		
10 MHz, 2nd harmonic	–28		
10 MHz, 3rd harmonic	–28		
50 MHz, 2nd harmonic	–28		
50 MHz, 3rd harmonic	–28		
75 MHz, 2nd harmonic	–28		

Serial Number:_____Report Number:_____Test Date:__/__/__

Source Spurious Responses

Measurement	Upper Limit (dBc)	Measured Value (dBc)	Pass/Fail
10.1875 MHz	–40		
101.1875 MHz	–40		
101.375 MHz	–40		
10.3875 MHz	–40		

Source Noise

Measurement	Upper Limit (dBc)	Measured Value (dBc)	Pass/Fail
8.0125 MHz, 512 Hz offset	–80		
8.0125 MHz, 2.56 kHz offset	–80		
8.0125 MHz, 12.801 kHz offset	–80		
8.0125 MHz, 64.006 kHz offset	–80		
8.0125 MHz, 320.031 kHz offset	–80		
8.0125 MHz, 1.600156 MHz offset	–80		
140.0125 MHz, 512 Hz offset	–80		
140.0125 MHz, 2.56 kHz offset	–80		
140.0125 MHz, 12.801 kHz offset	–80		
140.0125 MHz, 64.006 kHz offset	–80		
140.0125 MHz, 320.031 kHz offset	–80		
140.0125 MHz, 1.600156 MHz offset	–80		

HP 3589A Operation Verification Test Record

Test Facility _____

Facility Address _____

Tested By _____

Report Number _____

Customer Name _____

Serial Number _____

Installed Options _____

Date _____

Temperature _____

Humidity _____

Power Line Frequency _____

Serial Number:_____Report Number:_____Test Date:__/__/__

Test Instruments Used

Instrument	Model	Trace Number	Cal Due
Signal Generator			
Synthesizer			
Synthesizer/Level Generator			
Analyzer			
Multimeter			
Power Meter			
Power Sensor			
Step Attenuator			
Directional Bridge			
21 MHz Filter			
50 MHz Filter			
Frequency Standard			
Milliwatt Power Meter			

Serial Number:_____Report Number:_____Test Date:___/___/___

Local Oscillator Feedthrough

Measurement	Upper Limit (dBm)	Measured Value (dBm)	Pass/Fail
Feedthrough, –20 dBm range	–40		

Phase Noise

Measurement	Upper Limit (dB/Hz)	Measured Value (dB/Hz)	Pass/Fail
1 kHz Offset	–105		

Residual Responses

Measurement	Upper Limit (dBm)	Measured Value (dBm)	Pass/Fail
60 Hz	–110		
120 Hz	–110		
180 Hz	–110		
12.5 kHz	–110		
24.7623 kHz	–110		
35.7134 kHz	–110		
100 kHz	–110		
187.5 kHz	–110		
250 kHz	–110		
10 MHz	–110		

Serial Number:_____Report Number:_____Test Date:__/__/__

Noise Level

Measurement	Upper Limit (dBm/Hz)	Measured Value (dBm/Hz)	Pass/Fail
50 ohm, 150 MHz	–132		
50 ohm, 120 MHz	–132		
50 ohm, 19 MHz	–132		
50 ohm, 530 Hz	–124		
50 ohm, low distortion, 150 MHz	–122		
50 ohm, low distortion, 120 MHz	–122		
50 ohm, low distortion, 19 MHz	–122		
50 ohm, low distortion, 530 Hz	–114		
1 Mohm, 40 MHz	–110		
1 Mohm, 10.1 kHz	–100		
1 Mohm, 110 Hz	–80		

Frequency Accuracy

Measurement	Lower Limit (MHz)	Upper Limit (MHz)	Measured Value (MHz)	Pass/Fail
Accuracy @ 100 MHz				

Serial Number:_____Report Number:_____Test Date:___/___/___

Spurious Responses

Measurement	Upper Limit (dBc)	Measured Value (dBc)	Pass/Fail
Sum Reference, 10.8 MHz	–70		
Step combiner, 9.8 MHz	–70		
Step combiner, 149 8 MHz	–70		
API 1, 95.8125 MHz	–70		
API 1, 95.8129 MHz	–70		
API 1, 100.7925 MHz	–70		
API 1, 100.7929 MHz	–70		
API 2, 100.7925 MHz	–70		
API 3, 100.7925 MHz	–70		
API 4, 100.7925 MHz	–70		
Upper 3 MHz Sum Loop Sideband	–70		
Lower 3 MHz Sum Loop Sideband	–70		
Upper 10.123 kHz Sideband	–70		
Lower 10.123 kHz Sideband	–70		
Lower 100 kHz Sideband	–70		

Image Responses

Measurement	Upper Limit (dBc)	Measured Value (dBc)	Pass/Fail
40 MHz	–70		
60 MHz	–70		
61 MHz	–70		

Serial Number:_____Report Number:_____Test Date:__/__/__

Input Harmonic Distortion

Measurement	Upper Limit (dBc)	Measured Value (dBc)	Pass/Fail
47.265018 MHz, 2nd harmonic, low dist.	–80		
47.265018 MHz, 3rd harmonic, low dist	–80		
18.816541 MHz, 2nd harmonic, low dist.	–80		
18.816541 MHz, 3rd harmonic, low dist	–80		

Source Response†

Measurement	Lower Limit	Upper Limit	Measured Value	Pass/Fail
Source Accuracy @ 300 kHz	14 dBm	16 dBm	dBm	
Source Min. from 300 kHz	–1 dB	1 dB	dB	
Source Max. from 300 kHz	–1 dB	1 dB	dB	

† This test is not included in the ALT_PERF or ALT_OPVER procedure files.

Amplitude Accuracy and Flatness†

Measurement	Lower Limit (dBm)	Upper Limit (dBm)	Measured Value (dBm)	Pass/Fail
50 Ohm 30 kHz to 150 MHz Maximum	–0.5	0.5		
50 Ohm 30 kHz to 150 MHz Minimum	–0.5	0.5		
50 Ohm 300 kHz to 40 MHz Maximum	–0.4	0.4		
50 Ohm 300 kHz to 40 MHz Minimum	–0.4	0.4		
50 Ohm 100 Hz to 30 kHz Maximum	–1	1		
50 Ohm 100 Hz to 30 kHz Minimum	–1	1		
50 Ohm 10 Hz to 100 Hz Maximum	–2.5	2.5		
50 Ohm 10 Hz to 100 Hz Minimum	–2.5	2.5		

† This test is not included in the ALT_PERF or ALT_OPVER procedure files.

Serial Number:_____Report Number:_____Test Date:__/__/__

Alt_Amp Accuracy and Flatness†

Measurement	Lower Limit (dBm)	Upper Limit (dBm)	Measured Value (dBm)	Pass/Fail
Source Accuracy @ 300 kHz	14	16		
Source Min. from 300 kHz	–1	1		
Source Max. from 300 kHz	–1	1		
50 Ohm 30 kHz to 150 MHz maximum	–0.5	0.5		
50 Ohm 30 kHz to 150 MHz minimum	–0.5	0.5		
50 Ohm 300 kHz to 40 MHz maximum	–0.4	0.4		
50 Ohm 300 kHz to 40 MHz minimum	–0.4	0.4		
50 Ohm 100 Hz to 30 kHz maximum	–1	1		
50 Ohm 100 Hz to 30 kHz minimum	–1	1		
50 Ohm 10 Hz to 100 Hz maximum	–2.5	2.5		
50 Ohm 10 Hz to 100 Hz minimum	–2.5	2.5		

† This test is not included in the PERFORM or OP_VERIFY procedure files.

Reference Level Accuracy

Measurement	Lower Limit (dBm)	Upper Limit (dBm)	Measured Value (dBm)	Pass/Fail
–20 dBm Range	–20.3	–19.7		
–10 dBm Range	–10.3	–9.7		
0 dBm Range	–0.3	0.3		
10 dBm Range	9.7	10.3		
20 dBm Range	19.7	20.3		

Source Dynamic Accuracy

Measurement	Lower Limit (dB)	Upper Limit (dB)	Measured Value (dB)	Pass/Fail
10 dB attenuator	–0.2	0.2		
10 dB DAC attenuator	–0.2	0.2		
20 dB A attenuator	–0.4	0.4		
20 dB B attenuator	–0.4	0.4		
20 dB DAC attenuator	–0.4	0.4		

Serial Number:_____Report Number:_____Test Date:__/__/__

Source Harmonic Distortion

Measurement	Upper Limit (dBc)	Measured Value (dBc)	Pass/Fail
100 kHz, 2nd harmonic	–28		
100 kHz, 3rd harmonic	–28		
50 MHz, 2nd harmonic	–28		
50 MHz, 3rd harmonic	–28		

Source Spurious Responses

Measurement	Upper Limit (dBc)	Measured Value (dBc)	Pass/Fail
10.1875 MHz	–40		
101.1875 MHz	–40		
101.375 MHz	–40		
10.3875 MHz	–40		

Source Noise

Measurement	Upper Limit (dBc)	Measured Value (dBc)	Pass/Fail
8.0125 MHz, 512 Hz offset	–80		
8.0125 MHz, 64.006 kHz offset	–80		

HP 35689A/B Performance Test Record

Test Facility_____

Facility Address_____

Tested By_____

Report Number_____

Customer Name_____

Serial Number_____

Installed Options_____

Date_____

Temperature_____

Humidity_____

Power Line Frequency_____

Test Instruments Used

Instrument	Model	Trace Number	Cal Due
Spectrum/Network Analyzer			
Directional Bridge			
Z0 Termination			

Serial Number:_____Report Number:_____Test Date:___/___/___

Directivity and Source Match (HP 35689A)

Measurement	Upper Limit (dB)	Measured Value (dB)	Pass/Fail
Port 1 Directivity	–40		
Port 1 Source Match	–26		
Port 2 Directivity	–40		
Port 2 Source Match	–26		

Directivity and Source Match (HP 35689B)

Measurement	Upper Limit (dB)	Measured Value (dB)	Pass/Fail
Port 1 Directivity	–40		
Port 1 Source Match	–24		
Port 2 Directivity	–40		
Port 2 Source Match	–24		

Reflection

Measurement	Lower Limit	Upper Limit	Measured Value	Pass/Fail
S11 Magnitude	–1 dB	1 dB	dB	
S11 Phase	–5 deg	5 deg	deg	
S22 Magnitude	–1 dB	1 dB	dB	
S22 Phase	–5 deg	5 deg	deg	

Transmission

Measurement	Lower Limit	Upper Limit	Measured Value	Pass/Fail
S21 Magnitude	–1 dB	1 dB	dB	
S21 Phase	–5 deg	5 deg	deg	
S12 Magnitude	–1 dB	1 dB	dB	
S12 Phase	–5 deg	5 deg	deg	

Serial Number:_____ Report Number:_____ Test Date:___/___/___

Isolation

Measurement	Upper Limit (dB)	Measured Value (dB)	Pass/Fail
S21 Isolation	–90		
S12 Isolation	–90		

Return Loss

Measurement	Upper Limit (dB)	Measured Value (dB)	Pass/Fail
Input, S11	–20		
Input, S22	–20		
Input, Reference	–20		
Output, S11	–20		
Output, S22	–20		
Output, Reference	–20		

HP 35689A/B Operation Verification Test Record

Test Facility_____

Facility Address_____

Tested By_____

Report Number_____

Customer Name_____

Serial Number_____

Installed Options_____

Date_____

Temperature_____

Humidity_____

Power Line Frequency_____

Test Instruments Used

Instrument	Model	Trace Number	Cal Due
Spectrum/Network Analyzer			
Z0 Termination			

Serial Number:_____Report Number:_____Test Date:___/___/___

Directivity and Source Match (HP 35689A)

Measurement	Upper Limit (dB)	Measured Value (dB)	Pass/Fail
Port 1 Directivity	–40		
Port 1 Source Match	–26		
Port 2 Directivity	–40		
Port 2 Source Match	–26		

Directivity and Source Match (HP 35689B)

Measurement	Upper Limit (dB)	Measured Value (dB)	Pass/Fail
Port 1 Directivity	–40		
Port 1 Source Match	–24		
Port 2 Directivity	–40		
Port 2 Source Match	–24		

Reflection

Measurement	Lower Limit	Upper Limit	Measured Value	Pass/Fail
S11 Magnitude	–1 dB	1 dB	dB	
S11 Phase	–5 deg	5 deg	deg	
S22 Magnitude	–1 dB	1 dB	dB	
S22 Phase	–5 deg	5 deg	deg	

Transmission

Measurement	Lower Limit	Upper Limit	Measured Value	Pass/Fail
S21 Magnitude	–1 dB	1 dB	dB	
S21 Phase	–5 deg	5 deg	deg	
S12 Magnitude	–1 dB	1 dB	dB	
S12 Phase	–5 deg	5 deg	deg	

4

Troubleshooting the HP 3589A and HP 35689A/B

How to Use This Chapter

This chapter contains troubleshooting tests for the HP 3589A Spectrum/Network Analyzer and HP 35689A/B S-Parameter Test Set. These tests isolate most failures to the assembly. The tests include initial verification, power-on test, self tests, tests for miscellaneous failures, and tests for failing performance tests. Table 4-1 tells you which test to start with based on the failure. Each test either isolates the faulty assembly or sends you to another test.

Use the following steps to isolate failures to the assembly. See chapter 6, "Replacing Assemblies," to determine how to disassemble and assemble the instrument.

1. Review "Safety Considerations" and "Troubleshooting Hints."
2. Determine which troubleshooting test to start with by comparing the instrument's symptoms to the symptoms in "Choosing a Troubleshooting Test."
3. Follow the recommended troubleshooting procedure until you locate the faulty assembly.
4. Replace the faulty assembly and follow the directions in "What to Do After Replacing an HP 3589A Assembly" or "What to Do After Replacing an HP 35689A/B Assembly" in chapter 6, "Replacing Assemblies."

Safety Considerations

The HP 3589A Spectrum/Network Analyzer and HP 35689A/B S-Parameter Test Set are Safety Class 1 instruments (provided with a protective earth terminal). Although these instruments have been designed in accordance with international safety standards, this manual contains information, cautions, and warnings that must be followed to ensure safe operation and retain the instruments in safe operating condition. Service must be performed by trained service personnel who are aware of the hazards involved (such as fire and electrical shock).

Warning

Any interruption of the protective (grounding) conductor inside or outside the instrument, or disconnection of the protective earth terminal can expose operators to potentially dangerous voltages.

Under no circumstances should an operator remove any covers, screws, shields or in any other way access the interior of the HP 3589A Spectrum/Network Analyzer or HP 35689A/B S-Parameter Test Set. There are no operator controls inside the instruments.

Only fuses with the required current rating and of the specified type should be used for replacement. The use of repaired fuses or short circuiting the fuse holder is not permitted. Whenever it is likely that the protection offered by the fuse has been impaired, the instrument must be made inoperative and secured against any unintended operation.

When power is removed from the HP 3589A Spectrum/Network Analyzer, +11000 volts are present in the CRT for approximately 3 seconds. Be extremely careful when working in proximity to this area during this time. The high voltage can cause serious personal injury if contacted.

Caution

Do not connect or disconnect ribbon cables with the power switch set to ON (I). Power transients caused by connecting or disconnecting a cable can damage circuit assemblies.

Equipment Required

Tables 1-5 through 1-10 list the recommended equipment. Any equipment which meets the critical specifications given in the tables may be substituted for the recommended model.

Troubleshooting Hints

- Incorrect bias supply voltages can cause false diagnostic messages. Most troubleshooting procedures for the analyzer do not check the power supply voltages through the motherboard. If you suspect incorrect supply voltages to an assembly in the analyzer, use table 9-12 on page 9-24 and an extender board to check the voltages at the assembly.
- Cables can cause intermittent hardware failures.
- Noise or spikes in the power supply can cause the instrument to fail.
- Measurements in this chapter are only approximate (usually ± 1 dB or 10%) unless stated otherwise.
- Use chassis ground for all measurements in this chapter unless stated otherwise.
- Logic levels in this chapter are either TTL level high or TTL level low unless stated otherwise. Toggling signal levels continually change from one TTL level to the other.

Choosing a Troubleshooting Test

Use table 4-1 to determine which troubleshooting test to begin with. Test 1. Initial Verification checks the basics: power supply voltages, reset signals, and clocks. It then uses tests 2 through 8 to further isolate the failure. Test 9. Self Test runs all the analyzer's self tests. It then uses tests 10 through 31 to further isolate the failure. Test 32. Memory Battery checks the battery on the Memory assembly. Test 33. Fan Power determines if the fan is faulty. Test 34. Trigger/Gate determines the cause of HP-IB trigger and external trigger failures. Test 35. DIN Connector checks the fuse on the keyboard.

Note

If you abort a self test before the self test is finished, the analyzer may fail its calibration routine. To prevent this from happening press [**Preset**] or cycle power after you abort the self test.

The troubleshooting tests in this chapter assume only one independent failure. Multiple failures can cause false results.

Table 4-1. Troubleshooting Guide

Symptom	Troubleshooting Test
Screen blank Screen defective After power-on, >3 minutes before keys active No response when key is pressed Incorrect response when key is pressed	Test 1. Initial Verification
Calibration fails Performance test fails Local oscillator unlocked Intermittent failure HP-IB fails Test set fails	Test 9. Self Test
Nonvolatile states not saved after power cycled	Test 32. Memory Battery
Fan not running	Test 33. Fan Power
HP-IB trigger fails External trigger fails	Test 34. Trigger/Gate
External keyboard does not work	Test 35. DIN Connector

HP 3589A Initial Verification

Before starting Test 1. Initial Verification, check that the voltage selector switch on the rear of the analyzer is set for the local line voltage. Also check that the correct line fuse is installed in the rear panel fuse holder. For information on the voltage selector switch and the line fuse, see "HP 3589A Power Requirements" in chapter 2.

Test 1. Initial Verification

Use this test to check signals that are vital to the operation of the analyzer.

1. If the graticule appears after power-on but there is no response when keys are pressed, do the following:

   a. Set the power switch to STANDBY (⏻).

   b. Set the power switch to ON (I) and as soon as the graticule appears, disable the calibration routine by pressing the following keys:

      [F9]
      [F9]

      [**Special Fctn**]
      [AUTO CAL ON **OFF**]

   c. If the keys responded correctly, go to Test 10. All Locks Analyzer.

2. Set the power switch to STANDBY (⏻) and disconnect the power cord from the rear panel. Remove the top cover, place the Power Supply assembly in its test position, and remove the Memory assembly (see figures 6-2 through 6-5 in chapter 6, "Replacing Assemblies").

Caution

Do NOT remove earth ground (green/yellow wire) from the Power Supply assembly or the analyzer's chassis.

3. Disconnect the CPU power cable (W2) from J1 on the CPU assembly. Disconnect the motherboard power cable (W12) from J2 on the Power Supply assembly (see figure 4-1).

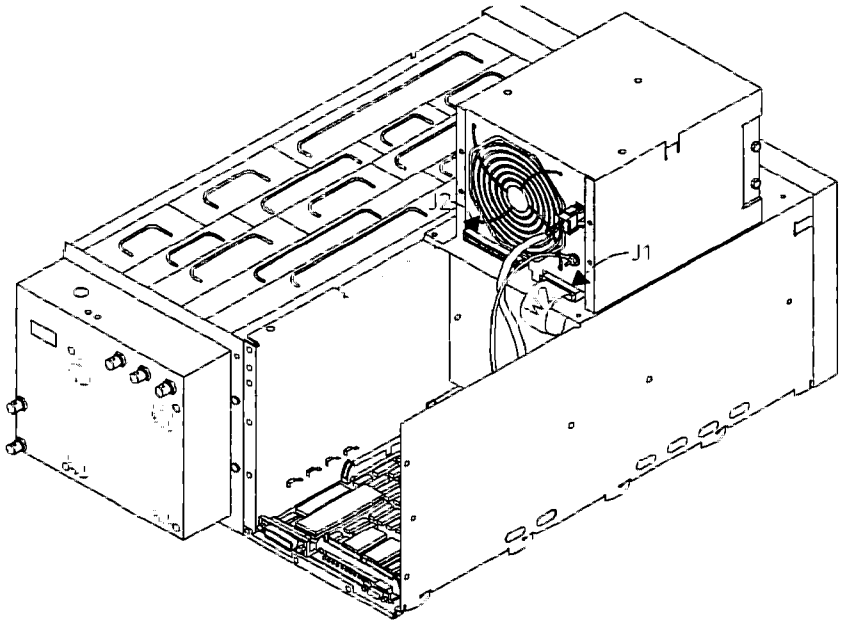


Figure 4-1. Connecting Test Board

4. Connect the power supply test board (from the service kit) to the CPU power cable (W2) and to J2 on the Power Supply assembly. Be careful not to short the test board to the analyzer's chassis.

Warning **The power supply test board dissipates high power from the Power Supply assembly. Be careful of the heat from the shield.**

---

5. Connect the power cord and set the power switch to ON (|). Check the voltages in table 4-2. There are no adjustments in the Power Supply assembly; therefore, if any of the voltages are incorrect replace the entire assembly.

Warning **If the Power Supply assembly is replaced, reattach the earth ground (green/yellow wire) from the Power Supply assembly to the analyzer's chassis to assure shock protection for the user.**

Table 4-2. Test Board Nominal Voltage Values

Test Location	Nominal Voltage	Minimum Voltage	Maximum Voltage	Ripple Tolerance
TP1	+8.4V	+7.9V	+10.5V	84 mVpp
TP2	+15V	+14.55V	+15 45V	30 mVpp
TP3	+18V	+18V	+27V	180 mVpp
TP4	-15V	-14.55V	-15.45V	30 mVpp
TP5	-18V	-18V	-27V	180 mVpp
TP6	+12V	+11.4V	+12.6V	120 mVpp
TP7	+5.1V	+4.84V	+5.36V	51 mVpp

6. Set the power switch to STANDBY (⏻). Disconnect the power supply test board. Reconnect the CPU power cable (W2) to J1 on the CPU assembly and the motherboard power cable (W12) to the Power Supply assembly. Replace the Memory assembly.

7. Set the power switch to ON (I). Check the voltages in table 4-3 (see figure 4-2).

Table 4-3. Initial Verification Nominal Voltage Values

Test Location	Signal Name	Nominal Voltage	Minimum Voltage	Maximum Voltage
A81 TP102	+5V	+5.1V	+4 845V	+5.355V
A81 TP103	+12V	+12V	+11.4V	+12.6V
A81 TP104	-11V	-11V	-10.45V	-11.55V

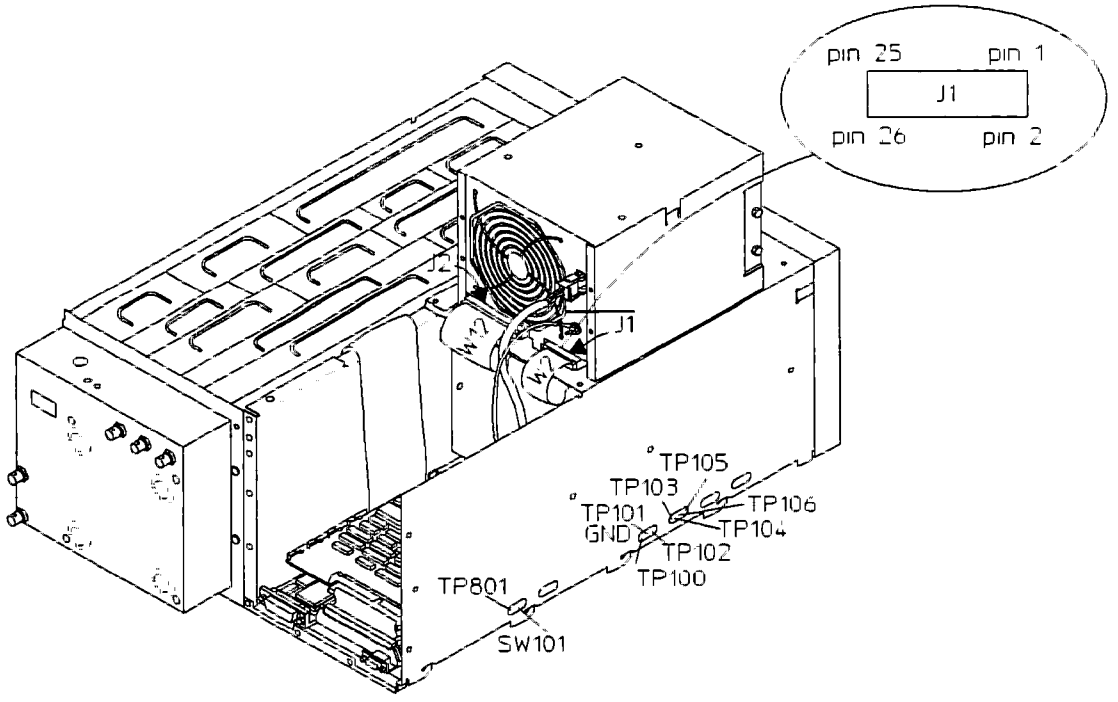


Figure 4-2. Initial Verification Test Locations

8. If the voltages are correct, go to step 9. If the voltages are incorrect, do the following:

   a. Set the power switch to STANDBY (⏻). Remove the Memory assembly.

   b. Disconnect all cables from the CPU assembly except the CPU power cable (W2). Disconnect the motherboard power cable (W12) from the Power Supply assembly.

   c. Set the power switch to ON (I). Check the voltages in table 4-3. If the voltages are incorrect, the CPU assembly is probably faulty.

   d. If the voltages are correct, set the power switch to STANDBY (⏻), reconnect one cable, set the power switch to ON (I), and check the voltages in table 4-3 again. Repeat this step until the faulty assembly or assemblies are located.

   e. If the failure occurs when the motherboard power cable (W12) is reconnected, set the power switch to STANDBY (⏻), remove one assembly from the card nest, set the power switch to ON (I), and check the voltages in table 4-3. If the voltages are still incorrect, repeat this step until the faulty assembly is located.

Note

Table 9-1, Power Supply Voltage Distribution, lists which assemblies use each voltage. Use the table to determine which assembly could be causing the failure.

Note

Both the A24 Step VCO assembly and the A41 Source Amplifier assembly have over-temperature protection circuits. These circuits force the power supply output voltages to zero if the analyzer's internal temperature becomes excessive. Before replacing either of these assemblies, make sure both fans are working properly and that the air flow is not restricted (cooling air enters from both sides and exhausts through the rear panel).

---

9. On the CPU assembly, attach a logic probe to TP100 (RST\).

10. While monitoring TP100, press SW101 (reset switch). If the logic level at TP100 went from high to low, go to step 11. If the logic level at TP100 did not go from high to low, do the following:

    a. Set the power switch to STANDBY (⏻). Disconnect the CPU power cable (W2) from J1 on the Power Supply assembly.

    b. Set the power switch to ON (I). With a logic probe, check J1 pin 13 (PVALID) on the Power Supply assembly for a TTL logic high (see figure 4-2). If the signal is incorrect, the Power Supply assembly is faulty.

    c. Set the power switch to STANDBY (⏻). Reconnect the CPU power cable. On the CPU assembly, attach a logic probe to TP100 and attach a jumper to TP801 (PVALID).

    d. Set the power switch to ON (I). While monitoring TP100, momentarily connect TP801 to chassis ground. If the logic level at TP100 did not go from high to low, the CPU assembly is probably faulty.

11. Using an oscilloscope and a 1 M Ω 10:1 probe, check the clock signals in figure 4-3.

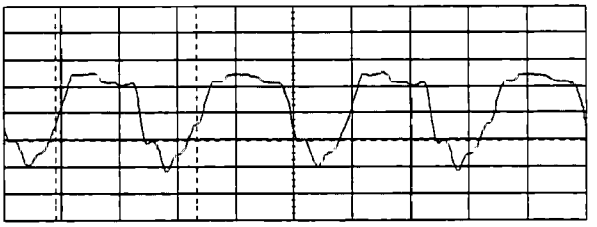
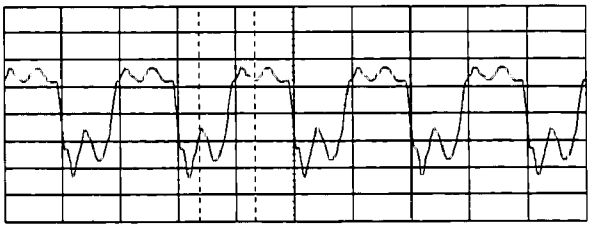
Oscilloscope Setup	Parameters	Waveform
Connect CH1 to A81 TP105 Connect GND to A81 TP101 CH1 V/div 2 V/div Input Impedance 1 M Ω CH1 Coupling dc Probe Atten 10 Display Mode Repetitive Averaging 8 Time/div 20 ns/div Trigger Auto	Time Duty Cycle	 **20 MHz (A81 OUT)**
Connect CH1 to A81 TP106 CH1 V/div 2 V/div Input Impedance 1 M Ω CH1 Coupling dc Probe Atten 10 Display Mode Repetitive Averaging 8 Time/div 50 ns/div Trigger Auto	Time Duty Cycle	 **10 MHz (A81 OUT)**

Figure 4-3. A81 CPU Clock Signals

12. Connect a 10:1 resistive divider probe with 500 Ω input resistance to an oscilloscope. Connect the probe to a dc blocking capacitor. Connect the blocking capacitor to A31 J8. Check the clock signal in figure 4-4.

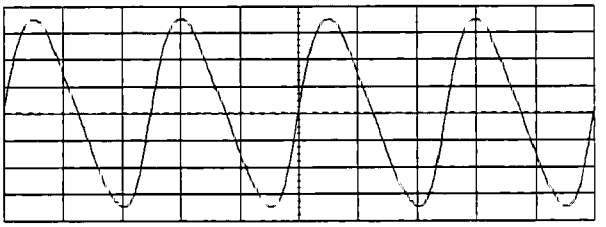
Oscilloscope Setup		Parameters	Waveform
Connect CH1 to A31 J8		Time Duty Cycle	 80 MHz (A31 OUT)
CH1 V/div	100 mV/div		
CH1 Coupling	dc		
CH1 Input Impedance	50 Ω		
Probe Atten	10		
Display Mode	Repetitive		
Averaging	8		
Time/div	5 ns/div		
Trigger	CH1		
Trigger level	0 V		

Figure 4-4. 80 MHz Reference Signals

13. If the signals in figures 4-3 and 4-4 are correct, go to Test 2. Power-on.

14. If the signal in figure 4-4 is incorrect, the Reference/Calibrator assembly is probably faulty.

15. Set the power switch to STANDBY (⏻). Disconnect the fast bus cable (W11) from J5 on the A62 ADC/Digital Filter assembly.

16. Set the power switch to ON (I). Check the signals in figure 4-3 again. If the signals are now correct, the ADC/Digital Filter assembly's EXT_CLK signal is probably faulty. If the signals are still incorrect, the CPU assembly is probably faulty.

Troubleshooting the HP 3589A Using the Power-On Test

Note Test 1. Initial Verification must be done before the power-on test messages are valid.

Use the power-on test when the screen is defective, when the analyzer does not respond correctly to the keyboard, or when it takes more than 3 minutes for the keyboard to become active. Any of the following conditions may cause a power-on failure:

- A defective CPU or Memory assembly.
- A defective assembly connected to the CPU assembly causing a bus failure.
- A defective cable between the CPU assembly and another assembly.
- A defective control line.

Test 2. Power-on

If Test 1. Initial Verification did not detect any problems, use this test to continue troubleshooting. This test points you to one of the following tests:

- Test 3. CPU, Memory, and Buses
- Test 5. Display
- Test 6. IIC Bus
- Test 7. Fast Bus

Note The Power Supply assembly is in its test position.

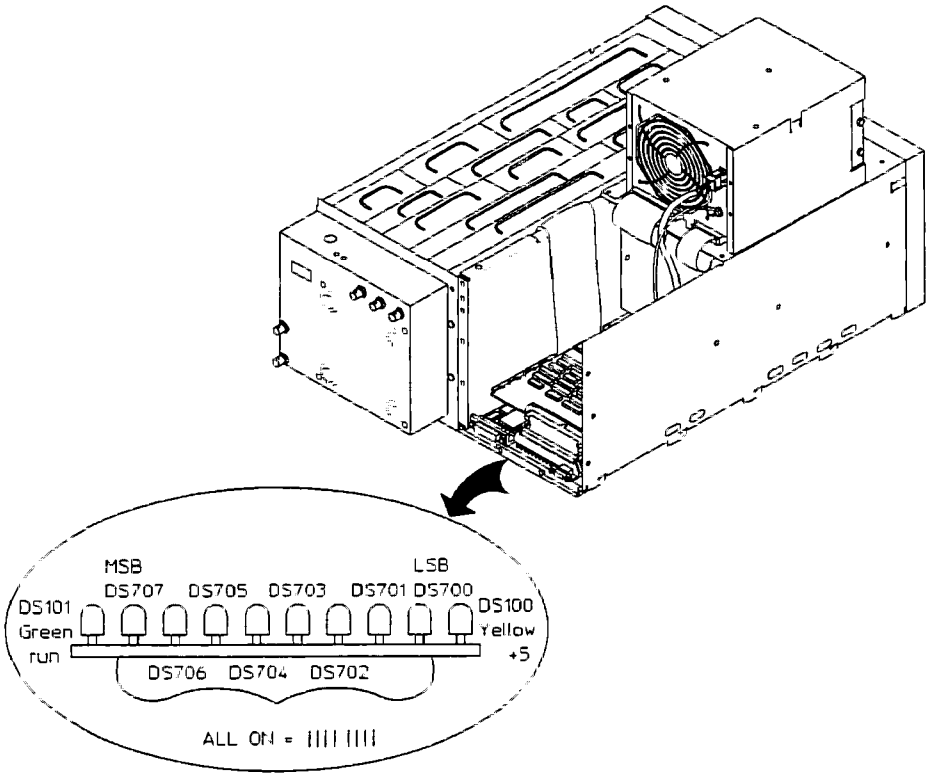


Figure 4-5. Power-on Test LEDs

1. Set the power switch to ON (I). On the CPU assembly, press SW101 (reset switch) while watching the power-on test LEDs (see figure 4-5). The power-on test LEDs pass sequence occurs if the LEDs respond as follows:
   - All power-on test LEDs are on momentarily as soon as SW101 is released.
   - DS100 (yellow, +5 LED) remains on as long as power is applied to the assembly.
   - DS101 (green, run LED) comes on as soon as SW101 is released.
   - DS707 through DS700 sequence through the codes listed in the table 4-4.

Table 4-4. Power-on Test Pass Sequence

Binary 0 = LED off 1 = LED on (DS707) (DS700)	Hexadecimal	~Time LEDs Visible	Description
0000 1000	08	*	starting LED DSACK test
1111 1111 0000 0000	FF 00	200 ms on 200 ms off	A81 flashes LEDs
0001 0011	13	*	starting A81 test
0001 0100	14	*	starting boot ROM checksum test
0000 1010	0A	*	starting display DSACK test
0001 0000	10	*	starting display test
0000 0001	01	*	starting A87 RAM DSACK test
0001 0111	17	*	starting A87 RAM size test
0001 1000	18	3s	starting A87 RAM bit test
0001 1001	19	3s	starting A87 refresh test
0001 1100	1C	5s	starting A87 program ROM test
0000 0000	00	4s	clear LEDs
1010 0001	A1	*	fast bus test
0000 0000	00	Remain off	clear LEDs

* When no failure occurs, these codes appear for only a very short time and probably won't be visible.

Note

See table 10-1 on page 10-2 for binary to hexadecimal conversion. For a complete list of the power-on test messages, see table 10-2 on page 10-3.

2. If a failure occurs in the core assemblies or on the buses, the power-on test pauses and LEDs DS707 through DS700 show a fail code for approximately 10 seconds. Compare your power-on test results to table 4-5 and follow the recommended troubleshooting test.

Table 4-5. Power-on Test Results

LEDs Sequence Results	Troubleshooting Test
LEDs show a fail code. A81 DS101 (green run LED) is off.	Test 3. CPU, Memory, and Buses
LEDs pass sequence occurs, but the screen is defective.	Test 5. Display
LEDs pass sequence occurs, but it takes more than 3 minutes before the keys are active. LEDs pass sequence occurs and screen appears normal, but keys do not function	Test 6. IIC Bus

Test 3. CPU, Memory, and Buses

Use this test to isolate the failure when the power-on test LEDs show a fail code.

Note The Power Supply assembly is in its test position.

---

1. Set the power switch to STANDBY (⏻). Remove the Memory assembly.
2. Disconnect the display cable (W3), front-panel cable (W5), and fast bus cable (W11) from J4, J3 and J6 on the CPU assembly. Disconnect the motherboard power cable (W12) from J2 on the Power Supply assembly (see figure 4-6).

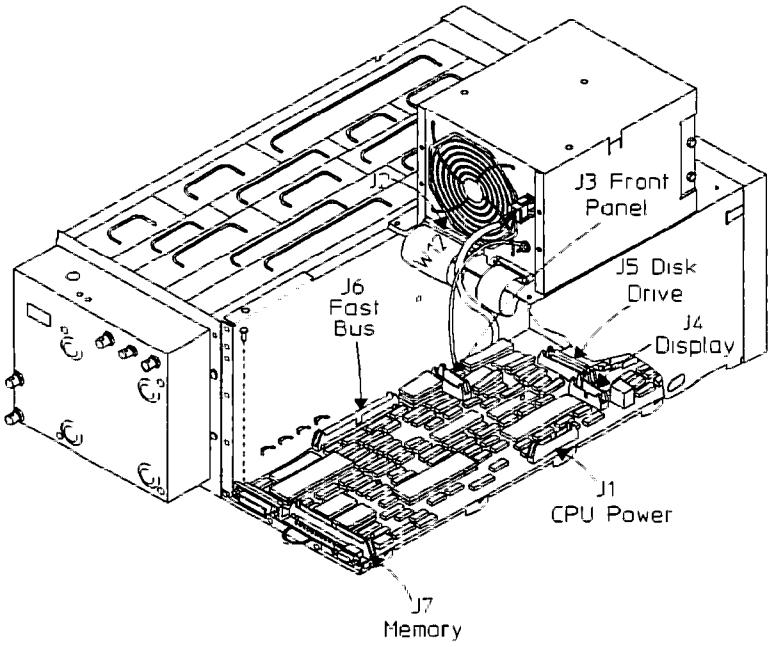


Figure 4-6. Cable Locations

3. Set the power switch to ON (I). On the CPU assembly, press SW101 (reset switch) while monitoring the power-on test LEDs (see figure 4-5). The LEDs display codes hexadecimal FF (1111 1111), briefly hexadecimal 14 (0001 0100), then hexadecimal 01 (0000 0001). If the LEDs do not respond correctly, the CPU assembly is faulty.

4. Set the power switch to STANDBY (⏻). Reconnect the Memory assembly with the assembly upside-down and outside the chassis. Be careful not to short the pins on back of the assembly.
5. Set the power switch to ON (I). Press SW101 while monitoring the power-on test LEDs. The LEDs pass sequence should occur with the final code hexadecimal A1 (1010 0001) remaining on the LEDs.
6. If the analyzer did not respond correctly, go to test 4. Memory.
7. Set the power switch to STANDBY (⏻). Connect the display cable (W3) to J4 on the CPU assembly.
8. Set the power switch to ON (I). Press SW101 while monitoring the power-on test LEDs and display. The LEDs pass sequence should occur with the final code hexadecimal A1 (1010 0001) remaining on the LEDs. The screen should display the message Booting System.
9. If the analyzer did not respond correctly, go to test 5. Display.
10. Set the power switch to STANDBY (⏻). Connect the front-panel cable (W5) to J3 on the CPU assembly and the motherboard power cable (W12) to J2 on the Power Supply assembly.
11. Set the power switch to ON (I). Press SW101 while monitoring the power-on test LEDs and the display. The LEDs pass sequence should occur with the final code hexadecimal A1 (1010 0001) remaining on the LEDs. The screen should display the message Booting System.
12. If the analyzer did not respond correctly, go to Test 6. IIC Bus.
13. Set the power switch to STANDBY (⏻). Connect the fast bus cable (W11) to J6 on the CPU assembly.
14. Set the power switch to ON (I), and monitor the power-on test LEDs.
15. If the LEDs show final code hexadecimal A1 (1010 0001), go to Test 7. Fast Bus.
16. If the failure still is not isolated, go to Test 6. IIC Bus.

Test 4. Memory

Use this test to separate Memory assembly failures from CPU assembly failures.

Note

The Power Supply assembly is in its test position. The motherboard power cable (W12) is disconnected from J2 on the Power Supply assembly. The Memory assembly is upside-down and outside the chassis. On the CPU assembly, the display cable (W3), the front-panel cable (W5), and the fast bus cable (W11) are disconnected.

1. Set the power switch to STANDBY (⏻). Disconnect the memory cable (W1) from J7 on the CPU assembly.
2. Set the power switch to ON (I). Using a logic probe, check that the signals listed in table 4-6 are toggling (see figure 4-7). If the signals are toggling, the Memory assembly is probably faulty.

Table 4-6. Memory Signals

Test Location	Signal Name	In/Out
A81 TP107	AS	A81 Out
A81 TP108	UDS	A81 Out
A81 TP109	LDS	A81 Out
A81 TP110	RW	A81 Out

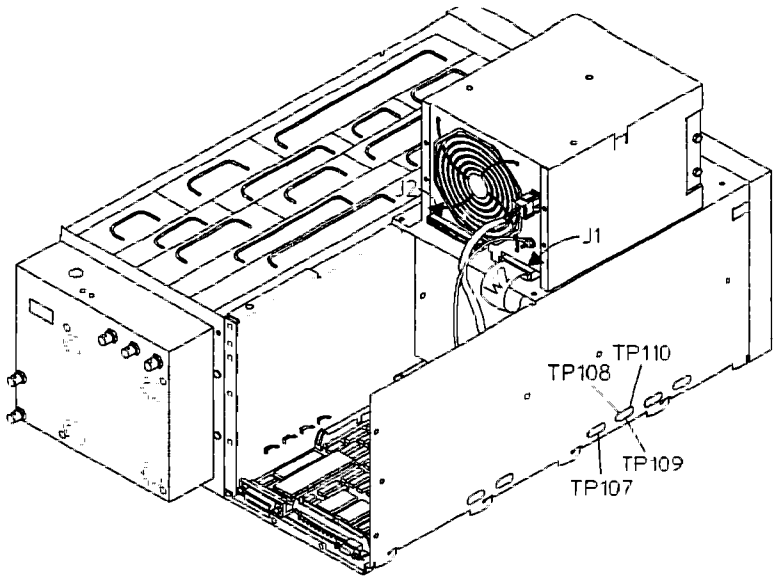


Figure 4-7. Memory Test Locations

Test 5. Display

Use this test to separate Display assembly failures from CPU assembly failures.

Note

The Power Supply assembly is in its test position. The motherboard power cable (W12) is disconnected from J2 on the Power Supply assembly. The Memory assembly is upside-down and outside the chassis. On the CPU assembly, the front-panel cable (W5) and the fast bus cable (W11) are disconnected.

1. Set the power switch to ON (|). Using a logic probe, check that the signals listed in table 4-7 are toggling (see figure 4-8 for test pin locations).

Table 4-7. Display Signals

Test Location	Signal Name	In/Out
A81 TP114	HB	A81 Out
A81 TP115	V SYNC	A81 Out
A81 TP116	H Sync	A81 Out

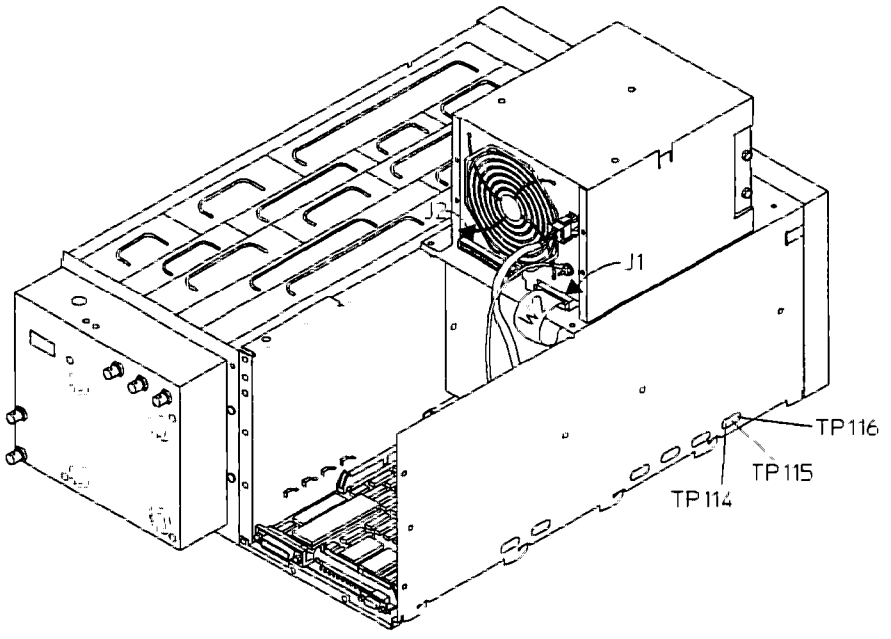


Figure 4-8. Display Controller Test Locations

2. If the signals are incorrect, do the following:

   a. Set the power switch to STANDBY (⏻). Disconnect the display cable (W3) from J4 on the CPU assembly.

   b. Set the power switch to ON (I). Check the signals again. If all the signals are now correct, the Display assembly is probably faulty.

3. Compare your screen to the typical symptoms listed in table 4-8.

Table 4-8. Display Test Troubleshooting Guide

Symptom	Probable Cause
Vertical and horizontal scanning is occurring. Part of information is missing, for example only half letters. Blocks of information are missing. Information on the screen is scrambled or mixed up. Vertical or horizontal stripes appear across the screen.	DRAM sub-block is failing on the CPU assembly.
Screen is blank. Screen is tilted, compressed, or distorted. Line across the screen.	Display assembly is failing.

Note Before replacing the Display assembly, do adjustment 18, "Display," in chapter 5.

4. If the failure still is not isolated, check the CPU assembly's control signals in Test 8. Control Lines.

Test 6. IIC Bus (Inter-IC Bus)

Use this test to isolate IIC bus failures to one of the following assemblies:

- Front Panel
- A11 Input
- A23 Step Phase Detector
- A31 Reference/Calibrator
- A33 Trigger
- A41 Source Amplifier
- A42 Source Conversion
- A51 Interpolation VCO
- A52 Fractional-N
- A62 ADC/Digital Filter
- A81 CPU

Note

The Power Supply assembly is in its test position. The Memory assembly is upside-down and outside the chassis. On the CPU assembly, the fast bus cable (W11) is disconnected.

---

1. Set the power switch to STANDBY (⏻). Connect the fast bus cable (W11) to the CPU assembly.
2. Disconnect the front-panel cable (W5) from J3 on the CPU assembly and the motherboard power cable (W12) from J2 on the Power Supply assembly.
3. On the CPU assembly, attach a logic probe to TP600 (IIC Serial Clock).
4. Set the power switch to ON (I). Press SW101 (reset switch) while monitoring TP600 (SCL) and the power-on test LEDs (see figure 4-9). If the CPU assembly is operating correctly, the TTL logic level at TP600 toggles when SW101 is released and a couple of times when 00 is displayed.
5. Attach the logic probe to TP601 (IIC Serial Data). Press SW101 while monitoring TP601 (SDA) and the power-on test LEDs. If the CPU assembly is operating correctly, the logic level at TP601 toggles when SW101 is released and a couple of times when 00 is displayed.
6. Set the power switch to STANDBY (⏻). Connect the front-panel cable (W5) to J3 on the CPU assembly.

7. Repeat steps 3, 4, and 5 to check that the front panel is not causing the failure.
8. Set the power switch to STANDBY (⏻). Connect the motherboard power cable (W12) to J2 on the Power Supply assembly.

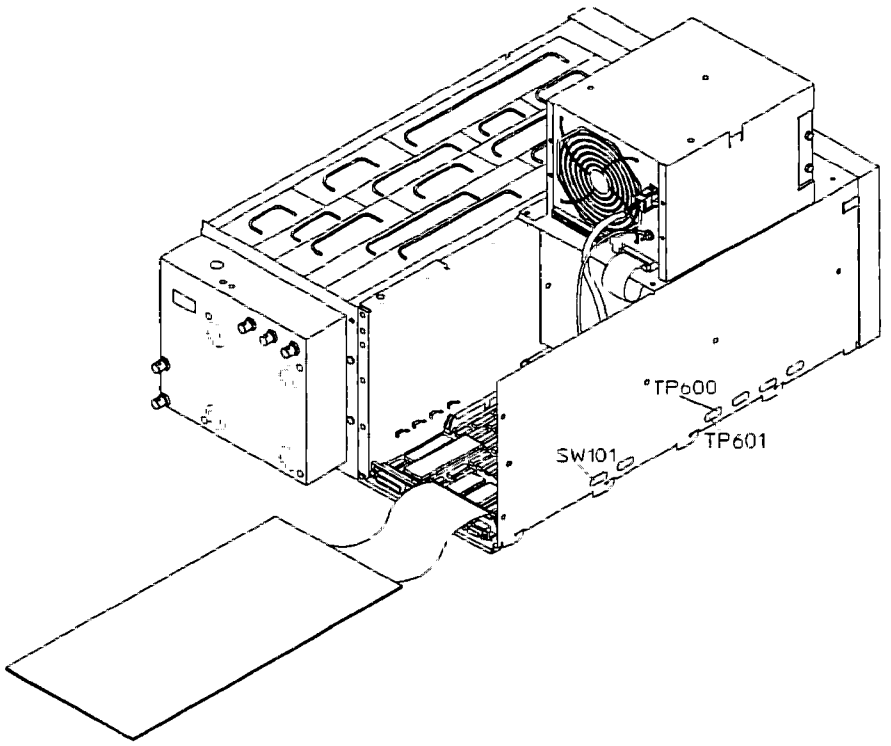


Figure 4-9. IIC Bus Test Locations

9. Set the power switch to ON (I). Press any key. If the analyzer did not respond, do the following:
   a. Set the power switch to STANDBY (⏻) and remove one of the following assemblies:
      A11 Input
      A23 Step Phase Detector
      A31 Reference/Calibrator
      A33 Trigger
      A41 Source Amplifier
      A42 Source Conversion
      A51 Interpolation VCO
      A52 Fractional-N
   b. Set the power switch to ON (I), then press any key. If the analyzer responds, the assembly just removed is probably faulty.

Note

Press a key before the calibration routine starts. The calibration routine may lock the front panel when an assembly is removed.

c. If the analyzer did not respond, repeat steps a and b until the faulty assembly is located.

10. If the failure still is not isolated, go to Test 7. Fast Bus.

Test 7. Fast Bus

Use this test to isolate fast bus failures to the CPU assembly, the ADC/Digital Filter assembly, or the fast bus cable.

Note

The Power Supply assembly is in its test position. The Memory assembly is upside-down and outside the chassis. The motherboard power cable (W12) is disconnected from the Power Supply assembly.

---

1. Set the power switch to STANDBY (⏻). Disconnect the fast bus cable (W11) from J5 on the ADC/Digital Filter assembly.
2. On the CPU assembly, set SW100 pin 4 and pin 6 to one (see figure 4-10).
3. Set the power switch to ON (I). The screen displays Fast Bus Toggle Test in progress.... Also the power-on test LEDs alternately flash hexadecimal AA (DS707, DS705, DS703, and DS701 are on) and hexadecimal 55 (DS706, DS704, DS702, and DS700 are on). If the analyzer did not respond correctly, the CPU assembly is probably faulty.
4. Using a logic probe, check the signals in table 4-9 at the fast bus cable. If the signals are correct, the ADC/Digital Filter assembly is probably faulty.

Note

The Fast Bus Toggle Test exercises most, but not all of the fast bus lines from the CPU assembly.

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5. If any of the signals are incorrect, disconnect the fast bus cable from the CPU assembly. Check the failing signals at J6 on the CPU assembly. If the signals are still incorrect, the CPU assembly is faulty.

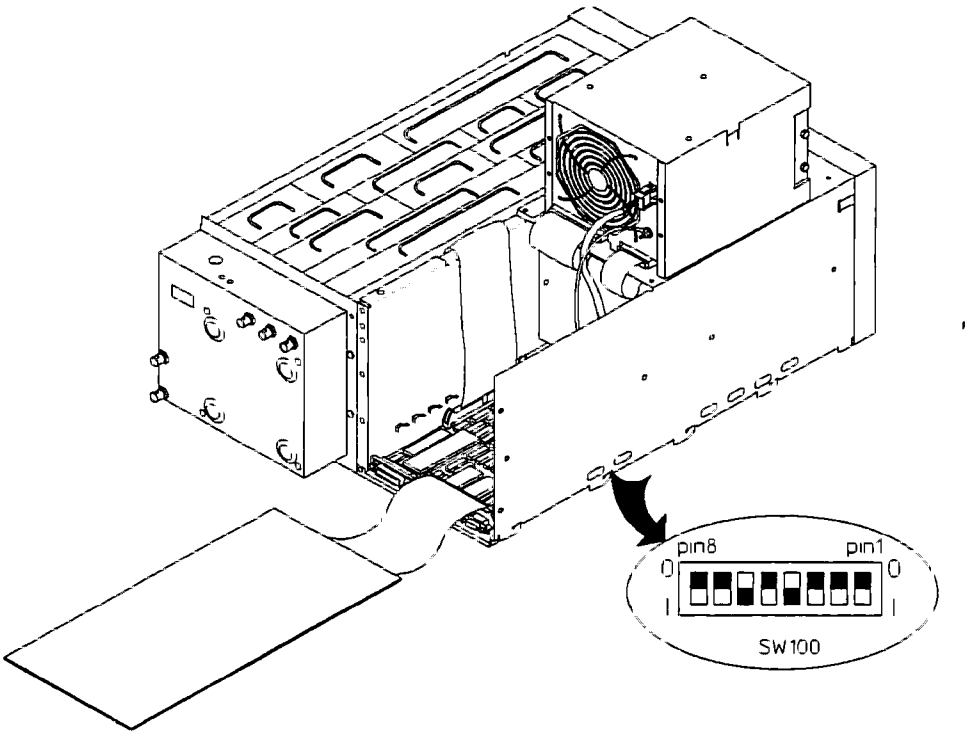

Figure 4-10. Switch Setting for Fast Bus Test

Table 4-9. Fast Bus Lines

Pin	Signal Name	TTL Logic State In Test Mode
1 to 31 odd	FD0 - FD15	Toggling
33 to 41 odd	FA1 - FA5	Toggling
43	FIRQ\	High
45	FRW	Toggling
47	SELA\	High
49	SELS\	Toggling
51	FDTACK\	High
53	ECLK	Toggling
55	REQ0\	High
57	ACK0\	High
59	PCL0\	High
61	DTC\	High
63	EXT_CLK	High
2 to 64 even	GND	Low

Test 8. Control Lines

Control line failures can cause false error codes and multiple failure messages. Table 4-10 lists the active state for each control line. The assembly listed in the table as the "Probable Faulty Assembly" is listed with the assumption that no other assembly is loading the line.

1. Set the power switch to STANDBY (⏻). Reinstall all assemblies and cables that were removed during troubleshooting. On the CPU assembly, check that all pins of SW100 are set to zero.

2. Set the power switch to ON (I). Check the signals in table 4-10 with a logic probe or oscilloscope (see figure 4-11).

Table 4-10. Data and Control Lines

Test Location	Signal Name	In/Out	Logic Level During Power-on	Logic Level After Power-on	Probable Faulty Assembly
A81 TP107	AS\	A81 Out	Toggling	Toggling	A81
A81 TP108	UDS\	A81 Out	Toggling	Toggling	A81
A81 TP109	LDS\	A81 Out	Toggling	Toggling	A81
A81 TP110	FRW	A81 Out	Toggling	Toggling	A81
A81 TP111	DTACK	A62, A87	Toggling	Toggling	A62, A81, A87
A81 TP112	BGACK\	A81 Internal	High	Toggling	A81
A81 TP113	BERR\	A81 Internal	High	High	Any
A81 TP600	SCL	A81 Out	High	Toggling	A81
A87 TP102	RAS1\	A87 Internal	Toggling	Toggling	A87
A87 TP103	RAS2\	A87 Internal	Toggling	Toggling	A87
A87 TP104	MUX\	A87 Internal	Toggling	Toggling	A87
A87 TP105	CASU\	A87 Internal	Toggling	Toggling	A87
A87 TP106	CASL\	A87 Internal	Toggling	Toggling	A87
A87 TP107	REFIN\	A87 Internal	Toggling	Toggling	A87
A87 TP108	REFOUT\	A87 Internal	Toggling	Toggling	A87
A87 TP109	ROMSEL\	A87 Internal	High	Toggling	A87
A87 TP110	MEM_DTACK\	A87 Out	Toggling	Toggling	A87
A87 TP111	RW	A81 Out	Toggling	Toggling	A81
A87 TP113	DS	A87 Internal	Toggling	Toggling	A87

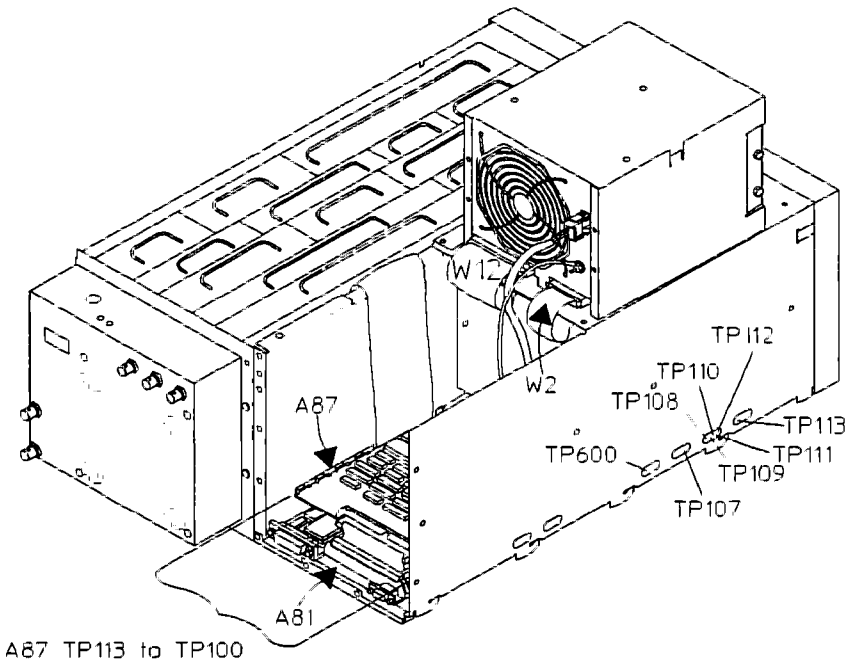

Figure 4-11. Control Lines Test Location

Troubleshooting Using the Self Tests

Test 9. Self Test thoroughly exercises the digital and analog circuits in the analyzer. However, some circuits are not tested, but they are used and can cause tests to fail. Other circuits are neither tested nor used. Table 4-11 lists these circuits. Keep this information in mind as you follow the self tests. If you suspect that one of these circuits is faulty, see table 4-11 and follow the recommended troubleshooting test.

Table 4-11. Circuits Not Tested by Test 9. Self Test

Used But Not Tested	Troubleshooting Test
Power Supply assembly	Test 1. Initial Verification
Ribbon cable	Test 3. CPU, Memory, and Buses
Control lines	Test 8. Control Lines
Not Used or Tested	
Disk Drive	Test 11. Disk Drive
HP-IB connector	Test 12. HP-IB/RS-232
Source BNC connector and last relay	Test 14. Source
Input protection circuits Input BNC and first relay	Test 18. Input Conversion
Rear panel oven output Rear panel reference output Rear panel reference input	Test 21. Reference
Memory battery Real-time clock	Test 32. Memory Battery
Rear panel fan	Test 33. Fan Power
Rear panel external trigger/gate Rear panel trigger/gate output	Test 34. Trigger/Gate
External Keyboard	Test 35. DIN Connector
HP 35689A/B Test Set	Test 36. Test Set Initial Verification

Test 9. Self Test

Use this test when one of the following occurs:

- Calibration fails
- Performance test fails
- Local oscillator unlocked
- Failure is intermittent
- HP-IB fails
- HP 35689A/B test set fails

1. Set the power switch to STANDBY (⏻) and disconnect all cables connected to the front panel. Remove the top cover (see figure 6-2 in chapter 6, "Replacing Assemblies").

2. Set the power switch to ON (I), then press the following keys:

   [**Special Fctn**]
   [F9]
   -99
   [F9]
   [SERVICE FUNCTIONS]
   [SELF TEST]
   [FUNCTIONL TESTS]
   [ALL]

3. When the tests have finished running, press the following keys:

   [**Special Fctn**]
   [SERVICE FUNCTIONS]
   [SELF TEST]
   [TEST LOG]

Note

To print the test log to a HP-IB printer, press the following keys:

[**Local/HP-IB**]
[SYSTEM CONTROLLR]
[**Special Fctn**]
[SERVICE FUNCTIONS]
[SELF TEST]
[TEST LOG]
[**Plot/Print**]
[PRINT ALL]

---

4. If the analyzer did not complete the tests (analyzer locks up), go to Test 10. ALL Locks Analyzer.
5. If the analyzer completes the tests, compare table 4-12 to the analyzer's test log. If the analyzer's test log matches more than one entry on the table, use the entry closest to the beginning of the table. The table lists the probable faulty assembly or assemblies and any recommended adjustment or troubleshooting procedure to do before replacing the assembly. If both an adjustment and a test are recommended, do the adjustment first.

Note

For the complete list of assemblies used in each self test, see table 10-3 on page 10-12. For additional information on the self tests, see "Self Test Descriptions" in chapter 10, "Internal Test Descriptions."

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6. If the analyzer failed a performance test and passed all self tests or all but the Quick confidence self test, see table 4-29 in "Troubleshooting Failing Performance Tests."
7. If the problem is intermittent and the analyzer passed all self tests, go to Test 22. Intermittent Failures.
8. If the analyzer passed all self test, review the circuits that are not used or tested in table 4-11.

Table 4-12. Self-Test Troubleshooting Guide

Failing Self Test	Probable Faulty Assembly	Adjustment	Troubleshooting Test
Processor	A81 CPU		Test 3. CPU, Memory, and Buses
ROM	A87/A88 Memory		Test 3. CPU, Memory, and Buses
RAM	A87/A88 Memory		Test 3. CPU, Memory, and Buses
Interrupt	A81 CPU		Test 3. CPU, Memory, and Buses
Mult fctn peripheral	A81 CPU		
Display digital	A81 CPU		
DMA	A81 CPU		
Math coprocssor	A81 CPU		
HP-IB	A81 CPU A87/A88 Memory		Test 33. Memory Battery
Disk controller	A81 CPU		
IIC bus	see test log		Test 6. IIC Bus
Fast bus	A81 CPU A62 ADC/Digital Filter		Test 7. Fast Bus
Front panel	Front Panel		
Digital filter gate array	A62 ADC/Digital Filter A32 300 MHz A33 Trigger		Test 13. Digital Filter
Detector gate array	A62 ADC/Digital Filter A33 Trigger		Test 13. Digital Filter
Source 187.5 kHz [187.5 kHz REFERENCE]	A42 Source Conversion A33 Trigger		Test 14. Source
Source gilbert cell [GILBERT CELL]	A42 Source Conversion		Test 14. Source
Mult loop tuning range	A51 Interpolation VCO A52 Fractional-N A33 Trigger	4. Interpolation VCO	Test 16. Interpolation Loop
Single loop tuning range	A21 Sum VCO A51 Interpolation VCO A52 Fractional-N A23 Step Phase Detector	5. Single Loop Control Voltage Clamps	Test 17. Single Loop
"Local Oscillator Unlocked" message displayed	A51 Interpolation VCO A52 Fractional-N A21 Sum VCO A22 Sum Phase Detector A23 Step Phase Detector A24 Step VCO		Test 15. Local Oscillator

Table 4-12. Self-Test Troubleshooting Guide (continued)

Failing Self Test	Probable Faulty Assembly	Adjustment	Troubleshooting Test
Source output level [OUTPUT CKTS]	A41 Source Amplifier A42 Source Conversion A21 Sum VCO A22 Sum Phase Detector A23 Step Phase Detector A24 Step VCO A31 Reference/Calibrator A32 300 MHz	10. Pretune Offset and Slope 13. Source Bandpass Filter	Test 14. Source
Receiver 2nd If [2ND IF LEVEL]	A61 IF A11 Input A12 First Conversion A13 Second Conversion A21 Sum VCO A32 300 MHz A41 Source Amplifier	14. First IF Bandpass Filter	Test 18. Input Conversion
Receiver ADC [ADC]	A62 ADC/Digital Filter A24 Step VCO A31 Reference/Calibrator A51 Interpolation VCO A61 IF	3. 300 MHz Reference VCO 12. Second IF Bandpass Filter 11. ADC Gain, Offset, and Reference	Test 18. Input Conversion
Post divider	A51 Interpolation VCO A21 Sum VCO	12. Second IF Bandpass Filter	Test 19. Sum Loop
Receiver autorange [AUTO RNG TRIP PTS]	A11 Input A41 Source Conversion	15. Autorange Threshold and 1 Meg Ohm Flatness 17. Calibrator Flatness and Level	Test 18. Input Conversion
Receiver 10 MHz [10 MHz LOCAL OSC]	A31 Reference/Calibrator A32 300 MHz A33 Trigger A21 Sum VCO A22 Sum Phase Detector A23 Step Phase Detector A24 Step VCO A51 Interpolation VCO A52 Fractional-N	3. 300 MHz Reference VCO 14. First IF Bandpass Filter 12. Second IF Bandpass Filter	Test 21. Reference
Source flatness [FLATNESS]	A41 Source Amplifier A42 Source Conversion		Test 14. Source
Quick confidence		3. 300 MHz Reference VCO 5. Single Loop Control Voltage Clamps 10. Pretune Offset and Slope 13. Source Bandpass Filter 14. First IF Bandpass Filter 12. Second IF Bandpass Filter 11. ADC Gain, Offset, and Reference	See "Troubleshooting Failing Performance Tests"

Test 10. ALL Locks Analyzer

Use this test to continue troubleshooting if the analyzer locked up while running the functional test ALL.

1. Set the power switch to ON (I) and as soon as the graticule appears, disable the calibration routine by pressing the following keys:

   [F9]
   [F9]
   [Special Fctn]
   [AUTO CAL ON **OFF**]

2. Press the following keys (allow enough time for each test to complete before pressing the next key) until a test fails or the analyzer locks up:

Note

A failure may cause the self tests to run very slow. Wait one minute before assuming the analyzer is locked up.

[F9]
– 99
[F9]
[SERVICE FUNCTIONS]
[SELF TEST]
[TEST LOG]
[CANCEL/RETURN]
[FUNCTIONL TESTS]
[CPU]
[PROCESSOR]
[ROM]
[RAM]
[INTERRUPT]
[MULT FCTN PERIPHERL]
[DISPLAY DGTL HW]
[SERVICE FUNCTIONS]
[SELF TEST]
[TEST LOG]
[CANCEL/RETURN]
[FUNCTIONL TESTS]
[DMA]
[MATH COPROCSSR]
[I/O]
[HP-IB]
[HP-IB FUNC TEST]
[ABORT/RETURN]
[INTERNAL DISK]

[DISK CONTROLLR]
[ABORT/RETURN]
[IIC BUS]
[FAST BUS]
[FRONT PANEL]
[ABORT/RETURN]
[RECEIVER]
[DIGITAL FILTER]
[DETECTOR]
[ABORT/RETURN]
[SOURCE]
[187.5 kHz REFERENCE]
[GILBERT CELL]
[ABORT/RETURN]
[LOCAL OSC]
[MULT-LOOP TUN RANGE]
[SNGL LOOP TUN RANGE]
[ABORT/RETURN]
[SOURCE]
[OUTPUT CKTS]
[ABORT/RETURN]
[RECEIVER]
[2ND IF LEVEL]
[ADC]
[ABORT/RETURN]
[LOCAL OSC]
[POST DIVIDER]
[ABORT/RETURN]
[RECEIVER]
[AUTO RNG TRIP PTS]
[10 MHz LOCAL OSC]
[ABORT/RETURN]
[SOURCE]
[FLATNESS]
[ABORT/RETURN]
[ABORT/RETURN]
[QUICK CONF TEST]

3. Locate the test that failed or locked up the analyzer in table 4-12. The table lists the probable faulty assembly and any recommended adjustment or troubleshooting procedure to do before replacing the assembly.

Test 11. Disk Drive

Use this test to isolate disk drive failures to the CPU assembly, the Disk Drive assembly, or the flexible disk.

Note

The assembly uses Logical Interchange Format (LIF), option 0-4. This is the same format used by the Series 200/300 BASIC system. To format a disk, press the following keys:

[**Disk Util**]
[DEFAULT DISK]
[INTERNAL DISK]
[CANCEL/RETURN]
[FORMAT DISK]
[PERFORM FORMAT]
[ENTER]

It takes about 1.5 minutes to format a disk.

---

1. Set the power switch to ON (I). Insert a formatted disk into the Disk Drive assembly and press the following keys:

[**Special Fctn**]
[F9]
– 99
[F9]
[SERVICE FUNCTIONS]
[SELF TEST]
[TEST LOG]
[CANCEL/RETURN]
[FUNCTIONL TESTS]
[I/O]
[INTERNAL DISK]
[ALL]

Note

This test takes about 20 minutes to complete if there are no failures.

---

2. If the Motor and Restore self tests pass and the Random Seek and Read self tests fail, the flexible disk is probably unformatted or faulty. If this occurs, use a different formatted disk and repeat step 1 to see if the error clears. Following is the typical error message when the disk is unformatted or faulty:

   Seek to n went to n
   read data verify error, sector n

   Where n is a sector number from 1 to 2464.

3. If the Disk Controller self test fails, the Disk Drive assembly or the CPU's disk drive controller is probably faulty. Before replacing the Disk Drive assembly, do the following to verify that the CPU's disk drive controller is operating correctly:

   a. Disconnect the power cord from the rear panel and place the Power Supply assembly in its test position. Remove the Memory assembly. See the disassembly/assembly illustrations in chapter 6, "Replacing Assemblies."

   b. With the Memory assembly upside-down and outside the chassis, connect the memory cable. Be careful not to short the pins on back of the assembly.

   c. Disconnect the disk drive cable (W4).

   d. Connect the power cord and set the power switch to ON (I). Press the following keys:
      [Special Fctn]
      [F9]
      – 99
      [F9]
      [SERVICE FUNCTIONS]
      [SELF TEST]
      [TEST LOG]
      [CANCEL/RETURN]
      [LOOP MODE **ON** OFF]
      [FUNCTIONL TESTS]
      [I/O]
      [INTERNAL DISK]
      [ALL]

e. Using a logic probe, check that the TTL signals in table 4-13 are toggling (see figure 4-12 for test locations).

Table 4-13. Disk Drive Control Signals

Test Location	Signal Name	In/Out
A81 U500(19)	8 MHz	A81 Internal
A81 U500(21)	1 MHz	A81 Internal
A81 U500(28)	DS0	A81 Internal
A81 U500(29)	DS1	A81 Internal
A81 U500(22)	DW	A81 Internal
A81 U501(12)	WRITE_DATA\	A81 Out

f. After checking the signals, press the following keys:

[ABORT/RETURN]
[ABORT/RETURN]
[ABORT/RETURN]
[LOOP MODE ON **OFF**]

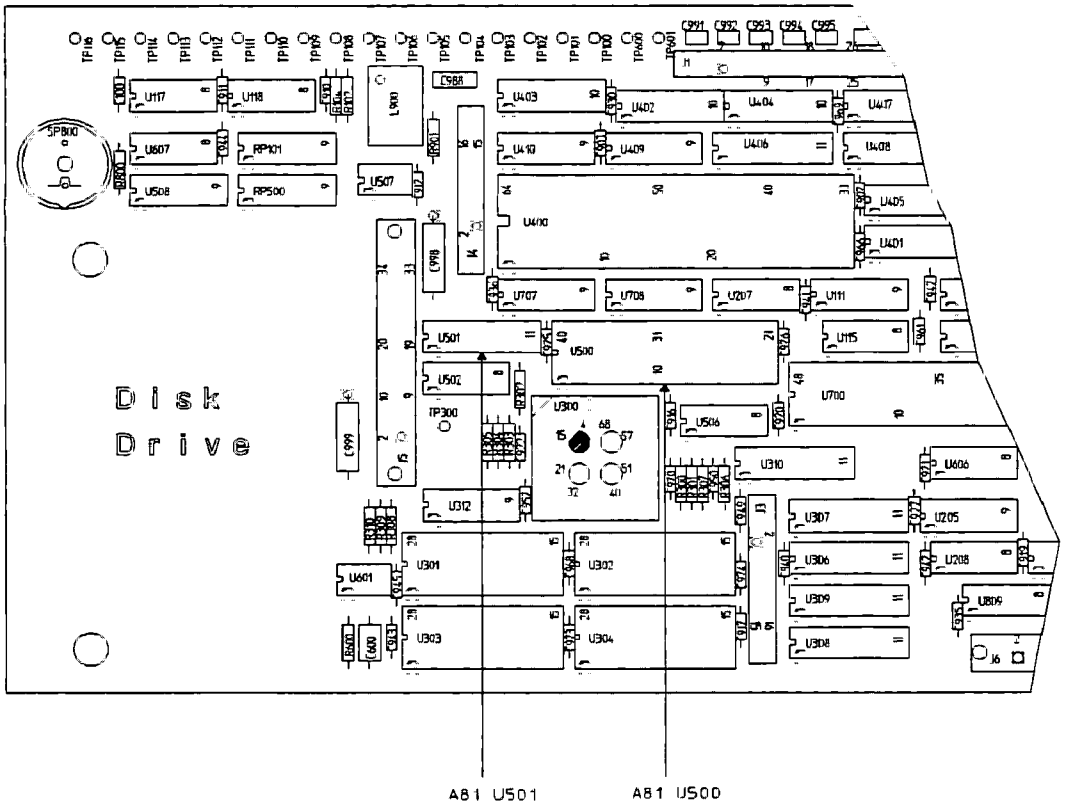


Figure 4-12. Disk Drive Controller Test Locations

Test 12. HP-IB/RS-232

Use this test to separate HP-IB sub-block failures from HP-IB connector failures.

Note The HP 3589A Spectrum/Network Analyzer's RS-232 connector is only used to control the HP 35689A/B S-Parameter Test Set.

---

1. Set the power switch to STANDBY (⏻) and remove the top cover (see the disassembly/assembly illustrations in chapter 6, "Replacing Assemblies").
2. Set the power switch to ON (|), then press the following keys:

   [Special Fctn]
   [F9]
   – 99
   [F9]
   [SERVICE FUNCTIONS]
   [SELF TEST]
   [FUNCTIONL TESTS]
   [I/O]
   [HP-IB]
   [HP-IB FUNC TEST]
3. If the HP-IB self test fails, the HP-IB sub-block on the CPU assembly is probably faulty.
4. Press the [HP-IB CONNECTOR] softkey.
5. Using a small jumper, short each HP-IB connector pin to the HP-IB connector ground while watching the display. When a pin is grounded, the corresponding pin in the display should have a dot in it. If this test fails, the HP-IB connector is probably faulty.

Note When pin 11 is grounded, the display should have a dot in ATN and may also have a dot in NDAC. The ground pins (pin 12, shield, and pins 18 through 24) will not have a dot when grounded with the jumper.

Test 13. Digital Filter

Use this test if the receiver is suspected of failing and all self tests listed before the Digital filter gate array in table 4-12 passed.

1. Using a spectrum analyzer (with frequency span set to ≤ 1 MHz) or an oscilloscope, check the signals in table 4-14 in the order listed. At the first incorrect signal, go to step 6 to check the probable faulty assembly's voltages at the connector.

Table 4-14. ADC/Digital Filter Frequency Reference

Test Location	Frequency	Amplitude	Output Impedance	Probable Faulty Assembly
A31 J8	80 MHz	– 5 dBm (ECL)	50 Ω	A31 Reference/Calibrator
A32 J2	60 MHz	– 2 5 dBm (ECL)	50 Ω	A32 300 MHz
A33 J3	250 kHz	3.3 Vp-p (TTL)	1 MΩ	A33 Trigger

2. Set the power switch to STANDBY (⏻), and reconnect all cables.

3. Set the power switch to ON (I), and check that A62 DS804 (LSWP – yellow LED) is on and briefly blinking off.

4. If the LED is not blinking and the message dma ok using internal test mode was included in the self-test message, the A33 Trigger assembly is probably faulty. If the message was not included, the A62 Digital/Filter assembly is probably faulty. Before replacing an assembly, go to step 6 to check the voltages at the connector.

5. If the LED is blinking, the A62 ADC/Digital Filter assembly is probably faulty. Do the next step before replacing the assembly.

6. Before replacing the probable faulty assembly, do the following to check that the voltages from the power supply assembly are present at the assembly's motherboard connector:

   a. Set the power switch to STANDBY (⏻). Remove the suspected assembly and place an extender board in the card nest.

   b. Set the power switch to ON (I), then check the pins of the extender board for correct voltages (see table 9-12 on page 9-24).

Test 14. Source

Use this test when the source is suspected of failing and all self tests listed before Source 187.5 kHz in table 4-12 passed.

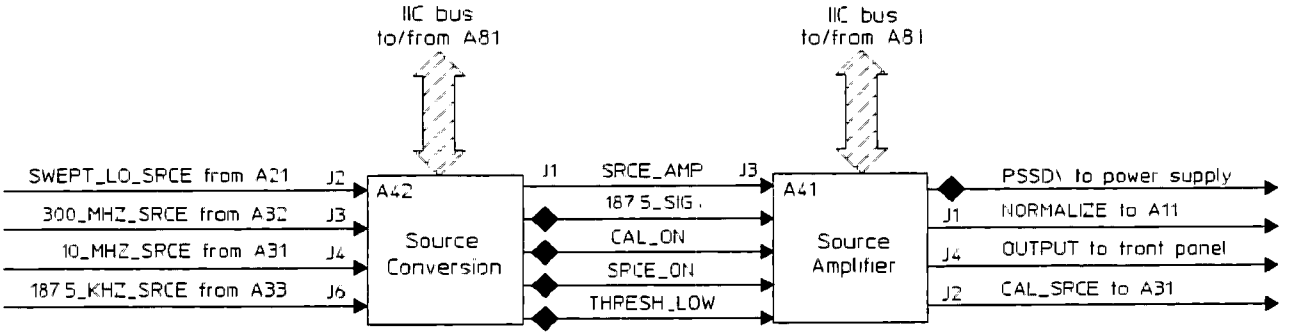


Figure 4-13. Source Block Diagram

Note

If a particular amplitude or frequency is failing, set the HP 3589A Spectrum/Network Analyzer to the failing amplitude or frequency.

---

1. Press the following keys:

   [**Preset**]
   [**Sweep**]
   [SWEEP AUTO **MAN**]
   [MANUAL FREQ]
   10 (or to the failing frequency)
   [MHz]
   [**Source**]
   [SOURCE **ON** OFF]
   [SOURCE AMPLITUDE]
   10 (or to the failing amplitude)
   [dBm]

2. Set the spectrum analyzer as follows:

Center Frequency	10 MHz (or to the failing frequency)
Frequency Span	1 MHz
Input Impedance	50 Ω

3. Connect the spectrum analyzer to A42 J1 using a BNC-to-SMB cable and compare the amplitude to table 4-15.

Table 4-15. Amplitude Setting and A42 J1 Amplitudes

Amplitude Setting (dBm)	A42 J1 Amplitude (dBm ± 3 dB)
15, 5, −5, −15, −25, −35	−42
14, 4, −6, −16, −26, −36	−43
13, 3, −7, −17, −27, −37	−44
12, 2, −8, −18, −28, −38	−45
11, 1, −9, −19, −29, −39	−46
10, 0, −10, −20, −30, −40	−47
9, −1, −11, −21, −31, −41	−48
8, −2, −12, −22, −32, −42	−49
7, −3, −13, −23, −33, −43	−50
6, −4, −14, −24, −34, −44	−51
−45	−52
−46	−53
−47	−54
−48	−55
−49	−56
−50	−57
−51	−58
−52	−59
−53	−60
−54	−61
−54.9	−62

4. If the amplitude at A42 J1 is correct, do the following:

   a. Set the power switch to STANDBY (⏻). Remove the screw at each end of the A41 Source Amplifier assembly, and place an extender board in the card nest.

   b. Set the power switch to ON (I), and press the following keys:
   [Source]
   [SOURCE **ON** OFF]

   c. Check that pin 16B (SRCE_ON) on the extender board is a TTL level high. If pin 16B is a TTL high, the A41 Source Amplifier assembly is probably faulty. If pin 16B is not a TTL high, the A42 Source Conversion assembly is probably faulty. Before replacing the assembly, go to step 6 to check the voltages at the connector.

5. If the amplitude at A42 J1 is incorrect, do the following:

   a. Press the [**Preset**] hardkey.

   b. Using a spectrum analyzer (with frequency span set to ≤ 1 MHz) or an oscilloscope, check the signals in table 4-16 in the order listed. At the first incorrect signal, go to step 6 if a probable faulty assembly is listed or to the recommended troubleshooting test.

Table 4-16. Source Reference Frequencies

Test Location	Frequency	Amplitude	Output Impedance	Probable Faulty Assembly or Troubleshooting Test
A31 J4	10 MHz	– 3 dBm (ECL)	50 Ω	A31 Reference/Calibrator
A31 J5	10 MHz	– 3 dBm (ECL)	50 Ω	A31 Reference/Calibrator
A31 J9	20 MHz	– 3 dBm (ECL)	50 Ω	A31 Reference/Calibrator
A32 J3	300 MHz	– 10 dBm ± 2 dB	50 Ω	A32 300 MHz
A32 J4	300 MHz	– 2 dBm ± 2 dB	50 Ω	A32 300 MHz
A33 J2	187.5 kHz	600 mVp-p square wave	50 Ω	A33 Trigger
A21 J2 †	310.1875 to 460.1875 MHz	– 10 dBm	50 Ω	Test 17. Single Loop

† Set spectrum analyzer's center frequency to 400 MHz and span to 200 MHz

   c. If all the signals are correct, the A42 Source Conversion assembly is probably faulty. Before replacing the assembly, do the next step.

6. Before replacing the probable faulty assembly, do the following to check that the voltages from the power supply assembly are present at the assembly's motherboard connector:

   a. Set the power switch to STANDBY (⏻). Remove the screw at each end of the suspected assembly. Remove the assembly and place an extender board in the card nest.

   b. Set the power switch to ON (I), then measure the pins of the extender board for correct voltages (see table 9-12 on page 9-24).

Test 15. Local Oscillator

Use this test when the "Local Oscillator Unlock" message appears on the screen and the following self tests passed:

- Digital filter gate array
- Detector gate array
- Mult loop tuning range
- Single loop tuning range

Note

The following procedure checks frequencies with a spectrum analyzer. However, if the failure mode requires more exact frequency measurements, use a frequency counter with $\pm 25 \times 10^{-3}$ Hz frequency accuracy.

---

1. Press the following keys:

   [**Preset**]
   [**Freq**]
   [FULL SPAN]
   [**Special Fctn**]
   [SERVICE FUNCTIONS]
   [SPCL TEST MODES]
   [LOCAL OSC CONFIG]
   [LOCAL OSC MULT]
   [**Sweep**]
   [SWEEP AUTO **MAN**]
   30.8125
   [MHz]

2. Set the spectrum analyzer as follows:

Start Frequency	20 MHz
Stop Frequency	60 MHz
Input Impedance	50 Ω

3. Connect the spectrum analyzer to A51 J4. The signal at A51 J4 should be 30.0 MHz, – 24 dBm ± 3 dB. If the signal is incorrect, go to Test 16. Interpolation Loop.

4. Using the HP 3589A's RPG, increase the manual frequency to 35.8 MHz. The signal at A51 J4 should slowly sweep from 30 MHz to 54.9 MHz, maintaining a – 24 dBm ± 3 dB amplitude. If the signal is incorrect, go to Test 16. Interpolation Loop.

5. Press the following keys:

   [**Sweep**]
   [MANUAL FREQ]
   50
   [MHz]

6. Connect the spectrum analyzer to A24 J2. The signal at A24 J2 should be 350 MHz, – 24 dBm ± 5 dB. If the signal at A24 J2 is incorrect, go to Test 20. Step Loop.

7. Connect the spectrum analyzer to A21 J3. The signal at A21 J3 should be 360.1875 MHz, 4 dBm ± 3 dB. If the signal at A21 J3 is incorrect, go to Test 19. Sum Loop.

Test 16. Interpolation Loop

Use this test when the local oscillator's interpolation loop is suspected of failing and the following self tests passed:

- Digital filter gate array
- Detector gate array

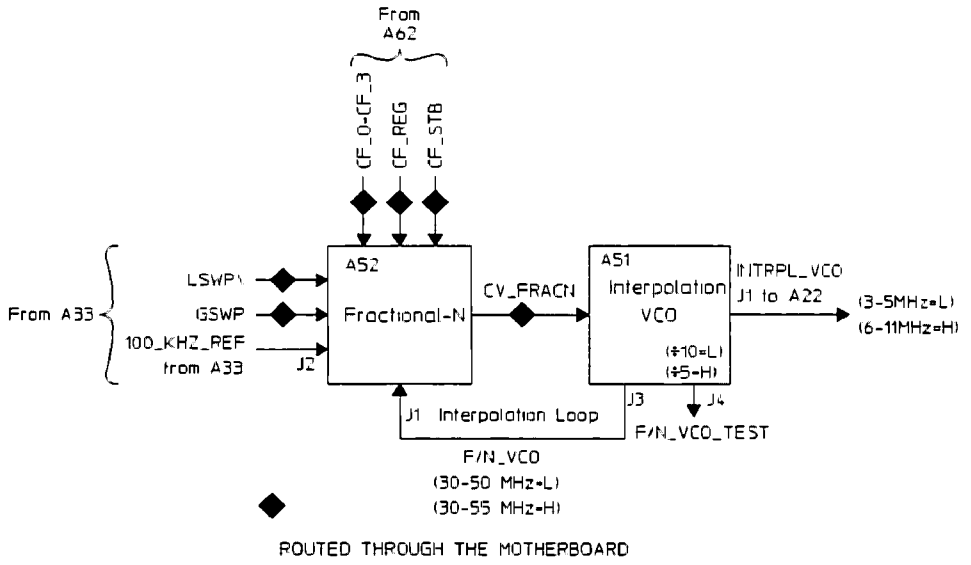


Figure 4-14. Local Oscillator Interpolation Loop

1. Using an oscilloscope with a 50 Ω input impedance, check that A33 J4 is a 100 kHz, TTL pulse.

2. If the signal at A33 J4 is incorrect, the A33 Trigger assembly is probably faulty. Before replacing the assembly, go to step 16 to check the voltages at the connector.

3. Set the power switch to STANDBY (⏻). Remove the screw at each end of the A51 Interpolation VCO assembly, and remove the assembly. Move A51 J101 to its test position, and place the assembly on an extender board.

4. Set the power switch to ON (I), then press the following keys:

   [**Freq**]
   [FULL SPAN]
   [**Sweep**]
   [SWEEP AUTO **MAN**]
   [MANUAL FREQ]
   0
   [Hz]

5. Using a spectrum analyzer with 50 Ω input impedance and the frequency span set to 50 MHz, check that A51 J4 is 55 MHz ± 0.5 MHz with an output level of – 24 dBm ± 3 dB.

6. If the signal at A51 J4 is incorrect, the A51 Interpolation VCO assembly is probably faulty. Before replacing the assembly, go to step 16 to check the voltages at the connector.

7. Set the power switch to STANDBY (⏻). Remove the test jumper and connect a ± 10 Vdc supply to the center pin of A51 J101.

8. Connect a spectrum analyzer to A51 J4 and set its frequency span to 30 MHz to 55 MHz.

9. Set the power switch to ON (I), then press the following keys:

   [**Freq**]
   [FULL SPAN]
   [**Sweep**]
   [SWEEP AUTO **MAN**]
   [MANUAL FREQ]
   0
   [Hz]

10. Vary the dc voltage from +10V to 0V while monitoring A51 J4. The frequency should vary between 30 MHz and 55 MHz as the dc voltage is varied. The output level should be – 24 dBm ± 3 dB.

11. If the signal at A51 J4 is incorrect, the A51 Interpolation VCO assembly is probably faulty. Before replacing the assembly, go to step 16 to check the voltages at the connector.

12. Set the power switch to STANDBY (⏻). Remove the A52 Fractional-N assembly and place an extender board in the card nest.

13. Set the power switch to ON (I), then press the following keys:

   [**Preset**]
   [**Special Fctn**]
   [F9]
   – 99
   [F9]
   [SERVICE FUNCTIONS]
   [SPCL TEST MODES]
   [LOCAL OSC CONFIG]
   [LOCAL OSC MULT]
   [**Sweep**]
   [SWEEP AUTO **MAN**]

14. While monitoring the signals in table 4-17 with a logic probe, change the HP 3589A's manual frequency using the RPG. Each line should toggle as the frequency changes.

Table 4-17. Control Frequency Signals

Extender Board Pin	Signal Name
4A	CF_REG
4B	CF0
4C	CF1
5A	CF_STB
5B	CF2
5C	CF3

15. If the signals in table 4-17 are correct, the A52 Fractional-N assembly is probably faulty. If the signals are not correct, the A62 ADC/Digital Filter assembly is probably faulty. Before replacing the assembly, do the next step.

16. Before replacing the probable faulty assembly, do the following to check that the voltages from the power supply assembly are present at the assembly's motherboard connector:

    a. Set the power switch to STANDBY (⏻). Remove the suspected assembly and place an extender board in the card nest.

    b. Set the power switch to ON (I), then check the pins of the extender board for correct voltages (see table 9-12 on page 9-24).

Test 17. Single Loop

Use this test when the local oscillator is suspected of failing in single loop mode and the following self tests passed:

- Digital filter gate array
- Detector gate array
- Mult loop tuning range

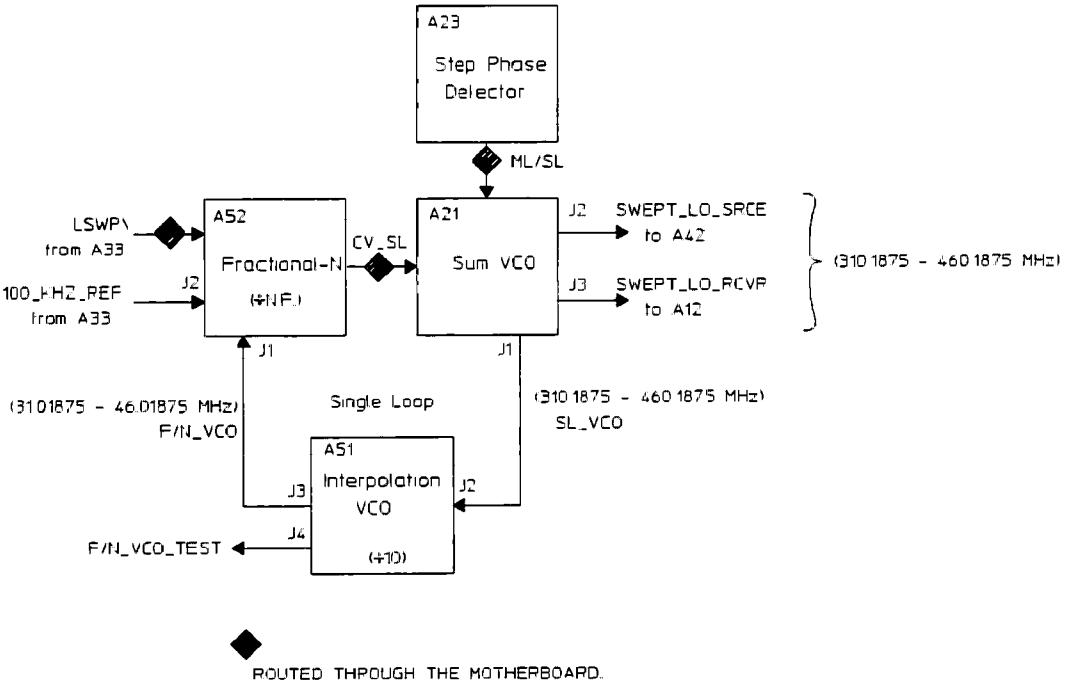


Figure 4-15. Local Oscillator in Single Loop Mode

1. Press the [**Preset**] key, then check the signals in table 4-18 using a spectrum analyzer.

Table 4-18. Single Loop Output Frequencies

Test Location	Frequency	Amplitude (± 3 dBm)	Output Impedance
A21 J2	310 to 460 MHz	– 10 dBm	50 Ω
A21 J3	310 to 460 MHz	+4 dBm	50 Ω
A51 J4	31 to 46 MHz	– 24 dBm	50 Ω

2. If all the signals are correct, the local oscillator is operating correctly in single loop mode. Go to Test 19. Sum Loop.

3. If the signal at A51 J4 is 31 to 46 MHz, but the signal at A21 J2 or A21 J3 is incorrect, the A21 Sum VCO assembly is probably faulty. Before replacing the assembly, go to step 16 to check the loop mode control signal.

4. Set the power switch to STANDBY (⏻). Remove the screw at each end of the A21 Sum VCO assembly, and remove the assembly. Move A21 J201 to its test position, and place the assembly on an extender board.

5. Set the power switch to ON (I). Check the signals in table 4-19 using a spectrum analyzer with its frequency span set to 50 MHz.

Table 4-19. Single Loop Output Frequencies in Test Mode

Test Location	Frequency (± 10 MHz)	Amplitude (± 3 dBm)	Output Impedance	Probable Faulty Assembly
A21 J1	445 MHz	+3 dBm	50 Ω	A21 Sum VCO
A21 J2	445 MHz	– 10 dBm	50 Ω	A21 Sum VCO
A21 J3	445 MHz	+4 dBm	50 Ω	A21 Sum VCO

6. If a signal is incorrect, go to step 16 to check the loop mode control signal.

7. Set the power switch to STANDBY (⏻). Remove the jumper from A21 J201, and connect a ± 10 Vdc supply to the center pin of A21 J201.

8. Connect a spectrum analyzer to A21 J1 and set its frequency span for 300 to 470 MHz.

9. Set the power switch to ON (I). While monitoring A21 J1, vary the dc voltage from +7V to – 1V. The signal at A21 J1 should vary between 310 and 460 MHz as the dc voltage is varied.

10. If the signal is correct, check that A21 J2 and A21 J3 vary between 310 and 460 MHz as the dc voltage is varied. The amplitudes should be the same as listed in the previous table.

11. If the signal at A21 J1, J2, or J3 is incorrect, the A21 Sum VCO assembly is probably faulty. Before replacing the assembly, go to step 16 to check the loop mode control signal.

12. Using an extender cable, connect A21 J1 to A51 J2.

13. Connect the spectrum analyzer to A51 J4 and set its frequency span for 30 to 50 MHz.

14. Vary the dc voltage while monitoring A51 J4. The signal should vary between 31 and 46 MHz as the dc voltage is varied. The output level should be – 24 dBm ± 3 dB.

15. If the signal at A51 J4 is correct, the A52 Fractional-N assembly is probably faulty. If the signal is incorrect, the A51 Interpolation VCO assembly is probably faulty. Before replacing the assembly, go to step 17 to check the voltages at the connector.

16. Before replacing the A21 Sum VCO assembly, do the following to check the loop mode control signal:

    a. Set the power switch to STANDBY (⏻). Remove the screws at each end of the A21 Sum VCO assembly and remove the assembly. Place an extender board in the card nest.

    b. Set the power switch to ON (I), then check that A21 J100 pin 8 (ML/SL) is a TTL level high. If it is not, the A23 Step Phase Detector assembly is probably faulty. Before replacing either assembly, do the next step.

17. Before replacing the probable faulty assembly, do the following to check that the voltages from the power supply assembly are present at the assembly's motherboard connector:

    a. Set the power switch to STANDBY (⏻). Remove the suspected assembly and place an extender board in the card nest.

    b. Set the power switch to ON (I), then check the pins of the extender board for correct voltages (see table 9-12 on page 9-24).

Test 18. Input Conversion

Use this test when the receiver is suspected of failing and all self tests listed before the Receiver 2nd If in table 4-12 passed.

Note If the "Local Oscillator Unlocked" message is displayed, go to Test 15. Local Oscillator.

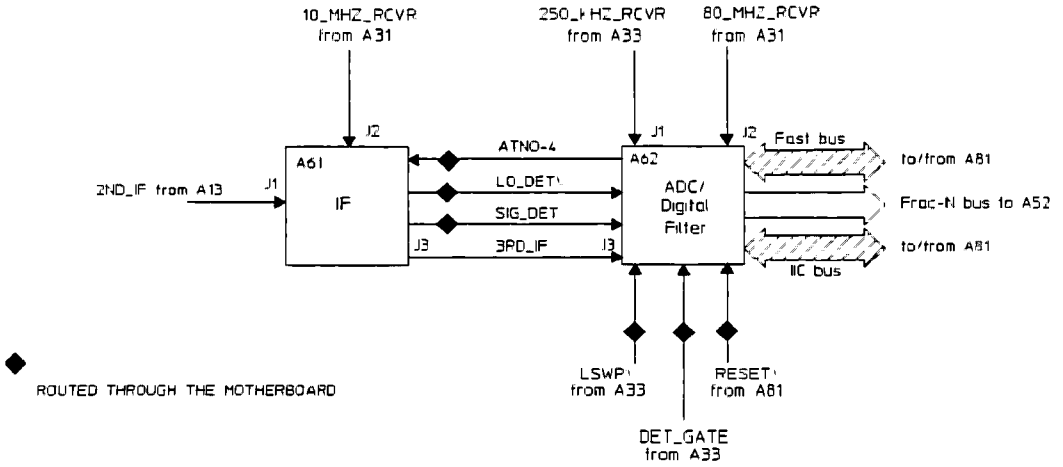


Figure 4-16. IF/ADC Block Diagram

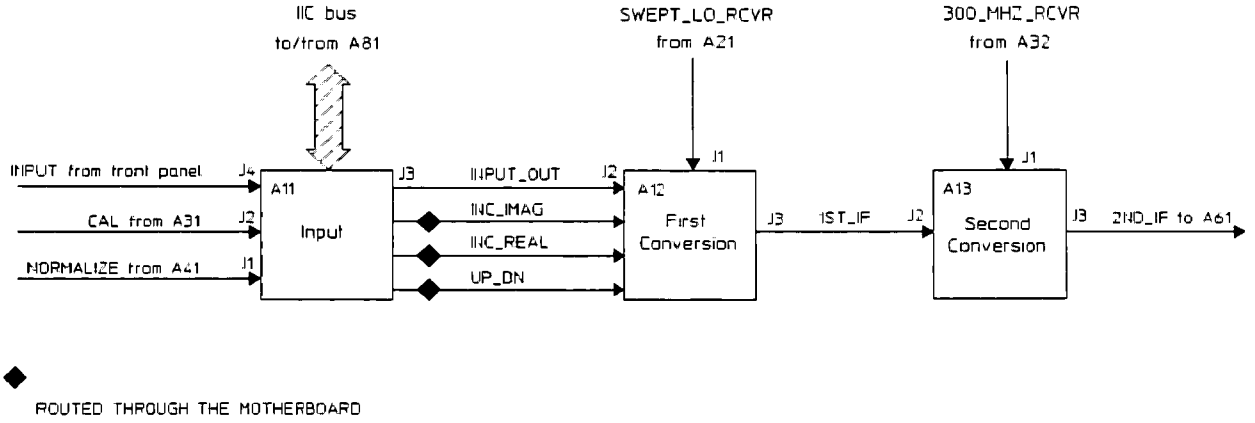


Figure 4-17. Input Conversion Block Diagram

1. Connect the signal generator to the front panel INPUT connector using a BNC cable.

2. Set the signal generator as follows:

Frequency	10 MHz
Amplitude	– 20 dBm

3. Press the following keys:

[Preset]
[Special Fctn]
[AUTO CAL ON **OFF**]
[Range/Input]
[RANGE]
– 20
[dBm]
[Sweep]
[SWEEP AUTO **MAN**]
10
[MHz]

4. Check the signals in table 4-20 using a spectrum analyzer with the frequency span set to ≤ 1 MHz. After checking a signal, reconnect the disconnected cable before checking the next signal. At the first incorrect signal, go to the recommended test or to step 24 if an assembly is listed as faulty.

Table 4-20. Input Conversion References and Signals

Test Location	Frequency	Amplitude (± 3 dB)	Output Impedance	Probable Faulty Assembly or Next Test
A11 J3	10 MHz	– 28 dBm	50 Ω	A11 Input
A21 J3	320.1875 MHz	4 dBm	50 Ω	Test 19. Sum Loop
A12 J3	310.1875 MHz	– 30 dBm	50 Ω	A12 First Conversion
A32 J5	300 MHz	0 dBm	50 Ω	A32 300 MHz
A13 J3	10.1875 MHz	– 37 dBm	50 Ω	A13 Second Conversion
A31 J3	10 MHz	– 3 dBm	50 Ω	A31 Reference/Calibrator
A61 J3	187.5 kHz	+7 dBm	50 Ω	Step 19
A51 J1	4.1875 MHz	– 5 dBm	50 Ω	A51 Interpolation VCO

5. If the signals in step 4 were correct and the Reciever 2nd IF self test passed, go to step 20.

6. Press the following keys:

   [**Special Fctn**]
   [SERVICE FUNCTIONS]
   [SPCL TEST MODES]
   [RECEIVER INPUT]
   [CONNCT TO SOURCE]

7. Connect the spectrum analyzer to A41 J1. The signal should be 10 MHz, – 10 dBm ± 3 dB. If the signal is incorrect, the A41 Source Amplifier assembly is probably faulty. Before replacing the assembly, go to step 24 to check the voltages at the connector.

8. Press the following keys:

   [CONNCT TO CALIBRATR]
   [**Marker**]
   [ZERO OFFSET]
   [**Special Fctn**]
   [SERVICE FUNCTIONS]
   [SPCL TEST MODES]
   [RECEIVER INPUT]

9. If the marker reading is not 0.00 ± 0.02 dB, go to step 19 to check the CAL signal.

10. Press the keys listed in table 4-21 and compare the marker readings to the table.

Table 4-21. Input Pads

Press key	Marker Reading
10 dB PAD IN	–10.00 ± 0.2 dB
10 dB PAD OUT	0.00 ± 0.2 dB
20 dB PAD A IN	–20.00 ± 0.2 dB
20 dB PAD A OUT	0.00 ± 0.2 dB
20 dB PAD B IN	–20.00 ± 0.2 dB
20 dB PAD B OUT	0.00 ± 0.2 dB

11. If a marker reading was incorrect, the A11 Input assembly is probably faulty. Before replacing the assembly, go to step 24 to check the voltages at the connector.

12. Press the following keys:

    [**Range/Input**]
        [1 MEGOHM]
    [**Special Fctn**]
        [SERVICE FUNCTIONS]
        [SPCL TEST MODES]
        [RECEIVER INPUT]
        [CONNCT TO SOURCE]
    [**Source**]
        –26
        [dBm]
    [**Marker**]
        [ZERO OFFSET]
    [**Special Fctn**]
        [SERVICE FUNCTIONS]
        [SPCL TEST MODES]
        [RECEIVER INPUT]

13. Press the keys listed in table 4-21 and compare the marker readings to the table. If a marker reading was incorrect, the A11 Input assembly is probably faulty. Before replacing the assembly, go to step 24 to check the voltages at the connector.

14. Change the signal generator's amplitude to 5 dBm.

15. Connect the spectrum analyzer to A61 J3.

16. Press the following keys:

    [**Preset**]
    [**Sweep**]
        [SWEEP AUTO **MAN**]
        10
        [MHz]
    [**Special Fctn**]
        [SERVICE FUNCTIONS]
        [SPCL TEST MODES]
        [IF ATTEN]
        16
        [dB]

17. Adjust the signal generator's amplitude for a spectrum analyzer readout of 6.00 dBm ± 0.05 dB at 187.5 kHz (spectrum analyzer's frequency span is 20 kHz).

18. Press the following keys:

        [IF ATTEN]
        15
        [dB]

19. The spectrum analyzer should now read 7.0 dBm ± 0.3 dB. If the signal at A61 J3 is incorrect do the following to check the CAL signal and attenuator control.

    a. Press the following keys:

    [**Preset**]
    [**Special Fctn**]
        [AUTO CAL ON **OFF**]
        [PRFM TESTS]
        [CALIBRATR TO INPUT]

    b. Connect the spectrum analyzer to A31 J1 and reconnect A61 J3 to A62 J3 using the original cable. The signal at A31 J1 should be 10 MHz, –20 dBm ± 3 dB. If the signal is incorrect, the A31 Reference/Calibrator assembly is probably faulty. Before replacing the assembly, go to step 24 to check the voltages at the connector.

    c. Set the power switch to STANDBY (⏻). Remove the screws at each end of the A61 IF assembly and remove the assembly. Place an extender board in the card nest.

    d. Set the power switch to ON (I), then press the following keys:

    [**Range/Input**]
        [AUTORANGE ON **OFF**]
    [**Special Fctn**]
        [F9]
        – 99
        [F9]
        [AUTO CAL ON **OFF**]
        [SERVICE FUNCTIONS]
        [SPCL TEST MODES]
        [IF ATTEN]
        0
        [dB]

    e. Check that pins 1A, 1B, 1C, 2A, and 2B on the extender board are a TTL level low. If they are incorrect, the A62 ADC/Digital Filter assembly is probably faulty. Before replacing the assembly, go to step 24 to check the voltages at the connector.

    f. Press the following keys:

        [IF ATTEN]
        31
        [dB]

    g. Check that pins 1A, 1B, 1C, 2A, and 2B on the extender board are a TTL level high. If they are incorrect, the A62 ADC/Digital Filter assembly is probably faulty. If they are correct, the A61 IF assembly is probably faulty. Before replacing the assembly, go to step 24 to check the voltages at the connector.

20. Press the following keys:

    [**Preset**]
    [**Special Fctn**]
        [AUTO CAL ON **OFF**]
        [SERVICE FUNCTIONS]
        [SPCL TEST MODES]
        [RECEIVER INPUT]
        [CONNCT TO CALIBRATR]
        [CANCEL/RETURN]
        [CALIBRATR **SWPT** TONE]

21. Connect the spectrum analyzer to A41 J2 and reconnect A61 J3 to A62 J3 using the original cable. The signal should be 200 kHz to 150 MHz, – 12 dBm. If the signal is incorrect, the A41 Source Amplifier assembly is probably faulty. Before replacing the assembly, go to step 24 to check the voltages at the connector.

22. Connect the spectrum analyzer to A31 J1 and reconnect A41 J2 to A31 J2 using the original cable. The signal should be 200 kHz to 150 MHz, – 20 dBm. If the signal is incorrect, the A31 Reference/Calibrator assembly is probably faulty. Before replacing the assembly, go to step 24 to check the voltages at the connector.

23. If all the signals in the previous steps are correct, the A62 ADC/Digital Filter assembly is probably faulty. Do the next step before replacing the assembly.

24. Before replacing the probable faulty assembly, do the following to check that the voltages from the power supply assembly are present at the assembly's motherboard connector:

    a. Set the power switch to STANDBY (⏻). Remove the screw at each end of the suspected assembly. Remove the assembly and place an extender board in the card nest.

    b. Set the power switch to ON (I), then measure the pins of the extender board for correct voltages (see table 9-12 on page 9-24).

Test 19. Sum Loop

Use this test when the local oscillator is suspected of failing in multiple loop mode and the following self tests passed.

- Digital filter gate array
- Detector gate array
- Mult loop tuning range

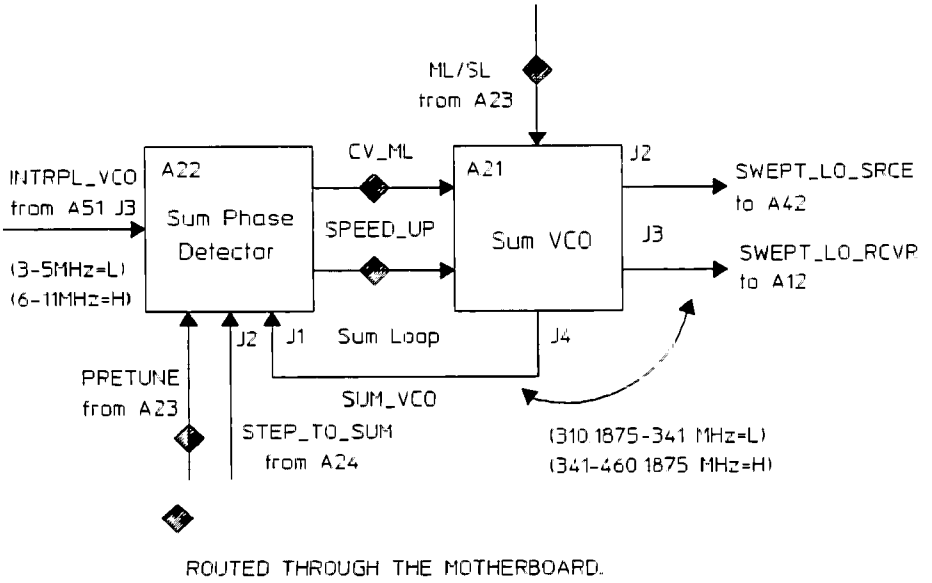


Figure 4-18. Local Oscillator Sum Loop

1. Set the power switch to ON (I), then press the following keys:

   [Special Fctn]
   [SINGLE CAL]
   [AUTO CAL ON **OFF**]
   [F9]
   – 99
   [F9]
   [SERVICE FUNCTIONS]
   [SPCL TEST MODES]
   [LOCAL OSC CONFIG]
   [LOCAL OSC SNGL **MULT**]

2. Using a spectrum analyzer, check the signals in table 4-22 in the order listed. At the first incorrect signal, go to the recommended test or to step 14 if an assembly is listed as faulty.

Table 4-22. Sum Loop Reference Frequencies

Test Location	Frequency	Amplitude (± 3 dB)	Output Impedance	Probable Faulty Assembly or Next Test
A24 J2	306 to 450 MHz	– 24 dBm	50 Ω	Test 20 Step Loop
A24 J1	306 to 450 MHz	– 8 dBm	50 Ω	A24 Step VCO
A51 J1	3 to 11 MHz†	– 3 dBm (ECL)	50 Ω	A51 Interpolation VCO

† There is a noticeable jump in the sweep between 5 and 6 MHz as the signal changes between 'L' and 'H' settings This occurs at an input frequency of approximately 30.8125 MHz.

3. Set the power switch to STANDBY (⏻). Remove the screw at each end of the A22 Sum Phase Detector assembly, and lift the assembly up about one inch.

4. Remove the screw at each end of the A21 Sum VCO, and place the assembly on an extender board.

5. Connect a ± 10V dc supply to A21 CVML (TP1, ground is at TP2).

6. Set the spectrum analyzer's frequency span to 300 MHz to 470 MHz and connect its 50 Ω input to A21 J4.

7. Set the power switch to ON (I), then press the following keys:

   [Special Fctn]
   [SINGLE CAL]
   [AUTO CAL ON **OFF**]
   [F9]
   – 99
   [F9]
   [SERVICE FUNCTIONS]
   [SPCL TEST MODES]
   [LOCAL OSC CONFIG]
   [LOCAL OSC SNGL **MULT**]

8. Vary the dc voltage from +7V to – 1V while monitoring A21 J4. The frequency should vary between 310 MHz to 460 MHz as the dc voltage is varied. The output level should be +8 dBm ± 3 dB.

9. If the signal at A21 J4 is correct, the A22 Sum Phase Detector assembly is probably faulty. Before replacing the assembly, go to step 14 to check the voltages at the connector. If the signal at A21 J4 is incorrect, the A21 Sum VCO assembly is probably faulty. Before replacing the assembly, go to step 13 to check control signals.

10. Remove the dc supply from A21 TP1.

11. Set the power switch to STANDBY (⏻), then push the A22 Sum Phase Detector assembly back into the card nest.

12. Set the power switch to ON (I), then press the following keys:

    [**Special Fctn**]
    [SINGLE CAL]
    [AUTO CAL ON **OFF**]
    [F9]
    – 99
    [F9]
    [SERVICE FUNCTIONS]
    [SPCL TEST MODES]
    [LOCAL OSC CONFIG]
    [LOCAL OSC SNGL **MULT**]

13. Before replacing the A21 Sum VCO assembly, check the signals in table 4-23.

Table 4-23. Sum Loop Control Signals

Signal Name	Test Location	Amplitude	Probable Faulty Assembly
ML/SL	A21 J100 pin 8	TTL Low	A23 Step Phase Detector
SPEED-UP	A21 J100 pin 7	TTL Low†	A22 Sum Phase Detector

† The signal occasionally pulses high. In manual sweep the signal is always low.

14. Before replacing the probable faulty assembly, do the following to check that the voltages from the power supply assembly are present at the assembly's motherboard connector:

    a. Set the power switch to STANDBY (⏻). Remove the suspected assembly and place an extender board in the card nest.

    b. Set the power switch to ON (I), then check the pins of the extender board for correct voltages (see table 9-12 on page 9-24).

Test 20. Step Loop

Use this test when the local oscillator is suspected of failing in multiple loop mode and the following self tests passed.

- Digital filter gate array
- Detector gate array
- Mult loop tuning range

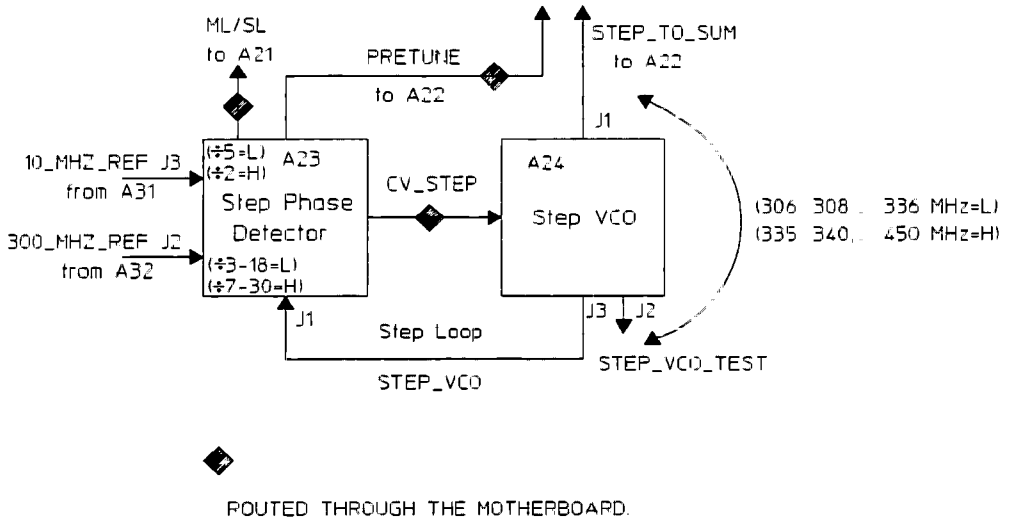


Figure 4-19. Local Oscillator Step Loop

1. Using a spectrum analyzer with its frequency span set to ≤ 1 MHz, check the signals in table 4-24 in the order listed. At the first incorrect signal, go to step 10.

Table 4-24. Step Loop Reference Frequencies

Test Location	Frequency	Amplitude (± 3 dB)	Output Impedance	Probable Faulty Assembly
A31 J9	20 MHz	– 3 dBm (ECL)	50 Ω	A31 Reference/Calibrator
A31 J4	10 MHz	– 3 dBm (ECL)	50 Ω	A31 Reference/Calibrator
A32 J4	300 MHz	– 2 dBm	50 Ω	A32 300 MHz

2. Set the power switch to STANDBY (⏻). Remove the screw at each end of the A24 Step VCO assembly, and remove the assembly. Move A24 J200 to its test position, and place the assembly on an extender board.

3. Set the power switch to ON (I), then press the following keys:
   [**Freq**]
   [FULL SPAN]
   [**Sweep**]
   [SWEEP AUTO **MAN**]
   [MANUAL FREQ]
   0
   [Hz]
4. Using a spectrum analyzer with 50 Ω input impedance and its frequency span set to 50 MHz, check that A24 J3 is 450 MHz ± 40 MHz, +10 dBm ± 5 dB.
5. If the signal at A24 J3 is incorrect, the A24 Step VCO assembly is probably faulty. Before replacing the assembly, go to step 10 to check the voltages at the connector.
6. Set the power switch to STANDBY (⏻). Remove the test jumper and connect a ± 10V dc supply to the center pin of A24 J200.
7. Set the spectrum analyzer's frequency span to 300 MHz to 470 MHz and connect its 50 Ω input to A24 J3.
8. Set the power switch to ON (I). Vary the dc voltage from +7V to – 1V while monitoring A24 J3. The frequency should vary between 306 MHz and 450 MHz as the dc voltage is varied. The output level should be +10 dBm ± 5 dB.
9. If the signal at A24 J3 is correct, the A23 Step Phase Detector assembly is probably faulty. If the signal at A24 J3 is incorrect, the A24 Step VCO assembly is probably faulty. Do the next step before replacing the assembly.
10. Before replacing the probable faulty assembly, do the following to check that the voltages from the power supply assembly are present at the assembly's motherboard connector.
    a. Set the power switch to STANDBY (⏻). Remove the suspected assembly and place an extender board in the card nest.
    b. Set the power switch to ON (I), then check the pins of the extender board for correct voltages (see table 9-12 on page 9-24).

Test 21. Reference

Use this test when reference signals are suspected of failing and the following self tests passed:

- Receiver 2nd If
- Receiver ADC
- Post divider
- Receiver autorange

Note

The following procedure checks frequencies with a spectrum analyzer. However, if the failure mode requires more exact frequency measurements, use a frequency counter with $\pm 25 \times 10^{-3}$Hz frequency accuracy.

---

1. If the analyzer has option 1D5 (High Stability Frequency Reference), do the following:

   a. Remove the rear panel jumper connecting OVEN REF OUT to EXT REF IN.

   b. Connect the spectrum analyzer's 50 Ω input to OVEN REF OUT and check that it is 10 MHz, +3 dBm ± 3 dB. If the signal is incorrect, do the following:

      i. Set the power switch to STANDBY (⏻), and disconnect the power cord from the rear panel. Remove the rear panel and fan/oven housing (see the assembly/disassembly illustrations in chapter 6, "Replacing Assemblies").

      ii. Disconnect the connector with the yellow, red, and black wires from the A91 Fan Power/Oven assembly (see figure 6-11).

      iii. Set the power switch to ON (I). Check that the voltage at the yellow wire is − 18 ± 2V and the voltage at the red wire is +18 ± 2V. If either voltage is incorrect, the motherboard or the wire is probably faulty. If the voltages are correct, the A91 Fan Power/Oven assembly is probably faulty.

2. Set the synthesizer as follows:

Frequency	10 MHz
Amplitude	5 dBm

3. Connect the synthesizer to the rear panel EXT REF IN connector.

4. Using a spectrum analyzer with its frequency span set to ≤ 1 MHz, check the signals in table 4-25 in the order listed. At the first incorrect signal, go to step 15.

Table 4-25. Reference/Calibrator Signals

Test Location	Frequency	Amplitude (± 3 dB)	Output Impedance	Probable Faulty Assembly
A31 J8	80 MHz	– 5 dBm	50 Ω	A31 Reference/Calibrator †
A31 J6	10 MHz	+3 dBm	50 Ω	A31 Reference/Calibrator
A31 J9	20 MHz	– 3 dBm	50 Ω	A31 Reference/Calibrator

† Before replacing this assembly, check adjustment 2 (80 MHz Reference VCXO)

5. Repeatedly check the signals in table 4-25 but set the synthesizer's frequency to 1 MHz, then 2 MHz, and finally 5 MHz.

Note

The analyzer may not be able to lock to a low frequency signal connected to EXT REF IN.

---

6. Again check the signals in table 4-25 but set the synthesizer's amplitude to – 5 dBm, then to +10 dBm.
7. Disconnect the synthesizer from the EXT REF IN connector, and on analyzer's with option 1D5 reconnect the rear panel jumper (EXT REF IN to OVEN REF OUT).
8. Using a BNC cable, connect REF OUT to the spectrum analyzer's 10 MHz reference input.
9. Press the following keys:

   [**Special Fctn**]
   [PRFM TESTS]
   [CALIBRATR TO INPUT]

10. Using a spectrum analyzer with the frequency span set to ≤ 1 MHz, check the signals in table 4-26 in the order listed. At the first incorrect signal, go to step 15.

Table 4-26. 300 MHz, Calibrator and Trigger Signals

Test Location	Frequency	Amplitude (± 3 dB)	Output Impedance	Probable Faulty Assembly
A32 J4	300 MHz	– 1 dBm	50 Ω	A32 300 MHz
A32 J5	300 MHz	1 dBm	50 Ω	A32 300 MHz
A31 J1	10 MHz	– 20 dBm	50 Ω	A31 Reference/Calibrator
A32 J2	60 MHz	– 2 dBm	50 Ω	A32 300 MHz
A33 J3	250 kHz	13 dBm	50 Ω	A33 Trigger

11. Press the following keys:

    [**Preset**]
    [**Freq**]
        [FULL SPAN]
    [**Sweep**]
        [SWEEP AUTO **MAN**]

12. For each of the following manual frequencies in table 4-27, set [MANUAL FREQ] to the frequency in the table and check the signal at A21 J3 using a spectrum analyzer.

Table 4-27. Sum VCO Frequencies

Manual Frequency	A21 J3 Frequency	A21 J3 Amplitude
0 Hz	310.1875 MHz	+4 dBm ± 3 dB
30.8125 MHz	341.0 MHz	+4 dBm ± 3 dB
150 MHz	460.1875 MHz	+4 dBm ± 3 dB

13. If the frequency at A21 J3 was incorrect for all manual frequencies, go to Test 17. Single Loop.

14. If the frequency at A21 J3 was correct for some manual frequencies and incorrect for others, do the following:

    a. Set [MANUAL FREQ] to a frequency that produced an incorrect frequency at A21 J3.

    b. In table 8-1 on page 8-17, locate the manual frequency in the Measurement Freq column. (Table 8-1 lists the frequencies of the different loops for all measurement frequencies.)

    c. Check the frequency of A51 J1 and compare to the Intrpl VCO frequency in table 8-1.

    d. If the frequency at A51 J1 is incorrect, go to Test 16. Interpolation Loop.

    e. Check the frequency of A24 J2 and A24 J1, and compare to the Step VCO frequency in table 8-1.

    f. If the frequency at A24 J2 or A24 J1 is incorrect, go to Test 20. Step Loop.

15. Before replacing the probable faulty assembly, do the following to check that the voltages from the power supply assembly are present at the assembly's motherboard connector.

    a. Set the power switch to STANDBY (⏻). Remove the suspected assembly and place an extender board in the card nest.

    b. Set the power switch to ON (I), then check the pins of the extender board for correct voltages (see table 9-12 on page 9-24).

Test 22. Intermittent Failures

Use this test to isolate intermittent failures to the assembly.

1. Check the common reasons for intermittent failures in table 4-28. If it's possible that your intermittent failure is caused by one of the common reasons given in the table, then follow the recommended troubleshooting procedure.

Table 4-28. Common Reasons for Intermittent Failures

Common Reasons	Troubleshooting Procedure
Loose screws and cables	Check that the screws in the analyzer are tight and that the cables are firmly in their sockets This is especially important since grounding for the analyzer depends on the cables and screws.
Power supply voltages	Check for correct power-supply voltages See Test 1. Initial Verification
Out-of-adjustment	Do the adjustments for the analyzer in chapter 5.
Air flow restricted	The analyzer cools by drawing air from both side and blowing it out the back panel. Check that the air flow was not restricted in these areas when the failure occurred.
External voltage	Verify that the line voltage is within the electrical specification for the analyzer. See chapter 2.

Caution 

Do not install a disk in the Disk Drive assembly. Running the disk in loop mode will wear out the disk drive head.

2. Set the power switch to ON (I), then press the following keys:

   [**Special Fctn**]
   [F9]
   – 99
   [F9]
   [SERVICE FUNCTIONS]
   [SELF TEST]
   [LOOP MODE **ON** OFF]
   [FUNCTIONL TESTS]
   [ALL]

3. After this test detects a failure, press the following keys:

   [ABORT/RETURN]
   [LOOP MODE ON **OFF**]

4. Compare table 4-12 on page 4-29 to the test log. If the analyzer's test log matches more than one entry on the table, use the entry closest to the beginning of the table. The table lists the probable faulty assembly or assemblies and any recommended adjustment or troubleshooting procedure to do before replacing the assembly. If both an adjustment and a test are recommended, do the adjustment first.

Note

All pass, fail, and abort messages are displayed on the test log along with the number of times a test passes, fails, or aborts.

When loop mode is activated, the analyzer continually repeats a test until power is cycled or loop mode is aborted by pressing [ABORT/RETURN]. If the power is cycled, the information in the test log is lost.

During some tests the keyboard is not active and loop mode cannot be aborted. If this occurs, wait for the test to finish.

If you abort a self test before the self test is finished, the analyzer may fail its calibration routine. To prevent this from happening, press [**Preset**] or cycle power after you abort a self test.

To run a specific self test in loop mode, press the following keys and then select the self test:

[**Preset**]
[**Special Fctn**]
[SERVICE FUNCTIONS]
[SELF TEST]
[LOOP MODE **ON** OFF]
[FUNCTIONL TESTS]

Troubleshooting Failing Performance Tests

Note

With the exception of the Quick Confidence test, all functional self tests in Test 9. Self Test must pass before table 4-29 is valid.

Use table 4-29 to determine which assembly is causing a performance test to fail. The table lists the assembly or assemblies most likely to cause the failure. In some cases, the failure can be isolated to one assembly based on the exact failure. When the cause of the failure cannot be isolated to one assembly, an additional test is provided to help isolate the faulty assembly. Multiple probable faulty assemblies are listed in order of probability.

Table 4-29. Failing Performance Test Troubleshooting Guide

Failing Performance Test	Probable Faulty Assembly (in order of probability)	Troubleshooting Test
Local Oscillator Feedthrough	A12 First Conversion A11 Input	Test 23. Local Oscillator Feedthrough
Phase Noise	A51 Interpolation VCO A52 Fractional-N A21 Sum VCO A22 Sum Phase Detector A23 Step Phase Detector A24 Step VCO A31 Reference/Calibrator A32 300 MHz A33 Trigger A91 Fan Power/Oven	Test 24. Phase Noise
Residual Responses	A12 First Conversion A13 Second Conversion A11 Input A61 IF	Test 25. Residual Responses
Noise Level	A61 IF A62 ADC/Digital Filter A12 First Conversion A11 Input A13 Second Conversion	Test 26. Noise Level
Frequency Accuracy	A31 Reference Calibrator A91 Fan Power/Oven	Test 27. Frequency Accuracy
Spurious Responses	A52 Fractional-N A51 Interpolation VCO A22 Sum Phase Detector A21 Sum VCO A24 Step VCO A23 Step Phase Detector	Test 28. Spurious Responses

Table 4-29. Failing Performance Test Troubleshooting Guide (continued)

Failing Performance Test	Probable Faulty Assembly (in order of probability)	Troubleshooting Test
Image Responses 40 85956 MHz fails 60.85956 MHz fails 61 35956 MHz fails	 A12 First Conversion A61 IF A61 IF	
Input Harmonic Distortion	A11 Input A12 First Conversion	Test 29 Input Harmonic Distortion
Intermodulation Distortion	A61 IF A12 First Conversion A11 Input	Test 30 Intermodulation Distortion
Source Response	A42 Source Conversion A41 Source Amplifier	Test 31 Source Response
Amplitude Accuracy and Flatness	A31 Reference/Calibrator [1] A11 Input [2]	
Reference Level Accuracy	A11 Input [3]	
Dynamic Accuracy	A62 ADC/Digital Filter [4]	
Source Dynamic Accuracy DAC attenuation fails pad attenuation fails	 A42 Source Conversion A41 Source Amplifier	
Input Return Loss	A11 Input	
Source Return Loss	A41 Source Amplifier	
Source Harmonic Distortion	A41 Source Amplifier	
Source Spurious Responses	A42 Source Conversion [5]	
Source Noise	A41 Source Amplifier [5]	

1 Provided the Source Amplitude Accuracy and Frequency Response performance test passed.

2 Provided the Source Amplitude Accuracy and Frequency Response performance test passed and failures only occurred in the 1 MΩ input impedance path.

3 If all ranges failed, the following assemblies could cause the failure:
A12 First Conversion
A13 Second Conversion
A61 IF
A62 ADC/Digital Filter

4 Provided the receiver passed all performance tests. Before replacing the A62 ADC/Digital Filter assembly, check the ADC Gain, Offset, and Reference adjustment. If the performance test still fails after replacing the assembly, the probable faulty assembly is listed below in order of probability:
A61 IF
A13 Second Conversion
A12 First Conversion
A11 Input

5 Provided the receiver passed all performance tests.

Test 23. Local Oscillator Feedthrough

Use this test to determine if the A11 Input assembly or the A12 First Conversion assembly is causing the Local Oscillator Feedthrough performance test to fail.

Note If local oscillator feedthrough null passes the Quick Confidence test and fails the performance test, the A12 First Conversion assembly is probably faulty.

---

1. Set the power switch to STANDBY (⏻). Remove the screw at each end of the A11 Input assembly, and place the assembly on an extender board.
2. Reconnect the following using extender cables:
   A11 J1 to A41 J1
   A11 J2 to A31 J1
   A11 J3 to A12 J2
3. Set the power switch to ON (|). Using an oscilloscope, monitor J5 pin 1A (INC_IMAG), pin 3A (INC_REAL), and pin 2A (UP_DN). During the calibration routine, narrow pulses are on pins 1A and 3A, and the signal on pin 2A toggles between high and low TTL levels.

Note The calibration routine occurs during power up. To repeat the calibration routine, press the following keys:
[**Special Fctn**]
[SINGLE CAL]

---

4. If the signals are correct, the A12 First Conversion assembly if probably faulty. If the signals are incorrect, the A11 Input assembly is probably faulty.

Test 24. Phase Noise

Use this test to determine which of the following assemblies is causing the Phase Noise performance test to fail:

- A51 Interpolation VCO
- A52 Fractional-N
- A21 Sum VCO
- A22 Sum Phase Detector
- A23 Step Phase Detector
- A24 Step VCO
- A31 Reference/Calibrator
- A32 300 MHz
- A33 Trigger
- A91 Fan Power/Oven

Note

If you have the optional A91 Fan Power/Oven assembly, remove the rear panel jumper (OVEN REF OUT to EXT REF IN), and repeat the Phase Noise performance test. If the test now passes, the A91 Fan Power/Oven assembly is probably faulty.

---

1. Set the signal generator for a 10 MHz, – 20 dBm signal and connect to the front panel INPUT connector.
2. Press the following keys:

[**Preset**]
[**Special Fctn**]
[SINGLE CAL]
[AUTO CAL ON **OFF**]
[**Sweep**]
[OVERSWEEP ON **OFF**]
[**Freq**]
[CENTER]
10
[MHz]
[SPAN]
5
[kHz]
[**Marker**]
[MARKER X ENTRY]
10.001
[MHz]
[**Marker Fctn**]
[NOISE LEVEL **ON** OFF]

3. Record the **Mkr** readout (dBm/Hz).
4. Change the signal generator's frequency to 100 MHz.
5. Press the following keys:

   [NOISE LEVEL ON **OFF**]
   [**Freq**]
   [CENTER]
   100
   [MHz]
   [**Marker**]
   [MARKER X ENTRY]
   100.001
   [MHz]
   [**Marker Fctn**]
   [NOISE LEVEL **ON** OFF]

6. If the **Mkr** readout is more than approximately 10 dB above the level recorded in step 3, then the A31 Reference/Calibrator assembly is probably faulty.
7. Set a spectrum analyzer's center frequency to 300 MHz and connect to A32 J4. If the noise level is > -95 dBc/Hz for offsets > 1 kHz, the A32 300 MHz assembly is probably faulty.
8. Connect an oscilloscope to A33 J4. The signal should be a 100 kHz, 1 Vp-p, approximate 1% duty cycle pulse. If the signal is not correct, the A33 Trigger assembly is probably faulty.
9. Reconnect the following using original cables.

   A31 J4 to A23 J3
   A32 J4 to A23 J2
   A33 J4 to A52 J2

10. Press the following keys:

    [NOISE LEVEL ON **OFF**]
    [Special Fctn]
    [PRFM TESTS]
    [CALIBRATR TO INPUT]
    [Freq]
    [CENTER]
    10
    [MHz]
    [Special Fctn]
    [F9]
    – 99
    [F9]
    [SERVICE FUNCTIONS]
    [SPCL TEST MODES]
    [LOCAL OSC CONFIG]
    [LOCAL OSC **SNGL** MULT]
    [Marker]
    [MKR TO PEAK]
    [ZERO OFFSET]
    [MARKER X ENTRY]
    10.001
    [MHz]
    [Marker Fctn]
    [NOISE LEVEL **ON** OFF]

11. Phase noise fails in single loop mode if the Δ **Mkr** readout is > – 105 dB/Hz. If single loop phase noise is failing, the A21 Sum VCO assembly or the A52 Fractional-N assembly is probably faulty.

12. Press the following keys:

    [Preset]
    [Sweep]
    [SWEEP AUTO **MAN**]
    [MANUAL FREQ]
    10
    [MHz]

13. Set the spectrum analyzer's center frequency to 316 MHz and connect to A24 J2. Measure and record the noise level at offsets >1 kHz.

14. Press the following keys:

    [MANUAL FREQ]
    100
    [MHz]

15. Change the spectrum analyzer's center frequency to 400 MHz and measure the noise level for offsets >1 kHz. If the noise level changed when the frequency changed, the A23 Step Phase Detector assembly or the A24 Step VCO assembly is probably faulty.

16. Change the spectrum analyzer's center frequency to 10.1875 MHz and connect to A51 J1. If the noise level is > – 110 dBc/Hz for offset frequencies >100 Hz, the A51 Interpolation VCO assembly is probably faulty.

17. Reconnect A51 J1 to A22 J3.

18. Change the spectrum analyzer's center frequency to 410.1875 MHz and span to 5 kHz. Connect the spectrum analyzer to A21 J3. If the shape of the noise peaks excessively (>5 dB), the A22 Sum Phase Detector assembly is probably faulty.

Test 25. Residual Responses

Use this test to determine which of the following assemblies is causing the Residual Responses performance test to fail:

- A12 First Conversion
- A13 Second Conversion
- A11 Input
- A61 IF

1. Disconnect all cables connected to the front panel INPUT connector.

2. Press the following keys:

   [**Preset**]
   [**Special Fctn**]
   [SINGLE CAL]
   [AUTO CAL ON **OFF**]
   [**Range/Input**]
   [RANGE]
   –20
   [dBm]
   [**Meas Type**]
   [NARROW BAND ZOOM]
   [**Avg/Pk Hld**]
   [AVERAGE]
   [**Freq**]
   [SPAN]
   36.0625
   [Hz]
   [CENTER] (to failing frequency)

3. After ten averages, press the following keys:

   [**Marker**]
   [ZERO OFFSET]

4. Disconnect the cable connected to A11 J3, press [**Meas Restart**], and wait for ten averages. The Δ **Mkr** readout should be between 0 dB and –6 dB. If the readout dropped more than approximately 6 dB, the A11 Input assembly is probably faulty.

5. Disconnect the cable connected to A12 J3, press [**Meas Restart**], and wait for ten averages. The Δ **Mkr** readout should be between 0 dB and –6 dB. If the readout dropped more than approximately 6 dB, the A12 First Conversion assembly is probably faulty.

6. Disconnect the cable connected to A13 J3, press [**Meas Restart**], and wait for ten averages. The Δ **Mkr** readout should be between 0 dB and –6 dB. If the readout dropped more than approximately 6 dB, the A13 Second Conversion assembly is probably faulty. If the readout is correct, A61 IF assembly is probably faulty.

Test 26. Noise Level

Use this test to determine which of the following assemblies is causing the Noise Level performance test to fail:

- A61 IF
- A62 ADC/Digital Filter
- A12 First Conversion
- A11 Input
- A13 Second Conversion

Note

The A11 Input assembly dominates the low frequency noise level. Therefore, if the failing frequencies are below 30 kHz, the A11 Input assembly is probably faulty.

If failures only occurred using the 1 MΩ input impedance, the A11 Input assembly is probably faulty.

---

1. Load the HP 3589A performance test software (see chapter 3, "How to Load the ITM_3589A Program").
2. Press the following keys:

   [TEST CONFIG]
   [STOP AFTER]
   [LIMIT FAILURE]
   [PROCEDURE]
   [PERFORMAN]
   [RETURN]
   [START TESTING]
   [ONE TEST]
   [NOISE LEVEL]

3. After the program stops on the failure, press the following keys:

   [**BASIC**]
   [**Trigger**]
   [ARM **AUTO** MAN]
   [**Marker**]
   [ZERO OFFSET]

4. Disconnect the cable connected to A11 J3. The Δ **Mkr** readout should be > – 2 dB/Hz. If the readout dropped more than approximately 4 dB when A11 J3 is disconnected, the A11 Input assembly is probably faulty.
5. Disconnect the cable connected to A12 J3. The Δ **Mkr** readout should be > – 2 dB/Hz. If the readout drops more than approximately 4 dB when A12 J3 is disconnected, the A12 First Conversion assembly is probably faulty.

6. Disconnect the cable connected to A13 J3. The Δ **Mkr** readout should be > – 2 dB/Hz. If the readout drops more than approximately 4 dB when A13 J3 is disconnected, the A13 Second Conversion assembly is probably faulty.

7. Disconnect the cable connected to A61 J3 and terminate A62 J3 into 50 Ω. The Δ **Mkr** readout should be > – 4 dB/Hz. If the readout drops more than approximately 6 dB when A61 J3 is disconnected, the A61 IF assembly is probably faulty. If the readout is correct, A62 ADC/Digital Filter assembly is probably faulty.

Test 27. Frequency Accuracy

Use this test to determine if the A31 Reference/Calibrator assembly or the optional A91 Fan Power/Oven assembly is causing the Frequency Accuracy performance test to fail.

Note

If the frequency accuracy performance test failed without option 1D5, the A31 Reference/Calibrator assembly is probably faulty.

The calculated frequency specification is based on the number of months since the last frequency adjustment. If unsure of the date, do the adjustment and repeat the performance test. If the performance test is done immediately after the adjustment, use zero for the number of months, otherwise use one.

---

1. Remove the rear panel jumper (OVEN REF OUT to EXT REF IN) and connect OVEN REF OUT to a frequency counter.
2. Divide the lower and upper frequency limit specifications calculated in the performance test by ten and compare to OVEN REF OUT.
3. If OVEN REF OUT is within specification, the A31 Reference/Calibrator assembly is probably faulty. If OVEN REF OUT is not within specification, the A91 Fan Power/Oven assembly is probably faulty.

Test 28. Spurious Responses

Table 4-30 lists spur types and the assembly or assemblies most likely to cause the failure.

If the A52 Fractional-N assembly is listed as the probable faulty assembly but the performance test still fails after replacing the assembly and doing the required adjustments (see table 6-1), the probable faulty assembly is listed below in order of probability:

- A51 Interpolation VCO
- A21 Sum VCO
- A22 Sum Phase Detector
- A24 Step VCO
- A23 Step Phase Detector

If the A22 Sum Phase Detector assembly is listed as the probable faulty assembly but the performance test still fails after replacing the assembly, the probable faulty assembly is listed below in order of probability:

- A21 Sum VCO
- A24 Step VCO
- A23 Step Phase Detector
- A52 Fractional-N
- A51 Interpolation VCO

Table 4-30. Spur Types

Source Frequency (MHz)	Spur Frequency (MHz)	Spur Type	Probable Faulty Assembly
7 8125	10.8428	sum reference	A22 Sum Phase Detector A21 Sum VCO
9 8125	9.8248	step comb	A22 Sum Phase Detector
149 8125	149.8248	step comb	A22 Sum Phase Detector
95.81274	95.81254	API 1	A52 Fractional-N †
95 8149	95.8129	API 1	A52 Fractional-N †
100.79274	100.79254	API 1	A52 Fractional-N †
100.7949	100.7929	API 1	A52 Fractional-N †
100 79454	100.79254	API 2	A52 Fractional-N †
100 794504	100.792504	API 3	A52 Fractional-N †
100 7945004	100.7925004	API 4	A52 Fractional-N †
1 8125	4.81373	3 MHz sideband on sum loop	A22 Sum Phase Detector A21 Sum VCO
7 81496	4.81373	3 MHz sideband on sum loop	A22 Sum Phase Detector A21 Sum VCO
144 8125	144.822623	10 123 kHz sideband on signal	A22 Sum Phase Detector A21 Sum VCO
144 832746	144.822623	10 123 kHz sideband on signal	A22 Sum Phase Detector A21 Sum VCO
89 9125	89.8125	100 kHz sideband	A52 Fractional-N †

† Before replacing the A52 Fractional-N assembly, go to chapter 5 and do adjustment 6. 100 kHz and API Spurs. Do not try to adjust the spurs using the performance test setup. The setup in the performance test is not the same as the setup for the adjustment. After replacing the assembly, do adjustment 6 before repeating the performance test.

Test 29. Input Harmonic Distortion

Use this test to determine if the A11 Input assembly or the A12 First Conversion assembly is causing the Input Harmonic Distortion performance test to fail.

Note

If failures only occurred in the 1 MΩ input impedance path, the A11 Input assembly is probably faulty.
If failures only occurred with low distortion mode on or off, but not both, the A11 Input assembly is probably faulty.

---

1. Press the following keys:

   [**Preset**]
   [**Special Fctn**]
   [SINGLE CAL]
   [AUTO CAL ON **OFF**]
   [**Range/Input**]
   [RANGE]
   0
   [dBm]
   [**Res BW**]
   [RES BW]
   4.5
   [Hz]
   [**Sweep**]
   [SWEEP AUTO **MAN**]
   [**Avg/Pk Hld**]
   [AVERAGE]
   [**Meas Type**]
   [LOW DIST ON OFF] (to failing mode)

2. Connect the test equipment as shown in figure 4-20.

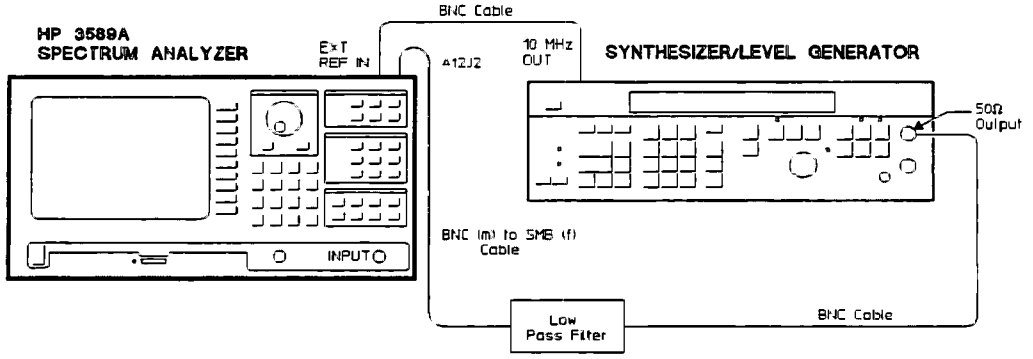


Figure 4-20. Troubleshooting Input Harmonic Distortion

3. Set the synthesizer/level generator as follows:

Amplitude	–28 dBm
Frequency	(to fundamental frequency of failing harmonic)

4. Press the following keys:

[Sweep]
[MANUAL FREQ] (to fundamental frequency of failing harmonic)
[Marker]
[ZERO OFFSET]
[Sweep]
[MANUAL FREQ] (to failing harmonic)

5. If the Δ **Man** readout is now within specification, the A11 Input assembly is probably faulty. If the Δ **Man** readout is still failing, the A12 First Conversion assembly is probably faulty.

Test 30. Intermodulation Distortion

Use this test to determine which of the following assemblies is causing the Intermodulation Distortion performance test to fail:

- A61 IF
- A12 First Conversion
- A11 Input

Note

If failures only occurred using the 1 MΩ input impedance path or the 50 Ω input impedance path, but not both, the A11 Input assembly is probably faulty.
If failures only occurred at 23.634734 MHz or 23.640148 MHz, the A61 IF assembly is probably faulty.

---

1. Load the HP 3589A performance test software (see chapter 3, "How to Load the ITM_3589A Program").
2. Press the following keys:

   [TEST CONFIG]
   [STOP AFTER]
   [LIMIT FAILURE]
   [PROCEDURE]
   [PERFORMAN]
   [RETURN]
   [START TESTING]
   [ONE TEST]
   [MORE]
   [INTERMODU DIST]

3. Connect the test equipment as shown in figure 4-21.

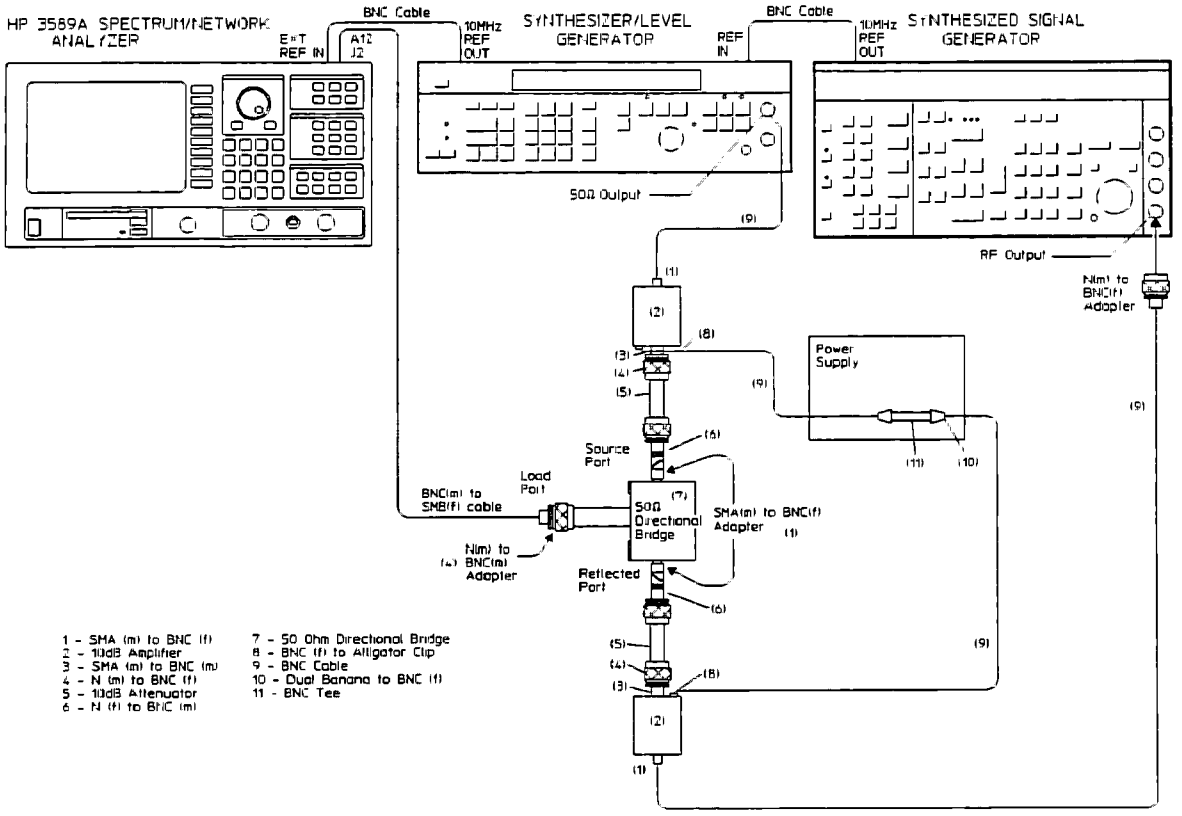


Figure 4-21. Troubleshooting Intermodulation Distortion

4. Press the [CONTINUE] softkey, then follow the directions on the screen until the message "Connect a 50 Ohm feedthrough termination between the bridge and the HP 3589A input" appears.

5. If the 50 Ω input impedance path now passed, the A11 Input assembly is probably faulty. If the 50 Ω input impedance path still failed, the A12 First Conversion assembly is probably faulty.

Test 31. Source Response

Use this test to determine if the A42 Source Conversion assembly or the A41 Source Amplifier assembly is causing the Source Amplitude Accuracy and Frequency Response performance test to fail.

Note

If the Source Dynamic Accuracy performance test also fails, the A42 Source Conversion assembly is probably faulty.

Before replacing the A42 Source Conversion assembly, check the Source Bandpass Filter adjustment.

---

1. Connect A42 J1 to the front panel INPUT connector using an SMB-to-BNC cable.
2. Press the following keys:

   [**Preset**]
   [**Special Fctn**]
   [AUTO CAL ON **OFF**]
   [**Source**]
   [SOURCE **ON** OFF]
   [**Scale**]
   [REFERENCE LEVEL]
   –41
   [dBm]
   [VERTICAL/DIV]
   1
   [dB]

3. The signal's amplitude should be – 46 dBm ± 3 dB, and its flatness should be ± 1 dB relative to the amplitude at 300 kHz. If the signal is correct, the A41 Source Amplifier is probably faulty. If the signal is incorrect, the A42 Source Conversion assembly is probably faulty. Before replacing the A42 Source Conversion assembly, check the Source Bandpass Filter adjustment.

Troubleshooting Miscellaneous Failures

The following tests provide troubleshooting information for miscellaneous failures that are not detected by the self tests.

Test 32. Memory Battery

Use this test when battery-backed-up memory is suspected of failing. This test separates Memory assembly failures from memory battery failures.

1. Press the following keys:

   [Preset]
   [Special Fctn]
   [NON-VOL SETUP]
   [DATE MMDDYY]
   010101
   [ENTER]

2. Set the power switch to STANDBY (⏻), then to ON (I).

3. Press the following keys:

   [Special Fctn]
   [NON-VOL SETUP]
   [DATE MMDDYY]

4. If the date is 01/01/01, the battery-backed-up memory is functioning correctly, go to Test 9. Self Test to continue troubleshooting.

5. If the date is incorrect, remove the Memory assembly (see the disassembly/assembly illustrations in chapter 6, "Replacing Assemblies").

6. Check the voltage at B402. If the voltage is 3.7 ± 1V, the Memory assembly is probably faulty. If the battery voltage is incorrect, replace the battery.

Note

Set the analyzer's HP-IB address after replacing the battery or the Memory assembly (see "Replacing the Memory Assembly" in chapter 6, "Replacing Assemblies").

Test 33. Fan Power

Use this test when the analyzer is operating correctly, but the fan on the BNC connector side of the analyzer is not working. This test determines which of the following is faulty:

- Motherboard
- A90 Fan Power assembly or optional A91 Fan Power/Oven assembly
- Fan

1. Set the power switch to STANDBY (⏻), and disconnect the power cord from the rear panel. Remove the top cover, rear panel, and fan/oven housing (see figures 6-2, 6-3, and 6-10 in chapter 6, "Replacing Assemblies").

2. Disconnect the connector with the yellow, red, and black wires from the A90 Fan Power assembly or the optional A91 Fan Power/Oven assembly (see figure 6-11).

3. Set the power switch to ON (I). Check that the voltage at the yellow wire is -18 ± 2V and the voltage at the red wire is $+18 \pm 2$V. If either voltage is incorrect, the motherboard or the wire is probably faulty.

4. Set the power switch to STANDBY (⏻). Reconnect the connector with yellow, red, and black wires, and disconnect the connector with the red and black wires.

5. Set the power switch to ON (I) and check that J3 pin 2 is -18 ± 2V. If the voltage is correct, the fan is probably faulty. If this voltage is incorrect, the A90 Fan Power assembly or the optional A91 Fan Power/Oven assembly is probably faulty.

Test 34. Trigger/Gate

Use this test when the analyzer is operating correctly, but the HP-IB trigger or external trigger/gate is not functioning. This test determines if the A33 Trigger assembly or A81 CPU assembly is faulty.

1. If the analyzer triggers using external trigger and does not trigger using HP-IB trigger, do the following:

   a. Set the power switch to STANDBY (⏻), and disconnect the power cord and HP-IB cable from the rear panel. Remove the top cover and place the Power Supply assembly in its test position (see figures 6-2, 6-3, and 6-5 in chapter 6, "Replacing Assemblies"). Disconnect the motherboard power cable (W12) from J2 on the Power Supply assembly. Reconnect the power cord and HP-IB cable.

   b. Set the power switch to ON (I), then press the following keys:
   [Trigger]
   [HP-IB TRIGGER]

   c. Using a logic probe, monitor J2 pin 1 (see figure 4-22) while sending an HP-IB trigger. If the signal at J2 pin 1 toggled when the HP-IB trigger occurred, the A33 Trigger assembly is probably faulty. If the signal did not toggle, the A81 CPU assembly is probably faulty.

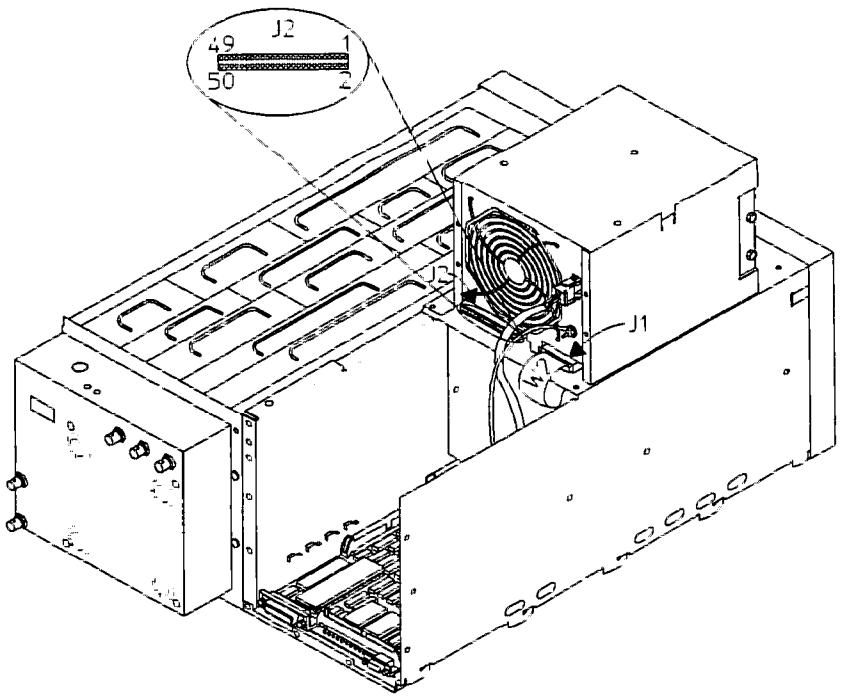


Figure 4-22. Troubleshooting Trigger/Gate

2. Press the following keys:

   [Special Fctn]
   [F9]
   – 99
   [F9]
   [SERVICE FUNCTIONS]
   [SELF TEST]
   [FUNCTIONL TESTS]
   [RECEIVER]
   [TRIGGER]

3. If the Trigger/Gate self-test fails, the A33 Trigger assembly is probably faulty. Before replacing the assembly, go to step 9 to check the voltages at the connector.

4. Set a synthesizer for a 2 Hz, 5 Vp-p square wave.

5. Using a BNC cable, connect the synthesizer's output to EXT TRIG/GATE on the rear panel.

6. Press the following keys:

   [Preset]
   [Trigger]
   [EXTERNAL TRIGGER]

7. The analyzer should briefly display WAITING FOR TRIGGER between each sweep. If this did not occur, the A33 Trigger assembly is probably faulty. Before replacing the assembly, go to step 9 to check the voltages at the connector.

8. Using a logic probe, check that TRIG/GATE OUT on the rear panel toggles between a TTL high and TTL low level. If this did not occur, the A33 Trigger assembly is probably faulty. Do the next step before replacing the assembly.

9. Before replacing the probable faulty assembly, do the following to check that the voltages from the power supply assembly are present at the assembly's motherboard connector:

   a. Set the power switch to STANDBY (⏻). Remove the screw at each end of the suspected assembly. Remove the assembly and place an extender board in the card nest.

   b. Set the power switch to ON (I), then measure the pins of the extender board for correct voltages (see table 9-12 on page 9-24).

Test 35: DIN Connector

Use this test to determine if the fuse for the DIN connector is failing before replacing the A72 Keyboard assembly.

1. Set the power switch to ON (I).
2. Check the voltage on pin 4 of the DIN connector for +5V (see figure 4-23).
3. If the voltage is correct, the A72 Keyboard assembly is probably faulty.
4. If the voltage is not correct, replace A72 F300 (see figure 4-24).

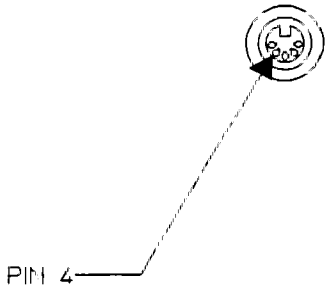


Figure 4-23. DIN Connector

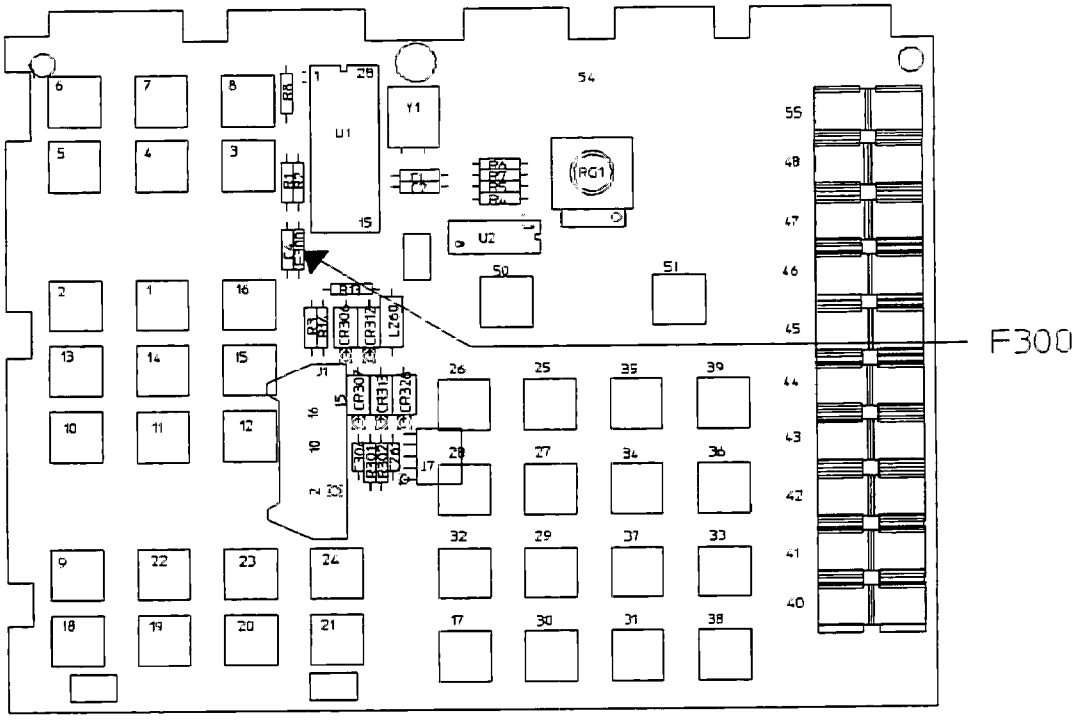


Figure 4-24. A72 Component Locator

Troubleshooting the HP 35689A/B

Before starting Test 36. HP 35689A/B Initial Verification, check that the voltage selector switch on the rear of the test set is set for the local line voltage. Also check that the correct line fuse is installed in the rear panel fuse holder. For information on the voltage selector switch and the line fuse, see "HP 35689A/B Power Requirements" in chapter 2.

Note

All functional self tests in Test 9. Self Test must pass before troubleshooting the test set.

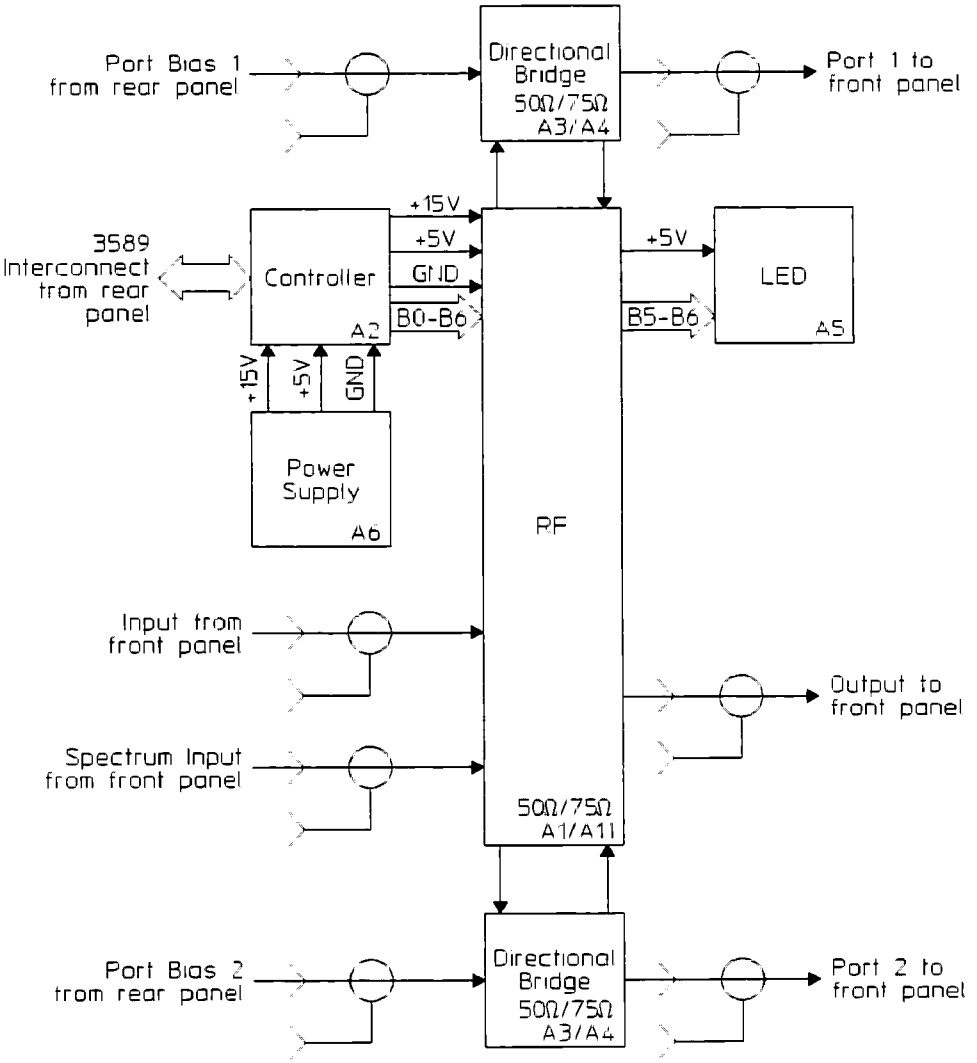


Figure 4-25. HP 35689A/B Overall Block Diagram

Test 36. HP 35689A/B Initial Verification

Use this test when the HP 35689A/B S-Parameter Test Set is suspected of failing and all the self tests for the HP 3589A Spectrum/Network Analyzer pass.

1. If the test set is already connected to the analyzer, go to step 2. If the test set is not connected to the analyzer, do the following:

   a. Set the analyzer's power switch to STANDBY (⏻) and the test set's power switch to OFF (o). Remove the test set's top cover (see the disassembly/assembly illustrations in chapter 6).

   b. Position the test set on its side next to the analyzer's display (see figure 4-26). Using 50 Ω N cables, connect the test set's INPUT connector to the analyzer's SOURCE connector and the test set's OUTPUT connector to the analyzer's INPUT connector. Using the interconnect cable, connect the analyzer's PORT 1 connector to the test set's 3589 INTERCONNECT connector.

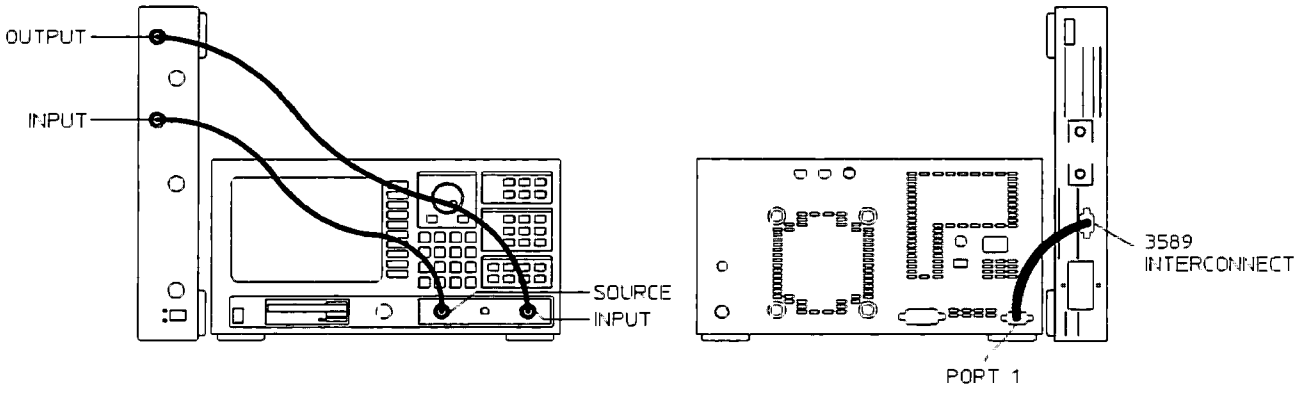


Figure 4-26. Troubleshooting Setup

2. Set the power switch to ON (I) on both the analyzer and test set. Press the following keys:

   [Preset]
   [Special Fctn]
   [F9]
   – 99
   [F9]
   [AUTO CAL ON **OFF**]
   [SERVICE FUNCTIONS]
   [SELF TEST]

3. Press the [TEST SET] softkey and listen for a clicking sound made by the relays when they change positions.

4. Press the [TEST LOG] softkey and compare the test log and the test set's symptoms to table 4-31. If the symptoms or test log matches more than one entry in the table, use the entry closest to

the beginning of the table. The table lists the probable faulty assembly or assemblies and any troubleshooting procedures to help isolate the failure.

Note

Table 4-31 lists the assembly or assemblies most likely to cause the failure. Multiple probable faulty assemblies are listed in order of probability.

Table 4-31. Test Set Troubleshooting Guide

Symptom or Test Log Message	Probable Faulty Assembly	Troubleshooting Test or Next Step
Test Set softkey not active	A2 Controller A6 Power Supply HP 3589A Interconnect cable	Step 5
Test Set self test fails and		
test log message: Invalid response to relay drive query	A2 Controller A6 Power Supply	Step 5
test log message:Relay drive bits set in error: nx n.	A2 Controller A6 Power Supply	Step 5
test log message:Relay drive bits cleared in error: nx n.	A2 Controller A6 Power Supply	Step 5
relays did not make a clicking sound	A1/A11 RF A6 Power Supply	Step 5
relays made a clicking sound	A1/A11 RF A3/A4 Directional Bridge	Test 37 for HP 35689A Test 38 for HP 35689B
Test Set self test passes but ..		
performance test fails	Connectors, cables, terminations A3/A4 Bridge of failing port	Step 6
SPECTRUM INPUT fails	A1/A11 RF	
port bias not working correctly	Rear panel cable to bridge A3/A4 Bridge of failing port	
front panel LED not working	A5 LED	

Note

The Test Set self test fails if the forward or reverse reference path flatness is greater than 20 dB or if the maximum reference path ratio is greater than 2 dB.

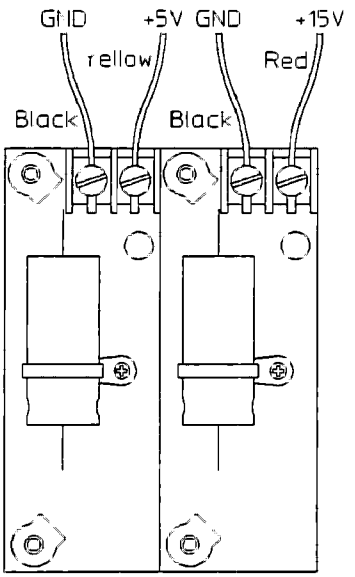


Figure 4-27. Power Supply Test Locations

5. Before replacing the probable faulty assembly, check the power supply's voltages to determine that the power supply is not causing the failure. The voltage at the screw connecting the yellow wire should be +5 V ± 0.25 V and the voltage at the screw connecting the red wire should be +15 V ± 0.75 V (see figure 4-27 for test locations).

6. If a directional bridge is suspected of failing, do the following:

   a. Do the "Directivity and Source Match" performance test (see the *HP 3589A Performance Test Guide*). If only one port fails, go to step c.

   b. Do the "Return Loss" performance test (see the *HP 3589A Performance Test Guide*). If the S_{11} measurement fails, then the Port 1 Directional Bridge assembly is the probable faulty assembly. If the S_{22} measurement fails, then the Port 2 Directional Bridge assembly is the probable faulty assembly. Before replacing the assembly, do the next step.

   c. Examine all connectors to the Directional Bridge assemblies. Damaged connectors can cause performance test failures. The Directional Bridge assembly's PORT connector can cause directivity failures and the PORT connector is the most common connector failure.

Test 37. HP 35689A Self Test Fails

Use this test to isolate the failure to the A1 RF assembly or to one of the A3 Directional Bridge assemblies. Figure 4-28 shows the signal paths through the RF and Directional Bridge assemblies during the various measurements.

Note

"Test 36. HP 35689A/B Initial Verification" must be done before the probable causes listed in this test are valid.

The test set is in its test position (see figure 4-26). The analyzer's SOURCE is connected to the test set's INPUT, the test set's OUTPUT is connected to the analyzer's INPUT. PORT 1 and PORT 2 are not connected.

---

1. Set the power switch to ON (I) on both the test set and the analyzer.
2. Press the following keys:

   [**Preset**]
   [**Meas Type**]
   [SWEPT SPECTRUM]
   [**Source**]
   [SOURCE **ON** OFF]
   [SOURCE AMPLITUDE]
   10
   [dBm]
   [**Special Fctn**]
   [F9]
   –99
   [F9]
   [AUTO CAL ON **OFF**]
   [SERVICE FUNCTIONS]
   [TEST SET CONFIG]
   [FORWARD REFERENCE]

3. The signal's amplitude should be –9 dBm ± 4 dB from 100 kHz to 150 MHz. If the signal is incorrect, the A1 RF assembly is probably faulty.
4. Disconnect the cable connected to the test set's INPUT connector. Connect the cable to the test set's SPECTRUM INPUT connector (the analyzer's SOURCE is connected to the test set's SPECTRUM INPUT).
5. Press the following keys:

   [SPECTRUM PORT]

6. The signal's amplitude should be 10 dBm ± 4 dB from 100 kHz to 150 MHz. If the signal is incorrect, the A1 RF assembly is probably faulty.

7. Disconnect the cable connected to the test set's SPECTRUM INPUT connector. Connect the cable to the test set's INPUT connector (the analyzer's SOURCE is connected to the test set's INPUT). Connect an N short to the test set's PORT 1 connector.

8. Press the following key:

   [FORWARD REFLECTN]

9. The signal's amplitude should be –9 dBm ± 4 dB from 100 kHz to 150 MHz. If the signal is correct, go to the next step. If the signal is incorrect, check the signals in table 4-32 in the order listed using the analyzer.

Table 4-32. Forward Reflection

Test Location	Amplitude 100 k - 150 MHz (± 4 dB)	Output Impedance	Probable Faulty Assembly
A1 J8 †	10 dBm	50 Ω	A1 RF
PORT 1 ‡ (remove short)	–3 dBm	50 Ω	Directional Bridge Port 1 N Connector
Directional Bridge J2 † (with short)	–9 dBm	50 Ω	Directional Bridge

† Use an N(m)-to-BNC(f) adapter, a BNC cable, and a BNC(f)-to-SMA(m) adapter.
‡ Use a 50 Ω N cable.

10. If disconnected, reconnect the test set's OUTPUT connector to the analyzer's INPUT connector. Disconnect the N short from the test set's PORT 1 connector and connect the N short to the test set's PORT 2 connector.

11. Press the following key:

    [REVERSE REFLECTN]

12. The signal's amplitude should be –9 dBm ± 4 dB from 100 kHz to 150 MHz. If the signal is correct, the A1 RF assembly is probably faulty. If the signal is incorrect, check the signals in table 4-33 in the order listed using the analyzer.

Table 4-33. Reverse Reflection

Test Location	Amplitude 100 k - 150 MHz (± 4 dB)	Output Impedance	Probable Faulty Assembly
A1 J7 †	10 dBm	50 Ω	A1 RF
PORT 2 ‡ (remove short)	–3 dBm	50 Ω	Directional Bridge Port 2 N Connector
Directional Bridge J2 † (with short)	–9 dBm	50 Ω	Directional Bridge

† Use an N(m)-to-BNC(f) adapter, a BNC cable, and a BNC(f)-to-SMA(m) adapter.
‡ Use a 50 Ω N cable.

Test 38. HP 35689B Self Test Fails

Use this test to isolate the failure to the A11 RF assembly or to one of the A4 Directional Bridge assemblies. Figure 4-28 shows the signal paths through the RF and Directional Bridge assemblies during the various measurements.

Note

"Test 36. HP 35689A/B Initial Verification" must be done before the probable causes listed in this test are valid.

The test set is in its test position (see figure 4-26). The analyzer's SOURCE is connected to the test set's INPUT, the test set's OUTPUT is connected to the analyzer's INPUT. PORT 1 and PORT 2 are not connected.

Caution

The HP 35689B Test Set has both 50 Ω and 75 Ω N connectors. If a 50 Ω cable or adapter is connected to one of the 75 Ω connectors, the 75 Ω connector will be damaged.

---

1. Set the power switch to ON (I) on both the test set and the analyzer.
2. Press the following keys:

   [**Preset**]
   [**Meas Type**]
   [SWEPT SPECTRUM]
   [**Source**]
   [SOURCE **ON** OFF]
   [SOURCE AMPLITUDE]
   9
   [dBm]
   [**Special Fctn**]
   [F9]
   –99
   [F9]
   [AUTO CAL ON **OFF**]
   [SERVICE FUNCTIONS]
   [TEST SET CONFIG]
   [FORWARD REFERENCE]

3. The signal's amplitude should be –10 dBm ± 4 dB from 100 kHz to 150 MHz. If the signal is incorrect, the A11 assembly is probably faulty.

4. Disconnect the cable connected to the test set's INPUT connector. Using a 50 Ω N(m)-to-BNC(f) adapter, a 25 Ω series resistor, a 75 Ω BNC cable, and a 75 Ω N(m)-to-BNC(f) adapter, connect the analyzer's SOURCE to the test set's SPECTRUM INPUT.

5. Press the following key:

   [SPECTRUM PORT]

6. The signal's amplitude should be 12.9 dBm ± 4 dB from 100 kHz to 150 MHz. If the signal is incorrect, the A11 RF assembly is probably faulty.

7. Disconnect the cable and adapters connecting the analyzer's SOURCE to the test set's SPECTRUM INPUT. Connect the analyzer's SOURCE to the test set's INPUT using a 50 Ω N cable. Connect a 75 Ω N short to the test set's PORT 1 connector.

8. Press the following key:

   [FORWARD REFLECTN]

9. The signal's amplitude should be –10.6 dBm ± 4.2 dB from 100 kHz to 150 MHz. If the signal is correct, go to the next step. If the signal is incorrect, check the signals in table 4-34 in the order listed using the analyzer.

Table 4-34. Forward Reflection

Test Location	Amplitude 100k - 150 MHz (± 4.3 dB)	Output Impedance	Probable Faulty Assembly
A11 J8 †	14.7 dBm	50 Ω	A11 RF
PORT 1 ‡ (remove short)	–0.4 dBm	75 Ω	Directional Bridge Port 1 N Connector
Directional Bridge J2 † (with short)	–10.6 dBm	50 Ω	Directional Bridge

† Use a SMA(m)-to-Right Angle SMA(m) cable and a 50 Ω N(m)-to-SMA(f) adapter.
‡ Use a 75 Ω N(m)-to-BNC(f) adapter, a 75 Ω BNC cable, a 25 Ω series resistor, and a 50 Ω N(m)-to-BNC(f) adapter.

10. If disconnected, reconnect the test set's OUTPUT connector to the analyzer's INPUT connector. Disconnect the 75 Ω N short from the test set's PORT 1 connector and connect the 75 Ω N short to the test set's PORT 2 connector.

11. Press the following key:

    [REVERSE REFLECTN]

12. The signal's amplitude should be –10.6 dBm ± 4.2 dB from 100 kHz to 150 MHz. If the signal is correct, the A11 RF assembly is probably faulty. If the signal is incorrect, check the signals in table 4-35 in the order listed using the analyzer.

Table 4-35. Reverse Reflection

Test Location	Amplitude 100k - 150 MHz (± 4.3 dB)	Output Impedance	Probable Faulty Assembly
A11 J7 †	14 7 dBm	50 Ω	A11 RF
PORT 2 ‡ (remove short)	–0.4 dBm	75 Ω	Directional Bridge Port 2 N Connector
Directional Bridge J2 † (with short)	–10.6 dBm	50 Ω	Directional Bridge

† Use a SMA(m)-to-Right Angle SMA(m) cable and a 50 Ω N(m)-to-SMA(f) adapter.

‡ Use a 75 Ω N(m)-to-BNC(f) adapter, a 75 Ω BNC cable, a 25 Ω series resistor, and a 50 Ω N(m)-to-BNC(f) adapter.

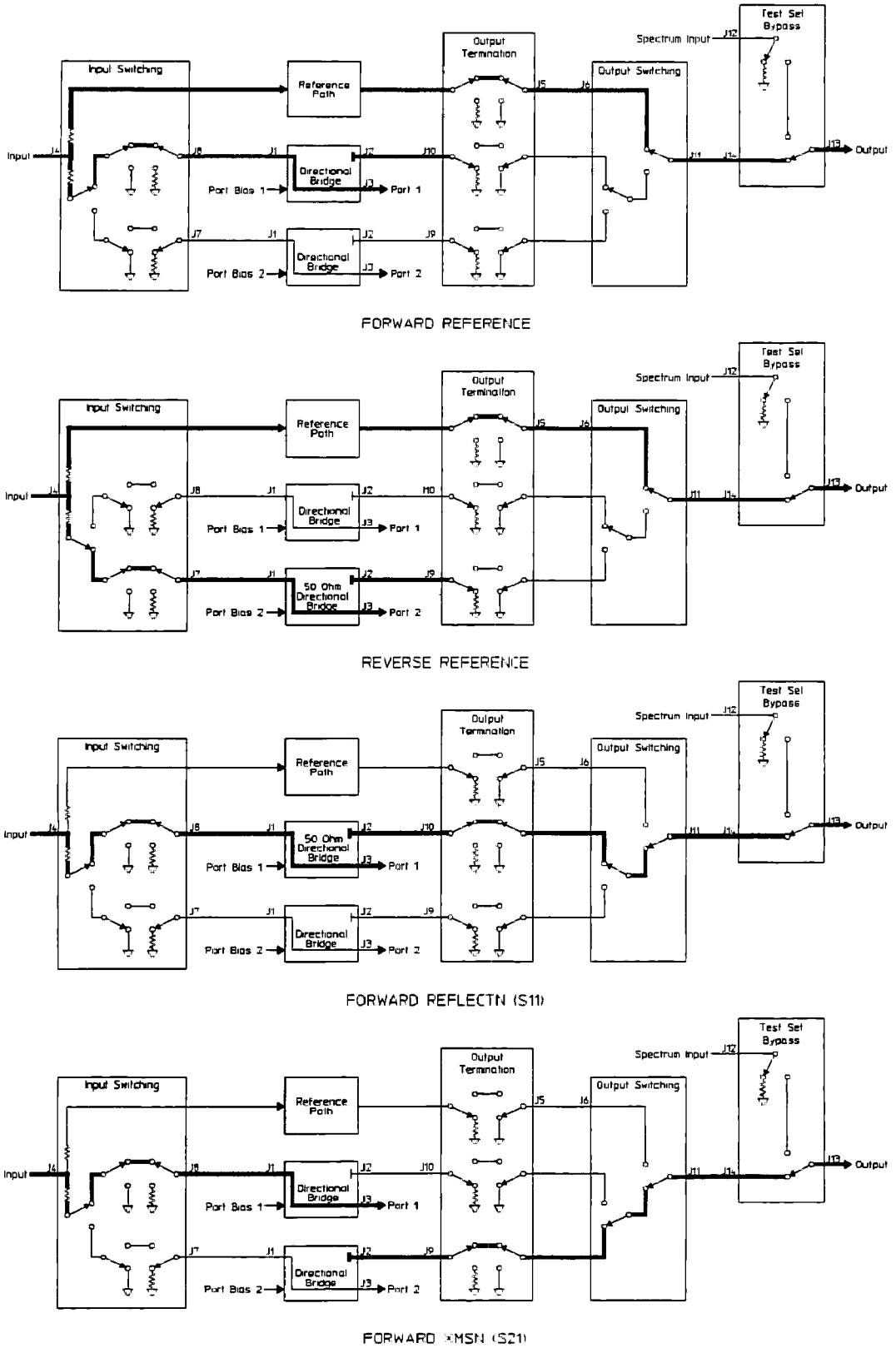
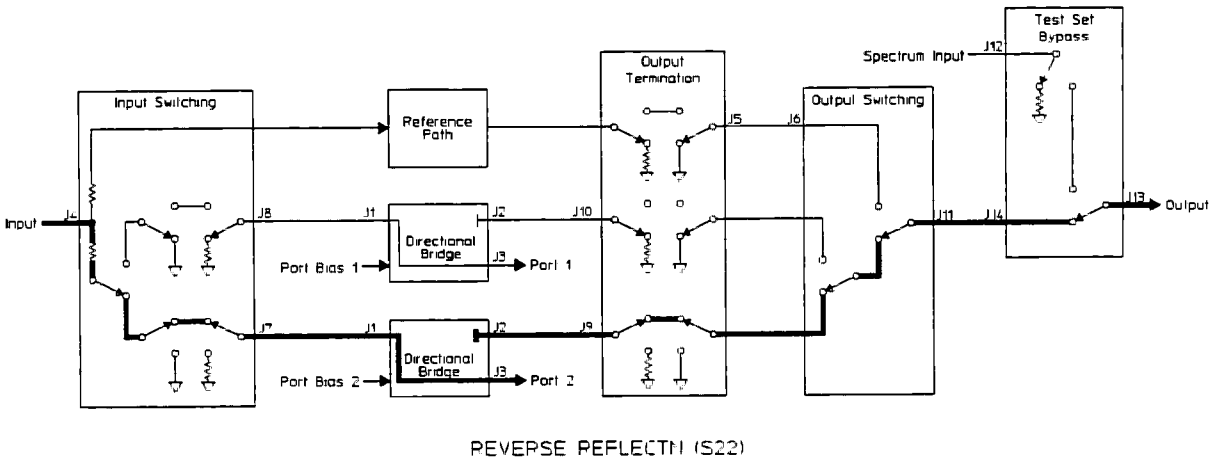
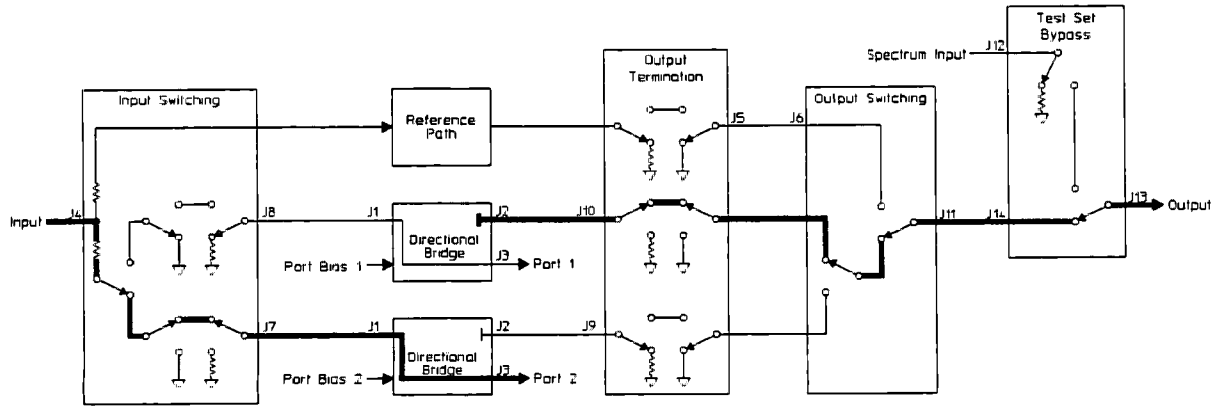


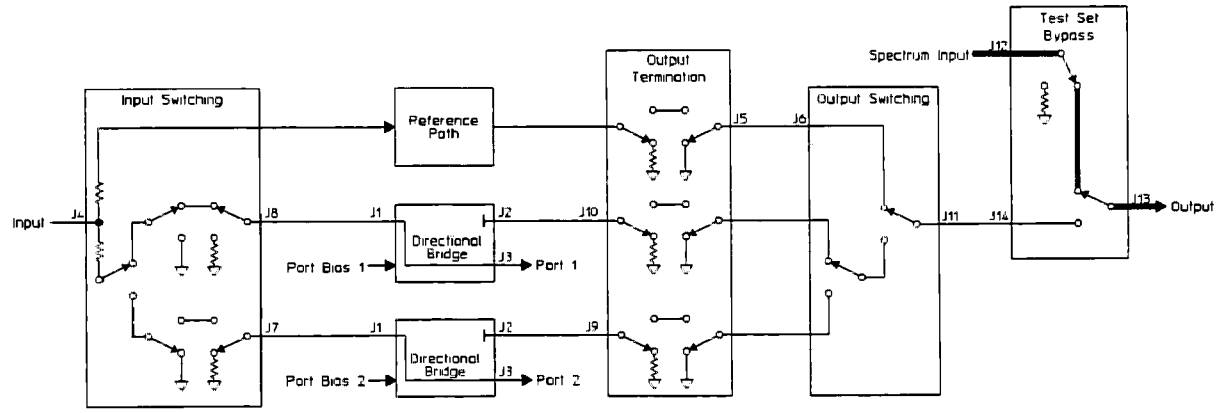
Figure 4-28. HP 35689A/B Signal Paths



REVERSE REFLECTN (S22)



REVERSE XMSN (S12)



SPECTRUM PORT

Figure 4-28. HP 35689A/B Signal Paths (continued)

5

Adjusting the HP 3589A

How to Use This Chapter

This chapter contains the adjustment procedures for the HP 3589A Spectrum/Network Analyzer. The HP 35689A/B S-Parameter Test Set does not have any adjustments. Use these adjustments if the analyzer does not meet its specifications or if instructed in chapter 4, "Troubleshooting the Analyzer," or chapter 6, "Replacing Assemblies," to perform these adjustments. These adjustments are not required for routine maintenance. Table 5-1 lists all the adjustments.

The top cover must be removed to perform all adjustments except "1. Oven Shutdown" and "16. Oven Frequency." For information on top cover removal, see "Disassembly/Assembly" in chapter 6, "Replacing Assemblies."

Note

Allow the HP 3589A Spectrum/Network Analyzer to warm up for at least an hour. This is critical for adjustment "2. 80 MHz Reference VCXO." Analyzers with the oven option (option 1D5) must cool off for at least 8 hours before doing adjustment "1. Oven Shutdown" and warm up for at least 48 hours before doing adjustment "16. Oven Frequency."

During many of these adjustment procedures, an adjustment message appears on the screen. The instructions on the screen are not as complete as the instructions in this manual. When an adjustment message appears on the screen, continue to follow the instructions in this manual. Failure to follow the instructions in this manual may result in an incorrect adjustment, which would appear as a hardware failure.

Table 5-1. Adjustments

Adjustment Procedure	Assembly	Component
1 Oven Shutdown	A91	R2
2. 80 MHz Reference VCXO	A31	C6, R13
3 300 MHz Reference VCO	A32	L506, L508
4 Interpolation VCO	A51	L101
5 Single Loop Control Voltage Clamps	A52	R423, R422
6. 100 kHz and API Spurs	A52	R416, R518, R521, R533
7. Sum VCO Filter	A21	L106, L107
8. Multiple Loop Control Voltage Clamps	A23	R463, R461
9. Step VCO Filter	A24	L506, 507
10. Pretune Offset and Slope	A23	R452, R457
11. ADC Gain, Offset, and Reference	A62	R407, R405, R431
12. Second IF Bandpass Filter	A61	L3-L6, L8-L10, C30, R11
13. Source Bandpass Filter	A42	CAV ADJ 1-CAV ADJ 4
14. First IF Bandpass Filter	A12	CAV ADJ 1-CAV ADJ 4
15. Autorange Thresholds and 1 Meg Ohm Flatness	A11	C413, C421, C423, R624, R626
16. Oven Frequency	A91	U3, R12
17. Calibrator Flatness and Level	A31	R322, C330
18. Display	Display	VR31-VR34, VR41, VR42, VR64, VR67, L403

Note

If an assembly is replaced, see table 6-1 for required adjustments and performance tests.

Safety Considerations

Although the HP 3589A Spectrum/Network Analyzer is designed in accordance with international safety standards, this guide contains information, cautions, and warnings that must be followed to ensure safe operation and to keep the unit in safe condition. Adjustments in this chapter are performed with power applied and protective covers removed. These adjustments must be performed by trained service personnel who are aware of the hazards involved (such as fire and electrical shock).

Warning

Any interruption of the protective (grounding) conductor inside or outside the unit, or disconnection of the protective earth terminal can expose operators to potentially dangerous voltages.

Under no circumstances should an operator remove any covers, screws, shields or in any other way access the interior of the HP 3589A Spectrum/Network Analyzer. There are no operator controls inside the analyzer.

Equipment Required

Tables 1-5 and 1-8 list the recommended equipment. Any equipment which meets the critical specifications given in the tables may be substituted for the recommended model.

Remote Operation

Adjustments can be set up using the remote operation capability of the HP 3589A Spectrum/Network Analyzer. See table 5-2 for a list of adjustments and corresponding HP-IB codes. See the *HP 3589A HP-IB Programmer's Reference* for general information on remote operation.

Table 5-2. HP-IB Codes to Set Up Adjustments

Adjustments	HP-IB Codes
4. Interpolation VCO	DIAG:FRAC:VCO:ADJ
5. Single Loop Control Voltage Clamps	DIAG:FRAC:SLO:CHIG DIAG:FRAC:SLO:CLOW
6. 100 kHz and API Spurs	DIAG:FRAC:SPUR:NULL DIAG:FRAC:SPUR:API:ONE DIAG:FRAC:SPUR:API:TWO DIAG:FRAC:SPUR:API:FOUR
7. Sum VCO Filter	DIAG:FRAC:SUMV:LPF
8. Multiple Loop Control Voltage Clamps	DIAG:FRAC:MLO:CLOW DIAG:FRAC:MLO:CHIG
9. Step VCO Filter	DIAG:FRAC:SVCO:LPF
10. Pretune Offset and Slope	DIAG:FRAC:PRET:OFFS DIAG:FRAC:PRET:SLOP
11. ADC Gain, Offset, and Reference	DIAG:ADJ:ADC:GAIN DIAG:ADJ:ADC:OFFS
12. Second IF Bandpass Filter	DIAG:REC TWO:ONE DIAG:REC TWO:TWO DIAG:REC TWO:THR DIAG:REC:TWO:FOUR DIAG:REC TWO:FIVE
13. Source Bandpass Filter	DIAG:ADJ:SOUR:RES
14. First IF Bandpass Filter	DIAG:REC:HRES
15. Autorange Thresholds and 1 Meg Ohm Flatness	DIAG:REC:RANG:UP DIAG:REC.RANG:DOWN DIAG:REC MOHM FLAT DIAG:REC MOHM FLAT:STEP DIAG:REC:MOHM:FLAT:STEP
17. Calibrator Flatness and Level	DIAG:CAL:LEV TEST:SOUR:DAC:ATT 16 dB DIAG:CAL:STEP DIAG:CAL:STEP DIAG:CAL.FLAT TEST:SOUR:DAC:ATT 16 dB DIAG:CAL:STEP DIAG:CAL:STEP
18. Display	TEST:DISP:PATT

1. Oven Shutdown

This procedure adjusts the heater shutdown trip point on the optional A91 Fan Power/Oven assembly. When the oven is cold, the heater shutdown circuit disconnects the oven output from the rear panel output connector. After the oven has been on long enough for the frequency to be stable, the heater shutdown circuit connects the oven output to the rear panel output connector.

Equipment Required: Spectrum Analyzer
BNC Cable

Note

The HP 3589A Spectrum/Network Analyzer must be off for at least 8 hours before this adjustment is made. Once power is applied, the adjustment **MUST** be completed within **FIVE MINUTES.**

1. Remove the screw on the oven-adjustment cover. Lift the screw side of the oven-adjustment cover and tilt back to the open position.
2. Connect the spectrum analyzer to the OVEN REF OUT connector (located on rear panel) using a BNC cable.
3. Set the spectrum analyzer as follows:

Center Frequency	10 MHz
Frequency Span	1 MHz
Reference Level	– 60 dBm

4. Set the power switch to ON (I), then check that the amplitude of the 10 MHz signal is approximately – 70 dBm or lower (oven is cold).
5. Change the reference level on the spectrum analyzer to 10 dBm.
6. Turn OVEN SHUTDOWN (A91 R2) counterclockwise until the amplitude of the 10 MHz signal is > 0 dBm. Then turn OVEN SHUTDOWN clockwise until the amplitude of the signal just returns to approximately – 70 dBm and turn an additional 10 degrees clockwise.
7. Return the oven-adjustment cover and screw, and rear panel jumper (OVEN REF OUT to EXT REF IN) to their original positions.

2. 80 MHz Reference VCXO

This procedure adjusts the control voltage for the 80 MHz reference VCXO on the A31 Reference/Calibrator assembly. The 80 MHz reference is the primary frequency reference for the analyzer.

Equipment Required:
- Frequency Counter
- BNC(m)-to-SMB(f) Cable
- Flat-Edge Adjustment Tool

Note

Before doing this adjustment, make sure the HP 3589A Spectrum/Network Analyzer has been ON (I) for approximately one hour to allow the 80 MHz reference VCXO to reach a stable operating temperature.

1. Disconnect the rear panel jumper (OVEN REF OUT to EXT REF IN) on analyzers with the optional oven.
2. Disconnect the cable from A31 J3, and connect the frequency counter to A31 J3 using a BNC-to-SMB cable.
3. Adjust FREQ ADJ FINE (A31 R13) to the center of its adjustment range.
4. Adjust FREQ ADJ CRS (A31 C6) for 10 MHz ± 10 Hz using the flat-edge adjustment tool in the service kit.
5. Adjust FREQ ADJ FINE for 10 MHz ± 1 Hz.
6. Disconnect the frequency counter from A31 J3, and reconnect the cable from A61 J2 to A31 J3.
7. Reconnect the rear panel jumper on analyzers with the optional oven.

3. 300 MHz Reference VCO

This procedure adjusts the control voltage for the 300 MHz reference VCO on the A32 300 MHz assembly. The 300 MHz reference is the high-frequency reference for the analyzer.

Equipment Required: Digital Multimeter
Extender Board
Extender Cable

1. Set the power switch to STANDBY (⏻). Remove the screw at each end of the A32 300 MHz assembly, and place the assembly on an extender board.
2. Reconnect A32 J1 to A31 J9 using an extender cable.
3. Connect the multimeter's input terminal to A32 TP400 (see figure 5-1) and its ground terminal to chassis ground.

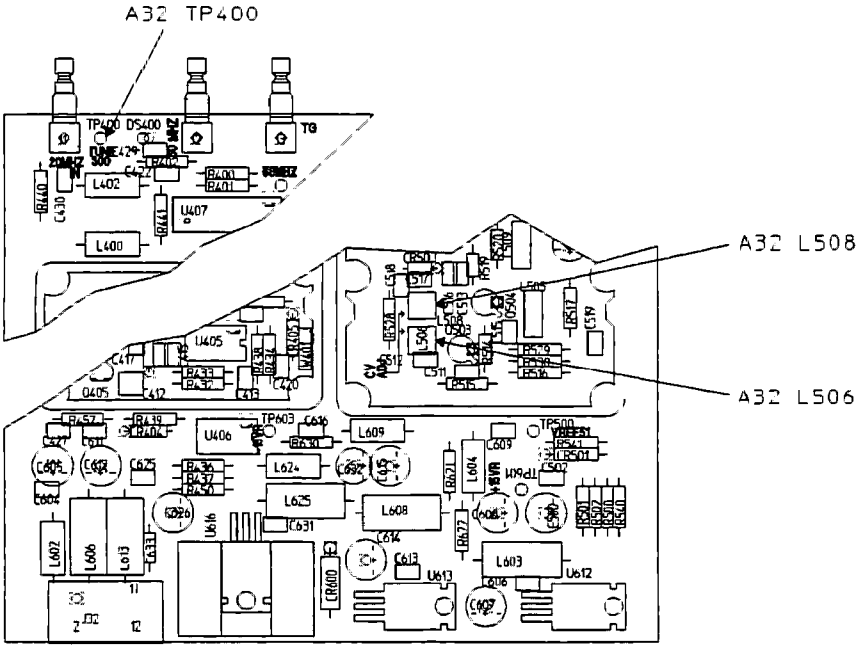


Figure 5-1. A32 300 MHz Component Locator

4. Set the power switch to ON (I). Through the holes in shield can, alternately adjust A32 L506 and L508 for -7.00 ± 0.25V.

5. Set the power switch to STANDBY (ϕ). Place the 300 MHz assembly into the card nest and replace the screws.

6. Reconnect the following using original cables:

   A32 J1 to A31 J9
   A32 J2 to A33 J1
   A32 J3 to A42 J3
   A32 J4 to A23 J2
   A32 J5 to A13 J1

4. Interpolation VCO

This procedure adjusts the frequency range of the interpolation VCO on the A51 Interpolation VCO assembly.

Equipment Required:

Frequency Counter
Extender Board
BNC(m)-to-SMB(f) Cable

1. Set the power switch to STANDBY (⏻). Remove the screw at each end of the A51 Interpolation VCO assembly, and remove the assembly from the card nest.

2. Move the jumper on A51 J101 to its test position (see figure 5-2). Place the assembly on an extender board.

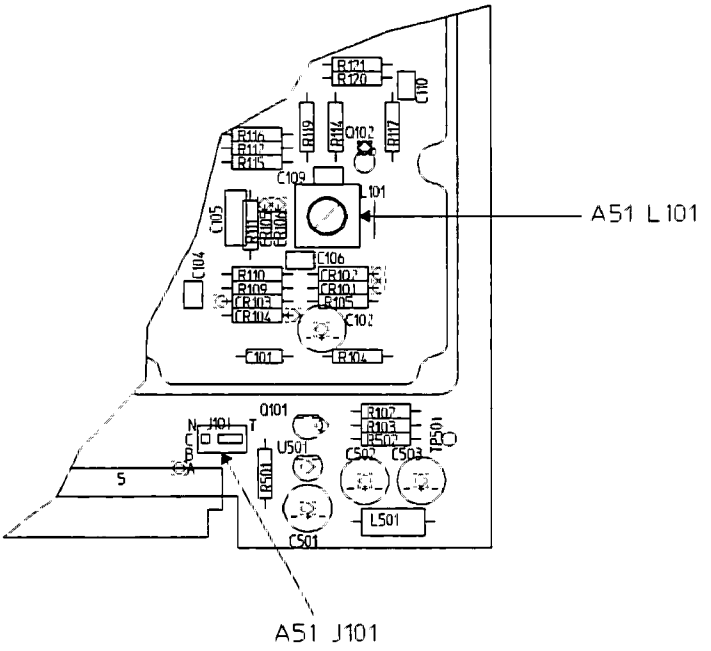


Figure 5-2. A51 Interpolation VCO Component Locator

3. Connect the frequency counter to A51 J4 using a BNC-to-SMB cable.

4. Set the power switch to ON (|), then press the following keys:

   [Special Fctn]
   [F9]
   – 99
   [F9]
   [SERVICE FUNCTIONS]
   [ADJUSTMTS]
   [LOCAL OSC]
   [INTRPL VCO]

5. Through the hole in the shield can, adjust A51 L101 for 55 ± 0.5 MHz using a plastic tuning tool.

6. Set the power switch to STANDBY (⏻). Move the jumper back to its normal position, and place the Interpolation VCO assembly into the card nest. Replace the screws.

7. Reconnect the following using original cables:

   A51 J1 to A22 J3
   A51 J2 to A21 J1
   A51 J3 to A52 J1
   A51 J4 (no connection)

5. Single Loop Control Voltage Clamps

This procedure adjusts the upper and lower out-of-limit voltages on the A52 Fractional-N assembly. The single loop control voltage is compared to the out-of-limit voltages. If the control voltage exceeds either the upper or lower out-of-limit voltage, the control voltage is clamped to the out-of-limit voltage.

Equipment Required: Frequency Counter
BNC(m)-to-SMB(f) Cable

1. Set the power switch to ON (|).
2. Disconnect the cable from A21 J3, and connect the frequency counter to A21 J3 using a BNC-to-SMB cable.
3. Press the following keys:
   [**Special Fctn**]
   [F9]
   – 99
   [F9]
   [SERVICE FUNCTIONS]
   [ADJUSTMTS]
   [LOCAL OSC]
   [SNGL LOOP CLAMPS
   [SNGL LOOP CLAMP-HI]
4. Disconnect the cable from A51 J3.
5. Adjust H.F.LIMIT (A52 R423) for 470 ± 2 MHz. If H.F.LIMIT cannot be adjusted to 470 ± 2 MHz, disconnect and reconnect A51 J3 until the loop unlocks and H.F.LIMIT can be adjusted.
6. Reconnect the cable from A51 J3 to A52 J1.
7. Press the [SNGL LOOP CLAMP-LOW] softkey.
8. Disconnect the cable from A52 J2.
9. Adjust L.F.LIMIT (A52 R422) for 290 ± 2 MHz.
10. Disconnect the frequency counter from A21 J3.
11. Reconnect A21 J3 to A12 J1 and A52 J2 to A33 J4.

6. 100 kHz and API Spurs

This procedure attenuates the 100 kHz sample and hold spur, and the API spurs on the A52 Fractional-N assembly.

Equipment Required:

Spectrum Analyzer
Extender Board
Extender Cables
BNC(m)-to-SMB(f) Cable
BNC Cable

1. Set the power switch to STANDBY (⏻). Remove the screw at each end of the A52 Fractional-N assembly, and place the assembly on an extender board.

Caution

To avoid damaging the cables connected to A33 J5 and J6, disconnect and position the cables away from the A52 Fractional-N assembly before removing or inserting the A52 Fractional-N assembly.

2. Reconnect the following using extender cables:

   A52 J1 to A51 J3
   A52 J2 to A33 J4
   A62 J1 to A33 J3
   A62 J2 to A31 J8

3. Disconnect the cable from A21 J2, and connect the spectrum analyzer to A21 J2 using a BNC-to-SMB cable. Connect the spectrum analyzer's 10 MHz reference output to EXT REF IN (on rear panel) using a BNC cable.

4. Set the spectrum analyzer as follows:

Center Frequency	400 MHz
Frequency Span	500 kHz
Reference Level	0 dBm

5. Set the power switch to ON (I), then press the following keys:

   [**Special Fctn**]
   [F9]
   – 99
   [F9]
   [SERVICE FUNCTIONS]
   [ADJUSTMTS]
   [LOCAL OSC]
   [SPURS]
   [100 kHz]

6. Adjust A52 R416 (see figure 5- 3) for a minimum spur level at approximately 400.2 MHz (figure 5-4 shows the spurs out of adjustment).

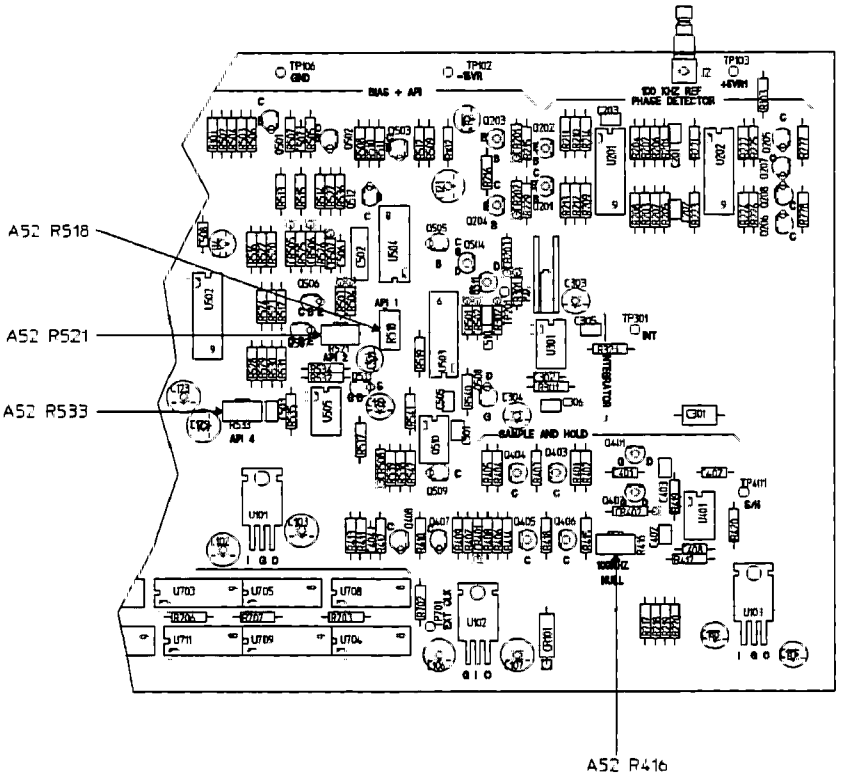


Figure 5-3. A52 Fractional-N Component Locator

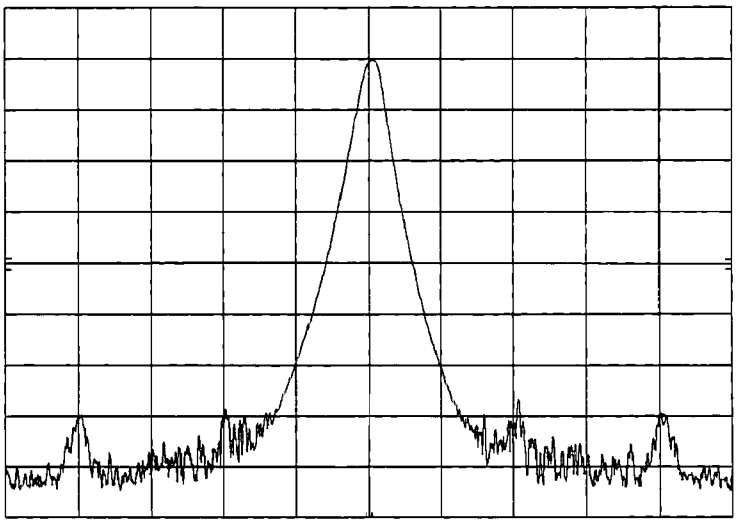


Figure 5-4. Spurs Out of Adjustment

7. Set the spectrum analyzer as follows:

Center Frequency	400.03 MHz
Frequency Span	20 kHz

8. Press the [API 1] softkey.
9. Adjust API 1 (A52 R518) for a minimum spur level at 400.033 MHz.
10. Change the spectrum analyzer's center frequency to 400.003 MHz.
11. Press the [API 2] softkey.
12. Adjust API 2 (A52 R521) for a minimum spur level at 400.006 MHz.
13. Change the spectrum analyzer's center frequency to 400.0001 MHz.
14. Press the [API 4] softkey.
15. Adjust API 4 (A52 R533) for a minimum spur level at 400.00303 MHz.
16. Set the power switch to STANDBY (⏻). Place the Fractional-N assembly into the card nest, and replace the screws.
17. Reconnect the following using original cables:

    A52 J1 to A51 J3
    A52 J2 to A33 J4
    A62 J1 to A33 J3
    A62 J2 to A31 J8
    A21 J2 to A42 J2
    A33 J5 to TRIG OUT (white cable)
    A33 J6 to EXT TRIG (black cable)

7. Sum VCO Filter

This procedure adjusts the low pass filter on the A21 Sum VCO assembly. This filter improves spectral purity of the VCO.

Equipment Required:
- Spectrum Analyzer
- Extender Board
- Extender Cable
- BNC(m)-to-SMB(f) Cable

1. Set the power switch to STANDBY (⏻). Remove the screw at each end of the A21 Sum VCO assembly, and place the assembly on an extender board.
2. Reconnect A21 J1 to A51 J2 using an extender cable. (A11 J2 to A31 J1 may be left unconnected.)
3. Connect the spectrum analyzer to A21 J2 using a BNC-to-SMB cable.
4. Set the power switch to ON (I), then press the following keys:
   - [**Special Fctn**]
   - [F9]
   - **– 99**
   - [F9]
   - [SERVICE FUNCTIONS]
   - [ADJUSTMTS]
   - [LOCAL OSC]
   - [SUM VCO LOW PASS]
5. Set the spectrum analyzer as follows:

Center Frequency	380 MHz
Frequency Span	200 MHz
Reference Level	– 5 dBm
dB per Division	1 dB
Maximum Hold	On

6. Through the holes in the shield can, alternately adjust A21 L106 and L107 (see figure 5-5) for a flatness (maximum amplitude minus minimum amplitude) of less than 3 dB(p-p). During this adjustment, periodically clear the spectrum analyzer's maximum hold function.

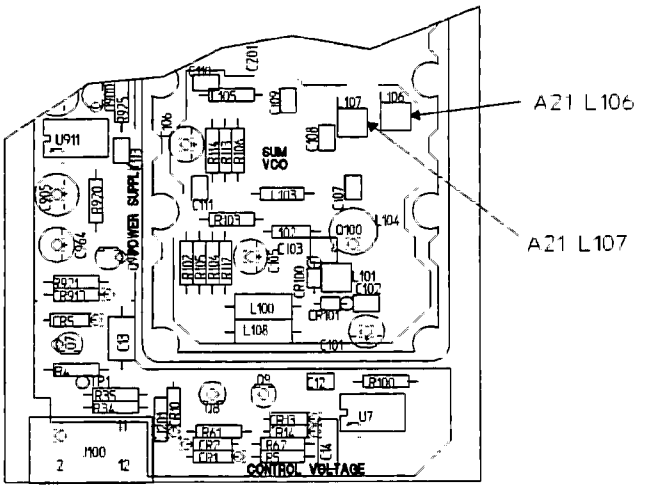


Figure 5-5. A21 Sum VCO Component Locator

7. Set the power switch to STANDBY (⏻). Place the Sum VCO assembly into the card nest, and replace the screws.

8. Reconnect the following using original cables:

   A21 J1 to A51 J2
   A21 J2 to A42 J2
   A21 J3 to A12 J1
   A21 J4 to A22 J1
   A11 J2 to A31 J1

8. Multiple Loop Control Voltage Clamps

This procedure adjusts the upper and lower out-of-limit voltages on the A23 Step Phase Detector assembly. The multiple loop control voltage is compared to the out-of-limit voltages. If the control voltage exceeds either the upper or lower out-of-limit voltage, the control voltage is clamped to the out-of-limit voltage.

Equipment Required: Frequency Counter
BNC(m)-to-SMB(f) Cable

1. Set the power switch to ON (I).
2. Disconnect the cables from A23 J3 and from A24 J1.
3. Connect the frequency counter to A24 J1 using a BNC-to-SMB cable.
4. Press the following keys:
   [**Special Fctn**]
   [F9]
   – 99
   [F9]
   [SERVICE FUNCTIONS]
   [ADJUSTMTS]
   [LOCAL OSC]
   [MULT LOOP CLAMPS]
   [MULT LOOP CLAMP-LOW]
5. Adjust STEP OOL_L (A23 R461) for 297 ± 0.5 MHz.
6. Reconnect the cable from A23 J3 to A31 J4.
7. Disconnect the cable from A23 J1.
8. Press the [MULT LOOP CLAMP-HI] softkey.
9. Adjust STEP OOL_H (A23 R463) for 470 ± 0.5 MHz.
10. Disconnect the frequency counter from A24 J1.
11. Reconnect A23 J1 to A24 J3 and A24 J1 to A22 J2.
12. Press the [**Preset**] hardkey to exit the adjustment mode.

9. Step VCO Filter

This procedure adjusts the low pass filter on the A24 Step VCO assembly. This filter improves the spectral purity of the VCO.

Equipment Required:

- Spectrum Analyzer
- Extender Board
- Extender Cable
- BNC(m)-to-SMB(f) Cable

1. Connect the spectrum analyzer to A24 J2 using a BNC-to-SMB cable.

2. Set the power switch to ON (I), then press the following keys:

   [**Special Fctn**]
   [F9]
   – 99
   [F9]
   [SERVICE FUNCTIONS]
   [ADJUSTMTS]
   [LOCAL OSC]
   [STEP VCO LOW PASS]

3. Set the spectrum analyzer as follows:

Center Frequency	380 MHz
Frequency Span	200 MHz
Reference Level	– 20 dBm
dB per Division	1 dB
Maximum Hold	On

4. If the flatness (maximum amplitude minus minimum amplitude) of the displayed signal is less than 3 dB(p-p), the step VCO filter is within tolerance and should not be adjusted. Disconnect the spectrum analyzer from A24 J2.

5. If the flatness (maximum amplitude minus minimum amplitude) of the displayed signal is larger than 3 dB(p-p), do the following:

   a. Set the power switch to STANDBY (⏻). Remove the screw at each end of the A24 Step VCO assembly, and place the assembly on an extender board.

   b. Reconnect A24 J3 to A23 J1 using an extender cable.

   c. Reconnect the spectrum analyzer to A24 J2 using a BNC-to-SMB cable.

d. Set the power switch to ON (I), then press the following keys:

[**Special Fctn**]
[AUTO CAL ON **OFF**]
[F9]
– 99
[F9]
[SERVICE FUNCTIONS]
[ADJUSTMTS]
[LOCAL OSC]
[STEP VCO LOW PASS]

e. Through the holes in the shield can, alternately adjust A24 L506 and L507 (see figure 5-6) for a flatness (maximum amplitude minus minimum amplitude) of less than 3 dB(p-p). During this adjustment, periodically clear the spectrum analyzer's maximum hold function.

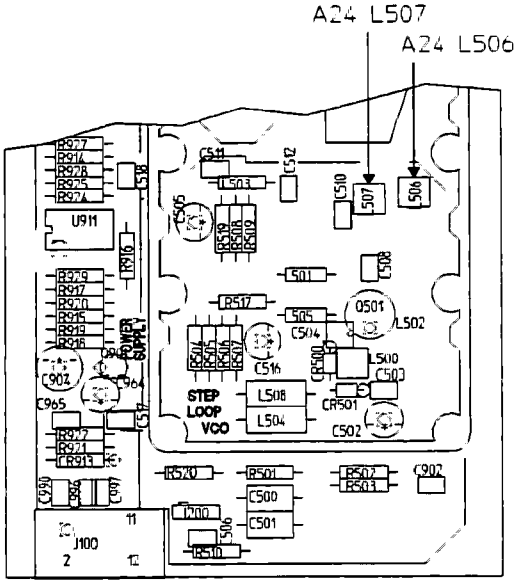


Figure 5-6. A24 Step VCO Component Locator

f. Set the power switch to STANDBY (⏻). Place the Step VCO assembly into the card nest, and replace the screws.

g. Reconnect the following using original cables:

A24 J1 to A22 J2
A24 J2 (no connection)
A24 J3 to A23 J1

10. Pretune Offset and Slope

This procedure adjusts the pretune offset and slope on the A23 Step Phase Detector assembly. Pretune offset is added to the control voltage, then amplified by pretune slope. The resulting voltage coarsely adjusts the sum VCO's frequency to ensure that the sum loop can phase lock.

Equipment Required: Frequency Counter
BNC(m)-to-SMB(f) Cable

1. Set the power switch to ON (I).
2. Disconnect the cables from A22 J3 and from A21 J3.
3. Connect the frequency counter to A21 J3 using a BNC-to-SMB cable.
4. Press the following keys:
   [**Special Fctn**]
   [F9]
   – 99
   [F9]
   [SERVICE FUNCTIONS]
   [ADJUSTMTS]
   [LOCAL OSC]
5. Press the [PRETUNE OFFSET] softkey.
6. Adjust PRETUNE OFFSET (A23 R452) for 450 ± 0.5 MHz.
7. Press the [PRETUNE SLOPE] softkey.
8. Adjust PRETUNE SLOPE (A23 R457) for 306 ± 0.5 MHz.

Note

If PRETUNE SLOPE cannot be adjusted for 306 ± 0.5 MHz, adjust either A21 L101 (see figure 5-5) or A24 L500 (see figure 5-6). Adjusting A21 L101 clockwise or A24 L500 counterclockwise reduces the frequency.

9. Repeat steps 5 through 8 until both PRETUNE OFFSET and PRETUNE SLOPE are within tolerance without adjustment.

10. Press the following keys:

    [**Preset**]
    [**Sweep**]
        [SWEEP AUTO **MAN**]
        [MANUAL FREQ]
        30
        [MHz]

11. The counter readout should be 336 ± 1 MHz. If the counter readout is not within tolerance, do the following:

    a. Press the following keys:

    [**Special Fctn**]
        [SERVICE FUNCTIONS]
        [ADJUSTMTS]
        [LOCAL OSC]
        [PRETUNE SLOPE]

    b. Adjust PRETUNE SLOPE (A23 R457) for 305.6 ± 0.1 MHz.

    c. Repeat steps 5 through 11 until all are within tolerance without adjustment.

    d. Press the [**Preset**] hardkey to exit the adjustment mode.

12. Disconnect the frequency counter from A21 J3.

13. Reconnect A21 J3 to A12 J1 and A22 J3 to A51 J1.

11. ADC Gain, Offset, and Reference

This procedure adjusts the second-pass gain, the first-pass offset, and the reference voltage for the ADC on the A62 ADC/Digital Filter assembly.

Equipment Required:

- Oscilloscope
- 1:1 Oscilloscope Probe
- Synthesizer
- Extender Board
- Extender Cables
- BNC(m)-to-SMB(f) Cable
- Capacitive Load
- BNC Cable

Note

Although a digital oscilloscope is listed in the recommended equipment list, this adjustment may be easier using an analog oscilloscope.

1. Set the power switch to STANDBY (⏻). Remove the screw at each end of the A62 ADC/Digital Filter assembly, and place the assembly on an extender board.
2. Reconnect A62 J1 to A33 J3 and A62 J2 to A31 J8 using extender cables. Reconnect the fast bus cable to A62 J5 using the fast bus extender cable.
3. Connect the oscilloscope to A62 TP400 (see figure 5-7) using a capacitive load and a 1:1 oscilloscope probe. Connect the probe ground clip to TP 505 (AGND).

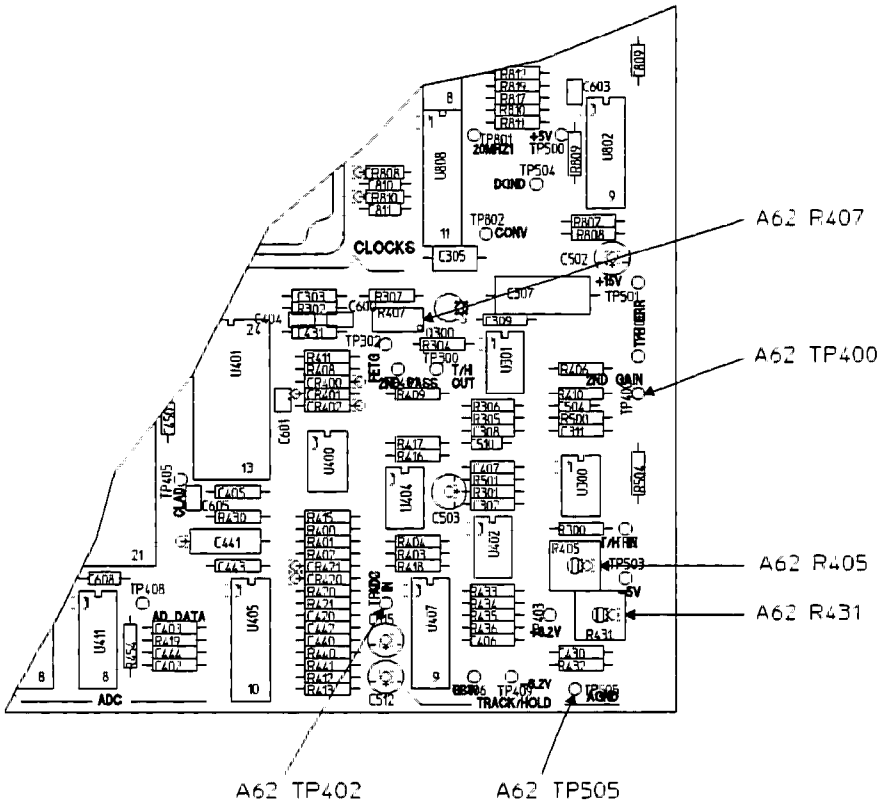


Figure 5-7. A62 ADC/Digital Filter Component Locator

4. Connect the synthesizer to A62 J3 using a BNC-to-SMB cable.

Note A 50Ω termination is required for synthesizers with 50Ω output impedance.

---

5. Connect the synthesizer's synchronous output to either the oscilloscope's channel 2 input or external trigger input using a BNC cable.

6. Set the synthesizer as follows:

Function	Sine Wave
Frequency	1 kHz
Amplitude	10 mVrms

7. Set the oscilloscope as follows:

Channel 1	Volts/Div	2 mV/div
	Offset	0V
	Coupling	1 MΩ ac
Time Base	Time/Div	500 μs/div
	Sweep	Triggered
Trigger	Level	500 mV
	Slope	Positive
	Mode	Edge
	Source	Channel 2 or Ext Trigger
Display	Mode	Real Time
	Resolution	8 bits
	(Analog Scope	BW Limit On)
	Screen	Single

8. Set the power switch to ON (I), then press the following keys:

   [**Special Fctn**]
   [F9]
   – 99
   [F9]
   [SERVICE FUNCTIONS]
   [ADJUSTMTS]
   [ADC]
   [ADC 2ND PASS GAIN]

9. Adjust A62 R407 for a flat trace on the oscilloscope display.

10. Remove the capacitive load from the oscilloscope, and connect the oscilloscope probe to A62 TP402.

11. Change the set up for the oscilloscope as follows:

Channel 1	Volts/Div	100 mV/div
	Coupling	1 MΩ dc
Display	Mode	Repetitive
	Averaging	Off
	Persistence	2.00s

12. Increase the synthesizer's amplitude to 400 mVrms.

13. Press the [ADC OFFST & REFERNC] softkey.

14. The oscilloscope display should look like figure 5-8. The following describes the signals shown on the oscilloscope display:
    - A straight, horizontal line in the upper half of the display.
    - A sine wave in the lower half of the display.
    - A "noisy" flat trace at the center of the sine wave.

    If the oscilloscope display does not look like figure 5-8, do the following:

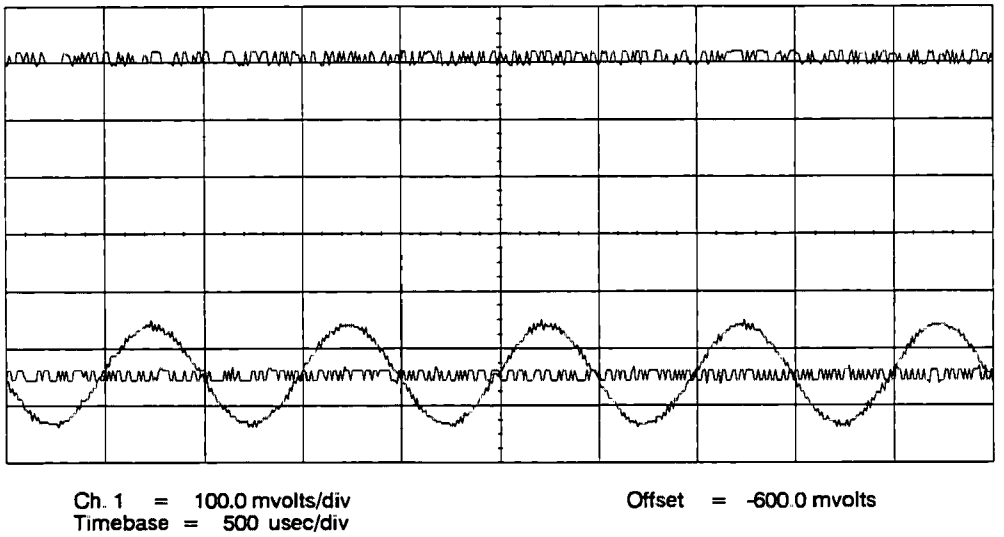


Figure 5-8. R431 and R405 Correctly Adjusted

a. If the oscilloscope display looks like figure 5-9, adjust A62 R431 for a flat "noisy" trace as shown in figure 5-10.

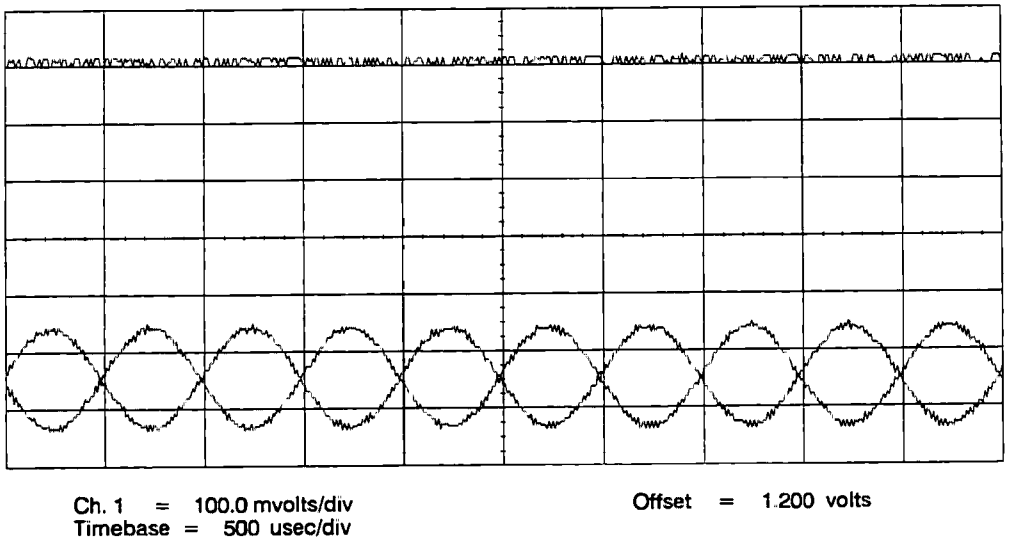


Figure 5-9. R431 and R405 Incorrectly Adjusted

b. If the oscilloscope display looks like figure 5-10, adjust A62 R405 to position the flat trace at the center of the sine wave trace as shown in figure 5-8.

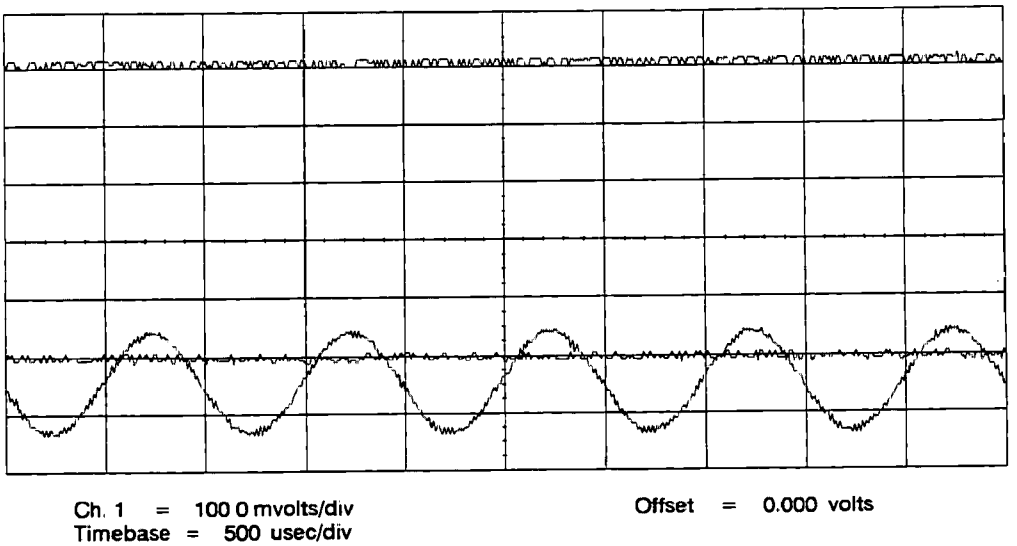


Figure 5-10. R405 Incorrectly Adjusted

15. Set the power switch to STANDBY (⏻). Place the ADC/Digital Filter assembly into the card nest, and replace the screws.

16. Reconnect the following using original cables:

    A62 J1 to A33 J3
    A62 J2 to A31 J8
    A62 J3 to A61 J3

12. Second IF Bandpass Filter

This procedure adjusts the second IF bandpass filter on the A61 IF assembly. This 10.1875 MHz bandpass filter attenuates signals outside the passband.

Equipment Required:

- Spectrum Analyzer
- Extender Board
- Extender Cables
- BNC Cable
- SMB(m)-to-SMB(m) Adapter
- N(m)-to-BNC(m) Adapter

1. Set the power switch to STANDBY (⏻). Remove the screw at each end of the A61 IF assembly, and place the assembly on an extender board.
2. Reconnect the following using extender cables (connecting A61 J1 to A13 J3 requires using two extender cables and an adapter):
   - A61 J1 to A13 J3
   - A61 J2 to A31 J3
   - A61 J3 to A62 J3
3. Set the power switch to ON (I), then press the following keys:
   - [**Special Fctn**]
   - [F9]
   - **– 99**
   - [F9]
   - [SERVICE FUNCTIONS]
   - [ADJUSTMTS]
   - [RECEIVER IF]
   - [2nd IF1]

Note

During this adjustment, the reference level automatically changes when the signal reaches the top or bottom of the displayed range. The analyzer beeps to indicate that the reference level changed.

4. Adjust A61 L3, L4, L5, L6, L8, L9, and L10 from the circuit side of the board (see figure 5-11 for component location) for a maximum **Man** readout (approximately – 25 dBm). Continue adjusting until no further improvement can be made.

Note

If the signal is below the displayed range, continue to adjust. The signal is not seen when the filter is too far out of adjustment.

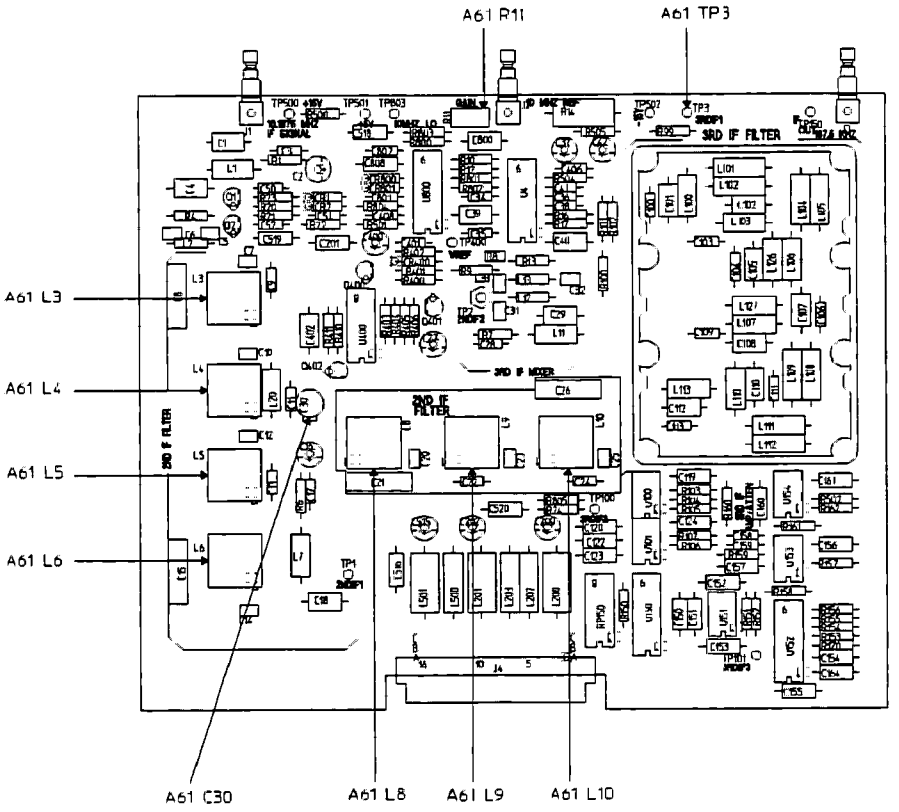


Figure 5-11. A61 IF Component Locator

5. Press the [2nd IF2] softkey.
6. Connect REF OUT (10 MHz) on the rear panel to INPUT on the front panel using a BNC cable and N-to-BNC adapter.
7. Adjust A61 C30 for a minimum **Man** readout.
8. Press the [2nd IF3] softkey.
9. Alternately adjust A61 L4 and L5 for a maximum **Man** readout.
10. Press the [2nd IF4] softkey.

11. Alternately adjust A61 L4 and L5 to center the peak and equalize the level of the sides (see figure 5-12).

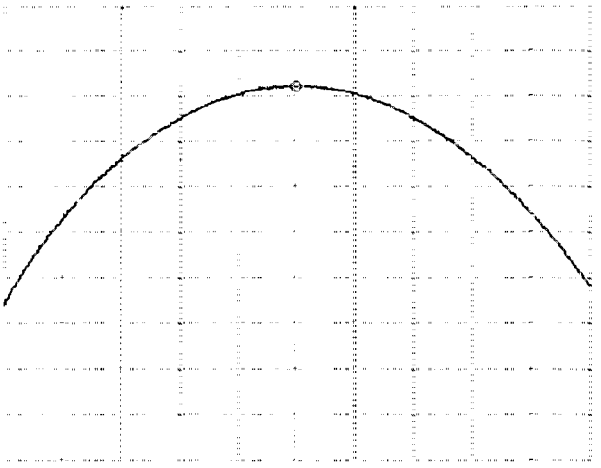


Figure 5-12. Second IF Adjustment

12. Set the spectrum analyzer as follows:

Input	1 MΩ
Center Frequency	187.5 kHz
Span	10 kHz
Scale	0 dBV

13. Connect the spectrum analyzer to A61 TP3 using a 1:1 oscilloscope probe.

14. Press the [2nd IF5] softkey.

15. Adjust A61 R11 for -32.0 ± 0.1 dBV.

16. Set the power switch to STANDBY (⏻). Place the IF assembly into the card nest, and replace the screws.

17. Reconnect the following using original cables:

    A61 J1 to A13 J3
    A61 J2 to A31 J3
    A61 J3 to A62 J3

13. Source Bandpass Filter

This procedure adjusts the four cavity helical resonator filter on the A42 Source Conversion assembly. This 310.1875 MHz bandpass filter attenuates signals outside of its narrow passband.

Equipment Required: Extender Board
Extender Cables

1. Set the power switch to STANDBY (⏻). Remove the screw at each end of the A42 Source Conversion assembly, and remove the assembly from the card nest.

Caution  To avoid damaging the cables connected to A33 J5 and J6, disconnect and position the cables away from the A42 Source Conversion assembly before removing or inserting the A42 Source Conversion assembly.

2. Remove the shield can covering A42 W202 and W203 (see figure 5-13). Move A42 W201, W202, and W203 to their test positions.

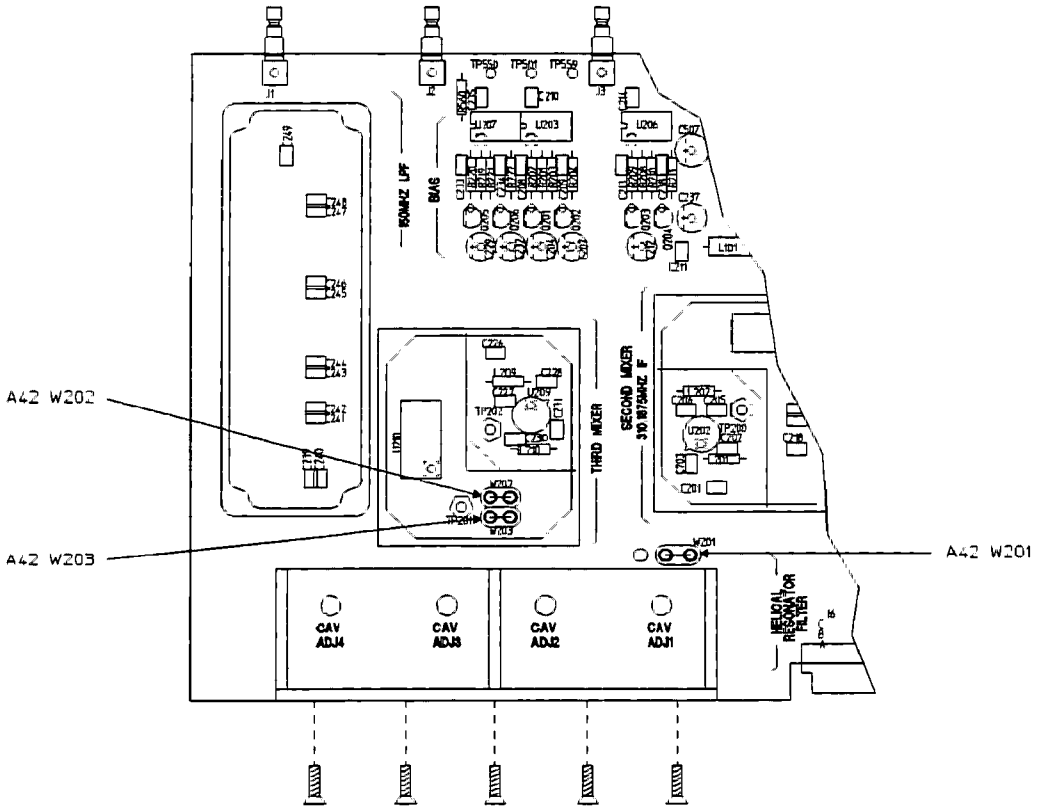


Figure 5-13. A42 Source Conversion Component Locator

3. Remove the plate covering the helix cavity. Then using a ball driver hex tool, turn all four tuning screws (CAV ADJ 1, 2, 3, and 4) clockwise until the screws just contact the helix structure inside the cavity (see caution below). Replace the plate covering the helix cavity.

Caution The helix structure will be damaged if the tuning screws are turned in too far. Be careful to only turn the screws until they just touch the helix structure inside the cavity.

---

4. Place the A42 Source Conversion assembly on an extender board.

5. Reconnect the following using extender cables:

   A42 J1 to A41 J3
   A42 J2 to A21 J2
   A42 J3 to A32 J3
   A42 J4 to A31 J5
   A42 J6 to A33 J2
   A52 J2 to A33 J4
   A62 J1 to A33 J3

6. Set the power switch to ON (I), then press the following keys:

   [**Special Fctn**]
   [F9]
   – 99
   [F9]
   [SERVICE FUNCTIONS]
   [ADJUSTMTS]
   [SOURCE]
   [HELICAL RESONATOR]

Note

During this adjustment, the reference level automatically changes when the signal reaches the top or bottom of the displayed range. The analyzer beeps to indicate that the reference level changed.

---

7. Adjust CAV ADJ 1 counterclockwise for a maximum signal level.
8. Adjust CAV ADJ 2 counterclockwise for a minimum signal level. (The minimum level should be about 15 dB smaller than the maximum level achieved in the previous step.)
9. Adjust CAV ADJ 3 counterclockwise for a maximum signal level.
10. Adjust CAV ADJ 4 counterclockwise for a minimum signal level.
11. Set the power switch to STANDBY (⏻). Return W201, W202, and W203 to their original positions. Replace the shield can.
12. Place the Source Conversion assembly into the card nest, and replace the screws.
13. Reconnect the following using original cables:

    A42 J1 to A41 J3
    A42 J2 to A21 J2
    A42 J3 to A32 J3
    A42 J4 to A31 J5
    A42 J6 to A33 J2
    A52 J2 to A33 J4
    A62 J1 to A33 J3
    A33 J5 to TRIG OUT (white cable)
    A33 J6 to EXT TRIG (black cable)

14. First IF Bandpass Filter

This procedure adjusts the four cavity helical resonator filter on the A12 First Conversion assembly. This 310.1875 MHz bandpass filter attenuates signals outside of its narrow passband.

Equipment Required: Extender Board
Extender Cables

1. Set the power switch to STANDBY (⏻). Remove the screw at each end of the A12 First Conversion assembly, and remove the assembly from the card nest.
2. Move A12 W801, W802, and W803 to their test positions (see figure 5-14).

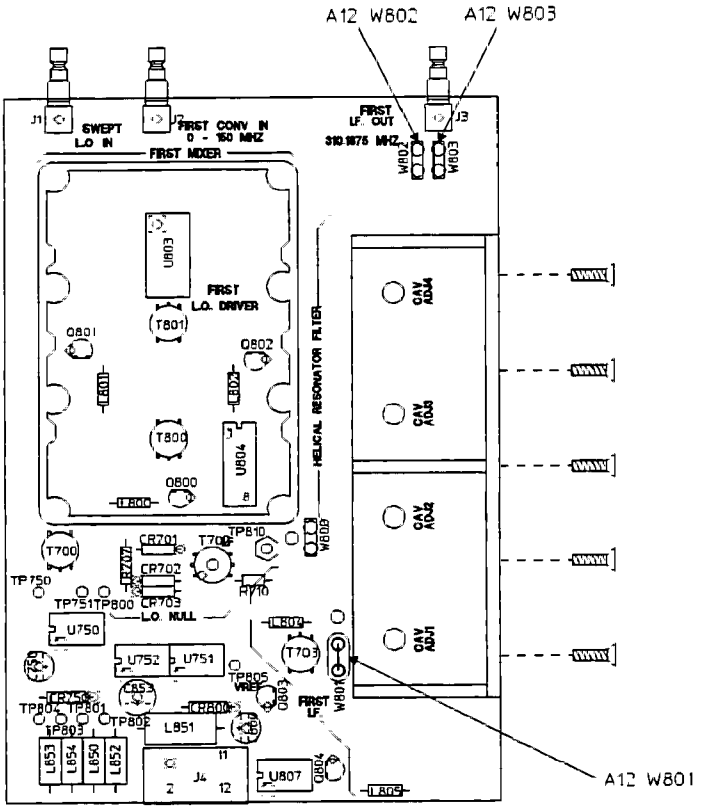


Figure 5-14. A12 First Conversion Component Locator

3. Remove the plate covering the helix cavity. Then using a ball driver hex tool, turn all four tuning screws (CAV ADJ 1, 2, 3, and 4) clockwise until the screws just contact the helix structure inside the cavity (see caution below). Replace the plate covering the helix cavity.

Caution 

The helix structure will be damaged if the tuning screws are turned in too far. Be careful to only turn the screws until they just touch the helix structure inside the cavity.

---

4. Place the assembly on an extender board.
5. Reconnect the following using extender cables:

   A12 J1 to A21 J3
   A12 J2 to A11 J3
   A12 J3 to A13 J2

6. Set the power switch to ON (|), then press the following keys:

   [Special Fctn]
   [F9]
   – 99
   [F9]
   [SERVICE FUNCTIONS]
   [ADJUSTMTS]
   [RECEIVER IF]
   [HELICAL RESONATOR]

Note 

During this adjustment, the reference level automatically changes when the signal reaches the top or bottom of the displayed range. The analyzer beeps to indicate that the reference level changed.

---

7. Adjust CAV ADJ 1 counterclockwise for a maximum signal level.
8. Adjust CAV ADJ 2 counterclockwise for a minimum signal level. (The minimum level should be about 15 dB smaller than the maximum level achieved in the previous step.)
9. Adjust CAV ADJ 3 counterclockwise for a maximum signal level.
10. Adjust CAV ADJ 4 counterclockwise for a minimum signal level.

11. Set the power switch to STANDBY (⏻). Return W801, W802, and W803 to their original positions.
12. Place the First Conversion assembly into the card nest, and replace the screws.
13. Reconnect the following using original cables:

    A12 J1 to A21 J3
    A12 J2 to A11 J3
    A12 J3 to A13 J2

15. Autorange Thresholds and 1 Meg Ohm Flatness

This procedure adjusts the range up and range down threshold for autorange on the A11 Input assembly. This procedure also adjusts the flatness of the frequency response of the 1 MΩ buffer.

Equipment Required:

Extender Board
Extender Cables
Small Adjustment Tool
50Ω Feedthrough Termination
BNC(m)-to-SMB(f) Cable
SMB(m)-to-SMB(m) Adapter
N(m)-to-BNC(f) Adapter

1. Set the power switch to STANDBY (⏻). Remove the screw at each end of the A11 Input assembly, and remove the assembly from the card nest.

2. Connect the 50Ω feedthrough termination to the SOURCE connector using an N-to-BNC adapter. Using the BNC-to-SMB cable and SMB-to-SMB adapter, connect the feedthrough termination to A11 J4 (SMB connector at bottom of A11 Input assembly). Place the assembly on an extender board.

3. Reconnect the following using extender cables:

   A11 J1 to A41 J1
   A11 J2 to A31 J1
   A11 J3 to A12 J2

4. Set the power switch to ON (I), then press the following keys:

   [**Special Fctn**]
   [F9]
   – 99
   [F9]
   [SERVICE FUNCTIONS]
   [ADJUSTMTS]
   [RECEIVER INPUT]
   [RANGE UP THRESHOLD]

5. Adjust A11 R624 (see figure 5-15) so that A11 CR606 just lights up, indicating that the upper threshold trip point was reached. (Turn A11 R624 counterclockwise to light A11 CR606.)

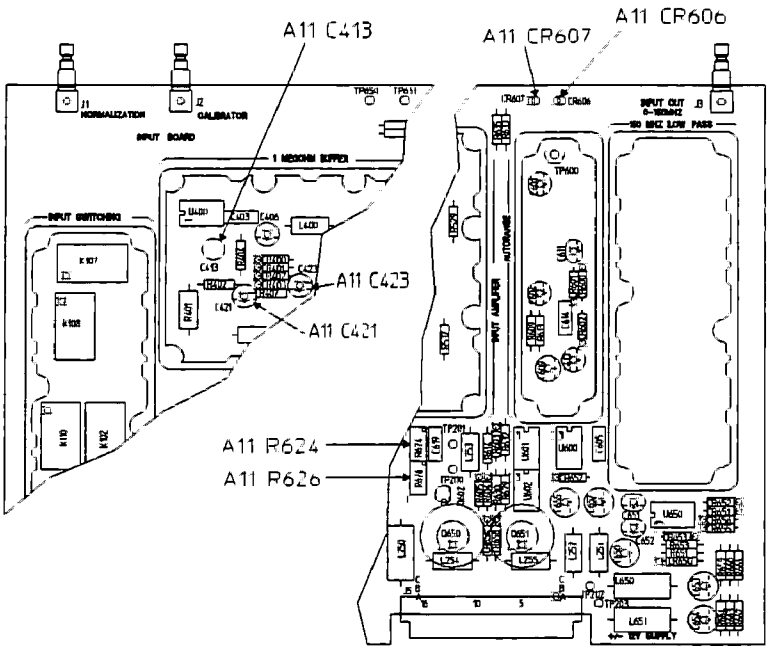


Figure 5-15. A11 Input Component Locator

6. Press the [RANGE DN THRESHOLD] softkey.
7. Adjust A11 R626 so that A11 CR607 just lights up, indicating that the lower threshold trip point was reached. (Turn A11 R626 clockwise to light A11 CR607.)
8. Press the [1 MOHM FLATNESS] softkey.
9. Using the small adjustment tool in the service kit, adjust A11 C423 through a hole in the shield can so the displayed waveforms are as close as possible without the ends crossing, especially at the upper frequence limit (see figure 5-16).
10. Press the [NEXT STEP] softkey.
11. Using the small adjustment tool in the service kit, adjust A11 C421 through a hole in the shield can so the displayed waveforms are as close as possible without the ends crossing, especially at the upper frequence limit (see figure 5-16).
12. Press the [NEXT STEP] softkey.
13. Using the small adjustment tool in the service kit, adjust A11 C413 through a hole in the shield can so the displayed waveforms are as close as possible without the ends crossing, especially at the upper frequence limit (see figure 5-16).

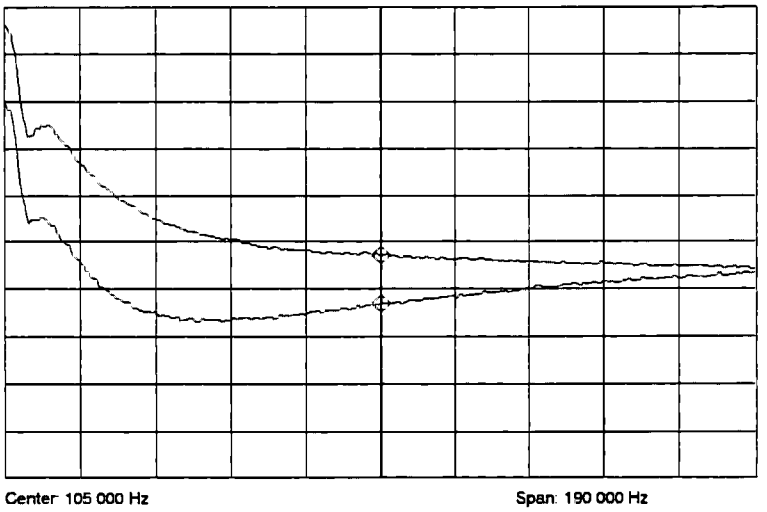


Figure 5-16. 1 Meg Ohm Flatness Adjustment

14. Set the power switch to STANDBY (⏻). Place the Input assembly into the card nest, and replace the screws.

15. Reconnect the following using original cables:

    A11 J1 to A41 J1
    A11 J2 to A31 J1
    A11 J3 to A12 J2

16. Oven Frequency

This procedure adjusts the frequency of option 1D5, A91 Fan Power/Oven assembly. The A91 Fan Power/Oven assembly provides the HP 3589A Spectrum/Network Analyzer with an absolute frequency reference.

Equipment Required:

- Oscilloscope
- Frequency Standard
- BNC Cable

Note

The HP 3589A Spectrum/Network Analyzer must be on for at least 48 hours before this adjustment is made.

1. Remove the screw on the oven-adjustment cover. Lift the screw side of the oven-adjustment cover and tilt back to the open position.
2. Connect the frequency standard's output to the oscilloscope's external trigger (make sure the frequency standard is properly terminated).
3. Connect OVEN REF OUT (located on the rear panel) to the oscilloscope's channel 1 input.
4. Adjust FINE FREQUENCY ADJUST (A91 R12) to the center of its adjustment range.
5. Set the oscilloscope as follows:

Channel 1	Volts/Div	500 mV/div
	Offset	0V
	Coupling	1 MΩ ac
Timebase	Time/Div	50 ns/div
	Sweep	Triggered
Trigger	Level	0V
	Slope	Positive
	Mode	Edge
	Source	External Trigger
Display	Mode	Real Time
	Screen	Single

6. Remove the oven screw and adjust COARSE FREQUENCY ADJUST (A91 U3) for a stable (not moving) display on the oscilloscope.
7. Change the oscilloscope timebase to 10 ns per division.
8. Adjust FINE FREQUENCY ADJUST for a stable (not moving) display on the oscilloscope.
9. Return the oven screw, oven-adjustment cover and screw, and rear panel jumper (OVEN REF OUT to EXT REF IN) to their original positions.

17. Calibrator Flatness and Level

This procedure adjusts the level and flatness of the calibration signal on the A31 Reference/Calibrator assembly.

Equipment Required:
- Milliwatt Power Meter (recommended)
  or Power Meter (alternate)
- BNC Cable
- N(f)-to-BNC(f) Adapters

Note This adjustment can be done with either a milliwatt power meter or a standard power meter. For best accuracy, use the milliwatt power meter.

1. Connect the power meter to the SOURCE connector (located on front panel).

Note If you are using a standard power meter, set its calibration factor for 300 kHz to improve the accuracy of this adjustment.

2. Press the following keys:

   [Preset]
   [Special Fctn]
   [F9]
   – 99
   [F9]
   [SERVICE FUNCTIONS]
   [ADJUSTMTS]
   [CALIBRATR]
   [CAL LEVEL]

3. After the message appears on the screen, press the following keys:

   [SRCE DAC ATTEN]
   16
   [dB]

4. Using the analyzer's numeric key entry, adjust SRCE DAC ATTEN for a 0 dBm ± 0.01 dB readout on the power meter (for example, press **16.15** [dB]).

5. Press the [NEXT STEP] softkey.
6. Disconnect the power meter. Using the N-to-BNC adapters and BNC cable, connect the SOURCE connector to the INPUT connector.
7. After the **Man** readout is stable, press the [NEXT STEP] softkey.
8. While monitoring the **Man** readout, adjust CAL LEVEL (A31 R322) for the value indicated in the message on the display.
9. Disconnect the cable from the SOURCE connector. Reconnect the power meter to the SOURCE connector.

Note

If you are using a standard power meter, set its calibration factor for 120 MHz to improve the accuracy of this adjustment.

---

10. Press the following keys:

    [**Preset**]
    [**Special Fctn**]
    [SERVICE FUNCTIONS]
    [ADJUSTMTS]
    [CALIBRATR]
    [CAL FLATNESS]

11. After the message appears on the screen, press the following keys:

    [SRCE DAC ATTEN]
    16
    [dB]

12. Using the analyzer's numeric key entry, adjust SRCE DAC ATTEN for a 0 dBm ± 0.01 dB readout on the power meter (for example, press **16.15** [dB]).
13. Press the [NEXT STEP] softkey.
14. Disconnect the power meter. Reconnect the INPUT connector to the SOURCE connector.
15. After the **Man** readout is stable, press the [NEXT STEP] softkey.
16. While monitoring the **Man** readout, adjust CAL FLAT (A31 C330) for the value indicated in the message on the display.
17. Disconnect the cable connected between the SOURCE connector and INPUT connector.
18. Press the [**Preset**] hardkey to exit the adjustment mode.

18. Display

This procedure adjusts the focus, intensity, and alignment of the Display assembly.

Equipment Required: None

Note If the Display assembly needs to be adjusted, adjust only the components that apply to the problem.

1. Press the following keys to view the test pattern:

   [**Special Fctn**]
   [F9]
   – 99
   [F9]
   [SERVICE FUNCTIONS]
   [SELF TEST]
   [FUNCTIONL TESTS]
   [DISPLAY]
   [TEST PATTERN]

2. Compare the test pattern to figure 5-17. Adjust as indicated in table 5-3 using a non-conductive screw driver.

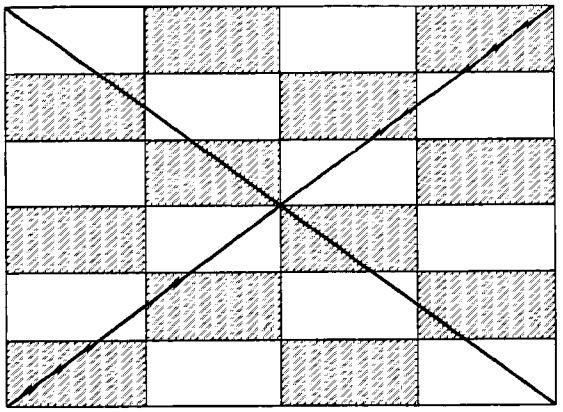


Figure 5-17. Center Portion of Display Test Pattern

Table 5-3. Display Adjustments

Adjustment Name	Adjust for...
Focus	Optimum focus
Brightness	Optimum intensity
Horizontal Width	Test pattern width of 6.89 ± 0.06 inches (175 ± 1.5 mm)
Vertical Hold	Vertically stable display
Vertical Linearity	Uniform height of blocks in test pattern
Vertical Position	Vertically centered test pattern
Vertical Size	Test pattern height of 4.92 ± 0.06 inches (128 ± 1.5 mm)
Horizontal Position	Horizontally centered test pattern
Horizontal Hold	Horizontally stable display

Note

If Vertical Linearity is adjusted, check Vertical Size and Vertical Position, and adjust if necessary.

3. Press the [**Preset**] hardkey to exit the adjustment mode.

6 Replacing Assemblies

6

Replacing Assemblies

How to Use This Chapter

This chapter tells you what to do after you replace an assembly and how to disassemble the analyzer and test set.

What to Do After Replacing an HP 3589A Assembly

After replacing an assembly in the HP 3589A Spectrum/Network Analyzer, do the following:

1. Reinstall all assemblies and cables that were removed during troubleshooting.
2. On the CPU assembly, check that all pins on SW100 are set to zero (see figure 6-1).
3. Do the required adjustments listed in table 6-1 (the adjustments are in chapter 5).
4. Do Test 9. Self Test in chapter 4.
5. Do the required performance tests listed in table 6-1 (the performance tests are in chapter 3).

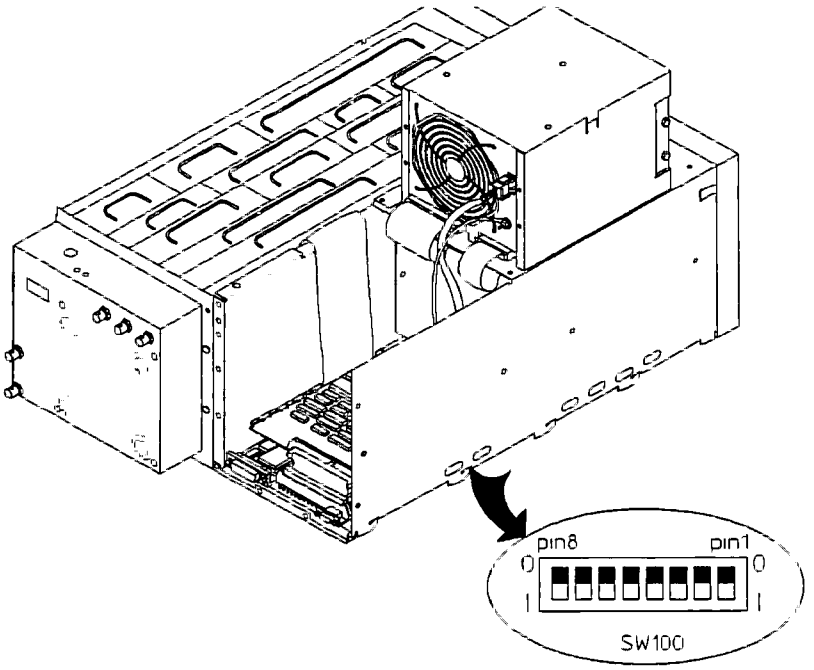


Figure 6-1. Normal Setting for A81 SW100

Table 6-1. Required Adjustments and Performance Tests

Assembly Replaced	Adjustments	Performance Tests
A11 Input	12. Second IF Bandpass Filter 15. Autorange Thresholds and 1 Meg Ohm Flatness	Local Oscillator Feedthrough Residual Responses Noise Level Input Harmonic Distortion Intermodulation Distortion Amplitude Accuracy and Flatness Reference Level Accuracy Dynamic Accuracy Input Return Loss
A12 First Conversion	12. Second IF Bandpass Filter 14. First IF Bandpass Filter	Local Oscillator Feedthrough Residual Responses Noise Level Image Responses Input Harmonic Distortion Intermodulation Distortion Reference Level Accuracy Dynamic Accuracy
A13 Second Conversion	12. Second IF Bandpass Filter	Residual Responses Reference Level Accuracy Dynamic Accuracy
A21 Sum VCO	4. Interpolation VCO 5. Single Loop Control Voltage Clamps 6. 100 kHz and API Spurs 7. Sum VCO Filter 8. Multiple Loop Control Voltage Clamps 9. Step VCO Filter 10. Pretune Offset and Slope	Phase Noise Spurious Responses
A22 Sum Phase Detector	4. Interpolation VCO 5. Single Loop Control Voltage Clamps 6. 100 kHz and API Spurs 7. Sum VCO Filter 8. Multiple Loop Control Voltage Clamps 9. Step VCO Filter 10. Pretune Offset and Slope	Phase Noise Spurious Responses
A23 Step Phase Detector	4. Interpolation VCO 5. Single Loop Control Voltage Clamps 6. 100 kHz and API Spurs 7. Sum VCO Filter 8. Multiple Loop Control Voltage Clamps 9. Step VCO Filter 10. Pretune Offset and Slope	Phase Noise Spurious Responses
A24 Step VCO	4. Interpolation VCO 5. Single Loop Control Voltage Clamps 6. 100 kHz and API Spurs 7. Sum VCO Filter 8. Multiple Loop Control Voltage Clamps 9. Step VCO Filter 10. Pretune Offset and Slope	Phase Noise Spurious Responses
A31 Reference/Calibrator	2. 80 MHz Reference VCXO 3. 300 MHz Reference VCO 17. Calibrator Flatness and Level	Phase Noise Frequency Accuracy Amplitude Accuracy and Flatness

Table 6-1 Required Adjustments and Performance Tests (continued)

Assembly Replaced	Adjustments	Performance Tests
A32 300 MHz	3 300 MHz Reference VCO	Phase Noise
A33 Trigger		Phase Noise
A41 Source Amplifier		Source Response Source Dynamic Accuracy Source Return Loss Source Harmonic Distortion Source Noise
A42 Source Conversion	13. Source Bandpass Filter	Source Response Source Dynamic Accuracy Source Spurious Responses
A51 Interpolation VCO	4. Interpolation VCO 5. Single Loop Control Voltage Clamps 6. 100 kHz and API Spurs 7. Sum VCO Filter 8. Multiple Loop Control Voltage Clamps 9. Step VCO Filter 10. Pretune Offset and Slope	Phase Noise Spurious Responses
A52 Fractional-N	4. Interpolation VCO 5. Single Loop Control Voltage Clamps 6. 100 kHz and API Spurs 7. Sum VCO Filter 8. Multiple Loop Control Voltage Clamps 9. Step VCO Filter 10. Pretune Offset and Slope	Phase Noise Spurious Responses
A61 IF	12. Second IF Bandpass Filter	Residual Responses Noise Level Image Responses Intermodulation Distortion Reference Level Accuracy Dynamic Accuracy
A62 ADC/Digital Filter	11. ADC Gain, Offset, and Reference	Noise Level Reference Level Accuracy Dynamic Accuracy
A81 CPU	see "Replacing the CPU Assembly"	see "Replacing the CPU Assembly"
A87 Memory	see "Replacing the Memory Assembly"	see "Replacing the Memory Assembly"
A88 Expanded Memory	see "Replacing the Memory Assembly"	see "Replacing the Memory Assembly"
A90 Fan Power		
A91 Fan Power/Oven	1. Oven Shutdown 16. Oven Frequency	Phase Noise Frequency Accuracy
A99 Motherboard		
Power Supply		
Disk Drive		
Display		
Front Panel		

Replacing the CPU Assembly

The analyzer's option 1D6 (Time-Gated Spectrum Analysis), option 1C2 (HP Instrument BASIC), and serial number are stored in EEPROM on the CPU assembly. Therefore, when the CPU assembly is replaced, the options must be reinstalled and the analyzer's serial number must be entered in EEPROM.

To reinstall option 1D6, set the analyzer's power switch to STANDBY (⏻). Insert *Service Disk 1* (included in the service kit) into the analyzer's disk drive. Set the power switch to ON (I). The Time-Gated Spectrum Analysis option is automatically reinstalled.

To reinstall option 1C2, set the analyzer's power switch to STANDBY (⏻). Insert *Service Disk 2* (included in the service kit) into the analyzer's disk drive. Set the power switch to ON (I). The HP Instrument BASIC option is automatically reinstalled.

To store the analyzer's serial number, use the HP-IB command, SYST:EEROM:SNUM *'serial number'*. For example, if your computer has HP BASIC and the analyzer's HP-IB address is set to 19, enter the following command:

```
OUTPUT 719;"SYST:EEROM:SNUM 'serial number'"
```

Replacing the Memory Assembly

The HP-IB address may need to be reset after replacing the Memory assembly or battery. Press the following keys to reset the HP-IB address:

[Local/HP-IB]
[SYSTEM CONTROLLR]
[ANALYZER ADDRESS]
11
[ENTER]

HP 3589A Disassembly/Assembly

Use the following illustrations to disassemble and assemble the HP 3589A Spectrum/Network Analyzer.

Warning

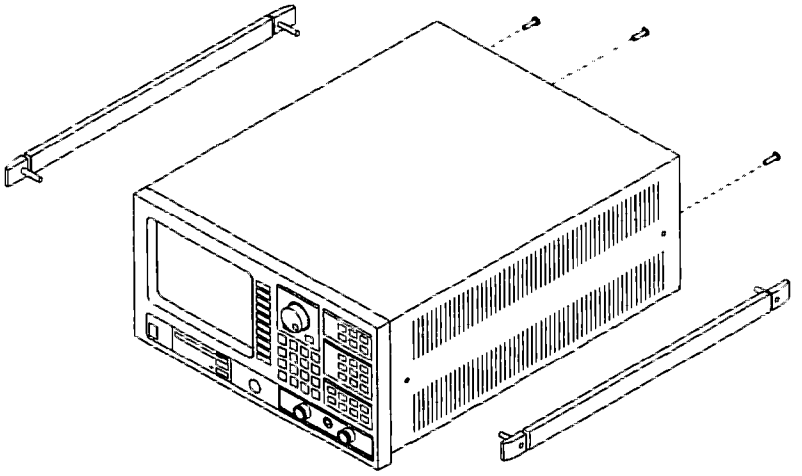
Disconnect the power cord from the rear panel before disassembly or assembly of the HP 3589A Spectrum/Network Analyzer.

Caution

Do not connect or disconnect ribbon cables from circuit assemblies with the line power turned ON (|).

To protect circuits from static discharge, remove or replace HP 3589A Spectrum/Network Analyzer assemblies only at static-protected work stations.

Warning **When replacing the handle assemblies, be careful to position properly and attach firmly. If improperly attached, the handles could come off when lifting the analyzer, causing personal injury.**



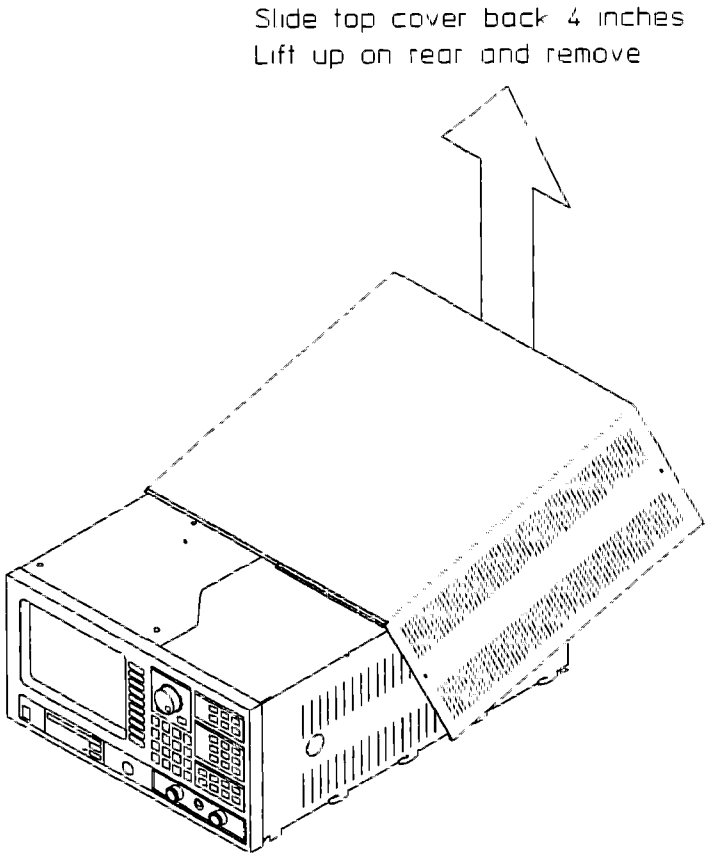


Figure 6-2. Top Cover

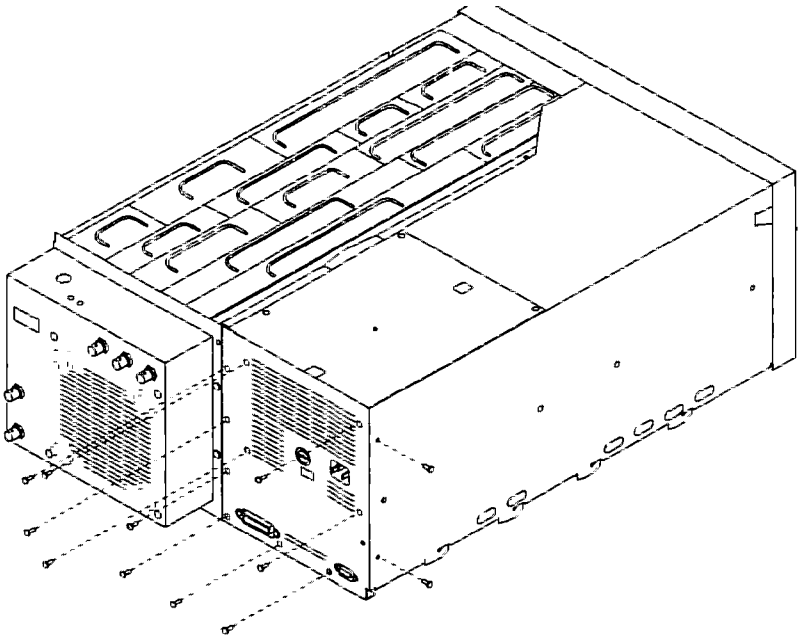


Figure 6-3. Rear Panel

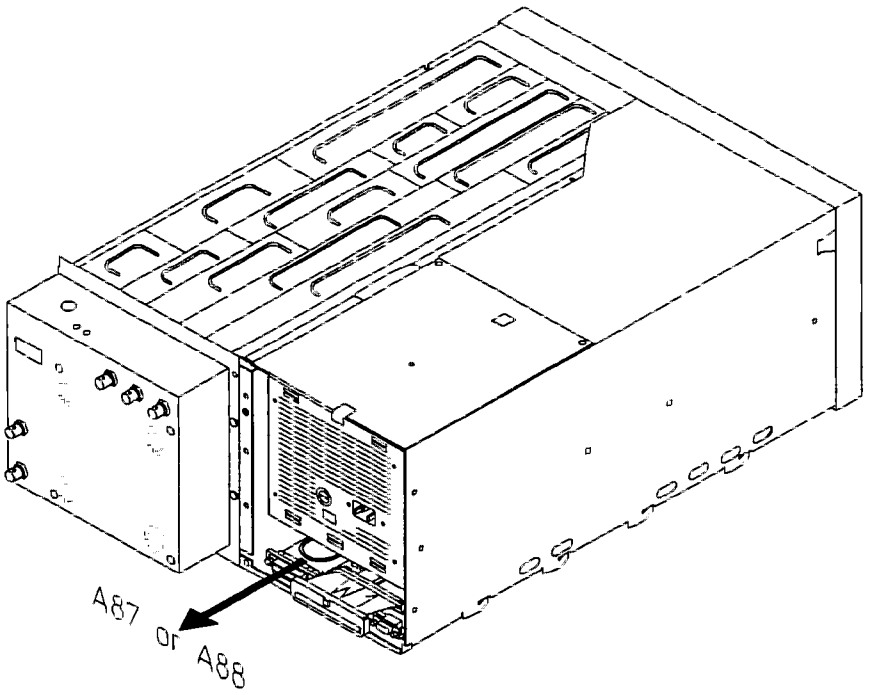


Figure 6-4. Memory

Caution

Do NOT remove the 3 screws that are marked with an X on the illustration. The Power Supply assembly will be damaged if the center screw is removed.

Do NOT remove the earth ground (green/yellow wire) from the Power Supply assembly or the analyzer's chassis.

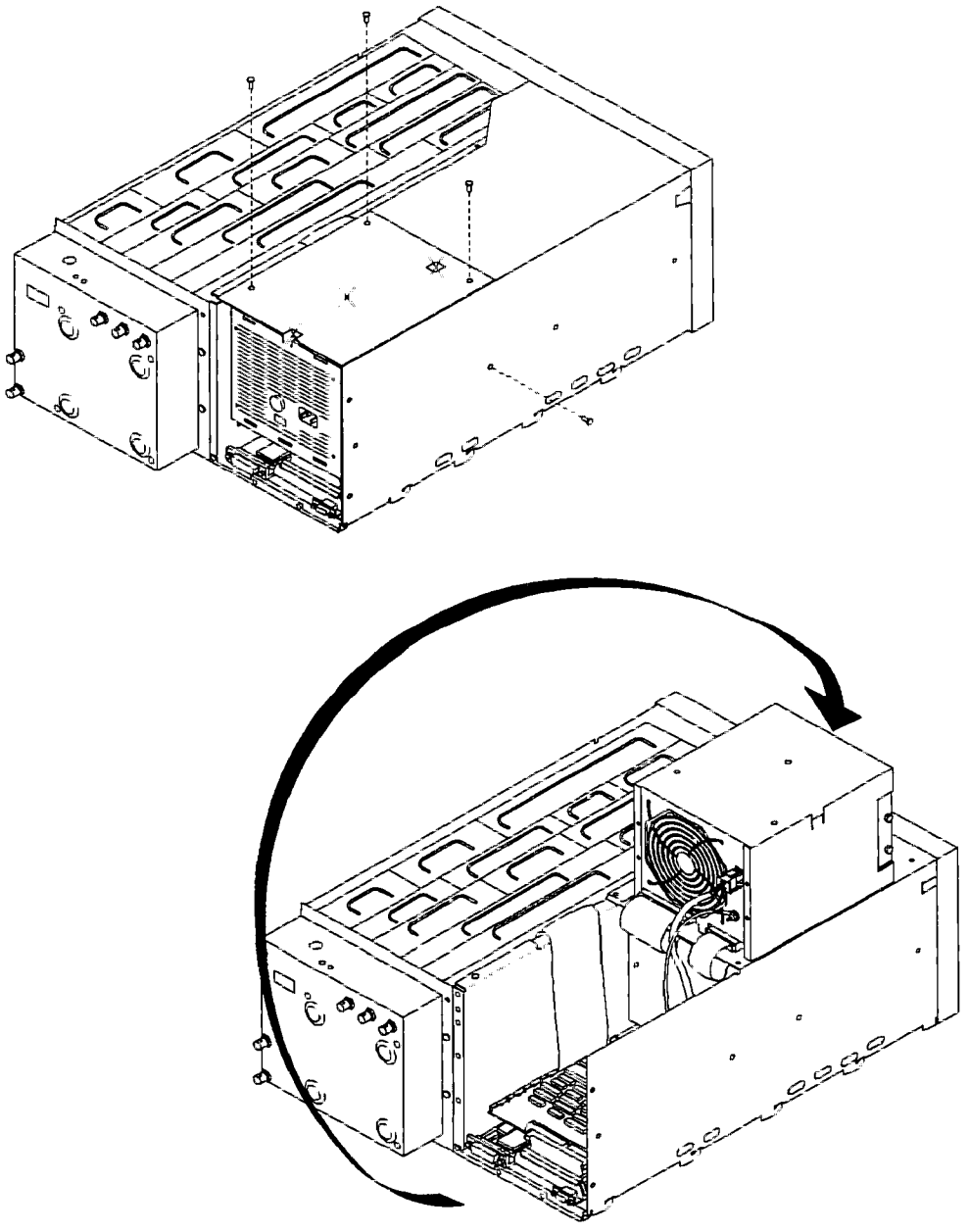


Figure 6-5. Power Supply

Note

Follow these steps when replacing the Front Panel assembly:

Connect the power cable and front-panel cable to the Front Panel assembly.
With the top of the Front Panel assembly tilted away from the analyzer, align the 3 plastic flanges (on the bottom of the Front Panel assembly) with the slots in the chassis.
Align the Disk Drive assembly with the opening on the Front Panel assembly.
Align the dress plate with the N connectors.
Push the top of the Front Panel assembly back, snapping the 3 clips into place.

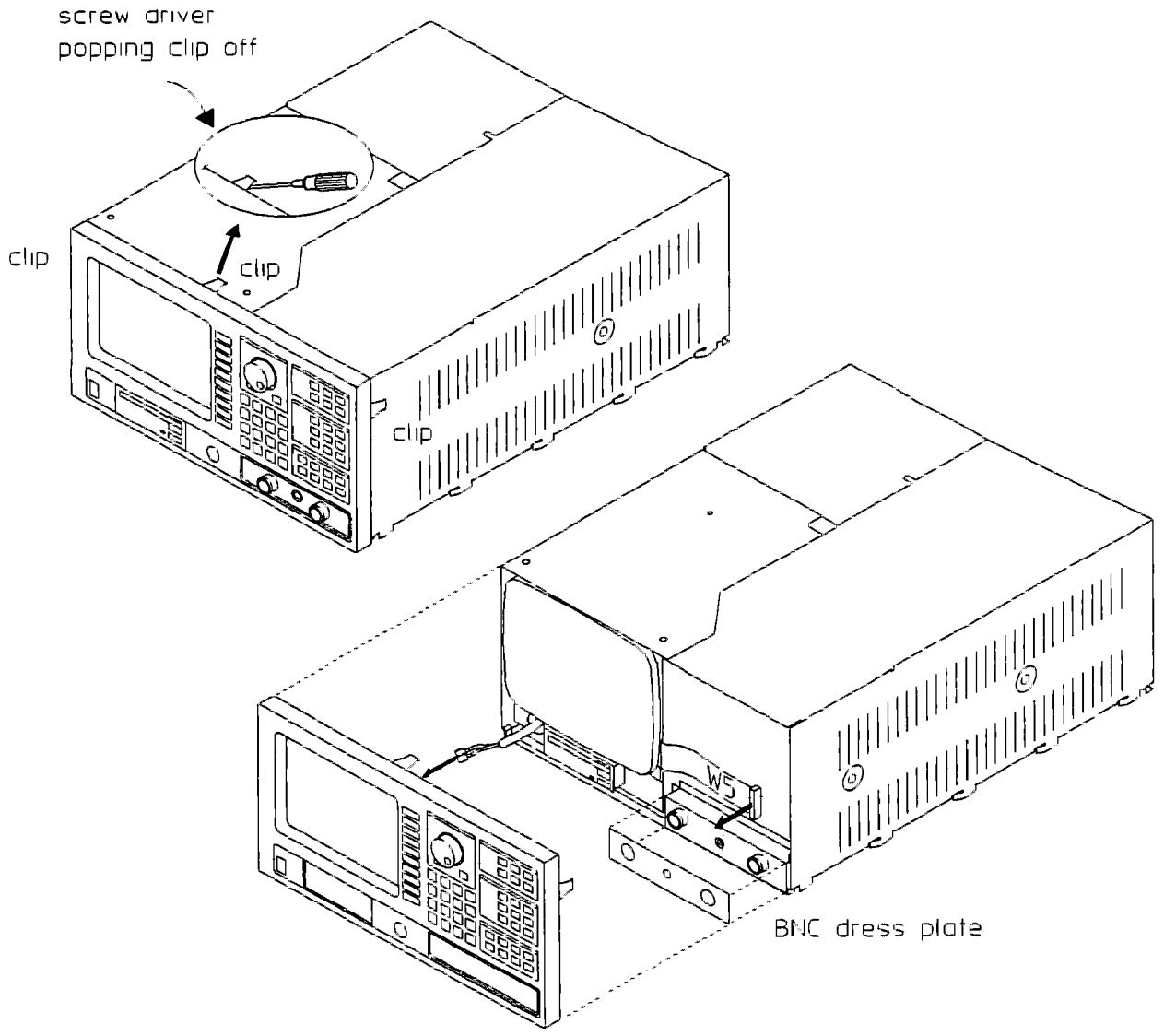


Figure 6-6. Front Panel

Note

When reinstalling the CPU assembly, connect the display cable before placing the CPU assembly in position.

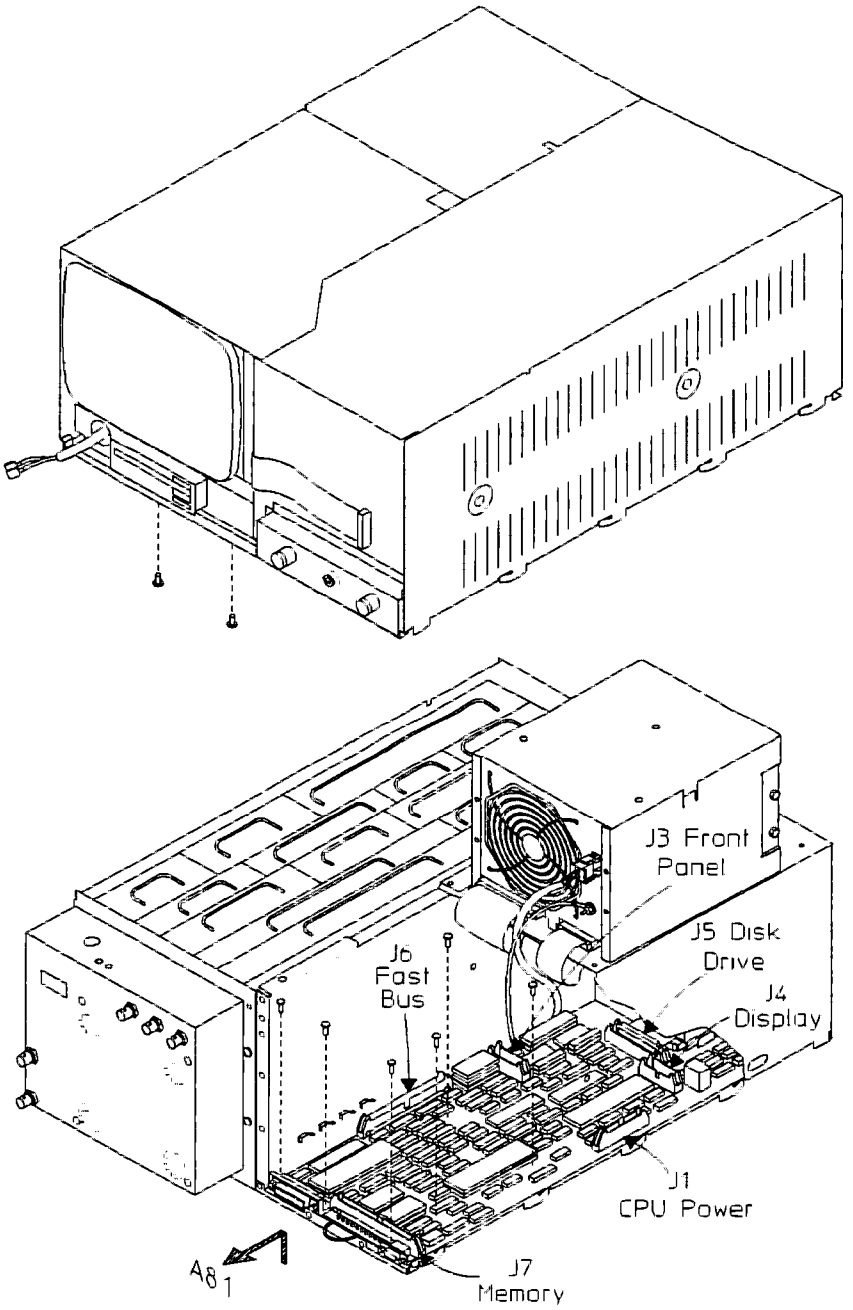


Figure 6-7. CPU

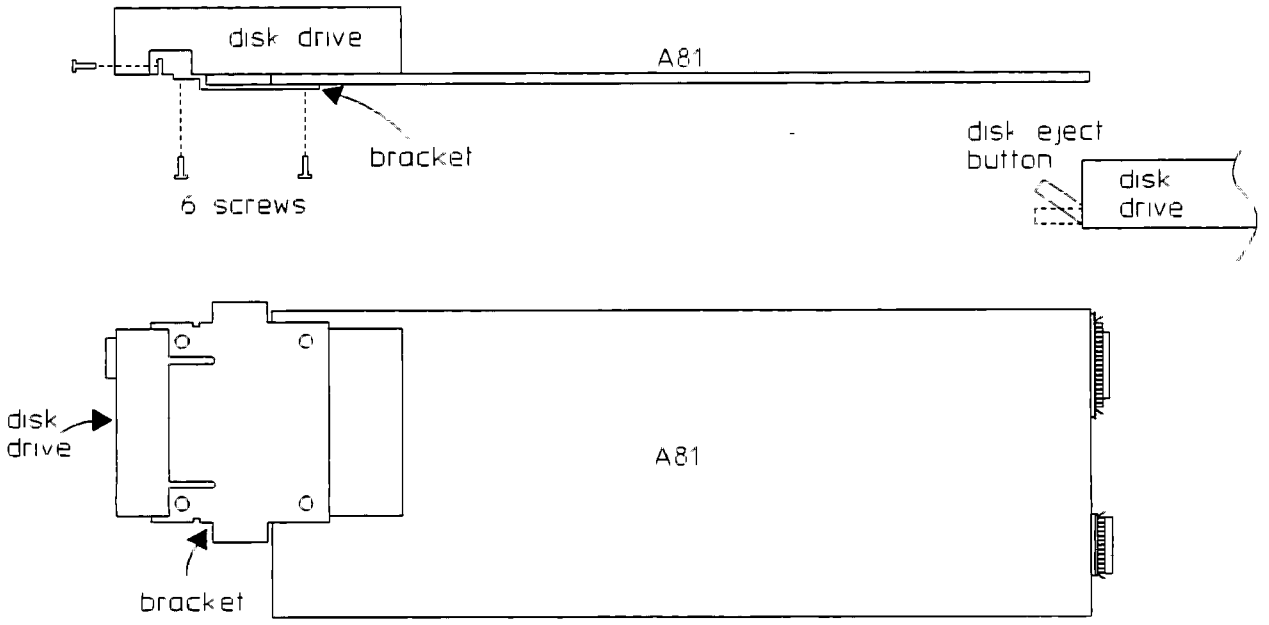


Figure 6-8. Disk Drive

Caution When replacing the Display assembly, be careful to keep the front-panel cable flat against the inside center wall.

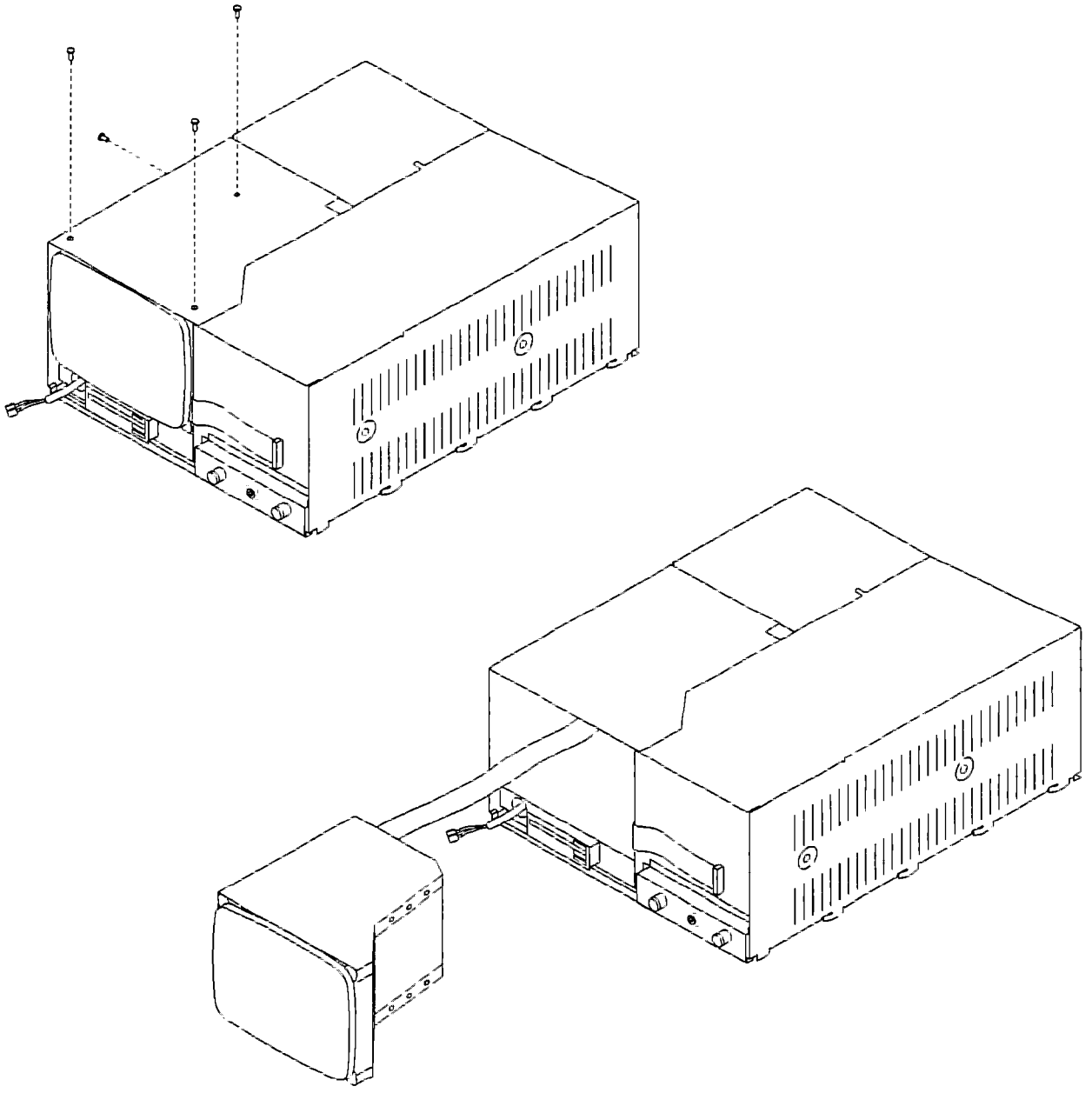


Figure 6-9. Display

Caution Before positioning the fan/oven housing against the chassis, connect the cable from the motherboard to the assembly, and carefully route the cable from the motherboard around the fan and the RF cables through the slots in the chassis.

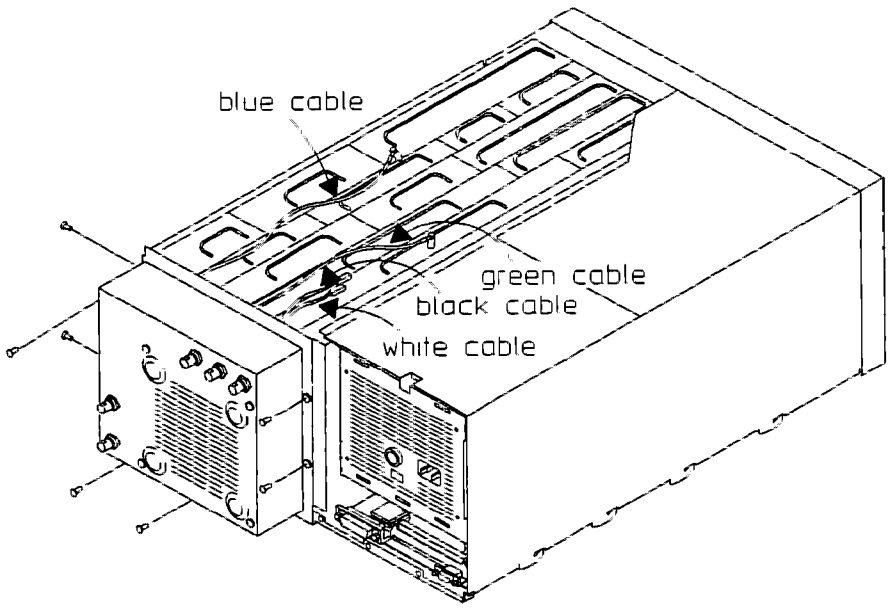


Figure 6-10. Fan/Oven Housing

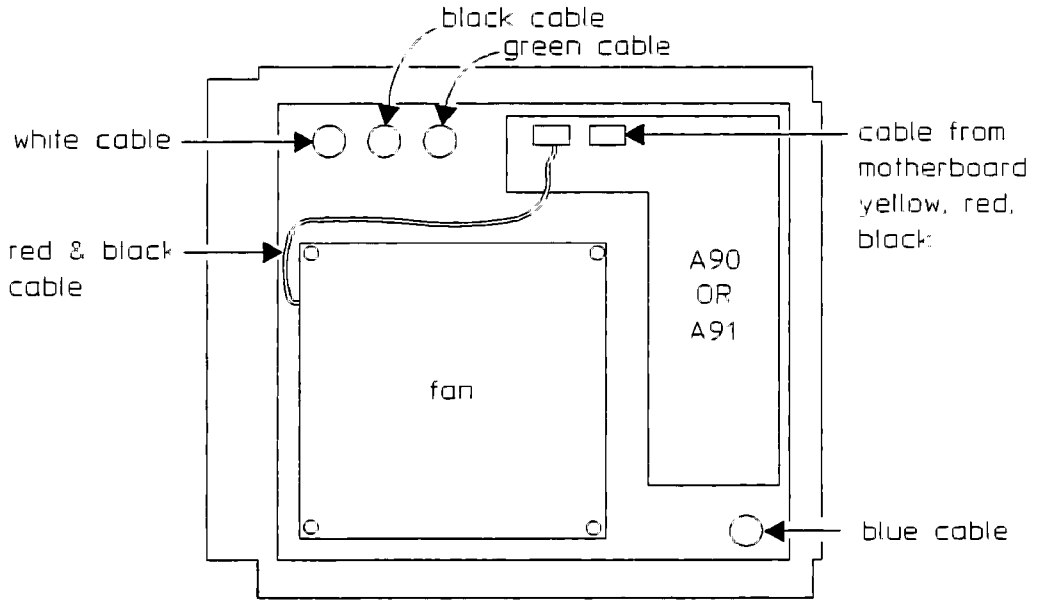


Figure 6-11. Fan/Oven

Note Connect motherboard power cable before placing card nest in chassis.

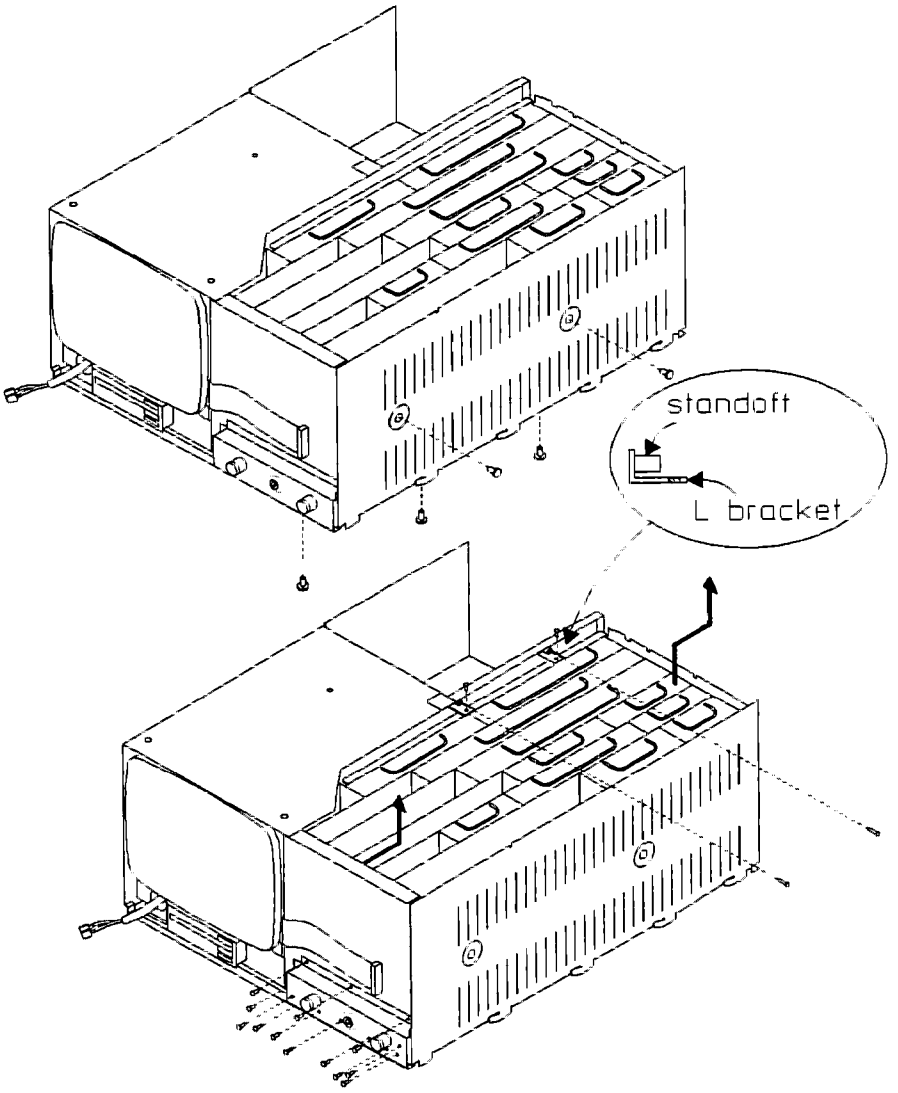


Figure 6-12. Card Nest

What to Do After Replacing an HP 35689A/B Assembly

After replacing an assembly in the HP 35689A/B S-Parameter Test Set, do the following:

1. Reinstall all assemblies and cables that were removed during troubleshooting.
2. Do Test 36. HP 35689A/B Initial Verification (see page 4-88).
3. Do the operation verification tests (see page 3-45).

HP 35689A/B Disassembly/Assembly

Use the following illustrations to disassemble and assemble the HP 35689A/B Test Set.

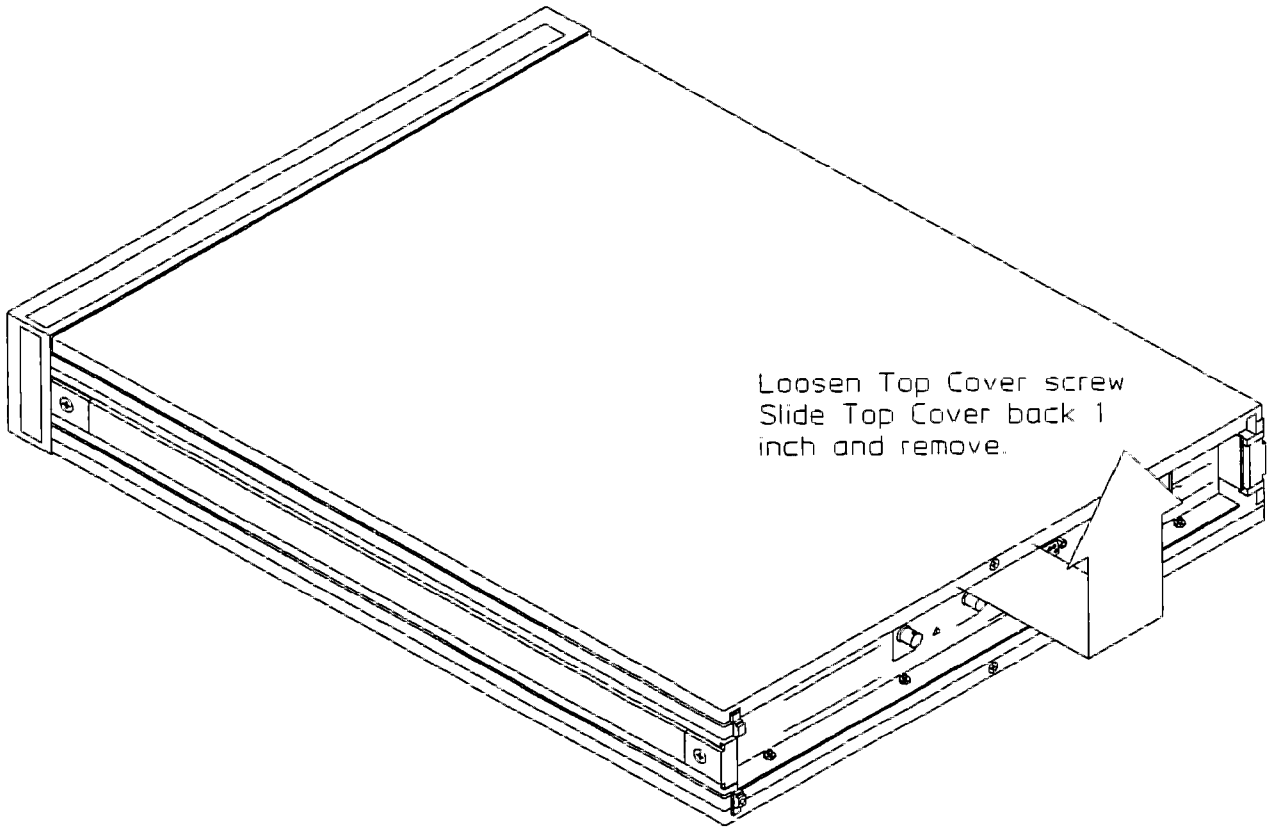


Figure 6-13. Top Cover

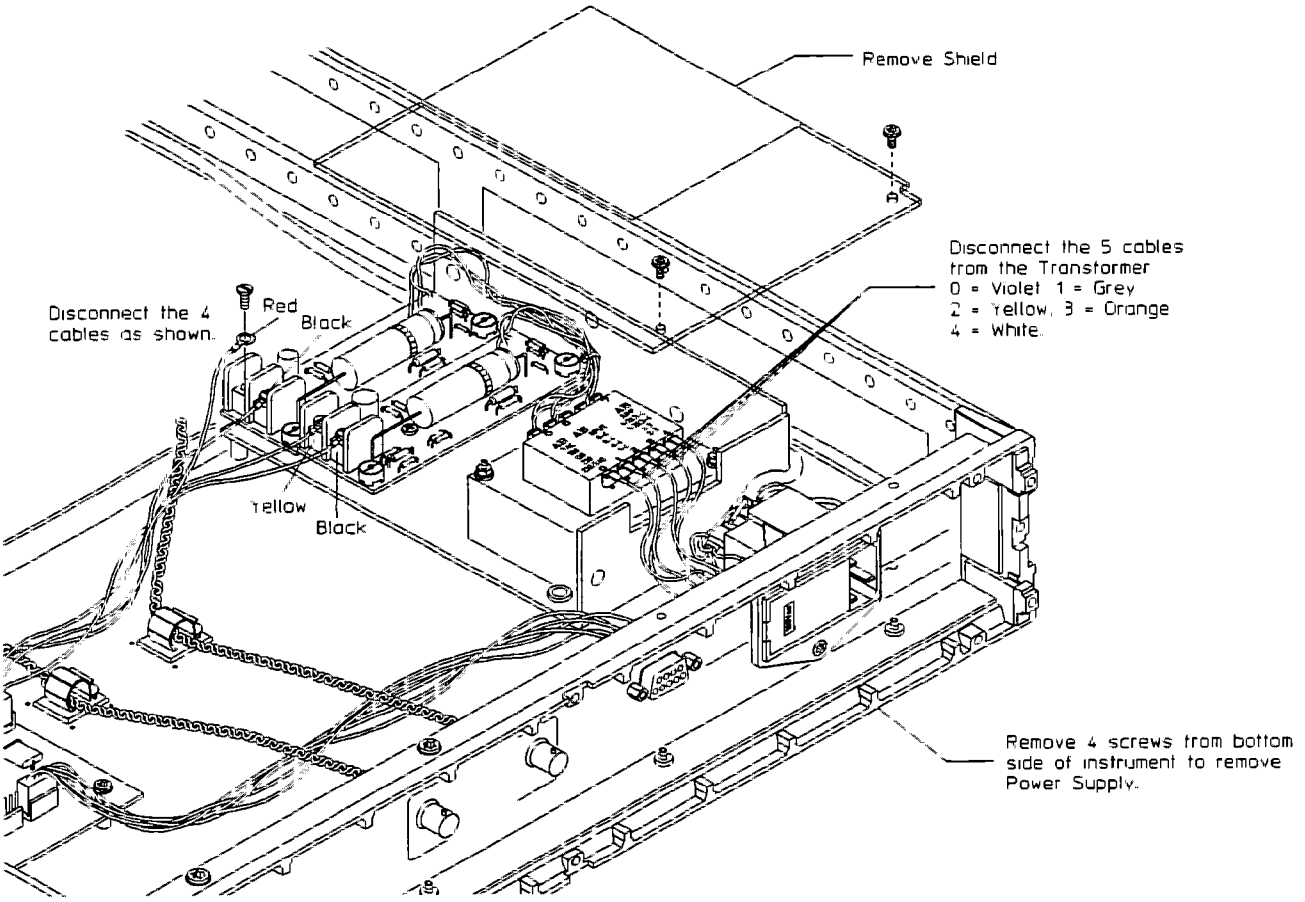


Figure 6-14. Power Supply

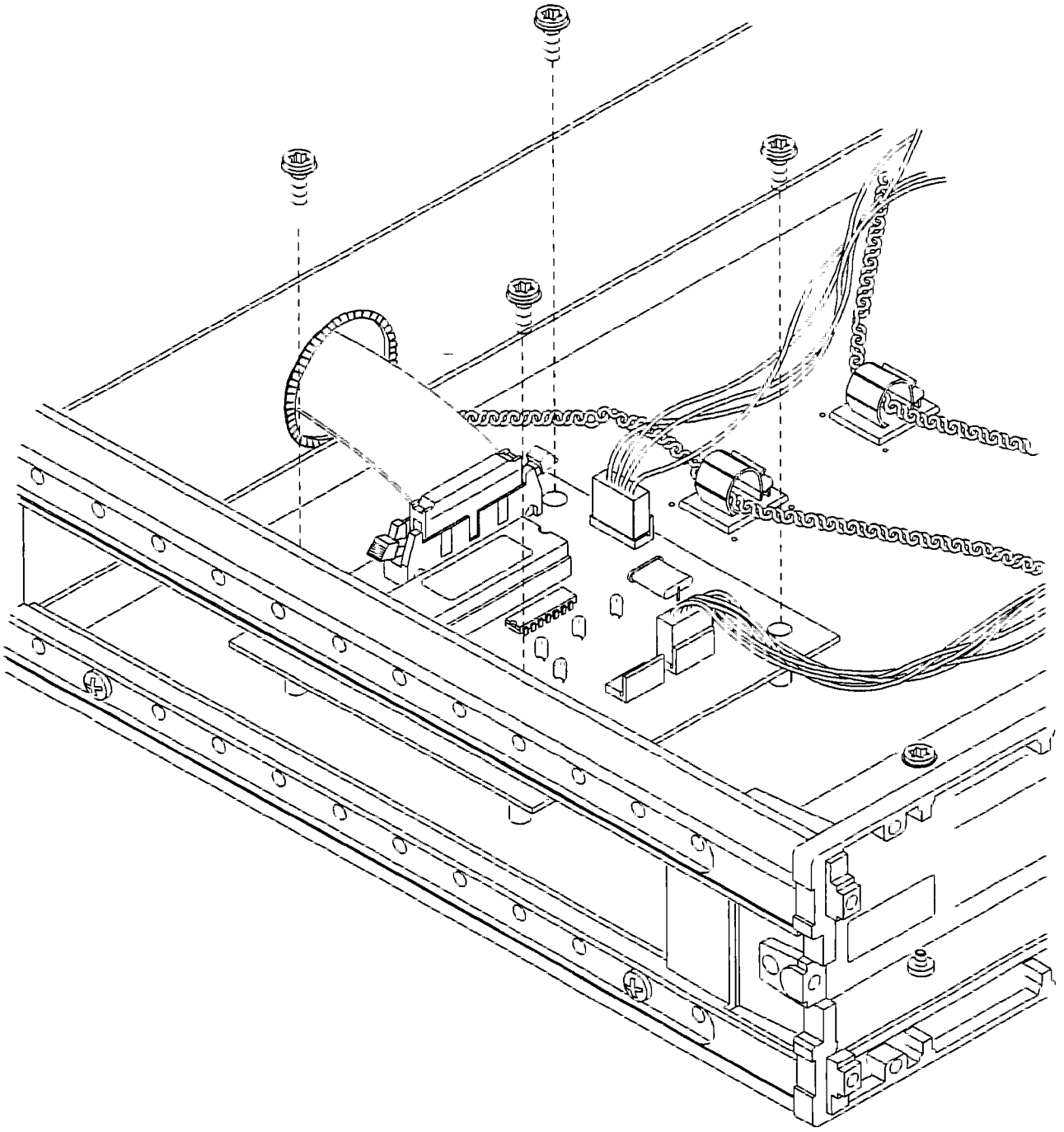


Figure 6-15. Controller Assembly

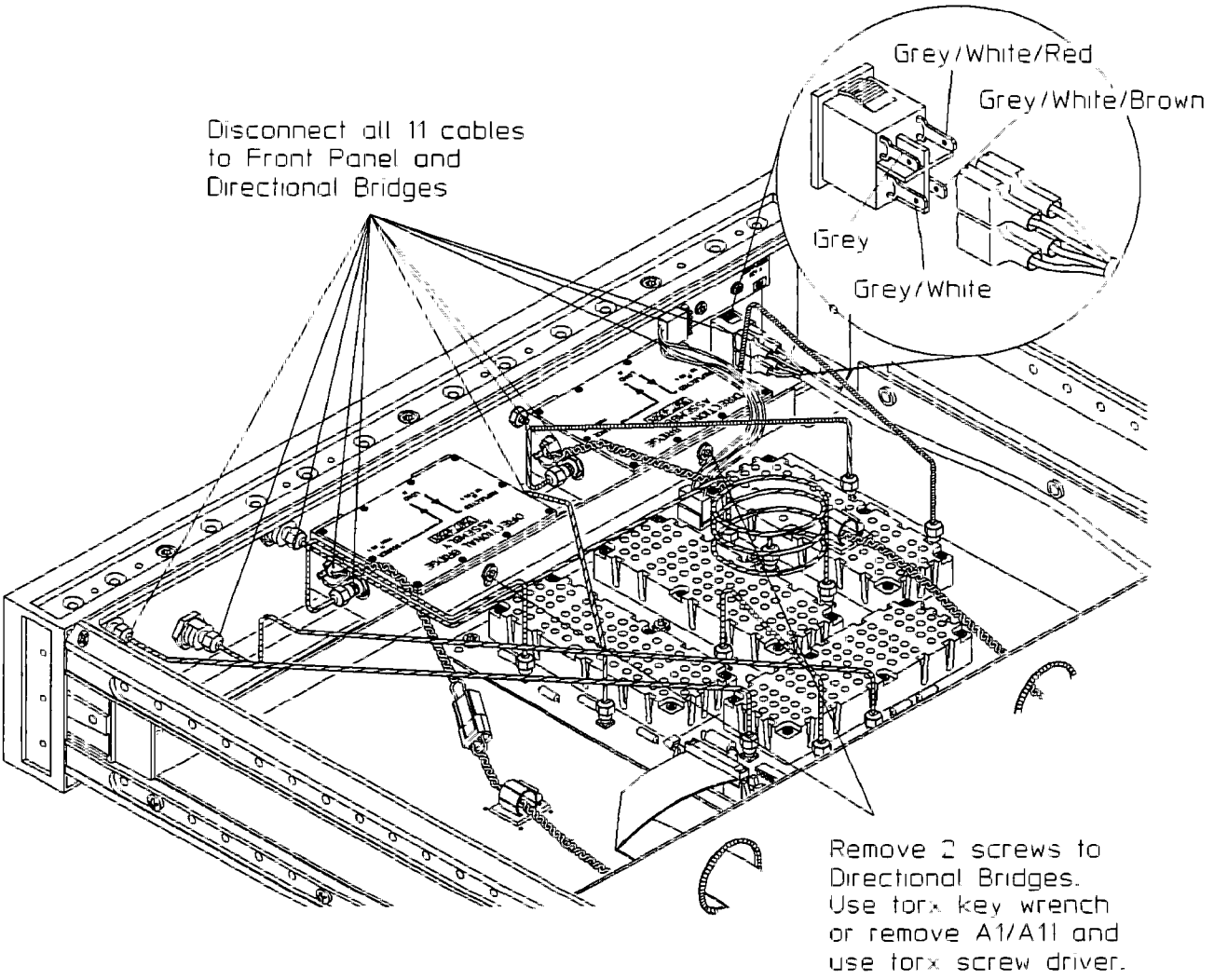


Figure 6-16. Directional Bridge

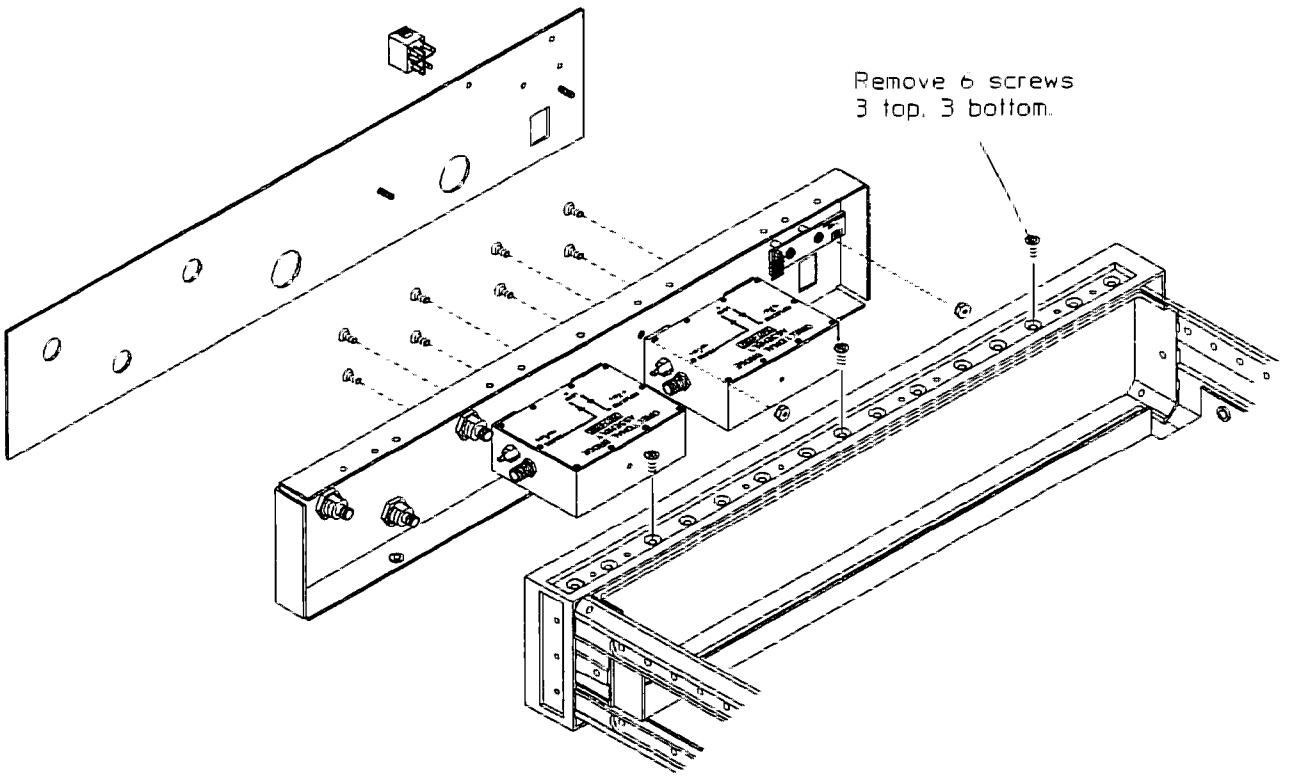


Figure 6-16. Directional Bridge (continued)

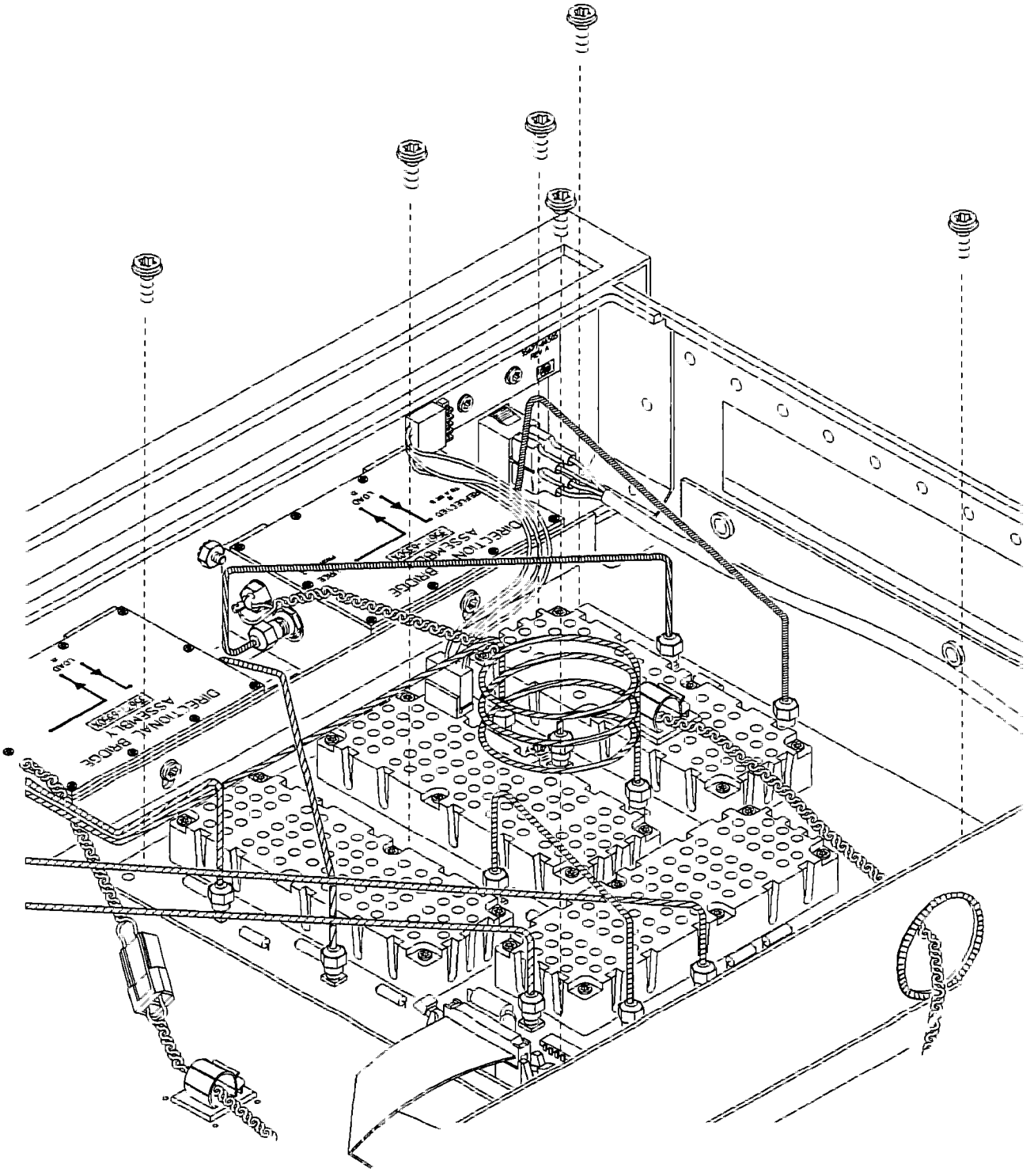


Figure 6-17. RF Assembly

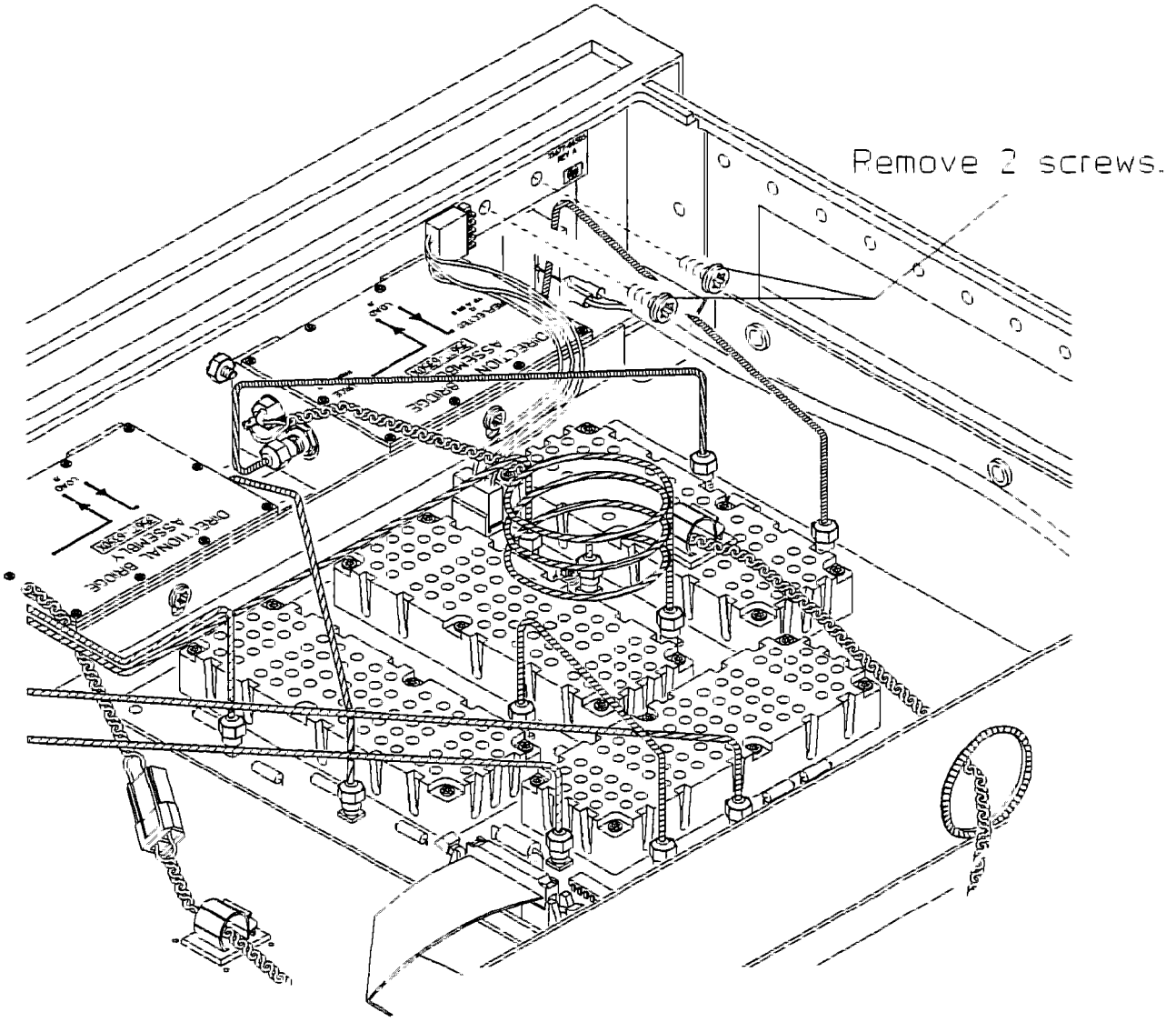


Figure 6-18. LED Assembly

Replaceable Parts

Introduction

This chapter contains information for ordering replacement parts for the HP 3589A Spectrum/Network Analyzer and HP 35689A/B S-Parameter Test Set.

Replacement parts for each instrument are separated into the following categories:

- Assemblies
- Cables
- Instrument Covers and Handles
- Assembly Covers and Brackets
- Front Panel Parts
- Rear Panel Parts
- Chassis Parts
- Card Nest Parts
- Screws, Washers, and Nuts
- Miscellaneous Parts

Caution

Many of the parts listed in this chapter are static sensitive. Use the appropriate precautions when removing, handling, and installing all parts to avoid unnecessary damage.

Ordering Information

Note

See the final pages in the back of this manual for a list of Hewlett-Packard sales and service office locations and addresses.

Ordering Non-Listed Parts

To order a part that is NOT listed in the replaceable parts tables, indicate the instrument model number, instrument serial number, description and function of the part, and the quantity of the part required. Address the order to the nearest Hewlett-Packard sales and service office.

Direct Mail Order System

Within the U.S.A., Hewlett-Packard can supply parts through a direct mail order system. Advantages of the Direct Mail Order System are:

- Direct ordering and shipment from the HP Parts Center.
- No maximum or minimum on any mail order. There is a minimum order for parts ordered through a local HP sales and service office when the orders require billing and invoicing.
- Transportation charges are prepaid. A small handling charge is added to each order.
- No invoicing. A check or money order must accompany each order.
- Mail order forms and specific ordering information are available through your local Hewlett-Packard sales and service office.

Table 7-1. Abbreviations Used

Abbreviations			
Ag	silver	Ne	neon
Al	aluminum	NO	normally open
A	ampere(s)	NPO	negative positive zero
Au	gold	–	(zero temperature coefficient)
cer	ceramic	ns	nanosecond(s) = 10^{-9} seconds
coef	coefficient	nsr	not separately replaceable
com	common	obd	order by description
conn	connection	OD	outside diameter
dep	deposited	p	peak
DPDT	double-pole double-throw	pc	printed circuit
DPST	double-pole single-throw	pF	picofarad(s) 10^{-12} farads
elect	electrolytic	piv	peak inverse voltage
encap	encapsulated	p/o	part of
F	farad(s)	pos	position(s)
FET	field effect transistor	poly	polystyrene
fxd	fixed	pot	potentiometer
GaAs*	gallium arsenide	p-p	peak-to-peak
GHz	gigahertz = 10^{+9} hertz	ppm	parts per million
Gd	guard(ed)	prec	precision (temperature coefficient
Ge	germanium		long term stability and/or tolerance)
gnd	ground(ed)	R	resistor
H	henry(ies)	Rh	rhodium
Hg	mercury	rms	root-mean-square
Hz	hertz (cycle(s) per second)	rot	rotary
ID	inside diameter	Se	selenium
impg	impregnated	sect	section(s)
incd	incandescent	Si	silicon
ins	insulation(ed)	sl	slide
kΩ	kilohm(s) = 10^{+3} ohms	SPDT	single-pole double-throw
kHz	kilohertz = 10^{+3} hertz	SPST	single-pole single-throw
L	inductor	Ta	tantalum
lin	linear taper	TC	temperature coefficient
log	logarithmic taper	TiO_2	titanium dioxide
mA	milliampere(s) = 10^{-3} amperes	tog	toggle
MHz	megahertz = 10^{+6} hertz	tol	tolerance
MΩ	megohms(s) = 10^{+6} ohms	trim	trimmer
met film	metal film	TSTR	transistor
mfr	manufacturer	V	volt(s)
ms	microsecond	vacw	alternating current working voltage
mtg	mounting	var	variable
mV	millivolt(s) = 10^{-6} volts	vdcw	direct current working voltage
μF	microfarad(s)	W	watts
μs	microsecond(s)	w/	with
μV	microvolt(s) = 10^{-6} volts	wiv	working inverse voltage
my	Mylar®	w/o	without
nA	nanoampere(s) = 10^{-9} amperes	ww	wirewound
NC	normally closed		

* optimum value selected at factory average value shown (part may be omitted)
**no standard type assigned selected or special type
® Dupont de Nemours

Table 7-1. Abbreviations Used (continued)

Designators			
A	assembly	Q	transistor
B	motor	QCR	transistor-diode
BT	battery	R	resistor
C	capacitor	RT	thermistor
CR	diode or thyristor	S	switch
DL	delay line	T	transformer
DS	lamp	TB	terminal board
E	misc electronic part	TC	thermocouple
F	fuse	TP	test point
FL	filter	TS	terminal strip
HR	heater	U	microcircuit
IC	integrated circuit	V	vacuum tube
J	jack	W	cable jumper
K	relay	X	socket
L	inductor	XDS	lampholder
M	meter	XF	fuseholder
MP	mechanical part	Y	crystal
P	plug	Z	network

Table 7-2. Manufacturers' Code List

Mfr No.	Mfr Name	Address
L0514	Degussa Corporation GFO Div.	Hayward, CA 94545
L2276	Syndetek Corporation	Spokane, WA 99202
L3095	Deltron Inc	Utilvend, PA 19454
L3606	Kasho (USA) Inc.	San Francisco, CA 94105
00848	Lee Mah Electronics	San Francisco, CA 94133
01642	Sons Tool Inc	Woodville, WI 55412
03480	Heyco Molded Products	Kentworth, NJ 07033
05030	Barry Controls	Brighton, MA 02135-9105
05502	Connor Spring & Mfg Co.	San Jose, CA 95112
05610	Camcar Screw & Mfg Co.	Rockford, IL 61101
05791	Lyn-Tron Inc	Burbank, CA 91505
06090	Raychem Corp	Bellevue, WA 98009
06363	Oudensha America Inc.	Elk Grove Villa, IL 60007
06860	Huber & Suhner AG	Essex, VT 05451
06916	Sony Corp	Toyko, JP
09328	Dreefs Switch Inc.	Waukegan, IL 60087
09441	Applied Engineering Product Co	Hamdem CT 06514
12136	PHC Industries Inc.	Philadelphia, PA 19101
22670	Nameplate	Seattle, WA 98119
28480	Hewlett-Packard Company	Palo Alto, CA 94304
30817	Instrument Specialties Co. Inc.	Placentia, CA 92670
34785	Dek Inc.	St Charles, IL 60174
3U116	TRW Electronic Components Group	Marshall, IL 62441
43744	Panasonic Industrial Co	Milpitas, CA 95035
55002	Power Conversion Inc.	Elmwood Park, NJ 07407
57003	Chomerics Shielding Technology	Carson, CA 90745
73734	Federal Screw Products Co.	Chicago, IL 60618
75915	Littelfuse Inc.	Des Plaines, IL 60016
76381	3M Co.	Seattle, WA 98124
77250	Lewis Screw Co.	Chicago, IL 60609
78471	Tilley Mfg Co	Morgan Hill, CA 95037
83486	Elco Industries Inc.	Rockford, IL 61101
86928	Seastrom Mfg Co.	Glendale, CA 91201
90949	Amphenol Corporation RF/Microwave Operation	Danbury, CT 06810

HP 3589A Reference Designators and Part Numbers

To order a part in tables 7-3 through 7-12, quote the Hewlett-Packard part number, the check digit (CD), indicate the quantity required, and address the order to the nearest Hewlett-Packard sales and service office. The check digit verifies that an order has been transmitted correctly, ensuring accurate and timely processing of the order. The first time a part is listed in the table, the quantity column lists the total quantity of the part used in the analyzer. See table 7-2 for a table listing the manufacturers' code numbers and the corresponding names and addresses.

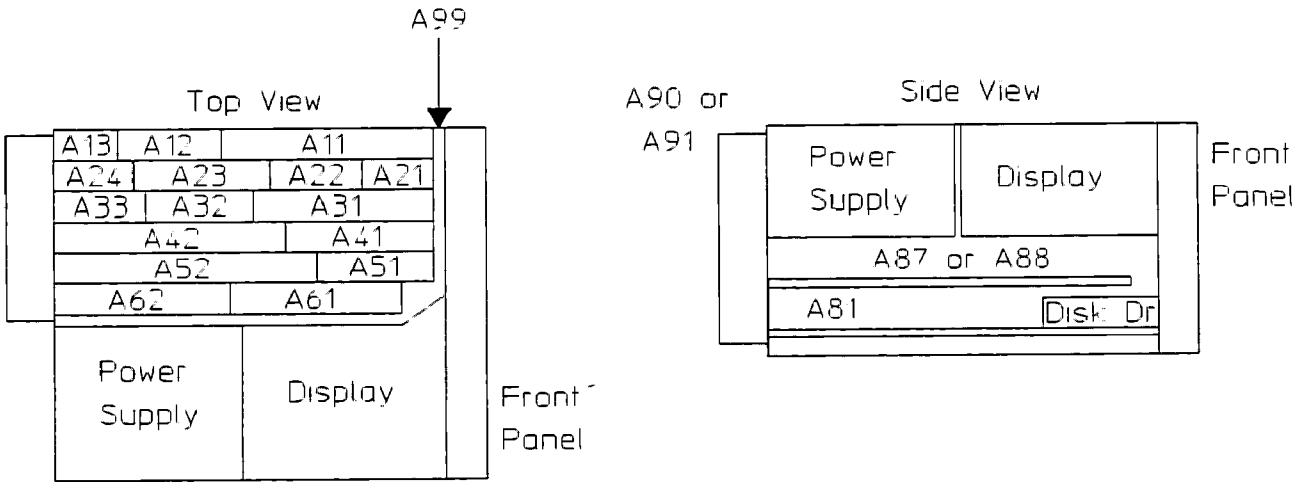


Figure 7-1. Reference Designators for Assemblies

Table 7-3. Assemblies

Ref.Des.	HP Part Number	CD	Qty	Description	Mfr. Code	Mfr. Part Number
A11	03589-69511	4	1	EXCHANGE PC ASSY - INPUT	28480	03589-69511
A12	03589-69512	5	1	EXCHANGE PC ASSY - FIRST CONVERSION	28480	03589-69512
A13	03588-69513	5	1	EXCHANGE PC ASSY - SECOND CONVERSION	28480	03588-69513
A21	03588-69521	5	1	EXCHANGE PC ASSY - SUM VCO	28480	03588-69521
A22	03588-69522	6	1	EXCHANGE PC ASSY - SUM PHASE DETECTOR	28480	03588-69522
A23	03588-69523	7	1	EXCHANGE PC ASSY - STEP PHASE DETECTOR	28480	03588-69523
A24	03588-69524	8	1	EXCHANGE PC ASSY - STEP VCO	28480	03588-69524
A31	03588-69531	7	1	EXCHANGE PC ASSY - REFERENCE/CALIBRATOR	28480	03588-69531
A32	03589-69532	9	1	EXCHANGE PC ASSY - 300 MHZ	28480	03589-69532
A33	03589-69533	0	1	EXCHANGE PC ASSY - TRIGGER	28480	03589-69533
A41	03589-69541	0	1	EXCHANGE PC ASSY - SOURCE AMPLIFIER	28480	03589-69541
A42	03588-69542	0	1	EXCHANGE PC ASSY - SOURCE CONVERSION	28480	03588-69542
A51	03588-69551	1	1	EXCHANGE PC ASSY - INTERPOLATION VCO	28480	03588-69551
A52	03589-69552	3	1	EXCHANGE PC ASSY - FRACTIONAL_N	28480	03589-69552
A61	03588-69561	3	1	EXCHANGE PC ASSY - IF	28480	03588-69561
A62	03589-69562	5	1	EXCHANGE PC ASSY - DIGITAL FILTER	28480	03589-69562
A72	35672-66572	0	1	PC ASSY - KEYBOARD	28480	35672-66572
A81	03589-69581	8	1	EXCHANGE PC ASSY - CPU	28480	03589-69581
A87	03589-69587	4	1	EXCHANGE PC ASSY - MEMORY	28480	03589-69587
A88	03589-69588	5	1	EXCHANGE PC ASSY - EXP MEMORY (OPT 1C1)	28480	03589-69588
A90	03588-66590	2	1	PC ASSY - FAN POWER	28480	03588-66590
A91	03588-66591	3	1	PC ASSY - FAN POWER/OVEN (OPTION 1D5)	28480	03588-66591
A99	03589-66599	2	1	PC ASSY - MOTHERBOARD	28480	03589-66599
A100	09123-69101	0	1	EXCHANGE DISC 3 5" FLOPPY DRIVE	06916	MP-F52W-30
A101	35672-69301	9	1	DSPL 9" RASTER GRN 576X400	43744	–
A103	35672-67501	7	1	PWR SPLY CUSTOM 180W-7 OUTPTS	3U116	35672-67501
A104	03561-68501	8	1	FAN-ASSY	28480	03561-68501

After replacing an assembly, see "What to Do After Replacing an HP 3589A Assembly" in chapter 6

New Disk Drive P/N 0950-1798

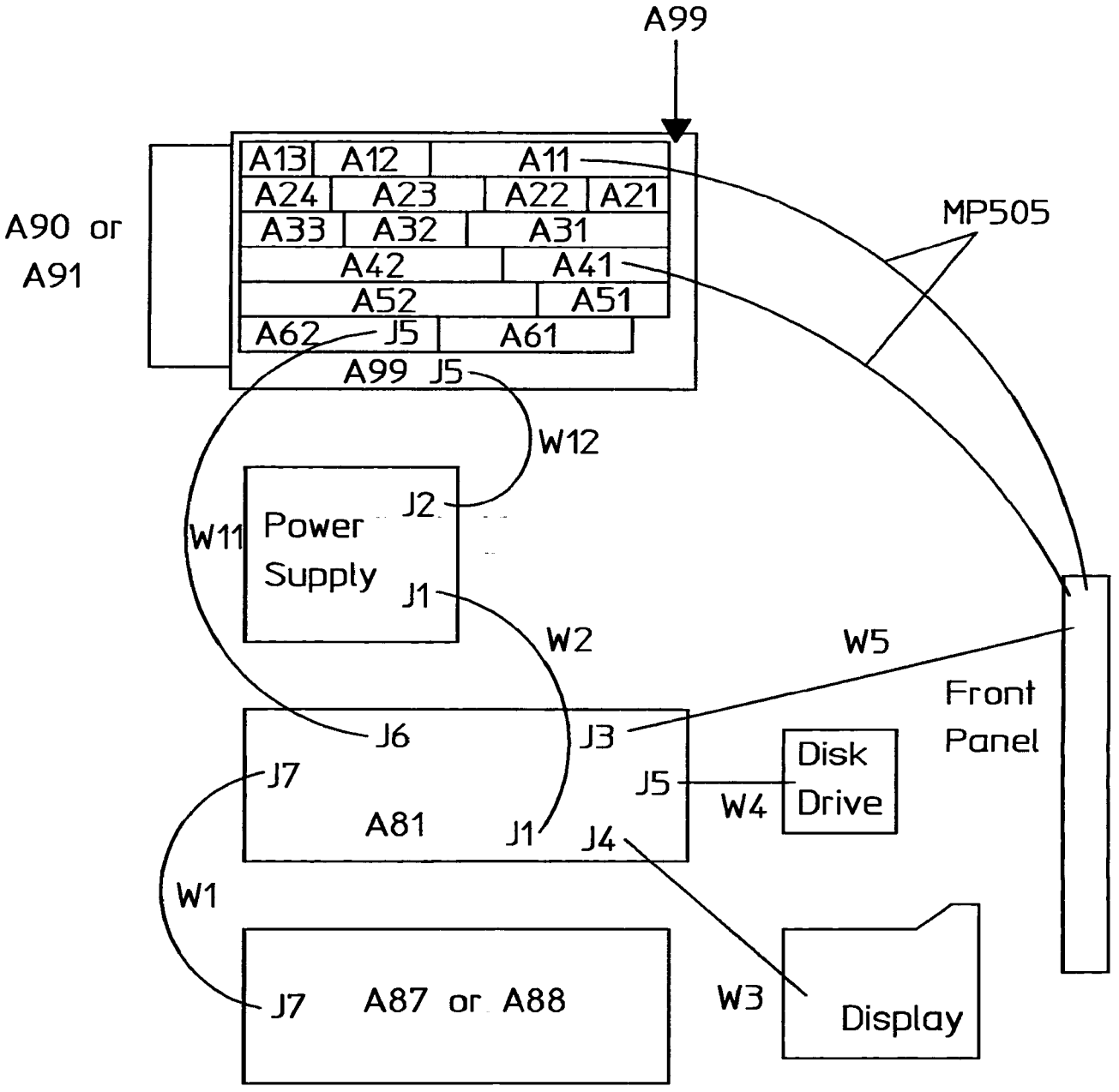


Figure 7-2. Reference Designators for Cables

Table 7-4. Cables

Ref.Des.	HP Part Number	CD	Qty	Description	Mfr. Code	Mfr. Part Number
W1	35672-61601	6	1	CBL-ASM RBN FHDR/FHDR 40MM GY - MEMORY	76381	35672-61601
W2	35672-61602	7	1	CBL-ASM RBN FHDR/FHDR 290MM GY - CPU PWR	76381	–
W3	35672-61603	8	1	CBL-ASM RBN FHDR/FHDR 325MM GY - DISPLAY	76381	–
W4	35672-61604	9	1	CBL-ASM RBN FHDR/FHDR 35MM GY - DISK DRIVE	76381	–
W5	35672-61605	0	1	CBL-ASM RBN FHDR/FHDR 450MM GY - FRNT PNL	76381	–
W7	35672-61607	2	1	CBL-ASM MLT FCRP/FHSG 615MM GY - PWR SW	28480	35672-61607
W11	35660-61611	4	1	CBL-ASM RBN FHDR/FHDR 350MM GY - FAST BUS	76381	–
W12	03588-61699	2	1	CBL-ASM RBN FSKT/FSKT 360MM - MTHRBRD PWR	L1624	–
W21	35665-61621	1	1	CBL-ASM FD1N1FHSG 200MM LG ML - DIN CONN	L2276	–
W101	03577-61621	7	2	CBL-ASM CXL FSMB/FSMB 220MM WHITE	28480	03577-61621
W102	03577-61622	8	1	CBL-ASM CXL FSMB/FSMB 160MM YELLOW	28480	03577-61622
W103	03577-61641	1	6	CBL-ASM CXL FSMB/FSMB 135MM ORANGE	28480	03577-61641
W104	03585-61602	4	10	CBL-ASM CXL FSMB/FSMB 76MM RED	28480	03585-61602
W105	03585-61605	7	2	CBL-ASM CXL FSMB/FSMB 330MM GREEN	28480	03585-61605
W106	03585-61606	8	1	CBL-ASM CXL FSMB/FSMB 406MM BLUE	28480	03585-61606
W107	03586-61677	4	4	CBL-ASM CXL FSMB/FSMB 265MM BLUE	28480	03586-61677
W108	03588-61602	7	1	CBL-ASM MBNC/FHSG 200MM BK-EXT TRIG/GATE	28480	03588-61602
W109	03588-61603	8	1	CBL-ASM MBNC/FHSG 200MM WT-TRIG/GATE OUT	28480	03588-61603
W110	03588-61604	9	1	CBL-ASM MBNC/MSMB 578MM BLUE - EXT REF IN	28480	03588-61604
W111	03588-61605	0	1	CBL-ASM MBNC/MSMB 478MM GREEN - REF OUT	28480	03588-61605
W112	03588-61607	2	1	CBL-ASM CXL FSMB/FSMB 85MM BLACK	28480	03588-61607
W113	03588-61608	3	1	CBL-ASM CXL FSMB/FSMB 270MM GRAY	28480	03588-61608
W114	03588-61695	8	1	CBL-ASM FHSH/STRP 75MM ML - PROBE POWER	28480	03588-61695
MP505	03589-61660	8	2	CBL-ASM RGD MN/MSMB (INPUT/SOURCE CABLES)	09441	03589-61660

Note

The reference designator for the screws that fasten the top cover and the handles to the chassis is MP609. See table 7-11 for the part number.

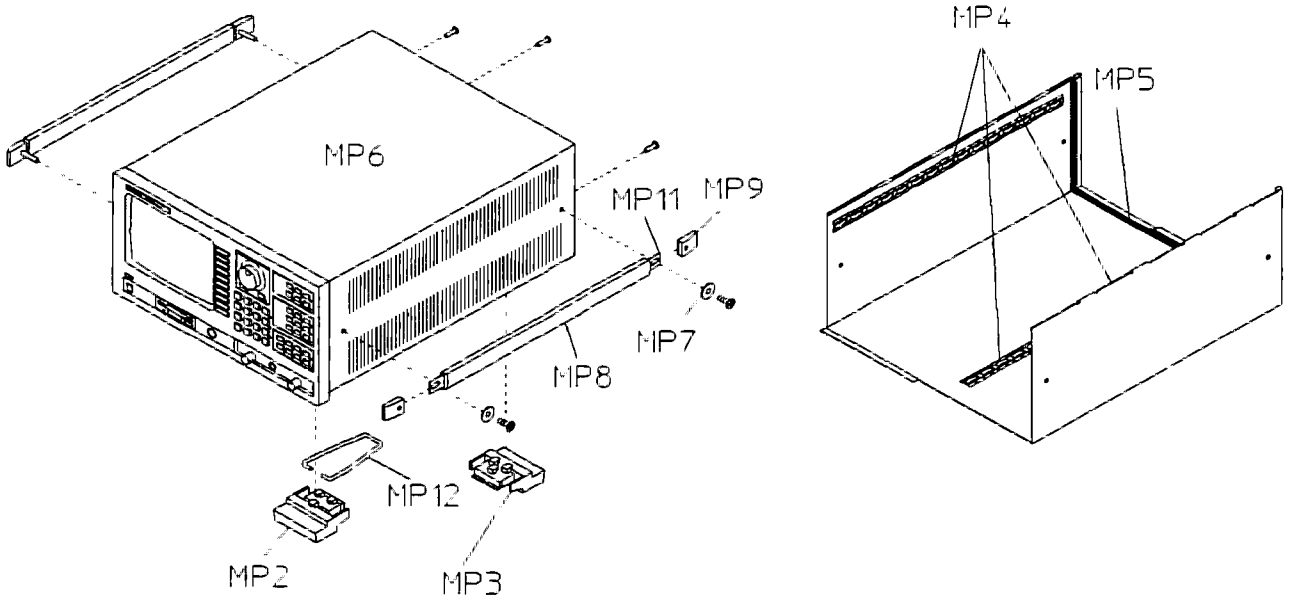


Figure 7-3. Reference Designators for Instrument Covers and Handles

Table 7-5. Instrument Covers and Handles

Ref.Des.	HP Part Number	CD	Qty	Description	Mfr. Code	Mfr. Part Number
MP2	5041-8801	8	2	MOLD FOOT II+	28480	5041-8801
MP3	5041-8822	3	2	MOLD FOOT-NON SKID II+	28480	5041-8822
MP4	8160-0636	6	3	STMP GROUND STRIP BE/CU .156H	30817	0786-0162-00
MP5	35672-44100	4	1	GSKT-EMI MONEL/NEOPRENE	57003	–
MP6	35672-04111	3	1	SHTF COVER AL	28480	35672-04111
MP7	35672-21703	5	4	MCHD RETAINER SS	28480	35672-21703
MP8	35672-41201	0	2	MOLD VINYL EXTRUSION	12136	35672-41201
MP9	35672-45004	9	4	MOLD ENDCAP	28480	35672-45004
MP11	35672-01202	7	2	MCHD SS STRAP SS	28480	35672-01202
MP12	1460-1345	5	2	TILT STAND SST	05502	–

Note

The reference designator for the screws that fasten the disk drive to the mounting bracket (MP104) is MP606. See table 7-11 for the part number.

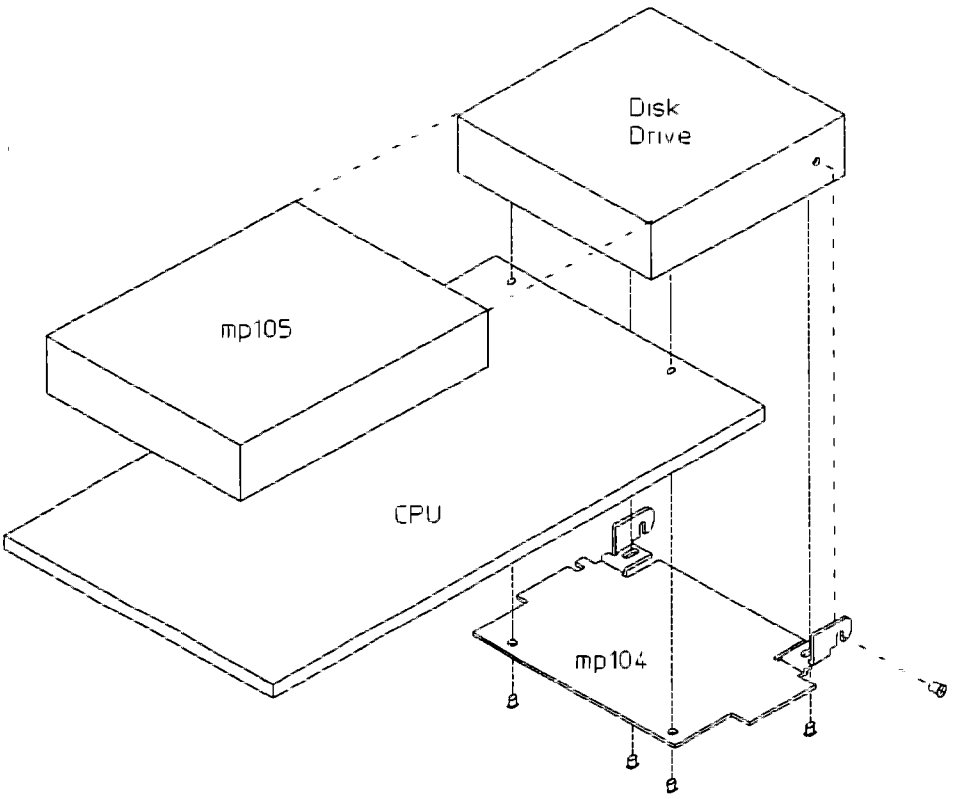


Figure 7-4. Reference Designators for Assembly Covers and Brackets

Table 7-6. Assembly Covers and Brackets

Ref.Des.	HP Part Number	CD	Qty	Description	Mfr. Code	Mfr. Part Number
MP104	35672-01211	8	1	SHTF BRKT-DISC DRIVE AL	28480	35672-01211
MP105	35672-00601	8	1	SHTF SHIELD-DISC DRIVE PLCR	28480	35672-00601
	03588-04111	3	1	A11 SHTF ASSY-COVER TOP ALSK	28480	03588-04111
	03588-04112	4	1	A12 SHTF ASSY-COVER TOP	28480	03588-04112
	03588-04113	5	1	A13 SHTF ASSY-COVER TOP	28480	03588-04113
	03588-04121	5	1	A21 SHTF ASSY-COVER TOP	28480	03588-04121
	03588-04122	6	1	A22 SHTF ASSY-COVER TOP	28480	03588-04122
	03588-04123	7	1	A23 SHTF ASSY-COVER TOP	28480	03588-04123
	03588-04124	8	1	A24 SHTF ASSY-COVER TOP	28480	03588-04124
	03588-04131	7	1	A31 SHTF ASSY-COVER TOP ALSK	28480	03588-04131
	03588-04132	8	1	A32 SHTF ASSY-COVER TOP ALSK	28480	03588-04132
	03588-04133	9	1	A33 SHTF ASSY-COVER TOP ALSK	28480	03588-04133
	03588-04141	9	1	A41 SHTF ASSY-COVER TOP ALSK	28480	03588-04141
	03588-04142	0	1	A42 SHTF ASSY-COVER TOP ALSK	28480	03588-04142
	03588-04151	1	1	A51 SHTF ASSY-COVER TOP ALSK	28480	03588-04151
	03588-04152	2	1	A52 SHTF ASSY-COVER TOP ALSK	28480	03588-04152
	03588-04161	3	1	A61 SHTF ASSY-COVER TOP ALSK	28480	03588-04161
	03588-04162	4	1	A62 SHTF ASSY-COVER TOP ALSK	28480	03588-04162
	03588-05002	3	1	A11 WFRM HANDLE-111MM BAIL	05502	—
	03588-05002	3	1	A12 WFRM HANDLE-111MM BAIL	05502	—
	03588-05001	2	1	A13 WFRM HANDLE- 53MM BAIL	05502	—
	03588-05001	2	1	A21 WFRM HANDLE- 53MM BAIL	05502	—
	03588-05001	2	1	A22 WFRM HANDLE- 53MM BAIL	05502	—
	03588-05002	3	1	A23 WFRM HANDLE-111MM BAIL	05502	—
	03588-05001	2	1	A24 WFRM HANDLE- 53MM BAIL	05502	—
	03588-05002	3	1	A31 WFRM HANDLE-111MM BAIL	05502	—
	03588-05002	3	1	A32 WFRM HANDLE-111MM BAIL	05502	—
	03588-05002	3	1	A33 WFRM HANDLE-111MM BAIL	05502	—
	03588-05002	3	1	A41 WFRM HANDLE-111MM BAIL	05502	—
	03588-05002	3	1	A42 WFRM HANDLE-111MM BAIL	05502	—
	03588-05002	3	1	A51 WFRM HANDLE-111MM BAIL	05502	—
	03588-05002	3	1	A52 WFRM HANDLE-111MM BAIL	05502	—
	03588-05002	3	1	A61 WFRM HANDLE-111MM BAIL	05502	—
	03588-05003	4	1	A62 WRFM HANDLE-142MM BAIL	05502	—

Note

The reference designator for the screws that fasten the lens (MP214) to the front panel (MP213) is MP616. The reference designator for all other screws used on the front panel is MP617. See table 7-11 for part numbers.

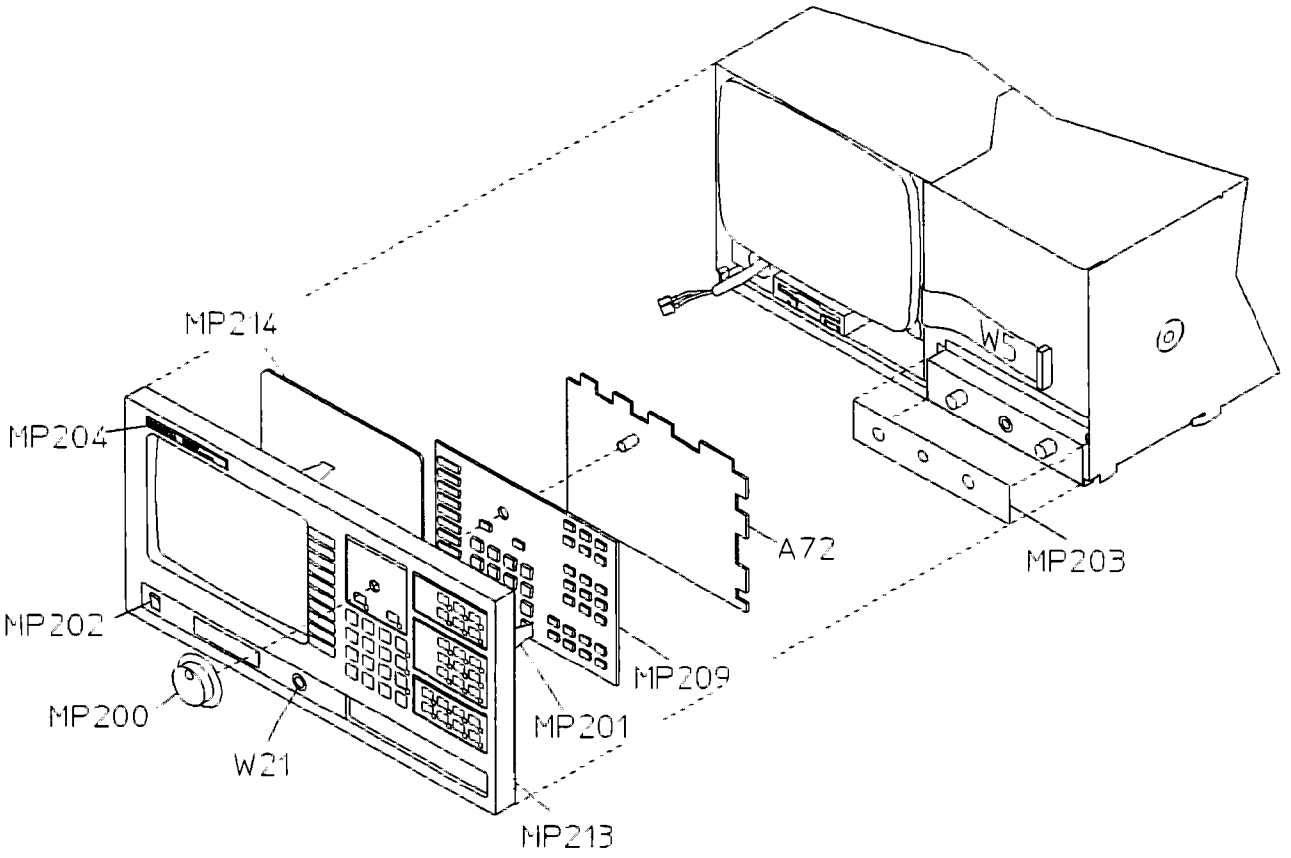


Figure 7-5. Reference Designators for Front Panel Parts

Table 7-7. Front Panel Parts

Ref.Des.	HP Part Number	CD	Qty	Description	Mfr. Code	Mfr. Part Number
MP200	03588-47401	4	1	MOLD KNOB-RPG II+	28480	03588-47401
MP201	35672-05011	4	3	ETCH CLIP MTG BECU	07466	–
MP202	3101-2987	5	1	SW–RKR	09328	WI 32/148
MP203	03589-34301	7	1	PLT-DRESS "03589A"	22670	–
MP204	03589-34302	8	1	PLT-NAME "03589A"	06363	–
MP209	03589-41901	8	1	KYPD ELASTOMERIC "3589A"	L3606	–
MP210	0890-0706	0	0	TUBING-HS .093-D/.046-RCVD 02-WALL	06090	VERSAFIT-3/32-BLK
MP213	03589-64311	2	1	PNL-FRT MOLDED	L0514	–
MP214	35672-49301	7	1	LNZ-CURVED RFI WINDOW	57003	35672-49301

Note

The reference designators for the screws and nuts that fasten the fan (A104) to the fan mount (MP304) are MP609 and MP615. The reference designator for the nuts that fasten the fan mount (MP304) to the rear panel (MP303) is MP614. The reference designator for the screws that fasten the A90/A91 assembly to the rear panel (MP303) is MP605. The reference designator for the inside BNC washers is MP622. The reference designators for the outside BNC washers and nuts are MP618 and MP619. The reference designator for the screws that fasten the rear panels (MP303 and MP301) to the rear of the chassis is MP606. The reference designator for the screws that fasten the rear panels (MP303 and MP301) and power supply to the top and sides of the chassis is MP610. The reference designator for the screw that fastens the top inside corner of the power supply to the chassis is MP613. See table 7-11 for part numbers.

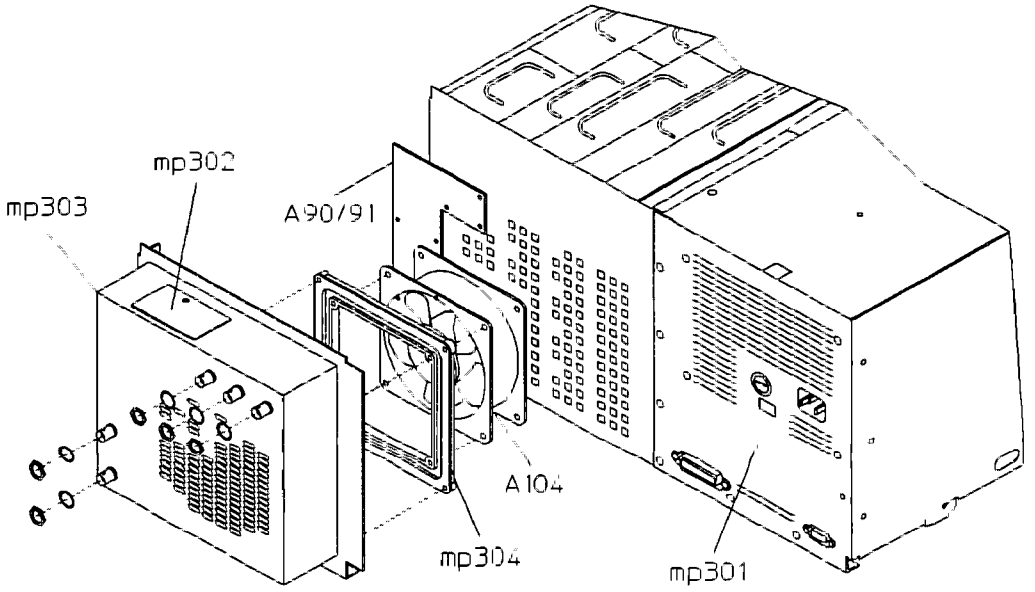


Figure 7-6. Reference Designators for Rear Panel Parts

Table 7-8. Rear Panel Parts

Ref.Des.	HP Part Number	CD	Qty	Description	Mfr. Code	Mfr. Part Number
MP301	03588-00225	2	1	SHTF PNL-REAR ALSK	28480	03588-00225
MP302	03588-04103	3	1	SHTF CVR-OVEN TWEAK ALSK	28480	03588-04103
MP303	03589-60201	1	1	SHTF ASSY-REAR PANEL ALSK	28480	03589-60201
MP304	1520-0247	2	1	MOLD FAN MOUNT	05030	FM-450-1
MP305	6960-0041	1	1	PLUG-HOLE FL-HD FOR .5-D-HOLE NYL	03480	2643 (BLACK)

Note

The reference designator for the screws that fasten the card nest to the chassis is MP608. The reference designator for the screws that fasten input housing (MP404) to the chassis is MP605. The reference designator for the screws that fasten the card nest bracket (MP402) to the chassis is MP607 and to the card nest is MP605. The reference designator for the nut that fastens the connector probe (MP413) to the input housing (MP404) is MP605.

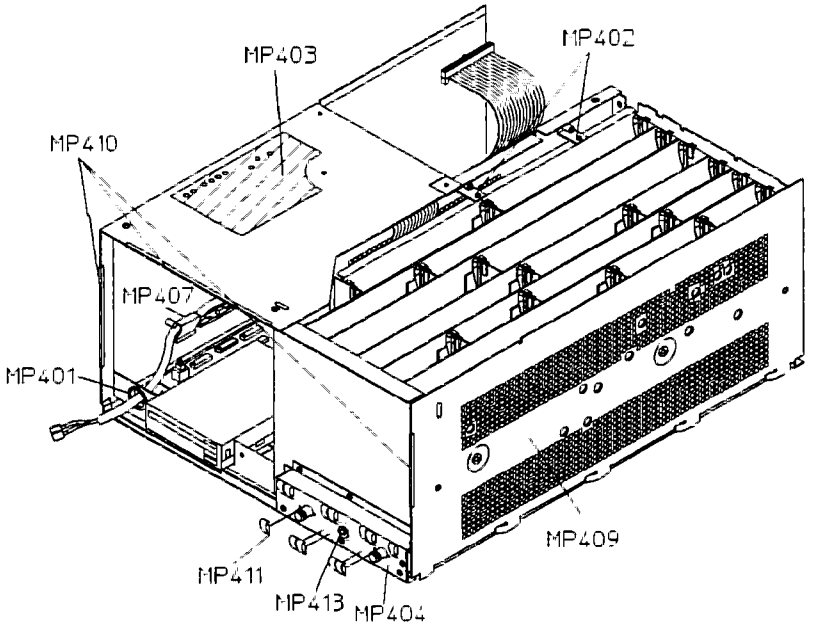


Figure 7-7. Reference Designators for Chassis Parts

Table 7-9. Chassis Parts

Ref.Des.	HP Part Number	CD	Qty	Description	Mfr. Code	Mfr. Part Number
MP401	0340-0881	7	1	GROMMET-SNAP BUSHING SHORTY	03480	2850 BLK (B-875-750)
MP402	03588-01210	7	2	STMP BRKT-CSS TO WALL AL	01642	–
MP403	03588-80401	4	1	LBL-DISPLAY 3588A	28480	03588-80401
MP404	03589-04101	2	1	SHTF HOUSING-INPUT AL	28480	03589-04101
MP405	0400-0002	2	1	GROMMET-RND .188-IN-ID .312-IN-GRV-OD	73734	1656
MP406	0400-0009	9	2	GROMMET-RND .125-IN-ID .25-IN-GRV-OD	28480	0400-0009
MP407	1400-0611	0	2	CLAMP-FL-CA 1-WD	76381	3484-1000
MP408	1400-1122	0	2	CLAMP-CABLE .187-DIA .735-WD NYL	34785	021-0188
MP409	35672-60211	2	1	SHTF WA-CHASSIS AL	28480	35672-60211
MP410	8160-0634	4	2	STMP BE/CU GROUND STRIP	30817	0097-0611-17
MP411	8160-0656	0	0	STMP RFI/EMI GASKET	30817	0097-500-17
MP412	8160-0683	3	3	STMP STRP-SPNG FLTR GRD	30817	0097-551-17-X
MP413	5060-0467	6	1	MOLD CONNECTOR PROBE	28480	5060-0467

Note

The reference designator for the washer between MP506 and the Motherboard (A99) is MP603. The reference designator for the washer between MP508 and MP507 is MP604. The reference designator for all screws used in the card nest is MP605. See table 7-11 for the part numbers.

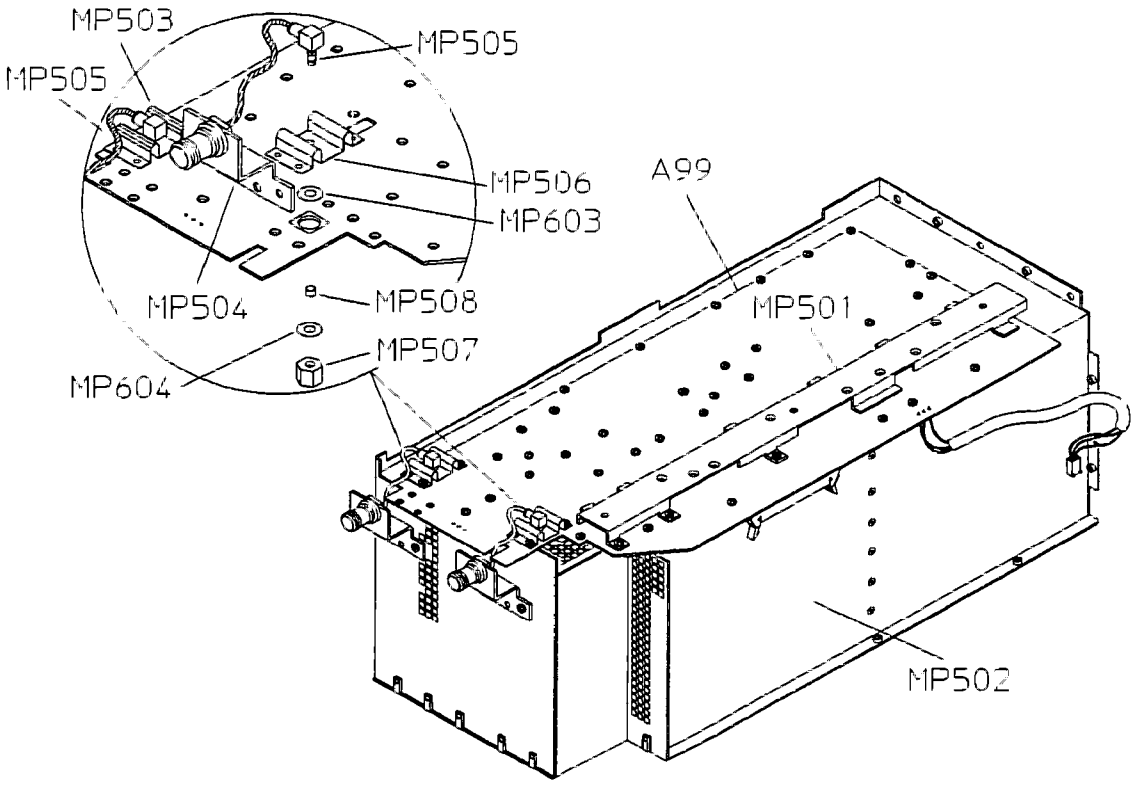


Figure 7-8. Reference Designators for Card Nest Parts

Table 7-10. Card Nest Parts

Ref.Des.	HP Part Number	CD	Qty	Description	Mfr. Code	Mfr. Part Number
MP501	03588-00219	4	1	SHTF BRKT-FOOT AL	28480	03588-00219
MP502	03588-60101	9	1	SHTF ASSY-CARD SUPPORT AL	28480	03588-60101
MP503	03589-01201	7	1	STMP BRKT-GROUND BECUTN	07466	–
MP504	03588-01206	1	2	SHTF BRKT-CONN AL	28480	03588-01206
MP505	03589-61660	8	2	CBL-ASM RGD MN/MSMB	09441	–
MP506	03588-01204	9	1	STMP BE/CU GROUND BRKT	07466	–
MP507	03588-23201	2	2	MCHD CONNECTOR GUIDE	28480	03588-23201
MP508	03588-21703	5	2	BSHG-BRASS 5MM ID 3.2MM THK	05791	–

Table 7-11. Screws, Washers, and Nuts

Ref.Des.	HP Part Number	CD	Qty	Description	Mfr. Code	Mfr. Part Number
MP603	03588-41701	5	2	WSHR-SHLDR 6.6MM ID TEFLON	05791	–
MP604	03588-41702	6	2	WSHR-FLAT 6.6MM ID .7TK TEFLON	05791	–
MP605	0515-0372	2	146	SCREW-MACHINE ASSEMPLY M3 X 0.5 8MM-LG	05610	–
MP606	0515-0372	2	22	SCREW-MACHINE ASSEMPLY M3 X 0.5 8MM-LG	05610	–
MP607	0515-0375	5	2	SCREW-MACHINE ASSEMPLY M3 X 0.5 16MM-LG	05610	–
MP608	0515-0433	6	5	SCREW-MACHINE ASSEMPLY M4 X 0.7 8MM-LG	05610	–
MP609	0515-0456	3	7	SCREW-MACHINE ASSEMPLY M4 X 0.7 20MM-LG	05610	–
MP610	0515-1946	8	1	SCR-MCH M3.5 6MMLG FHTX SST	77250	–
MP611	0515-1946	8	10	SCR-MCH M3.5 6MMLG FHTX SST	77250	–
MP613	0515-2033	6	1	SCR-MCH M3.0 10MMLG FHTX SST	77250	–
MP614	0535-0031	2	4	NUT-HEX W/LKWR M3 X 0.5 2.4MM-THK	28480	0535-0031
MP615	0535-0043	6	5	NUT-HEX W/LKWR M4 X 0.7 3.2MM-THK	28480	934KEPS-M4
MP616	0570-1378	6	14	SCR-TPG 0-50 .20LG FHPH STLZ	83486	276-000-0000-7N
MP617	0624-0708	9	15	SCR-MCH 3-28 .31LG SLPH STZN	83486	–
MP618	2190-0099	2	4	WASHER-LK INTL T 7/16 IN .472-IN-ID	73734	–
MP619	2950-0035	8	4	NUT-HEX-DBL-CHAM 15/32-32-THD	28480	2950-0035
MP620	2950-0154	2	2	NUT-HEX-DBL-CHAM 1/2-28-THD .078-IN-THK	28480	2950-0154
MP622	3050-0604	0	4	WASHER-FL MTLC 7/16 IN .5-IN-ID	86928	5710-94-16

Table 7-12. Miscellaneous Parts

Ref.Des.	HP Part Number	CD	Qty	Description	Mfr. Code	Mfr. Part Number
A72F300	2110-0665	0	1	FUSE 1A 125V NTD .28X.096	75915	R251001T1
A87B402	1420-0336	8	1	BATTERY	55002	T06/46
	5061-2819	8	1	BLANK PLASTIC DISK FOR TRANSPORTATION	28480	5061-2819
	2110-0056	3	1	6A 250V FAST ACTING FUSE	75915	312 006
	2110-0003	0	1	3A 250V FAST ACTING FUSE	75915	312 003
	6010-1147	7	1	HP FRENCH GRAY TOUCH-UP PAINT	28480	6010-1147

HP 35689A/B Reference Designators and Part Numbers

To order a part in tables 7-13 through 7-20, quote the Hewlett-Packard part number, the check digit (CD), indicate the quantity required, and address the order to the nearest Hewlett-Packard sales and service office. The check digit verifies that an order has been transmitted correctly, ensuring accurate and timely processing of the order. The first time a part is listed in the table, the quantity column lists the total quantity of the part used in the analyzer. See table 7-2 for a table listing the manufacturers' code numbers and the corresponding names and addresses.

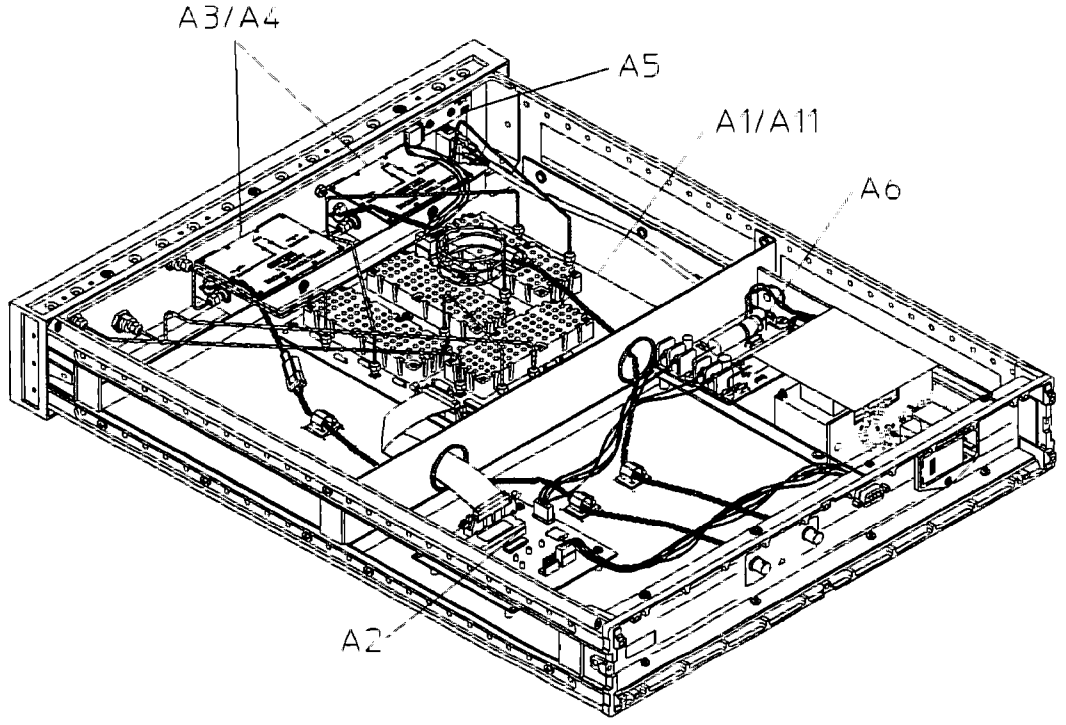


Figure 7-9. Reference Designators for Assemblies

Table 7-13. Assemblies

Ref.Des.	HP Part Number	CD	Qty	Description	Mfr. Code	Mfr. Part Number
A1	35689-69501	4	1	EXCHANGE PC ASSY 50 OHM RF	28480	35689-69501
A2	35689-66502	5	1	PC ASSY - CONTROL BOARD	28480	35689-66502
A3	35677-63502	5	2	DIR BRIDGE 50 OHM ASSY	28480	35677-63502
A4	35677-63504	7	2	DIR BRIDGE 75 OHM ASSY	28480	35677-63504
A5	35677-66505	4	1	LED BRD ASSY	28480	35677-66505
A6	35689-67501	6	1	POWER SUPPLY +5VDC/+15VDC	L3095	–
A11	35689-69511	6	1	EXCHANGE PC ASSY - 75 OHM RF	28480	35689-69511

After replacing an assembly, see "What to Do After Replacing an HP 35689A/B Assembly" in chapter 6.

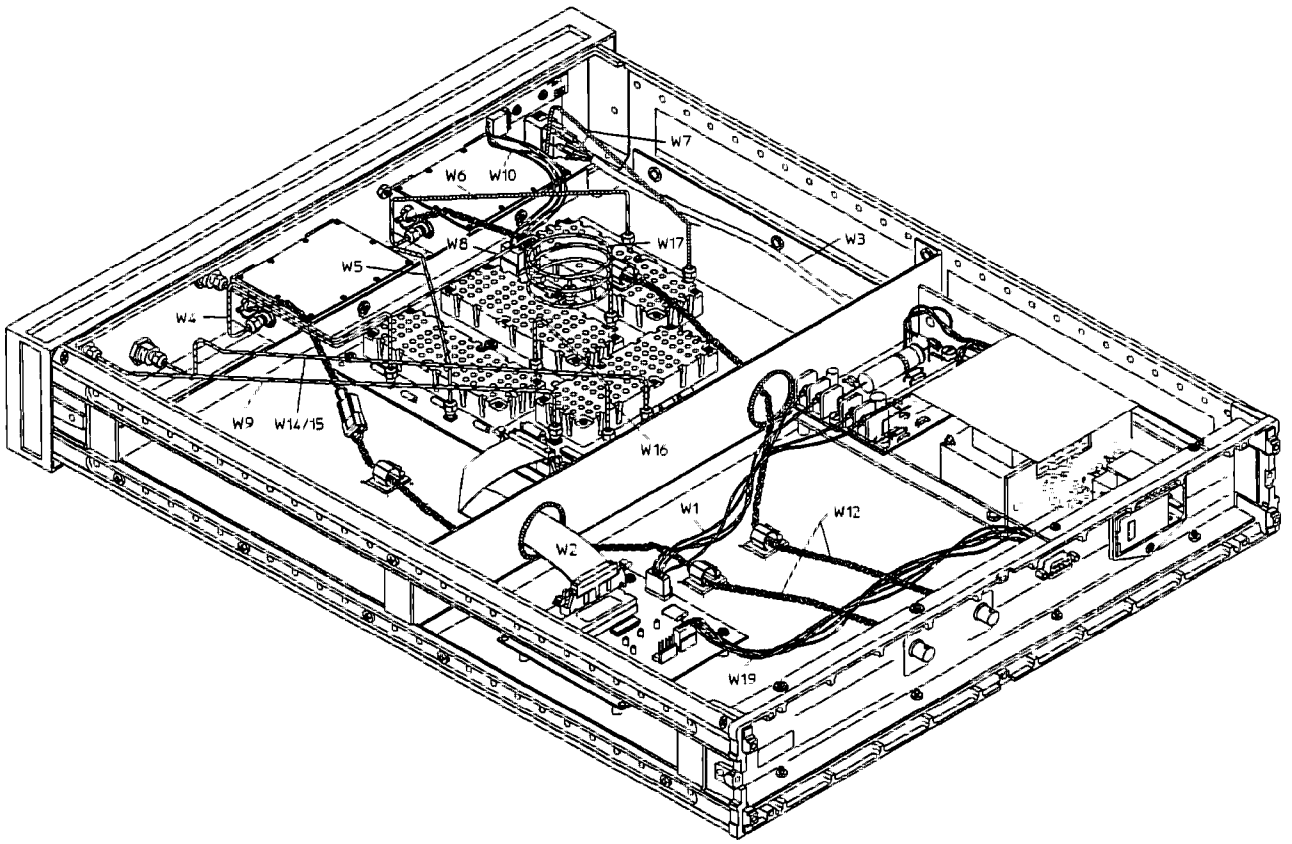


Figure 7-10. Reference Designators for Cables

Table 7-14. Cables

Ref.Des.	HP Part Number	CD	Qty	Description	Mfr. Code	Mfr. Part Number
W1	35689-61601	5	1	CBL-ASM FHSG/RING 230MM LG ML	28480	35689-61601
W2	35689-61602	6	1	CBL-ASM RBN FHSG/FHSG 225 MMLG	76381	–
W3	35689-61603	7	1	CBL-ASM DSC LINE FILTER	L2276	–
W4	35689-61604	8	1	CBL-ASM RGD MSMA/MSMA 235MM	00848	–
W5	35689-61605	9	1	CBL-ASM RGD MSMA/MSMA 235MM	00848	–
W6	35689-61606	0	1	CBL-ASM RGD MSMA/MSMA 235MM	00848	–
W7	35689-61607	1	1	CBL-ASM RGD MSMA/MSMA 235MM	00848	–
W8	35689-61608	2	1	CBL-ASM RGD MSMA/MSMA 270MM	00848	–
W9	35689-61609	3	1	CBL-ASM RGD MSMA/MSMA 287MM	00848	–
W10	35677-61610	2	1	CBL-ASM DSC fHSG/fHSG 180MM ML	28480	35677-61610
W12	35677-61612	4	2	CBL-ASM DSC FHSG/ STP 490MM ML	L2276	–
W14	35689-61614	0	1	CBL-ASM RGD MSMA/MSMA 338MM for HP 35689A	00848	–
W15	35689-61615	1	1	CBL-ASM RGD MSMA/MSMA 338MM for HP 35689B	00848	–
W16	35689-61616	2	1	CBL-ASM RGD MSMA/MSMA 145MM	00848	–
W17	35689-61617	3	1	CBL-RGD FSMA/FSMA	28480	35689-61617
W19	35689-61610	6	1	CBL-ASM FHSG/FDSB 270MM LG ML	28480	35689-61610

Note

The reference designator for the screws that fasten the handles to the chassis is MP605. The reference designator for the screws that fasten the top and bottom covers to the chassis is MP602. See table 7-19 for the part number.

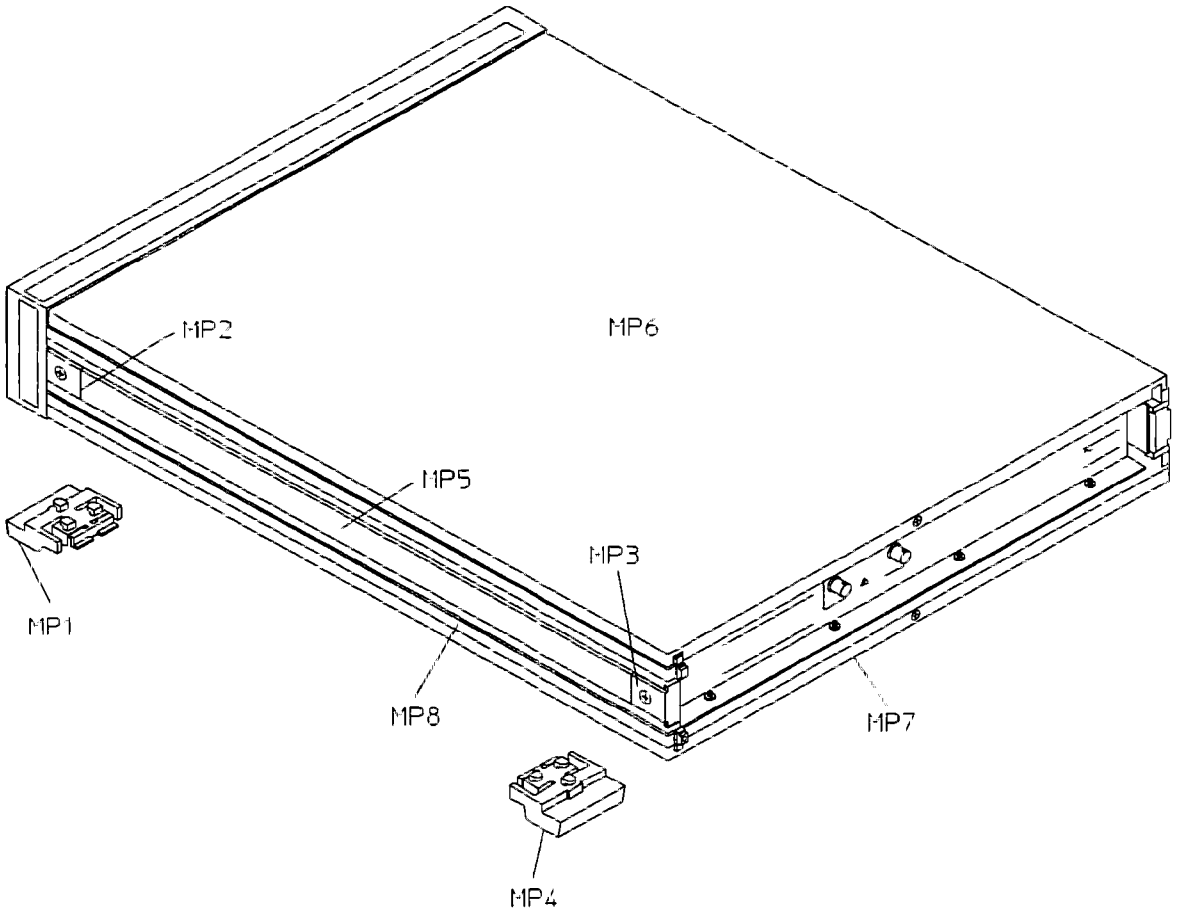


Figure 7-11. Reference Designators for Instrument Covers and Handles

Table 7-15. Instrument Covers and Handles

Ref.Des.	HP Part Number	CD	Qty	Description	Mfr. Code	Mfr. Part Number
MP1	5041-8801	8	2	MOLD FOOTII+	28480	5041-8801
MP2	5041-8819	8	2	MOLD STRP HDL CAP FRTII+	28480	5041-8819
MP3	5041-8820	1	2	MOLD STRP HDL CAP RRII+	28480	5041-8820
MP4	5041-8822	3	2	MOLD FOOT-NON SKIDII+	28480	5041-8822
MP5	5062-3705	5	2	SHTF ASSY-SD HNDL 574D II+SSTP	28480	5062-3705
MP6	5062-3736	2	1	SHTF CVR-TOP FM574D II+ALV	28480	5062-3736
MP7	5062-3748	6	1	SHTF CVR-BTM FM574D II+ALV	28480	5062-3748
MP8	5062-3777	1	2	SHTF CVR-SD RS 88H574D II+ALV	28480	5062-3777

Note

The reference designator for the screws that fasten the directional bridges to the sub-panel (MP203) is MP606. The reference designator for the nuts that fasten the dress plate (MP205) to the sub-panel (MP203) is MP609. The reference designator for the screws that fasten A5 to the front panel is MP602. The reference designator for the screws that fasten the front panel to the frame is MP606. See table 7-19 for the part number. The part number for the washers used with the front panel connector (MP201 and MP208) is HP 2190-0039. The part number for the nuts used with the front panel connector (MP201 and MP208) is HP 0590-0038.

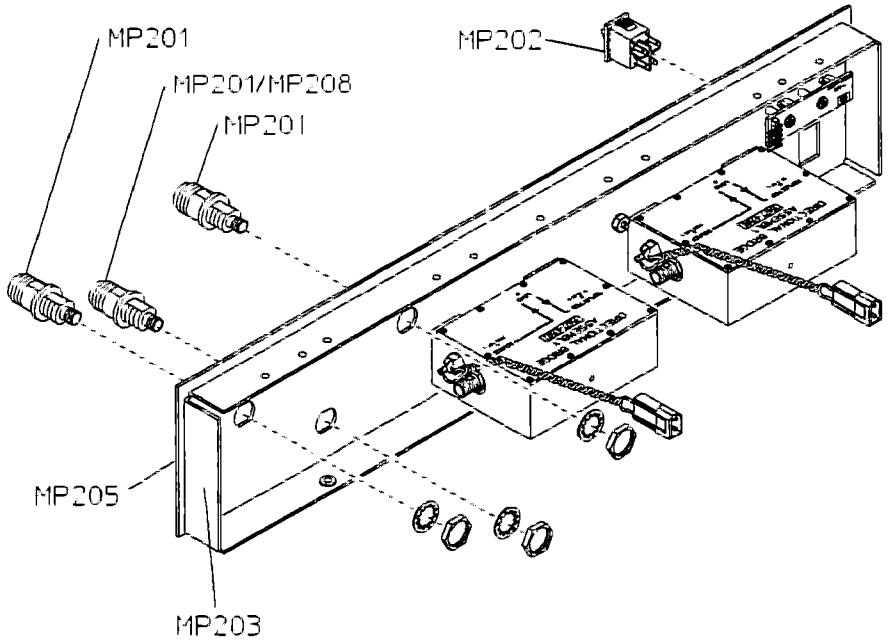


Figure 7-12. Reference Designators for Front Panel Parts

Table 7-16. Front Panel Parts

Ref.Des.	HP Part Number	CD	Qty	Description	Mfr. Code	Mfr. Part Number
MP201	1250-1811	5	3	ADAPTER-COAX STR F-N F-SMA for HP 35689A	06860	34N-SMA-50-2
MP201	1250-1811	5	2	ADAPTER-COAX STR F-N F-SMA for HP 35689B	06860	34N-SMA-50-2
MP202	3101-3014	1	1	SW-RKR	09328	WI32/217MZ
MP203	35689-00201	3	1	SHTF SUBPANEL AL	28480	35689-00201
MP204	35689-34301	5	1	PLT-NAME "35689A"	06363	–
MP204	35689-34302	6	1	PLT-NAME "35689B"	06363	–
MP205	35689-64301	8	1	PNL-FRT DRESS "35689A"	22670	–
MP205	35689-64302	9	1	PNL-FRT DRESS "35689B"	22670	–
MP206	5001-0538	8	2	TRIM-FRT FRM SD88 1H II+VYNL	28480	5001-0538
MP207	5041-8802	9	1	MOLD TRM-TOP FMII+	28480	5041-8802
MP208	1250-2351	0	1	CON-N/SMA ADAPTER 75 OHM for HP 35689B	06860	–
MP209	35689-24301	4	1	WSHR-CONNECTOR 75 OHM for HP 35689B	06860	–

Note

The reference designators for the nuts and washers that fasten the BNC connectors (MP302) to the rear panel are MP610 and MP611. The reference designator for the nuts that fasten the standoff (MP301) to the rear panel is MP609. The reference designators for the screws and nuts that fasten the line filter (W3) to the rear panel are MP609 and MP607. The reference designator for the screws that fasten the rear panel to the frame is MP602. See table 7-19 for the part numbers.

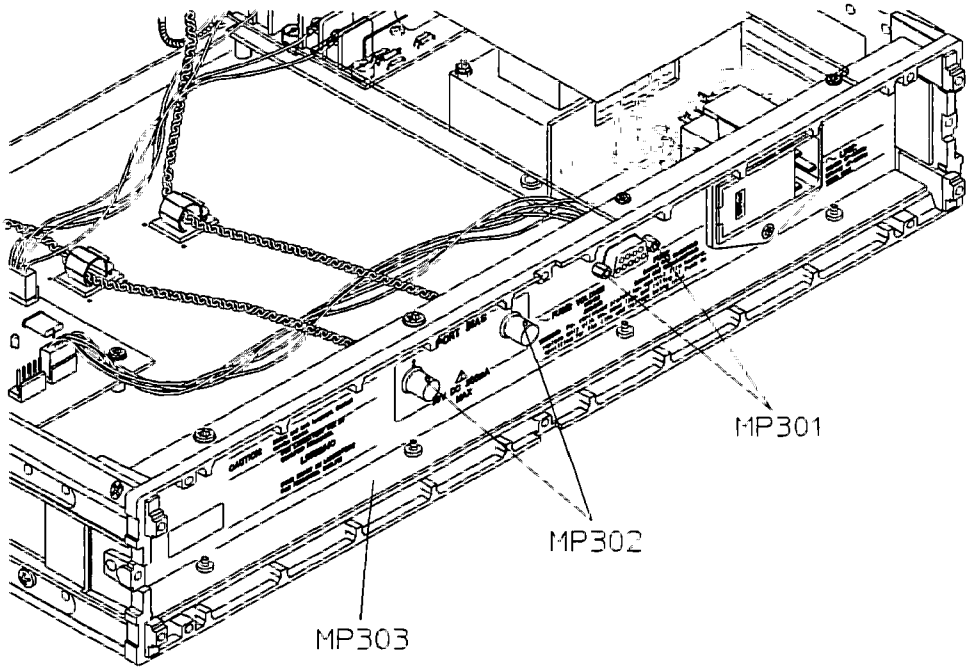


Figure 7-13. Reference Designators for Rear Panel Parts

Table 7-17. Rear Panel Parts

Ref.Des.	HP Part Number	CD	Qty	Description	Mfr. Code	Mfr. Part Number
MP301	0380-1689	9	2	STANDOFF-HEX 4.75-MM-LG M3.0 X 0.5-THD	05791	–
MP302	1250-0083	1	2	CONNECTOR-RF BNC FEM SGL-HOLE-FR 50-OHM	90949	31-221-1020
MP303	35689-00202	4	1	SHTF PANEL-REAR ALSK	28480	35689-00202

Note

The reference designator for the screws that fasten the struts (MP406) to the front and rear frames is MP608. The reference designator for the screws that fasten A6 to the deck is MP604. The reference designator for the screws that fasten the struts to the deck is MP603. The reference designator for the nut that fasten the ground wire to the rear panel is MP609. The reference designator for the screws that fasten the power supply shield (MP405) to the chassis is MP601. The reference designators for the screws and washers that fasten A3/A4 to the deck are MP602 and MP612. The reference designator for the screws that fasten A1/A11 and A2 to the deck is MP602. See table 7-19 for the part numbers.

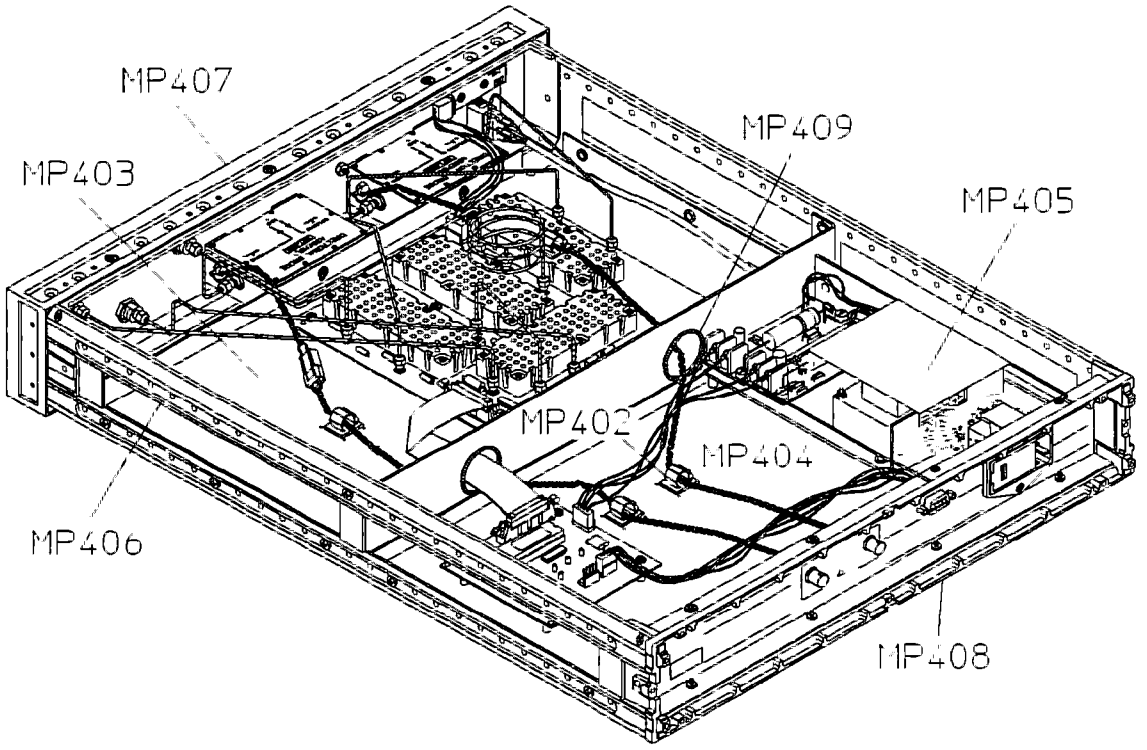


Figure 7-14. Reference Designators for Chassis Parts

Table 7-18. Chassis Parts

Ref.Des.	HP Part Number	CD	Qty	Description	Mfr. Code	Mfr. Part Number
MP401	0403-0179	0	2	BUMPER FOOT-ADH MTG	76381	SJ-5012 (BLACK)
MP402	1400-1122	0	4	CLAMP-CABLE .187-DIA .735-WD NYL	34785	021-0188
MP403	35689-00101	2	1	SHTF DECK-MOUNTING AL	28480	35689-00101
MP404	35689-00102	3	1	SHTF DECK-MOUNTING AL	28480	35689-00102
MP405	35689-64101	6	1	ASSY SHIELD	28480	35689-64101
MP406	5021-5833	8	2	CSTG STRT-SD88H 574D II AL	28480	5021-5833
MP407	5041-5853	4	1	CSTG FRM-FRT FMM 88.1H II + ALPT	28480	5041-5853
MP408	5021-5802	1	1	CSTG FRM-RRFM88.1H II AL	28480	5021-5802
MP409	0400-0082	8	2	GROMMET-CHAN NCH .09-IN-GRV-WD	12324	GSNY-085-9

Table 7-19. Screws, Washers, and Nuts

Ref.Des.	HP Part Number	CD	Qty	Description	Mfr. Code	Mfr. Part Number
MP601	0515-0372	2	2	SCREW-MACHINE ASSEMPLY M3 X 0.5 8MM- LG	05610	–
MP602	0515-0430	3	20	SCREW-MACHINE ASSEMPLY M3 X 0.5 6MM-LG	05610	–
MP603	0515-0433	6	12	SCREW-MACHINE ASSEMPLY M4 X 0.7 8MM-LG	05610	–
MP604	0515-0686	1	4	SCREW-MACH M4 X 0.7 20MM-LG PAN-HD	05610	–
MP605	0515-1132	4	4	SCREW-MACH M5 X 0.8 10MM-LG	77250	–
MP606	0515-1946	8	14	SCR-MCH M3.5 6MMLG FHTX SST	77250	–
MP607	0515-2033	6	2	SCR-MCH M3.0 10MMLG FHTX SST	77250	–
MP608	0515-2086	9	8	SCR-SPC M4.07MMLG FHTX SST	77250	–
MP609	0535-0031	2	7	NUT-HEX W/LKWR M3 X 0.5 2.4MM-THK	28480	–
MP610	2190-0016	3	2	WASHER-LK INTL T 3/8 IN .377-IN-ID	73734	–
MP611	2950-0043	8	2	NUT-HEX-DBL-CHAM 3/8-32-THD .094-IN-THK	28480	–
MP612	3050-0105	6	2	WASHER-FL MTLC NO. 4 .125-IN-ID	78471	–

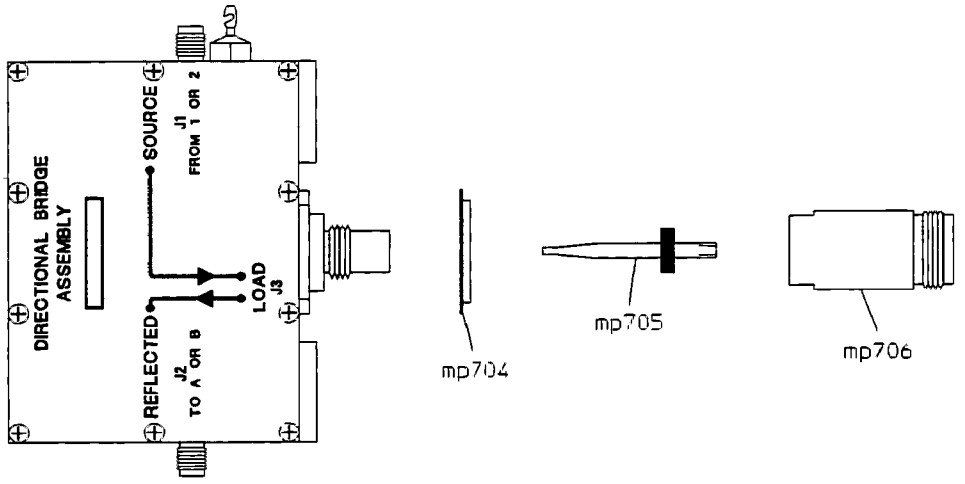


Figure 7-15. Reference Designators for Directional Bridges

Table 7-20. Miscellaneous Parts

Ref.Des.	HP Part Number	CD	Qty	Description	Mfr. Code	Mfr. Part Number
MP702	0890-0870	9	0	TUBING-HS .093-D/.046-RCVD .02-WALL	06090	VERSAFIT-3/32-CLEAR
MP703	0400-0226	2	0	GROMMET-CHAN .052-IN-GRV-WD	12324	GRNY-052-9
MP704	5021-1744	2	2	DRESS RING	28480	5021-1744
MP705	35677-67601	3	2	50 OHM CENTER CONDUCTOR	28480	35677-67601
MP705	35677-67602	4	2	75 OHM CENTER CONDUCTOR	28480	35677-67602
MP706	1250-0914	7	2	BODY: RF CONNECTOR	28480	1250-0914
	2110-0001	8	1	1A 250VAC NORMAL BLOW FUSE	75915	–
	2110-0012	1	1	500mA 250VAC NORMAL BLOW FUSE	75915	–
	6010-1147	7	1	HP FRENCH GRAY TOUCH-UP PAINT	28480	6010-1147

8

Circuit Descriptions

Introduction

This first part of this chapter contains the overall instrument description and individual assembly descriptions for the HP 3589A Spectrum/Network Analyzer. The last part of this chapter contains the overall instrument description and individual assembly descriptions for the HP 35689A/B S-Parameter Test Set. For signal descriptions and information on voltage and signal distribution, see chapter 9, "Voltages and Signals."

HP 3589A Spectrum/Network Analyzer

The HP 3589A Spectrum/Network Analyzer is a high performance, 10 Hz to 150 MHz, synthesized spectrum/network analyzer offering swept spectrum, narrow-band zoom, and vector network measurements. Swept spectrum mode uses digital IF filters that allow increased measurement speed (up to four times faster than conventional swept-tuned analyzers for comparable measurements) with no additional amplitude error or resolution loss. Narrow-band zoom uses an implementation of the Fast Fourier Transform to provide even faster measurements (up to 350 times faster than conventional swept-tuned analyzers for comparable measurements) with even greater resolving power. Narrow-band zoom mode can be used for spans of 40 kHz and less. Vector network mode provides complete frequency-domain characterization. With the addition of the HP 35689A/B S-Parameter Test Set, the HP 3589A can do complete one-port or two-port vector network analysis.

The HP 3589A Spectrum/Network Analyzer has a built-in source with programmable amplitude. Measurements can be saved using the 3.5-inch flexible disk drive or non-volatile memory. Plots and prints of the measurements can be made directly to HP-IB printers and plotters. Options include a high stability frequency reference, expanded memory, time-gated spectrum analysis, HP Instrument BASIC programming language (IBASIC), and PC-compatible keyboards.

Overall Block Diagram

Figure 8-1 shows the overall block diagram for the analyzer. Each block in the diagram represents a functional block in the instrument. The assembly (or assemblies) that performs the function is listed in the block.

The **Input/Conversion** and **IF/ADC** together function as the analyzer's receiver. Input/Conversion prepares the input signal for analog-to-digital conversion. Figure 8-2 shows the signal flow to and from each assembly in the Input/Conversion block. The IF further prepares the input signal and the ADC converts the signal from analog to digital. Figure 8-3 shows the signal flow to and from each assembly in the IF/ADC block.

The **Sum/Step Loop** and **Fractional-N** together function as the analyzer's local oscillator. The Sum/Step Loop provides the Fractional-N, Input/Conversion, and Source blocks with a signal that can sweep from 310.1875 to 460.1875 MHz. Figure 8-4 shows the signal flow to and from each assembly in the Sum/Step Loop block. The Fractional-N provides the Sum/Step Loop block with a signal that can sweep from 3 to 11 MHz and the single loop control voltage. Figure 8-5 shows the signal flow to and from each assembly in the Fractional-N block.

The **Frequency Reference** provides both high and low frequency reference signals, a sweep synchronization signal, a trigger signal, a precision amplitude signal for calibration, and control signals for gated-sweep measurements. Figure 8-6 shows the signal flow to and from each assembly in the Frequency Reference block.

The **Source** provides the tracking source output for the analyzer. Its frequency tracks the tuned receiver frequency, providing an output signal that can sweep from 10 Hz to 150 MHz. Its amplitude can be adjusted from +15 to –54.9 dBm. The Source also provides the normalization signal to the Input/Conversion block and the calibration signal to the Frequency Reference block. Figure 8-7 shows the signal flow to and from each assembly in the Source block.

The optional **Oven** provides a stable 10 MHz frequency reference. A BNC-to-BNC jumper from OVEN REF OUT to EXT REF IN (on the rear panel) connects this signal to the Frequency Reference block.

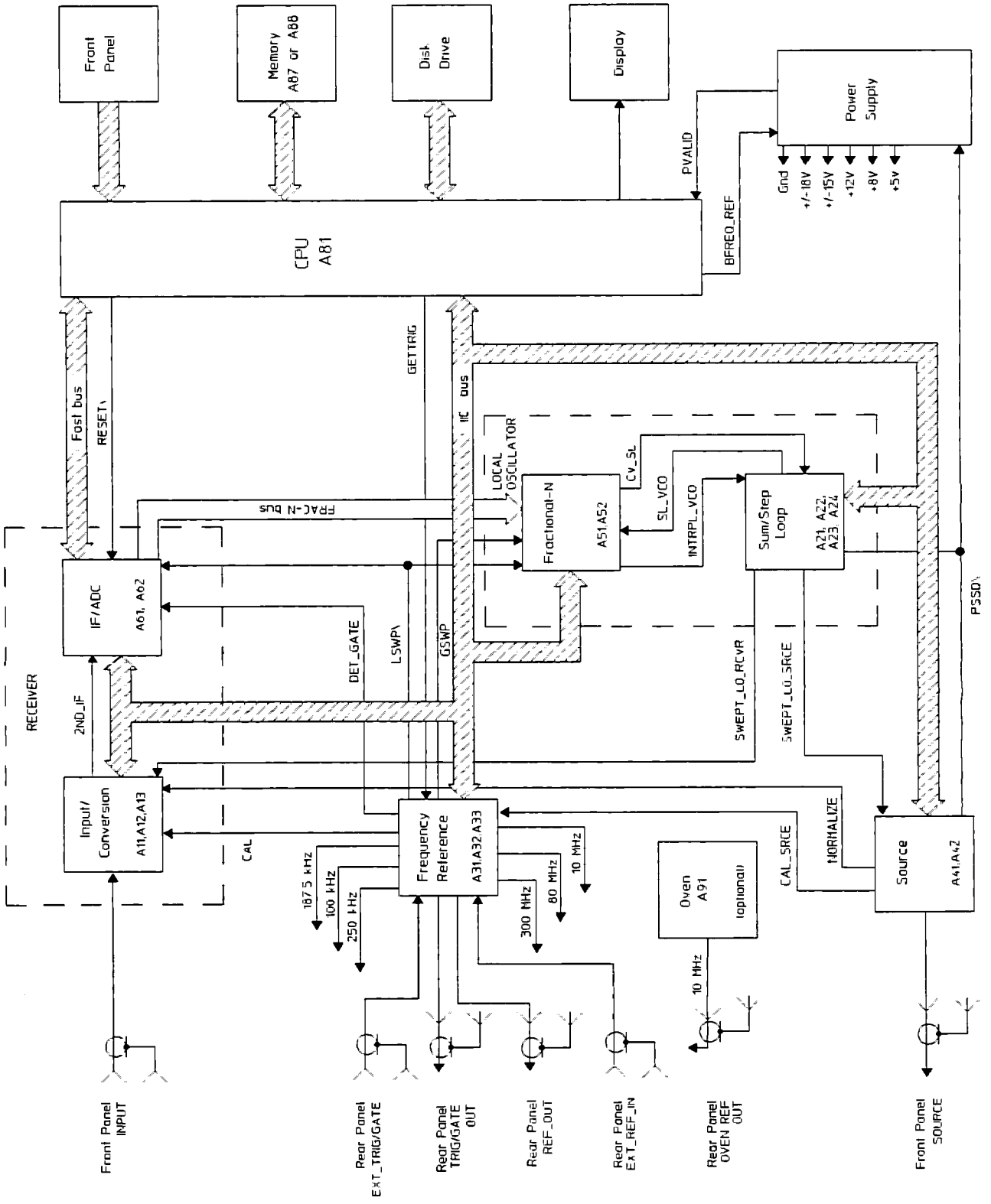


Figure 8-1. Overall Block Diagram

The **CPU** controls the analyzer. The following is a partial list of the operations it performs:

- Configures the assemblies
- Controls the Disk Drive assembly
- Controls the Display assembly
- Controls the HP-IB interface
- Initiates the power-up sequence and calibration routine
- Processes digital data from the ADC/Digital Filter assembly
- Computes the Fast Fourier Transform (FFT)
- Monitors for a front panel keystroke
- Monitors the assemblies for overloads or other error conditions
- Runs the self tests

The **Disk Drive** stores and retrieves information on 3.5-inch flexible disks.

The **Memory** contains RAM, NVRAM, ROM, and the battery-backed real time clock for the CPU.

The **Display** offers a view of the processed data. It is controlled by the CPU. See the description of the Display Controller for the "A81 CPU" later in this chapter for further details.

The **Front Panel** allows interaction with the analyzer. It consists of hardkeys, softkeys, an RPG, a DIN external keyboard connector, an Inter-IC (IIC) interface, and a plastic diffuser-screen for the Display.

The **Power Supply** provides the dc voltages shown in figure 8-1. See "Power Supply Voltage Distribution" in chapter 9 for further information.

Assemblies

The HP 3589A Spectrum/Network Analyzer consists of the assemblies shown below.

- A11 Input
- A12 First Conversion
- A13 Second Conversion
- A21 Sum VCO
- A22 Sum Phase Detector
- A23 Step Phase Detector
- A24 Step VCO
- A31 Reference/Calibrator
- A32 300 MHz
- A33 Trigger
- A41 Source Amplifier
- A42 Source Conversion
- A51 Interpolation VCO
- A52 Fractional-N
- A61 IF
- A62 ADC/Digital Filter
- A81 CPU
- A87 Memory
- A88 Expanded Memory (optional)
- A90 Fan Power
- A91 Fan Power/Oven (optional)
- A99 Motherboard
- Power Supply
- Disk Drive
- Display
- Front Panel

Note

In this chapter, the block diagrams show the connector numbers for signals routed through RF cables. The block diagrams do *not* show connector numbers for signals routed through the Motherboard assembly.

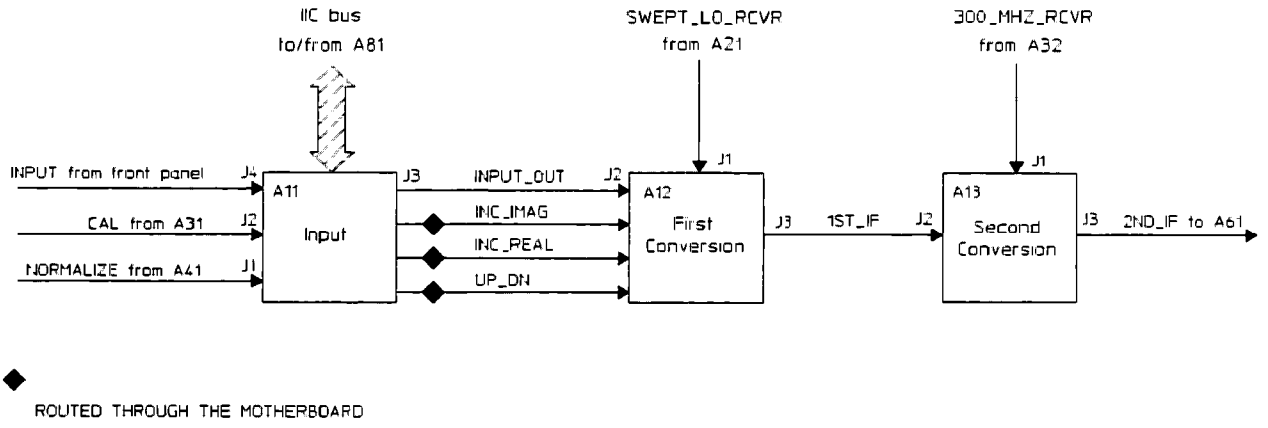


Figure 8-2. Input Conversion Block Diagram

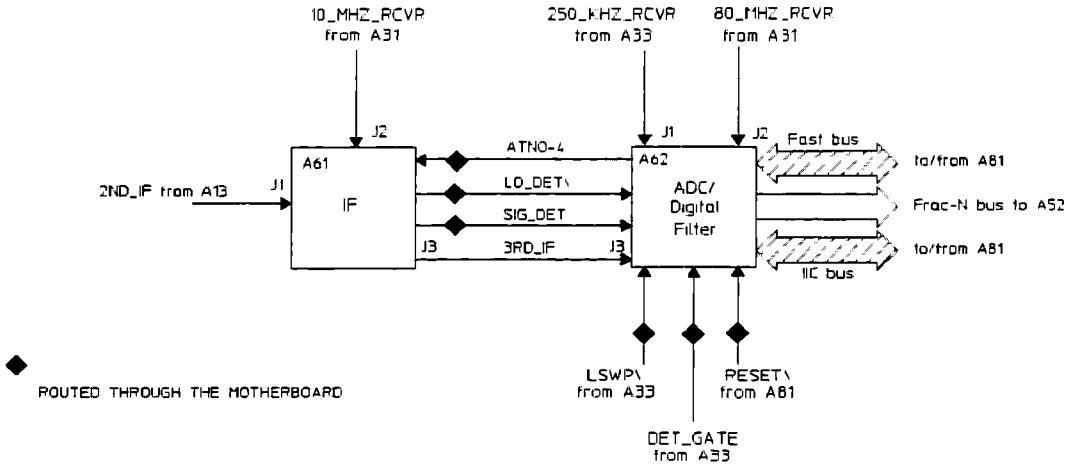


Figure 8-3. IF/ADC Block Diagram

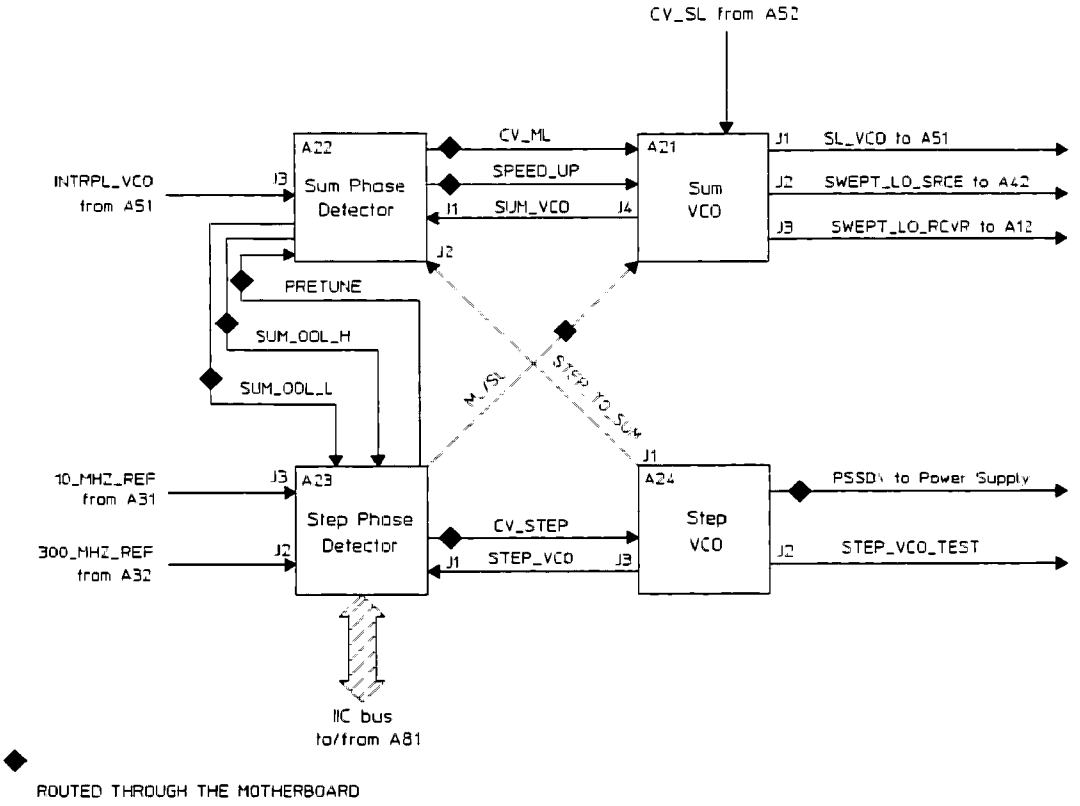


Figure 8-4. Sum and Step Loop Block Diagram

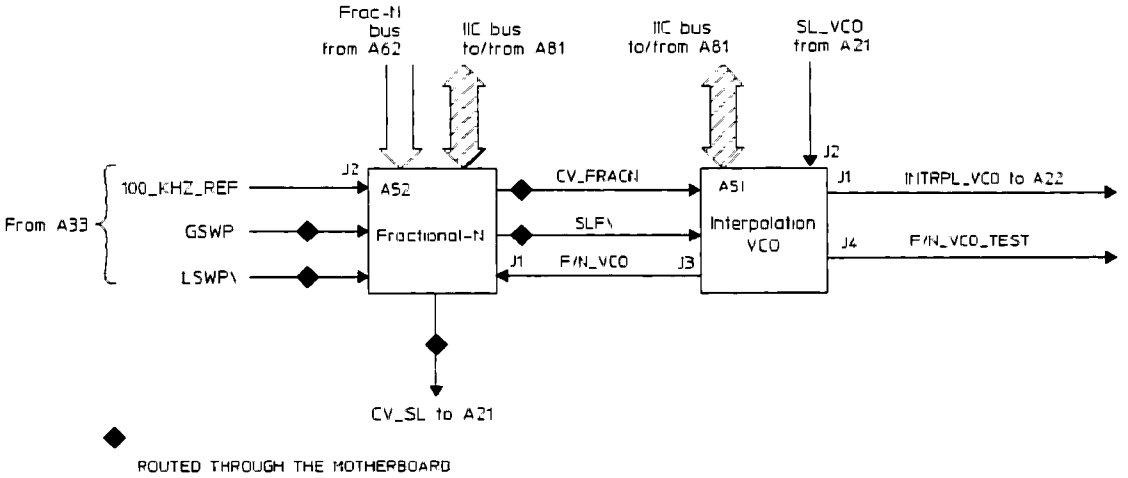


Figure 8-5. Fractional-N Block Diagram

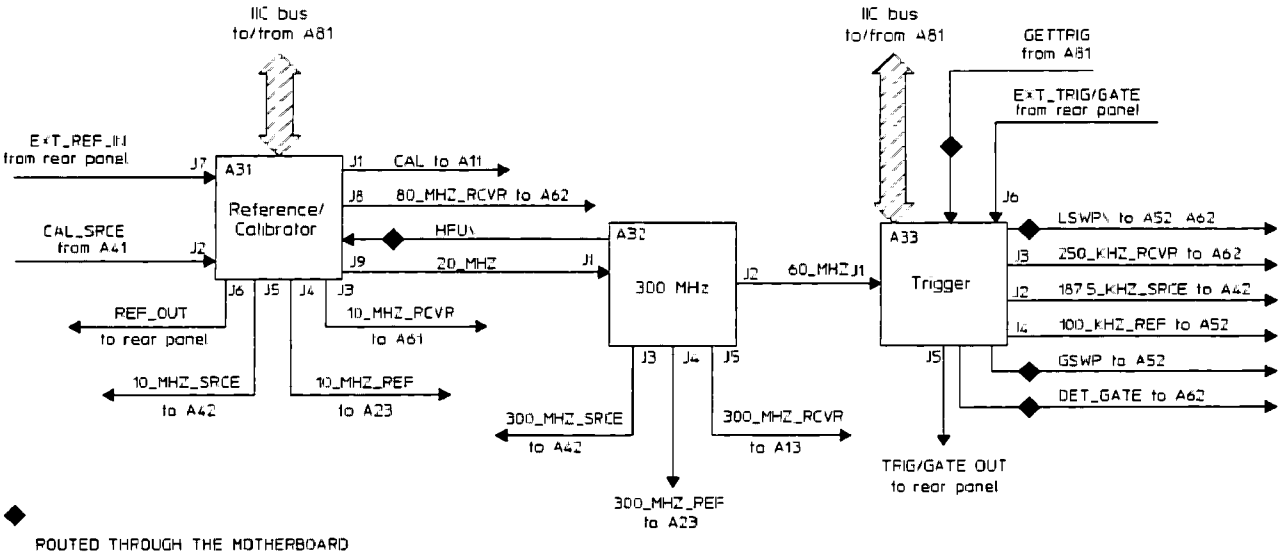


Figure 8-6. Frequency Reference Block Diagram

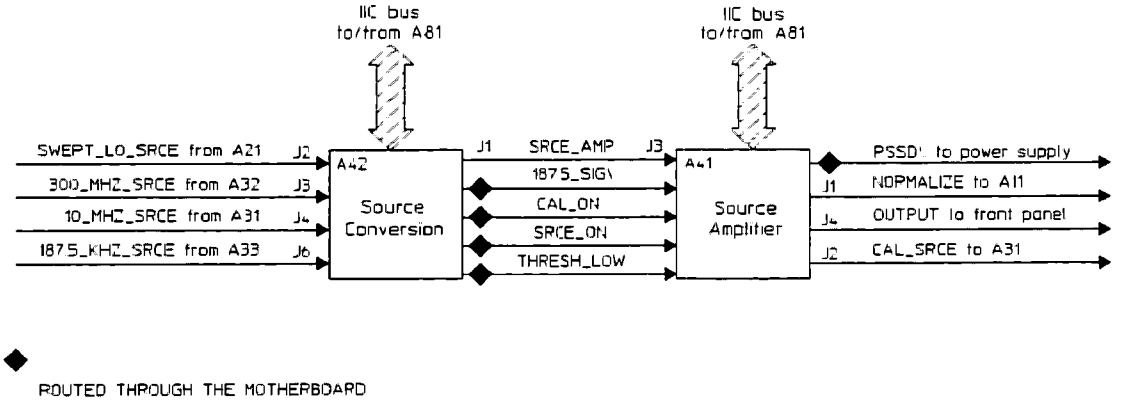


Figure 8-7. Source Block Diagram

A11 Input

The Input assembly is the first of five assemblies that condition the input signal before it is sent to the CPU assembly in digital form. The input signal can be a signal (10 Hz to 150 MHz) that is connected to the front-panel input connector, the normalization signal from the Source Amplifier assembly, or the calibration signal from the Reference/Calibrator assembly. Figure 8-8 shows the Input assembly's block diagram.

The **Input Switching** circuit selects either the signal connected to the front-panel input connector, the calibration signal from the Reference/Calibrator assembly, or the normalization signal from the Source Amplifier assembly. It then routes the selected signal to either the 50Ω or the 1 MΩ input impedance path.

The **1M Ohm Buffer** provides a 1 MΩ impedance path for the input signal. This circuit attenuates the input signal using one 10 dB and two 20 dB attenuator pads. This circuit also contains a flatness service adjustment and a 1MΩ input amplifier. Its maximum input level to the attenuator is +7 dBV and its output impedance is 50Ω.

The **50 Ohm Attenuator** provides a 50Ω impedance path for the input signal. This circuit attenuates the input signal using one 10 dB and two 20 dB attenuator pads. Its maximum input level is +20 dBm and its output impedance is 50Ω.

The **Input Amplifier** increases the input signal's amplitude by 5 dB and provides 50Ω output impedance to both the 150 MHz Low Pass Filter and the Autorange Detector.

The **150 MHz Low Pass Filter** attenuates signals greater than 150 MHz.

The **Autorange Detection** circuit compares the input signal to a service adjustable "range up" and "range down" threshold. The CPU assembly monitors the result of this comparison and then sets the 50Ω attenuators so the largest signal amplitude is at a level that displays maximum dynamic range.

The **Overload Protection** circuit monitors the 50Ω impedance path. If an overload occurs, this circuit causes the relays in Input Switching to disconnect the input signal.

The **IIC Interface** provides the interface between the CPU assembly and the Input assembly, and it provides the control lines that null local oscillator feedthrough on the First Conversion assembly. It also interrupts the CPU assembly if a range up, range down, or overload condition is detected.

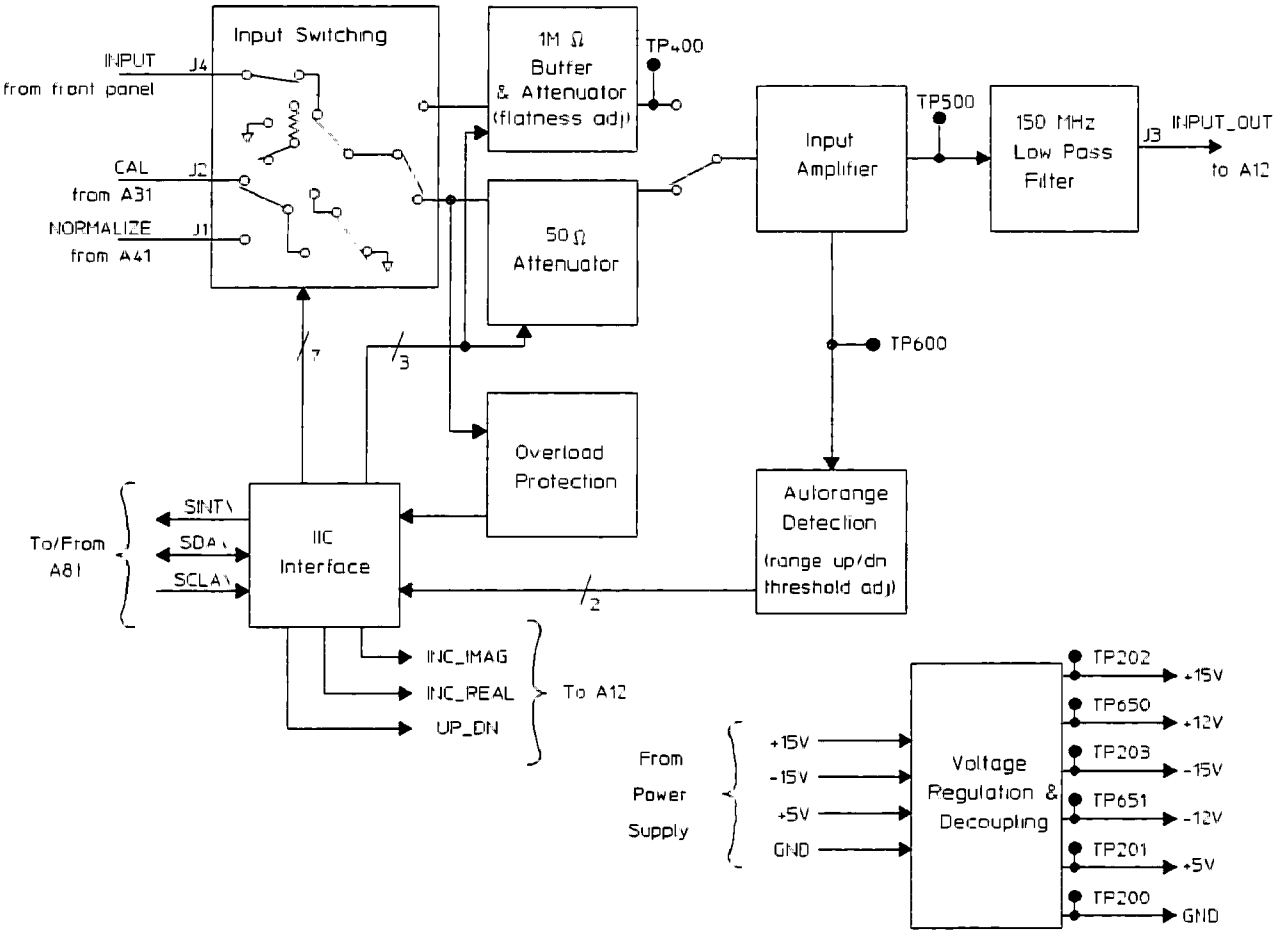


Figure 8-8. A11 Input Block Diagram

A12 First Conversion

The First Conversion assembly is the second of five assemblies that condition the input signal. This assembly mixes the swept LO signal with the signal from the Input assembly. The resulting 310.1875 MHz signal is routed to the Second Conversion assembly. Figure 8-9 shows the First Conversion assembly's block diagram.

The **First Conversion Mixer/Driver** first increases the amplitude of the swept LO signal (310.1875 to 460.1875 MHz) to +17 dBm at the mixer input. It then mixes the swept signal with the input signal. At the output of this circuit, a bandpass diplexer attenuates signals away from the 310.1875 MHz IF signal.

The **LO Feedthrough Cancellation** circuit generates a signal that reduces LO feedthrough. During calibration, LO feedthrough is measured and the information is sent to the CPU assembly. The CPU assembly then adjusts the amplitude and phase of the LO feedthrough cancellation signal using three control lines from the Input assembly.

The **First IF Amplifier** increases the amplitude of the 310.1875 MHz signal by approximately 15 dB. Between this circuit's two gain stages, it adds the LO feedthrough cancellation signal to the input signal. At the output of this circuit, a low pass filter attenuates signals greater than 350 MHz.

The **First IF Bandpass Filter** (a service adjustable helical resonator filter) attenuates signals out of the passband centered at 310.1875 MHz.

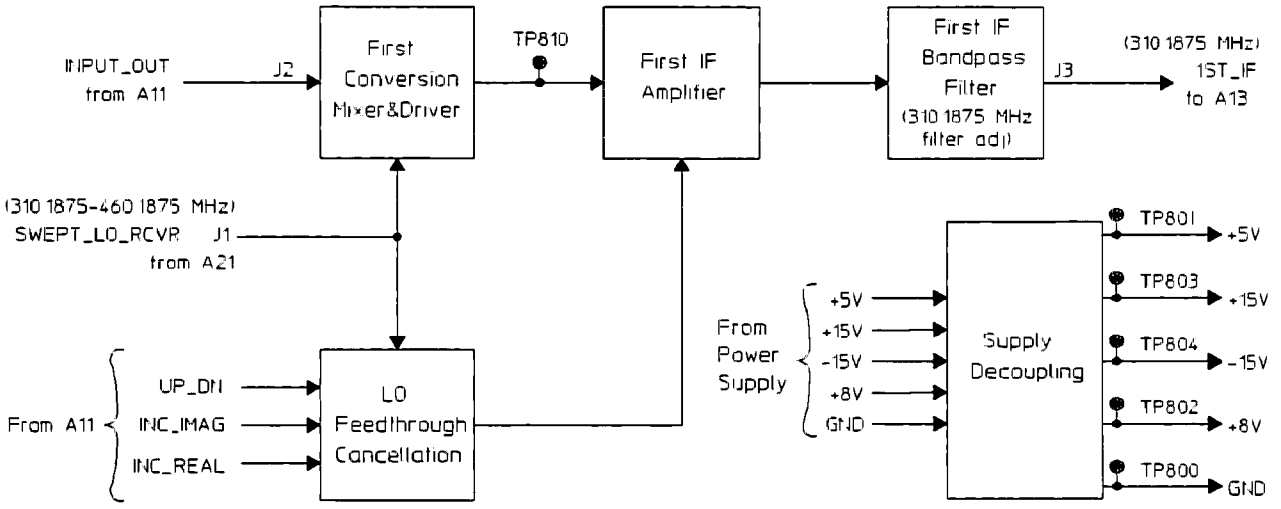


Figure 8-9. A12 First Conversion Block Diagram

A13 Second Conversion

The Second Conversion assembly is the third of five assemblies that condition the input signal. This assembly mixes a 300 MHz frequency reference with the 310.1875 MHz signal from the First Conversion assembly. The resulting 10.1875 MHz signal is routed to the IF assembly. Figure 8-10 shows the Second Conversion assembly's block diagram.

The **350 MHz Low Pass Filter** attenuates signals greater than 350 MHz.

The **Second Conversion Mixer/Driver** increases the amplitude of the 300 MHz reference signal to +17 dBm at the mixer input. It then mixes the reference signal with the 310.1875 MHz IF signal.

The **12 MHz Low Pass Filter** attenuates signals above the 10.1875 MHz second IF frequency.

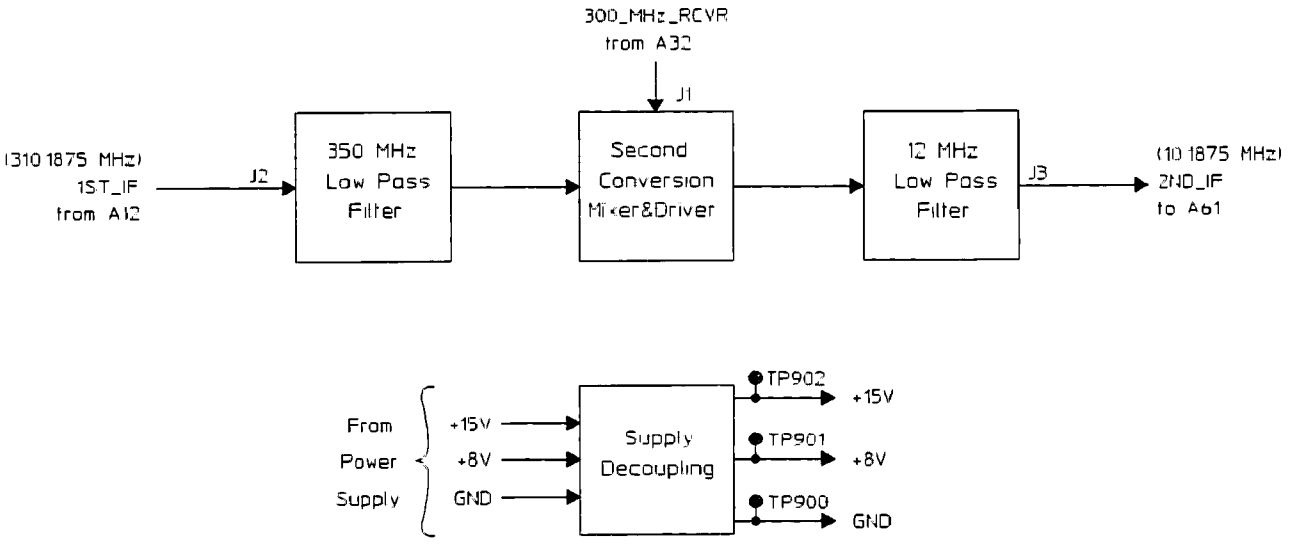


Figure 8-10. A13 Second Conversion Block Diagram

A21 Sum VCO

The Sum VCO assembly is one of six assemblies that together function as the analyzer's local oscillator. This assembly is used when the local oscillator operates in either single loop mode or multiple loop mode (see figures 8-12 and 8-13). The Sum VCO assembly provides four signals that can sweep from 310.1875 to 460.1875 MHz. Two of these signals provide feedback — one to close the single loop mode's single loop and another to close the multiple loop mode's sum loop. The other two signals provide the swept LO signal for the First Conversion assembly and the Source Conversion assembly. Figure 8-11 shows the Sum VCO assembly's block diagram.

In single loop mode, the **Control Voltage Switch** connects the single loop control voltage to the Sum Loop VCO. In multiple loop mode, this switch connects the multiple loop control voltage to the Sum Loop VCO. If multiple loop mode's sum loop is unlocked, the Out of Lock Detector on the Sum Phase Detector assembly provides a control line to this circuit that speeds up the sum loop's settling time. The IIC Interface on the Step Phase Detector assembly provides the control line that selects multiple or single loop mode. This switch also provides the control line for the Single Loop Bias Shutdown Switch.

The **Sum Loop VCO** generates a signal that can sweep from 310.1875 to 460.1875 MHz. The multiple or single loop control voltage controls the VCO's frequency. This circuit also contains two service adjustments — one to improve the spectral purity of the VCO and the other to improve the tracking of the sum loop VCO and step loop VCO to each other.

The **Sum Loop Buffers** route the swept signal through four buffered signal paths that are current biased by the **Amplifier Current Sources.**

In multiple loop mode, the **Single Loop Bias Shutdown Switch** turns off the current biasing for the single loop VCO signal path.

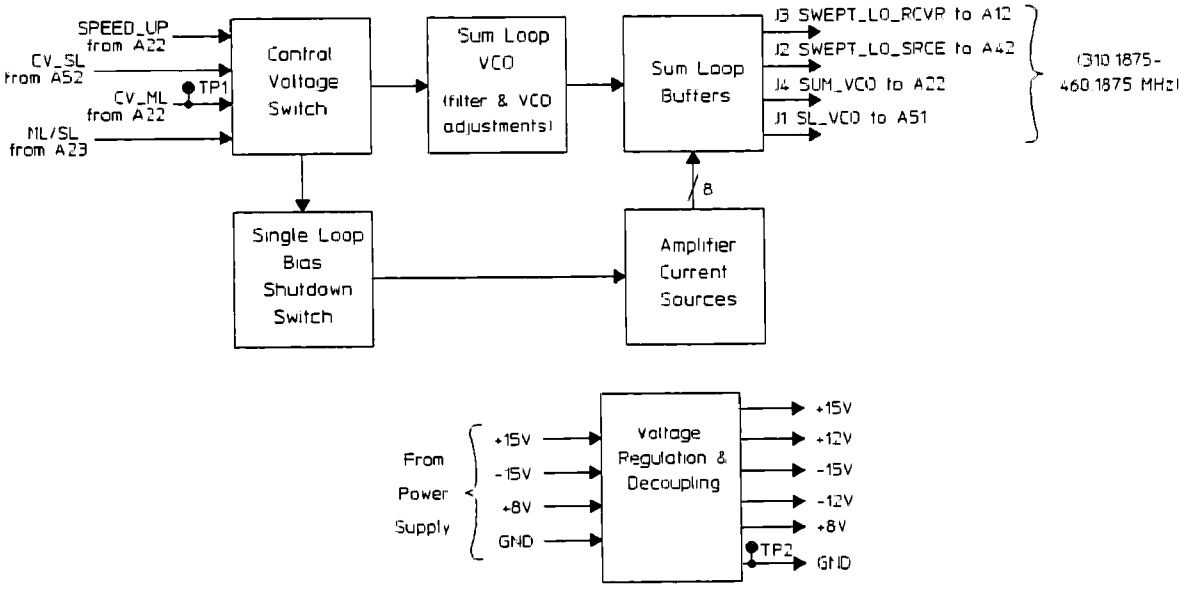


Figure 8-11. A21 Sum VCO Block Diagram

Note

The analyzer's local oscillator operates in either single loop mode or multiple loop mode. The CPU assembly selects which mode based on the frequency span, resolution bandwidth, and sweep time of the measurement. Single loop mode allows the fastest sweep time, and multiple loop mode provides better phase noise and spurious performance. Therefore, the local oscillator uses multiple loop mode for all narrow-band zoom measurements and for swept spectrum measurements with slow sweep time, narrow frequency span, and narrow resolution bandwidth. The local oscillator uses single loop mode for all other swept spectrum measurements and all network measurements.

In single loop mode, the local oscillator uses one PLL (phase-locked loop) — single loop (see figure 8-12). In multiple loop mode, the local oscillator uses three PLLs — step loop, interpolation loop, and sum loop (see figure 8-13).

In the single loop, the feedback signal (SL_VCO) is divided by ten. The resulting signal (F/N_VCO) is then divided down to 100 kHz. The phases of the divided signal and the 100 kHz reference signal (100_KHZ_REF) are compared and integrated by the integrator. The output voltage of the integrator becomes the control voltage (CV_SL) for the sum VCO. The output of the sum VCO is routed to three signal paths — one provides feedback (SL_VCO) for the single loop, and the other two provide the swept LO for the source and receiver (SWEPT_LO_SRCE and SWEPT_LO_RCVR).

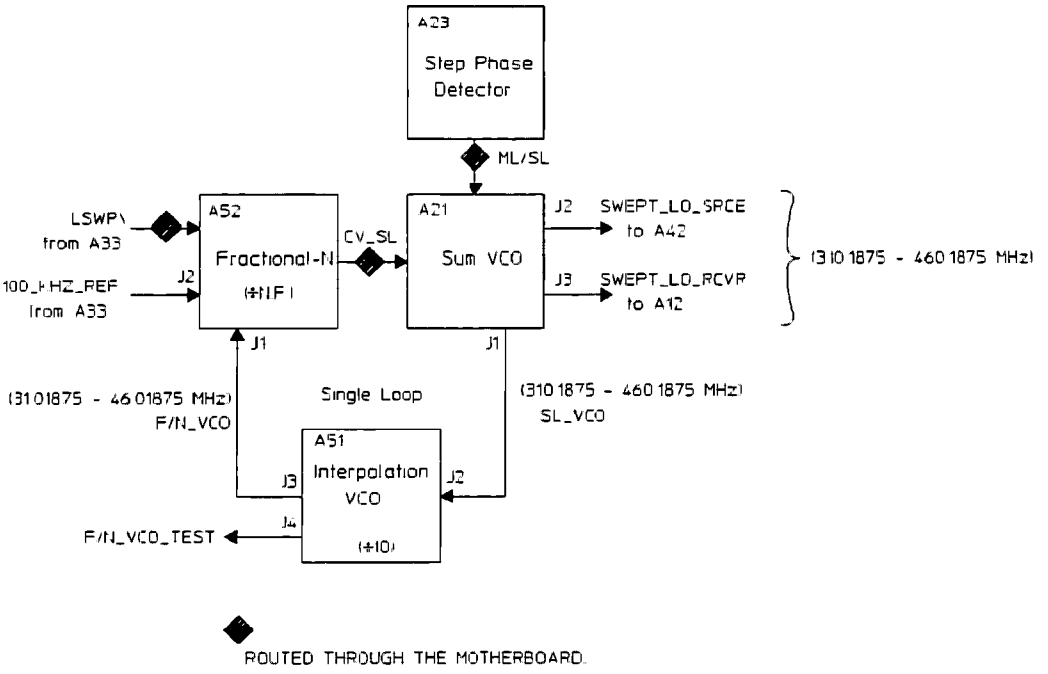


Figure 8-12. Local Oscillator in Single Loop Mode

Note

In the interpolation loop (see figure 8-13), the feedback signal (F/N_VCO) is divided down to 100 kHz. The phases of the divided feedback signal and the 100 kHz reference signal (100_KHZ_REF) are then compared, and integrated by the integrator. The output voltage of the integrator becomes the control voltage (CV_FRACN) for the interpolation VCO. The output of the interpolation VCO is routed to two signal paths — one provides feedback (F/N_VCO) to close the interpolation loop, and the other provides a signal that is divided by 5 or 10, then sent to the sum loop for fine frequency tuning (INTRPL_VCO).

In the step loop, the feedback signal (STEP_VCO) is mixed with the 300 MHz frequency reference (300_MHZ_REF). The difference frequency is divided down to 2 or 5 MHz. The 10 MHz frequency reference (10_MHZ_REF) is also divided down to 2 or 5 MHz. The phases of the two signals are compared, and integrated by the integrator. The output voltage of the integrator becomes the control voltage (CV_STEP) for the step VCO and the pretune voltage (PRETUNE) for the sum loop. The output of the step VCO is routed to two signal paths — one provides feedback (STEP_VCO) to close the step loop, and the other provides the sum loop with a phase reference (STEP_TO_SUM).

In the sum loop, the feedback signal (SUM_VCO) is mixed with the step signal (STEP_TO_SUM). The phases of the difference frequency and the interpolation VCO (INTRPL_VCO) are then compared, and integrated by the integrator. Pretune voltage (PRETUNE) is added to the output voltage of the integrator (to ensure that the sum loop can phase lock), and the resulting voltage becomes the control voltage (CV_ML) for the sum VCO. The output of the sum VCO is routed to three signal paths — one provides feedback to close the sum loop (SUM_VCO), and the other two provide the swept LO for the source and receiver (SWEPT_LO_SRCE and SWEPT_LO_RCVR).

The divide by numbers and frequencies that generate the lower swept LO frequencies (310.1875 to 341 MHz) are labeled L. The divide by numbers and frequencies that generate the higher swept LO frequencies (341 to 460.1875 MHz) are labeled H. See table 8-1 for a matrix of frequencies when the local oscillator is in multiple loop mode.

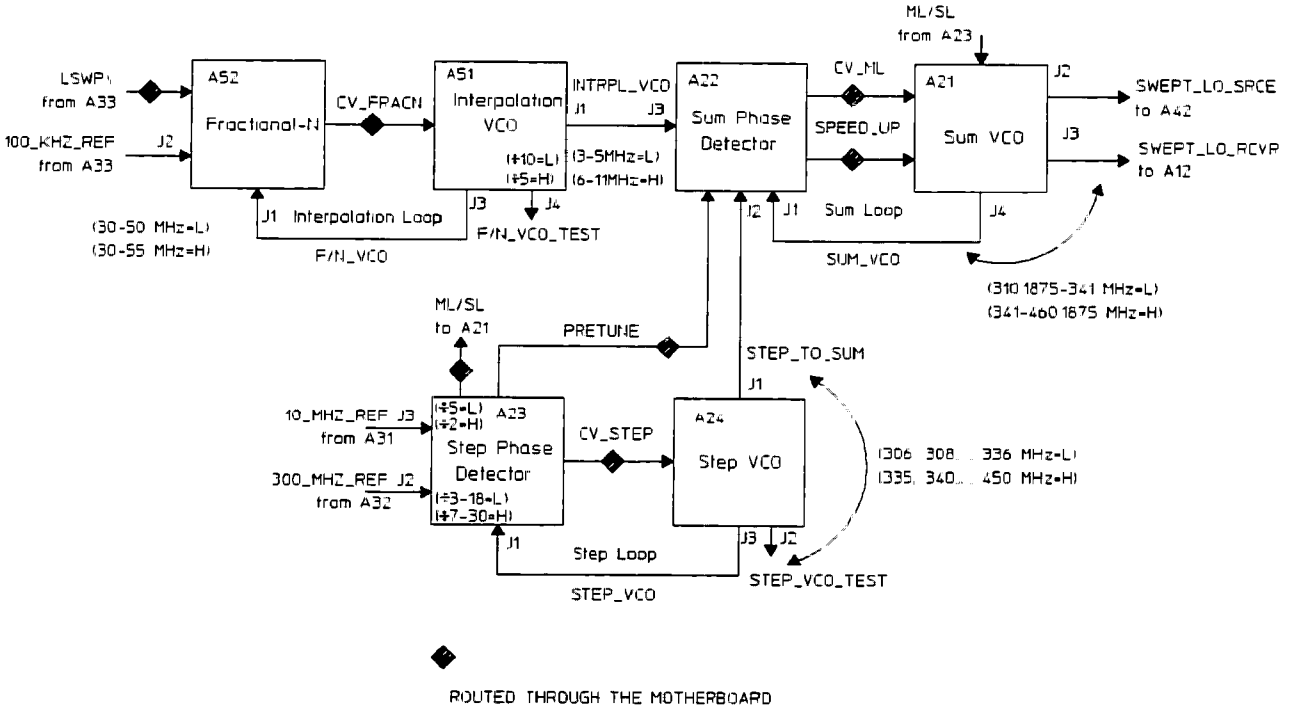


Figure 8-13. Local Oscillator in Multiple Loop Mode

Table 8-1. Multiple Loop Mode Frequency Matrix

Measurement Freq		Sum VCO		Step VCO		F/N VCO		Intrpl VCO	
Start ≥ (MHz)	Stop < (MHz)	Start (MHz)	Stop (MHz)	Freq (MHz)	Divide By N	Start (MHz)	Stop (MHz)	Start (MHz)	Stop (MHz)
0.0	0.8125	310.1875	311.0	306	3	41.875	50.0	4.1875	5.0
0.8125	2.8125	311.0	313.0	308	4	30.0	50.0	3.0	5.0
2.8125	4.8125	313.0	315.0	310	5	30.0	50.0	3.0	5.0
4.8125	6.8125	315.0	317.0	312	6	30.0	50.0	3.0	5.0
6.8125	8.8125	317.0	319.0	314	7	30.0	50.0	3.0	5.0
8.8125	10.8125	319.0	321.0	316	8	30.0	50.0	3.0	5.0
10.8125	12.8125	321.0	323.0	318	9	30.0	50.0	3.0	5.0
12.8125	14.8125	323.0	325.0	320	10	30.0	50.0	3.0	5.0
14.8125	16.8125	325.0	327.0	322	11	30.0	50.0	3.0	5.0
16.8125	18.8125	327.0	329.0	324	12	30.0	50.0	3.0	5.0
18.8125	20.8125	329.0	331.0	326	13	30.0	50.0	3.0	5.0
20.8125	22.8125	331.0	333.0	328	14	30.0	50.0	3.0	5.0
22.8125	24.8125	333.0	335.0	330	15	30.0	50.0	3.0	5.0
24.8125	26.8125	335.0	337.0	332	16	30.0	50.0	3.0	5.0
26.8125	28.8125	337.0	339.0	334	17	30.0	50.0	3.0	5.0
28.8125	30.8125	339.0	341.0	336	18	30.0	50.0	3.0	5.0
30.8125	35.8125	341.0	346.0	335	7	30.0	55.0	6.0	11.0
35.8125	40.8125	346.0	351.0	340	8	30.0	55.0	6.0	11.0
40.8125	45.8125	351.0	356.0	345	9	30.0	55.0	6.0	11.0
45.8125	50.8125	356.0	361.0	350	10	30.0	55.0	6.0	11.0
50.8125	55.8125	361.0	366.0	355	11	30.0	55.0	6.0	11.0
55.8125	60.8125	366.0	371.0	360	12	30.0	55.0	6.0	11.0
60.8125	65.8125	371.0	376.0	365	13	30.0	55.0	6.0	11.0
65.8125	70.8125	376.0	381.0	370	14	30.0	55.0	6.0	11.0
70.8125	75.8125	381.0	386.0	375	15	30.0	55.0	6.0	11.0
75.8125	80.8125	386.0	391.0	380	16	30.0	55.0	6.0	11.0
80.8125	85.8125	391.0	396.0	385	17	30.0	55.0	6.0	11.0
85.8125	90.8125	396.0	401.0	390	18	30.0	55.0	6.0	11.0
90.8125	95.8125	401.0	406.0	395	19	30.0	55.0	6.0	11.0
95.8125	100.8125	406.0	411.0	400	20	30.0	55.0	6.0	11.0
100.8125	105.8125	411.0	416.0	405	21	30.0	55.0	6.0	11.0
105.8125	110.8125	416.0	421.0	410	22	30.0	55.0	6.0	11.0
110.8125	115.8125	421.0	426.0	415	23	30.0	55.0	6.0	11.0
115.8125	120.8125	426.0	431.0	420	24	30.0	55.0	6.0	11.0
120.8125	125.8125	431.0	436.0	425	25	30.0	55.0	6.0	11.0
125.8125	130.8125	436.0	441.0	430	26	30.0	55.0	6.0	11.0
130.8125	135.8125	441.0	446.0	435	27	30.0	55.0	6.0	11.0
135.8125	140.8125	446.0	451.0	440	28	30.0	55.0	6.0	11.0
140.8125	145.8125	451.0	456.0	445	29	30.0	55.0	6.0	11.0
145.8125	150.0	456.0	460.1875	450	30	30.0	50.9375	6.0	10.1875

A22 Sum Phase Detector

The Sum Phase Detector assembly is one of six assemblies that together function as the analyzer's local oscillator. This assembly is used only when the local oscillator operates in multiple loop mode (see figure 8-13). The Sum Phase Detector assembly generates the multiple loop control voltage for the sum loop. If the control voltage is out of range, this assembly clamps the voltage and tells the CPU assembly. Figure 8-14 shows the Sum Phase Detector assembly's block diagram.

The **Offset Mixer** mixes the sum VCO signal with the step signal. When the sum VCO signal sweeps from 310.1875 to 341 MHz, the step signal steps from 306 to 336 MHz in 2 MHz increments. When the sum VCO signal sweeps from 341 to 460.1875 MHz, the step signal steps from 335 to 450 MHz in 5 MHz increments.

The **Sum Loop Phase Detector** compares the phase of the signal from the Offset Mixer to the phase of the interpolation VCO and generates a voltage relative to the phase difference. When the sum VCO signal is in the range from 310.1875 to 341 MHz, the interpolation signal sweeps from 3 to 5 MHz, and when the sum VCO signal is in the range from 341 to 460.1875 MHz, the interpolation signal sweeps from 6 to 11 MHz.

The **Sum Loop Integrator** integrates the phase difference of the two signals. To ensure that the sum loop can phase lock, pretune voltage is added to the output of the integrator. This voltage provides the control voltage for the multiple loop.

The **Out-of-Lock Detector** clamps the output of the integrator (before the pretune voltage is added) if the amplitude is not within the range of –0.6 to +0.15V. It then tells the CPU assembly that the amplitude is too high or too low, which means the sum loop is unlocked. The Out-of-Lock Detector also provides a control signal, which speeds up the sum loop's settling time when the sum loop is unlocked.

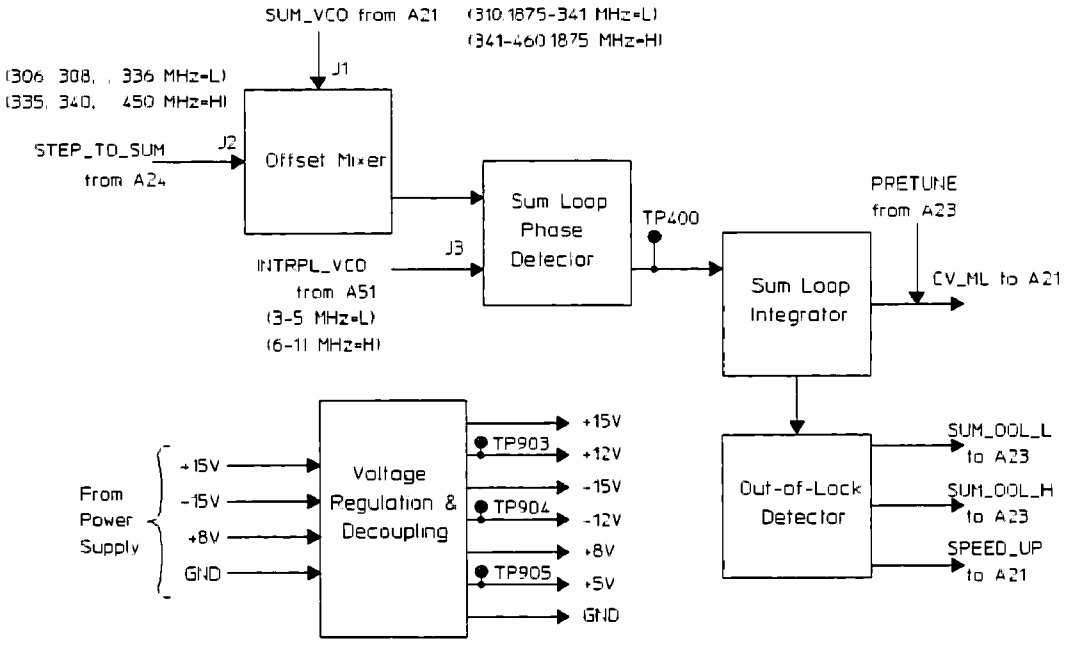


Figure 8-14. A22 Sum Phase Detector Block Diagram

A23 Step Phase Detector

The Step Phase Detector assembly is one of six assemblies that together function as the analyzer's local oscillator. This assembly is used when the local oscillator operates in either single loop mode or multiple loop mode (see figures 8-12 and 8-13). In single loop mode, the Step Phase Detector assembly provides only the loop mode control line. In multiple loop mode, this assembly provides the loop mode control line, the control voltage for the step loop, and the pretune voltage for the sum loop. Figure 8-15 shows the Step Phase Detector assembly's block diagram.

The **Step Loop Offset Mixer** mixes the 300 MHz frequency reference with the stepped VCO signal. It then filters and amplifies the resulting 6 to 150 MHz difference frequency.

The **Divide-by-N Counter** produces either a 2 or 5 MHz signal by dividing the 6 to 150 MHz difference frequency with a number between 3 and 30. When the step VCO signal steps from 306 to 336 MHz in 2 MHz increments, this circuit divides by a number (between 3 and 18) that produces a 2 MHz signal. When the step VCO signal steps from 335 to 450 MHz in 5 MHz increments, this circuit divides by a number (between 7 and 30) that produces a 5 MHz signal.

The **Step Size Divider** divides the 10 MHz frequency reference by 5 when the Divide-by-N Counter selects a number that produces a 2 MHz signal, or by 2 when the Divide-by-N Counter selects a number that produces a 5 MHz signal.

The **Step Loop Phase Detector** compares the phase of the signal from the Step Size Divider to the phase of the signal from the Divide-by-N Counter. It then generates a voltage proportional to the phase difference.

The **Step Loop Integrator** amplifies and integrates the phase difference voltage, creating the step loop control voltage.

The **VCO Clamps** compare the control voltage to service adjustable out-of-limit voltages. This circuit clamps the control voltage if its amplitude is not within the approximate range of –2 to +7V. It also tells the CPU assembly that the amplitude is too high or too low, which means the step loop is unlocked.

The **Pretune** circuit adds a service adjustable dc offset level to the control voltage, then amplifies it by a service adjustable gain. The resulting voltage coarsely adjusts the sum VCO's frequency to ensure that the sum loop can phase lock.

The **IIC Interface** provides the interface between the CPU assembly and the Step Phase Detector assembly, and it provides the loop mode control line to the Sum VCO assembly. It also interrupts the CPU assembly if either the sum loop or the step loop is unlocked.

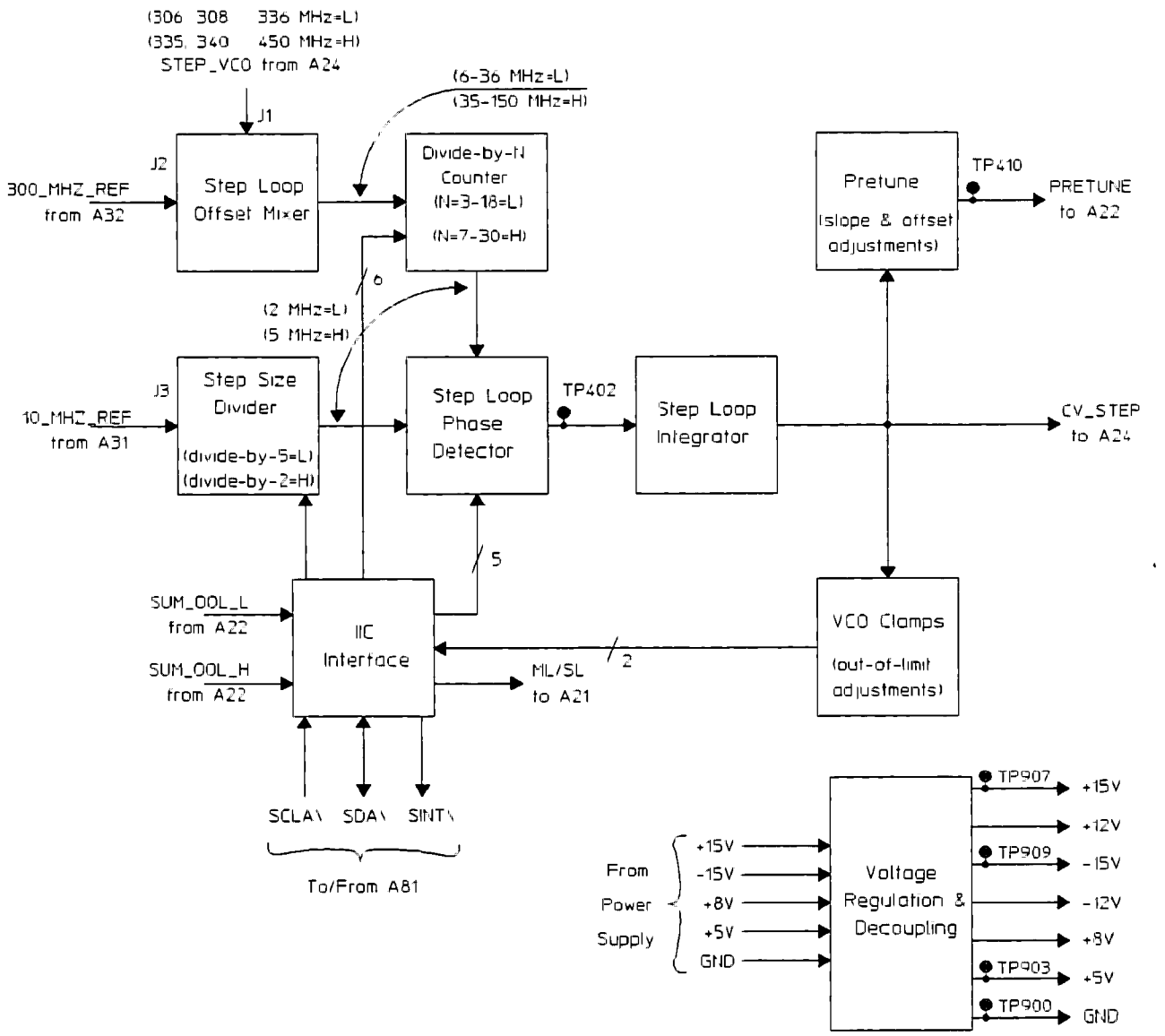


Figure 8-15. A23 Step Phase Detector

A24 Step VCO

The Step VCO assembly is one of six assemblies that together function as the analyzer's local oscillator. This assembly is used only when the local oscillator operates in multiple loop mode (see figure 8-13). The Step VCO assembly generates a 306 to 450 MHz signal that provides feedback for the step loop and an offset frequency reference for the sum loop. Figure 8-16 shows the Step VCO assembly's block diagram.

The **Step Loop VCO** generates a signal that steps from 306 to 336 MHz in 2 MHz increments or from 335 to 450 MHz in 5 MHz increments. In single loop mode, this VCO generates a 306 MHz signal even though the signal is not used. The step loop control voltage controls the VCO's frequency. This circuit also contains two service adjustments — one to improve the spectral purity of the VCO and the other to improve the tracking of the sum loop VCO and step loop VCO to each other.

The **Step Loop Buffers** route the signal into three separate signal paths that filter and amplify each signal. One signal provides feedback to close the step loop. Another signal provides an offset frequency reference for the sum loop. The third signal provides a test port to check the sum loop.

The **Thermal Switch** shuts down the Power Supply assembly if it senses an over-temperature condition.

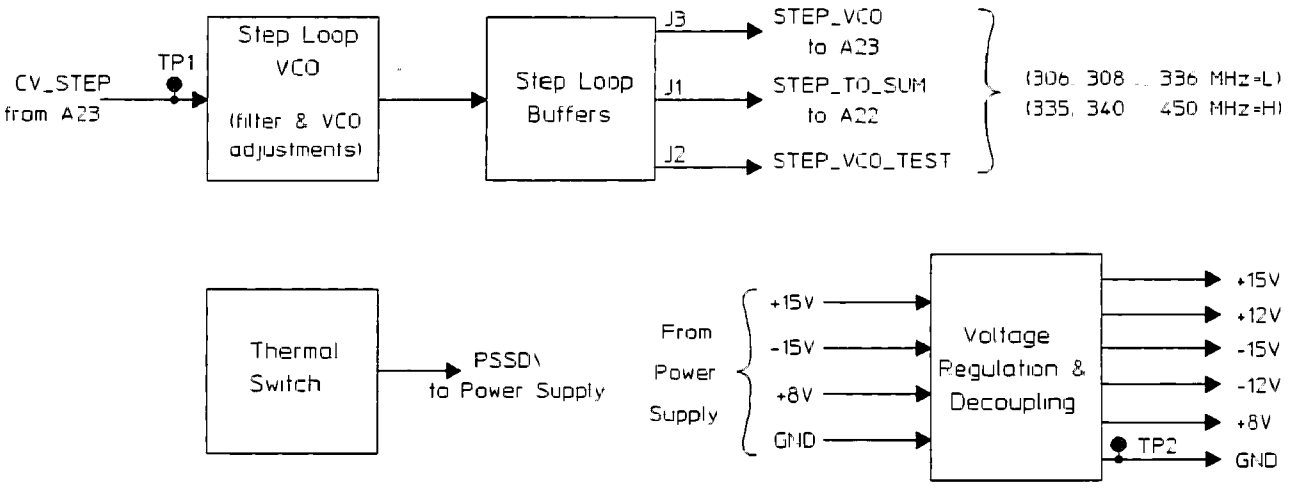


Figure 8-16. A24 Step VCO Block Diagram

A31 Reference/Calibrator

The Reference/Calibrator assembly provides three frequency references (80, 20, and 10 MHz) to various assemblies. It also provides a precision amplitude calibration signal to the Input assembly. This precision amplitude calibration signal is actually one of two signals — a precision leveled signal derived from the Source Amplifier assembly or a precision leveled fixed 10 MHz frequency reference. Figure 8-17 shows the Reference/Calibrator assembly's block diagram.

The **80 MHz VCXO** generates an 80 MHz signal, which is the analyzer's primary frequency reference. When an external frequency reference is present, feedback phase-locks the 80 MHz VCXO to the external reference. A service adjustment is provided to adjust the VCXO's frequency.

The **Divide-by-4** circuit divides the 80 MHz signal down to 20 MHz. The **Divide-by-2** circuit divides the 20 MHz signal down to 10 MHz.

The **Input Protection/Signal Conditioning** circuit limits and conditions the external frequency reference. The optional Fan Power/Oven assembly can supply the external frequency reference if a rear panel BNC-to-BNC jumper connects the oven output to the external frequency reference input.

The **External Reference Detector** detects the presence of the external reference, and tells both Tune Enable/Loop Filter/Integrator and the CPU assembly.

The **Sampling Phase Detector** compares the phase of the signal from the Divide-by-2 with the phase of the signal from Input Protection/Signal Conditioning and generates a voltage equal to the phase difference. This circuit can phase lock to an external frequency reference of 1, 2, 5, or 10 MHz.

The **Tune Enable/Loop Filter/Integrator** amplifies and filters the phase-difference voltage from the Sampling Phase Detector. It then routes the voltage to the 80 MHz VCXO as feedback to close the external reference phase-locked loop (PLL). If an external reference is not present, this circuit opens the PLL and routes zero volts to the 80 MHz VCXO. If the Beatnote Detector indicates that the loop is unlocked, this circuit selects a wider loop bandwidth in an attempt to lock.

The **Beatnote Detector** monitors the feedback voltage to the 80 MHz VCXO. If the feedback voltage is either too high or too low (approx ± 10V), indicating that the external reference PLL is unlocked, this circuit tells the Tune Enable/Loop Filter/Integrator and the CPU assembly.

During swept mode calibration, **Swept Cal** amplifies and conditions the swept 200 kHz to 150 MHz, approximate –11 dBm signal to a square wave with a –3 dBm fundamental. During fixed mode calibration, **Fixed 10 MHz Cal** conditions the 10 MHz signal to a square wave with a –3 dBm fundamental.

The **Precision Square Wave Generator** attenuates and conditions the –3 dBm swept or fixed calibration signal to a square wave with a –20 dBm precision amplitude fundamental. This circuit contains both a flatness and a level service adjustment.

The **IIC Interface** provides the interface between the CPU assembly and the Reference/Calibrator assembly. It also interrupts the CPU assembly if the Beatnote Detector indicates that the external reference PLL is unlocked or if the high frequency PLL on the 300 MHz assembly is unlocked.

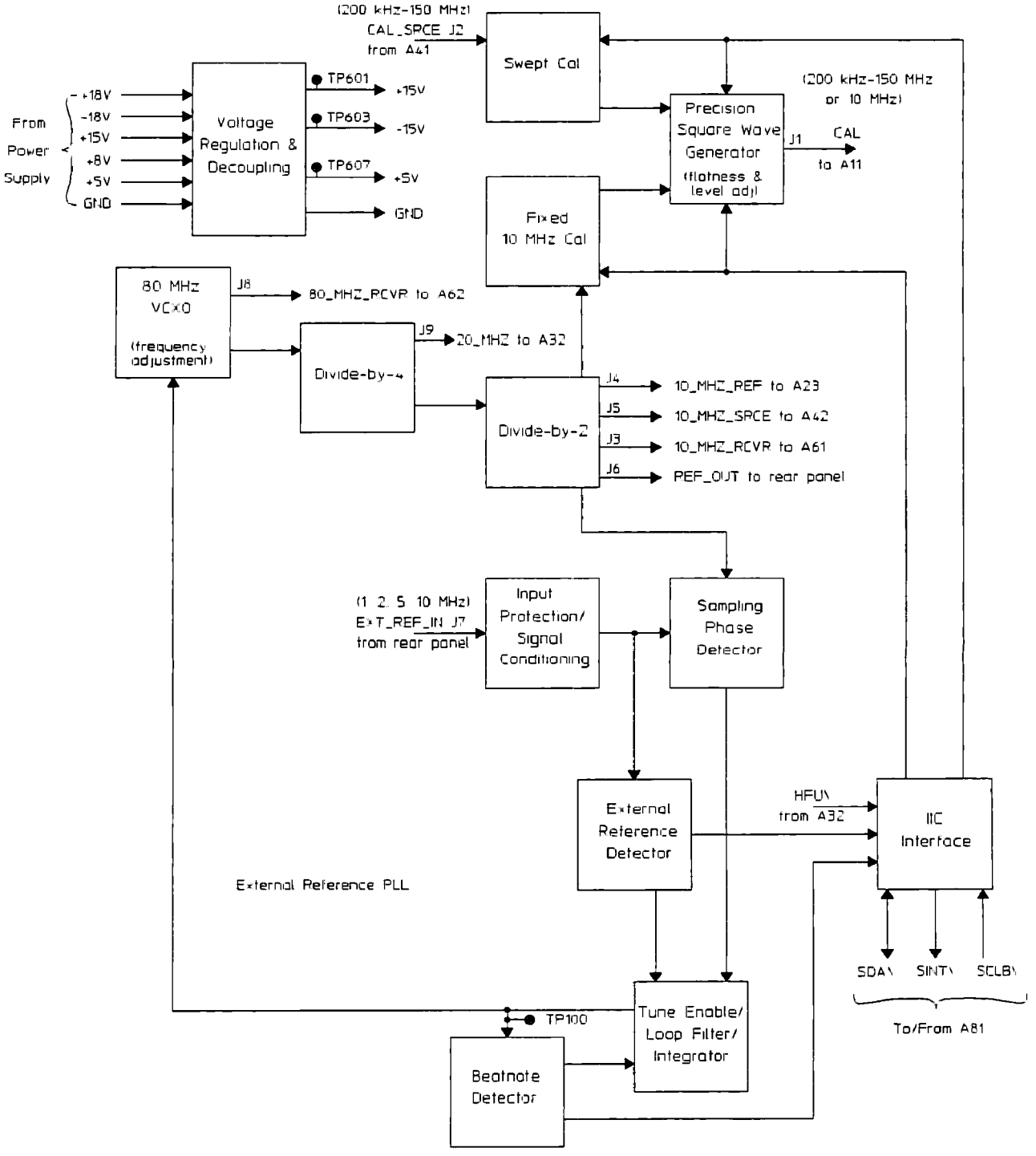


Figure 8-17. A31 Reference/Calibrator Block Diagram

A32 300 MHz

The 300 MHz assembly provides high-frequency references to various assemblies. The high-frequency references are 300 MHz and 60 MHz. These frequency references are phase locked to the Reference/Calibrator assembly at 20 MHz. Figure 8-18 shows the 300 MHz assembly's block diagram.

The **300 MHz VCO** generates a 300 MHz signal. A service adjustment sets the frequency of this VCO. Feedback from the Loop Filter/Integrator adjusts the frequency to keep this VCO phase locked with the 20 MHz reference signal.

The **300 MHz Amplifier** routes the 300 MHz signal to four signal paths and amplifies each signal.

The **Divide-by-5** circuit divides the 300 MHz signal down to 60 MHz and routes the signal to two signal paths. The **Divide-by-3** circuit divides the 60 MHz signal down to 20 MHz.

The **Digital Phase Detector** compares the phase of the 20 MHz signal to the 20 MHz reference signal and generates a voltage equal to the phase difference.

The **Loop Filter/Integrator** filters the phase difference voltage and sends it to the 300 MHz VCO as the control voltage.

The **PLL Unlocked Detector** monitors the voltage from the Loop Filter/Integrator. If the voltage goes too high or too low, the high-frequency PLL unlocks and the Reference/Calibrator assembly interrupts the CPU assembly.

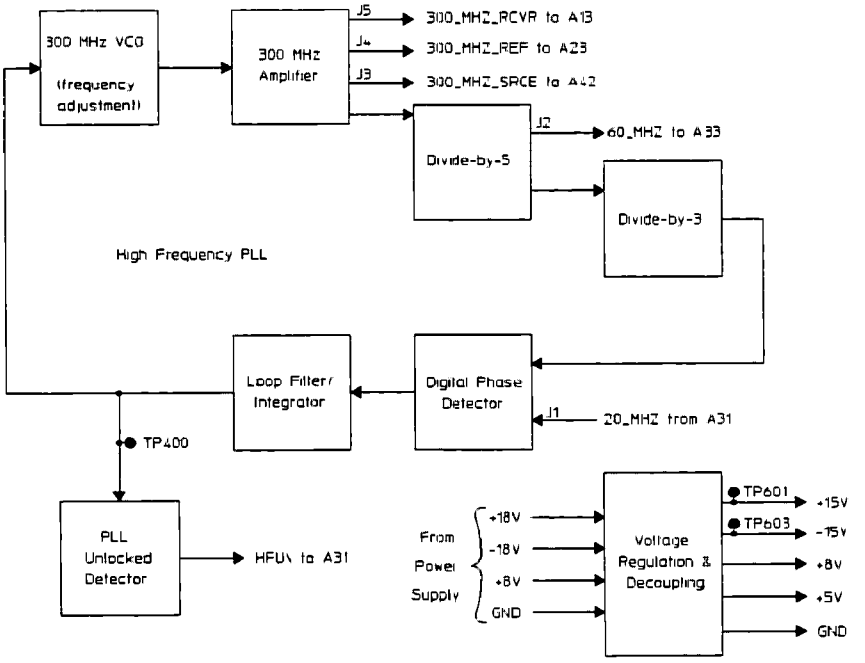


Figure 8-18. A32 300 MHz Block Diagram

A33 Trigger

The Trigger assembly provides low-frequency reference signals, gated-sweep control signals, the sweep synchronization signal (LSWP\), and the trigger signal. The low frequency reference signals are 100 kHz, 187.5 kHz, and 250 kHz. Figure 8-19 shows the Trigger assembly's block diagram.

The **Divide-by-4** circuit divides the 60 MHz signal down to 15 MHz. The **Divide-by-10** circuit divides the 15 MHz signal down to 1.5 MHz.

The **Clock Synchronization** circuit resets all low-frequency references at instrument power-up and provides the 1.5 MHz signal as a common clock.

The **Divide-by-6** circuit divides the 1.5 MHz signal down to a 250 kHz, TTL-level signal. The **Divide-by-8** circuit divides the 1.5 MHz signal down to a 187.5 kHz, 600 mVp-p, ac-coupled square wave. The **Divide-by-15** circuit reduces the 1.5 MHz signal to a 100 kHz, 1 Vp-p pulse, with an approximate 1% duty cycle.

The **Clock Divider/Delay Timer** circuit divides the 1.5 MHz signal by a number provided by the CPU assembly, generating the Slow Clock. This circuit also provides the Trigger & Sweep/Gate Control circuit with control signals for gated-sweep delay and width.

The **Trigger & Sweep/Gate Control** circuit generates the sweep synchronization signal (LSWP\), the gated-sweep synchronization signal (GSWP), and an enabling signal for gated-sweep data capture (DET_GATE).

This circuit can select internal trigger, HP-IB trigger (GETTRIG), or external trigger. Internal trigger is self-enabling. External trigger, and HP-IB trigger must be enabled by the CPU assembly. When the selected trigger occurs, Trigger & Sweep/Gate Control holds the trigger and after receiving a positive edge from the Slow Clock, outputs it as the sweep synchronization signal. Following a change in resolution bandwidth or an instrument power-up or preset, the negative edge of the sweep synchronization signal resets the phase of the digital filters on the ADC/Digital Filter assembly. On subsequent negative edges, the sweep synchronization signal is the sweep signal for the analyzer. During gated-sweep measurements, the gated-sweep synchronization signal is used with the sweep synchronization signal to provide the sweep signal for the analyzer.

The **IIC Interface** provides the interface between the CPU assembly and the Trigger assembly.

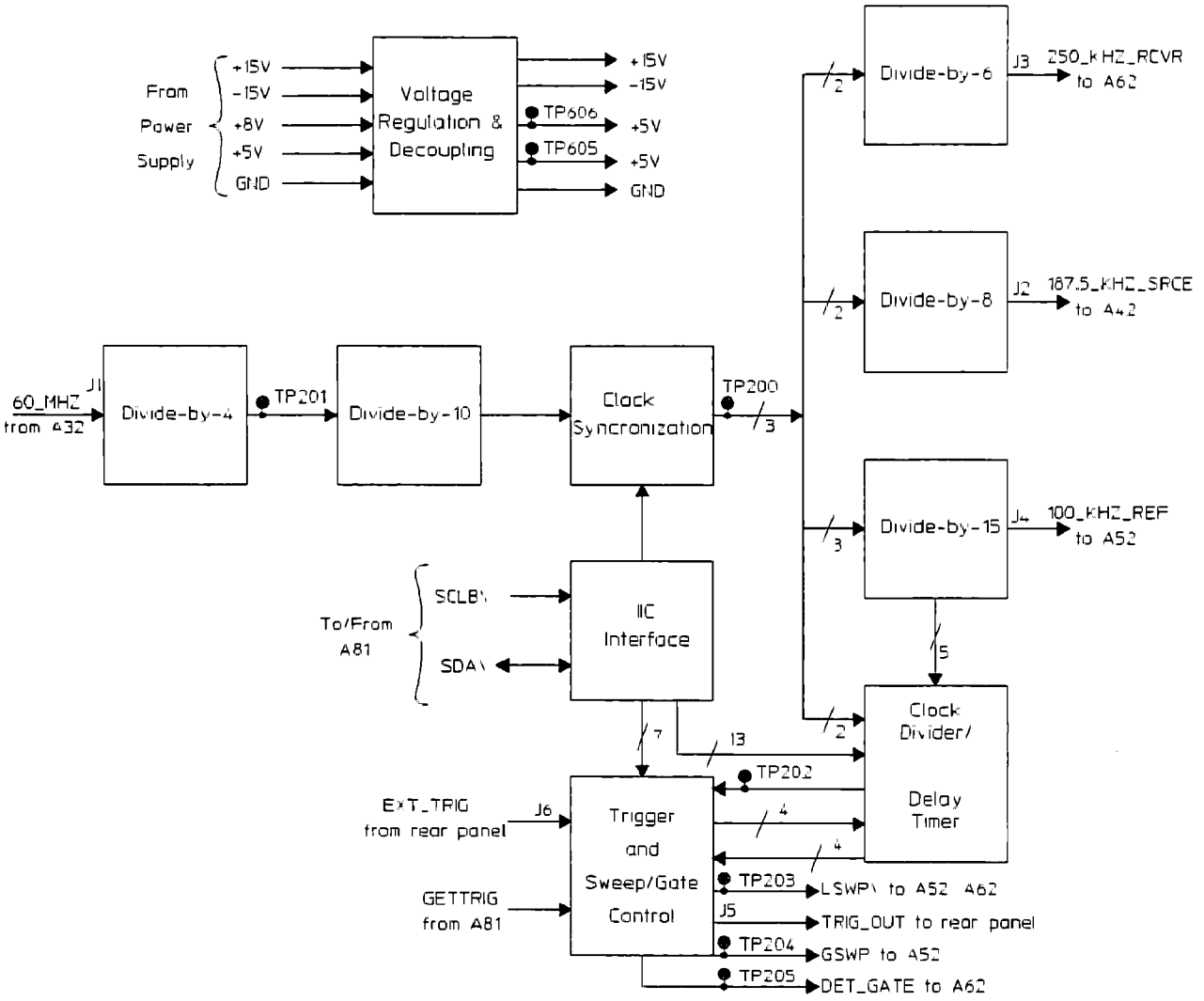


Figure 8-19. A33 Trigger Block Diagram

A41 Source Amplifier

The Source Amplifier assembly is one of two assemblies that together function as the analyzer's source. This assembly amplifies the signal generated by the Source Conversion assembly. It then routes this signal to either the Front Panel assembly, the Input assembly, or the Reference/Calibrator assembly. The output of the Source Amplifier assembly can sweep from 10 Hz to 150 MHz and its amplitude can be adjusted from +15 to –54.9 dBm. Figure 8-20 shows the Source Amplifier assembly's block diagram.

The two **22 dB Amplifiers** and the one **15 dB Amplifier** provide 59 dB of gain to the signal from the Source Conversion assembly.

The **DC Servo** provides feedback to drive the dc voltage to zero volts at the output of the 15 dB Amplifier.

The **Attenuator** provides from 0 to 50 dB of attenuation, in 10 dB increments.

The **Output Switching** circuit routes the source signal to either the front panel or the Input assembly (for normalized measurements). During calibration, this circuit also routes the source signal to the Reference/Calibrator assembly.

The **Overload Detector/Threshold Set** monitors the voltage at the output of the Source Amplifier assembly. If the voltage exceeds the threshold set by the Source Conversion assembly, this circuit tells the IIC Interface, which in turn, disconnects the output from the front panel and interrupts the CPU assembly.

The **IIC Interface** provides the interface between the CPU assembly and the Source Amplifier assembly. It also provides control logic for the signals from the Source Conversion assembly.

The **Thermal Switch** shuts down the Power Supply assembly if it senses an over-temperature condition.

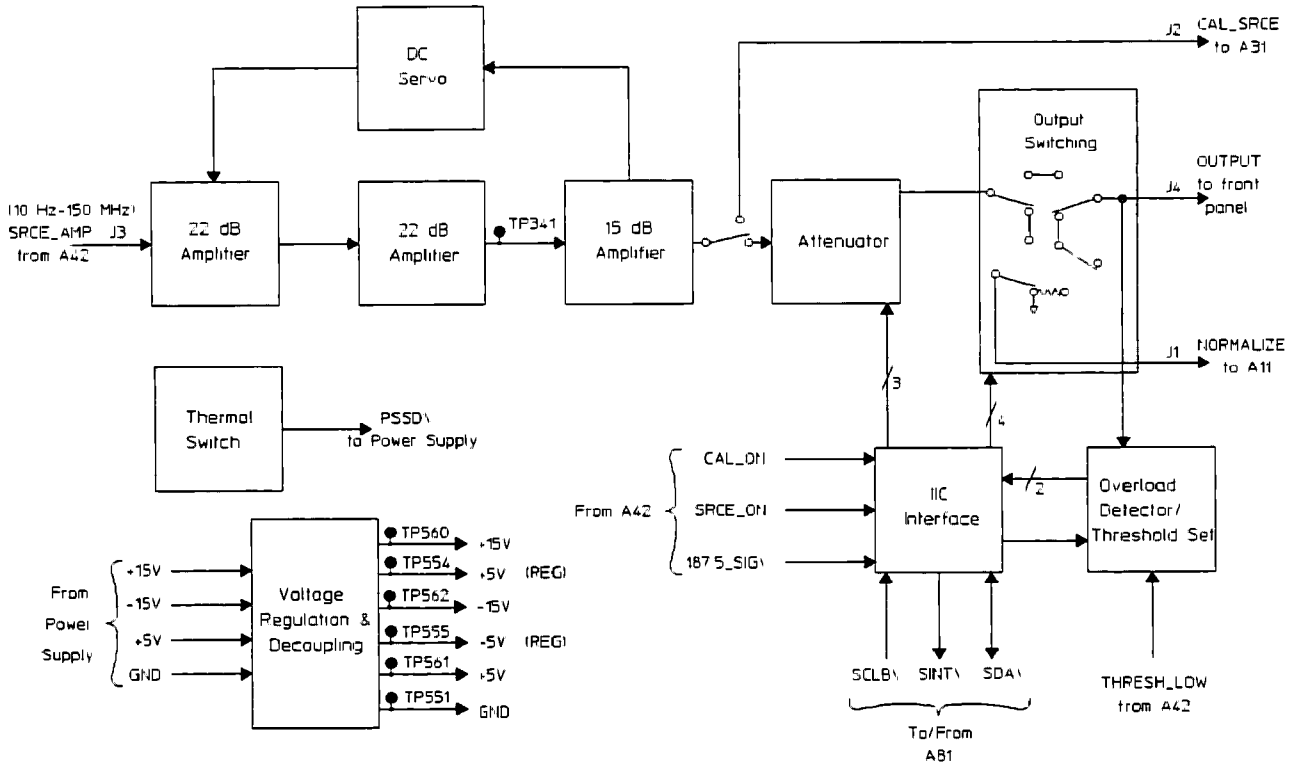


Figure 8-20. A41 Source Amplifier Block Diagram

A42 Source Conversion

The Source Conversion assembly is one of two assemblies that together function as the analyzer's source. The Source Conversion assembly generates the source signal, and the Source Amplifier assembly provides the final amplification for the source signal. Figure 8-21 shows the Source Conversion assembly's block diagram.

The **187.5 kHz Limiter** limits the amplitude of the 187.5 kHz square wave, providing the Gilbert Cell Multiplier with a constant-amplitude square wave. It also provides the dc bias voltage to the Gilbert Cell Multiplier.

The **187.5 kHz Detector** can check for the presence of the signal in one of two places — either at the input of the 187.5 kHz Limiter or the output of the Gilbert Cell Multiplier.

The **Amplitude Control** circuit converts digital data to the differential control signal.

The **Gilbert Cell Multiplier** generates a 187.5 kHz square wave with an amplitude proportional to the amplitude of the differential control signal. The square wave amplitude may be controlled over a 19.9 dB range.

The **190 kHz Low Pass Filter** attenuates signals above 190 kHz (harmonic energy of the 187.5 kHz square wave).

The **10 MHz Limiter/First Mixer** limits the amplitude of the 10 MHz reference signal. It then mixes the 10 MHz signal with the 187.5 kHz signal, producing a 10.1875 MHz signal.

The **10.1875 MHz Filter/Amplifier** filters and amplifies the 10.1875 MHz signal.

The **300 MHz LO Driver** amplifies the 300 MHz reference to +7 dBm at the input to the second mixer.

The **Second Mixer** mixes the 300 MHz signal with the 10.1875 MHz signal, producing a 310.1875 MHz signal.

The **310.1875 MHz Filter/Amplifier** filters and amplifies the 310.1875 MHz signal. This circuit contains a service-adjustable helical resonator filter.

The **LO Driver** amplifies the swept LO signal to +7 dBm at the input of the Third Mixer.

The **Third Mixer** mixes the swept LO signal (310.1875 to 460.1875 MHz) with the 310.1875 MHz signal, producing a frequency that tracks the tuned receiver frequency.

The **150 MHz Low Pass Filter** attenuates all signals above 150 MHz and routes the 10 Hz to 150 MHz swept signal to the Source Amplifier assembly.

The **IIC Interface** provides control lines from the CPU assembly to both the Source Conversion assembly and the Source Amplifier assembly.

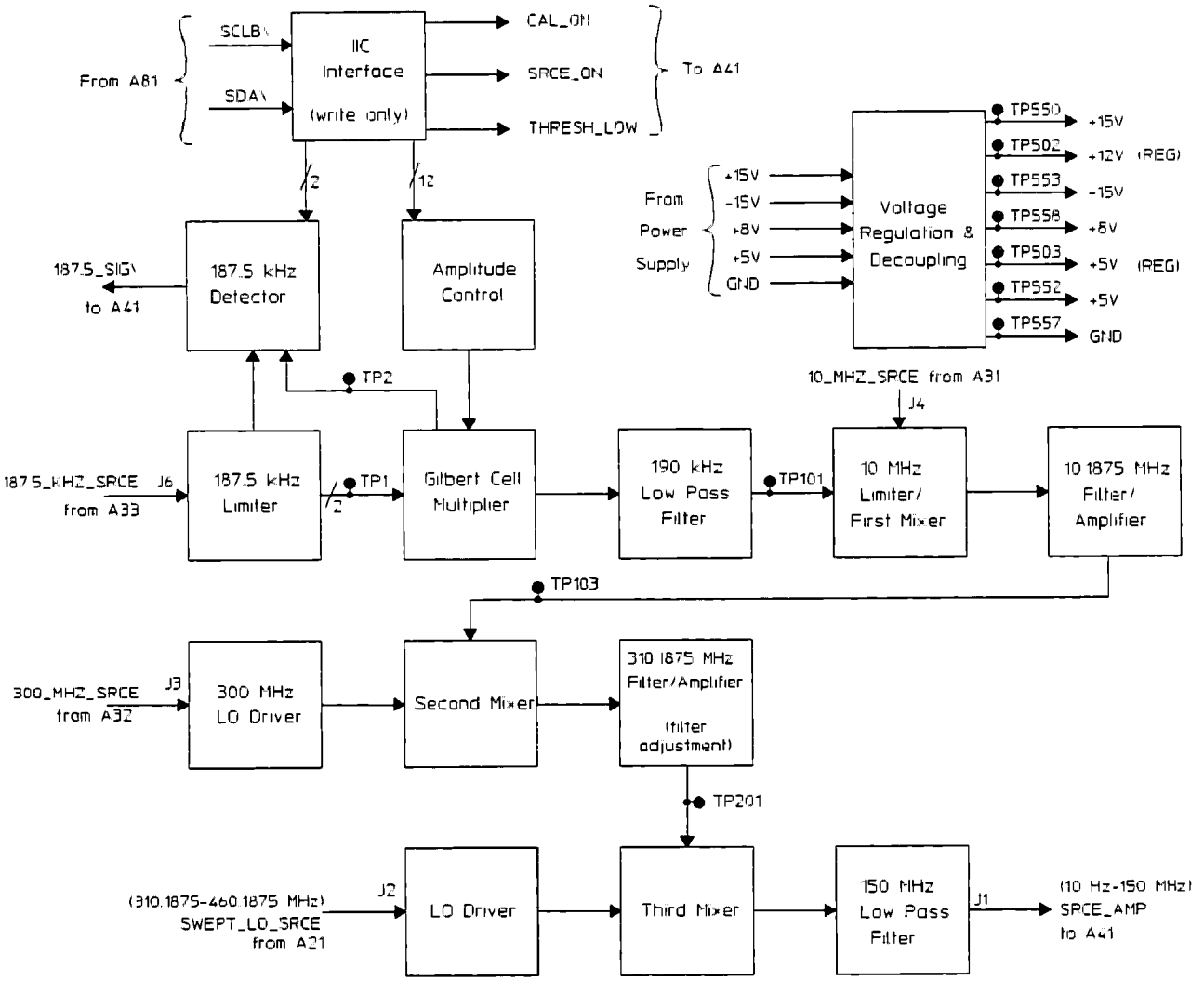


Figure 8-21. A42 Source Conversion Block Diagram

A51 Interpolation VCO

The Interpolation VCO assembly is one of six assemblies that together function as the analyzer's local oscillator. This assembly is used when the local oscillator operates in either single loop mode or multiple loop mode (see figures 8-12 and 8-13). In multiple loop mode, this assembly provides the interpolation VCO and feedback to close the interpolation loop. In single loop mode, this assembly provides feedback to close the single loop. Figure 8-22 shows the Interpolation VCO assembly's block diagram.

In multiple loop mode, the **Interpolation VCO** generates a signal that sweeps from 30 to 50 MHz or from 30 to 55 MHz. The fractional-N control voltage determines the frequency. There's also a service adjustment to control the frequency range. In single loop mode, this VCO is disabled.

The **VCO Buffer Amplifier** conditions the signal and routes it through two signal paths.

The **Divide-by-10/Divide-by-5** circuit divides the signal from the VCO Buffer by 10 or 5. For output frequencies lower than 341 MHz, the VCO sweeps from 30 to 50 MHz and this circuit divides it by 10 (providing a 3 to 5 MHz signal). For output frequencies higher than 341 MHz, the VCO sweeps from 30 to 55 MHz and this circuit divides it by 5 (providing a 6 to 11 MHz signal).

In single loop mode, the **Divide-by-10** circuit divides the single loop VCO signal by 10, resulting in a 31 to 46 MHz signal. In multiple loop mode, this circuit is disabled.

In single loop mode, the **Single/Multiple Loop Switch** sends the signal from the Divide-by-10 to the Fractional-N assembly to close the single PLL. In multiple loop mode, this circuit sends the signal from the VCO Buffer Amplifier to the Fractional-N assembly to close the interpolation PLL.

The **Control Voltage Detector** monitors the amplitude of the fractional-N control voltage, in both multiple and single loop mode. The fractional-N control voltage is the same as the single loop control voltage that is sent to the Sum VCO assembly, except the single loop control voltage is clamped. Therefore, checking the fractional-N control voltage is essentially the same as checking the single loop control voltage.

The **IIC Interface** provides the interface between the CPU assembly and the Interpolation VCO assembly. This circuit interrupts the CPU assembly if the control voltage (from the Control Voltage Detector) is too high or too low — a situation that will occur if the interpolation loop or the single loop is unlocked. The IIC Interface also interrupts the CPU assembly if the fractional-N signal on the Fractional-N assembly reaches the end of its sweep.

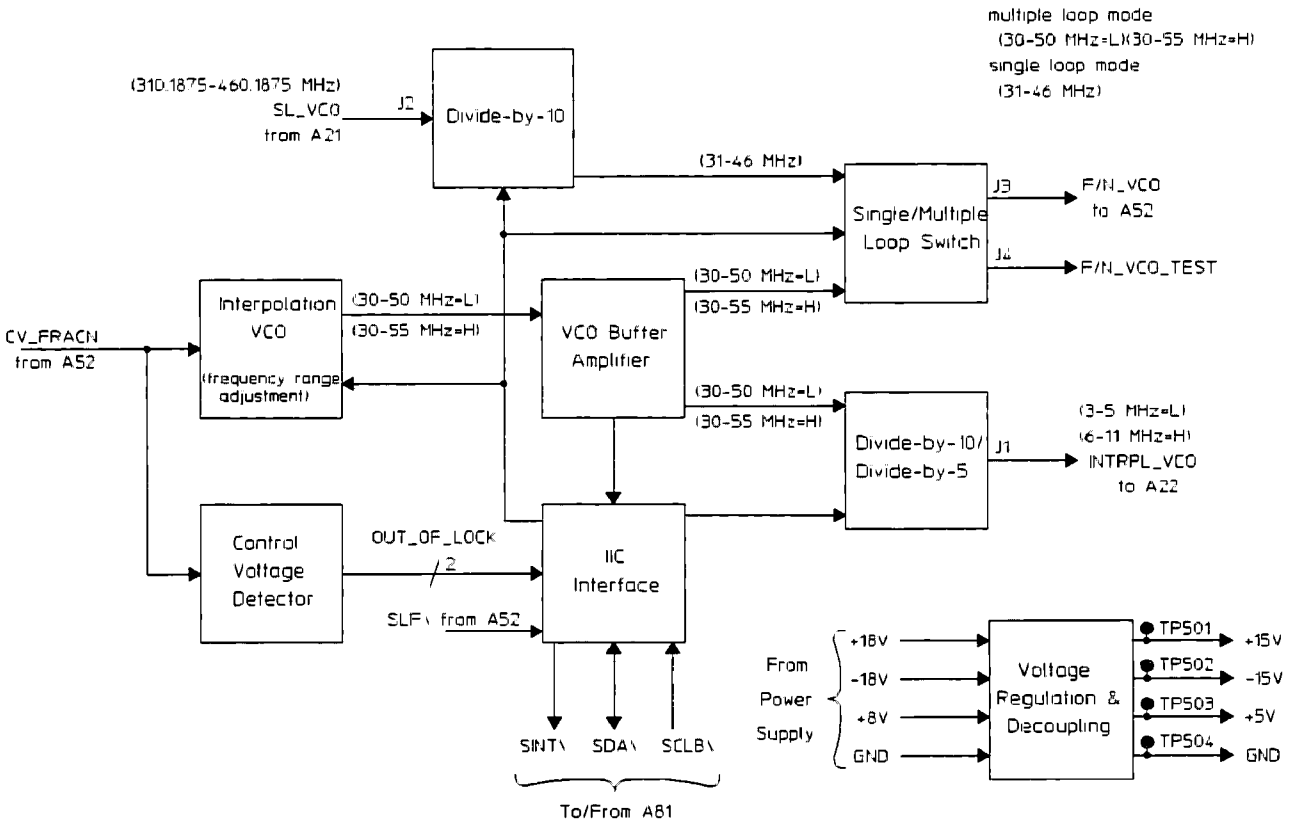


Figure 8-22. A51 Interpolation VCO Block Diagram

A52 Fractional-N

The Fractional-N assembly is one of six assemblies that together function as the analyzer's local oscillator. This assembly is used when the local oscillator operates in either multiple loop mode or single loop mode (see figures 8-12 and 8-13). In single loop mode, this assembly provides the control voltage for the single loop. In multiple loop mode, this assembly provides the control voltage for the interpolation loop. Figure 8-23 shows the Fractional-N assembly's block diagram.

The **Divide-by-N** circuit divides the fractional-N VCO signal down to 100 kHz.

The **Phase Comparator** compares the signal from the Divide-by-N with the 100 kHz reference signal and generates a pulse equal to the phase difference.

The **Integrator** and **Sample and Hold** circuits convert the phase-difference pulses to a dc voltage. A service adjustment minimizes the 100 kHz sample and hold spur.

The **API** (Analog Phase Interpolation) **Current Control** discharges the Integrator to help maintain a steady dc state. There are also service adjustments to minimize API spurs.

The **Multiple Loop Buffer** conditions the dc voltage and provides it as the control voltage for the interpolation loop.

The **Single Loop Buffer** conditions the dc voltage and provides it as the control voltage for the single loop. The Single Loop Buffer also clamps the control voltage if its amplitude is not within the approximate range of –2 to +7V. A service adjustment sets the range of the voltage clamps.

The **Fractional-N** integrated circuit controls the Divide-by-N, API Current Control, and Sample and Hold. The negative edge of the sweep synchronization signal (LSWP\) causes this circuit to start a sweep. During gated-sweep measurements, the gated-sweep synchronization signal (GSWP) is used with LSWP\ to control sweeping for each gate.

The **Interface** circuit provides the interface between the CPU assembly and the Fractional-N assembly. The Frac-N bus signals, CF_REG, CF_STB, and CF_0 through CF_3, are fast bus signals from the CPU assembly that were buffered and latched on the ADC/Digital Filter assembly. The Interface circuit uses CPU instructions, the LSWP\ signal, and the GSWP signal to provide control lines to the Fractional-N circuit.

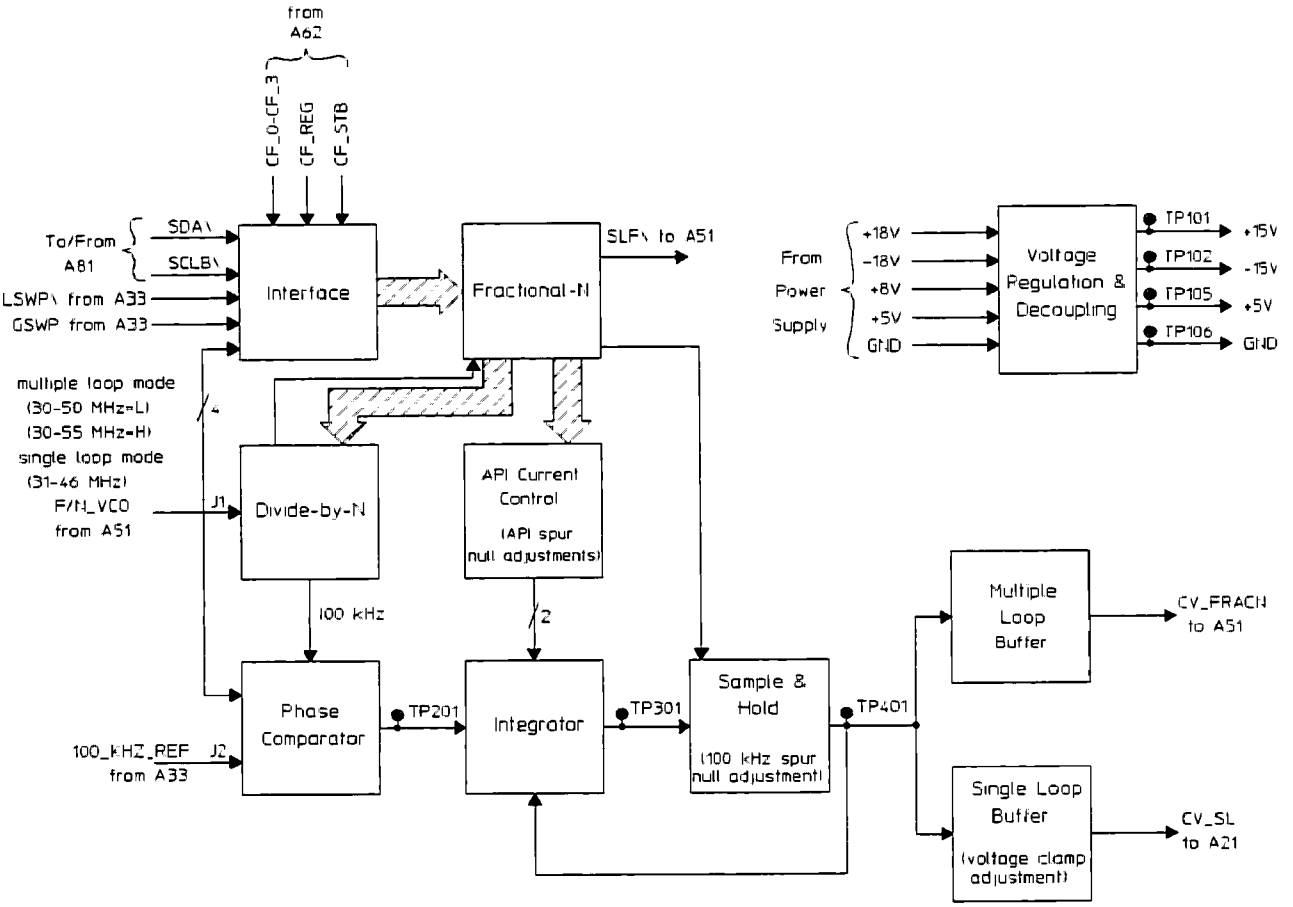


Figure 8-23. A52 Fractional-N Block Diagram

A61 IF

The IF assembly is the fourth of five assemblies that condition the input signal. This assembly converts the output of the Second Frequency Conversion assembly to the third IF signal. Figure 8-24 shows the IF assembly's block diagram.

The **Second IF Amplifier/Filter** amplifies and filters the second IF signal. Also, the analyzer's internal self-test routines use this circuit to detect if the second IF signal is approximately 15 dB over full scale. The filter in this circuit is service-adjustable.

The **10 MHz Reference Receiver** buffers the 10 MHz reference signal. If the 10 MHz reference signal is not present, the Fault Detector on the ADC/Digital Filter assembly interrupts the CPU assembly.

The **Third Conversion Mixer** mixes the second IF signal with the 10 MHz reference signal. This circuit contains a service adjustment to set the gain of the second IF signal.

The **Third IF Filter** then amplifies and filters the resulting 187.5 kHz signal.

The **Third IF Amplifier/Attenuator** amplifies and, under CPU control, subsequently attenuates the signal so that the maximum signal possible (without causing an overload) is available at the analog-to-digital converter (ADC) on the ADC/Digital Filter assembly.

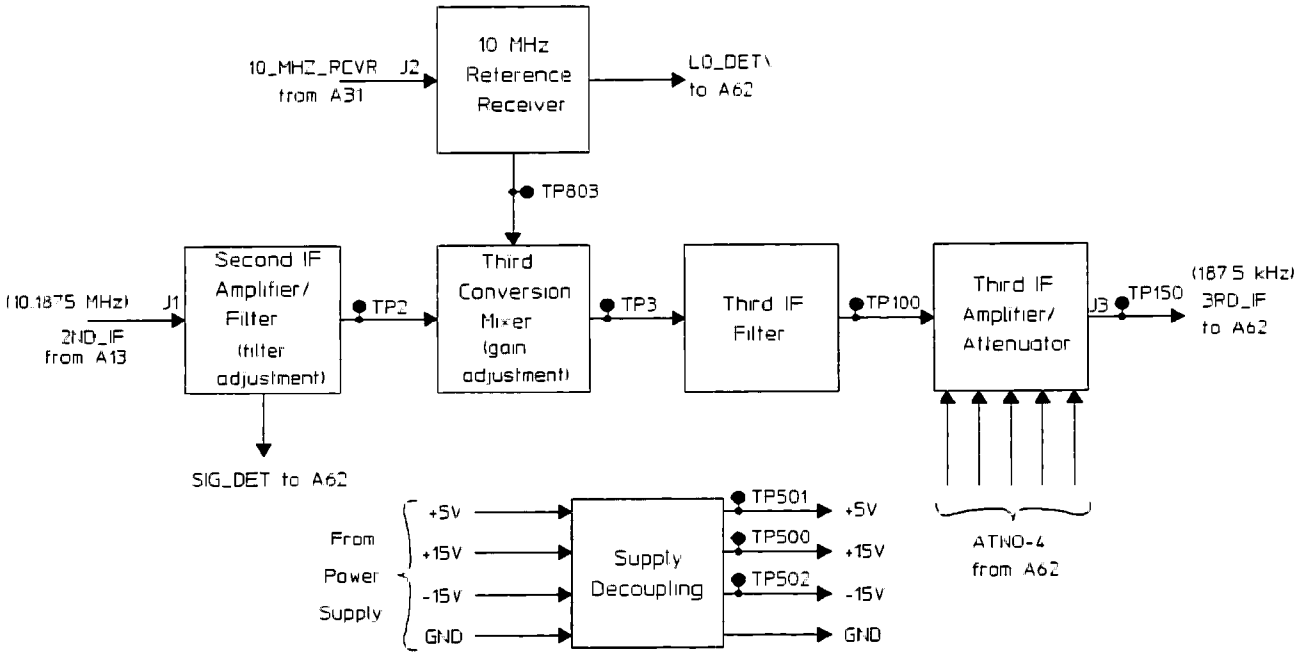


Figure 8-24. A61 IF Block Diagram

A62 ADC/Digital Filter

The ADC/Digital Filter assembly is the last of five assemblies to condition the input signal. This assembly converts the output of the IF assembly to digital data. The digital data is then digitally filtered and detected, then sent to the CPU assembly over the fast bus. Figure 8-25 shows the ADC/Digital Filter assembly's block diagram.

The **Track and Hold** circuit holds a voltage sample of the 187.5 kHz IF signal for the period of time required by the ADC to digitize the voltage.

The **ADC** circuit converts the voltage to a 13-bit digital word at a 250 kHz sample rate. After a complete conversion cycle, the ADC serially transfers the digital word to the Digital Filter.

The ADC circuit converts the voltage to a 13-bit digital word by passing the signal through an 8-bit A/D converter twice. On the first pass, the voltage is divided by four, then level shifted. Then dither (noise) is added to increase the accuracy of the analog-to-digital conversion. The 8-bit A/D converter converts the voltage to an 8-bit digital word. This first-pass word is converted back to a voltage and compared with the original voltage. A difference voltage is generated and converted to an 8-bit word. The second-pass word is added to the first-pass word, resulting in a 13-bit digital word that represents the IF signal.

The ADC circuits contain three service adjustments — one to null dc offset, one to set the reference voltage, and one to match the gain between the two conversion passes.

The **Digital Filter** circuit digitally mixes the 13-bit word with a 62.5 kHz sine wave and a 62.5 kHz cosine wave. (The 62.5 kHz signals result from dividing the 250 kHz sample clock by four.) The result of this digital mixing is two data streams — one representing the real part of the IF signal and the other representing the imaginary part of the IF signal. This circuit also provides the final resolution bandwidth filtering for each data stream.

The **Detector** sends the data streams from the Digital Filter to the CPU assembly over the fast bus. The Detector also squares the output of both digital filters, adds the squared values together, and sends the result to the CPU assembly.

The **Fractional-N Bus Interface** provides an interface between the Fractional-N assembly and the ADC/Digital Filter assembly. This circuit buffers and latches four fast bus data lines (FD0 to FD3) and one fast bus address line (FA1). A data strobe (CF_STB) writes the latched data lines (CF_0 to CF_3) and latched address line (CF_REG) to the Fractional-N assembly.

The **Reset Receivers** buffer the reset signal, the sweep synchronization signal, and the detect gate signal. The reset signal (RESET\) resets the ADC, Digital Filter, and Detector. The sweep synchronization signal (LSWP\) resets the phase of the gate arrays in the Digital Filter and initiates data transfer from the Detector. The detect gate signal (DET_GATE) controls the transfer of data between the Digital Filter and the Detector during gated-sweep measurements.

The **Sample Clock Receiver** buffers the 250 kHz reference signal and sends it to the ADC as the sample rate.

The **20 MHz Clock** divides the 80 MHz reference signal by four, creating two 20 MHz signals in quadrature (90 degree phase relationship). These signals provide the clock signals for the ADC, Digital Filter, Detector and the external clock signal for the CPU assembly. The external clock signal is sent to the CPU assembly over the fast bus. If this external clock signal is not present, the fast bus is disabled.

The **Fault Detection** circuit detects the presence of the 10 MHz reference and the input signal at the IF assembly. It also detects the presence of the 250 kHz reference and the 20 MHz clocks. This information is sent to the IIC Interface.

The **IIC Interface** provides the interface between the CPU assembly and the ADC/Digital Filter assembly. It also provides the interface between the CPU assembly and the IF assembly. If the 10 MHz reference, 250 kHz reference, or 20 MHz clock is not present, the IIC Interface interrupts the CPU assembly.

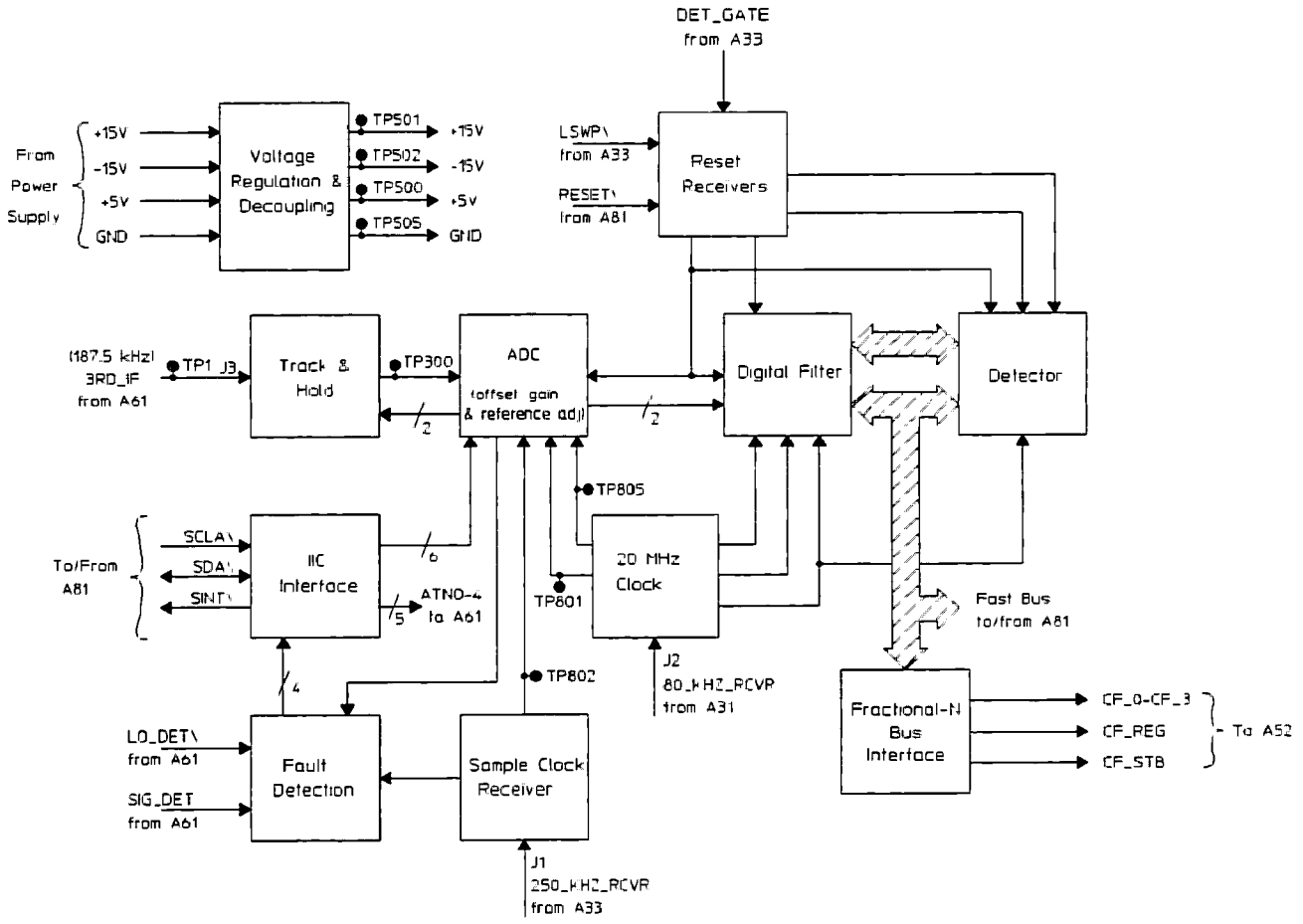


Figure 8-25. A62 ADC/Digital Filter Block Diagram

A81 CPU

The CPU assembly controls the entire analyzer. It performs multiple tasks, such as:

- Initiating the power-up sequence and calibration routines
- Capturing front panel keystrokes
- Configuring the measurement hardware
- Processing input data from the ADC/Digital Filter assembly
- Controlling the display
- Monitoring the hardware for faults or overloads
- Running the self tests
- Handling all data transfers for the fast bus, HP-IB, and Disk Drive assembly

Figure 8-26 shows the CPU assembly's block diagram. Figure 8-27 shows the CPU interface's block diagram.

The **MPU** (Microprocessor) controls the processor address bus and the buffered processor data bus. At power-up, this circuit initializes the analyzer from the information stored in the Monitor ROM. This circuit also processes interrupts from the Interrupt Handler and synchronizes data transfers on the processor data bus with the Data Transfer Handler. The MPU also has access to battery-backed-up SRAM on the Memory assembly. This allows the CPU assembly to store and update information such as the analyzer's address, default disk, and peripheral addresses.

The **DMA** (Direct Memory Access) **Controller** handles all DMA data transfers and controls the fast bus that connects the ADC/Digital Filter assembly to the CPU assembly. When a DMA data transfer occurs, the DMA Controller circuit takes control of the processor address and data busses. When the DMA data transfer is finished, the DMA Controller returns control of the busses to the MPU. Throughput from the ADC/Digital Filter assembly to the Memory assembly or to the Disk Drive assembly are examples of DMA data transfers.

The **TMS320** relieves the MPU of math intensive-tasks by supplying the computational power needed for accurate, high-speed signal processing operations — for example, windowing and Fast Fourier Transform (FFT) for the analyzer's narrow-band zoom mode. The TMS320 is a high speed (40 MHz) math co-processor that performs complex mathematical operations. It works as a slave co-processor to the MPU (68000), and it has its own Program RAM and Data RAM. This arrangement leaves the MPU free to perform other functions while the TMS320 performs math-intensive operations.

The **Interrupt Handler** processes interrupts for the MPU. It sets the interrupt priority level and returns an interrupt acknowledge to the circuit that generated the interrupt. If the MFP controller causes an interrupt, the MPU reads a status byte from the MFP controller to determine the circuit that caused the interrupt.

The **Data Transfer Handler** synchronizes data transfers in the analyzer with the MPU. When a data transfer occurs, the Data Transfer Handler notifies the MPU when the transfer is complete.

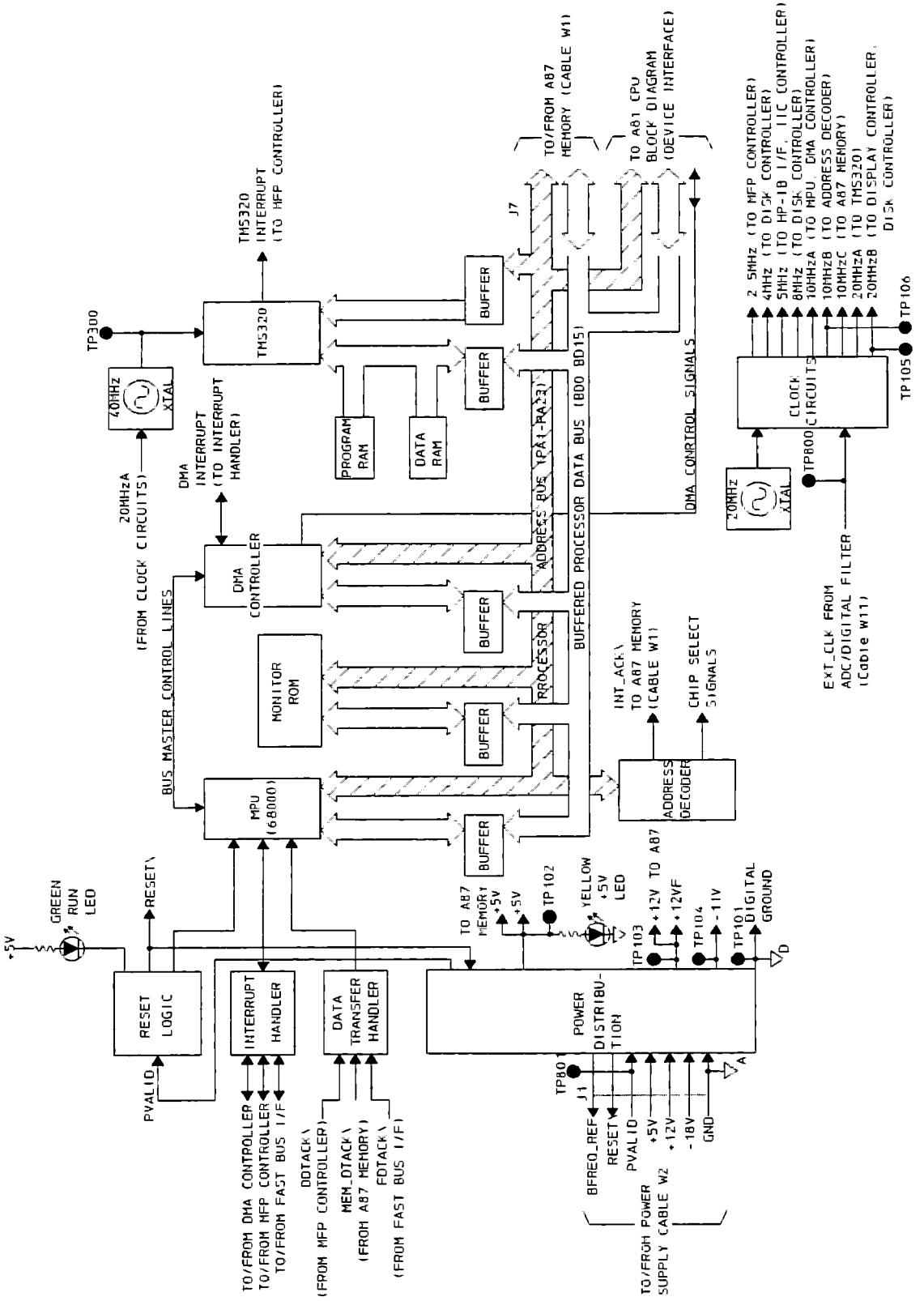


Figure 8-26. A81 CPU Block Diagram

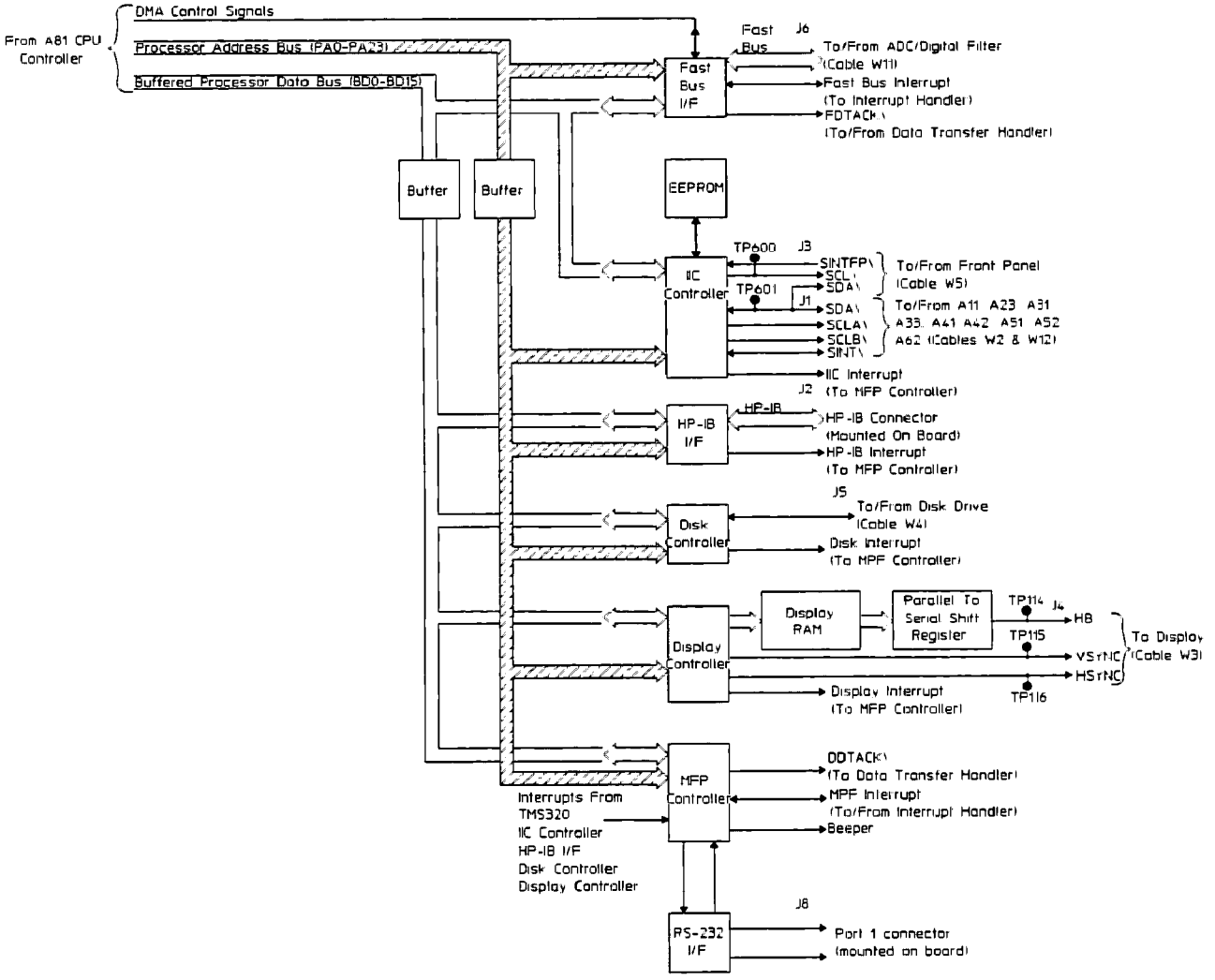


Figure 8-27. A81 CPU Interface Block Diagram

The **Clock Circuits** provide the clocks for the CPU, Disk Drive, and Memory assemblies. If the external clock from the ADC/Digital Filter assembly is present, this circuit synchronizes the CPU assembly with the rest of the analyzer.

The **MFP** (Multiple-Function Peripheral) **Controller** handles interrupts and handshaking during data transfers for the following circuits:

- TMS320
- IIC Controller
- HP-IB Interface
- Disk Controller
- Display Controller
- RS-232 Interface

Interrupts from these circuits are sent to the MFP Controller. When the MFP Controller receives an interrupt, it interrupts the Interrupt Handler, which in turn interrupts the MPU. The MPU then reads a status byte from the MFP Controller to determine the cause of the interrupt. The MFP Controller also tells the Data Transfer Handler if any data transfers occurred for these circuits.

The **RS-232 Interface** allows the analyzer to communicate with the test set.

The **Reset Logic** puts the analyzer into a known state (see figure 8-28). A reset occurs at power up (PVALID from the Power Supply assembly goes high), when the reset switch SW101 (located on the CPU assembly) is pressed, or when the MPU receives a reset instruction.

A low-to-high transition on pin 18 of the MPU causes the MPU to execute its reset routine (stored in ROM). When the MPU completes its reset routine, it forces RST\ high (notice that pin 18, RST\, of the MPU is bidirectional). This in turn forces RESET\ high, which tells the other assemblies that the reset routine is finished.

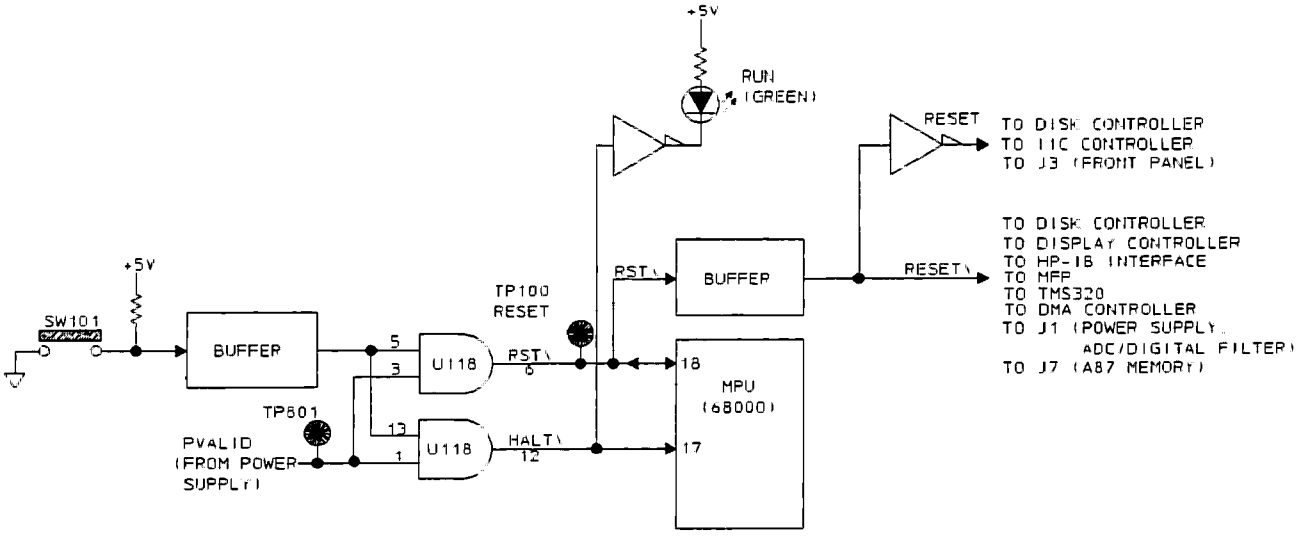


Figure 8-28. Reset Logic

The **Fast Bus Interface** connects the CPU assembly to the fast bus. All data transfers between the ADC/Digital Filter assembly and the CPU assembly occur over the fast bus. The fast-bus address lines (FA0 through FA5) and data lines (FD0 through FD15) are simply extensions of the processor address and data busses. This allows fast DMA transfers between the two assemblies. See "W11 Fast Bus Cable" (in chapter 9) for a description of the fast bus signals.

The **IIC** (Inter-IC) **Controller** manages the IIC bus. It allows direct communication between the CPU assembly and the following assemblies via the IIC bus:

- Front Panel
- Input
- Step Phase Detector
- Reference/Calibrator
- Trigger
- Source Amplifier
- Source Conversion
- Interpolation VCO
- Fractional-N
- ADC/Digital Filter
- Memory

All of these assemblies appear as slaves to the IIC Controller. The IIC Controller has access to an EEPROM, which allows the CPU assembly to store information such as the analyzer's serial number and IBASIC option. If the CPU assembly is replaced, the analyzer's serial number, IBASIC option, and Time-Gated Spectrum Analysis option must be stored in EEPROM on the new assembly (see "Replacing the CPU Assembly" in chapter 6). The IIC Controller also has access to a battery backed real-time clock on the Memory assembly.

The IIC bus consists of the following six signal lines:

- SCL\ (serial clock)
- SCLA\ (serial clock)
- SCLB\ (serial clock)
- SDA\ (serial data)
- SINT\ (serial interrupt)
- SINTFP\ (serial interrupt for Front Panel assembly)

Pull-up resistors connect these signals to logic high (all six lines are open collector or open drain). See "W5 Front Panel Cable" and "W12 Motherboard Power Cable" in chapter 9 for descriptions of the IIC signals.

The **HP-IB Interface** allows the analyzer to communicate with other devices such as plotters, printers, or a host computer via an HP-IB cable. This circuit handles all HP-IB functions for the analyzer. The analyzer's HP-IB connector is located on the CPU assembly.

The **Disk Controller** allows the analyzer to store or retrieve data from the internal 3.5-inch flexible Disk Drive assembly. It provides all the control signals necessary to operate the Disk Drive assembly. The Disk Controller performs the following functions:

- Turns on the disk drive motor
- Selects the disk drive head
- Turns on the disk drive LED
- Selects a track on the flexible disk
- Writes or reads serial data from the flexible disk

The Disk Controller puts data on the flexible disk in a bit stream that consists of data and clock bits. When data is read from the disk, this circuit separates the data bits from the clock bits, converts the serial data bits to an 8-bit parallel word, and puts the data word on the processor data bus. The operation is reversed when data is written to the disk.

The **Display Controller** positions information on the analyzer's display. The Display Controller takes parallel data from the processor data bus and places the data in display RAM (four 64K × 4-bit RAM chips). One bit in display RAM corresponds to one pixel on the display. The data in display RAM is then sent to a parallel-to-serial shift register. The shift register continuously updates the display with the contents of display RAM. The Display Controller also supplies the horizontal and vertical sync signals for the display, and it determines if the data on the display is full bright or half bright.

A87 Memory and A88 Expanded Memory

The Memory assembly provides the CPU assembly with flash EPROM, dynamic RAM, static RAM, and a real-time clock (see figure 8-29). The Memory assembly also provides battery backup for the static RAM and real-time clock. Memory is divided into 16-bit words. To access a memory location, the CPU assembly puts the address of the desired 16-bit word on the processor address bus. The CPU assembly can then read from (or write to) this memory location.

The optional Expanded Memory assembly replaces the Memory assembly, plus provides an additional two megabytes of RAM.

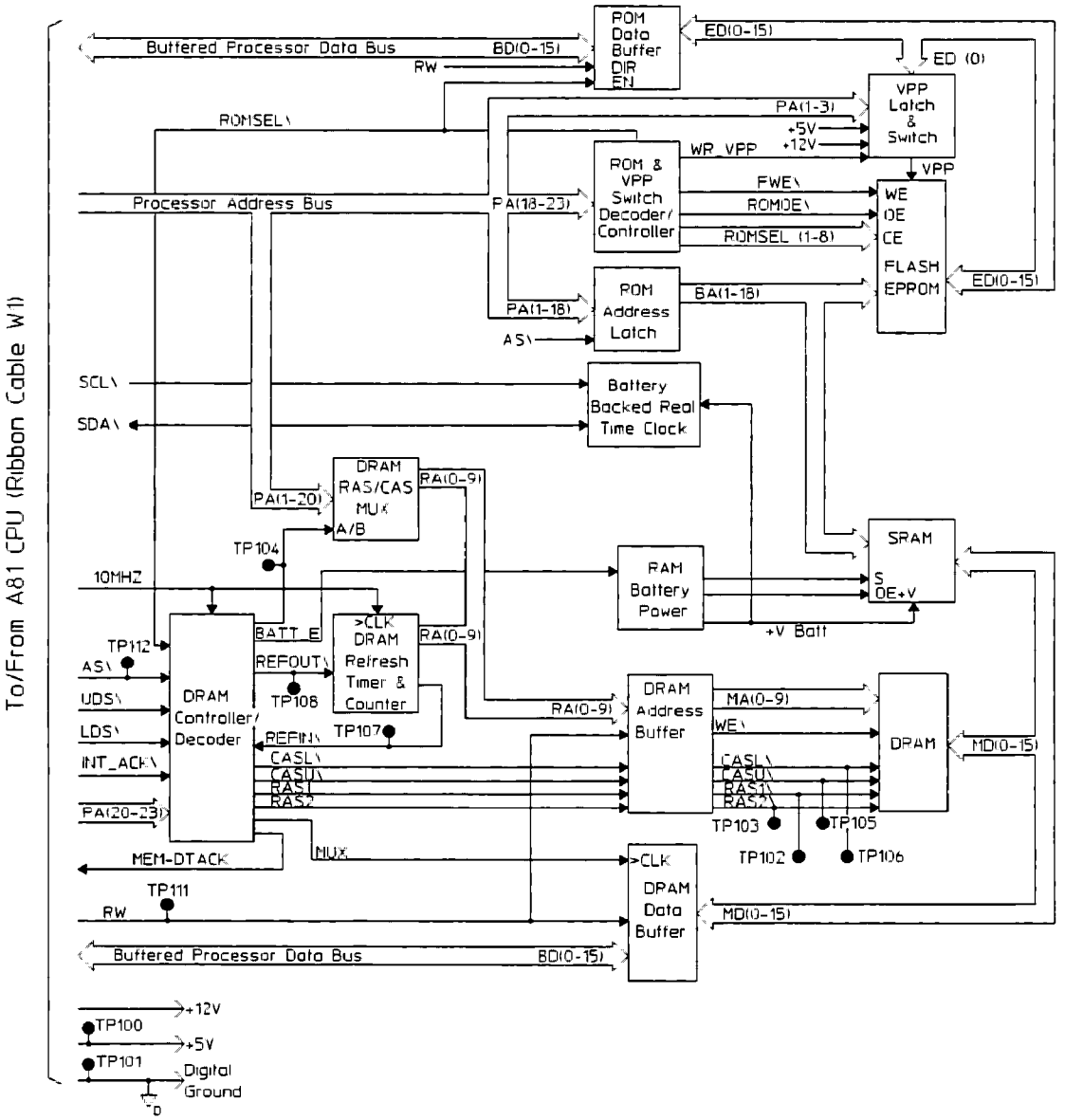


Figure 8-29. Memory and Expanded Memory Block Diagram

A90 Fan Power and A91 Fan Power/Oven

The Fan Power assembly provides power to the fan, which cools the card-nest side of the analyzer.

The optional Fan Power/Oven assembly provides power to the fan, which cools the card-nest side of the analyzer, and provides a stable 10 MHz frequency reference to the rear panel (OVEN REF OUT). During the oven warm-up cycle, oven reference output is disabled and the analyzer uses its internal crystal reference. When the oven reaches the proper operating temperature (about 10 minutes after power-up), oven reference output is automatically enabled. A BNC-to-BNC jumper connects the OVEN REF OUT connector to the EXT REF IN connector on the rear panel.

A99 Motherboard

The Motherboard assembly provides a common point of contact for voltage and signal distribution. This assembly filters some voltages and signals, and also provides power for the active probe connector on the front panel (+15V and –13V, derived from the analyzer's ± 15V supply). See "Motherboard Signals" in chapter 9 for a list of all signals that are distributed via the Motherboard assembly.

Front Panel

The Front Panel assembly sends information to the analyzer. This assembly consists of all the keys on the instrument's front panel (except for the power switch), the RPG, an external DIN keyboard connector, and an IIC interface. When a front panel key or external keyboard key is pressed or the RPG is turned, the IIC interface interrupts the CPU assembly. The CPU assembly then addresses the IIC interface and reads an 8-bit frame of data from the IIC bus to determine which key was pressed (for information about the IIC bus, see the description of the IIC Controller in "A81 CPU" earlier in this chapter).

Power Supply

The Power Supply assembly is a switching power supply that provides the voltages for all the assemblies in the analyzer. See "Power Supply Voltage Distribution" in chapter 9 for a list of these voltages and the assemblies that use each voltage.

Disk Drive

The internal Disk Drive assembly stores and retrieves information from 3.5-inch flexible disks. This assembly is mounted on (and controlled by) the CPU assembly. See the description of the Disk Controller in "A81 CPU" (earlier in this chapter) for further details.

Display

The Display assembly shows processed data sent by the CPU assembly. See the description of the Display Controller in "A81 CPU" (earlier in this chapter) for further details.

HP 35689A/B S-Parameter Test Set

The HP 35689A/B is a 100 kHz to 150 MHz S-parameter (scattering parameter) test set. The HP 35689A is designed for measuring 50-ohm devices while the HP 35689B is designed for measuring 75-ohm devices. The test set extends the measurement capability of the HP 3589A Spectrum/Network Analyzer and lets the analyzer make S-parameter measurements much faster by automatically selecting the appropriate combination of directional couplers. The test set also has a separate spectrum input that allows the analyzer to make spectrum measurements without disconnecting the test set.

Overall Block Diagram

Figure 8-24 shows the overall block diagram for the HP 35689A/B. Each block represents a functional block in the instrument. The assembly that performs the function is listed in the block.

The **Controller** provides the interface between the analyzer and the test set. The Controller decodes the instructions from the analyzer and sets the relays on the RF assembly. The A2 Controller assembly is used in both the HP 35689A and HP 35689B.

The **RF** assembly contains the relays that route the signal through the selected signal path. The A1 50 Ohm RF assembly is used in the HP 35689A and the A11 75 Ohm RF assembly is used in the HP 35689B.

The **Directional Bridges** are either 50 Ω or 75 Ω directional couplers. Two A3 50 Ohm Directional Bridges are used in the HP 35689A and two A4 75 Ohm Directional Bridges are used in the HP 35689B.

The **LED** assembly contains LEDs that indicate which mode the test set is in — forward or reverse. The A5 LED assembly is used in both the HP 35689A and HP 35689B.

The **Power Supply** provides +5 and +15 volts to the RF assembly and +5 volts to the Controller and LED assemblies. The A6 Power Supply is used in both the HP 35689A and HP 35689B.

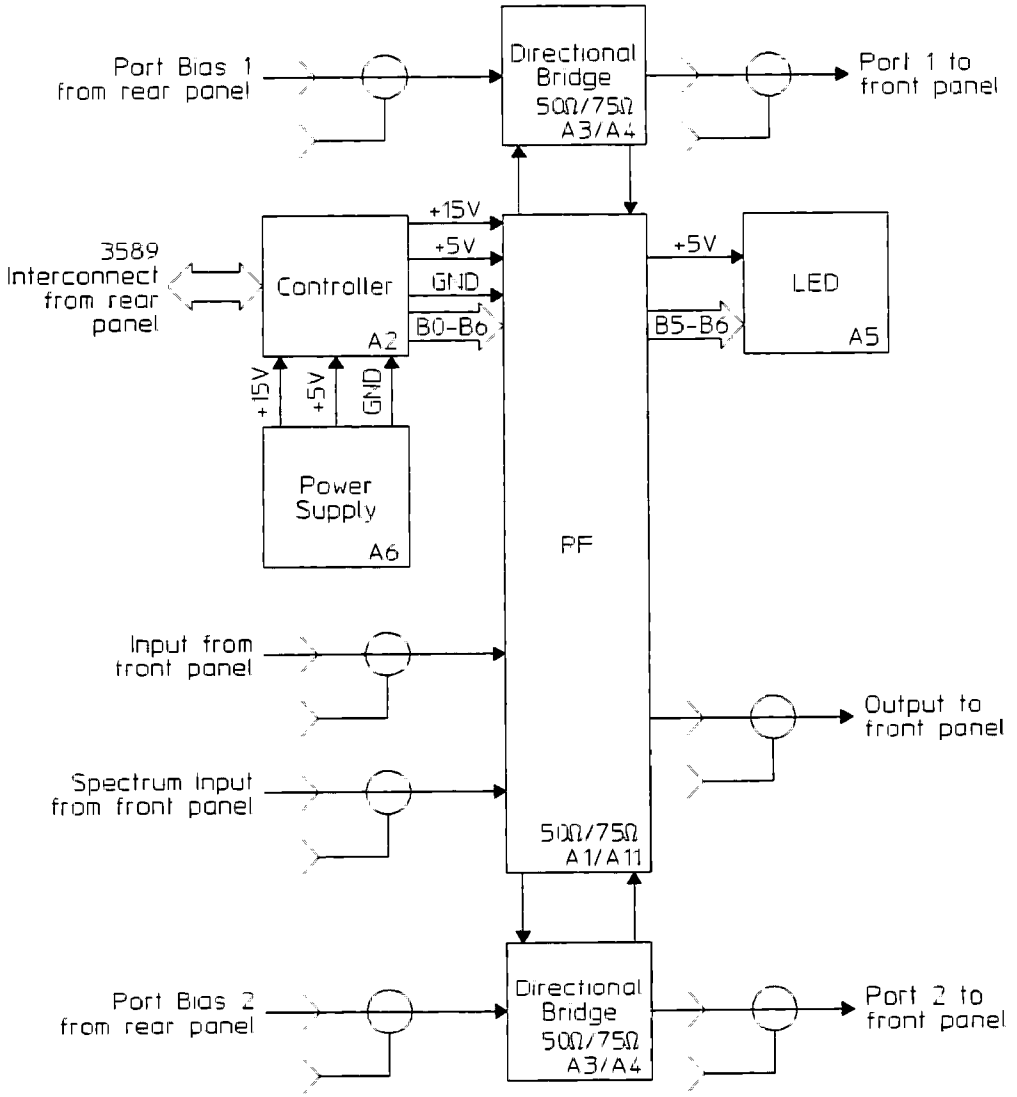


Figure 8-30. HP 35689A/B Overall Block Diagram

A1 50 Ohm RF

The A1 50 Ohm RF assembly is used in the HP 35689A S-Parameter Test Set. The 50 Ohm RF assembly contains the relays that route the signal through the selected signal path (see figure 8-31). Two A3 Directional Bridge assemblies are in the signal paths. In spectrum configuration, the signal is routed from the SPECTRUM INPUT to the OUTPUT. In reference configuration, the signal is routed from the INPUT through the Reference path to the OUTPUT. In forward reflection configuration (for S_{11} measurements), the signal is routed from the INPUT to PORT 1 and the signal at coupled port 1 is routed to the OUTPUT. In reverse reflection configuration (for S_{22} measurements), the signal is routed from the INPUT to PORT 2 and the signal at coupled port 2 is routed to the OUTPUT. In reverse transmission configuration (for S_{12} measurements), the signal is routed from the INPUT to PORT 2 and the signal at coupled port 1 is routed to the OUTPUT. In forward transmission configuration (for S_{21} measurements), the signal is routed from the INPUT to PORT 1 and the signal at coupled port 2 is routed to the OUTPUT. The amplitude loss from the INPUT to PORT 1 or PORT 2 is approximately 13 dB. The amplitude loss from PORT 1 or PORT 2 to the OUTPUT is approximately 6 dB. The amplitude loss from the INPUT to the OUTPUT through the reference path is approximately 19 dB.

The **Input Switching** circuit routes the analyzer's source to one of the Directional Bridges or to the Reference Path. During reference measurements, this circuit routes the signal to the Reference Path. During S_{11} and S_{21} measurement, this circuit routes the signal to PORT 1. During S_{12} and S_{22} measurements, this circuit routes the signal to PORT 2.

The **Reference Path** provides a 19 dB loss to match the loss in S_{11}, S_{12}, S_{21}, and S_{22} measurements.

Output Termination routes one signal to Output Switching and terminates the other two signal paths.

Output Switching selects the signal on the reference path, the coupled port 1 path, or the coupled port 2 path. During reference measurements, this circuit selects the signal on the reference path. During S_{11} and S_{12} measurements, this circuit selects the signal on the coupled port 1 path. During S_{21} and S_{22} measurements, this circuit selects the signal on the coupled port 2 path.

The **Test Set Bypass** selects either the signal from Output Switching or from the SPECTRUM INPUT connector. The spectrum input signal path allows the analyzer to make spectrum measurements without disconnecting the test set from the analyzer.

The **Relay Control Latch** sets the relay positions. The relay control lines are from the A2 Controller.

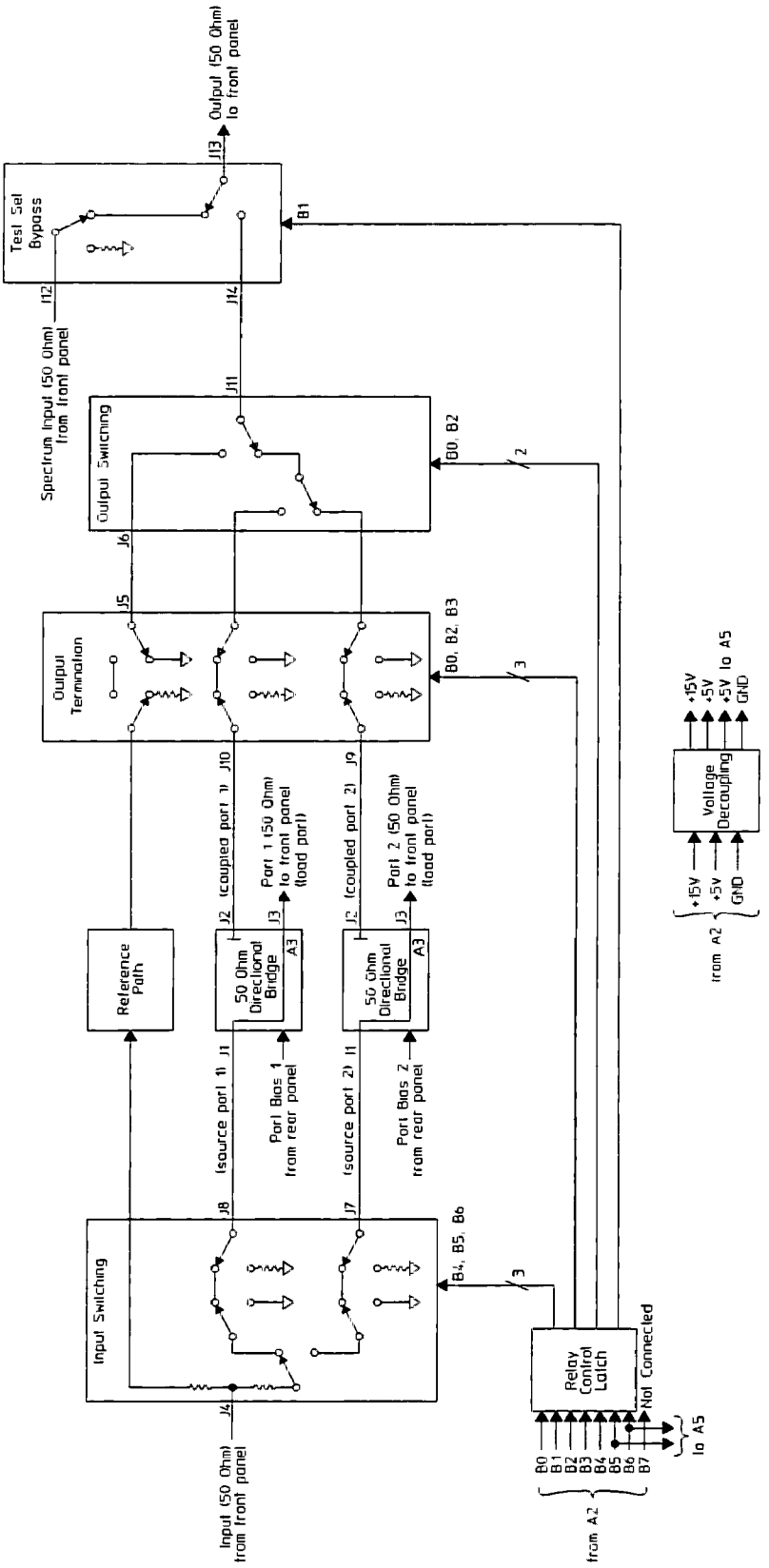


Figure 8-31. A1 50 Ohm RF Block Diagram

A2 Controller

The A2 Controller assembly is used in both the HP 35689A and HP 35689B S-Parameter Test Set. The A2 Controller assembly provides the interface between the analyzer and test set. The analyzer's CPU assembly controls the test set using the RS-232 receive data line. The Controller assembly decodes the RS-232 receive data line providing the relay control lines to the RF assembly. In the loopback self test, this assembly encodes the relay control lines providing the RS-232 transmit data line to the analyzer's CPU assembly.

A3 50 Ohm Directional Bridge

Two A3 50 Ohm Directional Bridge assemblies are used in the HP 35689A S-Parameter Test Set. See "A1 50 Ohm RF" for signal routing information. The 50 Ohm Directional Bridge assembly produces a voltage at its coupled port proportional to the amount of reflection along a transmission line or at its output port. The rear panel Port Bias connector can supply bias voltages to devices connected to the Directional Bridge's output port.

A4 75 Ohm Directional Bridge

Two A4 75 Ohm Directional Bridge assemblies are used in the HP 35689B S-Parameter Test Set. See "A11 75 Ohm RF" for signal routing information. The 75 Ohm Directional Bridge assembly produces a voltage at its coupled port proportional to the amount of reflection along a transmission line or at its output port. The rear panel Port Bias connector can supply bias voltages to devices connected to the Directional Bridge's output port.

A5 LED

The A5 LED assembly is used in both the HP 35689A and HP 35689B S-Parameter Test Set. The LED assembly contains LEDs that indicate which mode the test set is in — forward (S_{11} or S_{21}) or reverse (S_{12} or S_{22}).

A6 Power Supply

The A6 Power Supply assembly is used in both the HP 35689A and HP 35689B S-Parameter Test Set. The Power Supply assembly provides +5 and +15 volts. The Controller assembly uses +5 volts and routes both +5 and +15 volts to the RF assembly. The RF assembly uses +5 and +15 volts and routes +5 volts to the LED assembly.

A11 75 Ohm RF

The A11 75 Ohm RF assembly is used in the HP 35689B S-Parameter Test Set. The 75 Ohm RF assembly contains the relays that route the signal through the selected signal path (see figure 8-32). Two A4 Directional Bridge assemblies are in the signal paths. In spectrum configuration, the signal is routed from the SPECTRUM INPUT to the OUTPUT. In reference configuration, the signal is routed from the INPUT through the Reference path to the OUTPUT. In forward reflection configuration (for S_{11} measurements), the signal is routed from the INPUT to PORT 1 and the signal at coupled port 1 is routed to the OUTPUT. In reverse reflection configuration (for S_{22} measurements), the signal is routed from the INPUT to PORT 2 and the signal at coupled port 2 is routed to the OUTPUT. In reverse transmission configuration (for S_{12} measurements), the signal is routed from the INPUT to PORT 2 and the signal at coupled port 1 is routed to the OUTPUT. In forward transmission configuration (for S_{21} measurements), the signal is routed from the INPUT to PORT 1 and the signal at coupled port 2 is routed to the OUTPUT. The amplitude loss from the INPUT to PORT 1 or PORT 2 is approximately 19 dB. The amplitude loss from PORT 1 or PORT 2 to the OUTPUT is approximately 12 dB. The amplitude loss from the INPUT to the OUTPUT through the reference path is approximately 31 dB.

The **Input Switching** circuit routes the analyzer's source to one of the Directional Bridges or to the Reference Path. During reference measurements, this circuit routes the signal to the Reference Path. During S_{11} and S_{21} measurement, this circuit routes the signal to PORT 1. During S_{12} and S_{22} measurements, this circuit routes the signal to PORT 2.

The **Reference Path** provides a 31 dB loss to match the loss in S_{11}, S_{12}, S_{21}, and S_{22} measurements.

Output Termination routes one signal to Output Switching and terminates the other two signal paths.

Output Switching selects the signal on the reference path, the coupled port 1 path, or the coupled port 2 path. During reference measurements, this circuit selects the signal on the reference path. During S_{11} and S_{12} measurements, this circuit selects the signal on the coupled port 1 path. During S_{21} and S_{22} measurements, this circuit selects the signal on the coupled port 2 path.

The **Test Set Bypass** selects either the signal from Output Switching or from the SPECTRUM INPUT connector. The spectrum input signal path allows the analyzer to make 75 Ω spectrum measurements without disconnecting the test set from the analyzer.

The **Relay Control Latch** sets the relay positions. The relay control lines are from the A2 Controller.

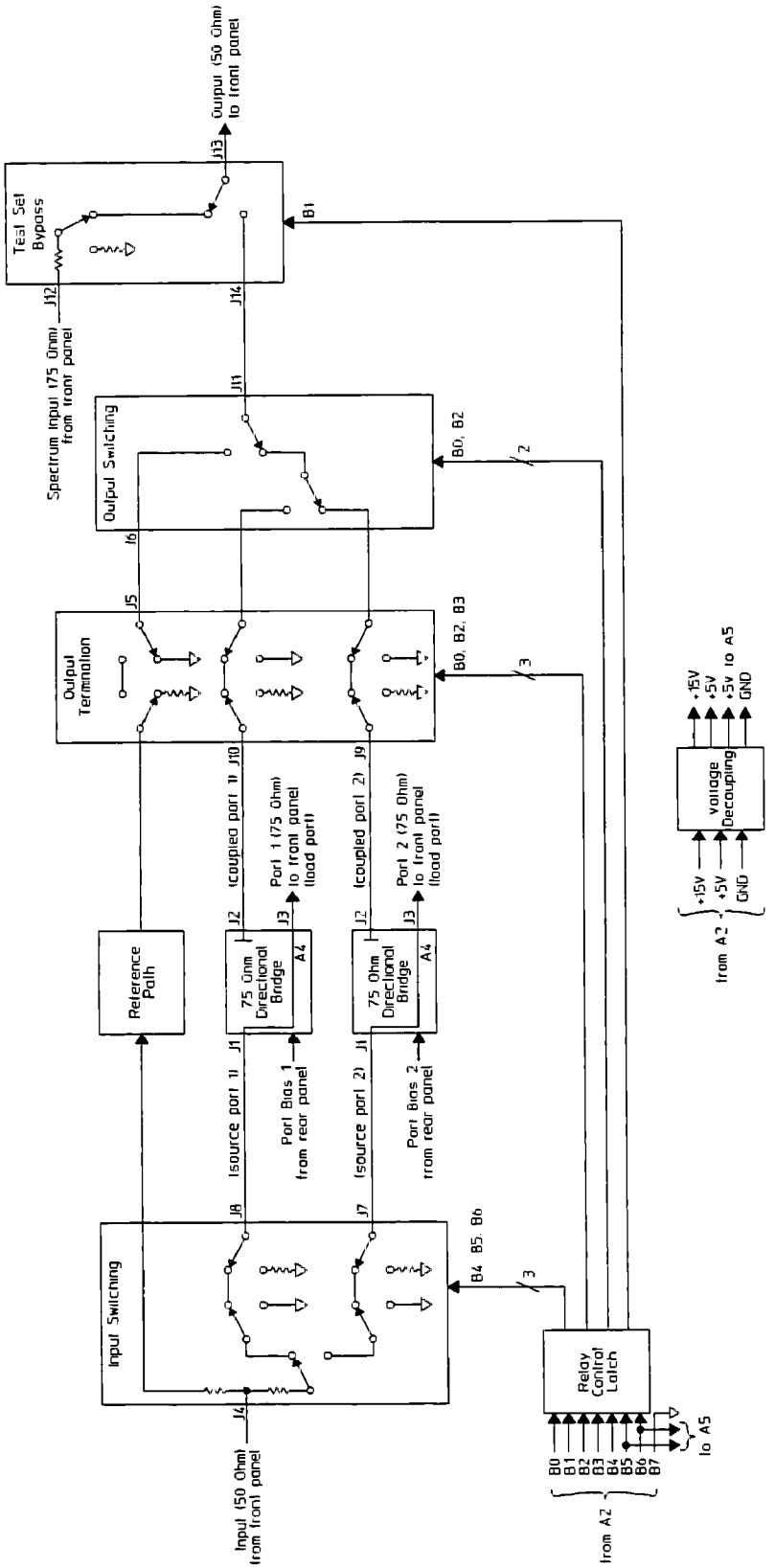


Figure 8-32. A11 75 Ohm RF Block Diagram

9 Voltages & Signals

9

Voltages and Signals

Introduction

This chapter shows where the signals and voltages are used in the HP 3589A Spectrum/Network Analyzer and the HP 35689A/B S-Parameter Test Set. This chapter also describes each signal.

Note Signals with a mnemonic that ends with a "\" are active low.

HP 3589A Spectrum/Network Analyzer

The following figures show assembly locations and ribbon cable connections for the HP 3589A Spectrum/Network Analyzer.

Assemblies

A11 Input
A12 First Conversion
A13 Second Conversion
A21 Sum VCO
A22 Sum Phase Detector
A23 Step Phase Detector
A24 Step VCO
A31 Reference/Calibrator
A32 300 MHz
A33 Trigger
A41 Source Amplifier
A42 Source Conversion
A51 Interpolation VCO
A52 Fractional-N
A61 IF
A62 ADC/Digital Filter
A81 CPU
A87 Memory
A88 Expanded Memory
A90 Fan Power
A91 Fan Power/Oven
A99 Motherboard

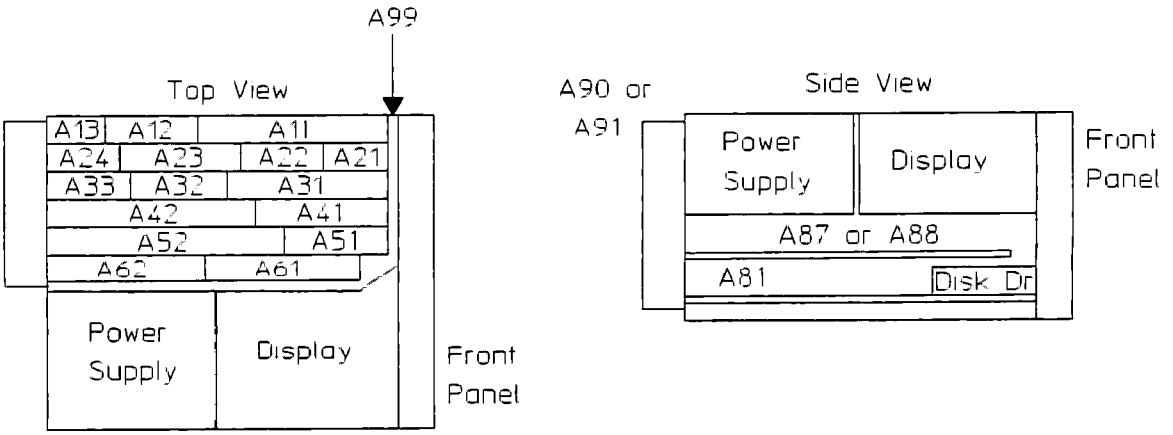


Figure 9-1. Assembly Locations

Cables

W1 Memory
W2 CPU Power
W3 Display
W4 Disk Drive
W5 Front Panel
W11 Fast Bus
W12 Motherboard Power

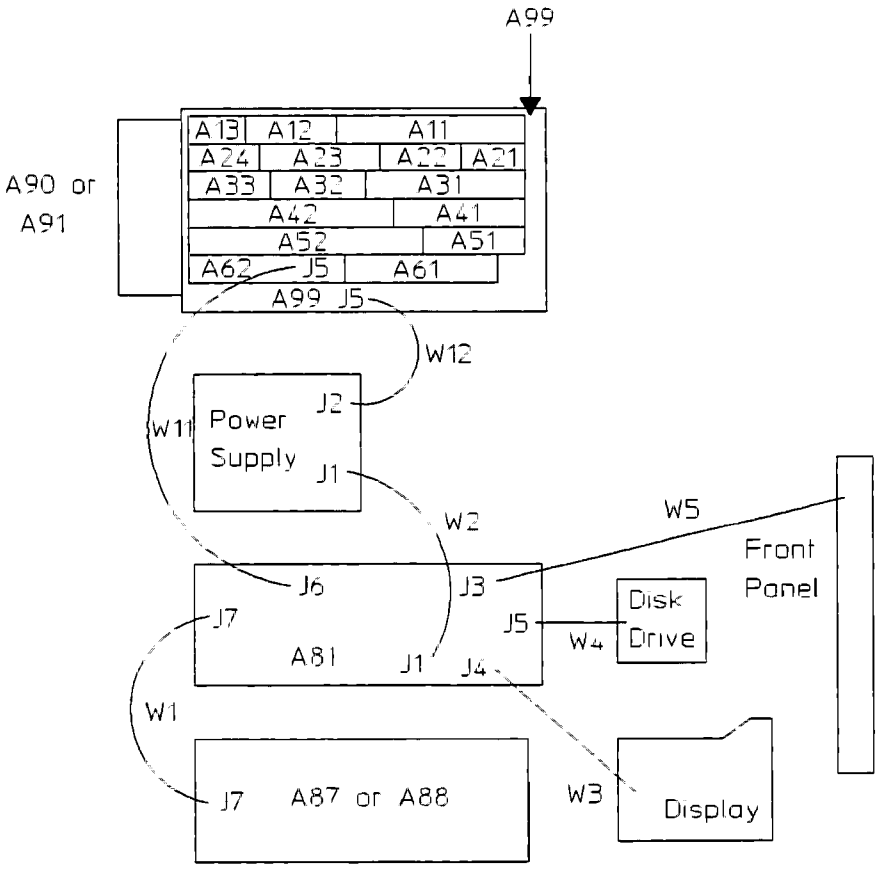


Figure 9-2. Ribbon Cable Connections

Power Supply Voltage Distribution

Table 9-1 shows the power supply voltages used by each assembly in the analyzer. In addition, the table also shows the path taken by these voltages and the location of individual test points. Some assemblies use the power supply voltages as supplied by the Power Supply assembly. However, most assemblies contain voltage regulation and voltage decoupling circuits to provide additional regulation and decoupling for their own use.

Table 9-1. Power Supply Voltage Distribution

From	Path	To	Voltages							
			+18V	+15V	+12V	+8V	+5V	-15V	-18V	Gnd
Pwr Supply J1	W2	A81 J1			√		TP102		√	TP101
	W2/A81/W1	A87/A88 J7			√		TP100			TP101
	W2/A81/W3	Display			√		√			√
	W2/A81/W4	Disk Drive			√		√			√
	W2/A81/W5	Front Panel					√			√
Pwr Supply J2	W12	A99 J5	√	√		√	√	√	√	√
	W12/A99	A11 J5		TP202			TP201	TP203		TP200
		A12 J4		TP803		TP802	TP801	TP804		TP800
		A13 J4		TP901		TP900				TP903
		A21 J100		√		√		√		√
		A22 J100		√		√		√		√
		A23 J100		TP907		√	TP903	TP909		TP900
		A24 J100		√		√		√		√
		A31 J10	√	√		√	√		√	√
		A32 J32	√			√	√		√	√
		A33 J7		√		√	TP605	√		√
		A41 J41		TP560			TP561	TP562		TP551
		A42 J42		TP550		TP558	TP552	TP553		TP559
		A51 J5	√			√			√	TP504
		A52 J3	√			√	TP105		√	TP106
		A61 J4		TP500			TP501	TP502		√
		A62 J4		TP501			TP500	TP502		TP504
		A90/91 J3							√	√
		A91 J2	√						√	√
		Probe Power		√				√ †		√

† A circuit on the Motherboard assembly reduces this voltage to –13V

Table 9-2 lists the pin numbers of the voltages and signals at the power supply connectors, J1 (connects to CPU) and J2 (connects to Motherboard). For a description of these signals, see "W2 CPU Power Cable" and "W12 Motherboard Power Cable" later in this chapter. For voltage tolerances and troubleshooting information, see "Initial Verification" in chapter 4.

Table 9-2. Power Supply Connectors J1 and J2

Signal Name	J1 Pin(s)	J2 Pin(s)
PSSD\	—	50
LSWP\†	—	37
BFREQ_REF	3	—
PVALID	13	—
SDA\‡	15	11
SCLB\‡	17	9
SCLA\‡	19	7
RESET\‡	21	5
SINT\‡	23	3
GETTRIG‡	25	1
+5V	5-10	15-20
+8V	—	45-49
+12V	1,2,4	—
+15V	—	41, 42
-15V	—	27, 29
+18V	—	33
-18V	26	23
Gnd	11,12-24 (even)	2-12 (even), 13, 14, 21, 22, 24-26, 28, 30-32, 34-36, 38-40, 43, 44

† This signal is not used by the Power Supply assembly.

‡ This signal passes directly from J1 to J2 and is not used by the Power Supply assembly

W1 Memory Cable

Table 9-3 lists signals and voltages routed through the memory cable. This table show several things — if the assembly generates or uses the signal or voltage, and if a signal is bidirectional. A description of each signal follows the table.

Table 9-3. Memory Cable

Signal Name	Pin(s)	A81J7	A87/A88 J7
10MHZ	60	S	●
AS\	48	S	●
BD0 — BD15	25-40	↔	↔
INT_ACK\	50	S	●
LDS\	46	S	●
MEM_DTACK\	54	●	S
PA1 — PA23	1-23	S	●
RW	52	S	●
SCL\	62	S	●
SDA\	64	S	●
UDS\	44	S	●
+5V	42,45,49,53,57,61	●	●
+12V	58	●	●
Gnd	24,41,43,47,51,55, 59,63	●	●

S This assembly is the source of the signal.
● This assembly uses the signal.
↔ This signal is bidirectional.

10MHZ — 10 MHz Clock — This is a 50% duty cycle, 10 MHz clock. It refreshes the dynamic RAM and synchronizes data transfers on the Memory assembly.

AS\ — Address Strobe — This line pulses low when a valid address is on the processor address bus (PA1 — PA23).

BD0 — BD15 — Buffered Data Bus — This is the buffered processor data bus from the CPU assembly. It is further buffered on the Memory assembly. Most data transfers between the two assemblies occur on this bus.

INT_ACK\ — Interrupt Acknowledge — This line goes low when the CPU assembly receives an interrupt. A low on this line prevents the Memory assembly from starting another memory cycle.

LDS\ — Lower Data Strobe — During a write cycle, this line pulses low when valid data is on BD0 through BD7. During a read cycle, this line pulses low when data should be placed onto BD0 through BD7.

MEM_DTACK\ Memory Data Transfer Acknowledge — This line pulses low after the Memory assembly places RAM or flash EPROM data on the Buffered Data Bus.

PA1 — PA23 Processor Address Bus — This is the processor address bus from the CPU assembly. It is buffered on the Memory assembly.

RW Read/Write — This line is high when the current memory cycle is a read. It goes low when the current memory cycle is a write.

SCL\ Serial Clock — This is the serial clock for the IIC bus. The IIC controller on the CPU assembly generates this clock to synchronize the transfer of data on the IIC bus.

SDA\ Serial Data — This is the IIC bus bidirectional data line. This line transmits real-time clock data between the CPU assembly and the Memory assembly in 8-bit frames. The IIC controller on the CPU assembly controls data transfers on the IIC bus.

UDS\ Upper Data Strobe — During a write cycle, this line goes low when data is valid on BD8 — BD15. During a read cycle, this line goes low when data should be placed onto BD8 — BD15.

W2 CPU Power Cable

Table 9-4 lists signals and voltages routed through the CPU power cable. This table show several things — if the assembly generates or uses the signal or voltage, and if a signal is bidirectional. A description of each signal follows the table.

Table 9-4. W2 CPU Power Cable

Signal Name	Pin(s)	A81J1	PwrJ1
BFREQ_REF	3	S	●
GETTRIG	25	S	—
PVALID	13	●	S
RESET\	21	S	—
SCLA\	19	S	—
SCLB\	17	S	—
SDA\	15	↔	—
SINT\	23	●	—
+5V	5-10	●	S
+12V	1,2,4	●	S
−18V	26	●	S
Gnd	11,12,14,16,18,20, 22,24	●	●

S This assembly is the source of the signal/voltage.
● This assembly uses the signal/voltage.
↔ This signal is bidirectional
– This assembly does not use this signal

Note

GETTRIG, SCLA\, SCLB\, SINT\, SDA\, and RESET\ are not used by the Power Supply assembly. Instead, these signals are routed between the CPU assembly and the Motherboard assembly by the CPU power cable, the Power Supply assembly, and the motherboard power cable. LSWP\ is present on the motherboard power cable but is not used by either the Power Supply assembly or the CPU assembly.

BFREQ_REF — Buffered Frequency Reference — This is a 50% duty cycle, 35.714 kHz clock generated by the CPU assembly to reduce noise and ripple from the Power Supply assembly. The Power Supply assembly phase locks its switching frequency to this clock.

GETTRIG — Group Execute Trigger — This is the group-execute trigger line from the HP-IB interface on the CPU assembly. When the selected trigger source is HP-IB, the Trigger assembly uses this line to trigger the analyzer.

PVALID	Power Valid — This line is high when the +5V supply from the Power Supply assembly is stabilized.
RESET\	System Reset — A low on this line resets the digital logic on the ADC/Digital Filter assembly. This line pulses low during power-up and power-down, when the processor is externally reset, and when the processor executes the RESET instruction.
SCLA\	Serial Clock A — This is a serial clock for the IIC bus. The IIC controller on the CPU assembly generates this clock to synchronize the transfer of data on the IIC bus.
SCLB\	Serial Clock B — This is another serial clock for the IIC bus. The IIC controller on the CPU assembly generates this clock to synchronize the transfer of data on the IIC bus.
SDA\	Serial Data — This is the IIC bus bidirectional data line. This line transmits data to or from the CPU assembly in 8-bit frames. The IIC controller on the CPU assembly controls data transfers on the IIC bus.
SINT\	Serial Interrupt — This is the IIC bus interrupt line. A low on this line interrupts the CPU assembly.

W3 Display Cable

Table 9-5 lists signals and voltages routed through the display cable. This table show several things — if the assembly generates or uses the signal or voltage, and if a signal is bidirectional. A description of each signal follows the table.

Table 9-5. W3 Display Cable

Signal Name	Pin(s)	A81J4	Display
FB	15	S	●
HB	13	S	●
HSYNC	5	S	●
VSYNC	7	S	●
+12V	9,11	●	●
+5V	10	●	●
Gnd	4,6,8,12,14,16	●	●
Not Used	1-3	—	—

S This assembly is the source of the signal.
● This assembly uses the signal.
↔ This signal is bidirectional.
— This assembly does not use this signal.

FB — Full Bright — A high on this line sets the Display assembly's electron beam to full bright.

HB — Half Bright — A high on this line sets the Display assembly's electron beam to half bright.

HSYNC — Horizontal Synchronization — A high on this line causes the Display assembly to do a horizontal retrace.

VSYNC — Vertical Synchronization — A high on this line causes the Display assembly to do a vertical retrace.

W4 Disk Drive Cable

Table 9-6 lists signals and voltages routed through the disk drive cable. This table show several things — if the assembly generates or uses the signal or voltage, and if a signal is bidirectional. A description of each signal follows the table.

Table 9-6. W4 Disk Drive Cable

Signal Name	Pin(s)	A81J5	Disk Drive
DCR\	1	S	●
DIRECTION	18	S	●
DISK_CHANGE\	2	●	S
DISK_IN\	13	●	S
DISK_READY\	34	●	S
DRIVE_SELECT_0\	10	S	●
DRIVE_SELECT_1\	12	S	●
DRIVE_SELECT_2\	14	S	●
DRIVE_SELECT_3\	6	S	●
HEAD_SELECT	32	S	●
IN_USE\	4	S	●
INDEX\	8	●	S
MOTOR_ON\	16	S	●
READ_DATA\	30	●	S
STEP\	20	S	●
T00\	26	●	S
WRITE_DATA\	22	S	●
WRITE_GATE\	24	S	●
WRITE_PROT\	28	●	S
+5V	3,5,7,9,11	●	●
+12V	29,31,33	●	●
Gnd	15,17,19,21,23,25, 27	●	●

S This assembly is the source of the signal.
● This assembly uses the signal
↔ This signal is bidirectional.
– This assembly does not use this signal.

DCR\ — Disk Change Reset — A low on this line resets DISK_CHANGE\. This line goes low when DISK_READY\ is low.

DIRECTION — Direction — This line sets the direction for the disk head. A high on this line sets the direction away from the spindle. A low on this line sets the direction toward the spindle.

DISK_CHANGE\	Disk Change — This line goes low when a flexible disk is removed from the Disk Drive assembly. This line remains low until a flexible disk is installed and either DCR\ or STEP\ goes low.
DISK_IN\	Disk In — This line goes low when a flexible disk is inserted in the Disk Drive assembly.
DISK_READY\	Disk Ready — This line goes low when a flexible disk is inserted and the index period of the disk motor is stable. A low on this line causes DCR\ to go low, which resets DISK_CHANGE\.
DRIVE_SELECT 0, 1, 2, 3	Drive Select — A low on DRIVE_SELECT 0 selects the Disk Drive assembly. DRIVE_SELECT 0 is connected to ground and DRIVE_SELECT 1, 2 and 3 are connected to +5V.
HEAD_SELECT	Head Select — A low on this line selects the lower disk drive head. A high on this line selects the upper disk drive head.
INDEX\	Index — This line pulses low with each revolution of the flexible disk.
IN_USE\	In Use — A low on this line turns on the disk drive LED. This line is low during disk access.
MOTOR_ON\	Motor On — A low on this line turns on the disk drive motor. This line goes low when a flexible disk is inserted.
READ_DATA\	Read Data — This line pulses low for each bit detected on the flexible disk.
STEP\	Step — A low on this line moves the disk drive head. When STEP\ and DIRECTION are low, the head moves toward the disk spindle. When STEP\ is low and DIRECTION is high, the head moves away from the disk spindle.
T00\	Track 00 — This line is low when the head is positioned over track 0 on the flexible disk.
WRITE_DATA\	Write Data — When WRITE_GATE\ is low, a low pulse on this line writes a bit to the disk.
WRITE_GATE\	Write Gate — When this line is low, information may be written to the Disk Drive assembly under control of the WRITE_DATA\ line.
WRITE_PROT\	Write Protect — This line is low when a write-protected disk is installed in the Disk Drive assembly.

W5 Front Panel Cable

Table 9-7 lists signals and voltages routed through the front panel cable. This table show several things — if the assembly generates or uses the signal or voltage, and if a signal is bidirectional. A description of each signal follows the table.

Table 9-7. W5 Front Panel Cable

Signal Name	Pin(s)	A81J3	Front Panel
RESET	5	S	•
SCL\	15	S	•
SDA\	13	↔	↔
SINTFP\	7	•	S
+5V	10	•	•
Gnd	6,8,12,14,16	•	•
Not Used	1,2,3,4,9,11	—	—

S This assembly is the source of the signal.
• This assembly uses the signal.
↔ This signal is bidirectional.
– This assembly does not use this signal.

RESET — System Reset — A high on this line resets the digital logic on the Front Panel assembly. This line pulses high during power-up and power-down, when the processor is externally reset, and when the processor executes the RESET instruction.

SCL\ — Serial Clock — This is the serial clock for the front panel IIC bus. The IIC controller on the CPU assembly generates this clock to synchronize the transfer of data from the Front Panel assembly.

SDA\ — Serial Data — This is the front panel IIC bus. When a front panel key is pressed or the RPG is turned, SINTFP\ interrupts the CPU assembly and this line transmits data to the CPU assembly in 8-bit frames.

SINTFP\ — Serial Interrupt from the Front Panel — A low on this line interrupts the CPU assembly. This line goes low when a front-panel key is pressed or when the RPG is turned.

W11 Fast Bus Cable

Table 9-8 lists signals and voltages routed through the fast bus cable. This table show several things — if the assembly generates or uses the signal or voltage, and if a signal is bidirectional. A description of each signal follows the table.

Table 9-8. W11 Fast Bus Cable

Signal Name	Pin(s)	A81J6	A62J5
ACK0\	57	S	•
DTC\	61	•	S
ECLK	53	S	—
EXT_CLK	63	•	S
FA1 — FA5	33-41 (odd)	S	•
FD0 — FD15	1-31 (odd)	↔	↔
FDTACK\	51	•	S
FIRQ\	43	•	S
FRW	45	S	•
PCL0\	59	•	S
REQ0\	55	•	S
SELA\	47	S	•
SELS\	49	S	—
Gnd	2-64 (even)	•	•

S This assembly is the source of the signal.
• This assembly uses the signal.
↔ This signal is bidirectional.
— This assembly does not use this signal.

ACK0\ — DMA Acknowledge — This line pulses low in response to a low on REQ0\ when the CPU assembly is ready for data.

DTC\ — Data Transfer Complete — This line goes low after the CPU assembly successfully reads the data from the ADC/Digital Filter assembly. When this line goes low, PCL0\ goes high to prevent the CPU assembly from trying another read cycle until the ADC/Digital Filter assembly is ready.

ECLK — Enable Clock — This is a 60% duty cycle, 1 MHz clock. The ADC/Digital Filter assembly does not use this clock or route it to any other assembly.

EXT_CLK — External Clock — This is a TTL level, 20 MHz clock that locks the system clock to the reference clock. It synchronizes the CPU assembly with the rest of the instrument.

FA1 — FA5 — Fast Bus Address Lines — These lines are a buffered form of the CPU assembly's processor address bus. The CPU assembly uses these lines to address different circuits on the ADC/Digital Filter assembly.

FD0 — FD15	Fast Bus Data Lines — These bidirectional data lines are an extension of the CPU assembly's buffered processor data bus.
FDTACK\	Fast Bus Data Transfer Acknowledge — A low on this line terminates asynchronous bus cycles.
FIRQ\	Fast Bus Interrupt Request — A low on this line interrupts the CPU assembly.
FRW	Fast Bus Read/Write — This line is high during a read cycle and low during a write cycle. This line is an extension of the read/write line (RW).
PCL0\	DMA Programmable Control Line — This line goes low in response to a low on ACK0\ when the ADC/Digital Filter assembly is ready to send data. This line goes high when DTC\ goes low.
REQ0\	DMA Request — This line goes low after the ADC/Digital Filter assembly collects a block of data and is ready to have the CPU assembly read the data.
SELA\	Asynchronous Select — A low on this line enables asynchronous circuits on the ADC/Digital Filter assembly.
SELS\	Synchronous Select — This line is low when a synchronous bus cycle is in operation. The ADC/Digital Filter assembly does not use this line or route it to any other assembly.

W12 Motherboard Power Cable

Table 9-9 lists signals and voltages routed through the motherboard power cable. This table show several things — if the assembly generates or uses the signal or voltage, and if a signal is bidirectional. A description of each signal follows the table.

Table 9-9. W12 Motherboard Power Cable

Signal Name	PWRJ2 Pin(s)	Power Supply	A99J5 Pin(s)	Motherboard
GETTRIG	1	—	50	●
LSWP\	37	—	14	S
PSSD\	50	●	1	S
RESET\	5	—	46	●
SCLA\	7	—	44	●
SCLB\	9	—	42	●
SDA\	11	—	40	↔
SINT\	3	—	48	S
+8V	45-49	S	2-6	●
+15V	41, 42	S	9,10	●
+18V	33	S	18	●
–15V	27, 29	S	22, 24	●
–18V	23	S	28	●
+5V	15-20	S	31-36	●
Gnd	2-12(even), 13, 14, 21, 22, 24-26, 28, 30-32, 34-36, 38-40, 43, 44	S	7, 8, 11-13, 15-17, 19-21, 23, 25-27, 29, 30, 37, 38, 39-49(odd)	●

S This assembly is the source of the signal.
● This assembly uses the signal.
↔ This signal is bidirectional.
– This assembly does not use this signal.

Note

GETTRIG, SCLA\, SCLB\, SINT\, SDA\, and RESET\ are not used by the Power Supply assembly. Instead, these signals are routed between the CPU assembly and Motherboard assembly by the CPU power cable, the Power Supply assembly, and the motherboard power cable.

GETTRIG — Group Execute Trigger — This is the group execute trigger line from the HP-IB interface on the CPU assembly. When the selected trigger source is HP-IB, the Trigger assembly uses this line to trigger the analyzer.

LSWP\ — Sweep Synchronization — This is the TTL sweep synchronization signal. After a change in resolution bandwidth or an instrument preset, the negative edge of this signal resets the digital filters on the ADC/Digital Filter assembly. On subsequent negative edges, this signal is the sweep signal for the analyzer.

PSSD\ — Power Supply Shut Down — A short circuit to ground on this line forces all Power Supply output voltages to zero. This line is normally an open circuit, but becomes a short circuit to ground if the analyzer's internal temperature becomes excessive.

RESET\ — System Reset — A low on this line resets the digital logic on the ADC/Digital Filter assembly. This signal is pulsed low during power-up and power-down, when the processor is externally reset, and when the processor executes the RESET instruction.

SCLA\ — Serial Clock A — This is the serial clock for the IIC bus. The IIC controller on the CPU assembly generates this clock. This clock synchronizes the transfer of data on the IIC bus.

SCLB\ — Serial Clock B — This is another serial clock for the IIC bus. The IIC controller on the CPU assembly generates this clock. This clock synchronizes the transfer of data on the IIC bus.

SDA\ — Serial Data — This is the IIC bus bidirectional data line. This line transmits data to or from the CPU assembly in 8-bit frames. The IIC controller on the CPU assembly controls data transfers on the IIC bus.

SINT\ — Serial Interrupt — This is the IIC bus interrupt line. A low on this line interrupts the CPU assembly.

RF Cables

Table 9-10 lists all signals routed through RF cables. The table shows where the cables are connected and which assembly generates the signal.

Table 9-10. RF Cables †

Signal Name	Assembly & Connector																Cable Color
	A11	A12	A13	A21	A22	A23	A24	A31	A32	A33	A41	A42	A51	A52	A61	A62	Rear Panel	
100_KHZ_REF										**J4**				J2				red
187.5_KHZ_SRCE										**J2**		J6						red
250_KHZ_RCVR										**J3**						J1		orange
10_MHZ_RCVR								**J3**							J2			yellow
10_MHZ_REF						J3		**J4**										blue
10_MHZ_SRCE								**J5**				J4						green
20_MHZ								**J9**	J1									red
60_MHZ									**J2**	J1								orange
80_MHZ_RCVR								**J8**								J2		green
300_MHZ_RCVR			J1						**J5**									orange
300_MHZ_REF						J2			**J4**									red
300_MHZ_SRCE									**J3**			J3						red
1ST_IF		**J3**	J2															red
2ND_IF			**J3**												J1			lt blue
3RD_IF															**J3**	J3		white
CAL	J2							**J1**										red
CAL_SRCE								J2			**J2**							red
EXT_REF_IN								J7									**EXT REF IN**	blue
EXT_TRIG/GATE										J6							**EXT TRIG/GATE**	black
F/N_VCO													**J3**	J1				orange
INPUT_OUT	**J3**	J2																black
INTRPL_VCO					J3								**J1**					white
NORMALIZE	J1										**J1**							orange
REF_OUT								**J6**									REF OUT	lt green
SL_VCO				**J1**									J2					orange
SRCE_AMP											J3	**J1**						red
STEP_TO_SUM					J2		**J1**											blue
STEP_VCO						J1	**J3**											blue
SUM_VCO				**J4**	J1													red
SWEPT_LO_RCVR		J1		**J3**														gray
SWEPT_LO_SRCE				**J2**								J2						blue
TRIG/GATE_OUT										**J5**							TRIG/GATE OUT	white

† The signal source is shown in boldface type.

100_KHZ_REF — 100 kHz Reference — This is a 100 kHz, 1 Vp-p, approximate 1% duty cycle pulse. This signal provides a phase reference for the Fractional-N assembly.

187.5_KHZ_SRCE — 187.5 kHz to Source — This is a 187.5 kHz, 600 mVp-p, ac-coupled square wave. The Source Conversion assembly mixes this signal with 10_MHZ_SRCE.

250_KHZ_RCVR — 250 kHz to Receiver — This is a 250 kHz, TTL-level signal. The ADC on the ADC/Digital Filter assembly samples on the rising edge of this signal.

10_MHZ_RCVR — 10 MHz to Receiver — This is a 10 MHz, –2 dBm, ac-coupled sine wave. The IF assembly mixes this signal with 2ND_IF.

10_MHZ_REF — 10 MHz Reference — This is a 10 MHz, –2 dBm, ac-coupled sine wave. This signal is divided by 5 or 2, then used as a phase reference on the Step Phase Detector assembly.

10_MHZ_SRCE — 10 MHz to Source — This is a 10 MHz, –2 dBm, ac-coupled sine wave. The Source Conversion assembly mixes this signal with 187.5_KHZ_SRCE.

20_MHZ — 20 MHz — This is a 20 MHz, ECL level, ac-coupled square wave. This signal provides the 300 MHz assembly with a phase reference.

60_MHZ — 60 MHz — This is a 60 MHz, ECL level, ac-coupled signal. The Trigger assembly divides this signal to generate 250_KHZ_RCVR, 187.5_KHZ_SRCE, and 100_KHZ_REF.

80_MHZ_RCVR — 80 MHz to Receiver — This is an 80 MHz, 50% duty cycle, ECL level signal. The ADC/Digital Filter assembly divides this signal by four to generate 20 MHz clock signals.

300_MHZ_RCVR — 300 MHz to Receiver — This is a 300 MHz, 0 dBm, ac-coupled sine wave. The Second Conversion assembly mixes this signal with 1ST_IF.

300_MHZ_REF — 300 MHz Reference — This is a 300 MHz, –2 dBm, ac-coupled sine wave. The Step Phase Detector assembly mixes this signal with STEP_VCO.

300_MHZ_SRCE — 300 MHz to Source — This is a 300 MHz, –10 dBm, ac-coupled sine wave. The Source Conversion assembly mixes this signal with a 10.1875 MHz signal.

1ST_IF — First Intermediate Frequency — This is a 310.1875 MHz signal with a nominal full-scale amplitude of –30 dBm. This signal is the input signal for the Second Conversion assembly.

2ND_IF — Second Intermediate Frequency — This is a 10.1875 MHz signal with a nominal full-scale amplitude of –37 dBm signal. This signal is the input signal for the IF assembly.

3RD_IF — Third Intermediate Frequency — This is a 187.5 kHz signal with a nominal full-scale amplitude of 3 dBV. This signal is the input signal for the ADC/Digital Filter assembly.

CAL — Calibration — This is a square wave with a –20 dBm precision-amplitude fundamental. The Reference/Calibrator assembly attenuates either CAL_SRCE or a fixed 10 MHz signal. The calibration and self-test routines use this signal at various times.

CAL_SRCE — Calibration Source — During calibration of the input path, this is a 200 kHz to 150 MHz, approximate –11 dBm signal. The Source Amplifier assembly routes this signal to the Reference/Calibrator assembly. The calibration, adjustment-setup, and self-test routines use this signal path at various times.

EXT_REF_IN — External Reference — This is the analyzer's external reference input from the optional Fan Power/Oven assembly or an external source. The signal can be a 1 MHz, 2 MHz, 5 MHz, or 10 MHz sine or square wave with an amplitude between 5 dBm and +10 dBm. This signal is routed from a BNC connector on the rear panel.

EXT_TRIG/GATE — External Trigger/Gate — This is the analyzer's external trigger input. During external trigger or gated-sweep measurements, the selected TTL level on this line triggers the analyzer. The selected TTL level is set by the user to active high or active low. This signal is routed from a BNC connector on the rear panel.

F/N_VCO — Fractional-N Voltage Controlled Oscillator — When the local oscillator is operating in single loop mode, this is a 31 to 46 MHz, dc-coupled, ECL level, square wave derived from dividing SL_VCO by 10. In multiple loop mode, this is a 30 to 55 MHz, dc-coupled, ECL level, square wave controlled by CV_FRACN. The Fractional-N assembly divides this signal down to 100 kHz.

Note

For information on the local oscillator's single and multiple loop modes, see figures 8-12 and 8-13.

INPUT_OUT — Input Out — This signal's frequency range is 10 Hz to 150 MHz and its full-scale amplitude is approximately –28 dBm ± 1 dB. This signal is the input signal after it is buffered or attenuated, then amplified and filtered. This signal is the input signal for the First Conversion assembly.

INTRPL_VCO — Interpolation Voltage Controlled Oscillator — This is either a 3 to 5 MHz or a 6 to 11 MHz, ac-coupled, ECL level, square wave. The frequency range depends on whether F/N_VCO is divided by ten or by five. The Sum Phase Detector uses this signal for a phase comparison. This signal is only present when the local oscillator is operating in multiple loop mode.

NORMALIZE — Normalize — The analyzer's calibration and self-test routines use this signal path at various times. During calibration of the source, this is a 300 kHz signal routed to the Input assembly.

REF_OUT — Reference Out — This is a 10 MHz, 50% duty cycle, ECL level, ac-coupled sine wave derived by dividing 20_MHZ by two. This signal is routed to a BNC connector on the rear panel.

SL_VCO — Single Loop Voltage Controlled Oscillator — This signal can sweep from 310.1875 to 460.1875 MHz. It is a +3 dBm signal controlled by CV_SL. The Interpolation VCO assembly divides this signal by 10 and routes it to the Fractional-N assembly as F/N_VCO. This signal is only present when the local oscillator is operating in single loop mode.

SRCE_AMP — Source Amplifier — This is a 10 Hz to 150 MHz, –41 to –60.9 dBm signal. This signal is the input for the Source Amplifier.

STEP_TO_SUM — Step to Sum Voltage Controlled Oscillator — When the local oscillator is operating in multiple loop mode, this is a 306 to 450 MHz, –8 dBm signal controlled by CV_STEP. This signal steps from 306 to 336 MHz in 2 MHz steps and from 335 to 450 MHz in 5 MHz steps. The Sum Phase Detector mixes this signal with SUM_VCO. When the local oscillator is operating in single loop mode, this is a 306 MHz signal that is not used.

STEP_VCO — Step Voltage Controlled Oscillator — When the local oscillator is operating in multiple loop mode, this is a 306 to 450 MHz, +10 dBm signal controlled by CV_STEP. This signal steps from 306 to 336 MHz in 2 MHz steps and from 335 to 450 MHz in 5 MHz steps. The Step Phase Detector mixes this signal with 300_MHZ_REF. When the local oscillator is operating in single loop mode, this is a 306 MHz signal that is not used.

SUM_VCO — Sum Voltage Controlled Oscillator — This signal can sweep from 310.1875 to 460.1875 MHz. Its amplitude is typically +8 dBm, and it is controlled by CV_ML. The Sum Phase Detector mixes this signal with STEP_TO_SUM. This signal is only used when the local oscillator is operating in multiple loop mode.

SWEPT_LO_RCVR — Swept Local Oscillator to Receiver — This signal can sweep from 310.1875 to 460.1875 MHz. When the local oscillator is operating in single loop mode, this signal is controlled by CV_SL, and in multiple loop mode, this signal is controlled by CV_ML. This signal's amplitude is typically +4 dBm. The First Conversion assembly mixes this signal with INPUT_OUT.

SWEPT_LO_SRCE — Swept Local Oscillator to Source — This signal can sweep from 310.1875 to 460.1875 MHz. When the local oscillator is operating in multiple loop mode, this signal is controlled by CV_SL, and in multiple loop mode, this signal is controlled by CV_ML. This signal's amplitude is typically –10 dBm. The Source Conversion assembly mixes this signal with 310.1875 MHz.

TRIG/GATE_OUT — Trigger/Gate Output — During gated-sweep measurements, this line is high during the time the measurement is being taken. During all other measurements, this is a buffered version of LSWP\ unless the trigger is in slave mode, then this is a buffered version of EXT_TRIG. This signal is routed to a BNC connector on the rear panel.

Motherboard Signals and Voltages

Table 9-11 lists all signals routed through the Motherboard. The table shows the first place a signal appears or could appear on the Motherboard. Table 9-12 lists voltages routed through the Motherboard (see table 9-1 for a complete list of assemblies using each voltage).

Table 9-11. Motherboard Signals

Signal Name	Assembly Using Signal															
	PWR	A11	A12	A21	A22	A23	A24	A31	A32	A33	A41	A42	A51	A52	A61	A62
	Motherboard Connector															
	J5	J11	J12	J21	J22	J23	J24	J31	J32	J33	J41	J42	J51	J52	J61	J62
	Connector Pin Number															
187.5 SIG\											1A	**16A**				
ATN0															1A	**16A**
ATN1															1B	**16B**
ATN2															1C	**16C**
ATN3															2A	**15A**
ATN4															2B	**15B**
CAL_ON											2A	**15A**				
CF_0														4B		**7B**
CF_1														4C		**7C**
CF_2														5B		**8B**
CF_3														5C		**8C**
CF_REG														4A		**8A**
CF_STB														5A		**7A**
CV_FRACN													1B	**16B**		
CV_ML				11	**9**											
CV_SL				12										**16A**		
CV_STEP						**1B**	11									
DET_GATE										**5**						1C
GETTRIG	**50**									11						
GSWP										**3**				1C		
HFU\								11	**12**							
INC_IMAG		**1A**	8													
INC_REAL		**3A**	11													
LO_DET\															**3B**	14B
LSWP\	14									**12**				1A		1B
ML/SL				8		**2B**										
PRETUNE					11	**1C**										
PSSD\	1						**8**				**3B**					
RESET\	**46**															2C
SCLA\	**44**	15A				16C										2A
SCLB\	**42**							9		9	15B 16A 16C	2B 3A 3C	15B 16A 16C	1B 3A 3C		
SDA\	**40**	**16B**				**15A**		**12**		**8**	**16B**	3B	**16B**	**3B**		**3B**
SIG_DET															**3C**	14C
SINT\	48	**14A**				**15C**		**8**			**14A**		**14A**			**1A**
SLF\													3B	**14B**		
SPEED_UP				7	**7**											
SRCE_ON											1B	**16B**				
SUM_OOL_H					**12**	2A										
SUM_OOL_L					**10**	1A										
THRESH_LOW											2B	**15B**				
UP_DN		**2A**	12													

† The first place on the Motherboard that the signal appears (or could appear) is shown in boldface type.

Table 9-12. Motherboard Voltages

Voltage	Assembly Using Voltage																		
	PWR	A11	A12	A13	A21	A22	A23	A24	A31	A32	A33	A41	A42	A51	A52	A61	A62	A90/91	P PWR
	Motherboard Connector																		
	J5	J11	J12	J13	J21	J22	J23	J24	J31	J32	J33	J41	J42	J51	J52	J61	J62	W1	W2
	Connector Pin Number or Wire Color																		
+18V	18								1	1				7A	7A			Red	
														7B	7B				
														7C	7C				
+15V	9	4A	1	1	1	1	4A	1	3		1	4A	4A			4A	4A		Red
	10	4B					4B					4B	4B			4B	4B		
		4C					4C					4C	4C			4C	4C		
+8V	2-6		5	5	5	5	10A	5	5	5	5		10A	10A	10A				
			6	6	6	6	10B	6	6	6	6		10B	10B	10B				
							10C						10C	10C	10C				
+5V	31-	12A	10				12A		10	10	10	12A	12A		12A	12A	12A		
	36	12B					12B					12B	12B		12B	12B	12B		
		12C					12C					12C	12C		12C	12C	12C		
−15V	22	5A	2		2	2	5A	2			2	5A	5A			5A	5A		Yel†
	24	5B					5B					5B	5B			5B	5B		
		5C					5C					5C	5C			5C	5C		
−18V	28								2	2				8A	8A			Yel	
														8B	8B				
														8C	8C				
Gnd	7-8	6A	4	4	4	4	3A	4	4	4	4	3A	6A	1A	6A	2C	6A	Blk	Blk
	11-	6B	7	7	9		3B	7	7	7	7	3C	6B	1C	6B	6A	6B		
	13	6C	9	9			3C	9				6A	6C	2A	6C	6B	6C		
	15-	9A					6A	12				6B	9A	2B	9A	6C	9A		
	17	9B					6B					6C	9B	2C	9B	9A	9B		
	19-	9C					6C					9A	9C	3A	9C	9B	9C		
	21	11A					9A					9B	11A	3C	11A	9C	11A		
	23	11B					9B					9C	11B	6A	11B	11A	11B		
	25-	11C					9C					11A	11C	6B	11C	11B	11C		
	27	13A					11A					11B	13A	6C	13A	11C	13A		
	29	13B					11B					11C	13B	9A	13B	13A	13B		
	30	13C					11C					13A	13C	9B	13C	13B	13C		
	37-						13A					13B	14A	9C	14A	13C	15C		
	39						13B					13C	14B	11A	14C				
	41						13C						14C	11B	15A				
	43													11C	15B				
	45													13A	15C				
	47													13B	16C				
	49													13C					

† A circuit on the Motherboard reduces this voltage to −13V before it is routed to the front panel for probe power.

187.5_SIG\ — 187.5 kHz Signal — This line is used during self tests and disabled during normal operation. This line goes low if the 187.5 kHz reference is present when a self test checks for the presence of the reference. This line also goes low if the output of the gilbert cell multiplier is present when a self test checks for the presence of the output.

ATN0 — ATN4 — Attenuator Control — These lines provide attenuator control for the IF assembly.

CAL_ON — Calibration Path Enable — A high on this line enables the calibration path from the Source Amplifier assembly to the Reference/Calibrator assembly.

CF_0 — CF_3 — Fractional-N Bus Data Lines — These data lines are derived from buffering and latching the fast bus data lines, FD0 through FD3.

CF_REG — Fractional-N Bus Register Address — This line is derived from buffering and latching the fast bus address line, FA1.

CF_STB — Fractional-N Bus Write Strobe — This line goes high when data is valid on CF_0 through CF_3.

CV_FRACN — Control Voltage to Fractional-N — This is the control voltage for the Interpolation VCO assembly. Its amplitude is between approximately –3V and +11.5V. This signal is only used when the local oscillator is operating in multiple loop mode.

Note

For information on the local oscillator's single and multiple loop modes, see figures 8-12 and 8-13.

CV_ML — Control Voltage Multiple Loop — This is the control voltage for the Sum VCO assembly. Its amplitude is between approximately –2V and +7V. This signal is only used when the local oscillator is operating in multiple loop mode.

CV_SL — Control Voltage Single Loop — This is the control voltage for the Sum VCO assembly. Its amplitude is between approximately –2 and +7V. This signal is only used when the local oscillator is operating in single loop mode.

CV_STEP — Control Voltage Step — This is the control voltage for the Step VCO assembly. When the local oscillator is operating in multiple loop mode, this signal's level is between approximately –2V and +7V. When the local oscillator is operating in single loop mode, this signal's level is approximately +7V.

DET_GATE — Detector Gate — This line is high when data can be transferred from the ADC/Digital Filter assembly's digital filter to the detector. This line is only used during gated-sweep measurements.

GETTRIG — Group Execute Trigger — This is the group execute trigger from the HP-IB interface on the CPU assembly. When the selected trigger source is HP-IB, the Trigger assembly uses this line to trigger the analyzer.

GSWP — Gate Sweep — This is the TTL gated-sweep synchronization signal. During gated-sweep measurements, this signal is used with LSWP\ to provide the sweep signal for the analyzer. This line is only used during gated-sweep measurements.

HFU\ — High Frequency Unlocked — This line is low when the 300 MHz phase-lock loop on the 300 MHz assembly is unlocked. A low on this line forces SINT\ low.

INC_IMAG — Increment Imaginary — This is the increment pulse for local oscillator feedthrough null imaginary axis control. UP_DN sets the increment direction. INC_IMAG, INC_REAL, and UP_DN interact to null the local oscillator feedthrough circuit on the First Conversion assembly.

INC_REAL — Increment Real — This is the increment pulse for local oscillator feedthrough null real axis control. UP_DN sets the increment direction. INC_IMAG, INC_REAL, and UP_DN interact to null the local oscillator feedthrough circuit on the First Conversion assembly.

LO_DET\ — Local Oscillator Detector — This line is low when the 10 MHz reference is not present on the IF assembly. A low on this line forces SINT\ low.

LSWP\ — Sweep Synchronization — This is the TTL sweep synchronization signal. After a change in resolution bandwidth or an instrument preset, the negative edge of this signal resets the digital filters on the ADC/Digital Filter assembly. On subsequent negative edges, this signal is the sweep signal for the analyzer.

ML/SL — Multiple Loop/Single Loop — This line is low when the local oscillator is in multiple loop mode and high when the local oscillator is in single loop mode. This line controls a switch on the Sum VCO assembly.

PRETUNE — Pretune — This signal coarsely adjusts the sum VCO. It is a scaled version of CV_STEP. When the local oscillator is operating in multiple loop mode, this signal's amplitude is between –2V and +7V. This voltage is added to the output of the integrator on the Sum Phase Detector assembly and becomes CV_ML. When the local oscillator is operating in single loop mode, this signal's amplitude is about +7V.

PSSD\ — Power Supply Shut Down — This line is normally an open circuit, but becomes a connection to ground if the analyzer's internal temperature becomes excessive. When this line is a connection to ground, all Power Supply output voltages are forced to zero.

RESET\ — System Reset — A low on this line resets the digital logic on the ADC/Digital Filter assembly. This line is pulsed low during power-up and power-down, when the processor is externally reset, and when the processor executes the RESET instruction.

SCLA\ — Serial Clock A — This is a serial clock for the IIC bus. The IIC controller on the CPU assembly generates this clock. This clock synchronizes the transfer of data on the IIC bus.

SCLB\ — Serial Clock B — This is another serial clock for the IIC bus. The IIC controller on the CPU assembly generates this clock. This clock synchronizes the transfer of data on the IIC bus.

SDA\ — Serial Data — This is the IIC bus bidirectional data line. This line transmits data to or from the CPU assembly in 8-bit frames. The IIC controller on the CPU assembly controls data transfers on the IIC bus.

SIG_DET — Signal Detection — This line is high when the signal at the 10.1875 MHz input of the IF assembly is approximately 15 dB over full scale.

SINT\ — Serial Interrupt — This is the IIC bus interrupt line. A low on this line interrupts the CPU assembly.

SLF\ — Sweep Limit Flag — This line goes low if the fractional-N integrated circuit on the ADC/Digital Filter assembly reaches the end of its frequency sweep. A low on this line can force SINT\ low.

SPEED_UP — Speed Up — When the sum loop is unlocked, this line is +15V and it speeds up the settling time of the sum loop. When the sum loop is locked, this line is –15V. This line controls a switch on the Sum VCO assembly. This line is only used when the local oscillator is operating in multiple loop mode.

SRCE_ON	Source On — This line is high when the source is on and low when the source is off.
SUM_OOL_H	Sum Out of Lock High — This line is high when the sum loop is unlocked because the frequency of the sum loop circuit is too high.
SUM_OOL_L	Sum Out of Lock Low — This line is high when the sum loop is unlocked because the frequency of the sum loop circuit is too low.
THRESH_LOW	Threshold Low — This line sets the overload detector threshold for the Source Amplifier assembly.
UP_DN	Up or Down — This line sets the increment direction for INC_IMAG and INC_REAL. When this line is low the increment direction is down. When this line is high the increment direction is up. INC_IMAG, INC_REAL, and UP_DN interact to null the local oscillator feedthrough circuit on the First Conversion assembly.

HP-IB Connector

Table 9-13 lists signals at the HP-IB connector (A81 J2). A description of each signal follows the table.

Table 9-13. HP-IB Connector (A81 J2)

Signal Name	Pin
ATN	11
DAV\	6
DIO1	1
DIO2	2
DIO3	3
DIO4	4
DIO5	13
DIO6	14
DIO7	15
DIO8	16
EOI\	5
IFC\	9
NDAC\	8
NRFD\	7
REN\	17
SRQ\	10
Shield	12
Logic Gnd	24
GND6	18
GND7	19
GND8	20
GND9	21
GND10	22
GND11	23

Note

The descriptions that follow for the HP-IB lines are general descriptions only. For a detailed description of how the analyzer interprets the HP-IB lines, see the HP 3589A HP-IB Programmer's Reference.

ATN — Attention — This line is controlled by the controller in charge. When this line is low, the DIO lines contain interface commands. When this line is high, the DIO lines contain data.

DAV\	Data Valid — This line goes low when valid data is on the bus and NRFD\ is high. This line is controlled by the HP-IB controller.
DIO1 — DIO8	Data Input/Output — These are inverted data lines that conform to IEEE specification IEEE-488. When ATN is low, these lines contain interface commands. When ATN is high, these lines contain data.
EOI\	End or Identify — If ATN is high, a low on this line marks the end of a message block. If ATN is low, a low on this line requests a parallel poll.
IFC\	Interface Clear — This line goes low to halt all current operations on the bus, unaddress all other devices, and disable serial poll. The system controller becomes the controller in charge.
NDAC\	Not Data Accepted — This line goes high when the DIO lines have been latched by the acceptor.
NRFD\	Not Ready for Data — This line goes high when the acceptor is ready to accept data.
REN\	Remote Enable — This line is low when the HP-IB has control and high during local operation.
SRQ\	Service Request — This line is low when a device on the HP-IB needs service.

Port 1 Connector

Table 9-14 lists signals at the Port 1 connector (A81 J8). Port 1 is an RS-232-C connector that allows the analyzer to control the HP 35689A/B S-Parameter Test Set. A description of each signal follows the table.

Table 9-14. Port 1 Connector (A81 J8)

Signal Name	Pin
DTR	1
RTS	4
RxD	3
TxD	2
Logic Gnd	7
Not Used	5-6, 8-9

DTR — Data Terminal Ready — This line is tied high. Some devices check this line for a high to verify that the analyzer is connected and ready.

RTS — Request To Send — This line is tied high. Some devices require this line to be high before transferring data.

RxD — Received Data — This is the serial RS-232-C receive data line. Data is transmitted on this line from the test set one byte at a time.

TxD — Transmitted Data — This is the serial RS-232-C transmit data line. Data is transmitted on this line to the test set one byte at a time.

HP 35689A/B S-Parameter Test Set

The following figures show assembly locations and ribbon cable connections for the HP 35689A S-Parameter Test Set. Cables with multiple signals or voltages (W1, W2, W10, and W19) are listed in their own section. Cables with one signal or voltage are listed together in the section called "Cables."

Assemblies

A1 50 Ohm RF
A2 Controller
A3 50 Ohm Directional Bridge
A4 75 Ohm Directional Bridge
A5 LED
A6 Power Supply
A11 75 Ohm RF

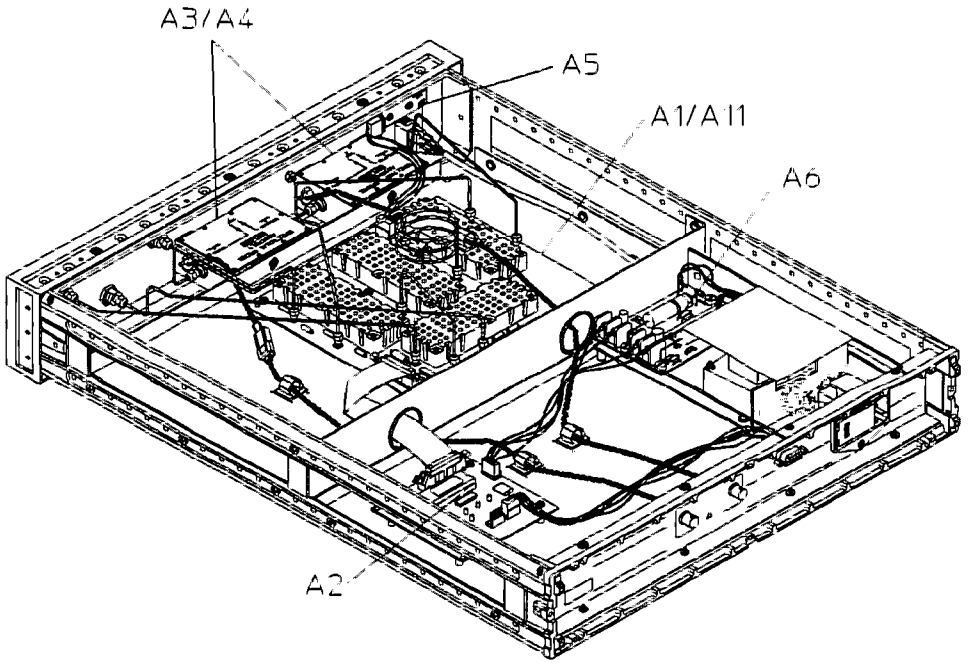


Figure 9-3. Assembly Locations

Cables

W1 Power
W2 Control
W3 Line Power Switch
W4 Srce Port 2
W5 Refld Port 2
W6 Srce Port 1
W7 Refld Port 1
W8 Input
W9 Output
W10 LED
W12 Port Bias
W14/15 Sptrm Input
W16 S-Prmtr Path
W17 Ref Path
W19 Interface

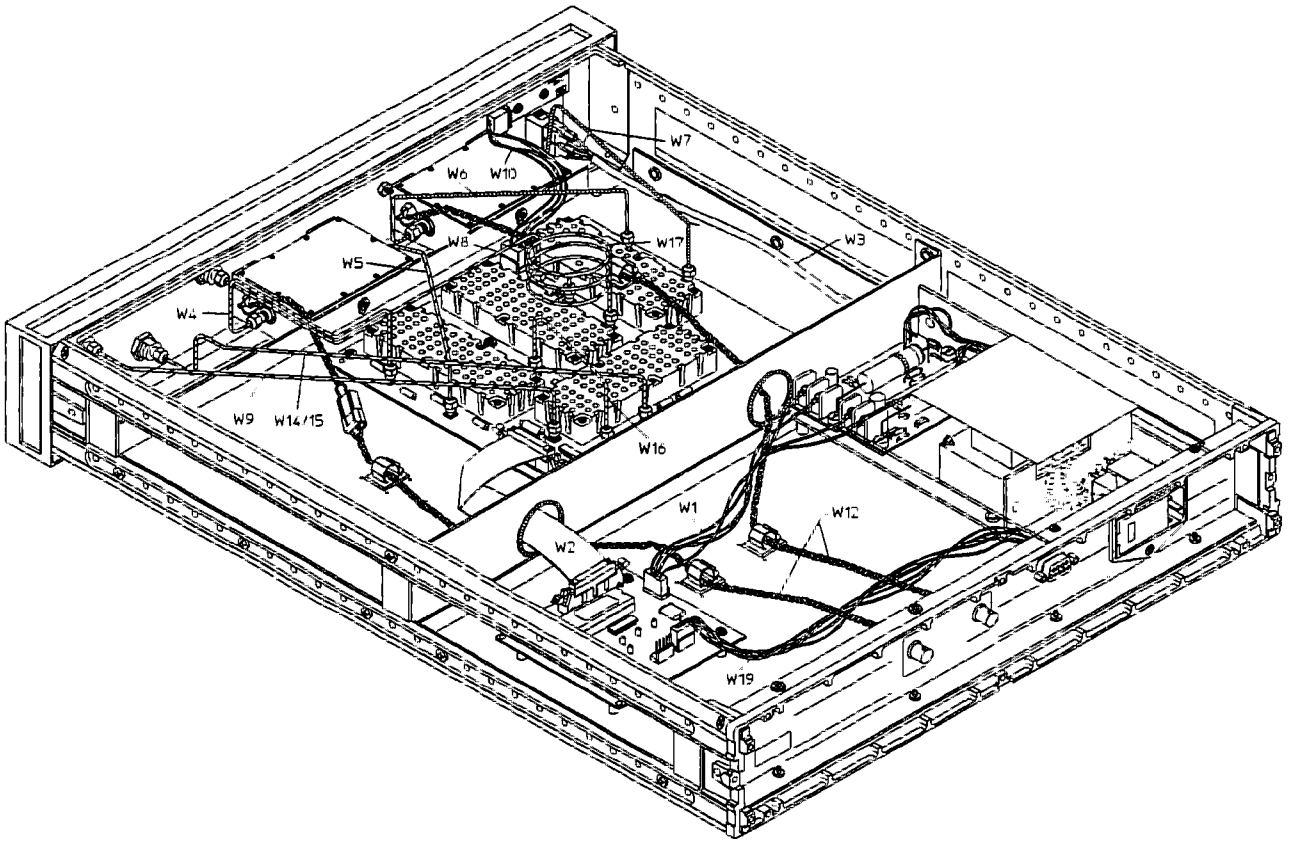


Figure 9-4. Cable Locations

Power Supply Voltage Distribution

Table 9-15 shows the power supply voltages used by each assembly in the test set. In addition, the table also shows the path taken by these voltages.

Table 9-15. Power Supply Voltage Distribution

From	Path	To	Voltages	
			+15V	+5V
A6	W1	A2 J4		√
	W1/A2/W2	A1 or A11 J29	√	√
	W1/A2/W2/A1 or A11	A5 J1		√

W1 Power Cable

Table 9-16 lists the wire colors and pin numbers for the voltages routed through the power cable.

Table 9-16. Power Cable

Voltage	Wire Color	A2J4 Pin(s)
+5V	Red	1
+15V	Yellow	2
GND	Black	3-4

W2 Control Cable

Table 9-17 lists the signals and voltages routed through the control cable. This table show several things — if the assembly generates or uses the signal or voltage, and if a signal is bidirectional. A description of each signal follows the table.

Table 9-17. Control Cable

Signal Name	Pin(s)	A2J3	A1/A11J29
B0	4	S	•
B1	3	S	•
B2	6	S	•
B3	5	S	•
B4	10	S	•
B5	9	S	•
B6	12	S	•
B7	13	•	S
+5V	15, 17	•	•
+15V	16, 18	—	•
GND	1-2, 7-8, 11, 14, 19-20	•	•

S This assembly is the source of the signal.
• This assembly uses the signal.
↔ This signal is bidirectional.
– This assembly does not use this signal

B0 Reference Termination — This line controls the relays in the Output Termination and Output Switching blocks that connect or terminate the reference path. A low on this line terminates the reference path and connects one of the coupled port paths to the Test Set Bypass block. A high on this line connects the reference path to the Test Set Bypass block.

B1 Spectrum Input — This line controls the relays in the Test Set Bypass block that connect or disconnect the spectrum path. A low on this line connects the Spectrum Input path to the test set's OUTPUT connector. A high on this line connects the Spectrum Input path to ground and connects the reference or coupled port path to the OUTPUT connector.

B2 Port 2 Termination — This line controls the relays in the Output Termination and Output Switching blocks that connect or terminate the coupled port 2 path and select the coupled port 1 path or the coupled port 2 path. A low on this line terminates the coupled port 2 path and connects the coupled port 1 path to the Output Switching block. A high on this line connects the coupled port 2 path to the Output Switching block.

B3 Port 1 Termination — This line controls the relays in the Output Termination block that connect or terminate the coupled port 1 path. A low on this line terminates the coupled port 1 path. A high on this line connects the coupled port 1 path to the Output Switching block.

B4 Port Select — This line controls the relay in the Input Switching block that routes the Input signal to the source port 1 path or the source port 2 path. A low on this line routes the Input signal to the source port 1 path. A high on this line routes the Input signal to the source port 2 path.

B5 Forward — This line controls the relays in the Input Switching block that connect or terminate the source port 1 path. A low on this line connects the Input signal to the source port 1 path. A high on this line terminates the source port 1 path. See the description of B5 in "W10 LED Cable."

B6 Reverse — This line controls the relays in the Input Switching block that connect or terminate the source port 2 path. A low on this line connects the Input signal to the source port 2 path. A high on this line terminates the source port 2 path. See the description of B6 in "W10 LED Cable."

B7 Impedance — This line tells the Control assembly the impedance of the RF assembly. On the A1 50 Ohm RF assembly, this line is not connected. On the A11 75 Ohm RF assembly, this line is connected to ground. Therefore, a high on this line tells the Control assembly that the test set is an HP 35689A, and a low on this line tells the Control assembly that the test set is an HP 35689B. The Control assembly sends this information to the analyzer.

W10 LED Cable

Table 9-18 lists the signals and voltages routed through the LED cable. This table show several things — if the assembly generates or uses the signal or voltage, and if a signal is bidirectional. A description of each signal follows the table.

Table 9-18. LED Cable

Signal Name	Pin(s)	A1/A11J30	A5J1
B5	2	●	●
B6	5	●	●
+5V	3	●	●

S This assembly is the source of the signal.
● This assembly uses the signal.
↔ This signal is bidirectional.
– This assembly does not use this signal.

B5 Forward — This line controls the Forward LED in the LED assembly. A low on this line turns on the Forward LED. A high on this line turns off the Forward LED. See the description of B5 in "W2 Control Cable."

B6 Reverse — This line controls the Reverse LED in the LED assembly. A low on this line turns on the Reverse LED. A high on this line turns off the Reverse LED. See the description of B6 in "W2 Control Cable."

W19 Interface Cable

Table 9-19 lists the signals routed through the interface cable. This table show several things — if the assembly generates or uses the signal or voltage, and if a signal is bidirectional. A description of each signal follows the table.

Table 9-19. Interface Cable

Signal Name	Rear Panel Connector Pin(s)	HP 3589A	A2 J1 Pin	A2J1
DTR	1	S	1	—
RTS	4	S	4	—
RxD	3	•	3	S
TxD	2	S	2	•
Logic Gnd	7	S	5	•
Not Used	5-6, 8-9	—		

S This assembly is the source of the signal.
• This assembly uses the signal.
↔ This signal is bidirectional.
– This assembly does not use this signal.

DTR — Data Terminal Ready — This line is tied high. Some devices check this line for a high to verify that the analyzer is connected and ready.

RTS — Request To Send — This line is tied high. Some devices require this line to be high before transferring data.

RxD — Received Data — This is the serial RS-232-C receive data line. Data is transmitted on this line from the test set to the analyzer one byte at a time.

TxD — Transmitted Data — This is the serial RS-232-C transmit data line. Data is transmitted on this line from the analyzer to the test set one byte at a time. This is the control line from the analyzer.

Cables

Table 9-20 lists the signals routed through the remaining cables. The signal source is shown in boldface type and a description of each signal follows the table.

Table 9-20. Cables

Signal Name	Cable	Connector			Connector Name	
		A1/11	A3/4 Port 1	A3/4 Port2	Front Panel	Rear Panel
CPLD_PORT_1	W7	J10	**J2**			
CPLD_PORT_2	W5	J9		**J2**		
INPUT	W8	J4			**Input**	
OUTPUT	W9	**J13**			Output	
PORT_BIAS	W12		J4			**Port Bias 1**
PORT_BIAS	W12			J4		**Port Bias 2**
REF_PATH	W17	**J5** to J6				
S-PRMTR_PATH	W16	**J11** to J14				
SPTRM_INPUT	W14/15	J12			**Spectrum Input**	
SRCE_PORT_1	W6	**J8**	J1			
SRCE_PORT_2	W4	**J7**		J1		

CPLD_PORT_1 — Coupled Port 1 — During S11 and S12 measurements, the signal coupled from port 1 is routed through this cable to the OUTPUT connector. The approximate signal loss from the PORT 1 connector to this cable is 6 dB with the HP 35689A and 12 dB with the HP 35689B.

CPLD_PORT_2 — Coupled Port 2 — During S21 and S22 measurements, the signal coupled from port 2 is routed through this cable to the OUTPUT connector. The approximate signal loss from the PORT 2 connector to this cable is 6 dB with the HP 35689A and 12 dB with the HP 35689B.

INPUT — Input — This is the input signal for the test set. During S-parameter measurements, the signal on this cable is the analyzer's source output. An external cable connects the analyzer's SOURCE connector to the test set's INPUT connector.

OUTPUT — Output — This is the output signal for the test set. During spectrum measurements, the signal on this cable is the signal connected to the front panel's SPECTRUM INPUT connector minus an approximate amplitude loss of 5.7 dB with the HP 35689B. During reference measurements, the signal on this cable is the signal connected to the test set's INPUT connector minus an approximate amplitude loss of 19 dB with the HP 35689A and 31 dB with the HP 35689B. During S11 and S12 measurements, the signal on this cable is the signal coupled from port 1. During S21 and S22 measurements, the signal on this cable is the signal coupled from port 2. An external cable connects the test set's OUTPUT connector to the analyzer's INPUT connector.

PORT_BIAS — Port Bias — The port bias cables allow you to supply bias voltages to devices connected to the front panel's port connectors. Connecting a voltage to the rear panel's PORT BIAS 1 connector supplies a bias voltage to the device connected to the PORT 1 connector. Connecting a voltage to the rear panel's PORT BIAS 2 connector supplies a bias voltage to the device connected to the PORT 2 connector.

REF_PATH — Reference Path — During reference measurements, the signal on this cable is the signal connected to the test set's INPUT connector minus an approximate amplitude loss of 19 dB with the HP 35689A and 31 dB with the HP 35689B.

S-PRMTR_PATH — S-Parameter Path — During reference measurements, the signal on this cable is the signal connected to the test set's INPUT connector minus an approximate amplitude loss of 19 dB with the HP 35689A and 31 dB with the HP 35689B. During S11 and S12 measurements, the signal on this cable is the signal coupled from port 1. During S21 and S22 measurements, the signal on this cable is the signal coupled from port 2.

SPTRM_INPUT — Spectrum Input — During spectrum measurements, the signal on this cable is routed to the test set's OUTPUT connector. This allows spectrum measurements without disconnecting the test set. The input impedance of the SPECTRUM INPUT connector is 50 Ω with the HP 35689A and 75 Ω with the HP 35689B. The output impedance at the OUTPUT connector is 50 Ω for both the HP 35689A and HP 35689B. Converting the signal from 75 Ω to 50 Ω results in an approximate 5.7 dB signal loss for the signal connected to the HP 35689B's SPECTRUM INPUT connector.

SRCE_PORT_1 Source Port 1 — During S11 and S21 measurements, the signal on this cable is the signal connected to the test set's INPUT connector. The approximate signal loss from this cable to the PORT 1 connector is 13 dB with the HP 35689A and 19 dB with the HP 35689B.

SRCE_PORT_2 Source Port 2 — During S12 and S22 measurements, the signal on this cable is the signal connected to the test set's INPUT connector. The approximate signal loss from this cable to the PORT 2 connector is 13 dB with the HP 35689A and 19 dB with the HP 35689B.

10 Internal Test Descriptions

10

Internal Test Descriptions

Introduction

This chapter describes the power-on test, calibration routine, fault log messages, and self tests. This chapter also lists the HP-IB command for each self test and the power-on and preset states.

Power-on Test Descriptions

The power-on test is run when the analyzer is powered up. This test exercises the CPU assembly and Memory assembly. This test is divided into low-level and high-level subtests.

Note 

The calibration routine is run immediately following the power-on tests. If an error occurs during the calibration routine, a failure message is recorded in the fault log.

Low-level Tests

The low-level power-on tests exercise the core of the CPU assembly and Memory assembly. If an error occurs during the low-level subtests, the test stops and displays an error code on the CPU assembly's power-on test LEDs (see Test 2. Power-on for details on decoding the power-on test LEDs).

High-level Test

The high-level power-on subtest exercises the fast bus. If an error occurs during the fast bus test, the analyzer locks up and the power-on LEDs display the fast bus error code (A1 hexadecimal).

Power-on Test Messages

Table 10-2 provides additional information for interpreting the power-on test LEDs. Using table 10-1, translate the power-on test LEDs to their equivalent hexadecimal code. Table 10-2 describes the power-on subtests in the order they are run. Table 10-2 also shows the relationship between a failing power-on subtest and the assemblies or sub-blocks.

Note

False error codes can be caused by shorts on the buses, reset line, or interrupt line. If an error code is caused by the last bus connected, it is probably the source of the failure.

Table 10-1. Binary to Hexadecimal

Binary 1 = LED on 0 = LED off	Hexadecimal
0000	0
0001	1
0010	2
0011	3
0100	4
0101	5
0110	6
0111	7
1000	8
1001	9
1010	A
1011	B
1100	C
1101	D
1110	E
1111	F

Table 10-2. Power-on Test Messages

Hexadecimal Code	Message	Assembly/Sub-block							
		Power Supply	A8: MPU (68901 & Address Decode	A8: MPU Buses, Coprocessor, DSP, MPU	A8: Monitor ROM	A8: Display Controller	A8: Memory	Fast Bus or IC Bus	Front Panel
		1	2	3	4	5	6	7	8
Undefined	Initial power-on	X	X	X					
08	LED DSACK failure	0	X	X	X				
FF*	CPU flashes LEDs	0	X	X	X				
13	CPU failure	0	X	X	X				
14	Boot ROM checksum failure	0	0	0	X				
0A	Display DSACK failure	0	0	0	0	X			
10	Display failure	0	0	0	0	X			
01	Main RAM DSACK	0	0	0	0	0	X		
17	Main RAM too small	0	0	0	0	0	X		
18	Main RAM bit failure	0	0	0	0	0	X		
19	Main RAM refresh failure	0	0	0	0	0	X		
1C	Program ROM checksum error	0	0	0	0	0	X		
00	Clear ~ 4s	0	X	X	0	0			
A1	Fast bus test	0	0	0	0	0	0	X	
	Front panel test	0	0	X	0	0	0	0	X

0 Assembly or sub-block is used but is probably not the cause of the failure message.
X Assembly or sub-block is probably the cause of the failure message.
(blank) Assembly or sub-block is not used in the test.

FF* If the area of failure is unclear, all LEDs flash continuously.

Calibration Routine

The calibration routine minimizes the receiver's LO feedthrough, and also provides amplitude correction for both the receiver and the source. The receiver's amplitude corrections are stored in memory as vectors. All measurements are multiplied by these vectors before being displayed (the vectors become part of the measurement). The calibration routine occurs immediately following the power-on tests and periodically afterwards to compensate for any drift. To manually start the calibration routine, press the [**Special Fctn**] hardkey followed by the [SINGLE CAL] softkey.

First, the calibration routine nulls the receiver's LO feedthrough. The receiver measures the LO feedthrough (response at 0 Hz input frequency) and sends the results to the CPU assembly. The CPU then sends control data to the Input assembly. The Input assembly decodes the control data and sends three control lines to the First Conversion assembly (see figure 10-1). These control lines adjust the real and imaginary components of the LO feedthrough cancellation signal. The LO cancellation signal then is added to the LO feedthrough. This process continues until a satisfactory null is achieved.

The calibration routine then produces amplitude correction for the IF assembly's attenuators. The calibrator generates a 10 MHz square wave with a -20 dBm precision-amplitude fundamental. This signal is sent to the receiver through the CAL path. Measurements are taken for all 32 attenuator settings, and the results are stored in memory.

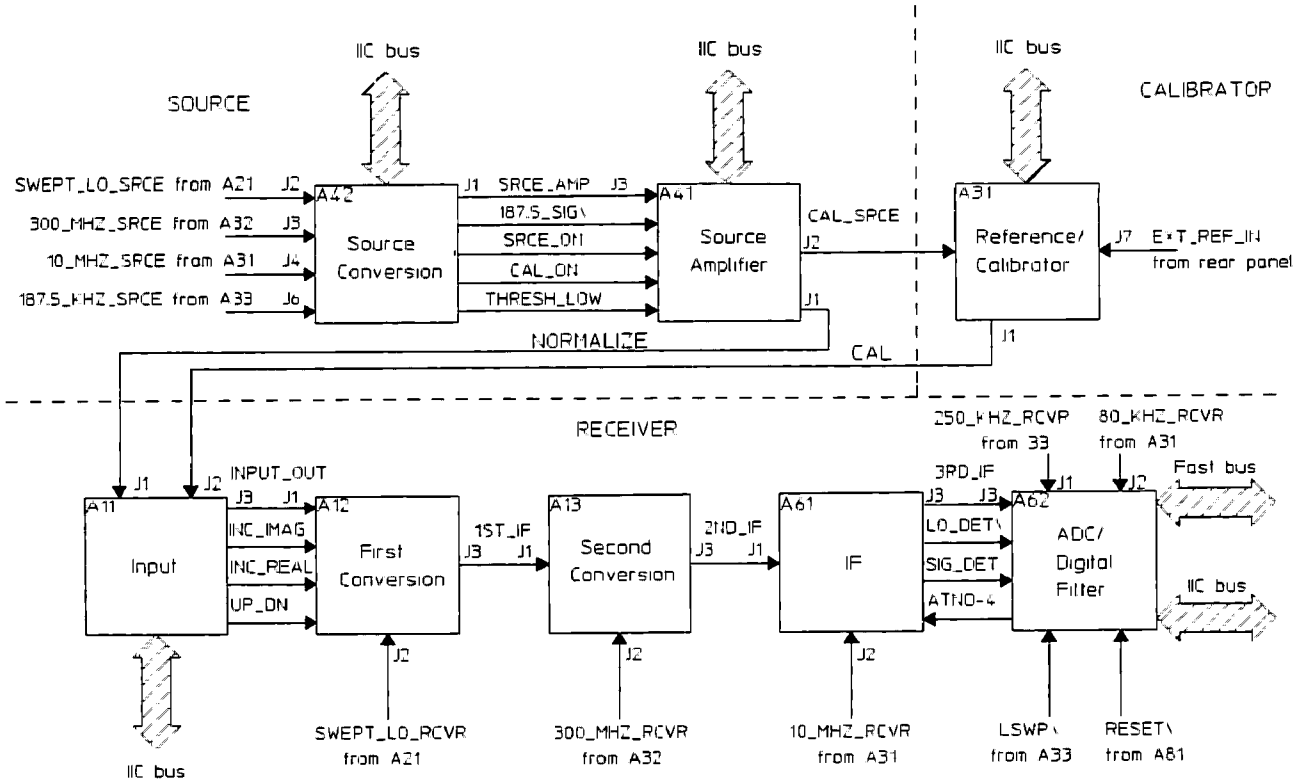


Figure 10-1. Calibration Block Diagram

Next, the calibration routine produces correction curves for the Input assembly's input paths. The source generates a swept 200 kHz to 150 MHz signal. This swept signal is sent to the calibrator through the CAL_SRCE path. The calibrator uses the swept signal to generate a swept 200 kHz to 150 MHz square wave with a –20 dBm precision-amplitude fundamental. This precision signal is sent to the receiver through the CAL path. Measurements are taken with the signal routed through the Input assembly's 50Ω input path (for all attenuators) and through the 1 MΩ input path. The measurement results are stored in memory as vectors.

The calibration routine then produces a correction curve for the shape of the 3rd IF filter. This correction curve is used in only narrow-band zoom measurements. The calibrator generates a 10 MHz square wave with a –20 dBm precision-amplitude fundamental. This precision signal is sent to the receiver through the CAL path. As the local oscillator sweeps, tracing out the shape of the 3rd IF, measurements are taken. The measurement result is stored in memory as a vector.

Last, the calibration routine produces amplitude correction data for the source. The source generates a 300 kHz signal. This signal is sent to the receiver through the NORMALIZE path. The receiver measures the signal at two different amplitudes and sends the measurement results to the CPU assembly. The CPU assembly then uses the measurement results to calculate the correction data for the source.

Calibration Error Message

Calibration correction vectors are compared with a set of maximum allowable error vectors. If any correction vector exceeds the maximum allowable error, the **Calibration failure** error message is displayed on the screen (for approximately 5 seconds) and placed in the Fault Log. To view the Fault Log, press the following keys:

[**Special Fctn**]
[F9]
– 99
[F9]
[SERVICE FUNCTIONS]
[FAULT LOG]

Note

Pressing the [**Special Fctn**] hardkey followed by the [F9] softkey, [+/–], [**9**], [**9**], and the [F9] softkey, enables and displays the [SERVICE FUNCTIONS] softkey. The [SERVICE FUNCTIONS] softkey remains enabled until power to the analyzer is removed.

Calibration Correction Curves

The calibration correction curves can be viewed for any input range or frequency span in the 50Ω input path. Figure 10-2 shows a typical calibration curve for the following instrument set up:

[**Preset**]
[**Range/Input**]
    [AUTORANGE ON **OFF**]
    [RANGE] (any range from –20 to +20 dBm)
[**Meas Type**]
    [LOW DIST ON OFF] (low distortion mode can be on or off)
[**Scale**]
    [REF TRACK ON **OFF**]
    [REFERENCE LEVEL]
    10
    [VERTICAL /DIV]
    1
    [dB]
[**Special Fctn**]
    [AUTO CAL ON **OFF**]
    [F9]
    – 99
    [F9]
    [SERVICE FUNCTIONS]
    [CAL OPTIONS]
    [CAL TRC **ON** OFF]
    [IF ATTEN ON OFF] (IF attenuation corrections can be on or off)
    [IF SHAPE ON OFF] (IF shape corrections can be on or off)
    [SOURCE ON OFF] (source corrections can be on or off)

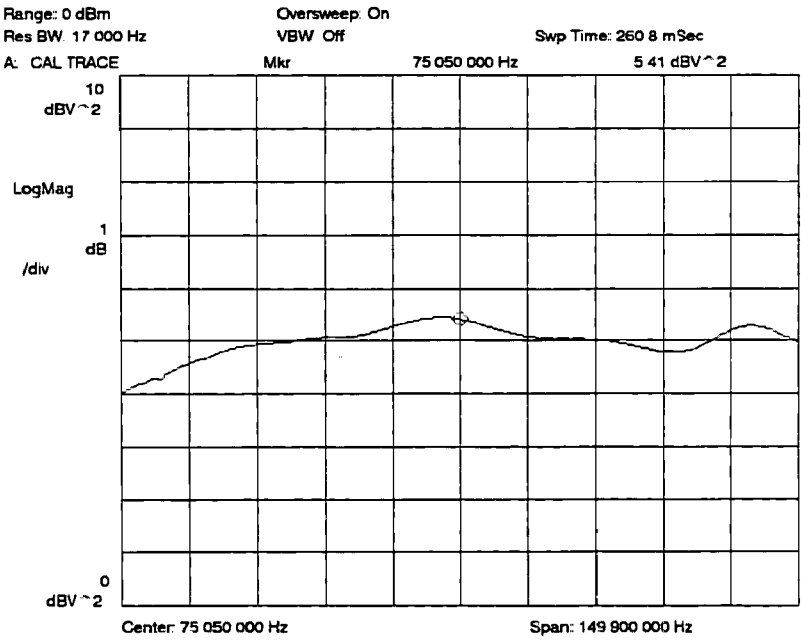


Figure 10-2. Typical 50 Ohm Input Calibration Curve

The calibration correction curves can be viewed for any frequency span in the 1 MΩ input path. Figure 10-3 shows a typical calibration curve for the following instrument set up:

[**Preset**]
[**Range/Input**]
[1 MEGOHM]
[AUTORANGE ON **OFF**]
[RANGE] (any range from –20 to +20 dBm)
[**Freq**]
[STOP]
40
[MHz]
[**Scale**]
[REF TRACK ON **OFF**]
[REFERENCE LEVEL]
10
[VERTICAL /DIV]
1
[dB]

[**Special Fctn**]

[AUTO CAL ON **OFF**]
[F9]
– 99
[F9]
[SERVICE FUNCTIONS]
[CAL OPTIONS]
[CAL TRC **ON** OFF]
[IF ATTEN ON OFF] (IF attenuation corrections can be on or off)
[IF SHAPE ON OFF] (IF shape corrections can be on or off)
[SOURCE ON OFF] (source corrections can be on or off)

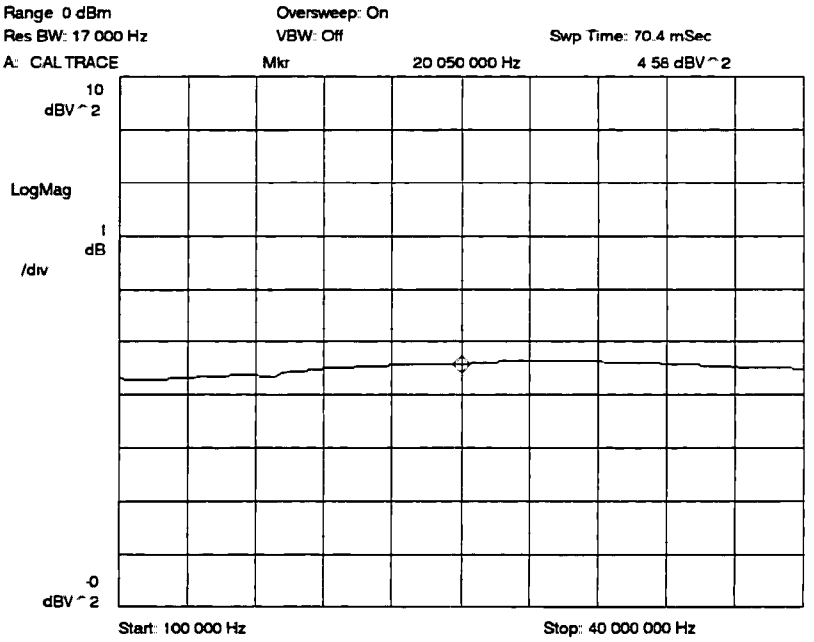


Figure 10-3. Typical 1 Meg Ohm Input Calibration Curve

Fault Log Messages

250 kHz Sample Clock failure	This error message occurs if a circuit on the ADC/Digital Filter assembly does not detect the 250 kHz reference signal from the Trigger assembly.
10 MHz third LO failure	This error message occurs if a circuit on the IF assembly does not detect the 10 MHz reference signal from the Reference/Calibrator assembly.
80 MHz clock failure	This error message occurs if a circuit on the ADC/Digital Filter assembly does not detect the 20 MHz clock signals. The 20 MHz clock signals are derived from dividing the 80 MHz reference signal by four. Since the Reference/Calibrator assembly's 80 MHz reference is the analyzer's primary frequency reference, many failures occur if the 80 MHz reference is not present.
300 MHz Ref Unlocked	This error message occurs if the control voltage for the 300 MHz VCO is too high or too low, indicating that the 300 MHz VCO is unlocked. Since the 300 MHz VCO is the analyzer's high frequency reference, many failures occur if it is unlocked. If the primary frequency reference from the Reference/Calibrator assembly is not present, the 300 MHz VCO unlocks.
Calibration failure	This error message occurs if the calibration routine generates correction vectors that exceed the maximum allowable error vectors.
Detector Gate Array DMA over-run	This error message occurs if the ADC/Digital Filter assembly's detector gate array detects an acknowledge signal from the CPU assembly's DMA controller when a request is not pending.
Detector Gate Array illegal input	This error message occurs if the ADC/Digital Filter assembly's digital filter gate array sends data to the detector gate array in an illegal format.
Filter Gate Array always busy	This error message occurs if the ADC/Digital Filter assembly's gate array takes too long to change out of "run" mode.
Filter Gate Array input over-sample	This error message occurs if the ADC/Digital Filter assembly's sample time is too short.
Frac N unlocked - frequency too high	This error message occurs if a circuit on the Interpolation VCO assembly detects that the amplitude of the fractional-N control voltage is too low (frequency too high). The fractional-N control voltage is monitored when the local oscillator is in multiple loop mode or single loop mode even though the Interpolation VCO is not used in single loop mode. Since the fractional-N control voltage is the same as the single loop control voltage, checking the fractional-N control voltage is essentially the same as checking the single loop control voltage.

Frac N unlocked - frequency too low	This error message occurs if a circuit on the Interpolation VCO assembly detects that the amplitude of the fractional-N control voltage is too high (frequency too low). The fractional-N control voltage is monitored when the local oscillator is in multiple loop mode or single loop mode even though the Interpolation VCO is not used in single loop mode. Since the fractional-N control voltage is the same as the single loop control voltage, checking the fractional-N control voltage is essentially the same as checking the single loop control voltage.
Internal measurement DMA Timeout	This error message occurs when any of the internal measurements fail because of unavailable data.
I2C: No Device Acknowledge	This error message occurs if the CPU assembly's IIC controller does not sense the acknowledge part of the formal handshake used to transmit data over the IIC bus.
I2C: Timeout	This error message occurs if the CPU assembly's IIC controller takes too long to tell the MPU that it is ready for a new command.
Input Tripped	This error message occurs if an overload occurs in the Input assembly's 50Ω impedance path. When this occurs, relays disconnect the input signal from the front panel.
LSWEEP timed-out	This error message occurs if the ADC/Digital Filter assembly does not sense an LSWP\ signal from the Trigger assembly during the time expected.
Power-on ROM Checksum error	This error message occurs if a power-on test detects a ROM checksum error.
Power-on test failure	This error message occurs if a power-on test fails.
Source Tripped	This error message occurs if the voltage at the output of the Source Amplifier assembly exceeds the threshold set by the Source Conversion assembly. When this occurs, the source output is disconnected from the front panel.
Step Loop unlocked	This error message occurs if a circuit on the Step Phase Detector assembly detects that the step loop control voltage is too high or too low, indicating that the step loop is unlocked. The control voltage is clamped to service adjustable limits when the step loop is unlocked.
Sum Loop unlocked	This error message occurs if a circuit on the Sum Phase Detector assembly detects that the amplitude of the integrator output is too high or too low, indicating that the sum loop is unlocked. The integrator output is clamped when the sum loop is unlocked.

Self-Test Descriptions

Thirty-six self tests are available that can be run in groups or individually. Table 10-3 lists the assemblies used by the self tests and shows the assembly that would be the most likely cause of a self-test failure. To run these self tests in the order shown, press the following keys:

[**Special Fctn**]
[F9]
– 99
[F9]
[SERVICE FUNCTIONS]
[SELF TEST]
[FUNCTIONL TESTS]
[ALL]

To run a single self test, press the softkey shown in the table instead of [ALL]. To determine the key path for the self-test softkeys, see table 10-4, "Self-Test Menu Map and HP-IB Commands."

Note

Certain instrument malfunctions cause multiple self-test failures. Therefore, to determine the most likely cause when more than one self test fails, look in table 10-3 for assemblies common to all failing self tests.

Table 10-3. Assemblies Used in Self Tests

Self Test Softkey	Assembly																		
	A81	A87	FP	DD	A62	A61	A13	A12	A11	A42	A41	A33	A32	A31	A52	A51	A24	A23	A22	A21
[PROCESSOR]†	X	0			0									0						
[ROM]†	0	X			0									0						
[RAM]†	0	X			0									0						
[INTERRUPT]	X	0			0									0						
[MULTI FCTN PERIPHERL]	X	0			0									0						
[DISPLAY DGTL HW]	X	0			0									0						
[DMA]	X	0			0									0						
[MATH COPROCSSR]	X	0			0									0						
[HP-IB FUNC TEST]	X	0			0									0						
[DISK CONTROLLR]	X	0			0									0						
[IIC BUS]	X	0	X		X				X	X	X	X		X	X	X		X		
[FAST BUS]‡	X	0			X									0						
[FRONT PANEL]‡	0	0	X		0									0						
[DIGITAL FILTER]	0	0			X							0	0	0						
[DETECTOR]	0	0			X							0	0	0						
[187.5 kHz REFERENCE]	0	0			0					X	0	0	0	0						
[GILBERT CELL]	0	0			0					X	0	0	0	0						
[MULT-LOOP TUN RANGE]	0	0			0							0	0	0	X	X		0		
[SNGL LOOP TUN RANGE]	0	0			0							0	0	0	X	X		0		X
[OUTPUT CKTS]	0	0			0					X	X	0	0	0	0	0	0	0	0	0
[2ND IF LEVEL]	0	0			0	X	X	X	X	0	0	0	0	0	0	0	0	0	0	0
[ADC]	0	0			X	0	0	0	0			0	0	0	0	0	0	0	0	0
[POST DIVIDER]	0	0			0	0	0	0	0			0	0	0	0	X	0	0	0	0
[AUTO RNG TRIP PTS]	0	0			0	0	0	0	X	0	X	0	0	0	0	0	0	0	0	0
[10 MHz LOCAL OSC]	0	0			0	0	0	0	0			X	X	X	X	X	X	X	X	X
[FLATNESS]	0	0			0	0	0	0	0	X	X	0	0	0	0	0	0	0	0	0
[QUICK CONF TEST]	0	0			X	X	X	X	X	X	X	0	0	X	0	0	0	0	0	0

X This assembly could be the cause of the failure message

0 This assembly is probably not the cause of the failure message but could be.

No symbol means that the assembly is not used by the self test.

† Low-level power-on tests

‡ High-level power-on tests

The motherboard, power supply, and display are used in every test.

Self Tests that Perform a Measurement

The following self tests perform measurements:

- ADC
- POST DIVIDER
- AUTO RNG TRIP PTS
- 10 MHz LOCAL OSC
- FLATNESS
- TEST SET

The measurements bypass any standard corrections and do not perform calibration data corrections. Therefore, all self-test measurements using analog data have limits larger than the standard calibration tolerances.

Some hardware setup modes used in these self tests are not used by normal measurements and cannot be accessed from the front panel. Once the hardware is set up, data is taken and time records are processed according to the needs of the specific test. Some tests monitor overloads, others require spectrum data, and others require time record data. After the data is collected, it is compared to an internal reference specification to determine if the self test passed or failed. The pass or fail information along with any additional information is placed in the Test Log.

Individual Self-Test Descriptions

[187.5 kHz REFERENCE]
(Source 187.5 kHz)

This test verifies that the reference signal is present at the input of the 187.5 kHz limiter on the Source Conversion assembly. In this test, a detector forces 187.5_SIG\ low if the 187.5_KHZ_SRCE signal is present. The Source Amplifier assembly provides control logic for 187.5_SIG\ and sends this information to the CPU assembly over the IIC bus.

[10 MHz LOCAL OSC]
(Receiver 10 MHz)

This test verifies that the swept LO signal, 300 MHz, 10 MHz, and 250 kHz reference signals are at the proper frequency. In this test, the 10 MHz calibration signal from the Reference/Calibrator assembly is connected to the receiver (the Input, First Conversion, Second Conversion, IF, and ADC/Digital Filter assemblies). This test then checks the output frequency of the ADC on the ADC/Digital Filter assembly.

[2ND IF LEVEL]
(Receiver 2nd IF)

This test verifies the integrity of the signal path through the Input, First Conversion, and Second Conversion assemblies up to the IF assembly. In this test the receiver's range is set to − 20 dBm and a 0 dBm signal (NORMALIZE) from the Source Amplifier assembly is connected to the Input assembly. The detector on the IF assembly forces SIG_DET high. The receiver's range is changed to 0 dBm, and SIG_DET returns to a logic low. The ADC/Digital Filter assembly provides the control logic for the SIG_DET signal and sends this information to the CPU assembly over the IIC bus.

[ADC]
(Receiver ADC)

This test verifies that the ADC on the ADC/Digital Filter assembly is functioning correctly. This test consists of 7 tests − positive overflow, negative overflow, positive limit, negative limit, 1st pass, 2nd pass, and zero. The positive and negative overflow tests set up the ADC test mode to cause positive and negative overflows, then checks the digital filter for interrupt flags The positive and negative limit tests check the ADC's positive and negative limits. The 1st and 2nd pass tests connect the 10 MHz calibration signal from the Reference/Calibrator assembly to the Input assembly. The 1st pass test sets the 2nd pass result to zero and checks the signal into the ADC for the proper value and the gate array for interrupts or overloads. The 2nd pass test sets the 1st pass result to zero and checks the signal into the ADC for the proper value and the gate array for interrupts or overloads. The zero test checks for minimal output when the signal is removed.

[AUTO RNG TRIP PTS]
(Receiver autorange)

This test checks all the selectable attenuator ranges on the A11 Input assembly. This test measures the level of the swept calibrator signal through each attenuator setting in the 50 Ω and 1 MΩ path. If all the 1 MΩ attenuator ranges fail, a warning about the A11 Input assembly's configuration is printed in the test log. This test also verifies that the receiver's auto range trip points are set correctly. This test calibrates the source at − 20 dBm, then connects the NORMALIZE signal from the Source Amplifier assembly to the Input assembly. The NORMALIZE signal is increased until the range up trip point is found, then decreased until the range down trip point is found. This test compares the trip points to acceptable levels.

[DETECTOR]
(Detector gate array)

This test verifies that the detector on the ADC/Digital Filter assembly is operating correctly. The microprocessor on the CPU assembly writes data to the detector over the fast bus. The microprocessor then reads the data and compares it to the data sent.

[DIGITAL FILTER]
(Digital filter gate array)

This test verifies that the digital filter's gate array on the ADC/Digital Filter assembly is operating correctly. The CPU assembly's microprocessor configures the digital filter's gate array over the fast bus. The microprocessor then reads the control lines to check circuits internal to the gate array and verify correct configuration. This test also writes to and reads from the gate array's RAM, checking for stuck bits.

[DISK CONTROLLR]
(Disk controller)

This test verifies that the disk controller on the CPU assembly is operating correctly. In this test, the microprocessor sends an invalid command to the disk controller, and the disk controller reports the command as invalid.

[DISPLAY DGTL HW]
(Display digital)

This test checks that the display controller on the CPU assembly is operating correctly. In this test, the microprocessor writes a pattern to the display controller, then reads the pattern checking for errors.

[DMA]
(DMA)

This test checks the DMA controller on the CPU assembly. In this test, the microprocessor writes to the DMA controller, then reads the registers checking for errors.

[FAST BUS]
(Fast bus)

This test verifies that the fast bus is operating correctly. In this test, the microprocessor on the CPU assembly writes data to the detector gate array on the ADC/Digital Filter assembly over the fast bus. The microprocessor then reads data.

[FLATNESS]
(Source flatness)

This test verifies the flatness of the source (Source Conversion and Source Amplifier assemblies) for all attenuator settings (10 dBm to − 50 dBm in 10 dB steps) from 200 kHz to 150 MHz. This test connects the NORMALIZE signal from the Source Amplifier assembly to the Input assembly. The receiver (the Input, First Conversion, Second Conversion, IF, and ADC/Digital Filter assemblies) measures the signal, and the microprocessor on the CPU assembly compares the results to acceptable levels.

[FRONT PANEL]
(Front panel)

This test verifies that the IIC controller on the Front Panel assembly is operating correctly. In this test, the microprocessor on the CPU assembly reads the IIC controller on the Front Panel assembly and verifies that no front-panel keys are held down.

[GILBERT CELL]
(Source gilbert cell)

This test verifies that the gilbert cell multiplier on the Source Conversion assembly is operating correctly. In this test, the gilbert cell generates a full scale signal and a detector forces 187.5_SIG\ low. The gilbert cell reduces its amplitude and 187.5_SIG\ returns to a logic high. The Source Amplifier assembly provides control logic for 187.5_SIG\ and sends this information to the CPU assembly over the IIC bus.

[HP-IB CONNECTOR]

This is a user-interactive test of the HP-IB connector on the CPU assembly. In this test, a diagram of the HP-IB connector is displayed on the screen. The user then connects an HP-IB pin to ground, and the pin is highlighted on the screen. See Test 12. HP-IB/RS-232 for the procedure to use with this softkey.

[HP-IB FUNC TEST]
(HP-IB)

This test verifies that the HP-IB interface on the CPU assembly is operating correctly. In this test, the microprocessor sets the HP-IB interface to a listen only state, then tests for a listen only state.

[IIC BUS]
(IIC bus)

This test verifies that the CPU assembly can write to and read from all assemblies with IIC interfaces. This test also checks the CPU assembly's EEROM. The following assemblies have IIC interfaces:

Front Panel
A11 Input
A23 Step Phase Detector
A31 Reference/Calibrator
A33 Trigger
A41 Source Conversion
A42 Source Amplifier (write only)
A51 Interpolation VCO
A52 Fractional-N
A62 ADC/Digital Filter

[INTERRUPT]
(Interrupt)

This test verifies that the interrupt circuits on the CPU assembly are operating correctly. In this test, the microprocessor writes to the interrupt registers and reads the registers for verification.

[LONG CONF TEST]

This test performs most of the self tests. The tests are performed in the following order:

[PROCESSOR]
[RAM]
[ROM]
[INTERRUPT]
[MULTI FCTN PERIPHERL]
[DISPLAY DGTL HW]
[FRONT PANEL]
[HP-IB FUNC TEST]
[IIC BUS]
[FAST BUS]
[DMA]
[MATH COPROCSSR]
[SNGL LOOP TUN RANGE]
[MULT-LOOP TUN RANGE]
[POST DIVIDER]
[AUTO RNG TRIP PTS]
[10 MHz LOCAL OSC]
[2ND IF LEVEL]
[ADC]
[DIGITAL FILTER]
[DETECTOR]
[TRIGGER]
[187 5 kHz REFERENCE]
[GILBERT CELL]
[OUTPUT CKTS]
[FLATNESS]
[QUICK CONF TEST]

[MATH COPROCSSR]
(Math coprocessor)

This test verifies the processing capability of the TMS320 signal processor on the CPU assembly. In this test, the microprocessor reads from and writes to the TMS320's SRAM. This test also does two cyclic redundancy checks on the TMS320's SRAM contents.

[MOTOR]
(Disk motor)

This test verifies that the Disk Drive assembly's motor is operating correctly. In this test, the CPU assembly's disk controller instructs the Disk Drive assembly to turn its motor on and off. While the motor is turning on and off, the disk controller monitors the DISK_READY\ signal. This test requires a flexible disk.

[MULT FCTN PERIPHERL]
(Mult fctn peripheral)

This test verifies that the MFP (multi-function peripheral) on the CPU assembly is operating correctly. In this test, the microprocessor writes to the MFP, then reads the registers checking for errors.

[MULT-LOOP TUN RANGE]
(Mult loop tuning range)

This test checks the tuning range of the local oscillator's interpolation loop (Interpolation VCO and Fractional-N assemblies). In this test, the local oscillator is in multiple loop mode and the Interpolation VCO's frequency is set to a minimum locking value. Then while monitoring the interpolation loop for an unlock condition, the Interpolation VCO's frequency is decreased until the loop unlocks. This test then sets the Interpolation VCO's frequency to a valid locking value and checks that the loop locked. Next this test sets the Interpolation VCO's frequency to a maximum locking value. Then while monitoring the interpolation loop for an unlock condition, the Interpolation VCO's frequency is increased until the loop unlocks. This test then sets the Interpolation VCO's frequency to a valid locking value and checks that the loop locked.

[OUTPUT CKTS]
(Source output level)

This test checks the output of the Source Amplifier assembly and verifies that the source can reduce its amplitude. In this test, the overload threshold is lowered and the overload detection circuit detects an overload. Then the source amplitude is reduced, and the overload detection circuit verifies that the overload is gone.

[POST DIVIDER]
(Post divider)

This test checks for proper operation of the divide-by-10/divide-by-5 circuit on the Interpolation VCO assembly. In this test, the local oscillator is in multiple loop mode, and the 10 MHz calibration signal is connected to the receiver. While the receiver is measuring the signal, the divide by number is changed from 10 to 5. This causes the frequency the receiver is measuring to change, indicated by the receiver unable to measure the calibration signal.

[PROCESSOR]
(Processor)

This test verifies that the microprocessor on the CPU assembly is operating correctly. In this test, the following microprocessor operations are tested:

Immediate move and compare instructions
Data and address registers
Data direct and address direct addressing modes
AND, EOR, OR, multiply, divide, shift, and rotate

[QUICK CONF TEST]
(Quick confidence)

This test calibrates the analyzer and checks the calibration limits. See "Calibration Routine" earlier in this chapter for a description of the calibration routine. This test lists the following calibration correction information in the test log:

LO null real: n, imag: n
1 MOhm nominal crtn: n
50 Ohm nominal crtn: n
src crtn: gain: n, offset: n

The **LO null real** and **imag** numbers are the calibration correction numbers to null the receiver's LO feedthrough. These numbers can range from 1 to 100, but typically range from 40 to 90. The nominal number is 50. This test fails if either the real or the imaginary number is 1 or 100.

The **1 MOhm and 50 Ohm nominal crtn** numbers are the calibration correction numbers for the receiver's 1 MΩ input path and 50Ω input path (− 20 dBm range, no attenuators engaged). The nominal number is 1.0 with typical numbers ranging from 0.4 to 2.5. When either the 1 MΩ or the 50Ω input path can not be calibrated, this test fails and the correction number is set to 1.000 (no correction applied).

The **src crtn gain** and **offset** numbers are the calibration gain and offset correction numbers for the source. The nominal number for gain is 1.00 with typical numbers ranging from 0.7 to 1.4. The nominal number for offset is 0 with typical numbers ranging from − 5 to 7.

[RAM]
(RAM)

This test checks the RAM on the Memory assembly. Before writing to a memory location, this test stores the memory contents in a register. The memory location is restored after the memory is tested. This test disables the keyboard and all interrupts.

[RANDOM SEEK]
(Disk random seek)

This test verifies that the Disk Drive assembly's head can move to a random sector on the flexible disk. In this test, the disk controller on the CPU assembly instructs the disk-drive head to move to a random sector. This test requires a flexible disk that is not write protected.

[READ]
(Disk read)

This test verifies that the Disk Drive assembly can read a flexible disk. In this test, the CPU assembly's disk controller instructs the Disk Drive assembly to read the current sector on the flexible disk. While the current sector is being read, the disk controller monitors the READ_DATA\ signal to verify the read operation. The current sector is set by the [SEEK SECTOR] test. This test requires a flexible disk that is not write protected.

[READ/WRITE]
(Disk read/write)

This test verifies that the Disk Drive assembly can read and write to a flexible disk. In this test, the CPU assembly's disk controller instructs the Disk Drive assembly to read the current sector on the flexible disk. While the current sector is being read, the disk controller monitors the READ_DATA\ signal to verify the read operation. The disk controller then instructs the Disk Drive assembly to write to the current sector. While the current sector is being written to, the disk controller monitors the WRITE_DATA\ signal to verify the write operation. The current sector is set by the [SEEK SECTOR] test. This test requires a flexible disk that is not write protected.

[READ/WRITE ALL]
(Disk read/write all)

This test verifies that the Disk Drive assembly can read and write to all sectors of a flexible disk. In this test, the CPU assembly's disk controller instructs the Disk

Drive assembly to read every available sector on the flexible disk (excluding privileged tracks). While the flexible disk is being read, the disk controller monitors the READ_DATA\ signal to verify the read operation. The disk controller then instructs the Disk Drive assembly to write to every available sector on the flexible disk (excluding privileged tracks). While the flexible disk is being written to, the disk controller monitors the WRITE_DATA\ signal to verify the write operation. This test stops on the first error. If there are no errors, this test takes approximately 20 minutes to complete. This test requires a flexible disk that is not write protected.

[RESTORE]
(Disk restore)

This test verifies that the Disk Drive assembly's head can move away from track 0, then back to track 0. In this test, the CPU assembly's disk controller instructs the disk-drive head to move away from track 0, then back to track 0. The disk controller monitors the T00\ signal to verify the move operation. This test requires a flexible disk that is not write protected.

[ROM]
(ROM)

This test calculates and verifies checksums for the program ROMs on the Memory assembly.

[SEEK SECTOR]
(Disk sector seek)

This test verifies that the Disk Drive assembly's head can move to a user specified sector on the flexible disk. In this test, the disk controller on the CPU assembly instructs the disk-drive head to move to a user specified sector. The user specified sector number must be in the range of valid sector numbers. The default sector number is 1. This test requires a flexible disk that is not write protected.

[SNGL LOOP TUN RANGE]
(Single loop tuning range)

This test checks the tuning range of the local oscillator's single loop (Sum VCO, Interpolation VCO, and Fractional-N assemblies). In this test, the local oscillator is in single loop mode and the Sum VCO's frequency is set to a minimum locking value. Then while monitoring the single loop for an unlock condition, the Sum VCO's frequency is decreased until the loop unlocks. This test then sets the Sum VCO's frequency to a valid locking value and checks that the single loop locked. Next this test sets the Sum VCO's frequency to a maximum locking value. Then while monitoring the single loop for an unlock condition, the Sum VCO's frequency is increased until the loop unlocks. This test then sets the Sum VCO's frequency to a valid locking value and checks that the single loop locked.

[TEST PATTERN]

This is a user-interactive test of the Display assembly and the CPU assembly's display controller. In this test, a test pattern is displayed on the screen. See adjustment 18, "Display."

[TEST SET]
(Test set)

This test verifies that the HP 35689A/B S-Parameter Test Set is functioning correctly. The first part of this test checks the A2 Controller assembly. The Controller assembly clears the relay control latch on the A1/A11 RF assembly. The Controller assembly then individually clears and sets all seven bits. After each bit is cleared or set, this test checks the relay bit setting. If the Controller assembly did not respond or if a relay bit setting is not correct, an error message is placed in the test log. Since there is a delay between each change in relay settings, you should be able to hear the relays switch fourteen times during the first part of this test. The second part of this test uses the analyzer to check the analog circuits on the A1/A11 RF assembly and the A3/A4 Directional Bridge assemblies. The analyzer sweeps from 200 kHz to 150 MHz with the source amplitude set to 10 dBm. The analyzer measures the test set's forward and reverse reference path for acceptable signal attenuation and frequency response flatness. If both reference paths have acceptable signal attenuation and frequency response flatness, then this test compares the frequency response flatness of each path to check that they match. The measured flatness of each path and the ratio match between the paths is entered into the test log.

[TRIGGER]
(Trigger/Gate)

This test checks the LSWP\ signal generated by the A33 Trigger assembly. The A62 ADC/Digital Filter assembly measures the LSWP\ period in swept-network measurement mode at all resolution bandwidth settings, then in edge-gated swept-spectrum measurement mode at several different resolution bandwidth settings. The test compares the measured period to the calculated period.

Table 10-4. Self Test Menu Map and HP-IB Commands

Self Test	HP-IB Command
[SELF TEST]	
[QUICK CONF TEST]	TEST:SHOR
[LONG CONF TEST]	TEST:LONG
[FUNCTIONL TESTS]	
[CPU]	
[PROCESSOR]	TEST:PROC:CPU
[RAM]	TEST:PROC:RAM
[ROM]	TEST:PROC:ROM
[INTERRUPT]	TEST:PROC:INT
[MULT FCTN PERIPHERL]	TEST:PROC:MFP
[DISPLAY DGTL HW]	TEST:PROC:DISP
[ALL]	TEST:PROC:ALL
[DISPLAY]	
[TEST PATTERN]	TEST:DISP.PATT
[DMA]	TEST:PROC:DMA
[I/O]	
[FRONT PANEL]	TEST:IO:FPAN
[HP-IB]	
[HP-IB FUNC TEST]	TEST:IO:GPIB
[HP-IB CONNECTOR]	
[INTERNAL DISK]	
[DISK CONTROLLR]	TEST:IO:DISK:CONT
[MOTOR]	TEST:IO:DISK:MOT
[RESTORE]	TEST:IO:DISK:REST
[RANDOM SEEK]	TEST:IO:DISK:RAND
[SEEK SECTOR]	TEST:IO:DISK:SEEK
[READ]	TEST:IO:DISK:READ
[READ/WRITE]	TEST:IO:DISK:WRIT
[READ/WRITE ALL]	TEST:IO:DISK:RWR
[ALL]	TEST:IO:DISK:ALL
[IIC BUS]	TEST:IO:IIC
[FAST BUS]	TEST:IO:FBUS
[ALL]	TEST:IO:ALL
[MATH COPROCSSR]	TEST:MATH
[LOCAL OSC]	
[SNGL LOOP TUN RANGE]	TEST:LOSC:SLO:TRAN
[MULT-LOOP TUN RANGE]	TEST:LOSC:MLO:TRAN
[POST DIVIDER]	TEST:LOSC:PDIV
[ALL]	TEST:LOSC:ALL

Table 10-4. Self Test Menu Map and HP-IB Commands (continued)

Self Test	HP-IB Command
[RECEIVER]	
[AUTO RNG TRIP PTS]	TEST:REC AUT
[10 MHz LOCAL OSC]	TEST:LOCS TENM
[2ND IF LEVEL]	TEST:IF:LEV
[ADC]	TEST:REC GARR
[DIGITAL FILTER]	TEST:DFIL:GARR
[DETECTOR]	TEST:DET:GARR
[TRIGGER]	TEST:TRIG
[ALL]	TEST:REC:ALL
[SOURCE]	
[FLATNESS]	TEST:SOUR:FLAT
[187 5 kHz REFERENCE]	TEST:SOUR:REF
[GILBERT CELL]	TEST:SOUR:GILB
[OUTPUT CKTS]	TEST:SOUR:LEV †
[ALL]	TEST:SOUR:
[ALL]	TEST ALL
[LOOP MODE ON OFF]	TEST LOOP ON TEST LOOP OFF
[TEST LOG]	TEST LOG:DATA?
[CLEAR TEST LOG]	TEST:LOG:CLE
[NEXT PAGE]	
[PREVIOUS PAGE]	
[TEST SET]	TEST:TSET

† This test will fail if the Source Amplifier assembly detects a voltage at its front-panel connector. Therefore, before running this test, disconnect any cable connected to the SOURCE connector.

Note

To view the analyzer's fault log via HP-IB, send SYST:FLOG:DATA?. To clear the fault log send SYST:FLOG:CLE.

Power-On and Preset State

The analyzer is in a known state after power up or after pressing the [**Preset**] key. Pressing the [**Preset**] key resets the analyzer as close to the power-on state as possible. States that are stored in battery-backed-up SRAM are listed in "Nonvolatile States." To view the power-on state, press [**Format**] [SETUP STATE] immediately after power up or after pressing the [**Preset**] key.

Nonvolatile States

The analyzer's serial number and options are stored in EEPROM on the CPU assembly. If the CPU assembly is replaced, the analyzer's serial number and options must be stored in EEPROM on the new assembly. See "Replacing the CPU Assembly" in chapter 6, "Replacing Assemblies."

The following lists user-accessible states that are stored in battery-backed-up SRAM on the Memory assembly. These states are NOT reset during power-on or by pressing the [**Preset**] key.

[**Disk Util**]
- [DEFAULT DISK]
  - [NON-VOL RAM DISK] or [VOLATILE RAM DISK] or [INTERNAL DISK] or [ROM DISK]

[**Local/HP-IB**]
- [SYSTEM CONTROLLR] or [ADDRESSBL ONLY]
- [ANALYZER ADDRESS]
- [PERIPHERL ADDRESSES]
  - [PLOTTER ADDRESS]
  - [PRINTER ADDRESS]

[**SAVE/RECALL**]
- [DEFAULT DISK]
  - [NON-VOL RAM DISK] or [VOLATILE RAM DISK] or [INTERNAL DISK] or [ROM DISK]

[**Special Fctn**]
- [NON-VOL SETUP]
  - [KEYBOARD SETUP]
    - [FRENCH] or [GERMAN] or [ITALIAN] or [SPANISH] or [SWEDISH/FINNISH] or [U.K. ENGLISH] or [U.S ENGLISH]
- [75 OHM SETUP]
  - [25 OHM] or [MINIMUM LOSS PAD]
- [TIME HHMM]
- [DATE MMDDYY]

11 Backdating

11

Backdating

Introduction

This chapter provides information necessary to modify this manual for instruments that differ from those currently being produced. The information in this chapter documents earlier instrument configurations and associated servicing procedures.

With the information provided in this chapter, this manual can be corrected so that it applies to any earlier version or configuration of the instrument.

12 Quick Reference

12

Quick Reference

Introduction

This chapter contains commonly used tables and all the block diagrams for the HP 3589A Spectrum/Network Analyzer and HP 35689A/B S-Parameter Test Set. All block diagrams, except the overall block diagrams, show the connector numbers for signals routed through RF cables. The block diagrams do *not* show connector numbers for signals routed through the analyzer's Motherboard assembly.

HP 3589A Spectrum/Network Analyzer

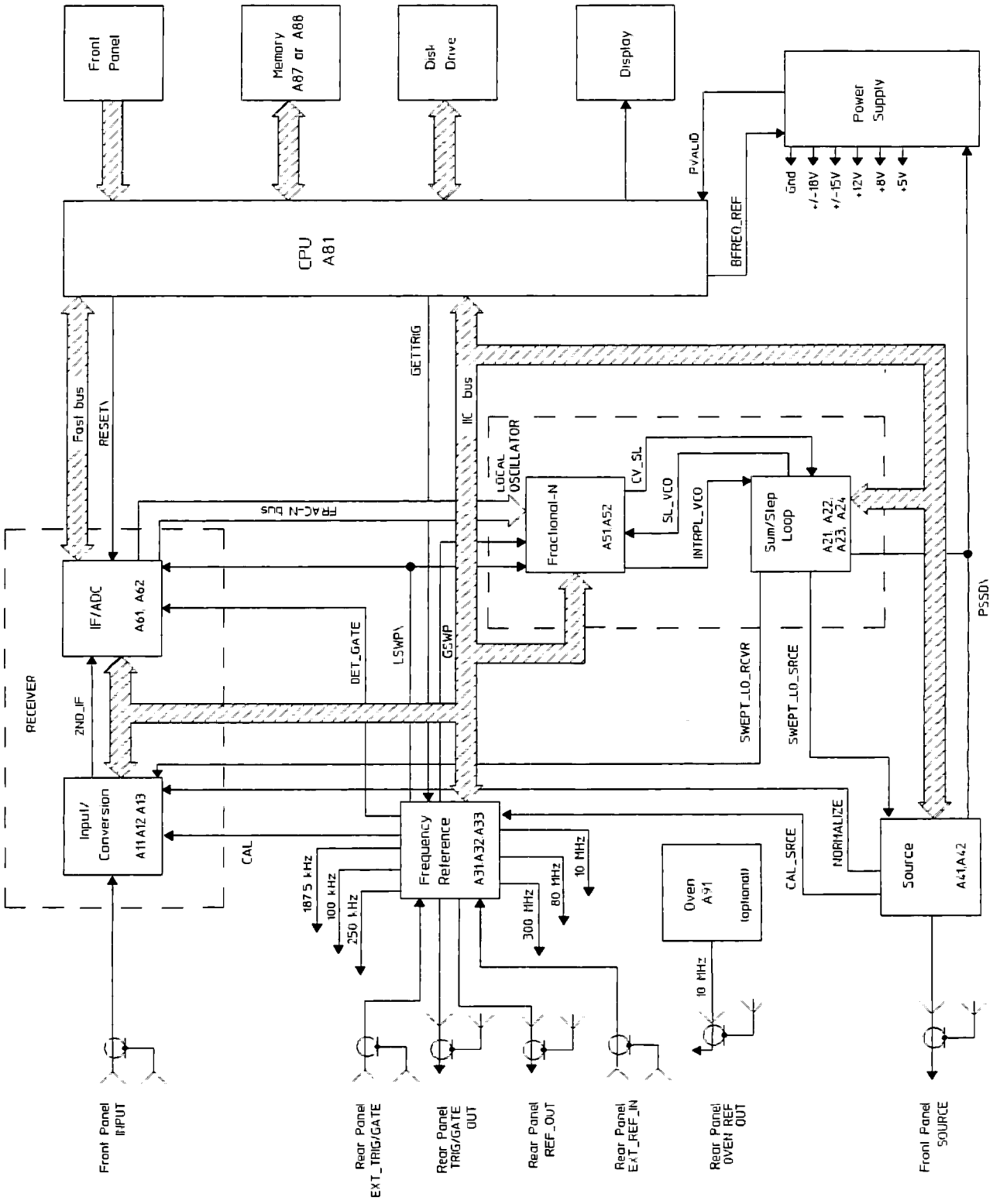


Figure 12-1. Overall Block Diagram

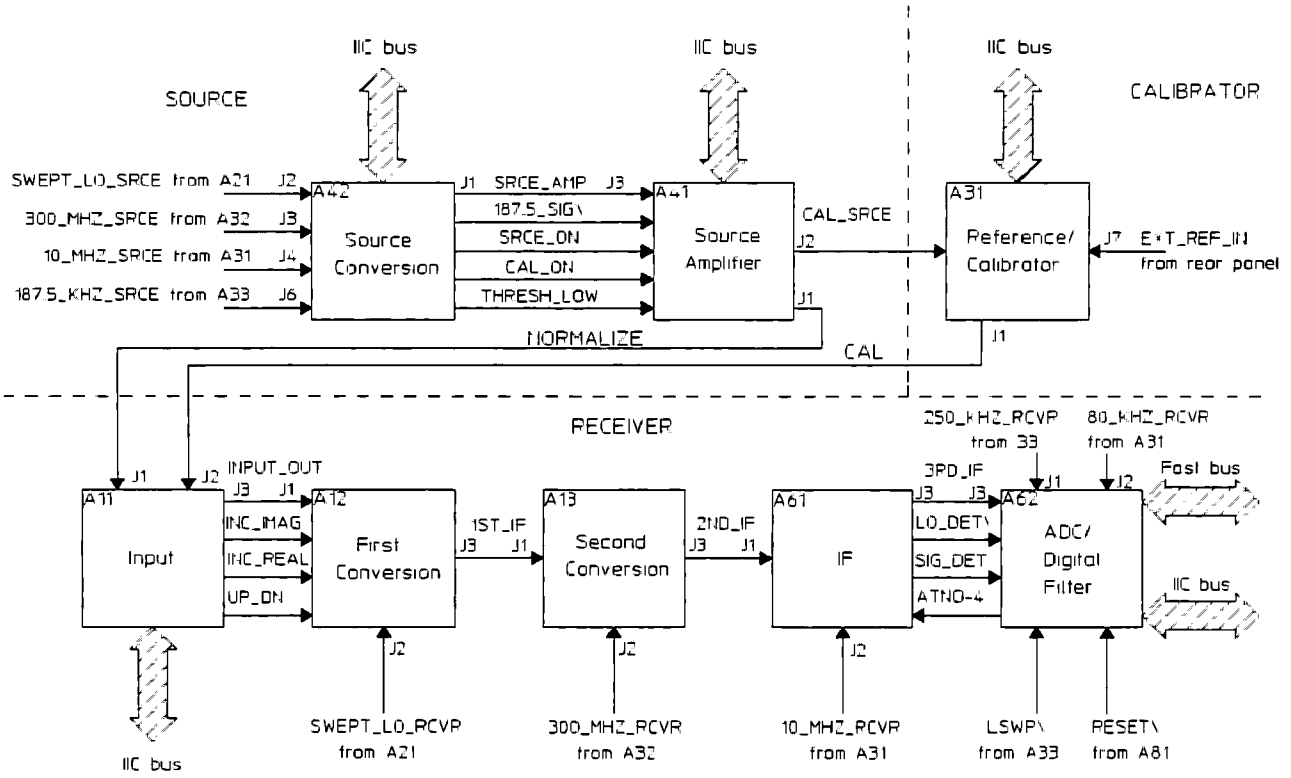


Figure 12-2. Calibration Block Diagram

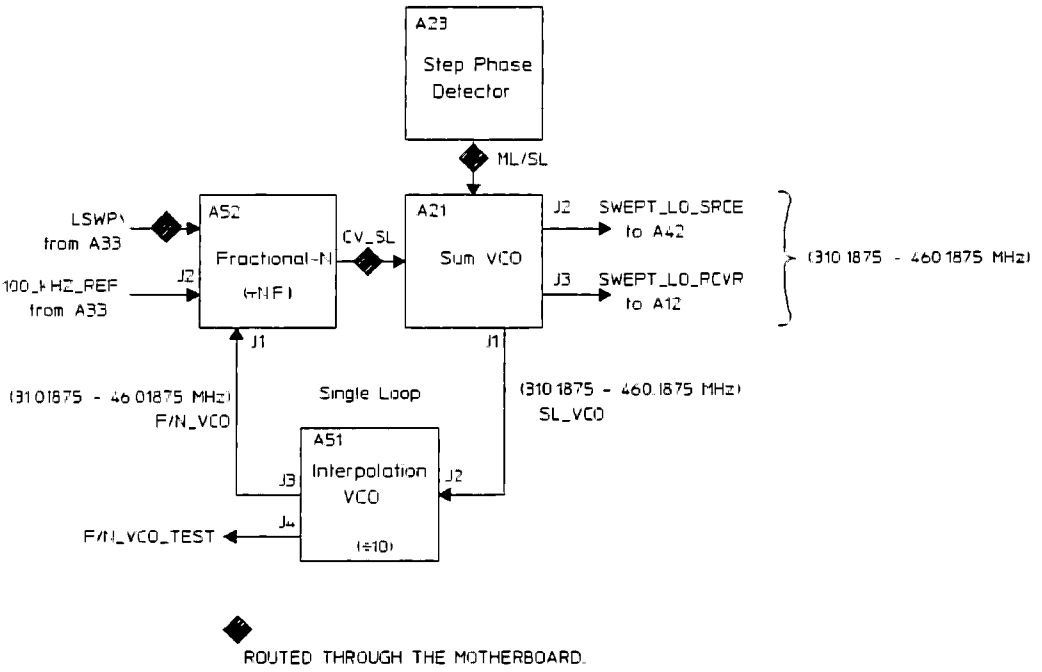


Figure 12-3. Local Oscillator in Single Loop Mode

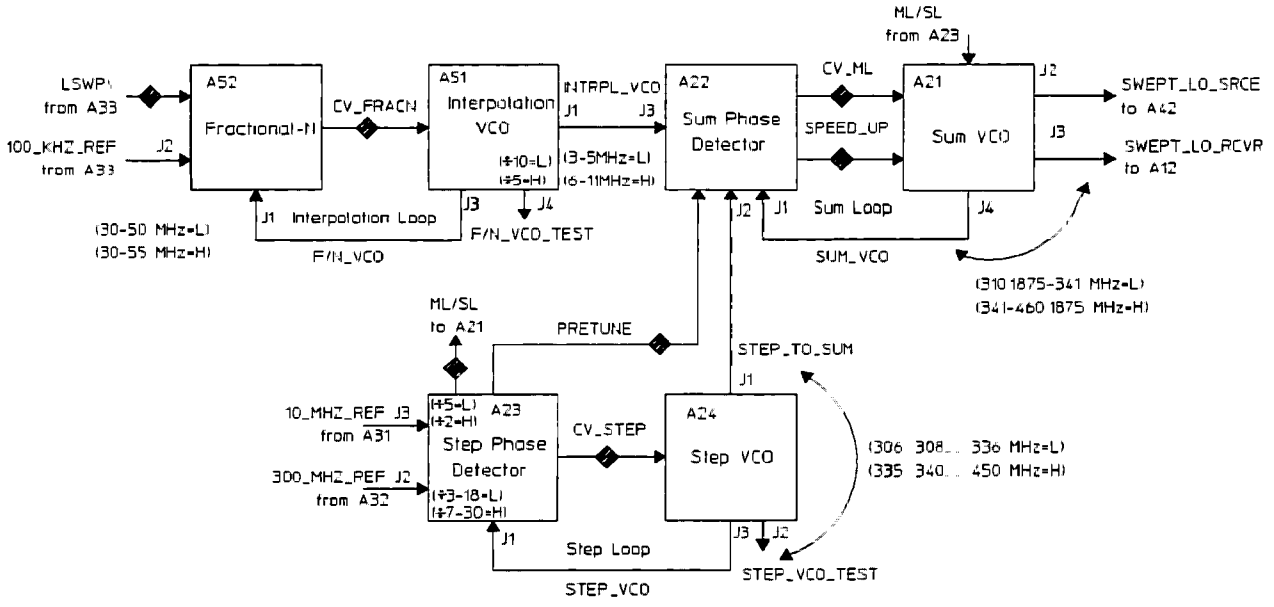


Figure 12-4. Local Oscillator in Multiple Loop Mode

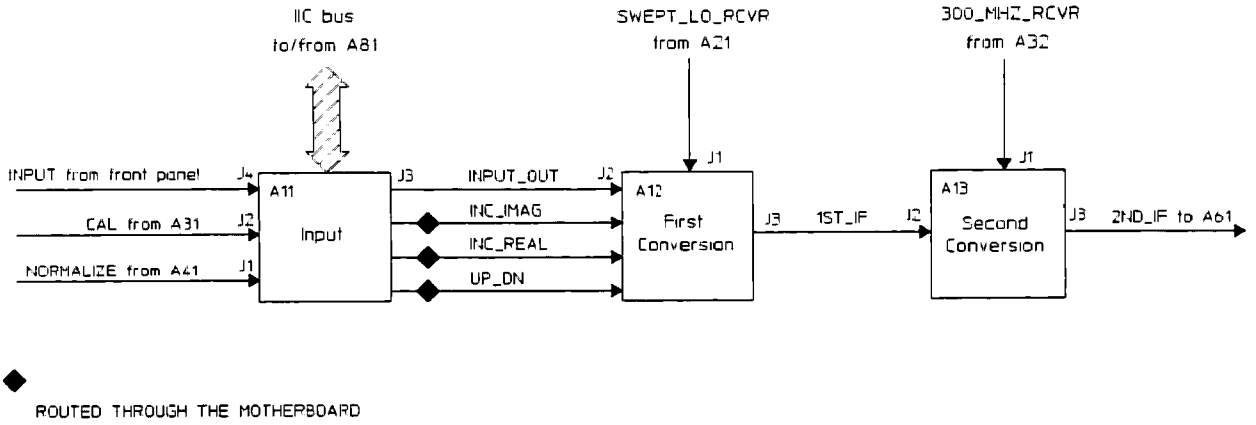


Figure 12-5. Input Conversion Block Diagram

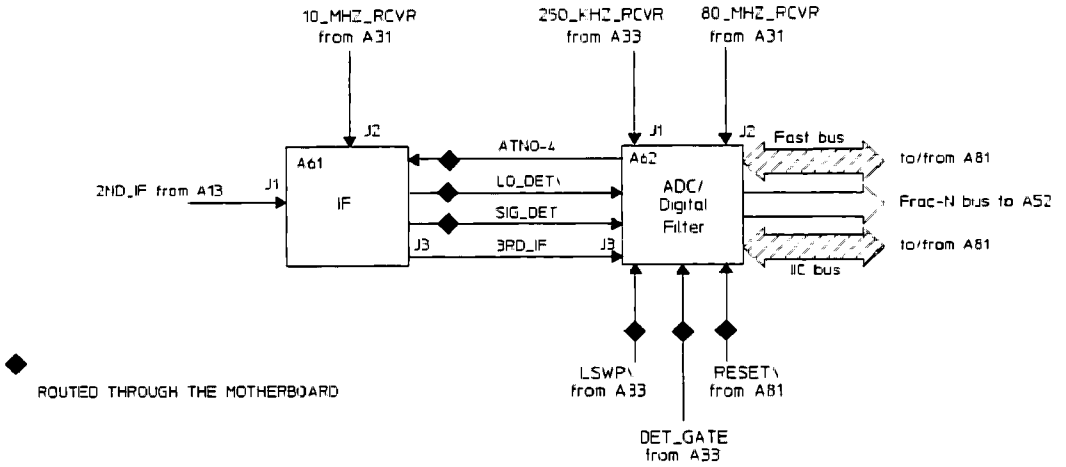


Figure 12-6. IF/ADC Block Diagram

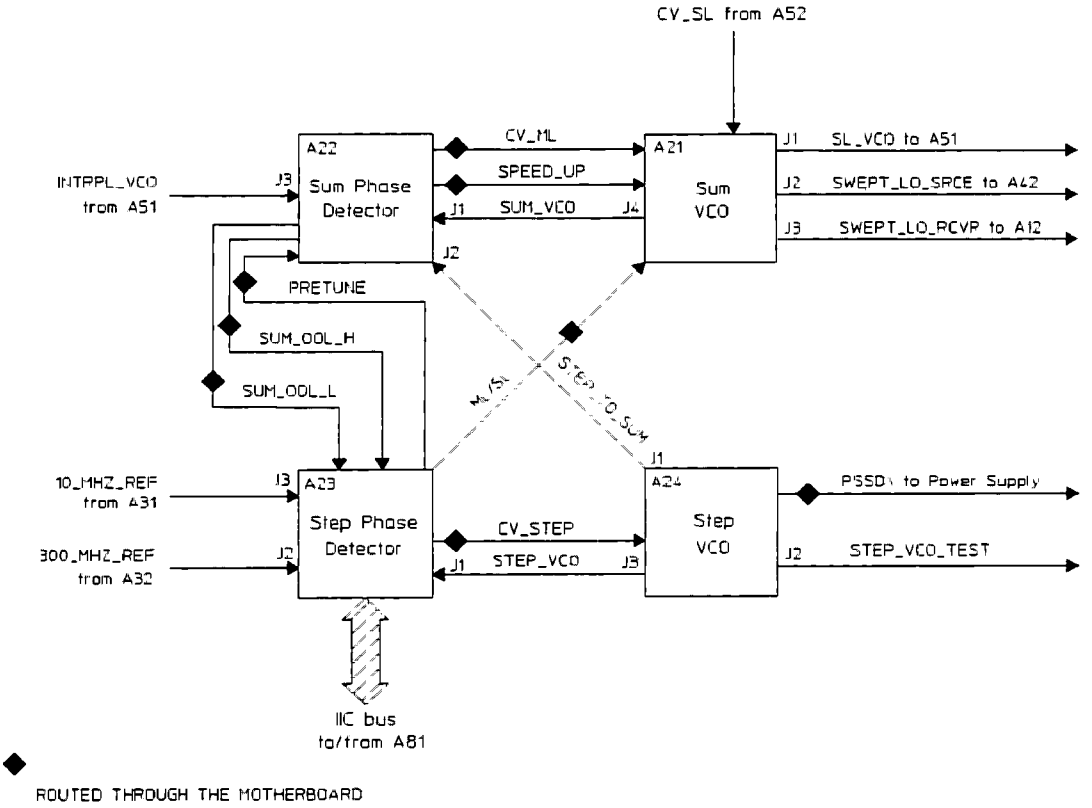


Figure 12-7. Sum and Step Loop Block Diagram

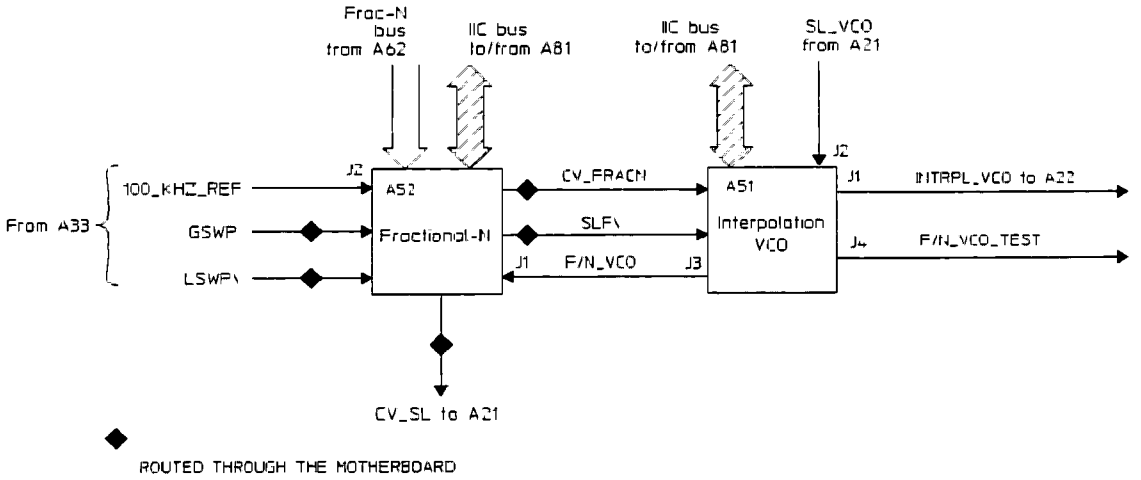


Figure 12-8. Fractional-N Block Diagram

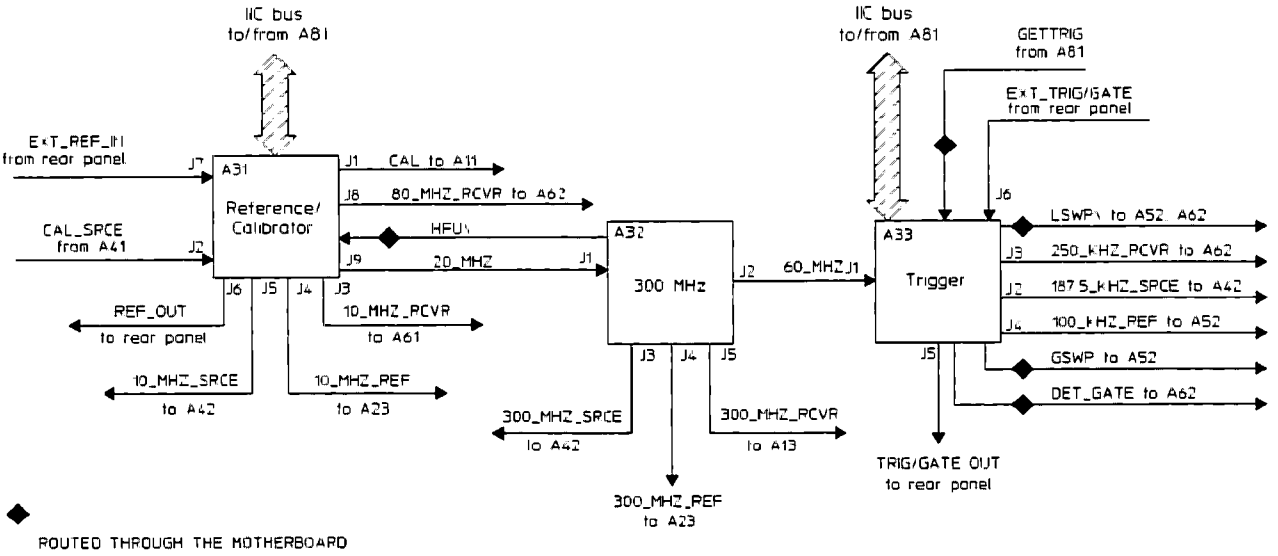


Figure 12-9. Frequency Reference Block Diagram

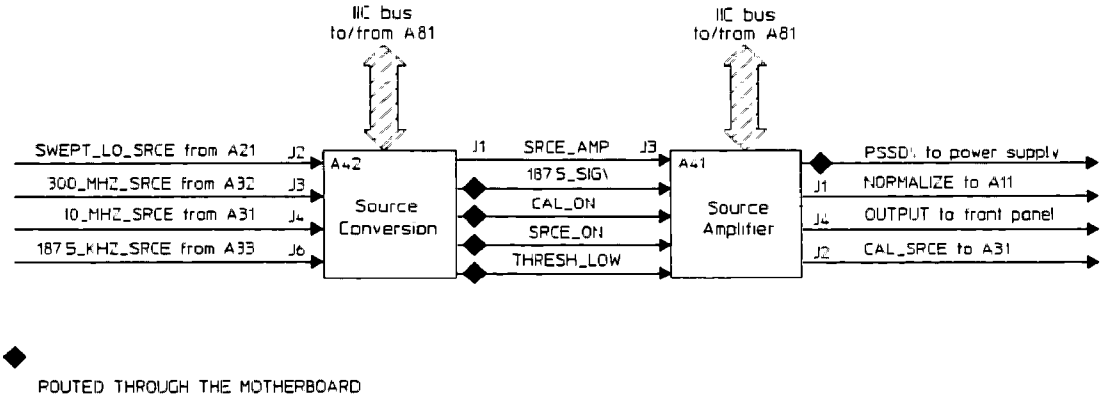


Figure 12-10. Source Block Diagram

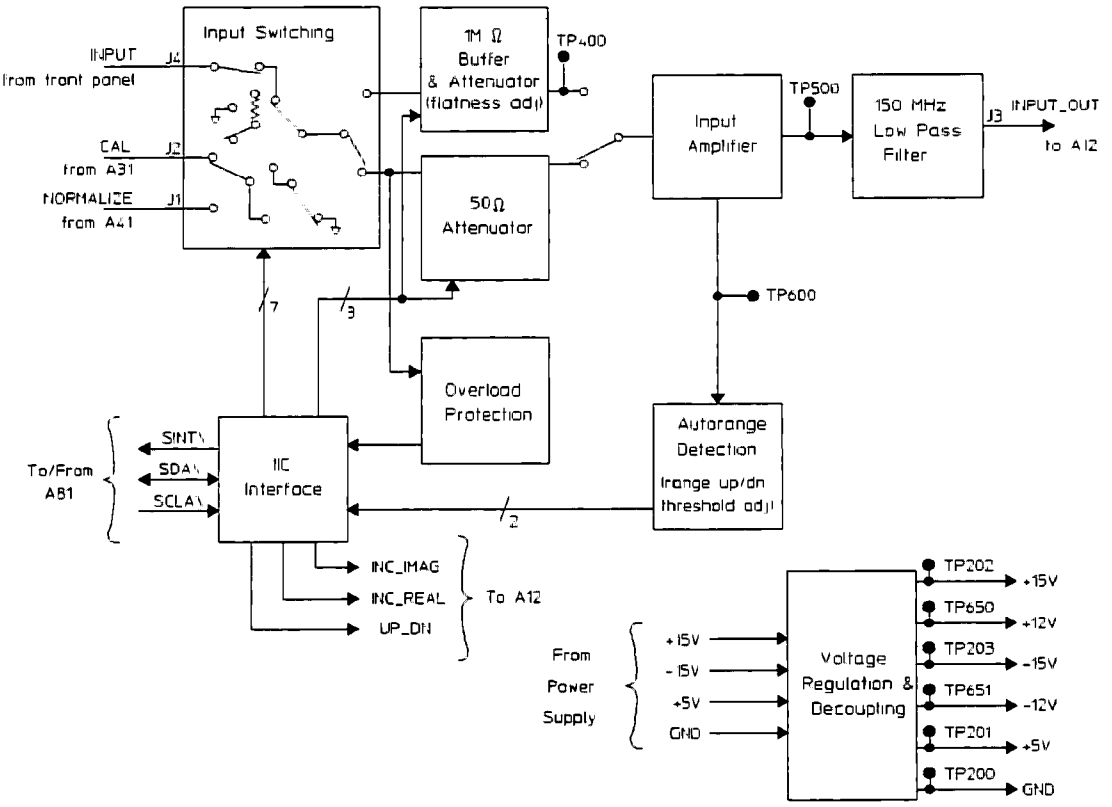


Figure 12-11. A11 Input Block Diagram

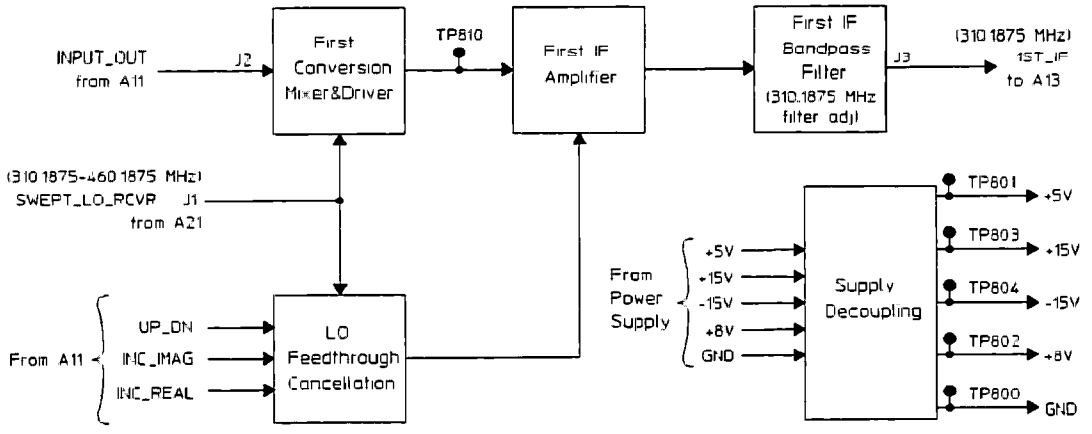


Figure 12-12. A12 First Conversion Block Diagram

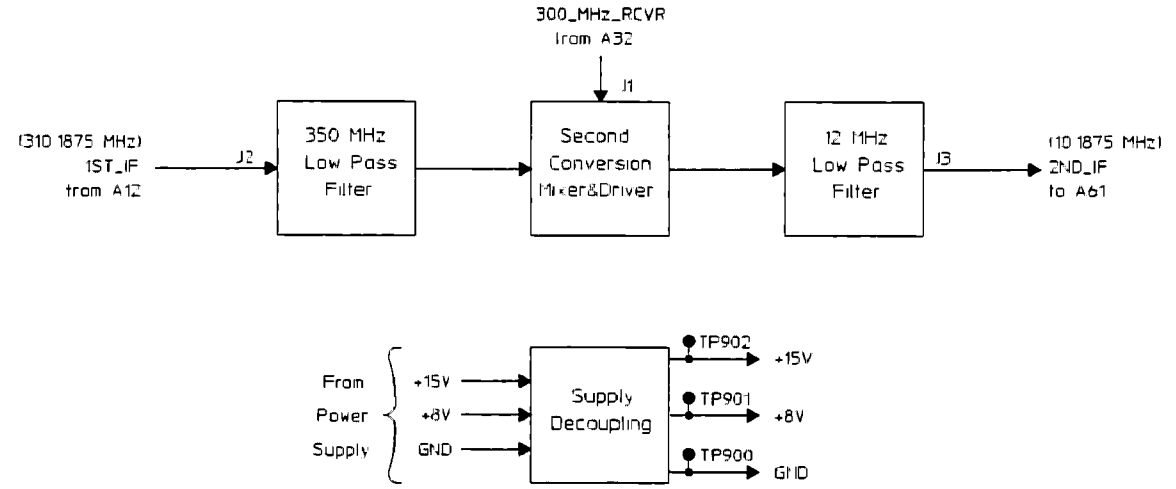


Figure 12-13. A13 Second Conversion Block Diagram

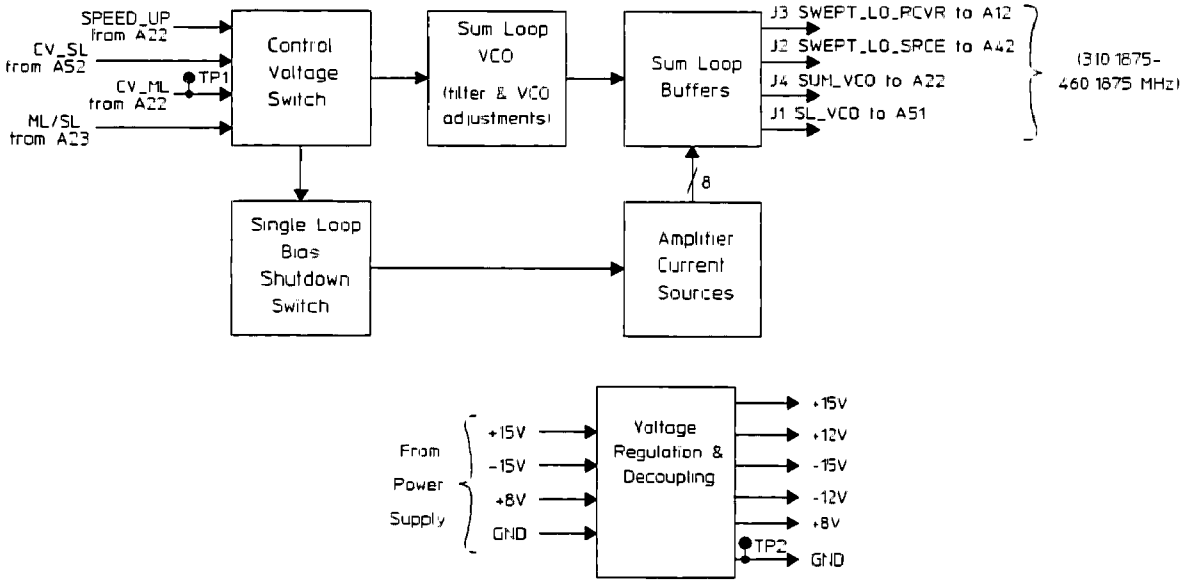


Figure 12-14. A21 Sum VCO Block Diagram

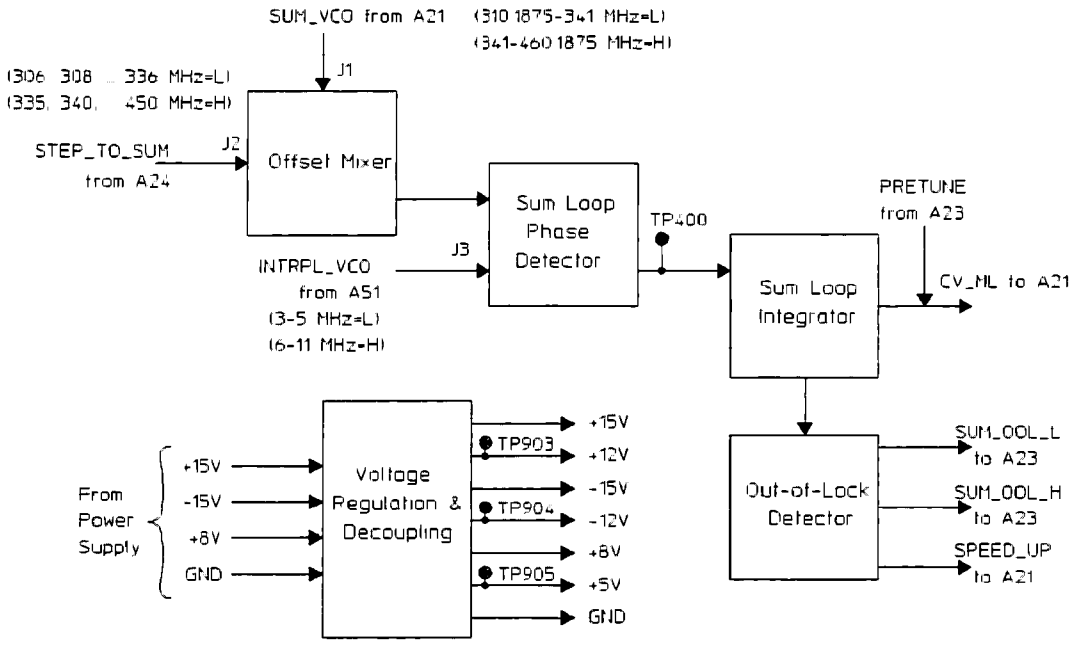


Figure 12-15. A22 Sum Phase Detector Block Diagram

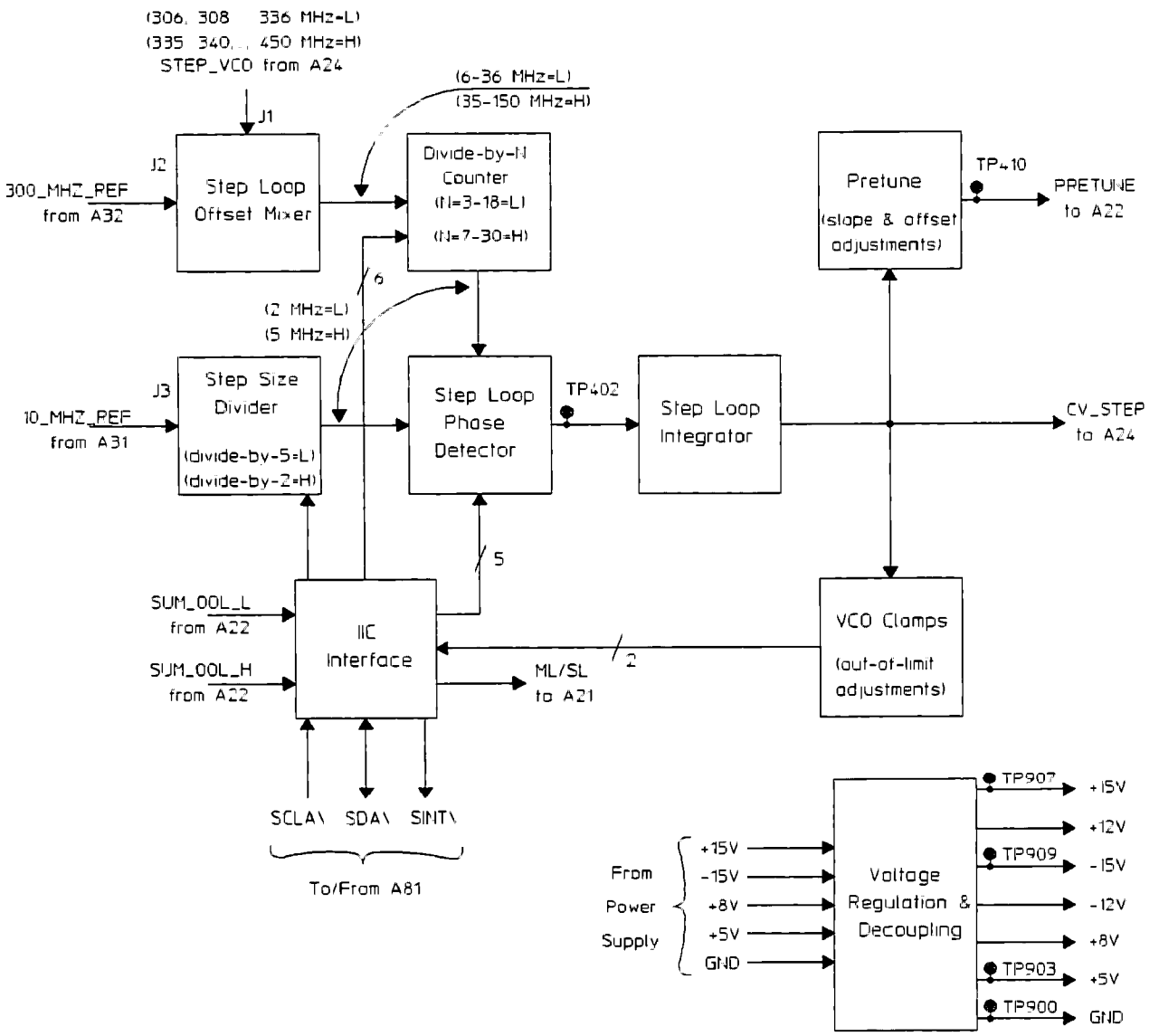


Figure 12-16. A23 Step Phase Detector

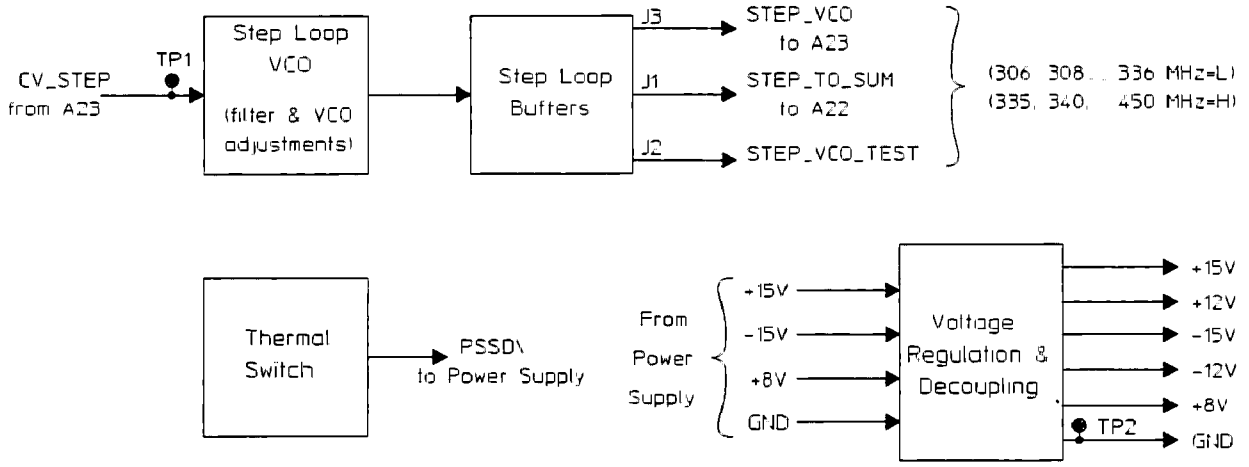


Figure 12-17. A24 Step VCO Block Diagram

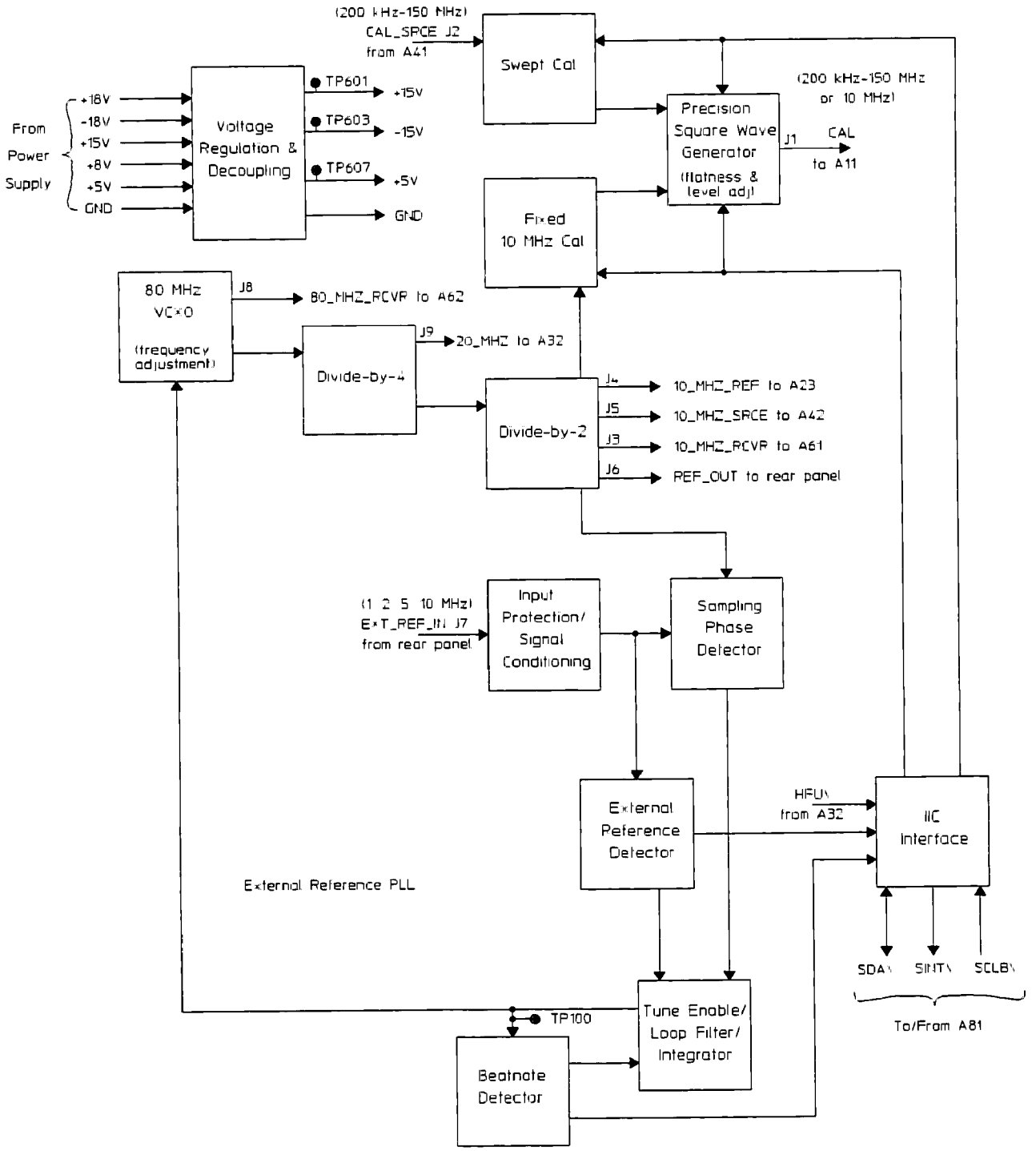


Figure 12-18. A31 Reference/Calibrator Block Diagram

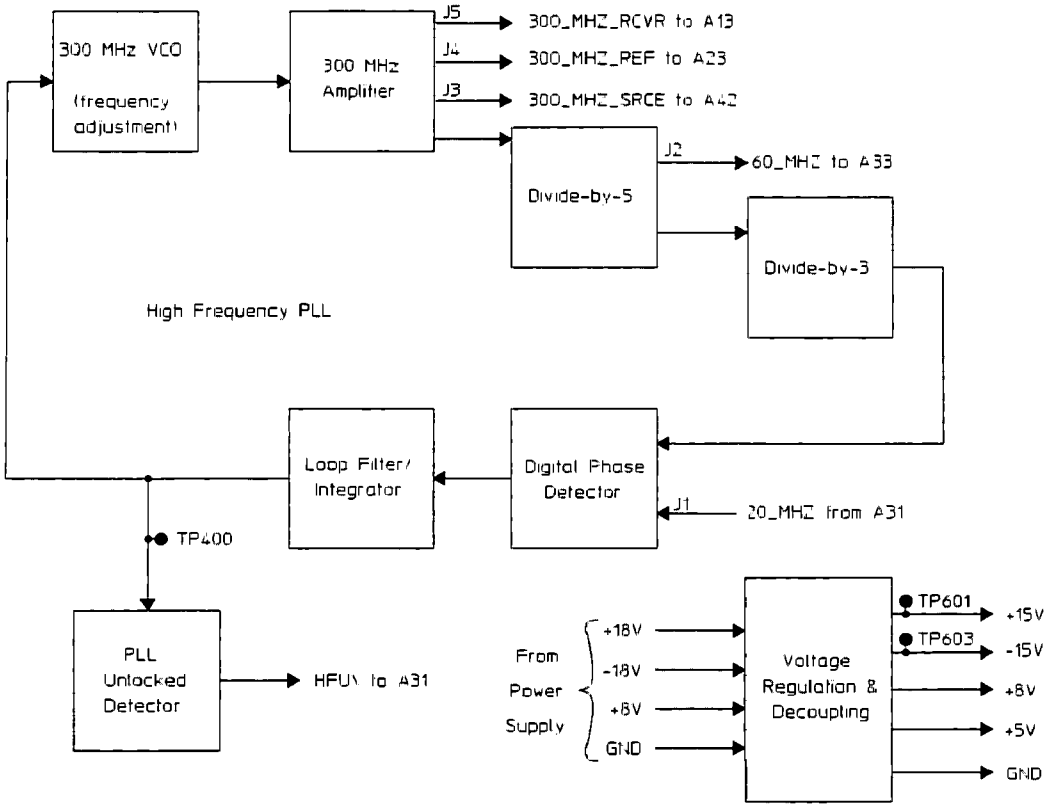


Figure 12-19. A32 300 MHz Block Diagram

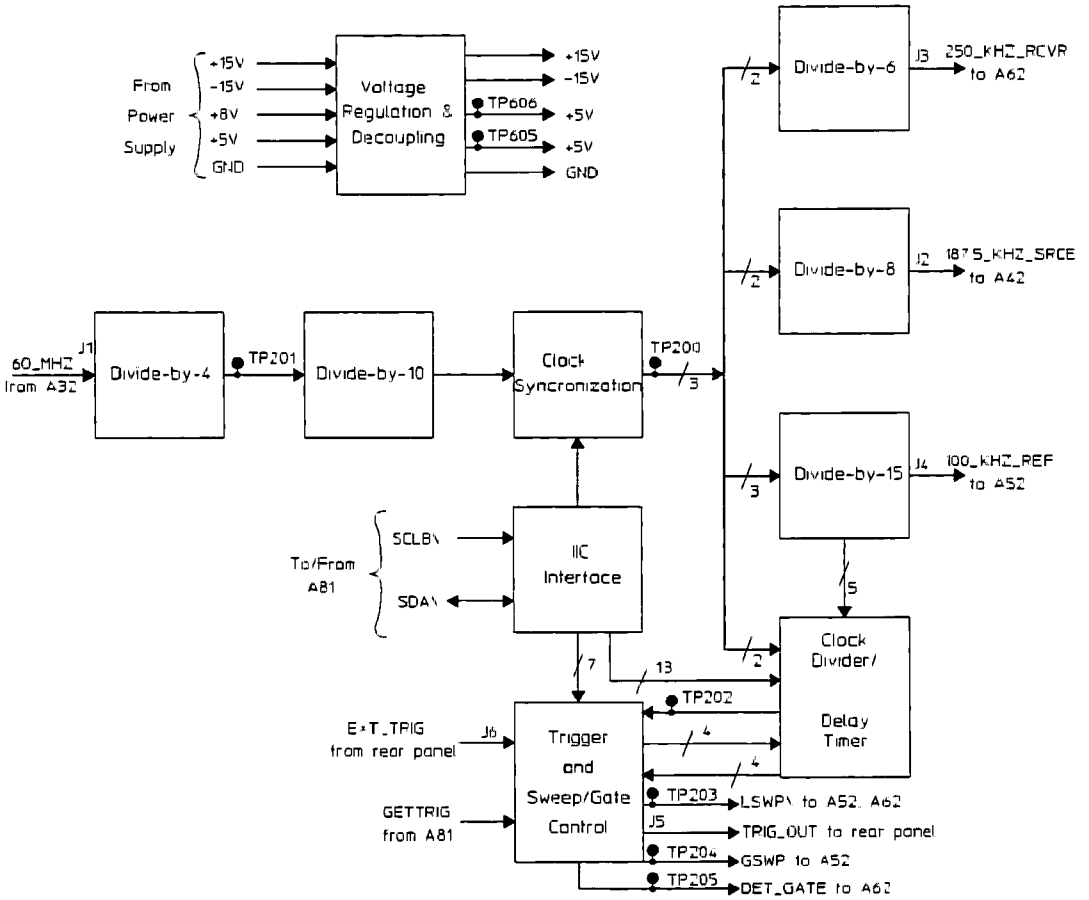


Figure 12-20. A33 Trigger Block Diagram

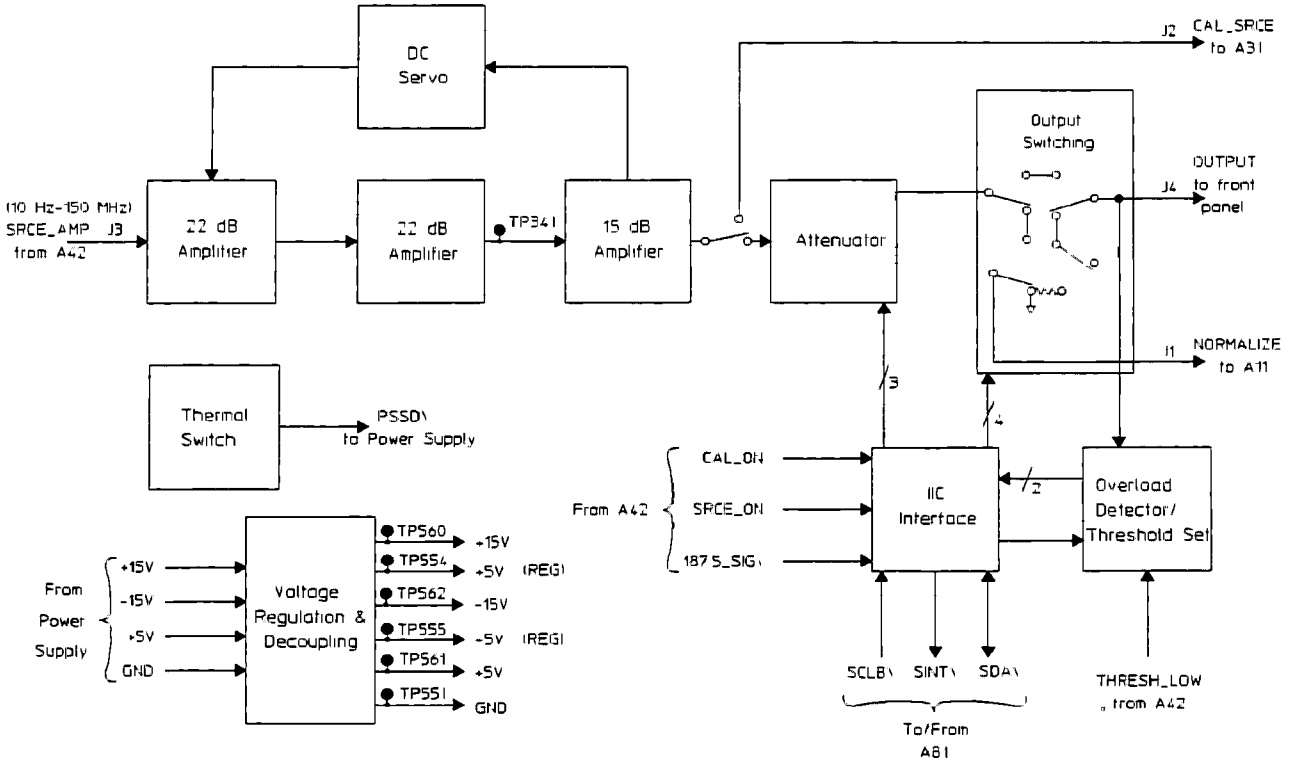


Figure 12-21. A41 Source Amplifier Block Diagram

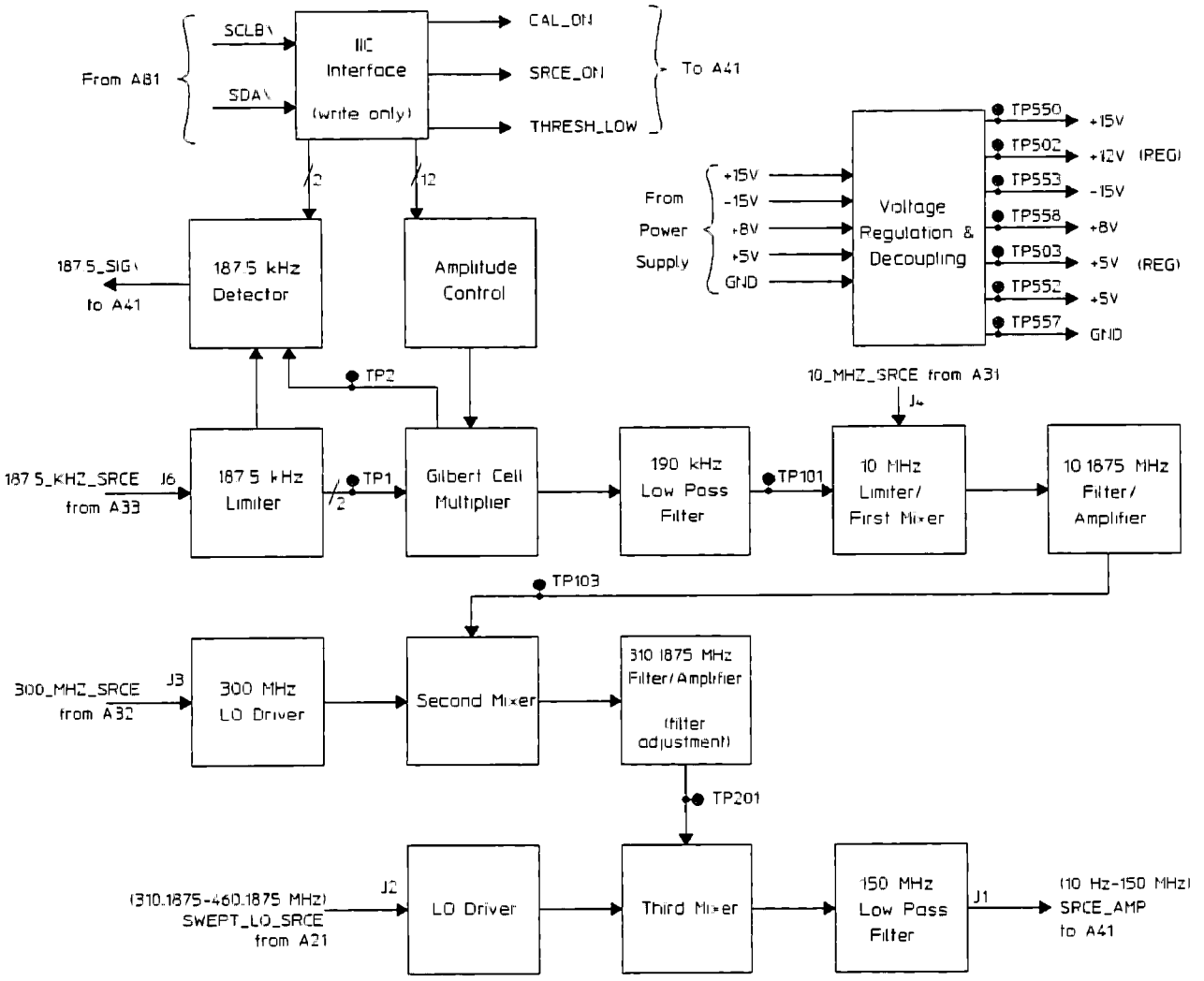


Figure 12-22. A42 Source Conversion Block Diagram

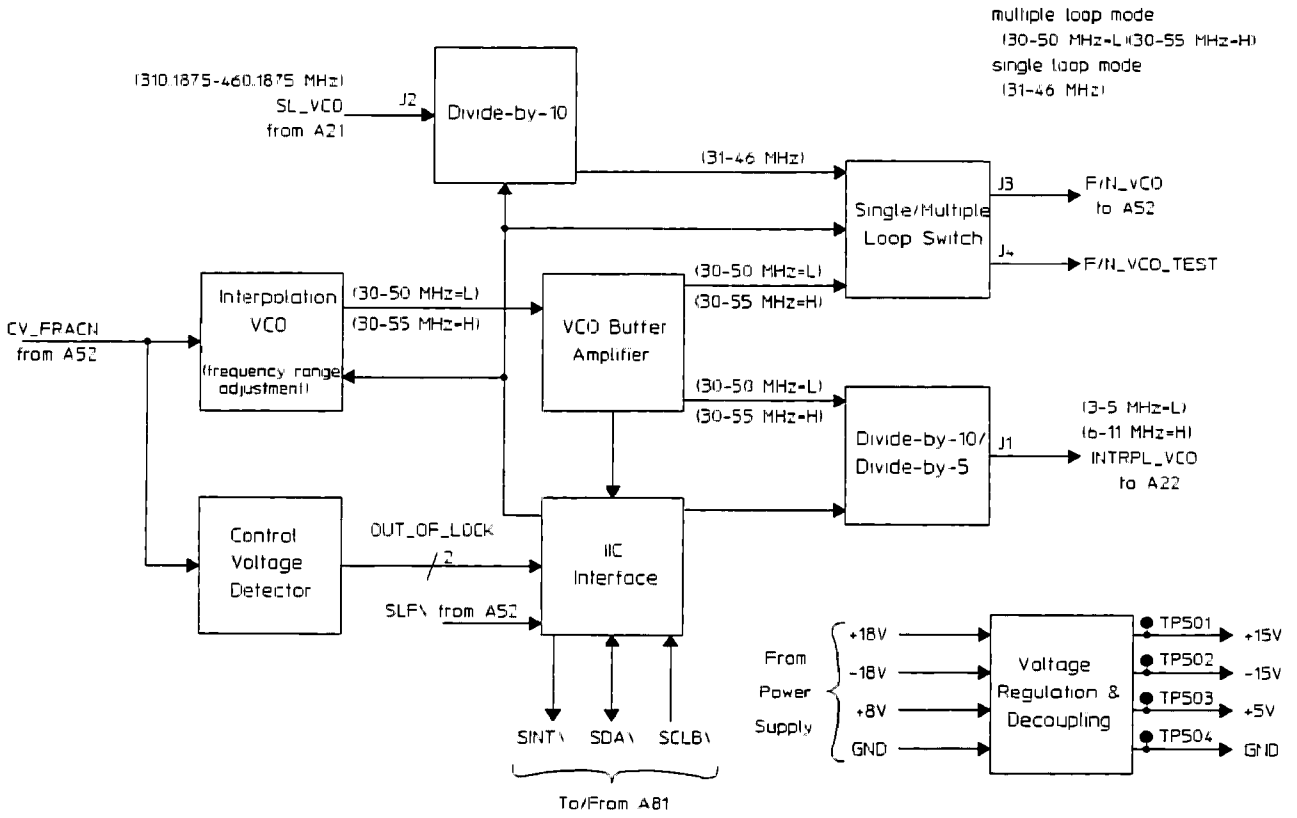


Figure 12-23. A51 Interpolation VCO Block Diagram

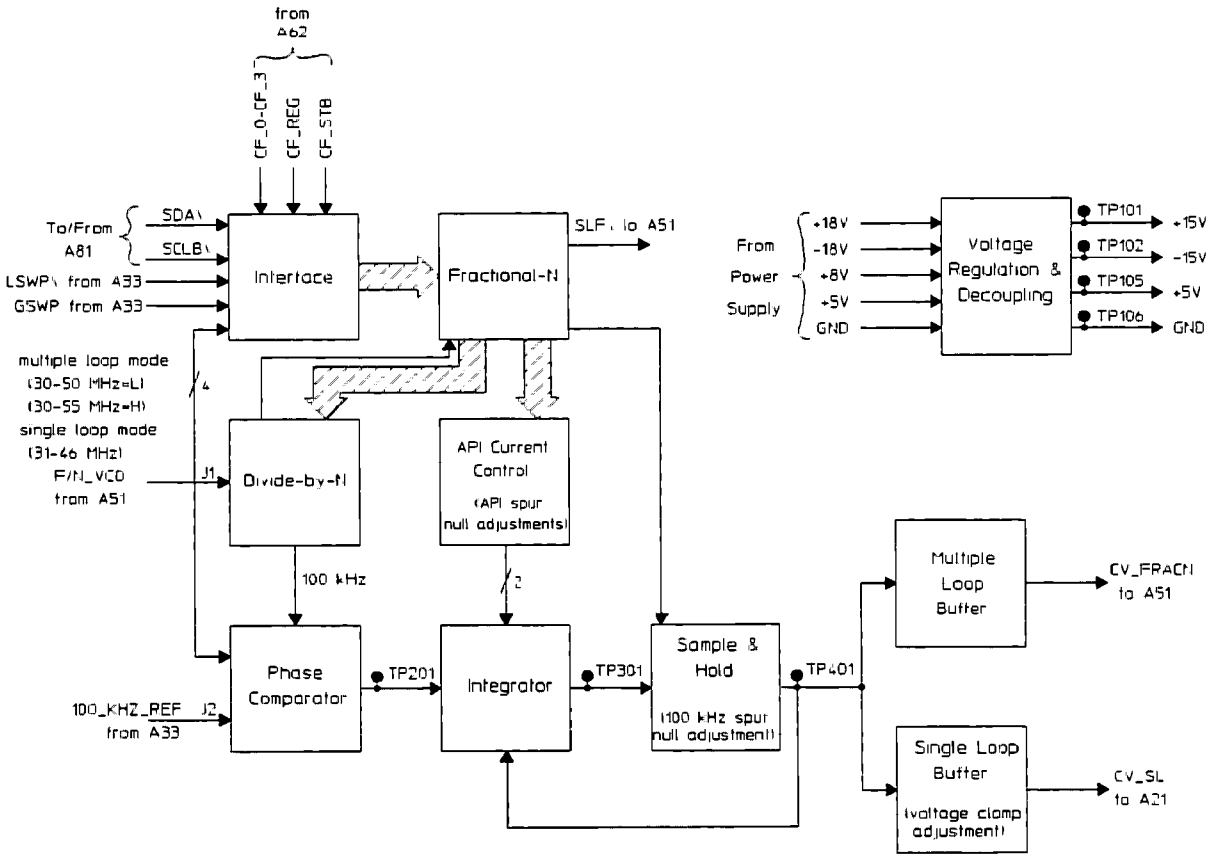


Figure 12-24. A52 Fractional-N Block Diagram

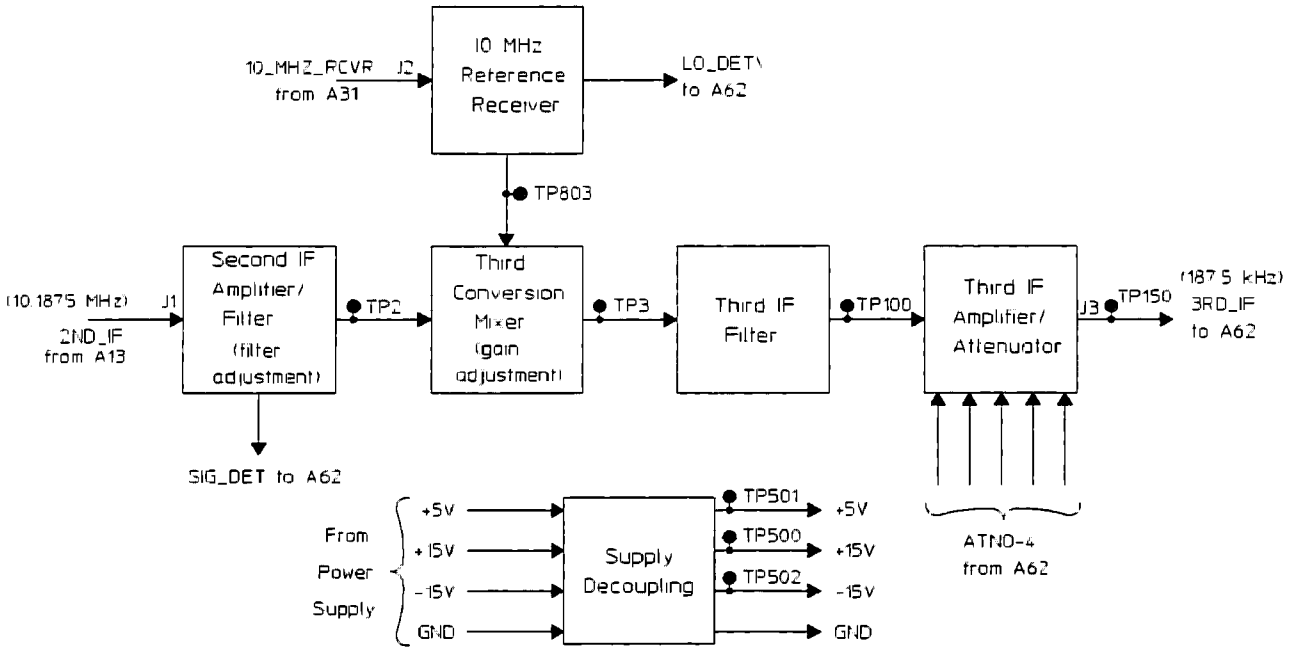


Figure 12-25. A61 IF Block Diagram

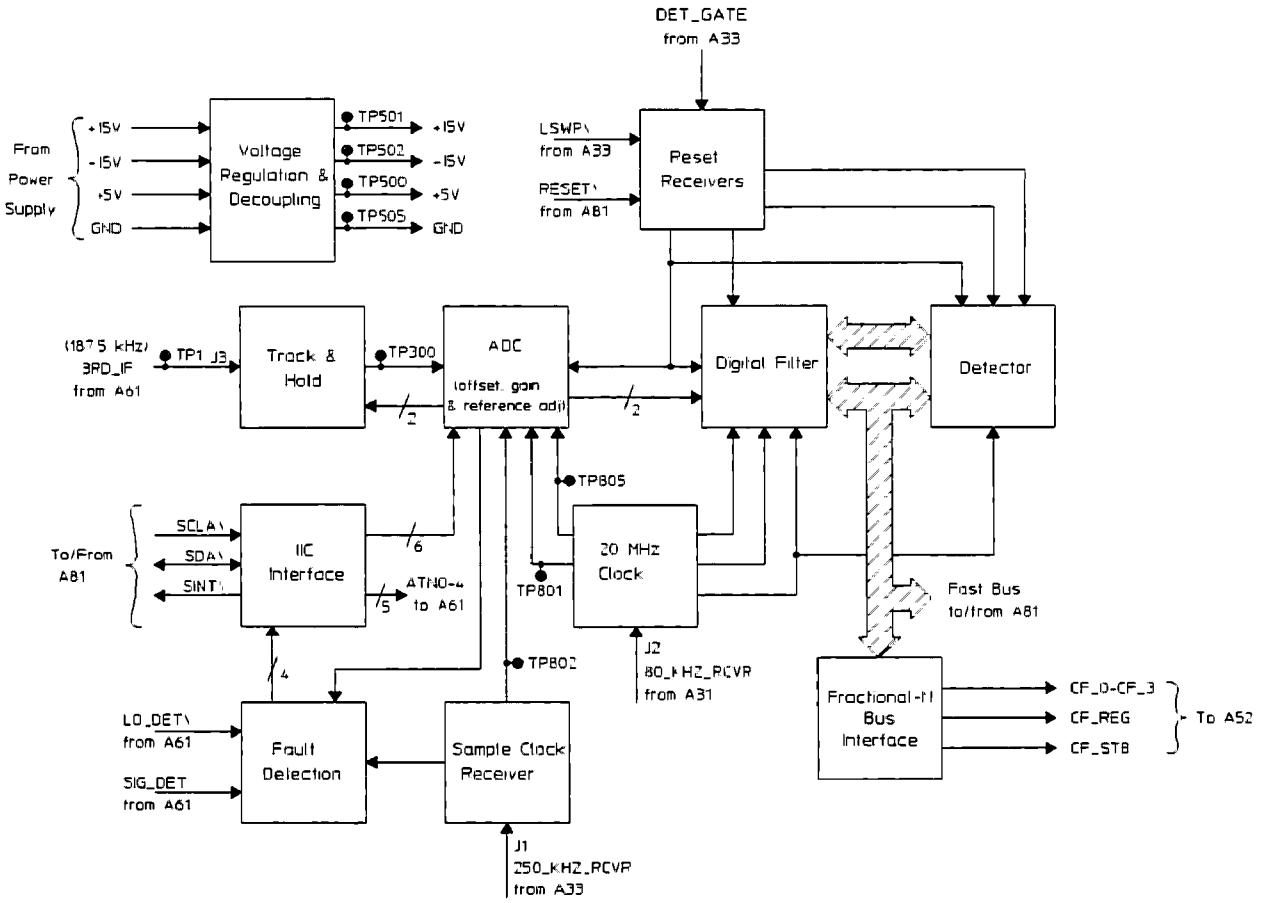


Figure 12-26. A62 ADC/Digital Filter Block Diagram

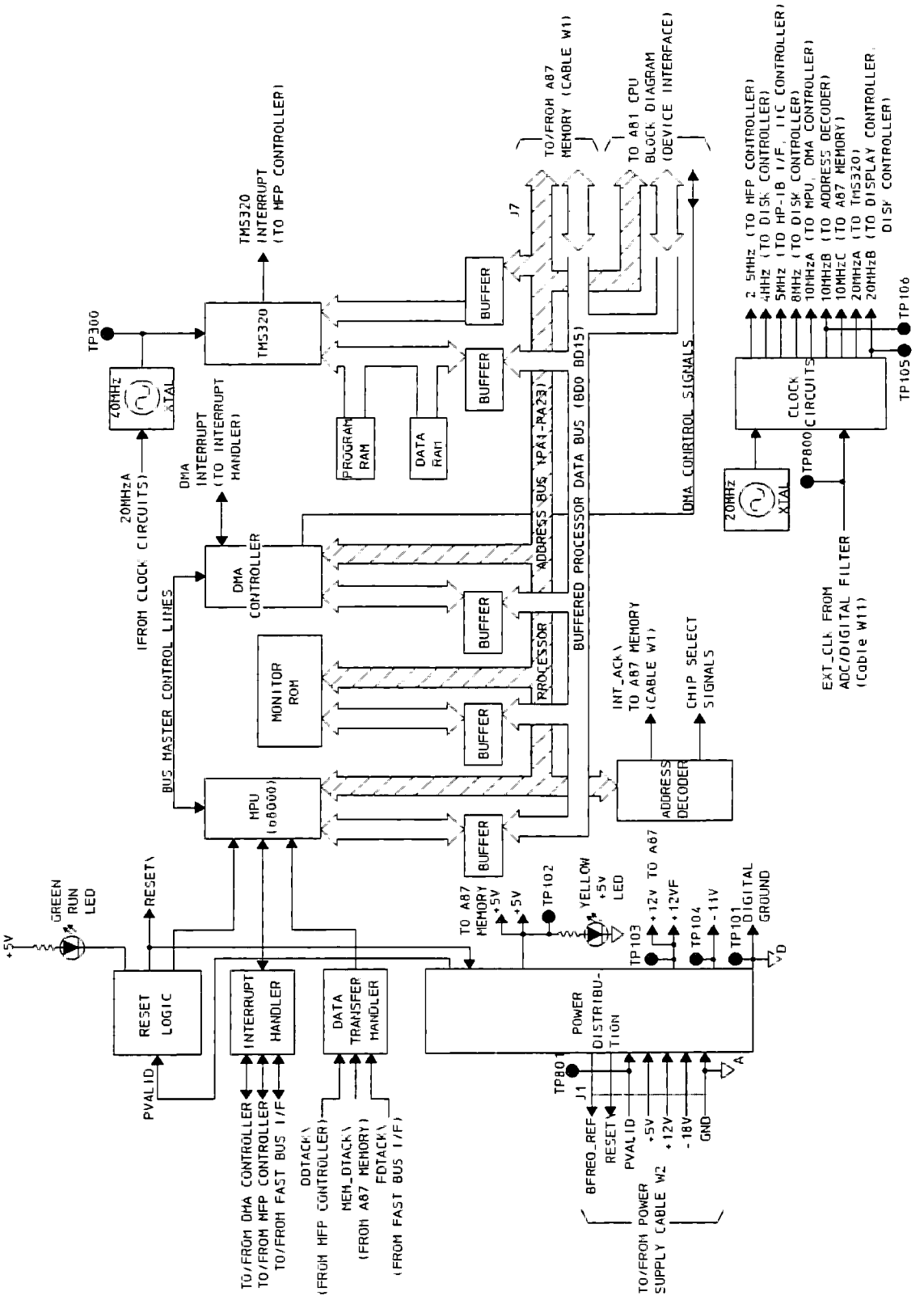


Figure 12-27. A81 CPU Block Diagram

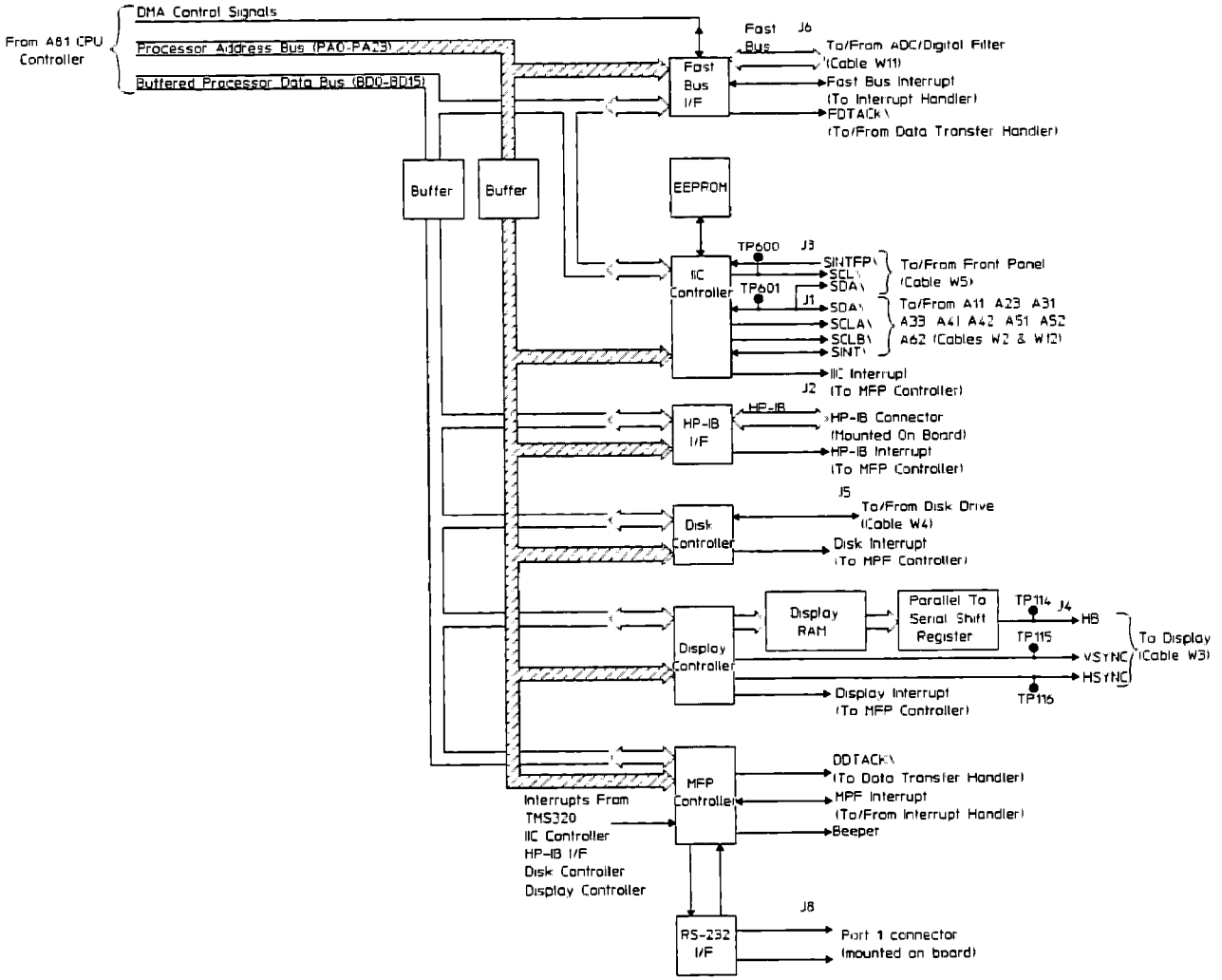


Figure 12-28. A81 CPU Interface Block Diagram

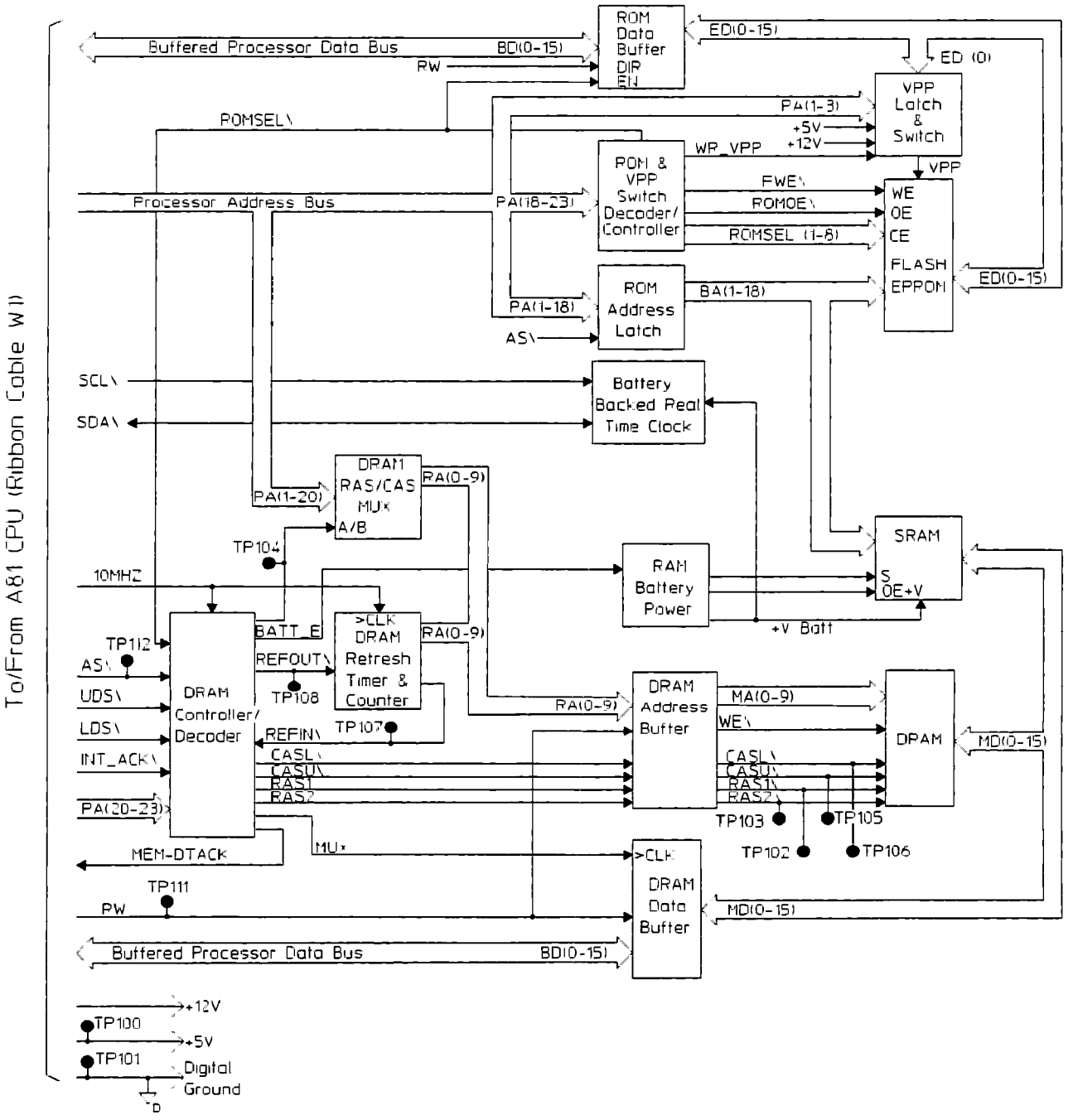


Figure 12-29. Memory and Expanded Memory Block Diagram

Table 12-1. Multiple Loop Mode Frequency Matrix

Measurement Freq		Sum VCO		Step VCO		F/N VCO		Intrpl VCO	
Start ≥ (MHz)	Stop < (MHz)	Start (MHz)	Stop (MHz)	Freq (MHz)	Divide By N	Start (MHz)	Stop (MHz)	Start (MHz)	Stop (MHz)
0.0	0.8125	310.1875	311.0	306	3	41.875	50.0	4.1875	5.0
0.8125	2.8125	311.0	313.0	308	4	30.0	50.0	3.0	5.0
2.8125	4.8125	313.0	315.0	310	5	30.0	50.0	3.0	5.0
4.8125	6.8125	315.0	317.0	312	6	30.0	50.0	3.0	5.0
6.8125	8.8125	317.0	319.0	314	7	30.0	50.0	3.0	5.0
8.8125	10.8125	319.0	321.0	316	8	30.0	50.0	3.0	5.0
10.8125	12.8125	321.0	323.0	318	9	30.0	50.0	3.0	5.0
12.8125	14.8125	323.0	325.0	320	10	30.0	50.0	3.0	5.0
14.8125	16.8125	325.0	327.0	322	11	30.0	50.0	3.0	5.0
16.8125	18.8125	327.0	329.0	324	12	30.0	50.0	3.0	5.0
18.8125	20.8125	329.0	331.0	326	13	30.0	50.0	3.0	5.0
20.8125	22.8125	331.0	333.0	328	14	30.0	50.0	3.0	5.0
22.8125	24.8125	333.0	335.0	330	15	30.0	50.0	3.0	5.0
24.8125	26.8125	335.0	337.0	332	16	30.0	50.0	3.0	5.0
26.8125	28.8125	337.0	339.0	334	17	30.0	50.0	3.0	5.0
28.8125	30.8125	339.0	341.0	336	18	30.0	50.0	3.0	5.0
30.8125	35.8125	341.0	346.0	335	7	30.0	55.0	6.0	11.0
35.8125	40.8125	346.0	351.0	340	8	30.0	55.0	6.0	11.0
40.8125	45.8125	351.0	356.0	345	9	30.0	55.0	6.0	11.0
45.8125	50.8125	356.0	361.0	350	10	30.0	55.0	6.0	11.0
50.8125	55.8125	361.0	366.0	355	11	30.0	55.0	6.0	11.0
55.8125	60.8125	366.0	371.0	360	12	30.0	55.0	6.0	11.0
60.8125	65.8125	371.0	376.0	365	13	30.0	55.0	6.0	11.0
65.8125	70.8125	376.0	381.0	370	14	30.0	55.0	6.0	11.0
70.8125	75.8125	381.0	386.0	375	15	30.0	55.0	6.0	11.0
75.8125	80.8125	386.0	391.0	380	16	30.0	55.0	6.0	11.0
80.8125	85.8125	391.0	396.0	385	17	30.0	55.0	6.0	11.0
85.8125	90.8125	396.0	401.0	390	18	30.0	55.0	6.0	11.0
90.8125	95.8125	401.0	406.0	395	19	30.0	55.0	6.0	11.0
95.8125	100.8125	406.0	411.0	400	20	30.0	55.0	6.0	11.0
100.8125	105.8125	411.0	416.0	405	21	30.0	55.0	6.0	11.0
105.8125	110.8125	416.0	421.0	410	22	30.0	55.0	6.0	11.0
110.8125	115.8125	421.0	426.0	415	23	30.0	55.0	6.0	11.0
115.8125	120.8125	426.0	431.0	420	24	30.0	55.0	6.0	11.0
120.8125	125.8125	431.0	436.0	425	25	30.0	55.0	6.0	11.0
125.8125	130.8125	436.0	441.0	430	26	30.0	55.0	6.0	11.0
130.8125	135.8125	441.0	446.0	435	27	30.0	55.0	6.0	11.0
135.8125	140.8125	446.0	451.0	440	28	30.0	55.0	6.0	11.0
140.8125	145.8125	451.0	456.0	445	29	30.0	55.0	6.0	11.0
145.8125	150.0	456.0	460.1875	450	30	30.0	50.9375	6.0	10.1875

Table 12-2. Motherboard Voltages

Voltage	Assembly Using Voltage																		
	PWR	A11	A12	A13	A21	A22	A23	A24	A31	A32	A33	A41	A42	A51	A52	A61	A62	A90/91	P PWR
	Motherboard Connector																		
	J5	J11	J12	J13	J21	J22	J23	J24	J31	J32	J33	J41	J42	J51	J52	J61	J62	W1	W2
	Connector Pin Number or Wire Color																		
+18V	18								1	1				7A	7A			Red	
														7B	7B				
														7C	7C				
+15V	9	4A	1	1	1	1	4A	1	3		1	4A	4A			4A	4A		Red
	10	4B					4B					4B	4B			4B	4B		
		4C					4C					4C	4C			4C	4C		
+8V	2-6		5	5	5	5	10A	5	5	5	5		10A	10A	10A				
			6	6	6	6	10B	6	6	6	6		10B	10B	10B				
							10C						10C	10C	10C				
+5V	31-	12A	10				12A		10	10	10	12A	12A		12A	12A	12A		
	36	12B					12B					12B	12B		12B	12B	12B		
		12C					12C					12C	12C		12C	12C	12C		
−15V	22	5A	2		2	2	5A	2			2	5A	5A			5A	5A		Yel†
	24	5B					5B					5B	5B			5B	5B		
		5C					5C					5C	5C			5C	5C		
−18V	28								2	2				8A	8A			Yel	
														8B	8B				
														8C	8C				
Gnd	7-8	6A	4	4	4	4	3A	4	4	4	4	6A	6A	1A	6A	6A	6A	Blk	Blk
	11-	6B	7	7	9		3B	7	7	7	7	6B	6B	1C	6B	6B	6B		
	13	6C	9	9			3C	9				6C	6C	2A	6C	6C	6C		
	15-	9A					6A	12				9A	9A	2B	9A	9A	9A		
	17	9B					6B					9B	9B	2C	9B	9B	9B		
	19-	9C					6C					9C	9C	3A	9C	9C	9C		
	21	11A					9A					11A	11A	3C	11A	11A	11A		
	23	11B					9B					11B	11B	6A	11B	11B	11B		
	25-	11C					9C					11C	11C	6B	11C	11C	11C		
	27	13A					11A					13A	13A	6C	13A	13A	13A		
	29	13B					11B					13B	13B	9A	13B	13B	13B		
	30	13C					11C					13C	13C	9B	13C	13C	13C		
	37-						13A							9C	14A				
	39						13B							11A	14C				
	41						13C							11B	15A				
	43													11C	15B				
	45													13A	15C				
	47													13B	16C				
	49													13C					

HP 35689A/B S-Parameter Test Set

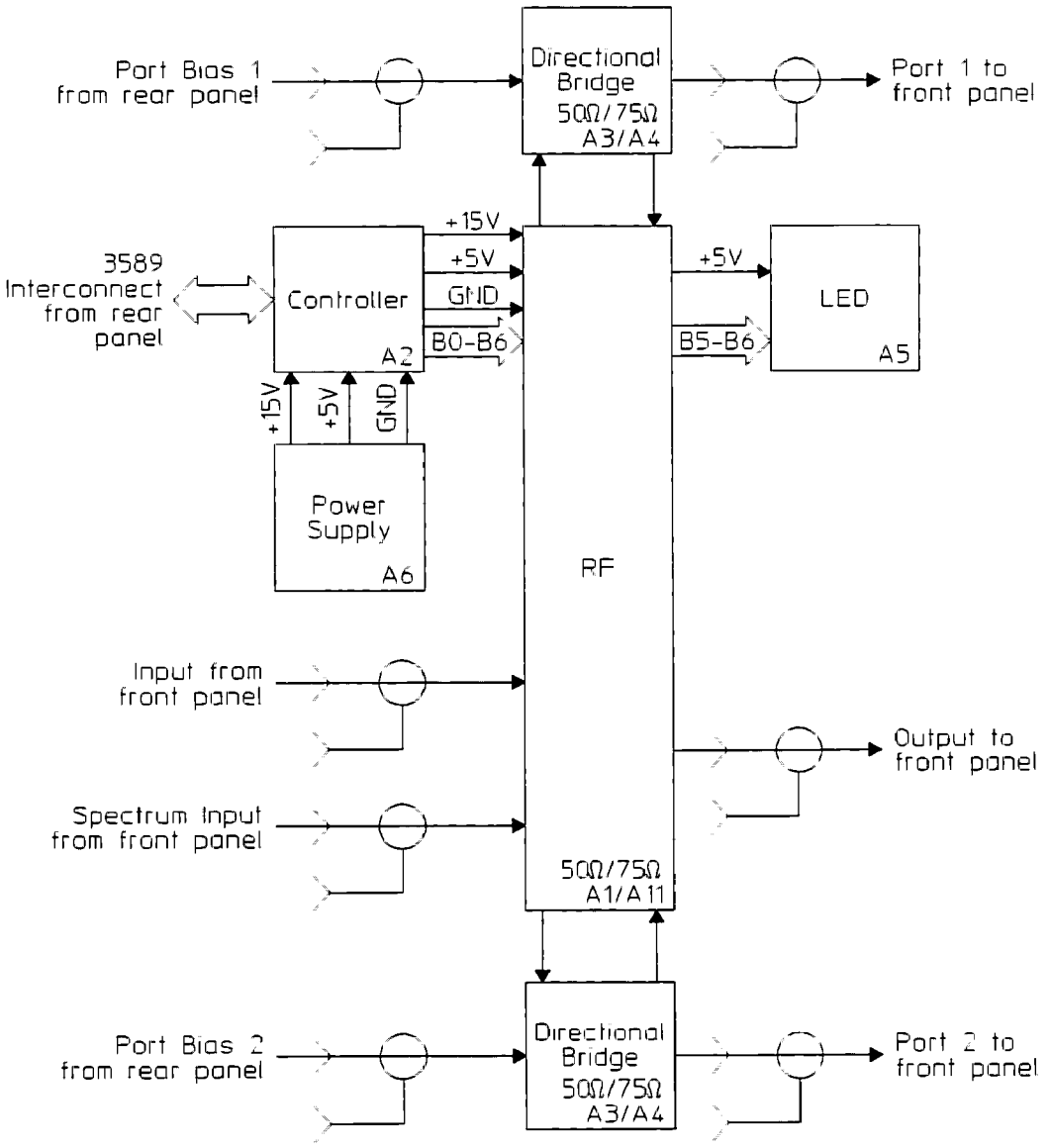


Figure 12-30. HP 35689A/B Overall Block Diagram

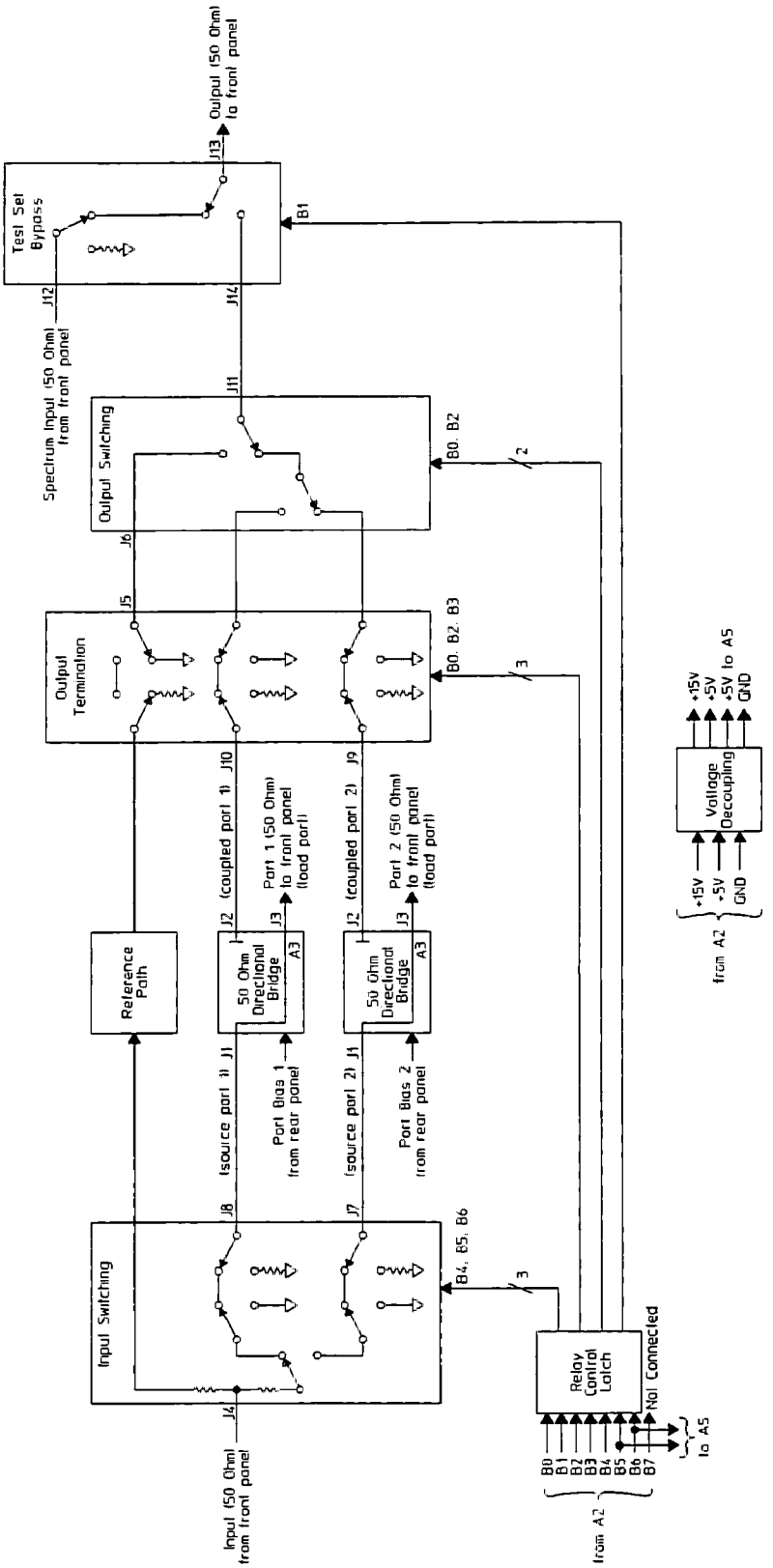


Figure 12-31. A1 50 Ohm RF Block Diagram

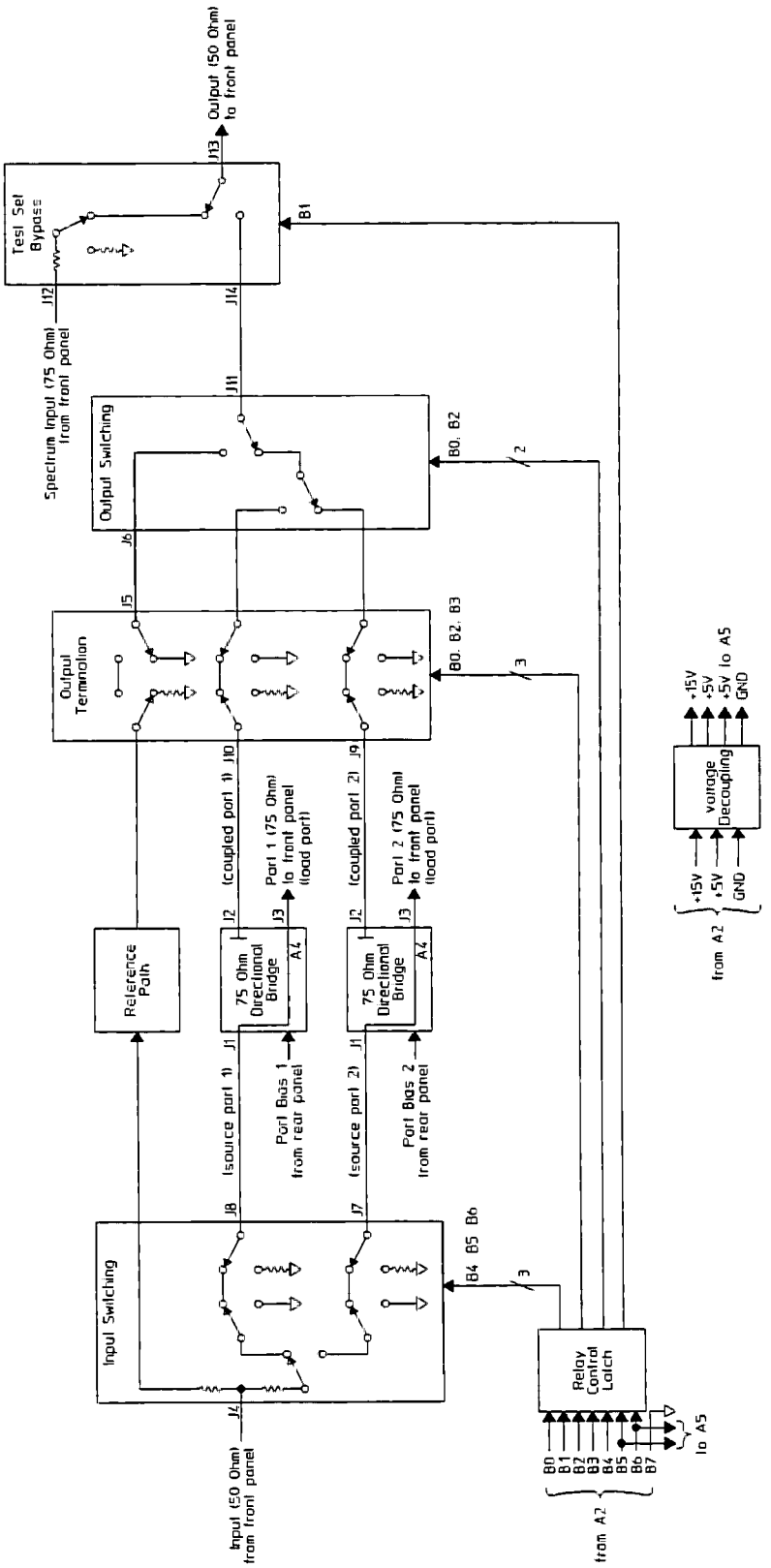


Figure 12-32. A11 75 Ohm RF Block Diagram

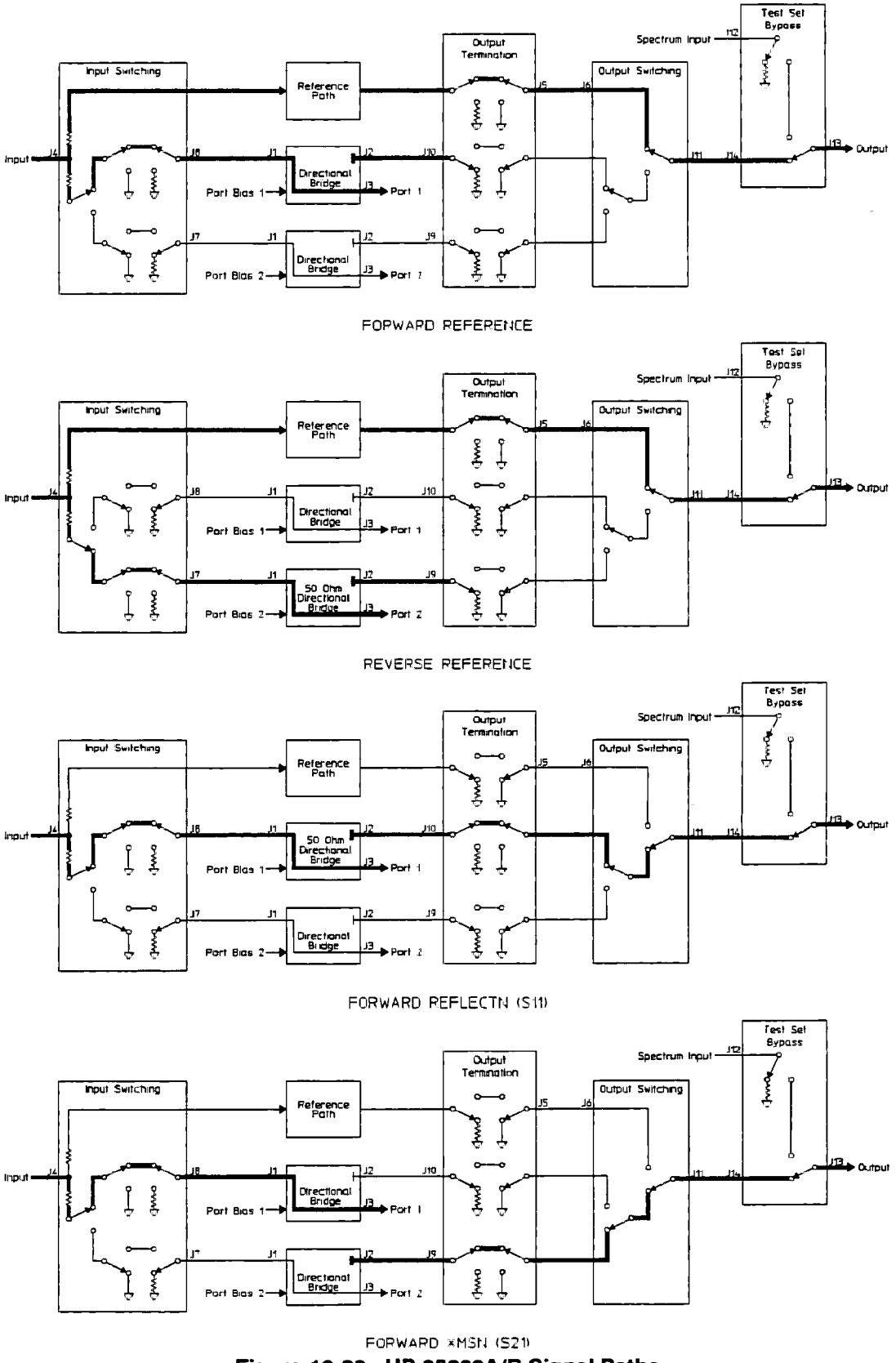
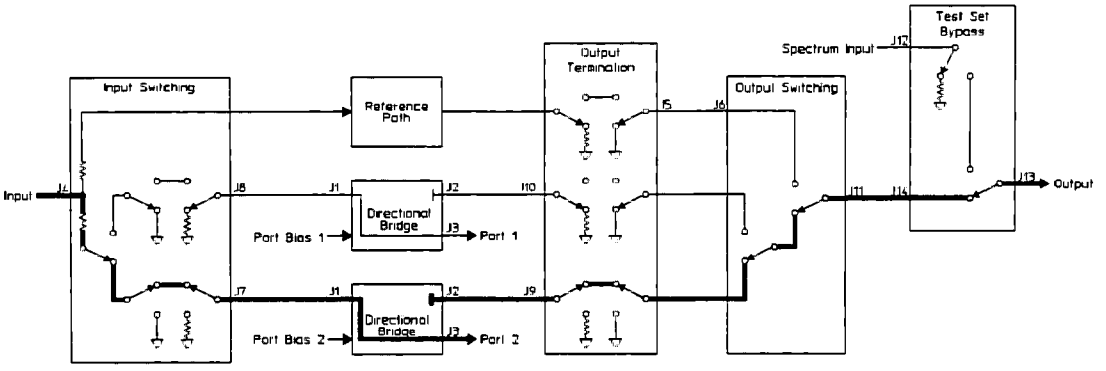
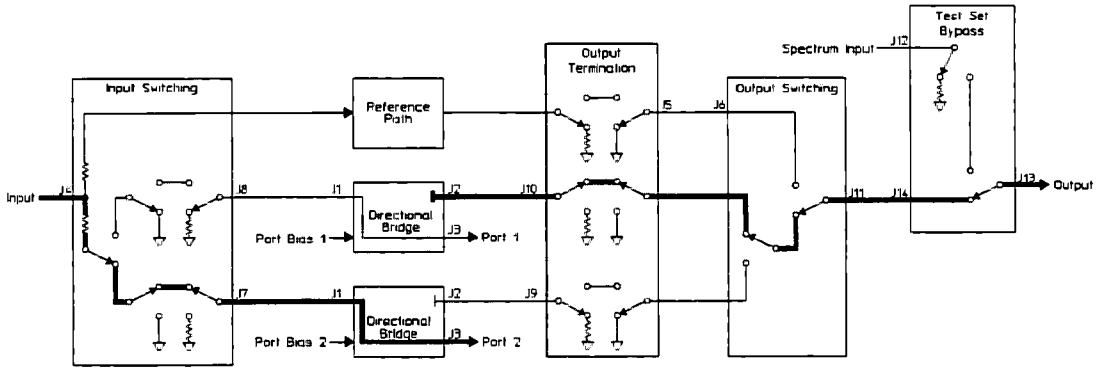


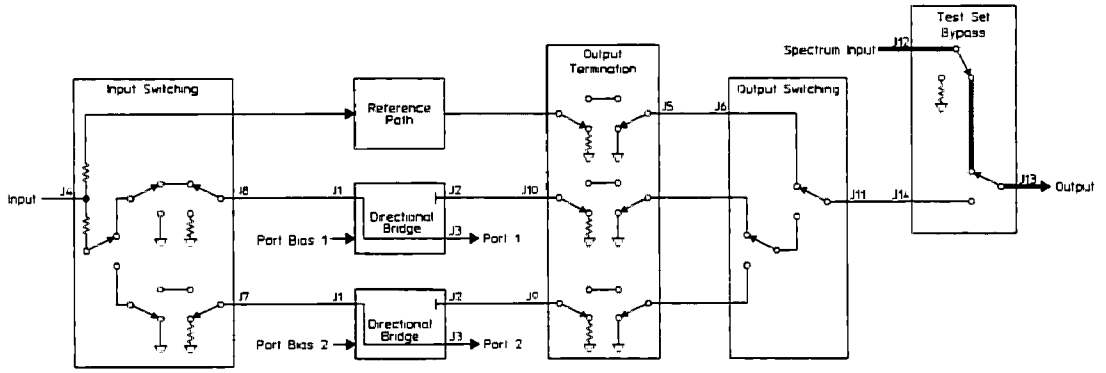
Figure 12-33. HP 35689A/B Signal Paths



REVERSE REFLECTN (S22)



REVERSE TRSN (S12)



SPECTRUM PORT

Figure 12-33. HP 35689A/B Signal Paths (cont)

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About this edition

February 1995: In this edition, Chapter 1 "Options" was changed to include option 1D7 50/75 ohm minimum loss pad. In Table 1-3, "Available Accessories", part number HP 11852B #C04 was changed to HP 11852B #004. In Chapter 3, Table 3-5, Measurement Uncertainty (50 ohm), some corrections were made between 300Khz and 40Mhz. There were some miscellaneous changes to Chapter 5. Chapter 7 had some corrections to Figure 7-2 and Figure 7-8. Table 7-3 had a part number correction and Table 7-4 had a part number added.

October 1991: Previous edition.