Keysight Technologies
Capture Highest DDR3/4 and LPDDR3/4 Data Rates Using Advanced Probe Settings on Logic Analyzers

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Purpose of Advanced Probe Settings Mode

Keysight Technologies, Inc. logic analyzer module inputs are optimized to provide a flat input bandwidth from DC to the specified limit when used with Keysight probes designed with specific tip resistor capacitor networks.

Occasionally, probing techniques involve additional tip isolation resistors to interface to the system under test. System interfaces using additional tip isolation resistors, such as DDR BGA (Ball Grid Array) interposers, can provide additional high-frequency attenuation on the sampled signals to the logic analyzer. This additional attenuation can result in smaller data valid windows observed on the logic analyzer at DDR/LPDDR data rates over 1333 Mb/s. To compensate for this additional attenuation, Keysight has included a mode referred to as APS (Advanced Probe Settings) that peaks the edges of the input signals to the logic analyzer. This peaking can improve the capture window of signals to the logic analyzer.

As an example: Evaluation has shown larger data valid windows to the logic analyzer when using the APS mode with DDR BGA interposers at speeds of DDR3-1333 Mb/s and higher. The eye openings presented to the user from the sample positions window are enlarged (compared to eye openings without APS enabled). Larger eye openings allow the user to set sample positions for State mode capture for data rates up to DDR3 2400 Mb/s [1].

Depending on probing methods, APS mode may apply for DDR3/4 or LPDDR3/4 data rates over 1333 Mb/s. Keysight recommends that DDR3 Eyefinder/Eyescan be run with APS mode enabled and disabled to determine the best setting for individual target systems.

Advantage of Advanced Probe Settings Mode

Advanced Probe Settings (APS) mode on Keysight logic analyzers enables significantly higher DDR3/4 and LPDDR3/4 data rate captures from BGA probing.

Example: Using W3633A (x4 and x8) or W3631A (x16) DDR3 BGA probes and with either the U4154A or 16962A logic analyzers, APS mode enables data rate captures up to the rates shown below.

DDR3 data rate with APS enabled

– U4154A: DDR3 2400 Mb/s [1]
– 16962A: DDR3 1600 Mb/s [1]

	Data rate with APS enabled	Without APS enabled
U4154A	2400 Mb/s [1]	1333 Mb/s [1]
16962A	1600 Mb/s [1]	1333 Mb/s [1]

1. Maximum data rates subject to signal integrity variations in the system under test.

Enabling APS Mode

APS mode is enabled in the Options menu and then applied to the input signals from the Buses/Signals menu.

Follow these steps:

1. To enable APS mode in your logic analyzer configuration, use the pulldown Edit button and select Options, as shown in Figure 1.

2. Check the "Enabled Advanced Probe Settings (APS) box, click OK on the Options window, as shown in Figure 1.
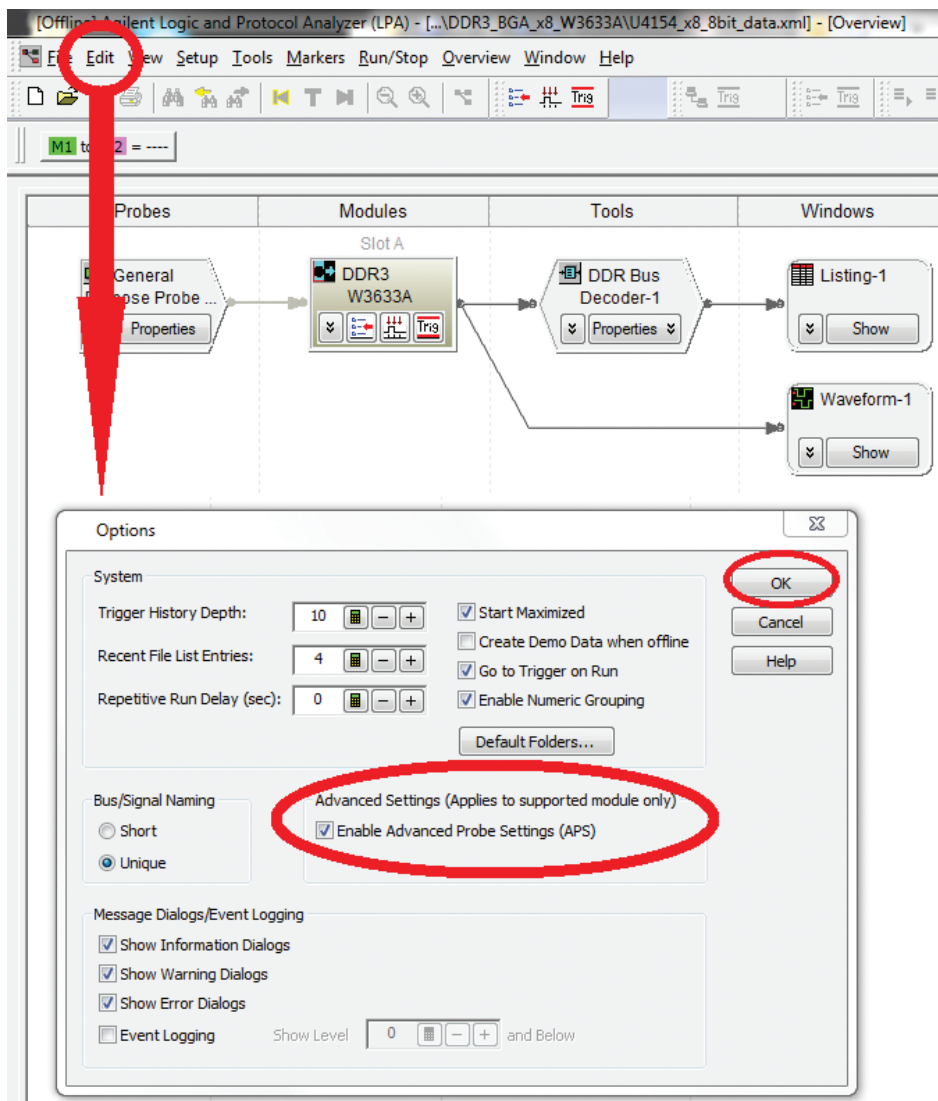

Figure 1. The Edit/Options window, with Enable Probe Settings (APS) selected

3. Click on the Buses/Signals icon to display to the Buses/Signals window, as shown in Figure 2.
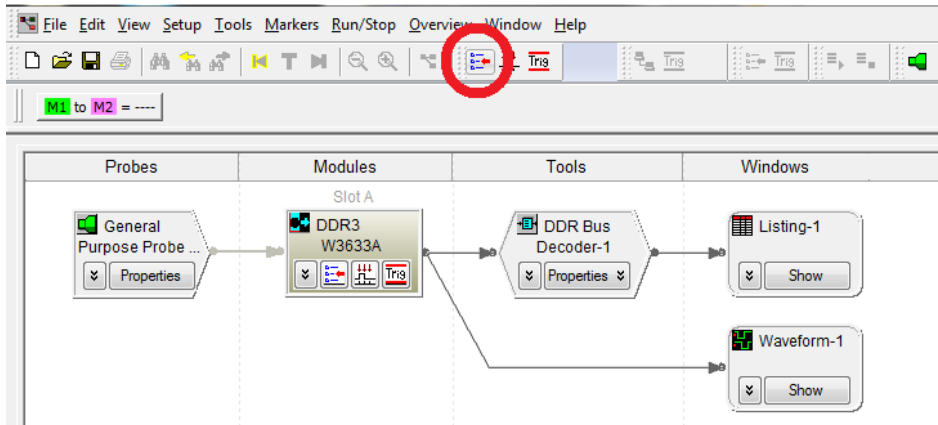

Figure 2. Buses/Signals icon

4. In the Buses/Signals window select APS, as shown in Figure 3. This will open up the Advanced Probe Settings window.
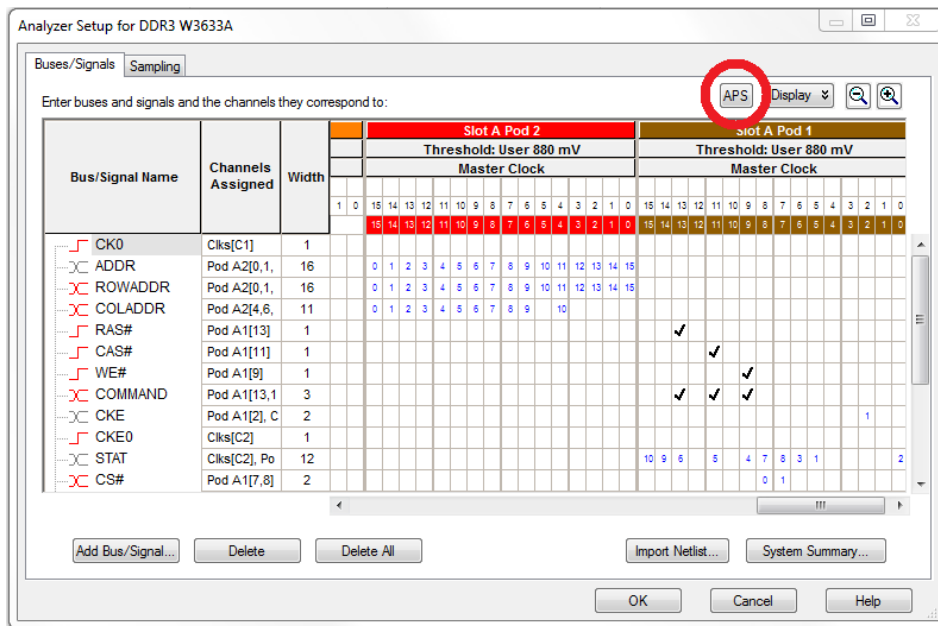

Figure 3. Buses and Signals window

5. As shown in Figure 4, in the Advanced Probe Settings window, select all modules in the configuration connected to probing that may benefit from enabling APS. Then select "OK".

    APS can be disabled from this window or from the Edit Options Window. It must be enabled in both windows.
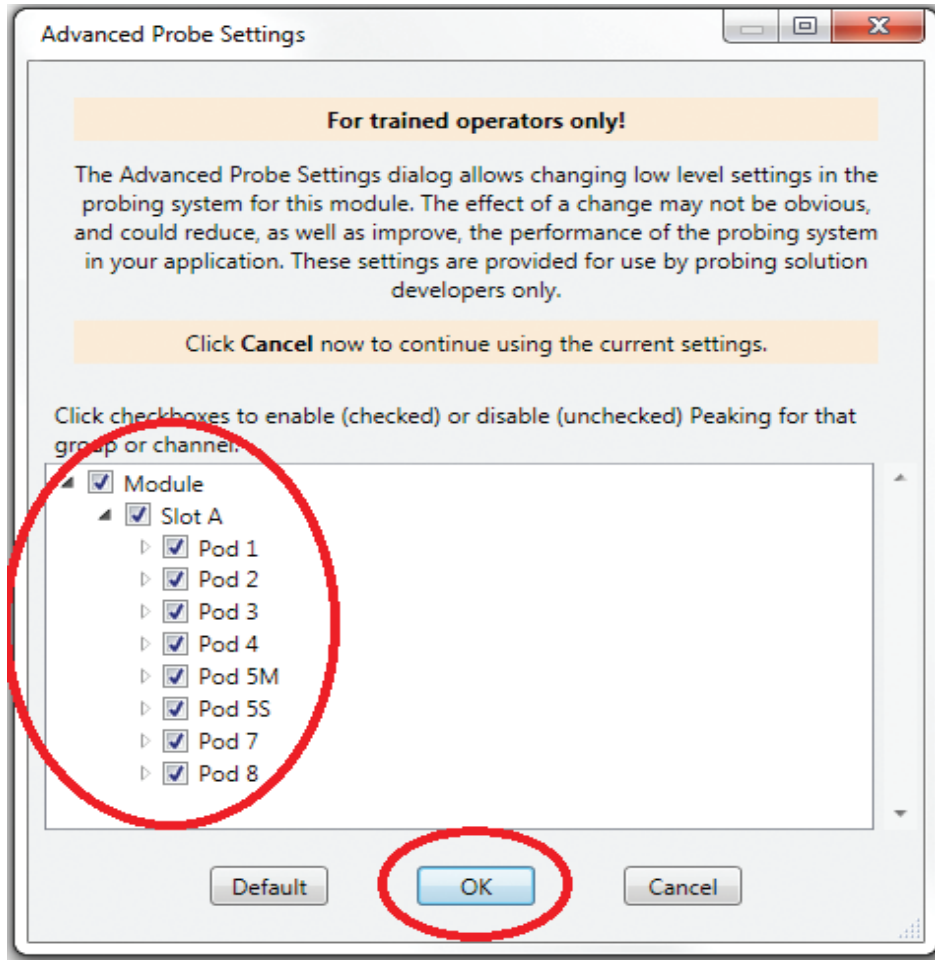

Figure 4. Advanced Probe Settings window. APS can be disabled from this window or from the Edit Options Window. It must be enabled in both windows.

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