Keysight Technologies

An Innovative Simulation Workflow for Debugging High-Speed Digital Designs Using Jitter Separation

White Paper

Abstract

This paper presents a new simulation workflow for jitter separation analysis. Jitter separation is a very promising tool that quickly identifies the sources of signal integrity degradation and thus enables easy optimization of a design to meet the low jitter requirements of multi-gigabit high speed digital SERDES devices.

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1.0 Introduction

As data rates in high-speed products increase, identifying and solving signal integrity problems becomes critical. Timing margins are becoming increasingly tight. Several distinct effects influence the integrity of signals.

The deviation of a signal transition from its ideal time is defined as jitter. Jitter becomes a problem when out-of-place edges start to corrupt the zero/one decision that should occur in the slicer circuit in the receiver. Breaking jitter into its various components is required to diagnose the most severe jitter problems. Several factors affect jitter. Power supply noise is a big contributor to the total jitter in the system. A power delivery network has a substantial impedance which causes a voltage ripple on the IC's supply lines. This supply noise translates into jitter on the clock and data edges. The amount of jitter is modulated by channel dispersion as signals propagate in the system. Channel loss, reflections and distortions from impedance discontinuities in the signal or return path, lead to attenuated and smeared data edges which can then cause inter-symbol interference (ISI). It is observed in both measurements and simulations that jitter can be amplified by a lossy channel even when the channel is linear, passive and noiseless [1].

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2.0 Mastering jitter by using EDA simulation

2.1 Electro-magnetic simulation

From the introduction, it is clear that the physical design plays a main role in signal integrity. An electro-magnetic (EM) simulation tool, such as Keysight Technologies, Inc. Momentum, can extract an accurate electrical model from an EDA database, which covers the entire frequency band from DC up to the highest relevant frequency which is related to the fastest rise time in the system. All aforementioned sources for jitter or jitter modulation caused by the physical design are captured in such EM model. There are however some key aspects that make one electro-magnetic simulator preferred over another.

2.1.1 Accurate EM model generation down to DC

A significant part of the energy spectrum of a time domain signal is in the DC to low frequency range. In particular, decoupling capacitors have a sharp impedance increase as the frequency drops from the 100 kHz range down to the DC point. Time-domain simulation tools require that this part of the spectrum is properly captured.

2.1.2 Accurate loss modeling for conductors and dielectrics

Conductors introduce a loss mechanism with a complex, frequency dependent behaviour. That effect can be modelled by using a surface impedance approach. The surface impedance captures the transition from a uniform current distribution at DC to a non-uniform distribution and skin-depth effect at higher frequencies. Conductor roughness can also contribute to conductor losses. Optionally, this can be specified to further refine the surface impedance by using a multi-level hemispherical model [4]. Loss in dielectric materials typically used in high speed digital boards or packages, such as FR4, are traditionally modeled assuming a simple frequency independent loss tangent. However this frequency independent permittivity is one of the sources of non-causal time domain responses. It has been demonstrated that the real part and the imaginary part of the complex permittivity must satisfy certain constraints (called the Kramers-Kronig relations) to preserve causality [5,6]. The Svensson/Djordjevic model is broadly accepted to fulfil the aforementioned causality requirement.

2.0 Mastering jitter by using EDA simulation (continued)

2.1 Electro-magnetic simulation (continued)

2.1.3 Simulation performance: Capability of handling many pins

Digital designs make frequent use of parallel busses. The number of input/output pins is typically large and it needs to be considered when choosing the method of computation of an EM simulator.

2.2 Fast channel simulation

Channel simulation is designed for rapid signal integrity analysis of linear channels in high speed serial and parallel communication links. In typical scenarios, Keysight's Advanced Design System (ADS) Channel Simulator is capable of processing million-bit patterns in approximately one minute, allowing for accurate analysis of eye diagram properties including density, width, height, bathtubs, and BER contours. The channel simulator accounts for ISI, random jitter, crosstalk, encoding, equalization, and other effects of interest to signal integrity designers. In addition to high-throughput simulations with long bit sequences, the Channel Simulator offers a statistical analysis mode for rapid calculation of statistical properties down to extremely low BERs.

2.3 Path to hardware validation

Beyond the typical SI analyses available in ADS, simulated waveforms can also be post-processed for jitter separation using Keysight's Infiniium real-time oscilloscope. It offers jitter decomposition algorithms that can separate and accurately quantify Random Jitter from Deterministic Jitter (DJ). Engineers have always had a predilection for oscilloscopes as the instrument to validate the behaviour of high speed serial data signals. From a simple eye diagram to jitter probability density functions with trend and spectral content analysis, the modern oscilloscopes such as Keysight Infiniium real-time oscilloscope can perform jitter separation. Recent improvements in the Infiniiview algorithms enable the most advanced insight into a DUT behaviour by offering DJ seperation into Data Dependent Jitter (composed of Duty-cycle Distorsion and InterSymbol Interferences), Periodic Jitter and Bounded Uncorrelated Jitter (Crosstalk Jitter). These algorithms are now go beyond simple Jitter Analysis as they can also be used to analyze vertical closing of the eye diagram by separating Random Noise from Deterministic Interferences. Thanks to Infiniiview, these new advanced jitter and noise analysis algorithms are also available for design engineers to use with simulated waveforms generated by ADS Channel Simulator. This can help to quickly understand and quantify what are the biggest eye closing factors in the system. This method allows the design team better predict if the system will meet it specifications at, say, a BER of 10e-12, and to focus their corrective actions on the most critical part of the design. Such insight and design space exploration is the best way of achieving on first-pass success for the fabricated PCB.

3.0 Presentation of the studied topology

In order to highlight the benefit of jitter separation, both measurements and simulations have been obtained using a test vehicle designed by THALES Communications & Security (Fig.1). The Stratix II GX FPGA based design consists of two differential lines (MGH) and four single-ended aggressors (SSN_SIGA). The stack-up of this test vehicle is composed of 12 layers but only the top five metal layers are significant for the high speed signals of interest. Eye diagrams of one of the multi-gigabit serial links named MGH_DIA2 were measured at the SMA connectors (Fig.2) while several aggressors were switched ON or OFF at several clock data rates.

MGH_DIA2 is a 190 mm long differential transmission line on layer 3 with one blind via on one side and a plated through hole (PTH) via on the other side. The width of the traces is w=130 µm and the spacing between the Positive channel (P) and the Negative channel (N) is s=150 µm. The transmitter of MGH_DIA2 is located in the FPGA "MN2" and its termination is a 100Ω differential impedance. SSN_SIGAs are single-ended simplex signals (from MN2 to MN4) and consist of buried microstrip lines on layers 2 and 3 (Fig.3). SSN_SIGA traces are approximately 160 mm long and LVTTL 3.3V transmitters are used.

As shown on Fig. 4, the positive channel MGH_DIA2_P is not directly on top of one of the two power planes "VCCINT" and "VCCH" unlike the negative channel MGH_DIA_N. Moreover the spacing between positive MGH_DIA2_P and SSN_SIGA_79 (d=120 µm) is inferior to the spacing between the two differential lines (s=150 µm). This means that positive MGH_DIA2_P has a higher coupling with the single-ended SSN_SIGA_79 trace than its negative MGH_DIA2_N pair for a distance of about 7 cm. This can be a problem for high speed signals because of crosstalk and differential to common mode conversion.

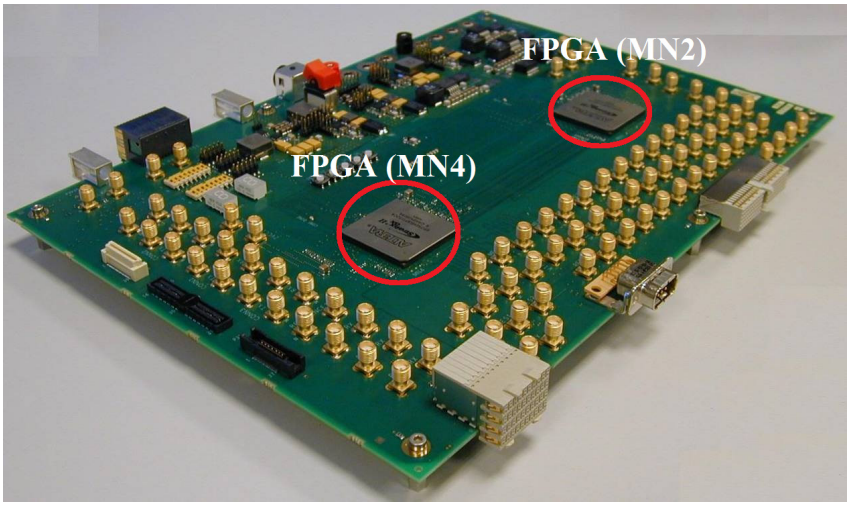

Figure 1. Test vehicle designed by THALES Communications & Security.

3.0 Presentation of the studied topology (continued)

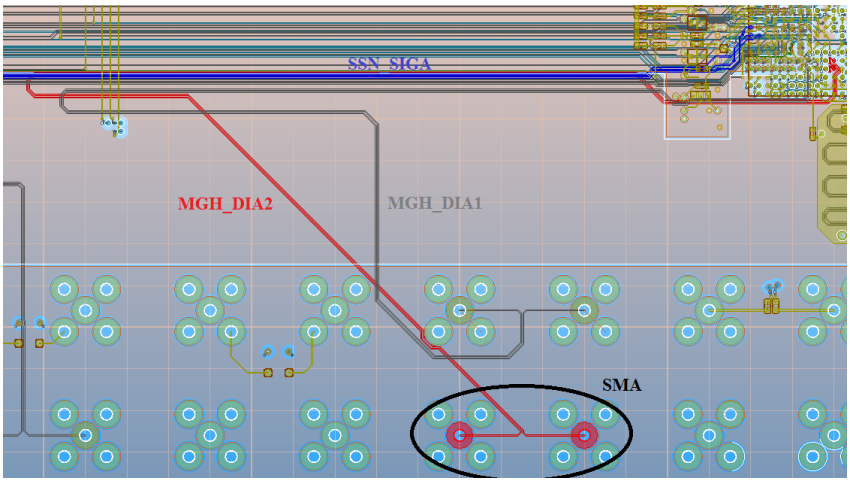

Figure 2. Differential lines (MGH) and Single-Ended aggressors (SSN_SIGA).

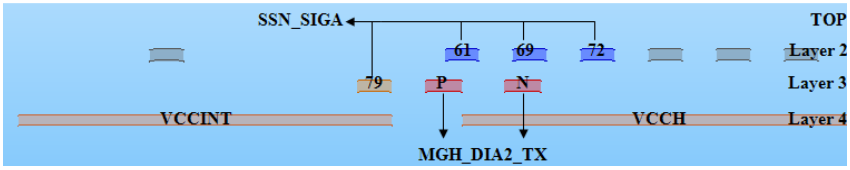

Figure 3. PCB cross section with differential and single ended nets.

4.0 Simulation settings

4.1 Electro-magnetic stimulation

The geometry of the board described above has been exported from Cadence Allegro to Keysight Momentum utilizing the ADS Design Flow Integration (ADFI) link. In order to reduce computation time and memory requirements, the critical nets are separated from the rest of the board in a process known as "critical net selection and cookie cutter" (Fig.4.). Moreover, the stack-up has been simplified by removing the copper layers from layer 5 to layer 12 but the total thickness of the board is not modified in order to keep the stub effect of the through vias. S-parameters have been calculated from DC to 10 GHz with a 5 GHz meshing. The adaptive frequency sweep calculation converged after 340 frequency points in 13 hours with 16 CPU cores and 16 GB RAM. The results of this EM simulation are used in the schematic environment of ADS 2012.08.

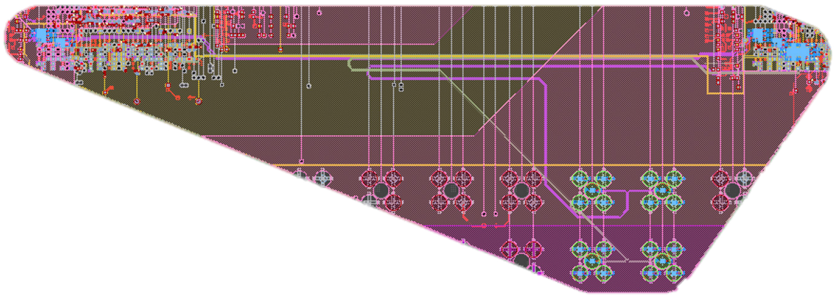

Figure 4. Section of the board simulated with ADS Momentum.

3.2 Circuit simulation

The channel simulations we want to proceed are not harmless because of very different characteristics of the signals taken into account (differential, single-ended, different data rates...). Indeed, high-speed serial links are coupled with low frequency signals (less than 200 MHz) which are respectively differential and single-ended signals. It is not possible to directly combine IBIS AMI models with IBIS models in the same computation for crosstalk studies because the IBIS AMI standard does not directly support single-ended I/O. Moreover, the IBIS AMI model of the Stratix II GX is not available. However, in the generic IBIS AMI models available in ADS, we have overstepped these limitations by modifying the IBIS model of the single-ended 3.3V LVTTL model to make it differential (Fig.5.). Then, the above scenarios with single ended, differential, and multiple data rates can be easily described in a channel simulation. The only caveat is that one must pay close attention to how the single-ended signal is converted to differential.. Return Path in single-ended I/Os is critical but it will not be taken into account in this type of Channel Simulation. An alternative configuration would be to use exclusively IBIS models so that the coupling through the return path (captured in the EM model) will be properly computed. The differential voltage output of the high-speed drivers has been set to 800 mV and a PRBS7 is used. The s4p package of the Stratix IV FPGA has been added at the output of the high speed drivers. Then, the Channel Simulator is launched in the "bit-by-bit" mode and 1 Mbits are acquired. The waveform is recorded in a *.bin file which

4.0 Simulation settings (continued)

4.2 Circuit simulation (continued)

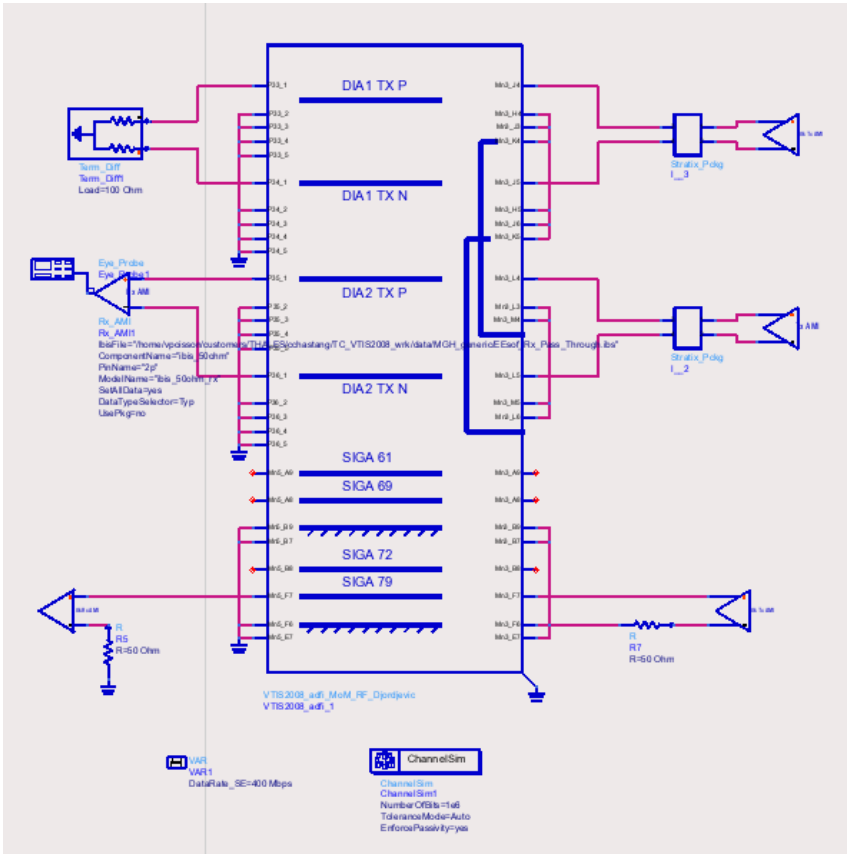

Figure 5. Mix of IBIS AMI models and IBIS models in ADS 2012.08.

5.0 MGH_DIA2 without single-ended aggressor

In order to observe the influence of the crosstalk on the eye diagram and the jitter separation of MGH_DIA2, its behaviour is analysed with the adjacent single-ended aggressor turned off. Unfortunately, the FPGA program only allows us to activate groups of four high speed links, so, MGH_DIA1 could still cause crosstalk on MGH_DIA2. Circuit simulations show us that the contribution of MGH_DIA1 on MGH_DIA2 reduces its eye opening by 20mV. The Random Jitter got by measurements is implemented into the IBIS AMI model of the MGH_DIA2 driver (RJ=0.02UI).

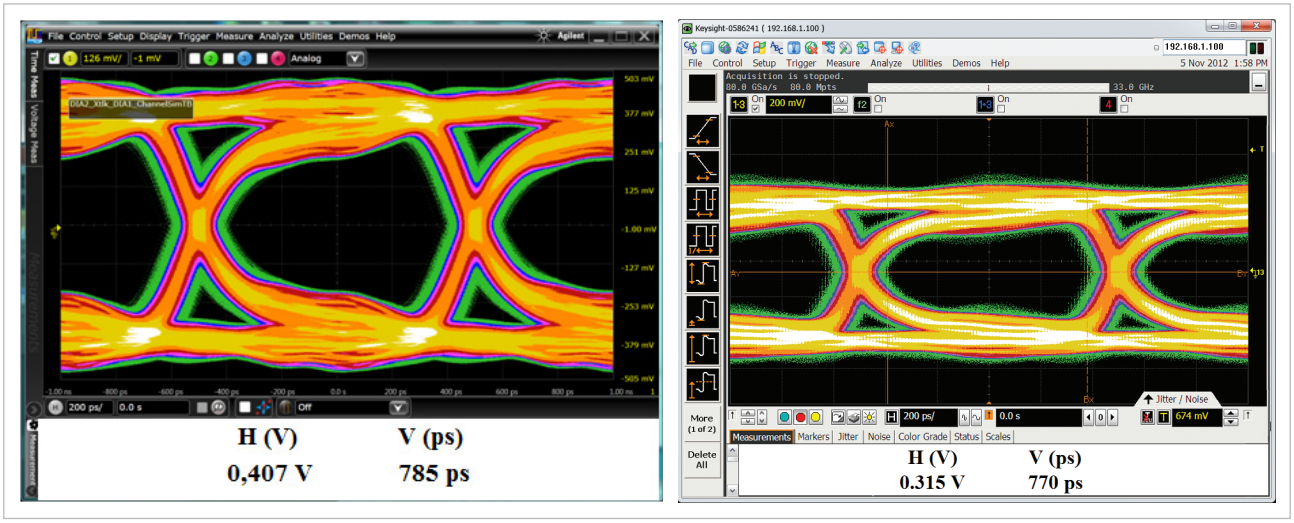

Figure 6. MGH_DIA2 eye diagram at 1 Gbps without single-ended aggressor. Simulation (LEFT), Measurment (RIGHT).

As shown on Fig.6 and Table I, the eye openings and jitter separations of MGH_DIA2 are quite similar in simulation and measurement. The presence of BUJ is due to the crosstalk between MGH_DIA2 and MGH_DIA1 and the unusual value of RJ show us a problem with the code of the PLL in the FPGA. Because of limitation in the IBIS AMI standard, noise due to power plane like SSN (Simultaneous Switching Noise) [5] is not taken into account. So, despite the calibration of the IBIS AMI model, PJrms, DCD and RJrms are undervalued in the simulation. Although all simulation parameters are not optimally set, the overall methodology is validated.

Jitter	Measurement	Simulation
TJ (BER-12)	375 ps	333 ps
RJrms	24 ps	20 ps
DJpp	41 ps	50 ps
PJrms	5 ps	1 ps
DDJpp	31 ps	41 ps
ISIpp	27 ps	40 ps
BUJpp	34 ps	40 ps
DCD	5 ps	0 ps

Table 1. Jitter separation of MGH_DIA2 without single-ended aggressor.

6.0 MGH_DIA2 with single-ended aggressor

In this part, the single-ended trace SSN_SIGA_79 is excited by the IBIS model of Stratix II GX. The signal is a LVTTL 3.3V square wave at 50 MHz.

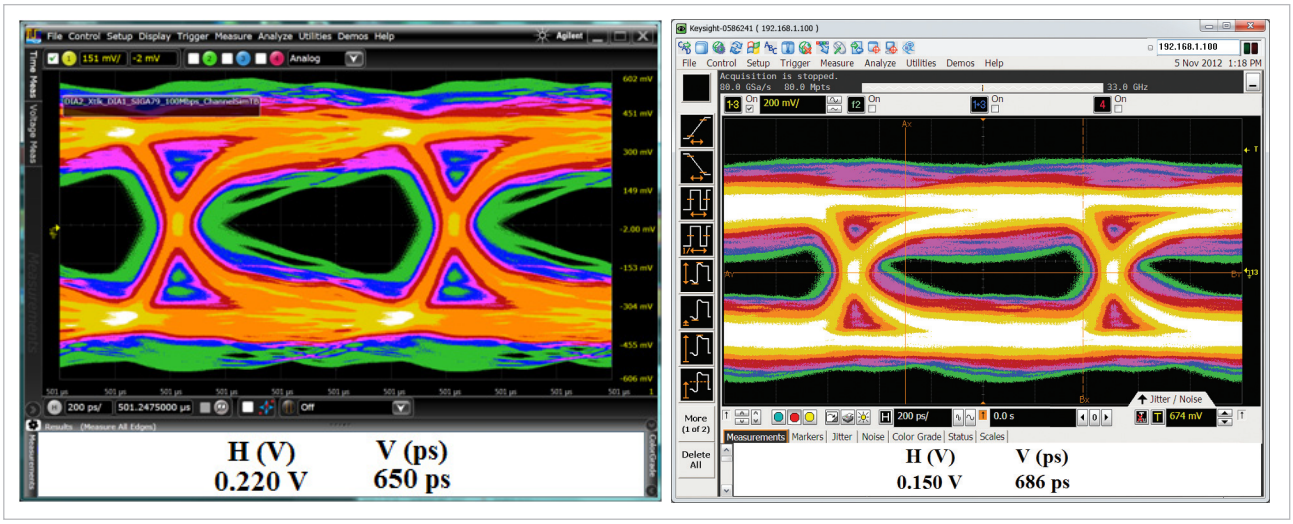

Figure 7. MGH_DIA2 eye diagram at 1 Gbsp with SSN-SIGA_79 at 50 MHz. Simulation (LEFT), Measurment (RIGHT).

Fig.7 compares simulated and measured eye diagrams of MGH_DIA2 at 1 Gbps. The eye opening has dramatically decreased due to crosstalk with SSN_SIGA_79. Because of the simplification of the EM model and the lack of power noise, the eye diagrams from simulation and measurement are not identical. However, the ratios between the MGH_DIA2 eye opening with and without the single-ended aggressor are quite similar:

– Simulation: $\Delta H=220/407=0.54$ and $\Delta V=650/785=0.83$
– Measurement: $150/315=0.48$ and $\Delta V=686/770=0.89$

Compared to Table I, jitter separation on Table II shows us that BUJ has tremendously increased, proving the presence of crosstalk on MGH_DIA2. The other jitter elements remain stable except for ISI, probably because of the interaction of additional reflections due to the crosstalk.

Jitter	Measurement	Simulation
TJ (BER-12)	438 ps	431 ps
RJrms	23 ps	20 ps
DJpp	108 ps	151 ps
PJrms	19 ps	26 ps
DDJpp	30 ps	58 ps
ISIpp	28 ps	57 ps
BUJpp	102 ps	127 ps
DCD	3 ps	0 ps

Table 2. Jitter separation of MGH_DIA2 without SSN_SIGA at 50 MHz.

7.0 Conclusion

This paper presents a new method for debugging high-speed serial links using jitter separation. In order to carry out this study, a new simulation flow has been defined. The geometry of the board is exported from Cadence Allegro to ADS Momentum in order to characterize the layout with EM simulations. Then, the results, presented as s-parameters blocks, are used in the ADS schematic environment allowing calculation of waveforms, taking into account IBIS and IBIS AMI models simultaneously. Finally, eye diagrams and jitter separations are studied in Keysight Infiniiview. This jitter separation method can be set up quickly and allow us to immediately determine which phenomenon is causing the worst degradation in the system. Thanks to this analysis, we will be able adapt the solution for each design problem by increasing the spacing, adding pre-emphasis or equalization, reducing via stub length, etc... However, design margins must still be added to account for the lack of power noise sources in the IBIS AMI standard which results in differences between simulation and measurement.

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