Keysight Technologies
GaAs MMIC TWA Users Guide

Application Note

Includes:

1. Device Schematic, Topology, and Theory of Operation Descriptions
2. Assembly, Bonding, & Biasing Recommendations
3. Extended Low–Frequency Operation Assembly Guidelines
4. Variable Gain Control Operation

KEYSIGHT TECHNOLOGIES

1.0 Introduction

This application note gives a technical overview of the TC700, TC702 and TC900 GaAs MMIC Traveling Wave Amplifiers (TWA). As a group, these amplifiers cover the 2 to 26.5 or 50 GHz frequency range with small signal gains between 8.5 and 9.5 dB, P1dB compression points up to 22 dBm at 20 GHz, 19 dBm at 26.5 GHz, or 10 dBm at 50 GHz. The TC700 models (1GG7-4012/13/14/15) represent four different RF screening levels of the same GaAs MESFET–based MMIC amplifier. The 1GG7-4115 has typical RF specifications, the 1GG7-4114 has guaranteed RF specifications up to 22 GHz, and the 1GG7-4112 or 1GG7-4113 are guaranteed up to 26.5 GHz. Also discussed in this application note is the TC702, a family of higher power MES-FET–based GaAs MMIC amplifier, (part numbers 1GG7-4019/20/21); and the TC900, a PHEMT– based GaAs MMIC TWA that delivers guaranteed RF specifications up to 50 GHz (part number 1GG6-4000).

These MMIC amplifiers also include two very useful design features: variable gain control, and a unique topology allowing operation to frequencies into the kHz range using external components. A detailed discussion of these topics, and how to properly bond and bias the amplifiers, will be covered in this application note.

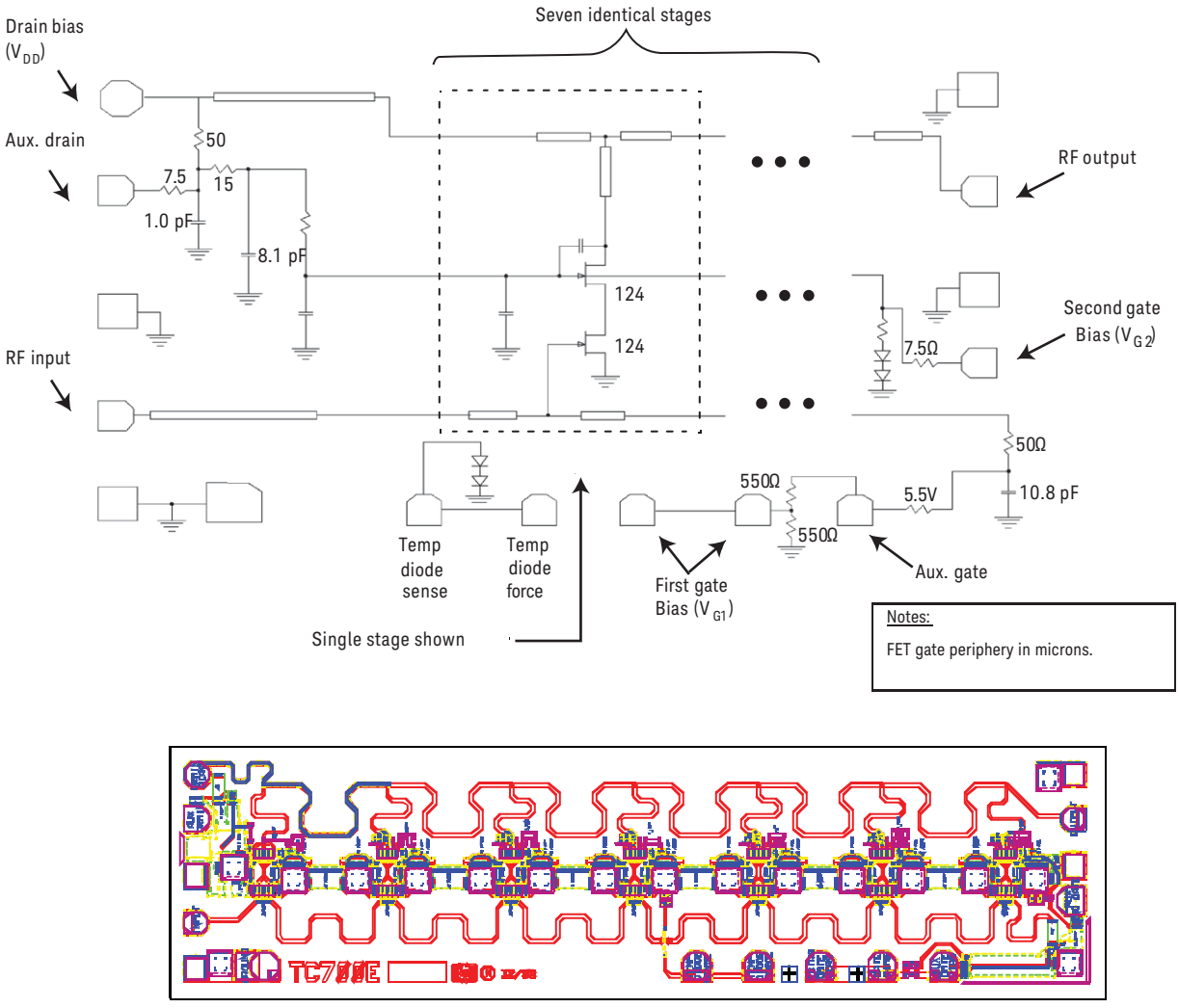
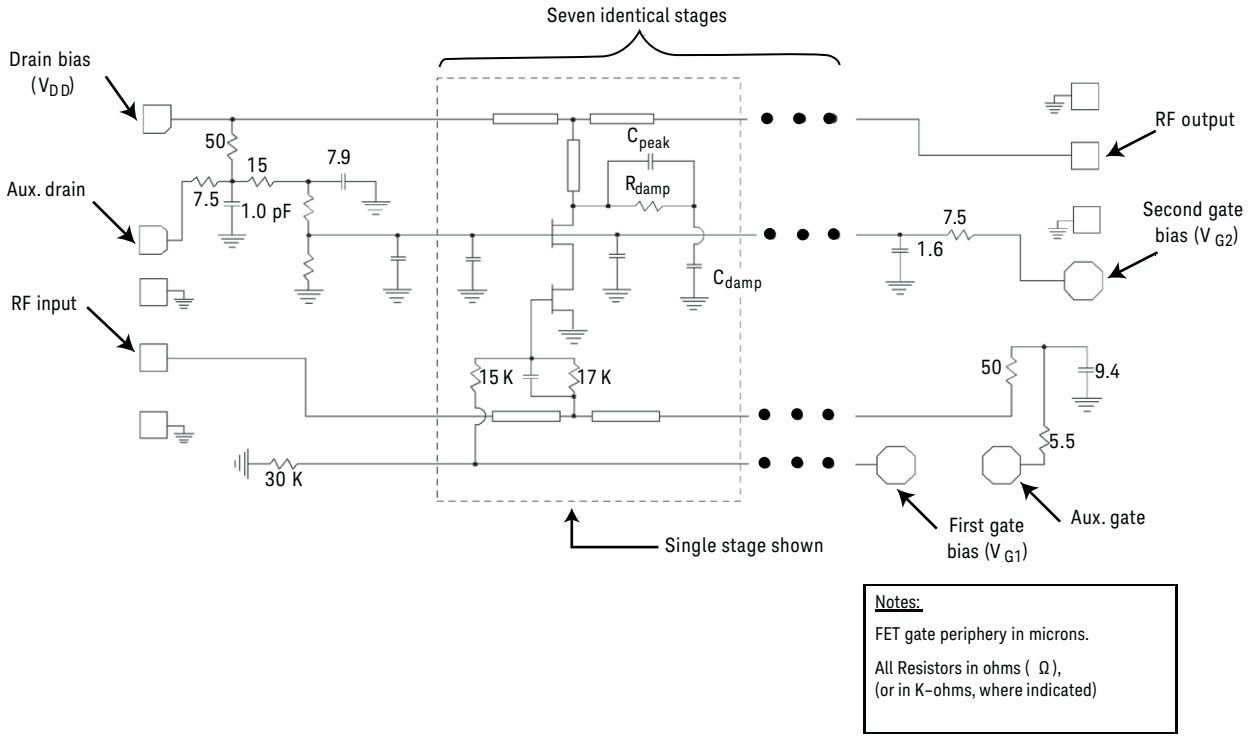


Figure 1. TC700 TWA schematic and topology

2.0 Device Schematic and Topology

The device topology and schematic for the TC700, TC702, TC900 are shown in Figures 1, 2, and 3, respectively. The various TC700 versions are all structurally the same, and the bonding and biasing techniques are identical. Each GaAs MMIC amplifier is a cascade of seven cascode stages. The cascode stages in the TC700 and TC702 use two 124 µm and 248 µm gate–width FETs, respectively. The larger gate periphery on the TC702 provides about 2.5 dB more output power (19 dBm typical) and slightly less gain than the TC700 (7.5 dB vs. 9.3 dB) at 26.5 GHz. The 50 GHz TC900 incorporates seven cascoded FET pairs stages with 48 µm gate–width per FET.

Refer to the TC700 schematic in Figure 1 for the following discussion. The RF input drives the lower FET of each stage of the MMIC amplifier from a series of transmission lines known as the “gate line.” The gate line is terminated in 50 Ω to ground through a 10.8 pF capacitor and includes a resistor network through which the gate bias (V_{G1}) is fed into the amplifier. This resistor network also includes an additional bonding pad (labeled Auxiliary Gate) that can be used with an external capacitor to extend the lower frequency range of the amplifier. This topic will be covered in detail later.



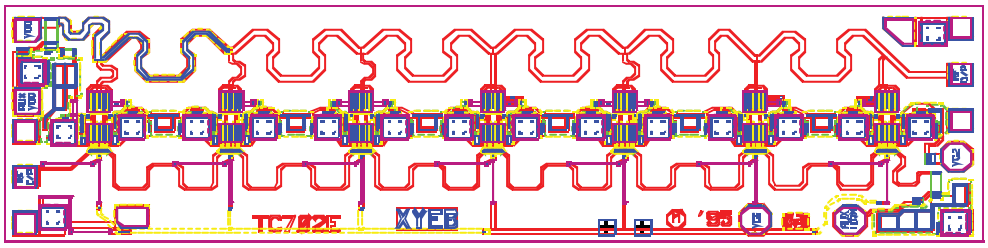


Figure 2. TC702 TWA schematic and topology

The RF output is connected, via the “drain line,” to the drains of the upper FETs of each stage and is terminated in a 50 Ω resistor. In this case, the terminated end of the 50 Ω resistor utilizes a special network that includes a shunt 1.0 pF capacitor connected to another shunt 8.1 pF capacitor through a 15 Ω resistor. The drain line termination also incorporates a resistor/shunt diode divider network which is used to set the operating bias point for the top row of FETs. This network includes an additional bonding pad (labeled Auxiliary Drain) that can be used with an external capacitor to extend the lower frequency range of the amplifier.

The schematic of the TC702 is similar to that of the TC700 with the exception of the gate line configuration. The TC702 incorporates two gate lines. See Figure 2. The first is an RF path which drives the lower FET of each stage and is terminated in 50 Ω. A bias gate line is used to feed DC bias to each FET through 15 KΩ resistors and is terminated in 30 KΩ to ground.

The schematic of the TC900 is also similar to that of the TC700 with slightly different gate–line and drain–line termination resistor values. See Figure 3. The bonding pads for the TC700, TC702 and TC900 are also shown in Figures 1, 2, and 3. Except for the TC900, the size of the DC bias pads is slightly larger than the RF pads to facilitate bonding. Adjacent to the RF input and output pads are additional ground pads which are only used during initial device testing, and can be used in conjunction with a coplanar launch structure. No bonds to these pads are required for normal operation since RF and DC ground is provided on chip by conductive vias.

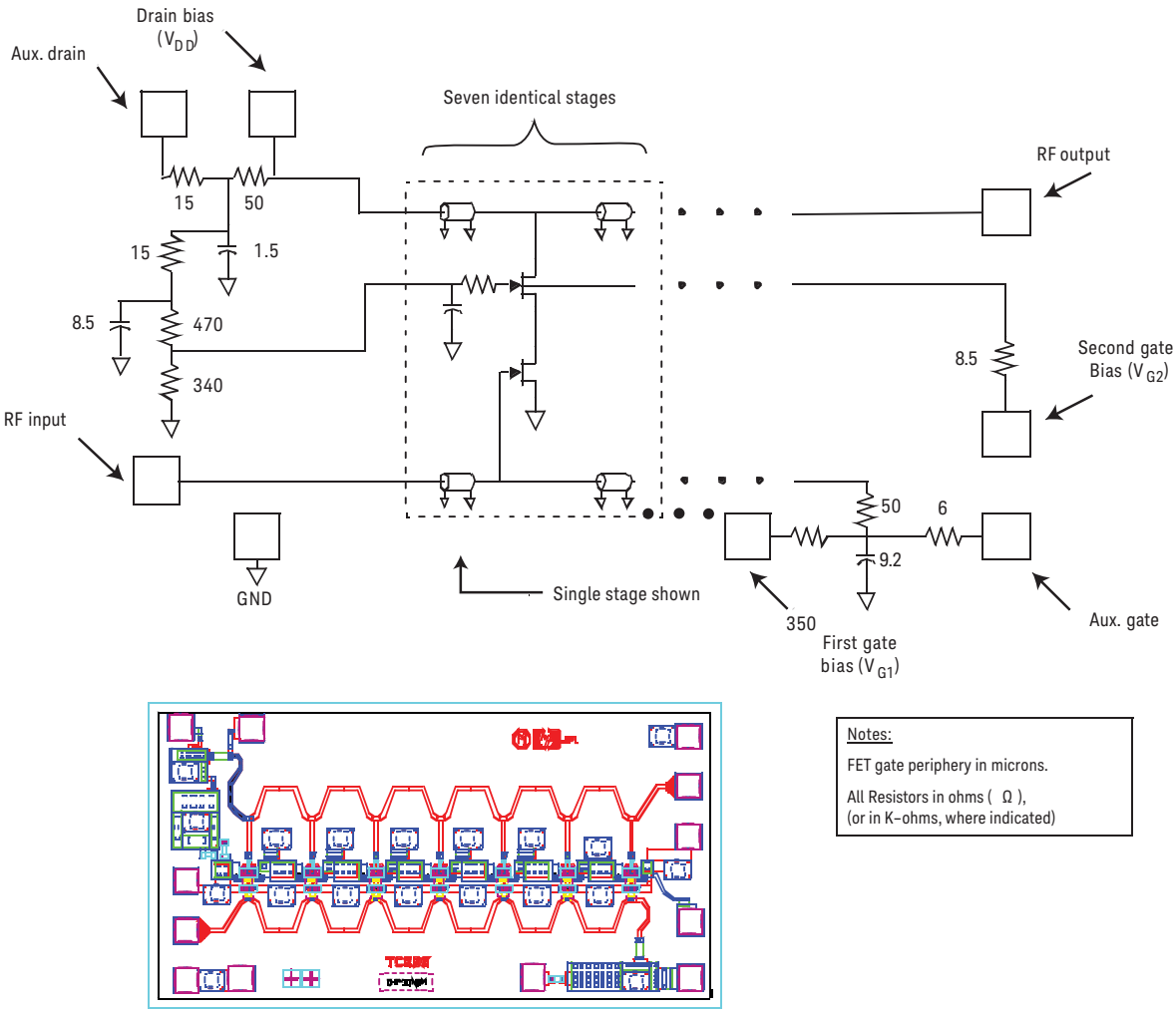


Figure 3. TC900 TWA schematic and topology

Using the simplest form of bonding, the TC700 and TC702 amplifiers will provide excellent RF performance over the full 2 to 26.5 GHz frequency range and the TC900 will operate to 50 GHz. The next sections describe how to properly bond and bias the amplifiers to get optimum performance.

3.0 Bonding the TWA

Only two RF and two DC bonds are needed for normal operation of the amplifiers. These RF bonds should be made with 500 line/inch gold mesh[1] to both the RF input and output pads on the TWA. These bonds should be kept as short as possible to reduce the RF lead inductance. Single 0.7 mil. or 1.0 mil. diameter gold wire may be used in place of the RF mesh bond, however, high frequency performance (> 20 GHz) will degrade slightly due to the increased inductance, especially for the TC900. Specifically, gain will decrease and input/output return loss will degrade slightly. The two DC bonds required include the FIRST GATE BIAS (V_{G1}) and DRAIN BIAS (V_{DD}) bonds (Figure 1). The gate bias is used to control the drain current (I_{DD}) of the device. The length of the gate bond wire is not critical because an on–chip decoupling circuit isolates the cascode stages of the MMIC amplifier from the external gate bias network. The gate bond wire is normally made short to insure mechanical rigidity. In cases where the bond wire must span great distances, small bonding islands can be used to split the length into shorter loops. Gate bias should only be applied using the FIRST GATE BIAS (V_{G1}) bond pad. Although gate bias can be fed into the device through the AUX GATE or RF INPUT pads, doing so will circumvent the on–chip protection circuit, designed to prevent excessive gate current under saturating RF drive levels, and therefore is not recommended. On the TC700, circuit consists of a series 550 Ω and a shunt 550 Ω resistor. On the TC702 the combination protection/ decoupling circuit consists of series 15 KΩ resistors between the gate bias line and the gates of each FET, and a shunt 30 KΩ resistor which terminates the gate bias line. On the TC905, these circuits consists of a series 350 Ω resistor.

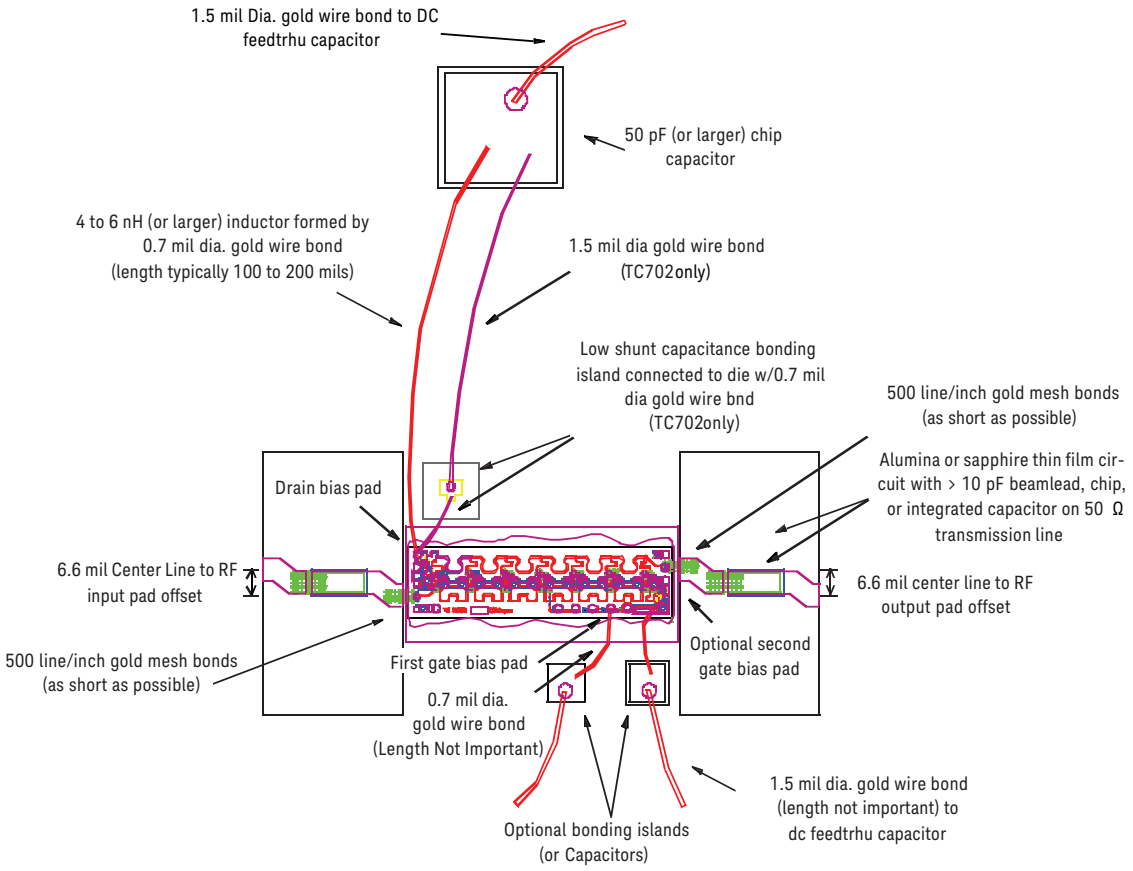


Figure 4. Typical bonding configuration for 2 to 26.5 GHz operation.

1. Buckbee–Mears Co., St. Paul, MN, (612-228-6400)

The length of the drain bias bond wire will affect the RF performance of the TWAs and is discussed in detail in the section entitled, “Drain Inductance.” Drain bias should be applied to the amplifier using the DRAIN Bias pad (V_{DD}). The transmission line between the drain bias pad and the first two stages has been reinforced with thicker gold to prevent electromigration in the event of excess DC current and is generally recommended for assemblies designed to operate over the 2 to 26.5 or 50 GHz frequency range. For broadband performance including operation to frequencies below 100 MHz, which is possible through the use of off–chip low–frequency circuitry (described later), the drain bias may be fed into the RF output pad by incorporating the drain bias RF choke circuitry into the AC coupling structure at the device output. However, the user is cautioned to insure the current drain through the RF output port is not allowed to exceed I_{DSS} of the device for indefinite periods. No bonds are required to any other pads for typical 2 to 26.5 (50) GHz operation.

A typical bonding configuration for 2 to 26.5 GHz operation on the TC700/TC702 is shown in Figure 4. The device is die–attached to a gold–plated molybdenum shim using a fluxless solder process. The suggested thin film circuits include 10 pF capacitors in series with the 50 Ω line. The lengths of the thin film circuits should be kept as short as possible for best small–signal gain performance. All DC bonds may be made using 0.7 mil diameter gold wire with the exception of the drain bias bond on the TC702. The current drawn by the TC702 (typically 250 mA) would stress and possibly fuse a long length of 0.7 mil diameter gold wire. The fusing current for pure gold bond wire is inversely proportional to the length of the bond. Table 1 lists the fusing current for various pure gold bond wire diameters as a function of the bond wire length.

Table 1 shows that a 1.5 mil diameter wire will easily handle the current of the TC702, but the drain bond pad is too small to directly bond a 1.5 mil wire onto it. A different bonding scheme is required to accommodate the larger diameter bond wire. When assembling a TC702, a low capacitance (< 100 fF) fused silica or alumina bonding island should be epoxied as close as possible to the drain bias pad of the TC702. Then, a short 0.7 mil diameter gold wire bond can be added between the bias pad and the bonding island. Due to the short length of the bond it will not fuse open. A long 1.5 mil bond may then be added between this island and the chip capacitor. The long length of this bond provides enough inductance to present a high impedance to the output drain line at frequencies below at least 2 GHz. Either a 0.7 mil or 1.0 mil diameter bond wire provides sufficient current carrying capacity for the TC900 TWA. A more general discussion of die–attach, bonding, and handling of GaAs MMICs can be found in application note, *GaAs MMIC ESD, Die Attach and Bonding Guidelines*, literature number 5991-3484EN.

Table 1. Fusing currents for pure gold bond wire

Fusing current (mA)

	Wire diameter		
Length (mils)	**0.7 mil**	**1.0 mil**	**1.5 mil**
50	800	1800	4700
100	450	1200	3300
200	250	750	2500
300	170	580	2100

4.0 Biasing the TWA

The proper DC biasing technique for the TWA is similar to that of a discrete FET. A negative voltage is required for the gate bias and a positive voltage is required for the drain bias.

Table 2 shows the recommended continuous operating bias values for the TC700, TC702 and the TC900. The simplest method for providing the bias to the TWA is to use two separate supplies; one positive and one negative. The positive supply must be able to supply enough current to meet the operating conditions specified in Table 2. Figure 5 shows a simple biasing setup which allows convenient monitoring of voltages and currents for the gate and drain.

Table 2. Recommended operating bias conditions

Parameter	TC700	TC702	TC900	Units
V_{DD}	7.0	8.0	5.0	volts
I_{DD}	150	250	75	mA
V_{GG}	~ –0.25	~ –0.4	~ –0.45	volts
I_{DSS}	200	350	150	mA

The recommended technique for applying bias to the GaAs MMIC amplifiers is outlined below. It assumes that the amplifier is assembled into an evaluation package with bonds connecting the device to external DC feedthru pins.

1. Connect the amplifier ground to the power supply commons before connecting the gate and drain leads. Be sure the voltages on both supplies are set to ZERO and any RF input signal is removed.
2. Connect the gate lead and then the drain lead to the package bias pins.
3. Slowly increase the negative gate voltage (V_{GG}) to about –2 volts. This should be enough negative potential to insure the device is in pinch– off.
4. Increase the drain voltage (V_{DD}) to +7 volts for the TC700, or +8 volts for the TC702, or +5 volts for the TC900.
5. Decrease the gate voltage (i.e., less negative voltage) until the drain current (I_{DD}) is 150 mA, 250 mA, or 75 mA for the TC700, TC702, or TC900, respectively.

5.0 Extended Low Frequency Performance

The TWAs can operate down to frequencies as low as a few hundred kilohertz with a few simple modifications to the standard assembly of Figure 4.

The low frequency performance of the TWA can be extended by doing the following:

1. Add external capacitors to the Auxiliary Gate (Aux Gate) and Auxiliary Drain (Aux Drain) bonding pads to improve the low frequency match.
2. Increase the capacitance of the DC blocking capacitors (C_{DC}) at the RF input and output ports.
3. Increase the inductance of the drain inductor (L_D) to provide a high impedance bias feed at lower frequencies.

All three factors are equally important since any one can limit the low frequency performance. The following sections discuss how to select these components for low frequency response. The following description and table values apply to the TC700 TWA and can be recalculated for the TC702 or TC900 using the formulas given.

5.1 Auxiliary drain and gate bypass capacitors

The ability to extend the low frequency of the TC700 , TC702 or TC900 is largely possible due to a key feature designed into the TWAs: access to both the drain and gate on–chip bypass capacitors using the AUX GATE and AUX DRAIN bond pads. Several low frequency performance characteristics are affected by the addition of external circuitry to these pads, and only the most significant characteristics are described here. Specifically, gain peaking around 1 to 1.5 GHz, and improvement in the input/output return loss and gain at frequencies below 2 GHz are discussed.

The drain and gate lines are terminated with a on–chip 50 Ω resistor to ground through on–chip capacitors ranging in value from 1 pF to 10 pF. Below about 2 GHz, these small capacitors are poor RF shorts. Input and output return loss degrades as the drain and gate line loads deviate from 50 Ω.

The loads can be restored close to 50 Ω, and RF performance improved, by adding large external capacitors (C_{AUX}) in parallel with the on–chip capacitors as shown in Figure 6. The capacitors must be attached from the AUX GATE bonding pad to ground and from the AUX DRAIN bonding pad to ground.

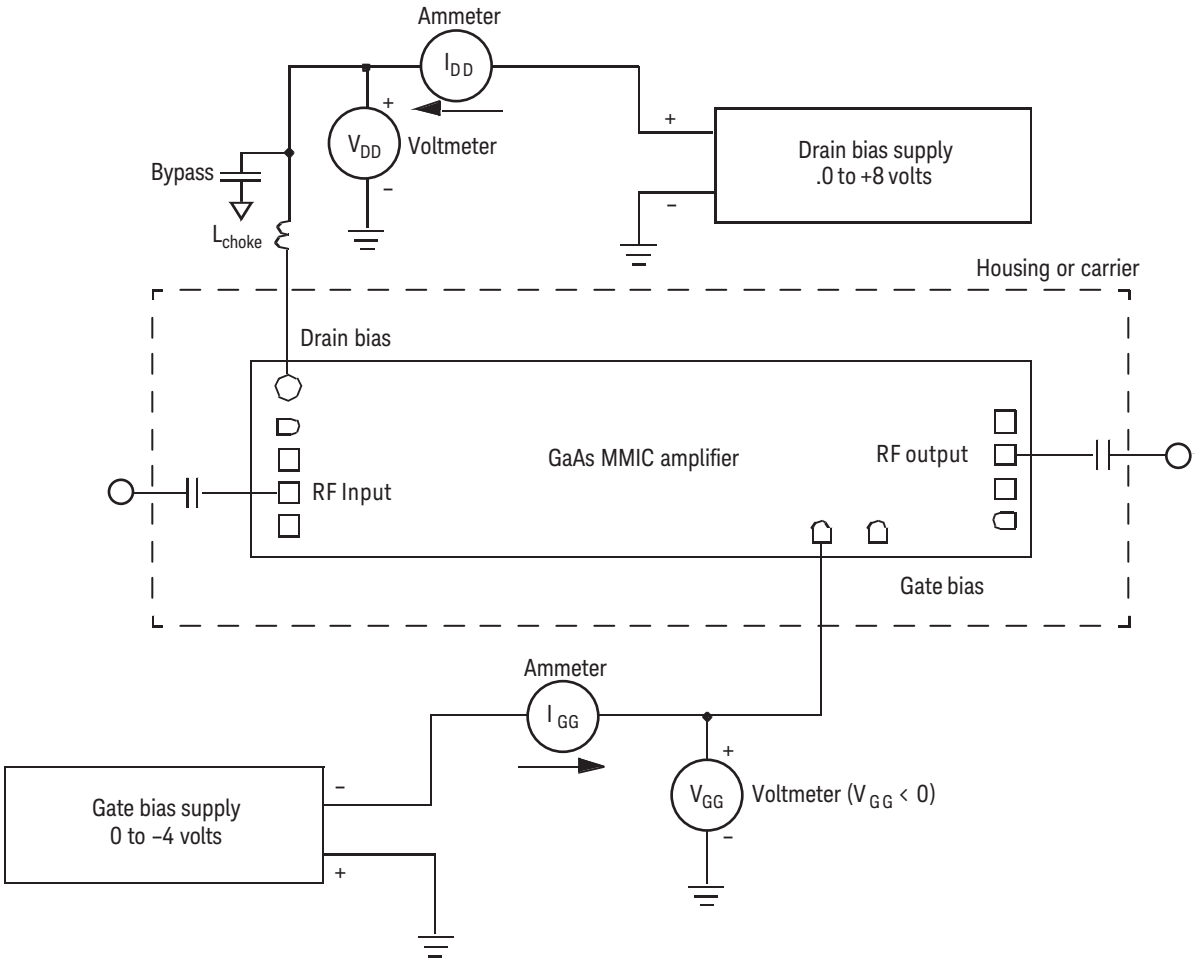


Figure 5. Simple power supply configuration for applying bias to the TWA

When bypass capacitors are connected to the AUX pads, the low frequency limit is extended down to the corner frequency determined by the bypass capacitor (C_{AUX}) and the combination of the on–chip 50 Ω load and small de–queing resistor. At this frequency the small–signal gain will increase in magnitude and stay at this elevated level down to the point where the C_{AUX} bypass capacitor acts as an open circuit, effectively rolling–off the gain completely. The low frequently limit can be approximated from the following equation:

$$fC_{AUX} = \frac{1}{2\,\pi(R_o + R_{DE\text{-}Q})\,C_{AUX}}\ (Hz)$$

where,

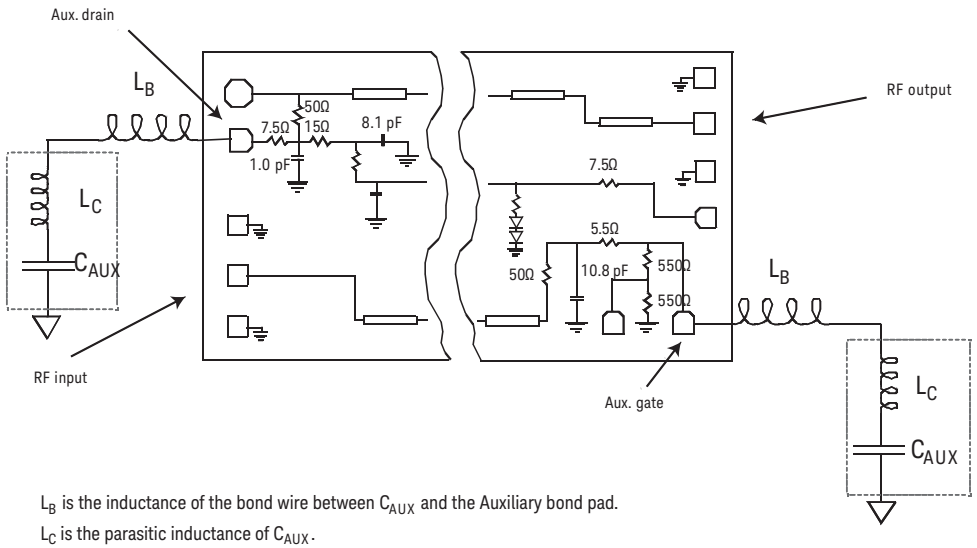
R_o is the 50 Ω gate or drain line termination resistor.
$R_{DE\text{-}Q}$ is the small series (< 15 Ω) de-Q'ing resistor,
and,

C_{AUX} is the capacitance of the bypass capacitor connected to the AUX DRAIN or AUX GATE pad in farads.

With the external bypass capacitors (C_{AUX}) connected to the AUX GATE and AUX DRAIN pads, gain will show a slight increase between 1.0 and 1.5 GHz. This is due to a series combination of C_{AUX} and the on–chip resistance but is exaggerated by the parasitic inductance of the bypass capacitor (L_C) and the inductance of the bond wire (L_D). Therefore the bond wire from the Aux pads to the bypass capacitors should be made as short as possible. The small 5.5 and 7.5 Ω resistors (TC700) are included on–chip next to the GATE AUX and DRAIN AUX bond pads to deque the effects of this parasitic inductance and limit the amount of peaking in gain.

In a typical assembly, the bypass capacitors are usually monoblock capacitors on the order of 0.01 or 0.047 µF depending on the desired low frequency operating point. These monoblocks have series parasitic inductance (L_C) of ~0.8 and ~1.3 nH for 0.01 and 0.047 µF capacitors, respectively.

Using the preceding formula, the required bypass capacitor value can be calculated for various desired corner frequencies. Since this equation does not take into account TWA transmission line impedances and on–chip resistive networks, a more accurate capacitance value may be obtained by modeling the TWA with a linear simulation program and an accurate small–signal model for the TWA. These results are summarized in Tables 3 and 4.



L_B is the inductance of the bond wire between C_{AUX} and the Auxiliary bond pad.
L_C is the parasitic inductance of C_{AUX}.

Figure 6. Low Frequency extension using capacitors (CAUX) on the TC700 auxiliary drain and auxiliary gate bond pads

Table 3. Maximum bypass capacitance connected to AUX GATE for TC700 extended low frequency performance

	Min capacitance, ($C_{AUX-Gate}$) for f =	
Frequency (MHz)	f_{CAUX}	$f(\|S_{11}\|=10$ dB)
0.01	280 nF	450 nF
0.1	28 nF	45 nF
1.0	2.8 nF	4.5 nF
10	280 pF	450 pF
100	28 pF	35 pF
1000	2.8 pF	NR

Table 4. Minimum bypass capacitance connected to Aux drain for TC700 extended low frequency performance

	Min capacitance, ($C_{AUX-Drain}$) for f =	
Frequency (MHz)	f_{CAUX}	$f\|S_{22}\|= 10$ dB
0.01	290 nF	350 nF
0.1	29 nF	35 nF
1.0	2.9 nF	3.5 nF
10	290 pF	350 pF
100	29 pF	25 pF
1000	2.9 pF	NR

Notes:
- The modelled results listed include a total series inductance ($L_C + L_B$) of 1.5 nH.
- $f(C_{AUX})$ is the lowest frequency at which the gain has increased ~ 1 to 2 dB from the midband gain values. The values of C_{AUX} listed in this column are calculated values.
- $f|S_{11,22}|$=10 dB is the lowest frequency at which the input/output return loss is still ≤ –10 dB. The values of CAUX listed in this column are modelled values.
- NR indicates that an external bypass capacitor is NOT REQUIRED to achieve this performance.

Table 5. Minimum DC blocking capacitance for various low frequency limits

	Min capacitance, ($C_{AUX-Drain}$) for f =		
Frequency (MHz)	f_{CDC}	$f(\|S_{21}\|= -3$ dB)	$f(\|S_{11,22}\|= -10$ dB)
0.01	320 nF	240 nF	480 nF
0.1	32 nF	24 nF	48 nF
1.0	3.2 nF	2.4 nF	4.8 nF
10	320 pF	240 pF	480 pF
100	32 pF	24 pF	48 pF
1000	3.2 pF	2.4 pF	4.8 pF

Notes:
- $f|S_{21}|$–3 dB is the lowest frequency at which the gain has decreased by 3 dB. The values of CDC listed in this column are modelled values.
- $f|S_{11,22}|$= –10 dB is the lowest frequency at which the input/ output return loss is still –10 dB. The values of C_{DC} listed in this column are modelled values.

5.2 DC Blocking Capacitance

A series DC blocking capacitor is required at the RF input and output of the amplifiers as shown in Figure 7. The value of this capacitor directly affects the low frequency performance of the TWA. It must be large enough to appear as a RF short circuit at the lowest desired operating frequency. However, a capacitor or AC coupling structure with low loss and low parasitic inductance is necessary for good high frequency performance. A beamlead capacitor or planar capacitor fits these requirements in most cases. For ultra–broadband performance, 100 KHz – 50 GHz for the TC900, for example, a complicated DC blocking structure, including suspended substrates with relieved ground planes and wide RF transmission line widths on which single–layer chip capacitors and large value monoblock capacitors are mounted, may be required.

The lower frequency limit (f_{CDC}) due to the DC blocking capacitor can be calculated, to first order, by the following equation:

$$f_{CDC} = \frac{1}{2\,\pi(R_o + C_{DC})}\ (\text{Hz})$$

where,

Ro is the RF input/output terminating resistance (50 Ω). C_{DC} is the DC blocking capacitance in farads. Using this equation, C_{DC} can be calculated for different desired corner frequencies. The equation is an approximation, because it does not take into account other factors, such as transmission line impedances and TWA termination networks. A more accurate C_{DC} value may be obtained by modeling the TWA and optimizing C_{DC} to yield the desired corner frequency. The calculated and modeled results for the TC700 are shown in Table 5.

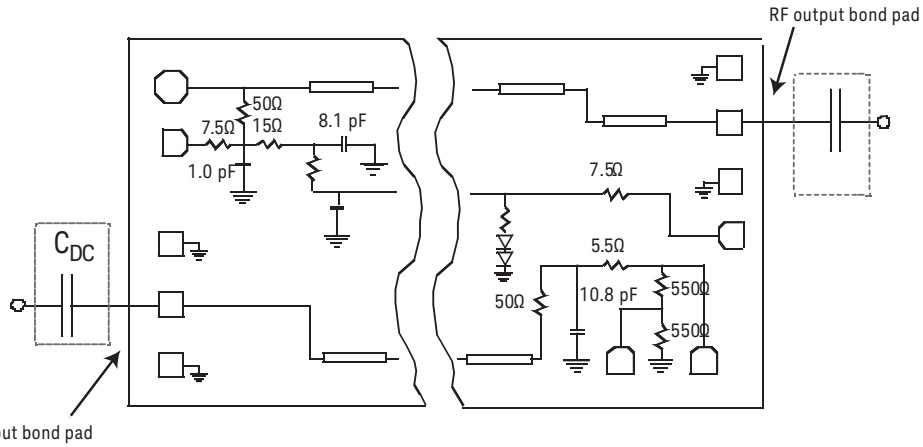


Figure 7. Location of DC blocking capacitors at the TC700 TWA RF input and output.

5.3 Drain Inductance

The drain bias pad is RF "hot" and must be isolated from the drain DC supply. Figure 8 shows a typical method of applying drain bias. This bias circuit passes DC to the drain line of the TWA while preventing the RF signal present on the drain line from appearing in the external DC biasing circuit. The series inductance of the bond wire (L_D) and the shunt capacitance of the bypass capacitor (C_D) form an RF choke circuit. The corner frequency (low frequency roll–off) is determined by the parallel combination of the drain bond wire inductance, L_D, and the on–chip 50 Ω resistor.

If the drain bond wire is too long, the bond may droop mid–span and short to the package floor, causing a DC and RF electrical short. In some assemblies, this long bond may act as a high impedance transmission line and may transform an open circuit appearing λ/4 from the drain to a short circuit at the drain bias pad. This results in a gain "suck–out" and a corresponding peak in the output return loss at the λ/4 frequency.

The recommended length for the drain bond is between 150 to 200 mils for 2–26.5 GHz operation, and 100 to 150 mils for 2–50 GHz operation; and should be bypassed in at least 50 pF to provide a good RF ground. Typically, a chip capacitor is used to provide this capacitance and acts as a bonding island between the drain bias pad and the feedthrough capacitor. Due to the length of this bond, radiative coupling between the bond and package floor, or between drain bonds of adjacent stages, may cause excessive ripple in the gain response. This may also degrade the output match the slightly at higher frequencies. To limit the gain ripple, non–conductive polyiron may be placed around the drain bond to reduce the radiative coupling. A 200 mil long bond wire has sufficient inductance to isolate the drain line from the power supply for frequencies down to about 1 GHz. To achieve operation to lower frequencies, air–coil or resonance–free, ferrite core, cylindrical or conically shaped wire–wound inductors with larger inductance values are required.

The bypass capacitor (C_D) can be either a chip capacitor, feedthrough capacitor, or a combination of the two. Its value must be large enough to insure that the series resonance of C_D and L_D is lower in frequency than that of the a parallel combination of L_D and 50 Ω. As a general rule, C_D should be greater than, or equal to, the DC blocking capacitance described earlier.

GaAs MMIC TWAs have a tendency to "bias oscillate" at frequencies between 1 kHz and 1 MHz. This is due to insufficient RF bypassing at the microcircuit or module connections. Typically, capacitive feedthroughs are employed to help suppress higher frequency oscillations. However, to prevent the low frequency bias oscillations, additional bypass capacitance (~0.1 to 0.5 µF) is required.

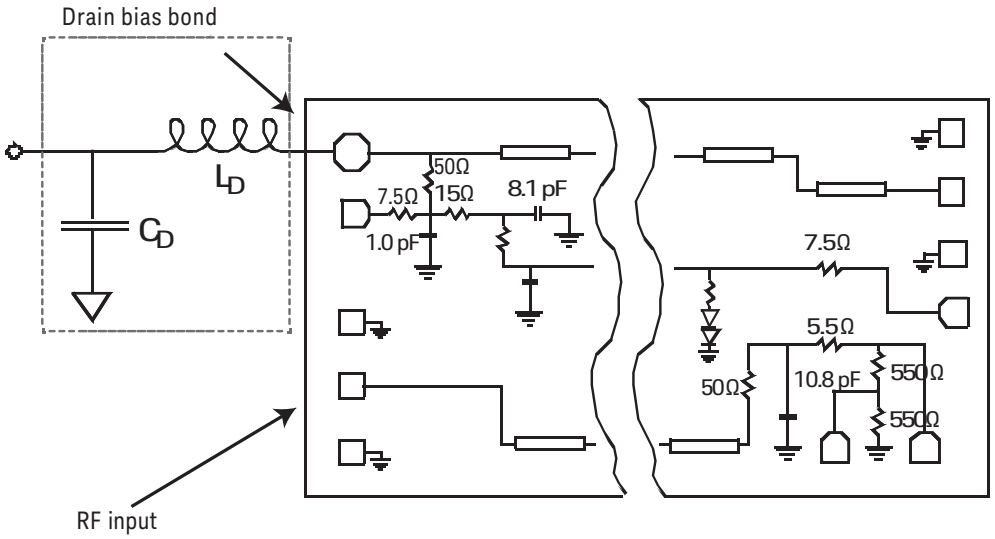


Figure 8. RF choke circuit used to isolate the drain voltage supply from the RF 'hot' drain bias

The lower frequency limit (f_{LD}) due to the drain bond wire inductance can be calculated using the following equation:

$$f_{LD} = \frac{R_o}{2 \pi L_D} \text{ (Hz)}$$

where,

R_0 is the RF input/output 50 Ω terminating resistance, and L_D is the inductance associated with the off–chip drain bias circuit.

This equation can be used to calculate the minimum values of L_D required for various desired corner frequencies. Modeling the drain bond as a lumped inductor yields slightly different results than this equation due to the termination and transmission line impedances which exist on–chip. The calculated and modelled results are shown in Table 6.

Table 6. Minimum drain bond inductance for various corner frequencies

		Min capacitance, (L_D) for f =	
Frequency (MHz)	**fL_0**	**f($\|S_{21}\|$= –3 dB)**	**f($\|S_{11,22}\|$= –10 dB)**
0.01	800 µH	400 µH	1.2 mH
0.1	80 µH	40 µH	120 µH
1.0	8 µH	4 µH	12 µH
10	800 µH	400 nH	1200 nH
100	80 nH	35 nH	115 nH
1000	8.0 nH	3.0 nh	10 nH

Notes:
– The calculated and modelled results assume a terminating capacitance, C_D, large enough to guarantee that the series resonance between C_D and L_D will be below the parallel resonance. If a fixed capacitance on the order of 1 to 20 nF is used, the minimum inductance required for operation down to 100 kHz or 1 MHz must be larger.

As a practical application of the preceding discussion, a single–stage TC700 amplifier was assembled. The amplifier was built to demonstrate the assembly techniques and performance calculations presented. The amplifier utilized 0.01 µF monoblock bypass capacitors connected to the AUX GATE and AUX DRAIN contacts, 150 pF DC blocking capacitors integrated as part of the RF input/output transmission lines, and a 5 µH wire–wound polyiron core inductor connected to the DRAIN BIAS pad.

As indicated by the preceding formula, the low frequency limit, in this case, is dominated by the 150 pF DC blocking capacitors. The bypass capacitors and drain inductor used are sufficiently large enough to guarantee a low–end limit much lower in frequency. The –3 dB roll–off in gain is 21.2 MHz and 15 MHz, for the calculated and modelled predictions, respectively. Modelled results also predicted the frequency at which the input and output return loss approached –10 dB to be about 30 MHz. The calculated and modelled results agree quite well with the measured results of the assembled amplifier. The low frequency roll–off (where gain is down by 3 dB) was measured on the amplifier to be 14.4 MHz. The input and output return loss were measured at less than –10 dB for $f \geq 29$ MHz.

In conclusion, proper application on the preceding assembly and design techniques to the TC700 , TC702 or TC900 can result in exceptional broadband performance. In this case, a 10 octave, single–stage amplifier with greater than 8 dB gain, and less than –10 dB return loss, was demonstrated over the full 30 MHz to 30 GHz frequency range.

6.0 Gain Control Using the Auxiliary Second Gate

Another feature designed into the TC700, TC702, and TC900 is the ability to control the gain of the amplifier via the auxiliary second gate bond pad. This allows the device to be used in a wide variety of applications where variable gain over a broad bandwidth is required. Such applications include automatic gain control (AGC) circuits, input signal modulation, leveled output power for improved source match and pulse modulation circuits.

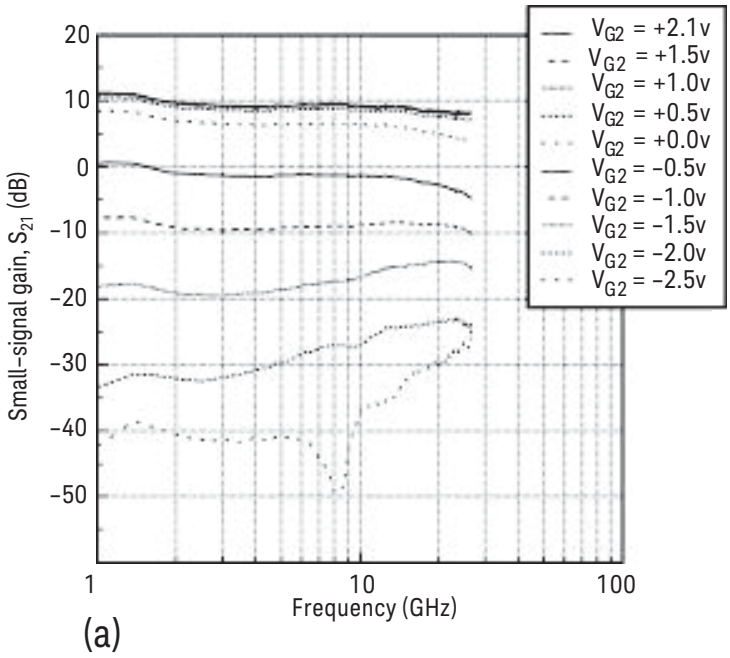
The SECOND GATE BIAS (V_{G2}) bond pad is connected to the gates of the upper FETs in every cascode stage by a small 7.5 Ω de–Q'ing resistor (TC702). The other end of the second gate line is terminated in an on–chip resistive/diode divider network which allows the second gate to self–bias to about 2.1 volts for the TC700, about 27% of V_{DD} for the TC702, and 39% of V_{DD} for the TC900. Under normal operating conditions, this pad is left open circuited, and therefore the drain current is set by the gate bias voltage applied to the lower FET in each stage. The nominal open–circuit voltage appearing at the SECOND GATE BIAS pad is about +2.1, +2.0 and+1.95 volts for the TC700 , TC702 and TC900, respectively. Under this operating condition, maximum gain and power are achieved from the TWA.

By applying an external voltage to the SECOND GATE BIAS pad (less than the open–circuit potential), the drain voltage on the lower FET can be decreased to a point where the lower FET enters the linear operating region. This will reduce the current drawn by each cascode stage and results in a decrease in gain. Second gate voltages (V_{G2}) ranging from +2.1 down to about +0.5 volts will reduce the gain of the TWA about 2 to 3 dB. Decreasing V_{G2} further will reduce the drain voltage on the lower FET towards zero, while pinching off the upper FET in each stage. At large negative values of V_{G2}, between 0.0 and –2.5 volts, the gain of the TWA will decrease significantly. This is illustrated in Figure 9, which shows the small–signal gain and output return loss (of a TC700 assembled in a small evaluation package) as a function of the voltage applied to the second gate.

Since the input and output return loss of the TWA is dominated by the gate and drain line terminations, varying the second gate voltage has minimal effect on the input/output match. This allows the user to adjust the gain of the TWA over wide dynamic range while maintaining good input/out return loss. At large negative voltages, between –1.5 and –2.5 volts, gain at lower frequencies begins to decrease more rapidly than that at higher frequencies causing significant positive gain slope. The maximum dynamic range is about 50 dB at lower frequencies and reduces to about 40 dB at high frequencies.

7.0 Conclusion

Applying simple assembly and bonding techniques to the TC700, TC702 or TC900 TWAs will provide excellent RF performance across the full 2 to 26.5 GHz, or 2 to 50 GHz frequency range. The low frequency performance can be extended through the use of special bonding techniques and external circuitry. Another feature designed into the device is the ability to control the gain of the device via the auxiliary second gate bonding pad while maintaining a good input and output match. The performance enhancements described in this application note allow the user maximum flexibility to use the TWA in a wide variety of applications.



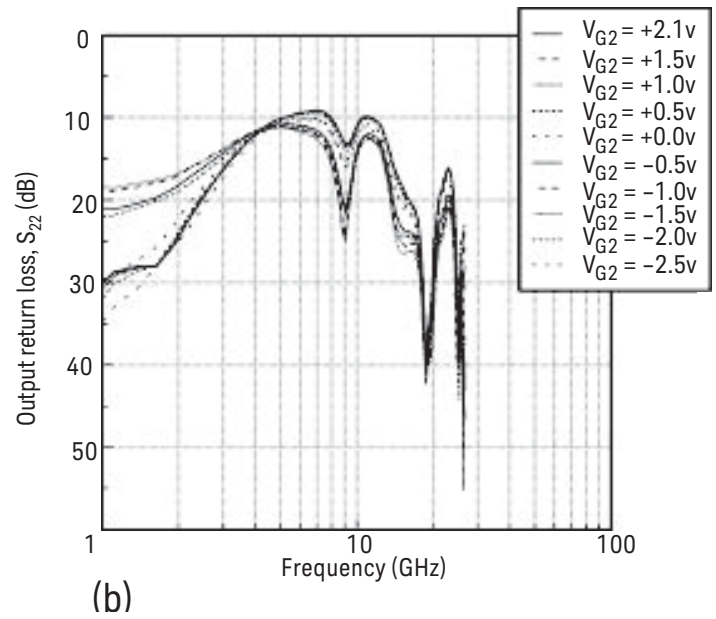


Figure 9. (a) S_{21} and (b) S_{22} of a TC700 TWA as a function of second gate voltage, V_{G2}

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