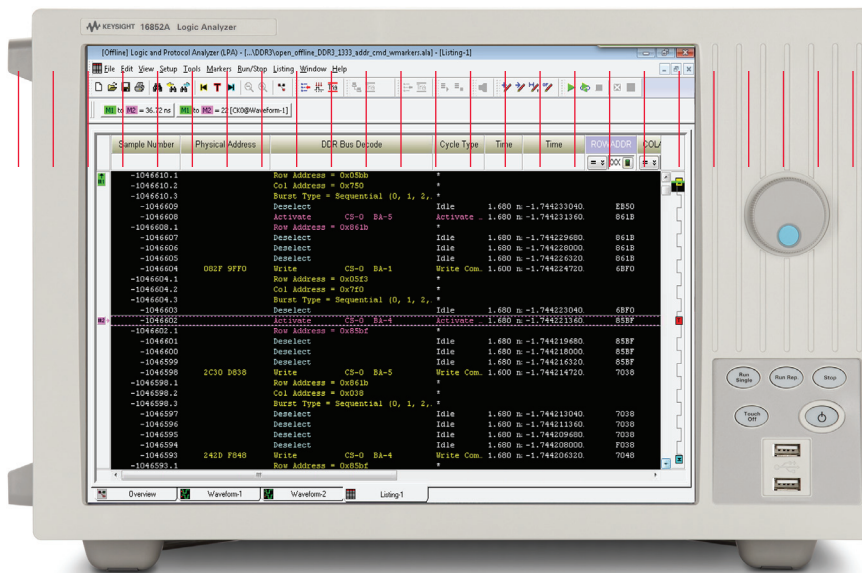


Keysight Technologies

Low-Cost DDR3 Decode and Analysis with the 16850 Series Portable Logic Analyzers

Application Note





Introduction

As embedded systems take on more sophisticated applications, they also require advanced external memory systems, such as DDR3, in order to offer adequate throughput. At times it can be helpful to see memory activity and perform some level of memory analysis in order to properly validate and debug a prototype system. New options now allow this at inexpensive price points compared to previous solutions. New general-purpose, low-cost logic analyzers, like the 16850 Series shown in Figure 1, offer the performance required for such measurements as well as related analysis tools to provide this kind of insight.

To support the goal of reducing the cost of these measurements, the DDR3 decoder in the solution has been modified to work from address and command signals only, thus reducing the total channel count necessary for meaningful measurements. For example, an entry-level 34-channel system can perform DDR3 1333 address and command state (synchronous) measurements and analysis for around \$36K. In the past, a logic analyzer solution that could offer these measurements and analysis required a budget of around \$100K.

This application note will outline how to make low-cost measurements on DDR3 interfaces and conduct performance analysis and compliance tests to evaluate these memory systems during debug and validation of a digital prototype.

Probing requirements for DDR3 measurements

In order to make real-time measurements on the interface between the DDR3 memory controller and memory devices, it is necessary to probe signals in a way that eliminates significant distortion and instead provides an accurate picture of those signals. A good probing option for designs with embedded memories is a BGA probe, as shown in Figure 2. Address, command, and data signals are intercepted and brought by coaxial ribbon cable to the logic analyzer. DDR3 BGA interposers contain a buried tip resistor to isolate the DRAM system from the logic analyzer probing. This probing scheme is workable to DDR3 rates of up to 2400 Mbit per second. This setup provides plenty of margin for the DDR3 1333 measurements made by the 16850 Series.

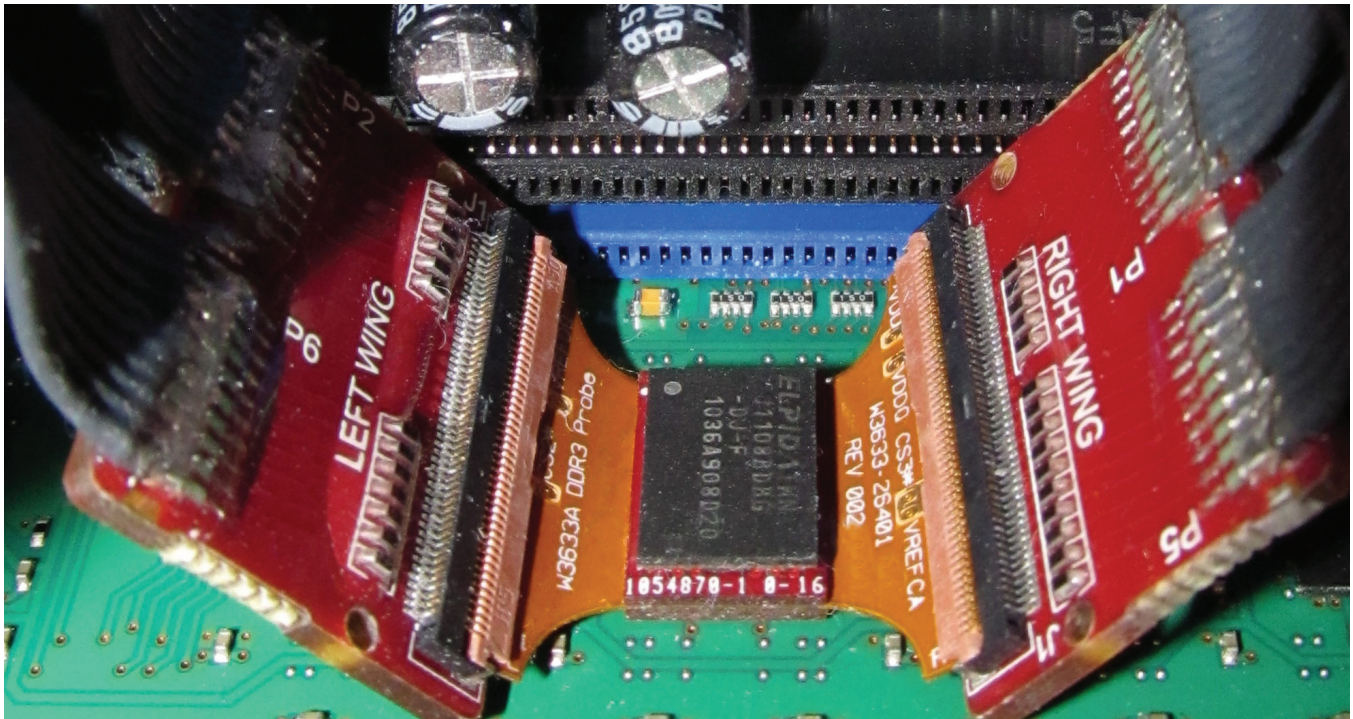


Figure 2. x8 DDR3 BGA probe connection.

Other probing options include the use of either a DIMM interposer or a mid-bus probe. Mid-bus probing involves placing connection pads or a connector somewhere along the PC board memory traces between the IC containing the memory controller and the memory ICs. A probe then touches those pads or it plugs into the connector to get access to the DDR3 signals.

DDR3 bus decode from address and command signals

One analysis tool that helps designers better understand how their external DDR3 memory is actually behaving is a memory decoder. This software takes raw acquired address and command state signals and converts them into a more easily understood format, as shown in Figure 4. Memory commands like “writes” and “reads” are displayed along with related chip select, bank address, row address, and column address information. Other commands like “activates” and “deselects” are shown. This state-mode trace capture is stored in deep memory so it reflects a significant amount of target activity time. The 16850 Series logic analyzers have a maximum input clock frequency of 700 MHz, which allows the state capture of 667 MHz address and command signals on DDR3 1333 memories.

Sample Number	Physical Address	DDR Bus Decode	Cycle Type	Time	Time	ROWADDR	COLADDR	A
-1046632		Deselect	Idle	1.760 n	-1.744271360	8400	000	
-1046631		Deselect	Idle	1.680 n	-1.744269680	8400	000	
-1046630		Deselect	Idle	1.600 n	-1.744268000	0400	000	
-1046629		Deselect	Idle	1.600 n	-1.744266480	0400	000	
-1046628		Deselect	Idle	1.680 n	-1.744264800	8400	000	
-1046627		Deselect	Idle	1.680 n	-1.744263120	8400	000	
-1046626		Deselect	Idle	1.760 n	-1.744261360	8400	000	
-1046625		Deselect	Idle	1.600 n	-1.744259760	8400	000	
-1046624		Activate CS-0 BA-7	Activate	1.680 n	-1.744258080	8613	213	
-1046624.1		Row Address = 0x8613	*					
-1046623		Deselect	Idle	1.680 n	-1.744256400	8613	213	
-1046622		Deselect	Idle	1.600 n	-1.744254800	8613	213	
-1046621		Deselect	Idle	1.680 n	-1.744253120	8613	213	
-1046620		Activate CS-0 BA-3	Activate	1.680 n	-1.744251440	05BB	1BB	
-1046620.1		Row Address = 0x05bb	*					
-1046619		Deselect	Idle	1.680 n	-1.744249760	85BB	1BB	
-1046618		Deselect	Idle	1.680 n	-1.744248080	85BB	1BB	
-1046617		Deselect	Idle	1.680 n	-1.744246400	85BB	1BB	
-1046616		Deselect	Idle	1.680 n	-1.744244720	85BB	1BB	
-1046615	3C3D 9808	Write CS-0 BA-7	Write Com...	1.680 n	-1.744243040	7008	008	
-1046615.1		Row Address = 0x8613	*					
-1046615.2		Col Address = 0x008	*					
-1046615.3		Burst Type = Sequential (0, 1, 2, ..	*					
-1046614		Activate CS-0 BA-1	Activate	1.680 n	-1.744241360	05F3	1F3	
-1046614.1		Row Address = 0x05f3	*					
-1046613		Deselect	Idle	1.680 n	-1.744239680	05F3	1F3	
-1046612		Deselect	Idle	1.680 n	-1.744238000	05F3	1F3	
-1046611		Deselect	Idle	1.600 n	-1.744236400	05F3	1F3	
-1046610	182D DF50	Write CS-0 BA-3	Write Com...	1.680 n	-1.744234720	6B50	750	
-1046610.1		Row Address = 0x05bb	*					
-1046610.2		Col Address = 0x750	*					
-1046610.3		Burst Type = Sequential (0, 1, 2, ..	*					

Figure 4. Memory decoder trace of DDR3 address and command lines.

Performance analysis

Although helpful, the typical deep-memory raw capture and related memory decoder output provide more information than can be easily evaluated manually by the logic analyzer user. But the DDR performance tool provides useful analysis by taking all the captured and decoded information and processing it into a variety of performance-oriented views. This valuable tool is one of four that are part of the B4622B protocol compliance and analysis toolset.

Now the specific steps are outlined to use the toolset:

From “Tools,” “External Applications,” select the “DDR Performance Tool,” as shown in Figure 5.

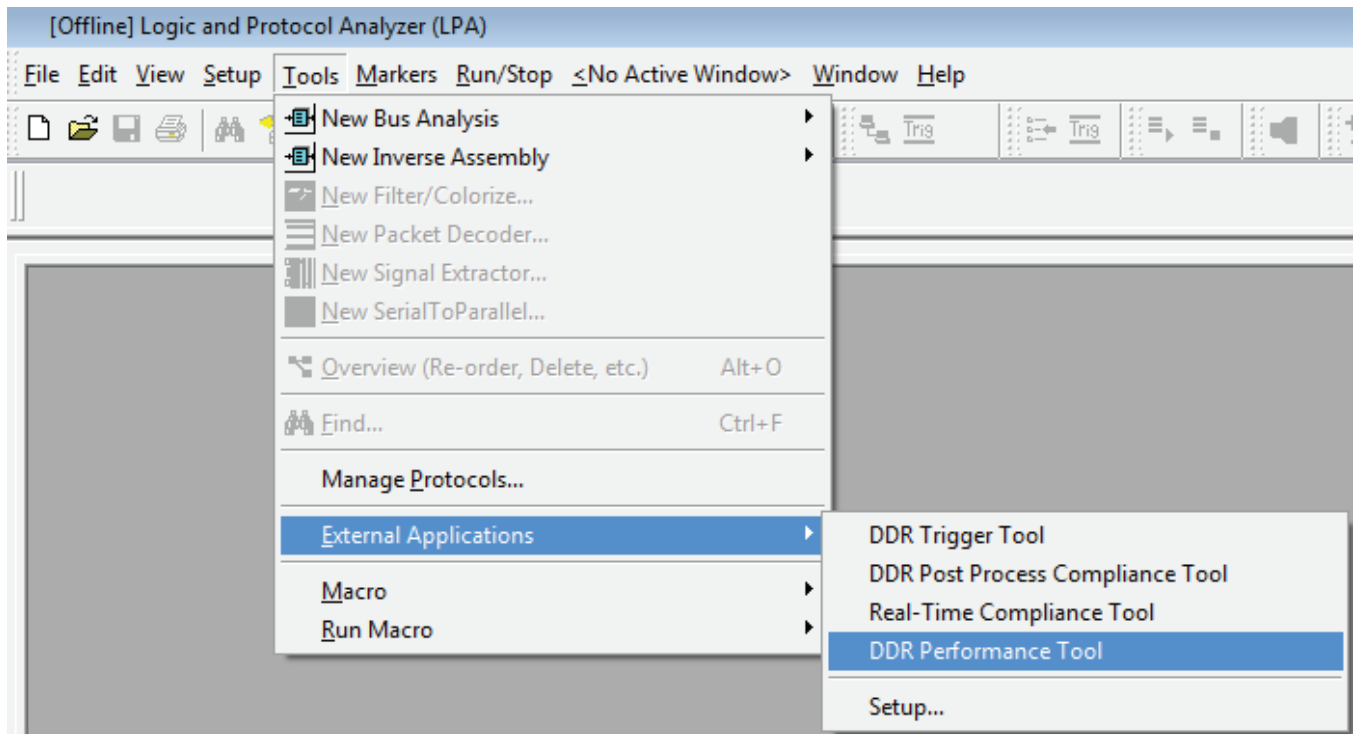


Figure 5. Launch of the DDR performance tool.

The configuration is using the DDR bus module called W3633A, the name of Keysight's DDR3 BGA probe used in this measurement.

Click "OK," as shown in Figure 6.

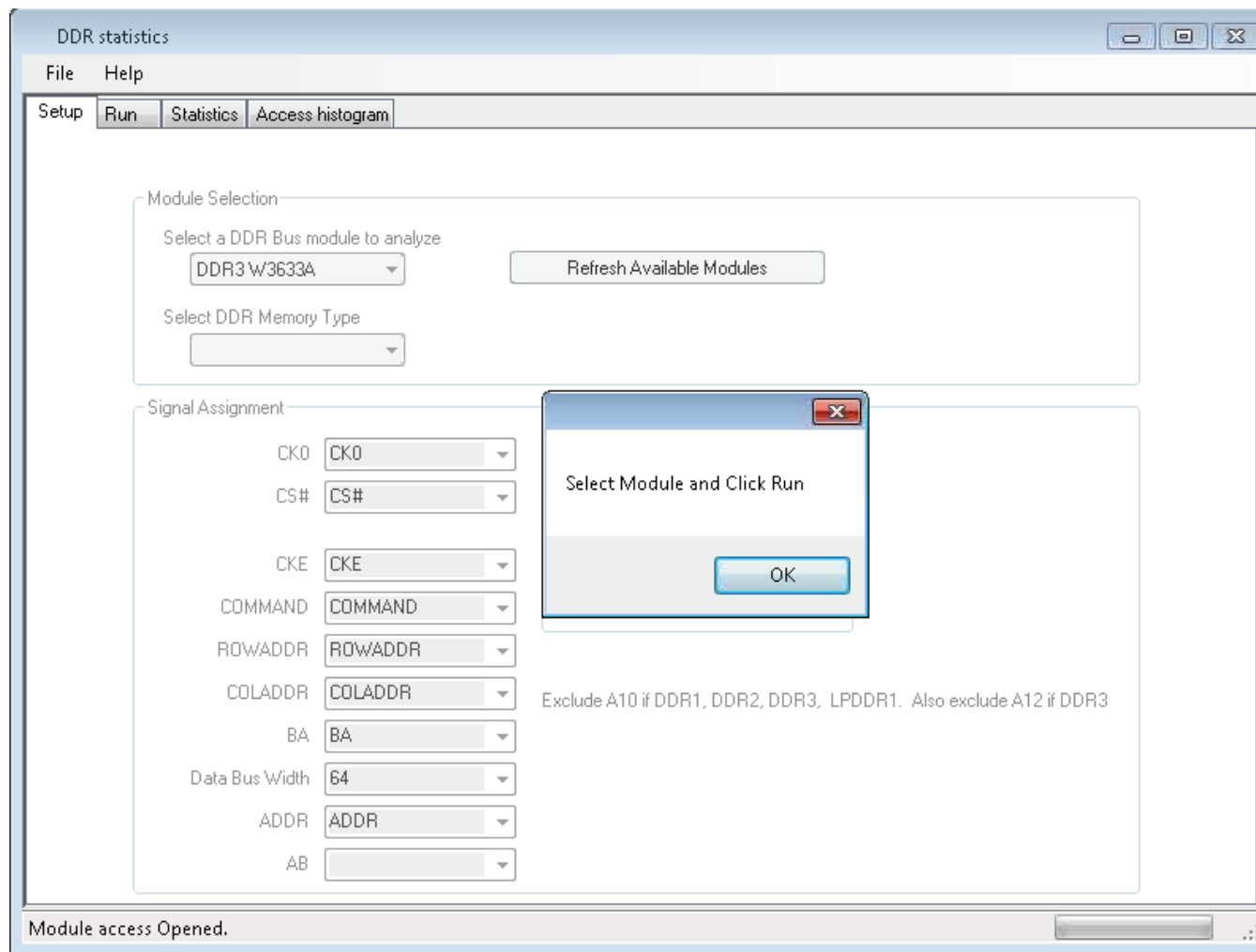


Figure 6. Select DDR bus module "DDR3W3633A," and press "OK".

Press the "Setup" tab, and note the settings from the configuration file shown in Figure 7.

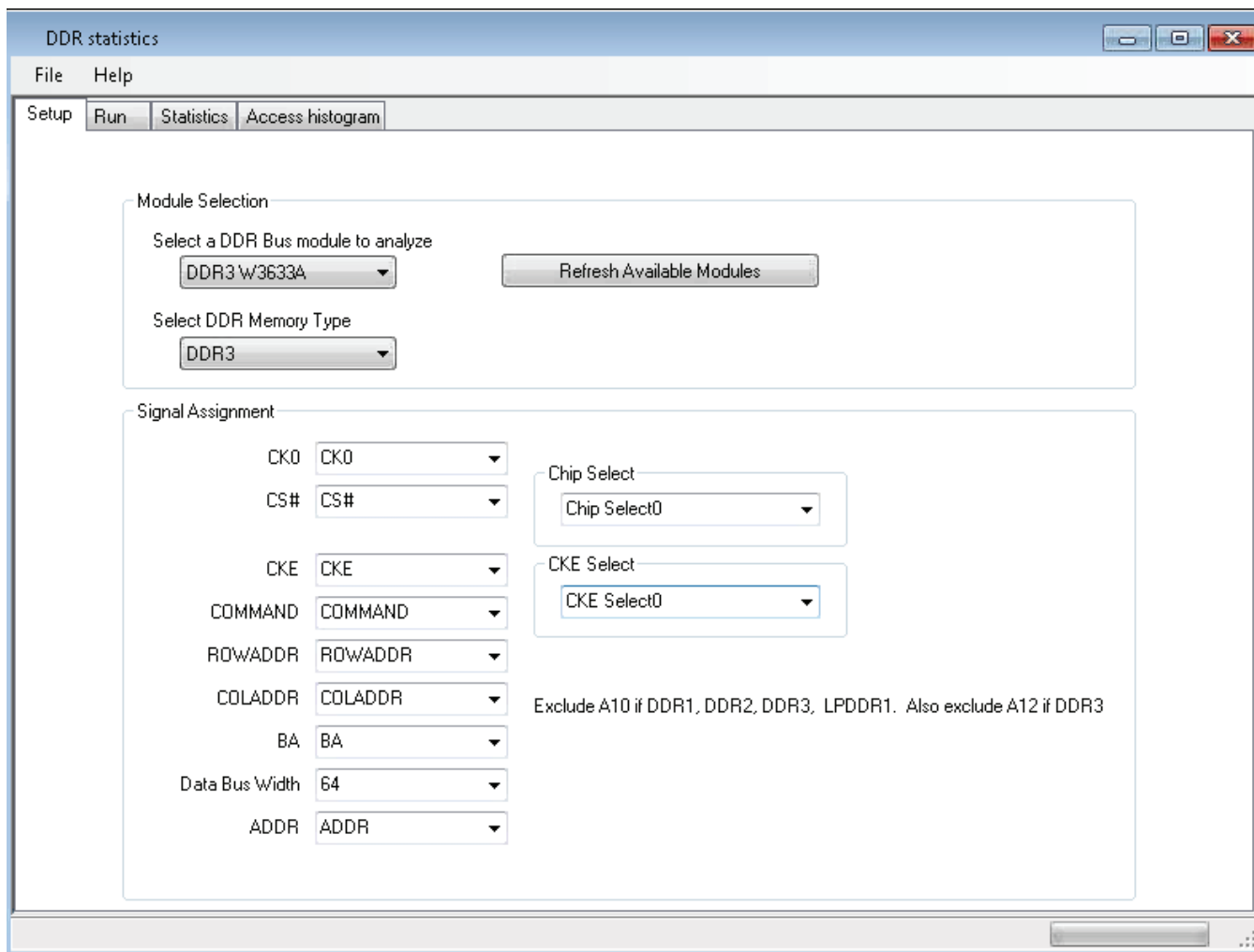


Figure 7. Setup for the DDR3 decoder.

Press the "Run" tab, and press the "Run" button, as shown in Figure 8.

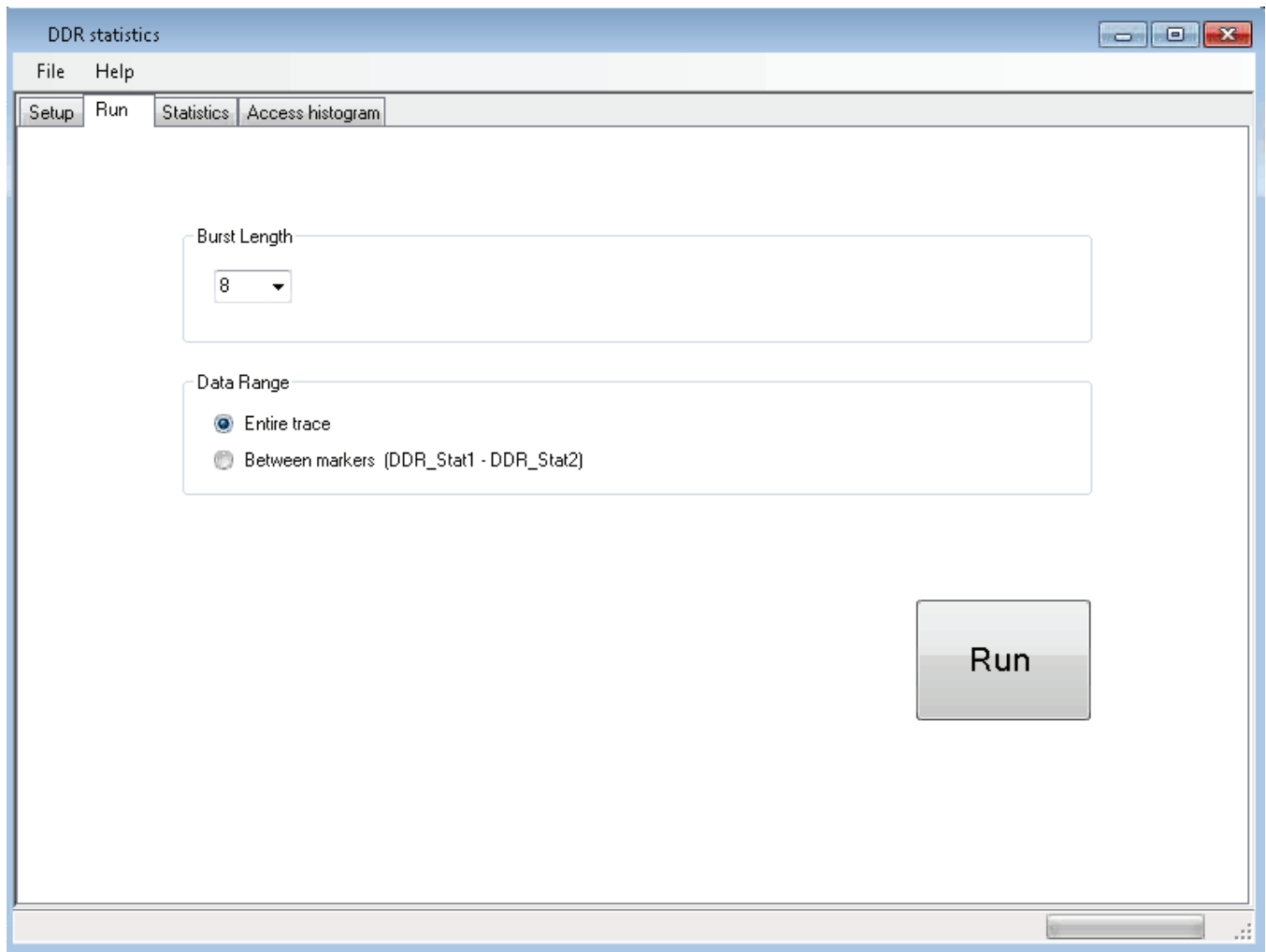


Figure 8. Choose default burst length equal to "8," use of the entire trace as the data range, and then press "Run".

Four examples of summary views from this first tool include the overview, refresh statistics, address histogram, and effective data rate, as seen in Figures 9-12.

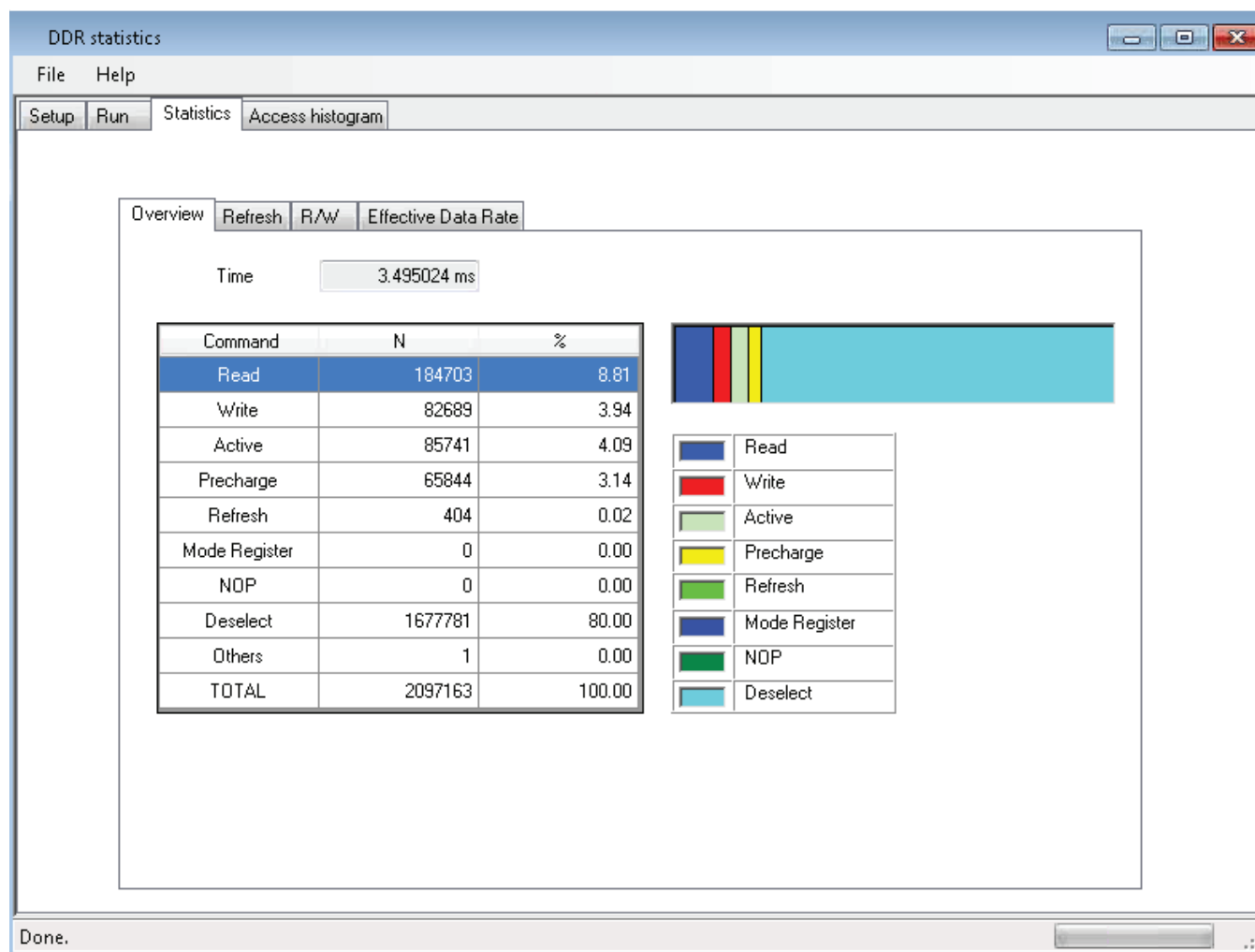


Figure 9. Performance tool analysis of command-type distribution.

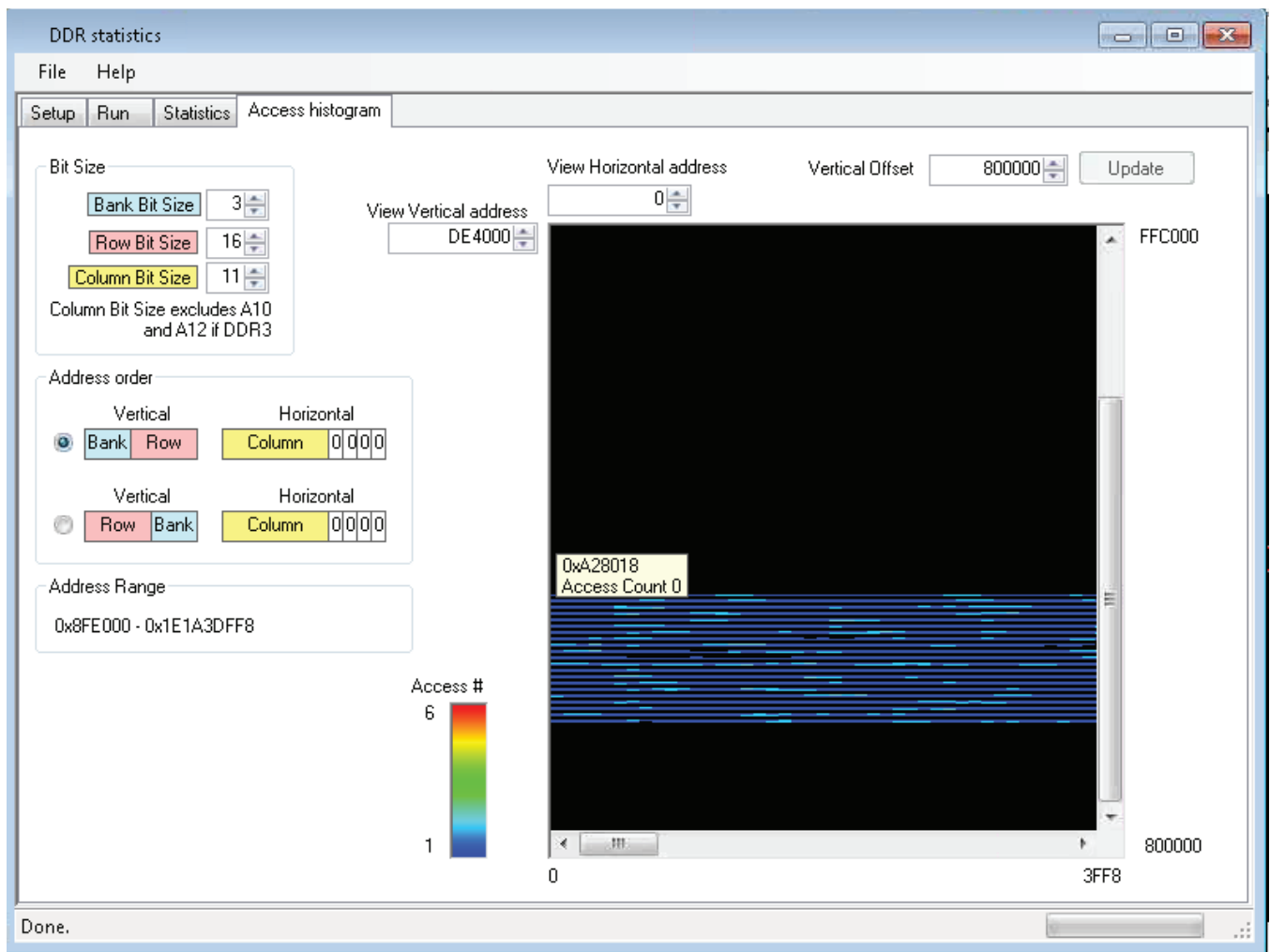


Figure 11. View of address space access distribution.

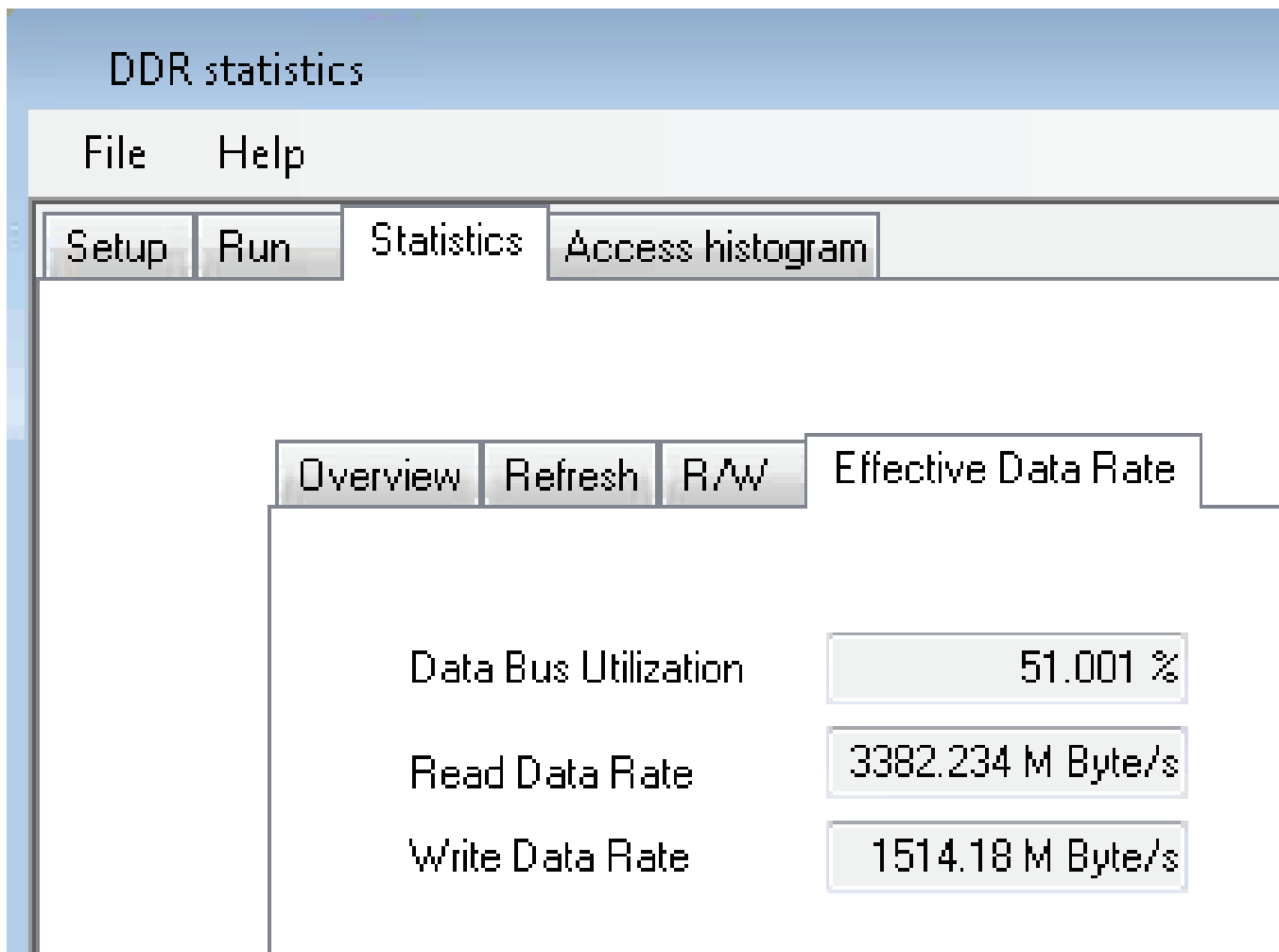


Figure 12. DDR performance tool view of effective data rate.

Expected memory command distributions can be verified with the “distribution view” of the performance analysis tool during particular modes of target operation. It is easy to see if the target system is spending too much time in memory “deselects,” for example.

A prototype might be working functionally but lack overall system throughput. A view of the read and write data rate can reveal a problem in the memory controller design. The overall efficiency factor can also indicate an issue. Here a 51% efficiency rate, although not necessarily bad, might not be adequate for the application. When it comes to using memory address space, the memory controller typically should spend very little time accessing a few memory locations and should spread those memory accesses over a range. The histogram view of the accessed memory space can reveal “hot spots” that can lead to premature memory failures.

Since the performance tool operates off of address and command signals, even a 34-channel model 16850 Series logic analyzer is adequate for the task, thus enabling a very low-cost option.

Memory compliance testing

Another type of memory evaluation that can be helpful during prototype turn-on is a test of compliance to the JEDEC specification. This evaluation can expose errors within a memory controller design. Non-compliance to the spec can result in data errors. A DDR post process compliance tool is available that also works from address and command memory signals saved in logic analyzer memory. The type of module is selected along with the type of memory being evaluated, its data rate, and the desired tests. With this information, a suite of evaluation parameters can be tested using the compliance tool.

Now the specific steps are outlined to perform compliance testing on the DDR3 memory system.

Launch the “DDR Post Process Compliance Tool” from “Tools,” “External Applications,” as shown in Figure 13.

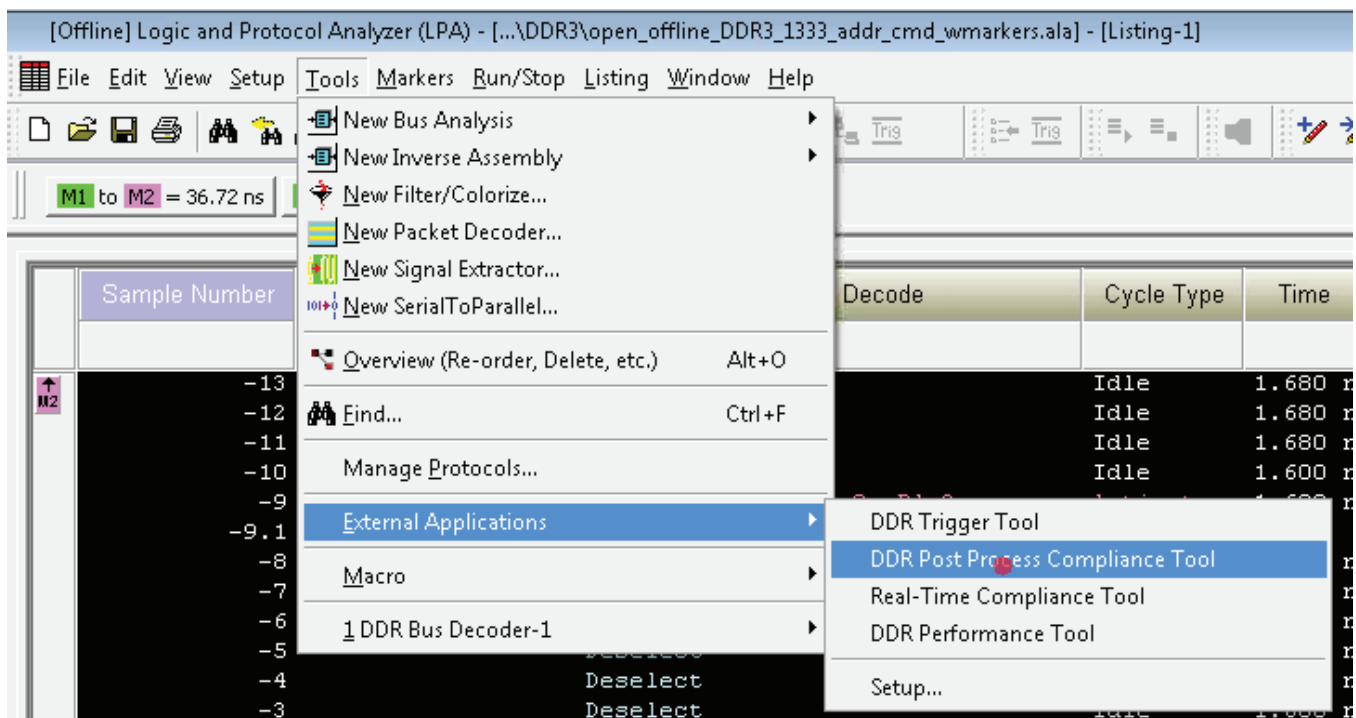


Figure 13. Launch the DDR post process compliance tool.

Then press the “Select Tests” tab and select all the JEDEC spec tests, as shown in Figure 14.

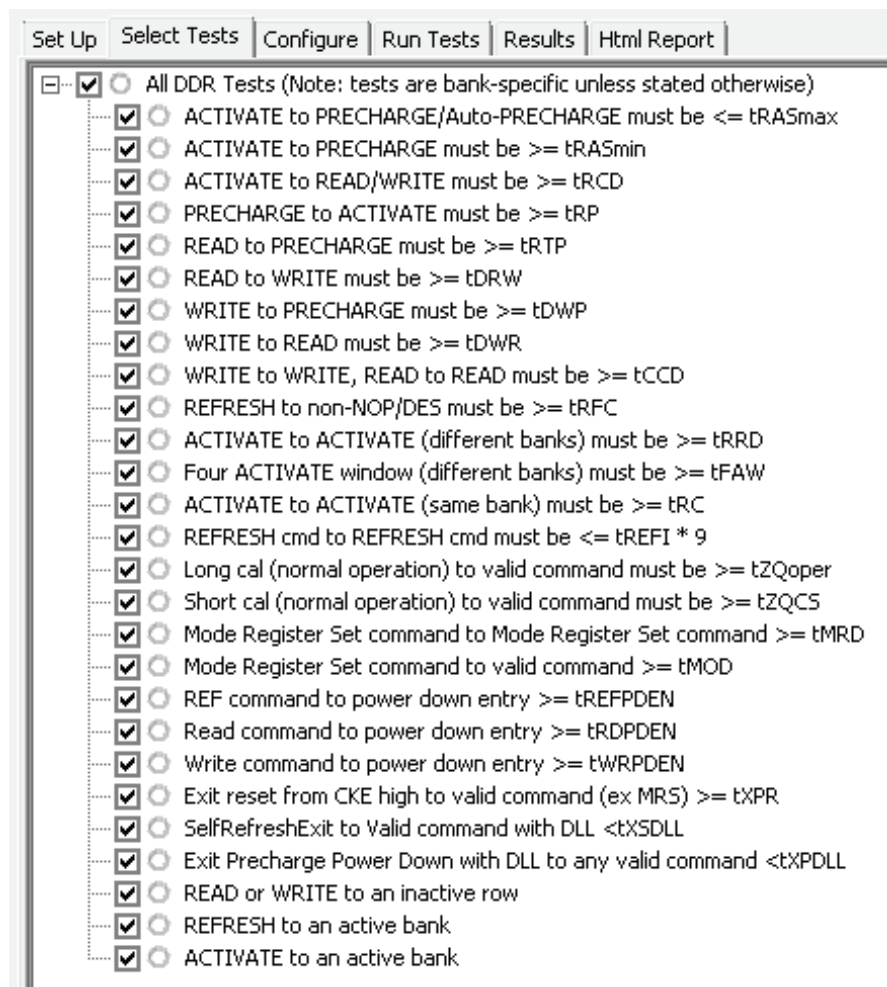


Figure 14. Select all memory compliance tests.

Press the “Configure” tab, “Activate/Refresh Limit Set,” and then select “DDR3_1333_2K_U4154,” as shown in Figure 15.

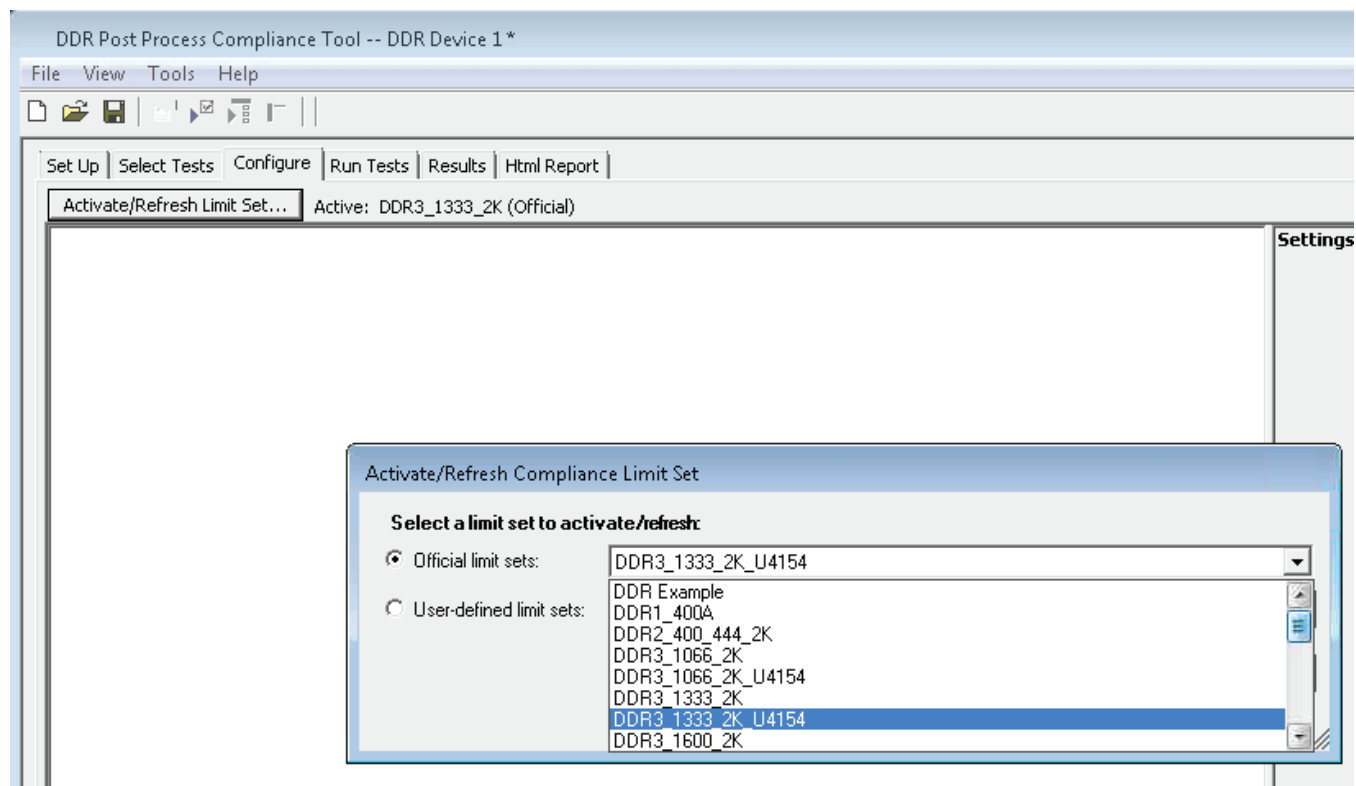


Figure 15. Select a limit set for the compliance tests of the DDR3 1333 memory.

Press the "Run Tests" tab and then the "Run" button, as shown in Figure 16.

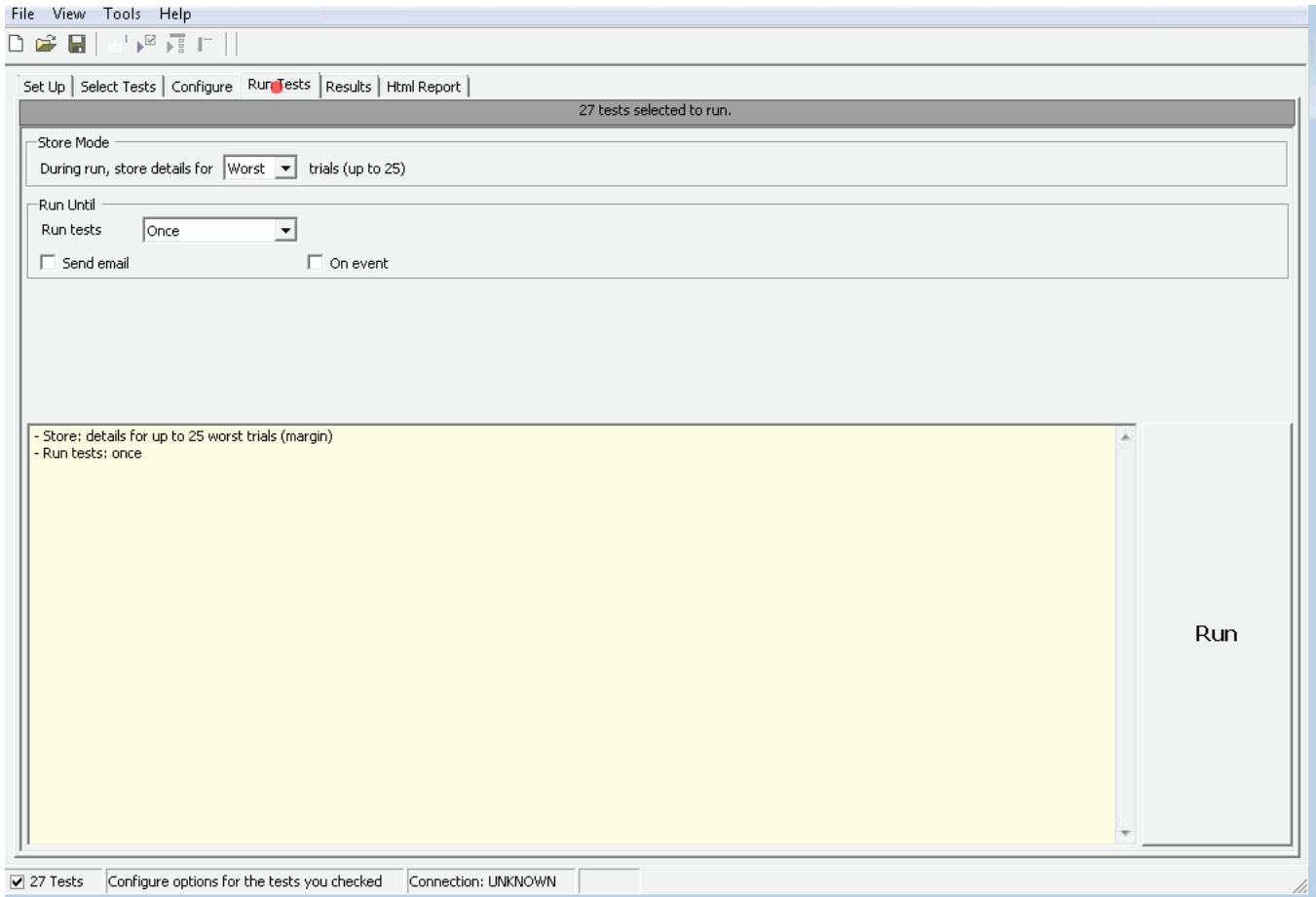


Figure 16. Select default settings to store details for the worst trials, and press "Run".

The results of such a test can be seen in Figure 17 where failures were discovered for the operation of four “activates” occurring from different banks of memory.

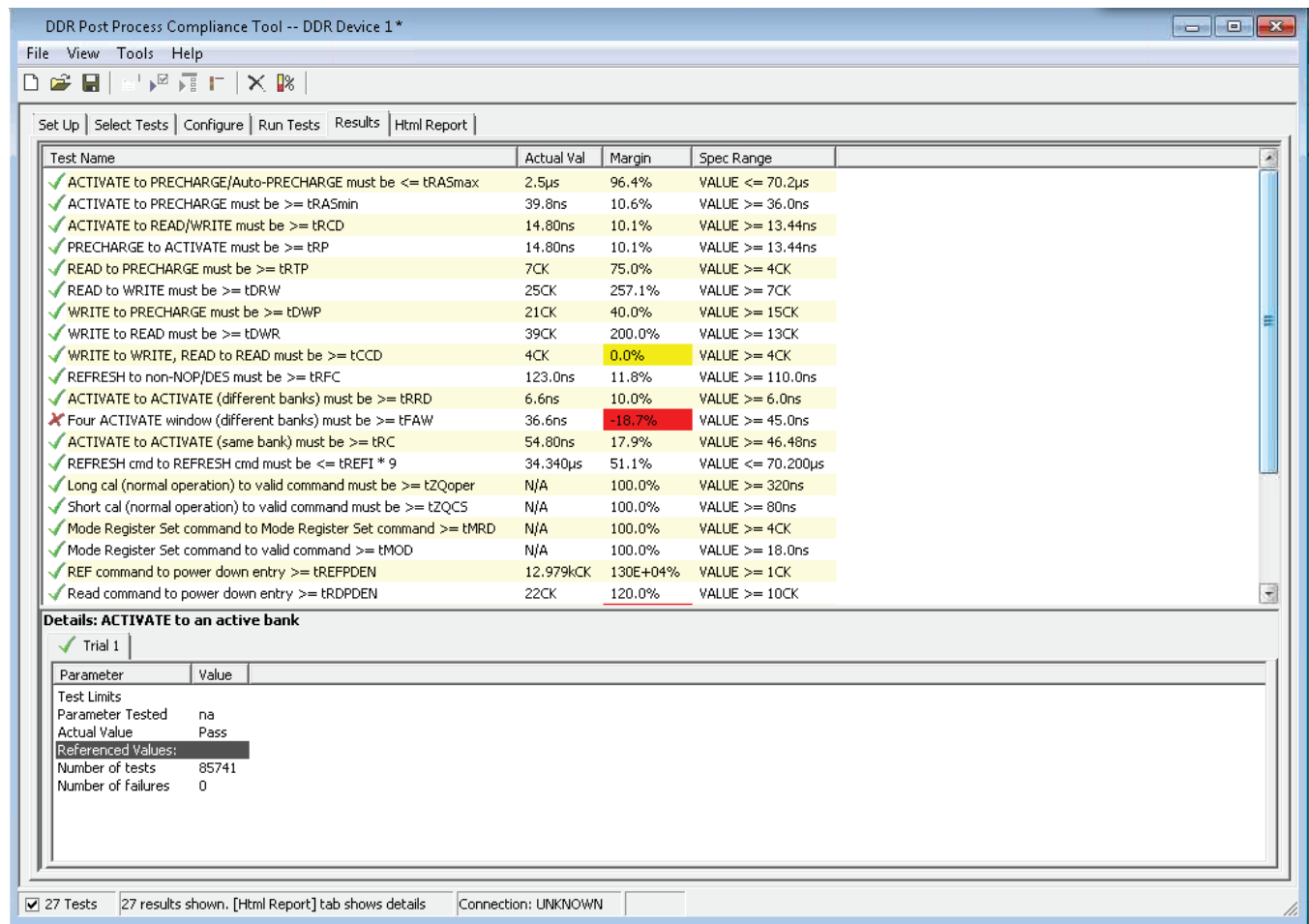


Figure 17. Memory compliance failure for four ACTIVATE windows (different banks) to be less than 45.0 ns.

By selecting the row that highlights an error, the interface displays the number of discovered errors in the trace compared to the total number of that particular operation that occurred in the trace. It also lists the first 25 exact state pairs associated with each error count in the deep memory trace. It is important not only to report that errors occur but also the specific locations of those errors so that a root cause of failure can be pursued. A real-time compliance tool also triggers the logic analyzer on a violation.

Timing-mode capture of address, command, and memory read and write data

The measurements so far have all been state (synchronous) capture, but timing (asynchronous) capture, including measurements on read and write data to track memory data flow, can also be useful. For the DDR3 1333 memory system being evaluated here, timing mode measurements require a timing sample rate that is fast enough to determine bus activity. A 3-to-1 ratio of logic analyzer sample rate to target system data rate is a good guideline to follow. For the 1333 data rate, this would translate to a 4 GHz or faster timing rate. The 16850 Series logic analyzers have a half-channel, 5-GHz timing speed that meets this requirement. A half-channel timing mode configuration is included with the analyzer for address, command, and data capture. An example capture is shown in Figure 18.

A 102-channel model is necessary to provide 48 channels in the half-channel mode so this measurement is able to capture address, command, and x8 or x16 data. Read and write data is not separated in timing capture, but settled data bus read and write values would still be seen in the DATA row with an expanded time/division setting. If the state capture of separate read and write data is required, a modular logic analyzer solution such as the U4154A offers a “dual sample mode” when in state capture mode that can accomplish this.

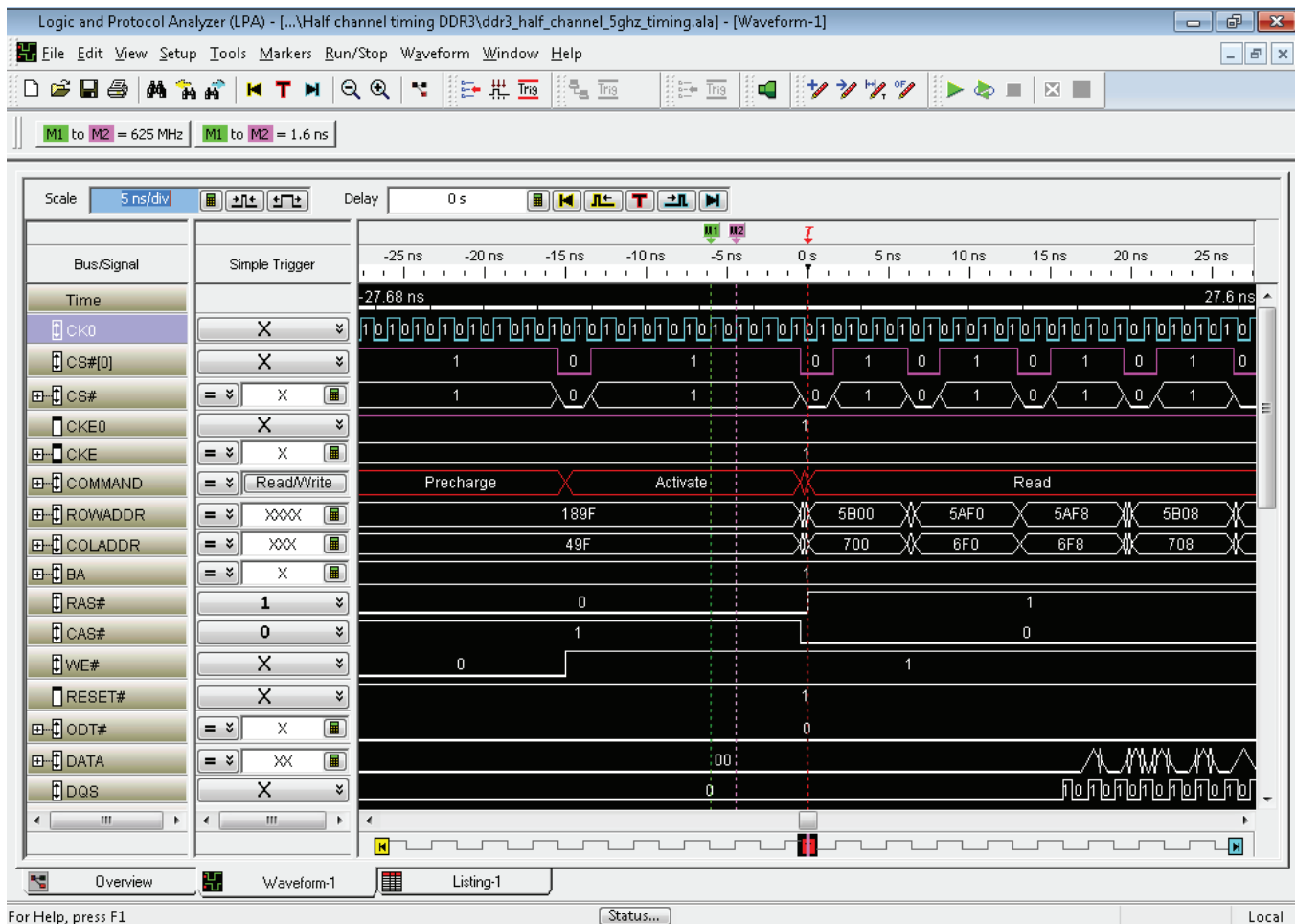


Figure 18. 5-GHz timing mode capture of DDR3 1333 address, command, and data

Positioning the 16850 Series portable logic analyzers with the modular U4154A analyzers

Both 16850 Series portable logic analyzers and the modular U4154A analyzers offer 2.5-GHz full-channel and 5-GHz half-channel timing measurements with deep memory. A comparison of timing and state mode capabilities is summarized in Figure 19 including use of the B4621B DDR decoder and the B4622B protocol compliance and analysis toolset.

Measurements	16850 Series portable (34-, 68-, 102-, and 136-channel models)	U4154A modular (136 channels per module)
Addr/Cmd state capture on DDR3 up to DDR3 1333 – including DDR decoder, protocol compliance and analysis toolset	Yes, up to DDR3 1333 (667 MHz clock, cmd, addr, requires 34-channel model with option 700 to increase max clock frequency to 700 MHz)	Yes, the U4154A can capture state data rates up to 4 Gb/s
Addr/Cmd state capture on DDR3 over DDR3 1333 – including DDR decoder, protocol compliance and analysis toolset	No	Yes, the U4154A can capture state data rates up to 4 Gb/s
Addr/Cmd/Data deep timing capture on DDR3 (no DDR decoder, no compliance and analysis toolset)	Yes, 5 GHz half channel* for up to DDR3 1600 x8 or x16, up to 256M sample depth (requires 102-channel model)	Yes, 5 GHz half channel* for up to DDR3 1600, up to 400M sample depth
Addr/Cmd/Data high-resolution “timing zoom” capture (simultaneous with normal state or timing capture from one probe point), 256k samples depth (no DDR decoder, no compliance and analysis toolset)	Yes, 12.5 GHz full channel (requires 68-channel model for x8 and x16 data width)	Yes, 12.5 GHz full channel
Addr/Cmd/data state capture on DDR2/3/4 and LPDDR2/3/4 – including DDR decoder, protocol compliance and analysis toolset	No (clock input limited to 700 MHz for state capture and cannot separate out DDR read and Writes for state capture and cannot demultiplex addr/cmd bus on LPDDR2/3)	Yes, the U4154A can capture data rates up to 4 Gb/s <i>Standard DDR3 probing covers data capture up to 2500 Mb/s. Data rates over 2500 require specialty probing</i> <i>As of Feb. 2014, DDR4 has been captured at data rates up to DDR4 2400. DDR4 is expected to achieve higher data rates in the future</i>

* Timing mode guideline is sample rate $\geq 3 \times$ data rate. 5-GHz sample rate allows viable timing captures up to DDR 1600. Decoders and compliance toolset are designed for state mode captures only.

Table 1. Comparison of 16850 Series portable logic analyzer and U4154A modular logic analyzer timing and state capture capabilities

State and timing measurement options and related probing requirements for 16850 Series analyzers

The state analysis capabilities of the 16850 Series allow it to make measurements and analysis on DDR2 and DDR3 memories up to DDR2/3 1333 (667 MHz clock) on address and control lines. Memory bus decode, compliance testing, and performance analysis are available in state mode only with related orderable tools. These options are outlined in Table 2. Timing analysis can be extended to memory data rates of 1600 Mbps by using half-channel, 5-GHz timing mode, but 102 channels are required to capture addr/cmd/x8-x16 data.

	DDR2 memory	DDR3 memory
Addr/Cmd only	Up to DDR2 1333 (667 MHz clock) state measurements on Addr/Cmd only. (No Data)	Up to DDR3 1333 (667 MHz clock) state measurements on Addr/Cmd only. (No Data)
	Requires 34 channel model or higher (one U4201A cable required providing two 90 pin pods)	
	Related Orderable SW Tools (State mode only):	
	B4621B Bus Decoder for DDR, DDR2, DDR3, DDR4 Debug and Validation (Only DDR2 and DDR3 are supported with the 16850 Series logic analyzer.)	
	B4622B Protocol Compliance and Analysis Toolset for DDR/2/3/4, and LPDDR/2/3 (Only DDR2 and DDR3 are supported with the 16850 Series logic analyzer.)	
	Supported probes with configuration files:	Supported probes with configuration files:
	x16 Addr/Cmd/Data DDR2 BGA probe (W2631B)(Requires E5384A ZIF probe) ¹	x16 Addr/Cmd/Data DDR3 BGA probe (W3631A)(Requires E5845A ZIF probe) ¹
	x8 Addr/Cmd/Data DDR2 BGA probe (W2633B)(Requires E5384A ZIF probe) ¹	x8 Addr/Cmd/Data DDR3 BGA probe (W3633A) (Requires E5847A ZIF probe) ¹
		FS2372 DDR3 DIMM interposer (Addr/Cmd only)
		FS2374 DDR3 SODIMM interposer (Addr/Cmd only)
Addr/Cmd/Data	Up to DDR2 800 (400 MHz clock) timing measurements using 2.5 GHz timing analyzer with deep memory (for 3:1 ratio of sample rate to data rate)	Up to DDR3 800 (400 MHz clock) timing measurements using 2.5 GHz timing analyzer with deep memory (for 3:1 ratio of sample rate to data rate)
	Requires 68 channel model or higher (two U4201A cables using three of the four 90 pin pods provided)	
	Supported probes with configuration files:	Supported probes with configuration files:
	x16 Addr/Cmd/Data DDR2 BGA probe (W2631B)(Requires E5384A ZIF probe)	x16 Addr/Cmd/Data DDR3 BGA probe (W3631A)(Requires E5845A ZIF probe)
	x8 Addr/Cmd/Data DDR2 BGA probe (W2633B)(Requires E5384A ZIF probe)	x8 Addr/Cmd/Data DDR3 BGA probe (W3633A) (Requires E5847A ZIF probe)

For higher speed memory analysis or greater channel count refer to the U4154A logic analyzer module.

Data pod is not connected for state measurements when used with the 16850 Series. Simultaneous state mode capture of read and write data requires a U4154A high-performance logic analyzer module with dual sample mode. The W3631A was designed to work with stacked DRAM under 2G bytes depth and brings out two CS and two ODT signals. An alternate probe, the W3636A, was designed for non-stacked DRAM of any depth, and brings out one CS, one ODT signal, and BA2 and A15. Refer to the W3630A Series BGA probe data sheet (publication number 5990-3179EN) for more details.

Table 2. Options for state and timing capture of DDR2/3 with the 16850 Series logic analyzers.

Summary

It is now possible to capture DDR3 1333 address and command signals with a low-cost, 34-channel general purpose portable logic analyzer in state (synchronous) mode and conduct memory decode, performance analysis, and compliance testing to help validate and debug digital designs. By using the 5-GHz half-channel timing mode with a 102-channel analyzer, waveforms of DDR3 1600 address, command, and x8 / x16 data signals from a DRAM can be viewed to help with overall system evaluation. Memory depth can be as high as 256M samples. The 12.5-GHz “timing zoom” timing capture can also be used for such measurements and only requires a 68-channel model analyzer to do so, however memory depth is limited to 256k samples. Although DDR decode of the DDR3 traffic is not supported in timing mode and performance analysis and compliance testing is not available in this mode, valuable debugging insight is provided by viewing the timing waveforms.

Modular analyzers (U4154A) are available for state capture on faster memories with higher data rates (up to 4G bit per second), including DDR3/4 and LPDDR2/3/4 memories. They also provide the capture and separation of memory read and write data and include DDR memory decode, performance analysis, and compliance testing.

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