Keysight M8195A
65 GSa/s Arbitrary Waveform Generator

Data Sheet
Version 1.0

M8195A Rev. 2 in a 2-slot AXIe chassis

M8195A Rev. 1, front panel view

KEYSIGHT TECHNOLOGIES

M8195A at a Glance

The M8195A is a new **arbitrary waveform generator** with highest combination of sample rate, bandwidth and channel density

- Sample rate up to 65 GSa/s (on up to 4 channels)
- Analog bandwidth: 20 GHz
- 8 bits vertical resolution
- Up to 16 GSa of waveform memory per AXIe module[1]
- 1, 2 or 4 differential channels per 1-slot high AXIe module (number of channels is software upgradeable)
- Multi-module synchronization up to 16 channels per 5-slot AXIe chassis[1]
- Advanced 3-level sequencing with external dynamic control[1]
- Load new waveforms on-the-fly without interrupting the playback of the previous one[1] (“memory ping-pong”)
- Amplitude up to 1 $_{Vpp(se)}$ (2 $V_{pp(diff.)}$), voltage window -1.0 ... +3.3V
- t_{rise}/fall 20%/80% < 18 ps (typ)
- Ultra low intrinsic jitter (RJ_{rms} < 200 fs @ 32 Gb/s PRBS 2^{11}-1)
- Built-in frequency and phase response calibrationBuilt-in frequency and phase response calibration for clean output signals
- 16-tap FIR filter in hardware for frequency response compensation[1]
- Precise trigger[1]
- Up to 2 markers with 1 sample resolution[1] (markers don’t reduce vertical resolution)

Go where you have never been able to test before: in speed, in bandwidth and in channel density – explore your possibilities

Key Applications

As devices and interfaces become faster and more complex, the M8195A AWG gives you the versatility to create the signals you need for digital applications, optical and electrical communication, advanced research, wideband radar and satcom.

- **Coherent optical** – a single M8195A module can generate 2 independent I/Q baseband signals (dual polarization = 4 channels) at up to 32 GBaud and beyond
- **Multi-level / Multi-channel digital signals** – generate NRZ, PAM4, PAM8, DMT, etc. signals at up to 32 Gbaud.
  Embed/De-embed channels, add Jitter, ISI, noise and other distortions.
- **Physics, chemistry and electronics research** – generate any mathematically defined arbitrary waveforms, ultra-short yet precise pulses and extremely wideband chirps
- **Wideband RF/µW** – generate extremely wideband RF signals with an instantaneous bandwidth of DC to 20 GHz for aerospace/defense/communication applications

Coherent optical applications

The M8195A supports leading edge research for 100 Gb/s, 400 Gb/s and 1 Tb/s optical transmission systems that require a very wideband electrical stimulus with a variety of complex modulation formats from **QPSK** to **nQAM** to **OFDM** at symbol rates up to 32 GBaud and beyond.

In order to drive dual-polarization systems, the M8195A has **4 independent, yet precisely synchronized analog output channels in a single module.** Since all 4 channels are generated by the same instrument without any external circuitry, precise synchronization down to the femto-second-range can be achieved and maintained.

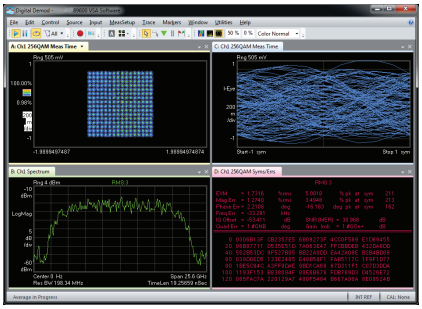


Figure 1: 256QAM @ 16 GBaud.

1. Available with M8195A Rev. 2

The M8195A uses digital pre-distortion techniques for frequency- and phase response compensation of the AWG output and any external circuits is required in order to achieve a **clean signal at the device under test.**

Distortions generated by cables, amplifiers, etc. can also be compensated by embedding / de-embedding the S-parameters of the respective circuits or by performing an “in-situ” calibration using the Keysight Vector Signal Analysis software.

The M8195A is suited very well to address those challenging requirements. With up to 4 channels per 1-slot AXIe module, each running at up to 65 GSa/s with 20 GHz of analog bandwidth in combination with advanced frequency response calibration techniques, it can generate clean as well as purposely distorted signals.

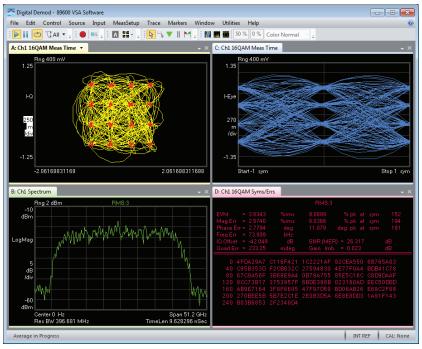


Figure 2: 16QAM @ 32 GBaud.

Multi-level / multi-channel digital signals

Increasing the data throughput on digital interfaces has traditionally been accomplished by increasing the data rate or by increasing the number of parallel signals. However, at a certain point, it is more cost-effective to consider multi-level signaling techniques. Examples are high-speed backplane connections using PAM4 or PAM8, but also technologies in the mobile application space.

The M8195A is ideally suited to address those multi-level / multi-channel interfaces using any standard or custom data format. The flexibility of the waveform generation at highest speeds, combined with excellent intrinsic jitter performance makes the M8195A a truly future proof instrument – independent in which direction the technology is moving.

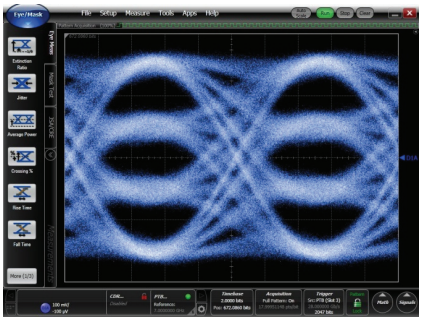


Figure 3: 4 PAM4 signal at 28 GBaud (= 56 Gbit/s).

At data rates of multiple Gb/s, the effect of cables, board traces, connectors etc. have to be taken into account in order to generate the desired signal at the test point of the device under test. The M8195A incorporates digital pre-distortion techniques for frequency- and phase response compensation of the AWG output and any external circuit to generate the desired signal **at the device under test.** Channels can be embedded / de-embedded if the S-Parameters of the respective circuits are provided.

Figure 4: 32 Gb/s PRBS 211-1 showing 138 fs RJ(rms).

With up to 4 differential output channels per 1-slot AXIe module and the ability to synchronize multiple modules, the M8195A is well-suited to stimulate multi-lane high-speed interfaces in a very economic fashion.

With the planned integration of the M8195A AWG into the M8000 Series of BER test solutions, Keysight allows you to address your high-speed digital receiver test needs with a common software platform and choose the BERT or AWG that best meets your needs.

Physics, chemistry and electronics research

Generate any arbitrary waveform you can mathematically describe e.g. in MATLAB and download it directly to the M8195A. This includes ultra-short yet precise pulses down to ~100 ps pulse width or extremely short, yet wideband RF pulses and chirps.

In conjunction with the M8197A synchronization module, these signals can be triggered from external sources with very low jitter.

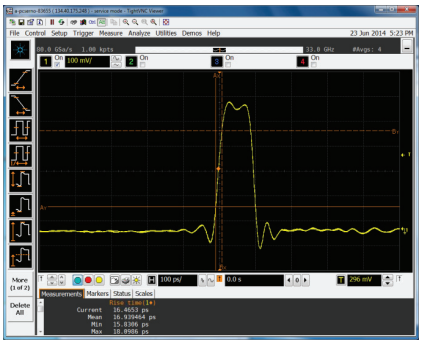


Figure 5: 100 ps pulse with 17 ps risetime

Wideband RF/uW signals

The M8195A can address wideband wireless, EW and Comms/Satcom applications where extremely wide instantaneous bandwidth (DC to 20 GHz) and fast frequency hopping are critical parameters.

With built-in frequency and phase calibration, it is straight forward to generate wideband multi-tone signals with a flat frequency response up to 20 GHz.

Wideband Wireless signals with any modulation scheme (e.g. nPSK, nQAM, APSK, OFDM, etc.) can be generated directly at carrier frequencies of up to 20 GHz. In many cases, this saves an additional up-conversion stage (e.g. in case of IEEE 802.11ad) or enables waveform generation directly at the carrier frequency.

Note that the available frequency range depends on the number of channels that are used simultaneously as well as the amount of memory per channel (see sample memory modes below).

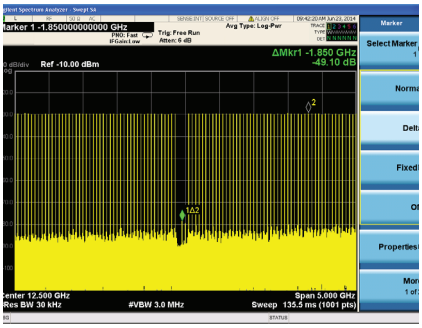


Figure 6: Multi-tone signal from 10 GHz to 15 GHz.

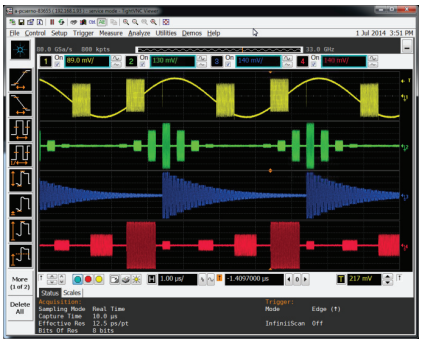


Figure 7: Four different pulsed signals up to 20 GHz.

Software

The basic functionality of the M8195A is controlled from a “Soft Front Panel” application running on the AXIe embedded controller or external PC or laptop. In addition to basic settings such as sample clock rate, output amplitudes, etc., the Soft Front Panel offers functionality to

- Load waveforms from files
- Generate standard waveforms (sine, square, etc.)
- Generate multi-tone waveforms
- Generate complex modulated waveforms (nPSK, nQAM, etc.)
- Generate binary and multi-level digital waveforms

In addition to the Soft Front Panel, the M8195A can be controlled via **SCPI** and **IVI-COM** remote programming interfaces.

External Software Applications that can be used to generate and download waveforms directly to the M8195A via SCPI or IVI-COM include MATLAB, LabView, C++, C# or any other .NET language

In addition, the M8195A integration into the following software applications is planned:

- M8070A – System Software for M8000 Series of BER Test Solutions
- M9099A – Waveform Creator Application Software
- W146xA – SystemVue Electronic System-Level Design Software

Configuration

The M8195A will be released in two phases, referred to as **"Rev 1"** and **"Rev 2"** in this document. Both product revisions are described in this datasheet. Differences between the Revisions are clearly marked in the "Specification" section below.

Customers can purchase the Rev 1 product to get an earlier delivery plus an upgrade to Rev 2. With the upgrade (Opt. U12 resp. U14, see below), the Rev 1 product will be replaced, once Rev 2 is available.

For **Rev 1,** the following products/options are available:

Product Number	Description	Comment
M8195A-R12	2 channel, 65 GSa/s AWG, 256 KSa per channel (Rev 1)	Must choose ONE of R12 or R14
M8195A-R14	4 channel, 65 GSa/s AWG, 256 KSa per channel (Rev 1)	
M8195A-U12	Upgrade from Rev 1 to Rev 2 for M8195A-R12	Hardware exchange
M8195A-U14	Upgrade from Rev 1 to Rev 2 for M8195A-R14	Hardware exchange

For **Rev 2,** the following products/options are available. Rev. 2 products can be ordered but will only be delivered after Rev 2 has been released.

Product Number	Description	Comment
M8195A-001	1 channel, 65 GSa/s, 2 GSa per module (Rev 2)	Must choose ONE of 001, 002 or 004
M8195A-002	2 channel, 65 GSa/s, 2 GSa per module (Rev 2)	
M8195A-004	4 channel, 65 GSa/s, 2 GSa per module (Rev 2)	
M8195A-16G	Upgrade to 16 GSa per module (Rev 2)	Software license
M8195A-SEQ	Sequencer functionality (Rev 2)	Software license
M8195A-FSW	Fast Switching (Rev 2)	Software license
M8195A-1A7	ISO 17025 report (Rev 2)	Document
M8195A-Z54	Z54 calibration report (Rev 2)	Document
M8195A-U02	Upgrade from 1 ch. to 2 ch. (Rev 2)	Software license
M8195A-U04	Upgrade from 2 ch. to 4 ch. (Rev 2)	Software license
M8197A	Synchronization Module for up to four M8195A modules (= 16 channels) per AXIe 5-slot chassis (Rev 2)	Required for multi-module operation
N6171A-M01	MATLAB license (basic)	Software license
N6171A-M02	MATLAB license (standard)	Software license
N6171A-M03	MATLAB license (extended)	Software license

In order to be operational, an **AXI chassis** plus either an embedded controller or external PC or laptop are required in addition to one or more M8195A/M8197A modules:
(See http://www.agilent.com/find/AXIe for more details)

Product Number	Description	Comment
M9502A-U20	2 slot AXIe chassis with USB Option	Choose 2-slot OR 5-slot chassis
M9505A-U20	5 slot AXIe chassis with USB Option	
M9536A	AXIe embedded controller	Choose either M9536A *or* M9048A+Y1202A *or* M9045B+Y1200B
M9048A	PCIe desktop card adapter Gen 2 x8	
Y1202A	PCIe cable for M9048A desktop adapter	
M9045B	PCIe laptop card adapter Gen 1 x4	
Y1200B	PCIe cable for M9045B laptop adapter	

For a “system” configuration that is dynamically configured based on the required number of channels, including AXIe chassis, embedded controller or external PC connectivity, please use the following product:

Product Number	Description	Comment
M8195S	M8195A system bundle, dynamically configured depending on the required number of channels. AXIe chassis, embedded controller or PC connectivity will automatically be added and the system is shipped pre-configured	

Specifications

General Characteristics

Sample Rate	54 GSa/s to 65 GSa/s
DAC resolution	8 bits
Number of channels per M8195A module	
Rev 1	2 or 4 (corresponds to Opt. R12 resp. R14)
Rev 2	1, 2 or 4 (corresponds to Opt. 001, 002, 004) Number of channels is software upgradable via license key

Sample Memory

Internal sample memory (Rev 1 + 2)	256 KSa per channel
Extended sample memory (Rev 2 only)	2 GSa per M8195A module (standard) 16 GSa per M8195A module (with Option 16G) (for modes of operation see table below)

Sample Memory Modes Rev 1

Mode	Available with Option	Sample Memory (standard)	Sample Memory (with Opt. 16G)	Max. Sample Rate	Interpolation	Max. output frequency	Analog BW (typ) (3 dB)
2 ch, int.mem.	R12, R14	256 KSa per ch.	Not available	65 GSa/s	none	> 20 GHz	20 GHz
4 ch, int.mem.	R14	256 KSa per ch.	Not available	65 GSa/s	none	> 20 GHz	20 GHz
Note: In Rev. 1, the waveforms in all channels have to be the same length							

Sample Memory Modes Rev 2

Mode	Available with Option	Sample Memory (standard)	Sample Memory (with Opt. 16G)	Max. Sample Rate	Interpolation (*)	Max. output frequency	Analog BW (typ) (3 dB)
1 ch, ext.mem.	001, 002, 004	2 GSa	16 GSa	65 GSa/s	None	> 20 GHz	20 GHz
2 ch, ext.mem.	002, 004	1 GSa per ch.	8 GSa per ch.	32.5 GSa/s	2 x	12.8 GHz	20 GHz
2 ch, int.mem.	002, 004	256 KSa per ch.	256 KSa per ch.	65 GSa/s	None	> 20 GHz	20 GHz
4 ch, ext.mem.	004	0.5 GSa per ch.	4 GSa per ch.	16.25 GSa/s	4 x	6.4 GHz	20 GHz
4 ch, int.mem.	004	256 KSa per ch.	256 KSa per ch.	65 GSa/s	None	> 20 GHz	20 GHz

(*) Interpolation is performed by FIR filters in hardware.
For 2x (4x) interpolation, samples are read from memory at a rate up to 32.5 GSa/s (16.25 GSa/s) and interpolated to a DAC sample rate of up to 65 GSa/s. The maximum output frequency is calculated as 80% of Nyquist. For Interpolation = None, the sample rate from memory is the same as the DAC sample rate

Frequency Switching Characteristics (Rev 2 Only)

Effective Frequency Switching Time[1]	
with option -FSW	38 ps
without option -FSW	> 505 µs

1. Effective switching frequency is determined as $1 / f_{max}$, with $f_{max} = f_{Sa(max)} / 2.5$

Out 1, 2, 3, 4

Output type	Single ended[2] or differential
Bandwidth (3 dB, excl. sin(x)/x roll-off)	20 GHz
Rise/Fall time[3] (20%/80%)	18 ps (typ)
Impedance	50 Ω (nom)
Amplitude	250 $mV_{pp(se)}$ to 1 $V_{pp(se)}$ into 50 Ω 500 $mV_{pp(diff.)}$ to 2 $V_{pp(diff.)}$ into 50 Ω
Amplitude resolution	400 µV (nom.)
DC amplitude accuracy[3]	±(2.5% +10 mV) (typ)
Voltage window (Rev. 1)	-550 mV to +550 mV single-ended into 50 Ω
Voltage window (Rev. 2)	-1.0 V to +3.3 V single-ended into 50 Ω
Offset resolution	400 µV (nom.)
DC offset accuracy[4]	± 20 mV (typ)
Differential offset (Rev. 2 only)	Adjustable
Termination voltage (Rev. 1)	0 V fixed
Termination voltage window (Rev. 2)	-1.5 V to + 3.5 V (Low level – 500 mV) to (High Level + 500mV)
Termination voltage resolution	300 µV (nom.)
Skew between any pair of outputs	0 ps ± 5 ps (typ)
Skew between normal and complement	0 ps ± 1 ps (nom)
Harmonic distortions[5,6]	
2nd Harmonic	-45 dBc (typ), f_{out} < 3 GHz -35 dBc (typ), f_{out} = 3 GHz... 8GHz -30 dBc (typ), f_{out} > 8 GHz
3rd Harmonic	-35 dBc (typ), f_{out} < 2 GHz -30 dBc (typ), f_{out} > 2 GHz
Two-Tone IMD[5]	-42 dBc (typ), f_{out1} = 990 MHz, f_{out2} = 1010 MHz
SFDR[5] (excluding harmonic distortions)	
In-band	-80 dBc (typ), f_{out} = 100 MHz, measured DC to 1 GHz -70 dBc (typ), f_{out} = DC...400 MHz, measured DC to 400 MHz -48 dBc (typ), f_{out} = DC...4 GHz, measured DC to 4 GHz -53 dBc (typ), f_{out} = 4 GHz...6 GHz, measured 4 GHz to 6 GHz -53 dBc (typ), f_{out} = 6 GHz...8 GHz, measured 6 GHz to 8 GHz -50 dBc (typ), f_{out} = 8 GHz...10 GHz, measured 8 GHz to 10 GHz -46 dBc (typ), f_{out} = 10 GHz...12 GHz, measured 10 GHz to 12 GHz -50 dBc (typ), f_{out} = 12 GHz...14 GHz, measured 12 GHz to 14 GHz -42 dBc (typ), f_{out} = 14 GHz...16 GHz, measured 14 GHz to 16 GHz -42 dBc (typ), f_{out} = 16 GHz...18 GHz, measured 16 GHz to 18 GHz -42 dBc (typ), f_{out} = 18 GHz...20 GHz, measured 18 GHz to 20 GHz -48 dBc (typ), f_{out} = 20 GHz...21 GHz, measured 20 GHz to 21 GHz -42 dBc (typ), f_{out} = 21 GHz...22 GHz, measured 21 GHz to 22 GHz
Adjacent band	-48 dBc (typ), f_{out} = DC...4 GHz, measured DC to 8 GHz -48 dBc (typ), f_{out} = 4 GHz...6 GHz, measured 3 GHz to 8 GHz -34 dBc (typ), f_{out} = 6 GHz...8 GHz, measured 4 GHz to 10 GHz -34 dBc (typ), f_{out} = 8 GHz...10 GHz, measured 6 GHz to 12 GHz -46 dBc (typ), f_{out} = 10 GHz...12 GHz, measured 8 GHz to 14 GHz -44 dBc (typ), f_{out} = 12 GHz...14 GHz, measured 10 GHz to 16 GHz -32 dBc (typ), f_{out} = 14 GHz...16 GHz, measured 12 GHz to 18 GHz -30 dBc (typ), f_{out} = 16 GHz...18 GHz, measured 14 GHz to 20 GHz -40 dBc (typ), f_{out} = 18 GHz...20 GHz, measured 16 GHz to 22 GHz -32 dBc (typ), f_{out} = 20 GHz...21 GHz, measured 18 GHz to 22 GHz -32 dBc (typ), f_{out} = 21 GHz...22 GHz, measured 19 GHz to 22 GHz

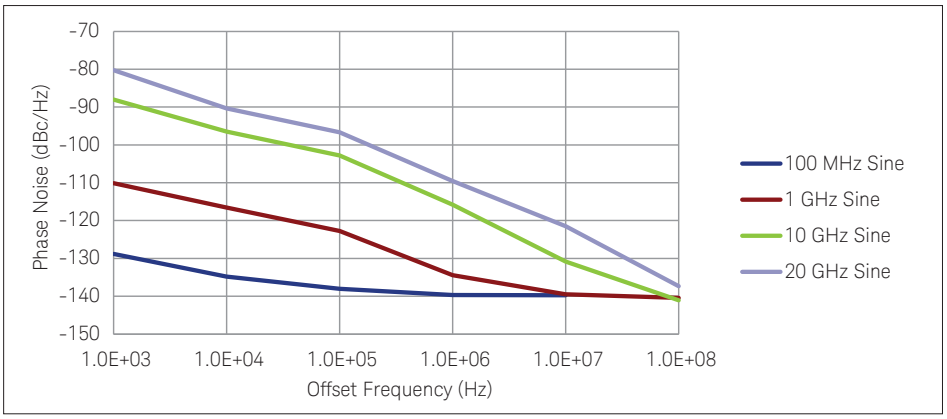
Out 1, 2, 3, 4 (continued)

Amplitude flatness (at SMA connector, compensated for sin(x)/x)	±2 dB (typ), f_{out} = DC...10 GHz +2 dB, -3 dB (typ), f_{out} = 10...20 GHz
Connector type	2.92 mm "K-Style" (female)

2. Unused output must be terminated with 50 Ω to GND
3. Termination voltage = 0 V; adjusted at 23 °C ambient temperature, amplitude increases by 0.4%/°C (typ) for ambient temperature below 23 °C
4. Termination voltage = 0 V
5. Sample Rate 64 GSa/s, output amplitude 500 $mV_{pp(se)}$
6. Measured with a balun (e.g. HL9402)

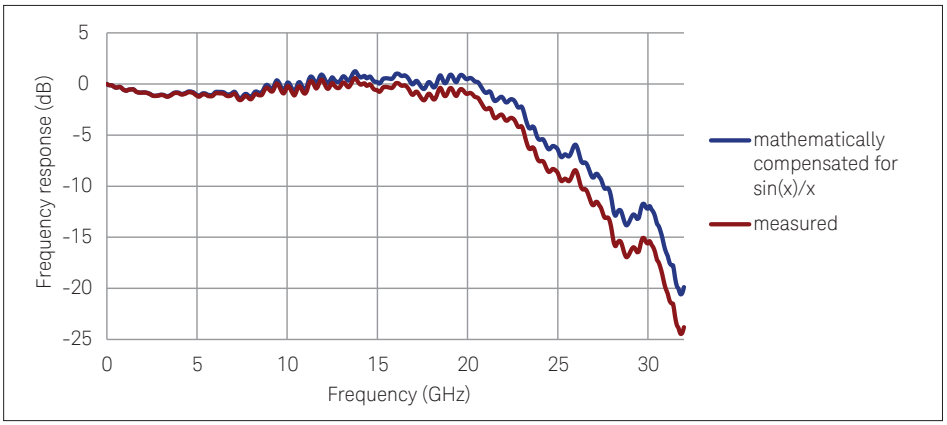
Phase Noise

Phase noise measured with a sample rate of 64 GSa/s, at Out 1, single ended, 500 mV amplitude



Frequency Response

Frequency response measured with a sample rate of 64 GSa/s and a multi-tone signal containing frequencies from DC to 32 GHz with equal amplitudes



Markers (Rev. 2 Only)

2 digital markers are available in the 1 ch, ext.mem mode only. They are available on Out 3 and 4 respectively. In all other modes, no markers are available. Markers do not reduce vertical resolution.

The granularity of markers is 1 sample, a maximum of one rising and one falling edge of a marker are possible within 128 samples.

Run Modes and Sequence Characteristics

Run modes	
Continuous	One waveform segment is continuously repeated
Triggered (Rev. 2 only)	A waveform segment/sequence is generated once after a trigger is received
Gated (Rev. 2 only)	A waveform segment/sequence is generated as long as the Trigger/Gate input is high
Sequencer modes	
Arbitrary	One waveform segment of arbitrary length is continuously looped
Sequence (Rev. 2 only, requires Option –SEQ)	One or more waveform segments are arranged in a linear sequence. Each segment can be repeated a programmable number of times or until an external event is signaled
Scenario (Rev. 2 only, requires Option –SEQ)	One or more sequences are arranged in a linear sequence. Each sequence can be repeated a programmable number of times or until an external event is signaled
Waveform granularity (the length of waveform segments must me a multiple of the granularity)	
int. memory	128 samples
ext. memory, 1 ch mode	256 samples
ext. memory, 2 ch mode	128 samples
ext. memory, 4 ch mode	64 samples
Minimum Waveform length	
int. memory	128 samples
ext. memory	tbd

Trigger/Gate Input (Rev 2 Only)

A Trigger/Gate input is provided on the front panel of the M8195A Rev. 2 and the M8197A.

- The Trigger/Gate Input of the M8195A affects the channels of that M8195A.
- The Trigger/Gate Input of the M8197A affect all channels of all M8195A that are combined in a multi-module system. To achieve best delay accuracy between Trigger/Gate Input and the OUT signals use the Trigger/Gate Input of the M8197A. See timing characteristics below.

Input Range	-4 V to +4 V
Threshold	
Range	-4 V to +4 V
Resolution	10 mV
Sensitivity	100 mV
Polarity	selectable, positive or negative
Input Impedance	50 Ω (nom), DC coupled
Connector type	SMA (female)

Event Input (Rev 2 Only)

An Event input is provided on the front panel of the M8195A and the M8197A.

- The Event input of the M8195A affects the channels of that M8195A.
- The Event input of the M8197A affects all channels of all M8195A that are combined in a multi-module system.

Input Range	-4 V to +4 V
Threshold	
Range	-4 V to +4 V
Resolution	10 mV
Sensitivity	100 mV
Polarity	selectable, positive or negative
Input Impedance	50 Ω (nom), DC coupled
Connector type	SMA (female)

Dynamic Control Input / General Purpose Output (M8197A only)

A bidirectional parallel input and output port is provided on the front panel of the M8197A synchronization module. When the port is configured as input, it can be used as 'Dynamic Control Input' for all channels of a synchronous system to control the sequencing by external hardware. The Dynamic Control Input affects all channels of a synchronous system. When the port is configured as a parallel output, the 14 digital lines can be individually controlled by software to represent logical states zero or one.

A detailed description of the Dynamic Control Input including timing diagram and pin assignment is shown in the M8195A User's Guide.

Configuration as Input	
Input Signals	Data[0..12]_In, Data_Select, Load
Number of addressable segments	2^{24} = 16 777 216
Data Rate	DC to 1 MHz
Setup time	tbd ns (Data_In, Data_Select to rising edge of Load)
Hold time	tbd ns (Rising edge of Load to Data[0..12]_In, Data_Select
Input Range	
Low level	0 V to +0.7V
High level	+1.6 V to 3.6 V
Input Impedance	Internal 10 kΩ to GND
Configuration as Output	
Output signals	Data[0..13]_Out
Output range	
Low level (-12 mA to 0 mA)	0 V to +0.4V
High level (0 mA to 12 mA)	+2.4 V to 3.3 V
Connector type	20 pin Mini D Ribbon (MDR) Connector[7]

7. Manufacturer: 3MTM. Manufacturer Part Number: N10220-52B2PC. 3M is a Trademark of 3M Company.

Timing Characteristics

Delay accuracy	
Trigger/Gate of M8195A to Out	±125 ps (typ)
Trigger/Gate of M8197A to Out	±40 ps (typ)
Event Input of M8195A to Out	±125 ps (typ)
Event Input of M8197A to Out	±125 ps (typ)
Initial skew between channels 1, 2, 3 or 4 of one M8195A AWG module	
Skew	0 ps (typ)
Accuracy	±6 ps (typ)
Total jitter, with pre-distortion	6 ps (pp) at 32 Gb/s PRBS (typ)
Random jitter, RMS	200 fs (typ)

Variable Delay (Rev 2 Only)

In order to compensate for e.g. external cable length differences as well as the initial skew, channel 1, 2, 3 and 4 can be jointly delayed with a very high timing resolution. In case the M8197A synchronization module is used to configure a synchronous system, the variable delay can be used to align the channels of multiple M8195A modules.

Setting the variable delay to e.g. 10ps has following effect:
Out 1, 2, 3 and 4 are delayed by 10 ps with respect to Trigger/Gate Input and Event Input.

Note: Modifying the variable delay always affects the delay of all four channels.

Delay range	0 ns to 10 ns
Delay resolution	50 fs
Delay accuracy	±10 ps (typ)

Reference Clock Input (M8195A and M8197A) (Rev 2 Only)

A clock reference input is provided on the front panel of the M8195A and the M8197A Synchronization module.

- The Clock Reference Input of the M8195A is used as the clock reference for all four channels of that M8195A.
- The Clock Reference Input of the M8197A synchronization module is used as the clock reference for all channels of all M8195A that are combined in a synchronous system.

Input frequency range	10 MHz to 17 GHz (continuous)
Lock range	±1 % (typ)
Input level	200 mV_{pp} to 2 V_{pp}
Impedance	50 Ω (nom)
Connector	SMA (female)

Reference Clock Output (M8195A and M8197A) (Rev 2 only)

Source: Backplane	
Output Frequency	$f_{out} = f_{Sa} / (32 * n)$ with n=1...1024 or $f_{out} = f_{Sa} / 256$
Frequency Accuracy	±20 ppm
Source: Internal	
Output Frequency	$f_{out} = f_{Sa} / (32 * n)$ with n=1...1024 or $f_{out} = f_{Sa} / 256$ or f_{out} = 100 MHz
Frequency Accuracy	±2 ppm
Source: Reference Clock Input of M8195A	
f_{in} = 10 ... 300 MHz	$f_{out} = f_{Sa} / (n * m)$ with n,m = 1...8
f_{in} = 1.68 GHz ... 2.048 GHz	$f_{out} = f_{in} / 8$
f_{in} = 210 MHz ... 17 GHz	$f_{out} = f_{Sa} / (32 * n)$ with n=1...1024 or $f_{out} = f_{Sa} / 256$
Output Amplitude	1 V_{pp} (typ) into 50 Ω
Source Impedance	50 Ω (nom), AC coupled
Connector	SMA (female)

Internal Synthesizer Clock Characteristics

Frequency	54 GHz to 65 GHz
Accuracy	±2 ppm
Resolution	7 digits (e.g. 6 kHz @ 60 GHz)
Phase noise (f_{Sa} = 64 GHz)	< -115 dBc/Hz (typ) at 10 kHz offset, f_{out} = 1 GHz < -95 dBc/Hz (typ) at 10 kHz offset, f_{out} = 10 GHz

Download Times (Rev 2 only)

1 M Samples	3 ms (meas)
128 M Samples	350 ms (meas)
512 M Samples	1.4 s (meas)
2 G Samples	6 s (meas)

Instrument Software

The M8195A is controlled by a combined Soft-Front-Panel and Firmware Application that runs on an embedded AXIe controller or external PC or laptop.

Supported Operating Systems	Win 7 (32 or 64 bit), Win 8 (32 or 64 bit), Win 8.1 (32 or 64 bit)
Required hard disk space	1 Gb
Interface to M8195A hardware	PCIExpress or USB
Application programming interfaces	SCPI, IVI-COM, LabView

General

Power consumption (Rev. 1)	60 W (nom) @ 65 GSa/s
Power consumption (Rev. 2)	180 W (nom) @ 65 GSa/s
Operating temperature	0°C to 40°C
Operating humidity	5% to 80% relative humidity, non-condensing
Operating altitude	Up to 2000 m
Storage temperature	-40 °C to +70 °C
Stored states	User configurations and factory default
Interface to controlling PC	PCIe (see AXIe chassis specification) USB
Form factor	1-slot AXIe
Dimensions (W x H x D)	322.25 mm x 30 mm x 281.5 mm
Weight	3 kg
Safety designed to	IEC61010-1, UL61010, CSA22.2 61010.1 tested
EMC tested to	IEC61326
Warm-up time	30 min
Calibration interval	2 years recommended
Warranty	3 years standard
Cooling requirements	When operating the M8195A choose a location that provides at least 80 mm of clearance at rear, and at least 30 mm of clearance at each side

Definitions

Specification (spec)

The warranted performance of a calibrated instrument that has been stored for a minimum of 2 hours within the operating temperature range of 0°C to 40°C and after a 45-minute warm up period. All specifications include measurement uncertainty and were created in compliance with ISO-17025 methods. Data published in this document are specifications (spec) only where specifically indicated.

Typical (typ)

The characteristic performance, which 80% or more of manufactured instruments will meet. This data is not warranted, does not include measurement uncertainty, and is valid only at room temperature (approximately 23°C).

Nominal (nom)

The mean or average characteristic performance, or the value of an attribute that is determined by design such as a connector type, physical dimension, or operating speed. This data is not warranted and is measured at room temperature (approximately 23°C).

Measured (meas)

An attribute measured during development for purposes of communicating the expected performance. This data is not warranted and is measured at room temperature (approximately 23°C).

Accuracy

Represents the traceable accuracy of a specified parameter. Includes measurement error and timebase error, and calibration source uncertainty.

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