Keysight Technologies
Electronic Warfare Signal Generation: Technologies and Methods

Application Note

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Introduction

Productive and efficient engineering of electronic warfare (EW) systems requires the generation of test signals that accurately and repeatably represent the EW environment. Simulation of multi-emitter environments, in particular, is vital to ensure realistic and representative testing.

Currently, these multi-emitter environments are simulated with large, complex, custom systems that are employed in the system qualification and verification stage, and not widely available to EW design engineers as R&D test equipment. Designers working on optimization and pre-qualification are therefore at a disadvantage compared to wireless engineers performing similar tasks. Engineers often learn of the nature and magnitude of performance problems later in the design phase, leading to delays, design rework, and solutions that are not well-optimized.

This application note will summarize the available technological approaches for EW signal and environment simulation, and the latest progress in flexible, high-fidelity solutions. For example, recent innovations in digital-to-analog converters (DACs) have brought direct digital synthesis (DDS) signal generation into the realm of practicality for EW applications through advances in both bandwidth and signal quality. DDS solutions and other innovations in agile frequency and power control will be discussed in the context of improving design-phase EW engineering productivity.

Realism and Fidelity in Multi-Emitter Environments

Validation and verification of EW systems is heavily dependent on testing with realistic signal environments. EW test realism increases as high-fidelity emitters are added to create density. In addition to emitter fidelity and density, platform motion, emitter scan patterns, receiver antenna models, direction of arrival, and multipath and atmospheric models enhance the ability to test EW systems under realistic conditions. EW systems are now designed to identify emitters using precise direction finding and pulse parameterization in dense environments of 8 to 10 million pulses per second.

The cost of test is as important as test realism, as the relationship between cost and test fidelity is exponential. As test equipment becomes more cost effective and capable, more EW testing can be performed on the ground—in a lab or chamber—rather than in flight. Even though flight testing can add test capability, it does so at great cost and is typically done later in the program lifecycle, adding risk and further cost to the program through missed deadlines if the system under test (SUT) fails. It is far better to test early in a lab environment with as much realism as possible where tests can be easily repeated to iteratively identify and fix problems.

Challenges of Simulating Multi-Emitter Environments

The modern spectral environment contains thousands of emitters—radios, wireless devices, and tens to hundreds of radar threats—producing millions of radar pulses per second amidst background signals and noise. A general overview of the threat frequency spectrum is shown in Figure 1.
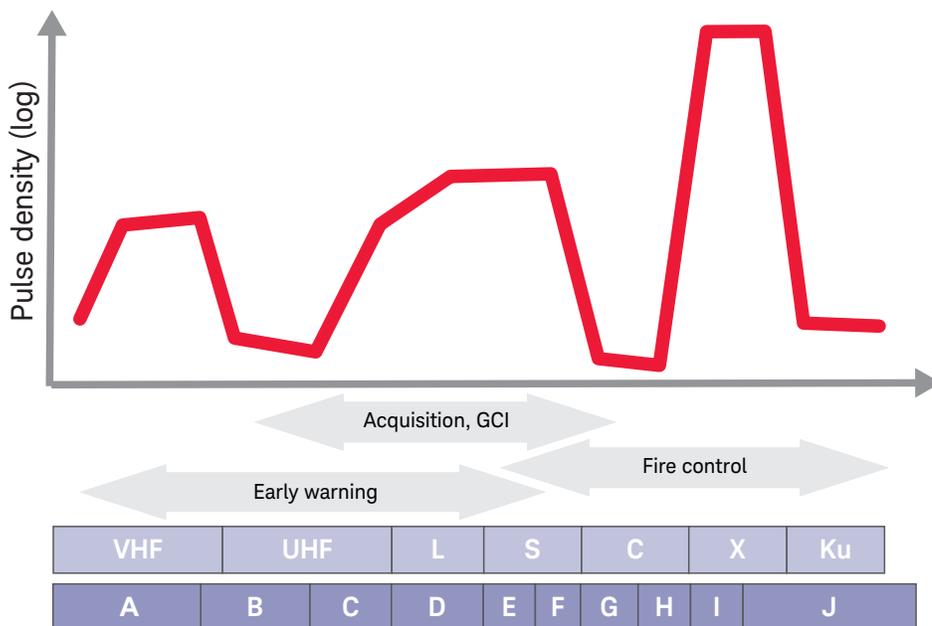

Figure 1. A general representation of the threat density vs. frequency band in a typical operational environment. The full RF/microwave environment would be a combination of the threat and commercial wireless environments.

Simulating this environment is a major challenge, especially in the design phase, when design flexibility and productivity are at their greatest. The situation is very different from the typical wireless design task, where a single signal generator can produce the required signal, perhaps augmented by a second signal generator to add interference or noise.

In EW design the multiplicity and density of the environment—and often the bandwidth—make it impractical to use a single source or a small number of sources to simulate a single emitter or a small number of emitters. Cost, space, and complexity considerations rule out these approaches.

The only practical solution is to simulate many emitters with a single source, and to employ multiple sources—each typically simulating many emitters—when required to produce the needed signal density or to simulate specific phenomena such as angle-of-arrival (AoA).

The ability to simulate multiple emitters at multiple frequencies depends on the pulse repetition frequency, duty cycle and number of emitters, and ability of the source to switch between frequency, amplitude, and modulation quickly.

A limiting factor in the use of a single signal generator to simulate multiple emitters is pulse collisions. Figures 2 and 3 show the number of pulse collisions expected for the cases of low and high pulse repetition frequency (PRF).
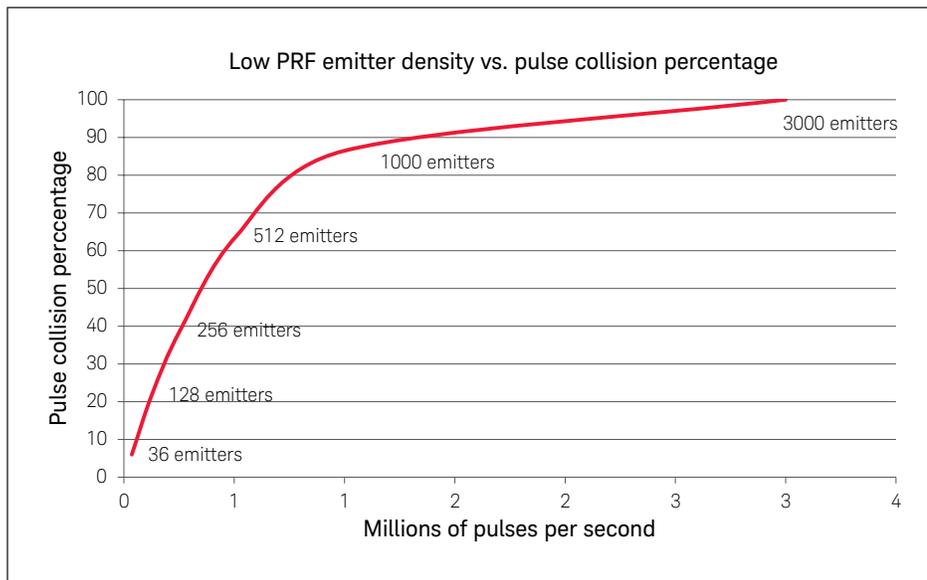

Figure 2. As the number of emitters grows, the number of pulse collisions grows even when all emitters use low PRF.
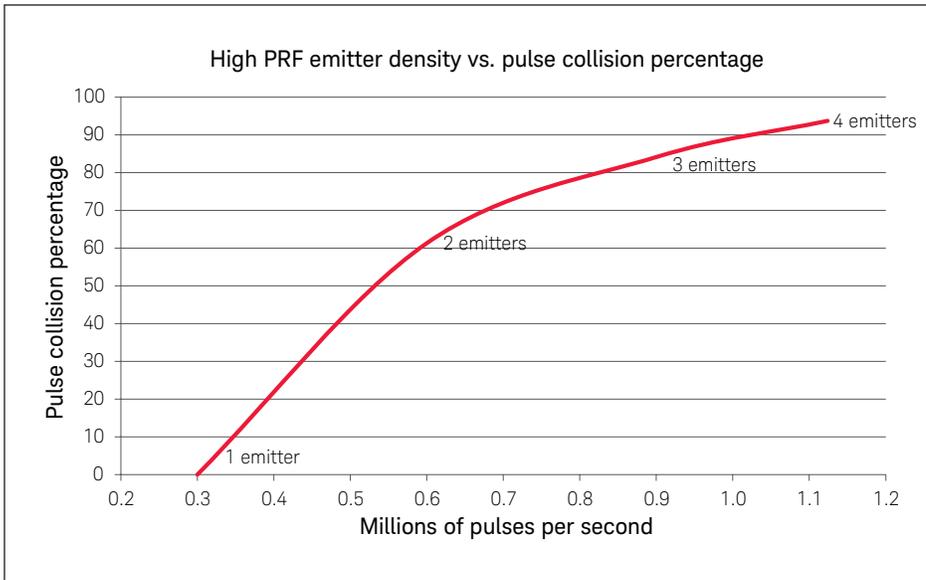
Figure 3. The percentage of pulse collisions climbs very quickly as high-PRF emitters are added to a simulation.

A source's agility is a factor in its ability to simulate multiple emitters. Source frequency and amplitude settling time (whichever is greater) is the transition time between playing one pulse descriptor word (PDW) and the next.

Total pulse density for a single source is limited by the sum of the transition time and the width of the transmitted pulses, a lockout period parameter as shown in Figure 4. It is obviously desirable that the lockout period be as short as possible, and therefore that the source settling times be as brief as possible.
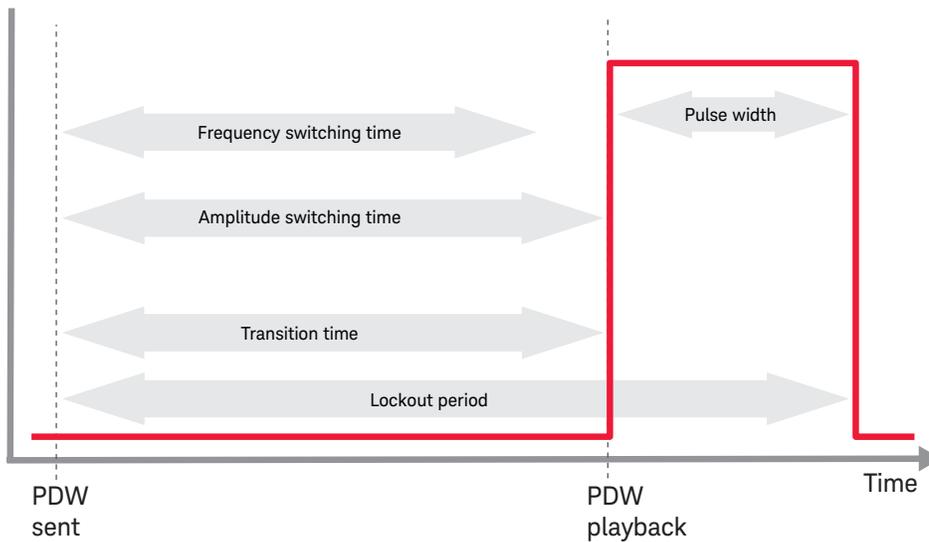

Figure 4. The ability to simulate multiple emitters depends not only on emitter parameters like PRF and pulse width, but also the frequency and amplitude switching speeds and setting times of the signal source used to synthesize the emitters. If the source is switching, it cannot play a pulse. If it is playing a pulse, it cannot switch. The source is unavailable to simulate a different threat during the lockout period.

To simulate high pulse density and the possibility of some overlapping pulses, it is often necessary to combine multiple sources. As more sources are added to the test configuration, pulse density should scale easily and seamlessly, ultimately reaching the desired tradeoff of satisfactory simulation realism and cost.

Technology Improvements Simplify System Integration and Reduce Cost

Simulating more threats to create more pulse density ultimately requires more parallel simulation channels, even if the simulation channel can switch frequency and amplitude quickly. This is because pulses begin to collide in the time domain as the number of emitters, their PRFs, and their duty cycles grow larger[1]. Pulses that overlap in the time domain must be played out of parallel generators or selectively dropped based on a PDW priority scheme. Unfortunately, the increased realism of a higher-density environment comes at a substantially higher system cost, as shown in Figure 5.
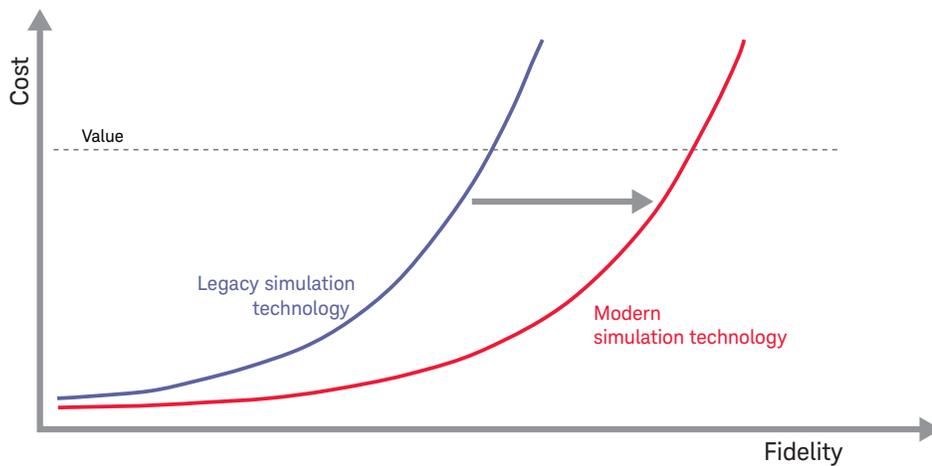

Figure 5. Simulation fidelity and cost increase exponentially. System integrators and evaluators must decide the level of cost vs. fidelity that ensures system performance. New simulation technologies enable more simulation realism and fidelity at lower cost.

In the past, simulations have generally been created with a separate component for each emulation function, such as signal generation, modulation/pulsing, attenuation or amplification, and phase shift. The same PDW would be sent to each functional component to provide output on a pulse-to-pulse basis. For instance, a synthesizer would generate the output frequency, while a separate modulator would create pulsed modulation and/or AM/FM/PM modulation. Amplifiers and attenuators would adjust the signal to the desired output power level. An example of this system topology is shown in Figure 6.
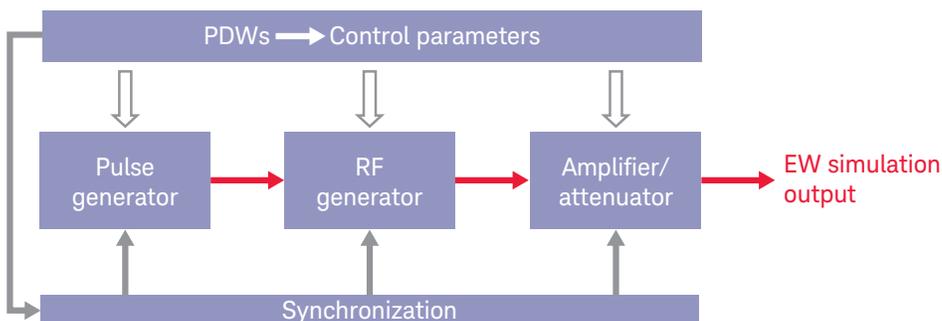

Figure 6. In the traditional approach, PDW control parameters are sent in parallel to multiple functional elements, on a pulse-to-pulse basis, to generate and modify the desired signal. This approach results in a complex system, demanding precise synchronization.

1. Philip Kazserman, "Frequency of pulse co-incidence given *n* radars of different pulse widths and PRFs," IEEE Trans. Aerospace and Electronic Systems, vol. AES-6. p. 657-662, September 1970.

Since multiple functional components are required to produce each output channel, time synchronization is a significant configuration and operational challenge. A wide variety of settling times and latencies must be fully characterized to optimize pulse density by minimizing lockout periods.

This approach can be scaled directly to create multiple coordinated channels, as shown in Figure 7. However systems configured in this way require a large footprint, occupying more rack space, and cost escalates quickly.
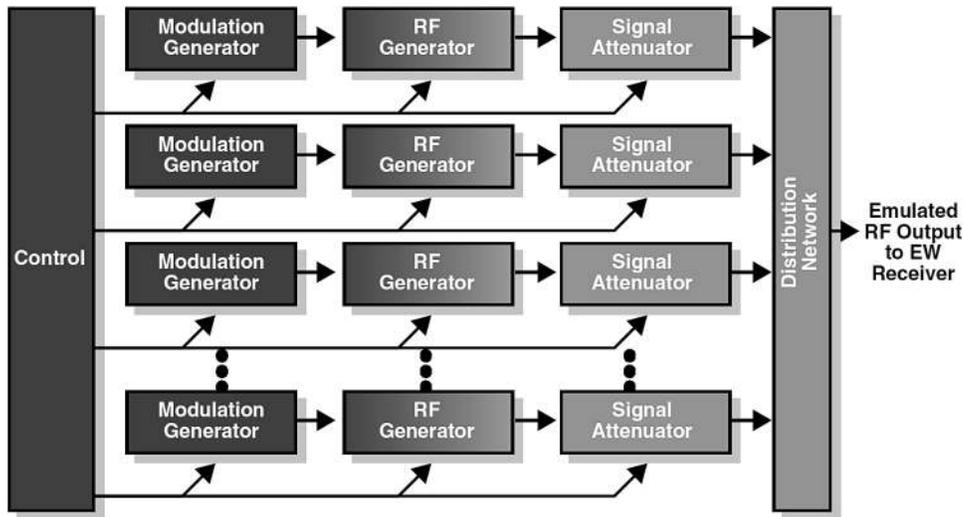

Figure 7. A signal generation approach using separate functional elements can be scaled up in a straightforward manner to increase pulse density and generate a more realistic environment. Unfortunately cost and space requirements scale up rapidly as well.[1]

The controller shown in Figure 7 would route PDWs to channels based on emitter parameters such as frequency, amplitude, and pulse repetition frequency and also the availability of each channel to implement the PDW. Since a channel cannot execute the parameters of two different PDWs at the same time, one could be shunted to a backup channel or dropped according to its priority.

Ultimately, EW receivers must be able to handle 8-10 million pulses per second where most of the pulse density occurs at X-band. EW receivers must be able to handle pulses arriving at the same time at different frequencies from different angles. Creating pulses that are coincident with one another in the time domain should be a goal of simulation to increase simulation realism.

Though Figure 7 describes a very capable system, the level of integration the system elements is rather low. Recent developments in analog and digital signal generation technologies are enabling a higher degree of integration, and solutions which are more cost- and space-efficient, as described in the section, "Increasing Integration in EW Test Solutions." There are several methods of controlling simulations depending on test objectives.

Control of Hardware-in-the-Loop Testing

Depending on the integration of simulation elements and the simulation length, scenarios can be played from list memory or streamed over a digital interface such as low-voltage differential signaling (LVDS). List mode plays PDWs from list memory for shorter scenario lengths with some ability to trigger between lists for an adaptive (closed-loop) simulation in response to the SUT.

For example, there is often a need to switch between one simulated threat mode to another in response to identification and jamming by the SUT. For long scenario lengths with fast control over scenario changes, PDWs can be streamed over the LVDS to the signal generation system operating in an agile controller mode. In this case, simulation software generates batches of PDWs according to simulation kinematic granularity and streams them ahead of their desired play time.

In either method of control, the goals are to stress the SUT with increasing pulse density, depending on the number of simulation channels available and the parameters of the threats to be simulated. As pulse density increases, PDWs can be dropped according to a priority scheme as they increasingly collide in the time domain and there are insufficient signal generation channels to play them.

Creating AoA

In addition to creating emitters with the desired fidelity and density, it is also important to match the geometry and kinematics of EW scenarios since the AoA of a radar threat to the EW system changes slowly compared to other parameters such as center frequency and pulse repetition frequency.

EW systems measure AoA and estimate distance using amplitude comparison, differential Doppler, interferometry (phase difference), and time difference of arrival (TDoA). Precise AoA measurements enable precise localization of radar threats. New stand-off jamming systems use active electronically-scanned arrays capable of precise beam forming to minimize loss of jamming power due to beam spreading towards a threat. Moreoever, EW receivers with better AoA capability reduce the need for pulse de-interleaving and sorting. Consequently, AoA is an increasingly-important test requirement.

Techniques for creating AoA

In the past, AoA was created with a combination of signal sources and analog phase shifters, attenuators, and gain blocks in the cable path to the SUT. Analog elements in the cable path took up a lot of space, had limited resolution, and were expensive. As an alternative, and depending on their architecture, sources can be linked together to create phase coherent output, allowing for finer control over creating phase fronts to the SUT. Similarly, amplitude control at the source can be used to create appropriate amplitude differences at SUT receive channels.

The ability to control AoA to meet modern test requirements depends on the architecture of the source. At a minimum, it should be possible to lock the local oscillators (LOs) of multiple sources together so that they all share the same phase. Often, calibration is required to finely align phase and timing between sources.

Creating small, accurate, and repeatable differences in phase or frequency between channels is the next challenge. Sources based on DDS architecture allow AoA to be controlled digitally in a numerically-controlled oscillator. Phase alignment in a DDS source is then a matter of sharing reference clocks. Calibrations to provide accuracy and repeatability can be uploaded to a table to be applied in real-time.

Overview of Source Technologies for EW Test

The characteristics and tradeoffs of EW signal generation systems are largely determined by the core synthesizer and oscillator technologies used. To provide insight into the most significant choices for EW engineers, this section will summarize the three principal technologies currently available:

- Direct analog synthesis (DAS)
- Phase-locked loop or indirect analog synthesis (PLL, frequently fractional-N)
- Direct digital synthesis (DDS)

General source requirements

Signal sources used to test EW systems must be broadband. Traditionally, a frequency range of 0.5 to 18 GHz was required. Frequency requirements have expanded dramatically in recent years, now beginning near DC and extending as high as 40 GHz. This allows systems to simulate early warning, fire control, and missile-seeker radars from a single output channel.

In addition to wide frequency coverage, sources for EW test must have fast frequency and amplitude switching speeds to simulate different radars operating in different modes in different frequency bands.

PLLs and fractional-N synthesis

Indirect synthesis

Most general-purpose sources today are PLL-based, where a broadband oscillator such as a voltage- controlled or YIG-tuned oscillator is locked to a stable reference in a phase-locked loop (PLL). The PLL improves signal quality by reducing phase noise and spurious signals in the output. To provide a combination of wide frequency range and fine frequency resolution, PLL-based sources have been configured with a combination of sum and step loops or a single loop with fine fractional division capability. These fractional-N PLLs offer excellent signal quality and fine frequency resolution in a cost-effective single-loop configuration, making them a good choice for general purpose signal sources.

Unfortunately, the required control loop filtering in PLLs results in a significant settling or loop-response time. This limits the ability of the synthesizer to switch frequency quickly. Due to their comparatively large transition time, these sources are limited in their ability to simulate multiple radar threats out of a single channel, even if they have the necessary broadband frequency coverage and frequency resolution. They also lack phase-repeatable switching capability.

Direct analog synthesis

A direct analog synthesizer typically contains several stable frequency references multiplied or divided from the same crystal oscillator reference. These frequency references (and their harmonics) can be switched in and out of the signal path and multiplied, divided, added, and subtracted to provide fine frequency resolution quickly. The frequencies of these references are chosen to reduce the amount of multiplication stages required such that phase noise increases only moderately as frequency is increased. Division to lower frequencies reduces the phase noise.

Since the switches and arithmetic operators used in the DAS approach operate very quickly and do not need loop filtering, these synthesizers have very high frequency agility. They have therefore been a common architecture for EW test solutions.

However, DAS technology has several drawbacks. First, numerous stages are required to achieve the desired frequency resolution. Switching parallel and series multiplication, division, and mixing stages requires more hardware than PLLs and generally reduces reliability. Second, circuit noise from each stage is cascaded, and phase noise is multiplied through the stages. Finally, each stage adds components which increase size, weight, and cost.

On the positive side for EW applications, DAS has the potential for limited phase-repeatable frequency switching. However, though all frequencies are usually derived from the same reference, divider ambiguities generally preclude full phase-coherent switching.

DDS now suitable for EW applications

The DDS approach, based on DAC circuits, is a natural fit for the needs of EW signal simulation. However, until recently, DACs were not available with the required combination of fast sample rates and high purity.

Fast sample rates are needed to produce outputs with very wide bandwidth, so that a minimum of multiplying stages can be used to produce the desired output frequencies. The use of either a large number of multiplying stages or a DAC of insufficient purity would limit the effective spurious-free dynamic range (SFDR) of the EW synthesizer. In concept, a DDS is one of the simplest types of signal generators. In a frequency-tunable DDS, data from a numerically-controlled oscillator is converted to analog form by a DAC and lowpass filtered to remove image frequencies and harmonics. A block diagram of the major elements of a DDS is shown in Figure 8.
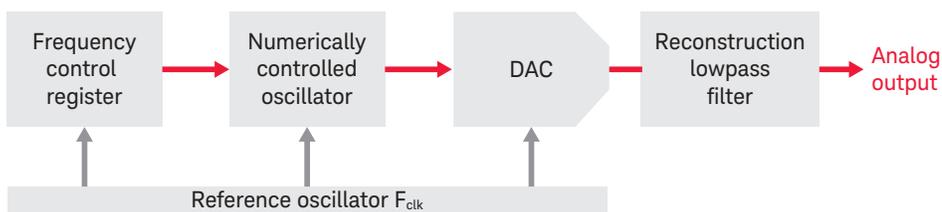

Figure 8. Principal functional blocks of a direct digital synthesizer.

The numerically-controlled oscillator itself consists of two elements: a phase accumulator (PA) and a phase-to-amplitude converter (PAC) as shown in Figure 9. In modern DDS designs, these are often implemented using field programmable gate arrays (FPGAs) or dedicated integrated circuits.
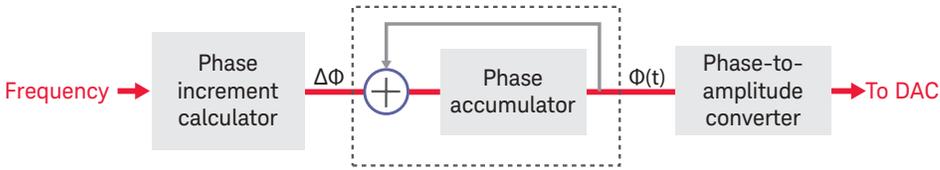

Figure 9. Functional block diagram of a numerically-controlled oscillator.

In frequency synthesis, a frequency control word—a delta phase—is sent to the phase accumulator along with the digital reference clock. For each clock cycle, this delta phase is added in the phase accumulator with high precision. The phase value generated by the accumulator is then converted to a sinusoidal amplitude in the phase-to-amplitude converter. The digital sine wave is then sent to the DAC and output at a frequency given by the DDS tuning equation, where N is the number of bits in the frequency control word[1]:

$$f_{out} = \frac{\Delta phase}{2^N} f_{clk}$$

This equation demonstrates that higher output frequencies are achieved by greater DAC clock frequencies while resolution is controlled by the number of bits in the frequency control word and phase accumulators. The numerically controlled oscillator behaves as a divider to the reference clock to provide frequencies with high resolution according to the bit depths of the phase register and frequency control word. Note that transitions to new frequencies happen in one clock cycle.

1. David Buchanan, "Choosing DACs for direct digital synthesis,"Analog Devices Application Note 237, Available: http://application-notes.digchip.com/013/13-14876.pdf

Advantages of DDS

The new Keysight UXG agile signal generator uses DDS technology made possible by a Keysight-proprietary DAC to generate multi-emitter simulations. DDS has several advantages over other synthesis technologies for EW applications:

– Digital control of extremely fine frequency and phase tuning increments within a single clock cycle. In the Keysight UXG, frequency resolution is one Hertz and phase resolution is sub-degree. Fractional-N techniques can provide micro-Hertz resolution, but frequency changes are much slower due to PLL filtering. DAS techniques provide rapid frequency switching, but at a cost in frequency resolution.
– Fast frequency hopping with phase continuity and phase repeatability to simulate multiple pulse-Doppler radars at different frequencies while maintaining their original phase. This combination of phase control and hopping speed is unique to the Keysight UXG. DAS techniques offer hop speed and frequency/phase repeatability only under limited conditions.
– Modulation is created in the digital domain, providing numerical precision and repeatability.

There are other advantages to using DDS that are of interest to the EW engineer. Many DDSs employ a digital modulator for amplitude, frequency, and phase modulation for creation of digitally-modulated signals in the numerically-controlled oscillator. Linear frequency modulated (LFM) chirps and Barker codes can also be directly synthesized using the numerically-controlled oscillator. Chirp bandwidth depends on the bandwidth of the bandpass filters after each multiplication stage and whether the signal is crossing a band.

Microwave source architecture using DDS

Modern EW applications require frequency coverage to 40 GHz, along with high agility and high purity. Digital signal processing technologies for numeric signal creation have been adequate for some time, but wideband DAC performance has been inadequate for these applications. Available DACs with very wide bandwidth and high clock rate have not been sufficiently pure, while DACs with good signal purity and high bit depth have been limited to lower frequency clocks and narrower bandwidth.

Recent DAC innovations from Keysight provide an example of a DAC and DDS suitable for EW test applications. The DAC has been designed for RF applications, with a combination of high bit depth and excellent purity, including spurious-free dynamic range and phase noise. The high sample rate of the DAC supports a wide bandwidth DDS that allows microwave frequencies to be synthesized with a low number of multiplication stages. Limiting multiplication stages limits the phase noise and spurious signals present in microwave output.

EW testing also requires precise signal amplitudes, over a wide range of power levels. These power levels must be switched as fast as frequencies are changed, without signal distortion from attenuator settling. As with the DAC, these demands have led Keysight to develop a new series of FET switches to implement a solid-state attenuator with high agility, low distortion, and an amplitude range of 120 dB. The agile amplitude range of the attenuator is 80 dB anywhere in the 0 dBm to -120 dBm output range.

The architecture of a true DDS based, agile microwave signal generator utilizing developments in DAC and FET switching technology is shown in Figure 10.
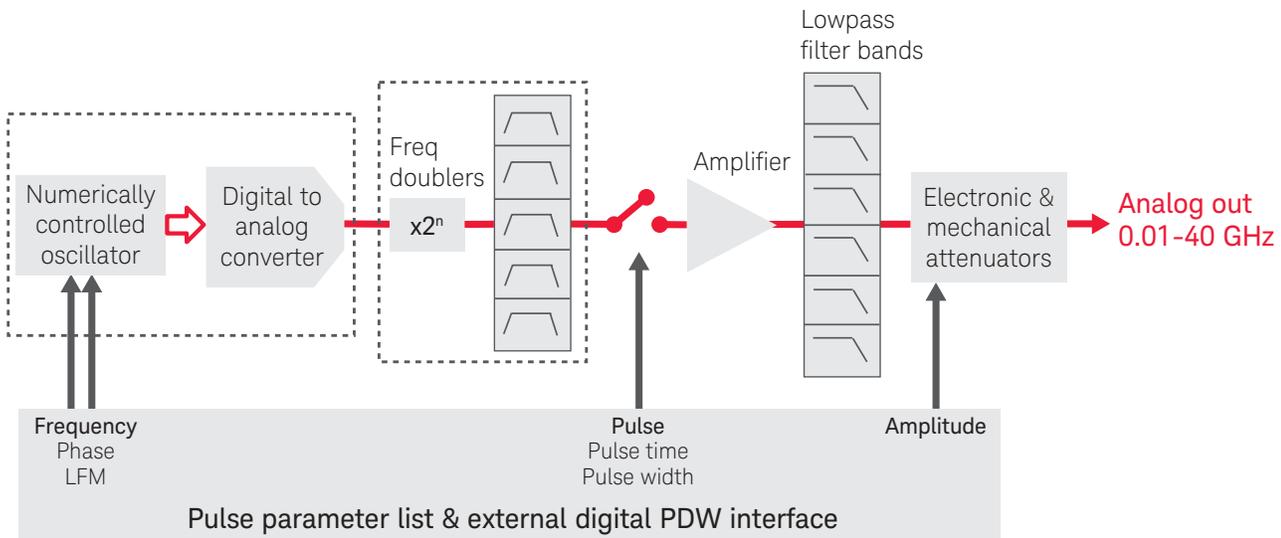
Figure 10. High-level block diagram of a DDS-based agile signal generator, covering 0.01 to 40 GHz.

Signal generation begins with a DDS, optimized for very low spurious output, since spurs increase for each doubling stage. A sequence of doubler circuits is then used as needed to create signals up to 40 GHz. Each multiplication stage employs bandpass filters to remove unwanted signals from the multipliers.

The FET-based agile attenuator is then used to produce the desired output levels. This attenuator provides very fast settling, matched to frequency switching speed, so that the source can implement open loop power control with high accuracy and no loss in switching time.

Increasing Integration in EW Test Solutions

A general trend in EW simulation solutions is to absorb more simulation elements into the RF/microwave signal source. For example, the Keysight UXG agile signal generator combines the intra-pulse modulation, pulse modulation, and amplification/attenuation stages into the fast frequency synthesizer.

By implementing a high level of functional integration, a DDS-based agile source, and a matching agile attenuator, the UXG can meet important functional and performance requirements for EW test:

- – Fast frequency, amplitude, and phase switching for fast transitions between multiple emitters
- – High dynamic range to match the dynamic range of the modern EW receiver
- – A wide, accurate, agile amplitude range to simulate multiple threats with accurate power levels and switch amplitude as quickly as frequency
- – Low noise floor to test receiver sensitivity as channels are combined
- – Pulse modulation with a high on/off ratio and fast settling with low distortion
- – Intrapulse modulation capability for pulse compression such as Barker codes and linear frequency modulation
- – Scalable to multi-channel and multi-port threat simulation to increase pulse density and realism easily
- – Wide frequency range from near DC to 40 GHz to keep pace with modern threat simulation requirements
- – BCD frequency control interface for backward compatibility with legacy sources previously used as LOs
- – LVDS interface to allow high-rate PDW streaming—EW simulation sources need a fast, full-featured interface for streaming complete PDWs at a high rate rather than frequency-only control

In systems with a traditional, distributed architecture (as described in Figure 7) the synchronization of an agile LO with functions such as pulse modulation, frequency/phase modulation, and amplitude control is a considerable challenge. In an integrated EW test solution such as the UXG, this synchronization is automatic, provided by the test equipment itself. By simplifying hardware and system complexity, this integrated approach promises to improve both performance and reliability.

Conclusion

A variety of technologies have been used to generate the signals needed for effective EW simulation. Each of these technologies has brought a different combination of benefits and challenges. The highest fidelity solutions have provided very realistic simulations of the EW environment but their use has been limited by their complexity and expense.

Recent innovations in core hardware such as DACs and FPGAs have enabled new solutions with the hardware simplicity and reliability of traditional test equipment. These solutions will provide dramatic improvements in solution cost and size, bringing high-fidelity EW environment simulation to a much earlier phase in the design process. Using realistic EW environment simulation at the optimization and pre-verification stages of design will improve performance, speed the design process, and reduce overall costs.

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