Errata

Title & Document Type: 8175A Digital Signal Generator Operating and Service Manual

Manual Part Number: 08175-90001

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HP References in this Manual

This manual may contain references to HP or Hewlett-Packard. Please note that Hewlett-Packard's former test and measurement, semiconductor products and chemical analysis businesses are now part of Agilent Technologies. We have made no changes to this manual copy. The HP XXXX referred to in this document is now the Agilent XXXX. For example, model number HP8648A is now model number Agilent 8648A.

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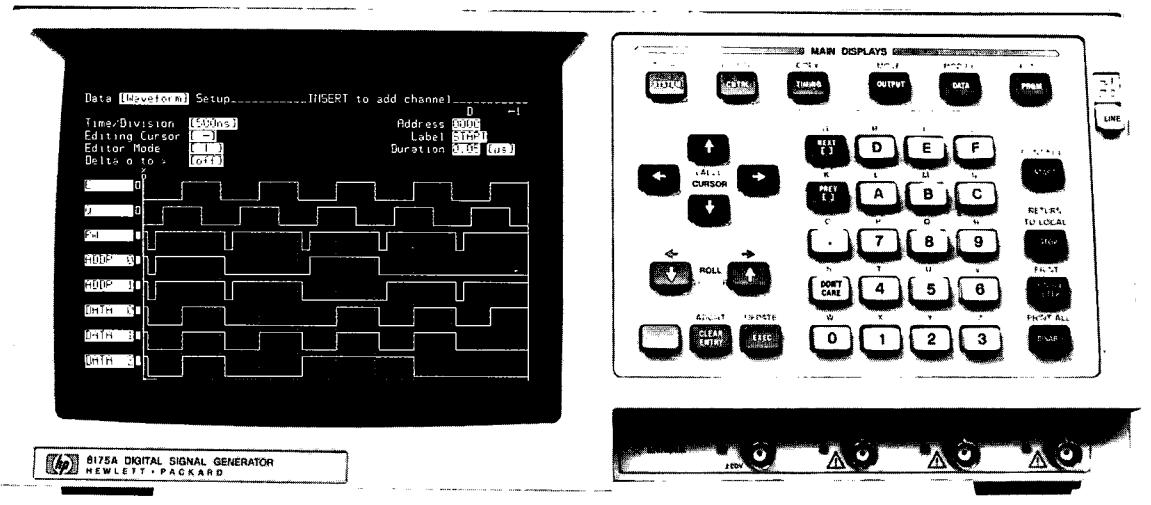
OPERATING AND SERVICE MANUAL

8175A DIGITAL SIGNAL GENERATOR



HEWLETT PACKARD

HP 8175A

HEWLETT PACKARD

OPERATING AND SERVICE MANUAL

8175A DIGITAL SIGNAL GENERATOR (Including Option 001)

SERIAL NUMBERS

This manual applies directly to instruments with serial number 2520G000152 and higher. Any change made in instruments having serial numbers higher than the above number will be found in a "Manual Changes" supplement supplied with this manual. Be sure to examine the supplement for changes which apply to your instrument and record these changes in the manual. Backdating information for instruments with lower serial numbers can be found in Section 7 (yellow pages).

HERRENBERGER STR. 130, D-7030 BOBLINGEN
FEDERAL REPUBLIC OF GERMANY

MANUAL PART No. 08175-90001
MICROFICHE PART No. 08175-95001

PRINTED: JULY 1985

SAFETY SUMMARY

The following general safety precautions must be observed during all phases of operation, service, and repair of this instrument. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of the instrument. Hewlett-Packard Company assumes no liability for the customer's failure to comply with these requirements.

GENERAL – This is a Safety Class I instrument (provided with terminal for protective earthing) and has been manufactured and tested according to international safety standards.

OPERATION – BEFORE APPLYING POWER comply with the installation section. Additionally, the following shall be observed:

Do not remove instrument covers when operating.
Before the instrument is switched on, all protective earth terminals, extension cords, auto-transformers and devices connected to it should be connected to a protective earth via a ground socket. Any interruption of the protective earth grounding will cause a potential shock hazard that could result in serious personal injury. Whenever it is likely that the protection has been impaired, the instrument must be made inoperative and be secured against any unintended operation.

Make sure that only fuses with the required rated current and of the specified type (normal blow, time delay, etc.) are used for replacement. The use of repaired fuses and the short-circuiting of fuseholders must be avoided.

Adjustments described in the manual are performed with power supplied to the instrument while protective covers are removed. Energy available at many points may, if contacted, result in personal injury.

Any adjustment, maintenance, and repair of the opened instrument under voltage should be avoided as much as possible, and when inevitable, should be carried out only by a skilled person who is aware of the hazard involved. Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation is present. Do not replace components with power cable connected.

Do not operate the instrument in the presence of flammable gases or fumes. Operation of any electrical instrument in such an environment constitutes a definite safety hazard.

Do not install substitute parts or perform any unauthorized modification to the instrument.

Capacitors inside the instrument may still be charged even if the instrument has been disconnected from its source of supply.

To prevent CRT implosion, avoid rough handling or jarring of the instrument. Handling of the CRT shall be done only by qualified maintenance personnel using approved safety mask and gloves.

SAFETY SYMBOLS

The apparatus will be marked with this symbol when it is necessary for the user to refer to the instruction manual in order to protect the apparatus against damage.

Indicates dangerous voltages.

Earth terminal

WARNING The WARNING sign denotes a hazard. It calls attention to a procedure, practice or the like, which, if not correctly performed or adhered to, could result in injury or loss of life. Do not proceed beyond a WARNING sign until the indicated conditions are fully understood and met.

CAUTION The CAUTION sign denotes a hazard. It calls attention to an operating procedure, practice, or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the equipment. Do not proceed beyond a CAUTION sign until the indicated conditions are fully understood and met.

WARNING

Dangerous voltages, capable of causing serious personal injury, are present in this instrument. Use extreme caution when handling, testing, and adjusting.

LIST OF CONTENTS

NOTE: Chapters 1 to 4 contents are listed in the Operating and Programming part of this manual.

SECTION 5: Adjustments Procedure

SECTION 6: Replaceable Parts

SECTION 7: Backdating

SECTION 8: Service

LIST OF ILLUSTRATIONS (Refer also to the Operating and Programming Manual)

Figure

LIST OF TABLES (Refer also to the Operating and Programming Manual)

Table

SECTION 5
ADJUSTMENTS

5-1 INTRODUCTION

This section describes the adjustments which will return the instrument to peak operating condition after repairs have been completed. An adjustment location diagram is given on a foldout page at the end of this section.

5-2 SAFETY CONSIDERATIONS

Although this instrument has been designed in accordance with international safety standards, this manual contains information, cautions and warnings which must be followed to ensure safe operation and to retain the instrument in a safe condition (see Sections 2 and 3).

WARNING

Any interruption of the protective (grounding) conductor (inside or outside the instrument) or disconnection of the protective earth terminal is likely to make the instrument dangerous. Intentional interruption is prohibited.

Any adjustment, maintenance or repair of the opened instrument with voltage applied should be avoided as much as possible and, when inevitable, should be carried out only by a skilled person who is aware of the hazard involved.

5-3 EQUIPMENT REQUIRED

The test equipment required for the adjustment procedure is listed in Table 1-1, Recommended Test Equipment. The critical specifications of substitue test instruments must meet or exceed the standards listed in the table if the instrument is to meet the standards set forth in Table 1-2, Specifications.

5-4 ADJUSTMENT PROCEDURE

The adjustment procedure is divided into the following sections:

An adjustments points locator diagram (Figure 5-5) is included at the end of the adjustment procedure.

Execute a paragraph completely and in the order in which it is presented. Only the significant instrument settings are given.

Allow a 30 minute warm-up period before starting the adjustments.

For adjustments on the CPU Board, Clock Board, Data Board or Fine Timing Board use the service connectors as shown in Figure 5-1.

CAUTION

Instrument must not be operated without cover over power supply and fan areas.

The Power Supply Board does not have to be removed for adjustments to be made to the output voltages (they can be monitored at the board's Test Connector).

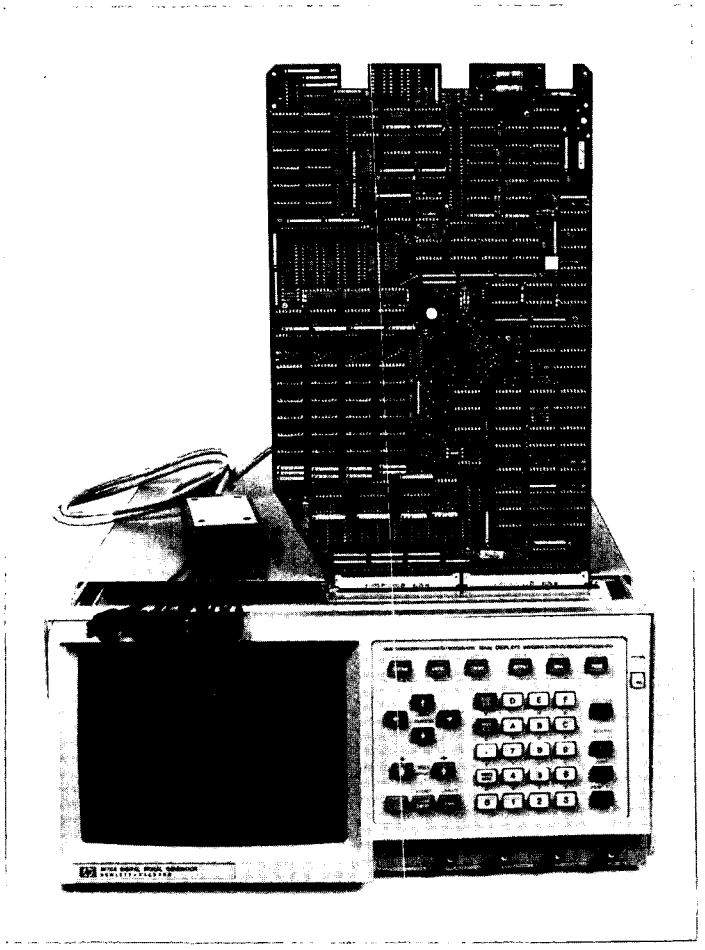


Figure 5-1. 8175A Service Position

5-5 POWER SUPPLY BOARD

Equipment: DVM, Power Supply

Procedure:

WARNING

Due to storage capacitors, lethal or harmful voltages are present on the board for up to FIVE minutes after disconnecting the line!
Therefore, before removing the Power Supply Board, ensure that FIVE minutes have elapsed after line disconnection (for discharging of all storage capacitors)!

1) Low Power Supply Threshold Adjustment (if necessary!)

With Power Supply Board out of Frame, to adjust the threshold of the Low Power Supply:
Apply + 15 VDC (max 20 VDC) to TP2 ("LPS" LED is ON).
Apply DVM controlled test voltage to the + 5V test pin on test connector.
Adjust A10R38 for the following limits:

"LPS" LED OFF with test voltage > = + 4.83V
"LPS" LED ON with test voltage < = + 4.85V

2) Output Voltage Adjust

Install the Power Supply Board back in the 8175A, and adjust the output voltages measured at the P.S. Bd. Test Connector, when instrument is in normal working condition (all supplied boards installed).

Test Connector	Adjust	Test Limit
+5V	R21	+ 5.00V +/- 50 mV
-5.2V	(R21)	- 5.20V +/- 50 mV
+15V	R48	+15.06V +/- 10 mV
+15V Video	R74	+15.06V +/- 10 mV
-15V	R49	-15.06V +/- 10 mV
+24V	R54	+24.06V +/- 20 mV
-24V	R55	-24.06V +/- 20 mV

5-6 MICROPROCESSOR BOARD

Equipment: DVM

Procedure:

1. Remove the Microprocessor Board from its normal position (disconnect the two ribbon cables first!) and plug it into the Service Connectors (Figure 5-1).
   Reconnect the ribbon cables.
   Turn Power ON, System Page, Configuration menu should be displayed.

2. Connect DVM low terminal to the GND Testpoint on the Microprocessor Board and measure at TP +10V.
   Adjust A20 R102 for + 10.00V +/- 10 mV.

5-7 CLOCK BOARD

Equipment: DVM, Pulse Generator, Osciloscope with 10017A Probe, Counter

Procedure:

1. Remove the Clock Board from its normal position (disconnect the three input cables first!), and plug it into the Service Connectors.
   Reconnect the cables.
   Turn Power ON, the System Page, Configuration menu should be displayed.
   Recall Standard Settings.

2. Confirm that the following reference voltages are correct:

Q50 Emitter	+4.00V	+-200mV
Q51 Emitter	-4.00V	+-200mV
C78 -5 Ref	-5.00V	+-200mV
C74 +5V Ref Osc	+5.00V	+-200mV
C71 -5.2V Osc	-5.00V	+-100mV
C72 +15V Osc	+14.8V	+-200mV
C73 -15V Osc	-13.0V	+-200mV
R100/101	+1.4V	+-200mV

   Connect DVM low terminal to the GND Testpoint on the Clock Board as near as possible to TP14 and measure with DVM high terminal at TP14 the +5V Ref Voltage.
   Adjust with A30R62 for +5.005 V +-5 mV.

3. **POD Input Threshold** (without a POD connected)

   Set 8175A:
   Control Page (PAR)
   Trigger POD Threshold [+] 0.0V

   Connect the DVM high terminal to TP1 and the GND terminal to shield of TP13.
   Adjust A30R6 for 0V +-1mV.

   Note:
   This adjustment will also be necessary if a DAC is changed on the CPU Board A20 or, if a new CPU Board is installed.

   Check for the following POD thresholds, the voltage at TP1:

Trigger Pod Threshold	**TP1**	
+9.9V	-1.65V	+-20mV
-9.9V	+1.65V	+-20mV
TTL	-234mV	+-10mV
ECL	+220mV	+-10mV

4. EXT/EXT CLK Input Compensation

Set 8112A:

PER	1us
HIL/LOL	+8V/-8V
DTY	50%

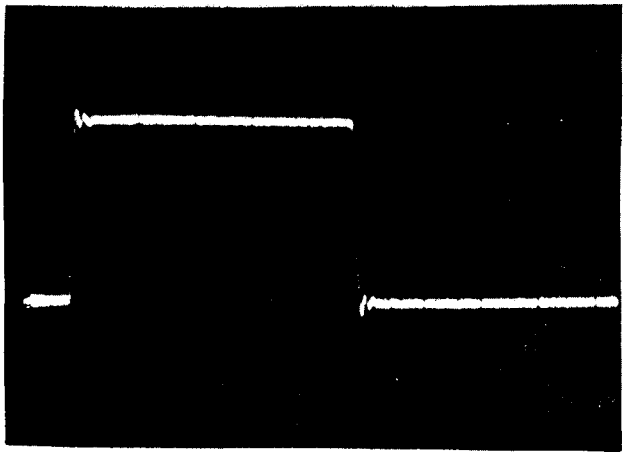
Set 8175A:
Control Page (PAR)
START and/or STOP from [external Input]
with START on [↑] Edge.

Scope settings:
Time/Div 0.1us
V/Div. 0.01

Connect 8112A output via 50 Ohm feedthrough to the EXT CLK BNC Input on rear panel. Connect 8112A trigger output to scope trigger input.

0160-4380

Connect the 10017A probe via a 1pF capacitor to the cathode of CR53.
Adjust A30C54 for a signal as shown in the following photo:



on disk
Ext Clock DISABLED

Connect the 8112A output signal via a 50 ohm feedthrough to the EXT INPUT BNC on 8175A front panel.
Connect the 10017A probe via a 1pF capacitor (as previously) to cathode of CR51
Adjust A3057 for a signal as shown in previous photo.

5. EXT INPUT Thresholds

Set 8112A:

PER	20 ns
DTY	50%
HIL/LOL	+0.150 V/-0.150V

Set 8175A:
Same as before plus:
External Input Threshold [+] 0.0V

Connect 10017A Probe to TP16, and measure signal on scope.
Adjust A30R61 for the best possible Square Wave Signal.

STEP 5 EXT INPUT THRESHOLD

best possible square wave

A30 C54 50 MHZ

Ø V 300mv around Ø V

TP16 A30R61

set threshold

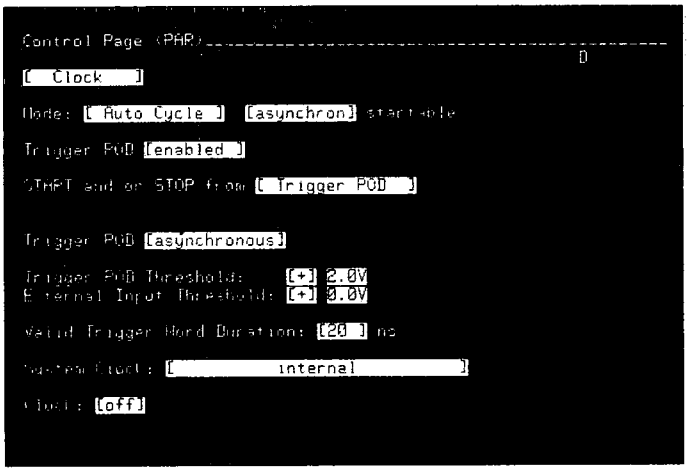
6. FILTERS

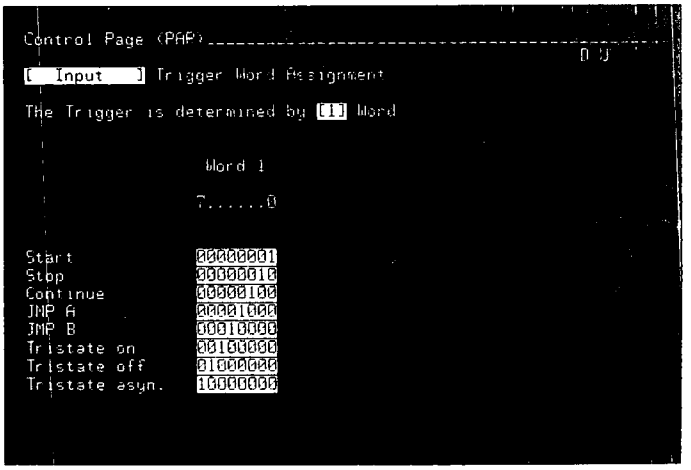
6a. Trigger Filter

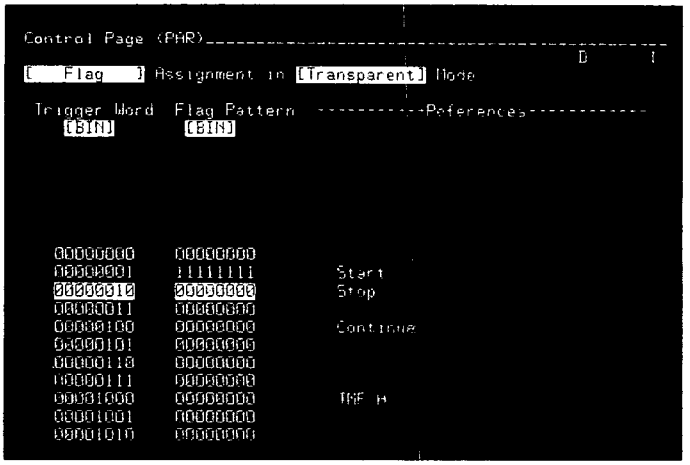
Set 8112A:

PER	1us
HIL	+4V
WID	20ns
LOL	0.0V

Set 8175A:
Recall Standard Settings.
Set the following three menus as shown:





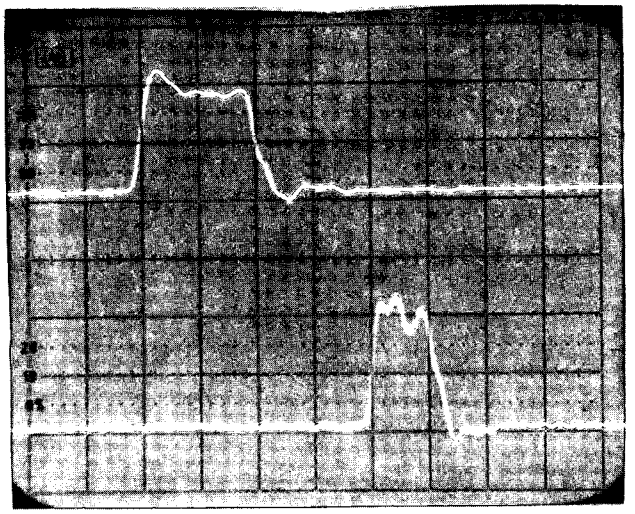


Set Scope:
Time/Div 100ns x 10
Ext. Trigger
Chop
CHA/CHB 50mV/Div

Connect the 8112A output to the Input Pod (15463A) CH0.
Connect 10017A Probe CHA to TP3 and 10017A Probe CHB to TP5.
Measure at TP3 for a signal with a pulse width of 20 ns (see photo below). If necessary, change 8112A WID slowly.

TP3

TP5



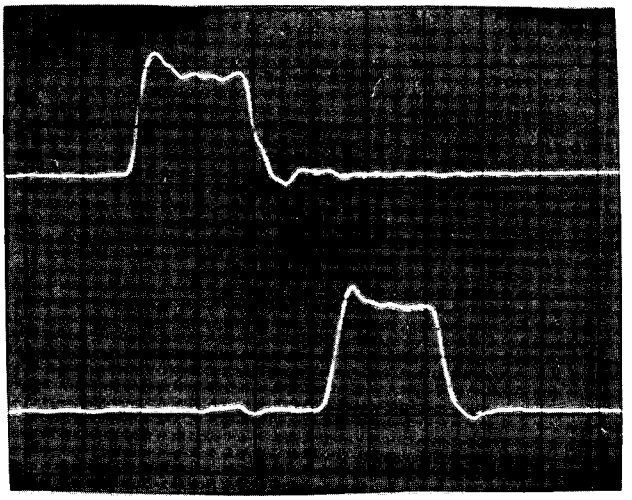
Turn A30R10 fully CW.
Adjust R10 slowly CCW until a stable signal (TP5) is displayed, see photo above.
Note: If 8112A output signal width is too small, no signal can be produced.

6b. Flag Filter

Connect CHB to TP13.
Turn A30R24 CW.
Adjust R24 slowly CCW until the signal becomes unstable, then turn CW until the signal becomes stable again (see photo below).

TP3

TP13



7. Master Clock Calibration

Set 8175A:
Control Page (PAR)
Mode: [Auto Cycle] [synchron] startable

Set Counter: FREQA, AC

Connect DVM to TP10.

Connect 8175A via an HP-IB cable to a controller (e.g., series 200 9826A/36A etc) and input the following program:
Output 7xx; "HW0,33,YYY" > EXECUTE

* 7xx = 8175A HP-IB Address
* YYY is a numeric value between 170 and 220.

Measure at TP10 while setting different values for YYY until a DVM reading as shown is produced:

+1.2V +-50mV.

Connect counter via probe 10017A to TP8.
Adjust the Master Clock via A30R99 for 99.9MHz +/- 0.05MHz.

5-8 DATA BOARD

Equipment:

DVM, Scope, 10017A 2x Pulse Generator 8112A

Procedure:

Check with DVM at following TP's for voltages as listed:

TP -5V	-5.1V	± 50 mV
TP +5V	+5.0V	± 50 mV
TP -0.7V	-0.7V	± 100 mV
TP -1.3V	-1.3V	± 100 mV

Latch/Data Timing Adjust:

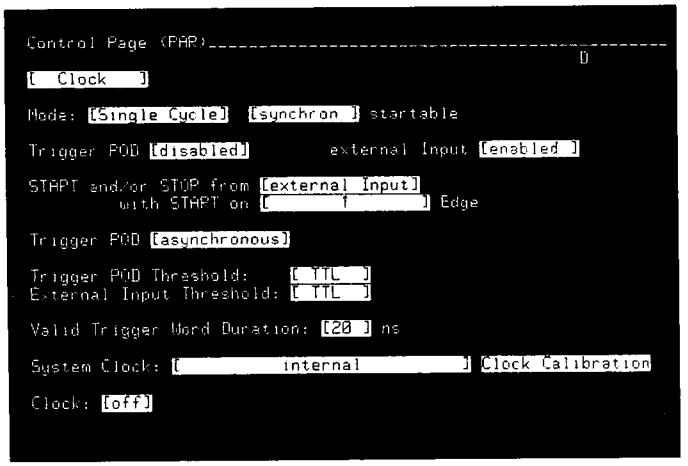
Set 8175A:
Recall Standard Settings. Note the details of the following menus, set same data/conditions as shown (remember to do an "Update"!):

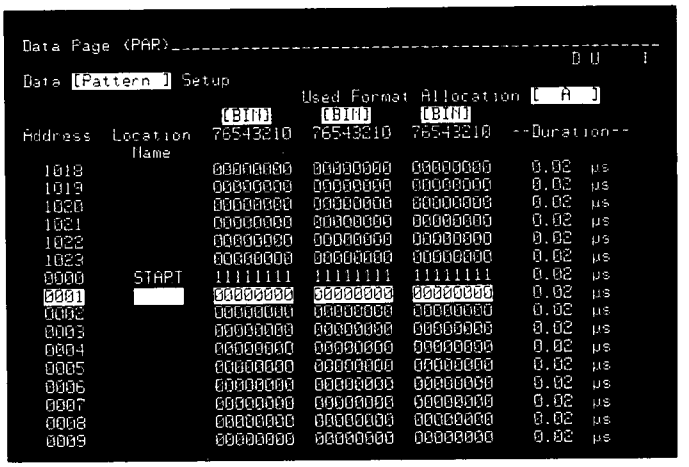
Set Scope:
Time 50 ns/Div x 10 Range
CHA/CHB 50 mV/Div, DC

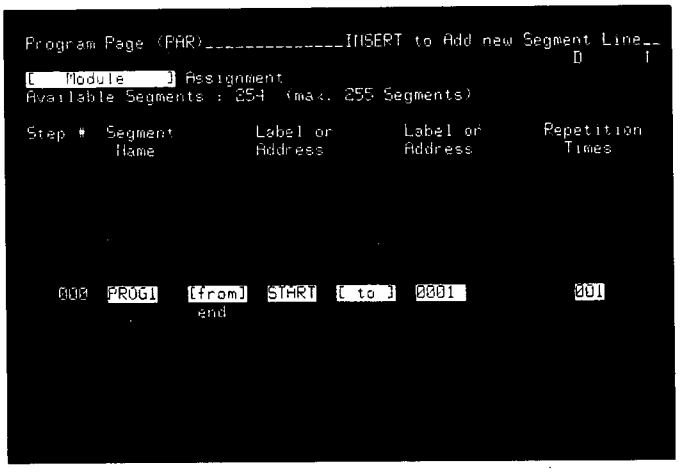
Set 8112A:

PER 1 us	HIL	+2V
WID 30 ns	LOL	0.0V
/ (Lin.)	LEE/TRE	10ns

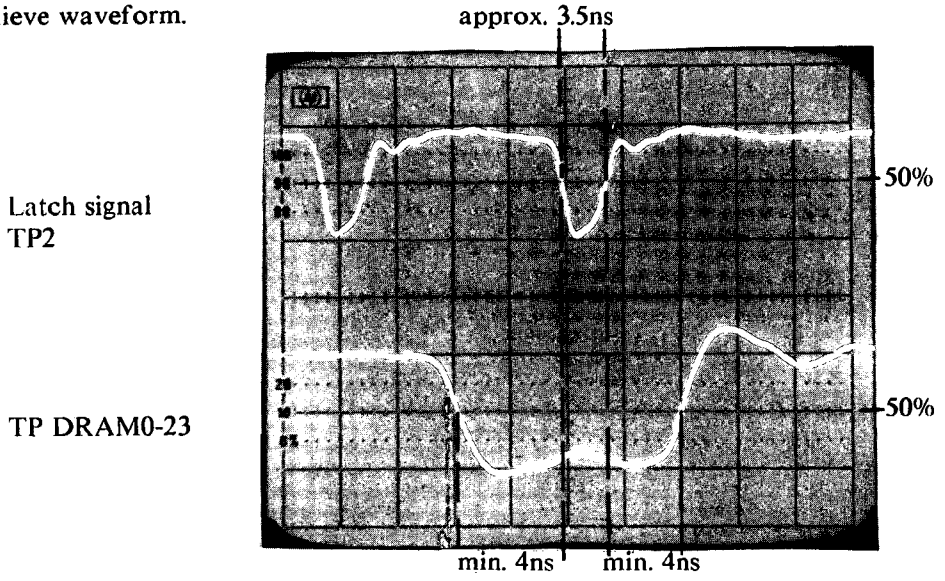
Connect 8112A (without 50 Ω feedthrough) to the EXT INPUT BNC of 8175A. Connect 8112A Trigger output to scope trigger input.







Connect scope CHA via 10017A Probe to A40 TP2. Check (via 10017A probe and CHB) at TP's DRAM0-23 that waveform as shown in following photo is produced. Adjust W1-W5 as necessary to achieve waveform.

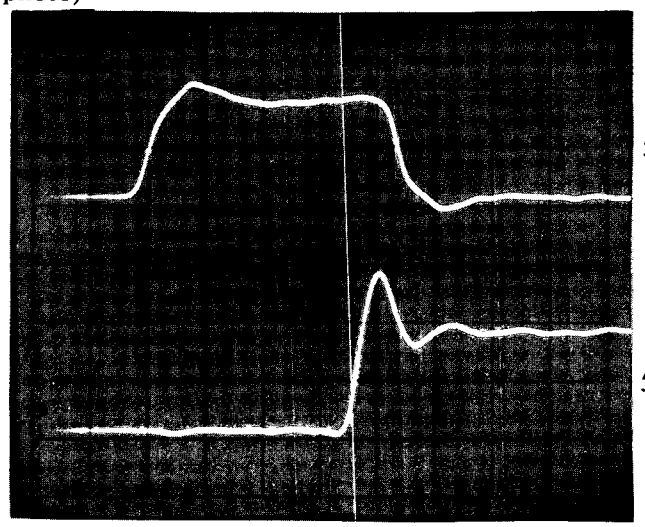


W1 = Signal LATCH delayed 1.5 ns
W2 = Signal LATCH undelayed
W3 = Signal PADDCLK2 undelayed
W4/W5 = Signal PADDCLK2 delayed 4.5 ns

Same settings as before:

Connect CHA to A40 TP12
Connect CHB to A40 TP11

Turn A40R88 fully CW
Adjust A40R66 for a delay of 18 ns ± 0.5 ns
pos. edge of TP12 signal to
pos. edge of TP11 signal (see photo)



5.9 FINE TIMING BOARD (OPTION 001)

Equipment: Scope, Time Mark Generator

Procedure:

Set 8175A:
Recall Standard Settings and set data etc. as follows:

SYSTEM > NEXT = [Storage] > CURSOR↓ = [store] > NEXT = [recall] Standard Settings > EXEC

CNTRL > CURSOR↓ = [Single Cycle] > NEXT = [Auto Cyle] > CURSOR↓ = Clock [off] > NEXT = [on] > CURSOR→ = 0.02 > 0.10 >
OUTPUT = [disabled] > NEXT = [enabled] > DATA > CURSOR↓ = Data Format Label A > blue > SYSTEM = INSERT > F > CURSOR→ = POD0 CH3 > NEXT 4x = **** >
DATA > NEXT = Data [Pattern Setup] > CURSOR↓ = Used Format Allocation [A] > NEXT = [F] > CURSOR↓ = Address 0000 > CURSOR→ > 1111 1111 (Address 0001) > PRGM > CURSOR↓ = PROG1 > CURSOR→ = 1023 > 0004 >
blue > EXEC = UPDATE > START

Scope settings:
Using the Time Mark Generator, check the oscilloscope time base accuracy in the 0.02 usec/Div x 10 Range. Note error and take time base error into account.
Connect Flag Pod channel 7 to oscilloscope ext. Trigger Input.

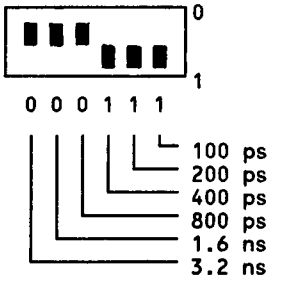
1. Switch 8175A TIMING = [Fine Timing off].
   Connect e.g. POD0 CH0 to channel A of scope. Set the leading edge of this signal (50% point of amplitude) to left of graticule as reference.

2. Switch 8175A on Timing Page (PAR) NEXT = [Fine Timing on].
   Check on scope for a Delay of 20 ns ± 200 ps.

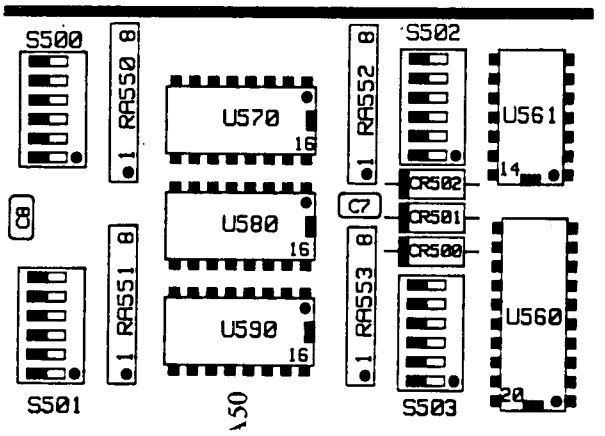
3. Adjust A50 S0 to get the best solution. After each new setting of S0, press NEXT 2x.

4. Repeat step 1 to 3 for:

POD0 CH1	adjust	S502
POD0 CH2	adjust	S501
POD0 CH3	adjust	S503



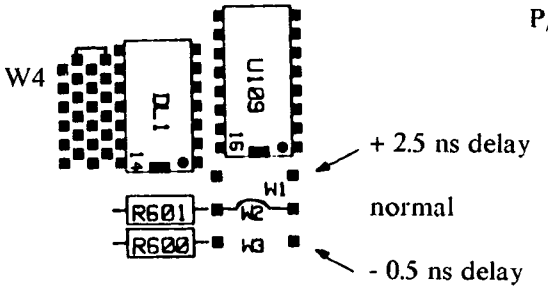
e.g. of 700 ps delay time settings



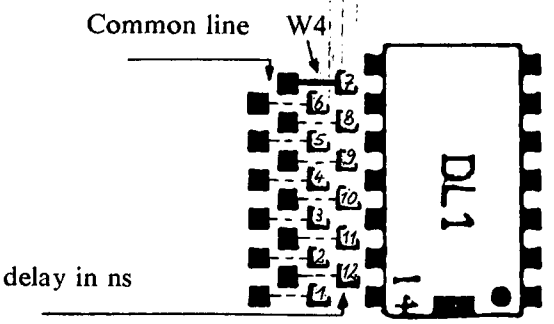
P/O A50

Make sure that the max. switched in delay time is ⩽ 5.5 ns.

5. If the 20 ns delay for CH0 to CH3 cannot be achieved, the soldered in wire links (W1 - W4) can be repositioned as required. (see diagram below)



P/O A50



6. With [Fine Timing on], connect POD0 CH0 to scope CHA. Set the leading edge of this signal (50% point of amplitude) to center of graticule as reference.

7. Connect in turn: POD0 CH1, CH2 and CH3 and check for max. skew of:
   ⩽ 6 ns with ECL POD
   ⩽ 7 ns with TTL/CMOS POD.

5-10 DISPLAY SYSTEM ADJUSTMENTS

NOTE

This adjustment procedure is in two parts: yoke and display driver. The Yoke Adjustment Procedure must be performed if any part of the Display System is replaced (CRT, display driver, or yoke) or if a dispaly cannot be aligned on the CRT screen. If the Yoke Adjustment Procedure is performaed, then the Display Driver Adjustment Procedure must also be done. If not done, then the latter may be done alone. It is good practise to discharge the CRT before beginning.

YOKE ADJUSTMENT PROCEDURE

a. Turn OFF 8175A.

b. Insure that the yoke is firmly pressed against the flange of the CRT. If not, loosen the yoke neck screw that attaches the yoke to the CRT and slide the yoke against the CRT. Gently tighten the screw until firm.

c. While holding a flexible straight edge from the lower-left corner to the upper-right corner of the CRT (facing the CRT), make a mark about one inch long with a water soluble felt pen across the center of the CRT. See Figure 5-2.

d. Repeat the above step for the upper-left corner and the lower-right corner forming an "X" in the center of the CRT. See Figure 5-2.

e. Adjust BRIGHTNESS control pot to minimum (full counter-clockwise). See Figure 5-3 for the display adjustment locations.

f. Remove the two yoke connectors.

g. Turn ON the 8175A.

h. Wait a short time, adjust BRIGHTNESS control pot until a dot appears on the CRT.

i. The dot should appear within a •3cm (1/8 inch) radius of the intersection of two lines. If this does not occur, align the dot using the centering rings on the yoke. See Figure 5-2.

j. Adjust the horizontal/vertical position by rotating the centering rings on the yoke.

k. Adjust VERT PHASE to vertically align the dot.

l. Turn OFF the 8175A and clean the CRT screen with mild soap and water.

m. Reconnect the two yoke connectors to the display driver.

h. Perform the Display Driver Adjustment Procedure.

DISPLAY DRIVER ADJUSTMENT PROCEDURE

a. Turn ON the 8175A.
Note, The +15V Video on the Power Supply Board must be adjusted correctly prior to making the following adjustments. Any susequent change to it will influence the following adjustments!

b. Adjust the BRIGHTNESS control pot until System Page is visible.

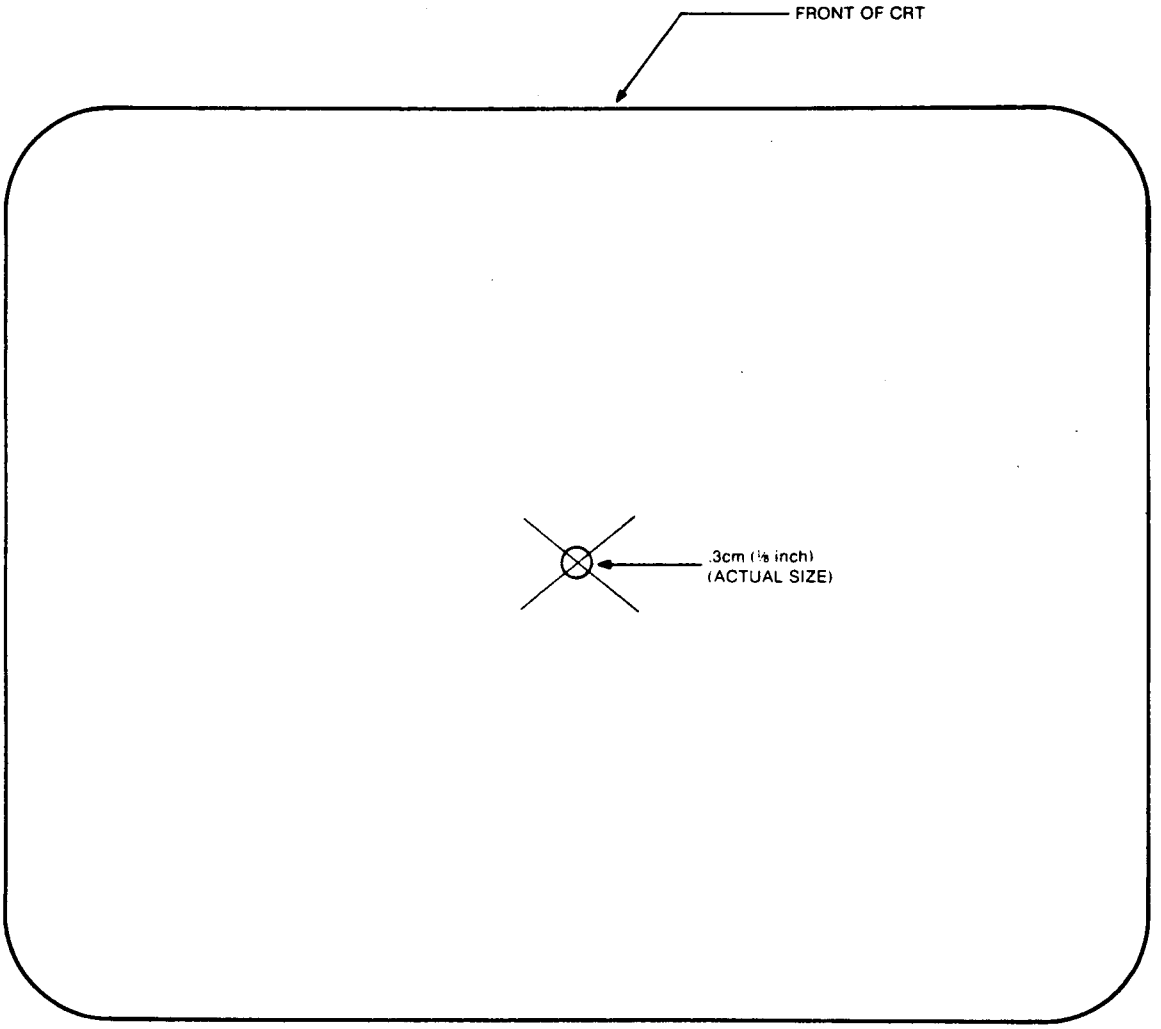


Figure 5-2. Yoke Centering Adjustment

c. Set 8175A: Data page Data [Waveform] Setup.

d. Adjust the VERT PHASE (position) until the Page lies symetrically positioned about the centre of the screen, with equal clearance top and bottom. Adjust the HEIGHT (gain) until the height of current display is approximately 111mm. See Figure 5-4.

e. Adjust HORIZ LINEARITY until the width of each column is the same.

f. Adjust HORIZ WIDTH until the complete display picture is positioned with equal "left and right" clearance. See Figure 5-4.

NOTE

The adjustments in step (e) and (f) interact. Therefore reiteration of these two steps may be necessary for best results.

g. Recheck, with the Data [Waveform] Setup menu displayed, steps i, j, and k of Yoke Adjustment Procedure. Ensure that the displayed menu is correctly positioned horizontally and vertically about the centre of the screen.

h. Adjust the BRIGHTNESS control for a comfortable CRT intensity level.

i. Set 8175A to the "Data [Pattern] Setup" Page. Adjust FOCUS control to archieve the best display.

j. Verify that the FLASHING CURSOR flashes at a rate of several times per second. If there are two different video levels but no flashing, the CPU board is defective. If there is no difference in video levels, the display board is defective. Refer to Service Block 2 for troubleshooting information.

k. The HOR HOLD adjustment has been pre-adjusted by the manufacturer and should not need to be changed.

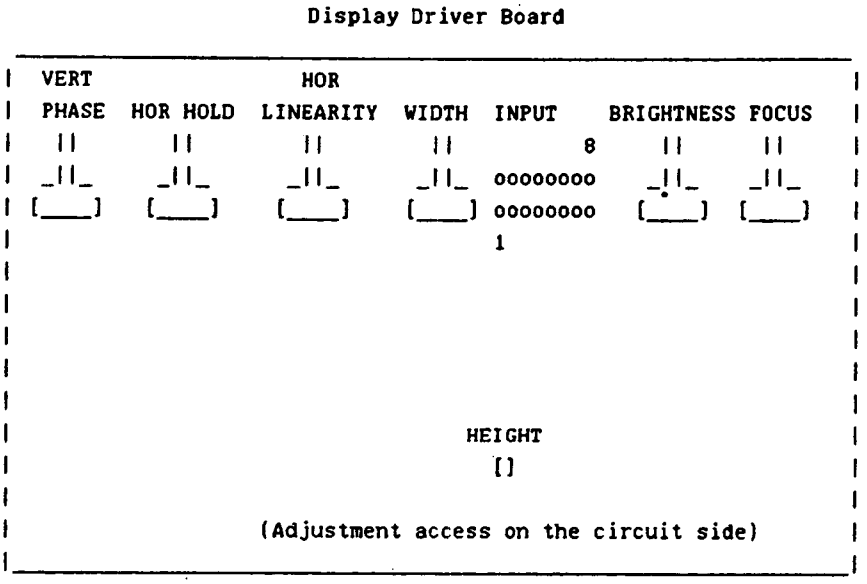


Figure 5-3. Display Adjustments Locations

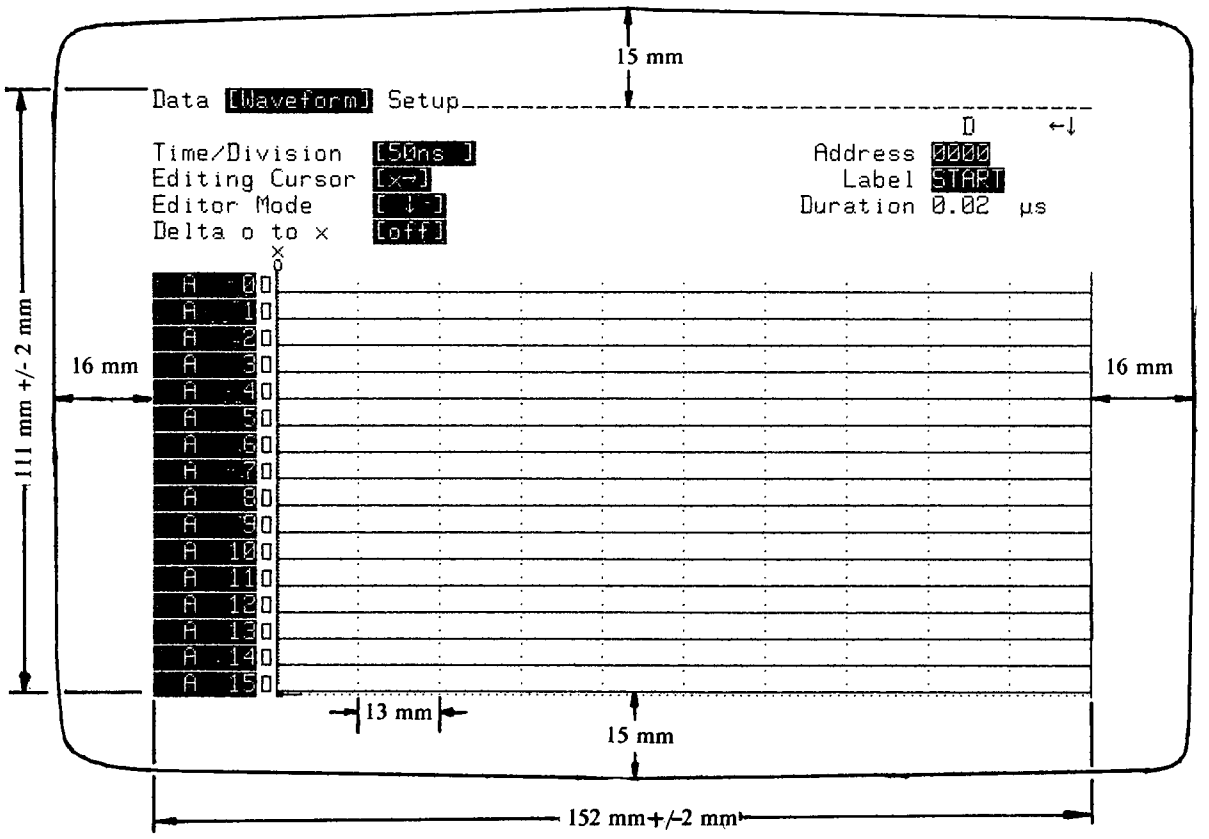
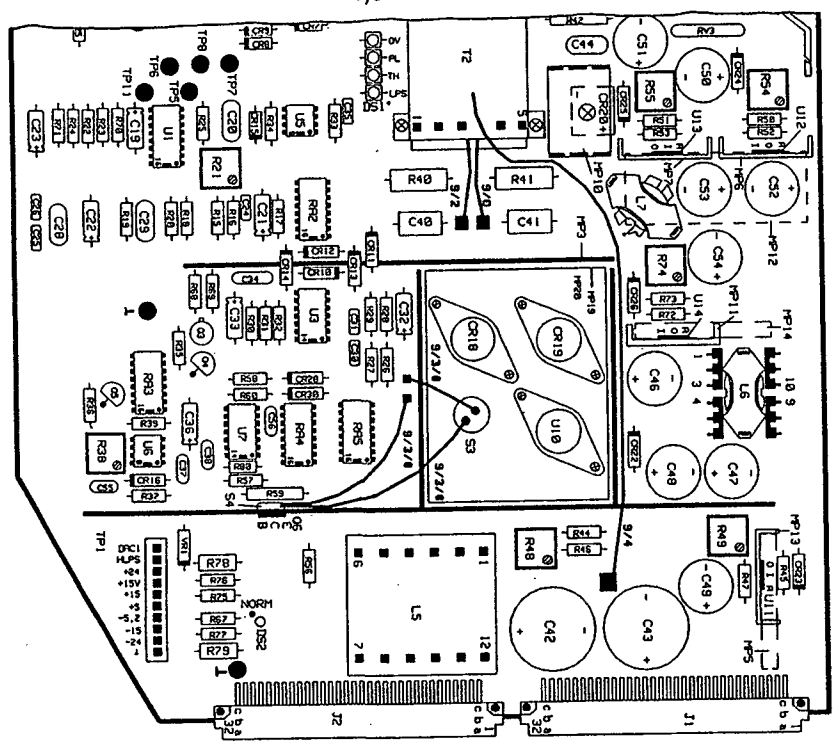


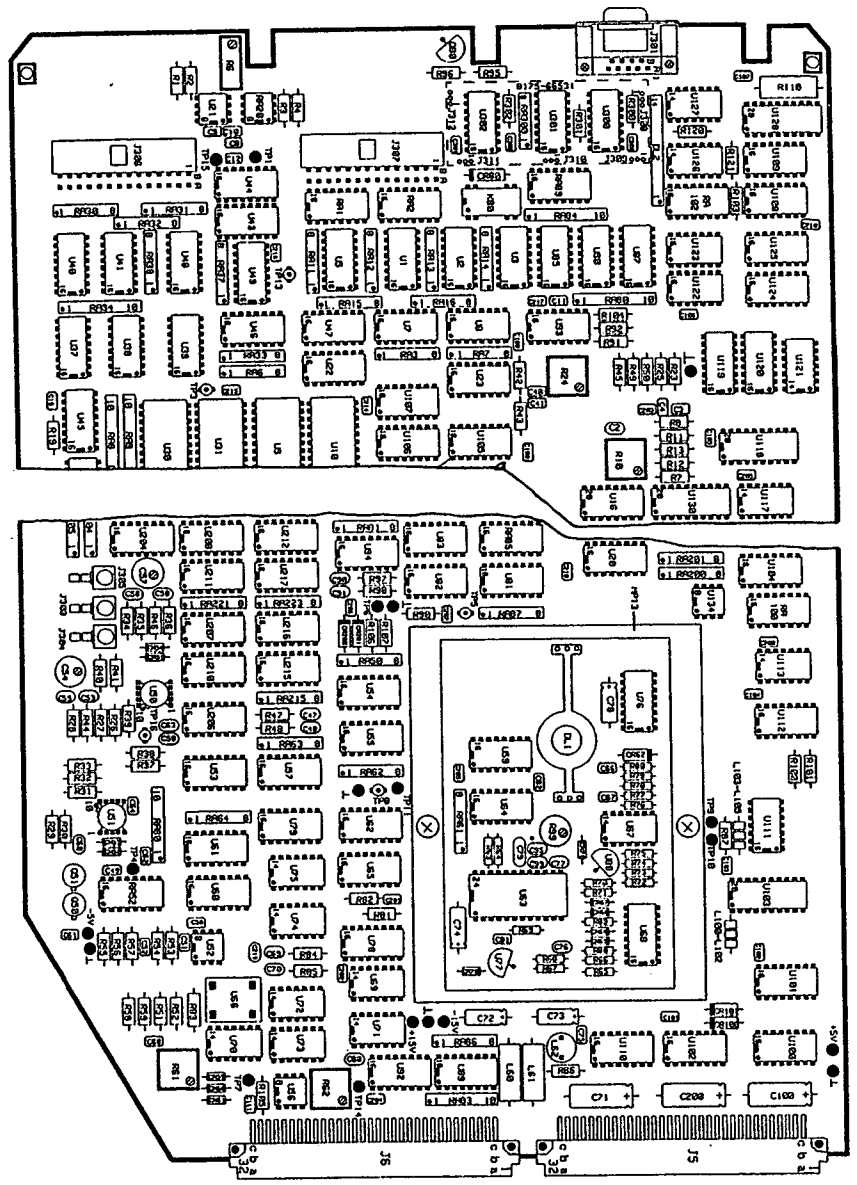
Figure 5-4. Display Adjustments Diagram

NOTE: All dimensions shown above are approximate.

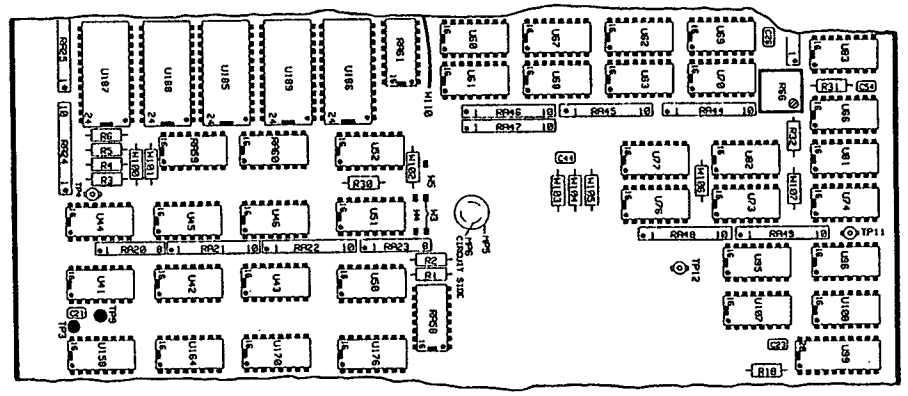
P/O A10 BD AY POWER SUPPLY 08175-66510



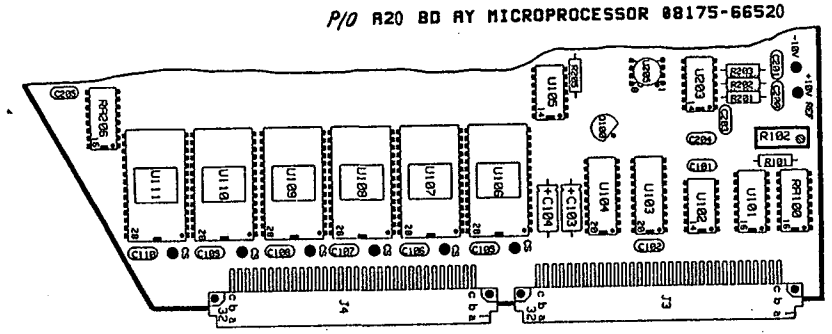
P/O A38 BD AY CLOCK 08175-66538



P/O A40 BD AY DATA 08175-66540



P/O A20 BD AY MICROPROCESSOR 08175-66520



P/O A50 BD AY FINE TIMING 08175-66552

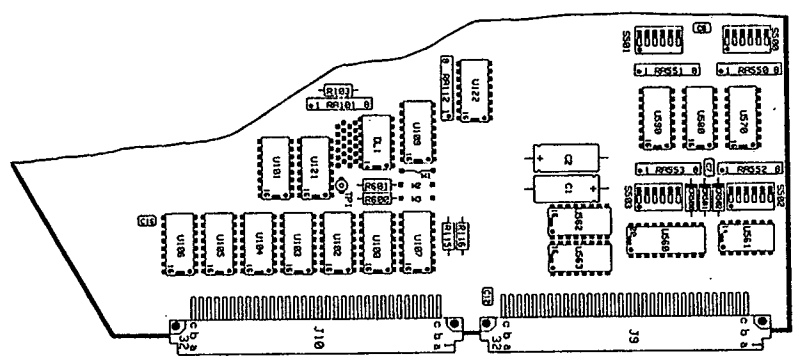


Figure 5-1. Adjustment Points Locator Diagram

SECTION 6

REPLACEABLE PARTS

6-1 INTRODUCTION

6-2 This section contains information for ordering parts. Table 6-1 lists abbreviations used in the parts list and elsewhere in the manual. Table 6-2 lists all replaceable parts in reference designator order.

6-3 ABBREVIATIONS

6-4 Table 6-1 lists abbreviations used in the parts lists, schematics and elsewhere in the manual. In some cases two forms of the abbreviation are used, one all in capital letters and one partial or no capitals. This occurs because the abbreviations in the parts list are always all capitals. However, in the schematics and other parts of the manual, the same abbreviations may have both lower and upper case letters.

6-5 REPLACEABLE PARTS

6-6 Table 6-2 is a list replaceable parts and is organized as follows:

a. Mainframe (chassis) parts in alpha-numerical order by reference designation.

b. Electrical assemblies and their components in alpha-numerical order by reference designation.

Reference designators are of the form A3R9 ie. resistor 9 on assembly 3.

The blue pages, at the end of the parts list, covers parts required for Option 001

6-7 The data given for each part is as follows:

a. Part number check digit
b. Hewlett-Packard part number
c. Item description

6-8 ORDERING INFORMATION

6-9 To order a part listed in the replaceable parts list, quote the Hewlett-Packard part number (with check digit), indicate the quantity required and address the order to the nearest Hewlett-Packard office (list of Sales/Service Offices at the rear of this manual). The check digit will ensure accurate and timely processing of the order.

6-10 To order a part that is not listed, include the instrument model number, serial number, a complete description of the part(s) required and the number of parts required. Address the order to the nearest Hewlett-Packard Sales/Service Office.

6-11 DIRECT MAIL ORDER SYSTEM (USA)

6-12 Within the USA, Hewlett-Packard can supply parts through a direct mail order system. Advantages of using the system are as follows:

a. Direct ordering and shipment from the HP Parts Center in Mountain View, California.

b. No maximum or minimum on any mail order (there is a minimum order amount for parts ordered through a local HP ofice when the parts require billing and invoicing).

c. Pre-paid transportation (there is a small handling charge f ,r each order).

d. No invoices - to provide these advantages, a check or money order must accompany each order.

6-13 Mail order forms and specific ordering information is available through the local HP office. Addresses and phone numbers are given at the back of this manual.

Table 6-1. Parts List Abbreviations

REFERENCE DESIGNATIONS

A . . . . . assembly
AT . . . attenuator; isolator; termination
B . . . . . fan; motor
BT . . . . . battery
C . . . . . capacitor
CP . . . . . coupler
CR . . . . . diode; diode thyristor; varactor
DC . . . directional coupler
DL . . . . . delay line
DS . . . . . annunciator; signaling device (audible or visual); lamp; LED
E . . . . . miscellaneous electrical part
F . . . . . fuse
FL . . . . . filter
H . . . . . hardware
HY . . . . . circulator
J . . . . electrical connector (stationary portion); jack
K . . . . . relay
L . . . . . coil; inductor
M . . . . . meter
MP . . . . . miscellaneous mechanical part
P . . . . electrical connector (movable portion); plug
Q . . . . . transistor: SCR; triode thyristor
R . . . . . resistor
RT . . . . . thermistor
S . . . . . switch
T . . . . . transformer
TB . . . . . terminal board
TC . . . . . thermocouple
TP . . . . . test point
U . . . . . integrated circuit; microcircuit
V . . . . . electron tube
VR . . . . voltage regulator; breakdown diode
W . . . . cable; transmission path; wire
X . . . . . socket
Y . . . . crystal unit (piezo-electric or quartz)
Z . . . . tuned cavity; tuned circuit

ABBREVIATIONS

A . . . . . ampere
ac . . . . alternating current
ACCESS . . . . . accessory
ADJ . . . . . adjustment
A/D. . . . . analog-to-digital
AF . . . . . audio frequency
AFC . . . . . automatic frequency control
AGC . . . . . automatic gain control
AL . . . . . aluminum
ALC . . . . automatic level control
AM . . . amplitude modulation
AMPL . . . . . amplifier
APC . . . . automatic phase control
ASSY. . . . . assembly
AUX . . . . . auxiliary
avg . . . . . average
AWG . . . . . American wire gauge
BAL . . . . . balance
BCD . . . . . binary coded decimal
BD . . . . . board
BE CU . . . . . beryllium copper
BFO . . . . beat frequency oscillator
BH . . . . . binder head
BKDN . . . . . breakdown
BP . . . . . bandpass
BPF. . . . . bandpass filter
BRS . . . . . brass
BWO . . . . backward-wave oscillator
CAL . . . . . calibrate
ccw . . . . counter-clockwise
CER . . . . . ceramic
CHAN . . . . . channel
cm . . . . . centimeter
CMO . . cabinet mount only
COAX . . . . . coaxial
COEF . . . . . coefficient
COM . . . . . common
COMP . . . . . composition
COMPL . . . . . complete
CONN . . . . . connector
CP . . . . . cadmium plate
CRT . . . cathode-ray tube
CTL . . . . complementary transistor logic
CW . . . . continuous wave
cw . . . . . clockwise
cm . . . . . centimeter
D/A. . . . digital-to-analog
dB . . . . . decibel
dBm . . . . decibel referred to 1 mW
dc . . . . . direct current
deg . . degree (temperature interval or difference)
. . ° . . . degree (plane angle)
°C . . . . . degree Celsius (centigrade)
°F . . . . degree Fahrenheit
°K . . . . . degree Kelvin
DEPC . . deposited carbon
DET . . . . . detector
diam . . . . . diameter
DIA . . . diameter (used in parts list)
DIFF AMPL . . . differential amplifier
div . . . . . division
DPDT . . . . . double-pole, double-throw
DR . . . . . drive
DSB . . . . double sideband
DTL . . . . diode transistor logic
DVM . . . . digital voltmeter
FCL . . . . emitter coupled logic
EMF . . electromotive force
EDP . . . . . electronic data processing
ELECT. . . . . electrolytic
ENCAP. . . . . encapsulated
EXT . . . . . external
F . . . . . farad
FET . . . . . field-effect transistor
F/F . . . . . flip-flop
FH . . . . . flatt head
FIL H . . . . . fillister head
FM . frequency modulation
FP . . . . . front panel
FREQ . . . . . frequency
FXD . . . . . fixed
g . . . . . gram
GE . . . . . germanium
GHz . . . . . gigahertz
GL . . . . . glass
GRD . . . . . ground(ed)
H . . . . . henry
h . . . . . hour
HET . . . . . heterodyne
HEX . . . . . hexagonal
HD . . . . . head
HDW . . . . . hardware
HF . . . . . high frequency
HG . . . . . mercury
HI . . . . . high
HP . . . . . Hewlett-Packard
HPF. . . . . high pass filter
HR . . . . . hour (used in parts list)
HV . . . . . high voltage
Hz . . . . . Hertz
IC. . . . . integrated circuit
ID. . . . . inside diameter
IF . . . . . intermediate frequency
IMPG . . . . . impregnated
in . . . . . inch
INCD . . . . . incandescent
INCL . . . . . include(s)
INP . . . . . input
INS . . . . . insulation
INT . . . . . internal
kg . . . . . kilogram
kHz . . . . . kilohertz
kΩ . . . . . kilohm
kV . . . . . kilovolt
lb . . . . . pound
LC . . . . . inductance-capacitance
LED . . light-emitting diode
LF . . . . . low frequency
LG . . . . . long
LH . . . . . left hand
LIM. . . . . limit
LIN . . . . linear taper (used in parts list)
lin . . . . . linear
LK WASH . . . lock washer
LO . . . low; local oscillator
LOG . . . logarithmic taper (used in parts list)
log . . . . . logarithm(ic)
LPF. . . . . low pass filter
LV . . . . . low voltage
m . . . . . meter (distance)
mA . . . . . milliampere
MAX . . . . . maximum
MΩ . . . . . megohm
MEG . . . . meg (10^6) (used in parts list)
MET FLM . . . . metal film
MET OX . . . metallic oxide
MF . . . medium frequency; microfarad (used in parts list)
MFR . . . . . manufacturer
mg . . . . . milligram
MHz . . . . . megahertz
mH . . . . . millihenry
mho . . . . . mho
MIN . . . . . minimum
min . . . . . minute (time)
' . . . . . minute (plane angle)
MINAT. . . . . miniature
mm . . . . . millimeter
MOD . . . . . modulator
MOM . . . . . momentary
MOS . . . . . metal-oxide semiconductor
ms . . . . . millisecond
MTG . . . . . mounting
MTR . . . meter (indicating device)
mV . . . . . millivolt
mVac . . . . . millivolt, ac
mVdc . . . . . millivolt, dc
mVpk . . . . millivolt, peak
mVp-p . . . millivolt, peak-to-peak
mVrms . . . . millivolt, rms
mW . . . . . milliwatt
MUX . . . . . multiplex
MY . . . . . mylar
μA . . . . . microampere
μF. . . . . microfarad
μH . . . . . microhenry
μmho. . . . . micromho
μs . . . . . microsecond
μV . . . . . microvolt
μVac . . . . . microvolt, ac
μVdc . . . . . microvolt, dc
μVp-p . . . microvolt, peak-to-peak
μVrms . . . . microvolt, rms
μW . . . . . microwatt
nA . . . . . nanoampere
NC . . . . . no connection
N/C . . . . . normally closed
NE . . . . . neon
NEG . . . . . negative
nF . . . . . nanofarad
NI PL . . . . . nickel plate
N/O . . . . normally open
NOM . . . . . nominal

NOTE

All abbreviations in the parts list will be in upper-case.

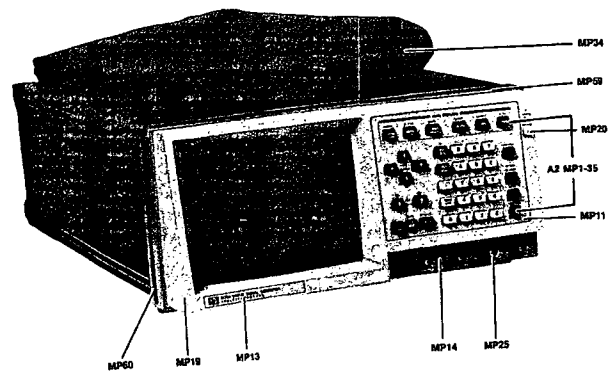
NORM . . . normal
NPN . . negative-positive-negative
NPO . . . negative-positive zero (zero temperature coefficient)
NRFR . . not recommended for field replacement
NSR . . . not separately replaceable
ns . . . nanosecond
nW . . . nanowatt
OBD . order by description
OD . . . outside diameter
OH . . . oval head
OP AMPL . . operational amplifier
OPT . . . option
OSC . . . oscillator
OX . . . oxide
oz . . . ounce
Ω . . . ohm
P . . . peak (used in parts list)
PAM . . . pulse-amplitude modulation
PC . . . printed circuit
PCM . . pulse-code modulation, pulse-count modulation
PDM . . . pulse-duration modulation
pF . . . picofarad
PH BRZ . phosphor bronze
PHL . . . Phillips
PIN . . . positive-intrinsic-negative
PIV . . . peak inverse voltage
pk . . . peak
PL . . . phase lock
PLO . . . phase lock oscillator
PM . . . phase modulation
PNP . . . positive-negative-positive
P/O . . . part of
POLY . . . polystyrene
PORC . . . porcelain
POS . . positive; position(s) (used in parts list)
POSN . . . position
POT . . . potentiometer
p-p . . . peak-to-peak
PP . . . peak-to-peak (used in parts list)
PPM . . . pulse-position modulation
PREAMPL . . preamplifier
PRF . . . pulse-repetition frequency
PRR . . . pulse repetition rate
ps . . . picosecond
PT . . . point
PTM . . . pulse-time modulation
PWM . . . pulse-width modulation
PWV . . . peak working voltage
RC . resistance-capacitance
RECT . . . rectifier
REF . . . reference
REG . . . regulated
REPL . . . replaceable
RF . . . radio frequency
RFI . . . radio frequency interference
RH . . . round head; right hand
RLC . . . resistance-inductance-capacitance
RMO . . rack mount only
rms . . . root-mean-square
RND . . . round
ROM . . read-only memory
R&P . . . rack and panel
RWV . . . reverse working voltage
S . . . scattering parameter
s . . . second (time)
" . . second (plane angle)
S-B . . . slow-blow (fuse) (used in parts list)
SCR . . . silicon controlled rectifier; screw
SE . . . selenium
SECT . . . sections
SEMICON . . . semiconductor
SHF . . . superhigh frequency
SI . . . silicon
SIL . . . silver
SL . . . slide
SNR . . signal-to-noise ratio
SPDT . . . single-pole, double-throw
SPG . . . spring
SR . . . split ring
SPST . . . single-pole, single-throw
SSB . . . single sideband
SST . . . stainless steel
STL . . . steel
SQ . . . square
SWR . . standing-wave ratio
SYNC . . . synchronize
T . . timed (slow-blow fuse)
TA . . . tantalum
TC . . . temperature compensating
TD . . . time delay
TERM . . . terminal
TFT . . thin-film transistor
TGL . . . toggle
THD . . . thread
THRU . . . through
TI . . . titanium
TOL . . . tolerance
TRIM . . . trimmer
TSTR . . . transistor
TTL . . transistor-transistor logic
TV . . . television
TVI . television interference
TWT . . traveling wave tube
U . . . micro (10^6) (used in parts list)
UF . . . microfarad (used in parts list)
UHF . . ultrahigh frequency
UNREG . . . unregulated
V . . . volt
VA . . . voltampere
V_{ac} . . . volts, ac
VAR . . . variable
VCO . . . voltage-controlled oscillator
Vdc . . . volts, dc
VDCW . . volts, dc, working (used in parts list)
V(F) . . . volts, filtered
VFO . . variable-frequency oscillator
VHF . . . very-high frequency
Vpk . . . volts, peak
Vp-p . . volts, peak-to-peak
Vrms . . . volts, rms
VSWR . . . voltage standing wave ratio
VTO . . . voltage-tuned oscillator
VTVM . . . Vacuum-tube voltmeter
V(X) . . . volts, switched
W . . . watt
W . . . with
WIV . . . working inverse voltage
WW . . . wirewound
W/O . . . without
YIG . . yttrium-iron-garnet
Z_o . . . characteristic impedance

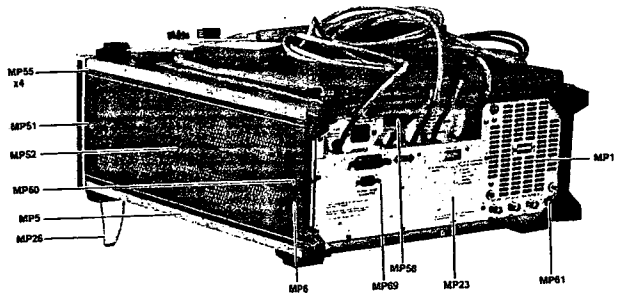
MULTIPLIERS

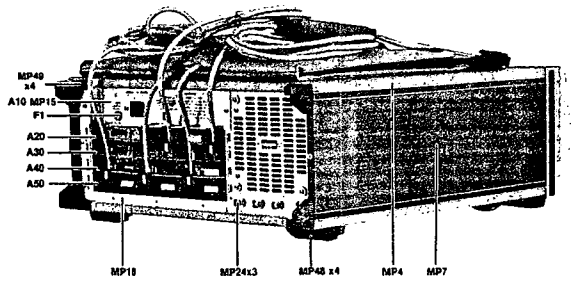
Abbreviation	Prefix	Multiple
T	tera	10^{12}
G	giga	10^{9}
M	mega	10^{6}
k	kilo	10^{3}
da	deka	10
d	deci	10^{-1}
c	centi	10^{-2}
m	milli	10^{-3}
μ	micro	10^{-6}
n	nano	10^{-9}
p	pico	10^{-12}
f	femto	10^{-15}
a	atto	10^{-18}

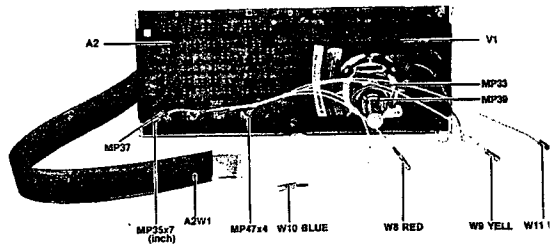
NOTE

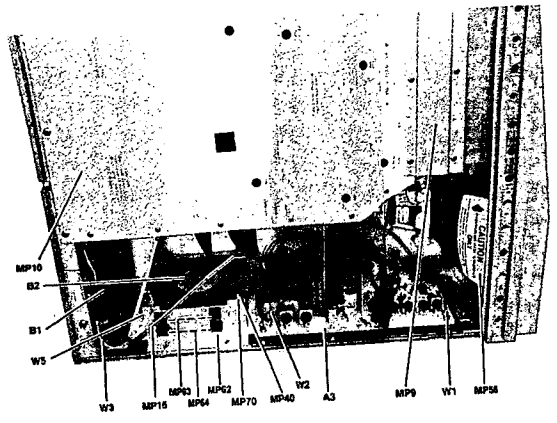
All abbreviations in the parts list will be in upper-case.

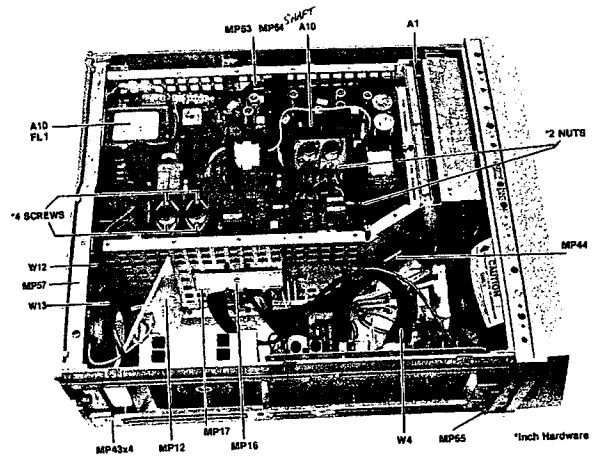












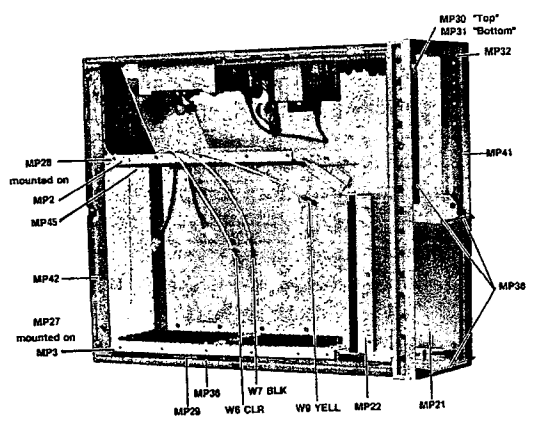


Figure 6-1. 8175A Mainframe Parts

REFERENCE DESIGNATOR	C D	H-P PART NUMBER	DESCRIPTION
FRAME			
A1	6	08175-66501	BD AY-MOTHER
A2	7	08175-66502	BD AY-KEY
A3	5	0950-0894	BD-AY DISPLAY
A10	7	08175-66510	BD AY-PWR SPPLY
A20	9	08175-66520	BD AY-CPU
A30	1	08175-66530	BD AY-CLOCK
A40	3	08175-66540	BD AY-DATA
A50	5	08175-66550	BD AY-BUFFER
		NOTE: See page 6-18 for A52 Fine Timing Bd. (Opt. 001) parts.	
B1	1	3160-0339	FAN-TBX 95/128V
B2	1	3160-0339	FAN-TBX 95/128V
F1	9	2110-0036	FUSE FB 8A 125V
MP1	4	08175-00119	PANEL REAR
MP2	8	08175-00139	BRACKET MIDDLE
MP3	0	08175-00149	BRACKET SIDE
MP4	2	08175-00183	CVR TOP CABINET
MP5	3	08175-00184	CVR BOTTOM CAB.
MP6	4	08175-00185	CVR SIDE W.HNDL
MP7	5	08175-00186	CVR SIDE PERFOR.
MP8	6	08175-00187	COVER BOTTOM
MP9	7	08175-00188	COVER TOP FRONT
MP10	8	08175-00189	COVER TOP
MP11	5	08175-00201	FRONT PANEL
MP12	3	08175-00639	SHIELD FAN
MP13	3	08175-00671	SHIELD FRONT
MP14	8	08175-01202	BNC BRACKET
MP15	1	08175-01205	BRACKET FAN
MP16	1	08175-01297	CBL CLAMP TOP
MP17	2	08175-01298	CBL CLAMP
MP18	3	08175-01299	BRACKET REAR
MP19	3	08175-42201	BEZEL FRONT
MP20	5	08175-47401	KEY CAP LINE
MP21	1	08175-60128	BRACKET FRONT 2
MP22	2	08175-60129	BRACKET FRONT
MP23	8	08175-60159	COVER REAR
MP24	1	1250-0083	CONN BNC BLKHD
MP25	3	1250-0118	CONN BNC BLKHD
MP26	5	1460-1345	TILT STAND
MP27	6	08175-03298	ADAPTER GROUND 2
MP28	7	08175-03299	ADAPTER GROUND 1
MP29	6	08175-04709	SUPPORT
MP30	7	08175-05097	CATCH FRAME TOP
MP31	8	08175-05098	CATCH FRAME BOTT
MP32	9	08175-05099	CATCH SIDE
MP33	8	9140-0720	YCKE
MP34	2	01630-84501	POUCH
MP35	8	2950-0001	NUT-HEX 318-32TH
MP36	8	0360-0244	TERM-LUG .070
MP37	5	0360-1190	TERM-LUG SLDR
MP38	0	0363-0125	CONTACT-FINGER
MP39	9	0460-0623	TAPE ELEC 1IN
MP40	8	0380-0599	SPACER
MP41	4	5021-5805	FRAME FRONT 177H
MP42	5	5021-5806	FRAME REAR 177H
MP43	2	5021-5837	STRUT CRNR 497.8
MP44	0	1400-0611	CLAMP CBL
MP45	4	08175-43101	GUIDE-PC BD
MP46	2	0403-0436	GUIDE CARD-PCA
MP47	0	08175-24701	SPACER BNC
MP48	8	5040-7201	FOOT
MP49	2	5040-7221	FOOT REAR
MP50	7	5041-6820	CAP STP HNDL RR
MP51	4	5041-6819	CAP STP HNDL FNT
MP52	3	5060-9804	STRAP HDL 497.8D
MP53	1	5040-9317	SHAFT-POWER-SW
MP54	1	5040-1149	SHAFT-LONG/GRAY
MP55	4	8160-0428	RFI ROUND STRIP
MP56	5	7121-4002	LBL-CRT CAUTION
MP57	3	7120-6264	LABEL-WARNING
MP58	5	7121-2527	LABEL METR &INCH
MP59	9	5040-7202	TRIM STRIP-TOP
MP60	1	5001-0440	TRIM-STRIP SIDE
MP61	3	6960-0001	BTN PLUG .5 DIA
MP62	2	08175-01206	BRACKET FAN TOP
MP63	4	08175-45008	EXTRACTOR RIGHT
MP64	5	08175-45009	EXTRACTOR LEFT
MP65	2	0403-0410	GUIDE PC BD BLK
MP66	6	0403-0406	GUIDE-PC BD
MP67	8	0403-0101	GUIDE PC BD WHT
MP68	9	0403-0269	GD-PC BLK 6.0-LG
MP69	7	1251-2942	CONN-LOCK R&P
MP70	2	0400-0193	GROM-SPCL .221
V1	1	2090-0066	TUBE ELECTRON
W1	2	8150-0005	WIRE 22 BLK
W2	0	8150-0102	WIRE 18 BLK
W3	5	8150-3284	WIRE 18 GRN/YEL
W4	1	08175-61605	CBL RIBBON 16CON
W5	5	8150-3284	WIRE 18 GRN/YEL
W6	8	08175-61608	CBL SMB/BNC
W7	8	08175-61609	CBL SMB/BNC
W8	8	08175-61610	CBL SMB/BNC
W9	8	08175-61611	CBL SMB/BNC
W10	8	08175-61612	CBL SMB/BNC
W11	8	08175-61613	CBL SMB/BNC
W12	9	08175-61614	CBL AY FAN
W13	9	08175-61615	CBL AY FAN LONG

REFERENCE DESIGNATOR		C D	H-P PART NUMBER	DESCRIPTION
A1	08175-66501			BD AY-MOTHER
A1	J1	9	1251-7796	CONN-POST-TP-SKT
A1	J2	9	1251-7796	CONN-POST-TP-SKT
A1	J3	9	1251-7796	CONN-POST-TP-SKT
A1	J4	9	1251-7796	CONN-POST-TP-SKT
A1	J5	9	1251-7796	CONN-POST-TP-SKT
A1	J6	9	1251-7796	CONN-POST-TP-SKT
A1	J7	9	1251-7796	CONN-POST-TP-SKT
A1	J8	9	1251-7796	CONN-POST-TP-SKT
A1	J9	9	1251-7796	CONN-POST-TP-SKT
A1	J10	9	1251-7796	CONN-POST-TP-SKT
A1	J11	9	1251-7796	CONN-POST-TP-SKT
A1	J12	9	1251-7796	CONN-POST-TP-SKT
A1	J13	7	1252-0027	CONN-DIN TYPE
A1	J14	7	1252-0027	CONN-DIN TYPE
A1	RA1	2	1810-0325	R-NETWORK DIP
A1	RA2	2	1810-0325	R-NETWORK DIP
A1	RA3	2	1810-0325	R-NETWORK DIP
A1	RA4	2	1810-0325	R-NETWORK DIP
A1	RA5	2	1810-0325	R-NETWORK DIP
A1	RA6	2	1810-0325	R-NETWORK DIP
A1	RA7	2	1810-0325	R-NETWORK DIP
A1	RA8	2	1810-0325	R-NETWORK DIP
A2	08175-66502			BD AY-KEY
A2	CR1	5	1990-0485	LED VISIBLE GRN
A2	CR2	5	1990-0485	LED VISIBLE GRN
A2	CR3	5	1990-0485	LED VISIBLE GRN
A2	CR4	5	1990-0485	LED VISIBLE GRN
A2	J21	0	8159-0005	RES ZERO OHMS
A2	J22	0	8159-0005	RES ZERO OHMS
A2	J23	0	8159-0005	RES ZERO OHMS
A2	J24	0	8159-0005	RES ZERO OHMS
A2	J25	0	8159-0005	RES ZERO OHMS
A2	J26	0	8159-0005	RES ZERO OHMS
A2	J27	0	8159-0005	RES ZERO OHMS
A2	MP1	1	5041-2781	KEY CAP-SYSTEM
A2	MP2	3	5041-4531	KEY, HALF CNTL
A2	MP3	9	5041-4529	KEY, HALF TIMING
A2	MP4	4	5041-4532	KEY, HALF OUTPUT
A2	MP5	2	5041-4530	KEY, HALF DATA
A2	MP6	2	5041-1693	PRGM CAP
A2	MP7	6	5041-2778	KEY CAP-NEXT
A2	MP8	5	5041-0903	KEY CAP D
A2	MP9	4	5041-2784	KEY CAP-E
A2	MP10	5	5041-2785	KEY CAP-F
A2	MP11	7	5041-4535	KEY, HALF START
A2	MP12	5	5041-2777	KEY CAP-PREV
A2	MP13	2	5041-0900	KEY CAP A
A2	MP14	3	5041-0901	KEY CAP B
A2	MP15	4	5041-0902	C CAP
A2	MP16	7	5041-0905	.-CAP
A2	MP17	7	5041-0913	KEY CAP 7
A2	MP18	8	5041-0914	KEY CAP 8
A2	MP19	9	5041-2789	KEY CAP-STOP
A2	MP20	3	5041-2783	KYCP-DON'T CARE
A2	MP21	4	5041-0910	KEY CAP 4
A2	MP22	5	5041-0911	KEY CAP 5
A2	MP23	6	5041-0912	KEY CAP 6
A2	MP24	5	5041-4533	KEY, SINGLE STEP
A2	MP25	8	5041-0906	KEY CAP 0
A2	MP26	9	5041-0907	KEY CAP 1
A2	MP27	0	5041-0908	KEY CAP 2
A2	MP28	1	5041-0909	KEY CAP 3
A2	MP29	6	5041-4534	KEY, HALF DISABL
A2	MP30	8	5041-4528	KEY, HALF EXEC
A2	MP31	3	5041-2791	KYCP-CLEAR ENTRY
A2	MP32	6	5041-0433	KEY CAP-BLUE
A2	MP33	2	5041-2782	KYCP-ARROW UP LT
A2	MP34	6	5041-2786	KYCP-ARROW SIDE
A2	MP35	7	5041-2787	KYCP-ARROW UP DK
A2	S1- S39	2	3101-2603	SW-PB SPST NO
A2	W1	0	08175-61604	CBL RIBBON 20CON
A10	08175-66510			BD AY-PWR SPPLY
A10	C1	1	0160-4962	C-F 1.0UF 200V
A10	C2	7	0180-3687	C-F 1000UF 200V
A10	C3	7	0180-3687	C-F 1000UF 200V
A10	C4	4	0160-4048	C-F .022UF 250V
A10	C5	8	0160-5347	C-F 1UF 10% 400V
A10	C6	6	0160-6054	C-F 1.5UF 10%
A10	C7	6	0160-6054	C-F 1.5UF 10%
A10	C8	5	0140-0180	C-F .002UF 300V
A10	C9	9	0160-4209	C-F .010UF 20%
A10	C10	9	0160-4209	C-F .010UF 20%
A10	C11	9	0180-2946	C-F 330UF 35V AL
A10	C12	3	0180-0291	C-F 1UF 35V
A10	C13	3	0180-0291	C-F 1UF 35V
A10	C14	0	0160-4812	C-F 220PF 100V5%
A10	C15	4	0160-4808	C-F 470PF 100V
A10	C16	4	0160-4808	C-F 470PF 100V
A10	C17	3	0180-0291	C-F 1UF 35V
A10	C18	3	0180-0291	C-F 1UF 35V
A10	C19	3	0180-0291	C-F 1UF 35V
A10	C20	2	0160-4426	C-F .01UF 1%
A10	C21	3	0180-0291	C-F 1UF 35V
A10	C22	3	0180-0291	C-F 1UF 35V
A10	C23	3	0180-0291	C-F 1UF 35V
A10	C24	9	0160-4209	C-F .010UF 20%
A10	C25	9	0160-4209	C-F .010UF 20%
A10	C26	9	0160-4209	C-F .010UF 20%
A10	C28	6	0160-0155	C-F 3300PF PLAST
A10	C29	2	0160-4822	C-F 1000P 100V
A10	C30	9	0160-4209	C-F .010UF 20%
A10	C31	9	0160-4209	C-F .010UF 20%
A10	C32	3	0180-0291	C-F 1UF 35V
A10	C33	3	0180-0291	C-F 1UF 35V
A10	C34	7	0160-4819	C-F 2200PF 5%
A10	C35	9	0160-4209	C-F .010UF 20%
A10	C36	0	0180-2690	C-F 3.3UF 15V
A10	C37	1	0160-5746	C-F 0.1UF 20%
A10	C38	9	0160-5728	C-F 1000PF 5%
A10	C40	7	0160-0164	C-F .039UF PLAST
A10	C41	7	0160-0164	C-F .039UF PLAST
A10	C42	7	0180-2704	C-F 5600UF 6.3V
A10	C43	7	0180-2704	C-F 5600UF 6.3V
A10	C44	7	0160-4819	C-F 2200PF 5%
A10	C45	7	0160-4819	C-F 2200PF 5%
A10	C46	2	0180-2733	C-F 470UF 25V
A10	C47	2	0180-2733	C-F 470UF 25V

REFERENCE DESIGNATOR		C D	H-P PART NUMBER	DESCRIPTION
A10	C48	2	0180-2733	C-F 470UF 25V
A10	C49	2	0180-2733	C-F 470UF 25V
A10	C50	5	0180-0582	C-F 270UF 40V
A10	C51	5	0180-0582	C-F 270UF 40V
A10	C52	5	0180-0582	C-F 270UF 40V
A10	C53	5	0180-0582	C-F 270UF 40V
A10	C54	2	0180-2733	C-F 470UF 25V
A10	C55	9	0160-0174	C-F .47UF 25VCER
A10	C56	2	0160-5747	C-F .047UF 20%
A10	CR1	3	1906-0224	DIO-FW BRDG 600V
A10	CR2	1	1901-0719	DIO-PWR 400V 3A
A10	CR3	1	1901-0719	DIO-PWR 400V 3A
A10	CR4	9	1906-0006	DIO MULT SI 400
A10	CR5	5	1901-0028	DIO 400C .75A
A10	CR7	3	1901-0050	DIO SW 80V 200MA
A10	CR8	3	1901-0050	DIO SW 80V 200MA
A10	CR9	3	1901-0050	DIO SW 80V 200MA
A10	CR10	3	1901-0050	DIO SW 80V 200MA
A10	CR11	3	1901-0050	DIO SW 80V 200MA
A10	CR12	3	1901-0050	DIO SW 80V 200MA
A10	CR13	3	1901-0050	DIO SW 80V 200MA
A10	CR14	3	1901-0050	DIO SW 80V 200MA
A10	CR15	3	1901-0050	DIO SW 80V 200MA
A10	CR16	3	1901-0050	DIO SW 80V 200MA
A10	CR17	4	1906-0051	DIO-FW BRDG 100V
A10	CR18	7	1906-0278	DIODES
A10	CR19	0	1906-0239	DIO-CR-RECT 45V
A10	CR20	6	1906-0079	DIO-FW BRDG 10A
A10	CR21	6	1906-0079	DIO-FW BRDG 10A
A10	CR22	7	1901-0731	DIO-PWR 400V 1A
A10	CR23	7	1901-0731	DIO-PWR 400V 1A
A10	CR24	7	1901-0731	DIO-PWR 400V 1A
A10	CR25	7	1901-0731	DIO-PWR 400V 1A
A10	CR26	7	1901-0731	DIO-PWR 400V 1A
A10	CR28	3	1901-0050	DIO SW 80V 200MA
A10	CR30	3	1901-0050	DIO SW 80V 200MA
A10	DS1	8	1990-0652	LED
A10	DS2	5	1990-0485	LED VISIBLE GRN
A10	E1	8	1970-0050	TUBE,VOLTAGE PRO
A10	E2	8	1970-0050	TUBE,VOLTAGE PRO
A10	F1	2	2110-0055	FUSE 4 AMP NB
A10	FL1	3	9135-0255	FILTER-LINE
A10	J1	2	1251-7799	3X32 PLUG
A10	J2	2	1251-7799	3X32 PLUG
A10	J3	6	1251-7826	CONN-POST 2 CONT
A10	L1	2	9100-4192	XFMR-BALN
A10	L2	1	9140-0624	IDCTR 270UH 10%
A10	L3	5	9100-1612	COIL CHOKE .33UH
A10	L4	5	9100-1612	COIL CHOKE .33UH
A10	L5	4	08175-61103	CHOKE 43uH 28A
A10	L6	5	08175-61104	CHOKE 43uH 8A
A10	L7	6	08175-61105	CHOKE 2X330 uH
A10	L8	7	08175-61106	CHOKE 2X1.3mH
A10	MP1	1	1205-0210	HT-SINK SEMICON
A10	MP2	1	1205-0210	HT-SINK SEMICON
A10	MP3	4	08175-01109	HEATSINK
A10	MP5	6	1205-0489	HEAT SINK-6021BS
A10	MP6	6	1205-0489	HEAT SINK-6021BS
A10	MP7	6	1205-0489	HEAT SINK-6021BS
A10	MP9	9	1205-0490	HEAT SINK
A10	MP10	2	1205-0295	HEAT-SINK
A10	MP11	6	1205-0489	HEAT SINK-6021BS
A10	MP12	7	08175-01102	HEATS DUAL
A10	MP13	8	08175-01103	HEATS ANGLE
A10	MP14	8	08175-01103	HEATS ANGLE
A10	MP15	4	08175-00169	BRACKET POWER
A10	MP17	2	08175-04101	COVER SAFETY
A10	MP18	4	08175-21701	BUSHING PWR SPLY
A10	MP19	1	08175-45401	INSULATOR 3XTO-3
A10	MP20	1	08175-45401	INSULATOR 3XTO-3
A10	Q1	6	1854-0963	XSTR NPN
A10	Q2	6	1854-0963	XSTR NPN
A10	Q3	9	1853-0281	XSTR SI 2907A
A10	Q4	6	1854-0583	XSTR MPS A18
A10	Q5	6	1854-0583	XSTR MPS A18
A10	Q6	2	1854-0828	XSTR NPN S T220
A10	R3	7	0757-0367	R-F 100K 1% .5W
A10	R4	7	0757-0367	R-F 100K 1% .5W
A10	R5	8	0698-3615	R-F 47 5%
A10	R6	0	0757-0394	R-F 51.1 1%
A10	R7	0	0757-0394	R-F 51.1 1%
A10	R8	8	0757-0384	R-F 20 1% .125W
A10	R9	9	0757-0442	R-F 10K1% .125W
A10	R10	3	0757-0280	R-F 1K 1% .125W
A10	R11	8	0698-3178	R-F 487 1% .125W
A10	R12	8	0698-3178	R-F 487 1% .125W
A10	R13	4	0757-0801	R-F 150 1% .5W
A10	R14	4	0757-0801	R-F 150 1% .5W
A10	R15	9	0757-0442	R-F 10K1% .125W
A10	R16	0	0698-4483	R-F 18.7K1%.125W
A10	R17	3	0757-0280	R-F 1K 1% .125W
A10	R18	6	0757-0465	R-F 100K1% .125W
A10	R19	3	0757-0199	R-F 21.5K1%
A10	R20	1	0757-0288	R-F 9.09K 1%.125
A10	R21	7	2100-3211	R-TRMR 1K 10%
A10	R22	1	0698-3155	R-F 4.64K 1%.125
A10	R23	9	0757-0442	R-F 10K1% .125W
A10	R24	3	0757-0462	R-F 75K1% .125W
A10	R25	4	0757-0281	R-F 2.74K 1%
A10	R26	9	0757-0442	R-F 10K1% .125W
A10	R27	8	0757-0459	R-F 56.2K1%
A10	R28	7	0757-0440	R-F 7.5K 1%.125W
A10	R29	7	0757-0440	R-F 7.5K 1%.125W
A10	R30	6	0757-0283	R-F 2K1% .125W F
A10	R31	8	0757-0459	R-F 56.2K1%
A10	R32	3	0698-3454	R-F 215K1% .125W
A10	R33	3	0757-0280	R-F 1K 1% .125W
A10	R34	3	0757-0280	R-F 1K 1% .125W
A10	R35	0	0757-0419	R-F 681 1% .125W
A10	R36	7	0757-0416	R-F 511 1% .125W
A10	R37	1	0757-0288	R-F 9.09K 1%.125
A10	R38	5	2100-0554	R-V 500 10% .5W
A10	R39	9	0757-0442	R-F 10K1% .125W
A10	R40	4	0698-3603	R-F 12 5% 2W MO
A10	R41	4	0698-3603	R-F 12 5% 2W MO
A10	R42	5	0757-0795	R-F 75 1% .5W MF
A10	R43	2	0757-0809	R-F 332 1% .5W
A10	R44	6	0698-4421	R-F 249 1% .125W
A10	R45	6	0698-4421	R-F 249 1% .125W
A10	R46	2	0698-4435	R-F 2.49K1%
A10	R47	2	0698-4435	R-F 2.49K1%
A10	R48	5	2100-0554	R-V 500 10% .5W
A10	R49	5	2100-0554	R-V 500 10% .5W
A10	R50	0	0698-4417	R-F 174 1% .125W
A10	R51	0	0698-4417	R-F 174 1% .125W
A10	R52	7	0698-3151	R-F 2.87K1%
A10	R53	7	0698-3151	R-F 2.87K1%
A10	MP21	3	2110-0642	HOLDER FUSE
A10	MP22	9	2110-0565	CAP FUSEHOLDR/UL

REFERENCE DESIGNATOR		C D	H-P PART NUMBER	DESCRIPTION
A10	R54	5	2100-0554	R-V 500 10% .5W
A10	R55	5	2100-0554	R-V 500 10% .5W
A10	R56	3	0811-1224	R-F 3 5% 3W
A10	R57	0	0699-0124	R-F 10.2K .1%
A10	R58	7	0699-0858	R-F 13K .1% .125
A10	R59	0	0811-2568	R-F 1 1% 3W
A10	R60	0	0757-0443	R-F 11K1% .125W
A10	R67	6	0757-0407	R-F 200 1% .125W
A10	R68	1	0698-3155	R-F 4.64K 1%.125
A10	R69	1	0698-3155	R-F 4.64K 1%.125
A10	R70	9	0757-0476	R-F 301K 1% .125
A10	R71	2	0757-0453	R-F 30.1K1%.125W
A10	R72	6	0698-4421	R-F 249 1% .125W
A10	R73	2	0698-4435	R-F 2.49K1%
A10	R74	5	2100-0554	R-V 500 10% .5W
A10	R75	0	0698-4425	R-F 1.54K1%
A10	R76	0	0698-4425	R-F 1.54K1%
A10	R77	0	0698-4425	R-F 1.54K1%
A10	R78	1	0757-0741	R-F 2.43K1% .25W
A10	R79	1	0757-0741	R-F 2.43K1% .25W
A10	R80	9	0698-7212	R-F 100 1% .05W
A10	RA1	6	1810-0337	R-NETWORK 8X4.7K
A10	RA2	6	1810-0337	R-NETWORK 8X4.7K
A10	RA3	1	1810-0316	R-NETWORK 8X10K
A10	RA4	1	1810-0316	R-NETWORK 8X10K
A10	RA5	4	1810-0319	R-NETWORK 8X100K
A10	RT1	2	0837-0263	THNS-SRG PTCTR
A10	RT2	4	0837-0215	THMS-SRG PTCTR
A10	RT3	2	0837-0263	THNS-SRG PTCTR
A10	RT4	2	0837-0263	THNS-SRG PTCTR
A10	RV1	0	0837-0120	VARISTOR 130VAC
A10	RV2	0	0837-0120	VARISTOR 130VAC
A10	RV3	7	0837-0309	SUPPRESSOR-VOLT
A10	S1	4	3101-2150	SW-PB DPDT 5A
A10	S2	7	3101-2608	SWITCH-SLIDE
A10	S3	2	3103-0091	SW-THRM +110C 6A
A10	S4	2	3103-0091	SW-THRM +110C 6A
A10	T1	6	9100-0417	XFMR PWR
A10	T2	2	08175-61101	XFMR PWR SWITCH
A10	T3	3	08175-61102	XFMR BASE DRIVE
A10	T4	3	08175-61102	XFMR BASE DRIVE
A10	T5	7	9100-4163	XFMR
A10	TP2	2	1251-0628	CONN POST TP SKT
A10	TP3	2	1251-0628	CONN POST TP SKT
A10	TP4	2	1251-0628	CONN POST TP SKT
A10	TP5	2	1251-0628	CONN POST TP SKT
A10	TP6	2	1251-0628	CONN POST TP SKT
A10	TP7	2	1251-0628	CONN POST TP SKT
A10	TP8	2	1251-0628	CONN POST TP SKT
A10	TP9	2	1251-0628	CONN POST TP SKT
A10	TP10	2	1251-0628	CONN POST TP SKT
A10	TP11	2	1251-0628	CONN POST TP SKT
A10	TP12	2	1251-0628	CONN POST TP SKT
A10	U1	5	1826-0565	IC TL494CN
A10	U2	9	1820-2111	IC SN75468N
A10	U3	7	1826-0161	IC 324
A10	U4	7	1826-0468	IC 3423
A10	U5	7	1826-0468	IC 3423
A10	U6	0	1826-1245	IC LIN 7L7702A
A10	U7	3	1826-0315	IC 348
A10	U8	9	1826-0147	IC MC7812CT
A10	U9	0	1826-0718	IC MC1404U5
A10	U10	6	1826-0748	IC LM 250K STEEL
A10	U11	9	1826-0527	IC LM337T
A10	U12	7	1826-0393	IC LM317T
A10	U13	9	1826-0527	IC LM337T
A10	U14	7	1826-0393	IC LM317T
A10	VR1	7	1902-0953	DIO ZNR 6.2V
A20	08175-66520			BD AY-CPU
A20	B1	5	9164-0173	ALARM AUDIBLE
A20	BT1	6	1420-0251	BATTERY-NICAD
A20	C101	8	0160-6080	C-F .068UF 50VDC
A20	C102	8	0160-6080	C-F .068UF 50VDC
A20	C103	5	0180-1746	C-F 15UF 20V TA
A20	C104	5	0180-1746	C-F 15UF 20V TA
A20	C105	8	0160-6080	C-F .068UF 50VDC
A20	C106	8	0160-6080	C-F .068UF 50VDC
A20	C107	8	0160-6080	C-F .068UF 50VDC
A20	C108	8	0160-6080	C-F .068UF 50VDC
A20	C109	8	0160-6080	C-F .068UF 50VDC
A20	C110	8	0160-6080	C-F .068UF 50VD'
A20	C200	8	0160-6080	C-F .068UF 50VDC
A20	C201	8	0160-6080	C-F .068UF 50VDC
A20	C203	8	0160-6080	C-F .068UF 50VDC
A20	C204	8	0160-6080	C-F .068UF 50VDC
A20	C205	8	0160-6080	C-F .068UF 50VDC
A20	C300	2	0180-2692	C-F 68UF 15V TA
A20	C302	8	0160-6080	C-F .068UF 50VDC
A20	C305	8	0160-6080	C-F .068UF 50VDC
A20	C306	5	0180-2207	C-F 100UF 10V
A20	C307	8	0160-6080	C-F .068UF 50VDC
A20	C308	8	0160-6080	C-F .068UF 50VDC
A20	C309	8	0160-6080	C-F .068UF 50VDC
A20	C310	8	0160-6080	C-F .068UF 50VDC
A20	C311	8	0160-6080	C-F .068UF 50VDC
A20	C312	8	0160-6080	C-F .068UF 50VDC
A20	C313	8	0160-6080	C-F .068UF 50VDC
A20	C314	8	0160-6080	C-F .068UF 50VDC
A20	C315	8	0160-6080	C-F .068UF 50VDC
A20	C316	8	0160-6080	C-F .068UF 50VDC
A20	C401	8	0160-6080	C-F .068UF 50VDC
A20	C402	8	0160-6080	C-F .068UF 50VDC
A20	C403	8	0160-6080	C-F .068UF 50VDC
A20	C404	8	0160-6080	C-F .068UF 50VDC
A20	C405	8	0160-6080	C-F .068UF 50VDC
A20	C406	8	0160-6080	C-F .068UF 50VDC
A20	C407	8	0160-6080	C-F .068UF 50VDC
A20	C408	8	0160-6080	C-F .068UF 50VDC
A20	C409	8	0160-6080	C-F .068UF 50VDC
A20	C410	8	0160-6080	C-F .068UF 50VDC
A20	C411	8	0160-6080	C-F .068UF 50VDC
A20	C412	8	0160-6080	C-F .068UF 50VDC
A20	C413	8	0160-6080	C-F .068UF 50VDC
A20	C414	8	0160-6080	C-F .068UF 50VDC
A20	C501	8	0160-6080	C-F .068UF 50VDC
A20	C502	8	0160-6080	C-F .068UF 50VDC
A20	C600	8	0160-6080	C-F .068UF 50VDC
A20	C601	8	0160-6080	C-F .068UF 50VDC
A20	C602	8	0160-6080	C-F .068UF 50VDC
A20	C603	8	0160-6080	C-F .068UF 50VDC
A20	C604	8	0160-6080	C-F .068UF 50VDC
A20	C605	8	0160-6080	C-F .068UF 50VDC

REFERENCE DESIGNATOR	CD	H-P PART NUMBER	DESCRIPTION
A20 C606	8	0160-6080	C-F .068UF 50VDC
A20 C607	8	0160-6080	C-F .068UF 50VDC
A20 C608	8	0160-6080	C-F .068UF 50VDC
A20 C609	5	0180-1746	C-F 15UF 20V TA
A20 C610	8	0160-6080	C-F .068UF 50VDC
A20 C611	8	0160-6080	C-F .068UF 50VDC
A20 C612	8	0180-0197	C-F 2.2UF 20V
A20 C613	8	0160-6080	C-F .068UF 50VDC
A20 C701	7	0160-5742	C-F 27PF 5% 100V
A20 C702	7	0160-5742	C-F 27PF 5% 100V
A20 C703	8	0160-6080	C-F .068UF 50VDC
A20 C704	8	0160-6080	C-F .068UF 50VDC
A20 C705	8	0160-6080	C-F .068UF 50VDC
A20 C706	8	0160-6080	C-F .068UF 50VDC
A20 C707	8	0160-6080	C-F .068UF 50VDC
A20 C708	8	0160-6080	C-F .068UF 50VDC
A20 C709	8	0160-6080	C-F .068UF 50VDC
A20 C710	8	0160-6080	C-F .068UF 50VDC
A20 C711	8	0160-6080	C-F .068UF 50VDC
A20 CR201	9	1901-0535	DIO SCHOT HP2311
A20 CR202	9	1901-0535	DIO SCHOT HP2311
A20 CR203	9	1901-0535	DIO SCHOT HP2311
A20 CR301	9	1901-0535	DIO SCHOT HP2311
A20 CR600	1	1901-1098	DIO-1N4150 50V
A20 J3	2	1251-7799	3X32 PLUG
A20 J4	2	1251-7799	3X32 PLUG
A20 J201	0	1251-3109	CONN POST-TP-HDR
A20 J202	2	1251-7666	CONN-POST 16 PIN
A20 J204	4	1200-0487	SKT IC 16CONT
A20 J205	3	1251-7162	CONN HPIB
A20 L201	0	9100-1641	COIL CHOKE 240UH
A20 L202	0	9100-1617	IDCTR 3.9UH 10%
A20 M246	4	1251-7999	COVER DUST CONN
A20 MP3	7	08175-21704	BUSHING SHORT
A20 MP4	3	08175-26106	PC PIN
A20 Q100	4	1853-0400	XSTR DARL MPSA64
A20 R101	6	0757-0283	R-F 2K1% .125W F
A20 R102	6	2100-3103	R-VAR 10K 10%
A20 R201	0	0698-3279	R-F 4.99K1%
A20 R202	6	0698-6360	R-F 10K.1% .125W
A20 R203	6	0698-6360	R-F 10K.1% .125W
A20 R205	5	0698-4123	R-F 499 1% .125W
A20 R209	8	0698-7229	R-F 511 1% .05W
A20 R210	8	0698-7229	R-F 511 1% .05W
A20 R302	9	0757-0418	R-F 619 1% .125W
A20 R401	3	0757-0389	R-F 33.2 1%
A20 R403	3	0757-0389	R-F 33.2 1%
A20 R405	1	0698-7660	R-F 61.9 1% .25W
A20 R601	3	0757-0389	R-F 33.2 1%
A20 R700	8	0698-3615	R-F 47 5%
A20 R702	6	0757-0283	R-F 2K1% .125W F
A20 R703	6	0757-0283	R-F 2K1% .125W F
A20 R704	6	0757-0283	R-F 2K1% .125W F
A20 R707	6	0757-0465	R-F 100K1% .125W
A20 R708	3	0757-0280	R-F 1K 1% .125W
A20 R709	6	0757-0407	R-F 200 1% .125W
A20 R710	3	0757-0280	R-F 1K 1% .125W
A20 RA100	1	1810-0316	R-NETWORK 8X10K
A20 RA206	1	1810-0316	R-NETWORK 8X10K
A20 RA207	1	1810-0316	R-NETWORK 8X10K
A20 RA208	1	1810-0316	R-NETWORK 8X10K
A20 RA303	8	1810-0470	R-NETWORK 8X2.2K
A20 RA402	4	1810-0533	R-NETW 33.0 OHM
A20 RA404	1	1810-0316	R-NETWORK 8X10K
A20 RA602	1	1810-0316	R-NETWORK 8X10K
A20 RA603	8	1810-0470	R-NETWORK 8X2.2K
A20 RT701	5	0837-0050	THMS 1K DIS
A20 S701	5	3101-2094	SW DIP 8ROCKER
A20 U101	6	1820-2861	IC 74F138 P
A20 U102	9	1820-1197	IC SN74LS00N
A20 U103	3	1820-2701	IC 74F374PC
A20 U104	7	1820-1997	IC SN74LS374N
A20 U105	4	1820-1209	IC SN74LS 38 N
A20 U106	8	08175-13702	E-PROM 3
A20 U107	9	08175-13703	E-PROM 4
A20 U108	0	08175-13704	E-PROM 5
A20 U109	1	08175-13705	E-PROM 6
A20 U110	2	08175-13706	E-PROM 7
A20 U111	3	08175-13707	E-PROM 8
A20 U202	4	1826-0639	D/A 8-BIT
A20 U203	3	1826-0315	IC 348
A20 U204	4	1826-0639	D/A 8-BIT
A20 U205	4	1826-0853	IC REF-01HJ
A20 U206	4	1826-0639	D/A 8-BIT
A20 U209	3	1820-2024	IC SN74LS244N
A20 U210	6	08175-13700	E-PROM 1
A20 U211	7	08175-13701	E-PROM 2
A20 U212	2	1818-3183	IC HM6264LP-15
A20 U213	2	1818-3183	IC HM6264LP-15
A20 U214	2	1818-3183	IC HM6264LP-15
A20 U215	2	1818-3183	IC HM6264LP-15
A20 U216	3	1820-1216	IC SN74LS138N
A20 U217	3	1858-0053	XSTR ARY 14P-DIP
A20 U300	3	1820-1208	IC SN74LS32N
A20 U301	6	1820-1144	IC SN74LS02N
A20 U303	3	1820-1216	IC SN74LS138N
A20 U304	3	1820-2701	IC 74F374PC
A20 U305	3	1820-1216	IC SN74LS138N
A20 U306	5	1820-2795	IC 74F244PC
A20 U307	4	1820-2075	IC SN74LS245N
A20 U308	9	1820-1238	IC-SN74LS253N
A20 U309	6	1820-1730	IC SN74LS273N
A20 U310	9	1820-1238	IC-SN74LS253N
A20 U311	6	1820-1730	IC SN74LS273N
A20 U312	9	1820-1238	IC-SN74LS253N
A20 U313	6	1820-1730	IC SN74LS273N
A20 U314	6	1820-2861	IC 74F138 P
A20 U315	9	1820-1197	IC SN74LS00N
A20 U316	7	1820-2763	IC 74F258PC
A20 U317	7	1820-2763	IC 74F258PC
A20 U318	7	1820-2911	IC MC68B29
A20 U319	8	1820-2102	IC SN74LS373N
A20 U320	8	1820-2102	IC SN74LS373N
A20 U321	7	1820-2854	IC 68B09E
A20 U322	6	1820-2506	IC 74F 04P
A20 U401	9	1820-1197	IC SN74LS00N
A20 U402	9	1820-1197	IC SN74LS00N
A20 U403	5	1820-2688	IC 74F11PC
A20 U404	9	1820-1204	IC SN74LS20N
A20 U405	9	1820-1204	IC SN74LS20N
A20 U406	7	1818-3005	IC HM4864P-2
A20 U407	7	1818-3005	IC HM4864P-2
A20 U408	7	1818-3005	IC HM4864P-2

REFERENCE DESIGNATOR		CD	H-P PART NUMBER	DESCRIPTION
A20	U409	7	1818-3005	IC HM4864P-2
A20	U410	7	1818-3005	IC HM4864P-2
A20	U411	7	1818-3005	IC HM4864P-2
A20	U412	7	1818-3005	IC HM4864P-2
A20	U413	7	1818-3005	IC HM4864P-2
A20	U414	2	1820-1439	IC SN74LS258AN
A20	U415	2	1820-1439	IC SN74LS258AN
A20	U416	6	1820-2853	IC MC68A45L
A20	U417	0	1820-1445	IC SN74 LS375N
A20	U418	6	1820-2150	IC-8279-5
A20	U419	3	1820-1216	IC SN74LS138N
A20	U420	8	1820-1451	IC SN74S38N
A20	U501	6	1820-1730	IC SN74LS273N
A20	U502	6	1820-1730	IC SN74LS273N
A20	U503	4	1820-2075	IC SN74LS245N
A20	U504	3	1820-2024	IC SN74LS244N
A20	U505	3	1820-2701	IC 74F374PC
A20	U506	3	1820-2024	IC SN74LS244N
A20	U507	6	1820-1730	IC SN74LS273N
A20	U508	0	1818-3074	IC-AM9233 CPC
A20	U509	6	1820-1201	IC SN74LS08N
A20	U510	5	1820-2696	IC 74F175PC
A20	U511	4	1820-2687	IC 74F10PC
A20	U512	8	1820-1112	IC SN74LS74AN
A20	U600	3	1820-2024	IC SN74LS244N
A20	U601	0	1820-1198	IC SN74LS03N
A20	U602	6	1820-1730	IC SN74LS273N
A20	U603	0	1820-1198	IC SN74LS03N
A20	U604	3	1820-2024	IC SN74LS244N
A20	U605	8	1820-1112	IC SN74LS74AN
A20	U606	7	1820-1278	IC SN74LS191N
A20	U607	7	1820-2763	IC 74F258PC
A20	U608	9	1820-2096	IC SN74LS393N
A20	U609	7	1820-2763	IC 74F258PC
A20	U610	9	1820-2096	IC SN74LS393N
A20	U611	3	1820-2024	IC SN74LS244N
A20	U612	4	1820-1457	IC-SN74S299N
A20	U613	1	1820-2692	IC 74F86PC
A20	U614	8	1820-1112	IC SN74LS74AN
A20	U615	1	1820-2684	IC 74F00PC
A20	U616	8	1820-1112	IC SN74LS74AN
A20	U617	1	1820-2684	IC 74F00PC
A20	U618	9	1826-0147	IC MC7812CT
A20	U701	5	1820-2604	IC 9513
A20	U702	6	1820-2548	IC 9914
A20	U703	8	1820-3431	IC DS75160AN
A20	U704	2	1820-3518	IC DS75162AN
A20	U708	6	1820-2506	IC 74F 04P
A20	U709	7	1820-1210	IC-SN74LS51N
A20	U710	5	1820-2696	IC 74F175PC
A20	U711	2	1820-1158	IC SN74S 1N
A20	U712	5	1820-2696	IC 74F175PC
A20	U713	0	1820-2691	IC 74F74PC
A20	U714	2	1820-2685	IC 74F02PC
A20	U715	1	1820-2684	IC 74F00PC
A20	U716	3	1820-2701	IC 74F374PC
A20	U717	8	1858-0058	XSTR QUAD PNP
A20	Y601	0	0410-1552	QUARTZ 3.6860MHZ
A20	Y701	7	1813-0275	XTAL-CLK-OSC 40
A20	Z1	1	1200-0567	SOCKET IC 28 PIN
A20	Z2	1	1200-0567	SOCKET IC 28 PIN
A20	Z3	1	1200-0567	SOCKET IC 28 PIN
A20	Z4	1	1200-0567	SOCKET IC 28 PIN
A20	Z5	1	1200-0567	SOCKET IC 28 PIN
A20	Z6	1	1200-0567	SOCKET IC 28 PIN
A20	Z7	1	1200-0567	SOCKET IC 28 PIN
A20	Z8	1	1200-0567	SOCKET IC 28 PIN
A20	Z10	7	1200-0654	SOCKET IC 40-CON
A20	Z11	7	1200-0654	SOCKET IC 40-CON
A20	Z12	7	1200-0654	SOCKET IC 40-CON
A20	Z13	7	1200-0654	SOCKET IC 40-CON
A20	Z14	7	1200-0654	SOCKET IC 40-CON
A20	Z15	7	1200-0654	SOCKET IC 40-CON

A30	08175-66530	BD AY-CLOCK

A30	C1	8	0160-5735	C-F 10PF 0.5PF
A30	C2	3	0160-5730	C-F 100PF 5%
A30	C3	8	0160-6080	C-F .068UF 50VDC
A30	C4	8	0160-6080	C-F .068UF 50VDC
A30	C8	8	0160-6080	C-F .068UF 50VDC
A30	C9	8	0160-6080	C-F .068UF 50VDC
A30	C10	8	0160-6080	C-F .068UF 50VDC
A30	C11	8	0160-6080	C-F .068UF 50VDC
A30	C12	8	0160-6080	C-F .068UF 50VDC
A30	*C19	2	0160-5739	C-F 15PF 5% 100V
A30	C40	8	0160-6080	C-F .068UF 50VDC
A30	C41	3	0160-5730	C-F 100PF 5%
A30	C47	9	0160-5744	C-F 56PF 5% 100V
A30	C48	9	0160-5744	C-F 56PF 5% 100V
A30	C49	8	0160-6080	C-F .068UF 50VDC
A30	C50	8	0160-6080	C-F .068UF 50VDC
A30	C51	8	0160-6080	C-F .068UF 50VDC
A30	C52	8	0160-6080	C-F .068UF 50VDC
A30	C53	9	0160-4382	C-F 3.3PF
A30	C54	0	0121-0515	C-VAR 2-8PF
A30	C55	0	0160-3872	C-F 2.2 PF 200V
A30	C56	9	0160-4382	C-F 3.3PF
A30	C57	0	0121-0515	C-VAR 2-8PF
A30	C58	0	0160-3872	C-F 2.2 PF 200V
A30	C59	9	0160-5736	C-F 22PF 5% 100V
A30	C60	9	0160-5736	C-F 22PF 5% 100V
A30	C61	8	0160-6080	C-F .068UF 50VDC
A30	C62	8	0160-6080	C-F .068UF 50VDC
A30	C63	8	0160-6080	C-F .068UF 50VDC
A30	C64	8	0160-6080	C-F .068UF 50VDC
A30	C66	1	0160-5746	C-F 0.1UF 20%
A30	C67	1	0160-5746	C-F 0.1UF 20%
A30	C68	8	0160-6080	C-F .068UF 50VDC
A30	C69	3	0160-5730	C-F 100PF 5%
A30	C70	3	0160-5730	C-F 100PF 5%
A30	C71	4	0180-0094	C-F 100UF 25V
A30	C72	8	0180-0197	C-F 2.2UF 20V
A30	C73	8	0180-0197	C-F 2.2UF 20V
A30	C74	8	0180-0197	C-F 2.2UF 20V
A30	C75	8	0160-6080	C-F .068UF 50VDC
A30	C76	9	0160-5728	C-F 1000PF 5%
A30	C77	9	0160-5728	C-F 1000PF 5%
A30	C78	2	0180-1743	C-F .1UF 35V TA
A30	C79	6	0160-3456	C-F 1000PF 1000V
A30	C80	9	0160-5728	C-F 1000PF 5%
A30	C81	8	0160-6080	C-F .068UF 50VDC
A30	C82	8	0160-6080	C-F .068UF 50VDC
A30	C90	9	0160-5744	C-F 56PF 5% 100V
A30	C91	9	0160-5744	C-F 56PF 5% 100V
A30	*C95	0	0160-3872	C-F 2.2 PF 200V
A30	C99	9	0160-5736	C-F 22PF 5% 100V
A30	C100	4	0180-0094	C-F 100UF 25V
A30	C101	8	0160-6080	C-F .068UF 50VDC

REFERENCE DESIGNATOR		C D	H-P PART NUMBER	DESCRIPTION
A30	C102	8	0160-6080	C-F .068UF 50VDC
A30	C103	8	0160-6080	C-F .068UF 50VDC
A30	C104	8	0160-6080	C-F .068UF 50VDC
A30	C105	8	0160-6080	C-F .068UF 50VDC
A30	C106	8	0160-6080	C-F .068UF 50VDC
A30	C107	8	0160-6080	C-F .068UF 50VDC
A30	C108	8	0160-6080	C-F .068UF 50VDC
A30	C109	8	0160-6080	C-F .068UF 50VDC
A30	C110	8	0160-6080	C-F .068UF 50VDC
A30	C111	8	0160-6080	C-F .068UF 50VDC
A30	C200	4	0180-0094	C-F 100UF 25V
A30	C201	8	0160-6080	C-F .068UF 50VDC
A30	C202	8	0160-6080	C-F .068UF 50VDC
A30	C203	8	0160-6080	C-F .068UF 50VDC
A30	C204	8	0160-6080	C-F .068UF 50VDC
A30	C205	8	0160-6080	C-F .068UF 50VDC
A30	C206	8	0160-6080	C-F .068UF 50VDC
A30	C207	8	0160-6080	C-F .068UF 50VDC
A30	C208	8	0160-6080	C-F .068UF 50VDC
A30	C209	8	0160-6080	C-F .068UF 50VDC
A30	C210	8	0160-6080	C-F .068UF 50VDC
A30	C211	8	0160-6080	C-F .068UF 50VDC
A30	C212	8	0160-6080	C-F .068UF 50VDC
A30	C213	8	0160-6080	C-F .068UF 50VDC
A30	C214	8	0160-6080	C-F .068UF 50VDC
A30	C215	8	0160-6080	C-F .068UF 50VDC
A30	C216	8	0160-6080	C-F .068UF 50VDC
A30	C217	8	0160-6080	C-F .068UF 50VDC
A30	C218	8	0160-6080	C-F .068UF 50VDC
A30	C219	1	0160-4574	C-F 1000PF 10%
A30	CR50	1	1901-1098	DIO-1N4150 50V
A30	CR51	1	1901-1098	DIO-1N4150 50V
A30	CR52	1	1901-1098	DIO-1N4150 50V
A30	CR53	1	1901-1098	DIO-1N4150 50V
A30	CR59	1	1901-1098	DIO-1N4150 50V
A30	CR60	1	1901-1098	DIO-1N4150 50V
A30	CR61	1	1901-1098	DIO-1N4150 50V
A30	CR62	9	1901-0535	DIO SCHOT HP2311
A30	CR64	4	0122-0161	DIODE-VVC
A30	CR65	4	0122-0161	DIODE-VVC
A30	CR66	4	0122-0161	DIODE-VVC
A30	CR67	4	0122-0161	DIODE-VVC
A30	CR70	1	1901-1098	DIO-1N4150 50V
A30	CR71	1	1901-1098	DIO-1N4150 50V
A30	CR80	7	1901-0731	DIO-PWR 400V 1A
A30	CR100	9	1901-0535	DIO SCHOT HP2311
A30	CR101	9	1901-0535	DIO SCHOT HP2311
A30	CR200	1	1901-1098	DIO-1N4150 50V
A30	CR201	1	1901-1098	DIO-1N4150 50V
A30	DL1	7	08175-61601	DELAY LINE AY
A30	DL2	3	1810-0730	DELAY LINE
A30	J5	2	1251-7799	3X32 PLUG
A30	J6	2	1251-7799	3X32 PLUG
A30	J301	8	1251-8008	CONN-RECT
A30	J303	8	1250-0543	CONN RF M SM-SNP
A30	J304	8	1250-0543	CONN RF M SM-SNP
A30	J305	8	1250-0543	CONN RF M SM-SNP
A30	J306	0	1251-7705	CONN-POST 28CONT
A30	J307	0	1251-7705	CONN-POST 28CONT
A30	J308	9	1251-3702	CONN-POST 3M
A30	J309	9	1251-3702	CONN-POST 3M
A30	J310	9	1251-3702	CONN-POST 3M
A30	J311	9	1251-3702	CONN-POST 3M
A30	J312	9	1251-3702	CONN-POST 3M

REFERENCE DESIGNATOR		C D	H-P PART NUMBER	DESCRIPTION
A30	K80	4	0490-1079	RELAY REED
A30	L60	5	9140-0131	COIL-FXD 10MH
A30	L61	5	9140-0131	COIL-FXD 10MH
A30	L62	7	9100-3149	COIL 220UH 10%
A30	L100	0	9170-0894	CORE MAGNETIC
A30	L101	0	9170-0894	CORE MAGNETIC
A30	L102	0	9170-0894	CORE MAGNETIC
A30	L103	0	9170-0894	CORE MAGNETIC
A30	L104	0	9170-0894	CORE MAGNETIC
A30	L105	0	9170-0894	CORE MAGNETIC
A30	MP5	7	08175-21704	BUSHING SHORT
A30	MP6	3	08175-26106	PC PIN
A30	MP13	8	08175-04107	CLOCK COVER
A30	Q50	2	1853-0036	XSTR SI 2N3906
A30	Q51	1	1854-0215	XSTR SI 2N3904
A30	Q80	1	1854-0215	XSTR SI 2N3904
A30	R1	0	0698-4483	R-F 18.7K1%.125W
A30	R2	0	0757-0443	R-F 11K1% .125W
A30	R3	9	0757-0442	R-F 10K1% .125W
A30	R4	2	0698-4443	R-F 4.53K1%
A30	R6	8	2100-3759	R-TRMR 2K 10%
A30	R7	3	0757-0280	R-F 1K 1% .125W
A30	R8	8	0698-3136	R-F 17.8K1%
A30	R10	0	2100-0567	R-TRMR 2K 10%
A30	R11	6	0757-0407	R-F 200 1% .125W
A30	R12	6	0757-0407	R-F 200 1% .125W
A30	R13	6	0757-0407	R-F 200 1% .125W
A30	R14	9	0757-0278	R-F 1.78K1%
A30	R15	1	0698-3155	R-F 4.64K 1%.125
A30	R16	0	0757-0443	R-F 11K1% .125W
A30	R17	3	0757-0454	R-F 33.2K1%.125W
A30	R18	6	0698-3225	R-F 1.43K1%
A30	R19	7	0698-7236	R-F 1K 1% .05W
A30	R20	7	0757-0408	R-F 243 1% .125W
A30	R21	0	0757-0419	R-F 681 1% .125W
A30	R23	5	0757-0349	R-F 22.6K1%.125W
A30	R24	0	2100-0567	R-TRMR 2K 10%
A30	R25	8	0757-0441	R-F 8.25K1%
A30	R26	6	0757-0449	R-F 20K1% .125W
A30	R27	8	0698-3540	R-F 15.4K1%
A30	R28	8	0757-0433	R-F 3.32K1%
A30	R29	2	0757-0180	R-F 31.6 1%
A30	R30	4	0757-0281	R-F 2.74K 1%
A30	R31	5	0698-4462	R-F 768 1% .125
A30	R32	7	0698-4399	R-F 88.7 1%.125W
A30	R33	2	0698-3437	R-F 133 1% .125W
A30	R34	6	0757-0449	R-F 20K1% .125W
A30	R35	8	0698-3540	R-F 15.4K1%
A30	R36	8	0757-0433	R-F 3.32K1%
A30	R37	2	0757-0180	R-F 31.6 1%
A30	R38	4	0757-0281	R-F 2.74K 1%
A30	R39	5	0698-4462	R-F 768 1% .125
A30	R40	7	0698-4399	R-F 88.7 1%.125W
A30	R41	2	0698-3437	R-F 133 1% .125W
A30	R42	6	0757-0407	R-F 200 1% .125W
A30	R43	6	0757-0407	R-F 200 1% .125W
A30	R44	7	0698-4422	R-F 1.27K1%
A30	R45	6	0757-0407	R-F 200 1% .125W
A30	R46	7	0698-4422	R-F 1.27K1%
A30	R47	3	0757-0280	R-F 1K 1% .125W
A30	R48	3	0757-0280	R-F 1K 1% .125W
A30	R49	7	0757-0317	R-F 1.33K1%
A30	R50	9	0757-0434	R-F 3.65K1%

REFERENCE DESIGNATOR		C D	H-P PART NUMBER	DESCRIPTION
A30	R51	0	0698-3279	R-F 4.99K1%
A30	R52	3	0757-0438	R-F 5.11K1%
A30	R53	0	0757-0401	R-F 100 1% .125W
A30	R54	9	0757-0442	R-F 10K1% .125W
A30	R55	9	0757-0442	R-F 10K1% .125W
A30	R56	0	0757-0401	R-F 100 1% .125W
A30	R57	9	0757-0442	R-F 10K1% .125W
A30	R58	0	0698-4483	R-F 18.7K1%.125W
A30	R59	3	0698-3157	R-F 19.6K 1%.125
A30	R61	0	2100-0567	R-TRMR 2K 10%
A30	R62	0	2100-3214	R-V 100K 10% .5W
A30	R63	8	0757-0409	R-F 274 1% .125W
A30	R64	8	0757-0409	R-F 274 1% .125W
A30	R65	7	0698-4521	R-F 154K1% .125W
A30	R66	7	0698-4521	R-F 154K1% .125W
A30	R67	4	0757-0405	R-F 162 1% .125W
A30	R68	7	0757-0408	R-F 243 1% .125W
A30	R69	8	0757-0409	R-F 274 1% .125W
A30	R70	0	0698-4409	R-F 127 1% .125W
A30	R71	5	0757-0399	R-F 82.5 1%.125W
A30	R72	3	0757-0438	R-F 5.11K1%
A30	R73	9	0757-0442	R-F 10K1% .125W
A30	R74	2	0698-3156	R-F 14.7K1%
A30	R75	2	0698-3156	R-F 14.7K1%
A30	R76	1	0698-3519	R-F 12.4K1%
A30	R77	6	0698-3499	R-F 40.2K1%
A30	R78	6	0757-0465	R-F 100K1% .125W
A30	R79	5	0698-4496	R-F 45.3K1%
A30	R80	2	0757-0453	R-F 30.1K1%.125W
A30	R81	6	0757-0415	R-F 475 1% .125W
A30	R82	6	0757-0415	R-F 475 1% .125W
A30	R83	2	0757-0354	R-F 3.65K1% .25W
A30	R84	2	0698-3445	R-F 348 1% .125W
A30	R85	2	0698-3445	R-F 348 1% .125W
A30	R86	3	0757-0280	R-F 1K 1% .125W
A30	R87	3	0757-0438	R-F 5.11K1%
A30	R88	9	0757-0442	R-F 10K1% .125W
A30	R89	9	0757-0442	R-F 10K1% .125W
A30	R90	2	0757-0429	R-F 1.82K1%
A30	R91	3	0757-0280	R-F 1K 1% .125W
A30	R92	4	0757-0273	R-F 3.01K1%
A30	R95	3	0757-0438	R-F 5.11K1%
A30	R96	7	0757-0416	R-F 511 1% .125W
A30	R97	3	0757-0280	R-F 1K 1% .125W
A30	R98	3	0757-0280	R-F 1K 1% .125W
A30	R99	9	2100-1788	R-VAR 500 .5W CE
A30	R100	0	0757-0427	R-F 1.5K1% .125W
A30	R101	0	0757-0435	R-F 3.92K1%
A30	R103	6	0757-0415	R-F 475 1% .125W
A30	R104	3	0757-0280	R-F 1K 1% .125W
A30	R105	9	0757-0442	R-F 10K1% .125W
A30	R106	3	0757-0280	R-F 1K 1% .125W
A30	R107	3	0757-0280	R-F 1K 1% .125W
A30	R108	3	0757-0438	R-F 5.11K1%
A30	R110	2	0698-3601	R-F 10 5% 2W MO
A30	R111	6	0757-0415	R-F 475 1% .125W
A30	R120	4	0757-0405	R-F 162 1% .125W
A30	R121	0	0698-4392	R-F 71.5 1/8W 1%
A30	RA1	7	1810-0338	R-NETW 100X8 DIL
A30	RA2	7	1810-0338	R-NETW 100X8 DIL
A30	RA3	5	1810-0203	R-NETWORK 7X470
A30	RA4	2	1810-0713	R-NETWORK 10 PIN
A30	RA5	1	1810-0712	R-NETWORK 8 PIN
A30	RA6	1	1810-0712	R-NETWORK 8 PIN
A30	RA7	5	1810-0203	R-NETWORK 7X470
A30	RA8	2	1810-0713	R-NETWORK 10 PIN

REFERENCE DESIGNATOR		C D	H-P PART NUMBER	DESCRIPTION
A30	RA9	2	1810-0713	R-NETWORK 10 PIN
A30	RA10	1	1810-0712	R-NETWORK 8 PIN
A30	RA11	5	1810-0203	R-NETWORK 7X470
A30	RA12	6	1810-0204	R-NETW 1.0KX7
A30	RA13	6	1810-0204	R-NETW 1.0KX7
A30	RA14	6	1810-0204	R-NETW 1.0KX7
A30	RA15	1	1810-0712	R-NETWORK 8 PIN
A30	RA16	1	1810-0712	R-NETWORK 8 PIN
A30	RA17	2	1810-0713	R-NETWORK 10 PIN
A30	RA18	1	1810-0712	R-NETWORK 8 PIN
A30	RA20	1	1810-0613	R-F NET 8-DIP
A30	RA30	5	1810-0229	R-NETWORK 7X330
A30	RA31	5	1810-0229	R-NETWORK 7X330
A30	RA32	5	1810-0229	R-NETWORK 7X330
A30	RA33	1	1810-0712	R-NETWORK 8 PIN
A30	RA34	2	1810-0713	R-NETWORK 10 PIN
A30	RA35	8	1810-1593	NETWORK-RES
A30	RA36	8	1810-1593	NETWORK-RES
A30	RA37	1	1810-0712	R-NETWORK 8 PIN
A30	RA38	1	1810-0712	R-NETWORK 8 PIN
A30	RA50	5	1810-0229	R-NETWORK 7X330
A30	RA52	6	1810-0337	R-NETWORK 8X4.7K
A30	RA60	2	1810-0713	R-NETWORK 10 PIN
A30	RA61	1	1810-0712	R-NETWORK 8 PIN
A30	RA62	5	1810-0229	R-NETWORK 7X330
A30	RA63	1	1810-0712	R-NETWORK 8 PIN
A30	RA64	1	1810-0712	R-NETWORK 8 PIN
A30	RA80	2	1810-0713	R-NETWORK 10 PIN
A30	RA81	1	1810-0712	R-NETWORK 8 PIN
A30	RA83	8	1810-0272	R-NETW 330.0 X9
A30	RA84	8	1810-0272	R-NETW 330.0 X9
A30	RA85	4	1810-0385	R-NETWORK 470X15
A30	RA86	1	1810-0712	R-NETWORK 8 PIN
A30	RA87	1	1810-0712	R-NETWORK 8 PIN
A30	RA89	4	1810-0301	R-NETWORK 16-PIN
A30	RA100	8	1810-0256	ARRAY 1K X 15
A30	RA102	8	1810-0256	ARRAY 1K X 15
A30	RA200	6	1810-0204	R-NETW 1.0KX7
A30	RA201	6	1810-0204	R-NETW 1.0KX7
A30	RA203	2	1810-0713	R-NETWORK 10 PIN
A30	RA204	2	1810-0713	R-NETWORK 10 PIN
A30	RA205	2	1810-0713	R-NETWORK 10 PIN
A30	RA215	1	1810-0712	R-NETWORK 8 PIN
A30	RA221	1	1810-0712	R-NETWORK 8 PIN
A30	RA223	1	1810-0712	R-NETWORK 8 PIN
A30	TP1	6	0360-2264	TEST POINT
A30	TP3	3	1250-1918	TEST-JACK
A30	TP4	6	0360-2264	TEST POINT
A30	TP5	3	1250-1918	TEST-JACK
A30	TP6	6	0360-2264	TEST POINT
A30	TP7	6	0360-2264	TEST POINT
A30	TP8	3	1250-1918	TEST-JACK
A30	TP9	6	0360-2264	TEST POINT
A30	TP10	6	0360-2264	TEST POINT
A30	TP11	6	0360-2264	TEST POINT
A30	TP12	6	0360-2264	TEST POINT
A30	TP13	3	1250-1918	TEST-JACK
A30	TP14	6	0360-2264	TEST POINT
A30	TP15	6	0360-2264	TEST POINT
A30	TP16	3	1250-1918	TEST-JACK
A30	U1	4	1820-3461	IC MC 10H115 P
A30	U2	4	1820-3461	IC MC 10H115 P
A30	U3	9	1820-2848	IC MC10H116P
A30	U5	9	1820-2822	IC MC10H105P
A30	U7	2	1820-3576	IC DIG 10H175

REFERENCE DESIGNATOR		C D	H-P PART NUMBER	DESCRIPTION
A30	U8	2	1820-3576	IC DIG 10H175
A30	U9	2	1816-1462	IC HM10422
A30	U10	2	1816-1462	IC HM10422
A30	U11	0	1820-2956	IC MC10H107P
A30	U12	0	1820-2956	IC MC10H107P
A30	U13	2	1820-3576	IC DIG 10H175
A30	U14	0	1820-2849	IC MC10H131P
A30	U16	9	1820-2848	IC MC10H116P
A30	U17	2	1820-3576	IC DIG 10H175
A30	U18	0	1820-2823	IC MC10H102P
A30	U19	0	1820-2849	IC MC10H131P
A30	U20	0	1820-2956	IC MC10H107P
A30	U21	9	1826-0139	IC 1458
A30	U22	4	1820-2900	IC MC 10H109P
A30	U23	9	1820-2848	IC MC10H116P
A30	U30	2	1816-1462	IC HM10422
A30	U31	2	1816-1462	IC HM10422
A30	U32	3	1820-2157	IC MC 3450P
A30	U33	3	1820-2157	IC MC 3450P
A30	U34	9	1826-0501	ANLG MUXR
A30	U35	9	1826-0501	ANLG MUXR
A30	U36	9	1826-0501	ANLG MUXR
A30	U37	0	1820-2956	IC MC10H107P
A30	U38	0	1820-2956	IC MC10H107P
A30	U39	0	1820-2956	IC MC10H107P
A30	U40	2	1820-3576	IC DIG 10H175
A30	U41	2	1820-3576	IC DIG 10H175
A30	U43	0	1820-1990	IC MC10100L
A30	U44	0	1820-1990	IC MC10100L
A30	U45	9	1820-2822	IC MC10H105P
A30	U46	2	1820-2403	IC MC10186P
A30	U47	8	1820-0817	IC MC10131P
A30	U48	2	1820-2891	IC MC10H101P
A30	U49	2	1820-2891	IC MC10H101P
A30	U50	1	1826-0975	IC 9685
A30	U51	1	1826-0975	IC 9685
A30	U52	9	1826-0139	IC 1458
A30	U53	0	1820-2849	IC MC10H131P
A30	U54	1	1820-0802	IC MC10102P
A30	U55	1	1820-0802	IC MC10102P
A30	U56	0	1826-0718	IC MC1404U5
A30	U57	0	1820-2823	IC MC10H102P
A30	U59	5	1820-0806	IC MC10109P
A30	U60	2	1820-0811	IC MC10117P
A30	U61	2	1820-0803	IC MC10105P
A30	U62	0	1820-2849	IC MC10H131P
A30	U63	4	1820-2611	IC 100 101 DC
A30	U64	9	1820-2848	IC MC10H116P
A30	U65	5	1820-1383	IC MC 10138L
A30	U66	1	1813-0435	CLOCK OSC.1MHZ
A30	U67	3	1826-0315	IC 348
A30	U68	9	1826-0501	ANLG MUXR
A30	U69	7	1820-1442	IC SN74LS290N
A30	U70	6	1820-1425	IC SN74LS132N
A30	U71	9	1820-1197	IC SN74LS00N
A30	U72	9	1820-1197	IC SN74LS00N
A30	U73	9	1820-1204	IC SN74LS20N
A30	U74	7	1820-1202	IC SN74LS10N
A30	U75	8	1820-1112	IC SN74LS74AN
A30	U76	4	1826-0639	D/A 8-BIT
A30	U77	5	1826-0276	IC MC78L05ACP
A30	U78	5	1820-1052	IC MC10125L
A30	U79	4	1820-0805	IC MC10107P
A30	U80	4	1820-3578	IC DIG 10H162
A30	U81	4	1820-3578	IC DIG 10H162
A30	U82	0	1820-2849	IC MC10H131P
A30	U83	0	1820-2849	IC MC10H131P
A30	U84	8	1820-2962	IC MC10H103P
A30	U85	2	1820-2891	IC MC10H101P
A30	U86	4	1820-2900	IC MC 10H109P
A30	U87	3	1820-2959	IC MC10H158P
A30	U88	4	1826-1281	IC VOLT.REG.-5V
A30	U89	2	1820-2891	IC MC10H101P
A30	U90	4	1820-3461	IC MC 10H115 P
A30	U92	9	1820-2848	IC MC10H116P
A30	U93	3	1820-2157	IC MC 3450P
A30	U94	0	1820-2823	IC MC10H102P
A30	U100	3	1820-1216	IC SN74LS138N
A30	U101	3	1820-1216	IC SN74LS138N
A30	U102	2	1820-1281	IC SN74LS139N
A30	U103	4	1820-2075	IC SN74LS245N
A30	U104	1	1820-1173	IC MC10124L
A30	U105	1	1820-1173	IC MC10124L
A30	U106	1	1820-1173	IC MC10124L
A30	U107	1	1820-1173	IC MC10124L
A30	U108	1	1820-1173	IC MC10124L
A30	U109	1	1820-1173	IC MC10124L
A30	U110	1	1820-1206	IC SN74LS 27N
A30	U111	8	1820-1568	IC SN74LS125AN
A30	U112	7	1820-1195	IC SN74LS175N
A30	U113	8	1826-0138	IC 339
A30	U114	8	1826-0138	IC 339
A30	U115	6	1820-1730	IC SN74LS273N
A30	U116	8	1826-0138	IC 339
A30	U117	8	1826-0138	IC 339
A30	U118	6	1820-1730	IC SN74LS273N
A30	U119	7	1820-1278	IC SN74LS191N
A30	U120	7	1820-1278	IC SN74LS191N
A30	U121	6	1820-1201	IC SN74LS08N
A30	U122	8	1826-0138	IC 339
A30	U123	8	1826-0138	IC 339
A30	U124	7	1820-1195	IC SN74LS175N
A30	U125	7	1820-1195	IC SN74LS175N
A30	U126	8	1826-0138	IC 339
A30	U127	8	1826-0138	IC 339
A30	U128	6	1820-1730	IC SN74LS273N
A30	U129	6	1820-1730	IC SN74LS273N
A30	U130	6	1820-1730	IC SN74LS273N
A30	U131	1	1820-1173	IC MC10124L
A30	U132	8	1826-0138	IC 339
A30	U133	8	1826-0138	IC 339
A30	U134	1	1826-0412	IC 393
A30	U201	9	1820-2963	IC-MC10H210P T
A30	U202	0	1820-3102	IC MC 10H016L
A30	U203	0	1820-2849	IC MC10H131P
A30	U204	0	1820-3102	IC MC 10H016L
A30	U205	0	1820-3102	IC MC 10H016L
A30	U206	0	1820-3102	IC MC 10H016L
A30	U207	0	1820-3102	IC MC 10H016L
A30	U208	0	1820-3102	IC MC 10H016L
A30	U209	4	1820-3338	IC MC 10 H 117
A30	U210	9	1820-2822	IC MC10H105P
A30	U211	4	1820-2900	IC MC 10H109P
A30	U212	4	1820-2900	IC MC 10H109P
A30	U214	0	1820-2849	IC MC10H131P
A30	U215	0	1820-3102	IC MC 10H016L
A30	U216	0	1820-3102	IC MC 10H016L
A30	U217	0	1820-3102	IC MC 10H016L

REFERENCE DESIGNATOR		C D	H-P PART NUMBER	DESCRIPTION
A31	08175-66531			BD AY EXTENDER
A31	C300	8	0160-6080	C-F .068UF 50VDC
A31	C301	8	0160-6080	C-F .068UF 50VDC
A31	C302	0	0160-5737	C-F 68PF 5% 100V
A31	R300	2	0757-0411	R-F 332 1% .125W
A31	R301	2	0757-0411	R-F 332 1% .125W
A31	R302	6	0757-0283	R-F 2K1% .125W F
A31	RA300	5	1810-0229	R-NETWORK 7X330
A31	U300	0	1820-2849	IC MC10H131P
A31	U301	0	1820-2849	IC MC10H131P
A31	U302	0	1820-2823	IC MC10H102P
A40	08175-66540			BD AY-DATA
A40	C1	6	0180-2208	C-F 220UF10% 10V
A40	C2	6	0180-2208	C-F 220UF10% 10V
A40	C3	6	0180-2208	C-F 220UF10% 10V
A40	C4	6	0180-2208	C-F 220UF10% 10V
A40	C5	8	0160-6080	C-F .068UF 50VDC
A40	C6	8	0160-6080	C-F .068UF 50VDC
A40	C7	8	0160-6080	C-F .068UF 50VDC
A40	C8	8	0160-6080	C-F .068UF 50VDC
A40	C9	8	0160-6080	C-F .068UF 50VDC
A40	C10	8	0160-6080	C-F .068UF 50VDC
A40	C11	8	0160-6080	C-F .068UF 50VDC
A40	C12	8	0160-6080	C-F .068UF 50VDC
A40	C13	8	0160-6080	C-F .068UF 50VDC
A40	C14	8	0160-6080	C-F .068UF 50VDC
A40	C15	8	0160-6080	C-F .068UF 50VDC
A40	C16	8	0160-6080	C-F .068UF 50VDC
A40	C17	8	0160-6080	C-F .068UF 50VDC
A40	C18	8	0160-6080	C-F .068UF 50VDC
A40	C19	8	0160-6080	C-F .068UF 50VDC
A40	C20	8	0160-6080	C-F .068UF 50VDC
A40	C21	8	0160-6080	C-F .068UF 50VDC
A40	C22	8	0160-6080	C-F .068UF 50VDC
A40	C23	8	0160-6080	C-F .068UF 50VDC
A40	C24	8	0160-6080	C-F .068UF 50VDC
A40	C26	8	0160-6080	C-F .068UF 50VDC
A40	C27	8	0160-6080	C-F .068UF 50VDC
A40	C28	8	0160-6080	C-F .068UF 50VDC
A40	C29	8	0160-6080	C-F .068UF 50VDC
A40	C30	8	0160-6080	C-F .068UF 50VDC
A40	C31	8	0160-6080	C-F .068UF 50VDC
A40	C32	8	0160-6080	C-F .068UF 50VDC
A40	C33	8	0160-6080	C-F .068UF 50VDC
A40	C34	8	0160-6080	C-F .068UF 50VDC
A40	C35	8	0160-6080	C-F .068UF 50VDC
A40	C36	8	0160-6080	C-F .068UF 50VDC
A40	C37	8	0160-6080	C-F .068UF 50VDC
A40	C38	8	0160-6080	C-F .068UF 50VDC
A40	C39	8	0160-6080	C-F .068UF 50VDC
A40	C40	8	0160-6080	C-F .068UF 50VDC
A40	C41	8	0160-6080	C-F .068UF 50VDC
A40	C42	8	0160-6080	C-F .068UF 50VDC
A40	C43	8	0160-6080	C-F .068UF 50VDC
A40	C44	8	0160-6080	C-F .068UF 50VDC
A40	C50	7	0160-4380	C-F 1PF 200V
A40	C51	8	0160-5743	C-F 82PF 5% 100V
A40	C52	6	0160-5741	C-F 47PF 5% 100V
A40	C53	6	0160-5741	C-F 47PF 5% 100V
A40	C54	6	0160-5741	C-F 47PF 5% 100V
A40	C100	8	0160-6080	C-F .068UF 50VDC
A40	C101	8	0160-6080	C-F .068UF 50VDC
A40	CR1	9	1901-0535	DIO SCHOT HP2311
A40	CR2	2	1901-0033	DIO 180V .2A
A40	DL1	4	1810-0616	DELAY LINE 14PIN
A40	DL2	4	1810-0616	DELAY LINE 14PIN
A40	J7	2	1251-7799	3X32 PLUG
A40	J8	2	1251-7799	3X32 PLUG
A40	L1	0	9170-0894	CORE MAGNETIC
A40	L2	0	9170-0894	CORE MAGNETIC
A40	L3	0	9170-0894	CORE MAGNETIC
A40	MP2	6	0361-0521	RIVET SEMITUB
A40	MP3	6	0361-0521	RIVET SEMITUB
A40	MP4	6	0361-0521	RIVET SEMITUB
A40	MP5	6	0361-0521	RIVET SEMITUB
A40	MP6	7	08175-21704	BUSHING SHORT
A40	MP7	3	08175-26106	PC PIN

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REFERENCE DESIGNATOR		CD	H-P PART NUMBER	DESCRIPTION
A40	R1	9	0757-0278	R-F 1.78K1%
A40	R2	9	0757-0278	R-F 1.78K1%
A40	R3	9	0757-0278	R-F 1.78K1%
A40	R4	9	0757-0278	R-F 1.78K1%
A40	R5	9	0757-0278	R-F 1.78K1%
A40	R6	9	0757-0278	R-F 1.78K1%
A40	R8	9	0757-0278	R-F 1.78K1%
A40	R9	9	0757-0278	R-F 1.78K1%
A40	R10	9	0757-0278	R-F 1.78K1%
A40	R11	9	0757-0278	R-F 1.78K1%
A40	R12	9	0757-0278	R-F 1.78K1%
A40	R13	3	0757-0280	R-F 1K 1% .125W
A40	R14	3	0757-0280	R-F 1K 1% .125W
A40	R15	3	0757-0280	R-F 1K 1% .125W
A40	R16	0	0757-0401	R-F 100 1% .125W
A40	R17	1	0757-0410	R-F 301 1% .125W
A40	R18	3	0757-0280	R-F 1K 1% .125W
A40	R19	0	0757-0401	R-F 100 1% .125W
A40	R20	1	0757-0410	R-F 301 1% .125W
A40	R21	3	0757-0280	R-F 1K 1% .125W
A40	R22	9	0757-0442	R-F 10K1% .125W
A40	R23	9	0757-0442	R-F 10K1% .125W
A40	R25	1	0698-3444	R-F 316 1% .125W
A40	R26	9	0757-0442	R-F 10K1% .125W
A40	R27	9	0757-0442	R-F 10K1% .125W
A40	R28	9	0757-0442	R-F 10K1% .125W
A40	R30	7	0698-0082	R-F 464 1% .125W
A40	R31	1	0757-0410	R-F 301 1% .125W
A40	R32	7	0698-0082	R-F 464 1% .125W
A40	R35	4	0757-0984	R-F 10 1% 1/2W F
A40	R40	2	0757-0403	R-F 121 1% .125W
A40	R41	4	0698-3439	R-F 178 1% .125W
A40	R42	7	0698-0082	R-F 464 1% .125W
A40	R43	7	0698-0082	R-F 464 1% .125W
A40	R66	6	2100-3252	RES-TRMR 5K 10%
A40	RA1	8	1810-0272	R-NETW 330.0 X9
A40	RA2	8	1810-0272	R-NETW 330.0 X9
A40	RA3	8	1810-0272	R-NETW 330.0 X9
A40	RA4	8	1810-0272	R-NETW 330.0 X9
A40	RA5	8	1810-0272	R-NETW 330.0 X9
A40	RA6	8	1810-0272	R-NETW 330.0 X9
A40	RA7	2	1810-0713	R-NETWORK 10 PIN
A40	RA8	2	1810-0713	R-NETWORK 10 PIN
A40	RA9	1	1810-0712	R-NETWORK 8 PIN
A40	RA10	1	1810-0712	R-NETWORK 8 PIN
A40	RA11	2	1810-0713	R-NETWORK 10 PIN
A40	RA12	0	1810-1595	NETWORK-RES
A40	RA13	0	1810-1595	NETWORK-RES
A40	RA14	0	1810-1595	NETWORK-RES
A40	RA15	0	1810-1595	NETWORK-RES
A40	RA16	0	1810-1595	NETWORK-RES
A40	RA17	0	1810-1595	NETWORK-RES
A40	RA18	0	1810-1595	NETWORK-RES
A40	RA19	0	1810-1595	NETWORK-RES
A40	RA20	1	1810-0712	R-NETWORK 8 PIN
A40	RA21	2	1810-0713	R-NETWORK 10 PIN
A40	RA22	2	1810-0713	R-NETWORK 10 PIN
A40	RA23	1	1810-0712	R-NETWORK 8 PIN
A40	RA24	1	1810-0275	R-NETW 9X1KOHM
A40	RA25	2	1810-0713	R-NETWORK 10 PIN
A40	RA26	2	1810-0713	R-NETWORK 10 PIN
A40	RA27	2	1810-0713	R-NETWORK 10 PIN
A40	RA28	1	1810-0712	R-NETWORK 8 PIN
A40	RA29	1	1810-0712	R-NETWORK 8 PIN
A40	RA30	2	1810-0713	R-NETWORK 10 PIN
A40	RA31	1	1810-0712	R-NETWORK 8 PIN
A40	RA32	2	1810-0713	R-NETWORK 10 PIN

REFERENCE DESIGNATOR		CD	H-P PART NUMBER	DESCRIPTION
A40	RA33	2	1810-0713	R-NETWORK 10 PIN
A40	RA34	2	1810-0713	R-NETWORK 10 PIN
A40	RA35	1	1810-0712	R-NETWORK 8 PIN
A40	RA36	2	1810-0713	R-NETWORK 10 PIN
A40	RA37	1	1810-0712	R-NETWORK 8 PIN
A40	RA38	1	1810-0712	R-NETWORK 8 PIN
A40	RA39	2	1810-0713	R-NETWORK 10 PIN
A40	RA40	5	1810-0203	R-NETWORK 7X470
A40	RA41	1	1810-0712	R-NETWORK 8 PIN
A40	RA42	1	1810-0712	R-NETWORK 8 PIN
A40	RA43	2	1810-0713	R-NETWORK 10 PIN
A40	RA44	9	1810-0273	R-NETW 10P 470X9
A40	RA45	9	1810-0273	R-NETW 10P 470X9
A40	RA46	9	1810-0273	R-NETW 10P 470X9
A40	RA47	9	1810-0273	R-NETW 10P 470X9
A40	RA48	9	1810-0273	R-NETW 10P 470X9
A40	RA49	9	1810-0273	R-NETW 10P 470X9
A40	RA50	5	1810-0203	R-NETWORK 7X470
A40	RA51	8	1810-0280	R-NETWORK 9X10K
A40	RA52	2	1810-0713	R-NETWORK 10 PIN
A40	RA53	9	1810-0273	R-NETW 10P 470X9
A40	RA54	1	1810-0712	R-NETWORK 8 PIN
A40	RA55	8	1810-1593	NETWORK-RES
A40	RA56	8	1810-1593	NETWORK-RES
A40	RA57	8	1810-1593	NETWORK-RES
A40	RA58	8	1810-1593	NETWORK-RES
A40	RA59	8	1810-1593	NETWORK-RES
A40	RA60	8	1810-1593	NETWORK-RES
A40	RA61	8	1810-1593	NETWORK-RES
A40	RA62	8	1810-1593	NETWORK-RES
A40	RA70	5	1810-0229	R-NETWORK 7X330
A40	RA71	1	1810-0712	R-NETWORK 8 PIN
A40	TP1	6	0360-2264	TEST POINT
A40	TP2	3	1250-1918	TEST-JACK
A40	TP3	6	0360-2264	TEST POINT
A40	TP4	3	1250-1918	TEST-JACK
A40	TP5	6	0360-2264	TEST POINT
A40	TP6	3	1250-1918	TEST-JACK
A40	TP7	3	1250-1918	TEST-JACK
A40	TP8	3	1250-1918	TEST-JACK
A40	TP9	6	0360-2264	TEST POINT
A40	TP10	3	1250-1918	TEST-JACK
A40	TP11	3	1250-1918	TEST-JACK
A40	TP12	3	1250-1918	TEST-JACK
A40	U1	9	1820-2848	IC MC10H116P
A40	U2	0	1820-2823	IC MC10H102P
A40	U3	0	1820-3102	IC MC 10H016L
A40	U4	5	1820-3222	IC 74F190PC
A40	U5	5	1820-3222	IC 74F190PC
A40	U6	5	1820-3222	IC 74F190PC
A40	U7	5	1820-3222	IC 74F190PC
A40	U8	5	1820-3222	IC 74F190PC
A40	U9	4	1820-3461	IC MC 10H115 P
A40	U10	5	1820-1052	IC MC10125L
A40	U11	1	1820-1173	IC MC10124L
A40	U12	8	1820-1287	IC-SN74LS37N
A40	U14	5	1820-3339	IC MC 10 H119
A40	U15	0	1820-3102	IC MC 10H016L
A40	U16	0	1820-3102	IC MC 10H016L
A40	U17	0	1820-3102	IC MC 10H016L
A40	U18	0	1820-2849	IC MC10H131P
A40	U19	2	1820-3435	IC MC10H209L
A40	U20	2	1820-3435	IC MC10H209L
A40	U21	9	1820-2963	IC-MC10H210P T

REFERENCE DESIGNATOR		C D	H-P PART NUMBER	DESCRIPTION
A40	U22	0	1820-3102	IC MC 10H016L
A40	U23	2	1820-3435	IC MC10H209L
A40	U24	3	1820-3337	IC MC10H104P
A40	U25	5	1820-3579	IC DIG 10H141
A40	U26	5	1820-3579	IC DIG 10H141
A40	U27	5	1820-3579	IC DIG 10H141
A40	U28	5	1820-3579	IC DIG 10H141
A40	U29	8	1820-3580	IC DIG 10H161
A40	U30	0	1820-2849	IC MC10H131P
A40	U31	0	1820-2956	IC MC10H107P
A40	U32	0	1820-2849	IC MC10H131P
A40	U33	0	1820-2849	IC MC10H131P
A40	U34	8	1820-3340	IC MC 10H121P
A40	U35	2	1820-3435	IC MC10H209L
A40	U36	3	1820-3337	IC MC10H104P
A40	U37	9	1820-2822	IC MC10H105P
A40	U38	3	1820-3337	IC MC10H104P
A40	U39	9	1820-2848	IC MC10H116P
A40	U41	0	5180-2447	IC WITH HTSK
A40	U42	0	5180-2447	IC WITH HTSK
A40	U43	0	5180-2447	IC WITH HTSK
A40	U44	0	1820-3102	IC MC 10H016L
A40	U45	0	1820-3102	IC MC 10H016L
A40	U46	0	1820-3102	IC MC 10H016L
A40	U47	0	5180-2447	IC WITH HTSK
A40	U48	0	5180-2447	IC WITH HTSK
A40	U49	0	5180-2447	IC WITH HTSK
A40	U50	8	1820-2962	IC MC10H103P
A40	U51	5	1820-3339	IC MC 10 H119
A40	U52	0	1820-2849	IC MC10H131P
A40	U60	0	1820-3102	IC MC 10H016L
A40	U61	0	1820-3102	IC MC 10H016L
A40	U62	0	1820-3102	IC MC 10H016L
A40	U63	0	1820-3102	IC MC 10H016L
A40	U64	0	1820-2849	IC MC10H131P
A40	U65	5	1820-3339	IC MC 10 H119
A40	U66	0	1820-2823	IC MC10H102P
A40	U67	1	1816-1338	IC 10145ADC
A40	U68	1	1816-1338	IC 10145ADC
A40	U69	1	1816-1338	IC 10145ADC
A40	U70	1	1816-1338	IC 10145ADC
A40	U71	0	1820-3102	IC MC 10H016L
A40	U72	4	1820-3578	IC DIG 10H162
A40	U73	0	1820-2849	IC MC10H131P
A40	U74	0	1820-2849	IC MC10H131P
A40	U76	8	1820-2962	IC MC10H103P
A40	U77	8	1820-2962	IC MC10H103P
A40	U78	0	1820-2849	IC MC10H131P
A40	U79	9	1820-2963	IC-MC10H210P T
A40	U80	2	1820-2891	IC MC10H101P
A40	U81	9	1820-2963	IC-MC10H210P T
A40	U82	4	1820-2900	IC MC 10H109P
A40	U83	3	1820-3337	IC MC10H104P
A40	U84	0	1820-2823	IC MC10H102P
A40	U85	0	1820-2849	IC MC10H131P
A40	U91	4	1820-2075	IC SN74LS245N
A40	U92	2	1820-1281	IC SN74LS139N
A40	U93	3	1820-1216	IC SN74LS138N
A40	U94	3	1820-1208	IC SN74LS32N
A40	U95	1	1820-1173	IC MC10124L
A40	U96	1	1820-1173	IC MC10124L
A40	U97	1	1820-1173	IC MC10124L
A40	U98	1	1820-1173	IC MC10124L
A40	U99	6	1820-1730	IC SN74LS273N
A40	U100	6	1820-1730	IC SN74LS273N

REFERENCE DESIGNATOR		C D	H-P PART NUMBER	DESCRIPTION
A40	U104	1	1820-1173	IC MC10124L
A40	U105	8	1820-3580	IC DIG 10H161
A40	U106	8	1820-3580	IC DIG 10H161
A40	U107	1	1820-1173	IC MC10124L
A40	U108	1	1820-1173	IC MC10124L
A40	U109	1	1820-1173	IC MC10124L
A40	U111	3	1820-1315	ANLG MUXR
A40	U112	3	1820-1315	ANLG MUXR
A40	U113	3	1820-1315	ANLG MUXR
A40	U114	3	1820-1315	ANLG MUXR
A40	U115	3	1820-1315	ANLG MUXR
A40	U116	3	1820-1315	ANLG MUXR
A40	U117	3	1820-1315	ANLG MUXR
A40	U118	3	1820-1315	ANLG MUXR
A40	U119	7	1820-1195	IC SN74LS175N
A40	U120	3	1820-2157	IC MC 3450P
A40	U121	3	1820-2157	IC MC 3450P
A40	U122	3	1820-2157	IC MC 3450P
A40	U123	3	1820-2157	IC MC 3450P
A40	U124	9	1826-0501	ANLG MUXR
A40	U125	9	1826-0501	ANLG MUXR
A40	U126	9	1826-0501	ANLG MUXR
A40	U131	9	1820-2822	IC MC10H105P
A40	U132	9	1820-2848	IC MC10H116P
A40	U133	9	1820-2848	IC MC10H116P
A40	U134	9	1820-2848	IC MC10H116P
A40	U135	9	1820-2848	IC MC10H116P
A40	U136	9	1820-2848	IC MC10H116P
A40	U137	9	1820-2848	IC MC10H116P
A40	U138	9	1820-2848	IC MC10H116P
A40	U140	1	5180-2446	IC WITH HTSK
A40	U141	1	5180-2446	IC WITH HTSK
A40	U142	1	5180-2446	IC WITH HTSK
A40	U143	1	5180-2446	IC WITH HTSK
A40	U144	1	5180-2446	IC WITH HTSK
A40	U145	1	5180-2446	IC WITH HTSK
A40	U146	1	5180-2446	IC WITH HTSK
A40	U147	1	5180-2446	IC WITH HTSK
A40	U148	1	5180-2446	IC WITH HTSK
A40	U149	1	5180-2446	IC WITH HTSK
A40	U150	1	5180-2446	IC WITH HTSK
A40	U151	1	5180-2446	IC WITH HTSK
A40	U152	1	5180-2446	IC WITH HTSK
A40	U153	7	5180-2445	IC WITH HTSK
A40	U154	7	5180-2445	IC WITH HTSK
A40	U155	7	5180-2445	IC WITH HTSK
A40	U156	7	5180-2445	IC WITH HTSK
A40	U157	7	5180-2445	IC WITH HTSK
A40	U158	7	5180-2445	IC WITH HTSK
A40	U159	7	5180-2445	IC WITH HTSK
A40	U160	7	5180-2445	IC WITH HTSK
A40	U161	7	5180-2445	IC WITH HTSK
A40	U162	7	5180-2445	IC WITH HTSK
A40	U163	7	5180-2445	IC WITH HTSK
A40	U164	7	5180-2445	IC WITH HTSK
A40	U165	7	5180-2445	IC WITH HTSK
A40	U166	7	5180-2445	IC WITH HTSK
A40	U167	7	5180-2445	IC WITH HTSK
A40	U168	7	5180-2445	IC WITH HTSK
A40	U169	7	5180-2445	IC WITH HTSK
A40	U170	7	5180-2445	IC WITH HTSK
A40	U171	7	5180-2445	IC WITH HTSK
A40	U172	7	5180-2445	IC WITH HTSK
A40	U173	7	5180-2445	IC WITH HTSK
A40	U174	7	5180-2445	IC WITH HTSK

REFERENCE DESIGNATOR		C D	H-P PART NUMBER	DESCRIPTION
A40	U175	7	5180-2445	IC WITH HTSK
A40	U176	7	5180-2445	IC WITH HTSK
A40	U178	9	1820-2963	IC-MC10H210P T
A40	U185	2	1816-1462	IC HM10422
A40	U186	2	1816-1462	IC HM10422
A40	U187	2	1816-1462	IC HM10422
A40	U188	2	1816-1462	IC HM10422
A40	U189	2	1816-1462	IC HM10422
A40	U200	3	1820-2157	IC MC 3450P
A40	U201	8	1820-1203	IC SN74LS11N
A40	U202	0	1820-2691	IC 74F74PC
A40	U203	0	1820-2691	IC 74F74PC
A40	U204	8	1820-1568	IC SN74LS125AN
A40	W1	5	1460-0579	WIREFORM
A40	W2	5	1460-0579	WIREFORM
A40	W3	5	1460-0579	WIREFORM
A40	W4	5	1460-0579	WIREFORM
A40	W5	5	1460-0579	WIREFORM
A40	W100	0	8159-0005	RES ZERO OHMS
A40	W101	0	8159-0005	RES ZERO OHMS
A40	W102	0	8159-0005	RES ZERO OHMS
A40	W103	0	8159-0005	RES ZERO OHMS
A40	W104	0	8159-0005	RES ZERO OHMS
A40	W105	0	8159-0005	RES ZERO OHMS
A40	W106	0	8159-0005	RES ZERO OHMS
A40	W107	0	8159-0005	RES ZERO OHMS
A40	W110	2	08175-61606	CBL AY SHLD

A50	08175-66550	BD AY-BUFFER

A50	C1	6	0180-2208	C-F 220UF10% 10V
A50	C2	6	0180-2208	C-F 220UF10% 10V
A50	C3	6	0180-2208	C-F 220UF10% 10V
A50	C4	3	0180-1794	C-F 22UF 35V
A50	C5	3	0180-1794	C-F 22UF 35V
A50	C6	6	0180-2208	C-F 220UF10% 10V
A50	C7	8	0160-6080	C-F .068UF 50VDC
A50	C8	8	0160-6080	C-F .068UF 50VDC
A50	C9	8	0160-6080	C-F .068UF 50VDC
A50	C10	8	0160-6080	C-F .068UF 50VDC
A50	C11	8	0160-6080	C-F .068UF 50VDC
A50	C12	8	0160-6080	C-F .068UF 50VDC
A50	C16	8	0160-6080	C-F .068UF 50VDC
A50	C17	8	0160-6080	C-F .068UF 50VDC
A50	C18	8	0160-6080	C-F .068UF 50VDC
A50	C19	8	0160-6080	C-F .068UF 50VDC
A50	C20	8	0160-6080	C-F .068UF 50VDC
A50	C21	8	0160-6080	C-F .068UF 50VDC
A50	C22	8	0160-6080	C-F .068UF 50VDC
A50	C23	8	0160-6080	C-F .068UF 50VDC
A50	C24	8	0160-6080	C-F .068UF 50VDC
A50	C25	8	0160-6080	C-F .068UF 50VDC
A50	C26	8	0160-6080	C-F .068UF 50VDC
A50	C27	8	0160-6080	C-F .068UF 50VDC
A50	C28	8	0160-6080	C-F .068UF 50VDC
A50	C29	8	0160-6080	C-F .068UF 50VDC
A50	C30	8	0160-6080	C-F .068UF 50VDC
A50	C31	8	0160-6080	C-F .068UF 50VDC
A50	C32	8	0160-6080	C-F .068UF 50VDC
A50	C34	8	0160-6080	C-F .068UF 50VDC
A50	C35	8	0160-6080	C-F .068UF 50VDC
A50	C36	8	0160-6080	C-F .068UF 50VDC
A50	C37	8	0160-6080	C-F .068UF 50VDC
A50	C40	8	0160-6080	C-F .068UF 50VDC
A50	C41	8	0160-6080	C-F .068UF 50VDC
A50	C42	8	0160-6080	C-F .068UF 50VDC
A50	C43	6	0160-3456	C-F 1000PF 1000V
A50	C44	8	0160-6080	C-F .068UF 50VDC
A50	C45	6	0160-3456	C-F 1000PF 1000V
A50	CR500	9	1901-0535	DIO SCHOT HP2311
A50	CR501	9	1901-0535	DIO SCHOT HP2311
A50	J9	5	1252-0075	CONN-DIN 96 MALE
A50	J10	5	1252-0075	CONN-DIN 96 MALE
A50	J501	0	1251-7705	CONN-POST 28CONT
A50	J502	0	1251-7705	CONN-POST 28CONT
A50	J503	0	1251-7705	CONN-POST 28CONT
A50	MP5	7	08175-21704	BUSHING SHORT
A50	MP6	3	08175-26106	PC PIN
A50	R480	3	0698-3438	R-F 147 1% .125W
A50	R501	3	0757-0280	R-F 1K 1% .125W
A50	R800	4	0698-3603	R-F 12 5% 2W MO
A50	R801	4	0757-0984	R-F 10 1% 1/2W F
A50	RA460	1	1810-0712	R-NETWORK 8 PIN
A50	RA461	5	1810-0203	R-NETWORK 7X470
A50	RA464	1	1810-0712	R-NETWORK 8 PIN
A50	RA469	1	1810-0712	R-NETWORK 8 PIN
A50	RA470	8	1810-0769	R-NETW.9X150
A50	RA471	8	1810-0769	R-NETW.9X150
A50	RA472	8	1810-0769	R-NETW.9X150
A50	RA473	0	1810-0381	R-NETWORK 7X150
A50	RA474	8	1810-0769	R-NETW.9X150
A50	RA475	8	1810-0769	R-NETW.9X150
A50	RA476	2	1810-0713	R-NETWORK 10 PIN
A50	RA477	2	1810-0713	R-NETWORK 10 PIN
A50	RA478	2	1810-0713	R-NETWORK 10 PIN
A50	RA479	2	1810-0713	R-NETWORK 10 PIN
A50	RA540	8	1810-0206	R-NETWORK 7X10K
A50	TP6	6	0360-2264	TEST POINT
A50	U100	4	1820-3461	IC MC 10H115 P
A50	U102	4	1820-3461	IC MC 10H115 P
A50	U103	4	1820-3461	IC MC 10H115 P
A50	U104	4	1820-3461	IC MC 10H115 P
A50	U105	4	1820-3461	IC MC 10H115 P
A50	U106	4	1820-3461	IC MC 10H115 P
A50	U107	9	1820-2848	IC MC10H116P
A50	U461	2	1820-2891	IC MC10H101P
A50	U462	1	1820-3400	IC MC 10 H 211
A50	U463	2	1820-2891	IC MC10H101P
A50	U470	5	1820-3595	IC DIGITAL100150
A50	U471	5	1820-3595	IC DIGITAL100150
A50	U472	5	1820-3595	IC DIGITAL100150
A50	U473	5	1820-3595	IC DIGITAL100150
A50	U474	5	1820-3595	IC DIGITAL100150
A50	U540	6	1820-1730	IC SN74LS273N
A50	U542	1	1820-1173	IC MC10124L
A50	U560	4	1820-2075	IC SN74LS245N
A50	U561	3	1820-1208	IC SN74LS32N
A50	U562	3	1820-1216	IC SN74LS138N
A50	U563	2	1820-1281	IC SN74LS139N

OPTION 001 (A52 Fine Timing Board)

REFERENCE DESIGNATOR		C D	H-P PART NUMBER	DESCRIPTION
A50	08175-66552			BD AY FINE TIMING
A50	C1	6	0180-2208	C-F 220UF10% 10V
A50	C2	6	0180-2208	C-F 220UF10% 10V
A50	C3	6	0180-2208	C-F 220UF10% 10V
A50	C4	3	0180-1794	C-F 22UF 35V
A50	C5	3	0180-1794	C-F 22UF 35V
A50	C6	6	0180-2208	C-F 220UF10% 10V
A50	C7	8	0160-6080	C-F .068UF 50VDC
A50	C8	8	0160-6080	C-F .068UF 50VDC
A50	C9	8	0160-6080	C-F .068UF 50VDC
A50	C10	8	0160-6080	C-F .068UF 50VDC
A50	C11	8	0160-6080	C-F .068UF 50VDC
A50	C12	8	0160-6080	C-F .068UF 50VDC
A50	C16	8	0160-6080	C-F .068UF 50VDC
A50	C17	8	0160-6080	C-F .068UF 50VDC
A50	C18	8	0160-6080	C-F .068UF 50VDC
A50	C19	8	0160-6080	C-F .068UF 50VDC
A50	C20	8	0160-6080	C-F .068UF 50VDC
A50	C21	8	0160-6080	C-F .068UF 50VDC
A50	C22	8	0160-6080	C-F .068UF 50VDC
A50	C23	8	0160-6080	C-F .068UF 50VDC
A50	C24	8	0160-6080	C-F .068UF 50VDC
A50	C25	8	0160-6080	C-F .068UF 50VDC
A50	C26	8	0160-6080	C-F .068UF 50VDC
A50	C27	8	0160-6080	C-F .068UF 50VDC
A50	C28	8	0160-6080	C-F .068UF 50VDC
A50	C29	8	0160-6080	C-F .068UF 50VDC
A50	C30	8	0160-6080	C-F .068UF 50VDC
A50	C31	8	0160-6080	C-F .068UF 50VDC
A50	C32	8	0160-6080	C-F .068UF 50VDC
A50	C34	8	0160-6080	C-F .068UF 50VDC
A50	C35	6	0160-6080	C-F .068UF 50VDC
A50	C36	6	0160-6080	C-F .068UF 50VDC
A50	C37	6	0160-6080	C-F .068UF 50VDC
A50	C40	6	0160-6080	C-F .068UF 50VDC
A50	C41	6	0160-6080	C-F .068UF 50VDC
A50	C42	6	0160-6080	C-F .068UF 50VDC
A50	C43	8	0160-3456	C-F 1000PF 1000V
A50	C44	8	0160-6080	C-F .068UF 50VDC
A50	C45	8	0160-3456	C-F 1000PF 1000V
A50	C46	8	0160-6080	C-F .068UF 50VDC
A50	C47	8	0160-6080	C-F .068UF 50VDC
A50	C48	8	0160-6080	C-F .068UF 50VDC
A50	C49	8	0160-6080	C-F .068UF 50VDC
A50	C50	8	0160-6080	C-F .068UF 50VDC
A50	C51	8	0160-6080	C-F .068UF 50VDC
A50	C52	8	0160-6080	C-F .068UF 50VDC
A50	C53	8	0160-6080	C-F .068UF 50VDC
A50	C54	8	0160-6080	C-F .068UF 50VDC
A50	C55	8	0160-6080	C-F .068UF 50VDC
A50	C56	8	0160-6080	C-F .068UF 50VDC
A50	C57	8	0160-6080	C-F .068UF 50VDC
A50	C58	9	0160-6080	C-F .068UF 50VDC
A50	C59	8	0160-6080	C-F .068UF 50VDC
A50	C60	9	0160-6080	C-F .068UF 50VDC
A50	C200	8	0160-5728	C-F 1000PF 5%
A50	C201	8	0160-5728	C-F 1000PF 5%
A50	C210	8	0160-5728	C-F 1000PF 5%
A50	C211	8	0160-5728	C-F 1000PF 5%
A50	C220	8	0160-5728	C-F 1000PF 5%
A50	C221	8	0160-5728	C-F 1000PF 5%
A50	C230	9	0160-5728	C-F 1000PF 5%
A50	C231	9	0160-5728	C-F 1000PF 5%
A50	C360	8	0180-0197	C-F 2.2UF 20V
A50	C361	8	0180-0197	C-F 2.2UF 20V
A50	CR300	6	1901-0376	DIO LOW LEAKAGE
A50	CR301	6	1901-0376	DIO LOW LEAKAGE
A50	CR500	9	1901-0535	DIO SCHOT HP2311
A50	CR501	9	1901-0535	DIO SCHOT HP2311
A50	CR502	9	1901-0535	DIO SCHOT HP2311

REFERENCE DESIGNATOR		C D	H-P PART NUMBER	DESCRIPTION
A50	DL1	4	1810-0616	DELAY LINE 14PIN
A50	J9	2	1251-7799	3X32 PLUG
A50	J10	2	1251-7799	3X32 PLUG
A50	J501	0	1251-7705	CONN-POST 28CONT
A50	J502	0	1251-7705	CONN-POST 28CONT
A50	J503	0	1251-7705	CONN-POST 28CONT
A50	L240	1	9140-0129	IDCTR 220UN 5%
A50	L250	1	9140-0129	IDCTR 220UN 5%
A50	L260	1	9140-0129	IDCTR 220UN 5%
A50	L270	1	9140-0129	IDCTR 220UN 5%
A50	L400	0	9100-2251	COIL-CHOKE .22UH
A50	L410	0	9100-2251	COIL-CHOKE .22UH
A50	L420	0	9100-2251	COIL-CHOKE .22UH
A50	L430	0	9100-2251	COIL-CHOKE .22UH
A50	MP4	6	1205-0033	HT-SINK TO-5
A50	MP5	7	08175-21704	BUSHING SHORT
A50	MP6	3	08175-26106	PC PIN
A50	Q200	3	1854-0720	XSTR SI NPN HF
A50	Q201	3	1854-0720	XSTR SI NPN HF
A50	Q210	3	1854-0720	XSTR SI NPN HF
A50	Q211	3	1854-0720	XSTR SI NPN HF
A50	Q220	3	1854-0720	XSTR SI NPN HF
A50	Q221	3	1854-0720	XSTR SI NPN HF
A50	Q230	3	1854-0720	XSTR SI NPN HF
A50	Q231	3	1854-0720	XSTR SI NPN HF
A50	Q240	5	1854-0392	XSTR 2N 5088
A50	Q241	2	1853-0086	XSTR 2N5087
A50	Q250	5	1854-0392	XSTR 2N 5088
A50	Q251	2	1853-0086	XSTR 2N5087
A50	Q260	5	1854-0392	XSTR 2N 5088
A50	Q261	2	1853-0086	XSTR 2N5087
A50	Q270	5	1854-0392	XSTR 2N 5088
A50	Q271	2	1853-0086	XSTR 2N5087
A50	Q400	9	1854-0809	TRANS.2N 2369A
A50	Q410	9	1854-0809	TRANS.2N 2369A
A50	Q420	9	1854-0809	TRANS.2N 2369A
A50	Q430	9	1854-0809	TRANS.2N 2369A
A50	R103	2	0757-0403	R-F 121 1% .125W
A50	R115	2	0757-0403	R-F 121 1% .125W
A50	R116	6	0757-0407	R-F 200 1% .125W
A50	R200	0	0757-0401	R-F 100 1% .125W
A50	R201	6	0757-0407	R-F 200 1% .125W
A50	R202	5	0698-4462	R-F 768 1% 125
A50	R203	7	0757-0721	R-F 274 1% .25W
A50	R204	6	0757-0407	R-F 200 1% .125W
A50	R205	0	0757-0401	R-F 100 1% .125W
A50	R206	5	0698-4462	R-F 768 1% .125
A50	R210	0	0757-0401	R-F 100 1% .125W
A50	R211	6	0757-0407	R-F 200 1% .125W
A50	R212	5	0698-4462	R-F 768 1% .125
A50	R213	7	0757-0721	R-F 274 1% .25W
A50	R214	6	0757-0407	R-F 200 1% .125W
A50	R215	0	0757-0401	R-F 100 1% .125W
A50	R216	5	0698-4462	R-F 768 1% .125
A50	R220	0	0757-0401	R-F 100 1% .125W
A50	R221	6	0757-0407	R-F 200 1% .125W
A50	R222	5	0698-4462	R-F 768 1% .125
A50	R223	7	0757-0721	R-F 274 1% .25W
A50	R224	6	0757-0407	R-F 200 1% .125W
A50	R225	0	0757-0401	R-F 100 1% .125W
A50	R226	5	0698-4462	R-F 768 1% .125
A50	R230	0	0757-0401	R-F 100 1% .125W
A50	R231	6	0757-0407	R-F 200 1% .125W
A50	R232	5	0698-4462	R-F 768 1% .125
A50	R233	7	0757-0721	R-F 274 1% .25W

REFERENCE DESIGNATOR	CD	H-P PART NUMBER	DESCRIPTION
A50 R234	6	0757-0407	R-F 200 1% .125W
A50 R235	0	0757-0401	R-F 100 1% .125W
A50 R236	5	0698-4462	R-F 768 1% .125
A50 R240	1	0698-3155	R-F 4.64K 1% .125
A50 R241	1	0698-3155	R-F 4.64K 1% .125
A50 R242	8	0698-4457	R-F 576 1% .125W
A50 R243	3	0757-0280	R-F 1K 1% .125W
A50 R244	4	0757-0273	R-F 3.01K1%
A50 R245	1	0698-3155	R-F 4.64K 1% .125
A50 R250	1	0698-3155	R-F 4.64K 1% .125
A50 R251	1	0698-3155	R-F 4.64K 1% .125
A50 R252	8	0698-4457	R-F 576 1% .125W
A50 R253	3	0757-0280	R-F 1K 1% .125W
A50 R254	4	0757-0273	R-F 3.01K1%
A50 R255	1	0698-3155	R-F 4.64K 1% .125
A50 R260	1	0698-3155	R-F 4.64K 1% .125
A50 R261	1	0698-3155	R-F 4.64K 1% .125
A50 R262	8	0698-4457	R-F 576 1% .125W
A50 R263	3	0757-0280	R-F 1K 1% .125W
A50 R264	4	0757-0273	R-F 3.01K1%
A50 R265	1	0698-3155	R-F 4.64K 1% .125
A50 R270	1	0698-3155	R-F 4.64K 1% .125
A50 R271	1	0698-3155	R-F 4.64K 1% .125
A50 R272	8	0698-4457	R-F 576 1% .125W
A50 R273	3	0757-0280	R-F 1K 1% .125W
A50 R274	4	0757-0273	R-F 3.01K1%
A50 R275	1	0698-3155	R-F 4.64K 1% .125
A50 R300	8	0698-4457	R-F 576 1% .125W
A50 R301	9	0757-1094	R-F 1.47K1%
A50 R302	8	0698-4457	R-F 576 1% .125W
A50 R303	9	0757-1094	R-F 1.47K1%
A50 R304	8	0698-4457	R-F 576 1% .125W
A50 R305	9	0757-1094	R-F 1.47K1%
A50 R306	8	0698-4457	R-F 576 1% .125W
A50 R307	9	0757-1094	R-F 1.47K1%
A50 R308	8	0698-4457	R-F 576 1% .125W
A50 R309	9	0757-1094	R-F 1.47K1%
A50 R310	8	0698-4457	R-F 576 1% .125W
A50 R311	9	0757-1094	R-F 1.47K1%
A50 R312	8	0698-4457	R-F 576 1% .125W
A50 R313	9	0757-1094	R-F 1.47K1%
A50 R314	8	0698-4457	R-F 576 1% .125W
A50 R315	9	0757-1094	R-F 1.47K1%
A50 R320	8	0698-4457	R-F 576 1% .125W
A50 R321	9	0757-1094	R-F 1.47K1%
A50 R322	8	0698-4457	R-F 576 1% .125W
A50 R323	9	0757-1094	R-F 1.47K1%
A50 R324	8	0698-4457	R-F 576 1% .125W
A50 R325	9	0757-1094	R-F 1.47K1%
A50 R326	8	0698-4457	R-F 576 1% .125W
A50 R327	9	0757-1094	R-F 1.47K1%
A50 R328	8	0698-4457	R-F 576 1% .125W
A50 R329	9	0757-1094	R-F 1.47K1%
A50 R330	8	0698-4457	R-F 576 1% .125W
A50 R331	9	0757-1094	R-F 1.47K1%
A50 R332	8	0698-4457	R-F 576 1% .125W
A50 R333	9	0757-1094	R-F 1.47K1%
A50 R334	8	0698-4457	R-F 576 1% .125W
A50 R335	9	0757-1094	R-F 1.47K1%
A50 R400	0	0698-3435	R-F 38.3 1%
A50 R402	2	0757-0403	R-F 121 1% .125W
A50 R410	0	0698-3435	R-F 38.3 1%
A50 R412	2	0757-0403	R-F 121 1% .125W
A50 R420	0	0698-3435	R-F 38.3 1%
A50 R422	2	0757-0403	R-F 121 1% .125W

REFERENCE DESIGNATOR	CD	H-P PART NUMBER	DESCRIPTION
A50 R430	0	0698-3435	R-F 38.3 1%
A50 R432	2	0757-0403	R-F 121 1% .125W
A50 R480	3	0698-3438	R-F 147 1% .125W
A50 R501	3	0757-0280	R-F 1K 1% .125W
A50 R600	2	0757-0403	R-F 121 1% .125W
A50 R601	4	0698-3439	R-F 178 1% .125W
A50 R800	4	0698-3603	R-F 12 5% 2W MO
A50 R801	4	0757-0984	R-F 10 1% 1/2W F
A50 RA101	9	1810-0272	R-NETW 10P 470X9
A50 RA102	5	1810-0203	R-NETWORK 7X470
A50 RA112	5	1810-0203	R-NETWORK 7X470
A50 RA460	1	1810-0712	R-NETWORK 8 PIN
A50 RA461	5	1810-0203	R-NETWORK 7X470
A50 RA464	1	1810-0712	R-NETWORK 8 PIN
A50 RA469	1	1810-0712	R-NETWORK 8 PIN
A50 RA470	8	1810-0769	R-NETW.9X150
A50 RA471	8	1810-0769	R-NETW.9X150
A50 RA472	8	1810-0769	R-NETW.9X150
A50 RA473	0	1810-0381	R-NETWORK 7X150
A50 RA474	8	1810-0769	R-NETW.9X150
A50 RA475	8	1810-0769	R-NETW.9X150
A50 RA476	2	1810-0713	R-NETWORK 10 PIN
A50 RA477	2	1810-0713	R-NETWORK 10 PIN
A50 RA478	2	1810-0713	R-NETWORK 10 PIN
A50 RA479	2	1810-0713	R-NETWORK 10 PIN
A50 RA500	8	1810-0280	R-NETWORK 9X10K
A50 RA510	8	1810-0280	R-NETWORK 9X10K
A50 RA520	8	1810-0280	R-NETWORK 9X10K
A50 RA530	8	1810-0280	R-NETWORK 9X10K
A50 RA540	8	1810-0206	R-NETWORK 7X10K
A50 RA550	8	1810-0206	R-NETWORK 7X10K
A50 RA551	8	1810-0206	R-NETWORK 7X10K
A50 RA552	8	1810-0206	R-NETWORK 7X10K
A50 RA553	8	1810-0206	R-NETWORK 7X10K
A50 RA1000	5	1810-0203	R-NETWORK 7X470
A50 RA1001	5	1810-0203	R-NETWORK 7X470
A50 S500	8	3101-2097	SW-SL 6-1A
A50 S501	8	3101-2097	SW-SL 6-1A
A50 S502	8	3101-2097	SW-SL 6-1A
A50 S503	8	3101-2097	SW-SL 6-1A
A50 TP1	3	1250-1918	TEST-JACK
A50 TP2	3	1250-1918	TEST-JACK
A50 TP3	3	1250-1918	TEST-JACK
A50 TP4	3	1250-1918	TEST-JACK
A50 TP5	3	1250-1918	TEST-JACK
A50 TP6	6	0360-2264	TEST POINT
A50 U100	4	1820-3461	IC MC 10H115 P
A50 U101	2	1820-3576	IC DIG 10H175
A50 U102	4	1820-3461	IC MC 10H115 P
A50 U103	4	1820-3461	IC MC 10H115 P
A50 U104	4	1820-3461	IC MC 10H115 P
A50 U105	4	1820-3461	IC MC 10H115 P
A50 U106	4	1820-3461	IC MC 10H115 P
A50 U107	9	1820-2848	IC MC10H116P
A50 U109	2	1820-3435	IC MC10H209L
A50 U112	2	1820-2891	IC MC10H101P
A50 U121	2	1820-3576	IC DIG 10H175
A50 U122	2	1820-2891	IC MC10H101P
A50 U300	3	0960-0685	HYBRID-CIRCUIT
A50 U301	3	0960-0685	HYBRID-CIRCUIT
A50 U302	3	0960-0685	HYBRID-CIRCUIT

REFERENCE DESIGNATOR		CD	H-P PART NUMBER	DESCRIPTION
A50	U303	3	0960-0685	HYBRID-CIRCUIT
A50	U304	3	0960-0685	HYBRID-CIRCUIT
A50	U305	3	0960-0685	HYBRID-CIRCUIT
A50	U306	3	0960-0685	HYBRID-CIRCUIT
A50	U307	3	0960-0685	HYBRID-CIRCUIT
A50	U308	3	0960-0685	HYBRID-CIRCUIT
A50	U309	3	0960-0685	HYBRID-CIRCUIT
A50	U310	3	0960-0685	HYBRID-CIRCUIT
A50	U311	3	0960-0685	HYBRID-CIRCUIT
A50	U312	3	0960-0685	HYBRID-CIRCUIT
A50	U313	3	0960-0685	HYBRID-CIRCUIT
A50	U314	3	0960-0685	HYBRID-CIRCUIT
A50	U315	3	0960-0685	HYBRID-CIRCUIT
A50	U320	3	0960-0685	HYBRID-CIRCUIT
A50	U321	3	0960-0685	HYBRID-CIRCUIT
A50	U322	3	0960-0685	HYBRID-CIRCUIT
A50	U323	3	0960-0685	HYBRID-CIRCUIT
A50	U324	3	0960-0685	HYBRID-CIRCUIT
A50	U325	3	0960-0685	HYBRID-CIRCUIT
A50	U326	3	0960-0685	HYBRID-CIRCUIT
A50	U327	3	0960-0685	HYBRID-CIRCUIT
A50	U328	3	0960-0685	HYBRID-CIRCUIT
A50	U329	3	0960-0685	HYBRID-CIRCUIT
A50	U330	3	0960-0685	HYBRID-CIRCUIT
A50	U331	3	0960-0685	HYBRID-CIRCUIT
A50	U332	3	0960-0685	HYBRID-CIRCUIT
A50	U333	3	0960-0685	HYBRID-CIRCUIT
A50	U334	3	0960-0685	HYBRID-CIRCUIT
A50	U335	3	0960-0685	HYBRID-CIRCUIT
A50	U340	8	1826-0740	ANLG SW
A50	U341	8	1826-0740	ANLG SW
A50	U342	8	1826-0740	ANLG SW
A50	U343	8	1826-0740	ANLG SW
A50	U344	8	1826-0740	ANLG SW
A50	U345	8	1826-0740	ANLG SW
A50	U346	8	1826-0740	ANLG SW
A50	U347	8	1826-0740	ANLG SW
A50	U350	8	1826-0740	ANLG SW
A50	U351	8	1826-0740	ANLG SW
A50	U352	8	1826-0740	ANLG SW
A50	U353	8	1826-0740	ANLG SW
A50	U354	8	1826-0740	ANLG SW
A50	U355	8	1826-0740	ANLG SW
A50	U356	8	1826-0740	ANLG SW
A50	U357	8	1826-0740	ANLG SW
A50	U360	5	1826-0226	IC UA7812HC
A50	U361	6	1826-0178	IC LM320H-12
A50	U440	4	1820-3461	IC MC 10H115 P
A50	U460	2	1820-2891	IC MC10H101P
A50	U461	2	1820-2891	IC MC10H101P
A50	U462	1	1820-3400	IC MC 10 H 211
A50	U463	2	1820-2891	IC MC10H101P
A50	U470	5	1820-3595	IC DIGITAL100150
A50	U471	5	1820-3595	IC DIGITAL100150
A50	U472	5	1820-3595	IC DIGITAL100150
A50	U473	5	1820-3595	IC DIGITAL100150
A50	U474	5	1820-3595	IC DIGITAL100150
A50	U500	6	1820-1730	IC SN74LS273N
A50	U510	6	1820-1730	IC SN74LS273N
A50	U520	6	1820-1730	IC SN74LS273N
A50	U530	6	1820-1730	IC SN74LS273N
A50	U540	6	1820-1730	IC SN74LS273N
A50	U542	1	1820-1173	IC MC10124L
A50	U560	4	1820-2075	IC SN74LS245N
A50	U561	3	1820-1208	IC SN74LS32N
A50	U562	3	1820-1216	IC SN74LS138N
A50	U563	2	1820-1281	IC SN74LS139N
A50	U570	9	1820-1238	IC-SN74LS253N
A50	U580	9	1820-1238	IC-SN74LS253N
A50	U590	9	1820-1238	IC-SN74LS253N
A50	W1	5	1460-0579	WIREFORM
A50	W2	5	1460-0579	WIREFORM
A50	W3	5	1460-0579	WIREFORM

7

BACK-DATING

SECTION 7

BACKDATING

7-1 INTRODUCTION

7-2 This section contains backdating information, which adapts this manual to instruments with serial numbers lower than that shown on the title page.

7-3 Changes are listed in the serial number order that they occured in the manufacture of the instrument. However, in adapting this manual to an instrument with serial number lower than that shown on the title page, apply the changes in reverse order. That is, begin with the latest change that applies to the serial number in question. Table 7-1 lists the serial number to which each change applies. Where changes to components occur, alter the associated schematic and layout diagrams as necessary.

Table 7-1 Manual backdating changes

CHANGE 1 (2 part change) For Serial numbers 2520G000151 and lower.

Part 1: Relating to Board A10 - Power Supply
In Table 6-3 Replaceable Parts, make the following changes:

Parts List for A10, change part numbers and values of following capacitors to read as shown:

A10 C2 0180-3546 C-F 820μF 200V
A10 C3 0180-3546 C-F 820μF 200V

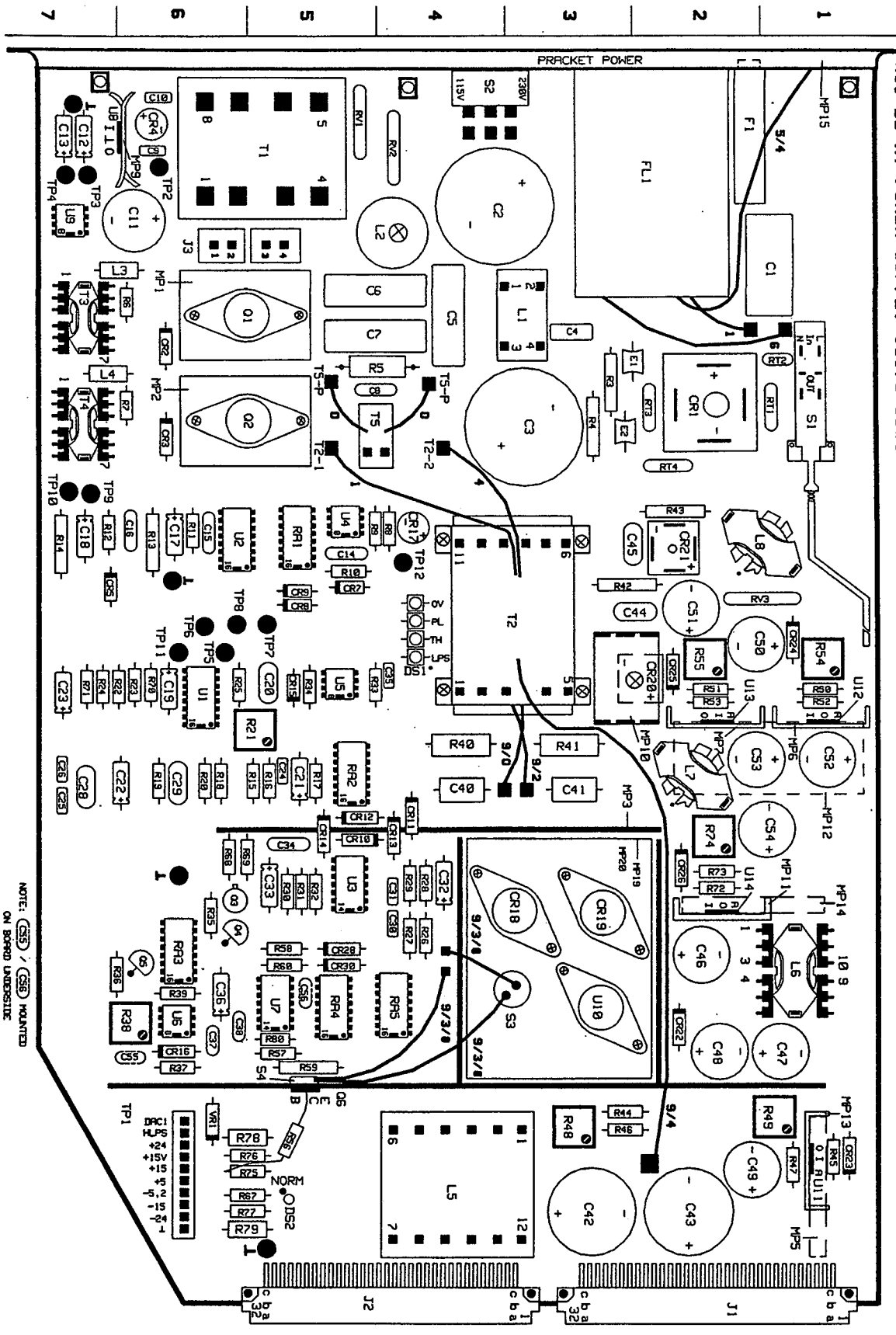
Note that these capacitor values result in time constants (of the circuits they form together with R3 and R4 respectively) of 80 seconds instead of the 100 seconds. Therefore, the corresponding values which appear in the **SAFETY CONSIDERATIONS** warnings of the Theory and Troubleshooting sections can be changed.

Change the values of these capacitors in schematic 10A.
Remove the existing board layout diagram and replace it with the one included here (some components are mounted in different positions).

CHANGE 1
Part 2 Relating to board A51, the Fine Timing Board:

The A51 type board differs significantly from the A52 type. Therefore, a complete service block wtih schematics, theory etc. is included here. Parts lists are also included. Replace the corresponding pages in this manual with the pages included here. It is recommended that you retain the removed pages and insert them in the rear of the manual.

A10 BD AY POWER SUPPLY 88175-66510



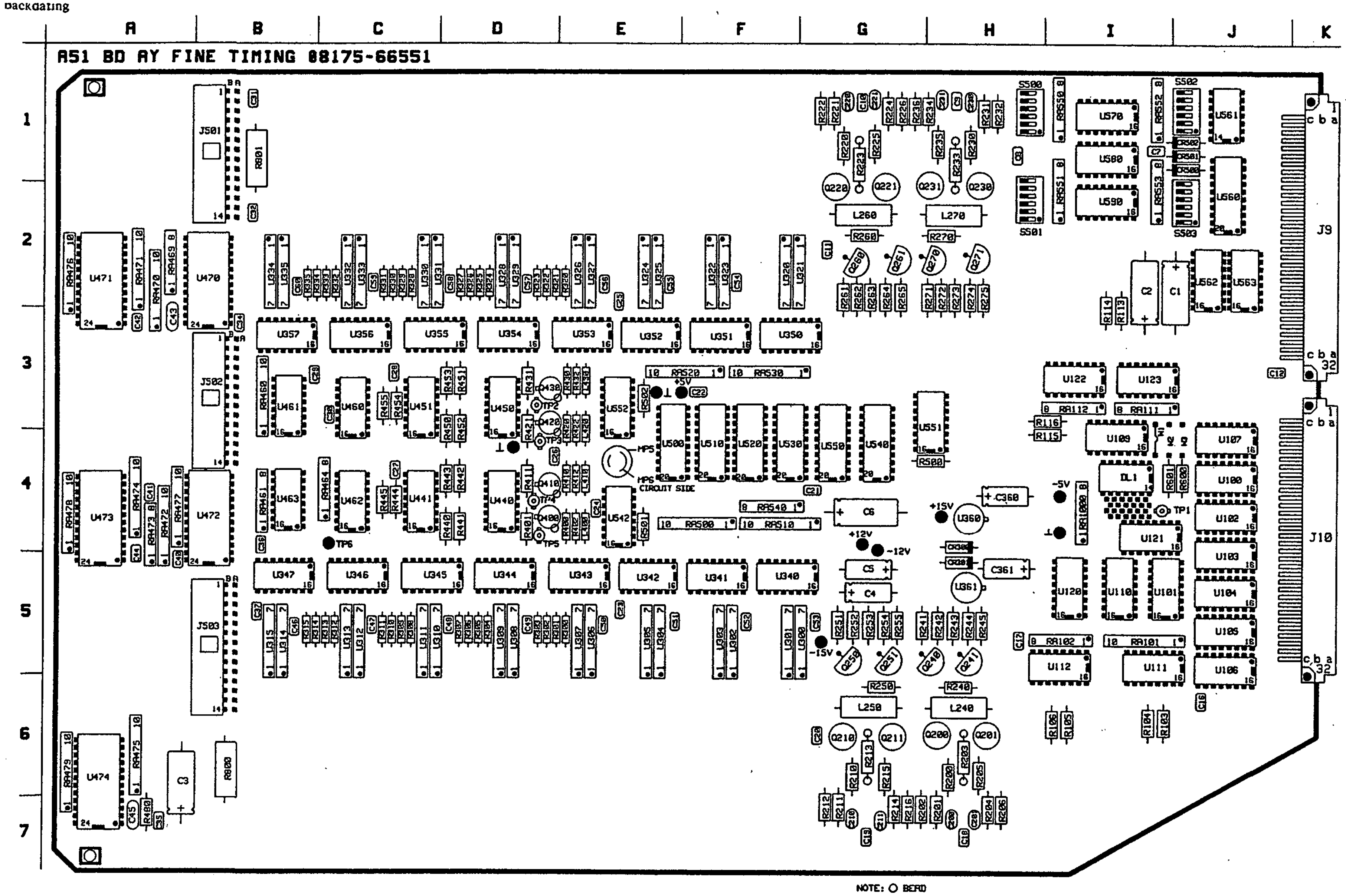
REF DES	GRID LOC
C1	B1/2
C2	A/B1/2
C3	C/D3/4
C4	B/C3
C5	B/C4
C6	B4/5
C7	B4/5
C8	C4/5
C9	A6
C10	A6
C11	A/B6/7
C12	A7
C13	A7
C14	D5
C15	D6
C16	D6
C17	D6
C18	D7
C19	E6
C20	E5
C21	F5
C22	F6
C23	E7
C24	F5
C25	F7
C26	F7
C28	F7
C29	F6
C30	G4
C31	G4
C32	G4
C33	G5
C34	G5
C35	E4
C36	G/H6
C37	H6
C38	H6
C40	F4
C41	F3
C42	I/J3
C43	I/J2
C44	E2/3
C45	D2
C46	G/H2
C47	H1/2
C48	H2
C49	I1/2
C50	E1/2
C51	E2
C52	F1
C53	F1/2
C54	F1/2
C55	H6/7
C56	G/H5

REF DES	GRID LOC
CR1	C/D2
CR2	C6
CR3	D6
CR4	A6
CR5	E6
CR7	E5
CR8	E5
CR9	E5
CR10	G4/5
CR11	F4
CR12	F4/5
CR13	F/G4
CR14	F/G5
CR15	E5
CR16	H6
CR17	D4
CR18	G3/4
CR19	G2/3
CR20	E2/3
CR21	D2
CR22	H2
CR23	I/I
CR24	E1
CR25	E2
CR26	G2
CR28	G5
CR30	H5
DS1	E4
DS2	I5
E1	C2/3
E2	C3
F1	A2
FL1	A/B1/2
J1	J1/2/3
J2	J3/4/5
J3	B5/6
L1	B/C3
L2	B4/5
L3	B6/7
L4	C6/7
L5	I/J3/4
L6	G/H1
L7	F2
L8	D/E1/2
MP1	B/C5/6
MP2	C5/6
MP3	F/G3/4
MP5	I/J1
MP6	F1
MP7	F2
MP9	A6

REF DES	GRID LOC
MP10	E/F2/3
MP11	G2
MP12	F1/2
MP13	I1
MP14	G2/1
MP15	A1
MP19	F/G3/4
MP20	F/G3/4
Q1	B5/6
Q2	C5/6
Q3	G6
Q4	G6
Q5	G/H6/7
Q6	H5
R3	C3
R4	C3
R5	C4/5
R6	B6
R7	C6
R8	D4
R9	D5
R10	D5
R11	D6
R12	D7
R13	D6
R14	D7
R15	F5
R16	F5
R17	F5
R18	F6
R19	F6
R20	F6
R21	F5/6
R22	E6/7
R23	E6
R24	E7
R25	E6
R26	G4
R27	G4
R28	G4
R29	G4
R30	G5
R31	G5
R32	G5
R33	E5
R34	E5
R35	G6
R36	H7
R37	H6
R38	H6/7
R39	H6
R40	F4
R41	F3
R42	E2/3

REF DES	GRID LOC
R43	D2
R44	I3
R45	I1
R46	I3
R47	I1
R48	I3
R49	I1
R50	E1
R51	E2
R52	E1
R53	E2
R54	E1
R55	I2
R56	I5
R57	H5
R58	G5
R59	H5
R60	H5
R67	I6
R68	G6
R69	G6
R70	E6
R71	E7
R72	G2
R73	G2
R74	F/G2
R75	I6
R76	I6
R77	I6
R78	I/J6
R79	H5
R80	H5
RA1	D5
RA2	F5
RA3	G6
RA4	H5
RA5	H5
RT1	C1
RT2	C1
RT3	C2
RT4	D2
RV1	A5
RV2	A4
RV3	E1/2
S1	B/C/D1
S2	A3/4
S3	H4
S4	H5
T1	A5/6
T2	D/E/F3/4
T3	C7
T4	D7
T5	C/D4/5

REF DES	GRID LOC
TP2	A6
TP3	A7
TP4	A7
TP5	E6
TP6	E6
TP7	E5
TP8	E6
TP9	D7
TP10	A7
TP11	E6
TP12	D4
U1	E/F6
U2	D6
U3	C5
U4	D5
U5	F5
U6	H6
U7	H5
U8	A6
U9	B7
U10	G2/3
U11	I1
U12	F1
U13	F2
U14	G2
VR1	I6



REF DES	GRID LOC	REF DES	GRID LOC	REF DES	GRID LOC	REF DES	GRID LOC	REF DES	GRID LOC	REF DES	GRID LOC	REF DES	GRID LOC
C1	J2/3	C60	B2	R103	I6	R270	H2	R443	C4	U100	J4	U345	C/D5
C2	I2/3	C200	H7	R104	I6	R271	G2	R444	C4	U101	J5	U346	C5
C3	A6/7	C201	H7	R105	I6	R272	H2	R445	C4	U102	J4	U347	B5
C4	G5	C210	G7	R106	I6	R273	H2	R450	D3/4	U103	J4/5	U350	F/G3
C5	G5	C211	G7	R113	I2	R274	H2	R451	D3	U104	J5	U351	F3
C6	G4	C220	G1	R114	I2	R275	H2	R452	D3/4	U105	J5	U352	E3
C7	I1	C221	G1	R115	H/I4	R300	E5	R453	D3	U106	J5/6	U353	D/E3
C8	H1	C230	H1	R116	H/I3	R301	D5	R454	C3	U107	J3/4	U354	D3
C9	H1	C231	H1	R200	H7	R302	D5	R455	C3	U109	I3/4	U355	C/D3
C10	G1	C360	H4	R201	H7	R303	D5	R480	A7	U110	I5	U356	C3
C11	G2	C361	H5	R202	G7	R304	D5	R500	G/H4	U111	I6	U357	C3
C12	K3	CR300	H5	R203	H6/7	R305	D5	R501	E4	U112	H/I6	U360	H4
C16	J6	CR301	H5	R204	H7	R306	D5	R502	E3	U120	I5	U361	H5
C17	H5	CR500	J1	R205	H7	R307	D5	R600	J4	U121	I5	U440	D4
C18	H7	CR501	J1	R206	H7	R308	C5	R601	I4	U122	I3	U441	D4
C19	G7	CR502	J1	R210	G7	R309	C5	R800	B6/7	U123	I/J3	U450	D3/4
C20	G6	DL1	I4	R211	G7	R310	C5	R801	B1	U300	G5/6	U451	C3/4
C21	G4	J9	K1/2/3	R212	G7	R311	C5	RA101	I5	U301	F5/6	U460	C3/4
C22	F3	J10	K3/4/5	R213	G6/7	R312	C5	RA102	H/I5	U302	F5/6	U461	B3/4
C23	E5	J501	B1/2	R214	G7	R313	C5	RA111	I3	U303	F5/6	U462	C4
C24	E4	J502	B3/4	R215	G7	R314	B5	RA460	B3/4	U304	E5/6	U463	B4
C25	E2	J503	B5/6	R216	G7	R315	B5	RA461	B4/5	U305	E5/6	U470	B2/3
C26	D4	L240	H6	R220	G1	R320	E5	RA464	B/C4	U306	E5/6	U471	A2/3
C27	C4	L250	G6	R221	G1	R321	D5	RA469	A2	U307	E5/6	U472	B4/5
C28	C3	L260	G2	R222	G1	R322	D5	RA470	A2/3	U308	D5/6	U473	B4/5
C29	B3	L270	H2	R223	G1/2	R323	D5	RA471	A2/3	U309	D5/6	U474	A6/7
C30	C3	L400	E4/5	R224	G1	R324	D5	RA472	A4/5	U310	D5/6	U500	E/F3/4
C31	B1	L410	E4	R225	G1	R325	D5	RA473	A4/5	U311	C5/6	U510	G3/4
C32	B2	L420	E3/4	R226	G1	R326	D5	RA474	A4	U312	C5/6	U520	F3/4
C34	B3	L430	E3	R230	H1	R327	D5	RA475	A6	U313	C5/6	U530	F/G3/4
C35	A7	MP5	E4	R231	H1	R328	C5	RA476	A2/3	U314	B5/6	U540	G3/4
C36	B5	MP6	E4	R232	H1	R329	C5	RA477	A4	U315	B5/6	U542	E4/5
C37	B5	Q200	H6	R233	H1/2	R330	C5	RA478	A4	U320	F2	U550	G3/4
C40	A5	Q201	H6	R234	H1	R331	C5	RA479	A6/7	U321	G2	U551	G/H3/4
C41	A4	Q210	G6	R235	H1	R332	C5	RA500	F/E4	U322	F2	U552	E3
C42	A3	Q211	G6	R236	G1	R333	C5	RA510	F/G4	U323	F2	U560	J1/2
C43	A3	Q220	G1	R240	H6	R334	B5	RA520	E/F3	U324	E2	U561	J1
C44	A5	1221	G1	R241	G5	R335	B5	RA530	F/G3	U325	E2	U562	J2/3
A45	A7	Q230	H1	R242	H5	R400	E4/5	RA540	F4	U326	E2	U563	J2/3
C46	B5	Q231	H1	R243	H5	R401	D4/5	RA550	I1	U327	E2	U570	I1
C47	C5	Q240	H6	R244	H5	R402	E4/5	RA551	I2	U328	D2	U580	I1
C48	D5	Q241	H6	R245	H5	R410	E4	RA552	I1	U329	D2	U590	I2
C49	D5	Q250	G6	R250	G6	R411	D4	RA553	I2	U330	C2	W1	I3/4
C50	E5	Q251	G6	R251	G5	R412	E4	RA1000	I4	U331	D2	W2	I3/4
C51	E5	Q260	G2	R252	G5	R420	E3/4	S500	H1	U332	C2	W3	I3/4
C52	F5	Q261	G2	R253	G5	R421	D3/4	S501	H2	U333	C2		
C53	G5	Q270	H2	R254	G5	R422	E3/4	S502	J1	U334	B2		
C54	F2	Q271	H2	R255	G5	R430	E3	S503	J2	U335	B2		
C55	E2	Q400	D4	R260	G2	R431	D3	TP1	I4	U340	F/C		
C56	E2	Q410	D4	R261	G2	R432	E3	TP2	D3	U341	F5		
C57	D2	Q420	D3/4	R262	G2	R440	D4/5	TP3	D4	U342	E5		
C58	D2	Q430	D3	R263	G2	R441	D4/5	TP5	D4	U343	D/E5		
C59	C2			R264	G2	R442	D4	TP6	C4/5	U344	D5		
				R265	G2								

SERVICE BLOCK 5 (PART OF)
FINE TIMING BOARD (A51)

THEORY OF OPERATION

Introduction

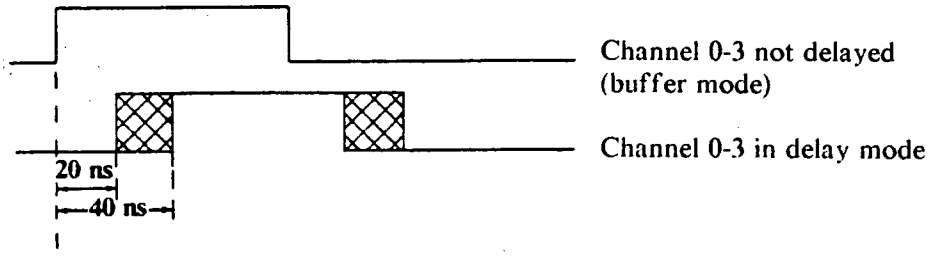
This part service block covers the Fine Timing Board type A51 (instead of A52) which is fitted to some model 8175A's. Note that in any case, it is installed only in those 8175A's which have Option 001 fitted.

The Fine Timing Board is based on the Buffer Board. It performs the same functions and also provides an additional "fine timing" (delay) capability. Its two functional modes are therefore:

- Buffer Mode
- Delay Mode

Buffer Mode
In buffer mode, the board is used either (in Parallel D.G. configuration) to sychronize all 24 data signals for minimum scew or, (in Serial D.G. configuration) to serialize the data for outputting from channels 0 and 2 of POD 0.

Delay Mode
In delay mode, the board performs the above stated "Buffer" functions and also:
enables 4 channels (2 if Serial D.G.) to be delayed (compared to the same channels when non-fine timed) by between 20 and 40 ns (Parallel D.G.) or 0 to 20 ns (Serial D.G.). See the figure below.



Functional Description

The Fine Timing Board comprises the five main sections or blocks listed below. The distribution of these over the schematics is shown in the block diagram Figure 8-5-1. Table 8-5-1 at the end of the theory section, explains all the mnemonics used on the schematics.

Input Circuitry
Delay Circuitry
Output Circuitry
Latch/Tristate Circuitry
Device Bus Interface

INPUT CIRCUITRY (Schematic 51B, 51C)

All incoming differential ECL data-signals from connector J10 are converted into single ended signals by the line receivers U100-U106 and are then fed to the output circuitry.

In addition to this, the ECL data-signals 0-3 are connected to the low-level-triggered Latch U101A-D (schematic 51C). It synchronizes the data-signals 0-3 via the signal LATCH1 for Parallel configuration (see Figure 8-5-2). In Serial configuration, the latches are transparent (HSERIAL=High and LATCH1=constant Low).

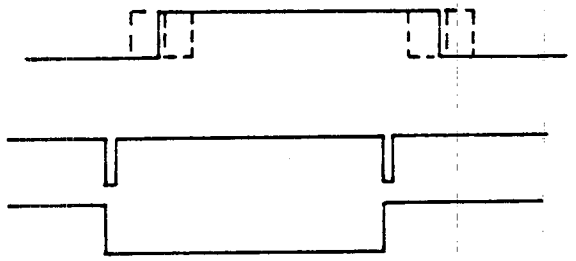


Figure 8-5-2

The data-signals of channels 0 and 1 are fed to the channel switch NOR-Gate U110A-D, which feeds the inverted data-signals to the Latch U121A-D in delay mode (signal SWITCH0 = Low).

Data-signals of channel 2 and 3 are also connected to a channel switch NOR-Gate U120A-D. The inverted signals are controlled by the signal SWITCH1 = Low, and then they are fed to the Latch U121 B/C.

The low-level-triggered data Latch U121 gives a fixed delay to the data-signals 0-3 in delay mode via the signal LATCH1A (see LATCH TRISTATE CIRCUITRY explanation). In relation to the data-signals 0-3 in buffer mode the delay is 20 ns (see Figure 8-5-3).

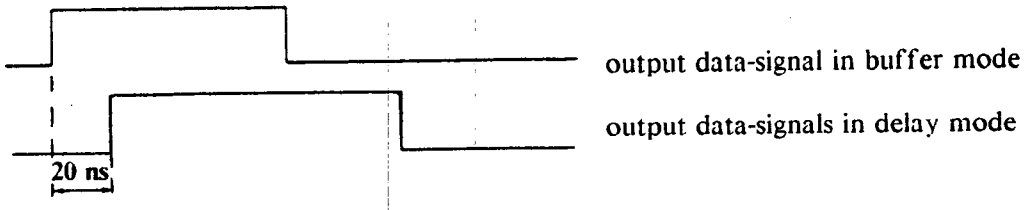


Figure 8-5-3.

From the latches, the data-signals 0-3 go to the strobe generators U111, U112, U122 and U123. In delay mode the signals are fed directly to the following difference-amplifiers (Q200-231, R200-236, C200-231) because the signals LSTROBE 0/1 and LSTROBE 2/3 are high and HINPUTOFF is low.
(The common input HINPUTOFF goes high only if the strobe RS-Flip Flops are set by the microprocessor.)

The difference amplifiers convert the data-signals to special levels (not ECL) to compensate the attenuation across the delay circuitry. The data-signals 0-3 are levelshifted by the temperature compensated current sources (Q240 - 271, R240 - 275, L240 - 270). These are used to compensate the base current of the last four delay line switches in the delay circuit (schematic 52D).

DELAY CIRCUITRY (Schematic 51D)

In delay mode, the data signals CH 0-3 can be delayed from 20 ns up to 40 ns by printed delay lines in 100 ps steps. They are switched in by the delay line switches U300-U335. (5.5 ns are used to compensate the scew between the data-signals 0-3.) The delay line switches (U300-315 and U320-335) route the data-signals through the corresponding delay lines. The switches are enabled by -12 V on pin 6 and pin 7 at open (see Figure 8-5-4).

The following is an operational description of one delay line switch (U300). Refer to Figure 8-5-4.
Q1 and Q4 are switched on and Q2 and 3 are switched off. Q2 and Q3 would be switched on for zero delay by holding pin 6 open and pin 7 at -12 V. They also serve to compensate the delay across Q1 and Q4 in delay configuration. The diodes CR1-CR4 are used to decouple the capacitance of the analog switch from the base of the delay line switch-transistors.

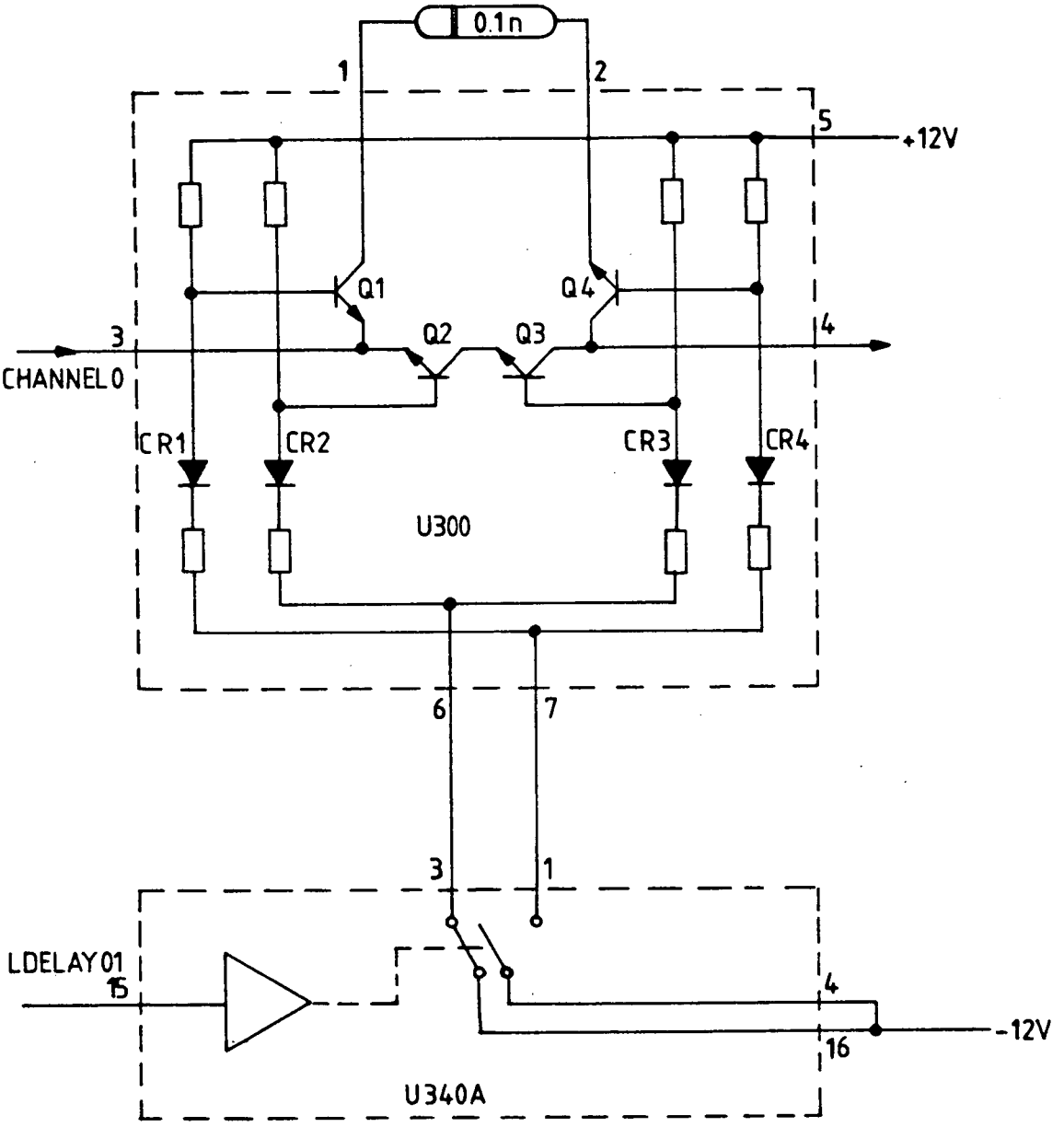


Figure 8-5-4. Delay Line Switch

The analog switches U340-357 (Figure 8-5-4) under the control of the incoming signals LDEL01-LDEL38, control the voltages at pins 6 and 7 of the delay line switches. The voltage regulators U360 and U361 provide special voltages (-12 V, +12 V) for the delay line switches. The resistor dividers R300/301 - 334/335 compensate the base current of the last four delay line switches.
From the delay circuitry, the data signals 0-3 are fed, via the peaker/Buffer section schematic 51E, to the output circuitry.

OUTPUT CIRCUITRY (Schematics 51C, 51B, 51E)

This comprises two sections or blocks:

- Output section channel 0-3
- Output section channel 4-23

Output Section Channel 0-3 (Schematics 51B and 51C)

The data signals Channel 0-3 are fed from the delay circuitry (schematic 51D) to the peaking circuits L400-430, R400-432 (schematic 51C), to improve the signal characteristics. They are then fed to the buffers Q400-430 and U440. From here they pass to the strobe-RS-Flip Flops (U440-441) for channel 0-1 and (U450-451) for channel 2-3. In delay mode the data-signals 0-3 reach the quad-NOR-Gate U460 unchanged.
In delay mode, the data signals CH0-3 are then connected via U460 to the low level triggered output Latch U470 (schematic 51B) because the common input of U460 (LDELAY) will be low. The undelayed data signals CH0-3 (U100/2,3,14,15) will be prevented from passing through the quad-NOR-Gate U461, because its control signal (HDELAY) will be high. The data signals are then converted into differential signals by the Latch U470 (latched when signal LATCH2=Low) and fed to the output pod connector J501.

Note that if delay mode is not used (buffer mode), the delayed data signals CH0-3 cannot pass through U460 (LDELAY=High). In this case, the undelayed data signals will be fed to the output latch U470 via U461 (HDELAY set low).

In Serial D.G. configuration, (HSERIAL=High) the input data passes directly through the output latch because the latch enable signal (LATCH2) U470/20 is set low (latch is in transparent mode). In this mode channel 0 and channel 2 are used for the serial output patterns and channel 1 is the serial clock output (see also theory of the Data Board).

In Parallel D.G. configuration (HSERIAL = LOW therefore LATCH2 is able to follow the incomming latch-signals), the input data is latched to the output of U470 when the latch signal at pin 20 goes high. The differential output signals are now synchronized, and they are fed to the output pod connector J501.

Output Section Channels 4-23 (Schematic 51B)

This section is really of significance only in Parallel D.G. configuration. The input data signals 4-23 are synchronously latched (U471-474) to the output pod connectors J502 and J503 by the latch signals LATCH3 - LATCH5. The operation is the same as described for channels when non-delayed. In Serial configuration, parallel output data is available from channels 4-23 but with an 8 times slower pattern duration.

LATCH TRISTATE CIRCUITRY (Schematic 51A)

The incoming differential ECL latch signals (HLATCH/LLATCH), are converted into a single ended signal by the line receiver U107C. This is then fed to the NOR-Gate U109A, which provides the signal LATCH1, and to the delay lines 0.5 ns and 2.5 ns. Depending on the jumper connected, the signal is then fed to U109B/11-13. This gate provides the signal LATCH1A, which is delayed afterwards by DL1 with special jumpers. (Information about selection of these delay lines is described in the Adjustment Procedure for the Fine Timing Board.

The signals LATCH1 and LATCH1A are at a constant low level for Serial D.G. configuration because the signal HSERIAL is high. In Parallel D.G. configuration, they are able to follow the incoming latch signals since HSERIAL will be low. The incoming differential ECL latch signals (HLATCH/LLATCH) are converted into a single-ended latch-signal by the line receiver U107B, it is then fed to the dual-NOR-Gate U462. U462B splits it into signals LATCH3 - LATCH5 (which are able to follow the incomming latch signals) for the output latches U471 - U474. U462A conditions the latch-signal the different functions of LATCH2 via the control-signals HSERIAL and HDELAY (U462A).

When HSERIAL (U462A/6) is high (n Serial D.G. config.) or HDELAY (U462A/7) goes high in delay mode, LATCH2 is constant low. In buffer mode, HSERIAL is low (parallel mode), signal LATCH2 is able to follow the incoming latch signals.

The tristate signals are also conditioned in this section. The incoming differential ECL tristate signal is buffered by the line receiver U107A, split by the quad-NOR-Gate U463 and then fed to the output pod connectors J501 to J503.

DEVICE BUS INTERFACE (Schematic 51A, 51D)

This section's main function is to interface the board with the MPU and to provide all control signals for the board. The section comprises three main blocks:

Interface section
Register section
Scew adjust section

INTERFACE SECTION (Schematic 51A)

This section includes the Octal bus transceiver U560, the OR-Gate U561, the diodes CR500, CR501 and CR502, and the decoders U562 and U563. U563 is activated by the signals LCEN and LMHS as they go low. When HCL1 goes high and HCL2 goes low, the diodes CR500, CR501 and CR502, are pulled to low so producing the Fine Timing Board identifying code number (for the CPU) of decimal 51.

When HCL1 and HCL2 go low, U560 is enabled. U560 is in read mode when LRHW goes low, Data D0-D7 will be transmitted to the HDD0-7 data bus.
In the write mode (LRHW=High), all incoming TTL data (HDD0-HDD7) is fed to the latch register U500 to 540.

The address decoder U562 is enabled when HDA5 goes high plus LDBV low (low-device bus valid, see theory of MPU) and when the inputs HDA3 and HDA4 of U563 go low. U562 provides the latch signal for the latch register U540 when U562 is enabled and signals HDA2 and HDA1 are high and HDA0 low.

REGISTER SECTION (Schematic 51A, 51D)

The input data D0 - D7 from U560 is written into the registers U500 to U540 when the latch-signals LCONTROL 0-3 (generated by U562/7,11,12,13) goes low and latched to the outputs when the latch-signal goes high afterwards. The TTL-signals from U540 are converted into the required ECL signals by the TTL-ECL Translator U542.

SCEW ADJUST SECTION (Schematic 51A)

This section provides the information to enable the microprocessor to compensate for the scew between data channels 0-3 in delay mode (see Adjustment procedure of the Fine Timing Board). This information is buffered by the switches S500-503 and multiplexed to the data bus by the multiplexers U570-590 and the write readtransmitter U560 in the following way:

HDA1	HDA0	LRHW	LDBV	
0	0	0	0	read scew info channel 0
0	1	0	0	read scew info channel 1
1	0	0	0	read scew info channel 2
1	1	0	0	read scew info channel 3

NOTE:
The processor samples the settings of S500 - S503 during turn-on, and whenever (via NEXT/PREV keys) Fine Timing is changed from off to on (**[Fine Timing off]** to **[Fine Timing on]** etc.)

Table 8-5-1. F.T. Bd. A51 Mnemonics Explanation

The first letter in a mnemonic means:

H : high active
L : low active
P : the rising edge of a signal is active
N : the falling edge of a signal is active

Mnemonic	Explanation
D0 - D7	TTL-Databus 0-7 on the board.
CONTROL0 - CONTROL3	These signals write the delay-information in U500 - U530.
HCL1, HCL2	High Control Line 1, 2.
HDA0 - HDA5	Address-lines of the device bus.
HDD0-7	High Device Data 0-7
HDELAY	Enables the delay-mode of the Fine Timing-Board.
HINPUTOFF	Turns OFF the Delay signal at the Strobe-Generator in the Buffer-Mode.
HSERIAL	This signal indicates the Serial-Mode.
HSTROBE0/1, HSTROBE2/3	These signals low enable the Delay-Mode of the Fine Timing Board.
LATCH1, LATCH1A	Latch signals for the input latches U100 and U121. In Serial-Mode LATCH1 and LATCH1A are low. The input latches U100 and U121 are transparent.
LATCH2 - LATCH5	Latch signals for the output-latches U470-U474. In Serial and Delay Mode LATCH2 is low. The output latch U470 is transparent.
LCEN	Low Card Enable.

LDBV	Low Device Bus Valid.
LDEL1 - LDEL38	Data for the Analog-Switches U300 - U357. It's the delay information.
LDELAY	This signal low enables the Delay-Mode of the Fine Timing Board.
LSTROBE0/1, LSTROBE2/3	These signals high enable the delay mode of the Finetiming Board.
LMHS	Low Master/High Slave.
LRHW	Low Read/High Write.
SWITCH0, SWITCH1	SWITCH0 is low in delay-mode. Channel 0 and 1 are enabled. SWITCH1 does the same with channel 2 and 3.

TROUBLESHOOTING (FINE TIMING BOARD A51)

General

Should a fault be isolated to the Fine Timing Board type A51, the theory of operation should be read and understood before proceeding with troubleshooting in this area.

CAUTION

Instrument must not be operated without cover over power supply and fan areas.

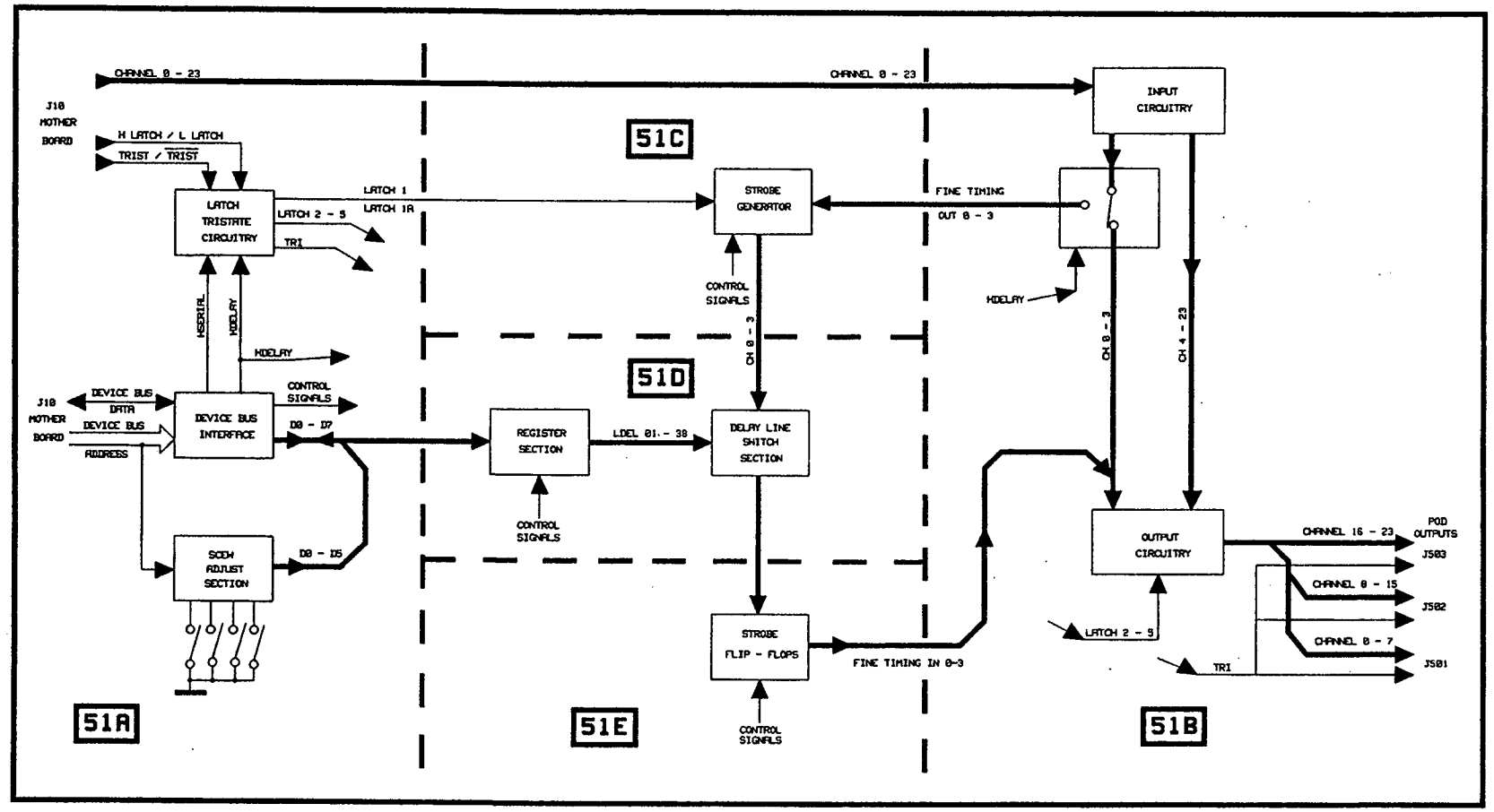
Procedure:

With power OFF, plug the Fine Timing Board into the 8175A test connectors.
Switch instrument ON, and Recall Standard Settings.

a) First check that the Power Supply Voltages at the following test points are correct:

TP +15V	+15V	± 50 mV
TP +12V	+12V	± 50 mV
TP +5V	+5V	± 50 mV
TP -5V	-5.2V	± 50 mV
TP -12V	-12V	± 50 mV
TP -15V	-15V	± 50 mV

BLOCK DIAGRAM FINE TIMING BOARD 8175A



b) For the test conditions shown in the table (configuration Par./Ser. and Fine Timing OFF or ON), confirm that the following ECL signal conditions are produced.

		SYSTEM Page		TIMING Page	
ECL Signal	U/pin	Parallel Mode	Serial Mode	Fine Timing OFF	Fine Timing ON
HDELAY	542/15			L	H
LDELAY	460/9			H	L
LATCH1	109/3	H able to follow HLATCH/ LLATCH	L		
LATCH1A	121/6	-"-	L		
LATCH2	462A/4	-"-	L	H able to follow HLATCH/ LLATCH	L
LATCH3,4,5	462B/12, 13,14	-"-	H able to follow HLATCH/ LLATCH	-"-	H able to follow HLATCH/ LLATCH
HSTROBE0/1	551/4	L	L	L	L
HSTROBE2/3	551/13	L	L	L	L
LSTROBE0/1	551/4	H	H	H	H
LSTROBE2/3	551/14	H	H	H	H
SWITCH0	542/14	L	L	L	L
SWITCH1	552/1	L	L	L	L

c) Set 8175A:

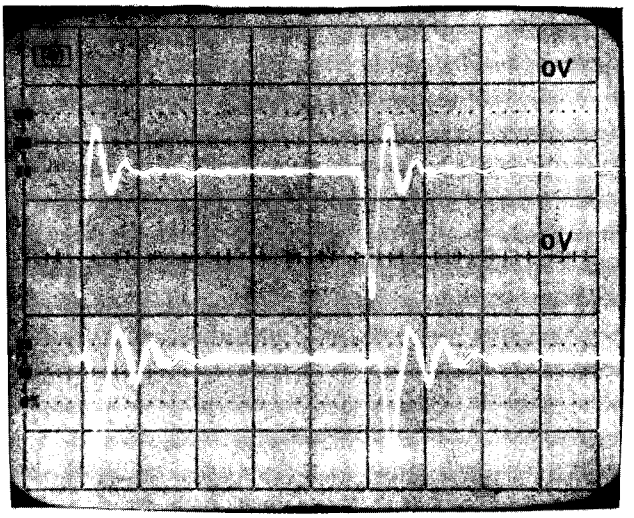
CNTRL > CURSOR↓ > NEXT = [Auto Cycle] >
DATA > CURSOR↓ = Period > 0.1 > DATA > NEXT > CURSOR↓ = Address 0000 > ROLL↑ =
Address 0001 > CURSOR→ = POD2 CH7 > 1 24x >
PRGM > CURSOR↓ = PROG1 > CURSOR→ = 1023 > 0001 >
OUTPUT > NEXT = enabled >
blue > EXEC = UPDATE > START

TIMING > NEXT = [Fine Timing on]

Set scope to: 0.02us/Div and 0.05 V/Div.

Then measure with Scope Probe 10017A, that signals at following components (refer to the photos) are correct:

0.05V/Div



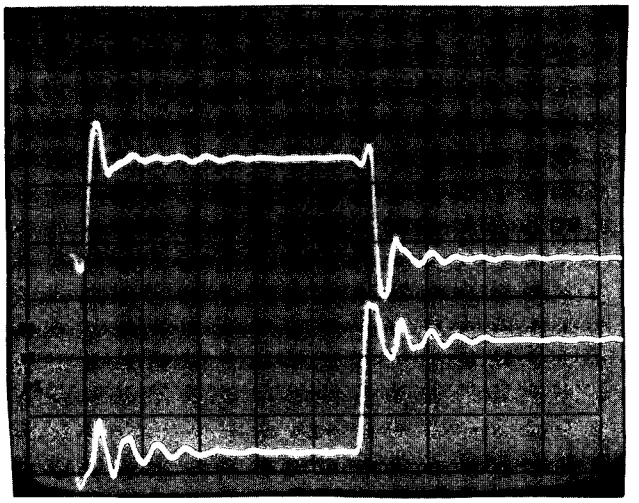
LATCH1

U101/6

LATCH1A

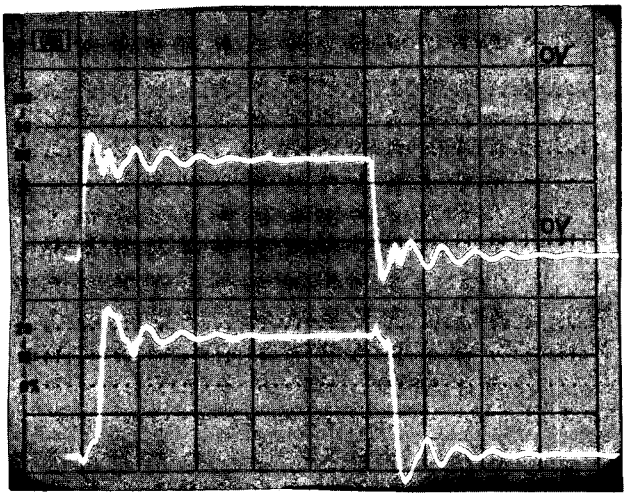
U121/6

The delay depends on connection of W1/W2 or W3 and of DL1



CH0
U101/10

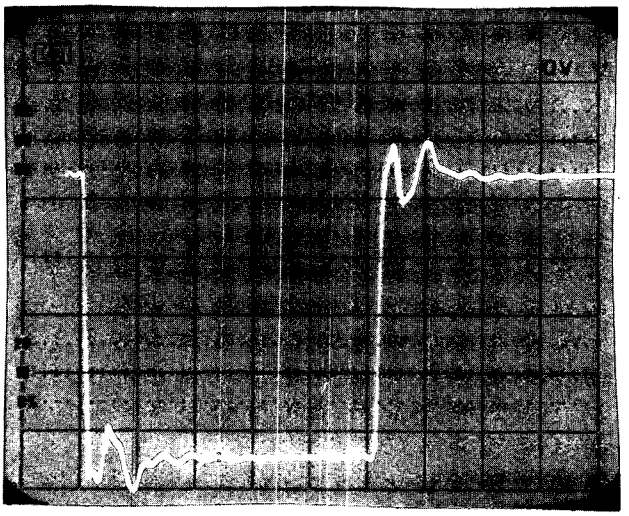
Q Output
U101/14



D Input
U121/10

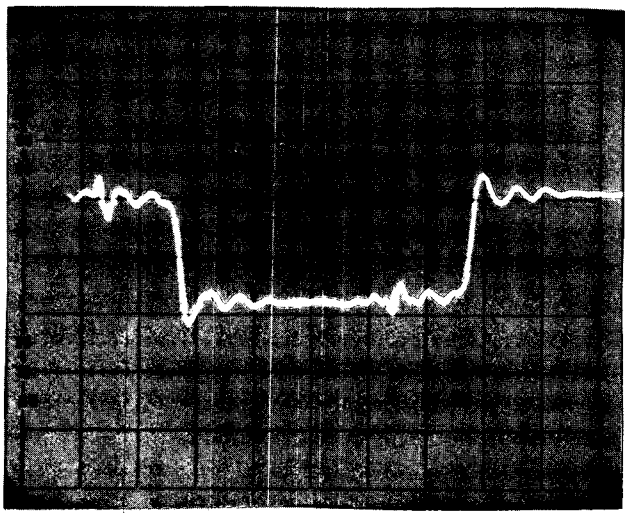
Q Output
U121/14

Q 201 Coll.



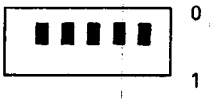
With delay set to 40 ns,
measure the signal at TP5

TP5.



Do the same check at the corresponding pins of channels 1, 2 and 3 related components.

Set the switch elements of S500 to the position shown (all to zero - 0). Press NEXT 2 times (to read in the new S500 settings).



Set 8175A: Timing Page (PAR)
[Fine Timing on]
CURSOR↓ = Channel 0 20.0 ns delay.
For each delay value shown in the following table, measure with a DVM the TTL levels at the IC pins indicated. (Do not change the S500 setting!)

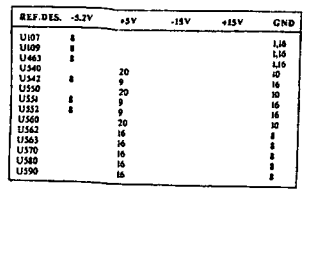
Delay	LDEL / U500	01 2	02 5	03 6	04 9	05 19	06 16	07 15	08 12	S500 setting
20.0	U300/6 -12V	1	1	1	1	1	1	1	1	
20.1	U302/6 -12V	0	1	1	1	1	1	1	1	----000001
20.2		1	0	1	1	1	1	1	1	----000010
20.3		0	0	1	1	1	1	1	1	
20.4	U304/6 -12V	1	1	0	1	1	1	1	1	---000100
20.5		0	1	0	1	1	1	1	1	
20.6		1	0	0	1	1	1	1	1	
20.7		0	0	0	1	1	1	1	1	
20.8	U306/6 -12V	1	1	1	0	1	1	1	1	---001000
20.9		0	1	1	0	1	1	1	1	
21.0		1	0	1	0	1	1	1	1	
21.1		0	0	1	0	1	1	1	1	
21.2		1	1	0	0	1	1	1	1	
21.3		0	1	0	0	1	1	1	1	
21.4		1	0	0	0	1	1	1	1	
21.5		0	0	0	0	1	1	1	1	
21.6	U314/6 -12V	1	1	1	1	0	1	1	1	---010000
23.2	U312/6 -12V	1	1	1	1	1	0	1	1	---100000
26.4	U310/6 -12V	1	1	1	1	1	1	0	1	
32.8	U310/6 -12V	1	1	1	1	1	1	1	0	
49.0	U308/6 -12V	1	1	1	0	1	1	0	0	

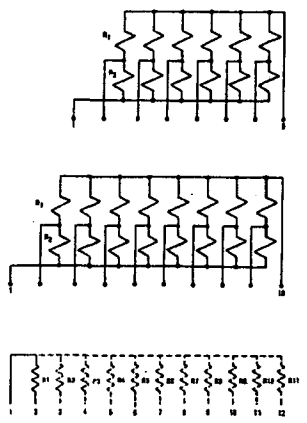
Set delay back to 20.0 ns then, for each of the S500 settings shown in the table above, check the corresponding TTL levels.
Note:
After making each new S500 setting, press NEXT 2 times (to read in the new settings).

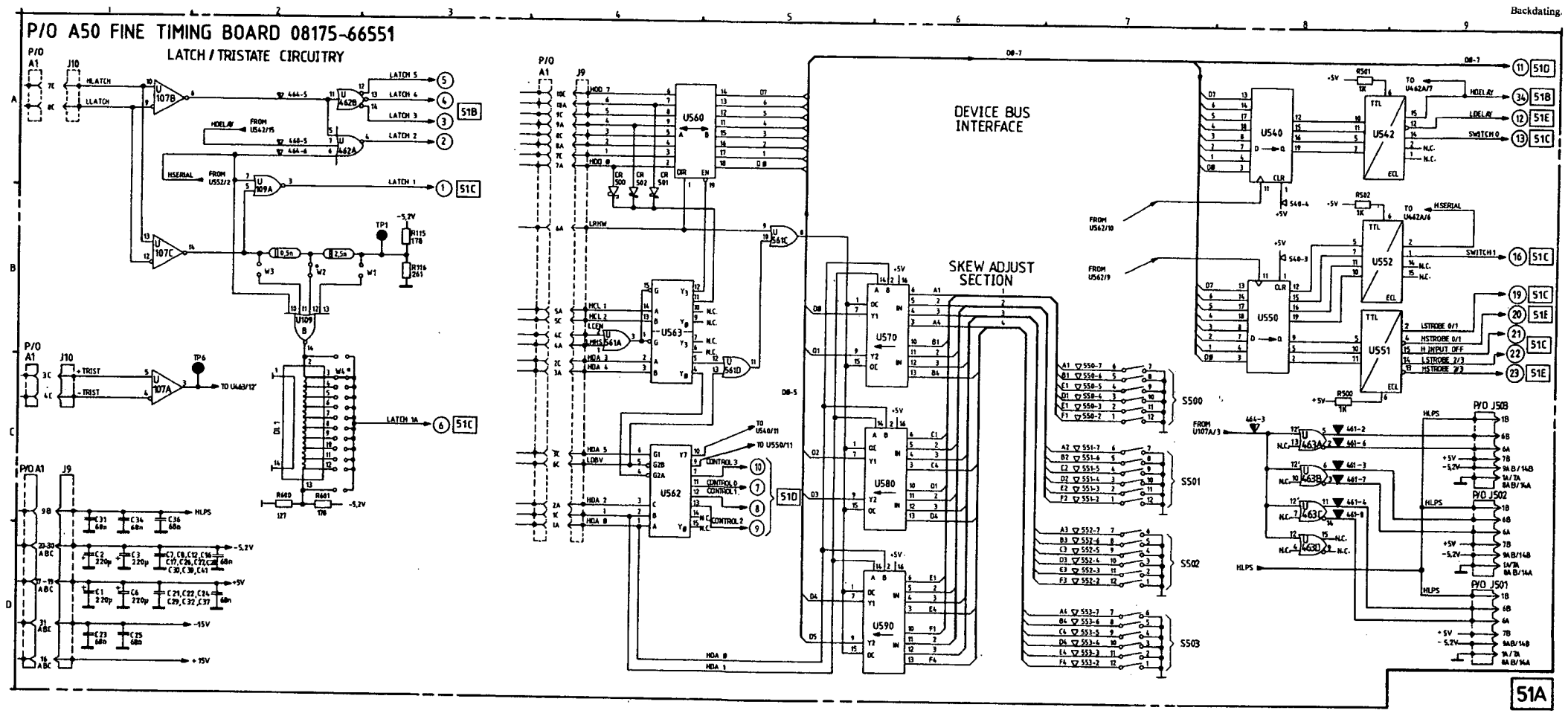
Do the same test (at appropriate pins of IC's U510, 520 and 530 etc.) for channels 1, 2, and 3. Change switch settings of S501, 502, and 503 respectively.

REF.DES.	-5.2V	+5V	-15V	+15V	GND
U107	8				16
U109	8				16
U463	8				16
U540		20			10
U542	8	9			16
U550		20			10
U551	8	9			16
U552		20			10
U562		16			8
U563		16			8
U570		16			8
U580		16			8
U590		16			8

RA	POWER PIN	VOLTAGE LEVEL	RESISTOR VALUE
460	1	-5.2V	8 PIN 150/240
461	1	-5.2V	7x470
464	1	-5.2V	8 PIN 150/240
550	1	+5V	7x10K
551	1	+5V	7x10K
552	1	+5V	7x10K
553	1	+5V	7x10K



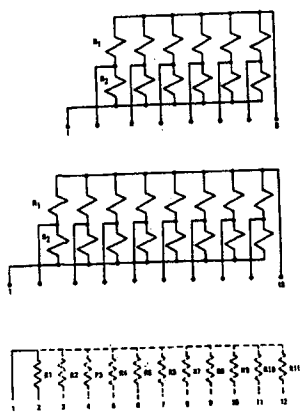




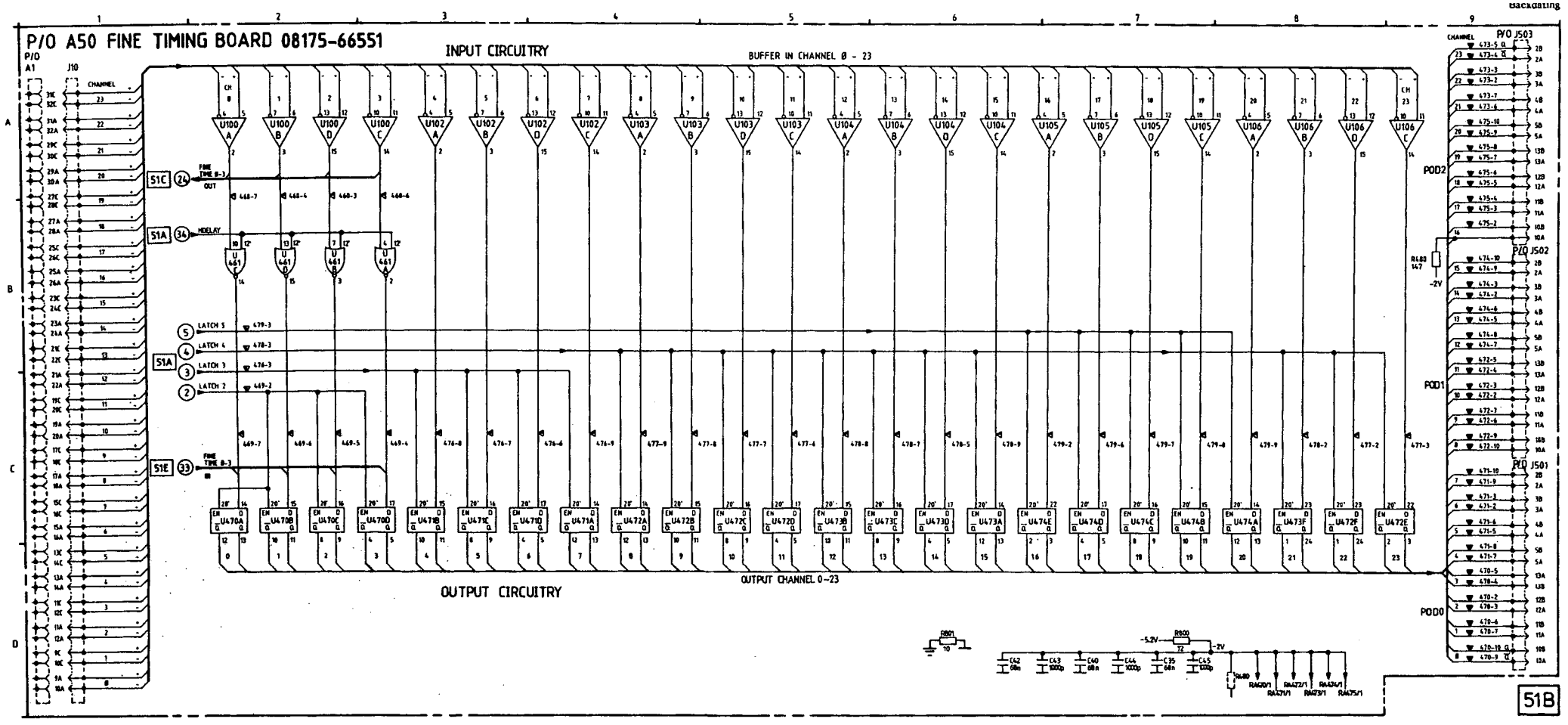
REF.DES.	-5.2V	+5V	-15V	+15V	GND
U100	8				16
U101	8				16
U103	8				16
U104	8				16
U105	8				16
U106	8				16
U468	8				16
U470	18				6,7
U471	18				6,7
U472	18				6,7
U473	18				6,7
U474	18				6,7

RA	POWER PIN	VOLTAGE LEVEL	RESISTOR VALUE
468	1	-5.2V	8 PIN 160/240
469	1	-5.2V	10 PIN 160/240
470	1	-5.2V	9x150
471	1	-5.2V	9x150
472	1	-5.2V	7x150
473	1	-5.2V	8x150
474	1	-5.2V	9x150
475	1	-5.2V	8 PIN 160/240
476	1	-5.2V	8 PIN 160/240
477	1	-5.2V	8 PIN 160/240
478	1	-5.2V	8 PIN 160/240
479	1	-5.2V	8 PIN 160/240

NOTE
*.0 SEE P.A VALUE TABLE FOR MORE INFORMATION
PIN NUMBER OF RESISTOR PACK
RESISTOR PACK NUMBER (R#)
ECL LINE BEING PULLED DOWN



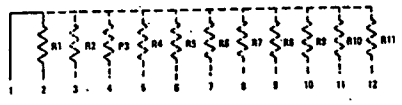
backplating

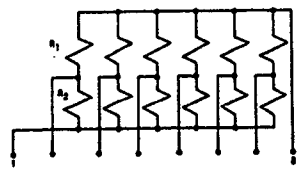


REF.DES.	-5.2V	+5V	-15V	+15V	GND
U101	8				1,16
U110	8				1,16
U111	8				1,16
U112	8				1,16
U120	8				1,16
U121	8				1,16
U122	8				1,16
U123	8				1,16

RA	POWER PIN	VOLTAGE LEVEL	RESISTOR VALUE
101	1	-5.2V	9x470
102	1	-5.2V	7x470
111	1	-5.2V	7x470
112	1	-5.2V	7x470
1000	1	-5.2V	7x470

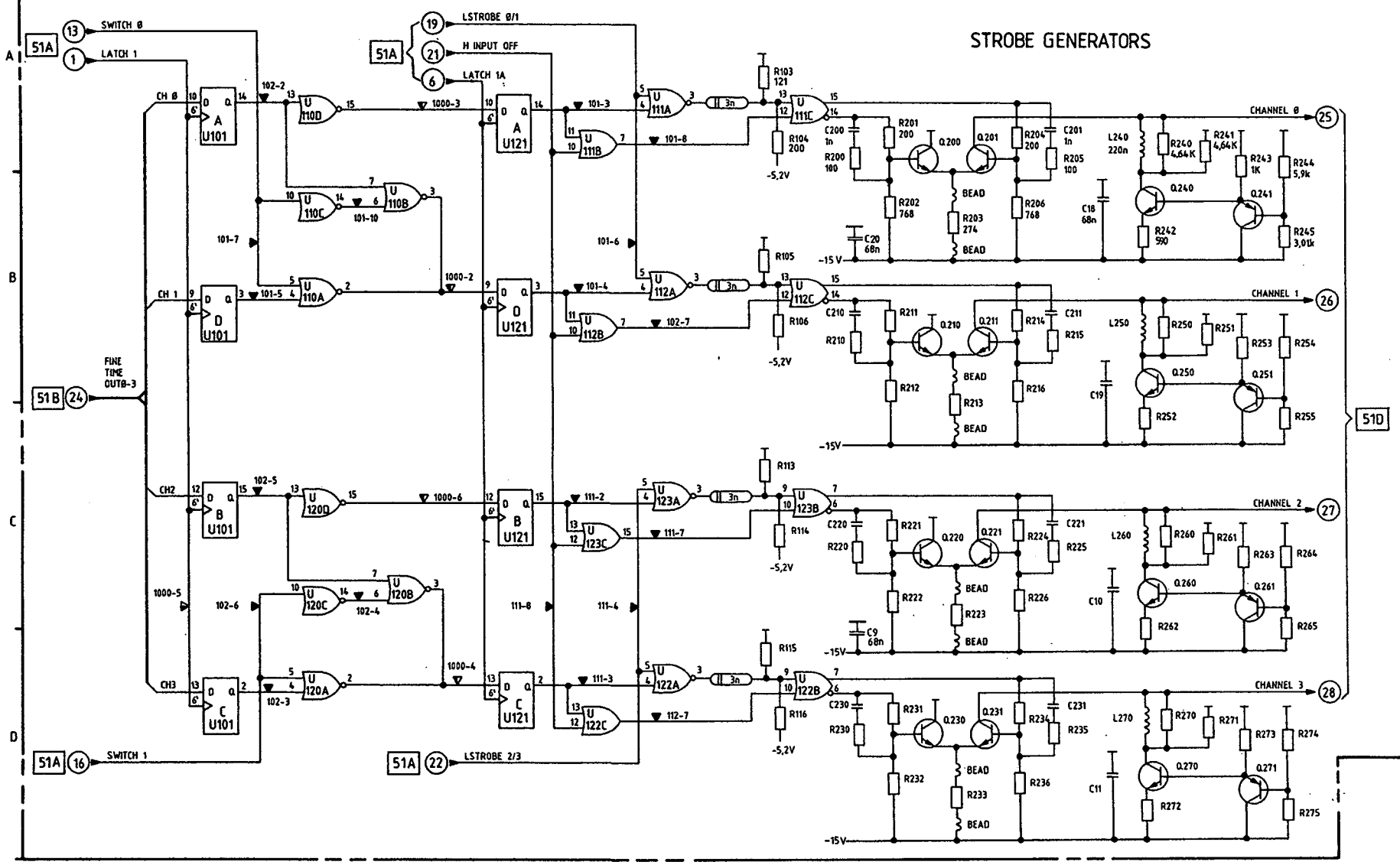
NOTE
e.g. ▼ XX - XX
- SEE RA VALUE TABLE FOR MORE INFORMATION
- PIN NUMBER OF RESISTOR PACK
- RESISTOR PACK NUMBER (RA)
- ECL LINE BEING PULLED DOWN





P/O A50 FINE TIMING BOARD 08175-66551

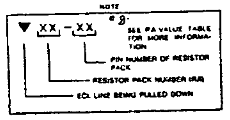
STROBE GENERATORS

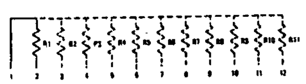


REF.DES.	-5.2V	+5V	-15V	+15V	GND
U300				5	
U301				5	
U302				5	
U303				5	
U304				5	
U305				5	
U306				5	
U307				5	
U308				5	
U309				5	
U310				5	
U311				5	
U312				5	
U313				5	
U314				5	
U315				5	
U320				5	
U321				5	
U322				5	
U323				5	
U324				5	
U325				5	
U326				5	
U327				5	
U328				5	
U329				5	
U330				5	
U331				5	
U332				5	
U333				5	
U334				5	
U335				5	
U340	4,5,9,16	12	14	11	13
U341	4,5,9,16	12	14	11	13
U342	4,5,9,16	12	14	11	13
U343	4,5,9,16	12	14	11	13
U344	4,5,9,16	12	14	11	13
U345	4,5,9,16	12	14	11	13
U346	4,5,9,16	12	14	11	13
U347	4,5,9,16	12	14	11	13
U350	4,5,9,16	12	14	11	13
U351	4,5,9,16	12	14	11	13
U352	4,5,9,16	12	14	11	13
U353	4,5,9,16	12	14	11	13
U354	4,5,9,16	12	14	11	13
U355	4,5,9,16	12	14	11	13
U356	4,5,9,16	12	14	11	13
U357	4,5,9,16	12	14	11	13
U500		20			10
U510		20			10
U520		20			10
U530		20			10

RA	POWER PIN	VOLTAGE LEVEL	RESISTOR VALUE
500	1	-5.2V	9x10K
510	1	-5.2V	9x10K
520	1	-5.2V	9x10K
530	1	-5.2V	9x10K
540	1	-5.2V	7x10K

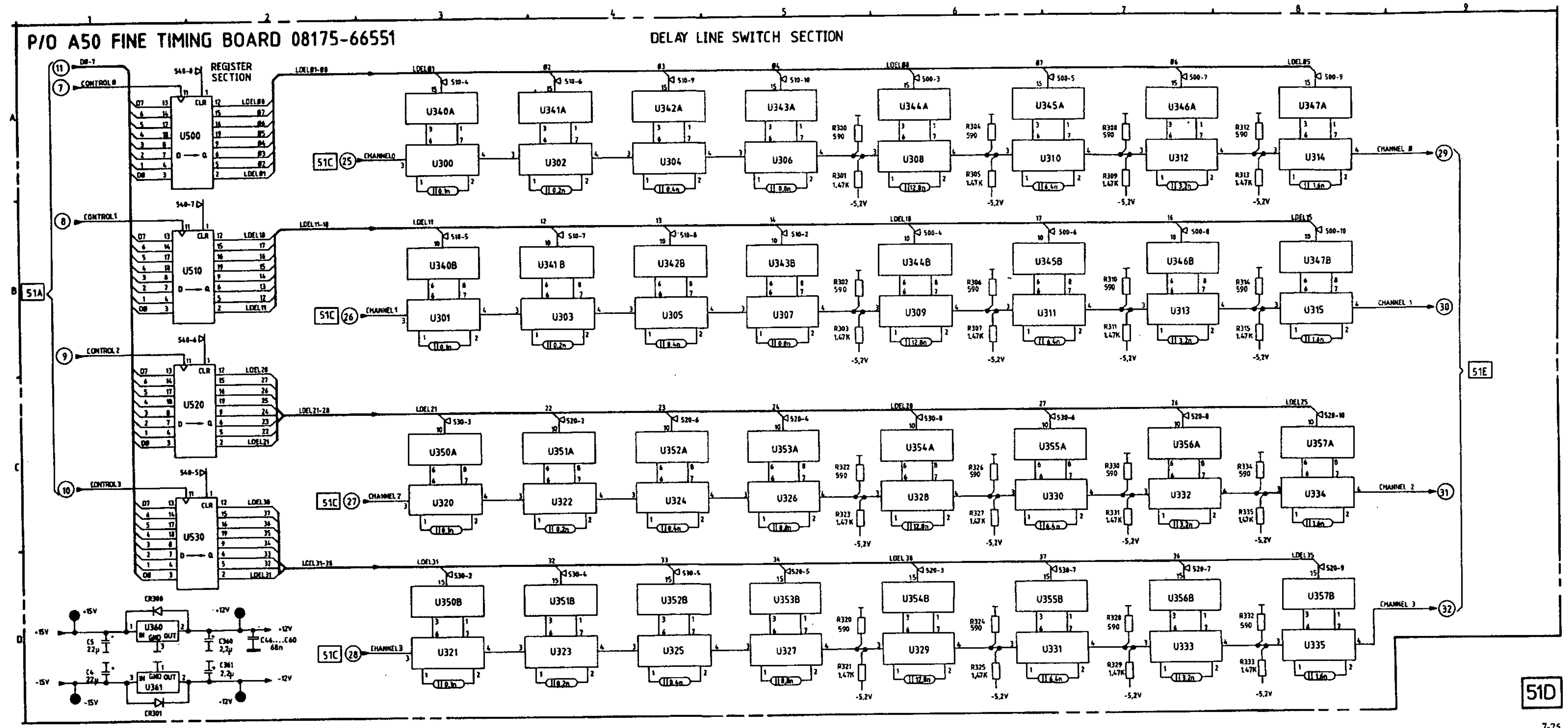
NOTE





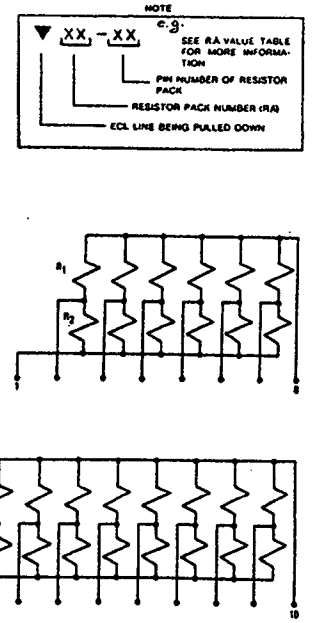
P/O A50 FINE TIMING BOARD 08175-66551

DELAY LINE SWITCH SECTION



REF.DES.	-5.2V	+5V	-15V	+15V	GND
U440	8				1,16
U441	8				1,16
U450	8				1,16
U451	8				1,16
U460	8				1,16

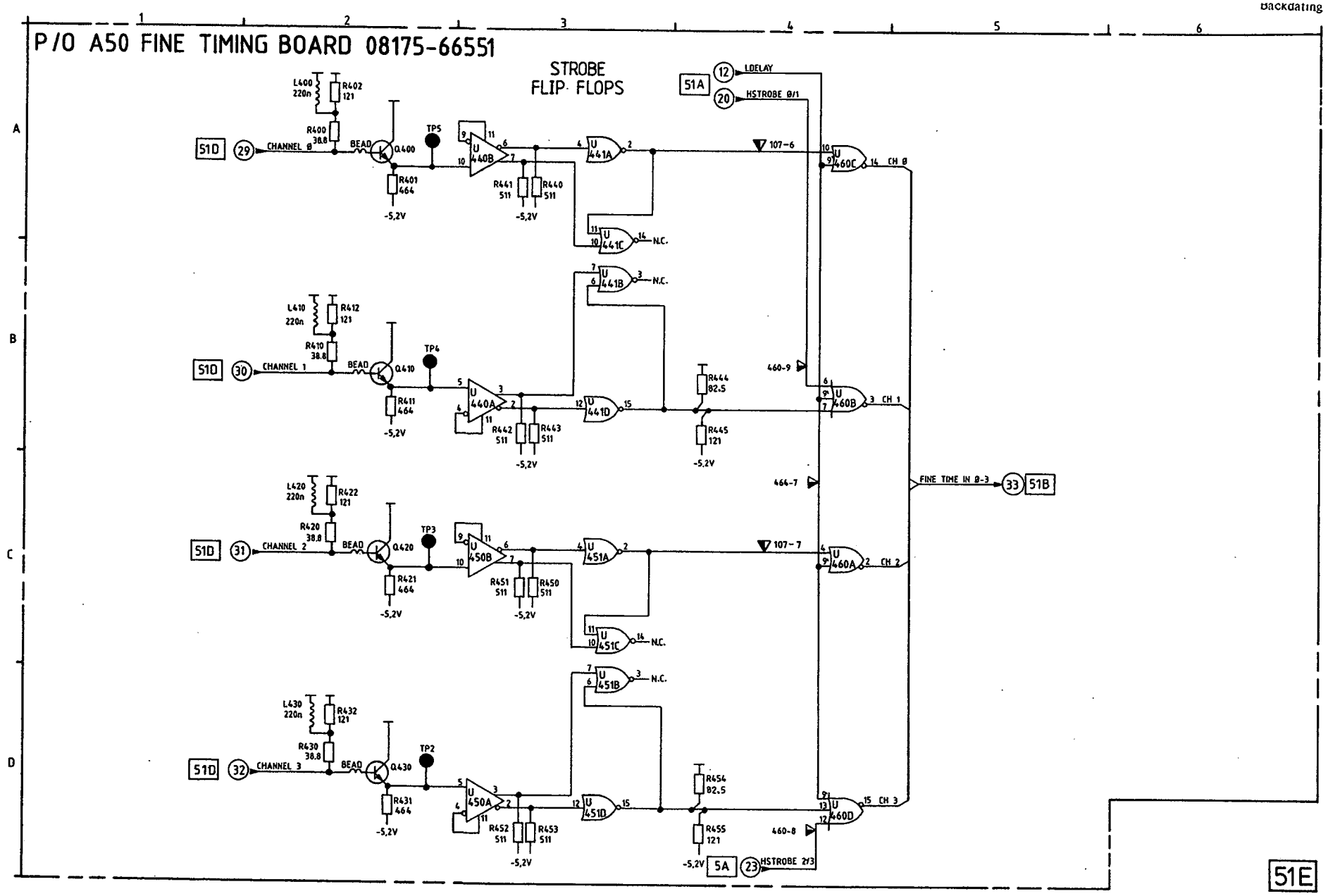
RA	POWER PIN	VOLTAGE LEVEL	RESISTOR VALUE
107	1	-5.2V	8 PIN 160/240
460	1	-5.2V	10 PIN 160/240
464	1	-5.2V	8 PIN 160/240



backdating

P/O A50 FINE TIMING BOARD 08175-66551

STROBE FLIP-FLOPS



51E

REFERENCE DESIGNATOR		C D	H-P PART NUMBER	DESCRIPTION
A51	08175-66551			BD AY-FINE TMG
A51	C1	6	0180-2208	C-F 220UF10% 10V
A51	C2	6	0180-2208	C-F 220UF10% 10V
A51	C3	6	0180-2208	C-F 220UF10% 10V
A51	C4	3	0180-1794	C-F 22UF 35V
A51	C5	3	0180-1794	C-F 22UF 35V
A51	C6	6	0180-2208	C-F 220UF10% 10V
A51	C7	8	0160-6080	C-F .068UF 50VDC
A51	C8	8	0160-6080	C-F .068UF 50VDC
A51	C9	8	0160-6080	C-F .068UF 50VDC
A51	C10	8	0160-6080	C-F .068UF 50VDC
A51	C11	8	0160-6080	C-F .068UF 50VDC
A51	C12	8	0160-6080	C-F .068UF 50VDC
A51	C16	8	0160-6080	C-F .068UF 50VDC
A51	C17	8	0160-6080	C-F .068UF 50VDC
A51	C18	8	0160-6080	C-F .068UF 50VDC
A51	C19	8	0160-6080	C-F .068UF 50VDC
A51	C20	8	0160-6080	C-F .068UF 50VDC
A51	C21	8	0160-6080	C-F .068UF 50VDC
A51	C22	8	0160-6080	C-F .068UF 50VDC
A51	C23	8	0160-6080	C-F .068UF 50VDC
A51	C24	8	0160-6080	C-F .068UF 50VDC
A51	C25	8	0160-6080	C-F .068UF 50VDC
A51	C26	8	0160-6080	C-F .068UF 50VDC
A51	C27	8	0160-6080	C-F .068UF 50VDC
A51	C28	8	0160-6080	C-F .068UF 50VDC
A51	C29	8	0160-6080	C-F .068UF 50VDC
A51	C30	8	0160-6080	C-F .068UF 50VDC
A51	C31	8	0160-6080	C-F .068UF 50VDC
A51	C32	8	0160-6080	C-F .068UF 50VDC
A51	C34	8	0160-6080	C-F .068UF 50VDC
A51	C35	8	0160-6080	C-F .068UF 50VDC
A51	C36	8	0160-6080	C-F .068UF 50VDC
A51	C37	8	0160-6080	C-F .068UF 50VDC
A51	C39	8	0160-6080	C-F .068UF 50VDC
A51	C40	8	0160-6080	C-F .068UF 50VDC
A51	C41	8	0160-6080	C-F .068UF 50VDC
A51	C42	8	0160-6080	C-F .068UF 50VDC
A51	C43	6	0160-3456	C-F 1000PF 1000V
A51	C44	6	0160-3456	C-F 1000PF 1000V
A51	C45	6	0160-3456	C-F 1000PF 1000V
A51	C46	8	0160-6080	C-F .068UF 50VDC
A51	C47	8	0160-6080	C-F .068UF 50VDC
A51	C48	8	0160-6080	C-F .068UF 50VDC
A51	C49	8	0160-6080	C-F .068UF 50VDC
A51	C50	8	0160-6080	C-F .068UF 50VDC
A51	C51	8	0160-6080	C-F .068UF 50VDC
A51	C52	8	0160-6080	C-F .068UF 50VDC
A51	C53	8	0160-6080	C-F .068UF 50VDC
A51	C54	8	0160-6080	C-F .068UF 50VDC
A51	C55	8	0160-6080	C-F .068UF 50VDC
A51	C56	8	0160-6080	C-F .068UF 50VDC
A51	C57	8	0160-6080	C-F .068UF 50VDC
A51	C58	8	0160-6080	C-F .068UF 50VDC
A51	C59	8	0160-6080	C-F .068UF 50VDC
A51	C60	8	0160-6080	C-F .068UF 50VDC
A51	C200	9	0160-5728	C-F 1000PF 5%
A51	C201	9	0160-5728	C-F 1000PF 5%
A51	C210	9	0160-5728	C-F 1000PF 5%
A51	C211	9	0160-5728	C-F 1000PF 5%
A51	C220	9	0160-5728	C-F 1000PF 5%
A51	C221	9	0160-5728	C-F 1000PF 5%

REFERENCE DESIGNATOR		C D	H-P PART NUMBER	DESCRIPTION
A51	C230	9	0160-5728	C-F 1000PF 5%
A51	C231	9	0160-5728	C-F 1000PF 5%
A51	C360	8	0180-0197	C-F 2.2UF 20V
A51	C361	8	0180-0197	C-F 2.2UF 20V
A51	CR300	6	1901-0376	DIO LOW LEAKAGE
A51	CR301	6	1901-0376	DIO LOW LEAKAGE
A51	CR500	9	1901-0535	DIO SCHOT HP2311
A51	CR501	9	1901-0535	DIO SCHOT HP2311
A51	CR502	9	1901-0535	DIO SCHOT HP2311
A51	DL1	4	1810-0616	DELAY LINE 14PIN
A51	J9	2	1251-7799	3X32 PLUG
A51	J10	2	1251-7799	3X32 PLUG
A51	J501	0	1251-7705	CONN-POST 28CONT
A51	J502	0	1251-7705	CONN-POST 28CONT
A51	J503	0	1251-7705	CONN-POST 28CONT
A51	L240	1	9140-0129	IDCTR 220UN 5%
A51	L250	1	9140-0129	IDCTR 220UN 5%
A51	L260	1	9140-0129	IDCTR 220UN 5%
A51	L270	1	9140-0129	IDCTR 220UN 5%
A51	L400	0	9100-2251	COIL-CHOKE .22UH
A51	L410	0	9100-2251	COIL-CHOKE .22UH
A51	L420	0	9100-2251	COIL-CHOKE .22UH
A51	L430	0	9100-2251	COIL-CHOKE .22UH
A51	L440	0	9170-0894	CORE MAGNETIC
A51	L441	0	9170-0894	CORE MAGNETIC
A51	L450	0	9170-0894	CORE MAGNETIC
A51	L451	0	9170-0894	CORE MAGNETIC
A51	MP4	6	1205-0033	HT-SINK TO-5
A51	MP5	7	08175-21704	BUSHING SHORT
A51	MP6	3	08175-26106	PC PIN
A51	Q200	3	1854-0720	XSTR SI NPN HF
A51	Q201	3	1854-0720	XSTR SI NPN HF
A51	Q210	3	1854-0720	XSTR SI NPN HF
A51	Q211	3	1854-0720	XSTR SI NPN HF
A51	Q220	3	1854-0720	XSTR SI NPN HF
A51	Q221	3	1854-0720	XSTR SI NPN HF
A51	Q230	3	1854-0720	XSTR SI NPN HF
A51	Q231	3	1854-0720	XSTR SI NPN HF
A51	Q240	5	1854-0392	XSTR 2N 5088
A51	Q241	2	1853-0086	XSTR 2N5087
A51	Q250	5	1854-0392	XSTR 2N 5088
A51	Q251	2	1853-0086	XSTR 2N5087
A51	Q260	5	1854-0392	XSTR 2N 5088
A51	Q261	2	1853-0086	XSTR 2N5087
A51	Q270	5	1854-0392	XSTR 2N 5088
A51	Q271	2	1853-0086	XSTR 2N5087
A51	Q400	9	1854-0809	TRANS.2N 2369A
A51	Q410	9	1854-0809	TRANS.2N 2369A
A51	Q420	9	1854-0809	TRANS.2N 2369A
A51	Q430	9	1854-0809	TRANS.2N 2369A
A51	R103	2	0757-0403	R-F 121 1% .125W
A51	R104	6	0757-0407	R-F 200 1% .125W
A51	R105	2	0757-0403	R-F 121 1% .125W
A51	R106	6	0757-0407	R-F 200 1% .125W
A51	R113	2	0757-0403	R-F 121 1% .125W
A51	R114	6	0757-0407	R-F 200 1% .125W
A51	R115	2	0757-0403	R-F 121 1% .125W
A51	R116	6	0757-0407	R-F 200 1% .125W
A51	R200	0	0757-0401	R-F 100 1% .125W
A51	R201	6	0757-0407	R-F 200 1% .125W
A51	R202	5	0698-4462	R-F 768 1% .125
A51	R203	7	0757-0721	R-F 274 1% .25W
A51	R204	6	0757-0407	R-F 200 1% .125W
A51	R205	0	0757-0401	R-F 100 1% .125W

REFERENCE DESIGNATOR	CD	H-P PART NUMBER	DESCRIPTION
A51 R206	5	0698-4462	R-F 768 1% .125
A51 R210	0	0757-0401	R-F 100 1% .125W
A51 R211	6	0757-0407	R-F 200 1% .125W
A51 R212	5	0698-4462	R-F 768 1% .125
A51 R213	7	0757-0721	R-F 274 1% .25W
A51 R214	6	0757-0407	R-F 200 1% .125W
A51 R215	0	0757-0401	R-F 100 1% .125W
A51 R216	5	0698-4462	R-F 768 1% .125
A51 R220	0	0757-0401	R-F 100 1% .125W
A51 R221	6	0757-0407	R-F 200 1% .125W
A51 R222	5	0698-4462	R-F 768 1% .125
A51 R223	7	0757-0721	R-F 274 1% .25W
A51 R224	6	0757-0407	R-F 200 1% .125W
A51 R225	0	0757-0401	R-F 100 1% .125W
A51 R226	5	0698-4462	R-F 768 1% .125
A51 R230	0	0757-0401	R-F 100 1% .125W
A51 R231	6	0757-0407	R-F 200 1% .125W
A51 R232	5	0698-4462	R-F 768 1% .125
A51 R233	7	0757-0721	R-F 274 1% .25W
A51 R234	6	0757-0407	R-F 200 1% .125W
A51 R235	0	0757-0401	R-F 100 1% .125W
A51 R236	5	0698-4462	R-F 768 1% .125
A51 R240	1	0698-3155	R-F 4.64K 1%.125
A51 R241	1	0698-3155	R-F 4.64K 1%.125
A51 R242	9	0698-4458	R-F 590 1% .125W
A51 R243	3	0757-0280	R-F 1K 1% .125W
A51 R244	4	0757-0273	R-F 3.01K1%
A51 R245	1	0698-3155	R-F 4.64K 1%.125
A51 R250	1	0698-3155	R-F 4.64K 1%.125
A51 R251	1	0698-3155	R-F 4.64K 1%.125
A51 R252	9	0698-4458	R-F 590 1% .125W
A51 R253	3	0757-0280	R-F 1K 1% .125W
A51 R254	4	0757-0273	R-F 3.01K1%
A51 R255	1	0698-3155	R-F 4.64K 1%.125
A51 R260	1	0698-3155	R-F 4.64K 1%.125
A51 R261	1	0698-3155	R-F 4.64K 1%.125
A51 R262	9	0698-4458	R-F 590 1% .125W
A51 R263	3	0757-0280	R-F 1K 1% .125W
A51 R264	4	0757-0273	R-F 3.01K1%
A51 R265	1	0698-3155	R-F 4.64K 1%.125
A51 R270	1	0698-3155	R-F 4.64K 1%.125
A51 R271	1	0698-3155	R-F 4.64K 1%.125
A51 R272	9	0698-4458	R-F 590 1% .125W
A51 R273	3	0757-0280	R-F 1K 1% .125W
A51 R274	4	0757-0273	R-F 3.01K1%
A51 R275	1	0698-3155	R-F 4.64K 1%.125
A51 R300	9	0698-4458	R-F 590 1% .125W
A51 R301	9	0757-1094	R-F 1.47K1%
A51 R302	9	0698-4458	R-F 590 1% .125W
A51 R303	9	0757-1094	R-F 1.47K1%
A51 R304	9	0698-4458	R-F 590 1% .125W
A51 R305	9	0757-1094	R-F 1.47K1%
A51 R306	9	0698-4458	R-F 590 1% .125W
A51 R307	9	0757-1094	R-F 1.47K1%
A51 R308	9	0698-4458	R-F 590 1% .125W
A51 R309	9	0757-1094	R-F 1.47K1%
A51 R310	9	0698-4458	R-F 590 1% .125W
A51 R311	9	0757-1094	R-F 1.47K1%
A51 R312	9	0698-4458	R-F 590 1% .125W
A51 R313	9	0757-1094	R-F 1.47K1%
A51 R314	9	0698-4458	R-F 590 1% .125W
A51 R315	9	0757-1094	R-F 1.47K1%
A51 R320	9	0698-4458	R-F 590 1% .125W
A51 R321	9	0757-1094	R-F 1.47K1%

REFERENCE DESIGNATOR	CD	H-P PART NUMBER	DESCRIPTION
A51 R322	9	0698-4458	R-F 590 1% .125W
A51 R323	9	0757-1094	R-F 1.47K1%
A51 R324	9	0698-4458	R-F 590 1% .125W
A51 R325	9	0757-1094	R-F 1.47K1%
A51 R326	9	0698-4458	R-F 590 1% .125W
A51 R327	9	0757-1094	R-F 1.47K1%
A51 R328	9	0698-4458	R-F 590 1% .125W
A51 R329	9	0757-1094	R-F 1.47K1%
A51 R330	9	0698-4458	R-F 590 1% .125W
A51 R331	9	0757-1094	R-F 1.47K1%
A51 R332	9	0698-4458	R-F 590 1% .125W
A51 R333	9	0757-1094	R-F 1.47K1%
A51 R334	9	0698-4458	R-F 590 1% .125W
A51 R335	9	0757-1094	R-F 1.47K1%
A51 R400	0	0698-3435	R-F 38.3 1%
A51 R401	7	0698-0082	R-F 464 1% .125W
A51 R402	2	0757-0403	R-F 121 1% .125W
A51 R410	0	0698-3435	R-F 38.3 1%
A51 R411	7	0698-0082	R-F 464 1% .125W
A51 R412	2	0757-0403	R-F 121 1% .125W
A51 R420	0	0698-3435	R-F 38.3 1%
A51 R421	7	0698-0082	R-F 464 1% .125W
A51 R422	2	0757-0403	R-F 121 1% .125W
A51 R430	0	0698-3435	R-F 38.3 1%
A51 R431	7	0698-0082	R-F 464 1% .125W
A51 R432	2	0757-0403	R-F 121 1% .125W
A51 R440	7	0757-0416	R-F 511 1% .125W
A51 R441	7	0757-0416	R-F 511 1% .125W
A51 R442	7	0757-0416	R-F 511 1% .125W
A51 R443	7	0757-0416	R-F 511 1% .125W
A51 R444	5	0757-0399	R-F 82.5 1%.125W
A51 R445	2	0757-0403	R-F 121 1% .125W
A51 R450	7	0757-0416	R-F 511 1% .125W
A51 R451	7	0757-0416	R-F 511 1% .125W
A51 R452	7	0757-0416	R-F 511 1% .125W
A51 R453	7	0757-0416	R-F 511 1% .125W
A51 R454	5	0757-0399	R-F 82.5 1%.125W
A51 R455	2	0757-0403	R-F 121 1% .125W
A51 R480	3	0698-3438	R-F 147 1% .125W
A51 R500	3	0757-0280	R-F 1K 1% .125W
A51 R501	3	0757-0280	R-F 1K 1% .125W
A51 R502	3	0757-0280	R-F 1K 1% .125W
A51 R600	2	0757-0403	R-F 121 1% .125W
A51 R601	4	0698-3439	R-F 178 1% .125W
A51 R800	4	0698-3603	R-F 12 5% 2W MO
A51 R801	4	0757-0984	R-F 10 1% 1/2W F
A51 RA101	9	1810-0273	R-NETW 10P 470X9
A51 RA102	5	1810-0203	R-NETWORK 7X470
A51 RA107	1	1810-0712	R-NETWORK 8 PIN
A51 RA111	5	1810-0203	R-NETWORK 7X470
A51 RA112	5	1810-0203	R-NETWORK 7X470
A51 RA460	2	1810-0713	R-NETWORK 10 PIN
A51 RA461	5	1810-0203	R-NETWORK 7X470
A51 RA464	1	1810-0712	R-NETWORK 8 PIN
A51 RA469	1	1810-0712	R-NETWORK 8 PIN
A51 RA470	8	1810-0769	R-NETW.9X150
A51 RA471	8	1810-0769	R-NETW.9X150
A51 RA472	8	1810-0769	R-NETW.9X150
A51 RA473	0	1810-0381	R-NETWORK 7X150
A51 RA474	8	1810-0769	R-NETW.9X150
A51 RA475	8	1810-0769	R-NETW.9X150
A51 RA476	2	1810-0713	R-NETWORK 10 PIN
A51 RA477	2	1810-0713	R-NETWORK 10 PIN
A51 RA478	2	1810-0713	R-NETWORK 10 PIN
A51 RA479	2	1810-0713	R-NETWORK 10 PIN

REFERENCE DESIGNATOR	CD	H-P PART NUMBER	DESCRIPTION
A51 RA500	8	1810-0280	R-NETWORK 9X10K
A51 RA510	8	1810-0280	R-NETWORK 9X10K
A51 RA520	8	1810-0280	R-NETWORK 9X10K
A51 RA530	8	1810-0280	R-NETWORK 9X10K
A51 RA540	8	1810-0206	R-NETWORK 7X10K
A51 RA550	8	1810-0206	R-NETWORK 7X10K
A51 RA551	8	1810-0206	R-NETWORK 7X10K
A51 RA552	8	1810-0206	R-NETWORK 7X10K
A51 RA553	8	1810-0206	R-NETWORK 7X10K
A51 RA1000	1	1810-0712	R-NETWORK 8 PIN
A51 S500	8	3101-2097	SW-SL 6-1A
A51 S501	8	3101-2097	SW-SL 6-1A
A51 S502	8	3101-2097	SW-SL 6-1A
A51 S503	8	3101-2097	SW-SL 6-1A
A51 TP1	6	0360-2264	TEST POINT
A51 TP2	6	0360-2264	TEST POINT
A51 TP3	6	0360-2264	TEST POINT
A51 TP4	6	0360-2264	TEST POINT
A51 TP5	6	0360-2264	TEST POINT
A51 TP6	6	0360-2264	TEST POINT
A51 U100	4	1820-3461	IC MC 10H115 P
A51 U101	2	1820-3576	IC DIG 10H175
A51 U102	4	1820-3461	IC MC 10H115 P
A51 U103	4	1820-3461	IC MC 10H115 P
A51 U104	4	1820-3461	IC MC 10H115 P
A51 U105	4	1820-3461	IC MC 10H115 P
A51 U106	4	1820-3461	IC MC 10H115 P
A51 U107	9	1820-2848	IC MC10H116P
A51 U109	2	1820-3435	IC MC10H209L
A51 U110	0	1820-2823	IC MC10H102P
A51 U111	9	1820-2822	IC MC10H105P
A51 U112	9	1820-2822	IC MC10H105P
A51 U120	0	1820-2823	IC MC10H102P
A51 U121	2	1820-3576	IC DIG 10H175
A51 U122	9	1820-2822	IC MC10H105P
A51 U123	9	1820-2822	IC MC10H105P
A51 U300	3	0960-0685	HYBRID-CIRCUIT
A51 U301	3	0960-0685	HYBRID-CIRCUIT
A51 U302	3	0960-0685	HYBRID-CIRCUIT
A51 U303	3	0960-0685	HYBRID-CIRCUIT
A51 U304	3	0960-0685	HYBRID-CIRCUIT
A51 U305	3	0960-0685	HYBRID-CIRCUIT
A51 U306	3	0960-0685	HYBRID-CIRCUIT
A51 U307	3	0960-0685	HYBRID-CIRCUIT
A51 U308	3	0960-0685	HYBRID-CIRCUIT
A51 U309	3	0960-0685	HYBRID-CIRCUIT
A51 U310	3	0960-0685	HYBRID-CIRCUIT
A51 U311	3	0960-0685	HYBRID-CIRCUIT
A51 U312	3	0960-0685	HYBRID-CIRCUIT
A51 U313	3	0960-0685	HYBRID-CIRCUIT
A51 U314	3	0960-0685	HYBRID-CIRCUIT
A51 U315	3	0960-0685	HYBRID-CIRCUIT
A51 U320	3	0960-0685	HYBRID-CIRCUIT
A51 U321	3	0960-0685	HYBRID-CIRCUIT
A51 U322	3	0960-0685	HYBRID-CIRCUIT
A51 U323	3	0960-0685	HYBRID-CIRCUIT
A51 U324	3	0960-0685	HYBRID-CIRCUIT
A51 U325	3	0960-0685	HYBRID-CIRCUIT
A51 U326	3	0960-0685	HYBRID-CIRCUIT
A51 U327	3	0960-0685	HYBRID-CIRCUIT
A51 U328	3	0960-0685	HYBRID-CIRCUIT
A51 U329	3	0960-0685	HYBRID-CIRCUIT
A51 U330	3	0960-0685	HYBRID-CIRCUIT
A51 U331	3	0960-0685	HYBRID-CIRCUIT
A51 U332	3	0960-0685	HYBRID-CIRCUIT
A51 U333	3	0960-0685	HYBRID-CIRCUIT
A51 U334	3	0960-0685	HYBRID-CIRCUIT
A51 U335	3	0960-0685	HYBRID-CIRCUIT
A51 U340	8	1826-0740	ANLG SW
A51 U341	8	1826-0740	ANLG SW
A51 U342	8	1826-0740	ANLG SW
A51 U343	8	1826-0740	ANLG SW
A51 U344	8	1826-0740	ANLG SW
A51 U345	8	1826-0740	ANLG SW
A51 U346	8	1826-0740	ANLG SW
A51 U347	8	1826-0740	ANLG SW
A51 U350	8	1826-0740	ANLG SW
A51 U351	8	1826-0740	ANLG SW
A51 U352	8	1826-0740	ANLG SW
A51 U353	8	1826-0740	ANLG SW
A51 U354	8	1826-0740	ANLG SW
A51 U355	8	1826-0740	ANLG SW
A51 U356	8	1826-0740	ANLG SW
A51 U357	8	1826-0740	ANLG SW
A51 U360	5	1826-0226	IC UA7812HC
A51 U361	6	1826-0178	IC LM320H-12
A51 U440	9	1820-2848	IC MC10H116P
A51 U441	0	1820-2823	IC MC10H102P
A51 U450	9	1820-2848	IC MC10H116P
A51 U451	0	1820-2823	IC MC10H102P
A51 U460	5	1820-3686	IC DIG.10H100
A51 U461	2	1820-2891	IC MC10H101P
A51 U462	1	1820-3400	IC MC 10 H 211
A51 U463	2	1820-2891	IC MC10H101P
A51 U470	5	1820-3595	IC DIGITAL100150
A51 U471	5	1820-3595	IC DIGITAL100150
A51 U472	5	1820-3595	IC DIGITAL100150
A51 U473	5	1820-3595	IC DIGITAL100150
A51 U474	5	1820-3595	IC DIGITAL100150
A51 U500	6	1820-1730	IC SN74LS273N
A51 U510	6	1820-1730	IC SN74LS273N
A51 U520	6	1820-1730	IC SN74LS273N
A51 U530	6	1820-1730	IC SN74LS273N
A51 U540	6	1820-1730	IC SN74LS273N
A51 U542	1	1820-1173	IC MC10124L
A51 U550	6	1820-1730	IC SN74LS273N
A51 U551	1	1820-1173	IC MC10124L
A51 U552	1	1820-1173	IC MC10124L
A51 U560	4	1820-2075	IC SN74LS245N
A51 U561	3	1820-1208	IC SN74LS32N
A51 U562	3	1820-1216	IC SN74LS138N
A51 U563	2	1820-1281	IC SN74LS139N
A51 U570	9	1820-1238	IC-SN74LS253N
A51 U580	9	1820-1238	IC-SN74LS253N
A51 U590	9	1820-1238	IC-SN74LS253N
A51 W1	5	1460-0579	WIREFORM
A51 W2	5	1460-0579	WIREFORM
A51 W3	5	1460-0579	WIREFORM

SECTION 8
SERVICE

8-1 INTRODUCTION

8-2 This section contains the information required to service the HP Model 8175A. The information includes theory of operation, troubleshooting, schematics, component layouts and block diagrams.

8-3 The schematics and component layouts are organized as Service Sheets, which are identified by a large number within a square in the lower right hand corners. These numbers (together with signal identifiers) are used for reference purposes within the theory/trouble shooting sections of the service blocks. Anindex detailing the board assembly/Service Sheet relationship, is given in Table 8-1*. Table 8-2 details the Service Blocks/instrument functions relationships. Schematic diagram symbols are given in Table 8-3.

Table 8-1. Index of assemblies

Assembly	Service Sheet
A1 Mother Board	1
A2 Keyboard	2
A3 Display Driver Bd	-
A10 Power Supply Bd	1A-1D
A20 CPU Board	2A-2G
A30 Clock Board	3A-3E
A40 Data Board	4A-4E
A50 Buffer or Fine Timing Bd*	50A-50B 52A-52D

*Note:
1. Referring to the Power Supply and Fine Timing boards, if your 8175A has a serial number lower than that given at the front of this manual, refer also to the Backdating section.
2. Assembly number A50 can be either a Buffer Board A50 or, (if Option 001) installed a Fine Timing Board A52.

8-4 SAFETY CONSIDERATIONS

8-5 This section contains warnings and cautions that must be followed for your protection and to avoid damage to the equipment.

WARNING

Maintenance described herein is performed with power supplied to the instrument, and protective covers removed. Such maintenance should be performed only by service-trained personnel who are aware of the hazards involved (for example, fire and electrical shock). Where maintenance can be performed without power applied, the power should be removed. When servicing is complete the After Service Check must be performed.

8-6 AFTER SERVICE CHECK

8-7 Execute the following checks when servicing is completed.

8-8 Disconnect power cord from line. Visually inspect interior of instrument for any sign of abnormal internally generated heat, such as discolored printed circuit boards or components, damaged insulation, or evidence of arcing. Determine cause and remedy it.

8-9 Check cabinet/ground pin continuity in accordance with IEC/VDE. Flex the power cord while making the measurement to detect any intermittent discontinuity. Check internal ground connections on boards and frame. Also check resistance of any front or rear panel terminals marked.

8-10 Check cabinet/line isolation in accordance with IEC/VDE. Replace any component which results in a failure, or refer to Production Memo or Service Note issued by product division for alternate action.

8-11 Check line fuse to verify that the proper value is installed.

8-12 Check that safety covers are installed.

8-13 Check that any co-axial and flat cables are properly connected. Check that all boards are correctly fitted and the required heatsinks are in place.

8-14 Inform Hewlett-Packard (internally, the responsible product division) of any repeated failures in the above tests or any other safety features.

8-15 SERVICE BLOCKS (THEORY/TROUBLESHOOTING)

8-16 The theory of operation and troubleshooting is divided into Service Blocks. Each of these, except the General Service Block, covers a complete function within the 8175A, The General Service block includes an overview of board functions and general points relating to troubleshooting, including a flowchart. This provides a fast means of isolating a fault down to a function. The technician should then proceed to the particular Service Block which deals with that function.

Table 8-2. Index of Service Blocks

Service Block	Functions
General	Overview and troubleshooting guide
1	Power Supply and Mother Board
2	CPU, Keyboard and Display Bd
3	Clock Board
4	Data Board
5	Buffer/Fine Timing (OPT) Board

8-17 Tables and Figures within each Service Block are given three - digit codes e.g.,
Figure 8-3-1. The first digit refers to the Manual Section (8), the second digit to the Service Block and the third to the Figure Number.
Figure 8-3-1 therefore means: Section 8, Service Block 3, Figure 1.

8-18 IC INFORMATION

8-19 IC power supply pinouts and resistor array information etc. for each board assembly, is given on each schematic as required.

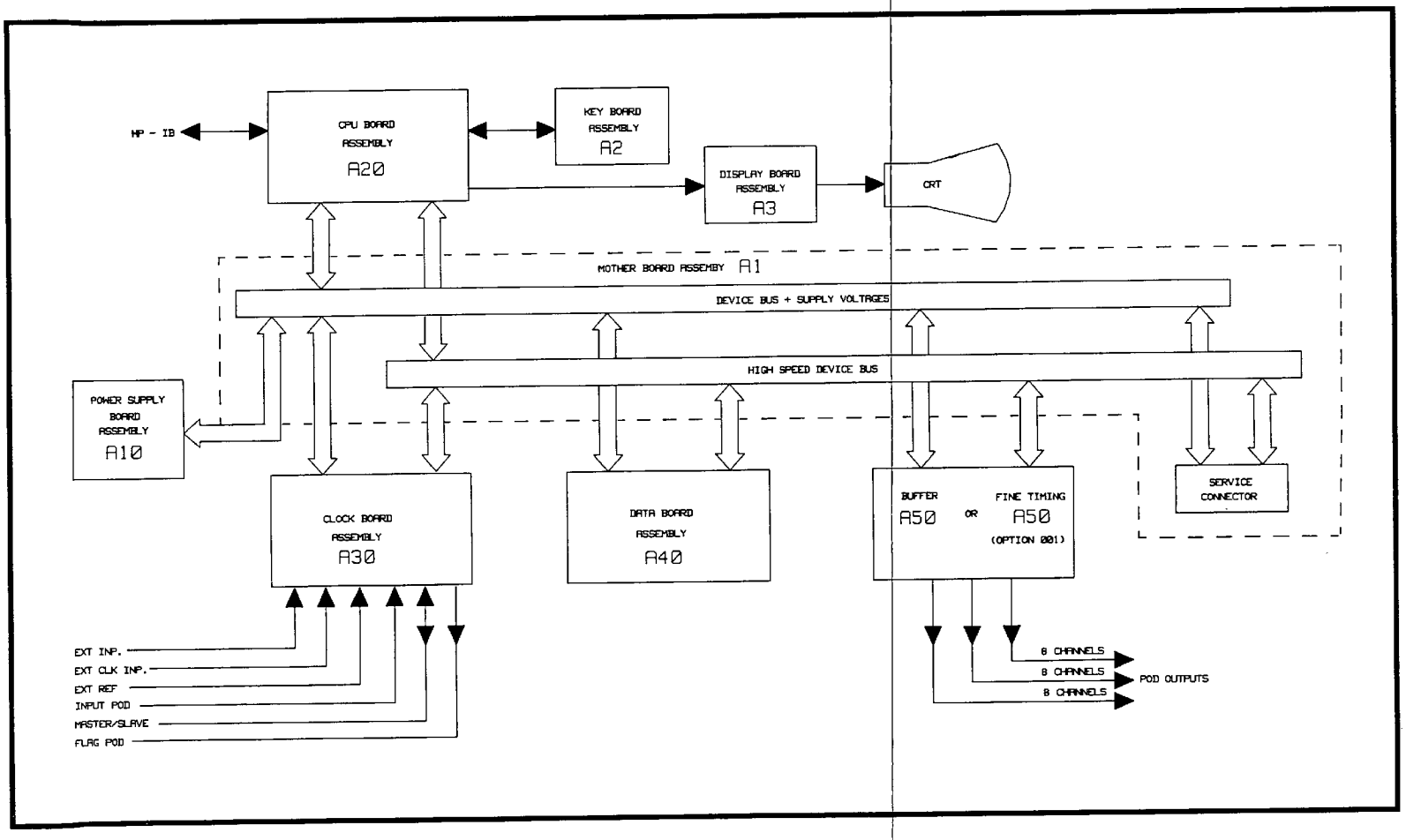


Figure 8-1. 8175A Board Identifier Block Diagram

Table 8-1 Schematic Diagram Symbols

NOTE: The following symbols conform as far as possible with ANSI Y 39.2, IEE No. 315 and ANSI Y 32.14. These standards should be consulted when further information is required.

General

Units — Resistance values are in ohms, capacitance values in microferads and inductance values in microhenries unless otherwise noted !

P/O — Part of

Asterisk denotes a factory selected value. The value shown is the nominal value.

Encloses front panel nomenclature.

Encloses rear panel nomenclature.

Heavy line indicates signal path.

Heavy dashed line indicates primary feedback path.

947 — Wire colour code. Same as resistor colour code. First number is wire body colour.

Wire or plug used as link.

Test point in a circuit. Point may/may not be identified on P.C. board.

Used with trimmer potentiometers or capacitors to indicate screwdriver adjustment.

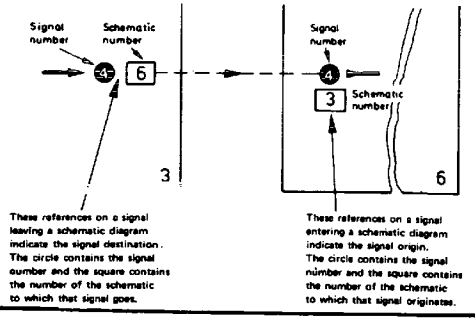
Direct connection to earth.

Ground connection to instrument chassis or frame.

Used when a number of common-return connections are at the same potential. If there is more than one such system in the same circuit, numbers are written in the triangles so that all connections with the same potential have the same number.

xV — Specific potential difference with respect to a potential reference level, eg. +10 V

Schematic Referencing



These references on a signal leaving a schematic diagram indicate the signal destination. The circle contains the signal number and the square contains the number of the schematic to which that signal goes.

These references on a signal entering a schematic diagram indicate the signal origin. The circle contains the signal number and the square contains the number of the schematic to which that signal originates.

Components

Normally open toggle switch. Circles (O) are used for the contacts to indicate a locking type switch.

Spring return, 2-position transfer switch. Triangle ( ) are used for the contacts to indicate a non-locking type switch.

2-position, 2-pole slide switch.

Air cored inductor.

Iron cored transformer. The dot (●) is used, when necessary, to indicate instantaneous polarity.

Capacitor

polarized — variable

bead — Ferrite bead

Relay

Diode

Zener diode

Schottky diode

Light Emitting Diode (LED)

Quartz (Crystal)

Fuse

Battery

15n — Delayline

Transistor

Resistor

variable — c.w

Thermistor / Varistor

Components

Array

" TTL pull up "

" ECL pull down "

" Divider "

Terminals and Connectors

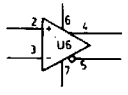
A1 — A2 — J6 — 3 — PIN NO — Soldered connection.

Example of fixed mate and female connectors with plug and socket and contact designators, eg. P.C. board edge connector and socket.

example of bulkhead mounted coaxial socket with free coaxial plug and cable.

example of coaxial cable with termination soldered to P.C. board.

Analog Symbols



Operational amplifier

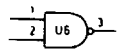
Voltage source

Current source

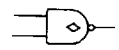
IN — ADJ — OUT — Voltage Regulator

Logic Symbols

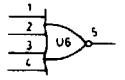
Positive logic is used unless otherwise specified.



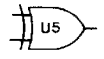
2-input NAND gate



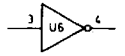
open collector



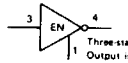
4-input NOR gate



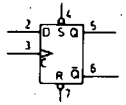
XOR



Inverter

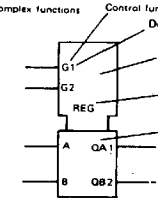


Three-state device. Output is high-impedance when EN is false, irrespective of input. Normal operation when EN is true.

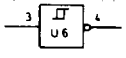


Flip-flop

Complex functions — Control function — Dependency — Control block — Logic function — Data block — Output depends on A and G1 — Output depends on B and G2



Control functions:
G-gate, C-clock EN-3-state, R-reset (Q low) S-set (Q high), ↑ (↓)-count up (down) → shift > edge-triggered.
Logic functions:
REG-register, SEL-selector CNTR-counter, (DE)MUX-(de)multiplexer



Schmitt trigger

Wired AND connection

Wired OR connection

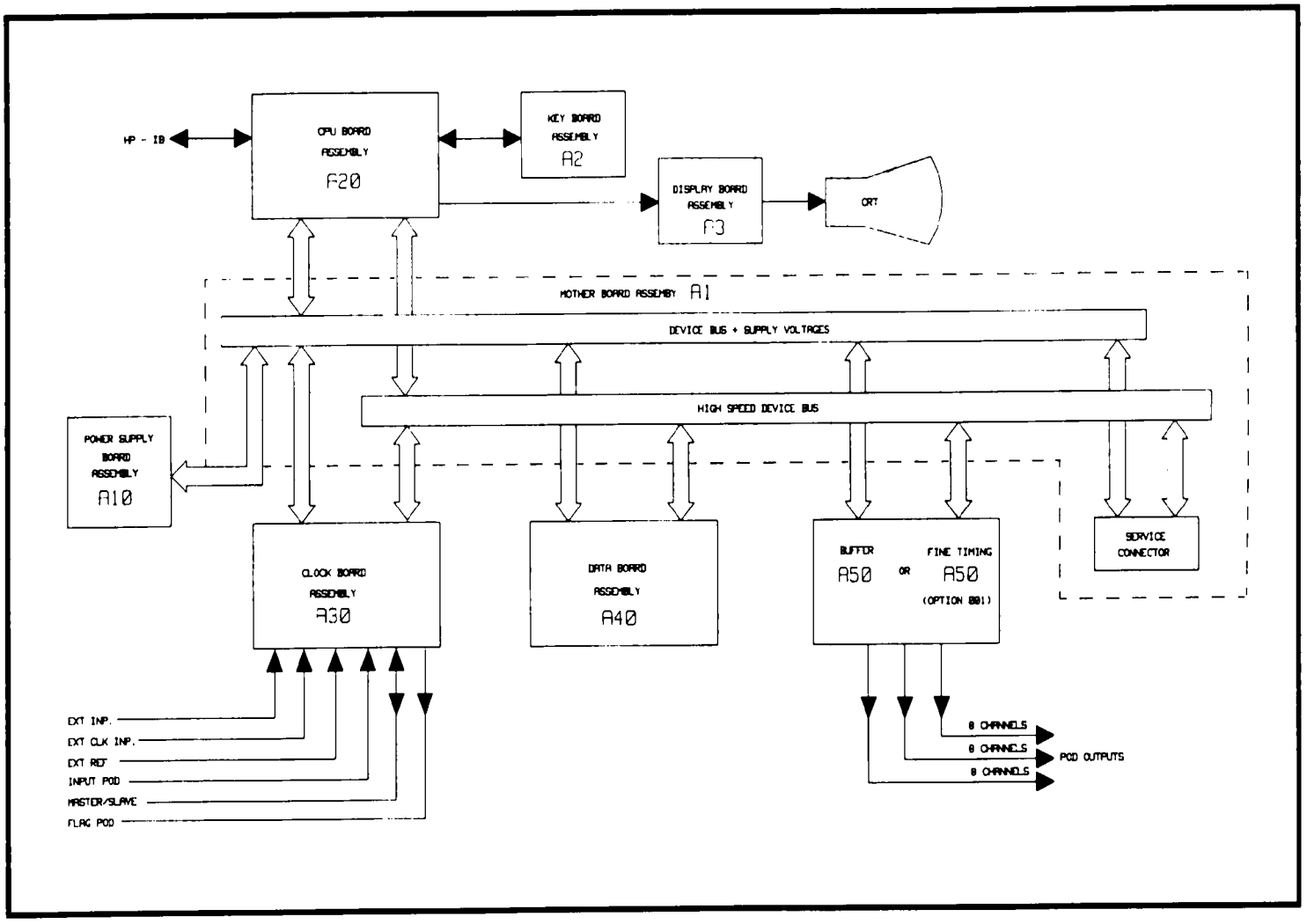


Figure 8-1. 8175A Board Identifier Block Diagram

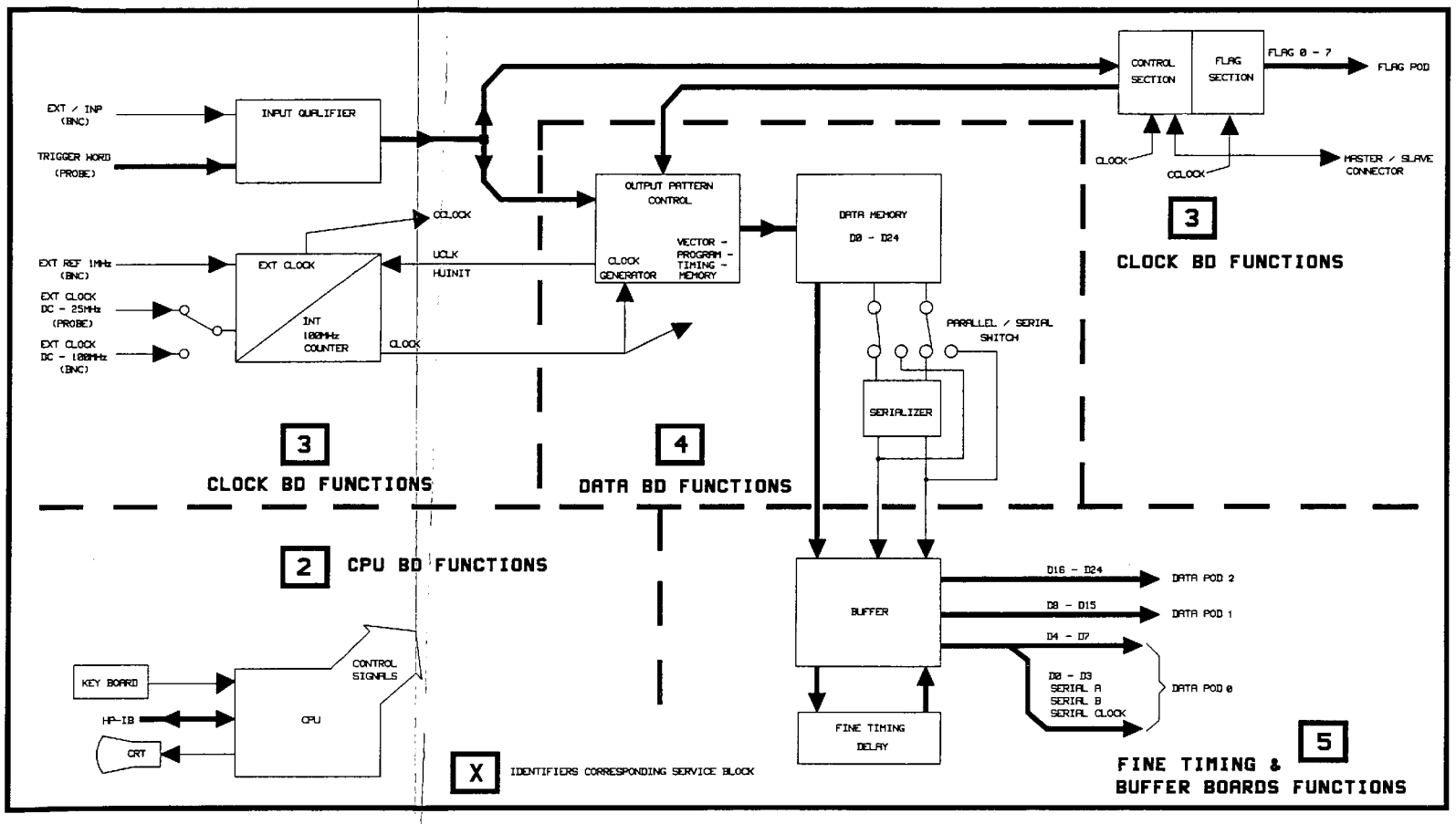


Figure 8-2. 8175A Functional Block Diagram

GENERAL SERVICE BLOCK

OVERVIEW AND TROUBLESHOOTING GUIDE

General

The purpose of this first "general" Service Block is to provide a brief overview of instrument/board functions. Figures 8-1 and 8-2 will help you to identify the boards and their main functions respectively. This will simplify and speed up the troubleshooting process.

Service Blocks 1 to 5 deal with instrument functions in depth. Each Block contains operational theory and a comprehensive troubleshooting guide.

Instrument Self-Test

At switch-on, with the 8175A configured via the HP-IB switch for normal Self Test, it will perform a self-test in order to ascertain that all circuits are functioning correctly. If a fault is detected, an error message will be displayed automatically. Any detected error will result in message identifying the faulty board being displayed. Depending on the type of the fault, the operator may be given the choice to continue using the 8175A or not. A more detailed or "Extended Self Test" is also available. This is described in the Troubleshooting information later in this section.

A flowchart (Figure 8-3) relevant to the previously described self test routines, is included. This will assist you in identifying the board/circuitry connected with any detected fault. In each case, a Service Block number is given alongside the error message. This is the service block that you should first refer to in order to begin in-depth troubleshooting. It may sometimes be necessary to refer to more than one Service Block in order to ascertain the location of the fault.

Shortform Functional Description of the Boards

You should refer to Figures 8-1 and 8-2 when reading the following paragraphs.

PWR (Power Supply) BOARD
This board supplies the various voltages which are used within the 8175A:
+24V, +15V, +15V Video, +5V, -5.2V, -15V and -24V
The power supply uses the "switching technique" for converting AC to the seven DC Voltages.

MOTHER BOARD
All boards are interconnected via the Mother Board. The two internal buses (and the supply voltages) are distributed via the following connectors:

Device Bus and supply voltages: connectors J1, J3, J5, J7, J9, J11 and J13.
High Speed Device Bus: connectors J2, J4, J6, J8, J10, J12 and J14.
Note that connectors J13 and J14 are "test connectors". Any board can be plugged into them (instead of into its normal connectors) and the 8175A operated in the normal way. Although also possible for the PSU board, it is not recommended due to safety reasons!

CPU (Central Processor) BOARD
The CPU Board is the interface between the operator and the system. The CPU board provides the settings related information required by the Data, Clock and Buffer/Fine Timing boards. It also provides keyboard control, display generation, HP-IB interfacing and waveform formation. Whether under HP-IB or local (front panel) control, the CPU board is responsible for all data processing in the instruments.

The CPU board may communicate with compatible external devices via the HP-IB. HP-IB is a parallel bi-directional form of communication. Devices connected to the HP-IB may be either talkers, listeners or controllers. The HP-IB switch (A20 S701) has to be set so as to configure the 8175A for this bus.

DISPLAY Board and CRT
The display drive is an OEM assembly, and is not serviced by HP. The display assembly receives video and timing information from the CPU Board.

CLOCK Board
The Clock Board delivers the 100 MHz master clock and all high speed control signals for the Data Board. It enables the 8175A to be interfaced to external instruments via the Input POD and/or the inputs: EXT. INPUT, EXT. CLOCK INPUT and EXT. REFERENCE. It also provides eight flag outputs, these are auxiliary asynchronous outputs additional to the 24 main outputs from the Buffer/Fine Timing Board.

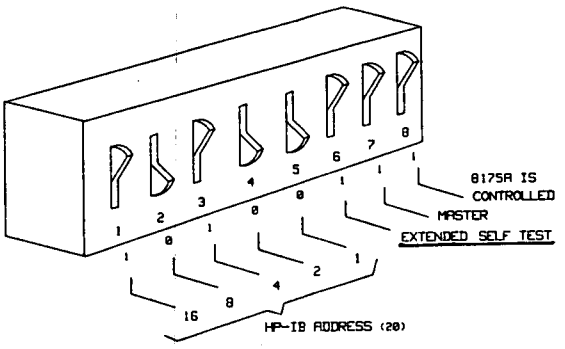
DATA Board
The Data Board generates the information for the 24 data channels, including the program segments requirements. Pattern timing duration is also generated on this board.

BUFFER/FINE TIMING Boards
The 8175A will include either a Buffer or, if Option 001 is installed, then a Fine Timing board. The Buffer Board either sychronizes all 24 data-signals for minimum scew between the channels in Parallel D.G. configuration or, serializes the data-signals to be output from channel 0 and 2 of POD 0 in Serial D.G. configuration.
The Fine Timing Board includes the capabilities of the Buffer board plus a "fine timing" capability. It therefore serves to:

synchronize or serialize the data channels and,
enables 4 channels (2 if Serial D.G.) to be delayed (compared to the same channels when non-fine timed) by between 20 to 40 ns (Parallel D.G.) or 0 to 20 ns (Serial D.G.).

Troubleshooting - General Points

Whenever an instrument fault is suspected, it is recommended that the 8175A be switched OFF and ON again. The normal (not Extended) self-test routine will then be executed. If a fault is detected, then a message indicating which board is involved will be displayed on the 8175A screen. The next step is to initiate the "Extended Self Test". This is done by switching the 8175A off, setting switch element 6 on the HP-IB switch to 1 (see figure below) and switching the 8175A on. The 8175A will now go through an extended self test routine and display a more specific error message. This can be interpreted by reference to Figure 8-3.



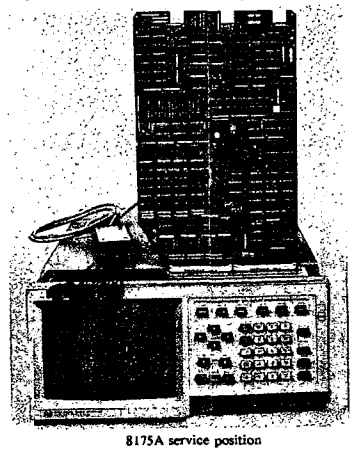
HP-IB Switch: Extended Self Test Setting

Figure 8-3 includes information to assist you in cross-referencing error messages to the actual board/circuit fault area. It should be noted that if a multiple fault condition occurs, the error message displayed will be relevant only to the first fault detected. On successful diagnosis and rectification of each error condition, the instrument will, after switch off and on (assuming a fault still exists), display the error message related to the next detected error condition.

Preparing the instrument for Service:

1. Switch instrument OFF and remove power cord.
2. Remove the upper two feet at the rear of the instrument by unscrewing the fastening screws.
3. Remove the single screw securing the top cover to the rear panel.
4. Slide the cover backwards and remove it.
5. Remove the test (service) connector cover plate (MP9, see Fiure 6-1, Mainframe parts Identifier). Each board (CPU, Data, Clock and Buffer/Fine Timing) can be removed* and plugged into the test connectors as previously mentioned (see Mother Board description). Check that all cable connections (of any cables which have to be disconnected then reconnected) are made properly.

*NOTE: To remove or replace a board, the Board Extractors (MP63 and 64) should be used.



8175A service position

CAUTION

Instrument must not be operated without cover over Power Supply and Fan areas.

NOTE: *In this instrument, both* **metric** *and* **inch** *threaded screws are used! Refer to Section 6 to identify the inch threaded items.*

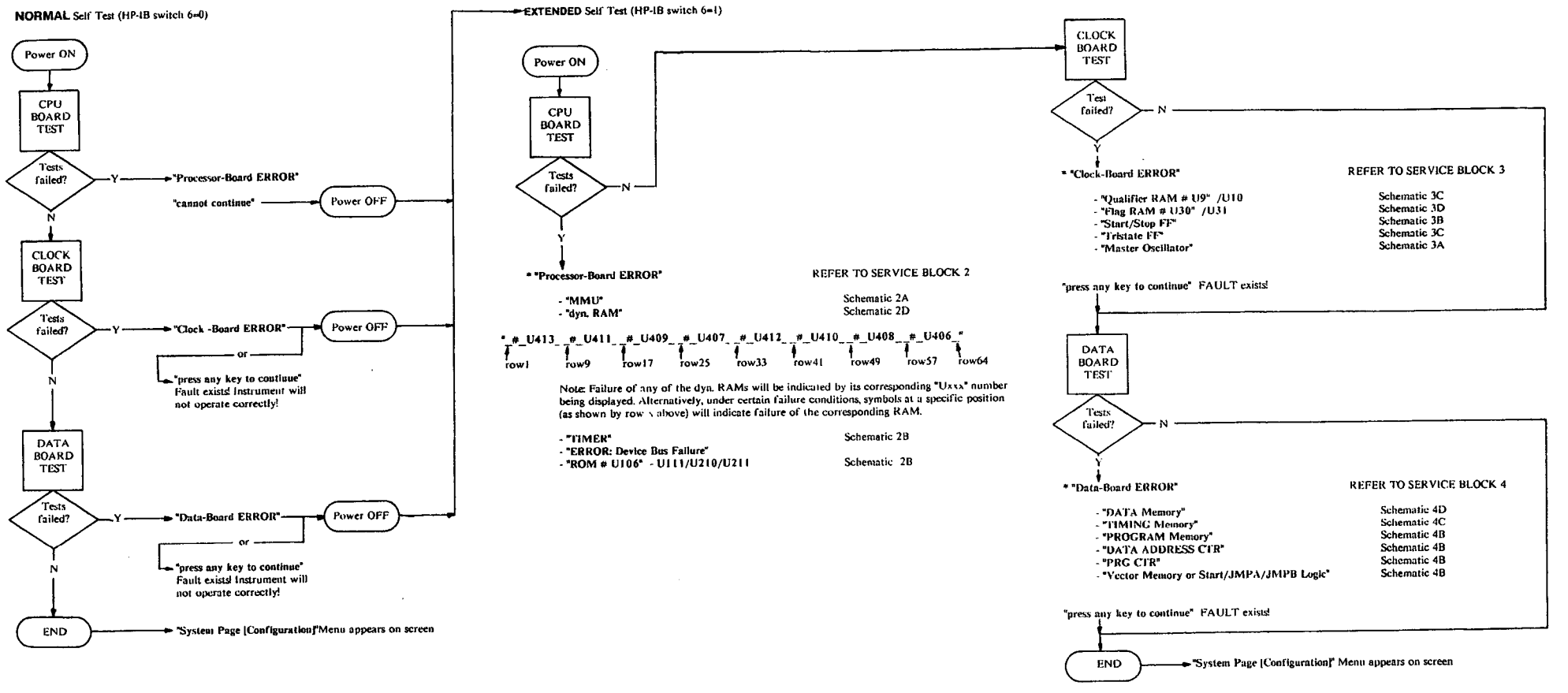


Figure 8-3. Self Test Routine/Troubleshooting Flowchart

Service

REF DES	GRID LOC	REF DES	GRID LOC	REF DES	GRID LOC	REF DES	GRID LOC	REF DES	GRID LOC
C1	B1/2	CR1	C/D2	MP10	E/F1/3	R43	D2	TP2	A6
C2	A/B1/2	CR2	C6	MP11	G2	R44	I3	TP3	A7
C3	C/D3/4	CR3	D6	MP12	F1/2	R45	I1	TP4	A7
C4	B/C3	CR4	A6			R46	I3	TP5	E6
C5	B/C4	CR5	E6	MP13	I1	R47	I1	TP6	E6
				MP14	G2/1				
C6	B4/5	CR7	E5	MP15	A1	R48	I3	TP7	E5
C7	B4/5	CR8	E5	MP19	F/G3/4	R49	I1	TP8	E6
C8	C4/5	CR9	E5	MP20	F/G3/4	R50	E1	TP9	D7
C9	A6	CR10	G4/5			R51	E2	TP10	A7
C10	A6	CR11	F4	Q1	B5/6	R52	E1	TP11	E6
				Q2	C5/6			TP12	D4
C11	A/B6/7	CR12	F4/5	Q3	G6	R53	E2		
C12	A7	CR13	F/G4	Q4	G6	R54	E1	U1	E/F6
C13	A7	CR14	F/G5	Q5	G/H6/7	R55	E2	U2	D6
C14	D5	CR15	E5	Q6	H5	R56	I5	U3	G5
C15	D6	CR16	H6			R57	H5	U4	D5
				R3	C3			U5	F5
C16	D6	CR17	D4	R4	C3	R58	G5		
C17	D6	CR18	G3/4	R5	C4/5	R59	H5	U6	H6
C18	D7	CR19	G2/3	R6	B6	R60	H5	U7	H5
C19	E6	CR20	E2/3	R7	C6	R67	I6	U8	A6
C20	E5	CR21	D2			R68	G6	U9	B7
				R8	D4			U10	G2/3
C21	F5	CR22	H2	R9	D5	R69	G6		
C22	F6	CR23	I/1	R10	D5	R70	E6	U11	I1
C23	E7	CR24	E1	R11	D6	R71	E7	U12	F1
C24	F5	CR25	E2	R12	D7	R72	G2	U13	F2
C25	F7	CR26	G2			R73	G2	U14	G2
		CR28	G5	R13	D6				
C26	F7	CR30	H5	R14	D7	R74	F/G2	VR1	I6
C28	F7			R15	F5	R75	I6		
C29	F6	DS1	E4	R16	F5	R76	I6		
C30	G4	DS2	I5	R17	F5	R77	I6		
C31	G4					R78	I6		
		E1	C2/3	R18	F6	R79	I/J6		
C32	G4	E2	C3	R19	F6	R80	H5		
C33	G5			R20	F6				
C34	G5	F1	A2	R21	F5/6	RA1	D5		
C35	E4			R22	E6/7	RA2	F5		
C36	G/H6	FL1	A/B1/2			RA3	G6		
				R23	E6	RA4	H5		
C37	H6	J1	J1/2/3	R24	E7	RA5	H5		
C38	H6	J2	J3/4/5	R25	E6				
C40	F4	J3	B5/6	R26	G4	RT1	C1		
C41	F3			R27	G4	RT2	C1		
C42	I/J3	L1	B/C3			RT3	C2		
		L2	B4/5	R28	G4	RT4	D2		
C43	I/J2	L3	B6/7	R29	G4				
C44	E2/3	L4	C6/7	R30	G5	RV1	A5		
C45	D2	L5	I/J3/4	R31	G5	RV2	A4		
C46	G/H2			R32	G5	RV3	E1/2		
C47	H1/2	L6	G/H1						
		L7	F2	R33	E5	S1	B/C/D1		
C48	H2	L8	D/E1/2	R34	E5	S2	A3/4		
C49	I1/2			R35	G6	S3	H4		
C50	E1/2	MP1	B/C5/6	R36	H7	S4	H5		
C51	E2	MP2	C5/6	R37	H6				
C52	F1	MP3	F/G3/4			T1	A5/6		
		MP5	I/J1	R38	H6/7	T2	D/E/F3/4		
C53	F1/2	MP6	F1	R39	H6	T3	C7		
C54	F1/2			R40	F4	T4	D7		
C55	H6/7	MP7	F2	R41	F3	T5	C/D4/5		
C56	G/H5	MP9	A6	R42	E3/3				

REF DES	ORID LOC
J1	B3/4/5
J2	A1/2/3
J3	B3/4/5
J4	A1/2/3
J5	B3/4/5
J6	A1/2/3
J7	B3/4/5
J8	A1/2/3
J9	B3/4/5
J10	A1/2/3
J11	B3/4/5
J12	A1/2/3
J13	B3/4/5
J14	A1/2/3
RA1	A3
RA2	A2
RA3	A1/2
RA4	A1
RA5	A3
RA6	A2
RA7	A1/2
RA8	A1

PSU &
M.-BOARD

SERVICE BLOCK 1
POWER SUPPLY AND MOTHER BOARD

THEORY OF OPERATION

Introduction and Block Theory

This service block covers Power Supply and Mother boards. The Power Suppply is described first. The 8175A power supply comprises three main sections or blocks, these are: Primary, Control and Secondary. Figure 8-1-1 identifies them and the corresponding schematics. The various mnemonics used within block diagrams and schematics of this service block are explained in Table 8-1-1. A brief overview of the functions of each section follows. Then, detailed explanations of each are given.

PRIMARY SECTION.

The primary section provides a rectified and conditioned switching source of approximately +/- 150 V dc, and also a transformed supply for control circuitry power. The primary section also provides protection to the supply from AC input surge current and overvoltage conditions. The internal cooling fans also derive their supply from this section.

CONTROL SECTION.

Control voltage generation, modulation and switching are the main functions of the control section. In addition, failure indication (via LED's) and associated protective (auto Shutdown) action etc, are a function of this section.

SECONDARY SECTION.

The secondary section is responsible for filtering, rectification and feedback for the DC power supply. Also, the Power On Reset circuit and the high level power supply for POD's are within this section. All supplies to the Mother Board (and the PSU Boards' test connector) are output from here.

Detailed Theory of Operation

The following paragraphs provide detailed theory of operation of the Power Supply board. It is presented under three separate headings as previously mentioned. The schematic(s) to be referred to in conjunction with each section, are shown within brackets alongside the headings.

PRIMARY SECTION (Schematic 1A)

When the Line Switch (S1) is turned "ON", the power supply operation begins. AC line is supplied to FL 1 which filters the AC for radio frequency interference (RFI). According to the setting of the line select switch (S2), the primary section will operate in one of two modes, either 230 VAC or 115 VAC.

230 VAC OPERATION

When S2 is in the 230 VAC mode, all four diodes of the bridge rectifier (CR1) are used, so providing full wave rectification. However, the voltage across the + and - outputs of CR1 is still ~ 300 V. In the 230 VAC mode, the primary inputs of T1 will be in series and will therefore still have 115 VAC across each primary winding.
The varistors RV1 and RV2 on the primary side of T1 are for transient suppression.
The thermistors RT1 and RT2 provide surge current protection for CR1.
The fans, in either the 230 VAC or 115 VAC mode, will always have 115 VAC driving them.

115 VAC OPERATION

For the 115V AC mode, the circuitry works as a half wave rectifier. Notice the way that the neutral line is wired to the primary output of the bridge rectifier (CR1). Only two of the diodes of CR1 are used. These are the two that are connected to the AC line input of CR1. This configuration produces ~ 300 V across the + and - outputs of CR1. Furthermore, while in the 115 VAC mode the primaries of T1 are in parallel so that 115 VAC is across each primary.
The outputs of T1 are in parallel and have the same voltage across them during either the 115 VAC or 230 VAC modes.

SURGE CURRENT PROTECTION

Because input filter capacitors C2 and C3 are connected directly across the rectified line, a form of surge current protection is provided to limit line surges during turn on. Thermistors RT1 and RT2 provide this protection.

NOTE: Due to a thermistors' high negative temperature coefficient of resistance, it presents a fairly high resistance when cold (during turn on) and a very low resistance when hot.

OVERVOLTAGE PROTECTION

During an AC overvolt situation E1, E2, RT3 and RT4 provide protection to the supply. When the neon bulbs (E1 and E2) reach their maximum voltage limit (~ 240 V), they drop to a low impedance and draw current through the thermistors (RT3 and RT4) and discharge C2 and C3. Fuse F1 will then blow.

RFI SUPPRESSION

RFI is generated by unwanted frequency energy caused by the switching components in the power supply. Inductors L1 (balun) and C1 prevent this radio frequency interference from being conducted back into the AC line.

WARNING

SAFETY CONSIDERATIONS

C2/R3 and C3/R4 have a discharge time constant of approx. 100 seconds.
The primary voltage lines have ~ 300 V across them, + and - 150 Vdc to ground.
The main filter bank, C2 and C3, contains enough energy to be a potential hazard to life, even with supply turned OFF.
Therefore, wait at least five minutes for C2 and C3 to discharge before servicing the power supply board.

CONTROL SECTION (Schematic 1B)

Control Voltage Operation

As soon as the AC is switched ON, CR4 rectifies the AC and starts charging C11, a ripple filter for the 12 Volt regulator U8. The output of U8 lags the input by about 3 V on power up until it stabilizes at +12 V. U8 is the power supply for the +12 Vc (a control power supply used only on the power supply board). +12 Vc supplies U9 which is the +5 V reference source (+5 Vref).

The control section consists mainly of the circuitry which controls the operation of the pulse width modulator (PWM). Also included is the error detection and execution circuitry needed to control modulation.

PWM Overview (see Figure 8-1-2 Block Diagram PWM)

A pulse width modulator (PWM) requires four signals for proper modulation:
a reference voltage, a feedback from the output to compare with the reference voltage for error detection, feedback current from the output for output current limiting and a predetermined switching frequency.

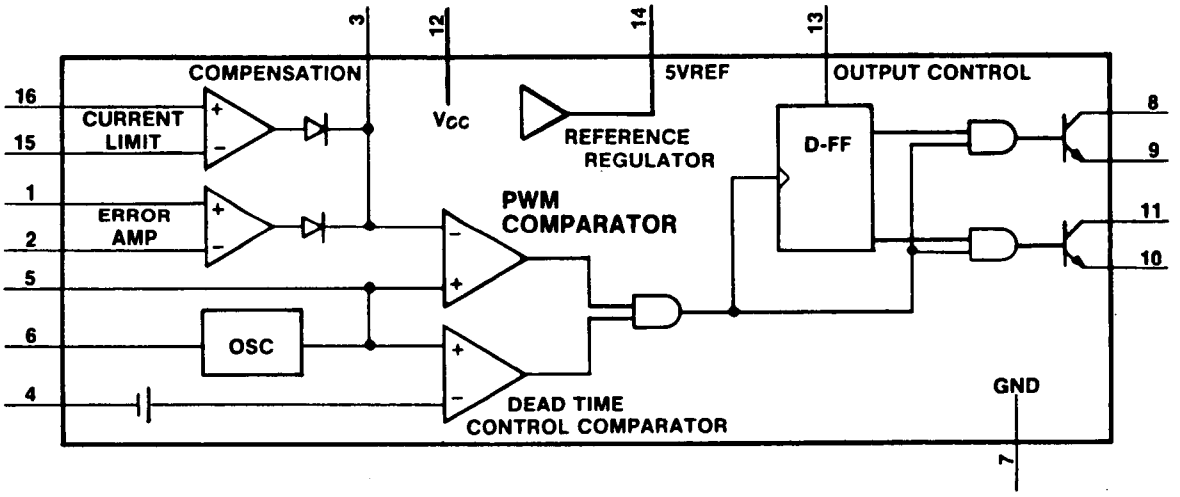


Figure 8-1-2 Functional Block Diagram of a PWM

A PWM modulates its output transistors' pulse width (ON time) according to the demands of the system. In this manner, it controls the amount of current each switching transistor delivers and therefore controls the power. The PWM configuration used by this supply is for push-pull modulation. Push-pull modulation means that each internal open collector output transistor is turned ON alternately by the pulse-steering flip-flop. This configuration is determined by the output control input (OC) pin 13 being tied to the PWM's internal 5 V reference regulator pin 14.

PWM Soft Start

When AC is switched ON, capacitor C19 has not charged. This forces the dead-time control input (DT) pin 4 of U1, to follow the internal 5 V reference regulator output (Vref), pin 14. Note, when dead-time is high both outputs are disabled (100% dead-time). While C19 is charging through R71, the output pulse widths are allowed to modulate slowly until dead-time is low and max. modulation is allowed. Soft start is used to prevent large current surges which may occur on power up. Also, a soft start prevents a false signal, possibly created by control circuitry, from resetting the PWM during power up.

PWM Switching Frequency

The 42 kHz internal oscillation frequency of the PWM (U1), is determined by the RC time constant of R25 and C20 connected to pins 6 (RT) and 5 (CT) of U1. Therefore, each open collector output transistor (pin 8 and 11) turns ON and OFF alternately at about 21 kHz.

Modulation Control

If the + 5V feedback voltage at pin 1 of U1, is higher than the reference voltage at pin 2, the PWM determines that the output voltage is too high. It then reduces its output transistors pulse widths to within limits.

PWM Current Limiting/-5.2 Current Limit

This power supply uses fold-back current limiting (see Fig. 8-1-3).
The actual current limit value is determined by sensing the DC voltage developed across the internal resistance of L5 (schematic 1D ④ / ⑤). Current limiting is done by comparing this voltage with the reference voltage at pin 16 of U1. If the + CL input of the internal comparator (U1/16) goes higher than the -CL input (U1/15), determined by the divider R70/RA1 connected to +5 Vref, the PWM's internal comparator output (refer to Fig. 8-1-2) goes more positive and reduces the width of the output pulses. This then results in a reduction of the output current.

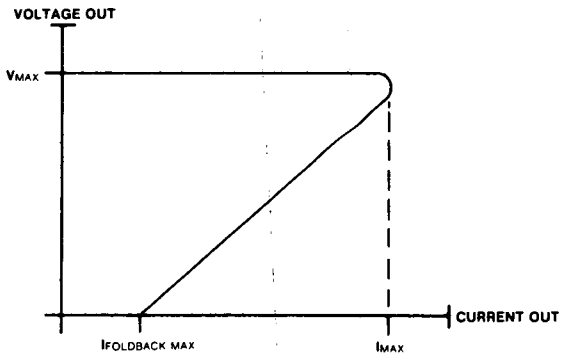


Figure 8-1-3 Fold-back Current Limiting

PWM Failure Execution

There are five failure execution circuits in the 8175A power supply. The effects of three of these failures on the PWM are covered here. The actual failure circuitry is covered later. Three of the failures affect the compensation/PWM comparator input (COMP) U1/3. The COMP input must be allowed to float during normal operation. If an error such as power current limit or a thermal shutdown occurs; pin 3 of U1 will be pulled high and the PWM's output transistors will be shut OFF.
When +5 V current limiting occurs, the PWM reduces modulation.

+5 CURRENT LIMIT
This circuit also uses fold-back current limiting. The DC component is taken from L6 (Schematic 1D ⑥/⑦) and is fed to U3d. The output of this circuit is then fed to the PWM's COMP input (U1/3). When a current limit occurs, pin 14 of U3 goes high, biases CR14, which makes pin 3 of U1 more and more positive and reduces the width of the output pulses.
This then results in a reduction of the output current.

U4 and U5 OPERATION
U4 and U5 are overvoltage sensors. Both U4 and U5 will turn ON an LED (P/O DS1) if an error condition is detected, they will generate SHUTDOWN. U4 and U5 work in the following manner. When the voltage at pin 2 exceeds the voltage at pin 7 by 2.6 volt, the output pin 8 latches high to turn ON the failure LED and generate SHUTDOWN. The capacitor on pins 3 and 4 of U4 and U5 determine the minimum amount of time that an error has to exist before they turn ON, thus preventing transient shutdowns.

POWER CURRENT LIMIT
U4 detects an error via T5. The change of current through the primary side of T5 (Schematic 1A) establishes a current flow in the secondary, rectified by CR17. This produces a voltage drop across R8, detected at pin of U4. If the voltage at pin 2 of U4 is greater than 2.6 volt (a slight delay is provided by C14), U4 latches a turns ON the power current limit LED "PL" (P/O DS1) and sets SHUTDOWN high which turns OFF U1.

THERMAL SHUTDOWN
The circuitry for U5 detects an over temperature condition and generates SHUTDOWN. Two normally closed thermal switches (S3,S4) are mounted on MP3. When the heatsink exceeds 110 degrees C, the thermal switch opens and U5 detects an error.
When pin 8 latches high, the thermal shutdown LED "TH" (P/O DS1) is turned ON. Then SHUTDOWN is generated and U1 is turned OFF.

FAILURE EXECUTION CIRCUITRY (Schematic 1 B)

+5 V OVERVOLTAGE
An overvoltage failure occurs when the +5 volt supply (schematic 1D ⑦) exceeds 6 volts making the voltage at pin 3 of U3A greater than the 5V reference (U1, Vref) on pin 2 of U3A. This in turn makes pin 1 of U3A go high, forcing two operations to occur. The first operation biases CR10 which keeps pin 3 of U3A high regardless of the overvolt condition. The second operation biases CR11, thus making the U2 output pin 16, 13 and 12 low. With U2 pin 12 low the "OV" (overvoltage) LED (P/O DS1) goes ON indicating an overvoltage failure. Furthermore, with U2 pin 16 and pin 13 low, U2 pins 11 and 10 are unable to deliver a switching frequency to the base drive transformers (T3 and T4). This turns OFF the supplies.

-5.2 OVERVOLTAGE
Except for polarity considerations, the -5.2 V overvoltage circuitry (U3B, CR12, CR13) operates the same as the +5 V overvoltage circuit. This circuit turns OFF when the -5.2 Volt supply (Schematic 1D ⑤) exceeds -6.2 volt.

NOTE: If an overvoltage failure or SHUTDOWN occurs, the AC must be switched OFF then ON in order to reset the overvoltage circuitry.

CURRENT SWITCHING OPERATION

The open collector outputs, pins 11 and 8 of U1, are complementary and nonoverlapping. For zero on-time (zero modulation time), both outputs are high. As demand increases, each output stays low (at different times, non-overlapping) for a long period until one is going high as the other is going low or until one of the feedback signals limits the pulse duration. Each output is inverted through U2 (pins 11, 10), another open collector device, and alternately causes changing current through the primaries of T3 and T4. These transformers alternately turn Q1 and Q2 (schematic 1A) ON and OFF which causes the current in the primary of T2 to alternate.

The signals CC1 and CC2 (schematic 1D(8) / (9)) are inverted by U2 (pins 14 and 15) prevent or delay the switching of Q1 and Q2. For example, suppose the following condition exists:
The power supply is experiencing a heavy demand and must allow close to max. modulation to meet it. Q1 has turned ON per the request of the PWM and has pulled the one mode of T2 to the + primary voltage. The PWM tells Q1 to turn OFF and Q2 to turn ON. Q2 can turn ON immediately, but Q1 cannot turn OFF that quickly because of charge storage. The CC2 signal is a feedback signal from the secondary of T2 sense this condition and will not allow Q2 to turn ON until Q1 turns OFF and the voltage on the secondary of T2 stabilizes. To allow Q2 to turn ON sooner, would have the effect of shorting the + primary voltage to the - primary voltage for a short period of time (an enormous waste of power not to mention damage to components).

SECONDARY SECTION (Schematics 1C/1D)

+5 V and -5.2 V Secondaries (Schematic 1D)

The operation of these two (of the four) switching supply secondaries is almost identical. The +5 V supply will be used as an example of their operation.
The alternating voltage in the center tapped secondary of T2 is full wave rectified by two Schottky diodes (CR 19) mounted on a heatsink (MP3). The R41/C41 is a snubber network that limits the dv/dt to protect the diodes. CC1 and CC2 (cross conduction 1 and 2) signals (8) and (9), prevent both switching transistors from being ON at the same time and shortening the + and - primary voltages together. L6 and C43 are the filter for the supply.

Except for polarity and signals CC1/CC2, the - 5.2 V supply is the same as the + 5 V supply.
LED "NORM" (DS2) being ON indicates that the supply is operating properly.

+24 V, -24 V, +15 V, +15 Video and -15 V Secondaries (Schematics 1C/1D)

The alternating voltage of T2 is full wave rectified by CR20 and CR21. R42/C44 and R43/C45 form snubber networks to protect CR20 and CR21. L7 and C46/C47 and also L8 and C50/C51 filter the outputs of the rectifiers before they are regulated by U10, U11, U12, U13 and U14. The outputs of the regulators are filtered by C48, C49, C52, C53 and C54 before the voltages are supplied to the motherboard.

POWER ON RESET (Schematic 1D)

Dependent on + 5V supply conditions, U6 generates the HPSV-signal for resetting the microprocessor and disabling output relays until voltage is sufficient. The threshold voltage of approx. 4.8V, at R 37, is adjustable via R38.

If the + 5V equals the threshold at power on, the reset signal is delayed for approx. 40 ms by C36. HPSV becomes high (> 4.0 V) and the RAMS' on the microprocessor board are supplied by VBAT via Q3. At power down, the signal change is undelayed. The state, if the +5 V is lower than the threshold, will be indicated by P/O DS1 "LPS" ON. HPSV is then low and VBAT is not supplied.
The RAMS then get power from the NiCd-batteries on the Microprocessor Board.

HIGH LEVEL POWER SUPPLY FOR POD'S (Schematic 1D)

This circuit supplies a controlled voltage to the TTL/CMOS-PODs.

The voltage of DAC1 output controls the Output voltage HLPS via U7D and Q6 up to 10.7 V. The control gain is set by R58/R57. The output current is sensed by R59. Its voltage difference is then amplified by U7A and compared with the maximum threshold of U7B. When the current exceeds 715 mA, comparator output U7A pin 1 rises and pulls down output voltage to limit load current.

The following table explains the meaning of the various mnemonics used within this service block.

Table 8-1-1. Mnemonics Explanation

Mnemonic	Meaning and Explanation
+ 12 Vc	+ 12 V Control. This is the control voltage used throughout the supply. If + 12Vc is not in regulation, the supply will not operate properly.
+ 5 Vref	+ 5V Reference. This is the reference voltage used throughout the supply. If + 5 Vref is not in regulation, the supply will not operate properly.
PWM5Vref	Pulse Width Modulator 5 V Reference. A +5 volt reference from U1's internal reference regulator.
SHUTDOWN	This signal is generated in several places and is responsible for turning OFF the PWM U1 by pulling pin 3 high.
"PL"	Power Limit. When this LED is ON, a non-linear surge in current has occured in the primary section. When asserted, the PWM U1 is turned OFF.
"TH"	Thermal. Thermal switches S3 or S4 opens when the MP3 temperature is greater than 110 degrees C. When the "TH" LED is ON, PWM U1 is turned OFF.
"OV"	Over Voltage. When this LED is ON, either the +5 or -5.2 volt supply has exceeded its voltage limits. When asserted, the PWM U1 is turned OFF.

Mnemonic	Meaning and Explanation
"LPS"	Low Power Supply. + 5V is lower than + 4.8 V. Therefore, HPSV is low.
"NORM"	Normal. When this LED is on, the power supply is working correctly.
R+5	Return + 5 . This is the current dependent + voltage. It is used by U3d to set the max. current limit.
R-5.2	Return -5.2. This is the current dependent - voltage. It is used by PWM U1 to set the max. current limit.
CC 1,2	Cross Conduction 1 and 2. Complementary signals used to prevent both switching transistors from being ON at the same time.
DAC1/HLPS	DAC1 voltage controls the output voltage of the High Level Pod Supply.
HPSV	High Power Supply Valid. This signal resets the microprocessor and latches of output relays if +5 V is higher than +4.8 V.
VBAT	VBAT. With HPSV high, Q3 supplies approx. +5 V to the RAM's on microprocessor board. If HPSV is low (unvalid), the RAM's are supplied by 2 NiCd-batteries (+2.4 V) placed on Microprocessor Board. This provides DATA retention.

Mother Board Information

All boards are interconnected via the Mother Board. The two internal buses (and the supply voltages) are distributed via the following connectors:

Device Bus and supply voltages: connectors J1, J3, J5, J7, J9, J11 and J13.
High Speed Device Bus: connectors J2, J4, J6, J8, J10, J12 and J14.
Note that connectors J13 and J14 are "test connectors". Any board can be plugged into them (instead of into its normal connectors) and the 8175A operated in the normal way.

Layout diagram 1 identifies the components on the board. Schematic 1 shows the distribution of the signals. Resistor arrays RA1 to RA8 are used to terminate the lines of the High Speed Device Bus.

PRIMARY SECTION 1A

L
E
N
LINE FILTER
F1
AC
POWER AND VOLTAGE SWITCHES
AC
PRIMARY RECTIFIER CR1
+150V DC
-150V DC
HALF-BRIDGE SWITCHING Q1/Q2
T2
T5 AND RECTIFIER CR17
T3 / T4
FAN
FAN
AC
CONTROL XFMR T1
RECTIFIER CR4
CONTROL POWER U8/U9
+5Vref
+12Vc
POWER CURRENT LIMIT U4
"PL"
SWITCHING CONTROL U2
"TH"
"OV"
+5Vref
+5V
-5,2V
R-5,2
MODULATION CONTROL CIRCUIT R21
-5,2 CURRENT LIMIT
PULSE WIDTH MODULATOR U1
U1Vref
THERMAL SHUTDOWN U5
+5 CURRENT LIMIT U3
+5 OVER-VOLTAGE U3
-5,2 OVER-VOLTAGE U3
R+5
+5V
+12Vc
+5V
+12Vc
+5Vref
-5,2V
CC2
CC1
CC1
CC2
R-5,2
-5,2V
R+5
+5V
+12Vc
CONTROL SECTION 1B

SECONDARY SECTION 1C/D

-5,2V RECTIFIER AND FILTERING CR18
GND
-5,2V
"NORM"
R-5,2V
+5V RECTIFIER AND FILTERING CR19
+5V
R+5
CC2
CC1
+15V/-15V RECTIFIER AND FILTERING CR20
+24V/-24V RECTIFIER AND FILTERING CR21
+15V REGULATION U10/R48
+15V
+15Vvideo REGULATION U14/R74
+15V video
-15V REGULATION U11/R49
-15V
+24V REGULATION U12/R54
+24V
-24V REGULATION U13/R55
-24V
HIGH LEVEL POWER SUPPLY U7/Q5
"LPS"
POWER ON RESET R38
U BAT U6/Q3/Q4

TEST CONNECTOR

DAC1
HLPS
+24V
+15V video
+15V
+5V
-5,2V
-15V
-24V
GND

MOTHERBOARD

GND
-5,2V
+5V
+15V
+15Vvideo
-15V
+24V
-24V
DAC1
HLPS
HPSV
VBAT

POWER SUPPLY BLOCKDIAGRAM

Figure 8-1-1. Power Supply Block Diagram

TROUBLESHOOTING

General

Should a fault be isolated to the Power Supply Board (A10), the theory of operation should be read and understood before proceeding with troubleshooting in this area. A troubleshooting flowchart (Figure 8-1-4) is included. This is designed to simplify identification of the faulty component(s). In addition, a table (8-1-2) which shows for different test conditions, the expected voltage levels at pins of IC's U1, U4 and U5 is included.

WARNING

Troubleshooting and adjustments within the switched power supply area
MUST BE UNDERTAKEN with extreme care.
Harzardous voltages are present on this board
and dangerous energy is stored even after power is removed.
C2/R3 and C3/R4 have a discharge time constant of approx. 100 seconds.
The primary voltage lines have ~ 300 V across them, + and - 150 VDC to ground.
Therefore, wait at least five minutes for capacitors to discharge
before servicing the power supply board.

CAUTION

Instrument must not be operated with out cover over
power supply and fan area.

Do not attempt to replace the 6 screws to fasten CR18, CR19, and U10
(on heatsink A10MP3) without a torque indicating screwdriver.
Tighten the 6 screws to 0.8 Nm torque maximum.

Introduction

Three different troubleshooting procedures are given. It is suggested that you use procedure 1 first and then go on to 2 or 3 depending on the result. Note that procedure 2 is basically a method of checking out the operation of the Control Section. Since it is done with the P.S. board removed from the 8175A and without AC supplied, the actual output voltages cannot be checked.

1. TROUBLESHOOTING USING THE LED FAILURE INDICATORS

Procedure:

By reading the flowchart Figure 8-1-4, and noting which of the corresponding failure indicating LED's are illuminated or not illuminated as appropriate, you can quickly confirm which sections of the Power Supply circuitry are functioning correctly or incorrectly. Note that when the P.S. board is operating correctly, only LED DS2 (NORM) will be illuminated. When any LED from group DS1 is illuminated, it indicates a fault condition.
On completion of this first procedure, go on to 2 or 3 as appropriate.

2. TROUBLESHOOTING WITH POWER SUPPLY BD REMOVED FROM THE FRAME

Procedure:

WARNING

Turn power OFF! Disconnect Power Cord!
Wait at least five minutes for capacitors C2 and C3 to discharge before servicing the power supply board.

Remove the Power Supply Board from the 8175A (disconnect FAN connectors).

Apply +15 V (max. +20 V) between TP2 and GND⊥. ("LPS" LED will switch ON).

Confirm first that the following voltages are correct:

TP3	**TP4**	**TP11 (U1 Pin 14)**
+12 **Vc**	+5 **Vref**	**Vref**
12V +/-100mV	5 V +/-100mV	5V +/- 100mV

Then check that the voltages in the appropriate section of Table 8-1-2 (Board out of Frame) are correct.

Confirm that the waveforms at the Test Points indicated on the schematics are correct. They are shown in the photos of Figure 8-1-5.

Disconnect one wire of Thermal Switch (S3).

Check that you get a "TH" Shutdown ("TH" LED is ON).
Measure voltages at U1 and U5 (see Table 8-1-2).

Switch off the external power supply, and resolder the wire of S3.

With +15V at TP2, apply a DVM controlled positive voltage (+5V) to the +5V test pin on test connector TP1.

Check the function of "LPS" LED for following limits:

"LPS" LED OFF with test voltage >= +4.83V
"LPS" LED ON with test voltage <= +4.85V

Vary test voltage, and verify that "OV" LED turns ON between +5.6V and +6.2V.

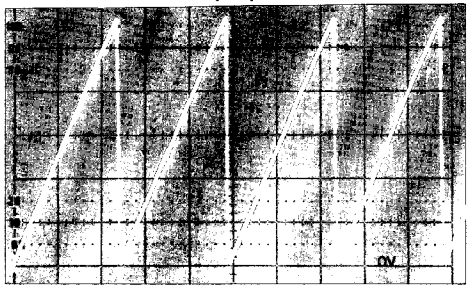
Switch off all external power supplies. Disconnect the test voltage from the +5 V test pin of TP1.

With +15V at TP2, apply a DVM controlled negative test voltage (-5.2V) to the -5.2V test pin of TP1 ("NORM" LED turns ON). Vary test voltage, and verify that "OV" LED turns ON between -5.8V and -6.4V.

Switch off the external power supply, and disconnect the external voltages.

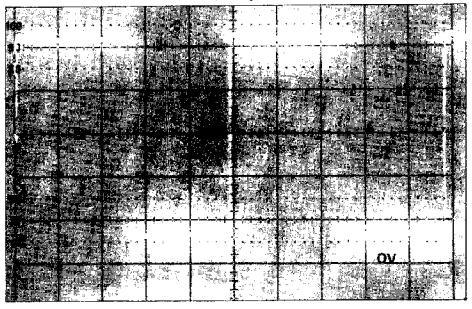
Install the board back in the 8175A, check that all cable connections are made properly, and turn Power ON.
After a few seconds the System Page **[Configuration]** menu should appear.

TP5



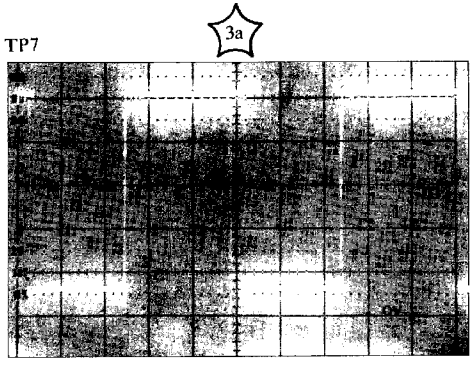
10 usec/DIV 0.05V/DIV

TP8



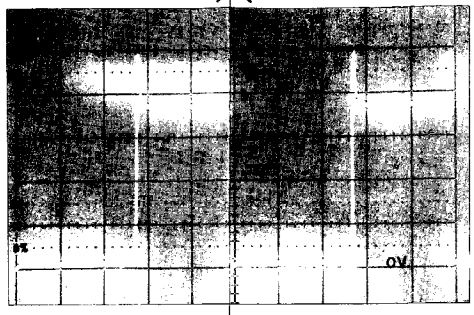
10 usec/DIV 0.1V/DIV

TP7



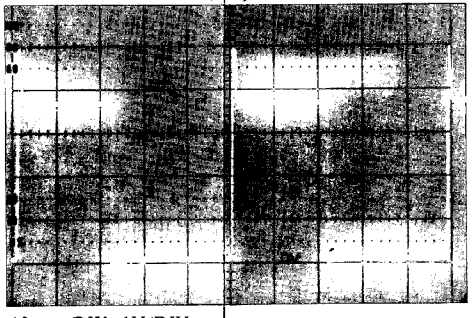
10 us/DIV 0.1V/DIV

TP10



10 usec/DIV 1V/DIV

TP9



10 usecDIV 1V/DIV

Figure 8-1-5. Signal Waveforms For Test Procedure 2

3. TROUBLESHOOTING USING DVM AND SCOPE

Check that the output voltages at test connector (TP1) of A10 are as follows:

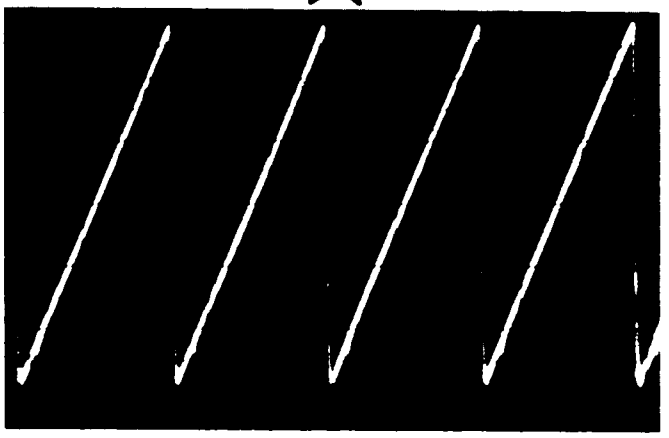
Test Connector TP1	Limit
+5V	+ 5.00V +/- 50mV
-5.2V	- 5.20V +/- 50mV
+15V	+15.06V +/- 20mV
+15V Video	+15.06V +/- 10mV
-15V	-15.06V +/- 10mV
+24V	+24.06V +/- 20mV
-24V	-24.06V +/- 20mV

Then check that the voltages in the appropriate section of Table 8-1-2 (Normal Working) are correct.

Confirm that the waveforms at the Test Points indicated on the schematics are correct. They are shown in the photos of Figure 8-1-6.

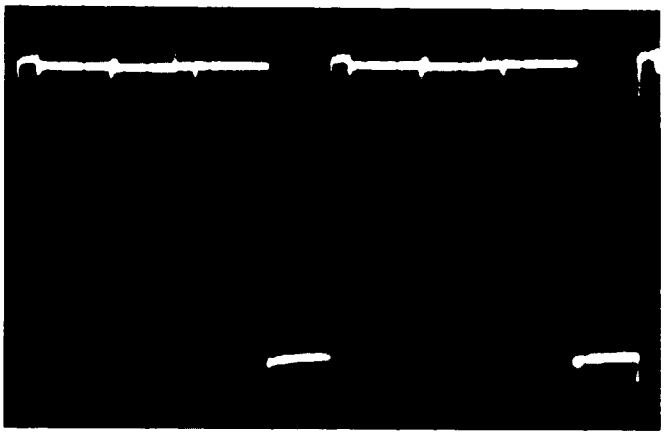
Refer to the flow chart (Figure 8-1-4).

TP5 1



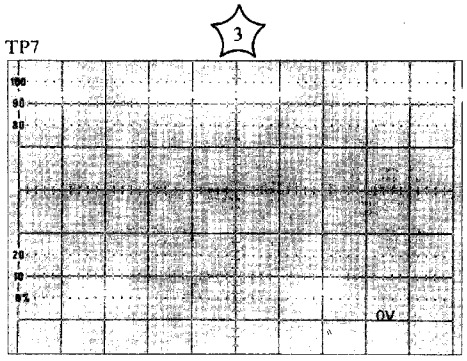
10 usec/DIV 0.05V/DIV

TP8 2



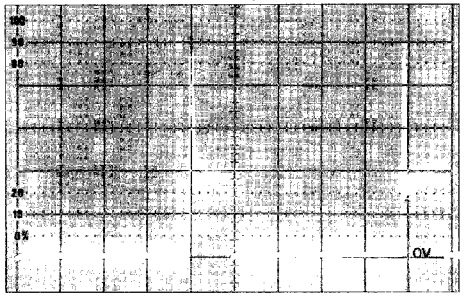
10 usec/DIV 0.1V/DIV

TP7



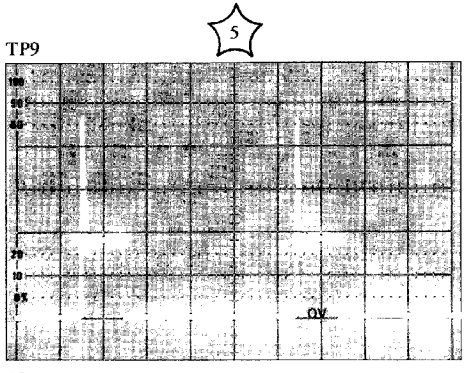
10 usec/DIV 0.1V/DIV

TP10



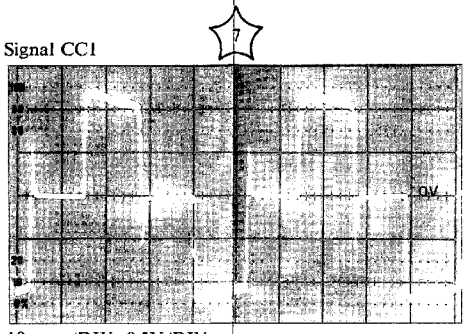
10 usec/DIV 1V/DIV

TP9



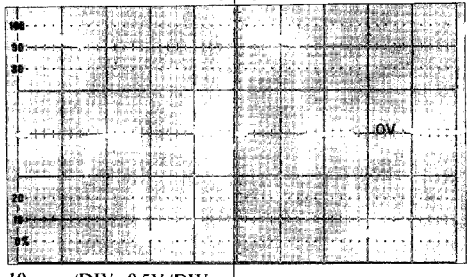
10 usec/DIV 1V/DIV

Signal CC1



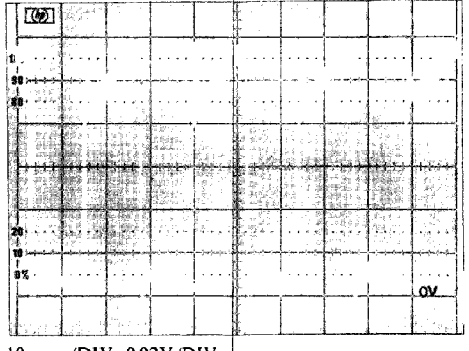
10 usec/DIV 0.5V/DIV

Signal CC2



10 usec/DIV 0.5V/DIV

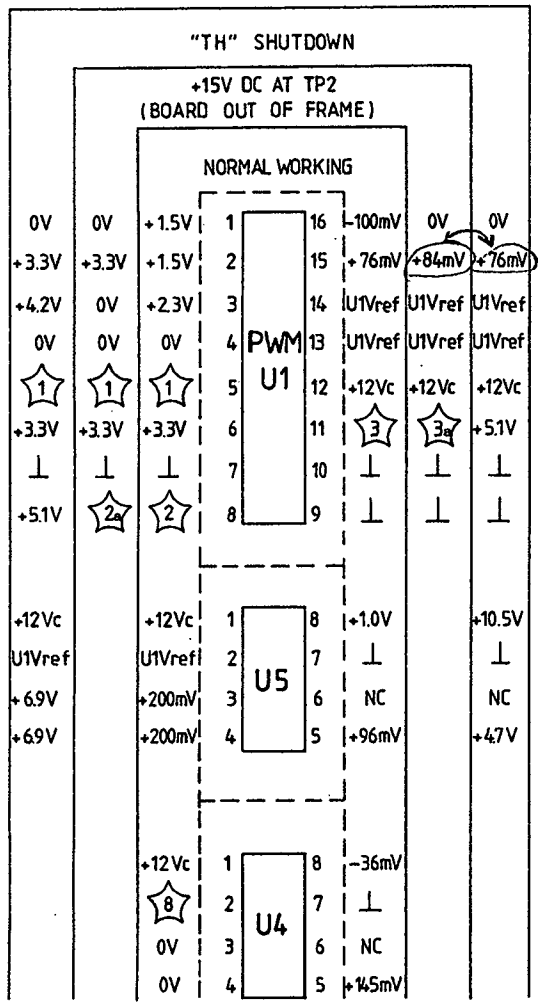
TP12



10 usec/DIV 0.02V/DIV

Figure 8-1-6. Signal Waveforms For Test Procedure 3

TABLE 8-1-2



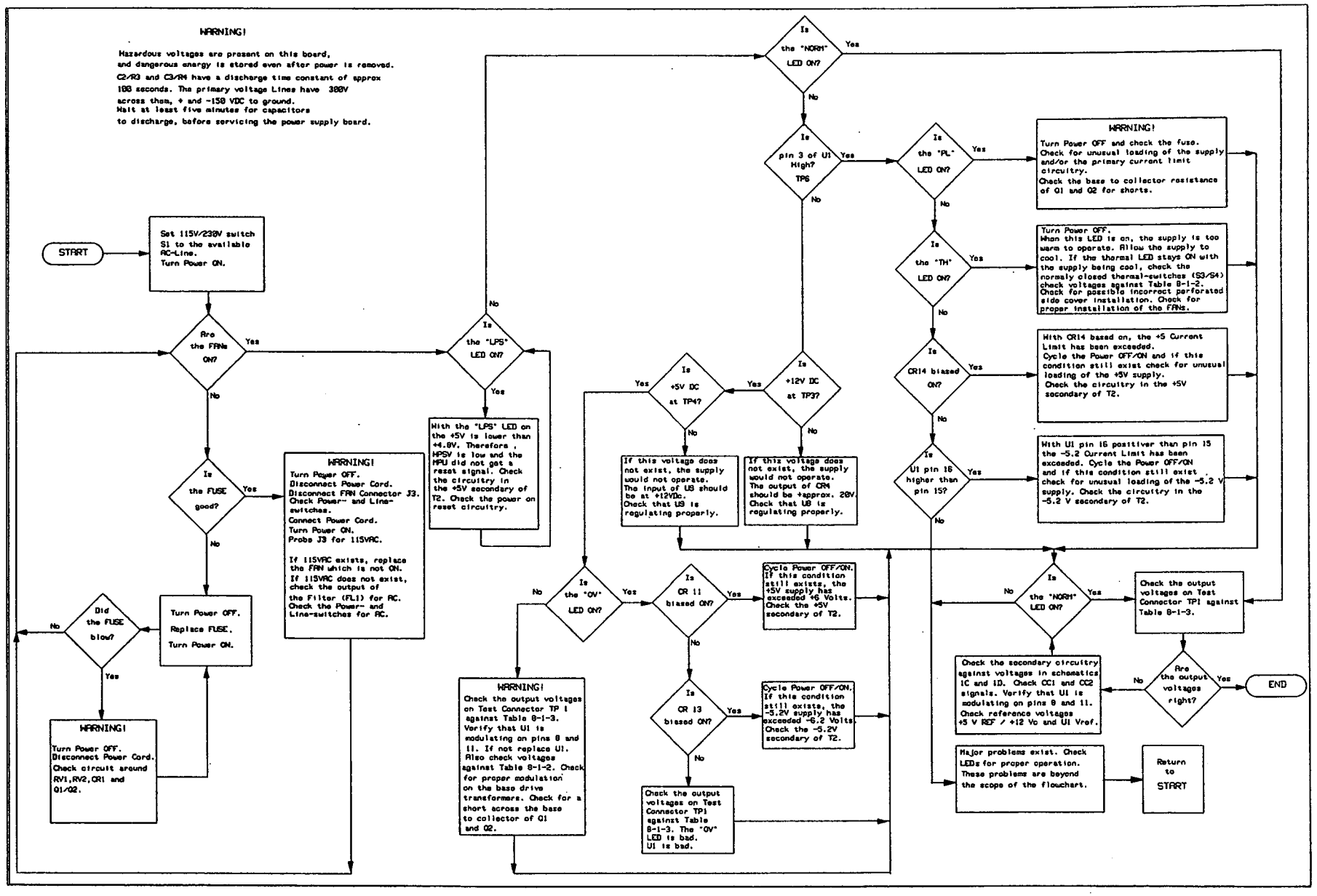
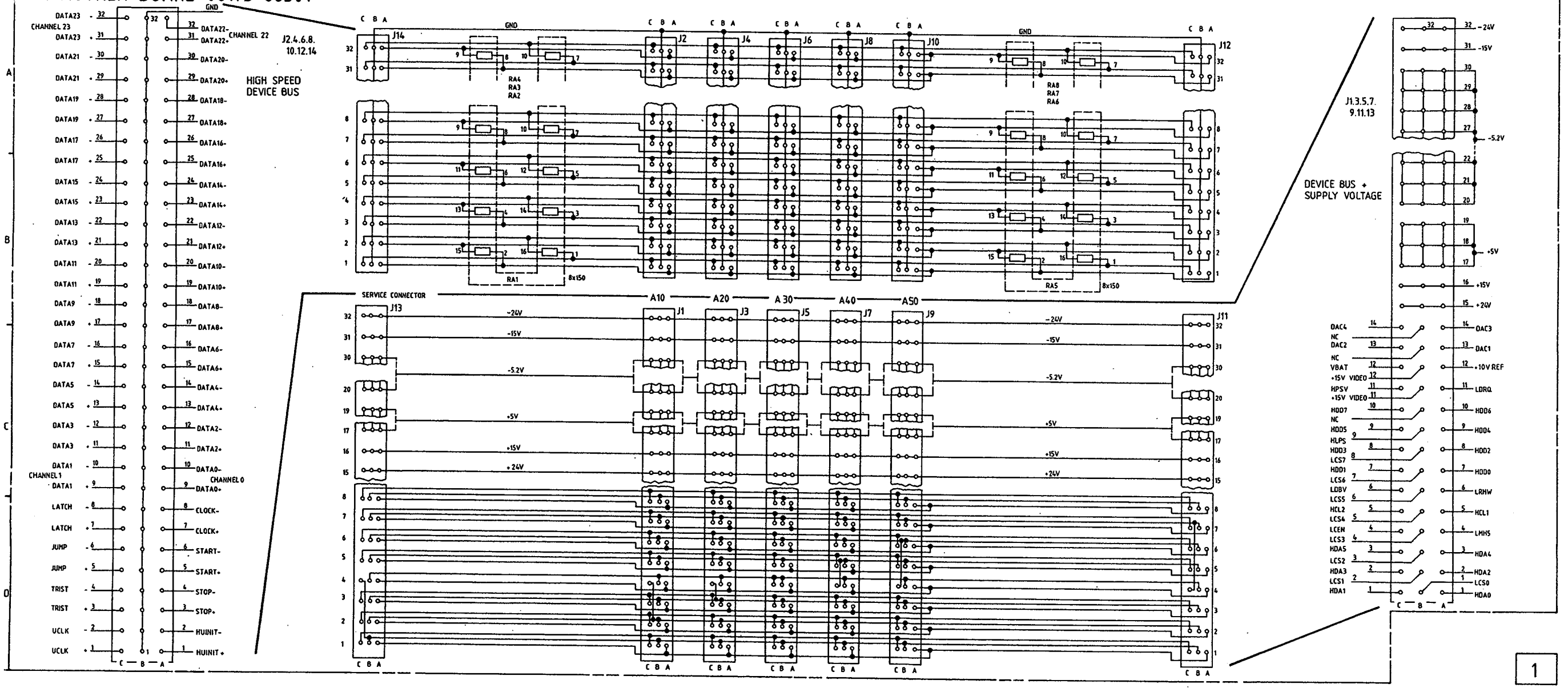


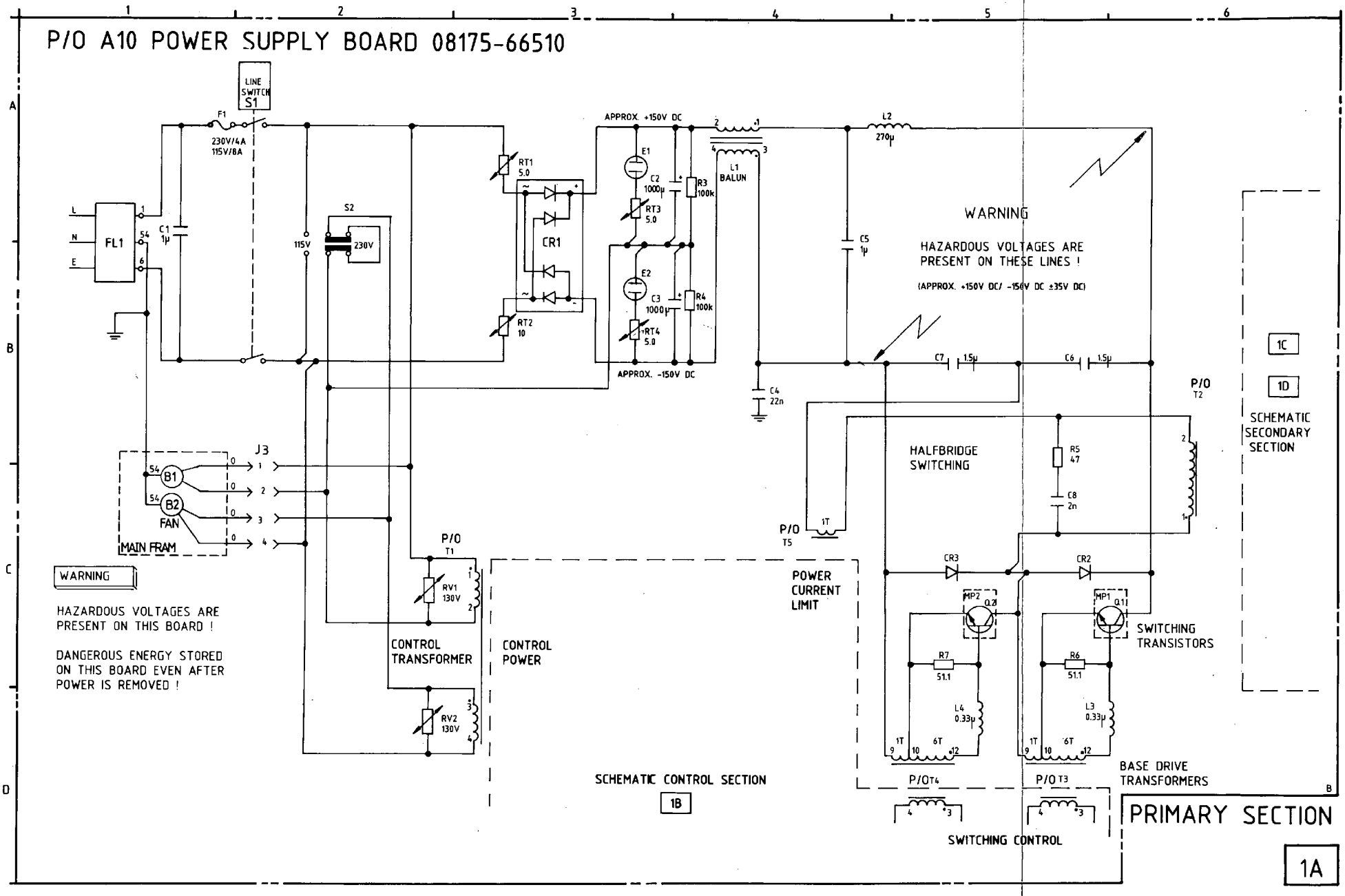
Figure 8-1-4. Troubleshooting Flowchart

A1 MOTHER BOARD 08175-66501

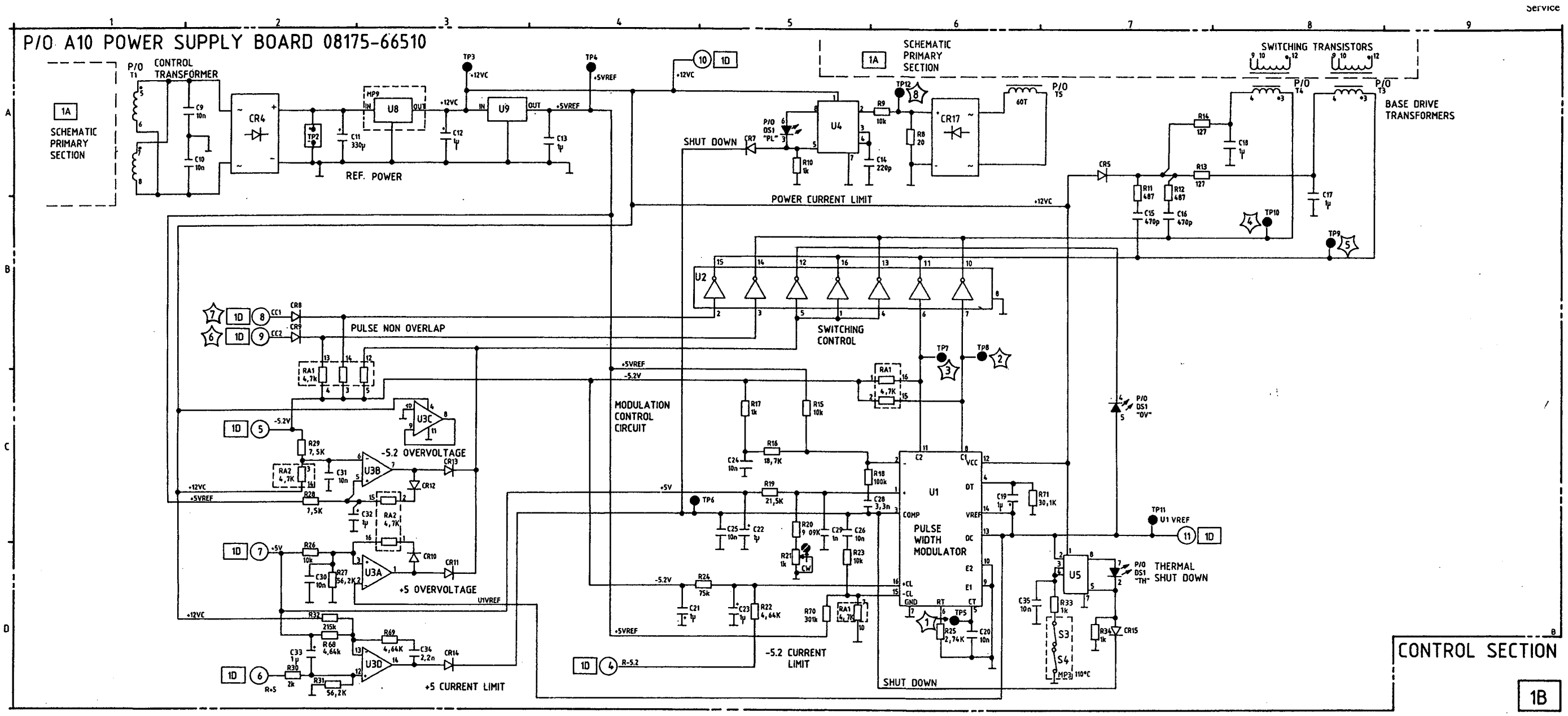


1

P/O A10 POWER SUPPLY BOARD 08175-66510

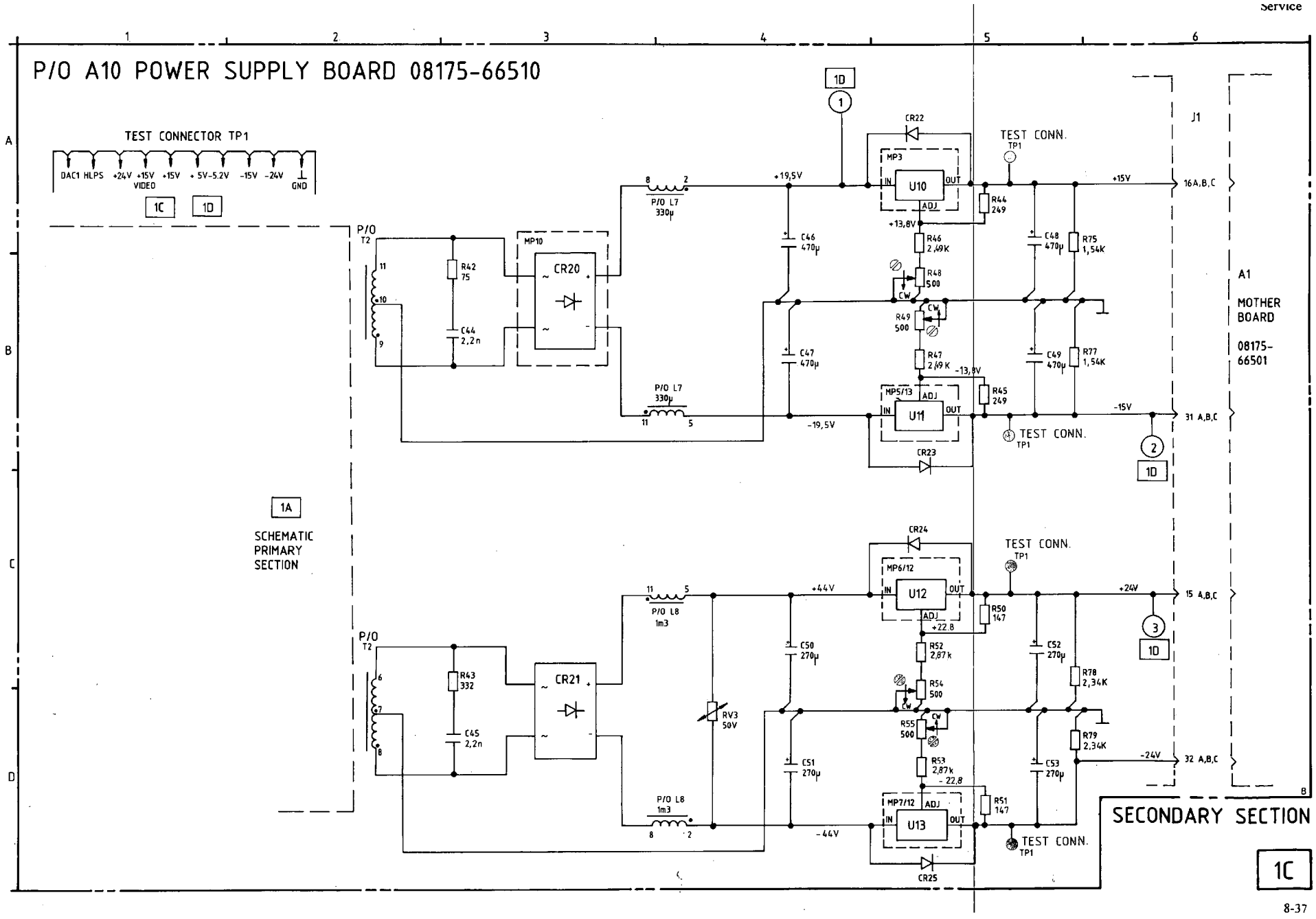


P/O A10 POWER SUPPLY BOARD 08175-66510

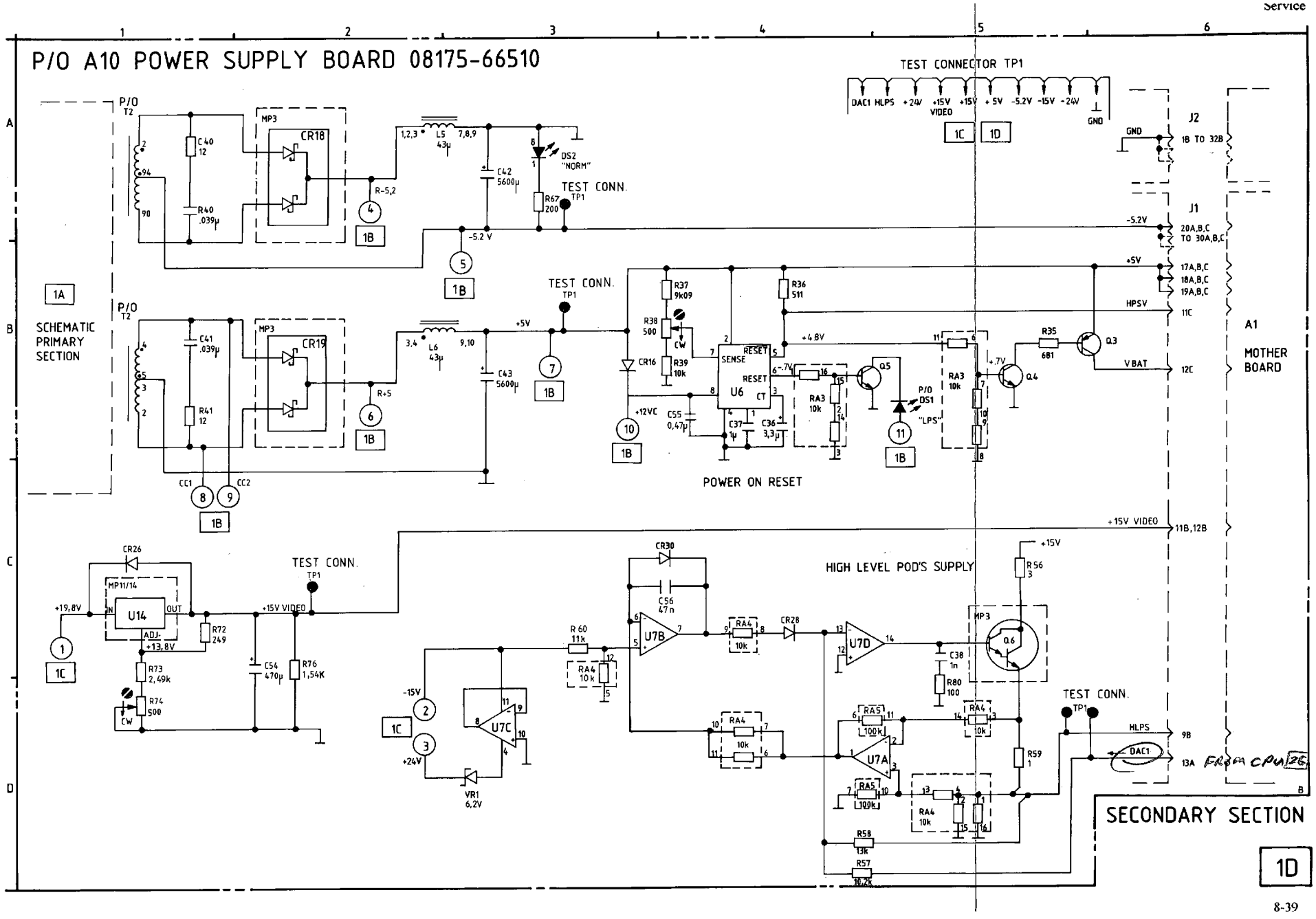


CONTROL SECTION

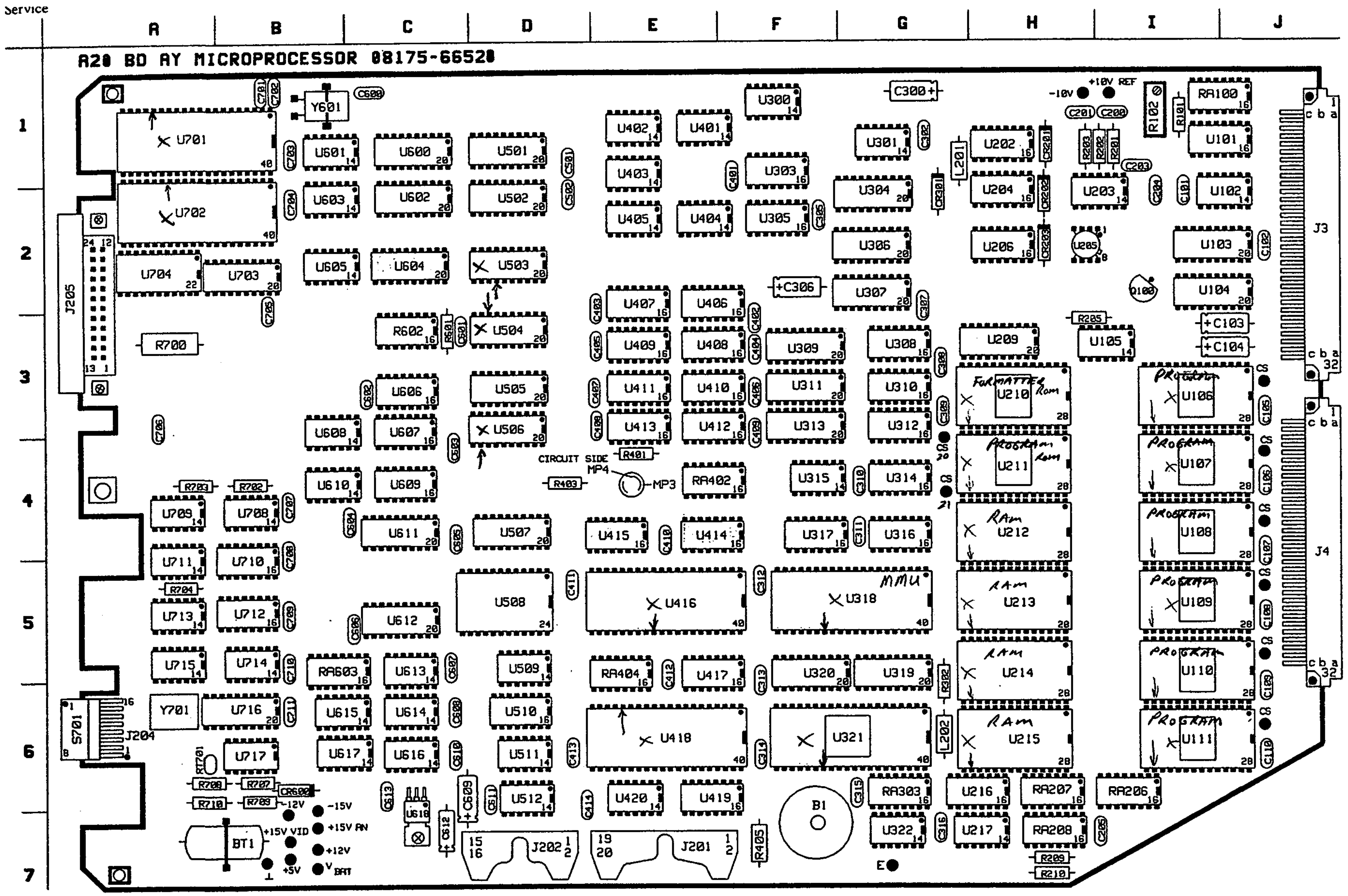
1B


P/O A10 POWER SUPPLY BOARD 08175-66510
TEST CONNECTOR TP1
DAC1 HLPS +24V +15V VIDEO +15V +5V-5.2V -15V -24V GND
1C
1D
1A
SCHEMATIC PRIMARY SECTION
P/O T2
R42 75
C44 2,2n
MP10
CR20
P/O L7 330µ
+19,5V
C46 470µ
C47 470µ
-19,5V
CR22
MP3
U10
ADJ
+13,8V
R46 2,49K
R48 500
R49 500
R47 2,49 K
-13,8V
MP5/13
U11
CR23
R44 249
R45 249
TEST CONN. TP1
C48 470µ
C49 470µ
R75 1,54K
R77 1,54K
+15V
-15V
J1
16 A,B,C
31 A,B,C
A1
MOTHER BOARD
08175-66501
P/O L8 1m3
+44V
-44V
CR24
MP6/12
U12
+22.8
R50 147
C50 270µ
C51 270µ
R52 2,87 k
R54 500
R55 500
R53 2,87k
- 22,8
MP7/12
U13
CR25
R51 147
C52 270µ
C53 270µ
R78 2,34K
R79 2,34K
+24V
-24V
15 A,B,C
32 A,B,C
P/O T2
R43 332
C45 2,2n
CR21
RV3 50V
SECONDARY SECTION

P/O A10 POWER SUPPLY BOARD 08175-66510



CPU &
K.-BOARD



REF DES	GRID LOC	REF DES	GRID LOC	REF DES	GRID LOC	REF DES	GRID LOC	REF DES	GRID LOC
B1	F6/7	C605	C4	R704	A5	U311	F3	U614	C6
BT1	A/B7	C606	B4	R707	B6	U312	G3	U615	B/C6
C101	I2	C607	C5	R708	A/B6	U313	F3	U616	C6
C102	J2	C608	C6	R709	B6	U314	G4	U617	B/C6
C103	I/J3	C609	C6/7	R710	A/B6	U315	F4	U618	C6/7
C104	I/J3	C610	C6	RA100	I/J1	U316	G4	U701	A/B1
C105	J3	C611	D6/7	RA206	I6	U317	F4	U702	A/B1/2
C106	J4	C612	C7	RA207	H6	U318	I/G5	U703	A/B2
C107	J4	C613	C6	RA208	H7	U319	G5	U704	A2
C108	J5	C701	B1	RA303	G6	U320	F5	U708	B4
C109	J6	C702	B1	RA402	E/F4	U321	F/G6	U709	A4
C110	J6	C703	B1	RA404	E5	U322	G7	U710	B4/5
C200	I1	C704	B2	RA602	C3	U401	E/F1	U711	A4/5
C201	H1	C705	B2/3	RA603	B/C5	U402	E1	U712	B5
C203	I1	C706	A3/4	RT701	A1	U403	E1	U713	A5
C204	I2	C707	B4	S701	A6	U404	E/F1	U714	B5
C205	I7	C708	B4/5	U101	I/J1	U405	E2	U715	A5
C300	G1	C709	B5	U102	I/J2	U406	E/F2	U716	A/B6
C302	G1	C710	B5	U103	I/J2	U407	E2	U717	B6
C305	F2	C711	B6	U104	I/J2	U408	E/F2	Y601	B1
C306	F2	CR201	H1	U105	H/I3	U414	E/F4	Y701	A6
C307	G2	CR202	H2	U106	I/J3	U415	E4	Test Point	
C308	G3	CR203	H2	U107	I/J4	U416	E/F5	E	G7
C309	G3	CR301	G1/2	U108	I/J4	U417	E/F5	CS	G3
C310	G4	CR600	B6	U109	I/J4/5	U418	E/F6	CS	G4
C311	G4	J3	J1/2/3	U110	I/J5/6	U419	E/F6/7	CS	J3
C312	F5	J4	J3/4/5	U111	I/J6	U420	E6/7	CS	J4
C313	F5/6	J201	D/E7	U202	H1	U501	D1	CS	J4
C314	F6	J202	C/D7	U203	H/I2	U502	D2	CS	J5
C315	G6	J204	A6	U204	H2	U503	D2	CS	J5
C316	G7	J205	A2/3	U205	H/I2	U504	D3	CS	J6
C401	F1	L201	G1	U206	H2	U505	D3		
C402	F3	L202	G6	U209	H3	U506	D3/4		
C403	E2	MP3	E4	U210	G/H3	U507	D4		
C404	F3	MP4	E4	U211	G/H4	U508	C/D5		
C405	E3	Q100	I2	U212	G/H4	U509	D5		
C406	F3	R101	I1	U213	G/H5	U510	D6		
C407	E3	R102	I1	U214	G/H5/6	U511	D6		
C408	E3/4	R201	I1	U215	G/H6	U512	D6		
C409	F3/4	R202	I1	U216	G/H6	U600	C1		
C410	E4	R203	H1	U217	G/H7	U601	B/C1		
C411	D5	R205	H/I3	U300	F1	U602	C1/2		
C412	E5	R209	H7	U301	G1	U603	B/C2		
C413	D6	R210	H7	U303	F1	U604	C2		
C414	D6/7	R302	G5/6	U304	G2	U605	B/C2		
C501	D1	R401	E4	U305	F2	U606	C3		
C502	D2	R403	D4	U306	G2	U607	C3/4		
C600	C1	R405	F7	U307	G2	U608	B/C3		
C601	C3	R601	C3	U308	G3	U609	C4		
C602	C3	R700	A3	U309	F3	U610	B/C4		
C603	C4	R702	B4	U310	G3	U611	C4		
C604	B4	R703	A4			U612	C5		
						U613	C5		

SERVICE BLOCK 2
CPU AND KEYBOARD

NOTE! IF CPU BOARD IS REPAIRED/REPLACED DO PERFORMANCE TESTS PARAGRAPHS 4-13 4-16 4-21 ADJUSTMENTS ON PAGE 5-4 & 5-5 IF NECESSARY

INTRODUCTION

This service block provides the component level theory and troubleshooting information necessary to service the CPU and keyboard.

The Display System used by the 8175 A is an OEM assembly and is not serviced by HP. The Display Driver, yoke and the CRT are each given a separate HP part number and should be ordered that way. Information to enable you to determine whether the Display System, (rather than the CPU system) is at fault, is included in the Troubleshooting section of this service block.

Note, the terms MPU and processor will be used throughout this manual in reference to the MC68B09E MICROPROCESSOR used on the CPU board.

Block Theory of Operation

Due to the large number of functional blocks within the CPU Board (refer to the block diagram Figure 8-2-1), an overview is first given of these. The order in which each block is described in the overview, is also used in the detailed theory of operation. This simplifies locating any required information.

CONTROL TIMING

The control timing section provides the CPU board with eight timing waveforms. Each waveform and its complement has a frequency of 1.27 MHz and the delay between each adjacent phase group is 50 ns. For example, P1 and P1N lead P2 and P2N by 50 ns.

RESET LOGIC

The purpose of this block is to keep certain key devices on the CPU board OFF while the power supply is turning ON. Different reset logic levels are provided.

MICROPROCESSING CIRCUITRY.

This includes the following sub-circuits:

MICROPROCESSOR UNIT (MPU)

The processor uses three 8-bit bi-directional data buses to communicate with other devices:

HDRW0-7	used for interfacing high impedance devices
HDBRW0-7	used to communicate with TTL devices
HDD0-7	used to reach low speed devices on the CPU board and to communicate or control the other boards in the 8175A via the Device Bus.

Addresses A11-15 are used to select tasks from the Memory Management Unit (MMU). Physical Addresses 0-10 (HPA0-10) combine with addresses HPA11-20 from the MMU to form the Physical Address bus. Clocking of the MPU E and Q clock inputs is provided by the Control Timing Section.

MEMORY MANAGEMENT UNIT (MMU) U318

Expanding the 64K addressable space of the processor, mapping and allocation of memory are some of the functions of the MMU. The MMU, controlled by the processor, outputs the Physical Addresses 11-20.

I/O - DECODING

This circuitry generates the select lines used to address the I/O devices on the CPU board which occupie 1K of memory space (another 1K is reserved for the so called 'Device Bus' used for the communication between the CPU and the other boards in the 8175 A).

CONTROL LATCHES

The processor uses these latches to control and/or enable several functions on the CPU board.

INTERRUPT PROCESSING

This circuitry is responsible for sampling and masking interrupts. The status of all interrupting devices is available to the processor. The MPU sets the priority for each interrupt, masks out lower priority interrupts, and services the interrupt with the highest priority. The priority and masking of each interrupt is determined by firmware.

HP-IB

Communication between separate systems is done over a high speed communications link called "Hewlett-Packard Interface Bus (HP-IB)".

SYSTEM STATUS SWITCH

The HP-IB requires a device address, and a controlled status on the bus. This status is determined by the settings of the system status switches which also select the level off self-test (normal or extended) executed by the 8175A each time the power is turned on, and whether this 8175A is the Master or Slave then two machines are connected together.

ROM AND ROM-SELECTION

The eight 16K word * 8 bit ROMs used by this system are each selected by an addressable 1 of 8 demultiplexer.

WAVEFORM FORMATTER

The purpose of the Waveform Formatter circuitry is to convert the output data information into an appropriate waveform shown on the CRT. The data is sampled for a low or high level or an edge. The information (or the symbols that make a waveform) is then displayed in the full-field graphics area via the dynamic RAM and the graphics buffer.

STATIC RAM, STATIC RAM SELECTION AND BATTERY-BACKUP

The four 8K words * 8 bit static RAMs used in the 8175 A are each selected by an addressable 1 of 8 demultiplexer. To keep their data information even at POWER OFF, the four chips are buffered by a battery which is activated each time the power is turned off.

DYNAMIC RAM

The CPU board also uses eight 64K word * 1bit dynamic RAMs. These RAM can be addressed by three devices (MPU, full-field scanning counter and CRT controller). During each processor cycle, two of them address the RAM (MPU and scanning counter or MPU and CRTC). The output data from these RAMs is latched to an HRAD0-7 bus that can be read by the CPU (over HDRW0-7) or used by either the Character ROM (to generate alpha-numeric symbols) or the graphics buffer to show the data waveforms on the screen.

TIMING CONTROL FOR DYNAMIC RAM

This block generates the timing signals (LCAS and LRAS) necessary to read and write from dynamic RAM. From the three groups which are able to address the dynamic RAM (MPU, full-field scanning counter and CRT controller) only one device is enabled at a given time. The sixteen addresses generated by the active device are then multiplexed by the Address Multiplexer Select (AMS) line into two eight bit address words loaded into the RAMs with LRAS and LCAS.

FULL-FIELD SCANNING COUNTER

This block provides the X and Y scanning information for RAM when graphics information is shown in the graphics area of the display. To provide RAM refresh, the scanning counter access the RAM during each retrace of the beam, even if no graphic mode is active.

CRT CONTROL

This includes the following functions:

CRT CONTROLLER (CRTC)

The CRTC is the interface between the Display System and the processor. Controlling CRT scanning, retrace execution, and cursor positioning are some of the functions of the CRTC. Like the MPU, the CRTC is only allowed to address the dynamic RAM at the proper time in a processor cycle. This is determined by the ON time of the CRT control multiplexers. At this time the full-field scanning multiplexers are disabled and vice versa.

CHARACTER ROM

The Character ROM converts the ASCII code for a given character into the 9 * 16 dot pattern used by this system to display characters. The data output is loaded into the display data shift register where it is serialized and sent to the display.

DISPLAY DATA SHIFT REGISTER AND DISPLAY DATA LATCHES

This block takes parallel display information by either the character ROM or the graphics buffer. The information is converted into a serial data stream and mixed with cursor and video brightness information. This data is then captured by the display data latches and supplied as video information to the display driver.

GRAPHICS OUTPUT BUFFER

The graphics output buffer routes the graphic information (generated by the Waveform Formatter and stored in dynamic RAM) to the display data shift register. When scanning of the full-field graphics takes place, this circuit will be ON and the character ROM will be OFF.

DISPLAY CONTROL

The functions of this block are enabling and disabling of:

- character ROM or graphics output buffer
- full-field scanning or CRTC address multiplexers

KEYBOARD CONTROLLER

Scanning of the keyboard and the four status LEDs from the front panel BNC ports is done by this block. The keyboard controller scans each row and column of the keyboard for a closed switch. When a change in the switch matrix is found, the processor is sent an interrupt request. The four status LEDs are scanned out of the internal RAM of the keyboard controller which is manipulated by the MPU.

KEYBOARD SWITCH PAD AND STATUS LEDS

The keyboard is a switch pad consisting of 39 keys, or switches, wired in a 6 * 8 row/column matrix. The four LEDs used to signalize the active state of the front panel BNC ports are also located on it.

TIMER

The Programmable Timer Unit (PTU) is controlled by the MPU. It provides a clock signal for the interface chip (either HP-IB or RS 232C), a signal source for an audio feedback beeper and different interrupt requests lines used by the MPU for synchronization or the real-time clock feature.

DEVICE BUS INTERFACE

To communicate with the other boards of the 8175 A and with the slow analog circuitry on the CPU board itself, the MPU uses the so called 'Device Bus Interface' which consists of address, data and control lines only changing their state then communication is needed.

ANALOG CONTROL CIRCUITRY

Three 8-bit Digital to Analog Converters are situated on the CPU board, they serve to control reference voltages.

Detailed Theory of Operation

The following paragraphs provide detailed theory of operation including the interfacing of the keyboard and Display System to the CPU. The schematics to be referred to are shown in brackets alongside each heading.

CONTROL TIMING (Schematic 2C)

A 20 MHz clock, derived from the 40 MHz main clock-oscillator Y 701 by D-flip-flop U 716E and NAND gate U 715C, is buffered by NAND gates U 715B and U 715A. It is then used to clock eight ones and then eight zeros through the two 4-bit D-registers U 710 and U 712 . Because the Q output of each D-register is the input for the following phase (that means P0 is the input of P1, P1 is the input of P2,.. and P7N feeds back to the input of P0), U 710 and U 712 form an 8-bit shift register which is forced by U 715D to power up in a twisted-ring configuration.
Each phase P0...P7 and also their complements P0N...P7N, has a frequency of 1.27 MHz and a duty cycle of 50 %. The delay between adjacent phases (e.g. P3 and P4) is 50 ns caused by the 20 MHz clock signal.

RESET LOGIC (Schematic 2A)

The purpose of this circuit is to keep certain circuitry on the CPU board OFF while the power supply is turning ON. The signal concerned with this - HPSV - is generated by the power supply board A10. It has a TTL low level (<0.4 V) and a minimum high level of 4 V which is necessary for the input level requirements of RST input of MPU U321/37 and MMU U318/20. This signal is also used to inactivate (HPSV = L) the chip select circuitry of the static RAM via the transistor array U217 (schematic 2B).
All other devices on the CPU board use the High or Low Master Reset levels of the signals HMR or LMR, derived from HPSV by the NAND gate U 105 C and the Inverter U 322 A.

MICROPROCESSING CIRCUITRY (Schematic 2A)

The processor U321 used by the 8175A is an MC 68B09E microprocessor unit (MPU). The MPU is an 8-bit processor capable of addressing 64K bytes of memory. However, along with the MC68B29 Memory Management Unit (MMU) U318 , up to 2M bytes of memory is addressable.
Table 2-1-1. is the Physical Address-to-allocation (memory map).

Table 8-2-1. Physical Address to Function Allocation

Physical Address	Function
00 0000H 05 FFFFH	Not Used
06 0000H 06 03FFH	Device Bus
06 0400H 06 07FFH	CPU I/O
06 0800H 11 FFFFH	Not Used
12 0000H 13 F7FFH	ROM
13 F800H 13 FFFFH	Not Used
14 0000H 14 FFFFH	Dynamic RAM
15 0000H 15 7FFFH	Static RAM
15 8000H 1F F7FFH	Not Used
1F F800H 1F FEFFH	ROM
1F FF00H 1F FF7FH	MMU
1F FF80H 1F FFFFH	ROM

MPU OPERATION

The MPU U321 communicates and controls the system via an 8-bit bi-directional data bus HDRW0-7 which is buffered by Bus Tranceiver U 503 into a second 8-bit bi-directional data bus HDBRW0-7. The processor addresses the system via 16 output lines. The first 11 of these address lines (A0-10) are latched by octal D-latches U 319 A and U 320 to provide hold considerations and buffering. The remaining 5 processor address lines (A11-15), are used to select one of the 32 task registers in the MMU which then outputs ten physical address lines (PA11-20). Some of these lines are latched and buffered by octal D-latches U 319 A,B and 4-bit latch U 417, before they are combined with HPA0-10 from the processor to form the address bus HPA0-20.

The clock inputs to the MPU are Q and E. Both of them are derived from phases of the control timing, that means each clock has a frequency of 1.27 MHz. The quadrature clock Q (P1N) leads the E clock by approximately 200 ns.

The read/write output indicates the direction in which data is being transfered on the data buses HDRW0-7 and HDBRW0-7. When this line is high, data is being read on the bus. When the read/write output is low, the MPU is writing to the bus.

The Bus Available (BA) U321/6 and Bus Status (BS) U321/5 outputs from the MPU provide the MMU with information about the class of bus operation for each cycle. The following is the MPU state truth table for the BA, BS outputs:

BA	BS	Definition of MPU States
0	0	Normal Running Mode
0	1	Interrupt Acknowledge (RST or IRQ)
1	0	SYNC Acknowledge (not used by the 8175A)
1	1	HALT or Bus Grant (not used by the 8175A)

The NMI, FIRQ, and Halt interrupt inputs to the processor are not used. However, the Interrupt Request line (LIRQ) to the processor (U321/3) is used. When an interrupt is detected in the interrupt circuitry, the LIRQ line is pulled low. With LIRQ low, the processor then initiates an interrupt sequence, provided the condition code register bit (I) is clear.

The RST input to the processor (U321/37), when asserted low, will RESET the processor until the RST line is high again.
Note: The processor will execute the present bus cycle before going to a RESET state.

MMU OPERATION

The Memory Management Unit (MMU) U318 is used to expand the 64K byte addressable space of the processor to a maximum of 2M byte. Expansion is achieved in two steps as follows:

(1) **Loading the MMU** is done when addresses A11-15 are all ones, the Register Access (LRA) line encoded from addresses HPA7-10 is active low. In this case, the addresses HPA0-6 from the processor select via the RS0-6 inputs which memory location inside the MMU is written to or read from the MPU via the bi-directional data bus HDRW0-7. In this mode, up to 4 blocks (Tasks) each consisting of 32 locations of 10-bit mapping RAM are loaded together with the internal MMU registers, one of them (5-bit task register) specifies which task is active.

(2) **Using the MMU as** an address-expander is done (with LRA inactive) only by addressing the MMU through A11-15 from the MPU. These five addresses select one of the 32 RAM-locations of the active task. The MMU therefore outputs the corresponding 10-bit content as the ten Physical Address lines (PA11-20). If A11-15 are all ones, the 128 bytes occupied by the MMU (LRA = low) can't be used for other devices (see memory-map in Table 8-2-1).

The MMU uses the same reset signal as the processor and the MPU determines the read/write status of the MMU via its R/W signal.

Also, the E clock is shared by MMU and MPU. The Q clock of the MMU leads that of the MPU by 50 ns to shorten the time where the addresses PA11-20 are in tristate.

I/O DECODING (Schematic 2A)

To select, or enable, an I/O operation and/or device, the so called I/O Strobe lines LIS 0-F are used. These signals are generated by the addressable 1 of 8 demultiplexers U 303 and U 305. The address of these two demultiplexers are formed from HPA9-10 and HPA20N by the NAND gates U402 A and D. The desired output is then selected via HPA6-8.
To avoid glitches on these select lines, the third enable signal for U303 and U305 is formed by the AND-OR-INVERT gate U 709A from timing signals (P3N, P4N and P6N) and the read/write signals HR, HW. Therefore, in read or write operation, this signal occurs when all other inputs are stable and changes before the others change their state. Table 8-2-2 shows the relation between I/O strobe and related function.

Table 8-2-2. Relationship between I/O, Strobe and Related Functions

Physical Address		I/O Function		Strobe Mnemonic
0EC00H	..	0EC3FH	read HP-IB address switch	LIS 0
0EC40H	..	0EC7FH	read Interrupt Status	LIS 1
0EC80H	..	0ECBFH	write Interrupt Mask	LIS 2
0ECC0H	..	0ECFFH	write Formatter	LIS 3
0ED00H	..	0ED3FH	write Control Latch U 501	LIS 4
0ED40H	..	0ED7FH	write Control Latch U 502	LIS 5
0ED80H	..	0EDBFH	not used	LIS 6
0EDC0H	..	0EDFFH	not used	LIS 7
0EE00H	..	0EE3FH	HP-IB controller	LIS 8
0EE40H	..	0EE7FH	read/write CRT controller	LIS 9
0EE80H	..	0EEBFH	read Keyboard controller	LIS A
0EEC0H	..	0EEFFH	write Keyboard controller	LIS B
0EF00H	..	0EF3FH	read/write ACIA (RS 232C)	LIS C
0EF40H	..	0EF7FH	read Timer	LIS D
0EF80H	..	0EFBFH	write Timer	LIS E
0EFC0H	..	0EFFFH	not used	LIS F

CONTROL LATCHES (Schematic 2A)

The processor outputs control information onto the bi-directional data bus HDBRW0-7 and clocks it into one of the two octal D-flip-flops U 501 or U 502 via the I/O-select lines LIS 4 or LIS 5. The resultant sixteen outputs are then used to control various system functions. Each control latch bit assignment is given in the following table (Table 8-2-3).

Table 8-2-3. Control Latch Bit Assignment

IC-Nr.	Name of Cntrl-bit	Bit pos. on HDBRW	logic level	Function controlled by this bit
U501	CL 0	0	*	LSB of graphic page
	CL 1	1	*	MSB of graphics page
	CL 2	2	H	enables HVSYNC
	CL 3	3	L	only alphanumeric CRT operation
			H	alphanum. and graphic operation
	CL 4	4	**	LSB of CRT Controller page
	CL 5	5	**	MSB of CRT Controller page
	CL 6	6	X	not used
	CL 7	7	X	not used
U502	CL 8	0	L	enables MPU to addr. ROM0 (U210)
			H	disables MPU to address ROM0
	CL 9	1	L	disabl. FORMATTER to addr. ROM0
			H	enabl. FORMATTER to addr. ROM0
	CL A	2	H	allows 8175A to be HPIBcontroll.
	CL B	3	L	normal Device Bus operation
			H	only read cycle on Device Bus
	CL C	4	X	control line HCL 1 \ used for
	CL D	5	X	control line HCL 2 } Dev. Bus / (***)
	CL E	6	L	clears HTI2 interrupt
	CL F	7	L	clears HTI1 interrupt

NOTE: (* or **): The combination of these two lines determine which 16Kbyte segment of the 64k bytes dynamic RAM is used for CRTC or graphic display operation

MSB	LSB	Kilo byte segment
0	0	0....15
0	1	16...31
1	0	32...47
1	1	48...63

(***): These two lines control the main functions of the Device Bus receivers:

HCL2	HCL1	Function
0	0	enables data bus
0	1	read board code
1	X	not used

INTERRUPT PROCESSING (Schematic 2A)

Eight different interrupts can be generated in the 8175A from five interrupt sources:

High Device Bus Interrupt (HDBI) U322E/10, is an interrupt signal derived from the common Low Device Bus Request (LDRQ) line (J3/11) used from the other boards to signal a request to the MPU.
High KeyBoard Interrupt (HKBI) signals a change in the keyboard matrix.
High Timer Interrupt 1-4 (HTI1-4) are the four interrupt signals generated by the programmable timer unit U701 (Schematic 2F).
High RS 232C Interrrupt (HRSI) is generated by the ACIA used for the RS 232C option of the 8175A. Note, this not currently available.
High HP-IB Interrupt (HIBI) is used to signal the interrupt request of the HP-IB controller U 702 used in the standard version of the 8175 A.

Each interrupt is given a specific firmware priority so that, if two or more interrupts occur simultaneously one will be serviced before the other. Interrupt priority is done by masking out the lower priority interrupts with a zero written into the octal D-latch U602. That means, those interrupts can't propagate through their respective NAND gate U601 or U603. Only the highest priority interrupt is given a one in U602 so that it passes its NAND gate thus, making the Interrupt Request (LIRQ) line low to the processor. The MPU will then service the interrupt, clear the device's interrupt request line, read the interrupt status buffer U600, and change the interrupt mask in U602 to sample the next highest priority interrupt.

HP-IB INTERFACE CIRCUITRY (Schematic 2A)

The Hewlett-Packard Interface Bus transfers data and commands between systems via 16 signal lines. The interfave functions for each system component are performed within the component so only passive cabling is needed to connect systems. The cables connect all instruments, controllers, and other components of the system in parallel. The following is a description of the inputs to the HP-IB controller, and the outputs as they relate to interface operations.

MPU TO HP-IB INTERFACE.

HP-IB controller U702 communicates via thirteen memory mapped registers. Six of the registers are read from, and seven are written to. The registers are used to pass control data to, and status information from, a system component. HPA2-0, connected to the register select lines (RS2-0), are used to select a particular register. A low on the chip enable line (CE) indicates that the processor is doing either a read or write from the selected register. Note that each combination of RS2-0 can indicate one of two different registers depending on whether a read or write operation is occuring. For example, a write operation with RS2-0 = 110 indicates a Parallel Poll register access, but a read to the same location indicates a Command Pass Through register access.

Reading or writing to a register is indicated by the level of HPA3. A high indicates an MPU read and the Data Bus In (DBIN) line will be asserted. When low, the Write Enable line (WE) is asserted and the MPU will write to a register. Data transfer are via the bi-directional data lines HDRW0-7 attached to the D7-0 lines of U702.

HP-IB INTERFACE LINES AND OPERATIONS.

The eight data I/O lines (DIO1-8) are reserved for the transfer of data and other messages in a byte-serial, bit-parallel manner. Data and message transfer is asynchronous and is coordinated by three handshake lines: Data Valid (DAV), Not Ready For Data (NRFD), and Not Data Accepted (NDAC). The other five lines are for management of bus activity. See Figure 8-2-2 for HP-IB signal lines.

Devices connected to the bus may be talkers, listeners, or controllers. The controlling device dictates the role of each of the other devices on the bus by setting the attention line (ATN) true (low true) and sending talk or listen addresses on the data lines.

The MPU reads the rear panel switches to determine its device bus address and loads this into the HP-IB controller. While the ATN line is true, all devices must listen to the data lines. When the ATN line is false, only devices that have been addressed will actively send or receive data; all other ignore the data lines.

Several listeners can be active simultaneously but only one talker can be active at a time. Whenever a talk address is put on the data lines (while ATN is true), all other talkers are automatically unaddressed.

Information is transmitted on the data lines under sequential control of the handshake lines (DAV, NRFD and NDAC). No step in the sequence can be initiated until the previous step is completed. Information transfer can proceed as fast as devices can respond, but no faster than the slowest device presently addressed as active. This permits several devices to receive the same message byte concurrently. For HP-IB handshake timing see Figure 8-2-3.

The ATN line is one of the five management lines. When ATN is true, addresses and universal commands are transmitted on only seven of the data lines using ASCII codes. When ATN is false, any code of 8 bits or less understood by talker and listener(s) may be used. The Interface Clear (IFC) line places the interface system in a known quiescent state via the abort message. The Remote Enable line (REN) is used with the remote, local and clear lockout/set local message to select either local or remote control of each device. Any active device can set the Service Request (SRQ) line true. This indicates the end of a multiple-byte transfer sequence. When the controlling device sets both the ATN and EOI lines true, each device capable of a parallel poll indicates its current status on the DIO line assigned to it.

The Interrupt line (INT) indicates an interrupt request when low. This signal is then inverted by U708 and routed to the interrupt mask where the MPU branches to a subroutine to service this interrupt.

HP-IB TRANSCEIVERS.

All of the input/output signals from the HP-IB controller are routed through two octal bus management transceivers U703 and U704. These devices are controlled by CONT (controller), TE (talk enable), and CLA (system controller). U704 controls the direction of command and data transfer signals. The direction of the command signals ATN, SRQ, and EOI is determined by the CONT line (U704/12), but IFC, and REN are directed by CLA (U704/1). Data transfer signals NRFD, NDAC, and DAV are controlled by TE (U704/2). The direction of a data flow through U703 is determined by ATN or EOI (U703/11). While TE (U703/1) controls whether U703 is tri-stated or in the open-collecter (enable) mode.

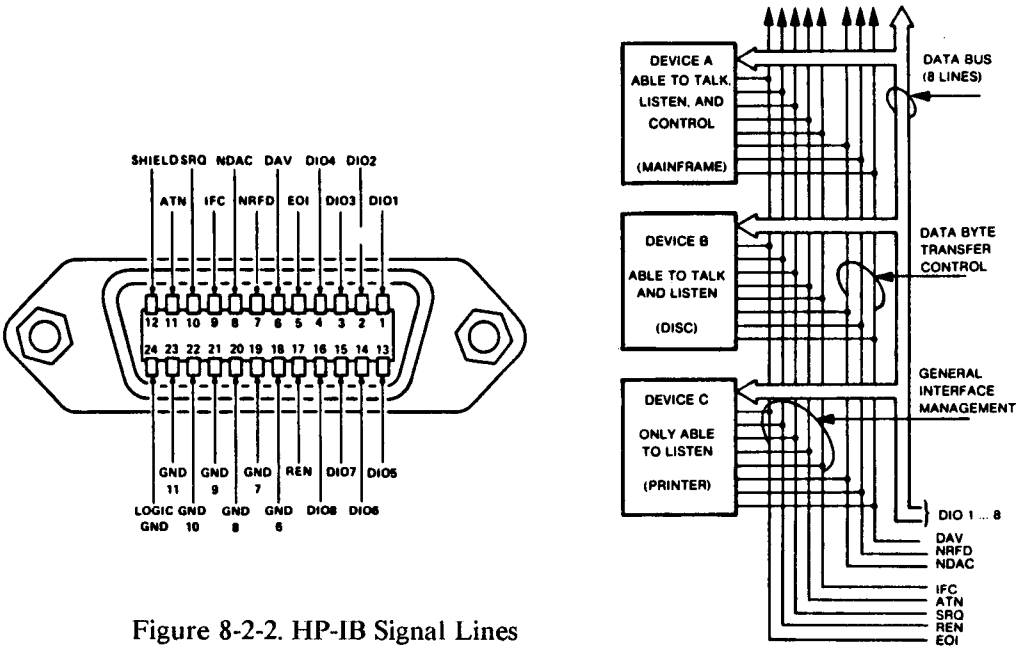


Figure 8-2-2. HP-IB Signal Lines

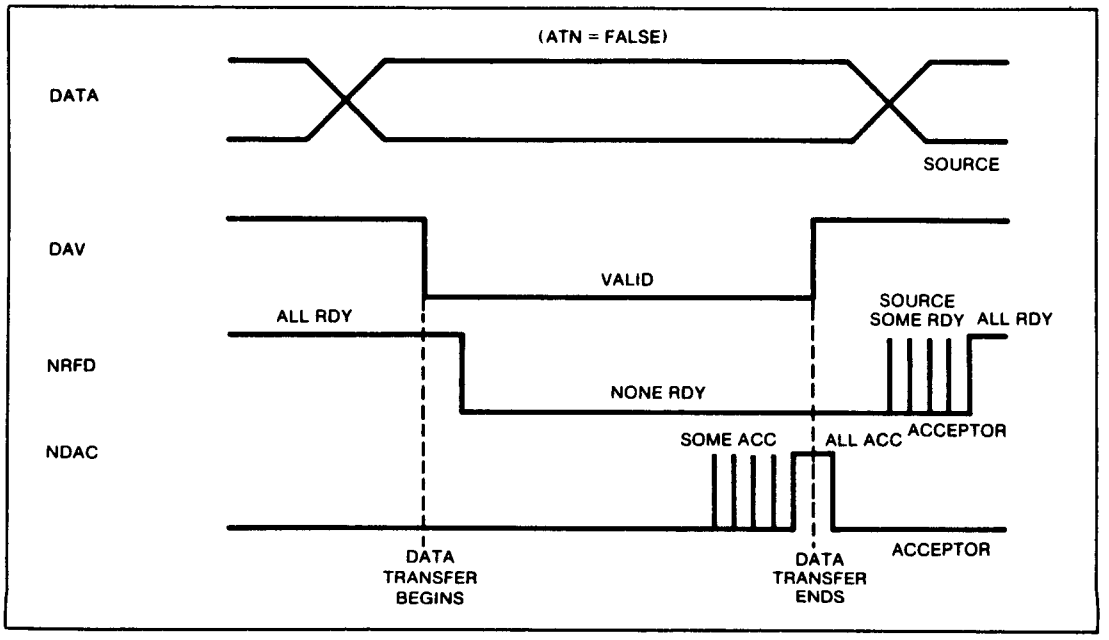


Figure 8-2-3. HP-IB Handshake Timing for One Talker and Multiple Listeners

SYSTEM STATUS SWITCHES (Schematic 2A)

The main use of the system status switch (S701) on the rear panel of the 8175A is in onnection with configuring the instrument on the HP-IB system bus. Only two switch positions are not used for interface-configuration.

Switch element 6 selects whether the self test (ST) routine used for testing some of the functions of the 8175A is to be a normal or an extended one:
(0 = normal ST-mode, 1 = extended ST-mode).

Switch element 7 is used when two 8175A's are to be operated in parallel, to determine which will be the MASTER and which the SLAVE:
(0 = Slave, 1 = Master).

Figure 8-2-4 shows example switch settings and explains the meaning of all of them.

The processor samples the setting of the system status switch only during turn-on by enabling octal buffer U604 via LIS 0. The MPU then writes the HP-IB address and status into the HP-IB controller U702 and decides whether to start the normal or the extended self test mode.

NOTE

Because the processor samples the setting of S701 only during turn-on, later changes of the configuration of S701 will not have an effect on the prior switch setting. Only cycling the power OFF/ON will cause a new reading of the system status switch.

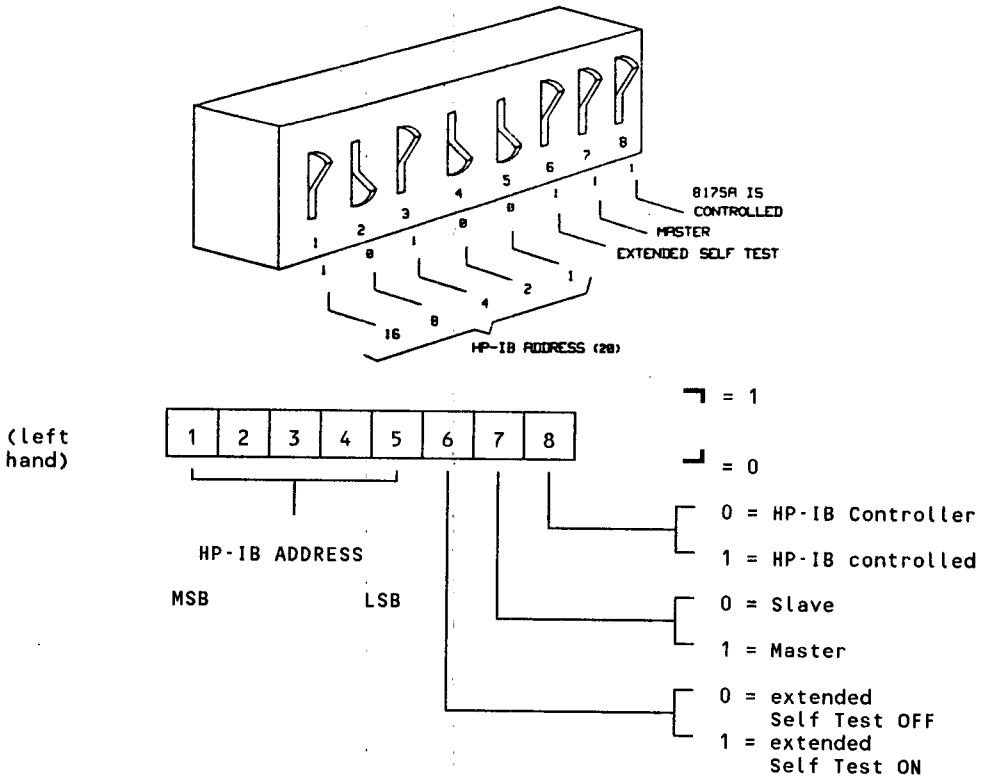


Figure 8-2-4. HP-IB System Status Switch - Settings Explanation

ROM AND ROM-SELECTION (Schematic 2B)

U314 is an addressable demultiplexer which is selected via U315 A,B. By also using the LRA line, address conflicts with the MMU, which must be mapped in this address range, are not possible. HPA13-15 select which of the eight outputs of U314 and therefore which of the eight 16k word * 8 bit program ROMs shall be enabled. HPA0-12 and HPA16 are tied in parallel to the address inputs of all ROMs, except those of U210 which also may be addressed by the Waveform Formatter. This means that the six address inputs (A2-7) of U210 (HF0-HF7) can be delivered by the MPU via U209 when control line CL 8 is low, or by the multiplexers U308, U310 and U312 of the Waveform Formatter when control line CL 9 is high.
NAND gate U315D combines the clock-signal P6N, and the High Read line (HR) to produce the Low Output Enable ROM signal LOER, used to activate the output buffers of the selected ROM and to read data information on the bi-directional data bus HDRW0-7.

WAVEFORM FORMATTER (Schematic 2B)

Basically, the Waveform Formatter is responsible for taking the output data information from the 8175A, and generating waveform display symbols on the graphic part of the screen. The hardware portion of the Formatter generates addresses that are referenced to four, 256-byte look-up tables in the so called Formatter ROM U210. The Formatter ROM then outputs the proper waveform symbol, that means either a high or low level or an edge. The Formatter is used to increase the waveform display update rate.

When a waveform display is requested by the user, the processor clocks the output data stored in RAM into the octal D-flip-flops U309, U311 and U313. By enabling the multiplexer U308, U310 and U312 with control line CL 9 (U322D/9) high and, at the same time disabling the octal buffer U209 via CL 8 (U209/1,19) high, the processor allows the Waveform Formatter to address the Formatter ROM U210. Then, according to the users choice of number of channels to be processed and the selected time per division on the screen, the processor will address a look up table stored in U210, and set the multiplexers to mask out the non-effective bits. The addressed look-up table then samples the data from the Waveform Formatter (HF0-5 and HPA0-1) and generates the proper waveform display symbols. The processor then reads this display information out of the U210 and stores it into the dynamic RAM. From here, it is routed later through the octal graphics buffer U611, and shifted out of the display data shift register U612, to the display (Schematic 2D).

STATIC RAM, STATIC RAM-SELECTION AND BATTERY-BACKUP (Schematic 2B)

Addresses HPA0-17 are used to address a single byte in the four 8K word * 8 bit RAMs U 212..U 215 used in the 8175A. HPA0-12 are tied in parallel to all thirteen address inputs of the RAMs. HPA13-15 are used to select the four used outputs of the demultiplexer U 216 which is addressed via HPA16 and HPA17.
The operation this block is dependent upon the state of the two signals HPSV and VBAT delivered from the power supply board. Their status can be explained as follows:

(1) **Normal operating mode:**
VBAT is driven near to the +5 V rail via a transistor on the PSU Board. This means that the battery is disconnected from the VBAT line and is charging through R 709.
HPSV is active high, therefore the four outputs of U216 pass through transistor array U 217 without effect on their logic level.

(2) **Battery Backup mode:**
When the +5 V rail drops below 4.75 V, the transistor on PSU Board which drives VBAT, switches off and the potential on this line begins to fall until it reaches the level of the battery voltage. At this moment the battery is made available to the RAMs via the transistors of U717. Thus the Vcc input of the four RAMs is never allowed to deteriorate far enough for the contents to become corrupted or lost.
HPSV simultaniously goes to the low state and therefore the transistors of U217 go to the off state. This means the potential on the low active CS-inputs off the RAMs are pulled to the battery voltage, and therefore no access is possible.

There are two further control signals used for the static RAMs:
Low Output Enable Static RAM (LOESR), derived from clock signal P6N and the High Read signal (HR), is used to read data to the data bus HDRW0-7.
Low Write Enable Static RAM, (LWESR) derived from clock signal P4N and the High Write signal (HW), is used to write data from the data bus HDRW0-7 into the RAMs.
Because HW is the complement signal of HR, at any one time only one of the two signals can be active low.

DYNAMIC RAM (Schematic 2D)

The CPU board uses eight 64K word * 1 bit dynamic RAMs U 406-413. Data input and output of these RAMs are separated. Therefore octal buffer U 504 is used to write data from the bi-directional data bus HDRW0-7, whereas octal D-flip-flop U 505 and octal buffer U506, are used for reading data from the dynamic RAM to HDRW0-7.

To select one specific location, sixteen address bits must be supplied. Because only eight address pins are available, this information must be delivered in two steps using two eight to four bit multiplexers for each device communicating with dynamic RAMs:
U316-317 for the MPU itself
U607-609 for the full-field scanning generator
U414-415 for the CRT controller U416

The Address Multiplexing Select (AMS) line (U716B/5) is connected to all six multiplexers and is used to switch between the two address-bytes. To avoid addressing conflicts between these three devices, the outputs of each multiplexer pair is enabled by a separate signal:

Low Enable MPU Addressing (LEMA) is active while the MPU addresses the dynamic RAM for read or write.

Low Enable Full-field Addressing (LEFA) is active

(a) in the graphics mode of the CRT to let the signals of the full-field scanning generator address the RAM.

(b) during each retrace period assuring that each of the 128 contiguous row addresses of the RAMs is selected within a 2 ms interval to provide RAM refreshing.

Low Enable CRTC Addressing (LECA) is active in the alphanumeric mode. Then the CRT controller reads data out of the dynamic RAM to display it on the CRT.

The RAMs require three external control signals LWEDR, LRAS and LCAS in order to insure proper data transfers:

Low Write Enable Dynamic RAM (LWEDR) distinguishs between read and write operations. It is generated by NAND gate U405A from timing information (P2N,P5N) and the high write line (HW).

Low Row Address Strobe (LRAS). The falling edge is used to strobe the row address information into the RAMs.

Low Column Address Strobe (LCAS). The falling edge is used to signalize a stable column address, the low state enables the output buffers of the RAMs and the rising edge latches this data byte into the octal D-Latch U 505.

TIMING CONTROL FOR DYNAMIC RAM (Schematic 2C)

The 40 MHz master clock from Y 701 and the 20 MHz output of U 716E are used to transform several timing phases via the gating action of AND-OR-INVERTER U711, DUAL-FLIP-FLOP U713, NOR gate U714 and seven flip-flops of octal D-flip-flop U716 into the three timing signals LRAS, LCAS and AMS used for dynamic RAM data transfers.

Address Multiplexer Select (AMS) signal lags LRAS by 25 ns, and is used to switch between the two bytes of RAM address information delivered by each device (MPU, graphics Counter or CRTC) communicating with the dynamic RAM.

The Low active Row and Column Address Strobes LRAS and LCAS, are needed during read, write and page mode read cycles of dynamic RAM, to latch the apprpopriate address information into the RAMs and to enable (with LCAS low) the output buffers of the RAMs.

Figure 8-2-5 shows the timing waveform relationships of these signals and demonstrates that during each processor cycle, three data bytes are latched into U505 to form the HRAD bus (schematic 2D):

while LEMA is active (MPU access), only one byte (named Dn or Dn+3) is latched into U505.
while LEFA or LECA is active (scanning counter or CRTC access) two bytes (named Dn+1,Dn+2 or Dn+4,Dn+5) are read from RAM in (because LRAS doesn't change) a so called 'page read mode' and latched into U505.

Figure 8-2-6 shows which bytes of this HRAD information is used by the character ROM or the graphics buffer and how the output of those devices it serialized by U612 (schematic 2D):

in graphics mode, the output of U611 is enabled via LGBE therefore the whole HRAD bus information reaches the data shift register. The timing of High Load Data shift Register (HLDR) ensures that only the two CRT-Info bytes are loaded into the shift register, serialized and send to the CRT.

in alpha-numeric mode OCTAL D-REGISTER U507 only captures the second byte of the CRT-Info. Because timing signal P1 is changing from high to low while U507 holds CHD0-7 constant, two bytes are leaving the character ROM. As in the graphic mode, the data shift register then loads and serializes them into the sixteen bits needed for one column of a character.

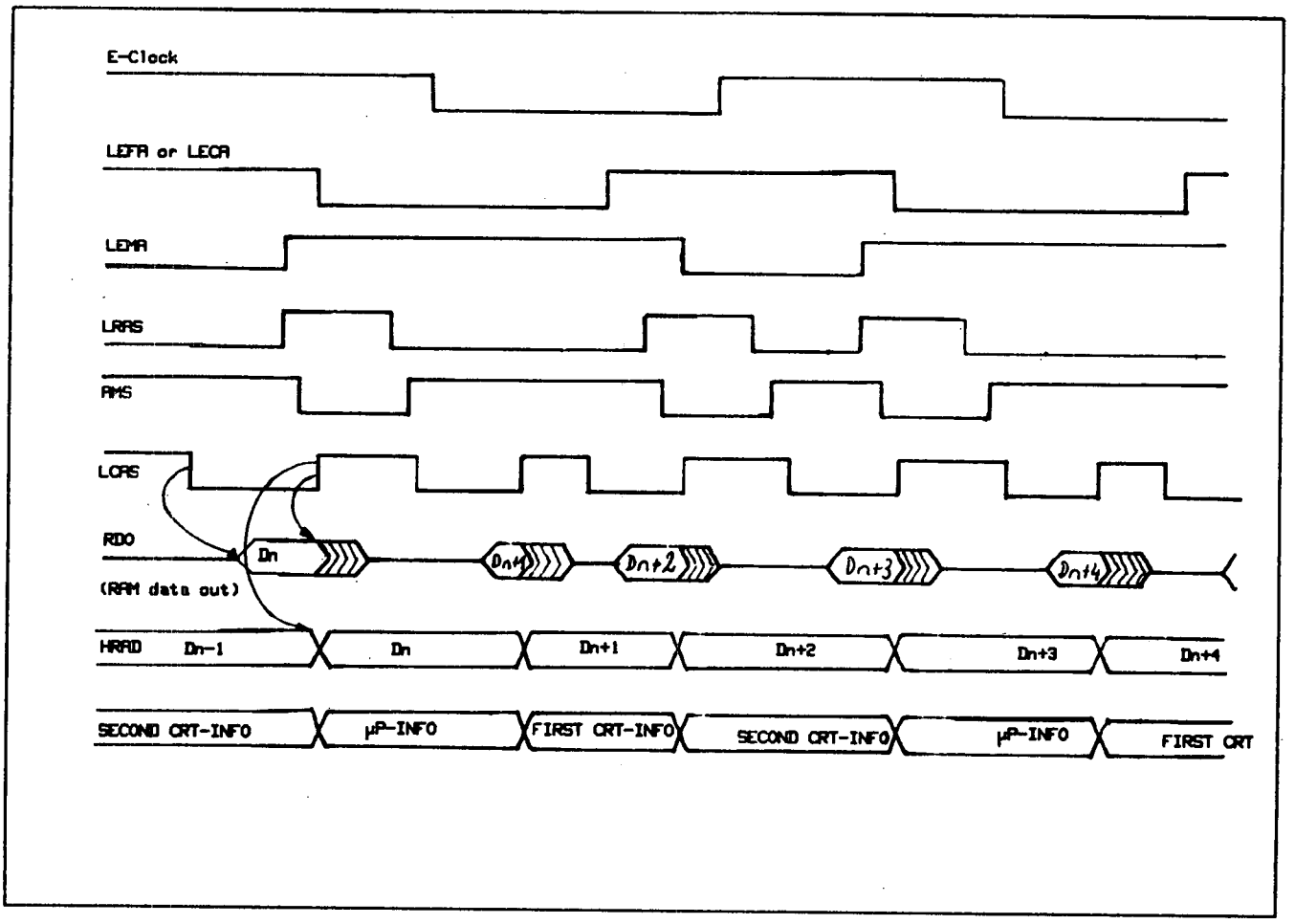


Figure 8-2-5. Dynamic Ram Timing Waveform Relationships

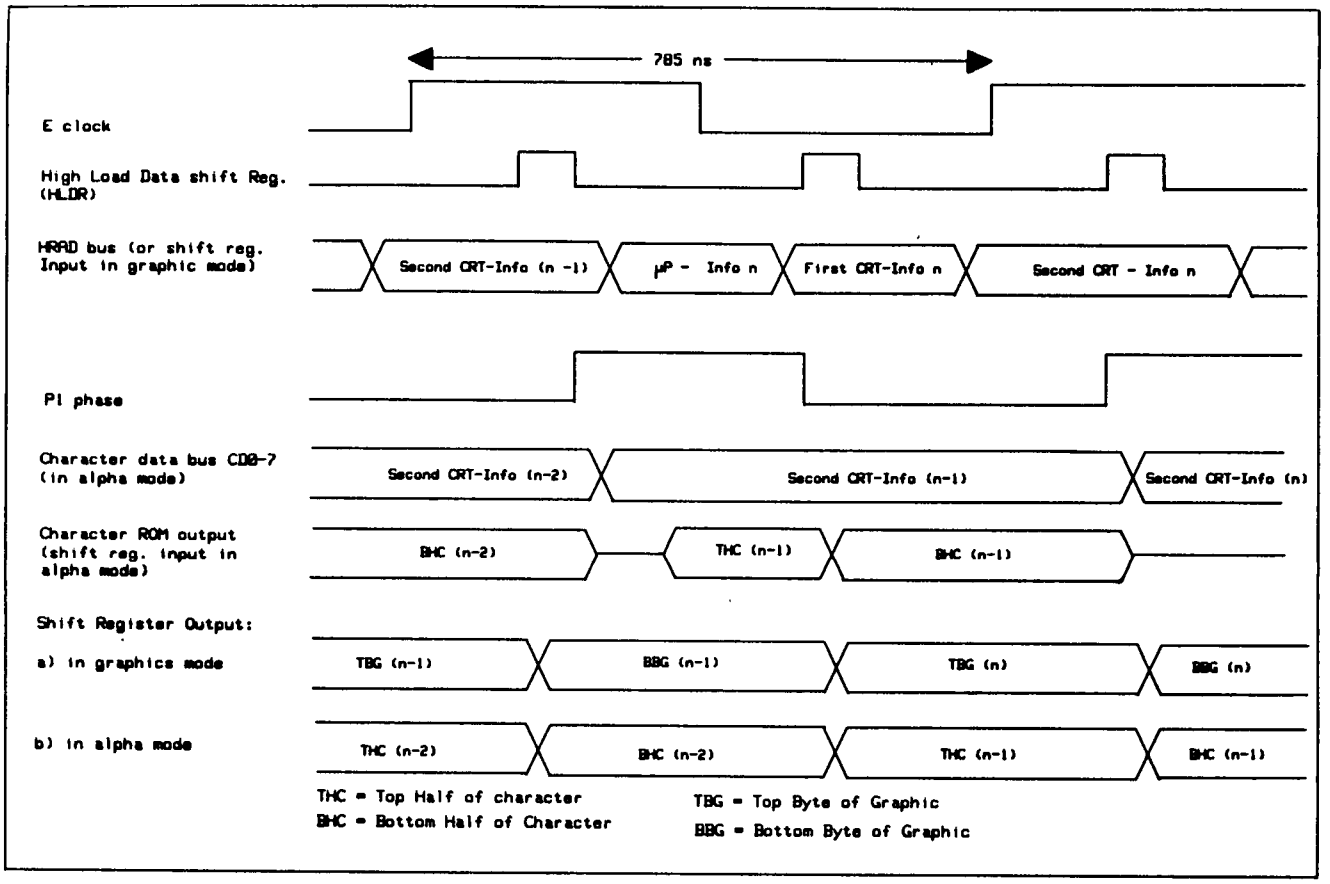


Figure 8-2-6. HRAD Bytes Utilization (ROM or Graphics Buffer)

FULL-FIELD SCANNING COUNTER (Schematic 2C)

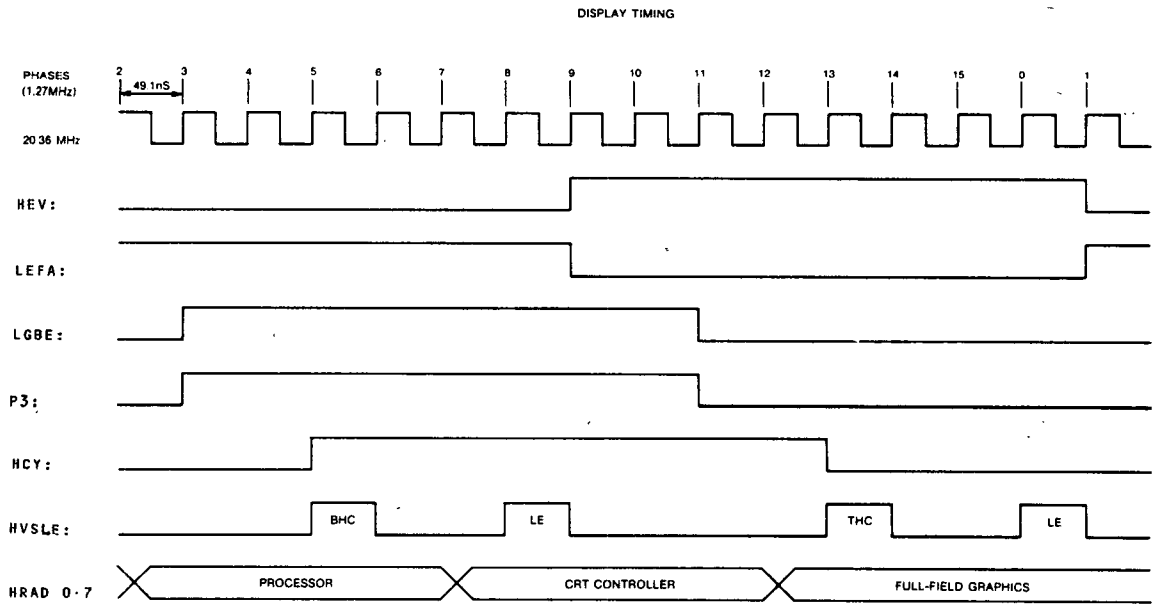
The full-field scanning counter provides scanning information necessary to display graphics in the 16K bit graphics area (512 x 256 bit) shown in Figure 8-2-9. Display timing waveforms are given in Figure 8-2- 7.

Scanning of the full-field graphics display area is done with five binary counters that are cascaded together in a ripple carry configuration. The vertical sweep speed is provided by the high speed Y counter U 608-A,B which is clocked by P5. Therefore, in graphic mode every 800 ns a 'page mode read' occurs and sixteen data bits are transferred to the CRT. The low speed X counter that produces the horizontal frame frequency of 60 Hz is realized with U 610-A,B and U 606 and is clocked via the output Y9 of U 608-B/10.

The Display Enable (DE) output of the CRT controller (U416/18) generates the three signals HCY, HCX and LLX which control the two counter groups:

During the long retrace time at the end of a frame, DE is inactive low. That means the two inverting outputs of DUAL-FLIP-FLOP U 616-A,B deliver a high. At the beginning of the new frame, DE is set high thereby activating the two clear signals HCY and HCX and the signal Low Load X counter (LLX) which presets U 606 to 07 hex. The next rising edge of P3N clocks the high state of DE into U 616B and inactivates HCY to low so that U 608A,B is able to count up. As the output Y8 of U 608B reaches high state, the LLX and the HCX signals also are inactivated and the X counter is now able to count up.

DE also is inactive during the short column retrace period, but that is only captured by U 616B because this flip-flop is clocked with 1.27 MHz signal P3N. U 616A doesn't see this low state of DE because there is no rising edge of Y8 during column retrace time. That means at the beginning of the next columns only HCY is activated.



HEV: ENABLE VIDEO (U510/10)
LEFA: LOAD CHARACTER ROM ADDRESS LATCH/ENABLE FULL FIELD DISPLAY (U507/1)
LGBE: GRAPHICS OUTPUT BUFFER ENABLE (U611/1,19)
P3: INCREMENT CRT CONTROLLER ADDRESS COUNTER (U416/21)
HCY: CLEAR "Y" COUNTER (U608/12,2)
HVSLE: VIDEO SHIFT REGISTER LOAD ENABLE (U612/1)
BHC: BOTTOM HALF OF CHARACTER
THC: TOP HALF OF CHARACTER
LE: LOAD ENABLE
HRAD 0-7 RAM DATA LATCH OUTPUT (U505)

Figure 8-2-7. Display Timing Waveforms For One MPU Cycle

CRT CONTROL (Schematic 2D)

This system uses the vertical scanning method to display information. With this type of scanning, the electron beam scans from top to bottom and from left to right. After each vertical scan the beam is moved horizontally to display another 23 characters. The non-interlace-mode is the type of raster scanning used. This means that one field per frame is scanned before the electron beam is returned to the top left hand corner of the display.

For resolution, the characters generated on a frame must be continually repeated in order to display them on the CRT. The character code stored in ROM and loaded in RAM is in ASCII and must be converted for use on the CRT. Since ASCII characters cannot be directly displayed, a character ROM (U508) is used to convert the ASCII codes into the 9*16 dot pattern used to generate characters. See Figure 8-2-8 for a typical dot pattern for a character.

CRT CONTROLLER (CRTC) OPERATION (Schematic 2D)

The CRTC is the interface between the MPU and the display system. The CRTC (U416) contains nineteen programmable registers. These registers are initialized by the processor via the HDRW0-7 data-bus. The MPU configures the CRTC to generate horizontal and vertical sync. raster addresses for the character ROM, a curser asserted signal. However, there are several control inputs whose signal contribute to the initialization process. These are described in the following paragraphs.

CRTC INTERFACING

The bi-directional data-bus HDRW0-7 is used for data transfer between the MPU and one of the internal registers of the CRTC. The high read/low write (HR) line U416/22 is used to determine whether a register is written to or read from. The register selected is determined by the state of HPA0 that is tied to the register select (RS) line U416/24. When HPA0 is low the address register is selected. When HPA0 is high, one of the data registers can be accessed. The enable (E) input U416/23 is used to clock data to or from the data input/output buffers.

The clock (CLK) input U416/21 is used mainly to synchronize the horizontal sync. register. The clock rate input is equal to the character rate of 1.27 MHz.

The low master reset (LMR) line is tied to the reset input (RES) of the CRTC (U416/2). When a low level is on this line, the CRTC is forced into the following state:

a) The display operation stops and all CRTC counters are cleared.

b) All outputs go low.

c) The control register remain unchanged and unaffected.

HORIZONTAL AND VERTICAL SYNC.

The sync. signals are generated by the CRTC timing registers. The horizontal registers are programmed in character time (785.79ns) units with respect to the left most displayed character. Note, that the horizontal sync. signal (HSYNC) from the CRTC U416/39 is NANDed (U509D) with the control latch bit 2 (CL2) signal. CL2 will go high when the processor is finished initializing the CRTC. The HSYNC signal then becomes the vertical sync. signal (HVSYNC) for the display driver board. The CRTC's vertical sync. timing registers are programmed in character line time (27.5 us) and are referenced to the top character position. Note, that the vertical sync. signal (VSYNC) from the CRTC (U416/40) becomes the horizontal sync. signal (HHSYNC) for the display driver board. See Figure 8-2-7 for the timing relationships of these signals.

DISPLAY ENABLE AND CURSER OUTPUTS

Display enable (DE) U416/18 is an active high output that indicates that addressing in the active display area is being provided by the CRTC. The curser (CUR) output signal to U510/7 is determined by the initialization of the CRTC curser registers U416/19. CUR is an active high signal that is exclusive-ORed (U613C) with HRAD7 to provide inverse/non-inverse display blinking on a character.

RAM ADDRESSING

The 14 memory addresses, MA0-13 (U416/4-17), from the CRTC are multiplexed together by U414 and U415 and used to addressed a 16K byte segment of dynamic RAM. The combination of the CL4 and CL5 inputs to U415/3,6 determine which 16K byte segment of RAM is available to the CRTC.

CL5	CL4	kilo byte segment
0	0	0 - 15
0	1	16 - 31
1	0	32 - 47
1	1	48 - 63

RASTER ADDRESSES

The CRTC provides 4 outputs, RA0-3, to be used by the character ROM U508 as the column address (1 of 9) for a character. In other words, RA0-3 position the character ROM so, that the correct character dots are displayed in the correct location on the raster.

CHARACTER GENERATION (Schematic 2D)

The circuitry responsible for the final processing of a character is the character ROM U508, graphics output buffer U611, the display data shift register U612, display control circuitry, and the display data latches U512A,B.

CHARACTER ROM

The 12-bit character ROM address consists of a 7-bit binary ASCII code (CHD0-6) that represents a standard symbol, ie, a letter, number, or a symbol. Also, a column address (HRA0-3) that corresponds to the dot column that is to be output, and a timing qualifier, P1. When character ROM U508 is enabled by LCRE (U508/18) and the output of AND gate U509A/3 is low, the proper 8 dot segment for a given character is output to the display data shift register. A dot represents one logical bit.

The dot matrix size for each character is 9 dots wide by 16 dots high. The following is an example of how a single character is displayed on the CRT.
Note, that there are 23 characters to a character column on the raster (refer to Figure 8-2-9). The output dot sequence for a character is in 8 dot segments from top to bottom, left to right. The character ROM outputs the first 8 bits to the shift register U612. While U612 serializes these, The timing signal P1 (18 2C) changes its state. That means, the address of ROM U508 changes and a second byte is output to U612. After serialization by U612, This byte gives the last 8 dots of the first column of our character - A

Now, with the column address remaiming unchanged, the sequence is repeated by applying the next 22 character codes to the ROM address inputs, and whereby filling the whole column of the CRT. After the following retrace period, the CRTC delivers the next column address HRA0-3. That means, now the second column of all 23 characters is written to the screen. This is done 9 times for each character. Thus, the 9*16 characters dot pattern. Note, that a high from U508 is equal to a dot being on. See Figure 8-2-8, for a typical dot pattern.

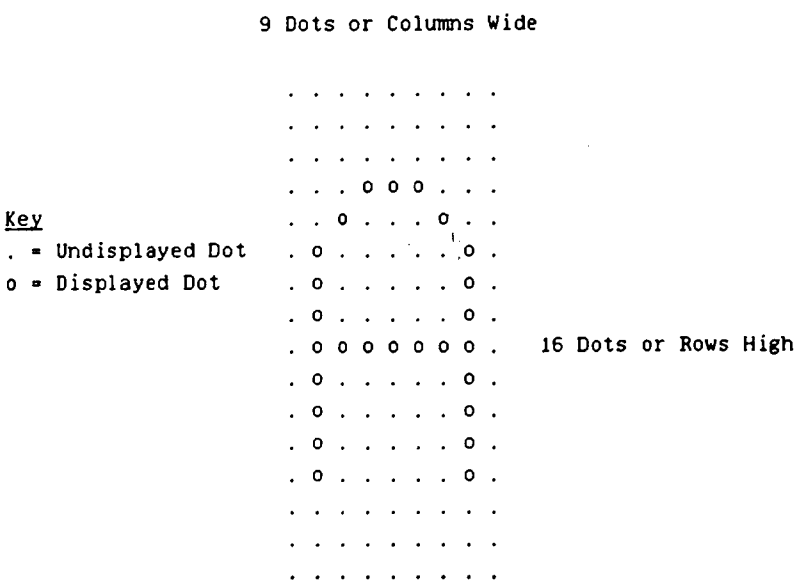


Figure 8-2-8 . A Typical 9x16 Dot Pattern For a Character

DISPLAY DATA SHIFT REGISTER

This device is responsible for converting parallel display information into a serial data stream. U612 can be configured for either shift left or parallel loading operations. This is determined by the level on pin 1 (HVSLE)

GRAPHICS OUTPUT BUFFER

While in the graphics mode, the character ROM (U508) is disabled and U611 is enabled. Graphic information (GD0-7) is then loaded into U612 and displayed in the full-field graphics display area.

DISPLAY DATA LATCHES

The display data latches U512A,B provide the video data for the display driver board. These latches are clocked at 20 MHz making a 50 ns dot rate. Quad D-flip-flop U510 provides timing for the curser and enables the video brightness circuitry realized with NAND gates U511A,C. The following is the output of U512A,B, which is the truth table for video information.

HFB	HHB	Video Output
0	0	OFF
0	1	Half-Bright
1	0	Full-Bright
1	1	Full-Bright

DISPLAY CONTROL (Schematic 2C)

This circuitry is responsible for controlling display operations. Via the static Control Line 3 (CL 3) 57 2A, the MPU selects between the alpha-numeric only mode (CL 3 low) and the alpha-numeric/graphic mixed mode (CL 3 high):

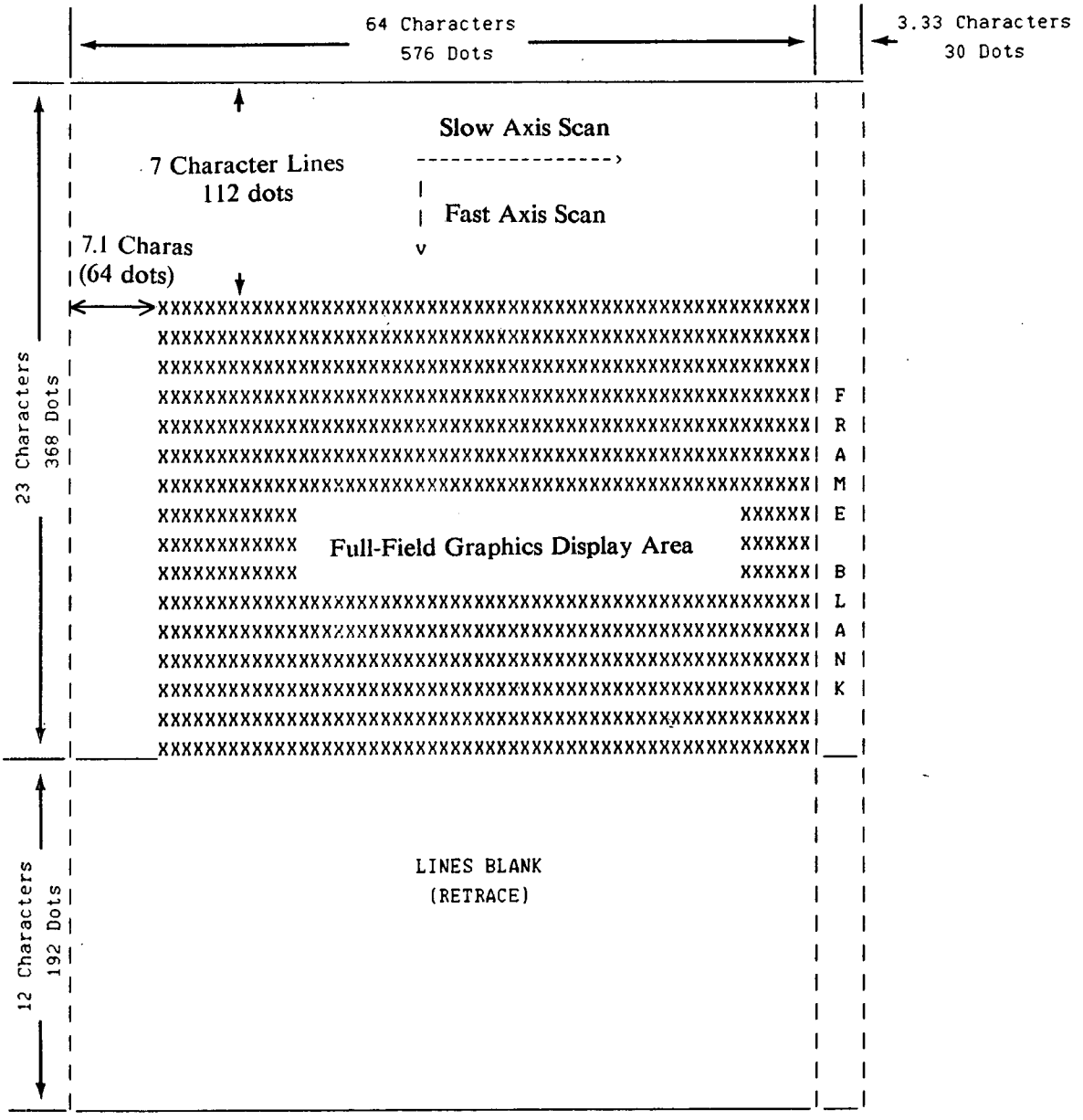
(A) Alpha-numeric only mode

Only the CRT controller is used to display information on the screen. This means that during the active DE cycles, only the two multiplexers U 414 and U 415 belonging to the CRTC are activated via LECA (Low Enable CRTC Addressing) U615/13 and via LCRE (Low Character ROM Enable) U614/8. Only the character ROM U 508 is used as source for the display data shift register U 612.

(B) Alpha-numeric/graphic mixed mode

Both the CRTC and the full-field scanning counter are used to bring information on the screen. By use of the two counter signals Y8 and X9, the display is split into (see Figure 8-2-9):

the alpha-numeric part (7 character rows at the top of the screen and 7.1 character columns at the left) controlled by the CRTC and supported by active LECA and LCRE.
the graphics part at the lower right consisting of 512*256 dots. The full-field scanning counter is enabled to access dynamic RAM through via LEFA (Low Enable Full-Field Addressing) U615D/11 and the data is directed to the data shift register by enabling the graphics output buffer via LGBE (Low Graphic Buffer Enable) U614/9.



Dot Rate:	20.36 MHz	Line Time:	27.503 uS
Dot Time:	49.1 nS	Line Blank Time:	9.43 uS
Character Rate:	1.27 MHz	Frame Rate:	60.0 Hz
Character Time:	785.8 nS	Frame Blank Time:	825 uS
Line Rate:	36.36 KHz		

Figure 8-2-9 Display Character Area

KEYBOARD SCANNING (Schematic 2F)

The keyboard controller, U418, is used to scan the Keyboard and the 4 LED's used on the front panel to indicate the active state of EXT INPUT, TRIG OUTPUT, OUTPUT A and OUTPUT B. U418 is programmed and controlled by the processor for each of these functions.

MPU TO KEYBOARD CONTROLLER INTERFACE

Because the chip select (CS) input U418/22 is tied low, the I/O control section of U 418 is always enabled. To control the data flow between the MPU and several internal registers and buffers of the keyboard controller, the two I/O-select lines LIS A and LIS B are used in conjunction with the address line HPA0 (see table below).

LIS A U418/10	LIS B U418/11	HPA0 U418/21	Function
0	1	0	read status of keyboard controller
0	1	1	read data from keyboard controller
1	0	0	write command to keyboard controll.
1	0	1	write data to keyboard controller

The 1.27 MHz signal P6 is tied to the clock (CLK) input of U 418/3. By programming U 418, this frequency is divided internally to 100 KHz which yields a 5 ms keyboard scan time or a 200/sec scan rate.
The Reset Line (RST) U418/9 is tied to the reset logic via the High Master Reset line (HMR).

KEYBOARD SCAN OPERATIONS

The keyboard controller uses the sensor matrix mode for scanning the keyboard: each switch corresponds to a specific location in a 8 bit * 8 bit sensor RAM on U 418. This sensor RAM keeps an image of the state of the switches in the sensor matrix. Scanning the rows of the sensor matrix, or keyboard is done with the combination of the encoded scan lines, SL0-2 (U418/32-34). These lines will count from zero to seven in binary thereby enabling 1 of 8 outputs of demultiplexer U 419. Six outputs of U 419 are connected to the Keyboard Row lines (KBR1-6) of the switches. That means each row, or byte, in the sensor matrix RAM corresponds to a row of switches via a low active line KBR. With each row asserted low, the state of the eight columns in the sensor matrix is sampled via the eight Key-Board Column lines (KBC0-7) and loaded into the respective bit locations of the byte addressed in sensor RAM by the active row.

If a low is sensed on a column line, it indicates a closed switch at the intersection of that row and column in the sensor matrix. If a key-location has changed value, the interrupt request line (HKBI) will go high and stay high at the end of a sensor matrix scan. The processor will service the interrupt and HKBI will go low. See Figure 8-2-10 for the keyboard switch to sensor matrix locations.
In the sensor matrix mode, debouncing of the switches is not done by U418. However, the advantage is that the MPU can determine how long a switch is depressed and use this information for a 'repeat-key'-function.

Byte \ Rows\	Bit Columns KBC7	KBC6	KBC5	KBC4	KBC3	KBC2	KBC1	KBC0
KBR0				row not used				
KBR1			SYS-TEM	CNTRL	TI-MING	OUT-PUT	DATA	PRGM
KBR2		CRSR ←	CRSR ↑	NEXT []	D	E	F	
KBR3		CRSR ↓	CRSR →	PREV []	A	B	C	START
KBR4				.	7	8	9	STOP
KBR5		ROLL ↓	ROLL ↑	DON'T CARE	4	5	6	SINGLE STEP
KBR6	BLUE	EXEC	CLEAR ENTRY	0	1	2	3	DIS-ABLE
KBR7				row not used				

Figure 8-2-10 Keyboard Switch to Sensor Matrix Address Locations (Keys don't exist for blank spaces above)

SCANNING OF FRONT-PANEL LEDS

The keyboard controller also has a 16 word * 8 bit internal display RAM, from which only eight bytes are used. With the internal frequency programmed to 100 KHz, the scan rate of this display RAM is also 200/sec. That means it takes 5 ms until the eight bytes are output via B0-3 and A0-3 outputs of the keyboard controller and the sequence is starting again. The contents of the four lowest bits of this RAM are used to drive the front panel status LED's, see following table:

MSB A 3	A 2	A 1	A 0	B 3	B 2	B 1	LSB B 0
not used	not used	not used	not used	Out B	Out A	Trig Out	Ext. Inp. I

The BD output signal of the keyboard controller inhibits all four LED's while the information on the B0-3 data outputs is changing. When the output data is stable, a high active BD line allows the open collector NAND gates U420 A-D to switch to an active low level on the Key-Board LED lines KBL1-4. The content of the display RAM is arranged in such a manner, that each RAM byte only has one LED on. Therefore, a maximum of one LED current flows through the current limiting resistor R 405 which is connected to the cathodes of all four LED's in parallel.

KEYBOARD SWITCH PAD

The keyboard is a 6*8 matrix consisting of 6 rows labeled KBR1-6 that are enabled one at a time, and 8 columns KBC0-7 that are sampled each row time for a closed switch. From the possible 48 interconnections in this matrix, only 39 are used. This 39 keys are single-pole single-throw switches.
The keyboard also carries the four status LED's used to indicate the active state of the signals:

EXT INPUT, TRIG OUTPUT; OUTPUT A, OUTPUT B

Schematic 2 identifies the components of the Key Board Assy A2.

TIMER (Schematic 2F)

U701 is a Programmable Timer Unit (PTU) U701 which is controlled by an external quartz crystal (Y601) with a frequency of 3.6864 MHz. The PTU delivers the folowing different signals used in the 8175A:

(1) the clock signal Fout for the correspondending interface chip (that means 3.6864 MHz for the standard 8175 A with HPIB-interface and 1.8432 MHz for the option with RS 232C interface)
(2) an interrupt in intervals of 20 ms (HTI1) used by the MPU to wait for or to count the lenght of events.
(3) a real-time clock produced via two 16 bit counters which provide interrupts in intervals of one minute (HTI2) and one day (HTI4).
(4) an interrupt signal derived from the output of an 16 bit counter (HTI3).
(5) a signal source for the piezoelectric beeper U701/38.

The two interrupt signals HTI2-3 are latched with the dual D-flip-flop U 605 and then can be cleared by the MPU in the corresponding interrupt service routine by use of the two static Control Lines CLE and CLF.

To control the data flow between the MPU and several registers and counters of the Programmable Timer Unit, the two I/O-select lines LISD and LISE are used together with the address line HPA0. See following table:

LIS D	LIS E	HPA0	Function
0	1	0	read status of programmable timer
0	1	1	read data from programmable timer
1	0	0	write command to programmable timer
1	0	1	write data to programmable timer

During power up, the PTU is deselected because the chip select input (CS) U701/10 is connected to the High Master Reset (HMR) line. After power up, this line goes inactive therebye enabling the PTU.

DEVICE BUS INTERFACE (Schematic 2E)

The MPU communicates with or controls, the other boards in the 8175A via the Device Bus. This bus consists of address, data and control lines, which change their state only when data is exchanged. Details are as follows:

Data Interface
An eight bit bi-directional Device Data bus (HDD0-7), is derived from HDBRW0-7 data bus. Depending on whether High Read (HR) or its complement High Write (HW) is active, an active High Device Bus (HDB) signal will either enable the OCTAL BUFFER U306, via Low Read Device Data (LRDD) line to read the HDD0-7 bus to the MPU or latch data from HDBRW0-7 bus into OCTAL D-FLIP-FLOP U 304 via High Write Device Data (HWDD). Output enable of U304 is done by High Read/Low Write (HRLW) signal which is derived from the High Write line via NOR gate U 301C/10 and 1 part of OCTAL D-FLIP-FLOP U103.

Address Interface
The Device Interface occupies 1K byte of memory space: the ten lowest address bits HPA0-9 are latched into the two OCTAL D-FLIP-FLOPs U103 and U104 via High Device Bus Address (HDBA) formed by AND gate U403C from address and timing information. This 1K byte address space is now divided into sixteen parts consisting of 64 locations addressed by High Device Address lines (HDA0-5). To quickly address one of these parts, three address lines are decoded into eight Low Card Select (LCS0-7) lines via 1 of 8 DEMULTIPLEXER U101. Each of them selecting one slot in the 8175A (except LCS7, because there are only seven slots). The remaining address line Low Master/High Slave (LMHS) is always pulled active low.

Device Bus Control Lines
Only four control lines handle the Device Bus transactions:
High Control Line 1 and 2
These two lines are identical to the static control signals CLC and CLD (U502/12,15) controlled by the MPU. They are used to select the main functions of the Device Bus

HCL2	HCL1	Function
0	0	enable data bus
0	1	read board code
1	X	not used

Low Read/High Write line (LRHW), used to control the direction of the dataflow :
LRHW low : MPU reads data from the Device Bus
LRHW high: MPU writes data on the Device Bus (Because LRHW and its complement HRLW are derived from HR via OCTAL D-FLIP-FLOP U103, these signals only can change if a new Device Bus operation with a different direction of data flow is started.)
Low Device Bus Valid (LDBV)
This signal is used to synchronize the address and data exchange on the Device Bus. By use of different timing phases for read and write operations (NAND gate U 401-C,D), this signal is only active while all other signals used or derived for the Device Bus are stable. That means, LDBV is the latest signal that goes active and the first one which becomes inactive.

ANALOG CONTROL CIRCUITRY (Schematic 2G)

The Analog circuitry of the processor board consists of:

Three eight bit Digital to Analog Converter (DAC) U202, U204 U206 and related Operational Amplifiers (OP) U 203-A,C,D. These are used to supply reference voltages for BNC- and POD-Threshold and the high level of the TTL/CMOS-POD.

Reference voltage generator U 205 and current booster Q 100. These are used to generate a stable reference voltage which must be adjusted via potentiometer R 102 to exactly 10 V. This voltage is used as reference for the three DAC's, and is also supplied to connector J3 for use by other boards. (Operational Amplifier U 203-B converts it to the -10 V reference.)

Because of its slow speed, the analog circuitry is controlled via the Device Bus Interface:

At initialization, the MPU sets the control line HCL1 68 2E high. Then it selects each slot in the 8175A. That means, the Low Card Enable line (LCEN U300 D,C/12,10) of the different boards are asserted low one after the other. With HCL1 high, the cathode of CR301 (and CR 302 if the processor board contains the RS 232C option) are asserted low by active LCEN whereas, Octal Transceiver U 307 is disabled. In this mode only those data lines connected to the diode(s) are asserted low because the HDD0-7 data bus is pulled up with Resistor Array RA100 (Schematic 2E). The MPU reads this code and after it has scanned all slots, it knows which boards are in the 8175A and under which address it can reach a special board.

After initialization, HCL1 is set low. If the MPU addresses its own slot, LCEN will be asserted low, thereby enabling the Octal Transceiver U 307.

Low Read/High Write (LRHW) line is used to select the desired direction of the dataflow at U 307 and also disables the DAC's in case of a read operation. Because there is more than one DAC, NAND gate U 102-A,B,C is used to select the desired part via a high level on the appropriate address line HDA0-2.

Data write to the selected DAC is then released by the syncronisation signal Low Device Bus Valid (LDBV).

MNEMONICS

Signals on the 8175A CPU board have been assigned mnemonics in alphabetical order that describe the active state and function of the signal. A prefix letter (H, or L) is used to indicate the active state of the signal and the remaining letters indicate its function. A "H" prefix indicates that the function is active in the "high" state; a "L" prefix indicates that the function is active in the "low" state (using positive logic). Table 8-2-4 is a listing of the mnemonics used on the schematics 2A through 2G.

Table 8-2-4. Mnemonics Listing and Explanation

Mnemonic	Description
10VREF	10 Volt Reference voltage supplied by the CPU board.
20MHz	20 MHz clock used to derive the 1.27 MHz clock rates of the control timing circuit. This signal also determines the dot rate for the CRT.
40MHz	40 MHz clock output of the main clock oszillator.
AMS	Address Multiplexer Select. Each functional group able to address the dynamic RAM (MPU,CRTC, or scanning counter) has a related multiplexer pair to isolate it from the other groups and to transform (by use of AMS) the needed sixteen address bits into two 8 bit words sent to the RAMs.
ATN	Attention. Ties to HP-IB ATN line via transceiver. Defines type of data on the interface data bus (addresses/commands or data).
CHD0-6	Character Data 0-6. ASCII code of characters stored in dynamic RAMs and supplied as address to the character ROM for presentation on the CRT.
CHD7	Character Data 7. Selects whether the related character (CHD0-6) shall be displayed in normal or invers video.
CL 0 - CL F	Control Line 0-F. Used by the MPU to control various system functions. See table 3-5-1 for the Control Latch bit assignments.
DAC1-3	Digital to Analog Converter 1-3. Analog output voltages used to control the thresholds of the POD-and BNC-inputs and the high level of TTL/CMOS-POD.
DAV	Data Valid. Ties to the HP-IB DAV line via transceiver chip. Indicates availability and validity of the data on the data bus.
DI0-7	Data Input 0-7. Data inputs of the dynamic RAMs.
DO0-7	Data Output 0-7. Data outputs of the dynamic RAMs.
EOI	End Or Identify. Bi-directional line that ties to the HP-IB EOI line via transceiver. Indicates end of data transfer or identifies initiation of polling operation.

Mnemonic	Description
FCONT	Frequency of Controller. Output signal of the programmable timer derived from 3.6864 MHz quartz. Used in the standard version for the HP-IB interface controller (FCONT = 3.6864 MHz) [or in the option version of the 8175 A for the RS 232C controller (FCONT = 1.8432 MHz)].
HCL1-2	High Control Line 1-2. Used to control the main functions of the device bus. Identical to control lines CL C and CL D.
HIBI	High Interface Bus Interrupt. Used to signalize the processor a request of the interface chip if the signal can pass the interrupt mask.
HCX	High Clear X. Used to clear the X counter for the graphics area at the beginning of a new frame.
HCY	High Clear Y. Used to clear the Y counter for the graphics area at the beginning of a new line.
HDA0-5	High Device Bus Address 0-5. Static address bus used to select 1 of 64 locations on the board enabled by the active LCS line during a device bus operation.
HDB	High Device Bus. Derived from address information to signal an MPU operation concerning the device bus.
HDBA	High Device Bus Address. Used to latch address information if the CPU communicates via the device bus.
HDBI	High Device Bus Interrupt. Used to signalize the processor a request from any other board (if the signal can pass the interrupt mask).
HDBRW0-7	High Buffered Data Read/Write 0-7. Bi-directional data bus derived from HDRW0-7 by octal buffer for communication between MPU and TTL devices on the CPU board.
HDD0-7	High Device Data 0-7. Bi-directional data bus used for communications between MPU and the other boards or the analog control circuit on the CPU board itself.
HDRAM	High Dynamic RAM. Derived from address information if the MPU accesses the dynamic RAM.
HDRW0-7	High Data Read/Write 0-7. Bi-directional data bus used beetween MPU and the high impedance devices on the CPU board.
HEV	High Enable Video.
HF0-5	High Formatter 0-5. Waveform information from the waveform formatter used to address the formatter ROM.

Mnemonic	Description
HFB	High Full Bright. The combination of this signal and the HHB signal detrmines the brilliance of the video displayed.
HHB	High Half Bright. The combination of this signal and the HFB signal determines the brilliance of the video displayed.
HHSYNC	High Horizontal SYNC. Used by the display driver board.
HKBI	High Key Board Interrupt. Used to signal the processor an request of the keyboard controller if the signal can pass the interrupt mask.
HMR	High Master Reset. This signal will stay at the acvtive high level for ca. 50 ms after the +5 volt supply exceeds approx. 4.8 volts.
HPA0-20	High Physical Address 0-20. This is the CPU systems Physical Address bus.
HPSV	High Power Supply Valid. Ca. 50 ms after the +5 volt supply exceeds approx. +4.8 volts this signal will become active signalizing stable supply (that means a low level on this line represents the reset mode).
HR	High Read. Indicates a data read operation. Used for devices on the CPU board.
HRA0-3	High Raster Addresses 0-3. Generated by the CRT controller and used by the character ROM as the column address for a character.
HRAD0-7	High RAM Data 0-7. Latched version of the dynamic RAM outputs. Changing three times during each processor cycle because clocked by LCAS.
HRLW	High Read/Low Write. Used to enable the outputs of the device bus data latch during an write operation.
HRS	High Read Static. Static version of the read line. Used for the control section of device bus interface.
HRSI	RS 232C Interrupt. Used to signalize the processor a request of the RS 232C controller (if the signal can pass the interrupt mask).
HTI1-4	High Timer Interrupt 1-4. Used by the programmable timer to signalize different requests to the CPU (if the signals can pass the interrupt mask).
HVSLE	High Video Shift Register load Enable.
HVSYNC	High Vertical SYNC. Used by the display driver board.
HW	High Write. Indicates a data write operation. Used for devices on the CPU board.
HWDD	High Write Device bus Data. Used by the MPU to clock data into the device bus latch for a write operation.

Mnemonic	Description
HWS	High Write Static. Static version of the write line. Used for the control section of device bus interface.
IFC	Interface Clear. Ties to the HP-IB IFC line via transceiver. Places I/O system into known quiescent (idle) state.
KBC0-7	KeyBoard Column 0-7. Return sense line of the keyboard switch matrix to the keyboard controller.
KBL1-4	KeyBoard LED 1-4. Open collector outputs driving the 4 status LEDs related to the BNC-ports on the front panel of the 8175 A.
KBLP	KeyBoard LED Pullup. Connected to the pullup resistor used for the four status LEDs on front panel.
KBR1-6	KeyBoard Row 1-6. Row lines of the keyboard switchmatrix stimulated by the keyboard controller.
LCAS	Low Column Address Strobe. Needed for data transfers with the dynamic RAM.
LCEN	Low Card Enable. The LCEN input of each slot of the 8175 A is connected to a different LCS line. Wherefore this line signalizes an access of the MPU board to the related board (slot).
LCRE	Low Character ROM Enable. Allows an access of the data shift register by character ROM, while the outputs of graphic buffer are disabled via inactive LEGB.
LCS 0-7	Low Card Select 0-7. Selects which slot on the 8175 A is addressed for a data exchange with the MPU (LCS 7 is not used because their are only 7 slots).
LDBV	Low Device Bus Valid. This line is used by the CPU to signalize stable information (data, address) on the 'device bus' used for communication between the CPU and the other boards.
LDRQ	Low Device Bus Request. An open collector line used by the other boards to signalize an request to the CPU.
LECA	Low Enable CRT controller Addressing. Enables the multiplexer pair used by the CRTC to address the dynamic RAM. At this time, the multiplexer pairs of the MPU and the full-field scanning counter are disabled.
LEFA	Low Enable Full-field Addressing. Enables the multiplexer pair used by the fullfield scanning counter to address the dynamic RAM. At this time, the multiplexer pairs of the MPU and the CRTC are disabled.
LEGB	Low Enable Graphic Buffer. Allows access of the data shift register by graphic buffer, while the outputs of the character ROM are disabled by inactive LECR.
LEMA	Low Enable MPU Addressing. Enables the multiplexer pair used by the MPU to address the dynamic RAM. At this time, the multiplexer pairs of the full-field scanning counter and the CRT controller are disabled.

Mnemonic	Description
LIRQ	Low Interrupt Request. Output signal from the interrupt circuitry to the MPU.
LIS 0-F	Low I/O-Strobe 0-F. Signals from the I/O decoder used for read/write or enable operations on the I/O devices on the CPU board. See table for detailed meaning of each strobe line.
LLX	Low Load X counter. Presets the X counter of the fullfield scanning circuitry to 07 hex.
LMHS	Low Master/High Slave. Address signal of the Device Bus which is always active low in the 8175 A.
LMR	Low Master Reset. This signal will stay at the acvtive low level for ca. 50 ms after the +5 volt supply exceeds approx. 4.8 volts.
LOER	Low Output Enable ROM. Used to enable the output buffers of the selected 1 of 8 ROMs during a read operation.
LOESR	Low Output Enable Static RAM. Used to enable the output buffer of the selected 1 of 4 static RAMs during a read operation.
LRA	Low Register Access. If address inputs A11-15 of the MMU are all ones, this signal will indicate an processor-access to the MMUs register.
LRAS	Low Address Strobe. Needed for data transfers with the dynamic RAM.
LRDD	Low Read Device bus Data. Used to read data from the Device Bus to the MPU.
LRHW	Low Read/High Write. Used to signalize the direction of the device bus data-flow.
LWEDR	Low Write Enable Dynamic RAM. Active if the MPU writes into the dynamic RAMs (CRTC and graphic counter can only read from the dynamic RAM).
LWESR	Low Write Enable Static RAM. Active if the MPU writes into the static RAMs.
NDAC	Not Data Accepted..HP-IB handshake line indicating acceptance of data by all devices.
NRFD	Not Ready For Data. HP-IB handshake line indicating that devices are ready to accept data.
P0-P7	Phase 0-7. Each phase is a 1.27 MHz signal from the control timing circuit. Adjacent phases are separated by 50 ns (e.g. P2 lags P1 by 50 ns).
P0N-P7N	Phase 0-7 Not. Complement of the P0-P7 signals.

Mnemonic	Description
REN	Remote Enable. Ties to the HP-IB REN line via transceiver. Enables alternate devices to provide programming data.
SRQ	Service Request. Ties to the HP-IB SRQ line via transceiver. Indicates a need for service; causes an interrupt of the current sequence to the controller.
VBAT	VBAT. With HPSV high, a transistor located on the power supply board of the 8175 A supplies approxi-mately + 5V on this line to the static RAMs of the microprocessor board. If HPSV goes low (unvalid), the RAMs are supplied by 2 NiCd-batteries (+2.4 V) placed on the CPU board to provide data retention.
X0-9	X cordinates for full-field graphics display area.
Y4-9	Y cordinates for full-field graphics display area.

BLOCK DIAGRAM CPU BOARD 8175A

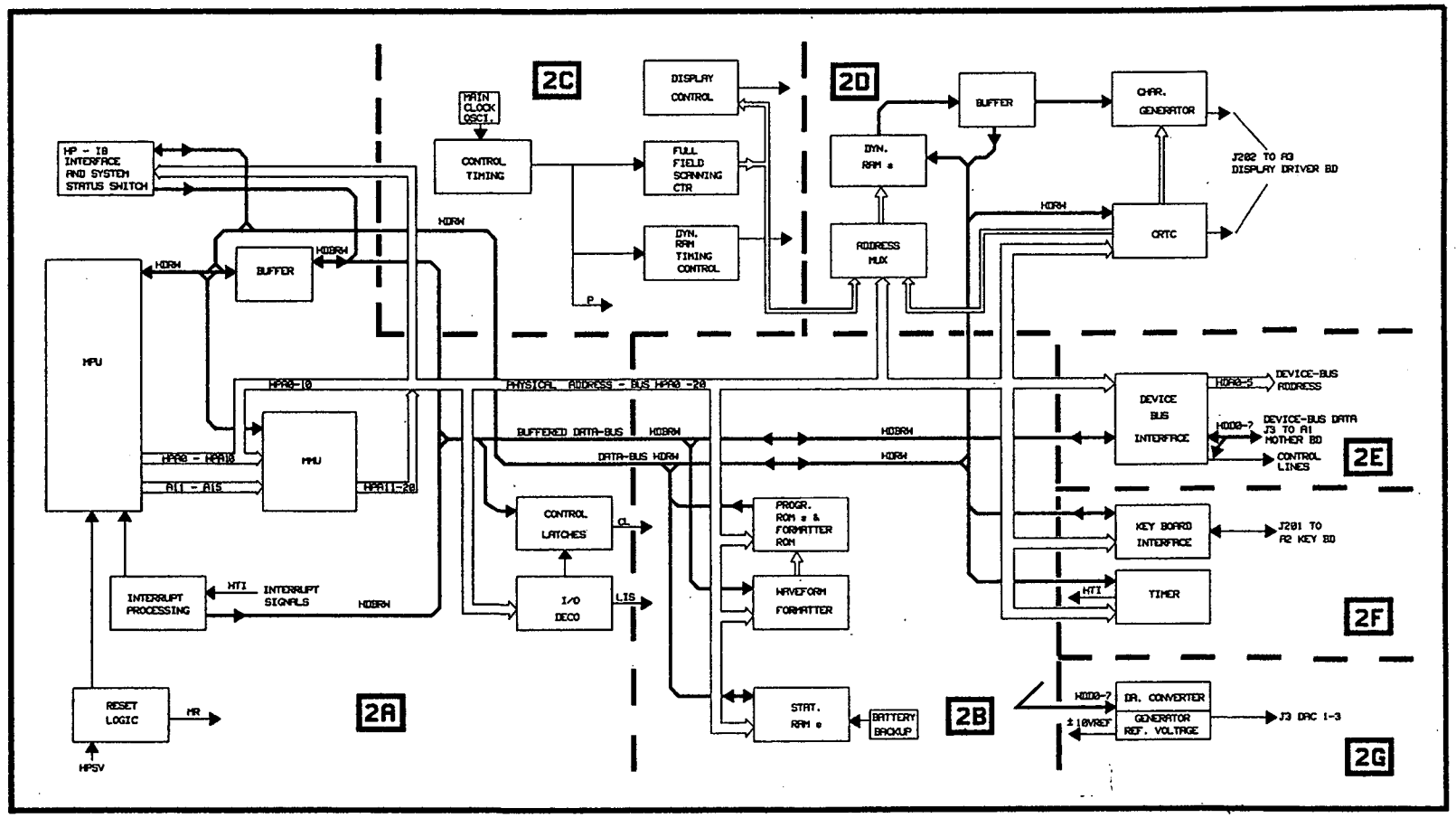


Figure 8-2-1. CPU (Microprocessor) Board Block Diagram

TROUBLESHOOTING

General

Should a fault be isolated to the CPU Board (A20), the theory of operation should be read and understood before proceeding with troubleshooting in this area.

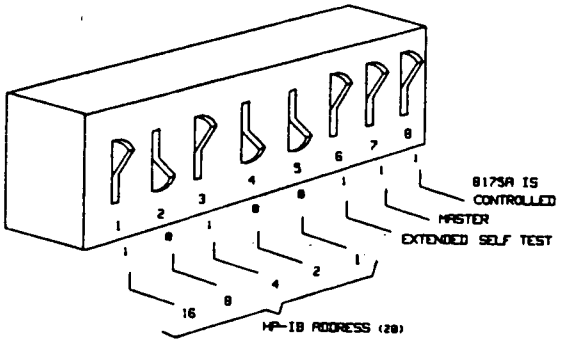
Due to the complexity of the CPU Board, conventional test techniques are used only for some simple checks to determine whether the microprocessor itself is functioning. The main part of the troubleshooting section involves signature analysis techniques which enables verification of correct device operation or malfunction.

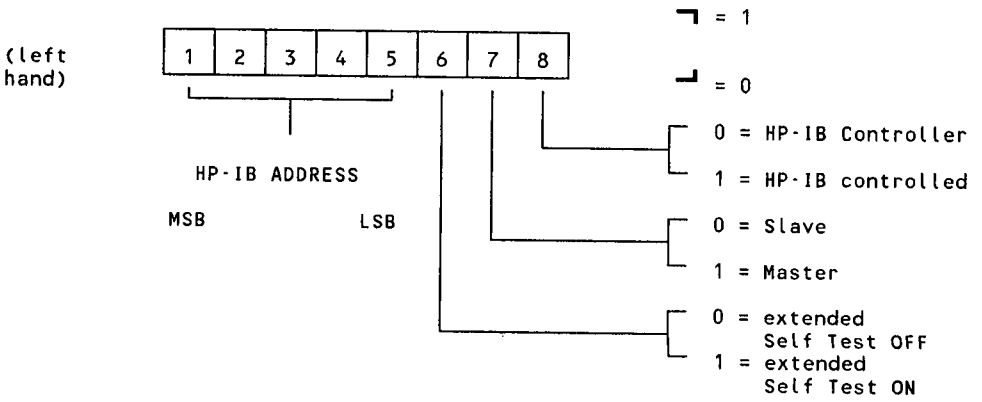
CAUTION

Instrument must not be operated without cover over POWER SUPPLY and FAN AREAS.

Procedure:

With power OFF, disconnect the two ribbon cables from the side of the board, remove the CPU Board (use the board extractors supplied) and plug it into the service (test) connectors. (The connectors are accessed by removing the small cover plate).
Reconnect the cables, ensuring that they are correctly connected.
Set the 8175A HP-IB Status switch as shown below (actual HP-IB address setting is unimportant, since a controller is not used).





Switch power ON. After a few seconds the System Page Configuration menu should be displayed.

1) PRELIMINARY CHECKS

a) First, check with DVM that the Power Supply Voltages and the Reference Voltages at TP's on this board are as follows:

TP	+5V	+5V ±mV
TP	+12V	+12V±mV
TP	+15V	+15V±mV
TP	+15V Video	+15V±mV
TP	-15V	-15V±mV
TP	(Opt.-12V	-12V±mV)
TP	+10V REF	+10V±mV

Confirm with DVM that Battery Voltage at: TP VBAT > 2.6V

With power OFF, confirm that VBAT = approx. 2.4V.
With power ON, connect the DVM in parallel to A20 R709 and measure the voltage (it is dependent upon the charging current)

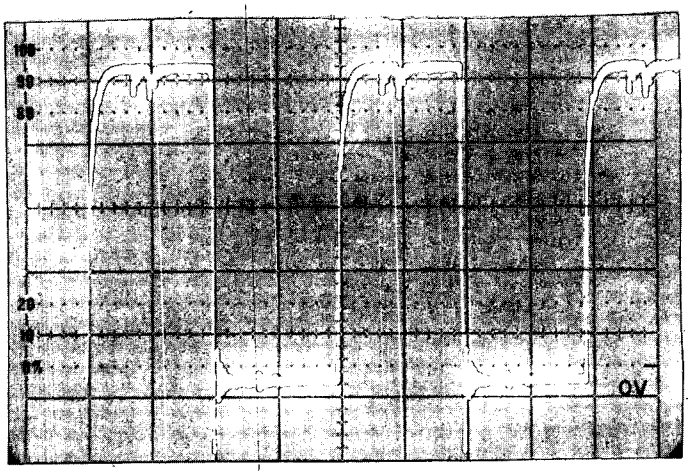
Voltage limit = 1.6V ± 300mV

(By spraying RT 701 with FREON, the current can be reduced to below 0.1mA.)

b) Measure with Scope Probe the MPU clock at TP E

200us/Div

1V/Div



HIL > + 4.4V

LOL < + 0.3V

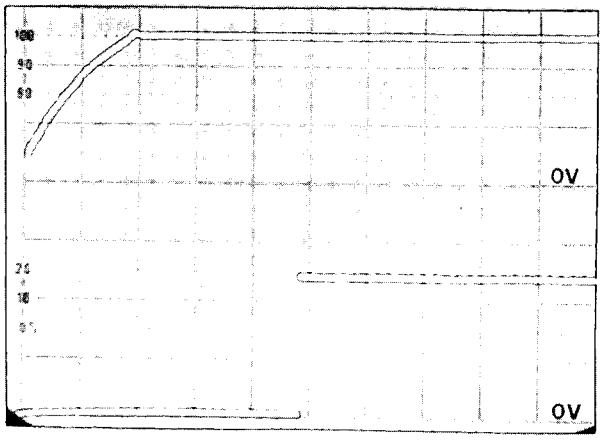
c) Measure the Reset Logic Waveforms HPSU (U321/37), HMR (U322A/1) and LMR (U322A/2) by turning 8175A OFF and ON again. Refer to figure of waveforms below:

20ms/Div
2V/Div

INTERN

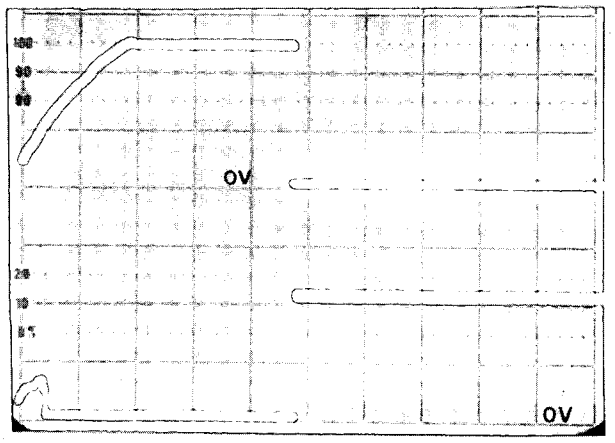
NORM

Trigger A



+5V

HPSU



LMR

HMR

d) Check the IRQ input of the MPU (U321/3) for a TTL High (No interrupt generated!).

2) SIGNATURE ANALYZER TESTS

To do the SA tests, the following two SA Extender Boards are required:
P/N 08175 - 66522 and
08175 - 66523
With power OFF, install the SA Extender Boards:
in place of MPU U321, install MPU ET 08175-66522. Install MPU on ET.
Remove MMU, install 08175-66523.
U318
7c

a) **Control Timing S.A. Test**

Set the switch on the "MMU ET" 08175 - 66522 as shown.

Signature Analyzer setting/connection points on A20 CPU Board:

START	⨍	TP "E"
STOP	⨍	TP "E"
CLOCK	⨍	U715A/3 (20MHz)
⊥		⊥

Note: Verify that reading at +5V is UP73. ✓

Check signatures against Table 8-2-5.

Table 8-2-5. Control Timing SA ✓ 4-19-88 ZC

		Schematics					
Signal Mnemonics	S.A.	2C IC/pin	2A IC/pin	2B IC/pin	2D IC/pin	2E IC/pin	2F IC/pin
P0	1UH1	U710/15			U613/1		
P0N	P1A2	U710/14	U318/16				
P1	0UP8	U710/10			U509/5+2		
P1N	U19C	U710/11; U711/4	U321/35; U417/4		U315/9; U519/9	U403/4	
P2	07U4	U710/7; U615D/12			U405/10		
P2N	U987	U710/6; U711/3	U403/11		U405/1		
P3	03UA	U710/2; U614/11			U416/21		
P3N	UH89	U710/3; U616/11	U709/9				
P4	01UH	U712/15; U711/5,10					
P4N	UU8P	U712/14	U709/10	U105/2	U315/10; U509/1	U403/2; U401/12	
P5	00UP	U712/10; U608/1	U322/13				
P5N	UP8H	U712/11			U405/2	U401/9	(U707/27 optRS232)
P6	8135	U712/7					U418/3
P6N	7U46	U712/6	U709/12	U105/4; U315/13	U405/12		
P7	F1H0	U712/2	U319/11; U320/11; U417/12				
P7N	3UA3	U712/3; U710/13; U711/2					

b) **Dyn. RAM Timing Control SA Test:**

Set the switch on the "MMU-ET" as set for step (a).
Signature Analyzer setting/connection points on A20 CPU Board:

START	∫	TP"E"
STOP	∫	TP"E"
CLOCK	∫	U715A/3 (20 MHz)
⊥		⊥

Check signatures against Table 8-2-6.

Table 8-2-6. Dyn. RAM Control Test SA ✓ 4-14-88 JC

Signal Mnemonic	S.A.	Schematic 2C IC/pin	2D IC/pin	2D IC/pin	2D IC/pin	2D IC/pin
	F612	U711/6				
	UUU0	U711/8				
LRAS	0F1H	U716C/6	U406-U413/4			
AMS	7121	U716B/5	U316/1	U317/1	U414/1	U415/1
LCAS	8764	U716F/15	U406-U413/15			

c) **Address Bus S.A. Test**

Set the switch on the "MMU-ET" as for step (a).

Signature Analyzer settings/connection points on A20 CPU Board:

START	∫	TP "PA20" on "MMU-ET"
STOP	∫	TP "PA20" on "MMU-ET"
CLOCK	\	TP "E"
⊥		⊥

Note: Notice that the gate rate is very slow. Wait until a stable SA is shown. Verify that reading at +5V is 3951. ✓

Check signatures against Table 8-2-7.

Table 8-2-7. Address Bus S.A. ✓ ZC. 4-14-88

MPU U321 pin		S.A.	U319 pin	U320 pin	U318 pin	Address Bus	IC	pin
8	A0	1730	14			HPA0	319	15
9	A1	0H10	7			HPA1		6
10	A2	56UA	13			HPA2		12
11	A3	8HC4	8			HPA3		9
12	A4	UP73		18		HPA4	320	19
13	A5	UUUU		3		HPA5		2
14	A6	U9C9		17		HPA6		16
15	A7	CHUU		4		HPA7		5
16	A8	1209		7		HPA8		6
17	A9	4FCA		13		HPA9		12
18	A10	423H		8		HPA10		9
19	A11	U3A7			6			
20	A12	1238			5			
21	A13	76UF			4			
22	A14	3H5H			3			
23	A15	3214			2			
MMU U318 pin								
40	PA11	U3A7		14		HPA11		15
39	PA12	1238	18			HPA12	319	19
38	PA13	1730	3			HPA13		2
37	PA14	3H5H	17			HPA14		16
36	PA15	3214	4			HPA15		5
35	PA16	76UF				HPA16		
34	PA17	0H10				HPA17		
33	PA18	56UA				HPA18		
32	PA19	8HC4				HPA19		
31	PA20	F722				HPA20	417	3

d) **ROM S.A. Test** SEE MANUAL CHANGE SHEET JAN. 88

Set the switch on the "MMU-ET" 08175-66523 as shown:

Signature Analyzer settings/connection points on A20 CPU Board:

START	↘	both to TP "CS" (ROM pin 20)
STOP	↗ OR ↘	of the ROM which will be measured
CLOCK	↗	U210/22 (LOER)
⊥		U211 PIN 22 ⊥

Note: Verify that reading at +5V is 1180 ✓ 349F

CAUTION

When the START and STOP of Signature Analyzer is changed to the next ROM CS test pin, switch 8175A OFF and ON again.

Check signatures of ROM's against the following table:

ROM S.A.

? UNSTABLE SEE CHG. SHEET.

	IC on schematic 2B							
pin	U210 S.A.	U211 S.A.	U106 S.A.	U107 S.A.	U108 S.A.	U109 S.A.	U110 S.A.	U111 S.A.
11	48C2	F931	A2H5	82A1	65UP	01A3	H044	036C
12	4704	A636	21U3	38HH	PA63	9P01	6456	84CP
13	0U05	C496	53H3	373H	66HC	89F4	462A	5F40
15	F0H6	5U20	2563	C1AC	C16P	P4P0	569C	PAS4
16	2353	847P	6FFC	73AF	H3F2	1119	6U95	F446
17	F01F	H4P1	9PSP	2C32	19U7	H424	150A	2038
18	9P9A	F7A3	1F29	U911	6F39	994H	FSP5	90F8
19	257F	P2A2	7325	17UC	UH6F	P672	257P	8AUC

e) **CRT Address Lines S.A. Test**

Set the switch on "MMU-ET" 08175-66523 as shown:

Signature Analyzer settings/connection points on A20 CPU Board:

START	↘	TP "PA20" on MMU-ET
STOP	↗	TP "PA20" on MMU-ET
CLOCK	↗	TP "E"
⊥		⊥

Note: Verify that reading at +5V is UP73.

Check signatures of dyn. RAM Address MUX against Table 8-2-8. ✓ 4-15-88 ZC

Table 8-2-8. CRT Address Lines SA

U414 pin	S.A.	U415 pin	S.A.
15	UP73	15	UP73
4	FA93	4	7C87
7	UP8H	7	2494
9	U165	9	C6F5
12	FH3F	12	U121

f) **HDBRW Data Bus Test**

Set the switch on "MMU-ET" 08175-66523 as shown:

Note: The beeper will output a pulsed tone!

Referring to the following list and photographs: REAR PANEL HPIB SWITCH
Set switch element 1 of S701 to HIGH then:
Measure with scope probe the signal at U604/12. It should be as shown on the photos.
Set switch back to low position, waveform should be as shown on the photos. Repeat same procedure for each switch element, measuring waveform at correspondending IC pin.

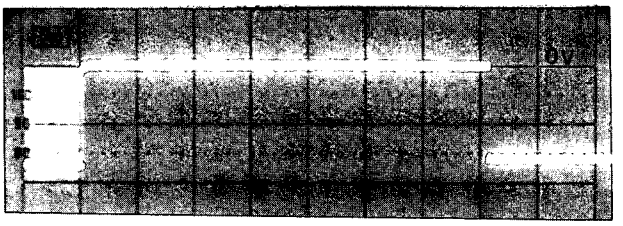
Switch Element		SEE PHOTO PG. 8-85	IC pin number
S701	1	in position high	U604/12
S701	2	in position high	U604/16
S701	3	in position high	U604/3
S701	4	in position high	U604/7
S701	5	in position high	U604/9
S701	6	in position high	U604/18
S701	7	in position high	U604/5
S701	8	in position high	U604/14

100us/Div

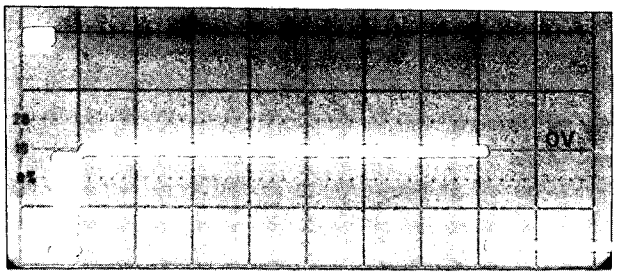
1V/Div

for U604/12,16,5,14

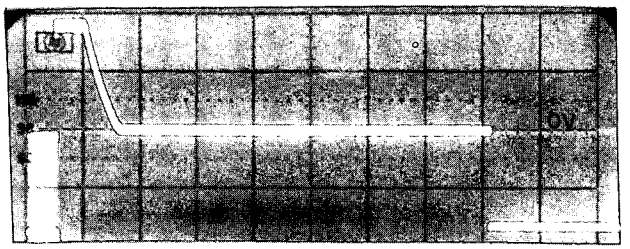
CLOSED

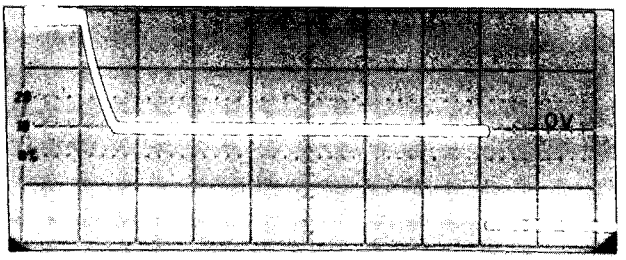


OPEN

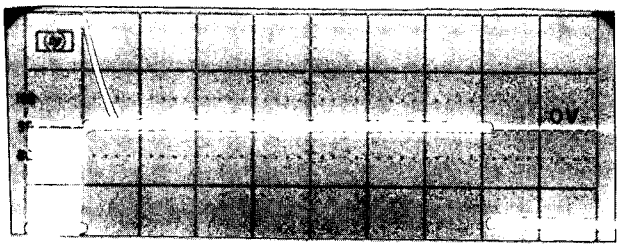


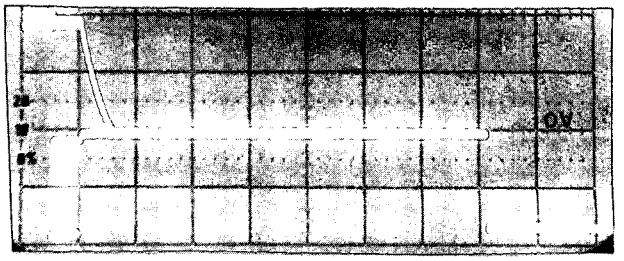
for U604/7,9 ?





for U604/3,18





g) **CRT Controller S.A. Test**

Switch OFF 8175A, refit the MPU and MMU devices on the CPU Board.

Signature Analyzer settings/connection points on A20 CPU Board.

START	∫	U416/40
STOP	∫	U416/40
CLOCK	∫	U416/21
⊥		⊥

Switch 8175A ON and wait until System Page **[Configuration]** menu displayed.

Note: Verify that reading at +5V is PAU7.

Check Signature of CRT Controller (IC U416 Schematic 2D) against Table 8-2-9.

Table 8-2-9. CRT controller SA

pin	S.A.	pin	S.A.
4	02A7	13	3PC1
5	2C83	14	5P3U
6	9530	15	PAU7
7	CH41	16	0000
8	6509	17	0000
9	94PC	18	94A5
10	8FHP	35	764H
11	HU3U	36	9451
12	56PO	37	H10A
		38	5C0A

DISPLAY SYSTEM/CRT TROUBLESHOOTING

The following procedure and information will help to determine if the CPU, Display Driver, or CRT is faulty. The first section determines if the CPU board is faulty, the second determines if the CRT or Display Driver is faulty.

CPU INTERFACE OPERATION VERIFICATION

NOTE

The following procedure assumes that there is NO video information being displayed on the CRT.

a. Turn OFF the 8175A.

b. With top cover removed. At the Display Driver board disconnect the 16 pin ribbon cable (W4) going to the CPU board (A20 J202).

c. See table 8-2-10 for cable pin assignments. Probe these pins and refer to Table 8-2-10 and 8-2-11.

d. See Table 8-2-11 for applicable electrical specifications if problems exist.

Table 8-2-10. CPU to Display Driver Cable Pin Assignments

Pin 1 is the red wire

(VER. SYNC.)	HVSYNC	1		2	GROUND
(HOR. SYNC.)	HHSYNC	3		4	GROUND
(VIDEO B)	HFB	5	P	6	GROUND
(VIDEO A)	HHB	7	I	8	GROUND
(SOURCE)	5V	9	N	10	GROUND
(SOURCE)	12V	11	S	12	GROUND
(SOURCE)	15V	13		14	GROUND
(SOURCE)	15V	15		16	GROUND

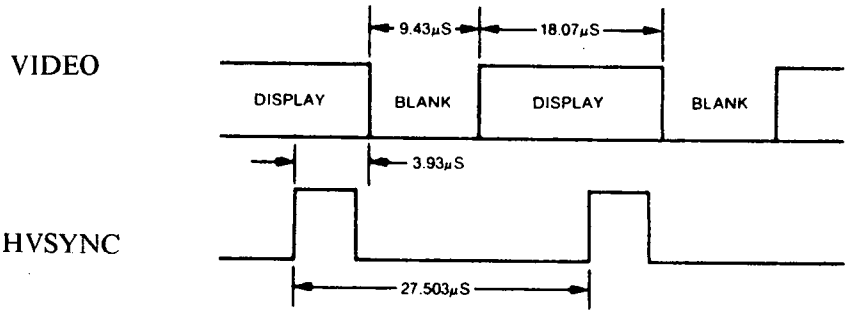
Table 8-2-10. Applicable Electrical Specifications

Vertical Sync. (fast axis)

a. Single-ended TTL input: HVSYNC

b. Sync signal timing caracteristics.

1. Pulse width and position relative to the video. Timing is a indcated below:



c. Scan direction is top to bottom.

Horizontal Sync. (slow axis)

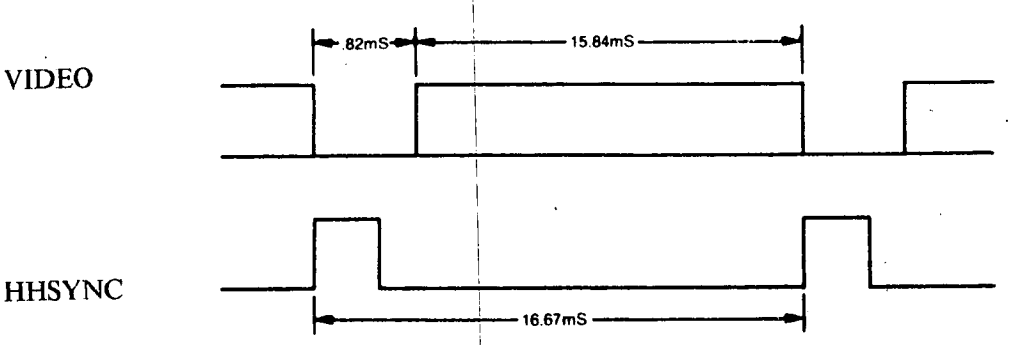
a. Single-ended input: HHSYNC

1. Low level signal is less than or equal to 0.4 volts.

2. High level signal is 5.0 volts +/- 5%.

b. Sync signal timing characteristics.

1. Pulse width and position relative to the video. Timing is indicated below:



c. Scan direction is left to right.

Table 8-2-10. Applicable Electrical Specifications (cont'd)

Video information

a. Single-ended TTL inputs.

1. Half-bright: HHB

2. Full-bright: HFB

b. Truth Table

HFB	HHB	Video Output
0	0	OFF
0	1	Half-bright
1	0	Full-bright
1	1	Full-bright

c. Dot period = 49.1 ns

Power Supplies

a. +5 volts + or -5%

b. +12 volts + or -5%; Imax = .085 Amps
(+12 volts used only for CRTY heater filament)

c. +15 volts + or -5%; Imax = .8 Amps average
1.5 Amps peak
.65 Amps typical
(+15 volts used for horizontal and vertical deflection)

DISPLAY DRIVER OPERATION VERIFICATION

The following procedure will help determine if the Display Driver or the CRT is faulty.

a. Verify that the 16 inputs form the CPU board meet the specifications given in Table 8-2-10 and 8-2-11.

WARNING

When performing the following tests, note that hazardous voltages are present!

b. If there is correct video information on the CRT, perform the Display System Adjustements procedure given in Section V (Adjustments). If any display cannot be performed, check the typical operating voltages for the CRT given in Table 8-2-11. Use a HIGH VOLTAGE PROBE for the measurements.

c. If the voltages to the CRT are correct, the Display Driver is bad and should be replaced.

d. If there is incorrect video information on the CRT, check the display generation circuitry on the CPU board, ie. CRT Controller, Character ROM, etc.

e. If there is NO video information on the CRT and the typical operating voltages for the CRT (see Table 8-2-12) are correct, then the CRT and Display Driver are suspect.

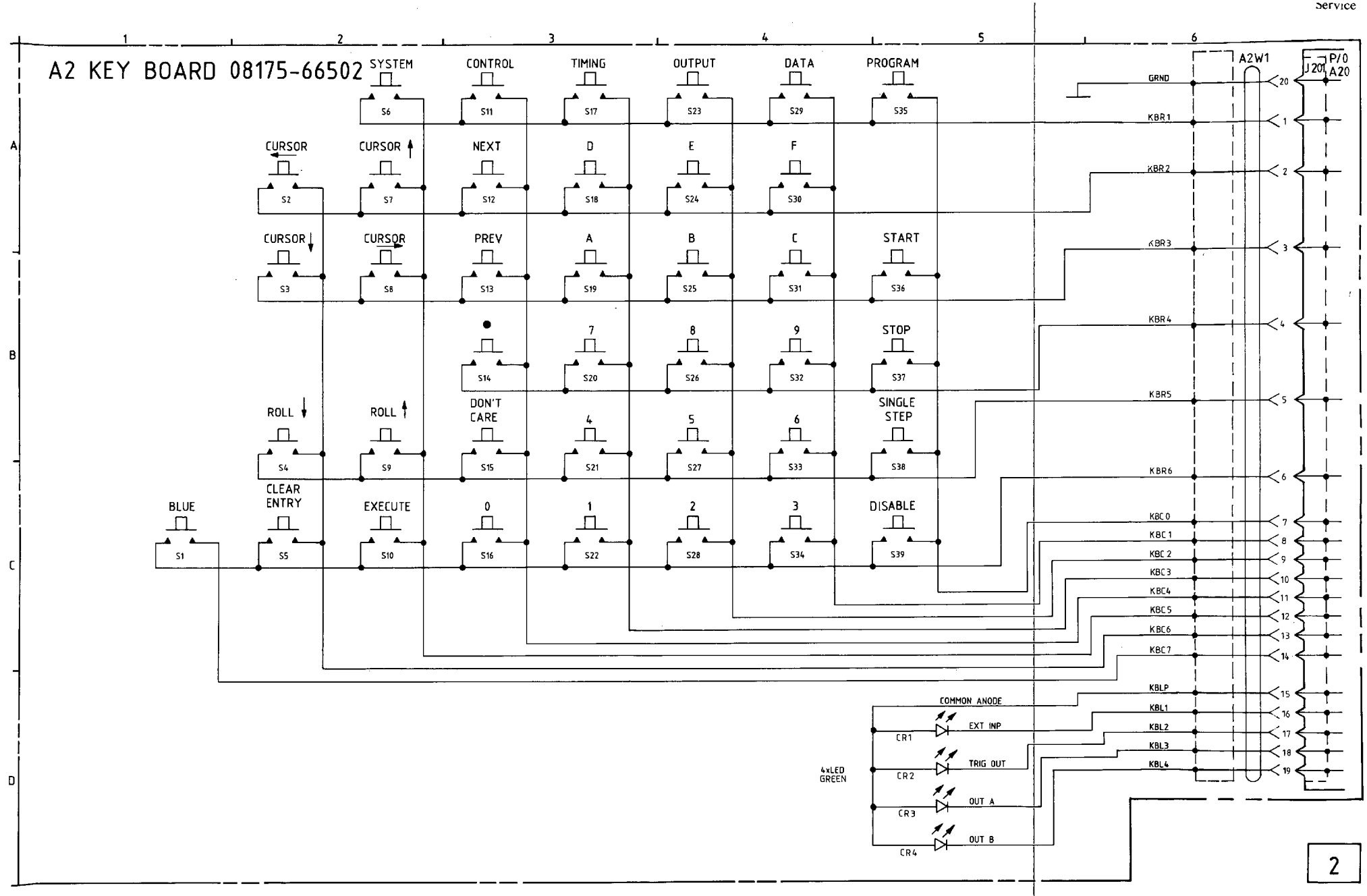
Table 8-2-12. Typical Operating Voltages For The CRT

NOTE

Unless otherwise specified, voltage values are positive with respect to Grid 1*.

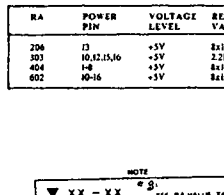
NAME	CATHOD PIN#	CATHOD CONNECTOR WIRE COLOR	TYPICAL OPERATING VOLTAGES
Grid 4	7	blue wire	0 to 400 Vdc
Grid 2	6	red wire	500-800 Vdc; Typ. 700 Vdc
Grid 1	5	not connected	
Heater	4	black wire	0V
Heater	3	brown wire	12 Vdc; 13.2 Vdc Max.
Cathode	2	yellow wire	48-82V
Grid 1*	1	green wire	0V
Anode		red post accelerator lead	8-12 KVdc; Typ. 10 KVdc

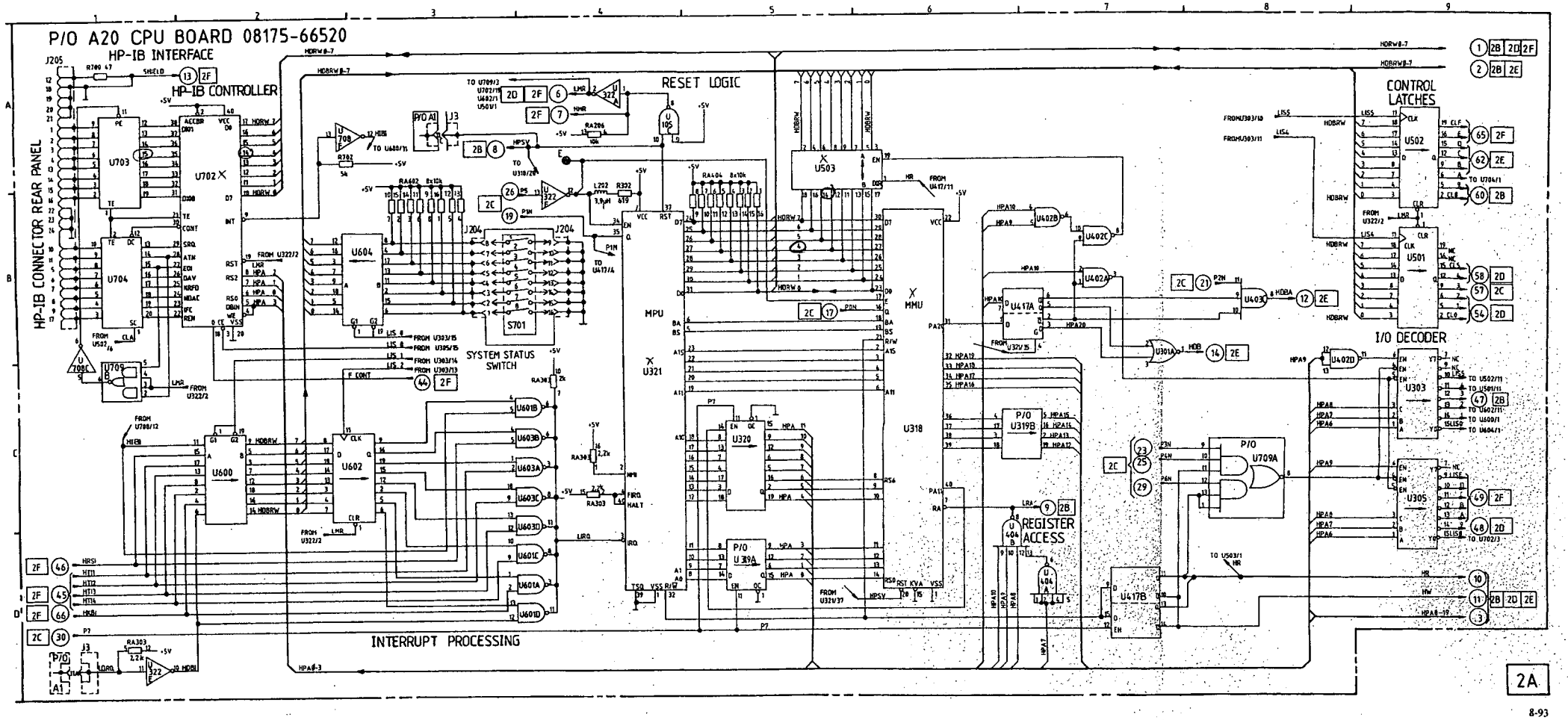
A2 KEY BOARD 08175-66502



REF.DES.	-5.2V	+5V	-15V	+15V	GND
U305		14			7
U306		16			8
U307		16			8
U308		20			10
U309		20			10
U310		20			10
U321		7			7
U322		14			7
U402		14			7
U403		14			7
U404		14			7
U417		14			7
U420		14			7
U501		20			10
U502		20			10
U503		20			10
U600		20			10
U601		20			10
U602		20			10
U603		20			10
U604		20			10
U702		20			10
U703		20			10
U704		20			10
U709		14			7

RA	POWER PIN	VOLTAGE LEVEL	RESISTOR VALUE
206	13	+5V	8x10K
303	10,12,15,16	+5V	2.2K
404	1-8	+5V	8x10K
602	10-16	+5V	8x10K

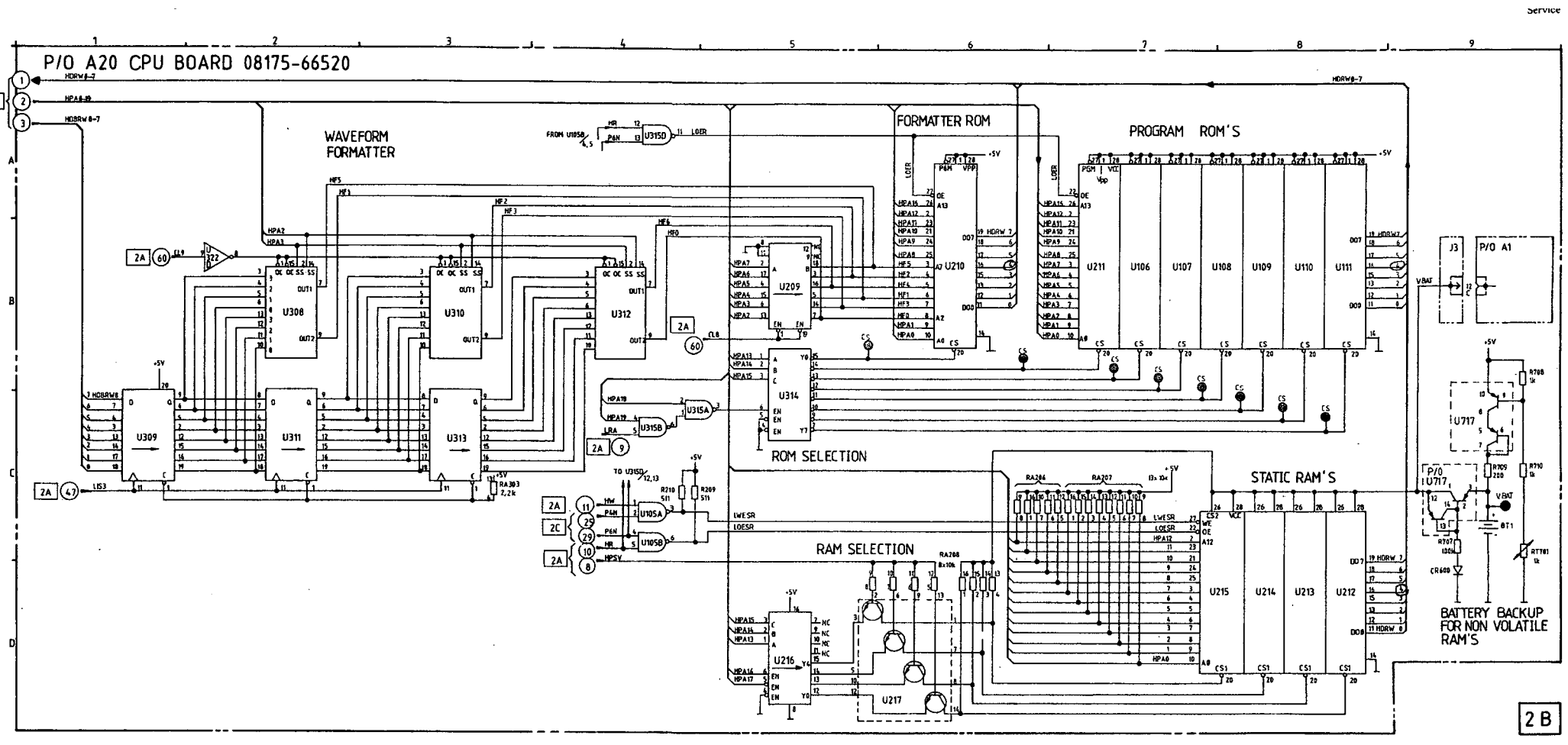




REF.DES.	-5.2V	+5V	-15V	+15V	GND
U305		14			7
U306		14			14
U307		14			14
U308		14			14
U309		14			14
U310		14			14
U311		14			14
U312		20			10
U313		14			14
U314		14			14
U315		14			64
U316		14			14
U317		14			14
U318		14			14
U319		14			14
U320		14			14
U321		14			14
U322		14			14

RA	POWER PIN	VOLTAGE LEVEL	RESISTOR VALUE
206	9-12,16	+5V	8x10K
207	9-16	+5V	8x10K
208	9-12	HPSV	8x10K
	13-16	VBAT	
303	13	+5V	8x2.2K

NOTE
E.G.
XX - XX
SEE RA VALUE TABLE FOR MORE INFORMATION
PIN NUMBER OF RESISTOR PACK
RESISTOR PACK NUMBER (RA)
ECL LINE BEING PULLED DOWN

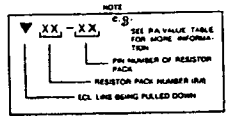


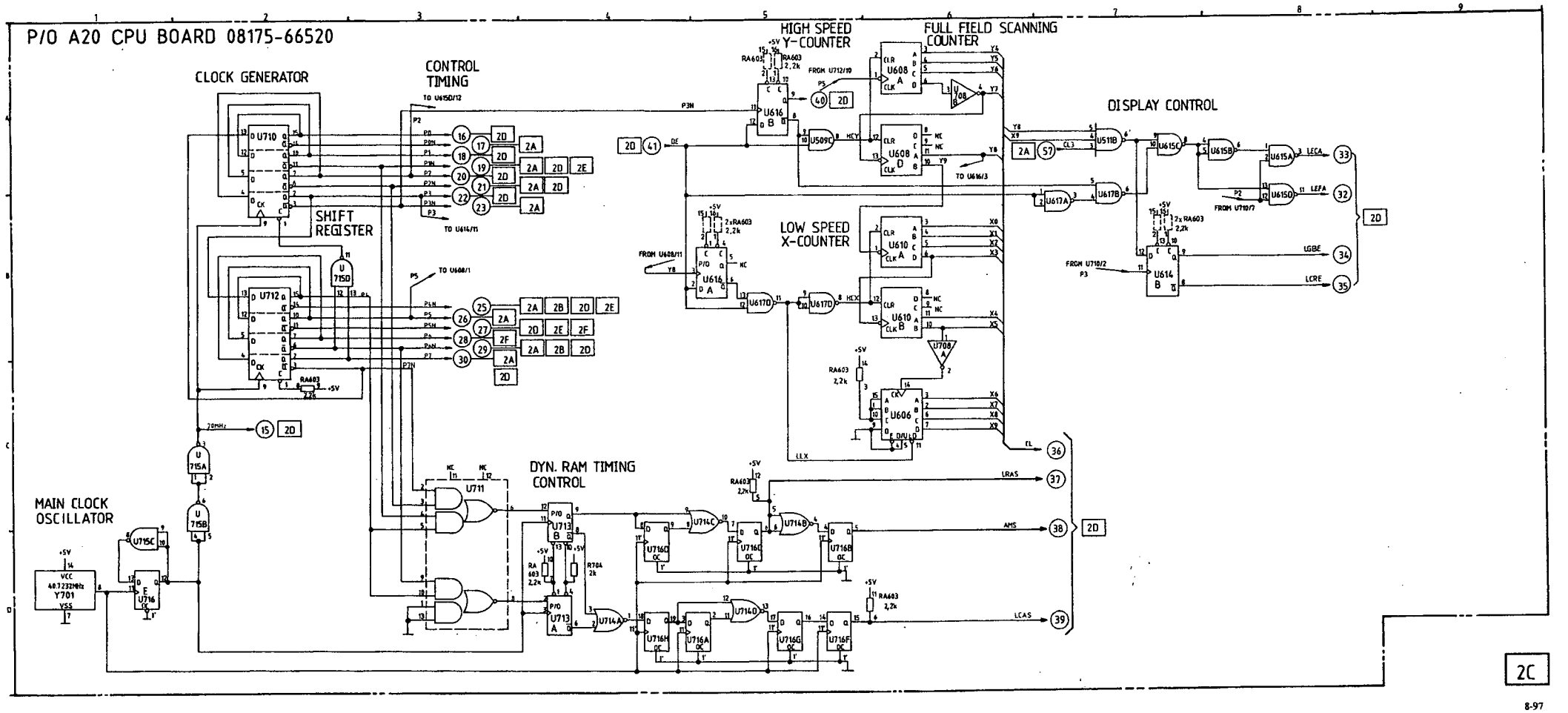
8-95

REF.DES.	-5.2V	+5V	-15V	+15V	GND
U509		14			7
U511		14			7
U606		16			8
U608		16			8
U610		14			7
U614		14			7
U615		14			7
U616		14			7
U617		14			7
U708		14			7
U710		16			8
U711		16			8
U712		16			8
U713		14			7
U714		14			7
U715		14			7
U716		20			10

RA	POWER PIN	VOLTAGE LEVEL	RESISTOR VALUE
603	9-12,14-16	+5V	8x2.2k

NOTE
e.g.:





REF.DES.	-5.2V	+5V	-15V	+15V	GND
U306		14			7
U315		14			7
U316		16			8
U317		16			8
U405		16			8
U406		8			8
U407		8			8
U408		8			8
U409		8			8
U410		8			8
U411		8			8
U412		8			8
U413		8			8
U414		16			8
U415		20			10
U416		20			10
U504		20			10
U505		20			10
U506		20			10
U507		20			10
U508		24			12
U509		14			7
U510		14			7
U511		14			7
U512		14			7
U607		16			8
U609		16			8
U611		20			10
U612		20			10
U613		14			7
U614		14			7

RA	POWER PIN	VOLTAGE LEVEL	RESISTOR VALUE
402	13,15,16	+5V	8x33 8x2.2K
603			

NOTE

XX - XX

SEE RA VALUE TABLE FOR MORE INFORMATION

PIN NUMBER OF RESISTOR PACK

RESISTOR PACK NUMBER (RA)

SCHEMATIC

P/O A20 CPU BOARD 08175-66520

ADDRESS MUX

GRAPHIC OUTPUT BUFFER

CHARACTER GENERATOR

CHARACTER ROM

DISPLAY DATA SHIFT REGISTER

DISPLAY DATA LATCHES

DYNAMIC RAM'S

CRT CONTROLLER

DYN. RAM ADDRESS MUX

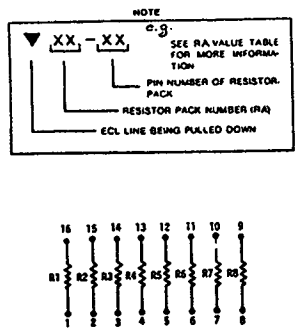
J202

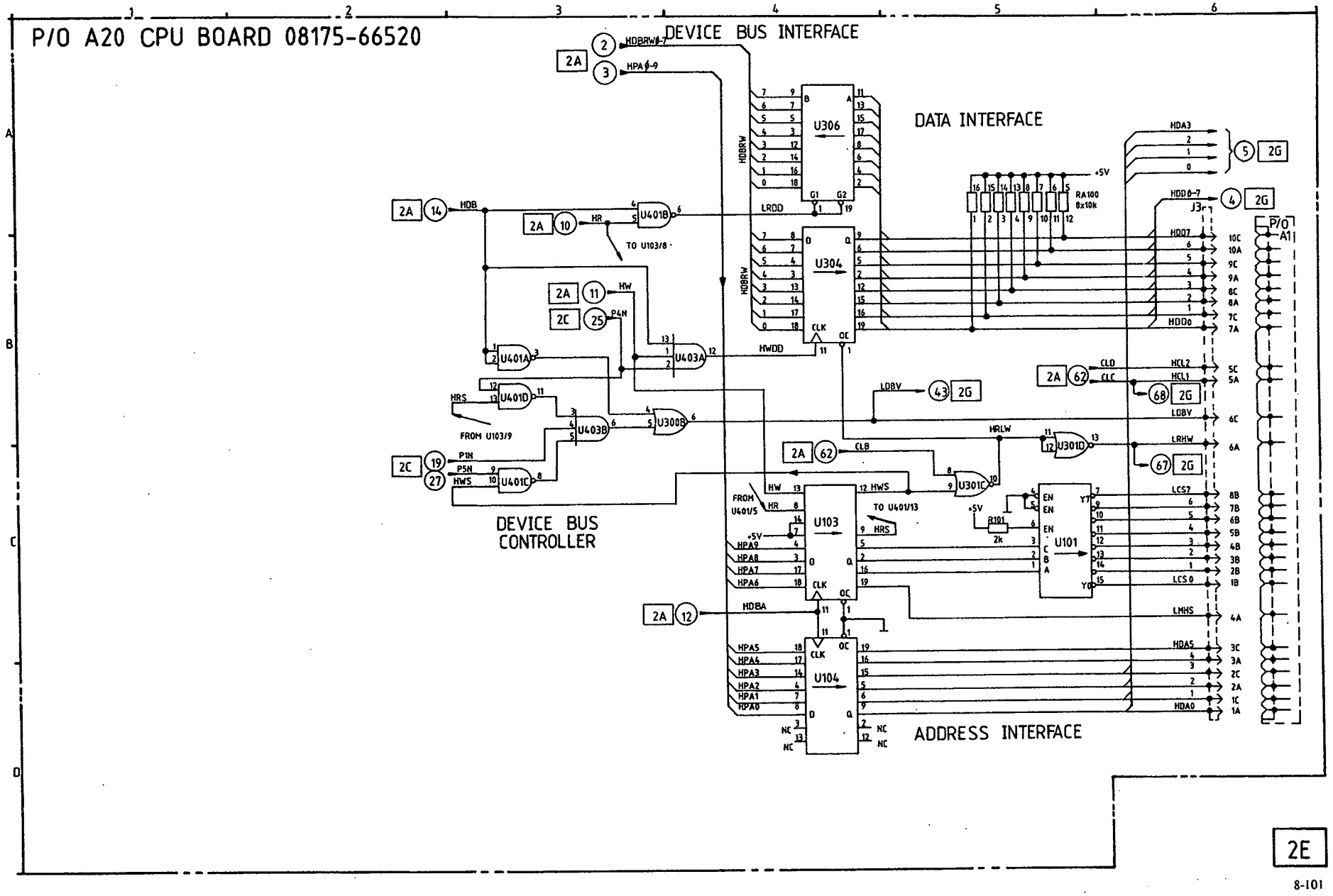
P/O A3

P/O A1

REF.DES.	-5.2V	+5V	-15V	+15V	GND
U101		16			8
U103		20			10
U104		14			7
U300		14			7
U301		14			7
U304		20			10
U306		20			10
U401		14			7
U403		14			7

RA	POWER PIN	VOLTAGE LEVEL	RESISTOR VALUE
100	5-8,13-16	+5V	8x10K





REF.DES.	-5.2V	+5V	-15V	+15V	GND
U322		14			7
U418		40			20
U419		16			8
U420		16			7
U605		14			7
U701		1			21
U705		14			7

RA	POWER PIN	VOLTAGE LEVEL	RESISTOR VALUE
303	6	-5.2V	2.2K

NOTE

XX-XX

SEE RP. VALUE TABLE FOR MORE INFORMATION

PIN NUMBER OF RESISTOR PACK

RESISTOR PACK NUMBER (RP)

ECL LINE BEING PULLED DOWN

P/O A20 CPU BOARD 08175-66520

P/O A21 CPU BOARD 08175-66521
RS 232 OPT.

P/O A1 J3 -15V -12V U616 IN OUT GND C615 2.2µ C614 2.2µ

REAR PANEL J203 PROTT GND SIGN GND SHIELD 13 2A

U705 U706 RA701 27k -12V +5V +12V

U707 DCD DTR DSR RTS CTS TXD RXD GND RI CS0 VCC HDRW7 HDRW0 HPA0 HPA1 LISC HR LMR PSM RS0 RS1 CS1 R/W RES X1 X2

R703 2K U708 HRS1 46 2A

TIMER

U701 PTU VSS OSC OSC5 OUT4 OUT5 OUT2 OUT1 OUT3 FOUT X1 X2 GND

HDW5 LISD LISE HPA0 HDRW7 HDB0 HTT1 HTT4 HTT2 HTT3 F-CONT. 44 2A

U322 RA303 2,2k BEEPER

2A 69 CLE CLF U605 C1.1 C1.2 D1 D2 C2.1 C2.2 Q1 Q2 NC

T601 3.686400MHz C702 27p C701 27p

2A 49 2A 45 2A

HDRW

KEY BOARD INTERFACE

2A 66 HKBI 2C 26 P6

U418 IRQ CLK RST RD WR A0 CS GND VCC B3 B2 B1 B0 RL7 RL0 SL2 SL1 SL0 DB7 DB0 LISA LISB HPA0 HDRW 7 HDRW 0 KBC7 KBC0

KEY BOARD CONTROLLER

2A 49

U419 C B A EN EN Y6 Y1 NC

RA303 2,2k

HDRW 0-7 HPA0 HPA1 HR LMR PSM 2A 27 2C

J201 GND +5V R605 6,8 KBLP KBL4 KBL3 KBL2 KBL1 KBC7 KBC0 KBR6

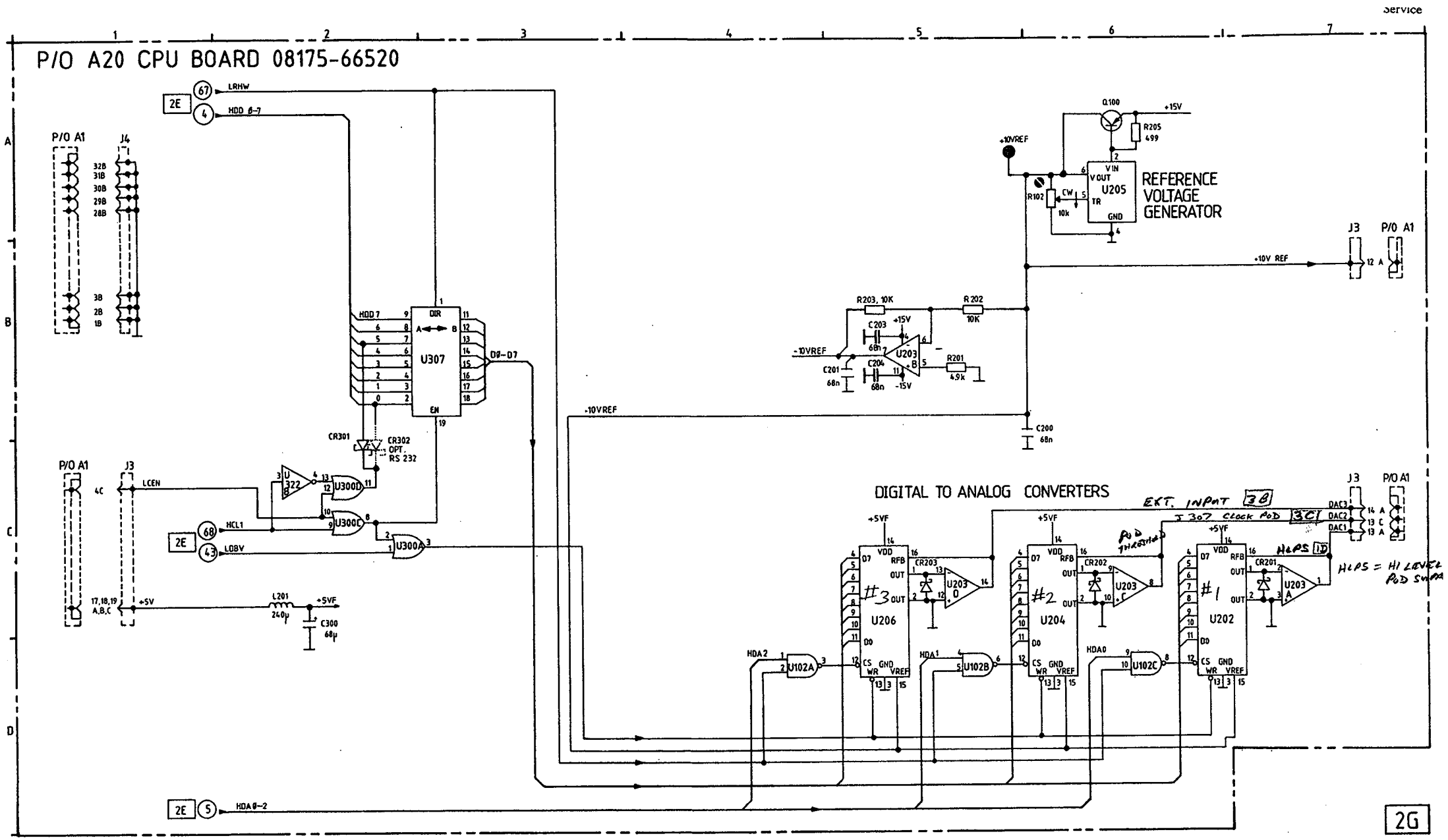
A2 W1 P/O A2

2F

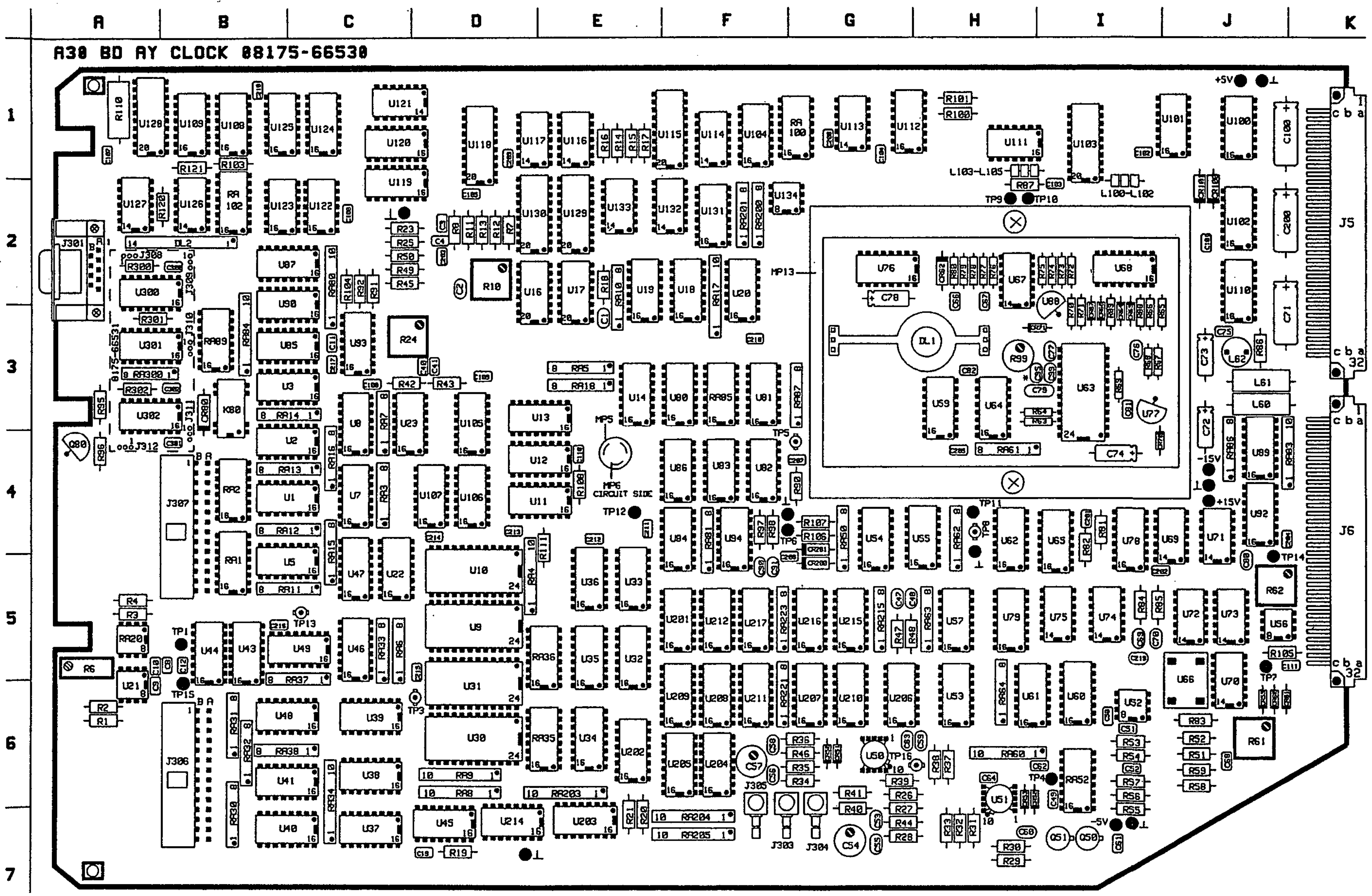
8-103

REF.DES.	-5.2V	+5V	-15V	+15V	GND
U102		14			7
U202		14			3
U203			11	4	
U204		14			3
U206		14			3
U300		14			7
U307		20			10
U322		14			7

P/O A20 CPU BOARD 08175-66520



2G



REF DES	GRID LOC
C1	E1
C2	D2
C3	D2
C4	D2
C8	B5
C9	A6
C10	A5
C11	C3
C12	B5
C19	D7
C40	D3
C41	D3
C47	G5
C48	G5
C49	I6
C50	I6
C51	I6
C52	I6
C53	G7
C54	G7
C55	G7
C56	F6
C57	F6
C58	F6
C59	G6
C60	H7
C61	I7
C62	H6
C63	G6
C64	H6
C66	H2
C67	H2
C68	J6
C69	I5
C70	I5
C71	I/J3
C72	J3/4
C73	J3
C74	I4
C75	J3
C76	I3
C77	I3
C78	G2
C79	H/I3
C80	J5
C81	I3
C82	H3
C90	F5
C91	F5
C95	H3
C99	I3
C100	I/J1
C101	J2
C102	I1
C103	I2
C104	G1
C105	D2
C106	C2
C107	A1
C108	C3
C109	D3
C110	E4
C111	K5
C200	I/J2
C201	I4
C202	I5
C203	D2
C204	J4
C205	H4
C206	F5
C207	F4
C208	G1
C209	D1
C210	F3
C211	E4
C212	E4
C213	D4
C214	D4
C215	D5
C216	B5
C217	C3
C218	B1
C219	I5
CR50	G6
CR51	G6
CR52	H6/7
CR53	H6/7
CR59	J6
CR60	J6
CR61	K6
CR62	H2
CR64	I3
CR65	I3
CR66	I3
CR67	I3
CR70	I4
CR71	I3
CR80	B3
CR100	J2
CR101	J2
CR200	G5
CR201	G4
DL1	G/H3
DL2	A/B2
J5	K1/2/3
J6	K3/4/5
J301	A2
J303	F7
J304	G7
J305	F7
J306	A/B6/7
J307	A/B4/5
J308	A2
J309	B2
J310	B3
J311	B4
J312	A4
K80	B3
L60	J3
L61	J3
L62	J3
L100	I2
L101	I2
L102	I2
L103	H1
L104	H1
L105	H1
MP5	E4
MP6	E4
MP13	G2
Q50	I7
Q51	I7
Q80	A4
R1	A6
R2	A6
R3	A5
R4	A5
R6	A5
R7	D2
R8	D2
R10	D2
R11	D2
R12	D2
R13	D2
R19	D7
R20	E6/7
R21	E6/7
R23	C2
R24	C/D3
R25	C2
R26	H6
R27	G7
R28	G7
R29	H7
R30	H7
R31	H7
R32	H7
R33	H7
R34	F/G6
R35	F/G6
R36	F/G6
R37	H6
R38	H6
R39	H6
R40	G7
R41	G6
R42	C3
R43	D3
R44	G7
R45	C2
R46	F/G6
R47	G5
R48	H5
R54	I6
R55	I6
R56	I6
R57	I6
R58	J6
R59	J6
R61	J6
R62	J/K5
R63	I3
R64	I3
R65	I3
R66	I3
R67	I3
R68	I3
R69	I3
R70	I3
R71	I3
R72	I2
R73	I2
R74	I2
R75	H2
R76	H2
R77	H2
R78	H2
R79	H2
R80	H2
R81	I4
R82	I4/5
R83	J6
R84	I5
R85	J5
R86	J3
R87	H1
R88	I3
R89	I3
R90	G4
R91	C2
R92	C2
R95	A3
R96	A4
R97	F4
R98	F4
R99	H3
R100	H1
R101	H1
R103	B1
R104	C2
R105	J/K5
R106	G4
R107	G4
R108	E4
R110	A1
R111	E4/5
R120	A/B2
R121	B1
RA1	B4/5
RA2	B4
RA3	C4
RA4	D4/5
RA5	E3
RA6	D5
RA7	C3/4
RA8	D6
RA9	D6
RA10	E2/3
RA11	B/C5
RA12	B/C4
RA13	B/C4
RA14	B/C3
RA15	C4/5
RA16	C3/4
RA17	F2/3
RA18	E3
RA20	A5
RA30	B6/7
RA31	B6
RA32	B6
RA33	C5
RA34	C6/7
RA35	D/E6
RA36	D/E5
RA37	B/C6
RA38	B/C6
RA50	G4/5
RA52	I6/7
RA60	H6
RA61	H4
RA62	H4/5
RA63	G5
RA64	H6
RA80	C2/3
RA81	F4/5
RA83	J4
RA84	B2/3
RA85	F3
RA86	J4
RA87	G3
RA89	B3
RA100	F/G1
RA102	B1/2
RA200	F2
RA201	F2
RA203	D/E6
RA204	F7
RA205	F7
RA215	G5
RA221	F6
RA223	F5
TP1	B5
TP3	C6
TP4	I6
TP5	G4
TP6	G4
TP7	J5
TP8	H4
TP9	H2
TP10	H2
TP11	H4
TP12	E4
TP13	C5
TP14	J4
TP15	B6
TP16	H6
U1	B/C4
U2	B/C4
U3	B/C3
U5	B/C4/5
U7	C4
U8	C3/4
U9	D5
U10	D5
U11	D/E4
U12	D/E4
U13	D/E3
U14	E3
U16	D2/3
U17	E2/3
U18	F2/3
U19	E2/3
U20	F2/3
U21	A5/6
U22	C/D4/5
U23	C/D3/4
U30	D6
U31	D5/6
U32	E5
U33	E4/5
U34	E6
U35	E5
U36	D5/6
U37	C7
U38	C6
U39	C6
U40	B/C7
U41	B/C7
U43	B5
U44	B5
U45	D7
U46	C5/6
U47	C4/5
U48	B/C6
U49	C5
U50	G6
U51	H6/7
U52	I6
U53	H6
U54	G4
U55	H4
U56	J5
U57	G/H5
U59	H3
U60	I6
U61	H6
U62	H4
U63	I3/4
U64	H3
U65	I4
U66	J5/6
U67	H2
U68	I2
U69	J4
U70	J5/6
U71	J4
U72	J5
U73	J5
U74	I5
U75	H/I5
U76	G/H2
U77	I3
U78	J5
U79	H5
U80	F3
U81	F3
U82	F4
U83	F4
U84	F4
U85	B/C3
U86	F4
U87	B/C2
U88	I2
U89	J3/4
U90	B/C2
U92	J4
U93	C3
U94	F4
U100	J1
U101	J1
U102	J1/2
U103	I1
U104	F1
U105	D3/4
U106	D4
U107	D5
U108	B1
U109	B1
U110	J2
U111	H1
U112	G/H1
U113	G1
U114	F1
U115	E/F1
U116	E1
U117	D/E1
U118	D1
U119	C/D1/2
U120	C/D1
U121	C/D1
U122	C2
U123	B/C2
U124	C1
U125	B/C1
U126	A2
U127	A2
U128	A1
U129	E2
U130	D/E2
U131	F2
U132	E/F2
U133	E2
U134	F/G2
U201	F5
U202	E6
U203	E7
U204	F6
U205	F6
U206	G6
U207	G6
U208	F6
U209	F6
U210	G6
U211	F6
U212	F5
U214	D/E7
U215	G5
U216	G5
U217	F5
08175-66531	
C300	B2
C201	B4
C302	B3
R300	A2
R301	A3
R302	A3
RA300	A/B3
U300	A/B2
U301	A/B3
U302	A/B3

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CLOCK
BOARD

SERVICE BLOCK 3
CLOCK BOARD

INTRODUCTION

The Clock Board interfaces with the "device bus" (see MPU) and the "high speed bus" on the motherboard. It has three main tasks:

It delivers all high speed control signals for the Data Board such as the 100 MHz Clock, and the control signals START and JUMP.

It interfaces the machine with external instruments/devices etc. via the Input pod and the BNC inputs Ext. Ref., Ext. Clock and Ext. Input.

It provides eight flag outputs. These are auxiliary and asynchronous outputs additional to the 24 main outputs.

Block Theory

The Clock Board comprises six main sections or blocks. An overview of these follows. Refer to the block diagram (Figure 8-3-1) to identify them. A table (Table 8-3-1) listing all the mnemonics used in schematics and other diagrams of this service block, is included at the end of the theory section. The six blocks are described in the detailed theory of operation in the same order as in the following overview.

100 MHz Master Clock Generator with phase lock loop and auto-calibration circuitry.

The input section for signal conditioning of the input signals from the Input pod or the three BNC-connectors.

Flag output section with driver circuits for the Flag Output pod.

Trigger filter sections.

Control section, including all the necessary circuits for the transformation of the input signals from the input section, or the device bus interface, into control signals for the Data Board.

Device bus interface, which interfaces between the MPU and the Clock Board. This enables information to be written into the control registers and RAMs on the Clock Board, and to be read from from circuits on the Clock Board, for status control and selftest reasons.

Detailed Theory of Operation

The following paragraphs provide detailed theory of operation for each of the six "blocks" previously described. The schematics to be referred to in each case, are shown in brackets alongside each heading .

100 MHZ MASTER CLOCK GENERATOR (Schematic 3A)

The actual oscillator section consists of a delay line oscillator built with ECL NOR Gate U63 and a 2 ns coaxial delay line feedback (DL1). The delay line is terminated with a network consisting of a voltage divider R70/R71 providing - 2V from 50 Ohm. R99 (adjustable resistor) provides a coarse frequency adjustment of +11 MHz -9 MHz. Varicaps CR 64 to CR 67 linked via C77 to the termination point, provide a fine, voltage dependent, frequency control of +2.6MHz -2.6 MHz.

The oscillator is synchronously startable via a second input of the NOR Gate (U 63C/12). When this input is held high, the oscillator will stop. A transition from high to low on this input will start the oscillator (with well defined start phase at the output). The additional circuitry connected with the 100 MHz Master Clock Generator is involved in providing the two modes of operation:

The free run mode with closed phase lock loop.
The synchronous start/stop mode with autocalibration capability.

The following components form a phase locked loop, (PLL) for oscillator control:

- reference crystal oscillator U66
- phase comparator U71, U72, U73, U74
- loop filter U67,
- VCO U63 and
- frequency divider U65, U78, U69.

The operating principles of the PLL are illustrated in Figure 8-3-2. The PLL is closed or opened by the analog switch U68. For running the oscillator in the synchronous start/stop mode, this analog switch is open. Calibration of the frequency with respect to the 1MHz crystal oscillator (U66), is possible via the DAC variable voltage source U76 (U67).

The microprocessor is able to monitor whether the frequency is too fast (FRUP) or too slow (FRDN), from the phase/frequency comparator latched outputs U75/5,9. Dependent upon the information received, the MPU calculates an appropriated value for the control of the DAC.

The 100 MHz Oscillator (VCO) output is buffered by the line receiver U64A/3 and then fed to the devices U60B, U62B, U61C. Here, selection of the required clock from one of the the three different clock sources is done. The clock sources and their signal names are:

Internal 100 MHz master clock (TP8)
External clock from rear panel BNC connector (PEXTCLK2)
External clock from input POD (PEXTCLK1)

The selected clock is fed via U302 (Schematic 3C) to the Buffer Circuit U85, and the Control Circuit U90, U87, U89 (Schematic 3C). These circuits deliver the clock and other control signals from the control section to the Mother Board (J6 high speed bus) and to the master/slave connector J301.

The selected clock is conditioned on the Data Board and then fed back (UCLK) to the Clock Generator, which is a programmable clock divider (Schematic 3A). This circuit delivers the Clock output CCLOCK (U214A/3) to the Flag Output Pod (schematic 3D) controlled by the HUINIT Line (see Data Board theory).

The selected clock is also fed to the buffers U64 B,D, measured by the PLL-Circuitry and fed as signal FRQLATCH to the frequency latch U82B (Schematic 3C). This is of significance when External clock is used.

Two error conditions can be detected when external clock signal is used:

clock too slow
clock too fast

If either of these error conditions occurs, a corresponding error message will be displayed at the top of the 8175A screen.

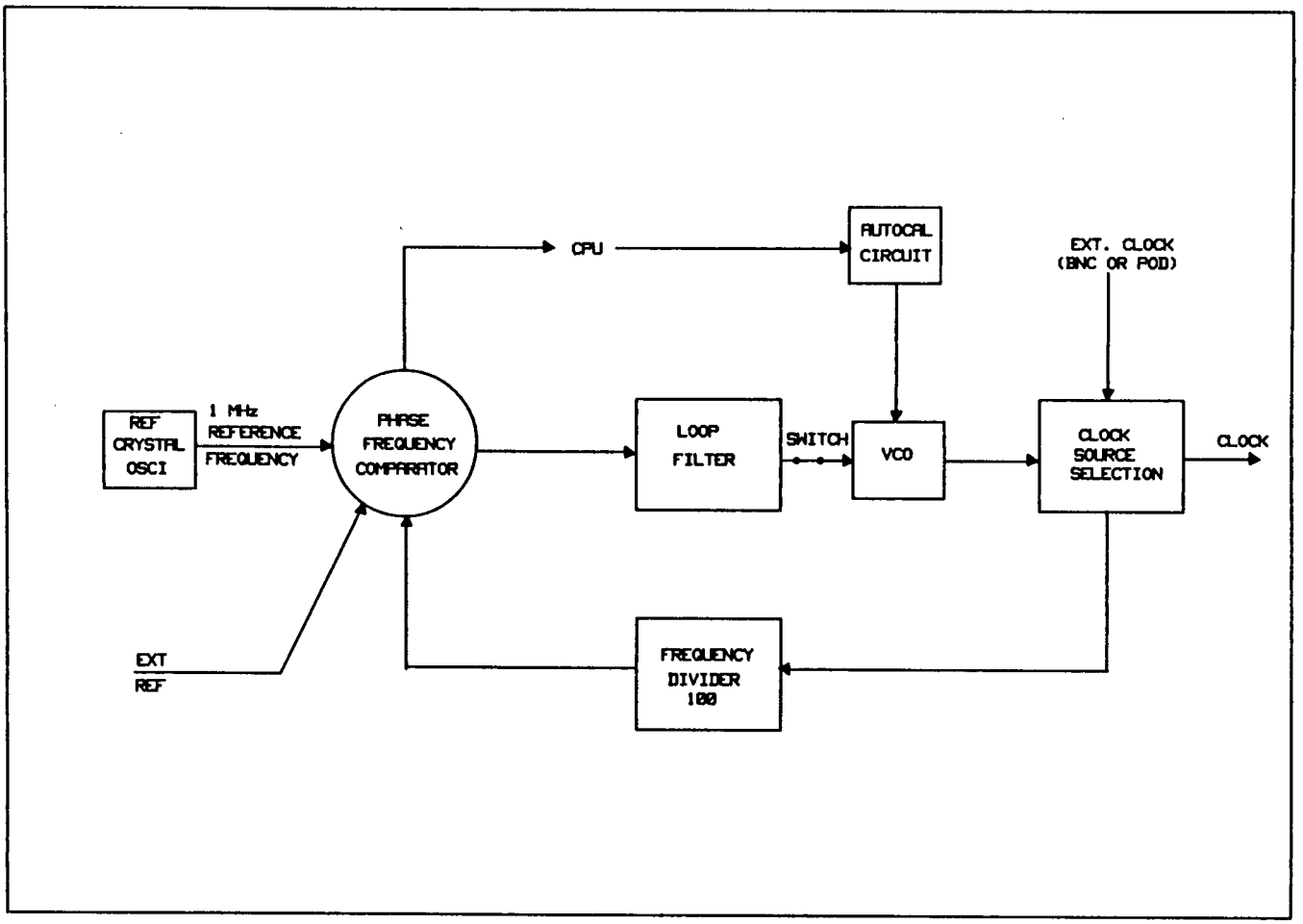


Figure 8-3-2. Phase Locked Loop (PLL) Operating Principles

Clock too slow
This is measured by the MPU via the frequency latch U82B (Schematic 3C). The MPU resets U82B via HFRR, waits a predefined time of typ. 140 ms, and reads the information of U82B via U93B on to the data bus line D6. If no positive clock edge occurs during this time at the trigger input of U82B/11, its output signal LFRQSL remains low and the MPU recognizes "fequency too slow".

If a pos. clock edge occurs, the output of U82B/14 goes high, and the MPU recognizes that a signal is present. Then the "clock too fast" measuring is done.

Clock too fast
(this means: F>100MHz if data timing >= 2 or 50 MHz if data timing = 1) It is measured by the PLL-circuitry. It compares the exteral clock frequency (which is divided by 100) with the internal or external Ref Oscillator signal. The output of U75A (FRUP) goes high if the frequency is too fast. This information is readable by the MPU via signal LRDFRQ (D0).

INPUT SECTION (Schematics 3B, 3C)

The input section is divided into three subsections:

The input and control circuitry for the signals coming from the Input pod (schematic 3C),
The circuitry for the signals coming from the BNC-connection (Schematic 3B) - Ext Input - at the front panel - Ext. Clock - at the rear panel and
Ext. Ref. at the rear panel (Schematic 3A).

Signals from the Input pod
These signals, (Schematic 3C) - eight data and one clock signal - are ECL differential signals fed through connector J307. They are terminated and pulled down with resistors RA 1,2,11,12,13,14 and converted to ECL single ended signals by line receivers U1,2,3.
Then the eight data signals are connected to the D-inputs of latches U7,8. They are clocked either by the positive or negative slope of the clock signal in synchronous mode, depending on the state of the control signal HPOSSLOPE (U12A/4). The latches are transparent (asynchronous mode), if the control signal LSTATE (U5A/4) is low. The clock signal is also connected, via signal PEXTCLK1 to U60 and can be used as master clock if external clock from pod is selected. The control signal HDISINP 36 3E forces the latch outputs to the low state. Therefore, the input pod signals are disabled if the qualifier RAMS U9, U10, and the flag RAMS U30, U31 are set by the MPU.

The threshold (PODTHR) for the pod, is a reference power supply (TP1) that specifies the comparator switching point on the pod hybrid chip. The supply is processor programmable via a DAC on the MPU board and allows threshold programming in the range of plus to minus 9.9V in 100mV increments. The voltage output of the DAC (DAC2) is taken from the Mother Board J5/13C, and converted to a voltage proportional to the required threshold (U21A,B). The ground sense line (GRDSENSE) from the pod, compensates the difference in ground levels between systems. This ensures that user selected threshold levels will relate correctly to the user system ground.

BNC Inputs - EXT. INPUT and EXT. CLOCK
The signals from the BNC-connectors (EXTINP) J303 and (EXTCLKINP) J304, (Schematic 3B) are terminated by R26,34 and divided by 6 with R27,44,28 and R35,46,36. They are then fed to the input of fast comparators U50, U51 which are protected against excessive voltage by clamping diodes CR50,51,52,53 and a clamping circuit Q50,51 and RA52. The output of U51 (PEXTCLK2) is fed to the clock source selection circuit U60 (Schematic 3A), and the outputs of U50 are connected to a flip flop U53. Control signals HT0-3 enable selection of the required START/STOP modes are done (see CONTROL SECTION description).

Threshold programming is done by the processor via a DAC on the MPU board and allows threshold programming in the range of plus to minus 9.9V in 100 mV increments. The voltage output of the DAC (DAC 3) is taken from the Mother Board (J5/14A) and converted to a voltage proportional to the required threshold (U52A, B). This voltage is supplied (TP4) to the termination and dividing network of each input. Therefore, the threshold for the Ext. Clock and Ext. Input is programmed at the same time.

BNC Input - EXT REF
The signal from the rear panel BNC-connector (PEXTREF) J305, is connected to the input pins 5 and 10 of the TTL NAND Gate U70 B,C (Schematic 3A). This input is protected against excessive voltages by R83 and clamping diodes CR60,61.
The Ext. Ref. Signal is then buffered and rectified with CR59 and C80 to a low level at U73/2, so disabling the internal 1 MHz crystal oscillator signal.
Simultaneously, the signal path for the Ext. Ref is enabled by high level at U70/9. Therefore, the Ext. Ref. Signal is connected to the reference input of the phase frequency comparator U71, U72, U73, U74.
If the Ext. Ref. signal is disconnected, the internal 1 MHz reference crystal oscillator signal is enabled with a high level at pin 2 of U73A pulled up with R105.

FLAG OUTPUT SECTION (SCHEMATIC 3D)

The Flag Output section provides eight Flag channels. They may be set or reset asynchronously to the 24 main outputs under microprocessor control, or under control of a predefined pattern at the input pod. The flag output connector (J306) on the rear panel, allows connection of an ECL output pod or a TTL/CMOS output pod. Eight differential line pairs are driven from the output driver IC's U48,49. The inputs of the drivers can each be fed via signal lines FLAGUP0/7, from one of two different wire-OR outputs. One is the latch output (U46/47) which provides set or reset signals of the flag outputs under Input pod control. The other outputs come from U43,44 and are driven under microprocessor control, via TTL latch U128 and TTL/ECL converter U126, 127 (schematic 3E). If the flag output is under MPU control, the control line LFLAGUP is set low enabling U43, U44 and HFLAGUP is set high forcing the latch output of U46, 47 to low.

When the Output Flags are to be set or reset under Input pod control, the operation is as follows:

The outputs of the input latches U7, 8 represents the current logic state of the pattern at the inputs of the Input pod connected to J307 (Schematic 3C). These eight outputs are connected via address lines HMAD0-7 to the address inputs A0 to A7 of the Flag Memory U30, 31 (256 x 8). These RAM's can be written to by the microprocessor via Flag Counter U119/120. The pattern that appears at the outputs of the RAMS was previously written into the locations by the MPU, now they are addressed by the pattern of the Input pod. If this output pattern differs from the last addressed pattern (which is latched in the first latches (40/41)) it will be recognized by the EX OR Comparators U37,38,39. A high pulse will then be output by the comparator(s) so triggering the Flag Filter mono flop (U23A,C) and making the first latches U40, 41 transparent.

The RAM output pattern will now propagate through the latch and be latched at the moment when the comparator recognizes that both, latch input and output-pattern, are the same. If no change at the RAM outputs occurs before the the trigger filter time elapses, this pattern is clocked into the flag output latch U46, 47. The via U22A3. Note that in the Transparent Flag mode, signal LLATCHFLAG (U40/13) is at constant low. In Latched Flag mode, this line goes low only for those specific patterns at the Input pod which are to change the output flags.

TRIGGER FILTER SECTION (Schematics 3C, 3D)

This comprises two subsections or blocks:

A Trigger filter for Start, Stop, Cont, JumpA,JumpB, TRION, TRIOFF in the Control Section.
A Flag filter for asynchronous tristate and the flags in the Flag Section.

The Trigger Filter

The main part of the trigger filter (Schematic 3C) is a retriggerable analog monoflop circuit (IC's U16, U17, U18,) which is able to block any information relating to start, stop etc., from reaching the following circuitry during the programmed trigger filter time.

If any change at the outputs of the qualifier RAM (U10) occurs, the latch U13 (controlled by the 8bit Data of the Input pod) and the error-gates U11, U12 start the analog monoflop U16 and latches this event into the latch U17. After a predefined trigger time (programmed by the MPU via R11-R17), the mono flop generates a positive trigger edge which latches U14, U19 providing that no new event at the outputs of U10 has retriggered the monoflop.

This information is fed to decoder U80, the from where the corresponding output pattern will be ouput. The enable signal for U80 is generated by the outputs of the latches U17, U14, U19 and the EXOR Gates U20 depending on a change at the outputs of U14, U19. Then it is fed, via exclusive OR/NOR Gate U11 and the flip flop U83, to the enable input of U80. The ouput patterns are enabled for 10 ns. If a new event retriggers the monoflop U16 during the trigger time, the new information will be taken as the latest and then cause the procedure as just described to be repeated.

The Flag Filter
(Schematic 3D) This is also a retriggerable monoflop (U23). This monoflop is triggered by any change of the outputs of U30, U31, U9 detected with the EX OR comparators U37, U38, U39. After a predefined trigger time (programmed by the MPU via R23, R24, R25, R45, R49, R50), the monoflop generates a latch signal which gives the new information to the Flag Output pod (or to the tristate circuitry) if no retrigger followed. If a retrigger via a new change of the outputs of U30, U31, U9, is detected during the trigger filter time, the present information will be blocked. The new information will then be processed as just previously described.

CONTROL SECTION (Schematic 3C)

The control section provides signals necessary for the control of the Data Board, including CLOCK, JMP, START, and for the control of the Buffer Board, including TRIST. It also includes the interface for synchronizing a second 8175A in the Master/Slave configuration. There are three potential sources of input signals for the control section:

BNC connector EXT. Input (Schematic 3B)
Input pod (Schematic 3C)
MPU via device bus interface (Schematic 3A)

EXT. Input (BNC)
After transforming the EXT. Input signal (Schematic 3B) to an ECL compatible level with the high speed comparator U50 (TP16), these signals are fed to the START/STOP selection circuit. Two, positive edge triggered, monoflops (U53, U57 and R47, C47 and R48, C48) differentiate it to small pulses either on the positive or on the negative threshold crossing of the input signal. These pulses are available at the outputs of the flipflops U53/15, 2. The required start/stop conditions are output from gates U54, U55 under control of signals HT0 - HT3:

HT3	HT2	HT1	HT0	Function
1	1	1	1	no action
1	0	1	1	Start on pos. edge
1	1	1	0	Start on neg. edge
1	0	1	0	Start on both edges
1	0	0	1	Start on pos. and stop on neg. edge
0	1	1	0	Start on neg. and stop on pos. edge

The output of the gates U54, 55 are the start signal PTRIGSTART (TP5) and the stop signal PTRIGSTOP (TP6).They are OR'ed with the start and stop signals from the other sources in the control section (Schematic 3C)

Input Pod
After conditioning (see INPUT SECTION description), the signals of the Input pod (Schematic 3C) are connected from the outputs of the latches U7, U8 to the address lines A0-A7 of the Qualifier Memory (U9, U10) via address lines HMAD0-7. These RAMs are MPU writeable via the device bus interface (MDI0-7). A pattern that was previously written into the location by the MPU, appears at the outputs of the RAMs. The RAMs are now addressed by the pattern at the Input pod. If this output pattern differs from the last addressed pattern (latched in the first latch U13, connected to the outputs of the RAMs) it will be recognized by the EXOR comparator U11, U12. This comparator outputs a high pulse which triggers the trigger filter monoflop and makes the first latch U13 transparent until the output of the latch is the same as the input. If no change at the RAM outputs occur befor the trigger filter time elapses, the pattern at the outputs of the first latch U13 is clocked into a second latch U17. Its function is described in the TRIGGER FILTER SECTION description. The outputs of U17 are fed to the 1 of 8 decoder U80 via the latches U14, U19 which are controlled by the trigger filter. Each of the eight outputs of the decoder corresponds to an action which may be triggered by the pattern of the input pod. This is shown in the following table:

U80 Decoder inputs			Action
A	B	C	
0	0	0	no action
1	0	0	START
0	1	0	STOP
1	1	0	CONTINUE
0	0	1	JMPA
1	0	1	JMPB
0	1	1	TRIST ON
1	1	1	TRIST OFF

The second output of the latch U14 (which is controlled by the trigger filter (see TRIGGER FILTER SECTION description) is ORed with the output of the tristate flipflop U203B pin 15, hich is set or reset by the decoder outputs TRISTON or TRISTOFF.

Each output of the decoder described above is wire ORed with an output of a second decoder. This second decoder U81 does the interfacing to the third source of input signals to the control section, the MPU. The only difference compared to te to the first decoder is, that the inputs are not driven by the outputs of the qualifier RAMs, but by the device bus address lines of the MPU. So every action which may be triggerable by an input pattern at the Input pod is also triggerable by the MPU.

The common part of the control section (independent of the controlling source) consists of:
flipflop U82A, the START/STOP flipflop and the TRIST flipflop (U203); the OR gates U84, the drivers for the Master/Slave interface U85, the receiver U90 also for the Master/Slave interface, U300 to 302, multiplexer U87 for the interface to the Mother Board. The output of the START/STOP flipflop U82A controls the oscillation of the master oscillator and is MPU readable via the ECL/TTL converter U93. This flipflop is set by the following OR'ed signals:

PSTART from the decoder described prevoiusly U80/81
PTRIGSTART from the Input Section (START/STOP Selection, Schematic 3A)
PCONTINUE from the decoder U80, U81
PJMPA from the decoder U80, U81
PJMPB from the decoder U80, U81

The START/STOP Flipflop is reset by following ORed signals:

PSTOP from the decoders U80, U81
PTRIGSTOP from the Input Section (START/STOP Selection, Schematic 3A)
and also from the signal HSTOP (U92A/3) from the Data Board in single cycle mode, when a program end is reached.

Gates U84 encode the START, JMPA, JMPB and CONTINUE commands into two lines as described in the following truth table:

EVENT	Mother Board line HSTART	Mother Board line HJMP
NO	0	0
START	1	1
JMPA	0	1
JMPB	1	0

These signals are synchronized with the clock by the flipflops U300, U301 and the gate U302. This is done as follows:
If a START (JUMP) occurs, it is latched in the FF U301 (which is self blocking, via its outputs) and fed to the synchronizing FF U300. If a pos. edge of the clock occurs at the trigger input of U300, a start (jump) pulse with a width of 20 ns is given to U85 with a defined phase to the clock. Then the FF U300, 301 are reset via the NOR gates U302.

The remaining gate U84B, ORes the two different TRIST sources: the tristate flipflop U203B, the HTRI-STATE signal from the latch U14. The signal HTRISTKEY from the MPU writeable register U115, is ORed with the Tristate Line by U84D. U85 A-D does the transformation of the three single ended lines and the clockline to four differential line pairs, with 50 Ohm serial termination (RA89) driving the master/slave interface connector J301 on rear panel and the receivers U90. This applies for the Master mode.

In the Slave mode, the outputs of U85 emitter follower are disabled by relay K80. In this case, J301 is an input connector for the slave, receiving the control and clock signals from the master. U90 buffers these signals and MUX U87 selects the delayed path in Master mode and the undelayed path in Slave mode. This is necessary to compensate the additional skew between master and slave (caused by the twisted pair transmission line between master and slave). U89 converts the four output signals of U87 to differential signals, which are fed to the high speed bus on the Mother Board via J6.

DEVICE BUS INTERFACE (Schematic 3E)

The principal function is the same as on the other boards and is described in the MPU part. It interfaces between the MPU and the Clockboard, allowing information to be written to control registers and RAMs on the Clockboard, to be read from circuits on the Clockboard for status control and selftest reasons.

The eight bit bidirectional databus is buffered by U103. The data flow direction is determined by the signal LRHW. Decoding of the address lines HDA0 - HDA5 is done by the main decoder U102 and the subdecoders U100, U101, U104 and U81. Every read or write cycle is synchronized by the signal LDBV. Card selection and board recognition is done by the signals LCEN, HCL1 and HCL2 via the main decoder U102 the gates U110 A,B and the diodes CR100, 101.

Table 8-3-1. Mnemonics Explanation

The first letter of a mnemonic means:

N: active on the falling edge
P: active on the rising edge
H: active high state
L: active low state

Mnemonic	Explanation
CCLOCK	Counter Clock is output of the user clock
CLOCK	Master Clock fed to the Data Board
CLOCK (invers)	Master Clock fed to user clock circuitry
CL0 - CL2	Buffered Clock0-2 for the user clock circuitry
CT0 - CT10	Counter bits 0-10 for user clock programming
CTR	Counter Range bit for user clock range 10 and 100
D0 - D7	TTL Data Bus 0-7
DONTCARE	Inactive line
EXTCLOCKINP	External Clock Input
EXTINP	External Input
FD0 - FD7	Flag RAM Data outputs
FLAG0 - FLAG7	Flag outputs 0-7 to the flag pod
FRDN	Frequency down for frequency calibration
FRQLATCH	Trigger the frequency latch
FRUP	Frequency up for frequency calibration
GRDSENSE	Ground Sense line. Compensates the ground levels between systems
GT0 - GT7	Glitch supress time 0-7 for the trigger filter
HDA0 - HDA5	High TTL Devicebus Address 0-5 from the CPU
HDISINP	High Disable Input blocks the Input Pod signals from the following circuitry
HEXT1	High External 1. Ext. clock selection (1 = Pod).
HEXT2	High External 2. Ext. clock selection (1 = BNC).

HFUNCTSEL 0-2	High Function Select 0-2 decodes the qualifier functions
HFRR	High Free Run, sets the internal clock oscillator in the free run mode and resets the frequency latch if ext. clock is used.
HLOCKPLL	High LOCK PLL
HMAD0 - HMAD7	High Memory Address 0-7 from the qualifier and the flag RAM's
HPOSSLOPE	High Positive Slope chooses the edge for Input pod data synchronization
HQUALOFF	High Qualifier OFF blocks the qualifier functions from the following circuitry
HSLAVE	High Slave sets the generator in slave mode
HSTARTOSC	High Start Oscillator starts the internal oscillator or enables the external clocks
HSTOP	High STOP stops the oscillator after single cycle and after the program single step
HT0 - HT3	High Trigger function 0-3 selects the different modes from the external clocks
HTRISTKEY	High Tristate Key disables all outputs
HTRISTATE	High Tristate is the asynchron tristate line
HPSS	High Processor Single Step selects the function start, etc. from the CPU
"L"	Low for open latch inputs
LADDCLK	Low Address clock steps the memory counter for the RAM's
LCLKCTRL	Low strobe signal for the clock control register
LCCLKREG1	Low strobe signal for the counter clock register 1
LCCLKREG2	Low strobe signal for the counter clock register 2
LCEN	Low Card enable
LCTRLREG1	Low strobe signal for the control register 1
LCTRLREG2	Low strobe signal for the control register 2
LCLKOFF	Low Clock OFF switches the userclock off
LDBV	Low Device Bus Valid
LEXTCLK	Low external Clock selects the external clocks

LFLAGUP	Low Flag Up set the circuitry into static mode
LFLAGUP0 - 7	Low Flag Up 0-7 set the flags by the CPU
LFULLCLK	Low Full Clock is used for a special programming external clock x 1 on the Data Board
LFRQSL	Identifies "clock too slow"
LGLITCHTIME	Low strobe signal for the Glitch Time register
LLDMEMADD	Low strobe signal for loading the memory address counter
LLATCHFLAG	Low Latch Flag latches the flags in latch mode
LRDFRQ	Low Read Frequency addresses the frequency comparator to read
LRDMEM	Low Read Memory enables the read circuitry from the RAM's
LRDOSCSTATE	Low Read Oscillator State addresses the state comparator to read the oscillator state and the Data Board state
LRHW	Low Read/High Wright
LSETFLAG	Low strobe signal for setting the Flag register
LSLAVE	Low Slave (see HSLAVE)
LSTATE	Low State selects the mode asynchronous or synchronous for the input pod
LSTART	Low Start identifies the state of the oscillator
LTRIGCTRL	Low strobe signal for the Trigger Control register
LVA	Low valid Address enable the CPU controlled functions like start, stop
LW0 - 1	Low write enable 0-1 for the RAM's
LWEDA	Low write enable DAC set the frequency calibration DAC into the write mode
MEMSEL	Memory select chooses the flag RAM or the qualifier RAM during the selftest
MDI0-7	Memory Data Input 0-7 for the Qualifier RAM
PEXTCLK1	External Clock line from input pod
PEXTCLK2	External Clock line from external BNC
PEXTREF	External Reference line

PCONTINUE	CONTINUE function
PJMPA	JumpA function
PJMPB	JumpB function
PODTHR	Programmable input pod threshold
PSTART	START function
QD0 - QD7	Qualifier Data output 0-7
TRIST	TRISTATE line
TRISTON	TRISTATE ON disables the data output pods
TRISTOFF	TRISTATE OFF enables the data output pods

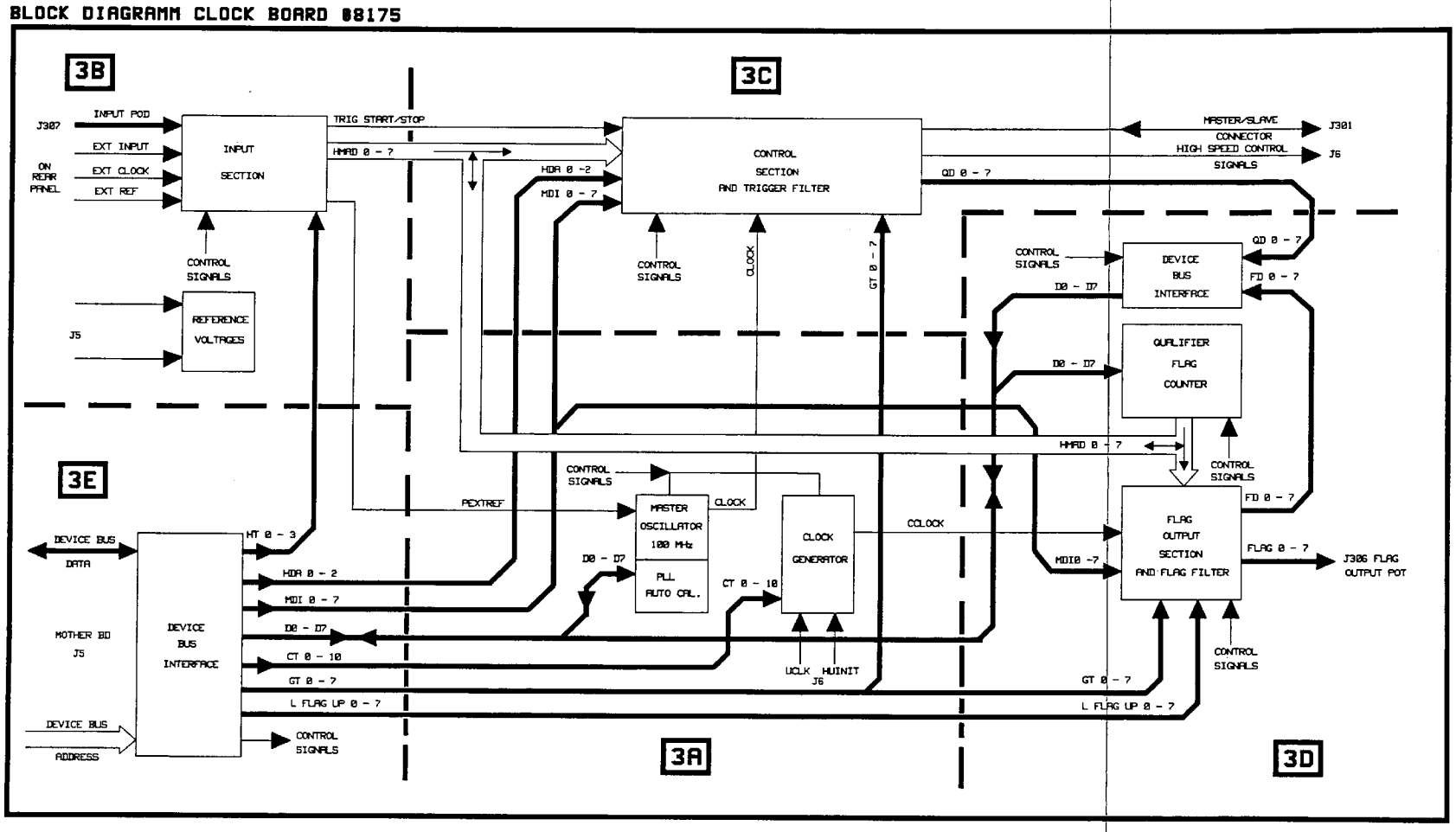


Figure 8-3-1. Clock Board Block Diagram

TROUBLESHOOTING

General

Should a fault be isolated to the Clock Board (A30), the theory of operation should be read and understood before proceeding with troubleshooting in this area.

CAUTION

Instrument must not be operated without cover over power supply and fan areas!

Procedure:

With power OFF, disconnect the three 50Ω input cables which can be seen going into the side of the board. The cables are:

J303 EXT. INPUT (yellow, shrink tubing), J304 EXT. CLOCK and J305 EXT. REF (black, shrink tubing). Remove the board (use the supplied board extractors) and plug it into the test (service) connector. This is accessed by removing the cover plate MP9.
Switch power ON. After a few seconds the System Page Configuration Menu should appear.

If an error message is displayed, press any key to continue. If possible, Recall Standard Settings.

1. First check with DVM that the Power Supply and reference voltages at TP's and components indicated as follows are correct. (Connect DVM low terminal to thhe GND Testpoint on this board as near as possible to TP14).

TP	+15V	+ 15.00V	± 50mV
TP14	+15V Ref.	+ 5.005V	± 5mV
C72	+15V Osc	+ 14.8V	± 200mV
C74	+5V Ref Osc	+ 5.00V	± 200mV
TP	+5V	+ 5.00V	± 50mV
Q50 Emitter	+4V	+ 4.00V	± 200mV
TP	15V	- 15.00V	± 50mV
C73	-15V Osc	- 13.0V	± 200mV
C78	-5V Ref	- 5.00V	± 200mV
TP	-5V	- 5.1V	± 50mV
C71	-5.2V Osc	- 5.0V	± 200mV
Q51 Emitter	-4V	- 4.0V	± 200mV
R100/101		+ 1.4V	± 200mV

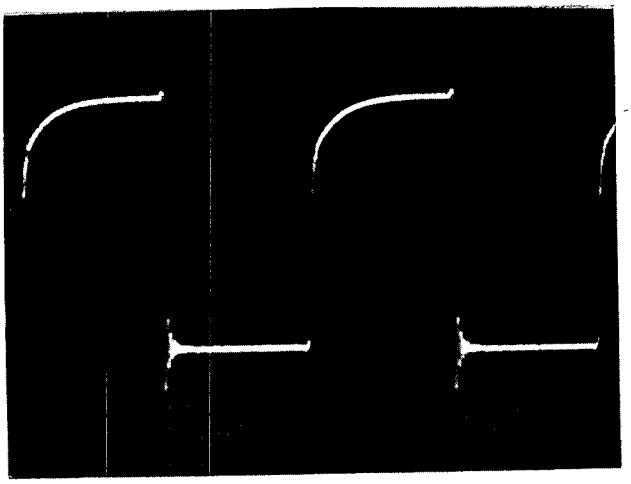
2. Set 8175A: Control Page (PAR)
   Mode: [Auto Cycle] [asynchron] startable

Measure HLOCK PLL at U68/9, 10, 11 = +5V ([asychron])
= +0.152V. ([sychron])

Measure with 10017A Probe at TP7, the 1 MHz Ref Crystal Oscillator signal.

Scope settings:
0.2usec/Div.
0.1V/Div.

TP7
1 MHz Ref
Cryst Osc.



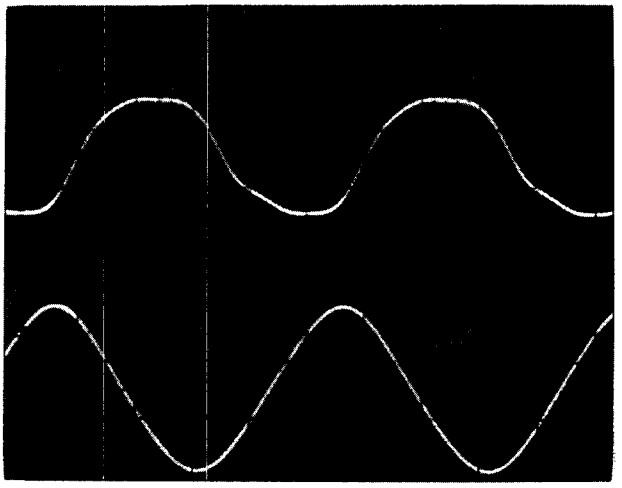
Measure with 10017A Probe at TP8, the 100MHz Master Clock and the Clock Signal U61C/15.

Scope settings:
0.02usec x 10/Div.
0.05V/Div.

To measure the Clock Signal:
Press 8175A START
Check that same signal produced at U90B/7.

TP8
100 MHz
M. Clk

U61/C15
Clk Sig.

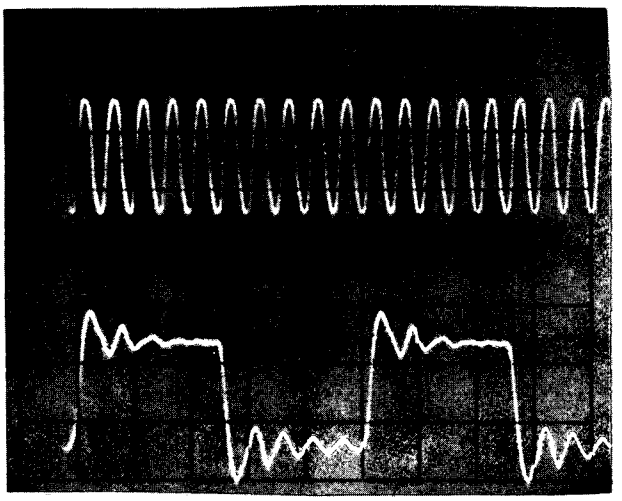


Measure with 10017A Probe, the signal at U65/15 compared to the 100 MHz Master Clock. The signal frequency should be the Master Clock divided by 10 as shown in the photograph.

Scope settings:
0.02us/Div.
0.05V/Div.
(Trigger on the slow signal)

100 MHz
M. Clk

U65/15.

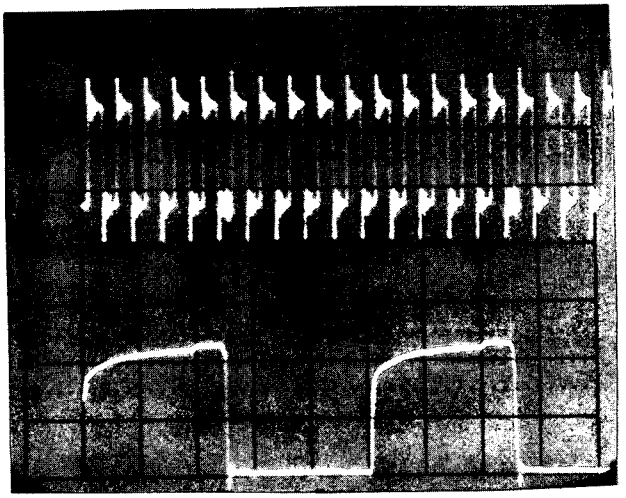


Measure with 10017A Probe, signal at U69/9 compared to the signal at U65/15.
The signal frequency should be the Master Clock divided by 100.

Scope Setting:
0.2us/Div
V/Div: 0.05V for U65/15 signal
0.2V for U69/9 signal
(Trigger on the slower signal)

U65/15

U69/9

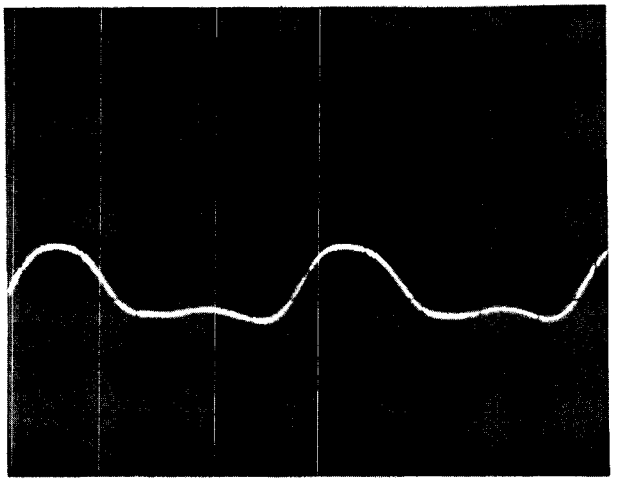


Measure with 10017A Probe the UCLK signal at U92/13.

Scope settings:

0.02x10us/Div.
0.05V/Div.

U92/13



Check with 10017A Probe the following signals:

CL0 U201A/3, CL1 U201A/4, CL2 U201/2

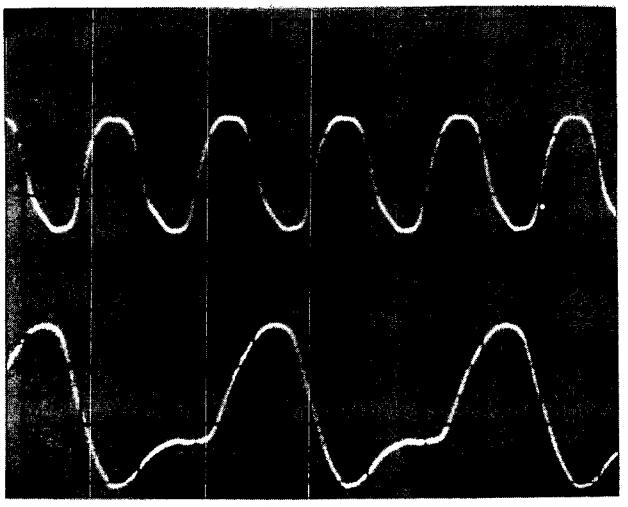
Set 8175A:

Control Page (PAR)
Clock: [on]
START

Measure with 10017A Probe, the signal CCLK compared to the 100 MHz Master Clock the CCLK signal.

Scope Settings:
0.05us x 10/Div.
0.05V/Div

100 MHz
M.Clk



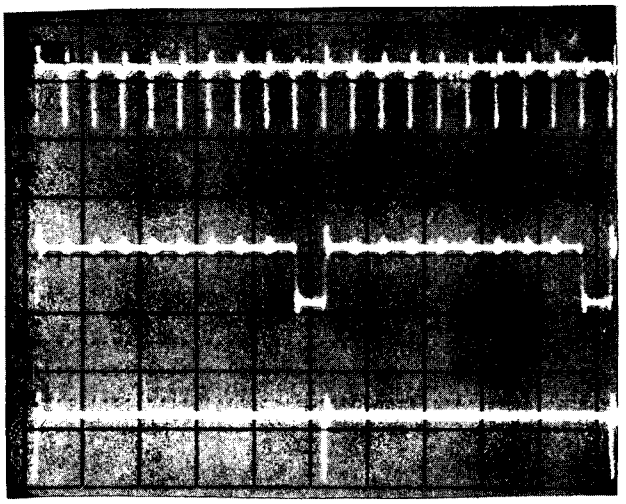
Change Resoultion from [10ns] to [1us], >START and:
check signals U209/3 and U209/14 and U201/12, 13, 14.
CTR signal will go to ECL 0.

Scope Settings:
0.2usDiv.
0.1V/Div.

U209/3

U209/14

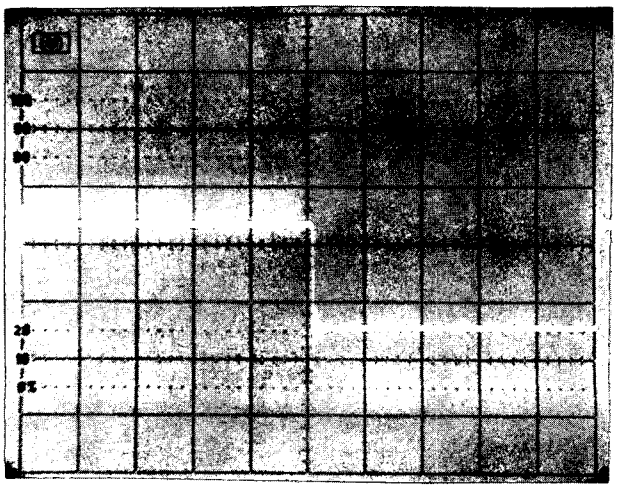
U201/12, 13, 14



CCLOCK signal
0.2us/Div.
0.05V/Div.

Measure for same signal at TP13
(HCLOCK OFF U45/11 = low)

TP13



With 8112A signal: PER 1us HIL +4V
DTY 50% LOC 0V

supplied to the EXT INPUT Connector (J303 TRG).

Measure the signals at TP6 compared to ECL signal at TP16 with 8175A settings:

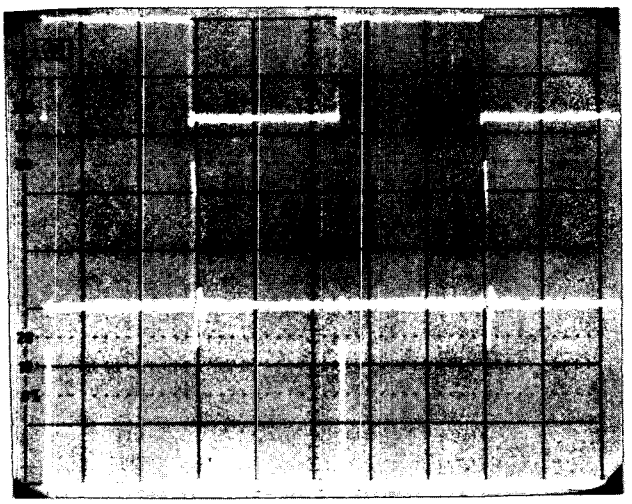
Control Page (PAR)
1. with START on [↑ and STOP on ↓] Edge
2. with START on [↓ and STOP on ↑] Edge

Scope Settings:
Time/Div 0.2us
V/Div 0.05

TP16

1.

2.



Measure the ECL signals at TP5 compared to the TP16 signal, with 8175A setting:

Clock Page (PAR)

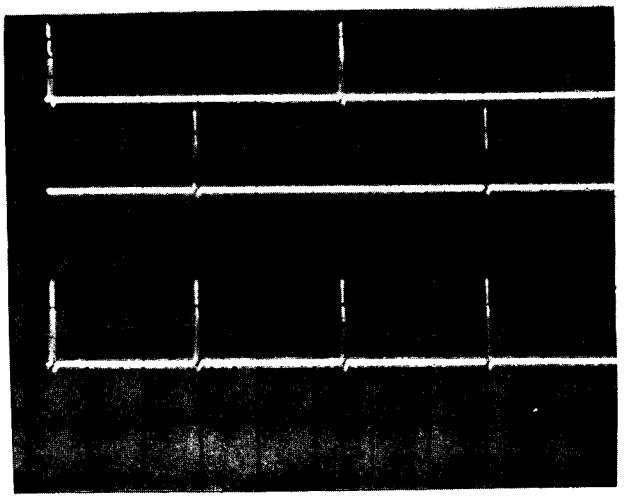
1. with START on [↑] Edge
2. with START on [↓] Edge
3. with START on [↕] Edge
4. with START on [↑STOP on↓] Edge
(same signal as 1.)
5. with START on [↓STOP on↑] Edge
(same signal as 2.)

Scope Setting
Time/Div 0.2us
V/Div 0.1

1.

2.

3.

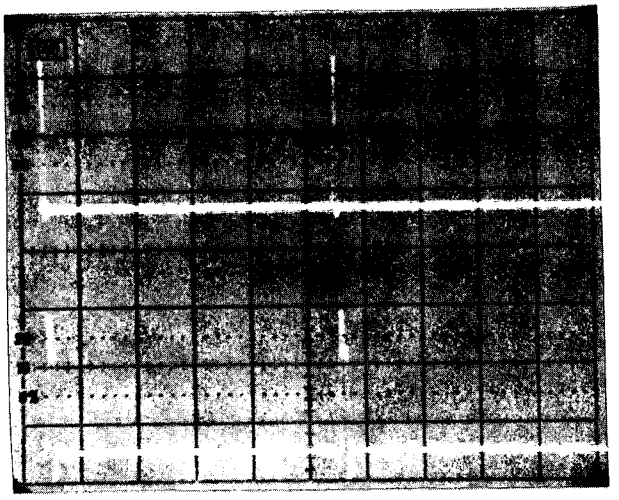


Measure with 10017A Probe at TP5, the PTRIG START signal and signal at U90D/12. Check for same signal at U90A/5.

Scope Settings:
Time/Div 0.2us
V/Div 0.05

TP5

U90D/12
U90A/5



Measure at U54 und U55, the signals HTO - HT3, as listed in Table 8-3-2.

Table 8-3-2.

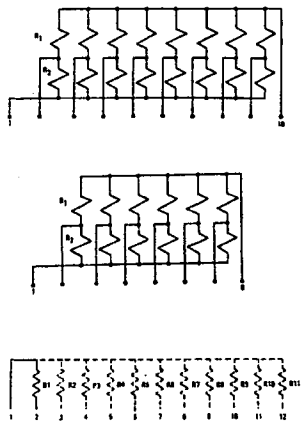
Function	U55A/5 HT3	U55B/7 HT2	U54B/7 HT1	U54A/5 HTO
no action	-0.4	-0.4	-0.4	-0.4
START on ↑ Edge	-0.4	-5.0	-0.4	-0.4
START on ↓ Edge	-0.4	-5.0	-0.4	-5.0
START on ↕ Edge	-0.4	-5.0	-0.4	-5.0
START on ↑ STOP on↓	-0.4	-5.0	-5.0	-0.4
START on ↓ STOP on↑	-5.0	-0.4	-0.4	-5.0

(Refer also to Adjustment Procedure Clock Board!)

REF.DES.	-5.2V	+5V	-15V	+15V	GND
U59	8				U6
U60	8				U6
U61	8				U6
U62	8				U6
U63	8-5VOSC				6,7
U64	8				U6
U65	8				U6
U66		14	11	4	7
U67					
U68	7	14			6,8
U69		14			7
U70		14			7
U71		14			7
U72		14			7
U73		14			7
U74		14			7
U75		14			7
U76		14			7
U79	8				U6
U92	8				U6
U201	8				U6
U202	8				U6
U203	8				U6
U204	8				U6
U205	8				U6
U206	8				U6
U207	8				U6
U208	8				U6
U209	8				U6
U210	8				U6
U211	8				U6
U212	8				U6
U213	8				U6
U214	8				U6
U215	8				U6
U216	8				U6
U217	8				U6

RA	POWER PIN	VOLTAGE LEVEL	RESISTOR VALUE
57	1	-5.2V	10 PIN 160/240
60	1	-5.2V	10 PIN 160/240
61	1	-5.2V	8 PIN 160/240
62	1	-5.2V	7x330
63	1	-5.2V	8 PIN 160/240
64	1	-5.2V	8 PIN 160/240
203	1	-5.2V	10 PIN 160/240
204	1	-5.2V	10 PIN 160/240
205	1	-5.2V	10 PIN 160/240
215	1	-5.2V	8 PIN 160/240
221	1	-5.2V	8 PIN 160/240
223	1	-5.2V	8 PIN 160/240

NOTE
e.g.
XX-XX
SEE PARTS VALUE TABLE FOR MORE INFORMATION
PIN NUMBER OF RESISTOR PACK
RESISTOR PACK NUMBER (RN)
ECL LINE BEING PULLED DOWN



Service

P/O A30 CLOCK BOARD 08175-66530

CLOCK GENERATOR

100MHz MASTER CLOCK GENERATOR

CLOCK SOURCE SELECTION

FREQUENCY DIVIDER

PHASE/FREQUENCY COMPARATOR

REF CRYSTAL OSCILLATOR

VCO

AUTOCAL CIRCUIT

ANALOG SWITCH

LOOP FILTER

RANGE COUNTER

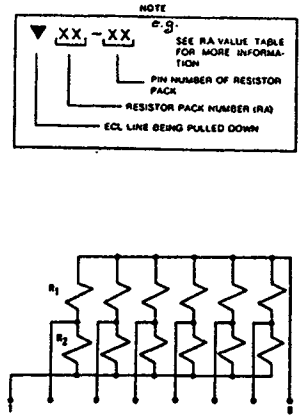
HIGH RESOLUTION COUNTER

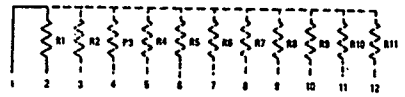
3A

8-131

REF.DES.	-5.2V	+5V	-15V	+15V	GND
U50	5				4,10
U51	5				4,10
U52			4	8	
U54	8				1,16
U55	8				1,16
U57	8				1,16

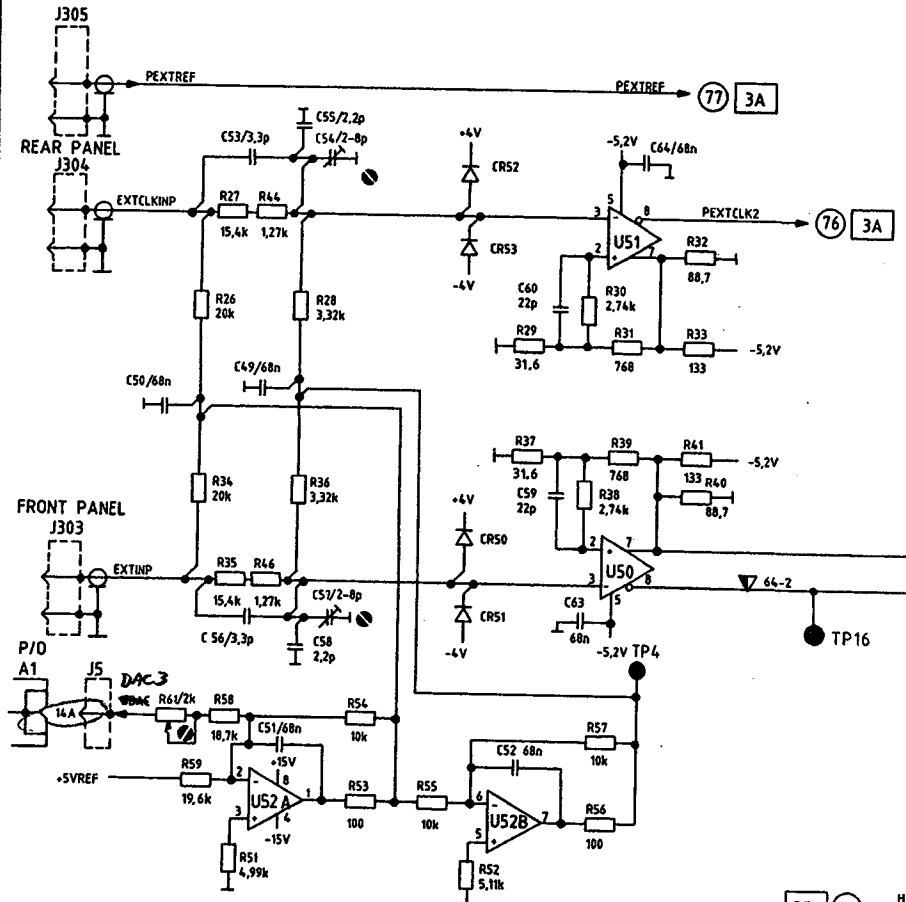
RA	POWER PIN	VOLTAGE LEVEL	RESISTOR VALUE
50	1	-5.2V	7x330
63	1	-5.2V	8 PIN 160/240
64	1	-5.2V	8 PIN 160/240



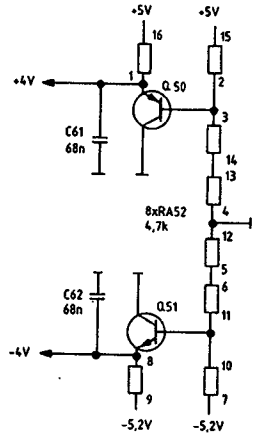


P/O A30 CLOCK BOARD 08175-66530

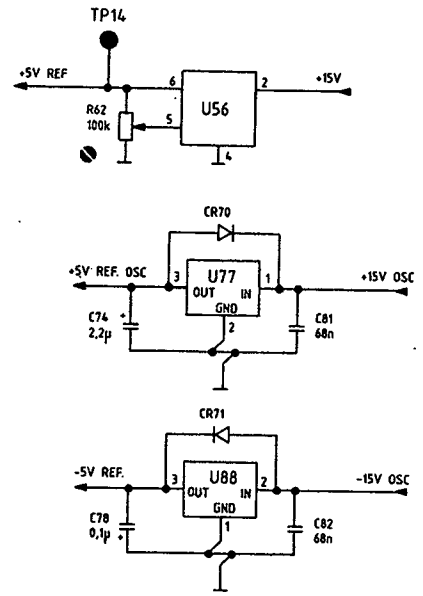
INPUT SECTION

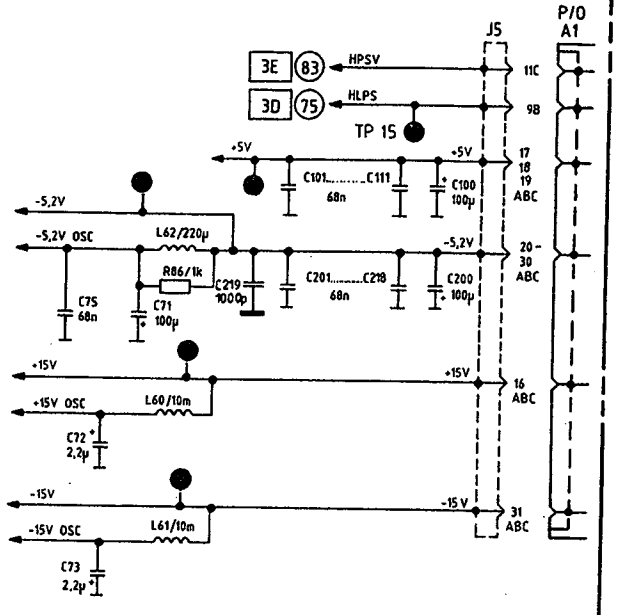


CLAMPING CIRCUIT

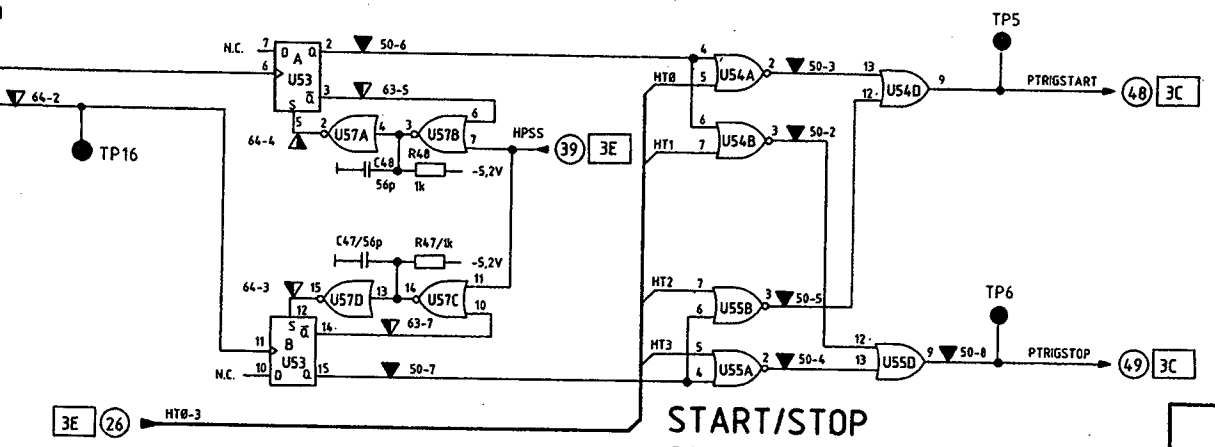


REF. VOLTAGES





START/STOP SELECTION



3B

REF.DES.	-5.2V	+5V	-15V	+15V	GND
U1	8				16
U2	8				16
U3	8				16
U5	8				16
U7	8				16
U8	8				16
U9	12				24
U10	12				24
U11	8				16
U12	8				16
U14	8				16
U16	8				16
U17	8				16
U18	8				16
U19	8				16
U20	8				16
U21		4	2		
U80	8				16
U81	8				16
U82	8				16
U83	8				16
U84	8				16
U86	8				16
U89	8				16
U90	8				16
U92	8				16
U93	8	16			8
U94	8				16
U303	8				16

RA	POWER PIN	VOLTAGE LEVEL	RESISTOR VALUE
3	1	-5.2V	7x470
4	1	-5.2V	10 PIN 160/240
5	1	-5.2V	8 PIN 160/240
7	1	-5.2V	7x470
8	1	-5.2V	10 PIN 160/240
9	1	-5.2V	10 PIN 160/240
10	1	-5.2V	8 PIN 160/240
11	1	-5.2V	7x470
12	1	-5.2V	7x1K
13	1	-5.2V	7x1K
14	1	-5.2V	7x1K
15	1	-5.2V	8 PIN 160/240
17	1	-5.2V	10 PIN 160/240
18	1	-5.2V	8 PIN 160/240
80	1	-5.2V	10 PIN 160/240
81	1	-5.2V	8 PIN 160/240
83	1	-5.2V	9x330
84	1	-5.2V	9x330
85	16	-5.2V	15 X 470
86	1	-5.2V	8 PIN 160/240
87	1	-5.2V	8 PIN 160/240
203	1	-5.2V	10 PIN 160/240

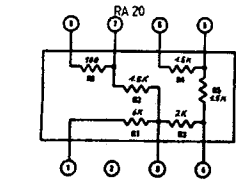
08175-66531

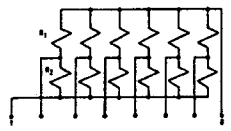
REF.DES.	-8.2V	+5V	-15V	+15V	GND
U300	8				16
U301	8				16
U302	8				16

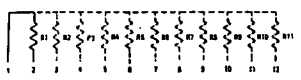
RA	POWER PIN	VOLTAGE LEVEL	RESISTOR VALUE
300	1	-5.2V	7x330

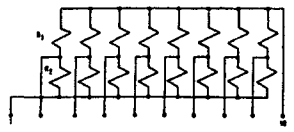
NOTE
C.D.
XX-XX
SEE RA VALUE TABLE FOR MORE INFORMATION
PIN NUMBER OF RESISTOR PACK
RESISTOR PACK NUMBER (RA)
ECL LINE BEING PULLED DOWN

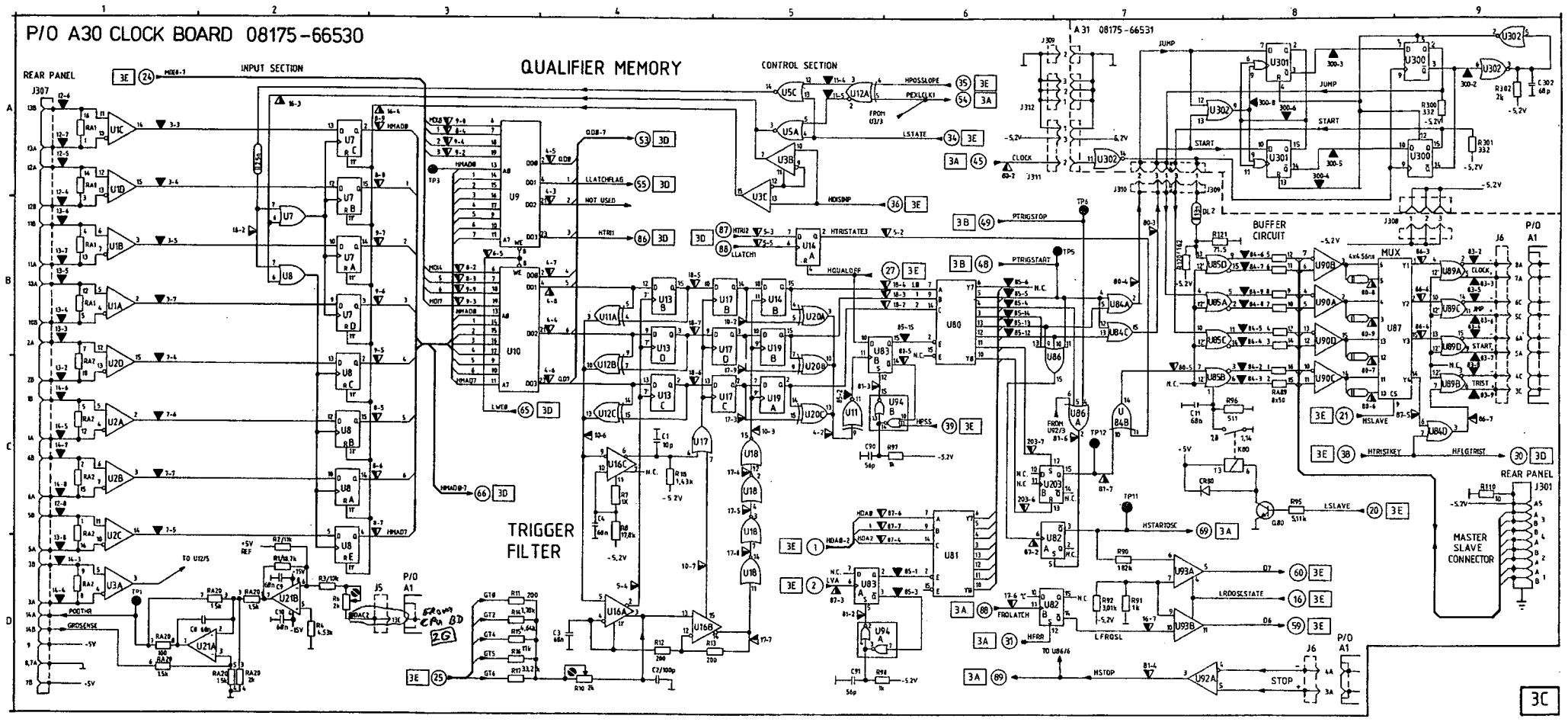
RA 20







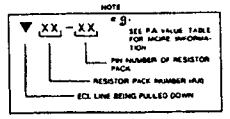


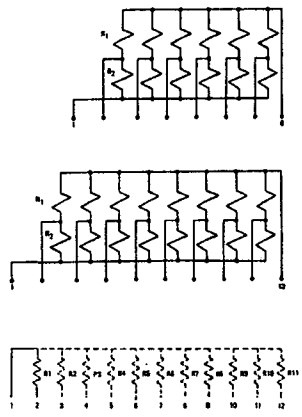


REF.DES.	-5.2V	+5V	-15V	+15V	GND
U5	8				1,16
U22	8				1,16
U23	8				1,16
U30	12				1,24
U31	12				1,24
U32	12	16			8
U33	12	16			8
U34	7	16			8
U35	7	16			8
U36	7	16			8
U37	8				1,16
U38	8				1,16
U39	8				1,16
U40	8				1,16
U41	8				1,16
U43	8				1,16
U44	8				1,16
U45	8				1,16
U46	8				1,16
U47	8				1,16
U48	8				1,16
U49	8				1,16
U119		16			8
U120		16			8

RA	POWER PIN	VOLTAGE LEVEL	RESISTOR VALUE
3	1	-5.2V	7x470
6	1	-5.2V	8 PIN 160/240
11	1	-5.2V	7x470
15	1	-5.2V	8 PIN 160/240
16	1	-5.2V	8 PIN 160/240
30	1	-5.2V	7x330
31	1	-5.2V	7X330
25	1	-5.2V	8 PIN 160/240
33	1	-5.2V	10 PIN 160/240
34	1	-5.2V	8 PIN 160/240
37	1	-5.2V	8 PIN 160/240
38	1	-5.2V	10 PIN 160/240
203	1	-5.2V	10 PIN 160/240
205	1	-5.2V	10 PIN 160/240

NOTE





Service

P/O A30 CLOCK BOARD 08175-66530

FLAG QUAL COUNTER

FLAG MEMORY

FLAG OUTPUT SECTION

OUTPUT LATCHES

OUTPUT DRIVERS

REAR PANEL J306

FLAG FILTER

TP3

TP13

FDB-7

FLAG UP B-7

MEMSEL

LRD MEM

LCLKOFF

LFLAGUP

LFLAGUP7

LFLAGUP8-7

LADDCLK

LLDMEMADD

LWB

LWE1

LWEB

MMADB-7

HMAD1

HMAD5

HMAD4

HMAD7

HMAD3

HMAD2

HMAD6

HMAD0

LLATCH1

LLATCH FLAG

HTRI1

HTRI2

CCLOCK

HFLGTRIST

HFLAG UP

HCLOCK OFF

TRISTATE

FLAG UP8

FLAG0

FLAG1

FLAG2

FLAG3

FLAG4

FLAG5

FLAG6

FLAG7

3D

REF.DES.	-5.2V	+5V	-15V	+15V	GND
U100		16			8
U101		16			8
U102		16			8
U103		20			10
U104	8	9			16
U105	8	9			16
U106	8	9			16
U109	8	9			16
U110		14			7
U111		14			7
U112		16			8
U113	12	3			
U114	12	3			
U115		20			10
U116	12	3			
U117	12	3			
U118		20			10
U121		14			7
U122	12	3			
U123	12	3			
U124		16			8
U125		16			8
U126	12	3			
U127	12	3			
U128		20			10
U129		20			10
U130		20			10
U131	4	9			16
U132	12	3			
U133	12	3			
U134	12	3			

RA	POWER PIN	VOLTAGE LEVEL	RESISTOR VALUE
7	1	-5.2V	7x470
200	16	GND	15x1K
102	16	GND	15x1K
200	16	GND	7x1K
201	16	GND	7x1K
223	1	-5.2V	8 PIN 150/240

NOTE
*3: SEE RA VALUE TABLE FOR MORE INFORMATION
XX - XX
PIN NUMBER OF RESISTOR PACK
RESISTOR PACK NUMBER #XX
ECL LINE BEING PULLED DOWN

16 9
1 8

service

P/O A30 CLOCK BOARD 08175-66530

DEVICE BUS INTERFACE

SUBDECODER

MAIN DECODER

BUS TRANSCEIVER

DATA
BOARD

SERVICE BLOCK 4
DATA BOARD

INTRODUCTION

The main function of the Data Board is to generate the data and timing information for the 24 data channels. Program related settings are also produced by this board. There are 24 data channels, with a memory depth of 1024 bits. The memory can be looped via a program. The program memory has a depth of 256 steps. The four entry points can be activated either by the MPU or by an external trigger event.

Pattern durations are programmable from 20ns up to max 9.99 sec with a resolution of 10ns, 1us, 100us or 10ms.

Block Theory

The Data Board comprises thirteen functional blocks or sections. These are listed below and can be identified by referring to the block diagram Figure 8-4-1. A table (Table 8-4-1) listing/explaining all the mnemonic used in this service block, is included at the end of the theory section. The order of presentation of the blocks as listed below is also used in the detailed theory of operation. The functions are grouped as shown on the block diagram/schematics.

Device Bus Interface

Interrupt logic/Initialization logic
Vector Memory
Program Counter
Program Memory
Address Counter

Timing Memory
Clock Generator
Timing Generator

Data Memory
Serializer
Line Driver

MUX/Vector Latch

Detailed Theory of Operation

DEVICE BUS INTERFACE (Schematic 4A)

The device bus interface is the connection circuit between the MPU and the circuits of the Data board. The 8 bit bidirectional data bus - HDD0 to HDD7, the 6 bit unidirectional address bus - HDA0 to HDA5, and the 5 bit unidirectional control bus are connected to this board via J7 (Device Bus).

All inputs and outputs are TTL compatible. LDBV is the most important control bus signal. With LDBV low, the data and addresses on the device bus are valid. The incoming data bus is buffered by the octal bus transceiver U91. The otputs from the TTL data bus (D0-D7) are then transformed by U95, U96 into ECL compatible signals (HD0-HD7).

All signals required by the Data Board circuits are decoded by the decoders U92, U93 and the D-Flip-Flops U99, U100. The outputs of these devices are also transformed into ECL compatible signals via U97, U98, U104, U107, U108 and U109. The decoders U105 and U106 (ECL 1 of 8 Decoders) generate the write-pulses (LW0-9) for the memories of the data board.

INTERRUPT LOGIC (Schematic 4B)

The incoming differential signals START and JUMP (from the Clock Board) are amplified by line receiver U1. The NOR Gates U76 A-C generates then the new signals PSTART, PJUMPA and PJUMPB. These three signals are the data information for the Flip Flops U73A, B and U74A. Also, a change on the START or JUMP-Signal generates via U66D/14 and U66A/2, the clock signal for the Flip Flops U73A, B and U74A. The delay between a change of START or JUMP and the positive going edge of the clock from U66A/2, is generated by the propagation delay of the two NOR-Gates U66 and the components R31, R66 and C54. R66 enables the delay between START and JUMP A/B to be adjusted to 18 ns (Testpoint 12 to 11). U73A/B and U74A store the START or JUMP A/B event. The outputs of these Flip-Flops address the Vector-Memory, and generate via U82B the signal HTRIG (TP11). U81A/B and U82A disable the Flip-Flops for a new event until the current one is completed.

The outputs of U77A, B, C (HSTARTAD, HJMPAAD and HJMPBAD) are the address lines for the vector memory. These lines are accessible either by the interrupt-logic U73A,B or U74, by the MPU U74A via the device bus interface (HSETSTART, HSETJMPA and HSETJMPB).

INITIALIZATION LOGIC (Schematic 4b)

Refer to Figure 8-4-2 when reading the following explanation. The signal HTRIG (U82B/15) goes high after a trigger event occurs. The next positive going edge of the 100MHz Clock (TP7) at Flip Flop U74B/11, will enable the Initialization Logic U71 and U72. HINT (U74B/15) goes high and a new trigger event (START/JUMPA,B) is prevented via U66A/5. The rising edge of HINT also sets both Flip Flops in U85. The outputs of these Flip Flops are HUCLKSTOP (U85/3) and HDCLKSTOP (U85/14). With these signals high, the clock output of the user clock UCLK (U39/7) or the Data Board clock (PTIMECLK) TP6 is switched off via Clock Generator U33A/B (Schematic 4C).
The third clock edge of the 100MHz Clock generates the reset signal HUINIT (U37/6,7) for the user clock counter of the Clock Board. Also, the signals HINIT and LINIT go true. If LINIT is low, the Program Counter is enabled for parallel load via U65/2. The same applies to the Address Counter and the Block Length Counter via U51/2. When HINIT is high, the parallel load for the timing counter is enabled via U21 and U18. HINIT high also controls the address clock LADDEN and the program clock LPRGEN, via U76 and U77 (Schematic 4A).

With these signals high, the Initialization Logic generates on the fourth clock edge, the signal PPRG (U79B/4). Signal PPRG clocks the parallel information of the Vector Memory in the Program Counters.
On the sixth clock edge, PADD2 loads the parallel information of the Program Memory into the Address Counters via signal PADDCLK1 and PADDCLK2 (TP4). Signal HADDS (U80A/5) is the reset signal of the Timing Counter (Schematic 4C) and the Serializer Control Unit U22 (Schematic 4D). If PADD2 occurs, the latch output U35 is disabled via signal HLATCHDIS = high.
The seventh clock edge generates the signal HJMPR (U80C/11). This signal resets U52 and the Flip Flops U73 and U74 via U81 and U82. A new trigger event is now possible. HINIT, LINIT and HTRIG will also be reset.
The eighth clock edge stops the whole Initialization Logic because HINT goes low. HLATCHDIS and HDCLKSTOP are reset for normal working conditions of the Data Board.
Note that, the fifth clock edge reset the HUCLKSTOP signal. Therefore, the Clock Board will get four clock edges more than the Data Board.

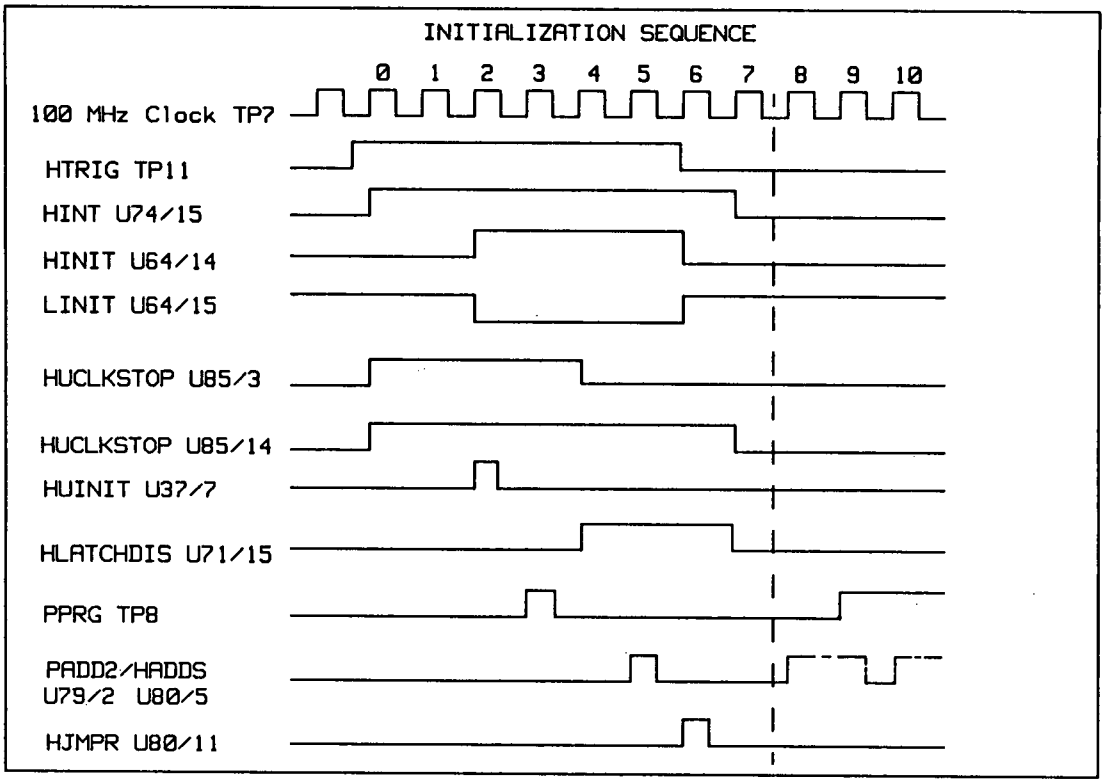


Figure 8-4-2. Initialization Sequence

VECTOR MEMORY (Schematic 4B)

HSTARTAD addresses the start vector, HJUMPAAD and HJUMPBAD addresses the jump vectors in the Vector Memory by the MPU. New information is written into the Vector Memory by addressing the desired vector and then by selecting LW8 or LW9 (U99 Schematic 4A).

PROGRAM COUNTER (Schematic 4B)

The parallel data inputs for the program counters (U60-U63) are 8 bit words, derived from the Vector Memory U67-U70. The outputs of the counters U60/U61 are also 8bit words (PMA0-PMA7) and represent the addresses for the Program Memory U185-U189. U62 and U63 are loaded with the block-length program, in (1 complement) because they are up counters. U64 and U65 are responsible for the parallel loading of the program counters. At the end of the inialization cycle the parallel load mode will be finished, by setting LINIT (U64B/15) high. In normal use LPRGSETUP is low.

The program counters are resetable via HPRGR (schematic 4A 38) going high. In "count mode" HPRGR is low.

Signal LPRGLOAD (U65/2) goes low, if either:
- LPRGSET UP (Device Bus Interface 4A 25) or,
- LINIT (Initialization logic U64B/15) or,
- the borrow outputs TC (U62/4 and U63/4) are low.

LPRGLOAD low, indicates parallel loading of the program counters.

The counters will then store the parallel data of the Vector Memory synchronously with the next positive going edge of signal PPRG (U79B/14). The signal LLASTBLK of D-Flip-Flop U64A/2 indicates: "last program block in process".

If signal HPRGSSEN at U64A/4 is high, LLASTBLK goes true each time. This means, the Program single step mode is turned on. In normal use (autocycle and singlecycle) HPRGSSEN must be low.

PROGRAM MEMORY (Schematic 4B)

Addressed by the Program Counter signal PMA0-PMA7, the program memory (U185 to U189) produces two 10 bit words. The data outputs of the RAM's are connected to the parallel data inputs of the Data-, Timing Address Counters (U41-43 and U47-U49) and the Block Length Counters (U44 to U46).

The first 10 bit word (PRAM0 - PRAM9) is the start address of the Data-, Time and Address Counters, the second one (PRAM10 - 19) is responsible for the block length.

To write new information into the memory, the write-enable signals LW5 or LW6 are used. If LW7 is addressed, the program counters will increment by one automatically for a new address of the Program Memory.

ADDRESS COUNTERS (Schematic 4B)

The outputs of the counters U41-U43 (DMA0 -9) and U47-U49 (TMA0 - 9) are connected to the address inputs of the Data and Timing Memory.
The Data Address Counters address the Data-Memory (Schematic 4D), the Time Address counters the Timing-Memory (Schematic 4C).
The Block Length is counted by U44-U46.
U50, U51 and U52A are the control circuits for the parallel loading of the Address Counters. All these counters are resetable via HADDR 4A 35 going high. In "count mode" HADDR is low. LADDLOAD1 (U50D/14) and LADDLOAD2 (U50C/15) low, indicates parallel loading of the counters. Both signals go low, if either LADDSETUP (Device Bus Interface 4A 32) or, LINIT (U64B/15) or, the borrow outputs TC (U46/4 and U45/4 and U44/4) is low. The counters will then store the parallel data of the Program Memory synchronously on the next positive going edge of PADDCLK1 or PADDCLK2. The parallel load mode will be finished, by setting LINIT high. In the "count mode" LINIT as well as LADDSETUP are high. Signal LLASTPAT (TP8) indicates: "Last pattern in process".

Because signal LLASTPAT is also the PPRG of the Program Counters U60-U63, a positive going edge of PPRG increments the Counters U60/U63.

TIMING MEMORY (Schematic 4C)

The Timing Memory size is 13 x 1kBit. It is organized as follows:

10Bit for the high resolution timing of 1024 possible steps
3Bit for the ranging.

The data-outputs of the Timing Memory (U140 - U152) are connected to the inputs of the high resolution counter (TRAM 0-9) and to the range counter (TRAM 10-12).

If LW4 is addressed, the address counters automatically increment by one.

CLOCK-GENERATOR (Schematic 4C)

The task of the Clock-Generator (U39, U1, U2. U9, U20, U33, U37, DL1 and DL2) is to generate clock signals for different parts of the Data and Clock Boards, and also to enable the Start/Stop-Mode (Single Cycle-Mode).

U1 is the Line Receiver of the Clock-Signal from the Clock Board. It gives the differential signal to U39. From U39 the 100 MHz Clock is first connected to the Initialization Logic U74 and U71 (Schematic 4B) and then via Delay Line DL1 to U33/9. DL1 has a fixed delay of 10ns. U33/3 together with U2/3 and U2/2 and R25/C50 generates a clock pulse with constant width of about 4ns.

DL1 with its 10ns delay, compensates the propagation delays of U71, U72, U74, U79 and U80 inclusive line delay.

The Clock, with constant width of 4ns, goes via Buffer U9 as PTIMECLK0 to U32/11. It also goes via printed delay lines of 0.8ns and U9 (PTIMECLK1), 0.8ns +2.5ns and U9 (PTIMECLK2 and PTIMECLK3) to different parts of the Data Board.

From U33/3, the clock signal goes via U39B/7 (UCLK), DL2 and U37B, back to the Clock Board. DL2 delays the clock UCLK by either 0ns, 5ns or 10ns, because the user clock edgs should occur after the data edge.

U20, U32A, U2 and R26/C51 are the STOP-Circuit of the Data Board.

When Single-Cycle is selected (via signal LSINGLCY), U20B/15 goes low if all other inputs LSERSTOP, LLASTBLK, LLASTPATT and LSTOP are low. The next positive going edge of PTIMECLK2 generates at U32/3 the signal HSTOPCLK. This signal immediately stops the Set-Input U33/5,12 the clocks of the Data Board and the Clock Board. Output U32A/2 stops the Oscillator of the Clock Board via U37A (STOP).

HSTOPCLK is reset by itself via the time responsible parts R26/C51 and U2 after about 80ns. This time is neccessary for the Clock Board to stop the Oscillator.

TIMING GENERATOR (Schematic 4C)

High Resolution Counter

The high resolution counter (U15-U17) is loaded with 10Bit information . The shortest programmable time is 20ns, the max. time is 10.24us with a resolution of 10ns. To enable the high resolution timing counter, signal LPERTC must be low. LPERTC goes low, either if the range counter is in use or if signal L10NS is low. L10NS is controlled by bit 12 of Timing Memory (TRAM12 U18A/7). The clock for the high resolution counter is PTIMECLK2. The Gates U19, 20 and 21 together with D Flip-Flop U18B generate the signal for the parallel loading of a new timing information. The counters U15-U17 and U18B divide the 100MHz clock by two for the shortest timing (20ns). For the max. timing (10.24us) the counters together with D Flip-Flop divide the clock by 1024. The D Flip-Flop U32B gets the timing information from U18B/15 via U23B and generates synchronously with PTIMECKL0 the signals:

PADDCLK1 (U32B/14) and PADDCLK2 (U39A/3).

These signals are necessary in order to get a new address for Data- and Timing Memories.
If PADDCLK2 via Buffer U39A goes high, U35 generates a latch signal LATCH , with a width of 3,5 ns, for the output latches of the Buffer- or Fine Timing-Board.

The signal LSTOP = low (U20A/2) indicates, that the last timing of a pattern is in process and the next clock edge will be the last one.

Range Counter
The range counter U3 to U8, U10, U11, U12 and U14 generates three timing signals: 1us, 100us and 10ms.
U14 combines these three signals with the information coming from decoder U29. The data source of this decoder is bit 10 (TRAM 10) and bit 11 (TRAM 11) of the timing memory latched by U30.
If, for example, signal L100us (U29/5) is low, U14 detects the 100us signal and the output signal (U14/2) LPERTC gets low for 10ns at a period of 100us. The high resolution counter is now the multiplicator by N of the desired timing range (N x 100us).
N will be loaded into the high resolution counter with the complement of the timing RAM's. HTIMELOAD (U18B/14) will synchronize the range counter with the high resolution counter.The Clock for the Range Counter is PTIMECLK1.

DATA MEMORY (Schematic 4D)

The Data Memory size is 24 x 1kBit. The data outputs DRAM3 -DRAM23 of the Data Memory (U153-U168) are connected to the inputs of the line drivers U132-U138. The outputs of U153-U168 are also connected to the serializer circuit (U25-U28). In Serial Mode the outputs of the Data RAMs U173-U176 are disabled. DRAM 0 - DRAM2 are OR connected with the outputs of the serializer via U131.

SERIALIZER (Schematic 4D)

The serializer is split into two parts:

- the shift registers U25-U28
- the control circuit U22, U23, U31, U34 and U38.

The shift registers U25/U26 are loaded with the data of U161-U168 (DRAM 8 - DRAM 15) and shift registers U27/U28 with the data of U153-U160 (DRAM 16 - DRAM 23). In serial mode the outputs of Data Memories U173-U176 are disabled, because the serializer outputs (SERCLK, SEROUT1 and SEROUT2) are OR connected with signals DRAM0 -DRAM2. The three functions (load parallel, shift and stop) of the shift registers are controlled via counter U22 and Gate U23B. The control circuit is initialized with signal HADDS, signal LTIMELOAD1 during the timing duration is in process. In the full clock Mode (timing generator is turned on), the shift register isn't stopped and generates a 100MBit serial data stream. Therefore, U22 controls the parallel loading of the shift registers. Clock of U22 and the shift registers U25-U28 is PTIMECLK3.

After each seventh shift movement in normal mode and after each fourth shift movement in full clock mode, a new pattern address will be clocked via (LSEREND) going low (U34/3). The Ex OR Gate U31 then generates the signal LSERSTP to stop the clock, if the single cycle mode is programmed.

LINE DRIVER (Schematic 4D)

The 24 outputs of the Data Memory (DRAM 0-DRAM 23) and the three outputs of the Serializer (SERCLK, SEROUT1 and SEROUT2), are connected to the line drivers U131-U138. The differential outputs are then connected via J8 to the high speed bus of the 8175A.

MUX (Schematic 4E)

The analog multiplexers (U111-U118 and U124-U126) are used to switch the data of the memories and the addresses of the counters to the ECL/TTL translaters (U120-U123).

Because the lines of the fast ECL-counters and the memories are optimized for high speed operation, these signals are sensed via R1-R11 and RA55-RA62 for good high frequency performance. The output lines of the translators (D0-D7) are connected to the Device Bus Interface (Schematic 4A), the MPU will be able to read the desired datas or addresses. The outputs of U120-U123 can also be in tristate mode. The selection of the desired data lines is done by writing a 3Bit word into the D-Latch U119.

VECTOR LATCH (Shematic 4A)

The vector latch (U200-U204) stores the currently running vector and the previous one. The incoming interrupt signals (HJMPAAD, HJMPBAD, HSTARTAD and VECLOAD) are transformed by U200 (ECL/TTL).

The encoded information of the current vector and the previous one, is latched by U201-U203. From ECL OR Gate U66 (Schematic 4D) via U200, a latch signal for U202 and U203 is generated by the ECL-Signals LPRGLOAD and PPRG. U204 is the connection between the vector latch and the Device-Bus-Interface (Schematic 4A).

Table 8-4-1. Mnemonics Explanation

The first letter of a mnemonic means:

N: active on the falling edge
P: active on the rising edge
H: active high state
L: active low state

Mnemonic	Explanation
100 MHZ	Main clock from Clock board.
D0 - D7	TTL DATABUS 0-7
DMA0-DMA9	Data-Memory Address 0 - 9.
DRAM 0-23	
HADDR	High Address Reset. It resets the Address-Counter.
HADDS	High Address Set. It enables the address load of the Address-Counter during interrupt.
HD0-HD7	High Data 0-7. ECL-Data bus on the Data board.
HDA0-HDA5	High Devicebus Address 0-5. TTL-Devicebus from the CPU board.
HDD0-HDD7	High Devicebus Data 0-7. TTL-Devicebus from/to the CPU board.
HDCLKSTOP	High Data Clock Stop. If this signal is high, the signals PTIMECLK0, 1, 2 and 3 are stopped.
HFULLCLK	High Full Clock. It enables the Serializer-Hardware of the Data board to generate a 100 MBit datastream.
HINT	High Interrupt. It indicates the Interrupt-Logic is on work.
HINIT	High Initialize. It starts the Interrupt-Logic.
HINITEN	High Initialization Enable enables the Initilization logic without trigger event.
HJMPR	High Jump Reset. It resets the Interrupt-Logic.

HJMPAAD	High Jump A Address addresses the Jump B Vector.
HJMPBAD	High Jump B Address addresses the Jump B Vector.
HLATCHDIS	High Latch Disable. If this signal is high during initialization, the LATCH output is disabled.
HPRGR	High Program Reset. It resets the Programm-Counter.
HPRGSSEN	High Program Single Step Enable
HSERIAL	High Serial. It indicates the Serial-Mode of the Data board.
HSETJMPA	High Set Jump A. It addresses the Jump A Vector of the Vector-Memory.
HSETJMPB	High set Jump B. It addresses the Jump B Vector of the Vector-Memory.
HSETSTART	High Set Startvector. It addresses the Start-Vector of the Vector-Memory.
HSTARTAD	High Start Address addresses the Start Vector.
HSTOPCLK	High Stop Clock stops the Clock on the Clock Board and the PTIMECKLS of the Data Board.
HSTOPUP	The same as HSTOPCLK, but it goes true via an MPU access of the Data Board Memories.
HTIMELOAD	High Time Load. It puts the High Resolution Timing-Counter in its parallel-mode. The next rising edge of PTIMECLK1 loads this Counter in parallel.
HTRIG	High Trig. If this signal goes high, a START or JUMPA,B is received.
HUINIT	High User clock Initialization resets the user clock circuit on the Clock Board
HUCLKSTOP	High User Clock Stop. If this signal is high, the clock of the user clock is stopped (low).
JUMP	Jump - Signal from the Clock board.
L08	L0 or 8 indicates that the shift register of the serializer must store a new byte before a new serialization.
L10NS	Low 10 NS. It indicates the highest speed mode of the Timing Generator.
L1US	Low 1 US. It indicates the 1 usec increment timing range of the Timing Generator.
L100US	Low 100 US. It indicates the 100 usec increment timing of the Timing Generator.
L10MS	Low 10 MS. It indicates the 10 msec increment timing of the Timing Generator.

LADDEN	Low Address Enable. It has the same function as LADDENUP, but it is generated by the Interrupt-Logic.
LADDENUP	Low Address Enable Up. It enables the Address Counter of the Data board for stepping by the MPU.
LADDLOAD1 and 2	Low Address Load1 and 2. They set the Address Counter in the parallel mode.
LADDSETUP	Low Address Set Up. It enables the Address-Counter to load the data from the Programm-Memory parallel, if addressed by the MPU.
LATCH	Latch, signal for the output latches of the Buffer or Fine Timing Board.
LCEN	Low Card Enable.
LCONTROLREG1 LCONTROLREG2	Low Control Register 1 and 2. They select the MPU access to Latches U99 or U100.
LDBV	Low Device Bus Valid. It indicates that data and address on the Device-Bus are valid.
LINIT	Low Initialization is the inverted signal of HINIT.
LLASTBL	Low Last Block. It indicates the last Programm Block is over.
LLASTPAT	Low Last Pattern. It indicates that the last pattern is in process.
LMEMSEL	Low Memory Select. It is the address for the selection of the desired memory or counter on the Dat board.
LMHS	Low Master/High Slave.
LPERTC	Low Period Terminal Count. It is the enable signal High Resolution Timing-Counter. If it is low, the next rising edge of PTIMECLK1 increments the counters.
LPRGEN	Low Programm Enable. It has the same function as LPRGENUP, but it is generated by the Interrupt Logic.
LPRGLOAD	Low Program Load. It indicates the parallel loading of the programm counters.
LPRGENUP	Low Programm Enable Up. It enables the Programm Counter hardware of the Data board for stepping by the MPU.
LPRGSETUP	Low Programm Set Up. It enables the Programm Counter to load the data from the Vector-Memory in parallel, if addressed by the MPU.
LREAD1-LREAD3	Low Read 1 - 3. They enable the MPU to read the Memories and counters of the Data board.

LRHW	Low Read / High Write.
LSEREND	Low Serial End. It indicates the end of the Serialization of one byte. This signal comes from the Serializer.
LSERIAL	Low Serial. - same function as HSERIAL
LSERSTP	Low Serial Stop indicates the STOP in Serial-Single-Cycle/Mode. This signal comes out of the Serializer.
LSINGLCY	Low Single Cycle. It indicates the Single Cycle-Mode of the Data Board.
LSTOP	Low Stop indicates the last clock of a pattern duration is received, a timing is done.
LTIMELOAD	Low Time Load. - same function as HTIMELOAD
LW0-LW9	Low Write 0 - 9. If addressed, writes the data on the ECL-Databus in the selected memory.
PADD1 and PADD2	Positive Address Clock 1 and 2. They come from the Timing Generator of the Data board and increment the Address-Counter, if the duration of a pattern is over.
PADDCLK1	Positive Address Clock1. It increments the Address Counter for the Timing-Memory.
PADDCLK2	Positive Address Clock2, It increment the Address Counter for the Data-Memory. It also generates the Latch-Pulse.
PADDSTEPUP1	Positive Address single Step. It increments the Address-Counter if addressed by the MPU.
PJUMPA	Positive Jump A. It executes the Jump A-Vector.
PJUMPB	Positive Jump B. It executes the Jump B-Vector.
PMA0-PMA7	Program Memory Address 0 - 7.
PPRG	Positive Program Clock. A positiv going edge of PPRG increments the Program Counters.
PPRGSTEPUP	Positive Program single Step. It increments the Program-Counter if addressed by te MPU.
PRAM0-PRAM19	Program RAM Outputs.
PRGSTEP	Program Step.
PSTART	Positive Start. It executes the Start-Vector.
PTIMECLK0,2	Positive Time Clock 0,2. They drive the Timing Generator of the Data board.
PTIMECLK1	Positive Time Clock 1. It drives the Range Counter of the Data Board

PTIMECLK3	Positive Time Clock 3. It drives the Serializer on the Data board.
SERCLK	Serial Clock. It indicates these clock edges which shift the parallel datas into serial datas.
SEROUT1 and 2	Serial Output 1 and 2. They are the outputs of the Serializer.
START	Start - Signal from the Clock board.
STOP	Stop. It disables the clock (100 MHz) on the Data board.
TMA0-TMA9	Timing Memory Address 0 - 9.
TRAM0-TRAM12	Timing RAM 0 - 12 These are the outputs of the Timing-Memory.
UCLK	User Clock signal of the userclock circuit.
VECLOAD	Vector Load. This signal writes the new vector in the vector latch and shifts the old one.

BLOCK DIAGRAM DATA BOARD 8175A

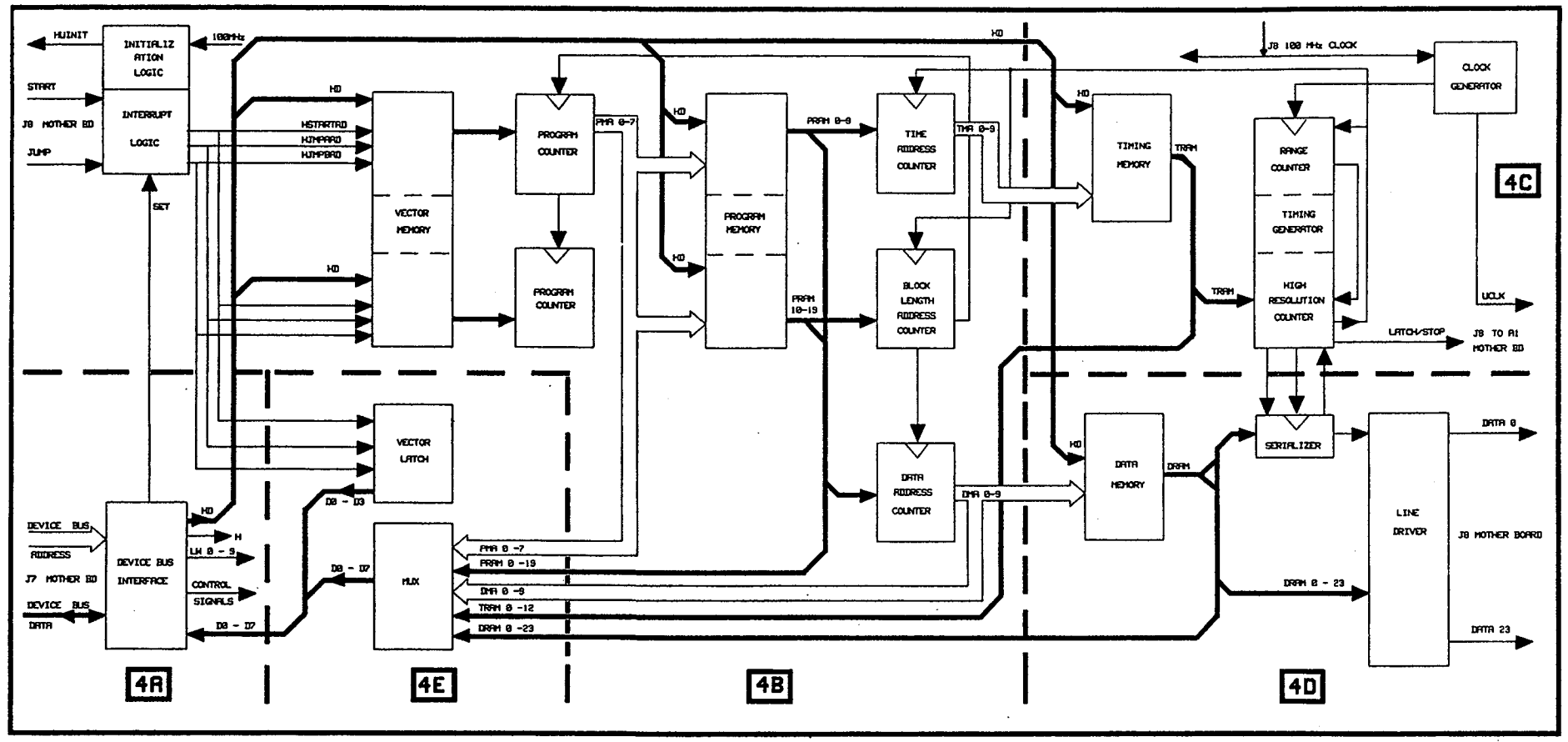


Figure 8-4-1. Data Board Block Diagram

TROUBLESHOOTING

General

Should a fault be isolated to the Data Board (A40), the theory of operation should be read and understood before proceding with troubleshooting in this area.

CAUTION

Instrument must not be operated without cover over power supply and fan areas.

Procedure:

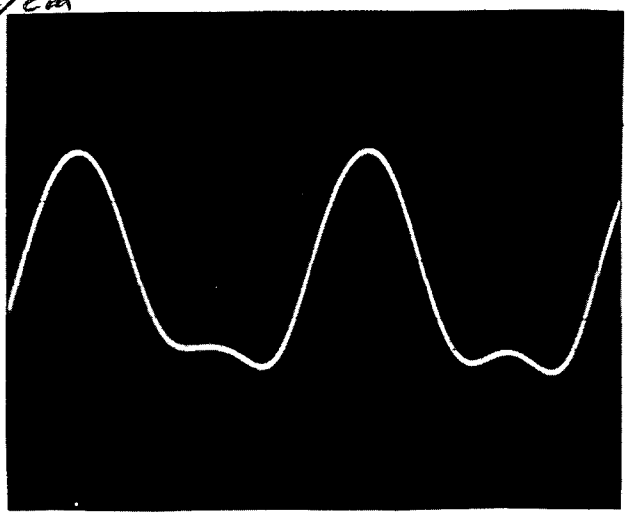
With power OFF, remove the Data Board (use the supplied board extractors) then plug it into the test (service) connector. This is accessed by removing the cover plate MP9
Switch power ON. After a few seconds the System Page Configuration Menu should appear.
If an error message is displayed, press any key to continue. If possible Recall Standard Settings.

1. First check with DVM that the Power Supply Voltages at the following TP's are correct.

TP +5V	+5.0V	± 50 mV
TP -5V	-5.1V	± 50 mV
TP -0.7V	-0.7V	± 100 mV
TP -1.3V	-1.3V	± 100 mV

2. On Control Page (PAR) change Mode: [Auto Cycle] > START .
Measure with 10017 Probe at TP7, the 100 MHz clock signal (ECL).

Scope Settings:
Time/Div 0.02us x 10 2 nsec/cm
V/Div 0.02
AC

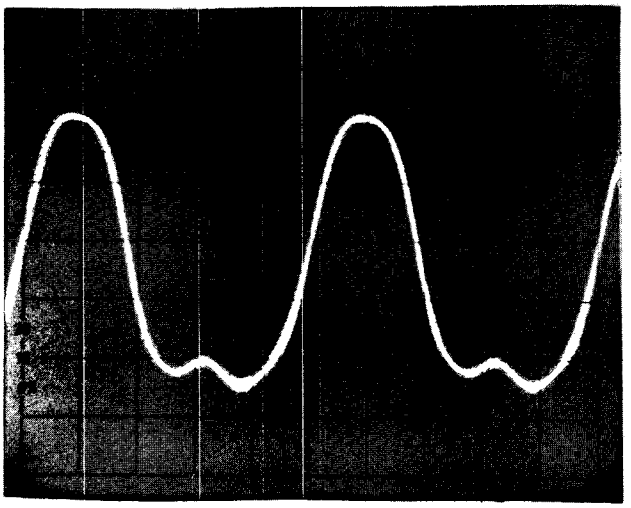


TP7
100 MHz

Measure with 10017A Probe at TP6. the P TIME CLK signal (ECL)

Scope Settings: as before

TP6
P TIME CLOCK



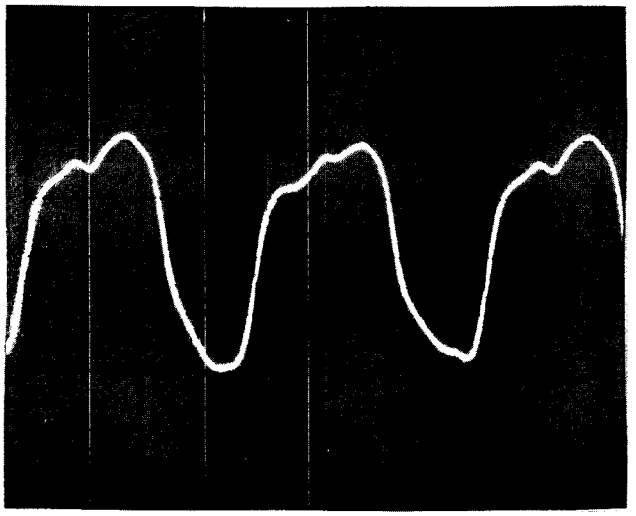
Check the signals at following devices (same waveforms as for PTIMECLK):

PTIMECLK0	U9/15	PTIMECLK2 U9/14
PTIMECLK1	U9/3	PTIMECLK3 U9/2

Measure with 10017A Probe at TP4, the PADDCLK2 signal (ECL)

Scope settings:
Time/Div 0.05us x 10 5nSec
V/Div 0.02
AC

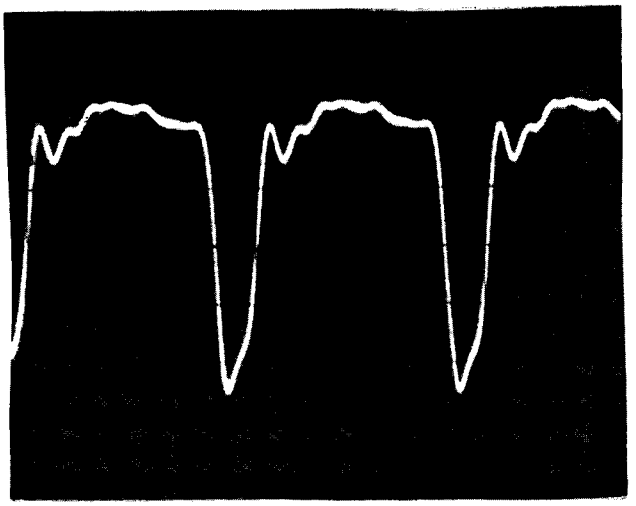
TP4
PADDCLK2



Measure with 10017 Probe at TP2, the LATCH signal (ECL)

Scope Settings: as before

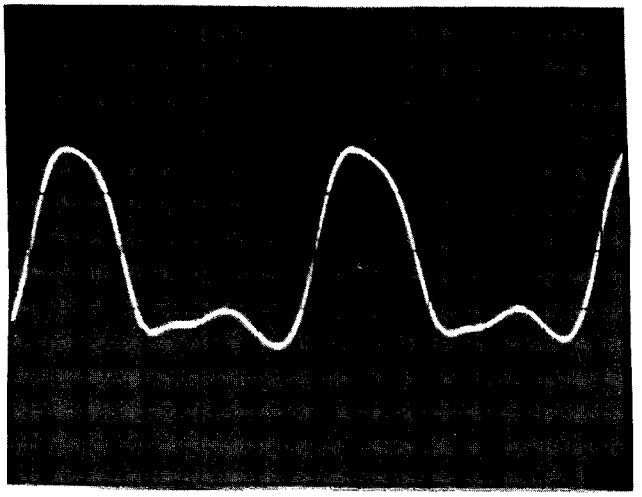
TP2
LATCH



Measure at TP10 the UCLK Signal.

Scope settings:
Time/Div 0.02 us x 10
V/Div 0.02
AC

TP10
UCLK

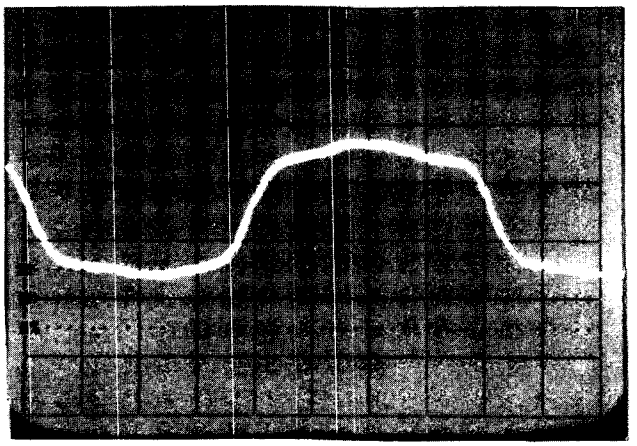


Set 8175A:

DATA > NEXT = Data [Pattern] Setup > CURSOR↓ = Address 0000 > CURSOR→ = POD2 CH7
> 1 24x > LOAD ALL ONES AT ADDRESS 0000
PRGM > CURSOR↓ = PROG1 > CURSOR→ = 1023 > 0001 >
blue > EXEC = UPDATE > START

Measure with 10017A Probe the DRAM 0-23 Signals at the respective test points. Refer to the board layout diagram to identify the test points.
Time/Div 0.05 us x 10
V/Div 0.05
DC

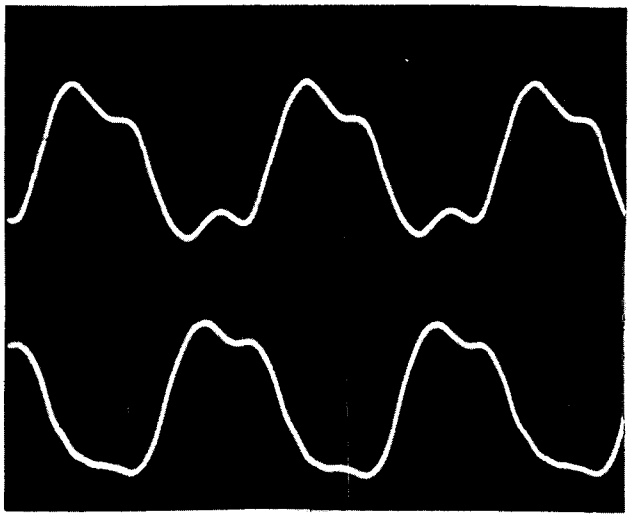
DRAM 0-23
SCHEMATIC 4D
IC U176 PIN 1,
U175 PIN 1,
ETC.



Measure with 10017A Probe the HTIMELOAD and LTIMELOAD signals.
Scope settings: as before.

U18/14
HTIMELOAD

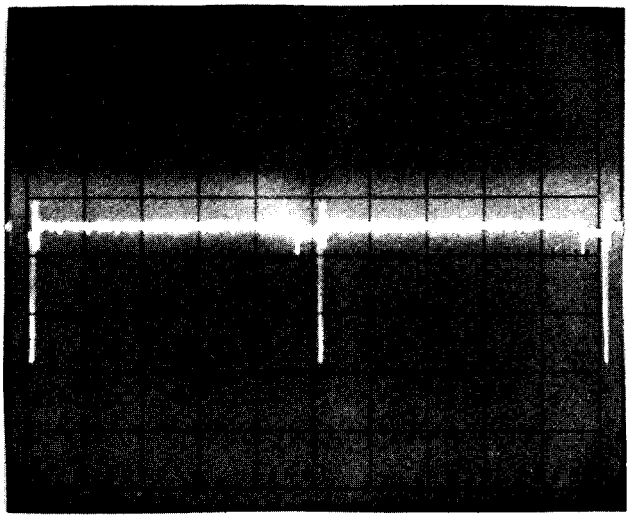
U21/3
LTIMELOAD



Set 8175A Data Page [Format] Allocation (PAR)
Period: 10 us

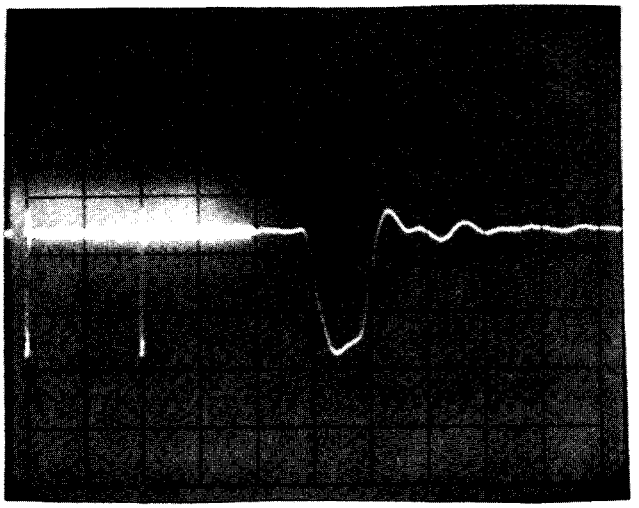
Measure via 10017A Probe at U11/12, the timing signal 1 us.
Set scope
Time/Div 0.2 us
V/Div 0.05
DC

U11/12



Measure via 10017A Probe the LPERTC Signal (U14/2).
(With signal L1us low, LPERTC goes low for 10 ns with a period of 1us).
Set scope
Time/Div 0.5 us
Delayed
Time/Div 0.01 us

U14/ .2



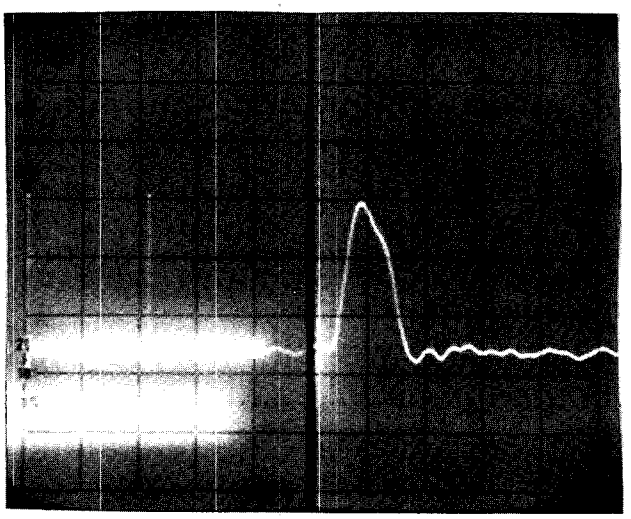
Check also that (with L1us low) HTIMELOAD goes high for 10 ns with a period of 10 us.

Set scope: U18-19

Time/Div 5 us

Delayed Time as before

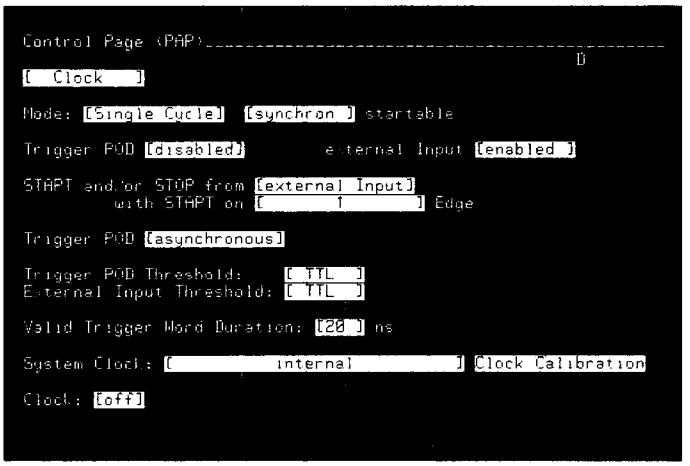
HTIMELOAD



Set 8175A:

[Clock] menu details to be as shown:

#1



Set 8112A:

Per 1.00 us	TTL/ fix
DEL min	HIL +2V
WID 30 ns	LOL 0V

Connect the 8112A output signal to the EXT INPUT BNC of 8175A.

GATED START POS

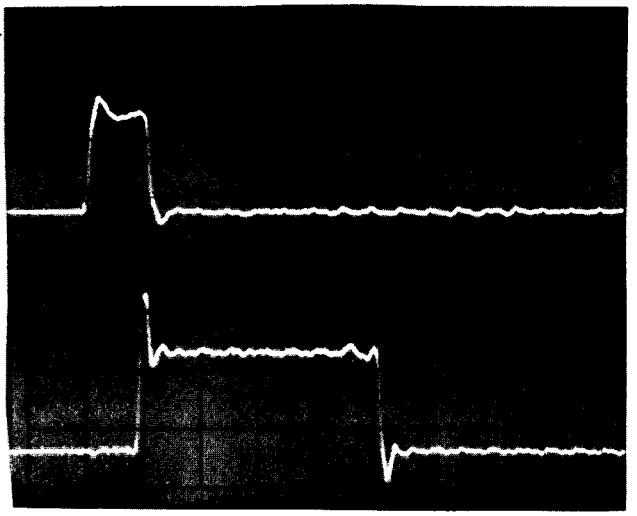
STOP NEG

WIDTH 160ns - 160ns

Measure with 10017A Probe the signal at TP12, and HTRIG signal at TP11
Scope settings:
Time/Div. 0.2 us x 10 20nsec
V/Div 0.05

TP12

TP11
HTRIG



#1.1

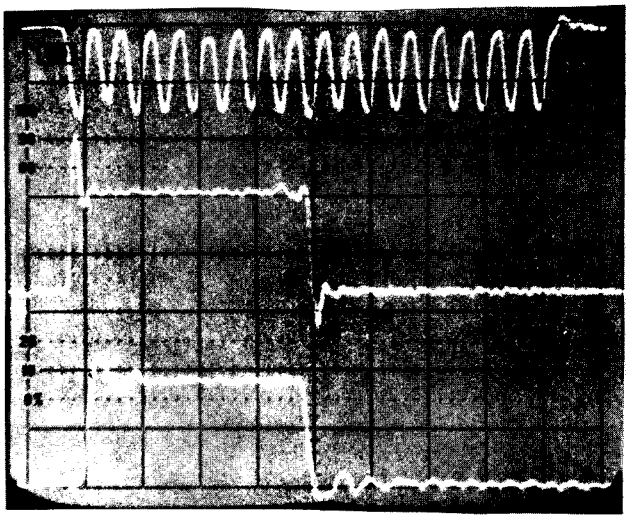
Measure with 10017A Probe the following ECL signals with respect to the 100 MHz clock.
Scope setting
0.2 us/Div x 10
0.05 V/Div

100 MHz Clock
TP7

CHA TP11
HTRIG

TRIG. on CH. A

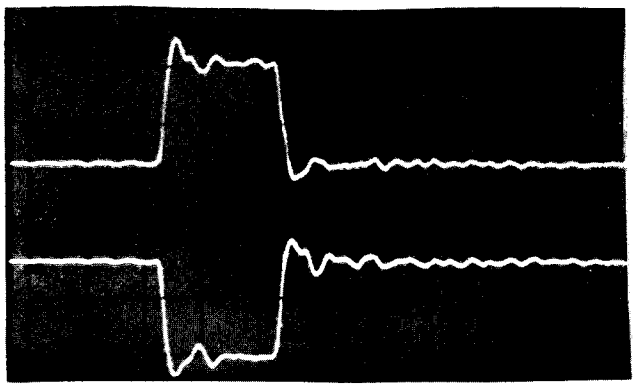
U74/15
HINT



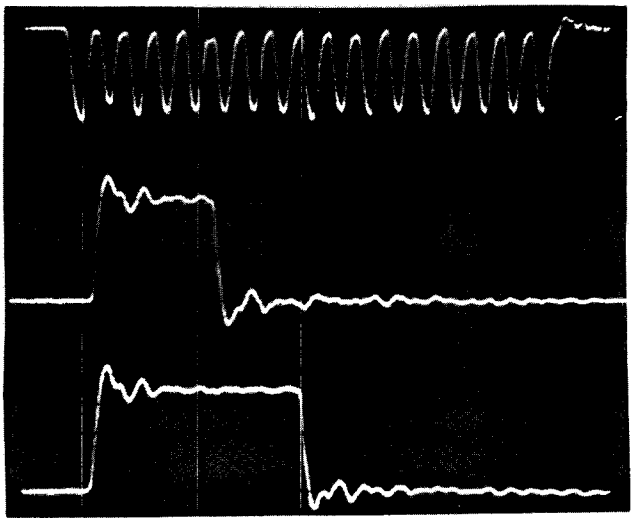
#1.2

U64/14
HINIT

U64/15
LINIT



#1.3

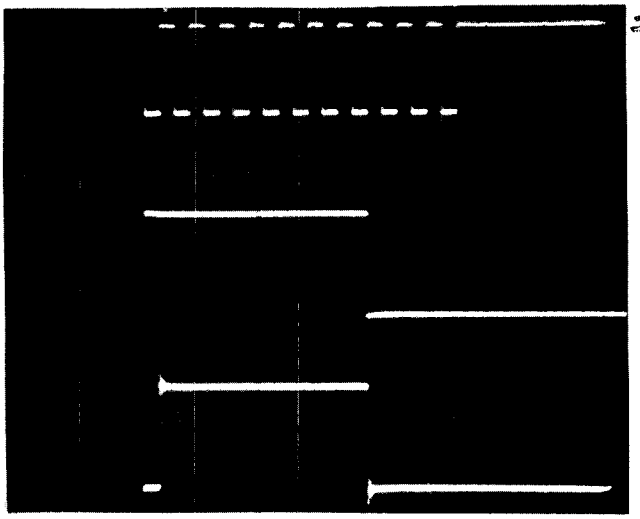


#1.4

SET UP #2

On Control Page [Cloc] menu, change: System Clock to [external from rear panel BNC].

→ Set 8112A PER to 100 us. WIDTH ≈ 11 MSEC
Apply a 1 MHz Square Wave Signal to the EXT. Clock BNC on rear panel
(e.g. 8007B: Period 1us, Width 500ns, Ampl. +2V
Delay min, TT min, Offset OFF, Norm) Scope setting
2us/Div
0.05 V/Div



#2.1

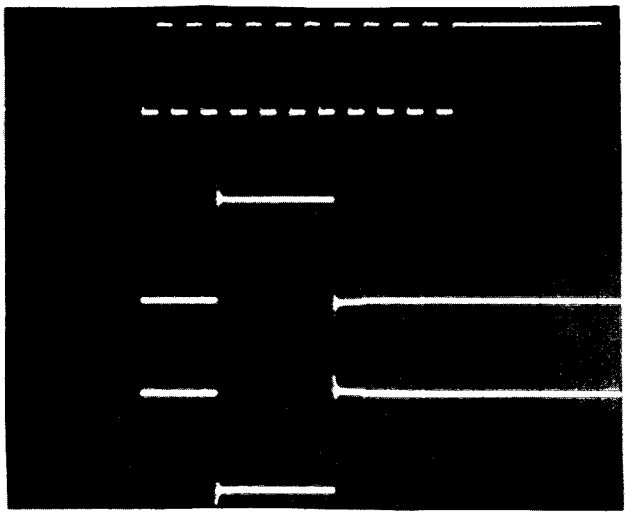
1 MHz External
Clock Signal

U64/14
HINIT

NOTES USE THIS AS THE TRIGGER TO CHECK FOR PROPER TIME RELATIONSHIP

U64/15
LINIT

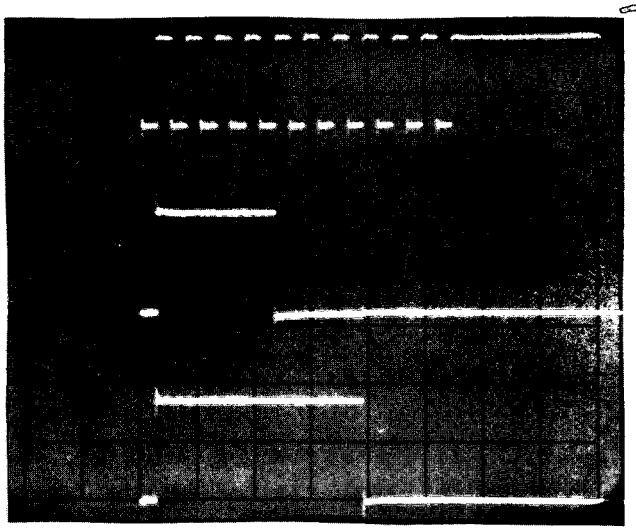
#2.2



U85/3
HUCLKSTOP

U85/14
HDCCLKSTOP

#2.3

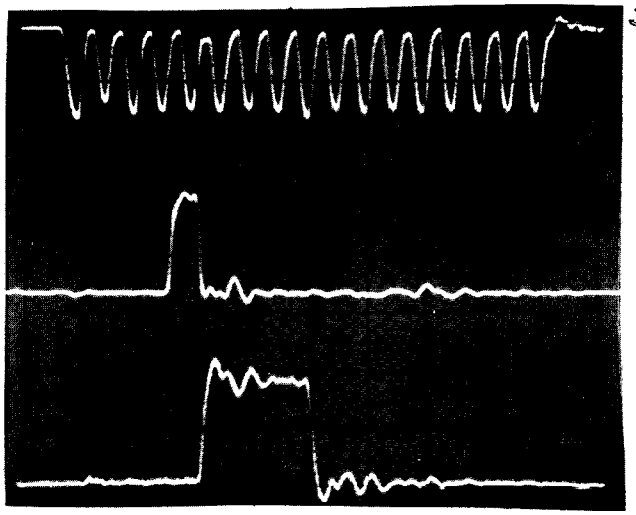


TRIGGER ?

U37/7
HUINIT

U71/15
HLATCHDIS

#1.5



#1.6

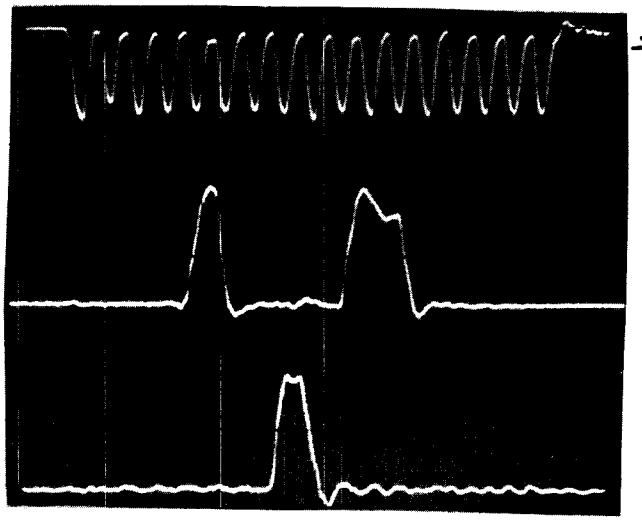
CH A

TRIG. ON A

U79/2
PADD2

20 n sec width

U80/5
HADD



#1.7

TP8
PPRG

U80/11
HJMPR

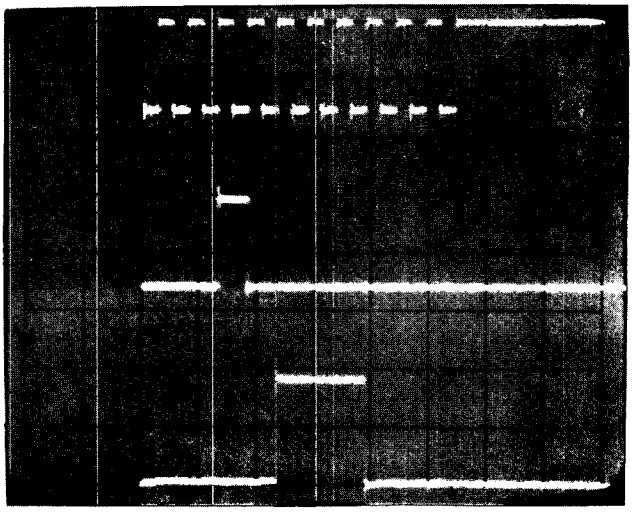
NOTE: With the internal 100 MHz Clock Signal, propagation times of IC's may have to be taken into account!

RESET 8175A
CLOCK TO [INTERNAL]
ON CONTROL PAGE
MODE [AUTO CYCLE]

#2.4

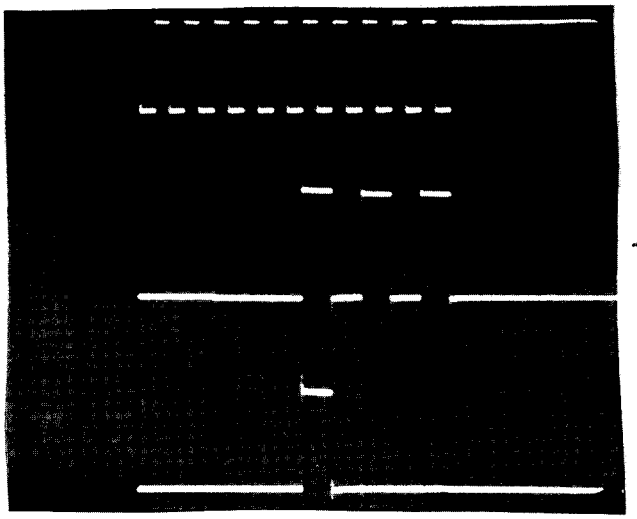
U37/7
HUINIT

U71/15
HLATCHDIS'



U79/2
PADD2

U80/5
HADD

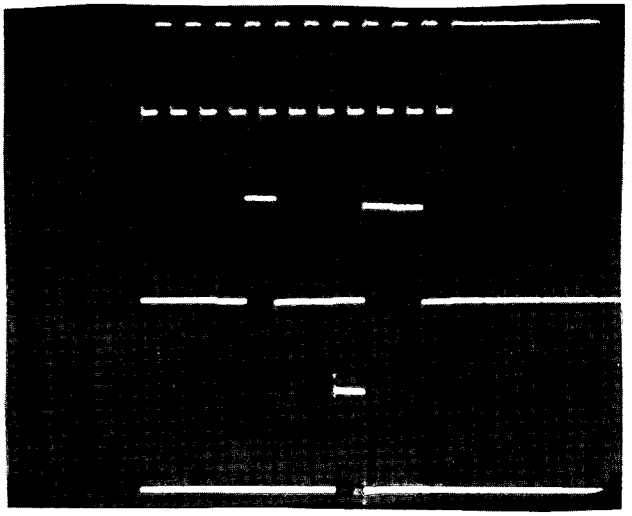


#2.5

OF PULSES ?

TP8
PPRG

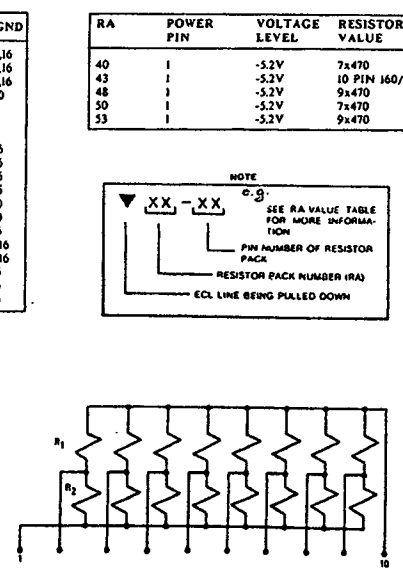
U80/11
HJMPR

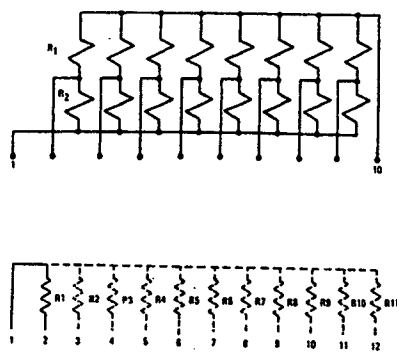


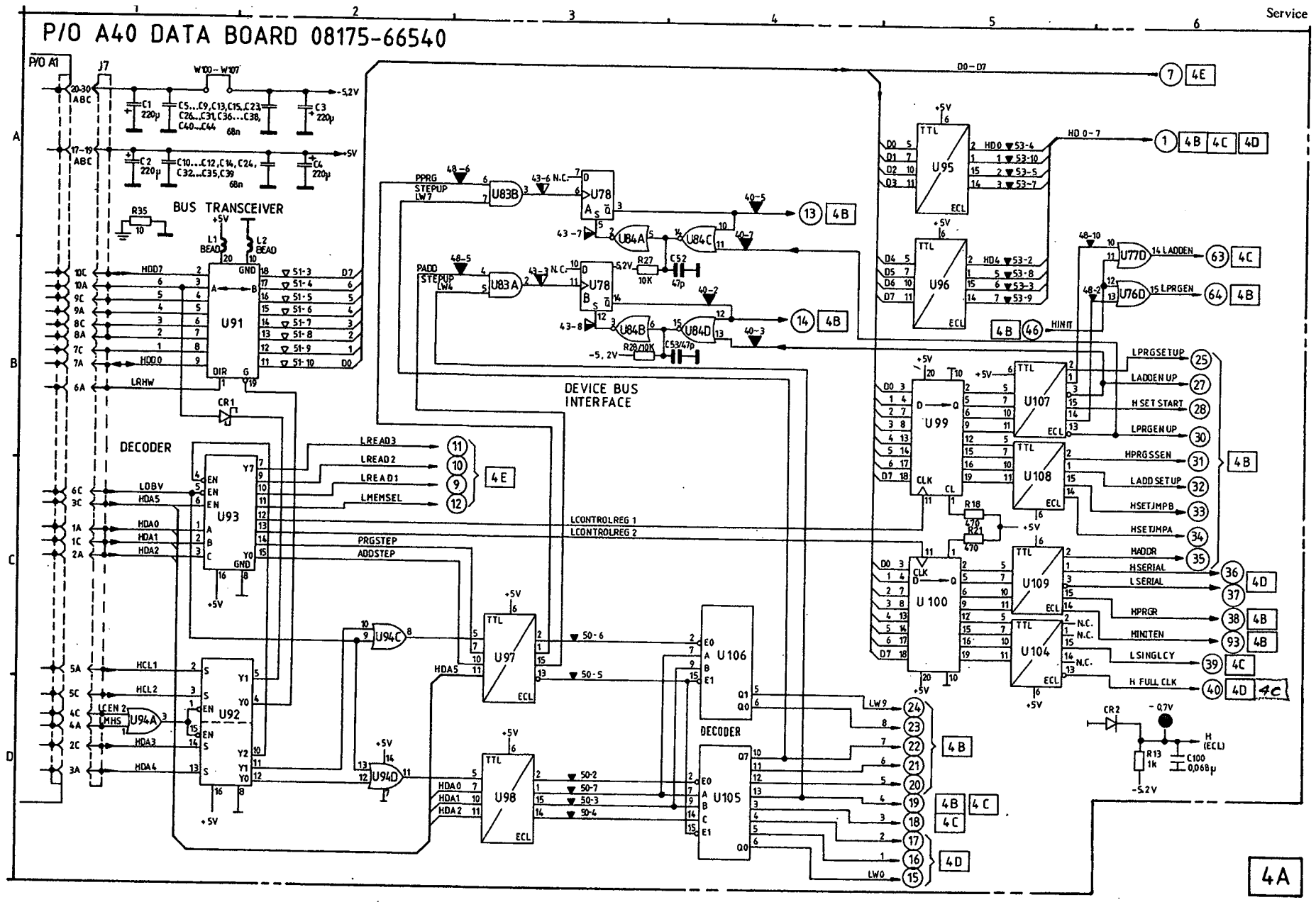
#2.6

REF.DES.	-5.2V	+5V	-15V	+15V	GND
U78	8				1,16
U83	8				1,16
U84	8				1,16
U91		20			10
U92		16			8
U93		16			8
U94		14			7
U95	8	9			16
U96	8	9			16
U97	8	9			16
U98	8	9			16
U99		20			10
U100		20			10
U104		9			16
U105	8				1,16
U106	8				1,16
U107		9			16
U108		9			16
U109		9			16

RA	POWER PIN	VOLTAGE LEVEL	RESISTOR VALUE
40	1	-5.2V	7x470
43	1	-5.2V	10 PIN 160/240
48	1	-5.2V	9x470
50	1	-5.2V	7x470
53	1	-5.2V	9x470



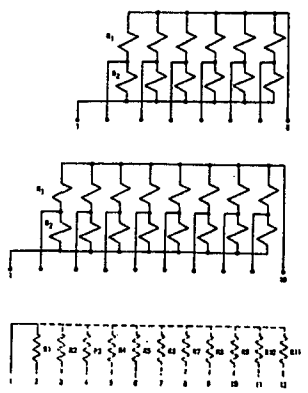


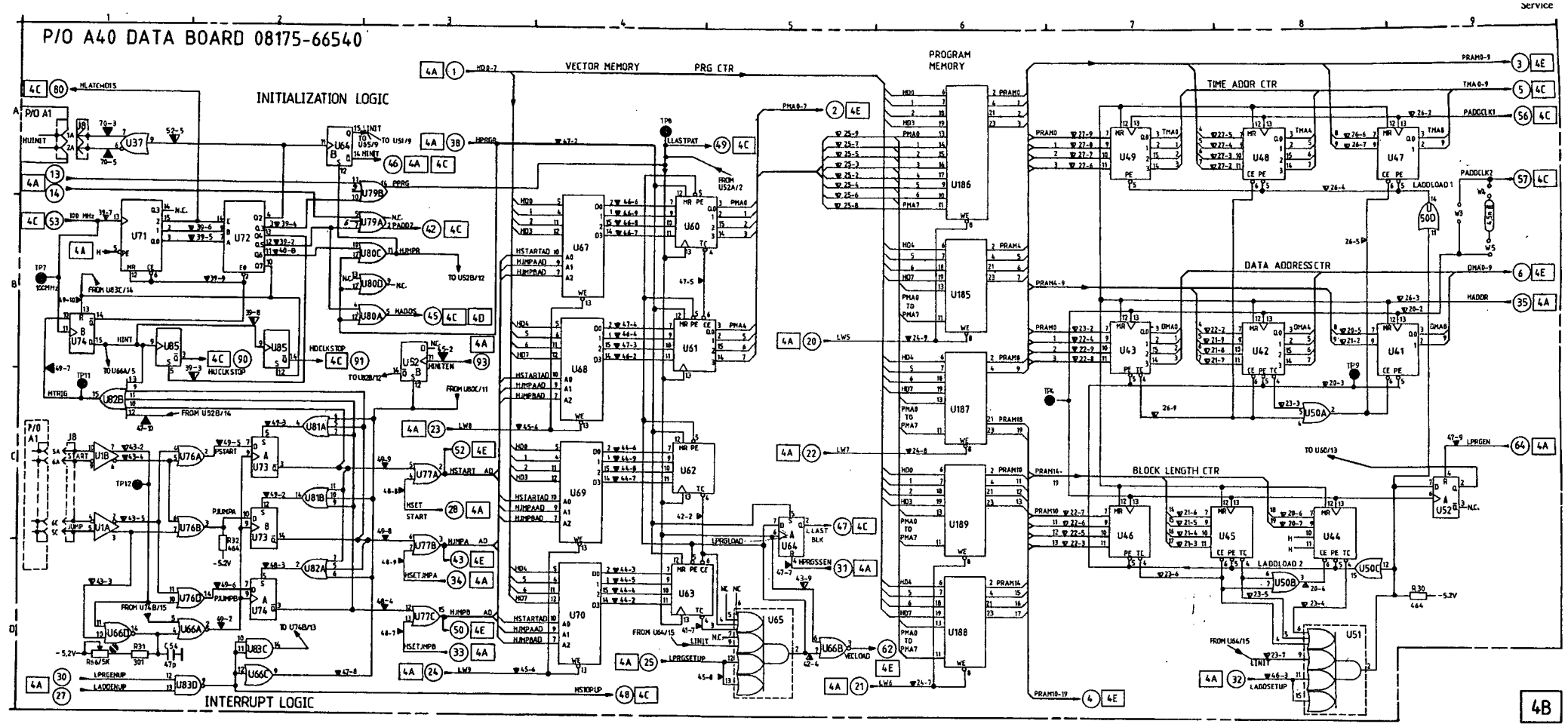


REF.DES.	-5.2V	+5V	-15V	+15V	GND
U1					U4
U37					U5
U41					U10
U42					U10
U43					U10
U44					U10
U45					U10
U46					U10
U47					U10
U48					U10
U49					U10
U50					U5
U51					U5
U52					U5
U60					U5
U61					U5
U62					U5
U63					U5
U64					U5
U65					U5
U66					U5
U67					U5
U68					U5
U69					U5
U70					U5
U71					U5
U72					U5
U73					U5
U74					U5
U76					U5
U77					U5
U79					U5
U80					U5
U81					U5
U82					U5
U83					U5
U85					U5
U185	12				U24
U186	12				U24
U187	12				U24
U188	12				U24
U189	12				U24

RA	POWER PIN	VOLTAGE LEVEL	RESISTOR VALUE
20	1	-5.2V	8 PIN 160/240
21	1	-5.2V	10 PIN 160/240
22	1	-5.2V	10 PIN 160/240
23	1	-5.2V	10 PIN 160/240
24	1	-5.2V	9x10K
25	1	-5.2V	10 PIN 160/240
26	1	-5.2V	10 PIN 160/240
27	1	-5.2V	10 PIN 160/240
39	1	-5.2V	10 PIN 160/240
40	1	-5.2V	7x470
41	1	-5.2V	8 PIN 160/240
42	1	-5.2V	8 PIN 160/240
43	1	-5.2V	10 PIN 160/240
44	1	-5.2V	9x60
45	1	-5.2V	9x470
46	1	-5.2V	9x470
47	1	-5.2V	9x470
48	1	-5.2V	9x470
49	1	-5.2V	9x470
32	1	-5.2V	10 PIN 160/240
70	1	-5.2V	7x330

NOTE
e.g.
XX - XX
SEE RA VALUE TABLE FOR MORE INFORMATION
PIN NUMBER OF RESISTOR PACK
RESISTOR PACK NUMBER (RA)
ECL LINE SEND PULLED DOWN





REF.DES.	-5.2V	+5V	-15V	+15V	GND
U1	8				16
U2	8				16
U3	8				16
U4		16			8
U5		16			8
U6		16			8
U7		16			8
U8		16			8
U9	8				16
U10		9			16
U11	8	9			16
U12		14			7
U14	8				16
U15					16
U16					16
U17					16
U18					16
U19					16
U20					16
U21					16
U22					16
U29					16
U30					16
U33					16
U36					16
U37					16
U39					16
U140					16
U141					16
U142					16
U143					16
U144					16
U145					16
U146					16
U147					16
U148					16
U149					16
U150					16
U151					16
U152					16
U178	8				16

RA	POWER PIN	VOLTAGE LEVEL	RESISTOR VALUE
5	1	-5.2V	9x330
6	1	-5.2V	9x330
11	1	-5.2V	10 PIN 160/240
28	1	-5.2V	8 PIN 160/240
29	1	-5.2V	10 PIN 160/240
30	1	-5.2V	8 PIN 160/240
31	1	-5.2V	10 PIN 160/240
33	1	-5.2V	10 PIN 160/240
34	1	-5.2V	8 PIN 160/240
35	1	-5.2V	8 PIN 160/240
36	1	-5.2V	8 PIN 160/240
37	1	-5.2V	8 PIN 160/240
38	1	-5.2V	8 PIN 160/240
41	1	-5.2V	8 PIN 160/240
46	1	-5.2V	9x470
52	1	-5.2V	10 PIN 160/240
54	1	-5.2V	8 PIN 160/24
70	1	-5.3V	7x330

NOTE

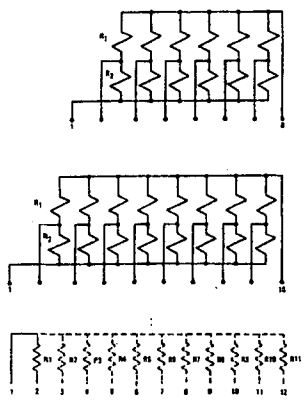
XX1 - XX2 - g

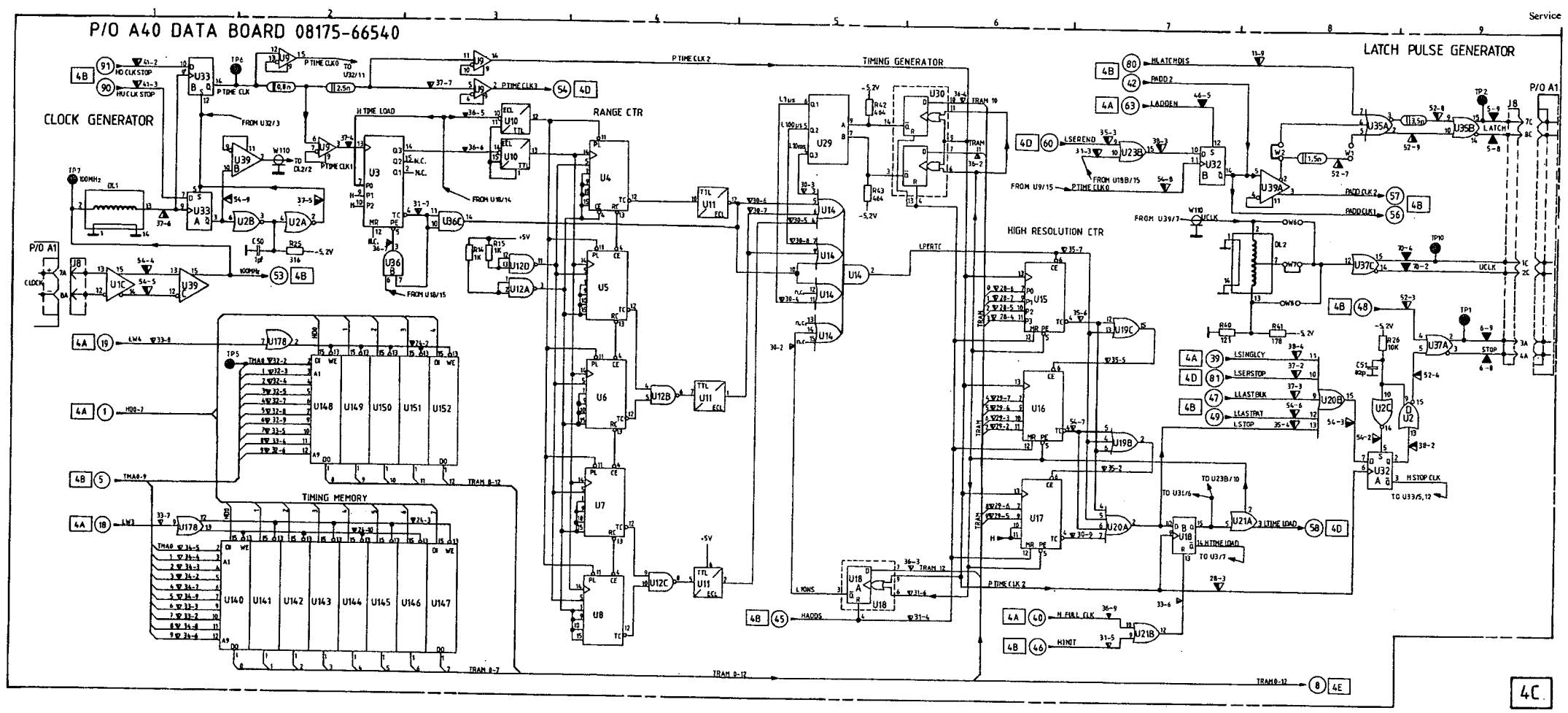
SEE RA VALUE TABLE FOR MORE INFORMATION

PIN NUMBER OF RESISTOR PACK

RESISTOR PACK NUMBER (RU)

ECL LINE BEING PULLED DOWN

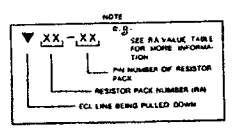


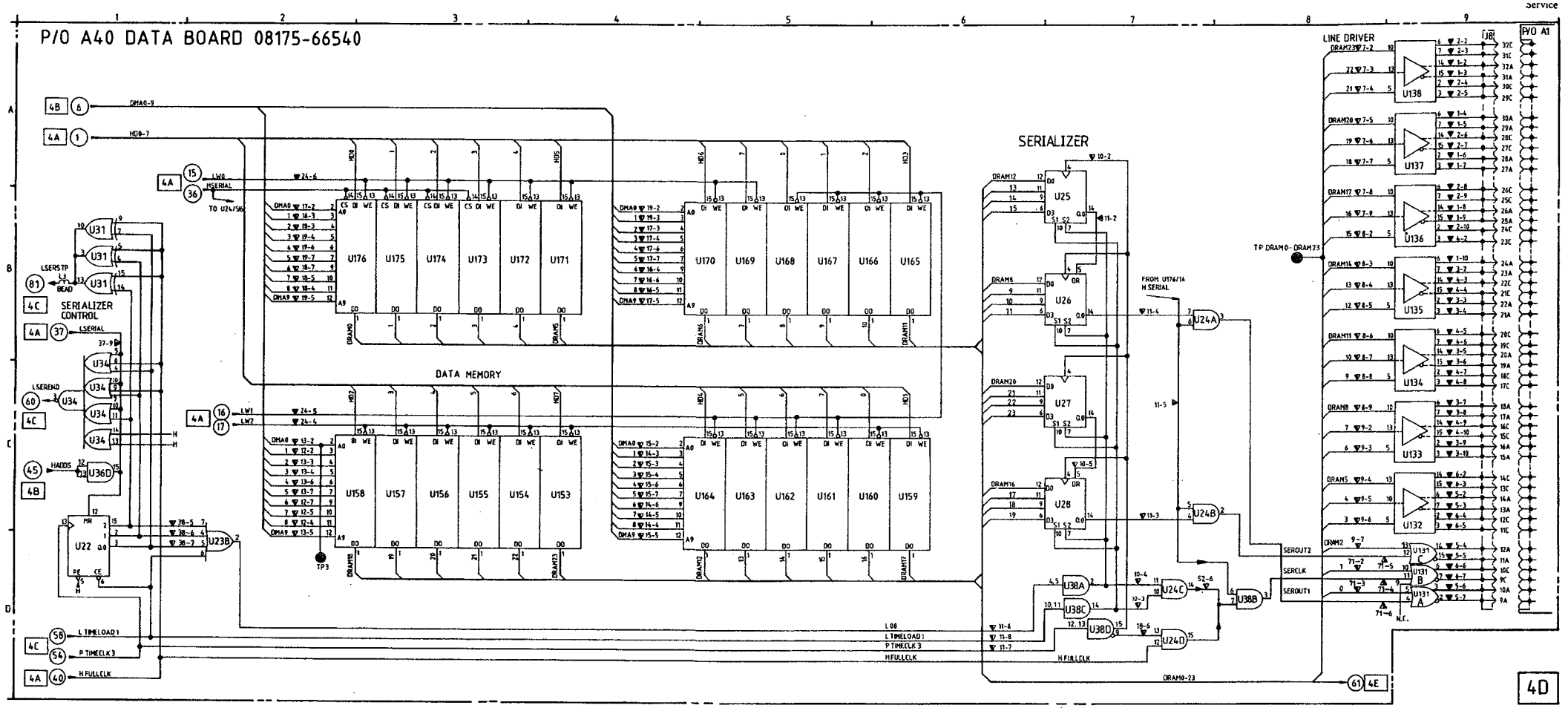


REF.DES.	-5.2V	+5V	-15V	+15V	GND
U22					J,16
U23					J,16
U24					J,16
U25					J,16
U26					J,16
U27					J,16
U28					J,16
U31					J,16
U34					J,16
U36					J,16
U38					J,16
U131					J,16
U132					J,16
U133					J,16
U134					J,16
U135					J,16
U136					J,16
U137					J,16
U138					J,16
U151					J,16
U154					J,16
U155					J,16
U156					J,16
U157					J,16
U158					J,16
U159					J,16
U160					J,16
U161					J,16
U162					J,16
U163					J,16
U164					J,16
U165					J,16
U166					J,16
U167					J,16
U168					J,16
U169					J,16
U170					J,16
U171					J,16
U172					J,16
U173					J,16
U174					J,16
U175					J,16
U176					J,16

RA	POWER PIN	VOLTAGE LEVEL	RESISTOR VALUE
1	1	-5.2V	9x330
2	1	-5.2V	9x330
3	1	-5.2V	9x330
4	1	-5.2V	9x330
5	1	-5.2V	9x330
6	1	-5.2V	9x330
7	1	-5.2V	10 PIN 160/240
8	1	-5.2V	10 PIN 160/240
9	1	-5.2V	10 PIN 160/240
10	1	-5.2V	8 PIN 160/240
11	1	-5.2V	10 PIN 160/240
12	1	-5.2V	8 PIN 220/330
13	1	-5.2V	8 PIN 220/330
14	1	-5.2V	8 PIN 220/330
15	1	-5.2V	8 PIN 220/330
16	1	-5.2V	8 PIN 220/330
17	1	-5.2V	8 PIN 270/330
18	1	-5.2V	8 PIN 220/330
19	1	-5.2V	8 PIN 220/330
24	1	-5.2V	9x1K
37	1	-5.2V	8 PIN 160/240
38	1	-5.2V	8 PIN 160/240
32	1	-5.2V	10 PIN 160/240
31	1	-5.2V	8 PIN 160/240

NOTE





REF.DES.	-5.2V	+5V	-15V	+15V	GND
U111	7	16			8
U112	7	16			8
U113	7	16			8
U114	7	16			8
U115	7	16			8
U116	7	16			8
U117	7	16			8
U118	7	16			8
U119		16			8
U120	12	16			8
U121	12	16			8
U123	12	16			8
U124	12	16			8
U125	7	16			8
U126	7	16			8
U200	7	16			8
U201	12	14			7
U202		14			7
U203		14			7
U204		14			7

RA	POWER PIN	VOLTAGE LEVEL	RESISTOR VALUE
42	1	-5.2V	8 PIN 160/240
55	1	-5.2V	8x1.8K
56	1	-5.2V	8x1.8K
57	1	-5.2V	8x1.8K
58	1	-5.2V	8x1.8K
59	1	-5.2V	8x1.8K
60	1	-5.2V	8x1.8K
61	1	-5.2V	8x1.8K
62	1	-5.2V	8x1.8K

NOTE

*S

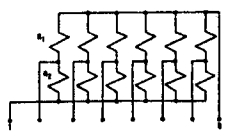
XX1-XX

SEE RA VALUE TABLE FOR MORE INFORMATION

PIN NUMBER OF RESISTOR PACK

RESISTOR PACK NUMBER -RUS

ECL LINE BEING PULLED DOWN



Service

P/O A40 DATA BOARD 08175-66540

DMA

PRAM

TRAM

DRAM

MUX

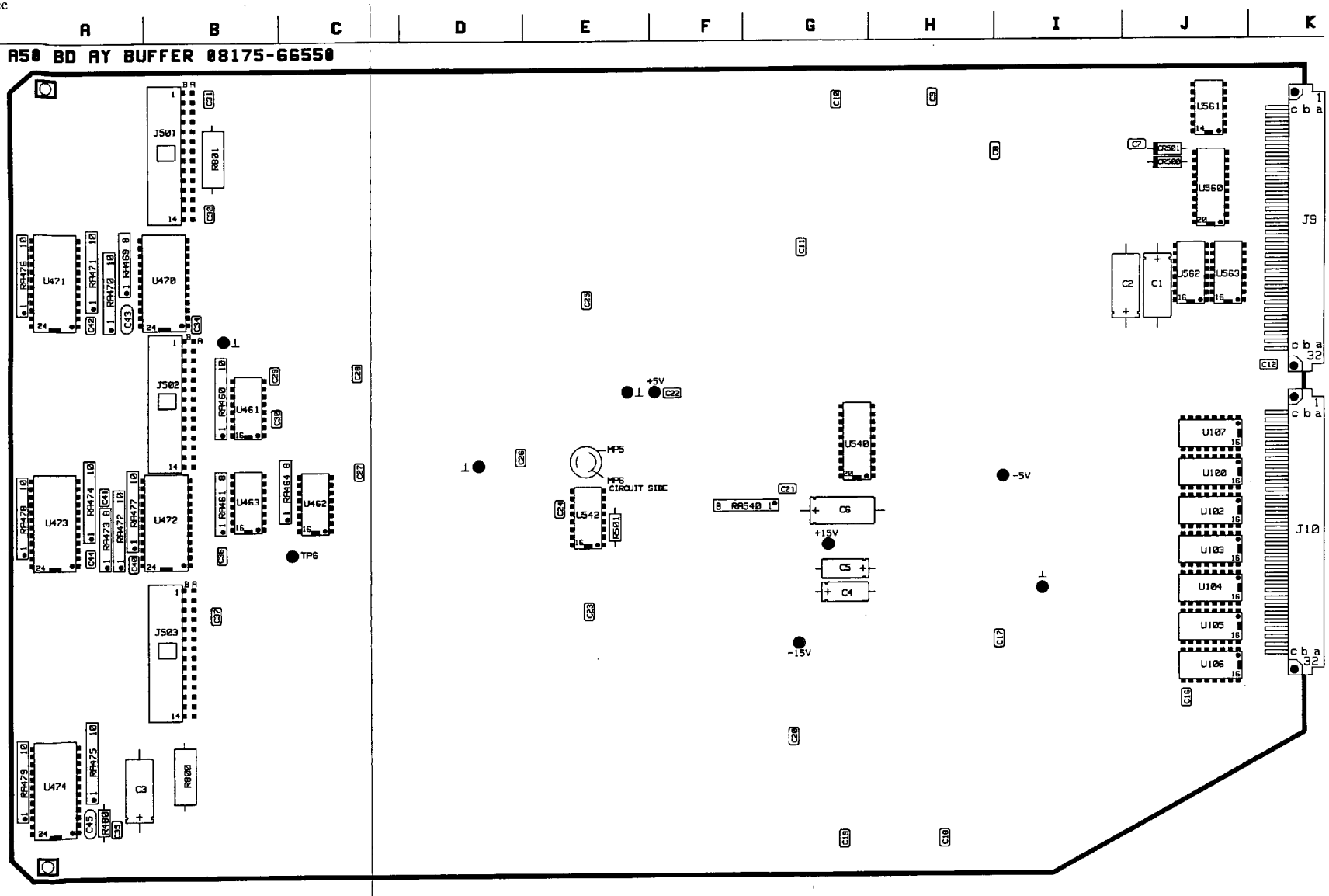
VECTOR LATCH

LREAD3

4E

8-175

A50 BD AY BUFFER 08175-66550



REF DES	GRID LOC	REF DES	GRID LOC
C1	J2/3	R480	A6
C2	I/J2/3	R501	E5
C3	A/B6/7	R800	B6/7
C4	G5	R801	B1
C5	G5		
		RA460	B3/4
C6	G4	RA461	B4
C7	J1	RA464	B/C4
C8	H/J1	RA469	A2
C9	H1	RA470	A2/3
C10	G1		
		RA471	A2/3
C11	F2	RA472	A4/5
C12	K3	RA473	A4/5
C16	J6	RA474	A4
C17	H/I5	RA475	A6
C18	H7		
		RA476	A2/3
C10	G7	RA477	A4
C20	G6	RA478	A4
C21	G4	RA479	A6/7
C22	F3	RA540	F/G4
C23	E5		
		TP6	C4/5
C24	E4		
C25	E2	U100	J4
C26	D4	U102	J4
C27	C4	U103	J4/5
C28	C3	U104	J5
		U105	J5
C29	B3		
C30	B3	U106	J5/6
C31	B1	U107	J3/4
C32	B2	U461	B3
C34	B3	U462	C4
		U463	B4
C35	A7		
C36	B4	U470	B2/3
C37	B5	U471	A2/3
C40	A5	U472	B4/5
C41	A4	U473	A4/5
		U474	A6/7
C42	A3		
C43	A3	U540	G3/4
C44	A4/5	U542	E4/5
C45	A7	U560	J1/2
		U561	J1
CR500	J1	U562	J2/3
CR501	J1	U563	J2/3
J9	K1/2/3		
J10	K3/4/5		
J501	B1/2		
J502	B3/4		
J503	B5/6		
MP5	E4		
MP6	E4		

BUFFER
BOARD

SERVICE BLOCK 5
BUFFER AND FINE TIMING BOARDS

INTRODUCTION

This is a two part service block which covers both of the above boards. A single asembly number of A50 is allocated for both types of board. A Fine Timing Board (A52) is installed (in place of the Buffer Board) only if your 8175A includes option 001. Therefore, your 8175A will have either an A50 or an A52 board installed, but not both. The first part of this service block covers theory and troubleshooting of the Buffer Board. Ignore this and refer to the second part if your 8175A has a Fine Timing Board installed.

NOTE: In the case of the Fine Timing Board, if your 8175A has a serial number lower than that shown at the front of this manual, refer to the Backdating section.

BUFFER BOARD

THEORY OF OPERATION

Introduction

The Buffer Board is used to either synchronize all 24 data-signals for minimum scew in Parallel D.G. configuration or, to serialize the data signals to channels 0 and 2 in Serial configuration.

The board comprises four main sections or blocks. They are shown on the block diagram (Figure 8-5-1) and are as follows:

Input Circuitry
Output Circuitry
Latch-Tristate Circuitry
Device Bus Interface

Note that, a table (8-5-1) which explains the mnemonics used on the schematics is included at the end of the theory section.

INPUT CIRCUITRY (Schematic 50B)

All incoming differential ECL data-signals from connector J10 are converted into single ended signals by the line receivers U100-U106, they are then fed to the output circuitry.

OUTPUT CIRCUITRY (Schematic 50B)

The output circuitry is divided into two main sections which are described as follows:

Output section channel 0-3
Output section channel 4-23

***Output* Section Channels 0-3**

The data-signals for channels 0-3 are fed to the quad-NOR-Gate U461 (the common input U461/12 is at low). The inverted data signals 0-3 are then fed directly to the inputs of the level-triggered ECL-data Latch U470.

When the 8175A is configured as a Serial D.G., (HSERIAL=High) the input data passes directly through the latch, because the latch enable signal (LATCH2) at U470/20 will be set low. (The latch is in transparent mode). In the Serial configuration, channel 0 and channel 2 are used for the serial output patterns and channel 1 is the clock output (see also theory of the Data Board).

When the 8175A is configured as a Parallel D.G., (HSERIAL = low) therefore LATCH2 will follow the incoming latch-signal. The input data will be latched to the outputs of U470 when the latch signal at pin 20 goes high. The differential output signals are then sychronized, and fed to the output pod connector J501.

Output Section Channels 4-23

This section is really of significance only in Parallel configuration. The input data-signals 4-23 are synchronously latched (U471-474) to the output pod connectors J502 and J503 by the latch-signals LATCH3 - LATCH5. The operation is as previously described for channels 0 - 3. (In Serial configuration, parallel data is available from channels 4-23, but with an 8 times slower pattern duration.)

LATCH-TRISTATE CIRCUITRY (Schematic 50A)

The incoming differential ECL latch-signal (HLATCH/LLATCH) is converted into a single ended latch-signal by the line receiver U107B and is fed to the dual-NOR-Gate U462. The resulting latch-signal is then split by U462B into signals LATCH3 - LATCH5 for the output latches U471 - U474.

Also, the latch-signal is fed to U462A from where the signal LATCH2 is produced. The output condition of LATCH2 depends on the control-signal HSERIAL. When HSERIAL (U462A/6) goes high (Seial configuration), LATCH2 is constant low. When HSERIAL goes low (Parallel configuration), LATCH2 is able to follow the incoming latch-signal.

Also in this section, the tristate-signals are conditioned. The incoming differential ECL tristate-signal is buffered by the line receiver U107A, split by the quad-NOR-Gate U463 and then fed to the output pod connectors J501 to J503.

DEVICE BUS INTERFACE (Schematic 50A)

This section's main function is to interface the board with the MPU and to provide the ECL control-signal HSERIAL. It comprises two functional blocks: this circuitry:

- Interface section
- Register section

Interface Section

This section includes the Octal bus transceiver U560, the OR-Gate U561, the diodes CR501, CR502, and the decoders U562 and U563. U563 is activated by the signals LCEN and LMHS as they go low. When HCL1 goes high and HCL2 goes low, the diodes CR501, CR502, are pulled to low so producing the Buffer Board identifying code number (for the CPU) of decimal 50.

When HCL1 and HCL2 go low, U560 is enabled. U560 is in read mode when LRHW goes low, Data D0-D7 will be transmitted to the HDD0-7 data bus.
In the write mode (LRHW=High), all incoming TTL data (HDD0-HDD7) is fed to the latch register U540.

The address decoder U562 is enabled when HDA5 goes high plus LDBV low (low-devicebus valid, see theory of MPU) and when the inputs HDA3 and HDA4 of U563 go low. U562 provides the latch-signal for the latch register U540 when U562 is enabled and signals HDA2 and HDA1 are high and HDA0 low.

Register Section

The input data D0 - D7 from U560 is written into the register U540 when the latch-signal at pin 11 goes low and latched to the outputs when the latch-signal goes high afterwards. The TTL-signals from U540 are converted into the required ECL signals by the TTL-ECL Translator U542.

NOTE: On the Buffer Board, the only signal from U542 which is used is HSERIAL. The other signals are related to Fine Timing functions.

Table 8-5-1 Mnemonics Explanation

The first letter in a mnemonic means:

H : high active
L : low active
P : the raising edge of a signal is the active
N : the falling edge of a signal is the active

Mnemonic	Explanation
D0 - D7	TTL - Databus 0-7 on the board.
HCL1, HCL2	High Control Line 1, 2.
HDA0 - HDA5	Address-lines of the devicebus.
HDD0-7	High Device Data 0-7.
HSERIAL	This signal indicates the Serial-Mode.
LATCH2 - LATCH5	Latch signals for the output-latches U470-U474. In Serial - Mode LATCH2 is low, therefore the output latch U470 is transparent.
LCEN	Low Card Enable.
LDBV	Low Device Bus Valid.
LMHS	Low Master/High Slave.
LRHW	Low Read/High Write

BLOCK DIAGRAM BUFFER BOARD 8175A

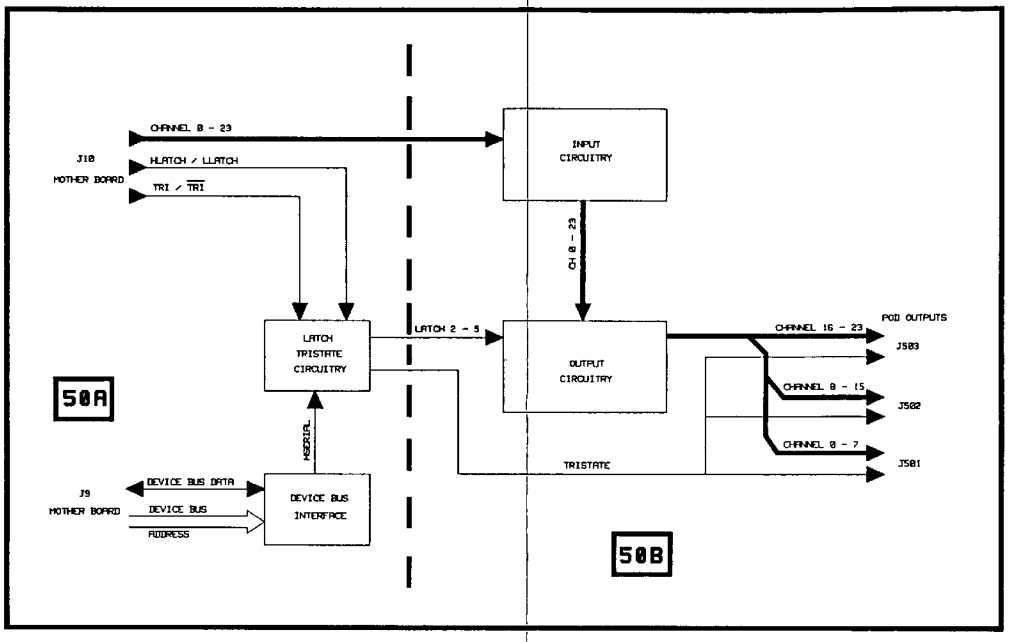


Figure 8-5-1. Buffer Board Block Diagram

TROUBLESHOOTING (BUFFER BOARD)

General

Should a fault be isolated to the Buffer Board (A50), the theory of operation should be read and understood before proceeding with troubleshooting in this area.

CAUTION

Instrument must not be operated without cover over power supply and fan area.

Procedure:

With power OFF, plug the Buffer Board into the 8175A test connectors.
Switch instrument ON, and Recall Standard Settings.

a) First check with a DVM that the Power Supply voltages at the following test points are correct:

TP +5V	+5V	± 50 mV
TP -5.2V	-5.2V	± 50 mV
TP +15V	+15V	± 50 mV
TP -15V	-15V	± 50 mV

b) Check that signal HDELAY = LOW, then for the two modes, check that signals:

Parallel Config.

HSERIAL	= Low
LATCH2	is able to follow the incoming latch signals HLATCH/LLATCH
LATCH3-5	are able to follow signals HLATCH/LLATCH

Serial Config.

HSERIAL	= High
LATCH2	= Low U470 is in transparent mode
LATCH3-5	are able to follow signals HLATCH/LLATCH

c) Set 8175A:

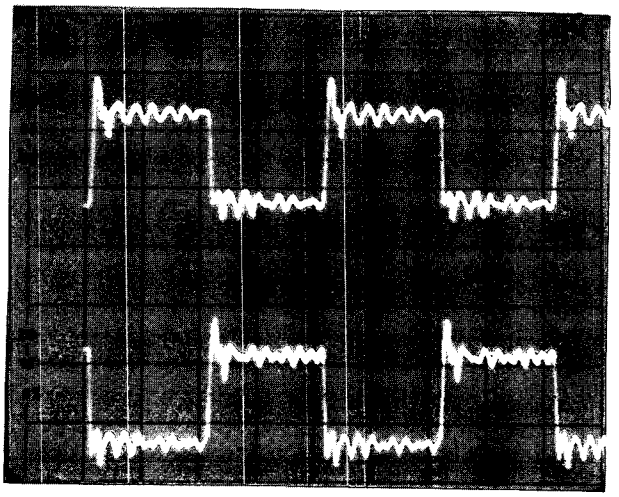
CNTRL > CURSOR↓ > NEXT = [Auto Cycle] >
DATA > CURSOR↓ = Period > 0.1 > DATA > NEXT > CURSOR↓ = Address 0000 > ROLL↑ =
Address 0001 > CURSOR→ = POD2 CH7 > 1 24x >
PRGM > CURSOR↓ = PROG1 > CURSOR→ = 1023 > 0001 >
OUTPUT > NEXT = enabled >
blue > EXEC = UPDATE > START

With scopes settings: 0.05 us/Div and 0.05 V/Div

measure the signals at the following conponents (refer to the photos).

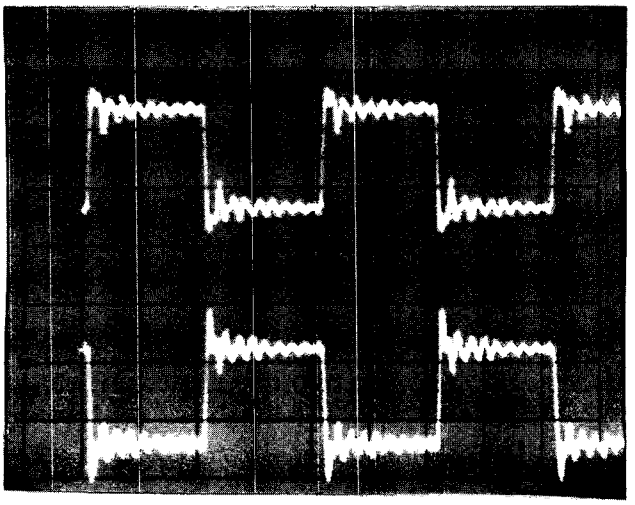
U100/5

U100/4



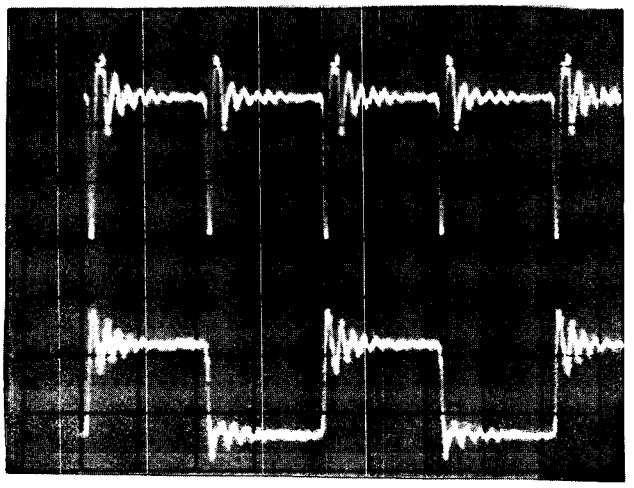
U461/10

U461/14



LATCH2 (U470/20)

U470/12
NOTE: for this test ensure that all PODs disconnected.



REF.DES.	-5.2V	+5V	-15V	+15V	GND
U407	8				14
U462	8				14
U463	8				14
U540		20			10
U542	8	9			10
U560		20			10
U561		14			7
U562		16			8
U563		16			8

RA	POWER PIN	VOLTAGE LEVEL	RESISTOR VALUE
460	1	-5.2V	8 PIN 160/240
461	1	-5.2V	7x470
464	1	-5.2V	8 PIN 160/240

NOTE

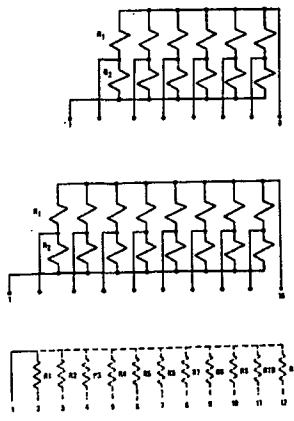
e.g. XX - XX

SEE RA VALUE TABLE FOR MORE INFORMATION

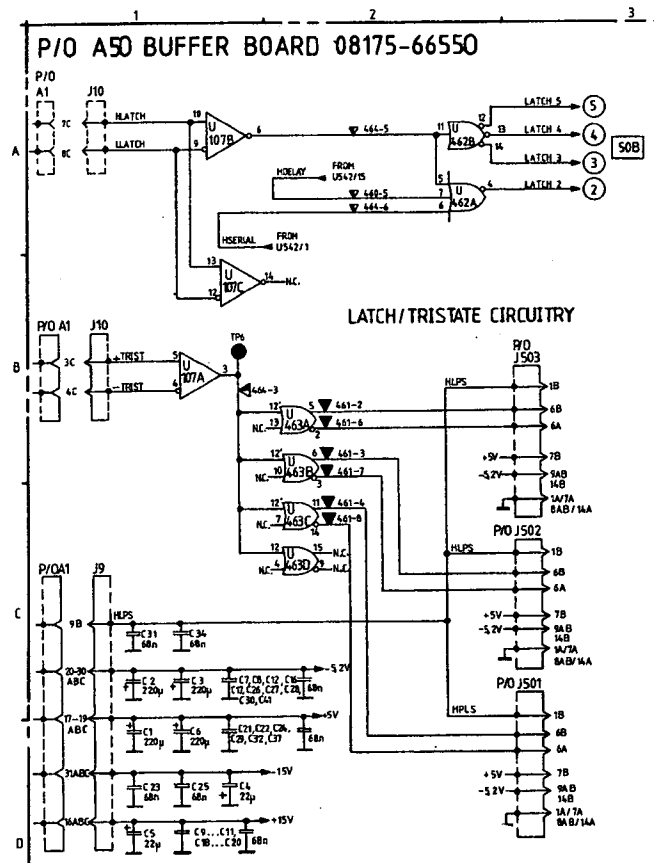
PIN NUMBER OF RESISTOR PACK

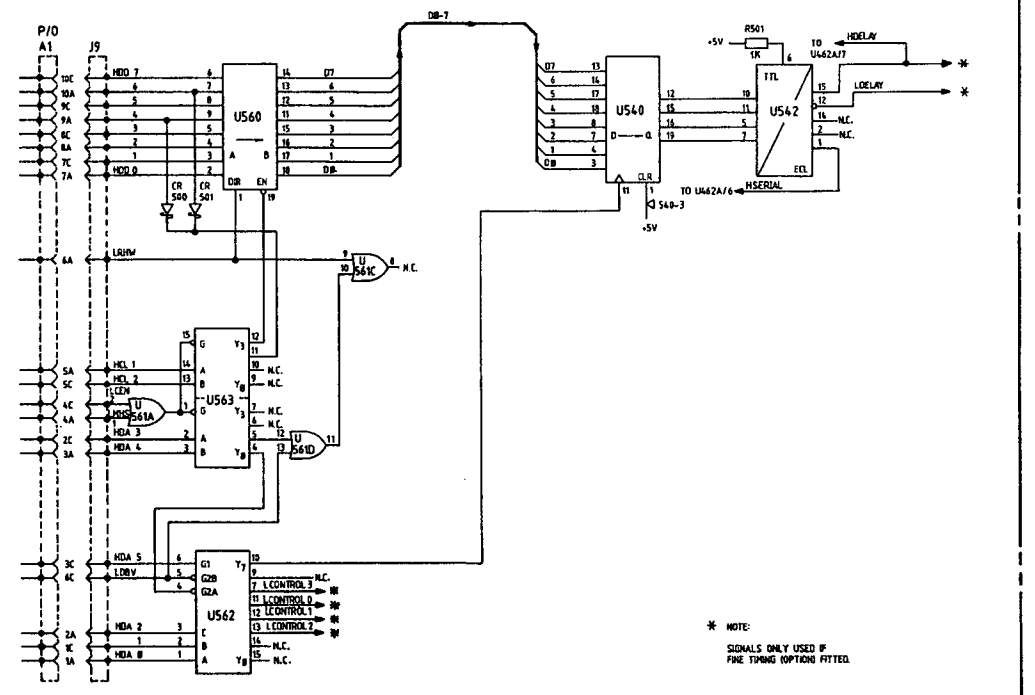
RESISTOR PACK NUMBER (RA)

ECL LINE BEING PULLED DOWN



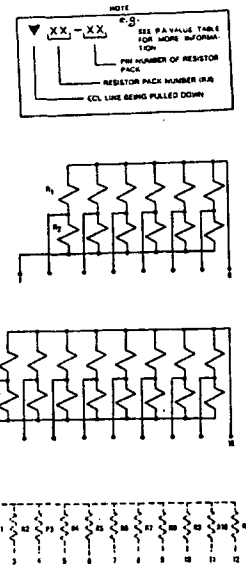
P/O A50 BUFFER BOARD 08175-66550

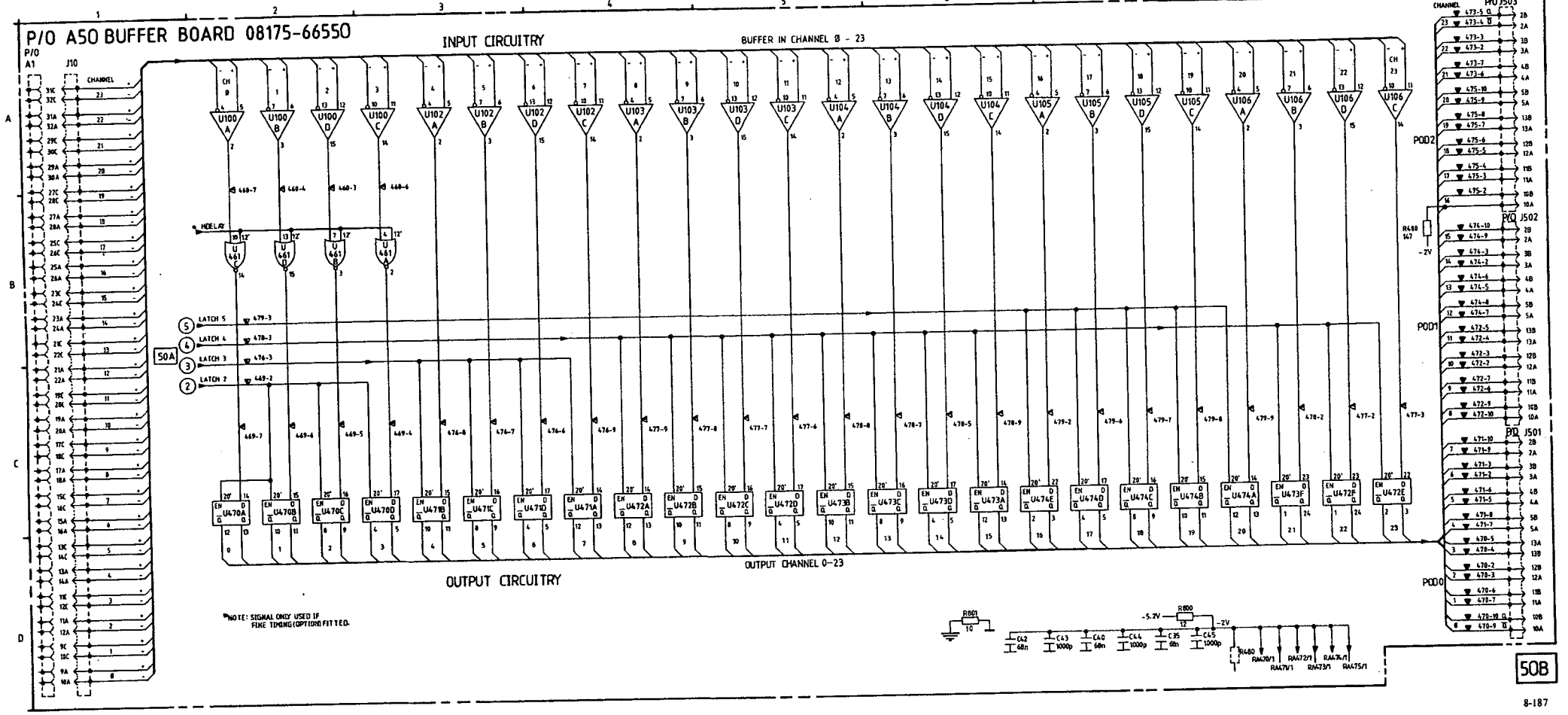


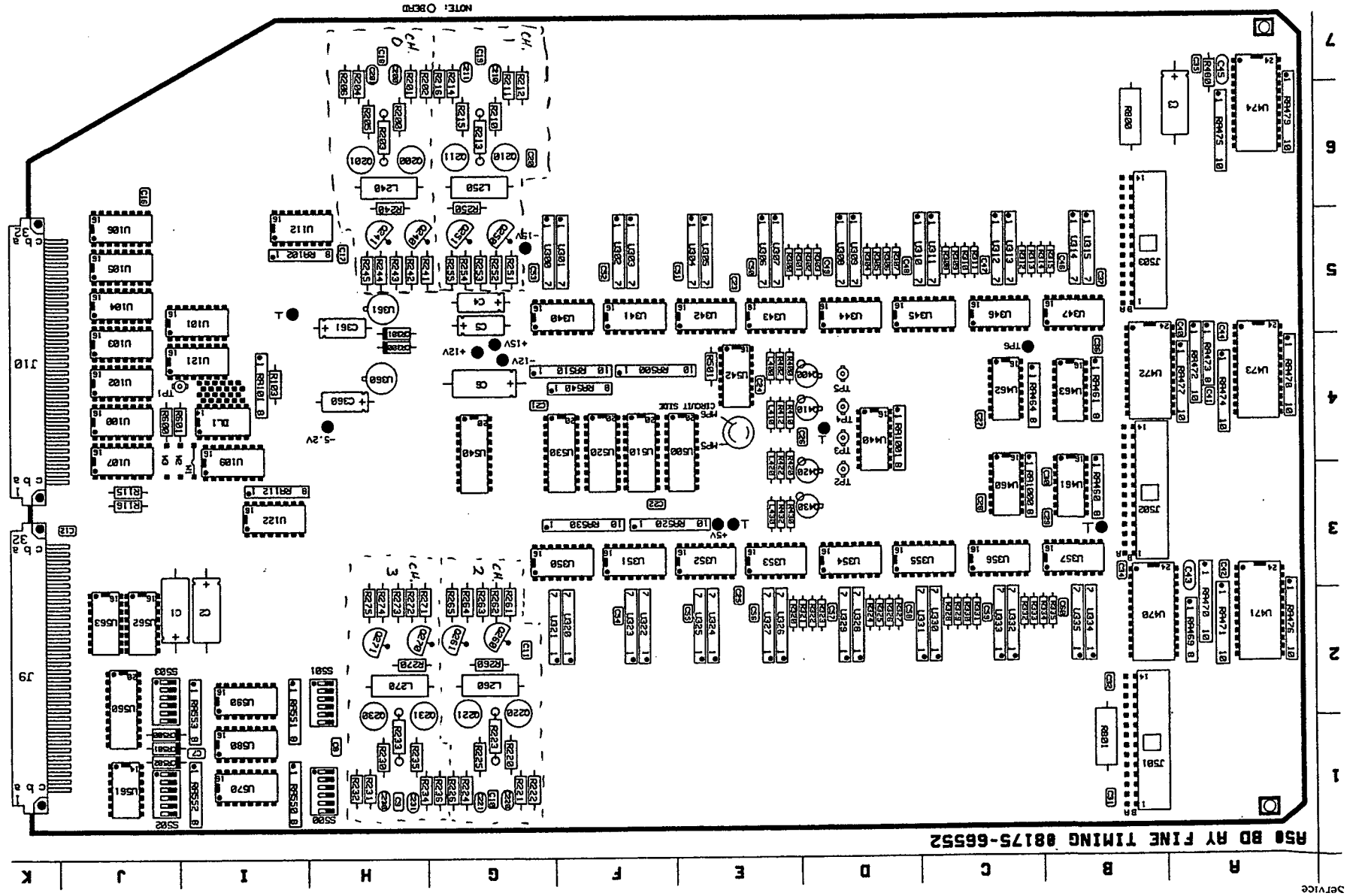


REF.DES.	-5.2V	+5V	-15V	+15V	GND
U100	8				1,16
U102	8				1,16
U103	8				1,16
U104	8				1,16
U105	8				1,16
U106	8				1,16
U468	8				6,7
U470	18				6,7
U471	18				6,7
U472	18				6,7
U473	18				6,7
U474	18				6,7

RA	POWER PIN	VOLTAGE LEVEL	RESISTOR VALUE
460	1	-5.2V	8 PIN 160/240
469	1	-5.2V	8 PIN 160/240
470	1	-5.2V	9x150
471	1	-5.2V	9x150
472	1	-5.2V	9x150
473	1	-5.2V	7x150
474	1	-5.2V	9x150
475	1	-5.2V	9x150
476	1	-5.2V	10 PIN 160/240
477	1	-5.2V	10 PIN 160/240
478	1	-5.2V	10 PIN 160/240
479	1	-5.2V	10 PIN 160/240







REF	GRID	REF	GRID	REF	GRID	REF	GRID	REF	GRID	REF	GRID	REF	GRID
DES	LOC	DES	LOC	DES	LOC	DES	LOC	DES	LOC	DES	LOC	DES	LOC
C1	J2/3	C200	H7	R103	I4	R275	H2	RA471	A2/3	U313	C5/6	U560	J1/2
C3	A6/7	C201	H7	R116	J3	R301	D5	RA472	A4/5	U314	B5/6	U561	J1
C4	G5	C210	G7	R115	J3	R300	E5	RA473	A4/5	U315	B5/6	U562	J2/3
C5	G5	C211	G7	R201	H7	R302	D5	RA474	A4	U320	F2	U563	J2/3
C6	G4	C220	G7	R202	G7	R303	D5	RA475	A6	U321	G2	U570	I1
C7	J1	C221	G1	R203	H6/7	R304	D5	RA476	A2/3	U322	F2	U580	I1
C9	H1	C230	H1	R204	H7	R305	D5	RA477	A4	U323	F2	U590	I2
C10	G1	C231	H1	R205	H7	R306	D5	RA478	A4	U324	E2	W1	J3/4
C12	K3	C360	H4	R206	H7	R307	D5	RA479	A6/7	U325	E2	W2	J3/4
C19	G7	C361	H5	R209	G7	R308	C5	RA500	F/E4	U326	E2	W3	J3/4
C40	A5	CR502	J1	R210	G7	R309	C5	RA510	F/G4	U327	E2		
C41	A4	CR501	J1	R211	G7	R310	C5	RA520	E/F3	U328	D2		
C45	A7	CR500	J1	R212	G7	R311	C5	RA530	F/G3	U329	D2		
C46	B5	Q220	G1	R214	G7	R313	C5	RA540	F4	U330	C2		
C47	C5	Q230	H1	R215	G7	R314	B5	RA551	12	U331	D2		
C48	D5	Q231	H1	R216	G7	R315	B5	RA552	11	U332	C2		
C49	D5	Q240	H6	R220	G1	R320	E5	RA553	12	U333	C2		
C50	E5	Q241	H6	R222	G1	R321	D5	RA1000	C3/4	U334	B2		
C51	E5	Q250	G6	R223	G1/2	R322	D5	RA1001	D3/4	U335	B2		
C52	F5	Q251	G6	R224	G1	R323	D5	RA1002	E3/4	U340	F/G5		
C53	G5	Q260	G2	R225	G1	R324	D5	S500	H1	U341	F5		
C54	F2	Q261	G2	R226	G1	R325	D5	S501	H2	U342	E5		
C55	E2	Q270	H2	R227	G1	R326	D5	S502	J1	U343	D/E5		
C56	E2	Q271	H2	R228	G1	R327	D5	S503	J2	U344	D5		
C64	B3	L430	E3	R229	G1	R328	C5	TP1	I4	U345	C/D5		
C82	B2	L410	E4	R230	H1	R329	C5	TP2	D3	U346	C5		
C91	B1	L400	E4/5	R231	H1	R330	C5	TP5	D4	U347	B5		
C92	B3	L270	H2	R232	H1	R331	C5	TP6	C4/5	U350	F/G3		
C93	B3	L260	G2	R234	H1/2	R332	C5	U100	J4	U352	E3		
C94	B3	L250	G6	R235	H1	R333	C5	U101	I/J5	U353	D/E3		
C95	A7	L430	E3	R236	G1	R334	B5	U102	J4	U354	D3		
C96	B5	MP5	E4	R241	G5	R335	B5	U103	J4/5	U355	C/D3		
C97	B5	MP6	E4	R242	H5	R400	E4/5	U104	J5	U356	C3		
C98	D2	Q400	D4	R243	H5	R402	E4/5	U105	J5	U357	C3		
C99	D2	Q410	D4	R244	H5	R410	E4	U106	J5/6	U360	H4		
C100	D2	Q430	D3	R245	H5	R412	E4	U107	J3/4	U361	H5		
C101	D2	Q420	D3/4	R250	G6	R420	E3/4	U109	I3/4	U440	D4		
C102	D2	Q431	D3	R251	G5	R422	E3/4	U112	H/I6	U460	C3/4		
C103	D2	Q432	D3	R252	G5	R430	E3	U121	I5	U461	B3/4		
C104	D2	Q433	D3	R253	G5	R432	E3	U122	I3	U462	C4		
C105	D2	Q434	D3	R254	G5	R480	A7	U300	G5/6	U463	B4		
C106	D2	Q435	D3	R255	G5	R501	E4	U301	F5/6	U470	B2/3		
C107	D2	Q436	D3	R260	G2	R600	J4	U302	F5/6	U471	A2/3		
C108	D2	Q437	D3	R261	G2	R601	I4	U303	F5/6	U472	B4/5		
C109	D2	Q438	D3	R262	G2	R800	B6/7			U473	B4/5		
C110	D2	Q439	D3	R263	G2	R801	B1	U304	E5/6	U474	A6/7		
C111	D2	Q440	D3	R264	G2	RA101	I4	U305	E5/6	U500	E/F3/4		
C112	D2	Q441	D3	R265	G2	RA102	H/I5	U306	E5/6	U510	G3/4		
C113	D2	Q442	D3	R270	H2	RA460	B3/4	U307	E5/6	U520	F3/4		
C114	D2	Q443	D3	R271	G2	RA461	B4/5	U308	D5/6	U530	F/G3/4		
C115	D2	Q444	D3	R272	H2	RA464	B/C4	U309	D5/6	U540	G3/4		
C116	D2	Q445	D3	R273	H2	RA469	A2	U310	D5/6	U542	E4/5		
C117	D2	Q446	D3	R274	H2	RA470	A2/3	U311	C5/6				
C118	D2	Q447	D3					U312	C5/6				

FINE T.
BOARD

FINE TIMING BOARD

THEORY OF OPERATION

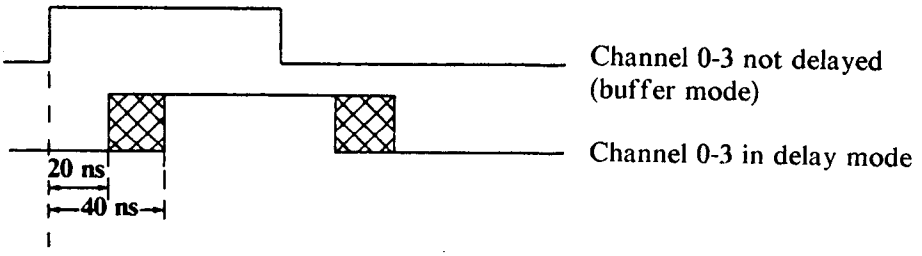
Introduction

The Fine Timing Board is based on the Buffer Board. It performs the same functions and also provides an additional "fine timing" (delay) capability. Its two functional modes are therefore:

- Buffer Mode
- Delay Mode

Buffer Mode
In buffer mode, the board is used either (in Parallel D.G. configuration) to sychronize all 24 data signals for minimum scew or, (in Serial D.G. configuration) to serialize the data for outputting from channels 0 and 2 of POD 0.

Delay Mode
In delay mode, the board performs the above stated "Buffer" functions and also:
enables 4 channels (2 if Serial D.G.) to be delayed (compared to the same channels when non-fine timed) by between 20 and 40 ns (Parallel D.G.) or 0 to 20 ns (Serial D.G.). See the figure below.



Functional Description

The Fine Timing Board comprises the five main sections or blocks listed below. The distribution of these over the schematics is shown in the block diagram Figure 8-5-1.

Input Circuitry
Delay Circuitry
Output Circuitry
Latch/Tristate Circuitry
Device Bus Interface

INPUT CIRCUITRY (Schematic 52B, 52C)

All incoming differential ECL data-signals from connector J10 are converted into single ended signals by the line receivers U100-U106 and are then fed to the output circuitry.

In addition to this, the ECL data-signals 0-3 are connected to the low-level-triggered Latch U101A-D (schematic 52C). It synchronizes the data-signals 0-3 via the signal LATCH1 for Parallel configuration (see Figure 8-5-2). In Serial configuration, the latches are transparent (HSERIAL=High and LATCH1=constant Low).

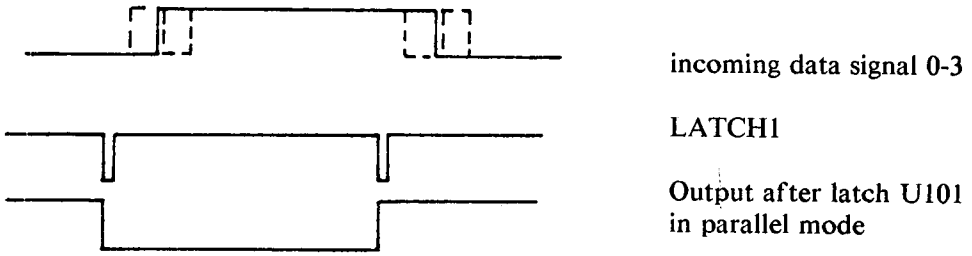


Figure 8-5-2

The low-level-triggered data Latch U121 gives a fixed delay to the data-signals 0-3 in delay mode via the signal LATCH1A (see Latch Tristate Circuitry explanation). In relation to the data-signals 0-3 in buffer mode, the delay is 20 ns (see Figure 8-5-3).

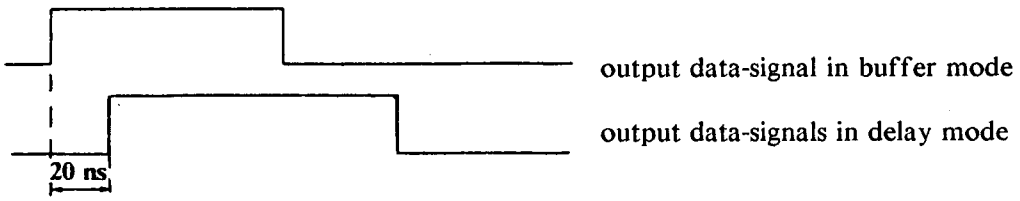


Figure 8-5-3

From the Latches U121, the data-signals 0-3 go to U112, U122. In delay mode (LDELAY=Low) the signals are fed to the following difference-amplifiers:
(Q200-231, R200-236, C200-231). The difference amplifiers convert the data-signals to special levels (not ECL) to compensate the attenuation across the delay circuitry. The data-signals 0-3 are levelshifted by the temperature compensated current sources (Q240 - 271, R240 - 275, L240 - 270). These are used to compensate the base current of the last four delay line switches in the delay circuit (schematic 52D).

DELAY CIRCUITRY (Schematic 52D)

In delay mode, the data signals CH 0-3 can be delayed from 20 ns up to 40 ns by printed delay lines in 100 ps steps. They are switched in by the delay line switches U300-U335. (5.5 ns are used to compensate the scew between the data-signals 0-3.) The delay line switches (U300-315 and U320-335) route the data-signals through the corresponding delay lines. The switches are enabled by -12 V on pin 6 and pin 7 at open (see Figure 8-5-4).

The following is an operational description of one delay line switch (U300). Refer to Figure 8-5-4.
Q1 and Q4 are switched on and Q2 and 3 are switched off. Q2 and Q3 would be switched on for zero delay by holding pin 6 open and pin 7 at -12 V. They also serve to compensate the delay across Q1 and Q4 in delay configuration. The diodes CR1-CR4 are used to decouple the capacitance of the analog switch from the base of the delay line switch-transistors.

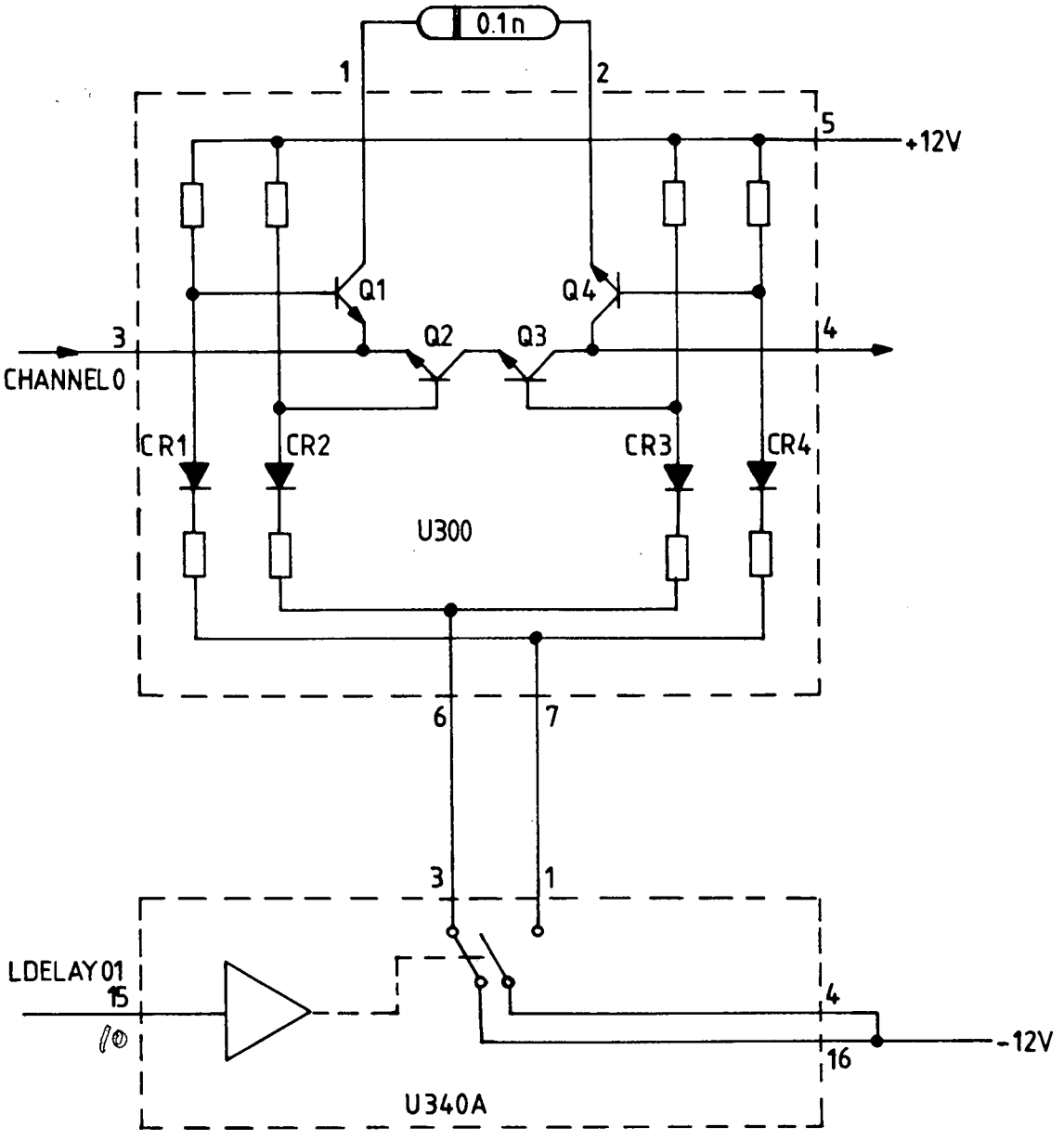


Figure 8-5-4. Delay Line Switch

The analog switches U340-357 (Figure 8-5-4) under the control of the incoming signals LDEL01-LDEL38, control the voltages at pins 6 and 7 of the delay line switches. The voltage regulators U360 and U361 provide special voltages (-12 V, +12 V) for the delay line switches. The resistor dividers R300/301 - 334/335 compensate the base current of the last four delay line switches.
From the delay circuitry, the data signals 0-3 are fed, via the peaker/Buffer section schematic 52C, to the output circuitry.

OUTPUT CIRCUITRY (Schematics 52C, 52B, 52E)

This comprises two sections or blocks:

- Output section channel 0-3
- Output section channel 4-23

Output Section Channel 0-3

The data signals Channel 0-3 are fed from the delay circuitry (schematic 52D) to the peaking circuits L400-430, R400-432 (schematic 52C), to improve the signal characteristics. They are then fed to the buffers Q400-430 and U440.

In delay mode, the data signals CH0-3 are then connected via U460 to the low level triggered output Latch U470 (schematic 52B) because the common input of U460 (LDELAY) will be low. The undelayed data signals CH0-3 (U100/2,3,14,15) will be prevented from passing through the quad-NOR-Gate U461, because its control signal (HDELAY) will be high. The data signals are then converted into differential signals by the Latch U470 (latched when signal LATCH2=Low) and fed to the output pod connector J501.

Note that if delay mode is not used (buffer mode), the delayed data signals CH0-3 cannot pass through U460 (LDELAY=High). In this case, the undelayed data signals will be fed to the output latch U470 via U461 (HDELAY set low).

In Serial D.G. configuration, (HSERIAL=High) the input data passes directly through the output latch because the latch enable signal (LATCH2) U470/20 is set low (latch is in transparent mode). In this mode channel 0 and channel 2 are used for the serial output patterns and channel 1 is the serial clock output (see also theory of the Data Board).

In Parallel D.G. configuration (HSERIAL = LOW therefore LATCH2 is able to follow the incomming latch-signals), the input data is latched to the output of U470 when the latch signal at pin 20 goes high. The differential output signals are now synchronized, and they are fed to the output pod connector J501.

OUTPUT SECTION CHANNELS 4-23 (Schematic 52B)

This section is really of significance only in Parallel D.G. configuration. The input data signals 4-23 are synchronously latched (U471-474) to the output pod connectors J502 and J503 by the latch signals LATCH3 - LATCH5. The operation is the same as described for channels when non-delayed. In Serial configuration, parallel output data is available from channels 4-23 but with an 8 times slower pattern duration.

LATCH TRISTATE CIRCUITRY (Schematic 52A)

The incoming differential ECL latch signals (HLATCH/LLATCH), are converted into a single ended signal by the line receiver U107C. This is then fed to the NOR-Gate U109A, which provides the signal LATCH1, and to the delay lines 0.5 ns and 2.5 ns. Depending on the jumper connected, the signal is then fed to U109B/11-13. This gate provides the signal LATCH1A, which is delayed afterwards by DL1 with special jumpers. (Information about selection of these delay lines is described in the Adjustment Procedure for the Fine Timing Board.

The signals LATCH1 and LATCH1A are at a constant low level for Serial D.G. configuration because the signal HSERIAL is high. In Parallel D.G. configuration, they are able to follow the incoming latch signals since HSERIAL will be low. The incoming differential ECL latch signals (HLATCH/LLATCH) are converted into a single-ended latch-signal by the line receiver U107B, it is then fed to the dual-NOR-Gate U462. U462B splits it into signals LATCH3 - LATCH5 (which are able to follow the incomming latch signals) for the output latches U471 - U474. U462A conditions the latch-signal the different functions of LATCH2 via the control-signals HSERIAL and HDELAY (U462A).

When HSERIAL (U462A/6) is high (n Serial D.G. config.) or HDELAY (U462A/7) goes high in delay mode, LATCH2 is constant low. In buffer mode, HSERIAL is low (parallel mode), signal LATCH2 is able to follow the incoming latch signals.

The tristate signals are also conditioned in this section. The incoming differential ECL tristate signal is buffered by the line receiver U107A, split by the quad-NOR-Gate U463 and then fed to the output pod connectors J501 to J503.

DEVICE BUS INTERFACE (Schematic 52A/52D)

This section's main function is to interface the board with the MPU and to provide all control signals for the board. The section comprises three main blocks:

Interface section
Register section
Scew adjust section

INTERFACE SECTION (Schematic 52A)

This section includes the Octal bus transceiver U560, the OR-Gate U561, the diodes CR500, CR501 and CR502, and the decoders U562 and U563. U563 is activated by the signals LCEN and LMHS as they go low. When HCL1 goes high and HCL2 goes low, the diodes CR500, CR501 and CR502, are pulled to low so producing the Fine Timing Board identifying code number (for the CPU) of decimal 51.

When HCL1 and HCL2 go low, U560 is enabled. U560 is in read mode when LRHW goes low, Data D0-D7 will be transmitted to the HDD0-7 data bus.
In the write mode (LRHW=High), all incoming TTL data (HDD0-HDD7) is fed to the latch register U500 to 540.

The address decoder U562 is enabled when HDA5 goes high plus LDBV low (low-device bus valid, see theory of MPU) and when the inputs HDA3 and HDA4 of U563 go low. U562 provides the latch signal for the latch register U540 when U562 is enabled and signals HDA2 and HDA1 are high and HDA0 low.

REGISTER SECTION (Schematic 52A)

The input data D0 - D7 from U560 is written into the registers U500 to U540 when the latch-signals LCONTROL 0-3 (generated by U562/7,11,12,13) goes low and latched to the outputs when the latch-signal goes high afterwards. The TTL-signals from U540 are converted into the required ECL signals by the TTL-ECL Translator U542.

SCEW ADJUST SECTION (Schematic 52A)

This section provides the information to enable the microprocessor to compensate for the scew between data channels 0-3 in delay mode (see Adjustment procedure of the Fine Timing Board). This information is buffered by the switches S500-503 and multiplexed to the data bus by the multiplexers U570-590 and the write readtransmitter U560 in the following way:

HDA1	HDA0	LRHW	LDBV	
0	0	0	0	read scew info channel 0
0	1	0	0	read scew info channel 1
1	0	0	0	read scew info channel 2
1	1	0	0	read scew info channel 3

NOTE:

The processor samples the settings of S500 - S503 during turn-on, and whenever (via NEXT/PREV keys) Fine Timing is changed from off to on (**[Fine Timing off]** to **[Fine Timing on]** etc.)

Table 8-5-2. Mnemonics Explanation

The first letter in a mnemonic means:

H : high active
L : low active
P : the rising edge of a signal is the active
N : the falling edge of a signal is the active

Mnemonic	Explanation
D0 - D7	TTL-Databus 0-7 on the board.
HCL1, HCL2	High Control Line 1, 2.
HDA0 - HDA5	Address-lines of the devicebus.
HDD0-7	High Device Data 0-7
HDELAY	Enables the delay-mode of the Finetiming-Board.
HSERIAL	This signal indicates the Serial-Mode.
LATCH1, LATCH1A	Latch-signals for the input latches U100 and U121. In Serial-Mode LATCH1 and LATCH1A are low. The input latches U100 and U121 are transparent.
LATCH2 - LATCH5	Latch signals for the output-latches U470-U474. In Serial- and Delay-Mode LATCH2 is low. The output latch U470 is transparent.
LCEN	Low Card Enable.
LCONTROL0 - LCONTROL3	These signals write the delay-information in U500 - U530.
LDBV	Low Device Bus Valid.

LDEL1 - LDEL38	Data for the Analog-Switches U300 - U357. It's the delay information.
LDELAY	This signal low enables the Delay-Mode of the Finetiming Board.
LMHS	Low Master/High Slave.
LRHW	Low Read/High Write.

TROUBLESHOOTING (FINE TIMING BOARD A52)

General

Should a fault be isolated to the Fine Timing Board (A52), the theory of operation should be read and understood before proceeding with troubleshooting in this area.

CAUTION

Instrument must not be operated without cover over power supply and fan areas.

Procedure:

With power OFF, plug the Fine Timing Board into the 8175A test connectors.
Switch instrument ON, and Recall Standard Settings.

a) First check with a DVM that the Power Supply Voltages at the following TP's on the board are correct.

TP +15V	+15V	± 50 mV
TP +12V	+12V	± 50 mV
TP +5V	+5V	± 50 mV
TP -5.2V	-5.2V	± 50 mV
TP -12V	-12V	± 50 mV
TP -15V	-15V	± 50 mV

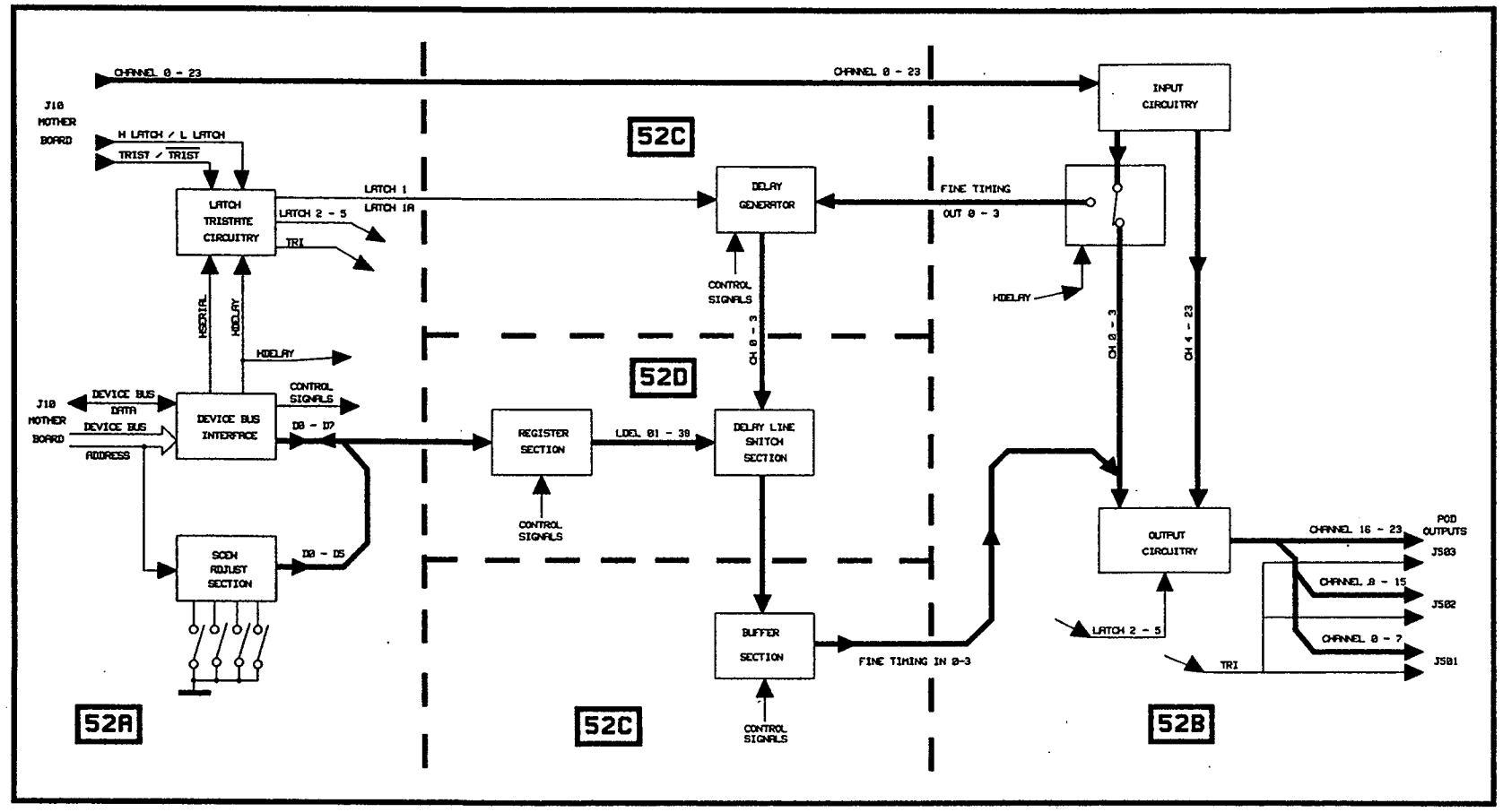


Figure 8-5-1. Fine Timing Board Block Diagram

b) For the test conditions shown in the table (configuration Par./Ser. and Fine Timing OFF or ON), confirm that the following ECL signal conditions are produced.

		SYSTEM Page		TIMING Page (Parallel Mode)	
ECL signal	U/pin	Parallel Mode	Serial Mode	Fine Timing OFF	Fine Timing ON
HDELAY	542/15			L	H
LDELAY	460/9,12 112,122/ 12			H	L
LATCH1	109/3	H able to follow HLATCH/ LLATCH	L ✓		
LATCH1A	121/6	-"-	L ✓		
LATCH2	462A/4	-"-	L ✓	H able to follow HLATCH/ LLATCH	L
LATCH3,4,5	462B/12, 13,14	-"-	H able to ✓ follow HLATCH/ LLATCH	-"-	H able to follow HLATCH/ LLATCH

c) Set 8175A:

CNTRL > CURSOR1 > NEXT = [Auto Cycle] >
DATA > CURSOR1 = Period > CH1 > DATA > NEXT > CURSOR2 = Address 0000 > ROLL# =
Address 0001 > CURSOR3 = POD2 CH7 > ↑ 24x >
PAGE > CURSOR4 = PROG1 > CURSOR5 = 1023 > CODE >
OUTPUT > NEXT = enabled >
CLOK > EXEC = UPDATE > START

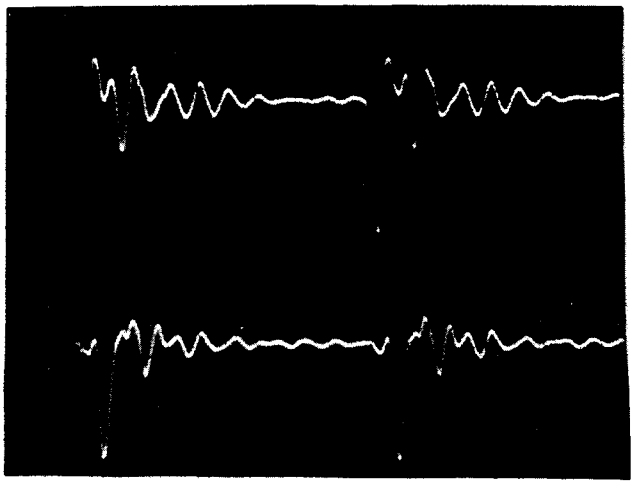
TIMING > NEXT = [Fine Timing on]

Set scope initially to: 0.02us/Div, 0.05V/Div, then change as required (see photos)

Then measure with Scope Probe 10017A, that signals at the following components (refer to the photos) are correct:

LATCH1

U101/6



LATCH1A

U121/6

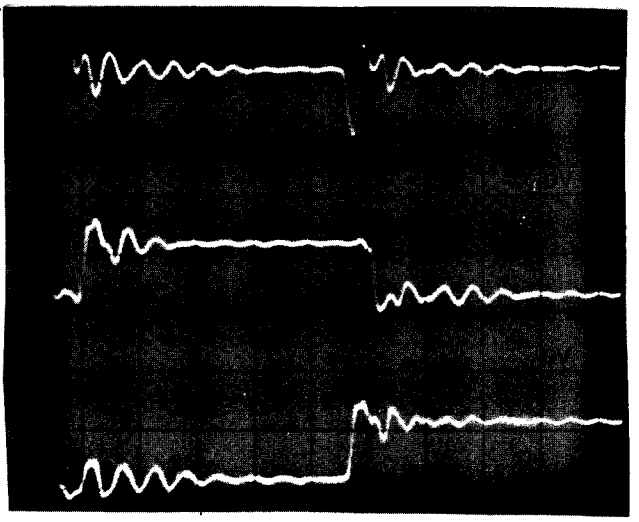
The delay depends on connection of W1/W2 or W3 and of DL1

0.1V/Div.

LATCH1
U101/6

CH0
U101/10

Q Output
U101/14

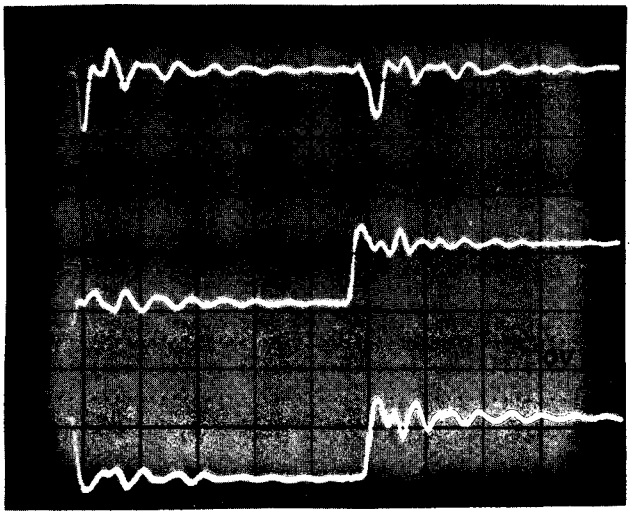


0.1V/Div.

LATCH1A
U121/6

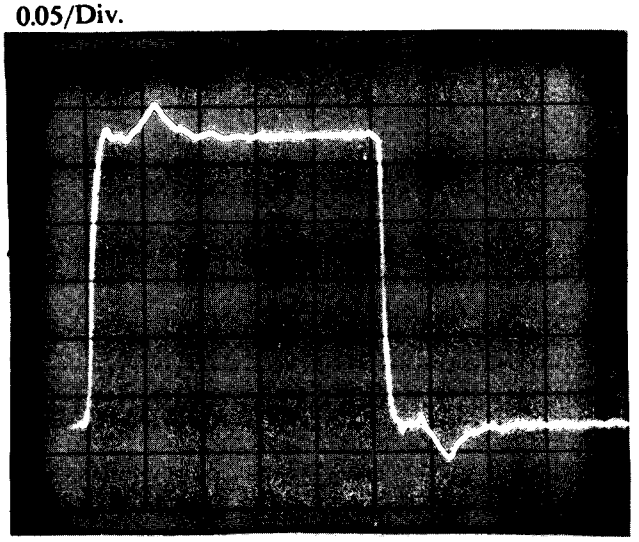
U121/10

Q Output
U121/14



0.05/Div.

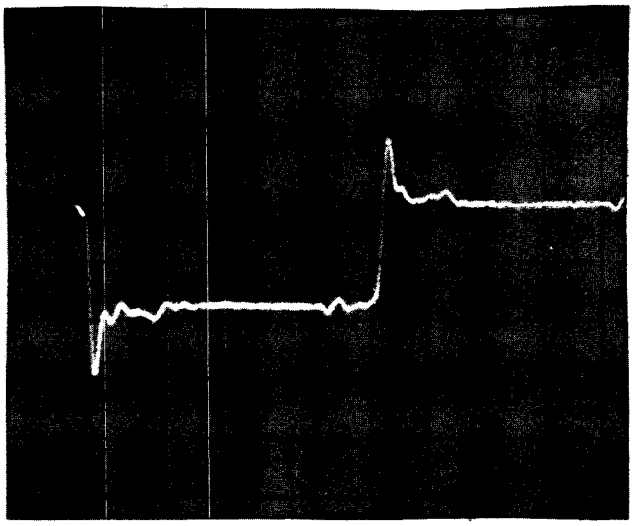
Q 201 Coll.



With delay set to 40 ns, measure the signal at TP5

0.05/Div.

TP5



Do the same check at the corresponding pins of channel 1, 2 and 3 related components.

Set the switch elements of S500 to the position shown (all to zero - 0). Press NEXT 2 times (to read in the new S500 settings).

Set 8175A: Timing Page (PAR)
[Fine Timing on]
CURSOR↓ = Channel 0 20.0 ns delay.
For each delay value shown in the following table, measure with a DVM the TTL levels at the IC pins indicated. (Do not change the S500 setting!)

Delay	LDEL / U500	01 2	02 5	03 6	04 9	05 19	06 16	07 15	08 12	S500 setting
20.0	U300/6 -12V	1	1	1	1	1	1	1	1	
20.1	U302/6 -12V	0	1	1	1	1	1	1	1	----000001
20.2		1	0	1	1	1	1	1	1	----000010
20.3		0	0	1	1	1	1	1	1	
20.4	U304/6 -12V	1	1	0	1	1	1	1	1	---000100
20.5		0	1	0	1	1	1	1	1	
20.6		1	0	0	1	1	1	1	1	
20.7		0	0	0	1	1	1	1	1	
20.8	U306/6 -12V	1	1	1	0	1	1	1	1	---001000
20.9		0	1	1	0	1	1	1	1	
21.0		1	0	1	0	1	1	1	1	
21.1		0	0	1	0	1	1	1	1	
21.2		1	1	0	0	1	1	1	1	
21.3		0	1	0	0	1	1	1	1	
21.4		1	0	0	0	1	1	1	1	
21.5		0	0	0	0	1	1	1	1	
21.6	U314/6 -12V	1	1	1	1	0	1	1	1	---010000
23.2	U312/6 -12V	1	1	1	1	1	0	1	1	---100000
26.4	U310/6 -12V	1	1	1	1	1	1	0	1	
32.8	U310/6 -12V	1	1	1	1	1	1	1	0	
49.0	U308/6 -12V	1	1	1	0	1	1	0	0	

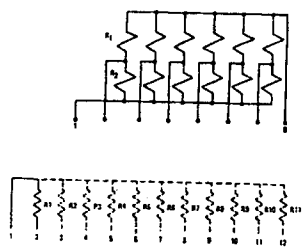
Set delay back to 20.0 ns then, for each of the S500 settings shown in the table above, check the corresponding TTL levels.
Note:
After making each new S500 setting, press NEXT 2 times (to read in the new settings).

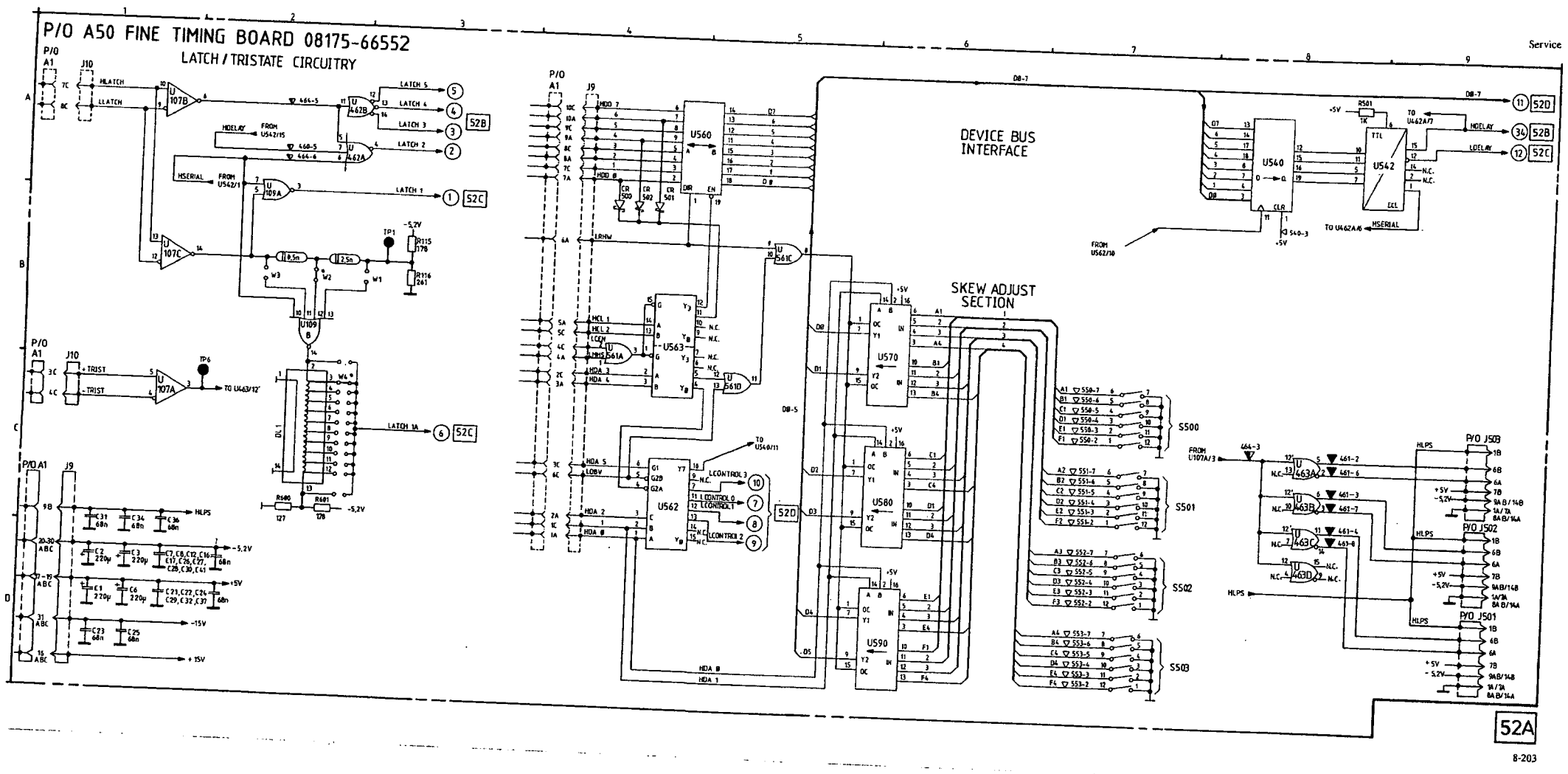
Do the same test (at appropriate pins of IC's U510, 520 and 530 etc.) for channels 1, 2, and 3. Change switch settings of S501, 502, and 503 respectively.

REF.DES.	-5.2V	+5V	-15V	+15V	GND
U107	4				1,16
U109	8				1,16
U462	8				1,16
U463	8				1,16
U560					10
U562	8	20			16
U563		8			8
U570		16			8
U580		16			8
U590		16			8

R#	POWER PIN	VOLTAGE LEVEL	RESISTOR VALUE
460	/	-5.2V	8 PIN 160/240
461	/	-5.2V	7x470
464	/	-5.2V	8 PIN 160/240
550	/	+5V	7x10K
551	/	+5V	7x10K
552	/	+5V	7x10K
553	/	+5V	7x10K

NOTE
SEE R# VALUE TABLE FOR MORE INFORMATION
PIN NUMBER OF RESISTOR PACK
RESISTOR PACK NUMBER (R#)
E.G. LINE BEING PULLED DOWN

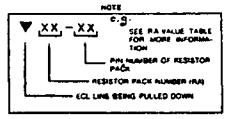


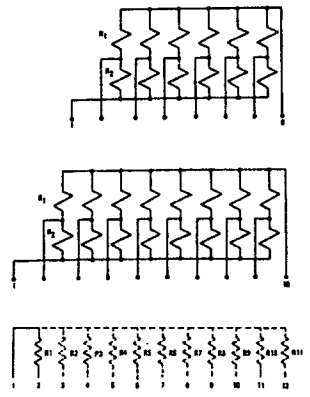


REF.DES.	-5.2V	+5V	-15V	+15V	GND
U100	8				L16
U102	8				L16
U103	8				L16
U104	8				L16
U105	8				L16
U106	8				L16
U461	8				L16
U470	16				6,7
U471	16				6,7
U472	16				6,7
U473	16				6,7
U474	16				6,7

RA	POWER PIN	VOLTAGE LEVEL	RESISTOR VALUE
460	1	-5.2V	8 PIN 160/240
469	1	-5.2V	10 PIN 160/240
470	1	-5.2V	9x150
471	1	-5.2V	9x150
472	1	-5.2V	9x150
473	1	-5.2V	9x150
474	1	-5.2V	9x150
475	1	-5.2V	9x150
476	1	-5.2V	8 PIN 160/240
477	1	-5.2V	8 PIN 160/240
478	1	-5.2V	8 PIN 160/240
479	1	-5.2V	8 PIN 160/240

NOTE (-3)





P/O A50 FINE TIMING BOARD 08175-66552

INPUT CIRCUITRY

BUFFER IN CHANNEL 0 - 23

OUTPUT CIRCUITRY

OUTPUT CHANNEL 0-23

CAUTION : U470 → U472
EXTREMLY ESD SENSITIVE

P/O J503

P/O J502

P/O J501

P002

P001

P000

52A

52B

52C

8-205

REF DES.	-5.2V	+5V	-15V	+15V	GND
U101	8				16
U112	8				16
U121	8				16
U440	8				16
U460	8				16

RA	POWER PIN	VOLTAGE LEVEL	RESISTOR VALUE
101	1	-5.2V	9x470
102	1	-5.2V	7x470
112	1	-5.2V	7x470
1000	1	-5.2V	7x470
1001	1	-5.2V	7x470

NOTE

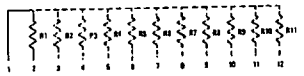
XX - XX

SEE P.A.VALUE TABLE FOR MORE INFORMATION

PIN NUMBER OF RESISTOR PACK

RESISTOR PACK NUMBER (R-S)

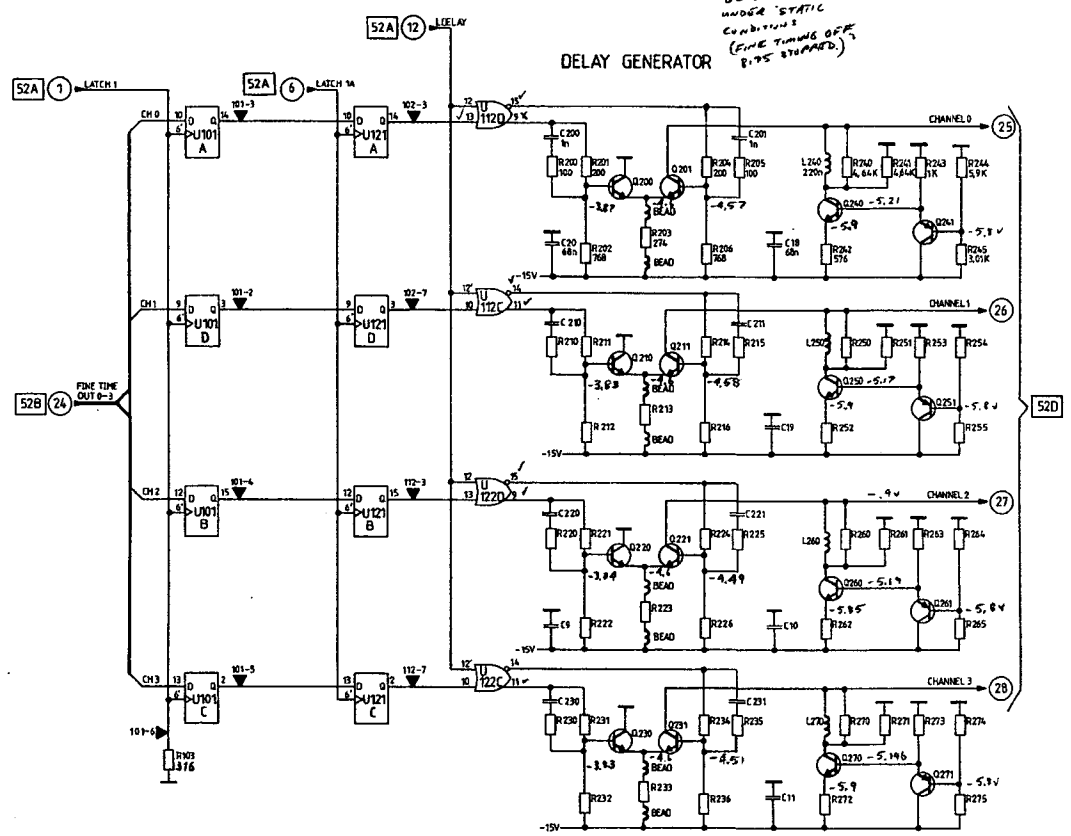
ECL LINE BEING PULLED DOWN



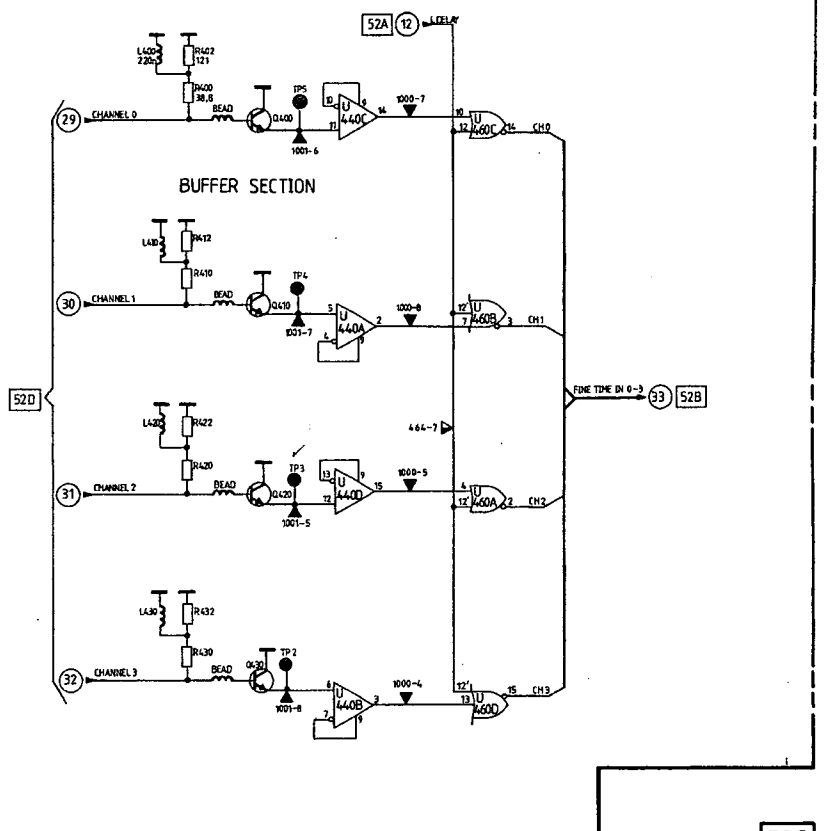
P/O A50 FINE TIMING BOARD 08175-66552

DC VOLTAGES UNDER STATIC CONDITIONS (FINE TIMING OFF, 8.75 STORED)

DELAY GENERATOR



BUFFER SECTION

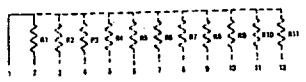


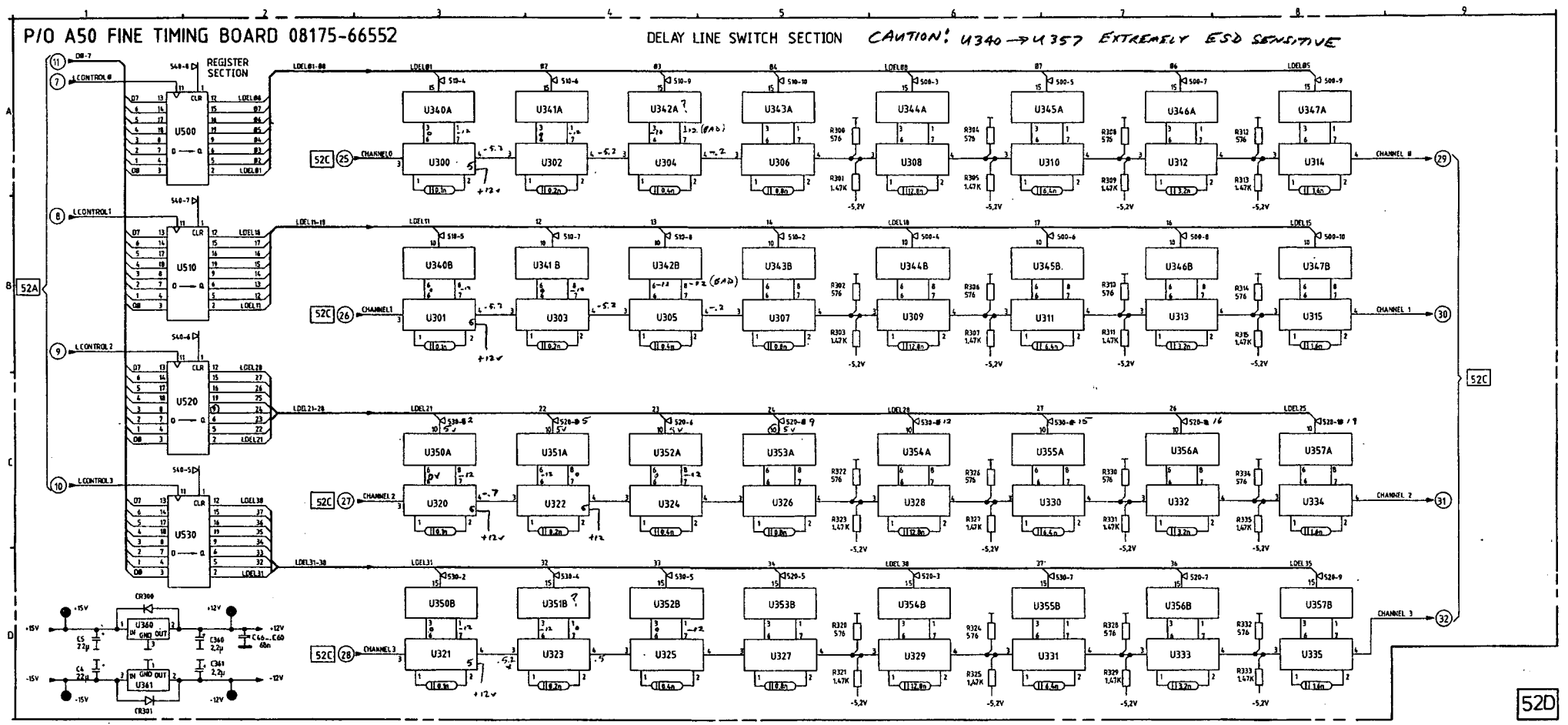
52C

REF.DES.	-5.2V	+5V	-15V	+15V	GND
U300				5	
U301				5	
U302				5	
U303				5	
U304				5	
U305				5	
U306				5	
U307				5	
U308				5	
U309				5	
U310				5	
U311				5	
U312				5	
U313				5	
U314				5	
U315				5	
U320				5	
U321				5	
U322				5	
U323				5	
U324				5	
U325				5	
U326				5	
U327				5	
U328				5	
U329				5	
U330				5	
U331				5	
U332				5	
U333				5	
U334				5	
U335				5	
U340	4,5,9,16	12	14	11	13
U341	4,5,9,16	12	14	11	13
U342	4,5,9,16	12	14	11	13
U343	4,5,9,16	12	14	11	13
U344	4,5,9,16	12	14	11	13
U345	4,5,9,16	12	14	11	13
U346	4,5,9,16	12	14	11	13
U347	4,5,9,16	12	14	11	13
U350	4,5,9,16	12	14	11	13
U351	4,5,9,16	12	14	11	13
U352	4,5,9,16	12	14	11	13
U353	4,5,9,16	12	14	11	13
U354	4,5,9,16	12	14	11	13
U355	4,5,9,16	12	14	11	13
U356	4,5,9,16	12	14	11	13
U357	4,5,9,16	12	14	11	13
U500		20			10
U510		20			10
U520		20			10
U530		20			10

RA	POWER PIN	VOLTAGE LEVEL	RESISTOR VALUE
500	1	-5.2V	9x10K
510	1	-5.2V	9x10K
520	1	-5.2V	9x10K
530	1	-5.2V	9x10K
540	1	-5.2V	7x10K

NOTE #3
XX-XX
SEE RA VALUE TABLE FOR MORE INFORMATION
PIN NUMBER OF RESISTOR PACK
RESISTOR PACK NUMBER #3
ECL LINE BEING PULLED DOWN





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Arranged alphabetically by country

Product Line Sales/Support Key

Key Product Line
- A Analytical
- CM Components
- C Computer Systems
- E Electronic Instruments & Measurement Systems
- M Medical Products
- P Personal Computation Products
- * Sales only for specific product line
- ** Support only for specific product line

IMPORTANT:These symbols designate general product line capability.They do not insure sales or support availability for all products within a line, at all locations.Contact your local sales office for information regarding locations where HP support is available for specific products.

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Telex: 380 3589/ACT BA
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Corso Svizzera, 185
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IVORY COAST

S.I.T.E.L.
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Bd. Giscard d'Estaing
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ABIDJAN 01
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Yokogawa-Hewlett-Packard Ltd.
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KOBE, 650
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KYOTO, 600
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Northrop Instruments & Systems Ltd.
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P

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Imtac LLC
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Telex: 2894 MUSKO PK
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Calle Samuel Lewis, Ed. Alfa
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Telex: 3483 ELECTRON PG
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Cia Electro Médica S.A.
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San Isidro
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LIMA 1
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Manual for Model Number	8175A Option 002
Manual printed on	October 1986
Manual Part Number	08175-90011

Make all ERRATA corrections.

Check the following table for your instrument serial prefix/serial number and make the listed changes to your manual.

▶ New Item

Serial Prefix or Serial Number		Manual Changes	Serial Prefix or Serial Number	Manual Changes
ERRATA				
2612G00416	and above	1		
2642G00716	and above	2		
2642G00956	and above	3		
2948G01686	and above	4		
2948G01706	and above	5		
2948G02146	and above	6		

MODEL 8175A Option 002

INDEX OF MANUAL CHANGES

MANUAL CHANGE	MISCELLANEOUS	FRAME	A70
ERRATA			
1			MP505,506,508,509, MP510,511,512,513, MP805,806,808,809, MP810,811,812,813
2	Page 5-26, 8-233		R405,493 R705,793
3			C208,210,443,503, C507,508,519,520, C521,522,743,803, C807,808,819,820, C821,822
4			U414,415,714,715
5			R585,586,885,886
6			C208,210,503,507, C508,519-522,803, C807,819-822

ERRATA

On Page 6-28 delete:

	A70 WRT	1258-0124	PIN PROG JUMPER
add:	A70 WR1	1258-0124	PIN PROG JUMPER

On Page 6-26, Delete:

	R465	0698-3558
	R466	0757-0438
Add:	R465	0757-0438
	R466	0698-3558

On Page 3-88, change to read:

Arb. related Commands of the OUTPUT Page:

```
.............
.............
Disable/Enable Arb. channel          CHN   CHN,0/1   -     C4
.............
.............
```

MANUAL CHANGE 1

On Page 6-25, change the Table of Replaceable Parts to read:

A70	MP505,506,508,509, MP510,511,512,513, MP805,806,808,809, MP810,811,812,813	1205-0662	HEATSINK

MANUAL CHANGE 2

On Page 5-26, Adjustments, change to read:

7. UAVC Gain A Adjust

   Measure with DVM at TP410

	Board Rev. A,B	Rev.C
Adjust A70R459 for	-1.2000V+/-.1mV	-0.8000V+/-.1mV

11. UAVC Gain B Adjust

    Measure with DVM at TP710

	Board Rev. A,B	Rev.C
Adjust A70R759for	-1.2000V+/-.1mV	-0.8000V+/-.1mv

On Page 6-26/27, change the Table of Replaceable Parts to read:

A70	R405,705	0698-7220	R-FXD 215 1% .05W
ADD:	R493,793	0698-7611	R-FXD 536 1% .125W

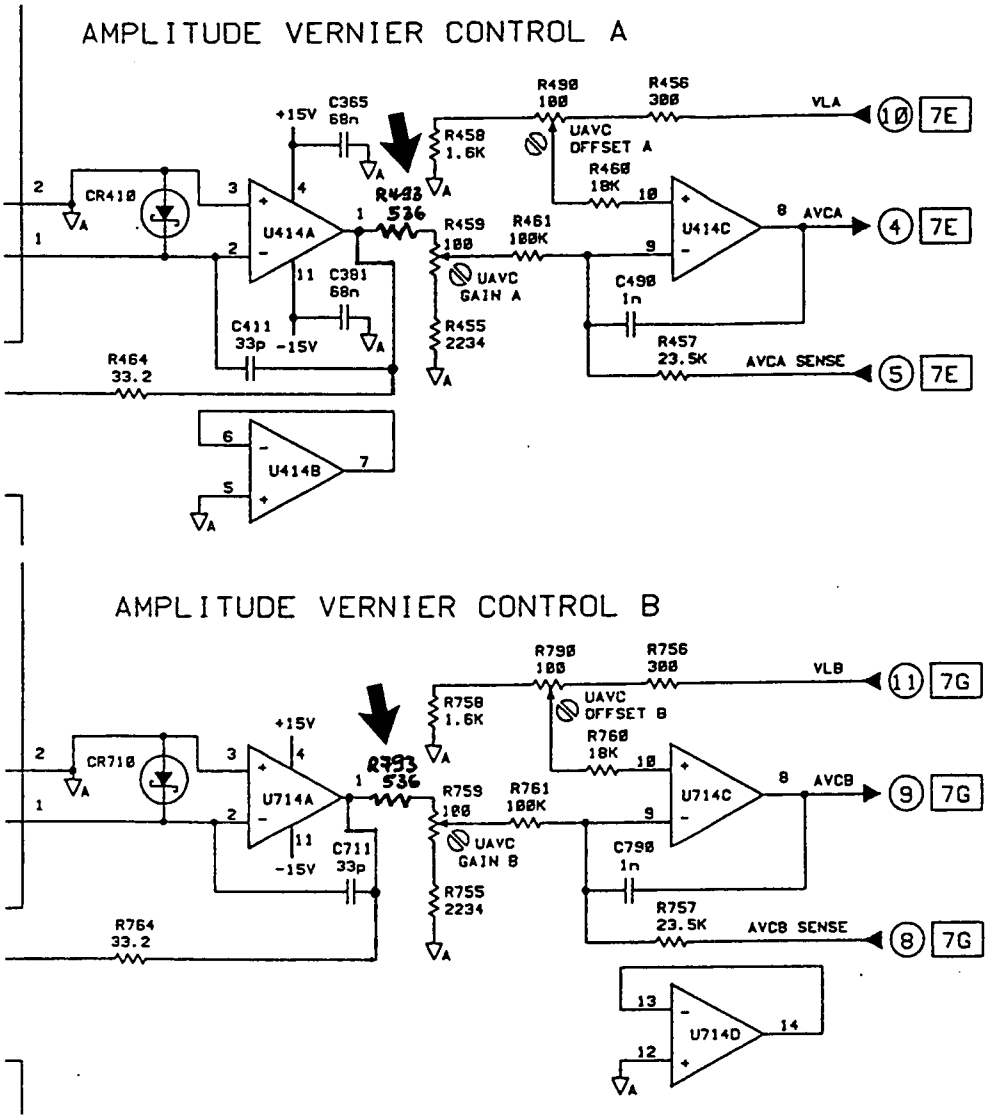
On Page 8-226 step 3. Amplitude Vernier Control Output A/B change Table 8-6-1 to read:

Table 8-6-1.

	Ampl. Range	AVCA Att. Factor	Bd. REV A,B AVCA/AVCB	REV C AVCA/AVCB
into 50 Ohm	0.2 V	1/2.5	+ .120 V - 1.2 V	+ .280 V - .800 V
	0.5 V	1/1	+ .120 V + .120 V	+ .280 V + .280 V
	1 V	1/2.5	- 1.2 V + .120 V	- .800 V + .280 V
	2 V	1/2.5	- .8 V	- .440 V
	5 V	1/1		
	10 V	1/2.5		
	16 V	1/1.25		
into open	0.5 V	1/2	- .100 V - 1.2 V	+ .100 V - .800 V
	1 V	1/1	+ .120 V - .100 V	+ .280 V + .100 V
	2 V	1/2.5	- 1.2 V + .120 V	- .800 V + .280 V
	5 V	1/2	- 1.2 V	- .800 V
	10 V	1/1		
	20 V	1/2.5		
	32 V	1/1		

MANUAL CHANGE 2 (Cont.)

On Page 8-233, change schematic 7B to read:



MANUAL CHANGE 3

On Page 6-23, change the Table of Replaceable Parts to read:

A70	C208,210,443,503, C507,508,519,520, C521,522,743,803, C807,808,819,820, C821,822	0160-6596	C-FXD .47UF 20%

MANUAL CHANGE 4

On Page 6-28, change the Table of Replaceable Parts to read:

A70	U414,415,714,715	1826-2177	IC AD713JN

MANUAL CHANGE 5

On Page 6-27/28, change the Table of Replaceable Parts to read:

A70	R585,586,885,886	0699-2863	R-FXD 29.11 .1% 2W

MANUAL CHANGE 6

On Page 6-23/24, change the Table of Replaceable Parts to read:

A70	C208,210,503,507 C508,519-522,803 C807,808,819-822	0160-3097	CAP 0.47uF 50V

8175A OPTION 002 (ARB)
OPERATING AND SERVICE MANUAL

PART NUMBER: 08175-90011

Please note the following:

This manual package for Option 002 comprises two parts: a bound Operating and Programming manual and a set of loose leaf pages which comprise the "Service Manual". The loose leaf pages are designed to be included at the end of each corresponding section within the standard 8175A manual 3 ring binder. They are numbered so as to follow on directly from the standard ones. Note that The Arb. Board service block should be inserted behind its register (supplied with this package) at the back of the standard service section.

HEWLETT PACKARD

OPERATING AND SERVICE MANUAL

8175A
Option 002

This manual applies directly to all 8175A's which have option 002 installed. Any changes made to the option which affect the manual, will be detailed in a "Manual Changes" supplement supplied with it. Ensure that you read through any such supplement and record the changes in your manual.

HERRENBERGER STR. 130, D-7030 BOEBLINGEN
FEDERAL REPUBLIC OF GERMANY

MANUAL PART No. 08175-90011
MICROFICHE PART No. 08175-95011

PRINTED: JUNE 1986

HEWLETT PACKARD

CERTIFICATION

Hewlett-Packard Company certifies that this product met its published specifications at the time of shipment from the factory. Hewlett-Packard further certifies that its calibration measurements are traceable to the United States National Bureau of Standards, to the extent allowed by the Bureau's calibration facility, and to the calibration facilities of other International Standards Organization members.

WARRANTY

This Hewlett-Packard product is warranted against defects in material and workmanship for a period of one year from date of shipment. During the warranty period, Hewlett-Packard Company will, at its option, either repair or replace products which prove to be defective.

HP warrants that its software and firmware designated by HP for use with an instrument will execute its programming instructions when properly installed on that instrument. HP does not warrant that the operation of the instrument, or software, or firmware will be uninterrupted or error free.

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LIST OF CONTENTS Option 002 (Arb.)

NOTE: The Option 002 (Arb.) pages listed below are assigned numbers which follow on directly from the corresponding standard 8175A service manual pages. It is suggested that you insert the pages at the appropriate positions in the standard 8175A service manual binder.

SECTION 5A Adjustments Procedure (Arb.)

SECTION 6A Replaceable Parts (Arb.)

SECTION 7A Backdating (Arb.)

No Backdating applicable when manual printed

SECTION 8A Service (Arb.)

SECTION 5 A

ADJUSTMENTS (ARB)

5-1 INTRODUCTION

This section describes the adjustments which will return the Arb. related outputs of the instrument to peak operating condition after repairs have been completed. An adjustment location diagram is given on a foldout page at the end of this section.

5-2 SAFETY CONSIDERATIONS

Although this instrument has been designed in accordance with internal safety standards, this manual contains information, cautions and warnings which must be followed to ensure safe operation and to retain the instrument in a safe condition (see Sections 2 and 3 of the Arb. Operating and Programming manual).

WARNING

Any interruption of the protective (grounding) conductor (inside or outside) or disconnection of the protective earth terminated is likely to make the instrument dangerous. Intentional interruption is prohibited.

Any adjustment, maintenance or repair of the opened instrument with voltage applied should be avoided as much as possible and, when inevitable, should be carried out only by a skilled person who is aware of the hazard involved.

5-3 EQUIPMENT REQUIRED

The test equipment required for the adjustment procedure is listed in Table 1-1, Recommended Test Equipment. The critical specifications of substitute test instruments must meet the standards set forth in Table 1-2, Specifications.

5-4 ADJUSTMENT PROCEDURE

The Arb. Adjustment procedure is numbered: 5-11 since the last procedure for the standard 8175A is 5-10.

NOTE:

The Arb. Adjustment procedure requires that a controller is available (e.g. HP Series 200 Controller). Significant programs are given.

The following Adjustment procedure enables the Dual Arbitrary Waveform Generator to be adjusted within the published specifications.
However, only by using a special procedure can the best possible calibration and hence performance be achieved. This special additional calibration can only be done by an HP Service Office or if the required test equipment and the Calibration program (VERICAL) is available.

An adjustment points locator diagram (Figure 5-2) is included at the end of this adjustment procedure.

Execute a paragraph completely and in the order in which it is presented. Only the significant instrument settings are given. Screen display figures are included to assist verification that the correct settings have been made. Ensure, that in such cases, your 8175A settings are identical to those of the screen displays given.

For adjustments on the Dual Arbitrary-Waveform Generator Board use the service connectors (as for the standard 8175A) as shown in Figure 5-1.

Allow a 30 minute warm-up period before starting the adjustments.

CAUTION

Instrument must not be operated without cover over power supply and fan areas.

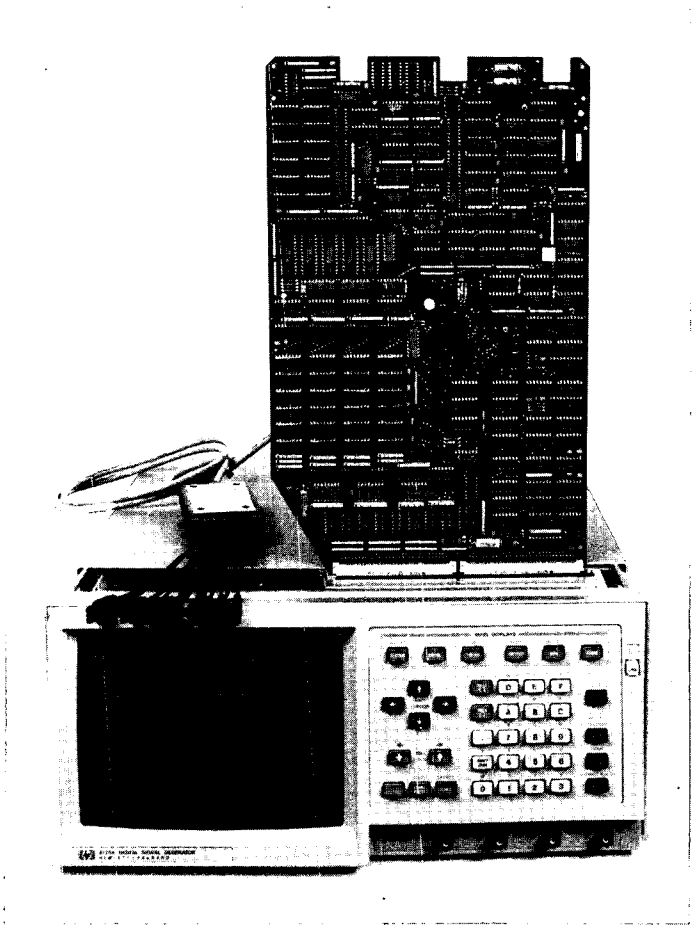


Figure 5-1. 8175A Service Position

5-11 ARB BOARD (OPTION 002)

Equipment: Controller, Printer, DVM, Scope, Probe 10021A
VERICAL Disc, SMB-BNC Cables

Procedure:

1. With power OFF, disconnect the four 50 Ohm cables, then remove the ARB Bd. from its normal position and plug it into the Service Connector.

   Turn power ON. The System Page configuration menu should be displayed.

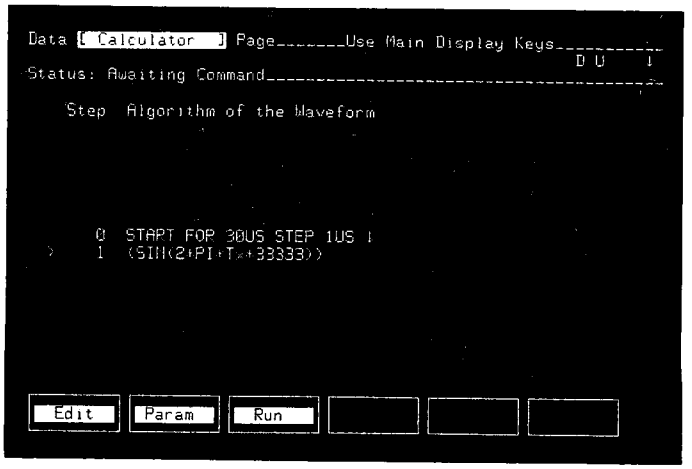
2. Make the following 8175A settings:

   Recall Standard Settings
   SYSTEM = [Configuration] > CURSOR ↓ = Arbitrary-Generator (ARB)
   CNTRL = [Clock] change Mode to [Auto Cycle]
   OUTPUT > NEXT
   change Level [ARB A]: into [open]
   Amplitude Range: [10V]
   Output: [enabled]
   Trigger Outputs: [enabled]
   OUTPUT > NEXT
   do the same changes for Level [ARB B]
   DATA > PREV
   on Data [Calculator] Page set up the following sinewave module:

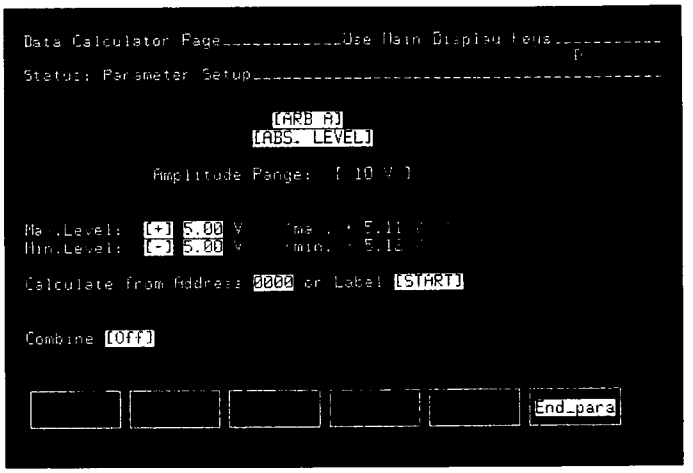
HEADER	>0	START FOR 30US STEP 1US
ALGORITHM	1	(SIN(2*PI*Tx*33333))

   The "Softkeys" are available via the corresponding *MAIN DISPLAY* keys.

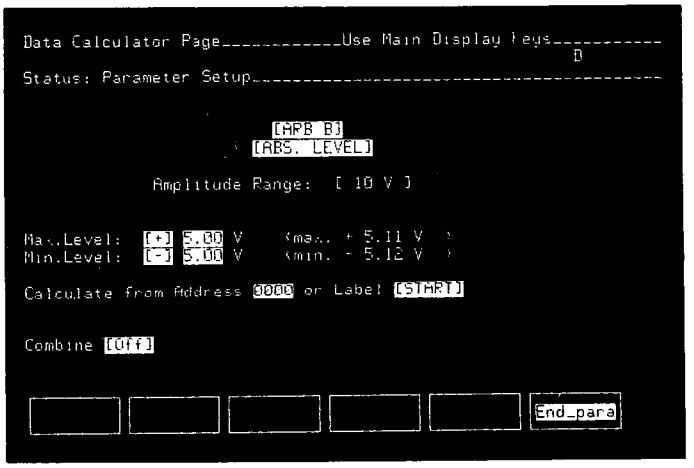
   "Edit" = *SYSTEM* > "Insert" = *SYSTEM* > S > T > A > R > T > DON'T CARE >
   "FOR" = *SYSTEM* > DON'T CARE > 3 > 0 > U > S > DON'T CARE >
   "STEP" = *CNTRL* > DON'T CARE > 1 > U > S > "Etc" = *PRGM* 5times >
   "Cr/lf" = *DATA* > "Etc" = *PRGM* 2times > "*" = *TIMING* 3times >
   "Etc" > ")" = *CNTRL* 2times > CURSOR ← 5times > "(" = *SYSTEM* 2times >
   CURSOR ← > "Etc" 2times > "Sin" = *SYSTEM* > CURSOR → > 2 > CURSOR → >
   "PI" = *DATA* > "Etc" > CURSOR → > "Tx" = *OUTPUT* > CURSOR → > 3
   5times > "Etc" > "End_ins" = *DATA* > "End_edit" = *PRGM*



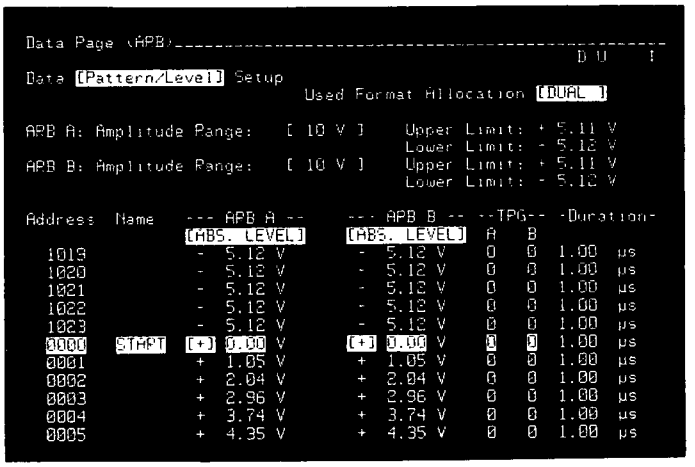
"Param" = *CNTRL* >
change: Max. Level: [+] 5.00 V
Min. Level: [-] 5.00 V



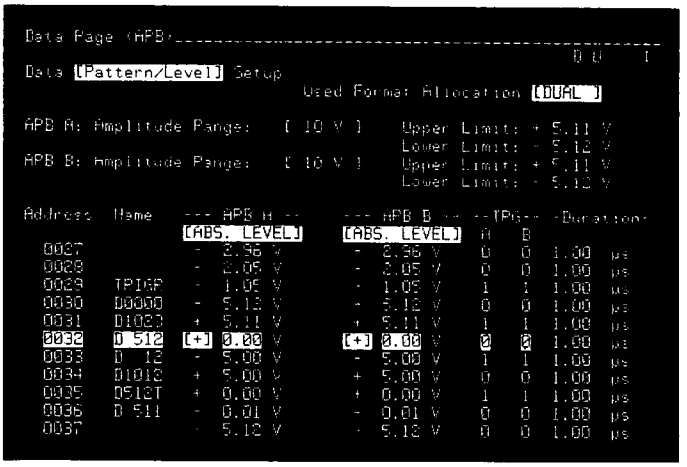
"End_para" = *PRGM* > "Run" = *TIMING*
"Param" = *CNTRL* > NEXT = [ARB B] >
check : Max. Level: [+] 5.00 V
Min. Level: [-] 5.00 V



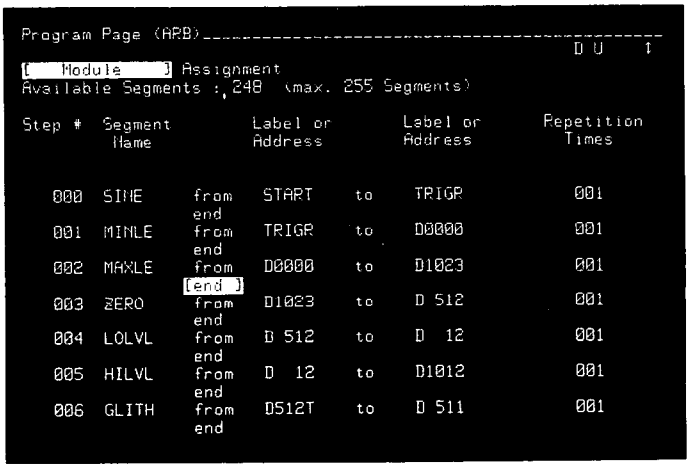
"End_para" = *PRGM* > "Run" = *TIMING* > NEXT 2times



CURSOR ↓ 3times = Address 0000 > 0 > 0 > 2 > 9 > CURSOR → >
T > R > I > G > R > CURSOR → 8times = TRIG A > 1 > 1 >
ROLL ↑ > blue and CURSOR → = LABEL ← 6times >
D > 0 > 0 > 0 > 0 > ROLL ↑ > LABEL ← >
D > 1 > 0 > 2 > 3 > NEXT = [+] > 5 > 1 > 1 > CURSOR → > NEXT = [+] >
5 > 1 > 1 > CURSOR → > 1 > 1 > ROLL ↑ > LABEL ← 6times >
D > DON'T CARE > 5 > 1 > 2 > NEXT = [+] > 0 > 0 > 0 > CURSOR → >
NEXT = [+] > 0 > 0 > 0 > ROLL ↑ > LABEL ← 4times
D > DON'T CARE 2times > 1 > 2 > CURSOR → 2times > 5 > 0 > 0 >
CURSOR → 3times > 0 > 0 > CURSOR C > 1 > 1 > ROLL ↑ > LABEL ← 6times >
D > 1 > 0 > 1 > 2 > NEXT = [+] > 5 > 0 > 0 > CURSOR → > NEXT = [+] >
5 > 0 > 0 > ROLL ↑ > LABEL ← 4times >
D > 5 > 1 > 2 > T > NEXT = [+] > 0 > 0 > 0 > CURSOR → > NEXT = [+] >
0 > 0 > 0 > CURSOR → > 1 > 1 > ROLL ↑ > LABEL ← 6times >
D > DON'T CARE > 5 > 1 > 1 > CURSOR → > 0 > 0 > 1 > CURSOR → 2times >
0 > 0 > 1 > ROLL ↓ 4times



PRGM = [Module] > CURSOR ↓ >
S > I > N > E > DON'T CARE > LABEL → 3times > T > R > I > G > R >
ROLL ↑ > blue and SYSTEM = INSERT >
M > I > N > L > E > CURSOR → > T > R > I > G > R > CURSOR → >
D > 0 > 0 > 0 > 0 > ROLL ↑ > INSERT >
M > A > X > L > E > CURSOR ← > D > 0 > 0 > 0 > 0 > CURSOR → >
D > 1 > 0 > 2 > 3 > ROLL ↑ > INSERT >
Z > E > R > 0 > DON'T CARE > CURSOR → > D > 1 > 0 > 2 > 3 > CURSOR → >
D > DON'T CARE > 5 > 1 > 2 > ROLL ↑ > INSERT >
L > 0 > L > V > L > CURSOR → > D > DON'T CARE > 5 > 1 > 2 > CURSOR → >
D > DON'T CARE 2times > 1 > 2 > ROLL ↑ > INSERT >
H > I > L > V > L > CURSOR → > D > DON'T CARE 2times > 1 > 2 >
CURSOR → > D > 1 > 0 > 1 > 2 > ROLL ↑ > INSERT >
G > L > I > T > H > CURSOR → > D > 5 > 1 > 2 > T > CURSOR → >
D > DON'T CARE > 5 > 1 > 1 > ROLL ↓ 6times >



3. Set 8175A:

```
PRGM > NEXT = [Trigger Event] Assignment
      check:      On START execute [SINE]
UPDATE > START
```

Connect the Outputs via 08160-61610 Cables to a Scope.

Allow a 30 minutes warm-up period before starting the adjustments!
Within that time confirm that the following Reference Voltages are correct:

The GND clip should always be connected to the nearest GND TP on Bd. !

TP + 10 VR	+ 10.000 V	+/- 10 mV
TP - 10 VR	- 10.000 V	+/- 10 mV
TP 404	+ 1.000 V	+/- 1 mV
TP 704	+ 1.000 V	+/- 1 mV

Before the Adjustment Procedure can be started, the EEPROM in the Calibration Circuitry must be set to a defined status. Therefore, first read out and print the stored calibration data, as follows:

The following program enables the EEPROM data to be read and printed.
An external printer, enables the data to be documented.
7xx is the HP-IB address of the HP 8175A.
7yy is the HP-IB address of the external printer

Input:

```
10   FOR A = 1 TO 112
20        OUTPUT 7xx; "HW0,41,";A          ! Set EEPROM address
30        OUTPUT 7xx; "HW?0,0,48"          ! Read EEPROM data
40        Enter 7xx;Dat
50        PRINTER IS 7yy
60        PRINT "Address: ";A;"  Data: ";Dat
70   NEXT A
80   LOCAL 7xx
90   PRINTER is 1
100  STOP
```

Set the Jumper on the circuit side of the board A70 to the "WRT" position.

The following program enables the EEPROM to be set to the defined status.

Input:

```
10   FOR A = 1 TO 112
20        OUTPUT 7xx;"HW0,41,";A           ! Set EEPROM address
30        OUTPUT 7xx;"HW0,48,";128         ! Write EEPROM data
40   NEXT A
50   STOP
```

Using the first program check that all addresses (1-112) are set to Data: 128.

A/B AMPLITUDE VERNIER ADJUSTMENTS

4. On Program Page(ARB) [Trigger Event] Assignment >
   change: On START execute [ZERO]
   CNTRL = [Clock] change Mode: [Single Cycle]
   UPDATE > START

   With a controller connected to the 8175A via HP-IB, input the following program:

   ```
   OUTPUT 7xx;"HW0,32,000"
   OUTPUT 7xx;"HW0,33,224"
   ```
   (7xx = 8175A HP-IB Address)

5. *UAVC Offset A Adjust*
   Measure with DVM at TP 410.
   Adjust A70R490 for +1.0000 V +/- 0.1mV.

6. Return 8175A to local. OUTPUT = Level [ARB A]
   change the Amplitude Range from [10V] to [5V] and back to [10V].

7. *UAVC Gain A Adjust*
   Measure with DVM at TP410.
   Adjust A70R459 for -1.2000 V +/- 0.1mV.

   NOTE! REV C BOARDS
   ADJUST TO −.80000 ± 0.1mv

8. Input the following program:

   ```
   OUTPUT 7xx;"HW0,36,000"
   OUTPUT 7xx;"HW0,37,224"
   ```

9. *UAVC Offset B Adjust*
   Measure with DVM at TP710.
   Adjust A70R790 for +1.0000V +/- 0.1mV.

10. Local 8175A. OUTPUT > NEXT = Level [ARB B]
    change Amplitude Range from [10V] to [5V] and back to [10V].

11. *UAVC Gain B Adjust*
    Measure with DVM at TP710.
    Adjust A70R759 for -1.2000V +/- 0.1mV.

    NOTE! REV C BOARDS
    ADJUST TO −.80000 ±0.1mv

A/B GAIN PREADJUST

12. On Program Page (ARB) [Trigger Event] Assignment
    change: On START execute [MAXLE]
    UPDATE > START

13. Measure with DVM at TP402 <= + 1.000 V
    at TP702 <= + 1.000 V

14. On the same page, change to read:

    On START execute [MINLE]
    UPDATE > START

15. Measure with DVM at TP402 - 0.4V to -0.8V.
    Center A70R409 if necessary.

    Measure with DVM at TP702 - 0.4V to -0.8V.
    Center A70R709 if necessary.

A/B SUMMING AMPLIFIER BALANCE

16. On same Page change to read:

    On START execute [SINE]
    CNTRL = [Clock] change Mode to [Auto Cycle]
    DATA > NEXT = Data [Format] Allocation
    change Period 0.1 [us]
    UPDATE > START

17. Measure with DVM at A70R447 wiper and preadjust A70R447 for 0V +/- 10 mV.
    Center R443.

    Measure with DVM at A70R747 wiper and preadjust A70R747 for 0V +/- 10 mV.
    Center R743.

18. Measure with Scope via Probe 10021A at:

    TP406. Adjust A70R432 for min sine signal (+ Balance)
    TP405. Adjust A70R441 for min sine signal (- Balance)
    TP407. Adjust A70R432/441 for min sine signal

    TP706. Adjust A70R732 for min sine signal (+ Balance)
    TP705. Adjust A70R741 for min sine signal (- Balance)
    TP707. Adjust A70R732/741 for min sine signal

    Test limit < 12 mVpp.

A/B SUMMING AMPLIFIER OFFSET

19. CNTRL = [Clock] change Mode to [Single Cycle]
PRGM = Program Page [Trigger Event] Assignment
change: On START execute [Zero]
OUTPUT change on Output Page (ARB)
Level [ARB A] into [open]
Amplitude Range: [2V]
UPDATE > START

20. *Range Error Adjust A*
Measure with DVM via Probe 10021A at TP403.

21. Adjust A70R443 for 0V +/- 0.5mV.

22. *Sum Amp Offset Adjust A*
Change the Amplitude Range to [10V].
Press START.

23. Adjust A70R447 for 0V +/- 0.5mV.

24. Change the Amplitude Range to [5V] and press START.
Check for 0V +/- 0.5mV.
Repeat steps 19 to 23 and readjust R443 and/or R447 if necessary.

25. Repeat steps 20 to 24 for Output B = [ARB B] into [open].
Measure with DVM at TP703 via Probe 10021A.
Range Error Adjust B
Adjust A70R743 for Amplitude Range [2V]
Range Error Adjust B
Adjust A70R747 for Amplitude Range [10V]

Press START after each change of Amplitude Range.

A/B LOW FREQUENCY GAIN

26. CNTRL = [Clock] change Mode to [Auto Cycle].
PRGM = Program Page [Trigger Event] Assignment
change: CONTINUOUS-Start [HILVL]
DATA > NEXT = Data [Format] Allocation, Duration: [fixed]
change: Period: 1.00 [ms]
OUTPUT change Amplitude Range A and B to [10V] into [open]
UPDATE > START

27. Connect OUTPUT A J702 to scope.
Adjust A70R515 for best pulse flatness.

28. Connect OUTPUT B J703 to scope.
Adjust A70R815 for best pulse flatness.

A/B OFFSET VERNIER

29. CNTRL = [Clock] change Mode to [Single Cycle]
PRGM = Program Page [Trigger Event] Assignment
check: On START execute [Zero]
UPDATE > START

30. *Offset-Offset Adjust A*
Connect OUTPUT A J702 to DVM using a 50 kOhm load

31. Adjust A70R454 for 0V +/- 15mV.

32. OUTPUT = Output Page (ARB) Level [ARB A]
change Output Mode: [complement]
Check for 0V +/- 15mV.
Switch between normal/complement several times and readjust A70R454 for best values symmetrical to 0V.

33. *Offset Gain Adjust A*
Set Output Mode to [normal]
Input following program via a controller connected to the 8175A

```
OUTPUT 7xx;"HW0,34,128"
OUTPUT 7xx,"HW0,35,028"
```

34. Adjust A70R451 for +16.00V +/- 25 mV.

35. Input following program

```
OUTPUT 7xx;"HW0,34,128"
OUTPUT 7xx;"HW0,35,012"
```

36. Measure with DVM for -16.00V +/- 25 mV.

37. Repeat steps 33 to 36 and readjust A70R451 for best symmetrical values.
Local 8175A.
Repeat steps 20 to 36 and readjust A70R454 / A70R451 if necessary.

38. *Offset-Offset Adjust B*
Connect OUTPUT B J703 to the DVM via 50 kOhm load.

39. Adjust A70R754 for 0V +/- 15mV.

40. Local 8175A.
OUTPUT > NEXT = Output Page (ARB) Level [ARB B]
change Output Mode: [complement]
Check for 0V +/- 15mV.
Switch between normal/complement several times and adjust A70R754 for best values symmetrical to 0V.

41. *Offset Gain Adjust B*
Input following program:

```
OUTPUT 7xx; "HW0, 38, 128"
OUTPUT 7xx; "HW0, 39, 028"
```

42. Adjust A70R751 for +16.00V +/- 25mV.

43. Input following program:

```
OUTPUT 7xx; "HW0, 38, 128"
OUTPUT 7xx; "HW0, 39, 012"
```

44. Measure with DVM for -16.00V +/- 25mV.

45. Repeat steps 41 to 44 and readjust A70R751 for best symmetrical values.
Local 8175A.
Repeat steps 38 to 44 and readjust A70R754 / A70R751 if necessary.

A/B AMPLITUDE ACCURACY

46. Local 8175A.
OUTPUT check Level [ARB A] and [ARB B] for

Amplitude Range: [10V] into [open]
Output: [enabled]
Output Mode: [normal]
CNTRL = [Clock] check for Mode: [Single Cycle]
PRGM = Program Page [Trigger Event] Assignment
change: On START execute [HILVL]
UPDATE > START

47. *ECL-DAC-Gain Adjust A*
Connect OUTPUT A J702 to DVM using 50 kOhm load.

48. Adjust A70R409 for +5.000V +/- 15mV.

49. OUTPUT = Level [ARB A]
change Output Mode: [complement].

50. Check for - 5.000V +/- 15mV.

51. Switch between normal/complement and adjust A70R409 for best symmetrical values.
(If necessary switch between normal/complement and readjust A70R409 for +5V/-5V +/- 25mV.)

52. PRGM = Program Page [Trigger Event] Assignment
Change: On START execute [LOLVL]
UPDATE > START
OUTPUT = Level [ARB A] Output Mode: [normal]

53. Switch between normal/complement and check for +5V/-5V +/-15mV.

54. *ECL-DAC-Gain Adjust B*
Connect OUTPUT B J703 to DVM using 50 kOhm load.
Repeat step 46.

55. Adjust A70R709 for +5.000V +/- 15mV.

56. On Output Page [ARB B] change the Output Mode to [complement]
and check for - 5.000V +/- 15mV.

57. Switch between normal/complement and adjust A70R409 for best symmetrical value.
(If necessary switch between normal/complement and readjust A70R709 for +5V/-5V +/- 25mV.)

58. Repeat step 52. Switch on OUTPUT Page [ARB B] between normal/complement and check for +5V/-5V +/-25mV.

59. Set both Output Modes to [normal].

A/B GLITCH REJECT

60. CNTRL = [Clock] change Mode to [Auto Cycle]
DATA = Data [Format] Allocation, Duration: [fixed]
change: Period: 0.1 [us]
PRGM = Program Page [Trigger Event] Assignment
change: CONTINUOUS-Start [GLITH]
UPDATE > START

61. *Glitch Minimizing A*
Connect OUTPUT A J702 to scope .

62. Adjust A70R471 for symmetrical glitches on signal.

63. *Glitch Minimizing B*
Connect OUTPUT B J703 to scope.

64. Adjust A70R771 for symmetrical glitches on signal.

A/B PULSE PERFORMANCE

65. OUTPUT change Level [ARB A]/[ARB B] into [50 Ohm].
Amplitude Ranges to [1V]
DATA = Data [Format] Allocation, Duration: [fixed]
change: Period: 0.5[us]
PRGM = Program Page [Trigger Event] Assignment
change: CONTINUOUS-Start [HILVL]
STOP > UPDATE > START

66. *Overshoot / Transition Time*
Connect OUTPUT A J702/OUTPUT B J703 via 50 Ohm Feedthrough to scope.

67. Check for Rise/Fall time <= 13 ns.
Check for Overshoot <= 5 %.
Adjust A70C431/C529 for Output A and A70C731/C829 for Output B.

68. Repeat Rise/Fall time and Overshoot measurement when changing on Output Page [normal]/[complement] and the Amplitude Range to [200mV], [500mV], [10V] and [16V].

NOTE:

The "WARNING Data Limitation ARB X" means only that the hardware is unable to output levels outside certain limits.
The 8175A itself is not faulty!

ARB BOARD CALIBRATION VERICAL SOFTWARE [EEPROM] [WRITE]

69. With Power OFF remove the ARB BD. from the Service Connector and plug it into its normal position.
Reconnect the four 50 Ohm cables! W14 (yellow) Trigger B to J707, W8 (red) Trigger A to J706, W10 (blue) OUTPUT A to J702, and W11 (white) OUTPUT B to J703.

    Turn Power ON.

    Allow a 30 minutes warm-up period before starting the calibration program.

70. With the 8175A and the DVM connected via HP-IB to a Controller, start the Arbitrary Calibration Program (part of VERICAL Program).

71. After the calibration has been done, set the Jumper on the circuit side of the board A70 to its position: "PRT".

A70 BD AY ARBITRARY 08175-66570

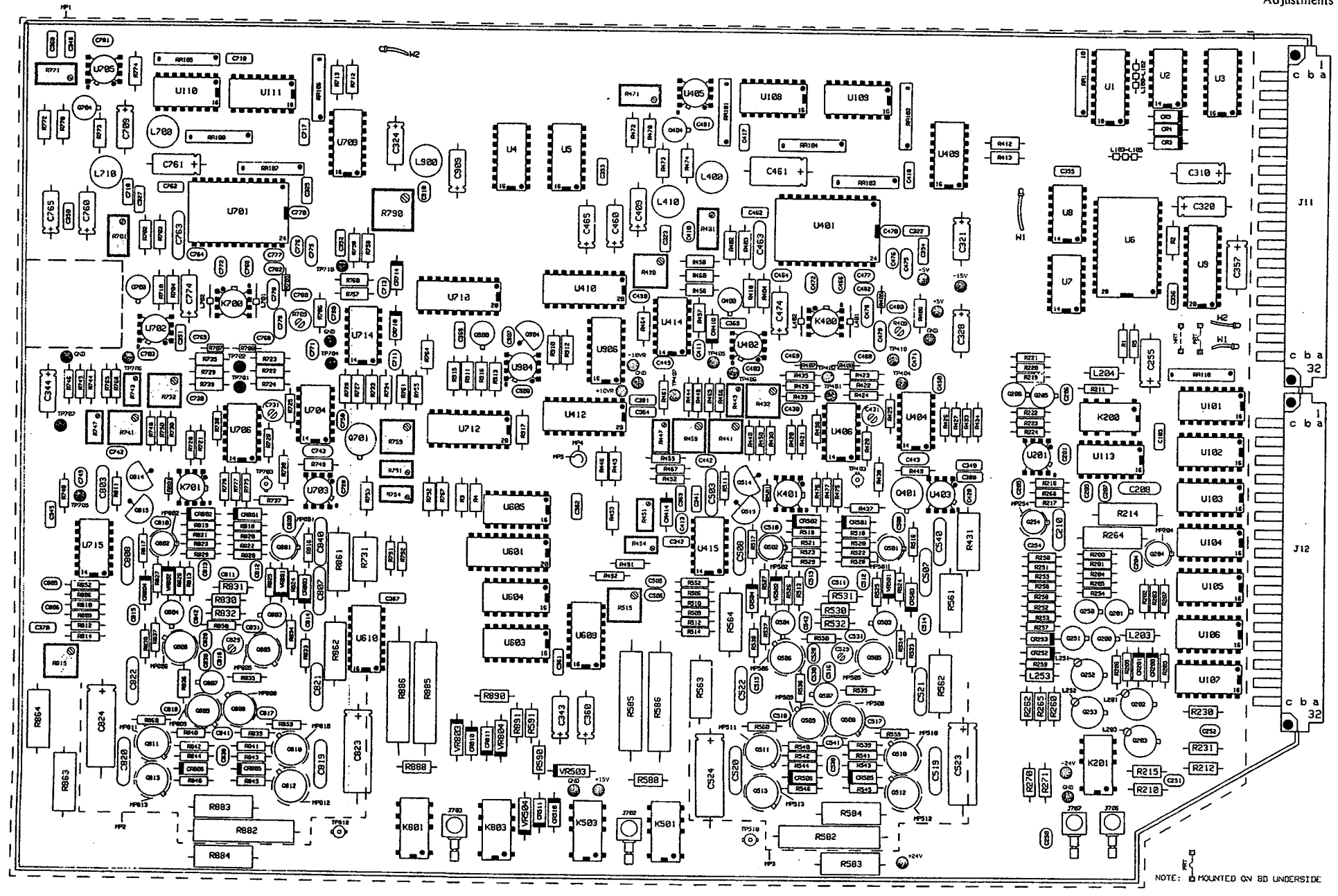


Figure 5-2. Adjustments Points Locator Diagram

STC

SN. 2642G00908

12-3-91

Amplitude at fullscale out of adjustment spec.

Range:	Channel:	Amplitude	Relerror	Adj.spec.
0.2V into 50 Ohm	A	.219V	9.366%	5.53%
1.0V into 50 Ohm	B	1.062V	6.151%	5.53%
10.0V into 50 Ohm	B	10.608V	6.075%	5.53%
0.5V into 50kOhm	B	.525V	5.054%	4.48%
2.0V into 50kOhm	B	2.130V	6.496%	5.53%
20.0V into 50kOhm	B	21.248V	6.242%	5.53%

Amplitude at fullscale after EEPROM calibration.

Range:	Channel:	Amplitude	Relerror	Adj.spec.
0.2V into 50 Ohm	A	.200V	-.033%	0.00%
0.5V into 50 Ohm	A	.501V	.127%	0.00%
1.0V into 50 Ohm	A	.999V	-.081%	0.00%
2.0V into 50 Ohm	A	1.998V	-.111%	0.00%
5.0V into 50 Ohm	A	5.004V	.088%	0.00%
10.0V into 50 Ohm	A	9.992V	-.084%	0.00%
16.0V into 50 Ohm	A	16.005V	.031%	0.00%
0.5V into 50kOhm	A	.500V	.094%	0.00%
1.0V into 50kOhm	A	1.000V	-.012%	0.00%
2.0V into 50kOhm	A	2.003V	.168%	0.00%
5.0V into 50kOhm	A	4.995V	-.096%	0.00%
10.0V into 50kOhm	A	10.016V	.157%	0.00%
20.0V into 50kOhm	A	19.990V	-.050%	0.00%
32.0V into 50kOhm	A	31.947V	-.165%	0.00%
0.2V into 50 Ohm	B	.200V	-.073%	0.00%
0.5V into 50 Ohm	B	.501V	.163%	0.00%
1.0V into 50 Ohm	B	.999V	-.132%	0.00%
2.0V into 50 Ohm	B	1.997V	-.160%	0.00%
5.0V into 50 Ohm	B	5.005V	.098%	0.00%
10.0V into 50 Ohm	B	9.983V	-.167%	0.00%
16.0V into 50 Ohm	B	15.983V	-.103%	0.00%
0.5V into 50kOhm	B	.500V	-.038%	0.00%
1.0V into 50kOhm	B	1.001V	.079%	0.00%
2.0V into 50kOhm	B	2.004V	.179%	0.00%
5.0V into 50kOhm	B	5.008V	.164%	0.00%
10.0V into 50kOhm	B	9.982V	-.179%	0.00%
20.0V into 50kOhm	B	19.987V	-.064%	0.00%
32.0V into 50kOhm	B	31.960V	-.126%	0.00%

Offset at 0V amplitude after EEPROM calibration.

Range:	Channel:	Normal	Complement	Adj.spec.
0.2V into 50 Ohm	A	-.22mV	-.03mV	0.00mV
0.5V into 50 Ohm	A	-.22mV	.12mV	0.00mV
1.0V into 50 Ohm	A	.15mV	-0.00mV	0.00mV
2.0V into 50 Ohm	A	-2.44mV	-.62mV	0.00mV
5.0V into 50 Ohm	A	-2.48mV	.87mV	0.00mV
10.0V into 50 Ohm	A	1.23mV	-.34mV	0.00mV
16.0V into 50 Ohm	A	1.05mV	.05mV	0.00mV
0.5V into 50kOhm	A	-.43mV	-.18mV	0.00mV
1.0V into 50kOhm	A	-.43mV	.25mV	0.00mV
2.0V into 50kOhm	A	.32mV	.01mV	0.00mV
5.0V into 50kOhm	A	-4.82mV	-2.43mV	0.00mV
10.0V into 50kOhm	A	-4.99mV	1.73mV	0.00mV
20.0V into 50kOhm	A	2.06mV	-.95mV	0.00mV
32.0V into 50kOhm	A	1.12mV	2.59mV	0.00mV

0.2V into 50 Ohm	B	-.10mV	-.21mV	0.00mV
0.5V into 50 Ohm	B	-.24mV	.02mV	0.00mV
1.0V into 50 Ohm	B	-.57mV	-.30mV	0.00mV
2.0V into 50 Ohm	B	-1.38mV	-2.50mV	0.00mV
5.0V into 50 Ohm	B	-.20mV	-.07mV	0.00mV
10.0V into 50 Ohm	B	-6.06mV	-2.39mV	0.00mV
16.0V into 50 Ohm	B	-2.51mV	7.92mV	0.00mV
0.5V into 50kOhm	B	-.18mV	.50mV	0.00mV
1.0V into 50kOhm	B	-.48mV	.05mV	0.00mV
2.0V into 50kOhm	B	-1.14mV	-.41mV	0.00mV
5.0V into 50kOhm	B	-2.39mV	4.43mV	0.00mV
10.0V into 50kOhm	B	-.60mV	-.26mV	0.00mV
20.0V into 50kOhm	B	-12.47mV	-4.76mV	0.00mV
32.0V into 50kOhm	B	-2.01mV	-3.31mV	0.00mV

OPTION 002 (A70 Arb. Board)

REFERENCE DESIGNATOR	CD	H-P PART NUMBER	DESCRIPTION
A 70	9	08175-66570	BD AY-ARBITRARY
A 70		08175-66570	BD AY-ARBITRARY
A 70 C 103	8	0160-6080	C-F .068UF 50VD
A 70 C 201	3	0160-5730	C-F 100PF 5%
A 70 C 204	1	0160-5746	C-F 0.1UF 20%
A 70 C 205	1	0160-5746	C-F 0.1UF 20%
A 70 C 206	1	0160-5746	C-F 0.1UF 20%
A 70 C 207	1	0160-5746	C-F 0.1UF 20%
A 70 C 208	1	0160-3097	C-F .47UF CE
A 70 C 209	1	0160-5746	C-F 0.1UF 20%
A 70 C 210	1	0160-3097	C-F .47UF CE
A 70 C 250	1	0160-5746	C-F 0.1UF 20%
A 70 C 251	1	0160-5746	C-F 0.1UF 20%
A 70 C 252	1	0160-5746	C-F 0.1UF 20%
A 70 C 254	1	0160-5746	C-F 0.1UF 20%
A 70 C 255	6	0180-0228	C-F 22UF 15V
A 70 C 310	6	0180-0228	C-F 22UF 15V
A 70 C 320	6	0180-0228	C-F 22UF 15V
A 70 C 321	6	0180-0228	C-F 22UF 15V
A 70 C 322	8	0160-6080	C-F .068UF 50VD
A 70 C 323	8	0160-6080	C-F .068UF 50VD
A 70 C 324	6	0180-0228	C-F 22UF 15V
A 70 C 325	8	0160-6080	C-F .068UF 50VD
A 70 C 327	8	0160-6080	C-F .068UF 50VD
A 70 C 328	5	0180-1746	C-F 15UF 20V TA
A 70 C 340	8	0160-6080	C-F .068UF 50VD
A 70 C 341	8	0160-6080	C-F .068UF 50VD
A 70 C 342	8	0160-6080	C-F .068UF 50VD
A 70 C 343	5	0180-1746	C-F 15UF 20V TA
A 70 C 344	5	0180-1746	C-F 15UF 20V TA
A 70 C 345	8	0160-6080	C-F .068UF 50VD
A 70 C 346	8	0160-6080	C-F .068UF 50VD
A 70 C 350	8	0160-6080	C-F .068UF 50VD
A 70 C 351	8	0160-6080	C-F .068UF 50VD
A 70 C 352	8	0160-6080	C-F .068UF 50VD
A 70 C 353	8	0160-6080	C-F .068UF 50VD
A 70 C 354	8	0160-6080	C-F .068UF 50VD
A 70 C 355	8	0160-6080	C-F .068UF 50VD
A 70 C 356	8	0160-6080	C-F .068UF 50VD
A 70 C 357	6	0180-0228	C-F 22UF 15V
A 70 C 360	5	0180-1746	C-F 15UF 20V TA
A 70 C 361	8	0160-6080	C-F .068UF 50VD
A 70 C 362	8	0160-6080	C-F .068UF 50VD
A 70 C 363	8	0160-6080	C-F .068UF 50VD
A 70 C 364	8	0160-6080	C-F .068UF 50VD
A 70 C 365	8	0160-6080	C-F .068UF 50VD
A 70 C 366	8	0160-6080	C-F .068UF 50VD
A 70 C 367	8	0160-6080	C-F .068UF 50VD
A 70 C 368	8	0160-6080	C-F .068UF 50VD
A 70 C 370	8	0160-6080	C-F .068UF 50VD
A 70 C 380	8	0160-6080	C-F .068UF 50VD
A 70 C 381	8	0160-6080	C-F .068UF 50VD
A 70 C 403	5	0160-5732	C-F 150PF 5%
A 70 C 409	6	0180-0228	C-F 22UF 15V
A 70 C 410	1	0160-5746	C-F 0.1UF 20%
A 70 C 411	3	0160-4386	C-F 33PF 5% 200
A 70 C 413	3	0160-4386	C-F 33PF 5% 200
A 70 C 417	8	0160-6080	C-F .068UF 50VD
A 70 C 418	8	0160-6080	C-F .068UF 50VD
A 70 C 428	9	0160-5736	C-F 22PF 5% 100
A 70 C 430	9	0160-5736	C-F 22PF 5% 100
A 70 C 431	1	0121-0467	C-VAR 2.5-9PF
A 70 C 442	1	0160-3873	C-F 4.7PF 200V
A 70 C 443	1	0160-3097	C-F .47UF CE
A 70 C 449	6	0160-4389	C-F 100PF 5%
A 70 C 450	1	0160-5746	C-F 0.1UF 20%
A 70 C 460	6	0180-0223	C-F 22UF 15V
A 70 C 461	6	0180-2208	C-F 220UF10% 10
A 70 C 462	8	0160-6080	C-F .068UF 50VD
A 70 C 463	1	0160-4300	C-F .047UF 100V
A 70 C 464	9	0160-5728	C-F 1000PF 5%
A 70 C 465	6	0180-0228	C-F 22UF 15V
A 70 C 466	7	0160-5726	C-F 0.01UF 20%
A 70 C 468	7	0160-5726	C-F 0.01UF 20%
A 70 C 469	7	0160-5726	C-F 0.01UF 20%
A 70 C 470	1	0160-5746	C-F 0.1UF 20%
A 70 C 471	9	0160-5728	C-F 1000PF 5%
A 70 C 472	9	0160-5728	C-F 1000PF 5%
A 70 C 474	6	0180-0228	C-F 22UF 15V
A 70 C 475	9	0160-4465	C-F .01UF 20%
A 70 C 476	6	0160-3456	C-F 1000PF 1000
A 70 C 477	7	0160-5750	C-F 2200PF 20%
A 70 C 478	9	0160-4465	C-F .01UF 20%
A 70 C 479	9	0160-3508	C-F 1 UF 50V
A 70 C 480	1	0160-5746	C-F 0.1UF 20%
A 70 C 481	5	0160-5732	C-F 150PF 5%
A 70 C 482	1	0160-5746	C-F 0.1UF 20%
A 70 C 490	9	0160-5728	C-F 1000PF 5%
A 70 C 503	1	0160-3097	C-F .47UF CE
A 70 C 505	7	0160-5726	C-F 0.01UF 20%
A 70 C 506	7	0160-5750	C-F 2200PF 20%
A 70 C 507	1	0160-3097	C-F .47UF CE
A 70 C 508	1	0160-3097	C-F .47UF CE
A 70 C 509	4	0160-5749	C-F 4700PF 20%
A 70 C 510	4	0160-5749	C-F 4700PF 20%
A 70 C 511	7	0160-5726	C-F 0.01UF 20%
A 70 C 512	1	0160-5746	C-F 0.1UF 20%
A 70 C 513	1	0160-5746	C-F 0.1UF 20%
A 70 C 514	1	0160-5746	C-F 0.1UF 20%
A 70 C 515	1	0160-5746	C-F 0.1UF 20%
A 70 C 516	1	0160-5746	C-F 0.1UF 20%
A 70 C 517	1	0160-5746	C-F 0.1UF 20%
A 70 C 518	1	0160-5746	C-F 0.1UF 20%
A 70 C 519	1	0160-3097	C-F .47UF CE
A 70 C 520	1	0160-3097	C-F .47UF CE
A 70 C 521	1	0160-3097	C-F .47UF CE
A 70 C 522	1	0160-3097	C-F .47UF CE
A 70 C 523	5	0180-2778	C-F 220UF 35V
A 70 C 524	5	0180-2778	C-F 220UF 35V
A 70 C 528	7	0160-4380	C-F 1PF 200V
A 70 C 529	1	0121-0524	C-V 1.5-4PF
A 70 C 531	0	0160-3872	C-F 2.2 PF 200V
A 70 C 538	8	0160-4381	C-F 1.5PF 200V
A 70 C 540	9	0160-3508	C-F 1 UF 50V
A 70 C 541	7	0160-5726	C-F 0.01UF 20%
A 70 C 542	9	0160-5736	C-F 22PF 5% 100
A 70 C 703	5	0160-5732	C-F 150PF 5%
A 70 C 709	6	0180-0228	C-F 22UF 15V

REFERENCE DESIGNATOR	CD	H-P PART NUMBER	DESCRIPTION
A 70 C 710	1	0160-5746	C-F 0.1UF 20%
A 70 C 711	3	0160-4386	C-F 33PF 5% 200
A 70 C 713	3	0160-4386	C-F 33PF 5% 200
A 70 C 717	8	0160-6080	C-F .068UF 50VD
A 70 C 718	8	0160-6080	C-F .068UF 50VD
A 70 C 728	9	0160-5736	C-F 22PF 5% 100
A 70 C 730	9	0160-5736	C-F 22PF 5% 100
A 70 C 731	1	0121-0467	C-VAR 2.5-9PF
A 70 C 742	0	0160-4383	C-F 6.8PF 200V
A 70 C 743	1	0160-3097	C-F .47UF CE
A 70 C 749	6	0160-4389	C-F 100PF 5%
A 70 C 750	1	0160-5746	C-F 0.1UF 20%
A 70 C 760	6	0180-0228	C-F 22UF 15V
A 70 C 761	6	0180-2208	C-F 220UF10% 10
A 70 C 762	8	0160-6080	C-F .068UF 50VD
A 70 C 763	1	0160-4300	C-F .047UF 100V
A 70 C 764	9	0160-5728	C-F 1000PF 5%
A 70 C 765	6	0180-0228	C-F 22UF 15V
A 70 C 766	7	0160-5726	C-F 0.01UF 20%
A 70 C 768	7	0160-5726	C-F 0.01UF 20%
A 70 C 769	7	0160-5726	C-F 0.01UF 20%
A 70 C 770	1	0160-5746	C-F 0.1UF 20%
A 70 C 771	9	0160-5728	C-F 1000PF 5%
A 70 C 772	9	0160-5728	C-F 1000PF 5%
A 70 C 774	6	0180-0228	C-F 22UF 15V
A 70 C 775	9	0160-4465	C-F .01UF 20%
A 70 C 776	6	0160-3456	C-F 1000PF 1000
A 70 C 777	7	0160-5750	C-F 2200PF 20%
A 70 C 778	9	0160-4465	C-F .01UF 20%
A 70 C 779	9	0160-3508	C-F 1 UF 50V
A 70 C 780	1	0160-5746	C-F 0.1UF 20%
A 70 C 781	5	0160-5732	C-F 150PF 5%
A 70 C 782	1	0160-5746	C-F 0.1UF 20%
A 70 C 790	9	0160-5728	C-F 1000PF 5%
A 70 C 803	1	0160-3097	C-F .47UF CE
A 70 C 805	7	0160-5726	C-F 0.01UF 20%
A 70 C 806	7	0160-5750	C-F 2200PF 20%
A 70 C 807	1	0160-3097	C-F .47UF CE
A 70 C 808	1	0160-3097	C-F .47UF CE
A 70 C 809	4	0160-5749	C-F 4700PF 20%
A 70 C 810	4	0160-5749	C-F 4700PF 20%
A 70 C 811	7	0160-5726	C-F 0.01UF 20%
A 70 C 812	1	0160-5746	C-F 0.1UF 20%
A 70 C 813	1	0160-5746	C-F 0.1UF 20%
A 70 C 814	1	0160-5746	C-F 0.1UF 20%
A 70 C 815	1	0160-5746	C-F 0.1UF 20%
A 70 C 816	1	0160-5746	C-F 0.1UF 20%
A 70 C 817	1	0160-5746	C-F 0.1UF 20%
A 70 C 818	1	0160-5746	C-F 0.1UF 20%
A 70 C 819	1	0160-3097	C-F .47UF CE
A 70 C 820	1	0160-3097	C-F .47UF CE
A 70 C 821	1	0160-3097	C-F .47UF CE
A 70 C 822	1	0160-3097	C-F .47UF CE
A 70 C 823	5	0180-2778	C-F 220UF 35V
A 70 C 824	5	0180-2778	C-F 220UF 35V
A 70 C 828	7	0160-4380	C-F 1PF 200V
A 70 C 829	1	0121-0524	C-V 1.5-4PF
A 70 C 831	0	0160-3872	C-F 2.2 PF 200V
A 70 C 838	8	0160-4381	C-F 1.5PF 200V
A 70 C 840	9	0160-3508	C-F 1 UF 50V
A 70 C 841	7	0160-5726	C-F 0.01UF 20%

REFERENCE DESIGNATOR	CD	P PART NUMBER	DESCRIPTION
A 70 C 842	9	0160-5736	C-F 22PF 5% 100
A 70 C 907	1	0160-5746	C-F 0 1UF 20%
A 70 C 908	1	0160-5746	C-F 0 1UF 20%
A 70 C 909	6	0180-0228	C-F 22UF 15V
A 70 C 910	8	0160-6080	C-F 068UF 50VD
A 70 CR3	9	1901-0535	DIO SCHOT HP231
A 70 CR4	9	1901-0535	DIO SCHOT HP231
A 70 CR5	9	1901-0535	DIO SCHOT HP231
A 70 CR200	5	1901-1068	DIO SCHOTTKY
A 70 CR201	5	1901-1068	DIO SCHOTTKY
A 70 CR252	5	1901-1068	DIO SCHOTTKY
A 70 CR253	5	1901-1068	DIO SCHOTTKY
A 70 CR410	9	1901-0535	DIO SCHOT HP231
A 70 CR414	9	1901-0535	DIO SCHOT HP231
A 70 CR501	7	1901-0179	DIO SI 15V .75N
A 70 CR502	7	1901-0179	DIO SI 15V .75N
A 70 CR503	7	1901-0179	DIO SI 15V .75N
A 70 CR504	7	1901-0179	DIO SI 15V .75N
A 70 CR505	3	1901-0050	DIO SW 80V 200M
A 70 CR506	3	1901-0050	DIO SW 80V 200M
A 70 CR510	1	1901-1098	DIO-1N4150 50V
A 70 CR511	1	1901-1098	DIO-1N4150 50V
A 70 CR710	9	1901-0535	DIO SCHOT HP231
A 70 CR714	9	1901-0535	DIO SCHOT HP231
A 70 CR801	7	1901-0179	DIO SI 15V .75N
A 70 CR802	7	1901-0179	DIO SI 15V .75N
A 70 CR803	7	1901-0179	DIO SI 15V .75N
A 70 CR804	7	1901-0179	DIO SI 15V .75N
A 70 CR805	3	1901-0050	DIO SW 80V 200M
A 70 CR806	3	1901-0050	DIO SW 80V 200M
A 70 CR810	1	1901-1098	DIO-1N4150 50V
A 70 CR811	1	1901-1098	DIO-1N4150 50V
A 70 J 11	2	1251-7799	3X32 PLUG
A 70 J 12	2	1251-7799	3X32 PLUG
A 70 J 702	8	1250-0543	CONN RF M SM-SN
A 70 J 703	8	1250-0543	CONN RF M SM-SN
A 70 J 706	8	1250-0543	CONN RF M SM-SN
A 70 J 707	8	1250-0543	CONN RF M SM-SN
A 70 K 200	0	0490-1546	RELAY 5 VDC 2A
A 70 K 201	0	0490-1546	RELAY 5 VDC 2A
A 70 K 400	9	0490-0670	RELAY 2C 5V
A 70 K 401	9	0490-0670	RELAY 2C 5V
A 70 K 501	0	0490-1546	RELAY 5 VDC 2A
A 70 K 503	0	0490-1546	RELAY 5 VDC 2A
A 70 K 700	9	0490-0670	RELAY 2C 5V
A 70 K 701	9	0490-0670	RELAY 2C 5V
A 70 K 801	0	0490-1546	RELAY 5 VDC 2A
A 70 K 803	0	0490-1546	RELAY 5 VDC 2A
A 70 L 100	0	9170-0894	CORE MAGNETIC
A 70 L 101	0	9170-0894	CORE MAGNETIC
A 70 L 102	0	9170-0894	CORE MAGNETIC
A 70 L 103	0	9170-0894	CORE MAGNETIC
A 70 L 104	0	9170-0894	CORE MAGNETIC
A 70 L 105	0	9170-0894	CORE MAGNETIC
A 70 L 201	3	9170-0029	FERRITE BEAD
A 70 L 202	3	9170-0029	FERRITE BEAD
A 70 L 203	5	5081-1973	INDUCTANCE 3BEA
A 70 L 204	4	9140-0114	COIL-CHOKE 10 U
A 70 L 251	3	9170-0029	FERRITE BEAD
A 70 L 252	3	9170-0029	FERRITE BEAD

REFERENCE DESIGNATOR	CD	H-P PART NUMBER	DESCRIPTION
A 70 L 253	5	5081-1973	INDUCTANCE 3BEA
A 70 L 400	7	9100-3149	COIL 220UH 10%
A 70 L 401	3	9170-0029	FERRITE BEAD
A 70 L 402	3	9170-0029	FERRITE BEAD
A 70 L 410	7	9100-3149	COIL 220UH 10%
A 70 L 700	7	9100-3149	COIL 220UH 10%
A 70 L 701	3	9170-0029	FERRITE BEAD
A 70 L 702	3	9170-0029	FERRITE BEAD
A 70 L 710	7	9100-3149	COIL 220UH 10%
A 70 L 900	7	9100-3149	COIL 220UH 10%
A 70 MP1	6	08175-04501	ARB-CASE
A 70 MP2	9	08175-01104	HEAT SINK PA CH
A 70 MP3	9	08175-01104	HEAT SINK PA CH
A 70 MP4	8	08175-21705	BUSHING LONG
A 70 MP5	4	08175-26107	PC PIN
A 70 MP204	0	1205-0037	HT-SINK XSTR
A 70 MP254	0	1205-0037	HT-SINK XSTR
A 70 MP501	0	1205-0037	HT-SINK XSTR
A 70 MP502	0	1205-0037	HT-SINK XSTR
A 70 MP505	3	1205-0329	HT-SINK SGL
A 70 MP506	3	1205-0329	HT-SINK SGL
A 70 MP508	3	1205-0329	HT-SINK SGL
A 70 MP509	3	1205-0329	HT-SINK SGL
A 70 MP510	3	1205-0329	HT-SINK SGL
A 70 MP511	3	1205-0329	HT-SINK SGL
A 70 MP512	3	1205-0329	HT-SINK SGL
A 70 MP513	3	1205-0329	HT-SINK SGL
A 70 MP710	7	1251-1556	SKT SGL-CONT
A 70 MP711	7	1251-1556	SKT SGL-CONT
A 70 MP712	7	1251-1556	SKT SGL-CONT
A 70 MP713	7	1251-1556	SKT SGL-CONT
A 70 MP801	0	1205-0037	HT-SINK XSTR
A 70 MP802	0	1205-0037	HT-SINK XSTR
A 70 MP805	3	1205-0329	HT-SINK SGL
A 70 MP806	3	1205-0329	HT-SINK SGL
A 70 MP808	3	1205-0329	HT-SINK SGL
A 70 MP809	3	1205-0329	HT-SINK SGL
A 70 MP810	3	1205-0329	HT-SINK SGL
A 70 MP811	3	1205-0329	HT-SINK SGL
A 70 MP812	3	1205-0329	HT-SINK SGL
A 70 MP813	3	1205-0329	HT-SINK SGL
A 70 Q 200	2	1853-0218	XSTR SI PNP
A 70 Q 201	2	1853-0218	XSTR SI PNP
A 70 Q 202	7	1854-0344	XSTR 1.26H2 200
A 70 Q 203	7	1854-0344	XSTR 1.26H2 200
A 70 Q 204	7	1854-0477	XSTR NPN 2N2222
A 70 Q 205	7	1854-0477	XSTR NPN 2N2222
A 70 Q 206	9	1853-0281	XSTR SI 2907A
A 70 Q 250	2	1853-0218	XSTR SI PNP
A 70 Q 251	2	1853-0218	XSTR SI PNP
A 70 Q 252	7	1854-0344	XSTR 1.26H2 200
A 70 Q 253	7	1854-0344	XSTR 1.26H2 200
A 70 Q 254	7	1854-0477	XSTR NPN 2N2222
A 70 Q 400	7	1854-0477	XSTR NPN 2N2222
A 70 Q 401	1	1854-0637	XSTR SI 2N2219A
A 70 Q 404	7	1854-0477	XSTR NPN 2N2222
A 70 Q 501	9	1854-0809	XSTR .2N 2369A
A 70 Q 502	9	1853-0405	XSTR SI 2N4209
A 70 Q 503	9	1854-0354	XSTR SI NPN
A 70 Q 504	2	1853-0218	XSTR SI PNP
A 70 Q 505	9	1853-0314	XSTR 2N2905A PN
A 70 Q 506	1	1854-0637	XSTR SI 2N2219A
A 70 Q 507	7	1854-0477	XSTR NPN 2N2222
A 70 Q 508	1	1854-0637	XSTR SI 2N2219A
A 70 Q 509	9	1853-0314	XSTR 2N2905A PN
A 70 Q 510	1	1854-0637	XSTR SI 2N2219A
A 70 Q 511	9	1853-0314	XSTR 2N2905A PN
A 70 Q 512	1	1854-0637	XSTR SI 2N2219A
A 70 Q 513	9	1853-0314	XSTR 2N2905A PN
A 70 Q 514	1	1854-0215	XSTR SI 2N3904
A 70 Q 515	2	1853-0036	XSTR SI 2N3906
A 70 Q 700	7	1854-0477	XSTR NPN 2N2222
A 70 Q 701	1	1854-0637	XSTR SI 2N2219A
A 70 Q 704	7	1854-0477	XSTR NPN 2N2222
A 70 Q 801	9	1854-0809	XSTR .2N 2369A
A 70 Q 802	9	1853-0405	XSTR SI 2N4209
A 70 Q 803	9	1854-0354	XSTR SI NPN
A 70 Q 804	2	1853-0218	XSTR SI PNP
A 70 Q 805	9	1853-0314	XSTR 2N2905A PN
A 70 Q 806	1	1854-0637	XSTR SI 2N2219A
A 70 Q 807	7	1854-0477	XSTR NPN 2N2222
A 70 Q 808	1	1854-0637	XSTR SI 2N2219A
A 70 Q 809	9	1853-0314	XSTR 2N2905A PN
A 70 Q 810	1	1854-0637	XSTR SI 2N2219A
A 70 Q 811	9	1853-0314	XSTR 2N2905A PN
A 70 Q 812	1	1854-0637	XSTR SI 2N2219A
A 70 Q 813	9	1853-0314	XSTR 2N2905A PN
A 70 Q 814	1	1854-0215	XSTR SI 2N3904
A 70 Q 815	2	1853-0036	XSTR SI 2N3906
A 70 Q 900	7	1854-0477	XSTR NPN 2N2222
A 70 Q 904	2	1853-0036	XSTR SI 2N3906
A 70 R 1	9	0757-0442	R-F 10K1% .125W
A 70 R 2	9	0757-0442	R-F 10K1% .125W
A 70 R 3	3	0757-0438	R-F 5.11K1%
A 70 R 4	3	0757-0438	R-F 5.11K1%
A 70 R 5	0	0757-0279	R-F 3.16K1%
A 70 R 200	8	0698-3178	R-F 487 1% .125
A 70 R 201	2	0757-0346	R-F 10 1% .125W
A 70 R 202	2	0698-3437	R-F 133 1% .125
A 70 R 203	3	0698-3446	R-F 383 1% .125
A 70 R 204	9	0698-4416	R-F 169 1% .125
A 70 R 205	4	0698-3447	R-F 422 1% 1/8W
A 70 R 206	1	0698-3262	R-F 40.2 1%
A 70 R 207	1	0698-3262	R-F 40.2 1%
A 70 R 208	2	0757-0346	R-F 10 1% .125W
A 70 R 209	2	0757-0346	R-F 10 1% .125W
A 70 R 210	5	0699-2000	R-F 154 1%
A 70 R 211	7	0698-8812	R-F 1 1% .125W
A 70 R 212	9	0699-1999	R-F 140 1%
A 70 R 214	5	0698-5965	R-F 50 1% .5W M
A 70 R 215	5	0699-2000	R-F 154 1%
A 70 R 216	6	0757-0407	R-F 200 1% .125
A 70 R 217	5	0698-4123	R-F 499 1% .125
A 70 R 219	9	0757-0442	R-F 10K1% .125W
A 70 R 220	0	0698-3279	R-F 4.99K1%
A 70 R 221	0	0698-3279	R-F 4.99K1%
A 70 R 222	4	0698-3497	R-F 6.04K1%
A 70 R 223	4	0757-0273	R-F 3.01K1%
A 70 R 224	3	0757-0280	R-F 1K 1% .125W
A 70 R 230	3	0699-2040	R-F 76.8 1%
A 70 R 231	9	0699-1999	R-F 140 1%
A 70 R 250	8	0698-3178	R-F 487 1% .125

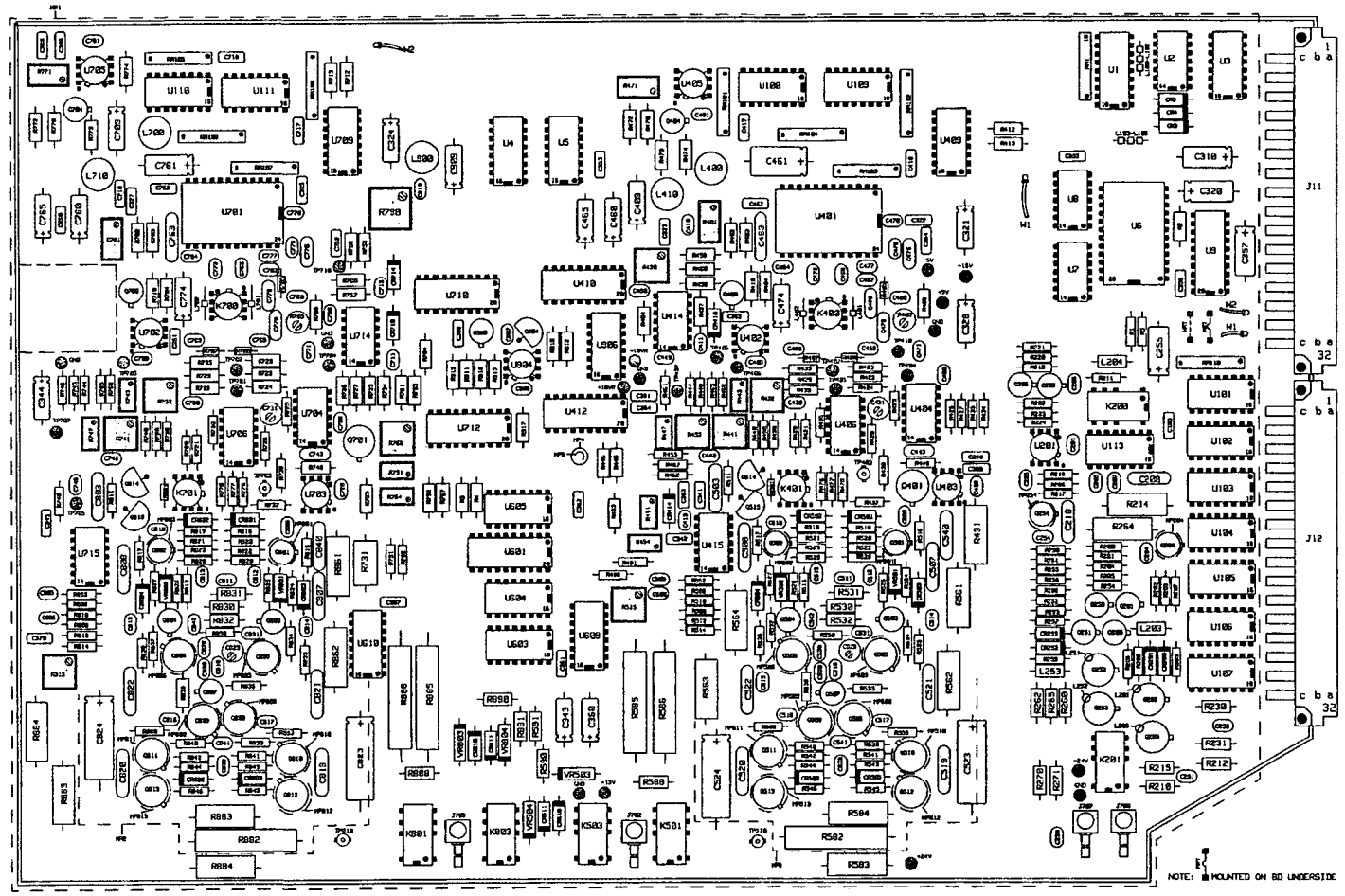
REFERENCE DESIGNATOR	CD	H-P PART NUMBER	DESCRIPTION
A 70 R 251	2	0757-0346	R-F 10 1% .125W
A 70 R 252	2	0698-3437	R-F 133 1% .125
A 70 R 253	3	0698-3446	R-F 383 1% .125
A 70 R 254	9	0698-4416	R-F 169 1% .125
A 70 R 255	4	0698-3447	R-F 422 1% 1/8W
A 70 R 256	1	0698-3262	R-F 40.2 1%
A 70 R 257	1	0698-3262	R-F 40.2 1%
A 70 R 258	2	0757-0346	R-F 10 1% .125W
A 70 R 259	2	0757-0346	R-F 10 1% .125W
A 70 R 260	5	0699-2000	R-F 154 1%
A 70 R 262	9	0699-1999	R-F 140 1%
A 70 R 264	5	0698-5965	R-F 50 1% .5W M
A 70 R 265	5	0699-2000	R-F 154 1%
A 70 R 266	6	0757-0407	R-F 200 1% .125
A 70 R 270	3	0699-2040	R-F 76.8 1%
A 70 R 271	9	0699-1999	R-F 140 1%
A 70 R 401	7	2100-3534	R-VAR 100 10%
A 70 R 402	7	0698-4125	R-F 953 1% .125
A 70 R 403	1	0757-0288	R-F 9.09K 1% .12
A 70 R 404	0	0757-0401	R-F 100 1% .125
A 70 R 405	1	0698-7222	R-F 261 1% .05W
A 70 R 406	0	0757-0401	R-F 100 1% .125
A 70 R 407	3	0698-7208	R-F 68.1 1% .05
A 70 R 408	3	0698-7208	R-F 68.1 1% .05
A 70 R 409	3	2100-2061	R-VAR 200 .5W C
A 70 R 410	6	0757-0283	R-F 2K1% .125W
A 70 R 412	0	0698-4409	R-F 127 1% .125
A 70 R 413	5	0757-0399	R-F 82.5 1% .125
A 70 R 420	2	0757-0346	R-F 10 1% .125W
A 70 R 421	2	0757-0346	R-F 10 1% .125W
A 70 R 422	1	0757-0428	R-F 1.62K 1%
A 70 R 423	1	0757-0428	R-F 1.62K 1%
A 70 R 424	2	0698-4469	R-F 1.15K1%
A 70 R 425	2	0698-4469	R-F 1.15K1%
A 70 R 426	6	0757-0407	R-F 200 1% .125
A 70 R 427	7	0698-4422	R-F 1.27K1%
A 70 R 428	9	0698-3442	R-F 237 1% .125
A 70 R 429	9	0757-0442	R-F 10K1% .125W
A 70 R 430	7	0698-8820	R-F 4.64 1% .12
A 70 R 431	4	0811-3750	R-F 135 1% 3W
A 70 R 432	5	2100-0554	R-V 500 10% .5W
A 70 R 433	5	0698-3498	R-F 8.66K1% .125
A 70 R 434	1	0698-3155	R-F 4.64K 1% .12
A 70 R 435	9	0757-0442	R-F 10K1% .125W
A 70 R 436	2	0757-0346	R-F 10 1% .125W
A 70 R 437	7	0698-4422	R-F 1.27K1%
A 70 R 438	6	0757-0407	R-F 200 1% .125
A 70 R 439	9	0757-0442	R-F 10K1% .125W
A 70 R 440	1	0757-0444	R-F 12.1K1% .125
A 70 R 441	6	2100-3252	R-TRMR 5K 10%
A 70 R 443	8	2100-3296	R-VAR 1K 20%
A 70 R 444	4	0698-8827	R-F 1M 1% .125W
A 70 R 445	9	0757-0442	R-F 10K1% .125W
A 70 R 446	9	0757-0442	R-F 10K1% .125W
A 70 R 447	6	2100-3096	R-VAR 50K 10%
A 70 R 448	4	0698-8827	R-F 1M 1% .125W
A 70 R 449	0	0757-0394	R-F 51.1 1%
A 70 R 450	7	0698-8820	R-F 4.64 1% .12
A 70 R 451	7	2100-3097	R-VAR 100K 10%
A 70 R 452	2	0698-6358	R-F 100K.1%
A 70 R 453	4	0699-0730	R-F 1M .1% .125
A 70 R 454	6	2100-3096	R-VAR 50K 10%
A 70 R 455	8	0699-0479	R-F 2.234K .1%
A 70 R 456	8	0698-6346	R-F 300.1% .125
A 70 R 457	5	0698-6608	R-F 23.5K 1%
A 70 R 458	7	0698-6759	R-F 1.6K1% .125
A 70 R 459	1	2100-0568	R-VAR 100
A 70 R 460	5	0698-8167	R-F 18K .1% .12
A 70 R 461	4	0699-0483	R-F 100K .1% .1
A 70 R 464	3	0757-0389	R-F 33.2 1%
A 70 R 465	8	0698-3558	R-F 4.02K1%
A 70 R 466	3	0757-0438	R-F 5.11K1%
A 70 R 467	3	0757-0389	R-F 33.2 1%
A 70 R 470	3	0757-0438	R-F 5.11K1%
A 70 R 471	9	2100-3502	R-VAR 200 10%
A 70 R 472	3	0698-4444	R-F 4.87K1%
A 70 R 473	3	0757-0280	R-F 1K 1% .125W
A 70 R 474	0	0757-0401	R-F 100 1% .125
A 70 R 475	9	0699-1931	R-F 45 0.1% 1/8
A 70 R 476	3	0699-1935	R-F 72 OHM 0.1%
A 70 R 477	9	0699-1931	R-F 45 0.1% 1/8
A 70 R 490	1	2100-0568	R-VAR 100
A 70 R 491	5	0698-4529	R-F 226K1% 1/8W
A 70 R 492	5	0698-4529	R-F 226K1% 1/8W
A 70 R 501	8	0698-7196	R-F 21.5 2% .05W
A 70 R 506	7	0698-3440	R-F 196 1% .125
A 70 R 509	6	0698-4421	R-F 249 1% .125
A 70 R 510	7	0757-0440	R-F 7.5K 1% .125
A 70 R 511	5	0698-6533	R-F 12.5K .1%
A 70 R 512	5	0698-6533	R-F 12.5K .1%
A 70 R 513	7	0698-8060	R-F 8.64K 1%
A 70 R 514	9	0699-1204	R-F 649.1% .125
A 70 R 515	1	2100-0568	R-VAR 100
A 70 R 516	0	0757-0443	R-F 11K1% .125W
A 70 R 517	0	0757-0443	R-F 11K1% .125W
A 70 R 518	7	0699-1864	R-F 59 OHM .1%
A 70 R 519	7	0699-1864	R-F 59 OHM .1%
A 70 R 520	3	0757-0280	R-F 1K 1% .125W
A 70 R 521	3	0757-0280	R-F 1K 1% .125W
A 70 R 522	3	0757-0280	R-F 1K 1% .125W
A 70 R 523	3	0757-0280	R-F 1K 1% 125W
A 70 R 524	0	0757-0401	R-F 100 1% .125
A 70 R 525	6	0757-0283	R-F 2K1% .125W
A 70 R 526	6	0757-0283	R-F 2K1% .125W
A 70 R 527	0	0757-0401	R-F 100 1% .125
A 70 R 528	6	0699-0211	R-F 859.1% .125
A 70 R 529	6	0699-0211	R-F 859.1% .125
A 70 R 530	3	0757-1022	R-F 1.78K 1%
A 70 R 531	3	0757-1022	R-F 1.78K 1%
A 70 R 532	3	0757-0751	R-F 7.5K 1% .25
A 70 R 533	2	0698-3429	R-F 19.6 1%
A 70 R 534	2	0698-3429	R-F 19.6 1%
A 70 R 535	3	0757-0280	R-F 1K 1% .125W
A 70 R 536	4	0698-3132	R-F 261 1% .125
A 70 R 537	2	0698-3429	R-F 19.6 1%
A 70 R 538	2	0698-3429	R-F 19.6 1%
A 70 R 539	2	0757-0346	R-F 10 1% .125W
A 70 R 540	2	0757-0346	R-F 10 1% .125W
A 70 R 541	6	0699-0211	R-F 859.1% .125
A 70 R 542	6	0699-0211	R-F 859.1% .125
A 70 R 543	2	0757-0346	R-F 10 1% .125W
A 70 R 544	2	0757-0346	R-F 10 1% .125W

REFERENCE DESIGNATOR	CD	H-P PART NUMBER	DESCRIPTION
A 70 R 545	2	0757-0346	R-F 10 1% .125W
A 70 R 546	2	0757-0346	R-F 10 1% .125W
A 70 R 550	7	0698-7260	R-F 10K 1% .05W
A 70 R 552	3	0757-0280	R-F 1K 1% .125W
A 70 R 559	2	0698-3429	R-F 19.6 1%
A 70 R 560	2	0698-3429	R-F 19.6 1%
A 70 R 561	2	0698-3601	R-F 10 5% 2W MO
A 70 R 562	2	0698-3601	R-F 10 5% 2W MO
A 70 R 563	2	0698-3601	R-F 10 5% 2W MO
A 70 R 564	2	0698-3601	R-F 10 5% 2W MO
A 70 R 582	6	0699-0146	R-F 53.6 1% 10W
A 70 R 583	3	0757-0818	R-F 825 1% .5W
A 70 R 584	3	0757-0818	R-F 825 1% .5W
A 70 R 585	2	0699-0530	R-F 61.11 .1% 1
A 70 R 586	2	0699-0530	R-F 61.11 .1% 1
A 70 R 588	5	0698-8258	R-F 247.5 1%
A 70 R 590	3	0757-0280	R-F 1K 1% .125W
A 70 R 591	3	0757-0280	R-F 1K 1% .125W
A 70 R 701	7	2100-3534	R-VAR 100 10%
A 70 R 702	7	0698-4125	R-F 953 1% .125
A 70 R 703	1	0757-0288	R-F 9.09K 1% .12
A 70 R 704	0	0757-0401	R-F 100 1% .125
A 70 R 705	1	0698-7222	R-F 261 1% .05W
A 70 R 706	0	0757-0401	R-F 100 1% .125
A 70 R 707	3	0698-7208	R-F 68.1 1% .05
A 70 R 708	3	0698-7208	R-F 68.1 1% .05
A 70 R 709	3	2100-2061	R-VAR 200 .5W C
A 70 R 710	6	0757-0283	R-F 2K1% .125W
A 70 R 712	0	0698-4409	R-F 127 1% .125
A 70 R 713	5	0757-0399	R-F 82.5 1% .125
A 70 R 720	2	0757-0346	R-F 10 1% .125W
A 70 R 721	2	0757-0346	R-F 10 1% .125W
A 70 R 722	1	0757-0428	R-F 1.62K 1%
A 70 R 723	1	0757-0428	R-F 1.62K 1%
A 70 R 724	2	0698-4469	R-F 1.15K1%
A 70 R 725	2	0698-4469	R-F 1.15K1%
A 70 R 726	6	0757-0407	R-F 200 1% .125
A 70 R 727	7	0698-4422	R-F 1.27K1%
A 70 R 728	9	0698-3442	R-F 237 1% .125
A 70 R 729	9	0757-0442	R-F 10K1% .125W
A 70 R 730	7	0698-8820	R-F 4.64 1% .12
A 70 R 731	4	0811-3750	R-F 135 1% 3W
A 70 R 732	5	2100-0554	R-V 500 10% .5W
A 70 R 733	5	0698-3498	R-F 8.66K1% .125
A 70 R 734	1	0698-3155	R-F 4.64K 1% .12
A 70 R 735	9	0757-0442	R-F 10K1% .125W
A 70 R 736	2	0757-0346	R-F 10 1% .125W
A 70 R 737	7	0698-4422	R-F 1.27K1%
A 70 R 738	6	0757-0407	R-F 200 1% .125
A 70 R 739	9	0757-0442	R-F 10K1% .125W
A 70 R 740	1	0757-0444	R-F 12.1K1% .125
A 70 R 741	6	2100-3252	R-TRMR 5K 10%
A 70 R 743	8	2100-3296	R-VAR 1K 20%
A 70 R 744	4	0698-8827	R-F 1M 1% .125W
A 70 R 745	9	0757-0442	R-F 10K1% .125W
A 70 R 746	9	0757-0442	R-F 10K1% .125W
A 70 R 747	6	2100-3096	R-VAR 50K 10%
A 70 R 748	4	0698-8827	R-F 1M 1% .125W
A 70 R 749	0	0757-0394	R-F 51.1 1%
A 70 R 750	7	0698-8820	R-F 4.64 1% .12
A 70 R 751	7	2100-3097	R-VAR 100K 10%
A 70 R 752	2	0698-6358	R-F 100K 1%
A 70 R 753	4	0699-0730	R-F 1M .1% .125
A 70 R 754	6	2100 3096	R-VAR 50K 10%
A 70 R 755	8	0699-0479	R-F 2.234K .1%
A 70 R 756	8	0698-6346	R-F 300 1% .125
A 70 R 757	5	0698-6608	R-F 23.5K 1%
A 70 R 758	7	0698-6759	R-F 1.6K1% .125
A 70 R 759	1	2100-0568	R-VAR 100
A 70 R 760	5	0698-8137	R-F 18K .1% .12
A 70 R 761	4	0699-0483	R-F 100K .1% .1
A 70 R 764	3	0757-0389	R-F 33.2 1%
A 70 R 765	8	0698-3558	R-F 4.02K1%
A 70 R 766	3	0757-0438	R-F 5.11K1%
A 70 R 767	3	0757-0389	R-F 33.2 1%
A 70 R 770	3	0757-0438	R-F 5.11K1%
A 70 R 771	9	2100-3502	R-VAR 200 10%
A 70 R 772	3	0698-4444	R-F 4.87K1%
A 70 R 773	3	0757-0280	R-F 1K 1% .125W
A 70 R 774	0	0757-0401	R-F 100 1% .125
A 70 R 775	9	0699-1931	R-F 45 0.1% 1/8
A 70 R 776	3	0699-1935	R-F 72 OHM 0.1%
A 70 R 777	9	0699-1931	R-F 45 0.1% 1/8
A 70 R 790	1	2100-0568	R-VAR 100
A 70 R 791	5	0698-4529	R-F 226K1% 1/8W
A 70 R 792	5	0698-4529	R-F 226K1% 1/8W
A 70 R 801	8	0698-7196	R-F 21.5 2% .05W
A 70 R 806	7	0698-3440	R-F 196 1% .125
A 70 R 809	6	0698-4421	R-F 249 1% .125
A 70 R 810	7	0757-0440	R-F 7.5K 1% .125
A 70 R 811	5	0698-6533	R-F 12.5K .1%
A 70 R 812	5	0698-6533	R-F 12.5K .1%
A 70 R 813	7	0698-8060	R-F 8.64K 1%
A 70 R 814	9	0699-1204	R-F 649 1% .125
A 70 R 815	1	2100-0568	R-VAR 100
A 70 R 816	0	0757-0443	R-F 11K1% .125W
A 70 R 817	0	0757-0443	R-F 11K1% .125W
A 70 R 818	7	0699-1864	R-F 59 OHM .1%
A 70 R 819	7	0699-1864	R-F 59 OHM .1%
A 70 R 820	3	0757-0280	R-F 1K 1% .125W
A 70 R 821	3	0757-0280	R-F 1K 1% .125W
A 70 R 822	3	0757-0280	R-F 1K 1% .125W
A 70 R 823	3	0757-0280	R-F 1K 1% .125W
A 70 R 824	0	0757-0401	R-F 100 1% .125
A 70 R 825	6	0757-0283	R-F 2K1% .125W
A 70 R 826	6	0757-0283	R-F 2K1% .125W
A 70 R 827	0	0757-0401	R-F 100 1% .125
A 70 R 828	6	0699-0211	R-F 859.1% .125
A 70 R 829	6	0699-0211	R-F 859.1% .125
A 70 R 830	3	0757-1022	R-F 1.78K 1%
A 70 R 831	3	0757-1022	R-F 1.78K 1%
A 70 R 832	3	0757-0751	R-F 7.5K 1% .25
A 70 R 833	2	0698-3429	R-F 19.6 1%
A 70 R 834	2	0698-3429	R-F 19.6 1%
A 70 R 835	3	0757-0280	R-F 1K 1% .125W
A 70 R 836	4	0698-3132	R-F 261 1% .125
A 70 R 837	2	0698-3429	R-F 19.6 1%
A 70 R 838	2	0698-3429	R-F 19.6 1%
A 70 R 839	2	0757-0346	R-F 10 1% .125W
A 70 R 840	2	0757-0346	R-F 10 1% .125W
A 70 R 841	6	0699-0211	R-F 859.1% .125
A 70 R 842	6	0699-0211	R-F 859.1% .125

REFERENCE DESIGNATOR	CD	H-P PART NUMBER	DESCRIPTION
A 70 R 843	2	0757-0346	R-F 10 1% .125W
A 70 R 844	2	0757-0346	R-F 10 1% .125W
A 70 R 845	2	0757-0346	R-F 10 1% .125W
A 70 R 846	2	0757-0346	R-F 10 1% .125W
A 70 R 850	7	0698-7260	R-F 10K 1% .05W
A 70 R 852	3	0757-0280	R-F 1K 1% .125W
A 70 R 859	2	0698-3429	R-F 19.6 1%
A 70 R 860	2	0698-3429	R-F 19.6 1%
A 70 R 861	2	0698-3601	R-F 10 5% 2W MO
A 70 R 862	2	0698-3601	R-F 10 5% 2W MO
A 70 R 863	2	0698-3601	R-F 10 5% 2W MO
A 70 R 864	2	0698-3601	R-F 10 5% 2W MO
A 70 R 882	6	0699-0146	R-F 53.6 1% 10W
A 70 R 883	3	0757-0818	R-F 825 1% .5W
A 70 R 884	3	0757-0818	R-F 825 1% .5W
A 70 R 885	2	0699-0530	R-F 61.11 .1% 1
A 70 R 886	2	0699-0530	R-F 61.11 .1% 1
A 70 R 888	5	0698-8258	R-F 247.5 1%
A 70 R 890	3	0757-0280	R-F 1K 1% .125W
A 70 R 891	3	0757-0280	R-F 1K 1% .125W
A 70 R 910	6	0698-6360	R-F 10K.1% .125
A 70 R 911	0	0757-0401	R-F 100 1% .125
A 70 R 912	0	0757-0401	R-F 100 1% .125
A 70 R 913	6	0698-6360	R-F 10K.1% .125
A 70 R 915	0	0757-0401	R-F 100 1% .125
A 70 R 916	0	0757-0401	R-F 100 1% .125
A 70 R 917	8	0698-6320	R-F 5K.1% .125W
A 70 RA1	8	1810-0280	R-NETWORK 9X10K
A 70 RA101	1	1810-0712	R-NETWORK 8 PIN
A 70 RA102	1	1810-0712	R-NETWORK 8 PIN
A 70 RA103	1	1810-0712	R-NETWORK 8 PIN
A 70 RA104	1	1810-0712	R-NETWORK 8 PIN
A 70 RA105	1	1810-0712	R-NETWORK 8 PIN
A 70 RA106	1	1810-0712	R-NETWORK 8 PIN
A 70 RA107	1	1810-0712	R-NETWORK 8 PIN
A 70 RA108	1	1810-0712	R-NETWORK 8 PIN
A 70 RA110	5	1810-0229	R-NETWORK 7X330
A 70 TP401	6	0360-2264	TEST POINT
A 70 TP402	6	0360-2264	TEST POINT
A 70 TP403	3	1250-1918	TEST-JACK
A 70 TP404	6	0360-2264	TEST POINT
A 70 TP405	6	0360-2264	TEST POINT
A 70 TP406	6	0360-2264	TEST POINT
A 70 TP407	6	0360-2264	TEST POINT
A 70 TP410	6	0360-2264	TEST POINT
A 70 TP510	3	1250-1918	TEST-JACK
A 70 TP701	6	0360-2264	TEST POINT
A 70 TP702	6	0360-2264	TEST POINT
A 70 TP703	3	1250-1918	TEST-JACK
A 70 TP704	6	0360-2264	TEST POINT
A 70 TP705	6	0360-2264	TEST POINT
A 70 TP706	6	0360-2264	TEST POINT
A 70 TP707	6	0360-2264	TEST POINT
A 70 TP710	6	0360-2264	TEST POINT
A 70 TP810	3	1250-1918	TEST-JACK
A 70 U 1	4	1820-2075	IC SN74LS245N
A 70 U 2	2	1820-1273	IC SN74LS28N
A 70 U 3	2	1820-1281	IC SN74LS139N
A 70 U 4	3	1820-1216	IC SN74LS138N
A 70 U 5	3	1820-1216	IC SN74LS138N
A 70 U 6	8	1818-3387	IC D2817A

REFERENCE DESIGNATOR	CD	H-P PART NUMBER	DESCRIPTION
A 70 U 7	3	1820-1208	IC SN74LS32N
A 70 U 8	9	1820-1197	IC SN74LS00N
A 70 U 9	6	1820-1730	IC SN74LS273N
A 70 U 101	9	1820-2848	IC MC10H116P
A 70 U 102	9	1820-2848	IC MC10H116P
A 70 U 103	4	1820-3461	IC MC 10H115 P
A 70 U 104	4	1820-3461	IC MC 10H115 P
A 70 U 105	4	1820-3461	IC MC 10H115 P
A 70 U 106	4	1820-3461	IC MC 10H115 P
A 70 U 107	4	1820-3461	IC MC 10H115 P
A 70 U 108	3	1820-3577	IC DIG 10H186A
A 70 U 109	3	1820-3577	IC DIG 10H186A
A 70 U 110	3	1820-3577	IC DIG 10H186A
A 70 U 111	3	1820-3577	IC DIG 10H186A
A 70 U 113	0	1820-2849	IC MC10H131P
A 70 U 201	2	1826-0059	1826-1460 REPL.
A 70 U 401	4	1826-1538	IC 10 BIT D/A
A 70 U 402	2	1826-0059	1826-1460 REPL.
A 70 U 403	2	1826-0059	1826-1460 REPL.
A 70 U 404	5	1858-0055	XSTR ARY 14P-DI
A 70 U 405	2	1826-0059	1826-1460 REPL.
A 70 U 406	9	1858-0075	XSTR ARY TO-116
A 70 U 409	1	1820-3400	IC MC 10 H 211
A 70 U 410	7	1826-1284	IC DAC 12 BIT
A 70 U 412	7	1826-1284	IC DAC 12 BIT
A 70 U 414	7	1826-0616	IC LINEAR
A 70 U 415	7	1826-0616	IC LINEAR
A 70 U 601	6	1820-1730	IC SN74LS273N
A 70 U 603	7	1820-1195	IC SN74LS175N
A 70 U 604	7	1820-1195	IC SN74LS175N
A 70 U 605	8	1820-1112	IC SN74LS74AN
A 70 U 609	9	1820-2111	IC SN75468N
A 70 U 610	9	1820-2111	IC SN75468N
A 70 U 701	4	1826-1538	IC 10 BIT D/A
A 70 U 702	2	1826-0059	1826-1460 REPL.
A 70 U 703	2	1826-0059	1826-1460 REPL.
A 70 U 704	5	1858-0055	XSTR ARY 14P-DI
A 70 U 705	2	1826-0059	1826-1460 REPL.
A 70 U 706	9	1858-0075	XSTR ARY TO-116
A 70 U 709	1	1820-3400	IC MC 10 H 211
A 70 U 710	7	1826-1284	IC DAC 12 BIT
A 70 U 712	7	1826-1284	IC DAC 12 BIT
A 70 U 714	7	1826-0616	IC LINEAR
A 70 U 715	7	1826-0616	IC LINEAR
A 70 U 904	7	1826-0111	IC 1458
A 70 U 906	8	1826-0740	ANLG SW
A 70 VR501	0	1902-3182	DIO 12.1V 5% .4
A 70 VR502	0	1902-3182	DIO 12.1V 5% .4
A 70 VR503	8	1902-1340	DIO ZNR 1N5355B
A 70 VR504	8	1902-1340	DIO ZNR 1N5355B
A 70 VR801	0	1902-3182	DIO 12.1V 5% .4
A 70 VR802	0	1902-3182	DIO 12.1V 5% .4
A 70 VR803	8	1902-1340	DIO ZNR 1N5355B
A 70 VR804	8	1902-1340	DIO ZNR 1N5355B
A 70 W 1	5	08175-61617	CBL AY-SHLD 140
A 70 W 2	6	08175-61618	CBL AY-SHLD 430
A 70 WRT	7	1258-0124	PIN PROG JUMPER

A70 BD AY ARBITRARY 08175-66570



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C103	I4	C442	F4	C718	B1	C908	D3	L105	H2	Q253	H6	R210	H/I6	R431	G4/5	R518	G4	R712	C1	R791	C5	R888	D6	U107	I6
C201	H4	C443	G4	C728	C4	C909	D2	L201	H5	Q254	H4	R211	H3	R432	F4	R519	F4	R713	C1	R792	D5	R890	D4	U108	F1
C204	I5	C449	G4	C730	B4	C910	D2	L202	H6	Q400	F3	R212	I6	R433	G4	R520	G5	R720	B4	R891	D4	U109	G1
C205	H4	C450	G4	C731	C4			L203	H/I5	Q401	G4	R214	H/I4	R434	G4	R521	F5	R721	B4	R910	E3	U110	B1
C206	H3	C460	E2	C742	A4			L204	H/I3	Q404	E2	R215	H/I6	R435	F3	R522	G5	R722	B3	R911	D3	U111	B/C1
C207	H4	C461	F2	C743	A4	CR3	I2																		
C208	H/I4	C462	F2	C749	A4	CR4	I2	L251	H5	Q501	G5	R216	H4	R436	F4	R523	F5	R724	G5	R810	A5	R912	E3	U113	H/I4
C209	H4	C463	F2	C750	C4	CR5	I2	L252	H6	Q502	F5	R217	H4	R437	G4	R525	G5	R724	B4	R811	A4	R913	D3	U201	H4
C210	H5/4	C464	F3	C760	A2	CR200	I5	L253	H5	Q503	G5	R219	H3	R438	G4	R526	F5	R725	C4	R812	A5	R915	D3	U401	F/G2
C250	H7	C465	E2	C761	B2	CR201	I5	L400	F2	Q504	F5	R220	H3	R439	F4	R527	F5	R726	C3/4	R813	B5	R916	D3	U402	F3
								L401	G3	Q505	G6	R221	H3	R440	F4			R727	C3/4	R814	A5	R917	D4	U403	G4
C251	I6	C466	G3	C762	B2	CR252	H5							R441	F4	R528	G5								
C252	I6	C468	G3	C763	B2	CR253	H5	L402	F3	Q506	F6	R222	H3	R443	F4	R529	F5	R728	B4	R815	A5	RA1	H1/2	U404	G3/4
C254	H4	C469	F3	C764	B3	CR410	F3	L410	E2	Q507	G6	R223	H4	R444	F4	R530	G5	R729	B3	R816	C5	RA101	F1/2	U405	E/F1
C255	I3	C470	G2	C765	A2	CR414	E4	L700	B3	Q508	G6	R224	H4	R445	E4	R531	G5	R730	B4	R817	B5	RA102	G1/2	U406	G3
C310	I2	C471	G3	C766	B2	CR501	G5	L701	B3	Q509	F6	R230	I6	R446	E4	R532	G5	R731	C5	R818	B5	RA103	G2	U409	G2
								L702	B3	Q510	G6	R231	I6					R732	B4	R819	B5	RA104	F/G2	U410	E3
C320	I2	C472	F3	C768	B3									R447	E4										
C321	G3	C474	F3	C769	B3	CR502	F5							R448	F4							RA105	B1		
C322	G2	C475	G3	C770	C2	CR503	G5	L710	A2	Q511	F6	R250	H5	R449	G4	R533	G5	R733	C3/4	R820	B5	RA106	C1/2	U412	E4
C323	E3	C476	G3	C771	C3	CR504	F5	L900	D2	Q512	G6	R251	H3	R451	E4	R535	G6	R734	C3/4	R821	B5	RA107	B/C2	U414	E3
C324	C2	C477	G3	C772	B3	CR505	G6			Q513	F6	R252	H5	R452	E4	R536	F5/6	R735	B3	R822	B5	RA108	B2	U415	E5
						CR506	F6			Q514	F4	R253	H5			R537	F5	R736	B4	R823	B5	RA110	I3	U601	D4/5
C325	C2	C478	G3	C774	B3			MP1	A1	Q515	F4	R254	H5					R737	B/C4	R824	C5			U603	D5/6
C327	B2	C479	G3	C775	C2/3			MP2	A7					R453	E4										
C328	G3	C480	G3	C776	C2	CR510	E6/7	MP3	F7			R255	H5	R454	E5	R538	F5					TP401	G4		
C340	G4	C481	G3	C777	C3	CR511	E6/7	MP4	E4	Q700	B3	R256	H5	R455	E4	R539	G6	R738	C4	R825	B5	TP402	G3		
C341	F4	C482	G3	C778	B3	CR710	C3	MP5	E4	Q701	C4	R257	H5	R456	F3	R540	F6	R739	B4	R826	B5	TP403	G4	U604	D5
						CR714	C3			Q704	A2	R258	H5	R457	F3	R541	G6	R740	B4	R827	B5	TP404	G4	U605	D4
C342	E5	C490	E3	C779	C3	CR801	B4			Q801	C5	R259	H5			R542	F6	R741	A/B4	R828	B5	TP405	F3	U609	E5
C343	S6	C503	F4	C780	C3			MP204	I5	Q802	B5							R743	B4	R829	B5			U610	C5
C344	A3/4	C505	E5	C781	A1			MP254	H4															U701	B/C2
C345	A4	C506	E5	C782	C3	CR802	B4	MP501	G3			R260	H6	R458	F3					R830	B5	TP406	F4		
C346	A1	C507	G5	C790	C3	CR803	C5	MP502	F5			R262	H6	R459	F4	R543	G6			R831	B5	TP407	E4		
						CR804	G5	MP503	G5	Q803	C5	R264	H/I4	R460	F3	R544	F6	R744	A3/4	R832	B5	TP410	G3	U702	B3
C350	A2	C508	F4/5	C803	A4	CR805	B6			Q804	B5	R265	H6	R461	E3/4	R545	G6	R745	A3/4	R833	C5/6	TP501	F7	U703	C4
C351	B3	C509	G4	C805	A5	CR806	B6			Q806	B5	R266	H4	R464	E3	R546	F6	R746	A3/4	R834	C5	TP701	B4	U704	C4
C352	C2	C510	F5	C806	A5					Q807	B6					R550	G6	R747	A4					U705	A1
C353	E2	C511	G5	C807	C5			MP506	F5	Q808	B6							R748	A4					U706	B4
C354	G3	C512	G5	C808	A5			MP508	G6											R835	B6				
						CR810	D6	MP509	F6			R270	H6	R465	F4					R836	B6	TP702	B3		
C355	H2	C513	F5	C809	C4	CR811	D6	MP510	G6	Q809	B6	R271	H6	R466	F4	R552	F5			R837	B5	TP703	B4		
C356	I3	C514	G5	C810	B4			MP511	F6	Q810	C6	R401	I2/3	R467	E4	R559	G6	R749	C4	R838	B5	TP704	C3	U709	C2
C357	I3	C515	F6	C811	B5	J11	I2			Q811	B6	R402	F3	R470	E2	R560	F6	R751	C/D4	R839	B6	TP705	A4	U710	D3
C360	E6	C517	G6	C812	B5	J12	I5	MP512	G6	Q812	C6	R403	F3	R471	E2	R561	G5	R752	D4			TP706	B3	U712	D4
C361	E5	C518	F6	C813	B5	J702	E7	MP513	F6	Q813	B6					R562	G6	R753	C4					U714	C3
						J703	E7	MP801	C4									R754	C/D4					U715	A5
C362	E4	C519	G6	C814	C5	J706	I7	MP802	B5	Q814	B4	R404	F3	R472	E2					R840	B6				
C363	E4	C520	I6	C815	B5	J707	H7	MP805	B5	Q815	B4	R405	G3	R473	E2	R563	F6	R755	D3/4	R841	B6	TP707	A4		
C364	E4	C521	G6	C816	B5					Q900	D3	R406	G3	R474	E2	R564	F6	R756	C2	R842	B6	TP710	C3		
C365	F3	C522	F6	C817	B6					Q904	D3	R407	I3	R475	G4	R582	F/G7	R757	C3	R843	B6	TP810	C7	U904	D3
C366	D3	C523	G6	C818	B6	K200	H/I4	MP806	B5			R408	G3	R476	F4	R583	G7	R758	C2	R844	B6			U906	E3
						K201	H6	MP808	B6							R584	G6	R759	C/D4						
C367	C5	C524	F6/7	C819	C6	K400	G3	MP809	B6	R1	I3	R409	F3	R477	G4							U1	H/I1		
C368	A1	C528	F5	C820	A6	K401	F4	MP810	C6	R2	I2	R410	F3	R490	E5			R760	C3	R845	B6	U2	I1	VR501	G5
C370	A5	C529	G5	C821	C6	K501	E7	MP811	B6	R3	D4	R412	H2	R491	E5	R585	E6	R761	D3/4	R846	B6	U3	I1	VR502	F5
C380	G4	C530	F5	C822	B6			MP812	C6	R4	D4	R413	H2	R492	E5	R586	E6	R764	D3	R860	B5	U4	D2	VR503	E6
C381	E4	C531	G5	C823	C6			MP813	B6	R5	I3	R420	F4	R501	F4	R588	E7	R765	A3/4	R852	A5	U5	E2	VR504	D6
						K503	E7									R590	E6	R766	A3/4	R859	C6			VR801	C5
C403	F3	C538	G6	C824	A6	K700	B3			R200	H5	R421	F4	R506	F5	R591	D4					U6	H/I2		
C409	E2	C540	G5	C828	B5	K701	B4	Q200	H5	R201	H5	R422	G3	R509	F5	R701	A2	R767	D4	R860	B6	U7	H3	VR802	B5
C410	F3	C541	G6	C829	B5	K801	D7	Q201	I5	R202	I5	R423	G3	R510	F5	R702	B2	R770	A2	R861	C5	U8	H2	VR803	D6
C411	F3	C542	F5	C830	B5	K803	D7	Q202	I6	R203	I5	R424	G4	R511	F4	R703	B2	R771	A1	R862	C5/6	U9	I2/3	VR804	D6
C413	E5	C703	B3	C831	B5			Q203	I6	R204	H5	R425	G4	R512	F5	R704	B3	R772	A2	R863	A6	U101	I4		
								Q204	I5							R705	C3	R773	A2	R864	A6			W1	I3
C417	F2	C709	A2	C838	B6	L100	I1															U102	I4	W2	I3
C418	G2	C710	A2	C840	C5	L101	I1	Q205	H4	R205	H5	R426	G4	R513	F5	R706	C3	R774	A1	R882	B7	U103	I4	WRT	I3
C428	G4	C711	C3	C841	B6	L102	I1	Q206	H4	R206	H5/6	R427	G4	R514	F5	R707	B3	R775	B4	R883	B6	U104	I5		
C430	F4	C713	C3	C842	B5	L103	H2	Q250	H5	R207	I5	R428	F3	R515	E5	R708	B3	R776	B4	R884	B7	U105	I5		
C431	G4	C717	C2	C907	D3	L104	H2	Q251	H5	R208	H5/6	R429	F3	R516	G4	R709	C3	R777	B4	R885	D5/6	U106	I5		
								Q252	H5	R209	I5/6	R430	F4	R517	F4	R710	B3	R790	C2	R886	C5/6				

SERVICE BLOCK 6
ARBITRARY W. G. BOARD

INTRODUCTION

In the following text the abbreviation "Arb." is used to refer to the Dual Arbitrary Waveform Generator. The main function of the Arb. Board (A70) is the generation of two amplitude independent analog signals - the arbitrary waveforms. These are derived from the data (and timing values) set by the user. The values are stored in appropriate memory on the Data Board (A40). On the Arb. Board, two output signals: Output A and Output B, together with the corresponding trigger outputs (TRIG OUTPUT and TRIG OUTPUT B), all determined from user settings, are produced under control of the MPU.

Block Theory

The Arb. Board comprises six functional blocks or sections. These are listed, together with a short explanation, below and can be identified by referring to the block diagram Figure 8-6-1. A table (Table 8-6-6) listing/explaining all the mnemonics used in this service block, is included at the end of theory section. In the detailed theory of operation the blocks are explained in the sequence as listed below.

Device Bus Interface. This interfaces between the MPU produced control signals and the Arb. Board.

Amplitude Range and Offset Control Circuitry. This produces the control voltages required by the Amplitude DAC and Offset Voltage Control Amplifier respectively.

Trigger Circuitry. This produces ECL or TTL (Trig) signals according to user requirements.

OUTPUT A D-A Conversion and Output Amplifier. This buffers and conditions the data (for Output A) input from the Data Board, feeds it to the fast D-A Converters and hence to the Power (Hf) Amplifier for offset addition and amplification. From here the output signal is fed, via a 20 dB attenuator and output relay, to the front panel OUTPUT A connector.

OUTPUT B D-A Conversion and Output Amplifier. As for Output A above.

Calibration Circuitry. This performs a calibration of the Amplitude and Offset DAC's each time a new level is set.

Detailed Theory of Operation

DEVICE BUS INTERFACE (Schematic 7A)

The device bus interface consists of two sub-blocks:

Bus Interface
Settings control, selection of Outputs A, B and TTL/ECL etc.

Bus Interface
The Bus Interface (comprising octal bus transceiver U1, NOR-Gates U2, decoders U3, U4, U5 and diodes CR3, CR4 and CR5) recognizes and activates the board access, decodes the addresses and latches the data. The 8 bit bidirectional data bus - HDD0 to HDD7, the 6 bit unidirectional address bus - HDA0 to HDA5, and the 5 bit unidirectional control bus are interfaced to this board via J11 (Device Bus).

All inputs and outputs are TTL compatible. With LDBV low, the data and address on the device bus are valid. U3 is activated by the signals LCEN and LMHS via NOR-Gates U2 A and B. When HCL1 goes high and HCL2 goes low, diodes CR3, CR4 and CR5 are pulled low resulting in the Arb. Board identifying code number (for the CPU) of hexadecimal 70 being output to the CPU.

When HCL1 and HCL2 go low, bi-directional octal bus transceiver U1 is enabled. U1 is set to read mode by LRHW going low, Data D0 to D7 will then be transmitted to the HDD0 - 7 data bus. In write mode (LRHW = High), all incoming TTL Data (HDD0 - 7) is fed to the D Flip-Flops U9, U601, U603 and U604 ,to the control circuitry DAC's and also EEPROM U6.

Address Decoders U5 and U4, decode addresses 32 to 41. They provide the clock signals for the D Flip-Flops U9, U601 to U605, and the control signals for the DAC's U410/U412/U710/U712. Table 8-6-1 lists the Bus Interface control signals etc.

Table 8-6-1. Bus Interface Control Signals.

BD Adr.	Adr. #	IC/pin	Mnemonic	Signal
70	32	U5/15	HAVLA	Control U410/16
70	33	U5/14	HAVHA	Clock U604/9 Control U410/4,15
70	34	U5/13	HOVLA	Control U412/16
70	35	U5/12	HOVHA	Clock U605A/3 Control U412/4,15
70	36	U5/11	HAVLB	Control U710/16
70	37	U5/10	HALHB	Clock U603/9 Control U710/4,15
70	38	U5/9	HOVLB	Control U712/16
70	39	U5/7	HOVHB	Clock U605B/11 Control U712/4,15
70	40	U4/15	LMBIT	Clock U601/11
70	41	U4/14	HEADS	Clock U9/11

Mnemonic explanations:

Hxxxx	High Level	xxxLx	Low Byte	xMBIT	Mode Bit
Lxxxx	Low Level	xxxHx	High Byte	xEADS	EPROM Address Setting
xAxxx	Amplitude	xxxxA	A Channel		
xOxxx	Offset	xxxxB	B Channel		
xxVxx	Vernier				

Settings Control A/B (Schematic 7A)

This circuitry consists of D Flip-Flops U601 to U605 and Drivers U609 and U610. U601 latches the enable signals for the Trigger and the Outputs A and B. It also latches the control signals for normal/complement mode of A and B and TTL/ECL level selection of the Trigger outputs. U603 and U604 latch the signals for the attenuator relays of Outputs A/B. The initialisation of the control circuitry DAC's is also done via signals CTRLA (B) and LDORA(B) from U603 and U604. U609 and U610 drive all relays on the board. Selection of positive or negative offset for channel A or B is done via signals +/-A (U605/5) and +/-B (U605/9).

AMPLITUDE RANGE AND OFFSET CONTROL CIRCUITRY (Schematic 7B)

This section includes the DAC's U410, U412, U710, U712 the OP Amps U414 A, C, U415C and U714 A, and 715 B. They produce the Amplitude Range and Offset Control voltages for Outputs A and B. The DAC Reference voltages (+ and - 10 VREF) are also produced here (U904, Q900, Q904) and are switched by U906 under control of signals +/- A and B.

These DAC's are 12-Bit DAC's. Since the data bus is only 8 bits wide (D0 to D7), a two step data transfer is required. The required data is formatted as a right-justified 8 + 4 bit data block. (See Figure 8-6-2 for explanation).

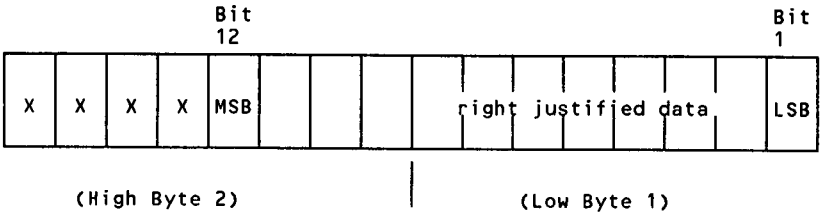


Figure 8-6-2. 8 + 4 Bit Data Formatting.

Figure 8-6-3 shows the timing diagram for automatic transfer of 8 + 4 bit data to the DAC register. The first write cycle loads the first byte of data to the input register. The second write cycle loads the second byte of data to the input register automatically and transfers both bytes to the DAC register. The DAC output is also updated. Table 8-6-2 lists the various DAC control signals etc.

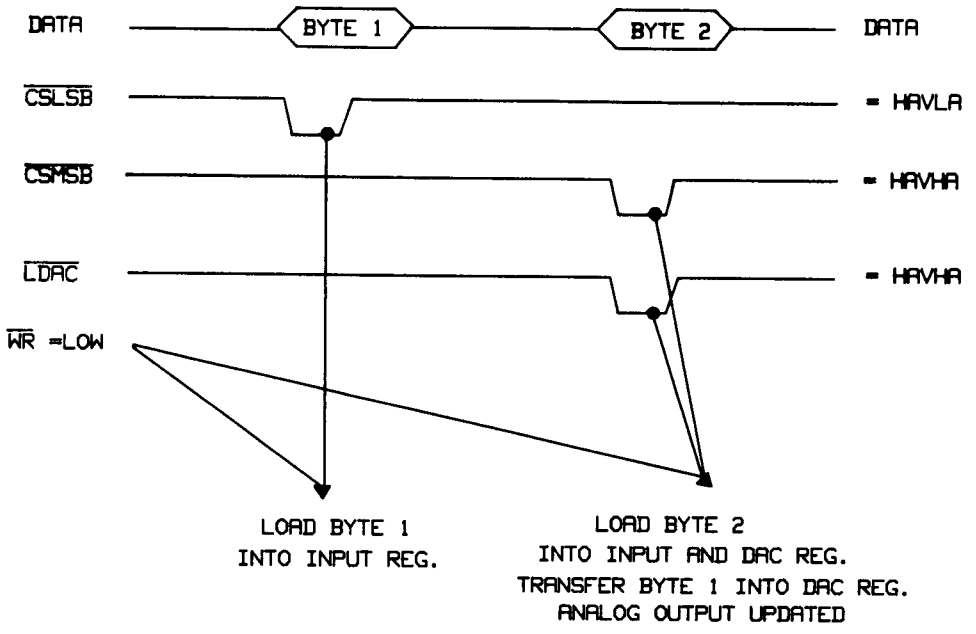


Figure 8-6-3. Automatic 8 + 4 bit Data Transfer.

Table 8-6-2. DAC control signals etc.

	DATA	BIT	HAVLA	HAVHA	HOVLA	HOVHA	HAVLB	HAVHB	HOVLB	HOVHB	LMBIT
LOW BYTE	D0	B1	X	--	X	--	X	--	X	--	HENA
	D1	B2	X	--	X	--	X	--	X	--	HENB
	D2	B3	X	--	X	--	X	--	X	--	HECL
	D3	B4	X	--	X	--	X	--	X	--	HENT
	D4	B5	X	--	X	--	X	--	X	--	N/CA
	D5	B6	X	--	X	--	X	--	X	--	-
	D6	B7	X	--	X	--	X	--	X	--	N/CB
	D7	B8	X	--	X	--	X	--	X	--	-
	IC		U410	U410	U412	U412	U710	U710	U712	U712	U601
HIGH BYTE	D0	B9	--	X	--	X	--	X	--	X	--
	D1	B10	--	X	--	X	--	X	--	X	--
	D2	B11	--	X	--	X	--	X	--	X	--
	D3	B12	--	X	--	X	--	X	--	X	--
	D4	B13	--	L14DBA	--	+/-A	--	L14DBB	--	+/-B	--
	D5	B14	--	L20DBA	--	--	--	L20DBB	--	--	--
	D6	B15	--	LDORA	--	--	--	LDORB	--	--	--
	D7	B16	--	CTRLA	--	--	--	CTRLB	--	--	--
	IC			U604		U605		U603		U605	

To ensure that the DAC's always start from a calibrated status, at 8715A power up the contents of the DAC registers are overridden by pulling the DF/DOR input (pin 5 of U410, 412, 710, 712) low. The CTRL input (pin 6) then determines whether the DAC register data is overridden by all 0s (Offset DAC, CTRL = low) or all 1s (Ampl. DAC, CTRL = high). (See Table 8-6-3).

The selection of a left or right-justified input data format is done by setting DF/DOR = high under control of the CTRL input. (See Table 8-6-3). For normal operation DF/DOR input must be held high.

Table 8-6-3. DAC Registers Contents Over-riding.

DF/DOR	CTRL	Function
Low	Low	DAC register contents overridden by all 0s (Offset DACs)
Low	High	DAC register contents overridden by all 1s (Ampl. DACs)
High	Low	Left-justified input data selected (not used)
High	High	Right-justified input data selected

Figure 8-6-4 shows a simplified DAC circuit. The basic principles as described in the following apply to the Ampl. Range Control and Offset Control DACs apply to the circuits as used on the Arb. Board.

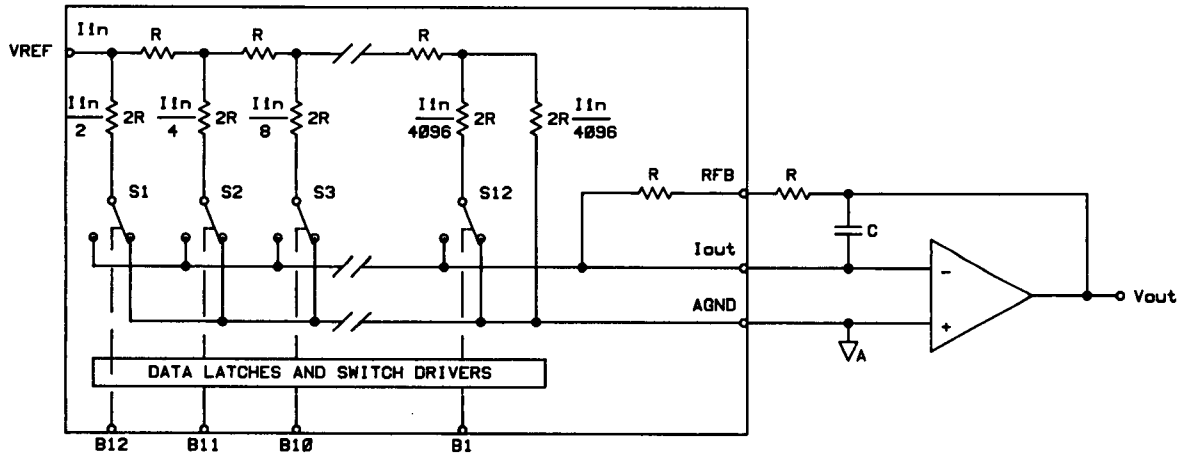


Figure 8-6-4. Simplified DAC Circuit.

The VRef terminal (pin 19 of the Ampl. DAC) is supplied with a negative reference voltage (positive or negative voltage for the Offset DAC's). The total current I_{in} is divided by two for each resistance path it meets (R-2R ladder structure), thus maintaining a constant current in each ladder leg independent of the switch state. By selecting any combination of the digital inputs, output currents between 1/4096 I_{in} and 4095/4046 I_{in} can be output. (See Table 8-6-4 for the relationship). The selected currents are then summed and given out as I_{out} at pin 1.

Table 8-6-4. D to A Conversion Relationship.

Binary Number in DAC register MSB LSB	Analog Output, Vout
1111 1111 1111	$-Vin\left(\frac{4095}{4096}\right) = -max.$
1000 0000 0000	$-Vin\left(\frac{2048}{4096}\right) = -1/2\ Vin$
0000 0000 0001	$-Vin\left(\frac{1}{4096}\right) = -min$
0000 0000 0000	0V

Amplitude Range Control A
The control signal (AVCA) is basically derived from the -10VRef and a multiplying factor. The factor is the decimal equivalent of the input to DAC U410, divided by 4096 (refer to Table 8-6-4). Quad. OP Amp. U414 inverts and scales the DAC output voltage. U414C then produces, with reference to signal VLA (+ 1.000 VRef), the reference voltage AVCA required by U401.

The control signal for B (AVCB) is produced in the same way by DAC U710 and OP Amp. U714 etc.

Offset Control A
The control signal (OVCA) is derived in a similar way to the Amplitude Control one. Basically, a 10 VRef (positive or negative selected via U906 as appropriate) is supplied to DAC U412. It is then scaled and converted by the DAC output buffer (U415C) and output as a signal of value between -/+ 7.8V.

Potentiometers R451 and R454 are used to adjust the gain and offset for the Offset control signal.

TRIGGER CIRCUITRY (Schematic 7C)

Two separate trigger signals are derived from data channels 0 and 2. The differential input signals are converted into single ended signals by U101 and latched via signal HLATCH into U113. These signals are amplified and level shifted to produce either TTL or ECL trigger signals. Thus is done under control of signal LECL via U201, and via the Trigger Output Amplifiers (Q200 to Q204 and Q250 to Q254).

Trigger Output A signal is fed to the front panel BNC connector J706 (TRIG OUTPUT A), Trigger Output B signal is connected to the rear panel BNC connector J707 (TRIG OUTPUT B).

CHANNEL A D-A CONVERSION AND AMPLIFICATION (Schematics 7D 7E 7F)

Data Conditioning (Schematic 7 D)
The DAC used here operates in a multiplying mode. The circuit operation is therefore somewhat different from that previously described (Ampl. Range Control etc.). All incoming differential ECL data-signals (Data 4 to 23) from connector J12 are converted into single ended signals by the line receivers U103, 104, 105. These signals are fed to the latches U108, U109 and synchronized via latch signals

derived from HLATCH/LLATCH. The 10-bit data word (HDCA0-HDCA9) is then fed to the high speed DAC Converter U401.

D-A Convertion (Schematic 7E)

This data is converted to an analog signal between -0.5V to +1.0V (U401/18) by the 10-bit high speed DAC U401. As previously started, the DAC works in the voltage multiplying mode. The DAC output signal, based on reference voltage VLA, is determined by the digital input word and the Range Control voltage AVCA (applied to pin 22). Signal AVCA attenuates the DAC output voltage by a factor of 1/1; 1/1.25; 1/2 or 1/2.5.

Table 8-6-5 shows the significance of the attenuation factor of AVCA, together with 14 and 20 dB attenuators, in Amplitude Range selection.

Table 8-6-5. Amplitude Range Selection.

AVCA ATT Factor	14dB Atten	20dB Atten	Ampl.Range/Step	Off.Range/Step	Load	Max.Datasteps
1/1.25	Off	Off	16Vpp/20mV	+/- 8V/20mV	50 Ohm	800
1/2.5	Off	Off	10Vpp/10mV	+/- 8V/10mV	50 Ohm	1000+24
1/1	On	Off	5Vpp/ 5mV	+/- 8V/ 5mV	50 Ohm	1000+24
1/2.5	On	Off	2Vpp/ 2mV	+/- 8V/ 5mV	50 Ohm	1000+24
1/2.5	Off	On	1Vpp/ 1mV	+/-.8V/ 1mV	50 Ohm	1000+24
1/1	On	On	0.5Vpp/.5mV	+/-.8V/.5mV	50 Ohm	1000+24
1/2.5	On	On	0.2Vpp/.2mV	+/-.8V/.5mV	50 Ohm	1000+24
1/1	Off	Off	32Vpp/50mV	+/-16V/50mV	High Z	640
1/2.5	Off	Off	20Vpp/20mV	+/-16V/20mV	High Z	1000+24
1/1	On	Off	10Vpp/10mV	+/-16V/10mV	High Z	1000+24
1/2	On	Off	5Vpp/ 5mV	+/-16V/ 5mV	High Z	1000+24
1/2.5	Off	On	2Vpp/ 2mV	+/-1.6V/2mV	High Z	1000+24
1/1	On	On	1Vpp/ 1mV	+/-1.6V/1mV	High Z	1000+24
1/2	On	On	0.5Vpp/.5mV	+/-1.6V/.5mV	High Z	1000+24

The bias control voltage source U405/Q404 is set to 0V (nominal GND) via R471 for Glitch minimizing. R409 enables the full-scale output current to be set as required.

Summing Amplifier (Schematic 7 E)

The normal signal (U401/18) and its complement (U401/19) can be interchanged via the normal/complement relay K400.

Normal and complement signals are added in the Summing Amplifier U404 (Transistor Quad.). This amplifier requires a constant current source U403/Q401 for better common mode rejection. The differental output of U404 is passed through a current mirror buffer stage (U406 Transistor Quad.) before being passed to the 14 dB pre-attenuator. This circuit effectively sums the differential output current and in so doing minimizes undesirable output offset and doubles the output current. Offset drift compensation is done by U414D.

HSA14A is the control signal for relay K401, which routes or bipasses the signal through the attenuator network. Refer to Table 8-6-5 for more information concerning attenuation and Amplitude Range etc.

Output Amplifier

The main functions of the Output Amplifier are to amplify the signal from the Summing Amplifier/Pre-attenuator (AMPA) and add the required offset voltage. The amplifier is in principle an inverting operational amplifier (see Figure 8-6-5), with a voltage gain determined by the equation: GAIN = Rfb/Rin.

The main (Hf) Amplifier circuitry (Q501 to Q513) has offset voltages and currents which have to be compensated for by two additional operational Amplifiers. These are: Offset Current and Control Amplifier (U415A) and Offset Voltage Control Amplifier (U415D). The offset current error of the Hf-Amplifier's inverting input is compensated via the Offset Current Control Amplifier. It detects the potential at the virtual ground at the inverting input of the Hf-amplifier. This potential is then compared to ground, the Offset Current Control amplifier then supplies the necessary current via Rc to maintain zero difference.

U415D detects any undesired offset voltage at the Hf-Amplifier output via the feedback network k.Rin/k.Rfb, and compensates it via the non-inverting input of the Hf-amp.

Note: this feedback network must be adjusted to provide the same dividing factor as the Hf-Amplifier feedback network.

The Offset Control Signal (OVCA) (derived from the Offset Control circuitry) is fed to the Hf-Amplifier via the summing point of the Offset Voltage Control Amplifier. It is therefore possible to reduce the necessary offset current by a factor "k". "k" is the constant ratio between corresponding resistors in the Hf-amplifier and the Offset Voltage Control Amplifier feedback networks e.g. Rfb and k.Rfb.
Figure 8-6-6 shows a simplified Hf -amplifier.

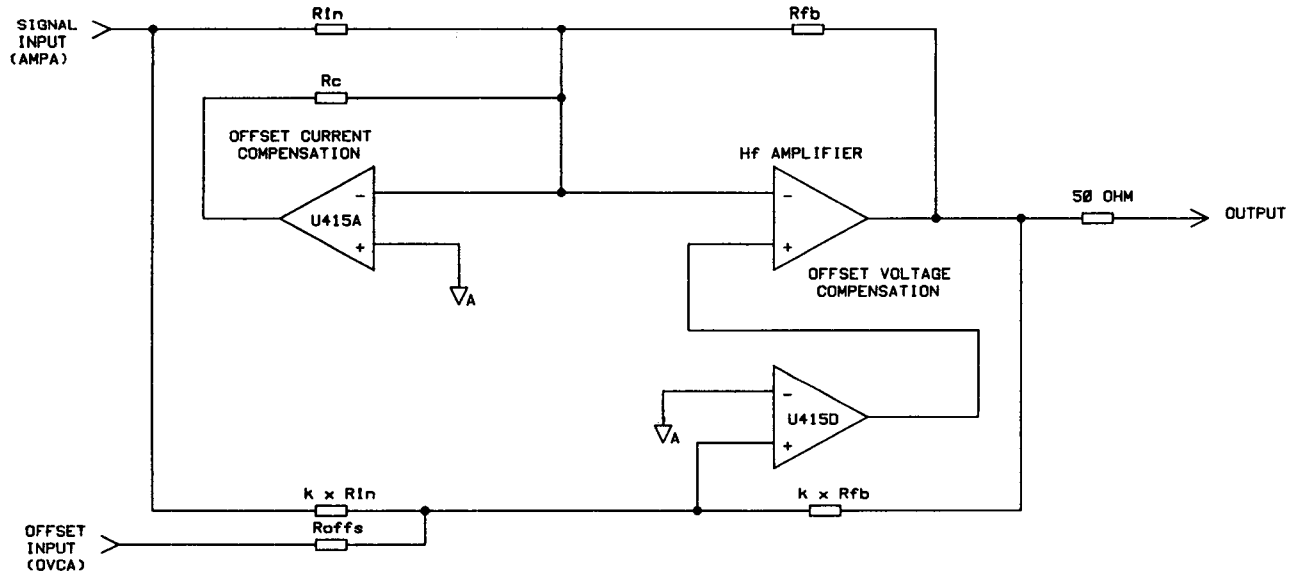


Figure 8-6-5. Simplified Output Amplifier.

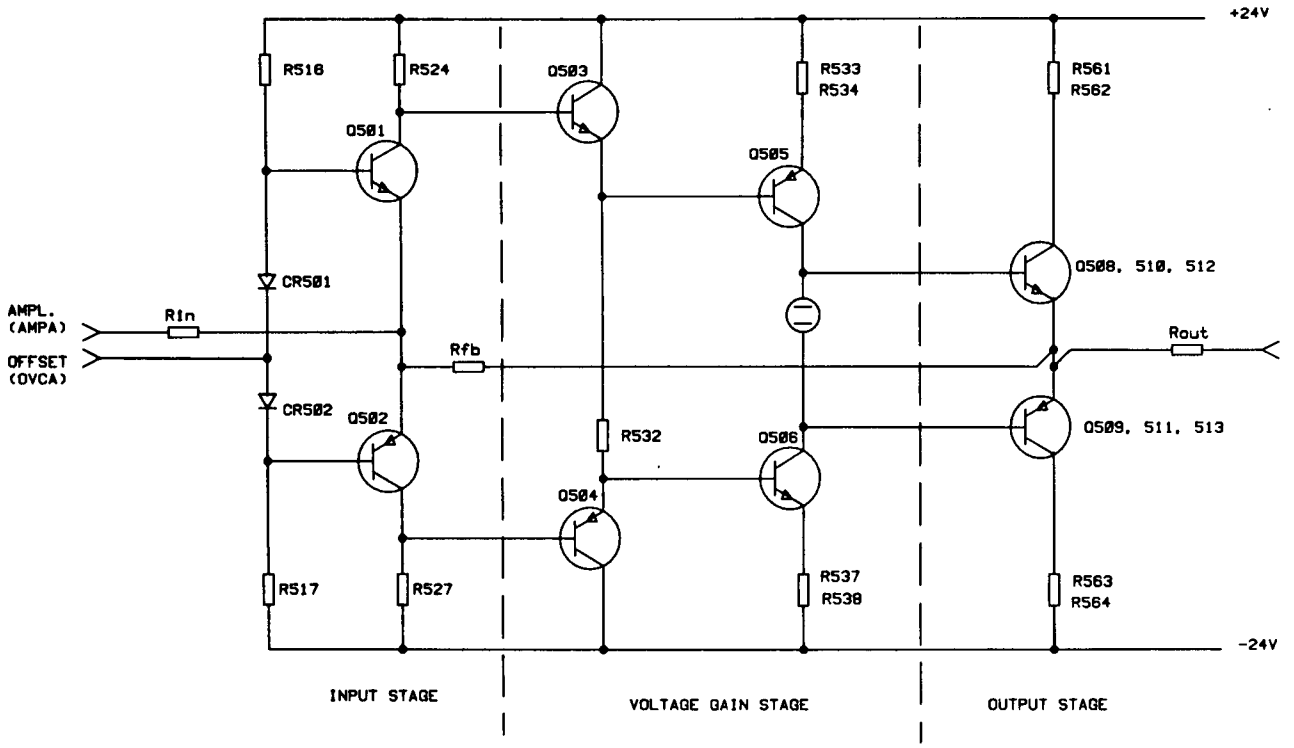


Figure 8-6-6. Hf Amplifier - Simplified Diagram.

The Hf Amplifier (Schematic 7 F)

The Hf-amplifier comprises three stages:

Input Q501/Q502
Voltage Gain Q503 to Q506
Output Q508 to Q513

Referring to Figure 8-6-6, the signal from the Summing Amplifier (AMPA) is applied to the inverting input of the Hf Amplifier where it is amplified by Q501, Q502 (common base amplifiers), CR501 and CR502 provide the required bias voltages. The offset signal (OVCA) is applied to the non-inverting input at the junction of CR501 and CR502, ensuring a constant reference point.

The output signals of this stage, produced across R524/R527 are applied to Q503 and Q504, the voltage gain stage input. These transistors operate as emitter followers and drive Q505 and Q506 to provide the actual voltage gain. The output stage consists of emitter followers Q508/Q510/Q512 and Q509/Q511/Q513 which decouple the low output impedance of Rout from the voltage gain stage.

The Hf Amplifier output is connected to R582/583/584 via R543/544/545/546 which form the 50 Ohm output impedance (Rout). HSA20A is the control signal to relay K501, which directs the signal path through the 20dB attenuator as necessary. The attenuator factor selected depends on the Amplitude range required etc.(See Table 8-6-5). Relay K503, under control of signal LENA enables the output to be enabled/disabled.

The same principles of operation apply for the circuitry associated with Output B. The schematics to be referred to are 7E,7G and 7H.

CALIBRATION CIRCUIT (Schematic 7A)

This circuitry consists of devices U6, U7, U8, U9. To meet the correct output specifications for both outputs, they must be calibrated. Therefore the control words CTL1-112 for all Amplitude and Offset ranges are stored in the EEPROM U6. These words are determined during a special calibration routine during production test. The control words are read by the CPU each time a new level is set and are added to the Standard Settings of the Amplitude and Offset DACs.

ARB. BD. MNEMONICS EXPLANATION

Signals on the 8175A Arb. Board have been assigned mnemonics from which the active state and function of the signal can be determined. A prefix letter (H or L) is used to indicate the active state of the signal (using positive logic) and the remaining letters indicate its function.

Table 8-6-6. Mnemonics and Examples.

Mnemonic	Explanation
+/-A(B)	+/- offset sign switch channel A (B)
AVCA(B)	Amplitude Vernier Control Voltage Channel A (B)
AVCA(B) SENSE	Amplitude Vernier Control Voltage Channel A (B) Sense Line
CTRLA(B)	Control Lines DACs Channel A (B)
D0-7	Data 0-7
EA0-7	EPROM Address 0-7
HAVHA(B)	High Amplitude Vernier High Byte Channel A (B)
HAVLA(B)	High Amplitude Vernier Low Byte Channel A (B)
HDA0-5	High Device Bus Address 0-5
HDATA0	High Data Trigger Line Channel A
HDATA2	High Data Trigger Line Channel B
HDATA4-23	High Data 4-23
HDCA(B) 0-9	High Data Channel A (B) 0-9 (0=LSB)
HDD0-7	High Device Bus Data 0-7
HEADS	High EPROM Address Setting
HECL / LECL	Set Trigger Outputs to ECL Level
HENA(B) / LENA(B)	Enables Output Channel A (B)
HENT / LENT	Enable Trigger Outputs
HLATCH	High Latch Signal
HOVHA(B)	High Offset Vernier High Byte Channel A (B)
HOVLA(B)	High Offset Vernier Low Byte Channel A (B)
HPSV	High Power Supply Valid
LCEN	Low Card Enable
LDBV	Low Device Bus Valid
LDORA(B)	Low Data Override Channel A (B)
LMBIT	Low Mode Bit
LMHS	Low Master/High Slave
LRHW	Low Read/High Write
L14DBA(B) / HSA14A(B)	Sets Attenuator 14dB Channel A (B)
L20DBA(B) / HSA20A(B)	Sets Attenuator 20dB Channel A (B)
N/CA(B) / LN/HCA(B)	Normal/Complement Switch Channel A (B)
OVCA(B)	Offset Voltage Control Line Channel A (B)
VLA(B)	Voltage Load Channel A (B)

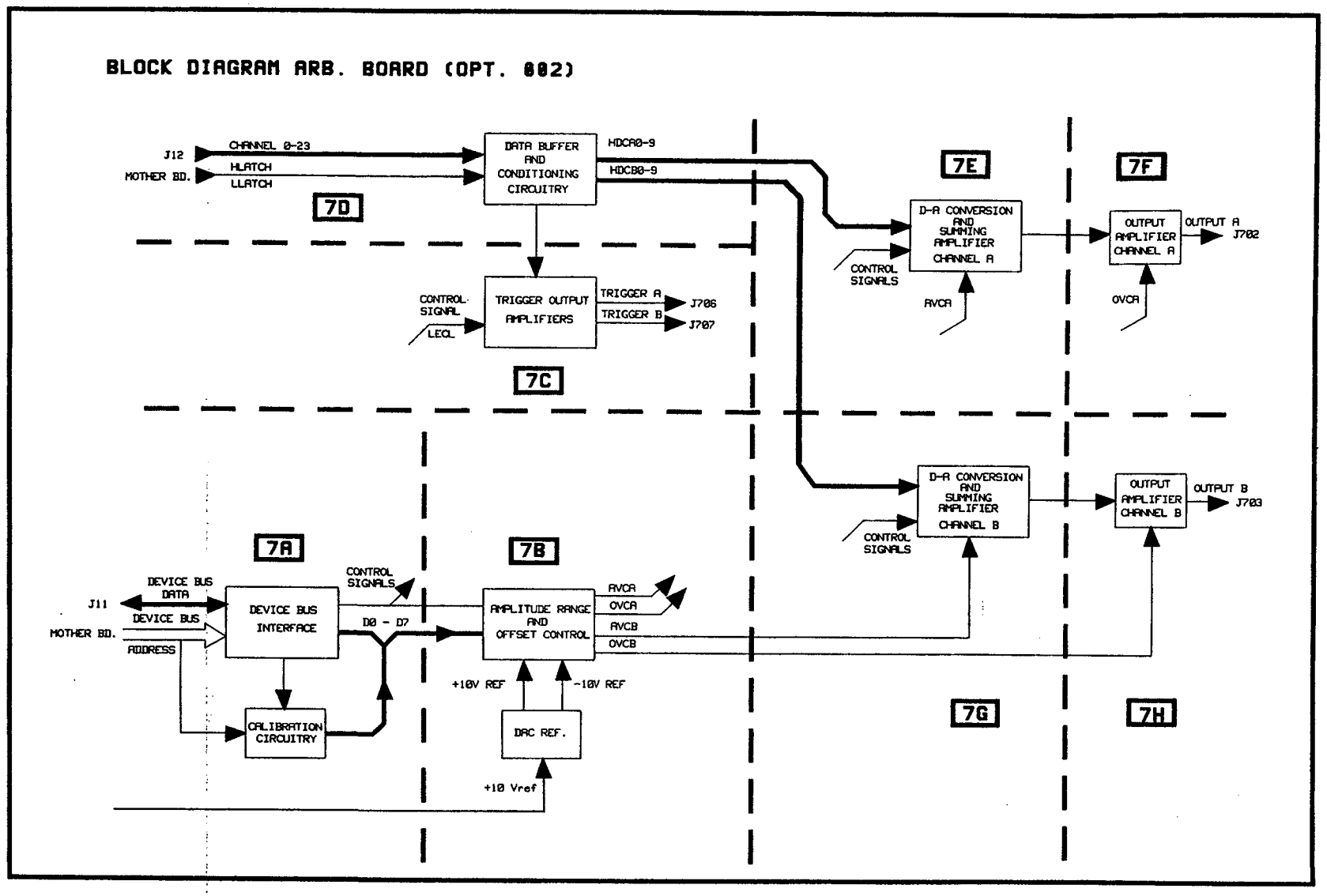


Figure 8-6-1. Arb. Board Block Diagram

TROUBLESHOOTING ARB.

General

Should a fault be isolated to the Arb. Bd. (A70), the theory of operation should be read and understood before proceeding with troubleshooting in this area.

CAUTION

Instrument must not be operated without cover over power supply and fan areas.

Procedure:

With power OFF, unscrew and remove the four stand offs on the rear of the instrument. Remove cover top cabinet MP4. Remove cover bottom cabinet MP5, remove cover bottom MP8. Disconnect the four 50 Ohm cables which are connected to the Arb. board A70.

The cables are:
J707 (W14 yellow, shrink tubing) TRIGGER B, J706 (W8, red, shrink tubing) TRIGGER A, J702 (W10, blue shrink tubing) OUTPUT A and J703 (W11, white, shrink tubing) OUTPUT B.
Remove board A70 (use the supplied board extractors) and plug it into the test (service) connectors. These are accessed by removing cover top front MP9. Arb. Bd. case A70/MP1 can be removed for better troubleshooting.

Switch power ON. After a few seconds the System Page Configuration Menu should appear. If an error message is displayed, press any key to continue. If possible, recall Standard Setting.

1. First check with DVM that the Power Supply Voltages at the following TP's are correct.

TP +24V	+24V	+/-250 mV
TP +15V	+15V	+/-100 mV
TP +10VRef	+10V	+/-8 mV
TP +5V	+5V	+/-50 mV
TP -5V	-5.2V	+/-50 mV
TP -10VRef	-10V	+/-8 mV
TP -15V	-15V	+/-100 mV
TP -24V	-24V	+/-200 mV
TP404/704	+1000V	+/-1mV

2. Set 8175A as follows:
NOTE! UPDATE AFTER CHANGING EACH MENU IN MAIN DISPLAY.
SYSTEM > CURSOR ↓ = Arbitrary Generator (ARB)
CNTRL > CURSOR ↓ = [Single Cycle] > NEXT = [Auto Cycle]
DATA > CURSOR ↓ = Period 0.02 [us] > 1.00 [us]

a. DATA > NEXT = Data [Pattern/Level] Setup
Use MODIFY to set up the level values as shown:

NOTE: LEVELS CHANGE TO ±250mV WHEN AMPLITUDE RANGE IS CHANGED FROM 200mV TO 500 mV

Address	ARB A	ARB B	TRG
0000	+100mV	+100mV	1 1
0511	+100mV	+100mV	1 1

EXEC
Use MODIFY to set up the level value as shown:

0512	-100mV	-100mV	0 0
1023	-100mV	-100mV	0 0

EXEC > UPDATE
OUTPUT > NEXT > enable ARB A, ARB B and TRIGGER.

Change the Amplitude Range to [500 mV] ? 200mV

SYSTEM > NEXT > [store] in location [LOC1] > EXEC

b) DATA > NEXT = Data [Calculator] Page [EDIT] [INSERT]

0 FOR 1MS STEP 1US ↓ CR/LF
1 (SIN (2*Pi*Tx*1000))
[END INST] [END EDIT]
Parameter: FOR ARB A AND ARB B

Max. level: +100 mV
Min. level: -100 mV
[END_Para] [RUN] COMPLETES & PASSES ANNUNCIATOR
[WARNING] SET DURATION VARIABLE IS DISPLAYED
DATA > NEXT = [Pattern/Level] Setup
Use MODIFY to change level value. [BLUE] [UPDATE] TO CLEAR ANNUNCIATOR

NOTE! DATA MAIN DISPLAY WAVEFORM SETUP SHOULD DISPLAY A SINE WAVE FOR ARB A AND B.

Address	ARB A	ARB B
1000	0.000mV	0.000mV
1023	0.000mV	0.000mV

UPDATE CHANGE THE AMPLITUDE TO [500 mV]
SYSTEM > [store] in location [LOC2] > EXEC

(For detailed information on how to set up waveform modules etc., refer to Section 5A (Adjustments Arb.), 5-11 etc.

Connect Trigger Output A to Scope Trigger Input.
Measure with Scope via 10017A Probe signals at the TP's either with setting a or b.

Scope Settings
Ext. Trigger

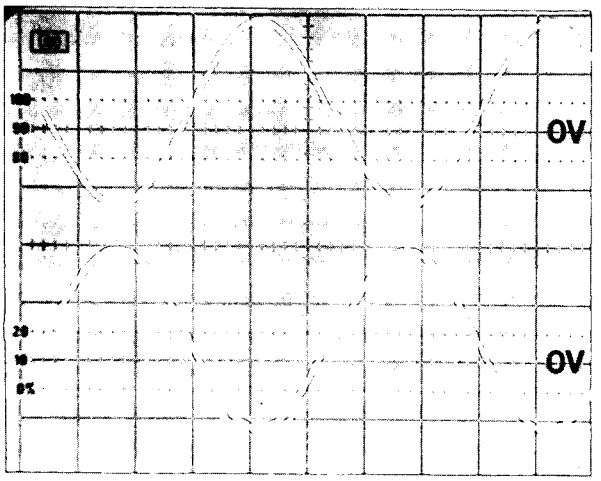
Time/Div .2ms
V/Div 0.05

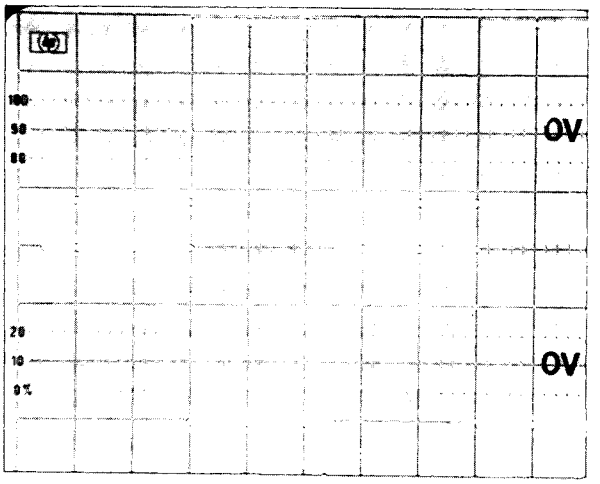
LOC 2 (b. SET UP)

LOC 1 (a. SET UP)

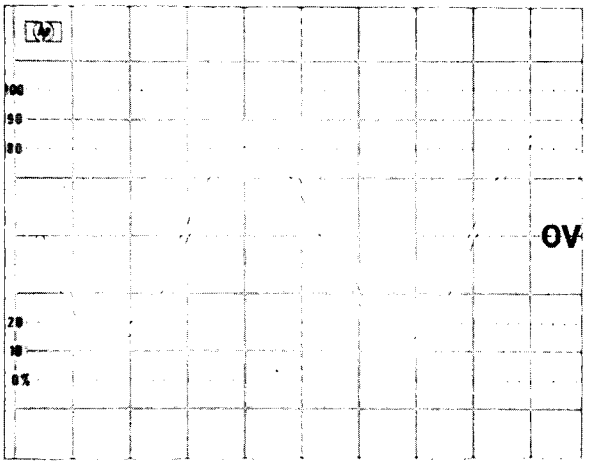
TP401/701

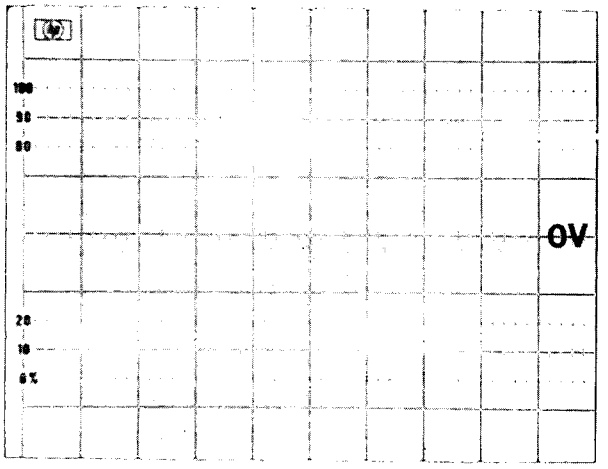
TP402/702





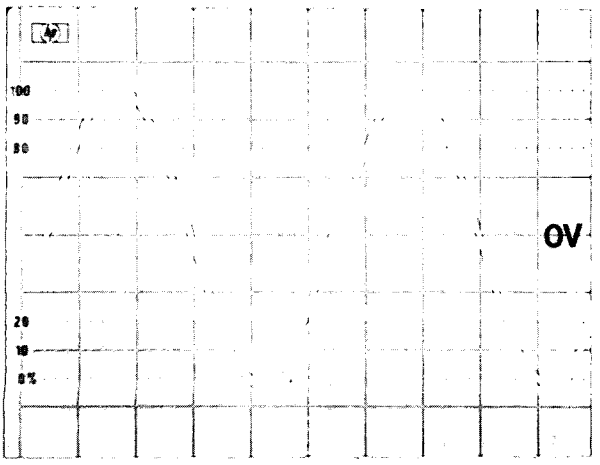
TP403/703

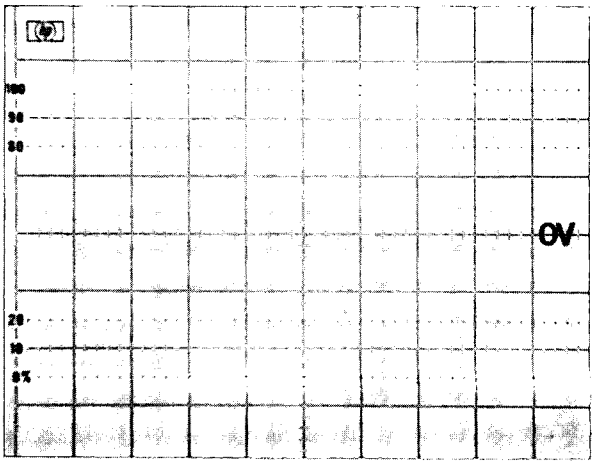




V/Div 0.1

TP510/810





3. Amplitude Vernier Control Output A/B

Measure with DVM at TP410/710 the signal AVCA/AVCB.

The dc voltage depends on the calculated EEPROM correction value. Table 8-6-1 shows the dc voltage with EEPROM set to the defined status (EEPROM data = 128). See Adjustments.

Table 8-6-1.

	Ampl. Range	AVCA Att. Factor	ACVA/AVCB
into 50 Ohm	0.2 V	1/2.5	+ .120 V
	0.5 V	1/1	- 1.2 V
	1 V	1/2.5	+ .120 V
	2 V	1/2.5	+ .120 V
	5 V	1/1	- 1.2 V
	10 V	1/2.5	+ .120 V
	16 V	1/1.25	- .8 V
into open	0.5 V	1/2	- .100 V
	1 V	1/1	- 1.2 V
	2 V	1/2.5	+ .120 V
	5 V	1/2	- .100 V
	10 V	1/1	- 1.2 V
	20 V	1/2.5	+ .120 V
	32 V	1/1	- 1.2 V

4. Current Mirror

To continue correct operation check the signal levels at U406, 407/10, 12 (emitters of transistor quad.) are identical.
Figure 8-6-1 shows the principle of the current mirror operation.

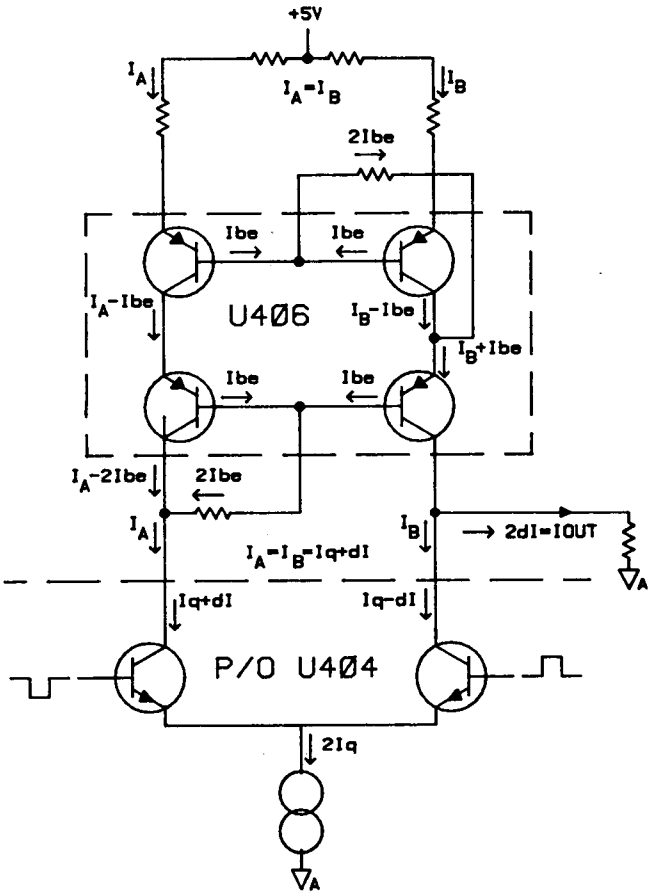


Figure 8-6-1. Current Mirror Principle.

5. Truth tables of control A/B signals

Table 8-6-2.

	Ampl. Range OutputA/OutputB	L14DBA L14DBB	HSA14A HSA14B	14dB Pre-Att. (K401/ K701)	L20DBA L20DBB	HSA20A HSB20B	20dB Att. (K501/ K801)
into 50 Ohm	0.2 V	L	H	ON	L	H	ON
	0.5 V	L	H	ON	L	H	ON
	1 V	H	L	OFF	L	H	ON
	2 V	L	H	ON	H	L	OFF
	5 V	L	H	ON	H	L	OFF
	10 V	H	L	OFF	H	L	OFF
	16 V	H	L	OFF	H	L	OFF
into open	0.5 V	L	H	ON	L	H	ON
	1 V	L	H	ON	L	H	ON
	2 V	H	L	OFF	L	H	ON
	5 V	L	H	ON	H	L	OFF
	10 V	L	H	ON	H	L	OFF
	20 V	H	L	OFF	H	L	OFF
	32 V	H	L	OFF	H	L	OFF

Table 8-6-3.

Output A/Output B	Signal	Status	Signal	Status	Relay	Status
normal/ complement	N/CA	H L	LN/HCA	L H	K400	ON OFF
normal/ complement	N/CB	H L	LN/HCB	L H	K700	ON OFF
enable/ disable	HENA	H L	LENA	L H	K503	ON OFF
enable/ disable	HENB	H L	LENB	L H	K803	ON OFF
TRIGGER OUTPUTS						
ECL/ TTL	HECL	H L	LECL	L H	K200	ON OFF
enable/ disable	HENT	H L	LENT	L H	K201	ON OFF
OFFSET					Switch	
A positive/ negative	+/- A	H L			U906/ 1,3	+10VRef -10VRef
B positive/ negative	+/- B	H L			U906/ 6,8	+10VRef -10VRef

6. Output Amplifier

The following hints will help to isolate a fault in the 8175A Output Amplifier A or B.

CAUTION

Do not operate without heat sinks A70MP2/MP3 installed on board.
If replacement of one of the transistors Q501-Q513/Q801-Q813 is necessary, first remove all heat sink securing screws, then plate and finally, if necessary, the transistor adaptors.
Do not attempt to remove a complete heat sink assembly i.e. plate and transistor adaptors together since damage to transistors will be likely.

Check voltage between CR501 and CR502 (CR801 and CR802). If it is fully negative (approx. -15V) check U415D, Q502, Q504 and Q506 (U715D, Q802, Q804 and Q806). If it is fully positive (approx. +15V) check U415D, Q501, Q503 and Q505 (U715D, Q801, Q803 and Q805).

If Q510, Q511 or Q512, Q513 (Q810-Q813) fail (emitter/collector short circuit) the 8175A regulated power supply rails will switch off. If it is necessary to replace any of the output stage transistors Q508-Q513 (Q808-Q813), check that CR505 and CR506 (CR805, CR806) are not defective.

If the Output A or B in pulse square wave has distored leading or trailing edges, and the input signal at TP403/703 is undistored, then make following test:

Set the 8175A to high output amplitude (16V, sym.)
If leading edge is distored, check Q503/Q505 (Q803/Q805).
If trailing edge is distored, check Q504/Q506 (Q804/Q806).

7. **Offset Vernier Control Output A/B**

Set 8175A:
DATA > NEXT = Data [Pattern/Level] Setup
Use MODIFY to set up the level value to 0.000V for Address 0000 to 1023.

UPDATE
OUTPUT > change the load to [open]
Change the Amplitude Range to [5V].
Change Offset as shown in Table 8-6-4.

Measure with DVM at U415C/8 for Offset A or U714B/7 for Offset B.

Table 8-6-4.

OFFSET A/B	U415/8 U714/7
+ 16 V	- 7.8 V
+ 10 V	- 4.9 V
+ 8 V	- 3.9 V
+ 5 V	- 2.45 V
+ 3 V	- 1.47 V
+ 1 V	- 0.49 V
0.00 V	0.00 V
- 1 V	+ 0.49 V
- 3 V	+ 1.47 V
- 5 V	+ 2.45 V
- 8 V	+ 3.9 V
- 10 V	+ 4.9 V
- 16 V	+ 7.8 V

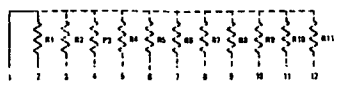
The dc voltage depends on the calculated EEPROM correction value. Table 8-6-4 shows the dc voltage with EEPROM set to the defined status. All voltages are approx. values (+/-10%).

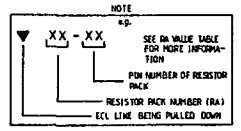
Due to high internal gain of the Output Amp. A or B, the voltage at its non-inverting input at CR501 and CR502 (CR801/CR802) varies by approx. only 5mV about 0V over the whole offset range. If the voltage is at either the max. positive or negative rail value (+ or -15V) then, either U415D/715D or the Amplifier is defective.

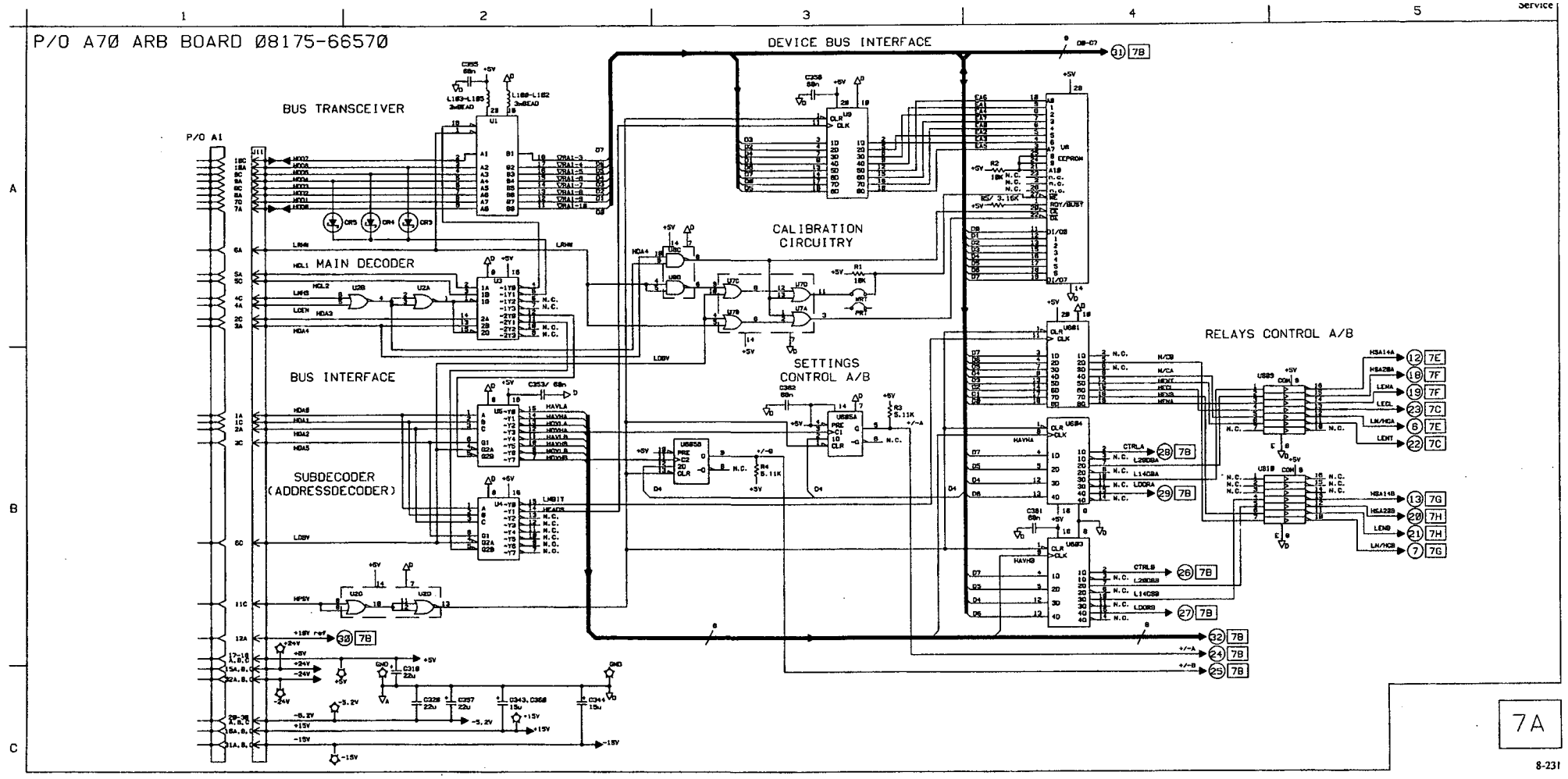
An offset error or failure can also be caused by a fault at U415A/715A, Q514, 515/Q814,815.

Ref. Des.	-5.2V	+5V	-15V	+15V	GND
U1		20			10
U2		14			7
U3		16			8
U4		16			8
U5		16			8
U6		28			14
U7		14			7
U8		14			7
U9		20			10
U601		20			10
U603		16			8
U604		16			8
U605		14			7
U609		9			8
U610		9			8

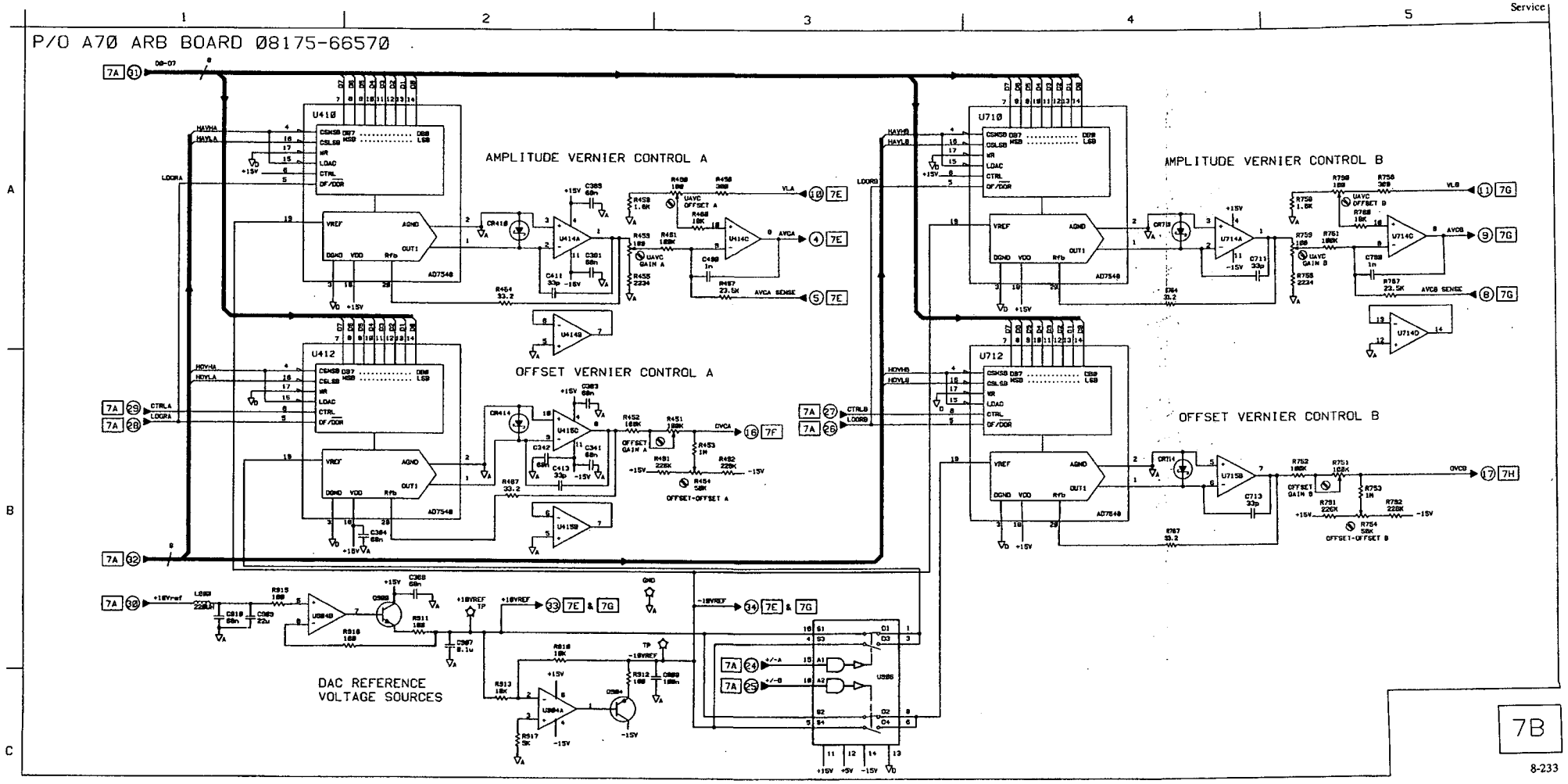
RA	Power Pin	Voltage Level	Resistor Value
1	1	+5V	9x10k







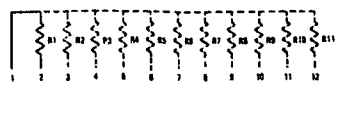
Ref. Des.	-5.2V	+5V	-15V	+15V	GND
U410				18	2/3
U412				18	2/3
U414			11	4	
U415			11	4	
U710				18	2/3
U712				18	2/3
U714			11	4	
U904			4	8	
U906		12	14	11	13



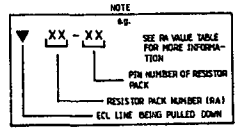
Model 8175A

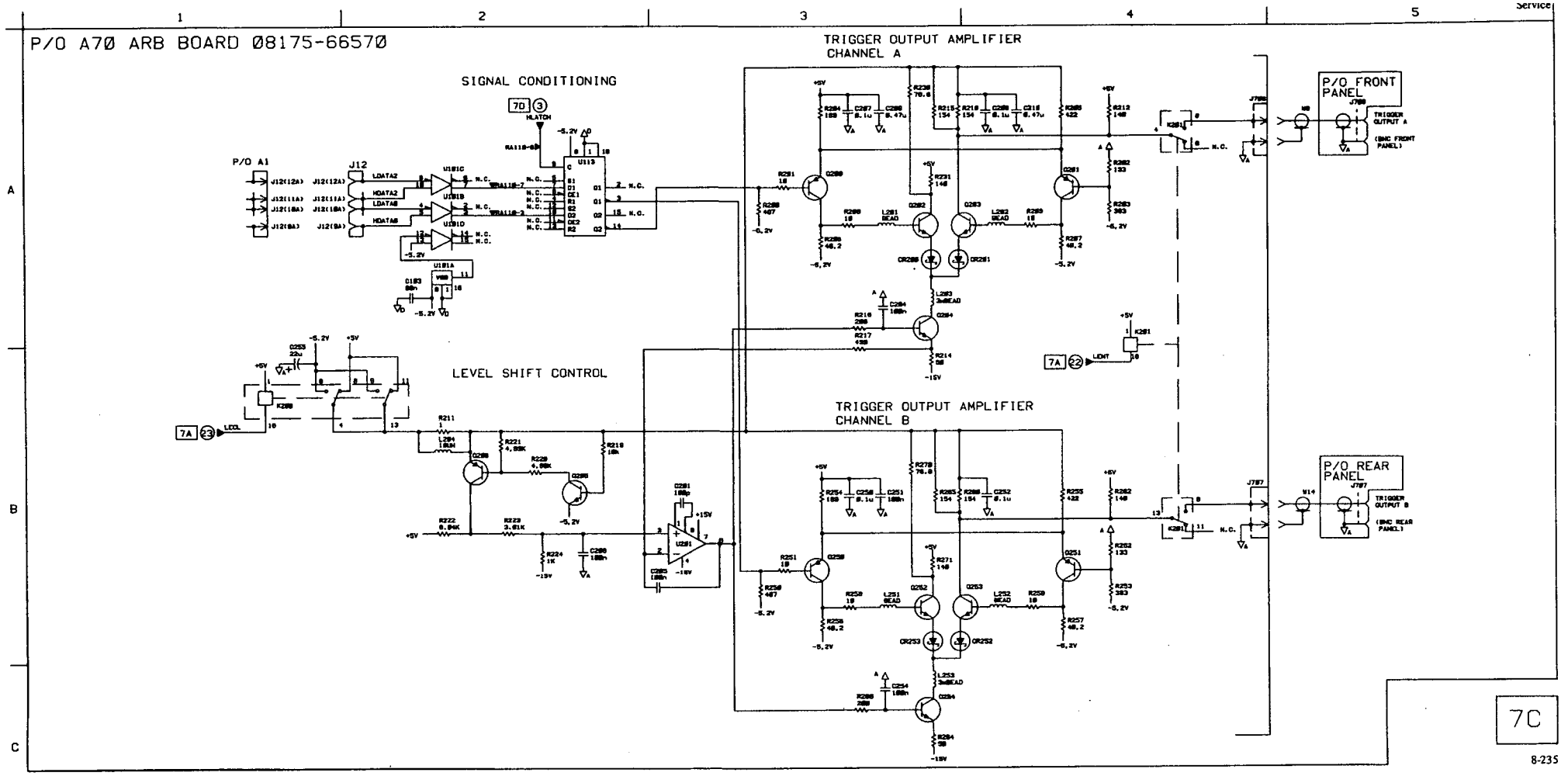
Ref. Des.	-5.2V	+5V	-15V	+15V	GND
U101 U113 U201	8 8		4	7	1/16 1/16

RA	Power Pin	Voltage Level	Resistor Value
110	1	-5.2V	7x330



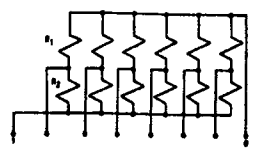
NOTE
6g.

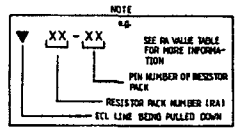


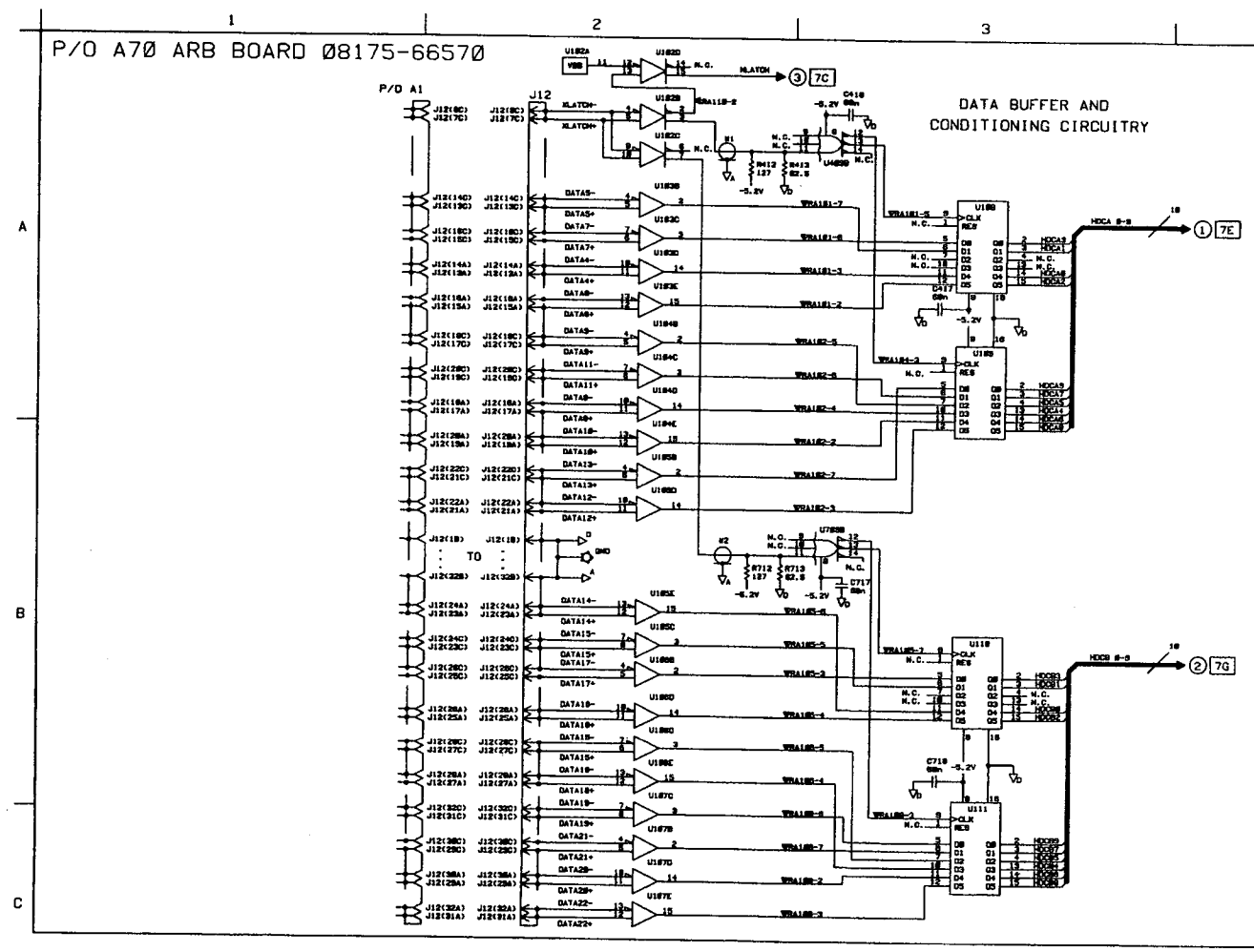


Ref. Des.	-5.2V	+5V	-15V	+15V	GND
U102	8				16
U103	8				16
U104	8				16
U105	8				16
U106	8				16
U107	8				16
U108	8				16
U109	8				16
U110	8				16
U111	8				16
U409	8				16
U709	8				16

RA	Power Pin	Voltage Level	Resistor Value
101	1	-5.2V	8Pin 160/240
102	1	-5.2V	8Pin 160/240
104	1	-5.2V	8Pin 160/240
105	1	-5.2V	8Pin 160/240
106	1	-5.2V	8Pin 160/240
108	1	-5.2V	8Pin 160/240

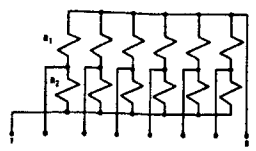


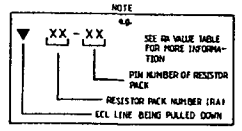


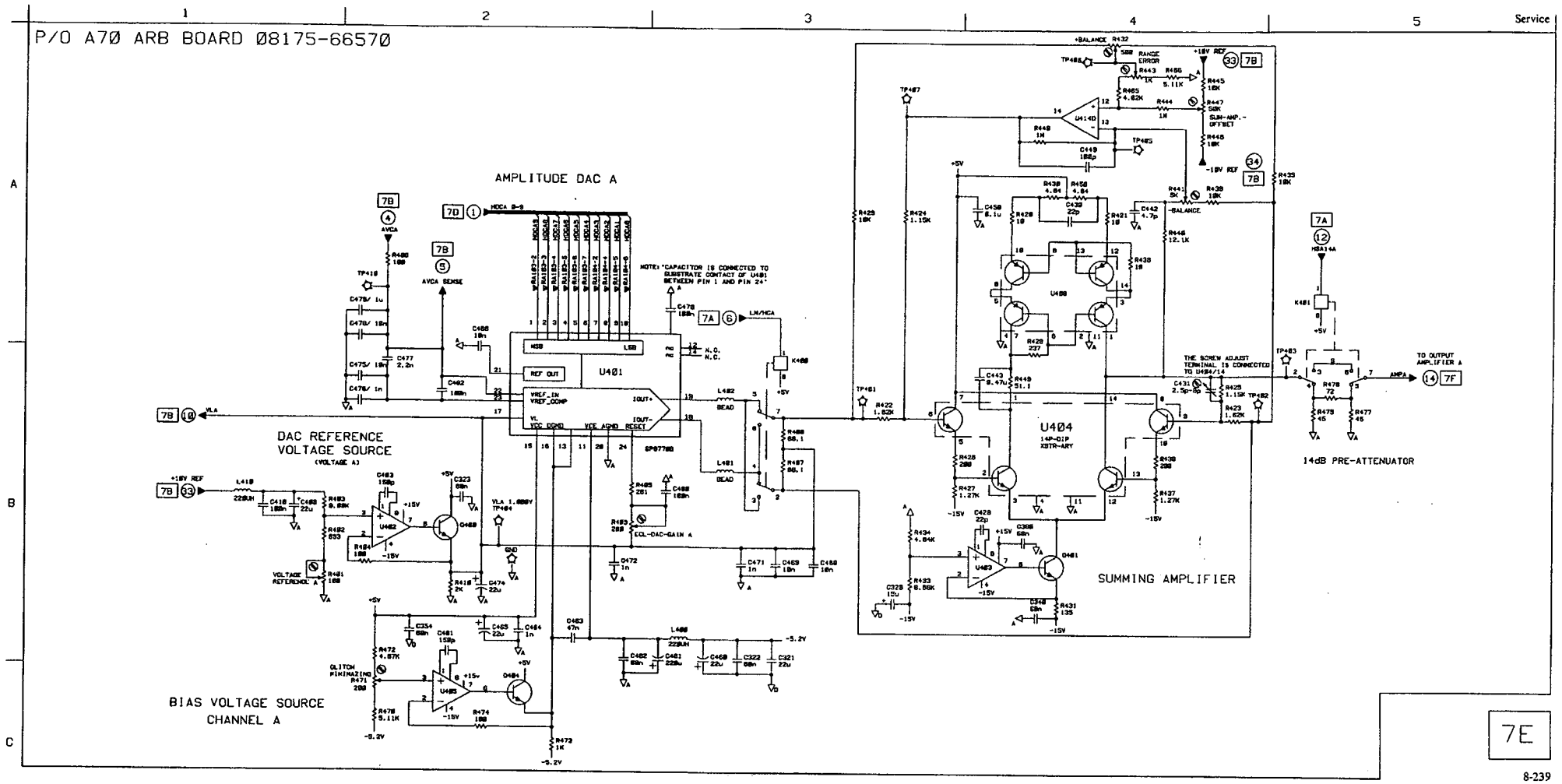


Ref. Des.	-5.2V	+5V	-15V	+15V	GND
U401	11	15	4	7	20
U402			4	7	
U403					4/11
U404			4	7	
U405					4/11
U406					

RA	Power Pin	Voltage Level	Resistor Value
103	1	-5.2V	8Pin 160/240
104	1	-5.2V	8Pin 160/240

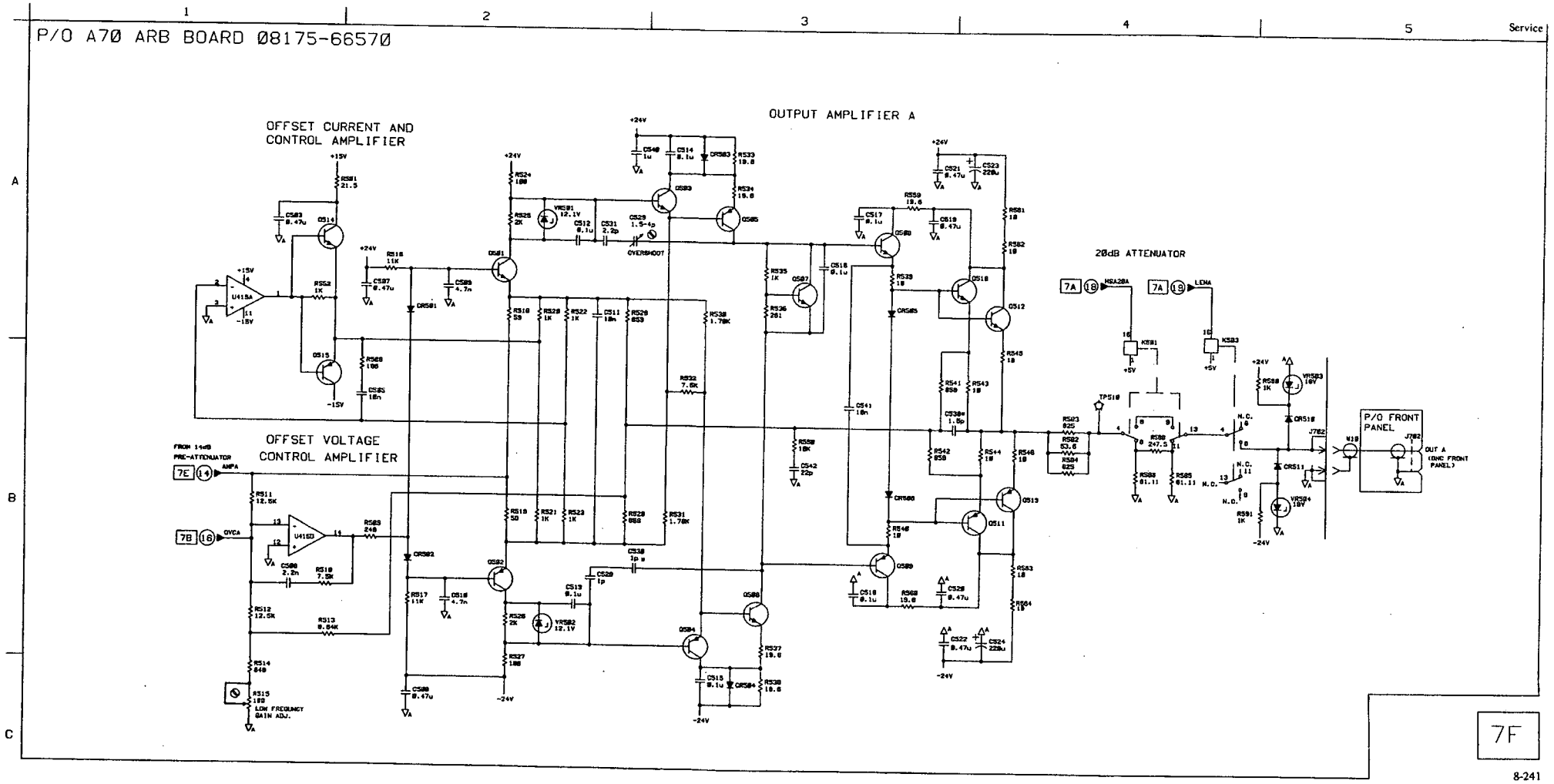






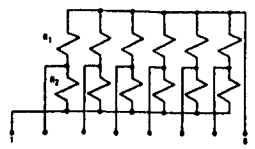
Model 8175A

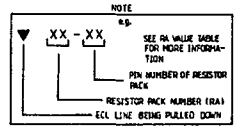
Ref. Des.	-5.2V	+5V	-15V	+15V	GND
U415			11	6	

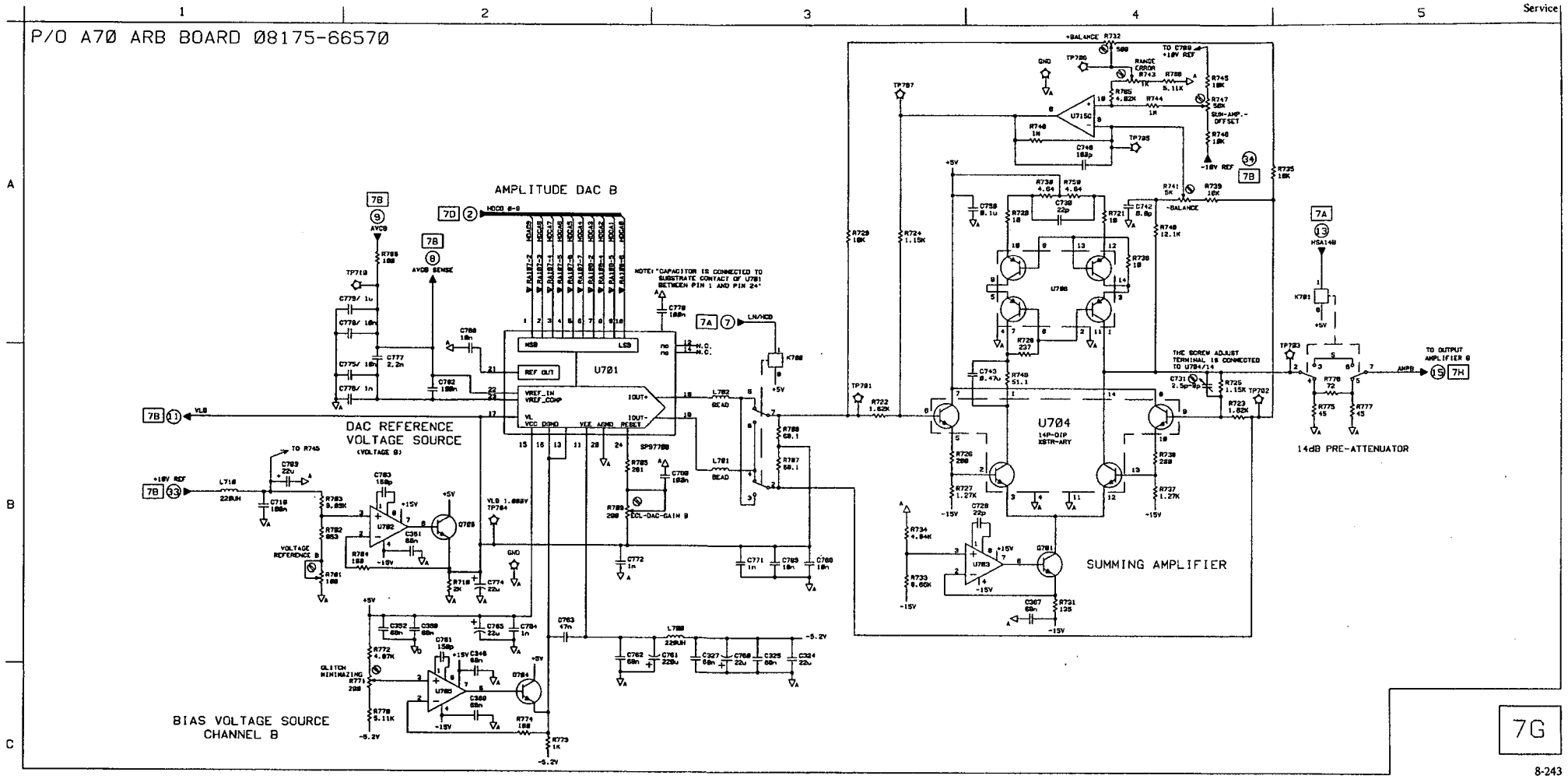


Ref. Des.	-5.2V	+5V	-15V	+15V	GND
U701	11	15			20
U702			4	7	
U703			4	7	
U704					4/11
U705			4	7	
U706					4/11

RA	Power Pin	Voltage Level	Resistor Value
107	1	-5.2V	8Pin 160/240
108	1	-5.2V	8Pin 160/240







Ref. Des.	-5.2V	+5V	-15V	+15V	GND
U715			11	4	

P/O A7Ø ARB BOARD Ø8175-66570

OFFSET CURRENT AND CONTROL AMPLIFIER

OUTPUT AMPLIFIER B

20dB ATTENUATOR

OFFSET VOLTAGE CONTROL AMPLIFIER

FROM 14dB PRE-ATTENUATOR

LOW FREQUENCY GAIN ADJ.

P/O FRONT PANEL J703

OUT 9 (BNC FRONT PANEL)

7H

Service Notes

SERVICE NOTE

SUPERSEDES:
None

HP MODEL 8175A DIGITAL SIGNAL GENERATOR

Serial Numbers: 2612G00416 and above

METRICATION OF THE OUTPUT AMPLIFIER HEATSINK

Problem

The heatsinks A70MP505-513 mounted to A70MP3 HEATSINK PA CH and A70MP805-813 mounted to A70MP2 HEATSINK PA CH are metric parts now.

There is a high probability that the English and metric hardware can be MIXED resulting in damaged hardware.

Solution

At any time an instrument is in for repair and parts (heatsink or screw) in the output heatsink assembly are to be replaced, make sure that you order the correct heatsink and/or screws.

Ordering information see next page.

MI/mi/WO

12/86-B1

HEWLETT PACKARD

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Ordering information is as follows:

ENGLISH THREAD SIZES

Instruments with S/N 2612G00415 and below

A70MP505 to MP513	1205-0329	HT-SINK SGL	(QTY 8)
	2200-0101	SCR-MACH 4-40	(QTY 8 in A70MP3)
A70MP805 to MP813	1205-0329	HT-SINK SGL	(QTY 8)
	2200-0101	SCR-MACH 4-40	(QTY 8 in A70MP2)

METRIC THREAD SIZES

Instruments with S/N 2612G00416 and above

A70MP505 to MP513	1205-0662	HT-SINK	(QTY 8)
	0515-0652	SCR-MACH M3x4	(QTY 8 in A1MP3)
A70MP805 to MP813	1205-0662	HT-SINK	(QTY 8)
	0515-0652	SCR-MACH M3x4	(QTY 8 in A1MP2)

SERVICE NOTE

SUPERSEDES:

None

HP MODEL 8175A DIGITAL SIGNAL GENERATOR

Serial Numbers: 2642G00715 and below

MODIFICATION TO INCREASE THE REALIBILITY OF THE

A / B AMPLITUDE VERNIER CONTROL CIRCUIT

Problem: *Excessive Temperature Drift and LF-Noise.*

On the A 70 BD-AY ARB, Rev A or B (HP 8175A OPT 002 Arbitrary Waveform Generator) the DAC - *SP9770B* - A70 U401 / 701 (P/N 1826-1538) with date codes x8650x or x8716x causes on NON modified boards an excessive temperature drift and a LF-noise.

Replacing the DAC A70 U401 / 701 on a NOT modified REV A, B board with a NEW IC (P/N 1826-1538 with date code x8648x and above) will cause the same problems.

Solution: *Replace DAC A70 U401 / U701.*

At any time an instrument with Serial Number 2642G00715 and below is in for repair and OPT 002 is installed and the date code of A70 U401 / 701 (P/N 1826-1538) is x8650x or x8716x, **make sure the modification is implemented, the board is readjusted, and tested!** See Procedure.

In case of replacing a def. A70 U401 / 701 on a REV A, B board and the date code of the new IC is x8648x and above, follow the same procedure.

MI/mi/WA 12/87-B1

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Procedure

CAUTION

The boards in this instrument are sensitive to electrostatic discharge (ESD).
Please use standard ESD precautions whenever the unit's covers are removed!

1. With the 8175A switched OFF, unscrew and remove the 4 rear frame feed of the instrument.

2. Unscrew and remove the cover bottom cabinet (MP5) and the cover bottom (MP8).

3. Disconnect the 4 SMB-Cables from the A70 Bd-Assy ARB.

4. Remove the A70 board from its slot.

5. Check A70 board revision –> REV A, B, or C (REV C - printed or labeled).
   REV C boards are modified and can be installed back in position!

6. Remove MP1 from Bd A70.

7. If on REV A, B boards the date code of U401 / 701 is x8648x and above and the board is not modified or you have to replace U401 / 701 with a new DAC (date code x8648x and above) do the following:

   Refer to Figure 1. Board Layout and Figure 2. Schematic

   Change: R405 / R705 0698-7220 R-fix 215 Ohm 1%

   Open the connection from U414 pin 1 to R459 and or U714 pin 1 to R759

   Insert (backloaded) R493 / R793 0698-7611 R-fix 563 Ohm 1%
   from U414 pin 1 to R459 / from U714 pin 1 to R759

8. Unscrew and remove cover top cabinet (MP4) and cover top front (MP9).

9. Plug the ARB board into the Service Connector on top of the Mother board.

10. Switch the unit ON and verify that the power up selftest message shows a "Power-Up Complete" indication, and shows on the System Page the Arbitrary Waveform Generator (ARB).

11. Follow the Adjustment procedure for OPT 002 Chapter 5, Para 5-11, step 1 to 6 of the O/S Manual OPT 002 (P/N 08175-90011).
    In step 7. *UAVC Gain A Adjustment.*
    Adjust A70 R459 for -0.8000V +/- 1mV.
    Do steps 8. to 10.
    In step 11. *UAVC Gain B Adjustment.*
    Adjust A70 R759 for -0.8000V +/- 1mV.

    The modifications do not influence steps 12. to 45.

    Follow step 46. to 71.

12. Switch the unit OFF. Carefully re-assemble the instrument.

13. Switch the unit ON, and follow the Performance Test for OPT 002, Chapter 4 of the O/P Manual OPT 002 (08175-90016).

Figure 1. Board Layout

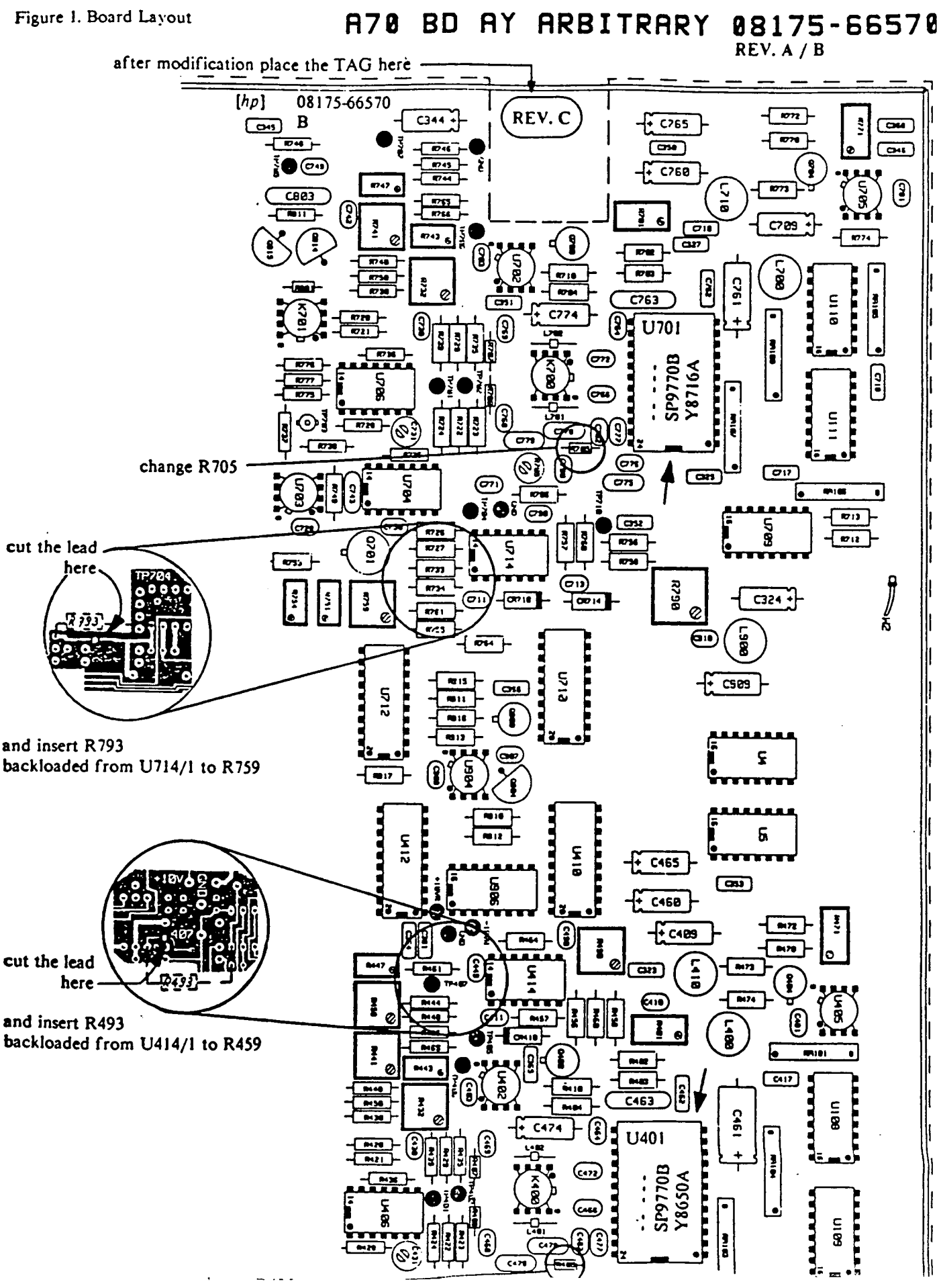
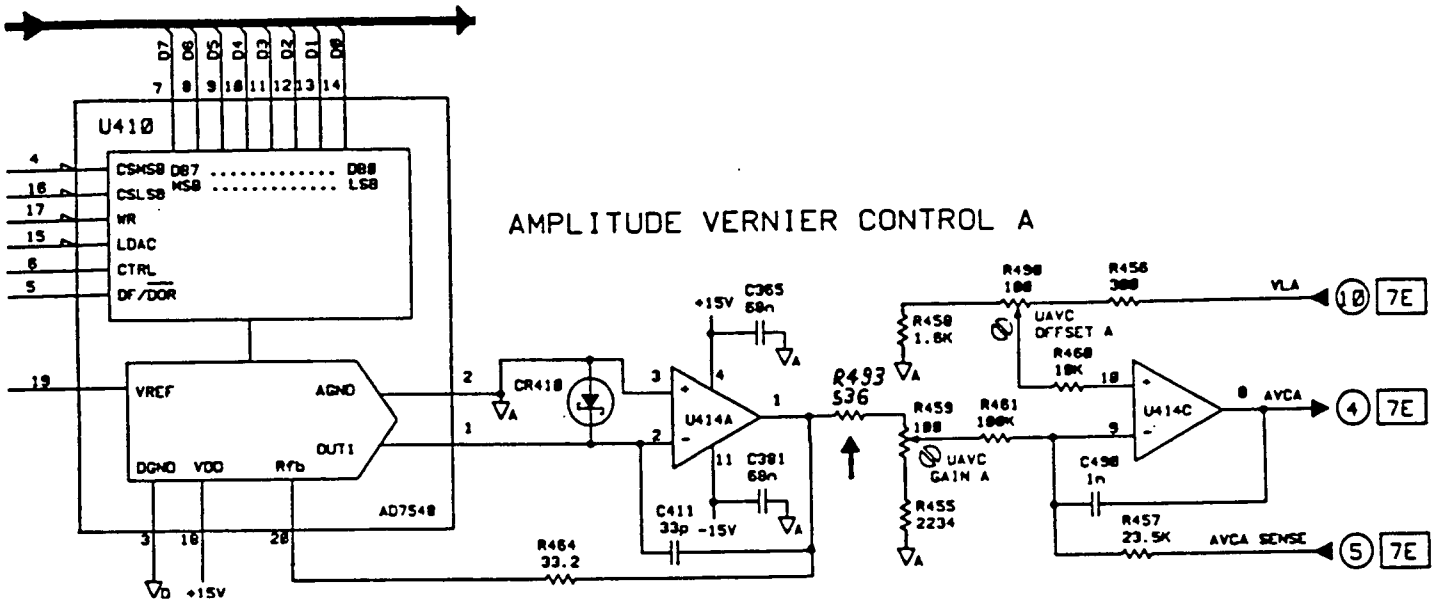
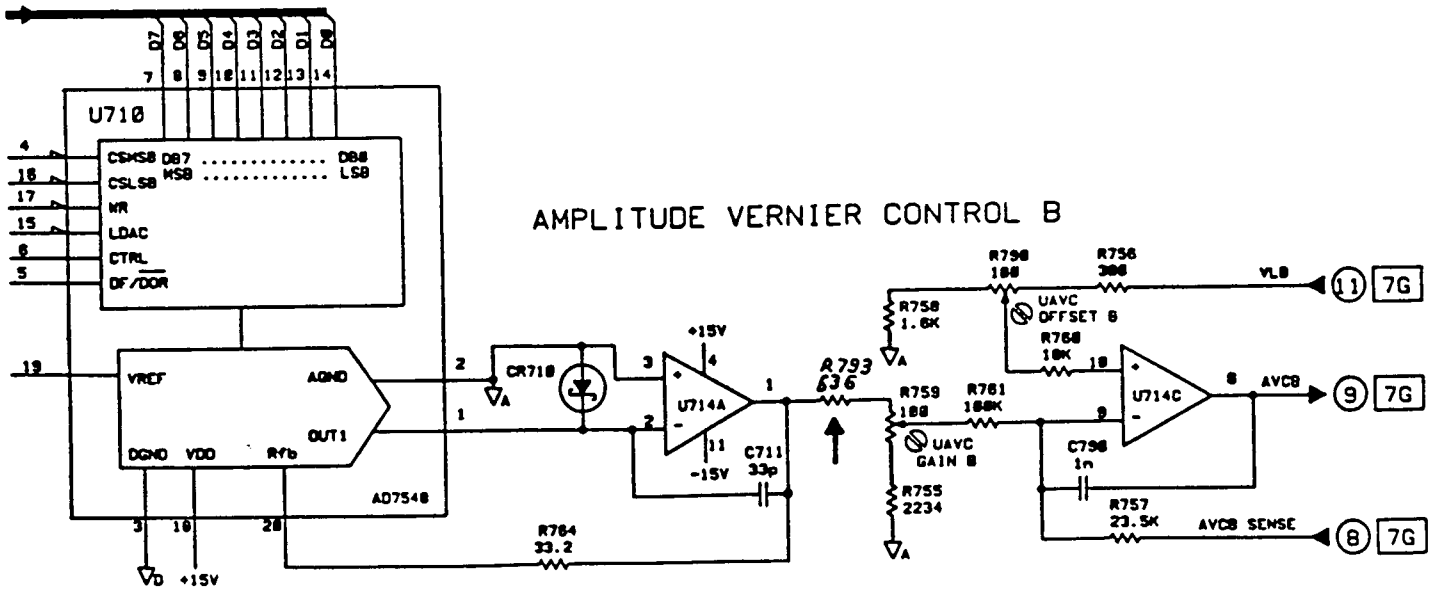


Figure 2. Schematic 7B P/O A70 ARB BOARD 08175-66570





HEWLETT PACKARD

MANUAL CHANGES

Manual for Model Number	8175A
Manual printed on	July 1985
Manual Part Number	08175-90001

07/92

Make all ERRATA corrections.

Check the following table for your instrument serial prefix/serial number /EDC and make the listed changes to your manual.

▶ New Item

Serial Prefix or Serial Number		Manual Changes
ERRATA		
2520G00231	#001	
2520G00251	and above	1
2520G00271	and above	2
2612G00326	and above	3
2612G00356	and above	4
2612G00396	and above	5
2612G00415	and above	6
2612G00435	and above	7
2612G00456	and above	8
2642G00576	and above	9
2642G00616	and above	10
2642G00956	and above	11
2642G00996	and above	12
2642G01036	and above	13
2642G01116	and above	14
2642G01326	and above	15
2903G01446	and above	16
2903G01506	and above	17
2932G01606	and above	18
2948G01646	and above	19
2948G01706	and above	20
2948G01726	and above	21
2948G01766	and above	22
2948G01946	and above	23
CHANGE TO EDC LABELS ON BOARDS (X-3116)		
2948G01966	and above	24
2948G02146	and above	25
2948G02176	and above	26

MODEL 8175A

INDEX OF MANUAL CHANGES

MANUAL CHANGE	MISCELLANEOUS	FRAME	A1	A2	A10	A20	A30	A31	A40
ERRATA	Page 6-8,6-9, 6-10,6-12 6-18,6-19 6-21,7-8, 8-25,8-29, 8-55, 8-128/129 8-142, 8-148, 8-159, 8-162								
1	Page 6-11					U701			
2	Page 6-10/11					R206,207 W1 U312,313	C99		
3	page 6-10					U210,211, U106,107, U109,111 W1 U108,110 W2			
4		MP11							
6					R29	R700			
7				A2 W1					

MODEL 8175A

INDEX OF MANUAL CHANGES

MANUAL CHANGE	MISCELLANEOUS	FRAME	A1	A2	A10	A20	A30	A31	A40
8	Page 6-13						R120,121, DL2		
9	Page 6-8 Page 6-5	A5, A6 MP2,12 B1,2			J4				
10	Page 6-16/17								U105,RA24, R124
11				S1-39	C55				
12		MP47							
13	Page 6-16								R124
14									R25
15						U406-413			
16		MP4 - 7, MP60,41, MP48,59, MP49,51, MP50,52							
17	B1,2,W1,2,3,5				CR18,19				R50,51,RA34 U140-141 U153-158, R124,RA12,13 RA16,17, U159-176 U144-152 U142,143
19		A20				U508			

MODEL 8175A
INDEX OF MANUAL CHANGES

MANUAL CHANGE	MISCELLANEOUS	FRAME	A1	A2	A10	A20	A30	A31	A40
20							U9,10,30,31		U185,186 U187,188, U189
22					CR5				
23					R29, U8				
: CHANGE TO EDC LABEL (X-3116) ON BOARDS ! ! !									
24									U140,141 U153,154, U155,156, U157,158, U142,143
25					C55				
26		A10			CR1, S1				

MODEL 8175A

INDEX OF MANUAL CHANGES

MANUAL CHANGE	MISCELLANEOUS	FRAME	A50
2	Page 6-18		C7,8,12,16,17,21,24 C26 thru 32 C34 thru 37 C40,41,42 C44
3			R800
5	Page 6-19		C207,217,227,237
17			C7,8,12,16,17,21,22 C24,26,27,28,29-32, C34-37,41,42
CHANGE TO EDC LABELS (X-3116) ON BOARDS ! ! !			

MODEL 8175A

INDEX OF MANUAL CHANGES (OPTION 001)

MANUAL CHANGE	MISCELLANEOUS	FRAME	A50 Option 001	
1	Page 6-19/6-20		C7thru12 C16thru32 C34,35,36, C37,40,41,42 C46thru60 C44	
17			C7-12,16-32, C34-37,40-42, C46-60	

CHANGE TO EDC LABELS (X-3116) ON BOARDS ! ! !

ERRATA

Make all ERRATA corrections

*Note: Since the Operating and Programming manual (08175-90006) can be separately ordered, it has its own Errata sheet (covering sections 1 to 4). This suplement covers errata and/or manual changes for sections 5 to 8 (service sections) only.

General point: Referring to Section 8 of the 90001 manual, some copies have the layout diagrams inserted (incorrectly) behind the corresponding registers instead of after. This can be easily checked and rectified.

Page 6-8: Change the Part Numbers/Descriptions etc. of the following components:

A10 C55	0160-3097	
A10 CR18	08175-88701	DIODE KIT
A10 CR19	08175-88701	DIODE KIT

Page 6-9:

Add:	A10 TP1 (CD=2)	1251-0628	CONN POST TP SKT
Change	A10 TP2-12 to:	0360-0535	TEST POINT

Page 6-10:

Add:	A20 MP1 (CD=3)	0380-0643	MOUNTING STUD

Change M 246 to read: MP2

Change following details of A20 U406 - 413 to read as shown:

1818-3483 IC TMS 4164-15NL

Page 6-12:

Add:	A30 MP14	1252-0220	DUST COVER

Page 6-18: Change following details of A40 W1 - W5 to read as shown:

1258-0124 JUMPER

Add:	W6,W7,W8	1258-0124	JUMPER

Add a * in front of W1,4,5,6 and 8 and a corresponding note to indicate that these jumpers are not necessarily installed on all A40 boards.

Page 6-19: Change following details of A50 R103 to read as shown:

0698-3444 R-F 316 1% .125W

Page 6-21: Change following details of A50 W1 to W3 to read as shown:

1258-0124 JUMPER

Add a * in front of W1 and W3 (indicates installed as required).

Page 7-8: At end of second to last paragraph, change last line details to read: "_delay circuit (schematic 51D)."

ERRATA (Cont.)

Page 8-25: Waveform photos for TP 10 and 9, change "1V/DIV" to read: "0.5V/DIV".

Page 8-29: Add the title: "Table 8-1-2" below left hand table.

Page 8-55: Towards end of the first paragraph, details should read:
"_of U210 (HF0-HF5)".

Pages 8-128/129:
For both cases where signals are to be compared with TP16 signal, the menu required should read:
"Control Page (PAR) [Clock]".

Page 8-142: In the Grid Locator list add a * (indicates installed as required) in front of W1, W4, and W5. Delete the * in front of W7.

Page 8-148: In the middle paragraph which starts "The shift registers U25/U26_", change text in the appropriate sentence so that it reads as follows:
"The control circuit is initialized with signal HADDS, signal LTIMELOAD1 stops the control circuit and shift register for the timing duration."

Page 8-159: Referring to the lower photo and corresponding test settings,
change "Delayed" to "Mixed" and change photo reference from "U11/12" to U14/2".

Page 8-162: Referring to the lower photo and corresponding test settings, the settings should read as follows:
"_Width 500ns, Ampl. +2V, Delay min, TT min, Offset OFF, Norm+)
Scope settings: 2us/Div, 0.05V/Div"

Page 6-4: Figure 6-1, 8175A Mainfraim Parts change in the picture where the frame Parts are shown W9 Yell To W14 Yell.

Page 6-5: ADD: W14 08175-61611 CBL SMB/BNC

Page 6-5: Change to read: MP2 08175-00138 BRACKET MID

ERRATA (Cont.)

ADD to SECTION 8 SERVICE:

8-20 POD INFORMATION

8-21 In the case of isolating a foult down to a POD, Input or Output POD, take the info given in Table 8-3 to order the correct POD replacement.

Table 8-3. Index of POD's

MODEL NO	Replaceable P/N
HP 15461A ECL POD	15461-69601
HP 15462A TTL/CMOS POD	15462-69601
HP 15463A TRIGGER POD	15463-68701
HP 15464A TTL POD	15464-69601

8-22 ACCESSORIE INFORMATION

8-23 Table 8-4 shows the replaceable part numbers of the available Accessories.

Table 8-4. Index of Accessories

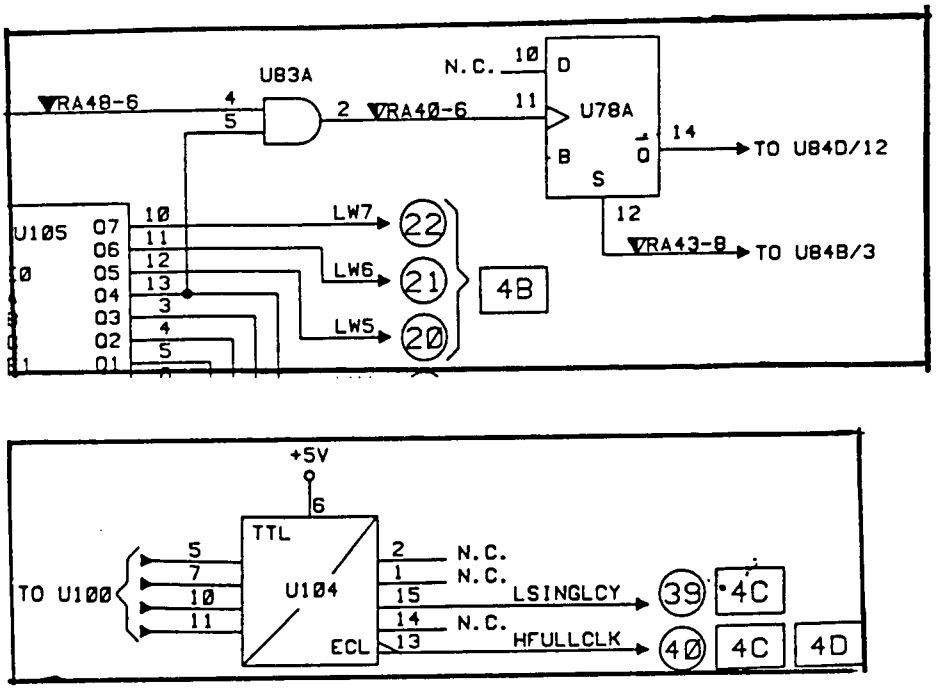
MODEL NO	Replaceable P/N
HP 15408A	15408-68701
HP 15409A	15409-68701
HP 15410A	15410-68701
HP 15411A	15411-68701
HP 15415A	15415-68701
HP 15429A	15429-68701

On Page 6-19, change the Table of Replaceable Parts to read:

A50	J9,10	1251-7799	Conn-Post-TP-HDR

ERRATA (Cont'd)

On Page 8-167, change Schematic and Grid Locator to read:



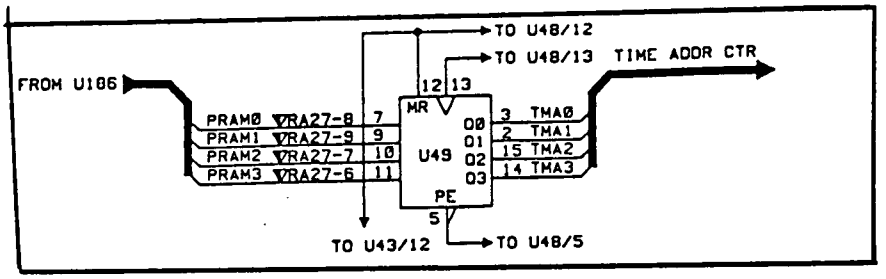
RA	GND PIN	POWER PIN	VOLTAGE LEVEL	RESISTOR VALUE
43	10	1	-5.2V	10 PIN 160/240
51		1	+5V	9X10K

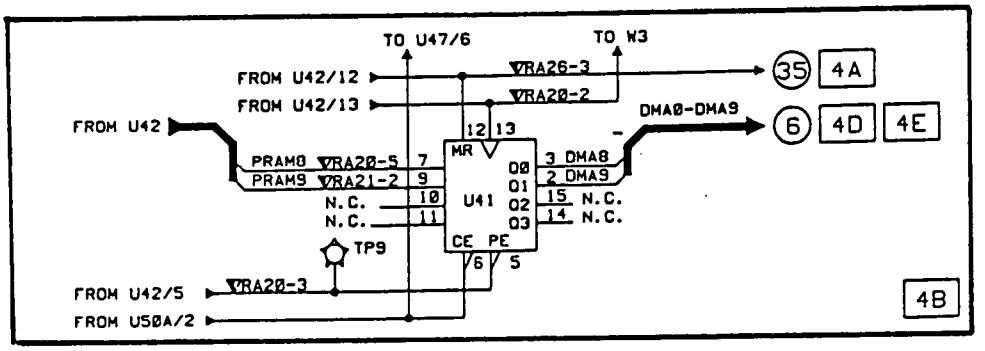
REF.DES.	-5.2V	+5V	-15V	+15V	GND
U84	8				1,16
U92		16			8

DELETE U91

ERRATA (Cont.)

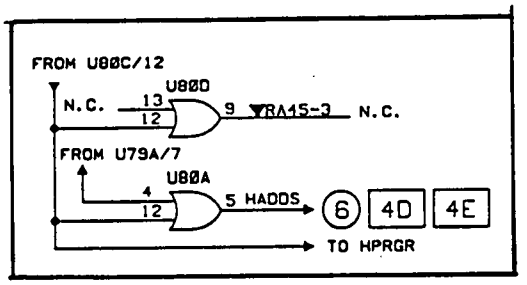
On Page 8-169, change to read:

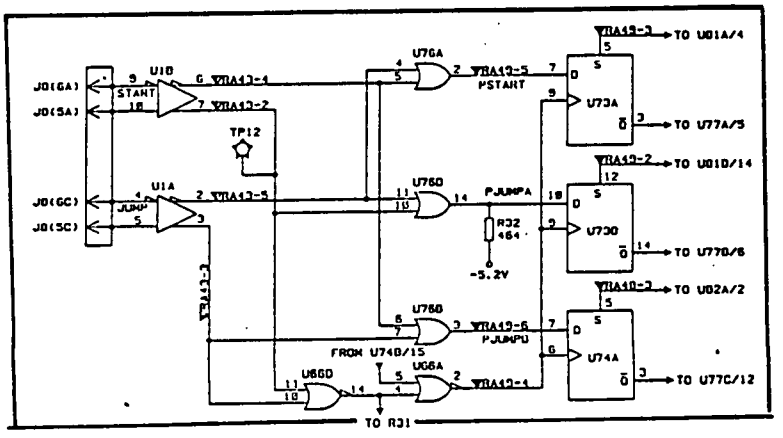




RA	GND PIN	POWER PIN	VOLTAGE LEVEL	RESISTOR VALUE
20	8	1	-5.2V	8PIN160/240
21	10	1	-5.2V	10PIN160/240
22	10	1	-5.2V	10PIN160/240
23	8	1	-5.2V	8PIN160/240
24	10	1	-5.2V	10PIN160/240
25	10	1	-5.2V	10PIN160/240
26	10	1	-5.2V	10PIN160/240
27	10	1	-5.2V	10PIN160/240
39	10	1	-5.2V	10PIN160/240
41	8	1	-5.2V	8PIN160/240
42	8	1	-5.2V	8PIN160/240
52	10	1	-5.2V	10PIN160/240

REF.DES.	-5.2V	+5V	-15V	+15V	GND
U79	8				1,15,16
U80	8				1,16
U81	8				1,15,16





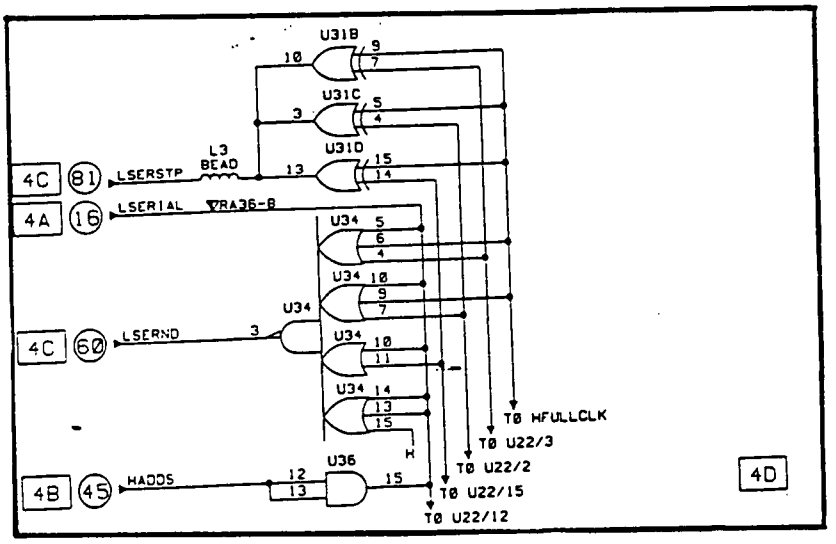
ERRATA (Cont.)

On Page 8-171 change to read:

RA	GND PIN	POWER PIN	VOLTAGE LEVEL	RESISTOR VALUE
11	10	1	-5.2V	10PIN160/240
28	8	1	-5.2V	8PIN160/240
29	8	1	-5.2V	8PIN160/240
30	10	1	-5.2V	10PIN160/240
31	8	1	-5.2V	8PIN160/240
32	10	1	-5.2V	10PIN160/240
33	10	1	-5.2V	10PIN160/240
35	8	1	-5.2V	8PIN160/240
36	10	1	-5.2V	10PIN160/240
37	8	1	-5.2V	8PIN160/240
38	8	1	-5.2V	8PIN160/240
54	10	1	-5.2V	10PIN160/240

DELETE RA34

On Page 8-173, change to read:



On Page 8-175, change to read:

RA	GND PIN	POWER PIN	VOLTAGE LEVEL	RESISTOR VALUE
42	8	1	-5.2V	8PIN160/240
51		1	+5V	9X10K

4E

On Page 8-108, : change C95 to read C99
change C99 to read C95

MANUAL CHANGE 1

On Page 6-11, change the Table of Replaceable Parts to read:

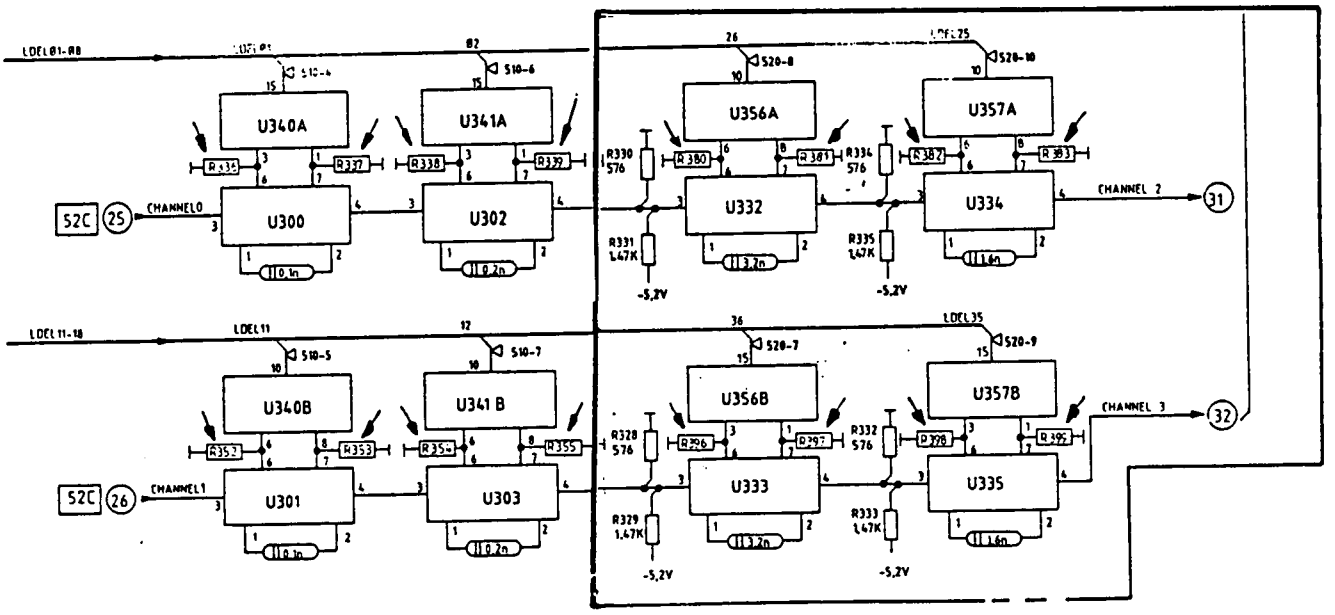
	A20 U701	1820-3911	IC 9513A

OPTION 001

On Page 6-19, 6-20, change the Table of Replaceable Parts to read:

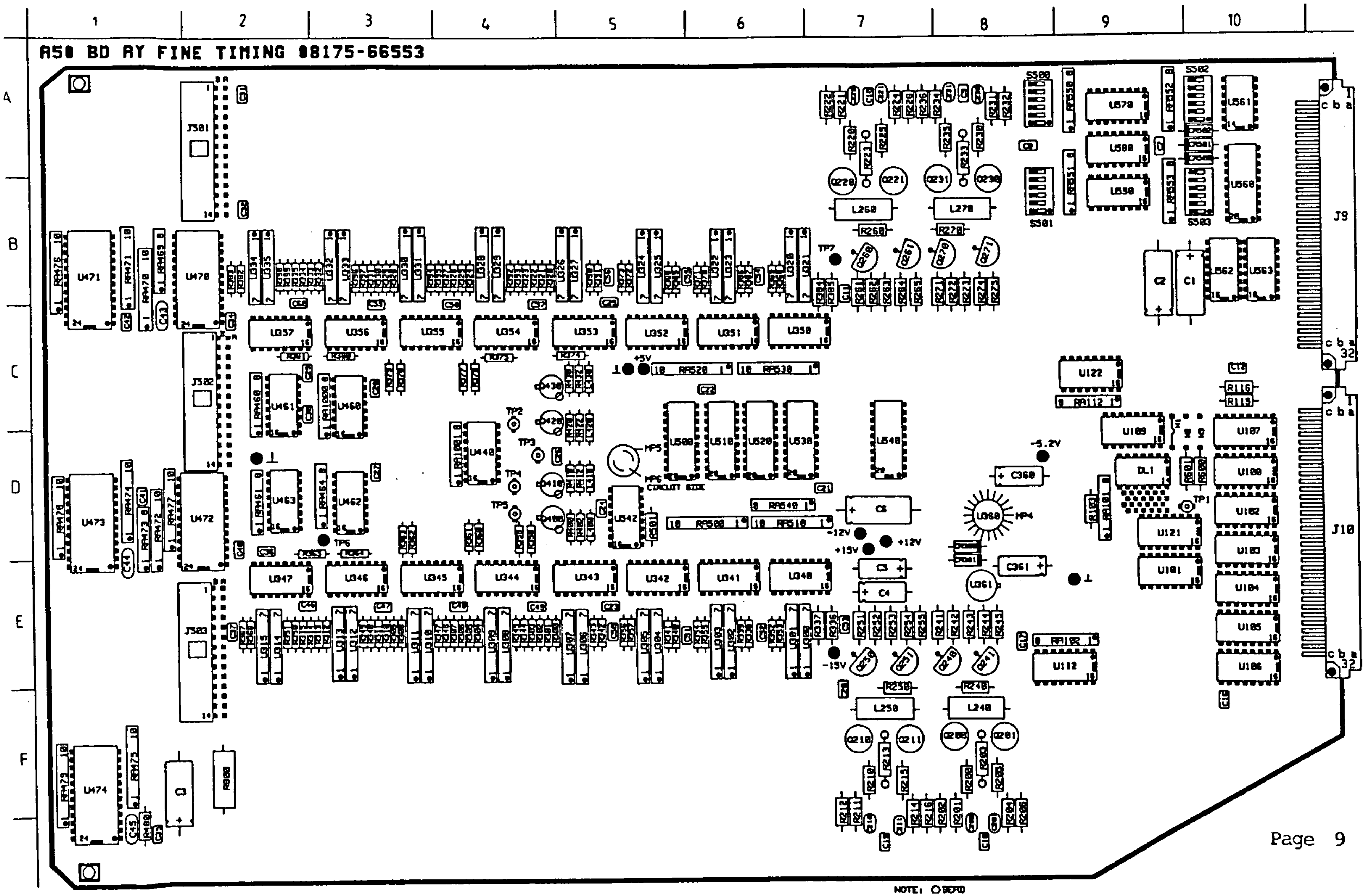
	A50	08175-66553	BD AY TIMING
	A50 C7thru12 C16thru32 C34,35,36 C37,40,41, C42 C46thru60	0160-4835	C-FXD .1Uf 50V
	A50 C44	0160-3456	C-FXD 1000Pf 1000 V
DELETE:	A50 R801		
ADD:	A50 R336 thru R399	0757-0447	R-FXD 12.1K 1%

On Page 8-209, change Schematic 52D as shown:



Change all 32 circuits als shown.

On Page 8-190, change Layout as shown:



MANUAL CHANGE 2

On Page 6-10/11, Replaceable Parts List:

ADD:	A20	R206	0757-0416	R-FXD .511
		R207		
		W1	8159-0005	JUMPERWIRE

DEL:	A20	U312
	A20	U313

On A20 Schematic, Page 8-95 :

ADD: R206 is connected from U209 Pin 16 to +5V

R207 is connected from U209 Pin 7 to +5V

W1 is connected between +5V to Pin 27 of U 106,107,108,109,110,111, 210,211

On Page 6-18, change the Table of Replaceable Parts to read:

A50 C 7,8,12,16,17, C 21,22,24,26, C 27,28,29,30, C 31,32,34,35, C 36,37,40,41,42	0160-4835	C-FXD .1UF 10% 50V
A50 C44	0160-3456	1000 PF 1000 V

DEL: A50 C 9,10,11,18,19, C20,23,25

A50 R 801

A50 C4,5

Delete the same parts on Page 8-178 A50 BD LAYOUT.

On Page 6-11, change the Table of Replaceable Parts to read:

A30 C99	0160-4493	C-FXD 27PF 5% 200V

MANUAL CHANGE 3

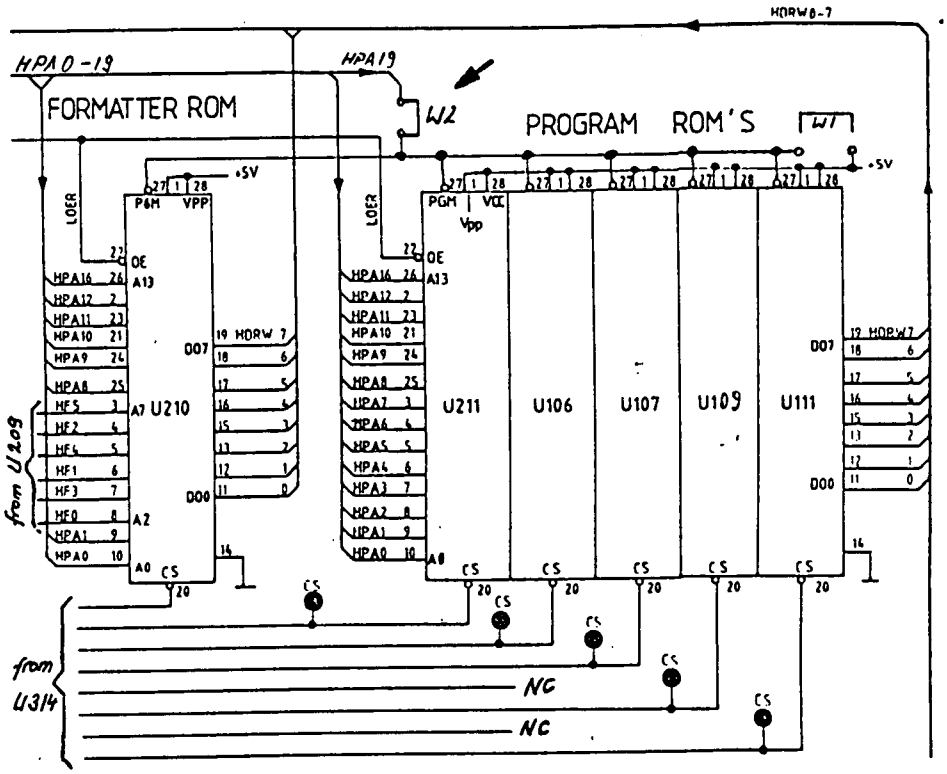
On Page 6-5, change the Table of Replaceable Parts to read:

A20	08175-66524	BD AY CPU BD

On Page 6-10, change the Table of Replaceable Parts to read:

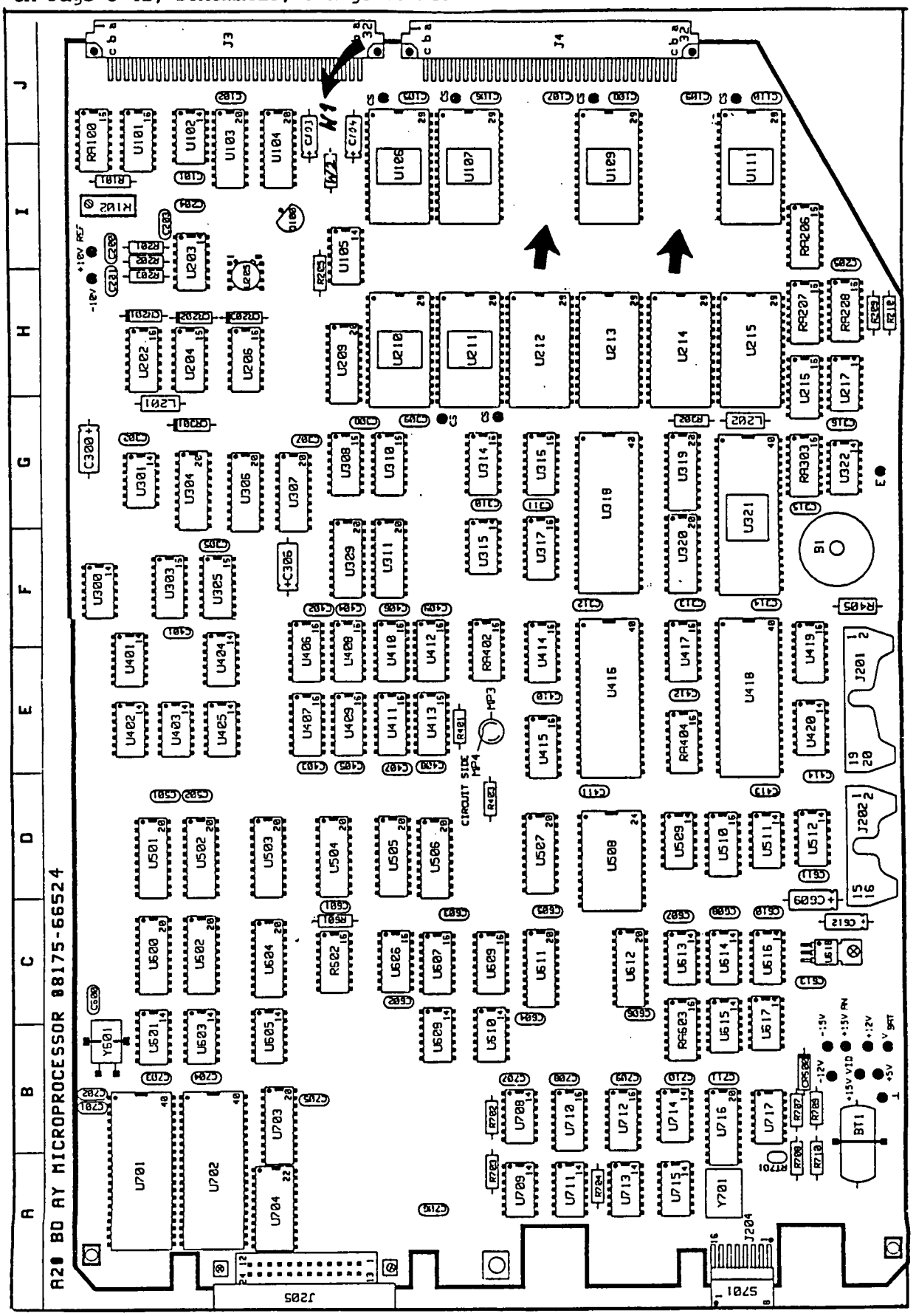
	A20 U210	08175-13710	E-PROM 1
	A20 U211	08175-13711	E-PROM 2
	A20 U106	08175-13712	E-PROM 3
	A20 U107	08175-13713	E-PROM 4
	A20 U109	08175-13715	E-PROM 6
	A20 U111	08175-13717	E-PROM 8
ADD:	A20 W2	8159-0005	JUMPERWIRE
DEL:	A20 W1		
	A20 U108,110		

Change Schematic "B to read (Page 8-95):



MANUAL CHANGE 3 (Cont.)

On Page 8-42, Schematic, change to read:



NOTE: W1 on 08175-66520 BOARD FOR 128K E-PROMS (8times)
W2 on 08175-66524 BOARD FOR 256K E-PROMS (6times)

MANUAL CHANGE 3 (Cont.)

On Page 8-83 step d) ROM S.A. Test change to read:

Set the switch on the "MMU-ET" 08175-66523 as shown
Signature Analyzer settings/Connection points on A20 CPU BD:

START ⌐¬ to TP "CS" (ROM pin 20) of the ROM which will be measured

STOP ⌐/ or ⌐¬ U211 pin 27 (HPA19)

CLOCK ⌐/ U211 pin 22 (LOER)

NOTE: Verify that reading at +5V is 3U9F whith START on "CS" of U210.

Check signatures of ROM's against the following table:

ROM S.A.

IC on Schematic 2B

pin	U210		U211		U106		U107		U109		U111	
	⌐/STOP⌐¬		⌐/STOP⌐¬		⌐/STOP⌐¬		⌐/STOP⌐¬		⌐/STOP⌐¬		⌐/STOP⌐¬	
11	PP3H	4HH6	2P99	C95C	43AU	3H4F	2709	35C5	P427	2U4U	H9H5	A10C
12	26U8	2782	3198	CFH2	7PC9	5P57	5684	7HC9	37UU	6U7H	13UH	18A5
13	2F9P	8413	4UP6	CF19	U82A	AF4P	34C0	67C4	7U9C	4208	8CF5	457P
15	HFFU	F27P	2FH9	FA0U	C282	79AU	45H8	C7HH	20U3	C327	F861	54P6
16	F65C	9HU5	F857	C987	ACA2	1A2A	PAHU	3P1F	6074	70C2	C624	269F
17	0631	FC93	A304	A95A	0F38	3FP0	3PH6	2PF2	5FC0	7CP6	1F67	AC9A
18	P379	052P	AU1H	7H42	3147	F234	1CH4	H229	CH2P	H20H	6298	9291
19	133H	F3C7	3045	C8CU	P30A	367A	9FFC	H46A	A55P	3A90	36UU	405P

MANUAL CHANGE 3 (Cont.)

On Page 6-11, change hte Table of Replaceable Parts to read:

A20	U701	1820-2604	IC 9513

On Page 6-5, change the Table of Replaceable Parts to read:

W10	08175-61620	CABLE AY
W11	08175-61621	CABLE AY

8175A On Page 6-18, change the Table of Replaceable Parts to read:

8175A#001 On Page 6-19, change the Table of Replaceable Parts to read:

A50	R800	0698-3605	R-FXD 120 OHM 5%

MANUAL CHANGE 4

On Page 6-5, change the Table of Replaceable Parts to read:

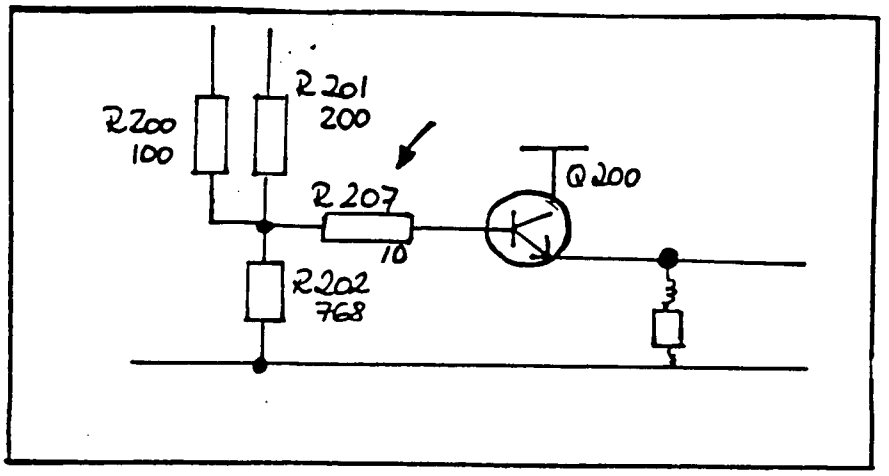
MP11	08175-40203	FRONT PANEL

MANUAL CHANGE 5

On Page 6-19, Replaceable Parts List, add:

A50	R207, R217, R227, R237	0757-0346	R-FXD 10 1% .125W

On Schematic, Page 8-207, add:



MANUAL CHANGE 6

On Page 6-8, change the Table of Replaceable Parts to read:

A10 R29	0698-3518	R-FXD 7.32 KOHM 1%

On Page 6-10, Replaceable Parts List:

Del: A20 R700

MANUAL CHANGE 7

On Page 6-5, change the Table of Replaceable Parts to read:

A2	08175-66504	BD-AY KEY

On Page 6-7, change the Table of Replaceable Parts to read:

A2 W1	08175-61622	CBL AY

MANUAL CHANGE 8

On Page 6-13, change the Table of Replaceable Parts to read:

A30	R120	0698-4409	R-FXD 127 1%
A30	R121	0757-0399	R-FXD 82,5 1%
A30	DL2	1810-0919	Delayline 13ns

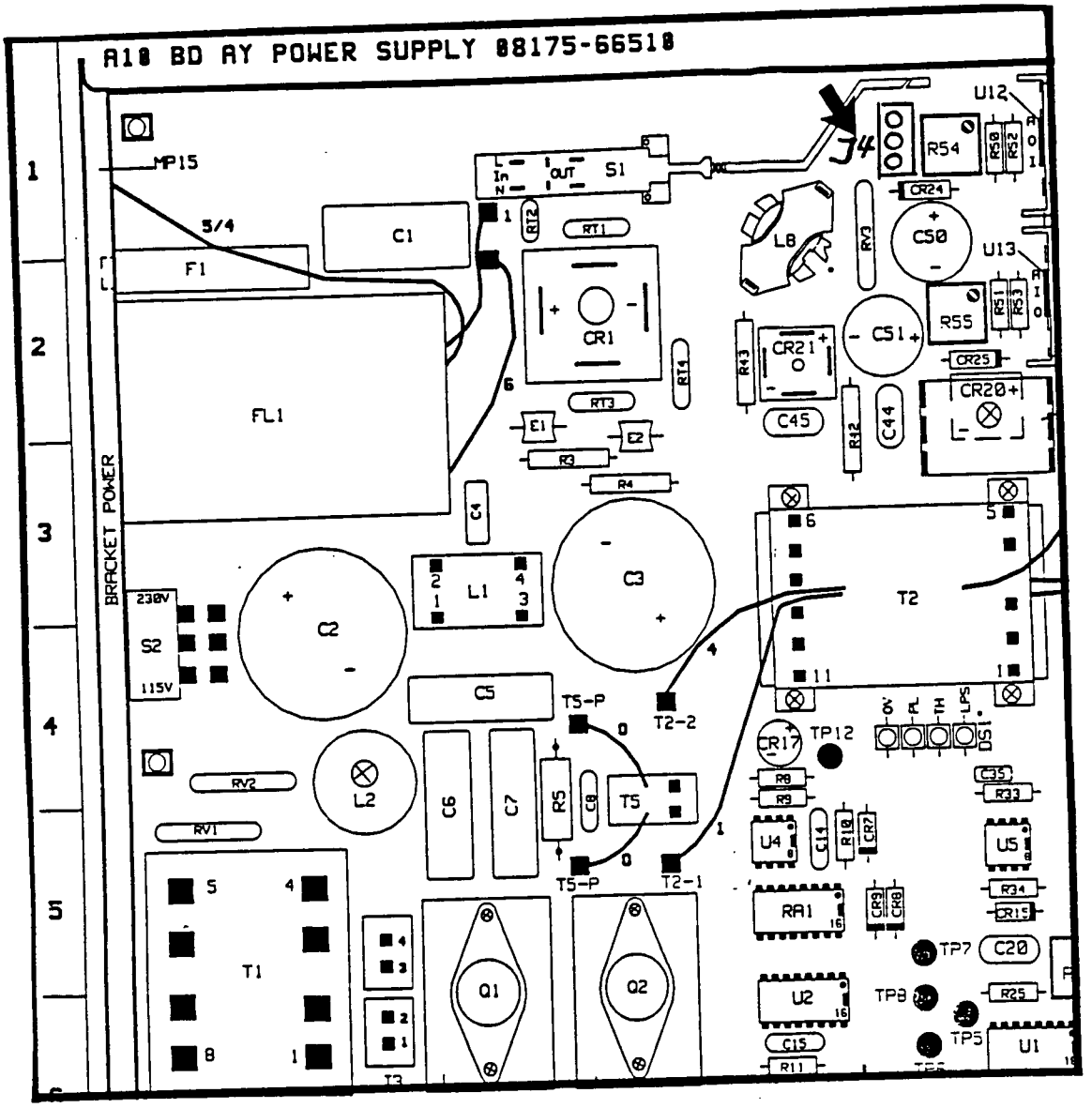
MANUAL CHANGE 9

On Page 6-5, Replaceable Parts List, change to read:

	MP2	08175-00138	BRACKET MIDDLE
	MP12	08175-00638	SHIELD FAN
	B1,2	3160-0510	FAN
ADD:	A10 J4	1251-4246	CONN. 3-PIN (Page 6-8)
	A5	08175-66505	BD AY CONTROL
	A6	08175-66506	BD AY SENSOR

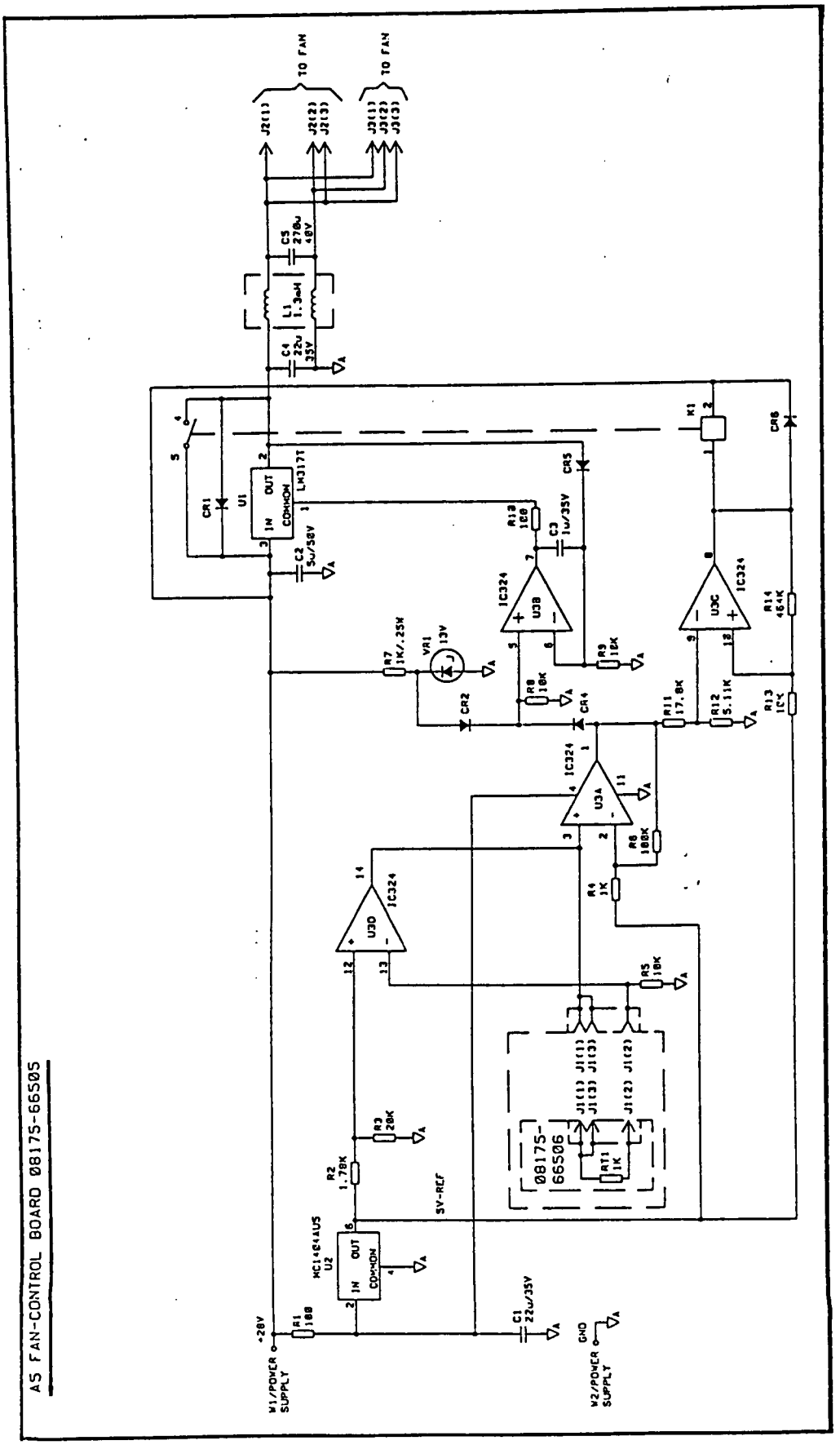
MANUAL CHANGE 9(Cont.)

On Page 8-12, Component Layout, add:

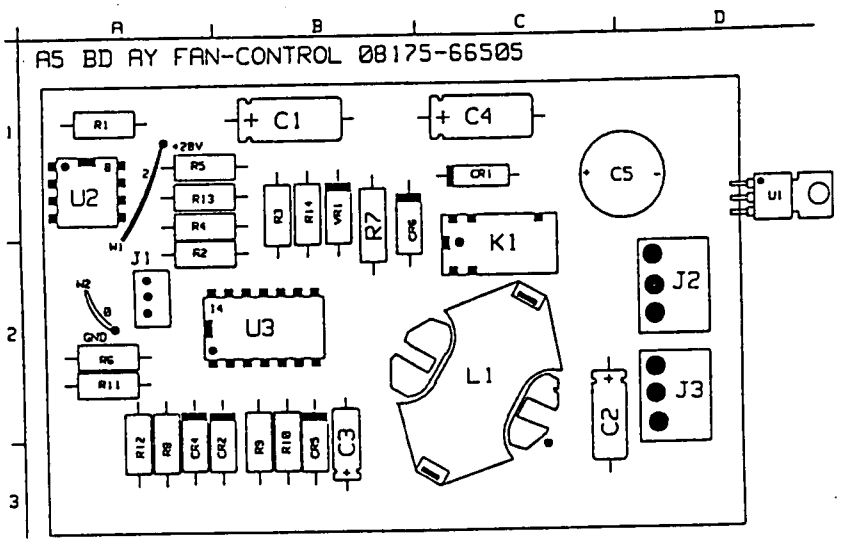


MANUAL CHANGE 9 (Cont.)

ADD: Component Layout & Schematic 08175-66505 & 08175-66506:



MANUAL CHANGE 9 (Cont.)



REF DES	GRID LOC	REF DES	GRID LOC	REF DES	GRID LOC
C1	B1	R1	A1	VR1	B1
C2	D2/3	R2	A2		
C3	B3	R3	B2	W1	A1
C4	C1	R4	A1	W2	A2
C5	D1	R5	A1		
CR1	C1	R6	A2		
CR2	B2/3	R7	B1/2		
CR4	B2/3	R8	A3		
CR5	B2/3	R9	B3		
CR6	B1/2	R10	B3		
J1	A2	R11	A2		
J2	D2	R12	A3		
J3	D2/3	R13	A1		
		R14	B1		
K1	C2				
		U1	D1		
L1	C2	U2	A1		
		U3	B2		

Add:

Repl.-Parts-List

A5 08175-66505 BD AY-CONTROL

REFERENCE DESIGNATOR	C D	H-P PART NUMBER	DESCRIPTION
C 1	3	0180-1794	C-F 22UF 35V
C 2	6	0180-0301	C-F 5UF 50V AL
C 3	3	0160-0291	C-F 1UF 35V
C 4	3	0180-1794	C-F 22UF 35V
C 5	5	0180-0582	C-F 270UF 40V
CR1	8	1901-0732	DIO PWR 1KV 1A
CR2	1	1901-1098	DIO-1N4150 50V
CR4	1	1901-1098	DIO-1N4150 50V
CR5	1	1901-1098	DIO-1N4150 50V
CR6	1	1901-1098	DIO-1N4150 50V
J 1	7	1251-5384	CONN 3-PIN N
J 2	8	1251-4246	CONN-3 PIN
J 3	8	1251-4246	CONN-3 PIN
K 1	1	0490-1232	RELAY 1C 24V
L 1	7	08175-61106	CHOKE 2X1.3mH
R 1	0	0757-0401	R-F 100 1% .125
R 2	9	0757-0278	R-F 1.78K1%
R 3	6	0757-0449	R-F 20K1% .125W
R 4	3	0757-0280	R-F 1K 1% .125W
R 5	9	0757-0442	R-F 10K1% .125W
R 6	6	0757-0465	R-F 100K1% .125
R 7	2	0757-0338	R-F 1K1% .25W F
R 8	9	0757-0442	R-F 10K1% .125W
R 9	9	0757-0442	R-F 10K1% .125W
R 10	0	0757-0401	R-F 100 1% .125
R 11	8	0698-3136	R-F 17.8K1%
R 12	3	0757-0438	R-F 5.11K1%
R 13	9	0757-0442	R-F 10K1% .125W
R 14	9	0698-3260	R-F 464K1% .125
U 1	7	1826-0393	IC LM317T
U 2	0	1826-0718	IC MC1404U5
U 3	7	1826-0161	IC 324
VR1	7	1902-0961	DIODE-ZENER
W 1	8	8150-0449	WIRE 24 RED
W 2	6	8150-0447	WIRE 24 BLK

A6 08175-66506 BD AY-SENSOR

REFERENCE DESIGNATOR	C D	H-P PART NUMBER	DESCRIPTION
J 1	2	1251-5369	CONN-POST-TP-BD
RT1	8	0853-0059	SENSOR-TEMP.
W 1	8	8150-0449	WIRE 24 RED
W 2	6	8150-0447	WIRE 24 BLK

MANUAL CHANGE 10

On Page 6-16/17, change the Table of Replaceable Parts to read:

	A40	U105	1820-0827	IC MC 10161P
	A40	RA24	1810-0713	R-NETWORK
ADD:	A40	R124	0698-7236	R-FXD 1K 1%

A40 BD AY-DATA:

R E V . D (intermediate Sulution)

R124 backloaded to U146 (Pin 8-13)
RA24 Pin 10 connected to U187 Pin24

R E V . E (Final Solution)

R124 located beside U146.

MANUAL CHANGE 11

On Page 6-7, change the Table of Replaceable Parts to read:

A2	S1-39	3101-2947	Keyswitch SPST

On Page 6-8, change the Table of Replaceable Parts to read:

A10	C55	0160-6596	C-FXD .47UF 20%

MANUAL CHANGE 12

On Page 6-5, Replaceable Parts List, change to read:

MP47	3050-0067	WASH BRS.375D

MANUAL CHANGE 13

On Page 6-16, Replaceable Parts List, add:

A40	R125	0757-0421	R-FXD 825 1% .125W

R125 is connected from U109 PIN8 (-5,2V)
to U109 PIN3

MANUAL CHANGE 14

On Page 6-16, change the Table of Replaceable Parts to read:

A40	R25	0757-0280	R-FXD 1K 1%

MANUAL CHANGE 15

On Page 6-10/11, change the Table of Replaceable Parts to read:

A20	U406,407,408, U409,410,411, U412,413	1818-3307	RAM 356 K

WITH 1818-3307 CONNECT PIN 1 and PIN 16 VIA BACKLOADED WIRE.

MANUAL CHANGE 16

On Page 6-5, Replaceable Parts List, change to read:

MP4	08175-04103	CVR TOP CABINET
MP5	08175-04104	CVR BOTTOM CAB.
MP6	08175-04105	CVR SIDE W.HANDLE
MP7	08175-04106	CVR SIDE PERF.
MP60	5001-0540	TRIM STRIP SIDE
MP41	5021-8405	FRAME FRONT 177H
MP48	5041-8801	FOOT
MP59	5041-8802	TRIM STRIP TOP
MP49	5041-8821	PNL REAR STD OFF
MP51	5041-8819	CAP STP HNDL FNT
MP50	5041-8820	CAP STP HNDL RR
MP52	5062-3704	STRAP HNDL 497.8D

MANUAL CHANGE 17

On Page 6-18/6-19, change the Table of Replaceable Parts to read:

	A50	C7,8,12,16,17, C21,22,24,26,27, C28,29,30,31,32, C34,35,36,37,41, C42	0160-6623	C-FXD .10UF 10% 50V
#001:	A50	C7-12,16-32, C34-37,40-42, C46-60	0160-6623	C-FXD .10UF 10% 50V

MANUAL CHANGE 18

On Page 6-5, Replaceable Parts List, change to read:

B1,2	08175-68501	FAN ASSY
W1	08175-61690	WIRE SET

Delete: W2,3,5

On Page 6-8, Replaceable Parts List, change to read:

A10	CR18,19	08175-88704	DIODE KIT

On Page 6-15,16,17,18, Replaceable Parts List, change to read:

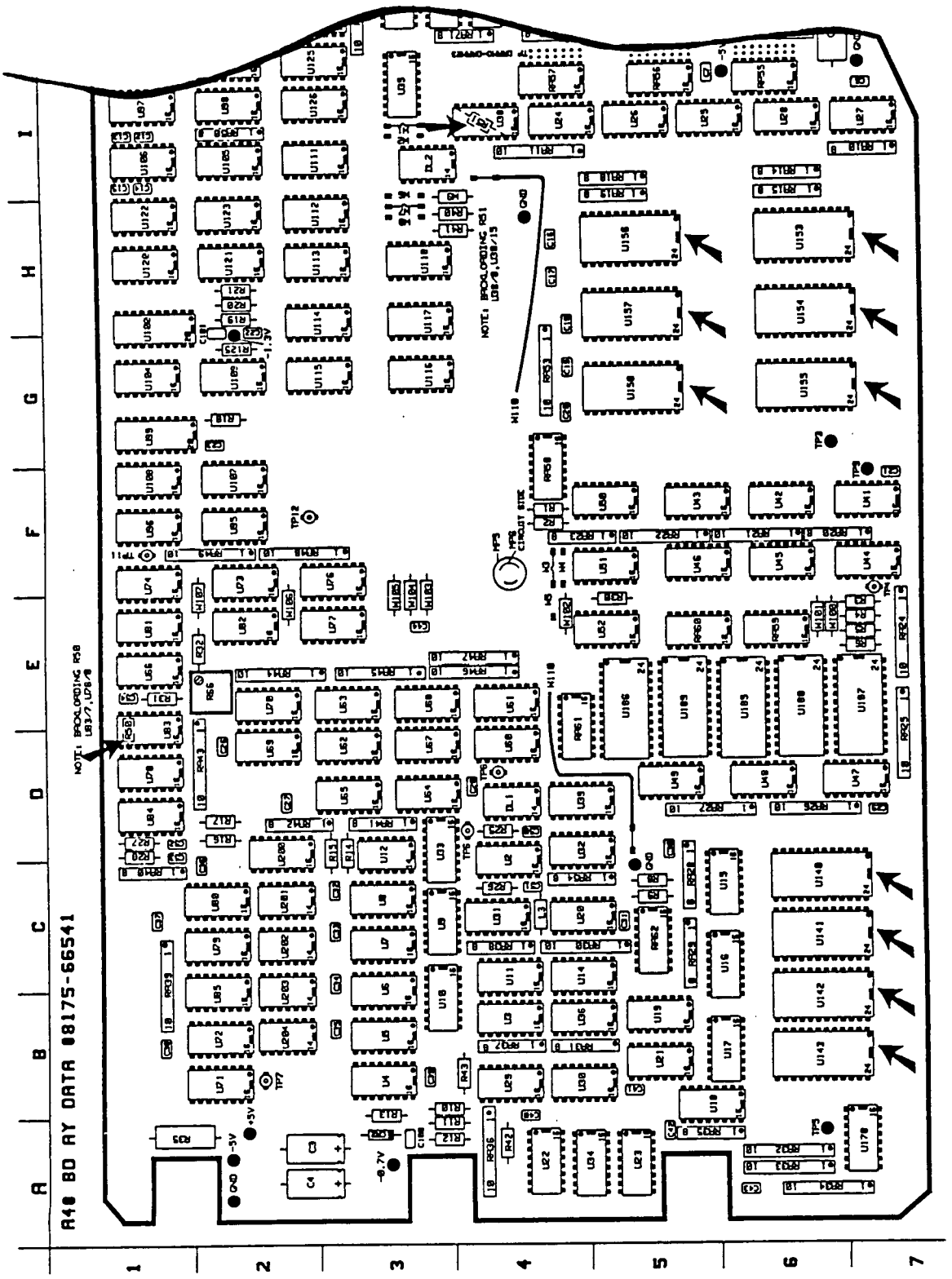
MAINLIST		A40	08175-66541	BD AY DATA
ADD:	A40	R50,51	0698-0082	R-FXD 464 1% .125W
change:	A40	U140-141	1816-1720	IC 10474-7
	A40	U153-158	1816-1721	IC 10474-10
		U142-143	" "	
		BACKLOADING R50	U83/7, U78/8	
		BACKLOADING R51	U38/8, U38/15	

Delete: A40 RA34, R124, RA12,13,16,17,
U159-176
U144-152

COMPONENT- AND SCHEMATIC-CHANGES SEE ON FOLLOWING PAGES!

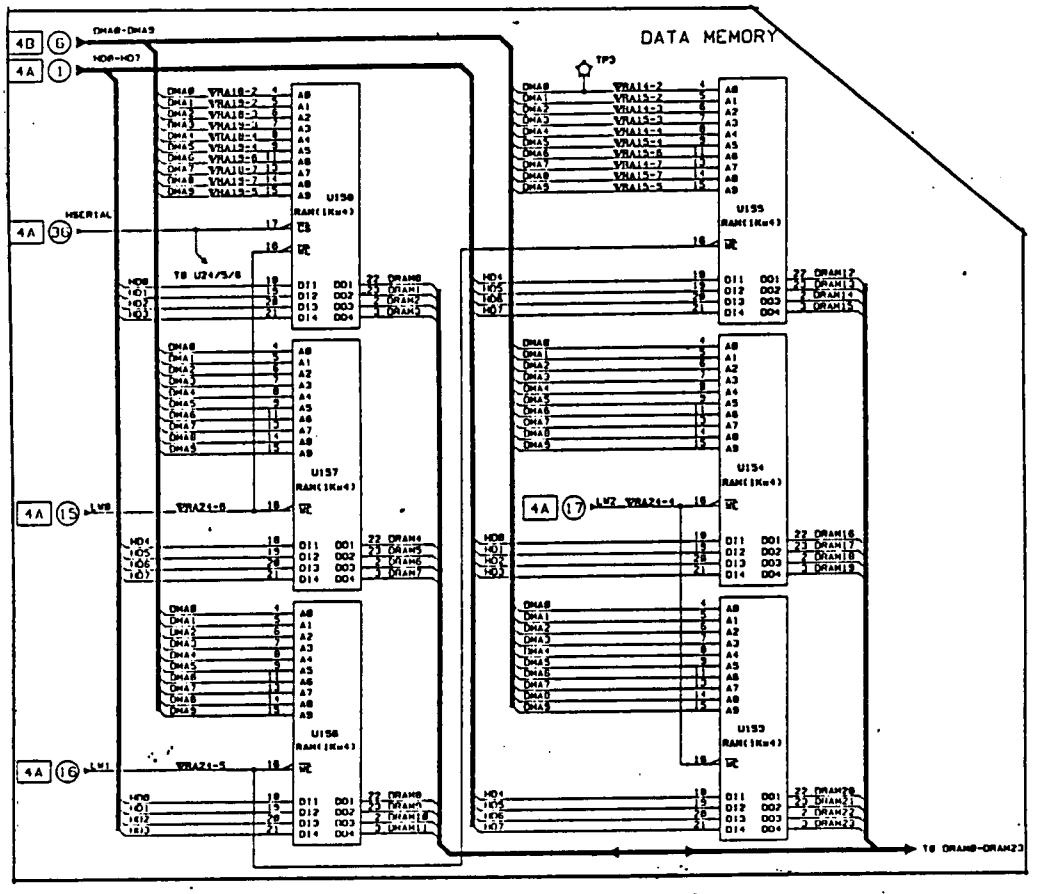
MANUAL CHANGE 18 (Cont.)

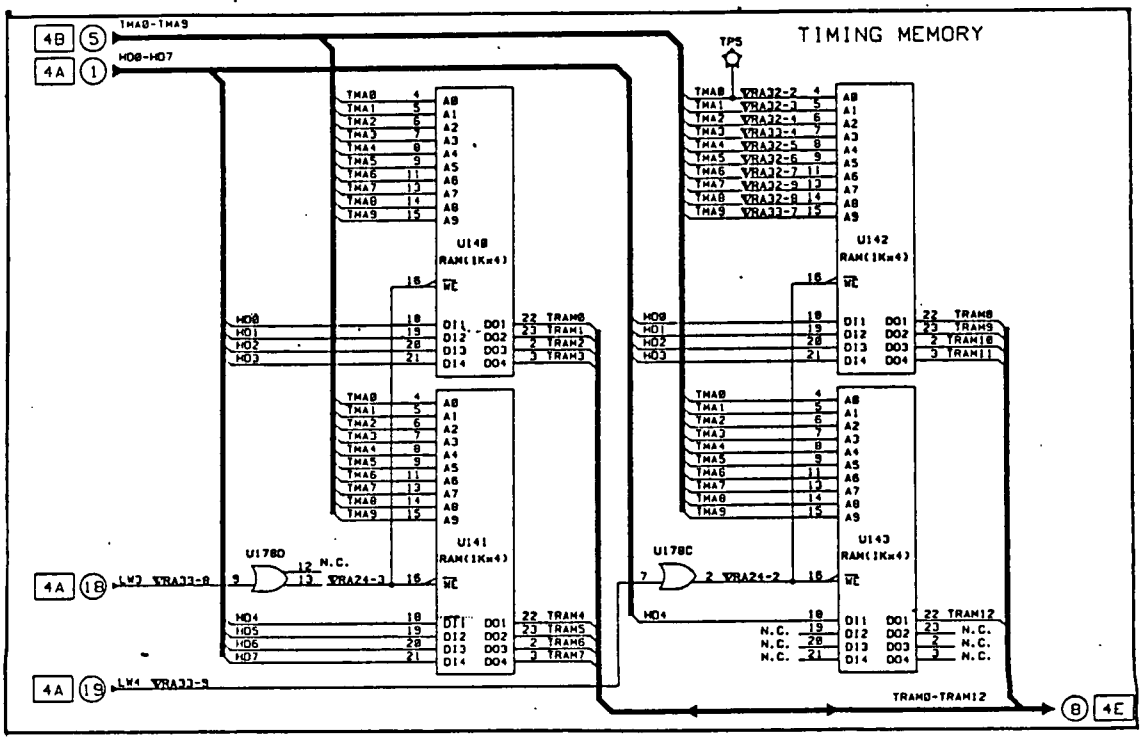
Component Layout, Page 8-142, change to read:



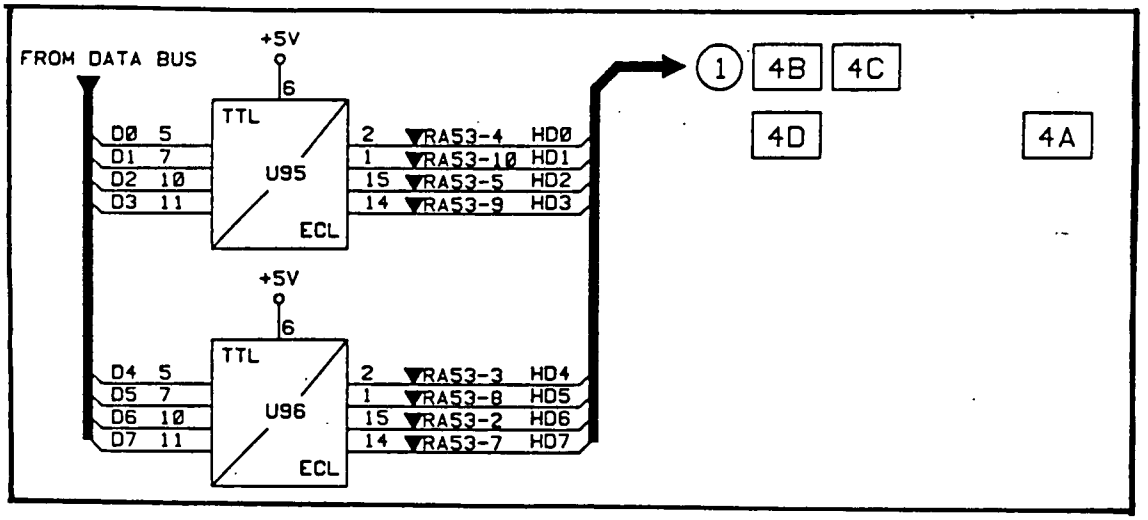
MANUAL CHANGE 18 (Cont.)

Change Schematic to read:





MANUAL CHANGE 18 (Cont.)



Page 8-167

RA	GND PIN	POWER PIN	VOLTAGE LEVEL	RESISTOR VALUE
7	10	1	-5.2V	10PIN160/240
8	10	1	-5.2V	10PIN160/240
9	8	1	-5.2V	10PIN160/240
10	8	1	-5.2V	8PIN160/240
11	10	1	-5.2V	10PIN160/240
14	8	1	-5.2V	8PIN220/330
15	8	1	-5.2V	8PIN220/330
18	8	1	-5.2V	8PIN220/330
19	8	1	-5.2V	8PIN220/330
37	8	1	-5.2V	8PIN160/240
38	8	1	-5.2V	8PIN160/240
71	8	1	-5.2V	8PIN160/240

DELETE RA12, RA13, RA16, RA17

Page 8-173

REF.DES.	-5.2V	+5V	-15V	+15V	GND
U140	12				1,24
U141	12				1,24
U142	12				1,24
U143	12				1,24

DELETE U144-U152

Page 8-171

REF.DES.	-5.2V	+5V	-15V	+15V	GND
U153	12				1,24
U154	12				1,24
U155	12				1,24
U156	12				1,24
U157	12				1,24
U158	12				1,24

DELETE U159-U176

Page 8-173

MANUAL CHANGE 18(Cont.)

Change in Adustment Procedure
MANUAL Page 5-3 Powersupply Board:

TESTCONNECTOR	ADJUST	TEST LIMIT
+5V	R21	+4.98V +/- 50mV
-5.2V	(R21)	-5.27V +/- 70mV

5-8 DATA BOARD:

TP-5V	-5.17V	+/- 70mV
TP+5V	+4.98V	+/- 50mV

MANUAL CHANGE 19

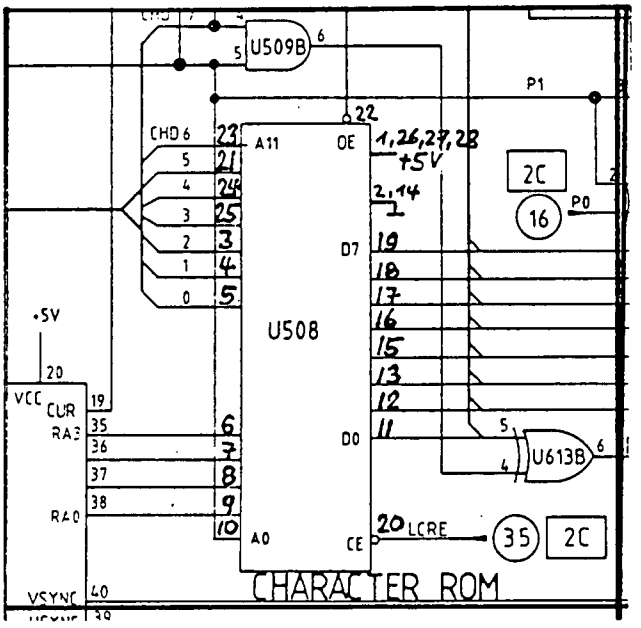
On Page 6-5, Replaceable Parts List, change to read:

A20		08175-66525	BD AY CPU

On Page 6-11, Replaceable Parts List, change to read:

A20	U508	08118-13705	ROM5

On Page 8-99, Schematic, change to read:



MANUAL CHANGE 20

On Page 6-10, Replaceable Parts List,

Delete: A20 MP2

MANUAL CHANGE 21

On Page 6-14, change the Table of Replaceable Parts to read:

A30	U9,10,30,31	1816-1594	IC MBM10422A-7Z
A40	U185,186,187 U188,189	1816-1594	IC MBM10422A-7Z

MANUAL CHANGE 22

On Page 6-8, change the Table of Replaceable Parts to read:

A10	CR5	1901-0731	DIO PWR RECT.

On Page 6-15/16, change the Table of Replaceable Parts to read:

A40	C50	0160-3872	C-FXD 2.2PF 200V
	R25	0698-3488	R-FXD 442 1% .125

MANUAL CHANGE 23

On Page 6-9, change the Table of Replaceable Parts to read:

A10	R29	0757-0440	R-FXD 7,5K 1%
A10	U8	1826-2357	IC TL 780-12CKC

MANUAL CHANGE 24

On Page 6-17, change the Table of Replacealbe Parts to read:

A40	(B-3119)	U140,141	08175-62901	ASSY RAM IC
A40	(B-3119)	U153,154 U155,156, U157,158, U142,143	08175-62902	ASSY RAM IC

MANUAL CHANGE 25

On Page 6-23/24, change the Table of Replaceable Parts to read:

A10	C55	0160-3097	CAP 0.47uF 50V

MANUAL CHANGE 26

On Page 6-5, change the Table of Replaceable Parts to read:

A10		08175-66511	BD AY PWR SPLY

On Page 6-8/9, change the Table of Replaceable parts to read:

		EDC-LBL		
A10	CR1	A-3205	1906-0408	DIO-FW BRDG
	S1		3101-2737	SW-PUSHBUTTO

HEWLETT PACKARD

MANUAL CHANGES

Manual for Model Number	8175A
Manual printed on	October 1986
Manual Part Number	08175-90006

Make all ERRATA corrections.

Check the following table for your instrument serial prefix/serial number and make the listed changes to your manual.

▶ New Item

Serial Prefix or Serial Number	Manual Changes	Serial Prefix or Serial Number	Manual Changes
ERRATA			
CHANGE 1			
CHANGE 2 Started October 1986			

ERRATA

Page 1-0: Figure 1-4, change H.P. Part Number to read: 5061-9678.

Page 3-55: Paragraph headed "**NOTE Single Step**",
delete sentence: "Refer also to _ and "CONT-Mode"".

Page 3-58: Paragraph headed "Address and Program Single-Step from [START]",
delete last two sentences: "A message will _as "**CONT-Mode**" continuous ones".

Page 3-88: Interchange the programs of Examples 1 and 2. Example 1 should include the program currently shown in Example 2 and vice-versa.

Page 3-108: "**QUERY MESSAGES**", last message: "Returns HP 8175A status information", add the command: "BSY?". Note also, that the **COMMAND DETAILS** headers (menom, data etc.) are incorrectly positioned.

Page 3-98: Add the following example (after Example 18):

EXAMPLE OF HOW TO USE SOME LEARN STRING COMMANDS

Example 19

This program example illustates a method (using Basic 2.0 with Basic Extension 2.1) of sending Learn String commands. The example uses the commands "SET?" and "SET" which enable return and acceptance respectively, of the whole Parameter set. (See page 3-109 for list of commands.) The same program example can easily be modified (by changing the commands within lines 30 and 40), to enable any other Learn String commands to be used. Note how in this example, the location (LOC) is set to 0, this defines the parameter set as the actual (displayed) one.

As can be seen, the program involves the use of ASSIGN and TRANSFER statements etc. Specific explanations concerning the significance of these is outside the scope of this manual. Therefore, if you wish to develop your own programs, you should refer to a Basic Programming Techniques manual or similar publication for more information.

```
10    DIM A$[5],B$[8],V$[10600] BUFFER
20    ASSIGN @Hpib_device TO 720
30    A$="SET? 0"
40    B$="SET 0,"
50    ASSIGN @Path TO BUFFER V$
60    OUTPUT @Path;B$;END
70    OUTPUT @Hpib_device;A$
80    TRANSFER @Hpib_device TO @Path;END
90    WAIT FOR EOT @Hpib_device
100   STATUS @Path,4;Count_out
110   PAUSE
120   TRANSFER @Path TO @Hpib_device;COUNT Count_out
130   END
```

ERRATA (Cont.)

Page B-2: Add the following note below step (11):
"Note: If wished, a print can also be stopped via the label "PSTOP". To use this capability, simply include the label at the appropriate address location on the (Pattern) Setup menu. This will then be the last line printed.

Page 3-71,72: For the STORE and (COPY channel) examples, the "After EXEC" display details should be interchanged.

Page 3-101: Bottom part of page, "Flag Mode" should read "Latched Flag Mode". Also, mnemonic details etc. for same are shown incorrectly positioned.
Add the command "Static Flag Mode ...FLM...2" after the Latched Flag Mode details.

Page 3-103: Bottom of page under Comments, "HLP" should be changed to "HILP".

Page 4-26: Step (2), in text and Table 4-12, change "800 mV" to read "600 mV".

Page 1-4: Table 1-1, Torque indicating screwdriver, change 8830-0013 to 8710-0902.

Page 1-5 : Table 1-2 Specifications
Top right hand paragraph: CLOCK
Change the NOTE to read:

Note: For ECL and TTL POD only and Pattern Duration ≥ 20 ns:
In serial mode an additional Serial Clock is available on pod 0, channel 1 providing a pulse at every bit.

Page 3-46: Add the above NOTE at bottom of Page, Serial Data Generation Configuration.

Page 4-9: Add the above NOTE to step 4-12A Specification.

Page 4-9/4-11/ and 4-13: Test set up:

Exchange the 15462A Pod connected to the Flag Pod Output A30J306 by 15461A/15464A.

Page 3-27: Printer HP-IB adress:

This defaults to 01, however it can be manually set to any number between 00 and 09 if no other instrument is assigned to that adress.

ERRATA (Cont.)

ADD: Page 1-6: Table 1-2 Specifications

HP 15462A TTL/CMOS POD

change to read:

TRANSITION TIMES

*into open: ≤ 3ns + high level x 1,4ns/V

into 50 pF: ≤ 9ns + high level x 1,8ns/V

*NOTE: into open means into 3pF/1M ohm

Page 4-21: Table 4-10, change to read:

15462A

into open

<= 3ns

+ high level x 1.4ns

Page 4-23: Table 4-11, change to read:

8175A TTL/CMOS HIGH LEVEL	15462A
+ 2.4V	6.36ns
+ 5.0V	10.0 ns
+ 9.9V	16.86ns

Page 4-4 and Page 4-9: 4-11 PATTERN DURATION WITH INTERNAL CLOCK

4-12 CLOCK TEST

In step Specification, change the accuracy to read:

Accuracy: ±0.05% of progr. value ±2.5 ns (asynchronous start)
±0.5% of progr. value ±2.5 ns (synchr. start, clock cal.)
±3% of progr. value ±2.5 ns (synchr. start, no clock cal.)

ERRATA (Cont.)

Page 4-5, Table 4-1 change to read:

	Counter Reading	
Period	low limit	high limit
0.05µs	47.475ns	52.252ns
0.09µs	87.455ns	92.545ns
0.10µs	97.455ns	102.55ns
0.5µs	497.25ns	502.75ns
0.9µs	897.05ns	902.95ns
1.00µs	997.0ns	1.003 µs
5.00µs	4.9945µs	5.0045µs
9.00µs	8.9925µs	9.0075µs
.....	.....	.....
.....	.....	.....
1.00s	999.5ms	1.0005s
9.99s	.....	.....

Page 4-6, Table 4-2 change to read:

Period	Counter Reading	
	low limit	high limit
0.10 us	94.5 ns	105.50 ns
1 us	967.5 ns	1.0325 us
9.00 us	8.7275ns	9.2725 us
100 us	97 us	103 us
900 us	873 us	927 us
10 ms	9.7 ms	10.3 us
1 s	970 ms	1.03 s

Page 4-6, Table 4-3 change to read:

Period	Counter Reading	
	low limit	high limit
0.10 us	97.0 ns	103.0 ns
1 us	992.5 ns	1.0075us
9.00 us	8.9525us	9.0475us
100 us	99.5 us	100.5 us
900 us	895.5 us	904.5 us
10 ms	9.95 ms	10.05 ms
1 s	995 ms	1.005 s

ERRATA (Cont.)

Page 4-7 Table 4-4, change to read:

Period	Counter Reading					
	low	high	low	high	low	high
.10µs	97.455ns	102.55ns	94.5ns	105.5ns	97.0ns	103.0ns
.02µs	17.49ns	22.51ns	16.9ns	23.1ns	17.4ns	22.6ns
*.01µs	7.495ns	12.505ns	7.20ns	12.8ns	7.45ns	12.55ns
	auto-cycle asynchr.start		auto-cycle synchr.start		auto-cycle synchr. start with clockcal.	

Page 4-10 Table 4-6, change to read:

Period of clock	auto-cycle asynchron		auto-cycle synchron		auto-cycle synchron startable clockcal.	
	Counter Reading					
	low	high	low	high	low	high
* .10µs	97.455ns	102.55us	94.5ns	105.50ns	97.0ns	103.0ns
1.00µs	997.0ns	1.003µs	967.5ns	1.0325µs	992.5ns	1.0075µs
9.00µs	8.9925µs	9.0075µs	8.7275µs	9.2725µs	8.9525µs	9.0475
**	----	----	----	----	----	----

Do the same changes to the

PERFORMANCE TEST RECORD

On Page 4-35 Test Number 4-11A Step 2, Step 3
On Page 4-35 Step 4.

ERRATA (Cont.)

Add to Page 4-1:

In the following tests change on 8175A OUTPUT Page the TTL/ CMOS-POD High Level to +5.0V and the TRIG LVL A of Counter to + 2.5V. If the ECL POD 15461A is used change the TRIG LVL of Counter to - 1.3V.

Page 4-8: Add after step 8 the following instruction:
"After each new Period setting press "Stop - Update - Start."
Delete in the Period header of Table 4-5: "Press START..SETTING)

Page 4-20: change in Table 4-9 the low level limit of 15462A Pod to < = 0.7V.

Page 4-32: Test E.Pod Input Threshold, change details to read as follows:

Min. Overdrive 250mV or 30% of input amplitude,...

In Step 7, change to read:

Set 8112A: HIL -0.4V LOL -0.7V.

Page 4-35: Step 2, change values to read as shown:

10ms	9.995ms
1.00s	999.5ms
9.99s	

In Step 3, change values to read as shown:

10ms 9.7ms 10.3ms

Page 4-39: 4-12B Steps 4 and 6, change Period of Clock values to read as shown:

2 x 1 200ns 200ns

ERRATA (Cont.)

On page 4-1 add:

General Points

Before starting with the **Performance Tests** get familiarized with the curser driven concept of the HP 8175A. Therefore, the **Operation** part of this Manual should be read and understood.

Each new paragraph of the Performance Tests begins with a set of known parameter values and operating conditions etc. The **Standard Settings** provide the ideal starting values. Therefore you should start by recalling them.

NOTE: When the Standard Settings are recalled, **all data is set to 0!**

How to Recall the Standard Settings

The Standard Settings are accessed via the System Page.

1. Press the SYSTEM key. This selects the System Page.
2. Press the NEXT[] key more times, until the *[Storage]* menu is displayed. (Pressing the PREV[] key once does the same.)
3. Press the CURSOR↓ key once. This positions the cursor in the *[store]* function field.
4. Press NEXT[] key until *[recall] Standard Settigns* is displayed in this function field.
5. Press EXEC key, this activates the function. The message 'Transfer in Process' will be displayed very briefly. When this message is replaced by the original one, 'Press EXEC to Activate Function', you can continue.

Below it's shown as it is written in the Performance Tests:

SYSTEM > NEXT = [Storage] > CURSOR↓ = [store] > NEXT = [recall] Standard Settings > EXEC

As you can see:

SYSTEM, NEXT, CURSOR↓ , EXEC	shows what you have to KEY in (front panel keys).
>	leads to that KEY you have to press next, once or more times (e.g. 4x).
=	shows what happens if you press this KEY, or what should be displayed, or where the highlighted blinking cursor should be placed.

All the other HP 8175A settings throughout the complete Performance Tests are shown in the same way!

ERRATA (Cont.)

On page 4-3 step 4. change to read:

Set 8175A:

SYSTEM > CURSOR↑ = Parallel Data Generator >
DATA > NEXT > CURSOR↓ = Address 1023 > ROLL↑ = Address 0000 >
blue > CURSOR→ 4x = POD0 CH7 > 01010101 >
(Address 0001) 10101010 10101010 10101010 >
blue > TIMING = COPY , [Copy Address] from > CURSOR→ > DON'T CARE > 0000 >
DON'T CARE > 0001 > DON'T CARE > 0002 > EXEC >
blue > TIMING = COPY , [Copy Address] from > CURSOR→ > DON'T CARE > 0000 >
DON'T CARE > 0003 > DON'T CARE > 0004 > EXEC >
blue > TIMING = COPY , [Copy Address] from > CURSOR→ > DON'T CARE > 0000 >
DON'T CARE > 0007 > DON'T CARE > 0008 > EXEC >
blue > TIMING = COPY , [Copy Address] from > CURSOR→ > DON'T CARE > 0000 >
DON'T CARE > 0015 > DON'T CARE > 0016 > EXEC >
blue > TIMING = COPY , [Copy Address] from > CURSOR→ > DON'T CARE > 0000 >
DON'T CARE > 0031 > DON'T CARE > 0032 > EXEC >
blue > TIMING = COPY , [Copy Address] from > CURSOR→ > DON'T CARE > 0000 >
DON'T CARE > 0063 > DON'T CARE > 0064 > EXEC >
blue > TIMING = COPY , [Copy Address] from > CURSOR→ > DON'T CARE > 0000 >
DON'T CARE > 0127 > DON'T CARE > 0128 > EXEC >
blue > TIMING = COPY , [Copy Address] from > CURSOR→ > DON'T CARE > 0000 >
DON'T CARE > 0255 > DON'T CARE > 0256 > EXEC >
blue > TIMING = COPY , [Copy Address] from > CURSOR→ > DON'T CARE > 0000 >
DON'T CARE > 0511 > DON'T CARE > 0512 > EXEC >
blue > EXEC = UPDATE > START

ERRATA (Cont.)

Page 3-108 "QUERY MESSAGES", last message: "Returns HP 8175A status information", add the command "BSY?".Note also that the COMMAND DETAILS headers (mnem, data, Unit, ref.) are incorectly positioned.

Add the following example after the Comments: C4

```
10   !Announcing the BSY? command. Lets you look
20   !up where the HP8175A has stopped.
30   !
40   OUTPUT 720; "CYM;SA"
50   OUTPUT 720; "BSY?"
60   ENTER 720;B$
70   PRINT "BSY STRING = ",B$
80   IF VAL(B$)=1 THEN
90      PRINT "8175A IS RUNNING"
100  ELSE
110     PRINT USING "K";"8175A HALTED AT ADDRESS ",B$(3,6)
120     PRINT USING "K";"      AT MEMORY SEGMENT ",B$(8,10)
130  END IF
140  PRINT
150  PRINT "PRESS CONTINUE TO STOP  8175A"
160  PAUSE
170  OUTPUT 720; "ST"
180  OUTPUT 720; "BSY?"
190  ENTER 720; B$
200  PRINT
210  PRINT "BSY STRING =", B$
220  IF VAL (B$)=1 THEN
230     PRINT "8175A IS RUNNING"
240  ELSE
250     PRINT USING "K";"8175A HALTED AT ADDRESS",B$ (3,6)
260     PRINT USING "K";       AT MEMORY SEGMENT",B$ (8,10)
270  END IF
280  LOCAL 720
290  END


BSY STRING =       1
8175A IS RUNNING

PRESS CONTINUE TO STOP 8175A

BSY STRING =        0,0064,006
8175A HALTED AT ADDRESS 0064
      AT MEMORY SEGMENT 006
```

ERRATA (Cont.)

On Page 1-0 (8175A Accessories) change to read:

10230-62101 change to read: 5959-0288 probe tip, 1 ea
(20 necessary per POD).

On Page 1-7, General, add the following text:

Acoustic Noise Emission:

For ambient temperature upto 23° C
LpA= 42 dB
Typical operator position,
normal operation.

Data are results from type tests per ISO 6081.

Geräuschemissionswerte:

Bei einer Umgebungstemperatur bis 23° C
LpA= 42 dB
am Arbeitsplatz,
normaler Betrieb.

Angabe ist das Ergebnis einer
Typprüfung nach DIN 45635 Teil 19.

CHANGE 1

Add: to Table 1-2 Specifications

HP 15464A TTL POD

(DATA OR FLAG OUTPUT POD)

NO. OF CHANNELS:	8
MAX. BIT RATE PER CHANNEL:	50 Mbit/s NRZ
HIGH LEVEL (into open):	5 V ± 5%
LOW LEVEL(into open):	≤0.7 V
TRANSITION TIMES	
into open:	≤ 6 ns
into 50 pF:	≤12 ns
FAN OUT PER CHANNEL:	15 LS TTL
OVERSHOOT, RINGING (into open):	≤ 20% of amplitude
MAX. EXTERNAL VOLTAGE AT INPUT AND OUTPUTS:	-3 V/ +8 V
DISABLE / ENABLE CHARACTERISTICS (TRI-STATE)	
T(ON), T(OFF):	≤50 ns
LEAKAGE CURRENT:	≤10 µA
RESIDUAL CAPACITANCE (typical):	≤50 pF
TRI-STATE INPUT at the output pod (TRIST)	
IMPEDANCE (typical):	10 kOhm/ 40 pF
THRESHOLD:	1.8 V
Min. overdrive:	150 mV

Add to CHAPTER 4 PERFORMANCE TEST

Page 4-1 add below step 4-9:

NOTE: In the follwoing tests the TTL/CMOS Pod HP 15462A can be replaced by TTL Pod HP 15464A.

For the following tests do the special changes:

Page 4-16 Para 4-14 SKEW
add to the Specification:

TTL Pod : < = 7ns; typical < = 5 ns

Page 4-17 step 2:

change TTL Pod < =7ns; typical < = 3ns
to: TTL/CMOS Pod < =7ns; typical < = 3ns

add: TTL Pod < =7ns; typical < = 5ns

CHANGE 1 (CONT.)

Page 4-20 Para 4-16 Level Test

add to Specification:

HP 15464A

High Level: +5V

Low Level : $\leq$ 700 mV

Accuracy : $\pm$ 5%

add to table 4-9

	High Level low limit	High Level high limit	Low Level
15464A	+4.75V	+5.25V	< = 0.7V

Page 4-21 Para 4-17 transition times

add to Specification

	15464A	
TT 10% - 90%	into open < = 6ns	into 50pF $\leq$ 12ns
Overshoot ringing	20% of amplitude into open	

Page 4-23 add to Table 4-11

15464A
< = 6ns

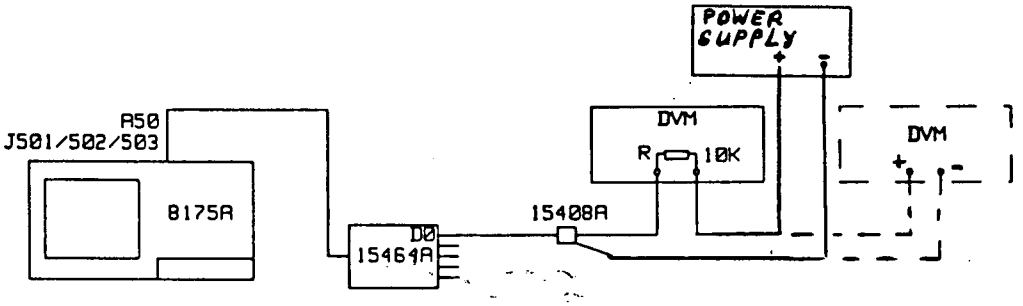
step 5. Measure transition times of all data channels of 15464A Pod for $\leq$ 12ns.

CHANGE 1 (Cont.)

Page 4-24 Para 4-18 TTL Leakage Current
changes Specification as follows:

	15462A	15464A
Leakage Current	$\leq$ 20µA	$\leq$10µA

Test set up for 15464A Pod



add to step 1: Set the external Power Supply
to +5.000V.

add to step 2: For 15464A Pod

I LEAKAGE = measured voltage/10 k $\leq$ 10µA

Page 4-25 Para 4-19 TRIST T (ON) , T (OFF)
add to Specification

Pod 15464A $\leq$ 50ns

CHANGE 1 (Cont.)

Page 4-26 step 1 in the figure add:

→ T ON ←	→ T OFF ←
15462A $\leq$ 30ns	$\leq$ 30ns
15464A $\leq$ 50ns	$\leq$ 50ns

step 2 Table 4-12 add

TTL Pod	+ 1.8V $\pm$ 150mV

C H A N G E 2

Page 1-3 Para 1-6 OPTIONS

Delete: D04 Deletes Standard Pod set (order PODs separately)

Add: 002 Dual Arbitrary Waveform Generator (O/P/S Manual 08175-90011)

003 ECL POD SET (includes 4 ea 15461A ECL POD's
1 15463A TRIGGER POD)

004 TTL POD SET (includes 4 ea 15464A TTL POD's
1 15463A TRIGGER POD)

005 TTL/CMOS POD SET (includes 4 ea 15462A TTL/CMOS POD's
1 15463A TRIGGER POD)

Para 1-7 ACCESSORIES SUPPLIED

Delete: 4 each HP 15462 TTL/CMOS POD's

1 HP 15463A TRIGGER POD

Para 1-8 ACCESSORIES AVAILABLE

PODS

Add: HP 15464A TTL POD(fixed TTL Level, includes 1 HP15429A)

On Page 1-0, delete in Figure 1-1:

Accessories 4x 15462A

1x 15463A

PRODUCT SUPPORT PLAN

FOR INTERNAL USE ONLY

Date: May 1986
Supersedes :
FINAL PSP
May 1985
Preliminary PSP
Dec 1985

To: PT01 INSTRUMENT SALES AND SERVICE OFFICES

From: BOEBLINGEN INSTRUMENT DIVISION (BI)
BOEBLINGEN, FEDERAL REPUBLIC OF GERMANY

Subject: **HP 8175A DIGITAL SIGNAL GENERATOR**

OPTION 001
Fine Timing

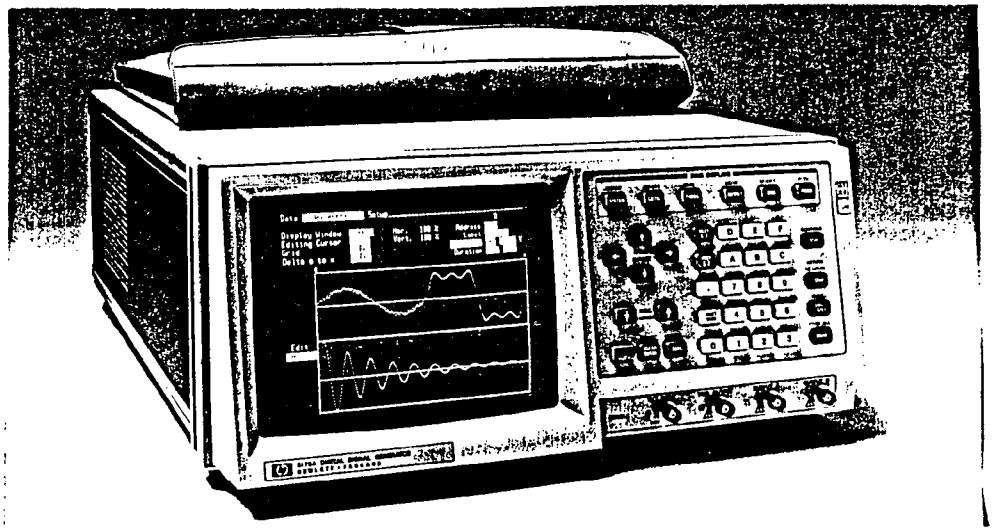
OPTION 002
Dual Arbitrary Waveform Generator

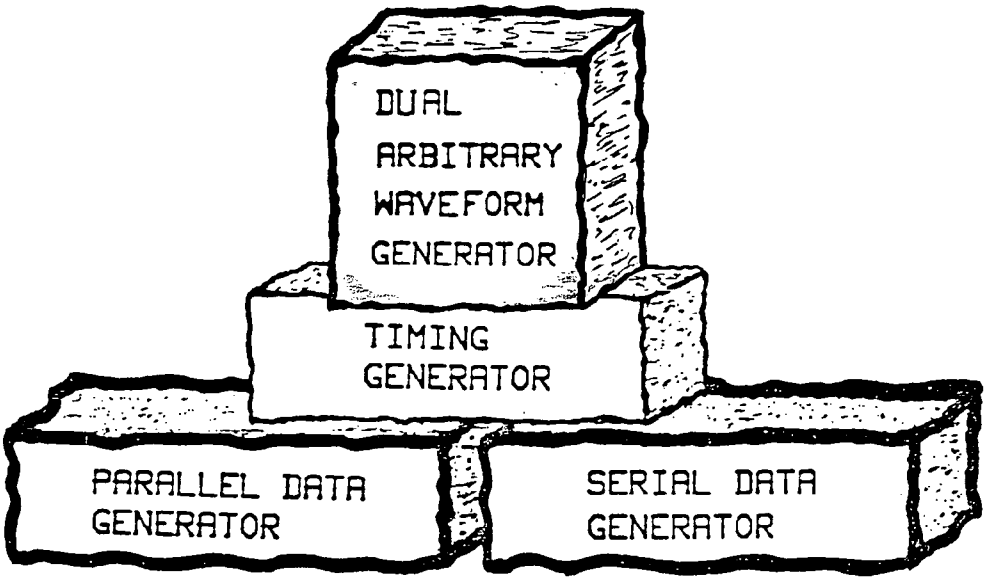
Manfred Illenseer/ir

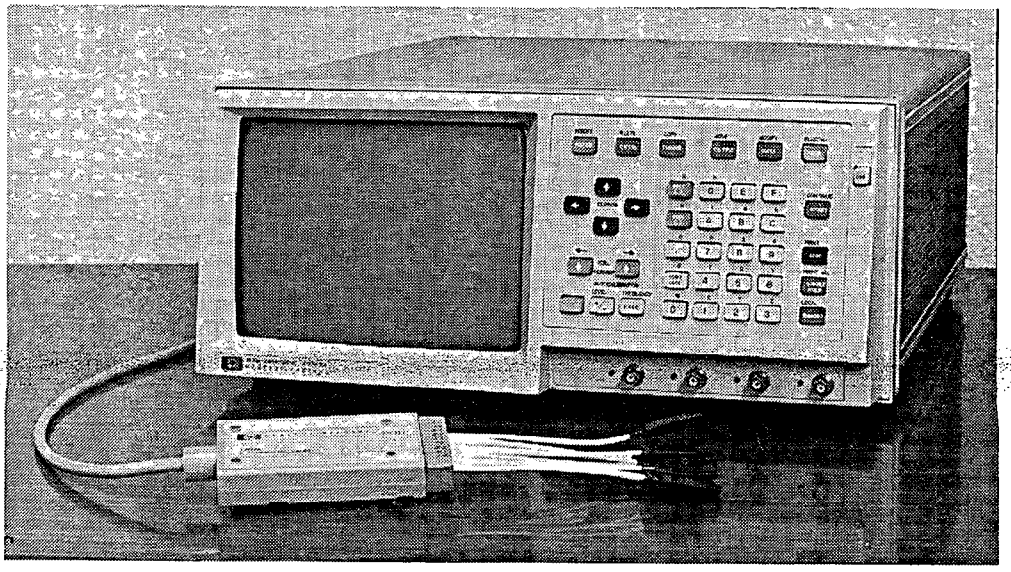
HEWLETT PACKARD

HEWLETT PACKARD — 8175A — BID

DIGITAL SIGNAL GENERATOR







HP 8175A DIGITAL SIGNAL GENERATOR

OPTION 001 / 002

PRODUCT SUPPORT PLAN

Contents

8175A DIGITAL SIGNAL GENERATOR and OPTION 001

1. General Description

The HP 8175A is a very flexible, fully HP-IB programmable DIGITAL SIGNAL GENERATOR. In contrast to the DICE market (ac parametric characterization of digital IC's and boards), the HP 8175A aims at our traditional, more diverse data/word generator areas.
The major area here is the simulation of signals of missing boards so that parts of complex systems can be functionally tested, at-speed and under real timing and level conditions. The 8175A's high speed, variable pattern duration and intelligent cycling capability now gives us the competitive edge to succeed in engineering bench and in HP-IB based ATE applications.

The HP 8175A DIGITAL SIGNAL GENERATOR is a universal stimulus capable of delivering the broad diversity of signals required in digital tests and measurements. This variety in signal type covers complex digital bit patterns and sophisticated pulse traces.
Actually the **HP 8175A** with **OPT 001** incorporates the stimulus capabilities of two types of generators:

* a Digital Pattern Generator with serial and parallel format

* a Digital Timing Generator with variable duration and delay (OPT 001)

The HP 1630x family of LOGIC ANALYZERs will be the best receiving end for the HP 8175A DIGITAL SIGNAL GENERATOR .

Product Description

HP 8175A DIGITAL SIGNAL GENERATOR, a stimulus for the

Traditional Data Generator Market.

Selectable modes give 24 x 1 kbit channels at 50 Mbit/s NRZ for multichannel-needs or two 8 kbit serial channels at NRZ data rates up to 100 Mbit/s. Even longer data sequences can be achieved by using the 8175A's program memory. This allows up to 255 pre-selectable data memory cycles to be sequenced as wished during data generation. By using this feature, looping and branching are possible. Also the data memory is cross-referenced to a timing memory with 10 ns resolution which determines the timely duration of every data pattern. These powerful features are augmented by interactive capability for instrument status control (START/STOP/3-State etc. via 8 bit programmable input register), for branching to other datacycles and/or for setting 8 programmable output flags on receipt of a DUT's or other request.

Where the standard 10 ns timing resolution is insufficient, a **Fine Timing Option 001** adds 20 ns to 40 ns delay with 100 ps resolution on 4 channels. This ensures very tight timing adjustments e.g. for clocking and strobe signals.

HP 8175A OPTION 002

DUAL ARBITRARY WAVEFORM GENERATOR

1.1 General Description

The DUAL ARBITRARY WAVEFORM GENERATOR (HP 8175A OPTION 002) is a universal stimulus which takes us into areas like simulation of "real-life" signals required in analog tests and measurements, e.g. in bio-medical or mechanical investigation, simulation of floppy-disc or tape head signals, or simulation of telecom modules and many others.
A 50MHz DAC with 1024 amplitude steps together with all the Data Generator's intelligent cycling features makes virtually any waveform possible.
With the HP 8175A Opt. 002 two different analog output signals are available with an amplitude of up to 16V peak-to-peak (32Vpp into open).
The extensive hardware capabilities are governed by a friendly user interface which, for the first time, takes the burden of setting up an arbitrary waveform from the operator.

The **HP 8175A** with **OPT 001** and **OPT 002** actually incorporates the stimulus capabilities of several types of generators in ONE instrument:

* Digital Pattern Generator (serial and parallel format)

* Digital Timing Generator (Opt. 001)

* DUAL ARBITRARY-WAVEFORM GENERATOR (Opt. 002)

An HP 1631A/D LOGIC ANALYZER or one of the DIGITIZING OSCILLOSCOPEs 54100x / 54200x can be partnered with the HP 8175A DIGITAL SIGNAL GENERATOR with Opt. 002 DUAL ARBITRARY WAVEFORM GENERATOR .

Product Description

The arbitrary waveform is achieved by converting the digital data repetitive (as set in the 8175A's memory) by means of a fast DAC. The output signal (ARB Waveform, Sine, Triangle) will be a series of stair steps. The period of signals which shall be simulated is always a function of the number of the discrete levels used to construct that waveform. If a waveform requires e.g. 5 level values, the max. repetition speed divides by 5 to 10MHz.
Since the data memory is used to hold the digital equivalent of the "analog signal", the timing simulator and the virtual memory expansion capability -inherent to the basic instrument- can be used to generate complex signals. The user interface allows setting-up any waveform in terms of voltage vs time duration for multi-level signals

Complex curves can be set-up with a minimum of user inputs by means of the SPLINE function. The SPLINE (linear, natural, periodic) is calculated by the microprocessor on the base of a few user definable points.
The CALCULATOR MODULE enables complex waveforms or patterns (mathematical functions) to be easily set up by means of one or more user defined modules. Each module includes a header and algorithm which together define the pattern (or part of pattern) required.
A selection of standard functions, operators and operands (FOR, STEP, SINE, COS, +, -, etc.) which can be included within the modules are available via softkeys.

1.2 Service Features - Diagnostics and Service Aids

Power-On Selftest and test routines

The actual function of the instrument is determined by the instrument's hardware and recognized by the instrument's firmware.

At power on the HP 8175A will run an internal selftest. This ROM - based check is devided into two parts:

* Normal Self-test
* Extended Self-test

The one, running at power-on is initialized from the rear-panel HP-IB switches. These checks are designed to check the Microprocessor Board (RAMs', ROMs' and Device Bus), the Clock Board (RAMs' and supported circuitries) and the Data Board (RAMs' and supported circuitries). Also the correct instrument configuration will be checked.
In normal Self-test a board level error will be displayed.
The extended Self-test shows the deffective circuit or component on the board.
Each power-on Self-test takes less than one minute to complete. On satisfactory completion, it will have proved that about 90% of the 8175A circuitry is functioning correctly. (There is no check against published specs.)

Calibration

The HP 8175A has two levels of calibration: "hard cal" and "soft cal".
The "hard cal" is required after replacement or repair of one of the main boards. The "hard cal" requires the analog balance adjustments to be performed manually/ automatic before the "soft cal" is performed. The calibration interval for "hard cal" is expected to be once a year and takes approximately 2 hours to complete (automatic). For OPT 002 "hard cal" add on approx. 1 hour (automatic). After a "hard cal" calibration, a performance verification should be performed to ensure the instrument meets its published specifications.
The "soft cal" can be performed by the user at any time to ensure the 8175A is frequency calibrated . The "soft cal" will be completed in a couple of seconds.

Troubleshooting

Manual Signature analysis will be used to troubleshoot digital failures;
analog failures will need manual troubleshooting techniques.
There are six slots for horizontal PC Boards. A vertical mounted Mother Board with two rows of 96 pin connectors provide the necessary interconnections for power, data transfer and high speed signals. For service purposes, additional connectors at the top of the Mother Board are provided, they will accept all PC Boards and allow troubleshooting and calibration without use of Extender Boards or Cables.

The optional FT Board or ARB Board can be retrofitted in those service centers being involved in repair activites. After retrofiting, a recalibration and performance test will be necessary.
OPT. 002 retrofiting of older instruments is possible but requires a special kit which is HP 8175A serial number dependent.
Appropriate Retrofit Kits will be set up (see step 2.3).

1.3 Factory Base Prices

HP 8175A DIGITAL SIGNAL GENERATOR includes Standart Pod Set (4 TTL/CMOS + 1 INPUT)	**14.1 K$**
OPTIONS	
# E01 includes 4 ECL Pods + 1 Trigger Pod (instead of Standard Pod Set)	**13.1 K$**
# T02 includes 4 TTL Pods + 1 TriggerPod (instead of Standard Pod Set)	**12.1 K$**
# D04 deletes Standard Pod Set	**-4.5 K$**
# 001 FINE TIMING	**1.0 K$**
# 002 DUAL ARBITRARY WAVEFORM GENERATOR	**3.0 K$**
ACCESSORIES	
HP 15461A ECL POD (fixed ECL level)	**750 $**
HP 15462A TTL/CMOS POD (prog. High level)	**1000 $**
HP 15463A TRIGGER POD	**500 $**
HP 15464A TTL POD (fixed TTL level)	**500 $**

1.4 Specifications

see Attachment 1

2. Sales / Support Data

2.1

	Sales Forecast Qty/year (Maturity)	Estimated Warranty Repairs Q3-86	Q4-86	Q1-87	Q2-87	Q3-87	Q4-87
USA:							
Neely	100	2	5	8	10	10	11
Midwest	32	1	1	2	3	3	3
Southern	40	1	2	3	4	4	5
Eastern	88	2	4	7	9	9	9
CANADA	40	1	2	3	4	4	5
EUROPE:							
UK	40	1	2	3	4	4	5
France	40	1	2	3	4	4	5
Germany	40	1	2	3	4	4	5
NER	40	1	2	3	4	4	5
SER	40	1	2	3	4	4	5
JAPAN	100	2	5	8	10	10	11

The sales forcast is based on historical sales distribution. Estimated repairs are based on projected sales and the estimated Annualized Failure Rate (AFR).

2.2 First Demo / Customer Shipment

	HP 8175A OPT. 002	HP 15464A
To be on CPL	May 1986	July 1986
NPT EUROPE	May 1986	May 1986
NPT USA	July 1986	July 1986
First Demo Shipment	May 1986	July 1986
First Customer Shipment	June 1986	July 1986

2.3 Support Strategy:

The HP 8175A is on a **return-to-bench**, component level repair strategy. The exceptions to this are the three Pods. For those, a Blue Stripe Exchange program will be set up.

Model	Blue Stripe Exchange P/N
HP 15461A	15461-69601
HP 15462A	15462-69601
HP 15464A	15464-69601

The CRT and the CRT controller board (2090-0066 / 0950-0894) are disposable and they are not supported by a Blue Stripe program. Therefore, new parts must be ordered.

Retrofit of OPTION

 # 001 Exchange Bd. Assy A50 Buffer
by Bd. Assy A52 Fine Timing (P/N 08175-66553)

 # 002 For HP 8175A S/N 2549G00111 to 00270
use Retrofit Kit 1 P/N 08175-68701
For HP 8175A S/N 2549G00271 to 00325
use Retrofit Kit 2 P/N 08175-68702
For HP 8175A S/N 2612G00326 and above
install OPT. 002

The **On-site** Repair Stategy will be:

For customer where down time is critical, exchange instrument by the use of stand-by spare units.

Basic Support Data

see Attachment 2

Parts Support

Parts stocking : All unique replaceable parts will be priced and set up on the Replacement Parts Price List.

2.4 Repair Locations

It will be possible to repair the HP 8175A (and Options) at any service center where the recommended test equipment is available. However, we recommend the following offices as repair locations for the HP 8175A:

EUROPE	Amsterdam	-	Benelux (and Northern European Region)
	Stockholm	-	Scandinavia
	Boeblingen	-	Germany
	Le Lignon	-	Switzerland*
	Milan	-	Italy*
	Orsay	-	France
	Winnersh	-	United Kingdom
			* and Southern European Region
U.S.(ICON)	ISC (Mount.View)	-	All U.S. and ICON
	Rolling Meadows	-	Midwest
	Paramus	-	Northeast / Mid-Atlantic
	Atlanta	-	Southeast
	Fullerton	-	Neely Sales Region
	Richardson	-	Southwest
	Englewood	-	Rocky Mountain
CANADA	Edmonton		
	Montreal		
JAPAN	YHPS		

3. **Warranty**

The HP 8175A carries the standard Hewlett-Packard one year bench warranty.

4. **Training**

A service training seminar (lecture/lab course) for bench repair - component level - will take place in Boeblingen and Colorado Springs in 1987.

Course No: - B493

5. **Documentation**

* Operating and Programming Manual (includes also Fine Timing Option)
  HP P/N 08175-90006
* Service Manual for the HP 8175A and Fine Timing Option
  HP P/N 08175-90001
* Operating Programming Manual OPT 002
  HP P/N 08175-90016
* Service Manual OPT 002
  HP P/N 08175-90011

The O & P Manuals contain all the information required to use the HP 8175A and Options both manually and with HP-IB. A Performance Test procedure will also be included.
The Service Manuals will contain all information necessary to service the corresponding instrument or options, including theory, block diagrams, schematics, component locators, troubleshooting informations, adjustment procedures and a parts replacement lists.

* Data Sheets P/N 5952-9560 / 5952-9595
* Demo Manuals
* Field Training Manuals
* Application Notes P/N 5952-9572

6. Support Equipment

Recommended Test Equipment

INSTRUMENT	REQUIRED CHARACTERISTCS	RECOMMENDED MODELS)	USE*
Oscilloscope	275 MHz Bandwidth	HP 1725A/1722B	P,A,T
Probe	10:1 8pF	HP 10017A	P,A,T
	1:1 36pF	HP 10021A	P,A,T
DVM	0.1V Range,>10MOhm	HP 3456A/3455A	P,A,T
		HP 3478A	
Counter	50 MHz START/STOP TI A to B	HP 5335A/5345A	P,A,T
Signature Multimeter		HP 5005A/(5004A)	T
Pulse Gen.	50 MHz,Wid <10ns	HP 8112A	P
Pulse Gen.	100 MHz	HP 8082A/(8007B)	P
Power Supply		HP 6205A/6237A	A,T
Time Marker	2ns		P
Logic Probe	ECL	HP 10525E	T
Logic Probe	TTL	HP 10525T	T
Controller	HP 200 Series Basic Compatible HP-IB Interface	HP 9816/9836	P,A
ET's	2 S.A.	HP 08175-66522	T
	Extender Boards	HP 08175-66523	
Torque Indicating Screwdriver		HP 8730-0012	T
		HP 8710-0669	
		(HP 8710-0902,-0901)	
Solder-in Receptacle		HP15429A	P,A,T
Plug-on BNC Adaptor		HP 15409A	P,A,T
BNC Tee		HP 1250-0781	P,A,T
BNC F to F		HP 1250-0080	P,A,T
BNC M to M		HP 1250-0216	P,A,T
BNC to Probe Adaptor		HP 1250-1454	P,A,T
BNC Connector RF		HP 1250-0018	P,A,T
Coax Test PT		HP 1250-1737	P,A,T
Probe Tip		HP 10230-62101	P,A,T
Cable		HP 08160-61610	A,T

* P=Performance Test A=Adjust T=Troubleshooting

SPECIFICATIONS

Specifications describe the instrument's warranted performance. Non-warranted values are described as 'typical'. All specifications are valid at the end of the output pod cables, at the probes of the input pod or at the respective BNC connectors of the mainframe. All specifications are valid in a 0° C to 55° C temperature range.

PARALLEL/SERIAL DATA GENERATOR

Parallel or serial operating mode can be selected.

DATA CAPACITY

	parallel	serial
NUMBER OF CHANNELS:	24	2
BITS PER CHANNEL:	1 024	8 192
MAX. BIT RATE PER CHANNEL:	50 Mbit/s NRZ	100 Mbit/s NRZ (ECL POD)

(consider Level and Transition Times specifications)

TIMING

In PARALLEL mode the duration of each individual pattern is programmable. The duration is equal for all data channels. In SERIAL mode the duration of the data bits is programmable with 8 succesive bits always having the same duration. The duration is equal for both channels.

PATTERN DURATION (with internal clock):

Range	Resolution
1) (10), 20 ns – 9.99 µs	10 ns
10µ – 999 µs	1 µs
1 ms – 99.9 ms	100 µs
0.1 s – 9.99 s	10 ms

1) 10 ns in serial mode with fixed timing

Accuracy: ±0.05% of progr. value ±2.5 ns (asynchronous start)
±0.5% of progr. value ±2.5 ns (synchr. start, clock cal.)
±3% of progr. value ±2.5 ns (synchr. start no clock cal.)

Jitter (max.): 0.1% of progr. value + 150 ps

PATTERN DURATION (with external clock):
Period of external clock x m

Range (m = No. of ext. clock cycles)				Resolution
2) (1)2	to	999	/	1 period
1.000	to	99.900	/	100 periods
100.000	to	9.990.000	/	10.000 periods
10.000.000	to	999.000.000	/	1.000.000 periods

2) min Pattern Duration in serial mode: 10 ns
min. Pattern Duration in parallel mode: 20 ns

CLOCK

The clock has a programmable period. It is available on line 7 of the pod for the output flags. The clock is derived from an internal system clock or from an external clock. See EXTERNAL CLOCK (BNC) and HP 15463A TRIGGER POD specifications.

Note: For ECL and TTL POD only and Pattern Duration ≧ 20 ns: In serial mode an additional Serial Clock is available on pod 0, channel 1 providing a pulse at every bit.

PERIOD (with internal clock):

Range	Resolution
20 ns – 9.99 µs	10 ns
2 µs – 999 µs	1 µs

Accuracy: ±0.05% of progr. value ±2.5 ns (asynchronous start)
±0.5% of progr. value ±2.5 ns (synchr. start, clock cal.)
±3% of progr. value ±2.5 ns (synchr. start, no clock cal.)

PERIOD (with external clock):
Period of external clock x m

Range (m): 2 . . . 999 [x 1]
2 . . . 999 [x 100]

SKEW between channels of

ECL pods:	≦6 ns; typical ≦3 ns
TTL/CMOS pods:	≦7 ns; typical ≦3 ns
TTL pods:	≦7 ns; typical ≦5 ns

Maximum time difference between the leading or trailing data bit edges of the same memory address with Fime Timing (opt. 001) off.

HP 15462A TTL/CMOS POD

(DATA OR FLAG OUTPUT POD)

NO. OF CHANNELS: 8

MAX. BIT RATE PER CHANNEL: 50 Mbit/s NRZ

LEVELS

Following level specifications apply for pattern durations and clock periods ≧ 50 ns, into open.

HIGH LEVEL (range/resolution): 2.4 V – 9.9 V/100 mV
Accuracy: ±5% of programmed value ±300 mV

LOW LEVEL: ≦0.7 V

Programmed high level is valid for all pods connected. High level of an individual pod can also track an external voltage applied to this pod. Ext. level overwrites progr. level if greater. The full level ranges can be achieved provided transition times do not violate pattern duration or clock width. To avoid violation transition times have to be shorter than pattern durations or clock width. Transition times depend on load terminations as specified below.

TRANSITION TIMES

into open:	≦3 ns + high level x 1.2 ns/V
into 50 pF:	≦9 ns + high level x 1.8 ns/V

FAN-OUT PER CHANNEL (typical): 10 LS TTL

OVERSHOOT, RINGING ≦20% of amplitude (into open)

MAX. EXTERNAL VOLTAGE AT OUTPUTS: -3 V / + 10 V

DISABLE / ENABLE CHARACTERISTICS (TRI-STATE)
T(ON), T(OFF): ≦30 ns

(Time difference between occurence of external ON or OFF signal at an output pod (TRIST) until outputs are disabled or enabled; High level of ext. signal ≦ High level at outputs)

LEAKAGE CURRENT:	≦20 µA
RESIDUAL CAPACITANCE:	≦40 pF
TRI-STATE INPUT at the output pod (TRIST)	
IMPEDANCE (typical):	10 kOhm/50 pF
THRESHOLD:	35% of programmed or ext. high level
Min. overdrive:	600 mV
MAX. EXTERNAL VOLTAGE AT INPUTS (TRIST, HIL):	0 V to 10 V

HP 15461A ECL POD

(DATA OR FLAG OUTPUT POD)

NO. OF CHANNELS	8
MAX. BIT RATE PER CHANNEL:	100 Mbit/s NRZ
LOW LEVEL:	≦ -1.60 V
HIGH LEVEL:	≧ -1.02 V
TRANSITION TIMES (20% - 80%; into 22 pF):	≦3 ns
FAN-OUT PER CHANNEL (typical):	5 ECL
OVERSHOOT, RINGING (into 22 pF):	≦20% of amplitude
MAX. EXTERNAL VOLTAGE AT OUTPUTS:	±5 V
DISABLE/ENABLE CHARACTERISTICS (ECL common LOW)	
T(ON), T(OFF)	≦15 ns

(Time difference between occurence of external ON or OFF signal at an output pod ($\overline{EN}$) until outputs are enabled or disabled.)

ENABLE/DISABLE INPUT ($\overline{EN}$)	
IMPEDANCE (typical):	60 kOhm/50 pF
INPUT CHARACTERISTICS:	ECL compatible
MAX. EXT. VOLTAGE AT INPUT ($\overline{EN}$):	0 V to -5 V

HP 15463A TRIGGER POD

(TRIGGER WORD INPUT POD)

This pod is used for external status and/or output flag control. In synchronous mode, it reads trigger words in at positive or negative transitions of a clock applied to this pod. In asynchronous mode it accepts trigger words without clock. The applied clock may be used as an alternative to the internal clock or to the external clock via BNC.

MAX. CLOCK RATE:	25 MHz
IMPEDANCE (typical):	100 kOhm/5 pF
THRESHOLD (range/resolution):	-9.9 V to +9.9 V/100 mV
Accuracy:	±2.5% ±120 mV
Min. overdrive:	250 mV or 30% of input amplitude, whichever is greater
Min. swing:	600 mV (P-P)
MAX. INPUT VOLTAGE:	±40 V

HP 15464A TTL POD

(DATA OR FLAG OUTPUT POD)

NO. OF CHANNELS:	8
MAX. BIT RATE PER CHANNEL:	50 Mbit/s NRZ
HIGH LEVEL (into open):	5 V ± 5%
LOW LEVEL(into open):	≦0.7 V
TRANSITION TIMES	
into open:	≦ 6 ns
into 50 pF:	≦12 ns
FAN OUT PER CHANNEL:	15 LS TTL
OVERSHOOT, RINGING (into open):	≦20% of amplitude
MAX. EXTERNAL VOLTAGE AT INPUT AND OUTPUTS:	-3 V/ +8 V
DISABLE / ENABLE CHARACTERISTICS (TRI-STATE)	
T(ON), T(OFF):	≦50 ns
LEAKAGE CURRENT:	≦10 µA
RESIDUAL CAPACITANCE (typical):	≦50 pF
TRI-STATE INPUT at the output pod (TRIST)	
IMPEDANCE (typical):	10 kOhm/ 40 pF
THRESHOLD:	1.8 V
Min. overdrive:	150 mV

EXTERNAL INPUT (BNC)

This is a connector at the front panel which, on application of a suitable signal, can be used to START datacycling on positive, negative or both transitions or, to START and STOP cycling with selectable transitions.

IMPEDANCE:	10 kOhm/50 pF
THRESHOLD (range/resolution):	-9.9 V to +9.9 V/100 mV
Accuracy:	±5% of progr. value ±250 mV
Min. swing:	600 mV (P-P)
Min. overdrive:	250 mV or 30% of input amplitude, whichever is greater
MAX. INPUT VOLTAGE:	±20 V

EXTERNAL CLOCK (BNC)

The applied clock may be used as an alternative to the internal system clock or the external clock via the input pod.

CLOCK RATE (range):	DC to 100 MHz

All other specifications see EXTERNAL INPUT (BNC).

EXTERNAL REFERENCE (BNC)

The internal timing reference (crystal) can be replaced by an external signal applied to a rear panel connector (1 MHz). Accuracy must be better than 0.01%.

INPUT CHARACTERISTICS:	LS TTL compatible
MAX. INPUT VOLTAGE:	±20 V

OPTION 001 FINE TIMING

Option can be retrofitted at HP service office.

PARALLEL DATAGENERATOR	
CHANNELS:	0,1,2 and 3 of pod 0
DELAY (range/resolution):	20 ns to 40 ns / 100 ps
vs same channel with Fine Timing 'OFF'	
Accuracy:	±5% of progr. value ±1 ns
SERIAL DATAGENERATOR	
CHANNELS:	0 and 2 of pod 0
DELAY (range/resolution):	0 ns to 20 ns / 100 ps
vs same channel progr. to 0 ns Delay	
Accuracy:	±5% of progr. value ±2 ns

SPECIFICATIONS

OPTION 002, DUAL ARBITRARY WAVEFORM GENERATOR

Option can be retrofitted at HP service office.

NUMBER OF OUTPUTS (Output A and Output B on front panel, can be separately disabled): 2

NUMBER OF BITS: 10

NUMBER OF DATA POINTS:

Horizontal: 1024 points

Vertical: 1000 points with additional 24 points override,
800 points for 16 V P-P Output Voltage Range,
640 points for 32 V P-P Output Voltage Range.

DIFFERENTIAL NON-LINEARITY: ≦1 LSB (monotonic)

OUTPUT IMPEDANCE: 50 Ohm ± 5%

OUTPUT LEVELS

Level Window defines the maximum output signal range for the sum of Offset and P-P Output Voltage.

Load Impedance: 50 Ohm

Level Window	P-P Output Voltage Range	P-P Output Voltage Res.	Offset Range	Offset Res.
±0.8 V	0.2 V	0.2 mV	±0.8 V	0.5 mV
±0.8 V	0.5 V	0.5 mV	±0.8 V	0.5 mV
±0.8 V	1 V	1 mV	±0.8 V	1 mV
± 8 V	2 V	2 mV	± 8 V	5 mV
± 8 V	5 V	5 mV	± 8 V	5 mV
± 8 V	10 V	10 mV	± 8 V	10 mV
± 8 V	16 V	20 mV	± 8 V	20 mV

Load Impedance ≧ 50 kOhm

Level Window	P-P Output Voltage Range	P-P Output Voltage Res.	Offset Range	Offset Res.
±1.6 V	0.5 V	0.5 mV	±1.6 V	0.5 mV
±1.6 V	1 V	1 mV	±1.6 V	1 mV
±1.6 V	2 V	2 mV	±1.6 V	2 mV
± 16 V	5 V	5 mV	± 16 V	5 mV
± 16 V	10 V	10 mV	± 16 V	10 mV
± 16 V	20 V	20 mV	± 16 V	20 mV
± 16 V	32 V	50 mV	± 16 V	50 mV

Accuracy (Output A and Output B):

Amplitude Accuracy: ±4% ±4 LSB 1)

Offset Accuracy:
±1% of programmed value
±4% of (programmed High Level of P-P Output Voltage + programmed Low Level of P-P Output Voltage) ÷ 2 2)

plus:

into 50 Ohm

± 10 mV for 0.2 V to 1 V P-P Output Voltage Range
or ± 25 mV for 2 V to 5 V P-P Output Voltage Range
or ± 50 mV for 10 V to 16 V P-P Output Voltage Range

into ≧ 50 kOhm

± 20 mV for 0.5 V to 2 V P-P Output Voltage Range
or ± 50 mV for 5 V to 10 V P-P Output Voltage Range
or ±100 mV for 20 V to 32 V P-P Output Voltage Range

1) Amplitude is programmed High Level - programmed Low Level.

2) If programmed High and Low Level of P-P Output Voltage are identical in magnitude but opposite in sign, this error will be zero.

TIMING (for Output A and B)

The maximum sample update rate is 50 MHz.
The Data Point Duration is 20 ns to 9.99 s (for more information see "Timing" of the PARALLEL mode, page 13).

TRIGGER OUTPUT CHARACTERISTICS

NUMBER OF TRIGGER OUTPUT CHANNELS: 2
(Trigger Output A on front panel, Trigger Output B on rear panel, can be commonly disabled)

TRIGGER OUTPUT IMPEDANCE: 50 Ohm ± 5%

TRIGGER OUTPUT LEVELS:

	Load Impedance 50 Ohm	Load Impedance ≧ 50 kOhm
TTL Low Level:	≦ 0.3 V	≦ 0.2 V
TTL High Level:	≧ 2.4 V	≧ 4.8 V
ECL Low Level:	≦ -1.6 V	
ECL High Level:	≧ -0.9 V	

Trigger Pulse Width: The trigger can be set for each individual data point to High Level or Low Level. The trigger width depends on the programmed Data Point Duration.

SUPPLEMENTARY CHARACTERISTICS

(describe typical non-warranted performance)

DELAYS

from \ to	Clock out (pod)	Data out (pod)
Ext. Clock in (pod):	150 ns	140 ns
Ext. Clock in (BNC):	110 ns	100 ns
Clock out(pod): 3)	–	10 ns

3) Time positive transition of clock is delayed with respect to a leading data bit transition (clock period = pattern duration).

RESPONSE TIMES (to perform action via pod)

CONT, STOP, TRISTATE ON/OFF: ≦ 170 ns 4)
+ trig. word duration

START, JMP A, JMP B: ≦ 170 ns 4)
+ trig. word duration
+ 9 clock periods 5)

OUTPUT FLAGS: ≦ 100 ns 4)
+ trig. word duration

4) Trigger word duration: 20, 50, 100, 500 ns.
Time window during which a trigger word has to be stable.

5) Clock period constant with internal clock: 10 ns; otherwise use clock period of external clock

START via BNC: ≦ 100 ns + 9 clock periods

STOP via BNC: ≦ 100 ns

SUPPLEMENTARY CHARACTERISTICS

(describe typical non-warranted performance)

OPTION 002, DUAL ARBITRARY WAVEFORM GENERATOR

REPEATABILITY: Factor 4 better than accuracy.

WAVEFORM CHARACTERISTICS
(Output A and Output B, at maximum P-P Output Voltage for all ranges into 50 Ohm)

Sinewave from 20 Hz ... 500 kHz, characterized by 100 Datapoints:

Harmonic signals: (98 harmonics taken into account)
from 20 Hz to 50 kHz: ≦ -51 dBc
from > 50kHz to 500 kHz: ≦ -46 dBc

Amplitude flatness: ±3% [±0.26 dB]
(reference is 1 kHz at 2 V P-P Output Voltage)

Triangle at 1 kHz, characterized by 1000 datapoints:

Integral nonlinearity between 10% and 90% of P-P Output Voltage (data point at steady state): ≦10 LSB

Pulse Performance:

Rise/Fall Time (10% to 90% of P-P Output Voltage): <16 ns
Settling Time
(from 10% of P-P Output Voltage to ±5% of final value): ≦20 ns

DELAYS

Trigger A to Channel A: <20 ns
Trigger B to Channel B: <20 ns
Channel A to Channel B: < 5 ns
Digital outputs to channel A and B: <15 ns

RESPONSE TIMES
(Refer to Page 15, TRISTATE ON/OFF function is not available for Outputs A and B and Trigger Outputs.)

DATA MEMORY

(LOAD, EDIT, UPDATE, SEQUENCING)

The memory can be loaded, manually or via HP-IB. The following complete data and parameter set-up's are readily accessible: Standard setting (memory cleared), active setting, 2 previously stored settings, and calculator setting (Option 002).
These settings are retained in a battery backed-up memory for up to 3 weeks when power is off.
Various editing functions allow to set, modify, move and copy blocks of data between addresses or channels. The following fixed patterns are available:
Up-counter/down-counter, definable increments and start/stop address; in parallel mode.
PRBS; length is 2 (exp n), n = 3 to 13 in serial mode.
Data codes include BIN, OCT, HEX, DEC

Data can be edited while the instrument is running without affecting the data currently being output. This is also possible viaHP-IB. The changes become active after an UPDATE command with status STOP.

Parameters waiting for an UPDATE are: Data patterns, Levels (Option 002) and timings, cycling definitions and input trigger/output flag assignments.

1 – 255 segments can be sequenced; segments are user definable in the 0000 to 1023 address range; segments may overlap.
START, CONTINOUS START, JMP A AND JMP B (BRANCHING) refer to user-assigned segment-names.

HP-IB CAPABILITY

The following HP-IB interface functions are implemented:
SH1, AH1, T6, TE0, L4, LE0, SR1, RL1, PP0, DC1, DT1, C0.

HP-IB PROGRAMMING TIMES (typical):

Times are measured by using the HP 9836A as an HP-IB controller. Reloading refers to programming a setting which once was set-up in the HP 8175A and transfered to the controller.

COMPLETE RELOAD TIME: 1.8 s

DATA/TIMING/PROGRAM RELOAD TIME: 800 ms
(Software and hardware update)

DATA/TIMING/PROGRAM RELOAD TIME: 180 ms
(Hardware update only)

FLEXIBLE DISC DRIVE ACCESS

Storage of set-ups, data and calculator formule (Option 002) on a flexible disc. Up to 256 settings can be managed depending on disc space.

HARD COPY

Any display can be copied to a graphics printer.

PARALLEL OPERATION

Two HP 8175A's can be operated in master-slave configuration, thus doubling the channel count to 48 channels or 4 analog channels (Option 002). Synchronization is provided by the HP 15430A cable.

GENERAL

ENVIRONMENTAL

STORAGE TEMPERATURE: -40 C to +65 C
OPERATING TEMPERATURE: 0 C to +55 C
HUMIDITY (0 C to +40 C): 95% R. H.

CALIBRATION

Within a recalibration period of 1 year the instrument is warrented to meet all specifications described after a warm-up time of 30 min. The pattern duration accuracy and the clock accuracy can be enhanced by the inbuilt autocalibration feature. To stay within that higher accuracy, autocalibration is recommended to be repeated every 0.5 hours and also as soon as environmental conditions have changed.

POWER: 115/230 V ac; -22% +10%
48 – 66 Hz; 630 VA max.

WEIGHT: Net 17,5 kg (38.8 lb)
Shipping 24,0 kg (53 lb)

DIMENSIONS
MAINFRAME: 190 mm high, 426 mm wide, 584 mm deep
(7.5 x 16.75 x 23 in)

PODS:

CABLE LENGTH	15461A	15462A	15464A	15463A
mainframe to pod:	1.6 m	1.6 m	1.6 m	1.6 m
pod to end of cable:	0.2 m	0.2 m	0.2 m	0.25 m

HP 8175A ORDERING INFORMATION

HP 8175A DIGITAL SIGNAL GENERATOR will be shipped with configurations
standard: 4 ea **HP 15462A** TTL/CMOS PODS,
1 ea **HP 15463A** TRIGGER POD
E01: replaces standard with 4 ea **HP 15461A** ECL PODS,
1 ea **HP 15463A** TRIGGER POD **
T02: replaces standard with 4 ea **HP 15464A** TTL PODS,
1 ea **HP 15463A** TRIGGER POD **
For individual configurations, order standard configuration with Delete Option D04.

OPTIONS

001 Fine Timing (100 ps resolution on four channels)
002 Dual Arbitrary Waveform Generator (2 analog outputs)
D04 Delete standard pods for individual requirements
908 Rack Flange Kit
910 Additional Operating / Programming / Service Manual
916 Additional Operating and Programming Manual

ACCESSORIES

Pods

HP 15461A ECL POD (fixed ECL level, includes 1 ea HP 15429A)
HP 15462A TTL/CMOS POD (progr. High Level, includes 1 ea HP 15429A)
HP 15463A TRIGGER POD (includes lead set and 10 ea probe tips)
HP 15464A TTL POD (fixed TTL level, includes 1 ea HP 15429A) **

Adapters for HP 15461A, HP 15462A and HP 15464A

HP 15408A plug-on grabbers with ground leads, 5 ea
HP 15409A plug-on BNC adapters, 5 ea
HP 15410A plug-on SMB adapters, 5 ea
HP 15411A plug-on coax open-end adapters, 5 ea
HP 15415A plug-on miniprobe, can be used with HP 10024A IC testclip, 5 ea
HP 15429A solder-in receptacles for connection to a PC board, 5x2 ea

Adapters for HP 15463A

HP PN 15463-63201 lead set
HP PN 10230-62101 probe tip, 1 ea (10 ea necessary per pod)

Others

HP 15430A cable for synchronized master-slave operation of two ea HP 8175A
HP 10062A Protective Cover (protects front cover)

PERIPHERALS (recommended, others - refer to manual)

HP 2225A Thinkjet graphics printer (for local version refer to catalog)
HP 9122D dual, double-sided 3.5 inch flexible disc drive
HP 92192A box of ten blank 3.5 inch double-sided discs
HP 10833A/D 1 meter (3.3 ft) / 0.5 meter (1.6 ft) HP-IB cable

** available in July 86

HEWLETT PACKARD

Attachment 2 — BASIC SUPPORT DATA WORKSHEET
HARDWARE SUPPORT

Component Model # HP 8175A (or with Option # 001) Division BID

Product Line 24 System Model # — System Option # —

I. HARDWARE SUPPORT STRATEGY

A. STRATEGY: Check one or both boxes below and complete applicable sections that follow.

On-Site ☐ Bench ☒

B. COMMENTS ON STRATEGY: Component Level Repair

C. POTENTIAL SUPPORT PROBLEMS: Three Pods (15461A, 15462A and 15464A) have been put on Blue Stripe Program.

II. SCHEDULED MAINTENANCE

A. ROUTINE PREVENTATIVE MAINTENANCE: (Show preventative maintanance time only.)

	Bench	On-Site
1. PM Cycle:	N/A (xx) PM/yr	N/A (xx) PM/yr
2. Average PM Time:	N/A (xx.x) h/PM	N/A (xx.x) h/PM

B. CALIBRATION: Full specification check and adjustment as needed.

1. Is calibration: (Check one or both boxes. If both apply, show both manual and automated data below.)
   Manual ☒ Automated ☒
2. Automated tests are performed on: SCAT ☐ PCU ☐ Other ☒
   If Other, describe Series 200 Controller with VERICAL Disc

		Bench	On-Site
3. Calibration Cycle:		1 (xx) Cal/yr	N/A (xx) Cal/yr
4. Average Cal Time:	(Manual)	5.0 (xx.x) h/Cal	N/A (xx.x) h/Cal
	(Automatic)	3.0 (xx.x) h/Cal	N/A (xx.x) h/Cal

5. Is calibration required as part of: Repair ☐ PM ☐ Other ☐
   If other, specify

C. OPERATION VERIFICATION. Short procedure providing a 90% level of confidence that the product meets its published specifications.

1. Is operation verification: (Manual ☒) Automated ☒
2. If automated, are tests performed on: SCAT ☐ PCU ☐ Other ☒
   If Other, describe Series 200 Controller with VERICAL Disc

	Bench	On-Site
3. Op Ver Cycle:	N/A (xx) OV/yr	N/A (xx) OV/yr
4. Average OP Ver Time: (2.0)	1.5 (xx.x) h/OV	N/A (xx.x) h/OV

5. Operation verification is a required part of:

Repair ☒ PM ☐ Other ☐

If other, specify _____

D. FUNCTIONAL TEST. Verifies that the product performs its designed functions.

	Bench	On-Site
1. Functional Test Cycle:	N/A (xx) FT/yr	N/A (xx) FT/yr
2. Ave Functional Test time:	0.5 (xx.x) h/FT	N/A (xx.x) h/FT

3. Is a functional test required as part of:

Repair ☒ PM ☐ Cal ☐ Other ☐

If other, specify **FT is part of OP Ver**

III. UNSCHEDULED MAINTENANCE – REPAIRS

A. DIAGNOSIS AND REPAIR. Time and materials required to setup and diagnose the fault, determine the corrective action and replace defective components. Does *not* include post-repair testing, (part B below).

	Bench	On-Site
1. Est Failure Factor*:	0.15 (xx) Fail/inst-yr	N/A (xx) Fail/inst-yr
2. Mean Time to Repair:	5.0 (xx.x) h/repair	N/A (xx.x) h/repair
3. Average Parts Charge: (Use List Price)	100 (xxxx) $/repair	N/A (xxxx) $/repair

* Data should be based on 2000 operating hours/year of product use under normal environmental and operating conditions. Failure factor is calculated as the annualized percent Failure Rate divided by 100.

B. POST-REPAIR CALIBRATIONS/OPERATION VERIFICATIONS/FUNCTIONAL TESTS If the time required to perform these operations after the repair differs from that shown in Section II, please explain and show charges below; otherwise enter "N/C" (No Change):

1. Explanation: N/C

	Bench	On-Site
2. Average Cal Time:	N/C (xx.x) h/Cal	N/C (xx.x) h/Cal
3. Average Time Op Ver Time:	N/C (xx.x) h/OV	N/C (xx.x) h/OV
4. Average Funct Test Time: (Use List Price)	N/C (xx.x) h/FT	N/C (xx.x) h/FT

IV. OTHER HARDWARE SERVICES: Complete this section for base system, show only incremental time for options (if applicable).

A. SITE PREP (On-Site only): Site review prior to installation to assess power and environmental requirements. Do *not* include travel time.

1. SITE PREP Time: N/A (xx.x) h
2. When performed: N/A

B. INSTALLATION (On-Site only): Inventorying, unpacking, installing and verifying the system is functioning (PT11). Start-up operator training (PT21). Do *not* include travel time.

1. System Hardware integration and Startup: N/A (xx.x) h
2. Start-up Operator Training: N/A (xx.x) h

C. LOANERS: If provision of loaner instruments is part of the service strategy for this product, attach a sheet giving model numbers needed, recommended quantity, and estimated probability of need.

V. SPECIAL COSTS NOT COVERED ABOVE (Period Overhauls, Expensive Parts, PM Suppliers, Vendor Repairs, Special Cals, etc.)

A. DESCRIPTION OF COSTS: N/A

	Bench	On-Site
B. TOTAL LABOR HOURS:	N/A h/yr	N/A h/yr
C. TOTAL PARTS CHARGE:	N/A $/yr	N/A $/yr
D. ADDITIONAL COSTS:	N/A $/yr	N/A $/yr

Attachment 2 — BASIC SUPPORT DATA WORKSHEET
HARDWARE SUPPORT

Component Model # HP 8175A Option # 002 Division BID
Product Line 24 System Model # — System Option # —

I. HARDWARE SUPPORT STRATEGY

A. STRATEGY: Check one or both boxes below and complete applicable sections that follow.

On-Site ☐ Bench ☒

B. COMMENTS ON STRATEGY: Component Level Repair

C. POTENTIAL SUPPORT PROBLEMS: The ARB OPT. has a special "Calibration Circuit". The Adjustments are divided into two parts: ADJ and EEPROM CAL. EEPROM CAL can be done only with use of the ARB VERICAL Disc.

II. SCHEDULED MAINTENANCE

A. ROUTINE PREVENTATIVE MAINTENANCE: (Show preventative maintanance time only.)

	Bench	On-Site
1. PM Cycle:	N/A (xx) PM/yr	N/A (xx) PM/yr
2. Average PM Time:	N/A (xx.x) h/PM	N/A (xx.x) h/PM

B. CALIBRATION: Full specification check and adjustment as needed.

1. Is calibration: (Check one or both boxes. If both apply, show both manual and automated data below.)
   Manual ☐ Automated ☒
2. Automated tests are performed on: SCAT ☐ PCU ☐ Other ☒
   If Other, describe Series 200 Controller with ARB VERICAL Disc

		Bench	On-Site
3. Calibration Cycle:		1 (xx) Cal/yr	N/A (xx) Cal/yr
4. Average Cal Time:	(Manual)	N/A (xx.x) h/Cal	N/A (xx.x) h/Cal
	(Automatic)	1.5 (xx.x) h/Cal	N/A (xx.x) h/Cal

5. Is calibration required as part of: Repair ☒ PM ☐ Other ☐
   If other, specify

C. OPERATION VERIFICATION. Short procedure providing a 90% level of confidence that the product meets its published specifications.

1. Is operation verification: (Manual ☒) Automated ☒
2. If automated, are tests performed on: SCAT ☐ PCU ☐ Other ☒
   If Other, describe Series 200 Controller with ARB VERICAL Disc

	Bench	On-Site
3. Op Ver Cycle:	N/A (xx) OV/yr	N/A (xx) OV/yr
4. Average OP Ver Time:	(1.5) 1.0 (xx.x) h/OV	N/A (xx.x) h/OV

5. Operation verification is a required part of:

Repair ☒ PM ☐ Other ☐

If other, specify _____

D. FUNCTIONAL TEST. Verifies that the product performs its designed functions.

	Bench	On-Site
1. Functional Test Cycle:	N/A (xx) FT/yr	N/A (xx) FT/yr
2. Ave Functional Test time:	0.5 (xx.x) h/FT	N/A (xx.x) h/FT

3. Is a functional test required as part of:

Repair ☒ PM ☐ Cal ☐ Other ☐

If other, specify **FT is part of OP Ver**

III. UNSCHEDULED MAINTENANCE – REPAIRS

A. DIAGNOSIS AND REPAIR. Time and materials required to setup and diagnose the fault, determine the corrective action and replace defective components. Does *not* include post-repair testing, (part B below).

	Bench	On-Site
1. Est Failure Factor*:	0.15 (xx) Fail/inst-yr	N/A (xx) Fail/inst-yr
2. Mean Time to Repair:	3.0 (xx.x) h/repair	N/A (xx.x) h/repair
3. Average Parts Charge: (Use List Price)	80 (xxxx) $/repair	N/A (xxxx) $/repair

* Data should be based on 2000 operating hours/year of product use under normal environmental and operating conditions. Failure factor is calculated as the annualized percent Failure Rate divided by 100.

B. POST-REPAIR CALIBRATIONS/OPERATION VERIFICATIONS/FUNCTIONAL TESTS If the time required to perform these operations after the repair differs from that shown in Section II, please explain and show charges below; otherwise enter "N/C" (No Change):

1. Explanation: N/C

	Bench	On-Site
2. Average Cal Time:	N/C (xx.x) h/Cal	N/C (xx.x) h/Cal
3. Average Time Op Ver Time:	N/C (xx.x) h/OV	N/C (xx.x) h/OV
4. Average Funct Test Time: (Use List Price)	N/C (xx.x) h/FT	N/C (xx.x) h/FT

IV. OTHER HARDWARE SERVICES: Complete this section for base system. show only incremental time for options (if applicable).

A. SITE PREP (On-Site only): Site review prior to installation to assess power and environmental requirements. Do *not* include travel time.

1. SITE PREP Time: N/A (xx.x) h
2. When performed: N/A

B. INSTALLATION (On-Site only): Inventorying, unpacking, installing and verifying the system is functioning (PT11). Start-up operator training (PT21). Do *not* include travel time.

1. System Hardware integration and Startup: N/A (xx.x) h
2. Start-up Operator Training: N/A (xx.x) h

C. LOANERS: If provision of loaner instruments is part of the service strategy for this product, attach a sheet giving model numbers needed, recommended quantity, and estimated probability of need.

V. SPECIAL COSTS NOT COVERED ABOVE (Period Overhauls, Expensive Parts, PM Suppliers, Vendor Repairs, Special Cals, etc.)

A. DESCRIPTION OF COSTS: N/A

	Bench	On-Site
B. TOTAL LABOR HOURS:	N/A h/yr	N/A h/yr
C. TOTAL PARTS CHARGE:	N/A $/yr	N/A $/yr
D. ADDITIONAL COSTS:	N/A $/yr	N/A $/yr

OP

ARB INSTALLATION INSTRUCTIONS

IMPORTANT

NOTE for Kits 08175-68701 and 08175-68702:

Before you start on this modification, ensure that the letter
enclosed with this Kit has to be sent to the customer
AND THAT HE HAS RE-AFFIRMED HIS INTENTION
to have the modification fitted.
If the modification IS to be done, send the 3.5" disc
(Data Conversion Program 08175-12305, enclosed with this Kit)
with the instrument when you return it to the customer.
Do NOT sent the disc if the instrument is to be returned unmodified!

This action does NOT apply to Kit 08175-68703,
because the firmware is compatible. For this reason, neither the customer letter nor the disc are included in Kit 08175-68703.

These instructions explain how to install the ARB Option (002) in the 8175A. There are three different categories of retrofit possible, which depend on the serial number of the standard 8175A:

For S/N	Kit	P/N	Procedure
2514G00111 to 2520G00270	Retro Kit 1	08175-68701	@
2549G00271 to 2549G00325	Retro Kit 2	08175-68702	#
2612G00326 and above	Retro Kit #002	08175-68703	*

NOTE:

The signs: @, #, * identify which steps are required for the particular serial numbers.

WARNING

The ROM's and the boards in this instrument are static sensitive.
Please use standard ESD precautions whenever the units covers are removed.

OPTION and RETRO KITS (General)

With the 8175A switched OFF, disconnect the power cord.

@#* 1. Unscrew and remove the 4 rear frame feed of the instrument.

@#* 2. Unscrew and remove the cover bottom cabinet (MP5) and cover bottom (MP8). Adapter Ground 1 and 2 (two strips of metal) are no longer used. (Note the different lengths of 3 and 11 screws!)

@ 3. Fit bumper (0403-0285) to the circuit side of the A50 as shown in Fig. 1.

@#* 4. Carefully plug BD-AY-ARB A70 into the lowest "slot" of the Mother Board.

@# 5. Install one Core Assy (08175-61619) on each Output Cable and fix it with two ty-wraps (one on each side) approx. 1 inch behind the SMB-Connecter.

OUTPUT A	W10 J702	blue shrink tubing
OUTPUT B	W11 J703	white shrink tubing

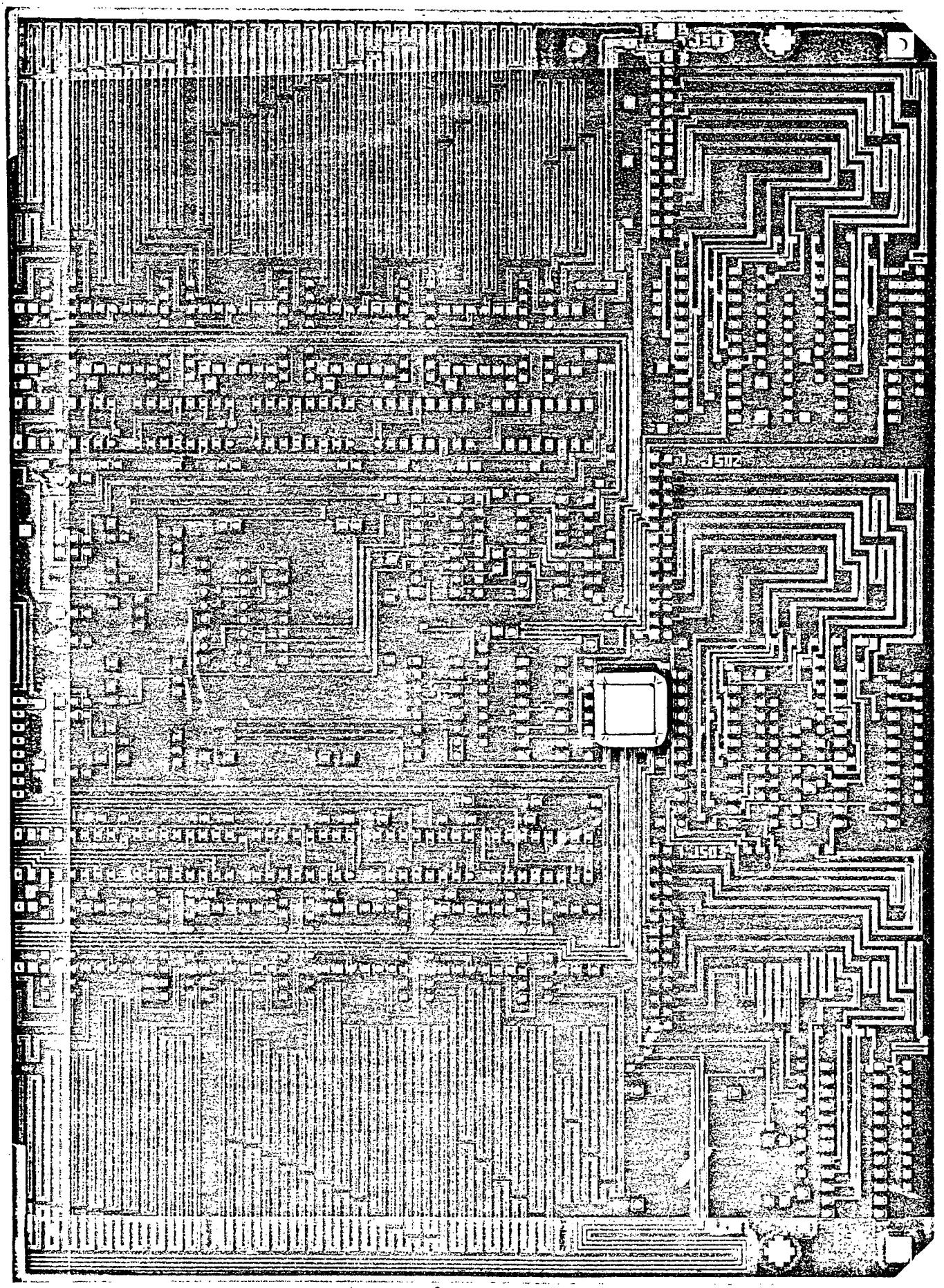
@#* 6. Connect the Output and Trigger cables to the A70 board.

@# 7. Use the adhesive tape to fix the insulator sheet to the cover bottom.

@#* 8. Install the cover bottom back in position, refit and tighten the cover bottom screws (3 short / 11 long).

@#* 9. Install the cover bottom cabinet back in position.

Figure 1. Bumper on circuit side of A50.



RETRO KITS (Specific)

@# 10. Unscrew and remove the cover top cabinet (MP4).

@# 11. Unscrew and remove the cable clamp top (MP16) and disconnect both cable ribbon from A20 Bd.-Assy-CPU.

@# 12. Unscrew and remove cover rear (MP23).

@# 13. Remove Bd.-Assy-CPU (08175-66520) from its slot (Use the Extractors).

@ RETRO KIT 1 (Specific)

14. Install the new Bd.-Assy-CPU (08175-66524), connect the cable ribbon, refit the cable clamp and tighten the screw.

15. Unscrew and remove the cover top front (MP9) and the cover top (MP10).

WARNING

Hazardous voltages are present on the A10 board and dangerous energy is stored even after power is removed. C2/R3 and C3/R4 have a discharge time constant of approx. 100 seconds. The primary voltage lines have approx. 300 V across them, + and - 150V DC to ground. Therefore, wait at least five minutes for capacitors to discharge before servicing the power supply board.

16. Disconnect the FAN-Cables. Unscrew and remove carefully the Power Supply Bd. (Take special care when disconnecting MP53/54 from Power Switch S1). Unscrew and remove the insulator from the circuit side of this board.

17. Replace A10C2 and C3 (820 uF) with the new 1000 uF capacitors.

18. Install the insulator back in position. Carefully install the board back in position. Reconnect the FAN-Cables and refit the cover top.

19. Disconnect the 3 SMB-Cables from the A30 Bd.-Assy-Clock.

20. Remove the A30 board from its slot and plug it into the Service Connector on top of the Mother Board. Switch the instrument ON and verify that the power on self test message indicates a "Power-Up Complete".
Check and readjust if necessary the power supply voltages.

21. Follow the Adjust Procedure, Para. 5-7, steps 3. and 5. of the 8175A O/S Manual (08175-90001).

22. Switch the unit OFF. Install the Clock Board A30 back in position and reconnect the 3 SMB-Cables.

RETRO KIT 2 (Specific)

14. CPU Board A20: Replace the 8 old ROM's with 6 new ROM's. The chart below identifies which new ROM replaces a corresponding old one. Ensure that each ROM is correctly positioned on the board.

REF. DESIG.	NEW ROM'S	OLD ROM'S
U210 EPROM 1	08175-13710	08175-13700
U211 EPROM 2	08175-13711	08175-13701
U106 EPROM 3	08175-13712	08175-13702
U107 EPROM 4	08175-13713	08175-13703
U108 EPROM 5	---	08175-13704
U109 EPROM 6	08175-13715	08175-13705
U110 EPROM 7	---	08175-13706
U111 EPROM 8	08175-13717	08175-13707

15. In addition, reposition (solder) Jumper wire from the W1 position to its W2 position. Also, solder the new board ID label -66524. This label will identify the board as now being a 08175-66524 board (A20 Bd.-Assy-CPU). Continue at step 22.

16. Plug the CPU Bd. into the Service Connector on top of the Mother Board. Switch the instrument ON and verify that the power on self test message indicates a "Power-Up Complete".
Check and readjust if necessary the power supply voltages.

Continue at step 23.

OPTION and RETRO KITS (General)

@#* 23. Switch the unit OFF. Carefully re-assemble the instrument.

@#* 24. Switch the unit ON and verify that the power up self test message shows a "Power-Up Complete" indication, and shows on the System Page the Arbitrary-Generator (ARB).

@#* 25. Follow the Performance Test for OPT 002, Chapter 4 of the O/P Manual OPT 002 (08175-90016).

Dear

Re : Your order
for OPT 002 Upgrade Kit, part number 08175-68701 / 08175-68702

Thank you very much for the above order. This letter is just to remind you that, when modified, your **HP8175A** will not only include the **ARBITRARY WAVEFORM GENERATOR** Option, but will be compatible with current models, i. e., the data file format will be changed.

This means, any data stored in the HP8175A will be lost. Also, any data files set up on disc either with the HP8175A as controller, or with an external controller, will no longer be readable!

To help you nevertheless use these files, a program will be returned with your modified **HP8175A** to convert the data.

The program is recorded on a 3.5" disc, and will run on any HP200/300 Series Computer with BASIC 3.0 . The disc is single-sided formatted.

Brief Operating Instructions are included with the disc for use with HP Series 200 Model 9816 Computer. For other HP Series 200/300 computers, you may have to modify the operating procedure a little. If you have no HP Series 200/300 computer available, you may have to modify the program.

Here's what we suggest you do: if you have data in the **HP8175A** which you need, store it on a 3.5" disc if you have not already done so. Probably the easiest way is to use the **HP8175A** as system controller and store under HP8175A file type "all". Then get in touch with us to proceed with the modification. In the interest of protecting your data we will NOT proceed with the modification until we hear from you.

Yours faithfully,

8175A VERICAL REV. 4.0

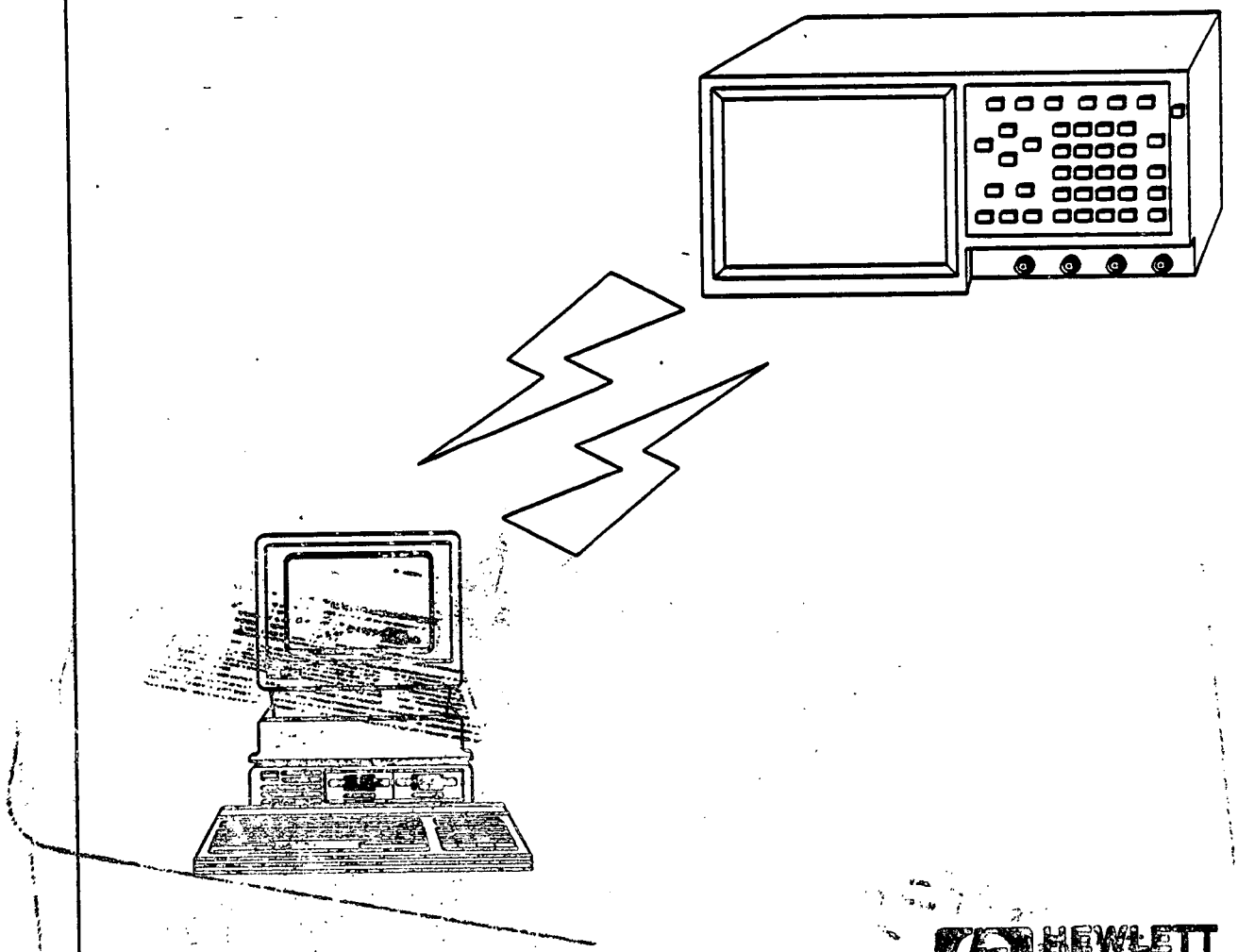
BUGS:

1.) DATA CAPACITY TEST USING 5335A COUNTER/54111D SCOPE 54111D RECOGNIZES SIGNAL OK THEN PROGRAM MOVES SIGNAL TO INPUT OF 5335A AND BEGINS COUNT, CONTINUES FOR OVER 1/2 HOUR WONT COME OUT OF LOOP.

2.) PATTERN DURATION TEST WITH SERIAL CLOCK, SYNCHRONOUS OR ASYNCHRONOUS MODE, HANGS UP AFTER 5335A TRIG. LEVEL IS SET, GOES TO TALK MODE AND REMOTE LED GOES OUT.

3.) REPORT FROM HP MTN. VIEW IS THAT LEVEL TEST AND TRISTATE TEST WONT WORK BECAUSE 8161A WILL ONLY OUTPUT 5V, TEST CALLS FOR 9V WHICH THE 8112A WILL PROVIDE (USED IN REV. 2.0 VERSION)

LEARN STRINGS: KEY TO FAST UPDATES ON THE HP 8175A



HEWLETT PACKARD

TABLE OF CONTENTS

INTRODUCTION

Learn Strings are simply strings of data produced by the HP 8175A that contain information about its current state (e.g. data in each address, timing, program page, control, etc.). Because these are simply binary strings, they can be transferred very quickly between a computer and the HP 8175A. One application would be to send a waveform from some other device (e.g. HP 1635 Logic Analyzer) thru a computer, to the HP 8175A for storage and later generation. Or, a large number of learn strings, each containing data for a different signal, could be stored on the computer's disk drive and rapidly sent back down to any software location or directly to hardware during a testing cycle. The computer could then be programmed to run any series of test signals automatically.

This guide outlines various methods of learn string transfers in both BASIC and PASCAL and includes a few sample programs to show examples of the exact syntax used in the commands (which can get tricky). Also, there is a brief description of what is actually in various learn strings so that you could conceivably produce your own (or better, alter existing) learn strings in a computer and then send the resulting waveform down to the HP 8175A.

This document assumes you have thorough knowledge of the HP 8175A and at least some familiarity with programming it through an HP-IB interface from a computer. A fair knowledge of either PASCAL or BASIC is also necessary to understand the programming examples. A quick summary and review of remote programming techniques for the HP 8175A in both langauges is provided in the appendix. Good references for additional information are:

8175A Digital Signal Generator Operating and Programming Manual
BASIC 4.0 Language Reference Manual
HP PASCAL Language Reference Manual
PASCAL 3.1 Procedure Library Manual (particularly the first 9 chapters over I/O techniques).

TYPES OF LEARN STRINGS

The are 4 major learn strings that can be accessed on every HP 8175A:

Mnemonic	Information Contained
TD	Timing and Data, Program Page
TF	Output Flags
TQ	Input Trigger Words
SET	Entire Parameter Set

In addition, on HP 8175A with Option 002 (Arbitrary Waveform Generator), there is one additional string for the calculator:

CLC	Arbitrary Waveform Calculator Module

PULLING LEARN STRING FROM THE HP 8175A

To pull one of these string from the HP 8175A into the computer, the computer must send a query message asking for it. The message is itself a string consisting of simply the appropriate mnemonic followed by a question mark and the memory location to pull the string from. The following commands will request the Timing and Data string from all possible locations:

TD?0	Timing and Data in ACTUAL memory
TD?1	Timing and Data in location 1 (denoted LOC1 on System Storage page)
TD?2	Timing and Data in location 2 (denoted LOC2 on System Storage page)
TD?3	Timing and Data of ACTUAL memory set, but directly from hardware

The first three locations (0-2) are simply software storage and the strings pulled from each have identical formats. Location 3, however, comes preformatted from the hardware and thus is very different. Therefore, even though the information is the same, strings pulled from locations 0, 1, or 2 can not be sent back to location 3 on the HP 8175A and vice versa.

The strings TD, TF, and TQ can all be pulled from any of the four locations (0-3). The SET string can only be pulled from the first three software locations (0-2) and not directly from hardware (3). The CLC string can only be pulled from ACTUAL memory (0) because it is never stored in either of the other two software locations, nor on the hardware.

Below are all possible strings that can be received or sent and their lengths:

Query String	Location	Length (bytes)
TD?	0/1/2	8787
	3	5897
TF?	0/1/2	300
	3	516*
TQ?	0/1/2	69
	3	516*
SET?	0/1/2	10244
CLC?	0	799

*These two strings, TF and TQ, when pulled from hardware (location 3) are actually identical because on hardware, the output flags from TF are directly linked to the input trigger patterns from TQ that they are associated with. Thus, on hardware, the two strings are massaged into one longer string which can be pulled up with either TF?3 or TQ?3.

SENDING LEARN STRINGS TO THE HP 8175A

To return the strings back to the HP 8175A, the same mnemonics for each string are used (without the question mark, of course). This is followed directly by the location, a comma, and then the learn string to be returned. It is very important that all this be sent without any end-of-line characters or other terminators separating the various parts. The following is an example with TD again. Here it is assumed that Soft$ contains a learn string from one of the three software locations (0-2) and that Hard$ contains a learn string from the hardware location:

TD0, Soft$	Sends string to ACTUAL memory location
TD1, Soft$	Sends string to memory storage location 1
TD2, Soft$	Sends string to memory storage location 2
TD3, Hard$	Sends string to ACTUAL location, but directly to hardware

Note that the same string could be sent to all three software locations, but not to the hardware.

PROGRAMMING EXAMPLES

Following are various examples of how to pull learn strings from an HP 8175A, store them in a disk file, and send them back. They are intended only to be examples, not actual application, and it is assumed you can pick and choose what you need from each for your own use. The programs are fairly short (although the listings here are filled with comments to make them clear, and thus look long) and show only some of the more basic techniques for I/O with the HP 8175A. For more advanced applications, please refer to the manuals suggested in the Introduction.

I/O WITH STRING VARIABLES

Since the learn strings are really just a series of bytes, it is convenient to store them in a string variable where each element can be accessed individually. Unfortunately, this technique is only really practical in BASIC as PASCAL limits its string length to 255 characters, shorter than most of the learn strings on the HP 8175A. Therefore, only BASIC examples are given here.

Below is a program that simply pulls a string from the HP 8175A and writes it to a disk file called LEARN. (NOTE: Be sure that the file LEARN does not already exist on your disk as this program will try to CREATE it and it is an error to CREATE a file that already exists in BASIC):

```
10    !This program pulls up a learn string and stores it to disk using
20    !string variables.
30 DIM B$[10250]
40    !Dimension a string big enough for any learn string
50 CREATE ASCII "LEARN",45
60    !Create an ASCII file large enough to hold string on disk
70    !If file already exists, an error is generated.  Existing files need only
80    !be opened with the ASSIGN statement below
90 ASSIGN @Fil TO "LEARN"
100 ASSIGN @Arb TO 720
110   !Establish IO paths for the file and the HP 8175A (at address 720 on HPIB)
120 PRINT "GETTING LEARN STRING . . ."
130 OUTPUT @Arb;"SET?0"
140   !Query HP 8175A to send a learn string over
150 ENTER @Arb USING "-K";B$
160    !Enter string from HP 8175A.  The USING statement insures string won't
170    !terminate on a LF or CR character.  Will wait for end signal from Arb
180 OUTPUT @Arb;"LO"
190    !Return HP 8175A to Local control
200 PRINT "STRING LENGTH = ";LEN(B$)
210 PRINT "WRITING STRING TO FILE . . ."
220 OUTPUT @Fil;B$
230    !Write string out to file
240 ASSIGN @Fil TO *
250    !Close file
260 PRINT "FINISHED"
270 END
```

The comments in the program are hopefully clear enough, but a couple of things are worth noting. The OUTPUT statements here all contain complete commands so they must be terminated by an end-of-line character. OUTPUT does this automatically unless a trailing semicolon is put after the statement to suppress it. This will be very important in the next example.

The ENTER statement in line 150 is what actually accepts the learn string from the HP 8175A into the string variable B$. The USING "-K" option is necessary to keep the input from ending prematurely if one of the characters in the string happens to be a Line Feed or Carriage Return. With this option, all characters sent are entered directly into the string until the HP 8175A sends an end of transmission signal.

The next example reads the string just stored in the disk file LEARN and sends it back to the HP 8175A

```
10     !This program retrieves a previously stored learn string from disk and
20     !sends it down to the HP 8175A using string variables.
30 DIM B$[10250]
40     !Dimension a string big enough for any learn string
50 ASSIGN @Fil TO "LEARN"
60 ASSIGN @Arb TO 720
70     !Establish IO paths for the file and HP 8175A (at address 720 on the HPIB)
80 PRINT "READING FILE . . ."
90 ENTER @Fil;B$
100    !Get string from disk file
110 PRINT "STRING LENGTH = ";LEN(B$)
120 PRINT "SENDING TO HP 8175A . . ."
130 OUTPUT @Arb;"SET0,";B$;
140    !Send it to the HP 8175A.  Note the semicolon separating the header
150    !string and B$ and the one trailing.  These suppress CR/LF and are ab-
160    !solutely necessary or all data sent is lost.  Alternatively, the header
170    !could be appended to the beginning of B$ directly: B$="SET0,"&B$
180    !The two can also be output separately, but the trailing semicolons must
190    !remain: OUTPUT @Arb;"SET0,";    OUTPUT @Arb;B$;
200 OUTPUT @Arb;"LO"
210    !Return HP 8175A to Local control
220 ASSIGN @Fil TO *
230    !Close file
240 PRINT "FINISHED"
250 END
```

Note here the ENTER statement is used without the USING option because it is retrieving the string from a disk file and the option is unnecessary. The statement simply loads the string variable B$ with all data from the file until it reaches the end of file or fills the string.

The OUTPUT statement in line 130 is an example of the use of a trailing semicolon to suppress the end of line character. Note also the semicolon between the header string ("SET0,") and the learn string itself, assuring that the whole string is sent as continuous data. As mentioned in the comment, this could have also been sent with separate statements (both with trailing semicolons) or as one string.

Both of these programs were made very general on purpose so they could be used to pull up any learn string from any location simply by changing the query/header strings sent. For example, to pull up the flags directly from the hardware, simply change the OUTPUT statement in line 130 of the first program so it sends the query string "TF?3" instead of "SET?0". Similarly, to send this string back, change the header string of the OUTPUT statement in line 130 of the second program to send "TF3," instead of "SET0,". Of course, to save memory, it would also be a good idea to change the string dimension of B$ so that it is just the right size for the learn string you require.

I/O WITH BUFFERS

Using buffers to transmit and receive learn strings can be faster than normal string variables and it allows much larger strings to be transmitted. Once in a buffer, the contents can be read into an array in PASCAL to access the individual bytes or to write to a file. In BASIC the buffer can be transferred directly to a file and, if the buffer is named, the individual elements can be accessed through the variable name. For more detailed information on buffers, see the BASIC Language Reference Manual or the PASCAL 3.1 Procedure Library Manual.

In the following BASIC program (see next page), a string is read from the HP 8175A into a buffer named B$ and then transfered directly into a disk file. Then, when you press the CONTINUE softkey, the program retrieves the learn string from the file and sends it back to the HP 8175A. (NOTE: Here again, make sure LEARN does not already exist on your disk as this will generate an error when this program tries to CREATE it.)

A few things worth noting about the program are:

The file created here must be a BDAT, not ASCII, as only this file type is allowed in transfer operations.

The program uses OUTPUT again in line 160 to query for the desired learn string, but then brings it in using TRANSFER. The first one (line 180) transfers data from the HP 8175A to the buffer; simultaneously, the second one (line 220) is transfering the same data into the file. The two TRANSFERS are overlapping, so they can not only fill the buffer from the HP 8175A and empty it into the file at the same time, but the program could also continue doing other things while they were running. In this case, however, it must wait for them to finish because the next statement (line 270) can't output the Local command until the interface is free.

Line 350 sends the header string (note the trailing semicolon) to prepare the HP 8175A for the return of the learn string. Then lines 430 and 460 use another pair of overlapping TRANSFER's to get the data from the file into the buffer and then into the HP 8175A.

Note the comments under each TRANSFER statement as they often give alternate methods which might fit your application more appropriately. Again, this program can use any learn string by simply changing the "SET" header and query strings.

```
10   ! This program pulls a learn string from the HP 8175A, stores it to disk
20   ! and then sends it back.  All transfers are done with buffers.
30 DIM B$[10250] BUFFER
40    !Dimension a Buffer big enough for any learn string
50 CREATE BDAT "LEARN",1,10250
60    !Create a Binay Data file on disk to hold learn string
70    !If the file already exists, an error will be generated. Old files
80    !only need to be opened with the ASSIGN statement below.
90 ASSIGN @Buf TO BUFFER B$
100 ASSIGN @Arb TO 720
110 ASSIGN @Fil TO "LEARN";FORMAT ON
120   !Establish IO paths for the Buffer, the HP 8175A and the File
130   !Note: 720 is the address of the HP 8175A on the HP-IB interface
140   !      FORMAT ON specifies file will be ASCII codes
150 PRINT "GETTING A LEARN STRING FROM HP 8175A . . ."
160 OUTPUT @Arb;"SET?0"
170    !Query HP 8175A for a learn string
180 TRANSFER @Arb TO @Buf;END
190    !Transfer data from HP 8175A to the Buffer until END signal is received
200    !from the HP 8175A.  Could also use a COUNT transfer if you know the
210    !exact string size:  TRANSFER @Arb TO @Buf;COUNT Bufsize
220 TRANSFER @Buf TO @Fil;END
230    !Transfer the contents of the buffer into the file. END updates the EOF
240    !(End Of File) pointer when transfer is complete (i.e. buffer empty)
250    !Note that these transfers are overlapping; data flows into the buffer
260    !form the Arb and out of the buffer into the file at the same time.
270 OUTPUT @Arb;"LO"
280    !Return HP 8175A to Local mode after transfers are complete
290 ASSIGN @Fil TO *
300    !Close file on disk
310 PRINT "GOT IT.  WAITING--HIT CONTINUE"
320 PAUSE
330 ASSIGN @Fil TO "LEARN"
340 PRINT "SENDING LEARN STRING BACK . . ."
350 OUTPUT @Arb;"PRE"
360    !Reset HP 8175A to standard settings (not really necessary)
370 OUTPUT @Arb;"SET0,";
380    !Prepare HP 8175A for the string to be sent back.  The trailing semicolon
390    !is very necessary to suppress the CR/LF normally sent by OUTPUT
400    !Alternatively, this string could be written directly to the buffer
410    !before reading data from the file:  OUTPUT @Buf;"SET0,";
420    !Then the whole thing would be transfered directly
430 TRANSFER @Fil TO @Buf;END
440    !Transfer data from file to the buffer until EOF is reached. (A COUNT
450    !transfer as above could also be used here.)
460 TRANSFER @Buf TO @Arb
470    !Send data from buffer to HP 8175A until buffer is empty.  Do NOT use
480    !an END transfer for this as that terminates with CR/LF, causing an
490    !error and complete loss of data sent.  Transfers are overlapping.
500 OUTPUT @Arb;"LO"
510 ASSIGN @Fil TO *
520 PRINT "FINISHED"
530 END
```

The next program is in PASCAL and contains two procedure to do the transfering in both directions: From_Arb_to_Disk and From_Disk_to_Arb. The main body of the program simply serves to call each of these at appropriate times and print messages to the screen. (NOTE: In PASCAL, if the filename used (here called SomeFile) already exists, it will simply be overwritten with no warning given!):

```
program LearnStrings (input,output);
{Contains procedures to pull a learn string from the HP 8175A and store it in
 a disk file.  This same is string is then pulled off the disk and sent back
 to the HP 8175A.  All transfers are done with buffers.}

  import        iodeclarations,          {General IO functions - see the Pascal}
                general_1,               {3.1 Workstation System Manual for     }
                general_2,               {information on each.                  }
                general_4;

  const BufSize = 10250;          {Large enough for any learn string}
        Arb = 720;                {Address of HP 8175A on HP-IB interface}

  var   c:char;


procedure From_Arb_to_Disk;
{Transfers Learn string from HP 8175A and stores in a disk file}

  type  Storage = packed array [1..BufSize] of char;

  var   BufName:buf_info_type;
        StoreArray:Storage;
        f:file of Storage;
        MaxSize, pos:integer;
        A_Char:char;

begin
  iobuffer (BufName,BufSize);           {Allocate buffer space}
  buffer_reset (BufName);               {Clear buffer}

  writestringln (Arb,'SET?0');          {Query for Learn String}
  transfer_end (Arb,serial_fastest,To_Memory,BufName);
               {Pulls in all data sent from HP-8175A until an end signal is
                received.  Could also use a count transfer if exact size known:
                transfer (Arb,serial_fastest,To_Memory,BufName,BufSize);}

  writestringln (Arb,'LO');             {Returns HP 8175A to Local mode}

  MaxSize:=buffer_data(BufName);        {Find exact size of buffer}
  write ('String length = ',MaxSize:1,' . . ');
  for pos:=1 to MaxSize do begin        {Read all characters out of the buffer}
    readbuffer (BufName,A_Char);        {and store them in a packed array.     }
    StoreArray[pos]:=A_Char;
  end;

  open (f,'SomeFile');          {Create an actual disk file associated with f}
                                {Overwrites 'SomeFile' if it already exists!!}
  write (f,StoreArray);         {Write the packed array to it}
  close (f,'lock');             {Close the file and make it permanent ('lock')}
end;
```

```
procedure From_Disk_to_Arb;
{This procedure takes a learn string previously stored on disk and sends it
 down to the HP 8175A}

  type  Storage = packed array [1..BufSize] of char;

  var   BufName:buf_info_type;
        StoreArray:Storage;
        f:file of Storage;
        pos:integer;

begin
  iobuffer (BufName,BufSize);           {Allocate Buffer space}
  buffer_reset (BufName);               {Clear Buffer}

  open (f,'SomeFile');          {Open a file containing a learn string}
  read (f,StoreArray);          {Read file into array}
  close (f,'lock');             {Close file}

  for pos:=1 to ord(StoreArray[3])*256+ord(StoreArray[4])+4 do
    writebuffer (BufName,StoreArray[pos]);
                {Write each character into the buffer.  Note that bytes 3 and
                 4 in every learn string contain the number of active bytes in
                 the string (plus 4 bytes for the header). Byte 3 is MSB}

  write ('String Length = ',buffer_data(BufName):1,' . . ');
  writestring (Arb,'SET0,');    {Prepares HP 8175A for data transfer. Note that
                                 writestring does NOT send a CR/LF!
                                 Alternatively, this could have been put in the
                                 buffer directly before the data:
                                   writebuffer_string (BufName,'SET0,');}

  transfer (Arb,serial_fastest,From_Memory,BufName,buffer_data(BufName));
           {Here the count transfer must be used to suppress any CR/LF}
  writestringln (Arb,'LO');     {Return HP 8175A to Local mode}
end;


{MAIN program}

begin
  ioinitialize;         {Reset all interfaces}

  write ('Bringing in a learn string from Arb . . . ');
  From_Arb_to_Disk;
  writeln ('finished.');   writeln('    Hit Return');
  read (c);

  write ('Sending learn string back to Arb . . . ');
  From_Disk_to_Arb;
  writeln ('finished.');   writeln('    Hit Return');
  read (c);

  iouninitialize;       {Reset all interfaces for program end}
end.
```

First, note the modules imported at the beginning--these all come from the PASCAL system IO library, which must thus be accessible when running the program. The best way to do this is to P-load this library into memory (with the P command) before attempting to execute the program.

The **ioinitialize/iouninitialize** pair bracketing the MAIN program simply clear the interfaces (i.e. the HP-IB) before starting/finishing I/O operations. It is a good idea to use these around any program that does I/O, but beware of calling them too quickly after your last input or output statement as they immediately clear all data on the interface, so your last statement might not get through in time.

Instead of BASIC's OUTPUT statement, PASCAL uses two separate statements: **writestring** and **writestringln**. The first acts like OUTPUT with a trailing semicolon, that is, no end of line characters are sent. The second is like a normal OUTPUT and does send an end of line character. PASCAL also offers a wide variety of other output (and input) statements described in the PASCAL 3.1 Procedure Library.

In **procedure From_Arb_to_Disk**, the buffer is first created (**iobuffer**) and then cleared (**buffer_reset**). The query string is sent with **writestringln** and then a **transfer_end** is used to bring all the data into the buffer. This statement will not terminate until the buffer is full or the HP 8175A sends an end of transmission signal.

Unlike BASIC, PASCAL does not allow the buffer to be transferred directly to a file, so it is first read into a packed array (**readbuffer**) and then this array is written to a file declared to be of the appropriate type.

In **procedure From_Disk_to_Arb**, the reverse process is done. First the file is read back into the array and then **writebuffer** reads it back into a buffer. This loop takes advantage of the fact that the third and fourth bytes of every learn string contain the total length of the string and uses this to set its upper limit (see the CONTENTS OF A LEARN STRING section of this manual).

A **writestring** then sends the header string to the HP 8175A (without an end of line) and the **transfer** sends all of the data in the buffer. Again, the **_end** suffix is not used here because that would send an end of line. Instead, a count transfer sends over the specified number of bytes.

Both of these transfers were serial; that is, the program must wait for them to be completed before continuing. PASCAL also supports overlap transfers. Refer to the PASCAL 3.1 Procedure Library Manual for information on all types of transfers and buffers.

One last thing to note about buffers in both PASCAL and BASIC is that they use dynamic variable space and pointers. Both languages have various routines to dispose of these pointers when the buffers are no longer needed so that this memory can be reclaimed for other uses. Refer to the appropriate Language manuals to determine what type of dispose might be best suited for your application.

CONTENTS OF A LEARN STRING

This section gives an overview of the structure of learn strings, as well as a detailed look at how data is stored in certain sections of the learn strings. With this information, you can easily alter a string in the computer to produce your own data, timing, trigger, and flag patterns to be sent back to the HP 8175A. Although the strings also contain various information over other parameters, such as programming, output control page, etc., this information is stored in large linked lists making it very difficult to alter correctly. It is recommended that for these changes, normal programming methods be used as they will invariably prove to be at least as fast, far more intuitive, and less error prone.

HEADER

All of the learn strings begin with a four byte header of the following form:

Byte	Value
1	35 ("#")
2	65 ("A")
3	MSB of length of string to follow
4	LSB of length of string to follow

So the first two bytes of every learn string are "#A", indicating that a binary string is to follow. The next two bytes indicate the string length. Note that when the length is computed from these bytes (i.e. Length=(Byte 3)*256+(Byte 4)), it only counts the number of "active" bytes following the header. The total length of the learn string then (as given in Types of Learn Strings section) is actually this number plus 4 for the four bytes of header on each.

After this header in all of the strings except for SET, the data begins immediately. In SET, two check sum bytes are sent directly after the length bytes (bytes 5 and 6) and then the data begins. These check sums are not trivial to calculate and if they are off, none of the data will be accepted by the HP 8175A. Furthermore, almost any changes you might want to make to data on the HP 8175A can be done through the other learn strings much more easily, so it is not recommended that this string be altered. It is, however, still a useful string to transfer back and forth for storage purposes because it does contain ALL of the current settings on the HP 8175A, so it can be used to quickly change from one test signal to another.

TD STRING - SOFTWARE LOCATIONS

The general structure of this string when taken from one of the software locations (i.e. Location 0-2) is as follows:

Byte Start	Length/Form	Contents
1	4 bytes	Header string
5	1024 x 6 bytes	Timing and Data
6149	6 bytes	Unused
6155	50 x 5 bytes	Label list
6405	1 byte	Timing type
6406	2 bytes	Fixed timing duration
6408	4 x 2 bytes	Program header
6416	255 x 9 bytes	Program page
8711	10 x 5 bytes	Program labels
8761	4 x 2 bytes	Program vector
8769	19 bytes	Mode and Control information
Total:	8787 bytes	

As mentioned before, the programming and mode information is in a linked list structure making it very difficult to change, so its contents will not be discussed here (bytes 6408-8787).

TIMING AND DATA: By far the most useful part of all the learn strings is this section on the timing and data information. This is where learn strings can be used to their greatest advantage when trying to save time in transfering data.

There are 6 bytes assigned to each programming address (0-1023) on the HP 8175A. They contain:

Bytes	Contents
1-3	Data for Pods 2-0
4-5	Variable timing duration
6	Label number

Data for Pods:

These 3 bytes can be read right off the data format page. Note that the order of the pods is also the same as on this page; that is, byte 1=POD 2, byte 2=POD 1, and byte 3=POD 0. The significance of each bit, of course, depends on the configuration being used:

Parallel Configuration: Each bit position corresponds directly to the given channel on the given pod.

Serial Configuration: Byte 1 (POD 2) is data for Serial B. Byte 2 (POD 1) is Serial A. Byte 3 is unused.

Arbitrary Waveform Configuration (Option 002): For this configuration, it is easier to forget about the three byte designations and simply number the bits from 1 to 24 in the same order they are displayed on the Data Format Page:

	Byte 1								Byte 2								Byte 3							
OLD:	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
NEW:	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
	_____ARB B_____/								_____ARB A_____/										CP B.	TR B.	CP A.	TR A.

The first 10 bits are Arb channel B. The next 10 are Arb channel A. The last 4 bits contain trigger and characteristic point information as follows:

Bit Number	Meaning
21	Characteristic Point, Arb B
22	Trigger, Arb B
23	Characteristic Point, Arb A
24	Trigger, Arb A

For the characteritic point bits, if the bit is set (=1), that point is considered a characteristic point by the Arb interpolator; unset (=0) indicates a "normal" point.

Variable Timing:

These two bytes contain the duration of this point when variable timing mode is used. The structure is as follows:

Byte 4								Byte 5							
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
_D2_/				_D1_/				_D0_/				DPt		Unit	

The first 3 half-bytes contain the three digits of the time duration (in Binary Coded Decimal form). Bits 3 and 2 of Byte 5 hold the position of the decimal point. The number they form (either 1, 2, or 3) indicates the number of digits to the left of the decimal point. The last two bits are the unit number:

Bit Value	Unit
1	uS (micro-seconds)
2	mS (milli-seconds)
3	S (seconds)

Label:

This is simply a number between 1 and 50 indicating what label is currently assigned to this memory address. If no label is assigned, the byte is zero.

LABEL LIST: This is a list (in ASCII) of up to 50 label names currently assigned to various memory addresses. Each name is 5 characters long, so to determine what label is at a given address, simply take the Label Number (byte 6 as describe above) minus 1, times 5 and this will be the position of the first character of the Label name in this list.

TIMING TYPE: This byte just indicates whether fixed or variable timing is currently being used. A 0 here means fixed mode; a 1 means variable mode.

FIXED TIMING DURATION: These two bytes hold the value assigned to all memory addresses when in the fixed timing mode. The time value is stored in exactly the same format as described above for Variable Timing.

TD STRING - HARDWARE LOCATION

The general structure of the TD string when taken directly from hardware (location 3) is as follows:

Byte Start	Length/Form	Contents
1	4 bytes	Header
5	1024 x 5 bytes	Timing and Data information
5125	255 x 3 bytes	Program page
5890	4 x 2 bytes	Program vector
Total:	5897 bytes	

TIMING AND DATA: Note now there are only five bytes for each memory address, instead of the six used in software, because the label byte is not used at the hardware.

The first three bytes contain the POD data in the same format as described for the software locations, except that the first and third bytes have now exchanged places:

Software Byte		Hardware Byte
Byte 1	⟹	Byte 3
Byte 2	⟹	Byte 2
Byte 3	⟹	Byte 1

Bytes 4 and 5 now hold the actual timing value that is being used for this point, whether that be the fixed value or the variable value. The format however is very different from that used in software:

Byte 5		Byte 4 (Note order of bytes shown)
7 6 5 4 3 2 1 0		7 6 5 4 3 2 1 0
0 0 0 Range	_____	Timing Value _____ /

It is best described by a procedure for converting the software version to the hardware one:

1. Determine Range of Duration:

Duration value between:	Range Number (Bits 2-4, Byte 5):
0.02 uS . . . 9.99 uS	4
10 uS . . . 999 uS	3
1.0 mS . . . 99.9 mS	1
0.1 S . . . 9.99 S	2

2. Convert the three-digit binary coded decimal number representing the time into a normal binary number (ignore the decimal point). This will result in a 10 bit number which will become the timing value after more manipulation.

3. Take the 2's Complement of the 10 bit timing value you just found. This is done by complementing every bit in the number (i.e. change all 1's to 0's and all 0's to 1's) and then add 1 to the resulting number.

4. Finally, if the time value was in the smallest range in step 1 above (i.e. the Range Number was 4), add 1 again to the now complemented timing value.

Now simply use binary operations to put the Timing Value and Range Number in their respective places in Bytes 4 and 5. Note that the top three bits of Byte 5 (5-7) should be set to 0 always.

To make this a little more concrete, let's go through the procedure for the default value of 0.02 uS. In software form, this is stored as:

	Byte 4	Byte 5
Bit:	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0
Value:	0 0 0 0 0 0 0 0	0 0 1 0 0 1 0 1
Decimal:	0	37

Step 1: Determine the range from the table. For 0.02 uS, the range number is 4, so we'll put this into the appropriate bits in the hardware form (and we will go ahead and set the top three bits to 0):

	Byte 5	Byte 4
Bit:	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0
Value:	0 0 0 1 0 0 _____	Timing Value _____ /
Decimal:	Undefined	

Step 2: Convert BCD time value to normal binary format (using 10 bits). Put these in the Timing Value position:

	Byte 5	Byte 4
Bit:	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0
Value:	0 0 0 1 0 0 0 0	0 0 0 0 0 0 1 0
Decimal:	16	2

Step 3: Take 2's complement of Timing Value (last 10 bits only!) Don't forget to add 1 after complementing all of the bits:

	Byte 5	Byte 4
Bit:	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0
Value:	0 0 0 1 0 0 1 1	1 1 1 1 1 1 1 0
Decimal:	19	254

Step 4: Since the timing value was in the lowest range, we need to add 1 to our final result:

	Byte 5	Byte 4
Bit:	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0
Value:	0 0 0 1 0 0 1 1	1 1 1 1 1 1 1 1
Decimal:	19	255

The resulting value is ready to be sent directly to the hardware location.

PROGRAMMING SECTION: As with the software location, changing the programming information with learn strings is too complex to be efficient, so it is suggested normal programming methods be used instead.

TF STRING - SOFTWARE LOCATIONS

The general structure of this string when pulled from one of the three software locations (Locations 0-2) is as follows:

Byte Start	Length/Form	Contents
1	4 bytes	Header
5	256 bytes	Flag patterns associated with each trigger value
261	32 bytes	Latched bits
293	7 bytes	Static flag patterns
300	1 byte	Flag Mode
Total:	300 bytes	

FLAG PATTERNS: These are simply the 256 possible flags that are output on given trigger patterns. They are found on the Control Page Flag Assignment menu on the HP 8175A. Each byte of the learn string simply contains one flag pattern associated with a trigger pattern (0-255).

LATCHED BITS: When the Flag mode is set to Latched, an additional column of bits appears to the right of the column of flags on the Flag Assignment menu. Each bit position holds either a "*", meaning enabled for latching, or a ".", meaning disabled. These correspond to 1's and 0's respectively in the 256 bits contained in these 32 bytes. So starting with Byte 1, bit 0 and continuing to Byte 32, bit 7, every set bit means an enabled flag; every zero bit means a disabled flag (in the Latched mode).

STATIC FLAGS: When in Static Flag mode, only seven flag patterns are set to correspond with the seven trigger functions found on the Control Page Simulate Trigger Functions menu. These seven bytes contain the flag values starting with START through TRIST off.

FLAG MODE: Indicates the current flag mode being used:

Value in Byte	Flag Mode
0	Transparent
1	Latched
2	Static

TF STRING - HARDWARE

The general structure of this string when pulled directly from the hardware location (Location 3) is as follows:

Byte Start	Length/Form	Contents
1	4 bytes	Header
5	256 bytes	Output Flag Patterns
261	256 bytes	Trigger funtions
Total:	516 bytes	

FLAG PATTERNS: These bytes are the same as the Flag Patterns discussed for the software locations The only difference is that in the Latched mode, only those flag patterns which are actually enabled for latching are stored on the hardware; the other flags are set to zero.

TRIGGER FUNCTIONS: These 256 bytes contain one of 8 numbers which indicates what trigger function is associated with each trigger value (0-255). This is determined from the Input Trigger Word Assignment Menu. The possible values are:

Value in byte:	Trigger Function:
32	Start
64	Stop
96	Continue
128	JMP A
160	JMP B
192	Tristate on
224	Tristate off
8	Tristate asyn.

TQ STRING - SOFTWARE LOCATIONS

The general structure of this string when taken from one of the three software locations (Location 0-2) is as follows:

Byte Start	Length/Form	Contents
1	4 bytes	Header
5	8 x 8 bytes	Input Trigger Words
69	1 byte	Number of additional Trigger Words
Total:	69 bytes	

INPUT TRIGGER: These are the trigger words used to initiate each of the eight functions (START thru TRISTATE asyn.) found on the Input Trigger Word Assignment Page. The 8 bytes for each function are broken down into 4 byte pairs, one pair for each possible trigger word associated with the function.

In each pair, the first byte acts as a control byte to indicate which of the bits (if any) in the trigger word are variable (shown as an 'X' on the HP 8175A). Any bit that is set in this byte indicates this bit is not variable (i.e. it is either a '1' or a '0' on the Assignment page). An unset bit indicates an 'X' in the trigger word, a variable bit.

The second byte in the pair is the actual trigger word containing the patterns of 0 and 1 used to define the trigger. Note here all X's are coded as normal set bits (1's).

ADDITIONAL PATTERNS: This byte simply holds the number of additional trigger words (i.e. the number more than the required 1) used to define each function. This can vary between 0 and 3, standing for 1 thru 4 trigger words respectively.

TQ STRING - HARDWARE LOCATION

As discussed earlier, this string is exactly identical to the TF string taken from the hardware location (Location 3) because the trigger words and output flags are linked on the hardware. Please refer to the TF STRING - HARDWARE LOCATION section for a description of the string's contents.

SET STRING - SOFTWARE LOCATIONS

This string is really just a conglomerate of all the previously described strings plus approximately 2000 bytes of control information defining all aspects of the current HP 8175A state. This information is stored in a linked list, making it very difficult to alter. Also all data is controlled by two checksum bytes which would have to be recalculated should any of the data be changed. For these reasons, it is recommended this string be used only to transfer the state of the HP 8175A back and forth to a computer for storage or automatic programming and that no data in it be changed.

The general structure is as follows:

Byte Start	Length/Form	Contents
1	4 bytes	Header
5	2 bytes	CheckSum
7	8783 bytes	TD String
8790	142 bytes	Control information
8932	296 bytes	TF String
9228	10 bytes	Control information
9238	65 bytes	TQ String
9303	942 bytes	Control information
Total:	10244 bytes	

The structure of each sub-string contained within the SET string is the same as when it is called up alone (minus the 4 header bytes on each). Note that the SET string can only be pulled up from the software locations (Location 0-2).

CLC STRING - LOCATION 0

As indicated, this string can only be pulled from the ACTUAL location since it is never stored in any of the other software location nor on the hardware. As with the programming modules, its form is fairly, so it should be used just for transferring modules back and forth for storage in the computer.

CHANGING LEARN STRINGS

It is highly recommended that you do not try to build an entire learn string yourself as this is too error prone and, in many cases, not enough information has been given to completely construct all parts of the string. Instead, it is better to pull up the string from the HP 8175A that contains the data you want to change, make the changes on the appropriate part, leaving the rest of the string untouched, and return the altered string back to the HP 8175A.

MORE PROGRAMMING EXAMPLES

Although the changing of timing and data information in most of the learn strings is fairly straight forward, it can become tricky in certain cases. To help make some of these procedures a little clearer, three programming examples follow covering some of the more complicated operations. Note that these are meant only as examples and they assume all entered data will be error free.

Changing data in the ARB A or ARB B channel using the TD string requires some delicate binary operations to place each bit correctly without destroying the rest of the string. The following PASCAL program (see next two pages) loads all of the data from an array into either channel A or B using binary operations to place the bits in the proper place in the string. It also sets the trigger points for each from a separate array and sets some of the points to characteristic points.

The documentation within the program should clear up most questions on what operations are being performed. Refer to the reference texts listed in the introduction for more help.

```
program ArbString (input,output);
{PUTS DATA FROM A STORAGE ARRAY INTO EITHER CHANNEL A OR B ON THE HP 8175A
 ARBITRARY WAVEFORM GENERATOR.}

{LIBRARY MODULES NEEDED}
import  IODECLARATIONS,          {Buf_Info_Type,Serial_Fastest,
                                  From_Memory,To_Memory}
        GENERAL_1,               {ioinitialize,iouninitialize}
        GENERAL_2,               {writestringln}
        GENERAL_4,               {iobuffer,buffer_reset,buffer_data,
                                  readbuffer_string,writebuffer_string,
                                  transfer,transfer_end}
        IOCOMASM;                {binand,binior}

  const Arb=720;         {ADDRESS OF HP 8175A ON HP-IB INTERFACE}
        Channel='A';     {CHANNEL TO PUT DATA INTO}

  type  DataStore = record                {SAMPLE DATA STORAGE}
                      Level:0..1023;      {VOLTAGE LEVEL (LIMITS IN DECIMAL)}
                      Trigger:0..1;       {TRIGGER POINT IS 0 OR 1}
                      SetCp:boolean;      {CHARACTERISTIC POINT?}
                    end;

  var   Data: array [0..1023] of DataStore;  {ARRAY HOLDING DATA FOR ALL
                                              1024 MEMORY POSITIONS}
        pos: integer;    {COUNTER}
        c: char;         {DUMMY VARIABLE TO PAUSE PROGRAM}



procedure ChangeData;
{ACTUALLY DOES THE BINARY OPERATIONS TO INSERT NEW DATA INTO A LEARN STRING}

  const BufSize = 8787;          {SIZE OF TD? LEARN STRING}

  var   bufold, bufnew: Buf_Info_Type;
        S:string[10];            {STRING TO HOLD EACH DATA SET}
        pos:integer;
        Free_Space:^integer;

begin   {CHANGEDATA}
  mark (Free_Space);     {MARK CURRENT TOP OF STACK FOR LATER RECOVERY}
  iobuffer (bufnew,BufSize);     {INITIALIZE BUFFERS}
  iobuffer (bufold,BufSize);
  buffer_reset(bufnew);          {CLEAR BUFFERS}
  buffer_reset(bufold);

  writeln ('Getting old data from Arb . . .');
  writestringln (Arb,'GEN2');    {PUT INTO ARBITRARY WAVEFORM CONFIG.}
  writestringln (Arb,'TD?0');    {QUERY FOR TD LEARN STRING}
  transfer_end (Arb,Serial_Fastest,To_Memory,bufold); {RECEIVE DATA}

  writebuffer_string (bufnew,'TD0,');   {START NEW BUFFER WITH RETURN STRING}
  readbuffer_string (bufold,S,4);      {TRANSFER HEADER INFORMATION FROM BUFOLD}
  writebuffer_string (bufnew,S);       {TO BUFNEW                              }
```

```
 writeln ('Changing to new data . . .');
 for pos:=0 to 1023 do with Data[pos] do begin
   readbuffer_string (bufold,S,6);   {READ OLD DATA INTO STRING}

   case Channel of
     'A':      begin          {PUT DATA INTO CHANNEL A}
                 S[2]:=chr(binand(ord(S[2]),192)+(Level div 16));
                 S[3]:=chr((Level mod 16)*16+(ord(S[3]) mod 16));
                              {SET BIT FOR CHARACTERISTIC POINT, IF NEEDED}
                 if SetCp then S[3]:=chr(binior(ord(S[3]),2))
                          else S[3]:=chr(binand(ord(S[3]),253));
                              {SET A TRIGGER POINT IF NEEDED}
                 if Trigger=1 then S[3]:=chr(binior(ord(S[3]),1))
                              else S[3]:=chr(binand(ord(S[3]),254));
               end;
     'B':      begin          {PUT DATA INTO CHANNEL B}
                 S[1]:=chr(Level div 4);
                 S[2]:=chr((Level mod 4)*64+(ord(S[2]) mod 64));
                              {CHARACTERISTIC POINT?}
                 if SetCp then S[3]:=chr(binior(ord(S[3]),8))
                          else S[3]:=chr(binand(ord(S[3]),247));
                              {TRIGGER POINT?}
                 if Trigger=1 then S[3]:=chr(binior(ord(S[3]),4))
                              else S[3]:=chr(binand(ord(S[3]),251));
               end;
   end;

   writebuffer_string (bufnew,S);   {WRITE CONVERTED STRING INTO NEW BUFFER}
 end;

 write ('Sending it back . . .');
 transfer (Arb,Serial_Fastest,From_Memory,bufnew,buffer_data(bufnew));
 transfer (Arb,Serial_Fastest,From_Memory,bufold,buffer_data(bufold));
          {SEND BACK NEW CONVERTED DATA (BUFNEW) AND THEN REMAINDER OF
           UNCHANGED LEARN STRING (BUFOLD)                          }
 writestringln (Arb,'LO');      {RETURN HP 8175A TO LOCAL}
 release (Free_Space);          {RELEASE TO PREVIOUSLY MARKED TOP OF STACK; THIS
                                 RECOVERS ALL DYNAMIC MEMORY USED BY THE BUFFERS}
end;    {CHANGEDATA}



{MAIN PROGRAM}
begin
  ioinitialize;          {READY ALL INTERFACES}
  writeln ('Initializing array . . .');

  for pos:=0 to 1023 do with Data[pos] do begin   {MAKE DATA ARRAY--SINE WAVE}
    Level:=round(511*sin(2*3.1415*pos/512)+512);
    if pos=0 then Trigger:=1 else Trigger:=0;     {MAKE FIRST POINT A TRIGGER}
    if (pos mod 4)=0 then SetCp:=true else SetCp:=false; {MAKE EVERY 4TH POINT}
                                                         {CHARACTERISTIC      }
  end;

  ChangeData;

  writeln ('finished.   Hit return to exit.');
  read (c);
  iouninitialize;        {RESET ALL INTERFACES}
end.
```

Another tricky procedure is the conversion of timing units from the form used in software to the form used in hardware in the TD string. The following program performs this conversion. Be careful when entering the time that you use the same format that the HP 8175A uses on its Data page Pattern/Level screen. Note you enter the three digits first, WITHOUT a decimal point, and then you are prompted to enter the position of the decimal point within this field:

```
program ConvertTime (input,output);
{CONVERTS TIME FROM SOFTWARE TO HARDWARE FORMAT}

import  IOCOMASM;       {32-BIT INTEGER, BINARY FUNCTIONS}

const   Zero = ord('0');        {USED TO CONVERT CHARACTER INPUT TO DIGITS}

type    TimeType = string[2];   {HOLDS A TWO BYTE TIME STRING}

var     SoftTime,HardTime:TimeType;
        x,DecPt,Unit:integer;
        Dig: array [1..3] of integer;
        InputChar:char;



function HardwareForm (Soft:TimeType):TimeType;
{DOES ACTUAL CONVERSION PROCESS}

  var   Hard: array [1..2] of integer;
        Time,Range: integer;
        TimeString: TimeType;

begin
  case binand (ord(Soft[2]),15) of      {STEP 1:FIND RANGE}
    5:          Range:=4;       {Time between: 0.02 uS ... 9.99 uS}
    13:         Range:=3;       {Time between:   10 uS ...  999 uS}
    10:         Range:=1;       {Time between:  1.0 mS ... 99.9 mS}
    7:          Range:=2;       {Time between:  0.1  S ... 9.99  S}
  end;

  Time:=(binand(ord(Soft[1]),240) div 16)*100+  {STEP 2:CONVERT TIME FROM BCD}
        binand(ord(Soft[1]),15)*10+             {TO NORMAL BINARY FORMAT}
        (binand(ord(Soft[2]),240) div 16);

  Time:=bincmp(Time)+1;                 {STEP 3:TAKE TWO'S COMPLEMENT}

  if Range=4 then Time:=Time+1;         {STEP 4:ADD 1 IF RANGE IS RIGHT}

  Hard[2]:=binand(Time,255);            {PUT ALL THE PARTS TOGETHER}
  Hard[1]:=binand(Time,768) div 256;
  Hard[1]:=binior(Hard[1],Range*4);

  strwrite(TimeString,1,x,chr(Hard[2]),chr(Hard[1]));   {BYTE ORDER!!}
  HardwareForm:=TimeString;     {RETURN THE NEW TIME STRING IN FUNCTION NAME}
end;
```

```
{MAIN PROGRAM}
begin
  write ('Enter a three digit time, without decimal point==> ');
  for x:=1 to 3 do begin
    read (InputChar);
    Dig[x]:=(ord(InputChar)-Zero);
  end;     writeln;

  write ('How many digits to the left of the decimal point? ');
  read (InputChar);   DecPt:=(ord(InputChar)-Zero);          writeln;

  write ('Choose Units:  1) uS   2) mS   3) S      Choose 1, 2 or 3==> ');
  read (InputChar);   Unit:=(ord(InputChar)-Zero);           writeln;

  SoftTime:='';          {PRODUCE SOFTWARE FORM OF TIME--BCD VALUE}
  strwrite(SoftTime,1,x,chr(Dig[1]*16+Dig[2]),chr(Dig[3]*16+DecPt*4+Unit));

  HardTime:=HardwareForm(SoftTime);      {CHANGE TO HARDWARE FORM}
  writeln;
  writeln ('Soft Form: ',ord(SoftTime[1]):1,' ',ord(SoftTime[2]):1);
  writeln ('Hard Form: ',ord(HardTime[1]):1,' ',ord(HardTime[2]):1);
end.
```

Finally, for the sake of completeness, the following routine computes the check sum bytes used in the SET string to insure the integrity of the data string. To make the example simple, a SET string is simply pulled from the HP 8175A and the checksum bytes are computed for it without making any changes to it. It is still recommended, however, that the SET string not be changed unless your application absolutely requires it:

```
program ComputeSum (output);
{Contains procedures to pull a learn string from the HP 8175A and store it in
 an array.  The routine CheckSum then computes the check sum for all the data
 and compares it with the checksum bytes sent in the string.}

  import        iodeclarations,          {General IO functions - see the Pascal}
                general_1,               {3.1 Workstation System Manual for     }
                general_2,               {information on each.                  }
                general_4,
                iocomasm;                {Binary routines}

  const BufSize = 10244;          {Size of SET learn string}
        Arb = 720;                {Address of HP 8175A on HP-IB interface}

  type  Storage = array [1..BufSize] of char;

  var   StoreArray:Storage;       {Array to hold learn string}
```

```
procedure CheckSum (DataArray:Storage);
{This procedure does the actual computation of the checksum for a learn string}

  var   A,B,            {Two bytes to hold developing check sums}
        pos,
        Carry1,Carry2:integer;  {Keep track of "Carry bits"}

begin   {CheckSum}
  pos:=7;       {Start at first byte beyond the header and checksum bytes}
  A:=0; B:=1;   {Initialize the check sum}

  repeat
    Carry1:=A mod 2;    {Shifts bits in A to the right and store carry}
    A:=A div 2;

    Carry2:=B mod 2;    {Rotates bits in B by first shifting right, storing }
    B:=B div 2;         {any carry, and setting top bit if there was a carry}
    if Carry1=1 then B:=B+128;        {from shifting A above              }

    if Carry2=1 then A:=bineor(A,180);    {Adjust A with an exclusive-or }
                                          {if rotating B produced a carry}
    A:=bineor(A,ord(DataArray[pos]));    {Exclusive-or the next two data bytes}
    pos:=pos+1;                          {with A and B respectively          }
    B:=bineor(B,ord(DataArray[pos]));
    pos:=pos+1;
  until pos>BufSize;

  writeln ('From string: ',ord(DataArray[5]):1,'  ',ord(DataArray[6]):1);
          {Just displays the check sum bytes in the string for comparison}
  writeln ('Computed:    ',A:1,'  ',B:1);
end;    {CheckSum}



procedure Get_Learn_String (var StoreArray:Storage);
{Transfers Learn string from HP 8175A and store in an array}

  var   BufName:buf_info_type;
        pos:integer;

begin
  iobuffer (BufName,BufSize);           {Allocate buffer space}
  buffer_reset (BufName);               {Clear buffer}

  writestringln (Arb,'SET?0');          {Query for Learn String}
  transfer_end (Arb,serial_fastest,To_Memory,BufName);
              {Pull in all data sent from HP-8175A until end signal}

  writestringln (Arb,'LO');             {Returns HP 8175A to Local mode}

  for pos:=1 to BufSize do readbuffer (BufName,StoreArray[pos]);
      {Read all characters out of the buffer and store them in an array.}
end;
```

```
{MAIN program}

begin
  ioinitialize;          {Reset all interfaces}

  writeln ('Bringing in a learn string from Arb . . . ');
  Get_Learn_String(StoreArray);
  writeln ('Computing Check Sum . . . ');
  CheckSum(StoreArray);
  writeln ('Finished.');

  iouninitialize;        {Reset all interfaces for program end}
end.
```

CONCLUSION

The programs presented here are meant to give you a starting point for writing your own applications using learn strings. Although at first glance the routines may seem long, they have been heavily commented and many small "extra" routines have been included in them so that they can act as stand alone programs for demonstration purposes. In most cases, the core function performed by each can be compressed into relatively few lines.

Hopefully the routines and descriptions given here are sufficient to allow a thorough understanding of what is actually going on, but for more advanced, detailed coverage of particular techniques, please see the reference list given in the introduction of this document.

APPENDIX: PROGRAMMING INFORMATION

Types of Programming

Besides changing data with learn strings, there are two different methods of remote control of the HP 8175A:

The DEVICE DEPENDENT method means that the cursor must first be positioned in the appropriate field before the value can be changed. The device-dependent commands for keyboard functions are implemented in a mnemonics-per-keystroke format. Since the representation of each and every cursor movement, button push, etc. quickly results in a large number of mnemonics, it is not recommended that you use this method for any large programs!

An example of this programming method would be sending the sequence:

"CD; NX; NX; NX"

This is the same as pressing ↓ and then NEXT three times on the front panel of the HP 8175A. Note that the series "NX; NX; NX" may also be written as "NX3".

The "NORMAL" METHOD requires that the instruction to change any setting is sent in the form of one or more specific HP-IB commands. The majority (but not all) such commands are page specific. An example of this type of command is:

"RST; DM 1; TSA1; CHD0,11001100; LO"

This particular sequence resets the HP 8175A and recalls standard settings; changes to the Data Page Pattern Setup menu; moves to address 1; changes the data in the first Pod there (i.e. POD 2) using binary base to the pattern "11001100"; returns the HP 8175A to local control. As you can see, this method allows much more powerful manipulations with fewer mnemonics than the Device Dependent method.

Please refer to the 8175A Operating and Programming Manual, Section 3G for a complete list of both types of command mnemonics. For programming in the Arbitrary Generator mode, see also the Option 002 Operating Manual, Section 3H.

Sending Command Sequences

The same BASIC and PASCAL instructions can be used to send command sequences as well as learn strings. In BASIC, the normal command is:

```
OUTPUT 7xx;"mnemonics (incomplete)";
OUTPUT 7xx;"mnemonics (completed)"
```

These send the appropriate HP-IB mnemonics to a device that is connected to the interface card 7, and set to the HP-IB address xx (0 to 30). The PASCAL equivalents to these BASIC statements are:

```
WRITESTRING (7xx, 'mnemonics (incomplete)');
WRITESTRINGLN (7xx, 'mnemonics (completed)');
```

Note that PASCAL provides various other procedures such as WRITECHAR and WRITENUMBERLN as well (see Recommended Literature in the Introduction of this document).

Note the only difference in each output pair is whether or not the mnemonics are followed by an end-of-line indicator (e.g. CR/LF). A trailing semicolon after an OUTPUT statement in BASIC suppresses this. In PASCAL, all statements are followed by a semicolon, so there are two separate functions: WRITESTRING does not send the end-of-line, while WRITESTRINGLN does. Since an end-of-line always indicates the end of a complete command sequence, it is important to suppress this when sending a long command string over a series of separate output statements.

For example, suppose you wanted to change a series of sequential memory addresses. You could send the following:

```
OUTPUT 720;"CHD0,";
OUTPUT 720;"10101010,";
OUTPUT 720;"11111111,11110000"
OUTPUT 720;"LO"
```

The first output starts the command to change data using binary base. The next two commands contain data patterns to be sent. Note the trailing semicolon after each statement to suppress the end-of-line; the HP 8175A will accept all the data as if it were sent in one complete string. The third output sends the end-of-line to terminate the change data command and the final output returns the HP 8175A to local control (also terminated with an end-of-line).

For all commands, note the following points: Mnemonics can be sent using either upper case or lower case letters. To increase efficiency and speed, multiple menomonic commands can be transmitted by one OUTPUT or WRITESTRINGLN statement, as demonstrated in the first two command strings. Note that in this case, the separate commands must be delimited by semicolons; these act as end-of-line characters within the string.

Be careful not to confuse the various uses of semicolons: In both PASCAL and BASIC, when sent within a command sequence (i.e. inside quotation marks), a semicolon is the same as an end-of-line. When placed outside the quotation marks following an output statement in BASIC, a semicolon suppresses the end-of-line. In PASCAL, a trailing semicolon (found after all commands) has no effect.

If you are not familiar with the HP-IB mnemonics, it is probably best to use BASIC since there is a SINGLE STEP key available to allow you to execute commands one at a time.

If an error does occur, the HP 8175A will display the wrong syntax in inverse video on the second line of the CRT. Since this can be deleted by a successive HP-IB command, you should not use multiple mnemonic commands until the sequence of commands has been tested.

HEWLETT PACKARD

MANUAL CHANGES

Manual for Model Number	8175A
Manual printed on	July 1985
Manual Part Number	08175-90001

12/93

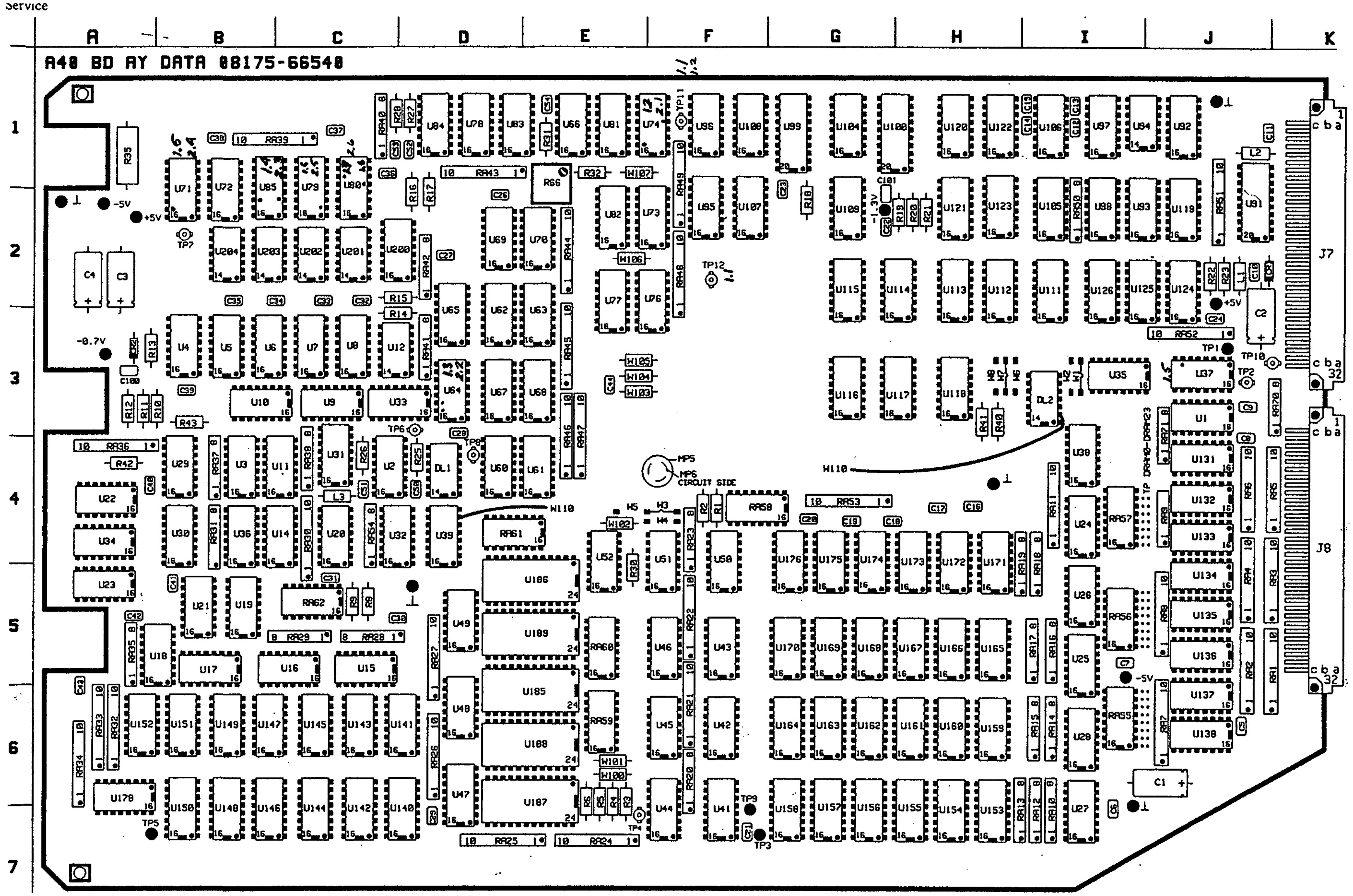
Make all ERRATA corrections.

Check the following table for your instrument serial prefix/serial number /EDC and make the listed changes to your manual.

▶ New Item

Serial Prefix or Serial Number		Manual Changes
ERRATA		
2520G00231	#001	
2520G00251	and above	1
2520G00271	and above	2
2612G00326	and above	3
2612G00356	and above	4
2612G00396	and above	5
2612G00415	and above	6
2612G00435	and above	7
2612G00456	and above	8
2642G00576	and above	9
2642G00616	and above	10
2642G00956	and above	11
2642G00996	and above	12
2642G01036	and above	13
2642G01116	and above	14
2642G01326	and above	15
2903G01446	and above	16
2903G01506	and above	17
2932G01606	and above	18
2948G01646	and above	19
2948G01706	and above	20
2948G01726	and above	21
2948G01766	and above	22
2948G01946	and above	23
CHANGE TO EDC LABELS ON BOARDS (X-3116)		
2948G01966	and above	24
2948G02146	and above	25
2948G02176	and above	26
2948G02236	and above	27

Serial Prefix or Serial Number		Manual Changes
ERRATA		
2948G02256	and above	28
2948G02276	and above	29
2948G02326	and above	30



REF DES	GRID LOC	REF DES	GRID LOC	REF DES	GRID LOC	REF DES	GRID LOC	REF DES	GRID LOC	REF DES	GRID LOC	REF DES	GRID LOC
C1	I/J6	DL1	D4	RA6	J4	RA59	E6	U37	J3	U107	F2	U165	H5
C2	J2/3	DL2	I3	RA7	J6	RA60	E5	U38	I4	U108	F1	U166	H5
C3	A2	J7	K1/2/3	RA8	J5	RA61	D/E4	U39	D4	U109	G2	U167	H5
C4	A2	J8	K3/4/5	RA9	J4	RA62	C5	U41	F6/7	U111	I2/3	U168	G5
C5	J6	L1	J2	RA10	I6/7	RA70	K3	U42	F6	U112H2/3		U169	G5
C6	I7	L2	J1	RA11	I4	RA71	J3/4	U43	F5	U113	H2/3	U170	G5
C7	I5	L3	C4	RA12	I6/7	TP1	J3	U44	F6/7	U114	G2/3	U171	H4/5
C8	J3	MP5	F4	RA13	H6/7	TP2	J3	U45	F6	U115	G2/3	U172	H4/5
C9	J3	MP6	F4	RA14	I6	TP3	F7	U46	F5	U116	G3	U173	H4/5
C10	J2	R1	F4	RA15	I6	TP4	E7	U47	D6/7	U117	G3	U174	G4/5
C11	J1	R2	F4	RA16	I5	TP5	B7	U48	D5/6	U118	H3	U175	G4/5
C12	I1	R3	E6/7	RA17	I5	TP6	D3	U49	D5	U119	J2	U176	G4/5
C13	I1	R4	E6/7	RA18	I4/5	TP7	B2	U50	F4/5	U120	H1	U178	A6/7
C14	I1	R5	E6/7	RA19	H4/5	TP8	D4	U51	F4/5	U121	H2	U185	D/E5/6
C15	I1	R6	E6/7	RA20	F6	TP9	F6	U52	E4/5	U122	H1	U186	D/E5
C16	H4	R8	C5	RA21	F5/6	TP10	K3	U60	D4	U123	H2	U187	D/E6/7
C17	H4	R9	C5	RA22	F5	TP11	F1	U61	E4	U124	J2/3	U188	D/E6
C18	G/H4	R10	A3	RA23	F4	TP12	F2	U62	D2/3	U125	I/J2/3	U189	D/E5
C19	G4	R11	A3	RA24	E/F7	U1	J3	U63	E2/3	U126	I2/3	U200	C2
C20	G4	R12	A3	RA25	D/E7	U2	C4	U64	D3	U131	J4	U201	C2
C21	F7	R13	A3	RA26	D6/7	U3	B4	U65	D2/3	U132	J4	U202	C2
C22	G2	R14	C/D3	RA27	D5/6	U4	B3	U66	E1	U133	J4	U203	B2
C23	G2	R15	C/D2	RA28	C/D5	U5	B3	U67	D3	U134	J5	U204	B2
C24	J3	R16	D1/2	RA29	B/C5	U6	B3	U68	E2	U135	J5	W1	I3
C26	D2	R17	D1/2	RA30	C4/5	U7	C3	U69	D2	U136	J5	W2	I3
C27	D2	R18	G2	RA31	B4	U8	C3	U70	E2	U137	J6	W3	F4
C28	D3	R19	G/H2	RA32	A6	U9	C3	U71	B1/2	U138	J6	W4	F4
C29	D7	R20	H2	RA33	A6	U10	B3	U72	B1/2	U140	C6/7	W5	E4
C30	D5	R21	H2	RA34	A6	U11	B4	U73	F2	U141	C6	*W6	H3
C31	C5	R22	J2	RA35	A5	U12	C3	U74	F1	U142	C6/7	*W7	H3
C32	C2	R23	J2	RA36	A/B4	U14	B4	U76	F2/3	U143	C6	*W8	H3
C33	C2	R25	D4	RA37	B4	U15	C5	U77	E2/3	U144	C6/7	W100	E6
C34	B/C2	R26	C4	RA38	C3/4	U16	B/C5	U78	D1	U145	C6	W101	E6
C35	B2	R27	D1	RA39	B/C1	U17	B5	U79	C1/2	U146	B6/7	W102	E4
C36	C1	R28	C1	RA40	C1	U18	A5	U80	C1/2	U147	B6	W103	E/F3
C37	C1	R30	E4/5	RA41	D3	U19	B5	U81	E1	U148	B6/7	W104	E/F3
C38	B1	R31	E1	RA42	D2	U20	C4	U82	E2	U149	B6	W105	E/F3
C39	B3	R32	E1	RA43	D1	U21	B5	U83	D1	U150	B6/7	W106	E/F2
C40	A4	R35	A1	RA44	E2	U22	A4	U84	D1	U151	B6	W107	E/F1
C41	B5	R40	H3	RA45	E3	U23	A5	U85	B1/2	U152	A6	W110	E4-I4
C42	A5	R41	H3	RA46	E3/4	U24	I4	U91	J1/2	U153	H6/7		
C43	A5/6	R42	A3	RA47	E3/4	U25	I5/6	U92	J1	U154	H6/7		
C44	E3	R43	B3	RA48	F2/3	U26	I5	U93	I/J2	U155	H6/7		
C50	D4	R66	E1/2	RA49	F1/2	U27	I6/7	U94	I/J1	U156	G6/7		
C51	C4	RA1	K5/6	RA50	I2	U28	I6	U95	F2	U157	G6/7		
C52	D1	RA2	J5/6	RA51	J2	U29	B4	U96	F1	U158	G6/7		
C53	C1	RA3	K5	RA52	J3	U30	B4	U97	I1	U159	H6		
C54	E1	RA4	J5	RA53	G4	U31	C3/4	U98	I2	U160	H6		
C100	A3	RA5	K4	RA54	C4	U32	C4	U99	G1	U161	H6		
C101	G2			RA55	I6	U33	C/D3	U100	G1	U162	G6		
CR1	J/K2			RA56	I5	U34	A4	U104	G1	U163	G6		
CR2	A3			RA57	I4	U35	I3	U105	I2	U164	G6		
				RA58	F/G4	U36	B4	U106	I1				

MODEL 8175A

INDEX OF MANUAL CHANGES

MANUAL CHANGE	MISCELLANEOUS	FRAME	A1	A2	A10	A20	A30	A31	A40
ERRATA	Page 6-8,6-9, 6-10,6-12 6-18,6-19 6-21,7-8, 8-25,8-29, 8-55, 8-128/129 8-142, 8-148, 8-159, 8-162								
1	Page 6-11					U701			
2	Page 6-10/11					R206,207 W1 U312,313	C99		
3	page 6-10					U210,211, U106,107, U109,111 W1 U108,110 W2			
4		MP11							
6					R29	R700			
7				A2 W1					

MODEL 8175A

INDEX OF MANUAL CHANGES

MANUAL CHANGE	MISCELLANEOUS	FRAME	A1	A2	A10	A20	A30	A31	A40
8	Page 6-13						R120,121, DL2		
9	Page 6-8 Page 6-5	A5, A6 MP2,12 B1,2			J4				
10	Page 6-16/17								U105,RA24, R124
11				S1-39	C55				
12		MP47							
13	Page 6-16								R124
14									R25
15						U406-413			
16		MP4 - 7, MP60,41, MP48,59, MP49,51, MP50,52							
17	B1,2,W1,2,3,5				CR18,19				R50,51,RA34 U140-141 U153-158, R124,RA12,13 RA16,17, U159-176 U144-152 U142,143
19		A20				U508			

MODEL 8175A
INDEX OF MANUAL CHANGES

MANUAL CHANGE	MISCELLANEOUS	FRAME	A1	A2	A10	A20	A30	A31	A40
20							U9,10,30,31		U185,186 U187,188, U189
22					CR5				
23					R29, U8				
CHANGE TO EDC LABEL (X-3116) ON BOARDS ! ! !									
24									U140,141 U153,154, U155,156, U157,158, U142,143
25					C55				
26		A10			CR1, S1				
27		MP71							
28							R15,16,17, R23,25,50, CR68		
29				J26,27					

INDEX OF MANUAL CHANGES

MANUAL CHANGE	MISCELLANEOUS	FRAME	A1	A2	A10	A20	A30	A31	A40
30									C51

MODEL 8175A

INDEX OF MANUAL CHANGES

MANUAL CHANGE	MISCELLANEOUS	FRAME	A50
2	Page 6-18		C7,8,12,16,17,21,24 C26 thru 32 C34 thru 37 C40,41,42 C44
3			R800
5	Page 6-19		C207,217,227,237
17			C7,8,12,16,17,21,22 C24,26,27,28,29-32, C34-37,41,42

CHANGE TO EDC LABELS (X-3116) ON BOARDS ! ! !

MODEL 81[redacted]

INDEX OF MANUAL CHANGES (OPTION 001)

MANUAL CHANGE	MISCELLANEOUS	FRAME	A50 Option 001	
1	Page 6-19/6-20		C7thru12 C16thru32 C34,35,36, C37,40,41,42 C46thru60 C44	
17			C7-12,16-32, C34-37,40-42, C46-60	

CHANGE TO EDC LABELS (X-3116) ON BOARDS ! ! !

ERRATA

Make all ERRATA corrections

*Note: Since the Operating and Programming manual (08175-90006) can be separately ordered, it has its own Errata sheet (covering sections 1 to 4). This suplement covers errata and/or manual changes for sections 5 to 8 (service sections) only.

General point: Referring to Section 8 of the 90001 manual, some copies have the layout diagrams inserted (incorrectly) behind the corresponding registers instead of after. This can be easily checked and rectified.

Page 6-8: Change the Part Numbers/Descriptions etc. of the following components:

A10 C55	0160-3097	
A10 CR18	08175-88701	DIODE KIT
A10 CR19	08175-88701	DIODE KIT

Page 6-9:

Add: A10 TP1 (CD=2) 1251-0628 CONN POST TP SKT

Change A10 TP2-12 to: 0360-0535 TEST POINT

Page 6-10:

Add: A20 MP1 (CD=3) 0380-0643 MOUNTING STUD

Change M 246 to read: MP2

Change following details of A20 U406 - 413 to read as shown:

1818-3483 IC TMS 4164-15NL

Page 6-12:

Add: A30 MP14 1252-0220 DUST COVER

Page 6-18: Change following details of A40 W1 - W5 to read as shown:

1258-0124 JUMPER

Add: W6,W7,W8 1258-0124 JUMPER

Add a * in front of W1,4,5,6 and 8 and a corresponding note to indicate that these jumpers are not necessarily installed on all A40 boards.

Page 6-19: Change following details of A50 R103 to read as shown:

0698-3444 R-F 316 1% .125W

Page 6-21: Change following details of A50 W1 to W3 to read as shown:

1258-0124 JUMPER

Add a * in front of W1 and W3 (indicates installed as required).

Page 7-8: At end of second to last paragraph, change last line details to read: "..delay circuit (schematic 51D)."

ERRATA (Cont.)

Page 8-25: Waveform photos for TP 10 and 9, change "1V/DIV" to read: "0.5V/DIV".

Page 8-29: Add the title: "Table 8-1-2" below left hand table.

Page 8-55: Towards end of the first paragraph, details should read:
"...of U210 (HF0-HF5)".

Pages 8-128/129:
For both cases where signals are to be compared with TP16 signal, the menu required should read:
"Control Page (PAR) [Clock]".

Page 8-142: In the Grid Locator list add a * (indicates installed as required) in front of W1, W4, and W5. Delete the * in front of W7.

Page 8-148: In the middle paragraph which starts "The shift registers U25/U26...", change text in the appropriate sentence so that it reads as follows:
"The control circuit is initialized with signal HADDS, signal LTIMELOAD1 stops the control circuit and shift register for the timing duration."

Page 8-159: Referring to the lower photo and corresponding test settings,
change "Delayed" to "Mixed" and change photo reference from "U11/12" to U14/2".

Page 8-162: Referring to the lower photo and corresponding test settings, the settings should read as follows:
"...Width 500ns, Ampl. +2V, Delay min, TT min, Offset OFF, Norm+)
Scope settings: 2us/Div, 0.05V/Div"

Page 6-4: Figure 6-1, 8175A Mainfraim Parts change in the picture where the frame Parts are shown W9 Yell To W14 Yell.

Page 6-5: ADD: W14 08175-61611 CBL SMB/BNC

Page 6-5: Change to read: MP2 08175-00138 BRACKET MID

ERRATA (Cont.)

ADD to SECTION 8 SERVICE:

8-20 POD INFORMATION

8-21 In the case of isolating a foult down to a POD, Input or Output POD, take the info given in Table 8-3 to order the correct POD replacement.

Table 8-3. Index of POD's

MODEL NO	Replaceable P/N
HP 15461A ECL POD	15461-69601
HP 15462A TTL/CMOS POD	15462-69601
HP 15463A TRIGGER POD	15463-68701
HP 15464A TTL POD	15464-69601

8-22 ACCESSORIE INFORMATION

8-23 Table 8-4 shows the replaceable part numbers of the available Accessories.

Table 8-4. Index of Accessories

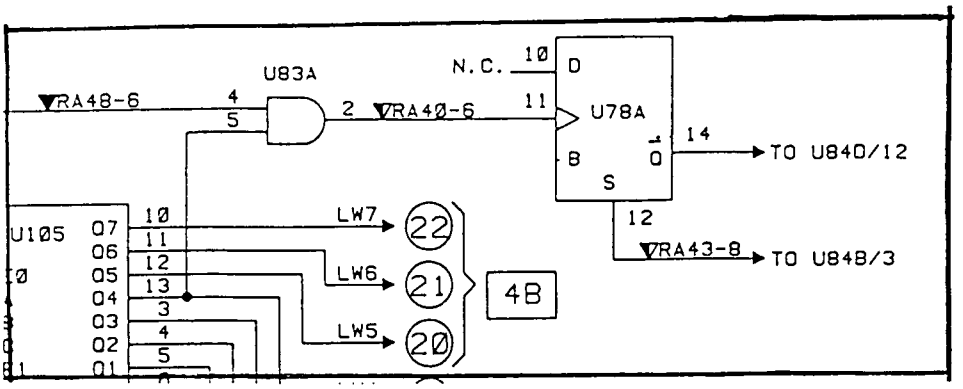
MODEL NO	Replaceable P/N
HP 15408A	15408-68701
HP 15409A	15409-68701
HP 15410A	15410-68701
HP 15411A	15411-68701
HP 15415A	15415-68701
HP 15429A	15429-68701

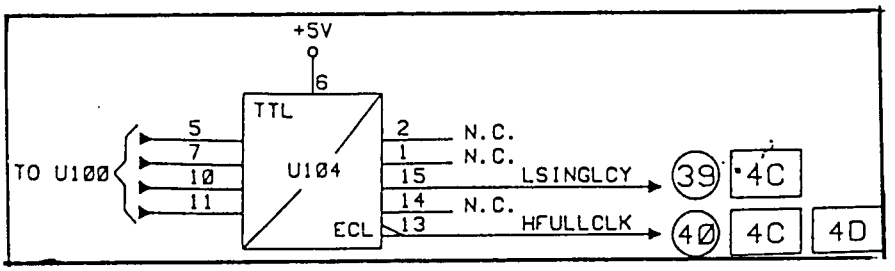
On Page 6-19, change the Table of Replaceable Parts to read:

A50	J9,10	1251-7799	Conn-Post-TP-HDR

ERRATA (Cont.)

On Page 8-167, change Schematic and Grid Locator to read:





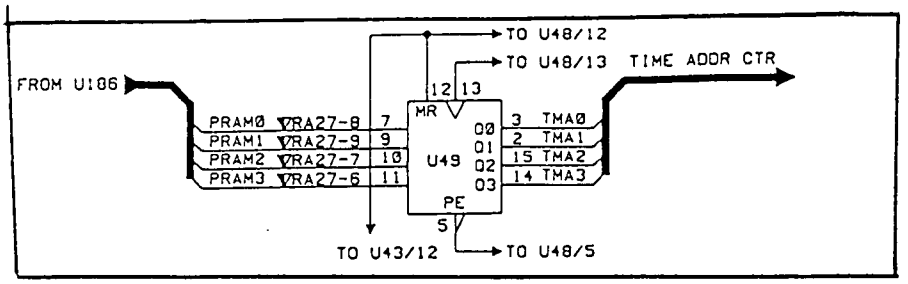
RA	GND PIN	POWER PIN	VOLTAGE LEVEL	RESISTOR VALUE
43	10	1	-5.2V	10 PIN 160/240
51		1	+5V	9X10K

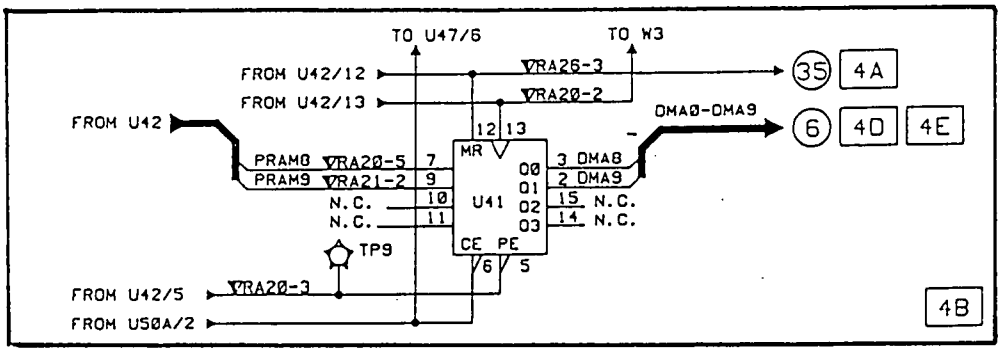
REF.DES.	-5.2V	+5V	-15V	+15V	GND
U84	8				1,16
U92		16			8

DELETE U91

ERRATA (Cont.)

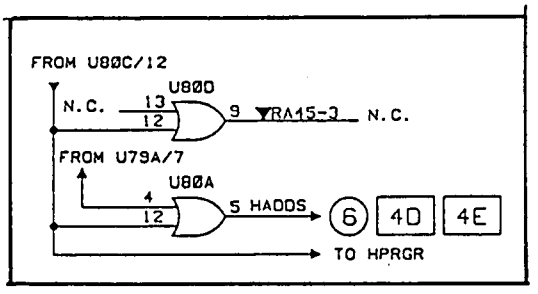
On Page 8-169, change to read:

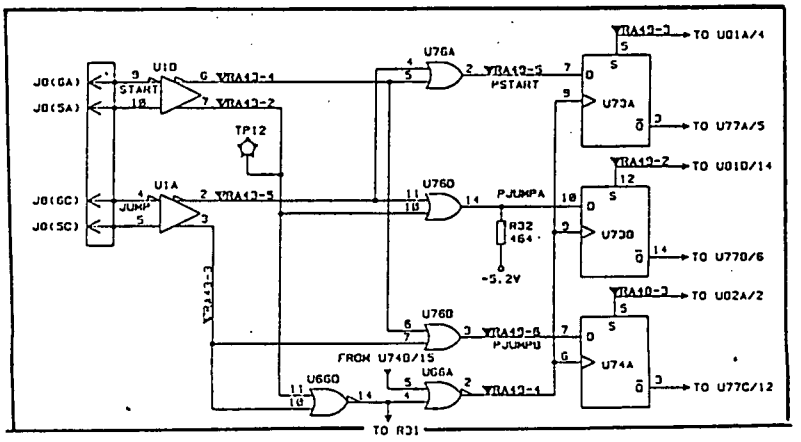




RA	GND PIN	POWER PIN	VOLTAGE LEVEL	RESISTOR VALUE
20	8	1	-5.2V	8PIN160/240
21	10	1	-5.2V	10PIN160/240
22	10	1	-5.2V	10PIN160/240
23	8	1	-5.2V	8PIN160/240
24	10	1	-5.2V	10PIN160/240
25	10	1	-5.2V	10PIN160/240
26	10	1	-5.2V	10PIN160/240
27	10	1	-5.2V	10PIN160/240
39	10	1	-5.2V	10PIN160/240
41	8	1	-5.2V	8PIN160/240
42	8	1	-5.2V	8PIN160/240
52	10	1	-5.2V	10PIN160/240

REF.DES.	-5.2V	+5V	-15V	+15V	GND
U79	8				1,15,16
U80	8				1,16
U81	8				1,15,16





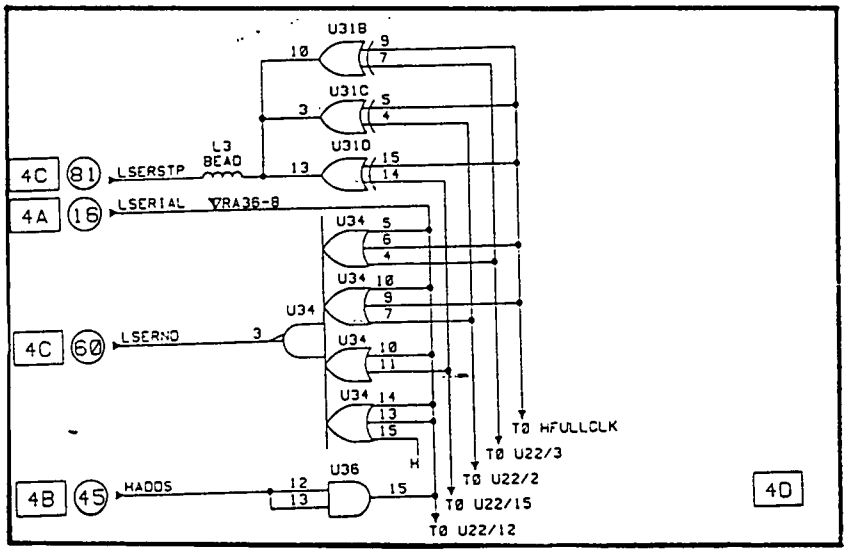
ERRATA (Cont.)

On Page 8-171 change to read:

RA	GND PIN	POWER PIN	VOLTAGE LEVEL	RESISTOR VALUE
11	10	1	-5.2V	10PIN160/240
28	8	1	-5.2V	8PIN160/240
29	8	1	-5.2V	8PIN160/240
30	10	1	-5.2V	10PIN160/240
31	8	1	-5.2V	8PIN160/240
32	10	1	-5.2V	10PIN160/240
33	10	1	-5.2V	10PIN160/240
35	8	1	-5.2V	8PIN160/240
36	10	1	-5.2V	10PIN160/240
37	8	1	-5.2V	8PIN160/240
38	8	1	-5.2V	8PIN160/240
54	10	1	-5.2V	10PIN160/240

DELETE RA34

On Page 8-173, change to read:



On Page 8-175, change to read:

RA	GND PIN	POWER PIN	VOLTAGE LEVEL	RESISTOR VALUE
42	8	1	-5.2V	8PIN160/240
51		1	+5V	9X10K

4E

On Page 8-108, : change C95 to read C99
change C99 to read C95

MANUAL CHANGE 1

On Page 6-11, change the Table of Replaceable Parts to read:

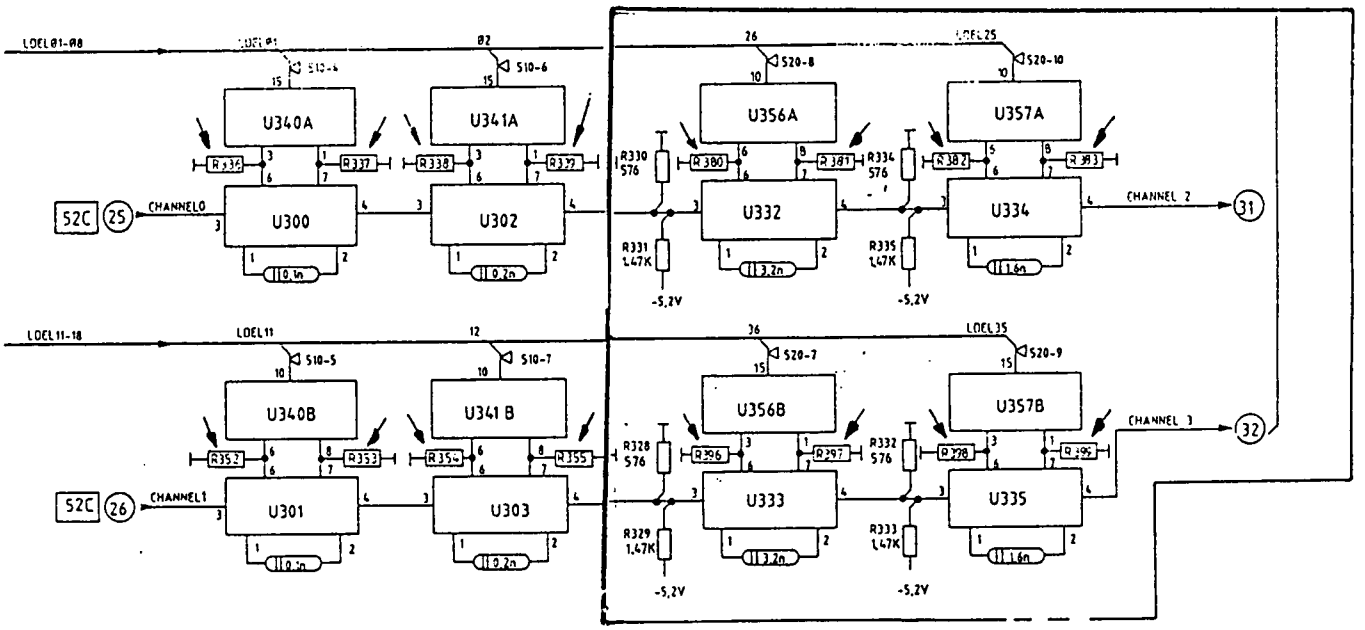
	A20 U701	1820-3911	IC 9513A

OPTION 001

On Page 6-19, 6-20, change the Table of Replaceable Parts to read:

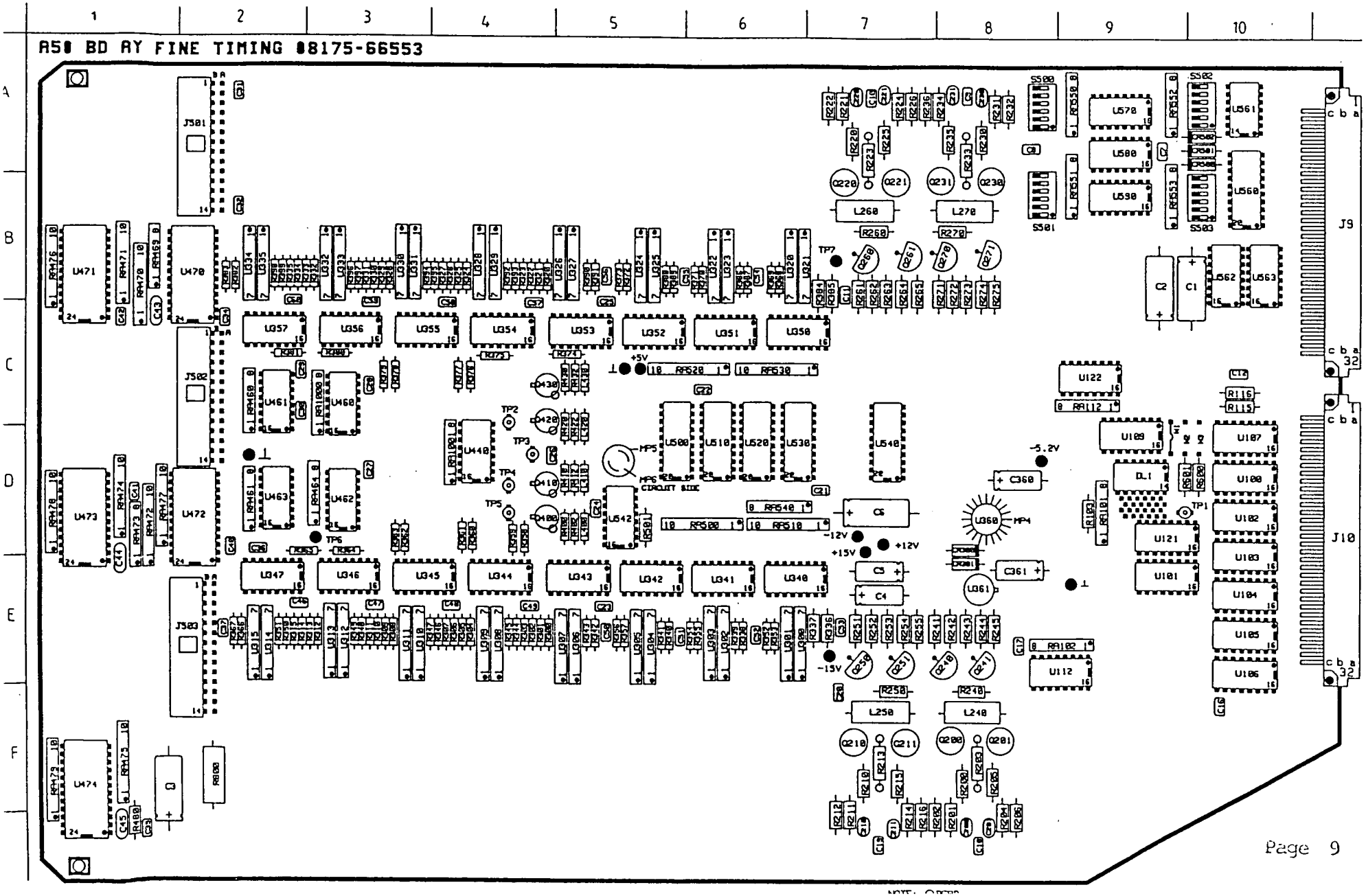
	A50	08175-66553	BD AY TIMING
	A50 C7thru12 C16thru32 C34,35,36 C37,40,41, C42 C46thru60	0160-4835	C-FXD .1Uf 50V
	A50 C44	0160-3456	C-FXD 1000Pf 1000 V
DELETE:	A50 R801		
ADD:	A50 R336 thru R399	0757-0447	R-FXD 12.1K 1%

On Page 8-209, change Schematic 52D as shown:



Change all 32 circuits als shown.

On Page 8-190, change Layout as shown:



MANUAL CHANGE 2

On Page 6-10/11, Replaceable Parts List:

ADD:	A20	R206	0757-0416	R-FXD .511
		R207		
		W1	8159-0005	JUMPERWIRE
DEL:	A20	U312		
	A20	U313		

On A20 Schematic, Page 8-95 :

ADD: R206 is connected from U209 Pin 16 to +5V

R207 is connected from U209 Pin 7 to +5V

W1 is connected between +5V to Pin 27 of U 106,107,108,109,110,111, 210,211

On Page 6-18, change the Table of Replaceable Parts to read:

A50 C 7,8,12,16,17, C 21,22,24,26, C 27,28,29,30, C 31,32,34,35, C 36,37,40,41,42	0160-4835	C-FXD .1UF 10% 50V
A50 C44	0160-3456	1000 PF 1000 V

DEL: A50 C 9,10,11,18,19, C20,23,25

A50 R 801

A50 C4,5

Delete the same parts on Page 8-178 A50 BD LAYOUT.

On Page 6-11, change the Table of Replaceable Parts to read:

A30 C99	0160-4493	C-FXD 27PF 5% 200V

MANUAL CHANGE 3 ↑326

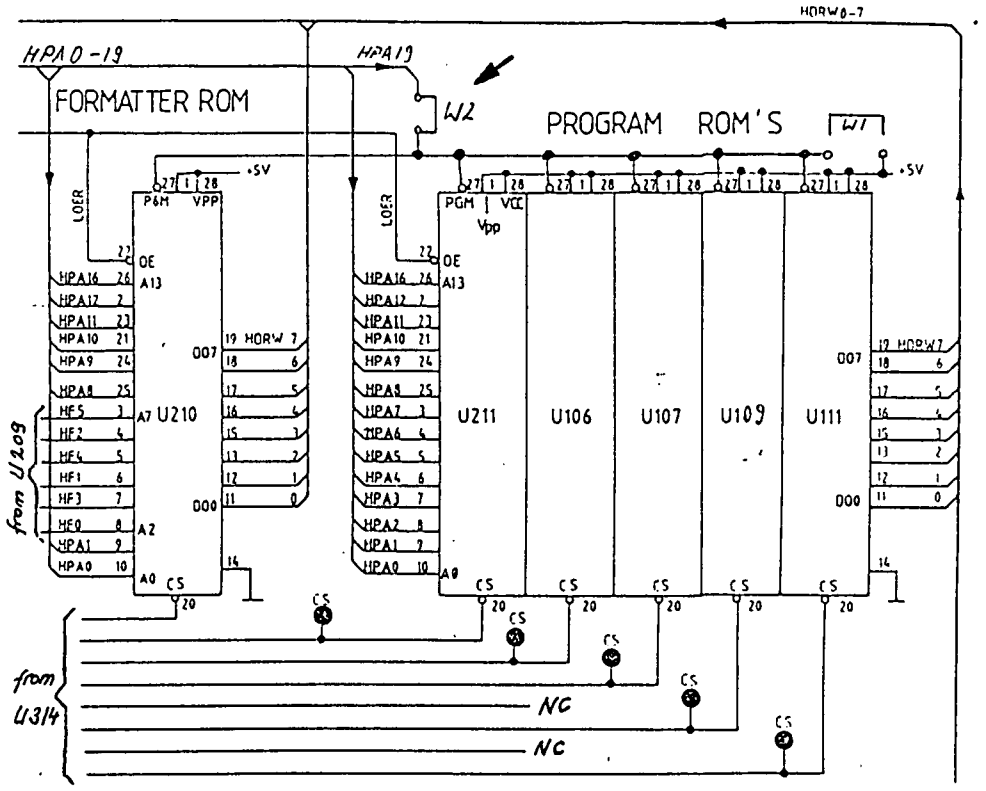
On Page 6-5, change the Table of Replaceable Parts to read:

	A20	08175-66524	BD AY CPU BD

On Page 6-10, change the Table of Replaceable Parts to read:

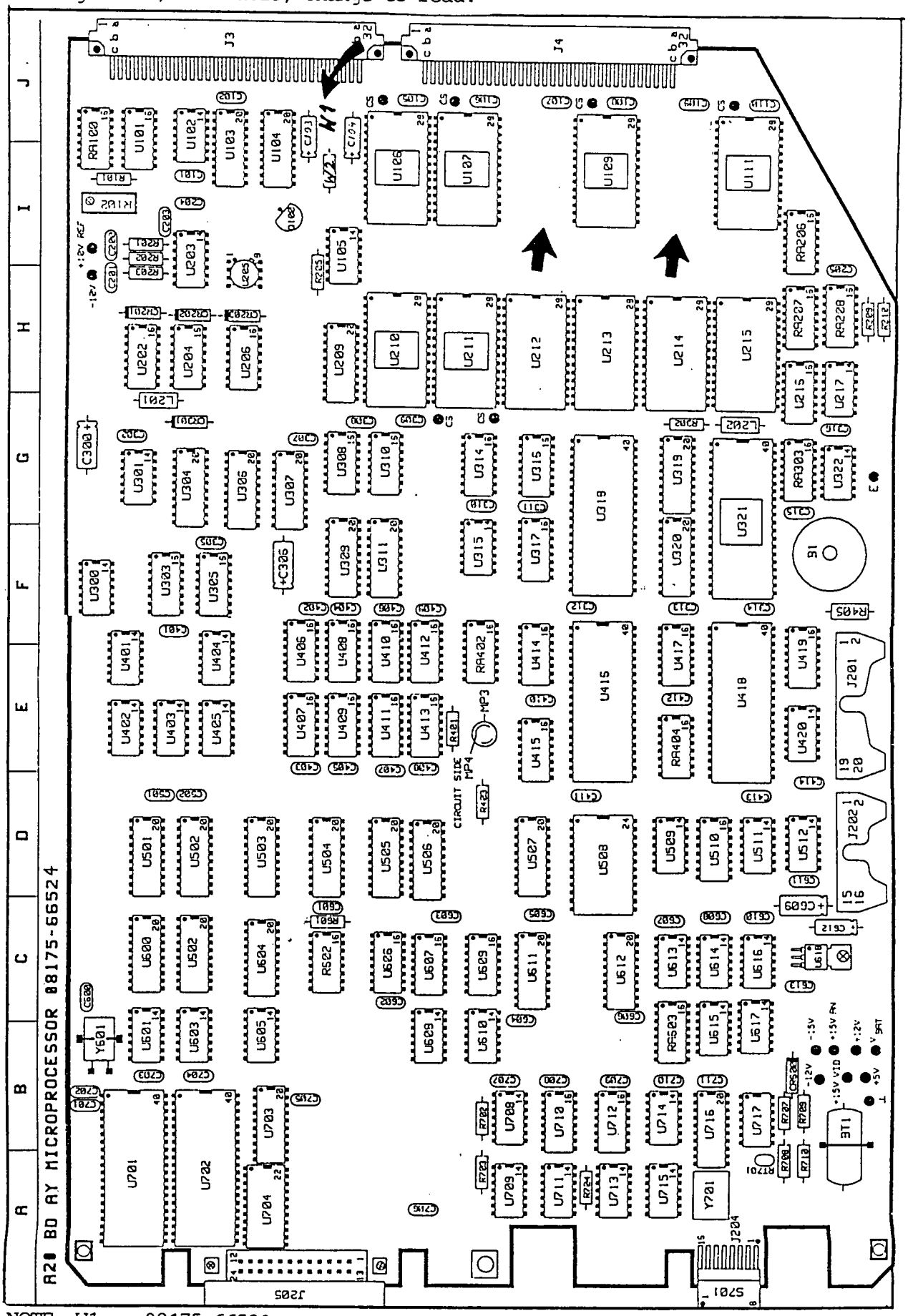
	A20 U210	08175-13710	E-PROM 1
	A20 U211	08175-13711	E-PROM 2
	A20 U106	08175-13712	E-PROM 3
	A20 U107	08175-13713	E-PROM 4
	A20 U109	08175-13715	E-PROM 6
	A20 U111	08175-13717	E-PROM 8
ADD:	A20 W2	8159-0005	JUMPERWIRE
DEL:	A20 W1		
	A20 U108,110		

Change Schematic "B to read (Page 8-95):



MANUAL CHANGE 3 (Cont.)

On Page 8-42, Schematic, change to read:



NOTE: W1 on 08175-66520 BOARD FOR 128K E-PROMS (8times)
W2 on 08175-66524 BOARD FOR 256K E-PROMS (6times)

MANUAL CHANGE 3 (Cont.)

On Page 8-83 step d) ROM S.A. Test change to read:

Set the switch on the "MMU-ET" 08175-66523 as shown Signature Analyzer settings/Connection points on A20 CPU BD:

START ⌐└ to TP "CS" (ROM pin 20) of the ROM which will be measured

STOP ┘┌ or ┌└ U211 pin 27 (HPA19)

CLOCK ┘┌ U211 pin 22 (LOER)

⊥ ⊥

NOTE: Verify that reading at +5V is 3U9F whith START on "CS" of U210.

Check signatures of ROM's against the following table:

ROM S.A.

IC on Schematic 2B

pin	U210		U211		U106		U107		U109		U111	
	┘STOP└		┘STOP└		┘STOP└		┘STOP└		┘STOP└		┘STOP└	
11	PP3H	4HH6	2P99	C95C	43AU	3H4F	2709	35C5	P427	2U4U	H9H5	A10C
12	26U8	2782	3198	CFH2	7PC9	5P57	5684	7HC9	37UU	6U7H	13UH	18A5
13	2F9P	8413	4UP6	CF19	U82A	AF4P	34C0	67C4	7U9C	4208	8CF5	457P
15	HFFU	F27P	2FH9	FA0U	C282	79AU	45H8	C7HH	20U3	C327	F861	54P6
16	F65C	9HU5	F857	C987	ACA2	1A2A	PAHU	3P1F	6074	70C2	C624	269F
17	0631	FC93	A304	A95A	0F38	3FP0	3PH6	2PF2	5FC0	7CP6	1F67	AC9A
18	P379	052P	AU1H	7H42	3147	F234	1CH4	H229	CH2P	H20H	6298	9291
19	133H	F3C7	3045	C8CU	P30A	367A	9FFC	H46A	A55P	3A90	36UU	405P

MANUAL CHANGE 3 (Cont.)

On Page 6-11, change hte Table of Replaceable Parts to read

A20	U701	1820-2604	IC 9513

On Page 6-5, change the Table of Replaceable Parts to read:

W10	08175-61620	CABLE AY
W11	08175-61621	CABLE AY

8175A On Page 6-18, change the Table of Replaceable Parts to read:

8175A#001 On Page 6-19, change the Table of Replaceable Parts to read:

A50	R800	0698-3605	R-FXD 120 OHM 5%

MANUAL CHANGE 4

On Page 6-5, change the Table of Replaceable Parts to read:

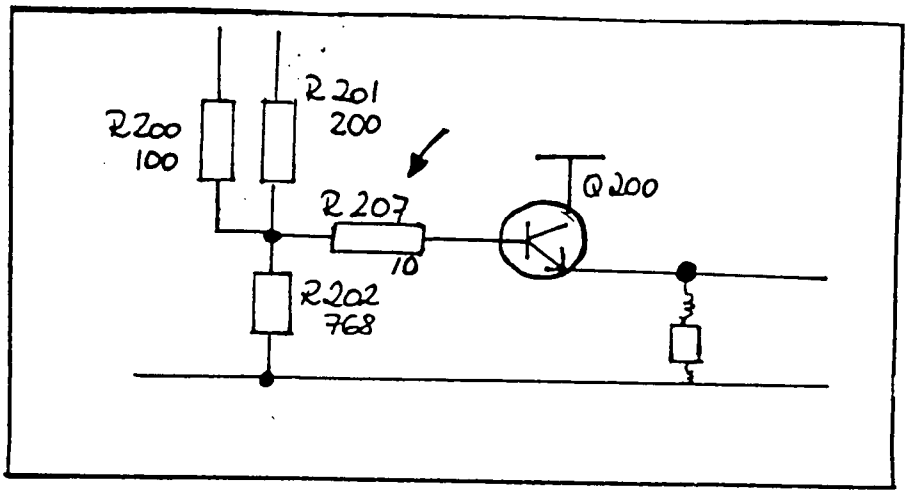
MP11	08175-40203	FRONT PANEL

MANUAL CHANGE 5

On Page 6-19, Replaceable Parts List, add:

A50	R207, R217, R227, R237	0757-0346	R-FXD 10 1% .125W

On Schematic, Page 8-207, add:



MANUAL CHANGE 6

On Page 6-8, change the Table of Replaceable Parts to read:

A10	R29	0698-3518	R-FXD 7.32 KOHM 1%

On Page 6-10, Replaceable Parts List:

Del: A20 R700

MANUAL CHANGE 7

On Page 6-5, change the Table of Replaceable Parts to read:

A2		08175-66504	BD-AY KEY

On Page 6-7, change the Table of Replaceable Parts to read:

A2	W1	08175-61622	CBL AY

MANUAL CHANGE 8

On Page 6-13, change the Table of Replaceable Parts to read:

A30	R120	0698-4409	R-FXD 127 1%
A30	R121	0757-0399	R-FXD 82,5 1%
A30	DL2	1810-0919	Delayline 13ns

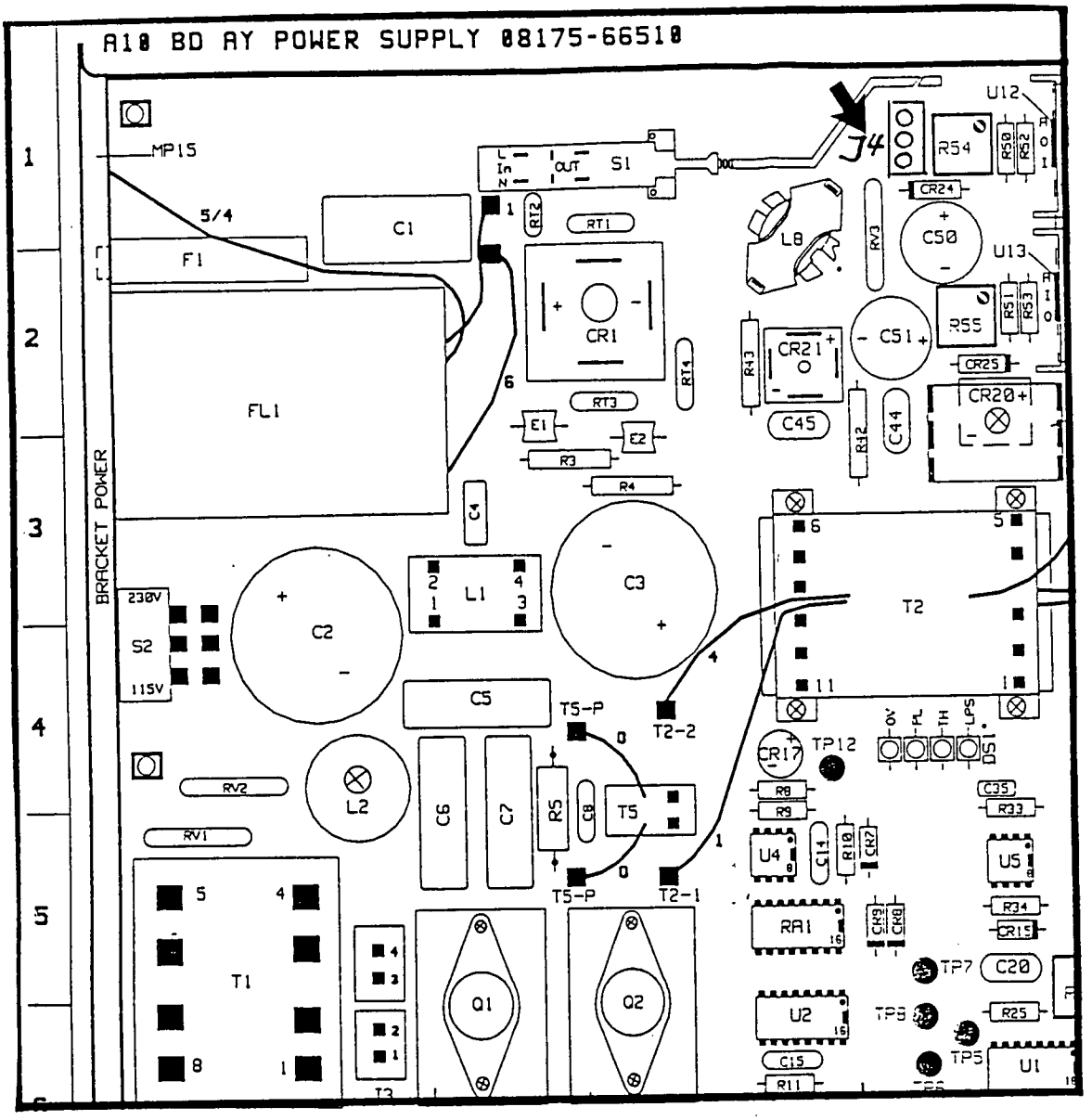
MANUAL CHANGE 9

On Page 6-5, Replaceable Parts List, change to read:

	MP2		08175-00138	BRACKET MIDDLE
	MP12		08175-00638	SHIELD FAN
	B1,2		3160-0510	FAN
ADD:	A10	J4	1251-4246	CONN. 3-PIN (Page 6-8)
	A5		08175-66505	BD AY CONTROL
	A6		08175-66506	BD AY SENSOR

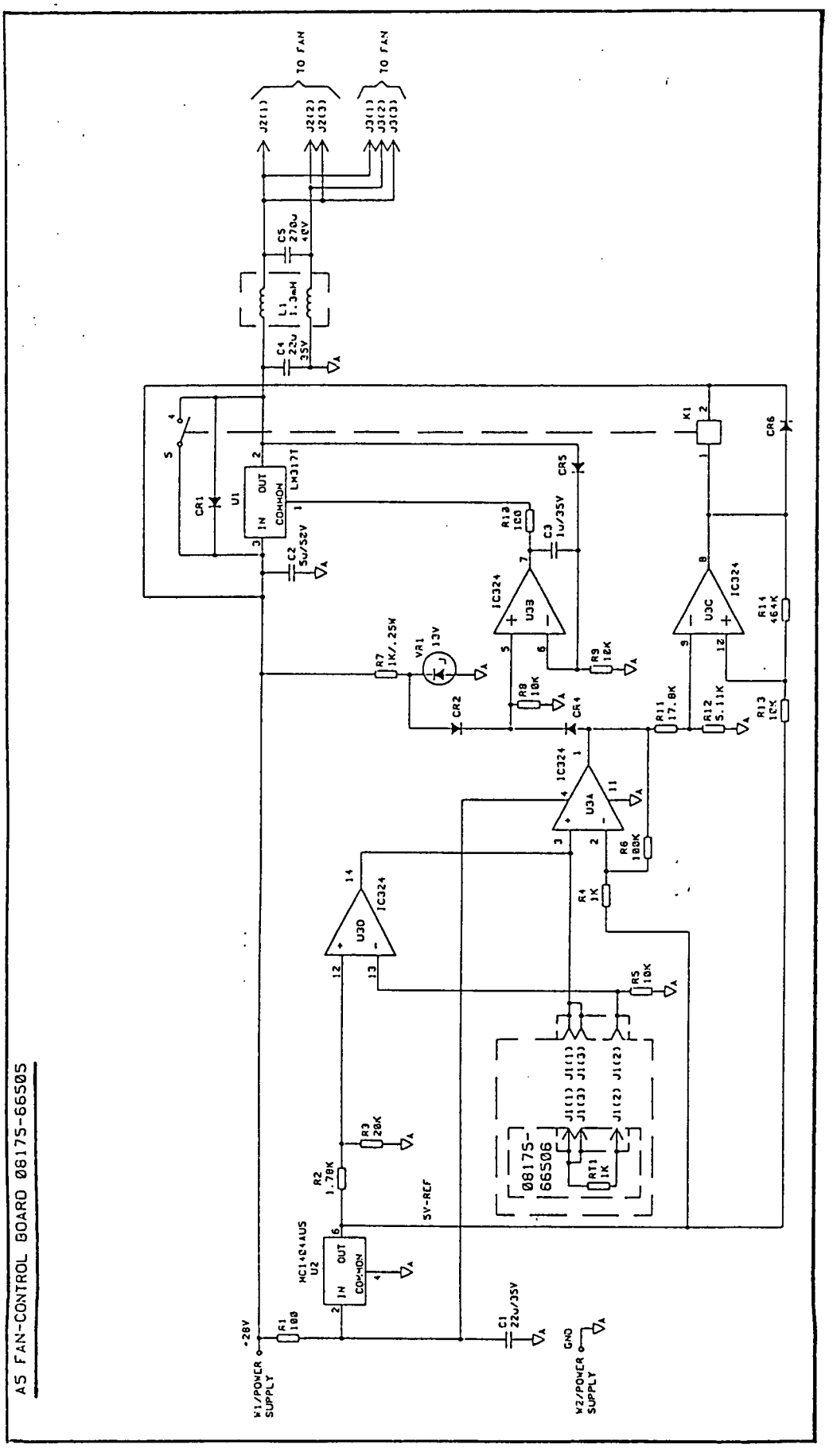
MANUAL CHANGE 9 (Cont.)

On Page 8-12, Component Layout, add:

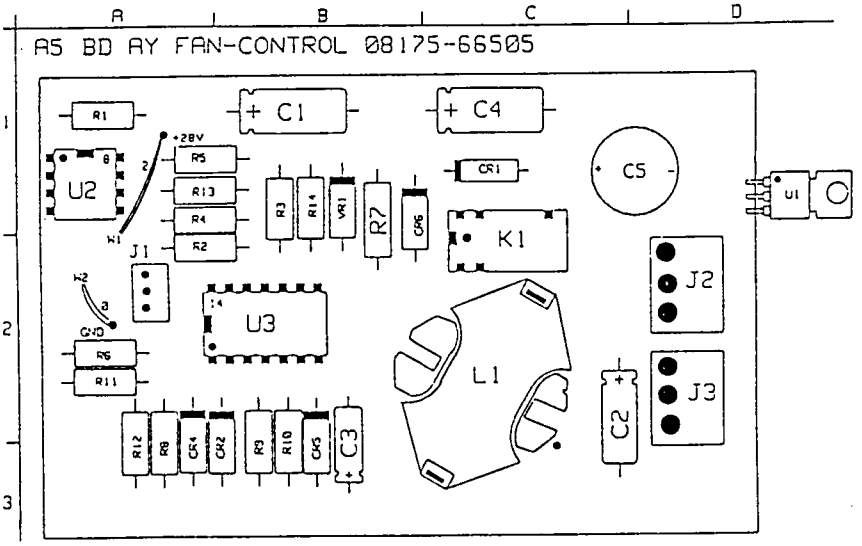


MANUAL CHANGE 9 (Cont.)

ADD: Component Layout & Schematic 08175-66505 & 08175-66506:



MANUAL CHANGE 9 (Cont.)



REF DES	GRID LOC	REF DES	GRID LOC	REF DES	GRID LOC
C1	B1	R1	A1	VR1	B1
C2	D2/3	R2	A2		
C3	B3	R3	B2	W1	A1
C4	C1	R4	A1	W2	A2
C5	D1	R5	A1		
CR1	C1	R6	A2		
CR2	B2/3	R7	B1/2		
CR4	B2/3	R8	A3		
CR5	B2/3	R9	B3		
CR6	B1/2	R10	B3		
J1	A2	R11	A2		
J2	D2	R12	A3		
J3	D2/3	R13	A1		
		R14	B1		
K1	C2				
		U1	D1		
L1	C2	U2	A1		
		U3	B2		

Add:

Repl.-Parts-List

A5 08175-66505 BD AY-CONTROL

REFERENCE DESIGNATOR	C D	H-P PART NUMBER	DESCRIPTION
C 1	3	0180-1794	C-F 22UF 35V
C 2	6	0180-0301	C-F 5UF 50V AL
C 3	3	0180-0291	C-F 1UF 35V
C 4	3	0180-1794	C-F 22UF 35V
C 5	5	0180-0582	C-F 270UF 40V
CR1	8	1901-0732	DIO PWR 1KV 1A
CR2	1	1901-1098	DIO-1N4150 50V
CR4	1	1901-1098	DIO-1N4150 50V
CR5	1	1901-1098	DIO-1N4150 50V
CR6	1	1901-1098	DIO-1N4150 50V
J 1	7	1251-5384	CONN 3-PIN N
J 2	8	1251-4246	CONN-3 PIN
J 3	8	1251-4246	CONN-3 PIN
K 1	1	0490-1232	RELAY 1C 24V
L 1	7	08175-61106	CHOKE 2X1.3mH
R 1	0	0757-0401	R-F 100 1% .125
R 2	9	0757-0278	R-F 1.78K1%
R 3	6	0757-0449	R-F 20K1% .125W
R 4	3	0757-0280	R-F 1K 1% .125W
R 5	9	0757-0442	R-F 10K1% .125W
R 6	6	0757-0465	R-F 100K1% .125
R 7	2	0757-0338	R-F 1K1% .25W F
R 8	9	0757-0442	R-F 10K1% .125W
R 9	9	0757-0442	R-F 10K1% .125W
R 10	0	0757-0401	R-F 100 1% .125
R 11	8	0698-3136	R-F 17.8K1%
R 12	3	0757-0438	R-F 5.11K1%
R 13	9	0757-0442	R-F 10K1% .125W
R 14	9	0698-3260	R-F 464K1% .125
U 1	7	1826-0393	IC LM317T
U 2	0	1826-0718	IC MC1404U5
U 3	7	1826-0161	IC 324
VR1	7	1902-0961	DIODE-ZENER
W 1	8	8150-0449	WIRE 24 RED
W 2	6	8150-0447	WIRE 24 BLK

A6 08175-66506 BD AY-SENSOR

REFERENCE DESIGNATOR	C D	H-P PART NUMBER	DESCRIPTION
J 1	2	1251-5369	CONN-POST-TP-BD
RT1	8	0853-0059	SENSOR-TEMP.
W 1	8	8150-0449	WIRE 24 RED
W 2	6	8150-0447	WIRE 24 BLK

MANUAL CHANGE 10

On Page 6-16/17, change the Table of Replaceable Parts to read:

	A40	U105	1820-0827	IC MC 10161P
	A40	RA24	1810-0713	R-NETWORK
ADD:	A40	R124	0698-7236	R-FXD 1K 1%

A40 BD AY-DATA:

R E V . D (intermediate Sulution)

R124 backloaded to U146 (Pin 8-13)
RA24 Pin 10 connected to U187 Pin24

R E V . E (Final Solution)

R124 located beside U146.

MANUAL CHANGE 11

On Page 6-7, change the Table of Replaceable Parts to read:

A2	S1-39	3101-2947	Keyswitch SPST

On Page 6-8, change the Table of Replaceable Parts to read:

A10	C55	0160-6596	C-FXD .47UF 20%

MANUAL CHANGE 12

On Page 6-5, Replaceable Parts List, change to read:

MP47	3050-0067	WASH BRS.375D

MANUAL CHANGE 13

On Page 6-16, Replaceable Parts List, add:

A40	R125	0757-0421	R-FXD 825 1% .125W

R125 is connected from U109 PIN8 (-5,2V)
to U109 PIN3

MANUAL CHANGE 14

On Page 6-16, change the Table of Replaceable Parts to read:

A40	R25	0757-0280	R-FXD 1K 1%

MANUAL CHANGE 15

On Page 6-10/11, change the Table of Replaceable Parts to read:

A20	U406,407,408, U409,410,411, U412,413	1818-3307	RAM 356 K

WITH 1818-3307 CONNECT PIN 1 and PIN 16 VIA BACKLOADED WIRE.

MANUAL CHANGE 16

On Page 6-5, Replaceable Parts List, change to read:

MP4	08175-04103	CVR TOP CABINET
MP5	08175-04104	CVR BOTTOM CAB.
MP6	08175-04105	CVR SIDE W.HANDLE
MP7	08175-04106	CVR SIDE PERF.
MP60	5001-0540	TRIM STRIP SIDE
MP41	5021-8405	FRAME FRONT 177H
MP48	5041-8801	FOOT
MP59	5041-8802	TRIM STRIP TOP
MP49	5041-8821	PNL REAR STD OFF
MP51	5041-8819	CAP STP HNDL FNT
MP50	5041-8820	CAP STP HNDL RR
MP52	5062-3704	STRAP HNDL 497.8D

MANUAL CHANGE 17

On Page 6-18/6-19, change the Table of Replaceable Parts to read:

A50	C7,8,12,16,17, C21,22,24,26,27, C28,29,30,31,32, C34,35,36,37,41, C42	0160-6623	C-FXD .10UF 10% 50V
#001: A50	C7-12,16-32, C34-37,40-42, C46-60	0160-6623	C-FXD .10UF 10% 50V

MANUAL CHANGE 18

On Page 6-5, Replaceable Parts List, change to read:

B1,2	08175-68501	FAN ASSY
W1	08175-61690	WIRE SET

Delete: W2,3,5

On Page 6-8, Replaceable Parts List, change to read:

A10	CR18,19	08175-88704	DIODE KIT

On Page 6-15,16,17,18, Replaceable Parts List, change to read:

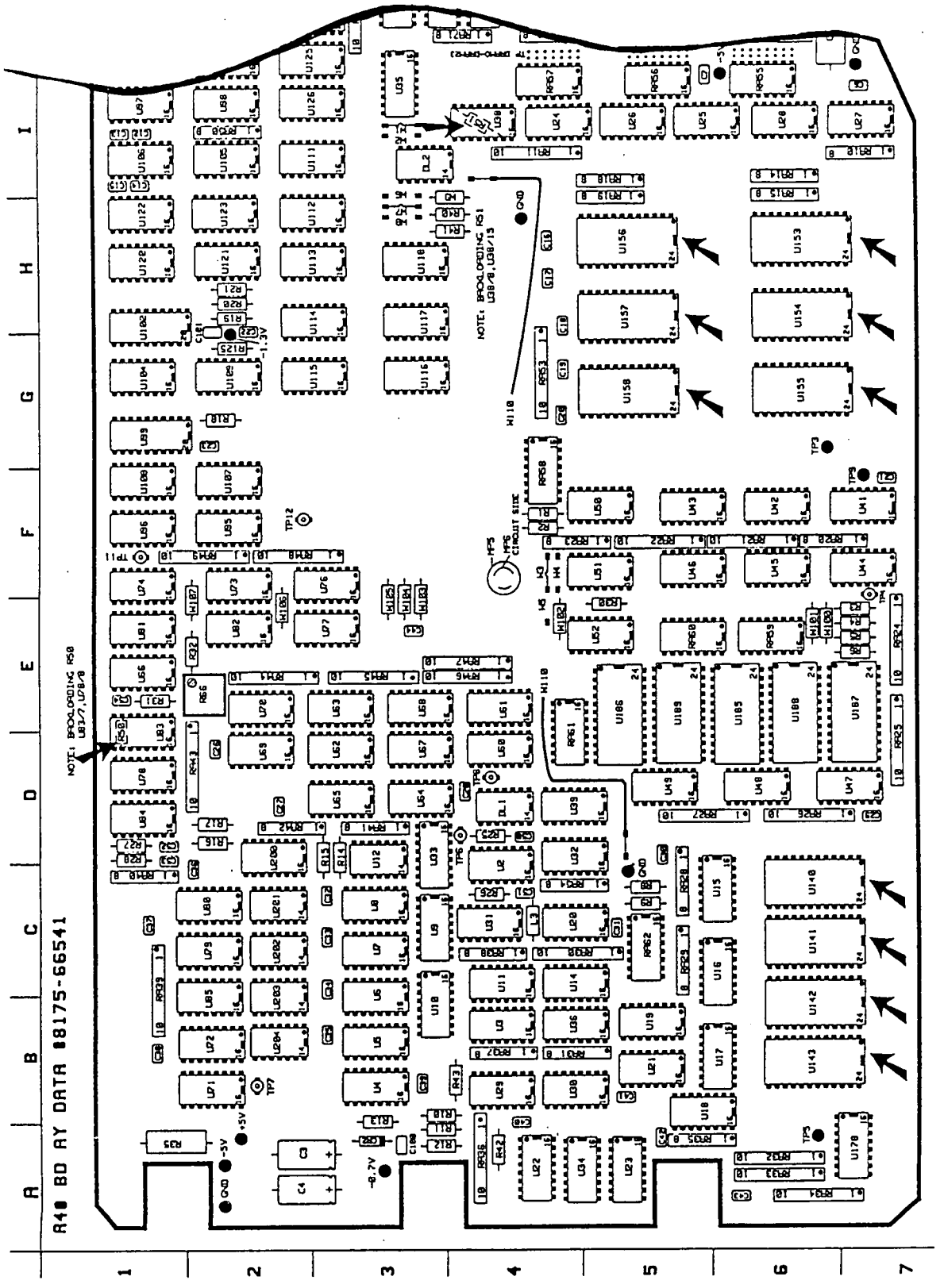
	MAINLIST	A40	08175-66541	BD AY DATA
ADD:	A40	R50,51	0698-0082	R-FXD 464 1% .125W
change:	A40	U140-141	1816-1720	IC 10474-7
	A40	U153-158	1816-1721	IC 10474-10
		U142-143	" "	
		BACKLOADING R50	U83/7, U78/8	
		BACKLOADING R51	U38/8, U38/15	

Delete: A40 RA34, R124, RA12,13,16,17,
U159-176
U144-152

COMPONENT- AND SCHEMATIC-CHANGES SEE ON FOLLOWING PAGES!

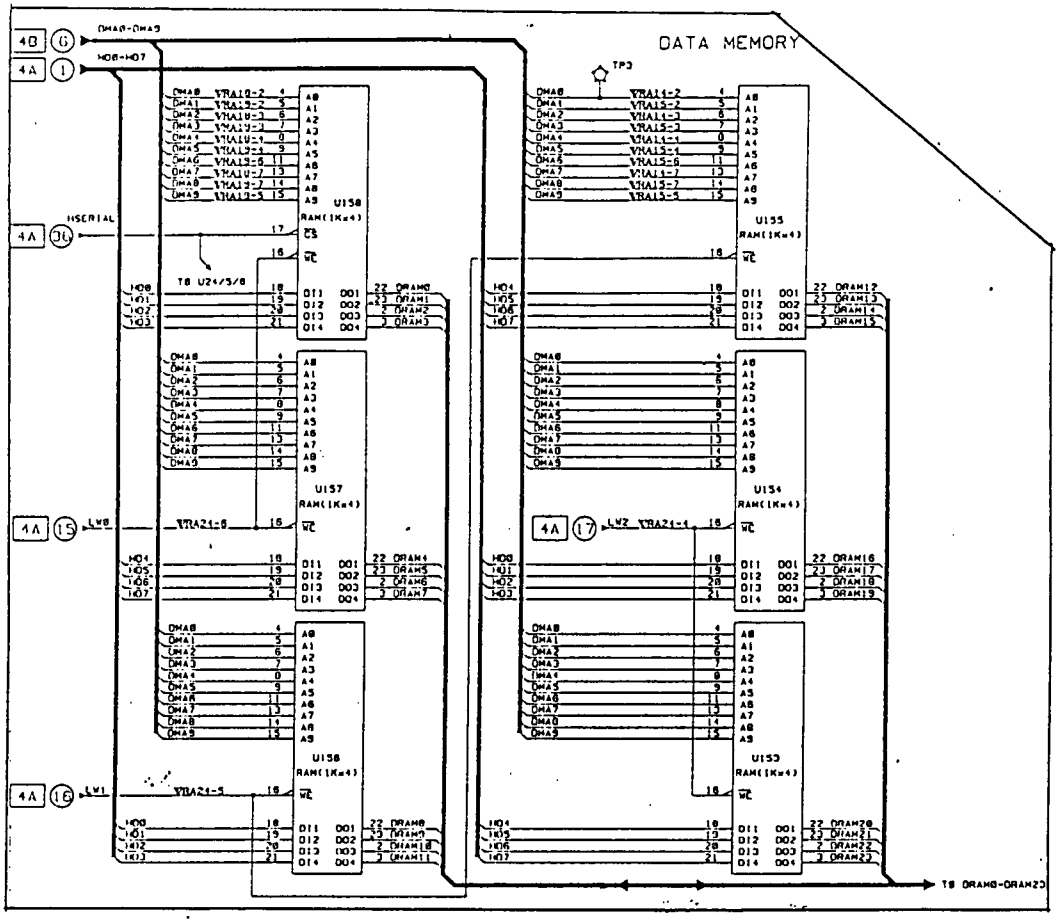
MANUAL CHANGE 18 (Cont.)

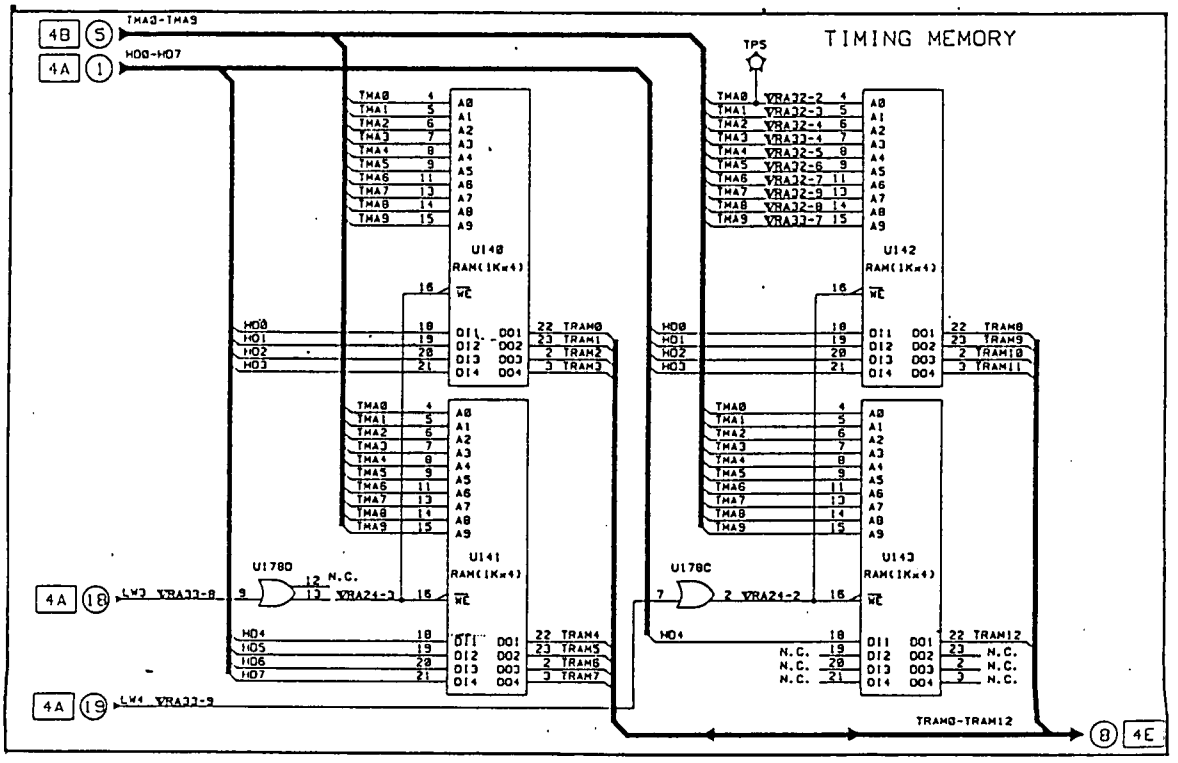
Component Layout, Page 8-142, change to read:



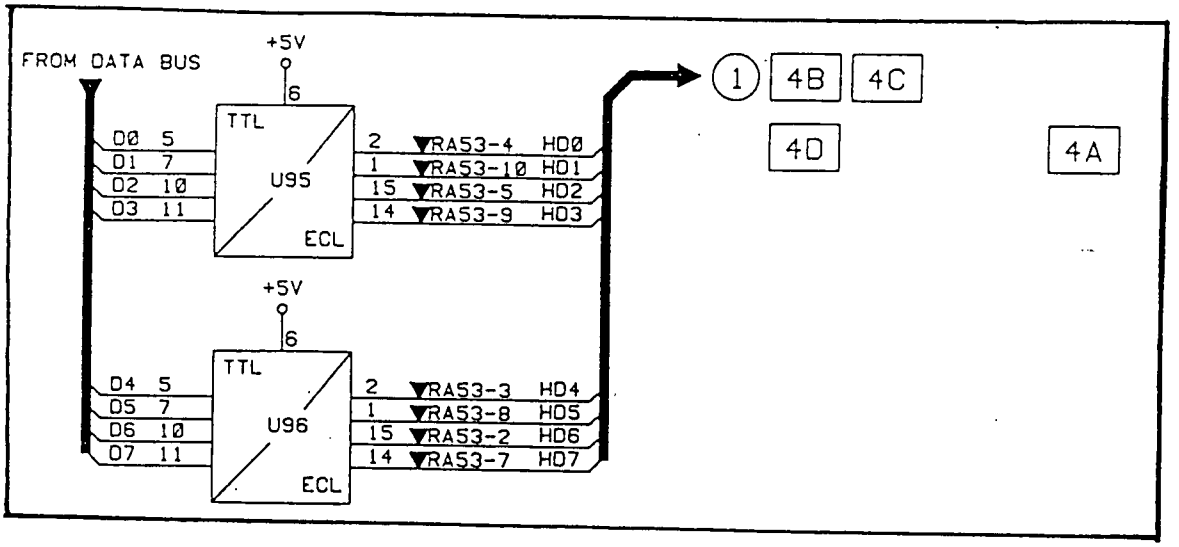
MANUAL CHANGE 18 (Cont.)

Change Schematic to read:





MANUAL CHANGE 18(Cont.)



Page 8-167

RA	GND PIN	POWER PIN	VOLTAGE LEVEL	RESISTOR VALUE
7	10	1	-5.2V	10PIN160/240
8	10	1	-5.2V	10PIN160/240
9	8	1	-5.2V	10PIN160/240
10	8	1	-5.2V	8PIN160/240
11	10	1	-5.2V	10PIN160/240
14	8	1	-5.2V	8PIN220/330
15	8	1	-5.2V	8PIN220/330
18	8	1	-5.2V	8PIN220/330
19	8	1	-5.2V	8PIN220/330
37	8	1	-5.2V	8PIN160/240
38	8	1	-5.2V	8PIN160/240
71	8	1	-5.2V	8PIN160/240

DELETE RA12, RA13, RA16, RA17

Page 8-173

REF.DES.	-5.2V	+5V	-15V	+15V	GND
U140	12				1,24
U141	12				1,24
U142	12				1,24
U143	12				1,24

DELETE U144-U152

Page 8-171

REF.DES.	-5.2V	+5V	-15V	+15V	GND
U153	12				1,24
U154	12				1,24
U155	12				1,24
U156	12				1,24
U157	12				1,24
U158	12				1,24

DELETE U159-U176

Page 8-173

MANUAL CHANGE 18 (Cont.)

Change in Adustment Procedure
MANUAL Page 5-3 Powersupply Board:

TESTCONNECTOR	ADJUST	TEST LIMIT
+5V	R21	+4.98V +/- 50mV
-5.2V	(R21)	-5.27V +/- 70mV

5-8 DATA BOARD:

TP-5V	-5.17V	+/- 70mV
TP+5V	+4.98V	+/- 50mV

MANUAL CHANGE 19

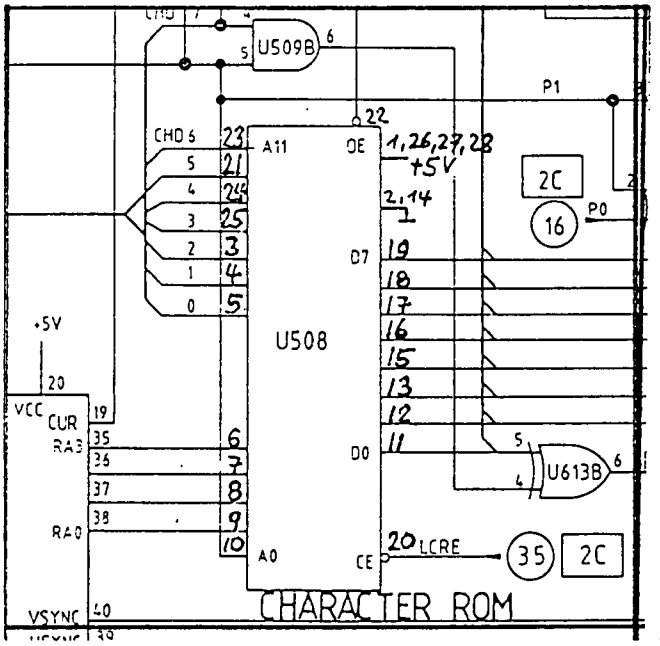
On Page 6-5, Replaceable Parts List, change to read:

A20		08175-66525	BD AY CPU

On Page 6-11, Replaceable Parts List, change to read:

A20	U508	08118-13705	ROM5

On Page 8-99, Schematic, change to read:



MANUAL CHANGE 20

On Page 6-10, Replaceable Parts List,

Delete: A20 MP2

MANUAL CHANGE 21

On Page 6-14, change the Table of Replaceable Parts to read:

A30	U9,10,30,31	1816-1594	IC MBM10422A-7Z
A40	U185,186,187 U188,189	1816-1594	IC MBM10422A-7Z

MANUAL CHANGE 22

On Page 6-8, change the Table of Replaceable Parts to read:

A10	CR5	1901-0731	DIO PWR RECT.

On Page 6-15/16, change the Table of Replaceable Parts to read:

A40	C50	0160-3872	C-FXD 2.2PF 200V
	R25	0698-3488	R-FXD 442 1% .125

MANUAL CHANGE 23

On Page 6-9, change the Table of Replaceable Parts to read:

A10	R29	0757-0440	R-FXD 7,5K 1%
A10	U8	1826-2357	IC TL 780-12CKC

MANUAL CHANGE 24

On Page 6-17, change the Table of Replacealbe Parts to read:

A40	(B-3119)	U140,141	08175-62901	ASSY RAM IC
A40	(B-3119)	U153,154 U155,156, U157,158, U142,143	08175-62902	ASSY RAM IC

MANUAL CHANGE 25

On Page 6-23/24, change the Table of Replaceable Parts to read:

A10	C55	0160-3097	CAP 0.47uF 50V

MANUAL CHANGE 26

On Page 6-5, change the Table of Replaceable Parts to read:

A10		08175-66511	BD AY PWR SPLY

On Page 6-8/9, change the Table of Replaceable parts to read:

		EDC-LBL		
A10	CR1	A-3205	1906-0408	DIO-FW BRDG
	S1		3101-2737	SW-PUSHBUTTO

MANUAL CHANGE 27

On Page 6-5, Replaceable Parts List ADD:

MP71	5021-2840	KEY-LOCK-FOO

Additional needed for MP48 (Rear Bottom Feet)

MANUAL CHANGE 28

On Page 6-12, change the Table of Repl. Parts List to read:

		EDC-LBL		
A30	R15	D-3305	0698-4442	RES 4.42K
	R16		0757-0442	RES 10K 1%
	R17		0757-0453	RES 30.1K
	R23		0757-0449	RES 20K 1%
	R25		0698-4471	RES 7.15K
	R50		0698-4439	RES 3.24K 1%

On Page 6-12, Repl. Parts List add:

		EDC-LBL		
A30	CR68	D-3305	0122-0161	DIO-VVC 2.15C

MANUAL CHANGE 28 (Cont.)

On Page 8-131, Schematic change to read:

CR68 is added in parallel to CR67 with the same polarity

On Page 8-135, Schematic change toeread:

Correct value of R15, R16, R17

On Page 8-137, Schematic change to read:

Correct value of R23, R25, R50

MANUAL CHANGE 29

On Page 6-7, Repl.Parts List, DELETE:

A2	J26,27	8159-0005	RES O CWM

MANUAL CHANGE 30

On Page 6-15, Repl.Parts List change to read:

EDC-LBL			
B-3343	A40	0160-5737	CAP 82PF 200