Revision 1.10

10-Oct, 2014

Keysight Method of Implementation (MOI) for MIPI D-PHY Conformance Tests Using Keysight E5071C ENA Network Analyzer Option TDR

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1. Modification Record

Revision	Comments	Issue Date
1.00	First Release	Dec 1, 2011
1.10	Updated procedures to Conformance Test Suite for D-PHY Physical Layer Version 1.1 Revision 03.	Oct 10, 2014

2. Purpose

This document is intended to provide the measurement procedures for the interface S-parameter and impedance tests defined in the MIPI Alliance Specification for D-PHY. The instrument operations contained in this document are designed for Keysight E5071C ENA Network Analyzer Option TDR.

3. References

MIPI Alliance Conformance Test Suite for D-PHY Physical Layer Version 1.1 Revision 03
MIPI Alliance Specification for D-PHY Version 1.1

4. Resource Requirements

1. ENA Series Network Analyzer with Enhanced Time Domain Option
   Note: Use the test set option of 4.5 GHz or above, and either of 2-port and 4-port.
   Note: E5071C firmware revision A.11.31 or above is installed.
   Note: E5071C-TDR application software revision A.01.56 or above is installed.
2. Electronic Calibration Module N4431B (for 4.5/6.5/8.5 GHz models) or N4433A (14/20 GHz models)
3. 3.5 mm cables of 4 GHz bandwidth or above x2

5. Test Procedure

5.1. Outline of Test Procedure

1. **Instrument Setup**
2. **Calibration and Adjustment**

   Time Domain Calibration with the Setup Wizard in the TDR Application Software

   Frequency Domain Calibration with the VBA Macro Program

3. **Measurements and Data Analysis**

   Time Domain Measurements

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   - HS-TX Single-Ended Output Impedance Mismatch
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   Frequency Domain Measurements

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   - HS-TX Common-Mode Return Loss
   - HS-TX Mode Conversion Limits
   - HS-RX Differential Return Loss
   - HS-RX Common-Mode Return Loss
   - HS-RX Mode Conversion Limits

*Note: Hard Keys (Keys located on the Front panel of E5071C) are displayed in Blue color and **Bold**. (Example:* **Avg**, **Analysis***)*

*Note: Soft keys (Keys on the screen) are displayed in **Bold**. (Example:* **S11**, **Real**, **Transform***)*

*Note: Buttons (in the TDR or VBA) are displayed in Green color and **Bold**. (Example:* **Trace**, **Rise Time**)

*Note: Tabs (in the TDR) are displayed in Brown color and **Bold**. (Example:* **Setup**, **Trace Control**)

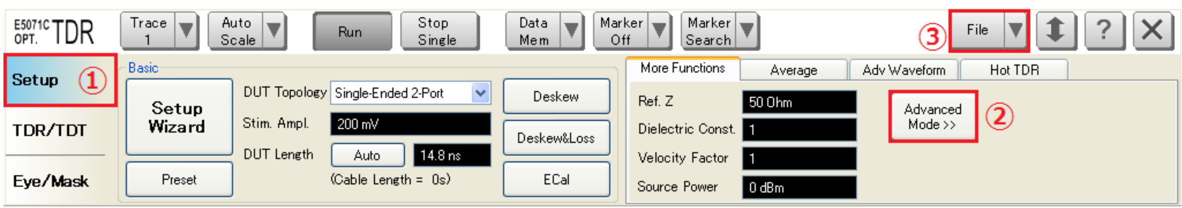
5.2. Instrument Setup

This section describes the procedures for recalling the state file and VBA macro that support the instrument setup. Download "E5071C-TDR Test Package for MIPI D-PHY Tx/Rx Devices" from www.keysight.com/find/ena-tdr_dphy-txrx.

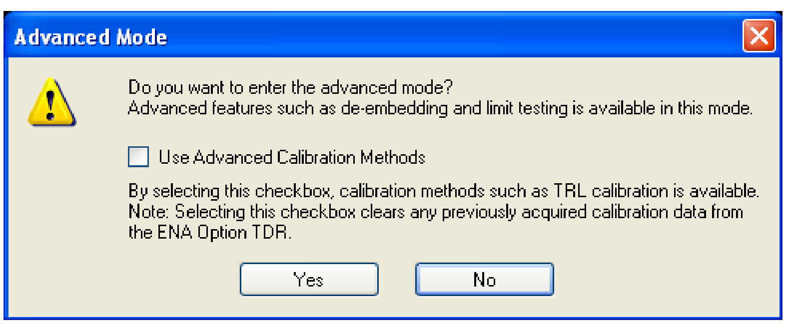
Extract the zip file and transfer the extracted files to the instrument with a USB flash memory. For manual measurement settings, refer to 6 Appendix.

5.2.1. Recalling State File

1. If TDR setup wizard appears, click **Close** button on the wizard.
2. Open **Setup** tab (item1).
3. Click **Advanced Mode** (item2).



4. A dialog box appears requesting for confirmation. Then click **Yes**. (Clear the check box for "Use Advanced Calibration Methods")

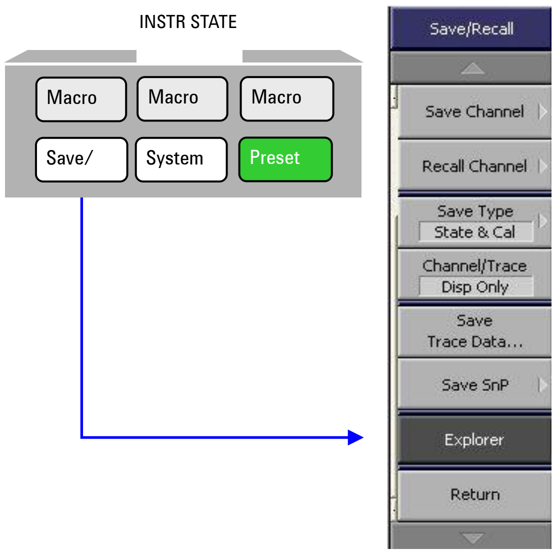


5. Click **File** (item3) and select **Recall State** to open the Recall State dialog box.
6. Specify the folder and appropriate state file name, and click **Open**.

E5071C Test Set Option	State File Name
240/245/260/265/280/285/440/445/460/465/480/485	MIPI_D-PHYv1.1_TxRx_24x-48x.tdr
2D5/2K5/4D5/4K5	MIPI_D-PHYv1.1_TxRx_2D5-4K5.tdr

5.2.2. Running VBA macro program

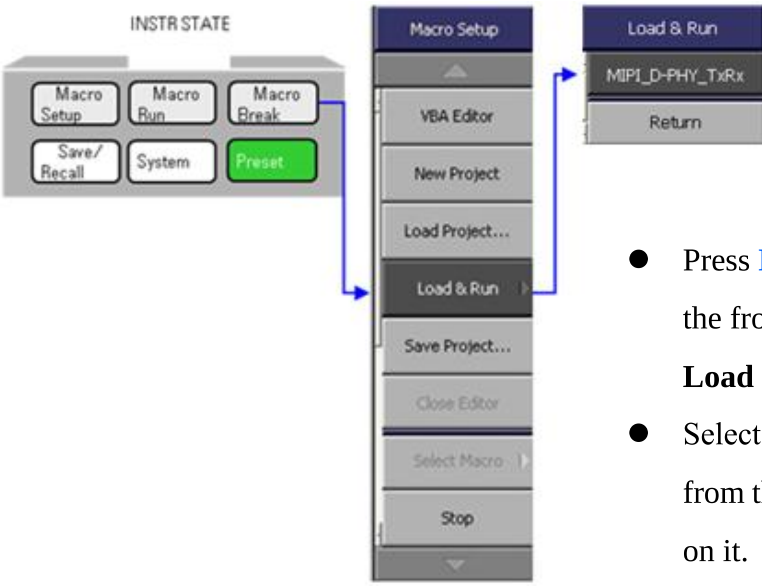
1. Installing the VBA macro program



Obtain the VBA macro program from Keysight and install it on the E5071C.

- Press **Save/Recall** on the front panel, then press the **Explorer** soft key.
- Using **Explorer**, copy the file to the "D:¥VBA" folder.

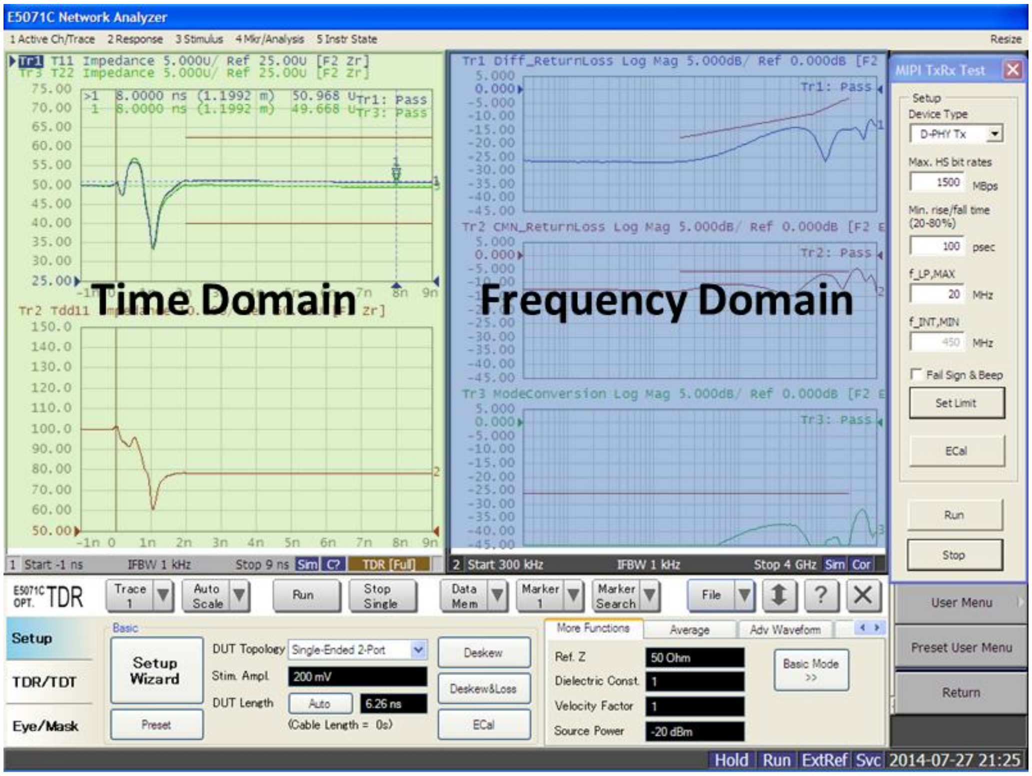
2. Running the VBA macro program



- Press **Macro Setup** button from the front panel, then click the **Load & Run** soft key.
- Select "MIPI_D-PHYv1.1_TxRx" from the soft key menu and click on it.

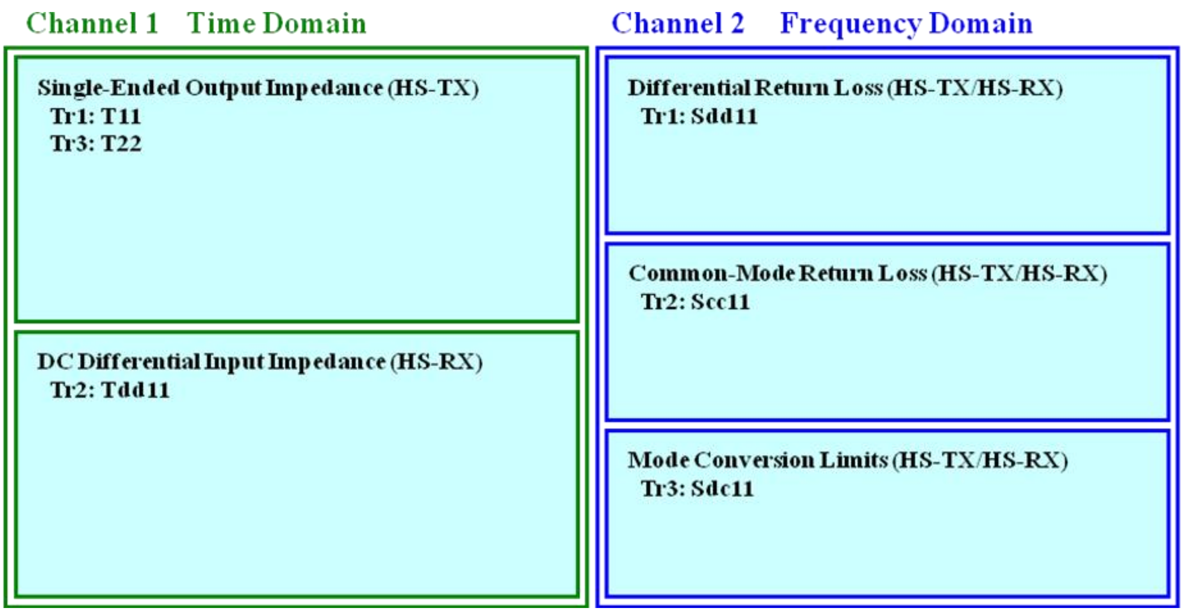
Screen Configuration

This section describes the screen configuration of ENA Option TDR.



Channel1 dedicated to time domain measurements is controlled by the TDR application software located at the bottom of the screen and Channel2 dedicated to frequency domain measurements is controlled by the VBA macro program located at the upper right of the screen.

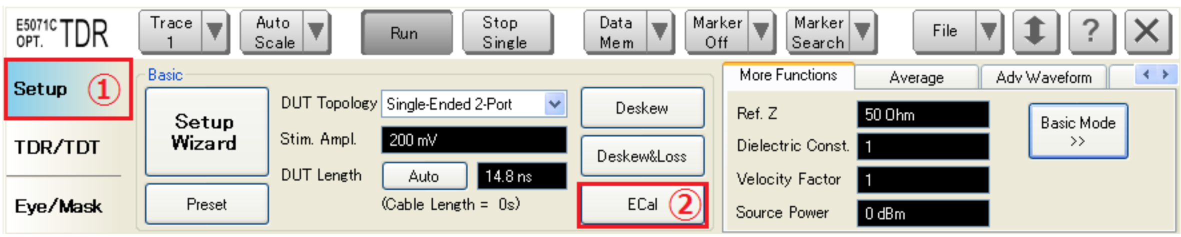
Description of Measurement Window



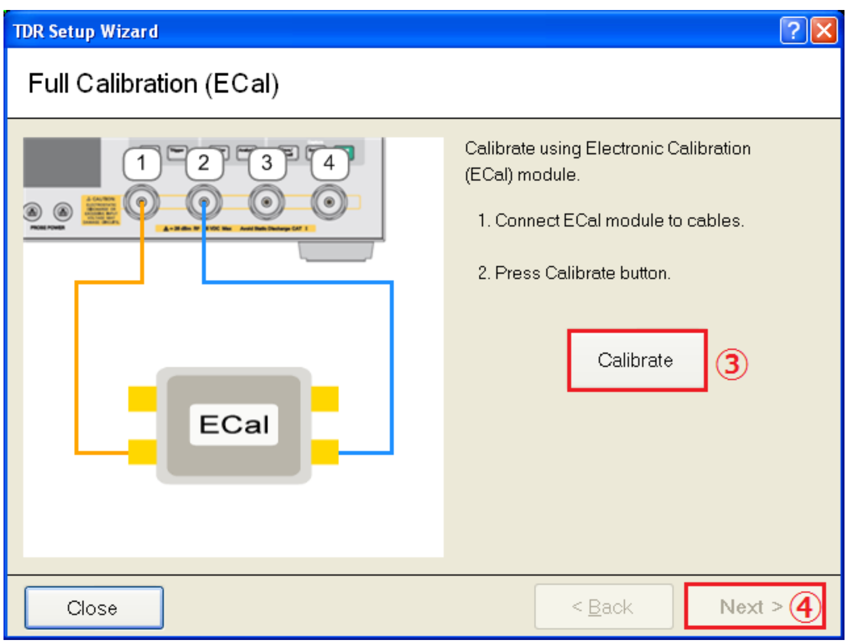
5.3. Calibration and Adjustment

5.3.1. Time Domain Calibration

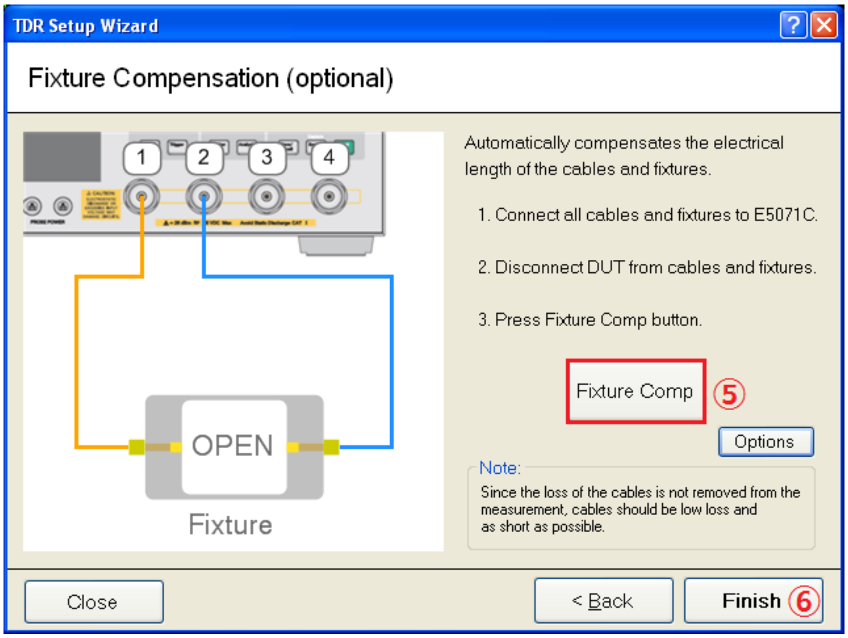
1. Connect the test cables to the port 1 and port 2 on the E5071C.
2. Press **Channel Next** key to select Channel1.
3. Open **Setup** tab (item1).
4. Click **ECal** (item2) to launch the Full Calibration (ECal) and Fixture Compensation wizard.



5. Connect the test cables to the ECal module.
6. Click **Calibrate** (item3), then it will start the full calibration. Wait until the check-mark appears on the right of Calibrate button.
7. Click **Next** (item4).

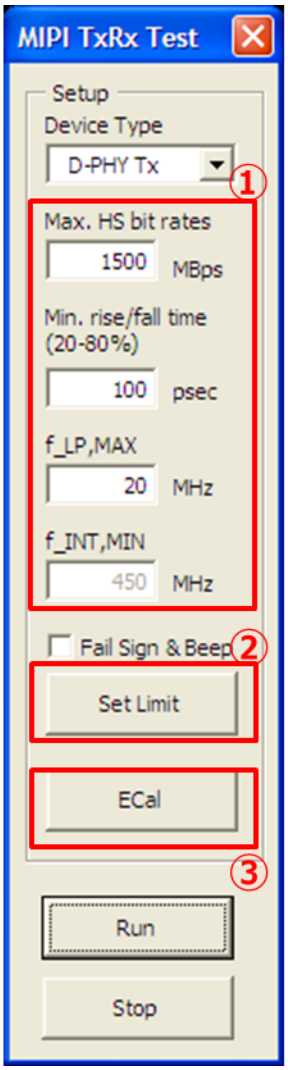


8. Connect port 1 and port 2 cables to the test fixtures and make the fixture end open.
9. Click **Fixture Comp** (item5), then it will start the fixture compensation. Wait until the check-mark appears on the right of Fixture Comp button.
10. Click **Finish** (item6).



5.3.2. Frequency Domain Calibration

1. Input the parameters expected with the DUT (item1)[1].
2. Click **Set Limit** (item2).
3. Connect port 1 and port 2 cables to the ECal module.
4. Click **ECal** (item3) to perform the Full Calibration (ECal).



[1] Minimum rise and fall time (20-80%) of 100 ps is applicable for Max. HS bit rates > 1000 Mbps. For Max. HS bit rates ≤ 1000 Mbps, should not use values below 150 ps.

5.4. HS-TX S-Parameters

5.4.1. Differential Return Loss (SDD11)

5.4.1.1. Purpose

To verify that the Differential Return Loss of the DUT's Clock and Data Lane HS transmitters exceeds the minimum conformance limits.

5.4.1.2. Test Procedure

1. Press **Channel Next** key to select Channel2.
2. Press **Channel Max** key to enlarge Channel2.
3. Ensure the VBA shows the desired maximum HS bit rates, minimum rise and fall times (20-80%), maximum toggle frequency for Low Power mode.
4. On the VBA macro, select "D-PHY Tx" from the drop down list and click Set Limit button.
5. Power on and configure the DUT to force its HS-TX into a fixed HS state, transmitting a continuous, repeating pattern on all Clock and Data Lanes.
6. Connect the DUT's Data Lane 0 transmitter to the Test System.
7. Click **Run** button on the VBA macro.

   Note: If the trace data is not stable, it is recommended that adjusting the IF Bandwidth narrower than the default setting, and check if the trace becomes stable: **Avg** > IF Bandwidth > (set a value).
8. Read the pass/fail sign on the trace (item 1 in Figure 5-1).
9. Repeat the previous three steps for all other Data Lane, and the Clock Lane.

5.4.1.3. Observable Results

For all Clock and Data Lanes, verify that the SDD11 HS-TX Differential Return Loss meets or exceeds the limits shown in the figure below.

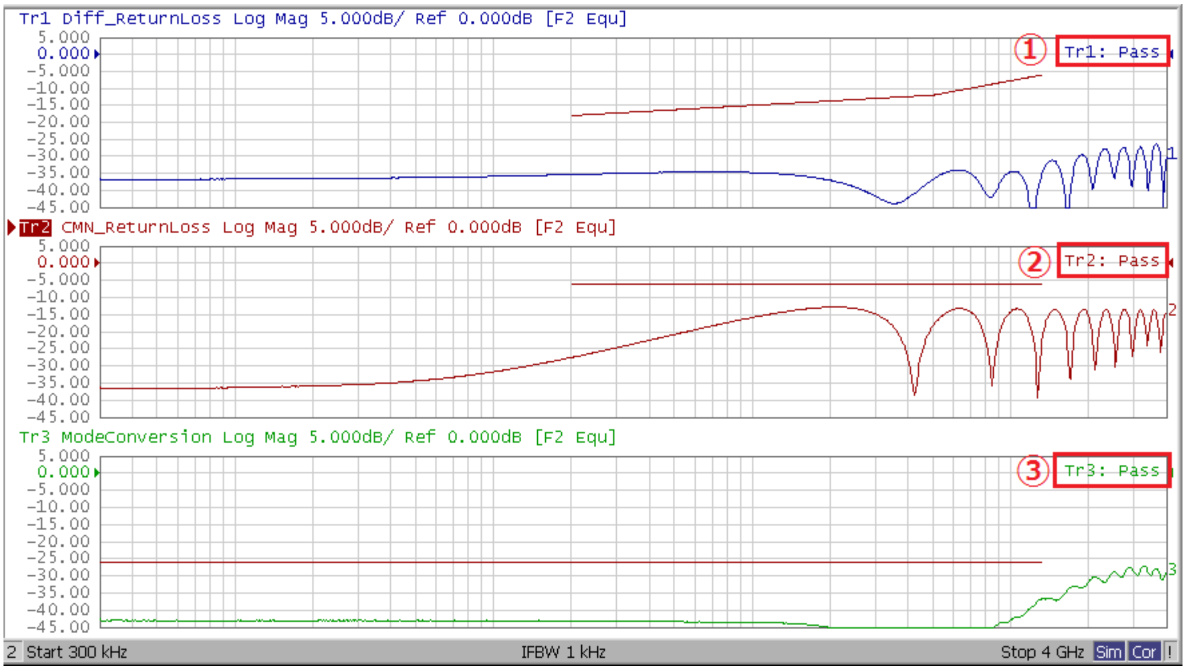


Figure 5-1 Differential Return Loss, Common-Mode Return Loss and Mode Conversion Limits (HS-TX) Example

5.4.2. Common-Mode Return Loss (SCC11)

5.4.2.1. Purpose

To verify that the Common-Mode Return Loss of the DUT's Clock and Data Lane HS transmitters exceeds the minimum conformance limits.

5.4.2.2. Test Procedure

1. Press **Channel Next** key to select Channel2.
2. Press **Channel Max** key to enlarge Channel2.
3. Ensure the VBA shows the desired maximum HS bit rates, minimum rise and fall times (20-80%), maximum toggle frequency for Low Power mode.
4. On the VBA macro, select "D-PHY Tx" from the drop down list and click Set Limit button.
5. Power on and configure the DUT to force its HS-TX into a fixed HS state, transmitting a continuous, repeating pattern on all Clock and Data Lanes.

6. Connect the DUT's Data Lane 0 transmitter to the Test System.
7. Click **Run** button on the VBA macro.

   Note: If the trace data is not stable, it is recommended that adjusting the IF Bandwidth narrower than the default setting, and check if the trace becomes stable: **Avg** > IF Bandwidth > (set a value).
8. Read the pass/fail sign on the trace (item 2 in Figure 5-1).
9. Repeat the previous three steps for all other Data Lanes, and the Clock Lane.

5.4.2.3. Observable Results

For all Clock and Data Lanes, verify that the SCC11 HS-TX Common-Mode Return Loss meets or exceeds the limits shown in the figure below.

5.4.3. Mode Conversion Limits (SDC11)

5.4.3.1. Purpose

To verify that the Mode Conversion S-parameters of the DUT's Clock and Data Lane HS transmitters exceed the minimum conformance limits.

5.4.3.2. Test Procedure

1. Press **Channel Next** key to select Channel2.
2. Press **Channel Max** key to enlarge Channel2.
3. Ensure the VBA shows the desired maximum HS bit rates, minimum rise and fall times (20-80%), maximum toggle frequency for Low Power mode.
4. On the VBA macro, select "D-PHY Tx" from the drop down list and click Set Limit button.
5. Power on and configure the DUT to force its HS-TX into a fixed HS state, transmitting a continuous, repeating pattern on all Clock and Data Lanes.
6. Connect the DUT's Data Lane 0 transmitter to the Test System.
7. Click **Run** button on the VBA macro.

   Note: If the trace data is not stable, it is recommended that adjusting the IF Bandwidth narrower than the default setting, and check if the trace becomes stable: **Avg** > IF

Bandwidth > (set a value).

8. Read the pass/fail sign on the trace (item 3 in Figure 5-1).
9. Repeat the previous three steps for all other Data Lanes, and the Clock Lane.

5.4.3.3. Observable Results

For all Clock and Data Lanes, verify that the SDC11 HS-TX Mode Conversion Loss meets or exceeds the limits shown in the figure below.

5.4.4. Single-Ended Output Impedance (Z_{OS})

5.4.4.1. Purpose

To verify that the Single-Ended Output Impedance (Z_{OS}) of the DUT's HS transmitters is within the conformance limits.

5.4.4.2. Test Procedure

1. Press **Channel Next** key to select Channel1.
2. Press **Channel Max** key to enlarge Channel1.
3. Power on and configure the DUT to force its HS-TX into a fixed HS state, transmitting a continuous, repeating pattern on all Clock and Data Lanes.
4. Connect the DUT's Data Lane 0 transmitter to the Test System.

   Note: If the trace data is not stable, it is recommended that adjusting the IF Bandwidth narrower than the default setting, and check if the trace becomes stable: **Setup** > **Average** > IF Bandwidth > (set a value).
5. Click **Stop Single** for Time Domain measurement.
6. Read the marker values[2] (item 1 in Figure 5-2) as Z_{OS} for the Dp and Dn pins.
7. Repeat the previous three steps for all other Data Lanes, and Clock lane.

5.4.4.3. Observable Results

For all Clock and Data Lanes, verify that Z_{OS} is between 40 and 62.5 ohms for both the Dp and Dn pins.

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[2] The markers are placed at 8 nsec by default. If the DUT response is not flat around the marker, adjust the marker position and horizontal scale.

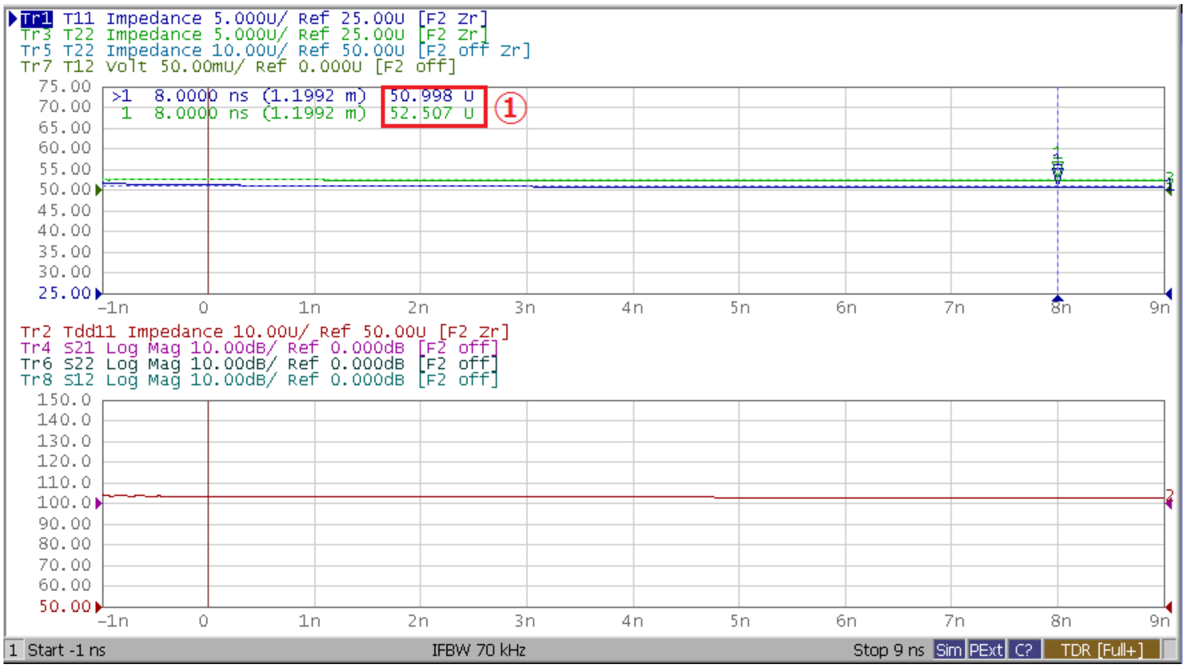


Figure 5-2 Single Ended Output Impedance (HS-TX) Example

5.4.5. Single-Ended Output Impedance Mismatch (ΔZ_{OS})

5.4.5.1. Purpose

To verify that the Single-Ended Output Impedance Mismatch (ΔZ_{OS}) of the DUT's HS transmitter is within the conformance limits.

5.4.5.2. Test Procedure

1. Obtain the Z_{OS} values for each Clock and Data Lane from Single-Ended Output Impedance.
2. Compute the ΔZ_{OS} value, as described below.
   - $\Delta Z_{OS} = 2(|Z_{OSDP} - Z_{OSDN}| / (Z_{OSDP} + Z_{OSDN}))$
3. For each lane, compute ΔZ_{OS} as described above.

5.4.5.3. Observable Results

For all Clock and Data Lanes, verify that ΔZ_{OS} is less than 10%.

5.5. HS-RX S-Parameters

5.5.1. Differential Return Loss (SDD11)

5.5.1.1. Purpose

To verify that the Differential Return Loss of the DUT's Clock and Data Lane HS receivers exceeds the minimum conformance limits.

5.5.1.2. Test Procedure

1. Press **Channel Next** key to select Channel2.
2. Press **Channel Max** key to enlarge Channel2.
3. Ensure the VBA shows the desired maximum HS bit rates, minimum rise and fall times (20-80%), maximum toggle frequency for Low Power mode, and minimum RF frequency.
4. On the VBA macro, select "D-PHY Rx" from the drop down list and click Set Limit button.
5. Power on and configure the DUT to force its RX into fixed state where the HS-RX termination is enabled.
6. Connect the DUT's Data Lane 0 receiver to the Test System.
7. Click **Run** button on the VBA macro.

   Note: If the trace data is not stable, it is recommended that adjusting the IF Bandwidth narrower than the default setting, and check if the trace becomes stable: **Avg** > IF Bandwidth > (set a value).
8. Read the pass/fail sign on the trace (item 1 in Figure 5-3).
9. Repeat the previous three steps for all other Data Lanes, and the Clock Lane.

5.5.1.3. Observable Results

For all Clock and Data Lanes, verify that the SDD11 HS-RX Differential Return Loss meets or exceeds the limits shown in the figure below.

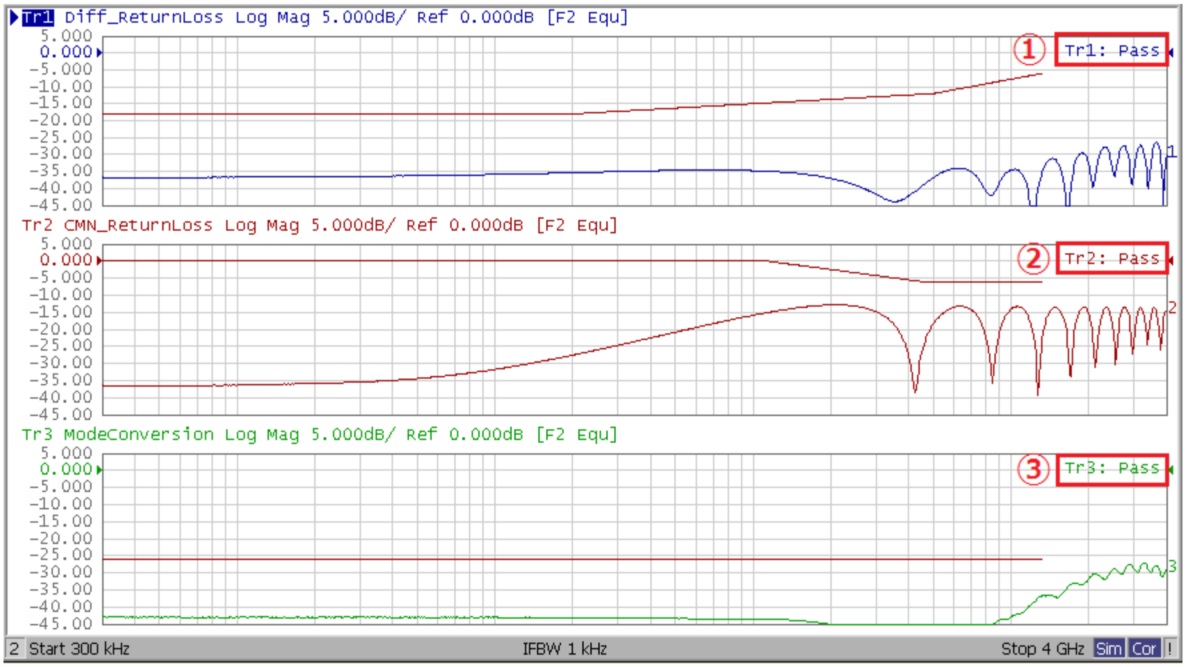


Figure 5-3 Differential Return Loss, Common-Mode Return Loss and Mode Conversion Limits (HS-RX) Example

5.5.2. Common-Mode Return Loss (SCC11)

5.5.2.1. Purpose

To verify that the Common-Mode Return Loss of the DUT's Clock and Data Lane HS receivers exceeds the minimum conformance limits.

5.5.2.2. Test Procedure

1. Press **Channel Next** key to select Channel2.
2. Press **Channel Max** key to enlarge Channel2.
3. Ensure the VBA shows the desired maximum HS bit rates, minimum rise and fall times (20-80%), maximum toggle frequency for Low Power mode, and minimum RF

frequency.

4. On the VBA macro, select "D-PHY Rx" from the drop down list and click Set Limit button.
5. Power on and configure the DUT to force its RX into fixed state where the HS-RX termination is enabled.
6. Connect the DUT's Data Lane 0 receiver to the Test System.
7. Click **Run** button on the VBA macro.

   Note: If the trace data is not stable, it is recommended that adjusting the IF Bandwidth narrower than the default setting, and check if the trace becomes stable: **Avg** > IF Bandwidth > (set a value).
8. Read the pass/fail sign on the trace (item 2 in Figure 5-3).
9. Repeat the previous three steps for all other Data Lanes, and the Clock Lane.

5.5.2.3. Observable Results

For all Clock and Data Lanes, verify that the SCC11 HS-RX Common-Mode Return Loss meets or exceeds the limits show in the figure below.

5.5.3. Mode Conversion Limit (SDC11)

5.5.3.1. Purpose

To verify that the Mode Conversion S-parameters of the DUT's Clock and Data Lane HS receivers exceed the minimum conformance limits.

5.5.3.2. Test Procedure

1. Press **Channel Next** key to select Channel2.
2. Press **Channel Max** key to enlarge Channel2.
3. Ensure the VBA shows the desired maximum HS bit rates, minimum rise and fall times (20-80%), maximum toggle frequency for Low Power mode, and minimum RF frequency.
4. On the VBA macro, select "D-PHY Rx" from the drop down list and click Set Limit button.

5. Power on and configure the DUT to force its RX into fixed state where the HS-RX termination is enabled.
6. Connect the DUT's Data Lane 0 receiver to the Test System.
7. Click **Run** button on the VBA macro.

   Note: If the trace data is not stable, it is recommended that adjusting the IF Bandwidth narrower than the default setting, and check if the trace becomes stable: **Avg** > IF Bandwidth > (set a value).
8. Read the pass/fail sign on the trace (item 3 in Figure 5-3).
9. Repeat the previous three steps for all other Data Lanes, and the Clock Lane.

5.5.3.3. Observable Results

For all Clock and Data Lanes, verify that the SDC11 HS-RX Mode Conversion Loss meets or exceeds the limits shown in the figure below.

5.5.4. DC Differential Input Impedance (Z_{ID})

5.5.4.1. Purpose

To verify that DC Differential Input Impedance (Z_{ID}) of the TUT's HS-RX line termination is within the conformance limits.

5.5.4.2. Test Procedure

1. Press **Channel Next** key to select Channel1.
2. Press **Channel Max** key to enlarge Channel1.
3. Power on and configure the DUT to force its RX into fixed state where the HS-RX termination is enabled.
4. Connect the DUT's Data Lane 0 receiver to the Test System.

   Note: If the trace data is not stable, it is recommended that adjusting the IF Bandwidth narrower than the default setting, and check if the trace becomes stable: **Setup** > **Average** > IF Bandwidth > (set a value).
5. Click **Stop Single** for Time Domain measurement.

6. Read the marker value[3] (item 1 in Figure 5-4) as Z_{ID}.

7. Repeat the previous three steps for all other Data Lanes, and Clock Lane.

5.5.4.3. Observable Results

For all Clock and Data Lanes, verify that Z_{ID} is between 80 and 125 Ohms.

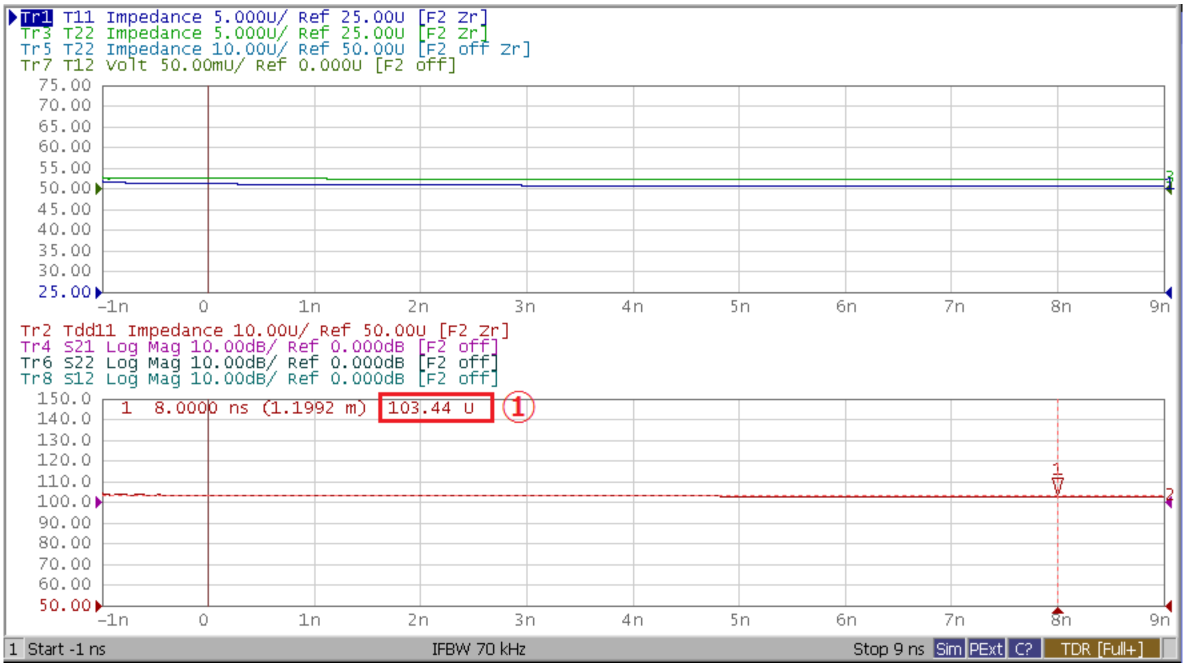


Figure 5-4 DC Differential Input Impedance (HS-RX) Example

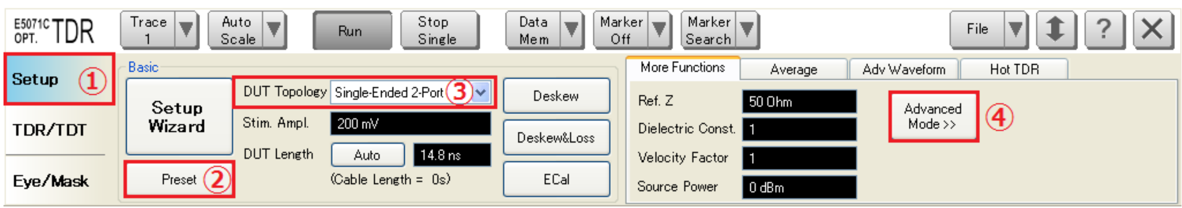
[3] The marker is placed at 8 nsec by default. If the DUT response is not flat around the marker, adjust the marker position and horizontal scale.

6. Appendix

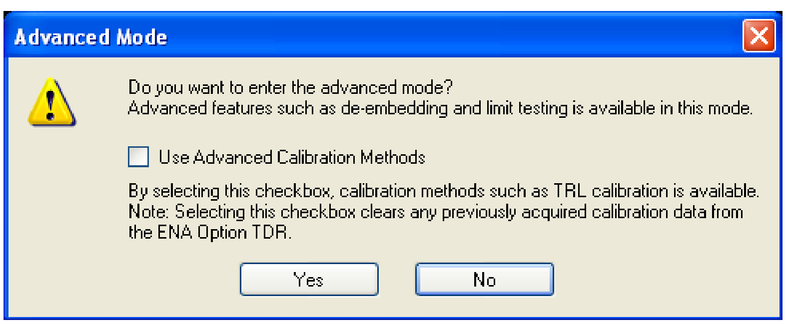
6.1. Manual Setup for Time Domain Measurement

6.1.1. Starting Setup

1. If TDR setup wizard was appeared, click **Close** button in the TDR setup wizard.
2. Open **Setup** tab (item1).
3. Click **Preset** (item2).
4. A dialog box appears requesting for confirmation. Then click **OK**.
5. Set **DUT Topology** (item3) to "Single-Ended 2-port".
6. Set **Source Power** to -20 dBm. (in More Function Tab)
7. Set **IF Bandwidth** to 1 kHz. (in Average Tab)
8. Click **Advanced Mode** (item4).



9. A dialog box appears requesting for confirmation. Then click **Yes** (Clear the check box for "Use Advanced Calibration Methods").

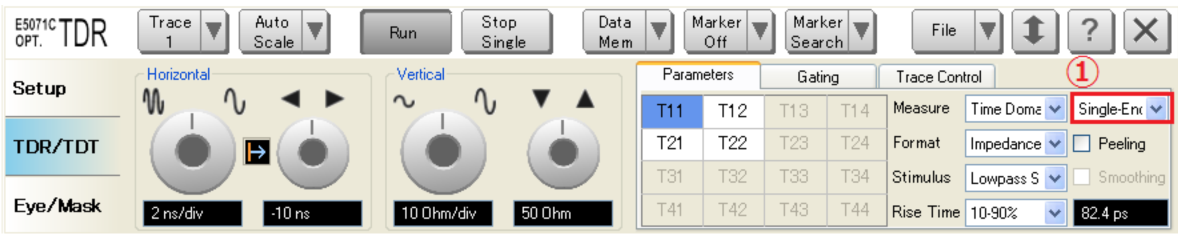


10. Click **Stop Single**.
11. Press **Display**.
12. Set **Num of Traces** to 3.
13. Click **Allocate Traces** > .

6.1.2. HS-TX Single-Ended Output Impedance

6.1.2.1. Measurement Setup

1. Open **TDR/TDT** tab.
2. Select **Trace1**.
3. Open **Parameters** tab.
4. Select the **Topology** (item1) of DUT to Single-Ended.

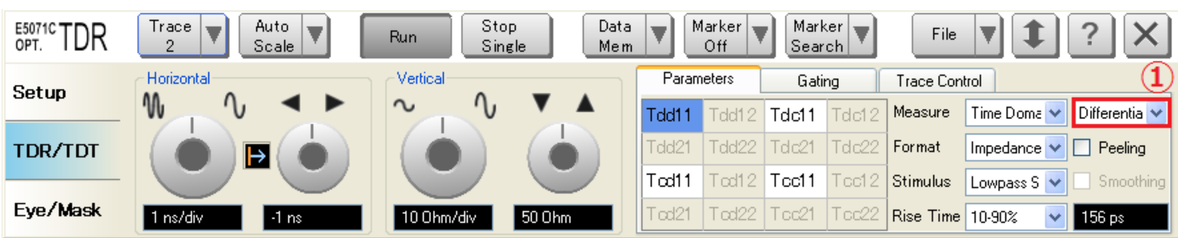


5. Set **Measure** to Time Domain.
6. Select **Format** to Impedance.
7. Set **Rise Time** to 100 ps (20-80%).
8. Click **T11** in the table.
9. Click the box below the left knob under Horizontal.
10. Input 1 nsec/div with the Entry dialog box.
11. Click the box below the right knob under Horizontal.
12. Input -1 nsec with the Entry dialog box.
13. Click the box below the left knob under Vertical.
14. Input 5 Ohm/div with the Entry dialog box.
15. Click the box below the right knob under Vertical.
16. Input 25 Ohm with the Entry dialog box.
17. Open **Trace Control** tab.
18. Clear Marker check box under Coupling.
19. Click **Trace Settings Copy** button. Then Trace Settings Copy dialog box appears.
20. Select **Trace1** in the From list.
21. Select **Trace3** in the To list.
22. Click **Copy**.

23. Click **Close**.
24. Select **Trace3**.
25. Open **Parameters** tab.
26. Click **T22** in the table.
27. Select **Trace1**.
28. Click **Maker** menu and select 1.
29. On Trace1, drag and drop the marker to 8 nsec.
30. Repeat the previous three steps for Trace3.

6.1.3. HS-RX DC Differential Input Impedance

1. Open **TDR/TDT** tab.
2. Select **Trace2**.
3. Open **Parameters** tab.
4. Select the **Topology** (item1) of DUT to Differential.

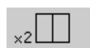


5. Select **Measure** to Time Domain.
6. Select **Format** to Impedance.
7. Set **Rise Time** to 100 ps (20-80%).
8. Click **Tdd11** in the table.
9. Click the box below the left knob under Horizontal.
10. Input 1 nsec/div with the Entry dialog box.
11. Click the box below the right knob under Horizontal.
12. Input -1 nsec with the Entry dialog box.
13. Click the box below the left knob under Vertical.
14. Input 10 Ohm/div with the Entry dialog box

15. Click the box below the right knob under Vertical.
16. Input 50 Ohm with the Entry dialog box.
17. Click **Marker** menu and select 1.
18. On Trace2, drag and drop the marker to 8 nsec.

6.2. Manual Setup for Frequency Domain Measurement

6.2.1. Channel and Trace Settings

1. Press **Display**.
2. Click **Allocate Channels** > .
3. Press **Channel Next**.
4. Click **Num of Traces** > **3**.
5. Click **Allocate Traces** > .

6.2.2. HS-TX/HS-RX Differential Return Loss

1. Press **Trace Next** to select Trace1.
2. Press **Sweep Setup** > **Power** > Set **Power** to -20 dBm.
3. Click **Return**.
4. Set **Points** to 1001.
5. Set **Sweep Type** to **Log Freq**.
6. Press **Start** > Set start value to 300 kHz.
7. Press **Stop** > Set stop value to 4 GHz.
8. Press **Avg** > Set **IF Bandwidth** to 1 kHz.
9. Press **Analysis** > **Fixture Simulator** > **Fixture Simulator** to turn it **ON**.
10. Click **Topology** > **Device** > **Bal**.
11. Click **Port1 (bal)** > **1-2**.
12. Click **Return**.
13. Click **BalUn ON All Traces**.
14. Click **Measurement** > **Sdd11**.

15. Press **Format** > **Log Mag**.
16. Press **Scale**.
17. Set **Scale/Div** to 5 dB/div.
18. Set **Reference position** to 9 Div.

6.2.3. HS-TX/HS-RX Common-Mode Return Loss

1. Press **Trace Next** to select Trace2.
2. Press **Meas** > **Scc11**.
3. Press **Format** > **Log Mag**.
4. Press **Scale**.
5. Set **Scale/Div** to 5 dB/div.
6. Set **Reference position** to 9 Div.

6.2.4. HS-TX/HS-RX Mode Conversion Limits

1. Press **Trace Next** to select Trace3.
2. Press **Meas** > **Sdc11**.
3. Press **Format** > **Log Mag**.
4. Press **Scale**.
5. Set **Scale/Div** to 5 dB/div.
6. Set **Reference position** to 9 Div.

6.3. Limit Test Settings

The E5071C-TDR provides a capability of setting limit lines to perform pass/fail test on each measurement.

6.3.1. Turning On/Off Fail Sign

If this option is turned on, a fail sign appears when one or more measurement items violate the limit lines. It is useful to check overall test result.

1. Press **Analysis** > **Limit Test** > **Fail Sign** to switch the fail sign ON/OFF.

6.3.2. Setting the Warning Beeper

If this option is turned on, a beep is generated when one or more measurement items violate the limit lines.

1. Press **System** > **Misc Setup** > **Beeper** > **Beep Warning** to switch the warning beeper ON/OFF.

6.3.3. Defining the Limit Line

Set limit lines to perform pass/fail tests on the following measurement items.

- HS-TX Differential Return Loss (Trace1 in Channel2)
- HS-TX Common-Mode Return Loss (Trace2 in Channel2)
- HS-TX Mode Conversion Limits(Trace3 in Channel2)
- HS-RX Differential Return Loss (Trace1 in Channel2)
- HS-RX Common-Mode Return Loss (Trace2 in Channel2)
- HS-RX Mode Conversion Limits(Trace3 in Channel2)

Note: If using the VBA, appropriate limit lines are automatically selected for Attenuation and Phase in accordance with the DUT cable type.

1. Press **Channel Next** key and **Trace Next** key to activate the trace on which limit lines should be set.
2. Press **Analysis** > **Limit Test** > **Edit Limit Line** to display the limit table shown below (Initially, no segments are entered in the limit table). Using the limit table, create/edit a segment.

	Type	Begin Stimulus	End Stimulus	Begin Response	End Response
1	MAX	0 s	600 ps	105 U	105 U
2	MIN	0 s	600 ps	75 U	75 U
3					

3. Enter the limit line data following the tables below.
4. Click **Return**.
5. Click **Limit Line** and turn it **ON**.
6. Click **Limit Test** and turn it **ON**.
7. Repeat 1 to 6 for each Measurement items.

Differential Return Loss (HS-TX)

Type	Begin Stimulus	End Stimulus	Begin Response	End Response
Max	$f_{LP,MAX}$	fh	-18 dB	-9 dB
Max	fh	f_{MAX}	-9 dB	-3 dB

Differential Return Loss (HS-RX)

Type	Begin Stimulus	End Stimulus	Begin Response	End Response
Max	0	$F_{LP,MAX}$	-18 dB	-18 dB
Max	$f_{LP,MAX}$	fh	-18 dB	-9 dB
Max	fh	f_{MAX}	-9 dB	-3 dB

$f_{LP,MAX}$: Toggle Frequency for Low Power mode

fh: Maximum HS bit rates / 2

f_{MAX}: 1 / (Minimum Rise and Fall Time (20-80%) * 5)

Common-Mode Return Loss (HS-TX)

Type	Begin Stimulus	End Stimulus	Begin Response	End Response
Max	$f_{LP,MAX}$	f_{MAX}	-6 dB	-6 dB

Common-Mode Return Loss (HS-TX)

Type	Begin Stimulus	End Stimulus	Begin Response	End Response
Max	0	$f_{INT,MIN} / 4$	0 dB	0 dB
Max	$f_{INT,MIN} / 4$	$f_{INT,MIN}$	0 dB	-6 dB
Max	$f_{INT,MIN}$	f_{MAX}	-6 dB	-6 dB

$f_{INT,MIN}$: Minimum RF Frequency

$f_{LP,MAX}$: Toggle Frequency for Low Power mode

f_{MAX}: 1 / (Minimum Rise and Fall Time (20-80%) * 5)

Mode Conversion Limits (HS-TX)

Type	Begin Stimulus	End Stimulus	Begin Response	End Response
Max	0	f_{MAX}	-26 dB	-26 dB

Mode Conversion Limits (HS-RX)

Type	Begin Stimulus	End Stimulus	Begin Response	End Response
Max	0	f_{MAX}	-26 dB	-26 dB

f_{MAX}: 1 / (Minimum Rise and Fall Time (20-80%) * 5)