

Keysight EEsof EDA

W2324 High Capacity Layout Pre-processor Element

Data Sheet

Key Features

The Advanced Design System (ADS) High Capacity Layout Pre-processor Element has the following capabilities when used in a high-speed digital design flow:

- Imports large PCB design files in ODB++ format into a pre-processor GUI
- Allows critical net selection and cookie cutting
- Exports processed segment of PCB to ADS Layout for EM modeling using Momentum and FEM Element
- Supports import of netnames and components

Overview

The High Capacity Layout Pre-processor Element is an ODB++ file format import and pre-processing tool that enables you to select the environment immediately around critical nets in preparation for electromagnetic (EM) modeling. This type of pre-processing is useful in high-speed digital design where the printed circuit board (PCB) is very complex and whose total geometry exceeds the capacity of an EM-based field solver. The solution is to focus in on a handful of critical nets, for example, a differential pair connecting two Serializer/Deserializer (SERDES) integrated circuits (ICs) that are a victim of crosstalk from one or more aggressor traces. An example of such a trace is shown in figure 2. Note that the board has been “cookie cut”, meaning a convex hull with a user-defined margin has been defined, leaving a portion of the board whose complexity is within the capacity constraints of full-accuracy, full-wave EM field solvers such as Momentum and FEM Element.

High Speed Digital Design Flow

A typical high-speed digital workflow including High Capacity Layout Pre-processor Element is shown in figure 1.

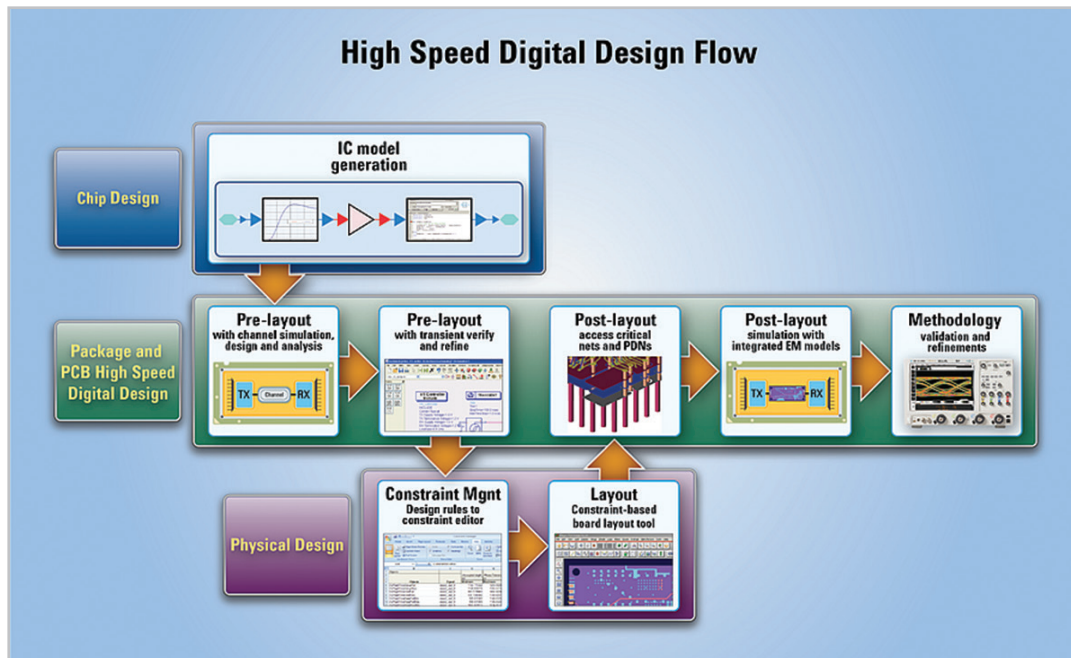


Figure 1
The High Capacity Layout Pre-processor is central to this high-speed digital design flow. The middle bar (green) and lower bar (purple) encloses steps performed by the signal integrity engineer in ADS, and by the physical designer in the third-party enterprise PCB tool, respectively. The task in the upper (blue) bar is performed by the chip designer.



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