Keysight Technologies
x1149 Boundary Scan Analyzer
Data Sheet

KEYSIGHT TECHNOLOGIES

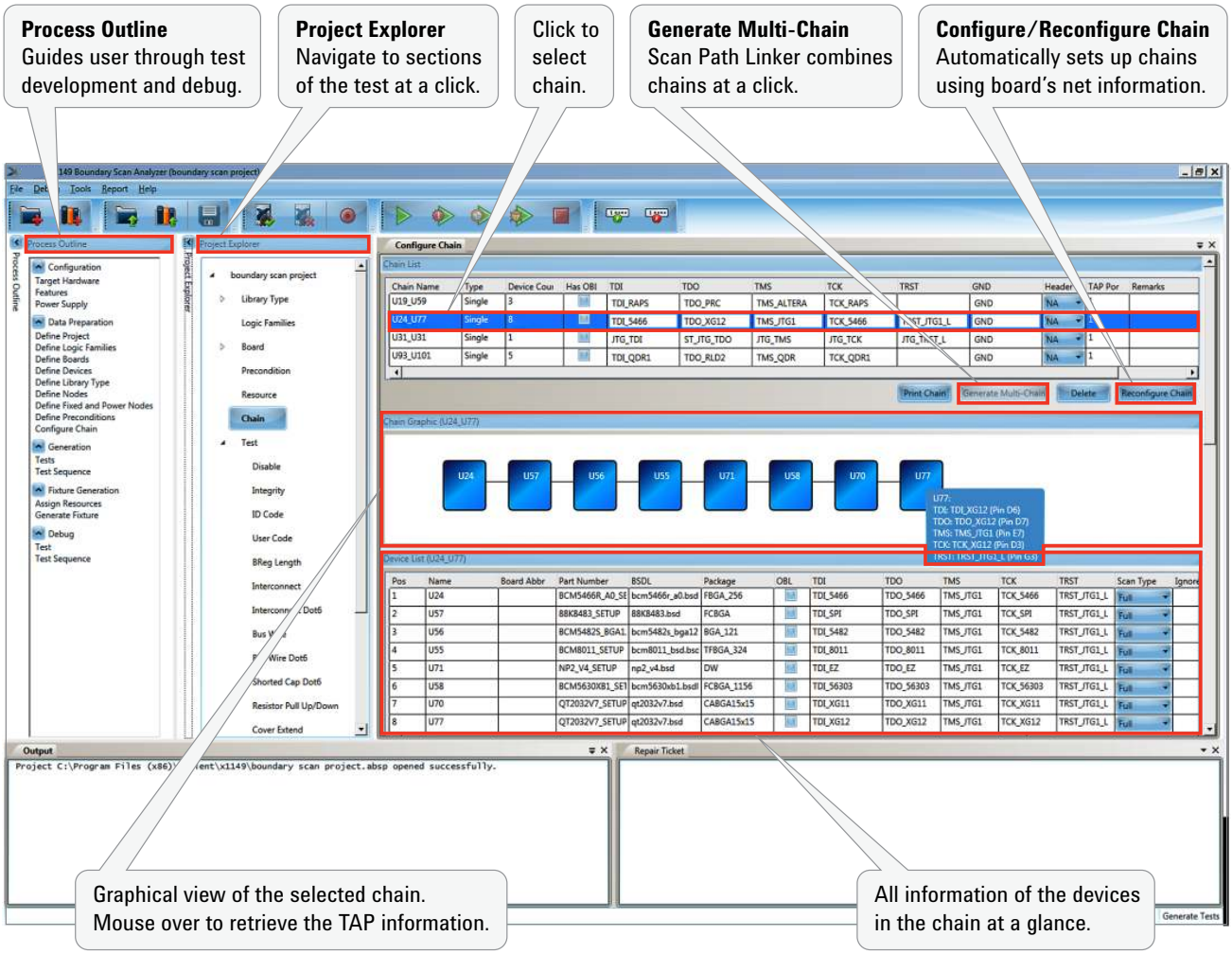
Overview

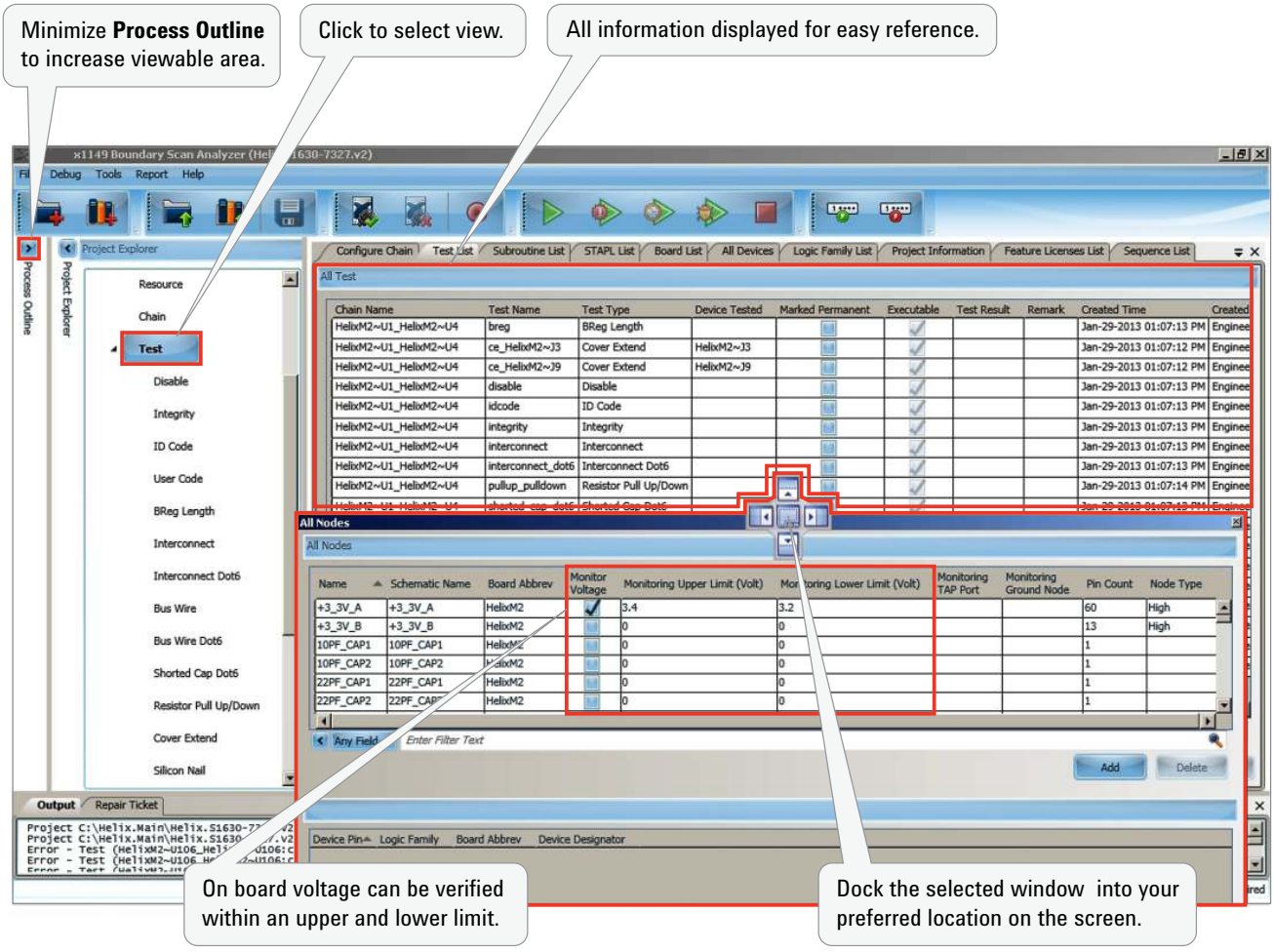
Product description

The Keysight Technologies, Inc. x1149 boundary scan analyzer is a printed circuit board tester in compliance with the IEEE 1149.1 Standard test access port (TAP) and boundary scan architecture. The Keysight x1149 offers an easy to use software interface for development, debug and production runtime.

Industries and Applications

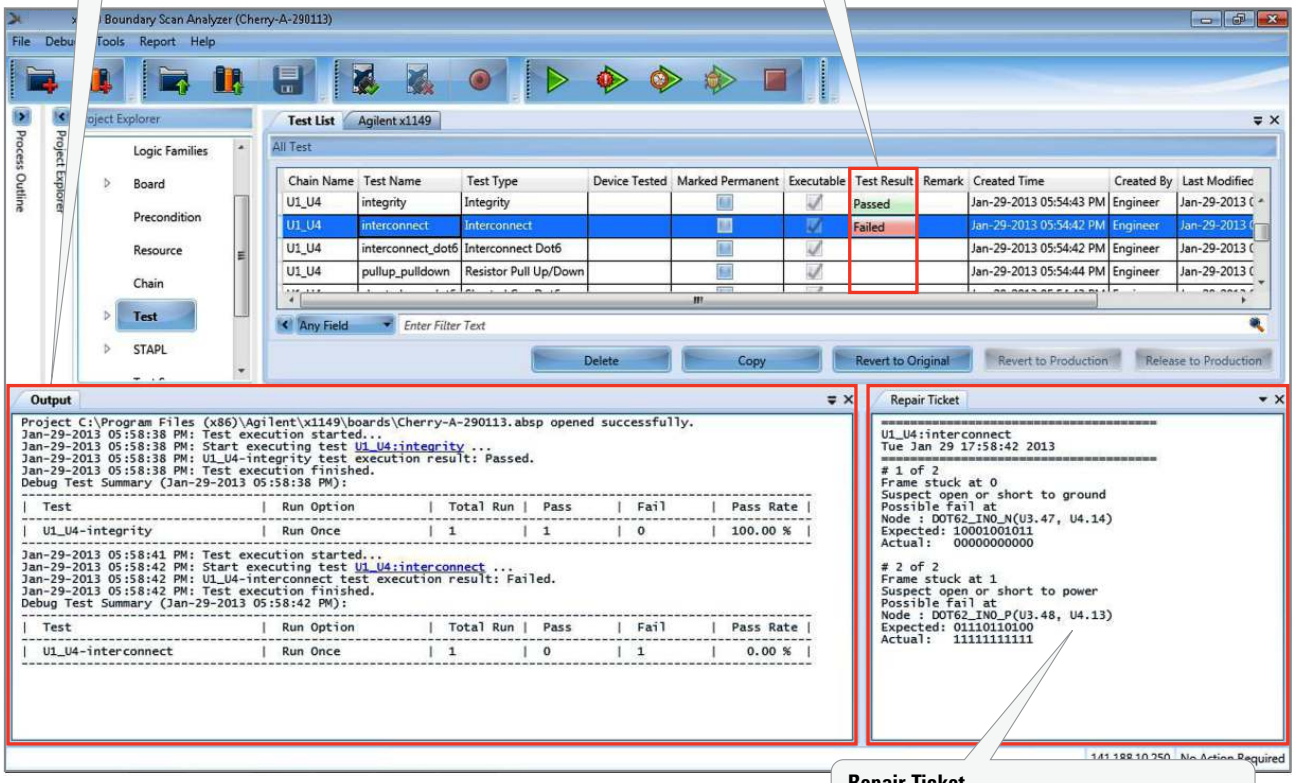
- Computational and server board test
- Network communication board test
- Aerospace and defense
- Automotive electronics test
- Industrial electronics test
- Medical device test




Minimize **Process Outline** to increase viewable area.
Click to select view.
All information displayed for easy reference.
On board voltage can be verified within an upper and lower limit.
Dock the selected window into your preferred location on the screen.

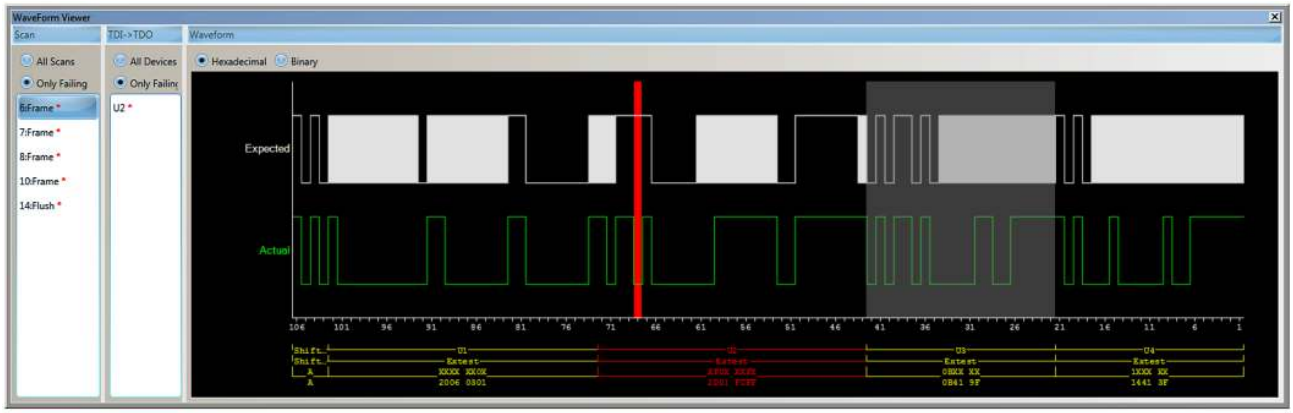
Output
Shows the results of all the tests for the chain(s).

Results of tests are highlighted in colors.
Test results can be sorted by clicking on the title tab.



Repair Ticket
Pin-level failure reporting and possible cause.

Choice of Waveform Viewer or Frame Debugger views to debug the test.



Frame Debugger

All Cells | Only Frame Cells | Only Failing Cells

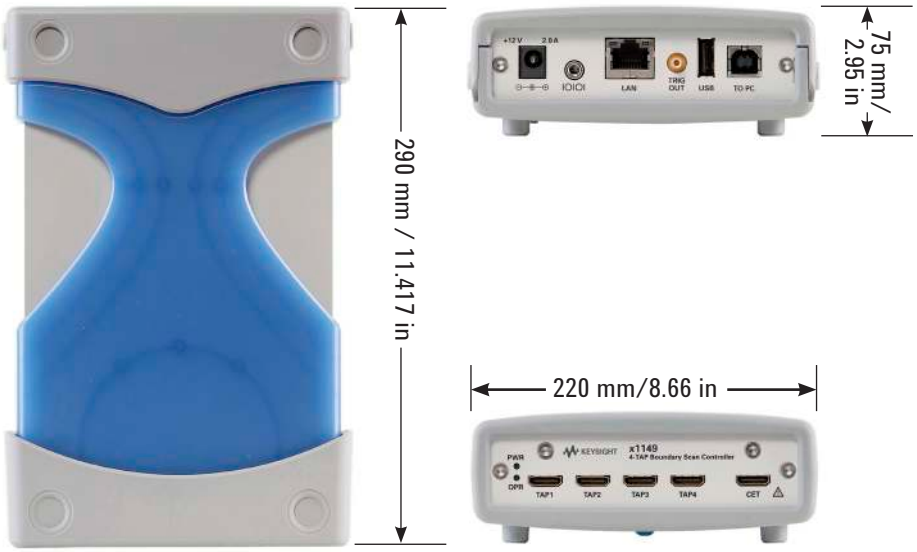
Chain Cell	Frame Cell?	Device Cell	Cell Type	Device	Pin	Node	Signature Type	Expected/Actual
67	✓	25	Receiver	U2	2	DOT11_RO3	Normal	LLHHHHHLLLL
68	✓	26	Receiver	U2	62	DOT11_RO2	Normal	LLHHHLHLLLH 00000000000
69	✓	27	Receiver	U2	60	DOT11_RO1	Normal	LLHHLHHLHLL
70	✓	28	Receiver	U2	58	DOT11_RO0	Normal	LLHHLLHLHLH
74	✓	2	Driver_Receiver	U1	27	NC_U1_27	Normal	10001011001
74	✓	2	Driver_Receiver	U1	26	NC_U8_26	Negative	01110100110
74	✓	2	Driver_Receiver	U1	27	NC_U1_27	Self-Monitor	HLLLHLHHLLH
75	✓	3	Driver_Receiver	U1	31	NC_U1_31	Normal	10001111000
75	✓	3	Driver_Receiver	U1	30	NC_U8_30	Negative	01110000111
75	✓	3	Driver_Receiver	U1	31	NC_U1_31	Self-Monitor	HLLLHHHHLLL
76	✓	4	Driver_Receiver	U1	35	NC_U1_35	Normal	10010010101
76	✓	4	Driver_Receiver	U1	34	NC_U8_34	Negative	01101101010
76	✓	4	Driver_Receiver	U1	35	NC_U1_35	Self-Monitor	HLLHLLHLHLH
77	✓	5	Driver_Receiver	U1	37	NC_U8_37	Normal	11001111000

Any Field | Enter Filter Text

Product characteristics and general specifications

Controller interface	Ethernet 10/100 MB
	High speed USB 2.0 (For firmware upgrade only)
Power requirement	+12 VDC (typical)
	2 A (maximum) input rated current
	Installation category II
Power consumption	+12 VDC, 260 mA (maximum)
Standard shipped accessories	AC/DC power adapter
	Power cord
	USB cable
	HDMI cable
	Diagnostic clip
	Keysight x1149 boundary scan analyzer 'Quick Start Guide'
	Keysight x1149 software release CD-ROM
	Certificate of calibration
	* Compatible with Microsoft ® Windows ® operating systems only.
Operating environment	Operating temperature from 0 °C to +55 °C
	Relative humidity at 15% to 85% at 40 °C (non-condensing)
	For indoor use only
Storage compliance	–20 °C to 70 °C
Safety compliance	CE ICES/NMB-001 ISM GRP.1 CLASS A 40 C N10149

Dimensions



Boundary Scan Controller dimension (width × depth × height)	290 mm x 220 mm x 75 mm / 11.417 in x 8.66 in x 2.95 in
Weight	550 g

TAP/IO port dimension (width × depth × height)	120.3 mm x 44.5 mm x 21 mm / 4.72 in x 1.75 in x 0.826 in
Weight	80 g
Warranty	One year plus 2nd year extended warranty.
Software update subscription	One year plus 2nd year extended subscription.

General specifications

Parameter/Specification **Driver/receiver resources**	
Types	GPIO, JTAG TAP
GPIO (General Purpose Input/Output)	5 output/driver pins programmable voltage and share with the common (VREF) Voltage Reference
	4 input/receiver pins with fully programmable receiver voltage.
JTAG Test Access Port (TAP)	Supports up to 4 TAP each with TCK,TDI,TDO,TMS with optional TRST signals as defined by IEEE Std 1149.1
	TDI, TMS, TRST programmable voltage reference share common VREF with the GP-output pins
	TDO programmable voltage receiver
	TCK has a separate programmable voltage reference (VREF) and slew rate.
Cover-Extend Technology (CET)	
Vectorless Enhanced (VTEP)	CET ARM, CET Rx/Tx, VTEP CLK/A/B/Hi/Lo+12 VDC Power
Ground pins	
Fixed location grounds per TAP module	TAP Module pins 1,3,5,7

Hardware GPIO (General Purpose Input/Output) specifications

Parameter/Specification **GPIO Specifications**	
Resources	5 drivers & 4 receivers with GND pins shared with TAP Pins
Sample/update rate READ, WRITE, READ/WRITE maximum sample/update rate	10 KHz / 100 usec
Per-pin settable features	OUT: data value (0,1, or Z)
	"0" – ≤ 100 mV
	"1" – ≥ VREF-100 mV
	"Z" – High Z
	IN: VREF (1.1~5.0 V)
General Purpose Input or Receiver	
IN/Receiver	Read digital data "0" or "1", according to VREF and threshold voltage. It can be used to measure the external voltage range from 0 V to 5 V
Reference channel group	+5 V to 0 V in 100 mV steps
Timing	De-skewed. No programmable edges
Termination	> 1 MΩ
Error Detection:	Windowing (two point receive reference), over-voltage, under-voltage, drive-check validation (receiver used to verify driver achieved drive state)
General Purpose Output or Driver	
Update rate(maximum)	10 KHz/100 µs
Output voltage [3]	Range: +5.0 V to +1.1 V, step resolution of 100 mV, static accuracy
Driver current [2]	10 mA @ 5 V
	2 mA @ 2.5 V
Continuous output current into a short [3]	50 mA at 5 V
	20 mA at 2.5 V
Rise/Fall time [4]	< 20 ns @ 2.5 V
	< 50 ns @ 1.1 V
Tri-state leakage current (maximum range [5])	–65 µA,+5 µ
Tri-state capacitance (maximum):	Maximum 0.7 nF
	Typical 0.45 nF
Disconnected capacitance	15 pF
Output skew (same board)	Typical < 5 ns
DC output resistance (typical)	35 - 50 Ω

Hardware JTAG TAP specifications

Parameter/Specification	Test Method
JTAG TAP Specifications	
Resources	TDI, TDO, TCK, TMS, TRST and a GND pair for each 4 TAP port
Clock maximum frequency	22.5 Mhz
Per-pin settable features	Data value (0,1, or Z), driver/receive reference; slew rate; termination high-impedance or 50 Ω
Timing	De-skewed. Programmable edges (TCK only)
JTAG TAP Receiver TDO	
Clock maximum frequency	11.25 Mhz
Reference voltage (thresholds)	High: +5 V
	Low: 0 V to 0.5 V
	Step resolution of 100 mV
	Static accuracy
Input voltage range	0 V to 5 V
Input resistance	> 40 KΩ
Pull-up terminations	100k Ω
JTAP TAP Driver TDI, TMS, TRST	
Clock maximum frequency	TDI – 11.25 MHz
	TMS – 7.5 MHz
	TRST – 10 KHz
Output voltage	+5 V to +1.1 V [2]
Driver current [3]	±10 mA @ 5 V
	±2 mA @ 2.5 V
Continuous output current into a short [3]	≥ 50 mA at 5 V
	> = 20 mA at 2.5 V
Rise/Fall time [3]	< 20 ns @ 2.5 V
	< 10 nS @ 1.1 V
Tri-state leakage current (maximum [5])	±65 µA
Tri-state capacitance (maximum)	1 nF
Output skew (TMS and TRST on all TAPs) (same board)	Typical ± 5 ns
DC output resistance (typical)	35 Ω, 50 Ω

Hardware JTAG TAP specifications (continued)

Parameter/Specification	
JTAP TAP Driver TCK	
Clock maximum frequency	22.5 Mhz
Output Voltage [2]	0 to 5 volts with 100 mV resolution)
Driver current [3]	10 mA @ 5 V
	2 mA @ 2.5 V
Continuous output current [3]	≥ 80 mA @ 5 V
	≤ 40 mA at 2.5 V
Slew rate: (see note 6)	40 V/µsec to 380 V/µsec
Tri-state leakage current (maximum [5])	–3.7 µA
Tri-state capacitance (maximum)	1.1 nF
Disconnected capacitance	15 pF
DC output resistance (typical)	50 Ω

Notes

1. There are 4 GND pins per TAP module, which are common for both GPIO and TAP signals in the same TAP 20-pin connector. However, the GND pins in different TAP modules are isolated.
2. Vref can be configured from 1.1 V to 5.0 V with a step of 0.1 V, which is common to all GPO and TMS/TDI/TRST signals. Vref clk can be separately configured in some situations where the high voltage of TCK needs to be a little higher than the other TAP signals. The logic output high is set to a voltage range from (Vref - 0.2V) to Vref, while the logic low is less than 0.2 V when output current is not more than 0.1 mA.
3. Capable to produce an output current of 10 mA when Vref = 5 V, or 2 mA when Vref = 2.5 V; load 100 Ω for the drive current test. The maximum current is tested when the output pin shorts to GND.
4. Rise time refers to the period when a signal rises from 0.1 Vref to 0.9V ref; fall time is the period when a signal falls from 0.9 Vref to 0.1 Vref.
5. Set the output at high-Z state and connect the pin to GND to measure the positive leakage current; connect the pin to a maximum voltage of power reference value (Vref) for negative leakage current measurement.
6. The TCK reference voltage is set to 5 V. When the voltage for slew rate configuration is set to 0.2 V, the reading of TCK slew rate is ≤ 30 V/uS; while this voltage is set 5 V, the reading is ≥ 400 V/uS.
7. The threshold voltage of TDO is normally set between 0.5 V and 3.5 V. The logic reading from TDO would be '1' if the input voltage ≥ (0.1 V + threshold voltage), and '0' if the input ≤ (threshold voltage – 0.1 V).

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