SERVICE MANUAL

Multiple Input Electronic Load Mainframes Agilent 6050A and 6051A

Part No. 06050-90003

Service Manual For instruments with Serial Numbers:

Agilent 6050A US37140101 and Above Agilent 6051A US37140101 and Above

For instruments with higher Serial Numbers, a change page may be included.

For instruments with lower Serial Numbers, refer to Appendix A.

Microfiche Part No. 06050-90004

Edition 1 Printed: November, 1989 Edition 2 Printed: January, 1992 Edition 3 Printed: November, 1999

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SAFETY SUMMARY

The following general safety precautions must be observed during all phases of operation, service and repair of this instrument. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of the instrument. Agilent Technologies assumes no liability for the customer's failure to comply with these requirements.

BEFORE APPLYING POWER.

Verify that the instrument is set to match the available line voltage.

GROUND THE INSTRUMENT.

This product is a Safety Class 1 instrument (provided with a protective earth terminal). To minimize shock hazard, the instrument chassis and cabinet must be connected to an electrical ground. The instrument must be connected to the ac power supply mains through a three-conductor power cable, with the third wire firmly connected to an electrical ground (safety ground) at the power outlet. Any interruption of the protective (grounding) conductor or disconnection of the protective earth terminal will cause a potential shock hazard that could result in personal injury. If the instrument is to be energized via an external autotransformer for voltage reduction, be certain that the autotransformer common terminal is connected to the neutral (earth pole) of the ac power lines (supply mains). This instrument is equipped with a line filter to reduce electromagnetic interference (EMI), and must be connected to a properly grounded receptacle to minimize EMI.

FUSES.

Fuses are contained inside the unit, and are not user-replaceable. Only trained service personnel should replace blown fuses, and only after identifying and correcting the problem which caused the fuse(s) to blow.

DO NOT OPERATE IN AN EXPLOSIVE ATMOSPHERE.

Do not operate the instrument in the presence of flammable gases or fumes.

KEEP AWAY FROM LIVE CIRCUITS.

Operating personnel must not remove instrument covers. Component replacement and internal adjustments must be made by qualified service personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power, discharge circuits and remove external voltage sources before touching components.

DO NOT SERVICE OR ADJUST ALONE.

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

DO NOT EXCEED INPUT RATINGS.

Operation at line voltages or frequencies in excess of those stated on the data plate may cause leakage currents in excess of 3.5 mA peak.

SAFETY SYMBOLS.



Instruction manual symbol: the product will be marked with this symbol when it is necessary for the user to refer to the instruction manual (refer to Table of Contents).



Indicates hazardous voltages.



Indicate earth (ground) terminal.



The WARNING sign denotes a hazard. It calls attention to a procedure, practice, or the like, which, if not correctly performed or adhered to, could result in personal injury. Do not proceed beyond a WARNING sign until the indicated conditions are fully understood and met.



The CAUTION sign denotes a hazard. It calls attention to an operating procedure, or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product. Do not proceed beyond a CAUTION sign until the indicated conditions are fully understood and met.

DO NOT CIRCUMVENT SAFETY DEVICES.

AC mains power exists on exposed terminals in various locations in the mainframe and on the load modules. To protect the user against the danger of electric shock, the unit is equipped with a safety interlock that removes as mains power when the top cover is removed. Do not attempt to defeat the function of the safety interlock.

DO NOT SUBSTITUTE PARTS OR MODIFY INSTRUMENT.

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification to the instrument. Return the instrument to an Agilent Technologies Sales and Service Office for service and repair to ensure that safety features are maintained.

Instruments which appear damaged or defective should be made inoperative and secured against unintended operation until they can be repaired by qualified service personnel.

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Introduction

Scope

This manual contains information for troubleshooting and repairing the Electronic Load mainframe and modules to the component level. Replaceable-parts lists and circuit diagrams for the mainframe are also provided. Verification procedures are included to aid in determining the performance level either before or after repair. Calibration procedures and specifications for the Electronic Load are included in the Operating Manual. Replaceable-parts lists, circuit diagrams, and verification procedures for the load modules are given in the individual module service manuals, which should be used with this manual

Related Documents

The following documents are also related to this manual:

- Agilent 6050A and 6051A Operating Manual Part No. 06050-90001 Provides specifications, local and remote operation, calibration procedures.
- Electronic Load Family Programming Reference Guide Part No. 06060 90005 Describes HPSL programming commands, status reporting.

Firmware Revisions

Some information in this manual, and SA (signature analysis) information in particular, is associated with specific versions of the Electronic Load firmware. Each Electronic Load returns the revision number of its primary interface firmware in response to the "*IDN?" query. Both primary and secondary interface ROMs have a label that also specifies the firmware revision. See "Signature Analysis" in Chapter 3.

Manual Revisions

Agilent Technologies instruments are identified by a two-part, ten-character serial number, such as 2931A-00101. The first five characters (e.g. 2931A) are the serial prefix, which is the same for all identically made instruments. The last five digits (e.g. 00101) are a unique serial number assigned to each instrument. If a significant design change is made, the prefix changes but the last five numbers continue in sequence.

This manual was written for Electronic Load mainframes with the same serial prefix and with serial numbers equal to or lower than the one shown on the title page. If the prefix number on your Electronic Load mainframe is higher than the one on the title page, then the Electronic Load mainframe was made after publication of the manual and may have hardware and/or firmware differences not covered in the manual. If there are such differences, they are documented in one or more "Manual Changes" sheets sent with the manual. If the prefix of your Electronic Load mainframe is below that listed on the title page, then your Electronic Load mainframe was made prior to those covered in this manual. Refer to Appendix A for any backdating information that may be required.

Safety Considerations

The Electronic Load is a Safety Class 1 instrument that has a protective earth terminal. Refer to the Safety Summary page at the beginning of this manual for general safety procedures and the meaning of safety symbols appearing in the manual and on the Electronic Load.

Disassembly Procedures

Introduction

The following procedures will make it easier for you to disassemble major components on the Electronic Load mainframes and Modules. Refer to Figure 5-1 and Table 5-5 for the location of the mainframe mechanical components.

Before proceeding with any disassembly, disconnect the ac power cord and remove the top cover. Then proceed to the applicable procedure.

Fans

6060A Mainframe

- Remove all modules from the unit.
- Remove the side covers from the unit.
- Remove the six screws securing the fan shroud and remove the shroud.
- The fans are accessible when the shroud is removed.
- Disconnect the fan cable from the applicable fan.
- When reassembling the fans, make sure the fan label faces the back of the unit. When replacing the fan shroud, make sure ALL the tabs are inserted in the holes in the bottom of the chassis before tightening the screws.

606lA Mainframe

- Remove the front panel (see Front Panel).
- Remove the left side cover from the unit.
- Disconnect the fan cable.
- Remove the two screws securing the fan and remove the fan.
- When reassembling the fan, make sure the fan label faces the back of the unit.

Front Panel

- Remove the left side cover from the unit.
- Remove the trim strip from the top of the front panel frame.
- Disconnect the keypad/display cable from J203/J202 and the power cable from J209 on the GPIB board. (see Chapter 3).
- Remove the two top screws as well as the two outside bottom screws that secure the front panel to the front panel frame and remove the front panel.

GPIB Board

CAUTION

This assembly contains static sensitive components. Observe all standard electrostatic procedures when removing or replacing the GPIB board (see Chapter 3).

- Remove the modules from the two slots closest to the GPIB board.
- Remove the left side cover from the unit.
- Disconnect the keypad/display cable from J203/J202. the power cable from J209, the transformer cable from J206/J207, and the fan cable from J205.
- Remove the Hex standoffs on the GPIB connector on the rear panel.
- Remove the screw that secures the ground wire to the chassis.
- Remove all the screws that secure the shield to the GPIB board and the fan shroud.
- Remove the shield.
- Turn the ends of the two plastic GPIB board standoffs 1/4 turn to loosen them and remove the GPIB board.

Note:

On the 6051A you must also remove the screw that secures the switch bracket on the GPIB board to the chassis.

• When reinstalling the GPIB board, lift up the safety interlock bracket on the side panel so that the switch on the GPIB board is correctly positioned under the bracket when the board is installed.

Keypad

- Remove the front panel (see Front Panel).
- Remove the nuts securing the keypad to the front panel and remove the keypad pc board.
- The keypad and keypad spacer come out when the pc board is removed.

CAUTION

Remove the cable from the keypad only if replacing the keypad or cable. The cable connector located on the back of the keypad is not designed for routine disconnection. If the cable must be disconnected carefully pull the connector straight out. To avoid breaking the pins DO NOT rock the connector back and forth.

- When reinstalling the cable, be sure to line up the cable stripe over the hole marked with a square. Also, make sure the pins are all properly aligned before reinstalling the connector.
- When reinstalling the keypad, remember to install the spacer between the keypad and the front panel.

LCD Display and Window

- Remove the front panel (see Front Panel).
- Remove the two nuts securing the LCD display to the front panel and remove the LCD display.
- The display window comes out when the display is removed.

CAUTION

Remove the cable from the display only if replacing the display or cable. The cable connector located on the back of the display is not designed for routine disconnection. If the cable must be disconnected carefully pull the connector straight out. To avoid breaking the pins DO NOT rock the connector back and forth.

• When reinstalling the cable, be sure to line up the cable stripe over the hole marked with a square. Also, make sure the pins are all properly aligned before reinstalling the connector.

Line Switch

- Remove the front panel (see Front Panel).
- Record the color code and location of each wire connected to the switch.
- Disconnect the wires from switch terminals.
- Release the locking tabs by pressing them inward against the body of the switch and remove the switch.

Modules

CAUTION

The module assemblies contain static sensitive components. Observe all standard electrostatic procedures when disassembling the modules (see Chapter 3).

- Disconnect all wires connected to the back of the module.
- Disconnect all ribbon cables connected to the top of the modules.
- Loosen the 1/4-turn fastener at the front and the thumbscrew at the rear of the module. Remove the module by grasping it with the 1/4 turn fastener and the thumbscrew.
- Place the module on the workbench chassis-side down.
- Rotate and remove the plastic fasteners under the module.
- Remove the two screws that secure the rear panel to the module's chassis.
- Remove the two screws near the ribbon cables that secure the power board to the module's chassis.

Note:

The Agilent 60504B/07B have two additional screws at the bottom of the power board that secure the power board to the chassis. Remove these also.

• Grasp the power board by the binding posts and the end opposite the binding posts. Slide the board slightly in the direction of the binding posts to clear the input connector and carefully lift up on the assembly. The control board and power board assemblies will now come apart.

Note:

On the Agilent 60504B/07B you must disconnect the ribbon cable that connects the two boards before you can completely separate the power board and control board assemblies. You must also remove the control board from the chassis before you can reconnect the control board to the ribbon cable for troubleshooting.

• When reassembling the module, do not fully tighten the screws until after all components are assembled.

Power Transistors (located on modules)

The power transistors on each module are comprised of subassemblies containing four transistors each. If any one of the four transistors fail, *the entire subassembly must be replaced* .

- Disassemble the module (see Module).
- Remove the three screws that secure the defective subassembly to the heatsink.

Note:

On the Agilent 60504B/07B modules you must first disassemble the heatsink before you can access the defective subassembly. First remove the three screws that secure the heatsink spacer to the heatsink. Then completely loosen the ten screws that secure the heatsink to the T-bar. Separate the heatsink from the T-bar taking care that the heatsink screws don't fall out of the holes. This makes it easier to reassemble the heatsink.

- Cut all the transistor leads on the defective subassembly close to the transistor bodies and remove the subassembly.
- Unsolder the cut transistor leads from the power board and clean the corresponding mounting holes.
- When replacing the subassembly, be sure to apply heat-conducting grease or a new thermal pad to the back of the subassembly before reinstalling the heatsink.

CAUTION

Do not use any heatsink compound using silicone which can migrate and foul electrical contacts elsewhere in the system. An organic zinc oxide cream such as American Oil and Supply Company Heatsink Compound is recommended.

Transformer (on mainframe)

- Remove the front panel (see Front Panel).
- Record the color code and location of each wire connected to the transformer.
- Disconnect the wires from the transformer.
- Use a short #2 Pozidrive screwdriver to remove the two screws securing the transformer, and remove the transformer from the unit.

Troubleshooting

WARNING

Most of the procedures described here are performed with power applied and protective covers removed. These procedures should be done only by trained service personnel who are aware of the hazards involved such as electrical shock or fire. Where procedures can be done with power turned off, disconnect the ac line cord from the instrument.

Please read the entire procedure and be sure you understand each step before you begin.

Introduction

This chapter provides troubleshooting and repair information for the Electronic Load mainframe and modules. Before attempting to troubleshoot the Electronic Load, ensure that the problem is with the load itself and not with an associated circuit, power source, or power line. The verification tests in each module service manual enable this to be determined without removing the covers from the Electronic Load.

Overall troubleshooting procedures are provided to isolate a problem to a functional area of circuitry. Once a problem has been isolated to a functional area, additional troubleshooting procedures are given to isolate the problem to the defective component(s).

If a component is found to be defective, replace it and then conduct the verification tests given in each module service manual Chapter 2. Note that when certain components are replaced, the load must be recalibrated (see "Post Repair Calibration" later in this chapter). If the serial EEPROM chip U211 is replaced, the Electronic Load must be initialized before it is recalibrated. See "EEPROM Initialization" later in this chapter.

Chapter 5 in this manual lists all of the replaceable parts for the Electronic Load mainframe.

Test Equipment Required

Table 3-1 lists the test equipment required to troubleshoot the Electronic Load. Recommended models are listed.

Electrostatic Discharge (ESD) Protection

The following practices should be followed when working on the Electronic Load.



Do not underestimate the potential for damage from electrostatic discharge (ESD). Generally an electrostatic discharge must be at least 3500 volts for you to feel it, at least 4500 volts for you to hear it. Obviously charges of less than 3500 volts can be expected to do significant damage to many types of electronic components even though you will be unaware of the discharge when you touch the component or assembly and complete failure may not occur.

Table 3-1 Test Equipment Required for Troubleshooting

Туре	Purpose	Recommend Model
GPIB Controller	Communicate with the load via the GPIB	HP9825, Series 85, Series 200/300
Signature Analyzer	Test most of the primary and secondary circuits	Agilent 5005A/B
Digital Voltmeter	Check various voltage levels	Agilent 3456A
Power Source	Provide required input, bias GPIB Board	Agilent 6032A
Logic Probe	Check data bus lines	Agilent 545A
Oscilloscope	Check waveforms and signal levels	Agilent 1741A
Clip Leads	Connect IC pins together	AP Products Model LTC
1	1	I .

- Work only at static-free workstations. These workstations should include special conductive work surfaces (such as a table mat, part number 9300-0797) grounded through a one-megohm resistor. Note that metal table tops and highly conductive carbon-impregnated plastic surfaces are too conductive; they can act as large capacitors and shunt charges too quickly. The work surface should have distributed resistance of between 10⁶ and 10¹² ohms per square.
- While working with equipment on which no point exceeds 500 volts, use a conductive wrist strap in contact with skin. The wrist strap should be connected to ground through a one-megohm resistor. A wrist strap with insulated cord and built-in resistor is recommended, such as 3M Co. number 1066 (part numbers 9300-0969 [small] and 9300-0970 [large]).
- Ground all conductive equipment or devices that may come in contact with static-sensitive components or assemblies
 containing them.
- All grounding (device being repaired, test equipment, soldering iron, work surface, wrist strap, etc) should be done to a single, common ground.
- Where direct grounding of objects in the work area is impractical, a static neutralizer should be used (ionized-air blower directed at work). Note that this method is considerably less effective than direct grounding and provides less protection for static-sensitive devices.
- Always store or transport static-sensitive devices (all semiconductors and thin-film devices) in conductive material. Attach warning labels to the container or bag enclosing the device.
- Always turn power off before removing or installing printed-circuit boards.
- Low-impedance test equipment (signal generators, logic pulsers, etc) should be connected to static-sensitive inputs only
 while the components are powered.
- Use a metalized solder-removing tool (solder sucker) such as part number 8690-0227.
- Use a mildly activated rosin core solder (such as Alpha Metal Reliacore number 1, part number 8090-0098) for repair. The flux residue of this type of solder can be left on the printed-circuit board. Generally, it is safer not to clean the board after repair. Do not use Freon or other types of spray cleaners. If necessary, the board can brushed using a natural-bristle brush only. Do not use nylon-bristle or other synthetic-bristle brushes. Do not use high-velocity air blowers (unless ionized).

- Keep the work area free of non-conductive objects such as Styrofoam-type cups, polystyrene foam polyethylene bags, and plastic wrappers. Non-conductive devices that are necessary in the area can be kept from building up a static charge by spraying them with an anti-static chemical such as part number 92176S.
- Do not wear nylon clothing. Keep clothing of any kind from coming within 12 inches (0,3 m) of static-sensitive devices.
- Do not allow long hair to come in contact with static-sensitive assemblies.
- Do not exceed the maximum rated voltages specified for the device.

Overall Troubleshooting Procedures

WARNING

To avoid the possibility of personal injury remove the instrument from operation before attempting any service procedures. Turn off ac power and disconnect all wires from the mainframe and modules including input leads sense leads GPIB cable and the ac line cord. Make connections to the instrument only as required for a specific procedure.

AC mains voltage is present on exposed pins on the top edge of the mainframe GPIB Board and each module whenever the unit is turned on.

Overall troubleshooting procedures for the Electronic Load are given in the flowchart of Figure 3-1. The procedures first ensure that an ac input failure or bias supply failure are not causing the problem and that the load passes the turn-on selftest (no error messages). The normal turn-on selftest indications are described in Chapter 3 of the Operating Manual.

If the load passes selftest, Figure 3-1 directs you to perform the front panel verification procedures to determine if any load function(s) are not calibrated or are not operating properly. If the load passes the front panel verification tests, Figure 3-1 checks to see if the load can be programmed from an GPIB controller. If the load fails any of the tests, you are directed to the applicable troubleshooting procedure. Signature analysis (SA) is used to troubleshoot the load's primary and secondary microprocessor circuits. The SA mode is also used to generate waveforms which are used to troubleshoot the analog circuits. In addition, a list of test points with signal measurement information is provided to help you troubleshoot.

Selftest Sequence and Error Messages

The turn-on selftest sequence consists of tests on both the primary and secondary circuits. The word 'primary' refers to either the primary interface or primary processor. Any Agilent 6050A/6051A mainframe failure is a primary failure and troubleshooting procedures should begin with the GPIB board. The words "secondary" or "channel" refers to the secondary processor and analog circuits found in the modules. For all secondary or channel failures, troubleshooting procedures should begin with the module. All hardware errors are secondary errors.

Note:

The initial failure symptom is based on visual observation. At power-on, LOOK at the Agilent 6050A/6051A front panel LCD for an error number or message. Since it is possible to miss seeing an error at power up, simply repeat the test by turning power off then on again.

If the load fails the selftest, the input will remain disabled and the display should indicate the type of failure. Table 3-2 lists all of the selftest error codes that can appear on the front panel display and provides the appropriate troubleshooting information.

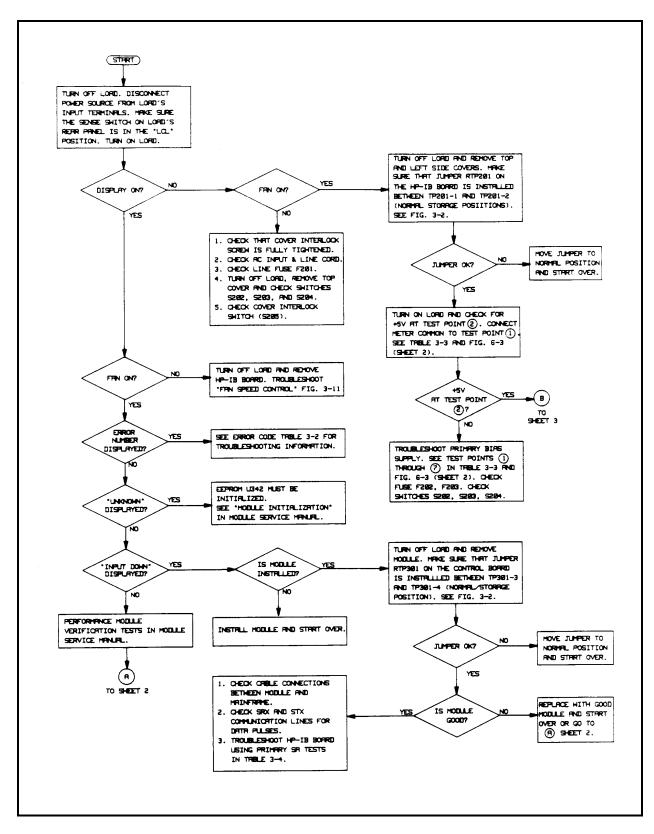


Figure 3-1. Overall Troubleshooting Flowchart (Sheet 1 of 3)

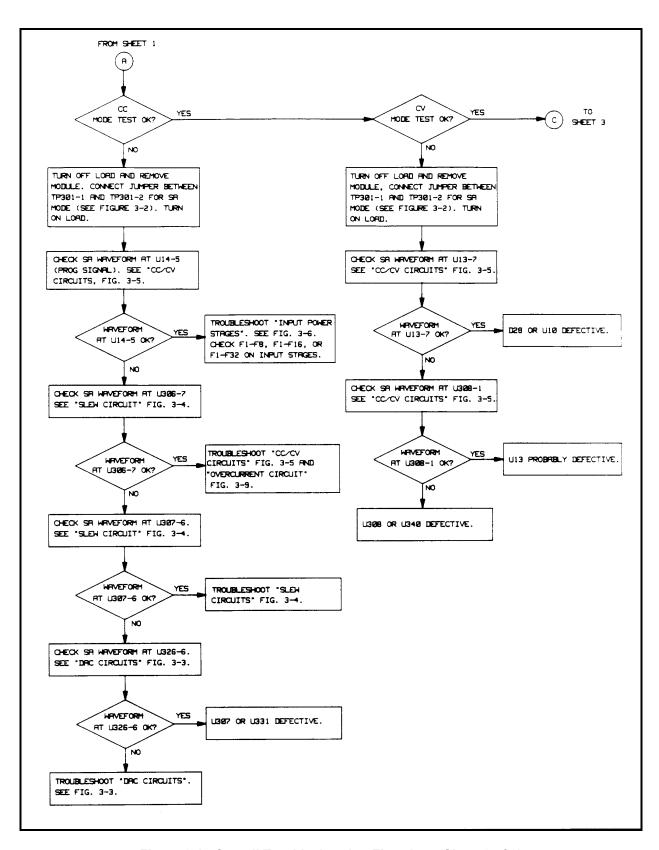


Figure 3-1. Overall Troubleshooting Flowchart (Sheet 2 of 3)

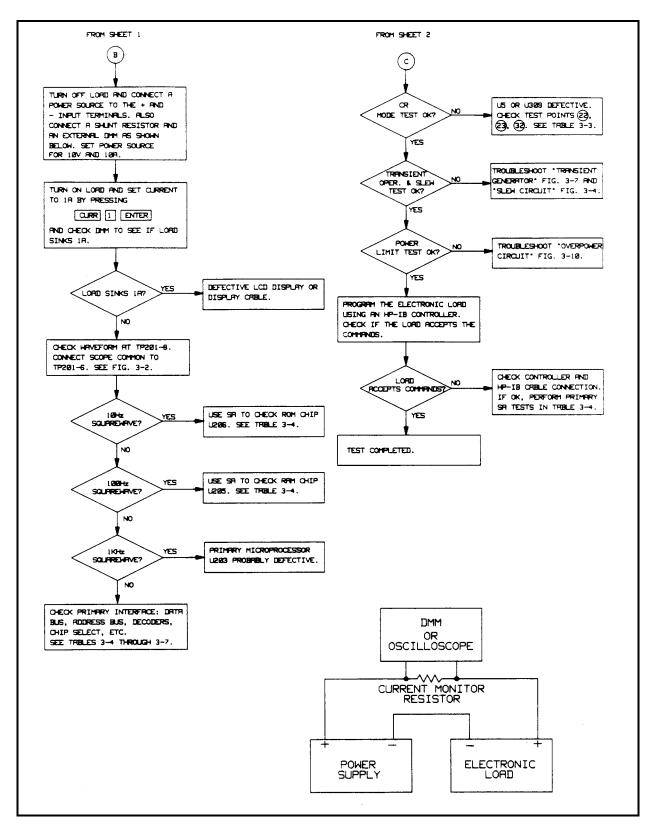


Figure 3-1. Overall Troubleshooting Flowchart (Sheet 3 of 3)

Primary Circuits

The turn-on selftest sequence of the primary microprocessor consists of two parts:

1. The selftest is performed by the primary microprocessor (U203) and starts when the primary clear (PCLR) signal goes false (High). First, the RAM, ROM, and the microprocessor's internal timer selftests are performed. If any of these tests fail, the front panel display will probably remain blank. The failure can be detected by measuring a square wave on the SA GATE line at TP201-8 (see Figure 3-2). The type of failure is indicated as follows:

10Hz square wave--indicates a RAM failure 100Hz square wave--indicates a ROM failure 1KHz square wave--indicates a internal timer failure

Square waves will not have a 50% duty cycle. It is also possible for a selftest failure to "lock-up" the microprocessor and cause a blank front panel display and no error square wave to appear on the SA_GATE line. If "lock-up" occurs, try to isolate the problem by performing the Primary Signature Analysis Tests or by replacing U203.

2. If part 1 passes selftest, the test continues and checks the read/write cycles and the internal trigger circuit. If these tests pass, the primary interface tests are performed. If any test fails, the front panel displays "ERROR x" for two seconds (see Table 3-2), then normal voltage/current will be displayed and the **Err** annunciator will turn on. Depressing the [Error] key will cause "ERROR -330" (SELF-TEST FAIL) to be displayed.

Secondary Circuits

The turn-on selftest sequence of the secondary microprocessor consists of two parts:

1. The selftest is performed by the secondary microprocessor (U301) and starts when the secondary power clear (SPCLR) signal goes false (High). Any secondary failures are reported to the primary interface. The secondary microprocessor will first check its internal RAM, ROM, and timer. If one of these tests fail, selftest is halted and "ERROR xxx" will be displayed (see Table 3-2).

It is possible for a secondary RAM, ROM, or Timer failure to "lock-up" the secondary processor and no secondary error number is reported. If this occurs try to isolate the problem by performing the Secondary Signature Analysis Tests.

2. If part 1 passes selftest, the test continues by checking the secondary EEPROM (U342). Next the operation and accuracy of the main and transient DACs are tested. If these tests pass, the volts/amps readings will appear on the display indicating that the selftest has been successfully completed.

If the EEPROM or any of the DAC tests fail, or if no module is installed in the mainframe, the front panel displays "ERROR -xxx" for 2 seconds (see Table 3-2), then "INP DOWN 1" followed by "INPUT DWN". Finally the Err annunciator will turn on. Depressing the ______ (blue shift key) followed by the **Error** key, will cause "ERROR -330" (SELF-TEST FAIL) to be displayed. Depressing these keys a second time, will cause "ERROR -240" (HARDWARE ERROR) to be displayed. Note that Error -240 only appears with secondary component failures.

If error "UNKNOWN" is displayed the EEPROM (U342) must be initialized.

The "INPUT DWN" message can also occur because of communication problems between the primary and secondary processor. Check the SRX and STX data lines (test points (15) and (16) on Table 3-3) for the presence of data pulses using a logic probe.

"INPUT DWN" can also occur if the line switch is cycled repetitively, or under certain abnormal line conditions. If this is the case, cycling ac power to the load will reset the load.

Table 3-2. Selftest Error Code

Code	Error Description	Procedure		
PRIMARY PART 2 ERRORS				
-4	The primary microprocessor U203 read/write test to the GPIB talker/listener chip U202 failed.	Use Primary SA Test Tables 3-4 and 3-6 to check address and data lines.		
- 5	The primary microprocessor U203 test of the internal trigger lines failed.	Use Primary SA Test Table 3-7 to check the primary trigger circuit. Then refer to "Trigger Circuit Troubleshooting" and Figure 3-8.		
- 6	The primary microprocessor U203 test of the ac line trigger circuits failed.	Same as above.		
- 7	The primary microprocessor U203 test of the timer circuit trigger failed.	Same as above.		
-101	SECONDARY PART 1 ERRORS Secondary microprocessor U301 internal RAM failure.	Replace U301.		
-102	Either power board disconnected. thermistor RT2 missing or open, or U301 internal ROM failure.	Make sure power board connected. If connected. check RT2. If O.K., replace U301.		
-103	Secondary microprocessor U301 internal timer failure.	Replace U301.		
SECONDARY PART 2 ERRORS				
-104	EEPROM (U342) checksum error.	Create a checksum by programming: "CAL:MODE ON;:CAL:SAVE" then turn power off, wait; 5 seconds and turn power on. If error code -104 does not appear again, calibrate the load as described in the Operating Manual. If error code -104 does appear again, check the EEPON line (test point 7 in Table 3-3). If EEPON is ok, use SA Table 3-14 (U341) to check the data input and output lines to U342.		
-105	Main DAC circuit (U320/U326) zero or full scale point is above the high tolerance level.	Refer to "DAC Circuits Troubleshooting" and Figure 3-3.		
-106	Main DAC circuit (U320/U326) zero or full scale point is below the low tolerance level.	Same as above.		
-107	Transient DAC circuit (U321/U325) zero or full scale point is above the high tolerance level.	Same as above.		
-108	Transient DAC circuit (U321/325) zero or full scale point is below the low tolerance level.	Same as above.		

Test Points

Table 3-3 lists test points that are referred to in many of the troubleshooting procedures. Each test point is identified by a circled number (e.g., ①), the circuit point (e.g., U308-1), and signal name (e.g., CV PROG). The "Measurement and Conditions" column describes the signal that should be measured and the conditions (e.g. operating mode) required to make the measurement. The circuit locations of the test points are shown on the troubleshooting diagrams (Figures 3-3 through 3-11), and on the component locations diagrams that accompany the schematic sheets.

Note:

When taking measurements, make sure that you connect the DMM or oscilloscope common to the proper circuit common as indicated in Table 3-3.

Table 3-3. Test Points

Test Point Number	Signal	Measurement and Conditions	
GPIB BOARD			
Connect meter or scope common to test point ① when taking measurements at test points			
2 through 7			
① - C233	Primary/Chassis ground	-	
2 + C233	+ 5V (primary bias)	+ 5V (4.8 to 5.2V)	
3 cath -D212	+ 13V (primary bias rectifiers)	+ 13V (13 to 17 Vdc)	
4 J2-10	PCLR1	Held low (0V) for 80ms (approx.) at power on and then goes high (5V).	
5 Q201-3	PCLR	Goes high for 80ms (approx.) at power on and then goes low.	
6 Q201-12	PCLR	Held low for 80ms (approx.) at power on and then goes high.	
⑦ Q201-6	EEPON	At power on, holds the EEPROM's clock off to protect against accidental data write when power is initially applied.	
Connect meter com	_	ROL BOARD neasurements at test points (9) through (45).	
8 +C352	Secondary common		
9 w1	+5V secondary bias	+5V (4.8 to 5.2V)	
10 +C353	+ 15V secondary bias	$+ 15V \pm 1V$	
(1) - C352	-15V secondary bias	$-15V \pm 1V$	
(12) cath -D315	+ 26V (secondary bias rectifiers)	+ 23V to + 29V	
(3) Q301-12	SPCLR	Held low for 80ms (approx.) at power on and then goes high.	
4 Q301-6	EEPON	At power on, holds the EEPROM's clock off to protect against accidental data writes when power is initially applied.	
15 U333-7	SRX	Secondary receive serial data line. Toggles between 0 and 5V.	
16 U334-3	STX	Secondary transmit serial data line. Toggles between 0 and 5V.	

Table 3-3. Test Points (continued)

Test Point Number	Signal	Measurement and Conditions	
① U308-1	CV PROG	In VOLT MODE, + 10V with full rated voltage programmed; +0.5V with 3 volts programmed.	
		In CURR MODE or RES MODE (middle and high ohm ranges), + 13V.	
		In RES MODE (low ohm range), < 1V.	
18 U308-7	CC PROG	In CURR MODE, + 10V with full rated current programmed.	
		In VOLT MODE, RES MODE (low ohm range), or with INPUT OFF: - 0.5V.	
		In RES MODE (middle and high ohm ranges), < 1V.	
19 U351-10	TRANS_EN	High level with transient operation programmed on (TRAN ON). Low level with transient operation programmed off (TRAN OFF).	
20 U324-1	SLEW	In CURR MODE, -10V with full rated current programmed; 0V with zero current programmed.	
		In VOLT MODE, -10V with full rated voltage programmed; 0V with zero voltage programmed.	
② U309-16	DAC_REF	Low level in CURR or VOLT MODE. High level in RES MODE (any range).	
② U309-8	CR	Low level in RES MODE (low ohm range). High level in CURR, VOLT, or RES (middle or high ohm range) MODE.	
② U309-1	CG	Low level in RES MODE (middle or high ohm range). High level in CURR, VOLT, or RES (low ohm range) MODE.	
24 TB301-9	PORT	High level with PORT0 ON programmed. Low level with PROT0 OFF programmed.	
25 U329-4	-10 V Ref	-10V (9.95 to 10.05V).	
6 U323-1	+ 12V Ref	+ 12V (11.28 to 11.44V).	
	T	POWER BOARD	
② U5-5	PROG	Under normal operating conditions (input is regulated) measurement	
(60501B/02B/03B)		should be:	
U12-5		-0.22 V X Iin (60501B) -0.11V X Iin (60502B/07B)	
60504B/07B)		-0.66V X Iin (60503B)	
		-0.055V X Iin (60504B)	
		With input unregulated or disconnected, the measurement will be:	
		≈2V in CURR Mode	
		$\approx +0.2$ V in VOLT or RES MODE	

Table 3-3. Test Points (continued)

Test Point Number	Signal	Measurement and Conditions
28 cath-D17	+ OV	+ 14V when OV condition is false (normal)13V when OV condition is true.
29 U16-1	CC Loop Gain control	+ 15V when input voltage is more than 2.5V15V when input voltage is less than 2.5V.
30	NOT USED	
③ U9-1	RNG	Low level when the high current range or the middle resistance range is programmed. High level when the low current range, the low resistance range, or the high resistance range is programmed.
32 U14-1 U15-1*	-VMON	-0.167 X Input Voltage (e.g0.167 X 60 = -10.02V)
33 cath D11	+ OP	- 0.9V (full rated voltage input) to - 6V (zero volts input) when the OP condition is false. Pulses when the OP condition is true. See test point 3.
34 U10-1,2,13,14	-OP	-14V when the OP condition is false. Pulses when the OP condition is true. See Figure 3-10.
35 U17-1	-VMONA	-0.167 X Input Voltage (e.g. 0.167 X 60 = - 10.02V)
36 37 38	NOT USED	
(39) cath-D55	OC circuit control	+ 13V when OC condition false (normal). + 8V when OC condition is true or when input stages are unregulated.
④ Q11-E	OC circuit control	+ 10V when OC condition is false (normal). + 8.5V when unregulated or when OC condition is true.
(41) cath-D23	Input Power Stage Turn on	+ 5V when turned on. 0V when turned off.
42 U5-1 U5-7*	Input Power Stage 2 D	(approx.) 6± .5V with full rated input current. (approx.) -0.5V with the input off.
(43) Q2-1	Input Power Stage 2 D	(approx.) 5.2V with full rated input current. (approx.) 4.0V with 10% rated input current. (approx.) 2.5V at zero input current.
44 U6-7 U6-1*	Input Power Stage 2 D	1.25V for 60501B, 60502B, 60503B, 60504B. 0.625V for 60507B at full input current.
€ 5 U15-1 U14-1*	-IMON	-10.02V at full input current.

^{*}ON 60504B/07B ONLY.

Signature Analysis

Note:	You cannot use signature analysis to troubleshoot units with the following serial numbers:
	Agilent 6050A: 3714A05433 and up; US37140101 and up.
	Agilent 6051A: 3714A00711 and up; US37140101 and up.

The easiest and most efficient method of troubleshooting microprocessor based instruments is signature analysis (SA). The SA technique is similar to signal tracing with an oscilloscope in linear circuits. Part of the microcomputer memory is dedicated to signature analysis and a known bit stream is generated to stimulate as many nodes as possible within the circuit. However, because it is virtually impossible to analyze a bit stream with an oscilloscope, a signature analyzer is used to compress the bit stream into a four character signature. By comparing signatures of the IC under test to the correct signatures for each node, faults can usually be isolated to one or two components.

Signature analysis tests are provided for most of the digital circuits in the primary and secondary circuits of the Electronic Load. There are six primary SA tests given in Tables 3-4 through 3-9, and five secondary tests given in Tables 3-10 through 3-14. Refer to "Firmware Revisions" for information about the valid firmware revisions for the signature analysis tables.

References are made to the appropriate SA test table from the troubleshooting flow charts or procedures. The following general rules apply to signature analysis testing of the primary and secondary circuits.

- 1. Be sure to use the correct test setup connections for the specific test. See "Test Setup for Signature Analysis".
- 2. Note the signatures for Vcc (+5V) and common on the IC being examined. If an incorrect signature is the same as that of Vcc or common, that pin (or point in the circuit) is probably shorted to Vcc or ground.
- 3. If two pins have identical signatures, they are probably shorted together.
- 4. If two signatures are similar, it is only a coincidence.
- 5. If a signature is incorrect at an input pin, but is correct at its source (output of previous IC), check for printed circuit track or soldering problems.
- 6. An incorrect signature at an output could be caused by a faulty component producing the output. It can also be caused by an input short circuit in another component on the board.

Firmware Revisions

The primary ROM chip (U205) and the secondary microprocessor chip (U301) are identified with labels that specify the revision of the Electronic Load's firmware.

The signatures given in Primary SA Tables 3-4 through 3-9 are valid for ROM chip U205 firmware revision "Rev A.01.01". You can also identify the revision of the U205 firmware using the *IDN? query in the program listed below.

```
10 DIM L$[40]
20 OUTPUT 705;"*IDN?"
30 ENTER 705; L$
40 DISP L$
50 END
```

The computer will display the Electronic Load mainframe's model number and the firmware revision of the U205 primary ROM chip: "Agilent-Technologies, 6050A, 0,A.01.01".

The signatures given in Secondary SA Tables 3-10 through 3-14 are valid for secondary microprocessor chip U301 revision "Rev A.02.01". Note that the U301 revision is only identified by the label; it cannot be read back using the *IDN? query.

Test Header Jumper Positions

The Electronic Load mainframe contains a primary test header (TP201) located on the GPIB Board, and each module contains a secondary test header (TP301) located on the Control Board. The test headers have jumper positions for signature analysis and other functions as described below.

Primary Test Header TP201 Pins	Description		
1 and 2	+ 5V (primary).		
3 and 4	With jumper RTP201 installed between these pins, the primary microprocessor is placed in the SA mode. Removing RTP201 takes the microprocessor out of the SA mode.		
5 and 6	With jumper RTP201 installed between these pins, the primary microprocessor will ignore calibration commands, providing security against unauthorized calibration. With RTP201 removed, the microprocessor will respond to calibration commands.		
7 and 8*	SA gate test points (normal operating/storage position for RTP201).		
9 thru 16	Test points for the chip select signals CSP0 through CSP7.		

^{*}As shipped from the factory, jumper RTP201 is installed between TP201 pins 7 and 8. Both of these pins are connected to the primary SA gate signal, which is used as the start/stop signal when taking signatures during primary SA testing. See "Test Setup for Signature Analysis"

Secondary Test Header TP301 Pins	Description		
1 and 2	With jumper RTP301 installed between these pins, the secondary microprocessor is placed in the SA mode. Removing RTP301 takes the microprocessor out of the SA mode.		
3 and 4*	SA gate test points (normal operating/storage position for RTP301).		
5 and 7	With RTP301 installed between these pins, the secondary microprocessor will skip selftest at power-on. With RTP301 removed, the selftest will be performed.		
6	Connected to secondary common.		
8	+ 5V (secondary).		

^{*} As shipped from the factory, jumper RTP301 is installed between pins 3 and 4. Both of these pins are connected to the secondary SA gate signal, which is used as the start/stop signal when taking signatures during secondary SA testing. See "Test Setup for Signature Analysis".

Test Setup for Signature Analysis

Chapter 2 contains instructions for disassembling the mainframe and modules to allow access for troubleshooting and repair. Figure 3-2 illustrates the primary (TP201) and secondary (TP301) test header connections required to perform the signature analysis tests given in Tables 3-4 through 3-14.

The following paragraphs describe the setups for troubleshooting the mainframe GPIB Board, and the Control Board and Power Board in the load modules. As a general rule, the GPIB Board is tested first, with no modules connected. Then, the GPIB Board is installed in the mainframe and individual load modules are tested.

GPIB Board Troubleshooting Setup

To troubleshoot the GPIB Board, it must be removed from the mainframe to allow access to components. DO NOT CONNECT THE AC MAINS LINE CORD TO THE GPIB BOARD WHILE TROUBLESHOOTING THE GPIB BOARD.

- a. Carefully lay the GPIB Board on an insulated work surface. Do not slide the board around.
- b. Connect a 15-volt 0.3-amp dc power supply to J207, pins 4 and 5. See Figure 3-2a for the location of J207. The polarity of the connections to J207 pins 4 and 5 does not matter. Use of the J207-connector assembly supplied with Service Kit 06050-60004 is recommended.
- c. Make the following connections for signature analysis.
 - 1. Connect jumper RTP201 in the SA position (SA_MODE) across pins 3 and 4 of the primary test header TP201 (see Figure 3-2b).
 - 2. Set up and connect the signature analyzer's CLOCK, START, STOP, and GND inputs as follows:

Signature Analyzer Input CLOCK	Setting	TP201 Connection Connections are listed for each specific test (see Tables 3-4 thru 3-9).
START .		TP201-7
STOP		TP201-8
GND		TP201-6

- d. Turn on the signature analyzer and use the probe to take signatures at the applicable test points given in the signature analysis tables.
- e. Upon completion of the signature analysis tests, disconnect the signature analyzer leads and return jumper RTP201 to its normal operating position between TP201-1 and TP201-2.

Load Module Troubleshooting Setup

To troubleshoot a load module, the Control Board and Power Board must be separated following the instructions given in Chapter 2. The GPIB Board should be installed in the mainframe, with the ac mains line cord connected normally. Connections between the GPIB Board and the load module under test are made using the extender cable assembly supplied in Service Kit 06050-60004.

WARNING

AC mains voltage is present on exposed pins on the top edge of the mainframe GPIB Board and each module whenever the unit is turned on.

- a. Carefully lay the Control Board and Power Board on an insulated work surface directly next to the mainframe.
- b. Using extender cables, connect the Control Board to the GPIB Board in the mainframe.
- c. Make the following connections for signature analysis.
 - 1. Connect jumper RTP301 in the SA position (SA_EN) across pins 1 and 2 of the secondary test header TP301 as shown in Figure 3-2c.
 - 2. Set up and connect the signature analyzer 's CLOCK, START, STOP, and GND inputs as follows:

Signature Analyzer Input	Edge Setting	TP201 Connection
CLOCK		TP301-7
START		TP301-3
STOP		TP301-4
GND		TP301-6

- d. Turn on the signature analyzer and use the probe to take signatures at the applicable test points given in the signature analysis tables.
- e. Upon completion of the signature analysis tests, disconnect the signature analyzer leads and return jumper RTP301 to its normal operating position between TP301-3 and TP301-4.

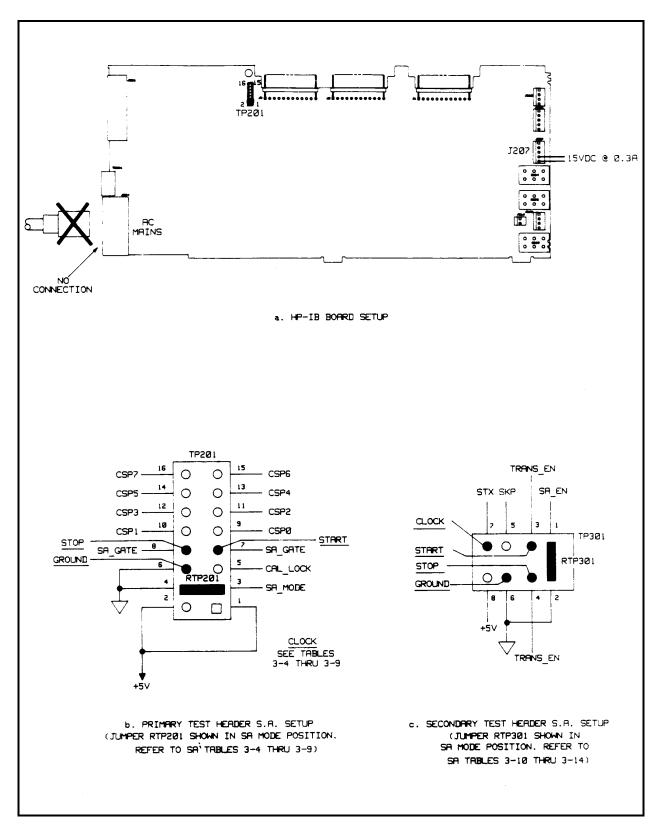


Figure 3-2. Signature Analysis Setup

Table 3-4. Primary Microprocessor Signature Analysis

Description: These signatures check primary microprocessor U203, ROM U205, and RAM U206. The signatures are valid for ROM U205 firmware revision "Rev A.01.01". Use the test setup described in "Test Setup for S.A.". Connect the signature analyzer's CLOCK input to U207-9.

C:		-4		
ы	2N	aι	ur	es:

Signatures:				
	μP U203	ROM U205	RAM U206	
+5V	U203-4,7,21 = 1HC4	U205-28 = 1HC4	U206-28,14 = IHC4	
Common	U203-1,9,10	U205-14	U206-1,14,22	
4 MHz	U203-2,3		, ,	
1 MHz	U203-40	U205-22	U206-26	
	U203-6 = +5V	0203-22	0200-20	
PLCR	0203-0 = +3 v			
A (O)	11202 12 - 4249	U205-10 = A2A8	U206-10 = A2A8	
A(0)	U203-13 = A2A8			
A(1)	U203-14 = 7379	U205-9 = 7379	U206-9 = 7379	
A(2)	U203-15 = ICF8	U205-8 = 1CF8	U206-8 = 1CF8	
A(3)	U203-16 = CC35	U205-7 = CC35	U206-7 = CC35	
A(4)	U203-17 = HP8C	U205-6 = HP8C	U206-6 = HP8C	
A(5)	U203-18 = 2HHU	U205-5 = 2HHU	U206-5 = 2HHU	
A(6)	U203-19 = 6AO7	U205-4 = 6AO7	U206-4 = 6AO7	
A(7)	U203-20 = F5CP	U205-3 = F5CP	U206-3 = F5CP	
A(8)	U203-29 = A21F	U205-25 = A21F	U206-25 = A21F	
A(9)	U203-28 = F103	U205-24 = F103	U206-24 = F103	
A(10)	U203-27 = 56HC	U205-21 = 56HC	U206-21 = 56HC	
	U203-27 = 36HC U203-26 = 45FH	U205-21 = 30HC U205-23 = 45FH	U206-21 = 36HC U206-23 = 45FH	
A(11)				
A(12)	U203-25 = 66C4	U205-2 = 66C4	U206-2 = 66C4	
A(13)	U203-24 = HP62	U205-26 = HP62		
A(14)	U203-23 = C861	U205-27 = C861		
A(15)	U203-22 = 71CU	U205-1 = 71CU		
D(0)	U203-37 = HOAA	U205-11 = HOAA	U206-11 = HOAA	
D(1)	U203-36 = FA61	U205-12 = FA61	U206-12 = FA61	
D(2)	U203-35 = A477	U205-13 = A477	U206-13 = A477	
D(3)	U203-34 = HUUO	U205-15 = HUUO	U206-15 = HUUO	
D(4)	U203-33 = CP8H	U205-16 = CP8H	U206-16 = CP8H	
D(5)	U203-32 = 3H8H	U205-17 = 3H8H	U206-17 = 3H8H	
D(6)	U203-31 = CPPH	U205-18 = CPPH	U206-18 = CPPH	
D(7)	U203-30 = F446	U205-19 = F446	U206-19 = F446	
CED IN	11202 11 - 2244			
SER_IN	U203-11 = 2244			
SER_OUT	U203-12 = unstable			
R/W	U203-38 = HA6H		U206-27 = HA6H	
CE		U205-20 = HOC7		
CE1		U206-22 = IHC4	U206-20 = AA38	
	11207 2 - 114 OD	11315 A - 11AOD	11217 2 - 71611	
	U207-3 = UA8P	U215-4 = UA8P	U217-3 = 71CU	
	U207-4 = P73A	U215-5 = FH03	U217-4 = C861	
	U207-8 = E clock	U215-6 = AA38	U217-5 = HP62	
	U207-9 = E clock		U217-6 = HOC7	
	U207-12 = FHO3		U217-8 = UA8P	
	U207-13 = HOC7		U217-9 = 66C4	
			U217-10 = 45FH	
			U217-11 = 56HC	
			021/11 30110	

Table 3-5. GPIB Interface Signature Analysis (Primary)

Description: These signatures check the GP-IB talker/listener IC U202. The signatures are valid for ROM U205 firmware revision "Rev A.01.01". Use the test setup described in "Test Setup for S.A." Connect the signature analyzer's CLOCK input to TP201-12 (CS3).

Signatures:

U202-1 = 7339 pulsing U202-2 =U202-3 = 1 MHz "E" clockU202-4 = OOOO PLCRU202-5 = OOOO pulsing U202-6 U202-7 = 7339 + 5VU202-8 = OOOO commonU202-9 = 7339 pulsing U202-10 = OOOO pulsing U202-11 =U202-12 = OC57U202-13 = O5ACU202-14 = 167UU202-15 = A83PU202-16 = 69P1U202-17 = 2O5AU202-18 = 1427U202-19 = H6C9U202-20 = OOOO commonU202-21 = 23UHU202-22 = 54A6U202-23 = 8OAOU202-24 = 7339U202-25 = 7339U202-26 = 7339U202-27 = 713FU202-28 = 7692U202-29 = 71PFU202-30 = U253U202-31 = 338FU202-32 = 5363U202-33 = 6314U202-34 = 7C2UU202-35 = 7435U202-36 = 7339U202-37 = 7339U202-38 = 7339U202-39 = 7435

U202-40 = 7339 + 5V

Table 3-6. Front Panel Interface Signature Analysis (Primary)

Description: These signatures check the front panel interface IC's U246 U209, U210 and U212. The signatures are valid for ROM U205 firmware revision "Rev A.01.01". Use the test setup described in "Test Setup for S.A.". Connect the signature analyzer's CLOCK input to the chip select line of the IC under test as specified below.

Signatures:	CL OCV to TD201 14 (CS5)
U246 Display Driver - connect	CLOCK to TP201-14 (CS5)
U246-1 = O1UF + 5V	U246-11 = OOOO pulsing
U246-2 = OO81	U246-12 = OOO8
U246-3 = O1O2	U246-13 = OO1O
U246-4 = OO81	U46-14 = OOO8
U246-5 = OO4O	U46-15 = OOO4
U246-6 = OO2O	U246-16 = OOO2
U246-7 = OO4O	U246-17 = OOO4
U246-8 = OO2O	U246-18 = OOO2
U246-9 = OO1O	U246-19 = OOO1
U246-1O = OOOO common	U246-20 = O1UF + 5V
U209, U212 Keypad Drivers - connect	CLOCK to TP201-13 (CS4)
U209-1 = O7U3 +5V	U209-11 = OOOO pulsing
U209-2 = OO81	U209-12 = O3O6
U209-3 = O1O2	U209-13 = O6OH
U209-4 = O64U	U209-14 = OOO8
U209-5 = O327	U209-15 = OOO4
U209-6 = O3OU	U209-16 = O3O5
U209-7 = O61U	U209-17 = O6OC
U209-8 = O225	U209-18 = OO81
U209-9 = O112	U209-19 = OO4O
U209-10 = OOOO common	U209-20 = O7U3 + 5V
U212-1 = OO81	U212-8 = O4OA
U212-2 = O7OH	U212-9 = O3OH
U212-3 = OOO4	U212-10 = O4OA
U212-4 = O7U4	U212-11 = O327
U212-5 = O112	U212-12 = O78F
U212-6 = O6OU	U212-13 = OO4O
U212-7 = OOOO common	U212-14 = O7U3 + 5V
U210 Keypad Receiver - connect	CLOCK to TP201-10 (CS11)
U210-1,19 = OOOO pulsing Lo (Chip Select)	
U210-2,18 = O1UF	press keypad " 1 " = O17H
U210-3,17 = O1UF	press keypad " 8 " = O17H
U210-4,16 = O1UF	L AL.
U210-5,15 = O1UF	press keypad " 4 " = O17H
U210-6,14 = O1UF	press keypad " 9 " = O17H
U210-7,13 = O1UF	press keypad " 7 " = O17H
U210-8,12 = O1UF	press keypad " 0 " = O17H
U210-9,11 = O1UF	pulsing 9 (fast), 11 (slow)
U210-10 = OOOO common	
U210-20 = O1UF +5V	

Table 3-7. Trigger Circuit Signature Analysis (Primary)

Description: These signatures check the operation of the primary trigger circuits. The signatures are valid for ROM U205 firmware revision "Rev A.01.01". Use the test setup described in "Test Setup for S.A.". Connect the signature analyzer's CLOCK input to the IC under test as specified below.

Signatures:

U208 - connect CLOCK to U235-12 (CS10) U208-1 = 7U39 + 5VU208-11 = OOOO pulsing LOU208-2 = 28F7U208-12 = 162PU208-3 = 518PU208-13 = 2F5FU208-14 = 2P41U208-4 = 2OH3U208-5 = 1069U208-15 = 1720U208-6 = 1009U208-16 = 1726U208-7 = 2O12U208-17 = 2P4HU208-8 = 2072U208-18 = 2P4CU208-9 = 1O39U208-19 = 1725U208-10 = OOOOU208-20 = 7U39 + 5VU207, 213-217, 219, 226, 247 - connect CLOCK to U207-9 (E clock) U233-8 = 154UU247-1 = OOOOU219-1 = C762U233-9 = 767FU247-2 = 3P88U219-2 = OOOOU219-3 = AAH6U233-10 = 6333U247-3 = H451U233-11 = 767FU247-4 = 145PU219-4 = 7P87U233-12 = U15FU247-5 = 4C3HU219-5 = H451U247-6 = H451U233-13 = 154UU219-6 = C762U247-7 = OOOO comU219-7 = OOOO comU207-5 = C762U247-8 = H451U219-8 = 7P87U207-6 = AAH6U247-9 = 648AU219-9 = OOOOU247-10 = 648AU207-10 = OOOOU219-10 = 6333U207-11 = 1HC4U247-11 = H451U219-11 = 7P87U247-12 = 1HC4U219-12 = OOOOU217-1 = AAH6U247-13 = 5U47U219-13 = 6333U217-2 = 1HC4U247-14 = 1HC4 + 5VU219-14 = 1HC4 + 5VU217-12 = OOOOU217-13 = OOOOU215-1,2,3,8,9,10,11,12,13 = 6333U213-1 = OOOOU214-1 = OOOOU216-1 = 8U6AU226-1 = FA61U213-2 = OOOOU214-2 = 0000U216-2 = OOOOU226-2 = A477U213-3 = OOOOU214-3 = 5AC1U216-3 = OOOOU226-3 = HUUOU213-4 = 3842U214-4 = 92HPU216-4 = 1HC4U226-4 = CP8HU213-5 = OOUUU214-5 = 92HPU216-5 = OOOOU226-5 = 3H8HU213-6 = OOOOU214-6 = 8U6AU216-6 = 1HC4U226-6 = CPPHU213-7 = 5AC1U214-7 = AAH6U216-7 = 1HC4U226-7 = F446U226-8 = OOOOU213-8 = OOOO comU214-8 = OOOO comU216-8 = OOOO comU213-9 = 92HPU214-9 = H525U216-9 = OOOOU226-9 = 1HC4U213-10 = E clockU214-10 = PU28U216-10 = 1HC4U226-10 = 1HC4U213-11 = AAH6U214-11 = 885FU216-11 = 1HC4U226-11 = 92HPU213-12 = OOOOU214-12 = OOOOU216-12 = 1HC4U226-12 = OOOOU213-13 = OOOOU214-13 = OOOOU216-13 = 8U6AU226-13 = 1HC4U213-14 = OOOOU214-14 = OOOOU216-14 = OOOOU226-14 = C762U213-15 = OOOOU214-15 = OOOOU216-15 = C762U226-15 = HOAA

U216-16 = 1HC4 + 5V

U226-16 = 1HC4 + 5V

U213-16 = 1HC4 + 5V

U214-16 = 1HC4 + 5V

Table 3-7. Trigger Circuit Signature Analysis (Primary) continued

```
U228 - connect CLOCK = TP201-16 (CS7)
U228-1 = UFP6 + 5V
                                            U228-11 = OOOO Pulsing LO
U228-2 = 5505
                                            U228-12 = OOO8
U228-3 = AAOC
                                            U228-13 = OO10
U228-4 = 6679
                                            U228-14 = OOO8
U228-5 = 333F
                                            U228-15 = OOO4
U228-6 = OU39
                                            U228-16 = OOO2
U228-7 = 1P72
                                            U228-17 = OOO4
U228-8 = OO20
                                            U228-18 = OOO2
U228-9 = OO10
                                            U228-19 = OOO1
U228-10 = OOOO com
                                            U228-20 = UFP6 + 5V
```

Table 3-8. Module Interface Signature Analysis (Primary)

Description: These signatures check the module communications, U229 data transmission to modules, U230 data transmission from modules, and U239, which indicates the number of modules installed. Connect the signature analyzer's clock input to the IC under test as specified below.

U229, 230 - connect CLOCK to U207-9 (E clock)

U229-1 = C2CC	U230-1 = 1HC4
U229-2 = 5HCF	U230-2 = 1HC4
U229-3 = 56U6	U230-3 = 1HC4
U229-4 = unstable	U230-4 = 1HC4
U229-5 = U123	U230-5 = 3UUO
U229-6 = 1HC4 + 5V	U230-6 = 2244
U229-7 = unstable	U230-7 = U123
U229-8 = OOOO com	U230-8 = OOOO com
U229-9 = unstable	U230-9 = 56U6
U229-10 = unstable	U230-10= 5HCF
U229-11 = unstable	U230-11 = C2CC
U229-12 = unstable	U230-12 = OOOO
U229-13 = unstable	U230-13 = 1HC4
U229-14 = unstable	U230-14 = 1HC4
U229-15 = unstable	U230-15 = 1HC4
U229-16 = 1HC4 + 5V	U230-16 = 1HC4 + 5V

U239 - connect CLOCK to CS9 (U235-13)

Chip Select	U239-1,19 = OOOO Pulse LO	
Slot 1	U239-2,18 = O1UF	short $J2-6$ to $J2-8 = OOOO$
Slot 2	U239-4,16 = O1UF	short $J2-5$ to $J2-8 = OOOO$
Slot 3	U239-6,14 = O1UF	short $J2-4$ to $J2-8 = OOOO$
Slot 4	U239-8,12 = O1UF	short $J2-3$ to $J2-8 = OOOO$
Slot 5	U239-11,9 = O1UF	short $J2-2$ to $12-8 = OOOO$
Slot 6	U239-13,7 = O1UF	short $J2-1$ to $J2-8 = OOOO$
Slot 7	U239-15,5 = O1UF	short J208-4 to J2-8= OOOO
CAL_LOCK	U239-17,3 = O1UF	short TP201-5 to TP201- $4 = OOOO$

Table 3-9. Fan Speed Control Signature Analysis (Primary)

Description: These signatures check the fan speed control circuits. Connect the signature analyzer's clock input to the IC under test as specified below.

Signatures:

U227- connect CLOCK to TP201-15 (CS6)

U227-1 = O1UF + 5V	U227-11 = OOOO Pulse LO
U227-2 = OO81	U227-12 = OOO8
U227-3 = O102	U227-13 = OO10
U2274 = OO81	U227-14 = OOO8
U227-5 = OO40	U227-15 = OOO4
U227-6 = OO20	U227-16 = OOO2
U227-7 = OO40	U227-17 = OOO4
U227-8 = OO20	U227-18 = OOO2
U227-9 = OO10	U227-19 = OOO1
U227-10 = OOOO com	U227-20 = O1UF + 5V

U233, U241, 242, 245 - connect CLOCK to U207-9 (E clock)

U241-1 = 1HC4 + 5V	U242-1 = 1HC4 + 5V
U241-2 = 7P1P	U242-2 = OOOO

U233-1 = 2171U233-2 = 2171

U233-3 = OOOO Pulsing LO

U233-4 = 762CU233-5 = 762C

U233-6 = OOOO Pulsing LO

U233-7 = OOOO com

U245-1 = 1233	U245-8 = OOOO
U245-2 = OOOO	U245-9 = 1687
U245-3 = 85F9	U245-10 = OOOO
U245-4 = OOOO	U245-11 = 5255

U245-5 = U28H U245-12 = OOOO Pulsing

U245-6 = OOOO U245-13 = 899A U245-7 = OOOO com U245-14 = 1HC4 + 5V

Table 3-10. Secondary Microprocessor Signature Analysis

Description: These signatures check secondary microprocessor U301 and latches U302 and U330. The signatures are valid for U301 firrnware revisions "Rev A.02.01". Use the test setup described in "Test Setup for S.A."

Signatures:

Front Panel Display = "INPUT DWN"

	U301	U302	U330
+ 5V	U301-7,4,9,21,39	U302-20	U330 20
Common	U301-1	U302-10	U330-10
SPCLR	U301-6 = +5V	U302-1 = +5V	U330-1 = +5V
4 MHz	U301-2,3		
1 MHz	U301-40		
SD(7)	U301-30 = H083	U302-14 = H083	U330-4 = H083
SD(6)	U301-31 = IUUO	U302-17 = 1UUO	U330-17 = IUUO
SD(5)	U301-32 = 8A16	U302-13 = 8A16	U330-13 = 8A16
SD(4)	U301-33 = 834A	U302-8=834A	U330-7 = 834A
SD(3)	U301-34 = P070	U302-18 = P070	U330-3 = P070
SD(2)	U301-35 = U93A	U302-3=U94A	U330-18 = U93A
SD(1)	U301-36 = AP48	U302-4= AP48	U330-14 = AP48
SD(0)	U301-37 = UFOA	U302-7= UFOA	U330-8 = UFOA
	U301-8 = +5V	U302-5= 6A19	U330-9 = 6AH2
	U301-8 = +3V U301-10 = H82C	U302-5 = 0A19 U302-6 = P921	U330-15 = 1ACH
	U301-10 = 1182C U301-11 = +5V	U302-2= A9H8	U330-13 = 1ACH U330-19 = 46AH
	U301-12 = 0000	U302-9 = C1H7	U330-11 = H82C pulsing
	U301-13 = 24A7	U302-11 = 9457	U330-2 = H82C pulsing
	U301-14 = A264	U302-16 = 3505	U330-16 = U746
	U301-15 = OUPA	U302-15 = H210	U330-12 = HH1A
	U301-16 = HHC8	U302-12 = 0CH8	U330-5 = 64PC
	U301-17 = 41UA	U302-19 = AUH1	U330-6 = 746A
	U301-18 = 9986		
	U301-19 = HCA7		
	U301-20 = 0620		
	U301-23 = 0000		
	U301-24 = 77UA		
	U301-25 = 0000		
	U301-26 = 927H		
	U301-27 = 15C4		
	U301-28 = 3PAF		
	U301-29 = 4234		
	U318-10 = 41AH		
	U318-8 = 9986		
	U318-12 = 64PC		
	U318-2,3,5,6,7,9,13 = 0000		
	U318-1,4,11,14 = H82C		

Table 3-11. Main DAC, Transient DAC, Data Bus Signature Analysis (Secondary)

Description: These signatures check main DAC U320, transient DAC U321, and secondary data bus B latches U319. The signatures are valid for U301 firmware revisions "Rev A.02.01". Use the test setup described in "Test Setup for S.A.".

Signatures:

	U319	U320	U321
Common	U319-20 = +5V U319-10	U320-20 = +15V	U321-20 = +15V
	U319-10 U319-1 = +5V	U320-1,3,10,12,18	U321-1,3,10,12,18
SPCLR			
SD(0)	U319-7 = UFOA		
SD(1)	U319-13 = AP48		
SD(2)	U319-14 = U93A U319-8 = P070		
SD(3) SD(4)	U319-8 = P070 U319-4 = 834A		
SD(4) SD(5)	U319-3 = 8A16		
SD(5) SD(6)	U319-18 = IUUO		
SD(7)	U319-17 = H083		
	2017 17 11000		
SDB(0)	U319-6 = F592	U320-7 = F592	U321-7 = F592
SDB(l)	U319-12 = F3P2	U320-6 = F3P2	U321-6 = F3P2
SDB(2)	U319-15 = 4461	U320-5 = 4461	U321-5 = 4461
SD8(3)	U319-9 = 5UA2	U320-4 = 5UA2	U321-4 = 5UA2
SDB(4)	U319-5 = 63AU	U320-16 = 63AU	U321-16 = 63AU
SDB(5)	U319-2 = 17C1	U320-15 = 17C1	U321-15 = 17C1
SDB(6)	U319-19 = 6A0C	U320-14 = 6A0C	U321-14 = 6A0C
SDB(7)	U319-16 = P635	U320-13 = P635	U321-13 = P635
CLIZ	11210 11 40112		
CLK WR1	U319-11 = 4OH3	U320-2 = 57A2	
WR1		0.320-2 - 3/A2	U321-2 = 1UPU
XBFER		U320-17 = 41AH	U321-17 = 41AH
B1/B2		U320-17 = 41A11 U320-19 = 0620	0321 17 - 1 1M1
1			

Table 3-12. Transient Generator Signature Analysis (Secondary)

-	_		_		through U355. Th	_	valid for U301
	ons "Rev A.0	2.01". Use the	e test setup d	escribed in t	he "Test Setup for	S.A.".	
Signatures:	11254 20	11255 20	11240.20	11250 16	11251 (7.0	11252 16	11252 14
+5V	U354-20	U355-20	U349-20	U350-16	U351-6,7,8	U352-16	U353-14
Common	U354-10	U355-10	U349-10	U350-8	U351-4,5,18	U352-8	U353-7
SD(0)		U354-3	= UFOA		U355-3 = UFOA	A	
SD(1)		U354-4	= AP48		U355-4 = AP48		
SD(2)		U354-7	= U93A		U355-7 = U93A	Λ.	
SD(3)		U354-8	= P070		U355-8 = P070		
SD(4)		U354-1	3 = 834A		U355-13 = 834A	A	
SD(5)		U354-14	4 = 8A16		U355-14 = 8A1	6	
SD(6)		U354-1'	7 = 1UUO		U355-17 = 1UU	JO	
SD(7)		U354-1	8 = H083		U355-18 = H08	3	
RCK_LOW		U354-1	l = UP15				
RCK_HI					U354-11 = 355I	F	
OE		U354-1	= 8986			U3	351-12 = 8986
OE					U355-1 = 51AH	I U3	355-11 = 51AH
Q1		U354-2	= 6P1A		U355-2 = 6P1A	T I I	350-4 = 6P1A
Q2		U354-5			U355-5 = A989		350-5 = A989
Q3		U354-6			U355-6 = 486A		350-6 = 486A
Q4		U354-9			U355-9 = FH57		350-7 = FH57
Q5			2 = U1AC		U355-12 = U1A		350-10 = U1AC
Q6			5 = 8HF6		U355-15 = 8HF		850-10 = 8HF6
Q7			6 = CCU8		U355-16 = CCU		350-11 = GHG 350-12 = CCU8
Q8			$\theta = 50P3$		U355-19 = 50P3		$350 \cdot 12 = 6000$ $350 \cdot 13 = 50$ P3
U349-1,5,8,16	U350-1		U352-2,4,			= 0000 pulsing	
U349-12,13	U351-10,1		U352-3,7,	,15	U353-6,8 = H	82C pulsing	
U349-2 = FU49		U351-1					
U349-3 = 98H4		U351-2					
U349-4 = 746A		U351-3					
U349-6 = H82C		U351-9					
U349-7 = H8HI	1		4 = P9H3				
U349-9 = 0000	17	U351-13	5 = H82C				
U349-11 = C1H		11252 1	11020				
U349-14 = H82	_		= H82C				
U349-15 = FU4			= H82C				
U349-17 = 40U			= 00U6				
U349-18 = 0000) = H8HH				
U349-19 = C1H	1 /		1 = H82C 3 = H82C				
U350-2 = H82C	3						
U350-3 = P9H3		U353-1	= 4OUU				
U350-9 = H82C		U353-2	= H82C				
U350-14 = FU4	.9	U353-3	= C1H7				
U350-15 = FU4	.9	U353-4	= H82C				
		U353-10	O = H82C				
		U353-12	2 = H82C				
		U353-13	3 = 4OUU				

Table 3-13. Readback, Slew Rate, Analog Switch Signature Analysis (Secondary)

Description: These signatures check the readback DAC U322, slew rate decoder U345, and analog switch U346. The signatures are valid for U301 firmware versions "Rev A.02.01". Use the test setup described in "Test Setup for S.A.".

Sign	otu	roc
SIED	aıu	res

Signatures:			
+ 15V - 15V	U322-20	XX2.47.4.20	U346-13 U346-4
+5V Common + 12VREF	U322-1,3,10,12 U322-8	U345-1,20 U345-10	U346-12 U346-5
SD(0) SD(1) SD(2) SD(3) SD(4) SD(5) SD(6) SD(7)	U322-7= UFOA U322-6 = AP48 U322-5 = U93A U322-4 = P070 U322-16 = 834A U322-15 = 8A16 U322-14 = 1UUO U322-13 = H083		
WR1/WR2 B1/B2/XFER	U322-2,18 = P9HA U322-17, 19 = HCA7		
SDB(0) SDB(1) SDB(2) SDB(3) SDB(4) SDB(5) SDB(6) SDB(7)		U345-3 = F592 U345-4 = F3P2 U345-7 = 4461 U345-8 = 5UA2 U345-13 = H82C U345-14 = H82C U345-17 = 6AOC U345-18 = H82C	
SLW1 SLW2 SLW3 SLW4		U345-2 = OU8C U345-5 = 1187 U345-6 = 7P88 U345-9 = 8PCU	U346-8 = OU8C U346-9 = 1187 U346-16 = 7P88 U346-1 = 8PCU
CLK TOGGLE		U345-11 - CCF9 U345-16 - 98H4	

Table 3-14. Chip Select, Status Readback, EEPROM Decoder Signature Analysis (Secondary)

Description: These signatures check the chip select IC U304, the status readback IC U303. The signatures are valid for U301 firmware revisions "Rev A.02.01". Use the test setup described in the "Test Setup for SA".

Signatures:

+5V Common	U303-16 U303 = 8		U304-6,16 U304-5-8
SD(0) SD(1) SD(2) SD(3)	U303-10 = UFOA U303-13 = AP48 U303-9 = U93A U303-1 = P070	S0 S1 S2	U304-1 = 24A7 U304-2 = A264 U304-3 = OUPA
LCLR UNREG BO OV OP STAT_EN	U303-4,6,12,14 = P921 U303-11 = H82C U303-3 = H82C U303-7 = H82C U303-15 = H82C U303-5 = HH1A	CS0 CS1 CS2 CS3 CS4 CS5 RCK_LOW RCK_HI STB	U304-15 = 57A2 U304-14 = 1UPU U304-13 = CCF9 U304 12 = P9HA U304-11 = 4OH3 U304-10 = 9457 U304-9 = UP15 U304-7 = 355F U304-4 = HHC8

DAC Circuits Troubleshooting (Figure 3-3)

These circuits generate the SLEW signal which controls the input power stages. This analog signal is produced by the combined outputs from the main DAC/amplifier (U320/U326) and the transient DAC/amplifier (U321/U325). The DACs/amplifiers convert the data on bus lines SDB0-7 into analog signals.

The HIGH signal (active LO) from the transient generator (see Figure 3-7) closes switch U309 causing the output of the transient/DAC amplifier to be combined with the output from the main DAC/amplifier. The resulting SLEW signal is sent to the input power control circuit via inverting amplifier U324 and the slew circuits (see Figure 3-4).

The SLEW signal is also read back to microprocessor U301 via comparator U327. Readback DAC/amplifier U322/U328 converts the data on bus lines SD0-7 into a reference signal that allows the microprocessor to successively approximate the value of the SLEW signal. The SLEW readback signal is used during selftest to determine if the DACs are operating properly.

To troubleshoot the DAC circuits, place the Electronic Load in the SA mode by connecting the jumpers in test headers TP201 and TP301 in the SA mode positions (see Figure 3-2). The waveforms shown in Figure 3-3 can only be generated when the SA mode is on.

First, check that the SA waveforms shown on Figure 3-3 are correct. If these waveforms are not correct, check the SD0-7 data bus lines to the readback DAC U322 using SA Tables 3-10 and 3-13. Next, check the SDB0-7 data lines to the main (U320) and transient (U321) DACs using SA Table 3-9. If there is a problem on the data lines, SA should isolate the problem to the faulty component.

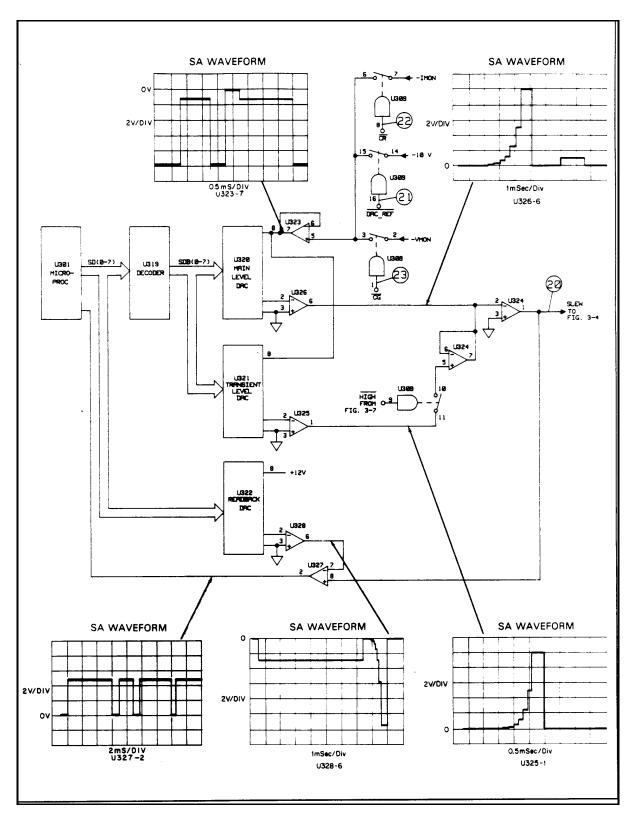


Figure 3-3. DAC Circuits Troubleshooting

If the unit has failed selftest by reporting an error 105-108 at turn-on and no problem can be found using SA, the IMON adjustment may be at fault. Refer to "POST REPAIR CALIBRATION" and perform the IMON Adjustment.

Also, check if the switches in U309 are operating properly. Turn off the SA mode by removing the jumpers. Now check test points (21), (22) and (23) using the measurement conditions specified in Table 3-3. A switch should close when the applicable test point is a Low level. If the switches are operating properly, check test points (45) (-IMON), (25) (-10V), and (32) (-VMON)

If all signatures and test points check out, the DAC or amplifier that is generating the incorrect waveform is probably faulty.

Slew Circuit Troubleshooting (Figure 3-4)

This circuit consists primarily of three operational amplifier stages (U306 and U307) and four analog switches (U346). The four switches determine the slew rate by selecting loop gain and response time combinations. The switches are controlled by the SLW1-SLW4 signals to provide 12 slew rates.

To troubleshoot the slew circuit, place the Electronic Load in the SA mode by connecting the jumpers in test headers TP201 and TP301 in the SA mode positions (see Figure 3-2). The SA waveforms at the top of Figure 3-4 can only be generated when the SA mode is on. If the SA waveforms are incorrect, check the SDB0-7 data inputs to U305 and the SLW signal outputs from U305 using SA Table 3-13. If the signatures are correct, an amplifier or switch is probably defective.

The waveforms at the bottom of Figure 3-4 are generated when various slew rates are programmed. These waveforms check the operation of the slew circuit switches (U317). They are not generated in the SA mode. To generate these waveforms, turn the SA mode off (remove jumpers) and program 3 different slew rates (.001, 0.5 and 2.5 A/ μ s) from the front panel as shown in the following sequence. Use a scope with delayed sweep to verify the waveforms shown for slew rate in Figure 3-4.

```
MODE = CURR

CURR = 5

Tran Level = 10

Freq = 80

Dcycle = 50

Tran on/off = on

Slew = .001 (Slew Rate #1) | 60502A

Slew = .5 (Slew Rate #9) | only

Slew = 2.5 (Slew Rate #11) |
```

The three slew rates programmed from the front panel toggle all four switches in the slew circuit. Refer to the following table if you need to check the state of the switches for a specific slew rate. Remember that the front panel is programmed in microseconds. Note that when the SLW signal is LO, the switch it closed; when the SLW signal is HI, the switch is open. If the slew rate tests check out, and a problem still exists, troubleshoot the CC/CV control circuits as described in the next section.

SLEW RATE SWITCH SETTINGS Refer to Module Operating Manual for Slew Rate Steps

Slew Rate	SLW1	SLW2	SLW3	SLW4
#1	HI	HI	LO	HI
#2	HI	LO	LO	HI
#3	LO	HI	LO	HI
#4	HI	HI	HI	HI
#5	HI	LO	HI	HI
#6	LO	HI	HI	HI
#7	HI	HI	LO	LO
#8	HI	LO	LO	LO

HI

HI

LO

HI

LO

HI

HI

HI

LO

LO

LO

LO

CC/CV CONTROL CIRCUIT TROUBLESHOOTING (Figure 3-5)

#9

#10

#11

#12

Depending upon which operating mode (and range in the CR mode) is selected, either the CC or the CV loop controls the conduction of the input power stages. If the CC or CR (middle and high ranges only) mode is selected, the CC in Signal goes low connecting the SLEW signal to the CC control circuit (U308, U16). If the CV or CR (low range only) mode is selected, the CV in Signal goes low connecting the SLEW signal to the CV control circuit (U308, U13).

LO

НІ

HI

LO

The overvoltage (OV) circuit (U17, D17) is also shown on Figure 3-5. When an OV condition is detected, the OV circuit generates a negative signal on the PROG signal line via diode D17, which causes the input power stages to increase current flow to attempt to limit input voltage. R64 and D18 latch the OV circuit on. When activated, the OV circuit overrides the CC and CV control circuits.

Normally, the output of U17-7 is held high by the positive bias on input U17-5. This bias is controlled by the output of inverting amplifier U17-1, the output of which varies from 0 to -10 volts as the voltage at the input terminals varies from zero to the rated input voltage. When the voltage at the input terminals exceeds the load's rated input, the output of U17-1 pulls input U17-5 less positive until U17-5 is less positive than U17-6. This causes the output of U17-7 to go low, generating the negative signal on the PROG line.

To troubleshoot the CV or CC circuits, place the Electronic Load in the SA mode by connecting the jumpers in test headers TP201 and TP301 in the SA mode positions (see Figure 3-2). The waveforms shown in Figure 3-5 can only be generated when SA mode is on. If the waveforms are correct but a problem exists, troubleshoot the input power stages as described in the next section.

If the waveforms are incorrect, turn off the SA mode (remove jumpers) and check that the CC and CV switches in U340 are operating properly. If the \overline{CC} EN or \overline{CV} EN input is LO, the applicable switch should be closed. You can use SA Table 3-10 to check the \overline{CC} EN, or \overline{CV} EN signals. Next, check test points 27 through 31 using the measurement conditions specified in Table 3-3. Also, check test points 32 (-VMON), 45 (-IMON), and 26 (+12V ref).

If both the CC and CV control loops have problems, there may be another circuit affecting the CC and CV circuits. Troubleshoot the input power stages, current limit, and power limit circuits as described in subsequent sections.

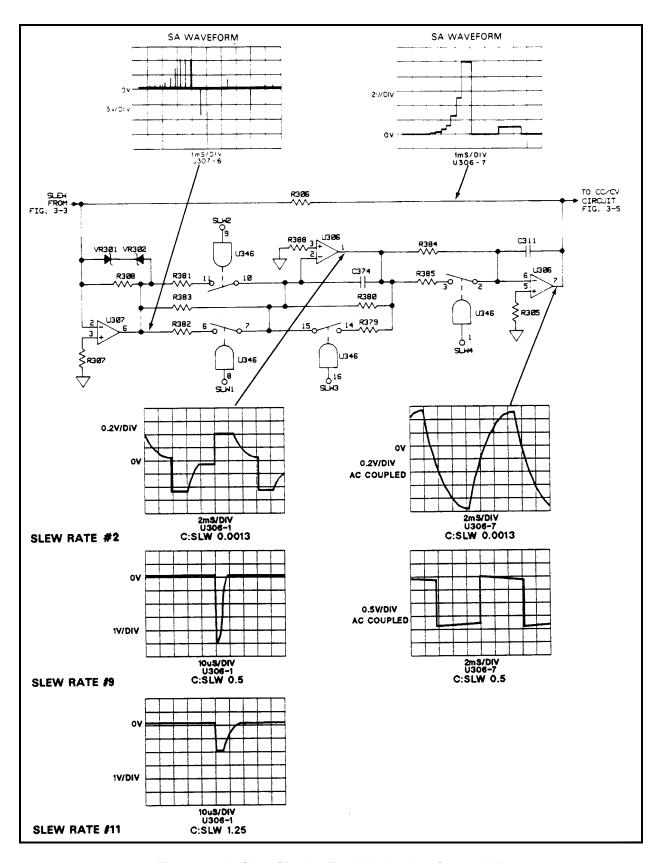


Figure 3-4A. Slew Circuits Troubleshooting for 60501B

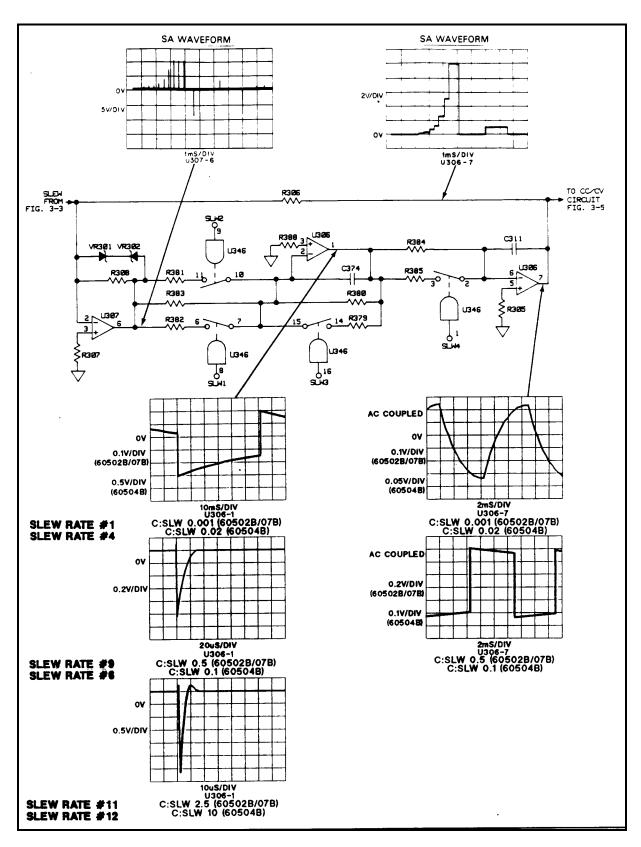


Figure 3-4B. Slew Circuits Troubleshooting for 60502B/04B/07B

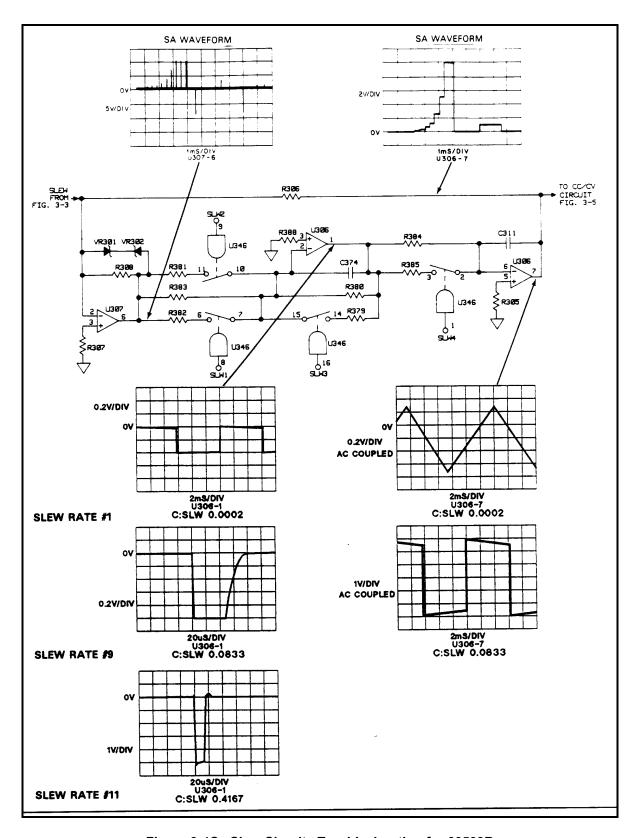


Figure 3-4C. Slew Circuits Troubleshooting for 60503B

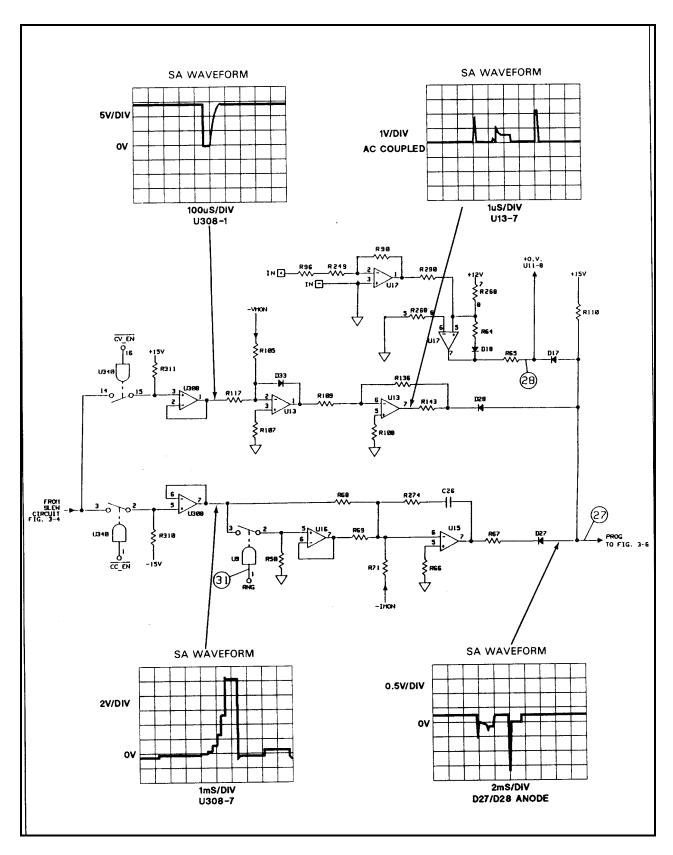


Figure 3-5. CC/CV Control Circuits Troubleshooting

Input Power Stages Troubleshooting (Figure 3-6)

There are four, eight or sixteen identical input power stages (depending on the module) connected in parallel. Figure 3-6 shows one, which consists primarily of a power FET (in quad array Q2), a monitor amplifier (U6) and an error amplifier (U5). Schematic details are shown in the corresponding module Power Board schematics.

To troubleshoot the input power circuits, place the Electronic Load in the SA mode by connecting the jumpers in test headers TP201 and TP301 in the SA mode positions (see Figure 3-2). The waveform shown in Figure 3-6 at the output of the error amplifier can only be generated in the SA mode. Check that this waveform appears at the output of the error amplifier in each input power stage. Refer to the Power Board schematic to locate the output pin of each error amplifier. Checking each stage may isolate the problem to a specific stage.

If the problem is isolated to a specific stage, turn the SA mode off (remove jumpers) and check the test points (41) through that correspond with applicable circuit points in the defective stage. Use the measurement conditions specified in Table 3-3. Also, check the applicable fuses in the specific stage. As shown in Figure 3-6, fuses F5 and F13 are used by stage Q2D.

If all stages have a problem, check test points ② and ⑤ (see Table 3-3). Also, check voltage suppressor (VR28) and diode (D56) which are connected across the + and - INPUT) terminals. Make sure that SENSE switch S1 on the rear panel is set to the LCL position if remote sensing is not being used.

Transient Generator Troubleshooting (Figure 3-7)

The transient generator (U349-U355) allows the input power stages to switch between two load levels. It produces the HIGH control signal which is sent to the DAC circuits to switch the transient DAC output.

Troubleshooting the transient circuit consists of performing the general troubleshooting procedures if the transient circuit will not perform any functions, or performing the frequency or toggle/pulse mode troubleshooting if there is a problem in those areas.

General Troubleshooting

First, check the data bus and internal clock. Use signature analysis to check the SD 0-7 data lines at U354 and U355 (see Table 3-10). Check for the presence of the 1MHz clock signal at U349-1, U350-1, U351-13, and U352-4, 12 (see Figure 3-7).

Next, perform the front panel actions indicated in the Checkout table using a scope and logic probe to monitor the results. Make sure that the unit is at the factory default setting of 1000Hz, 50% duty cycle.

Transient Generator Frequency

If the transient generator will not change frequency, press [TRAN ON] on the front panel and program the transient frequencies according to the FSEL table. Check FSEL inputs at U351-1,2,3 with a logic probe. Check the $1\mu s$ pulse intervals at U350-14, and U351-14 with a scope.

FSEL TABLE

Front Panel	FS	EL INPUT	S	interval between 1µs pulses		
Frequency	0	1	2	@U350-14	@U351-14	
10000Hz	LO	LO	LO	LO	50µs	
1000Hz	HI	LO	LO	10μs	500μs	
100Hz	LO	HI	LO	100μs	5ms	
10Hz	HI	HI	LO	1ms	50ms	
1Hz	LO	LO	HI	10ms	500ms	

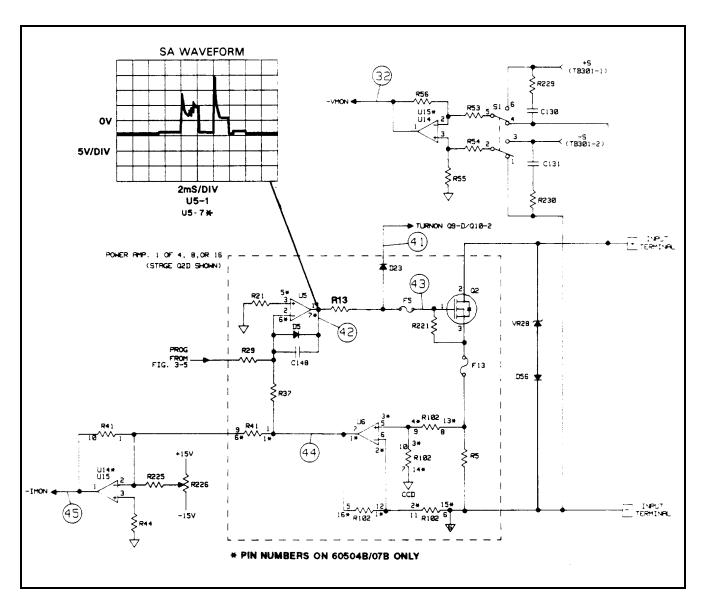


Figure 3-6. Input power Stages Troubleshooting

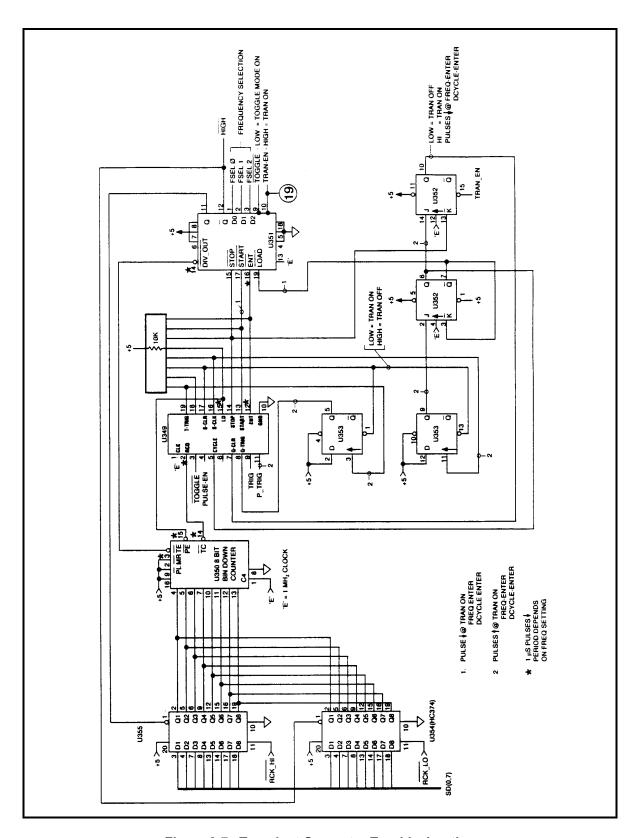


Figure 3-7. Transient Generator Troubleshooting

Toggle or Pulse Modes

To check the transient generator in toggle and pulse modes, run the following program:

10 LOOP

20 OUTPUT 705;"TRAN ON;:TRAN:MODE TOGG"

30 DISP "TRAN:MODE TOGG"

40 PAUSE

50 OUTPUT 705;"TRAN:MODE PULS"

60 DISP "TRAN:MODE PULS"

70 PAUSE

80 END LOOP

90 END

During the pauses, use a logic probe to make the following checks:

Toggle Mode	Pulse Mode
U349-3 = LO	U349-4 = HI
U350-3 = LO	U349-14 = toggling
U351-9, 11, 14 = LO	U352-13 = toggling
U351-12 = HI	

After the pause, press "Continue" to generate the next trigger.

CHECKOUT TABLE

				RES	SULT				
FRONT		use scope	e			use logic	probe		
FRONT PANEL ACTION	TRANS_EN signal	U351- 11,12	U349- 2,12,15	U350- 3	U349- 7	U349- 17	U349-5,8, 11,16,19	U351- 17,19	
Turn on unit	TTL Lo	11=LO 12=Hi	Negative pulse every 0.5ms	Negative pulse every 0.01ms	TTL Lo	TTL Hi			
Press TRAN ON	TTL Hi	1KHz sq. wave	Negative pulse every 0.5ms	Negative pulse every 10µs	TTL Hi	TTL Lo	Positive pulse when TRAN ON pressed.	Negative pulse when TRAN ON pressed.	
Press FREQ 100 ENTER	TTL Hi	1KHz sq. wave	Negative pulse every 5ms	Negative pulse every 100µs	Negative pulse when FREQ and ENTER pressed.	Positive pulse when FREQ and ENTER pressed.	Positive pulse when FREQ and ENTER pressed.	Negative pulse when FREO and ENTER pressed.	
Press TRAN OFF	TTL Lo	11=LO 12=Hi	Negative pulse every 5ms	Negative pulse every 100µs	TTL Lo	TTL Hi			

Trigger Circuit Troubleshooting (Figure 3-8)

The Multiple Electronic Load can be triggered over the HPIB using the GET function, the *TRIG common command, or the TRIG subsystem HPSL command. The TRIG subsystem lets you select either the ac line frequency, internal timer, or TRIG command as the trigger source. There is also an external TRIGGER input on the mainframe for external trigger inputs.

Troubleshooting the trigger circuit consists of sending commands or running programs that generate signal pulses in the direction indicated in the following discussion (also refer to Figure 3-8). If a signal does not toggle where indicated, the IC or gate that generates that signal is probably defective.

AC Line Triggers

First use an oscilloscope to check that the waveforms at U243-14 and Q211-11 are correct.

If the waveform is correct, send string "TRIG:SOUR LINE" and check the GPIB board as follows:

U208-9 (LSNK_EN) goes high U247-11 (TRIG) U219-13 (TRIG_OUT) U215-11 (PRI_TRIG) U219-10

toggle at line frequency

On the module Control board, check that:

U318 pins 1,2,3,9,10,11,13, all toggle at the line frequency.

Note:

An ac line frequency of 60Hz produces a trigger period of 16.67ms; 50Hz produce a trigger period of 20ms.

Internal Timer Triggers

Send the string "TRIG:SOUR TIM" and check the GPIB board as follows:

U228-12 (TRIG_EN) goes high U207-6 goes low U219-9 becomes active U215-11 (PRI_TRIG) pulses @ 1ms intervals

Note:

On the module Control board, observe that U318 pins 1,2,3,9,10,11,13, also pulse at 1ms intervals.

Next send the string "TRIG:TIM 1" or "TRIG:SOUR TIM;:TRIG:TIM 1" and check that PRI_TRIG (U215-11) pulses low at 1ms intervals.

Level Triggers (*TRG and TRIG command)

The following program continuously toggles all labeled signal lines in Figure 3-8 in the indicated direction.

10 LOOP 20 OUTPUT 705;"CURR:LEV;TRIG 5" 30 OUTPUT 705;"TRIG:SOUR BUS" 40 OUTPUT 705;"*TRG" 50 OUTPUT 705;"CURR 1" 60 END LOOP 70 END

The next program does essentially the same thing as the previous one except it lets you manually step through the program to toggle the signal lines. Press [Continue] after each pause to continue the program.

```
10 OUTPUT 705; "CURR:LEV;TRIG 5"
20 OUTPUT 705; "TRIG:SOUR BUS" !TOGGLE ON RUN
30 PAUSE
40 OUTPUT 705; "*TRG" !TOGGLE ON TRG
50 PAUSE
60 OUTPUT 705; "CURR 1" !TOGGLE ON LEV
70 END
```

Note that READ_TRIG (U210-11) is high at power on. When stepping through the program, READ_TRIG goes low at line 30 and high again at line 10, RESET_TRIG (U208-2) is also high at power on and goes low in 10µs pulse intervals. This signal is easier to see using the first program.

Group Enable Trigger (GET function)

Note that P_TRIG (U208-12) is used via firmware to generate Bus triggers. GET_EN (U208-5) is always true and is NOT used to generate triggers.

When running the following program, observe that P_TRIG (U208-12) pulses high, and PRI_TRIG (U215-11) toggles low.

```
10 OUTPUT 705;"TRIG:SOUR BUS"
20 LOOP
30 OUTPUT 705;"*TRG"
40 WAIT .1
50 END LOOP
60 END
```

External Triggers

To generate external triggers for this circuit, send the string "TRIG:SOUR EXT" and observe that U207-10, U247-3, and U215-11 pulse whenever TRIG IN is shorted to common (short TB201-1 to TB201-4).

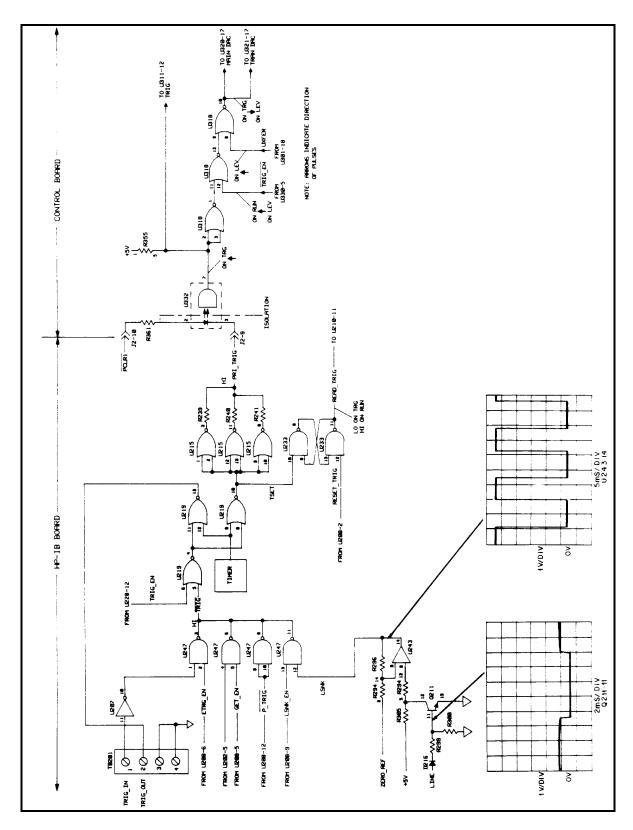


Figure 3-8. Trigger Circuit Troubleshooting

Overcurrent Circuit Troubleshooting (Figure 3-9)

This circuit limits the maximum current the load can sink for different input voltages and/or power conditions. The primary components in this circuit are amplifier U5 (U12 in 60504B/07B) and transistors Q11 and Q12.

At power on the secondary power clear (SPCLR) signal provides a High level via D35 to drive U5 (U12 in 60504B/07B) low, turning Q11 on. With Q11 on, PROG goes high (less negative) and turns off the input power FETs.

When the input voltage is about 6.3V (9V on 60507B; 40V on 60503B) or lower, D33 is forward biased, causing voltage divider R214, R213, R59, and R58 to hold U5 (U12 in 60504B/07B) at approximately - 7V. This clamps the maximum input current capability between

30A and 33A for 60501B.

45A and 66A for 60502B.

10A and 11A for 60503B.

102A and 133A for 60504B.

46A and 53A for 60507B.

As the input voltage increases from 63V to 65V (9V to 155V on 60507B; 40V to 260V on 60503B), D53 is reverse biased and the input voltage will appear across the voltage divider. This causes the voltage at U5 (U12 in 60504B and 60507B) to decrease from - 7 volts to - 0.8V. At an input of 65V (155V on 60507B; 260V on 60503B), D54 turns on and holds U5 (U12 on 60504B and 60507B) at - 0 8V volts and limits the maximum input current capability to less than 5A for 60501B.

9A for 60502B.

2A for 60503B.

2A 101 00303D

15A for 60504B.

8.5A for 60507B.

When the input voltage reaches 75V (170V on 60507B; 287V on 60503B), the OV circuit goes to -13V and pulls PROG low (more negative) via D17. The input power stages will now attempt to sink more current and decrease the input voltage. If the combination of input voltage and current (power) is greater than the power stages can sink when OV condition occurs, the overpower circuit will override the OV circuit and limit the maximum current capability of the load.

The -15Vx bias voltage is a delayed bias derived from the normal -15V supply. When the load is first turned on, -15Vx is not present and U5-6 (U12 on 60504B and 60507B) is at common potential. This causes Q11 to conduct pulling IPROG high. Q12 is also on, connecting Q11 to the + 15V bias. When -15Vx comes on, Q12 turns off causing U5-6 (U12 on 60504B and 60507B) to go more negative than U5-5 (U12 on 60504B and 60507B). This turns off Q11, allowing PROG to go negative. VR27 supplies Q11 collector current once -15Vx is available.

To troubleshoot the current limit circuit, check test points ②, ③ , ③ and ④ using the measurement conditions and readings specified in Table 3-3.

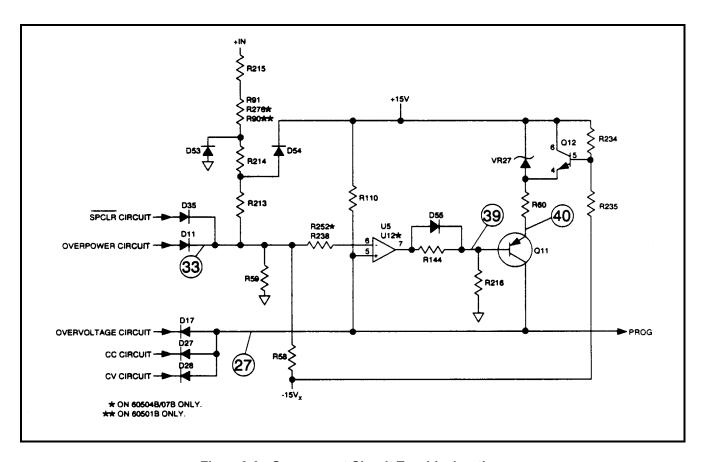


Figure 3-9. Overcurrent Circuit Troubleshooting

Overpower Circuit Troubleshooting (Figure 3-10)

This circuit limits the power sinking capability of the load to either one to two minutes or 50 milliseconds, depending on the temperature of the heatsink assembly

The circuit monitors the input voltage and current to determine if an overpower condition exists. The circuit consists of amplifier U17, the four comparators U10, and summing resistor pack R142. Signal levels representing the input voltage and current are summed with the + 12V reference voltage via resistors to determine if an overpower condition exists. The signal levels are scaled to allow different combinations of voltage and current to be compared (e.g. high voltage/low current; high current/low voltage; etc). If the load is operating in overpower and the EPU bit is alse, the load may operate in overpower for up to two minutes until the EPU bit goes true. If EPU is true, the load will only operate in the overpower state for 50 milliseconds before going to power shutdown. The EPU bit (bit 9) setting is dependent on the temperature of the heatsink assembly.

To check the status of the EPU bit, send the string "STAT:CHAN:COND?".

When the overpower circuit is active, limiting input power capability, the comparator circuit becomes a relaxation oscillator and its output voltage at test point will go between -14 volts and 0V (see waveform on Figure 3-10).

Troubleshooting the power limit circuit consists of checking test points (34), (35), and (45) using the measurement conditions and readings specified in Table 3-3. Also check the +12V reference, the U10 comparator, resistor pack R142 and temperature monitor circuit RT2, U327.

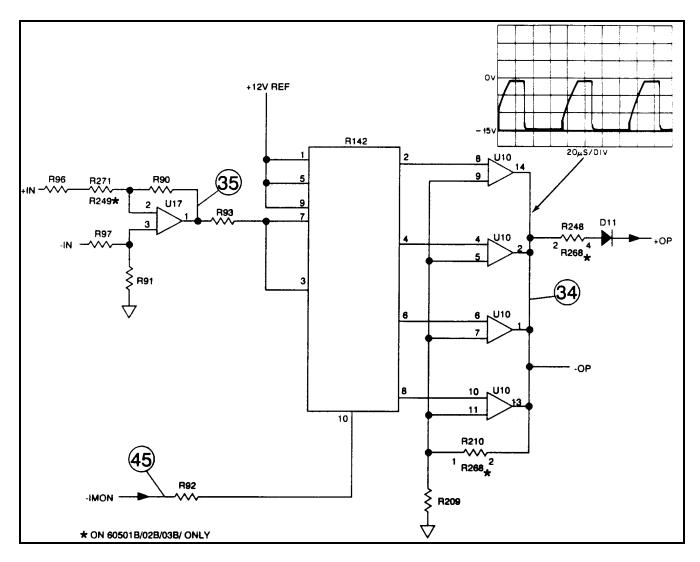


Figure 3-10. Overpower Circuit Troubleshooting

Fan Speed Control Troubleshooting (Figure 3-11)

WARNING

Use extreme caution when troubleshooting the GPIB board when it is removed from the mainframe while connected to AC line voltage. AC line voltage is present throughout the fan speed control circuit located on the lower third of the board. Although removed from the mainframe, the GPIB board must remain connected to the transformer cable, the fan cable, and the line switch cable. The safety interlock switch must also be engaged.

Figure 3-11 is the main troubleshooting tool if the fans are not running or if they do not change speed. Note that a Agilent 6050A mainframe with three or fewer single-width modules installed will not turn fan #2 on. Fan #2 is turned on only when there are four or more single-width modules installed.

If the fans are not running, or if they continually run at top speed, remove the GPIB board from the mainframe and use an oscilloscope to check the waveforms in Figure 3-11. Start with the waveform at the fan and work back to the control circuits to locate the defective part. The waveform at U243-1 is the normal power-on waveform.

WARNING

Checking the waveform across U242 pins 4-6 involves circuits that are connected to the ac mains. To lessen the danger of personal injury, the mainframe should be connected to the ac mains through an isolation transformer when checking the fan supply. When checking all other waveforms, connect the oscilloscope common to one of the common points shown in the figure.

If the fans do not change speed, use the following chart to troubleshoot the fan speed circuit. The individual inputs for U245 and U233 can be controlled using the fan command from the front panel keypad by pressing the **shift** key, then **9**, and then entering a value that corresponds to the bit you want to toggle. Press **Enter** to enter the value.

For example, pressing **shift**, **9**, **2**, **5**, **6**, **Enter** will toggle the Fan 2 OFF bit (256). Although there are fifteen discrete speeds for each fan, distinguishing a speed change between two adjacent numbers is difficult. The chart only provides three examples to program the fans off, slow, or fast.

Check if the bit indicated on the chart is high (1) or low (0) at the following pins:

Fan2 Speed 0 = U233-4.5

Fan2 Speed 1 = U245-3

Fan2 Speed 2 = U245-5

Fan2 Speed 3 = U245-11

Fan1 Speed 0 = U233-1,2

Fan1 Speed 1 = U245-13

 $Fan1_Speed\ 2 = U245-9$

Fan1 Speed 3 = U245-1

Fan2 OFF = U209-16

Note:

The automatic fan speed control circuit varies the speed of the fans based on the temperature of the module heatsinks. Programming the fans from the front panel disables the automatic fan speed control. You must cycle ac power to re-enable the automatic fan speed control.

	50/60	Fan2			Fa	n2				Fa	.n2		Re	esult
	Hz	OFF	Speed	3,	2,	1,	0	Speed	3,	2,	1,	0	Fan 1	Fan 2
Decimal	512	256		128	64	32	16		8	4	2	1		
Value														
768	1	1		0	0	0	0		0	0	0	0	slow	off
512	1	0		0	0	0	0		0	0	0	0	slow	slow
767	1	0		1	1	1	1		1	1	1	1	fast	fast

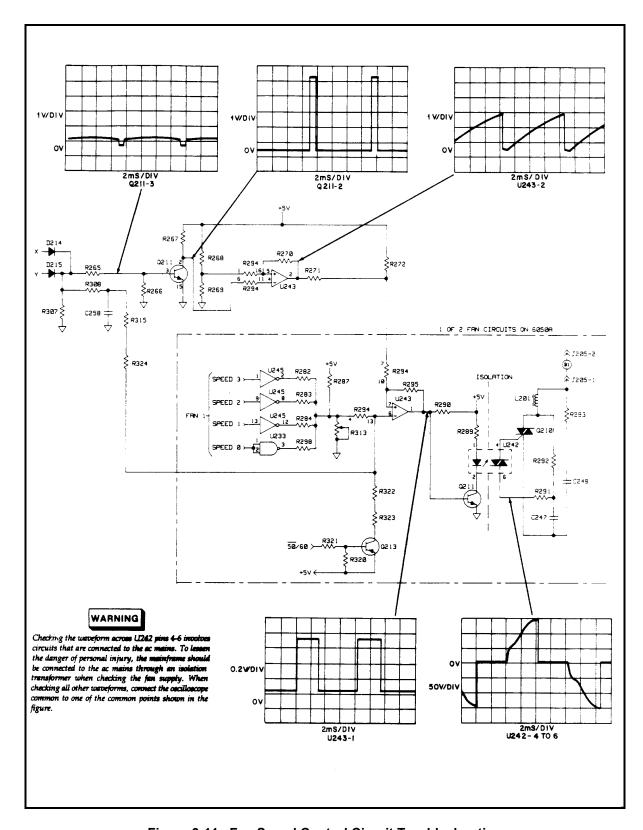


Figure 3-11. Fan Speed Control Circuit Troubleshooting

Post Repair Calibration

Calibration is required annually and whenever certain components are replaced. If certain control board components (U13-16, U306-308, U320-326, U329) are replaced, the Electronic Load module must be recalibrated as described in the Operating Manual.

If any input power stage component is replaced, the Current Monitor (IMON) circuit must be recalibrated. The IMON adjustment procedure is as follows:

- a. Turn load off. Disconnect any connections to the input terminals. Remove top cover.
- b. Connect DMM between the IMON adjustment test points J2-1 and J2-3 as shown on the Power Board Component Locations Diagram in the Module Service Manual.
- c. Turn Electronic Load on and adjust R226 (see the component location diagram) for a reading of 0 ± 0.5 millivolts on the DMM.

If the serial EEPROM chip U211 on the mainframe or U342 on the module is replaced, the Electronic Load must be initialized first and then recalibrated.

EEPROM Initialization

":DIAG:CAL:PRIM 0,6050"

Serial EEPROM chip U211 on the GPIB board stores the Electronic Load's GPIB address and model number as well as other constants. The load was initialized (the EEPROM programmed) with the proper constants before the load was shipped from the factory. If the GPIB board assembly or the EEPROM chip (U211) is replaced, the load must be reinitialized with the proper constants by programming the following commands in the order indicated. After it has been initialized, the Electronic Load must be recalibrated as described in of the Operating Manual. Module initialization is discussed in the appropriate module Service Manual.

! model number

! turn calibration mode on

6050A "·CAL 1

! model number suffix and GPIB address 5 ":DIAG:CAL:PRIM 1,16645" ":DIAG:CAL:PRIM 21,0" ! initial *SRE value ":DIAG:CAL:PRIM 22,0" ! initial *ESE value ":DIAG:CAL:PRIM 23,1" ! initial *PSC value "*RST" ! reset factory default state "*SAV 0 ! to location 0 6051A ":CAL 1" ! turn calibration mode on ":DIAG:CAL:PRIM 0,6051" ! model number ":DIAG:CAL:PRIM 1,16645 ! model number suffix and GPIB address 5 ":DIAG:CAL:PRIM 21,0" ! initial *SRE value ":DIAG:CAL:PRIM 22,0" ! initial *ESE value ":DIAG:CAL:PRIM 23,1" ! initial *PSC value "*RST" ! reset factory default state "*SAV 0" ! to location 0

Principles Of Operation

Introduction

Figure 4-1 is a block diagram illustrating the major circuits and signals within the Electronic Load. Each block on the diagram identifies the schematic diagram sheet where the circuits are shown in detail. Schematic diagrams for the mainframe, consisting mainly of the GPIB Board, are on foldout pages at the end of this manual. Schematic diagrams for the Control Board and Power Board are provided with the Service Manuals for the individual load modules. Note that the block diagram provided in this manual and described in this chapter covers both the mainframe and load module.

The block diagram shows many of the major signals between blocks, but most of the control signals to and from the microprocessors are not shown. Multiple signal lines are sometimes combined into one for clarity. For example, the outputs of the OV, OP, and UNREG Status Comparators are shown on a single line.

The electronic load is functionally divided into three assemblies, the GPIB Board (which is part of the mainframe), and the Control Board and Power Board (which are part of each module). The block diagram and this description are similarly divided.

At the end of this chapter is a description of how the mainframe identifies data sent to and from each module.

Bias Supplies

The electronic load contains two Bias Supplies. One is on the GPIB Board, and supplies bias for the primary microprocessor and other circuits referenced to chassis common. The other is on the Control Board, and supplies voltages for the secondary microprocessor and other circuits referenced to the--input. Both Bias Supplies generate clear signals that are used to ensure proper start-up when the unit is turned on.

GPIB Board Circuits

Circuits on the mainframe GPIB Board provide the interface between the electronic load and the user, generate trigger signals, and control fan speed. The GPIB Interface is the link between the electronic load and the system controller. Almost all communication between the electronic load and the controller is processed by the primary microprocessor, except that Group Execute Trigger (GET) goes directly from the GPIB Interface to the Trigger-Source Select circuits.

The Primary Microprocessor interprets commands from the GPIB or from the front-panel keypad to control the load's input current. The Primary Microprocessor also processes measurement and status data received from the input circuits via the Secondary Microprocessor. This data may be read back to the controller over the GPIB and/or displayed on the unit's front-panel display.

The Primary Microprocessor circuits contain an EEPROM (electrically erasable programmable memory), which stores the load's GPIB address, model number, and other information. The EEPROM is non-volatile, allowing it to retain stored information after power is turned off and back on.

The Trigger-Source Select circuit selects one of four trigger-source signals to be applied to the Trigger Generator. LSNK is

the ac line-synchronization signal derived from the Bias Supply circuits. TRIG_IN is derived from the external trigger signal connected to the rear panel. GET is received directly from the GPIB. P_TRIG* is generated in the primary microprocessor from either the *TRG or TRIG commands received via the GPIB. The Trigger Generator circuit includes the internal timer, which generates trigger signals from the clock (E) and frequency select (FSEL) signals. The Trigger Generator selects between TRIG* and the timer signal to produce the PRI_TRIG signal, which is sent to the modules. A trigger signal is also supplied to the rear-panel TRIGGER OUT connector for use with external equipment.

The Fan Supply And Speed Control circuit varies the fan speed as required to provide adequate cooling for the number of modules installed and the power to be dissipated, while minimizing noise.

The Load Modules Interface circuit connects the selected module to the SER_OUT and SER_IN ports of the primary microprocessor. This circuit also informs the microprocessor how many modules are installed in the mainframe. A further description is provided at the end of this chapter.

Control Board Circuits

Signals between the mainframe GPIB Board and the module Control Board are connected via ribbon cables across the top edges of each board to optocouplers on the Control Board. These optocouplers, and the transformer in the Secondary Bias Supply, provide isolation between the chassis-ground referenced circuits in the mainframe and the circuits in the load modules, each of which is referenced to its own - Input.

The Secondary Microprocessor associated with each module controls the operation of the module. It translates the serial data received from the Primary Microprocessor into a parallel data bus and other control signals. Values are loaded into the Main DAC, Transient DAC, Transient Generator, and Readback DAC via the data bus. The Secondary Microprocessor circuits contain an EEPROM which stores the module's min/max values, ranges, and other information, as well as calibration constants.

The DAC Reference Select circuit enables one voltage - IMON*, VMON*, or -10V_REF to be the VREF supplied to the Main DAC and Transient DAC. Which reference is used depends on the operating mode and range.

Transient operation causes the input power stages to switch between two load levels. The Transient Generator uses the frequency select (FSEL) and clock (E) signals from the microprocessor to generate the timing signal, HIGH*, which opens and closes the solid-state switch in the output of the Transient DAC circuit. The outputs of the Main DAC, the Transient DAC, and the EXT PROG signal from the rear-panel connector are summed to produce SLEW.

In transient operation, SLEW has a step change from the main value to the transient value and back again, at a frequency controlled by the Transient Generator. RC networks in the Slew Rate Control circuit integrate the step changes in accordance with the programmed slew rate to allow a controlled transition from one load setting to another.

Solid-state switches in the output of the Slew Rate Control circuit determine if the programming signal becomes CV_PROG or CC_PROG.

Also located on the Control Board are the Readback DAC and Readback Comparators. Input voltage, input current, and heatsink temperature are read by successive approximation. The Readback DAC and comparator also return a test signal to the microprocessor during selftest to determine if the DAC circuits are operating properly.

The input voltage and current monitor signals, VMON and IMON, are buffered and connected to the rear-panel terminal strip.

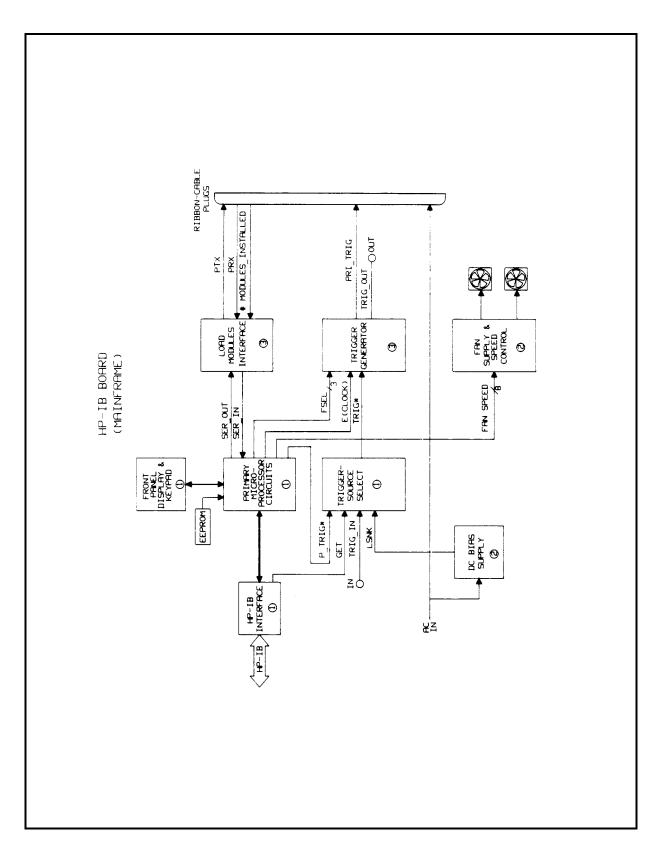


Figure 4-1. Block Diagram (Sheet 1 of 3)

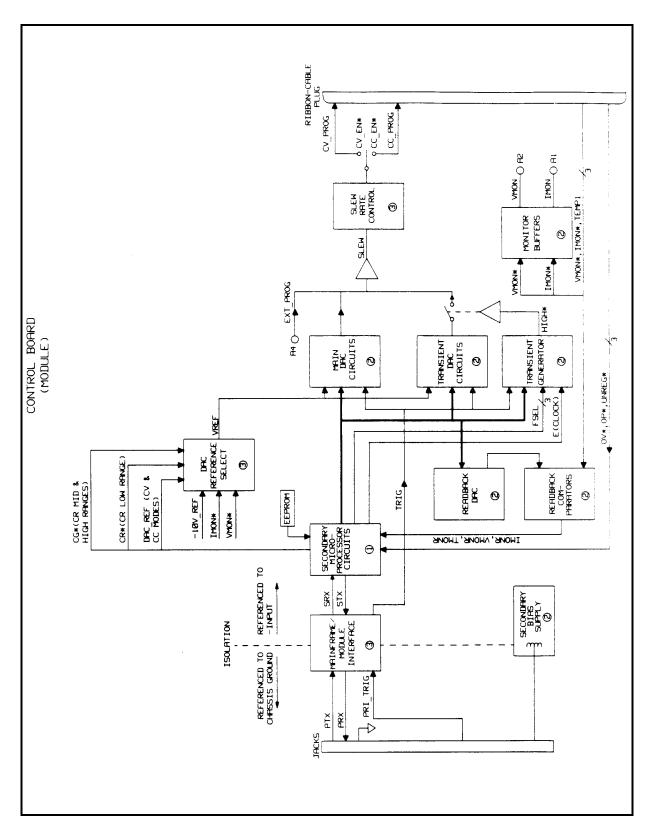


Figure 4-1. Block Diagram (Sheet 2 of 3)

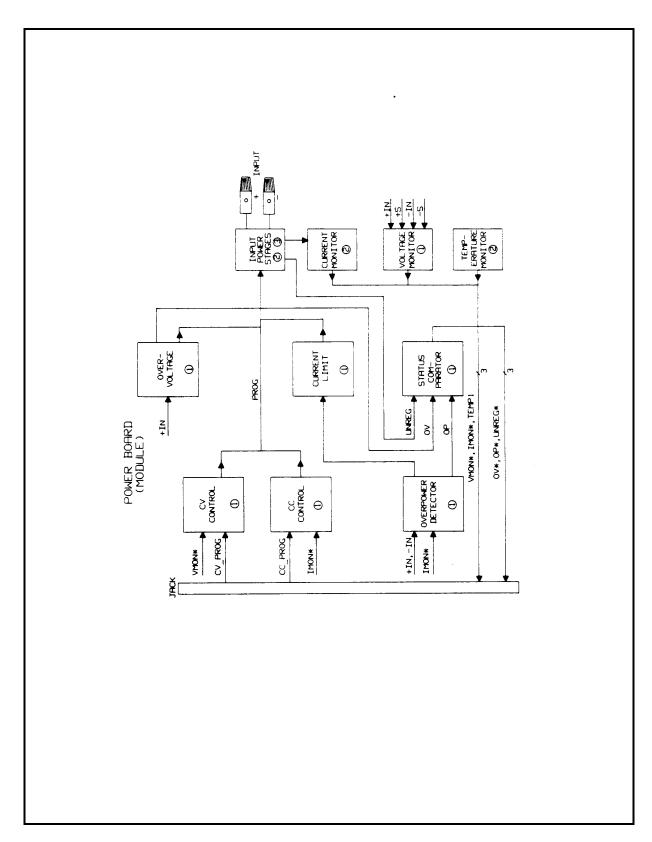


Figure 4-1. Block Diagram (Sheet 3 of 3)

Power Board Circuits

The CV Control circuit compares CV_PROG, which represents what the input voltage should be, to VMON*, which represents what the input voltage actually is. Similarly, the CC Control circuit compares CC_PROG to IMON*. Either the CV Control circuit or CC Control circuit, depending on the operating mode and range, generates the programming signal, PROG, that controls the conduction of the Input Power Stages. The Overvoltage and Current Limit circuits can also control PROG in case of an overvoltage or overpower condition.

The Overvoltage circuit takes control of the input power stages if an overvoltage condition occurs. The Overvoltage circuit controls PROG to cause the input stages to increase current flow to limit the input voltage. The OV circuit does not turn off the input power stages.

The Current Limit circuit limits the load's input current to a value within its rating. The value is set slightly above the current rating of the module. The circuit is also activated to limit input current when an overpower condition occurs, and at turn on.

The Overpower Detector circuit monitors the input voltage and input current to determine if an overpower condition exists. In the event the load begins to operate beyond the power limit boundary, the Overpower Detector turns on the Current Limit circuit, which overrides the PROG output of either the CV Control or CC Control circuit to limit the load's input current. Once the power has been returned to a safe operating area, the circuit allows the current to rise again.

There are either four, eight, or sixteen Input Power Stages connected in parallel. Each stage consists mainly of a power FET, error amplifier, and an input current monitor amplifier. Each FET is connected across the load's + and - Input terminals with a fuse and current monitoring resistor. The error amplifier in each stage compares the PROG signal from the CV or CC Control circuits to the actual value of input current to produce an error signal which controls the conduction of each FET to maintain the voltage or current at the input terminals at the programmed value.

In CC mode, the Input Power Stages will sink a current in accordance with the programmed value of current, regardless of the input voltage. In CR mode, the Input Power Stages will sink a current linearly proportional to the input voltage in accordance with the programmed resistance value. In CV mode, the Input Power Stages will attempt to sink enough current to control the source voltage to the programmed voltage level.

The Input Power Stages also generate UNREG if the FETs are not regulating the input power.

The Status Comparators inform the microprocessor if there is an overvoltage, overpower, or unregulated condition. The Current, Voltage, and Temperature Monitor circuits return IMON*, VMON*, and TEMP1 signals to the microprocessor.

Module/Mainframe Communication

Figure 4-2 shows how the primary microprocessor on the mainframe GPIB Board determines how many modules are installed in the mainframe. (Connections of interest are shown by heavier lines.) The modules are daisychained together, with plug P2 on a module mated to jack J2 on the next lower-numbered module. P2 on the slot 1 module mates to J2 on the mainframe GPIB Board. Pin P2-6 on each module is grounded.

Therefore, a module installed in slot 1 will cause pin J2-6 on the GPIB Board to be grounded, a module installed in slot 2 will cause pin J2-5 on the GPIB Board to be grounded, etc.

Note that dual-width modules are seen by the mainframe as a single module. The serial data ports on connectors J3/P3 are similarly daisychained.

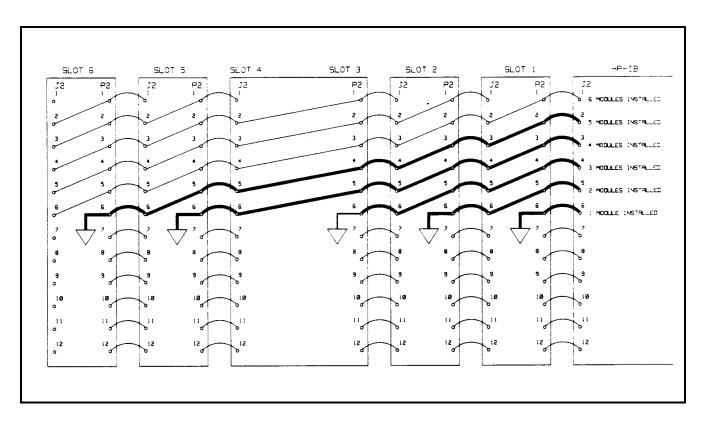


Figure 4-2. Module/Mainframe Communication

Replaceable Parts

Introduction

Table 5-4 lists the electrical components and Table 5-5 lists the mechanical components for the Agilent 6050A/6051A Electronic Load Mainframes. These tables provide the following information:

- Reference designation (see Table 5-1)
- Agilent part number
- Description of part (see Table 5-2)
- Manufacturer's Federal Supply Code number (see Table 5-3 for manufacturer's name and address)
- Manufacturer's part number

Refer to Figure 5-1 and 5-2 for component locations.

How To Order Parts

You can order parts from your local Agilent Technologies sales office. (Refer to the list at the end of this manual for the office nearest you.) When ordering parts, include the following information:

- Agilent part number
- Description of the part
- Quantity desired
- Electronic Load model number (Agilent 6050A)

If the part is not manufactured by Agilent Technologies and the manufacturer's part number is listed, you may order it directly from them. Locate the manufacturer's Federal Supply Code and refer to Table 5-3.

Table 5-1. Reference Designators

A	Assembly	RTB	Removable Terminal Block
В	Blower	RTP	Removable Jumper
C	Capacitor	S	Switch
D	Diode	T	Transformer
F	Fuse	TB	Terminal Block
J	Terminal Jack	TP	Test Pin
MP	Mechanical Part	U	Integrated Circuit
P	Terminal Plug	VR	Voltage Regulator
Q	Transistor	W	Cable Assembly
RT	Thermal Resistor	Y	Oscillator

Table 5-2. Part Description Abbreviations

AL	Aluminum	PE	Polyester	
CC	Carbon Composition	PD	Power Dissipation	
CER	Ceramic	PP	Polypropylene	
DIP	Dual In-line Package	PWR	Power	
DPDT	Double Pole Double Throw	RECT	Rectifier	
FF	Flip-Flop	SIP	Single In-line Package	
FXD	Fixed	TA	Tantalum	
GEN-PURP	General Purpose	TC	Temperature Coefficient	
IC	Integrated Circuit	TF	Thin Film	
MACH	Machine	W/	With	
MO	Metal Oxide			

Table 5-3. Federal Supply Codes

Code	Manufacturer	City & State
00779	AMP Inc.	Harrisburg, PA
07716	I R C Division of TRW	Burlington, IA
01121	Allen Bradley Company	Milwaukee, WI
01295	Texas Instruments Inc.	Dallas, TX
03888	Pyrofilm Resistor Co. Inc.	Whippany, NJ
04713	Motorola Semiconductor Products	Phoenix, AZ
07263	Fairchild Semiconductor Corp.	Hicksville, NY
11236	CTS of Berne Inc.	Berne, IN
11502	I R C Division of TRW	Boone, NC
14433	ITT Semiconductors	W. Palm Beach, FL
15801	Fanwell Electronics Inc.	Framingham, MA
16299	Corning Glass Works	Raleigh, NC
17856	Siliconix Inc.	Santa Clara, CA
18873	Dupont E I DE Nemours and Co.	Wilmington, DE
19701	Mepco/Electro Corp.	Mineral Wells, TX
20432	Podlin Co.	Franklin Park, IL
24546	Corning Glass Works	Bradford, PA
26742	Methode Electronics Inc.	Chicago, IL
27014	National Semiconductor Corp.	Santa Clara, CA
27167	Corning Glass Works	Wilmington, NC
27264	Molex Products Inc.	Downers Grove, IL
28480	Hewlett-Packard Co.	Palo Alto, CA
34649	Intel Corp.	Mountain View, CA
56289	Sprague Electric Co.	North Adams, MA
71468	ITT Cannon Electric	Santa Ana, CA
72799	General Electric Co.	Pittsfield, MA
75915	Littlefuse Inc.	Des Plaines, IL
91637	Dale Electric Inc.	Columbus, NE
96733	San Fernando Electric Mfg. Co.	San Fernando, CA

Table 5-4. Agilent 6050A/6051A Parts List - Electrical

Ref.	HP		Mfr.	Mfr
Desig.	Part No.	Description	Code	Part No.
A3	5063-3440	GPIB BOARD ASSEMBLY	28480	
C201	0160-5422	CAPACITOR-FXD .047µF ±20% 50Vdc CER	16299	
C202	0160-4808	CAPACITOR-FXD 470pF ±5% 100Vdc CER 0±30	16299	
C203	0180-3798	CAPACITOR-FXD 4700μF +30 -10% 25Vdc AL	56289	
C205,206	0160-4787	CAPACITOR-FXD 22pF ±5% 100Vdc CER 0±30	16299	
C207-211	0160-5422	CAPACITOR-FXD .047µF ±20% 50Vdc CER	16299	
C214,215	0160-5422	CAPACITOR-FXD .047µF ±20% 50Vdc CER	16299	
C223	0160-4835	CAPACITOR-FXD .1μF ±10% 50Vdc CER	16299	
C224,225	0160-4439	CAPACITOR-FXD 4700pF ±20% 250Vac METAL	28480	
C226	0160-4413	CAPACITOR-FXD .6μF ±10% 250Vac METAL	28480	
C230-232	0160-5422	CAPACITOR-FXD .047µF ±20% 50Vdc CER	16299	
C233,234	0180-0374	CAPACITOR-FXD 10µF ±10% 20Vdc TA	56289	150D106X9020B2
C235,236	0160-5422	CAPACITOR-FXD .047µF ±20% 50Vdc CER	16299	
C237	0160-4787	CAPACITOR-FXD 22pF ±5% 100Vdc CER 0+30	16299	
C238	0180-0376	CAPACITOR-FXD .47μF ±10% 35Vdc TA	56289	150D474X9035A2
C239	0160-5098	CAPACJTOR-FXD .22μF ±10% 50Vdc CER	16299	CAC05X7R224J050A
C241	0160-5422	CAPACITOR-FXD .047µF ±20% 50Vdc CER	16299	
C242	0160-4835	CAPACITOR-FXD .1µF ±10~o 50Vdc CER	16299	
C243	0160-4463	CAPACITOR-FXD .lµF ±1% 50Vdc METAL-PE	28480	
C244	0160-4835	CAPACITOR-FXD .lµF ±10% 50Vdc CER	16299	
C245	0160-4065	CAPACITOR-FXD .lµF ±20% 250Vac METAL	28480	
C246	0160-4259	CAPACITOR-FXD .22µF ±10% 250Vac METAL	28480	
C247	0160-4065	CAPACITOR-FXD .1µF ±20% 250Vac METAL	28480	
C248	0160-4259	CAPACITOR-FXD .22µF ±10% 250Vac METAL	28480	
C249-257	0160-5422	CAPACITOR-FXD .047μF +20% 50Vdc CER	16299	
C258	0180-0291	CAPACITOR-FXD 1047µI +20% 35Vdc TA	56289	150D105X9035A2
C259	0160-4835	CAPACITOR-FXD .1µF±10% 50Vdc CER	16299	130010377033712
C261, 263	0160-5422	CAPACITOR-FXD .047µF ±20% 50Vdc CER	16299	
C201, 203	0160-3422	CAPACITOR-FXD .01µF ±10% 50Vdc CER	10299	
D202	1901-0033	DIODE-GEN PURP 180V 200mA IN645	28480	
D202 D204	1901-0033	DIODE-GEN PURP 180V 200mA IN645	28480	
D204 D205-208	1901-0055	DIODE-PWR RECT 400V 1A 200NS IN4936	28480	
D203-200	1901-1005	DIODE-PWR RECT 400V 1A 200Ns 1N4936	28480	
D213-216	1901-0033	DIODE-GEN PURP 180V 200mA IN645	28480	
F201	2110-0010	FUSE (INCH) 5A 250V	75915	312 005
F202,203	2110-0820	FUSE (METRIC) .5A 250V	28480	312 000
J1-3	1252-2789	CONNECTOR-POST RT ANGLE 12-CONTACT	27264	26-58-6121
J201	1252-0268	CONNECTOR GPIB 24-CONTACT	18873	68519-001
J202,203	1252-0034	CONNECTOR-POST 16-CONTACT	18873	66506-044
J204	1252-3771	CONNECTOR-AC POWER	82389	EAC303
J205	1252-0056	CONNECTOR-POST 4-CONTACT	27264	09-74-1041
J206,207	1251-8512	CONNECTOR-POST 5-CONTACT	27264	09-74-1051
J208	1252-1152	CONNECTOR-POST 10-CONTACT	76381	3591-6022
J209	1252-0056	CONNECTOR-POST 4-CONTACT	27264	09-74-1041
J210	1252-0055	CONNECTOR-POST 2-CONTACT	27264	09-74-1021

Table 5-4. Agilent 6050A/6051A Parts List - Electrical (continued)

Ref.	HP		Mfr.	Mfr
Desig.	Part No.	Description	Code	Part No.
L200,201	06050-80002	CHOKE, RFI	28480	
Q201	1858-0054	TRANSISTOR ARRAY 16-PIN DIP	72799	
Q207	1853-0059	TRANSISTOR PNP 2N5876 SI TO-3 PD=150W	04713	
Q208	1853-0036	TRANSISTOR PNP SI PD=310mW	04713	
Q209,210	1884-0331	THYRISTOR-TRIAC TO-220AB	04713	
Q211	1858-0023	TRANSISTOR ARRAY 16-PIN DIP	72799	
Q212,213	1853-0036	TRANSISTOR PNP SI PD=310mW	04713	
R201	1810-0560	NETWORK-RES 16-PIN DIP 5.6K OHM X 8	28480	
R202	0698-3359	RESISTOR 12.7K 1% .125W TF TC=0±100	24546	CT4-1/8-T0-1272-F
R203,204	8159-0005	RESISTOR-ZERO OHMS 22 AWG LEAD DIA	72982	
R205	0757-0442	RESISTOR 10K 1% .125W TF TC=0±100	24546	CT4-1/8-T0-1002-F
R208	0698-3631	RESISTOR 330 5% 2W MO TC=0±200	11502	
R214	1810-0280	NETWORK-RES 10-SIP 10.0K OHM X 9	91637	MSP10A01
R215	0698-3644	RESISTOR 5.1K 5% 2W MO TC=0±200	27167	FP42-2-T00-5101-J
R228	1810-0280	NETWORK-RES 10-SIP 10.0K OHM X 9	91637	MSP10A01
R236	1810-0278	NETWORK-RES 10-SIP 3.3K OHM X 9	91637	
R237	1810-0207	NETWORK-RES 8-SIP 22.0K OHM X 7 1236	28480	
R238-241	0757-0394	RESISTOR 51.1 1% .125W TF TC=0 ±100	24546	CT4-1/8-T0-51RI-F
R242,243	0757-0442	RESISTOR 10K 1% .125W TF TC=0±100	24546	CT4-1/8-T0-1002-F
R244	0683-1055	RESISTOR 1M 5% .25W CF TC=0-800	01121	CB1055
R245	0757-0442	RESISTOR 10K 1% .125W TF TC=0±100	24546	CT4-1/8-T0-1002-F
R246	0757-0316	RESISTOR 42.2 1% .125W TF TC=0±100	07716	
R247	0757-0436	RESISTOR 4.32K 1% .125W TF TC=0±100	24546	CT4-1/8-T0-4321-F
R248	0698-3441	RESISTOR 215 1% .125W TF TC=0±100	24546	CT4-1/8-T0-215R-F
R249	0698-6322	RESISTOR 4K .1% .125W TF TC=0±25	91637	
R250	0757-0472	RESISTOR 200K 1% .125W TF TC=0±100	24546	CT4-1/8-T0-2003-F
R251	0757-0280	RESISTOR 1K 1% .125W TF TC=0±100	24546	CT4-1/8-T0-1001-F
R252	0757-0472	RESISTOR 200K 1% .125W TF TC=0±100	24546	CT4-1/8-T0-2003-F
R253	0698-8827	RESISTOR 1M 1% .125W TF TC=0±100	19701	
R254	0757-0394	RESISTOR 51.1 1% .125W TF TC=0 ±100	24546	CT4-1/8-T0-51RI-F
R255	0699-1797	RESISTOR 10M 5%		
R256	0757-0438	RESISTOR 5.11K 1% .125W TF TC=0±100	24546	CT4-1/8-T0-5111-F
R257	0757-0420	RESISTOR 750 1% .125W TF TC=0±100	24546	CT4-1/8-T0-751-F
R258	0698-0084	RESISTOR 2.15K 1% .125W TF TC=0±100	24546	CT4-1/8-T0-21.;1-F
R259	0757-0472	RESISTOR 200K 1% .125W TF TC=0±100	24546	CT4-1/8-T0-2003-F
R260	0698-0084	RESISTOR 2.15K 1% .125W TF TC=0±100	24546	CT4-1/8-T0-2151-F
R261	0757-0438	RESISTOR 5.11K 1% .125W TF TC=0±100	24546	CT4-1/8-T0-5111-F
R262	0757-0436	RESISTOR 4.32K 1% .125W TF TC=0±100	24546	CT4-1/8-T0-4321-F
R263	0698-3644	RESISTOR 5.1K 5% 2W MO TC=0±200	27167	FP42-2-T00-5101-J
R264-266	0757-0442	RESISTOR 10K 1% .125W TF TC=0±100	24546	CT4-1/8-T0-1002-F
R267,268	0757-1093	RESISTOR 3K 1% .125W TF TC=0±100	24546	CT4-1/8-T0-3001-F
R269	0757-0280	RESISTOR 1K 1% .125W TF TC=0±100	24546	CT4-1/8-T0-1001-F
R270	0698-8827	RESISTOR 1M 1% .125W TF TC=0±100	19701	
R271	0757-0280	RESISTOR 1K 1% .125W TF TC=0±100	24546	CT4-1/8-T0-1001-F
R272	0698-6358	RESISTOR 100K .1% .125W TF TC=0±25	07716	
R273	0698-8827	RESISTOR 1M 1% .125W TF TC=0±100	19701	
R274	0757-1093	RESISTOR 3K 1% .125W TF TC=0±100	24546	CT4-1/8-T0-3001-F
R275	0757-0407	RESISTOR 200 1% .125W TF TC=0±100	24546	CT4-1/8-T0-201-F

Table 5-4. Agilent 6050A/6051A Parts List - Electrical (continued)

Ref.	HP		Mfr.	Mfr
Desig.	Part No.	Description	Code	Part No.
R276	0683-1815	RESISTOR 180 5% .25W CF TC=0-400	01121	CB1815
R277	0764-0025	RESISTOR 2K 5% 2W MO TC=0±200	11502	
R278	0757-0198	RESISTOR 100 1% .5W TF TC=0±100	19701	
R280	0757-0427	RESISTOR 1.5K 1% .125W TF TC=0±100	24546	CT4-1/8-T0-1501-F
R281	0698-5808	RESISTOR 4K 1% .125W TF TC =0±100	24546	CT4-1/8-T0-4001-F
R282	0757-0407	RESISTOR 200 1% .125W TF TC=0±100	24546	CT4-1/8-T0-201-F
R283	0757-1093	RESISTOR 3K 1% .125W TF TC=0±100	24546	CT4-1/8-T0-3001-F
R284	0757-0439	RESISTOR 6.81K 1% .125W TF TC=0±100	24546	CT4-1/8-T0-6811-F
R285	0757-0442	RESISTOR 10K 1% .125W TF TC=0±100	24546	CT4-1/8-T0-1002-F
R286	0757-0427	RESISTOR 1.33K 1% .125W		
R287	0757-0442	RESISTOR 10K 1% .125W TF TC=0±100	24546	CT4-1/8-T0-1002-F
R288	0757-0317	RESISTOR 1.5K 1% .125W		
R289	0757-1093	RESISTOR 3K 1% .125W TF TC=0±100	24546	CT4-1/8-T0-3001-F
R290	0757-0407	RESISTOR 200 1% .125W TF TC=0±100	24546	CT4-1/8-T0-201-F
R291	0683-1815	RESISTOR 180 5% .25W CF TC=0-400	01121	CB1815
R292	0764-0025	RESISTOR 2K 5% 2W MO TC=0±200	11502	
R293	0757-0198	RESISTOR 100 1% .5W TF TC=0±100	19701	
R294	1810-0319	NETWORK-RES 16-DIP 100.0K OHM X 8	91637	MDP1603-104G
R295,296	0698-8827	RESISTOR 1M 1% .125W TF TC=0±100	19701	
R297	0757-0442	RESISTOR 10K 1% .125W TF TC=0±100	24546	CT4-1/8-T0-1002-F
R298	0757-0446	RESISTOR 15K 1% .125W TF TC=0±100	24546	CT4-1/8-T0-1502-F
R299-304	0757-0442	RESISTOR 10K 1% .125W TF TC=0±100	24546	CT4-1/8-T0-1002-F
R305,306	0757-1093	RESISTOR 3K 1% .125W TF TC=0±100	24546	CT4-1/8-T0-3001-F
R307	0757-0442	RESISTOR 10K 1% .125W TC TC=0±100	24546	CT4-1/8-T0-1002-F
R308	0757-0465	RESISTOR 100K 1% .125W TF TC=0±100	24546	CT4-1/8-T0-1003-F
R309	0757-0407	RESISTOR 200 1% .125W TF TC=0±100	24546	CT4-1/8-T0-201-F
R314,315	0757-0465	RESISTOR 100K 1% .125W TF TC=0±100	24546	CT4-1/8-T0-1003-F
R316	0698-8826	RESISTOR 825K 1% .125W TF TC=0±100	19701	
R317	0757-0458	RESISTOR 51.1K 1% .125W TF TC=0±100	24546	CT4-1/8-T0-5112-F
R318	0698-8959	RESISTOR 619K 1% .125W TF TC=0±100	19701	
R319	0757-0470	RESISTOR 162K 1% .125W TF TC=0±100	24546	CT4-1/8-T0-1623-F
R320,21	0757-0465	RESISTOR 100K 1% .125W TF TC=0±100	24546	CT4-1/8-T0-1003-F
R322	0698-8826	RESISTOR 825K 1% .125W TF TC=0±100	19701	
R323	0757-0462	RESISTOR 75K 1% .125W TF TC=0±100	24546	CT4-1/8-T0-7502-F
R324	0698-8826	RESISTOR 825K 1% .125W TF TC=0±100	19701	
R325	0698-3160	RESISTOR 31.6K 1% .125W TF TC=0±100	24546	CT4-1/8-T0-3162-F
R326	0757-1093	RESISTOR 3K 1% .125W TF TC=0±100	24546	CT4-1/8-T0-3001-F
RT1	8159-0005	RESISTOR-ZERO OHMS 22 AWG LEAD DIA	72982	
RT201	0837-0220	THERMISTOR 10K-OHM TC=-3.83%/C DEG	75263	
RTP201	1258-0209	REMOVABLE JUMPER 2-POSITION (TP201)	28480	
S202-204	3101-2828	LINE SELECT SWITCH DPDT	28480	
S205	3101-3006	SWITCH-INTERLOCK	28480	
TB201	0360-2312	TERMINAL BLOCK 4-CONTACT	28480	

Table 5-4. Agilent 6050A/6051A Parts List - Electrical (continued)

Ref.	HP			Mfr
Desig.	Part No.	Description		Part No.
TP201	1251-4927	CONNECTOR-POST TYPE 16-CONTACT	28480	
U201	1820-6045	IC GPIB TRANSCEIVER	28480	
U202	1821-1740	IC GPIB TALKER/LISTENER	34649	P8291A
U203	1821-3617	IC MICROPROCESSOR CMOS 8-BIT CMOS 1MHZ	S4013	
U204	1820-5978	IC 3-TO-8-LINE DECODER CMOS/74AC	07263	74ACl38PC
U205	06050-80018	IC EPROM AM27512D	28480	
	1200-0567	SOCKET 28-CONTACT (U205)	28480	
U206	1818-3183	IC 64K STATIC RAM CMOS	28480	
U207	1820-2921	IC HEX INVERTER CMOS/74HC	27014	MM74HC04N
U208,209	1820-3399	IC FF CMOS/74HC D-TYPE POS-EDGE-TRIG	04713	MC74HC273N
U210	1820-3297	IC OCTAL BUS DRIVER CMOS/74HC	04713	MC74HC244N
U211	1818-3921	IC 1K EEPROM NMOS	27014	MM74HC04N
U212	1820-4053	IC HEX INVERTER CMOS/74HC	01295	SN74HC05N
U213	1820-3197	IC BIN COUNTER CMOS/74HC NEG-EDGE-TRIG	04713	MC74HC4020N
U214	1820-3176	IC 8-TO-1-LINE MULTIPLEXER CMOS/74HC	27014	MC74HC151N
U215	1820-3298	IC QUAD OR GATE CMOS/74HC 2-INPUT	27014	MC74HC32N
U216	1820-3173	IC FF CMOS/74HC J-K NEG-EDGE-TRIG	27014	MC74HC112N
U217	1820-3098	IC TPL NOR GATE CMOS/74HC 3-INPUT	27014	
U219	1820-2924	IC QUAD NOR GATE CMOS/74HC 2-INPUT	04713	MC74HC02N
U226	1820-4995	IC BIN COUNTER CMOS/74HC POS-EDGE-TRIG	28480	
U227,228	1820-3399	IC FF CMOS/74HC D-TYPE POS-EDGE-TRIG	04713	MC74HC273N
U229	1820-3079	IC 3-TO-8-LINE DECODER CMOS/74HC	04713	MC74HC138N
U230	1820-3176	IC 8-TO-1-LINE MULTIPLEXER CMOS/74HC	27014	MC74HC151N
U233	1820-3183	IC QUAD NAND GATE CMOS/74HC 2-INPUT	04713	
U234	1826-0122	IC REGULATOR-FXD 4.8/5.2V	07263	UA7805UC
U235	1820-5978	IC 3-TO-8-LINE DECODER CMOS/74AC	07263	74AC138PC
U237	1826-1343	IC REGULATOR (REF-ADJ 2.5/36V) 8-PIN DIP	01295	TL431CP
U238	1826-0412	IC DUAL PRECISION COMPARATOR 8-PIN DIP	27014	LM393N
U239	1820-3297	IC OCTAL BUS DRIVER CMOS/74HC	04713	MC74HC244N
U241,242	1990-0845	OPTO-ISOLATOR IF=50MA-MAX	04713	
U243	1826-0138	IC QUAD COMPARATOR 14-PIN DIP	27014	LM339N
U245	1820-4053	IC HEX INVERTER CMOS/74HC	01295	SN74HC05N
U246	1820-3399	IC FF CMOS/74HC D-TYPE POS-EDGE-TRIG	04713	MC74HC273N
U247	1820-3183	IC QUAD NAND GATE CMOS/74HC 2-INPUT	04713	
U248	1820-6170	IC GPIB TRANSCEIVER	28480	
VR1,2	1902-0955	ZENER DIODE 7.5V 5% PD=.4W	07263	
W1	7175-0057	RESISTOR-ZERO OHMS SOLID TINNED COPPER	62223	
W2	06050-60051	GROUND WIRE	28480	
W3	06050-80004	CABLE-INTERLOCK SWITCH	28480	
Y201	0410-1627	RESONATOR-CER 4.0MHZ FREQ TOL: ±0.5%	28480	

Table 5-4. Agilent 6050A/6051A Parts List - Electrical (continued)

Ref.	HP		Mfr.	Mfr
Desig.	Part No.	Description	Code	Part No.
	06050-60002	6050A FRONT PANEL ASSEMBLY	28480	
	06051-60002	6051A FRONT PANEL ASSEMBLY	28480	
A1	5063-2304	LCD DISPLAY	28480	
A2	5020-2713	PC BOARD-KEYPAD	28480	
S1	06060-40001	KEYPAD	28480	
S201	3101-2862	SWITCH-ON/OFF	28480	
W6	06050-80006	CABLE-DISPLAY/KEYBOARD (A1,2 to	28480	
		J202,203)		
W7	06632-80002	CABLE-AC (S201 to J209)	28480	
		CHASSIS	28480	
B1,2	5060-3538	FAN (B2 not used on 6051A)	28480	
D1,2	3000-3338	When replacing fan, refer to Service Note	20400	
		6050A-02 for installation of fan motor hub.		
RTB2	1252-1488	MATING PLUG FOR TB201 (trigger)	28480	
T201	9100-4761	TRANSFORMER	28480	
W4				
6050A	06050-80007	CABLE-FAN (Bl,2 to J205)	28480	
6051A	06051-80003	CABLE-FAN (B1 to J205)	28480	
W5	06050-80010	CABLE-TRANSFORMER (T201 to J206/207)	28480	

Table 5-5. Agilent 6050A/6051A Parts List - Mechanical

Ref Desig.	Ref Desig. Agilent Part Quantity Description		Description
	No.	-	-
A3	5060-3303		GPIB BOARD ASSEMBLY
MP1	2110-0689	4	FUSE CLIP
MP2	2110-0642	1	FUSEHOLDER
MP3	2110-0565	1	FUSEHOLDER CAP
MP4	1205-0561	1	HEAT SINK (Q207)
MP5	2360-0398	2	SCREW-MACH 6-32 (Q207)
MP6	0535-0031	5	NUT-HEX W/LOCKWASHER (J201,204; Q209,210)
MP7	3050-0891	2	WASHER-FLAT (J204)
MP8			
6050A	06050-00008	1	SWITCH BRACKET (S205)
6051A	06051-00012	1	SWITCH BRACKET (S205)
MP9	0515-0886	2	SCREW-MACH M3X0.5 (MP8 to A3)
MP10			
6050A	0515-0886	2	SCREW-MACH M3X0.5 (A3 to MP26)
6051A	0535-1105	2	SCREW-MACH M3X0.5 (A3 to MP26)
			, , ,

Table 5-5. Agilent 6050A/6051A Parts List - Mechanical (continued)

Ref.	HP	Quantity	
Desig.	Part No.	Quantity	Description
Desig.	1 411 1101		FRONT PANEL ASSEMBLY
MP11	5040-5448	1	WINDOW (A1)
MP12	2010 2110	1	WINDOW (III)
6050A	5021-8405	I	FRONT FRAME
6051A	5021-8417	Ĭ	FRONT FRAME
MP13	5021 0117	1	TROTT FIGURE
6050A	06050-00004	I	FRONT SUB-PANEL
6051A	06051-00001	1	FRONT SUB-PANEL
MP14	00021 00001	1	TROTT SCB THIVEE
6050A	06050-00001	1	SCREENED PANEL
6051A	06051-00002	1	SCREENED PANEL
MP15	06051-00002	1	SPACER (S1)
MP6	0535-0031	6	NUT-HEX W/LOCKWASHER (A2 to MP13)
MP10	0535-0031	2	SCREW-MACH M3X0.5 (A1 to MP13)
MP7	3050-0891	8	WASHER (A1,2)
MP17	0515-0896	4	SCREW-MACH M4X0.7 (MP13 to MP12)
MP18	0535-0082	1	NUT-HEX W/LOCKWASHER (MP14 to MP13)
MP19	1400-0611	$\begin{bmatrix} 1 \\ 2 \end{bmatrix}$	CABLE CLAMP (W6) on 6050A only
MP20		$\frac{1}{2}$	SIDE TRIM
MP20 MP21	5001-0540	2	SIDE I KIW
6050A	5041-8802	1	TOP TRIM
6051A	5041-8803	1	TOP TRIM
0031A	3041-8803	1	TOP TRIVI
	06050-00006	1	6050A CHASSIS
	06051-00004	$\begin{bmatrix} 1 \\ 1 \end{bmatrix}$	6051A CHASSIS
	00031-0004	1	0031A CHASSIS
MP22	0380-0644	2	STANDOFF-HEX .255 IN (J201 to chassis)
1411 22	0300-0044	2	Flat washer p/n 3050-0849
MP23	2190-0034	2	LOCKWASHER (J201)
WH 23	2170 0054	1	Flat washer p/n 3050-084
MP24			That washer pin 3030 004
6050A	06050-00013	1	PANEL-RIGHT SIDE
6051A	06051-00007	1	PANEL-RIGHT SIDE
MP25	00031 00007	1	THIVE RIGHT SIDE
6050A	06050-20003	1	PANEL-A3 BOARD
	06051-20008	1	PANEL-A3 BOARD
MP26	00001 20000		THE TO DOTHE
6050A	06050-20007	1	CONNECTOR GUIDE-PLASTIC
6051A	06050-20007	1	CONNECTOR GUIDE-BRACKET
MP27	0535-1105	2	SCREW-MACH M3X0.5 (MP26 to MP25/chassis) on 6051A
1411 2 /	0333-1103		only
MP28	0361-1239	5	RIVET-PLASTIC (MP26 to MP25) on 6050A only
MP29	0380-1705	$\begin{bmatrix} 3 \\ 2 \end{bmatrix}$	STANDOFF-PLASTIC (MF26 to MF25) on 6050A only STANDOFF-PLASTIC 1/4 TURN (A3 to chassis)
MP29 MP30	06050-20001		MODULE SUPPORT PANEL on 6050A only
		1 2	
MP31	06050-20002	3	FAN SUPPORT BRACKET on 6050A only

Table 5-5. Agilent 6050A/6051A Parts List - Mechanical (continued)

Ref.	HP	Quantity	
Desig.	Part No.	Q	Description
MP32			·
6050A	06050-00012	1	SHROUD-FAN
6051A	06051-00006	1	SHROUD-FAN
MP33	1390-0233	6	FASTENER CLIP 1/4-TURN (module to chassis) on 6050 only
		2	FASTENER CLIP 1/4-TURN (module to chassis) on 6051 only
MP34*	0515-2022	3	SCREW-SELF TAP M4-FLH (MP30 to MP31) on 6050A only
MP35*	0515-2023	7	SCREW-SELF TAP M4-FLH (MP30 to MP12; MP30 to chassis)
			on 6050A only
MP36	0515-0216	4	SCREW-MACH M4X0.7 (Bl,2 to MP31,MP32) on 6050A only
		2	SCREW-MACH M4X0.7 (B1 to MP32) on 6051A only
MP23	2190-0856	2	LOCKWASHER (B1) on 6051A only
MP37	0515-1114	6	SCREW-MACH M4X0.7 (MP24 to chassis) on 6051A only
		8	SCREW-MACH M4X0.7 (MP24,MP25 to MP32; MP24 to chassis)
			on 6050A only
MP38	2200-0205	2	SCREW-MACH 4-40 (T201 to chassis)
MP7	3050-0891	2	WASHER-FLAT (T201)
MP17	0515-0896	2	SCREW-MACH M4X0.7 (MP12 to chassis) on 6050A only
MP39	0515-0885	5	SCREW-MACH M4X0.7 (MP12,W2 to chassis) on 6050A only
		16	SCREW-MACH M4X0.7 (MP32 to MP12; MP25 to MP32;
			MP8, MP12, MP32, and W2 to chassis) on 6051A only
MP40	2190-0646	2	LOCKWASHER (W2)
MP41	1400-1281	3	CABLE CLIP (W4,5) on 6050A only
MP19	1400-0611	1	CABLE CLAMP (W6) on 6050A only
		2	CABLE CLAMP (W6) on 6051A only
MP42			·
6050A	06050-00002	1	COVER-TOP
6051A	06051-00003	1	COVER-TOP
MP43	06051-00010	1	COVER-RIGHT SIDE
MP44	06051-00011	1	COVER-LEFT SIDE
MP45	5062-3705	2	STRAP HANDLE
MP46	5041-8819	2	STRAP HANDLE CAP (front)
MP47	5041-8820	2	STRAP HANDLE CAP (rear)
MP48	0515-1132	4	SCREW-MACH M5X0.8 (MP45-47 to chassis)
MP49	06050-80003	1	REAR PANEL LABEL
MP50	5041-8801	4	FOOT
			MISCELLANEOUS
	9211-3251	1	CARTON, SHIPPING for 6050A only
	9211-6308	1	CARTON, SHIPPING for 6051A only
	9220-3172	2	FLOATER for 6050A only
	9222-0456	1	BAG, CUSHION ED for 6051A only
	06050-90001	1	OPERATING MANUAL
	06060-90005	1	PROGRAMMING REFERENCE GUIDE

^{*}Do not reuse the self tapping screws once they have been removed from the support panel or fan brackets. Use screws with regular thread instead.

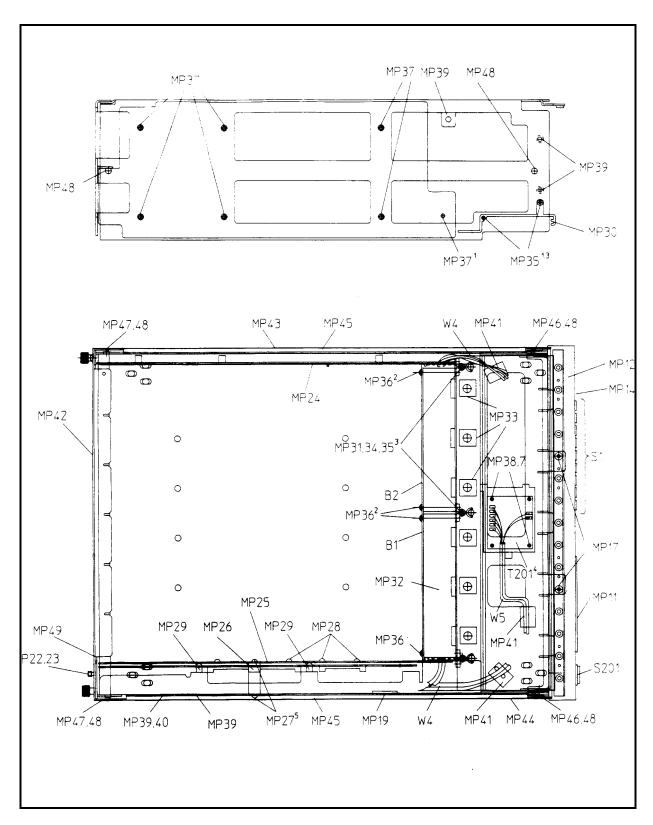


Figure 5-1. Mechanical Parts Locations

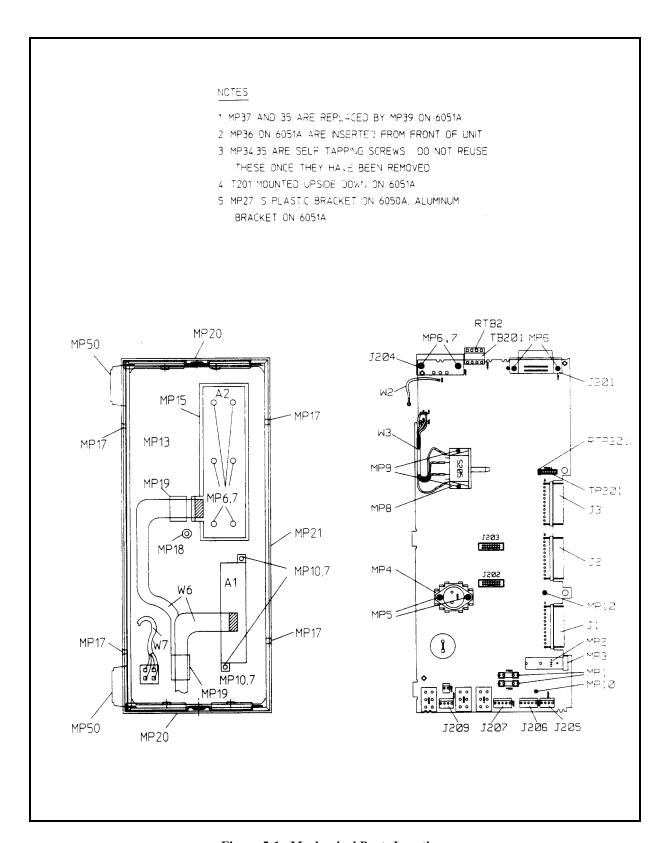


Figure 5-1. Mechanical Parts Locations

Diagrams

Introduction

This chapter contains the test point and component location diagram, schematic diagrams, and related tables useful for maintenance of the electronic load mainframe. Similar information for each model of plug-in load module is provided in the module service manuals. Ordinarily, maintenance is done with both a mainframe and at least one module, so the module service manuals should be available for use with this manual.

Test Point and Component Locations

Figure 6-2 is an assembly drawing of the GPIB Board assembly which shows the location of test points and components on the GPIB Board. The test points are described in Table 3-3, and are used in various troubleshooting procedures provided in Chapter 3.

Figure 6-2 includes a grid by which components can be located on the assembly. Table 6-2 is an alphanumeric listing of each of the electrical components on the GPIB Board assembly. The coordinates listed for each component give the location (to within 1/10 of a unit) for one pin of that component (pin 1 if numbered).

For example, R244 (located near the upper left corner of Figure 6-2) has coordinates listed in Table 6-2 of 1.2 and - 5.0. Looking at Figure 6-2, you can see that one pin of R244 is located on the -5 coordinate, 2/10 of the way between coordinates 1 and 2.

For another example, U227 (located near the center of the board) has coordinates of 6.0 and -3.7. Looking at Figure 6-2, you can see that pin 1 of U227 is located on the 6 coordinate, 7/10 of the way between coordinates - 3 and - 4. Table 5-4 gives the part number and description of each electrical part.

Schematic Diagram

Figure 6-1 shows the connections between the GPIB Board and the front-panel-mounted keypad. Figure 6-3 is the schematic diagram of the Electronic Load mainframe. Notes that apply to all of the schematic sheets are given in Table 6-3. Most of the electrical components are mounted on the GPIB Board, with exceptions noted on the schematic. The Agilent 6050A and 6051A are electrically identical except that the Model 6051A has only one fan. The block diagram description in Chapter 4 provides a general description of circuit operation.

Signal Descriptions

Table 6-1 lists, alphabetically, all the signal names that appear on the schematic, along with a brief description of the signal's function. To help you locate where signals come from and go to, Table 6-1 lists the coordinates for each appearance of a signal on each sheet of the schematic. Coordinates printed in bold indicate the signal origin.

For example, when CAL_LOCK is active it locks out software calibration. CAL_LOCK originates in area 8C of sheet 1, and it also appears in area 4A of sheet 3.

Table 6-1. Signal-Name Descriptions

Mnemonic	Function	Sheet 1	Sheet 2	Sheet 3
	GPIB BOARD			
CAL_LOCK	Software-calibration lockout (D)	8C		4A
CLR	Initialize transient generator (D)			6D
CS2*	GPIB interface read (D)	7C , 6B		
CS3*	GPIB interface write (D)	7C , 6B		
CS4*	Keypad chip select (D)	7C, 3C		
CS5*	Display chip select (D)	7C , 3B		
CS6*	Fan-speed chip select (D)	7C, 3B		
CS7*	Control-signals-latch select bit (D)	8C , 8C, 3C		
CS8*	Trigger-generator-counter latch select bit (D)	8D , 8C		2C
CS9*	Number-of-modules-installed readback select (D)	8D, 8C		3A
CS10*	Control-signals-latch select bit (D)	8D, 3A		JA
CS10*				
	Keypad readback chip select (D)	7C, 3D		0.0
Е	Primary μP clock (D)	4C , 7C, 6C,		8C
EEDONA	EEDD OLG U. 11 (D)	6B	40	
EEPON*	EEPROM power-on disable (D)	2A	2B	
ETRG_EN	External trigger enable/disable (D)	3A , 5A		
FAN1_SPEED0 \		2B	5B	
FAN1_SPEED1		2B	5B	
FAN1_SPEED2		2B	5C	
FAN1 SPEED3		2B	5C	
FAN2 SPEED0	Fan-speed control signals (D)	2B	5C	
FAN2 SPEED1		2B	5C	
FAN2 SPEED2		2B	5C	
FAN2 SPEED3 /		2B	5D	
FAN2_SFEED3 /		2B 2C	2D	
_			2D	0D
FSELO \	T: (D)	2C		8D
FSEL1	Trigger-generator frequency-select bits (D)	2C		8D
FSEL2 /		2C		8D
GET_EN	Group Execute Trigger enable/disable (D)	3A , 5A		
LINE_SENSE	Line-voltage fan-speed compensation (A)		5D,	
			2C, 2B	
LSNK	AC line sync input to trigger circuit (D)	6A	5C	
LSNK_EN	Line sync trigger enable/disable (D)	3A , 6A		
PCLR	Power-on clear to GPIB interface (D)	6A	2A	
PCLR*	Power-on clear to μP and display (D)	1A, 4C	2A	7B
PCLR1*	Power-on clear signal to modules (D)		2B	8B
PRI TRIG	Trigger signal to modules (D)			2C, 8C
PRX1 \				8A , 7A
PRX2				8A , 7A
PRX3	Serial data from modules (D)			8A, 7A
PRX4	Serial data from modules (D)			8B, 7A
· •			1	
PRX5			1	8B, 7A
PRX6				8B , 7A
PRX7 /				7B , 7A

Table 6-1. Signal-Name Descriptions (continued)

PTX2 PTX3 PTX4	Mnemonic	Function	Sheet 1	Sheet 2	Sheet 3
PTX3 Serial data to modules (D) 58, 8A PTX5 FTX6 5B, 8B PTX7 FTX6 5B, 8B PTX7 / FTRIG* Trigger signal from controller (D) 3A, 5B READ_TRIG Indicates to μP that a trigger has occurred (D) 3B, 3D R/W* RAM read/write (D) 4C, 6C RESET_TRIG Resets trigger latch after μP reads it (D) 3A, 4B SA_GATE Primary-μP SA gate (D) 4D, 8C SCO SC, 4C SCO SC, 4C SC1 Module address to serial data port (D) 2C SER_IN Serial data input to μP (D) 4D SER_OUT Serial data output from μP (D) 4D SIOEN* Module I/O enable (D) 2C TRIG_EN Trigger enable/disable (D) 2C TRIG_S Trigger developed from 1-of-4 sources (D) 6A TRIG_OUT Trigger input (D) 2A, 6B TRIG_OUT Trigger input to trigger latch (D) 4A X AC in to line-sense and line-sync circuits 6B, 8C, 5D	PTX1 \				5B , 8A
PTX4 PTX5 PTX6 PTX7 P_TRIG* READ_TRIG RAM read/write (D) RESET_TRIG SA_AMODE SCO \ SCO \ SCI SCI SCI Serial data input to μP (D) SER_IN SER_OUT SIOEN* SER_OUT SIOEN* SER_OUT SIOEN* SIOEN* SIOEN* Trigger enable/disable (D) TRIG_EN Trigger enable/disable (D) TRIG_ST TRIG_ST Trigger output (D) TRIG_OUT Trigger output (D) Trigger output (D) Trigger output (D) TRIG_OUT TRIG_OUT Trigger input to trigger latch (D) X AC supply to Fan 2	PTX2				5B , 8A
PTX4 PTX5 PTX6 PTX7 PTX6 PTX7 PTX6 PTX7 PTX6 PTX7 PTRIG* Indicates to μP that a trigger has occurred (D)	PTX3				5B , 8A
PTX5 5B, 8B PTX6 5B, 8B PTX7 / 5B, 8B P_TRIG* Trigger signal from controller (D) 3A, 5B READ_TRIG Indicates to μP that a trigger has occurred (D) 3B, 3D R/W* RAM read/write (D) 4C, 6C RESET_TRIG Resets trigger latch after μP reads it (D) 3A, 4B SA_GATE Primary-μP SA gate (D) 4D, 8C SA_MODE Primary-μP SA mode enable (D) 8C, 4C SC0 \ 2C 5B SC1 Module address to serial data port (D) 2C 5B SER_IN Serial data input to μP (D) 4D 4A SER_OUT Serial data output from μP (D) 4D 5B SIOEN* Module I/O enable (D) 2C 5B TRIG_EN Trigger enable/disable (D) 2C 5B TRIG_OUT Trigger output (D) 2A, 6B 7A, 5C TRIG_OUT Trigger input to trigger latch (D) 4A 3C X AC in to line-sense and line-sync circuits 6B, 8C, 5D <	PTX4	Serial data to modules (D)			5B , 8B
PTX6 PTX7 / P_TRIG* READ_TRIG READ_TRIG ROW* RESET_TRIG READ_TRIG RESET TRIGGEN RESET_TRIGGEN RAM read/write (D) RAG, 6C SEC SB SB, 7B SB, 7B SB, 3B SB, 7B SB, 3D RAM read/write (D) RAG, 6C SB, 8C SD SD TRIGGEN RESET_TRIGGEN RESET_TRIGGEN RAM read/write (D) RAG, 6C SC SD SA, 5B SB, 7B SB, 3D RAM RAM read/write (D) RAG, 6C SC SB SC TRIGGEN RESET_TRIGGEN RESET_TRIGGEN RAM read/write (D) RAG, 6C SC SB SC SC SD SC SC SD	PTX5				
PTX7 / P_TRIG* READ_TRIG READ_TRIG READ_TRIG RESET_TRIG RESET Primary-μP SA gate (D) RESET_TRIG RESET SET RIG RESET Preads it (D) RESET_AD RESET	PTX6				
P_TRIG* READ_TRIG READ_TRIG READ_TRIG RAM read/write (D) RESET_TRIG RESET_TRIG RESET_TRIG RESET_TRIG RESET_TRIG RESET_TRIG RESET_TRIG RESET_TRIG RESET_TRIG RESET Primary-μP SA gate (D) RESET_DEATE RESET_TRIG RESET Primary-μP SA gate (D) RESET_DEATE RESET_DEATE RESET_TRIG RESET Primary-μP SA gate (D) RESET_DEATE RESET_DEATE RESET_DEATE RESET_TRIG RESET RESET_DEATE					
READ_TRIG R/W* RAM read/write (D) RESET_TRIG RAM read/write (D) RESET_TRIG READ_TRIG RAM read/write (D) RESET_TRIG RESET_TRIG Resets trigger latch after μP reads it (D) RESET_DEAD RAM read/write (D) RESET_DEAD RAM r	•	Trigger signal from controller (D)	3A . 5B		, ,
R/W* RESET_TRIG RESET_TRIG RESETS trigger latch after μP reads it (D) RESET_TRIG RESETS trigger latch after μP reads it (D) RESET_TRIG RESETS trigger latch after μP reads it (D) RESET_OPER SA_MODE SA_MODE Primary-μP SA mode enable (D) RESET_OPER SA_MODE SCO \ SER_IN SER_IN SER_OUT SET SIOEN* TRIG_EN TRIG_EN Trigger enable/disable (D) TRIG* Trigger developed from 1-of-4 sources (D) TRIG_OUT TSET Trigger input to trigger latch (D) Trigger input to trigger latch (D) TRIG_OUT TSET AC supply to Fan 2 RAM read/write (D) AD AC supply to Fan 2 4C, 6C AD, 4A B, 4B AC, 6C AD, 4A BC, 6C AD, 4A BD AC, 6C AD, 4C BD AC, 6C BD AC, 6D	_				
RESET_TRIG SA_GATE SA_GATE Primary-μP SA gate (D) SCO \ SCO \ SCI SC2 / SER_IN SER_OUT SIOEN* TRIG_EN TRIG_EN TRIG_EN TRIG_IN TRIG_OUT TSET XFER_1 \ CASEBRE ACSEBRE A					
SA_GATE SA_MODE SA_MODE SCO \ SCO \ SCI SC2 / SER_IN SER_OUT SIOEN* TRIG_EN TRIG_EN TRIG_ST TRIG_IN TRIG_OUT TRIG_COUT TRIG_COUT Trigger input to to trigger latch (D) Trigger input to trigger latch (D) TRIG_COUT Trigger input to trigger latch (D) Trigger input to trigger latch (D) TRIG_COUT Trigger input to trigger latch (D) Trigger input to trigger latch (D) TRIG_COUT Trigger input to trigger latch (D) Trigger input to t			-		
SA_MODE SCO \ SCO \ SCI			-		
SCO \ SC1 Module address to serial data port (D) SC2 / SC3 SER_IN Serial data input to μP (D) SER_OUT Serial data output from μP (D) SIOEN* Module I/O enable (D) TRIG_EN Trigger enable/disable (D) TRIG_TRIG_IN External trigger input (D) TRIG_OUT Trigger output (D) TRIG_OUT Trigger input to trigger latch (D) X AC in to line-sense and line-sync circuits SB					
SC1 Module address to serial data port (D)2C5BSC2 /2C5BSER_INSerial data input to μP (D)4D4ASER_OUTSerial data output from μP (D)4D5BSIOEN*Module I/O enable (D)2C5BTRIG_ENTrigger enable/disable (D)2C8D, 6CTRIG_INTrigger developed from 1-of-4 sources (D)6A7A, 5CTRIG_INExternal trigger input (D)2A, 6B3BTSETTrigger output (D)2A3BXAC in to line-sense and line-sync circuits6B, 8C, 5DXFER_1 \AC supply to Fan 27C, 1D	_	Timery at orthode endote (D)			5B
SC2 / SER_IN SER_OUT SER_OUT SIOEN* TRIG_EN TRIGG_IN TRIG_OUT TRIG_OUT TRIGG_OUT TRIGG in to line-sense and line-sync circuits Serial data input to μP (D) 4D 4A 4A 4A 4B 4A 4B 4A 4B 4A 4B 4A 4B 4B 4B 4B 4A 4B	•	Module address to serial data port (D)			
SER_INSerial data input to μP (D)4D4ASER_OUTSerial data output from μP (D)4D5BSIOEN*Module I/O enable (D)2C5BTRIG_ENTrigger enable/disable (D)2C8D, 6CTRIG*Trigger developed from 1-of-4 sources (D)6A7A, 5CTRIG_INExternal trigger input (D)2A, 6BTRIG_OUTTrigger output (D)2A3BTSETTrigger input to trigger latch (D)4A3CXAC in to line-sense and line-sync circuits6B, 8C, 5DXFER_1 \AC supply to Fan 27C, 1D	· ·	Module address to serial data port (D)			
SER_OUT SIOEN* SIOEN* Module I/O enable (D) TRIG_EN TRIG_EN Trigger enable/disable (D) TRIG_IN TRIG_OUT TRIG_OU	•	Social data input to UD (D)			
SIOEN* TRIG_EN TRIGG* TRIG_IN TRIGGOUT TSET X AC in to line-sense and line-sync circuits TGEN TRIG_EN Trigger enable/disable (D) TRIGGEN TRIGGEN Trigger enable/disable (D) TRIGGEN TRIGGOUT Trigger input (D) TRIGGOUT Trigger input to trigger latch (D) AC supply to Fan 2 2C 8D, 6C 8D, 6C 7A, 5C AC supply to Fan 2	_				
TRIG_EN TRIG* Trigger enable/disable (D) TRIG* TRIG_IN External trigger input (D) TRIG_OUT TSET X AC in to line-sense and line-sync circuits Trigger enable/disable (D) AC supply to Fan 2 SD, 6C AA AB, 6C AA BD, 6C 7A, 5C AA 3B 3C AB, 8C, 5D 7C, 1D	_				
TRIG* TRIG_IN External trigger input (D) TRIG_OUT TSET X AC in to line-sense and line-sync circuits Trigger developed from 1-of-4 sources (D) External trigger input (D) 2A, 6B 2A, 6B 3B 3C AC supply to Fan 2 AC supply to Fan 2					
TRIG_IN TRIG_OUT TSET TSET TSET T AC in to line-sense and line-sync circuits TRIG_OUT TSET TSET TO AC supply to Fan 2 Trigger input (D) Trigger input (D) Trigger latch (D) AC supply to Fan 2 AC supply to Fan 2 AC 4A AC 5B AC 5D TC, 1D					
TRIG_OUT TSET TSET TRIG_OUT Trigger output (D) Trigger input to trigger latch (D) AC in to line-sense and line-sync circuits AC supply to Fan 2 Trigger output (D) 4A 3B 3C 6B, 8C, 5D 7C, 1D					/A, 3C
TSET			/		3R
X AC in to line-sense and line-sync circuits AC in to line-sense and line-sync circuits AC supply to Fan 2 AC supply to Fan 2 AC supply to Fan 2					
XFER_1 \ AC supply to Fan 2 5D 7C, 1D			72 1	6B 8C	30
XFER_1 \ AC supply to Fan 2 7C, 1D		The in to line sense and line sync enealts			
	XFER 1 \	AC supply to Fan 2			
1 AFEN / / 1 1 /K 1 /K	XFER 2 /	The supply to Tun 2		7B , 1D	
XFER 3 \ AC supply to Fan 1 \ 7B, 1C	_	AC supply to Fan 1			
XFER 5 / 7A, 1C		The supply to I all I			
AC in to line-voltage sense circuit AC in to line-voltage sense circuit		AC in to line-voltage sense circuit			
ZERO REF Reference for line-sync circuit 4D, 7C					
	_			1D , /C	8C, 4A
		` /			8C, 4A
		· /			8C, 4A
					8C, 4A
					8C, 4A
		· /			8C, 4A
50*/60 Line-frequency fan-speed compensation (A) 2C 3C, 3B		` /	2C	3C. 3B	,

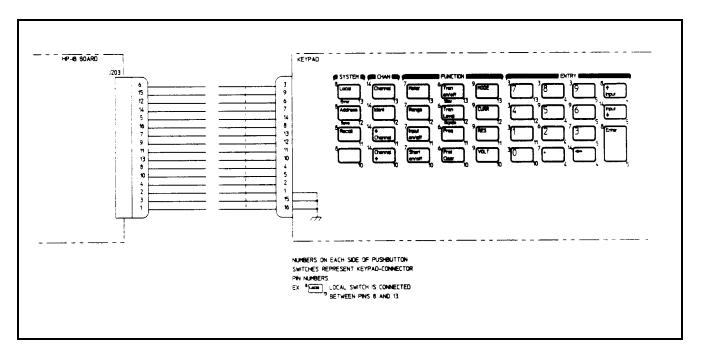


Figure 6-1. Keypad Wiring

Table 6-2. Component Locations

COO	RDINA	TES	COOL	RDINA	TES	COO	RDINA	TES	COO	RDINA	TES	COO	RDINA	TES	COORD	INATE	S	COOR	DINAT	ES
	"A"	"B"		"A"	"B"		"A"	"B"		"A"	"B"		"A"	"B"		"A"	"B"		"A"	"B"
C201	8.6	-3.7	C246	11.0	-2.5	J203	7.8	-3.5	R246	0.6	-3.4	R282	6.4	-3.9	R317	7.3	-4.3	U212	7.8	-2.4
C202	8.8	-3.2	C247	11.8	-2.9	J204	0.4	-5.2	R247	11.2	-4.8	R283	5.9	-5.3	R318	9.2	-5.8	U213	4.2	-5.6
C203	12.0	-5.2	C248	12.6	- 2.5	J205	14.4	-0.6	R248	0.6	- 4.4	R284	5.8	-5.3	R319	9.3	- 5.8	U214	4.8	-5.6
C205	3.7	-2.1	C249	1.4	-0.3	J206	14.4	-1.3	R249	10.9	-4.2	R285	6.1	-5.8	R320	7.2	-4.3	U215	1.6	-4.4
C206	3.7	-2.3	C250	2.3	-0.1	J207	14.4	-2.4	R250	11.1	-3.7	R286	6.7	-5.8	R321	7.4	-4.8	U216	3.7	-5.6
C207	5.6	-1.5	C251	3.8	-3.9	J208	12.9	-3.4	R251	10.8	-3.7	R287	6.0	-3.9	R322	7.7	-5.3	U217	2.5	-5.5
C208	9.0	-1.3	C252	3.7	-0.3	J209	14.4	-4.8	R252	12.2	-3.7	R288	6.0	-5.3	R323	7.5	-4.3	U219	1.6	-3.5
C209	8.0	-1.3	C253	3.1	-0.3	J210	13.7	-5.0	R253	11.0	-3.7	R289	8.2	-4.3	R324	7.8	-5.3	U226	4.8	-2.4
C210	2.8	-2.8	C254	2.7	-5.7	L200	10.3	-1.3	R256	12.4	-3.7	R290	11.2	-4.2	R325	9.1	-5.8	U227	6.0	-3.7
C211	5.0	-5.7	C255	7.5	-1.5	L201	11.6	-1.3	R257	11.9	-3.7	R291	11.4	-2.6	R326	8.1	-4.8	U228	4.8	-3.7
C214a	4.4	-1.5	C256	6.3	-1.5	Q201	12.0	-4.3	R258	11.4	-4.2	R292	11.6	-3.1	RT1	8.5	-4.2	U229	6.6	-2.4
C215	3.8	-5.8	C257	12.6	-5.8	Q207	10.1	-4.8	R259	11.6	-4.2	R293	12.8	-2.0	RT201	9.0	-3.0	U230	6.0	-2.4
C223	10.9	-5.7	C258	9.2	-4.9	Q208	11.3	-5.1	R260	11.8	-3.7	R294	8.1	-4.9	S202	14.5	-4.2	U233	6.6	-4.9
C224	1.0	-5.0	C259	8.7	-2.6	Q209	10.2	-3.2	R261	11.5	-3.7	R295	7.5	-5.8	S203	14.5	-5.7	U234	10.8	-5.0
C225	1.0	-5.6	D202	1.1	-3.9	Q210	11.8	-3.2	R262	11.7	-3.7	R296	7.9	-5.8	S204	14.5	-3.4	U235	4.2	-3.7
C226	1.6	-5.0	D204	1.1	-4.0	Q211	8.9	-4.9	R263	0.2	-4.2	R297	5.9	-3.9	TB201	-0.1	-3.5	U237	12.5	-4.3
C230	1.9	-2.8	D205	12.9	-5.8	Q212	7.1	-5.1	R264	12.3	-4.2	R298	6.4	-5.8	TP1	2.1	-5.9	U238	11.1	-4.3
C231	1.2	-4.6	D206	12.8	-5.1	Q213	7.1	-5.4	R265	8.7	-4.8	R299	8.3	-4.8	TP2	2.1	-6.1	U239	8.4	-2.4
C232	3.7	-1.3	D207	12.8	-5.8	R201	8.4	-3.7	R266	7.7	-4.3	R300	8.5	-4.3	TP3	0.7	-5.3	U241	9.8	-3.6
C233	11.1	-5.7	D208	12.9	-5.1	R202	8.7	-3.2	R267	7.9	-4.3	R301	2.3	-0.2	TP6	2.5	-6.1	U242	11.4	-3.6
C234	3.4	-0.2	D212	11.4	-5.7	R205	6.7	-3.6	R268	6.3	-3.9	R302	6.2	-5.8	TP9	2.5	-5.9	U243	8.8	-5.4
C235	6.8	-1.3	D213	12.0	-4.2	R208	0.3	-3.0	R269	7.8	-4.8	R303	6.3	-5.8	TP201	4.7	-1.1	U245	6.6	-4.5
C236	0.6	-3.7	D214	8.9	-4.8	R214	5.2	-2.4	R270	8.1	-5.3	R304	6.5	-5.8	U201	1.3	-2.4	U246	9.4	-2.4
C237	12.5	-4.2	D215	8.6	-4.8	R215	1.1	-3.2	R271	7.6	-5.3	R305	8.4	-4.8	U202	2.3	-2.4	U247	5.3	-5.5
C238	10.7	-4.3	D216	8.8	-4.8	R228	8.7	-2.4	R272	8.0	-4.3	R306	6.2	-3.9	U203	3.3	-2.4	VR1	2.2	-4.1
C239	13.1	-5.2	F201	12.7	-1.1	R237	7.4	-3.7	R273	8.0	-5.8	R307	9.0	-4.3	U204	4.2	-1.1	VR2	1.1	-3.6
C240	1.1	-3.5	F202	13.6	-2.9	R238	10.7	-5.7	R274	11.3	-3.7	R308	9.0	-5.8	U205	2.4	-4.3	W1	10.6	-5.7
C241	2.5	-1.7	F203	13.2	-2.9	R239	0.6	-4.3	R275	10.3	-3.7	R309	6.1	-3.9	U206	3.3	-4.3	Y201	3.5	-2.3
C242	8.5	-3.9	J1	10.3	-0.9	R240	0.6	-4.2	R276	9.8	-2.6	R311	6.8	-4.8	U207	3.1	-5.5			
C243	6.7	-4.2	J2	7.4	-0.9	R241	0.6	-3.8	R277	10.0	-3.1	R313	6.9	-5.7	U208	5.4	-3.7			
C243	7.2	-4.2	J3	5.1	-0.9	R242	3.7	-1.6	R278	11.2	-2.2	R314	7.6	-4.3	U209	7.2	-2.4			
C244	5.8	-4.7	J201	0.1	-1.7	R243	3.7	-1.7	R280	6.6	-5.3	R315	7.3	-5.8	U210	7.2	-3.7			
C245	10.2	- 2.9	J202	9.4	-3.5	R244	1.2	- 5.0	R281	5.8	- 4.4	R316	7.4	- 5.3	U211	6.6	-3.7			

Table 6-3. Schematic Diagram Notes

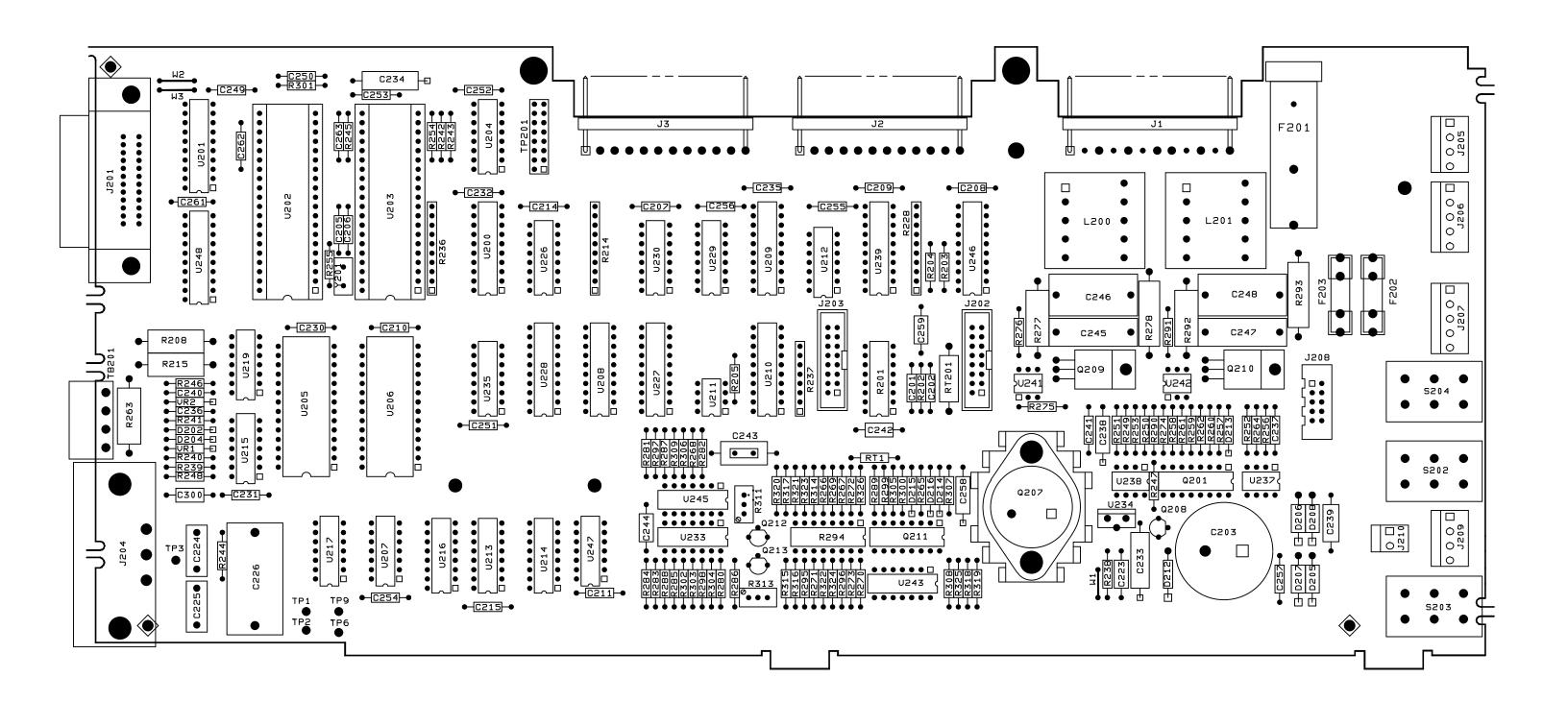
- 1. All resistors are in ohms $\pm 1\%$, 1/8 W, unless otherwise specified.
- 2. All capacitors are in microfarads unless otherwise specified.
- 3. All unmarked capacitors are 0.047µF.
- 4. An asterisk negates a signal name. For example, $\overline{\text{CS2}}$ appears on the schematic as CS2*.
- 5. Signal lines that are terminated by flags continue on other sheets, and may also go to other locations on the same sheet (see Table 6-3). Note that flags do not indicate signal flow direction.

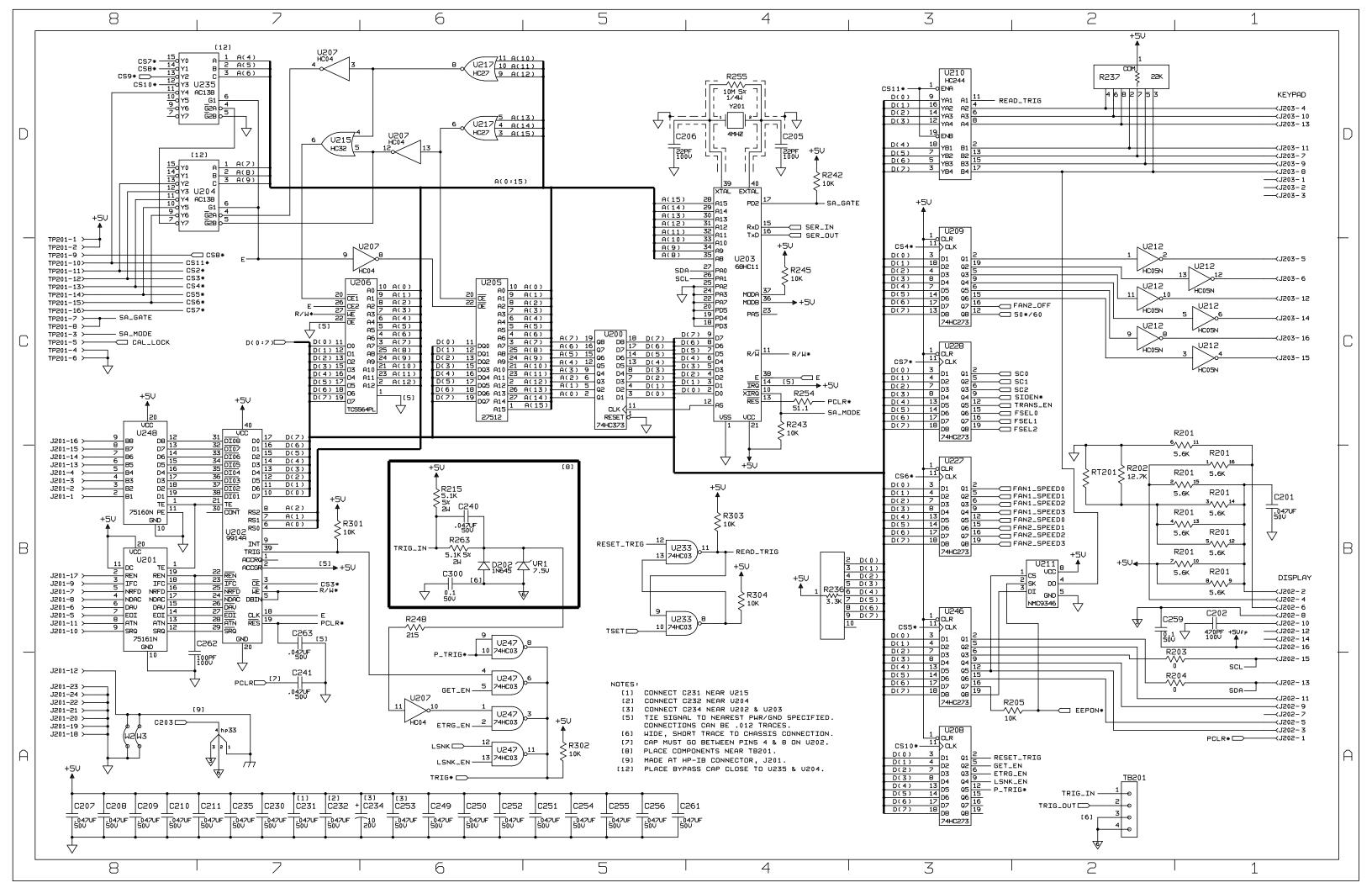
6. Unterminated signal lines go to at least one other location of the same schematic sheet.

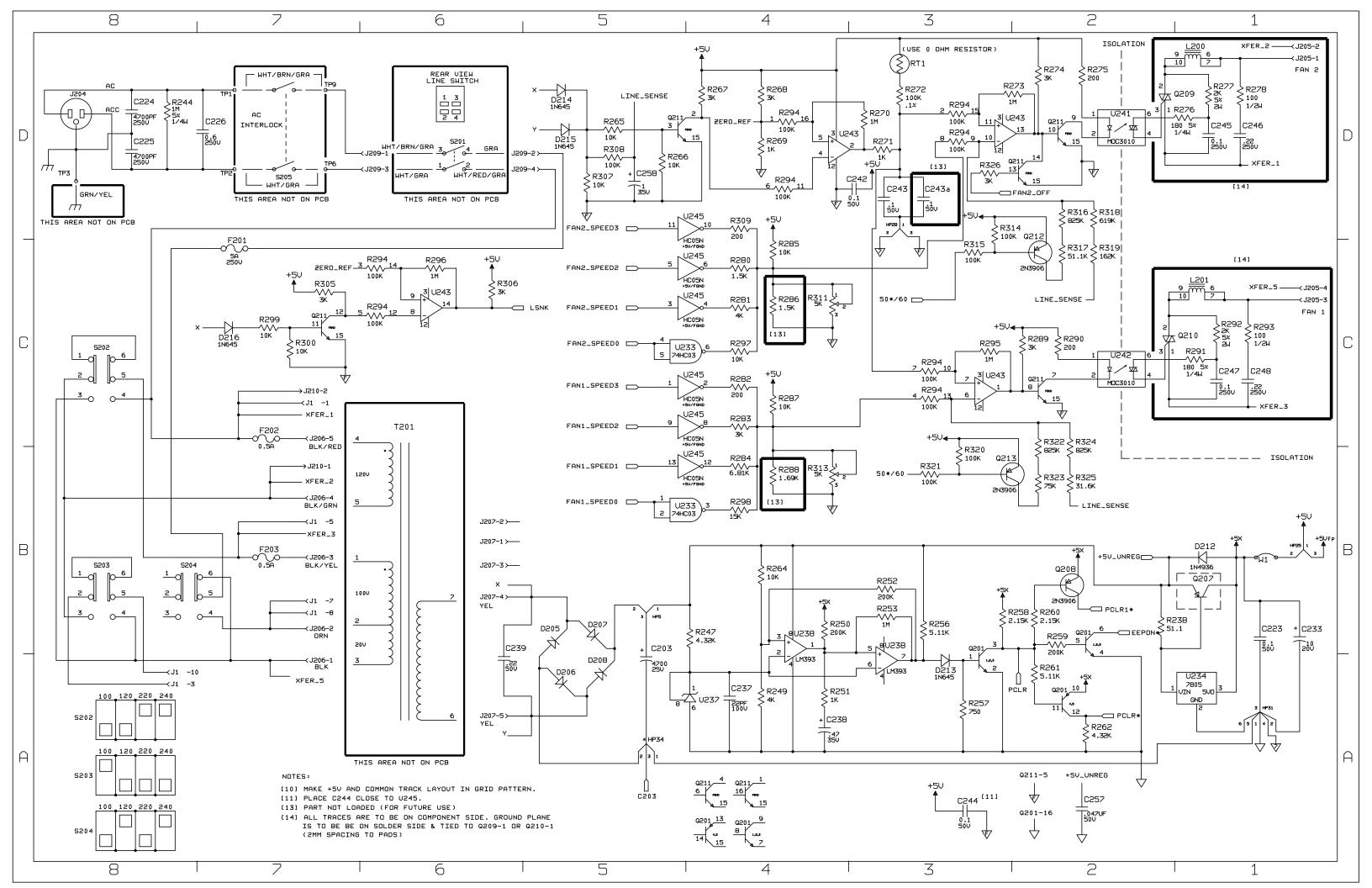
- 7. Heavy signal lines represent multiple-wire data buses.
- 8. Unless otherwise noted, bias connections to integrated-circuit packages are as follows:

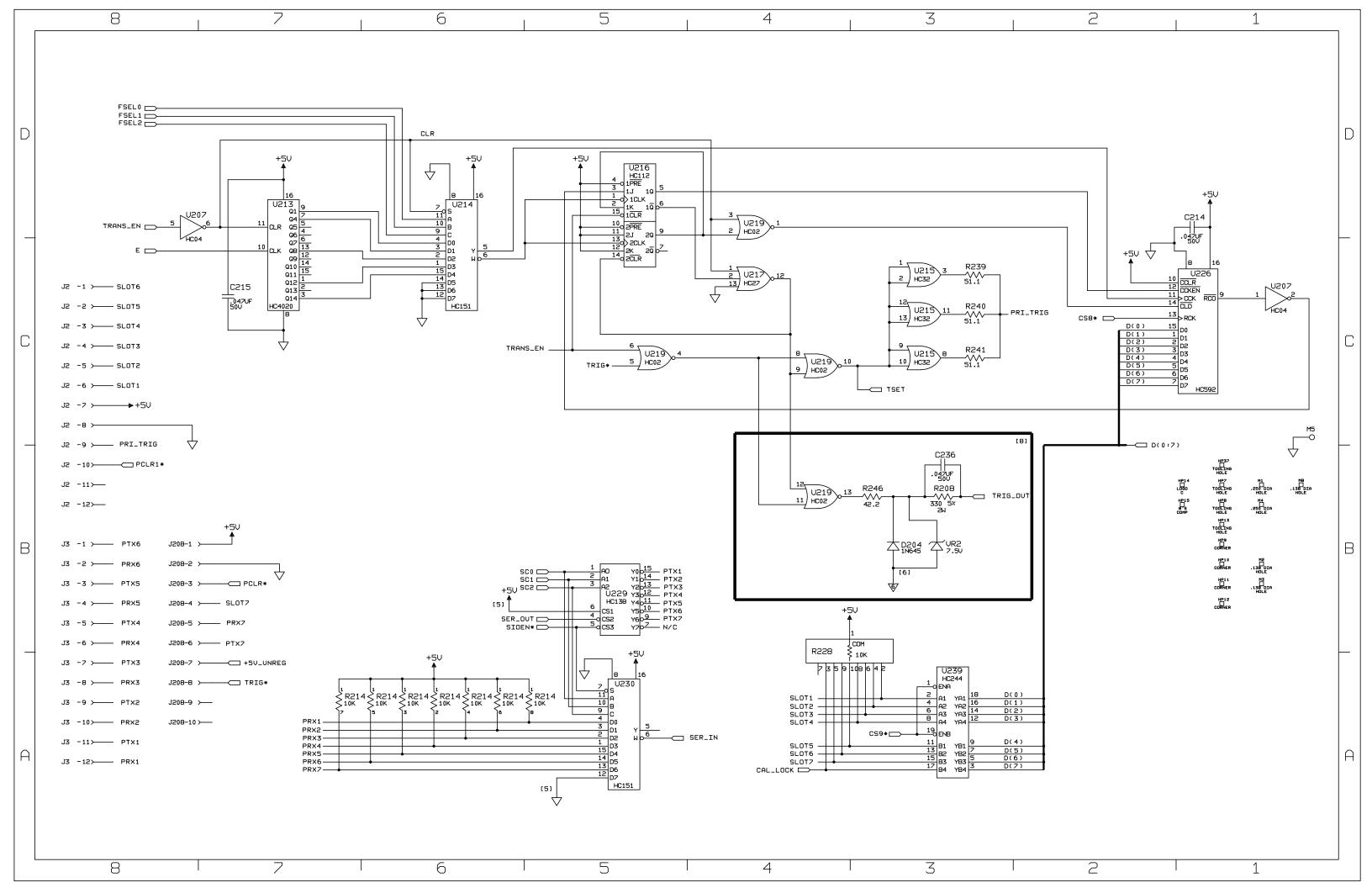
	Common	+ 5V
14-pin packages	pin 7	pin 14
16-pin packages	pin 8	pin 16
20-pin packages	pin 10	pin 20

9. Primary refers to the microprocessor and related circuits on the GPIB board. Secondary refers to the microprocessor and related circuits on the Control Board.









Manual Backdating

This section describes changes that must be made to the manual so that it applies to instruments with serial numbers lower than those listed on the title page. Look in the following table for the serial number of your instrument, and make only those changes listed for your instrument. Note that for some changes, you may be instructed to update the instrument if certain components are being replaced during repair.

	Agilent 6050A	
Serial Prefix	Serial Number	Changes
2908A	00101-00110	1-8
2913A	00111-00152	1-7
2921A	00153-00332	1-6
2935A	00333-00402	1-5
2940A	00403-01862	1-4
3211A	01863-02402	1-4
3307A	02403-02482	1-3
3312A	02483-03342	1-3
3435A	03343-04672	1-2
3620A	04673-05432	1
	Agilent 6051A	
Serial Prefix	Serial Number	Changes
2927A	00101-00220	1-4
3211A	00221-00300	1-4
3307A	00311-00450	1-3
3436A	00451-00600	1, 2
3624A	00601-00710	1

Change 1

Make the following GPIB board parts list changes:

Change: A3 GPIB board to p/n 5060-3550

U202 to p/n 1820-2549

U203 to p/n 1820-3367

U205 to p/n 06050-80011

Delete: C263, 0.047uF, p/n 0160-5422

R203,204 0 ohm, p/n 8159-0005

R236 Network, 3.3k p/n 1810-0278

R245 10K 1%, p/n 0757-0442

R254 51.1 1% p/n 0757-0394

R255 10M 5% p/n 0699-1797

Change 2

Change R286 to R311, 5k pot 10% p/n 2100-3089. Change R288 to R313, 5k pot 10% p/n 2100-3089.

Change 3

Make the following GPIB board parts list changes: Change: A3 GPIB board to p/n 5060-3303.

Delete: U201, p/n 1820-6045.

U248, p/n 1820-6170.

C300, .1uF p/n 0160-4835.

C261, .047uF, p/n 0160-5422.

Add: U201, p/n 1LH4-0001.

Change 4

In the parts list and on the schematic (sheet 1 of 3), Delete C300, 0.1uF 10% 50V, p/n 0160-4835. Add C240, p/n 0160-5422.

Change 5

Remove C259 from the parts list and from the schematic (sheet 1, B2). Remove RT1 from the parts list and from the schematic (sheet 2, D3). On the schematic, replace RT1 with a short (i.e., connect R272 to +5V).

In the parts list, change the GPIB Board to 5060-3257. If the GPIB Board has to be replaced, use the GPIB Board assembly number 5060-3303 listed in Table 5-4. Note that some components at the front edge of the GPIB Board are shifted slightly from the coordinates given in Figure 6-2 and Table 6-2.

Change 6

In the parts list, change the keypad pc board to P/N 5020-2691. If the keypad pc board has to be replaced in these units, you must use p/n 5020-2691.

Change 7

In these units, EEPROM U205, P/N 06050-80011, is Rev A.01.00. For signature analysis, use the signatures provided in this appendix instead of the signatures in Tables 3-4 through 3-9. If U205 has to be replaced, use P/N 06050-80011 Rev A.01.01, for which the signatures provided in Tables 3-4 through 3-9 are correct.

Change 8

In the parts list and on the schematic (sheet 2, C4), change R311, 5K pot, to R286, 1.5K resistor. Also change R313 (sheet 2, B4), 5K pot, to R288, 1.69K resistor. If either R286 or R288 has to be replaced, use 5K pots, P/N 2100-3089, listed in Table 5-4 for R311 (R286) and R313 (R288)

Table 3-4. Primary Microprocessor Signature Analysis

Description: These signatures check primary microprocessor U203, ROM U205, and RAM U206. The signatures are valid for ROM U205 firmware revision "Rev A.01.01". Use the test setup described in "Test Setup for S.A.". Connect the signature analyzer's CLOCK input to U207-9.

Signatures:			
	μP U203	ROM U205	RAM U206
+5V	U203-4,7,21 = 437U	U205-28 = 437U	U206-28,14 = 437U
Common	U203-1,9,10	U205-14	U206-1,14,22
4 MHz	U203-2,3		
1 MHz	U203-40	U205-22	U206-26
PLCR	U203-6 = +5V		
A(0)	U203-13 = OUC7	U205-10 = OUC7	U206-10 = OUC7
A(1)	U203-14 = 3PU9	U205-9 = 3PU9	U206-9 = 3PU9
A(2)	U203-15 = H88F	U205-8 = H88F	U206-8 = H88F
A(3)	U203-16 = H2FP	U205-7 = H2FP	U206-7 = H2FP
A(4)	U203-17 = 3P77	U205-6 = 3P77	U206-6 = 3P77
A(5)	U203-18 = 8PO6	U205-5 = 8PO6	U206-5 = 8PO6
A(6)	U203-19 = F73H	U205-4 = F73H	U206-4 = F73H
A(7)	U203-20 = AU81	U205-3 = AU81	U206-3 = AU81
A(8)	U203-29 = FCUU	U205-25 = FCUU	U206-25 = FCUU
A(9)	U203-28 = A8PO	U205-24 = A8PO	U206-24 = A8PO
A(10)	U203-27 = A4P1	U205-21 = A4P1	U206-21 = A4P1
A(11)	U203-26 = C7U7	U205-23 = C7U7	U206-23 = C7U7
A(12)	U203-25 = 948P	U205-2 = 948P	U206-2 = 948P
A(13)	U203-24 = 9H46	U205-26 = 9H46	
A(14)	U203-23 = 43CP	U205-27 = 43CP	
A(15)	U203-22 = 8A6O	U205-1 = 8A60	
D(0)	U203-37 = C22U	U205-11 = C22U	U206-11 = C22U
D(1)	U203-36 = 418H	U205-12 = 418H	U206-12 = 418H
D(2)	U203-35 = 8795	U205-13 = 8795	U206-13 = 8795
D(3)	U203-34 = 6953	U205-15 = 6953	U206-15 = 6953
D(4)	U203-33 = 9O7A	U205-16 = 9O7A	U206-16 = 9O7A
D(5)	U203-32 = 5F5P	U205-17 = 5F5P	U206-17 = 5F5P
D(6)	U203-31 = C65F	U205-18 = C65F	U206-18 = C65F
D(7)	U203-30 = P43U	U205-19 = P43U	U206-19 = P43U
SER_IN	U203-11 = 2C34		
SER_OUT	U203-12 = unstable		
R/W	U203-38 = 97F2		U206-27 = 97F2
CE		U205-20 = 75A3	
CE1		U206-22 = 437U	U206-20 = U4U3
	U207-3 = 567U	U215-4 = 567U	U217-3 = 8A6O
	U207-4 = 1500	U215-5 = 36HF	U217-4 = 43CP
	U207-8 = E clock	U215-6 = U4U3	U217-5 = C762
	U207-9 = E clock		U217-6 = 75A3
	U207-12 = 36HF		U217-8 = 567UP
	U207-13 = 75A3		U217-9 = 948P
			U217-10 = C7U7
			U217-11 = A4P1

Table 3-5. GPIB Interface Signature Analysis (Primary)

Description: These signatures check the GP-IB talker/listener IC U202. The signatures are valid for ROM U205 firmware revision "Rev A.01.01". Use the test setup described in "Test Setup for S.A." Connect the signature analyzer's CLOCK input to TP201-12 (CS3).

```
U202-1 = 7339 pulsing
U202-2 =
U202-3 = 1 \text{ MHz "E" clock}
U202-4 = OOOO PLCR
U202-5 = OOOO pulsing
U202-6 =
U202-7 = 7339 + 5V
U202-8 = OOOO common
U202-9 = 7339 pulsing
U202-10 = OOOO  pulsing
U202-11 =
U202-12 = OC57
U202-13 = O5AC
U202-14 = 167U
U202-15 = A83P
U202-16 = 69P1
U202-17 = 2O5A
U202-18 = 1427
U202-19 = H6C9
U202-20 = OOOO common
U202-21 = 23UH
U202-22 = 54A6
U202-23 = 8OAO
U202-24 = 7339
U202-25 = 7339
U202-26 = 7339
U202-27 = 713F
U202-28 = 7692
U202-29 = 71PF
U202-30 = U253
U202-31 = 338F
U202-32 = 5363
U202-33 = 6314
U202-34 = 7C2U
U202-35 = 7435
U202-36 = 7339
U202-37 = 7339
U202-38 = 7339
U202-39 = 7435
U202-40 = 7339 + 5V
```

Table 3 6. Front Panel Interface Signature Analysis (Primary)

Description: These signatures check the front panel interface IC's U246 U209, U210 and U212. The signatures are valid for ROM U205 firmware revision "Rev A.01.01". Use the test setup described in "Test Setup for S.A.". Connect the signature analyzer's CLOCK input to the chip select line of the IC under test as specified below.

Signatures:	
U246 Display Driver- connect	CLOCK to TP2O1-14 (CS5)
WAACA OALIE STV	Water 0000 1:
U246-1 = O1UF + 5V	U246-11 = OOOO pulsing
U246-2 = OO81	U246-12 = OOO8
U246-3 = O1O2	U246-13 = OO1O
U246-4 = OO81	U246-14 = OOO8
U246-5 = OO4O	U246-15 = 0004
U246-6 = OO2O	U246-16 = OOO2
U246-7 = OO4O	U246-17 = OOO4
U246-8 = OO2O	U246-18 = OOO2
U246-9 = OO10	U246-19 = 0001
U246-10 = OOOO common	U246-20 = O1UF + 5V
U209, U212 Keypad Drivers - connect	CLOCK to TP201-13 (CS4)
U209-1 = O7U3 + 5V	U209-11 = OOOO pulsing
U209-2 = OO81	U209-12 = O3O6
U209-3 = O1O2	U209-13 = O6OH
U209-4 = O245	U209-14 = OOO8
U209-5 = O122	U209-15 = OOO4
U209-6 = O2OH	U209-16 = O2O7
U209-7 = O41A	U209-17 = O4O8
U209-8 = O42A	U209-18 = O68P
U209-9 = O215	U209-19 = O347
U209-10 = OOOO common	U209-20 = O7U3 + 5V
U212-1 = OO81	U212-8 = O4OA
U212-2 = O7OH	U212-9 = O20H
U212-3 = OOO4	U212-10 = O60U
U212-4 = O7U4	U212-11 = O122
U212-5 = O215	U212-12 = O40A
U212-6 = O4OA	U212-13 = O347
U212-7 = OOOO common	U212-14 = O7U3 + 5V
U210 Keypad Receiver - connect	CLOCK to TP201-10 (CS11)
U210-1,19 = OOOO pulsing Lo (Chip Select)	
U210-2,18 = O1UF	press keypad " 1 " = O17H
U210-3,17 = O1UF	press keypad " 8 " = O17H
U210-4,16 = O1UF	
U210-5,15 = O1UF	press keypad " 4 " = O17H
U210-6,14 = O1UF	press keypad " 9 " = O17H
U210-7,13 = O1UF	press keypad " 7 " = O17H
U210-8,12 = O1UF	press keypad " 0 " = O17H
U210-9,11 = O1UF	pulsing 9 (fast), 11 (slow)
U210-10 = OOOO common	
U210-20= O1UF +5V	

Table 3-7. Trigger Circuit Signature Analysis (Primary)

Description: These signatures check the operation of the primary trigger circuits. The signatures are valid for ROM U205 firmware revision "Rev A.01.01". Use the test setup described in "Test Setup for S.A.". Connect the signature analyzer's CLOCK input to the IC under test as specified below.

Signatures:

U208 - connect CLOCK to U235-12 (CS10)

```
U208-11 = OOOO  pulsing LO
U208-1 = 7U39 + 5V
U208-2 = 28F7
                                    U208-12 = 162P
U208-3 = 518P
                                    U208-13 = 2F5F
U208-4 = 20H3
                                    U208-14 = 2P41
U208-5 = 1069
                                    U208-15 = 1720
U208-6 = 1009
                                    U208-16 = 1726
U208-7 = 2O12
                                    U208-17 = 2P4H
U208-8 = 2O72
                                    U208-18 = 2P4C
U208-9 = 1039
                                    U208-19 = 1725
U208-10 = OOOO
                                    U208-20 = 7U39 + 5V
```

U207, 213-217, 219, 226, 247 - connect CLOCK to U207-9 (E clock)

ı	, , ,		,	
	U233-8 = 154U	U247-1 = OOO(O	U219-1 = C762
	U233-9 = 28C7	U247-2 = 3P88		U219-2 = OOOO
	U233-10 = 3HU8	U247-3 = 8A9A		U219-3 = U41H
	U233-11 = 28C7	U247-4 = 145P		U219-4 = 7P87
	U233-12 = U15F	U247-5 = 4C3H		U219-5 = 8A9A
	U233-13 = 154U	U247-6 = 8A9A		U219-6 = C762
		U247-7 = OOO(Ocom	U219-7 = OOOO com
	U207-5 = C762	U247-8 = 8A9A		U219-8 = 7P87
	U207-6 = U41H	U247-9 = 648A		U219-9 = OOOO
	U207-10 = OOOO	U247-10 = 648A	Α	U219-10 = 3HU8
	U207-11 = 437U	U247-11 = 8A9A	A	U219-11 = 7P87
		U247-12 = 437U	J	U219-12 = OOOO
	U217-1 = U41H	U247-13 = 5U47	7	U219-13 = 3HU8
	U217-2 = 437U	U247-14 = 437U + 5V		U219-14 = 437U + 5V
	U217-12 = OOOO			
	U217-13 = OOOO	U215-1,2,3,8,9,1	10,11,12,13 = 3HU8	
	U213-1 = OOOO	U214-1 = OOOO	U216-1 = H1A1	U226-1 = 418H
	U213-2 = OOOO	U214-2 = OOOO	U216-2 = OOOO	U226-2 = 8795
	U213-3 = OOOO	U214-3 = 5AC1	U216-3 = OOOO	U226-3 = 6953
	U213-4 = 3842	U214-4 = 92HP	U216-4 = 437U	U226-4 = 907A
	U213-5 = OOOO	U214-5 = 92HP	U216-5 = OOOO	U226-5 = 5F5P
	U213-6 = OOOO	U214-6 = H1A1	U216-6 = 437U	U226-6 = C65F
	U213-7 = 5AC1	U214-7 = U41H	U216-7 = 437U	U226-7 = P43U
	U213-8 = OOOO com	U214-8 = OOOO com	U216-8 = OOOO com	U226-8 = OOOO
	U213-9 = 92HP	U214-9 = H525	U216-9 = OOOO	U226-9 = 437U
	U213-10 = E clock	U214-10 = PU28	U216-10 = 437U	U226-10 = 437U
	U213-11 = U41H	U214-11 = 885F	U216-11 = 437U	U226-11 = 92HP
	U213-12 = OOOO	U214-12 = OOOO	U216-12 = 437U	U226-12 = OOOO
	U213-13 = OOOO	U214-13 = OOOO	U216-13 = H1A1	U226-13 = 437U
	U213-14 = OOOO	U214-14 = OOOO	U216-14 = OOOO	U226-14 = C762
	U213-15 = OOOO	U214-15 = OOOO	U216-15 = C762	U226-15 = C22U
	U213-16 =437U +5V	U214-16 =437U +5	U216-16 = 437U + 5V	U226-16 = 437U + 5V

Table 3-7. Trigger Circuit Signature Analysis (Primary) continued

```
U228 - connect CLOCK = TP201-16 (CS7)
U228-1 = UFP6 + 5V
                                            U228-11 = OOOO Pulsing LO
U228-2 = 5505
                                            U228-12 = OOO8
U228-3 = AAOC
                                            U228-13 = OO10
U228-4 = 6679
                                            U228-14 = OOO8
U228-5 = 333F
                                            U228-15 = OOO4
U228-6 = OU39
                                            U228-16 = OOO2
U228-7 = IP72
                                            U228-17 = OOO4
U228-8 = OO20
                                            U228-18 = OOO2
U228-9 = OO10
                                            U228-19 = OOO1
U228-10 = OOOO com
                                            U228-20 = UFP6 + 5V
```

Table 3-8. Module Interface Signature Analysis (Primary)

Description: These signatures check the module communications, U229 data transmission to modules, U230 data transmission from modules, and U239, which indicates the number of modules installed. Connect the signature analyzer's clock input to the IC under test as specified below.

```
U229, 230 - connect CLOCK to U207-9 (E clock)
```

U229-1 = 7H51	U230-1 = 437U
U229-2 = 284O	U230-2 = 437U
U229-3 = 3O9C	U230-3 = 437U
U229-4 = unstable	U230-4 = 437U
U229-5 = U123	U230-5 = 684C
U229-6 = 437U + 5V	U230-6 = 2C34
U229-7 = 437U + 5V	U230-7 = U123
U229-8 = OOOO com	U230-8 = OOOO com
U229-9 = unstable	U230-9 = 309C
U229-10 = unstable	U230-10= 284O
U229-11 = unstable	U230-11 = 7H51
U229-12 = unstable	U230-12 = OOOO
U229-13 = unstable	U230-13 = 437U
U229-14 = unstable	U230-14 = 437U
U229-15 = unstable	U230-15 = 437U
U229-16 = 437U + 5V	U230-16 = 1HC4 + 5V

U239 - connect CLOCK to CS9 (U235-13)

Chip Select	U239-1,19 = OOOO Pulse LO	
Slot 1	U239-2,18 = O1UF	short $J2-6$ to $J2-8 = OOOO$
Slot 2	U239-4,16 = O1UF	short $J2-5$ to $J2-8 = OOOO$
Slot 3	U239-6,14 = O1UF	short $J2-4$ to $J2-8 = OOOO$
Slot 4	U239-8,12 = O1UF	short $J2-3$ to $J2-8 = OOOO$
Slot 5	U239-11,9 = O1UF	short $J2-2$ to $12-8 = OOOO$
Slot 6	U239-13,7 = O1UF	short $J2-1$ to $J2-8 = OOOO$
Slot 7	U239-15,5 = O1UF	short J208-4 to J2-8= OOOO
CAL_LOCK	U239-17,3 = O1UF	short TP201-5 to TP201-4 = $OOOO$

Table 3-9. Fan Speed Control Signature Analysis (Primary)

Description: These signatures check the fan speed control circuits. Connect the signature analyzer's clock input to the IC under test as specified below.

Signatures:

```
U227- connect CLOCK to TP201-15 (CS6)
```

```
U227-11 = OOOO Pulse LO
U227-1 = O1UF + 5V
U227-2 = OO81
                                              U227-12 = OOO8
U227-3 = O102
                                              U227-13 = OO10
U227-4 = OO81
                                              U227-14 = OOO8
U227-5 = OO40
                                              U227-15 = OOO4
U227-6 = OO20
                                              U227-16 = OOO2
U227-7 = OO40
                                              U227-17 = OOO4
                                              U227-18 = OOO2
U227-8 = OO20
U227-9 = OO10
                                              U227-19 = OOO1
U227-10 = OOOO com
                                              U227-20 = O1UF + 5V
```

U233, U241, 242, 245 - connect CLOCK to U207-9 (E clock)

U241-1 = 437U + 5V	U242-1 = 437U + 5V
U241-2 = 90F3	U242-2 = OOOO

U233-1 = 2171U233-2 = 2171

U233-3 = OOOO Pulsing LO

U233-4 = 762CU233-5 = 762C

U233-6 = OOOO Pulsing LO

U233-7 = OOOO com

U245-7 = OOOO com

U245-8 = OOOO
U245-9 = 1687
U245-10 = OOOO
U245-11 = 5255
U245-12 = OOOO Pulsing
U245-13 = 899A

U245-14 = 437U + 5V

"A" Load Modules Troubleshooting

This section describes the changes that must be made to the troubleshooting procedures in section 3 of the manual that apply to "A" modules.

Earlier "A" Load Modules

Use the troubleshooting procedures on pages B-2 through B-15 in this appendix when troubleshooting the earlier "A" load modules. The earlier "A" load modules contain control boards and power boards with the following assembly numbers:

	Control Board	Power Board
Agilent 60501A	60502-60020	60501-60021
Agilent 60502A	60502-60020	60502-60021
Agilent 60503A	60503-60020	60503-60021
Agilent 60504A	60504-60020	60504-60021

Refer to the service manuals that accompany your load modules to determine if your load module uses one of the above board assemblies .

Later "A" Modules

Use the troubleshooting procedures for the "B" load modules discussed in Chapter 3 of this manual when troubleshooting the later "A" load modules. The later "A" load modules contain control boards and power boards with the following assembly numbers:

	Control Board	Power Board
Agilent 60501A	60502-60023	60501-60022
Agilent 60502A	60502-60023	60502-60024
Agilent 60503A	60503-60023	60503-60022
Agilent 60504A	60504-60023	60504-60024

Refer to the service manuals that accompany your load modules to determine if your load module uses one of the above board assemblies .

Table 3-3. Test Points (continued)

Test Point Number	Signal	Measurement and Conditions	
17) U308-1	CV PROG	In VOLT MODE, + 10V with full rated voltage programmed; +0.5V with 3 volts programmed.	
		In CURR MODE or RES MODE (middle and high ohm ranges), + 13V.	
(18)	CC PROG	In RES MODE (low ohm range), 0 to +10V depending upon resistance value programmed. In CURR MODE, + 10V with full rated current programmed.	
U308-7		In VOLT MODE, RES MODE (low ohm range), or with INPUT OFF: -13V.	
		In RES MODE (middle and high ohm ranges), 0 to + 10V depending upon resistance value programmed.	
①9 U315-1	TRANS_EN	High level with transient operation programmed on (TRAN ON). Low level with transient operation programmed off (TRAN OFF).	
20 U324-1	SLEW	In CURR MODE, -10V with full rated current programmed; 0V with zero current programmed.	
		In VOLT MODE, -10V with full rated voltage programmed; 0V with zero voltage programmed.	
②1) L1200 16	DAC_REF	Low level in CURR or VOLT MODE. High level in RES MODE (any range).	
U309-16 ② U309-8	CR	Low level in RES MODE (low ohm range). High level in CURR, VOLT, or RES (middle or high ohm range) MODE.	
3 U309-1	CG	Low level in RES MODE (middle or high ohm range). High level in CURR, VOLT, or RES (low ohm range) MODE.	
24 TB301-9	PORT	High level with PORT0 ON programmed. Low level with PORT0 OFF programmed.	
25	-10V Ref	-10V (9.95 to 10.05V).	
U329-4 26 U323-1	+ 12V Ref	+ 12V (11.28 to 11.44V).	
		POWER BOARD	
② U14-5	IPROG	Under normal operating conditions (input is regulated) measurement should be: $-0.1V \times 1$ Iin (e.g. $-0.1V \times 6 = 0.6V$).	
		With input unregulated or disconnected, the measurement will be: - 7V in CURR Mode. +0.9V in VOLT or RES MODE.	
28) cath-D17	+ OV	+ 14V when OV condition is false (normal)13V when OV condition is true.	

Table 3-3. Test Points (continued)

Test Point Number	Signal	Measurement and Conditions	
29	CC Loop Gain	+ 15V when input voltage is more than 2.5V.	
U16-1	control	-15V when input voltage is less than 2.5V.	
30	NOT USED		
③) ③1) U9-1	RNG	Low level when the high current range or the middle resistance range is programmed.	
		High level when the low current range, the low resistance range, or the high resistance range is programmed.	
③ U14-1 U15-1*	-VMON	-0.167 X Input Voltage (e.g0.167 X 60 = -10.02V).	
33) cath-D11	+OP	-0.9V (full rated voltage input) to -6V (zero volts input) when the OP condition is false. Pulses when the OP condition is true. See test point 3.	
34) U10-1,2,13,14	- OP	-14V when the OP condition is false. Pulses when the OP condition is true. See Figure 3-10.	
3 5 U17 -1	-VMONA	-0.167 X Input Voltage (e.g. 0.167 X 60 = - 10.02V).	
③6 U9-16	EPC_EN	Low level when extended power is available. High level when extended power is not available.	
③7 U12-1	OP circuit	-10V when input is at full rated current with extended power not available8.5V when input is at full rated current with extended power available.	
38 U12-7	OP circuit	Same as above except when input is at full rated voltage.	
39 cath-D55	OC circuit control	+ 13V when OC condition false (normal). + 8V when OC condition is true or when input stages are unregulated.	
40 Q11-E	OC circuit control	+ 10V when OC condition is false (normal). +8.5V when unregulated or when OC condition is true.	
(41) cath-D23	Input Power Stage Turn on	+5V when turned on. 0V when turned off.	
42 U5-1 U5-7*	Input Power Stage 2 D	6.3V (approx.) with full rated current input. -0.5V (approx.) with the input off.	
43 Q2-1	Input Power Stage 2 D	5.4V (approx.) with full rated current input. 4.0V (approx.) with 10% rated current input0.5V (approx.) with zero current input.	
(44) U6-7 U6-1*	Input Power Stage 2 D	Approximately 0.167 X In/8 (e.g. 0.167 X 0.5 X 60/8 = 1.25V)	
45 U15-1 U14-1*	-IMON	-0.167 X Input current (e.g., .167 X 60 = -10.02V)	
0.10 1 0111			

Note: Pin Numbers on 60504A are marked by *.

Table 3-10 Secondary Microprocessor Signature Analysis

Description: These signatures check secondary microprocessor U301 and latches U302 and U330. The signatures are valid for U301 firmware revisions "Rev A.01.01" and "Rev A.01.02". Use the test setup described in "Test Setup for S.A."

Signatures:

Front Panel Display = "INPUT DWN"

	U301	U30Q	U330
+ 5V	U301-7,4,9,21,39 = 1CAU	U302-20 = 1CAU	U330-20 = 1CAU
Common U301-1		U302-10	U330-10
SPCLR	U301-6 = 1CAU+5V	U302-1 = 1CAU+5V	U330-1 = 1CAU+5V
1 MHz	U301-40		
SD(7)	U301-30 = 674O	U302-14 = 674O	U330-4 = 674O
SD(6)	U301-31 = FPOU	U302-17 = FPOU	U330-17 = FPOU
SD(5)	U301-32 = O343	U302-13 = O343	U330-13 = O343
SD(4)	U301-33 = 7792	U302-8 = 7792	U330-7 = 7792
SD(3)	U301-34 = 93AU	U302-18 = 93AU	U330-3 = 93AU
SD(2)	U301-35 = 89AA	U302-3 = 89AA	U330-18 = 89AA
SD(1)	U301-36 = 2OOF	U302-4 = 2OOF	U330-14 = 2OOF
SD(0)	U301-37 = 1P45	U302-7 = 1P45	U330-8 = IP45
	U301-8 = 1CAU+5V	U302-2 = F1HA	U330-19 = AFPF
	U301-10 = 1CAU pulsing	U302-19 = FHU1	U330-2 = 1CAU pulsing
	U301-11 = ICAU+5V	U302-16 = IUF1	U330-16 = H495
	U301-12 = OOOO pulsing	U302-15 = OOOU	U330-5 = IUP5
	U301-13 = CH72	U302-13 = P27H	U330-11 = 1CAU pulsing
U301-14 = 6471		U302-12 = 83OO	U330-12 = P6C3
	U301-15 = 21A2	U302-9 = 23AP	U330-6 = 9AFP
	U301-16 = COH6	U302-6 = 8933	U330-9 = P3U5
	U301-17 = 2UU2	U302-5 = O21U	U330-15 = C3C3
U301-18 = 7A6C			
	U301-19 = C975		
	U301-20 = 6F2F		
	U301-22 = unstable		
	U301-23 = OOOO pulsing		
	U301-24 = H65P		
	U301-25 = OOOO pulsing		
	U301-26 = 6OUC		
	U301-27 = 3964		
	U301-28 = F96O		
	U301-29 = 5O93		
	U318-5.6= OOOO		
	U318-4 = 1CAU + 5V		

Table 3-11. Main DAC, Transient DAC, Data Bus Signature Analysis (Secondary)

Description: These signatures check main DAC U320, transient DAC U321, and secondary data bus B latches U319. The signatures are valid for U301 firmware revisions "Rev A.01.01" and Rev A.01.02". Use the test setup described in "Test Setup for S.A.".

	U319	U320	U321	
	U319-20 = 1CAU + 5V	U320-20 = +15V	U321-20 = +15V	
Common	U319-10	U320-1,3,10,12,18	U321-1,3,10,12,18	
SPCLR	U319-1 = 1CAU + 5V			
SD(0)	U319-7 = IP45			
SD(l)	U319-13 = 2OOF			
SD(2)	U319-14 = 89AA			
SD(3)	U319-8 = 93AU			
SD(4)	U319-4 = 7792			
SD(5)	U319-3 = 0343			
SD(6) SD(7)	U319-18 = FPOU U319-17 = 674O			
SD(7)	0319-17 - 0740			
SDB(0)	U319-6 = 55U3	U320-7 = 55U3	U321-7 = 55U3	
SDB(l)	U319-12 = 43AA	U320-6 = 43AA	U321-6 = 43AA	
SDB(2)	U319-15 = F421	U320-5 = F421	U321-5 = F421	
SD8(3)	U319-9 = 9CP2	U320-4 = 9CP2	U321-4 = 9CP2	
SDB(4)	U319-5 = OOFH	U320-16 = OOFH	U321-16 = OOFH	
SDB(5)	U319-2 = O6OO	U320-15 = O6OO	U321-15 = O6OO	
SDB(6)	U319-19 = 3U83	U320-14 = 3U83	U321-14 = 3U83	
SDB(7)	U319-16 = OO1U	U320-13 = OO1U	U321-13 = OO1U	
	U319-11 = P8OC			
		U32-2 = 21PA	U321-2 = 868H	
		U320-17 = 61F4	U321-17 = 61F4	
		U320-19 = 6F2F	U321-19 = 1CAU + 5V	
		U318-10 = 61F4		
		U318-8 = 7A6C		
		U318-12 = IUP5		
		U318-2,3,5,6,7,9,13 = OOOO		
		U318-1,4,11,14 = 1CA		

Table 3-12. Transient Generator Signature Analysis (Secondary)

Description: These signatures check transient generator IC's U310 through U316. The signatures are valid for U301 firmware revisions "Rev A.01.01" and "Rev A.01.02". Use the test setup described in the "Test Setup for S.A.".

+5V = 1CAU Common	U312-16 U312-8	U313-10,16 U313-8	U310-16 U310-8	U311-16 U311-8	U314-10,15,16 U314-3,8	U316-14 U316-7
Common	0312 0	0313-0	0310 0	0311-0	0314 3,0	0310 7
SD(0)		U312-15	= 1P45		U313-15 =	= 1P45
SD(1)		U312-1 =			U313-1=2	
SD(2)		U312-2 =			U313-2 =	
SD(3)		U312-3 =	93AU		U313-3 =	93AU
SD(4)		U312-4 =	7792		U313-4 =	7792
SD(5)		U312-5 =	0343		U313-5 =	0343
SD(6)		U312-6 =	FPOU		U313-6 =	FPOU
SD(7)		U312-7 =	6740		U313-7 =	674O
			1CAU pul		U313-9 =	84U8
			= 1CAU pu	ılsing		
		U312-11			U313-11 =	
		U312-12			U313-12 =	
		U312-13			U313-13 =	
		U312-14	= 84U8		U313-14 =	= 1CAU pulsing
U310-10 = 1 MHz		U314-1 = 1CAU		-	U314-9	9 = 6CH5
U310-11 = OOOO pulsing		U314-2 = 9AFP			U314-10 = 1CAU + 5V	
	1 0	U314	1-3 = OOO()	U314-	11 = 9U57
U311-9 = OOOU		U314-4 = 1CAU pulsing		pulsing	U314-U - OOOO pulsing	
U311-10 = IUF1		U314-5 = 1CAU			U314-13 = 5895	
U311-11 = 83O	O	U314-6 = OOOO)	U314-14 = 1CAU pulsing	
		U314	1-7 = 707A		U314-	15 = 1CAU + 5V
U315-1 = 1CAU	I nulsing	11316	5-1 = 84U8		11316-9	8 = 9AFP
U315-2 = OOOO pulsing		U316-2 = OOOO		U316-9 = 84U8		
U315-10 = OOOO pulsing U316-3 = 9U57		,	U316-10 = 9U57			
U315-11 = 1CA			6-4 = 9U57			11 = OOOO pulsing
0313-11 1CA	o puising		6-5 = 84U8			12 = OOOO pulsing
			6-6 = 84U8			13 = 1CAU pulsing
		0310	, 0 0 0 0 0		0310-	15 16/16 puising

Table 3-13. Readback, Slew Rate, Analog Switch Signature Analysis (Secondary)

Description: These signatures check the readback DAC U322, slew rate decoder U345, and analog switch U346. The signatures are valid for U301 firmware revisions "Rev A.01.01" and "Rev A.01.02". Use the test setup described in "Test Setup for S.A.".

3			
+ 15V - 15V			U346-13 U346-4
+5V	U322-20= 1CAU	U345-1,20 = 1CAU	U346-12= 1CAU
Common	U322-1,3,10,12	U345-10	U346-5
+ 12VREF	U322-8	0343-10	0340-3
1 12 V KL1	0322-0		
SD(0)	U322-7= 1P45		
SD(1)	U322-6 = 2OOF		
SD(2)	U322-5 = 89AA		
SD(3)	U322-1 = 93AU		
SD(4)	U322-16 = 7792		
SD(5)	U322-15 = O343		
SD(6)	U322-14 = FPOU		
SD(7)	U322-13 = 674O		
, ,			
WR1/WR2	U322-2,18 = UFP7		
B1/B2/XFER	U322-17,19 = C975		
SDB(0)		U345-3 = 55U3	
SDB(1)		U345-4 = 43AA	
SDB(2)		U345-7 = F421	
SDB(3)		U345-8 = 9CP2	
SDB(4)		U345-13 = OOFH	
SDB(5)		U345-14 = O6OO	
SDB(6)		U345-17 = 3U83	
SDB(7)		U345-18 = OO1U	
SLW1		U345-2 = OPAC	U346-8 = OPAC
		U345-5 = 1087	
SLW2		U345-6 = 6U88	U346-9 = 1087
SLW3			U346-16 = 6U88
SLW4		U345-9 = O337	U346-1 = O337
CLK		U345-11 = H53P	
İ			

Table 3-14. Chip Select, Status Readback, EEPROM Decoder Signature Analysis (Secondary)

Description: These signatures check the chip select IC U304, the status readback IC U303, and EEROM decoder U341 The signatures are valid for U301 firmware revisions "Rev A.01.01" and "Rev A.01.02". Use the test setup described in the "Test Setup for SA".

Signatures:

+5V Common	U303-16 = 1CAU U303-8		U304-6,16 = 1CAU U304-5-8	U341-20 = 1CAU U341-10,13,15,17
SD(0) SD(1) SD(2) SD(3)	U303-10 = 1P45 U303-13 = 2OOF U303-9 = 89AA U303-1 = 93AU	S0 S1 S2	U304-1 = CH72 U304-2 = 6471 U304-3 = 21A2	
LCLR X UNREG OV OP STAT_EN	U303-4,6,12,14 = 8933 U303-3 = 1CAU pulsing U303-11 = unstable U303-7 = 1CAU +5V U303-15 = 1CAU+5V U303-5 = P6C3	CS0 CS1 CS2 CS3 CS4 CS5 RCK_LOW RCK_HI STB	U304-15 = 21PA U304-14 = 868PA U304-13 = H53P U304-12 = UFP7 U304-11 = P8OC U304-10 = P27H U304-9 = 6746 U304-7 = 48U7 U304-4 = COH6	
SD(0) SD(1) SD(2) SD(3) SD(4) SD(5) SD(6) SD(6) SD(7)	U341-2 = IP45 U341-4 = 200F U341-6 = 89AA U341-8 = 93AU U341-9 = 7792 U341-7 = O343 U341-5 = FPOU U341-3 = 6740			U341-1 = 1CAU +5V U341-11 = 1CAU +5V U341-12 = 1CAU +5V U341-14 = OOOO U341-16 = 1CAU +5V U341-18 = 1CAU +5V U341-19 = 1CAU +5V

DAC Circuits Troubleshooting (Figure 3-3)

These circuits generate the SLEW signal which controls the input power stages. This analog signal is produced by the combined outputs from the main DAC/amplifier (U320/U326)and the transient DAC/amplifier (U321/U325). The DACs/amplifiers convert the data on bus lines SDB0-7 into analog signals.

The HIGH signal (active LO) from the transient generator (see Figure 3-7) closes switch U309 causing the output of the transient/DAC amplifier to be combined with the output from the main DAC/amplifier. The resulting SLEW signal is sent to the input power control circuit via inverting amplifier U324 and the slew circuits (see Figure 3-4).

The SLEW signal is also read back to microprocessor U301 via comparator U327. Readback DAC/amplifier U322/U328 converts the data on bus lines SD0-7 into a reference signal that allows the microprocessor to successively approximate the value of the SLEW signal. The SLEW readback signal is used during selftest to determine if the DACs are operating properly.

To troubleshoot the DAC circuits, place the Electronic Load in the SA mode by connecting the jumpers in test headers TP201 and TP301 in the SA mode positions (see Figure 3-2). The waveforms shown in Figure 3-3 can only be generated when the SA mode is on.

First, check that the SA waveforms shown on Figure 3-3 are correct. If these waveforms are not correct, check the SD0-7 data bus lines to the readback DAC U322 using SA Tables 3-10 and 3-13. Next, check the SDB0-7 data lines to the main (U320) and transient (U321) DACs using SA Table 3-9. If there is a problem on the data lines, SA should isolate the problem to the faulty component.

If the unit has failed selftest by reporting an error 105-108 at turn-on and no problem can be found using SA, the IMON adjustment may be at fault. Refer to "POST REPAIR CALIBRATION" and perform the IMON Adjustment.

Also, check if the switches in U309 are operating properly. Turn off the SA mode by removing the jumpers. Now check test points ② ,② and, ② using the measurement conditions specified in Table 3-3. A switch should close when the applicable test point is a Low level. If the switches are operating properly, check test points ④ (-IMON), ② (-10V), and ③ (-VMON).

If all signatures and test points check out, the DAC or amplifier that is generating the incorrect waveform is probably faulty.

Slew Circuit Troubleshooting (Figure 3-4)

This circuit consists primarily of three operational amplifier stages (U306 and U307) and four analog switches (U346). The four switches determine the slew rate by selecting loop gain and response time combinations. The switches are controlled by the SLW1-SLW4 signals to provide 12 slew rates.

To troubleshoot the slew circuit, place the Electronic Load in the SA mode by connecting the jumpers in test headers TP201 and TP301 in the SA mode positions (see Figure 3-2). The SA waveforms at the top of Figure 3-4 can only be generated when the SA mode is on. If the SA waveforms are incorrect, check the SDB0-7 data inputs to U305 and the SLW signal outputs from U305 using SA Table 3-13. If the signatures are correct, an amplifier or switch is probably defective.

The waveforms at the bottom of Figure 3-4 are generated when various slew rates are programmed. These waveforms check the operation of the slew circuit switches (U317). They are not generated in the SA mode. To generate these waveforms, turn the SA mode off (remove jumpers) and program 3 different slew rates (.001, 0.5 and 2.5 A/ μ s) from the front panel as shown in the following sequence. Use a scope with delayed sweep to verify the waveforms shown for slew rate in Figure 3-4.

```
MODE = CURR
CURR = 5
Tran Level = 10
Freq = 80
Dcycle = 50
Tran on/off = on
Slew = .001 (Slew Rate #1)
Slew = .5 (Slew Rate #9)
Slew = 2.5 (Slew Rate #11)
```

The three slew rates programmed from the front panel toggle all four switches in the slew circuit. Refer to the following table if you need to check the state of the switches for a specific slew rate. Remember that the front panel is programmed in microseconds. Note that when the SLW signal is LO, the switch it closed; when the SLW signal is HI, the switch is open. If the slew rate tests check out, and a problem still exists, troubleshoot the CC/CV control circuits as described in the next section.

SLEW RATE SWITCH SETTINGS

Refer to Module Operating Manual for Slew Rate Steps				
Slew Rate	SLW1	SLW2	SLW3	SLW4
#1	HI	HI	LO	HI
#2	HI	LO	LO	HI
#3	LO	HI	LO	HI
#4	HI	HI	HI	HI
#5	HI	LO	HI	HI
#6	LO	HI	HI	HI
#7	HI	HI	LO	LO
#8	HI	LO	LO	LO
#9	LO	HI	LO	LO
#10	HI	HI	HI	LO
#11	HI	LO	HI	LO
#12	LO	HI	HI	LO

CC/CV Control Circuit Troubleshooting (Figure 3-5)

Depending upon which operating mode (and range in the CR mode) is selected, either the CC or the CV loop controls the conduction of the input power stages. If the CC or CR (middle and high ranges only) mode is selected, the CC_EN signal goes low connecting the SLEW signal to the CC control circuit (U308, U16). If the CV or CR (low range only) mode is selected, the CV_EN signal goes low connecting the SLEW signal to the CV control circuit (U308, U13).

The overvoltage (OV) circuit (U17, D17) is also shown on Figure 3-5. When an OV condition is detected, the OV circuit generates a negative signal via diode D17 which causes the input power stages to increase current flow in order to limit the input voltage. The OV condition is detected when the input voltage exceeds 75V. When activated the OV circuit takes control from the CC or CV control circuit.

To troubleshoot the CV or CC circuits, place the Electronic Load in the SA mode by connecting the jumpers in test headers TP201 and TP301 in the SA mode positions (see Figure 3-2). The waveforms shown in Figure 3-5 can only be generated when SA mode is on. If the waveforms are correct but a problem exits, troubleshoot the input power stages as described in the next section.

If the waveforms are incorrect, turn off the SA mode (remove jumpers) and check that the CC and CV switches in U340 are operating properly. If the \overline{CC} EN or \overline{CV} EN input is LO, the applicable switch should be closed. You can use SA Table 3-10 to check the \overline{CC} EN and \overline{CV} EN signals. Next, check test points 27 through 31 using the measurement conditions specified in Table 3-3. Also, check test points 32 (- VMON), 45 (- IMON), and 46 (+ 12V ref).

If both the CC and CV control loops have problems, there may be another circuit affecting the CC and CV circuits. Troubleshoot the input power stages, current limit, and power limit circuits as described in subsequent sections.

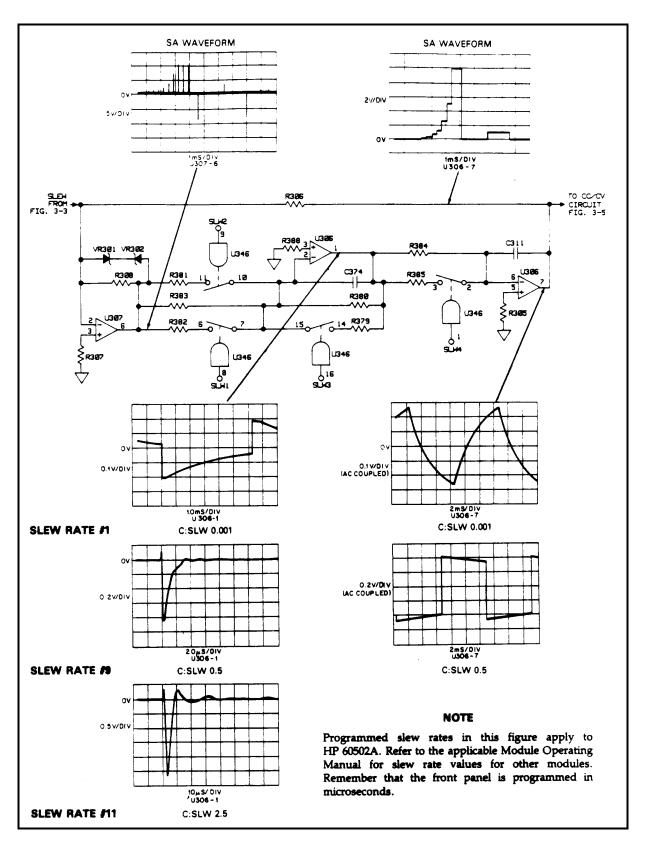


Figure 3-4. Slew Circuits Troubleshooting

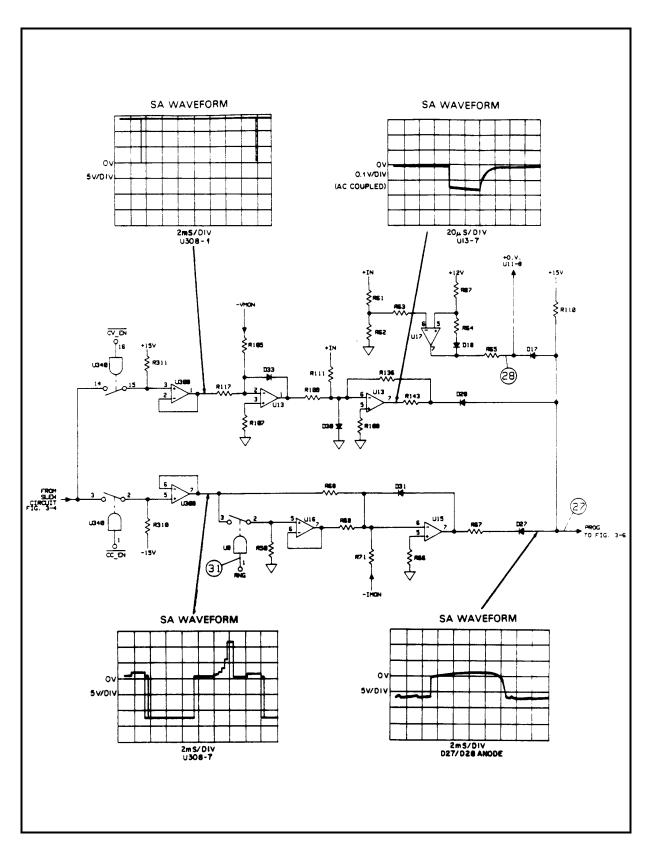


Figure 3-5. CC/CV Control Circuits Troubleshooting

Input Power Stages Troubleshooting (Figure 3-6)

There are four, eight or sixteen identical input power stages (depending on the module) connected in parallel Figure 3-6 shows one, which consists primarily of a power FET (in quad array Q2), a monitor amplifier (U6) and an error amplifier (U5). Schematic details are shown in the corresponding module Power Board schematics.

To troubleshoot the input power circuits, place the Electronic Load in the SA mode by connecting the jumpers in test headers TP201 and TP301 in the SA mode positions (see Figure 3-2). The waveform shown in Figure 3-6 at the output of the error amplifier can only be generated in the SA mode. Check that this waveform appears at the output of the error amplifier in each input power stage. Refer to the Power Board schematic to locate the output pin of each error amplifier. Checking each stage may isolate the problem to a specific stage.

If the problem is isolated to a specific stage, turn the SA mode off (remove jumpers) and check the test points (41) through that correspond with applicable circuit points in the defective stage. Use the measurement conditions specified in Table 3-3. Also, check the applicable fuses in the specific stage. As shown in Figure 3-6, fuses F5 and F13 are used by stage Q2D.

If all stages have a problem, check test points 32 and 45 (see Table 3-3). Also, check voltage suppressor (VR28) and diode (D56) which are connected across the + and - INPUT terminals. Make sure that SENSE switch S1 on the rear panel is set to the LCL position if remote sensing is not being used.

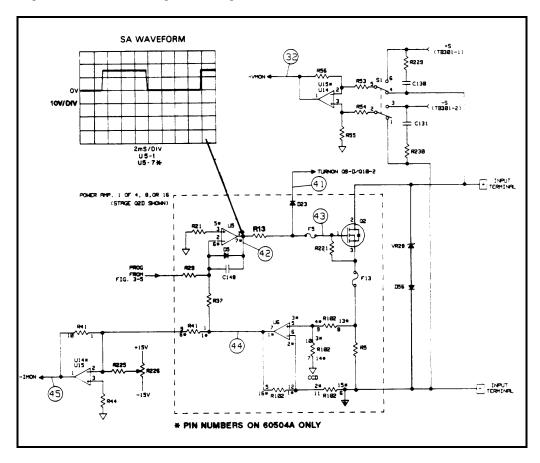


Figure 3-6. Input Power Stages Troubleshooting

Transient Generator Troubleshooting (Figure 3-7)

The transient generator (U310-U316) allows the input power stages to switch between two load levels. It produces the HIGH control signal which is sent to the DAC circuits to switch the transient DAC output.

Troubleshooting the transient circuit consists of checking the output of U314-7, the frequency and FSEL inputs to U311, the trigger inputs to U311 and U314, and the outputs of U312 and U313.

To check the output of U314, turn the transient mode on from the front panel. With the transient mode on, check the condition of the TRANS_EN signal at test point (9) according to Table 3-3. Now use a scope and check the output frequency at U314-7. Because the frequency is determined by the programmed value, return the instrument to the factory default settings. The factory default frequency should be 1KHz with a 50% duty cycle.

If the frequency at U314-7 is incorrect or nonexistent, check the inputs and output of U311. From the front panel, program the transient frequencies according to the Frequency Selection Table. Check the output of U311-5. Check the FSEL inputs at U311 pins 11, 10, and 9.

Also, check the outputs of U312 and U313 at pin 9. With transient mode on, they should output negative going pulses at intervals equal to the inverse of the programmed frequency. For example, if 1KHz is programmed, U312-9 and U313-9 should generate negative pulses at 1ms intervals. You can use signature analysis to check the SD0-7 data lines into U312 and U313 (see Table 3-12).

To check that the transient generator is being triggered correctly, run the following program. This program continuously generates 1.5µs TRIG and TRIG signal pulses at U311-12 and U314-1. If the pulses are not generated, troubleshoot the trigger circuits as described in the next section.

10 OUTPUT 705;"TRAN:MODE PULS;TWID 1"
20 OUTPUT 705;"TRIG:SOUR BUS"
30 OUTPUT 705;"TRAN ON"
40 OUTPUT 705;"*TRG"
50 ! PAUSE
60 GOTO 10
70 END

Note:

With the PAUSE line included in the program, a trigger is generated each time you press CONTINUE.

Frequency Selection (FSEL) Table Frequency @ FSEL				
50% Duty Cycle	0	1	2	U311-5
1KHz	LO	LO	LO	500KHz
500Hz	HI	LO	LO	62.5KHz
100Hz	LO	HI	LO	15.6KHz
10Hz	HI	HI	LO	3.9KHz
5Hz	LO	LO	HI	976Hz
1Hz	HI	LO	HI	244Hz
0.25HZ	LO	HI	HI	61Hz

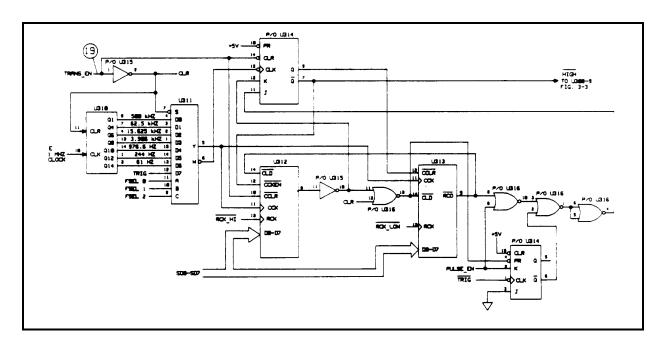


Figure 3-7. Transient Generator Troubleshooting

Overcurrent Circuit Troubleshooting (Figure 3-9)

This circuit limits the maximum current the load can sink for different input voltage and/or power conditions. The primary components in this circuit are amplifier U14 and transistors Q11 and Q12.

At power on the secondary power clear (SPCLR) signal provides a High level via D35 to drive U14-7 Low turning Q11 on. With Q11 turned on, IPROG goes High (less negative) and turns off the input power FETs (load will not sink current).

When the input voltage is approximately 6.3V or lower, diode D53 is forward biased causing voltage divider R214, R213, R59, and R58 to hold U14-6 at approximately - 7 volts. This will clamp the maximum input current capability between 60 and 70 amps

As the input voltage increases from 6.3 to 65 volts, diode D53 is reverse biased and the input voltage will appear across the voltage divider. This causes the voltage at U14-6 to decrease from - 7 volts to - 0.8 volts. At an input of 65 volts, diode D54 turns on and holds U14-6 at - 0.8 volts and limits the maximum input current capability to less than 9 amperes.

When the input voltage reaches 75 volts the OV circuit goes to -13 volts and pulls IPROG Low (more negative) via diode D17. The input power stages will now attempt to sink more current and decrease the input voltage. If the combination of input voltage and current (power) is greater than the power stages can sink when OV condition occurs, the overpower circuit (see next paragraph) will override the OV circuit and limit the maximum current capability of the load.

The -15VX bias voltage is a delayed bias derived from the normal -15V supply. When the load is first turned on, -15V is not present and U14-6 is at common potential. This causes Q11 to conduct pulling IPROG High. Q12 is also on connecting Q11 to the + 15V bias. When -15VX comes on, Q12 turns off causing U14-6 to go more negative than U14-5. This turns off Q11 allowing IPROG to go negative. VR27 supplies Q11 collector current once -15VX is available.

To troubleshoot the current limit circuit, check test points ②, ③, and ④ using the measurement conditions and readings specified in Table 3-3.

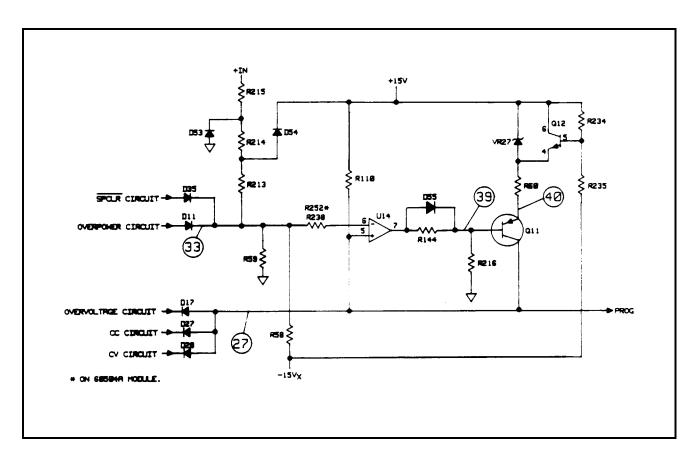


Figure 3-9. Overcurrent Circuit Troubleshooting

Overpower Circuit Troubleshooting (Figure 3-10)

This circuit limits the power sinking capability of the load to one of two different power ranges depending upon the temperature of the input power FET heat sink assembly.

The circuit monitors the input voltage and the input current in order to limit the current when an overpower condition exists. The circuit consists of amplifier U12, power select components (U9, R92-R95), and four comparators (U10) as shown in Figure 3-10. Signal levels representing the input voltage and input current are summed with a reference voltage (+12V REF) via resistors to determine if an overpower condition exists. The signal levels are scaled to allow different combinations of voltage and current (e. g., high voltage and low current, high current and low voltage, etc.) to be compared. If external power is available, the circuit increases the current and voltage limits to allow the load to operate in the extended power range. Thus, the load has two power limits, normal (300 to 396 watts) and extended (400 to 530 watts).

When extended power is unavailable, the $\overline{\text{EPC}_{EN}}$ (extended power capability enable) signal is false (High) and the EPU (extended power unavailable) bit 9 in the status register is true. When extended power is available, the $\overline{\text{EPC}_{EN}}$ signal is true (Low) and the EPU bit is false. To check the EPU bit, send the string "STAT:CHAN:COND?".

When the overpower circuit is active (limiting input power capability), the comparator circuit becomes a relaxation oscillator and output voltage will go between -14 volts and 0 volts (see waveform at test point 34 on Figure 3-10).

Troubleshooting the power limit circuit consists of checking test points 3 through 3 using the measurement conditions and readings specified in Table 3-3.

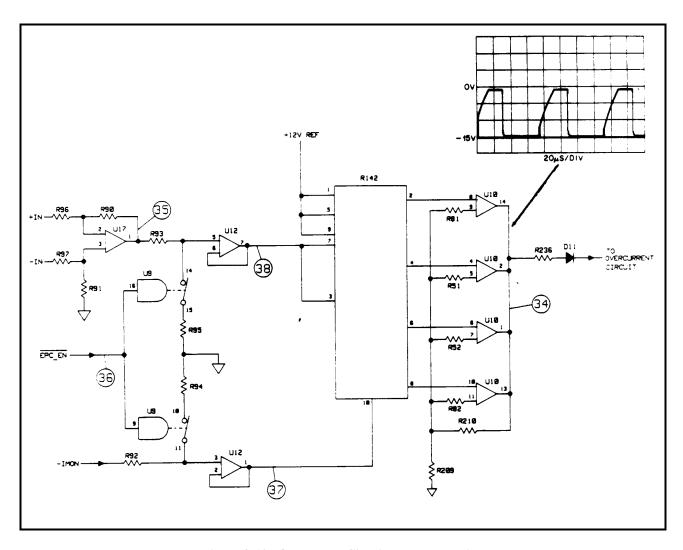


Figure 3-10. Overpower Circuit Troubleshooting

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