# DisplayPort™

# Standard

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# Agilent MOI for DisplayPort PHY CTS 1.2b Sink Tests Using J-BERT N4903B and Calibration Using DSA90000A/X/Q Series Oscilloscopes



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# **1 MODIFICATION RECORD**

Version	Date	Comments	
Version 0.83	Nov 7, 2012	Initial Draft for VESA Test Implementation Group Review	
Version 0.84	Dec 6, 2012	Formatting changes	
Version 0.85	Jan 7, 2013	Removed TTC requirements on HBR2 crosstalk signals	
		Changed to TTC range for RBR, HBR and HBR2 victim signal	
		Added tolerance bands to eye height without cross talk for HBR2	
		Introduced averaging of multiple scope measurement results to all calibration steps	
		Added appendix for RBR ISI and eye height measurements	
		Added appendix for test automation	
		Added Andreas Pfau and Carmen Manzanero-Martin from BitifEye to Acknowledgement list	
Version 0.9 Feb 25, 2013 Added requirer Added E Appe Added F Apper		Removed requirement to calibrate eye opening per SJ frequency	
		Added requirement to calibrate eye opening per lane	
		Added E Appendix: ISI adjustment using de-emphasis	
		Added F Appendix: Use of other receptacle fixtures	

# 2 INTRODUCTION

These Methods of Implementations describe the step-by-step calibration and procedures to perform DP 1.2b sink tests of the VESA DisplayPort Logo Compliance Program using the Agilent J-BERTN4903B and DSA90000A/X/Q Series Oscilloscopes. Other Stressed Signal Generators can be used as long as below calibration procedures can be performed. This procedure is in conformance with the PHY Compliance Test Specification (CTS) 1.2b. Sink tests are required to qualify a Sink product or silicon building block for Logo certification and listing on the DP Integrators List.

Formally, each test description in the CTS contains the following sections:

**Test Objective** 

**Interoperability statement** 

**Test conditions** 

Measurement requirements and

Pass/fail criteria

This MOI reduces the CTS test description to practice using the specified test equipment and procedures in an effort to standardize testing across ATCs and equipment manufacturers who perform their own certification measurements.

# 3 REFERENCES

The following documents are referenced in this text:

[1] DP PHY CTS Revision 1.2b

Once reviewed and approved by VESA, the most current versions of the CTS can be found at: <a href="http://www.vesa.org/join-vesamemberships/member-downloads/">http://www.vesa.org/join-vesamemberships/member-downloads/</a>

# **4** ACKNOWLEDGEMENTS

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# Sink Jitter Tolerance Test (4.1)

# 6 **Pre-test Procedures:**

Prior to making any measurements, the following steps must be taken to assure accurate measurements: Allow a minimum of 45 minutes warm-up time for oscilloscope and J-BERT N4903B Ensure the oscilloscope and skew is calibrated per Agilent's user documentation on calibration. Make sure you use a torque wrench with the proper torque specification to make all SMA connections.

# 7 Test Objective

The DisplayPort PHY CTS 1.2b Section 4 outlines the requirements for Sink testing.

# 8 Test Conditions

Refer to Section 4.1.3 of the PHYCTS 1.2b for the verbose details of the test conditions. Table 1 below is a summary of these conditions for each data rate.

Stressed Eye Parameter	RBR	HBR	HBR2	
Transition Time Converter (TTC) Value for Main Link Stressed Signal	The value of the transition time converter used for the main link depends on the channel + TTC combination used to achieve the required compliance interconnect channel ISI, see 9.1.			
Transition time for crosstalk signals, measured at TP3	150ps (10% to 90%)	150ps (10% to 90%)	>50ps (10% to 90%)	
Bit Rate	1.62Gb/s	2.7Gb/s	5.4Gb/s	
Calibration Test Point	TP3	TP3_Eq	TP3_Eq	
Test Signal Pattern	127 Bit PRBS7	127 Bit PRBS7	CP2520	
			(PHY1.2Bb CTS Appendix A Pattern 1)	
Compliance	570mUI +/-5%	161mUI +/-5%	220mUI +/-5%	
(CIC) ISI	at TP3	at TP3_EQ	at TP3_EQ	
	(use N4915A-006)	(use JBERT-B Opt. J20)	(use JBERT-B Opt. J20)	
RJ (RMS)	8.1mUI	13.5mUI	16.7mUI	
SJ <sub>FIXED</sub> @ 200MHz	NA	NA	100mUI	
SJ <sub>SWEEP</sub> Approximate				
2MHz	981mUI	904mUI	505mUI	
10MHz	111mUI	225mUI	116mUI	
20MHz	80mUI	182mUI	104mUI	

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100MHz	NA	168mUI	100mUI
Calibrated Eye Height with Crosstalk	$46mV_{diff}$ +/-10%	$150 m V_{diff} + -10\%$	90mV <sub>diff</sub> +/-10%
SSC	33 KHz, triangular shape	ed, 5000 ppm down spread	
Pre-Emphasis	No	No	No
Crosstalk Pattern	D24.3 (quarter rate Clock) 405MHz Clock	D24.3 (quarter rate Clock) 675MHz Clock	D24.3 (quarter rate Clock) 1.35GHz Clock
Crosstalk Amplitude	134mV <sub>diff</sub> applied at TP3	450mV <sub>diff</sub> applied at TP3	Adjusted for proper EYE Height at TP3_EQ
FAUX Crosstalk (if DUT supports FAUX)	No	Yes	Yes
Test Time	Refer to Table 4-1 of the	CTS	

Figure 1: Table of Stressed Eye Test Conditions

# 9 Sink Test Calibration Procedure

The following Figure shows the conceptual setup as described in Figure 4-3 of the PHYCTS 1.2b.



#### Figure 2: PHY CTS 1.2b HBR/HBR2 Conceptual Setup (Figure 4-3 in PHY CTS 1.2b)

The following procedure describes step-by-step how to calibrate the stressed impairments per the PHY CTS 1.2b. Follow the steps appropriate for HBR2, HBR, and RBR. The detailed example shown is for HBR2 as specified in Table 4-4 of the PHYCTS 1.2b. Since the lanes on test fixture vary in ISI and cross talk behavior the calibration steps for ISI,  $SJ_{sweep}$  and eye opening without and with cross talk have to be done per lane.

Note: The introduction to each step is the method described in the PHYCTS 1.2b for HBR/HBR2 is in italics. The sub-steps to each numbered step are the detailed procedure. RBR calibration is very similar to HBR/HBR2 calibration except that all calibration is done at TP3 instead of TP3\_EQ, so it is described as such in each setup.

#### 9.1 ISI Verification

- 1. The SSG shall be turned on with amplitude set to differential and shall be AC coupled. An attenuator shall be used to maintain sufficiently large amplitude coming from the SSG so to stay out of the noise floor of the SSG.
  - a. Ensure J-BERT N4903B and DSA have reached temperature and have been calibrated as described in the pretest procedure above.
  - b. Make sure the J-BERT N4903B Data Signals are turned off while making connections.
  - c. Connect the following Channel for each of the bit rates from DATA/DATA# of the J-BERT N4903B:

Connected from Co	onnected from ATA/DATA# Output of DEBT D add the following	Connected from DATA/DATA#
JBERT-B, add the following components in the order listed: cor	omponents in the order listed:	Output of JBERT-B, add the following components in the order listed:
2 ea. DC Blocks 2 e	ea. DC Blocks	2 ea. DC Blocks
1 Meter Phase Matched * 1 M	Meter Phase Matched *	1 Meter Phase Matched *
ISI Channel, e.g. N4915A-006 (TP3 RBR Connections) with 150ps 20% to 80% TTCs. 1 Meter Phase Matched * 1 ea. VESA Approved DP Plug Adapter 1 ea. VESA Approved DP Receptacle Fixture 2 ea. SMA-Male to SMA-Male Adapters (or short cables if required by fixture design) Connected to CH1/CH3 of Scope 1 e Receptacle Fixture 2 ea. SMA-Male to SMA-Male Adapters (or short cables if required by fixture design) Connected to CH1/CH3 of Scope 1 e Adareq Co	<ul> <li>SI Channel, e.g.:</li> <li>24" ISI Channel (Opt. J20) with 60ps 10% to 90% TTCs in combination with Wilder plug fixture</li> <li>20" ISI Channel (Opt. J20) with 100ps 10% to 90% TTCs in combination with Agilent plug fixture</li> <li>Meter Phase Matched ables*</li> <li>ea. VESA Approved DP Plug dapter</li> <li>ea. VESA Approved DP Plug dapter</li> <li>ea. SMA-Male to SMA-Male dapters (or short cables if equired by fixture design)</li> <li>onnected to CH1/CH3 of cope</li> </ul>	<ul> <li>INICELET Hase Matched</li> <li>ISI Channel, e.g.:</li> <li>32" ISI Channel (Opt. J20) with 60ps 10% to 90% TTCs in combination with Wilder plug fixture</li> <li>28" ISI Channel (Opt. J20) with 100ps 10% to 90% TTCs in combination with Agilent plug fixture</li> <li>1 Meter Phase Matched Cables*</li> <li>1 ea. VESA Approved DP plug Fixture.</li> <li>1 ea. Wilder DP Receptacle Fixture</li> <li>2 ea. SMA-Male to SMA-Male Adapters (or short cables if required by fixture design)</li> <li>Connected to CH1/CH3 of Scope</li> </ul>

\* ISI is highly dependent on the type, length, and quality of the cables used for testing. It is recommended to adjust cable lengths or add SMA connectors to the channel as needed to 'fine tune' the ISI to the target value +/- 5%. Alternatively the ISI can be

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fine-tuned by using a channel with more loss and applied de-emphasis, see E appendix.

Note: The above table is an example of a HW setup that provides adequate ISI for the setup used during development of this MOI. The actual ISI calibration results may vary depending on J20, cables and adapters used. It is up to the user to ensure that the ISI values in the PHY CTS 1.2b for ISI are achieved and measured. You should make sure to capture the screenshot of the ISI you calibrate to and keep it with your test results for future reference. It is not required to use the J20 module. Any other combination of ISI traces and/or cables can be used as long as the ISI is within target limits.

2. Using the test pattern (PRBS7 for HBR CP2520 for HBR2), verify that the ISI measured at TP3\_EQ is equal to the ISI value in Table 4-3 of the PHY1.2B CTS for HBR and Table 4-4 of the PHY1.2B CTS for HBR2. The JMD's clock recovery shall be set to the second order clock recovery function described in Section 2.1 for this step. For RBR, use PRBS7 and calibrate ISI at TP3 without equalizer.

For RBR	For HBR	For HBR2
In the J-BERT N4903B PG > Bit Rate Setup Menu:	In the J-BERT N4903B PG > Bit Rate Setup Menu:	In the J-BERT N4903B PG > Bit Rate Setup Menu:
Select 1.620 Gb/s (DP-RBR)	Select 2.7 Gb/s (DP-HBR)	Select 5.4 Gb/s (DP- HBR2)
In Pattern > Select Menu	In Pattern > Select Menu	In Pattern > Select Menu
Select 2 <sup>n</sup> – 1, and Select 2 <sup>7</sup> -1 (PRBS7)	Select 2 <sup>n</sup> – 1, and Select 2 <sup>7</sup> -1 (PRBS7)	Select User Pattern from File.
In PG Data Output Menu:	In PG Data Output Menu:	Select Pattern
Set $V_{ampl}$ to $1V_{diff}$	Set $V_{ampl}$ to $600mV_{diff}$	C:\N4903B\Pattern\Demo
Turn on the PG Data Outputs	Turn on the PG Data Outputs	\DisplayPort\HBR2_SR-CP-
See C appendix for detailed procedure.	Use Equalizer, Serial Data and EZJIT wizards to make ISI	CP- SR248_CompEyePattern.ptrn
Repeat measurement at least 5	measurement on oscilloscope. See Appendix B for detailed	(AKA CP2520)
times and average the results.	procedure.	Press OK
Verify ISI to be 570mUI +/-5%.	Repeat measurement at least 5	Press Apply
	times and average the results.	Press OK
	Verify ISI to be 161mUI +/-5%.	In PG Data Output Menu:
		Set $V_{ampl}$ to $1V_{diff}$
		Turn on the PG Data Outputs
		Use Equalizer, Serial Data and EZJIT wizards to make ISI measurement on oscilloscope. See Appendix B for detailed procedure.
		Repeat measurement at least 5 times and average the results.

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Verify ISI to be 220mUI +/-5% as shown in the below example.
1 A

Bit Rate						
Value and Uni	ts: 5.40000	0 Gb/s DP-HE	3R2			
Preset					r	- 1
4.2500	Gb/s	4G FC		^	Add Preset	
4.992	Gb/s	MIPI-HS Gea	ar 3A			
5.0	Gb/s	USB 3.0	<u></u>		Delete Prese	et i i
5.0	GD/S		2.0			-
5.824	Gb/s	MIPI-HS Ges	ar 3B(26MHz Be	f Clk)		
5 8304	Gb/s	MIPI-HS Gea	ar 3B ar 3B			-
5.8368	Gb/s	MIPI-HS Gea	ar 3B(19.2MHz F	(ef Clk)		
6.0	Gb/s	SATA 3		,		
8.0	Gb/s	PCI Express	3.0	~		
					*	
attern Genera	ator 📕	ock Jitter/ Outp	Error Detect	or 🔳	Sync Data	Clock
Pattern Genera 40000 Gb/s 2111 Fig Select Patter	ator In PRBS Characteristics	ock Jitter/ Output SS: ISI/SSC ON J-BERT N	Error Detect 5.40000 Gb/s 2 4903B HBF	Dr 11-1 PRBS Erro 22 Bit Rat	Sync Data Loss Loss te Setup	Clock Loss
Pattern Genera 40000 Gb/s 2111 Fig Select Patter Pattern G	ator I 1 PRBS C ure 3: . n	ock Jitter/ Outp ISI/SSC ON J-BERT N	Error Detect 5.40000 Gb/s 2' 4903B HBF	or 11-1 PRBS Eno 22 Bit Rat	sync Data Loss Loss te Setup	Clock Loss
Pattern Genera 40000 Gb/s 2111 Fig Select Pattern Pattern G	ator Charles C	ock Jitter/ Outpo J-BERT N or Pattern	4903B HBF	or 11-1 PRBS Erro 22 Bit Ra	sync Data Loss Loss te Setup ? Browse	Clock Loss
Pattern Genera 40000 Gb/s 2111 Fig Select Pattern Pattern G © User F © Memo	n Pattern 1 Pattern 1 Pattern 1	or Pattern	Error Detect 5.40000 Gb/s 2' 4903B HBF	or 11-1 PRBS Eno 22 Bit Ran	, Sync Data te Setup ? Browse Pattern:	Clock Loss
Pattern Genera 40000 Gb/s 2111 Fig Select Pattern Pattern G O User F O Memo C 21n-1	n Pattern 1 Pattern 1 Pattern 1	Difference of the second secon	Error Detect 5.40000 Gb/s 2 4903B HBF	or 11-1 PRBS Eno 22 Bit Rat	pync Data te Setup ? Browse Pattern:	Clock
Pattern Genera 40000 Gb/s 2111 Fig Select Pattern Pattern G © User F © Memo © 2^n-1 © 2^n	ator 1 PRBS Ure 3: . n Generato Pattern 1 ry User	or Pattern	ttern Size	Dr 11-1 PRBS Erro 22 Bit Rat Selected F C:\N4903B\Pa DisplayPort\HI 248_CompEyef	Rowse Pattern: ttern: Browse Pattern: ttern\Demo BR2_SR-CP-CP-SF Pattern.ptm	Clock
Pattern Genera 40000 Gb/s 2111 Fig Select Pattern Pattern G O User F O Memo C 2^n-1 C 2^n C Mark I	ator Charles C	Dr Pattern	ttern Size	Dr 11-1 PRBS Erro 22 Bit Rat Selected F C:\N4903B\Pa DisplayPort\HI 248_CompEyef	Rowse Pattern: ttern Pattern Pattern,ptm	Clock
Pattern Genera 40000 Gb/s 2111 Fig Select Pattern G O User F O Memo O 2^n-1 O 2^n O Mark I	ator 1 PRBS Qure 3: 4 Qure 3: 4 Quenerator Pattern 1 ry User Density	Der Pattern	ttern Size	Dr 11-1 PRBS Erro 22 Bit Rat Selected F C:\N4903B\Pa \DisplayPort\H1 248_CompEyef	Browse Pattern: ttern\Demo BR2_SR-CP-CP-SP Pattern.ptm	Clock
Pattern Genera 40000 Gb/s 2111 Fig Select Pattern Pattern G O User F O Memo O 2^n-1 O 2^n Mark I 1/2	ator 1 PRBS <b>ure 3:</b> <b>n</b> Generator Pattern 1 ry User Density	Der Pattern	ttern Size	or 11-1 PRBS Eno 2 Bit Rat Selected F C:\N4903B\Pa \DisplayPort\H1 248_CompEyef	Browse Pattern: ttern\Demo BR2_SR-CP-CP-SP Pattern.ptm	Clock
Pattern Genera 40000 Gb/s 2111 Fig Select Pattern G © User F © Memo © 2^n-1 © 2^n © Mark I 1/2 © Zero S	ator 1 PRBS Ure 3: . 1 1 PRBS C 1 PRBS C 1 PRBS C C C C C C C C C C C C C	Dir Pattern	ttern Size	Selected F C:\N4903B\Pa DisplayPort\HI 248_CompEyef	Pattern.ptm Pattern.ptm	Clock Loss
Pattern Genera 40000 6b/s 2111 Fig Select Pattern G © User F © Memo © 2^n-1 © 2^n © Mark I 1/2 © Zero S 13	ator 1 PRBS 2 1 PRBS 2 1 1 2 1 2 1 2 1 2 1 2 1 2 1 2 1 2 1 2 1 2 1 2 1 2 1 2 1 2 1 2 1 2 1 1 1 1 1 1 1 1 1 1 1 1 1	or Pattern	ttern Size	or 11-1 PRBS Eno 2 Bit Rat Selected F C:\N4903B\Pa \DisplayPort\H1 248_CompEyef	Browse Pattern: tern\Demo BR2_SR-CP-CP-SF Pattern.ptm	Clock Loss
Pattern Genera 4000 Gb/s 211 Fig Select Patter Pattern G O User F O Memo O 21n-1 O 21n Mark I 1/2 O Zero S 13	ator 1 PRBS 2 1 PRBS 2 1 1 1 1 1 1 1 1 1 1 1 1 1	or Pattern	ttern Size	or 11-1 PRBS Eno 2 Bit Ran Selected F C:\N4903B\Pa DisplayPort\H1 248_CompEyef	bync Data Loss Data te Setup ? Browse Pattern: ttem\Demo BR2_SR-CP-CP-SF Pattern.ptm	Clock Loss

Figure 4: J-BERT N4903B HBR2 Pattern Setup



Figure 6: J-BERT N4903B HBR2 TP3\_EQ ISI Verification

Note: In this example, the measured ISI value is 220.1mUI, small variations between the measured value and the target value of jitter will be compensated for in 9.3.2. Capture and save the screenshot of the oscilloscope measurement to demonstrate that the proper value has been achieved.

Important: In order to setup the oscilloscope for best measurements, follow the procedure in B appendix. It is important to get the vertical signals properly scaled without clipping before applying Ch1-Ch3 function and equalization.

#### 9.2 RJ Calibration

- 1. Calibrate Rj(rms) using D24.3 pattern with JMD using constant clock at TP3\_EQ. For RBR, measure at Rj at TP3.
  - a. In Pattern > Select Pattern Menu:
    - Select User Pattern from File.
    - Select Browse
    - Select Pattern:

C:\N4903B\Pattern\Demo\DisplayPort\D24.3.ptrn

Select Pattern 🔹 🔀	
Pattern Generator Pattern	
© User Pattern from File Browse	
C Memory User Pattern 1 Selected Pattern:	
C 2^n-1 Pattern Size - c:\N4903B\Pattern\Demo	
C 2^n	
C Mark Density PRBS	
13	
C Sequence	
Error Datactor Pattern tracks the Pattern Generator Pattern	
<u>O</u> K <u>C</u> ancel <u>A</u> pply <u>H</u> elp	

Figure 7: J-BERT N4903B D24-3\_Clock Pattern

b. In the J-BERT N4903B Jitter > Jitter Setup Menu, disable all jitter terms accept RJ

	Menu -11 -10 Jitter Jitter on/off	ER: not av -9 -8 -7 -6 er Setup 2 % ss	railable . 5 -4 -3 -2 -1 0 ) ;C/SJ	Elapsed I	00:00:00 610ps	Error A	0.15 UI	220p:	Rem	- ote 1.188
	ssc 💋	Deviation 0.5 %	Frequency 33.00 kHz			Data & Aux Data	Trigge Ref. C	r & lock	Clock -	
	sj 💋	Amplitude 0 mUI	Frequency 500 Hz			SSC/SJ	-	SSC/S	53	
	PJ 1 💋	Amplitude 100 mUI	Frequency 100.0000 MHz			610ps	Delay		220.	
•	PJ 2 💋	Amplitude 116 m∪I	Frequency 10.0000 MHz			_220ps	en ha	τ	22up	5
	BUJ 💋	Amplitude 0 mUI					_−Config	uration -		_
	RJ 💋	Amp rms 11 m∪I	Amp p-p 154 mUI					SSC	rSSC	1
	Ext 💋	Ampinade (i 1.034 UI	nex) 479 mV				R	3/BUJ	sRJ	1
	Pattern Gen 5.40000 Gb/s D	erator 24.3	Clock Jitter/ Loss ISI/SSC	Outputs ON	Error Dete 5.40000 Gb/s	ctor D24.3	Error	Sync Loss	Data Loss	Clock Loss

Figure 8: J-BERT N4903B HBR2 RJ Adjustment

c. In the oscilloscope, using the Analysis > Serial Data > Clock Recovery menu, change the clock recovery from 2nd Order PLL to Constant Frequency.



#### Figure 9: Constant Frequency CDR for RJ and SJ Calibration

d. Alternate between adjusting RJ on the J-BERT N4903B user interface and press the Single Acquisition Button on the Oscilloscope until the RJ is calibrated to the following values.

For RBR	For HBR	For HBR2
Adjust RJ to 8.1mUI RMS Repeat measurement at least 3 times and average the results.	Adjust RJ to 13.5mUI RMS Repeat measurement at least 3 times and average the results.	Adjust RJ to 16.7mUI RMS, 200mUI Pk-Pk (16.7 RMS x 12.0)
		Repeat measurement at least 3 times and average the results.



Figure 10: HBR2 RJ Measurement

Note: In this example, the measured RJ value is 16.4mUI RMS. The measured RJ is multiplied by 12.0 to reach the  $10^{-9}$  BER value in the specification to use for the correction in 9.3.1. In this case, this is  $16.4 \times 12.0 = 196.8$ mUI.

#### 9.3 SJ Calibration

#### 9.3.1 SJ<sub>FIXED</sub> Calibration

- 1. For HBR2 only, Calibrate SJ<sub>FIXED</sub> using D24.3 pattern with JMD using constant clock at TP3\_EQ.
  - a. In the J-BERT N4903B Jitter > Jitter Setup Menu, disable all Jitter terms accept PJ 1
     b. Set the frequency in PJ 1 to 200MHz.



Figure 11: J-BERT N4903B HBR2 SJ<sub>FIXED</sub> Adjustment

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c. Alternate between adjusting PJ 1 on the J-BERT N4903B user interface and pressing the Single Acquisition Button on the Oscilloscope until the PJ<sub>(d-d)</sub> is calibrated to the following values.

For RBR	For HBR	For HBR2
NA	NA	Adjust PJ 1 to 100mUI as shown in the below example
		Repeat measurement at least 3 times and average the results.



Figure 12: J-BERT N4903B HBR2 SJ<sub>FIXED</sub> Measurement

Note: In this example, the measured PJ value is 101.2 mUI.

#### 9.3.2 SJ<sub>SWEEP</sub>

1. Calibrate SJ<sub>SWEEP</sub> at each frequency with JMD using constant clock at TP3\_EQ. Note: To account for small inaccuracies in measurement of ISI, RJ and SJ<sub>FIXED</sub> compared to the spec, the SJ<sub>SWEEP</sub> should be adjusted as follows to ensure correct TJ at TP3\_EQ:

For HBR:  $SJ_{SWEEP} = SJ_{SWEEP}$  (Table 4-3)\*(1 + (323mUI - measured\_mUI(ISI + RJ))/168mUI). For HBR2:  $SJ_{SWEEP} = SJ_{SWEEP}$  (Table 4-4)\*(1 + (520mUI - measured\_mUI(ISI + RJ + SJ\_{FIXED}))/100mUI).

#### Notes:

RJ in this formula is  $Pk-Pk = 12.0 \times RJ(rms)$ . In the above equations, the denominator of the measurement error correction (168mUI for HBR and 100mUI for HBR2) is equivalent to the high frequency  $SJ_{SWEEP}$  value in

Tables 4-3 and 4-4 of the CTS. The error term is divided by the HF jitter amplitude to account for effect of the equalization and jitter transfer function at TP3 EQ.

a. For HBR and HBR2, Calculate the required SJ<sub>SWEEP</sub> target value based on the equation above using the measured values from 9.1, 9.2 and 9.3.1.

f(SJ)	<b>TJ(JTHBRrx</b> )	ISI	RJ(RMS)	Approximate SJ <sub>SWEEP</sub>
[MHz]	[mUI]	[mUI]	[mUI]	[mUI]
2	1227	161	13.5	904
10	548	161	13.5	225
20	505	161	13.5	182
100	491	161	13.5	168

Table 4-3: Jitter Component Settings for High Bit Rate

Table 4-4: Jitter Component Settings for High Bit Rate 2							
f(SJ)	TJ(JTHBR2rx)	ISI	RJ(RMS)	Approximate SJ <sub>SWEEP</sub>	SJ <sub>FIXED</sub> @ 200MHz		
[MHz]	[mL0]	[mL1]	[mL11]	[mLil]	[mL1]		
2	1026	220	16.7	505	100		
10	636	220	16.7	116	100		
20	624	220	16.7	104	100		
100	620	220	16.7	100	100		

#### Figure 13: Table 4-3 and 4-4 from the PHY CTS 1.2b

For this example, the target value for SJ<sub>SWEEP</sub> is calculated as follows:

 $SJ_{SWEEP(2MHz)} = 505 * (1 + (.520 - (220+197+101))/100) = 505 * 1.02 = 515$  $SJ_{SWEEP (10MHz)} = 116 * (1 + (.520 - (220+197+101))/100) = 116 * 1.02 = 118$  $SJ_{SWEEP(20MHz)} = 104 * (1 + (.520 - ((220+197+101)))/100) = 104 * 1.02 = 106$  $SJ_{SWEEP (100MHz)} = 110 * (1 + (.520 - ((220+197+101)))/100) = 110 * 1.02 = 112$ 

- b. In the J-BERT N4903B Jitter Setup menu, disable all Jitter terms accept PJ 2.
- c. Set the frequency for PJ 2 to 10 MHz.
- d. Alternate between adjusting the PJ 2 on J-BERT N4903B user interface and pressing the Single Acquisition Button on the Oscilloscope until the PJ<sub>(d-d)</sub> is calibrated to the following values.

For RBR	For HBR	For HBR2
Correction factor for $SJ_{SWEEP}$ does not apply. Use the equation below to arrive at the target value for PJ 2.	Adjust PJ 2 to the new target value based on the calculations made above.	Adjust PJ 2 to the new target value based on the calculations made above.

Henry -11-10 -3 -8 -7 -6 Jitter Setup Jitter on/off	vailable -5 -4 -3 -2 -1 0 D SC/SJ	Elapsed 0.00 UI	00:00:00 610ps	Error A	.dd 0.12 UI	220ps		
SSC 2015 %	Frequency 33.00 kHz			Data & Aux Data	Trigger 8 Ref. Cloc	k Clock		
SJ Z Amplitude	Frequency 500 Hz			SSC/SJ		SSC/SJ	-	
PJ 1 March Amplitude	Frequency 200.0000 MHz			610ps	Delay		-	
PJ 2 116 mUI	Frequency 10.0000 MHz	>		220ps	lo bs	220	ps	
BUJ Mamplitude					Configura	ation		
RJ Mmp rms	Amp p-p 154 mUI				SS	c rssc		
Ext Manual Amplitude (	max) 496 mV				RJ/B	UJ SRJ	-	
Pattern Generator			Error Dete	ctor				
5.40000 Gb/s D24.3	Clock Jitter/ Loss ISI/SSC	Outputs ON	5.40000 Gb/s	D24.3	Error Lo	nc Data ss Loss	Clock Loss	

Figure 14: J-BERT N4903B SJ<sub>SWEEP</sub> (10MHz) Adjustment





Note: In this example, the measured PJ value is 117.9mUI.

For RBR:

 $SJ_{SWEEP} = TJ - measured_mUI (ISI + RJ)$ 

#### Table 4-2: Jitter Component Settings for Reduced Bit Rate

f(SJ)	<b>TJ(JTRBRrx)</b>	ISI	RJ(RMS)	Approximate SJ
[MHz]	[mUI]	[mUI]	[mUI]	[mUI]
2	1648	570	8.1	981
10	778	570	8.1	111
20	747	570	8.1	80

#### Figure 16: Table 4-2 from the PHY CTS 1.2b

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#### 9.4 Eye Height Calibration

1. Change the pattern on the SSG to the pattern to be used for the testing:

For RBR and HBR:	PRBS7
For HBR2:	CP2520

Use the procedure in 9.1 to return to the test pattern to be used for testing on the J-BERT N4903B.

- For HBR, apply a non-phase aligned crosstalk aggressor signal (D24.3 pattern) with amplitude of 450mVdifferential (1.35V divided by 3) to TP3 as in Figure 4-3 [of the PHY1.2b CTS]. For HBR2, crosstalk aggressors will be applied in 9.4.2 below.
   For RBR, apply a non-phase aligned crosstalk aggressor signal (D24.3 pattern with amplitude of 138mV (414mV/3).
  - a. Connect 2ea. Divide by 3 RF power dividers (JFW Model # 50PD-292P) or divide by 4 power dividers (terminate unused leg) to the TRIGGER/REF-CLK DATA/DATA# and Outputs of the J-BERT N4903B using 1ea. pair of matched SMA cables.
    - b. Connect output of power dividers using 3ea. pair of SMA cables to the specified crosstalk lanes for the DUT.
    - c. Example: If Lane0 is being tested, the differential crosstalk signals are connected to Lane1, Lane2, and Lane3.



d. In the J-BERT N4903B menu go to PG Setup > Trigger/Ref Clock Setup and set Clock Output Divider to be 4 as shown below for HBR2.

PG Trigger/Reference Clock Output 🔹 👔 🔀	
Reference Clock	
Clock Output Divider 4 1.35 GHz	
C Alternate Pattern Trigger Level	
C Alternate Pattern Trigger Pulse	
C Sequence Trigger	
Pattern Trigger Position	
Bit Position (For user and 2^n Pattern)	
0	
N-bit Trigger Pattern (For 2^n-1 PRBS) (binary)	
0000000	
Shift Trigger Position	
OK Cancel Apply Help	

Figure 18: HBR2 crosstalk Setup for Trigger/Reference Clock Output

- e. In the J-BERT N4903B go to PG Setup > Clock/Jitter Output menu.
  - i. Set the Trigger Output to the following based on the data rate being testing:



Figure 19: Controlling Crosstalk Amplitude on the J-BERT N4903B

For RBR	For HBR	For HBR2
Set crosstalk amplitude to $414mV_{diff}$ .	Set cross talk amplitude to $1.35V_{diff}$ .	Set the Clock/Trigger output amplitude to 0V during this step. Crosstalk amplitude will be applied in 9.4.2.

3. If the Sink DUT supports FAUX, ensure that the DUT is transmitting FAUX traffic to emulate crosstalk during calibration.

If the device supports FAUX hook the AUX signals on the Wilder plug fixture to the DUTs FAUX signal using another adapter. Make sure FAUX signals from the DUT are signaling during the next calibration steps.

- 4. Turn on all jitter stress impairments ((ISI, RJ, SJ<sub>FIXED</sub>, SJ<sub>SWEEP</sub>, crosstalk, SSC) on the SSG.
  - a. ISI is achieved with the HW channel in Step 2.
  - b. In the JBERT-B, select Jitter Output Menu.
    - ii. Enable the RJ calibrated in9.2.
    - iii. If testing HBR2, Enable the SJ<sub>FIXED</sub> (PJ 2) calibrated in9.3.1.
    - iv. Enable the SJ<sub>SWEEP</sub> (PJ 1) at 10MHz with amplitude determined in 9.3.2.
    - v. Enable SSC with frequency of 33 KHz and 5000ppm with a triangle profile.

							r	
Menu -11 -10 -9 -8 -7 -6 Jitter Setu	vailable _ -5 -4 -3 -2 -1 0 p	Elapsed 00:00:	00	Error A	dd	ert B	- mote	
Jitter on/off 🕺 S	sc/sj	0.00 UI	610ps	1 3.294	UI	37 220ps	1.188	
SSC Z Deviation	Frequency 33.00 kHz		Da Au	ita & Ix Data	Trigger Ref. Clo	& Clock		
SJ Z Amplitude 0 mUI	Frequency 500 Hz			ssc/sj		SSC/SJ		
PJ 1 Z 100 mVI	Frequency 200.0000 MHz			610ps	Delay		-	
PJ 2 2 Amplitude 116 mUI	Frequency 10.0000 MHz		1-	220ps	lo be	220	ips	
BUJ 2 Amplitude					Configu	ration ——		
RJ Z Amp rms	Amp p-p 154 mUI				9	isc rss		
Ext 21 Amplitude (	(max) 379 mV				RJ	/BUJ SRJ	-	
Pattern Generator 5.40000 Gb/s D24.3	Clock Jitter/ Loss ISI/SSC	Outputs ON 5.400	or Detecto 100 Gb/s D2	or 4.3	Error	Sync Data Loss Loss	Clock Loss	

Figure 20: Turn On All Stressors

#### 9.4.1 Eye Height Calibration without Crosstalk

- 1. Calibrate the amplitude of the SSG to achieve an EYE Height 150mV at TP3 EQ for HBR and 120.0mV at TP3\_EQ without crosstalk for HBR2; with the JMD using the 2<sup>nd</sup> order clock recovery function described in Section 2.1 of the DP1.2a Standard.
  - a. In the J-BERT N4903B Jitter > PG Output Menu, Select the data output amplitude adjustment.

BER: not a -11 -10 -9 -8 -7 -6 PG - Data	vailable -5 -4 -3 -2 -1 0 Elapsed 00:00:00 Output	Error Add Insert B A _ Remote	1
0.5V	Viii 177 mV Vampt 353 mV Vio 0 mV VdifAmp 706 mV Vio 177 mV Xov 50 %	Termination 0 mV Logic Level Custom Output Blanking Electrical Idle	
	Both         Delay         92.6 ps           Aux Data         Vhi         0 mV           Vampt         0 mV         Vof         0 mV           VdiffAmp         0 mV         Vlo         0 mV	Polarity Inverted  Termination 0 mV Logic Level Custom Electrical Idle	
Pattern Generator	Clock Utputs 5 7355 6b/c 221	PBBS From Sync Data Clock	

Figure 21: J-BERT N4903B Differential Amplitude Adjustment

b. In the oscilloscope, using the Analysis > Serial Data > Clock Recovery menu, change the Clock Recovery from Constant Frequency to 2<sup>nd</sup> Order PLL.

Clock Recovery	
Clock recovery applies to seria	al Close
decode, serial data analysis, RJ/DJ, and TIE jitter meas.	Help
Clock Recovery Method	Advanced
Second Order PLL	•
Nominal Data Rate	
5.40000000 Gb/s	
Loop Bandwidth	
6.500002 MHz	
Damping Factor	
1.000	

Figure 22: DSA 2<sup>nd</sup> Order PLL Clock Recovery

- c. On the Oscilloscope, Select Measure > Eye > Eye Height Measurement.
- d. Alternate between adjusting the Vampl on the J-BERT N4903B user interface and pressing the Single Acquisition Button on the Oscilloscope until the Eye Height is calibrated to the following values.

For RBR	For HBR	For HBR2
Adjust Eye Height to 46mV <sub>diff</sub> +/-10%	Adjust Eye Height to 150mV <sub>diff</sub> +/-10%	Adjust Eye Height to 120mV <sub>diff1</sub> +/-10% as shown in the below
Repeat measurement at least 5 times and average the results. See C appendix	Repeat measurement at least 5 times and average the results.	example Repeat measurement at least 5 times and average the results.

Note: Capture a minimum of 1 million unit intervals with the JMD in order to achieve a repeatable EYE opening measurement. The vertical EYE height shall be measured using the same methodology as described in B appendix.



Figure 23: J-BERT N4903B HBR2 Eye Height Measurement without Crosstalk

Note: In this example, the measured PJ value is 121mV.

#### 9.4.2 Eye Height Calibration with Crosstalk

- 1. For HBR2, apply a non-phase aligned crosstalk aggressor signal (D24.3 pattern) with amplitude of 500mV differential (1.50V divided by 3) to TP3 as in Figure 4-3. Adjust the amplitude of the crosstalk aggressor signal until the EYE Height at TP3\_EQ is 90mV<sub>diff</sub>.
  - a. In the J-BERT N4903B go to PG Setup > Clock/Jitter Output menu.



Figure 24: HBR2 crosstalk Amplitude on the J-BERT N4903B

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Note: Crosstalk is highly dependent on the Receptacle fixture used.

b. Alternate between adjusting the Vamp on the J-BERT N4903B user interface and pressing the Single Acquisition Button on the Oscilloscope until the Eye Height is calibrated to the following value.

For RBR	For HBR	For HBR2
NA	NA	Adjust the Clock/Trigger Vamp Height measurement on the Scope is 90mV <sub>diff</sub> +/-10% Repeat measurement at least 5 times and average the results.



Figure 25: HBR2 Eye Height Measurement with crosstalk

- 2. At TP3, disconnect 'P' (Plug) type adapter from the 'R' (Receptacle) calibration adapter and connect the 'P' type adapter to the DUT for testing (Figure 4-4).
  - a. At TP3, disconnect 'P' (Plug) type adapter from the 'R' (Receptacle) calibration adapter and connect the 'P' type adapter to the DUT for testing (Figure 4-4).
  - b. Disconnect the Plug fixture from the calibration Receptacle fixture for the test. Refer to the Testing the DUT section below.

Note: Always calibrate for a four lane configuration even if the device under test is a single lane or two lane device. Perform the testing with aggressor signals applied on all lanes independent of the actual device configuration.

# 10 Testing the DUT

- 1. At each Frequency
  - a. Test for Frequency Lock using D10.2 pattern for each data rate.
  - b. Test for Symbol Lock using Symbol Lock pattern at each data rate and each frequency.
  - c. Inject Errors and confirm correct amount of errors is being detected.
  - d. Test the Sink at each data rate and duration as described in Table 4-1 of the PHY CTS 1.2b.

Data Rate	Jitter Frequency	Number of Bits	Max Number of Bit Errors Allowable	Observation Time <sup>1</sup> (seconds)	Data Rate Offset
HBR2 HBR RBR	2 MHz	10 <sup>12</sup>	1000	HBR2=185s HBR=370s RBR=620s	0
HBR2 HBR RBR	10 MHz	10 <sup>11</sup>	100	HBR2=19s HBR=37s RBR=62s	+350ppm +350ppm +350ppm
HBR2 HBR RBR	20 MHz	10 <sup>11</sup>	100	HBR2=19s HBR=37s RBR=62s	0
HBR2 HBR	100 MHz	1011	100	HBR2=19s HBR=37s	0
To evalua 370ps/UI * 10	te multiply numb 1 <sup>11</sup> UI = 37 secon	per of bits by ds	the unit interval in ps.	( <i>i.e.</i> for $HBR: 10^{11}$ l	bits at HBR =

#### Figure 26: Sink Test Times

# A. Appendix: Agilent Equipment List for 1.2b DisplayPort Sink Testing

- 1 ea. Agilent J-BERT N4903B with the following options:
  - Opt. G07, G13, C07 or C13 Base Option
  - Opt. J20 Interference Channel
  - Opt. J10 Jitter Sources
  - Opt. J11 SSC
- 1 ea. Agilent 90000A/X/Q Oscilloscope (12GHz or above).

Note: Appendix B shows how to create the proper setup for making calibration measurements.

- 1 ea. SMA Torque Wrench
- 3 ea. 1m SMA or 3.5mm Matched Pair Cable Sets for Stressed Signal Path, e.g. N4871A
- 4 ea. 1m SMA Cable Pairs for Crosstalk, e.g. 2x 15442A cable sets.
- 2 ea. DC Blocks e.g. N9398C
- 2 ea. 60ps 10% to 90% TTCs (Transition Time Converters), e.g. BitifEye BIT-1001-0000-0 or PSPL 5915-100-60PS
- 4 ea. 150ps 20% to 80% TTCs used for HBR and RBR for aggressor lanes and RBR victim lane setup, e.g. 15435A
- 12 ea. 2.4mm(m) to 3.5mm(f) adapters, e.g. N4911A-002
- 11 ea. SMA(m) 500hm Terminations, e.g. N4911A-004
- 2 ea. ÷3 Power Dividers (JFW Model # 50PD-292P) or ÷4 Power Dividers
- 1 ea. N4915A-006 DP ISI Generator, used for RBR testing
- 1 ea. DP Mated Adapter Pair, e.g. BitifEye BIT-1050-0045-0 or Wilder Technologies DPI-TPA-PRA
- 1 ea. DP AUX Channel Controller, e.g. Agilent W2642B or Unigraf DPT-200
- 1 ea. N5990A Test Automation Software Platform (optional) with:
  - Opt. 010 Core
  - Opt. 155 DisplayPort Receiver Test Library
- 1 ea. N4916B with Opt. STD De-emphasis Signal Converter for ISI adjustment, optional
- 1 ea. N4915A-010 Connection Cable Kit for N4916B and N4903B, required for N4916B

# B. Appendix: Agilent 90000A/X/Q Setup Steps for Sink Calibration

#### **ISI Channel Scope Setup**

The following procedure shows the Step-Step procedure for achieving the measurement results in this MOI for Sink Calibration.

1. Setup the Physical Connection for ISI as documented in 9.1 of the Calibration Procedure.

Note: The physical ISI channel changes between the bit rates supported but the general measurement procedure is the same. This Step-Step is for HBR2, but highlights what is different when calibrating HBR and RBR.

#### **Initial Scope Setup**

- 1. Press Default Setup on the Front Panel to start from a known instrument state.
- 2. Press Front Panel Auto Scale
- 3. Verify signals are symmetric on screen, set vertical to best sensitivity to make sure signals are using as much of the A/Ds range as possible without clipping. If the signal is not symmetric and looks similar to the following screenshot, check your connections until the live signal is symmetric.



**F**igure 27: Single Ended HBR2 TP3 Signals

- 4. In the Channel Setup, menu, select Differential Channels 1&3
- 5. Turn Off the Blue trace, Channel (3+1).



Figure 28: Differential HBR2 TP3 Signals

#### **Signal Equalization**

- 1. Go to Analyzer > Equalizer Menu.
- 2. Setup Equalizer as follows for HBR2 and HBR, skip this step for RBR.
  - a. For HBR2:
    - i. Data Rate = 5.4Gb/s
    - ii. Equalizer Type = CTLE
    - iii. # of Poles = 3
    - iv. DC Gain = 1.0
    - v. Zero Frequency = 640MHz
    - vi. Pole 1 Frequency = 2.7GHz
    - vii. Pole 2 Frequency = 4.5GHz
    - viii. Pole 3 Frequency = 13.5GHz
      - ix. Turn Display On

Equalizer Setup			
Equalization Wizard		Close	
Equalization Wizard Linear Eq (FFE / CTLE) Display Scaling Source Channel 1 - 3 • Data Rate 5.400000000 Gb/s • Linear Equalizer Type FFE © CTLE DC Gain 1.000 • Zero Frequency 640 MHz •	Decision Feedback Eq (DFE) Enable Source CTLE # of Taps 1 Auto Set DFE renders as a Real Time Eye. Set up and enable Real Time Eye to enable DFE. # of Poles 2 © 3	Close Help Tap Setup Clock Recovery	
Pole 1 Frequency 2.700 GHz Pole 2 Frequency 4.500 GHz Pole 3 Frequency 13.500 GHz	$H(s) = \frac{A_{dc} \cdot \omega_{p1} \cdot \omega_{p2} \cdot \omega_{p3}}{\omega_{z}} \cdot \frac{s + \omega_{j}}{(s + \omega_{p1}) \cdot (s + \omega_{p3})}$	$\frac{k}{2}\cdot(s+\omega_{p3})$	

Figure 29: HBR2 Equalizer Menu Settings

- b. For HBR:
  - i. Data Rate = 2.7Gb/s
  - ii. Equalizer=CTLE
  - iii. # of Poles = 2
  - iv. DC Gain = 1.0
  - v. Zero Frequency = 725MHz
  - vi. Pole 1 Frequency = 1.35GHz
  - vii. Pole 2 Frequency = 2.5GHz
- c. Press Close on Equalizer Setup Menu.
- d. Turn Off C1-C3 Waveform so only Equalized Waveform is displayed.
- 3. The results in the TP3\_EQ waveform for HBR2 and HBR and non-equalized waveform for RBR.



Figure 30: HBR2 Differential TP3-EQ Signal

#### **Measuring ISI**

- 1. To Get ISI Measurement, Go to Analysis EZJIT menu.
  - a. Select the Jitter Wizard.
  - b. The first screen should look like the following, verify the defaults are as shown below

Figure 31: Jitter Wizard Settings...

Jitter Wizard: Sour	ce and Type	X
Setup       Checklist         ✓       General         Setup       Source         Type       Measurement         Setup       Clock         Recovery       Thresholds         Acquisition       Calibration	Set the source and typ measurement. TIE acc according to a recover and Unit Interval meas be used on clock or '10 waveforms. Source CTLE Measurement © TIE (Phase) ○ Period ○ N-Unit Interval	e of umulates jitter ed clock. Period urements can )' data C 丘 C 丘 C 丘 C 夭
Help		
	Back Next >	Cancel

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- c. Press Next.
- d. Click through Source Type using the defaults.
- e. In Measurement Setup, change BER Level to 1E-9 per the PHY CTS 1.2b.

Setup ✓	Checklist General Setup	Set the pattern length. Arbitrary data is live traffic where the pattern length is unknown. Periodic data is PRBS or other repeating patterns.	
~	Source Type	outer repeating patterns.	
+	Measurement Setup	Pattern Length	
	Clock Recovery	<ul><li>⊙ Periodic</li><li>○ Arbitrary</li></ul>	
	Thresholds	🗹 Auto	
	Acquisition	63 (2 <sup>6</sup> -1)	
	Calibration		
	Help	1E-9	
		Back Next > Cancel	

f. In Clock Recovery, set the Clock recovery as follows to meet the PHY CTS 1.2b requirements.

Jitter	Wizard: Cloc	k Recovery 🛛 🔀
Setup ✓ ✓	Checklist General Setup Source Type Measurement Setup Clock Recovery Thresholds	Setup clock recovery. Clock recovery applies to high speed serial data analysis, RJ DJ and TIE Jitter measurements. Clock Recovery Method Second Order PLL Nominal Data Rate 5.40000000 Gb/s Loop Bandwidth 6.260000 MHz Damping Factor
	Acquisition Calibration Help	1.000

- i. For HBR2:
  - Clock Recovery Method = Second Order PLL
  - Nominal Bit Rate = 5.4Gb/s
  - Loop Bandwidth = 6.26MHz
  - Damping Factor = 1.0

- ii. For HBR:
  - Clock Recovery Method = Second Order PLL
  - Nominal Bit Rate = 2.7Gb/s
  - Loop Bandwidth = 10MHz
  - Damping Factor = 1.51
- iii. For RBR use external trigger for ISI and eye height measurements, see C appendix.

For RBR RJ measurements use:

- Clock Recovery Method = Second Order PLL
- Nominal Bit Rate = 1.62Gb/s
- Loop Bandwidth = 10MHz
- Damping Factor = 1.51
- g. In Acquisition, select Manual and increase the Record Length to 8.4Mpts or higher. This will ensure one Million Unit Intervals as specified in the PHY CTS 1.2b. It also represents repeatable jitter measurements on the CP2520 pattern used for HBR2.

1	Jitter V	Vizard: Acq	uisition 🔀
	Setup (	C <mark>hecklist</mark> General Setup	Based upon the specified loop bandwidth, it will take 769 ns for the clock to lock to the data. It is
	~	Source Type	rate to maximum and set the memory depth to Calculate.
	~	Measurement Setup	☑ Set maximum sample rate
	~	Clock Recovery	Norma Daril
	~	Thresholds	Calculate Track Timebase (Automatic)
	<b>→</b>	Acquisition Calibration	Manual     8.38861 Mpts     ■
		Help	
		<	Back Next > Cancel

- h. Click Calibration, using the defaults.
- i. Press Finish from the Calibration screen.
- j. Before leaving the Jitter menu, select mUI as the Units.

Jitter Setup Wizar	'd	Close	
Source	e •	Help	
Measurement ⊙ TIE (Phase) ○ Period ○ N-Unit Interval	Edges ে र्न ल २	Advanced	
Pattern Length	Units ○ Second ● Unit Interval Graphs ○ 1 ● 4 ○ 2		
2520 bits	Bathtub Scale ⊙ BER Scale ○ Q Scale		
RJ Bandwidth	Crenh Ceele	Clock	
⊙ wide (White) ⊙ Narrow (Pink)		TIE Filter	
BER Level	Clifiedi		

- k. Press Close to leave the Jitter menu.
- 1. The DSA will take a few moments to calculate and display the Jitter measurement results.



Figure 32: HBR2 Differential TP3-EQ Signal with ISI Measurement

m. Verify ISI is within 5% of the specification limit. If it is not 5%, adjustments on the ISI channel are needed to be within a +/- 5% target. Adjust channel and try again. To acquire a

new waveform Press Clear Screen to clear the previous acquisition date, then the Single button to acquire a new waveform.

Note: If a N4916B is De-emphasis Signal Converter is part of the setup ISI can be reduced by applying a post cursor, see E appendix.

#### Eye Diagram Display

- 1. To create Eye diagram, select Analysis > Serial Data
  - a. Select Serial Data Wizard.
  - b. Use same clock recovery set in Jitter Wizard.

etup Checklist General Setup Source Type Measurement	Setup clock recovery. Clock recovery applies to high speed serial data analysis, RJ DJ and TIE jitter measurements. Clock Recovery Method Second Order PLL	
Setup Clock Recovery Thresholds Acquisition	5.40000000 Gb/s	
Calibration Help		

- c. Click Next.
- d. Click through Thresholds and Time Interval Measurements screens with the default settings.
- e. In Real Time Eye, select Turn on real time eye display and Use a color graded display.

Setup	p Checklist Clock Recovery	The real time eye display creates an eye diagram by overlaying each unit interval of the data waveform according to the recovered clock. The update of the display will be relatively	
•	Inresnoids	slow as each interval is plotted.	
~	Time Interval Measurement		
<b>→</b>	Real Time Eye	$\underline{\lambda}$	
	Display Clock	✓ Turn on real time eye display	
	Acquisition	✓ Use a color graded display	
	Help	Select which bits to include	
		○ Transition	

- f. Click Next.
- g. Click through Display Clock screen using default of Off
- h. In Acquisition, Deselect Fast Update and increase Memory to 8.4Mpts or higher.

Serial I	Data Wizard:	: Acquisition 🛛 🔀
Setup ✓ ✓ ✓ ✓	Checklist Clock Recovery Thresholds Time Interval Measurement Real Time Eye Display Clock Acquisition Help	Based upon the specified loop bandwidth, it will take 769 ns for the clock to lock to the data. It is recommended that you fix the sample rate to 40.0 GSa/s and set the memory depth to 46.2 kpoints. Memory 8.38861 Mpts Sample Rate 40.0 GSa/s The main timebase scale (range / 10) determines the interval for folding the data for the real time eye display. The timebase range should be set to 2 unit intervals to give a nice display. Time zero is the position of the recovered clock. 37 ps/
	<	Back Next > Cancel

- i. Click Next and Finish
- j. The DSA will take a few moments to create the real time eye diagram.



Figure 34: HBR2 Differential TP3-EQ Eye Diagram

#### **RJ and SJ Calibration Scope Setup**

- 1. Select Analysis > Serial Data
- 2. Select Clock Recovery
- 3. Change Clock Recovery to Constant Frequency. This removes the CDR's Jitter Transfer Function filter from the Jitter measurement.
- 4. Change the J-BERT N4903B Pattern from CP2520 (HBR2) or PRBS7 (HBR and RBR) to D24.3 pattern (quarter rate clock). This removes DDJ from the measurement.
- 5. Enable RJ on the Scope J-BERT N4903B and set to a value equivalent to the target value in the specification.
- 6. Press the Clear Display button on the scope front panel.
- 7. Press the Single button on the scope front panel.
- 8. The DSA will take a few moments to update the eye diagram and measurements.
- 9. Adjust Random Jitter on J-BERT N4903B until it matches the target value.



Figure 35: HBR2 Random Jitter Calibration

- 10. On the J-BERTN4903B, disable RJ.
- 11. To calibrate the SJ terms, on the J-BERT N4903B, enable the desired PJ term to calibrate (PJ 1 or PJ 2). Each SJ term needs to be calibrated independently.
- 12. Set the PJ to the specification target value.
- 13. Press the Clear Display button on the scope front panel.
- 14. Press the Single button on the scope front panel.
- 15. The DSA will take a few moments to update the eye diagram and measurements.
- 16. Adjust Periodic Jitter on J-BERT N4903B until PJ(d-d) matches the target value in the PHY CTS 1.2b.



Figure 36: HBR2 Sinusoidal Jitter Calibration

#### Eye Height Calibration (with and without crosstalk)

- 1. On the J-BERT N4903B, turn on all Jitter terms on J-BERT N4903B Jitter menu. RJ, PJ 1 (HBR2 only), PJ 2, and SSC.
- 2. On the J-BERT N4903B, change the pattern back to CP2520 (HBR2) or PRBS7 (HBR and RBR) from D24.3.
- 3. If testing HBR or RBR, go to Trigger Amplitude menu on the J-BERT N4903B and set the Trigger Amplitude to the specified amplitude in the PHY CTS 1.2b.
- 4. If testing HBR2, set the Trigger Amplitude to Zero. This amplitude will be increased after establishing the non-crosstalk eye amplitude.
- 5. On the DSA, select Analysis > Serial Data > Clock Recovery, and return the Clock recovery to 2nd Order PLL.
- 6. On the DSA, select measurements Eye > Eye Height Measurement and set the measurement to measure at the 50% UI point.
- 7. Press the Clear Display button on the scope front panel.
- 8. Press the Single button on the scope front panel.
- 9. If testing RBR or HBR, calibrate the Eye Height to the PHY CTS 1.2b target value. See C appendix for RBR measurements.
- 10. If testing HBR2, calibrate the Eye Height to the non-crosstalk target value.



Figure 37: HBR2 without Crosstalk Eye Height Calibration

11. If calibrating HBR2; on the J-BERT N4903B, increase the value in the Trigger Amplitude from zero to a value that yields the target eye height with crosstalk.



Figure 38: HBR2 with Crosstalk Eye Height Calibration

# C. Appendix: RBR ISI and Eye Height Measurements

According to PHY CTS 1.2b the RBR stress test signal is measured at TP3 before an equalizer. The required ISI component is 570mUI. The measurement methods used for HBR2 and HBR cannot be applied in this case since the ISI creates problems for the clock recovery algorithms of the scope. The following sections describe alternative measurement methods. The measurements do not use clock data recovery but a clock or trigger signal provided by J-BERT instead. Therefore SSC should be deactivated for the measurements.

#### **RBR ISI Measurement**

ISI will be measured indirectly by using eye opening or  $jitter_{pp}$  measurements with ISI and without ISI. The delta of the two measurements is jitter caused by ISI. To measure the eye opening without ISI a clk/2 pattern, 1010, is used. The eye opening measurement with ISI is done using a PRBS 2<sup>7</sup>-1. All jitter sources are turned off on J-BERT. Amplitude for the data signal above 500mV<sub>diff</sub> is recommended for this measurement. The measurement should be performed on the differential data signal at TP3.

#### **BERT based ISI Measurement for RBR**

The J-BERT's Output Timing Measurement can be used to determine the eye opening or phase margin for a desired BER level. Since a PRBS 2<sup>7</sup>-1 is a very short pattern a BER level of 10<sup>-6</sup> is more than sufficient.



Figure 39: J-BERT Output Timing based ISI measured for RBR

The ISI is determined as the delta of the two phase margin measurement, 915mUI - 336mUI = 579mUI. This measurement requires a BERT error detector and cannot be done on J-BERT options G07 and G13.

#### Scope based ISI measurement for RBR

A horizontal histogram which slices through the center of the crossing point is used to measure jitter<sub>pp</sub>. The scope is triggered by a signal from J-BERT's clock or trigger output. Scope settings:

- Set up scope for a measurement on a differential signal either by using a differential SMA probe head or HW based channel subtraction (channel 1-3 or channel 2-4)
- Use 1kpts acquisition depths
- Set display mode to color grade
- Adjust crossing point to center of the display with two eyes
- Activate an horizontal histogram Analyze → Histogram and select a thin window from the center of the left eye to the center of the right eye
- Activate an histogram peak to peak measurement

J-BERT settings:

- Select a clk/2 pattern (1010) on J-BERT for the no ISI measurement and select a PRBS 2<sup>7</sup>-1 pattern for the pp measurement with ISI
- Select  $1V_{diff}$  amplitude for the data output
- Deactivate SSC and all jitter sources
- Set data rate to 1.62Gb/s

For the measurement clear the display and let the scope run for a fixed amount of time, e.g. 2 minutes. Note the hist<sub>pp</sub> reading and repeat for at least five times. Average the results for the pp no ISI measurements. Repeat for the hist<sub>pp</sub> with ISI measurements.



Figure 40: RBR ISI measurement step 1 for jitter base line



Figure 41: RBR ISI measurement step 2 for jitter with ISI

In this example the hist<sub>pp no ISI</sub> measurement was 58.9ps and the hist<sub>pp with ISI</sub> measurement was 406.7ps. The delta is 347.8ps or 563.4mUI. The target limits are 570mUI+-5%.

#### Eye Height Measurement for RBR

A vertical histogram which slices through the one level and one for the zero level are used to measure eye height boundaries for the zero level and one level. The delta is the eye height. The scope is triggered by a signal from J-BERT's clock or trigger output.

Scope settings:

- Set scope up for a measurement on a differential signal either by using a differential SMA probe head or HW based channel subtraction (channel 1-3 or channel 2-4)
- Use 1kpts acquisition depths
- Set display mode to color grade
- Adjust eye in the center of the display
- Activate a vertical histogram Analyze → Histogram and slice thinly through the one level starting in the center of the eye for the one level boundary and change the window in the voltage axis to slice through the zero level starting from the center of the eye for the zero level boundary
- Activate an histogram peak to peak measurement

The measurements for one level and zero level boundaries need to be done with the same left and right limits for the histogram window to get the eye height for a specific timing setting.



Figure 42: RBR eye height boundary measurement for one level

The one level eye height boundary is the min level of the histogram. The zero level is max level of the histogram.



Figure 43: RBR eye height boundary measurement for zero level

In this example the one level eye height boundary is  $18.9 \text{mV}_{\text{diff}}$  and the zero level eye height boundary is  $24.6 \text{mV}_{\text{diff}}$ . The eye height is the delta  $\rightarrow 18.9 \text{mV}_{\text{diff}} - (-24.6 \text{mV}_{\text{diff}}) = 43.5 \text{mV}_{\text{diff}}$ . The target for RBR is  $46 \text{mV}_{\text{diff}} + 10\%$ .

# D. Appendix: Test Automation

Test and calibration automation is provided by the N5990A Test Automation Platform. The sink test automation is offered by the N5990A-155 receiver test library and the N5990A-255 offers an interface to the DisplayPort Source Test application of the 90000 Series Real-Time Scopes.

The N5990A-155 sink test automation library remote controls the Agilent J-BERT N4903B as well as Agilent's 90000 Real-Time Scopes for calibration and the Agilent / Quantum Data or Unigraf Aux Channel Controller for sink test automation.

All calibration and test steps are automated with the exception of necessary cabling changes.

#### **Test Station Configuration**

In a first step the test instruments required for the sink tests have to be selected and the VISA remote addresses have to be assigned. This is done in the DisplayPort Station Configurator program. The user is guided through the individual steps of the station configuration.

Note, the predefined addresses may not be correct!

Figure 44: Test station selection

DisplayPort 1.0 and 1.1 testing can be done with J-BERT A/B and ParBERT while for DisplayPort 1.2 testing a J-BERT is recommended.

9 ValiFrame Configuration V	Wizard	
Step 2: Station Config	uration	Note, the predefined addresses may not be correct!
	Pattern Generator:	AUX Channel Controller: Agilent W2642A
A J-BERT (N4903B or N4903A) is used as the pattern generator		
	Cancel	<pre></pre>
	ValiFrame Configuration Step 2: Station Config A.J-BERT (N4903B or N4903A) is used as the pattern generator	ValiFrame Configuration Wizard  Step 2: Station Configuration  A.J-BERT (N49038 or N4903A) is used as the pattern generator!  Cancel  Cancel

Figure 45: Instrument assignment

The station configurator accepts any VISA remote addresses or a VISA alias for the instruments. For calibration the J-BERT and scope need to be online while the aux channel controller can be offline. For the sink test itself the BERT and the aux channel controller need to be online and the scope can be offline.

р <b>о</b> . ша		onnguración	Note, the predenned addresses	s may not be contecti
struments				
Mode	Status	Instrument	Address	Description
🗸 Online 🗌	Not Tested	AgDSO	TCPIP0::141.121.85.69::inst0::INSTR	Real-Time Oscilloscop
Offline	Not Tested	DisplayPort Test U7232B	192.168.0.2	DisplayPort Tx Applica
🗹 Online	Not Tested	JBERT	BERTLAN	J-BERT for Pattern an
Offline	Not Tested	DisplayPort Test Controller	192.168.1.11	Agilent W2642A to ac
rument Ado	dress: TCPIP0::1	41.121.85.69::inst0::INSTR	Apply Address	Check Connections
ıliFrame	Configuratio	n Wizard	<pre></pre>	Finish
aliFrame ep 3: Ins	Configuration strument C	n Wizard	< Back	Finish
aliFrame ep 3: Ins	Configuration strument C	n Wizard onfiguration	< Back	Finish
a <mark>liFrame</mark> ep 3: Ins struments Mode	Configuration strument C Status	n Wizard onfiguration	< Back Note, the predefined addresses Address	Finish
aliFrame ep 3: Ins struments Mode 2 Online	Configuration strument C Status Successful	n Wizard onfiguration	< Back Note, the predefined addresses Address TCPIP0::141.121.85.69::inst0::INSTR	Finish Trinsh Tr
aliFrame ( ep 3: Ins istruments Mode Online	Configuration strument C Status Successful Offline	Cancel n Wizard onfiguration Instrument AgDS0 DisplayPort Test U7232B	< Back Note, the predefined addresses Address TCPIP0:141.121.85.69::inst0::INSTR 192.168.0.2	Finish may not be correct! Description Real-Time Oscilloscop DisplayPort Tx Applica
aliFrame ep 3: Ins struments Mode Online Offline Offline	Configuration strument C Status Successful Offline Successful Offline	Cancel n Wizard onfiguration Instrument AgDS0 DisplayPort Test U7232B JBERT DisplayPort Test Controller	< Back Note, the predefined addresses Address TCPIP0::141.121.85.69::inst0::INSTR 192.168.0.2 BERTLAN 192.168.1.11	Finish  rmay not be correct!  Description Real-Time Oscilloscop DisplayPort Tx Applica J-BERT for Pattern an Anient W2F2A In ac
aliFrame ep 3: Ins struments Mode Online Offline Offline	Configuration strument C Status Successful Offine Successful Offine	Cancel n Wizard onfiguration Instrument AgDS0 DisplayPort Test U7232B JBERT DisplayPort Test Controller	< Back Note, the predefined addresses Address TCPIP0::141.121.85.69::inst0::INSTR 192.168.0.2 BERTLAN 192.168.1.11	Finish  may not be correct!  Description Real-Time Oscilloscop DisplayPort Tx Applica J-BERT for Pattern an Agilent W/2642A to ac
aliFrame ep 3: Ins struments Mode 2 Online 0 Offline 0 Offline	Configuration strument C Status Successful Offline Successful Offline	Cancel Cancel Configuration Instrument AgDS0 DisplayPort Test U7232B JBERT DisplayPort Test Controller	< Back Note, the predefined addresses Address TCPIP0::141.121.85.69::inst0::INSTR 192.168.0.2 BERTLAN 192.168.1.11	Finish  s may not be correct!  Description Real-Time Oscilloscop DisplayPort Tx Applice J=BERT for Pattern an Agilent W2642A to ac
atif rame ep 3: Ins struments Mode Online Offline Offline	Configuration strument C Status Successful Offline Successful Offline	Lancel n Wizard onfiguration Instrument AgDS0 DisplayPort Test U72328 JBERT DisplayPort Test Controller 41.121.85.69::inst0::INSTR	< Back Note, the predefined addresses Address TCPIP0::141.121.85.69::inst0::INSTR 192.168.0.2 BERTLAN 192.168.1.11 Apply Address	Finish  rmay not be correct!  Description Real-Time Oscilloscop DisplayPort Tx Applica J-BERT for Pattern an Agilent W2642A to ac  Check Connections

#### Figure 46: Instrument remote address assignment



#### **DUT Configuration Setup**

The calibration steps and sink test depend on several DUT capabilities. Aux channel support, number of lanes as well as supported data rates are specified in the DUT configuration.

N5990A Test Automation Software Platform		
File Station Sequencer Help		
Configure DUT und Save Start Abort Pause Print Troperties Log List	All Results 💌	
DisplayPort - not configured		
eventy message	1/7/2013 1:29:59 PM	
ogress Opening online connection to DSO Infinitum Series at scopeLAN	1/7/2013 1:29:59 PM	
ogress Opening offline connection to U7232B at 192.168.0.2	1/7/2013 1:29:59 PM	
rogress Upening online connection to W43034 at 552H LAN pages Depening offline connection to W2642A at 192 168 1 11	1/7/2013 1:29:59 PM 1/7/2013 1:29:59 PM	
fo N5990A Test Automation Software Platform startup complete!	1/7/2013 1:30:00 PM	
	Cavial Bus Family DisalayPart Station	

Figure 47: The SW needs to be configured for DUT under test

Additionally setup specifics like aggressor channel distribution are specified in the configure product screen.

6 Configure Product
Product
Product Number: DisplayPort 🗸 Serial Number:
Product Type: Sink 💌 Port Name: 1 💌
Description:
Number of Lane(s): 4 Spec Version: DP1.2b
CTest User Name: DisplayPort Tester
Comment:
Initial Start Date: 1/7/2013 9:30:52 PM      O Compliance Mode
Last Test Date: 1/7/2013 9:30:52 PM O Expert Mode
Sink PHY Test  Read Error Counter only once  Sink Capabilities
Use dummy AUX Channel Controller
Error Counter doesn't support reset on read
Use Differential Probe for Calibration
Skip Link Training
Use 4-Way Dividers for Aggressor Lanes Use Attenuators
Keep Signals after test
UK

Figure 48: Supported lanes and data rates as well as operating modes

The test automation software offers two operating modes: The default compliance mode and an expert mode. The expert mode allows changes to calibration and test settings as well as allows additional tests for device characterization.

DisplayPort Test Implementation Group

# **Automated Sink Calibration**

Calibration steps are grouped by data rates. RBR and HBR calibration consist of

- ISI verification
- RJ calibration
- Eye height calibration

HBR2 calibration of

- ISI verification
- RJ calibration
- Fixed SJ at 200MHz calibration
- Eye height calibration without crosstalk
- Eye height calibration with cross talk applied

All calibration steps are CTS compliant.

1110 500	tion Sequencer	Help								
الچ Configure DI	🗁 🛃 UT Load Save	Start A	bort Pause		I Properties	Log List				All Results
	DisplayPort         1.2b           Calibration         BRB           BRB         SISCalib           BRD         SISCalib           SISCAL         SISCalib           SISCAL         SISCalib           SISCAL         SISCAL           SISCAL         SISSIN           SISCAL	ration RBR; ; a Jitter Calibra ming Calibrat ming Calibrat ration HBR Jitter Calibrat ming Calibrat or Lanes Cali or Lanes Cali or Lanes Cali or Lanes Cali rate	12/11/2012 9: 12/ion RBR 32C ion RBR SSC ion RBR SSC ion RBR SSC ion HBR SSC ion HBR SSC ion HBR SSC ion HBR SSC ion HBR SSC ion HBR2 SSC ion HBR3 SSC ion HBR	43:52 AM 117/2012 2 10MHz SJ 20MHz SJ 20MHz SJ 20MHz SJ 20MHz SJ 100MHz S 20MHz SJ 20MHz SJ 20MHz SS 20MHz SS 2	L55:34 PM 12/11/2012 ; 12/11/201 ; 12/11/201 j 2/11/201 J J J J J J J J J J J J J J J J J J J	1:55:32 PM 2 1:55:32 PI 2 1:55:32 PI	4	LisplayPat     BisplayPat     Repetitions     Use Dummy ALX Channel     Calibration     Use Differential Probe     Debugging Options     Step Mode     Parade DPS21 Device     Send PHY Test Request to     Repetitions	Cor False False False ad True	
Progress Progress Progress	Instrument Connect Opening online co Opening offline co	tions nnection to D nnection to U	SO Infiniium S 7232B at 192.	eries at sc 168.0.2	opeLAN				1/7 1/7 1/7	/2013 1:29:59 PM /2013 1:29:59 PM /2013 1:29:59 PM
Progress Progress	Opening online co Opening offline co	nnection to N nnection to W	4903A at BEF /2642A at 192	TLAN 168.1.11					1/7	/2013 1:29:59 PM /2013 1:29:59 PM /2013 1:29:59 PM

Figure 49: Calibration step selection

Several calibration steps can be selected by check marks and the test automation will execute the selected calibration steps sequentially. The user gets prompted only in the beginning and when a setup change is necessary.



#### **Figure 50: Connection instruction prompt**

Successful calibration steps are indicated by green smiley faces, unsuccessful ones by red faces and the step in progress by a runner.



Figure 51: Progress update in log section and MS Excel

# **Automated Sink Testing**

Sink tests are grouped by lane and sub grouped by data rate and jitter frequency. Several tests can be check marked and the software executes the selected tests sequentially prompting the user when a setup change is necessary or user input is required.



#### Figure 52: Test setup connection prompt

🙀 🖉 - 🔍 - Л 2MHz HBR2 L0:1 - Microsoft Ex 💶 🗆	9 N5990A Test Automation Software Platform	
🖼 Home Insert Page Layout Formulas Data Review View 🎯 – 🕫	File Station Sequencer Help	
$\lambda$ Arial $v$ $0$ $a$ $a$ $a$ $B$ $I$ $I$ $A$ $A$ $a$ $a$ $Paste$ $A$ $a$ $A$ $A$ $a$ $a$	Configure DUT Load Save Start Abot Pause Print Properties	Log List All Results 🗸
Clipboard © Font © Editing	e - Will Sink Lane 0	Bit Error Rate Testing     Sequence File CP2520Tps3
A1 • Product Number: DisplayPort	High Bitrate	Link Quality Pattern Hint 5
A B C D E F G H	High Bitrate 2	Observation Time Factor 1
2	🚽 🔁 Jitter Tolerance Test 2 MHz SJ HBR2 Lane 0	Lalibration
3 Jitter Tolerance Test 2 MHz SJ HBR2 Lane 0	WOT Jitter Tolerance Test 10 MHz SJ HBR2 Lane 0	ISI I race Length HBH2 32
4 The Sink Jitter Tolerance Test, as defined in the DP Compliance Test Specification, secton 4.1. This test generates a stressed eye		E Jitter
5 8 Number of Jacos 4	VIT I Jitter Tolerance Test 100 MHz SJ HBR2 Lane 0	Fij Amplitude (FMS) 16.7 mUI
7 Spec. Version 1.2	Jitter Tolerance Test 2 MHz SJ Zero-Cable HBR2 Lane 0	E Segueror
8 ISI Amplitude 220 mUl	Jitter Tolerance Test 10 MHz SJ Zero-Cable HBR2 Lane 0	Procedure Error Case Rehavior Proceed With Next Procedure
3 SSC Programmy 33 MHz 10 SSC Amplitude 0.5 %	Jitter Tolerance Test 20 MHz SJ Zero-Cable HBR2 Lane 0	Procedure Erior Case Behavia Proceed with Next Procedure Procedure Eailed Case Behavia Proceed With Next Procedure
11 Sequence File CP2520Tps3	Jitter Tolerance Test 100 MHz SJ Zero-Cable HBR2 Lane (	Posetitions 0
12 ISITrace Length HBI 32	KUN Variable Parameter Test Lane 0	
13 Link Geality Pattern ' 5	🖨 🗌 RUM Sink Lane 2	SC Englisher 22 kHz
15 RJ Amplitude (RMS 16.7 mUI	Reduced Bitrate	SSC Amplitude 0.5 %
16 Fixed SJ Amplitude 100 mUI	INVE Litter Telerance Test 2MUs STRRP Lane 2	Use SSC True
17 Observation Time Fr 1 18 Has Dumma ALIX CL False	Please wait	E Veltage
19 Step Mode False		Euro Opening (with Aggregater 1, 90 m)/
20 Parade DP621 Devic False	Wait until the end of the observation time. Please	cye opening (with Agglessol 1 30 mv
21 Send PHY Test Reg True 22 Use Differential Pro False	prepare to read the error counter exactly after the time	
23	<ul> <li>period is elapsed:</li> <li>blate: This dialogue;</li> </ul>	
Jitter Freq. Sin-Jitter Amp. Number of Errors Max Spec	of the observation time!	
25 (most [min2] [min3] [] (min3)ec [] [] (min3)ec [] []	or the observation time:	
26	2	Benetition
28	e 2	Персикию
29	e 2	
30	ne 2	
32	Time left: 00:02:44	Date 🛆
33	reque	ncy 2MHz 1/7/2013 2:25:48 PM
34	glessi	1/7/2013 2:25:58 PM
36	Progress Try to lock Frequency	1/7/2013 2:25:59 PM
37	Progress Frequency locked	1/7/2013 2:26:01 PM
38	Progress Try to achieve symbol lock Progress Sumbol lock achieved	1/7/2013 2:26:01 PM 1/7/2013 2:26:02 PM
40	Info Error counter test passed: 2 errors where injected => CTS allows 2 to 4	errors, and the error counter shows a value of 2 1/7/2013 2:26:02 PM
41		×
42	<	
44	Performing procedure step 0 of iteration 0, total step count is 0	Serial Bus Family DisplayPort Station

Figure 53: Frequency lock, symbol lock and error counter are checked automatically

The test automation checks for frequency lock and symbol lock as well as controls the DUT's error counter if a supported aux channel controller is connected and the DUT supports aux channel control.

# E. Appendix: ISI Adjustment Using De-emphasis

A de-emphasized signal can be used to fine tune ISI if the channel without de-emphasis measures an ISI number above the target range.

#### Setup a De-emphasized Signal

Both the N4916B De-emphasis Signal Converter and the channel add method which combines data and aux data can be used for this approach. The channel add method requires N4903B Opt. 002.

#### N4916B De-emphasis Signal Converter

J-BERT N4903B	Stressed Signal Generator	
	N4916B	

Figure 54: Setup with N4916B De-Emphasis Signal Converter

The N4916B De-emphasis Signal Converter acts as front-end for the J-BERT N4903B. It is connected to the J-BERT N4903B using the N4915A-010 connection cable kit and is controlled by J-BERT via an USB connection. The unused data out bar connector needs to be terminated.

Before first use the timing between J-BERT N4903B and N4916B needs to be adjusted:

• Activate N4916B de-emphasis signal converter

Menu -11 -10 -9 Cont	BER: 0.500E0 -8 -7 -6 -5 -4 -3 ig	-2 -1 0 Elapsed 00:00:0	04 Erro	or Add Break	Remote
Refresh					
Identify	Connection	Enable Function	S/W Rev	VISA Resource N	lame
N4916B	DATA_OUT	DeEmphasis	Update!	USB0::2391::2306	4::MY51300
<					>
Seten Setu	Th cat here for	e Input Timing of the E ibrated for the combin s to be re-calibrated if detailed calibration in Input	De-Emphasis Sign ation of N4903B, N one of these chan istructions. Timing Setup 5	al Converter has to 14916B and cable i ges. Refer to the h Load Calibra	be kit. And alp system tion Setting
Pattern Gene 8.00000 Gb/s Sec	rator 📖 juence, B: Clock Loss	Jitter/ Outputs 7.999	or Detector 98 Gb/s PCle3_Mod Compliance	- Error Sync	Data Clock Loss Loss

Figure 55: Activate N4916B and prepare for Timing Adjustment

- Perform timing adjustment for N4916B
  - a. Press "Load Calibration Setting" once
  - b. Change data rate to 7Gb/s for a N4903B-C07 or 12.5Gb/s for a N4903B-C13
  - c. Connect main clock out normal to ED clock in
  - d. Select Input Timing Setup to 1. Do NOT press "Load Calibration Setting"
  - e. Perform Auto Align of ED
  - f. Start error count by pressing the start button once and wait until the accumulation is finished.

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Figure 56: Align Error Detector and Start/Stop Error Counter

g. Switch to Accumulated Results and note the recorded BER

uninalated 1	cobuitb (	und m		1000100		LIC.			· · · · ·
-11 -10 -9 -8 -3 Accumu	R: 0.000 7 -6 -5 -4 -3 -2 llated Res	-1 0 Elapse	8 00:02:05	Erro	Add	Break	Rem	-	
			Deller				<u> </u>	_	
۰ <b>.</b>			Katios						
· ·								-	
-2 -									
-4 -								-	
-6 -								1	
8 <u>-</u>								<u>.</u>	
								-	
-10 -								-	
-120		0.02		0.04					
0.00									
0 Days									
Accumulated Depute	0.001.1			L.		. In		. 1	
Accumulateu Results	G.821 Measur	rements   In	erval Results	Accumulatio	n Parame	eter   Burs	st Result	s	
Measurement		Curre	ent Period	Previous Pe	riod				
Bit Count	<b>FD</b> )	1.00	134538E12	61,806,989	,824				
Error Count	ER)	0.00	00000	0.0000000	J				
Errored 1's Patic		0.00	00000	0,0000000	1			=	
Errored 1's Court	, it	0.00	00000	0					
Errored O's Ratio		0.00	00000	0.0000000	)				
Errored O's Cour	it	0		0				~	
: Pattern Generator	- III I		Error De	tector	111	111	ET.		
Sequence	.B: Clock Ji	tter/ Output	2 00000 CM	- 207 1 DDDC	E	Sync	Data	Clock	

Figure 57: Accumulated Results for N4916B / N4903B Timing Adjustment

- h. Repeat steps c to g for all 6 input timing settings.
- i. One or two input timing settings will show a BER>0. Choose the input timing setting which is the furthest away from the failing input timing settings, e.g. 2 failed choose 5.

Note: If a J-BERT generator only option (-G07 or -G13) is used. Set data rate to HBR2 data rate and change to the HBR2 pattern sequence including the compliance pattern. Use an HBR2 capable receiver with its built-in error counter for the accumulated ber measurement for timing settings 1 to 6.

#### Channel Add of Data Out and Aux Data Out



Figure 58: De-emphasized Signals by Channel Add of Data Out and Aux Data Out

Combine Aux Data Out and Data Out as shown above and activate de-emphasis mode for aux data output.

	BER:	<b>0.000</b>	4 -3 -2 -1 0 Elapsed 00:00:00 Error Add Insert B
$\bigcirc$	PG - Bit I	Rate	Setup
	File	>>	<u> </u>
27.7	External Instrument(s)	>>	
010	Pattern	>>	PG Setup
<u>s</u>	PG Setup	>>	Add Preset
	ED Setup	>>	Data Output E Delete Preset
	Analysis	>>	Clock/Trigger Output
XX	Jitter	>>>	Trigger/Ref Clock Setup Ref Clk)
	Results	>>	Aux Data Setup Iz Ref Clk)
	Utility	>>	Error Add Setup
	Help	~	Alt Pattern and Aux In Setup Setup Station Sta
PG Aux Data Output			
Clock Divided by 2 2.700 GHz			
© Second Channel			
C Multiplexer Mode			
De-Emphasis Bit Offset			
	<u>о</u> к		<u>C</u> ancel <u>A</u> pply <u>H</u> elp

Figure 59: Activate De-Emphasis Mode for Aux Data Output

#### **ISI Adjustment Procedure**

- a. Set up J-BERT N4903B and scope according to section 9.1
- b. Set de-emphasis to 0dB
- c. Select the first J20 trace which leads to an ISI number higher than the target value
- d. Measure ISI according to B appendix
- e. Increase post cursor until ISI measurement is within target range. The post cursor should not exceed -6dB.



Figure 60: ISI Adjustment by Applying De-Emphasis

Note: In above example -0.8dB would result in ISI in the middle of the target range

# F. Appendix: Use of other Receptacle Fixtures

The use of other receptacle fixtures than the Wilder DP receptacles will influence the measured ISI, the  $SJ_{sweep}$  to be applied as well as the measured eye heights without and with crosstalk because of their different trace and crosstalk characteristics. If other receptacle fixtures are used correction methods for ISI and eye height without and with crosstalk have to be applied. Specific correction methods per lane might be required. It is outside the scope of this document to describe methods to determine such correction methods.