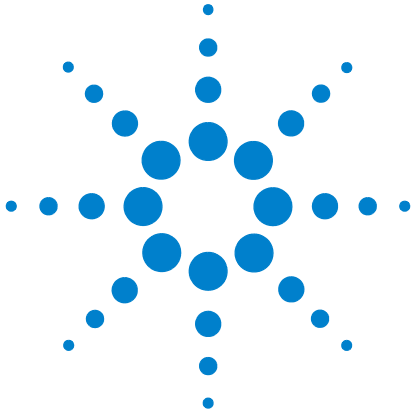

Agilent TS-8900
Functional Test System

Diagnostics User Guide

Agilent Technologies

Notices

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Double-click the link to **Test & Measurement**. Select your country from the drop-down menus. The Web page that appears next has contact information specific for your country.

If you do not have access to the Internet, call one of the numbers in Table 1.

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United States and Canada:	Test and Measurement Call Center (800) 452 4844 (toll-free in US)
Europe:	(41 22) 780 8111
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United States and Canada:	Test and Measurement Call Center (800) 452 4844 (toll-free in US)

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1 Legal Information

Legal Information

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Double-click the link to **Test & Measurement**. Select your country from the drop-down menus. The Web page that appears next has contact information specific for your country

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Japan:	Measurement Assistance Center (81) 0426 56 7832
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Asia-Pacific:	(85 22) 599 7777

Manufacturing Address

Agilent Technologies Microwave Products (Malaysia) Sdn. Bhd.

Bayan Lepas Free Industrial Zone,

11900 Penang,

Malaysia.

2
Safety and Regulatory Information

Safety Information

Safety Summary

The following general safety precautions must be observed during all phases of operation of this instrument. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of the instrument. Agilent Technologies, Inc. assumes no liability for the customer's failure to comply with these requirements.

Safety Notice

CAUTION A **CAUTION** notice denotes a hazard. It calls attention to an operating procedure, practice, or the like, that, if not correctly performed or adhered to, could result in damage to the product or loss of important data. Do not proceed beyond a **CAUTION** notice until the indicated conditions are fully understood and met.

WARNING **A WARNING notice denotes a hazard. It calls attention to an operating procedure, practice, or the like that, if not correctly performed or adhered to, could result in personal injury or death. Do not proceed beyond a WARNING notice until the indicated conditions are fully understood and met.**

General

This product is provided with a protective earth terminal. The protective features of this product may be impaired if it is used in a manner not specified in the operation instructions.

WARNING **DO NOT OPERATE IN AN EXPLOSIVE ATMOSPHERE. Do not operate the product in the presence of flammable gases or flames.**

WARNING **DO NOT REMOVE RACK PANELS OR INSTRUMENT COVERS. Operating personnel must not remove any rack panels or instrument covers. Component replacement and internal adjustments must be made only by qualified service personnel. Products that appear damaged or defective should be made inoperative and secured against unintended operation until they can be repaired by a qualified service personnel.**

WARNING **The protection provided by the TS-8900 system may be impaired if the system is used in a manner not specified by Agilent.**

Environmental Conditions

The TS-8900 Functional Test System is designed for indoor use only. Table 2-1 shows general environmental requirements.

Table 2-1 Environment Requirements

Environment Conditions	Requirements
Maximum Altitude	2000 meters
Temperature (Operation)	5 ° C to 40 ° C
Maximum Relative Humidity	The test system is designed to operate in the range from 5% to 80% relative humidity (non-condensing).

CAUTION This product is designed for use in Installation Category II and Pollution Degree 2, per IEC 61010-1 and 664 respectively.

Before Applying Power

Verify that the product is set to match the available line voltage and all safety precautions are taken. Note the external markings of the instruments described in **"Safety Symbols and Regulatory Markings".**

Ground The System

To minimize shock hazard, the instrument chassis and cover must be connected to an electrical protective earth ground. The instrument must be connected to the ac power mains through a grounded power cable, with the ground wire firmly connected to an electrical ground (safety ground) at the power outlet. Any interruption of the protective (grounding) conductor or disconnection of the protective earth terminal will cause a potential shock hazard that could result in personal injury.

Fuses

Use only fuses with the required rated current, voltage, and specified type (normal blow, time delay). Do not use repaired fuses or short-circuited fuse holders. To do so could cause a shock or fire hazard.

WARNING **In order to avoid electrical hazards, all system internal fuses must be replaced by trained and qualified personnel.**

Operator Safety Information

WARNING **Module connectors and Test Signal cables connected to them cannot be operator accessible.**

Cables and connectors are considered inaccessible if a tool (e. g. screwdriver, wrench, socket, etc.) or a key (equipment in a locked cabinet) is required to gain access to a conductive surface connected to any cable conductor (High, Low or Guard).

WARNING **Assure the equipment under test has adequate insulation between the cable connections and any operator-accessible parts (doors, covers, panels shields, cases, cabinets, etc.)**

Verify there are multiple and sufficient protective means (rated for the voltages you are applying) to assure the operator will NOT come into contact with any energized conductor even if one of the protective means fails to work as intended. For example, the inner side of a case, cabinet, door cover or panel can be covered with an insulating material as well as routing the test

cables to the front panel connectors of the module through non-conductive, flexible conduit such as that used in electrical power distribution.

Safety Symbols and Regulatory Markings

Symbols and markings on the system, in manuals and on instruments alert you to potential risks, provide information about conditions, and comply with international regulations. Table 2-2 defines the symbols and markings you may find in a manual or on an instrument.

Table 2-2 Safety Symbols and Regulatory Markings

Safety symbols	
	Warning: risk of electric shock.
	Warning: hot surface
	Caution: refer to accompanying documents.
	Laser radiation symbol: marked on products that have a laser output.
	Alternating current.
	Both direct and alternating current.
	Three-phase alternating current.
	Earth (ground) terminal
	Protective earth (ground) terminal
	Frame or chassis terminal
	Terminal is at earth potential. Used for measurement and control circuits designed to be operated with one terminal at earth potential.
N	Terminal for neutral conductor on permanently installed equipment.

Safety symbols	
	Terminal for line conductor on permanently installed equipment.
	Standby (supply); units with this symbol are not completely disconnected from ac mains when this switch is off. To completely disconnect the unit from ac mains, either disconnect the power cord, or have a qualified electrician install an external switch.
Regulatory markings	
ICES/NMB-001	This text indicates that the ISM device complies with Canadian ICES-001. Cet appareil ISM est conforme à la norme NMB-001 du Canada.
	The CSA mark is a registered trademark of the Canadian Standards Association.
	The C-tick mark is a registered trademark of the Spectrum Management Agency of Australia. This signifies compliance with the Australian EMC Framework regulations under the terms of the Radio Communications Act of 1992.
	This instrument complies with the WEEE Directive (2002/96/EC) marking requirement. This affixed product label indicates that you must not discard this electrical/electronic product in domestic householdwaste.
	The CE mark is a registered trademark of the European Community. If it is accompanied by a year, it indicates the year the design was proven.

Electrostatic Discharge (ESD) Precautions

Static electricity is destructive to your production process and the TS-8900. Careless handling and poor site planning can cause system reliability problems and reduce your product yield. The system may not be as easily damaged as the modules you will be testing, but good anti-static planning will help ensure high reliability.
The ESD symbol below indicates areas where ESD caution must be exercised. This is to prevent damage to instruments and/or test disruption.

ESD Symbol	
	**Caution: Static Sensitive**. Electrostatic discharge in this area may cause equipment damage or test disruption.

While not an exhaustive list of anti-static precautions, Table 2-3 shows suggestions to consider as you plan your system area:

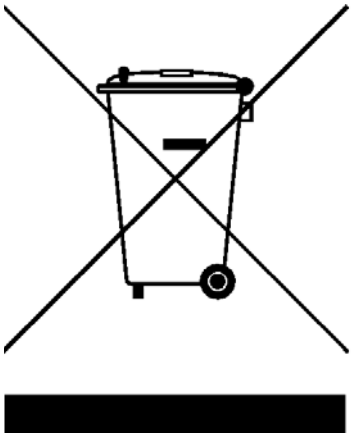
Table 2-3 Suggested Anti-Static Solutions for Site Planning

Precaution	Suggested Solution
Anti-static flooring	Plan to use an anti-static floor covering or mats.
Grounding straps	Plan for foot straps in conjunction with anti-static flooring and wrist straps for system operators.

CAUTION The system test rack is secured to the pallet of the shipping crate and wrapped with a plastic wrap. Do not move the crate or the test rack and pallet to a static sensitive area until you have removed the plastic wrap from the test rack.

End of Life: Waste Electrical and Electronic Equipment (WEEE) Directive 2002/96/EC

This product complies with the WEEE Directive (2002/96/EC) marking requirement. The affixed product label (see below) indicates that you must not discard this electrical/electronic product in domestic household waste.



Product Category:
With reference to the equipment types in the WEEE directive Annex 1, this product is classified as a “Monitoring and Control Instrumentation” product.

Do not dispose in domestic household waste

To return unwanted products, contact your local Agilent office, or see:

http://www. agilent. com/environment/product

for more information.

3
Running Diagnostics

This chapter describes the overview of diagnostic testplans, DGN testplan, CEDGN testplan and how to use the diagnostics test fixtures to verify the operation of system equipment.

NOTE Diagnostic testing is intended to verify basic connectivity and instrument functionality. It does not provide a full functional test of instrumentation and specifications.

Overview of Diagnostics Testplans

The verification strategy incorporates both standard and optional tests using different testplans. The standard testplan is shipped with each system. The testplans for the optional tests are included with the diagnostic test fixtures.

The standard tests verify both the core system instrument operation and internal test paths. It uses a testplan called "U8971A_DGN.tpa", simply called "DGN". "DGN" does not require external hardware, but verifies about 80% of the system functionality. These testplans are located in directory:

C:\Program Files\Agilent\TS-5000 System Software\testplan\DGN

NOTE For more detailed description of the "DGN" testplan, go to Diagnostic Testing Details.

The tests uses the "Customer Engineer Diagnostics" testplans (file name: "CEDGN *.tpa"), simply called "CEDGN". "CEDGN" completes the test coverage. It uses optional test hardware that is supplied with the kit. An understanding of test system operation and interpreting "CEDGN" test results are required to execute the tests. These testplans are located in directory:

C:\Program Files\Agilent\TS-5000 System Software\Service\U8970A\Testplans

The tests are executed in Agilent TestExec SL and TS-5000 system programming environment, and use both standard and specialized test actions. The programs can be edited to improve and/or reduce test coverage. Systems equipped with non-standard equipment do not have tests incorporated in either "DGN" or "CEDGN". You have to add tests for those systems.

Configuring and Running the DGN Testplan

1 Start Agilent Test Exec SL by clicking this icon on the desktop:

2 Load "U8971A_DGN.tpa" testplan into TestExec SL. "DGN" Testplans are located in this directory:

C:\Program Files\Agilent\TS-5000 System Software\testplan\DGN

3 Before running the testplan, identify the instrumentation you want to test in the first lines of the testplan as shown on Figure 3-1. Place a 1 next to instruments you want to test, a 0 next to those instruments you do not want to test (or that are not in your system).

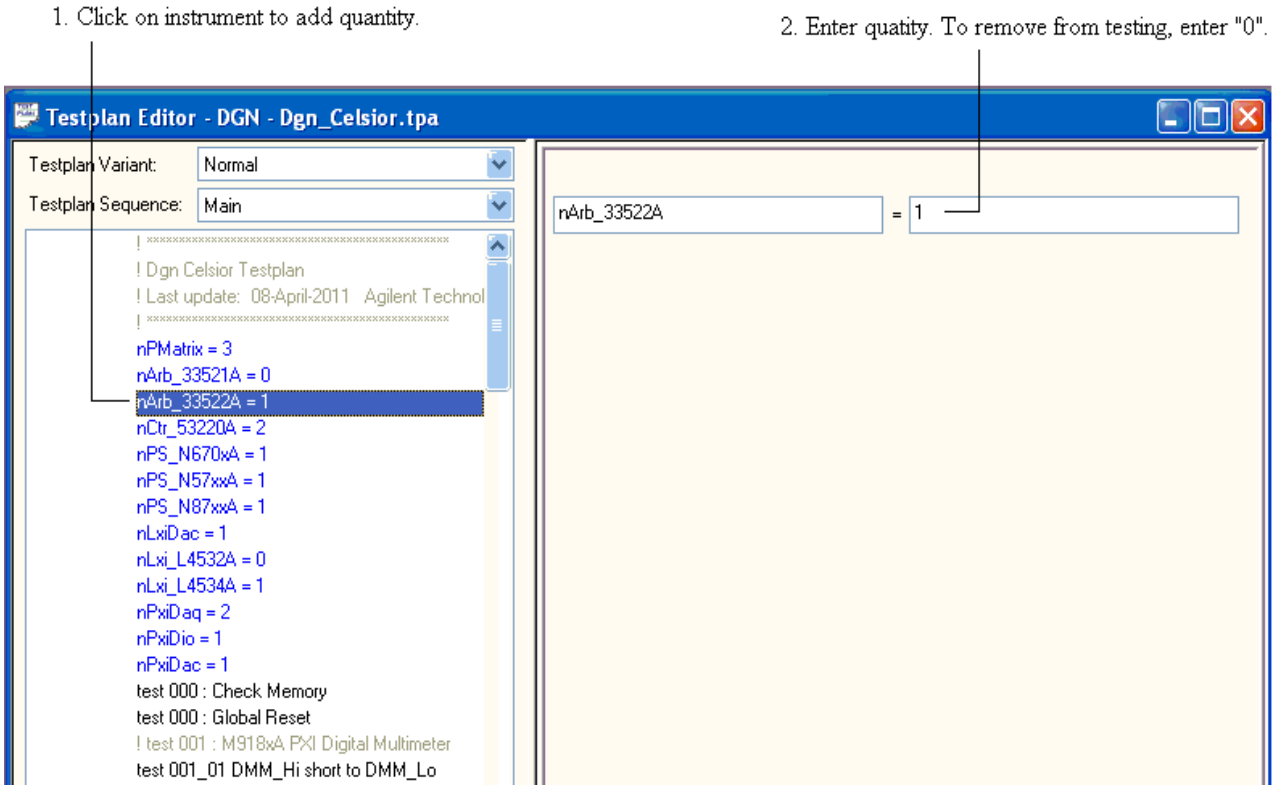


Figure 3-1 Specify the Instruments to be Tested in DGN Testplan

4 Click ▶ to run the testplan. The testplan will run tests on each system instrument configuration specified in step 3 and display the results of the testing.

Configuring and Running the CEDGN Testplan

1 Start Agilent Test Exec SL by clicking this icon on the desktop:

2 There are multiple testplans for TS-8900 Functional Test Systems. The each testplan is for specific instrument, module or card that is accessible at the Express Connect interface.

Table 3-1 CEDGN Testplan Description and Flow

Testplan Filename	Topology filename	Description
CEDGN_E878XA_PinMatrix.tpa	CEDGN_E878XA_PinMatrix.ust	SLU E8782A/E8783A Pin Matrix Card CEDGN Test
CEDGN_E6175A_LoadCard.tpa	CEDGN_E6175A_LoadCard.ust	SLU E6175A 8 Channel Load Card Test
CEDGN_U7177A_LoadCard.tpa	CEDGN_U7177A_LoadCard.ust	SLU U7177A 24 Channel Load Card CEDGN Test
CEDGN_E6178B_LoadCard.tpa	CEDGN_E6178B_LoadCard.ust	SLU E6178B 8 Channel Hi Power Load Card Test
CEDGN_N9377A_LoadCard.tpa	CEDGN_N9377A_LoadCard.ust	SLU N9377A 16 Channel Load Card CEDGN Test
CEDGN_N9379A_LoadCard.tpa	CEDGN_N9379A_LoadCard.ust	SLU N9379A 48 Channel Load Card CEDGN Test
CEDGN_E6198B_Utility.tpa	CEDGN_E6198B_Utility.ust	E6198B SLU Mainframe Utility CEDGN Test
CEDGN_L4451A_LXIDAC.tpa	CEDGN_L4451A_LXIDAC.ust	LXI L4451A 4 Channel DAC CEDGN Test
CEDGN_M9185A_DAC.tpa	CEDGN_M9185A_DAC.ust	PXI M9185A 8/16 Channel DAC CEDGN Test
CEDGN_M9186A_VI.tpa	CEDGN_M9186A_VI.ust	PXI M9186A Voltage Current Source CEDGN Test
CEDGN_M9187A_DIO.tpa	CEDGN_M9187A_DIO.ust	PXI M9187A Digital IO CEDGN Test
CEDGN_M9216A_DAQ.tpa	CEDGN_M9216A_DAQ.ust	PXI M9216A HV DAQ CEDGN Test
CEDGN_RS232.tpa	CEDGN_RS232.ust	RS-232 COM port CEDGN Test
CEDGN_SoftingCAN.tpa	CEDGN_SoftingCAN.ust	Softing CAN CEDGN Test

3 Load the appropriate testplan and its corresponding topology file based on your installed hardware into TestExec SL.

Testplans are located in this directory:

C:\Program Files\Agilent\TS-5000 System Software\Service\U8970A\Testplans

Topology files are located in this directory:

C:\Program Files\Agilent\TS-5000 System Software\Service\U8970A\Ust

4 Load the topology file (*. ust) of the hardware to be tested and edit the Modules folder content:

- Disable - Check to disable. Uncheck to enable. Depends on availability of the module in the system.
- Set "Slot #" - Depends on the slot number the card is installed on the Switch Load Unit. (Applicable to SLU cards only)
- Set "Instrument Descriptor/Resource" - LXI, PXI, GPIB module address. Obtained from Agilent IO Libraries Suite. (VISA Address)
- Set "PCI Slot Number" and "Serial Number" - Depends on the installed Softing CAN.

Once complete editing, save and close the topology file.

5 Load the testplan together with its corresponding topology file. Before running the testplan, identify the instrumentation configuration you want to test in the first lines of the testplan as shown on Figure 3-2. Place a 1 next to instrument configuration you want to test, a 0 next to those instrument configurations you do not want to test (or that are not in your system).

6 Click  to run the testplan. The testplan will run tests on each system instrument configuration specified in step 5 and display the results of the testing.

7 Follow the instructions appearing on the display throughout the test.

8 Repeat step 4 until all instrumentation available in your system are tested.

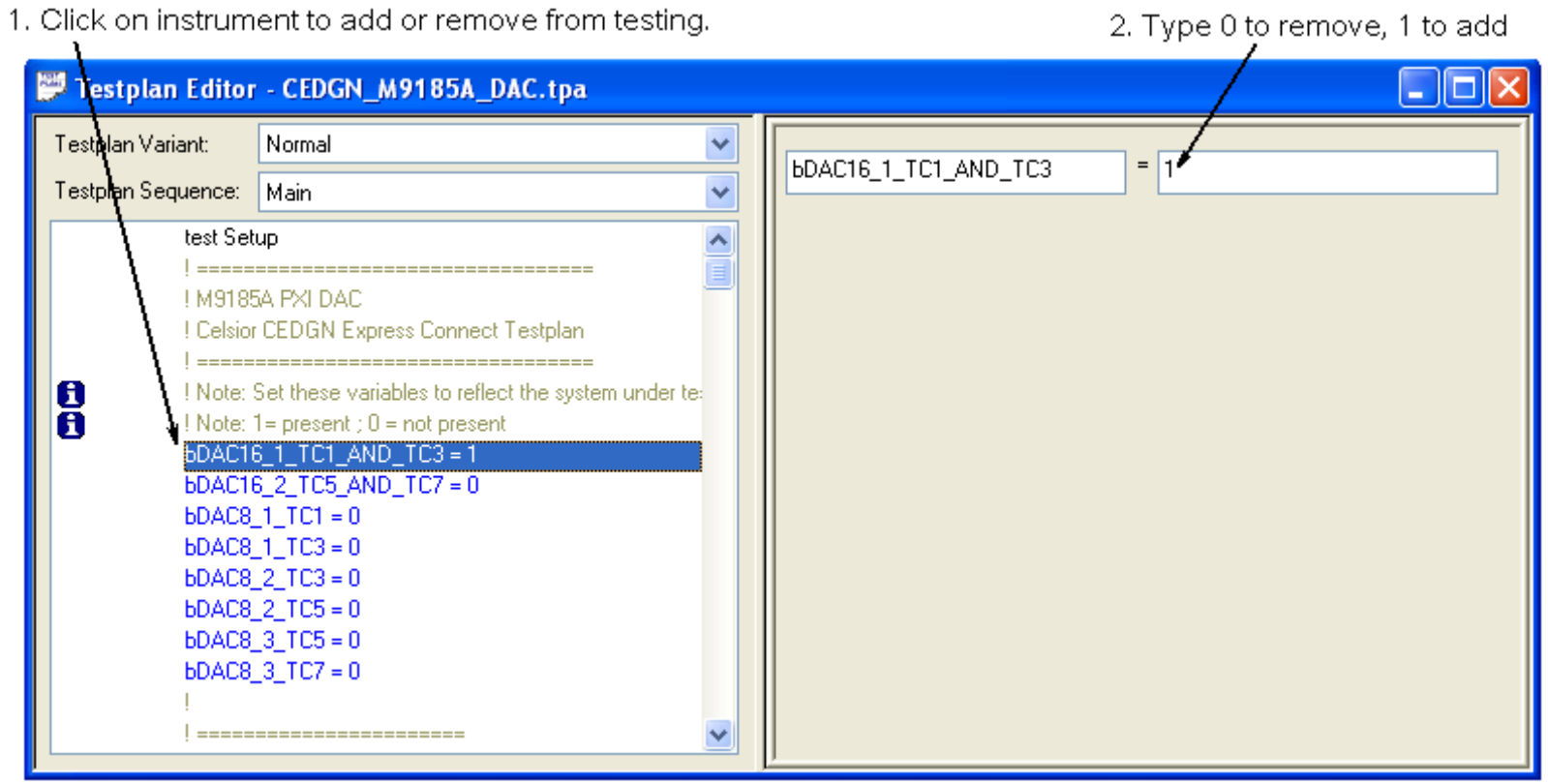


Figure 3-2 Specify the Instruments to be Tested in CEDGN Testplan

Installing the Diagnostic Test Fixture

While running the CEDGN testplan, specific diagnostic test fixtures are required to install on the Test System Interface based on the message prompted. Figure 3-3 shows the CEDGN Board #1 (U8970-66603) to TC1 and CEDGN Board #3 (U8970-66605) to TC4. Both boards are linked by Cable (E6170-61607). This fixture configuration is used to test the connectivity and instrumentations functionality in TC4.

Figure 3-3 Installing CEDGN Board #1 (U8970-66603) to TC1 and CEDGN Board #3 (U8970-66605) to TC4 with both boards linked by cable (E6170-61607).

Figure 3-4 shows connection of 8-Ch Heavy Duty Card diagnostic cable E6170-61618. The Positronic connector on HP2 and cable to Abuses. This diagnostic cable is used to test the connectivity of 8-Ch Heavy Duty Card on HP2.

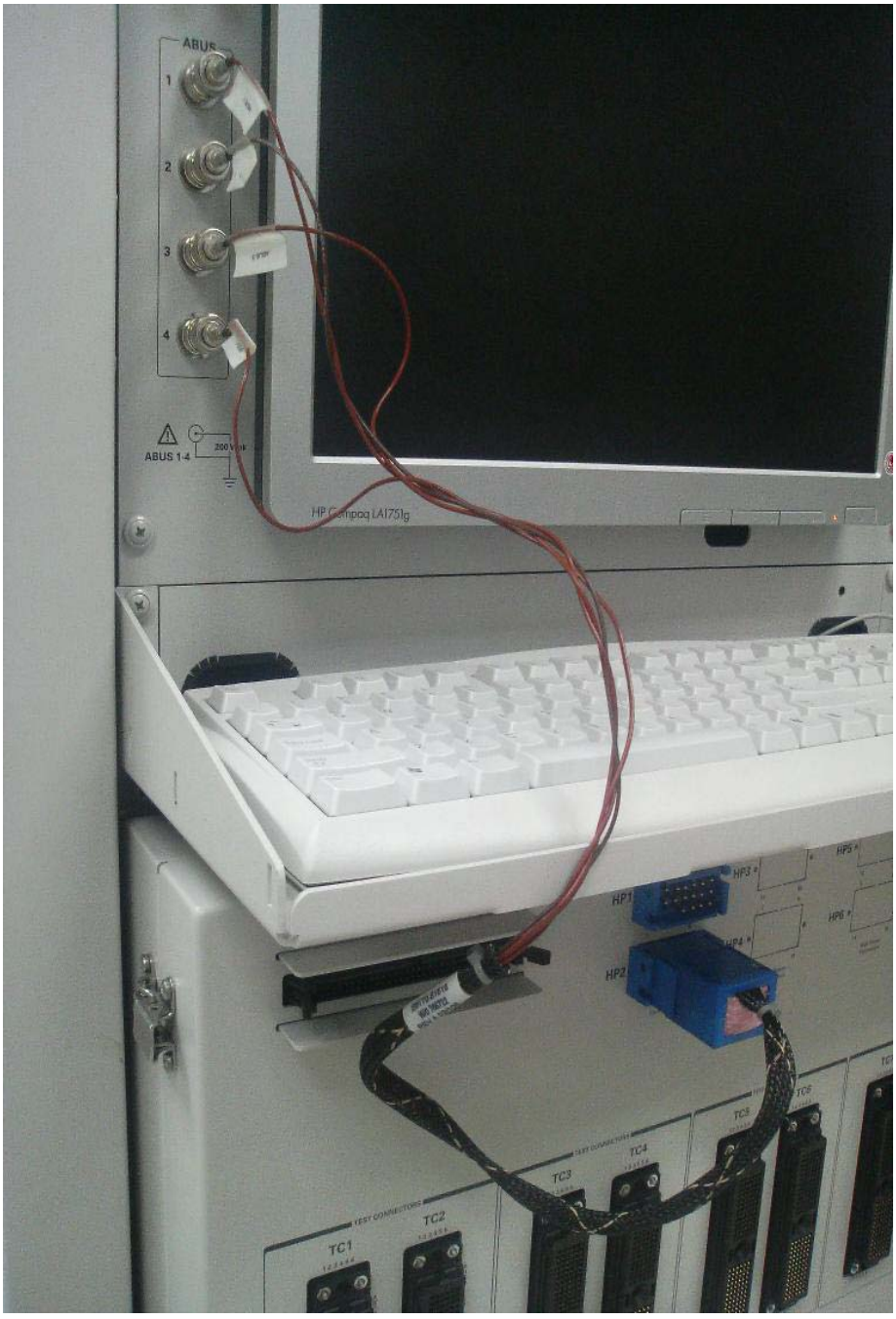


Figure 3-4 Installing 8-Ch Heavy Duty Card diagnostic cable E6170-61618 on HP2 and BNC connectors to Abus1, Abus2, Abus3 and Abus4.

Resolving Test Failures

Test failures can be caused by improper switch settings on the Diagnostic Test Fixture, improper system equipment specification, or the actual test system instrument failure.

Before troubleshooting the system equipment, make sure the test fixture switches are properly set and the test system instrumentation is properly specified. If the problem appears to be system equipment, swap the instrument and/or the cable between the instrument and the Test System Interface.

Chapter 4 contains detailed descriptions of each test that may help in isolating equipment problems to a particular component.

4
Diagnostic Testing Details

DGN Testplan Description and Flow

The standard DGN diagnostic program consists of tests designed for specific system subassemblies. Generally, DGN tests are organized as follows:

- System reset.
- Test of other instruments, such as tests of the E6198A Switch/Load Unit , 3352xA Arbitrary Waveform Generator , 53220A Counter, power supply, and etc.
- Several tests dedicated to Pin Matrix Modules - open/close relay tests.
- Tests of PXI modules, such as M9186A DAQ, M9185A 8/16-CH DAC, M9187A IO and etc.

NOTE Load cards are not tested by DGN.

NOTE L4451A LXI DAC and PXI module(s) functionality is not tested by DGN.

Test 000: Check Memory
Test 000: Global reset

- This test group gets IPC information, initializes and resets all instruments in the system configuration editor (SCE).

Test 001: M918xA PXI Digital Multimeter
Test 001: ABUS 1, 2, 3, 4

- This test group verifies DMM_Hi and DMM_Lo connection and ABUS float for ABUS 1, 2, 3 and 4.

Test 002: E6198B Agilent Switch/Load unit

- This test group measures SLU DAC#1 & DAC#2 output.

Test 003: 335xA GPIB Arbitrary Waveform Generator

- This tests group consists of 2 tests. First test is performing instrument self test, waits for the instrument to complete the test, and queries the instrument for the results. Second test is generating 5V from Arbitrary Waveform Generator and measure using DMM as shown in Figure 4-1 below.

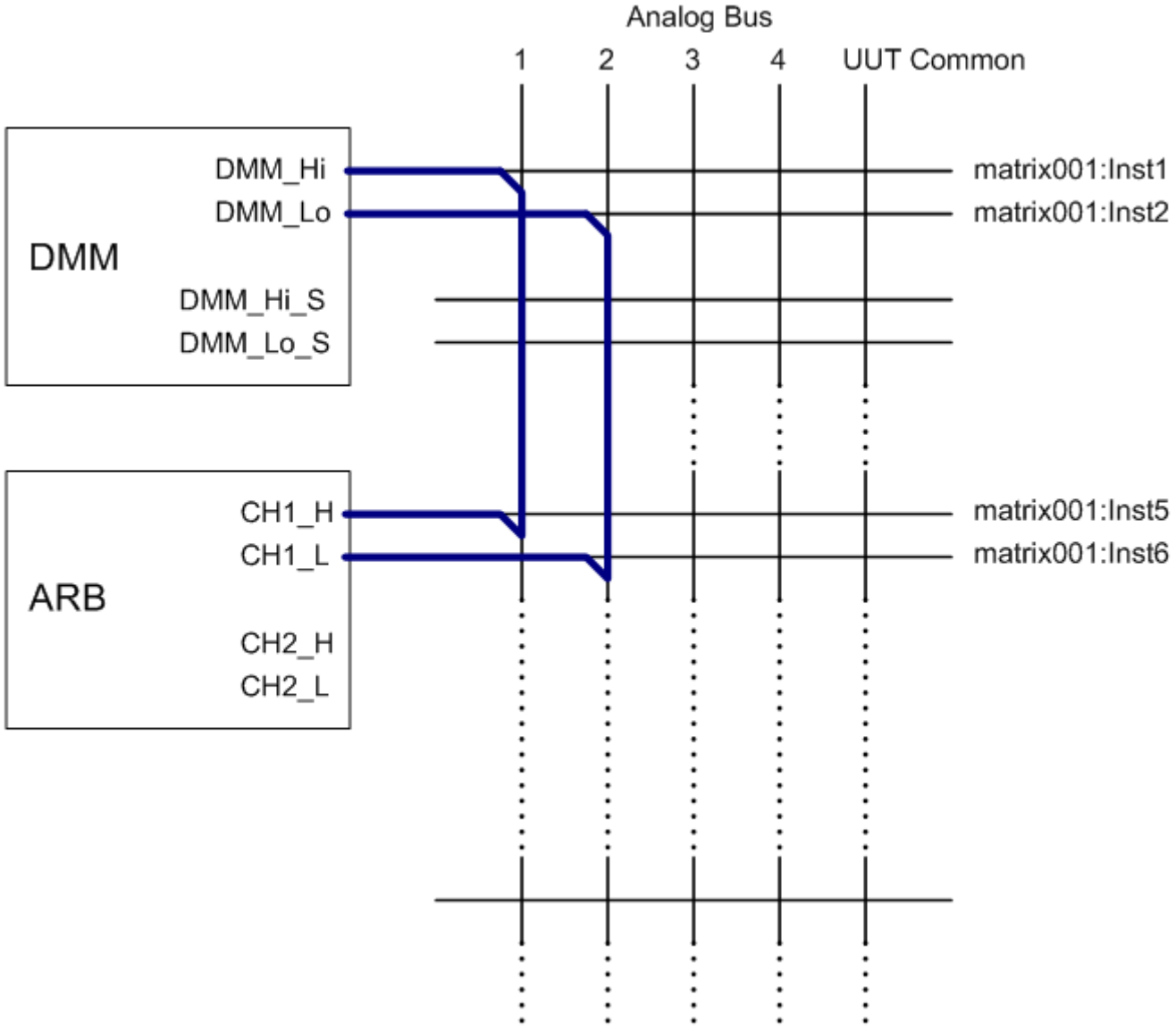


Figure 4-1 Generate 5V from Arbitrary Waveform Generator and measure using DMM.

Test 004: 53220A GPIB Universal Frequency Counter

- This test group consists of 3 tests. First test is performing instrument self test, waits for the instrument to complete the test, and queries the instrument for the results.
- For second test, counter is connected to the DMM. The counter output is enabled and the expected 50 ohms resistance present in matrix path is measured using the DMM and compared to limits. Next, the counter's output is disabled and a High Z resistance measurement is made and compared against limits. Figure 4-2 illustrates this test for Channel 1.

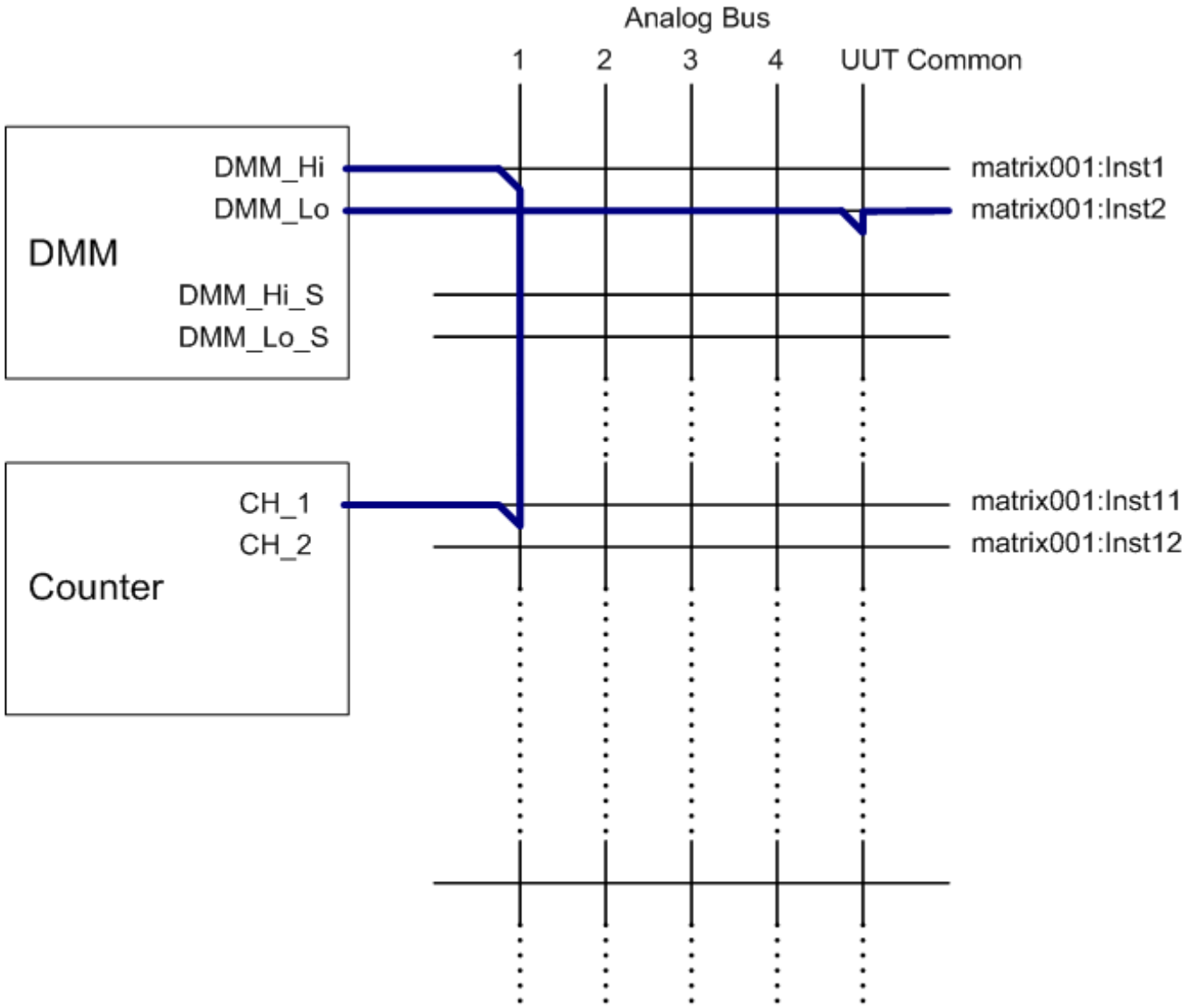


Figure 4-2 Test Counter 50 Ohm and Hi Z for Channel1.

- Third test is required only if ARB is present. The counter output is connected to the ARB output and measures the output signal properties. See Figure 4-3 below.

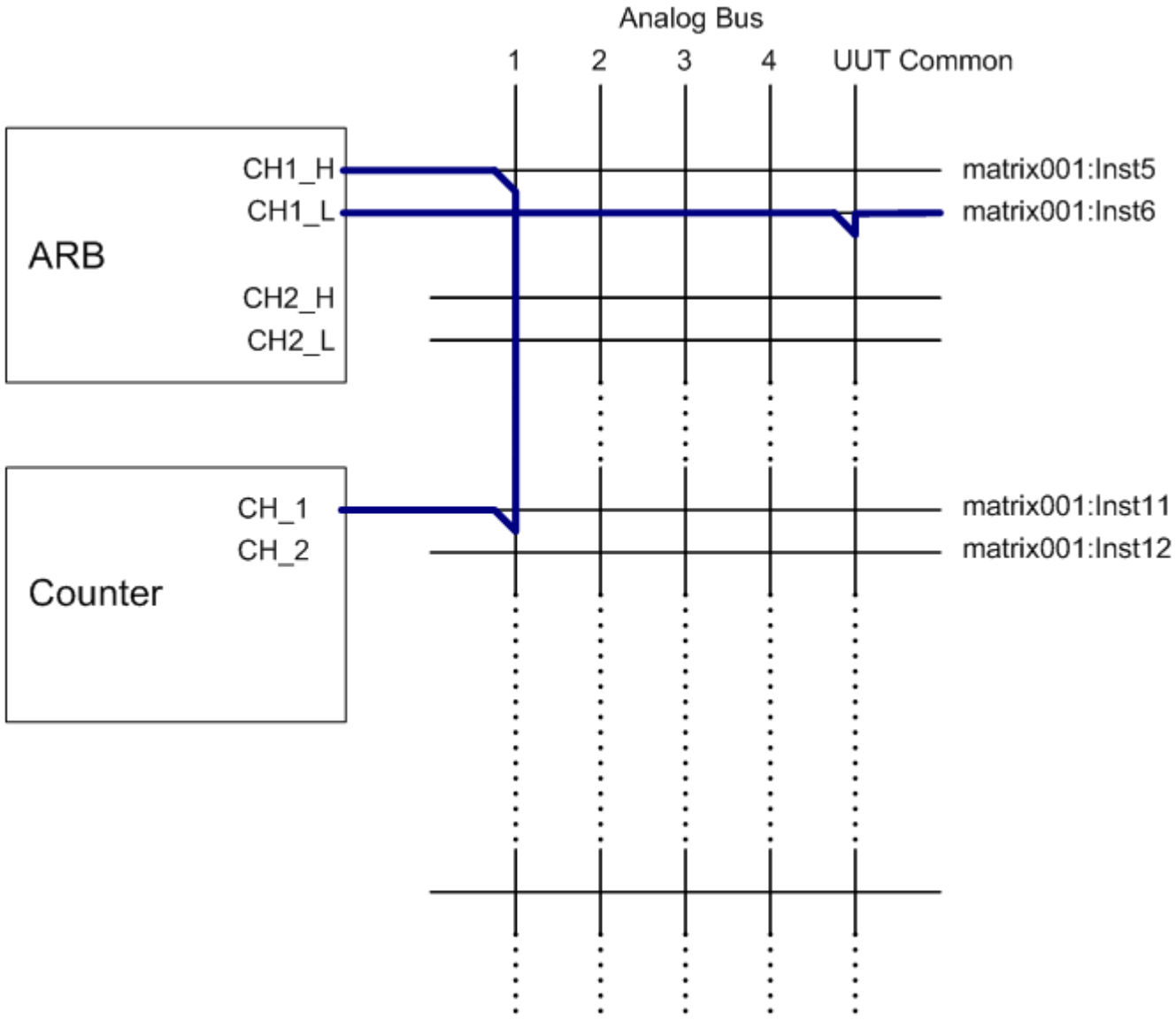


Figure 4-3 Counter measures Arbitrary Waveform Generator output signal properties.

Test 005: L4451A LXI Digital/Analog Converter

- This test group performs instrument self test, waits for the instrument to complete the test, and queries the instrument for the results.

Test 006: L453xA LXI Digitizer

- This test group consists of 3 tests. First test performs instrument self test, waits for the instrument to complete the test, and queries the instrument for the results.
- The second test is required only if ARB is present. The digitizer output is connected to the ARB output and captures the output signal properties. See Figure 4-4 below.

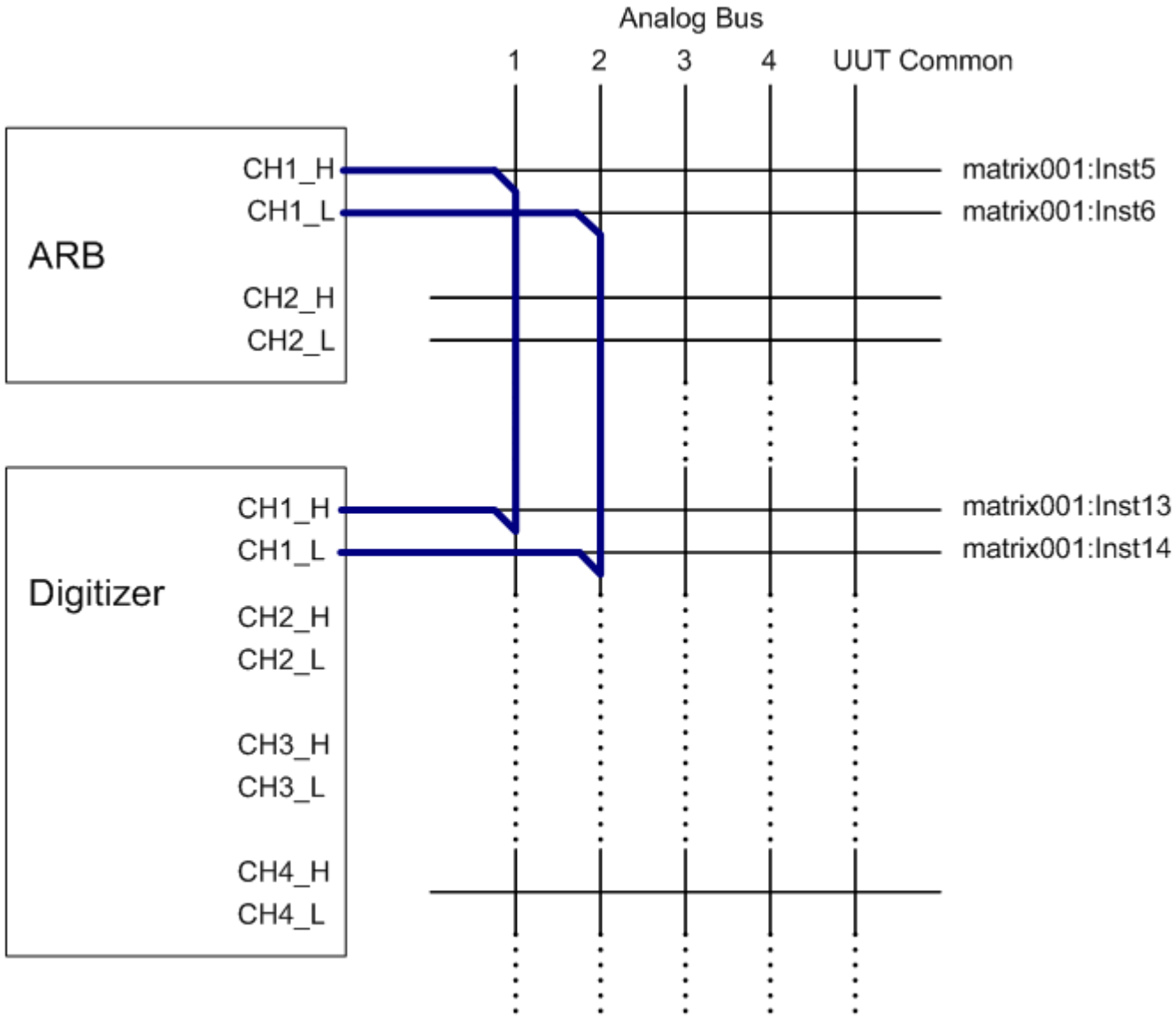


Figure 4-4 Digitizer captures Arbitrary Waveform Generator output signal properties.

Test 007: Power Supply

- This test group performs instrument self test, waits for the instrument to complete the test, and queries the instrument for the results. Repeat test for all selected Agilent power supply.

Test 008: Pin Matrix Relay Open/Close

- This test group consists of matrix row close and open tests. Figure 4-5 and Figure 4-6 illustrate measure short and open by DMM for matrix001:row-1 to matrix001:row-n, where n = 2, 3. . . 63, 64.

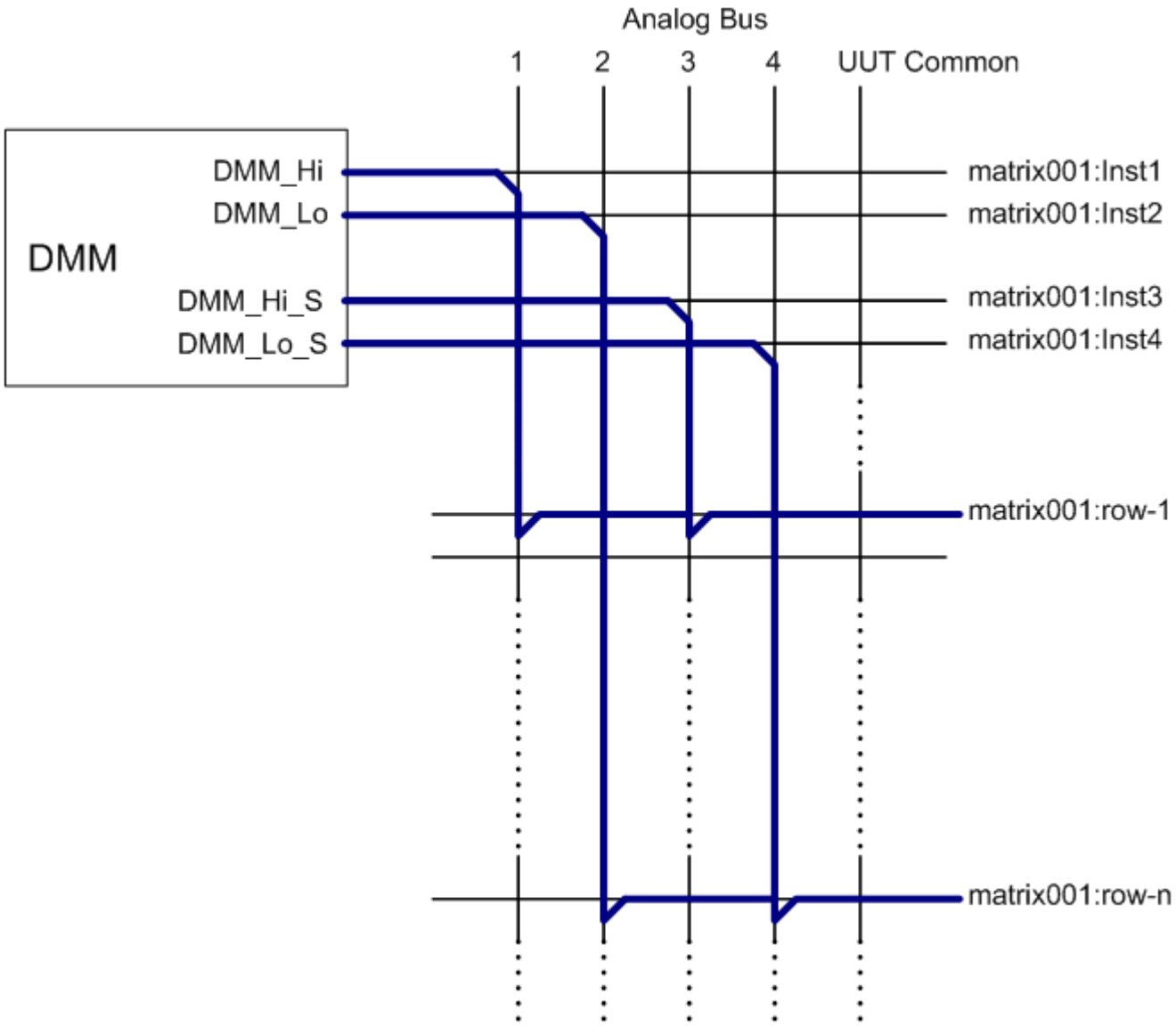


Figure 4-5 Measure short by DMM for matrix row 1 and matrix row-n open.

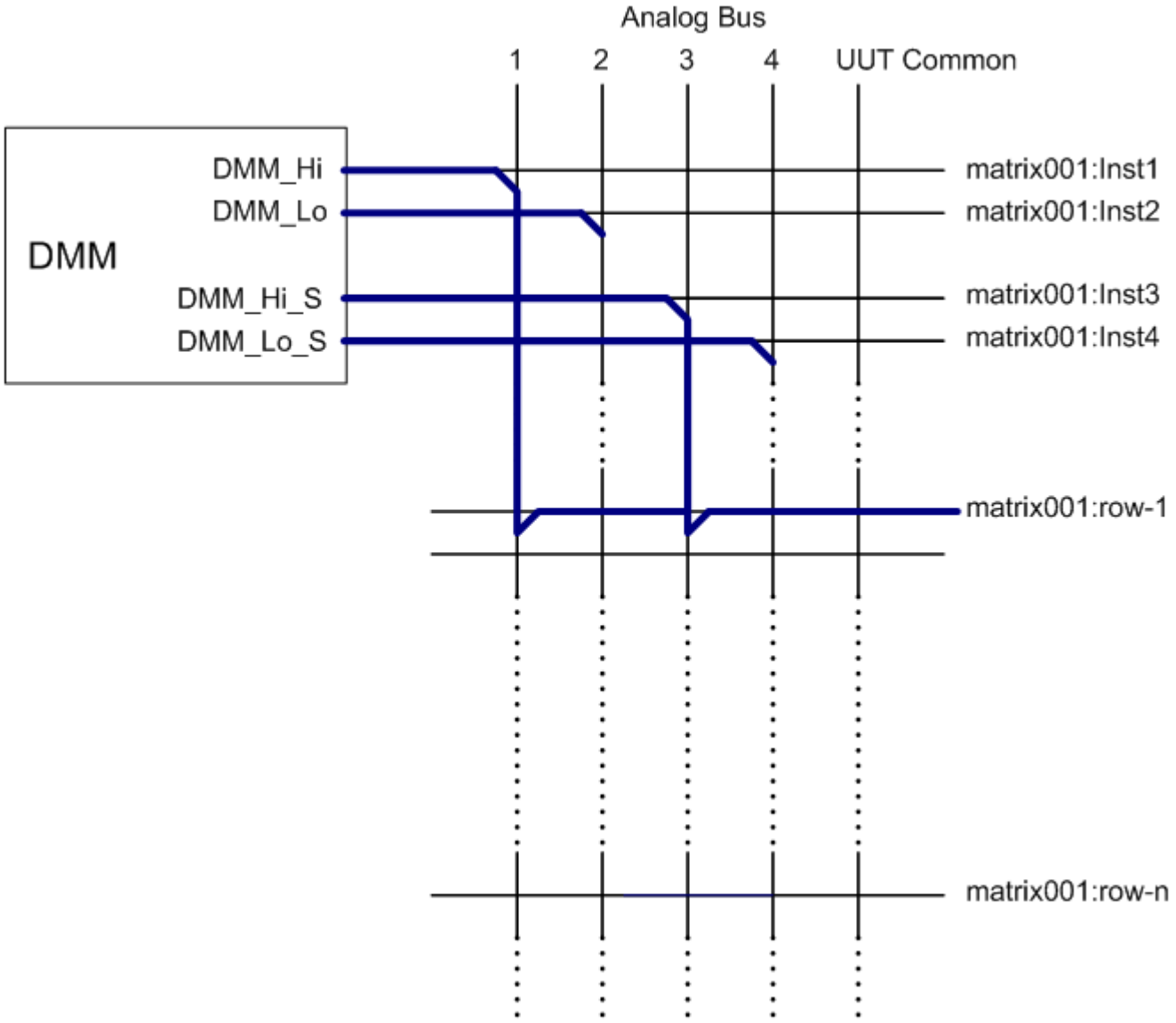


Figure 4-6 Measure open by DMM for matrix row 1 and matrix row-n open.

Test 009: M9216A PXI Data Acquisition (DAQ)
Test 009: M9187A PXI Digital IO
Test 009: M9185A PXI Digital/Analog Converter

- This test group gets information from each selected PXI modules.

Test Fixture Description

The test system uses Express Connect interface, test fixtures below are required to run the CEDGN testplans. Refer to Appendix A for more details.

U8970-66603 PCA-DIAGNOSTIC NUMBER 1 (Board #1)

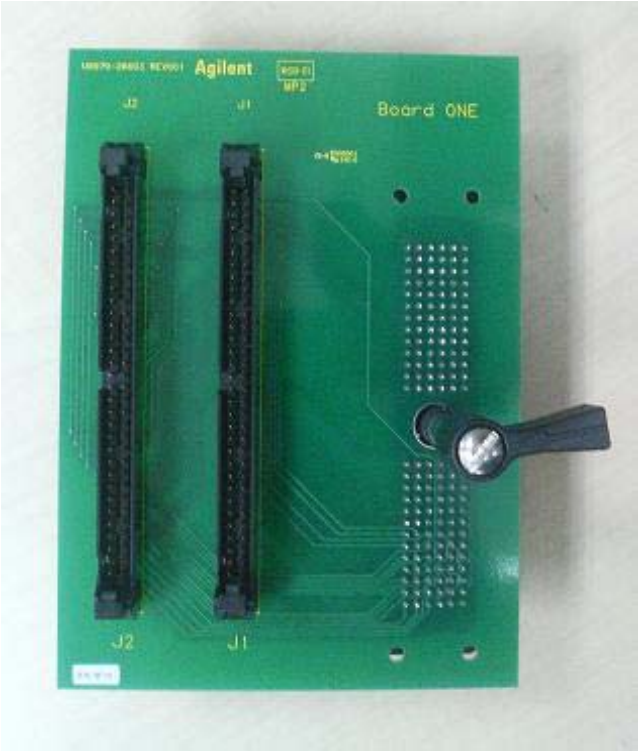


Figure 4-7 CEDGN Board #1 (U8970-66603 PCA- Diagnostic Number 1)

U8970-66604 PCA-DIAGNOSTIC NUMBER 2 (Board #2)

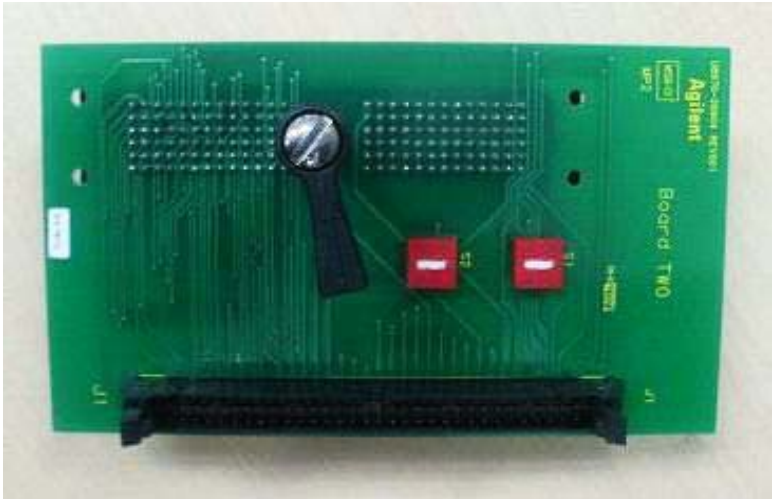


Figure 4-8 CEDGN Board #2 (U8970-66604 PCA- Diagnostic Number 2)

U8970-66605 PCA-DIAGNOSTIC NUMBER 3 (Board #3)

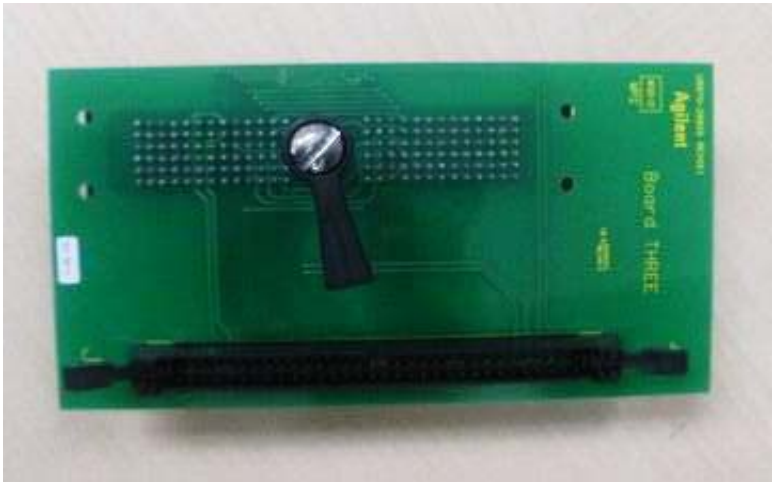


Figure 4-9 CEDGN Board #3 (U8970-66605 PCA- Diagnostic Number 3)

U8970-66606 PCA-DIAGNOSTIC NUMBER 4 (Board #4)

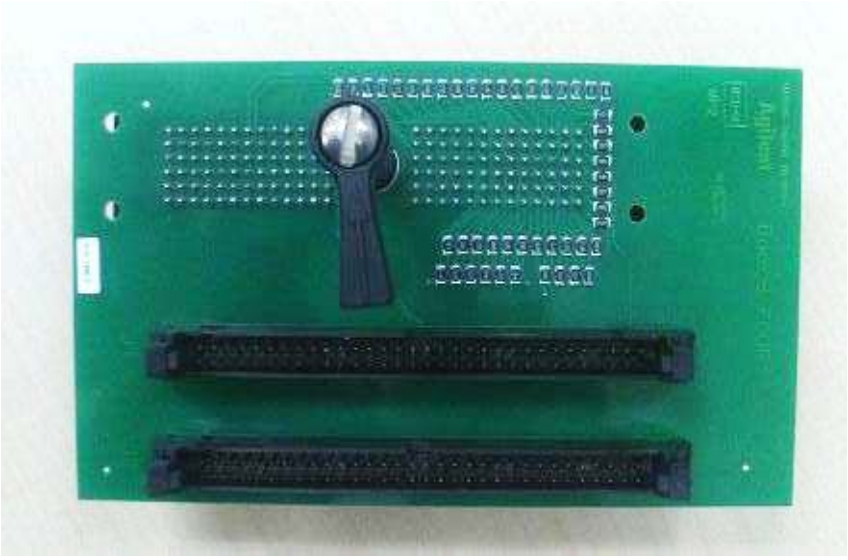


Figure 4-10 CEDGN Board #4 (U8970-66606 PCA- Diagnostic Number 4)

U8970-66607 PCA-DIAGNOSTIC NUMBER 5 (Board #5)

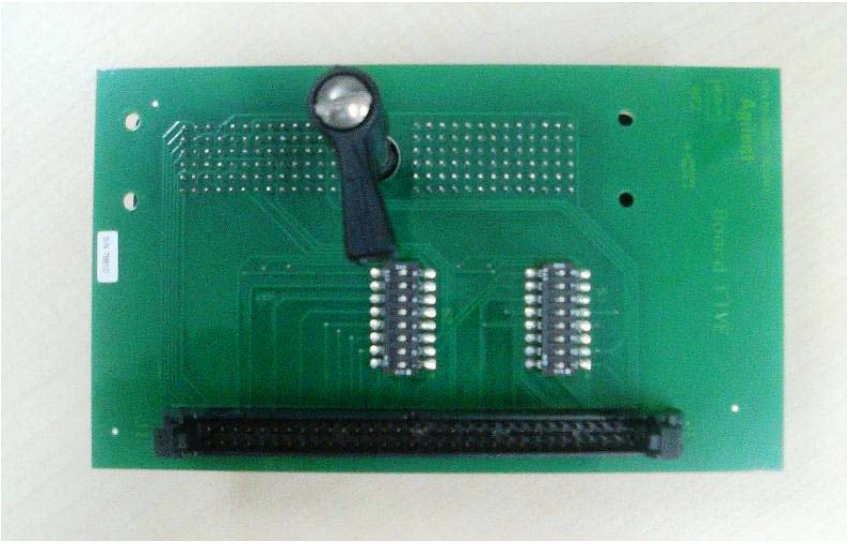


Figure 4-11 CEDGN Board #5 (U8970-66607 PCA- Diagnostic Number 5)

E6170-61607 CABLE 2X 2X32 IDC PIN 1 TO PIN 1

Figure 4-12 CEDGN Cable (E6170-61607 Cable 2X 2X32 IDC Pin 1 To Pin 1)

E6170-61618 Diagnostic Cable

Figure 4-13 Diagnostic Cable (E6170-61618) for 8 Channel Heavy Duty Card

E2240-67012 CEDGN LOOPBACK CONNECTOR

Figure 4-14 CEDGN Loopback Connector (E2240-67012) CEDGN test load module for E6175A, U7177A, and N9377A

E6170-66520 820OHM LOADED MEZZANINE CARD

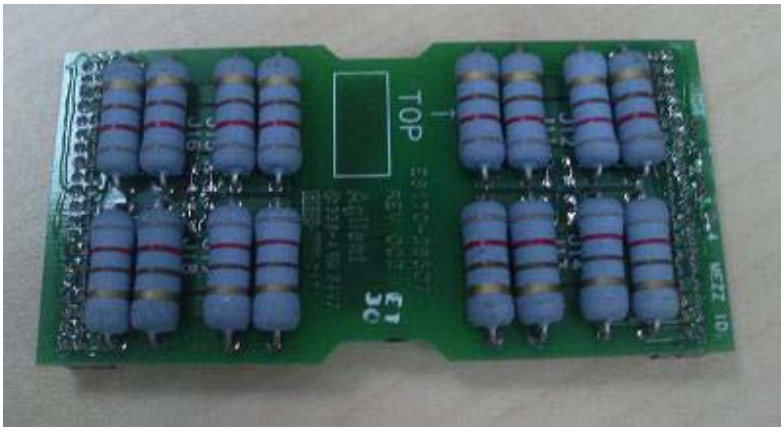


Figure 4-15 820OHM Loaded Mezzanine Card (E6170-66520) CEDGN test load module for N9379A

E6170-61619 CABLE-HEAVY DUTY LOAD JUMPER

Figure 4-16 Heavy Duty Load Card Load Loopback (E6170-61619) CEDGN test load for E6178B

CEDGN Testplan Description and Flow

There are multiple testplans for TS-8900 Functional Test System. Each testplan tests specific instrument / module / card. Each testplan is accompanied by a topolgy file.

Below is the list of CEDGN testplans.

Table 4-1 CEDGN Testplan Description and Flow

Testplan Filename	Topology filename	Description
CEDGN_E878XA_PinMatrix.tpa	CEDGN_E878XA_PinMatrix.ust	SLU E8782A/E8783A Pin Matrix Card CEDGN Test
CEDGN_E6175A_LoadCard.tpa	CEDGN_E6175A_LoadCard.ust	SLU E6175A 8 Channel Load Card Test
CEDGN_U7177A_LoadCard.tpa	CEDGN_U7177A_LoadCard.ust	SLU U7177A 24 Channel Load Card CEDGN Test
CEDGN_E6178B_LoadCard.tpa	CEDGN_E6178B_LoadCard.ust	SLU E6178B 8 Channel Hi Power Load Card Test
CEDGN_N9377A_LoadCard.tpa	CEDGN_N9377A_LoadCard.ust	SLU N9377A 16 Channel Load Card CEDGN Test
CEDGN_N9379A_LoadCard.tpa	CEDGN_N9379A_LoadCard.ust	SLU N9379A 48 Channel Load Card CEDGN Test
CEDGN_E6198B_Utility.tpa	CEDGN_E6198B_Utility.ust	E6198B SLU Mainframe Utility CEDGN Test
CEDGN_L4451A_LXIDAC.tpa	CEDGN_L4451A_LXIDAC.ust	LXI L4451A 4 Channel DAC CEDGN Test
CEDGN_M9185A_DAC.tpa	CEDGN_M9185A_DAC.ust	PXI M9185A 8/16 Channel DAC CEDGN Test
CEDGN_M9186A_VI.tpa	CEDGN_M9186A_VI.ust	PXI M9186A Voltage Current Source CEDGN Test
CEDGN_M9187A_DIO.tpa	CEDGN_M9187A_DIO.ust	PXI M9187A Digital IO CEDGN Test
CEDGN_M9216A_DAQ.tpa	CEDGN_M9216A_DAQ.ust	PXI M9216A HV DAQ CEDGN Test
CEDGN_RS232.tpa	CEDGN_RS232.ust	RS-232 COM port CEDGN Test
CEDGN_SoftingCAN.tpa	CEDGN_SoftingCAN.ust	Softing CAN CEDGN Test

The following paragraphs describe the test flow of each testplan.

CEDGN_E878XA_PinMatrix.tpa (Pin Matrix CEDGN Test Flow)

The testsplan supports testing of one E8782A and four E8783A Pin Matrix Card. User is required to set the variables to reflect the system under test.
1 = present, 0 = not present

bMtrx1 = 1st Pin Matrix E8782A
bMtrx2 = 2ndPin Matrix E8783A
bMtrx3 = 3rd Pin Matrix E8783A
bMtrx4 = 4th Pin Matrix E8783A
bMtrx5 = 5th Pin Matrix E8783A

Device that user sets as not present will not be tested. The test starts by performing:

Not Acceptable Combination Checking

- Checks user settings for any not acceptable combination. Stops test and provide error message if not acceptable selection is found.

Matrix1 E8782A on TC1 Tests

- Display instruction to Install CEDGN Board #5 on TC1. S1 and S2 on CEDGN Board #5 are all toggled to ON (CLOSE).
- Setup DMM for 4W resistance measurement.
- Perform Matrix1 loopback resistance measurements between Row1-Row2, Row3-Row4, until Row31-Row32.

Matrix2 Row1-Row32

- Display instruction to Install CEDGN Board #5 on appropriate TC. S1 and S2 on CEDGN Board #5 are all toggled to ON (CLOSE).

Matrix2 E8783A Row1-Row32 Tests

- Setup DMM for 4W resistance measurement.
- Perform Matrix2 loopback resistance measurements between Row1-Row2, Row3-Row4, until Row31-Row32.

Matrix2 Row33-Row64

- Display instruction to Install CEDGN Board #5 on appropriate TC. S1 and S2 on CEDGN Board #5 are all toggled to ON (CLOSE).

Matrix2 E8783A Row33-Row64 Tests

- Setup DMM for 4W resistance measurement.
- Perform Matrix2 loopback resistance measurements between Row33-Row34, Row35-Row36, until Row63-Row64.

Matrix3 Row1-Row32

- Display instruction to Install CEDGN Board #5 on appropriate TC. S1 and S2 on CEDGN Board #5 are all toggled to ON (CLOSE).

Matrix3 E8783A Row1-Row32 Tests

- Setup DMM for 4W resistance measurement.
- Perform Matrix3 loopback resistance measurements between Row1-Row2, Row3-Row4, until Row31-Row32.

Matrix3 Row33-Row64

- Display instruction to Install CEDGN Board #5 on appropriate TC. S1 and S2 on CEDGN Board #5 are all toggled to ON (CLOSE).

Matrix3 E8783A Row33-Row64 Tests

- Setup DMM for 4W resistance measurement.
- Perform Matrix3 loopback resistance measurements between Row33-Row34, Row35-Row36, until Row63-Row64.

Matrix4 Row1-Row32

- Display instruction to Install CEDGN Board #5 on appropriate TC. S1 and S2 on CEDGN Board #5 are all toggled to ON (CLOSE).

Matrix4 E8783A Row1-Row32 Tests

- Setup DMM for 4W resistance measurement.
- Perform Matrix4 loopback resistance measurements between Row1-Row2, Row3-Row4, until Row31-Row32.

Matrix4 Row33-Row64

- Display instruction to Install CEDGN Board #5 on appropriate TC. S1 and S2 on CEDGN Board #5 are all toggled to ON (CLOSE).

Matrix4 E8783A Row33-Row64 Tests

- Setup DMM for 4W resistance measurement.
- Perform Matrix4 loopback resistance measurements between Row33-Row34, Row35-Row36, until Row63-Row64.

Matrix5 Row1-Row32

- Display instruction to Install CEDGN Board #5 on TC8. S1 and S2 on CEDGN Board #5 are all toggled to ON (CLOSE).

Matrix5 E8783A Row1-Row32 Tests

- Setup DMM for 4W resistance measurement.
- Perform Matrix5 loopback resistance measurements between Row1-Row2, Row3-Row4, until Row31-Row32.

Matrix 1 Aux 1-8 Testing

- Display instruction to Install CEDGN Board #2 on TC1. S1 and S2 on CEDGN Board #2 are toggle to DOWN position.
- Setup DMM for 4W resistance measurement.
- Perform Matrix1 loopback resistance measurements between Aux1-Aux2, Aux3-Aux4, Aux5-Aux6 and Aux7-Aux8.

Matrix 1 Aux 33-40 Testing

- Display instruction to Install CEDGN Board #2 on TC3. S1 and S2 on CEDGN Board #2 are toggle to DOWN position.
- Setup DMM for 4W resistance measurement.
- Perform Matrix1 loopback resistance measurements between Aux33-Aux34, Aux35-Aux36, Aux37-Aux38 and Aux39-Aux40.

Matrix 2 Aux 1-8 Testing

- Display instruction to Install CEDGN Board #2 on TC5. S1 and S2 on CEDGN Board #2 are toggle to DOWN position.
- Setup DMM for 4W resistance measurement.
- Perform Matrix2 loopback resistance measurements between Aux1-Aux2, Aux3-Aux4, Aux5-Aux6 and Aux7-Aux8.

Matrix 2 Aux 33-40 Testing

- Display instruction to Install CEDGN Board #2 on TC7. S1 and S2 on CEDGN Board #2 are toggle to DOWN position.
- Setup DMM for 4W resistance measurement.
- Perform Matrix2 loopback resistance measurements between Aux33-Aux34, Aux35-Aux36, Aux37-Aux38 and Aux39-Aux40.

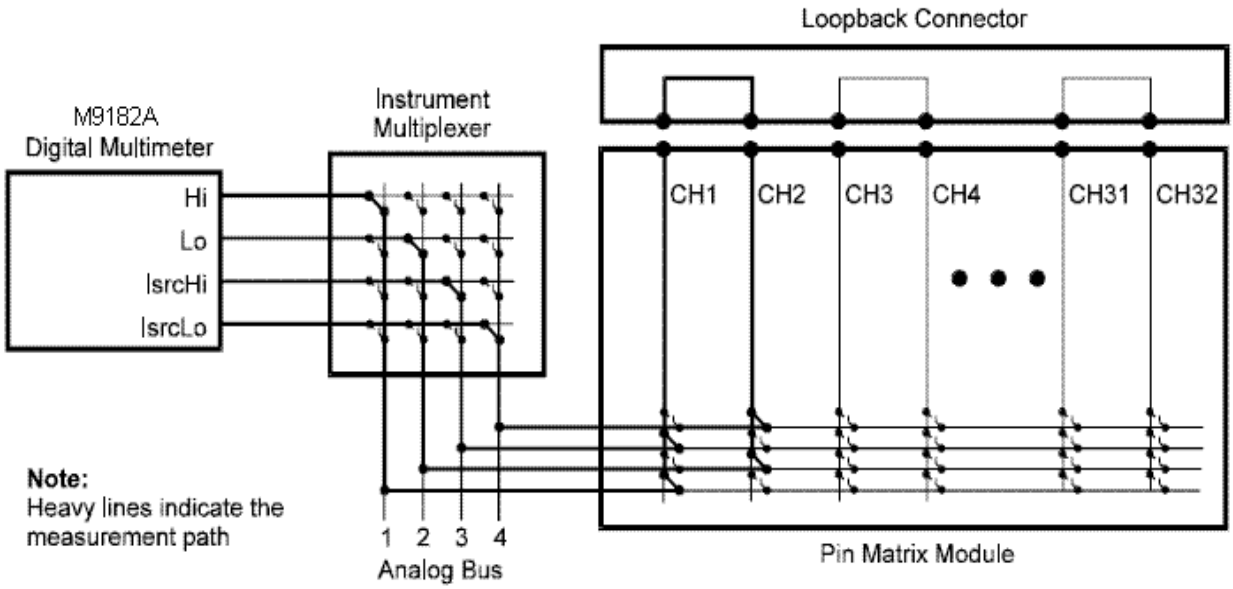


Figure 4-17 Pin Matrix Loopback Test

CEDGN_E6175A_LoadCard.tpa (8 Channel Load Card CEDGN Test Flow)

The testsplan supports testing of eight E6175A Load Cards. User is required to set the variables to reflect the system under test.

1 = present, 0 = not present

bLC8CH_1 = 1st E6175A
bLC8CH_2 = 2nd E6175A
bLC8CH_3 = 3rd E6175A
bLC8CH_4 = 4th E6175A
bLC8CH_5 = 5th E6175A
bLC8CH_6 = 6th E6175A
bLC8CH_7 = 7th E6175A
bLC8CH_8 = 8th E6175A

Device that user sets as not present will not be tested. The test starts by performing:

Not Acceptable Combination Checking

- Checks user settings for any not acceptable combination. Stops test and provide error message if not acceptable selection is found.

E6175A 8 Channel Load Card LC8CH_1 Tests

- Display instruction to Install load module E2240-67012 on LC8CH_1 Load Card.
- For LC8CH_1 on TC1, display instruction to install CEDGN Board #4 on TC1 and Cable E6170-61607 from SLU Utility Connector to J2 of Board #4.
- For LC8CH_1 on other TC, display instruction to install CEDGN Board #1 on TC1 and CEDGN Board #4 on appropriate TC. Install Cable E6170-61607 from SLU Utility Connector to J2 of Board #4. Install Cable E6170-61607 from J1 of Board #1 to J1 of Board #4.
- Setup DMM to perform 2W resistance measurement.
- Measure LC8CH_1 load card loopback path resistance from CH1-CH5, CH2-CH6, CH3-CH7 and CH4-CH8 via Row1 and Row2.
- Measure LC8CH_1 load card sense resistor path:
  CH1 & CH2 Current Sense, CH3 & CH4 Current Sense, CH5 & CH6 Current Sense, and CH7 & CH8 Current Sense via Row25 and Row26.

E6175A 8 Channel Load Card LC8CH_2 Tests

- Display instruction to Install load module E2240-67012 on LC8CH_2 Load Card.
- Display instruction to install CEDGN Board #1 on TC1 and CEDGN Board #4 on appropriate TC. Install Cable E6170-61607 from SLU Utility Connector to J2 of Board #4. Install Cable E6170-61607 from J1 of Board #1 to J1 of Board #4.
- Setup DMM to perform 2W resistance measurement.
- Measure LC8CH_2 load card loopback path resistance from CH1-CH5, CH2-CH6, CH3-CH7 and CH4-CH8 via Row1 and Row2.
- Measure LC8CH_2 load card sense resistor path: CH1 & CH2 Current Sense, CH3 & CH4 Current Sense, CH5 & CH6 Current Sense, and CH7 & CH8 Current Sense via Row25 and Row26.

E6175A 8 Channel Load Card LC8CH_3 Tests

- Display instruction to Install load module E2240-67012 on LC8CH_3 Load Card.
- Display instruction to install CEDGN Board #1 on TC1 and CEDGN Board #4 on appropriate TC. Install Cable E6170-61607 from SLU Utility Connector to J2 of Board #4. Install Cable E6170-61607 from J1 of Board #1 to J1 of Board #4.
- Setup DMM to perform 2W resistance measurement.
- Measure LC8CH_3 load card loopback path resistance from CH1-CH5, CH2-CH6, CH3-CH7 and CH4-CH8 via Row1 and Row2.
- Measure LC8CH_3 load card sense resistor path: CH1 & CH2 Current Sense, CH3 & CH4 Current Sense, CH5 & CH6 Current Sense, and CH7 & CH8 Current Sense via Row25 and Row26.

E6175A 8 Channel Load Card LC8CH_4 Tests

- Display instruction to Install load module E2240-67012 on LC8CH_4 Load Card.
- Display instruction to install CEDGN Board #1 on TC1 and CEDGN Board #4 on appropriate TC. Install Cable E6170-61607 from SLU Utility Connector to J2 of Board #4. Install Cable E6170-61607 from J1 of Board #1 to J1 of Board #4.
- Setup DMM to perform 2W resistance measurement.
- Measure LC8CH_4 load card loopback path resistance from CH1-CH5, CH2-CH6, CH3-CH7 and CH4-CH8 via Row1 and Row2.

- Measure LC8CH_4 load card sense resistor path:
  CH1 & CH2 Current Sense, CH3 & CH4 Current Sense, CH5 & CH6 Current Sense, and CH7 & CH8 Current Sense via Row25 and Row26.

E6175A 8 Channel Load Card LC8CH_5 Tests

- Display instruction to Install load module E2240-67012 on LC8CH_5 Load Card.
- Display instruction to install CEDGN Board #1 on TC1 and CEDGN Board #4 on appropriate TC. Install Cable E6170-61607 from SLU Utility Connector to J2 of Board #4. Install Cable E6170-61607 from J1 of Board #1 to J1 of Board #4.
- Setup DMM to perform 2W resistance measurement.
- Measure LC8CH_5 load card loopback path resistance from CH1-CH5, CH2-CH6, CH3-CH7 and CH4-CH8 via Row1 and Row2.
- Measure LC8CH_5 load card sense resistor path:
  CH1 & CH2 Current Sense, CH3 & CH4 Current Sense, CH5 & CH6 Current Sense, and CH7 & CH8 Current Sense via Row25 and Row26.

E6175A 8 Channel Load Card LC8CH_6 Tests

- Display instruction to Install load module E2240-67012 on LC8CH_6 Load Card.
- Display instruction to install CEDGN Board #1 on TC1 and CEDGN Board #4 on appropriate TC. Install Cable E6170-61607 from SLU Utility Connector to J2 of Board #4. Install Cable E6170-61607 from J1 of Board #1 to J1 of Board #4.
- Setup DMM to perform 2W resistance measurement.
- Measure LC8CH_6 load card loopback path resistance from CH1-CH5, CH2-CH6, CH3-CH7 and CH4-CH8 via Row1 and Row2.
- Measure LC8CH_6 load card sense resistor path:
  CH1 & CH2 Current Sense, CH3 & CH4 Current Sense, CH5 & CH6 Current Sense, and CH7 & CH8 Current Sense via Row25 and Row26.

E6175A 8 Channel Load Card LC8CH_7 Tests

- Display instruction to Install load module E2240-67012 on LC8CH_7 Load Card.
- Display instruction to install CEDGN Board #1 on TC1 and CEDGN Board #4 on appropriate TC. Install Cable E6170-61607 from SLU Utility Connector to J2 of Board #4. Install Cable E6170-61607 from J1 of Board #1 to J1 of Board #4.
- Setup DMM to perform 2W resistance measurement.
- Measure LC8CH_7 load card loopback path resistance from CH1-CH5, CH2-CH6, CH3-CH7 and CH4-CH8 via Row1 and Row2.
- Measure LC8CH_7 load card sense resistor path: CH1 & CH2 Current Sense, CH3 & CH4 Current Sense, CH5 & CH6 Current Sense, and CH7 & CH8 Current Sense via Row25 and Row26.

E6175A 8 Channel Load Card LC8CH_8 Tests

- Display instruction to Install load module E2240-67012 on LC8CH_8 Load Card.
- Display instruction to install CEDGN Board #1 on TC1 and CEDGN Board #4 on appropriate TC. Install Cable E6170-61607 from SLU Utility Connector to J2 of Board #4. Install Cable E6170-61607 from J1 of Board #1 to J1 of Board #4.
- Setup DMM to perform 2W resistance measurement.
- Measure LC8CH_8 load card loopback path resistance from CH1-CH5, CH2-CH6, CH3-CH7 and CH4-CH8 via Row1 and Row2.
- Measure LC8CH_8 load card sense resistor path: CH1 & CH2 Current Sense, CH3 & CH4 Current Sense, CH5 & CH6 Current Sense, and CH7 & CH8 Current Sense via Row25 and Row26.

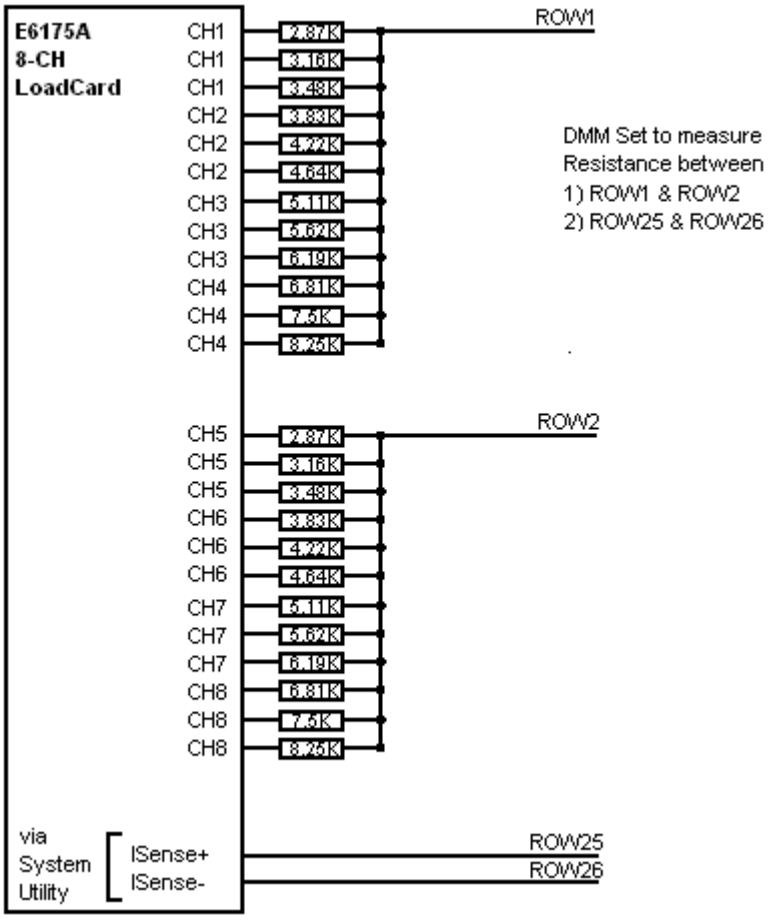


Figure 4-18 E6175A 8 Channel Load Card Test

CEDGN_U7177A_LoadCard.tpa (24 Channel Load Card CEDGN Test Flow)

The testsplan supports testing of eight U7177A Load Cards. User is required to set the variables to reflect the system under test.

1 = present, 0 = not present

bLC24CH_1 = 1st U7177A
bLC24CH_2 = 2nd U7177A
bLC24CH_3 = 3rd U7177A
bLC24CH_4 = 4th U7177A
bLC24CH_5 = 5th U7177A
bLC24CH_6 = 6th U7177A
bLC24CH_7 = 7th U7177A
bLC24CH_8 = 8th U7177A

Device that user sets as not present will not be tested. The test starts by performing:

Not Acceptable Combination Checking

- Checks user settings for any not acceptable combination. Stops test and provide error message if not acceptable selection is found.

U7177A 24 Channel Load Card LC24CH_1 Tests

- Display instruction to Install load module E2240-67012 on LC24CH_1 Load Card.
- For LC24CH_1 on TC1, display instruction to install CEDGN Board #4 on TC1 and Cable E6170-61607 from SLU Utility Connector to J2 of Board #4.
- For LC24CH_1 on other TC, display instruction to install CEDGN Board #1 on TC1 and CEDGN Board #4 on appropriate TC. Install Cable E6170-61607 from SLU Utility Connector to J2 of Board #4. Install Cable E6170-61607 from J1 of Board #1 to J1 of Board #4.
- Setup DMM to perform 2W resistance measurement.
- Measure LC24CH_1 load card loopback path resistance from CH1-Com1 until CH12-Com12 via Row1 and Row8
  CH13-Com13 until CH24-Com24 via Row2 and Row7
- Measure LC24CH_1 load card sense resistor path:
  CH1 Sense until CH24 Sense via Row25 and Row26.

U7177A 24 Channel Load Card LC24CH_2 Tests

- Display instruction to Install load module E2240-67012 on LC24CH_2 Load Card.
- Display instruction to install CEDGN Board #1 on TC1 and CEDGN Board #4 on appropriate TC. Install Cable E6170-61607 from SLU Utility Connector to J2 of Board #4. Install Cable E6170-61607 from J1 of Board #1 to J1 of Board #4.
- Setup DMM to perform 2W resistance measurement.
- Measure LC24CH_2 load card loopback path resistance from CH1-Com1 until CH12-Com12 via Row1 and Row8
  CH13-Com13 until CH24-Com24 via Row2 and Row7
- Measure LC24CH_2 load card sense resistor path:
  CH1 Sense until CH24 Sense via Row25 and Row26.

U7177A 24 Channel Load Card LC24CH_3 Tests

- Display instruction to Install load module E2240-67012 on LC24CH_3 Load Card.
- Display instruction to install CEDGN Board #1 on TC1 and CEDGN Board #4 on appropriate TC. Install Cable E6170-61607 from SLU Utility Connector to J2 of Board #4. Install Cable E6170-61607 from J1 of Board #1 to J1 of Board #4.
- Setup DMM to perform 2W resistance measurement.
- Measure LC24CH_3 load card loopback path resistance from CH1-Com1 until CH12-Com12 via Row1 and Row8
  CH13-Com13 until CH24-Com24 via Row2 and Row7
- Measure LC24CH_3 load card sense resistor path:
  CH1 Sense until CH24 Sense via Row25 and Row26.

U7177A 24 Channel Load Card LC24CH_4 Tests

- Display instruction to Install load module E2240-67012 on LC24CH_4 Load Card.
- Display instruction to install CEDGN Board #1 on TC1 and CEDGN Board #4 on appropriate TC. Install Cable E6170-61607 from SLU Utility Connector to J2 of Board #4. Install Cable E6170-61607 from J1 of Board #1 to J1 of Board #4.
- Setup DMM to perform 2W resistance measurement.
- Measure LC24CH_4 load card loopback path resistance from CH1-Com1 until CH12-Com12 via Row1 and Row8
  CH13-Com13 until CH24-Com24 via Row2 and Row7
- Measure LC24CH_4 load card sense resistor path:
  CH1 Sense until CH24 Sense via Row25 and Row26.

U7177A 24 Channel Load Card LC24CH_5 Tests

- Display instruction to Install load module E2240-67012 on LC24CH_5 Load Card.
- Display instruction to install CEDGN Board #1 on TC1 and CEDGN Board #4 on appropriate TC. Install Cable E6170-61607 from SLU Utility Connector to J2 of Board #4. Install Cable E6170-61607 from J1 of Board #1 to J1 of Board #4.
- Setup DMM to perform 2W resistance measurement.
- Measure LC24CH_5 load card loopback path resistance from CH1-Com1 until CH12-Com12 via Row1 and Row8
  CH13-Com13 until CH24-Com24 via Row2 and Row7
- Measure LC24CH_5 load card sense resistor path:
  CH1 Sense until CH24 Sense via Row25 and Row26.

U7177A 24 Channel Load Card LC24CH_6 Tests

- Display instruction to Install load module E2240-67012 on LC24CH_6 Load Card.
- Display instruction to install CEDGN Board #1 on TC1 and CEDGN Board #4 on appropriate TC. Install Cable E6170-61607 from SLU Utility Connector to J2 of Board #4. Install Cable E6170-61607 from J1 of Board #1 to J1 of Board #4.
- Setup DMM to perform 2W resistance measurement.
- Measure LC24CH_6 load card loopback path resistance from CH1-Com1 until CH12-Com12 via Row1 and Row8
  CH13-Com13 until CH24-Com24 via Row2 and Row7
- Measure LC24CH_6 load card sense resistor path:
  CH1 Sense until CH24 Sense via Row25 and Row26.

U7177A 24 Channel Load Card LC24CH_7 Tests

- Display instruction to Install load module E2240-67012 on LC24CH_7 Load Card.
- Display instruction to install CEDGN Board #1 on TC1 and CEDGN Board #4 on appropriate TC. Install Cable E6170-61607 from SLU Utility Connector to J2 of Board #4. Install Cable E6170-61607 from J1 of Board #1 to J1 of Board #4.
- Setup DMM to perform 2W resistance measurement.
- Measure LC24CH_7 load card loopback path resistance from CH1-Com1 until CH12-Com12 via Row1 and Row8
  CH13-Com13 until CH24-Com24 via Row2 and Row7
- Measure LC24CH_7 load card sense resistor path:
  CH1 Sense until CH24 Sense via Row25 and Row26.

U7177A 24 Channel Load Card LC24CH_8 Tests

- Display instruction to Install load module E2240-67012 on LC24CH_8 Load Card.
- Display instruction to install CEDGN Board #1 on TC1 and CEDGN Board #4 on appropriate TC. Install Cable E6170-61607 from SLU Utility Connector to J2 of Board #4. Install Cable E6170-61607 from J1 of Board #1 to J1 of Board #4.
- Setup DMM to perform 2W resistance measurement.
- Measure LC24CH_8 load card loopback path resistance from CH1-Com1 until CH12-Com12 via Row1 and Row8
  CH13-Com13 until CH24-Com24 via Row2 and Row7
- Measure LC24CH_8 load card sense resistor path:
  CH1 Sense until CH24 Sense via Row25 and Row26.

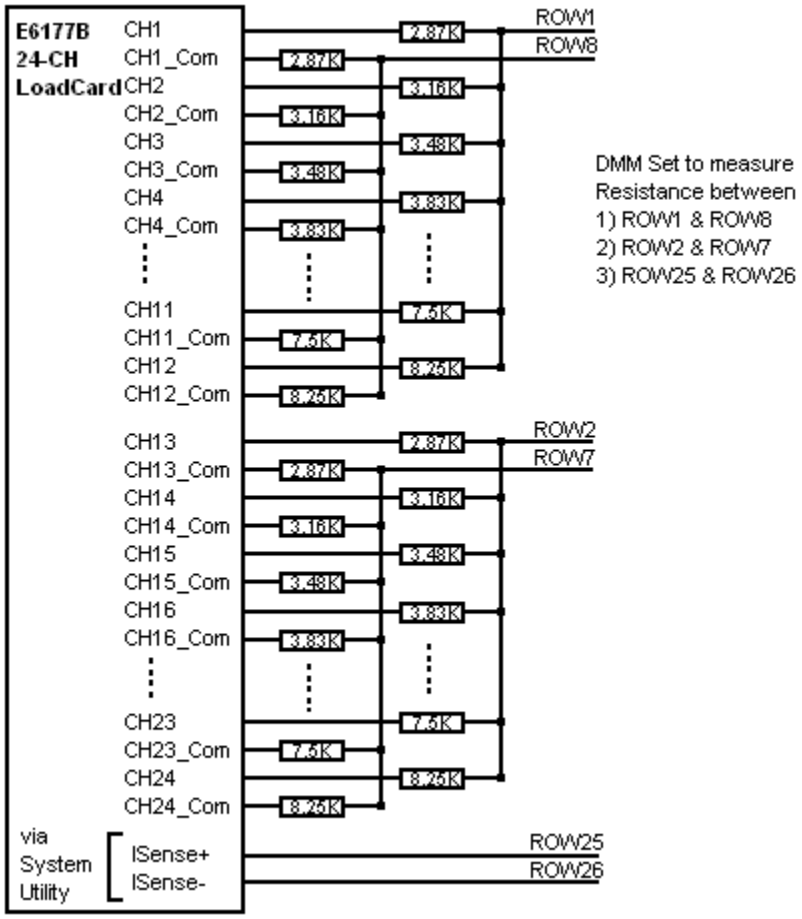


Figure 4-19 U7177A 24 Channel Load Card Test

CEDGN_E6178B_LoadCard.tpa (8 Channel High Power Load Card CEDGN Test Flow)

The testsplan supports testing of eight E6178B High Power Load Cards. User is required to set the variables to reflect the system under test.

1 = present, 0 = not present

bLC8CH_1 = 1st E6178B
bLC8CH_2 = 2nd E6178B
bLC8CH_3 = 3rd E6178B
bLC8CH_4 = 4th E6178B
bLC8CH_5 = 5th E6178B
bLC8CH_6 = 6th E6178B
bLC8CH_7 = 7th E6178B
bLC8CH_8 = 8th E6178B

Device that user sets as not present will not be tested. The test starts by performing:

Not Acceptable Combination Checking

- Checks user settings for any not acceptable combination. Stops test and provide error message if not acceptable selection is found.

E6178B 8 Channel High Power Load Card LC8CH_1 Tests

- Display instruction to disconnect power supply from (P100)PWR1 and (P200)PWR2 of E6178B_1. Short PWR1 to PWR2 of E6178B_1. Install load loopback cable E6170-61619 on E6178B_1. Install Diagnostic Cable (E6170-61618) on appropriate HP connector.
- Setup DMM to perform 2W resistance measurement.
- Measure LC8CH_1 load card loopback path resistance from
  CH1-CH2 via Positronic pin5 and pin11 (ABUS1 & ABUS3)
  CH1-CH2 via Positronic pin6 and pin12 (ABUS2 & ABUS4)
  CH1-CH3 via Positronic pin5 and pin17 (ABUS1 & ABUS3)
  CH1-CH3 via Positronic pin6 and pin18 (ABUS2 & ABUS4)
  CH1-CH4 via Positronic pin5 and pin3 (ABUS1 & ABUS3)
  CH1-CH4 via Positronic pin6 and pin4 (ABUS2 & ABUS4)
  CH1-CH5 via Positronic pin5 and pin9 (ABUS1 & ABUS3)
  CH1-CH5 via Positronic pin6 and pin10 (ABUS2 & ABUS4)
  CH1-CH6 via Positronic pin5 and pin15 (ABUS1 & ABUS3)
  CH1-CH6 via Positronic pin6 and pin16 (ABUS2 & ABUS4)
  CH1-CH7 via Positronic pin5 and pin1 (ABUS1 & ABUS3)
  CH1-CH7 via Positronic pin6 and pin2 (ABUS2 & ABUS4)
  CH1-CH8 via Positronic pin5 and pin7 (ABUS1 & ABUS3)
  CH1-CH8 via Positronic pin6 and pin8 (ABUS2 & ABUS4)

E6178B 8 Channel High Power Load Card LC8CH_2 Tests

- Display instruction to disconnect power supply from (P100)PWR1 and (P200)PWR2 of E6178B_2. Short PWR1 to PWR2 of E6178B_2. Install load loopback cable E6170-61619 on E6178B_2. Install Diagnostic Cable (E6170-61618) on appropriate HP connector.
- Setup DMM to perform 2W resistance measurement.
- Measure LC8CH_2 load card loopback path resistance from
  CH1-CH2 via Positronic pin5 and pin11 (ABUS1 & ABUS3)
  CH1-CH2 via Positronic pin6 and pin12 (ABUS2 & ABUS4)
  CH1-CH3 via Positronic pin5 and pin17 (ABUS1 & ABUS3)
  CH1-CH3 via Positronic pin6 and pin18 (ABUS2 & ABUS4)
  CH1-CH4 via Positronic pin5 and pin3 (ABUS1 & ABUS3)
  CH1-CH4 via Positronic pin6 and pin4 (ABUS2 & ABUS4)
  CH1-CH5 via Positronic pin5 and pin9 (ABUS1 & ABUS3)
  CH1-CH5 via Positronic pin6 and pin10 (ABUS2 & ABUS4)
  CH1-CH6 via Positronic pin5 and pin15 (ABUS1 & ABUS3)
  CH1-CH6 via Positronic pin6 and pin16 (ABUS2 & ABUS4)
  CH1-CH7 via Positronic pin5 and pin1 (ABUS1 & ABUS3)
  CH1-CH7 via Positronic pin6 and pin2 (ABUS2 & ABUS4)
  CH1-CH8 via Positronic pin5 and pin7 (ABUS1 & ABUS3)
  CH1-CH8 via Positronic pin6 and pin8 (ABUS2 & ABUS4)

E6178B 8 Channel High Power Load Card LC8CH_3 Tests

- Display instruction to disconnect power supply from (P100)PWR1 and (P200)PWR2 of E6178B_3. Short PWR1 to PWR2 of E6178B_3. Install load loopback cable E6170-61619 on E6178B_3. Install Diagnostic Cable (E6170-61618) on appropriate HP connector.
- Setup DMM to perform 2W resistance measurement.
- Measure LC8CH_3 load card loopback path resistance from
  CH1-CH2 via Positronic pin5 and pin11 (ABUS1 & ABUS3)
  CH1-CH2 via Positronic pin6 and pin12 (ABUS2 & ABUS4)
  CH1-CH3 via Positronic pin5 and pin17 (ABUS1 & ABUS3)
  CH1-CH3 via Positronic pin6 and pin18 (ABUS2 & ABUS4)
  CH1-CH4 via Positronic pin5 and pin3 (ABUS1 & ABUS3)
  CH1-CH4 via Positronic pin6 and pin4 (ABUS2 & ABUS4)
  CH1-CH5 via Positronic pin5 and pin9 (ABUS1 & ABUS3)
  CH1-CH5 via Positronic pin6 and pin10 (ABUS2 & ABUS4)
  CH1-CH6 via Positronic pin5 and pin15 (ABUS1 & ABUS3)
  CH1-CH6 via Positronic pin6 and pin16 (ABUS2 & ABUS4)
  CH1-CH7 via Positronic pin5 and pin1 (ABUS1 & ABUS3)
  CH1-CH7 via Positronic pin6 and pin2 (ABUS2 & ABUS4)
  CH1-CH8 via Positronic pin5 and pin7 (ABUS1 & ABUS3)
  CH1-CH8 via Positronic pin6 and pin8 (ABUS2 & ABUS4)

E6178B 8 Channel High Power Load Card LC8CH_4 Tests

- Display instruction to disconnect power supply from (P100)PWR1 and (P200)PWR2 of E6178B_4. Short PWR1 to PWR2 of E6178B_4. Install load loopback cable E6170-61619 on E6178B_4. Install Diagnostic Cable (E6170-61618) on appropriate HP connector.
- Setup DMM to perform 2W resistance measurement.
- Measure LC8CH_4 load card loopback path resistance from
  CH1-CH2 via Positronic pin5 and pin11 (ABUS1 & ABUS3)
  CH1-CH2 via Positronic pin6 and pin12 (ABUS2 & ABUS4)
  CH1-CH3 via Positronic pin5 and pin17 (ABUS1 & ABUS3)
  CH1-CH3 via Positronic pin6 and pin18 (ABUS2 & ABUS4)
  CH1-CH4 via Positronic pin5 and pin3 (ABUS1 & ABUS3)
  CH1-CH4 via Positronic pin6 and pin4 (ABUS2 & ABUS4)
  CH1-CH5 via Positronic pin5 and pin9 (ABUS1 & ABUS3)
  CH1-CH5 via Positronic pin6 and pin10 (ABUS2 & ABUS4)
  CH1-CH6 via Positronic pin5 and pin15 (ABUS1 & ABUS3)
  CH1-CH6 via Positronic pin6 and pin16 (ABUS2 & ABUS4)
  CH1-CH7 via Positronic pin5 and pin1 (ABUS1 & ABUS3)
  CH1-CH7 via Positronic pin6 and pin2 (ABUS2 & ABUS4)
  CH1-CH8 via Positronic pin5 and pin7 (ABUS1 & ABUS3)
  CH1-CH8 via Positronic pin6 and pin8 (ABUS2 & ABUS4)

E6178B 8 Channel High Power Load Card LC8CH_5 Tests

- Display instruction to disconnect power supply from (P100)PWR1 and (P200)PWR2 of E6178B_5. Short PWR1 to PWR2 of E6178B_5. Install load loopback cable E6170-61619 on E6178B_5. Install Diagnostic Cable (E6170-61618) on appropriate HP connector.
- Setup DMM to perform 2W resistance measurement.
- Measure LC8CH_5 load card loopback path resistance from
  CH1-CH2 via Positronic pin5 and pin11 (ABUS1 & ABUS3)
  CH1-CH2 via Positronic pin6 and pin12 (ABUS2 & ABUS4)
  CH1-CH3 via Positronic pin5 and pin17 (ABUS1 & ABUS3)
  CH1-CH3 via Positronic pin6 and pin18 (ABUS2 & ABUS4)
  CH1-CH4 via Positronic pin5 and pin3 (ABUS1 & ABUS3)
  CH1-CH4 via Positronic pin6 and pin4 (ABUS2 & ABUS4)
  CH1-CH5 via Positronic pin5 and pin9 (ABUS1 & ABUS3)
  CH1-CH5 via Positronic pin6 and pin10 (ABUS2 & ABUS4)
  CH1-CH6 via Positronic pin5 and pin15 (ABUS1 & ABUS3)
  CH1-CH6 via Positronic pin6 and pin16 (ABUS2 & ABUS4)
  CH1-CH7 via Positronic pin5 and pin1 (ABUS1 & ABUS3)
  CH1-CH7 via Positronic pin6 and pin2 (ABUS2 & ABUS4)
  CH1-CH8 via Positronic pin5 and pin7 (ABUS1 & ABUS3)
  CH1-CH8 via Positronic pin6 and pin8 (ABUS2 & ABUS4)

E6178B 8 Channel High Power Load Card LC8CH_6 Tests

- Display instruction to disconnect power supply from (P100)PWR1 and (P200)PWR2 of E6178B_6. Short PWR1 to PWR2 of E6178B_6. Install load loopback cable E6170-61619 on E6178B_6. Install Diagnostic Cable (E6170-61618) on appropriate HP connector.
- Setup DMM to perform 2W resistance measurement.
- Measure LC8CH_6 load card loopback path resistance from
  CH1-CH2 via Positronic pin5 and pin11 (ABUS1 & ABUS3)
  CH1-CH2 via Positronic pin6 and pin12 (ABUS2 & ABUS4)
  CH1-CH3 via Positronic pin5 and pin17 (ABUS1 & ABUS3)
  CH1-CH3 via Positronic pin6 and pin18 (ABUS2 & ABUS4)
  CH1-CH4 via Positronic pin5 and pin3 (ABUS1 & ABUS3)
  CH1-CH4 via Positronic pin6 and pin4 (ABUS2 & ABUS4)
  CH1-CH5 via Positronic pin5 and pin9 (ABUS1 & ABUS3)
  CH1-CH5 via Positronic pin6 and pin10 (ABUS2 & ABUS4)
  CH1-CH6 via Positronic pin5 and pin15 (ABUS1 & ABUS3)
  CH1-CH6 via Positronic pin6 and pin16 (ABUS2 & ABUS4)
  CH1-CH7 via Positronic pin5 and pin1 (ABUS1 & ABUS3)
  CH1-CH7 via Positronic pin6 and pin2 (ABUS2 & ABUS4)
  CH1-CH8 via Positronic pin5 and pin7 (ABUS1 & ABUS3)
  CH1-CH8 via Positronic pin6 and pin8 (ABUS2 & ABUS4)

E6178B 8 Channel High Power Load Card LC8CH_7 Tests

- Display instruction to disconnect power supply from (P100)PWR1 and (P200)PWR2 of E6178B_7. Short PWR1 to PWR2 of E6178B_7. Install load loopback cable E6170-61619 on E6178B_7. Install Diagnostic Cable (E6170-61618) on appropriate HP connector.
- Setup DMM to perform 2W resistance measurement.
- Measure LC8CH_7 load card loopback path resistance from
  CH1-CH2 via Positronic pin5 and pin11 (ABUS1 & ABUS3)
  CH1-CH2 via Positronic pin6 and pin12 (ABUS2 & ABUS4)
  CH1-CH3 via Positronic pin5 and pin17 (ABUS1 & ABUS3)
  CH1-CH3 via Positronic pin6 and pin18 (ABUS2 & ABUS4)
  CH1-CH4 via Positronic pin5 and pin3 (ABUS1 & ABUS3)
  CH1-CH4 via Positronic pin6 and pin4 (ABUS2 & ABUS4)
  CH1-CH5 via Positronic pin5 and pin9 (ABUS1 & ABUS3)
  CH1-CH5 via Positronic pin6 and pin10 (ABUS2 & ABUS4)
  CH1-CH6 via Positronic pin5 and pin15 (ABUS1 & ABUS3)
  CH1-CH6 via Positronic pin6 and pin16 (ABUS2 & ABUS4)
  CH1-CH7 via Positronic pin5 and pin1 (ABUS1 & ABUS3)
  CH1-CH7 via Positronic pin6 and pin2 (ABUS2 & ABUS4)
  CH1-CH8 via Positronic pin5 and pin7 (ABUS1 & ABUS3)
  CH1-CH8 via Positronic pin6 and pin8 (ABUS2 & ABUS4)

E6178B 8 Channel High Power Load Card LC8CH_8 Tests

- Display instruction to disconnect power supply from (P100)PWR1 and (P200)PWR2 of E6178B_8. Short PWR1 to PWR2 of E6178B_8. Install load loopback cable E6170-61619 on E6178B_8. Install Diagnostic Cable (E6170-61618) on appropriate HP connector.
- Setup DMM to perform 2W resistance measurement.
- Measure LC8CH_8 load card loopback path resistance from
  CH1-CH2 via Positronic pin5 and pin11 (ABUS1 & ABUS3)
  CH1-CH2 via Positronic pin6 and pin12 (ABUS2 & ABUS4)
  CH1-CH3 via Positronic pin5 and pin17 (ABUS1 & ABUS3)
  CH1-CH3 via Positronic pin6 and pin18 (ABUS2 & ABUS4)
  CH1-CH4 via Positronic pin5 and pin3 (ABUS1 & ABUS3)
  CH1-CH4 via Positronic pin6 and pin4 (ABUS2 & ABUS4)
  CH1-CH5 via Positronic pin5 and pin9 (ABUS1 & ABUS3)
  CH1-CH5 via Positronic pin6 and pin10 (ABUS2 & ABUS4)
  CH1-CH6 via Positronic pin5 and pin15 (ABUS1 & ABUS3)
  CH1-CH6 via Positronic pin6 and pin16 (ABUS2 & ABUS4)
  CH1-CH7 via Positronic pin5 and pin1 (ABUS1 & ABUS3)
  CH1-CH7 via Positronic pin6 and pin2 (ABUS2 & ABUS4)
  CH1-CH8 via Positronic pin5 and pin7 (ABUS1 & ABUS3)
  CH1-CH8 via Positronic pin6 and pin8 (ABUS2 & ABUS4)

Clean Up Information

- Display instruction to remove all Short from PWR1 and PWR2 of all E6178B load cards.

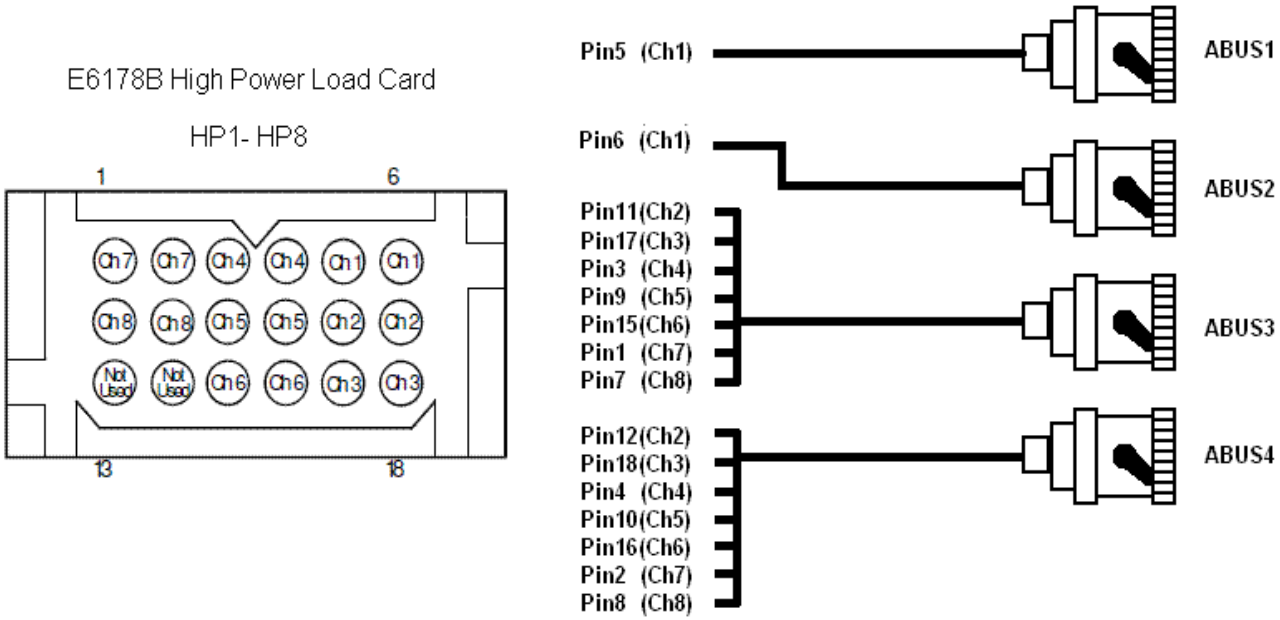


Figure 4-20 E6178B 8 Channel High Power Load Card Test

CEDGN_N9377A_LoadCard.tpa (16 Channel Load Card CEDGN Test Flow)

The testsplan supports testing of eight N9377A Load Cards. User is required to set the variables to reflect the system under test.

1 = present, 0 = not present

bLC16CH_1 = 1st N9377A
bLC16CH_2 = 2nd N9377A
bLC16CH_3 = 3rd N9377A
bLC16CH_4 = 4th N9377A
bLC16CH_5 = 5th N9377A
bLC16CH_6 = 6th N9377A
bLC16CH_7 = 7th N9377A
bLC16CH_8 = 8th N9377A

Device that user sets as not present will not be tested. The test starts by performing:

Not Acceptable Combination Checking

- Checks user settings for any not acceptable combination. Stops test and provide error message if not acceptable selection is found.

N9377A 16 Channel Load Card LC16CH_1 Tests

- Display instruction to Install load module E2240-67012 on LC16CH_1 Load Card.
- For LC16CH_1 on TC1, display instruction to install CEDGN Board #4 on TC1 and Cable E6170-61607 from SLU Utility Connector to J2 of Board #4.
- For LC16CH_1 on other TC, display instruction to install CEDGN Board #1 on TC1 and CEDGN Board #4 on appropriate TC. Install Cable E6170-61607 from SLU Utility Connector to J2 of Board #4. Install Cable E6170-61607 from J1 of Board #1 to J1 of Board #4.
- Setup DMM to perform 2W resistance measurement.
- Measure LC16CH_1 load card loopback path resistance from CH1-CH2 via Loadx.1 until CH7-CH8 via Loadx.1 using Row1 and Row8
  CH9-CH10 via Loadx.1 until CH15-CH16 via Loadx.1 using Row2 and Row7
- Measure LC16CH_1 load card sense resistor path:
  CH1 Current Sense until CH16 Current Sense via Row25 and Row26.

N9377A 16 Channel Load Card LC16CH_2 Tests

- Display instruction to Install load module E2240-67012 on LC16CH_2 Load Card.
- Display instruction to install CEDGN Board #1 on TC1 and CEDGN Board #4 on appropriate TC. Install Cable E6170-61607 from SLU Utility Connector to J2 of Board #4. Install Cable E6170-61607 from J1 of Board #1 to J1 of Board #4.
- Setup DMM to perform 2W resistance measurement.
- Measure LC16CH_2 load card loopback path resistance from CH1-CH2 via Loadx.1 until CH7-CH8 via Loadx.1 using Row1 and Row8
  CH9-CH10 via Loadx.1 until CH15-CH16 via Loadx.1 using Row2 and Row7
- Measure LC16CH_2 load card sense resistor path:
  CH1 Current Sense until CH16 Current Sense via Row25 and Row26.

N9377A 16 Channel Load Card LC16CH_3 Tests

- Display instruction to Install load module E2240-67012 on LC16CH_3 Load Card.
- Display instruction to install CEDGN Board #1 on TC1 and CEDGN Board #4 on appropriate TC. Install Cable E6170-61607 from SLU Utility Connector to J2 of Board #4. Install Cable E6170-61607 from J1 of Board #1 to J1 of Board #4.
- Setup DMM to perform 2W resistance measurement.
- Measure LC16CH_3 load card loopback path resistance from CH1-CH2 via Loadx.1 until CH7-CH8 via Loadx.1 using Row1 and Row8
  CH9-CH10 via Loadx.1 until CH15-CH16 via Loadx.1 using Row2 and Row7
- Measure LC16CH_3 load card sense resistor path:
  CH1 Current Sense until CH16 Current Sense via Row25 and Row26.

N9377A 16 Channel Load Card LC16CH_4 Tests

- Display instruction to Install load module E2240-67012 on LC16CH_4 Load Card.
- Display instruction to install CEDGN Board #1 on TC1 and CEDGN Board #4 on appropriate TC. Install Cable E6170-61607 from SLU Utility Connector to J2 of Board #4. Install Cable E6170-61607 from J1 of Board #1 to J1 of Board #4.
- Setup DMM to perform 2W resistance measurement.
- Measure LC16CH_4 load card loopback path resistance from CH1-CH2 via Loadx.1 until CH7-CH8 via Loadx.1 using Row1 and Row8
  CH9-CH10 via Loadx.1 until CH15-CH16 via Loadx.1 using Row2 and Row7
- Measure LC16CH_4 load card sense resistor path:
  CH1 Current Sense until CH16 Current Sense via Row25 and Row26.

N9377A 16 Channel Load Card LC16CH_5 Tests

- Display instruction to Install load module E2240-67012 on LC16CH_5 Load Card.
- Display instruction to install CEDGN Board #1 on TC1 and CEDGN Board #4 on appropriate TC. Install Cable E6170-61607 from SLU Utility Connector to J2 of Board #4. Install Cable E6170-61607 from J1 of Board #1 to J1 of Board #4.
- Setup DMM to perform 2W resistance measurement.
- Measure LC16CH_5 load card loopback path resistance from CH1-CH2 via Loadx.1 until CH7-CH8 via Loadx.1 using Row1 and Row8
  CH9-CH10 via Loadx.1 until CH15-CH16 via Loadx.1 using Row2 and Row7
- Measure LC16CH_5 load card sense resistor path:
  CH1 Current Sense until CH16 Current Sense via Row25 and Row26.

N9377A 16 Channel Load Card LC16CH_6 Tests

- Display instruction to Install load module E2240-67012 on LC16CH_6 Load Card.
- Display instruction to install CEDGN Board #1 on TC1 and CEDGN Board #4 on appropriate TC. Install Cable E6170-61607 from SLU Utility Connector to J2 of Board #4. Install Cable E6170-61607 from J1 of Board #1 to J1 of Board #4.
- Setup DMM to perform 2W resistance measurement.
- Measure LC16CH_6 load card loopback path resistance from CH1-CH2 via Loadx.1 until CH7-CH8 via Loadx.1 using Row1 and Row8
  CH9-CH10 via Loadx.1 until CH15-CH16 via Loadx.1 using Row2 and Row7
- Measure LC16CH_6 load card sense resistor path:
  CH1 Current Sense until CH16 Current Sense via Row25 and Row26.

N9377A 16 Channel Load Card LC16CH_7 Tests

- Display instruction to Install load module E2240-67012 on LC16CH_7 Load Card.
- Display instruction to install CEDGN Board #1 on TC1 and CEDGN Board #4 on appropriate TC. Install Cable E6170-61607 from SLU Utility Connector to J2 of Board #4. Install Cable E6170-61607 from J1 of Board #1 to J1 of Board #4.
- Setup DMM to perform 2W resistance measurement.
- Measure LC16CH_7 load card loopback path resistance from CH1-CH2 via Loadx.1 until CH7-CH8 via Loadx.1 using Row1 and Row8
  CH9-CH10 via Loadx.1 until CH15-CH16 via Loadx.1 using Row2 and Row7
- Measure LC16CH_7 load card sense resistor path:
  CH1 Current Sense until CH16 Current Sense via Row25 and Row26.

N9377A 16 Channel Load Card LC16CH_8 Tests

- Display instruction to Install load module E2240-67012 on LC16CH_8 Load Card.
- Display instruction to install CEDGN Board #1 on TC1 and CEDGN Board #4 on appropriate TC. Install Cable E6170-61607 from SLU Utility Connector to J2 of Board #4. Install Cable E6170-61607 from J1 of Board #1 to J1 of Board #4.
- Setup DMM to perform 2W resistance measurement.
- Measure LC16CH_8 load card loopback path resistance from CH1-CH2 via Loadx.1 until CH7-CH8 via Loadx.1 using Row1 and Row8
  CH9-CH10 via Loadx.1 until CH15-CH16 via Loadx.1 using Row2 and Row7
- Measure LC16CH_8 load card sense resistor path:
  CH1 Current Sense until CH16 Current Sense via Row25 and Row26.

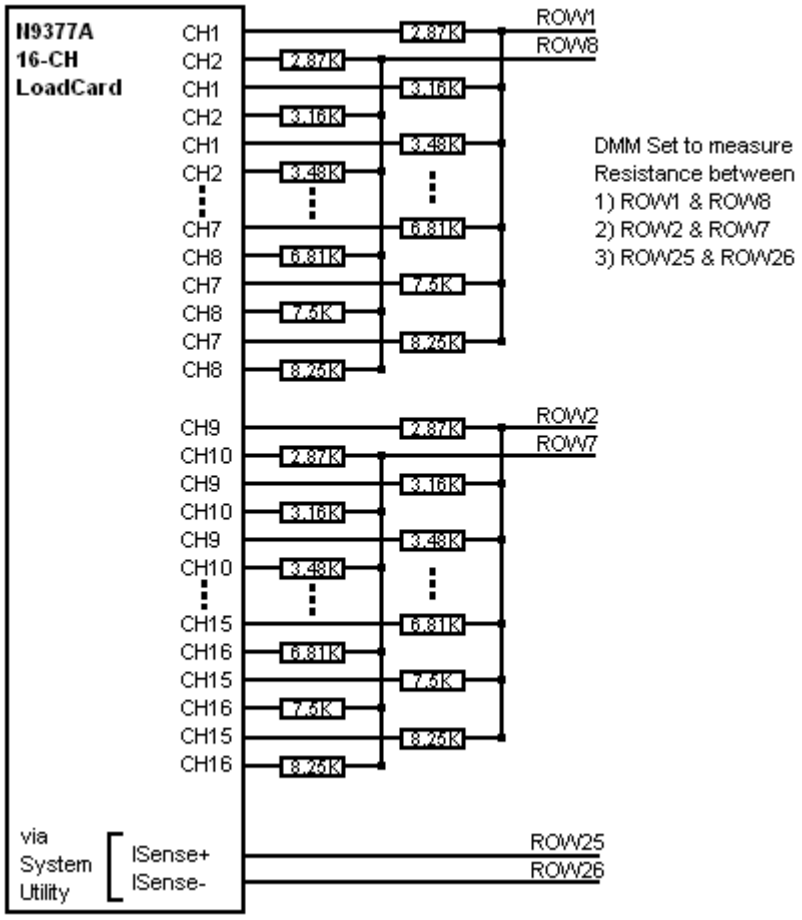


Figure 4-21 N9377A 16 Channel Load Card Test

CEDGN_N9379A_LoadCard.tpa (48 Channel Load Card CEDGN Test Flow)

The testsplan supports testing of four N9379A Load Cards. User is required to set the variables to reflect the system under test.

1 = present, 0 = not present

bLC48CH_1 = 1st N9379A
bLC48CH_2 = 2nd N9379A
bLC48CH_3 = 3rd N9379A
bLC48CH_4 = 4th N9379A

NOTE: All N9379A need to be installed with load modules E6170-66520

Device that user sets as not present will not be tested. The test starts by performing:

N9379A 48 Channel Load Card LC48CH_1 on TC1 (CH1 until CH24) Tests

- Display instruction to install CEDGN Board #4 on TC1.
- Setup DMM to perform 2W resistance measurement.
- Measure LC48CH_1 load card loopback path resistance from CH1-Com1 via Load1.1/Load1.2 until CH12-Com12 via Load12.1/Load12.2 using Row 1 and Row8.
  CH13-Com13 via Load13.1/Load13.2 until CH24-Com24 via Load24.1/Load24.2 using Row 2 and Row7.

N9379A 48 Channel Load Card LC48CH_1 on TC2 (CH25 until CH48) Tests

- Display instruction to install CEDGN Board #1 on TC1 and CEDGN Board #4 on appropriate TC2. Install Cable E6170-61607 from J1 of Board #1 to J1 of Board #4.
- Setup DMM to perform 2W resistance measurement.
- Measure LC48CH_1 load card loopback path resistance from CH25-Com25 via Load25.1/Load25.2 until CH36-Com36 via Load36.1/Load36.2 using Row 1 and Row8.
  CH37-Com37 via Load37.1/Load37.2 until CH48-Com48 via Load48.1/Load48.2 using Row 2 and Row7.

N9379A 48 Channel Load Card LC48CH_2 on TC3 (CH1 until CH24) Tests

- Display instruction to install CEDGN Board #1 on TC1 and CEDGN Board #4 on appropriate TC3. Install Cable E6170-61607 from J1 of Board #1 to J1 of Board #4
- Setup DMM to perform 2W resistance measurement
- Measure LC48CH_2 load card loopback path resistance from CH1-Com1 via Load1.1/Load1.2 until CH12-Com12 via Load12.1/Load12.2 using Row 1 and Row8.
  CH13-Com13 via Load13.1/Load13.2 until CH24-Com24 via Load24.1/Load24.2 using Row 2 and Row7.

N9379A 48 Channel Load Card LC48CH_2 on TC4 (CH25 until CH48) Tests

- Display instruction to install CEDGN Board #1 on TC1 and CEDGN Board #4 on appropriate TC4. Install Cable E6170-61607 from J1 of Board #1 to J1 of Board #4.
- Setup DMM to perform 2W resistance measurement.
- Measure LC48CH_2 load card loopback path resistance from CH25-Com25 via Load25.1/Load25.2 until CH36-Com36 via Load36.1/Load36.2 using Row 1 and Row8.
  CH37-Com37 via Load37.1/Load37.2 until CH48-Com48 via Load48.1/Load48.2 using Row 2 and Row7.

N9379A 48 Channel Load Card LC48CH_3 on TC5 (CH1 until CH24) Tests

- Display instruction to install CEDGN Board #1 on TC1 and CEDGN Board #4 on appropriate TC5. Install Cable E6170-61607 from J1 of Board #1 to J1 of Board #4
- Setup DMM to perform 2W resistance measurement.
- Measure LC48CH_3 load card loopback path resistance from CH1-Com1 via Load1.1/Load1.2 until CH12-Com12 via Load12.1/Load12.2 using Row 1 and Row8.
  CH13-Com13 via Load13.1/Load13.2 until CH24-Com24 via Load24.1/Load24.2 using Row 2 and Row7.

N9379A 48 Channel Load Card LC48CH_3 on TC6 (CH25 until CH48) Tests

- Display instruction to install CEDGN Board #1 on TC1 and CEDGN Board #4 on appropriate TC6. Install Cable E6170-61607 from J1 of Board #1 to J1 of Board #4.
- Setup DMM to perform 2W resistance measurement.
- Measure LC48CH_3 load card loopback path resistance from CH25-Com25 via Load25.1/Load25.2 until CH36-Com36 via Load36.1/Load36.2 using Row 1 and Row8.
  CH37-Com37 via Load37.1/Load37.2 until CH48-Com48 via Load48.1/Load48.2 using Row 2 and Row7.

N9379A 48 Channel Load Card LC48CH_4 on TC7 (CH1 until CH24) Tests

- Display instruction to install CEDGN Board #1 on TC1 and CEDGN Board #4 on appropriate TC7. Install Cable E6170-61607 from J1 of Board #1 to J1 of Board #4
- Setup DMM to perform 2W resistance measurement.
- Measure LC48CH_4 load card loopback path resistance from CH1-Com1 via Load1.1/Load1.2 until CH12-Com12 via Load12.1/Load12.2 using Row 1 and Row8.
  CH13-Com13 via Load13.1/Load13.2 until CH24-Com24 via Load24.1/Load24.2 using Row 2 and Row7.

N9379A 48 Channel Load Card LC48CH_4 on TC8 (CH25 until CH48) Tests

- Display instruction to install CEDGN Board #1 on TC1 and CEDGN Board #4 on appropriate TC8. Install Cable E6170-61607 from J1 of Board #1 to J1 of Board #4.
- Setup DMM to perform 2W resistance measurement.
- Measure LC48CH_4 load card loopback path resistance from CH25-Com25 via Load25.1/Load25.2 until CH36-Com36 via Load36.1/Load36.2 using Row 1 and Row8.
  CH37-Com37 via Load37.1/Load37.2 until CH48-Com48 via Load48.1/Load48.2 using Row 2 and Row7.

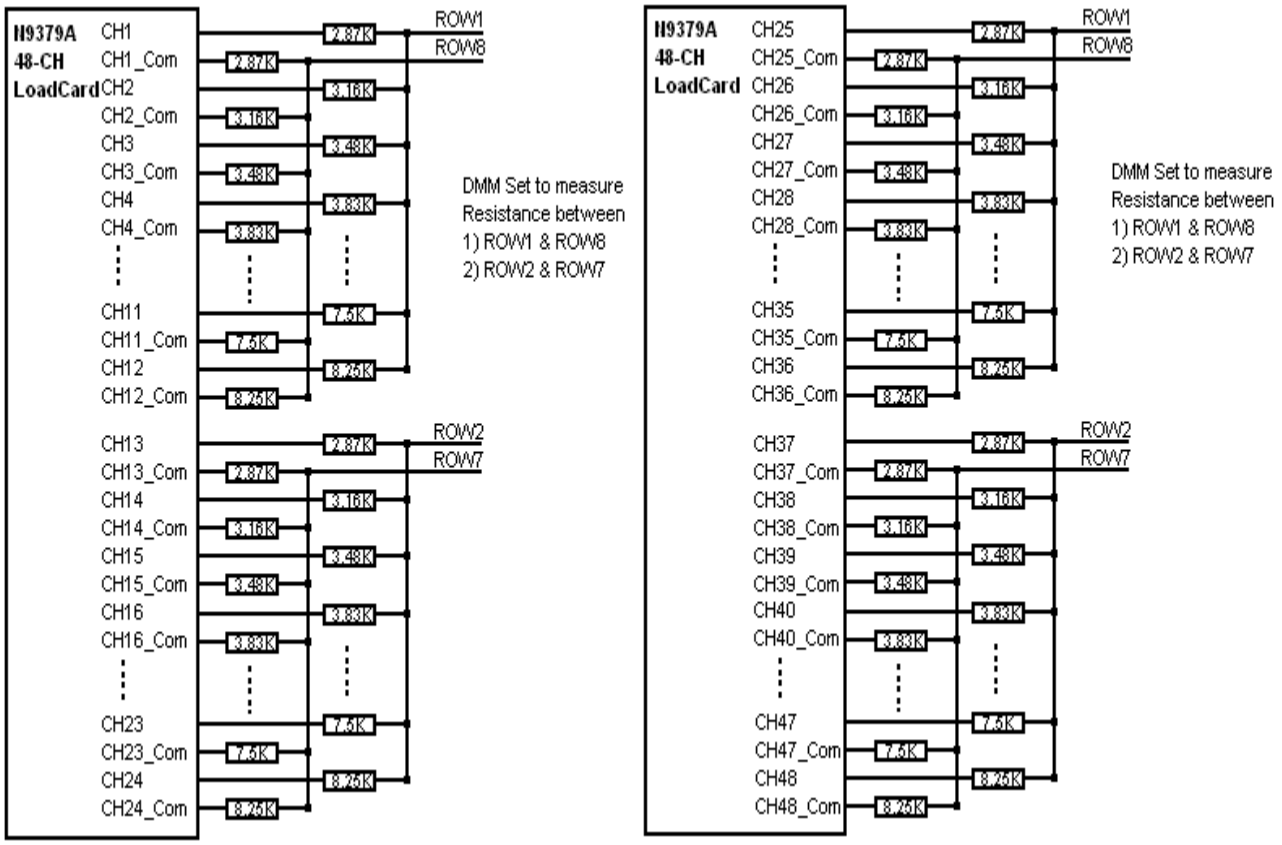


Figure 4-22 N9379A 48 Channel Load Card Test

CEDGN_E6198B_Utility.tpa (Switch Load Unit Utility CEDGN Test Flow)

The testsplan performs testing on the SLU Utility Connector at the Express Connect front panel.

SLU Utility Setup Information

- Display instruction to install CEDGN Board #1 on TC1. Install Cable E6170-61607 on SLU Utility Connector to J2 of Board #1.

SLU Utility System_Gnd Tests

- Setup DMM to measure voltage.
- Measure for 12V using fixed +12V reference at pin49 of SLU Utility Connector and changing System_Gnd. Covers System_Gnd at pin1, pin2, pin11, pin12, pin55, pin56, pin57, pin58, pin62 and pin64.

SLU Utility +12Vdc_Supply Tests

- Setup DMM to measure voltage.
- Measure for 12V using fixed System_Gnd at pin1 of SLU Utility Connector and changing +12Vdc_Supply. Covers +12Vdc_Supply at pin49, pin50, pin51 and pin52.

SLU Utility -12Vdc_Supply Tests

- Setup DMM to measure voltage.
- Measure for -12V between System_Gnd at pin1 and -12Vdc_Supply at pin54 of SLU Utility Connector.

SLU Utility DAC1 Tests

- Setup DMM to measure voltage.
- Measure for DAC1 output voltage at -16V, +16V and 0V.

SLU Utility DAC2 Tests

- Setup DMM to measure voltage.
- Measure for DAC2 output voltage at -16V, +16V and 0V.

SLU Utility FixtureID to OpenDrainOut Tests

- Uses 8bit OpenDrainOut as output and 8bit FixtureID as input.
- Tests OpenDrainOut and FixtureID Write/Read function covering 8bit data pattern:
  10101010 (170)
  01010101 (85)
  11111111 (255)
  00000000 (0)

SLU Utility Digital In to Digital Out Tests

- Uses 8bit Digital Out as output and 8bit Digital In as input.
- Tests Digital Out and Digital In Write/Read function covering 8bit data pattern:
  10101010 (170)
  01010101 (85)
  11111111 (255)
  00000000 (0)

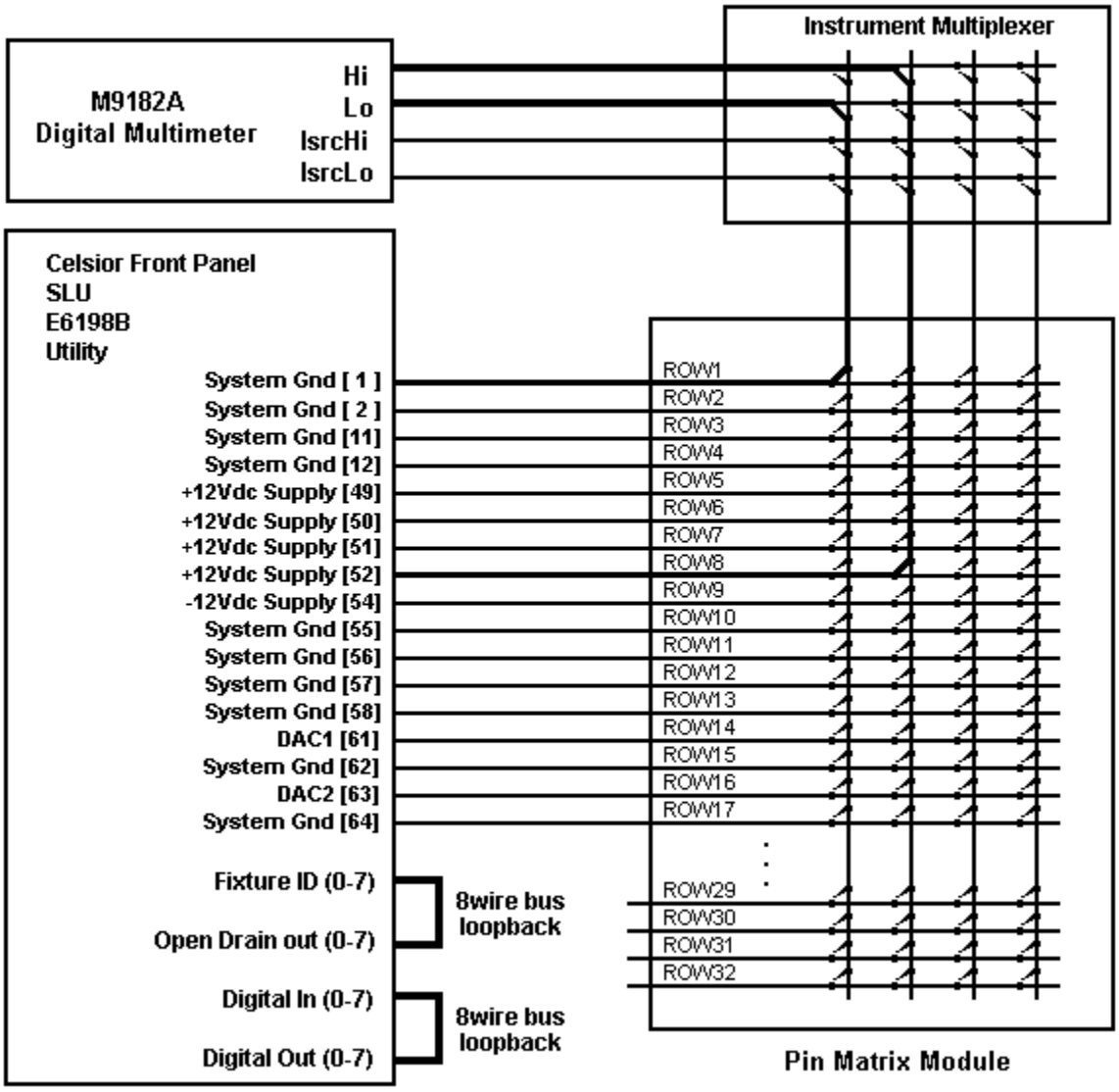


Figure 4-23 E6198B Switch Load Unit Utility Test

CEDGN_L4451A_LXIDAC.tpa (4 Channel LXI DAC CEDGN Test Flow)

The testsplan supports testing of two L4451A DAC.

User is required to set the variables to reflect the system under test.

1 = present, 0 = not present

bLXIDAC1 = 1st L4451A
bLXIDAC2 = 2nd L4451A

Device that user sets as not present will not be tested. The test starts by performing:

Not Acceptable Combination Checking

- Checks user settings for any not acceptable combination. Stops test and provide error message if not acceptable selection is found.

L4451A LXI DAC1 Tests

- Display instruction to install CEDGN Board #1 on TC1 and CEDGN Board #3 on appropriate TC. Install Cable E6170-61607 from J1 of Board #1 to J1 of Board #3.
- Setup DMM to perform voltage measurement.
- Measure DAC1 output for:
  CH1 with sense via Row9, Row10 and Row11, Row12
  CH1 without sense via Row9 and Row11
  CH2 with sense via Row13, Row14 and Row15, Row16
  CH2 without sense via Row13 and Row15
  CH3 with sense via Row17, Row18 and Row19, Row20
  CH3 without sense via Row17 and Row19
  CH4 with sense via Row21, Row22 and Row23, Row24
  CH4 without sense via Row21 and Row23
- Setup LXI DAC1 output 3V on CH1 when External Trigger is detected.
- Use SLU internal DAC1 to generate a simulated trigger to LXI DAC1.
- Measure for 3V at LXI DAC1 CH1 output for trigger response.

L4451A LXI DAC2 Tests

- Display instruction to install CEDGN Board #1 on TC1 and CEDGN Board #3 on appropriate TC. Install Cable E6170-61607 from J1 of Board #1 to J1 of Board #3.
- Setup DMM to perform voltage measurement.
- Measure DAC2 output for:
  CH1 with sense via Row9, Row10 and Row11, Row12
  CH1 without sense via Row9 and Row11
  CH2 with sense via Row13, Row14 and Row15, Row16
  CH2 without sense via Row13 and Row15
  CH3 with sense via Row17, Row18 and Row19, Row20
  CH3 without sense via Row17 and Row19
  CH4 with sense via Row21, Row22 and Row23, Row24
  CH4 without sense via Row21 and Row23
- Setup LXI DAC2 output 3V on CH1 when External Trigger is detected.
- Use SLU internal DAC1 to generate a simulated trigger pulse to LXI DAC2.
- Measure for 3V at LXI DAC2 CH1 output for trigger response.

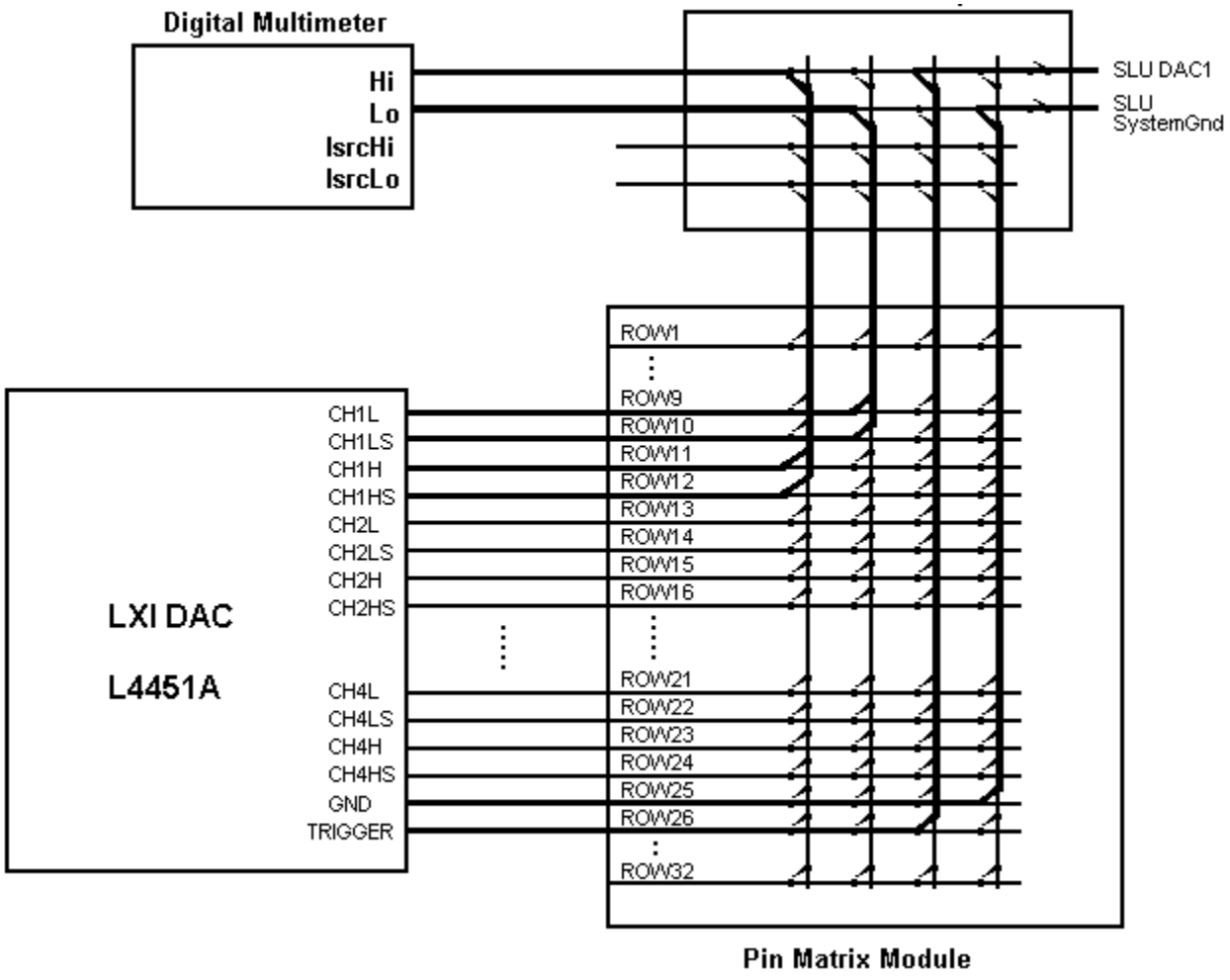


Figure 4-24 L4451A LXI DAC Test

CEDGN_M9185A_DAC.tpa (8/16 Channel PXI DAC CEDGN Test Flow)

The testsplan is for testing of M9185A 8/16 Channel DAC. It supports two 16 Channel DAC or three 8 Channel DAC or one 16 Channel and one 8 Channel DAC.

User is required to set the variables to reflect the system under test.

1 = present, 0 = not present

bDAC16_1 = 1st 16 Channel M9185A
bDAC16_2 = 2nd 16 Channel M9185A
bDAC8_1 = 1st 8 Channel M9185A
bDAC8_2 = 2nd 8 Channel M9185A
bDAC8_2 = 3rd 8 Channel M9185A

Device that user sets as not present will not be tested. The test starts by performing:

Not Acceptable Combination Checking

- Checks user settings for any not acceptable combination. Stops test and provide error message if not acceptable selection is found.

M9185A 16 Channel PXI DAC1 (CH1-CH8) on TC1 Tests

- Display instruction to install CEDGN Board #2 on TC1 and toggle S1 and S2 on Board #2 to DOWN position.
- Setup DMM to perform voltage measurement.
- Measure DAC16_1 output for (-16V, +16V and 0V) on channel:
  CH1 with/without sense
  CH2 with/without sense
  CH3 with/without sense
  CH4 with/without sense
  CH5 with/without sense
  CH6 with/without sense
  CH7 with/without sense
  CH8 with/without sense
- Display instruction to toggle S1 and S2 on Board #2 to UP position.
- Setup PXI DAC16_1 to output 16V on CH8 when External Trigger is detected.
- Use SLU internal DAC1 to generate a simulated trigger to PXI DAC16_1.
- Measure for 16V at PXI DAC16_1 CH8 output for trigger response.

M9185A 16 Channel PXI DAC1 (CH9-CH16) on TC3 Tests

- Display instruction to install CEDGN Board #1 on TC1. Install CEDGN Board #2 on TC3 and toggle S1 and S2 on Board #2 to DOWN position. Install Cable E6170-61607 on J1 of Board #1 to J1 of Board #2.
- Setup DMM to perform voltage measurement.
- Measure DAC16_1 output for (-16V, +16V and 0V) on channel:
  CH9 with/without sense
  CH10 with/without sense
  CH11 with/without sense
  CH12 with/without sense
  CH13 with/without sense
  CH14 with/without sense
  CH15 with/without sense
  CH16 with/without sense

M9185A 16 Channel PXI DAC2 (CH1-CH8) on TC5 Tests

- Display instruction to install CEDGN Board #1 on TC1. Install CEDGN Board #2 on TC5 and toggle S1 and S2 on Board #2 to DOWN position. Install Cable E6170-61607 on J1 of Board #1 to J1 of Board #2.
- Setup DMM to perform voltage measurement.
- Measure DAC16_2 output for (-16V, +16V and 0V) on channel:

CH1 with/without sense
CH2 with/without sense
CH3 with/without sense
CH4 with/without sense
CH5 with/without sense
CH6 with/without sense
CH7 with/without sense
CH8 with/without sense

- Display instruction to toggle S1 and S2 on Board #2 to UP position.
- Setup PXI DAC16_2 to output 16V on CH8 when External Trigger is detected.
- Use SLU internal DAC1 to generate a simulated trigger to PXI DAC16_2.
- Measure for 16V at PXI DAC16_2 CH8 output for trigger response.

M9185A 16 Channel PXI DAC2 (CH9-CH16) on TC7 Tests

- Display instruction to install CEDGN Board #1 on TC1. Install CEDGN Board #2 on TC7 and toggle S1 and S2 on Board #2 to DOWN position. Install Cable E6170-61607 on J1 of Board #1 to J1 of Board #2.
- Setup DMM to perform voltage measurement.
- Measure DAC16_2 output for (-16V, +16V and 0V) on channel:
  CH9 with/without sense
  CH10 with/without sense
  CH11 with/without sense
  CH12 with/without sense
  CH13 with/without sense
  CH14 with/without sense
  CH15 with/without sense
  CH16 with/without sense

M9185A 8 Channel PXI DAC1 (CH1-CH8) Tests

- For DAC8_1 on TC1, display instruction to install CEDGN Board #2 on TC1 and toggle S1 and S2 on Board #2 to DOWN position.
- For DAC8_1 on other TC, display instruction to install CEDGN Board #1 on TC1. Install CEDGN Board #2 on appropriate TC and toggle S1 and S2 on Board #2 to DOWN position. Install Cable E6170-61607 on J1 of Board #1 to J1 of Board #2.
- Setup DMM to perform voltage measurement.
- Measure DAC8_1 output for (-16V, +16V and 0V) on channel:
  CH1 with/without sense
  CH2 with/without sense
  CH3 with/without sense
  CH4 with/without sense

CH5 with/without sense
CH6 with/without sense
CH7 with/without sense
CH8 with/without sense

- Display instruction to toggle S1 and S2 on Board #2 to UP position.
- Setup PXI DAC8_1 to output 16V on CH8 when External Trigger is detected.
- Use SLU internal DAC1 to generate a simulated trigger to PXI DAC8_1.
- Measure for 16V at PXI DAC8_1 CH8 output for trigger response.

M9185A 8 Channel PXI DAC2 (CH1-CH8) Tests

- Display instruction to install CEDGN Board #1 on TC1. Install CEDGN Board #2 on appropriate TC and toggle S1 and S2 on Board #2 to DOWN position. Install Cable E6170-61607 on J1 of Board #1 to J1 of Board #2.
- Setup DMM to perform voltage measurement.
- Measure DAC8_2 output for (-16V, +16V and 0V) on channel:
  CH1 with/without sense
  CH2 with/without sense
  CH3 with/without sense
  CH4 with/without sense
  CH5 with/without sense
  CH6 with/without sense
  CH7 with/without sense
  CH8 with/without sense
- Display instruction to toggle S1 and S2 on Board #2 to UP position.
- Setup PXI DAC8_2 to output 16V on CH8 when External Trigger is detected.

- Use SLU internal DAC1 to generate a simulated trigger to PXI DAC8_2.
- Measure for 16V at PXI DAC8_2 CH8 output for trigger response.

M9185A 8 Channel PXI DAC3 (CH1-CH8) Tests

- Display instruction to install CEDGN Board #1 on TC1. Install CEDGN Board #2 on appropriate TC and toggle S1 and S2 on Board #2 to DOWN position. Install Cable E6170-61607 on J1 of Board #1 to J1 of Board #2.
- Setup DMM to perform voltage measurement.
- Measure DAC8_3 output for (-16V, +16V and 0V) on channel:
  CH1 with/without sense
  CH2 with/without sense
  CH3 with/without sense
  CH4 with/without sense
  CH5 with/without sense
  CH6 with/without sense
  CH7 with/without sense
  CH8 with/without sense
- Display instruction to toggle S1 and S2 on Board #2 to UP position.
- Setup PXI DAC8_3 to output 16V on CH8 when External Trigger is detected.
- Use SLU internal DAC1 to generate a simulated trigger to PXI DAC8_3.
- Measure for 16V at PXI DAC8_3 CH8 output for trigger response.

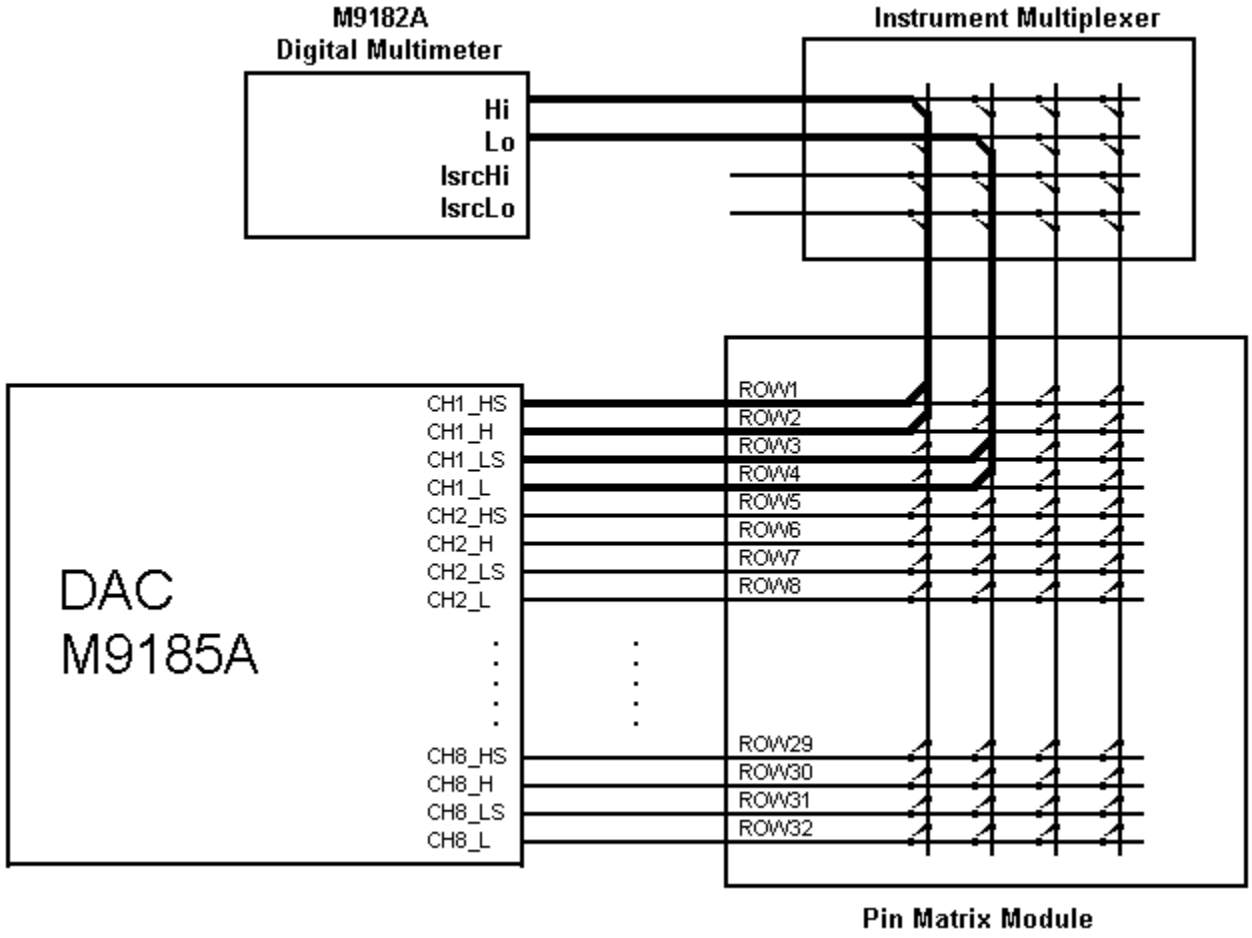


Figure 4-25 M9185A PXI DAC Output Test

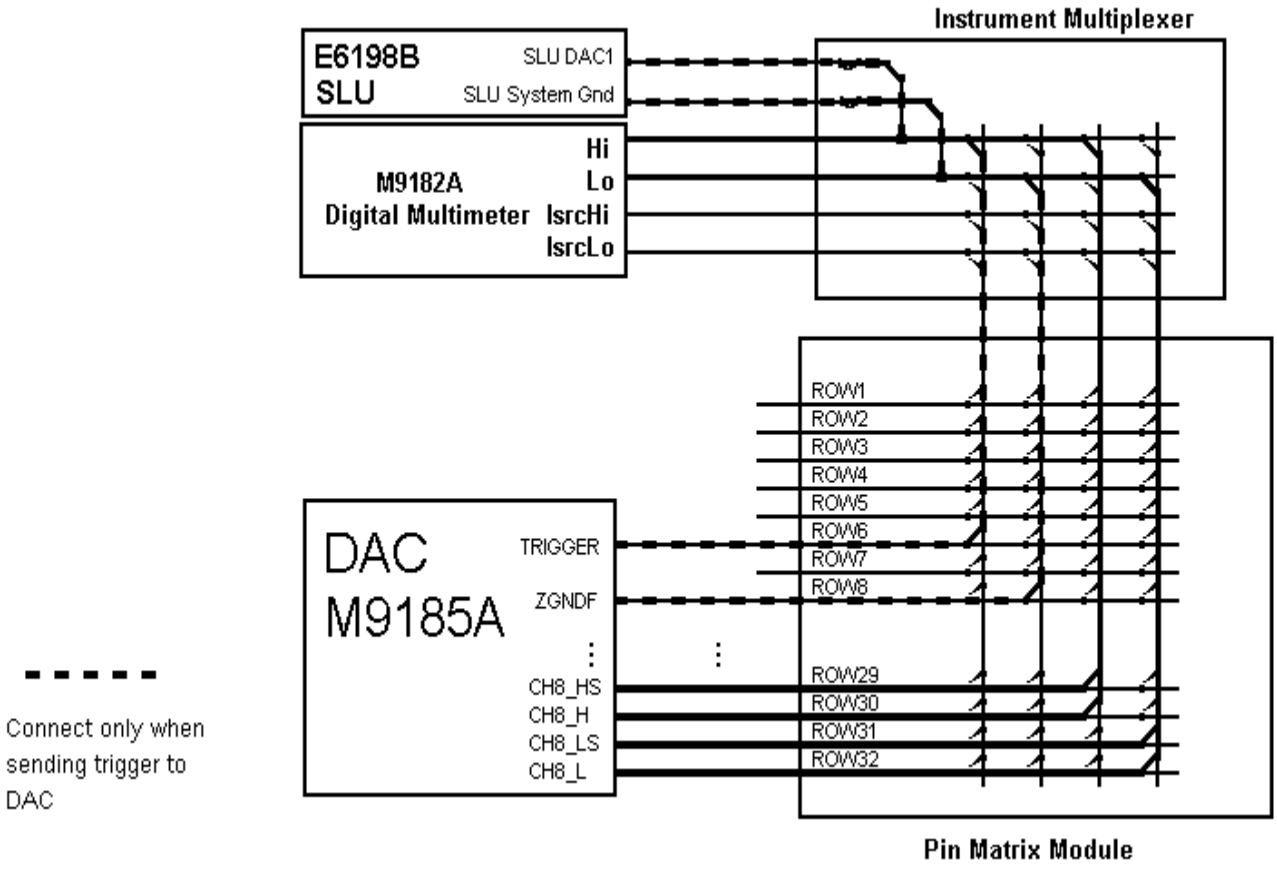


Figure 4-26 M9185A PXI DAC Trigger Test

CEDGN_M9186A_VI.tpa (VI Source CEDGN Test Flow)

The testsplan supports testing of two M9186A VI Source modules.

It is used to verify the connectivity of VI Source module Safety Interlock on the Express Connect TC connector. Test will abort with EXCEPTION ENCOUNTERED error if safety interlock is not installed.

User is required to set the variables to reflect the system under test.

1 = present, 0 = not present

bVI1 = 1st VI Source M9186A
bVI2 = 2nd VI Source M9186A

Device that user sets as not present will not be tested. The test starts by performing:

Not Acceptable Combination Checking

- Checks user settings for any not acceptable combination. Stops test and provide error message if not acceptable selection is found.

M9186A VI Source Module VI1 Tests

- Display instruction to install CEDGN Board #3 on appropriate TC.
- Setup DMM to perform voltage measurement covering:
  VI1 Low Voltage 0ohm Path
  VI1 Low Voltage 10ohm Path
  VI1 Low Voltage 100ohm Path
  VI1 Low Voltage 1kohm Path
  VI1 Low Voltage 10kohm Path
  VI1 High Voltage 0ohm Path
  VI1 High Voltage 100ohm Path
- Setup DMM to perform current measurement covering:
  VI1 Low Current
  VI1 High Current

M9186A VI Source Module VI2 Tests

- Display instruction to install CEDGN Board #3 on appropriate TC.
- Setup DMM to perform voltage measurement covering:
  VI2 Low Voltage 0ohm Path
  VI2 Low Voltage 10ohm Path
  VI2 Low Voltage 100ohm Path
  VI2 Low Voltage 1kohm Path
  VI2 Low Voltage 10kohm Path
  VI2 High Voltage 0ohm Path
  VI2 High Voltage 100ohm Path
- Setup DMM to perform current measurement covering:
  VI2 Low Current
  VI2 High Current

CEDGN_M9187A_DIO.tpa (DIO CEDGN Test Flow)

The testsplan supports testing of two M9187A DIO modules. User is required to set the variables to reflect the system under test.

1 = present, 0 = not present

bDIO1 = 1st M9187A DIO
bDIO2 = 2nd M9187A DIO

Device that user sets as not present will not be tested. The test starts by performing:

Not Acceptable Combination Checking

- Checks user settings for any not acceptable combination. Stops test and provide error message if not acceptable selection is found.

M9187A DIO1 on TC2 (Channel 1-16) Tests

- Setup SLU internal DAC1 to output 5V for use on DIO1 Vext.
- Display instruction to install CEDGN Board #1 on TC1 and CEDGN Board #3 on TC2. Install Cable E6170-61607 on J1 of Board #1 to J1 of Board #3.
- Test connectivity of Vext and FPGND(P1), FPGND(P2), FPGND(P3), FPGND(P4), FPGND(V1), FPGND(V2), FPGND(V3) using DIO1 output Channel 1 to generate a high and low state output and using DIO1 input Channel 1 to detect the high and low state.
- Test DIO1 output Channel 1-16 by output high and low state for all channels. Test DIO1 input Channel 1-16 by detecting the high and low state generated by the output channels.

M9187A DIO1 on TC4 (Channel 17-32) Tests

- Setup SLU internal DAC1 to output 5V for use on DIO1 Vext.
- Display instruction to install CEDGN Board #1 on TC1 and CEDGN Board #3 on TC4. Install Cable E6170-61607 on J1 of Board #1 to J1 of Board #3.
- Test connectivity of Vext and FPGND(P1), FPGND(P2), FPGND(P3), FPGND(P4), FPGND(V1), FPGND(V2), FPGND(V3) using DIO1 output Channel 17 to generate a high and low state output and using DIO1 input Channel 17 to detect the high and low state.
- Test DIO1 output Channel 17-32 by output high and low state for all channels. Test DIO1 input Channel 17-32 by detecting the high and low state generated by the output channels.

M9187A DIO2 on TC6 (Channel 1-16) Tests

- Setup SLU internal DAC1 to output 5V for use on DIO2 Vext.
- Display instruction to install CEDGN Board #1 on TC1 and CEDGN Board #3 on TC6. Install Cable E6170-61607 on J1 of Board #1 to J1 of Board #3.
- Test connectivity of Vext and FPGND(P1), FPGND(P2), FPGND(P3), FPGND(P4), FPGND(V1), FPGND(V2), FPGND(V3) using DIO2 output Channel 1 to generate a high and low state output and using DIO2 input Channel 1 to detect the high and low state.
- Test DIO2 output Channel 1-16 by output high and low state for all channels. Test DIO2 input Channel 1-16 by detecting the high and low state generated by the output channels.

M9187A DIO2 on TC8 (Channel 17-32) Tests

- Setup SLU internal DAC1 to output 5V for use on DIO2 Vext.
- Display instruction to install CEDGN Board #1 on TC1 and CEDGN Board #3 on TC8. Install Cable E6170-61607 on J1 of Board #1 to J1 of Board #3.
- Test connectivity of Vext and FPGND(P1), FPGND(P2), FPGND(P3), FPGND(P4), FPGND(V1), FPGND(V2), FPGND(V3) using DIO2 output Channel 17 to generate a high and low state output and using DIO2 input Channel 17 to detect the high and low state.
- Test DIO2 output Channel 17-32 by output high and low state for all channels. Test DIO2 input Channel 17-32 by detecting the high and low state generated by the output channels.

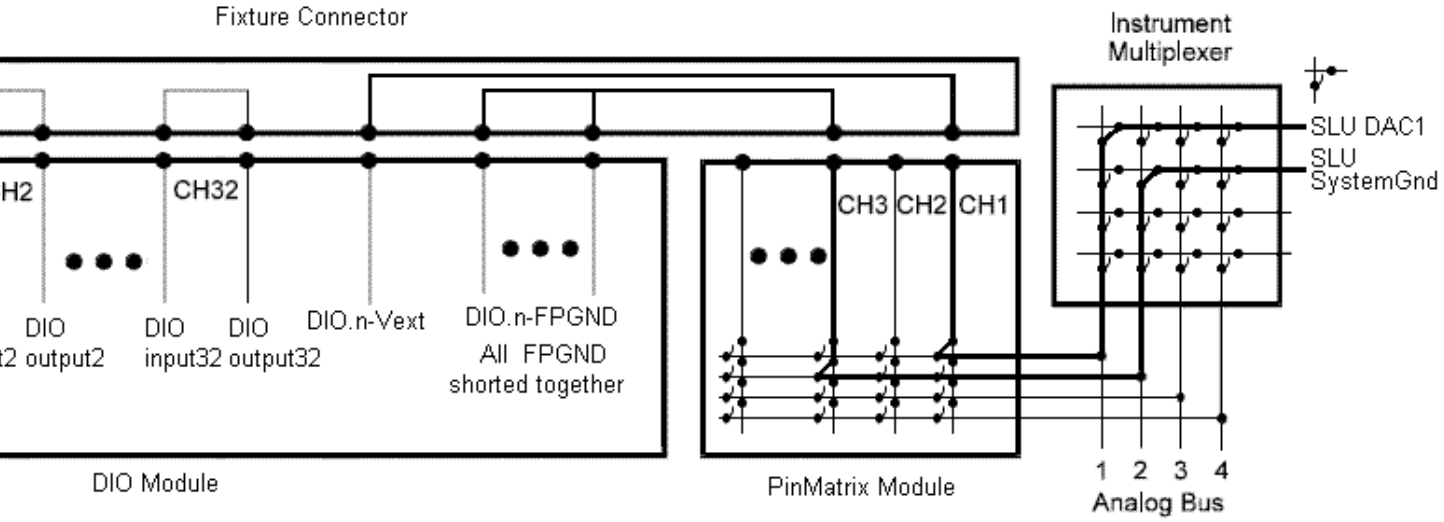


Figure 4-27 M9187A DIO Test

CEDGN_M9216A_DAQ.tpa (High Voltage Data Acquisition CEDGN Test Flow)

The testsplan supports testing of four M9216A DAQ.

User is required to set the variables to reflect the system under test.

1 = present, 0 = not present

bDAQ1 = 1st M9216A

bDAQ2 = 2nd M9216A

bDAQ3 = 3rd M9216A

bDAQ4 = 4th M9216A

Device that user sets as not present will not be tested. The test starts by performing:

Not Acceptable Combination Checking

- Checks user settings for any not acceptable combination. Stops test and provide error message if not acceptable selection is found.

M9216A DAQ1 Tests

- Display instruction to install CEDGN Board #1 on TC1 and CEDGN Board #5 on appropriate TC. OPEN all 16 actuators on switch S1 and S2 of Board #5. Install Cable E6170-61607 from J1 of Board #1 to J1 of Board #5.
- Setup SLU internal DAC1 to output 5V.
- Route 5V from DAC1 to individual DAQ channel and use DAQ to measure each channel.DAC1 EarthGnd is connected to DAQ ground via UUTCommon of PinMatrix.

  Test covers:
  DAQ1 1A (via Row1)
  DAQ1 1B (via Row2)
  DAQ1 1C (via Row3)
  DAQ1 1D (via Row4)
  DAQ1 2A (via Row5)
  DAQ1 2B (via Row6)
  DAQ1 2C (via Row7)
  DAQ1 2D (via Row8)
  DAQ1 3A (via Row9)
  DAQ1 3B (via Row10)
  DAQ1 3C (via Row11)
  DAQ1 3D (via Row12)
  DAQ1 4A (via Row13)
  DAQ1 4B (via Row14)
  DAQ1 4C (via Row15)
  DAQ1 4D (via Row16)
  DAQ1 5A (via Row17)
  DAQ1 5B (via Row18)
  DAQ1 5C (via Row19)
  DAQ1 5D (via Row20)
  DAQ1 6A (via Row21)
  DAQ1 6B (via Row22)
  DAQ1 6C (via Row23)
  DAQ1 6D (via Row24)
  DAQ1 7A (via Row25)

DAQ1 7B (via Row26)
DAQ1 7C (via Row27)
DAQ1 7D (via Row28)
DAQ1 8A (via Row29)
DAQ1 8B (via Row30)
DAQ1 8C (via Row31)
DAQ1 8D (via Row32)

M9216A DAQ2 Tests

- Display instruction to install CEDGN Board #1 on TC1 and CEDGN Board #5 on appropriate TC. OPEN all 16 actuators on switch S1 and S2 of Board #5. Install Cable E6170-61607 from J1 of Board #1 to J1 of Board #5.
- Setup SLU internal DAC1 to output 5V.
- Route 5V from DAC1 to individual DAQ channel and use DAQ to measure each channel.DAC1 EarthGnd is connected to DAQ ground via UUTCommon of PinMatrix.

  Test covers:
  DAQ2 1A (via Row1)
  DAQ2 1B (via Row2)
  DAQ2 1C (via Row3)
  DAQ2 1D (via Row4)
  DAQ2 2A (via Row5)
  DAQ2 2B (via Row6)
  DAQ2 2C (via Row7)
  DAQ2 2D (via Row8)
  DAQ2 3A (via Row9)
  DAQ2 3B (via Row10)
  DAQ2 3C (via Row11)
  DAQ2 3D (via Row12)
  DAQ2 4A (via Row13)
  DAQ2 4B (via Row14)
  DAQ2 4C (via Row15)
  DAQ2 4D (via Row16)
  DAQ2 5A (via Row17)
  DAQ2 5B (via Row18)
  DAQ2 5C (via Row19)
  DAQ2 5D (via Row20)
  DAQ2 6A (via Row21)
  DAQ2 6B (via Row22)
  DAQ2 6C (via Row23)
  DAQ2 6D (via Row24)
  DAQ2 7A (via Row25)
  DAQ2 7B (via Row26)
  DAQ2 7C (via Row27)
  DAQ2 7D (via Row28)

DAQ2 8A (via Row29)
DAQ2 8B (via Row30)
DAQ2 8C (via Row31)
DAQ2 8D (via Row32)

M9216A DAQ3 Tests

- Display instruction to install CEDGN Board #1 on TC1 and CEDGN Board #5 on appropriate TC. OPEN all 16 actuators on switch S1 and S2 of Board #5. Install Cable E6170-61607 from J1 of Board #1 to J1 of Board #5.
- Setup SLU internal DAC1 to output 5V.
- Route 5V from DAC1 to individual DAQ channel and use DAQ to measure each channel.DAC1 EarthGnd is connected to DAQ ground via UUTCommon of PinMatrix.

  Test covers:
  DAQ3 1A (via Row1)
  DAQ3 1B (via Row2)
  DAQ3 1C (via Row3)
  DAQ3 1D (via Row4)
  DAQ3 2A (via Row5)
  DAQ3 2B (via Row6)
  DAQ3 2C (via Row7)
  DAQ3 2D (via Row8)
  DAQ3 3A (via Row9)
  DAQ3 3B (via Row10)
  DAQ3 3C (via Row11)
  DAQ3 3D (via Row12)
  DAQ3 4A (via Row13)
  DAQ3 4B (via Row14)
  DAQ3 4C (via Row15)
  DAQ3 4D (via Row16)
  DAQ3 5A (via Row17)
  DAQ3 5B (via Row18)
  DAQ3 5C (via Row19)
  DAQ3 5D (via Row20)
  DAQ3 6A (via Row21)
  DAQ3 6B (via Row22)
  DAQ3 6C (via Row23)
  DAQ3 6D (via Row24)
  DAQ3 7A (via Row25)
  DAQ3 7B (via Row26)
  DAQ3 7C (via Row27)
  DAQ3 7D (via Row28)
  DAQ3 8A (via Row29)
  DAQ3 8B (via Row30)
  DAQ3 8C (via Row31)
  DAQ3 8D (via Row32)

M9216A DAQ4 Tests

- Display instruction to install CEDGN Board #1 on TC1 and CEDGN Board #5 on appropriate TC. OPEN all 16 actuators on switch S1 and S2 of Board #5. Install Cable E6170-61607 from J1 of Board #1 to J1 of Board #5.
- Setup SLU internal DAC1 to output 5V.
- Route 5V from DAC1 to individual DAQ channel and use DAQ to measure each channel.DAC1 EarthGnd is connected to DAQ ground via UUTCommon of PinMatrix.

  Test covers:
  DAQ4 1A (via Row1)
  DAQ4 1B (via Row2)
  DAQ4 1C (via Row3)
  DAQ4 1D (via Row4)
  DAQ4 2A (via Row5)
  DAQ4 2B (via Row6)
  DAQ4 2C (via Row7)
  DAQ4 2D (via Row8)
  DAQ4 3A (via Row9)
  DAQ4 3B (via Row10)
  DAQ4 3C (via Row11)
  DAQ4 3D (via Row12)
  DAQ4 4A (via Row13)
  DAQ4 4B (via Row14)
  DAQ4 4C (via Row15)
  DAQ4 4D (via Row16)
  DAQ4 5A (via Row17)
  DAQ4 5B (via Row18)
  DAQ4 5C (via Row19)
  DAQ4 5D (via Row20)
  DAQ4 6A (via Row21)
  DAQ4 6B (via Row22)
  DAQ4 6C (via Row23)
  DAQ4 6D (via Row24)
  DAQ4 7A (via Row25)
  DAQ4 7B (via Row26)
  DAQ4 7C (via Row27)
  DAQ4 7D (via Row28)
  DAQ4 8A (via Row29)
  DAQ4 8B (via Row30)
  DAQ4 8C (via Row31)
  DAQ4 8D (via Row32)

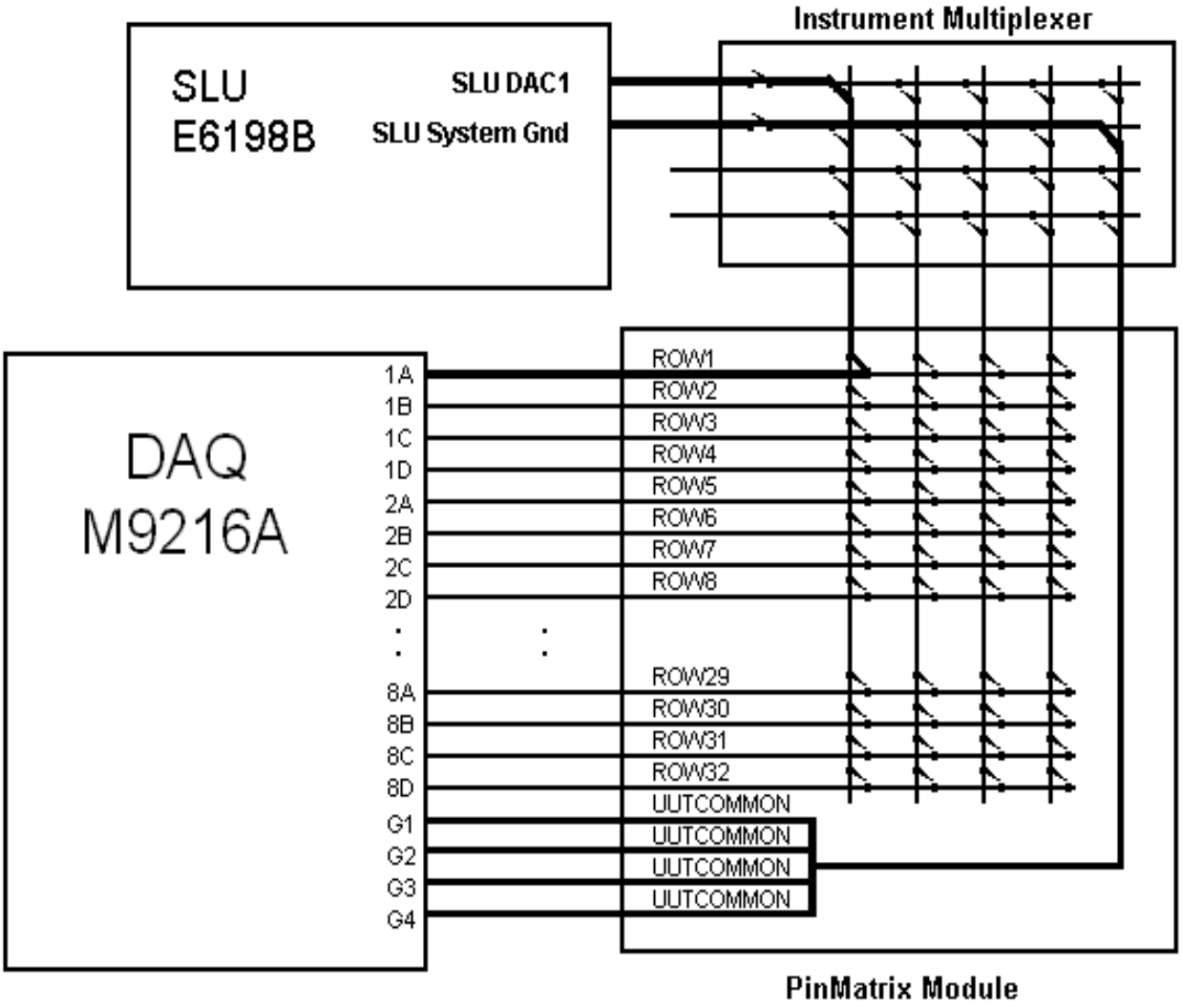


Figure 4-28 M9216A High Voltage Data Acquisition Test

CEDGN_RS232.tpa (RS232 Serial COM CEDGN Test Flow)

The testsplan supports testing of four RS232 COM ports. It is a loopback test where Tx and Rx of the COM port is connected together.

User is required to set the variables to reflect the system under test.

1 = present, 0 = not present

bCOM1 = 1st COM Port
bCOM2 = 2nd COM Port
bCOM3 = 3rd COM Port
bCOM4 = 4th COM Port

Device that user sets as not present will not be tested. The test starts by performing:

COM1 on TC1 Tests

- Display instruction to Install CEDGN Board #1 on TC1.
- Use COM1 to transmit characters “This is test com1”.
- Use COM1 to receive and compare to ensure the received characters matches the transmitted characters.

COM2 on TC3 Tests

- Display instruction to Install CEDGN Board #1 on TC3.
- Use COM2 to transmit characters “This is test com2”.
- Use COM2 to receive and compare to ensure the received characters matches the transmitted characters.

COM3 on TC5 Tests

- Display instruction to Install CEDGN Board #1 on TC5.
- Use COM3 to transmit characters “This is test com3”.
- Use COM3 to receive and compare to ensure the received characters matches the transmitted characters.

COM4 on TC7 Tests

- Display instruction to Install CEDGN Board #1 on TC7.
- Use COM4 to transmit characters “This is test com4”.
- Use COM4 to receive and compare to ensure the received characters matches the transmitted characters.

CEDGN_SoftingCAN.tpa (Softing CAN CEDGN Test Flow)

The testsplan supports testing of two Softing CAN cards. Each card has two CAN ports. User is required to set the variables to reflect the system under test.

1 = present, 0 = not present

bCAN1_1_AND_CAN1_2_TC1 = 1st Softing CAN card with CAN ports on TC1
bCAN2_1_TC3 = 2nd Softing CAN card with CAN port 1 on TC3
bCAN2_2_TC5 = 2nd Softing CAN card with CAN port 2 on TC5

Device that user sets as not present will not be tested. The test starts by performing:

CAN1_1 and CAN1_2 communication test

- Display instruction to Install CEDGN Board #1 on TC1.
- Use CAN1_1 to transmit to CAN1_2. Verify transmitted data matched received data.
- Use CAN1_2 to transmit to CAN1_1. Verify transmitted data matched received data.

CAN1_1 and CAN2_1 communication test

- Display instruction to Install CEDGN Board #1 on TC1 and CEDGN Board #2 on TC3. Install Cable E6170-61607 on J1 of Board #1 to J1 of Board #2.
- Use CAN1_1 to transmit to CAN2_1. Verify transmitted data matched received data.
- Use CAN2_1 to transmit to CAN1_1. Verify transmitted data matched received data.

CAN1_1 and CAN2_2 communication test

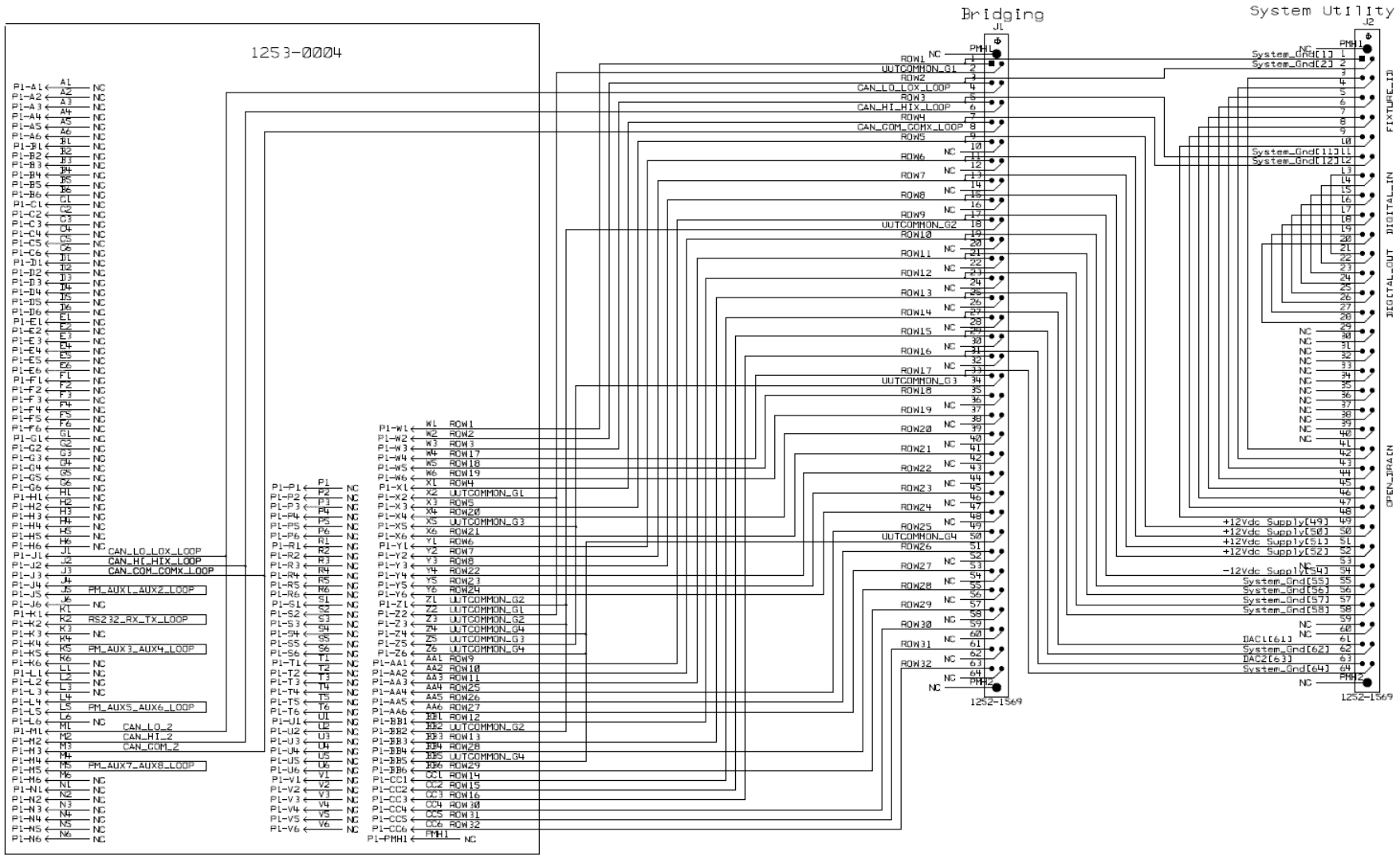
- Display instruction to Install CEDGN Board #1 on TC1 and CEDGN Board #2 on TC5. Install Cable E6170-61607 on J1 of Board #1 to J1 of Board #2.
- Use CAN1_1 to transmit to CAN2_2. Verify transmitted data matched received data.
- Use CAN2_2 to transmit to CAN1_1. Verify transmitted data matched received data.

A
Diagnostic Test Fixture Details

Celsior Test Fixture Schematics

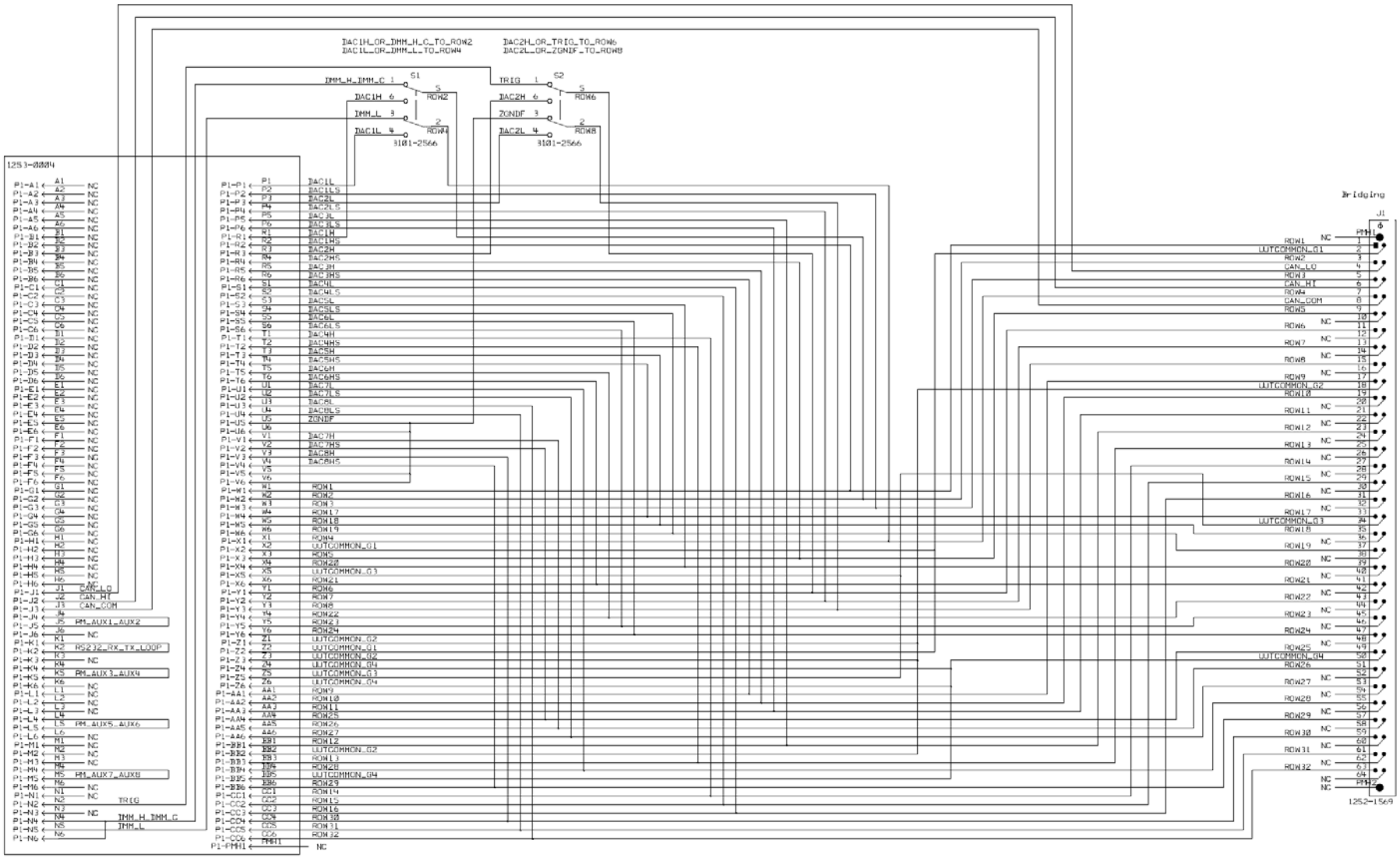
Schematic for U8970-66603 PCA-Diagnostic Number 1 (Board #1)

Figure A-1 U8970-66603 PCA-Diagnostic Number 1 (Board #1)



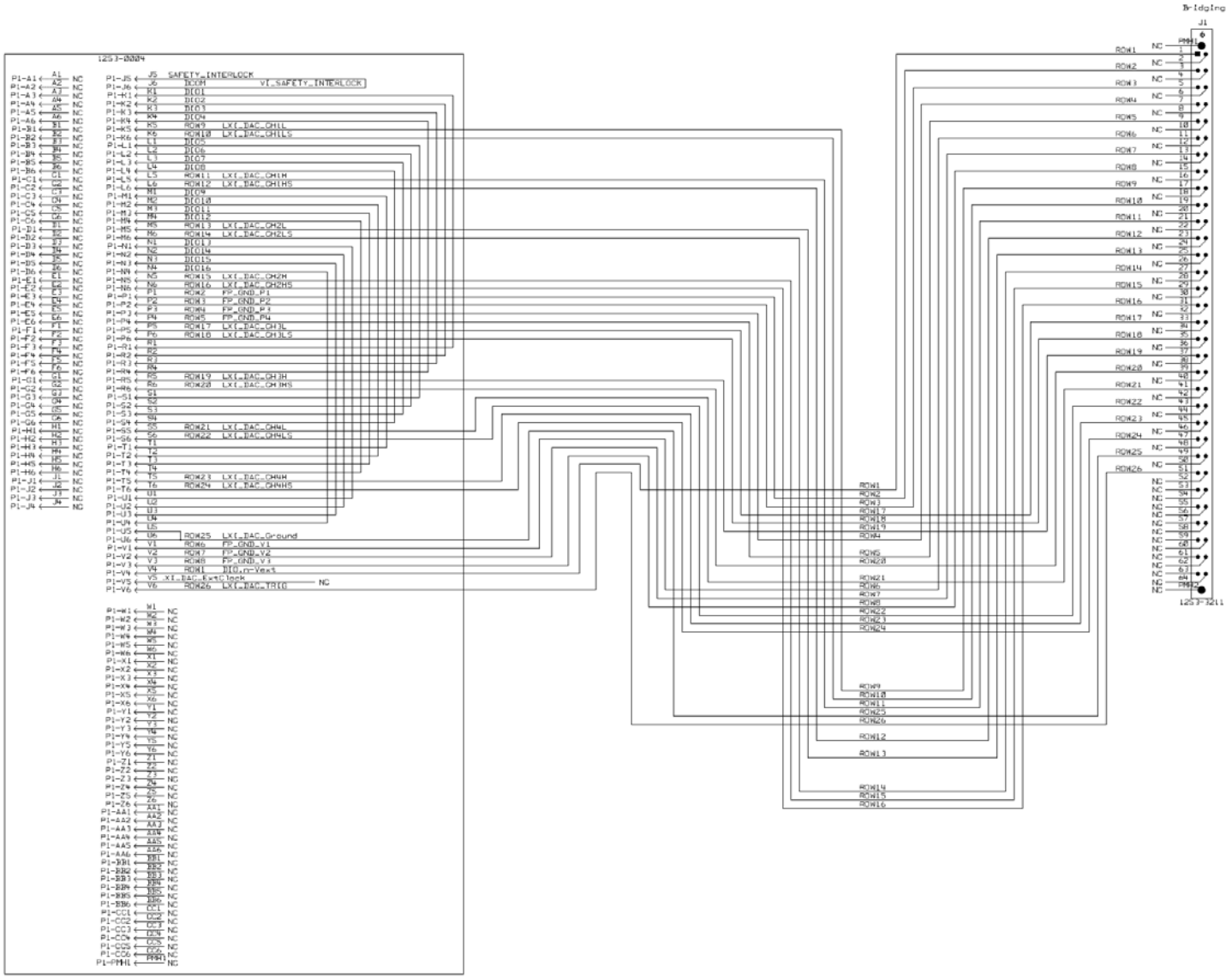
Schematic for U8970-66604 PCA-Diagnostic Number 2 (Board #2)

Figure A-2 U8970-66604 PCA-Diagnostic Number 2 (Board #2)



Schematic for U8970-66605 PCA-Diagnostic Number 3 (Board #3)

Figure A-3 U8970-66605 PCA-Diagnostic Number 3 (Board #3)



Schematic for U8970-66606 PCA-Diagnostic Number 4 (Board #4)

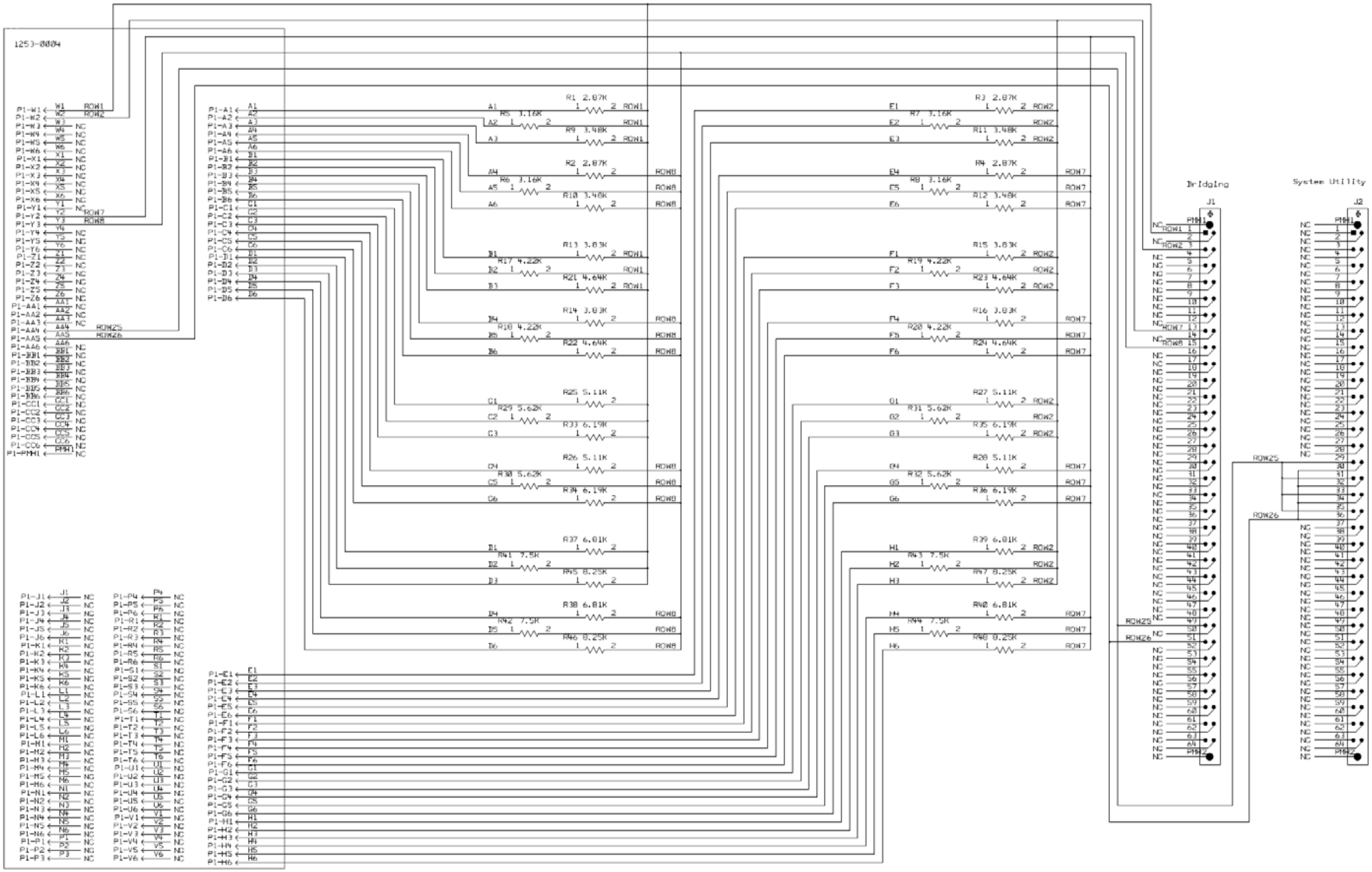


Figure A-4 U8970-66606 PCA-Diagnostic Number 4 (Board #4)

Schematic for U8970-66607 PCA-Diagnostic Number 5 (Board #5)

Figure A-5 U8970-66607 PCA-Diagnostic Number 5 (Board #5)

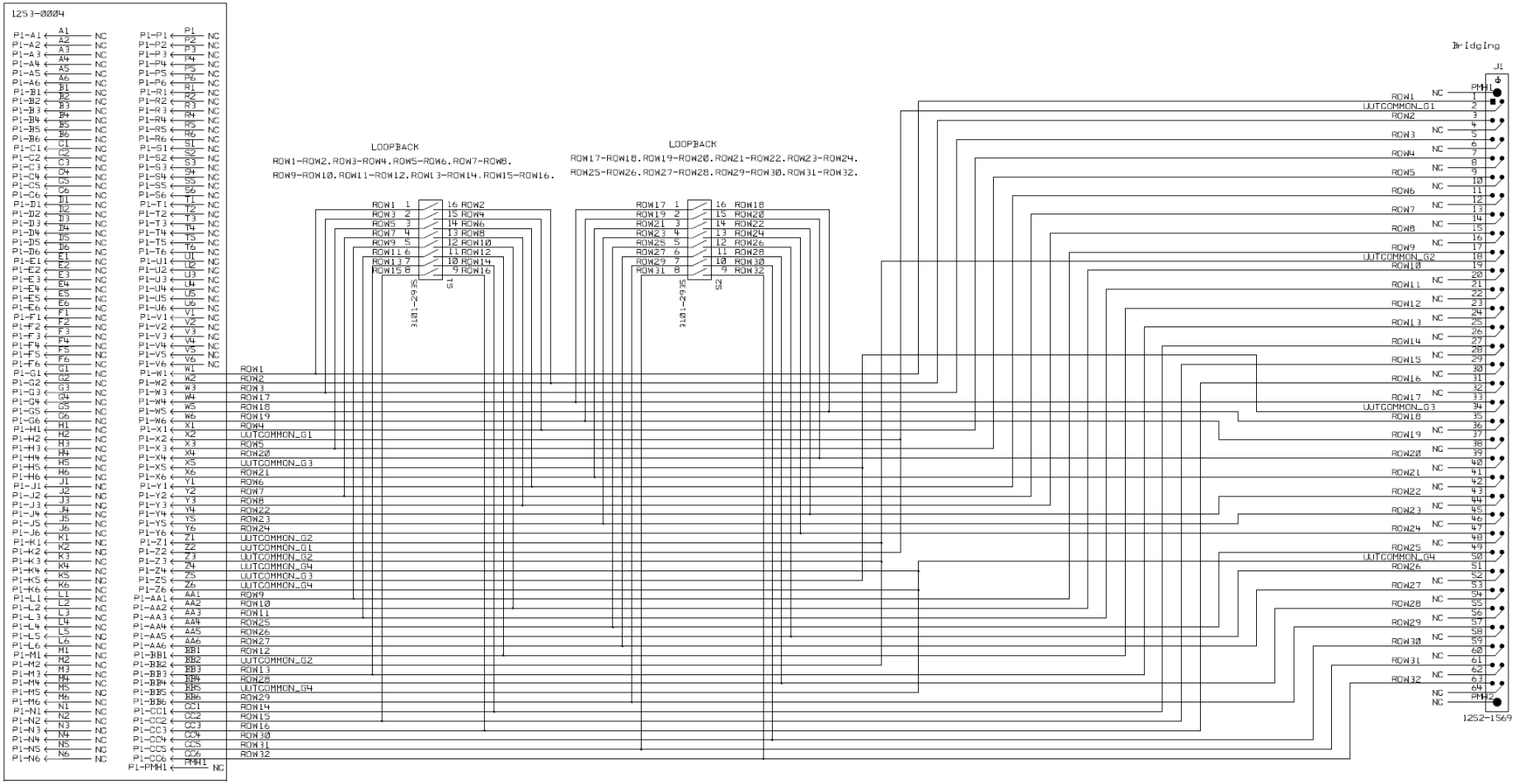


Table A-1 CEDGN Board #2 switch mapping summary

matrix row #	switch	TC connector pin
row 2	S1 (UP position)	PXI DAC DMM_H and PXI DAC DMM_C
	S1 (DOWN position)	PXI DAC1H
row 4	S1 (UP position)	PXI DAC DMM_L
	S1 (DOWN position)	PXI DAC1L
row 6	S2 (UP position)	PXI DAC TRIGGER
	S2 (DOWN position)	PXI DAC2H
row 8	S2 (UP position)	PXI DAC ZGNDF
	S2 (DOWN position)	PXI DAC2L

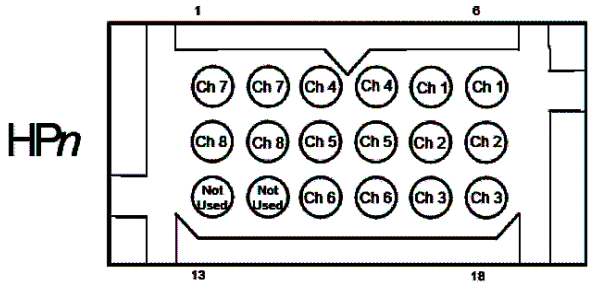
Table A-2 CEDGN Board #5 switch mapping summary

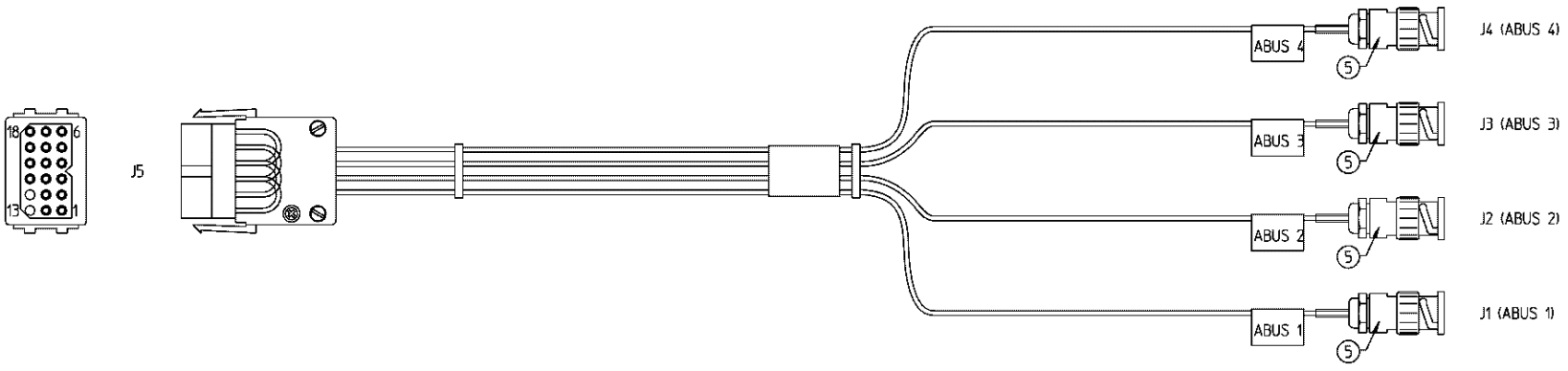
matrix row #	switch	TC connector pin
row 1	S1 Actuator 1 (ON) -CLOSE	row 2
	S1 Actuator 1 (OFF) -OPEN	NC
row 3	S1 Actuator 2 (ON) -CLOSE	row 4
	S1 Actuator 2(OFF) -OPEN	NC
row 5	S1 Actuator 3 (ON) -CLOSE	row 6
	S1 Actuator 3 (OFF) -OPEN	NC
row 7	S1 Actuator 4 (ON) -CLOSE	row 8
	S1 Actuator 4 (OFF) -OPEN	NC
row 9	S1 Actuator 5 (ON) -CLOSE	row 10
	S1 Actuator 5 (OFF) -OPEN	NC
row 11	S1 Actuator 6 (ON) -CLOSE	row 12
	S1 Actuator 6 (OFF) -OPEN	NC
row 13	S1 Actuator 7 (ON) -CLOSE	row 14
	S1 Actuator 7 (OFF) -OPEN	NC
row 15	S1 Actuator 8 (ON) -CLOSE	row 16
	S1 Actuator 8 (OFF) -OPEN	NC
row 17	S2 Actuator 1 (ON) -CLOSE	row 18
	S2 Actuator 1 (OFF) -OPEN	NC
row 19	S2 Actuator 2 (ON) -CLOSE	row 20
	S2 Actuator 2 (OFF) -OPEN	NC
row 21	S2 Actuator 3 (ON) -CLOSE	row 22
	S2 Actuator 3(OFF) -OPEN	NC
row 23	S2 Actuator 4 (ON) -CLOSE	row 24
	S2 Actuator 4 (OFF) -OPEN	NC
row 25	S2 Actuator 5 (ON) -CLOSE	row 26
	S2 Actuator 5 (OFF) -OPEN	NC
row 27	S2 Actuator 6 (ON) -CLOSE	row 28
	S2 Actuator 6 (OFF) -OPEN	NC
row 29	S2 Actuator 7 (ON) -CLOSE	row 30
	S2 Actuator 7 (OFF) -OPEN	NC
row 31	S1 Actuator 8 (ON) -CLOSE	row 32
	S1 Actuator 8 (OFF) -OPEN	NC

Schematic for E6170-61618 Diagnostic Cable for 8 Channel Heavy Duty Card

Figure A-6 E6170-61618 Diagnostic Cable for 8 Channel Heavy Duty Card

J5 PIN NUMBER	ITEM 5 NUMBER
1	J3
2	J4
3	J3
4	J4
5	J1
6	J2
7	J3
8	J4
9	J3
10	J4
11	J3
12	J4
13	N/C
14	N/C
15	J3
16	J4
17	J3
18	J4





Schematic for E6170-61607 Cable (Cable -2X 2X32 IDC PIN1 to PIN1)

Figure A-7 E6170-61607 Cable (Cable -2X 2X32 IDC PIN1 to PIN1)