

U4998A HDMI/MHL Protocol/Audio/Video Analyzer and Generator

User Guide



Notices

© Agilent Technologies, Inc. 2012

No part of this manual may be reproduced in any form or by any means (including electronic storage and retrieval or translation into a foreign language) without prior agreement and written consent from Agilent Technologies, Inc. as governed by United States and international copyright laws.

Trademarks

Microsoft®, MS-DOS®, Windows®, Windows 2000®, and Windows XP® are U.S. registered trademarks of Microsoft Corporation.

Adobe®, Acrobat®, and the Acrobat Logo® are trademarks of Adobe Systems Incorporated.

Software Release

Version 05.50.0000

Edition

November 2012

Available in electronic format only

Agilent Technologies, Inc. 1900 Garden of the Gods Road Colorado Springs, CO 80907 USA

Warranty

The material contained in this document is provided "as is," and is subject to being changed, without notice, in future editions. Further, to the maximum extent permitted by applicable law, Agilent disclaims all warranties, either express or implied, with regard to this manual and any information contained herein, including but not limited to the implied warranties of merchantability and fitness for a particular purpose. Agilent shall not be liable for errors or for incidental or consequential damages in connection with the furnishing, use, or performance of this document or of any information contained herein. Should Agilent and the user have a separate written agreement with warranty terms covering the material in this document that conflict with these terms, the warranty terms in the separate agreement shall control.

Technology Licenses

The hardware and/or software described in this document are furnished under a license and may be used or copied only in accordance with the terms of such license.

Restricted Rights Legend

If software is for use in the performance of a U.S. Government prime contract or subcontract, Software is delivered and licensed as "Commercial computer software" as defined in DFAR 252.227-7014 (June 1995), or as a "commercial item" as defined in FAR 2.101(a) or as "Restricted computer software" as defined in FAR 52.227-19 (June 1987) or any equivalent agency regulation or contract clause. Use, duplication or disclosure of Software is subject to Agilent Technologies' standard commercial license terms, and non-DOD Departments and Agencies of the U.S. Government will receive no greater than Restricted Rights as defined in FAR 52.227-19(c)(1-2) (June 1987). U.S. Government users will receive no greater than Limited Rights as defined in FAR 52.227-14 (June 1987) or DFAR 252.227-7015 (b)(2) (November 1995), as applicable in any technical data.

Safety Notices

CAUTION

A **CAUTION** notice denotes a hazard. It calls attention to an operating procedure, practice, or the like that, if not correctly performed or adhered to, could result in damage to the product or loss of important data. Do not proceed beyond a **CAUTION** notice until the indicated conditions are fully understood and met.

WARNING

A WARNING notice denotes a hazard. It calls attention to an operating procedure, practice, or the like that, if not correctly performed or adhered to, could result in personal injury or death. Do not proceed beyond a WARNING notice until the indicated conditions are fully understood and met.

Contents

1 Introduction to U4998A HDMI/MHL Protocol/Audio/Video Analyzer and Generator

What is U4998A HDMI/MHL Protocol/Audio/Video Analyzer and Generator 10

Features 11 Components 12 Hardware Components 12 13 Software Components Sample Setup of U4998A 16 U4998A Roles and Usage Scenarios 17 For Compliance Testing of a Source DUT 18 For Compliance Testing of a Sink DUT 25 For Debugging Source and Sink Devices 28

2 Establishing a Connection between U4998A and DUT

Before you start 32 Accessing the Agilent Logic and Protocol Analyzer GUI 33 Online mode 33 Offline mode 33 Accessing the Agilent Logic and Protocol Analyzer GUI in offline mode 33 Accessing the Agilent Logic and Protocol Analyzer GUI in online mode 35 Setting up a Connection between U4998A and DUT 36 **Connection modes** 36 Setting up a Connection between U4998A and DUT 37

3 Performing HDMI/MHL Compliance Testing for a Source Device

Overview 40 Configuring U4998A Data Capture Settings 42 Defining the EDID Block of U4998A 45 EDID Files Corresponding to HDMI Source Tests 47 EDID Files Corresponding to MHL Source Tests 49

Video Formats Supported by each EDID File 50 **Contents of Predefined EDID Files** 53 Setting up the EDID for U4998A 58 Using Multiple EDIDs for U4998A 58 Starting the Data Capture 61 Uploading the Captured data in a File 62 Monitoring the Transmitted Data on a Connected Sink Device 63 Evaluating the Captured Data for Compliance to HDMI/MHL CTS 64 Passed and Failed Tests 66 Supported HDMI Source Tests 68 Supported MHL Source Tests 70 Starting the Evaluation of Captured Data 70 Viewing Test Results 72 Importing Captured Data into Agilent Logic and Protocol Analyzer for further Analysis 78 Converting a .cap file to a module CSV file 79 Importing the Module CSV file into Logic and Protocol Analyzer GUI **Determining Frame Numbers in the Converted CSV File** 83 Locating Errors in the Converted CSV File 85

Viewing the Converted Data in Logic and Protocol Analyzer 90

4 Testing a HDMI/MHL Sink Device

Overview 98

Using the Predefined Audio and Video Files for transmission 99 Naming convention for the predefined audio and video files 100 Supported Sink Tests 101 Video Format Timings supported by .vgf Files 101

Configuring Frame Settings for Transmission to a Sink Device 104

Starting and Stopping the Transmission of Frames 107

Evaluating the Sink Device for Compliance to HDMI/MHL CTS 109
8-16 Acceptance of all valid packet types 109
8-21 Audio Clock Regeneration 112
Test 8-23. Audio Formats 113

Test 8-25. Deep Color 114

5 Debugging a HDMI/MHL Source and Sink Device

Overview 126

Configuring U4998A Data Capture Settings 127 Connecting U4998A to DUTs 127 EDID Block of the Sink DUT 127
Resetting the Hot Pug Detect Mechanism from U4998A 128
Starting the Data Capture and Uploading the Captured Data 128
Importing Captured Data into Agilent Logic and Protocol Analyzer 128
Viewing the Converted Data in Logic and Protocol Analyzer for Debugging 129

6 Using COM Interface for HDMI/MHL Testing

Overview 132 Before you start 133 **COM Servers** 133 134 Examples on Usage Method for Configuring U4998A Settings 135 DoCommands 135 XML Elements Hierarchy for DoCommands 135 <Module> Element 138 <Connection> Element 138 <Capture> Element 139 <Evaluate> Element and its Descendants 140 <Generate> Element and its Descendants 150 Methods for Capturing HDMI/MHL Data 153 WriteEDID 153 **HPDReset** 153 StartCapture 154 LEDRefresh 155 ExportCapture 155 Methods for Evaluating the Captured Data 156 **GetBitmapFiles** 156 GetTMDSClockValue 156 StartEvaluate 157 Methods for Generating HDMI/MHL Data 159 StartGenerator 159 StopGenerator 160 Status 161 WaitReady 162



1

Agilent U4998A HDMI/MHL Protocol/Audio/Video Analyzer and Generator User Guide

Introduction to U4998A HDMI/MHL Protocol/Audio/Video Analyzer and Generator

What is U4998A HDMI/MHL Protocol/Audio/Video Analyzer and Generator 10 Features 11 Components 12 Sample Setup of U4998A 16 U4998A Roles and Usage Scenarios 17

This chapter provides information on the hardware and software components of U4998A HDMI/MHL Protocol/Audio/Video Analyzer and Generator. This chapter also describes its features and various roles in testing HDMI/MHL sink and source devices.



What is U4998A HDMI/MHL Protocol/Audio/Video Analyzer and Generator

The Agilent U4998A HDMI/MHL Protocol/Audio/Video Analyzer and Generator (hereafter referred to as U4998A) is a test and debug tool that provides features for testing the HDMI/MHL sink and source devices. You can use it to perform HDMI/MHL compliance testing and debug HDMI/MHL devices.

U4998A can test a HDMI/MHL source device by capturing the data transmitted by this device and analyzing the captured data for compliance to HDMI/MHL Compliance Test Specifications (CTS). It can also test a HDMI/MHL sink device by transmitting audio and video frames to this device to analyze if the device passes the HDMI/MHL CTS sink tests.

Features

This topic lists the key features of U4998A.

- Provides debug as well as compliance testing features to test HDMI DUTs as per the HDMI 1.4b CTS and MHL DUTs as per MHL 1.2 CTS.
- Provides HDMI IN as well as HDMI OUT connectors to act as a receiver and a transmitter over a HDMI link.
- Supports HDMI CTS 1.4a/1.4b sink and source tests. All the source tests except 7-1 till 7-15 and 7-20 till 7-22 are supported. For running sink tests, it provides the required audio/video files for all sink tests except 8-2, 8-27, and 8-28.
- Supports 3.2.2.1, 3.2.2.2, 3.2.2.3, 3.2.3.1, 3.2.3.2, 3.2.3.3, 3.2.3.4, 3.2.4.1, 3.2.4.2, and 3.2.4.3 MHL source tests.
- Supports 4.2.1.1, 4.2.1.2, 4.2.2.1, 4.2.2.2, 4.2.2.3, 4.2.3.1, and 4.2.3.2 MHL sink tests.
- Supports a maximum memory depth of 4GB for capturing the data received from DUT.
- Supports offline evaluation of the data received from a source HDMI/MHL DUT for testing compliance to HDMI/MHL CTS. This data can be stored in .cap files.
- As a HDMI/MHL sink device, U4998A can accept any audio and video format from the source DUT and capture it in a .cap file.
- As a HDMI/MHL source device, U4998A provides a set of predefined video files in the .vgf format and audio files in the .aaf format for transmission to a sink DUT. This set of audio and video files are provided as per the HDMI/MHL sink tests requirements so that you can run various sink tests for the DUT.

Components

The following is a list of hardware and software components of U4998A.

Hardware Components

U4998A HDMI/MHL Protocol/Audio/Video Analyzer and Generator module

The U4998A HDMI/MHL Protocol/Audio/Video Analyzer and Generator is a module installed in an Agilent AMP or AXIe chassis, for example, the Agilent M9502A portable 2-slot chassis. The module can emulate a HDMI/MHL sink or source device and can transmit or receive data over an HDMI link. The module is connected to an HDMI DUT using an HDMI cable and to an MHL DUT via the U4995A MHL adapter and MHL cable shipped with the module (if you have purchased the MHL hardware license).

You need a Category-2 Certified HDMI cable (supporting transfer rates of up to 340Mhz or 10.2gbps).

Chassis

You can use one of the following chassis to install the U4998A module:

- Agilent U4002A 2-slot AMP chassis
- Agilent M9502A 2-slot or M9505A 5-slot AXIe chassis

These chassis have slots which you can use to install application modules such as the U4998A module.

Controller PC

The Controller PC hosts the U4998A software to allow you to set up, configure, and use the U4998A module using GUIs/APIs.

The controller PC is connected to Agilent AMP or AXIe chassis via a PCIe x4/x8 Host Interface board.

For more information about these hardware components, refer to the *AXIe Based Logic Analysis and Protocol Test Modules Installation Guide*. This guide is available for download at www.agilent.com and is also located at:



Figure 1 Location of U4998A Guides

Refer to the Agilent M9502A/M9505A AXIe Chassis Startup Guide to get detailed information about the AXIe chassis.

Software Components

All the software components of U4998A are installed on the controller PC.

Agilent Logic and Protocol Analyzer

NOTE

You do not need the Agilent Logic Analyzer hardware for HDMI/MHL testing.

The Agilent Logic and Protocol Analyzer software provides a GUI interface to set up, configure, and use the frame generator and capture capabilities of the U4998A module. In the context of this module, you can use the Agilent Logic and Protocol Analyzer software to:

- configure and establish a connection between the U4998A module and HDMI/MHL DUT.
- configure the settings that control how and where the data received from DUT is captured for evaluation and analysis.
- configure the settings that control the audio/video frames that the U4998A module transmits to an HDMI/MHL DUT.
- define the EDID block of U4998A when it acts as a terminator.
- start and stop the transmission of frames to an HDMI/MHL DUT.

The topics that follow in this guide describe these tasks in detail.

HDMI/MHL Evaluator

The HDMI/MHL Evaluator software is used to perform an offline evaluation on the captured HDMI/MHL data that a source DUT transmitted to U4998A.

You can capture the data transmitted by a source HDMI/MHL DUT using the Agilent Logic and Protocol Analyzer software and store it in a .cap file. You can then evaluate the data from this file using HDMI/MHL Evaluator for testing DUT's compliance to HDMI/MHL specifications. HDMI Evaluator provides a number of HDMI and MHL source tests that you can run on the captured data to check if the source DUT passes these tests.

In the HDMI/MHL Evaluator application, only the U4998A tab of the GUI is used. The other tab N5998A is not applicable to U4998A and instead the Logic and Protocol Analyzer GUI is used to perform all other tasks except the evaluation task. The N5998A tab of the GUI is applicable and used if you are using and are connected to the N5998A HDMI/MHL Analyzer hardware.

U4998A HDMI Video Generator Files software

When you install this software component,

• a set of predefined Video and Audio Generator files (.vgf and .aaf) are installed. You can transmit any of these predefined video files to an HDMI sink DUT from U4998A using the Agilent Logic and Protocol Analyzer GUI.

To know more, refer to the topic, "Using the Predefined Audio and Video Files for transmission" on page 99.

• a set of EDID sample data files (.edi files) are installed. You can use any of these files to define the EDID of U4998A when emulating an HDMI sink device.

To know more, refer to the topic, "Defining the EDID Block of U4998A" on page 45.

U4998A MHL Video Generator Files software

When you install this software component,

• a set of predefined Video and Audio Generator files (.vgf and .aaf) are installed. You can transmit any of these predefined video files to an MHL sink DUT from U4998A using the Agilent Logic and Protocol Analyzer GUI.

To know more, refer to the topic, "Using the Predefined Audio and Video Files for transmission" on page 99.

• a set of EDID sample data files (.edi files) are installed. You can use any of these files to define the EDID of U4998A when emulating an MHL sink device.

To know more, refer to the topic, "Defining the EDID Block of U4998A" on page 45.

Agilent Generate Module CSV from HDMI/MHL Capture File utility

This utility is an optional software component and requires a software license. This utility converts the HDMI/MHL capture file (.cap file) that has the data received from HDMI/MHL source DUT into a module CSV file. You can import the converted module CSV file into the Agilent Logic and Protocol Analyzer GUI for deeper analysis of the captured data.

To know more about this utility and how to use it, refer to the topic "Importing Captured Data into Agilent Logic and Protocol Analyzer for further Analysis" on page 78 in this guide.

For more information on how to install these software components, refer to the AXIe Based Logic Analysis and Protocol Test Modules Installation guide located at <Install location of Logic Analyzer>\help\pdfs.

Sample Setup of U4998A

The following is a sample setup of U4998A with all its software and hardware components for testing an HDMI DUT.





The following is a sample setup of U4998A with all its software and hardware components for testing an MHL DUT.





U4998A Roles and Usage Scenarios

U4998A can emulate:

- an HDMI source or sink device to test or debug HDMI devices.
- an MHL source or sink device to test or debug MHL devices.

This topic illustrates and briefly describes its roles and usage for compliance testing and debugging of HDMI/MHL devices based on its various connection modes.

You can use U4998A to test HDMI and MHL devices to ensure that these are compliant to HDMI/MHL specifications.

For Compliance Testing of a Source DUT

For HDMI Source DUT Compliance Testing

For an HDMI source DUT, U4998A can act as a terminator and can receive the data transmitted by the source DUT over an HDMI link to evaluate and analyze this data as per the source tests.

The following figure illustrates a typical configuration of U4998A as a Terminator in the context of HDMI compliance testing.

Logic Analyzer GUI (Configure Data Capture Setup and Start Capture)





As illustrated in the above figure, the Logic and Protocol Analyzer GUI is used to configure the HDMI connection and data capture settings of U4998A. The HDMI connection is configured in the *Capture* mode to ensure that U4998A emulates the role of a HDMI sink device. The source DUT reads the EDID of U4998A and transmits data to U4998A. The transmitted data is stored in U4998A memory from where it is uploaded in a specified .cap file as per the configured data capture settings. This captured data is then used in the HDMI Evaluator GUI to evaluate the source DUT as per the HDMI specifications.

Refer to the "Performing HDMI/MHL Compliance Testing for a Source Device chapter to know more about the usage of U4998A as a Terminator.

Besides using U4998A to capture the data transmitted by a source DUT, you can also connect U4998A to a sink device on the other end. This allows you to do capturing as well as real-time monitoring of the data transmitted by the source DUT. The sink device connected to U4998A is not considered a sink DUT in this case and this device just provides a way of passively displaying the data transmitted by the source DUT. The source DUT reads the EDID of U4998A in this case to transmit data according to U4998A's EDID.

The following figure illustrates a typical configuration of U4998A for capturing as well as monitoring the HDMI data transmitted by a source DUT.





As illustrated in the above figure, the Logic and Protocol Analyzer GUI is used to configure the HDMI connection and data capture settings of U4998A. The HDMI connection is configured in the *Mirror* mode to ensure that U4998A emulates the role of a HDMI sink device. The source DUT reads the EDID of U4998A through the DDC communication between source DUT and U4998A and transmits data to U4998A. U4998A:

- stores the transmitted data in its memory from where it is uploaded into a .cap file as per the configured data capture settings. This captured data is then used in the HDMI Evaluator GUI to evaluate the source DUT as per the HDMI specifications.
- simultaneously sends the transmitted data to the connected sink device for displaying the data.

NOTE	Ensure that you have the U4998A-PSV license or U4998U-PSV upgrade license to use U4998A in the Mirror connection mode.
	For MHL Source DUT Compliance Testing
	For an MHL source DUT, U4998A can act as a terminator and can receive the MHL data transmitted by the source DUT to evaluate and analyze this data as per the MHL source tests.
NOTE	Ensure that you have the U4998A-MHL hardware license to use U4998A for MHL testing.
	The U4995A MHL adapter is used between the U4998A module and source DUT while establishing hardware connections. One end of the adapter is connected to U4998A's HDMI IN connector via an HDMI cable. The other end of the adapter is connected to the MHL source DUT via an MHL cable.

The following figure illustrates a typical configuration of U4998A as a Terminator in the context of MHL compliance testing.



Logic Analyzer GUI (Configure MHL Data Capture Setup and Start Capture)



As illustrated in the above figure, the Logic and Protocol Analyzer GUI is used to configure the connection mode and data capture settings of U4998A. The connection to the source DUT is configured in the *Capture* mode to ensure that U4998A emulates the role of a MHL sink device. The source DUT reads the EDID of U4998A and transmits data to U4998A. The transmitted data is stored in U4998A memory from where it is uploaded in a specified .cap file as per the configured data capture settings. This captured data is then used in the HDMI/MHL Evaluator GUI to evaluate the source DUT as per the MHL specifications.

Refer to the "Performing HDMI/MHL Compliance Testing for a Source Device chapter to know more about the usage of U4998A as a Terminator.

For Compliance Testing of a Sink DUT

For HDMI Sink DUT Compliance Testing

For an HDMI sink DUT, U4998A can act as a generator and can transmit the specified audio/video frames to the sink DUT over an HDMI link.

The following figure illustrates a typical configuration of U4998A as a Frame Generator in the context of HDMI testing.

Logic Analyzer GUI (Configure Frame Setup and Start transmission)

State (2010) A children (2010) A children (2010) State (2010) A children (2010) A children (2010) Matchine Matchine Call Dial (2010) A children (2010) Call Dial (2010) A	Appen Universe (Cardigatetter, (Overview) gener gener gener getter på H T H R R R M [FEET] Is T [FEE] [H [FEET] Sner Constant See Cardinate (See See) Print Constant See Cardinate (See See See) Print Constant See Cardinate (See See See) Print Constant See Cardinate (See See See) Print See (See See See See See) Print See (See See See See See See See See) Print See (See See See See See See See See Se		
	Connection and Frame settings		Run Sink Tests on the received data Data Evaluation
	U4998A HDMI Analyzer and Generator Module HDMI OUT	HDMILink	HDMI Sink DUT

Figure 7 Usage as a Generator in HDMI testing

As illustrated in the above figure, the Logic and Protocol Analyzer GUI is used to configure the HDMI connection and frame settings of U4998A. The HDMI connection is configured in the *Frame Generator* mode to ensure that U4998A emulates the role of a HDMI source device. In this scenario, no EDID communication takes place between U4998A and sink DUT. U4998A transmits the configured audio and video frames to DUT when you start the data transmission using the Logic and Protocol Analyzer GUI. You can evaluate the data received at the DUT end to check if the DUT passes the sink tests as per the HDMI specifications.

Refer to the "Testing a HDMI/MHL Sink Device chapter to know more about the usage of U4998A as a Generator.

For MHL Sink DUT Compliance Testing

For an MHL sink DUT, U4998A can act as a generator and can transmit the specified audio/video frames to the sink DUT.

NOTE Ensure that you have the U4998A-MHL hardware license to use U4998A for MHL testing.

The U4995A MHL adapter is used between the U4998A module and MHL sink DUT while establishing hardware connections. One end of the adapter is connected to U4998A's HDMI OUT connector via an HDMI cable. The other end of the adapter is connected to the MHL sink DUT via an MHL cable.

The following figure illustrates a typical configuration of U4998A as a Frame Generator in the context of MHL testing.



Logic Analyzer GUI (Configure Frame Setup and Start transmission)

AXIe Chassis

Figure 8 Usage as a Generator in MHL testing

As illustrated in the above figure, the Logic and Protocol Analyzer GUI is used to configure the connection and frame settings of U4998A. The connection is configured in the *Frame Generator* mode to ensure that U4998A emulates the role of an MHL source device. In this scenario, no EDID communication takes place between U4998A and MHL sink DUT. U4998A transmits the configured audio and video frames to DUT when you start the data transmission using the Logic and Protocol Analyzer GUI. You can evaluate the data received at the DUT end to check if the DUT passes the sink tests as per the MHL specifications.

Refer to the "Testing a HDMI/MHL Sink Device chapter to know more about the usage of U4998A as a Generator.

For Debugging Source and Sink Devices

For debugging purposes, U4998A can act as a pass through device between an HDMI source and an HDMI sink DUT. It can passively monitor and capture the data transmitted from the source DUT to the sink DUT. This passive monitoring and capturing can help debug the root cause of a problem. You can identify if the source DUT or the sink DUT is the cause of a problem.



Figure 9 Usage of U4998A for debugging HDMI sink and source devices

As illustrated in the above figure, the Logic and Protocol Analyzer GUI is used to configure the connection and data capture settings of U4998A. The connection is configured in the **Pass through** mode to ensure that U4998A performs the role of passing through the data that it receives from an HDMI source DUT to an HDMI sink DUT. The source DUT reads the EDID of the sink DUT. U4998A:

- stores the data transmitted by the source DUT in its memory from where it is uploaded into a .cap file as per the configured data capture settings. This captured data is then used to troubleshoot and debug problems.
- simultaneously sends the transmitted data to the connected sink DUT.

NOTE Ensure that you have the U4998A-PSV license or U4998U-PSV upgrade license to use U4998A in the Pass-through connection mode.

Refer to the "Debugging Source and Sink Devices" on page 123 to know more about the usage of U4998A in the pass through mode. 1 Introduction to U4998A HDMI/MHL Protocol/Audio/Video Analyzer and Generator



 $\label{eq:constraint} \begin{array}{l} \mbox{Agilent U4998A HDMI/MHL Protocol/Audio/Video Analyzer and Generator} \\ \mbox{User Guide} \end{array}$

2 Establishing a Connection between U4998A and DUT

Before you start 30 Accessing the Agilent Logic Analyzer GUI 31 Setting up a Connection between U4998A and DUT 34

This chapter provides information on how you can create an appropriate connection between U4998A and DUT to perform HDMI/MHL testing.



Before you start

Before you start configuring connection settings between the U4998A and DUT, ensure that you have:

- Installed the U4998A module into the Agilent Digital Test Console chassis or the Agilent AXIe chassis. Refer to the AXIe Based Logic Analysis and Protocol Test Modules Installation Guide to know more.
- Installed the required software (Agilent Logic and Protocol Analyzer and HDMI/MHL Evaluator) on Controller PC. Refer to the *AXIe Based Logic Analysis and Protocol Test Modules Installation Guide* to know more.
- Connected the Agilent chassis to the Controller PC via a PCI Express cable. Refer to the AXIe Based Logic Analysis and Protocol Test Modules Installation Guide to know more.
- In case of HDMI testing, connected the HDMI DUT to U4998A using a HDMI cable. It is recommended that you define the EDID block of U4998A (when using it as a sink device for testing a source DUT) before connecting it to the source DUT. This is because the source DUT immediately reads the EDID of U4998A on getting connected. Absence of the desired EDID for U4998A can cause problems in data transmission as per the U4998A capabilities.
- In case of MHL testing, connected the MHL DUT to U4998A via the U4995A MHL adapter that accompanied the module shipment. The adapter is connected to U4998A using an HDMI cable and to the MHL DUT using an MHL cable.

Accessing the Agilent Logic and Protocol Analyzer GUI

You use the Agilent Logic and Protocol Analyzer GUI to configure connection settings between U4998A and DUT and to configure settings needed for HDMI/MHL testing.

This topic describes how you can access this GUI in offline and online modes to set up a connection and to perform configuration tasks for HDMI/MHL testing.

Online mode

In this mode, the Agilent Logic and Protocol Analyzer software (hosted on the Controller PC) is connected to the U4998A module. This mode is preferred when you want to perform the HDMI/MHL configuration and testing tasks while being connected to the U4998A module. For tasks, such as starting the transmission of frames to a DUT or capturing data transmitted by DUT, a connection to the U4998A module is needed. Therefore, for such tasks, you need to access the Agilent Logic and Protocol Analyzer GUI in the online mode.

Offline mode

In this mode, there is no connection between the U4998A module and Controller PC hosting the Logic and Protocol Analyzer software. This mode is preferred for setting up and saving the testing configurations without being connected to the U4998A module. These configurations can later be used to perform HDMI/MHL testing when the Agilent Logic and Protocol Analyzer GUI is connected to the U4998A module in an online mode.

Accessing the Agilent Logic and Protocol Analyzer GUI in offline mode

1 Click Start > Programs > Agilent Logic Analyzer > Agilent Logic and Protocol Analyzer option on the Windows task bar.

The Offline Startup Options dialog box is displayed.

2 Click **Continue Offline** to start the Agilent Logic and Protocol Analyzer application in the offline mode, that is, not connected to the U4998A module.

The Create a New Configuration dialog box is displayed.

- **3** Select the type of analysis hardware which you want to configure in offline mode. In this case, select the **U4998A HDMI Protocol/Audio/Video Analyzer and Generator** option from the **Type of Card** listbox to configure U4998A in offline mode.
- **4** From the **Number of Cards in** listbox, select the number of cards in the hardware module. For U4998A, you can select One Card Module.
- **5** Select the starting slot for U4998A.
- 6 Click OK.

The Agilent Logic and Protocol Analyzer GUI is displayed with a module added for U4998A in the Overview window. You can use this module to configure and use the U4998A module for HDMI/MHL testing.

🦉 [Offline] Agilent Logic Analyzer - Unnamed Confi 🔳 🗖 🔀
Tile Edit View Setup Tools Markers Run/Stop Overview Window Help
▋D 📽 🖬 🚳 ぬ 🐂 ๙ 💌 T 💌 🔍 🔍 🐄 共日
M1 to M2 =
Modules
Slot 2
HDMI-102
Cverview
For Help, press F1 (tatus.)

Figure 10 HDMI module added in offline mode

Accessing the Agilent Logic and Protocol Analyzer GUI in online mode

1 Click Start > Programs > Agilent Logic Analyzer > Agilent Logic and Protocol Analyzer option on the Windows task bar.

The Agilent Logic and Protocol Analyzer GUI is displayed. Due to the existence of a connection between Logic and Protocol Analyzer and U4998A in online mode, a module is automatically added for U4998A in the Overview window of Logic and Protocol Analyzer. You can use this module to configure and use U4998A for HDMI/MHL testing.

Agilent Logic Analyzer - Unnamed Configuration	
Tile Edit View Setup Tools Markers Run/Stop Overview Window Help	- 8 ×
🗈 🖻 🖶 🎒 🗛 🐂 🕷 🕨 T 💌 🔍 🔍 🐄	
M1 to M2 =	
Modules	
Slot 2	
HDMI-102	
	>
S Overview	
For Help, press F1	fitatus.

Figure 11 HDMI module added in online mode

Setting up a Connection between U4998A and DUT

To perform HDMI/MHL compliance testing or debugging a DUT using U4998A, you first need to set up a connection between U4998A and DUT.

When you connect U4998A and an HDMI DUT using an HDMI cable, the two devices get connected through a Hot Plug Detect mechanism. For an MHL DUT, the U4995A MHL adapter is used between U4998A and DUT.

Once the devices are connected, you need to configure the connection settings. The connection settings primarily indicate how you want to use U4998A for testing a HDMI/MHL DUT. U4998A can emulate a source or a sink HDMI/MHL device or a pass through device depending on the connection settings.

U4998A has four connection modes available to ensure that an appropriate connection is established based on the specific HDMI/MHL testing scenario. The following section describes these connection modes of U4998A.

Connection modes

- U4998A-Frame Generator You use this connection mode when you want U4998A to emulate a HDMI/MHL source device to test a HDMI/MHL sink device. In this mode, U4998A can transmit the configured audio and video frames to a HDMI/MHL sink DUT. This mode is useful for performing HDMI/MHL compliance testing of a sink DUT.
- **U4998A-Capture (Terminator)** You use this connection mode when you want U4998A to emulate a HDMI/MHL sink device to test a HDMI/MHL source device. In this mode, U4998A can capture the data transmitted by a HDMI/MHL source DUT to analyze and evaluate the source DUT's compliance to HDMI/MHL specifications.
- **U4998A- Pass- through** You use this connection mode when you want U4998A to act as a pass through device between an HDMI source and an HDMI sink DUT connected to HDMI IN and OUT connectors of U4998A. This mode is useful when you want to debug an HDMI source or a sink DUT. In this mode, U4998A can capture the data transmitted by the HDMI source DUT to the HDMI sink DUT. You can then analyze the captured data to troubleshoot the cause of a problem.

• U4998A-Mirror - You use this connection mode when you want U4998A to emulate an HDMI sink device to test an HDMI source device. In this mode, U4998A can capture the data transmitted by an HDMI source DUT to analyze and evaluate the source DUT's compliance to HDMI specifications. In this mode, you can also connect U4998A to a sink device to display the input signals that U4998A receives from the HDMI source DUT. This ensures simultaneous capturing as well as monitoring of the data transmitted by the source DUT.

To get a visual representation and description of U4998A setup in all these connection modes, refer to the topic "U4998A Roles and Usage Scenarios.

Setting up a Connection between U4998A and DUT

You use the Agilent Logic and Protocol Analyzer GUI to configure the connection settings between U4998A and DUT. You can access this GUI in either online or offline mode to accomplish this task.

NOTE

Ensure that you have the appropriate license for the required connection mode to use U4998A in that mode. The following are the licenses available for these connection modes.

- U4998A-CMP Capture/Compliance testing license
- U4998A-GEN Generator license

These licenses are included in the U4998A Standard license.

- U4998A-PSV or U4998U-PSV Passive Monitoring license. With this license, you get the Pass-through and Mirror modes of U4998A. This license needs to be obtained separately.

To set up a HDMI/MHL connection

- 1 Access the Agilent Logic and Protocol Analyzer GUI with appropriate U4998A hardware configurations. Refer to the topic "Accessing the Agilent Logic Analyzer GUI" on page 31 to know more.
- 2 Click the HDMI module displayed in the **Overview** window of Logic and Protocol Analyzer GUI.
- **3** Select **Setup** -> **Setup** from the menu displayed on clicking the HDMI module.

The Setup dialog box is displayed.

- 4 Click the **Connection Setup** tab to configure the connection settings between U4998A and DUT.
- **5** From the **Connection** listbox, select the appropriate connection type needed based on the HDMI/MHL testing scenario. Refer to "Connection modes" on page 34 to know more.
- **6** Based on the connection type selected, you can get a visual representation of the HDMI/MHL connection by clicking the **Connection diagram** button.
- 7 In the Link Naming and Lane Setup group box, select the Clock Source that you want to use for the HDMI link. The following options are available for selecting a clock source:
 - **TMDS** This is applicable if you selected Capture, Pass-through, or Mirror modes. Selecting this option ensures that U4998A uses the TMDS clock transmitted by the sink DUT as a frequency reference for the data recovery on the three TMDS data channels. The TMDS clock runs at a rate corresponding to the pixel rate of the video transmitted from DUT.
 - **Internal** This is applicable if U4998A emulates a generator. Selecting this option ensures that U4998A transmits an internal clock to the sink DUT to recover the transmitted data as per that clock frequency reference.
- 8 If required, you can change the name of the HDMI link between U4998A and DUT. To do this, select the HDMI Link from the Link Naming and Lane Setup group box and click Rename.
- **9** You can add multiple HDMI links using the **Add Folder** button displayed in the **Link Naming and Lane Setup** group box. You may want to add folders to organize the HDMI Links folder specially when the number of frames are large.
- 10 Click Apply and then OK.


3

Agilent U4998A HDMI/MHL Protocol/Audio/Video Analyzer and Generator User Guide

Performing HDMI/MHL Compliance Testing for a Source Device

Overview 40 Configuring U4998A Data Capture Settings 42 Defining the EDID Block of U4998A 45 Starting the Data Capture 61 Uploading the Captured data in a File 62 Monitoring the Transmitted Data on a Connected Sink Device 63 Evaluating the Captured Data for Compliance to HDMI/MHL CTS 64 Importing Captured Data into Agilent Logic and Protocol Analyzer for further Analysis 78 Viewing the Converted Data in Logic and Protocol Analyzer 90

This chapter describes how you can configure U4998A to test if a HDMI/MHL source DUT is compliant to HDMI/MHL specifications. It describes how you can capture, evaluate, and analyze the data that U4998A receives from a source DUT.



Overview

The following figure illustrates the broad steps that you need to perform to do HDMI/MHL compliance testing for a source DUT using U4998A.



Figure 14 HDMI/MHL Capture flow

The topics that follow describe each of these tasks in detail.

Refer to the topic "U4998A Roles and Usage Scenarios" on page 17 to get a pictorial representation of U4998A as a terminator.

Configuring U4998A Data Capture Settings

NOTE

To perform compliance testing for a HDMI/MHL source DUT, U4998A needs to emulate a HDMI/MHL sink device that can receive data from the source DUT. Therefore, ensure that you select the connection type as U4998A - Capture or U4998A - Mirror while setting up a connection between U4998A and DUT.

Refer to the topic "Setting up a Connection between U4998A and DUT" on page 34 to know more about these modes.

The data capture settings control how and where you want to capture the data received from a HDMI/MHL source DUT for compliance evaluation and analysis.

You use the Logic and Protocol Analyzer GUI to configure the capture setup.

Setup
Connection Setup Capture Setup Frame Setup
Capture Setup
Capture Memory Depth 128 (1-4096]MB
Detected TMDS Clock 67127155 Hz Copy
Hot Plug Detect (HPD) Reset
LED Status Refresh
Capture Mode O DVI 💿 HDMI 🔘 MHL
Capture Storage
Increment file number between captures, starting with 1
Capture File base C:\Users\dvutest\Documents\Agilent Technologies\Logic Analyzer\Export Files\HDMICapture.cap
EDID Setup
EDID File No Edid File Is Selected
Apply OK C

To configure the data capture settings:

- 1 Access the **Setup** dialog box by clicking **Setup** > **Setup** from the drop-down menu displayed for the HDMI module.
- 2 Click the Capture Setup tab.
- 3 In the **Capture Memory Depth** field, specify the memory depth of U4998A that you want to use for capturing the data received from DUT. By default, **128** MB is the default allocation for capturing data in U4998A module memory. You can either type a desired value for memory depth or increase/decrease the default value as per your requirement. The specified memory depth should be within the range of 1 to 4096 MB. When the selected capture memory depth is full, the U4998A module stops capturing the data. Consider the following points when selecting capture memory depth:
 - Out of the maximum capture memory available, some part is consumed by internal logic.
 - A pixel requires eight bytes in the capture memory of U4998A module and subsequently in the capture file. For source audio tests, you calculate the memory depth required to capture at least two seconds of sample time.

The TMDS clock frequency is detected and displayed in the **Detected TMDS Clock** field. This field displays the current frequency of the TMDS clock based on the pixel rate of the transmitted video from DUT. You need to specify this frequency value in the HDMI/MHL Evaluator GUI while running some of the HDMI/MHL Source tests on the captured data. You can view this frequency value before or after the data capture.

You can use the **Copy** button displayed with the **Detected TMDS Clock** field to copy the currently detected TMDS clock frequency and paste it in the **TMDS Clock(Hz)** field in the HDMI/MHL Evaluator GUI.

4 Click the Reset button displayed with the Hot Plug Detect field to force the emulation of the Hot Plug Detect mechanism. On clicking Reset, DUT reperforms the initialization sequence without going through the Hot Plug Detect with U4998A. This is particularly useful in instances such as forcing the DUT to read the updated or changed EDID block of U4998A as a part of the initialization sequence. DUT reads the EDID block of U4998A immediately on getting connected. If you have updated the EDID block after connection, then clicking

NOTE

Reset before	starting the	capture can	serve the	purpose
of forcing the	e DUT to rea	ad the updat	ed EDID.	

- **5** Click the **Refresh** button displayed with the **LED Status** field to manually refresh the status of the TMDS data channel LEDs for the HDMI IN connector on the front panel of the U4998A module.
- **6** From the **Capture Mode** options, select the protocol (DVI, HDMI, or MHL) to indicate whether you want to capture DVI, HDMI, or MHL data. The default option is **HDMI**.

NOTE

In the **Capture mode** options, the **MHL** option is disabled if you do not have the U4998-MHL hardware license. To use the U4998A module for MHL source or sink testing, you need the MHL hardware license.

- 7 The fields in the **Capture storage** group control where you want to save the captured data for evaluation and analysis. For capture storage, you have the following two options:
 - Specify the location and name of the .cap file in the **Capture File Base** field. This ensures that whenever you click Upload, the captured data stored in the memory of U4998A is uploaded in the specified .cap file. If the .cap file already exists due to a previous capture run, then the contents of the file gets overwritten by the current upload.
 - Specify the location and name of the .cap file to be used as a base in the **Capture File Base** field. Additionally, select the **Increment File Number between Captures**, **starting with** checkbox and specify an integer value for the increment. This ensures that whenever you click Upload, the captured data stored in the memory of U4998A module is uploaded in a new .cap file with the same base name but appended by the applicable incremented number.

NOTE	When the capture completes, you use the Upload button to upload the
NUL	data stored in the memory of the U4998A module to the specified .cap file.
	If you click Upload before starting the data capture, either a .cap file of 0
	KB is created at the specified location or a .cap file with the data from
	some previous capture in the memory is created.

8 Click Apply and then OK.

Defining the EDID Block of U4998A

When U4998A emulates a sink device (in Capture and Mirror connection modes), HDMI/MHL source DUT needs to read its EDID (Extended Display Identification Data) block. Therefore, while testing a source DUT, you need to define the EDID block of U4998A. Defining this block ensures that the source DUT can adjust the data transmission based on U4998A's configurations and capabilities as defined in this block.

Defining the EDID block also helps you test and analyze if the source DUT can read the EDID block of the sink device (U4998A in this case) and can transmit audio and video formats as per the capabilities of the sink device.

U4998A provides a number of predefined EDID sample data files. You need to install:

- the *U*4998A HDMI Video Generator Files software component to get a set of predefined EDID files for HDMI testing.
- the *U*4998A *MHL Video Generator Files* software component to get a set of predefined EDID files for MHL testing.

On installing the above-mentioned components, a set of .edi files is installed at a default location or a location that you specify while installation. The following figures display the default locations for the installation of sample EDID data files for MHL and HDMI.









As per the source test requirements, you can use a predefined EDID file to define the EDID block structure for U4998A. If needed, you can also use your own EDID file for this purpose.

EDID Files Corresponding to HDMI Source Tests

The set of predefined EDID files for HDMI are as per the requirements of HDMI source tests. The following tables list the EDID files that are provided for each of the supported HDMI source tests. For the tests that require multiple EDID files, more than one EDID files are listed in the table.

		EDID	DVI							
Test	Test Name	01.EDI	02.EDI	03.EDI	04.EDI	05.EDI	09.EDI	11.EDI	12.EDI	01.EDI
Source	e Protocol									
7-16	Legal Codes	•								
7-17	Basic Protocol	•								
7-18	Extended Control Period	•								
7-19	Packet Types	•		•						
Source	e Video									
7-23	Pixel Encoding. RGB to RGB-only Sink		٠						•	
7-24	Pixel Encoding. YCbCr to YCbCr Sink	•						•		
7-25	Video Format Timing	•								
7-26	Pixel Repetition	•								
7-27	AVI InfoFrame	•					•			
Source	e Audio									
7-28	Audio IEC Compliance	•		•						
7-29	ACR	•		•						
7-30	Audio Packet Jitter	•		٠						
7-31	Audio InfoFrame	•		٠						
7-32	Audio Layout	•		•						
Source	e Interoperability with DVI									
7-33	Interoperability with DVI	•	٠	•						•
Source	e Advanced Features									
7-34	Deep Color				•					
7-35	Gamut Metadata Transmission					•				

 Table 1
 HDMI Compliance Tests and Corresponding EDID Files (sheet 1 of 2)

* Where multiple EDIDs are listed, refer to "Using Multiple EDIDs for U4998A" on page 58.

 Table 2
 HDMI Compliance Tests and Corresponding EDID Files (sheet 2 of 2)

Test	Test Name	EDID01.EDI	EDID02.EDI	EDID06.EDI	EDID07.EDI	EDID08.EDI	EDID09.EDI	EDID10.EDI	EDID14.EDI	EDID15.EDI	EDID16.EDI	EDID17.EDI	EDID18.EDI	EDID19.EDI	EDID20.EDI
Source	e Advanced Features														
7-36	High Bitrate Audio			• as per HD MI CTS 1.4a	• as per HD MI CTS 1.4a					• as per HD MI CTS 1.4b	• as per HD MI CTS 1.4b	• as per HD MI CTS 1.4b	• as per HD MI CTS 1.4b		
7-37	One Bit Audio					• as per HD MI CTS 1.4a								• as per HD MI CTS 1.4b	• as per HD MI CTS 1.4b
7-38	3D Video Format Timing	•	•				٠								
7-39	4k X 2k Video Format Timing								•						
7-40	Extended Colorimetry							•							

* Where multiple EDIDs are listed, refer to "Using Multiple EDIDs for U4998A" on page 58.

EDID Files Corresponding to MHL Source Tests

The set of predefined EDID files for MHL are as per the requirements of MHL source tests. The following table lists the EDID files that are provided for each of the supported MHL source tests. For the tests that require multiple EDID files, more than one EDID files are listed in the table.

Test	Test Name	EDID01.EDI	EDID02.EDI	EDID03.EDI
3.2.2.1	Legal Codes	•		
3.2.2.2	Basic Protocol		•	
3.2.2.3	Packet Types			•
3.2.3.1	Video Format Timing	•		
3.2.3.2	Pixel Encoding		•	
3.2.3.3	AVI InfoFrame	• For YCb Cr out put	• For RG B out put	
3.2.3.4	Video Quantization	• For YCb Cr out put	• For RG B out put	
3.2.4.1	Audio Test IEC60958		•	
3.2.4.2	Audio Clock Regeneration		•	
3.2.4.3	Audio InfoFrame		•	

 Table 3
 MHL Compliance Tests and Corresponding EDID Files

Video Formats Supported by each EDID File

.

The following table lists the video formats supported by each EDID file.

Format	CEA Video ID Code	EDID01.EDI	EDID02.EDI	EDID03.EDI	EDID04.EDI	EDID05.EDI	EDID06.EDI	EDID07.EDI	EDID08.EDI	EDID09.EDI	EDID10.EDI	EDID11.EDI	EDID12.EDI	EDID14.EDI	DVI01.EDI
640 x 480 @ 59.94 / 60 Hz	1	•	•	•	•	•				•	•	•	•		
720 x 480 @ 59.94 / 60 Hz	2, 3	•	•	•	•	•				•	•	•	•		
720 x 480p @ 119.88 / 120 Hz	48, 49														
720 x 480p @ 239.76 / 240 Hz	56, 57														
720 x 576p @ 50Hz	17, 18	٠	•	•	•	•				•	•	•	•		
720 x 576p @ 100 Hz	42, 43														
720 x 576p @ 200 Hz	52, 53														
720 (1440) x 240p @ 59.94 / 60 Hz	8, 9														
720 (1440) x 288p @ 50 Hz	23, 24														
720 (1440) x 480i @ 119.88 / 120 Hz	50, 51														
720 (1440) x 480i @ 239.76 / 240 Hz	58, 59														
720 (1440) x 576i @ 100 Hz	44, 45														
720 (1440) × 576i @ 200 Hz	54, 55														
1280 x 720p @ 23.98 / 24 Hz	60														
1280 x 720p @ 25 Hz	61														
1280 x 720p @ 29.97 / 30 Hz	62														
1280 x 720p @ 50Hz	19	٠	•	•	•	•				•	•	•	•		
1280 x 720 @ 59.94 / 60 Hz	4	٠	•	•	•	•				•	•	•	•		
1280 x 720p @ 100 Hz	41														
1280 x 720p @ 119.88 / 120 Hz	47														
1440 x 480i @ 59.94 / 60 Hz	6, 7	•	•	•	•	•				•	•	•	•		
1440 x 480p @ 59.94 / 60 Hz	14, 15								•						
720 (1440) × 576i @ 50 Hz	21, 22	•	•	•	•	•				•	•	•	•		
1440 x 576p @ 50 Hz	29, 30								•						
1920 x 1080p @ 23.98 / 24 Hz	32									•	•				
1920 x 1080p @ 25 Hz	33														
1920 x 1080p @ 29.97 / 30 Hz	34														
1920 x 1080i @ 50 Hz	20	•	•	•	•	•				•	•	•	•		
1920 x 1080p @ 50 Hz	31	•	•	•	•	•				•	•	•	•		
1920 x 1080i @ 59.94 / 60 Hz	5	•	•	•	•	•				•	•	•	•		
1920 x 1080p @ 59.94 / 60 Hz	16	•	•	•	•	•				•	•	•	•		
1920 x 1080i (1250 total) @ 50 Hz	39														

Table 4 Video Format and Corresponding EDIDs (Sheet 1 of 2)

Format	CEA Video ID Code	EDID01.EDI	EDID02.EDI	EDID03.EDI	EDID04.EDI	EDID05.EDI	EDID06.EDI	EDID07.EDI	EDID08.EDI	EDID09.EDI	EDID10.EDI	EDID11.EDI	EDID12.EDI	EDID14.EDI	DVI01.EDI
1920 x 1080i @ 100 Hz	40														
1920 x 1080i @ 119.88 / 120 Hz	46														
2880 x 240p @ 59.94 / 60 Hz	12, 13														
2880 x 288p @ 50 Hz	27, 28														
2880 x 480i @ 59.94 / 60 Hz	10, 11														
2880 x 480p @ 59.94 / 60 Hz	35, 36						•	٠							
2880 x 576i @ 50 Hz	25, 26														
2880 x 576p @ 50 Hz	37, 38						•	٠							
3840 x 2160p @ 23.98/ 24,/25/ 29.97/ 30 Hz	H01, H02, H03													•	
4096 x 2160p @ 24 Hz	H04													•	

Table 4 Video Format and Corresponding EDIDs (Sheet 1 of 2)

Table 5Video Format and Corresponding EDIDs (Sheet 2 of 2)

Format	CEA Video ID Code	EDID15.EDI	EDID16.EDI	EDID17.EDI	EDID18.EDI	EDID19.EDI	EDID20.EDI
640 x 480 @ 59.94 / 60 Hz	1	٠		•		•	
720 x 480 @ 59.94 / 60 Hz	2, 3	•		•		•	
720 x 480p @ 119.88 / 120 Hz	48, 49		•		٠		٠
720 x 480p @ 239.76 / 240 Hz	56, 57						
720 x 576p @ 50Hz	17, 18	•		•		•	
720 x 576p @ 100 Hz	42, 43		٠		٠		٠
720 x 576p @ 200 Hz	52, 53						
720 (1440) x 240p @ 59.94 / 60 Hz	8, 9	•		•		•	
720 (1440) x 288p @ 50 Hz	23, 24	•		•		•	
720 (1440) x 480i @ 119.88 / 120 Hz	50, 51		•		٠		٠
720 (1440) x 480i @ 239.76 / 240 Hz	58, 59						
720 (1440) x 576i @ 100 Hz	44, 45		•		٠		٠
720 (1440) x 576i @ 200 Hz	54, 55						
1280 x 720p @ 23.98 / 24 Hz	60						
1280 x 720p @ 25 Hz	61						
1280 x 720p @ 29.97 / 30 Hz	62						
1280 x 720p @ 50Hz	19	•		•		•	
1280 x 720 @ 59.94 / 60 Hz	4	•		•		•	
1280 x 720p @ 100 Hz	41		•		٠		٠

Format	CEA Video ID Code	EDID15.EDI	EDID16.EDI	EDID17.EDI	EDID18.EDI	EDID19.EDI	EDID20.EDI
1280 x 720p @ 119.88 / 120 Hz	47		٠		٠		•
1440 x 480i @ 59.94 / 60 Hz	6, 7	•		•		•	
1440 x 480p @ 59.94 / 60 Hz	14, 15	•		•		•	
720 (1440) x 576i @ 50 Hz	21, 22	•		•		•	
1440 x 576p @ 50 Hz	29, 30	•		•		•	
1920 x 1080p @ 23.98 / 24 Hz	32		•		•		٠
1920 x 1080p @ 25 Hz	33		•		٠		٠
1920 x 1080p @ 29.97 / 30 Hz	34		٠		٠		٠
1920 x 1080i @ 50 Hz	20	•		٠		•	
1920 x 1080p @ 50 Hz	31	•		٠		•	
1920 x 1080i @ 59.94 / 60 Hz	5	•		٠		•	
1920 x 1080p @ 59.94 / 60 Hz	16	•		٠		•	
1920 x 1080i (1250 total) @ 50 Hz	39		٠		٠		٠
1920 x 1080i @ 100 Hz	40		٠		٠		٠
1920 x 1080i @ 119.88 / 120 Hz	46		٠		٠		٠
2880 x 240p @ 59.94 / 60 Hz	12, 13	•		٠		٠	
2880 x 288p @ 50 Hz	27, 28	•		٠		•	
2880 x 480i @ 59.94 / 60 Hz	10, 11	•		•		•	
2880 x 480p @ 59.94 / 60 Hz	35, 36		٠		٠		٠
2880 x 576i @ 50 Hz	25, 26	•		٠		٠	
2880 x 576p @ 50 Hz	37, 38		٠		٠		٠
3840 x 2160p @ 23.98/ 24,/25/ 29.97/ 30 Hz	H01, H02, H03						
4096 x 2160p @ 24 Hz	H04						

Contents of Predefined EDID Files

The following table lists the contents of each of the predefined EDID file.

 Table 6
 EDID File Contents

File Name	Formats	Video Data Block (VIC No)	Audio Data Block	Speaker Allocation Data Block	VSDB (Vendor Specific Data Block)	VCDB (Video Capability Data Block)	Colorimetry Data Block
EDID01.EDI	Basic Audio YCbCr 422/444	1, 2, 3, 4, 5, 6, 7, 16, 17, 18, 19, 20, 21, 22, 31	LPCM 2ch 48/44/32 kHz 16 bit		Length: 5		
EDID02.EDI	Basic Audio RGB	1, 2, 3, 4, 5, 6, 7, 16, 17, 18, 19, 20, 21, 22, 31	LPCM 2ch 48/44/32 kHz 16 bit		Length: 5		
EDID03.EDI	Basic Audio YCbCr 422/444	1, 2, 3, 4, 5, 6, 7, 16, 17, 18, 19, 20, 21, 22, 31	LPCM 8ch 192/176/96/88 /48/44/32 kHz 24/20/16 bit	RLC/RRC, FLC/FRC, RC, RL/RR, FC, LFE, FL/FR	Length: 6 Supports_AI = 1		
EDID04.EDI	Basic Audio YCbCr 422/444	1, 2, 3, 4, 5, 6, 7, 16, 17, 18, 19, 20, 21, 22, 31	LPCM 2ch 48/44/32 kHz 16 bit	FL/FR	Length: 7 Supports_AI = 1 DC_36 bit CD_Y444 [†] Max TMDS Clock: 225 MHz		
EDID05.EDI	Basic Audio YCbCr 422/444	1, 2, 3, 4, 5, 6, 7, 16, 17, 18, 19, 20, 21, 22, 31	LPCM 2ch 48/44/32 kHz 16 bit	FL/FR	Length: 7 Supports_AI = 1 DC_36 bit ^a CD_Y444 ^b Max TMDS Clock: 225 MHz		xyYCC709 xyYCC601 Metadata0
EDID06.EDI	Basic Audio YCbCr 422/444	35, 36, 37, 38	DTS=HD 2ch Byte 1: 0x59 192 (x4) kHz Byte 2: 0x40 Byte 3: 0x01		Length: 6 Supports_AI = 1		
EDID07.EDI	Basic Audio YCbCr 422/444	35, 36, 37, 38	MAT 2ch Byte 1: 0x61) 192/96/48 (x4) kHz Byte 2: 0x54 Byte 3: 0x00		Length: 6 Supports_AI = 1		

File Name	Formats	Video Data Block (VIC No)	Audio Data Block	Speaker Allocation Data Block	VSDB (Vendor Specific Data Block)	VCDB (Video Capability Data Block)	Colorimetry Data Block
EDID08.EDI	Basic Audio YCbCr 422/444	14, 15, 29, 30	One Bit Audio 8ch Byte 1: 0x40 44.1 kHz Byte 2: 0x02 Byte 3: 0x00		Length: 6 Supports_AI = 1		
EDID 09.EDI	Basic Audio YCbCr 422/444	1, 2, 3, 4, 5, 6, 7, 16, 17, 18, 19, 20, 21, 22, 31, 32	LPCM 2ch 48/44/32 kHz 16 bit	FL/FR	Length: 14 Supports_AI = 1 DC_36 bit ^a Max TMDS Clock: 225 MHz HDMI_Video _present: = 1 3D_present = 1 HDMI_VIC _LEN = 0 HDMI_3D _LEN = 0 CNC30 = 0,0,0,1		
EDID 10.EDI	Basic Audio YCbCr 422/444	1, 2, 3, 4, 5, 6, 7, 16, 17, 18, 19, 20, 21, 22, 31, 32	LPCM 2ch 48/44/32 kHz 16 bit	FL/FR	Length: 7 Supports_AI = 1 DC_36 bit ^a Max TMDS Clock: 225 MHz		AdobeRGB AdobeYCC601 sYCC601 xvYCC601 xvYCC709 Byte #3 = 0
EDID10a.EDI	Basic Audio YCbCr 422/444	1, 2, 3, 4, 5, 6, 7, 16, 17, 18, 19, 20, 21, 22, 31, 32	LPCM 2ch 48/44/32 kHz 16 bit	FL/FR	Length: 7 Supports_AI = 1 DC_36 bit ^a Max TMDS Clock: 225 MHz		Byte #3 = 0
EDID11.EDI	Basic Audio YCbCr 422/444	1, 2, 3, 4, 5, 6, 7, 16, 17, 18, 19, 20, 21, 22, 31	LPCM 2ch 48/44/32 kHz 16 bit		Length: 5	QY = 0 QS = 0	
EDID12.EDI	Basic Audio RGB	1, 2, 3, 4, 5, 6, 7, 16, 17, 18, 19, 20, 21, 22, 31	LPCM 2ch 48/44/32 kHz 16 bit		Length: 5	QY = 0 QS = 0	

3 Performing HDMI/MHL Compliance Testing for a Source Device

 Table 6
 EDID File Contents

File Name	Formats	Video Data Block (VIC No)	Audio Data Block	Speaker Allocation Data Block	VSDB (Vendor Specific Data Block)	VCDB (Video Capability Data Block)	Colorimetry Data Block
EDID13.EDI	Basic Audio YCbCr 422/444	1 through 62	LPCM 2ch 48/44/32 kHz 16 bit, 20 bit, 24 bit	FL/FR	Length: 26 A=1, B=0, C=0, D=0 Supports_AI = 1 DC_36 bit ^a Max TMDS Clock: 225 MHz CNC30 = 0,0,0,1 HDMI_Video _present: = 1 3D_present = 1,, 3D_Mult_present = 2 HDMI_VIC _LEN = 0 HDMI_3D _LEN = 16 3D_Structure_AL L = 0x01, 0x41 3D_MASK = 0x01, 0x12 Supports HDMI_14a primary 3D video formats		
EDID14.EDI	Basic Audio YCbCr 422/444	1, 2, 3, 4, 5, 6, 7, 16, 17, 18, 19, 20, 21, 22, 31, 32, 34, 60, 62	LPCM 2ch 48/44/32 kHz 16 bit, 20 bit, 24 bit	FL/FR	Length: 14 A=1, B=0, C=0, D=0 Supports_AI = 1 Max TMDS Clock: 300 MHz CNC30 = 0,0,0,1 HDMI_Video_pres ent = 1 3D_present = 1, 3D_Mult_present = 0 HDMI_VIC_Len =4, HDMI_3D_LEN = 0 HDMI_VIC_1, 2, 3, 4 Supports HDMI 1.4a primary 3D video formats		

File Name	Formats	Video Data Block (VIC No)	Audio Data Block	Speaker Allocation Data Block	VSDB (Vendor Specific Data Block)	VCDB (Video Capability Data Block)	Colorimetry Data Block
EDID15.EDI	Basic Audio YCbCr 422/444	1 to 31	DTS=HD 2ch Byte 1: 0x59 192 (x4) kHz Byte 2: 0x40 Byte 3: 0x01		Length: 6 Supports_AI = 1		
EDID16.EDI	Basic Audio YCbCr 422/444	32 to 51	DTS=HD 2ch Byte 1: 0x59 192 (x4) kHz Byte 2: 0x40 Byte 3: 0x01		Length: 6 Supports_AI = 1		
EDID17.EDI	Basic Audio YCbCr 422/444	1 to 31	MAT 2ch Byte 1: 0x61) 192/96/48 (x4) kHz Byte 2: 0x54 Byte 3: 0x00		Length: 6 Supports_AI = 1		
EDID18.EDI	Basic Audio YCbCr 422/444	32 to 51	MAT 2ch Byte 1: 0x61) 192/96/48 (x4) kHz Byte 2: 0x54 Byte 3: 0x00		Length: 6 Supports_AI = 1		
EDID19.EDI	Basic Audio YCbCr 422/444	1 to 31	One Bit Audio 8ch Byte 1: 0x40 44.1 kHz Byte 2: 0x02 Byte 3: 0x00		Length: 6 Supports_AI = 1		
EDID20.EDI	Basic Audio YCbCr 422/444	32 to 51	One Bit Audio 8ch Byte 1: 0x40 44.1 kHz Byte 2: 0x02 Byte 3: 0x00		Length: 6 Supports_AI = 1		
DVI01.EDI							

* Indicates support for RGB 4:4:4 at the specified pixel size.

† Indicates YCbCr 4:4:4 is supported for all modes indicated by DC_36 bit.

Setting up the EDID for U4998A

It is recommended to define the EDID block of U4998A before connecting it to the source DUT because the DUT reads the EDID block immediately after getting connected. However, if you want to define the EDID block of U4998A after connecting the two devices, then you need to use the **Hot Plug Detect -> Reset** button in the **Capture Setup** tab before starting the capture. Clicking Reset ensures that the DUT reads the updated EDID information while redoing the initialization tasks.

To define the EDID block of U4998A

- **1** Access the **Setup** dialog box for the HDMI module added in the Agilent Logic and Protocol Analyzer GUI.
- 2 Click the Capture Setup tab.
- **3** From the **EDID Setup** section, click the **EQU** button.
- **4** Browse to the location where you have stored the EDID file or browse to the location where the predefined EDID files are located.
- 5 Select the .edi file and click Open.
- 6 Click Apply and then OK.

Using Multiple EDIDs for U4998A

There are some source tests that require data to be captured and analyzed with multiple EDIDs. For such tests, you can change the EDID file set for U4998A and then click **Reset** in the **Capture Setup** tab to force DUT to read the updated EDID block. The following screen highlights this option.

Connection Setup	Capture Setup Frame Setup EDID Setup	
- Capture Setup		
Capture Memory Dep	128 ~ ~ [1-4096]MB	
Detected TMDS Cloc	k Comu	
Detected THDS Cloc	~ Hz Copy	
Hot Plug Detect (HPI	D) Reset	
LED Status	Refresh	
100 100 100 100		
Capture Mode		
Capture Storage -		
Increment file n	umber between captures, starting with 1 2 A Re	set
Capture File base	C:\HDMI\Inputs\Cap files\102210_105836.cap	Upload
-		
-EDID Setup		
-EDID Setup	an edd ela a colonad	
EDID Setup	No Edid File Is Selected	
EDID Setup	No Edid File Is Selected	E.
EDID Setup	No Edid File Is Selected	

Figure 17 Resetting the EDID file

The following table lists the broad steps for using the multiple EDIDs in the context of specific source tests that require multiple EDIDs as per specifications.

Test	Multiple EDID Files Usage
Test 7-19 Packet Types	Use the EDID files EDID01.edi and EDID03.edi.
	First use EDID file EDID03.edi, and run the test.
	Review the test results. If the source device transmitted an ACP, ISRC1, or ISRC2
	packet, use EDID file EDID01.edi and repeat the test.
Test 7-28 Audio IEC Compliance	Use the EDID files EDID01.edi and EDID03.edi.
	First use EDID file EDID03.edi. if the source device has the capability of outputting
	multi-channel audio. Else, use EDID01.edi.
Test 7-29, 7-30, 7-31, and 7-32	Use the EDID files EDID01.edi and EDID03.edi.
	Use EDID file EDID03.edi if the source device has the capability of outputting MAT
	audio. Else, use EDID01.edi.

Test	Multiple EDID Files Usage
Test 7-33 Interoperability with DVI	Use EDID files EDID01.edi, EDID02.edi, EDID03.edi, and DVI01.edi. According to the
	compliance test specification:
	- In step 1 of the specification, use EDID file DVI01.edi. This EDID configures the
	U4998A to appear as a DVI sink device.
	- In step 5, as the specification calls for an EDID that has an HDMI VSDB length of 5,
	use EDID01.edi (for YCbCr 422/444 color space) or EDID02.edi (for RGB color
	space). These two EDID files meet the required VSDB length.
	- In step 7, an EDID with a VSDB length greater than 5 is required. Use EDID03.edi.
Test 7-36 High Bitrate Audio	Use EDID files EDID06.edi and EDID07.edi.
	Use EDID file EDID06.edi, if source device has the capability of outputting DTD-HD
	audio. If source device has the capability of outputting MAT audio, use EDID07.edi.
Test 7-38 3D Video Format Timing	Use the EDID Files EDID09.edi and EDID01.edi or EDID02.edi.
	First, use the EDID file EDID09.edi and run the test.
	For the "Change HDMI VSDB in Protocol Analyzer to length = 5" step, use the
	EDID01.edi (for YCbCr 422/444 color space) or EDID02.edi (for RGB color space).
	These two EDID files meet the required VSDB length.

Starting the Data Capture

This topic describes how to start capturing the data received from an HDMI/MHL DUT.

Before you start the data capture, ensure that:

- the data capture setup is ready.
- the EDID block of U4998A is defined so that the DUT transmits as per the capabilities and configurations of U4998A. To ensure that the DUT reads the latest and updated EDID information, you can click Hot Plug Detect
 > Reset in the Capture Setup tab.
- the source DUT is connected to the HDMI IN Connector on the U4998A module. In case of an MHL DUT, it is connected to U4998A via the U4995A MHL adapter.
- the source DUT is switched on and configured to provide HDMI/MHL data output.
- the Logic and Protocol Analyzer GUI is in the online mode.

To start the data capture

- 1 Access the Logic and Protocol Analyzer GUI.
- 2 Click the **Run** toolbar button.

When you start the data capture, the captured data is stored in the memory of the U4998A module from where you can upload it into a specified .cap file.

The TMDS data channel LEDs for the HDMI IN connector on the front panel of U4998A module turns green indicating the start of capture. If the LEDs turn orange, it indicates the reception of data but the three TMDS data channels are not aligned. The LEDs turn red if non HDMI data is received.

The data capture stops:

- when you manually stop the data capture using the **Stop Acquisition** toolbar button in Logic and Protocol Analyzer.
- when the capture memory depth of U4998A module is full.

Uploading the Captured data in a File

Once the data capture is complete, you need to upload the captured data from the memory of U4998A to the .cap file that you specified in the Capture setup.

To upload data

- 1 Access the **Setup** dialog box for the HDMI module in the Logic and Protocol Analyzer GUI.
- 2 Click the Capture Setup tab.
- 3 Click Upload displayed with the Capture file base field.

If you have selected the **Increment File number between Captures** option in the **Capture setup** tab, then clicking **Upload** creates a new .cap file appended with the applicable incremented number. All the data that exist at that time in the memory of U4998A is uploaded in this new file.

If you have not selected the **Increment File number between Captures** option in the **Capture setup** tab, then clicking **Upload** overwrites the specified .cap file with the data that exist at that time in the memory of U4998A.

Monitoring the Transmitted Data on a Connected Sink Device

While testing a source DUT, there may be situations when you also want to display the data that the source DUT transmits to U4998A besides capturing this data. There may also be some DUTs that have only HDMI output.

To accomplish this, you need to:

- Configure the U4998A Connection mode as **Mirror**. You need U4998A-PSV or U4998U-PSV license to use this mode.
- Connect the source DUT to the HDMI IN connector of U4998A.
- Connect a sink device to the HDMI OUT connector of U4998A. The sink device is then used as a medium for displaying the data transmitted by the source DUT to U4998A.

The rest of the steps remain the same as described for testing a source device in the "Overview topic.

Evaluating the Captured Data for Compliance to HDMI/MHL CTS

When you have uploaded the captured data in the specified .cap file, you can run various HDMI/MHL source compliance tests on the data stored in this file. You do not need connectivity to U4998A or DUT while doing the compliance evaluation.

You use the **HDMI/MHL Protocol Analyzer** GUI to run the supported source compliance tests on the captured HDMI/MHL data. This GUI is installed when you install the HDMI/MHL Evaluator software. In this GUI, you use the **U4998A** tab when using the U4998A module for data capture. The other tab **N5998A** is not applicable for use with U4998A and is used with the Agilent N5998A hardware. For all other HDMI/MHL testing tasks except the offline evaluation of the captured data, you use the Logic and Protocol Analyzer GUI.

The following screens displays the U4998A tab in the HDMI/MHL Protocol Analyzer GUI.

🚏 HDMI / MHL Protocol	Analyzer : Version 2.10.1005			
U4998A N5998A				
Incontract				
HDMI Evaluator MHL E	valuator			
		Video Format Tin		
Target File Name	C:\Inputs\Cap files\102210_105836.cap File Open	1 : 640×480p.0		
		1.0100100000		
Log type		Select Test ID		
By frame By Source Source Sour		Full HDMI Com		
	Test ID 7-25 : Video Format Timing	Expert M		
O By test case				
	 Verify that no AVI InfoFrame is transmitted. 	Protocol		
# Frame1	Error : 1 AVI InfoFrame Packet(s) exist(s).	🖸 HDMI		
# Frame2	Dividual and a should be within all succession			
E-Frame3	Pixel clock should be within allowable range.	Color Format		
710	Error . Pixel clock is out of allowable range.	XVYCC		
710	HSYNC//SYNC notarity should be equal to penative/penative	C YCbCr(4:		
710	719 Pass			
725				
725	Number of pixel clocks that HSYNC remains active should be 96.0 (HS_LEN)			
728	Pass	Color Depth -		
-729		🖸 24 bits		
-730	Number of pixel clocks from end of Video Data Period to HSYNC active edge s	C 36 bits		
- 731	Pass			
-732	Number of nivel clocks in Video Data Period minus 2 (for Guard Band) should	Quantization I		
Frame4	Pass	C Limited R.		
Frame5		C Limited R		
🗄 Frame6	Number of pixel clocks between two HSYNC active edges should be 800.0 (H_			
🗄 Frame7	Pass	Content Type		
🗄 Frame8		No Data		
# Frame9	Number of lines that VSYNC remains active should be 2 (VS_LEN)	C Graphics		
# Frame10	Pass	C Photo		
Frame11	Number of Video Data Bariada between each two VOVNC estive addee about			
🗄 Frame12	Pace	Options		
# Frame13	1 400	AVI InfoF		
Frame14	Number of pixel clocks between VSYNC active edges divided by H TOTAL sho	Audio		
B-Frame15	Pass	ACP, ISR		
# Frame16		🗌 🗍 3D Video		
E Framel /	Number of HSYNC pulses from VSYNC active edge to Video Data Period shou	C Frame		
# Frameto	Pass			

As displayed in the above screen, the U4998A tab contains the following two tabs:

• **HDMI Evaluator** - You use this tab to run HDMI compliance tests on the captured data received from a source HDMI DUT. You can run either full HDMI compliance tests or a specific HDMI CTS source test on the data in the .cap file.

• **MHL Evaluator** - You use this tab to run MHL compliance tests on the captured data received from a source MHL DUT. You can run either full MHL compliance tests or a specific MHL CTS source test on the data in the .cap file.

Refer to the AXIe Based Logic Analysis and Protocol Test Modules Installation guide to know how to install the HDMI/MHL Evaluator software. This guide is available on www.agilent.com.

Passed and Failed Tests

When you run a source test on a .cap file, the frames in the .cap file are evaluated and the test status (Pass/Fail) is displayed for each frame. The failed tests are displayed in red.

The following screen displays Full HDMI Compliance test results in the HDMI/MHL Evaluator GUI.

🕫 HDMI / MHL Protocol	Analyzer : Version 2.10.1005	
U4998A N5998A		
HDMI Evaluator MHL E	valuator	
		Video Format Tir
Target File Name	C:\Inputs\Cap files\102210_105836.cap File Open	1 : 640x480p (
-Log type		Select Test ID
Log type		Full HDMI Com
By frame	 Test ID 7-25 : Video Format Timing	
C By test case	rescib 7-25. Video Format Liming	Expert M
	- Verify that no AVI InfoFrame is transmitted.	-Protocol
⊞-Frame1	Error : 1 AVI InfoFrame Packet(s) exist(s).	🖸 HDMI
⊯ Frame2		
🖹 Frame3	Pixel clock should be within allowable range.	Color Format
-716	Error : Pixel clock is out of allowable range.	XVYCC
710	HSYNC/VSYNC notarity should be equal to penative/penative	C YCbCr(4:
710	Pass	C YCbCr(4;
725		
-726	Number of pixel clocks that HSYNC remains active should be 96.0 (HS_LEN)	
728	Pass	Color Depth -
- 729	Number of size blocks from and of Video Date Deviad to UOVNO estiva advant	🖸 24 bits
- 730	Number of pixel clocks from end of video Data Penod to HSYNC active edge si	C 36 bits
- 731	1 435	
732	Number of pixel clocks in Video Data Period minus 2 (for Guard Band) should	Quantization
Frame4	Pass	🐑 Limited R.
⊞ Frame5		C Limited R
⊞ Frame6	Number of pixel clocks between two HSYNC active edges should be 800.0 (H_	
H Frame /	Pass	C No Data
Erame9	Number of lines that VSYNC remains active should be 2 (VS_LEN)	C Graphics
#-Frame10	Pass	Caraphics
B Frame11		O Photo
⊮ Frame12	Number of Video Data Periods between each two VSYNC active edges should	Options
⊯ Frame13	Pass	AVI InfoF
🗷 Frame14	Number of nivel clocks between VSYNC active addres divided by H_TOTAL she	🗌 Audio
⊞ Frame15	Pass	ACP, ISR
⊯ Frame16		T 3D Video
B Frame17 B Frame18	Number of HSYNC pulses from VSYNC active edge to Video Data Period shou Pass	C Frame

Figure 18 Failed source test in HDMI/MHL Evaluator

🕫 HDMI / MHL Protocol /	Analyzer : Version 2.10.1005			
U4998A N5998A				
HDMI Evaluator MHL Ev	aluator			
		r	Video Format Timing	
Target File Name	C:\Inputs\Cap files\102210_105836.cap	File Open	1 : 640x480p @ 59.9	4Hz
-Log type			- Select Test ID	Exp
G n (Full HDMI Compliance	
 By trame By test case 	 Test ID 7-19 : Packet Types		Expert Mode Se	elect Test II
	8 NULL Packet		Protocol	
Frame1	0 ACR Packet		C HDMI	C DVI
# Frame2	0 Audio Sample Packet			
E-Frame3	1 General Control Packet		Color Format	-
710	0 ISBC1 Packet		XVYCC	🖲 RGB
719	0 ISRC2 Packet		C YCbCr(4:2:2)	C Adobr
710	0 One Bit Audio Sample Packet		C YCbCr(4:4:4)	C Adob
725	0 DST Audio Packet			C sycci
726	0 High Bitrate(HBR) Audio Stream Packet			
728	0 Gamut Metadata Packet		Color Depth	_
-729	U Vendor Specific InfoFrame Packet		24 bits	C 30 bit
- 730	0 Source Product Description InfoFrame Packet		🔿 36 bits	C 48 bit
- 731	0 Audio InfoFrame Packet		- Ouestization Range	
732	0 MPEG Source InfoFrame Packet		Quantization Range	
⊞ Frame4			Climited Range C	R Full Rang
H Frames	Test ID 7-19 : PASS		C Limited Range	C Full R

Figure 19 Passed source test in HDMI/MHL Evaluator

Supported HDMI Source Tests

All the source tests except 7-1 till 7-15 and 7-20 till 7-22 are supported in this release.

The following table lists the supported source tests and the settings that you need to do for each of these tests in the HDMI/MHL Evaluator GUI.

	Table 7	Supported HDMI Source	Tests
--	---------	-----------------------	-------

		E	ut	Setting	ıs Availa	ble in HC	DMI/MH	L Evalua	tor GUI
Test ID	Test Name	Included in Full Compliance Evaluatic	Requires Measureme of TMDS Clock	Protocol	Color Format	Color Depth	Quantization Range	Content Type	Options
Source P	rotocol								
7-16	Legal Codes	•							•
7-17	Basic Protocol	•							•
7-18	Extended Control Period	•							•
7-19	Packet Types	•							•
Source V	ideo								
7-23	Pixel Encoding. RGB to RGB-only Sink				•				•
7-24	Pixel Encoding. YCbCr to YCbCr Sink				•				•
7-25	Video Format Timing	•	•						•
7-26	Pixel Repetition	•							•
7-27	AVI InfoFrame				•			•	•
Source A	udio								
7-28	Audio IEC Compliance	•							•
7-29	ACR	•	•						•
7-30	Audio Packet Jitter	•							•
7-31	Audio InfoFrame	•							•
7-32	Audio Layout	•							•
Source In	teroperability with DVI								
7-33	Interoperability with DVI			•					•
Source Advanced Features									
7-34	Deep Color		•		•	•			•
7-35	Gamut Metadata Transmission								•
7-36	High Bitrate Audio								•
7-37	One Bit Audio								•
7-38	3D Video Format Timing		•		•			•	•
7-39	4K X 2K Video Format Timing								•
7-40	Extended Colorimetry				•		•	•	•

Supported MHL Source Tests

The following table lists the supported MHL source tests and the settings that you need to do for each of these tests in the HDMI/MHL Evaluator GUI.

Table 8	Supported	MHL	Source	Tests

				Settings Available in HDMI/MHL Evaluator GUI		
Test ID	Test Name	Included in Full MHL Compliance Evaluation	Requires Measurement of MHL 3X Clock (Hz)	Color Format	YCC Quantization Range	Options
3.2.2.1	Legal Codes	•				
3.2.2.2	Basic Protocol	•				
3.2.2.3	Packet Types	•				
3.2.3.1	Video Format Timing	•	•			•
3.2.3.2	Pixel Encoding			•		
3.2.3.3	AVI InfoFrame	•		•		•
3.2.3.4	Video Quantization			•	•	•
3.2.4.1	Audio Test IEC60958	•				•
3.2.4.2	Audio Clock Regeneration	•	•			•
3.2.4.3	Audio InfoFrame	•				•

Starting the Evaluation of Captured Data

NOTE

You can use only the U4998A tab in the HDMI/MHL Evaluator GUI when working with U4998A. The other tab N5998A in this GUI is not applicable for use with U4998A and is used with the Agilent N5998A hardware. For all other HDMI/MHL testing tasks except the offline evaluation of the captured data, you use the Agilent Logic and Protocol Analyzer GUI.

- 1 Access the HDM/MHLI Evaluator GUI by clicking **Start** > **Programs** > **HDMI Evaluator** > **HDMI Evaluator** option on the Windows task bar.
- 2 Click the U4998A tab.
- **3** To run HDMI source tests, click the **HDMI Evaluator** tab. To run MHL source tests, click the **MHL Evaluator** tab.

- 4 Click **File Open** to open a captured HDMI/MHL data file (.cap file).
- **5** From the **Video Format Timing** listbox, select the Video Format Timing applicable for the data in the .cap file.
- **6** From the **Select Test ID** listbox, select the source test that you want to run. You can:
 - either select the Full Compliance option to run full HDMI/MHL CTS tests on the data in the .cap file. Refer to "Supported HDMI Source Tests" on page 68 and "Supported MHL Source Tests" on page 70 to get a list of source tests included in the Full HDMI Compliance and Full MHL Compliance options.
 - or a specific HDMI/MHL CTS source test on the data in the .cap file.
- 7 When running HDMI tests, enter the TMDS clock frequency, if enabled for the selected HDMI test. When running MHL tests, enter the MHL 3x clock frequency, if enabled for the selected MHL test.
- 8 For each source test, you need to specify the values for the expected parameters. These parameters are available as editable field in the HDMI Evaluator and MHL Evaluator tabs when you select a test. The actual parameter values are stored in the .cap file. Based on the actual and expected values, the test results are derived and displayed. Refer to "Supported HDMI Source Tests" on page 68 and "Supported MHL Source Tests" on page 70 to get a list of parameters/settings applicable for each source test.
- 9 While running some tests, you need to specify the detected TMDS Clock frequency. For such tests, you can use the Copy button displayed with the Detected TMDS Clock field in the Capture Setup tab of Logic and Protocol Analyzer GUI to copy the currently detected TMDS clock frequency and paste it in the TMDS Clock(Hz) field in the HDMI/MHL Evaluator GUI.

10 Click Start.

When you click Start, the selected tests are run on each frame repeatedly from the beginning of the first complete frame in the captured file. As captured data usually begins in the middle of a frame, the data in the beginning incomplete frame is not tested. Frames are defined as starting from the first pixel of the vertical blanking. For Test ID 7-29, 7-30, 7-36, and 7-37, the target .cap file must have the HDMI data for more than 2 seconds.

NOTE

You can select the **Expert Mode** checkbox to get complete control on which tests to run on the captured data. As the name implies, this feature is not required for normal testing but is provided for troubleshooting and experimenting by advanced users. Selecting this checkbox enables the **Expert Mode Select Test ID(s)** button which you can use to select the tests to run.

Viewing Test Results

On running a test, the test results are displayed in the Test Results pane of the HDMI Evaluator/MHL Evaluator tab.

The following screen displays the results of a test.

🕫 HDMI / MHL Protocol	Analyzer : Version 2.10.1005			
U4998A N5998A				
HDMI Evaluator MHL E	valuator			
,			, Video Format Timing	
Target File Name	C:\Inputs\Cap files\102210_105836.cap F	ïle Open	1:640×480p @ 59.9	94Hz
-Log type			– Select Test ID	Exp
G. Du fuene			Full HDMI Compliance	•
G By test case	Test ID 7-19 : Packet Types		Expert Mode S	elect Test I
	8 NULL Packet		Protocol	
	0 ACR Packet		C HDMI	C DVI
B-Frame2	0 Audio Sample Packet			
E-rrames	1 General Control Packet		Color Format	
717	0 ISRC1 Packet		XVYCC	💌 RGB
-718	0 ISRC2 Packet		C YCbCr(4:2:2)	C Adob
719	0 One Bit Audio Sample Packet		U YCDCr(4;4;4)	C Adob
-725	0 DST Audio Packet			C sycc
- 726	0 High Bitrate(HBR) Audio Stream Packet		- Color Depth	
- 728	0 Garriul Melauala Packel 0 Vendor Specific InfoErame Packet		Color Depart	Contra
- 729	1 AVI InfoFrame Packet		Ve 24 bits	U SU bit
- 730	0 Source Product Description InfoFrame Packet		C 36 bits	C 48 bit
- 731	0 Audio InfoFrame Packet		- Ouantization Range	
TJZ	0 MPEG Source InfoFrame Packet		C Limited Range C	DR Eull Rapi
Frame5	Test ID 7-19 - PASS		C Limited Range	C Eullo
	Testilo (*13.1 Add		Cumiceu Range	€ Full K

Use the Navigator pane on the left to jump to specific sections in the Test Results pane. In the Navigator pane, double click either a test or a frame to jump to the corresponding data for that test or frame in the Test Results pane. The following color convention is followed:

- A green colored test or frame label indicates a pass condition.
- A red colored label represents a failure
- A yellow colored label represents a skipped item.

Test numbers shown in the Navigator pane do not include the hyphen character. For example, test 7-16 is listed as 716.

Use the Log Type selections at any time to change the organization of the Navigator pane between tests and frames.

Test Data Log File

When you click Start to run a test, all the information shown in the window's Test Results pane is saved to a text log file. This file is saved in the same folder as the captured data file. The name of the file is formed using the current year, month, day, hour, minute, and second as in yyyymmddHHMMSS.txt. For example, 20091023163205.txt.

Packet Log File

If you select Full HDMI Compliance or (7-19) Packet Types, a log of data packets is saved to a text packet log file. Click **Packet LOG** in the HDMI Evaluator tab and select the types of packets that you want recorded. This log file is saved in the same folder as the captured data file. The name of the file is formed using the current year, month, day, hour, minute, and second as in logPacketyyyymmddHHMMSS.txt. For example, logPacket20091023163205.txt.





Viewing the Video Image

When you run test 7-23, 7-24, 7-27, 7-34, 7-38, or 7-40, a video Image window appears for every frame. This window allows you to visually inspect the video. The following figure shows the Image window for tests 23 and 24. The windows for tests 27 and 34 are very similar. For each displayed image, confirm the integrity of the image. Then click NEXT Frame or Finish.


Data File

Figure 21 Video Image Window for Test 23 and Test 24

In the Image window, you can specify the period of the pixel you are interested in. Select Video Data Period for video period only or Total Period for all the periods. You can also specify the coordinate of the pixel. The data of the three channels are decoded and displayed as binary value, and the data period is displayed as well.

Saved Image Files

When you click NEXT, the video image is saved to a file (bmp format). The file is saved to the same folder as the captured data file. The picture file's name is comprised of the name of the captured data file, an index number for the image, and the current year, month, day, hour, minute, and second. For example, it the first image was named,

VIC034_RGB_8Bit_30Hz_0_20091023163205.bmp

the second image could be named VIC034_RGB_8Bit_30Hz_1_20091023163257.bmp

Saved Decoded Data File

Click Export to File to save a text file (.txt) that has all of the decoded data of the frame by pixel index. The files is saved to the same folder as the captured data file. The file is given the same name as the captured data file with "_Frame_x" appended, where the x stands for the frame number. For example, if the captured data file is named

VIC034_RGB_8Bit_30Hz.cap

the text file for the first frame will be named VIC034_RGB_8Bit_30Hz_Frame_1.txt

Tests 7-23 and 7-24

The video image is decoded according to the color format selected in the HDMI Evaluator window. The saved graphics file is created according to the aspect ratio and size of the captured frame.

Test 7-27

The video image is decoded according to AVI InfoFrame Packet. The video image window will not appear if the Video Format Timing selection doesn't match the video format timing of the data file. The saved graphics file is created according to the aspect ratio and size of the captured frame. When video image window appears, you can change the aspect ratio of video image by clicking 4:3 or 16:9.

Test 7-34

The video image is decoded by the color format selected in the HDMI Evaluator window. The video image window will not appear if:

- the Color Depth selection doesn't match the color depth of data file.
- the Video Format Timing selection doesn't match the video format timing of the data file

For 30-bit color depth, the TMDS clock frequency should be 33.75 MHz. For 36-bit color depth, the TMDS Clock frequency should be 40.5 MHz, which is $1.5 \ge 27$ MHz. For 48-bit color depth, the TMDS Clock frequency should be 54 MHz, which is $2 \ge 27$ MHz.

The saved graphics file is created according to the aspect ratio and size of the captured frame.

Audio Jitter

When tests 7-30, 7-36, 7-37, or Full HDMI Compliance are performed, the result of audio jitter appear every two seconds. In case of video format 720 x 480p at 60/59.94Hz, the result of audio jitter appears on every 120 frames. For other formats:

- 1920 x 1080i at 60/59.94 Hz: Every 60 frames
- 720 x 576p at 50 Hz: Every 100 frames
- 1920 x 1080i at 50 Hz: Every 50 frames

Importing Captured Data into Agilent Logic and Protocol Analyzer for further Analysis

You can debug and perform deeper analysis on the captured data by importing the captured data into Agilent Logic and Protocol Analyzer GUI. The captured data is stored in a specified .cap file. You can convert the .cap file into a Module CSV (Comma Separated Values) file. You can then import this Module CSV file in Agilent Logic and Protocol Analyzer GUI as a data import module to analyze the data.

You use the **Generate CSV** utility to convert a .cap file to a module CSV file. Refer to the *AXIe Based Logic Analysis and Protocol Test Modules Installation guide* (available on www.agilent.com) to know about the installation of this utility. You can use this utility if you have the required software license. You can obtain a software license for this utility by clicking the **Software Licensing** button in the Generate Module CSV dialog box.

The following screen displays the dialog box for this utility.

🤠 Generate Mod	ule CSV from HDMI Cap	ture File : Version 1.42.1	002	_ 🗆 🛛				
Input file name:	C:\HDMI\Inputs\Cap files\10	2210_105836.cap		Browse				
Output file name:	C:\HDMI\Inputs\Cap files\csv files\102210_105836.csv Browse							
TMDS Clock (Hz)	2500000	Start Point	End Point					
		 Beginning of Trace 	O End of Trace					
		O First Frame	⊙ Number of Frame:	; 100				
Software Licen	ising	Generat	e Output File	Exit				

Figure 22 Generate CSV Utility

NOTE

You do not need the Agilent Logic Analyzer hardware or U4998A hardware to use this utility.

While performing conversion of a .cap file to a module CSV file, you have the option of converting the entire .cap file or specific frames from the .cap file to a module CSV file. If you want to inspect and debug specific frames, then it is recommended to specify only those frame numbers while conversion to reduce the conversion time and the CSV file size.

Converting a .cap file to a module CSV file

1 Click Start > Programs > HDMI Evaluator > Generate CSV option on the Windows task bar.

The Generate Module CSV from HDMI Capture File dialog box is displayed.

- 2 In the **Input file name** field, specify the name and location of the .cap file that you want to convert.
- **3** In the **Output file name** field, specify the name and location where you want the utility to store the converted module CSV file.
- **4** In the **TMDS Clock (Hz)** field, specify the TMDS clock frequency applicable for the data captured in the specified .cap file. The conversion utility uses this frequency value to generate timestamps for display of the data in different views in Agilent Logic and Protocol Analyzer GUI. It is recommended that you specify the value of this field based on the frequency value displayed in the **Detected TMDS Clock** field in the Capture Setup tab of Logic and Protocol Analyzer GUI. By doing this, you can ensure that correct timestamps are generated for the captured data which may be useful in some debugging scenarios.
- **5** In the **Start point** section, select the start point in the .cap file from where the conversion of captured data should start. You can either start the conversion of captured data from the start of trace or from a specific frame number.
- **6** In the **End point** section, select the end point in the .cap file at which you want to stop the conversion of the captured data. You can instruct the conversion to be done either till the end of trace or till the number of specified frames from the start point.

NOTE	To properly evaluate an interlaced frame, always include the frame before and after the desired frame in the conversion. For example, to analyzer frame 86, specify frame 85 as the first frame and 3 as the Number of frames to include frame 87 also in the conversion. For each extra frame that you wish to convert, add 2 to the number you specify in the Number of Frames field.
	If you're converting only one frame, specify 2 in the Number of Frames field. Entering 1 would only convert half of the frame.
	7 Click Generate Output File.
NOTE	When an entire .cap file is converted, conversion time can be quite long and requires up to 25 GB of free space on the computer's hard drive. Although the application may appear to stall, an hour glass indicates that the conversion is still progressing.

The module CSV file is created at the specified location.

Importing the Module CSV file into Logic and Protocol Analyzer GUI

- **1** Access the Agilent Logic and Protocol Analyzer GUI in offline or online mode.
- 2 Click File > Import.

The Import dialog box is displayed.

- 3 Select the Module CSV Text File option and click OK.
- **4** Specify the name and location of the Module CSV file that you want to import.
- 5 Click Import.

A Data Import module is added in the Overview window of Logic and Protocol Analyzer GUI. The specified module CSV file is loaded in this module.



Figure 23 Data import module in Logic and Protocol Analyzer

For viewing and analyzing the data in the CSV file, you can add data viewing and analysis tools available in Logic and Protocol Analyzer such as Waveform View and Listing View. Refer to the topic "Viewing the Converted Data in Logic and Protocol Analyzer" on page 90 to know more.

These views allow you to navigate using markers and Zoom in /Zoom out features. In these views, you can locate a frame that you want to inspect and mark that frame by clicking the Markers > New option.

New Marker	X
Name Frame 189	OK Cancel
Comments	

Figure 24 New Marker Dialog Box

Drag the marker to the beginning of the frame as shown in the following figure. The beginning of a frame occurs at the last falling edge of the VDP to precede a Vsync. When the cursor gets close to the falling edge of VDP, it snaps to the edge.



Figure 25 Dragging a Marker Onto a Frame

Using these markers, you can view a specific frame in the Listing View of Logic and Protocol Analyzer. Right click anywhere in the Listing view and select the frame you wish to view.

And and the second of the second se	and the second s	and the second s
10.005845117 ms		
10.005858585 ms		
10.005872053 ms		
10.005885521 ms		
10.005898989 ms	Undo	
10.005912457 ms		
10.005925925 ms	GO 10 🕨	Time
10.005939393 ms	Go To Beginning Of Data	Sample
10.005952861 ms	Go To End Of Data	Frame 190
10.005966329 ms	Place Marker	Frame 189
10.005979797 ms		Frame 188
10.005993265 ms	Find	M1
10.006006733 ms	Find Next	M2
10.006020201 ms	Find Previous	MZ
10.006033669 ms		Trigger
10.006047137 ms	Properties	More
10.006060605 ms		
10.006074073 ms		
10.006087541 ms		
10.006101009 ms		
10.006114477 ms		and the second second



From the sample line where the frame begins, move forward through pixels to get to the line you want. Use the ratio of pixels-per-line that is appropriate to your format. For example, to reach the beginning of line 2, move forward 2200 pixels (there are 2200 pixel-per-line). Therefore, add 2200 to the current sample #, 2473085, and get 2475285. Click Go To > Sample and enter 745149 to view line 2.

A pixel is marked the same way as a line. Go to the beginning of the line you want. Then, move forward to the pixel number you want.

Determining Frame Numbers in the Converted CSV File

If you want to inspect a specific frame, the following section describes how to determine the number of that frame in the converted CSV file.

Progressive formatted data

For progressive formatted video data, finding a frame in the converted CSV file is simple because there is a direct correspondence between frame numbers in the captured and converted data files.

Interlaced formatted data

For interlaced formatted data, there are two converted frames for each frame in the .cap file. Therefore, the frame numbers in the captured and converted data files no longer correspond and you need to calculate the frame numbers for viewing frames in the converted file as described below.

- 1 In a text editor, open the test evaluation log file that corresponds to the .cap file. This .txt file is created in the same folder as the .cap file when you run evaluation on the .cap file using HDMI Evaluator.
- **2** At the top of the file, locate the number of pixels discarded as shown in the following figure. This is the pixel offset for the first frame.



Figure 27 Pixel Offset to First Frame

3 Locate any frame in the log file. At the end of the listing for the frame, a line lists how many pixels were discarded. This value is the number of pixel-per-frame as shown in the following figure.

	File Edit Format View Help
Start of Frame Information	Frame No = 1 Test ID 7-16 : Legal Codes
	Video Data Code Disparity Check : OK
	Control Period codes : OK
	TERC4 codes : OK
	Data Island Guard Band : OK
	Video Guard Band : OK
	Test ID 7-16 : PASS
Pixels in Frame	2475000 pixel(s) was/were discarded.

Figure 28 Pixels-Per-Frame Value

4 If the pixel offset to frame 1 is less than half of the pixels-per-frame, use the following equation to determine the number to enter into the First Frame field:

$$F_{\text{converted file}} = (F_{\text{data file}} \times 2) - 1$$

where $F_{data file}$ is the frame number in the captured data file that you want to inspect. $F_{converted file}$ is the corresponding frame in the converted CSV data file. For example, if you wanted to inspect the frame corresponding to frame 189 in the captured data file, you would need to view frame 377 in the converted data file.

5 If the pixel offset to frame 1 is greater than half of the pixels-per-frame, use the following equation to determine the number to enter into the First Frame field:

$$F_{\text{converted file}} = (F_{\text{data file}} \times 2)$$

where $F_{data file}$ is the frame number captured data file that you want to inspect. $F_{converted file}$ is the corresponding frame in the converted CSV data file. To inspect the frame corresponding to frame 189 in the captured data file, you would need to view frame 378 in the converted data file.

Locating Errors in the Converted CSV File

This topic describes how you can identify the precise pixel where an error occurs in a converted CSV file for inspection and analysis.

To identify an error location:

- 1 Open the test log (.txt file) that corresponds to the converted file. This .txt file is created in the same folder as the .cap file when you run evaluation on the .cap file using HDMI Evaluator.
- **2** Within the log file, identify the location of errors by the frame, line, and pixel as shown in the following figure. In



this figure, the first error is located in Frame 189, Line 924, at pixel 413.

Figure 29 Error Pixel and Line Locations in Log File

3 Use the following equation to locate the corresponding pixel where the error occurs within the converted data file. The equation is valid for both progressive and interlaced formats.

$$Pixel = F_{first} + (F_{error} - 1)(pixels/frame) + (L_{error} - 1)(pixels/line) + (P_{error} - 1)$$

Where:

 F_{first} is pixel offset to the first frame. At the *top* of the log file, locate the number of pixels discarded as shown in Figure 30. This is the pixel offset for the first frame.





 F_{error} is number of the frame that contains the error. L_{error} is the line number of the error.

 P_{error} is the pixel where the error occurs. The pixel location of the error can be off a few pixels due to pixel errors in the data.

pixels/frame is listed at the *end* of a frame section in the log. It is noted as the number of discarded pixels. Refer the following figure.



Figure 31 Pixels-Per-Frame Value

pixels/line is listed in Table 9 on page 88 for each video code. Pixels-per-line is not recorded in the log file.

CEA Video ID Code	Format	Pixels/Line
1	640 x 480 @ 59.94 / 60 Hz	800
2, 3	720 x 480 @ 59.94 / 60 Hz	858
4	1280 x 720 @ 59.94 / 60 Hz	1650
5	1920 x 1080i @ 59.94 / 60 Hz	2200
6, 7	1440 x 480i @ 59.94 / 60 Hz	1716
8, 9	720 (1440) x 240p @ 59.94 / 60 Hz	1716
10, 11	2880 x 480i @ 59.94 / 60 Hz	3432
12, 13	2880 x 240p @ 59.94 / 60 Hz	3432
14, 15	1440 x 480p @ 59.94 / 60 Hz	1716
16	1920 x 1080p @ 59.94 / 60 Hz	2200
17, 18	720 x 576p @ 50Hz	864
19	1280 x 720p @ 50Hz	1980
20	1920 x 1080i @ 50 Hz	2640
21, 22	1440 x 576i @ 50 Hz	1728
23, 24	720 (1440) x 288p @ 50 Hz	1728
25, 26	2880 x 576i @ 50 Hz	3456
27, 28	2880 x 288p @ 50 Hz	3456
29, 30	1440 x 576p @ 50 Hz	1728
31	1920 x 1080p @ 50 Hz	2640
32	1920 x 1080p @ 23.98 / 24 Hz	2750
33	1920 x 1080p @ 25 Hz	2640
34	1920 x 1080p @ 29.97 / 30 Hz	2200
35, 36	2880 x 480p @ 59.94 / 60 Hz	3432
37, 38	2880 x 576p @ 50 Hz	3456
39	1920 x 1080i (1250 total) @ 50 Hz	2304
40	1920 x 1080i @ 100 Hz	2640
41	1280 x 720p @ 100 Hz	1980
42, 43	720 x 576p @ 100 Hz	864
44, 45	720 (1440) x 576i @ 100 Hz	1728
46	1920 x 1080i @ 119.88 / 120 Hz	2200
47	1280 x 720p @ 119.88 / 120 Hz	1650
48, 49	720 x 480p @ 119.88 / 120 Hz	858
50, 51	720 (1440) x 480i @ 119.88 / 120 Hz	1716
52, 53	720 x 576p @ 200 Hz	864
54, 55	720 (1440) x 576i @ 200 Hz	1728
56, 57	720 x 480p @ 239.76 / 240 Hz	858
58, 59	720 (1440) x 480i @ 239.76 / 240 Hz	1716

 Table 9
 Pixels/Line per VIC (Sheet 1 of 2)

CEA Video ID Code	Format	Pixels/Line
60	1280 x 720p @ 23.98 / 24 Hz	3300
61	1280 x 720p @ 25 Hz	3960
62	1280 x 720p @ 29.97 / 30 Hz	3300

 Table 9
 Pixels/Line per VIC (Sheet 2 of 2)

Viewing the Converted Data in Logic and Protocol Analyzer

Progressive Format

If the .cap file used for conversion has data in the progressive format, then the converted data is displayed in the logic and Protocol analyzer as shown in the following figure. All the pixels up to the first frame have been discarded by U4998A, because these are not complete frames. The first complete frame, as shown in this figure, is considered frame 1.



Falling Edge of VDP

Figure 32 First Frame Displayed on Logic and Protocol Analyzer

A Frame begins at the last falling edge of the VDP that precedes a VSYNC and continues until the next frame begins. Because the end of the data contains an incomplete frame (ignored by the U4998A), the last frame ends with the last falling edge of the VDP as shown in the following figure.



Figure 33 Last Frame Displayed on Logic and Protocol Analyzer

The first line starts at a frame's first pixel and continues for the numbers of pixels in a line. See Figure 34. The pixels-per-line is unique to the format as listed in Table 9 on page 88. The beginning of a line falls a few pixels before the rising edge of the DI. There are two HSYNCs for every line. A pixel corresponds to a sample. Pixels are visible in waveform view and Listing view. See Figure 35 and Figure 36.



Figure 34 The Beginning of Line





	Platet ar	Transaction Tra	Tone, . Ill	and have	, atopl		a-,	· ····			بالمراجع والمستعار المراجع	
		- 🖬 🎒 🗛 🦮	# P	< T)		0	*	11 0	H Tria	8 4 _a	10 4 17 3	14.7
	11							1.0				.1
	Be	eginning of Frame 211	to Beginn	ning of Lin	<mark>e 2</mark> = 22	00[C	HOJ	Beginnin	g of Line 2	2 to B	eginning Line 3 = 2200 (CH0	1
		Sample Number	CHD	CH1	CH2	۷	Н	VGB	VDP	DI	Time	
	1	520772159	100	100	100	ō	ō	ő	1	ō	3.506883259736	s
		520772160	3FF	3FF	3FF	ō	o	ō	1	o	3.506883266470	s
		520772161	100	100	100	ō	ō	ō	1	o	3.506883273204	s
		520772162	3FF	3FF	3FF	ō	ō	ō	1	o	3.506883279938	5
		520772163	100	100	100	o	o	0	1	0	3.506883286672	3
		520772164	3FF	3FF	3FF	0	0				3.506883293406	s
		520772165	100	100	100	0					3.506883300140	
		520772166	100	100	100						3.506883306874	
		520772167	3FF	3FF	3FF						3.506883313608	
		520772168	100	100	100						3.506883320343	
		520772169	3FF	3FF	3FF						3.506883327077	
		520772170	100	100	100						3.506883333811	
		520772171	3FF	3FF	3FF						3.506883340545	
		520772172	100	100	100						3.506883347279	
		520772173	3FF	3FF	3FF						3.506883354013	
		520772174	100	100	100	0					3.506883360747	
		520772175	100	100	100						3.506883367481	
		520772176	3FF	3FF	3FF						3.506883374215	
		520772177	100	100	100						3.506883380949	
		520772178	3FF	3FF	3FF						3.506883387683	
		520772179	100	100	100	0					3.506883394417	
First Pixel —		520772180	3FF	ЗFF	ЗFF	0		0		0	3.506883401151	5
		520772181	100	100	100	0	0	0		0	3.506883407885	
		520772182	3FF	3FF	3FF	0					3.506883414619	
		520772183	100	100	100	0	0	0		0	3.506883421353	
		520772184	100	100	100	0	0	0		0	3.506883428087	
		520772185	3FF	3FF	3FF	0					3.506883434821	
		520772186	100	100	100	0	0	0	1	0	3.506883441555	5
	- Be -	520772187	354	354	354	0	0	0	0	0	3.506883448289	3
Second Pixel	SE +	520772188	354	354	354	0	0	0	0	0	3.506883455023	3
		520772189	354	354	354	0	0	0	0	0	3.506883461757	5
		520772190	354	354	354	0	0	0	0	0	3.506883468491	3
	L'allans,	A CONTRACTOR	4154	- MAR	UAB.	0	_0.	0		- O	3, 505868,40522,5	3

Figure 36 Pixels in Listing View

Interlaced Video Data

To determine the start of the first frame, if the pixel offset to the first frame is:

- less than 50% frame width, the first frame begins at the last falling edge of the VDP to precede the first VSYNC.
- greater than 50% of frame width, then the first frame begins at the last falling edge of the VDP to precede the third VSYNC. See Figure 37.



Figure 37 Pixel Offset is Greater than 50% of Frame Width

In interlaced formatted files, Logic and Protocol Analyzer reads every half frame as a whole frame. Therefore, there are four VSYNCs-per-frame instead of the two VSYNCs-per-frame seen in progressive formats. See Figure 38.





The last frame ends at the last full (interlaced) frame and is located by counting full frames from frame 1 until the last full frame is reached.

The first line starts at a frame's first pixel and continues for the numbers of pixels in a line. See Figure 39. The pixels-per-line is unique to the format as listed in Table 9 on page 88. The beginning of a line falls a few pixels before the rising edge of the DI. There are two HSYNCs for every line.

A pixel corresponds to a sample and is visible in waveform view and Listing view. See Figure 40 and Figure 41.

Bus/Signal 2 CH0	29.870580158 ms	29.877720158 m 	ns 29.8846	360158 ms + + + 3 3 3	29.892000158 m 354 354 354	is 2 i i	9.899140158 m 1 1 1 1		29.9062801
D+CH0 D+CH1 D+CH2 V H	0 0	() 190) 190)		3 3 3	354 354 354				(\) 29⊂ ¥ 29⊂ ¥
a-cH1 and an and a state of the state of th	0 0	19C X		3	854				29C X
V H	0 <u>0</u>	19CX		3	354) (K	29C 🖌
V H	0 0	1							
н	0 0						0		
				l	0				0
VGB									0
VDP	1								
DI	0 1				0				1
Time 29.8658	98991 ms								
			-		and the second second				
	-			Line	1			• •	Line







Figure 40 Start of First and Second Pixels of Frame 211 Shown in Waveform View

	maket an		Tone .G	anany	stras!			A.w.,		· · · · ·	در به دادری ^{به رس} اند این از در هار به از از از از از از از	وروحي وروم	
		≝ ⊌ ⊜ M ` A	6 F	< T)	H Q		×.	10-1	t <u>ing</u>	1%	12 I * * *	17.7	
	E	Beginning of Frame 211 to Beginning of Line 2 = 2200 [CH0]							Beginning of Line 2 to Beginning Line 3 = 2200 (CH0)				
		Sample Number	CHO	CHI	CHD	V	н	VCR	VDP	DI	Time	_	
		Sample Number	CHU	CHI	GHZ	×.	-	VGB	VDP	DI	11018		
		520772159	100	100	100						3.506883259736	s	
		520772160	3FF	3 F F	3 F F						3.506883266470	8	
		520772161	100	100	100						3.506883273204	5	
		520772162	3FF	3 F F	3 F F						3.506883279938	5	
		520772163	100	100	100						3.506883286672	5	
		520772164	3FF	3FF	3FF						3.506883293406	5	
		520772165	100	100	100						3.506883300140	5	
		520772166	100	100	100						3.506883306874	8	
		520772167	3FF	3 F F	3FF						3.506883313608	5	
		520772168	100	100	100						3.506883320343	8	
		520772169	3FF	3FF	3FF						3.506883327077	8	
		520772170	100	100	100						3.506883333811	5	
		520772171	3FF	3FF	3FF						3.506883340545	5	
		520772172	100	100	100						3.506883347279	5	
		520772173	3FF	3FF	3FF						3.506883354013	5	
		520772174	100	100	100						3.506883360747	5	
		520772175	100	100	100						3.506883367481	5	
		520772176	3FF	3FF	3FF						3.506883374215	3	
		520772177	100	100	100						3.506883380949	5	
		520772178	3FF	3FF	3FF						3.506883387683	8	
		520772179	100	100	100						3.506883394417	5	
First Pixel —		520772180	3FF	3 F F	3FF						3.506883401151	5	
		520772181	100	100	100	0					3.506883407885	3	
		520772182	3FF	3FF	3FF						3.506883414619	5	
		520772103	100	100	100	0	0	0		0	3.506003421353	5	
		520772184	100	100	100	0	0	0		0	3.506883428087	5	
		520772185	3FF	3FF	3FF						3.506883434821	5	
		520772186	100	100	100	0	0	0	1	0	3.506883441555	8	
	<u> </u>	520772187	354	354	354	0	0	0	0	0	3.506883448289	8	
cond Pixel —		520772188	354	354	354	0	0	0	Û	0	3.506883455023	5	
		520772189	354	354	354	0	0	0	0	0	3.506883461757	5	
		520772190	354	354	354						3.506883468491	5	
	L.Jan	520272191	354	DEB.	OAB_	0	.0	0	. 0		3,506883475225	5	

Figure 41 First and Second Pixels of Frame 211 Shown in List View



Agilent U4998A HDMI/MHL Protocol/Audio/Video Analyzer and Generator User Guide

Testing a HDMI/MHL Sink Device

Overview 98

Using the Predefined Audio and Video Files for transmission 99 Configuring Frame Settings for Transmission to a Sink Device 104 Starting and Stopping the Transmission of Frames 107 Evaluating the Sink Device for Compliance to HDMI/MHL CTS 109

This chapter describes how you can configure U4998A to test a HDMI/MHL sink DUT. It also describes how you can transmit predefined audio/video frames from U4998A to a sink DUT for various sink tests.



4 Testing a HDMI/MHL Sink Device

Overview

The following figure illustrates the broad steps that you need to perform to test a HDMI/MHL sink DUT using U4998A.



Figure 42 HDMI/MHL Generator flow

The topics that follow describe each of these tasks in detail.

Refer to the topic "U4998A Roles and Usage Scenarios" on page 17 to get a pictorial representation of U4998A as a generator.

Using the Predefined Audio and Video Files for transmission

While testing a sink DUT, U4998A emulates the role of a generator and transmits the audio and video files that you specify for transmission. It does not, however, read the EDID of the sink DUT for the transmission.

A set of predefined video (.vgf) and audio (.aaf) files are provided that you can transmit from U4998A to a DUT. To get this set of predefined audio/video files, you need to install the following software component:

- **U4998A HDMI Video Generator Files utility** This utility installs a set of predefined .vgf and .aaf files at the default location or a location that you specify while installation. You can use these files for HDMI sink device testing.
- U4998A MHL Video Generator Files utility This utility installs a set of predefined .vgf and .aaf files at the default location or a location that you specify while installation. You can use these files for MHL sink device testing.

The following figure displays the default locations for the installation of these files for HDMI and MHL.



Figure 43 Default location of predefined Audio and Video files for HDMI





These audio/video files are as per the requirements of various HDMI CTS 1.4a/1.4b and MHL CTS 1.2 sink tests to help you run these tests at the sink DUT end.

For HDMI, the files are organized in subfolders on the basis of the correspond sink test. For instance, the Video and audio files for test 8- 23 are located in the 8-23 Audio Formats folder.

For MHL, the files are organized in subfolders on the basis of the image patterns specified in the MHL CTS for various MHL sink tests.

Naming convention for the predefined audio and video files

The following is the naming convention used for the .vgf files.

	VIC14_RGB_10Bit_59Hz_RPT02.vgf
Video Identification Code —	
Color Space —	
Color Depth —	
Frequency —	
Optional Attribute — (Pixel repitition = 02)	

The following is the naming convention used for the .aaf files.

	VSync32kHz_F32kHz_S16Bit	_2Channels.aaf
Audio Sampling Frequency		
Sample Size		
Channel Count		

Supported Sink Tests

HDMI Sink Tests

U4998A provides the required audio/video files for all sink tests except for 8-22, 8-27, and 8-28 tests.

MHL Sink Tests

U4998A provides the required audio/video files for 4.2.1.1, 4.2.1.2, 4.2.2.1, 4.2.2.2, 4.2.2.3, 4.2.3.1, and 4.2.3.2 MHL sink tests.

Video Format Timings supported by .vgf Files

The following table lists the video format timings supported by the .vgf files.

4 Testing a HDMI/MHL Sink Device

CEA Video	Format
Identification Code	
1	640 x 480 @ 59.94 / 60 Hz
2, 3	720 x 480 @ 59.94 / 60 Hz
4	1280 x 720 @ 59.94 / 60 Hz
5	1920 x 1080i @ 59.94 / 60 Hz
6, 7	1440 x 480i @ 59.94 / 60 Hz
8, 9	720 (1440) x 240p @ 59.94 / 60 Hz
10, 11	2880 x 480i @ 59.94 / 60 Hz
12, 13	2880 x 240p @ 59.94 / 60 Hz
14, 15	1440 x 480p @ 59.94 / 60 Hz
16	1920 x 1080p @ 59.94 / 60 Hz
17, 18	720 x 576p @ 50Hz
19	1280 x 720p @ 50Hz
20	1920 x 1080i @ 50 Hz
21, 22	720 (1440) x 576i @ 50 Hz
23, 24	720 (1440) x 288p @ 50 Hz
25, 26	2880 x 576i @ 50 Hz
27, 28	2880 x 288p @ 50 Hz
29, 30	1440 x 576p @ 50 Hz
31	1920 x 1080p @ 50 Hz
32	1920 x 1080p @ 23.98 / 24 Hz
33	1920 x 1080p @ 25 Hz
34	1920 x 1080p @ 29.97 / 30 Hz
35, 36	2880 x 480p @ 59.94 / 60 Hz
37, 38	2880 x 576p @ 50 Hz
39	1920 x 1080i (1250 total) @ 50 Hz
40	1920 x 1080i @ 100 Hz
41	1280 x 720p @ 100 Hz
42, 43	720 x 576p @ 100 Hz
44, 45	720 (1440) x 576i @ 100 Hz
46	1920 x 1080i @ 119.88 / 120 Hz
47	1280 x 720p @ 119.88 / 120 Hz
48, 49	720 x 480p @ 119.88 / 120 Hz
50, 51	720 (1440) x 480i @ 119.88 / 120 Hz
52, 53	720 x 576p @ 200 Hz
54, 55	720 (1440) x 576i @ 200 Hz
56, 57	720 x 480p @ 239.76 / 240 Hz
58, 59	720 (1440) x 480i @ 239.76 / 240 Hz
60	1280 x 720p @ 23.98 / 24 Hz

CEA Video Identification Code	Format
61	1280 x 720p @ 25 Hz
62	1280 x 720p @ 29.97 / 30 Hz
63	1920 x 1080p @ 119.88 / 120 Hz
64	1920 x 1080p @ 100 Hz
H01	3840 x 2160p @ 29.97 / 30 Hz
H02	3840 x 2160p @ 25 Hz
H03	3840 x 2160p @ 23.98/ 24 Hz
H04	4096 x 2160p @ 24 Hz

Configuring Frame Settings for Transmission to a Sink Device

NOTE

To test a HDMI/MHL sink DUT, U4998A needs to emulate a HDMI/MHL source device that can transmit data to the DUT. Therefore, ensure that you select the connection type as **U4998A** -**Frame Generator** while setting up a connection between U4998A and DUT.

The frame settings control which video and audio files (from the predefined set) you want to transmit to the sink DUT from U4998A.

You use the Agilent Logic and Protocol Analyzer GUI to configure the frame settings.

Setup						
Connection Setup Capture Setup Frame Setup						
Start	Start Clock Deviation 0%					
Video Properties				Audio Properties 🔽 Enable Audio Properties		
Directory: Int Techn	Directory: Int Technologies\Logic Analyzer\HDMI\Generator Data\8-21 Audio Clock Re			Directory: C:\Users\Public\Documents\Agilent Technologies\Logic Analyzer\HDMI\Ger		
Video Format Timing:	Video Format Timing: USER DEFINED VGF FILE			Sample Frequency: USER DEFINED AAF FILE		
VIC01_RGB_8bit_60H	VIC01_RGB_8bit_60Hz.vgf			VSync48kHz_F48kHz_S16Bit_2Channels.aaf		
VIC02_RGB_8BIt_60H VIC17_RGB_8Bit_50H	z.vgf z.vgf					
Video Format				Audio Format		
Color Space	RGB Color Depth	8 bit VIC	1	Channel Count 2 ch Format I2S Coding Type PCM Size 16		
Frequency	60 Hz Mode	2D LNSBE	0	Channel No 0 Level Shift 0 db Sampling Frequency 48.0 KHz		
Pixel Repetition	0x Quantization	Default PNELE (0	- Clock Regeneration		
TMDS Data Rate	25200000 Hz Content	Not Specified PNSRI	0	D[300-1500] 1000 N(128 x fs/D) 6144.00 CTS 25200.00		
Active format ratio	Same As Picture Ratio	LNETE	0	The user should determine the tractional relation between the TMUS clock and Audio reference clock (128*Audio Sample Rate[fs]). The exact relation between the two clocks will be 138 x fs = fTMUS, clock x N/CTS. Note: Only interest value would be considered.		
				Apply OK Cancel Help		

To configure frame settings:

- 1 Access the **Setup** dialog box by clicking **Setup-> Setup** from the drop-down menu displayed for the HDMI module.
- 2 Click the Frame Setup tab.
- **3** If needed, select the deviation from the standard TMDS clock frequency. You can choose 0%, -0.5%, or 0.5% as the deviation from the Clock Deviation listbox.
- 4 In the Video Properties section, click the <u>S</u> button displayed with the **Directory** field to browse and navigate

to the directory that contains the predefined set of .vgf files for transmission. The default directory displayed is C:\Users\Public\Public Documents\Agilent Technologies\Logic Analyzer. From this directory, you can navigate to its HDMI\Generator Data subdirectory for HDMI vgf files or to its MHL\Generator Data subdirectory for MHL vgf files. The default location may slightly vary depending on your operating system.

- 5 The Video Format Timing listbox displays a list of video formats supported by the vgf files. From this listbox, you:
 - a either select a video format. Consequently, the vgf files in the selected directory that match the selected video format are displayed in the open listbox below the Video Format Timing listbox.
 - b or select the USER DEFINED VGF FILE option.
 Consequently, all the vgf files from the selected directory are displayed in the open listbox below the Video Format Timing listbox.
- 6 From the displayed list of vgf files in the open listbox, select a vgf file that you want to transmit.

The format specific details of the selected file are displayed in the **Video Format** section.

The selection of a video file also enables the **Audio Properties** section.

- 7 Some sink tests such as 8-21 and 8-23 require the presence of audio with video transmission. For such tests, you can send an audio file as well for transmission by selecting the **Enable Audio Properties** checkbox. This enables all the audio related fields in the tab.
- 8 In the Audio Properties section, click the button displayed with the Directory field to browse and navigate to the directory that contains the predefined set of .aaf files for transmission. The default directory displayed is C:\Users\Public\Public Documents\Agilent Technologies\Logic Analyzer. From this directory, you can navigate to its HDMI\Generator Data subdirectory for HDMI aaf files or to its MHL\Generator Data subdirectory for MHL aaf files. The default location may slightly vary depending on your operating system.
- **9** The **Sample Frequency** listbox displays a list of audio frequencies supported by the aaf files. From this listbox, you:
 - **a** either select a sample frequency. Consequently, the aaf files in the selected directory that match the selected

sample frequency are displayed in the open listbox below the **Sample Frequency** listbox.

- b or select the USER DEFINED AAF FILE option.
 Consequently, all the aaf files from the selected directory are displayed in the open listbox below the Sample Frequency listbox.
- **10** From the displayed list of aaf files in the open listbox, select an aaf file that you want to transmit.

The format specific details of the selected file are displayed in the **Audio Format** section.

- 11 The fields in the Clock Regeneration section are used to regenerate the audio clock based on the ACR packet data. You can specify an integer value between 300 to 1500 in the D field based on which the N parameter (ACR packet data) is calculated and displayed in the N field.
- 12 Click Apply and then OK.

Starting and Stopping the Transmission of Frames

When you have selected the video and audio files for transmission to DUT, you can start the transmission of these files. You use the **Frame Setup** tab in the Logic and Protocol Analyzer GUI to start the transmission of frames in the specified files.

Before starting the transmission, ensure that:

- the Logic and Protocol Analyzer GUI is in the online mode.
- the HDMI sink DUT is connected to the HDMI OUTPUT Connector of the U4998A module, switched on, and configured to accept HDMI data input. For an MHL sink DUT, ensure that it is connected to the HDMI OUTPUT connector of the U4998A module via the U4995A MHL adapter, switched on, and configured to accept MHL data input.
- you have the U4998A-GEN Generator testing license to transmit data to DUT.

To start the transmission of frames

- 1 Access the **Setup** dialog box by clicking **Setup-> Setup** from the drop-down menu displayed for the HDMI module.
- 2 Click the Frame Setup tab.
- **3** Click the **Start** button.

On clicking **Start**, the Start button is disabled and the Stop button gets enabled. U4998A starts transmitting the selected vgf and aaf files continuously till you click the **Stop** button to manually stop the transmission.

Setup					
Connection Setup	Capture Setup Fran	ne Setup EDID Set	tup		
Start	op Clock Deviat	tion 0% 🔽			
Video Properties		8		Audio Properti	es 📝 Enabl
Video File ~echnolo	gies\Logic Analyzer\HD	MI\Generator Data\8-2	1 Audio Clock Re 📴	Audio File ~\+	IDMI\Genera
Video Format				Audio Format -	
Color Space	RGB	LNETE	0	Sampling F	requency
Color Depth	8 bit	LNSBE	0] Sar	nple Size
Pixel Repetition	1x	PNELE	0	Chan	nel Count
Mode(2D/3D)	2D	PNSRI	0	C.	ding Type
Content	Not Specified	Quantization	Limit	Clock Regenerat	tion
VIC	1	Frequency	60 Hz	D[300-1500]	1000
Acti	ve format aspect ratio	Same As Picture Aspe	ect Ratio	N(128 x fs/D)	6144.00

Figure 45 Start of transmission from U4998A

The TMDS Data Channel LEDs for the HDMI OUT connector on the front panel of U4998A turn green indicating the start of transmission. If the LEDs turn orange, it indicates the start of transmission but the three TMDS data channels are not aligned. The LEDs turn red if non HDMI data is transmitted.

4 To manually stop the transmission, click the **Stop** button.

Evaluating the Sink Device for Compliance to HDMI/MHL CTS

The audio and video files provided with U4998A are as per the requirements of the supported HDMI/MHL sink tests. When you transmit a specific audio and video file from U4998A to DUT, you can evaluate the DUT for the sink test corresponding to the transmitted files.

This topic lists which .vgf files are available for each of the supported HDMI sink test. It also lists the attributes such as Color format, Color depth, Repetition factor for these .vgf files.

8-16 Acceptance of all valid packet types

Video generator files for the test 8-16 are located in the folder shown in the following figure. Each file in the highlighted folder is dedicated for one of the packet types. The specific packet is sent repeatedly.



Figure 46 Location of 8-16 vgf files

The tables that follow list:

- the files provided for the two required video format timings: 720 x 480p or 720 x 576p.
- the packet type supported by each video generator file.
- the contents of each packet.

CE.	Color Space		ice		
A Vide ntifica					-
otion			~	×	
Code	Video Format Timings	RGB	CbCr	vYCC	File Name
2	720 x 480p, 60 Hz	•			VIC02_RGB_8Bit_60Hz_GC1.vgf
	720 x 480p, 60 Hz	•			VIC02_RGB_8Bit_60HzGC2.vgf
	720 x 480p, 60 Hz	•			VIC02_RGB_8Bit_60Hz_IS1.vgf
	720 x 480p, 60 Hz	•			VIC02_RGB_8Bit_60Hz_IS2.vgf
	720 x 480p, 60 Hz	•			VIC02_RGB_8Bit_60Hz_MPG.vgf
	720 x 480p, 60 Hz	•			VIC02_RGB_8Bit_60Hz_NUL.vgf
	720 x 480p, 60 Hz	•			VIC02_RGB_8Bit_60Hz_SPD.vgf
	720 x 480p, 60 Hz	•			VIC02_RGB_8Bit_60Hz_VSI.vgf
	720 x 480p, 60 Hz		•		VIC02_Y444_8Bit_60Hz_GC1.vgf
	720 x 480p, 60 Hz		•		VIC02_Y444_8Bit_60HzGC2.vgf
	720 x 480p, 60 Hz		•		VIC02_Y444_8Bit_60Hz_IS1.vgf
	720 x 480p, 60 Hz		•		VIC02_Y444_8Bit_60Hz_IS2.vgf
	720 x 480p, 60 Hz		•		VIC02_Y444_8Bit_60Hz_MPG.vgf
	720 x 480p, 60 Hz		•		VIC02_Y444_8Bit_60Hz_NUL.vgf
	720 x 480p, 60 Hz		•		VIC02_Y444_8Bit_60Hz_SPD.vgf
	720 x 480p, 60 Hz		•		VIC02_Y444_8Bit_60Hz_VSI.vgf
3	720 x 480p, 60 Hz			٠	VIC03_xvYCC444_8Bit_60Hz.vgf
17	720 x 576p, 50 Hz	•			VIC17_RGB_8Bit_50Hz_GC1.vgf
	720 x 576p, 50 Hz	•			VIC17_RGB_8Bit_50HzGC2.vgf
	720 x 576p, 50 Hz	•			VIC17_RGB_8Bit_50Hz_IS1.vgf
	720 x 576p, 50 Hz	•			VIC17_RGB_8Bit_50Hz_IS2.vgf
	720 x 576p, 50 Hz	•			VIC17_RGB_8Bit_50Hz_MPG.vgf
	720 x 576p, 50 Hz	•			VIC17_RGB_8Bit_50Hz_NUL.vgf
	720 x 576p, 50 Hz	•			VIC17_RGB_8Bit_50Hz_SPD.vgf
	720 x 576p, 50 Hz	•			VIC17_RGB_8Bit_50Hz_VSI.vgf
	720 x 576p, 50 Hz		•		VIC17_Y444_8Bit_50Hz_GC1.vgf
	720 x 576p, 50 Hz		•		VIC17_Y444_8Bit_50HzGC2.vgf
	720 x 576p, 50 Hz		•		VIC17_Y444_8Bit_50Hz_IS1.vgf
	720 x 576p, 50 Hz		•		VIC17_Y444_8Bit_50Hz_IS2.vgf
	720 x 576p, 50 Hz		•		VIC17_Y444_8Bit_50Hz_MPG.vgf
	720 x 576p, 50 Hz		•		VIC17_Y444_8Bit_50Hz_NUL.vgf
	720 x 576p, 50 Hz		•		VIC17_Y444_8Bit_50Hz_SPD.vgf
	720 x 576p, 50 Hz		•		VIC17_Y444_8Bit_50Hz_VSI.vgf
18	720 x 576p, 50 Hz			٠	VIC18_xvYCC444_8Bit_50Hz.vgf

 Table 10
 Video Format Timings and Video Generator Files
				Che	cked p	acket	Pa s are i	cket T nserte	ype ed in tl	ne HDI	VII stre	eam.		
Filename	Filename Suffix	Null	General Control Clear_AVMUTE = 1	General Control Set_AVMUTE = 1	Vendor-Specific Info Frame	MPEG Source Info Frame	Source Product Description	AVI Info Frame	Audio Info Frame	Auto Content Protection	ISRC1 ISRC_Cont = 0	ISRC1 ISRC_Cont = 1	ISRC 2	Metadata Packet
VIC02_RGB_8Bit_60Hz_NU1.vgf	NU1	•						-						
VIC17_RGB_8BIt_50HZ_INU1.Vgf		•						-						
VICUZ_RGB_8BIT_60HZ_GC1.vgf	GC1		•					-						
VICI7_RGB_8BIT_50HZ_GCT.Vgf			•			-		-						
VICUZ_RGB_8BIT_60HZ_GCZ.vgf	GC2			•				-						
VICT7_RGB_8Bit_50Hz_GC2.vgf				•				-						
VICU2_RGB_8Bit_60Hz_VS1.vgf	VS1				•			÷					<u> </u>	
VIC17_RGB_8Bit_50Hz_VS1.vgf					•			.*	-+				<u> </u>	
VIC02_RGB_8Bit_60Hz_MPG.vgf	MPG					•		1	2'					
VIC17_RGB_8Bit_50Hz_MPG.vgf						•		-						
VIC02_RGB_8Bit_60Hz_SPD.vgf	SPD						•	-						
VIC17_RGB_8Bit_50Hz_SPD.vgf							•	-						
VIC02_RGB_8Bit_60Hz_IS1.vgf	IS1									•	•			
VIC17_RGB_8Bit_50Hz_IS1.vgf										•	•			
VIC02_RGB_8Bit_60Hz_IS2.vgf	152									•		•	•	
VIC17_RGB_8Bit_50Hz_IS2.vgf	102									•		•	•	
V1C03_xvYC444_8Bit_60Hz.vgf	none													•
V1C18_xvYC444_8Bit_50Hz.vgf	none													٠

Table 11 Video Generator Files with Supported Packets

* Always output

† Always output when any audio generator file is selected

Table 12Contents of Packet

Description	Header	Body
Null	00 00 00	
General Control #1	03 00 00	$10\ 00\ 00\ 00\ 00\ 00\ 00\ 00\ 00\ 00\ $
General Control #2	03 00 00	01 00 00 00 00 00 00 01 00 00 00 00 00 0
Vendor Specific Info Frame	81 01 17	CS 00 0C 03 41 67 69 6C 65 6E 74 20 54 65 63 68 6E 6F 6C 6F 67 69 65 73 (C-ID) Agilent Technologies

Table 12Contents of Packet

Description	Header	Body
Source Product Description Info Frame	83 01 1A	CS 53 6F 75 72 63 65 20 50 72 6F 64 75 63 74 20 44 65 73 63 72 69 70 74 69 6F 6E Source Product Description
MPEG Source Info Frame	85 01 0A	CS 80 96 98 00 00 00 00 00 00 00
Audio Content Protection	04 00 00	00 00 00 00 00 00 00 00 00 00 00 00 00
ISRC1	05 C2 00 or 05 42 00	00 00 00 00 00 00 00 00 00 00 00 00 00
ISRC2	06 00 00	00 00 00 00 00 00 00 00 00 00 00 00 00
Gamut Metadata	0A 80 30	91 9B A3 C5 95 63 62 A2 54 31 00 00 00 00 00 00 00 00 00 00 00 00 00

* Packet data is shown in hexadecimal

† Clear_AVMUTE = 1

```
$ Set_AVMUTE = 1
```

** Agilent company ID = 00 0C 03

8-21 Audio Clock Regeneration

Video and audio generator files for the test 8-21 are located in the following highlighted folder.





Test 8-21 verifies audio clock regeneration using a minimum and a maximum "N" parameter (ACR packet data). The following equation is used to derive the N parameter:

N Parameter =
$$\frac{128 \times fs}{D}$$

where f_s is the audio sample rate and *D* set to 1500 for a minimum N parameter and *D* set to 300 for a maximum N parameter.

When transmitting the relevant audio file for the test 8-21, specify the value for D in the **Clock Regeneration** section in the Frame Setup tab in Logic and Protocol Analyzer as displayed below.

Connection Setup C	apture Setup	Frame Setup EDID Set	up				
Start Sto	Clock De	viation 0% 🐱					
Video Properties				Audio Prop	erties 🔽 Enabl	e Audio Properties —	
Video File ~echnologi	es\Logic Analyzer\H	HDMI\Generator Data\8-21	Audio Clock Re 🗔	Audio File	~\HDMI\Gene	erator Data\8-21 Aud	lio Cł 🖳
Video Format			<i></i>	Audio Form	nat		
Color Space	RGB	LNETE	0] Sampl	ing Frequency	48.0 KHz	Channel Num
Color Depth	8 bit	LNSBE	0]	Sample Size	16 bit	Forr
Pixel Repetition	1x	PNELE	0]	Channel Count	2 ch	Level S
Mode(2D/3D)	2D	PNSRI	0]	Coding Type	PCM	
Content	Not Specified	Quantization	Limit	Clock Rege	neration		
VIC	2	Frequency	60 Hz	D[300-15	00] 100	0 The user s	hould determine tween the TMDS
Activ	e format aspect ra	tio Same As Picture Aspe	ect Ratio] N(128 x fs	/D) 6144.00	reference ([fs]). The e	clock (128*Audio exact relation bet
TMDS Data Rate	27027000 Hz			0	CTS 27027.00	CTS, Note: considered	be 128 x fs = fTI Only integer val

Figure 48 Value of D for test 8-21

Test 8-23. Audio Formats

Video and audio generator files for the test 8-23 are located in the following highlighted folder. One video format file and three types of two-channel L-PCM audio generator files (32 kHz, 44.1 kHz, and 48 kHz) are provided.



Figure 49 Location of Test 8-23 Folder

Test 8-25. Deep Color

Video and audio generator files for the test 8-25 are located in the following highlighted folders.



Figure 50 Location of Test 8-25 Folder

The following table lists the attributes such as color format and color depth supported by the video generator files for the test 8-25.

CEA Ider	CEA		Color Format			or De	epth	Re	petit	ion	
∖ Vid ntific			orma	n 				ſ	acto	r	
eo atio			(срс	(CPC							
1 Code	Video Format Timings	RGE	r 4:2:2	r 4:4:4	24 Bit	30 Bit	36 Bit	0	2	4	File Name
1	640 x 480p, 59.94 Hz	•		-	•	-	-	٠			VIC01_RGB_8Bit_59Hz.vgf
	640 x 480p, 60 Hz	•			•			•			VIC01_RGB_8Bit_60Hz.vgf
	640 x 480p, 59.94 Hz	•				٠		٠			VIC01_RGB_10Bit_59Hz.vgf
	640 x 480p, 60 Hz	•				•		٠			VIC01_RGB_10Bit_60Hz.vgf
	640 x 480p, 59.94 Hz	•					٠	٠			VIC01_RGB_12Bit_59Hz.vgf
	640 x 480p, 60 Hz	•					•	•			VIC01_RGB_12Bit_60Hz.vgf
	640 x 480p, 59.94 Hz			•	•			٠			VIC01_Y444_8Bit_59Hz.vgf
	640 x 480p, 60 Hz			•	•			٠			VIC01_Y444_8Bit_60Hz.vgf
	640 x 480p, 59.94 Hz			•		٠		٠			VIC01_Y444_10Bit_59Hz.vgf
	640 x 480p, 60 Hz			•		•		٠			VIC01_Y444_10Bit_60Hz.vgf
	640 x 480p, 59.94 Hz			٠			٠	٠			VIC01_Y444_12Bit_59Hz.vgf
	640 x 480p, 60 Hz			٠			٠	٠			VIC01_Y444_12Bit_60Hz.vgf
2	720 x 480p, 59.94 Hz	٠			٠			٠			VIC02_RGB_8Bit_59Hz.vgf
	720 x 480p, 60 Hz	•			•			•			VIC02_RGB_8Bit_60Hz.vgf
	720 x 480p, 59.94 Hz	•				٠		•			VIC02_RGB_10Bit_59Hz.vgf
	720 x 480p, 60 Hz	•				٠		•			VIC02_RGB_10Bit_60Hz.vgf
	720 x 480p, 59.94 Hz	•					٠	•			VIC02_RGB_12Bit_59Hz.vgf
	720 x 480p, 60 Hz	•					•	•			VIC02_RGB_12Bit_60Hz.vgf
	720 x 480p, 59.94 Hz			•	٠			٠			VIC02_Y444_8Bit_59Hz.vgf
	720 x 480p, 60 Hz			٠	٠			•			VIC02_Y444_8Bit_60Hz.vgf
	720 x 480p, 59.94 Hz			٠		٠		•			VIC02_Y444_10Bit_59Hz.vgf
	720 x 480p, 60 Hz			٠		٠		•			VIC02_Y444_10Bit_60Hz.vgf
	720 x 480p, 59.94 Hz			٠			•	•			VIC02_Y444_12Bit_59Hz.vgf
	720 x 480p, 60 Hz			•			٠	٠			VIC02_Y444_12Bit_60Hz.vgf
3	720 x 480p, 59.94 Hz	•			•			٠			VIC03_RGB_8Bit_59Hz.vgf
	720 x 480p, 60 Hz	•			•			•			VIC03_RGB_8Bit_60Hz.vgf
	720 x 480p, 59.94 Hz	•				•		•			VIC03_RGB_10Bit_59Hz.vgf
	720 x 480p, 60 Hz	•				•		٠			VIC03_RGB_10Bit_60Hz.vgf
	720 x 480p, 59.94 Hz	•					•	٠			VIC03_RGB_12Bit_59Hz.vgf
	720 x 480p, 60 Hz	•					•	٠			VIC03_RGB_12Bit_60Hz.vgf
	720 x 480p, 59.94 Hz			•	•			٠			VIC03_Y444_8Bit_59Hz.vgf
	720 x 480p, 60 Hz			•	•			٠			VIC03_Y444_8Bit_60Hz.vgf
	720 x 480p, 59.94 Hz			•		•		٠			VIC03_Y444_10Bit_59Hz.vgf
	720 x 480p, 60 Hz			•		•		•			VIC03_Y444_10Bit_60Hz.vgf

Table 13Video Generator Files for Test ID 8–25 (Sheet 1 of 10)

CEA V Identi		F	Color Format			or De	pth	Re F	petiti acto	ion r	
^r ideo fication Code	Video Format Timings	RGB	YCbCr 4:2:2	YCbCr 4:4:4	24 Bit	30 Bit	36 Bit	0	2	4	File Name
	720 x 480p, 59.94 Hz			٠			٠	٠			VIC03_Y444_12Bit_59Hz.vgf
	720 x 480p, 60 Hz			٠			٠	٠			VIC03_Y444_12Bit_60Hz.vgf
4	1280 x 720p, 59.94 Hz	٠			٠			٠			VIC04_RGB_8Bit_59Hz.vgf
	1280 x 720p, 60 Hz	٠			٠			٠			VIC04_RGB_8Bit_60Hz.vgf
	1280 x 720p, 59.94 Hz	٠				٠		٠			VIC04_RGB_10Bit_59Hz.vgf
	1280 x 720p, 60 Hz	•				•		٠			VIC04_RGB_10Bit_60Hz.vgf
	1280 x 720p, 59.94 Hz	•					•	٠			VIC04_RGB_12Bit_59Hz.vgf
	1280 x 720p, 60 Hz	٠					٠	•			VIC04_RGB_12Bit_60Hz.vgf
	1280 x 720p, 59.94 Hz			٠	٠			•			VIC04_Y444_8Bit_59Hz.vgf
	1280 x 720p, 60 Hz			٠	٠			•			VIC04_Y444_8Bit_60Hz.vgf
	1280 x 720p, 59.94 Hz			•		•		٠			VIC04_Y444_10Bit_59Hz.vgf
	1280 x 720p, 60 Hz			٠		٠		٠			VIC04_Y444_10Bit_60Hz.vgf
	1280 x 720p, 59.94 Hz			٠			٠	٠			VIC04_Y444_12Bit_59Hz.vgf
	1280 x 720p, 60 Hz			٠			٠	٠			VIC04_Y444_12Bit_60Hz.vgf
5	1920 x 1080i, 59.94 Hz	٠			٠			٠			VIC05_RGB_8Bit_59Hz.vgf
	1920 x 1080i, 60 Hz	٠			٠			•			VIC05_RGB_8Bit_60Hz.vgf
	1920 x 1080i, 59.94 Hz	٠				•		•			VIC05_RGB_10Bit_59Hz.vgf
	1920 x 1080i, 60 Hz	•				•		٠			VIC05_RGB_10Bit_60Hz.vgf
	1920 x 1080i, 59.94 Hz	•					•	٠			VIC05_RGB_12Bit_59Hz.vgf
	1920 x 1080i, 60 Hz	٠					٠	٠			VIC05_RGB_12Bit_60Hz.vgf
	1920 x 1080i, 59.94 Hz			•	•			٠			VIC05_Y444_8Bit_59Hz.vgf
	1920 x 1080i, 60 Hz			٠	٠			•			VIC05_Y444_8Bit_60Hz.vgf
	1920 x 1080i, 59.94 Hz			•		•		٠			VIC05_Y444_10Bit_59Hz.vgf
	1920 x 1080i, 60 Hz			•		•		٠			VIC05_Y444_10Bit_60Hz.vgf
	1920 x 1080i, 59.94 Hz			•			•	٠			VIC05_Y444_12Bit_59Hz.vgf
	1920 x 1080i, 60 Hz			•			•	٠			VIC05_Y444_12Bit_60Hz.vgf
6	720 (1440) x 480i, 59.94 Hz	٠			٠				•		VIC06_RGB_8Bit_59Hz.vgf
	720 (1440) x 480i, 60 Hz	•			•				•		VIC06_RGB_8Bit_60Hz.vgf
	720 (1440) x 480i, 59.94 Hz	•				•			•		VIC06_RGB_10Bit_59Hz.vgf
	720 (1440) x 480i, 60 Hz	•				•			•		VIC06_RGB_10Bit_60Hz.vgf
	720 (1440) x 480i, 59.94 Hz	•					•		•		VIC06_RGB_12Bit_59Hz.vgf
	720 (1440) x 480i, 60 Hz	•					•		•		VIC06_RGB_12Bit_60Hz.vgf
	720 (1440) x 480i, 59.94 Hz			•	•				•		VIC06_Y444_8Bit_59Hz.vgf
	720 (1440) x 480i, 60 Hz			•	•				•		VIC06_Y444_8Bit_60Hz.vgf
	720 (1440) x 480i, 59.94 Hz			•		٠			٠		VIC06_Y444_10Bit_59Hz.vgf

Table 13Video Generator Files for Test ID 8–25 (Sheet 2 of 10)

CEA V Identi		F	Color orma	t	Colo	or De	pth	Re F	petit acto	ion r	
'ideo fication Code	Video Format Timings	RGB	YCbCr 4:2:2	YCbCr 4:4:4	24 Bit	30 Bit	36 Bit	0	2	4	File Name
	720 (1440) x 480i, 60 Hz			٠		٠			٠		VIC06_Y444_10Bit_60Hz.vgf
	720 (1440) x 480i, 59.94 Hz			٠			•		٠		VIC06_Y444_12Bit_59Hz.vgf
	720 (1440) x 480i, 60 Hz			٠			•		٠		VIC06_Y444_12Bit_60Hz.vgf
7	720 (1440) x 480i, 59.94 Hz	٠			٠				٠		VIC07_RGB_8Bit_59Hz.vgf
	720 (1440) x 480i, 60 Hz	٠			٠				٠		VIC07_RGB_8Bit_60Hz.vgf
	720 (1440) x 480i, 59.94 Hz	٠				٠			٠		VIC07_RGB_10Bit_59Hz.vgf
	720 (1440) x 480i, 60 Hz	٠				٠			٠		VIC07_RGB_10Bit_60Hz.vgf
	720 (1440) x 480i, 59.94 Hz	•					•		•		VIC07_RGB_12Bit_59Hz.vgf
	720 (1440) x 480i, 60 Hz	٠					•		٠		VIC07_RGB_12Bit_60Hz.vgf
	720 (1440) x 480i, 59.94 Hz			٠	٠				٠		VIC07_Y444_8Bit_59Hz.vgf
	720 (1440) x 480i, 60 Hz			•	٠				٠		VIC07_Y444_8Bit_60Hz.vgf
	720 (1440) x 480i, 59.94 Hz			•		•			٠		VIC07_Y444_10Bit_59Hz.vgf
	720 (1440) x 480i, 60 Hz			•		•			٠		VIC07_Y444_10Bit_60Hz.vgf
	720 (1440) x 480i, 59.94 Hz			•			•		٠		VIC07_Y444_12Bit_59Hz.vgf
	720 (1440) x 480i, 60 Hz			•			•		٠		VIC07_Y444_12Bit_60Hz.vgf
14	1440 x 480p, 59.94 Hz	٠			٠			٠			VIC14_RGB_8Bit_59Hz.vgf
	1440 x 480p, 59.94 Hz	٠			٠				٠		VIC14_RGB_8Bit_59Hz_RPT02.vgf
	1440 x 480p, 60 Hz	٠			٠			٠			VIC14_RGB_8Bit_60Hz.vgf
	1440 x 480p, 60 Hz	٠			٠				٠		VIC14_RGB_8Bit_60Hz_RPT02.vgf
	1440 x 480p, 59.94 Hz	٠				٠		٠			VIC14_RGB_10Bit_59Hz.vgf
	1440 x 480p, 59.94 Hz	٠				٠			•		VIC14_RGB_10Bit_59Hz_RPT02.vgf
	1440 x 480p, 60 Hz	٠				•		٠			VIC14_RGB_10Bit_60Hz.vgf
	1440 x 480p, 60 Hz	٠				•			٠		VIC14_RGB_10Bit_60Hz_RPT02.vgf
	1440 x 480p, 59.94 Hz	٠					•	٠			VIC14_RGB_12Bit_59Hz.vgf
	1440 x 480p, 59.94 Hz	٠					•		٠		VIC14_RGB_12Bit_59Hz_RPT02.vgf
	1440 x 480p, 60 Hz	٠					•	٠			VIC14_RGB_12Bit_60Hz.vgf
	1440 x 480p, 60 Hz	٠					•		٠		VIC14_RGB_12Bit_60Hz_RPT02.vgf
	1440 x 480p, 59.94 Hz			•	٠			٠			VIC14_Y444_8Bit_59Hz.vgf
	1440 x 480p, 59.94 Hz			•	٠				٠		VIC14_Y444_8Bit_59Hz_RPT02.vgf
	1440 x 480p, 60 Hz			•	٠			٠			VIC14_Y444_8Bit_60Hz.vgf
	1440 x 480p, 60 Hz			•	٠				٠		VIC14_Y444_8Bit_60Hz_RPT02.vgf
	1440 x 480p, 59.94 Hz			٠		•		٠			VIC14_Y444_10Bit_59Hz.vgf
	1440 x 480p, 59.94 Hz			٠		•			٠		VIC14_Y444_10Bit_59Hz_RPT02.vgf
	1440 x 480p, 60 Hz			•		•		•			VIC14_Y444_10Bit_60Hz.vgf
	1440 x 480p, 60 Hz			٠		٠			٠		VIC14_Y444_10Bit_60Hz_RPT02.vgf
				_				_	_	-	

 Table 13
 Video Generator Files for Test ID 8–25 (Sheet 3 of 10)

CE		Color		Color Depth			Re	petiti	ion		
ntifi		F	orma	It				F	acto	r	
deo catio			YCb	ЧCЬ							
on C		-	Cr 4	Cr 4	24	30	36				
ode	Video Format Timings	ЗGВ	:2:2	:4:4	Bit	Bit	Bit	0	2	4	File Name
	1440 x 480p, 59.94 Hz			•			•	٠			VIC14_Y444_12Bit_59Hz.vgf
	1440 x 480p, 59.94 Hz			•			•		•		VIC14_Y444_12Bit_59Hz_RPT02.vgf
	1440 x 480p, 60 Hz			•			•	٠			VIC14_Y444_12Bit_60Hz.vgf
	1440 x 480p, 60 Hz			•			•		٠		VIC14_Y444_12Bit_60Hz_RPT02.vgf
15	1440 x 480p, 59.94 Hz	•			•			٠			VIC15_RGB_8Bit_59Hz.vgf
	1440 x 480p, 59.94 Hz	•			٠				٠		VIC15_RGB_8Bit_59Hz_RPT02.vgf
	1440 x 480p, 60 Hz	٠			٠			٠			VIC15_RGB_8Bit_60Hz.vgf
	1440 x 480p, 60 Hz	•			٠				٠		VIC15_RGB_8Bit_60Hz_RPT02.vgf
	1440 x 480p, 59.94 Hz	•				•		٠			VIC15_RGB_10Bit_59Hz.vgf
	1440 x 480p, 59.94 Hz	٠				٠			٠		VIC15_RGB_10Bit_59Hz_RPT02.vgf
	1440 x 480p, 60 Hz	٠				٠		٠			VIC15_RGB_10Bit_60Hz.vgf
	1440 x 480p, 60 Hz	٠				٠			٠		VIC15_RGB_10Bit_60Hz_RPT02.vgf
	1440 x 480p, 59.94 Hz	•					•	•			VIC15_RGB_12Bit_59Hz.vgf
	1440 x 480p, 59.94 Hz	٠					٠		•		VIC15_RGB_12Bit_59Hz_RPT02.vgf
	1440 x 480p, 60 Hz	•					•	•			VIC15_RGB_12Bit_60Hz.vgf
	1440 x 480p, 60 Hz	•					•		•		VIC15_RGB_12Bit_60Hz_RPT02.vgf
	1440 x 480p, 59.94 Hz			•	•			•			VIC15_Y444_8Bit_59Hz.vgf
	1440 x 480p, 59.94 Hz			•	•				•		VIC15_Y444_8Bit_59Hz_RPT02.vgf
	1440 x 480p, 60 Hz			٠	٠			٠			VIC15_Y444_8Bit_60Hz.vgf
	1440 x 480p, 60 Hz			٠	٠				٠		VIC15_Y444_8Bit_60Hz_RPT02.vgf
	1440 x 480p, 59.94 Hz			٠		٠		٠			VIC15_Y444_10Bit_59Hz.vgf
	1440 x 480p, 59.94 Hz			٠		٠			٠		VIC15_Y444_10Bit_59Hz_RPT02.vgf
	1440 x 480p, 60 Hz			٠		٠		٠			VIC15_Y444_10Bit_60Hz.vgf
	1440 x 480p, 60 Hz			٠		٠			٠		VIC15_Y444_10Bit_60Hz_RPT02.vgf
	1440 x 480p, 59.94 Hz			٠			٠	٠			VIC15_Y444_12Bit_59Hz.vgf
	1440 x 480p, 59.94 Hz			•			•		•		VIC15_Y444_12Bit_59Hz_RPT02.vgf
	1440 x 480p, 60 Hz			•			•	•			VIC15_Y444_12Bit_60Hz.vgf
	1440 x 480p, 60 Hz			•			٠		•		VIC15_Y444_12Bit_60Hz_RPT02.vgf
16	1920 x 1080p, 59.94 Hz	٠			٠			٠			VIC16_RGB_8Bit_59Hz.vgf
	1920 x 1080p, 60 Hz	٠			٠			٠			VIC16_RGB_8Bit_60Hz.vgf
	1920 x 1080p, 59.94 Hz	٠				•		•			VIC16_RGB_10Bit_59Hz.vgf
	1920 x 1080p, 60 Hz	•				•		•			VIC16_RGB_10Bit_60Hz.vgf
	1920 x 1080p, 59.94 Hz	•					•	•			VIC16_RGB_12Bit_59Hz.vgf
	1920 x 1080p, 60 Hz	•					•	•			VIC16_RGB_12Bit_60Hz.vgf
	1920 x 1080p, 59.94 Hz			٠	•			٠			VIC16_Y444_8Bit_59Hz.vgf

 Table 13
 Video Generator Files for Test ID 8–25 (Sheet 4 of 10)

CEA V Identi		F	Color Format		Col	or De	epth	Re I	petit Facto	ion r	
ideo fication Code	Video Format Timings	RGB	YCbCr 4:2:2	YCbCr 4:4:4	24 Bit	30 Bit	36 Bit	0	2	4	File Name
	1920 x 1080p, 60 Hz			٠	٠			٠			VIC16_Y444_8Bit_60Hz.vgf
	1920 x 1080p, 59.94 Hz			•		٠		•			VIC16_Y444_10Bit_59Hz.vgf
	1920 x 1080p, 60 Hz			•		٠		•			VIC16_Y444_10Bit_60Hz.vgf
	1920 x 1080p, 59.94 Hz			•			•	•			VIC16_Y444_12Bit_59Hz.vgf
	1920 x 1080p, 60 Hz			•			•	•			VIC16_Y444_12Bit_60Hz.vgf
17	720 x 576p, 50 Hz	٠			٠			٠			VIC17_RGB_8Bit_50Hz.vgf
	720 x 576p, 50 Hz	٠				٠		٠			VIC17_RGB_10Bit_50Hz.vgf
	720 x 576p, 50 Hz	•					•	•			VIC17_RGB_12Bit_50Hz.vgf
	720 x 576p, 50 Hz			٠	٠			٠			VIC17_Y444_8Bit_50Hz.vgf
	720 x 576p, 50 Hz			•		٠		٠			VIC17_Y444_10Bit_50Hz.vgf
	720 x 576p, 50 Hz			٠			•	٠			VIC17_Y444_12Bit_50Hz.vgf
18	720 x 576p, 50 Hz	•			•			٠			VIC18_RGB_8Bit_50Hz.vgf
	720 x 576p, 50 Hz	٠				٠		٠			VIC18_RGB_10Bit_50Hz.vgf
	720 x 576p, 50 Hz	٠					•	٠			VIC18_RGB_12Bit_50Hz.vgf
	720 x 576p, 50 Hz			•	•			٠			VIC18_Y444_8Bit_50Hz.vgf
	720 x 576p, 50 Hz			•		٠		•			VIC18_Y444_10Bit_50Hz.vgf
	720 x 576p, 50 Hz			•			•	•			VIC18_Y444_12Bit_50Hz.vgf
19	1280 x 720p, 50 Hz	•			•			٠			VIC19_RGB_8Bit_50Hz.vgf
	1280 x 720p, 50 Hz	•				٠		•			VIC19_RGB_10Bit_50Hz.vgf
	1280 x 720p, 50 Hz	•					•	•			VIC19_RGB_12Bit_50Hz.vgf
	1280 x 720p, 50 Hz			•	٠			•			VIC19_Y444_8Bit_50Hz.vgf
	1280 x 720p, 50 Hz			•		٠		•			VIC19_Y444_10Bit_50Hz.vgf
	1280 x 720p, 50 Hz			٠			•	٠			VIC19_Y444_12Bit_50Hz.vgf
20	1920 x 1080i, 50 Hz	•			•			٠			VIC20_RGB_8Bit_50Hz.vgf
	1920 x 1080i, 50 Hz	•				٠		•			VIC20_RGB_10Bit_50Hz.vgf
	1920 x 1080i, 50 Hz	٠					•	٠			VIC20_RGB_12Bit_50Hz.vgf
	1920 x 1080i, 50 Hz			٠	٠			٠			VIC20_Y444_8Bit_50Hz.vgf
	1920 x 1080i, 50 Hz			٠		٠		٠			VIC20_Y444_10Bit_50Hz.vgf
	1920 x 1080i, 50 Hz			٠			•	٠			VIC20_Y444_12Bit_50Hz.vgf
21	720 (1440) x 576i, 50 Hz	•			•			٠			VIC21_RGB_8Bit_50Hz.vgf
	720 (1440) x 576i, 50 Hz	•				٠		•			VIC21_RGB_10Bit_50Hz.vgf
	720 (1440) x 576i, 50 Hz	•					•	٠			VIC21_RGB_12Bit_50Hz.vgf
	720 (1440) x 576i, 50 Hz			٠	•			٠			VIC21_Y444_8Bit_50Hz.vgf
	720 (1440) x 576i, 50 Hz			٠		٠		٠			VIC21_Y444_10Bit_50Hz.vgf
	720 (1440) x 576i, 50 Hz			٠			•	٠			VIC21_Y444_12Bit_50Hz.vgf

 Table 13
 Video Generator Files for Test ID 8–25 (Sheet 5 of 10)

CE.		Color		Cole	or De	pth	Re	petiti	ion		
A Via		F	orma	t				F	acto	r	
leo catio			үсь	үсь							
on C		т	Cr 4	Cr 4	24	30	36				
ode	Video Format Timings	ßB	:2:2	:4:4	Bit	Bit	Bit	0	2	4	File Name
22	720 (1440) x 576i, 50 Hz	٠			•			•			VIC22_RGB_8Bit_50Hz.vgf
	720 (1440) x 576i, 50 Hz	٠				•		•			VIC22_RGB_10Bit_50Hz.vgf
	720 (1440) x 576i, 50 Hz	٠					•	•			VIC22_RGB_12Bit_50Hz.vgf
	720 (1440) x 576i, 50 Hz			٠	•			•			VIC22_Y444_8Bit_50Hz.vgf
	720 (1440) x 576i, 50 Hz			•		•		•			VIC22_Y444_10Bit_50Hz.vgf
	720 (1440) x 576i, 50 Hz			•			•	•			VIC20_Y444_12Bit_50Hz.vgf
29	1440 x 576p, 50 Hz	٠			•			٠			VIC29_RGB_8Bit_50Hz.vgf
	1440 x 576p, 50 Hz	٠			•				•		VIC29_RGB_8Bit_50Hz_RPT02.vgf
	1440 x 576p, 50 Hz	٠				٠		•			VIC29_RGB_10Bit_50Hz.vgf
	1440 x 576p, 50 Hz	٠				٠			•		VIC29_RGB_10Bit_50Hz_RPT02.vgf
	1440 x 576p, 50 Hz	•					•	•			VIC29_RGB_12Bit_50Hz.vgf
	1440 x 576p, 50 Hz	•					•		•		VIC29_RGB_12Bit_50Hz_RPT02.vgf
	1440 x 576p, 50 Hz			•	•			•			VIC29_Y444_8Bit_50Hz.vgf
	1440 x 576p, 50 Hz			•	•				•		VIC29_Y444_8Bit_50Hz_RPT02.vgf
	1440 x 576p, 50 Hz			•		•		•			VIC29_Y444_10Bit_50Hz.vgf
	1440 x 576p, 50 Hz			٠		٠			٠		VIC29_Y444_10Bit_50Hz_RPT02.vgf
	1440 x 576p, 50 Hz			٠			٠	٠			VIC29_Y444_12Bit_50Hz.vgf
	1440 x 576p, 50 Hz			٠			٠		٠		VIC29_Y444_12Bit_50Hz_RPT02.vgf
30	1440 x 576p, 50 Hz	٠			٠			٠			VIC30_RGB_8Bit_50Hz.vgf
	1440 x 576p, 50 Hz	•			•				•		VIC30_RGB_8Bit_50Hz_RPT02.vgf
	1440 x 576p, 50 Hz	٠				•		•			VIC30_RGB_10Bit_50Hz.vgf
	1440 x 576p, 50 Hz	٠				•			٠		VIC30_RGB_10Bit_50Hz_RPT02.vgf
	1440 x 576p, 50 Hz	•					٠	٠			VIC30_RGB_12Bit_50Hz.vgf
	1440 x 576p, 50 Hz	•					٠		٠		VIC30_RGB_12Bit_50Hz_RPT02.vgf
	1440 x 576p, 50 Hz			٠	٠			٠			VIC30_Y444_8Bit_50Hz.vgf
	1440 x 576p, 50 Hz			٠	٠				٠		VIC30_Y444_8Bit_50Hz_RPT02.vgf
	1440 x 576p, 50 Hz			•		•		٠			VIC30_Y444_10Bit_50Hz.vgf
	1440 x 576p, 50 Hz			٠		٠			٠		VIC30_Y444_10Bit_50Hz_RPT02.vgf
	1440 x 576p, 50 Hz			٠			٠	•			VIC30_Y444_12Bit_50Hz.vgf
	1440 x 576p, 50 Hz			٠			٠		٠		VIC30_Y444_12Bit_50Hz_RPT02.vgf
31	1920 x 1080p, 50 Hz	•			•			٠			VIC31_RGB_8Bit_50Hz.vgf
	1920 x 1080p, 50 Hz	•				•		٠			VIC31_RGB_10Bit_50Hz.vgf
	1920 x 1080p, 50 Hz	•					٠	٠			VIC31_RGB_12Bit_50Hz.vgf
	1920 x 1080p, 50 Hz			•	•			٠			VIC31_Y444_8Bit_50Hz.vgf
	1920 x 1080p, 50 Hz			٠		٠		٠			VIC31_Y444_10Bit_50Hz.vgf

Table 13Video Generator Files for Test ID 8–25 (Sheet 6 of 10)

CEA V Identii	CEA Vi		Color orma	ıt	Colo	or De	pth	Re F	petiti acto	ion r	
ideo ication Code	Video Format Timings	RGB	YCbCr 4:2:2	YCbCr 4:4:4	24 Bit	30 Bit	36 Bit	0	2	4	File Name
22		_		•	-		•	•			
32	1920 X 1080p, 23.96 HZ	•			•			•			
	1920 x 1080p, 24 Hz	•			•			•			VIC32_RGB_8BIt_24Hz.vgf
	1920 x 1080p, 23.98 Hz	•				•		•			
	1920 x 1080p, 24 Hz	•				•		•			VIC32_RGB_10Bit_24Hz.vgf
	1920 x 1080p, 23.98 Hz	•					•	•			VIC32_RGB_12Bit_23Hz.vgf
	1920 x 1080p, 24 Hz	•					•	•			VIC32_RGB_12Bit_24Hz.vgf
	1920 x 1080p, 23.98 Hz			•	•			•			VIC32_Y444_8Bit_23Hz.vgf
	1920 x 1080p, 24 Hz			•	٠			٠			VIC32_Y444_8Bit_24Hz.vgf
	1920 x 1080p, 23.98 Hz			•		•		•			VIC32_Y444_10Bit_23Hz.vgf
	1920 x 1080p, 24 Hz			•		•		•			VIC32_Y444_10Bit_24Hz.vgf
	1920 x 1080p, 23.98 Hz			٠			٠	٠			VIC32_Y444_12Bit_23Hz.vgf
	1920 x 1080p, 24 Hz			٠			٠	٠			VIC32_Y444_12Bit_24Hz.vgf
35	2880 x 480p, 59.94 Hz	•			•			•			VIC35_RGB_8Bit_59Hz.vgf
	2880 x 480p, 59.94 Hz	•			٠				•		VIC35_RGB_8Bit_59Hz_RPT02.vgf
	2880 x 480p, 59.94 Hz	•			٠					٠	VIC35_RGB_8Bit_59Hz_RPT04.vgf
	2880 x 480p, 60 Hz	•			•			•			VIC35_RGB_8Bit_60Hz.vgf
	2880 x 480p, 60 Hz	•			•				•		VIC35_RGB_8Bit_60Hz_RPT02.vgf
	2880 x 480p, 60 Hz	٠			•					•	VIC35_RGB_8Bit_60Hz_RPT04.vgf
	2880 x 480p, 59.94 Hz	٠				٠		٠			VIC35_RGB_10Bit_59Hz.vgf
	2880 x 480p, 59.94 Hz	•				•			•		VIC35_RGB_10Bit_59Hz_RPT02.vgf
	2880 x 480p, 59.94 Hz	•				•				•	VIC35_RGB_10Bit_59Hz_RPT04.vgf
	2880 x 480p, 60 Hz	•				•		•			VIC35_RGB_10Bit_60Hz.vgf
	2880 x 480p, 60 Hz	٠				٠			٠		VIC35_RGB_10Bit_60Hz_RPT02.vgf
	2880 x 480p, 60 Hz	٠				٠				٠	VIC35_RGB_10Bit_60Hz_RPT04.vgf
	2880 x 480p, 59.94 Hz	٠					٠	٠			VIC35_RGB_12Bit_59Hz.vgf
	2880 x 480p, 59.94 Hz	٠					٠		٠		VIC35_RGB_12Bit_59Hz_RPT02.vgf
	2880 x 480p, 59.94 Hz	٠					•			٠	VIC35_RGB_12Bit_59Hz_RPT04.vgf
	2880 x 480p, 60 Hz	٠					•	•			VIC35_RGB_12Bit_60Hz.vgf
	2880 x 480p, 60 Hz	•					٠		٠		VIC35_RGB_12Bit_60Hz_RPT02.vgf
	2880 x 480p, 60 Hz	•					٠			٠	VIC35_RGB_12Bit_60Hz_RPT04.vgf
	2880 x 480p, 59.94 Hz			•	•			٠			VIC35_Y444_8Bit_59Hz.vgf
	2880 x 480p, 59.94 Hz			•	•				٠		VIC35_Y444_8Bit_59Hz_RPT02.vgf
	2880 x 480p, 59.94 Hz			•	•					٠	VIC35_Y444_8Bit_59Hz_RPT04.vgf
	2880 x 480p, 60 Hz			•	•			٠			VIC35_Y444_8Bit_60Hz.vgf

 Table 13
 Video Generator Files for Test ID 8–25 (Sheet 7 of 10)

CEA Iden	CEA		Color Format			Color Depth			petiti acto	ion r	
Vid									αυιυ	•	
eo atio			/СЬС	/CbC							
n Coc	Video Format Timinga	RG	r 4:2	r 4:4	24 E	30 E	36 E	•	2		File News
de	video Format Timings	ΪB	:2	:4	3it	Sit	3it	U	2	4	
	2880 x 480p, 60 Hz			•	•				•		VIC35_Y444_8Bit_60Hz_RP102.vgf
	2880 x 480p, 60 Hz			•	•					•	VIC35_Y444_8Bit_60Hz_RP104.vgf
	2880 x 480p, 59.94 Hz			•		•		•			VIC35_Y444_10Bit_59Hz.vgf
	2880 x 480p, 59.94 Hz			•		•			•		VIC35_Y444_10Bit_59Hz_RPT02.vgf
	2880 x 480p, 59.94 Hz			•		•				•	VIC35_Y444_10Bit_59Hz_RPT04.vgf
	2880 x 480p, 60 Hz			٠		•		٠			VIC35_Y444_10Bit_60Hz.vgf
	2880 x 480p, 60 Hz			٠		•			•		VIC35_Y444_10Bit_60Hz_RPT02.vgf
	2880 x 480p, 60 Hz			•		•				•	VIC35_Y444_10Bit_60Hz_RPT04.vgf
	2880 x 480p, 59.94 Hz			٠			•	٠			VIC35_Y444_12Bit_59Hz.vgf
	2880 x 480p, 59.94 Hz			•			•		•		VIC35_Y444_12Bit_59Hz_RPT02.vgf
	2880 x 480p, 59.94 Hz			٠			٠			٠	VIC35_Y444_12Bit_59Hz_RPT04.vgf
	2880 x 480p, 60 Hz			•			•	•			VIC35_Y444_12Bit_60Hz.vgf
	2880 x 480p, 60 Hz			٠			٠		٠		VIC35_Y444_12Bit_60Hz_RPT02.vgf
	2880 x 480p, 60 Hz			•			٠			٠	VIC35_Y444_12Bit_60Hz_RPT04.vgf
36	2880 x 480p, 59.94 Hz	٠			٠			٠			VIC36_RGB_8Bit_59Hz.vgf
	2880 x 480p, 59.94 Hz	٠			٠				٠		VIC36_RGB_8Bit_59Hz_RPT02.vgf
	2880 x 480p, 59.94 Hz	٠			٠					٠	VIC36_RGB_8Bit_59Hz_RPT04.vgf
	2880 x 480p, 60 Hz	٠			٠			٠			VIC36_RGB_8Bit_60Hz.vgf
	2880 x 480p, 60 Hz	•			•				٠		VIC36_RGB_8Bit_60Hz_RPT02.vgf
	2880 x 480p, 60 Hz	٠			٠					٠	VIC36_RGB_8Bit_60Hz_RPT04.vgf
	2880 x 480p, 59.94 Hz	•				٠		•			VIC36_RGB_10Bit_59Hz.vgf
	2880 x 480p, 59.94 Hz	•				٠			٠		VIC36_RGB_10Bit_59Hz_RPT02.vgf
	2880 x 480p, 59.94 Hz	٠				•				٠	VIC36_RGB_10Bit_59Hz_RPT04.vgf
	2880 x 480p, 60 Hz	٠				•		•			VIC36_RGB_10Bit_60Hz.vgf
	2880 x 480p, 60 Hz	٠				•			٠		VIC36_RGB_10Bit_60Hz_RPT02.vgf
	2880 x 480p, 60 Hz	٠				•				٠	VIC36_RGB_10Bit_60Hz_RPT04.vgf
	2880 x 480p, 59.94 Hz	٠					٠	•			VIC36_RGB_12Bit_59Hz.vgf
	2880 x 480p, 59.94 Hz	٠					٠		•		VIC36_RGB_12Bit_59Hz_RPT02.vgf
	2880 x 480p, 59.94 Hz	٠					٠			٠	VIC36_RGB_12Bit_59Hz_RPT04.vgf
	2880 x 480p, 60 Hz	٠					٠	٠			VIC36_RGB_12Bit_60Hz.vgf
	2880 x 480p, 60 Hz	٠					٠		٠		VIC36_RGB_12Bit_60Hz_RPT02.vgf
	2880 x 480p, 60 Hz	٠					٠			٠	VIC36_RGB_12Bit_60Hz_RPT04.vgf
	2880 x 480p, 59.94 Hz			٠	٠			٠			VIC36_Y444_8Bit_59Hz.vgf
	2880 x 480p, 59.94 Hz			٠	٠				•		VIC36_Y444_8Bit_59Hz_RPT02.vgf
	2880 x 480p, 59.94 Hz			٠	٠					٠	VIC36_Y444_8Bit_59Hz_RPT04.vgf

 Table 13
 Video Generator Files for Test ID 8–25 (Sheet 8 of 10)

Ide CE/	Color		Color Depth Repetition				petiti	ion			
A Vic		F	orma	It			-	F	acto	r	
leo catio			УСЬ	YC b							
on Co		в	Cr4:	Cr4:	24	30	36				
ode	Video Format Timings	GB	2:2	4:4	Bit	Bit	Bit	0	2	4	File Name
	2880 x 480p, 60 Hz			•	•			•			VIC36_Y444_8Bit_60Hz.vgf
	2880 x 480p, 60 Hz			•	•				•		VIC36_Y444_8Bit_60Hz_RPT02.vgf
	2880 x 480p, 60 Hz			•	•					•	VIC36_Y444_8Bit_60Hz_RPT04.vgf
	2880 x 480p, 59.94 Hz			٠		•		٠			VIC36_Y444_10Bit_59Hz.vgf
	2880 x 480p, 59.94 Hz			•		•			•		VIC36_Y444_10Bit_59Hz_RPT02.vgf
	2880 x 480p, 59.94 Hz			•		•				•	VIC36_Y444_10Bit_59Hz_RPT04.vgf
	2880 x 480p, 60 Hz			•		•		٠			VIC36_Y444_10Bit_60Hz.vgf
	2880 x 480p, 60 Hz			•		•			•		VIC36_Y444_10Bit_60Hz_RPT02.vgf
	2880 x 480p, 60 Hz			•		•				•	VIC36_Y444_10Bit_60Hz_RPT04.vgf
	2880 x 480p, 59.94 Hz			•			•	٠			VIC36_Y444_12Bit_59Hz.vgf
	2880 x 480p, 59.94 Hz			٠			•		٠		VIC36_Y444_12Bit_59Hz_RPT02.vgf
	2880 x 480p, 59.94 Hz			٠			٠			٠	VIC36_Y444_12Bit_59Hz_RPT04.vgf
	2880 x 480p, 60 Hz			٠			٠	٠			VIC36_Y444_12Bit_60Hz.vgf
	2880 x 480p, 60 Hz			•			•		•		VIC36_Y444_12Bit_60Hz_RPT02.vgf
	2880 x 480p, 60 Hz			•			•			•	VIC36_Y444_12Bit_60Hz_RPT04.vgf
37	2880 x 576p, 50 Hz	•			٠			•			VIC37_RGB_8Bit_50Hz.vgf
	2880 x 576p, 50 Hz	٠			•				٠		VIC37_RGB_8Bit_50Hz_RPT02.vgf
	2880 x 576p, 50 Hz	٠			•					٠	VIC37_RGB_8Bit_50Hz_RPT04.vgf
	2880 x 576p, 50 Hz	•				٠		٠			VIC37_RGB_10Bit_50Hz.vgf
	2880 x 576p, 50 Hz	٠				٠			٠		VIC37_RGB_10Bit_50Hz_RPT02.vgf
	2880 x 576p, 50 Hz	٠				٠				٠	VIC37_RGB_10Bit_50Hz_RPT04.vgf
	2880 x 576p, 50 Hz	٠					•	•			VIC37_RGB_12Bit_50Hz.vgf
	2880 x 576p, 50 Hz	٠					•		٠		VIC37_RGB_12Bit_50Hz_RPT02.vgf
	2880 x 576p, 50 Hz	٠					٠			٠	VIC37_RGB_12Bit_50Hz_RPT04.vgf
	2880 x 576p, 50 Hz			٠	٠			٠			VIC37_Y444_8Bit_50Hz.vgf
	2880 x 576p, 50 Hz			•	٠				•		VIC37_Y444_8Bit_50Hz_RPT02.vgf
	2880 x 576p, 50 Hz			•	٠					•	VIC37_Y444_8Bit_50Hz_RPT04.vgf
	2880 x 576p, 50 Hz			٠		٠		٠			VIC37_Y444_10Bit_50Hz.vgf
	2880 x 576p, 50 Hz			٠		٠			٠		VIC37_Y444_10Bit_50Hz_RPT02.vgf
	2880 x 576p, 50 Hz			٠		٠				٠	VIC37_Y444_10Bit_50Hz_RPT04.vgf
	2880 x 576p, 50 Hz			٠			٠	٠			VIC37_Y444_12Bit_50Hz.vgf
	2880 x 576p, 50 Hz			٠			٠		٠		VIC37_Y444_12Bit_50Hz_RPT02.vgf
	2880 x 576p, 50 Hz			•			•			•	VIC37_Y444_12Bit_50Hz_RPT04.vgf
38	2880 x 576p, 50 Hz	٠			•			٠			VIC38_RGB_8Bit_50Hz.vgf
	2880 x 576p, 50 Hz	•			•				٠		VIC38_RGB_8Bit_50Hz_RPT02.vgf

 Table 13
 Video Generator Files for Test ID 8–25 (Sheet 9 of 10)

CEA Vi Identif		F	Color orma	t	Col	or De	pth	Re F	petit acto	ion r	
ideo ication Code	Video Format Timings	RGB	YCbCr 4:2:2	YCbCr 4:4:4	24 Bit	30 Bit	36 Bit	0	2	4	File Name
	2880 x 576p, 50 Hz	•			•					٠	VIC38_RGB_8Bit_50Hz_RPT04.vgf
	2880 x 576p, 50 Hz	•				•		•			VIC38_RGB_10Bit_50Hz.vgf
	2880 x 576p, 50 Hz	٠				•			•		VIC38_RGB_10Bit_50Hz_RPT02.vgf
	2880 x 576p, 50 Hz	٠				•				•	VIC38_RGB_10Bit_50Hz_RPT04.vgf
	2880 x 576p, 50 Hz	٠					٠	٠			VIC38_RGB_12Bit_50Hz.vgf
	2880 x 576p, 50 Hz	٠					•		•		VIC38_RGB_12Bit_50Hz_RPT02.vgf
	2880 x 576p, 50 Hz	٠					•			٠	VIC38_RGB_12Bit_50Hz_RPT04.vgf
	2880 x 576p, 50 Hz			•	•			٠			VIC38_Y444_8Bit_50Hz.vgf
	2880 x 576p, 50 Hz			•	•				•		VIC38_Y444_8Bit_50Hz_RPT02.vgf
	2880 x 576p, 50 Hz			•	•					•	VIC38_Y444_8Bit_50Hz_RPT04.vgf
	2880 x 576p, 50 Hz			•		•		٠			VIC38_Y444_10Bit_50Hz.vgf
	2880 x 576p, 50 Hz			•		•			•		VIC38_Y444_10Bit_50Hz_RPT02.vgf
	2880 x 576p, 50 Hz			٠		٠				٠	VIC38_Y444_10Bit_50Hz_RPT04.vgf
	2880 x 576p, 50 Hz			•			•	٠			VIC38_Y444_12Bit_50Hz.vgf
	2880 x 576p, 50 Hz			•			•		•		VIC38_Y444_12Bit_50Hz_RPT02.vgf
	2880 x 576p, 50 Hz			٠			٠			٠	VIC38_Y444_12Bit_50Hz_RPT04.vgf

Table 13Video Generator Files for Test ID 8–25 (Sheet 10 of 10)



Agilent U4998A HDMI/MHL Protocol/Audio/Video Analyzer and Generator User Guide

Debugging Source and Sink Devices

Overview 124

This chapter provides information on how you can use U4998A to debug source and sink devices.



5 Debugging Source and Sink Devices

Overview

You can use U4998A to debug problems encountered when a source and a sink DUT are connected. The following figure illustrates the broad steps that you need to perform to use U4998A as a pass through device between a HDMI source and sink DUT for debugging these DUTs.





The tasks displayed in the above figure are described later in this topic.

Refer to the topic "U4998A Roles and Usage Scenarios" on page 17 to get a pictorial representation of U4998A for debugging source and sink devices.

Configuring U4998A Data Capture Settings

You use the **U4998A-Pass-through** connection mode to use U4998A as a pass through device and passively capture signals between an HDMI source and a sink DUT for debugging purposes. You need the U4998A-PSV or U4998U-PSV license to use this mode.

The pass-through connection mode of U4998A is effective when debugging the connected HDMI source and sink DUTs. The TMDS signals are transmitted from the source to the sink DUT in this case and U4998A can passively capture these signals to analyze and troubleshoot a problem. You can also use other modes (Capture, Generator, or Mirror) of U4998A to debug a source or a sink DUT individually. However, these modes are more effective in HDMI/MHL Compliance testing of a source or a sink DUT.

Refer to the topic "Setting up a Connection between U4998A and DUT" on page 34 to know how to set the connection mode using the Logic and Protocol Analyzer GUI.

Connecting U4998A to DUTs

Make the required hardware connections to connect U4998A to the source and sink DUTs. Connect the source DUT to the HDMI IN connector and sink DUT to HDMI Out connector of U4998A.

EDID Block of the Sink DUT

The source DUT is connected to the sink DUT through U4998A in case of pass through scenario of U4998A. The TMDS signals are transmitted from the source to the sink DUT in this case. Therefore, the source DUT reads the EDID of the sink DUT and not U4998A in this case.

Resetting the Hot Pug Detect Mechanism from U4998A

While debugging DUTs using the pass-through mode, there may be situations when you need the DUT to reperform the initialization sequence. In such a situation, you can perform the Hot Plug Detect (HPD) reset from U4998A. This eliminates the need for removing and reconnecting the HDMI cables while debugging DUTs. You use the Logic and Protocol Analyzer GUI to reset the HPD from U49998A.

To reset the HPD

- **1** Access the U4998A Setup dialog box in the Logic and Protocol Analyzer GUI.
- 2 Click the Capture Setup tab.
- 3 Click the **Reset** button displayed with the **Hot Plug Detect (HPD)** field.
- 4 Click OK.

Starting the Data Capture and Uploading the Captured Data

Once you have configured the hardware setup and connection and capture settings of U4998A, you can start capturing the data transmitted from the source to the sink DUT. You use the Logic and Protocol Analyzer GUI to start the data capture.

To start the data capture

- 1 Access the Logic and Protocol Analyzer GUI in the online mode.
- 2 Click the Run toolbar button.

When you start the data capture, the captured data is stored in the memory of the U4998A module from where you can upload it into a specified .cap file. To know about uploading the captured data, refer to the topic "Uploading the Captured data in a File" on page 62.

Importing Captured Data into Agilent Logic and Protocol Analyzer

Once the captured data is uploaded in the specified .cap file, you can import this .cap file into the Agilent Logic and Protocol Analyzer GUI. To do this, you need to first convert the .cap file into a module CSV file and then import it in the Agilent Logic and Protocol Analyzer GUI as a data import module to debug and analyze the data. To know more, refer to the topic "Importing Captured Data into Agilent Logic and Protocol Analyzer for further Analysis" on page 78.

Viewing the Converted Data in Logic and Protocol Analyzer for Debugging

Refer to the topic "Viewing the Converted Data in Logic and Protocol Analyzer" on page 90 to know how you can view the data that you converted from the .cap file into a module CSV file in Logic and Protocol Analyzer GUI.

5 Debugging Source and Sink Devices



Agilent U4998A HDMI/MHL Protocol/Audio/Video Analyzer and Generator User Guide

Using COM Interface for HDMI/MHL Testing

Overview 132 Before you start 133 Method for Configuring U4998A Settings 135 Methods for Capturing HDMI/MHL Data 153 Methods for Evaluating the Captured Data 156 Methods for Generating HDMI/MHL Data 159 Status 161 WaitReady 162

This chapter describes how you can configure, control, and use U4998A using COM interface for performing automated HDMI/MHL testing.



Overview

Besides using the U4998A's GUI components, you can also use the COM interface to configure, control, and use U4998A. The COM Interface allows you to write programs to automate HDMI/MHL testing.

This chapter describes the COM APIs as per the following three broad areas of their usage in the context of HDMI/MHL testing.

- Generate HDMI/MHL data
- Capture HDMI/MHL data
- Evaluate the captured data for HDMI/MHL compliance

The topics that follow describe how to use COM APIs to perform these tasks.

The following is the list of methods described in this chapter.

- "DoCommands
- "ExportCapture
- "GetBitmapFiles
- "GetTMDSClockValue
- "HPDReset
- "LEDRefresh
- "StartCapture
- "StartGenerator
- "StartEvaluate
- "Status
- "StopGenerator
- "WaitReady
- "WriteEDID

Before you start

To use the COM interface, you need to ensure that the following software components of U4998A are installed:

- Agilent Logic and Protocol Analyzer You need this software component for capturing as well as generating HDMI/MHL data.
- **HDMI/MHL Evaluator** You need this component for evaluating the captured HDMI/MHL data in an offline mode, that is without connecting to U4998A hardware.
- U4998A HDMI/MHL Video Generator Files You need this component to get a set of predefined .vgf and .aaf files that you can transmit to a DUT. Separate installers are available for HDMI and MHL Video Generator files.

COM Servers

The following two COM servers are applicable to automate HDMI/MHL testing.

• Agilent Logic Analyzer COM Server - This is typically installed at:

C:\Program Files (x86)\Agilent Technologies\Logic Analyzer\agClientSvr.dll

While using this COM Server, ensure that:

- The COM server connects to a local instance of the Agilent Logic and Protocol Analyzer application. If the Logic and Protocol Analyzer application is not started, the COM server's Connect command starts it.
- You store the capture (.cap) files and the Generator (.vgf and .aaf) files on the PC that is connected to the U4998A module. Typically, you store these files on the controller PC that has all the required software components of U4998A and is connected to the Agilent AXIe chassis via a PCIe interface. This is important to remember when you are using a remote connection to the U4998A hardware.
- **HDMI Evaluator COM Server** This COM server is embedded in the HDMI/MHL Evaluator application, which is typically installed in the following folder:

C:\Program Files\HDMI Evaluator\ HDMIProtocolAnalyzer.exe When you create an HDMI Evaluator COM object, it starts the HDMIProtocolAnalyzer.exe in the COM Server mode without a graphical user interface. While using this COM Server, ensure that:

- Only one instance of HDMIProtocolAnalyzer.exe is running.
- If you try to create an HDMI Evaluator COM object and run the HDMI/MHL Evaluator application simultaneously, the operation will fail.

Examples on Usage

For examples on using the COM servers, refer to the following folders:

Logic Analyzer COM Server (for capturing and transmitting HDMI/MHL data)	C:\Program Files (x86)\Agilent Technologies\Logic Analyzer\LA COM Automation\Visual C++ Examples\ HDMI
HDMI Evaluator COM Server (for offline evaluation of the captured data)	C:\Program Files\HDMI Evaluator\ Examples

Method for Configuring U4998A Settings

DoCommands

Applicable COM Server Object

Use this method with the Agilent Logic Analyzer COM Server and HDMI Evaluator COM Server objects as per the following table.

To configure HDMI/MHL connection, capture, and generator settings	Logic Analyzer COM Server object
To configure settings for the offline evaluation of the captured data	HDMI Evaluator COM Server object

Syntax

VARIANT_BOOL DoCommands ([in] BSTR XMLCommand);

Description

This method configures the settings needed to create the HDMI/MHL connection and to capture, evaluate, and generate HDMI/MHL data. For instance, this method configures the U4998A module's memory depth that you want to use for storing the captured data.

The DoCommands method requires an XMLCommand argument that is formed from XML elements which are described as follows.

XML Elements Hierarchy for DoCommands

The DoCommands method requires an XML-based string as the argument, XMLCommand. The XMLCommand string configures the HDMI/MHL settings for capture, evaluate, and generate tasks. You build the XML string using the elements documented in this section. If you're not familiar with writing XML, there are many widely available introductory books as well as web sites.

Element Hierarchy

The following list displays the hierarchy of the XML elements. The element <Module> is the root element. Under <Module>, there are <Connection>, <Capture>,

<Evaluate>, and <Generate> elements to configure the connection, capture, evaluate, and generate settings respectively. Each of these elements has its own descendants, for example, <Add/> is a descendant of <Evaluate> but not of <Generate>.

```
<Module>
  <Connection> See "<Connection> Element,
 page 138
  <Capture> See "<Capture> Element, page 139
  <Evaluate> See "<Evaluate> Element and its
 Descendants, page 140
   <Protocol/>
   <TestID>
     <Add/>
     <Clear/>
     <Full/>
     <Remove>
     <Set>
   <MHLTestID>
     <Add/>
     <Clear/>
     <Full/>
     <Remove>
     <Set>
   <Color/>
   <Options>
  <Generate> See "<Generate> Element and its
 Descendants, page 150
   <Audio/>
   <Vidio/>
```

Creating XML Command Strings

The XMLCommand string must start and end with the root element <Module>.

<Module Name='MyModule'> ... <Module>

The <Module> element must include the attribute Name. Note that this attribute is parsed but not used.

Elements that have content, like <Module>, must use both an open tag and a closed tag with all of their content between the tags. Empty elements are elements that have no content (child elements or text, for example). You can optionally write an empty element by closing the start tag with /> and omitting an end tag. For example, the <Set> element has no content <Set></Set>

and can be optionally written as:

```
<Set/>
```

Element attributes are used to set specific settings. In the following example, the attribute Format has a value of RGB. Notice the required quotes on the attribute value. These can be double or single quotes.

<Color Format='RGB' Depth='24'/>

Notice that <Color> is considered an empty element (has no child element), even though it has attributes.

XML is case sensitive, so be sure to create your strings using the exact upper and lower-case letters shown in this section.

Four elements are children of the <Module> element: <Connection>, <Capture>, <Evaluate>, and <Generate>. These elements and their descendants configure the settings in the U4998A's connection, Capture, and Generator windows respectively.

In the following example fragment, an XML command string is initialized and used in a DoCommands method. Since double quotes are used to declare the string, single quotes must be used to specify all attribute values within the XML. Notice that indented code lines indicate element parent-child relationships. For example, <Evaluate> has the <TestID> child and the <Clear> descendant (grandchild) element.

```
<Module Name='MyModule'>
<Capture Clock='25' Size='100' File='C:\
MyFile.cap' Protocol='HDMI'/>
<Generate>
...
</Generate>
<Evaluate>
<TestID>
<Clear/>
</TestID>
...
</Evaluate>
</Module>
```

"... DoCommands([in] xml_command_string);

<Module> Element

<Module> is the root element. It contains child elements of <Connection>, <Capture>, <Evaluate>, and <Generate>.

Child Elements - <Connection>, <Capture>, <Evaluate>,
 <Generate>

Parent Elements - none

Attributes

Name	Value	Description
Name	HDMI Evaluator	Required attribute.
	wywodule	used.

Example

```
<Module Name='MyModule'>
<Evaluate>
<Protocol Name='HDMI'/>
</Evaluate>
</Module>
```

<Connection> Element

NOTE

Check that you have installed the Agilent Logic Analyzer software to configure the connection capabilities. Refer to the *AXIe Based Protocol Testing and Logic Analysis Modules Installation Guide* to know more about installation. This guide is available on www.agilent.com.

The <Connection> element sets the HDMI/MHL connection type.

This element does not have any children.

Child Elements - none

Parent Element - <Module>

Attributes

Name	Value	Description
Setup	Generate	Sets the connection in the generator mode. Effective for HDMI/MHL compliance testing of a sink device.
	Capture	Sets the connection in the capture and analyzer mode. Effective for HDMI/MHL compliance testing of a source device.
	Pass-through	Sets the connection in the pass-through mode. Effective for debugging HDMI/MHL source and sink DUTs.
	Mirror	Sets the connection in the mirror mode. Effective for HDMI/MHL compliance testing of a source device.

To know about these connection modes in detail, refer to the topic "U4998A Roles and Usage Scenarios" on page 17.

Example

```
<Module Name='MyModule'>
<Connection Setup='Generate'/>
</Module>
```

<Capture> Element

NOTE

Check that you have installed the Agilent Logic and Protocol Analyzer software to configure the capture capabilities. Refer to the *AXle Based Protocol Testing and Logic Analysis Modules Installation Guide* to know more about installation. This guide is available on www.agilent.com.

The <Capture> element selects HDMI/MHL capture settings such as Pixel Clock frequency and memory depth of U4998A module for storing the captured data. The <Capture> element does not have any children.

Child Elements - none

Parent Element - <Module>

Attributes

Name	Value	Description
Clock		The Clock attribute is parsed but not used in U4998A.
	25	25 to 74.999 MHz HDMI pixel clock
	75	75 to 129.999 MHz HDMI pixel clock
	130	130 to 164.999 MHz HDMI pixel clock
	165	165 to 224.999 MHz HDMI pixel clock
File	file name	File name including path. Example: C:\ Capture\MyFile.cap
Size	integer	Size in megabytes (MB).
Protocol	DVI HDMI MHL	The protocol (DVI, HDMI, or MHL) to indicate whether you want to capture DVI, HDMI, or MHL data. The default is HDMI.

Example

```
<Module Name='MyModule'>
<Capture Clock='25' Size='100' File='C:\Capture\
MyFile.cap' Protocol='HDMI'/>
</Module>
```

<Evaluate> Element and its Descendants

NOTE

Check that you have installed the HDMI Evaluator software to run source tests for HDMI compliance. Refer to the *AXle Based Protocol Testing and Logic Analysis Modules Installation Guide* to know more about installation. This guide is available on www.agilent.com.

The <Evaluate> element contains child elements that are used to specify settings for HDMI/MHL evaluation. The <Evaluate> element's attributes are used to specify the captured HDMI/MHL data file for evaluation, the Video Identification Code (VIC), and the TMDS clock frequency.

Child Elements

The following element hierarchy displays all the available elements:

```
<Evaluate>
<Color/>
<Content/>
<Options>
<PacketLog>
```

```
<Add/>
 <Clear/>
 <Remove/>
 <Set/>
<Protocol/>
<Quantization/>
<TestID>
 <Add/>
 <Clear/>
 <Full/>
 <Remove>
 <Set>
<MHLTestID>
 <Add/>
 <Clear/>
 <Full/>
 <Remove>
 <Set>
```

Parent Element - <Module>

Attributes

Name	Value	Description
Clock	frequency	TMDS clock frequency between 25 MHz and 225 MHz in Hertz. Example: 27027000
File	file name	File name including path. Example: C:\ Capture\MyFile.cap
Format	Refer to Table 14 on page 143 for a listing of attribute values.	Video identification code string

Example

```
<Module Name='HDMI Evaluator'>

<Evaluate Clock='27027000' Format='1 :

640x480p 59.94Hz'

File='C:\Capture\MyFile.cap'>

<TestID>

<Set/>

<Clear/>

<Full/>

<Remove Name='7-16'/>

<Add Name='7-34'/>

<Add Name='7-36'/>

</TestID>

<PacketLog>
```

```
<Set/>
    <Clear/>
    <Add Name='NUL'/>
    <Remove Name='NULL'/>
    </PacketLog>
    <Content Type='None'/>
    <Quantization Range='Either'/>
    <Protocol Name='DVI'/>
    <Color Format='RGB' Depth='24'/>
    <Options AVI='1' Audio='0' ACP='0'
ThreeD='0' VSDB='0'
    Colorimetry='0'GreaterTwo='0'/>
    </Evaluate>
</Module>
```

CEA Video		CEA Video	
ID Code	Format Attribute Value	ID Code	Format Attribute Value
1	1 : 640x480p @ 59.94 Hz	22	22 : 720(1440)x576i @ 50 Hz
	1 : 640x480p @ 60 Hz	23	23 : 720(1440)x288p @ 50 Hz
2	2 : 720x480p @ 59.94 Hz	24	24 : 720(1440)x288p @ 50 Hz
	2 : 720x480p @ 60 Hz	25	25 : 2880x576i @ 50 Hz
3	3 : 720x480p @ 59.94 Hz	26	26 : 2880x576i @ 50 Hz
	3 : 720x480p @ 60 Hz	27	27 : 2880x288p @ 50 Hz
4	4 : 1280x720p @ 59.94 Hz	28	28 : 2880x288p @ 50 Hz
	4 : 1280x720p @ 60 Hz	29	29 : 1440x576p @ 50 Hz
5	5 : 1920x1080i @ 59.94 Hz	30	30 : 1440x576p @ 50 Hz
	5 : 1920x1080i @ 60 Hz	31	31 : 1920x1080p @ 50 Hz
6	6 :720(1440)×480i @ 59.94 Hz	32	32 : 1920x1080p @ 23.98 Hz
	6 : 720(1440)x480i @ 60 Hz		32 : 1920x1080p @ 24 Hz
7	7 :720(1440)×480i @ 59.94 Hz	33	33 : 1920x1080p @ 25 Hz
	7 : 720(1440)x480i @ 60 Hz	34	34 : 1920x1080p @ 29.97 Hz
8	8 : 720(1440)x240p @ 59.94 Hz		34 : 1920x1080p @ 30 Hz
	8 : 720(1440)x240p @ 60 Hz	35	35 : 2880x480p @ 59.94 Hz
9	9 : 720(1440)x240p @ 59.94 Hz		35 : 2880x480p @ 60 Hz
	9 : 720(1440)x240p @ 60 Hz	36	36 : 2880x480p @ 59.94 Hz
10	10 : 2880x480i @ 59.94 Hz		36 : 2880x480p @ 60 Hz
	10 : 2880x480i @ 60 Hz	37	37 : 2880x576p @ 50 Hz
11	11 : 2880x480i @ 59.94 Hz	38	38 : 2880x576p @ 50 Hz
	11 : 2880x480i @ 60 Hz	39	39 : 1920x1080i (1250 total) @ 50 Hz
12	12 : 2880x240p @ 59.94 Hz	40	40 : 1920x1080i @ 100 Hz
	12 : 2880x240p @ 60 Hz	41	41 : 1280x720p @ 100 Hz
13	13 : 2880x240p @ 59.94 Hz	42	42 : 720x576p @ 100 Hz
	13 : 2880x240p @ 60 Hz	43	43 : 720x576p @ 100 Hz
14	14:1440x480p @ 59.94 Hz	44	44 : 720(1440)x576i @ 100 Hz
	14:1440x480p@60Hz	45	45 : 720(1440)x576i @ 100 Hz
15	15:1440x480p @ 59.94 Hz	46	46 : 1920x1080i @ 119.88 Hz
16	16 : 1920x1080p @ 59.94 Hz		46 : 1280x720p @ 120 Hz
	16 : 1920x1080p @ 60 Hz	47	47 : 1920x1080i @ 119.88 Hz
17	17 : 720x576p @ 50 Hz		47 : 1280x720p @ 120 Hz
18	18 : 720x576p @ 50 Hz	48	48 : 720x480p @ 119.88 Hz
19	19 : 1280x720p @ 50 Hz		48 : 720x480p @ 120 Hz
20	20 : 1920×1080i @ 50 Hz	49	49 : 720x480p @ 119.88 Hz
21	21 : 720(1440)×576i @ 50 Hz		49 : 720x480p @ 120 Hz

 Table 14
 VIC Attribute Values for <Evaluate> and <Video> Elements (Sheet 1 of 2)

6 Using COM Interface for HDMI/MHL Testing

CEA Video		CEA Video	
ID Code	Format Attribute Value	ID Code	Format Attribute Value
50	50 : 720(1440)x480i @ 119.88H Hz	64	64 : 1920x1080p @ 100Hz
	50 : 720(1440)x480i @ 120 Hz	H01	H01 : 3840x2160p @ 29.97Hz
51	51 : 720(1440)x480i @ 119.88H Hz		H01 : 3840x2160p @ 30Hz
	51 : 720(1440)x480i @ 120 Hz	H02	H02 : 3840x2160p @ 25Hz
52	52 : 720x576p @ 200 Hz	H03	H03 : 3840x2160p @ 23.98Hz
53	53 : 720x576p @ 200 Hz		H03 : 3840x2160p @ 24Hz
54	54 : 720(1440)×576i @ 200 Hz	H04	H04 : 40896x2160p @ 24Hz
55	55 : 720(1440)x576i @ 200 Hz		
56	56 : 720x480p @ 239.76 Hz		
	56 : 720x480p @ 240 Hz		
57	57 : 720x480p @ 239.76 Hz		
	57 : 720x480p @ 240 Hz		
58	58 : 720(1440)x480i @ 239.76 Hz		
	58 : 720(1440)x480i @ 240 Hz		
59	59 : 720(1440)x480i @ 239.76 Hz		
	59 : 720(1440)x480i @ 240 Hz		
60	60 : 1280x720p @ 23.98 Hz		
	60 : 1280x720p @ 24 Hz		
61	61 : 1280x720p @ 25 Hz		
62	62 : 1280x720p @ 29.97 Hz		
	62 : 1280x720p @ 30 Hz		
63	63 : 1920x1080p @ 119.88Hz		
	63 : 1920x1080p @ 120Hz		

 Table 14
 VIC Attribute Values for <Evaluate> and <Video> Elements (Sheet 2 of 2)

<Add> Element

Adds a test for evaluation.

Child Elements - none

Parent Elements - <TestID>, <MHLTestID>, <PacketLog>

Attributes

Name	Values	Description			
When <add< td=""><td>d> is a child of <testi< td=""><td>)></td></testi<></td></add<>	d> is a child of <testi< td=""><td>)></td></testi<>)>			
Name	7-16 7-17 7-18 7-19 7-23 7-24 7-25 7-26 7-27 7-28 7-29 7-30 7-31 7-32 7-33 7-34 7-35 7-36 7-37 7-38 7-39 7-40	A single Test ID. Example: 7-16			
When <add< td=""><td>d> is a child of <mhlt< td=""><td>estID></td></mhlt<></td></add<>	d> is a child of <mhlt< td=""><td>estID></td></mhlt<>	estID>			
Name	3.2.2.1 3.2.2.2 3.2.2.3 3.2.3.1 3.2.3.2 3.2.3.3 3.2.3.4 3.2.4.1 3.2.4.2 3.2.4.3	A single MHL Test ID. Example: 3.2.2.1			
When <add< td=""><td>d> is a child of <packe< td=""><td>etLog></td></packe<></td></add<>	d> is a child of <packe< td=""><td>etLog></td></packe<>	etLog>			
Name	NUL	Null Packet			
	ACP	ACP Packet			
	ACR	ACR Packet			
	AIF	Audio InfoFrame Packet			
	ASP	Audio Sample Packet			
	AVI	Auxiliary Video InfoFrame Packet			
	DST	Direct Stream Transport Audio Packet			
	GCP	General Control Packet			
	GMP	Gamut Metadata Packet			
	HBR	High Bit Rate Audio Stream Packet			
	ILL	Illegal Packet Type			
	IS1	ISRC1 Packet			
	IS2	ISRC2 Packet			
	MPG	MPEG Source InfoFrame Packet			
	OBA	One Bit Audio Sample Packet			
	SPD	Source Product Description InfoFrame Packet			
	VSI	Vendor Specific InfoFrame Packet			

Example

<Add Name='7-16'/>

<Clear> Element

Clears all HDMI/MHL tests from HDMI/MHL evaluation. Clears all packet selections from the Packet Log.

Child Elements - none

Parent Elements - <TestID>, <MHLTestID>, <PacketLog>

Attributes - none

<Color> Element

Sets the color format and depth for HDMI/MHL evaluation.

Child Elements - none

Parent Elements - <Evaluate>

Attributes

Name	Value	Description			
Format	AdobeRGB	Color space used in video.			
	AdobeYCC601				
	RGB	-			
	sYCC601	_			
	xvYCC				
	YCbCr(4:2:2)	_			
	YCbCr(4:4:4)	_			
Depth	24	24 bit color depth			
	30	30 bit color depth			
	36	36 bit color depth			
	48	48 bit color depth			

Example

<Color Format='RGB' Depth='24'/>

<Content> Element

Sets the type of video content.

Child Elements - none

Parent Elements - <Evaluate>

Attributes

Name	Value	Description
Туре	None	Type of video content.
	Cinema	
	Game	
	Graphics	
	Photo	
Example

<Content Type='Cinema'/>

<Full> Element

Includes a set of HDMI/MHL tests that are used for full HDMI/MHL compliance. The included tests are as follows:

For full HDMI compliance - 7-16, 7-17, 7-18, 7-19, 7-25, 7-26, 7-28, 7-29, 7-30, 7-31, and 7-32.

For full MHL compliance - 3.2.2.1, 3.2.2.2, 3.2.2.3, 3.2.3.1, 3.2.3.3, 3.2.4.1, 3.2.4.2, 3.2.4.3

Child Elements - none

Parent Elements - <TestID>

Attributes - none

<Options> Element

Sets various options for evaluation of HDMI/MHL data, including AVI InfoFrame Packet, Audio, ACP, ISRC1, ISRC2 Packet, and 3D Video Format.

Child Elements - none

Parent Elements - <Evaluate>

Attributes

Name	Value	Description (Select or Disables)
AVI	0 or 1	AVI InfoFrame packet
Audio	0 or 1	Audio
ACP	0 or 1	ACP, ISRC1, and ISRC2 packet
ThreeD	0-3	0 = 2D video format
		1 = Frame Packing 3D video format 2 = Side-by-Side (Half) 3D video format 3 = Top-and-Bottom 3D video format
VSDB	0 or 1	HDMI VSDB Length = 5
Colorimetry	0 or 1	Colorimetry Data Block Byte #3 = 0
GreaterTwo	0 or 1	2-Channel PCM Audio

Example

```
<Options AVI='1' Audio='0' ACP='0' ThreeD='0'
VSDB='0' Colorimetry='0'GreaterTwo='0' />
```

<PacketLog> Element

Container element for selections for the packet log.

Child Elements - <Add>, <Clear>, <Remove>, <Set>

Parent Elements - <Evaluate>

Attributes - none

<Protocol> Element

Sets the HDMI, MHL, or DVI as the protocol while capturing data.

Child Elements - none

Parent Elements - <Evaluate>

Attributes

Name	Value	Description
Name	DVI	Digital Visual Interface protocol
	HDMI	HDMI protocol
	MHL	MHL protocol

Example

<Protocol Name='HDMI'/>

<Quantization> Element

Sets the range of quantization (lossy compression) present on the video.

Child Elements - none

Parent Elements - <Evaluate>

Attributes

Name	Value	Description
Range	Either	Can be either limited range or full range.
	Full	Full quantization range
	Limited	Limited quantization range

Example

<Quantization Range='Either'/>

<Remove> Element

Removes a test from the HDMI/MHL evaluation. Removes a packet type from the Packet Log.

Child Elements - none

Parent Elements - <TestID>, <MHLTestID>, <PacketLog>

Attributes

Name	Value	Description
When <r< td=""><td>emove> is a child of <testid></testid></td><td></td></r<>	emove> is a child of <testid></testid>	
Name	7-16 7-17 7-18 7-19 7-23 7-24 7-25 7-26 7-27 7-28 7-29 7-30 7-31 7-32 7-33 7-34 7-35 7-36 7-37 7-38 7-39 7-40	A single Test ID. For example: 7-16
When <r< td=""><td>emove> is a child of <mhltestid></mhltestid></td><td></td></r<>	emove> is a child of <mhltestid></mhltestid>	
Name	3.2.2.1 3.2.2.2 3.2.2.3 3.2.3.1 3.2.3.2 3.2.3.3 3.2.3.4 3.2.4.1 3.2.4.2 3.2.4.3	A single MHL Test ID. For example: 3.2.2.1
When <r< td=""><td>emove> is a child of <packetlog></packetlog></td><td></td></r<>	emove> is a child of <packetlog></packetlog>	
Name	NUL	Null Packet
	ACP	ACP Packet
	ACR	ACR Packet
	AIF	Audio InfoFrame Packet
	ASP	Audio Sample Packet
	AVI	Auxiliary Video InfoFrame Packet
	DST	Direct Stream Transport Audio Packet
	GCP	General Control Packet
	GMP	Gamut Metadata Packet
	HBR	High Bit Rate Audio Stream Packet
	ILL	Illegal Packet Type
	IS1	ISRC1 Packet
	IS2	ISRC2 Packet
	MPG	MPEG Source InfoFrame Packet
	OBA	One Bit Audio Sample Packet
	SPD	Source Product Description InfoFrame Packet
	VSI	Vendor Specific InfoFrame Packet

Example

<Remove Name='7-16'/>

<Set> Element

Selects all the Test IDs for HDMI/MHL evaluation. Selects all packet types for the Packet Log.

Child Elements - none

Parent Elements - < TestID>, < MHLTestID>, < PacketLog>

Attributes - none

<TestID> Element

Container element for evaluation test selection.

Child Elements - <Add>, <Clear>, <Full>, <Remove>, <Set>

Parent Elements - <Evaluate>

Attributes - none

<Generate> Element and its Descendants

NOTE

Check that you have installed the U4998A HDMI Video Generator Files software to use the .vgf and .aaf files mentioned in this section. Refer to the *AXIe Based Protocol Testing and Logic Analysis Modules Installation Guide* to know more about installation. This guide is available on www.agilent.com.

The <Generate> element contains child elements that are used to specify settings for the HDMI/MHL video timing generator.

Child Elements

The following element hierarchy shows all the available elements:

<Generate> <Video> <Audio>

Parent Elements - <Module>

Attributes - none

Example

```
<Module Name='MyModule'>

<Generate>

<Video File='C:\Capture\MyFile.vgf'

Deviation='+'/>

<Audio With='0'/>

</Generate>

</Module>
```

<Audio> Element

Enables (and disables) audio output and selects an audio data file. You can specify the audio files (.aaf files) from the set of predefined audio files installed at the following folders:

- C:\Users\Public\Documents\Agilent Technologies\ Logic Analyzer\MHL\Generator Data\Audio Files
- C:\Users\Public\Documents\Agilent Technologies\ Logic Analyzer\HDMI\Generator Data\

Child Elements - none

Parent Elements -<Generate>

Attributes

Name	Value	Description
File	<file name=""></file>	Example: C:\Users\Public\Documents\Agilent Technologies\Logic Analyzer\HDMI\Generator Data\8-23 Audio Formats[16bit]L=1kHz_R= 1kHz@32kHz_No1.agf
With	0 or 1	Generate with audio enable or disable
D	300 - 1500	D parameter used in (128 x fs / D)

Example

```
<Audio File='C:\Users\Public\Documents\Agilent
Technologies\Logic Analyzer\HDMI\Generator
Data\Audio Files\8-23 Audio
Formats[16bit]L=1kHz_R=1kHz@32kHz_No1.agf'
With='1' D='300'/>
```

<Video> Element

Specifies video file and Video Identification Code (VIC) for HDMI/MHL video timing generator output.

Child Elements - none

Parent Elements - <Generate>

Attributes

Name	Value	Description
File	<file name=""></file>	Example: C:\Capture\MyFile.vgf
Deviation	0 or + or –	Sets the deviation from the standard TMDS clock frequency to 0%, +0.5%, or –0.5%.

Example

<Video File='C:\Capture\MyFile.vgf' Deviation='+'/>

Methods for Capturing HDMI/MHL Data

NOTE

Check that you have installed Agilent Logic and Protocol Analyzer software to use the methods described in this topic. Refer to the *AXle Based Protocol Testing and Logic Analysis Modules Installation Guide* to know more about installation. This guide is available on www.agilent.com.

WriteEDID

Applicable COM Server Object

Use this method with the Agilent Logic Analyzer COM server object.

Syntax

VARIANT BOOL WriteEDID([in] BSTR EDIDFileName);

Description

Defines the EDID for the U4998A module when it emulates a sink device. The method defines the EDID as per the specified .edi file. This method returns when the write is complete.

Parameter	Description
[in] BSTREDIDFileName	The full path and name of the EDID file that you want to use to define the EDID for the U4998A module.

Failures can occur with the following causes:

- The specified EDIDFileName is not valid.
- U4998A module is not connected to the controller PC.

HPDReset

Applicable COM Server Object

Use this method with the Agilent Logic Analyzer COM Server object.

Syntax

void HPDReset();

Description

Forces the emulation of the Hot Plug Detect mechanism. On executing this command, DUT reperforms the initialization sequence without going through the Hot Plug Detect with U4998A. This is particularly useful in instances such as forcing the DUT to read the updated or changed EDID block of U4998A as a part of the initialization sequence. DUT reads the EDID block of U4998A immediately on getting connected. If you have updated the EDID block after connection, then executing this command before starting the capture can serve the purpose of forcing the DUT to read the updated EDID.

StartCapture

Applicable COM Server Object

Use this method with the Agilent Logic Analyzer COM Server object.

Syntax

VARIANT BOOL StartCapture();

Description

Starts capturing HDMI/MHL data from the source DUT into the U4998A module memory. When connected, the U4998A module is ready to capture data. Therefore, the capture starts immediately without any waiting time needed for the hardware to be ready for capture.

This method returns when the capture is complete. Failures can occur when the U4998A module is not connected to the controller PC.

You can use the Status() to find out if the capture has completed.

NOTE

You cannot simultaneously generate and capture data.

LEDRefresh

Applicable COM Server Object

Use this method with the Agilent Logic Analyzer COM Server object.

Syntax

void LEDRefresh();

Description

Refreshes the status of the TMDS data channel LEDs for the HDMI IN connector on the front panel of the U4998A module.

ExportCapture

Applicable COM Server Object

Use this method with the Agilent Logic Analyzer COM Server object.

Syntax

VARIANT_BOOL ExportCapture([in] BSTR
ExportFileName);

Description

Exports the captured data to the specified .cap file. ExportCapture() returns when the export completes or when a write to ExportFileName fails. Failures can occur with the following causes:

- ExportFileName is not valid.
- Upload size is less than 1 or greater than 4096 MB.
- U4998A hardware is not connected to the controller PC.
- No data has been captured

Parameter	Description
[in] BSTR ExportFileName	The full path and name of the .cap file in which you want to export the data captured from a source DUT.

Methods for Evaluating the Captured Data

NOTE

Check that you have installed the HDMI/MHL Evaluator software to use the methods described in this topic. Refer to the *AXIe Based Protocol Testing and Logic Analysis Modules Installation Guide* to know more about installation. This guide is available on www.agilent.com.

GetBitmapFiles

Applicable COM Server Object

You need to use this method with the HDMI Evaluator COM Server object. If you use this method with the Agilent Logic Analyzer COM server object, it returns an empty string.

Syntax

BSTR GetBitmapFiles();

Description

The tests 7-23, 7-24, 7-27, 7-34, 7-38, and 7-40 can generate image files. The GetBitmapFiles method returns the names of any image files created in the last call to StartEvaluate(). Only one of these tests should be run per call to StartEvaluate(). The file names (in the order created) are returned in an XML string as shown in this example:

```
<Bitmap>
<File Name='C:\Capture\
MyFile_0_20091020134237.bmp'/>
<File Name='C:\Capture\
MyFile_1_20091020134239.bmp'/>
</Bitmap>
```

GetTMDSClockValue

Applicable COM Server Object

You need to use this method with the Agilent Logic Analyzer COM server object.

Syntax

BSTR GetTMDSClockValue();

Description

Some HDMI source tests such as 7-25 and 7-29 require you to specify the TMDS Clock frequency while running these tests. The GetTMDSClockValue method returns the currently detected TMDS clock frequency as displayed in the **Detected TMDS Clock** field in the **Capture Setup** tab of Logic and Protocol Analyzer GUI. You can use the returned value to input the clock frequency into the HDMI Evaluator software.

StartEvaluate

Applicable COM Server Object

Use this method with the HDMI Evaluator COM Server object. If you use this method with the Agilent Logic Analyzer COM server object, it always returns false.

Syntax

```
VARIANT_BOOL StartEvaluate([in] BSTR
EvaluatorFileName, [in] BSTR
PacketLogFileName, [in] VARIANT_BOOL
ImageDialog);
```

Description

Starts the HDMI Evaluator. Use the DoCommands method to specify the input filename of captured data and all options.

Parameter	Description
[in] BSTR EvaluatorFileName	The path and name of the file where the evaluation results will be saved.
[in] BSTR PacketLogFileName	The path and name of the file where the packet log results will be saved. The packet log is produced only for the test 7-19.

Parameter	Description
[in] VARIANT_BOOL ImageDialog	Set the argument to true to enable the Video Image window so that you can visually inspect each video frame. Set the argument to false to disable the Video Image window. Video Image window applies to tests 7-23, 7-24, 7-27, 7-34, 7-38, and 7-40.

This method returns when the evaluation completes. However, if you set the ImageDialog parameter to true, this method will not return until you complete input to the Video Image window.

The method fails if you do not set up any tests to run on the captured data using the DoCommands method. Refer to "Viewing the Video Image" on page 74 to learn about the Image window.

NOTE

You do not need U4998A module or any license to evaluate a captured data file. The evaluation is done in an offline mode using HDMI Evaluator.

Methods for Generating HDMI/MHL Data

NOTE

Check that you have installed Agilent Logic and Protocol Analyzer and U4998A HDMI/MHL Video Generator Files software components to use the methods described in this topic. Refer to the *AXle Based Protocol Testing and Logic Analysis Modules Installation Guide* to know more about installation. This guide is available on www.agilent.com.

StartGenerator

Applicable COM Server Object

Use this method with the Agilent Logic Analyzer COM server object.

Syntax

VARIANT_BOOL StartGenerator();

Description

Starts the transmission of frames to the sink DUT.

Use the "DoCommands method to specify the video and audio generator (.vgf and .aaf) files that you want to transmit to the DUT. Failures can occur with the following causes:

- The specified Video Generator File (.vgf) not found or not valid.
- The specified Audio Generator File not found or not valid (if audio is enabled by specifying With == 1 in DoCommands)
- U4998A hardware is not connected to the controller PC.

When connected, the U4998A module is ready to transmit data to DUT. Therefore, the transmission starts immediately without any waiting time needed for the hardware to be ready for transmission.

You can use the Status() to find out if the transmission from U4998A has started.

You cannot simultaneously generate and capture data.

NOTE

StopGenerator

Applicable COM Server Object

Use this method with the Agilent Logic Analyzer COM server object.

Syntax

VARIANT_BOOL StopGenerator();

Description

Stops the transmission of data from U4998A module to DUT.

Status

Applicable COM Server Object

Use this method with the Agilent Logic Analyzer COM server object.

Syntax

BSTR Status();

Description

Returns a status string from the U4998A module indicating the current status of capture/generator activity on the module. The status string may contain the substrings shown in the following table.

Substring	Description
Running	U4998A is currently capturing data from DUT.
Stopped	No measurement (capture) is occurring, measurement has stopped.
Generating	U4998A module is currently generating signals on its HDMI/MHL OUTPUT.

WaitReady

Applicable COM Server Object

Use this method with the Agilent Logic Analyzer COM server object.

Syntax

```
void WaitReady([in] long Seconds);
```

Description

When connected, U4998A module is ready to capture data. Therefore, WaitReady() always returns true for U4998A module.

Index

element, 138

Symbols

, <mark>138</mark> aaf 1

.aaf, 14, 15, 99 .bmp file extension, 75 .cap file, 15, 44, 78 .txt file extension, 73, 76 .vgf, 14, 15, 99, 105

A

ACP attribute, 145 ACP Packet, 145 ACR attribute, 145 ACR Packet, 145 ACR packet data, 106, 112 Add element, 144 Agilent Logic Analyzer COM Server, 133 Agilent Logic Analyzer software, 13 Agilent Logic and Protocol Analyzer, 13 Agilent U4998A HDMI/MHL Protocol/Audio/Video Analyzer and Generator. 10 AIF attribute, 145 ASP attribute, 145 attribute ACP, 147 Audio, 147 AVI. 147 Clock, 140, 141 Colorimetry, 147 Depth, 146 Deviation, 152 File, 141, 151, 152 Format, 141, 146 GreaterTwo, 147 Name, 138, 145, 148, 149 Protocol, 140 Range, 148 Size, 140 ThreeD, 147 Type, 146 VSDB. 147 With, 151 audio and video files, 99 Audio element, 151 audio IEC compliance, 59 Audio InfoFrame Packet, 145 audio jitter, 77 Audio Sample Packet, 145 Auxiliary Video InfoFrame Packet, 145 AVI packet, 145

AXIe chassis, 12, 32

C

Capture element. 139 capture memory depth, 43 Capture mode, 18, 22 Capture/Compliance testing license, 37 Chassis, 12 Clear element. 145 Clock Deviation, 104 Clock Source, 38 Color Depth, 76 Color element, 146 COM interface, 132 COM servers, 133 compliance testing, 17 Connection element, 138 Content element. 146 Controller PC, 12, 33

D

D field, 106 Data Import module, 80 debug, 126 debugging, 10, 17 DST attribute, 145 DST Audio Packet, 145 DVI, interoperability with, 60

E

EDID, 32, 43, 45 element Add, 144 Audio, 151 Capture, 139 Clear, 145 Color, 146 Content, 146 Evaluate, 136, 139, 140 Full, 147 Generate, 136, 150 hierarchy, 135 Module, 135, 138 Options, 147 PacketLog, 148 Protocol, 148 Quantization, 148 Remove, 149 Set, 150 Test ID, 150 Video, 151

End point, 79 Evaluate element, 136, 139, 140 evaluation log file, 73 Export to File, 76 ExportCapture, 155

F

Finish, 74 First Frame, 85 Frame Generator mode, 25, 27 frame settings, 104 Frame Setup, 107 frames, visually inspecting, 74 Full element, 147

G

Gamut Metadata Packet, 73, 145 GCP attribute, 145 General Control Packet, 145 Generate CSV utility, 78 Generate element, 136, 150 Generator, 36 generator, 99 Generator license, 37 GetBitmapFiles, 156 GetTMDSClockValue, 156 GMP attribute, 145

H

HBR attribute, 145 HDMI Compliance Testing, 18 HDMI compliance testing, 10 HDMI connection, 37 HDMI CTS 1.4a, 11 HDMI Evaluator, 14 HDMI Evaluator COM Server, 133 HDMI OUT connector, 108 HDMI Testing sample setup, 16 hierarchy of the XML elements, 135 High Bit Rate Audio Stream Packet, 73, 145 Hot Plug Detect, 43 Hot Plug Detect, 43 Hot Plug Detect, 128 HPD, 128 HPDReset, 153

ILL attribute, 145 Illegal Packet Type, 73, 145 Image window, 74, 158

Index

interlaced formatted data, 84 Interlaced Video Data, 93 Internal clock, 38 IS1 attribute, 145 IS2 attribute, 145 ISRC1 Packet, 73, 145 ISRC2 Packet, 73, 145

L

LEDRefresh, 155 license, 15 Listing View, 81 log files, 73

Μ

markers, 82 memory depth, 11 methods ExportCapture, 155 GetBitmapFiles, 156 StartCapture, 154 StartEvaluate, 157 StartGenerator, 159 Status, 159 StopGenerator, 160 WaitReady, 162 WriteEDID, 153 MHL, 10 MHL adapter, 21, 26 MHL cable, 21, 26 MHL Compliance Testing, 21 MHL compliance testing, 10 MHL connection, 37 MHL EDID files, 49 MHL hardware license, 44 MHL sink tests, 11 MHL source tests., 11 MHL testing hardware license, 21, 26, 30 MHL testing sample setup, 16 Mirror mode, 20, 24, 37 Module CSV file, 78 module CSV file. 15 Module element, 135, 138 MPEG Source InfoFrame Packet, 73, 145 MPG attribute, 145

Ν

N Parameter, 113 N parameter, 113 Navigator pane, 72 NEXT Frame, 74 notices, 2 NUL attribute, 145 Null Packet, 145

0

OBA attribute, 145

offline evaluation, 14 Offline mode, 33 One Bit Audio Sample Packet, 73, 145 online mode, 33 Options element, 147

Ρ

packet contents, 111 Packet LOG, 73 Packet Log File, 73 packet log file, 73 PacketLog element, 148 Pass through, 29 pass through, 126 Passive Monitoring license, 37 passive monitoring license, 21, 24, 30 Pass-through mode, 36 PCI Express cable. 32 pixels-per-frame, 87 pixels-per-line, 87, 88 predefined EDID files, 45 Progressive Format, 90 progressive formatted video data, 83 Protocol element, 148

0

Quantization element, 148

R

Remove element, 149

S

Set element, 150 Software Licensing, 78 Source Product Description InfoFrame Packet, 73, 145 source tests, 11 SPD attribute, 145 Start point, 79 StartCapture, 154 StartEvaluate, 157 StartGenerator, 159 Status, 159, 161 StopGenerator, 160 Supported Sink Tests, 101

T

Terminator, 36 terminator, 18, 21 Test ID element, 150 Test Results pane, 72 TMDS, 38 TMDS clock frequency, 43 trademarks, 2

U

U4995A, 26 U4998A HDMI 1.4a Protocol/Audio/Video Analyzer and Generator module, 12 U4998A HDMI Video Generator Files software, 14 U4998A HDMI Video Generator Files software component, 45 U4998A HDMI Video Generator Files utility, 99 U4998A MHL Video Generator Files software, 14 U4998A MHL Video Generator Files software component, 45 U4998A tab, 14 U4998A-Pass-through connection mode, 127 U4998A-PSV license, 21, 24, 30

V

Vendor Specific InfoFrame Packet, 73, 145 Video Data Period, 75 Video element, 151 Video Format Timing, 76 Video Format Timings, 101 video generator files, 111, 113 video identification codes corresponding EDIDs, 50, 51 Video Image Window, 74 VSI attribute, 145

W

WaitReady, 153, 162 Waveform View, 81

X

XML-based string argument, 135