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A Portable 1100-MHz Frequency Counter

This new addition to the 5300 Measuring System is well suited for checking out land mobile communications and aeronautical navigation equipment.

by Hans J. Jekat

BY 1985, HALF OR MORE of the land mobile communications equipment in the United States may be operating in the recently opened 806-to-902-MHz and 928-to-947-MHz frequency channels. To help keep these mobile transmitters on frequency, a portable frequency counter will be needed.

The new Model 5305A 1100-MHz Frequency Counter (Fig. 1) fills this need. It is the first portable counter to reach 1100 MHz, a frequency range that also takes in air traffic control and television channels 14 to 69 (Fig. 2). The new counter has the advantage of being a snap-on functional module for the low-cost, compact 5300 Measuring System, which now includes two mainframes, eight snap-on functional modules, and three auxiliary modules: battery pack, analog output, and HP interface bus output.

Frequencies from 70 MHz to 1100 MHz are measured at a 50Ω front-panel input. A second input is provided for measuring frequencies from 50 Hz to 80 MHz; input impedance is 1 MΩ. Frequencies are prescaled by 16 at the high-frequency input and counted directly at the other input.

The recommended mainframe for use with the new counter is the eight-digit Model 5300B (see page 6). Recommended time base is an optional temperature compensated crystal oscillator that has an aging rate less than 1.2 parts in 10^6 per year. This oscillator is available as an option for either the mainframe or the counter module. If such high time-base stability is not required, the standard mainframe time base may be used.

Special Fuse Holder

The heart of the 1100-MHz input channel is a completely enclosed 50Ω front end containing a 1300-MHz amplifier, an 1100-MHz binary, and a 550-MHz binary (Fig. 3). To protect this assembly from large input signals, a special fuse holder was designed (see Fig. 4). The fuse, an inexpensive commercially available type, is located in the input BNC connector and the cavity that holds it is tuned to have an SWR less than 1.1 over the entire frequency range.

This special fuse protection gives the user a great deal of mobility by relieving him of any worry that he may damage his expensive front end because he is not sure what power he is applying to the input. If he blows the fuse, he loses only a few cents and thirty

Cover: *Model 5305A, a new low-cost, compact, portable 1100-MHz frequency counter, is well suited for checking land mobile communications transmitters in two newly opened U.S. channels between 806 and 947 MHz. Its key component, a specially fused, divide-by-four front end, is shown in the foreground. (We are grateful to the mobile paramedic unit of the City of Palo Alto for their help with the background photo.)*

In this Issue:

Fig. 1. *The new Model 5305A 1100-MHz Frequency Counter (lower module) is shown here with the eight-digit Model 5300B mainframe (upper module). Insertion of a battery pack between the two modules makes the counter completely portable for checking mobile communications systems.*

seconds of his time.

Flexible Attenuator

To make the counter useful for measuring a wide variety of input signals, a PIN-diode π attenuator, Fig. 5, precedes the input amplifier. The attenuator may be controlled manually or automatically. When the SENSITIVITY control is in its AGC position, the attenuator is controlled by an operational amplifier that senses the output level of the input amplifier. This setting is especially useful for measuring noisy signals. For measuring amplitude-modulated signals, manual sensitivity control is more useful. The attenuator has a range of 0 to 40 dB.

Although this attenuator offers the user great flexibility, it can cause problems for the input amplifier. If the user sets the SENSITIVITY control for maximum sensitivity and applies the maximum input signal of 5V rms, the amplifier will be overdriven, ringing will occur, and the counter will count incorrectly. To overcome this problem a second control loop samples the amplifier input level. If it exceeds a preset value, attenuation is added automatically to reduce the signal to a safe operating level. When this occurs, a front-panel light-emitting diode indicator lamp turns on. Attenuation can then be added manually to take the overload control circuit out of the measurement. The

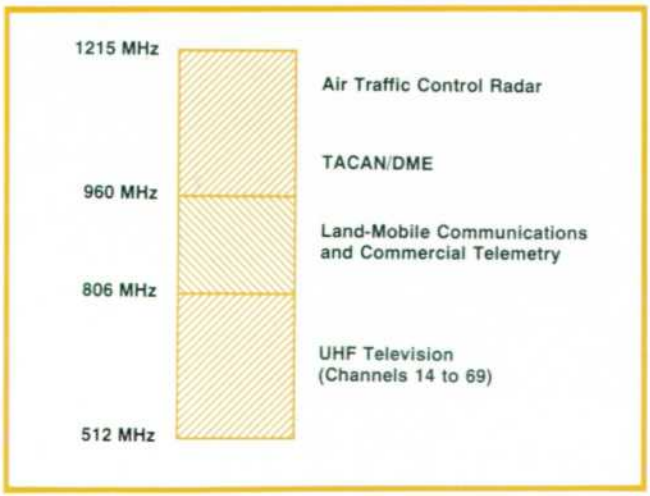


Fig. 2. *Frequency spectrum allocations within the range of the 1100-MHz counter.*

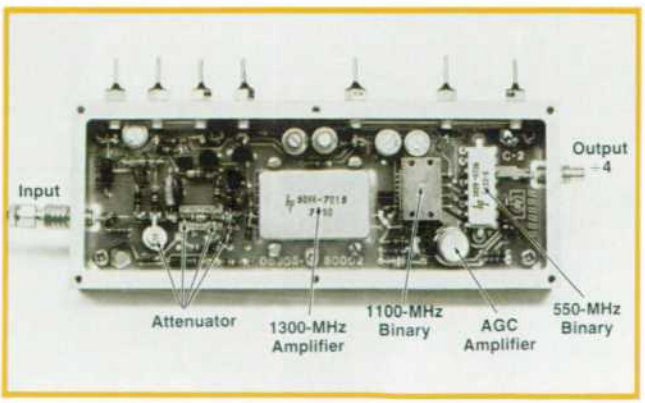


Fig. 3. *Completely enclosed high-frequency front end contains an attenuator, a broadband amplifier, a high-speed binary, and a second binary.*

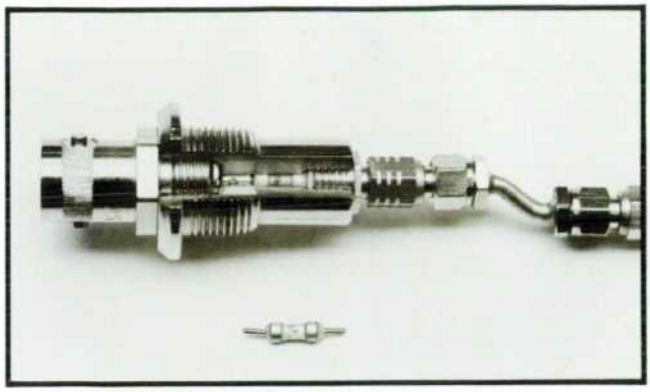


Fig. 4. *Special fuse holder in the input BNC connector takes inexpensive, easily obtainable fuses. Fuse protection frees the user from worrying about applying too much power and damaging his expensive front end.*

indicator lamp can also serve as a level indicator, informing the user that he has applied more than enough input signal for proper counting.

When the SENSITIVITY control is placed in the AGC position the indicator lamp turns on to indicate this fact.

1100-MHz Binary

The input amplifier, a thin-film circuit, has a bandwidth of 1300 MHz. Typically, the counter will count much higher than 1100 MHz, and the use of a 1300-MHz amplifier assures that the high-frequency limit depends only on the 1100-MHz thin-film binary (divide-by-two circuit) that follows the amplifier. The binary is the fastest digital circuit needed in the counter.

The high-speed binary uses special dual-transistor chips, a common-emitter type and a common-collector type (Fig. 6). The chips are made by a new HP 5-GHz transistor process. Putting differential pairs on a monolithic substrate results in very close matching and reduces the number of discrete transistor chips in the binary from 16 to 8. This helps increase the production yield of the finished binary.

Fig. 7 is the binary schematic diagram. The circuit is a master-slave flip-flop divider. Two current-mode flip-flops are cross-coupled in a master-slave configuration. Second-level current switches control updating and latching of the flip-flops. Output of the master is shifted into the slave on a positive transition of the input voltage, then inverted and transferred back to the master on the next negative transition.

Stages are coupled directly to each other. A very small logic swing of 250 mV is used, large enough to drive the current switches, but small enough to keep the switching transistors in the active region to reduce parasitic-capacitance time constants. To eliminate rise and fall time differences all stages are driven differentially, taking advantage of the nearly perfect matching of the monolithic transistor pairs. A peaking coil is used to boost the toggle speed.

The current switches are not offset (i.e., biased at different levels), so the divider may oscillate unless

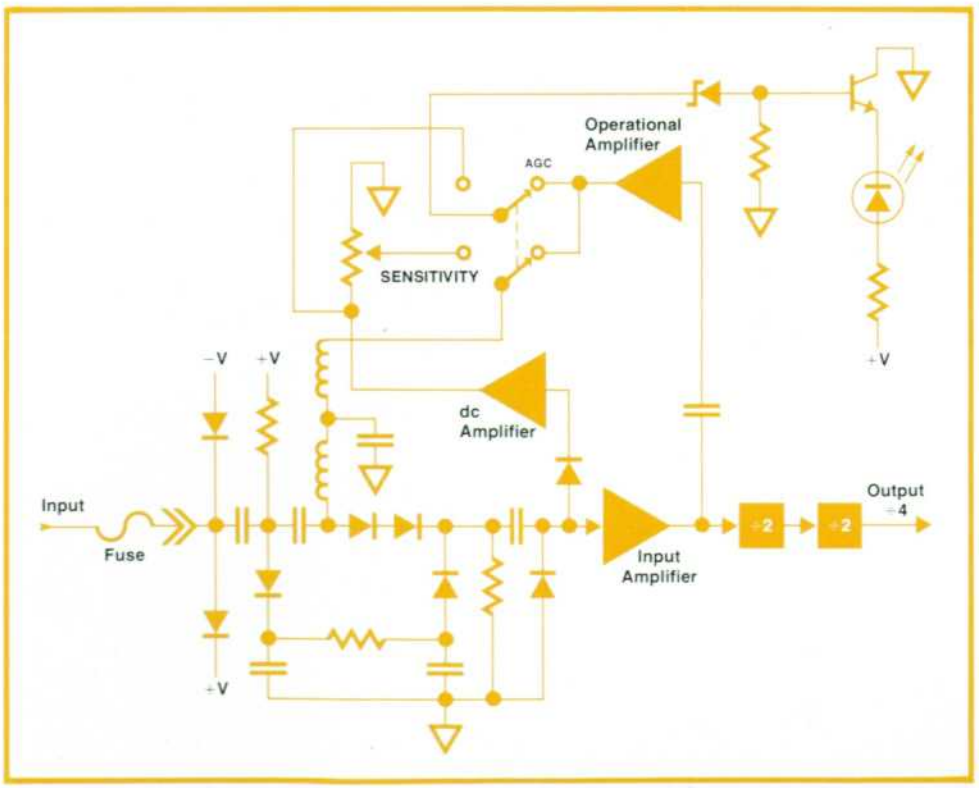


Fig. 5. *Input attenuator may be controlled manually or automatically. Usually automatic sensitivity control is better for noisy signals; manual control is better for amplitude-modulated signals.*

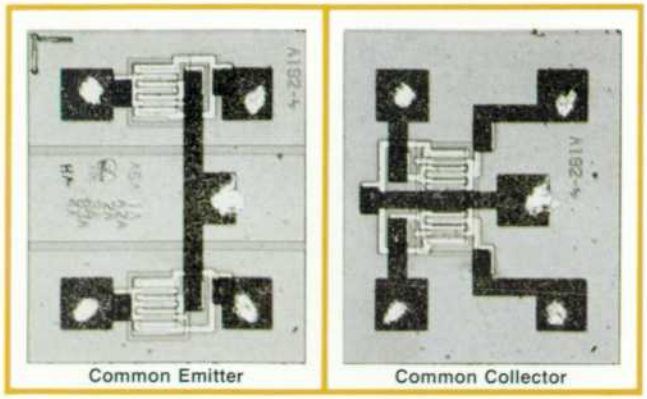


Fig. 6. *Special dual-transistor chips, made by a new 5-GHz transistor process, are used in the high-speed binary in the 1100-MHz front end.*

the input current switch sees switching times that are less than the propagation time of the master-slave section.

The outputs of the master and slave flip-flops go to a differential output amplifier, which interfaces directly with an HP E²L monolithic binary that requires a 600-mV logic swing. A diode in the power supply of the master-slave section keeps the differential output amplifier from saturating.

Low-Frequency Design

The high-speed binary is not preceded by a Schmitt trigger. This is no problem for UHF measurements, but would have made it difficult for the binary to operate below 70 MHz to get a good overlap with the 80 MHz input channel. The problem at low frequencies is that, in the absence of a Schmitt trigger, the zero-crossing transitions of the input signal may not be sharp enough for proper triggering.

To lower the minimum frequency and at the same time reduce ambiguous counts that are often seen when the counter is used on the threshold of its sensitivity, a feedback loop is used (see Fig. 8). The loop

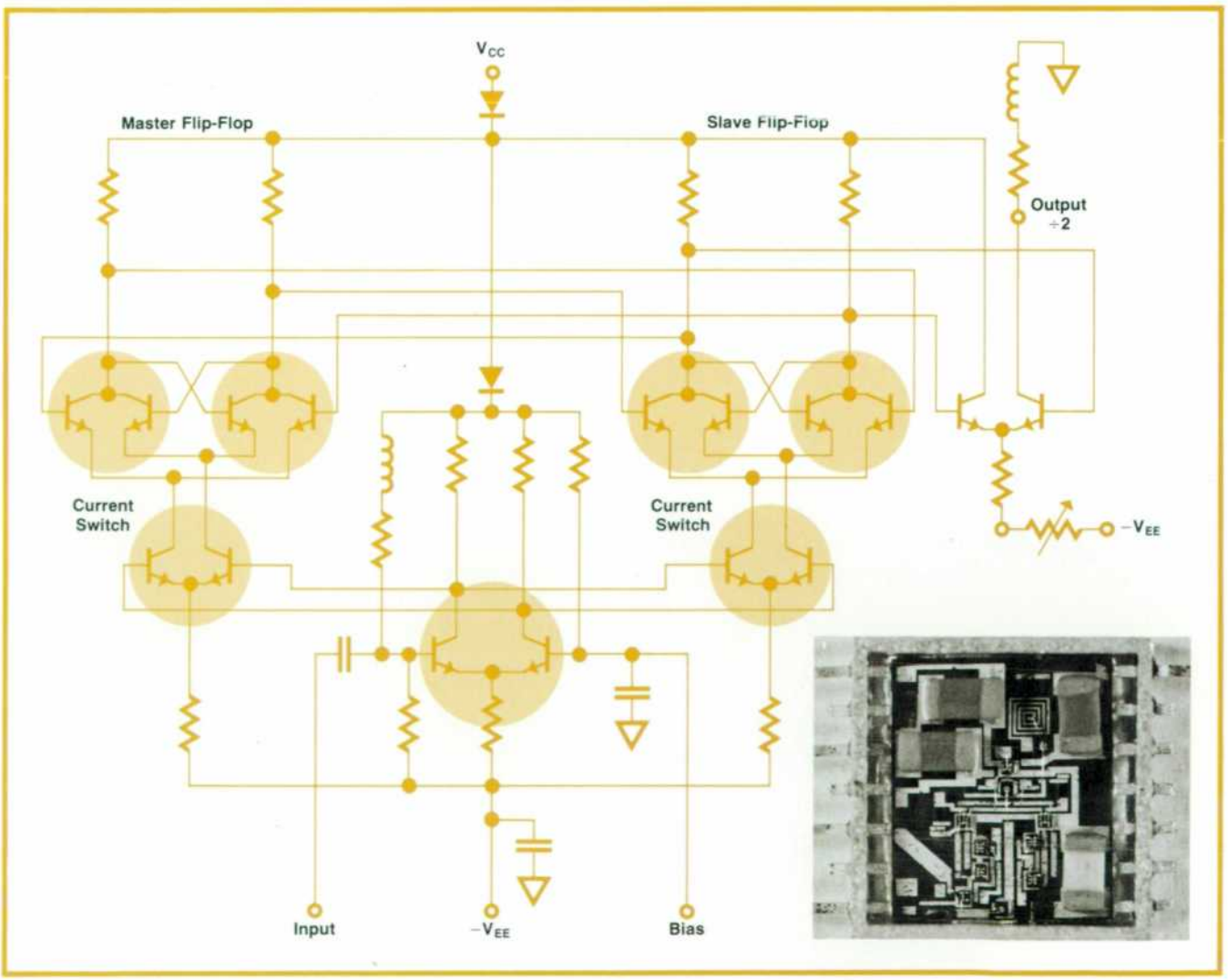


Fig. 7. *High-speed binary is a master-slave flip-flop divide-by-two circuit.*

An Eight-Digit Mainframe for the 5300 Measuring System

Model 5300B, a new eight-digit mainframe for the 5300 Measuring System, is compatible with all eight 5300-series timer, counter, and multimeter snap-on modules, and with all three "in-between" modules including the battery pack. It was developed in response to the needs of many users for more "resolution at a glance"—that is, more digits in the display—and more power supply capacity to handle existing snap-on modules under more severe environmental conditions and to allow more power for new modules, such as the 5305A 1100-MHz Counter and the 5308A Universal Timer/Counter.

Internally, the new mainframe differs from its predecessor in many ways. The 5300B uses eight single-digit low-cost display units, whereas the 5300A uses a single six-digit unit. Using individual digits cut down both the development cost and the factory cost compared to tooling an eight-digit version of the 5300A display.

In the 5300A, strobing of digits is performed by a single integrated circuit that includes a clock oscillator, a counter, and six digits, however, so several separate IC's perform this function in the 5300B. Again, an objective was to save development time.

The major differences between the two mainframes are in the decade counting chain. Although the 5300B displays eight digits, it has only seven decade counters. Six decades are provided by the same MOS LSI circuit used in the 5300A. In the B version, this circuit is preceded by a higher-speed low-power Schottky TTL decade that has its own latch.

When the eighth digit is used it must be driven by a decade counter in the snap-on module. At present, Models 5303B, 5305A, and 5308A have this capability. These modules count higher frequencies, so the seven digits that are adequate for most 10-MHz counting tasks are not quite enough for them.

The seventh decade in the new mainframe precedes the MOS circuit. This makes it necessary to subtract one from the digit address code generated by the strobing circuits to make the information in the MOS decades appear in the proper display digits. The 5306A Multimeter module complicates matters by requiring that the mainframe have only six decades for voltage and resistance measurements so the overflow indicator will work properly. A read-only memory solves the problem. It stores two digit-address multiplexing programs, one for the 5306A and another for all the other modules. The 5306A program gates the frequency to be counted directly to the MOS decades—bypassing the extra decade—and does not subtract one from the digit-address code. The other program sends the unknown frequency to the high-speed decade, subtracts one from the digit-address code, and enables the latch outputs of the high-speed decade at the proper time. The 5306A is detected by the mainframe by the fact it is the only module that adds one to the digit-address code; it does this to blank the most significant digit and display the sign of a voltage measurement in that location.

The temperature-compensated crystal oscillator (TCXO) previously available in the FCC type-approved 5303B 525-MHz Counter module is now available as an option in the 5300B mainframe. This makes this same high-stability time base available to all the modules. It is especially appropriate for the new Model 5305A 1100-MHz Counter.

To make room for the TCXO the BCD output that is standard in the 5300A was deleted. Digital output capability can be provided by the 5312A HP Interface Bus module. Two signals were added to the 50-pin interface connector that joins mainframe and modules to allow the 5312A to keep the mainframe in a hold condition and initiate a measurement at will, and to transmit overflow information.

A new digital-to-analog converter module, Model 5311B, has replaced the earlier 5311A. The new converter has the extra columns of selectivity to accommodate either the eight-digit mainframe or the six-digit mainframe.

P. Thomas Mingle

keeps the counter from counting unless a substantial input signal is present. It then automatically increases the input sensitivity during the gate time, so the counter sees a signal that far exceeds its threshold level. Thus there is no possibility of ambiguous counts. Also, because a large signal has a faster zero-crossing transition than a smaller signal of the same frequency, the problem of low-frequency triggering is minimized.

As Fig. 8 shows, the input of the high-speed binary is a differential amplifier. Input A is the signal input. Input B is used to bias the binary for maximum sensitivity. When the dc offset from input A to input B is about −1.485V, the binary has maximum sensitivity; however, it is also perfectly balanced and will oscillate even without an input signal. To avoid this, the offset of input B is changed slightly, just enough to avoid oscillation. In practice, the additional offset is 20 mV or less.

When the binary is set for maximum sensitivity its threshold is about 45 mV peak. If a signal larger than this is applied to point A the binary will function correctly. If the input signal at point A is less than 45 mV peak, the binary may divide by two or it may feed the input signal through without division, which would result in an incorrect reading. This ambiguity is avoided by the feedback loop.

When the counter is reset, initiating a measurement, the $\overline{Q}$ output of the arming flip-flop shown in Fig. 8 goes to its high state. This keeps the gate from opening and changes the offset of input B to about −1.32V. This means that the signal at input A must have a peak amplitude of at least 165 mV to pass through the −1.32V threshold and cause the counter to react.

Now when the input signal is large enough, it gets through the chain of prescalers and reaches the arming flip-flop. The $\overline{Q}$ output of the arming flip-flop goes to its low state and latches there. The gate then opens and counting begins. When $\overline{Q}$ goes low, it also re-

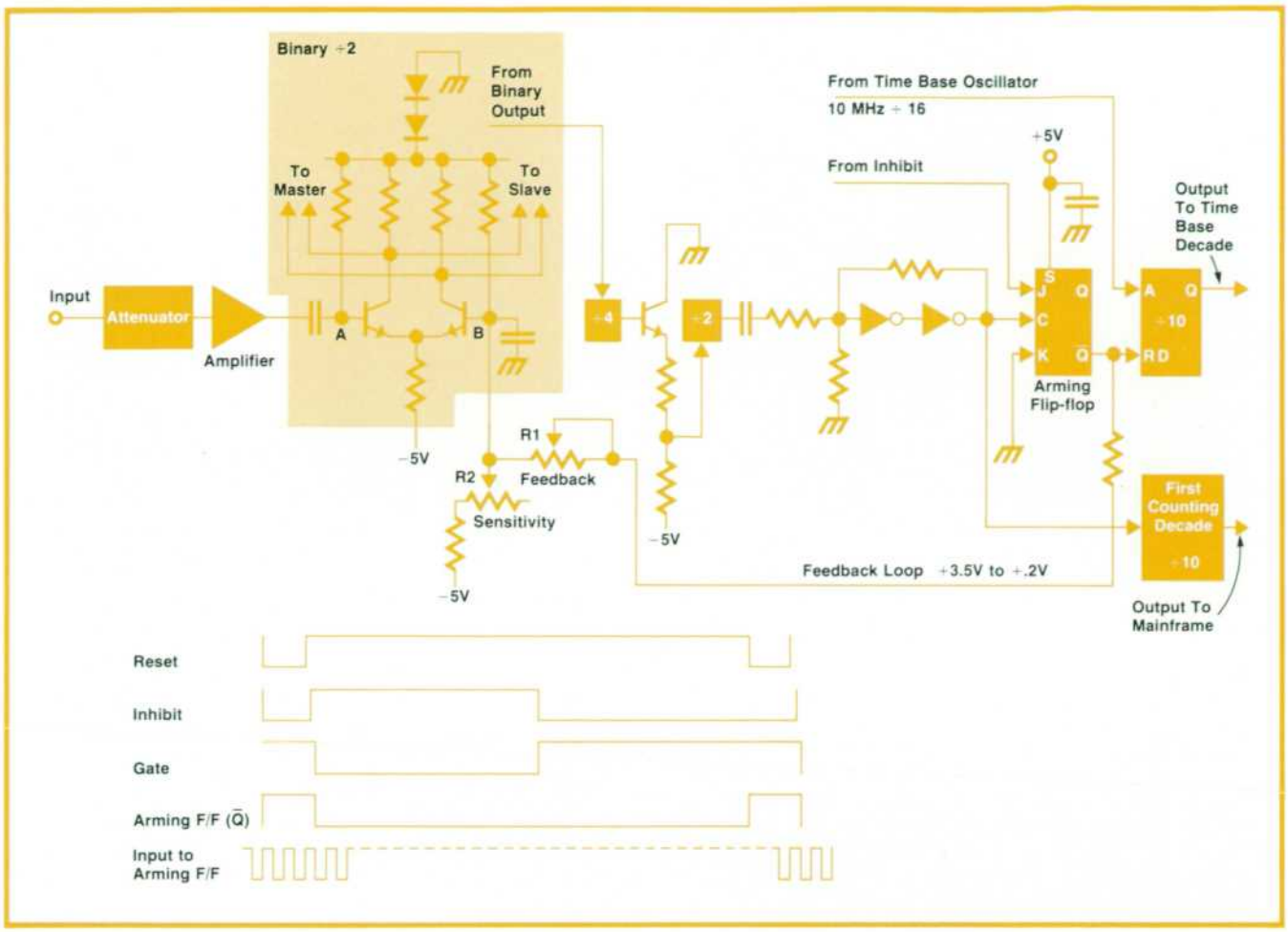


Fig. 8. *Feedback loop reduces input sensitivity until a large enough input signal is present, then increases sensitivity during counting.*

duces the offset of input B of the first binary to its minimum level of −1.485V plus or minus a few millivolts, so the binary has maximum sensitivity. However, the input signal is now much larger than the threshold signal, so there are no triggering or ambiguity problems.

The two offsets of input B are set by adjusting R1 and R2. These interact to a degree, but R1 is primarily for feedback loop adjustment and R2 is primarily for sensitivity adjustment.

Decade Counters and Display

The fastest decade of the eight-decade counting chain is located in the 5305A as shown in Fig. 8. The output of this decade goes to the 5300B mainframe, which contains the other seven decades and the eight-digit display.

Acknowledgments

I would like to express my appreciation to the following people for their assistance in the development of the 5305A Counter. The performance of the counter could not have been achieved without the outstanding 5-GHz transistor process development by Dave DiPietro. The excellent support from the Santa Clara thin-film department, especially Barry Welsh and Jerry Merkelo, was greatly appreciated. I

Hans J. Jekat

Hans Jekat holds the equivalent of a BS degree in electrical engineering from the Technische Hochschule in Munich. He moved to the U.S.A. in 1958, and since 1964 has been with HP's Santa Clara Division. Now project leader for the 5300 Measuring System, he designed the 5300A mainframe, several of the MOS/LSI circuits used in the 5300 system and other instruments, and the high-speed binary for the 5305A Counter. He holds several patents related to his counter work. Hans is married, has two young sons, and lives in Redwood City, California. For many years a trainer of show horses, he's currently teaching his sons to ride and appreciate horses as he does.

A New 5-GHz Transistor Process

The dual-transistor chips used in the input high-speed binary of the new Model 5305A 1100-MHz Frequency Counter are fabricated by a new bipolar integrated circuit process that produces transistors having an f_T of 5 GHz, more than twice as high as previously attained.[1]

Basic to the development of the new process was a computer simulation of an E²L gate to identify the factors limiting gate propagation delay. An accurate high-frequency large-signal transistor model was needed. The model chosen was the Ebers-Moll model modified to include high-frequency behavior and the Early effect. The model is shown in Fig. 1. Parameters added for high-frequency effects are series resistors R_B, R_C, and R_E and junction capacitors C_{BC}, C_{BE}, C_{jE}, C_{jC}, and C_{CS}. C_{BE} is proportional to forward transit time $\tau_F = 1/(2\pi f'_T)$, where f'_T is the limiting value of f_T. C_{jE}, C_{jC}, and C_{CS} are depletion-layer capacitances.

The simulation showed that τ_F and R_B were the principal elements that determine propagation delay. Decreases of 50% in each of these parameters resulted in decreases of 35% and 17%, respectively, in propagation delay. Similar changes in C_{jC}, C_{jE}, and C_{CS} reduced propagation delay by 5% or less.

HP's 2-GHz bipolar transistor process was then modified to reduce τ_F and R_B. Key features of the new process are an ion implantation of boron for the base region and the use of a combination of molybdenum and gold for metallization. The active base region is formed by an implanted predeposition of boron followed by a thermal drive-in diffusion. A base insert reduces R_B. To reduce R_C, a buried collector layer and collector insert are used. The emitter is formed by diffusion of phosphorus; emitter stripe width is 2.5 μm. First and second metallizations—separated by a layer of silicon dioxide—both consist of a layer of gold over a layer of molybdenum. Epitaxial-layer thickness and resistivity are 2.4 μm and 0.6 ohm-cm, the same as in the earlier 2-GHz process.

Fig. 2 shows the gain-bandwidth product of a typical transistor as a function of collector bias current.

The new process is not limited to transistor production. More complex monolithic circuits are under development.

David M. DiPietro

Reference

1. D.M. DiPietro, "A New 5 GHz f_T Monolithic Integrated Circuit Process for High-Speed Digital Circuits," International Solid State Circuits Conference, 1975.

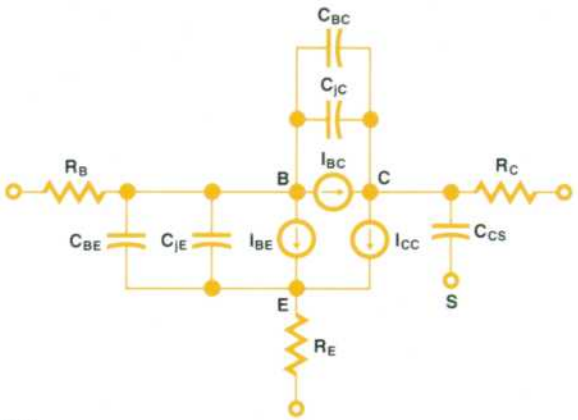


Fig. 1

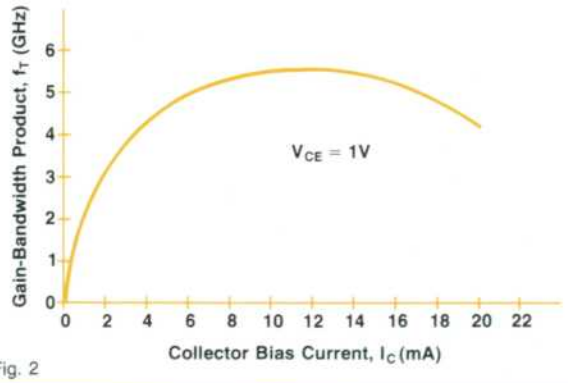


Fig. 2

would like to thank Tom Mingle and Chuck Howley for their electrical design of the 5300B mainframe and Larry Johnson for his marketing support. Product introduction was eased with the dedicated support and help of Tommy Thomason, Don Larke, and Jim Feagin. My thanks also to Ian Band, engineering section manager, for his support in the project.

Big Timer/Counter Capability in a Portable Package

This 75-MHz, eight-function universal timer/counter is another snap-on module for the low-cost, compact 5300 Measuring System. Compatibility with battery pack, digital-to-analog converter, and HP interface bus modules provides extra versatility.

by Kenneth J. MacLeod

A MAJOR FACTOR IN OUR DECISION to design a more powerful universal counter module for the 5300 Measuring System was our confidence that semiconductor technology had advanced to a point where we would be able to include most of the features and specifications that would be expected in a full-rack-width counter without sacrificing the compactness and low cost of the 5300 system.[1] We felt that such a counter would be valuable to many users.

The result, Model 5308A 75-MHz Timer/Counter (Fig. 1), is an eight-digit, eight-function universal timer and counter. It counts directly to 75 MHz and achieves subnanosecond resolution in measuring repetitive time intervals. In addition to a wide selection of manual ranges for all functions, it has a novel autoranging system for four functions. Its capabilities are substantially better than those of previous 5300-system counters, and compare favorably with some much larger and more expensive units.

The frequency range of 75 MHz, 50% higher than previous 5300-system universal counters, was achieved by the use of Schottky TTL integrated circuits. Because it counts directly, the new module offers ten times more resolution than its prescaled

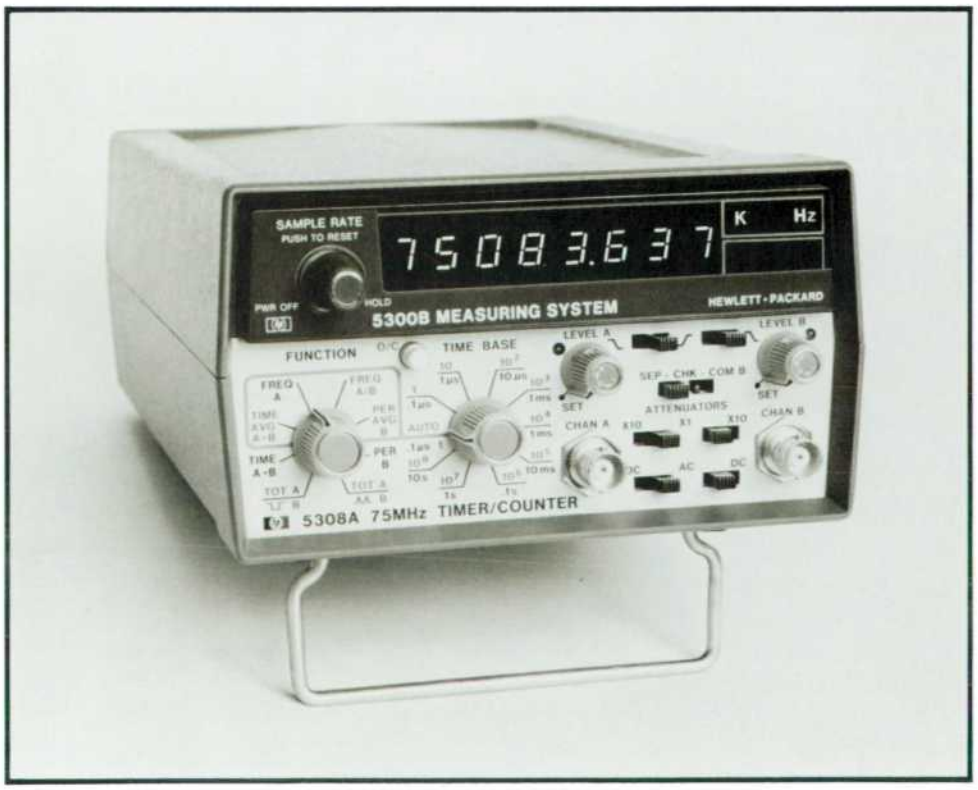


Fig. 1. *Model 5308A 75-MHz Timer/Counter (lower module) is an eight-function, eight-digit universal timer and counter that works with the 5300B mainframe. Features include autoranging, trigger lights, and preset trigger levels for logic measurements.*

50-MHz predecessor.

The 5308A Timer/Counter works only with the new eight-digit mainframe, Model 5300B, and not with the earlier six-digit mainframe. Although it can display eight digits, the new mainframe contains only seven decade counters, relying on the snap-on module to provide an eighth decade if desired. The new timer/counter contains this counting decade.

Timer/Counter Functions

The eight functions provided by the 5308A are:

- Frequency
- Frequency ratio
- Period
- Period average
- Time interval
- Time interval average
- Totalize counts on one channel during a pulse on the other
- Totalize counts on one channel between two pulses on the other.

The last three functions are all new to 5300-system universal counters.

Time interval averaging improves resolution on repetitive time intervals. The system used is quite similar to that of the larger HP 5326 and 5327 counters.[2,3] Resolution increases approximately as the square root of the number of unique events averaged. For a single time interval, resolution is limited by the 10-MHz internal oscillator to 100 nanoseconds. If 10^6 events are averaged, resolution is improved by a factor of 10^3 to 100 picoseconds.

In contrast to resolution, the accuracy of time interval measurements is more dependent on the difference in propagation delays between the two channels. Measurements are guaranteed accurate within one nanosecond. This is achieved by making both input channels as identical as possible in every respect. Both Schmitt triggers, for example, are on the same IC chip, and both time interval synchronizers are on a single chip.

The two new totalizing functions provide flexible electrical gating, and should be widely useful in diagnosing problems in digital communications and computation systems. Events may be totalized on channel A at rates up to 75 MHz. Channel B can open and close the gate on four combinations of transitions. The panel markings indicate totalizing from a negative-going transition to a positive one (⎍), or from one positive-going transition to the next (⩘). These markings assume the channel B slope switch is in the ⎍ position; placing it in the ⎎ position inverts the polarities of all transitions mentioned above, thus providing the other two combinations, ⎍ and ⩛

Several other features have been built into the function "totalize A from one pulse on B to the next." First, the totalizing can be started and stopped by pressing a manual OPEN/CLOSE pushbutton. While totalizing is under way, the TIME BASE OUTPUT port on the rear panel provides a replica of the channel A input signal (up to 10 MHz) scaled by the factor 10^N indicated by the TIME BASE selector switch. In the CHECK mode, the 10-MHz oscillator is substituted for channel A. This results in a manually or electrically operated stopwatch. Once again, the TIME BASE OUTPUT provides 10 MHz scaled by the indicated factor while the count is in progress. This serves as a handy source of any decade frequency from 0.1 Hz to 10 MHz.

Autoranging

The TIME BASE selector switch has ten positions: nine are manual ranges and the tenth is AUTO. The nine manual ranges may be selected for any function. For instance, periods may be measured with a resolution from 1 femtosecond (10^{-15}s) to 10 seconds, and an overflow point from 100 nanoseconds to 1 gigasecond.

Most users will find they rarely need to select any TIME BASE position except AUTO. This provides human-oriented autoranging for four functions: frequency, frequency ratio, period average, and time interval average. When AUTO is selected, the 5308A automatically selects a range that results in a measurement time between 0.11 second and 1.1 second. Thus the user gets measurements with the best resolution possible within a convenient gate time, which we have found, based on observations of typical users, to be in the range 0.1 to 1 s. The 5308A is the first counter to provide such autoranging for frequency ratio and time interval average (see box, page 11).

The four functions that are not autoranged operate in their highest-resolution range when AUTO is selected. Since the eight-digit display allows totalizing up to 10^8 counts or measuring a period or time interval up to 10 seconds in this range without overflow, it is satisfactory for the great majority of measurements. As a result, the user can ignore the TIME BASE selector except on rare occasions.

Under all conditions, correct decimal points and annunciators are displayed by the 5308A. This is true even for frequency ratio and totalizing with prescaling, which have traditionally left these computations to the user.

Central Control ROM

Much of the new capability of the 5308A Timer/Counter was made possible by the addition of a single IC: the central control ROM (read-only memory). This circuit controls all signal multiplexing and all decimal points and annunciators. It decodes 184 combinations of FUNCTION, TIME BASE, CHECK switch,

A Universal Autoranging System for a Universal Timer/Counter

Autoranging schemes have been available in counters for several years, but none are usable for as many functions as the system employed in the 5308A. Conventional autoranging was introduced to prevent overflow when measuring high frequencies in counters that have few digits. The gate time is automatically shortened, thereby reducing resolution and preventing overflow.

Such a system is hardly necessary for the 5308A, since the maximum input frequency of 75 MHz can be counted to a resolution of 1 Hz (gate time of one second) in the 8-digit display without overflow. Why then should the 5308A have an autoranging system at all?

The answers to this question are found in measurement functions other than frequency. First, when measuring only one parameter, such as period average, it is a nuisance to calculate the time base selection for maximum resolution. Second, when alternately measuring two parameters, it is usually necessary to change the time base selection each time the function is switched. Both these difficulties are removed by the 5308A.

As a simple example of the time base calculation problem, consider measuring the average period of a 2-kHz signal. A single period is 500 microseconds. The result will be displayed as 500.0 μs, using only four of the eight available digits. To achieve maximum resolution, we can set the time base to average 10^4 periods. This yields a display of 500.00000 μs, but the measurement takes five seconds. To get more rapid measurements, the user would probably settle for a time base selection of 10^3 periods and a display of 500.0000 μs. In practice, most users are found to make a time base selection by trial and error when measuring period average, time interval average, and frequency ratio. The 5308A makes all these selections automatically if desired.

Now if this user also needs to measure the frequency of a 30-kHz signal, he can easily select a one-second gate time, for a display of 30.000 kHz. But this means a change of time base selection is required for each change of function. Here is another case where autoranging makes measurements faster and easier.

How Does It Work?

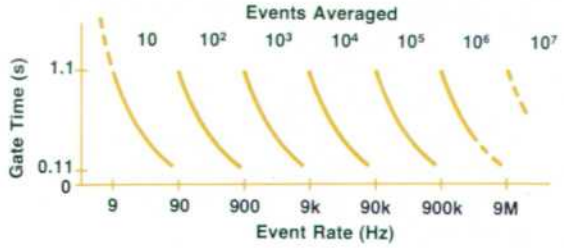
The new autoranging system combines the patented "log time base" of the 5300B mainframe[1] with a 0.11-second timer in the 5308A (see Fig. 2). The timer is the commercially available type 555 integrated circuit timer used as a one-shot. It is triggered by the opening of the gate. About 0.11 second after the opening of the gate, the 555 clocks FF1, enabling FF2 to be clocked on the next log pulse. The log time base produces pulses when 10 events have occurred, and when 10^2, 10^3,..., 10^7, 10^8 events have occurred. The first of these pulses to occur after 0.11 s has elapsed will close the gate. Because the pulses represent powers of ten of the event rate, some pulse will close the gate after it has been open for a time between 0.11 and 1.1 s.

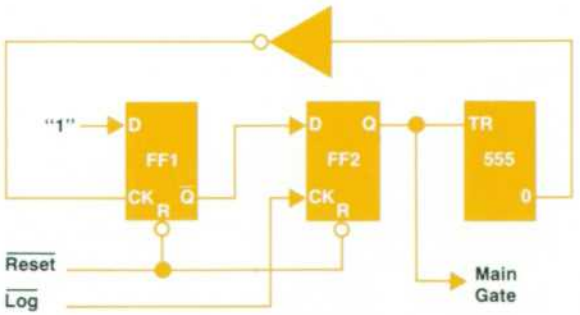
Returning to the example of measuring the period average of a 2-kHz signal, we see that log time base pulses occur at 5 ms, 50 ms, 500 ms, 5 s, and so on. These represent 10, 10^2, 10^3, and 10^4 events. The first of these to occur after 0.11 s elapses is the 500-ms pulse, representing 10^3 events. This pulse closes the gate. This is probably the same gate time the user would have selected.

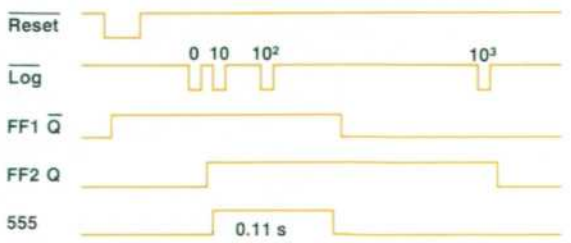
When measuring frequency in the AUTO mode, the 5308A always selects a 1-s gate time. If the 555 had been set to a nominal value of 0.1 s, component tolerances would have caused some units to produce an actual time of 0.095 s and others to produce 0.105 s. This would have caused the 5308A to select either 0.1-s or 1.0-s gate times. To force a 1.0-s gate time in frequency measurements despite component tolerances, the nominal value was raised to 0.11 s.

Thanks to the inexpensive 555 timer, the 5308A performs autoranging on the user's own terms: convenient gate time. Resolution is the best possible within this constraint. Previous considerations of display overflow or underfilling are ignored. Since events may occur at an arbitrary rate, it is possible for the first time to autorange in time interval average and frequency ratio measurements.

Users who have special needs for longer or shorter automatic measurement times can request special versions of the 5308A. Any decade range of measurement times can be provided. For example, if faster response is needed to allow rapid signal changes to be followed, a range of gate times from 0.03 to 0.3 s could be requested.







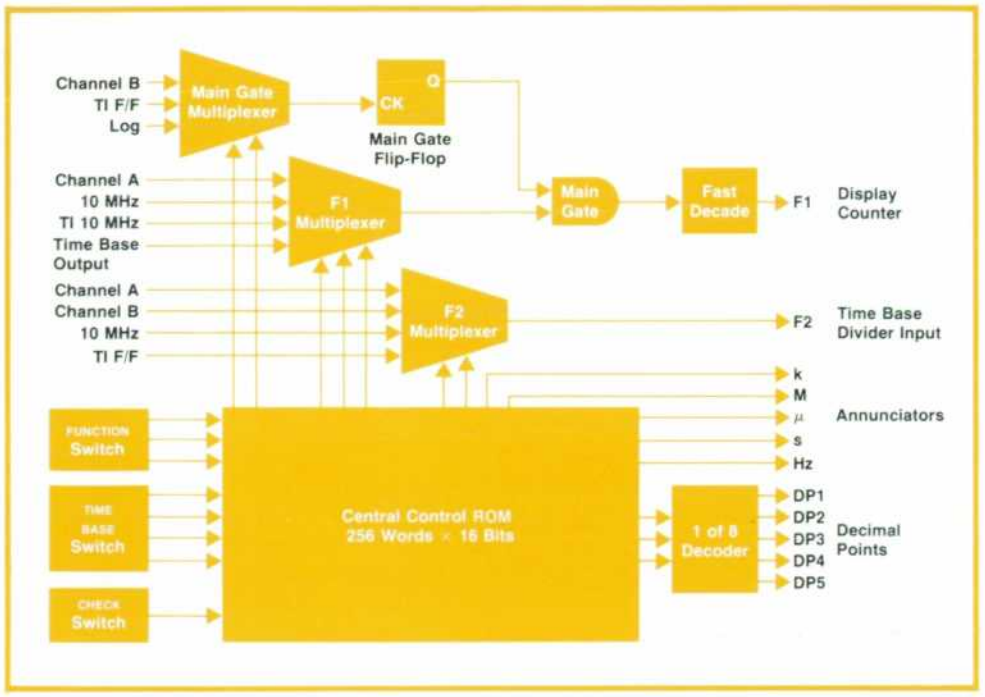


Fig. 2. *5308A function control circuit. Central control ROM made possible much of the new capability of the 5308A, including autoranging and time interval averaging.*

and event rate. Essentially all the low-speed logic that would have been necessary to implement the 5308A is replaced by the central control ROM (see Fig. 2). The central control ROM is a 4096-bit NMOS ROM organized as 256 words of 16 bits each. Besides allowing more functional decoding to be performed, the central control ROM also was instrumental in making the low-speed logic more compact. This was the factor that made possible the addition of synchronizers for time interval averaging, the circuitry to display the contents of the fast decade, and even the autoranging system.

Input Channels

Each of the two input channels has selectable ac or dc coupling, a switchable attenuator, a slope switch, and a trigger level control with a range of ±2V. Jacks on the rear panel allow monitoring of the trigger levels with an external DVM or other high-impedance voltmeter.

Also on the rear panel is a SET TRIGGER LEVEL switch, which presets the trigger level of either channel when the LEVEL knob is rotated to the SET detent. The three preset levels are 0V, +0.15V, and −0.13V. The 0V preset, the only one available on previous counters, is used for sine, square, or other symmetric waves. The two new presets enable easier measurement of logic signals; as the electronics world becomes increasingly digital, more counter users find themselves measuring the parameters of these signals. The new +0.15V preset sets the trigger level at one-tenth the threshold of TTL logic. This allows TTL measurements either with a 10:1 divider probe or with a direct probe and the built-in 10:1 attenuator of the 5308A. The −0.13V preset sets the trigger level at one-tenth the ECL threshold.

A SEPARATE/COMMON B switch, when set to COMMON B, connects the signal from the channel B input port to both internal channels. This allows time interval and time interval average measurements to be made from one point to another on a single input signal. Pulse width and rise time are the parameters most commonly measured using this mode. Unlike some other counters, the 5308A does not connect the input ports together in the COMMON B position. Instead, it completely disconnects the channel A port, coupling switch, and attenuator. This has three advantages. First, it prevents a signal source connected to one port from damaging another source connected to the other port. Second, in the frequency function, it allows switching between two independent signals at the two ports by simply sliding the SEPARATE/COMMON B switch from one position to the other. Third, it maintains a 1-MΩ input impedance when switched to the COMMON B mode.

Trigger and Gate Indicators

Adjacent to the LEVEL knobs are LED trigger indicator lights, another feature not previously available on 5300 snap-ons. These indicators blink when the channel is triggering at about 1 kHz or less, and glow steadily when triggered at higher frequencies. They also stretch a single narrow pulse or a single threshold crossing to produce a visible flash. Trigger indicating lights are always a convenience, and they can be nearly indispensable for setting up a two-channel measurement without benefit of a DVM.

When the main gate is open, a TTL low signal is

available at the GATE OUT connector on the rear panel. This signal can be used to intensify an oscilloscope trace of the input waveforms during time interval measurements, providing a graphic confirmation of the measurement being performed.

Use with "In-Between" Modules

In combination with the new 5300B mainframe, the 5308A provides a universal timer/counter with all the capability needed for most bench applications. With the addition of a 5310A Battery Pack, it becomes fully portable for field use. It can also take its place in instrument systems by using the 5311B Analog Output module[4] or the 5312A HP Interface Bus module.[5]

Acknowledgments

Definition of the 5308A was the result of discussions with Ian Band, Larry Johnson, Jim Horner, Bill Kampe, and Al Langguth. Product design was performed by Bruce Corya and Gary Schultheis. Bernie Barke did the industrial design. Pilot runs were shepherded by Roy Criswell, Burt Olson, Don Larke, and Jim Feagin.

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1. I.T. Band, H.J. Jekat, and E.E. May, "Lilliputian Measuring System Does Much, Costs Little," Hewlett-Packard Journal, August 1971.
2. R. Schmidhauser, "Measuring Nanosecond Time Intervals by Averaging," Hewlett-Packard Journal, April 1970.
3. "Time Interval Averaging," Hewlett-Packard Application Note 162-1.
4. J.F. Horner, L.W. Masters, and P.T. Mingle, "DMM and DAC Modules Expand Low-Cost Measuring System," Hewlett-Packard Journal, June 1973.
5. G.D. Sasaki and L.P. Johnson, "Minimal Cost Measuring Instruments for Systems Use," Hewlett-Packard Journal, January 1975.

Kenneth J. MacLeod

Ken MacLeod, a native of Philadelphia, Pennsylvania, holds a BA degree from Ursinus College (1969), a BSEE degree from the University of Pennsylvania (1970), and an MSEE degree from Stanford University (1973). With HP since 1970, Ken has designed hardware and software for a high-speed test system and served as principal designer of the 5307A and 5308A Counters. He's a member of the IEEE Computer Society. In his spare time, Ken is a pistol marksman who reloads his own ammunition. He also dabbles in politics, and he and his wife enjoy touring in the American West, using their home in San Jose, California as their base of operations. They're expecting their first child in August.

SPECIFICATIONS

HP Model 5308A 75 MHz Timer/Counter

Input Channels A and B

RANGE: dc Coupled: 0 to 75 MHz
ac Coupled: 20 Hz to 75 MHz

SENSITIVITY: (Min) 25 mV rms sine wave to 10 MHz, 50 mV rms sine wave to 75 MHz, 150 mV p-p pulse at minimum pulse width of 10 ns. Sensitivity can be decreased by 10 using Attenuator Switch.

IMPEDANCE: 1 MΩ shunted by less than 50 pF.

OVERLOAD PROTECTION:

DC RANGE:		
X1:	dc to 400 kHz	125 Vrms
	400 kHz to 5 MHz	5×10^7 V Hz product
	5 MHz to 75 MHz	10 Vrms
X10:	dc to 4 MHz	250 Vrms
	4 MHz to 75 MHz	1×10^8 V Hz product
AC RANGE:	dc to 10 Hz	200V peak or above ratings, whichever is lower.

TRIGGER LEVEL: PRESET position centers triggering at 0 volts, TTL or ECL threshold, or continuously variable over the range of ±2.0V or ±20V with attenuator in X10 position. Trigger level available on rear panel BNC connectors for DVM monitoring.

SLOPE: Independent selection of triggering on positive or negative slope.

CHANNEL INPUTS: Separate or Common B.

GATE OUTPUT: Rear panel BNC. TTL Low level while gate is open may be used to intensity modulate an HP oscilloscope.

TIME BASE/SCALING OUTPUT: Available at rear panel BNC.

Frequency

RANGE: 0 to 75 MHz. Channel A or Channel B. Direct count.

GATE TIMES: 8 manually selectable times from 1 μs to 10 seconds. AUTO position selects gate time for maximum resolution within a 1.1 second measurement time.

ACCURACY: ±1 count ± time base accuracy.

DISPLAY: Hz, kHz, and MHz with positioned decimal point.

Frequency Ratio

DISPLAY: Fa/Fb, measured over N periods of Fb. N = 1 to 10^8, selectable in decade steps with automatic decimal position and annunciators. AUTO position selects N automatically for maximum resolution within a 1.1 second measurement time.

RANGE: Channel A: 0 to 75 MHz. Channel B: 0 to 5 MHz.

ACCURACY: ±1 count of Fa ± trigger error of Fb*.

Period

RANGE: 0 Hz to 5 MHz. Channel B.

RESOLUTION: 100 ns to 10 s in decade steps.

ACCURACY: ±1 count ± time base accuracy ± trigger error*.

DISPLAY: μs, s, or ks with positioned decimal point.

Period Average

RANGE: 0-5 MHz. (200 ns to 10 s). Channel B.

PERIODS AVERAGED: 10-10^8 manually selectable in decade steps. AUTO position automatically selects number of periods for maximum resolution within a 1.1 second measurement time.

FREQUENCY COUNTED: 10 MHz.

ACCURACY: ±1 count ± time base accuracy ± trigger error*.

DISPLAY: ms (ns), μs, with positioned decimal points.

Time Interval

RANGE: 200 ns to 10^8 s. 25 ns minimum pulse width. Separate or Common B.

RESOLUTION: 100 ns to 10 s in decade steps.

ACCURACY: ±1 count ± time base accuracy ± trigger error*.

DISPLAY: μs, s, or ks with positioned decimal point.

Time Interval Average

RANGE: 1 ns to 10 s. Dead time between intervals, 200 ns. Minimum pulse width, 25 ns. Channels A and B separate or Common B.

INTERVALS AVERAGED: 1 to 10^8 selectable in decade steps. Auto position selects number of intervals to give maximum resolution within a measurement time of 1.1 second.

DISPLAY: ms (ns), μs, or s with positioned decimal point.

ACCURACY:

$$\pm \text{Time base accuracy} \pm 5\text{ ns} \pm \frac{[\text{Trigger Error}^* \pm 100\text{ ns}]}{\sqrt{\text{Intervals Averaged}}}$$

Totalize

Totalizes Channel A while Channel B is low.

Totalizes Channel A between pulses on Channel B.

RANGE: 75 MHz on Channel A in X1 position, 10 MHz in other positions.

ACCURACY: ±1 count ± trigger error on Channel B*.

DISPLAY: Displays count. Can scale display with annunciator by use of time base switch to increase count capacity.

General

NOTE: 5308A is compatible with 8-digit 5300B mainframe only.

CHECK: Inserts internal 10 MHz reference frequency into counting decades. Displays 10^7 counts for X10 through X10^8 position with proper decimal position and annunciator.

OPERATING TEMPERATURE: 0° to 50°C.

POWER REQUIREMENTS: Including 5300B mainframe, nominally 15 watts.

WEIGHT: Net, 0.9 kg (2 lb).

DIMENSIONS: With mainframe 89 mm H (3½") × 160 mm W (6¼") × 248 mm L (9¾").

PRICE IN U.S.A.: 5308A, $450
5300B, $460

MANUFACTURING DIVISION: SANTA CLARA DIVISION
5301 Stevens Creek Boulevard
Santa Clara, California 95050

*For any waveshape, trigger error (μs) is less than ±0.005/Signal Slope (V/μs). For period average, this is less than ±0.3% of one period ÷ periods averaged for signals with 40 dB or better signal-to-noise ratio.

A High-Current Power Supply for Systems That Use 5-Volt IC Logic Extensively

This switching-regulated power supply gives 100A at 5 V with 70% efficiency. A heat-removal system allows compactness without loss of reliability.

by Mauro DiFrancesco

ONE OF THE PECULIARITIES OF THE present technical environment is that power supplies are often as large as the systems they power. Large-scale integrated-circuit technology does not necessarily reduce power consumption in proportion to size.

This situation has spurred developments in switching regulated power supplies, which are much smaller and less wasteful of power than equivalent series regulated supplies. This article describes a new switching regulated supply (Fig. 1) that delivers up to 100 amperes at 5 volts but is only one-third the size and has only one-fifth the weight of an equivalent series-regulated supply. It's designed for original equipment manufacturers (OEMs) who use large amounts of 5-volt logic in CPU's, add-on memory systems, computer peripherals, telecommunications systems, and other digital equipment.

Although smaller size and lower power consumption are obviously the major benefits of this kind of supply, other benefits are not immediately apparent. For example, though the purchase price is some 10 to 15% higher than that of an equivalent series-regulated power supply, long-term costs are lower, a result of the higher efficiency. Since power dissipated (P_D) is related to power output (P_o) by

$$P_D = \left(\frac{1}{E} - 1\right) P_o,$$

it can be seen that a 500-W switching supply with an efficiency (E) of 70% dissipates 215 W, while a typical 40% efficient series-regulated supply dissipates 750 W. Assuming a typical electrical power cost of 3.5 cents per kilowatt-hour, the price differential would be recovered in only six months of operation, and this without taking into account additional savings from the reduction in needed cooling equipment and the power it uses.

The price of the switching regulated power supply can be expected to remain stable over the years as the cost of the expensive semiconductors it uses continue to decline, a factor of importance to systems manufacturers now designing new equipment. The price of other types of power supplies, on the other hand, can be expected to rise because of the greater use of basic raw materials, principally aluminum, copper and iron, that are growing in cost.

Efficient Performance

The new power supply, Model 62605M, is a modular type designed for permanent installation. It occupies only ¼ cubic foot (7700 cm³) and weighs 14 lb (6.4 kg). Its 5-volt output remains constant within 0.1% with any load from 0 to 100 amperes and the output returns to within 1% of nominal in less than

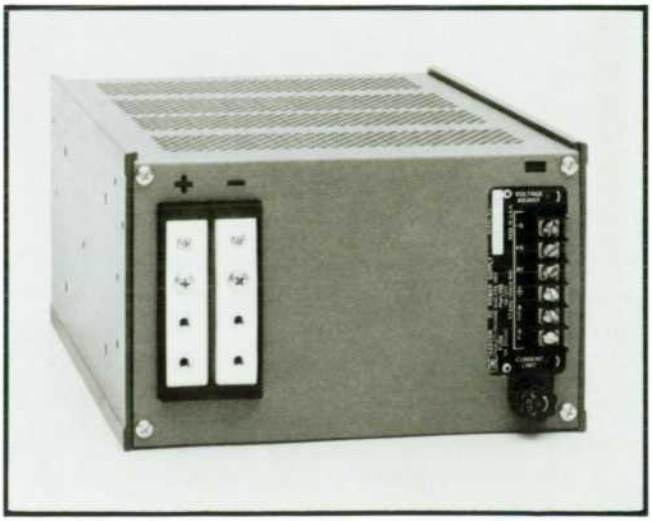


Fig. 1. *Model 62605M Power Supply, designed for permanent installation, supplies current in a range from 0 to 100 A at 5 V. The switching regulator achieves 70% efficiency at full output.*

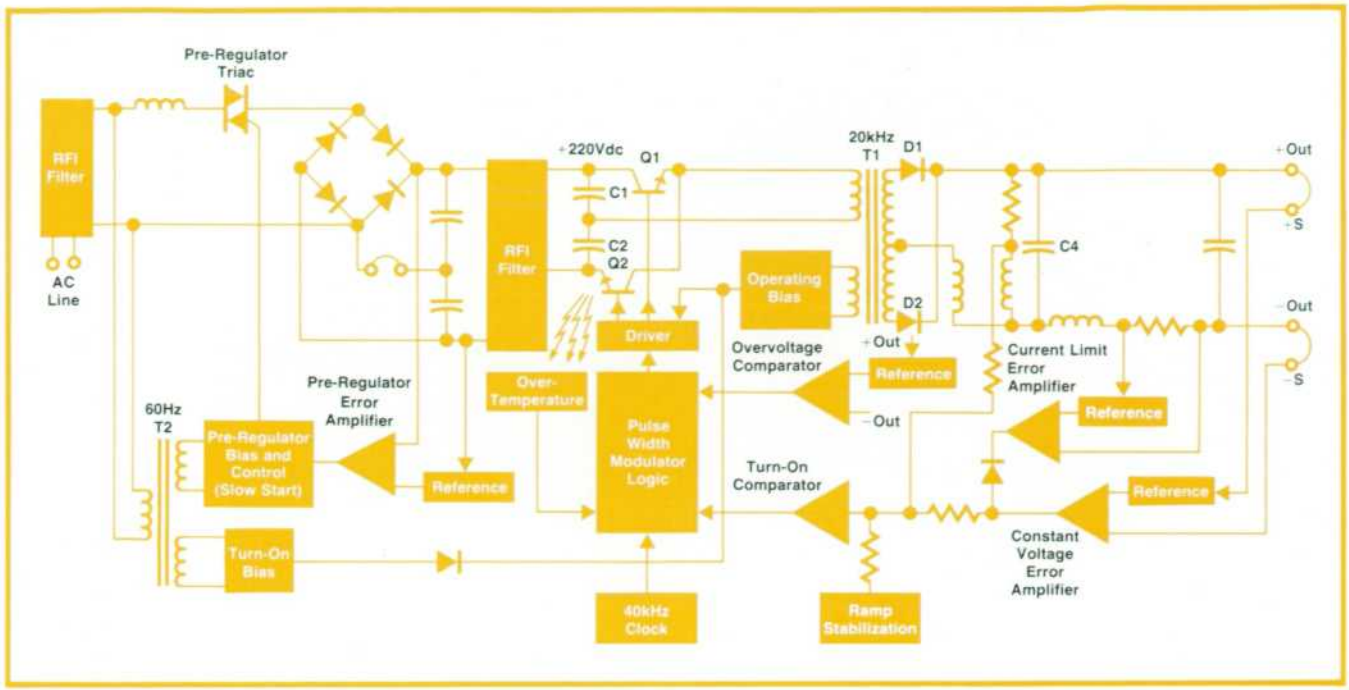


Fig. 2. *Block diagram of the Model 62605M modular power supply. It operates directly from a 220V power line when the shorting strap is in place. With the strap removed (and some other minor changes), the input rectifiers no longer function as a bridge but become a voltage doubler that enables use on a 120V line.*

1.5 ms following a 50-ampere change in load. Ripple and noise (PARD) are less than 50 mV p-p (20 Hz to 20 MHz) and drift is less than 0.1% over an 8-hour period. The isolated output allows either output terminal to be grounded. It has overvoltage, overcurrent, overtemperature and reverse voltage protection.

Basic Considerations

During the conceptual stage of the power supply design, particular attention was devoted to the components in the main power mesh as this is where the major expense is and where the most heat is generated. Taking the effect of these components on cost effectiveness and on size and weight as a primary consideration, the block diagram of Fig. 2 evolved.

The use of a line-synchronous preregulator was a key factor in obtaining our objectives. First of all, by holding the input to the switching regulators relatively constant, it permitted the use of lower voltage transistors and capacitors, the two costliest items in the power supply. The coarse regulation it provides also allows the main regulator to achieve finer regulation with a minimum of additional gain.

A third benefit results from the inclusion of a slow-start circuit that the preregulator circuit allowed us to incorporate. This prevents large powerline current surges at turn-on which, at this power level, could weld switch contacts and trip circuit breakers, or cause line-voltage transients that affect other equipment.

The main regulator operates similarly to other switching regulated power supplies developed by Hewlett-Packard.[1] In brief, transistors Q1 and Q2 alternately generate rectangular pulses that are stepped down in voltage by transformer T1, rectified by diodes D1 and D2 and smoothed by the LC networks that follow. The voltage-error amplifier responds to changes in the output voltage, adjusting the width of the Q1-Q2 pulses to bring the output voltage back to nominal.

Because Q1 and Q2 are alternately either fully turned on or completely turned off, the power dissipated in these components is much reduced over that of a series-pass regulator. This is one of the major benefits of the switching regulator.

Another benefit arises from the 20-kHz pulse repetition rate, which allows the use of much smaller —and hence lighter—transformers, chokes, and filter capacitors.

Heat Removal

Although the new supply is 70% efficient, that means that upwards of 200W is dissipated at this power level. Removing this heat to allow use of a smaller enclosure presented an interesting design challenge.

The principal sources of heat are the switching transistors, about 30 watts each, and the power rectifiers, 35 watts each. To achieve reliability goals, heat

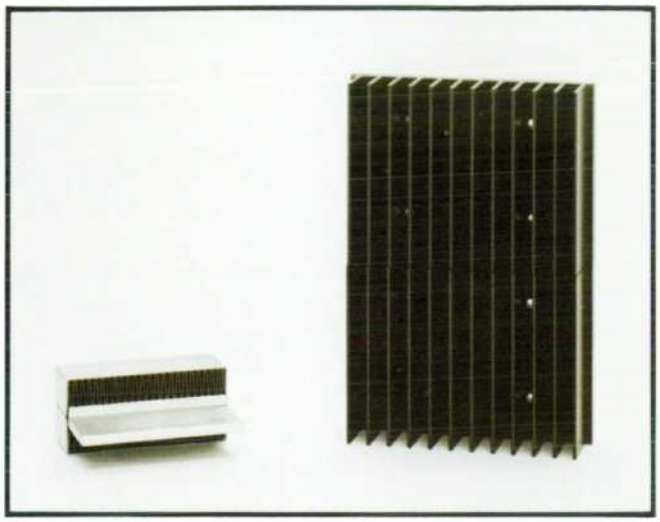


Fig. 3. *Heat is removed from the power mesh through a heat exchanger (left) that rises in temperature only 0.5°C/W with an air flow of 10 ft³/s. An equivalent convection-cooled heat sink is shown on the right.*

sinks with thermal resistances of about 0.5°/W would be required to hold junction temperatures below 125°C in a 40°C environment. This ruled out convection cooling because of the huge heat sink that would be required. Therefore it was decided to use forced-air cooling and a heat sink made with convoluted fin stock (Fig. 3), about the most efficient thermal convector available. An air duct concentrates the air flow where needed most.

The overall decrease in component temperatures achieved by the use of forced-air cooling resulted in a higher MTBF (mean time before failure) than would have been possible with convection cooling. MTBF, according to HP quality assurance procedures, is 45,000 hours*.

Considerable size and weight reductions in the magnetics, as well as cost, was also made possible by the more efficient cooling (see Fig. 7).

Forced-air cooling can have disadvantages, however. These include fan unreliability, dust clogging, air intake blockage and the need for maintenance. All were considered in the design. The fan selected is a self-lubricated, low-speed, high-reliability fan that has an MTBF exceeding 80,000 hours and that needs no maintenance. Tests in a dusty environment showed that cooling is not adversely affected by a build-up of dust inside the power supply but if the user deems that an air filter is necessary, one can be added with insignificant degradation in cooling performance. If the air intakes or outlets should be blocked inadvertently, causing a rise in internal temperature, a thermal switch shuts off the supply to prevent damage.

*By contrast, an equivalent series-regulator supply using 20 pass transistors in parallel on a heat sink that maintains junction temperatures below 160°C, would have a MTBF of 25,000 hours.

Electrical Noise

One of the main objections to switching-regulated power supplies has been the generation of electromagnetic interference (EMI). This interference can be conducted out the power line and out the dc output, or it can be radiated. In working out the design of the Model 62605M, three major sources of EMI had to be contended with: the preregulator triac, the switching transistors, and the main rectifiers. The triac noise is controlled by a rather large 120-Hz filter choke in series with the line. The 20-kHz noise generated by the switching transistors is controlled by two LC filter sections in the main power mesh. Electrostatic shielding in the main power transformer (T1 in Fig. 2) prevents this noise from being conducted to the secondary.

Noise from the rectifiers was controlled by several techniques. First, the main transformer is designed to minimize leakage inductance, which provides an impedance across which current transients develop voltage noise. Second, RC damper networks across the rectifiers reduce current transients by preventing rapid changes in rectifier current. Third, the Schottky rectifiers used virtually eliminate reverse recovery current that would act on what little leakage inductance there is. As a result, even though more than 100A is being switched on and off at a 20-kHz rate, noise at the output is less than 15 mV rms, or 50 mV p-p (20 Hz to 20 MHz).

Radiation is controlled by the air duct, a sheet-metal enclosure that surrounds the power mesh.

Mechanical Design

A primary goal in the mechanical design was ease of assembly and disassembly for serviceability. A disassembled unit is shown in Fig. 4. The central module (A) contains the inductor and capacitors used to filter the preregulator output. The right side (B) has the small-signal control circuits, EMI filters, and the ac line rectifier and preregulator triac. This assembly plugs on to the central circuit board. The power output assembly is mounted on the left-side circuit board (C) which is inserted in the air duct/radiation shield (D). This plugs on to the other side of the central circuit board. A cover and eight screws complete the assembly. It can be completely disassembled with a screwdriver in only three minutes, and there are no wires to unsolder.

The design complies with the safety requirements of the International Electrotechnical Commission (IEC 348) and the unit is being submitted to the Underwriters' Laboratory for approval under UL Standard 478. These are important considerations for this type of supply because of the number of internal components connected to the ac power line.

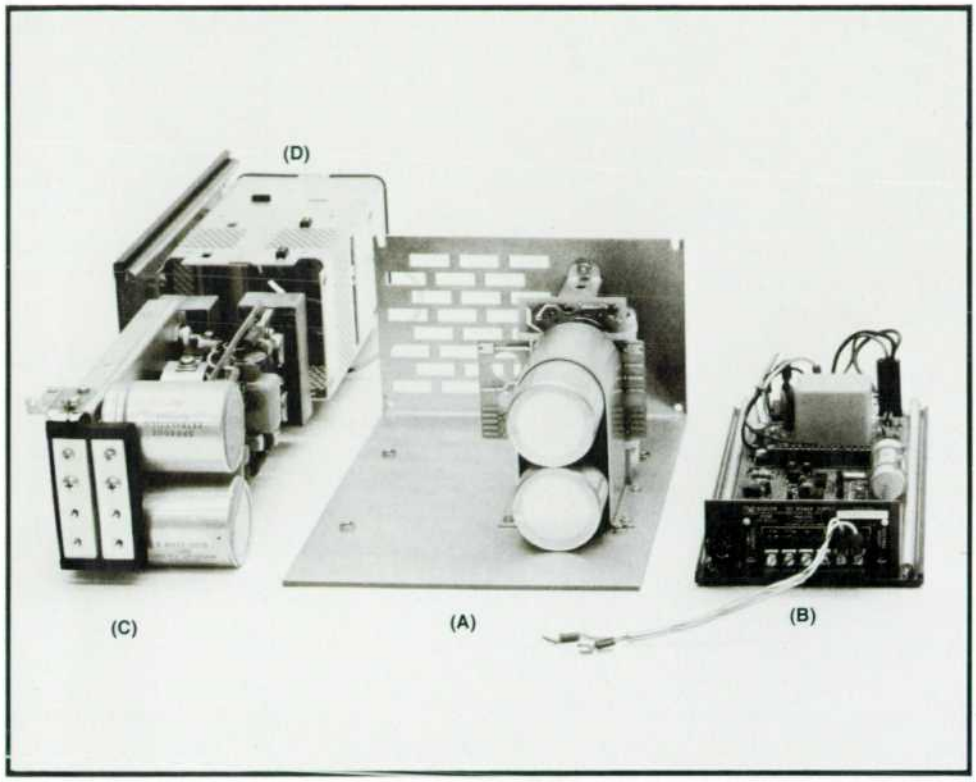


Fig. 4. *Modular construction simplifies assembly and disassembly.*

Circuit Details

Operation of the preregulator is diagrammed in Fig. 5. The rectified line voltage is compared to a reference and the result used as an error signal to control the slope of a ramp voltage (waveform C). The ramp is compared to the rectified sine wave (B) and when the two coincide, the triac is gated on.

If the preregulator output voltage were low compared to the reference, a steeper ramp would be generated. This results in an earlier gate pulse and, consequently, more electrical charge into the line rectifiers to restore the output voltage to the desired level.

Capacitor C3 provides loop stabilization but it also insures slow start-up by preventing the ramp from being too steep at turn-on. The result is a slowly increasing triac conduction angle at turn-on.

The preregulator's 220V output is converted to 5V by the two-transistor switch and transformer shown in Fig. 6. The two-transistor configuration was considered most cost effective for the switch even though four smaller transistors, which would be operated in a bridge to achieve the desired power level, cost much less. Analysis showed that the added cost of the extra components needed to assure proper timing in the

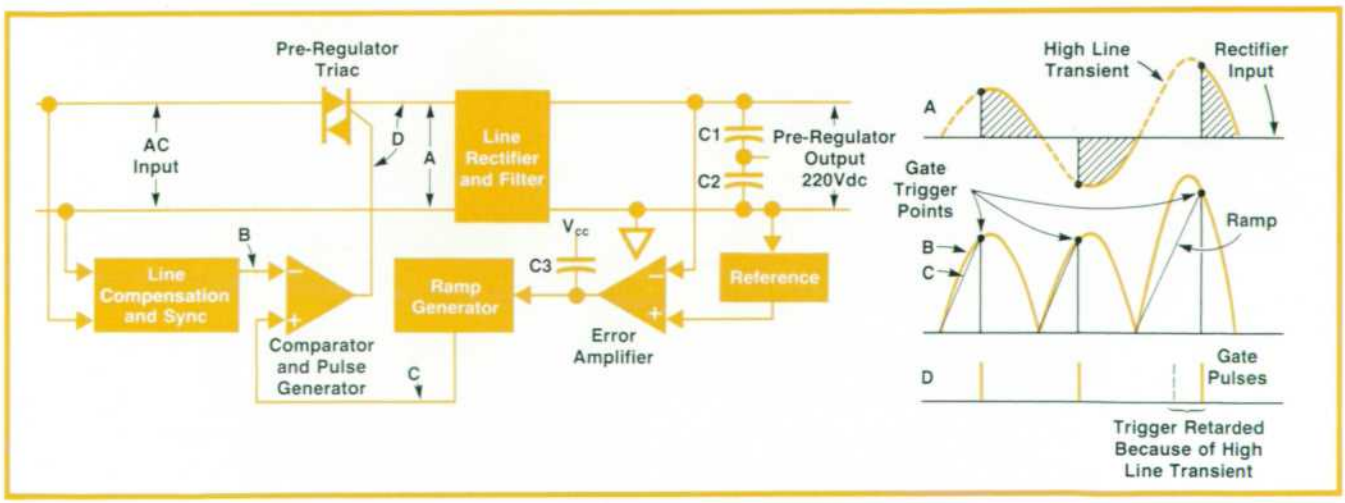


Fig. 5. *Block diagram of the preregulator section. Operation is explained by the waveforms, which also show how the preregulator responds immediately to a change in line voltage.*

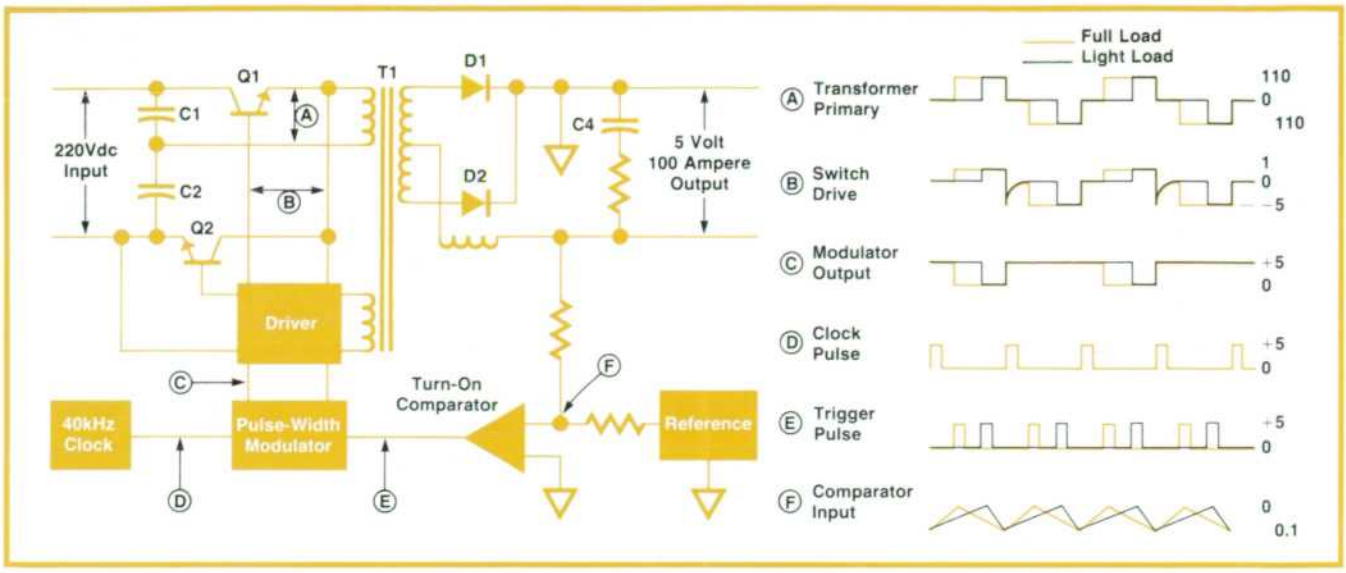


Fig. 6. *Switching regulator circuit operates at 20 kHz, a repetition rate that is an optimum compromise with respect to cost, size, dissipation, parts availability, and acoustic noise. The colored waveforms show full-load operation. The black waveforms are typical of lightly loaded operation.*

bridge circuit would negate the lower cost of the smaller transistors.

The waveforms shown in Fig. 6 describe the operation of the regulator. The output is summed algebraically with a reference voltage of opposite polarity to derive an error voltage near the zero level. As in other switching regulators, the dc output following the first LC filter has a triangular ripple. When neither switching transistor is on, current drawn by the load from capacitor C4 generates the rising portion of the triangular waveform (it's taken from the negative bus). When the ripple reaches the zero level, the comparator turns on one of the switching transistors, which then charges C4, reversing the slope of the ripple. The transistor remains on until turned off by the next-occurring clock pulse.

If less current were drawn from the power supply, the upward slope of the ripple would be less and transistor turn-on would occur at a later time with respect to the clock pulses. The conduction time of the transistor would thus be shorter, maintaining the output voltage at a constant level.

Steering logic in the modulator causes the two switching transistors Q1 and Q2 to turn on alternately, resulting in the bipolar pulse train on the primary of transformer T1 (waveform A). However, due to inherent differences in circuit delays, the on times of the transistors could differ slightly, thus giving rise to a dc component in the current supplied to T1. If allowed to continue, the dc current would eventually build up to a level sufficient to saturate T1, ultimately leading to the destruction of the transistors. To eliminate this possibility, the transformer is accoupled to the preregulator by capacitors C1 and C2. A dc component in the switching transistors causes a net charge on the capacitors that shifts the bias on the transistors, compensating for the unbalance. As a result, T1 receives equal positive and negative volt-second pulses.

The power required to drive the switching transistors is about 30 watts. Drive power usually is obtained directly from the power line through a bias transformer, but for this supply, a 2½-lb, 12-cubic inch transformer (1 kg, 190 cm^3) would be needed. Significant size and cost savings were realized by obtaining the drive power from an auxiliary winding on main power transformer T1. This required a 5% increase in the size of T1 but since T1 weighs only 7 oz (0.2 kg), the increase was insignificant. An auxiliary winding on the preregulator bias transformer (T2 in Fig. 2) supplies the small amount of bias need for start up of the switching operation.

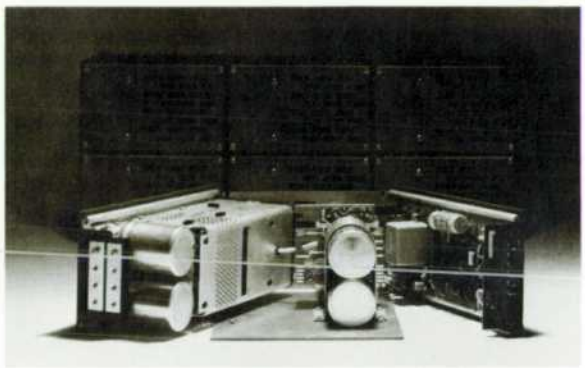
Mauro DiFrancesco

Mauro DiFrancesco has been specializing in heavy-duty power supplies ever since joining Hewlett-Packard in 1964. His first project was a modular power supply for vacuum-tubes, and he contributed to the 0.2-2 kW LVR series, among several others, before assuming responsibility for the 62605M. Mauro has BSEE and MSEE degrees from Rutgers University (Brunswick, N.J.). Only recently married, he enjoys amateur sports: softball, basketball, tennis, golfing, and skiing.

SPECIFICATIONS

Model 62605M 100-W Switching Regulated Modular Power Supply

OUTPUT VOLTAGE: 5 V ±0.25 V.
OUTPUT CURRENT: 100 A at 40°C.
DC OUTPUT ISOLATION: output is isolated from chassis ground. Either output terminal may be grounded.
LOAD EFFECT (load regulation): 0.05% from 0 to 100% of rated output current.
SOURCE EFFECT (line regulation): 0.05% for any change within input voltage range (104-127, 187-250 V ac).
PARD (ripple and noise): less than 15 mV rms, 50 mV p-p (20 Hz to 20 MHz).
TEMPERATURE COEFFICIENT: less than 0.02%/°C.
DRIFT (stability): less than 0.1% over 8-hour interval following 30-minutes warmup.
LOAD EFFECT TRANSIENT RECOVERY: Output voltage returns to within 1% of nominal in less than 1.5 ms following a load change from 100% to 50%, or 50% to 100%.
TURN-ON AND TURN-OFF TRANSIENT: no overshoot outside of regulation and ripple band. Output voltage decreases smoothly after carryover time.
CARRYOVER TIME: output voltage remains within 2% of specified nominal for more than 15 ms while delivering full load current following removal of ac input power.
OPERATING TEMPERATURE: 0 to 40°C ambient. Output current for continuous operation is derated linearly from 100 amps at 40°C to 60 amps at 70°C.
COOLING: Built-in fan.
THERMAL PROTECTION: internal thermostat shuts off output for an overtemperature condition.
REVERSE VOLTAGE PROTECTION: supply is protected against application of reverse polarity voltage across output terminals. Maximum steady state reverse current can be up to 25% of rated output current.
AC INPUT PROTECTION: 15 A line fuse (for 120 V ac operation) in extractor post on rear of supply.
INPUT POWER:
LINE: 104-127 V ac (187-250 V ac with Option 106), 48-63 Hz, single phase.
LINE CURRENT: 11.5 amps rms maximum at 127 V ac line.
INPUT TRIP SIGNAL: contact closure between terminals A1 and +S on rear barrier strip remotely trips overvoltage circuit.
OVERVOLTAGE TRIP SIGNAL: terminal A1 has voltage of 15 V ±2 V with respect to +S under normal operating conditions. This voltage falls to approximately 0.8 volts when overvoltage occurs. Terminal A1 can supply 0.1 mA in the high state and can sink 10 mA in the low state.
REMOTE SENSING: terminals are provided which correct for lead-voltage drop of up to 0.25 V while maintaining 5 V at the load. Load is protected if sensing leads are inadvertently opened.
MOUNTING: supply can be mounted in any position provided air intake and outlet holes are not blocked.
DIMENSIONS: 20.7 cm W × 12.8 cm H × 29.2 cm D (8.14 × 5.03 × 11.50 inches).
WEIGHT: 6.4 kg. (14 lb).
PRICE IN U.S.A.: 62605M, $650.
MANUFACTURING DIVISION: NEW JERSEY DIVISION
Green Pond Road
Rockaway, New Jersey 07866



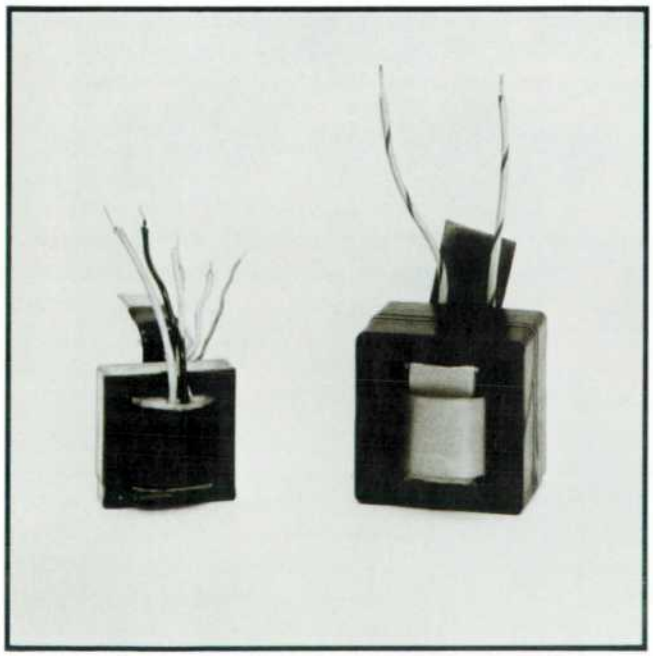


Fig. 7. *Efficient cooling also reduced the size of the magnetic components. Main power transformer T1 on the left handles 500 watts with the forced-air cooling. By comparison, the convection-cooled transformer on the right can handle only 200 watts.*

Acknowledgments

Bob Peck provided much appreciated counsel and advice on the basic configuration. Tim Kriegel, Rich Myers, Win Seipel and Mike Benes contributed to the electrical design with much help provided by technician George McGreen. The mechanical design was by Don Pauser with help from Tom Cox.

Reference

1. B.W. Dudley and R.D. Peck, "High Efficiency Modular Power Supplies Using Switching Regulators", Hewlett-Packard Journal, December 1973.

Band-Selectable Fourier Analysis

Frequency resolution in selected bands can be as much as 100 times better than conventional baseband Fourier analysis.

by H. Webber McKinney

FOURIER ANALYZERS are computer-based instruments that take advantage of the fast Fourier transform to perform digital spectrum analysis of input signals in the frequency range dc to 100 kHz. They are widely used in the analysis of mechanical structures, vibrations, communications networks, electronic circuits, control systems, and many other devices and physical phenomena.

Because of their dependence on the Fourier transform, Fourier analyzers have been limited to baseband spectral analysis, that is, the frequency band under analysis always extends from dc to some maximum frequency determined by the rate at which the input signal is sampled. A problem with baseband analysis is that, to increase the frequency resolution for a given sample rate, the number of lines in the computed spectrum must increase, and this requires a corresponding increase in the number of samples used to compute the spectrum. As the number of samples increases, processing time and computer memory requirements multiply rapidly, thus placing a practical limit on frequency resolution.

Band-Selectable Fourier Analysis

Band-selectable Fourier analysis, or BSFA, a new capability of the HP 5451B Fourier Analyzer, is a measurement technique that makes it possible to perform Fourier analysis over a frequency band whose upper and lower frequencies are independently selectable. BSFA provides increased frequency resolution without increasing the number of spectral lines stored in the computer. The improvement in resolution is greater than 100 times, compared to standard Fourier analysis. Dynamic range is maintained at 80 dB when the major signal is within the selected band, and is increased to 90 dB or more when the major signal is outside the band. The upper frequency limits for BSFA power spectrum and frequency response measurements are 19 kHz and 9 kHz, respectively The lower limit is dc.

Figs. 1 and 2 show the advantages of BSFA in power spectrum measurements. Fig. 3 shows a two-channel, transfer function BSFA measurement. In a BSFA measurement the sampled input signal is digitally filtered to remove all information outside the

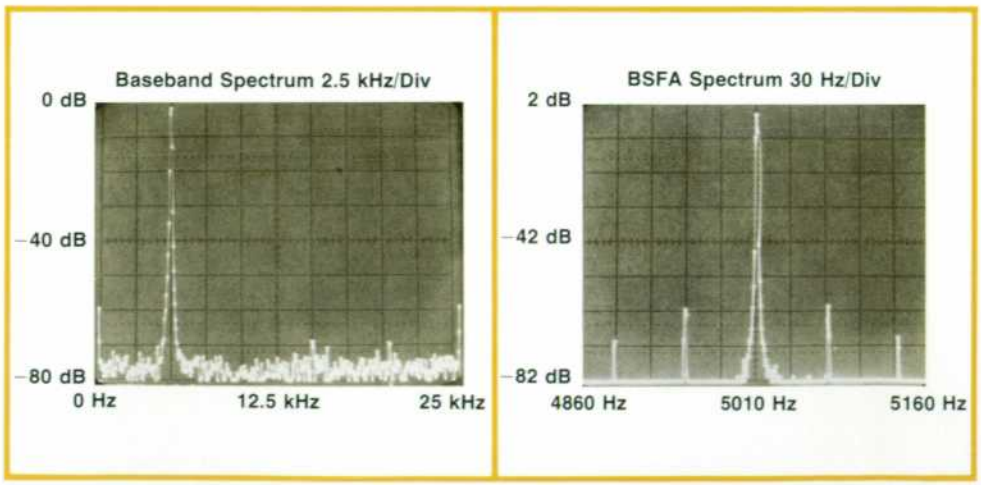


Fig. 1. *The resolution and dynamic range improvements of band-selectable Fourier analysis (BSFA), a new capability of the 5451B Fourier Analyzer, are demonstrated by these power spectra of the output of a sine wave generator. The conventional baseband spectrum shows the 5-kHz fundamental and the third harmonic at −69 dB. The noise floor is 72 dB down. The BSFA spectrum shows that the fundamental is actually at 5010 Hz and that there are 60-Hz and 120-Hz sidebands. The noise floor is greater than 80 dB down.*

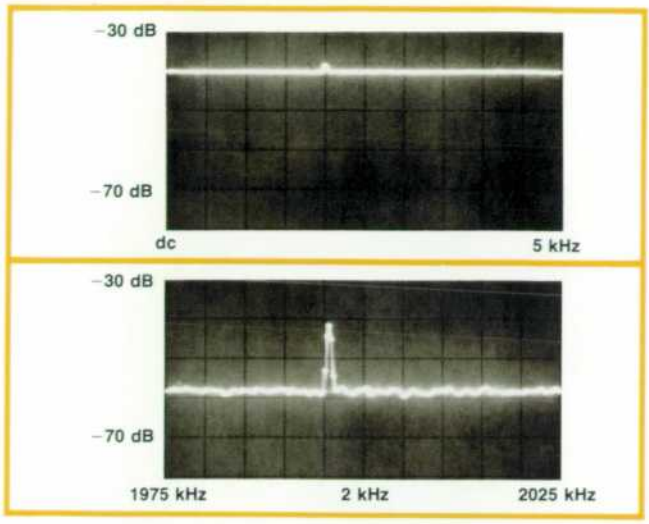


Fig. 2. *In the baseband spectrum of a sine wave buried in white noise the sine wave appears only 2 dB above the noise after 10 000 averages. In the BSFA spectrum after only 100 averages, the sine wave is 17 dB above the noise and consequently is much more detectable. BSFA's 100 × improvement in resolution results in a reduced mean value for the white noise; however, the noise variance is greater because fewer measurements were averaged. The two measurements required the same total time.*

specified frequency band, and only samples corresponding to the desired frequency band are stored. The increased dynamic range of BSFA is a result of the sharp rolloffs of the digital filters, and of the increased resolution, which reduces the effect of the white quantizing noise of the Fourier analyzer's analog-to-digital converters (see reference 1). Out-of-band signals are attenuated by at least 90 dB relative to a full-scale in-band spectral line.

The Fourier analyzer operator may identify the frequency band of interest either by specifying the bandwidth and center frequency or by specifying the upper and lower limits of the band as percentages of the currently displayed bandwidth. The system calculates the best fit to the operator's request and prints out the actual band. 95% coverage of the requested band is assured if the requested band is within the allowable range.

BSFA measurement bandwidths are selectable in steps of (sample frequency)/5n, where n is an integer. Center-frequency settability is always better than 0.1% of the maximum frequency. Center frequency and bandwidth stability are better than one part in 10^6.

How BSFA Works

Fig. 4 shows the signal flow in a normal baseband Fourier frequency spectrum measurement. Also shown in Fig. 4 are the spectra of the input signal, the output of the anti-aliasing filter, and the sampled signal, and the resulting Fourier transform. Notice that

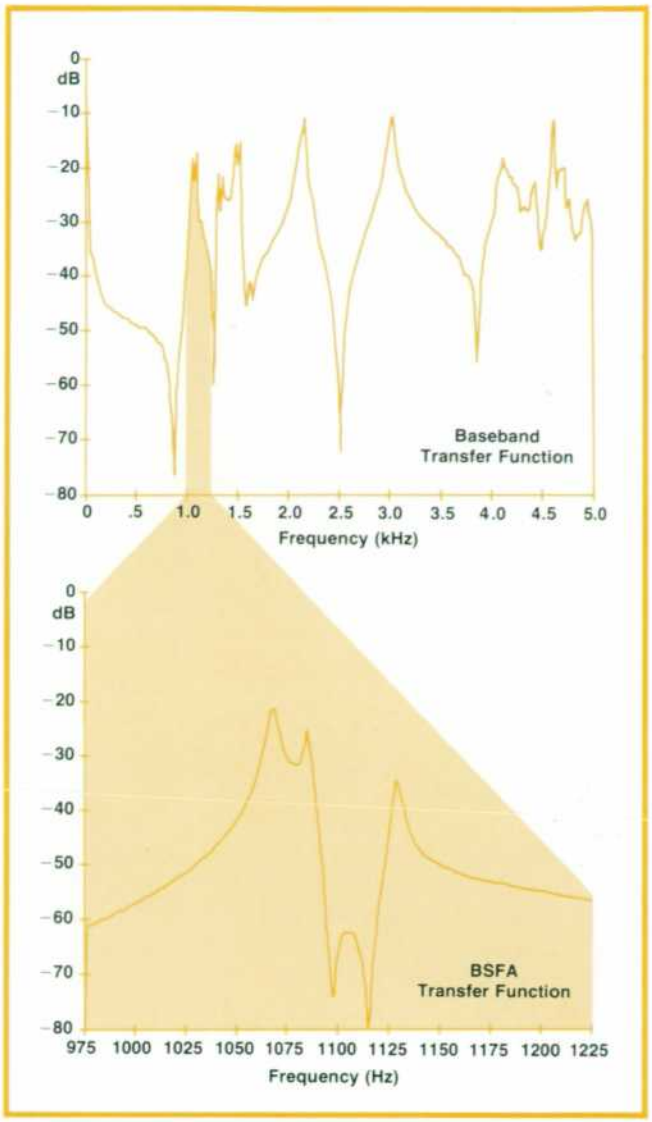


Fig. 3. *In this mechanical impedance measurement on a squeaky automobile disc brake rotor, BSFA made possible an accurate determination of the modes of vibration and the damping associated with each mode.*

for a fixed sampling frequency F_s the spacing of the spectral lines (Δf) is inversely proportional to the number of samples (N).

The time required for the fast Fourier transform is proportional to $N\log_2 N$. For values of N greater than 256 this time increasingly dominates the total processing time for Fourier analysis measurements. Also, as many as 6N words of computer main memory may be required for data storage in transfer function measurements, making it prohibitively expensive to allow N to be more than a few thousand. This limits the attainable Δf.

Baseband Fourier analysis gives equal frequency resolution from dc to half the sampling frequency. If equal resolution is required then the restrictions of baseband analysis are unavoidable. However, most

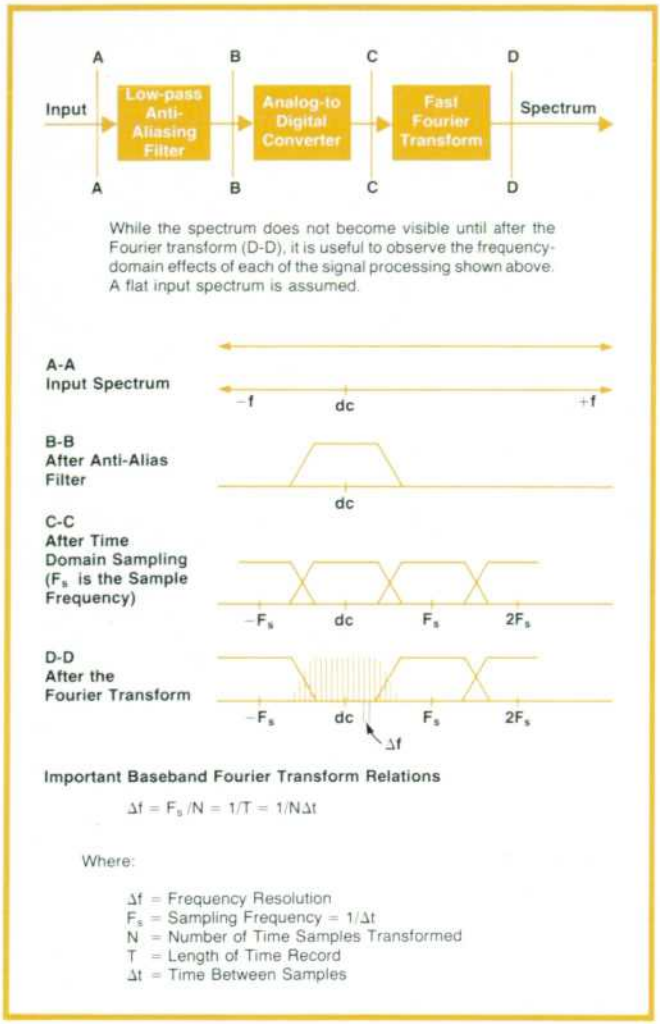


Fig. 4. *Signal flow in baseband Fourier Analysis, showing spectra that result from individual processing steps. A flat input spectrum is assumed.*

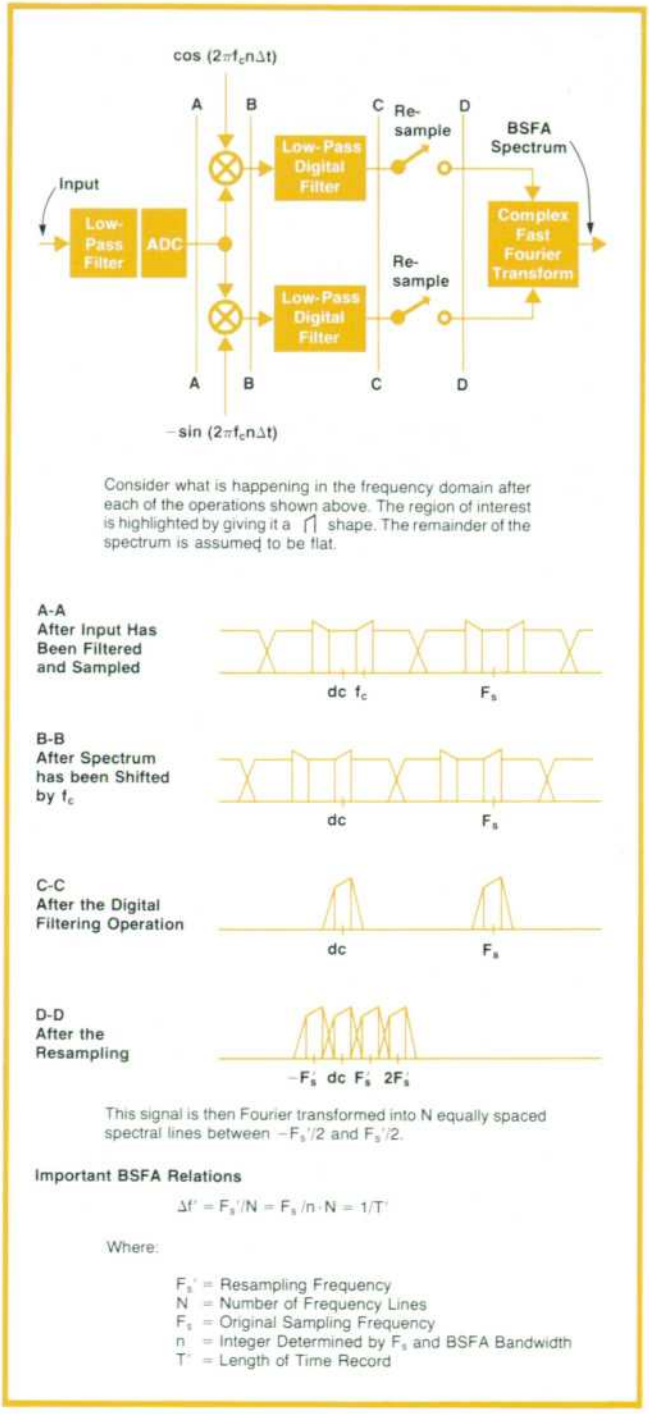


Fig. 5. *BSFA signal flow. A frequency shift by f_c centers the analysis band on the frequency of interest and digital filtering removes information outside the band of interest.*

measurements require high resolution over only a portion of the baseband. This is where BSFA makes its contribution.

Fig. 5 shows the signal flow in a BSFA frequency spectrum measurement. Also shown are the spectrum of the filtered, sampled input signal and the spectra resulting from a frequency shift by an amount f_c, the digital filtering operation, and resampling at a rate F'_s. The results of resampling are Fourier-transformed into N equally spaced spectral lines between $-F'_s/2$ and $F'_s/2$. Resolution is

$$\Delta f' = F'_s/N = F_s/nN = 1/nT = 1/T'$$

where F_s is the original sampling frequency, F'_s is the resampling frequency, N is the number of spectral lines, T′ is the length of the time record of the input signal, and n is an integer determined by F_s and the selected BSFA bandwidth. Thus resolution is improved by a factor of n over a baseband measurement. However, the time record of the input signal is n times as long, and nN input samples are required, even though only N points are stored.

Digital Filtering

Computationally efficient digital filters that have high out-of-band rejection are the primary requirement for band-selectable Fourier analysis. Fig. 6

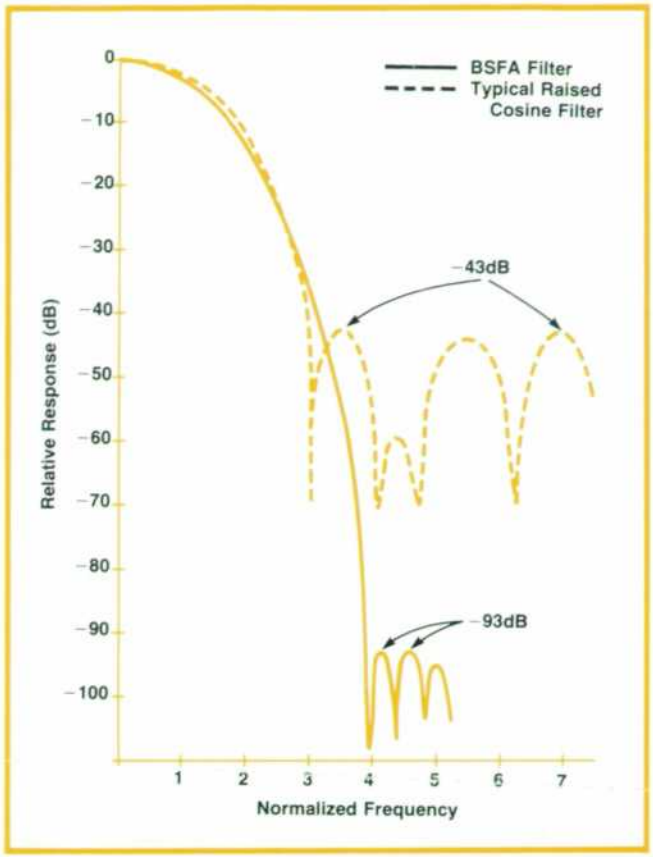


Fig. 6. *BSFA digital filters have high out-of-band rejection, a primary requirement for BSFA. Here the BSFA filter frequency response is compared with a commonly used raised cosine filter. Note the 50 dB greater out-of-band rejection of the BSFA filter.*

shows the frequency response of the digital filters used in the 5451B. The response has a −3 dB to −90 dB shape factor of four for all bandwidths. The passband is flat only within 3 dB, but the filter shape is known precisely and results are corrected to 0.1 dB accuracy after the Fourier transform operation.

The filtering operation is performed by convolving the impulse response of the filter with the sampled input waveform. Convolutional digital filters have an advantage over recursive filters in that they are inherently stable. In an operation like BSFA, where the filtering operation is followed immediately by resampling, convolutional filters have the additional advantage that only the outputs that will be selected in the resampling need ever be calculated. Thus filtering and resampling are merged, greatly increasing computational efficiency.

For even greater efficiency a filter having a symmetrical impulse response is used. By summing appropriate pairs of input samples and then convolving the pairs with half the impulse response, the number of required multiplications is cut in half. As a result, each BSFA filter requires only 2½ multiplications per input point.

Digital filter bandwidth is tuned by changing the length of the filter impulse response.

Reduced Storage

The amount of computer memory needed to store BSFA data is considerably less than would be required in a baseband measurement of the same frequency resolution. This is true even though the length of the measured input record is also the same.

BSFA requires less storage because the entire sampled time record is never stored in the main computer memory all at once. Instead, it is broken into N shorter records, each of which is processed individually, and only N points are stored. For a 100× improvement in resolution relative to a baseband measurement with the same number of spectral lines about 1.2K additional words of storage are required for BSFA buffers. In a baseband measurement 100N words would be required for the same resolution, or 102,400 words for N = 1024, a typical number.

The Frequency Shift Operation

The frequency shift is required in BSFA to center the digital filter on the frequency band of interest. According to the Fourier shift theorem, shifting a signal's frequency spectrum is equivalent to multiplication of the signal by a complex exponential. Such a function has a cosinusoidal real part and a sinusoidal imaginary part. For BSFA, samples of the real and imaginary parts are synthesized, and the data samples are multiplied by them, as shown in Fig. 5.

Because all of the BSFA computations are linear, the complex exponential could multiply the filter impulse response instead of the input data. This implicit shift saves two multiplications per input point and reduces the total number of multiplications per input sample to five.

The implicit shift approach has the disadvantage of restricting the center frequency of the selected band to being an integer submultiple of the sampling frequency. As a result, a tunable sampling frequency is required to provide unrestricted center frequency selection. The 5451B BSFA option uses both implicit and explicit shifts. The implicit shift is used whenever maximum processing speed is needed.

On-Line and Off-Line BSFA

The 5451B BSFA software performs both on-line and off-line analysis. In the on-line mode, the one or two input signals from the analog-to-digital converters are processed immediately, and only the shifted, filtered, reduced data is stored in the computer memory. This means that the BSFA computations must be done fast enough to keep up with the incoming sample rate. For maximum speed, the implicit frequency shift is used, resulting in a word processing rate greater than 18 kHz.

In the off-line mode, up to 32 channels of digitized input data can be stored on magnetic tape or disc and band-selectable Fourier analysis can be performed on any part of it. The explicit frequency shift is used because the sampling frequency is fixed when the data is originally recorded, and therefore cannot depend on the analysis band, which must be selectable. Processing speed is not a problem because the entire sampled input is stored and can be read and processed off-line at a slower rate than the original sampling rate with no loss of information.

For off-line BSFA, the maximum useful frequency is determined by the rate at which data can be transferred from the analog-to-digital converters to the mass storage device without losing any samples. For the 5451B Fourier Analyzer and the HP 7900A Disc Drive the transfer rate is 39,000 samples per second.

Microcode

Band-selectable Fourier analysis is a combination of software and firmware. The computer in the 5451B is the microprogrammable HP 2100S. The digital filters and all time-critical BSFA operations are implemented in 2100 microcode.

Acknowledgments

Harold Sampson and Dave Snyder provided microcode and lots of additional help.

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H. Webber McKinney

Webb McKinney received his BSEE and MSEE degrees in 1968 and 1969 from the University of Southern California. After joining HP in 1969, he spent a year as a sales and applications engineer, then moved into the Fourier Analyzer development lab, where he helped design the 5470A Fast Fourier Processor and served as Band Selectable Fourier Analyzer project manager. He was born in Upland, in southern California, and now lives in Los Altos, a few hundred miles farther north. He's married and has a small daughter. Webb enjoys the time he spends with his family and friends, and in the out-of-doors, camping and hiking. He also plays guitar.

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