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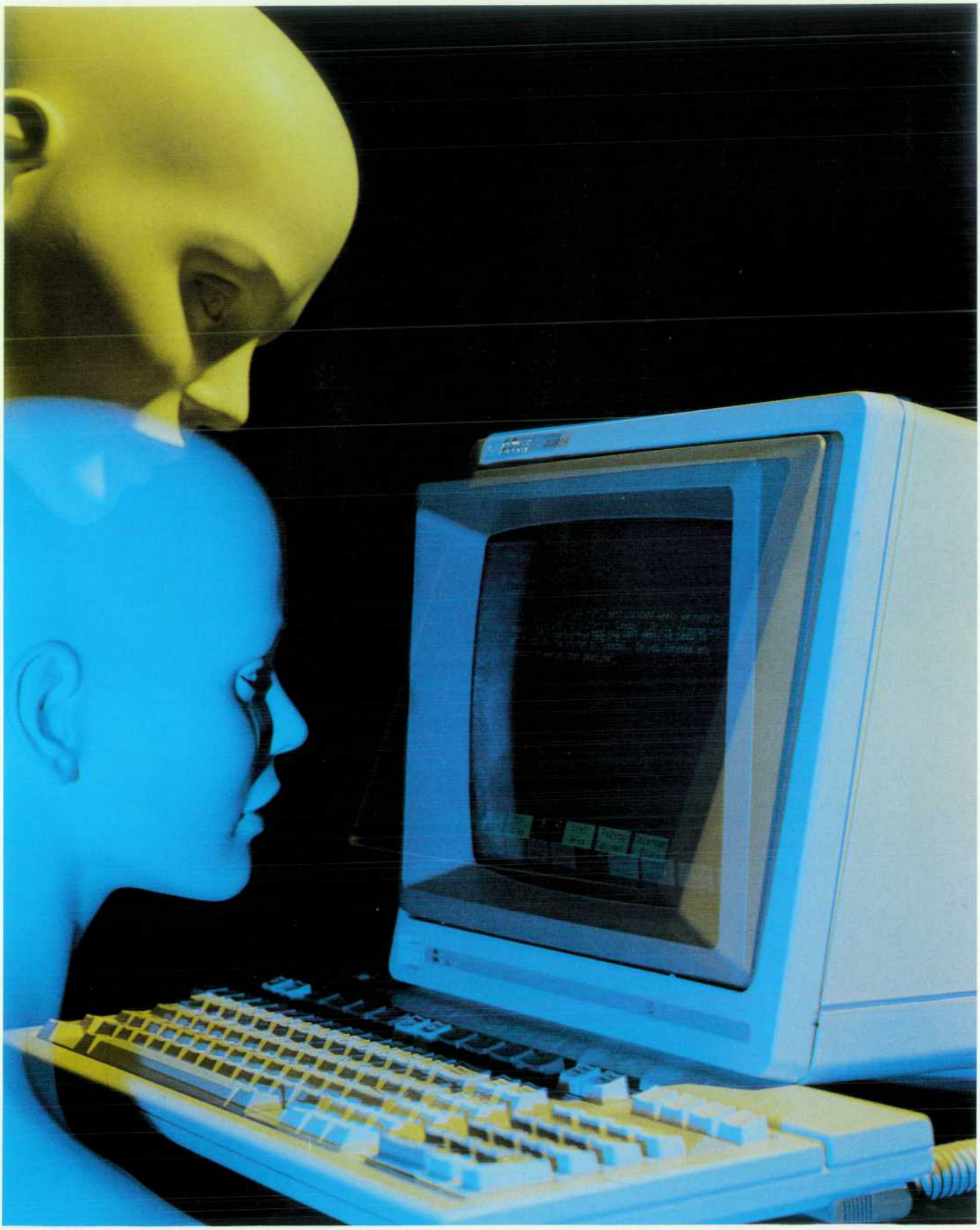

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Articles

In this Issue

The video display terminal, or VDT, is the latest addition to the typical office worker's battery of standard equipment, joining such old standbys as the in basket, the desk calendar, and the telephone. With increasing frequency, however, the "VDT" on an individual's desk is likely to be a personal computer rather than a simple terminal driven by a host computer. A PC can act like a terminal if its owner so chooses, but it can also operate as a stand-alone computer with local intelligence and mass storage capability. In the future, the PC may replace the VDT as their costs become comparable, but today there are still plenty of applications for the simple VDT, provided that it meets several important user requirements. First, it has to be low in cost, because the cost of terminals is an increasing proportion of the cost of an office-automation computer system. Second, it has to be ergonomically designed, because we've learned that people develop physical problems when they have to adapt to their work areas rather than the other way around. Third, a VDT has to be compact and quiet to fit into the office environment. Fourth, it has to be reliable, and finally, it has to work with the customer's computer system. In the articles on pages 4 to 22, the designers of the HP 2392A Display Terminal tell us how they addressed these requirements in the design and manufacture of their product. To lower costs, for example, the HP 2392A printed circuit board production facility in Grenoble is almost completely automated. Our cover illustrates the terminal's ergonomic design, which includes tilt and swivel mechanisms, a choice of display colors, and the same low-profile keyboard that's used on HP PCs and other computer equipment.

Need a multicolor overhead transparency for a presentation and fifty copies of it, also in color, to hand out to those attending? The HP 7550A Graphics Plotter is designed for this kind of job. Under the direction of a user's graphics program running on a host computer, the HP 7550A can make multiple copies of an eight-color original graph automatically. The plotter automatically loads sheets of paper and transparency material (film and vellum material have to be loaded by hand) and races through the paper plots wth 6g acceleration and up to 80-centimeter-per-second pen speed. These and other advanced features of this intelligent plotter are described by its designers in the articles on pages 25 to 36.

-R. P. Dolan

What's Ahead

The deceptively simple concept of ejecting minute ink droplets to form high-quality text by momentarily boiling the ink in the nozzle cavity is the subject of next month's issue. The development of this technology and the first HP product to use it, the ThinkJet printer, will be described.

A Low-Cost, Compact, Block-Mode Computer Terminal

The design emphasizes ergonomics and very high reliability as well as low cost and compactness.

by Jean-Louis Chapuis and Michèle Prieur

IN 1981, HEWLETT-PACKARD introduced the HP 2622A Terminal, which was the basic product of the HP 262X family. At that time, the low-cost terminals war had already started, and many of HP's competitors were offering new character- and block-mode terminals at very aggressive prices. A market study showed that more and more customers were becoming sensitive to the cost of their video display units, because they represent a significant part of the total cost of a computer system.

In response, the HP 2392A Terminal project was started at HP's Grenoble Personal Computer Division. The project had very ambitious objectives:

- Cut the manufacturing cost of the previous terminal in half
- Develop a new package design emphasizing ergonomics and compactness
- Achieve a reliability equivalent to less than a single failure every ten years.

It was realized early in the project that only the use of specialized VLSI components would drastically reduce the component costs and allow the price and reliability objectives to be met. Two VLSI chips were designed. One is a CRT controller manufactured at HP's Cupertino Integrated Circuits Operation (see article, page 9). The other is an ECL gate array developed with an outside vendor. As a result, the HP 2392A (Fig. 1) has one fourth as many chips on its logic board as its predecessor (see Fig. 2), yet offers greatly improved performance and features.

Even the power supply of this new terminal was an in-house design. This was because no commercially available power unit could match the stringent requirements for reliability, compactness, and price.

Ergonomics requirements dictated a tilt and swivel capability. The traditional method of providing the tilt feature has been an articulated pedestal that tilts the entire unit. This method adds substantial height to the terminal and increases its shipping bulk. The solution was to hinge the CRT tube and tilt the tube itself with respect to the terminal housing. The external dimension constraints imposed by HP's corporate design standardization program (width of 325 mm) and the internal space required by the tilting tube left little room for electronics. Various attempts at the layout and arrangement of the power supply and sweep printed circuit boards were made to facilitate heat dissipation and avoid a cooling fan, which is highly undesirable in the office environment.

A very close relationship with HP's U.S. divisions was required to ensure a good integration of the terminal with HP computers, software, and printers. On the other hand, close collaboration was necessary with European countries to localize the product.

Fig. 1. *HP 2392A Terminal.*

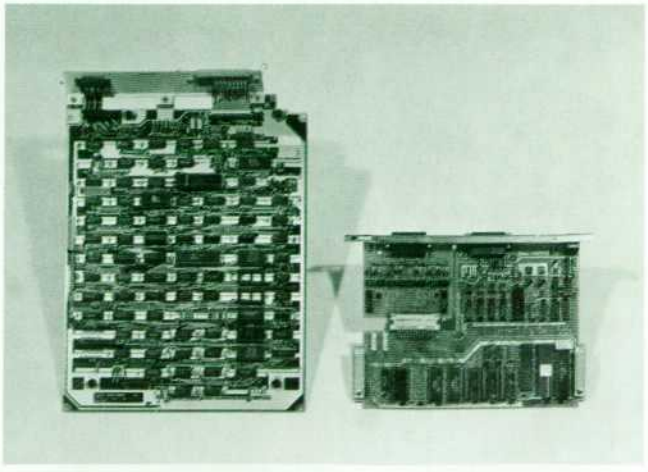

Fig. 2. *The HP 2392A's logic board (right) has only one fourth as many chips as earlier HP designs (left).*

Feature Set and Firmware Design

Compatibility with existing HP block-mode terminals was of paramount importance for the HP 2392A. Therefore, the HP 2392A firmware is a superset of the firmware of its predecessor, the HP 2622A. Additional features include smooth scrolling, a parallel or serial printer port, dynamic allocation of display memory, secret video enhancement, and datacom speeds up to 19,200 baud.

The HP 2392A can display softkey labels and error messages in ten languages and can handle 17 national keyboards. It supports the Roman8 character set standard, which includes both USASCII characters and international characters. The 256 Roman8 characters are represented by 8-bit codes.

The Parity/Data Bits field in the datacom configuration menu allows the user to specify whether character codes are sent as 7-bit codes or as 8-bit codes. If the 8-bit mode is selected, international characters are accessed directly rather than being taken from an alternate character set, which is accessed indirectly through additional control code. If the 7-bit mode is selected, the terminal uses the ISO replacement method, which is compatible with the HP 2622A's 7-bit mode.

Some functions normally performed by hardware are partially done by the HP 2392A firmware. For instance, keyboard encoding and debouncing uses a minimum of hardware (see box, page 7).

The smooth scrolling of the display is also partially handled in an NMI (nonmaskable interrupt) routine, where a smooth scroll counter is maintained. The video structure is updated according to this counter.

Video Structure

The display memory uses dynamic allocation, which means that characters to be displayed are stored in memory blocks taken from a linked list of free blocks. The video structure is composed of linked row headers, which point to data blocks that contain the row data.

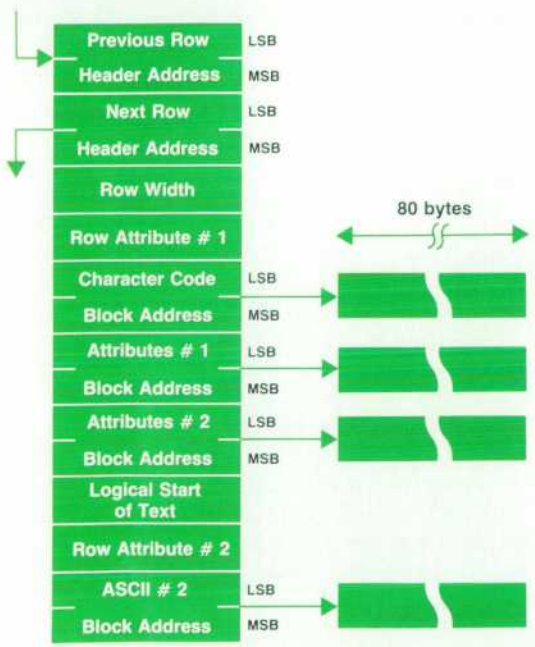

Fig. 3. *In the HP 2392A's display memory, linked row headers point to data blocks that contain the characters for each row.*

One normal row is composed of a 16-byte header and from one to four 80-byte data blocks.

When a line is empty, only a header of 16 bytes is used. Whenever one character is entered in this row, an 80-byte block is fetched from the pool of free blocks and is allocated to this header. Thus, $16+80=96$ bytes are required to display a complete row of normal characters.

If some video attributes (e.g., inverse video, blinking, etc.) or some software attributes (unprotected fields in format-mode applications) are required, then two more 80-byte blocks are fetched from the pool and linked to the row header using the attribute addresses in the header, as shown in Fig. 3. Thus, to display a row with hardware and software attributes, $16+3\times80=256$ bytes are used.

The last block address shown in Fig. 3, the ASCII #2 block address, is used when a secret video enhancement is required in the row. The logical start of text is used in the line modify and modify all modes.

The HP 2392A can display up to two pages of text even in the worst-case situation (full 80-character rows with attributes). In a typical case, the terminal can display up to four pages. If no attributes are required, it can display four pages. Additional RAM can be ordered as an option, allowing the terminal to display up to eight pages.

Because of dynamic allocation, a situation may arise where no more 16-byte headers are available from the 16-byte block pool. In such a situation, 80-byte blocks are fetched from the free 80-byte block pool and are used by the terminal firmware to create new row headers.

Block Mode

The block-mode tear-apart firmware handles transfer requests. It is divided into three main parts: request handling, handshake handling, and actual transfers. Each of these parts is independent of the others.

When a transfer is requested, a routine is called that decides the type of transfer requested. Then another routine decides the type of handshake to be used and whether the transfer is to be performed immediately or put in a waiting state. Fig. 4 shows the sequence of operations.

Configuration

The various terminal characteristics can be configured easily by displaying and modifying the configuration menus on the screen. The user can change the contents of these menus and then alter the terminal's configuration characteristics by saving them in nonvolatile CMOS memory, which is mapped in a part of the terminal memory called CMOS-Image. For security reasons, this part of the terminal RAM is duplicated in two different areas of the nonvolatile RAM.

These areas, called CMOS1 and CMOS2, are only modified by the SAVE key or by certain softkeys, whose states are also saved in this memory. The softkeys whose states are saved in the CMOS memory are: remote mode, auto linefeed, block mode, modify all, to external, and to display.

At power-on, CMOS1 is copied into CMOS-Image. It pro-

vides information on how the terminal was last configured. CMOS-Image contains the current state of the terminal. This part of RAM can be modified by escape sequence or by the SAVE key.

A CMOS scratch RAM is used to display the configuration menu. A scratch area is necessary since the user may change the menu and decide not to save it.

When it is turned on for the first time, the terminal is configured with default values.

Parser

Every character received is interpreted as a command or part of a command and triggers the appropriate action. In terms of language theory, these commands are phrases obeying the rules of a regular grammar, and therefore may be recognized by a finite state machine.

The HP 2392A's state machine consists of a control unit (CU) and a language descriptor (LD). The latter is a collection of data describing the commands accepted by the terminal. The former is a very short program, able to execute the elementary orders issued by the LD. Both are designed to take advantage of the separation of commands into families. This makes the state machine modular and easy to change. Only, the LD has to be modified or rewritten if new commands or applications are implemented.

In the LD, the elementary building block is the transition. When it receives a character, the state machine executes a move from an initial state to a final state, and triggers an action. This is a transition. Several transitions are possible for a given initial state, depending on the input character.

A state is the collection of all the transitions issued from it. These transitions must be contiguously listed in memory, but their order is irrelevant. If the first transition does not match the input character, the following transition is tried, and so on until a match is found. Thus, the last transition must collect the unexpected input characters.

A family is a collection of related states. It is represented by a list containing the addresses of these states.

An application is a collection of families. It is represented by a list containing the addresses of these families.

The CU is designed with reentrance capability to allow several applications to run simultaneously. Every application has a dedicated workspace for its variables.

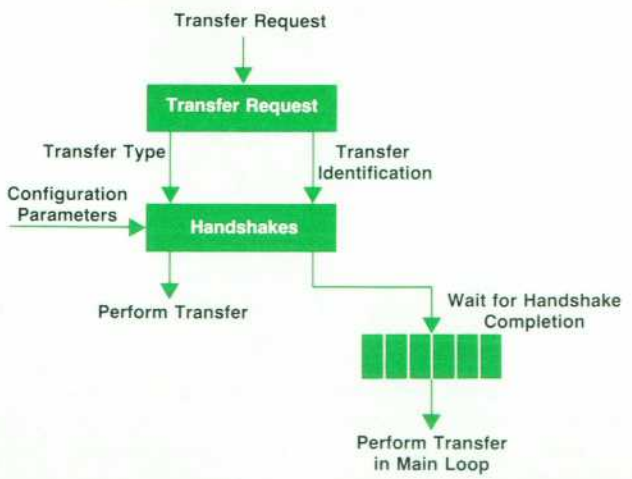

Fig. 4. *Block mode transfer handling in the HP 2392A.*

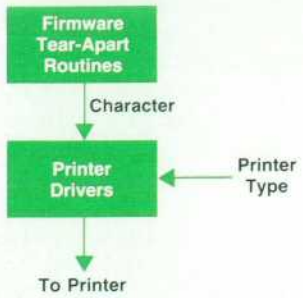

Fig. 5. *For output to an external printer, one of four printer drivers is chosen, depending on the printer type.*

External Port

The routines that handle data transfers to the external port are in fact the routines of the tear-apart firmware with small modifications. These routines get characters from the video RAM and send them to a driver, which transforms them if necessary so they can be understood by the printer connected to datacom port 2 (Fig. 5).

There are four printer drivers, one of which is chosen according to the printer type. The terminal recognizes two types of printers: HP printers (HP 267X) and others. Both kinds of printers have USASCII character sets, but international characters and alternate character sets (e.g., line drawing set) are handled differently. Both types of printers also have 7-bit and 8-bit modes.

The Other_7bits driver uses ISO replacement for the international characters and accesses the line drawing set as an alternate character set. The Other_8bits driver implements 8-bit datacom. With the 267X_7bits driver, the Roman extension and line drawing sets are considered as alternate sets. They are accessed via escape sequences and control codes. With the 267X_8bits driver, the Roman extension and line drawing sets are also considered as alternate character sets, but they are accessed via escape sequences and bit 8 is set to 1.

Test Programs

The HP 2392A has three types of built-in test programs: Power-on tests, self-tests, and manufacturing test. Power-on tests are executed at power-on. These test the ROMs and the RAMs (including the CMOS RAM). If no errors are detected, control is passed to the main program. Otherwise, the terminal gives a number of beeps corresponding to the test that failed and the program stops.

There are three self-tests: terminal test, port 1 test, and port 2 test. The terminal test tests the ROMs and RAMs and displays the test pattern on the screen. The port 1 test and the port 2 test differ only by the address of the hardware handshake lines. During these tests, serial transmission and the hardware handshake lines are tested.

The manufacturing test is performed at power-on if a special module is plugged in. This test has three different modes. The first mode is a complete test of the hardware (ROMs, RAMs, interrupt lines, port 1, and port 2). Errors are displayed on LEDs located on the special module. This program can run with a minimum hardware configuration.

A Reliable, Low-Cost Keyboard Interface

Low-cost communication between a detachable keyboard and a terminal processor board can be achieved using a simple hardware/software procedure. Traditional keyboard interface circuits rely generally on data transfer between the keyboard itself and the processor board. Either serial or parallel data transfer may be used. Serial transfer requires four lines: two for power, one for data, and one sync line. Specialized chips are often used, along with other components, to transmit the serial data stream. On the other hand, parallel data transfer requires at least eight data lines, one strobe, and two power lines.

To reduce component count and overall interface cost, the HP 2392A uses a different approach originally developed for the HP 2621B Display Terminal and later used in the HP 150 Personal Computer. The main advantage of this method is that it does not require the transmission of key number information, either coded or not. The hardware in the keyboard consists of column drivers, row scanners, and a 7-bit counter to address up to 128 key locations (see Fig. 1). On the processor board, one byte in memory is dedicated as the image of the counter in the keyboard. A five-wire, low-cost telephone cable is used for the physical connection, allowing for two power lines and three control lines: increment, reset, and key state.

The principle of operation is straightforward. It is based on the identity of the contents of the counter in the keyboard and its memory image on the processor side. The scanning routine in the processor board clears the image byte in memory and issues a reset to the interface, effectively clearing the keyboard counter. The key state line is sampled to check the status of key location 0. The scanning routine then increments the image byte in memory and issues an increment to the interface. Key location 1 is addressed, and its status is read on the key state line. This process is repeated until the last key location on the keyboard has been checked, the reset line is activated again, and the image byte is cleared. Any time a key is found in the depressed state, the scanning routine looks in the image byte to find the key location.

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Development Engineer
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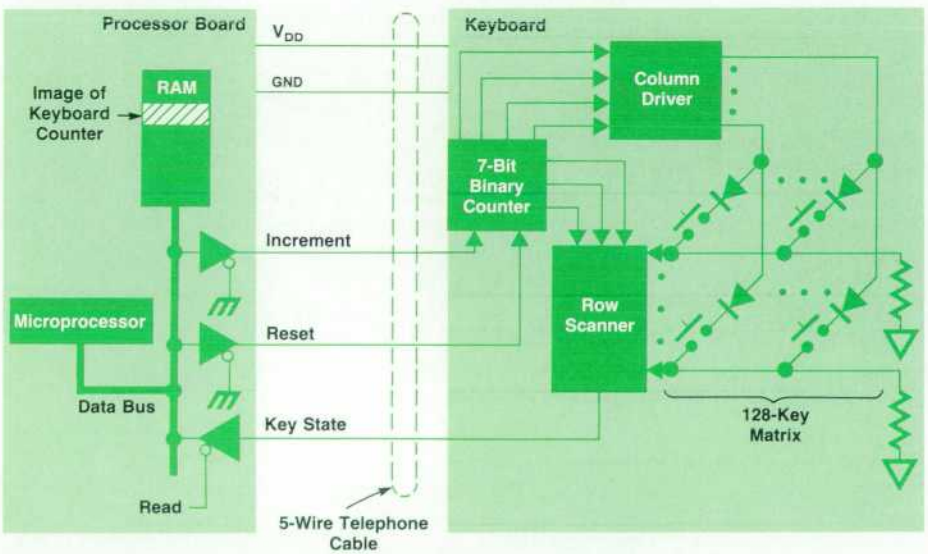


Fig. 1. *Diagram of the low-cost connection scheme between the keyboard and the processor of the HP 2392A Terminal.*

This test is performed continuously in a loop. The second mode is identical to the first, but the test is performed only once. In the third mode, the terminal only fills the screen with @ to allow the operator to adjust the screen during production.

Acknowledgments

Several persons worked on the HP 2392A firmware, Nicolas Tripon was in charge of the parser and the datacom code. Nadine Odet worked mainly on the configuration and the softkey parts. Michel Ghidossi wrote all of the test modules and Freddie Barbut was in charge of the keyboard code. We would like to thank all of the people who helped us test this software for HP 2622A compatibility on application programs, and especially Jacques Duharest.

Mechanical Design of a Low-Cost Terminal

by Michel Cauzid

THE HP 2392A TERMINAL is the first HP display product that conforms to a new HP industrial design program for computer products. This program has the objective of giving different computer products consistent shapes, dimensions, and colors. Consistent dimensions allow products to be used side by side or on top of one another. A new range of colors, paler than those used previously, has been introduced, in tune with a trend towards lighter colors for office equipment and furniture.

The program also emphasizes consistent implementation of good human factors features for display products..This includes such things as integral display tilt and swivel mechanisms, detached low-profile keyboard, and terminal controls on the front panel.

External Design

Two new colors are used for the HP 2392A Terminal. French gray is used for the bezel, and parchment white is used for all the other parts. A new smoother texture is employed for all external areas. Attention has been paid to the choice of these colors and texture to minimize the reflection of light on the monitor housing.

The main purpose of screen tilt and swivel is to provide an optimum viewing angle for operators of different size, allowing them to achieve the most comfortable posture. The operator can tilt the terminal to reduce glare from ambient lighting. The contribution of the HP 2392A in this area is the integration of the tilt movement in the enclosure. Internal tilt allows simple vertical adjustment of the CRT without having to move the entire enclosure. The nominal tilt range is 0 degrees vertical to 20 degrees back. The swivel in the base allows 360 degrees of rotation.

All user controls are located on the front, below the CRT. The power button is located on the lower left portion of the display bezel. Brightness control is located under the lower right portion of the display bezel.

The HP 2392A is designed for minimum size and maximum configurational flexibility. It is a member of the 325-mm stack family of products defined by the new industrial design programs. In this family, all peripherals, such as printers, are external to the terminal enclosure. The overall width of the terminal is 325 mm. Since the 12-in CRT's width is 275 mm, only 25 mm is available on each side for the tilt mechanism.

Internal Design

An internal metallic chassis holds the logic, power supply, and sweep boards, as well as the screen tilt mechanism. This sheet-metal part forms a rigid frame for the terminal. All the architecture is based around the sheet-metal frame. This permitted more flexibility during the tooling phase.

The CRT is fastened to the moving bezel with two metallic brackets. This assembly tilts around two holes in the metallic chassis. It is balanced by a spring and braked by friction. Fig. 1 is a drawing of the terminal, showing the tilt mechanism.

Three other plastic parts make an aesthetic enclosure: the cover, the front bezel, and the plastic chassis. Under the plastic chassis, a pedestal with rubber feet provides the swivel function.

The plastic molding compound used for the packaging is an ABS from Borg Warner Company (Cycolac KJUV). For friction compatibility between the pedestal and chassis, the pedestal is molded with Makrolon, a polycarbonate

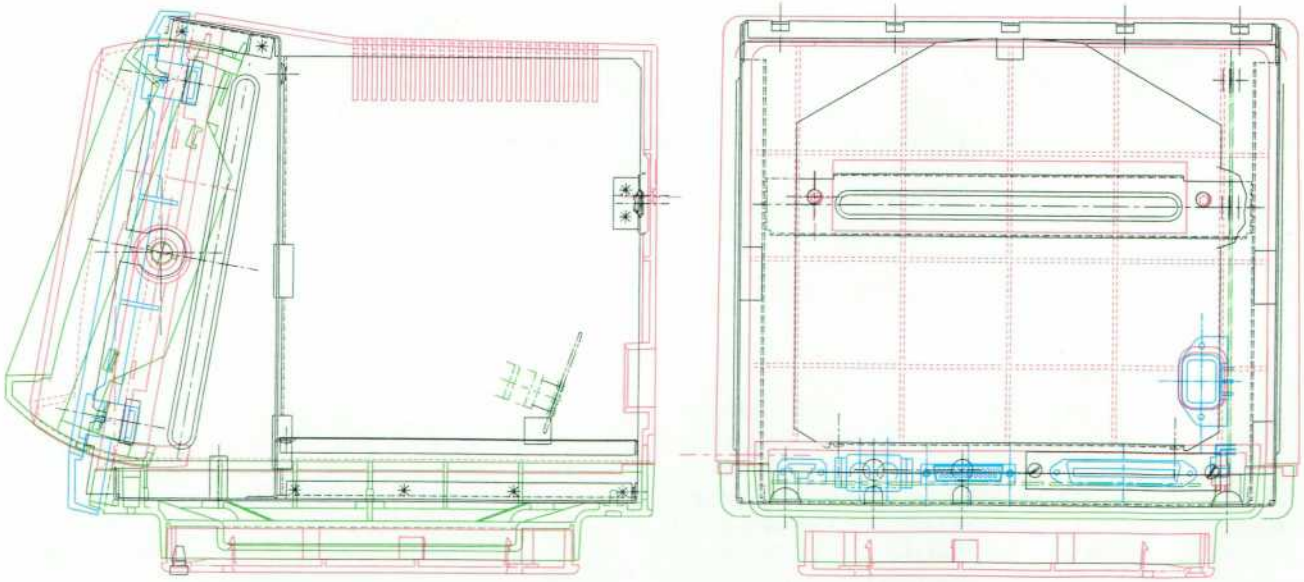


Fig. 1. *An HP Draft drawing of the HP 2392A CRT tilt mechanism.*

from Bayer.

Internal connections are minimized. The only connections using wires are between the CRT and the boards. All the other connections are directly on the boards.

Five Design Phases

The mechanical design team was relatively small. During the five design phases, this team had to design the parts, draw the schematics, choose the subcontractors, assist in the tooling setup, and perform the tests. These tasks were made easier by the use of HP Draft (see below).

During the conceptual phase, the team was responsible for conceiving and defining the physical parts used in the product. The objectives were to reduce stock levels, minimize inventory problems, reduce the assembly time, and use standard circuit sizes. For the materials choice, we looked for competitively priced materials with high-quality characteristics. We designed all parts as tooled parts and we subcontracted the production of all parts.

The next phase was the documentation phase. The basic three-view mechanical drawing is the primary document that directs people in producing each part. Each member of the team designed parts and created drawings using HP Draft. The simulation capabilities of HP Draft guaranteed that the parts would fit together properly.

The next phase was the modeling phase. Usually a designer first makes mechanical drawings of a new part, and then to verify the design, sends the drawings to a model shop to have one or two parts made. For the HP 2392A, we were able to go directly from the first drawings to molds. We subcontracted to an external model shop the manufacture of soft molds. With these tools we obtained 100 parts using a new process based on low-pressure injection. Once painted, these parts look very similar to traditional injection-molded parts.

The fourth mechanical design phase was the tooling phase. The HP 2392A has five major tooled pastic parts, five major tooled sheet-metal parts, and ten miscellaneous tooled metal or plastic parts. The production of these parts is subcontracted. The ideal subcontractor from our point of view is the one who can combine efficient production with enough flexibility to be on our design team. This means reacting quickly in case of modifications to avoid wasting valuable time. To meet our schedule, we finalized the plastic parts first, since modifying sheet metal is easier than modifying molds. All the molds are designed so that the parts can be injected in polycarbonate or in ABS.

In the test phase, our major problem was the behavior of the moving CRT during the shock and vibration tests, and the efficiency of the package with this tilt mechanism. In addition to the standard environmental tests we tested the tilt mechanism extensively to verify the choice of the friction material.

HP Draft

HP Draft is a software program that runs on HP 9000 Model 520 and HP 9845B Computers. It facilitates the production of two-dimensional mechanical drawings by working interactively with the designer, who has great flexibility in specifying positions, points, intersections, objects, and so on. Fig. 1 of this article is an example of an HP Draft drawing.

The HP 2392A project was started using an HP 9845B Desktop Computer and an HP 7580A Plotter. At the end, the equipment included three HP 9845Bs, an HP 7580A, and an HP 7585A Plotter.

It is very difficult to estimate the amount of time saved by using HP Draft, but it is undoubtedly true that both the quality and the speed of obtaining final drawings were considerably increased. HP Draft permitted a simulation of the assembly of all parts, and hence saved time and enhanced quality.

HP Draft was especially useful in dealing with our subcontractors. We quickly supplied them with accurate and reliable drawings when design changes occurred.

Acknowledgments

The mechanical design team included Claude Carpentier, industrial designer Jacques Firdmann, Jean-Claude Serres, and Hugues de Charentenay.

VLSI Design in the HP 2392A Terminal

by Jean-Jacques Simon

WHEN HP'S GRENOBLE Personal Computer Division received the charter to design the first of a new generation of display terminals, the objective was to design a terminal that was more powerful, more reliable, and smaller than the previous generation of equivalent products, and that cost half as much.

An analysis showed that the only way to achieve this was to integrate the CRT display controller function. Commercially available controllers did not provide all the functions required by the terminal, and the use of standard MSI chips would consume a large portion of the available board space. A comparison with existing terminals, like the HP 2622A, showed that about 30 MSI or SSI packages could be replaced by a single custom IC. By doing so, the cost of the CRT control function could be reduced by more than 80%.

One of the main objectives was low price. We had to select an integrated circuit process that would yield low-cost parts and that was readily available, well supported, and relatively easy to design with. Among the HP processes available at that time, NMOS-C, manufactured at two locations in the U.S.A., was chosen.

CRT Controller Functions

The HP 2392A's CRT controller (CRTC) is in charge of all the display support functions. Its internal RAM, sequencer PLAs,* and character ROM allow it to fetch ASCII codes from the processor's RAM, store them locally for the duration of a character row on the screen, and convert them to the dot pattern representing the character shape. All these functions are performed with minimum help from the processor, since the CRTC works in a DMA (direct memory access) mode. The CRTC also provides the synchronization signals required to operate the CRT.

The logic board of the HP 2392A can be described with the block diagram in Fig. 1. It is essentially an 8088 microprocessor with ROM and RAM space, a UART,* clock generation logic, and the CRTC. The 8088 and the CRTC share the same RAM space. When characters are entered though the keyboard or received from the datacom port, the microprocessor stores them in the display RAM area. On every vertical retrace time, an NMI (nonmaskable interrupt) is issued to the processor, which executes a routine that writes frame information into the CRTC's register stack.

One of the CRTC registers is the top header address (THA) register. In this register, the microprocessor writes the address of the first block of pointers in the linked list of pointers for the characters to be displayed in the current frame (see Fig. 2). The master sequencer in the CRTC is programmed to use the THA as the first address for a DMA sequence during which it fetches the contents of the top header pointer block. The pointer block, or row header, as described in Fig. 3, contains enough information to find the data and attributes blocks for the current row of characters, as well as the address of the next pointer block, which is used during the following DMA cycle. The row width register in the pointer block indicates the number of displayed characters in the row to be fetched. The DMA cycle is adjusted for that number of characters, reducing bus use by the CRTC. Valid row width values are between 0 and 79 for numbers of characters between 1 and 80. If the row width code is set to 99, the current row on the display is empty, and there is no DMA at all (the row buffer in the chip is filled with space characters).

The row attributes register contains information associated with each row of characters on the display (see Fig. 3). If bit 4 is not set, there will be no DMA cycle for attributes. If bit 3 is set, this row is part of the memory lock area on the screen. Bits 0, 1, and 2 determine the width and height of the characters in the current row. For double-height characters, two pointer blocks contain the same

*PLA = Programmable Logic Array.
UART = Universal Asynchronous Receiver/Transmitter.

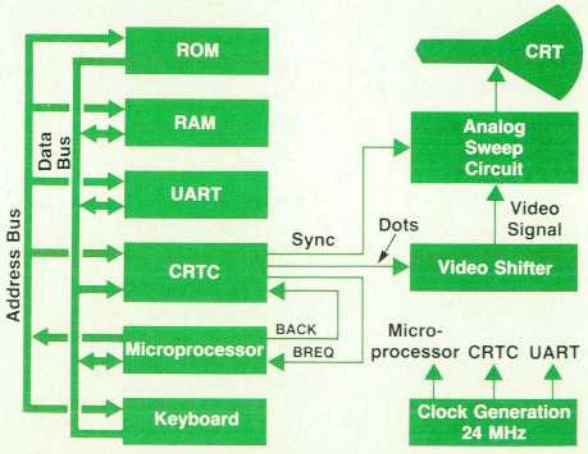


Fig. 1. *Logic block diagram of the HP 2392A Terminal.*

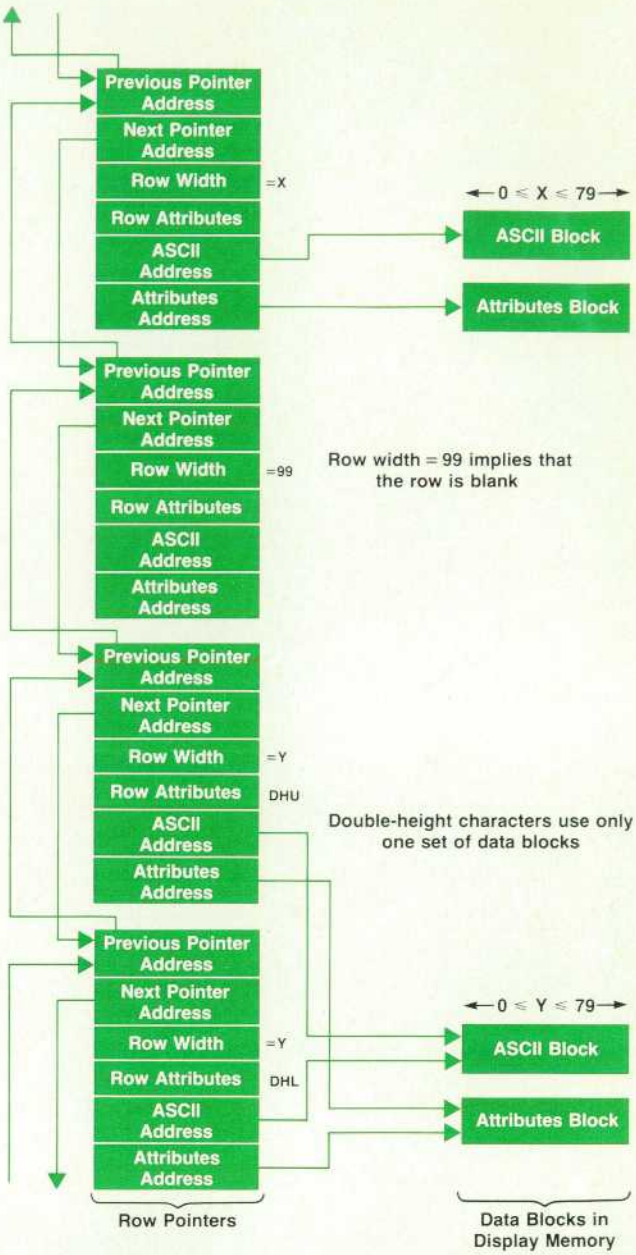


Fig. 2. *Characters to be displayed are specified by a linked list of pointers.*

Byte Number	Row Header Information
0	Previous Row Header Low Byte
1	Previous Row Header High Byte
2	Next Row Header Low Byte
3	Next Row Header High Byte
4	Row Width
5	Row Attributes **
6	Character Address Low Byte
7	Character Address High Byte
8	Attribute Address Low Byte
9	Attribute Address High Byte

**Row Attribute Bit Definition:
b7=b6=b5=not used by CRTC
b4=ATTP (attribute block present)
b3=NSS (not scrolling=lock row)
b2=DHU (double height upper part)
b1=DHL (double height lower part)
b0=DW (double width row)

Fig. 3. *Pointer block structure. The row attributes register contains information associated with each row on the display.*

ASCII address (and attributes address, if needed). The first has bit 2 (DHU) set in the row attributes register to indicate the double-height upper part, and the second has bit 1 (DHL) set to indicate the double-height lower part. The ROM line generator uses this information to access the same information twice, in consecutive scan lines, so that the character is displayed two times taller than normal. For double width, bit 0 (DW) is set in the row attributes register, telling the master sequencer to read each character in the ASCII and attributes blocks twice. The character codes in the internal row buffer are then effectively doubled. The attributes logic on the chip can then double each dot in a scan line to make the character appear wider than normal. To do so, it uses the column number information, indicating the parity of the current character location on the screen, along with the DW bit.

The master sequencer in the CRTC is programmed to execute the DMA cycles, using the addresses found in each consecutive pointer block of the linked list of pointers. The DMA cycles are initiated at fixed time intervals by the CRTC, which asserts its BREQ (bus request) output. The microprocessor answers the handshake with its BACK (bus acknowledge) line, as soon as it completes execution of the current instruction. The use of DMA techniques for data transfer between RAM and the CRTC minimizes the amount of processor time needed to support the display. In the worst case, no more than 15% of the data and address bus bandwidth is used by the CRTC. The rest is available to the microprocessor.

CRTC Architecture

The CRTC is built around four internal buses, through which all the data and timing information is exchanged. Fig. 4 is the CRTC block diagram. The internal data bus and the address bus communicate with the external microprocessor data and address lines. The column number bus (CN bus) and the four-phase clock are exclusively internal. The sequence of operations and the flow of data in the chip are controlled by a master sequencer PLA using 18 inputs, 28 outputs, and 132 minterms. The master sequencer reads the contents of the register stack and the outputs of the column counter and uses them with its present state to determine its next sequence.

The register stack contains 16 registers, each 8 bits wide, an 8-bit incrementer, and a PLA to decode the instructions from the master sequencer. The register stack can input data from the internal data bus and output data to it. The outputs of the incrementer can be directed onto the internal address bus during a DMA operation. The instruction set of the stack includes simple operations between registers, such as increment, transfer, input, output, and NOP.

The column counter is a free-running toggle counter that outputs the value of the current character number across the screen, from 0 to 79. It counts through 109 to account for horizontal retrace.

The row buffer is a three-transistor dynamic RAM array of 2080 bits, organized as two banks of 80 13-bit words. Two DMA cycles are necessary to load one bank of the row buffer, one for ASCII data (8 bits) and one for attributes (5 bits). The words in the row buffer are addressed using the CN bus. As a result, read and write operations on this RAM are done synchronously with the display of the characters on the terminal screen. While the contents of one row buffer bank are read out to display on the screen, the second bank is written to, so that it is ready to be used for display after the current row of characters. At that time, the role of the two buffer banks is reversed.

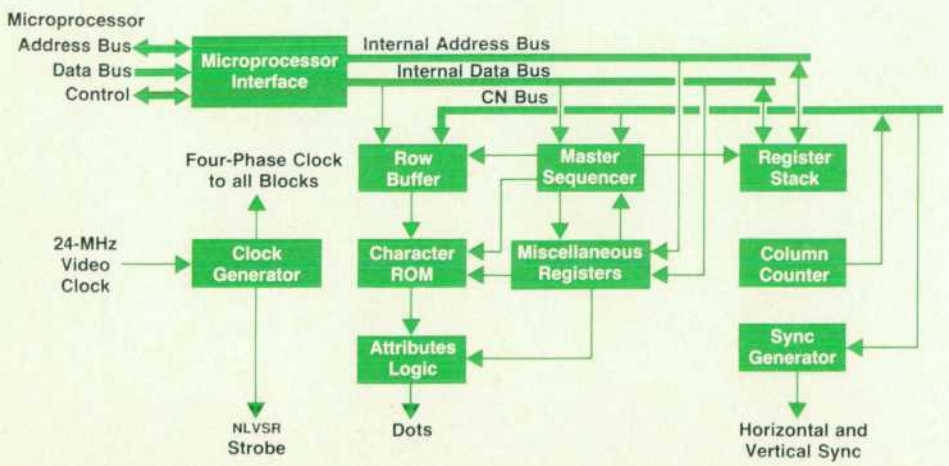


Fig. 4. *Block diagram of the VLSI CRT controller chip used in the HP 2392A Terminal.*

The character ROM is programmed with the dot patterns used to draw the characters on the screen, using a matrix 9 dots wide and 14 dots tall. The display process requires that the successive dot patterns forming one scan line be fetched and assembled into one continuous stream of dots, to be shifted at the video frequency (24 MHz). To display one scan line, the ROM addresses are formed by combining the scan line number from the register stack and the ASCII codes for the characters at each consecutive column number location. The ASCII codes come from the row buffer, addressed by the column counter output value. The information in one row buffer bank is used fourteen times, once for each scan line. Each time, a new scan line number is read from the register stack by the master sequencer. The master sequencer orders the stack to increment the scan line register during the horizontal retrace time.

The character ROM contains 256 character patterns. Each character is described as 14 groups of 8 bits for a total of 28,672 bits. The ROM cell and decoder designs were leveraged from an earlier HP 64K-bit ROM design.

The attributes logic block modifies the ROM output patterns according to the attribute bits for each character stored in the row buffer. Four attributes are processed by this block: inverse video, blinking, underline, and half bright. The cursor visible on the terminal screen is also added into the dot stream in this block, according to XY coordinates stored in one of the miscellaneous registers (part of the frame information written by the microprocessor during vertical retrace time).

Finally, the dot patterns corresponding to the characters to be displayed on the screen are output on the CRTC dot outputs as 9-bit words. A strobe signal (NLVSR) is provided by the clock generation block; this acts as the load enable for a fast gate array chip in which the dot shifting at the video frequency (24 MHz) takes place (see box, next page).

All of the CRTC blocks run synchronously on a four-phase nonoverlapped clock that has a period of 375 ns, equal to a character time, or 9 dots. This results in most of the chip running at 2.67 MHz. The register stack works at a 5.33-MHz rate, executing two operations within one basic four-phase cycle. The clock generation block inputs the 24-MHz video clock and derives the four-phase clocks and the NLVSR strobe signal from it. Although it would not be practical to make a whole chip work at such frequencies in the NMOS-C process, the performance of the process is sufficient for the small portion of logic necessary to achieve the correct phase relation between the 24-MHz main clock and the NLVSR strobe signal.

CRTC Layout

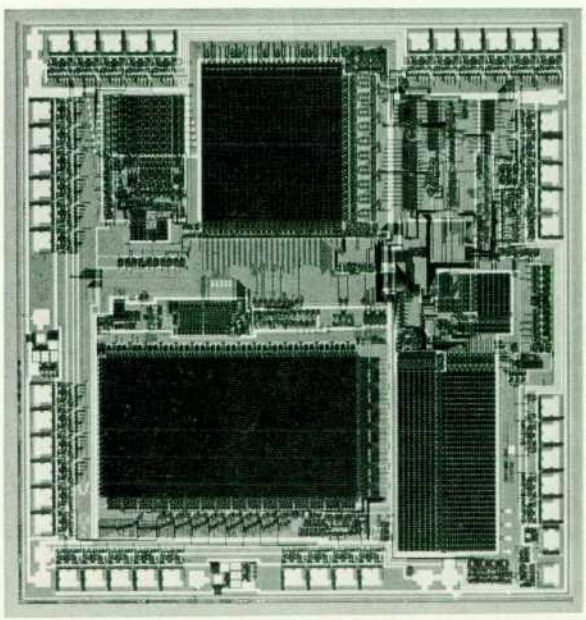
Fig. 5 shows the CRTC chip layout. The main blocks, such as ROM, RAM, PLAs, registers, and miscellaneous logic, are easily identified. One of the main advantages of VLSI is demonstrated here. The small ROM line generator block, which computes the effective scan line number used to address the ROM, would require a very large number of gates and a lot of board space if it were implemented in standard TTL logic. Designed as part of the chip using an array of pass transistors arranged in a barrel shifter, the whole function uses only about 1% of the total chip area. Operation of the ROM line generator is described in the box on page 15.

The total number of transistors on the CRTC chip is approximately 55,000. There are approximately 28,000 in ROM, 6000 in RAM, 12,000 in the PLAs, 2000 in the register stack, and 7000 in miscellaneous logic.

Design Tools

Being the first HP division to begin IC design outside the U.S.A., the Grenoble team had to face some unusual situations. Most of them were associated with limitations in the tools, which U.S. designers generally solved by going to a bigger, more powerful computer. Others required information exchange, and we could not fly to the U.S. every

(continued on page 14)



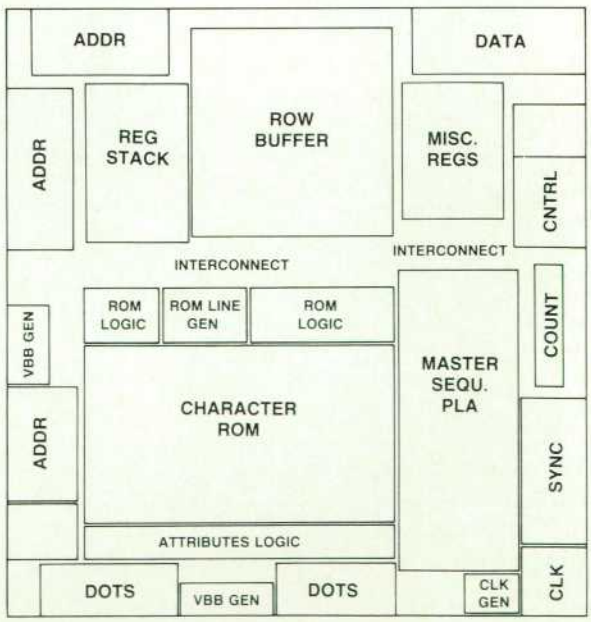


Fig. 5. *CRT controller chip and layout.*

A Fast Gate Array Companion for a CRT Controller

Because of the speed limitations of the NMOS technology used for the HP 2392A Terminal's CRT controller chip, the CRTC outputs, in parallel, the 9-dot pattern and the half bright attribute for the current scan line of the characters to be displayed. A separate gate array chip shifts these parallel dot patterns to a serial flow of bright and dark dots for the video amplifier input, and provides the gain control input of the video amplifier with the half bright attribute correctly synchronized to the first dot of each character, as shown in Fig. 1.

Standard HP character generators use half shifting capability to improve the character definition (one character line of dots may be shifted one half dot downstream), as shown in Fig. 2. In classical designs, this feature at certain times calls for twice the normal dot frequency, as shown in Fig. 3a. This effect can lead to marginal designs when standard Schottky TTL circuits are used. This need for high-frequency capability was avoided in the HP 2392A by using a slightly different shifting model where the unused 9th dot in half-shifted lines is dropped, which does not affect the visible result on the screen, as shown in Fig. 3b. The cost was a few additional gates. However, saving a few gates is not so important within a large gate array as it would be in a classical design using discrete ICs.

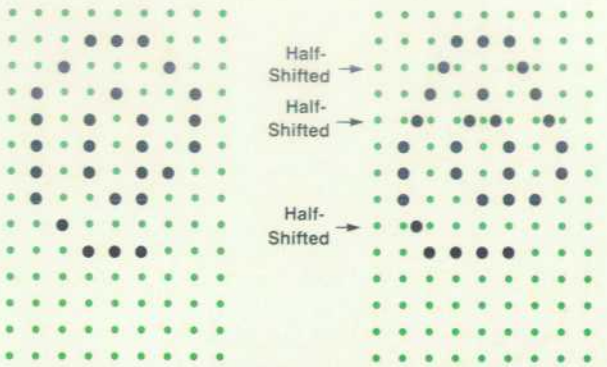


Fig. 2. *Half shifting is used to improve character definition. (left) @ character without half shift. (right) @ character with half shift.*

Gate Array Benefits

Cost reduction is one benefit of this gate array design, because the number of parts is reduced. An improvement in the reliability is also expected, both from the reduction in the number of parts and from the improvement of the design margins as explained above.

The high-frequency signals within the gate array are the main contributors to the EMI generated by the system. Their concentration within a single IC has a very positive impact on the EMI behavior of the terminal.

This video stage uses 40% of the available circuits within the chosen gate array (MCA500ALS from Motorola). The remaining circuits (Fig. 4) are used to reduce the logic board random logic (clock generation, UART interfacing, bell tone generator), thus providing additional board cost reduction, improvement of reliability, and improvement of the terminal's EMI performance.

This complete set of functions uses 100% of the available circuits. The complexity is equivalent to 18 to 20 SSI/MSI TTL circuits.

Design Stages

The MCA500ALS is a macrocell array, rather than a standard gate array. The internal part of the logic is divided into 24 blocks of elementary components (transistors, resistors, etc.).

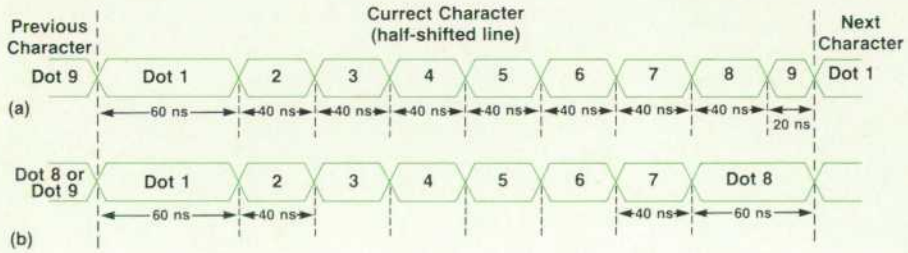


Fig. 3. *Classical half shifting model (a) calls for twice the normal dot frequency (note 20-ns dot). HP 2392A shifting model (b) does not place this demand on the CRT drive circuits.*

During the first design step, a first level of interconnection from a library assigns each of these blocks to a defined and characterized logic function. For instance, one block may be converted to two D flip-flops, or to four 2:1 multiplexers.

This very rapid step to macro logic functions permits very precise preliminary investigations. Using 100% of the available

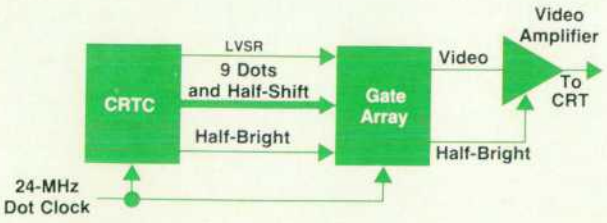


Fig. 1. *The gate array chip interfaces the CRT controller chip to the video amplifier.*

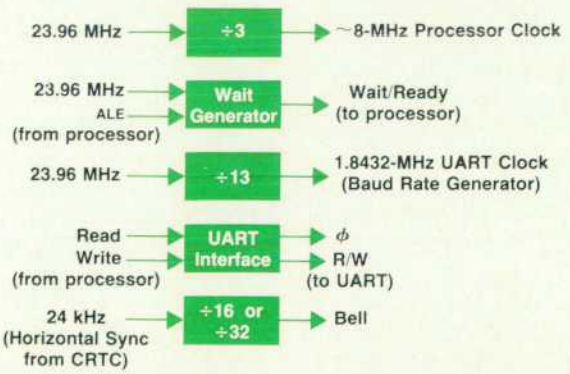


Fig. 4. *Besides the video serial register stage (Fig. 1), the gate array chip also provides the circuits shown here.*

hardware can be anticipated without any risk. Accurate prediction of the dynamic performance is achievable from the characterization of the logic functions in the library.

In the second design step, the interconnections between these logic blocks are defined. At this step, the simulation capabilities of the development tools permit verification of the combinatorial logic of the circuit, estimation of the dynamic performance, taking into account the true load of each circuit, and evaluation of the metal length.

At the third design step, the physical positions of the 24 logic blocks and their physical interconnections are defined. Automatic placing and routing are available, but in our case it failed because 100% of the available circuits are used, so a very dense interconnection is necessary.

Placing was completely done by hand. Then autorouting drew all of the interconnections except one, at once. The last wire was placed by hand.

When hand placing is used, automatic verification of some design rules is necessary. Detailed verification (static, functional, or dynamic) is also available, and the results correlated well with measurements performed 12 weeks later on the first samples of the circuit.

This design took eight engineer-days, after four days of training.

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time we had a question to answer.

From the beginning, we had decided to rely on supported HP tools, both hardware and software. We used most of the tools available for schematic entry, simulation, artwork layout, extraction, and design rules checking.

When we started our design in early 1982, the only artwork layout systems available within HP were IGS on the HP 3000,[1] and Piglet on the HP 9845C.[2] We started our layout with both systems, allocating Piglet to cell and block design and the IGS station to layout and full-chip editing.

We used Draw[3] and Spice[3] on the HP 3000 to create schematics and perform electrical simulations of basic cells and blocks. At Grenoble, we do not have a link to a mainframe computer, so we relied totally on the HP tools. For example, Spice on the HP 3000 cannot deal with more than 30 to 40 transistors at a time. Therefore, only simple cells can be checked in one simulation pass. To overcome this limitation and be able to simulate the behavior of more complex signal paths, we wrote a program to create a piecewise-linear description of a Spice output. To check a signal path of, say, 80 transistors, our procedure was to split the schematic into three smaller schematics of 25 to 30 devices each, in such a way that each smaller block was driving a load equivalent to that in the original circuit. The first block was then simulated with Spice, a piecewise-linear approximation of the output was created and used as an input for simulation of the second block, and so on.

The design rules check of the full chip was also a problem. We learned very early in the development that the HP 3000 could not check a large design in one pass, so we performed design rules checks on overlapping windows, each covering a quarter of the chip.

Logic simulation and test vector generation were done with the Testaid program on the HP 1000.[3] Again, special programs were written to pass information between the data base on the HP 3000 and the HP 1000 system, simplifying the interface to Testaid and creating readable output listings on which the behavior of the circuit could be checked.

We were able to overcome the physical distances and the delays by resorting to yet another set of HP tools. We did not want to waste one to two weeks for mail delivery when sending the artwork archive tapes to Cupertino for manufacturing. Instead, we decided to use the data transfer capability of HP's worldwide Comsys system. We just had to store our archive data on a tape on our HP 3000 and give it to our Comsys operator in the next room. Two hours later, the data was available in the Comsys computer in Cupertino. The whole operation lasted less than half a day, and no tape ever traveled from Grenoble to Cupertino. In late 1982, when HP DeskManager (formerly HP Mail[4]) became widely available, we used it extensively to exchange not only information, but also programs and process data.

Evolution and Current Development

The NMOS-C process has evolved since we began designing the CRTC chip. In early 1984, a new, shrunk version of the process was made available to the designers. It brought the minimum channel length from 3 to 2.4 μm, using a linear 20% shrink on all dimensions. Designs to be fabricated in the new NMOS-CS process can be laid out using standard NMOS-C rules, and the 20% shrink is applied when manufacturing the masks. Of course, new process parameters are used for Spice simulations and circuit extraction, so that normal layouts are simulated as if they were shrunk, to check the behavior of the final circuit. The shrunk version of the process lets the same layout run approximately twice as fast as in the standard process, and the chip area is reduced by about 40%.

We plan to take advantage of this process evolution to design the successors of the CRTC chip. We are currently integrating on the CRTC all the functions that now reside in the fast gate array chip, such as the video shifter, the microprocessor clock and wait-state generation, and UART clock generation. The new NMOS-CS process allows us to design the 24-MHz shifters that could not be done safely in the standard version.

Acknowledgments

When the HP 2392A project began, the NMOS-C process had just been released, and we got the assurance of very good support from HP's Cupertino Integrated Circuits Operation. No one at HP in Grenoble had designed ICs at that time. I took the HP VLSI class while on assignment in the U.S.A. Then we hired John Connolly, an experienced HP IC designer. John became our class instructor for the first session of the VLSI class taught outside the U.S. in an HP division, and helped us gain the knowledge of IC design necessary to start our project. The design team included John Connolly, Richard Brabant, Khambao Panyasak, and

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How to Scroll Smoothly

In a classical video display terminal, the rows of characters jump up or down when the roll up or roll down key is pressed. This can cause eyestrain and fatigue for the operators. The HP 2392A moves the rows up and down in a smooth linear motion. The displacement is not really linear, but actually consists of small jumps of two scan lines at a time on every frame time (16 milliseconds), as shown in Fig. 1.

Fig. 2 is a block diagram of the circuits involved in smooth scrolling.

The master sequencer in the HP 2392A's CRT controller (CRTC) manages all video timing by updating the contents of the registers in the register stack (scan line number, row number, and frame number). The video display timing description is an absolute reference, as opposed to the description of the screen as viewed by the user, which is relative. When smooth scrolling is enabled, the relative and absolute values are not identical.

The ROM line generator translates the absolute value of the scan line number into the relative matrix line number of the characters to be displayed. The matrix line number, called the ROM line, forms a four-bit part of the ROM address.

The optional ANSI version of the HP 2392A implements the double-height feature. Two bits in the row attributes part of the pointer blocks are used to designate double-height upper (DHU) and double-height lower (DHL). Because of this, the algorithm used to compute the relative line number has two forms.

Normal height. The ROM line address is the octal representation of the decimal sum of the absolute scan line number (SLN), and the smooth scrolling value (SS), modulo 14.

DH false: RL = (SLN + SS) mod 14

Double height. The ROM line address is the octal representation of the following (next page):

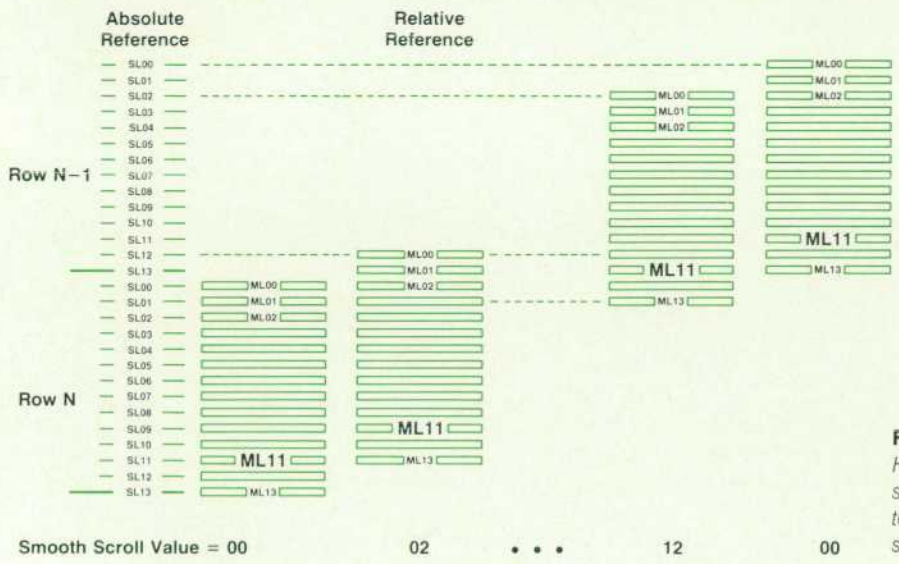

Fig. 1. *Smooth scrolling moves the HP 2392A display up or down two scan lines at a time, so the characters appear to move smoothly instead of jumping from row to row.*

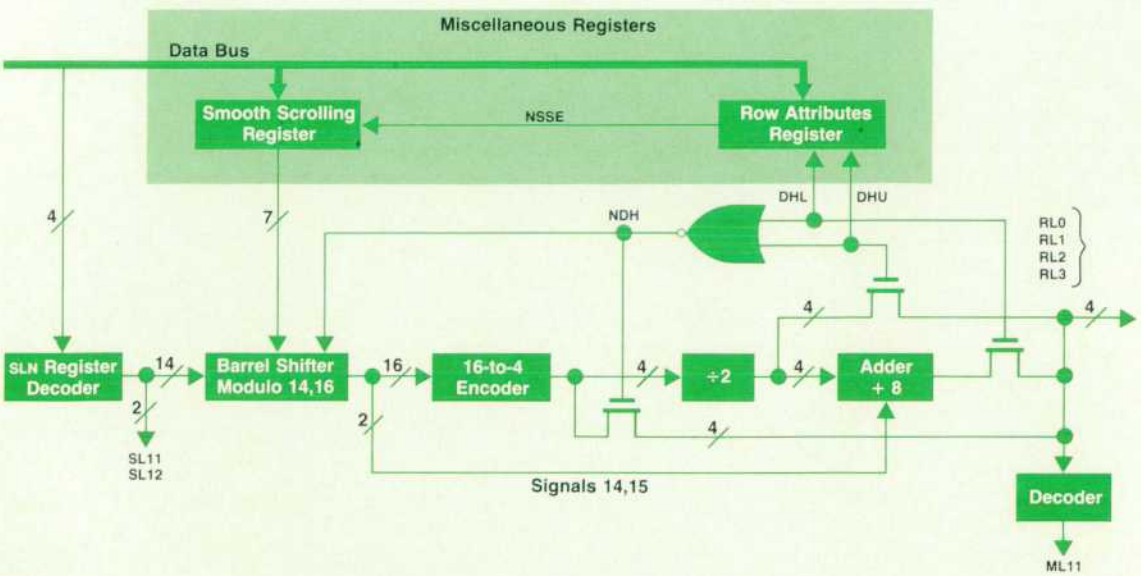

Fig. 2. *Smooth scrolling hardware diagram.*

DH true: if DHU, RL = INTEGER[(SLN+SS) mod 16 / 2]

if DHL and (SLN+SS)=14 or 15, then
RL = INTEGER[(SLN+SS) mod 16 / 2]

if DHL and [SLN+SS] ≠ 14 or 15, then
RL = INTEGER[(SLN+SS) mod 16 / 2] + 8.

This results in the same ROM line being generated twice, so that each line of the character matrix appears twice, and the character is two times as large on the screen.

The ROM line generator also generates some signals used in the attributes logic. Matrix line 11 (ML11) is the relative line number in the character matrix that is turned on when the underline attribute bit is present. SL11 and SL12 are the addresses of the scan lines on which the cursor can be displayed.

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Development Engineer
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myself for the design, and Guy Pascal for the mask layout. The design started in February 1982, and first prototypes came out in April 1983. Fully functional parts were available in November 1983, and ship release for the CRTC chip occurred in May 1984.

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Fully Automated Production of Display Terminal Printed Circuit Assemblies

by Christian-Marcel Dulphy

THE HP 2392A TERMINAL is designed for fully automated production of the three printed circuit assemblies that contain its analog and digital electronics. At HP's Grenoble Personal Computer Division, one of two production sites, production of these assemblies is entirely automated. The expected benefits of this high degree of automation include:

- Increased quality: error rate between 4 and 10 times better than manual assembly
- Tedious tasks done by machines
- Increased productivity: between 3 and 30 times faster than manual assembly
- Space savings
- Work-in-process savings.

To make fully automated production possible, guidelines for automatic insertion of DIP (dual in-line package), axial, and oddly shaped components were written and given with comments to printed circuit board designers at the very beginning of the product design, and checked and improved at each step, from prototypes to pilot run. The design effort concentrated on standardization of components (including board size), minimization of component count, standardization of component hole sizes and distances between components, and orientation and insertability considerations. Every step of the process was examined, including wave soldering.

Components and vendors were chosen by the materials engineering group, taking into account insertability and solderability. The odd components especially had to have accurate mechanical design to be handled by robots, either directly or through light conformation (mechanical adjustment of lead positions relative to the part's body). Components also had to have appropriate packing (plastic sticks).

The result of this design effort is that we are now able to insert all of the logic board components automatically, except for one, which is still hand-loaded (but will eventually be inserted by the robot). This includes battery contacts, the crystal clock, multipin connectors, potentiometers, and DIP sockets.

For the two other boards (power supply and sweep), we are able to insert 103 components by axial inserter and 41 by robot. The 26 components left are insertable by robot, but will need a different dispatching approach.

The automated assembly line uses a type II passthrough system from Universal—boards are automatically fed in and out without handling. The machines are:

- A multimode DIP inserter (0.3 and 0.6-in DIP widths) from Universal
- A variable-center-distance (VCD) axial inserter from Universal
- A six-axis robot from SCEMI.

The boards are transferred from machine to machine by

cassette and loop conveyors to avoid manual handling. The wave soldering and washing equipment from Treiber uses the same cassettes, and boards are automatically fed through it.

Odd Component Insertion by Robot

Components are delivered in tubes by our vendors. The tubes are loaded on mechanical handlers adapted to each component family. The robot, Fig. 1, picks the parts and inserts them with the same hand. A mechanical clinch (50 mm wide maximum) performs the necessary bending of a few leads under the printed circuit board. Both the clinch mechanism and the point of insertion are fixed. The tooling plate with the board on it moves for each insertion cycle. The robot is driven by an HP 1000 A600 Computer, which allows us to drive two robots or one robot plus vision at an insertion rate of 6.5 seconds per component. The automatic board transfer system and the clinch operation are driven by a programmable controller, which is the computer's slave.

The six-axis robot inserts eight connectors, one socket, one potentiometer, one crystal clock, and the battery contacts. After insertion of over 10,000 components its bad-insertion rate is around 1500 ppm. The next step will be to introduce conformation to handle components that have less accuracy between leads and body than the ones now handled. Eventually, vision will be introduced for the worst-case components in pallets or distributed randomly.

Specifications of the robot's performance are as follows:

Repeatability: 0.04 mm
Maximum insertable area: 360 × 457 mm
Clinches up to three leads under the board
Uses passthrough handling
Can insert 60 different components at 12 stations on 5 levels
Misinsertion detected by pressure switch located in the hand of the robot
Maximum capacity: Up to 150,000 components/month on two shifts.

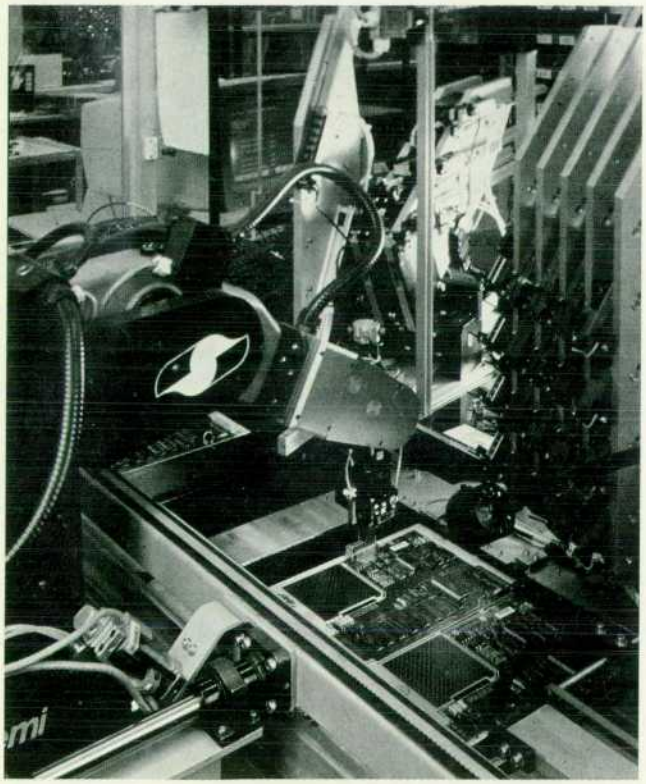

Fig. 1. *Six-axis robot inserts odd components.*

For better mechanical integrity, better dispatching repeatability, and faster control, components are ordered delivered in transparent plastic sticks. The required accuracy between leads and body is presently 0.05 mm to 0.1 mm.

Standard Component Insertion

For insertion of dual in-line integrated circuit packages, we use a multimode DIP inserter with two heads, one for 0.3-in width and one for 0.6-in width. A verifier is used with the 0.3-in head and we will soon have one on the 0.6-in head also. The verifier checks the polarity and roughly the logical function of the IC. This avoids misloading of components.

The axial VCD inserter takes care of axial components with a maximum diameter of 8.92 mm and a maximum length of 15.75 mm. The maximum center distance (distance between the two insertion holes) is 20.33 mm and the minimum is 3.81 mm. This machine requires a sequenced reel with the components placed in the order in which they will be inserted. This is done by another machine—a sequencer. The sequencer pulls the components from the vendor's reels and produces a new reel after checking for value, tolerance, and polarity.

Specifications of the standard component inserters' performance are as follows:

Maximum insertable area: 360 × 457 mm
Speed (in components per hour)
DIP inserter: 1600 actual (4000 theoretical)
VCD inserter: 7500 actual (12,500 theoretical)
Sequencer: 15,000 actual (22,500 theoretical)

Printed Circuit Board Design Guidelines

To facilitate automatic production, printed circuit boards are required to be the standard size, 360×457 mm. Subpanels measuring 285×457 mm may be used. No components can be placed along two edges of the boards or subpanels to facilitate automatic transfer and wave soldering without frames (5 mm along the 457-mm dimension must be free of components). For the DIP and VCD inserters, printed circuit board holes (finished) must be 0.4 mm larger than the maximum diameter of the component leads. For the robot, a finished hole 0.6 mm larger than the maximum lead diameter is required. Every IC must have the same orientation. The same rule applies for polarized axial or odd components. Axial components must be aligned at either 0 or 90 degrees. Additional rules take care of the volume of the machines' jaws or hand, and the volume of the clinch mechanism.

Acknowledgments

Many thanks to Yves Bonfort, printed circuit assembly manager, who has been a great help in implementing, improving, and pushing this project.

A Low-Cost, Reliable Analog Video Display Terminal Design

by René Martinelli and Jean Yves Chatron

THE ANALOG ELECTRONIC CIRCUITS in the HP 2392A Terminal are the power supply and the video circuit.

The main design goals for the HP 2392A's power supply were:

- Low cost
- Low power dissipation because of the compact terminal chassis and the absence of a cooling fan
- Meet international regulations for electromagnetic interference (VDE, FCC) and safety (UL, CSA, VDE, IEC)
- High reliability (which means low component count).

At the beginning of the project we investigated the possibility of using a commercially available supply. We eliminated this choice because we realized that a low-cost terminal cannot be built with a mixture of different, separately designed subassemblies. A single-team design is needed for the best coherent solution. Power supplies are a critical factor in the reliability of any terminal, and it is easier to solve problems that might occur in production if the design team is the same as that for the rest of the terminal.

The choice of a primary switching power supply was mandatory for heat dissipation reasons and for the potential influence on the CRT caused by a 50/60-Hz transformer.

Power requirements are as follows:

+5V, 2A	
+12V, 0.7A	Total secondary power = 32W
−12V, 0.4A	Primary power = 45W
+37V, 0.25A	

In the HP 2392A, internal thermal resistance is about 0.25°C/W, which leads to less than 15°C temperature increase above ambient temperature without forced air cooling.

Power Supply Principle

The HP 2392A power supply is based on the principle of the self-oscillating, nonsynchronous blocking converter. This is derived from the traditional flyback converter. Power conversion is done in two successive steps. First, energy is stored in the power transformer primary windings, and then the same energy is discharged in the secondary windings. The primary switching transistor and the secondary rectifiers are never turned on at the same time.

In contrast to the classical fixed-frequency, variable-duty-cycle conversion, both frequency and duty cycle are variable. The charge time (switching transistor on) is dependent on the line voltage. The discharge time (switching transistor off) is dependent on load variations. The system is self-oscillating, which means that the frequency is not imposed by the control circuit.

Fig. 1 is a block diagram of the power supply and Fig. 2 is a schematic diagram. The heart of the system is the TDA 4600 IC (U2). Its functions can be summarized as follows:

- Built-in startup circuit that gives a low startup current.
- Base current control. This is well-known as one of the biggest trouble areas in switching mode power supplies.
- Internal switching-power-transistor current image simulation. This makes possible automatic control of the saturated current gain of the switching transistor and automatic overload detection.

Fig. 3 shows how the power conversion scheme works, using a simplified schematic diagram for one of the output voltages. In Fig. 3, V_{in} represents the rectified line voltage (across C23 and C24 in series), L is the primary inductance of power transformer T1, and D represents one of the output rectifiers.

When switching transistor Q1 is on, L is charged and I_C rises linearly ($dI/dt = V_{in}/L$). Note that V_{in} is proportional to the line voltage. When Q1 is off, L is discharged through the secondary winding of T1. I_D decreases linearly ($dI/dt = -(V_{out} + V_D)/L$), where V_{out} = constant = regulated

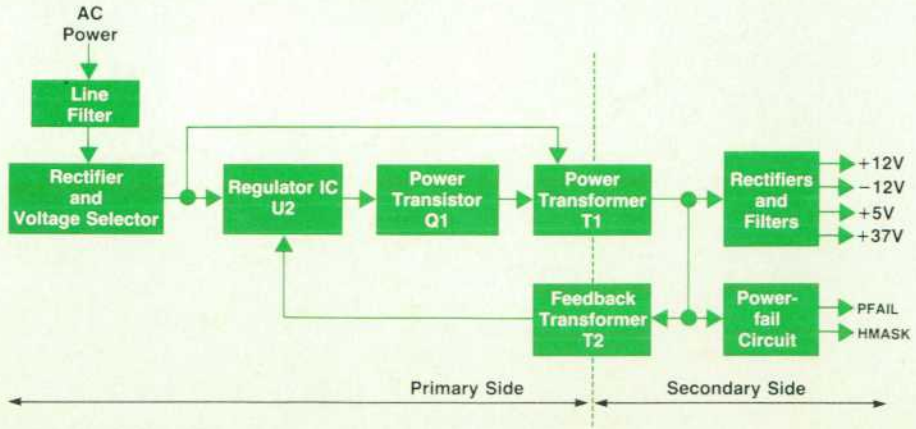

Fig. 1. *Block diagram of the HP 2392A power supply.*

secondary voltage. The switching transistor collector voltage is $V_{ce} = V_{in} + NV_{out}$, where N is the primary/secondary turns ratio of T1.

The third period in the regulation cycle is when both D and Q1 are off. During this time V_{ce} starts a self-oscillation whose frequency is dependent on L and the capacitor in the RCD network connected in parallel with Q1. These components (C32, R33, CR29, and CR30 in Fig. 2) are used to optimize the safe operating area of the switching transistor.

The secondary voltage of T1 follows the primary waveform; primary and secondary voltages are related by the turns ratio of T1.

Regulation

Since the system is self-oscillating, the TDA 4600 (U2) does not provide any clock or oscillator; it only monitors each phase to provide the appropriate controls, which are as follows:

Power supply startup. The TDA 4600 receives power through R20 and C30 during the initial turn-on time. Start-up current is only 5 mA, so the power dissipation in R20 is only 1.5W. When secondary power is available, it is rectified by CR26 and CR27 and supplied to the TDA 4600. The interesting point is that no auxiliary 50/60-Hz transformer is needed, which reduces the cost, the board space, and any potential interference with the nearby CRT.

Start of cycle. As shown in Fig. 3, the secondary voltage crosses zero during the third phase of the cycle (self-oscillation). This zero point is fed back to U2 pin 2 through an RC network (R24, C28), and causes a delay that determines the start of the next cycle. At this point the switching transistor voltage and current are almost zero, which increases the reliability of the transistor by decreasing its power dissipation.

Feedback and reference voltages. An internal positive reference voltage is available on U2 pin 1. A secondary voltage is rectified by CR25, and consequently, a negative voltage is available on C25. A combination of the positive reference voltage and the negative feedback voltage is sent to U2 pin 3 by the resistive network consisting of R29, R32, R26, and R25. This is the regulation loop error signal.

Because of very strict safety regulations, it was not possible to find acceptable low-cost optocouplers, so we use a small transformer for feedback (T2). Its primary is connected to the 5V secondary winding and its secondary is rectified by CR25.

We could have used one of the secondary windings of T1, but again safety regulations impose large primary-to-secondary spacing, which gives bad coupling and thus very loose feedback. Another advantage of our solution is that we use only a single regulator for the four output dc voltages, and two separate transformers give less interaction between the different voltages.

Current sensing. Generally, a current-sensing resistor is used in power supplies to provide current measurement. In a switching mode power supply it is not easy to do that, so a different technique is used here. Fig. 4 shows how it works.

When the switching transistor Q1 is on, the current I flowing in it can be derived from the relation $V_{in} = L(dI/dt)$. The voltage v on pin 4 of U2 can be derived (when very close to zero) from the equation $V_{in} = (dv/dt)(R27 \cdot C26)$. Therefore, the voltage v is an "image" of the current I. The

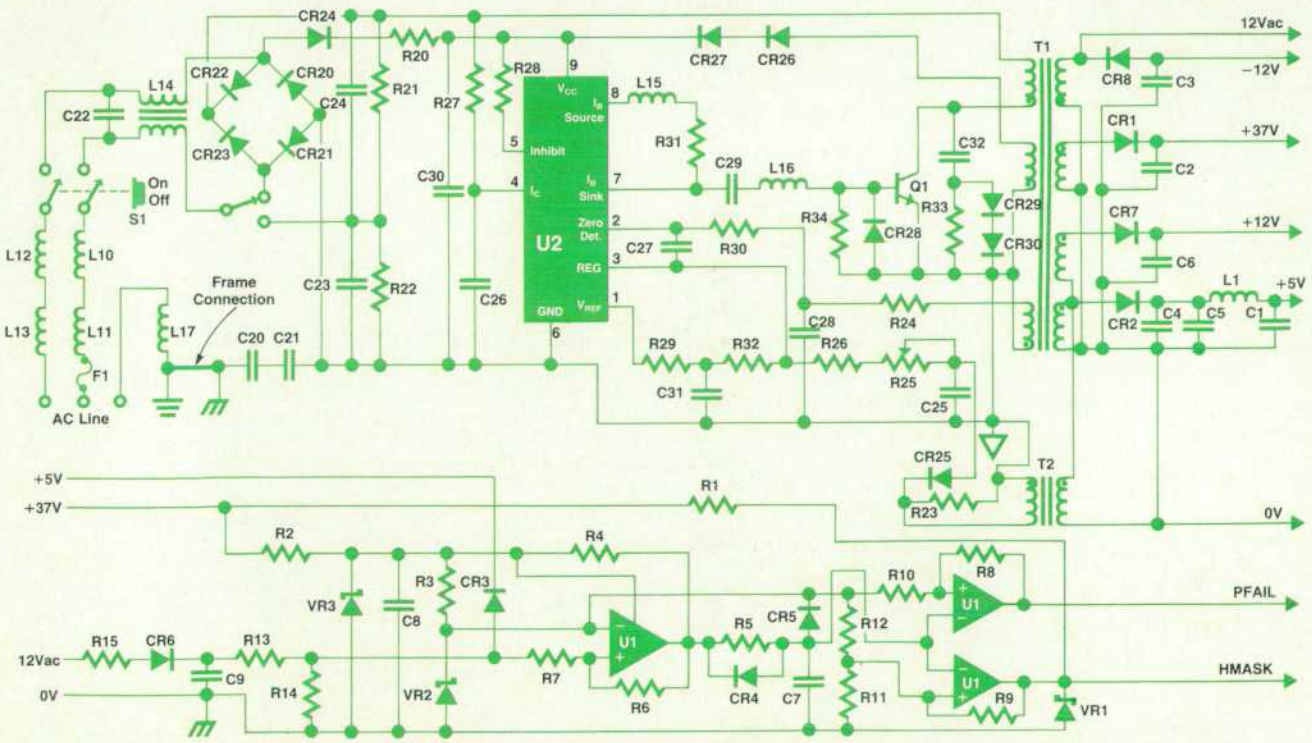

Fig. 2. *HP 2392A power supply schematic diagram.*

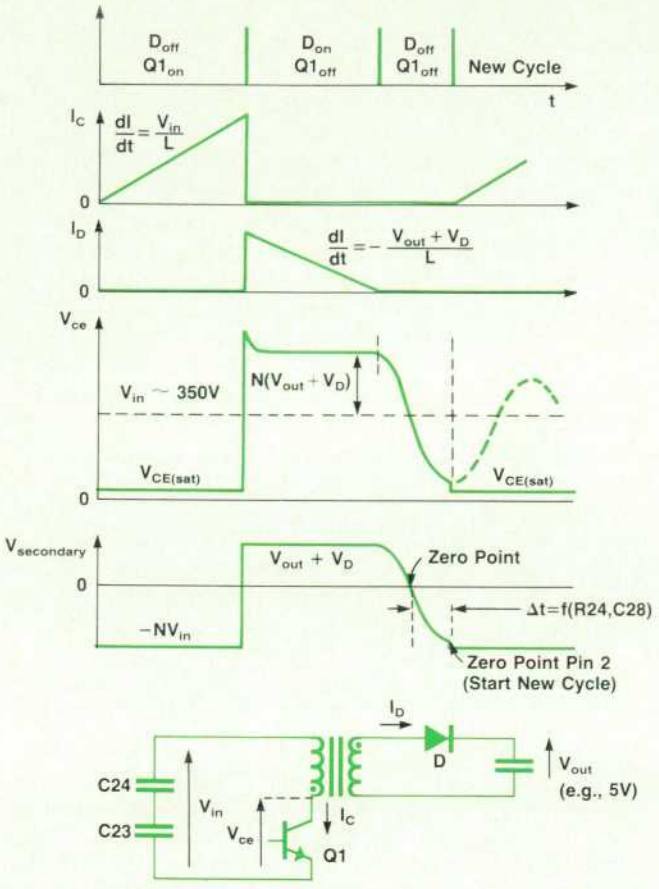

Fig. 3. *Simplified power supply schematic and waveforms illustrating the power conversion scheme.*

TDA 4600 uses it internally to manage the base current of Q1 so that the saturated current gain of Q1 is maintained at the proper value. The voltage v is also used for overload protection. When a secondary overcurrent or a primary malfunction occurs, primary switching is automatically turned off.

Powerfail detection. Powerfail circuitry is needed to predict a future secondary dc voltage drop as soon as the line voltage is shut down. In a switching mode power supply this is a tricky problem when no auxiliary 50/60-Hz transformer is used. The secondary voltage (Fig. 3) has two interesting points. First, the positive portion follows the regulated dc voltage (of course, this assumes that the dc voltage is positive). Second, the negative portion follows V_{in}, which is directly dependent on the line voltage. Fig. 2 shows how these points are exploited. We use the 12Vac secondary winding and rectify it positively with CR6 and C9. The voltage on C9 will drop a few milliseconds before all the regulated dc outputs. This voltage is processed by U1 and associated circuitry to produce two signals. PFAIL tells the processor board either that power will fail (during power-off) or that the output voltages are stabilized (power-on). HMASK is used to block the conduction of the horizontal drive transistor during power-on to increase the reliability of this transistor.

Conducted Interference Suppression

For suppression of conducted electromagnetic interference, we decided not to use off-the-shelf filters, preferring to build our own filter on the power supply board. One advantage is lower cost, because the filter is not general-purpose, but is designed exactly for the interference caused by the terminal. A second reason for building our own filter is that the filter layout is more important than the filter itself. The best choice is to mount it on the power supply board very close to the ac plug without extra wiring.

Referring to Fig. 2, L14 is a double-core, wound, common mode inductance used in all similar filters. It must be noted the only one X capacitor is used (C22) to cut off differential noise. The Y capacitor is connected between the primary common and the ground. We use two capacitors in series (C20 and C21) to comply with safety regulations. L17 consists of three turns of wire around a ferrite bead. This enables us to have a floating ground that cuts off common mode noise. Between the ac plug and the power switch we use a series of chokes (L10 through L13) to suppress interference caused at high frequencies (around 25 MHz) by the video and logic board signals. This design has passed VDE level B with a typical margin of 6 dB, sufficient to qualify for the VDE radio protection mark.

CRT Display Circuitry

Fig. 5 is a block diagram of the CRT display circuitry. Figs. 6, 7, and 8 are schematic diagrams of the vertical amplifier, horizontal drive circuit, and video amplifier, respectively.

The vertical and horizontal drive circuits are both located on the same single-layer printed circuit board. The video amplifier is mounted at the rear of the CRT neck on a separate board.

The vertical amplifier schematic (Fig. 6) shows a classic linear amplifier. There are two stages.

Q2 is used as a switch controlled by the vertical sync pulses. When the switch is on (vertical retrace) the voltage on C18 is zero. As soon as Q2 is off, the collector voltage of Q2 rises linearly, generating the sawtooth waveform needed for vertical deflection.

U1, Q6, and Q7 form a voltage-to-current converter that causes the current in the deflection yoke to be a linear ramp. The vertical frequency is 60 Hz and the vertical

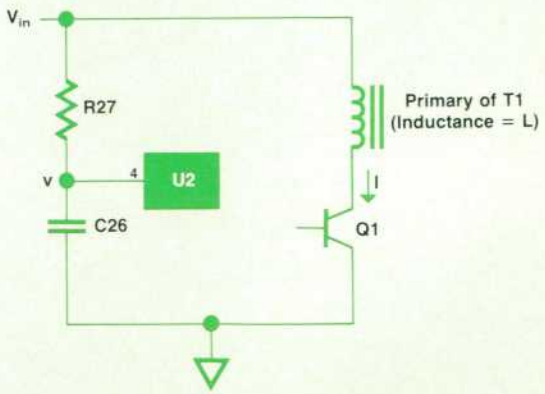

Fig. 4. *Instead of a current-sensing resistor, the HP 2392A power supply uses the voltage v to measure the current I.*

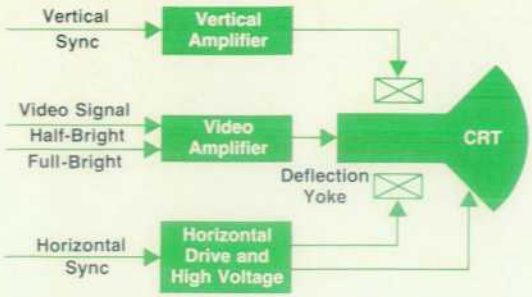

Fig. 5. *Block diagram of the video display circuits.*

retrace time is 1 ms. The use of a classical operational amplifier and two complementary transistors was preferred to the use of an integrated off-the-shelf vertical amplifier because of cost and component count. No heat sink is needed for Q6 and Q7.

The network connected between the deflection yoke (point A in Fig. 6) and ground needs some explanation. R21 is used as a current-sense resistor to provide feedback to operational amplifier U1. C21 is used as an ac path for the deflection current. The voltage across C21 is parabolic with time, since it is an integration. This voltage is fed back to U1 to generate the S-shaped waveform needed for CRT deflection.

The output transistors work in class B. Only one is conducting at a time, which gives much better reliability and eliminates production adjustments. To avoid crossover distortion in the middle of the screen we use a very small compensation capacitor (C13 = 10 pF) to minimize the transition time.

In the horizontal drive circuit (Fig. 7), the classical concept of a flyback transformer has been used, with the following features:

- No transformer is used to drive the base of the power switching transistor Q5. We use capacitive coupling (C15) instead.
- At this level the biggest problem is the turn-off time variation from one transistor to another, which generally makes the use of a one-shot adjustment in production mandatory for horizontal image centering. To avoid this problem, the switching transistors Q4 and Q5 operate without saturation through the use of an antisaturation diode CR4.
- The network CR7-C16-R20 is used as a dynamic clamp to reduce the amplitude of dangerous transient voltages that could occur if some malfunction happens in the horizontal sync circuit (e.g., during service or in a bad environment). This increases the reliability of Q5.
- A voltage supply of 37V is used instead of the often-found 12V supply. The advantages are that the 37V low-current supply is cheaper to produce with our power supply concept, and that there is no need for bootstrap conversion from 12V to 37V in the horizontal drive circuitry. Power efficiency is better by a factor of more than two, because only one transformer is needed to go from 115/220V to 37V.

The purpose of the video amplifier (Fig. 8) is to drive the CRT cathode either with full peak-to-peak voltage swing for full brightness (0 to 30V) or half swing (15V to 30V). Q2 is the video amplifier, and Q1 is the full/half-bright mode switch. The same antisaturation technique that is used in the horizontal drive circuitry is implemented with diode CR3. The video amplifier board is mounted on the neck of the CRT for two reasons. One is lower capacitance of the cathode connection, which simplifies the video circuitry and increases the speed (minimum dot duration is 40 ns). The other is lower electromagnetic radiation because of a lower voltage swing on the connecting wires (0.5V p-p input instead of 30V p-p output).

Radiated Interference Suppression

For radiated interference, the main source is the logic

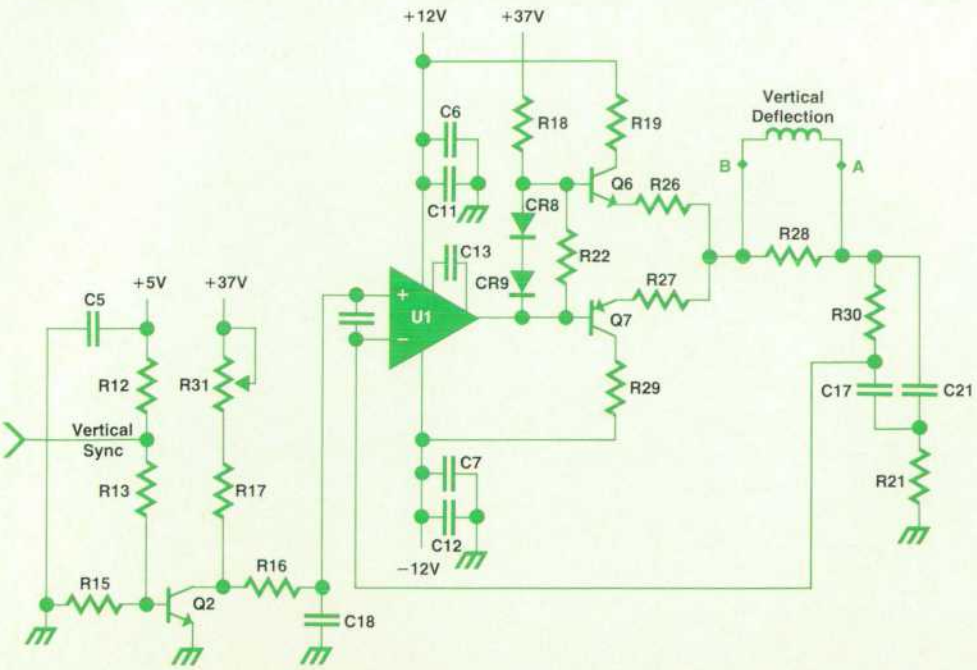

Fig. 6. *Vertical amplifier schematic diagram.*

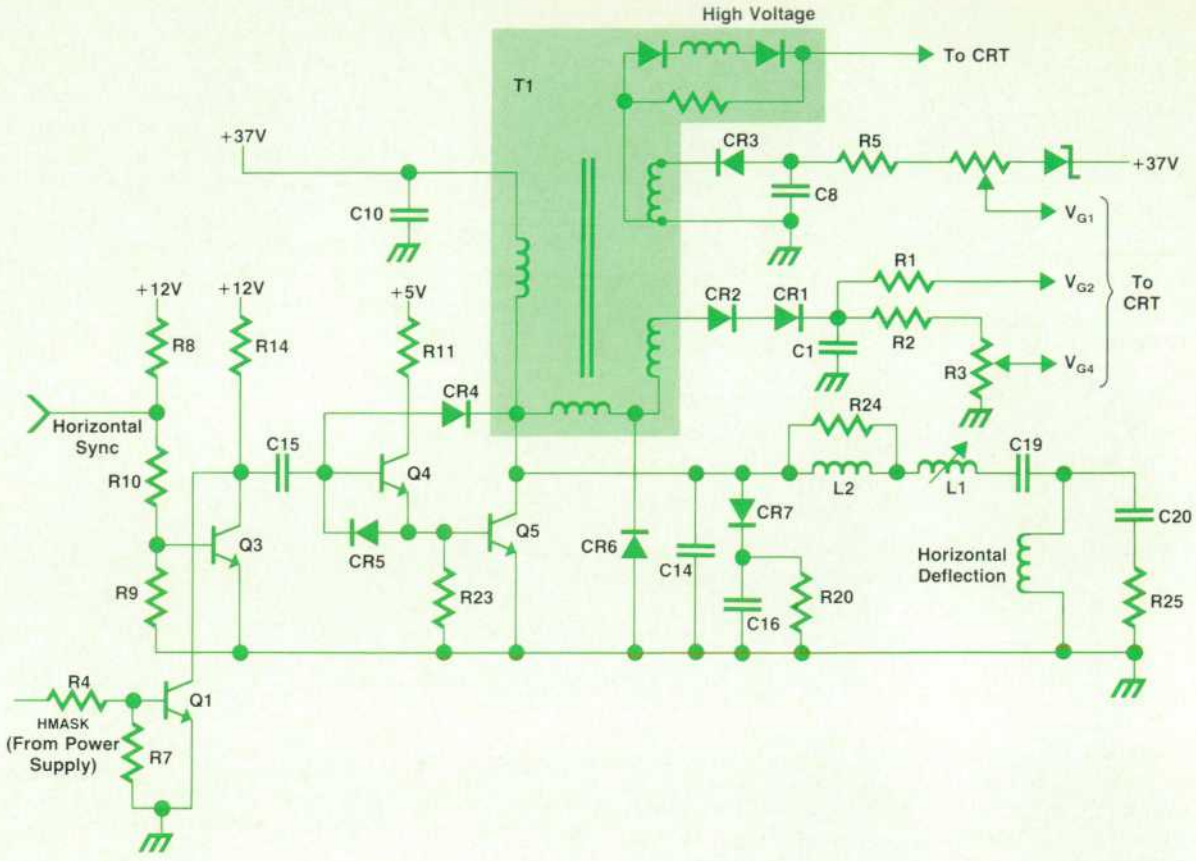

Fig. 7. *Horizontal drive circuit schematic diagram.*

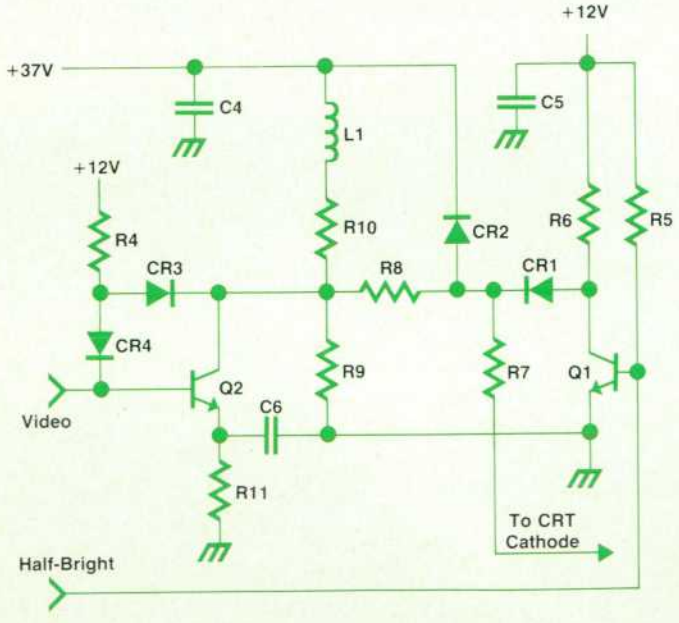

Fig. 8. *Video amplifier schematic diagram.*

circuitry (microprocessor buses and clocks) and the 25-MHz video circuitry (from the CRTC to the CRT cathode). As mentioned earlier, the decision was made to mount the video board as a separate assembly close to the CRT neck, which eliminates the need for expensive shielded cables. On the logic board we tried to minimize the speed of the logic whenever possible, and to minimize the length of all critical traces. The video traces were greatly reduced by integrating many functions into a gate array and a CRTC chip (see article, page 9).

The clock oscillator was responsible for interference at all the multiples of its fundamental frequency (8 MHz). Only 2 cm of printed circuit traces between the oscillator and the gate array was enough for the radiation to exceed the acceptable level. To cure this problem, we asked the oscillator manufacturer to change the waveshape from square to half sine.

The result is that we passed VDE level B with a typical margin of 6 dB without any shielding on the boards or internal cables. The logic board has only two layers, while many similar designs use four layers for EMI suppression.

The use of a shield around the logic board would have caused many problems. An efficient shield must be hermetically closed, which means thermal problems incompatible with the no-fan design of the HP 2392A. The only way to guarantee shielding effectiveness in production would have been to use expensive gaskets, which is not acceptable for a low-cost design.

Authors

April 1985

4 Low-Cost Terminal

Jean-Louis Chapuis

Jean-Louis Chapuis is a section manager at HP's Grenoble Networks Division and has been at HP since 1978. He provided technical marketing support for the HP 263X family of printers and 264X family of terminals, was the designer of the HP 3074M Data Link Adapter, and was the project manager for the HP 2392A Terminal. Before coming to HP he was a researcher and teacher in an R&D lab for the French Air Force. Jean-Louis is a native of Rochefort, France and earned an electronic engineering degree from the École Supérieure d'Électricité in 1977. He lives in Meylan, France with his wife and two daughters and likes skiing, bicycling, and reading.

Michèle Prieur

Michèle Prieur came to HP in 1980, the same year she earned a degree in electronic engineering from the École Supérieure D'Électricité. She contributed to the development of the firmware for the HP 2392A and is now working on terminal emulation. She is interested in terminal firmware and application software for personal computers. Michèle was born in Lyon, France and is a resident of Grenoble, France. She is married and enjoys horseback riding.

8 Terminal Mechanical Design

Michel Cauzid

Michel Cauzid was born in Vouziers, France and received his diploma from the École Nationale Supérieure de Méchanique et Microtechniques in 1970. Before coming to HP in 1979, he taught mathematics in Africa as an alternative to French military service and worked in micromechanics. At HP he has been a mechanical designer for the HP 2333A Controller, the HP 3092 Terminal, and the HP 2392A. Michel's professional specialty is computer-aided design. He is a resident of Bresson, France, is married, has four sons, and enjoys hiking.

9 Terminal VLSI Design

Jean-Jacques Simon

Born in Metz, France, Jean-Jacques Simon studied electronics at the University of Nice, from which he received masters and doctoral degrees (1975 and 1978). At HP since 1977, he has contributed to hardware and firmware development of a number of terminal products, including the HP 3075A, 3077A, and 2642A. He was also the project leader for IC development for the HP 2392A Terminal and is coauthor of a patent on the HP Human Interface Loop. Jean-Jacques is married, has two children, and lives in Saint Egrève, France. He likes outdoor activities and rides his motorbike to work every day, even in the winter.

16 Automated Production

Christian-Marcel Dulphy

Christian-Marcel Dulphy was born in Tonnay-Charente, France and graduated in 1966 from the École Nationale Supérieure d'Électronique et de Radioélectricité de Grenoble. Before coming to HP in 1972 he served as a chief petty officer in the French Navy and worked as an electronics technician and as an R&D engineer. His HP experience has centered on engineering and management in production and manufacturing. He contributed to the development of the manufacturing process for the HP 2100 Computer and the HP 7905 Disc Drive. His professional interests include robotics and automation. Christian-Marcel is married, has three children, and lives in Saint-Egrève, France. When he is not involved in do-it-yourself projects, he enjoys cross-country skiing, hiking, gardening, and reading.

18 Terminal Analog Design

Jean-Yves Chatron

Jean-Yves Chatron joined HP's Grenoble Division in 1973, where he has worked as a production engineer, a service engineer, and as an R&D engineer. He contributed to the development of the HP Interface Bus for the HP 3075A Terminal and designed the power supply for the HP 2392A. A native of Nantes, France, he received an engineering degree from the Institut Universitaire de Technologie (1972) and served in the Army as a radio communicator. He now lives near Grenoble, is married and is the father of two sons and a daughter. Outside of work, he is interested in audio electronics.

René Martinelli

René Martinelli was born near Grenoble, France and received a master of science degree from the University of Grenoble (1969) and an electronic engineering degree from the University of Toulouse (1971). His experience before coming to HP in 1973 was in IC test design. At HP he has been a production engineer on the HP 2100 and HP 21MX series of computers, the supervisor of the local HP repair center, and an R&D engineer. He contributed to the design of the HP 307X family of terminals and was the project leader for the analog design of the HP 2392A Terminal. He lives with his wife and son in Eybens, France and likes amateur radio and skiing.

25 Intelligent Plotter

Martin L. Stone

Martin Stone received his BSME degree from the University of Texas at Austin in 1973 and came to HP's San Diego Division in the same year. He has been a manufacturing engineer and was an R&D engineer and project manager for the HP 7550A Plotter. A native of Dallas, Texas, he now lives in San Diego, California and enjoys backpacking, racquetball, golf, and playing his guitar.

Todd L. Russell

Todd Russell is an R&D engineer at HP's San Diego Division. Since coming to HP in 1978 he has contributed to the design of plotter products, including the HP 7090A and the HP 7550A. Todd was born in Los Angeles, California and now lives in San Diego, California with his wife and son. He is a scoutmaster and commissioner for the Boy Scouts of America and is interested in camping, softball, tennis, and church activities.

Peter L. Ma

Peter Ma was born in Hong Kong and educated at the University of Washington (BSEE, 1978) and at Stanford University (MSEE, 1982). He joined HP in 1978 and designed the I/O processor system for the HP 7310A Printer and the digital circuits and gate arrays for the HP 7470A Plotter. He was the project leader

for the electronic design of the HP 7550A and is now the section manager for manufacturing engineering. Peter lives in San Diego, California and is interested in tennis, skiing, water sports, and traveling. He is also an audio enthusiast.

Jeffery W. Groenke

A native of Minneapolis, Minnesota, Jeff Groenke attended the University of Minnesota (BSME, 1980) and San Diego State University (MSME, 1983). He has been at HP since 1980 and has worked as a manufacturing engineer and later as an R&D engineer for the HP 7550A. He is a member of the ASME and is continuing his engineering education at the University of California at San Diego. Jeff is a resident of San Diego, is married, and has a son. His outside interests include skiing, bicycling, sports cars, and spending time with his family.

29 Pen-Lift Mechanism

Hatem E. Mostafa

Hatem Mostafa is an R&D project leader at HP's San Diego Division. After joining HP in 1979, he designed the power supply for the HP 7580A Plotter. Later he designed the linear motor, the drive electronics, and the servo control system for the penlift for the HP 7550A. He is the coauthor of a November, 1981 HP Journal article on the HP 7580A. Hatem was born in Cairo, Egypt and received his BSEE degree from the University of Minnesota in 1979 and his MSEE degree from Stanford University in 1982. He lives in San Diego, California with his wife and loves the ocean. He enjoys scuba diving, body surfing, and walking on the beach.

Tammy V. Herr

At HP's San Diego Division since 1980, Tammy Herr has been a development engineer and mechanical designer. More recently she has worked as a regional sales engineer and sales development engineer. She is a native of San Diego, California and presently lives in Fallbrook, California with her husband. She likes skiing, bicycling, body surfing, sailing, and guitar playing.

31 X-Y Servo

David C. Tribolet

Born in Tucson, Arizona, Dave Tribolet was educated at the University of Arizona (BSME, 1978) and Stanford University (MSME, 1979 and MSEE, 1982). Since coming to HP in 1979 he has been a mechanical designer for the HP 7470A Graphics Plotter and a project leader for the HP 7550A Plotter. He is now an R&D project manager. He is the coauthor of an HP Journal article on the HP 7470A and is named as a coinventor on a patent on a bidirectional pen change mechanism. His work has also resulted in a patent application on a switchless pen sensor. Dave lives in San Diego, California, teaches a machine design course at the University of California at San Diego, and enjoys basketball and bicycling.

Thomas J. Halpenny

Author's biography appears elsewhere in this section.

Kenneth A. Regas

Ken Regas was born in San Diego, California, served in the U.S. Navy, and received a BA degree in management from Golden Gate University in 1976. He also studied at San Jose State University (BSME, 1980) and at Stanford University through the HP fellowship program (MSME, 1984). At HP since 1980, he contributed to the development of the HP 7550A and is now an R&D project leader. Ken is a resident of Poway, California, is married, has two children, and is interested in machine design and control.

34 Plotter Firmware

Thomas J. Halpenny

Tom Halpenny came to HP in 1974 and has worked on firmware development for a number of HP plotters, including the HP 7245A, HP 7221B, HP 7220A, and HP 7550A. He received his BS degree in engineering from Harvey Mudd College in 1973 and his MSEE degree from Stanford University in 1974, and is interested in computer programming and firmware development. A native of San Diego, California, Tom now lives in Escondido, California, is married and has a young daughter. He likes bicycling, video engineering, and reading books to his daughter.

An Intelligent Plotter for High-Throughput, Unattended Operation

This plotter quickly produces multiple copies of high-quality graphics output for use in presentations and reports. Its high throughput and automatic cut-sheet feeder make it useful for unattended operation in shared environments.

by Martin L. Stone, Peter L. Ma, Jeffery W. Groenke, and Todd L. Russell

THE EXPLOSION OF COMPUTER GRAPHICS in the business and technical environments has been intensified by the availability of products that generate hard-copy color graphics easily. Hewlett-Packard's pen plotters have made major contributions in this area, especially with the advent of microgrip plotting technology.[1,2] The application of this technology made HP plotters excellent high-performance, high-quality, low-cost solutions for both environments. There were features, however, that plotter customers were demanding, but that did not yet exist. These consisted of much greater throughput, unattended operation, more intelligence, and drafting plotter capabilities in an A/B-media-size machine. The addition of these features at a very low price while retaining the highest quality was paramount in the design of the HP 7550A Graphics Plotter (Fig. 1).

The HP 7550A is an eight-pen, A/B-size plotter with high quality and performance. Its increased throughput was achieved by developing high-performance servos to drive the pen and paper axes and the pen-lift mechanism. Placing the HP 7550A's microprocessor in all three servo loops, performing extensive servo modeling, and developing sophisticated control firmware were all key points in the resulting high-quality, high-performance, low-cost design. Plots done on the HP 7550A take less than half the time that they take on many other small-format plotters without sacrificing plot quality.

The customer's need to minimize time in handling pens and paper is answered by the HP 7550A's design. Thanks to the automatic cut-sheet feeder, the user no longer has to load plain paper or transparencies by hand, and the great inconvenience of tearing off sprocket holes or separating plots along perforations is eliminated. The design of the pen-lift mechanism contributes to lengthening the life of

Fig. 1. *The HP 7550A 8-Pen Graphics Plotter is designed for high-throughput, unattended operation. These features allow the preparation of multiple copies of high-quality computer graphics, automated output of single charts for process monitoring, or use as a central graphics server.*

the pen by carefully controlling the velocity of the pen as it hits the paper. These features make the HP 7550A an excellent choice as a central source of hard-copy graphics, or for automatic test and process control systems.

Ease of use, or friendliness, comes from the extensive firmware features included in the HP 7550A. One key contribution is the internal, 12K-byte, user-definable graphics memory. This memory space can be allocated for five different functions: I/O buffer, vector buffer, replot buffer, space for polygon fill definition, and downloadable character space.

Two of the most powerful features are the replot and polygon fill capabilities. The replot buffer enables the user to store an entire plot in the HP 7550A and then reproduce it up to 99 times. Now the user can give a presentation using transparencies plotted by the HP 7550A and give the audience personal copies of the same information produced quickly and easily on paper. The polygon (area) fill capability is a real time-saving benefit in user programming and plotting time. Instead of programming a plotter to move stroke by stroke (many, many instructions) to fill a complex solid or crosshatched area, all the user must do is invoke two or three HP-GL (Hewlett-Packard Graphics Language) commands to define a polygon and a fill type. From this information, the HP 7550A automatically figures out the required number and pattern of strokes.

Another contribution is the 32-character liquid-crystal display on the front panel. This display, coupled with the keyboard design, gives the user a simple menu-driven front panel that is easy to operate. Also, with the use of an internal nonvolatile memory, the customer can completely configure the HP 7550A in an RS-232-C/V.24 or HP-IB (IEEE 488) environment through the front panel, thus eliminating bothersome rear-panel switches.

The final major customer need addressed by the HP 7550A is for a plotter for the low-cost CAD/CAM systems available today. Users of these systems want a quality A/B-size drafting plotter with a price in agreement with the rest of their system. The HP 7550A is designed to use both polyester film and vellum paper, and liquid-ink as well as roller-ball pens. The high throughput of this plotter makes it a very good solution for producing check plots quickly, and its drafting-quality output produces excellent final drawings.

Mechanical Design

The mechanical design of the HP 7550A is characterized by the widespread use of plastic molded parts. This low-cost design approach was taken while still keeping quality and reliability as the top objectives. Many parts are designed to serve several purposes.

- Pen carriage:
  - Actuates a cam that lifts the pinch wheels for paper loading.
  - Actuates a cam to uncap pens during pen picks.
- Pen-lift mechanism:
  - Opens access door to platen surface to begin automatic paper-load sequence.
  - Senses paper during paper loading.
- Carousel sensing pair:
  - Detects presence, type, and positions of pens in carousel.
  - Detects up/down position of plotter window.

The key mechanical designs are highlighted in the articles on pages 29 and 31.

Electronic Design

The objective of the electronic design was to develop a cost-effective means of providing a high level of functionality and many enhanced features. For instance, one main printed circuit board contains nearly all of the electronic circuits, leaving only a small portion on the servo motor's optical encoder board and the pen-lift's encoder board. More functions and higher performance can be found on the one main board than are on seven separate boards from an earlier HP plotter. Several design philosophies helped achieve this, such as replacing analog circuitry with digital circuitry whenever possible, using large-scale integration (LSI), eliminating the need for any adjustments, and performing many functions with the same components.

The single 68000 microprocessor controls every movement in the servo motors and pen-lift mechanism from commands received through the HP-IB or RS-232-C interface. It services the front panel and rotates the carousel

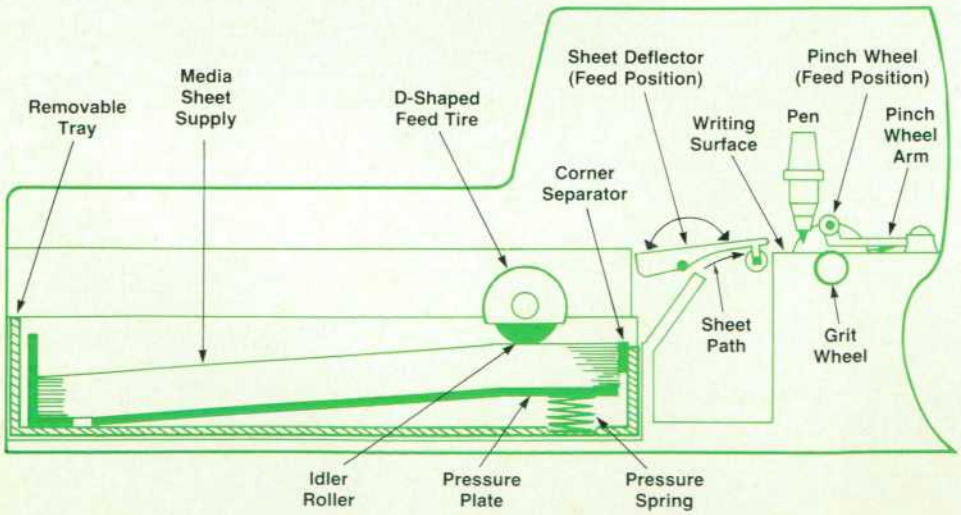

Fig. 2. *The HP 7550A Plotter's sheet-feed mechanism is similar to that of a photocopier, but with much higher alignment accuracy. It can feed up to 150 sheets without reloading.*

and paper-feed step motors. It also participates in measuring the unregulated power supply voltage for the servo motors by successive approximation. The task of continuously pulsing the LED (light-emitting diode) in the carousel detector is performed entirely by the microprocessor, rather than by a separate timer circuit.

The digital electronics section is greatly simplified by the use of the 68000 microprocessor and two custom standard-cell ICs manufactured at HP's Cupertino Integrated Circuits Operation. The microprocessor's strong output drive capabilities and the use of high-density ROMs and RAMs eliminate the need for any costly address or data bus buffering. The two custom 40-pin NMOS ICs contribute to significant cost savings by replacing more than 80 small-to-medium-scale ICs. Overall, the digital section is mostly made up of a handful of LSI components, reaping the benefits of increased reliability and reduced board space and power consumption.

The power supply portion of the electronics offered some interesting challenges. The servo motors require a power supply with very high (greater than 300 watts) peak power capabilities to produce the desired accelerations and decelerations. Since servo performance depends on the supply voltage, a costly regulated design would seem necessary. However, by not regulating the voltage, but instead measuring the value and compensating the servo operating parameters in firmware by using the microprocessor, optimum performance can be maintained. To help keep the power supply simple, a single switching circuit provides three regulated voltages—a tightly controlled 5-volt output along with two adequately controlled 12-volt outputs. The switching circuit takes advantage of a sophisticated IC regulator and employs a switching element that gives three outputs rather than just one. The result is a much reduced parts count and improved efficiency and reliability.

Unattended Media Handling

Unattended operation requires that a plotter be able to supply a new sheet of plotting media without user intervention. Most plotters that feature automatic media handling use a system that supplies the media from a rolled or fanfold format. It was decided early in its design that these formats were unacceptable for the HP 7550A's intended market. These formats require special paper which is more expensive. To change the media type, the user must go through a time-consuming sequence of removing and changing the supply and getting the new media started in the feed system.

Hence, the decision was made to design this new plotter with an integral system for feeding precut stacks of sheet media. The system requirements were that it be able to remove individual sheets from a supply stack, deliver each to the writing area, and align each sheet with the pen axis within two-tenths of a degree. Also, it had to eject and stack completed plots automatically and provide capabilities for feeding ANSI A and B and ISO A3 and A4 papers, as well as A and A4 transparency film. The system had to be very reliable, yet provide easy access if a feed failure should occur. In addition, the ability to load single sheets manually was required.

The cut-sheet feeding system for the HP 7550A uses a forward buckling technique for separating the top sheet from the supply stack (Fig. 2). This technique, commonly seen on inexpensive photocopiers, was selected because of its low cost and high reliability. The stack of sheets is first placed in a removable tray in which are mounted two corner separators, one at either side of the forward edge of the stack. These separators allow the feed tires to buckle an individual sheet off the top of the stack. The stack is pressed up against the feed rollers by two compression springs under a hinged plate, which is located in the tray directly beneath the stack. Two different trays are available. One comes with the instrument and can be adjusted easily for A or A4 media sizes. The other is an inexpensive option and can be adjusted easily for B or A3 media.

A significant contribution of the sheet feeder is the design of the feed shaft system. Conventional feed systems use two rubber tires mounted to the feed shaft by one-way mechanical clutches and forced down on the stack, requiring an elaborate mechanism to relieve the tension springs when the user desires to insert or remove the tray. The HP 7550A uses a specially designed feed tire which has a flat cut on one side, giving it the shape of a D. When the flat side is lined up parallel with the surface of the top sheet, there is no contact, and the tray can be removed easily without the need for any complex release mechanisms. A key element of this system is that the HP 7550A's microprocessor must be able to determine the orientation of the feed shaft, so the flats can be positioned parallel to the media when a sheet is not being fed. To do this, a very simple encoder was designed, consisting of a molded plastic gear with a narrow slit and an LED emitter-detector pair. This gear runs off the same gear the step motor uses to drive the shaft. The gear is keyed to the shaft orientation and passes between the emitter-detector pair. When the slit passes in front of the emitter, the receiver generates a signal that indicates to the processor that the shaft is aligned, and the feed cycle is complete.

Once the sheet has been pushed from the tray, it strikes

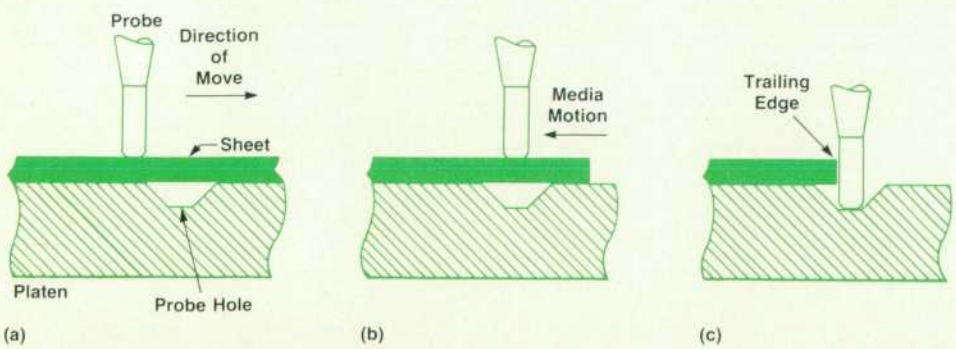

Fig. 3. *Edge sensing. (a) A probe on the Z carriage bottoms on the media. (b) The Y carriage moves the probe over a hole in the platen. (c) As the trailing edge of the sheet passes, the probe drops into the hole.*

a ramped surface, which directs it upward into a deflector. This deflector can be rotated open by motion of the Z carriage (pen-lift mechanism) to direct the sheet onto the platen. The pinch wheels are raised by engaging the Y carriage (pen-holder carriage) with a rotating cam. The sheet is fed until the D-shaped feed tires have completed a full revolution, passing the leading edge of the sheet under the raised pinch wheels. The Y carriage then disengages the cam, lowering the pinch wheels and grabbing the sheet between the pinch and grit wheels. Then, the sheet is ready to be pulled from the tray with the X-axis drive motor.

Edge sensing is done with the Z carriage. The Y carriage is moved over the platen and the pen holder is lowered. Since there is no pen in the holder at this time, lowering continues until a probe bottoms on the sheet on the platen surface (Fig. 3a). The position is read from the Z-carriage linear encoder and recorded. The platen height (including media thickness) is now known. The Y carriage then makes a short move, dragging the probe across the sheet until it is over a hole in the platen. Now the sheet is pulled from the tray (Fig. 3b). As the trailing edge passes, the probe drops to the bottom of the hole, signaling the end of the sheet (Fig. 3c). The paper length (A/A4 or B/A3) can be determined by reading how long the sheet was pulled before the trailing edge was detected.

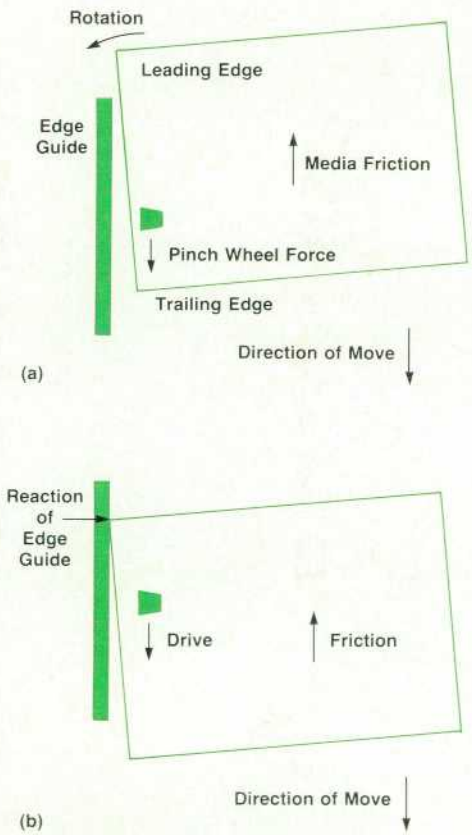

Fig. 4. *Sheet alignment. (a) As the first move begins, the sheet rotates about the left pinch/grit wheel combination and toward the edge guide. (b) As the move continues, the edge under the left pinch/grit wheel combination approaches the guide. Then a move in the reverse direction completes the alignment of the sheet against the guide.*

Once the entire sheet is on the platen, the alignment sequence starts by raising the right pinch wheel, leaving only the left pinch wheel engaged. The sheet is then driven back and forth twice. Initially the sheet is completely away from the left guide. As the first move begins, a mechanical couple is set up between the driving left grit wheel on one hand and the media's friction against the platen surface (Fig. 4a) and its inertia on the other. This causes the sheet to rotate about the left grit wheel and swing in against the edge guide. A stop above this guide keeps the sheet from climbing up and over it. As the move continues, the media edge under the left pinch wheel approaches the edge guide (Fig. 4b). The left grit wheel direction is then reversed, causing the trailing edge to move completely against the guide. After two more passes, the sheet is firmly aligned to the guide.

The final tasks are to find the trailing edge accurately (it is roughly known already) and to determine whether ISO or ANSI standard media is being used. The trailing edge is found as before. To determine which standard is used, the sheet width must be measured. The position of the left edge is now known to be at the edge guide. Only the right edge need be found to calculate the sheet width. The procedure is similar to that for finding the trailing edge. The Y carriage is moved to the right side of the platen over a slot (underneath and perpendicular to the right edge of the sheet) and inside the edge of an ANSI sheet, which is the narrower of the two (11 inches versus 297 mm). The probe is lowered until it bottoms on the sheet. The Y carriage is then moved enough to the right to be beyond an ANSI sheet edge. If the probe drops into the slot, the size is known to be ANSI. Otherwise, it is assumed to be ISO. The plotting area is now set.

After plotting, the sheet is unloaded on command by ejecting it past the grit wheels, stacking it in a catch tray placed behind the plotter. A new sheet is then automatically loaded, aligned, and ready for plotting.

Acknowledgments

The success of the HP 7550A was due to the great efforts of many people. Product design was done by Dick Kemplin and Lynn Palmer. The project benefited from the early leadership of Neal Martini, as well as continued support from Peggy Wyman and John Page. Bill Royce had the responsibility for the power supply and motor drive circuits and for meeting product electromagnetic-compatibility goals. Dave Ellement and John Wickeraad were involved in designing the custom ICs and the digital circuits.

Special thanks to Wally Halliday for the initial sheet feeding mechanism, Mark Majette for the media drive axis, and Kevin Bockman for the unloading design.

We could not have been successful without the extensive efforts of our manufacturing team: Juergen Przyllas, John Morton, Steve Lorenc, Rich Mandle, Marv Kozai, Otto Hirr, Dave Kelly, and Tim Holscher. And we give special thanks for the support and guidance of Norm Johnson.

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Low-Mass, Low-Cost Pen-Lift Mechanism for High-Speed Plotting

by Tammy V. Herr and Hatem E. Mostafa

THE PEN-LIFT MECHANISM in the HP 7550A Plotter was designed to minimize manufacturing cost and to minimize the overall mass of the pen carriage assembly while meeting performance criteria of reducing cycle time (pen down and pen up) and providing variable writing forces for various pen types.

Mechanics

The pen-lift assembly (Fig. 1) consists largely of inexpensive injection-molded plastic parts. Every element of the vertically moving assembly attaches to a complex and highly critical part, the pen holder. The most severe operating condition imposed on this holder is during pen exchange, when several pounds of force are exerted on the pen pawl during sliding contact with the HP 7550A's 8-pen carousel. To supply the strength and lubricity necessary to survive pen exchange, the pen holder is molded of polycarbonate filled with 30% glass and 15% Teflon.™

Miniature radial ball bearings mounted on the pen holder constrain the assembly to the desired vertical motion. Dynamic modeling was performed to determine the optimal combination of bearing geometry and preload required to sustain the imposed loads while inducing no frictional forces greater than 3 gm.

Actuation for vertical travel and pen-down force is provided by a highly efficient linear motor. A coil-wound bobbin is electromagnetically translated over a pole cap and magnet column located inside a voice-coil cup. Energizing this coil with an electric current produces a vertical force proportional to the input current. An inexpensive insulation-displacement connector terminates the bobbin coil wire, eliminating a soldering operation. This magnetic assembly weighs only 40 grams and delivers 122 grams of force per root watt of power dissipation.

Because of the accumulation of tolerances, the distance between the pen nib and the platen surface can vary from 1.5 to 4 mm. Therefore, the geometry of the voice-coil cup is optimized for minimizing leakage flux, thus providing a constant force over the entire 4-mm working range of the pen-lift assembly. An optical encoder senses the vertical position of the pen-lift assembly to within 0.05 mm. The use of digital feedback eliminates the offset and drift problems inherent in traditional analog feedback systems.

Control

The pen-lift control system provides the minimum pen up/down cycle time while reducing pen impact momentum to maximize pen nib life. The control system's complexity is reduced and its reliability is greatly enhanced by incorporating the plotter's microprocessor into it. For any given control mode, the microprocessor can determine the position and velocity of the pen by reading an encoder register. Using the proper algorithm, the processor outputs two pulse-width-modulated signals to the pen-lift driver (see Fig. 2). The front end of the pen-lift driver performs a differential digital-to-analog conversion on the two control

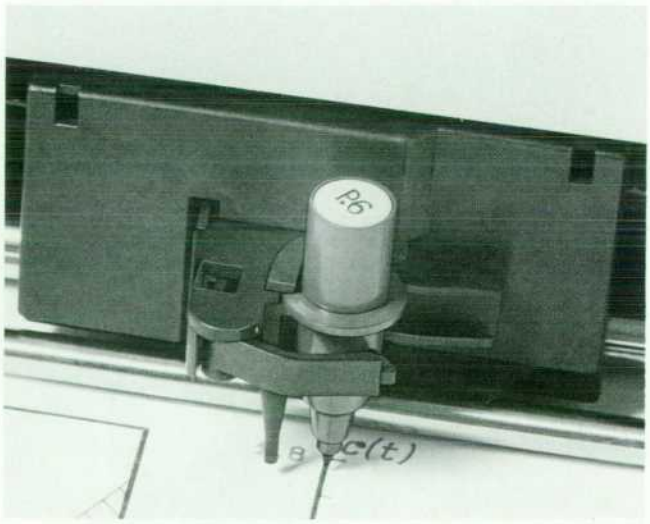


Fig. 1. *The pen-lift mechanism used in the HP 7550A Plotter is based on an electromagnetic voice-coil actuator and the use of the plotter's microprocessor to control pen drop velocity.*

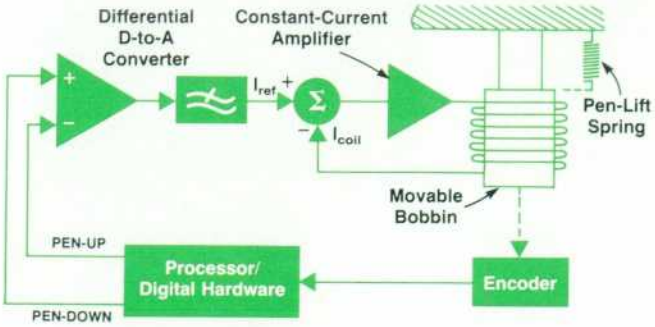


Fig. 2. *Block diagram of pen-lift control system.*

signals and the resulting single-ended analog signal is fed into a constant-current amplifier. The amplifier then drives the electromagnetic actuator appropriately.

The control system operates in four modes: pen down, fast drop, slow drop, and de-energized. In pen-down mode the system operates as a constant-force servo. That is, a constant force is applied to the pen nib against the plotting surface independent of vertical pen position. The writing force is chosen by the microprocessor from a set of eight values, depending on pen type. When a pen-up command is encountered in pen-down mode, the control system switches to a position servo and raises the pen 1.5 mm above the platen. The control system is now in fast-drop mode. The actual pen-up move requires no delay before lateral movement with the pen can begin. As long as lateral pen-up moves remain within a 2.5-cm radius from the location of the last pen-up command, the system continues to operate in fast-drop mode.

Because platen irregularities over a 2.5-cm lateral distance are considered to be minor, the pen height is considered to be known within a tight tolerance. Given a known pen height, the control system can execute a pen-down command very quickly. The pen-down move is accomplished in this case by switching the control system from a position to a velocity servo and then commanding the pen to descend at a high velocity. Slightly before impact, the control system significantly decreases the pen's downward velocity, thereby greatly reducing the impact momentum as the pen nib strikes the plotting media (see Fig. 3a). The final impact velocity is selected by the microprocessor as a function of pen type. This dual velocity approach makes it possible to lower the pen at a high speed, while independently selecting the optimum impact velocity for various pen and media combinations to reduce pen bounce and increase pen-nib life. The result is a pen-down delay of only 34 ms.

If, on the other hand, a lateral move greater than 2.5 cm occurs while the control system is in fast-drop mode, no assumptions about the distance of the pen from the platen can be made accurately enough. Therefore, the control system switches to slow-drop mode. When a pen-down command is executed in this mode, a slow velocity must be used during the entire pen descent until the pen contacts the platen. The pen-down delay in this mode can be as long as 60 ms (see Fig. 3b).

When a pen is picked from the 8-pen carousel, the pen-lift control system is in de-energized mode. In this mode, the mechanism is held at its topmost position by the pen-lift spring. It is in this initial state that the control system adaptively compensates for all offsets present in the system. These offsets include variations in the actuator force constant, pen-lift spring holding force and spring constant, and current driver offsets. The compensation is accomplished by using the constant-force servo to maintain the pen at an equilibrium position very near the platen. The force generated by the servo is exactly the amount needed to null all constant offsets in the system. A second force component that is proportional to pen position is also generated. This position-dependent force compensates for the effects of the pen-lift spring force constant. The overall offset nulling force is now added to all command forces generated in the different pen-lift operating modes. The elimination of any adjustment procedures on the manufacturing line makes the pen-lift mechanism a cost-effective, highly reliable system.

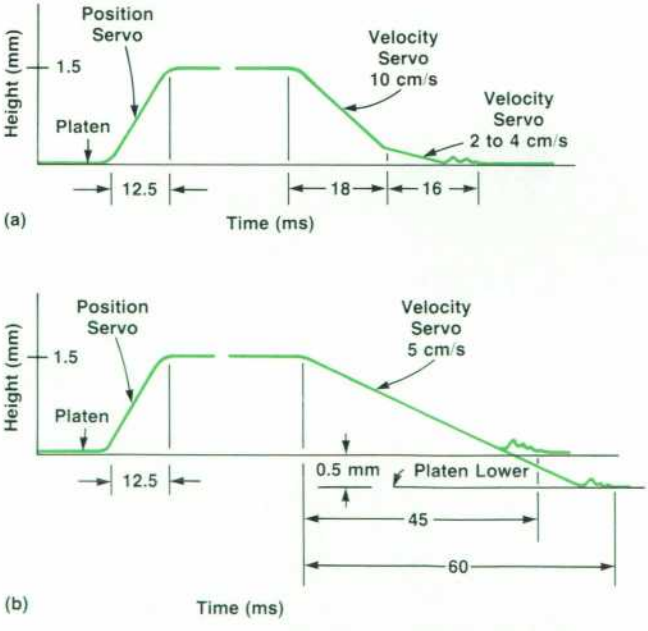


Fig. 3. *Pen height versus time for (a) fast-drop mode and (b) slow-drop mode.*

Acknowledgment

Special acknowledgment is extended to Chuong Ta for his excellent mechanical design contributions to the pen lift.

The HP 7550A X-Y Servo: State-of-the-Art Performance on a Budget

by David C. Tribolet, Kenneth A. Regas, and Thomas J. Halpenny

THE HP 7550A GRAPHICS PLOTTER features 6g acceleration along a vector, a maximum speed of 80 cm/s, repeatability of 0.1 mm with a given pen, and line quality comparable to the HP 7580 family of drafting plotters. At present, this represents the state of the art in plotter performance. The HP 7550A plotting mechanism uses two rare-earth magnet dc motors, each equipped with an optical encoder. Each motor drives one of two axes: the paper axis (X) or the pen axis (Y).

Both servo loops are closed in the HP 7550A's microprocessor using position and velocity feedback. Velocity feedback is provided not by a tachometer, but rather by using an estimate of the velocity derived from the encoder position information (Fig. 1).

The encoder positions for the X and Y axes are maintained in separate 8-bit registers. These 8-bit registers overflow every 256 counts (equal to a distance of 1.6 mm), but that is not a problem since the servo works with incremental encoder values. As long as the encoder register value changes by less than ±128 counts between samples, the servo can maintain its position with 8 bits. As it happens, the position changes only by a maximum of 38 counts between 300-microsecond samples, but 8 bits is a convenient size for the HP 7550A's microprocessor.

The servo motor control calculation during encoder sample n is:

$$M_n = (R_n - X_n) - [K_v/(K_pT)](X_n - X_{n-1}) \qquad (1)$$

The challenge is to convert this expression to "incremental" form, that is, to a function of $X_n - X_{n-1}$. To do this, the following definitions are necessary:

- The position error, where you want to be minus where you are, is defined to be $E_n = R_n - X_n$
- The "reference generator," which moves the reference R_n between encoder samples, computes increments in the reference which we call the reference velocity $V_n = R_n - R_{n-1}$.

Using these definitions, we have:

$$M_n = V_n + E_{n-1} - [1 + K_v/(K_pT)](X_n - X_{n-1}) \qquad (2)$$

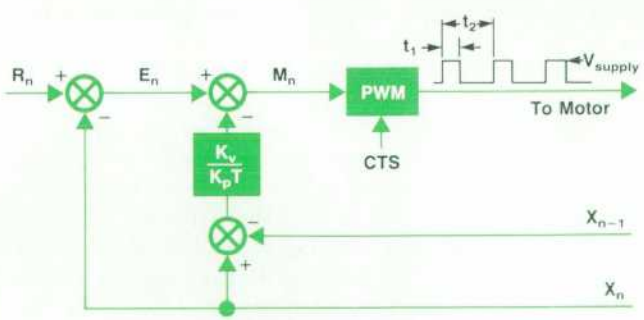
Note that each term on the righthand side of this equation is a small difference between two potentially large numbers, and hence amenable to 8-bit computations. Also note that the existence of position error E_n does not necessarily indicate failure to plot on the reference trajectory. The tracking servos are designed to lag the reference at any nonzero velocity. This lag is produced by velocity feedback in the control loop. By matching the dynamic response of the two servos, we ensure that position errors on the two axes are proportional to their respective reference velocities, placing the actual pen position on the reference trajectory (see Fig. 2).

The factor $1 + K_v/(K_pT)$ is a constant, so the multiplication of $X_n - X_{n-1}$ by this factor is implemented by a "hard-coded" multiply. For example, if $1 + K_v/(K_pT) = 8$, then the quantity $X_n - X_{n-1}$ is simply shifted left by 3 bits. The reference generator moves the X-axis and Y-axis references from one point to the next. The reference for each axis is accelerated to a maximum speed, maintained at that speed for a time, and finally decelerated near the endpoint. Since a straight line is always drawn from one point to the next, the ratio of Y-axis to X-axis reference velocities equals the slope of the line (see Fig. 3).

To conserve processor time, a new pair of X-axis and Y-axis reference velocities is computed once every four servo samples (1.2 ms), rather than every sample. The minimum addressable unit (one plotter unit, or P.U.) equals 0.025 mm (approximately 0.001 inch). Since there are exactly four encoder counts per P.U., the reference velocity is computed in P.U. per 1.2 ms, and the result V_n is sent to the servo (which expects reference increments in encoder counts) four times during the next four servo interrupts. This is a convenient way to convert from P.U. to encoder counts.

Curvy Servo Algorithm

The curved-line reference generator enables the HP



K_p = Position Gain (volts/count) = V_{supply}/CTS
K_v = Velocity Gain (volt-second/count)
X_n = Encoder Position at nth Interrupt (count)
R_n = Reference Position at nth Interrupt (count)
T = Servo Period (seconds)
E_n = Position Error at nth Interrupt (counts)
M_n = Motor Control at nth Interrupt (counts)
CTS = Counts to Saturation (counts)
t_1 = K×M_n
t_2 = K×CTS
K = 0.5 μs/count
V_{supply} = Unregulated Supply Voltage

Fig. 1. *HP 7550A servo diagram.*

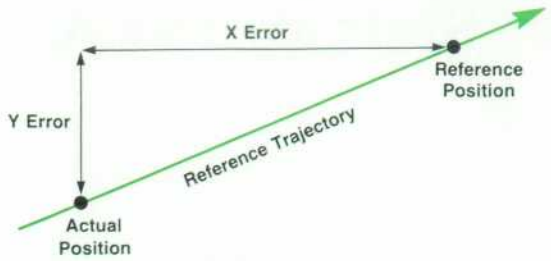


Fig. 2. *Matching the dynamic response of the two servos places the actual pen position on the reference trajectory.*

7550A to maximize line quality by drawing continuous curves without stopping at intermediate points. All curves are drawn as a sequence of short line-segment vectors, each having a slope slightly different from the previous one. Most plotters begin and end a vector at rest, with a reference velocity equal to zero. This is the easiest to implement because the reference generator needs to have no knowledge of previous or future vectors in a sequence. However, the HP 7550A's curved-line generator looks into the future by collecting a group of vectors into a first-in, first-out queue called the vector buffer. It usually takes longer to collect the vectors of a curve than it takes to plot them, so collecting vectors early before plotting prevents loss of throughput. A collection of vectors is released for plotting when either a pen-up command is received, the vector buffer becomes filled, or a certain amount of time has elapsed since the last vector was received by the vector buffer while the previous vector is plotting.

Fig. 4 shows how collected vectors become active. The vector buffer has a head pointer, from which vector information is taken to draw lines. It also has an active tail pointer and a virtual tail pointer. Vectors are added to the buffer at the virtual tail pointer. The vectors between the head and active tail pointers are those currently being plotted, while those between the active tail and virtual tail pointers are the vectors being collected. Collected vectors are released to be plotted simply by changing the active tail pointer to equal the virtual tail pointer.

Referring to Fig. 5, as the pen nears the end of vector 1 at point P, it slows to a maximum turning speed, which depends on the turning angle A. The smaller the turning angle, the larger the maximum turning speed can be. If the turning angle is large, then the turning speed reduces to zero. The actual turning speed also depends on the length of succeeding vectors. For example, suppose that a curve only has two vectors, the turning angle is 0 degrees, and the length of vector 2 is very small, say one plotter unit (see Fig. 6). Then the actual turning speed between vectors 1 and 2 is almost zero, since the plotter must stop at the end of vector 2 anyway.

When the curved-line generator is activated, it controls all vectors generated internally by the HP 7550A, as well as the vectors generated externally by the user. The plotter therefore performs the same curving action whether a circle is generated internally with the HP-GL circle instruction CI, or externally with the user computing each of the chord segments and sending them to the plotter.

The curved-line generator is one of two software-selectable reference generators. It has a fixed acceleration of 3.5g along the longer axis of a vector, while the conventional reference generator allows from 1 to 6g acceleration along the vector.

Vector Buffer

The vector buffer can also be used to increase plotting throughput for both reference generators. There is a critical vector length, approximately 100 P.U., below which the HP 7550A takes longer to prepare the vector for plotting than it actually takes to plot it. Without the vector buffer, the pen must sit idle for a time while the controller sends the vector to the plotter. Most plots have a mix of long and short vectors and pen-lift operations. With the vector buffer, the HP 7550A is able to prepare several vectors ahead of time while it is plotting a long vector or doing a pen lift so that, when the short vectors come along, there will be much less idle plotting time. Hence, throughput is significantly enhanced.

Cost-saving Strategies

To extract the best possible performance from the X and Y servos at minimum cost, several strategies are used. First, design solutions from existing product lines were borrowed for the HP 7550A, saving engineering manpower for the task of optimizing these technologies. The dc servo motor used in the HP 7580 family of drafting plotters is unsurpassed in the marketplace for performance at a low price, so we decided to build our machine around it, matching mechanism and drive electronics to its capabilities. Particular attention was paid to minimizing drive inertia and to optimizing motor speed reduction in the light of compet-

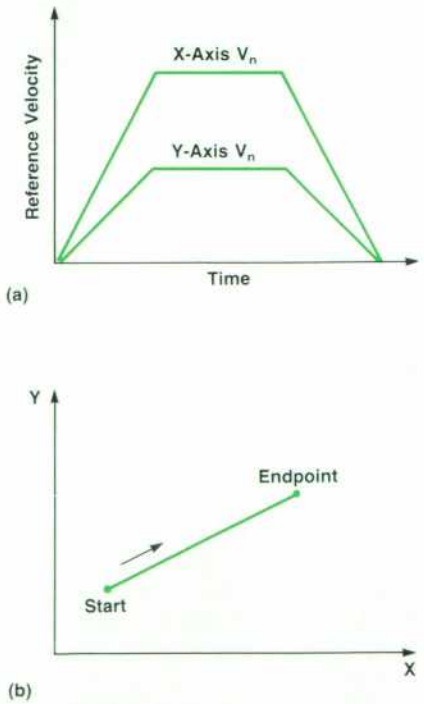


Fig. 3. *(a) Reference velocities versus time for the X and Y axes and (b) the corresponding plot of X versus Y with a slope = ½.*

ing concerns. Increasing the drive ratio improves encoder resolution and improves servo robustness by making motor inertia, which doesn't vary, dominant compared to load inertia, which does. On the other hand, the efficiency of power transfer from motor to load decreases with increased drive ratio, at least in the neighborhood of the HP 7550A's design parameters. In the final design, the load inertia reflected to the motor is approximately 35% of the total inertia and the encoder resolution is 4 counts per P.U. (1 P.U. = 0.025 mm).

Mounted on each motor is a 500-line optical encoder leveraged from another successful plotter line—the HP 7470 family of personal plotters.[1] Also leveraged from the HP 7470 family is the idea of driving the pen carriage with a timing belt. Converting rotary to linear motion via a timing belt has proven to be cheap, easy to assemble, reliable, nearly backlash-free, and—with aramid-fiber reinforced belts—quite rigid. And, of course, the paper moving technology introduced by HP with the HP 7580A[2] is continued in the HP 7550A.

Another key design strategy was to minimize the number of mechanical and electrical parts, maximizing the functionality of each. Thus all servo digital electronics, equivalent to dozens of off-the-shelf ICs, are integrated into a single VLSI package, saving part cost, board space, power consumption, and assembly cost. Similarly, two highly complex injection-molded plastic parts form the mechanical skeleton of the machine, providing not only the structural rigidity necessary to support 6g accelerations, but also the writing surface, the vacuum plenum for paper hold-down, many attachment points for other components, and even an electrical grounding path for protection against static discharge.

We also sought to minimize the number of adjustments made during assembly of the machine. Speed reduction between motor and output drive, for example, is done with spring-tensioned timing belts instead of gears, saving a tricky backlash adjustment. Timing belt drives are also quieter and less expensive. Closing the servo loop in the microprocessor rather than through analog hardware not only eliminates expensive power-hungry components that are not easily integrated into compact circuits, but also eliminates the potentiometer adjustments generally associated with analog servo circuitry.

Probably the most powerful strategy employed to keep cost down and performance up was taking full advantage of the machine's intelligence, the microprocessor. (The 68000 is the brain inside some of today's more advanced personal computers.) For example, the gain of each pulse-width-modulation (PWM) motor drive amplifier is proportional to the voltage supplied to it. Rather than install expensive circuitry to regulate this voltage, we allow it to vary. The microprocessor periodically senses this voltage (via inexpensive PWM-style circuitry) and adjusts input to the drivers accordingly.

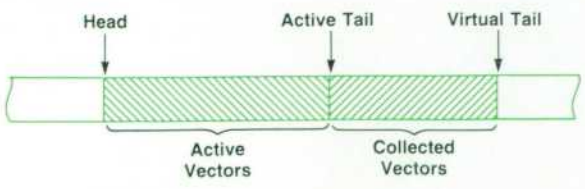


Fig. 4. *The HP 7550A's curved-line generator uses a FIFO buffer to collect data describing vectors before they are plotted. Pointers shown are used to indicate vectors being plotted.*

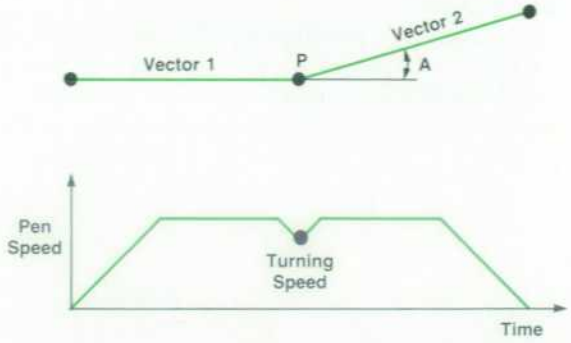


Fig. 5. *The turning speed at the junction of two successive vectors is an inverse function of the turning angle A.*

Another variation for which the microprocessor provides compensation is in the motors themselves. Because of manufacturing tolerances, dc motor gain may vary as much as 25% from nominal. Inasmuch as dynamic matching of the axes is a key to good line quality, mismatched X and Y motors could produce unsatisfactory plots. To head off this potential problem, the plotter's firmware includes a self-calibration procedure, performed in the factory. During a series of programmed moves, the performance of the two servos is analyzed by a special algorithm and the result used to adjust forward-loop gain K_p on each axis. This adjustment is stored in nonvolatile memory.

Because the HP 7550A presses motor performance to its limits, we have observed that some "pathological" plots (generally with certain types of solid area fill) can cause the motors to overheat. Rather than derate the machine for all plots—making all users pay for the needs of a few—we again resort to firmware. During plotting, the microprocessor continuously monitors the power demanded of each motor. Whenever either motor has more demanded of it than can be sustained under worst-case conditions, the nominal acceleration of the plotter is reduced to 3g until that motor has a chance to cool down.

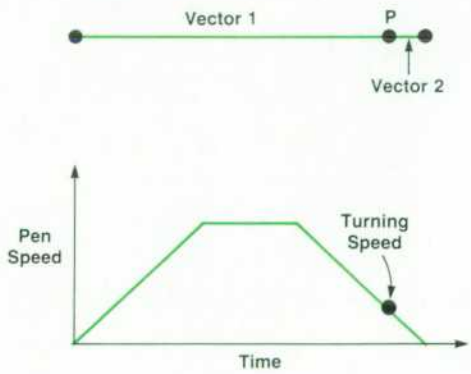


Fig. 6. *The turning speed at the junction of two successive vectors is also a direct function of the length of the second vector.*

Acknowledgments

The successful development of the HP 7550A servo was a team effort. The authors would like to thank Kevin Bockman, David Ellement, Tammy Herr, Peter Ma, Randy Coverstone, and Mark Majette for their numerous contributions.

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Firmware Provides Simple and Powerful Plotter Operation

by Thomas J. Halpenny

AN ESSENTIAL INGREDIENT in the success of the HP 7550A Graphics Plotter design was shifting as much complexity as possible from the electronic hardware to the microprocessor firmware. A 68000 microprocessor, running at 6 MHz, was chosen to accomplish the objectives. This choice centered on the following:

- The instruction set allows compatibility with the HP-GL firmware of the HP 7580 family of drafting plotters, and provides a growth path for future plotters.
- The processor is fast enough to perform the X-axis and Y-axis servo computations every 300 microseconds, and the pen-axis servo computation every 600 microseconds.
- It has multiple interrupt capability with no additional electronics. The system has a 300-microsecond time base interrupt, a serial I/O interrupt, and an HP-IB I/O interrupt capability.
- The 68000 has a large linear address space to simplify electronics and firmware.

Front Panel

The HP 7550A front-panel controls and indicators are designed to be simpler, friendlier, and more flexible than

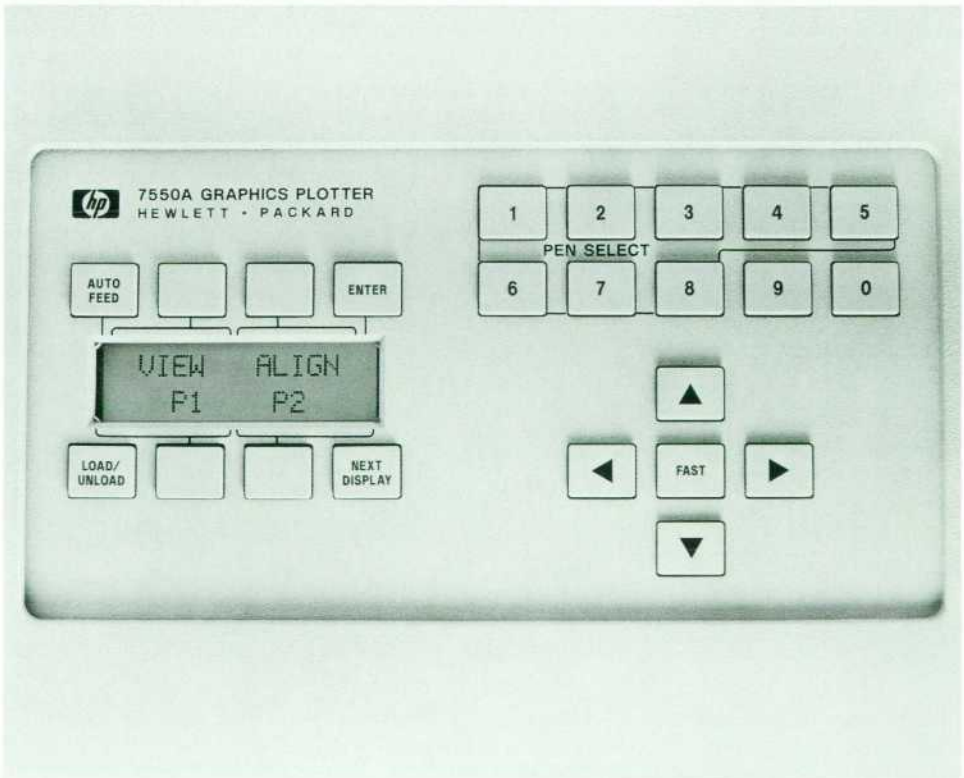

Fig. 1. *Front-panel layout of the HP 7550A Graphics Plotter.*

those of earlier plotters. Early HP plotters had several pushbuttons and LED indicators to perform setup functions and display status. As these plotters evolved, more functions were added to the front panel in the form of more pushbuttons and LEDs. Many users told us that the front panel was getting to be too imposing. Too many pushbuttons and LEDs made it difficult to separate the most often used functions from those that were seldom used. At the same time, the early plotters had a rear panel with an ever-growing bank of configuration switches used primarily to establish the HP-IB or RS-232-C interface configuration with the host computer.

The HP 7550A has a simple layout of three groups of front-panel controls (Fig. 1). The numbered keys are used for manual selection of pens and the number of copies to be plotted. The cursor keys are used to position the pen. The keys that surround a two-line-by-16-alphanumeric-character liquid-crystal display perform all the rest of the functions. The rear-panel switches of previous plotters are entirely replaced by this last group of keys and the display, along with an EAROM (electrically alterable read-only memory) to maintain the configuration in nonvolatile memory. Four of the keys are unlabeled. These softkeys are used with the display and the **NEXT DISPLAY** key to access a menu structure of up to four softkey functions per display.

The result of this layout is a structure in which the most often used functions are the easiest to access, while the seldom used configuration functions are hidden. The paper loading functions have dedicated keys because the user needs these functions often.

The HP 7550A has a dual I/O capability. Either HP-IB or RS-232-C interfaces can be used to communicate with the host computer. The firmware automatically senses which interface is used to communicate with the plotter. This interface is enabled and the other one is shut down. The plotter thus frees the user from having to worry about one more configuration switch. The plotter also automatically senses paper size, a function that required a configuration switch on an earlier plotter.

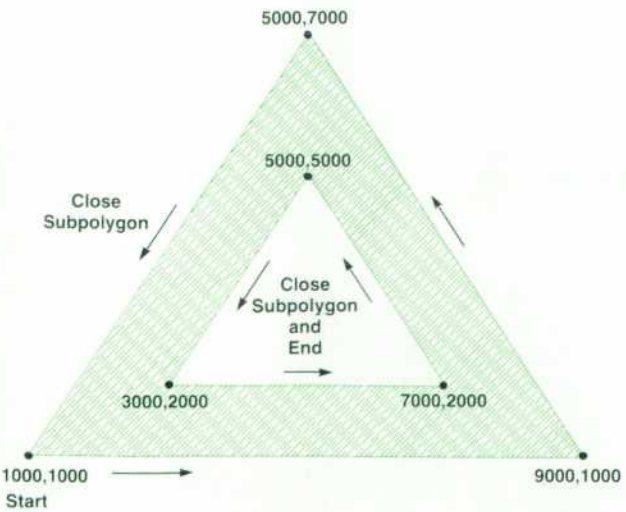

Fig. 2. *Example of polygon generation and area fill as performed by the HP 7550A. See text for associated HP-GL commands.*

The liquid-crystal display also enables the HP 7550A to communicate plotter status to the user much better than before. If the plotter requires operator attention, the display can supply the required message in English. The display is also available to the host computer for display of messages and is used to make internal factory self-tests more versatile than before, at no extra cost.

Firmware Enhancements

Most of the major firmware enhancements of the HP 7550A are centered on the existence of 12,800 bytes of RAM in the plotter. This is called graphics memory and is divided among the following five graphics buffers:

- HP-GL instruction input buffer
- Polygon area fill and edging buffer
- Downloadable character set buffer
- Replot buffer
- Vector buffer.

Each of these subsystems is initially assigned a reasonable amount of memory that will enable it to operate properly under most plotting conditions. The user can change the allocations, however, to increase the memory allocated to a particular buffer, at the expense of other buffers which might not be used at all.

The HP-GL instruction input buffer accepts all graphics instructions from a host computer and holds them until the plotter is ready to execute them. This buffer has been resident in most earlier HP plotters, but until now had always been a fixed size.

The polygon area fill and edging buffer holds polygon vertex and line intersection information to enable the plotter to edge and fill a polygon with a large variety of fill patterns automatically. The vertices of the polygon are sent to the plotter using the same instructions as the computer would use to send vector information to plot. This is accomplished by placing the plotter into polygon mode, sending the vertices, and then returning the plotter to vector mode. At this time the host computer can send instructions to fill and edge the polygon. This scheme allows the host computer to use the same scaling operations for polygons as it does for regular vector information.

The following example illustrates how the host computer can use simple HP-GL instructions to define and fill a polygon. An HP-GL instruction consists of a two-letter mnemonic to specify the operation, followed by a number of parameters, and ending with a semicolon. Table I lists and defines the HP-GL instructions used below.

The following set of HP-GL instructions will generate the simple polygon shown in Fig. 2:

```
PU; PA 1000,1000;
PM 0;
PD; PA 9000,1000, 5000,7000, 1000,1000;
PM 1;
PA 3000,2000, 7000,2000, 5000,5000, 3000,2000;
PM 2;
LT 4; FT 3,50,45; FP; LT; EP;
```

Notice that this figure has a "hole" in it. This is made possible by using the PM 1; instruction to define the polygon as a number of subpolygons. Whenever the user does

Table I

HP-GL Mnemonic	Action
PU;	Pen up (raise the pen)
PD;	Pen down (lower the pen)
PA X,Y;	Plot absolute (move to coordinates X,Y)
LT 4;	Line type (dashed line pattern 4)
LT;	Line type (solid line pattern)
PM 0;	Polygon mode 0 (clears polygon buffer and enters definition mode)
PM 1;	Polygon mode 1 (closes current subpolygon, i.e., allows holes)
PM 2;	Polygon mode 2 (closes current subpolygon and ends definition mode)
FT P,S,A;	Fill type (pattern P, line spacing is S plotter units, and line angle is A degrees)
FP;	Fill polygon interior with fill type
EP;	Edge polygon with line type

this, the currently defined subpolygon is closed, and a final vertex is added to the subpolygon to return to the starting coordinates of the subpolygon definition. The HP-GL instructions for this example include the closing endpoints of each of the two subpolygons, but these were unnecessary.

The DL (downloadable character) instruction allows a user to design characters and save them in the downloadable character set buffer for convenient repeated use in labeling instructions. A character is defined by sending to the plotter its ASCII character code, followed by a sequence of pen-up, pen-down, and X-Y coordinate instructions that one would use to draw the character on the character generator's primitive grid coordinate system. The resulting characters can then be manipulated with the same size, direction, slant, and positioning transformations that can be used with the resident character sets. Up to 94 separate characters can be specified, each associated with a unique ASCII printing character.

The replot buffer is capable of holding an entire plot's worth of HP-GL instructions, depending on the length of the plot. The host computer can then command the HP 7550A to make up to 99 copies of the saved plot without having to retransmit the data. The sheet feeder automatically changes pages between plots. The following HP-GL instruction sequence is used:

BF;	Buffer plot (clear replot buffer and begin storing data)
RP 5;	Replot (make 5 copies of the saved plot)

The BF and RP functions can also be activated using the front panel, in case the user does not have access to the host computer's data stream. This allows a user to capture a plot and make several copies manually.

The HP-GL graphics instructions are stored in a compacted format to maximize data storage capacity. This function is best used in conjunction with other advanced HP-GL instructions. For example, if the host computer uses the plotter's character generator, then only one byte of storage is required for each character drawn. However, if the computer uses PA instructions to draw each stroke of a character individually, then at least four bytes are required for each vector drawn.

The vector buffer is used to hold primitive vector and pen-lift information. It is used by the curved line generator to collect curves, and it helps to increase plotting throughput. This buffer is described in more detail in the servo article on page 31.

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