These pages removed as part of manual update from Rev 4 → 5 as instructed on update sheet.

R.C.

SECTION 4 — CALIBRATION

SECTION 4 - CALIBRATION

4-1 GENERAL

This section contains calibration procedures for the following assemblies and systems:

These procedures should be performed as a result of one or more of the following conditions:

1. If, during the course of normal operation, the FM/AM-1500 or any major function thereof fails to meet the performance specifications as provided in "SECTION 3 - PERFORMANCE EVALUATION".

2. If a module is found to be defective and requires replacement (see Table 4-1, MODULE REPLACEMENT & CALIBRATIOM REQUIREMENTS).

3. If the recommended 12 month calibration interval is due.

4-1-1 SAFETY PRECAUTIONS

As with any piece of electronic equipment, extreme caution should be taken when working on "live" circuits. Certain circuits and/or components within the FM/AM-1500 contain extremely high voltage potentials, CAPABLE OF CAUSING SERIOUS BODILY INJURY OR DEATH (see following WARNINGS)! When performing the calibration procedures in this section be sure to observe the following precautions:

WARNING

THE OSCILLOSCOPE CONTROL AND DEFLECTION PC BOARD AND THE CRT CARRY A VOLTAGE POTENTIAL OF MORE THAN 2000 VDC WHEN THE FM/AM-1500 IS ENERGIZED. DO NOT CONTACT THESE OR ANY ASSOCIATED COMPONENTS DURING TROUBLE-SHOOTING.

WHEN WORKING WITH "LIVE" CIRCUITS OF HIGH POTENTIAL, KEEP ONE HAND IN POCKET OR BEHIND BACK, TO AVOID SERI-OUS SHOCK HAZARD.

REMOVE ALL JEWELRY OR OTHER COSMETIC APPAREL BEFORE PERFORMING ANY CALIBRATION PROCEDURES INVOLVING LIVE CIRCUITS.

USE ONLY INSULATED TROUBLESHOOTING TOOLS WHEN WORKING WITH LIVE CIRCUITS.

FOR ADDED INSULATION, PLACE A RUBBER BENCH MAT UNDER-NEATH ALL POWERED BENCH EQUIPMENT, AND A RUBBER FLOOR MAT UNDERNEATH THE TECHNICIAN'S CHAIR.

HEED ALL WARNINGS AND CAUTIONS CONCERNING MAXIMUM VOLTAGES AND POWER INPUTS.

4-1-2 CALIBRATION EQUIPMENT REQUIREMENTS

Appendix E at the rear of this manual contains a comprehensive list of test equipment suitable for performing any of the procedures listed in this manual. Any other equipment meeting the specifica-tions listed in Appendix E may be substituted in place of the recom-mended models.

NOTE

For certain procedures in this manual, the equip-ment listed in Appendix E may exceed the minimum required specifications; for this reason, minimum use specifications appear with all calibration procedures, where accessory test equipment is required.

4-1-3 DISASSEMBLY REQUIREMENTS

To perform any of the calibration procedures contained in this sec-tion, the exterior case must be removed from the FM/AM-1500. Refer to "SECTION 6 - MECHANICAL ASSEMBLIES/PC BOARDS" for illustrations of case removal or, if required, module disassembly. In the proce-dures, numbers in parentheses following any adjustable port refers to the designator assigned in Figures 3-1 and 3-2 of this Manual or the Reference Designator assigned to the component on that Assembly or Schematic (see Sections 6 and 7 of this manual).

IF THIS MODULE IS REPAIRED OR REPLACED / THEN THE FOLLOWING CALIBRATION PROCEDURES MUST BE PERFORMED	PRELIMINARY	POWER SUPPLY	FREQUENCY STANDARD	FREQUENCY SYNTHESIS		RECEIVE					GENERATE			SPECTRUM ANALYZER	MICROPROCESSOR
				HIGH LOOP	LOW LOOP	RECEIVE SIGNAL	O' SCOPE	FREQUENY ERROR	MODULATION	INPUT/OUTPUT POWER	RF POWER	DUPLEX OFFSET	DUAL TONE GENERATOR		
CLOCK DIVIDER	●		●												
CPU / MEMORY PC BD	●			●											
DELAY LINE	●			●											
DEMOD AUDIO PC BD.	●	●				●		●	●	●	●				
DIODE SWITCH	●														
DUAL TONE GENERATOR PC BD	●												●		
DUAL VCO	●			●		●					●				
DUPLEX OFFSET	●											●			
FM GENERATOR	●								●		●				
GENERATE MIXER	●										●			●	
HIGH LOOP	●			●											
HIGH / LOW PASS FILTER	●			●											
I/O INTERFACE PC BD.	●					●					●				
LCD / KEYBOARD	●														
LOW PASS FILTER	●			●											
LOW LOOP	●				●										
LOW LOOP MIXER	●				●										
OSC. CONT. + DEFL. PC BD.	●						●		●						
OUTPUT AMP	●										●				
BUFFER AMP A or B	●			●											
POWER SUPPLY	●	●													
POWER TERMINATION	●										●				
SPECTRUM ANALYZER L.O.	●													●	
SPECTRUM ANALYZER I.F.	●													●	
SPECTRUM ANALYZER R.F.	●													●	
40 V POWER SUPPLY	●	●													
89-90 MHz RECEIVER	●					●									
1300 MHz I.F. GENERATOR	●										●				
1300 MHz I.F. RECEIVER	●					●									

Table 4-1 Module Replacement and Calibration Requirements

4-2 PRELIMINARY CALIBRATION

SPECIAL ACCESSORY EQUIPMENT REQ'D: 1 Small Slotted Screwdriver
1 Ohmmeter—Any

FIGURE REFERENCES: None

TEST SET-UP DIAGRAM: N/A

STEP PROCEDURE

1. Set FM/AM-1500 in the position in which it will be operating, to allow the meters to be zeroed.

NOTE

The meter must be zeroed after the unit is placed in the position it will be operating.

2. Set PWR/OFF/BATT Switch (13) to "OFF".

3. Adjust MODULATION Meter Mechanical Zero Adjustment (2) for an indication as close as possible to "0" on MODULATION Meter: (1). Gently tap on Meter faceplate to ensure that the needle is not sticking and that it settles to "0".

4. Adjust FREQ ERROR Mechanical Zero Adjustment (40) for an indication as close as possible to "0" on FREQ ERROR Meter (41). Gently tap on Meter faceplate to ensure that the needle is not sticking and that it settles to "0".

5. Check all knobs on front panel for the following:

   a. Correct alignment to front panel.

   b. Correct range stops.

   c. Knobs are securely tightened to control shafts.

   d. Knobs are close to front panel, but do not bind.

6. Test resistance on Power Supply as follows:

Pin # of J6003	Function	Minimum Resistance
7	-12 V	200Ω
4 or 5	+5 V	155Ω
1	+12 V	42Ω

NOTE

Ground positive (+) lead of Ohmmeter for positive voltage test points. Ground negative (-) lead of Ohmmeter for negative voltage test points.

4-3 POWER SUPPLY CALIBRATION

SPECIAL ACCESSORY EQUIPMENT REQ'D:
- 1 Small Slotted Screwdriver
- 1 DC Voltmeter – Any
- 1 DC Power Supply – Variable from +10.9 V to +12 V

FIGURE REFERENCES:
- Rear Panel/Power Supply Module (Figure 6-8)
- Demod Audio PC Board (Figure 6-25)

TEST SET-UP DIAGRAM: N/A

WARNING

THE DIFFERENCE IN POTENTIAL BETWEEN THE FLOATING GROUND AND CIRCUIT OR CHASSIS GROUND CAN EXCEED 300 VOLTS PEAK. THIS POTENTIAL CAN CAUSE SERIOUS INJURY OR EVEN DEATH. ALWAYS USE AN ISOLATION TRANSFORMER AND TAKE EXTREME CARE WHEN WORKING INSIDE THE POWER SUPPLY MODULE.

NOTE

FM/AM-1500 Serial Numbers 1005 thru 1425 contain DEMOD AUDIO PC Board 7010-5034-700. FM/AM-1500 Serial Numbers 1426 thru 2817 contain DEMOD AUDIO PC Board 7010-5037-300. FM/AM-1500 Serial Numbers 2818 and on contain DEMOD AUDIO PC Board 7010-5038-900. All adjustments and test points referenced in the following calibration procedure are for the 7010-5037-300 and 7010-5038-900 PC Boards only. For adjustments and test points on 7010-5034-700 PC Boards, see FM/AM-1500 Maintenance Manual Rev. 0 thru Rev. 3.

STEP	PROCEDURE
1.	Connect AC line cord to FM/AM-1500.
2.	Set PWR/OFF/BATT Switch (13) to "PWR".
3.	Measure 16 VDC output at FL6002 on Power Supply. Verify voltage is +16 VDC (±0.5 V). If not, adjust R5741 on Power Supply PC Board #1 for correct voltage.
4.	Set PWR/OFF/BATT Switch (13) to "OFF".

STEP	PROCEDURE

5. Disconnect battery plug J6005.

NOTE

Thru Serial Number 2134 (without cooling fan), both J6005 and J6004 must be disconnected.

6. Connect Battery Load Simulator to J6005.

7. Set PWR/OFF/BATT Switch (13) to "PWR".

8. Adjust load control on Battery Load Simulator for load of 0.3 Amps. Verify voltage on Battery Load Simulator is +14.5 VDC. If not, adjust R5706 on Power Supply PC Board #1 for correct voltage.

9. Depress BATT TEST Button (14) and verify that top scale on the MODULATION Meter (1) reads the same as the battery voltage in Step 8. If not, adjust R4887 on the DEMOD AUDIO PC Board.

NOTE

Use an extender card to make adjustment or remove CPU/MEMORY PC Board and use extender ribbon cable.

10. Adjust load on Battery Load Simulator for load of 1.3 (±0.3) Amps. Verify voltage on Battery Load Simulator is 5 VDC (±2 V). If not, repeat Step 8.

11. Set PWR/OFF/BATT Switch (13) to "OFF".

12. Disconnect Battery Load Simulator from J6005.

13. Set PWR/OFF/BATT Switch (13) to "OFF".

14. Connect Voltmeter between FL6005 and chassis ground. Verify voltage indication is +12 VDC (±0.5 V). If out of tolerance adjust R4851.

15. Connect Voltmeter between FL6006 and chassis ground. Verify voltage indication is +5.075 VDC (±0.225 V). If out of tolerance, return to Step 4.

16. Connect Voltmeter between FL6007 and chassis ground. Verify voltage indication is -12 VDC (±0.5 V). If out of tolerance, return to Step 4.

17. Use a Voltmeter to measure the output of the 40 V Power Supply at pin 3 of P5601. Verify voltage is +40.5 VDC (±4.5 V).

18. Set PWR/OFF/BATT Switch (13) to "OFF".

19. Connect an external +12 VDC Power Supply to Battery Plug J6005

20. Set PWR/OFF/Batt switch (13) to "BATT".

STEP	PROCEDURE
21.	Reduce external Power Supply to 10.9 VDC. Verify FM/AM-1500 shuts off at input of 10.9 VDC. If not, adjust R4919 on DEMOD AUDIO PC Board.
22.	Adjust external Power Supply to +12 VDC.
23.	Set PWR/OFF/BATT Switch (13) to "OFF" and then back to "BATT". Verify that FM/AM-1500 shuts off in 7 to 11 minutes.

4-4 FREQUENCY STANDARD CALIBRATION

SPECIAL ACCESSORY EQUIPMENT REQ'D:
- 1 Frequency Counter – Capable of reading 10 MHz
- 1 10 MHz Standard – Amplitude of 2 Vp-p
- 1 Oscilloscope – Capable of 10 MHz

FIGURE REFERENCES: Oven Oscillator Assembly (Figure 6-12)

TEST SET-UP DIAGRAM: N/A

STEP PROCEDURE

1. Set PWR/OFF/Batt switch to "PWR".
2. Connect external Frequency Counter to 10 MHz REF Connector (62) on rear of FM/AM-1500.
3. Adjust INT REF CAL Adjustment (17) CW and CCW while observing Frequency Counter. Verify a frequency range of at least 3 Hz (±2 Hz). If out of tolerance, adjust the screw for the oven oscillator to correct frequency range and leave the frequency centered at 10 MHz.

NOTE

If the optional Oven Oscillator is installed, the variable frequency will be approximately 3 Hz.

4. Observe Frequency Counter and adjust INT REF CAL Adjustment (17) for a reading of 10 MHz (±2 Hz).
5. Using external Oscilloscope, connect a 10 MHz Standard (WWV is suggested) to external input of Oscilloscope and connect a coax cable between Channel A of Oscilloscope and 10 MHz REF Connector (62) on FM/AM-1500.
6. Adjust INT REF CAL Adjustment (17) on FM/AM-1500 until displayed signal on Oscilloscope "stops".
7. Connect an external 10 MHz Standard, with amplitude of 2 Vp-p or greater, to 10 MHz REF Connector (62). Verify EXT REF Indicator (14) illuminates.
8. Disconnect all test equipment from FM/AM-1500.

4-5 FREQUENCY SYNTHESIS FUNCTIONAL BLOCK

4-5-1 HIGH LOOP CALIBRATION

SPECIAL ACCESSORY EQUIPMENT REQ'D:	1 Frequency Counter – Capable of reading 1210 MHz
	1 Spectrum Analyzer – Capable of measuring 1210 MHz
	1 TF-30, Tune Fixture – See Appendix D
	1 Digital Multimeter – Any
	1 Oscilloscope – Any
FIGURE REFERENCES:	FM/AM-1500 Interconnect (Figure 7-1)
	High Loop #1 and #2 Schematics (Figures 7-12 and 7-13))
	High Loop PC Boards #1 and #2 (Figure 6-13)
	Dual VCO Mechanical Assembly (Figure 6-14)
TEST SET-UP DIAGRAM:	N/A

STEP PROCEDURE

1. Place FM/AM-1500 in upright position.
2. Remove two screws securing HIGH LOOP Module in module rack and pull module out, then reconnect all connectors.

CAUTION

BE CAREFUL TO INSULATE EXPOSED PC BOARDS FROM POSSIBLE SHORT-CIRCUITING.

3. Rotate ANALY DISPR Control (38) to "1 M".
4. Disconnect coax cables P601 and P602 from J601 and J602 on the HIGH/LOW PASS FILTER Module and connect P601 to P602 using a SMB to SMB connector.
5. Disconnect P3004 from DELAY LINE Module output at J3004. Disconnect P2403 from J2403 on DUAL VCO.
6. Using an SMB to SMB tee, connect an external Frequency Counter to the 1210 MHz output (J2402) of the DUAL VCO Module.
7. Set PWR/OFF/BATT Switch (13) to "PWR".

8. Adjust C2003 on DUAL VCO for an indicated frequency of 1210 MHz (±1 MHz).

9. Disconnect Frequency Counter.

10. Using an external Spectrum Analyzer, measure the RF level of the 1210 MHz LO at J2402 and at J2401 on the DUAL VCO. Verify both RF levels are +5 to +12 dBm.

11. Disconnect Spectrum Analyzer and connect P2402 to J2402 and P2401 to J2401.

12. Using an external Spectrum Analyzer, measure the RF level at the output of OUTPUT BUFFER B, J6902B. Verify RF level is +5 to +12 dBm at 1210 MHz.

13. Disconnect Spectrum Analyzer and reconnect P6902B to J6902B.

14. Use Keyboard (20 to select 299.0000 MHz on LCD (21) FREQUENCY Readout.

15. Disconnect P2806 from J2806 on HIGH LOOP Module.

16. Connect TF-30 to P2406 on Dual VCO and DVM to BNC connector on TF-30 as illustrated in Figure 4-1.

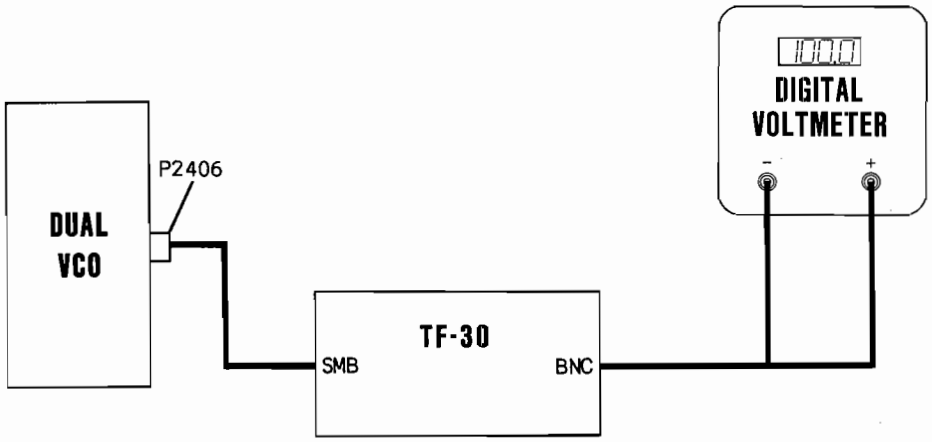

Figure 4-1 TF-30 Tune Fixture Hook-Up

17. Using an external Frequency Counter and an SMB Tee connector, measure the input frequency at J3005 on DELAY LINE Module.

18. Counter as listed below. Record voltage readings of DVM at listed frequencies.

    a. 50 MHz = _____ Volts

    b. 1120 MHz = _____ Volts

STEP	PROCEDURE

19. Adjust TF-30 for a displayed frequency on external Frequency Counter of greater than 390 MHz.

20. Disconnect DVM from TF-30 and connect DVM to center contact of J2806 on HIGH LOOP Module. Adjust R2373 (LOW LIMIT) on HIGH LOOP PC Board #2 for the same voltage as recorded in Step 18a.

21. Adjust TF-30 for a displayed frequency on external Frequency Counter of less than 380 MHz. Adjust R2372 (HIGH LIMIT) on HIGH LOOP PC Board #2 for the same voltage as recorded in Step 18b.

22. Disconnect TF-30 from P2406 on Dual VCO and connect P2806 to J2806 on HIGH LOOP Module. Connect P2403 to J2403 on Dual VCO. Verify that Freq LOCK Indicator (43) on front panel of FM/AM-1500 is illuminated, indicating phase-lock. If not, adjust R2341 (GAIN) on HIGH LOOP PC Board #2 until phase-lock is achieved.

NOTE

The logic for control of the Freq LOCK Indicator is on the DEMOD AUDIO PC Board, as explained in Section 2 of this Manual. If adjusting R2341 does not give desired results, the HIGH LOOP Module is not necessarily faulty.

23. Using Keyboard (20) select RF 050.0000 MHz on LCD (21)FREQUENCY Readout. Rotate ANALY DISPR Control (38) to "10 K".

24. Disconnect external Frequency Counter and connect external Spectrum Analyzer in its place.

25. While observing external Spectrum Analyzer, adjust R2341 (GAIN) on HIGH LOOP PC Board #2 for a flat RF noise floor on each side of 140 MHz display. Note and record level of noise floor (The noise should be flat approximately 20-60 kHz from the center of the band, @ 50 dBc).

26. Using Keyboard (20) select RF 999.0000 MHz on LCD (21) FREQUENCY Readout.

27. Rotate ANALY DISPR Control (38) to "500 K".

28. Observe displayed signal on external Spectrum Analyzer at about 1090 MHz. Adjust R2308 (NULL) on HIGH LOOP PC Board #2 for lowest possible RF levels on 500 kHz and 1 MHz sidebands.

29. Observe displayed signal on external Spectrum Analyzer for the selected frequencies. Verify noise floor level rises no more than 5 dB (±1 dB) above floor level noted and recorded in Step 25, on each side of RF signal. Also verify sidebands at 500 kHz and 1 MHz remain nulled.

Selected RF (Using Keyboard 20 for LCD (21) Display)	Displayed RF (On External Spectrum Analyzer)
250.0000 MHz	340 MHz
450.0000 MHz	540 MHz
850.0000 MHz	940 MHz

30. Using Keyboard (21), select RF 460.0000 MHz on LCD (21) FREQUENCY Readout.

31. Rotate ANALY DISPR Control (38) to "1 M".

32. Connect a DVM, set to measure DC, to pin 1 of U2315A on HIGH LOOP PC Board #2.

33. Adjust R2387 on HIGH LOOP PC Board #2 so voltage on DVM switches from -10 VDC to +10 VDC as LCD (21) FREQUENCY Readout is changed from ≥ approximately 440.0000 MHz to ≤ approximately 480.0000 MHz.

NOTE

The actual switching point varies from set to set and is basically dependent on the crossover point of the HIGH/LOW PASS FILTER, which is now disconnected.

34. Disconnect fast tune line coax cable, P2805, from J2805 on HIGH LOOP Module. Verify Freq LOCK Indicator (43) on front panel blinks on and off.

35. Connect fast tune line coax cable, P2805, to J2805 on HIGH LOOP Module.

36. Connect P601 to J601 and P602 to J602 on the HIGH/LOW PASS FILTER Module.

STEP	PROCEDURE

37. Verify displayed signal on external Spectrum Analyzer changes for each corresponding frequency entered on Keyboard (20 and displayed on LCD (21) FREQUENCY Readout.

LCD (21) FREQUENCY Display	External Spectrum Analyzer Displayed RF
000.0000 MHz	90.0000 MHz
111.1111 MHz	201.1111 MHz
222.2222 MHz	312.2222 MHz
333.3333 MHz	423.3333 MHz
444.4444 MHz	534.4444 MHz
555.5555 MHz	645.5555 MHz
666.6666 MHz	756.6666 MHz
777.7777 MHz	867.7777 MHz
888.8888 MHz	978.8888 MHz
999.9999 MHz	1089.9999 MHz

38. Connect coax cable, P3004 to DELAY LINE Module output at J3004. Verify RF noise level 100 kHz on both sides of displayed signal drops ≥5 dB.

39. Disconnect external Spectrum Analyzer from J3005 on DELAY LINE Module and connect P3005 to J3005.

40. Using an external Spectrum Analyzer, measure output level at J2405 on DUAL VCO Module. Verify +5 to +12 dBm output level.

41. Disconnect Spectrum Analyzer from J2405 and connect P2405 to J2405.

42. Using an external Spectrum Analyzer, measure output level at J2404 on DUAL VCO Module. Verify a +5 to +12 dBm output level.

43. Disconnect Spectrum Analyzer from J2404 and connect P2404 to J2404.

44. Using an external Spectrum Analyzer, measure output level at J6902A on BUFFER AMP A. Verify a +5 to +12 dBm output level.

45. Disconnect Spectrum Analyzer from J6902A and reconnect P6902A to J6902A.

46. Set FM/AM-1500 controls as follows:

CONTROL	SETTING
Keyboard (20)	010.0000 MHz (LCD FREQUENCY Display)
ANALY DISPR (38)	"2 M"
DISPLAY (51)	"ANALY"

47. Connect an external Oscilloscope to pin 1 Test Point of U2308A on HIGH LOOP PC Board #2. Adjust R2359 (ZERO) for 0 VDC (±1 VDC) on Oscilloscope.

48. Using Keyboard (20) select RF 999.0000 MHz to display on LCD (21) FREQUENCY Readout.

STEP	PROCEDURE

49. Adjust R2330 (FREQUENCY) on HIGH LOOP PC Board #2 for 0 VDC (±1 VDC) on Oscilloscope.

50. Repeat Steps 46 thru 49, then go to Step 51.

51. Using Keyboard (20), select the following settings for display on LCD (21) FREQUENCY Readout and verify voltage level on external Oscilloscope is 0 VDC (±5 VDC) for each setting.

    LCD (21) FREQUENCY Readout

    900.2000 MHz
    800.2000 MHz
    700.2000 MHz
    600.2000 MHz
    500.2000 MHz
    400.2000 MHz
    300.2000 MHz
    200.2000 MHz
    100.2000 MHz
    000.2000 MHz

52. Disconnect all test equipment and re-install all coaxes and modules.

4-5-2 LOW LOOP CALIBRATION

SPECIAL ACCESSORY EQUIPMENT REQ'D: 1 Spectrum Analyzer – Capable of measuring 79.3 MHz

FIGURE REFERENCES: FM/AM-1500 Interconnect (Figure 7-1)

Low Loop Module (Figure 6-19)

Low Loop Mixer Module (Figure 6-20)

TEST SET-UP DIAGRAM: N/A

STEP PROCEDURE

1. Set PWR/OFF/BATT switch (13) to "PWR".
2. Use Keyboard (20) to select 000.0000 MHz on LCD (21) FREQUENCY Readout.
3. Using external Spectrum Analyzer, measure output level at J4001 on Low Loop Module. Verify level is -12 dBm (+2, -3 dBm) at 9.3 MHz.
4. Verify output frequency as displayed on external Spectrum Analyzer is equal to 9.3000 MHz minus the decimal portion of the selected RF as shown:

Selected LCD (21) FREQUENCY Readout	Spectrum Analyzer Displayed RF
XXX.0000 MHz	9.3000 MHz (9.3000-.0000)
XXX.1111 MHz	9.1889 MHz (9.3000-.1111)
XXX.2222 MHz	9.0778 MHz (9.3000-.2222)
XXX.3333 MHz	8.9667 MHz (9.3000-.3333)
XXX.4444 MHz	8.8556 MHz (9.3000-.4444)
XXX.5555 MHz	8.7445 MHz (9.3000-.5555)
XXX.6666 MHz	8.6334 MHz (9.3000-.6666)
XXX.7777 MHz	8.5223 MHz (9.3000-.7777)
XXX.8888 MHz	8.4112 MHz (9.3000-.8888)
XXX.9999 MHz	8.3001 MHz (9.3000-.9999)

NOTE

"X" in the above examples is equal to any digit.

5. Disconnect Spectrum Analyzer from J4001 and connect P4001 to J4001 on LOW LOOP Module.
6. Using external Spectrum Analyzer, measure output level at J1804 on LOW LOOP MIXER Module. Verify level is +4 to +12 dBm at approximately 79.3 MHz.
7. Disconnect Spectrum Analyzer from J1804 and connect P1804 to J1804 on LOW LOOP MIXER Module.

STEP	PROCEDURE
8.	Using external Spectrum Analyzer, measure output level at J1803 on LOW LOOP MIXER Module. Verify level is +4 to +12 dBm at approximately 79.3 MHz.
9.	Disconnect all test equipment and connect all removed coax cables.

4-6 RECEIVER FUNCTIONAL BLOCK

4-6-1 RECEIVER SIGNAL CALIBRATION

SPECIAL ACCESSORY EQUIPMENT REQ'D:

1 Audio Distortion Analyzer – HP8903A

1 Digital Voltmeter – Any

1 RF Signal Generator – Capable of generating 125.5 MHz at -90 dBm

1 Frequency Counter – Capable of reading 10 kHz

1 10K Resistor – 5%

1 1 µF Tantalum Capacitor – 20%

1 Function Generator – Capable of 120 kHz sine wave

1 Oscilloscope – Any

FIGURE REFERENCES: Demod Audio PC Board (Figure 6-25)

I/O Interface PC Board (Figure 6-39)

TEST SET-UP DIAGRAM: N/A

NOTE

FM/AM-1500 Serial Numbers 1005 thru 1425 contain DEMOD AUDIO PC Board 7010-5034-700. FM/AM-1500 Serial Numbers 1426 thru 2817 contain DEMOD AUDIO PC Board 7010-5037-300. FM/AM-1500 Serial Numbers 2818 and on contain DEMOD AUDIO PC Board 7010-5038-900. All adjustments and test points referenced in the following calibration procedure are for the 7010-5037-300 and 7010-5038-900 PC Boards only. For adjustments and test points on 7010-5034-700 PC Boards, see FM/AM-1500 Maintenance Manual Rev. 0 thru Rev. 3.

STEP	PROCEDURE
1.	Connect a Digital Voltmeter (DVM) between pin 24 of J4701 on DEMOD AUDIO PC Board and pin 35 of U4337 on I/O INTERFACE PC Board.
2.	Short pin 24 of J4701 to ground and adjust R4350 on I/O INTERFACE PC Board to give an indicated zero volts on DVM.
3.	Remove short between pin 24 of J4701 and ground.

4. Connect DVM between Test Point 1 (TP1) and ground on I/O INTERFACE PC Board. Adjust R4354 on I/O INTERFACE PC Board for an indicated +2.00 VDC on DVM.

5. Set FM/AM-1500 controls as follows:

CONTROL	SETTING
(6) DEV/PWR	"20 KHz"
(7) MODULATION	"FM2"
(20) Keyboard	RF 120.2000 MHz (on LCD FREQUENCY Readout)
(51) DISPLAY	"METER"

6. Connect an RF Generator, set at 120.2 MHz at -30 dBm, to ANTENNA Connector (56).

7. Connect DVM to pin 5 of U4733 on DEMOD AUDIO PC BOARD. Verify a voltage reading on DVM of +1.6 to +2.5 VDC.

8. Adjust modulation, at a 1 kHz rate, on RF Generator until CRT Meter reads 20 kHz deviation.

9. Adjust R4950 (DEV/MOD METER CAL) on DEMOD AUDIO PC Board for an indicated 20 kHz deviation on MODULATION Meter (1).

10. Turn off modulation of RF Generator signal.

11. Rotate DEV/PWR Control (6) to "SIG". Adjust R4840 (SIG STR CAL) on DEMOD AUDIO PC Board for an indicated 99.9% on CRT Meter.

12. Disconnect RF Generator from FM/AM-1500.

13. Rotate MODULATION Control (7) to "SSB".

14. Adjust R4707 (SSB INJECTION LEVEL) on DEMOD AUDIO PC Board until needle on MODULATION Meter (1) just barely deflects to the right. At this point, slowly adjust R4707 so not to deflect needle to the right.

NOTE

This adjustment sets the beat frequency oscillation point of the AM Detector when in SSB.

15. Connect RF Generator, set at 120.2 MHz CW at -30 dBm, to ANTENNA Connector (56).

16. Select RF of 120.2010 MHz to display on LCD (21) FREQUENCY Readout and verify a 1 kHz demod tone is heard.

17. Connect the TONES OUTPUT Connector (27) to the SCOPE/SINAD INPUT Connector (24).

STEP	PROCEDURE

18. Set FM/AM-1500 controls as follows:

CONTROL	SETTING
(6) DEV/PWR	"SINAD"
(20) Keyboard	TONE 1 1000.0 Hz (LCD Display)
(31) TONE 2	Fully ccw
(33) TONE 1	Fully cw
(39) DEV/VERT	"1 V/DIV"

19. Adjust R4854 (SINAD NULL No. 1) and R4857 (SINAD NULL No. 2) on DEMOD AUDIO PC Board for maximum indication on CRT Meter and MODULATION Meter (1).

NOTE

Maximum SINAD on MODULATION Meter (1) is full scale to the left.

20. Rotate DISPLAY Control (51) to "SCOPE". Rotate VERT VERNIER Control (44) for a display on CRT eight major divisions peak to peak.

21. Rotate TONE 1 Control (33) fully ccw. Set LCD (21) to 1800 Hz TONE 2. Rotate TONE 2 Control (31) for a display on CRT 2 major divisions peak to peak.

22. Rotate TONE 1 Control (33) fully cw. Rotate DISPLAY Control (51) to "METER".

23. Adjust R4855 (R4861) (SINAD CAL) on DEMOD AUDIO PC Board until 12 dB SINAD is indicated on CRT Meter and MODULATION Meter (1) indicates 12 dB SINAD (±1 dB).

24. Rotate MODULATION Control (7) to "FM 3". Connect DEMOD OUTPUT Connector (25) to external Oscilloscope.

25. Connect an external Frequency Counter to FM output connector of RF Generator. Vary the modulation rate of the RF Generator from 500 Hz to 10 kHz to verify displayed demod output level on external Oscilloscope remains constant and the CRT Meter reads within 1 count of external Frequency Counter.

26. Adjust CW output of RF Generator from -30 dBm to -50 dBm. Verify receiver of FM/AM-1500 remains quiet.

NOTE

Test Point 1 (TP1) is provided to allow Function Generator, connected in Steps 27 and 28, to be connected directly to the unit.

27. Solder a 10 K resistor and a 1 µF tantalum capacitor in series. Connect the (+) end of the capacitor to pin 2 of U4733 on DEMOD AUDIO PC Board.

28. Connect a Function Generator, set to 20 kHz sine wave, to the free end of the 10 K resistor.

STEP	PROCEDURE
29.	Rotate MODULATION Control (7) to "FM 4".
30.	Connect a coax cable between the DEMOD OUTPUT Connector (25) and the SCOPE/SINAD INPUT Connector (24). Rotate DISPLAY Control (51) to "SCOPE". Adjust output of Function Generator so displayed signal height on CRT is four major divisions (two positive, two negative).
31.	Adjust the Function Generator output frequency to 50 kHz. Verify display on CRT is less than 10% smaller than display in Step 30 (less than two minor divisions down from positive peaks).
32.	Adjust the Function Generator output frequency to 120 kHz. Verify display on CRT is less than 30% smaller than display in Step 30 (less than six minor divisions down from positive peaks).
33.	Rotate MODULATION Control (7) to "FM 3".
34.	Adjust Function Generator for 10 kHz and adjust output level so displayed signal height on CRT is four major divisions (two positive, two negative).
35.	Adjust the Function Generator output frequency to 15 kHz. Verify display on CRT is less than 10% smaller than display in Step 34 (less than two minor divisions down from positive peaks).
36.	Adjust the Function Generator output frequency to 30 kHz. Verify display on CRT is less than 30% smaller than display in Step 38 (less than six minor divisions down from positive peaks).
37.	Rotate MODULATION Control (7) to "FM 2".
38.	Adjust Function Generator for 1 kHz and adjust output level so displayed signal height on CRT is four major divisions (two positive, two negative).
39.	Adjust the Function Generator output frequency to 5 KHz. Verify display on CRT is less than 10% smaller than display in Step 38 (less than two minor divisions down from positive peaks).
40.	Adjust the Function Generator output frequency to 10 KHz. Verify display on CRT is less than 20% smaller than display in Step 38 (less than four minor divisions down from positive peaks).
41.	Adjust the Function Generator output frequency to 15 KHz. Verify display on CRT is less than 30% smaller than display in Step 38 (less than six minor divisions down from positive peaks).
42.	Rotate DEV/PWR Control (6) to "120 KHz".

STEP	PROCEDURE

43. Using an external Oscilloscope and probe, verify full wave rectified signal with equal peaks is present on pin 7 of U4770 on DEMOD AUDIO PC Board.

44. Disconnect Function Generator from TP1.

45. Connect external RF Generator, set at 120.2 MHz, -50 dBm with 25 kHz deviation at 1 kHz sine wave rate, to ANTENNA Connector (56).

46. Rotate MODULATION Control (7) to "FM 4" and use Keyboard (20 to set 120.2000 MHz as LCD (21) FREQUENCY Readout.

47. Using a Distortion Meter, measure distortion out of DEMOD OUTPUT Connector (25). Verify distortion is less than 2%.

48. Rotate MODULATION Control (7) to "FM 1".

49. Reduce the deviation on RF Generator until indicated distortion on Distortion Meter is less than 2%. Verify deviation on RF Generator is ≥5 kHz.

50. Adjust output of RF Generator to 125.5 MHz CW at -90 dBm.

51. Set FM/AM-1500 controls as follows:

CONTROL	SETTING
(6) DEV/PWR	"SIG"
(7) MODULATION	"FM 1"
(20) Keyboard	125.5000 MHz (LCD FREQUENCY Readout)
(23) SQUELCH	Fully ccw
(51) DISPLAY	"METER"

52. Observe SIGNAL Meter on CRT. Adjust input level on RF Generator until SIGNAL Meter reads "20". Note and record input level of RF Generator.

53. Set 125.5250 MHz as LCD (21) FREQUENCY Readout.

54. Adjust output level of RF Generator until SIGNAL Meter on CRT reads "20". Verify the output level of RF Generator is at least 25 dB greater than level noted and recorded in Step 52.

55. Set 125.5500 MHz as LCD (21) FREQUENCY Readout.

56. Adjust output level of RF Generator until SIGNAL Meter on CRT reads "20". Verify output level of RF Generator is at least 40 dB greater than level noted and recorded in Step 52.

57. Disconnect all test equipment.

4-6-2 OSCILLOSCOPE CALIBRATION

SPECIAL ACCESSORY EQUIPMENT REQ'D:
1 Function Generator – Capable of 1 MHz sine wave and 10 KHz triangle wave

1 Power Supply – Variable from 0 to 40 VDC

FIGURE REFERENCES: Oscilloscope Control and Deflection PC Board (Figure 6-26)

TEST SET-UP DIAGRAM: N/A

STEP PROCEDURE

1. Set FM/AM-1500 Controls as follows:

CONTROL	SETTING
(3) HORIZ VERNIER	Fully cw in "CAL"
(13) PWR/OFF/BATT	"OFF"
(44) VERT VERNIER	Fully cw in "CAL"
(45) VERT POS	Centered
(46) FOCUS	Centered
(47) INTENSITY	Centered
(51) DISPLAY	"OFF"
(54) HORIZ POS	Centered

2. Remove Oscilloscope Control and Deflection PC Board, install extender board and install Oscilloscope Control and Deflection PC Board on extender board.

3. Set FM/AM-1500 Controls as follows:

CONTROL	SETTING
(5) HORIZ	".01 mS/DIV"
(13) PWR/OFF	"PWR"
(39) DEV/VERT	"1 V/DIV"
(51) DISPLAY	"SCOPE"

4. Verify Oscilloscope is illuminated.

5. Adjust R9553 (INTENSITY) for desired intensity of CRT.

6. Adjust R5182 (FOCUS) for desired focus of CRT.

7. Adjust R9565 and R9566 (TRACE ROTATION) until Oscilloscope trace is parallel to the horizontal graticules on the CRT.

8. Rotate Display Control (51) to "ANALY".

9. Disconnect P5402 from Spectrum Analyzer IF Module and P4603 from Spectrum Analyzer LO Module.

10. Short pins 14 and 15 to pin 3 (Gnd) of J5102 on Oscilloscope Control and Deflection PC Board. Verify analyzer sweep disappears from CRT.

STEP	PROCEDURE

11. Adjust R9559 (HORIZ CENTER) and R9561 (VERT CENTER) to center dot in exact center of CRT.

12. Remove short between pin 14 and pin 3 of J5102. Apply +0.800 VDC to pin 14. Adjust R5188 (VERT GAIN) to position dot on CRT at junction of major vertical graticule and uppermost horizontal graticule.

13. Again short pin 14 to pin 3 (Gnd) of J5102.

14. Remove short between pin 15 and pin 3 of J5102. Apply +2.00 VDC to pin 15 of J5102. Adjust R5193 (HORIZ GAIN) to position dot on CRT at junction of major horizontal graticule and rightmost vertical graticule.

15. Again short pin 15 to pin 3 (Gnd) of J5102.

16. Repeat sequence of Steps 10 thru 15 until no further adjustments are required to achieve desired positions of dot on CRT before continuing.

17. Remove shorts between pins 14 and 15 and pin 3 (Gnd) of J5102.

18. Set FM/AM-1500 Controls as follows:

CONTROL	SETTING
(39) DEV/VERT	"1 V/DIV"
(51) DISPLAY	"SCOPE"
(52) DC/AC	"DC"

19. Adjust VERT POS Control (45) and HORIZ POS Control (54) to center trace on CRT. Verify trace is 10.1 major divisions in length, centered on the major horizontal axis. Adjust R5119 (SWEEP WIDTH) for correct length of trace.

20. Using external Power Supply and BNC cable, apply +4.00 VDC to SCOPE/SINAD INPUT Connector (24). Adjust R5126 (EXTERNAL VERT GAIN) until trace is on uppermost major horizontal graticule of CRT.

21. Set DC/AC Switch (52) to "AC". Verify trace on CRT goes to major (center) horizontal axis.

22. Set DC/AC Switch (52) back to "DC". Adjust output of external Power Supply to +40 VDC and rotate DEV/VERT Control (39) to "10 V/DIV". Verify trace on CRT is on uppermost major horizontal graticule.

23. Rotate DEV/VERT Control (39) to ".1 V/DIV" and adjust output of external Power Supply to +0.4 VDC. Verify trace on CRT is on uppermost major horizontal graticule.

24. Rotate DEV/VERT Control (39) to ".01 V/DIV" and adjust output of external Power Supply to +0.04 VDC. Verify trace on CRT is on uppermost major horizontal graticule.

STEP	PROCEDURE
25.	Rotate DEV/VERT Control (39) to "1 V/DIV" and rotate HORIZ Control (5) to ".1 mS/DIV".
26.	Disconnect external Power Supply from FM/AM-1500.
27.	Using external Function Generator and 50 BNC coax cable, inject a 1 kHz sine wave signal into SCOPE/SINAD INPUT Connector (24). Adjust Signal Generator output power until trace on CRT is six major divisions peak-to-peak.
28.	Adjust output of external Function Generator to a 1 MHz sine wave. Verify trace on CRT is 4.2 to 7.8 major divisions in amplitude. If not, adjust C5115 for correct amplitude.
29.	Adjust output of external Function Generator back to 1 kHz sine wave. Rotate VERT VERNIER Control (44) ccw and verify UNCAL Indicator (Vertical) (42) illuminates and that display on CRT does not oscillate.
30.	Repeat Steps 27 and 28 and then rotate VERT VERNIER Control (44) fully cw to "CAL".
31.	Rotate HORIZ VERNIER Control (3) fully ccw and verify display on CRT increases in frequency.
32.	Rotate HORIZ VERNIER Control (3) fully cw to "CAL".
33.	Adjust output of external Function Generator to a 1 kHz triangle wave. Adjust R5116 (SWEEP RATE) for five major horizontal divisions between positive and negative peaks of display.
34.	Adjust output of external Function Generator to a 10 kHz triangle wave. Rotate HORIZ Control (5) to ".01 mS/DIV". Verify one complete cycle (±20%) is displayed on CRT.
35.	Adjust output of external Function Generator to a 1 kHz triangle wave. Rotate HORIZ Control (5) to ".1 mS/DIV". Verify one complete cycle (±20%) is displayed on CRT.
36.	Adjust output of external Function Generator to a 100 Hz triangle wave. Rotate HORIZ Control (5) to "1.0 mS/DIV". Verify one complete cycle (±20%) is displayed on CRT.
37.	Adjust output of external Function Generator to a 10 Hz triangle wave. Rotate HORIZ Control (5) to "10 mS/DIV". Verify one complete cycle (±20%) is displayed on CRT (50).
38.	Rotate HORIZ Control (5) to "TONES". Set LCD (21) to 10 Hz TONE 1. Rotate TONE 1 Control (33) cw and verify Lissajous pattern is available on CRT (50).
39.	Rotate DISPLAY Control (51) to "TONES" and adjust R9556 (BRIGHTNESS) for approximately the same brightness as was displayed on CRT (50) in "SCOPE".

STEP	PROCEDURE
40.	Observe the size of the menu raster displayed on CRT and adjust R5161 (VERTICAL RASTER) and R5169 (HORIZ RASTER) until display touches the bottom and the right sides of the CRT (50).
41.	Observe the display on CRT and adjust R9528 (ASTIGMATISM) for best focus across the screen.
42.	Remove Oscilloscope Control and Deflection PC Board from extender board, remove extender board from FM/AM-1500 and install Oscilloscope Control and Deflection PC Board in FM/AM-1500.
43.	Connect P5402 to Spectrum Analyzer IF Module and P4603 to Spectrum Analyzer LO Module.

4-6-3 FREQUENCY ERROR CALIBRATION

SPECIAL ACCESSORY EQUIPMENT REQ'D:
- 1 RF Signal Generator – Capable of 130 MHz at -110 dBm
- 1 Oscilloscope – Any

FIGURE REFERENCES: Demod Audio PC Board (Figure 6-25)

TEST SET-UP DIAGRAM: N/A

NOTE

FM/AM-1500 Serial Numbers 1005 thru 1425 contain DEMOD AUDIO PC Board 7010-5034-700. FM/AM-1500 Serial Numbers 1426 thru 2817 contain DEMOD AUDIO PC Board 7010-5037-300. FM/AM-1500 Serial Numbers 2818 and on contain DEMOD AUDIO PC Board 7010-5038-900. All adjustments and test points referenced in the following calibration procedure are for the 7010-5037-300 and 7010-5038-900 PC Boards only. For adjustments and test points on 7010-5034-700 PC Boards, see FM/AM-1500 Maintenance Manual Rev. 0 thru Rev. 3.

STEP PROCEDURE

1. Set FM/AM-1500 Controls as follows:

CONTROL	SETTING
(7) MODULATION	"FM2"
(19) GEN/REC	"REC"
(20) Keyboard	010.0000 MHz (LCD FREQUENCY Readout)
(37) FREQ ERROR	"300 Hz"

2. Connect a BNC/BNC coax between 10 MHz REF Connector (62) and ANTENNA Connector (56). Adjust R4790 (FREQ ERROR ZERO) on DEMOD AUDIO PC Board for a zero indication on FREQ ERROR Meter (41).

3. Set FM/AM-1500 Controls as follows:

CONTROL	SETTING
(20) Keyboard	010.0100 MHz (LCD FREQUENCY Readout)
(37) FREQ ERROR	"10 kHz"

4. Adjust R4838 (FREQ METER CAL) on DEMOD AUDIO PC Board for an indication of -1.0 on FREQ ERROR Meter (41).

5. Set RF 010.0030 MHz on LCD (21)FREQUENCY Readout. Rotate FREQ ERROR Control (37) to "3 kHz". Verify FREQ ERROR Meter (41) reads -3.0.

STEP	PROCEDURE

6. Set RF 010.0010 MHz on LCD (21) FREQUENCY Readout. Rotate FREQ ERROR Control (37) to "1 kHz". Verify FREQ ERROR Meter (41) reads -1.0.

7. Set RF 010.0003 MHz on LCD (21) FREQUENCY Readout. Rotate FREQ ERROR Control (37) to "300 Hz". Verify FREQ ERROR Meter (41) reads -3.0.

8. Set RF 010.0001 MHz on LCD (21) FREQUENCY Readout. Rotate FREQ ERROR Control (37) to "300 Hz". Verify FREQ ERROR Meter (41) reads -1.0.

9. Rotate FREQ ERROR Control to "30 Hz". Verify needle on FREQ ERROR Meter (41) is pegged.

10. Set FM/AM-1500 Controls as follows:

CONTROL	SETTING
(7) MODULATION	"AM2"
(21) LCD	120.2000 MHz
(37) FREQ ERROR	"10 kHz"

11. Connect an external RF Generator set at 120.2 MHz, CW, to ANTENNA Connector (56). Adjust R4798 (AM FLYWHEEL VOLTAGE) on DEMOD AUDIO PC Board until needle on FREQ ERROR Meter (41) is centered.

12. Set external RF Generator to 150% AM.

13. Connect an external Oscilloscope to pin 6 of U4717 on DEMOD AUDIO PC Board. Adjust R4744 (AM FLYWHEEL OFFSET) on DEMOD AUDIO PC Board for a null signal on external Oscilloscope.

14. Set external RF Generator for a CW output.

15. Connect external Oscilloscope to pin 3 of U4717 on DEMOD AUDIO PC Board. Verify approximately +6 V on Oscilloscope. Note and record voltage.

16. Connect external Oscilloscope to pin 6 of U4717. Adjust R4798 (AM FLYWHEEL VOLTAGE) on DEMOD AUDIO PC Board for same voltage as noted and recorded in Step 15.

NOTE

If R4798 does not allow desired voltage to be achieved, adjust it as close as possible and then repeat Steps 12 thru 16.

17. Set external RF Generator to 150% AM.

18. Connect external Oscilloscope to pin 6 of U4717. Adjust R4744 (AM FLYWHEEL OFFSET) on DEMOD AUDIO PC Board for a null signal on Oscilloscope.

19. Disconnect RF Generator from FM/AM-1500.

20. Set FM/AM-1500 Controls as follows:

CONTROL	SETTING
(7) MODULATION	"FM3"
(19) GEN/REC	"REC"
(20) Keyboard	1000.0 Hz LCD TONE 1 Readout 1000.0 Hz LCD TONE 2 Readout
(26) Tone 2 FM/OFF/AM	"OFF"
(28) Tone 1 FM/OFF/AM	"OFF"
(37) FREQ ERROR	"300 AUDIO Hz"
(51) DISPLAY	"METER"

21. Adjust TONE 2 Control (31) for a 450 Hz deviation indication on MODULATION Meter (1).

22. Connect an external Oscilloscope to pin 1 of U4738 on DEMOD AUDIO PC Board.

23. Using TONE 2 Control (31), vary indicated deviation on MODULATION Meter (1) from 450 Hz to maximum indication and back to 450 Hz. Verify AGC level on Oscilloscope is constant over entire range.

24. Use Keyboard (20) to set TONE 1 LCD (21) Readout to 0710.0 Hz and TONE 2 LCD (21) Readout to 0410.0 Hz . Verify FREQ ERROR Meter (41) reads -3.0 and CRT Meter indicates 410 Hz.

25. Use Keyboard (20) to set TONE 1 LCD (21) Readout to 0410.0 Hz and TONE 2 LCD (21) Readout to 0710.0 Hz. Verify FREQ ERROR Meter (41) reads +3.0 and CRT (50) Meter indicates 710 Hz.

26. Use Keyboard (20) to set TONE 1 LCD (21) Readout to 0409.0 Hz and TONE 2 LCD (21) Readout to 0709.0 Hz. Verify FREQ ERROR Meter (41) and CRT (50) Meter DO NOT read +3.0 and 709 Hz, respectively.

27. Rotate FREQ ERROR Control (37) to "300 Hz" and verify CRT (50) Meter reads 709 Hz.

28. Rotate FREQ ERROR Control (37) to "30 AUDIO Hz" and set LCD (21) to 0120.0 Hz TONE 1 and 0150.0 Hz TONE 2. Verify FREQ ERROR Meter (41) reads +3.0 and CRT (50) reads 150 Hz.

29. Rotate FREQ ERROR Control (37) to "3 AUDIO Hz" and set LCD (21) to 9997.0 Hz TONE 1 and 10000 Hz TONE 2. Rotate TONE 2 Control (31) for an indication of 1000 Hz deviation on MODULATION Meter (1). Verify FREQ ERROR Meter reads +3.0 and CRT (50) reads 10,000 Hz.

30. Connect external Oscilloscope to pin 9 of P4702 on DEMOD AUDIO PC Board.

STEP	PROCEDURE

31. Set FM/AM-1500 Controls as follows:

CONTROL	SETTING
(7) MODULATION	"FM2"
(18) DUPLEX/SIMPLEX	"SIMPLEX"
(19) GEN/REC	"GEN"
(20) Keyboard	1000.0 Hz TONE 1 Readout

32. Rotate TONE 1 Control (33) to obtain a 150 Hz deviation indication on MODULATION Meter (1).

33. Rotate TONE 1 Control (33) slowly until a square wave occurs on external Oscilloscope. Verify deviation indication is ≤450 Hz on MODULATION Meter (1).

34. Set FM/AM-1500 Controls as follows:

CONTROL	SETTING
(7) MODULATION	"FM1"
(19) GEN/REC	"REC"
(20) Keyboard	RF 850.5000 MHz (LCD FREQUENCY Readout)
(23) SQUELCH	Fully ccw
(37) FREQ ERROR	"300 Hz"

35. Connect external Signal Generator to ANTENNA Connector (56). Set RF Generator to 850.5000 MHz at -90 dBm.

36. Observe the FREQ ERROR Meter (41) while slowly lowering the RF level output of external RF Generator. Verify RF Generator output is -101 dBm or less when FREQ ERROR Meter (41) indicates 100 Hz.

37. Disconnect all test equipment.

4-6-4 MODULATION CALIBRATION

SPECIAL ACCESSORY EQUIPMENT REQ'D:

1 RF Generator – Capable of 130 MHz at -30 dBm

1 Boonton Modulation Meter – Capable of reading 15 kHz deviation; selectable filters

1 Digital Voltmeter – Any

1 Function Generator – Capable of 8 Vp-p Sine Wave.

FIGURE REFERENCES: Demod Audio PC Board (Figure 6-25)
Oscilloscope Control and Deflection PC Board (Figure 6-26)

TEST SET-UP DIAGRAM: N/A

NOTE

FM/AM-1500 Serial Numbers 1005 thru 1425 contain DEMOD AUDIO PC Board 7010-5034-700. FM/AM-1500 Serial Numbers 1426 thru 2817 contain DEMOD AUDIO PC Board 7010-5037-300. FM/AM-1500 Serial Numbers 2818 and on contain DEMOD AUDIO PC Board 7010-5038-900. All adjustments and test points referenced in the following calibration procedure are for the 7010-5037-300 and 7010-5038-900 PC Boards only. For adjustments and test points on 7010-5034-700 PC Boards, see FM/AM-1500 Maintenance Manual Rev. 0 thru Rev. 3.

STEP PROCEDURE

1. Set FM/AM-1500 controls as follows:

CONTROL	SETTING
(4) AVG PEAK/PEAK	PEAK
(6) DEV/PWR	2 KHz
(7) MODULATION	FM2
(19) GEN/REC	REC
(20) Keyboard	RF 120.2000 MHz (LCD FREQUENCY Readout)

2. Set the following controls on the Modulation Meter:

CONTROL	SETTING
High-Pass Filter	300 Hz
Low-Pass Filter	15 kHz

STEP	PROCEDURE

3. Set the following controls on the RF Generator:

CONTROL	SETTING
FREQUENCY	120.2 kHz
AMPLITUDE	-30 dBm
RATE	1 kHz

4. Connect the RF Generator to a BOONTON Modulation Meter and adjust level to 10 kHz deviation at 1 kHz rate as indicated on Modulation Meter.

5. Disconnect RF Generator from Modulation Meter and connect output of RF Generator to ANTENNA Connector (56).

6. Connect a Digital Voltmeter to DEMOD OUTPUT Connector (25).

7. Adjust R4803 (FM DEMOD LEVEL) on DEMOD AUDIO PC Board to give an indicated 0.566 VRMS on Digital Voltmeter.

8. Set output modulation of RF Generator to CW.

9. Set the following FM/AM-1500 Controls:

CONTROL	SETTING
(6) DEV/PWR	60 kHz
(7) MODULATION	FM2

10. Connect Digital Voltmeter to pin 7 of U4785.

11. Adjust R4912 (FM 2 ZERO) on DEMOD AUDIO PC Bd to give an indicated zero voltage reading on Digital Voltmeter.

12. Connect Digital Voltmeter to pin 1 of U4773.

13. Adjust R4897 (PEAK DETECTOR ZERO) on DEMOD AUDIO PC Board for an indicated zero voltage reading on Digital Voltmeter.

14. Set the following controls on the BOONTON Modulation Meter:

CONTROL	SETTING
FUNCTION	kHz – DEVIATION
HIGH-PASS FILTER	10 kHz
LOW-PASS FILTER	3 kHz
RANGE	10
PEAK	PK – PK/2
TUNING	Auto

15. Select -10 dBm CW on RF Generator.

16. Connect RF Generator to BOONTON Modulation Meter and note the Residual FM of the Modulation.

    RESIDUAL FM: _____

17. Select the following FM/AM-1500 Controls:

CONTROL	SETTING
(4) AVG PEAK/PEAK Switch	Peak
(7) MODULATION	FM1
(39) DEV/VERT Control	2 kHz/DEV
(55) ATTENUATOR SWITCH	(Antenna)40 dB

18. Select "Meter" on DISPLAY (51) Control.

19. Verify Residual FM on CRT (50) is same as on BOONTON Modulation Meter (Step 16). Adjust R5009 (FM 1 ZERO) on DEMOD AUDIO PC Board, as needed.

20. Set Modulation Control (7) to "FM 2".

21. Verify Modulation Meter (1) measures same Residual FM as BOONTON Modulation Meter (Step 16). Adjust R5012 (FM 2 ZERO) on DEMOD AUDIO PC Board, as needed.

22. Set Low-pass filter on BOONTON Modulation Meter to 15 kHz.

23. Connect RF Generator to BOONTON Modulation Meter and note Residual FM displayed on Modulation Meter.

    RESIDUAL FM: _____

24. Set Modulation Control (7) to "FM 3".

25. Connect RF Generator to Antenna Connector (56).

26. Verify CRT (50) measures same Residual FM as BOONTON Modulation Meter (Step 23). Adjust R5010 (FM 3 ZERO) on DEMOD AUDIO PC Board, as needed.

27. Set Modulation Control (7) to "FM 4".

28. Set Low-pass filter on BOONTON Modulation Meter to 120 kHz.

29. Connect RF Generator to BOONTON Modulation Meter and note the Residual FM displayed on the Modulation Meter.

    RESIDUAL FM: _____

30. Connect RF Generator to Antenna Connector (56) of the FM/AM-1500.

31. Verify CRT (50) measures same Residual FM as Boonton Modulation Meter (Step 29). Adjust R5011 (FM 4 ZERO) on DEMOD AUDIO PC Board, as needed.

32. Set the following BOONTON Modulation Meter controls:

CONTROL	SETTING
HIGH-PASS FILTER	300 Hz
LOW-PASS FILTER	3 kHz

33. Set the following FM/AM-1500 controls:

CONTROL	SETTING
(4) AVG PEAK/PEAK Switch	AVG-PEAK
(6) DEV/PWR Control	2 kHz
(7) MODULATION Control	FM 2
(51) DISPLAY Control	Meter

34. Connect RF Generator to ANTENNA Connector (56) and note Residual FM.

    RESIDUAL FM: _____

35. Set AVG PEAK/PEAK Switch (4) to "PEAK" and note Residual FM shown on CRT display (50).

    RESIDUAL FM: _____

36. Connect RF Generator to BOONTON Modulation Meter and note Residual FM.

    RESIDUAL FM: _____

37. Adjust RF Generator to 5 kHz at 1 kHz rate.

NOTE

This signal must be adjusted to include the Residual FM noted in Step 36.

38. Connect RF Generator to ANTENNA Connector (56).

39. Set DEV/PWR Control (6) to "6 kHz DEV".

40. Adjust R4913 (PEAK DEV), as needed, to attain 5 kHz on CRT (50) and adjust R4950 to attain 5 kHz on MODULATION Meter (1).

NOTE

This signal must be adjusted to include the Residual FM noted in Step 36 (i.e., 5 kHz + RESIDUAL in Step 36).

41. Set AVG PEAK/PEAK Switch (4) to "AVG PEAK".

42. Adjust R4914 (AVG DEV) to 5 kHz Deviation.

NOTE

This signal must be adjusted to include the Residual FM noted in Step 36 (i.e., 5 kHz + RESIDUAL in Step 36).

43. Repeat Steps 14 through 42 to fine tune the set, before proceeding.

44. Set the following FM/AM-1500 Controls:

CONTROL	SETTING
(5) HORIZ Control	.1 ms/DIV
(6) DEV/PWR	2 kHz/DIV DEV
(51) DISPLAY Control	SCOPE

45. Adjust R4873 (DEV CAL) pot on Oscilloscope Control and Deflection PC Board, as needed, to read five divisions peak to peak, centering the scope trace peaks on the CRT.

46. Set the following controls on the BOONTON Modulation Meter.

CONTROL	SETTING
HIGH-PASS FILTER	300 Hz
LOW-PASS FILTER	3 kHz

47. Connect RF Generator to BOONTON Modulation Meter and note Residual FM.

RESIDUAL FM: _____

48. Select 1 kHz tone on RF Generator.

49. Adjust FM deviation on RF Generator to 1 kHz (±1 kHz).

NOTE

This signal must be adjusted to include the Residual FM noted in Step 36.

50. Set the following FM/AM-1500 controls:

CONTROL	SETTING
(4) AVG PEAK/PEAK Switch	PEAK/DEV
(6) DEV/PWR Control	2 kHz DEV
(7) MODULATION Control	FM2

51. Connect RF Generator to ANTENNA Connector (56).

52. Set the following BOONTON Modulation Meter Controls:

CONTROL	SETTING
HIGH-PASS FILTER	3 kHz
LOW-PASS FILTER	15 kHz

53. Set the following RF Generator controls:

CONTROL	SETTING
MODULATION	NONE (CONTINUOUS WAVE)
AMPLITUDE	-10 dBm

54. Connect RF Generator to BOONTON Modulation Meter and note Residual FM.

RESIDUAL FM: _____

55. Adjust RF Generator for 2 kHz deviation at 6 kHz rate.

NOTE

This signal must be adjusted to include the Residual FM noted in Step 54.

56. Set the following FM/AM-1500 Controls:

CONTROL	SETTING
(4) AVG PEAK/PEAK Switch	PEAK/DEV
(6) DEV/PWR Control	6 kHz

57. Connect RF Generator to ANTENNA Connector (56).

58. Adjust R4768 (6 kHz DEV), as needed, for 2 kHz deviation.

NOTE

This signal must be adjusted to include the Residual FM noted in Step 54.

59. Set the following controls on the BOONTON Modulation Meter.

CONTROL	SETTING
LOW-PASS FILTER	120 kHz
HIGH-PASS FILTER	3 kHz

60. Set the RF Generator modulation to CW.

61. Connect the RF Generator to the BOONTON Modulation Meter and note the Residual FM

RESIDUAL FM: _____

62. Adjust the RF Generator for 8 kHz deviation at 10 kHz rate.

NOTE

This signal must be adjusted to include the Residual FM noted in Step 61.

63. Set the following FM/AM-1500 controls:

CONTROL	SETTING
(6) DEV/PWR Control	20 kHz DEV
(7) MODULATION Control	FM 3

64. Connect RF Generator to ANTENNA Connector (56).

65. Adjust R4778 (10 kHz ADJ), as needed, for 8 kHz deviation.

NOTE

This signal must be adjusted to include the Residual FM noted in Step 16.

STEP	PROCEDURE

66. Set the following FM/AM-1500 controls:

CONTROL	SETTING
(7) MODULATION Control	FM 2, FM 3 or FM 4
(51) DISPLAY Control	SCOPE
(39) DEV/Vert Control	20 kHz/DIV

67. Set RF Generator to 60 kHz Deviation at 1 kHz Rate.

68. Connect RF Generator to ANTENNA Connector (56).

69. Verify no clipping of peaks (either positively or negatively) on CRT display (50).

70. Set output of RF Generator to CW.

71. Set FM/AM-1500 Controls as follows:

CONTROL	SETTING
(4) AVG PEAK/PEAK	PEAK
(6) DEV/PWR	2%
(7) MODULATION	AM 2
(51) DISPLAY	METER

72. Adjust R4918 (AM ZERO) on DEMOD AUDIO PC Board an indication of zero on CRT (50) and on MODULATION Meter (1).

73. Set RF Generator to 50% AM with a 1 kHz tone.

74. Rotate DEV PWR Control (6) to 6%. Set AVG PEAK/PEAK Switch to PEAK. Adjust R4810 (AM% CAL) on DEMOD AUDIO PC Board for an indicated 50% on CRT (50) and on MODULATION Meter (1).

75. Set FM/AM-1500 Controls as follows:

CONTROL	SETTING
(6) DEV/PWR	20 kHz
(7) MODULATION	FM2
(19) GEN/REC	GEN
(51) DISPLAY	TONES

76. Select TONE SEQUENCE Menu on CRT (50) and enter following data as Item 01:

T1	1000.0	10.0	9000
T2	0000.0	0.0	

Then press "EXEC, 2ND, T.SEQ, 1, ., ENTER".

77. Adjust R3333 in FM Generator Module until CRT (50) reads 10 kHz deviation.

78. Connect a microphone to MIC Connector (34). While talking into microphone, adjust R4932 (FM MIKE LEVEL) on DEMOD AUDIO PC Board for maximum 5 kHz deviation on MODULATION Meter (1).

STEP	PROCEDURE

79. Set FM/AM-1500 Controls as follows:

CONTROL	SETTING
(6) DEV/PWR	6%
(7) MODULATION	AM 2
(19) GEN/REC	GEN

80. Select TONE SEQUENCE Menu on CRT (50) and enter following data as Item 01:

T1	1000.0	5.0	9000
T2	0000.0	0.0	

81. Press "EXEC, 2ND, T.SEQ, 1, ., ENTER"

82. Adjust R7983 (AM % MOD) on DEMOD AUDIO PC Board so MODULATION Meter (1) reads 50% modulation.

83. While keying microphone, adjust R4933 (AM MIKE LEVEL) on DEMOD AUDIO PC Board for maximum 95% AM on MODULATION Meter (1).

84. Rotate MODULATION Control (7) to FM 2.

85. Check the pins on the EXT ACC Connector (29) (see Figure 3-4):

Pin #	Output/Input	Method
1	+12 V out	Voltage check
2	-12 V out	Voltage check
3	+5 V out	Voltage check
4	Tone Gen out	Signal check
5	Ext FM Mod in	Signal check
6	Tone Key in	Ground to test
7	Mike Key in	Ground to test
8	Demod out	Signal check
9	Power Ground	----------
10	Signal Ground	----------

86. Connect a Function Generator into EXT FM MOD Connector (32).

87. Set FM/AM-1500 Controls as follows:

CONTROL	SETTING
(6) DEV/PWR	20 kHz
(7) MODULATION	FM 2
(19) GEN/REC	GEN
(26) Tone 2 FM/OFF/AM	OFF
(28) Tone 1 FM/OFF/AM	OFF

88. Adjust Function Generator so 15 kHz of deviation is indicated on MODULATION Meter (1). Verify output signal of Function Generator is between 4 and 8 Vp-p sine wave.

89. Connect Function Generator to EXT AM MOD Connector (30).

90. Rotate MODULATION Control (7) to AM 1.

STEP	PROCEDURE

91. Adjust Function Generator so 90% AM is indicated on MODULATION Meter (1). Verify output signal of Function Generator is between 2 and 4 Vp-p sine wave.

92. Set FM/AM-1500 Controls as follows:

CONTROL	SETTING
(6) DEV/PWR	6 kHz
(7) MODULATION	FM 2
(19) GEN/REC	GEN
(37) FREQ ERROR	3 AUDIO Hz

93. Select DCS Menu on CRT (50) and enter following data into Items 1 thru 4:

01	000	NORM	0.5
02	006	NORM	0.5
03	146	NORM	0.5
04	777	NORM	0.5

94. For each item in previous step, push:

"EXEC, 2ND, DCS, (ITEM #), ENTER"

Verify valid reception code for each item while speaking into a keyed microphone.

95. Disconnect all test equipment.

4-6-5 INPUT/OUTPUT POWER CALIBRATION

SPECIAL ACCESSORY EQUIPMENT REQ'D:
- 1 DC Power Supply – Capable of +1 VDC
- 1 RF Power Source – Capable of 10 W at 850 MHz
- 1 270Ω Resistor – 5%

FIGURE REFERENCES: Demod Audio PC Board (Figure 6-25)

Power Termination Mechanical Assembly (Figure 6-33)

TEST SET-UP DIAGRAM: N/A

STEP PROCEDURE

1. Set FM/AM-1500 Controls as follows:

CONTROL	SETTING
(6) DEV/PW	"15 WATTS"
(19) GEN/REC	"GEN"
(22) VOLUME	Fully cw
(31) TONE 2	Fully ccw
(33) TONE 1	Fully ccw

2. Using external Power Supply, apply +1 VDC to FL6204 on Power Termination Module. Verify speaker output changes from no output to noise.
3. Disconnect external Power Supply from Power Termination Module.
4. Zero MODULATION Meter (1) to give an indication of zero watts by adjusting R4871 (ZERO PWR) on the DEMOD AUDIO PC Board.
5. Using an external RF Power Source, apply 10 watts of RF power at 120.2 MHz to the TRANS/-40 dB DUPLEX Connector (11). Adjust R4904 (15 W) on DEMOD AUDIO PC Board for following indications:
   a. CRT power meter reads 10 watts. Note and record.
   b. MODULATION Meter (1) reads between 9 and 11 watts. Note and record.
   c. When DISPLAY Control (51) is rotated to "ANALY", the display on the CRT is approximately at the -40 dB level.
6. Rotate DEV/PWR Control (6) to "150 WATTS". Adjust R4881 (150 W) on DEMOD AUDIO PC Board for following indications:
   a. CRT power meter reads 10 watts.
   b. MODULATION Meter (1) reads between 9 and 11 watts.
7. Change RF Power Source to apply 10 watts at 850 MHz.

STEP	PROCEDURE

8. Rotate DEV/PWR Control (51) to "15 WATTS". Adjust R6212 (DET FLATNESS) in POWER TERMINATION Module for following indications:

   a. CRT power meter reads within 0.5 watts of reading in Step 5.a.

   b. MODULATION Meter (1) reads within 0.5 watts of reading in Step 5.b.

9. Change RF Power Source to 0 watts. Slowly increase RF Power Source and verify FM/AM-1500 switches from Generate mode to Receive mode at approximately 100 mW.

10. Connect a 270Ω resistor between FL6202 on POWER TERMINATION Module and ground. Verify OVERTEMP Indicator (9) on front panel is illuminated.

11. Disconnect all test equipment.

4-7 GENERATOR FUNCTIONAL BLOCK

4-7-1 RF OUTPUT POWER CALIBRATION

SPECIAL ACCESSORY EQUIPMENT REQ'D:

1 Digital Voltmeter – Any

1 Spectrum Analyzer – Capable of measuring 1000 MHz

1 BOONTON Power Meter – Capable of reading -30 dBm

1 BOONTON Modulation Meter – Capable of reading 3.3 kHz deviation at 1000 MHz input

1 Oscilloscope – Any

300 Hz Low Pass Filter – See Appendix D

FIGURE REFERENCES:

FM Generator Mechanical Assembly (Figure 6-27)

Demod Audio PC Board (Figure 6-25)

Generator Mixer PC Board (Figure 6-28)

I/O Interface PC Board (Figure 6-39)

TEST SET-UP DIAGRAM: N/A

NOTE

FM/AM-1500 Serial Numbers 1005 thru 1425 contain DEMOD AUDIO PC Board 7010-5034-700. FM/AM-1500 Serial Numbers 1426 thru 2817 contain DEMOD AUDIO PC Board 7010-5037-300. FM/AM-1500 Serial Numbers 2818 and on contain DEMOD AUDIO PC Board 7010-5038-900. All adjustments and test points referenced in the following calibration procedure are for the 7010-5037-300 and 7010-5038-900 PC Boards only. For adjustments and test points on 7010-5034-700 PC Boards, see FM/AM-1500 Maintenance Manual Rev. 0 thru Rev. 3.

STEP	PROCEDURE
1.	Set PWR/OFF/Batt switch (13) to "PWR".
2.	Present only under the following conditions: GEN/REC Switch (19) is in "GEN" or DISPLAY Control (51) is in "TRACK" or "SWEEP".

3. Set FM/AM-1500 Controls as follows:

CONTROL	SETTING
(10) RF Output Level	"-30 dBm"
(18) DUPLEX/SIMPLEX	"SIMPLEX"
(19) GEN/REC	"GEN"
(20) Keyboard	RF 500.0000 MHz (LCD FREQUENCY Readout)
(31) TONE 2	Fully ccw
(33) TONE 1	Fully ccw
(51) DISPLAY	Anywhere but on "TRACK" or "SWEEP"

4. Using external Spectrum Analyzer, measure the RF output at J4206 on the FM Generator Module. Verify output is -13 (+5, -6) dBm at 68.6 MHz.

5. Using external Spectrum Analyzer, measure the RF output at J4403 on the Generator Mixer Module. Adjust R3412 (F1 FIXED) and R3423 (F2 FIXED) in Generator Mixer Module to peak display. Adjust R3436 (OUTPUT LEVEL) in Generator Mixer Module to set output level to -12 to -16 dBm.

6. Connect a BOONTON Power Meter to TRANS/-40 dB DUPLEX Connector (11). Adjust R4963 (RF LEVEL) on DEMOD AUDIO PC Board for a reading of -30 dBm (±2.0 dB) on Power Meter.

7. Repeat Step 6 for following selected RF frequencies:

SECECTED FREQUENCIES

100 kHz	400 MHz
10 MHz	500 MHz
50 MHz	600 MHz
100 MHz	700 MHz
200 MHz	800 MHz
300 MHz	900 MHz

8. Disconnect Power Meter from, and connect external Spectrum Analyzer to TRANS/-40 dB DUPLEX Connector (11). Set external Spectrum Analyzer to 1 MHz/DIV dispersion, 300 kHz bandwidth and 10 dB/DIV.

9. Step FREQUENCY readings on LCD (21) as follows:

1 MHz Steps	10 MHz Steps
0 – 50 MHz	50 – 88 MHz
88 – 176 MHz	177 – 400 MHz
400 – 500 MHz	500 – 850 MHz
850 – 950 MHz	950 – 999 MHz

Verify at each step:

a. The spectrum 2 MHz on each side of carrier is rounded and does not break into oscillations (refer to Figure 4-2).

b. The spectrum between 1 MHz and 1.8 MHz on each side of carrier varies no more than 3 dB.

c. The delay line locks on each frequency – i.e., there is no excessive noise on Spectrum Analyzer.

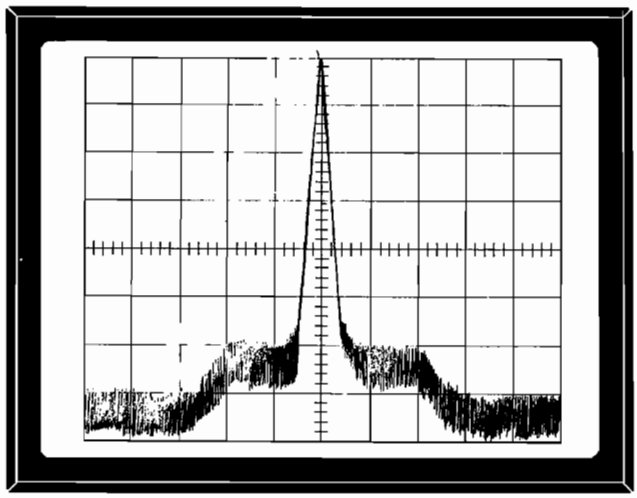

Figure 4-2 RF Output Display

10. Observe Spectrum Analyzer at following frequency settings:

30.2 MHz
175.2 MHz
450.2 MHz
850.2 MHz

Verify the spectrum 100 kHz on each side of the carrier is 65 dBc or lower.

11. Set FM/AM-1500 Controls as follows:

CONTROL	SETTING
(10) RF Output Level"	10 dBm"
(18) DUPLEX/SIMPLEX	"DUPLEX"
(21) LCD	850.2000 MHz

12. Using external Spectrum Analyzer, measure the RF output at the DUPLEX OUTPUT Connector (16). Verify level is -10 dBm (2 dB). Disconnect coax to DUPLEX OUTPUT Connector (16).

13. Connect a 50Ω Termination to DUPLEX OUTPUT Connector (16). Using external Spectrum Analyzer, measure RF output level at TRANS/-40 dB DUPLEX Connector (11). Verify output level is -50 dBm (3 dB).

14. Repeat Steps 12 and 13 for a 120.2000 MHz setting on LCD (21).

15. Connect Modulation Meter, 300 Hz Low-pass Filter and Digital Voltmeter to FM/AM-1500 as shown in Figure 4-3. Set Modulation Meter filters to 30 Hz high-pass and 3 KHz low-pass.

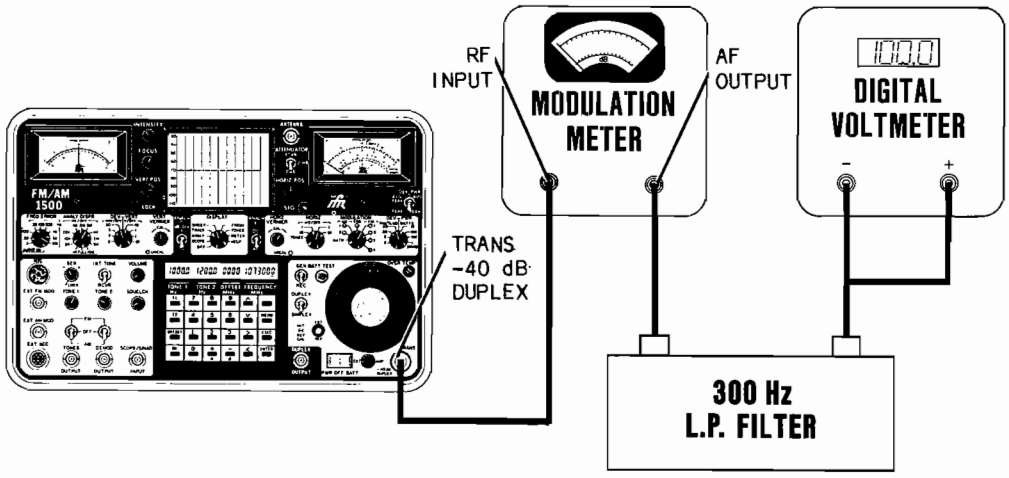

Figure 4-3 Residual FM Test Hookup

16. Set FM/AM-1500 Controls as follows:

CONTROL	SETTING
(20) Keyboard	120.2 Hz TONE 1 Readout
(28) Tone 1 FM/OFF/AM	"AM"
(51) DISPLAY	"METER"

17. Adjust TONE 1 Control (33) for 10 KHz deviation.

18. Record VRMS reading on DVM as A.

19. Adjust TONE 1 Control fully CCW.

20. Record VRMS reading on DVM as B.

21. Calculate residual FM as follows:

10 kHz/A = X/B (X = residual FM)
Verify residual FM < 50 Hz.

22. Set Modulation Meter to 300 Hz high-pass and 3 kHz low-pass. Disconnect 300 Hz low-pass filter and connect DVM to AF Output of Modulation Meter.

23. Set TONE 1 LCD (21) Readout to 1000.0 Hz. Adjust TONE 1 Control (33) for 3.3 KHz (±10 Hz) deviation.

STEP	PROCEDURE

24. Measure the VRMS out of the Modulation Meter AF Output at the following FREQUENCY settings on the LCD (21): 100.2 MHz, 850.2 MHz and 999 MHz. Record reading at each setting as A.

25. Adjust TONE 1 Control fully ccw. Record reading at 100.2 MHz, 850.2 MHz and 999 MHz as B. Calculate dB ratio for each setting as follows:

    Ratio = 20 x log (A/B)

    Verify ratio is 40 dB or greater for each setting.

    NOTE:

    If DVM has a Relative button, it may be used to give a dB reading at each step.

26. Connect external Spectrum Analyzer to DUPLEX OUTPUT Connector (16).

27. Select 000.1000 MHz on LCD (21). Verify second harmonic (±200 kHz) is 25 dBc or lower.

28. Select 450.2000 MHz on LCD (21). Verify:

    a. Second harmonic (900.4 MHz) is 25 dBc or lower.

    b. Non-harmonics at 540.2 MHz and 850.4 MHz are at most -40 dBc and all other signals are 60 dBc or lower.

    c. Noise 20 KHz from 450.2000 MHz is 55 dBc or lower when on 3 KHz bandwidth.

29. Select 090.2000 thru 990.2000 MHz on LCD (21) in 100 MHz steps. Verify:

    a. Second harmonics in all cases are 25 dBc or lower.

    b. All non-harmonics are 40 dBc or lower.

30. Set FM/AM-1500 Controls as follows:

CONTROL	SETTING
(18) DUPLEX/SIMPLEX	"SIMPLEX"
(19) GEN/REC	"GEN"
(20) Keyboard	RF 850.2000 MHz (LCD FREQUENCY Readout)

31. Connect external Spectrum Analyzer to TRANS/-40 dB DUPLEX Connector (11).

32. Rotate RF Output Level Control (10) from -10 dBm to -80 dBm. Verify output level on display of Spectrum Analyzer is equal (±2 dB) to RF Output Level Control setting across the range.

33. Rotate RF Output Level Control (10) from -80 dBm to -127 dBm. Verify output level on display of Spectrum Analyzer is equal (±2.5 dB) to RF Output Level Control setting across the range.

34. Rotate RF Output Level Control (10) to -30 dBm.

35. Select RF SWEEP Menu on CRT. Enter following data:

Start	0.1 MHz
Stop	990.1 MHz
Inc STEP	10.0 MHz
Inc RATE	1000 ms

Then press: "EXEC, 2nd, FSWP, 1, ENTER, 2nd, STEP". Press "v" Key until 0.1 MHz (beginning) is reached.

36. Connect Oscilloscope and Voltmeter, with a BNC Tee, to X-OUT Connector (59) on rear panel of FM/AM-1500. Verify voltage of 0 VDC. If not, adjust R4333 on I/O Interface PC Board for 0 VDC.

37. Press: "EXEC, ENTER".

38. Observe RF SWEEP signal on external Spectrum Analyzer as it steps up each 10 MHz. Verify High Loop locks on each frequency, with no oscillations.

39. Observe Oscilloscope and verify voltage changes with each INC STEP of menu.

40. Observe Voltmeter when FREQ SWEEP Menu finishes sweeping. Verify voltage is +10 VDC. Adjust R4331 on I/O INTERFACE PC Board for +10 VDC, if necessary.

41. Set FM/AM-1500 Controls as follows:

CONTROL	SETTING
(18) DUPLEX/SIMPLEX	"DUPLEX"
(19) GEN/REC	"GEN"
(21) LCD	860.2000 MHz

42. Connect external Spectrum Analyzer to DUPLEX OUTPUT Connector (16). Set Spectrum Analyzer to 10 MHz/DIV at 860.4 MHz center frequency.

43. Select both (+) and (-) 45 MHz OFFSET on LCD (21), and verify while rotating RF Level Output Control (10) from -10 to -80 dBm that:

    a. RF output level on Spectrum Analyzer is within 2 dB of RF Output Level over the range.

    b. Spurs on signal with -45 MHz OFFSET applied are 60 dBc or lower within +35 MHz to +55 MHz of carrier.

    c. Spurs on signal with +45 MHz OFFSET applied are 40 dBc or lower within -35 MHz to -55 MHz of carrier.

4-7-2 DUPLEX OFFSET CALIBRATION

SPECIAL ACCESSORY EQUIPMENT REQ'D: 1 Spectrum Analyzer – Capable of measuring 230 MHz at -4 dBm

FIGURE REFERENCES: FM/AM-1500 Interconnect (Figure 7-1)

DUPLEX OFFSET Mechanical Assembly (Figure 6-30)

TEST SET-UP DIAGRAM: N/A

STEP PROCEDURE

1. Set FM/AM-1500 Controls as follows:

CONTROL	SETTING
(13) PWR/OFF	"PWR"
(18) DUPLEX/SIMPLEX	"DUPLEX"
(19) GEN/REC	"GEN"
(21) LCD	00.00 MHz OFFSET

2. Using an external Spectrum Analyzer and an SMB to SMB tee, measure output level at J3201 on DUPLEX OFFSET Module. Verify level is -8 to -4 dBm at 180 MHz. Note and record level.

3. While observing external Spectrum Analyzer, verify all keypad digits from 00.00 to 49.99 operate in both plus and minus and that the output frequency steps from +49.99 MHz to -49.99 MHz on either side of 180 MHz as follows:

LCD (21) Setting	Displayed RF
-49.99 MHz OFFSET	229.99 MHz
-48.88 MHz OFFSET	228.88 MHz
-47.77 MHz OFFSET	227.77 MHz
-46.66 MHz OFFSET	226.66 MHz
-45.55 MHz OFFSET	225.55 MHz
-44.44 MHz OFFSET	224.44 MHz
-33.33 MHz OFFSET	213.33 MHz
-22.22 MHz OFFSET	202.22 MHz
-11.11 MHz OFFSET	191.11 MHz
00.00 MHz OFFSET	180.00 MHz
+11.11 MHz OFFSET	168.89 MHz
+22.22 MHz OFFSET	157.78 MHz
+33.33 MHz OFFSET	146.67 MHz
+44.44 MHz OFFSET	135.56 MHz
+45.55 MHz OFFSET	134.45 MHz
+46.66 MHz OFFSET	133.34 MHz
+47.77 MHz OFFSET	132.23 MHz
+48.88 MHz OFFSET	131.12 MHz
+49.99 MHz OFFSET	130.01 MHz

STEP	PROCEDURE

4. Set GEN/REC Switch (19) to "REC".

5. Observe displayed signal on external Spectrum Analyzer. Verify RF level is at least 50 dB below level noted and recorded in Step 2.

6. Disconnect all test equipment and reconnect all removed coax cables.

4-7-3 DUAL TONE GENERATOR CALIBRATION

SPECIAL ACCESSORY EQUIPMENT REQ'D:
- 1 Oscilloscope – Any
- 1 Distortion Analyzer – Capable of measuring distortion at 20 kHz
- 1 150Ω, 1/4 W Resistor
- 1 Frequency Counter – Capable of reading 66 kHz

FIGURE REFERENCES: Dual Tone Generator PC Board (Figure 6-34)

TEST SET-UP DIAGRAM: N/A

STEP PROCEDURE

1. Set FM/AM-1500 controls as follows:

CONTROL	SETTING
(13) PWR/OFF	"PWR"
(20) Keyboard	1000.0 Hz, TONE 1 Readout
(31) TONE 2	Fully ccw
(33) TONE 1	Fully cw

2. Load the TONES OUTPUT Connector (27) with a 150Ω, 1/4 W Resistor.

NOTE

Make a connector box for Resistor and put a BNC tee on the output as shown in Appendix D.

3. Connect external Oscilloscope to one side of BNC tee.
4. Connect external Distortion Analyzer to other side of BNC tee.
5. Verify sine wave output level is ≥7.1 Vp-p.
6. Verify audio distortion is ≥0.7% at 1000 Hz.
7. Select 10000.0 Hz TONE 1 on LCD (21).
8. Disconnect Oscilloscope and connect Frequency Counter in its place. Verify output frequency is 10,000 Hz (±1 Hz). If not, adjust trimcap C4505 on DUAL TONE GENERATOR PC Board.
9. Select 2000.0 Hz TONE 1 on LCD (21).
10. Verify audio distortion is within 0.7% at 20,000 Hz.
11. Select 50.0 Hz TONE 1 on LCD (21).
12. Verify audio distortion is <2% at 50 Hz.

STEP	PROCEDURE

13. Set FM/AM-1500 controls as follows:

CONTROL	SETTING
(21) Keyboard	50.0 Hz TONE 2 Readout
(31) TONE 2	Fully cw
(33) TONE 1	Fully ccw

14. Verify audio distortion is <2% at 50 Hz.

15. Select 20000.0 Hz TONE 2 on LCD (21).

16. Verify audio distortion is <0.7% at 20,000 Hz.

17. Select 1000.0 Hz TONE 2 on LCD (21).

18. Verify audio distortion is <0.7% at 1000 Hz.

19. Select each of the following frequencies and verify output frequency is equal (±0.1 Hz) to selected frequency.

TONE 2 on LCD (21)

409.6 Hz	416.0 Hz
409.7 Hz	422.4 Hz
409.9 Hz	435.2 Hz
410.0 Hz	460.8 Hz
410.4 Hz	512.0 Hz
411.2 Hz	614.4 Hz
412.8 Hz	

20. Select each of the following frequencies and verify output frequency is equal (±0.01%) to selected frequency.

TONE 2 on LCD (21)

2048 Hz	16384 Hz
4096 Hz	32768 Hz
8192 Hz	65536 Hz

21. Rotate TONE 1 Control (33) fully cw and rotate TONE 2 Control (31) fully ccw.

22. Select each of the following frequencies and verify output frequency is equal (±0.01%) to selected frequency.

TONE 1 on LCD (21)

2048 Hz	16384 Hz
4096 Hz	32768 Hz
8192 Hz	65536 Hz

23. Select the following frequencies and verify output frequency is equal (±0.1 Hz) to selected frequency.

TONE 1 on LCD (21)

409.6 Hz
409.7 Hz
409.9 Hz
410.0 Hz

24. Disconnect all test equipment.

4-8 SPECTRUM ANALYZER FUNCTIONAL BLOCK

4-8-1 SPECTRUM ANALYZER

SPECIAL ACCESSORY EQUIPMENT REQ'D:
1 Spectrum Analyzer – Capable of measuring 500 MHz at -30dBm

1 RF Generator – Capable of generating 1000 MHz at -30dBm

FIGURE REFERENCES:
FM/AM-1500 Interconnect (Figure 7-1)

Spectrum Analyzer LO Mechanical Assembly (Figure 6-36)

Spectrum Analyzer IF Mechanical Assembly (Figure 6-35)

Generator Mixer Mechanical Assembly (Figure 6-28)

Spectrum Analyzer RF Mechanical Assembly (Figure 6-37)

89-90 MHz Receiver Mechanical Assembly (Figure 6-24)

TEST SET-UP DIAGRAM: N/A

STEP PROCEDURE

1. Set FM/AM-1500 Controls as follows:

CONTROL	SETTING
(19) GEN/REC	"REC"
(21) Keyboard	120.2000 MHz (LCD FREQUENCY Readout)
(38) ANALY DISPR	"1 M"
(48) dB/DIV	"10 dB/DIV"
(49) ANAL V	Center pot
(51) DISPLAY	"ANALY"
(53) ANAL H	Center pot

2. Using external Oscilloscope, observe voltage on pin 5 of J4603 on Spectrum Analyzer LO Module. Adjust ANAL H Adjustment (53) on front panel for a voltage indication within 0.3 VDC from ground.

3. Observe base line sweep on CRT. Adjust R3560 (HORIZ GAIN) on Spectrum Analyzer LO Module until sweep ends 5.2 major divisions to the left of the major vertical axis.

4. Adjust R3547 (SYMMETRY) on Spectrum Analyzer LO Module to center trace equally on both sides of major vertical axis.

5. Repeat Steps 3 and 4 until no further adjustment is necessary.

6. Connect an RF Generator set at 1000 MHz, -30 dBm, to ANTENNA Connector (56).

7. Set LCD (21) to 500.0000 MHz and rotate ANALY DISPR Control (38) to "FULL".

8. Verify 1000 MHz signal on CRT is five major divisions to the right of the major vertical axis and that the 0 MHz signal is five major divisions (-1 minor division, +1.5 minor divisions) to the left of the major vertical axis. Adjust R3601 (WIDE DISPR) on Spectrum Analyzer LO Module for correct location of 1000 MHz signal.

NOTE

If it is necessary to adjust R3601, it may be necessary to repeat Steps 2 thru 5 to readjust centering and symmetry.

9. Set output frequency of RF Generator to 500.2 MHz at -30 dBm.

10. Rotate ANALY DISPR Control (38) to "10 M". Set LCD (21) to 510.2000 MHz. Verify displayed signal on CRT is 1 major division (±1 minor division) to the left of the major vertical axis.

11. Rotate ANALY DISPR Control (38) to "5 M". Set LCD (21) to 505.2000 MHz. Verify displayed signal on CRT is 1 major division (±1 minor division) to the left of the major vertical axis.

12. Rotate ANALY DISPR Control (38) to "2 M". For the following frequencies, verify signal on CRT is within 1.5 minor divisions of the major vertical axis.

LCD (21) FREQUENCY	RF Generator Setting
999.9999 MHz	1000 MHz
700.0000 MHz	700 MHz
000.0000 MHz	No RF

13. Set LCD (21) to 500.2000 MHz. Set RF Generator to 500.2000 MHz at -40 dBm. Rotate ANALY DISPR Control (38) to "1 M". Adjust R3529 (FREQ CENTER) on Spectrum Analyzer LO Module until displayed signal is centered on major vertical axis of CRT.

14. Set RF Generator to 497 MHz and then to 503 MHz. Verify displayed signal on CRT is centered, first, on the third major division to the left, and likewise to the right, of the major vertical axis. Adjust R3567 (NARROW DISPERSION) on Spectrum Analyzer LO Module for proper centering.

15. For the following RF Generator frequencies and ANALY DISPR Control settings, verify displayed signal on CRT is centered on the third major division to the left, and likewise to the right of the major vertical axis.

ANALY DISPR (38) Setting	Tolerance Minor Divisions	RF Generator Setting (MHz)	
.5 M	±1	501.5	498.5
.2 M	±1	500.6	499.4
.1 M	±1	500.3	499.7
20 K	±1	500.06	499.04
10 K	±1	500.03	499.07
2 K	±7	500.006	499.004
1 K	±7	500.003	499.007

NOTE

Adjust R3615 (300 Hz BW ANALY CNTR) as needed to center tolerance (3 minor divisions) to the dispersion settings at 2K and 1K. After completing narrow dispersion checks, repeat Steps 6 through 12 to recheck Wide Dispersion centering.

16. Rotate ANALY DISPR Control (38) to "1 M".

17. Disconnect RF Generator from ANTENNA Connector (56). Set RF Generator to 10.7 MHz at -20 dBm. Disconnect P5401 from J5401 on the Spectrum Analyzer IF Module. Connect RF Generator to J5401.

18. Connect an external Spectrum Analyzer to Test Point 2 (TP2) on Spectrum Analyzer IF Module. Adjust R3938 (30 kHz BW GAIN) on Spectrum Analyzer IF Module for a 2.5 MHz signal at -22 dBm at TP2.

NOTE

External Spectrum Analyzer must be equipped with a DC Block for Steps 18 and 19.

19. Rotate ANALY DISPR Control (38) to "2 M". Adjust R3919 (650 kHz BW GAIN) for a 2.5 MHz signal at -19 dBm at TP2.

20. Disconnect Spectrum Analyzer from TP2. Rotate ANALY DISPR Control (38) to ".1 M".

21. Set RF Generator to 0 MHz output. Adjust R3961 (BASE LINE) on Spectrum Analyzer IF Module until base line on CRT is on the -108 dB graticule.

22. Set RF Generator to 10.7 MHz at -30 dBm. Adjust R3959 (DETECTOR GAIN) until displayed signal on CRT is on the -40 dB graticule.

23. Set RF Generator to 10.7 MHz at -20 dBm. Adjust R3941 (LOG LIN) until displayed signal on CRT is on the -30 dB graticule.

STEP	PROCEDURE

24. Set RF Generator to 10.7 MHz at -70 dBm. Adjust R3942 (AMP 1 GAIN) until displayed signal on CRT is on the -80 dB graticule.

25. Set RF Generator to 10.7 MHz at -90 dBm. Adjust R3951 (AMP 2 GAIN) until displayed signal on CRT is on the -100 dB graticule.

26. While stepping the output level of the RF Generator from -20 dBm to -80 dBm, verify displayed signal on CRT steps from -30 dB to -90 dB and is within 2 dB of each selected graticule. If tolerance is not met at each step, repeat Steps 20 thru 26.

27. Set dB/DIV Switch (48) to "1". Rotate VERT POS Control (45) fully cw.

28. Set RF Generator to 10.7 MHz at -20 dBm. Adjust R3963 (OFFSET) until displayed signal on CRT is on the -20 dB graticule.

29. Set RF Generator to 10.7 MHz at -30 dBm. Adjust VERT POS Control (45) until displayed signal on CRT is on the top horizontal graticule.

30. Set RF Generator to 10.7 MHz at -38 dBm. Adjust R3969 (1 dBm/DIV GAIN) until displayed signal on CRT is on the bottom horizontal graticule.

31. Repeat Steps 28 thru 30 and verify a tolerance of 1 minor division can be met at each step without having to adjust the trimpots.

32. Disconnect P4403 from J4403 on GENERATOR Mixer Module. Connect external Spectrum Analyzer to J4403. Center signal on external Spectrum Analyzer at 90 MHz and set external Analyzer controls to 1 MHz/DIV and 1 ms/DIV sweep.

33. Rotate DISPLAY Control to "ANALY". Adjust R3412 (F1 FIXED) and R3423 (F2 FIXED) on GENERATOR MIXER Module for maximum gain of signal on external Spectrum Analyzer. Then adjust R3436 (OUTPUT) on GENERATOR MIXER Module for an output level of -11 to -16 dBm at 90 MHz.

34. Rotate DISPLAY Control to "ANALY". Adjust R3412 (F1 FIXED) and R3423 (F2 FIXED) on GENERATOR MIXER Module for maximum gain of signal on external Spectrum Analyzer. Then adjust R3436 (OUTPUT) on GENERATOR MIXER Module for an output level of -11 to -16 dBm at 90 MHz.

35. Observe external Spectrum Analyzer and verify sweep signal from 84 to 96 MHz is flat (within 1 dB). If not, adjust R3413 (F1 GAIN), R3415 (F1 OFFSET), R3417 (F2 GAIN) and R3421 (F2 OFFSET) on GENERATOR MIXER Module.

NOTE

The above mentioned resistors are interactive and may need repeated adjustments to obtain the correct signal.

STEP	PROCEDURE

36. Disconnect Spectrum Analyzer from J4403. Connect P4403 to J4403 on GENERATOR MIXER Module.

37. Using a BNC to BNC coax cable, connect ANTENNA Connector (56) to TRANS/-40 dB DUPLEX Connector (11). Rotate RF Output Level Control (10) to -40 dB.

38. Observe displayed signal on CRT. Adjust R3794 (TRACKING OFFSET) and R3791 (TRACKING GAIN) on Spectrum Analyzer RF Module for maximum level and flatness within 1 dB.

NOTE:

Ensure S3701 on Spectrum Analyzer RF Module is in "RUN" position (to the left, looking from outside of Module).

39. Select the entire range (0-9) of the 100 kHz digit on LCD (21). Verify displayed signal is flat (±1 dB) for entire range.

40. Disconnect TRANS/-40 dB DUPLEX Connector (11) from ANTENNA Connector (56). Connect ANTENNA Connector (56) to DUPLEX OUTPUT Connector (16).

41. Set FM/AM-1500 Controls as follows:

CONTROL	SETTING
(10) RF Output Level	-30 dBm
(18) DUPLEX/SIMPLEX	"DUPLEX"
(19) GEN/REC	"GEN"
(21) Keyboard	500.0000 MHz (LCD FREQUENCY Readout)
(38) ANALY DISPR	"10 K"
(51) DISPLAY	"ANALY"

42. Rotate ANALY DISPR Control (38) to "1 K". Adjust R3771 (300 kHz BW GAIN) on Spectrum Analyzer RF Module until signal level on CRT is on the -30 dB graticule.

43. Rotate ANALY DISPR Control (38) to "1 M". Adjust R3777 (650 kHz BW GAIN) on Spectrum Analyzer RF Module until signal level on CRT is on the -30 dB graticule.

44. Set ATTENUATOR Switch (55) to "20 dB". Verify signal level on CRT is on -50 dB graticule (±2 dB).

45. Set ATTENUATOR Switch (55) to "40 dB". Verify signal level on CRT is on -70 dB graticule (±2 dB).

46. Set ATTENUATOR Switch (55) to "0 dB". Rotate RF Output Level Control (10) to -30 dBm.

47. Rotate ANALY DISPR Control (38) to all settings except "2 K" and verify signal level on CRT is -30 dB (±2 dB) for each setting.

STEP	PROCEDURE

48. Set FM/AM-1500 Controls as follows:

CONTROL	SETTING
(7) MODULATION	"AM 1"
(21) LCD	500.0000 MHz 1000.0 Hz, TONE 1
(28) Tone 1 FM/OFF/AM	"AM"
(38) ANALY DISPR	"FULL"
(51) DISPLAY	"TRACK"

49. Disconnect ANTENNA Connector (56) from DUPLEX OUTPUT Connector (16). Connect ANTENNA Connector (56) to TRANS/-40 dB DUPLEX Connector (11).

50. Note the position of the carrier signal on CRT with TONE 1 Control (33) fully ccw. Verify, when TONE 1 Control (33) is rotated fully cw, the RF envelope peaks at least +6 dBc and -26 dBc.

51. Rotate TONE 1 Control (33) fully ccw. Rotate ANALY DISPR Control (38) to ".1 M". Select 000.0000 MHz on LCD (21). Disconnect ANTENNA Connector (56) from TRANS/-40 dB DUPLEX Connector (11). Adjust R9302 and R9303 in Mixer Null Module to put top of signal on CRT on the top graticule, or as near as possible.

52. Rotate ANALY DISPR Control (38) to "FULL". Select 500.0000 MHz on LCD (21). Connect ANTENNA Connector (56) to TRANS/-40 dB DUPLEX Connector (11).

53. Rotate TONE 1 Control (33) fully ccw. Set dB/DIV Switch (48) to "1". Verify tracking flatness on CRT ±4 dB (to 950 MHz), or within 6 dB above 950 MHz.

54. Rotate ANALY DISPR Control (38) to "10 M". Select 050.0000 MHz on LCD (21). Verify tracking flatness on CRT of ≤2 dB from 0 to 50 MHz.

55. Disconnect coax from ANTENNA Connector (56) and connect a BNC tee to ANTENNA Connector. Then connect coax to one side of tee. Connect an open length of coax to the other side of tee. Verify linear cable fault nulls across the band.

56. Disconnect open length of coax from tee.

57. Rotate RF Output Level Control (10) to -100 dBm and verify cross-talk noise does NOT appear on the base line on CRT.

58. Rotate DISPLAY Control (51) to "ANALY". Rotate ANALY DISPR Control (38) to "FULL".

59. Observe base line on CRT display. Verify a straight base line with no signal present.

60. Rotate ANALY DISPR Control (38) to "1 M". Note and record base line level.

STEP	PROCEDURE

61. Select 015.0000 MHz on LCD (21). Verify base line rises ≤2 dB from level in Step 63.

62. Select 005.0000 MHz on LCD (21). Verify base line rises ≤2 dB from 5 to 10 MHz and no extraneous signals are present.

63. Set FM/AM-1500 Controls as follows:

CONTROL	SETTING
(18) DUPLEX/SIMPLEX	"SIMPLEX"
(19) GEN/REC	"GEN"
(38) ANALY DISPR	"10 K"
(51) DISPLAY	"ANALY"

64. Rotate GEN/LOCK Control (35) from fully (-) (not in "LOCK") to fully (+). Verify signal on CRT shifts at least ±10 kHz on each side of center frequency.

65. Rotate GEN/LOCK Control (35) to "LOCK". Verify signal level on CRT is between -35 and -65 dBm.

66. Disconnect all test equipment.

4-9 MICROPROCESSOR FUNCTIONAL BLOCK

There are no adjustments on the CPU/MEMORY PC Board. There are four adjustments on the I/O Interface PC Board: R4350, R4354, R4331 and R4333. R4350 and R4354 are adjusted during RECEIVER SIGNAL calibration (4-6-1). R4331 and R4333 are adjusted during RF OUTPUT POWER calibration (4-7-1).

MAINTENANCE MANUAL

FM/AM-1500

COMMUNICATIONS SERVICE MONITOR

10200 West York Street/Wichita, Kansas 67215 U.S.A./(316)522-4981/TWX 910-741-6952

1002-5001-100
04

PUBLISHED BY
IFR SYSTEMS, INC.
Wichita, Kansas

SYSTEMS, INC.

TO: HOLDERS OF THE FM/AM-1500 MAINTENANCE MANUAL (1002-5001-100)

The pages contained in Revision 5 are listed below. Please remove and insert affected pages in the FM/AM-1500 Maintenance Manual.

REMOVE PAGES	INSERT PAGES
List of Effective Pages, Page A	List of Effective Pages, Page A
List of Effective Pages, Page B	List of Effective Pages, Page B
Table of Contents, Page vi	Table of Contents, Page vi
Table of Contents, Page vii	Table of Contents, Page vii
List of Illustrations, Page xi	List of Illustrations, Page xi
Section 4 - Calibration, 4-1 thru 4-62	Section 4 - Calibration, 4-1 thru 4-62

LIST OF EFFECTIVE PAGES

The manual pages listed below which are affected by a current change or revision, are so identified by a revision number and an asterisk.

Date of issue for original and changed pages are:

Original	0	February 15, 1986
Revision	1	September 15, 1986
Revision	2	May 15, 1987
Revision	3	February 1, 1988
Revision	4	June 15, 1989
Revision	5	December 15, 1991

TOTAL NUMBER OF PAGES IN THIS MANUAL IS 532 CONSISTING OF THE FOLLOWING:

Pg. No.	Change No.	Pg. No.	Change No.
Title Page	0	2-45	4
Copyright Page	4	2-46	0
Warning Page	0	2-47 thru 2-48	4
Caution Page	0	2-49	0
A thru C	4	2-50	3
D Blank	3	2-51 thru 2-54	0
i thru iii	0	2-55	4
iv thru 1-2	4	2-56 thru 2-59	1
1-3 thru 1-4	3	2-60	4
2-1	4	2-61	0
2-2	2	2-62	4
2-3	3	2-63	1
2-4 thru 2-5	4	2-64 thru 2-66	4
2-6 thru 2-7	0	2-67	0
2-8 thru 2-11	4	2-68 thru 2-70	4
2-12	0	2-71 thru 2-72	1
2-13	4	2-73 thru 2-76	4
2-14 thru 2-18	0	2-77 thru 2-78	0
2-19 thru 2-21	4	2-79	4
2-22 thru 2-23	0	2-80	0
2-24 thru 2-27	4	2-81 thru 2-84	4
2-28	0	2-85	0
2-29 thru 2-33	4	2-86 thru 3-3	4
2-34	0	3-4	0
2-35	4	3-5	4
2-36	0	3-6	0
2-37	4	3-7	4
2-38 thru 2-44	0	3-8 Blank	0

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3-11 thru 3-15	4
3-16 Blank	0
3-17 thru 3-19	4
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3-21 thru 3-23	4
3-24 Blank	0
3-25	4
3-26 Blank	0
3-27 thru 3-34	4
3-35 thru 3-36	0
3-37 thru 3-43	4
3-44 Blank	0
3-45 thru 3-46	4
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4-1 thru 4-2	5
4-3 thru 4-4 Blank	0
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5-13 thru 5-14	4
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5-21 thru 5-25	4
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5-36 thru 5-37	0
5-38 thru 5-41	4
5-42	1
5-43	4
5-44	0
5-45	4
5-46	0
5-47	4

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5-49	0
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5-53	0
5-54 thru 5-55	4
5-56	1
5-57	4
5-58	0
5-59	4
5-60	0
5-61	4
5-62	0
5-63 thru 5-64	4
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5-66	3
5-67 thru 5-76	0
6-1 thru 6-2	0
6-3 thru 6-4	3
6-5 thru 6-6	1
6-7	3
6-8	1
6-9	0
6-10 thru 6-12	4
6-13	3
6-14	2
6-15	4
6-16	0
6-17	3
6-18 thru 6-23	4
6-24	3
6-25 thru 6-28	0
6-29 thru 6-30	4
6-31 thru 6-32	0
6-33	4
6-34	3
6-35 thru 6-38	4
6-39	3
6-40	4
6-41	3
6-42 thru 6-43	4
6-44 thru 6-45	3
6-46 thru 6-47	4
6-48	3
6-49 thru 6-50	4
6-51 Blank	4
6-51a thru 6-51b	4

WARNING:

HIGH VOLTAGE EQUIPMENT

THIS EQUIPMENT CONTAINS CERTAIN CIRCUITS AND/OR COMPONENTS OF EXTREMELY HIGH VOLTAGE POTENTIALS, CAPABLE OF CAUSING SERIOUS BODILY INJURY OR DEATH. WHEN PERFORMING ANY OF THE PROCEDURES CONTAINED IN THIS MANUAL, HEED ALL APPLICABLE SAFETY PRECAUTIONS.

RESCUE OF SHOCK VICTIMS

1. DO NOT ATTEMPT TO PULL OR GRAB THE VICTIM
2. IF POSSIBLE, TURN OFF THE ELECTRICAL POWER.
3. IF YOU CANNOT TURN OFF ELECTRICAL POWER, PUSH, PULL OR LIFT THE VICTIM TO SAFETY USING A WOODEN POLE, A ROPE OR SOME OTHER DRY INSULATING MATERIAL.

FIRST AID

1. AS SOON AS VICTIM IS FREE OF CONTACT WITH SOURCE OF ELECTRICAL SHOCK, MOVE VICTIM A SHORT DISTANCE AWAY FROM SHOCK HAZARD.
2. SEND FOR DOCTOR AND/OR AMBULANCE.
3. KEEP VICTIM WARM, QUIET AND FLAT ON HIS/HER BACK.
4. IF BREATHING HAS STOPPED , ADMINISTER ARTIFICIAL RESUSCITATION. STOP ALL SERIOUS BLEEDING.

CAUTION

INTGRATED CIRCUITS AND SOLID STATE DEVICES SUCH AS MOS FET'S, ESPECIALLY CMOS TYPES, ARE SUSCEPTIBLE TO DAMAGE BY ELECTROSTATIC DISCHARGES RECEIVED FROM IMPROPER HANDLING, THE USE OF UNGROUNDED TOOLS, AND IMPROPER STORAGE AND PACKAGING. ANY MAINTENANCE TO THIS UNIT MUST BE PERFORMED WITH THE FOLLOWING PRECAUTIONS:

1. BEFORE USE IN A CIRCUIT, KEEP ALL LEADS SHORTED TOGETHER EITHER BY THE USE OF VENDOR-SUPPLIED SHORTING SPRINGS OR BY INSERTING LEADS INTO A CONDUCTIVE MATERIAL.

2. WHEN REMOVING DEVICES FROM THEIR CONTAINERS, GROUND THE HAND BEING USED WITH A CONDUCTIVE WRISTBAND.

3. TIPS OF SOLDERING IRONS AND/OR ANY TOOLS USED MUST BE GROUNDED.

4. DEVICES MUST NEVER BE INSERTED INTO NOR REMOVED FROM CIRCUITS WITH POWER ON.

5. PC BOARD, WHEN TAKEN OUT OF THE SET, MUST BE LAID ON A GROUNDED CONDUCTIVE MAT OR STORED IN A CONDUCTIVE STORAGE BAG.

NOTE

Remove any built-in power source, such as a battery, before laying PC Boards on conductive mat or storing in conductive bag.

6. PC BOARDS, IF BEING SHIPPED TO THE FACTORY FOR REPAIR, MUST BE PACKAGED IN A CONDUCTIVE BAG AND PLACED IN A WELL-CUSHIONED SHIPPING BOX.

CAUTION

THE USE OF SIGNAL GENERATORS FOR MAINTENANCE AND OTHER ACTIVITIES CAN BE A SOURCE OF ELECTROMAGNETIC INTERFERENCE TO AVIATION RECEIVERS, WHICH CAN CAUSE DISRUPTION AND INTERFERENCE TO AERONAUTICAL SERVICE OUT TO A DISTANCE OF SEVERAL MILES.

USERS OF THIS EQUIPMENT SHOULD SCRUTINIZE ANY OPERATION WHICH RESULTS IN RADIATION OF A SIGNAL (DIRECTLY OR INDIRECTLY) AND SHOULD TAKE NECESSARY PRECAUTIONS TO AVOID POTENTIAL COMMUNICATION INTERFERENCE PROBLEMS.

LIST OF EFFECTIVE PAGES

The manual pages listed below which are affected by a current change or revision, are so identified by a revision number and an asterisk.

Date of issue for original and changed pages are:

Original ..... 0 ..... February 15, 1986
Revision ..... 1 ..... September 15, 1986
Revision ..... 2 ..... May 15, 1987
Revision ..... 3 ..... February 1, 1988
Revision ..... 4 ..... June 15, 1989

TOTAL NUMBER OF PAGES IN THIS MANUAL IS 532 CONSISTING OF FOLLOWING:

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D Blank	3
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*iv thru xvi	4
*1-1 thru 1-2	4
1-3 thru 1-4	3
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3-10 Blank	0
*3-11 thru 3-15	4
3-16 Blank	0
*3-17 thru 3-19	4
3-20	0
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6-44b thru 6-45	3
*6-46 thru 6-47	4
6-48	3
*6-49 thru 6-50	4
*6-51 Blank	4
*6-51a thru 6-51b	4

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7-1	3
*7-2	4
*7-2a	4
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*7-3 thru 7-5	4
7-6 thru 7-10	3
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*7-24b Blank	4
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7-30 thru 7-31	3
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7-33	3
*7-34	4
7-35 thru 7-36	3
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7-38 thru 7-49	3
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F-2	0
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G-2 Blank	0
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H-2	3
J-1 thru J-2	0
K-1	0
K-2	1
K-3	1
K-4 Blank	1

C/D Blank

PREFACE

SCOPE

This manual contains maintenance instructions for the FM/AM-1500 Communication Service Monitor. The information in this manual will enable the technician to:

1. Service, test, repair or replace any major assembly or module within the test set.

2. Maintain the operating condition of the set to expected performance standards.

3. Understand the principles of operation as they relate to the overall operation of the set, as well as to individual circuits.

ORGANIZATION

The contents of this manual are divided into the following major sections

SECTION 1 - INTRODUCTION

Provides a brief description of the electrical and mechanical configuration of the FM/AM-1500, intended to familiarize the technician with the overall structure of the set.

SECTION 2 - THEORY OF OPERATION

Describes the FM/AM-1500 circuit theory on the system, functional and detailed levels, based on accompanying block diagrams.

SECTION 3 - PERFORMANCE EVALUATION

Contains "covers on" functional checkout procedures for evaluating the performance of the FM/AM-1500.

SECTION 4 - CALIBRATION

Contains step by step calibration and alignment procedures for use during normal calibration intervals or when replacement parts are installed in the FM/AM-1500.

SECTION 5 - TROUBLESHOOTING

Contains step by step troubleshooting recommendations for use in isolating fault conditions within the major electrical circuits.

SECTION 6 - MECHANICAL ASSEMBLIES/PC BOARDS

Contains mechanical assembly drawings of all assemblies and PC Boards within the FM/AM-1500.

SECTION 7 - SCHEMATICS

Contains FM/AM-1500 interconnect diagrams and circuit schematics.

SECTION 8 - GPIB OPTION

Contains theory, performance test, calibration, troubleshooting, assembly drawing and schematic information on the GPIB Option as installed in the FM/AM-1500.

SECTION 9 - CELLULAR OPTION

Contains theory, performance test, calibration, troubleshooting, assembly drawing and schematic information on the Cellular Option as installed in the FM/AM-1500.

APPENDICES

Contain useful supplementary maintenance and operational data.

CORRECTIVE MAINTENANCE PROCEDURE

The Corrective Maintenance Flowchart shown in Figure i is intended to serve as a guide in directing the technician through the trouble-shooting/repair process. By observing this general sequence, the technician will be able to use the procedures within this manual to return the FM/AM-1500 to normal operation.

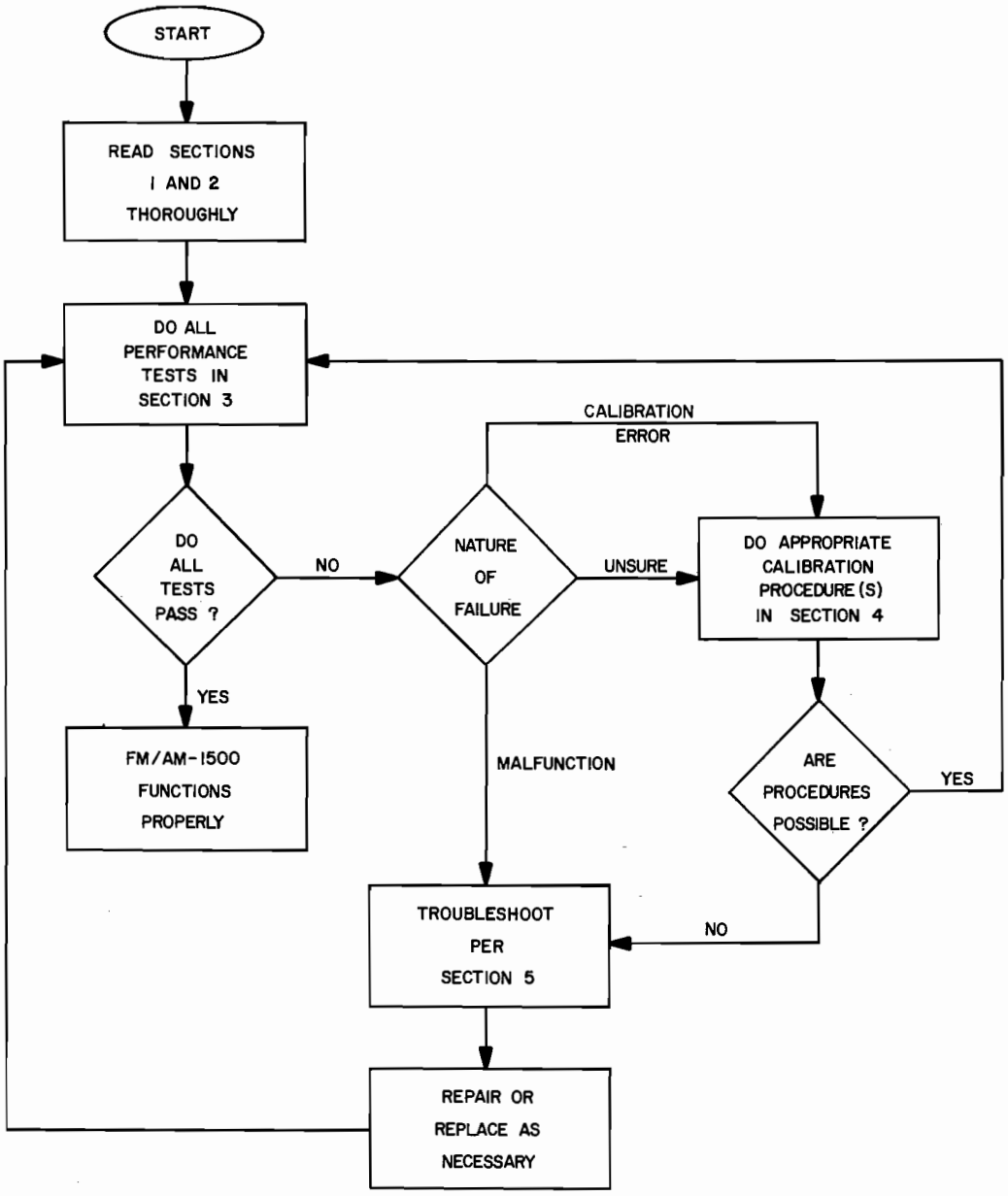

Figure i Corrective Maintenance Flowchart

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SECTION 1 - INTRODUCTION

1-1 GENERAL

This section provides a brief description of the internal electrical and mechanical configuration of the FM/AM-1500. An "exploded" composite drawing of the FM/AM-1500 is provided in Figure 1-1 to aid the technician in identifying and locating the major assemblies and modules which comprise the set.

1-2 ELECTRICAL DESCRIPTION

The FM/AM-1500 is a microprocessor-controlled, digitally synthesized communications service monitor. The signal generator is capable of generating modulated or unmodulated carrier signals within a range of 100 kHz to 999.9999 MHz (in 100 Hz steps), at a continuously variable output level of 0 to -128 dBm.

NOTE

+20 dBm output may be achieved with an optional High Output Amplifier which attaches to the TRANS/-40 dB DUPLEX Connector (11) on the front panel.

The receiver is a quadruple conversion, super-heterodyne type, capable of monitoring communications signals within a range of 300 kHz to 999.9999 MHz (in 100 Hz steps). The individual modules which make up each major circuit are listed in Table 1-1.

POWER DISTRIBUTION CIRCUITS
Power Supply
+40 V Power Supply

FREQUENCY STANDARD CIRCUITS
Clock Divider
TCXO (optional)
Oven Oscillator (optional)

FREQUENCY SYNTHESIS CIRCUITS
High Loop
Dual VCO
Low Pass Filter
High/Low Pass Filter
Delay Line
Buffer Amplifiers A & B
Low Loop
Low Loop Mixer

RECEIVER CIRCUITS
1300 MHz IF Receiver
89-90 MHz Receiver
Demod Audio PC Board
Ocilloscope Control & Deflection PC Board

GENERATOR CIRCUITS
FM Generator
Generate Mixer
1300 MHz IF Generator
Output Amplifier
Duplex Offset
Power Termination
Dual Tone Generator
High Output Amplifier (Optional)

NOTE: Thru Ser. No. 1406, a Diode Switch was included in the Receiver Circuit. Ser. No. 1407 and on, Diode Switch is part of the 1300 MHz Receiver Module.

SPECTRUM ANALYZER CIRCUITS
Spectrum Analyzer LO
Spectrum Analyzer RF
Spectrum Analyzer IF

MICROPROCESSOR CIRCUITS
CPU/Memory PC Board
I/O Interface PC Board

Table 1-1 FM/AM-1500 Major Electrical Systems

1-3 MECHANICAL DESCRIPTION

Mechanically, the FM/AM-1500 consists of the major groupings listed in Table 1-2. Refer to Figure 1-1 for location of each module.

CASE ASSEMBLY

UPPER FLOOR MODULES

1300 MHz IF Receiver	Output Buffers
1300 MHz IF Generator	High/Low Pass Filter
Output Amplifier	Low Pass Filter
Generate/Mixer	TCXO (optional)
Dual VCO	

REAR PANEL MODULES

Power Supply	+40 V Power Supply
Power Termination	Batteries
Oven Oscillator (optional)	GPIB Interface (optional)

MOTHER BOARD MODULES

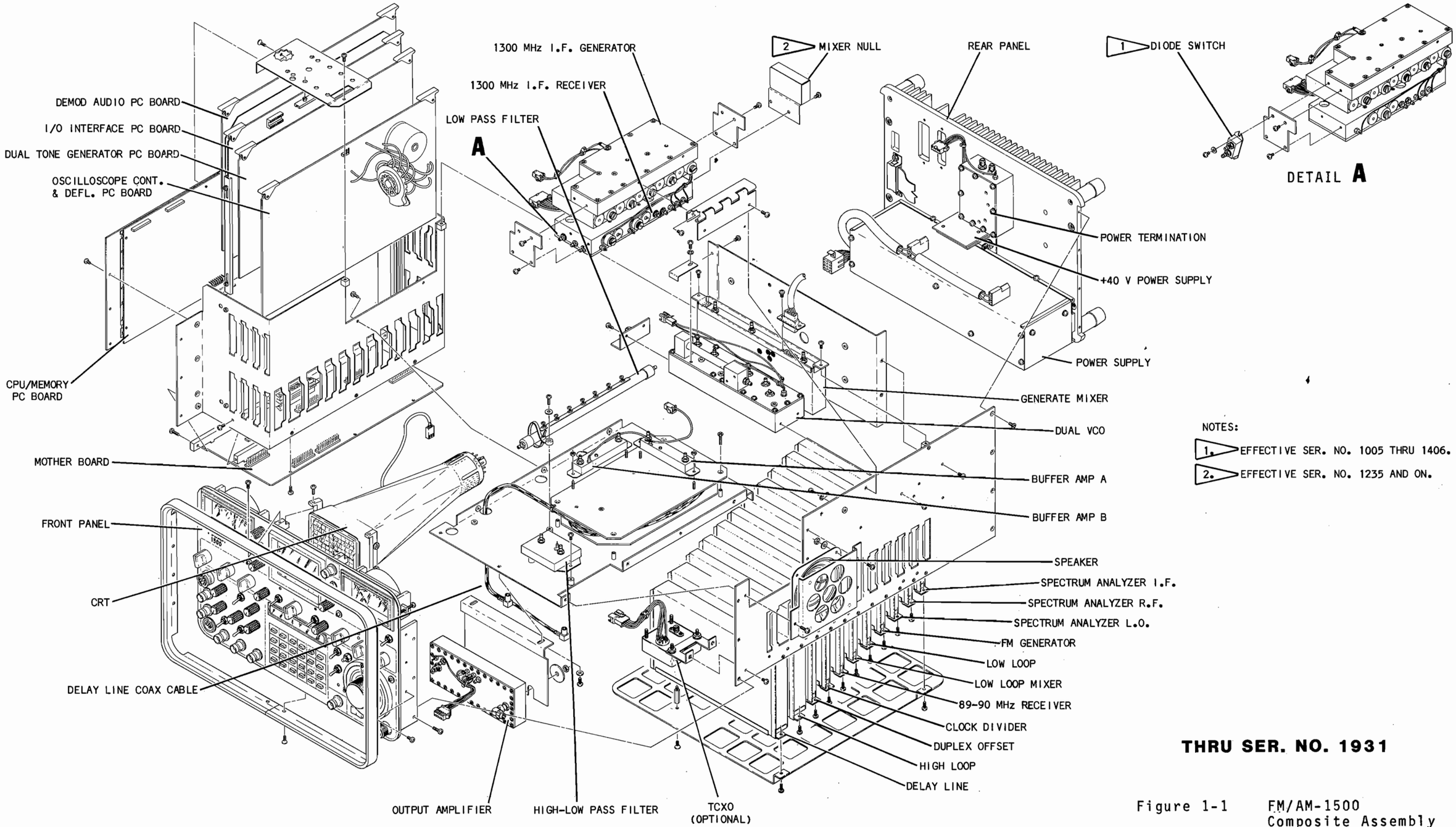
I/O Interface PC Bd.	Demod Audio PC Bd.
Osc. Cont. & Defl. PC Bd.	Dual Tone Generator PC Bd.
CPU/Memory PC Bd.	

LOWER FLOOR MODULES

S/A L.O.	High Loop
S/A I.F.	Low Loop
S/A R.F.	Clock Divider
89-90 MHz Receiver	Delay Line
	Low Loop Mixer
	FM Generator
	Duplex Offset

Note: Thru Ser. No. 1406, a Diode Switch was included in the Upper Floor Modules. Ser. No. 1407 and on, the Diode Switch is part of the 1300 MHz Receiver Module.

Table 1-2 FM/AM-1500 Mechanical Structure

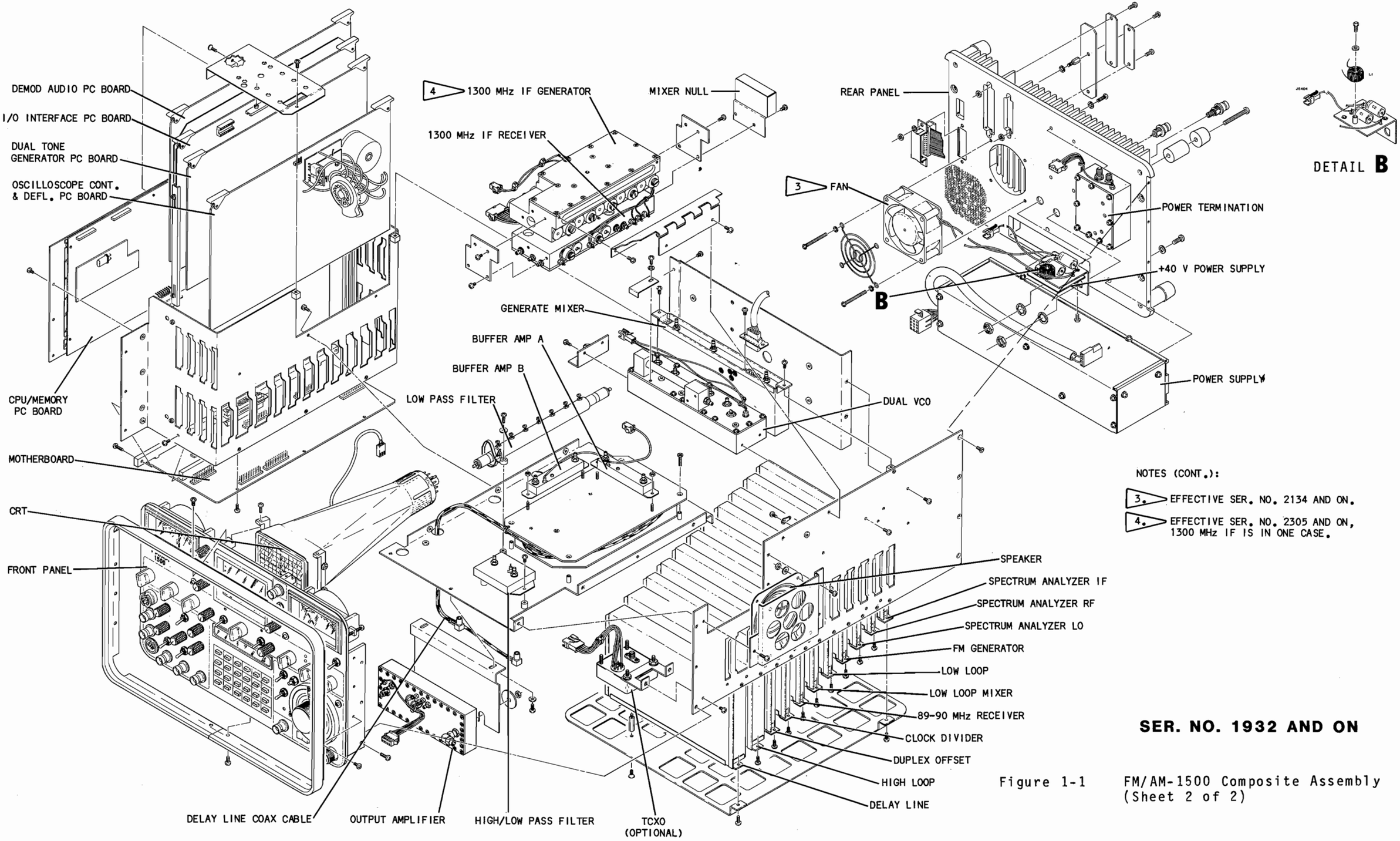


NOTES:

1. EFFECTIVE SER. NO. 1005 THRU 1406.
2. EFFECTIVE SER. NO. 1235 AND ON.

THRU SER. NO. 1931

Figure 1-1 FM/AM-1500 Composite Assembly (Sheet 1 of 2)



NOTES (CONT.):

3. EFFECTIVE SER. NO. 2134 AND ON.

4. EFFECTIVE SER. NO. 2305 AND ON, 1300 MHz IF IS IN ONE CASE.

SER. NO. 1932 AND ON

Figure 1-1 FM/AM-1500 Composite Assembly (Sheet 2 of 2)

SECTION 2 - THEORY OF OPERATION

2-1 GENERAL

This section contains three levels of Theory of Operation and is organized as follows:

1. SYSTEM THEORY OF OPERATION

   Paragraph 2-2 provides a simplified description of signal flow through the FM/AM-1500, for both signal generator and receiver operation. This description is based on the System Block Diagram shown in Figure 2-1.

2. FUNCTIONAL AND DETAILED THEORY OF OPERATION

   Paragraphs 2-3 thru 2-9 provide a description of the major functional groupings in the FM/AM-1500. Following each discussion of a major function are detailed discussions of each module contained in the functional group just discussed. All functional groups are accompanied by block diagrams, as are the individual modules (where necessary).

2-2 SYSTEM THEORY OF OPERATION

2-2-1 GENERAL

The FM/AM-1500 is a microprocessor controlled, digitally synthesized communications service monitor. The receiver is a quadruple conversion, superheterodyne receiver, capable of monitoring communications signals within a range of 300 kHz to 999.9999 MHz. The signal generator is capable of generating modulated or unmodulated carrier signals within the range of 100 kHz to 999.9999 MHz, at an output level which is continuously variable from 0 to -128 dBm. (The output level may be increased up to +20 dBm with the use of an optional High Output Amplifier.) See Figure 2-1, FM/AM-1500 System Block Diagram.

2-2-2 RECEIVER OPERATION

The frequency of the signal to be received is determined by the FREQUENCY MHz setting of the LCD on the front panel. The input signal can be received at the TRANS/-40 dB DUPLEX Connector or at the ANTENNA Connector. If applied at the ANTENNA Connector, the received signal is sent to the 1300 MHz IF Receiver Module to begin up-conversion. If applied at the TRANS/-40 dB DUPLEX Connector, the received signal (if 100 mW or greater) is sent to the 1300 MHz IF Receiver Module at a -40 dB level.

In the 1300 MHz IF Receiver, the received signal is mixed with a VCO signal to produce a 1st IF of 1300 MHz. The signal is filtered and amplified, before again being mixed with a VCO signal to produce a 2nd IF of 90 MHz.

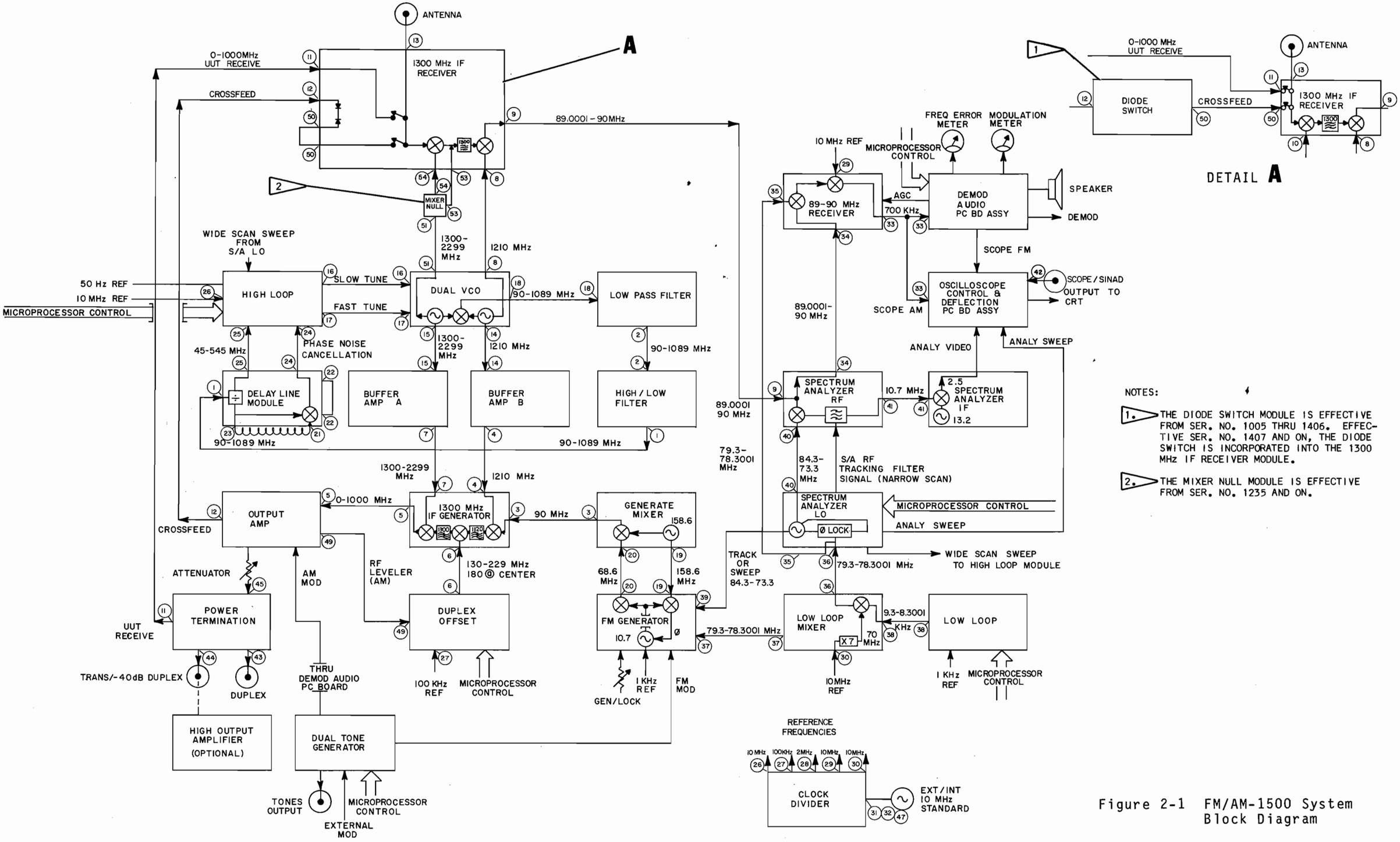
The 2nd IF is sent to the 89-90 MHz receiver and mixed with a Low Loop signal to produce a 10.7 MHz 3rd IF signal. The 3rd IF is mixed with a 10 MHz reference signal to produce the 4th IF of 700 kHz, which is fed to the audio processing portions of the set for demodulation and display on meters and readouts.

2-2-3 GENERATOR OPERATION

The frequency of the signal to be generated is determined by the FREQUENCY MHz setting of the LCD on the front panel. Signal Generation begins in the FM Generator, where an IF source signal, from either the Spectrum Analyzer LO or from the Low Loop, is mixed with a 10.7 MHz VCO signal to form a 1st IF of approximately 68.6 MHz. The 1st IF is mixed and converted, in the Generate Mixer, to a 90 MHz 2nd IF signal.

The 2nd IF is converted three times in the 1300 MHz IF Generator Module: first, to 1120 MHz, by mixing with a 1210 MHz High Loop signal; second, to 1250 to 1350 MHz by mixing with a 180 MHz injection frequency, which can be offset ±49.99 MHz to create a generate duplex offset; and third, to 0-1000 MHz output signal by mixing with a 1300 to 2299 MHz High Loop signal.

The output signal is routed through the Output Amp and Power Termination Modules. It is output at the TRANS/-40 dB DUPLEX Connector and/or DUPLEX OUTPUT Connector, depending on mode of operation.



NOTES:

1. THE DIODE SWITCH MODULE IS EFFECTIVE FROM SER. NO. 1005 THRU 1406. EFFECTIVE SER. NO. 1407 AND ON, THE DIODE SWITCH IS INCORPORATED INTO THE 1300 MHz IF RECEIVER MODULE.

2. THE MIXER NULL MODULE IS EFFECTIVE FROM SER. NO. 1235 AND ON.

Figure 2-1 FM/AM-1500 System Block Diagram

2-3 POWER DISTRIBUTION FUNCTIONAL THEORY

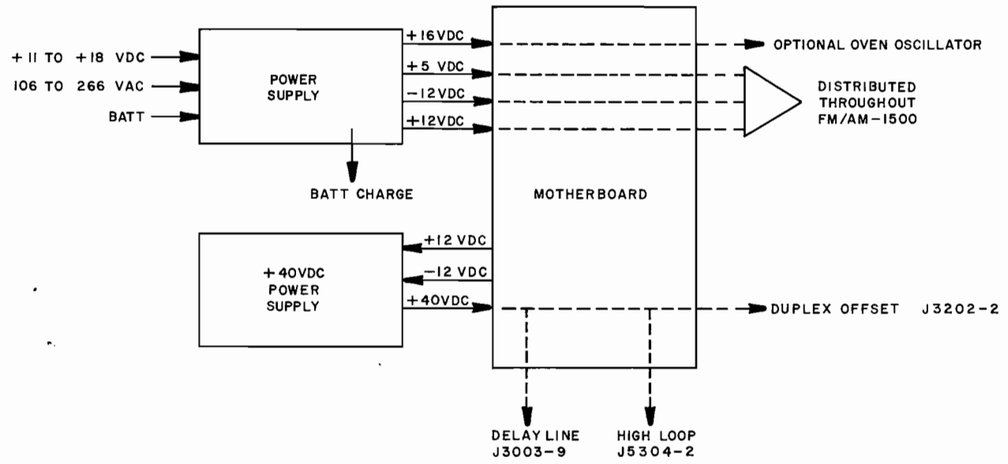


Figure 2-2 Power Distribution Functional Block Diagram

Power Distribution in the FM/AM-1500 is chiefly through the Mother Board. (See Figure 2-2). Power inputs to the Power Supply are converted to +5, +12, -12 and +16 VDC outputs. The +16 VDC output is available to power an optional Oven Oscillator (10 MHz standard, discussed in Frequency Reference Functional Theory). The remaining three outputs are distributed through the Motherboard to the individual modules, switches and controls throughout the FM/AM-1500. The +40 V Power Supply uses the +12 VDC and -12 VDC lines to develop a +40 VDC output which is distributed through the Motherboard to the High Loop Module, where it is used to develop tune voltages and to the Duplex Offset Module where it is used to control the tune voltages. The +40 V is also used by the Delay Line Module for phase-shift purposes.

2-3-1 Power Supply Module Detailed Theory

The Power Supply Module can operate on AC or DC (See Figure 2-3). The AC input can be 106 to 266 VAC and can be 50 to 400 Hz. The DC input can be an external 11 to 18 VDC source or it can be the internal battery source. When the front panel PWR/OFF/BATT Switch is set to PWR or to BATT, +12, +5 and -12 VDC voltages are output to the Motherboard. A +16 VDC output is also sent to the Motherboard where it is available to power an optional Oven Oscillator.

The AC Line voltage is filtered and rectified by T5801 and bridge rectifier BR5801. The output of the rectifier, several hundred volts DC, is filtered by C5803 and C5804. The negative output is floating common which serves the:

- 1st Trapezoid Oscillator
- 1st Comparator
- 1st Driver
- 1st MOS Switch
- Current Sense Resistors
- Fast Current Limiter
- Slow Current Limiter

WARNING

THE DIFFERENCE OF POTENTIAL BETWEEN THE FLOATING GROUND AND CIRCUIT, OR CHASSIS, GROUND CAN EXCEED 300 V PEAK. THIS POTENTIAL CAN CAUSE SERIOUS INJURY OR EVEN DEATH. ALWAYS USE AN ISOLATION TRANSFORMER AND TAKE EXTREME CARE WHEN WORKING INSIDE THE POWER SUPPLY MODULE.

The several hundred volts DC out of the rectifier is applied to one end of the step-down transformer T5701 and to the +15 V floating regulator (Q5703 and Q5714). The +15 V floating regulator provides power for:

- 1st Trapezoid Oscillator
- 1st Comparator
- 1st Driver
- Opto Isolator
- Slow Current Limiter

The 1st Trapezoid Oscillator (U5701) produces a trapezoidal waveform

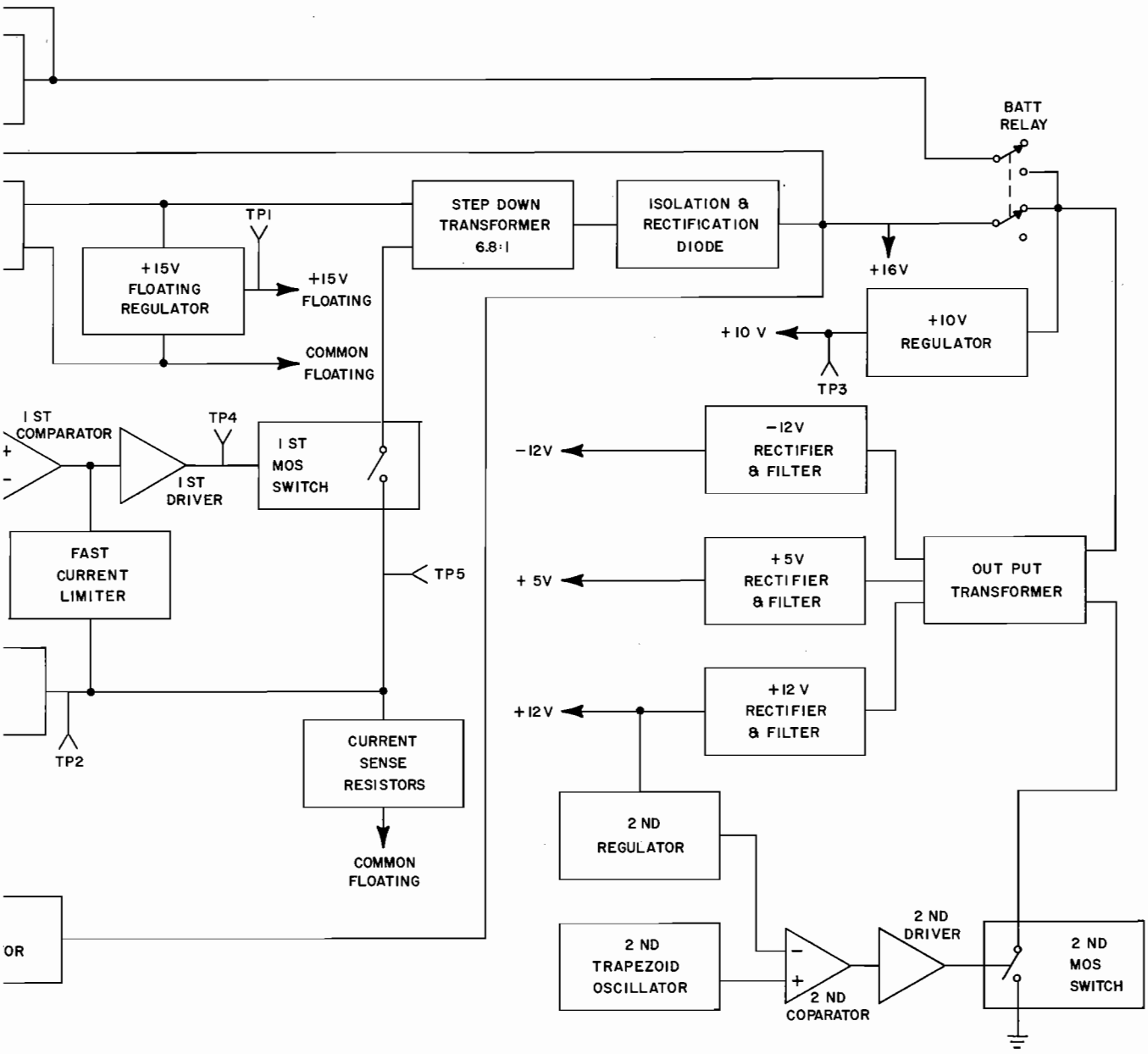


Figure 2-3 Power Supply Detailed Block Diagram

The 1st MOS Switch essentially grounds one side of the step-down transformer during the time that the rectangular wave from the 1st Driver is high. The output of the step-down transformer is rectified by the isolation and rectification diode CR5710. The output of the isolation and rectification diode is applied to the 1st Regulator which adjusts the output of the opto isolator and the duty cycle of the rectangular wave to produce +16 VDC at the output of the Isolation and Rectification Diode.

The current sense resistors, R5728 thru R5731, produce a voltage proportional to the current passing thru the 1st MOS Switch. This voltage is applied to the fast and slow current limiters. The fast current limiter (Q5711) reduces the output of the 1st Driver if the current exceeds approximately 5A. The fast current limiter limits the peak current. The slow current limiter (U5704) integrates the voltage sample from the current sense resistors and applies its output to the negative side of the 1st Comparator, which causes the duty cycle to be reduced if the average current thru the 1st VMOS Switch exceeds a predetermined value.

The output of the Isolation and Rectification Diode is applied to the Battery Charger and to the Line Relay. The Battery Charger (U5703, Q5701, Q5702) provides 14.2 VDC to charge the internal 12 V battery. The Battery Charger also limits charging current to a safe level. Notice that external DC is also applied to the Battery Charger and to the Line Relay. When using external DC, the Isolation and Rectification Diode prevents the external DC from flowing thru the secondary of the step-down transformer. The battery is then charged by external DC (providing that the external DC is above approximately 13 VDC).

When the Line Relay (K5701) is energized, the output of the Isolation and Rectification Diode or external DC (whichever is applicable) is applied to the +10 V Regulator and to one side of the primary of the output transformer T5702.

NOTE

On FM/AM-1500 serial numbers 1142 and subsequent, the Line Relay (K5701) and its associated diode (CR5712) have been deleted. R5701 and CR5728 were added, thus making a solid state means of switching the FM/AM-1500 on and off. CR6001 was also added between pins 9 and 3 of J6003. For

When the Battery Relay (K5702) is energized, the battery voltage is applied to the +10 V regulator and one side of the primary of the output transformer. When the set is off, both the Battery and Line Relays are de-energized.

The +10 V Regulator (Q5706 and CR5714) supplies power for:

- 2nd Trapezoid Oscillator
- 2nd Comparator
- 2nd Driver
- 2nd Regulator

The 2nd Trapezoid Oscillator (U5705) produces a trapezoidal waveform which is applied to the positive side of the 2nd Comparator (U5706). The negative side of the 2nd Comparator is driven by the 2nd Regulator (U5707) which controls the DC level at the negative input and therefore the duty cycle of the output of the 2nd Comparator. The output of the 2nd Comparator is applied to the 2nd Driver (Q5712 and Q5713). The 2nd Driver supplies the necessary current to give the 2nd MOS Switch fast turn-on and turn-off characteristics. The 2nd MOS Switch (Q5708, Q5709, and Q5710) grounds the other side of the primary of T5702 when the output of the 2nd Driver is high. T5702 has three secondaries which are rectified to produce +12, -12, and +5 VDC. The output of the +12 V rectifier is applied to the 2nd Regulator which adjusts the duty cycle of the Comparator to produce +12 V at the output of the +12 V rectifier.

2-3-2 +40 V Power Supply Module Detailed Theory

The +40 V Power Supply converts +12 and -12 VDC inputs to an output voltage of approximately +40 volts (See +40V Power Supply Schematic in Section 7 of this Manual). U5601 is an astable multivibrator of approximately 39 kHz, creating a square wave from the outputs of Q5602 and Q5603. The 24 Vp-p square wave is applied to the voltage doubler of CR5601, CR5602, CR5603 and CR5604. The output of the voltage doubler is approximately +40 VDC.

2-4 FREQUENCY STANDARD FUNCTIONAL THEORY

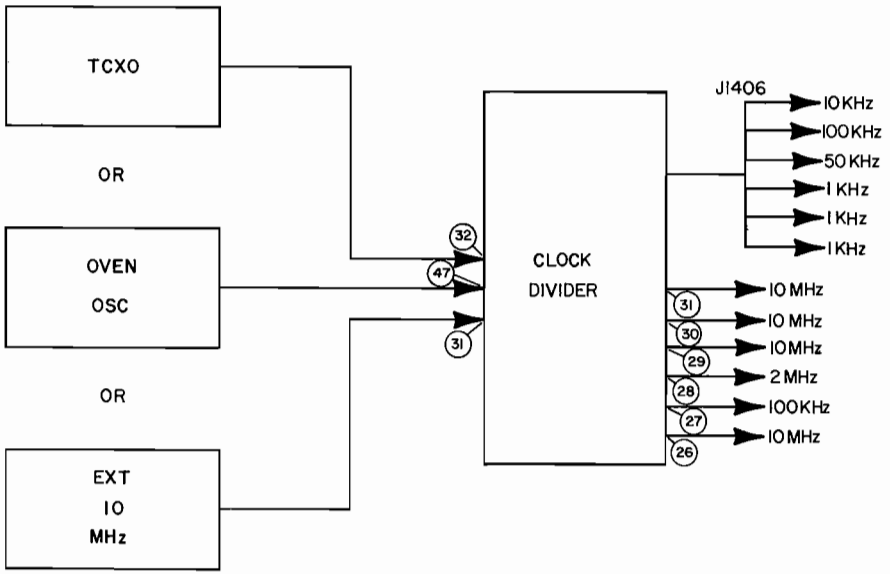


Figure 2-4 Frequency Standard Functional Block Diagram

The 10 MHz reference standard used in the FM/AM-1500 may be one of three sources (See Figure 2-4): an optional TCXO (Temperature Compensated Crystal Oscillator), an optional Oven Oscillator or an external 10 MHz standard (input through 10 MHz REF Connector on the rear panel). Regardless of whether or not an internal 10 MHz standard is installed, the FM/AM-1500 will switch over to the external 10 MHz standard, if connected. The 10 MHz standard is input to the Clock Divider Module where it is converted to the reference frequencies used by other modules of the FM/AM-1500.

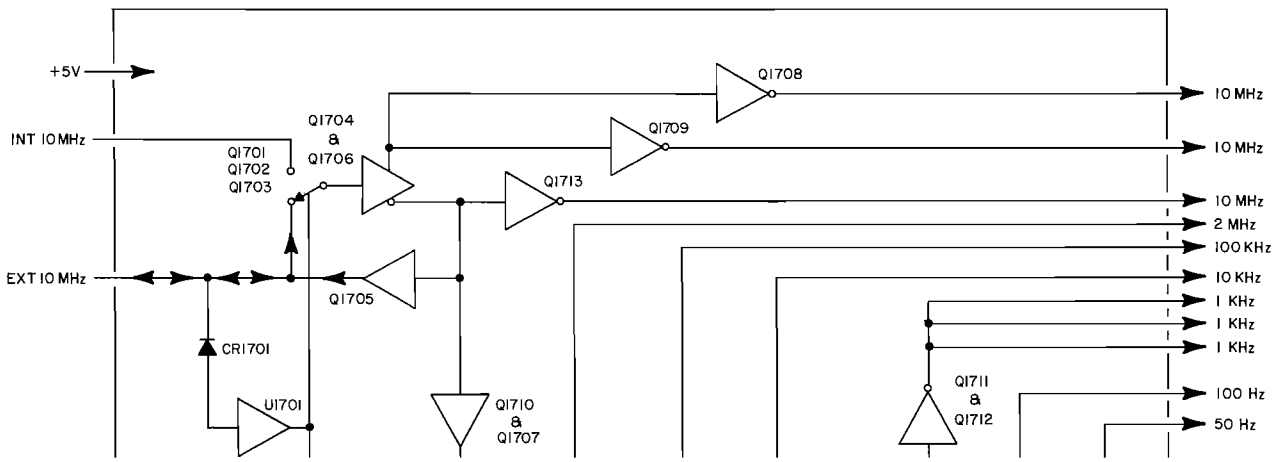
2-4-1 Clock Divider Module Detailed Theory

The 10 MHz internal standard signal is input at J1401 and sent through Q1701 when its base is biased high (See Figure 2-5). Transistors Q1704 and Q1706 buffer the 10 MHz sent to the individual driver transistors. Transistor Q1705 provides a 10 MHz test signal of approximately 0.8 Vp-p which is available at the 10 MHz REF Connector on the rear panel.

When an external 10 MHz TTL signal of approximately 2 Vp-p or greater is input from the 10 MHz REF Connector on the rear panel, it is input at J1402 and detected at CR1701. U1701 will then switch off the internal input at Q1701 and switch the external signal through at Q1702 to the buffer transistors. Transistor Q1714 will also conduct, causing the EXT REF Indicator Lamp on the front panel to illuminate.

The 10 MHz signal is split and buffered by Q1704, then output through Q1708 to J1404 for use by the 89-90 MHz Receiver and through Q1709 to J1402 for use by the High Loop PC Board.

The output of Q1706 goes to Q1705, Q1707 and Q1713. Q1713 buffers the output to J1403 for use by the Low Loop Mixer module. When the external reference is not used, Q1705 buffers the 10MHz to J1402. Q1707 buffers the 10 MHz to Q1710, where it is amplified to a leve needed by U1702A. U1702, U1703 and U1704 each contain two "Divide-by-Two" and two "Divide-by-Five" circuits. Table 2-1 shows the input and output pins for each frequency. U1705 buffers the divider output before sending it to the CPU and the optional GPIB.



IC	INPUT	PIN (FROM) /PIN (TO)	FACTOR	OUTPUT FREQUENCY
U1702	10 MHz	4/1	5	2 MHz
	2 MHz	6/3	2	1 MHz
	1 MHz	15/13	2	500 kHz
	500 kHz	12/10	5	100 kHz
U1703	100 kHz	4/1	5	20 kHz
	20 kHz	6/3	2	10 kHz
	10 kHz	15/13	2	5 kHz
	5 kHz	12/10	5	1 kHz
U1704	1 kHz	4/1	5	200 kHz
	200 Hz	6/3	2	100 kHz
	100 Hz	15/13	2	50 Hz

Table 2-1 Clock Divider Frequencies (U1702, U1703, U1704)

2-5 FREQUENCY SYNTHESIS FUNCTIONAL THEORY

The Frequency Synthesis Functional Block is divided into two major sections: High Loop and Low Loop (See Figure 2-6).

High Loop Section

The function of the High Loop Section is to phase-lock the two VCO's in the Dual VCO Module with a 10 MHz reference frequency that is input into the High Loop Module. The High Loop Section consists of the following modules:

- High Loop
- Dual VCO
- Low Pass Filter
- High/Low Pass Filter
- Delay Line
- Buffer Amplifiers A & B

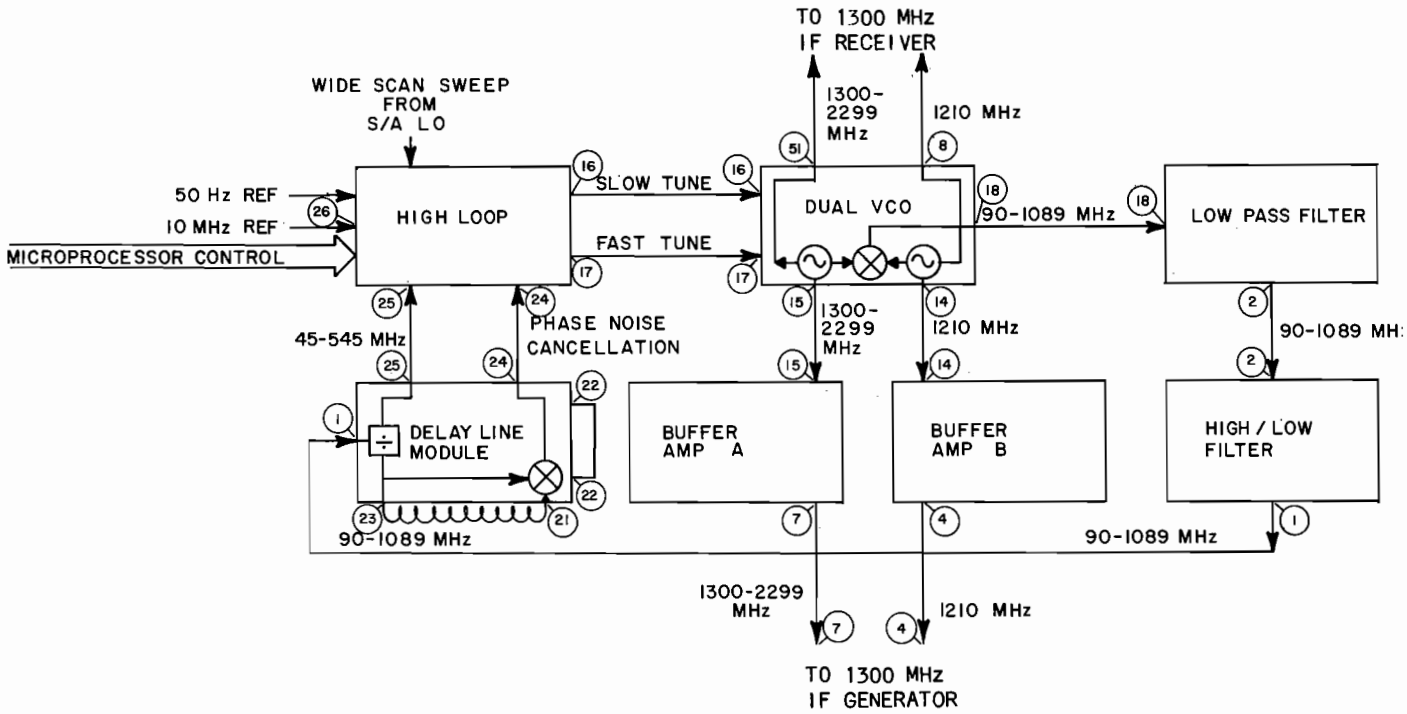
Failure of any of these modules will result in the failure of High Loop Section.

Low Loop Section

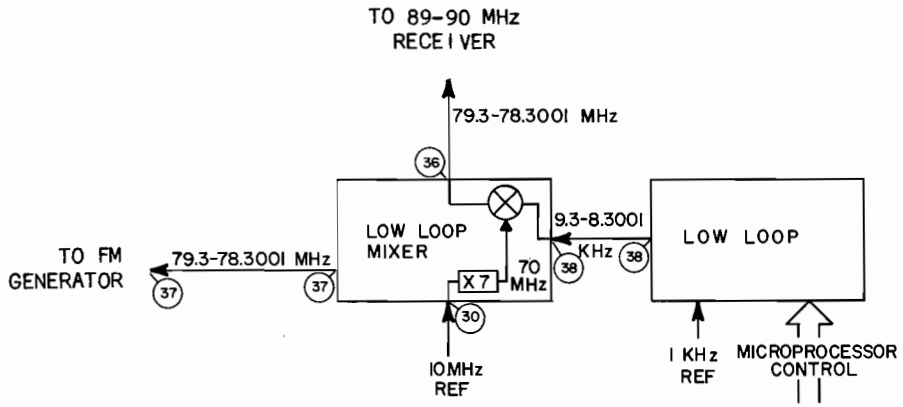
The function of the Low Loop Section is to phase-lock the frequency generated by the four lower digits of the RF frequency setting on the front panel with the VCO in the Low Loop Module. The resulting phase-locked frequency will then be fed to the Generator Functional Block, the Spectrum Analyzer Functional Block and to the Receiver Functional Block. The Low Loop Section consists of the following modules:

- Low Loop
- Low Loop Mixer

Failure of any of these modules will result in the failure of the Low Loop Section.



HIGH LOOP SECTION



2-5-1 High Loop Module Detailed Theory

General

The High Loop Module provides phase-locked frequency control of the Dual VCO Module as the operating frequency is selected between 000 and 999 MHz (the three upper digits of the selected frequency). Operation of the High Loop Module can be divided into two major sections: the normal phase-lock loop, and the wide scan mode. These modes are controlled by the setting of the front panel ANALY DISPR Control. Settings from 1 K thru 1 M are "normal". Settings from 2 M thru FULL are "wide scan". In normal settings, the system goes into a fixed mode of operation, placing the 1300-2300 MHz VCO (in the Dual VCO Module) on the commanded frequency. In wide scan settings, the 1300-2300 MHz VCO is swept and slaved to the analyzer sweep, and is centered about the commanded frequency. (See Figure 2-7 and the High Loop Schematic in Section 7 of this manual.)

NORMAL (FIXED) MODE

Programmable Divider Circuit

The 45 to 545 MHz frequency from the Delay Line Module enters at J2801 on the digital board to drive the programmable divider circuit and a fixed divider chain. IC's U2201, U2202, U2203, U2204 and associated components form the programmable divider. The programmable divider operates from 45 - 544 counts, depending on the frequency selected on the keypad. IC's U2201 and U2202 operate as a ÷10/÷11 swallow counter. U2201 will divide by 11 until U2202 reaches zero count. At zero count, pin 14 of U2213A goes high, stopping U2202 from counting, and pulling pin 2 of U2201 high. U2201 will now divide by 10 until the next load condition.

The output of U2201, pin 8, synchronously clocks down the divider chain. When U2203 and U2204 have counted down through counts 00 to 99, flip-flop U2205A will be set, enabling the end-of-counts gate at pin 13 of U2213C. Forty-five more counts are needed to clear the counter. When counter U2203 has counted down to two counts before zero, pin 10 of U2205B is enabled. The next clock pulse at pin 11 of U2205B will set the flip-flop, causing a new number to be loaded into the programmable dividers. Flip-flop U2205A is reset at pin 1, and then pin 10 of U2205B is returned to a low condition. The next clock pulse at pin 11 of U2205B will clear the flip-flop and end the load condition to begin a new count cycle. The output frequency of the programmable divider should be 500 kHz. The 500 kHz signal is sent to an ECL to TTL level translator composed of Q2219 and Q2220. The TTL output at the collector of Q2220 is buffered by U2214A. The output of U2214A is sent to the Frequency Comparator and Phase Correction Circuits, and also sent to a ÷10,000 circuit to develop a 50 Hz reference signal used in the wide scan mode (to be discussed later).

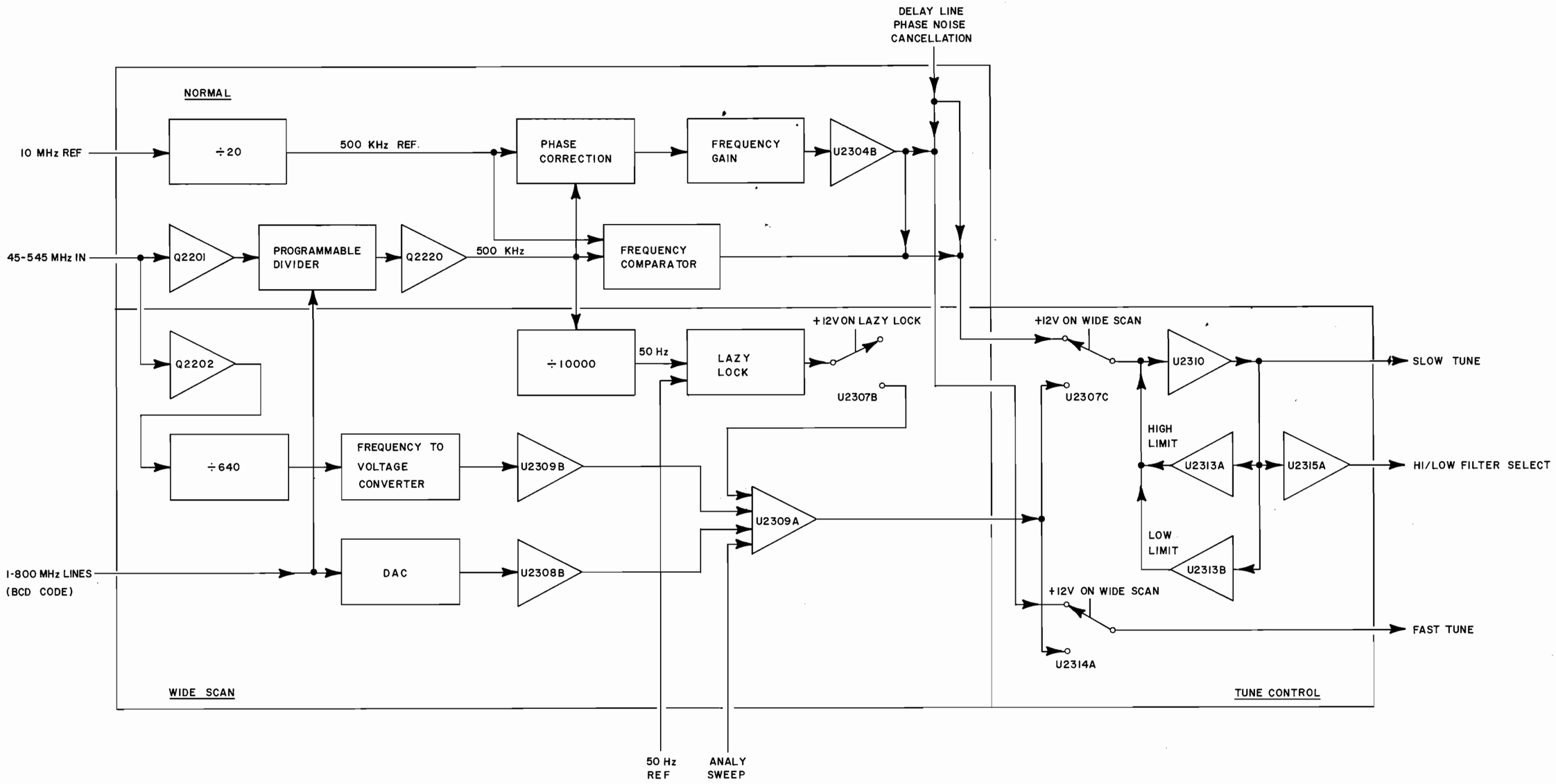


Figure 2-7 High Loop Detailed Block Diagram

Frequency Comparator Circuit

A 10 MHz reference input at J2802 is divided by two in U2209A and then by 10 in U2210 to yield a 500 kHz reference frequency. When wide scan (2M, 5M, 10M and full positions of the front panel ANALY DISPR Control) is selected, Q2203 is turned on to disable U2209A by pulling pin 6 low. This removes the reference frequency from the circuit for tracking analyzer operation.

The frequency comparator system is composed of U2211A, U2211B, U2214C, CR2209, CR2210, C2230 and U2215B. The reference 500 kHz is presented to U2211B (pin 5) and the divider chain output is presented to U2211A (pin 1). If the frequency at U2211A is less than 500 kHz, U2211B (pin 8) will be discharging the voltage at C2230 (through CR2210). A low voltage at U2215B (pin 5) will force the output (pin 7) low. Similarly, if the frequency at U2211A is greater than 500 kHz, U2211A (pin 12) will be charging C2230 through CR2209, and U2215B (pin 7) will be forced high.

If both frequencies at U2211A and U2211B are 500 kHz (normal phase lock condition), U2211A (pin 12) and U2211B (pin 9) will both be high, enabling gate U2214C which resets U2211A and U2211B. During this condition, U2211A (pin 12) and U2211B (pin 8) will be equal and opposite, maintaining a static condition at C2230 and approximately zero volts at the output of U2215B (pin 7).

When the set periods of U2211 are not equal, C2229 will charge up and pull up on the base of Q2218 to indicate an out of phase-lock condition. However, if wide scan is selected, Q2221 will turn on and Q2218 will turn off to disable CR2225 and to supply a +12 V signal to the LOCK Logic on the Demod Audio PC Board.

The control voltage developed by the frequency comparator goes to the Analog board through E1 (pin 4) to a diode network (CR2302, CR2303, CR2304 and CR2305). This network is activated when the control voltage moves 2 diode gaps either positive or negative from its normal zero reference. This circuit exists so that the frequency comparator cannot prematurely take control of the High Loop. This allows an extremely limited amount of frequency tuning to be done through the 1210 MHz oscillator (fast tune line). Output from this network is summed through R2344 at U2307C (pin 12) with the frequency gain information, and with a phase noise cancellation from the Delay Line (through R2345).

Phase Correction Circuit

The first sample and hold circuit is composed of Q2208, Q2209, Q2210 and Q2213. C2225 is the hold capacitor. The reference 500 kHz is buffered by Q2208 and presented to Q2209 and Q2210. The 500 kHz programmable divider output is presented to Q2213 which develops a sample pulse. The sample pulse controls the conduction of Q2209 and Q2210. Sampling at the peak (or high condition) results in Q2209 being turned off and Q2210 being turned on, increasing the voltage on C2225. Sampling at the low point of the 500 kHz results in Q2210 being turned

off and Q2209 on. The collector voltage at Q2209 pulls down, decreasing the voltage at C2225. The increasing or decreasing voltage at C2225 slews the Dual VCO frequency such that the sampling pulse occurs at the 500 kHz transition point, achieving the phase lock condition.

The voltage at C2225 is buffered by Q2212 and Q2307 (on the analog board) and presented to the second sampler Q2203. The second sample pulse is developed through Q2214 and Q2301 (on the analog board). These two transistors provide a fixed delay to separate the second sample pulse away from the first sample pulse. When the gate of Q2303 goes high, voltage at the source is coupled to the drain and held by C2321 (the second hold capacitor). Q2302 provides a signal 180° out of phase with the signal at Q2301 and is coupled through C2305 to C2321 to null 500 kHz transition noise. The voltage at C2321 goes to U2304A where gain is adjusted such that zero volts occur at the output of U2304A (pin 1).

Frequency Gain Circuit

The output of U2304A is presented to the frequency gain circuit which is composed of switches U2305A, U2305B, U2305C, U2306A, U2306B and U2306C. The switches are controlled by the 6 frequency select lines (from 40 MHz through 800 MHz). The gain of op-amp U2304B is controlled by the resistance ratios of the frequency gain control, along with R2341 and R2340.

The output of U2304B (pin 7) is summed, through R2345, with the frequency comparator and the phase noise cancellation from the Delay Line at U2307C (pin 12). The output of U2304B (pin 7) is also presented to U2314A (pin 2) where it is summed with phase noise cancellation from the Delay Line. Operation of U2314A is similar to U2307C in that it is switched according to the wide scan control line. The output of U2314A goes to the fast tune line (J2805).

WIDE SCAN MODE

In the wide scan condition, the VCO is swept such that the average center frequency is maintained by the High Loop Module and the sweep width is controlled by the dispersion setting of the Spectrum Analyzer.

The slow tune voltage and a limited amount of fast tune voltage on wide scan can be the sum of 4 signals. One source is the frequency to voltage converter. Another source is the frequency find signal from the DAC's. A third source is the tracking analyzer sweep ramp voltage. A fourth is the lazy lock signal except it is not active in the full scan condition.

÷640 Circuit

Q2202 and Q2203 are switched on by the +12 V in wide scan. Q2203 pulls the reset line of U2209A low, removing the 500 kHz reference signal. This disables the frequency comparator and phase correction circuits of the normal (fixed) phase lock system.

The 45-545 MHz input from the Delay Line Module is buffered by Q2202 and sent to a fixed divider circuit composed of U2206, U2207 and U2208. Q2204 and Q2205 translate the output of U2207 from ECL to TTL. The output of Q2205 clocks U2208.

Frequency to Voltage Converter Circuit

The frequency to voltage converter relative to the commanded DAC voltage is analogous to the frequency detector of the normal (fixed) mode of operation. It is responsible for steering the frequency of the 1300-2300 MHz VCO over a wide range.

The output of U2208 is conditioned by Q2206 and Q2207 into a sharply defined square wave. The upward transition of the square wave turns on Q2216, and a current proportional to the frequency is supplied to C2220 and R2240. Q2215 limits the lower control voltage on the emitter of Q2216 to approximately 6.2 V. The upward limits on the emitter of Q2216 are controlled by its base being held to about 6 V. The output voltage of this circuit is approximately 0-5 V (when the ANALY DISPR Control is in FULL). The output voltage is fed to U2309 for amplitude adjustment and then fed through R2356 to be summed with other correction voltages at U2309B (pin 6) for wide scan operation.

DAC Circuit

The 1-800 MHz (BCD coded) lines are converted in DAC's U2301, U2302 and U2303 to a control voltage for the tune lines. The output currents of the DAC's are summed at U2308B (pin 6). R2330 is provided for gain adjustment (according to the center frequency). The resulting voltage out of U2308B (pin 7) is fed through R2231 to U2309B (pin 6) for summing with the other correction voltages. The voltage is normally positive in approximately the same magnitude as the average negative contribution from U2309A.

Tracking Analyzer Sweep Ramp Voltage

The S/A sweep ramp voltage is input at pin 24 of J2803, from the Spectrum Analyzer L.O. Module. The voltage is routed through R2375 for summation at U2309B (pin 6).

Lazy Lock Phase Detector Circuit

The lazy lock information is analogous to the phase detector information in the normal (fixed) mode. It is responsible for maintaining the center frequency in a phase-locked condition.

The "Lazy lock" contribution begins with the 500 kHz output of the divider chain of the normal (fixed) mode. This output is buffered by U2214A and divided by two at U2209B. The TTL output of U2209B is converted to CMOS level by Q2217 and divided by 5000 by U2212. When the count reaches 50 Hz at pin 2, U2216 is enabled, resetting U2212. This 50 Hz signal is presented to U2311 on the analog board, where it is compared with the 50 Hz reference signal coming from the Clock Divider

module. The error signal at U2311 (pin 13) is filtered through R2364, C2325 and R2365 to an average DC level. A gain adjust circuit, controlled by U2307A and Q2304, which parallel R2378, R2379 and C2322 with the filter, is enabled when the 400 MHz or 800 MHz line is selected. The average correction voltage is integrated by U2308A and fed to U2307B (pin 4) through R2377. U2307B is controlled from the +12 V lazy lock line developed in the Spectrum Analyzer L.O. assembly. This line will go low only in the FULL setting of the ANALY DISPR Control. The voltage correction from the lazy lock is fed through U2307B and summed directly at U2309B (pin 6).

The resultant output voltage of the summed inputs to U2309B is fed to the fast tune and slow tune switches (U2314A and U2307C respectively). The diode network of CR2311 and CR2309 allow a faster resetting of the slow tune voltage to the sweep start condition. In wide scan, pins 13 and 14 of U2307C are connected to integrator U2310 and Q2306 and to the slow tune line. Also, pins 1 and 15 of U2314A are connected allowing wide scan information to the fast tune line.

Output Selection

U2307C is a FET switch whose control line is pin 11. In the normal (fixed) mode, pin 11 is low connecting pins 12 and 14. When wide scan is selected, pin 11 is high connecting pins 13 and 14. The control voltage at pin 14 of U2307C is presented to a system composed of an Integrator (U2310, Q2306 and C2323) a high and low limiter (U2313A and U2313B) and a switch control for the Hi/Lo Pass Filter (U2315A).

When a high condition is sensed at U2310A (pin 2), the output of U2310A (pin 1) pulls down, increasing conduction through Q2306 and lowering the collector voltage which is fed through R2354 to the slow tune line (J2806).

When the low condition is sensed at U2310A (pin 2), the output goes high, reducing conduction through Q2306, and allowing the collector voltage to increase.

The limiting circuit is used to prevent the 1300-2300 MHz VCO from being driven either too high (above 2330 MHz) or too low (below 1275 MHz). When the integrator commands the VCO to go to a frequency above 2330 MHz (U2310A, pin 2, senses low voltage), U2313A (pin 1) goes positive. This positive voltage sums at U2310A (pin 2) through CR2207 and R2350 to prevent the integrator from further increasing the slow tune voltage. This voltage is set according to the individual VCO requirements by R2372. Similarly, a too high condition at U2310A (pin 2) will force U2313B (pin 7) down, limiting further decreasing of the slow tune voltage. This limit is set by R2373.

Switching of the Hi/Lo Pass Filter Module occurs at the specific frequency required by the Hi/Lo Pass Filter and is set by R2387 to switch at + or -10 V.

2-5-2 Dual VCO Module Detailed Theory

NOTE

The Dual VCO Module is designated by IFR Systems, Inc. as being non-repairable in the field. It should be returned to the factory for repair.

The Dual VCO Module supplies the first and second L.O. signals to the 1300 MHz IF Receiver and the 1300 MHz IF Generator Modules, as controlled by the High Loop Module. (See Figure 2-8 and the Dual VCO Schematic in Section 7 of this Manual).

First VCO

The first VCO frequency of 1300 to 2299 MHz is controlled by the slow tune line input at J2406 from the High Loop Module. The tune voltage can vary from 0 to +40 V, depending on the frequency selected. The +12 V power applied at FL2401 is subregulated to approximately +11 V at Q2101 for the oscillator transistor, Q2102. Q2103 and Q2104 amplify the oscillator signal for a +7 to +12 dBm output at J2404 to the 1300 MHz IF Receiver. Q2105 and Q2106 amplify the oscillator signal for a +7 to +12 dBm output at J2405 to the Output Buffer A module. Q2107 and Q2108 amplify the oscillator signal for a +7 to +12 dBm signal to MXR2401.

Second VCO

The second VCO frequency of 1210 MHz is controlled by the fast tune line input at J2403 from the High Loop Module. The +12 V power applied at FL2402 is subregulated to approximately +11 V at Q2001 for the oscillator transistor, Q2002. Q2003 and Q2004 amplify the oscillator signal for a +7 to +12 dBm signal output at J2401 to the Output Buffer B Module. Q2005 and Q2006 amplify the oscillator signal for a +7 to +12 dBm signal output at J2402 to the 1300 MHz IF Receiver Module. Q2007 and Q2008 amplify the oscillator signal for a +7 to +12 dBm signal to a 1400 MHz low-pass filter, FL2403. The second harmonic of 1210 MHz is eliminated by FL2403.

The two VCO signals are mixed in MXR2401 to produce a difference frequency of 90 to 1089 MHz, which is output at J2407 to the Low Pass Filter Module.

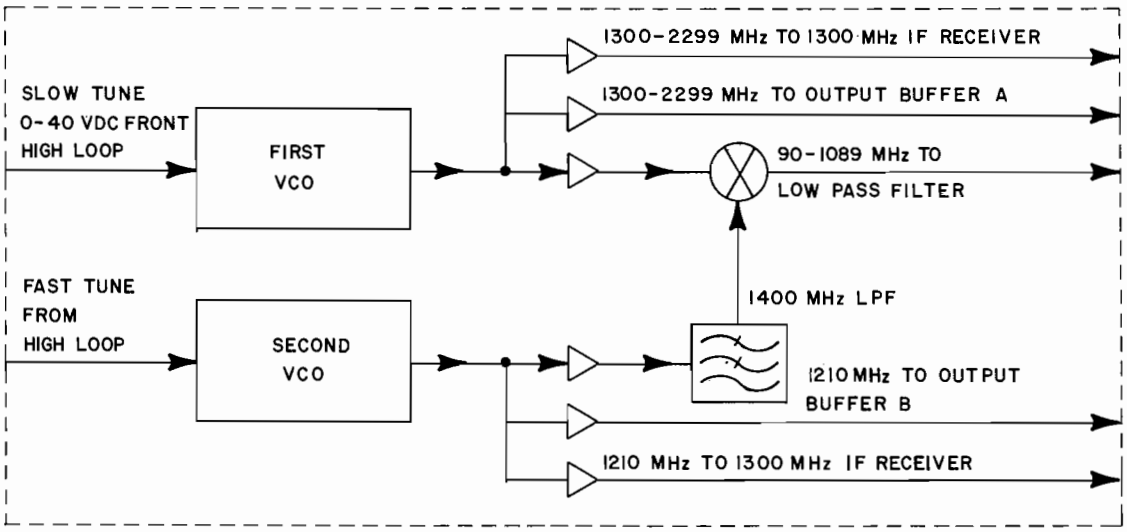


Figure 2-8 Dual VCO Detailed Block Diagram

2-5-3 Low Pass Filter Module Detailed Theory

The Low Pass Filter Module is a tubular, in line low-pass filter connected between the Dual VCO Module and the High/Low Pass Filter Module. The Low Pass Filter must pass 90-1089 MHz, and attenuate the 1210 MHz signal by approximately 40 dB (See the Low Pass Filter Mechanical Assembly Detail in Section 6 of this Manual.)

2-5-4 High/Low Pass Filter Module Detailed Theory

The High/Low Pass Filter Module is controlled from the High Loop Module to act as either a high-pass or low-pass filter. The 90-1089 MHz signal from the Low Pass Filter Module is input at J601. If the control line at FL601 is approximately +10 V, the module acts as a high-pass filter from appoximately 450 MHz to 1089 MHz. If the control line at FL601 is approximately -10 V, the module acts as a low pass filter from 90 to 520 MHz. The crossover frequency varies from module to module, but is marked on the outside of each module as calibrated at the factory. (See the High/Low Pass Filter Schematic in Section 7 of the Manual.)

NOTE

The actual crossover frequency to be used in calibration is 90 MHz less than the frequency marked on the module. This is because the actual operating frequency is 90 MHz above the frequency selected on the Keyboard.

2-5-5 Delay Line Module Detailed Theory

The Delay Line Module creates a residual component cancellation signal to clean the High Loop Section Composite Spectrum. It also divides the 90-1089 MHz signal from the Dual VCO by two for input to the High Loop Module. (See Figure 2-9 and the Delay Line Schematic in Section 7 of this Manual.)

RF Source

The 90-1089 MHz RF input at J3005 is amplified by U2601, U2602 and U2603 to drive U2604 as a divide-by two. One 45-545 MHz signal, out of pin 10 of U2604 is output at J3006 to the High Loop Module.

The RF source for the phase control circuitry is switched from two sources. A +5 V control line (if 455 MHz or greater is selected on the Keyboard) at pin 5 of J3003 enables the output of pin 11 of U2604 (90-545 MHz) to be the source. If the +5 V control line goes to 0 V (when 454 MHz or less is selected on the Keyboard), the source is pin 4 of U2603.

The selected RF source (90-544 MHz if 0-454 MHz is selected on the keyboard, or 228-499 MHz if 455-999 MHz is selected on the keyboard) then splits in two directions. The RF in one direction is amplified by Q2602 and Q2601 and output from J3007 on Board #2 through the Delay Line Coax Cable (75' of coax) to J3001 on Board #1. The RF in the other direction is amplified by Q2603 and Q2604, and then low-pass filtered in selectable filters, as controlled by U2501. The output at J3008 is then sent through a jumper coax to J3002 on Board #1.

Phase Shift Circuit

The jumpered input at J3002 is amplified by Q2509 and sent to one port of MXR2501. The input signal at J3001, through the Delay Line Coax Cable, is amplified in a series of amplifiers which includes two stages of phase shifting (Q2403 and Q2405). As the voltage on varactor diodes CR2403 and CR2404 is varied (SW2501 switches between integrator control or manual control, for test purposes) from 0-30 V, the impedance of the varactors becomes significantly smaller or significantly larger than R2515 and R2523, respectively. This produces a theoretical phase shift of 180° per stage of phase shifting (although realistic limitations won't permit this). The output of the amplifiers is subsequently low-pass filtered in selectable filters, as controlled by U2501. The output of the filters is amplified by Q2508 and sent to an input port of MXR2501. The phase difference between the two inputs to MXR2501 is 90° or 270°, depending on which way K2502 is set by the integrator circuit.

Differential Amplifier Circuit

The differential amplifier consists of Q2519, Q2520, Q2521 and Q2522. The gain of the differential amplifier is increased through relay K2501, if 455 MHz or greater is selected. The integrator circuit will

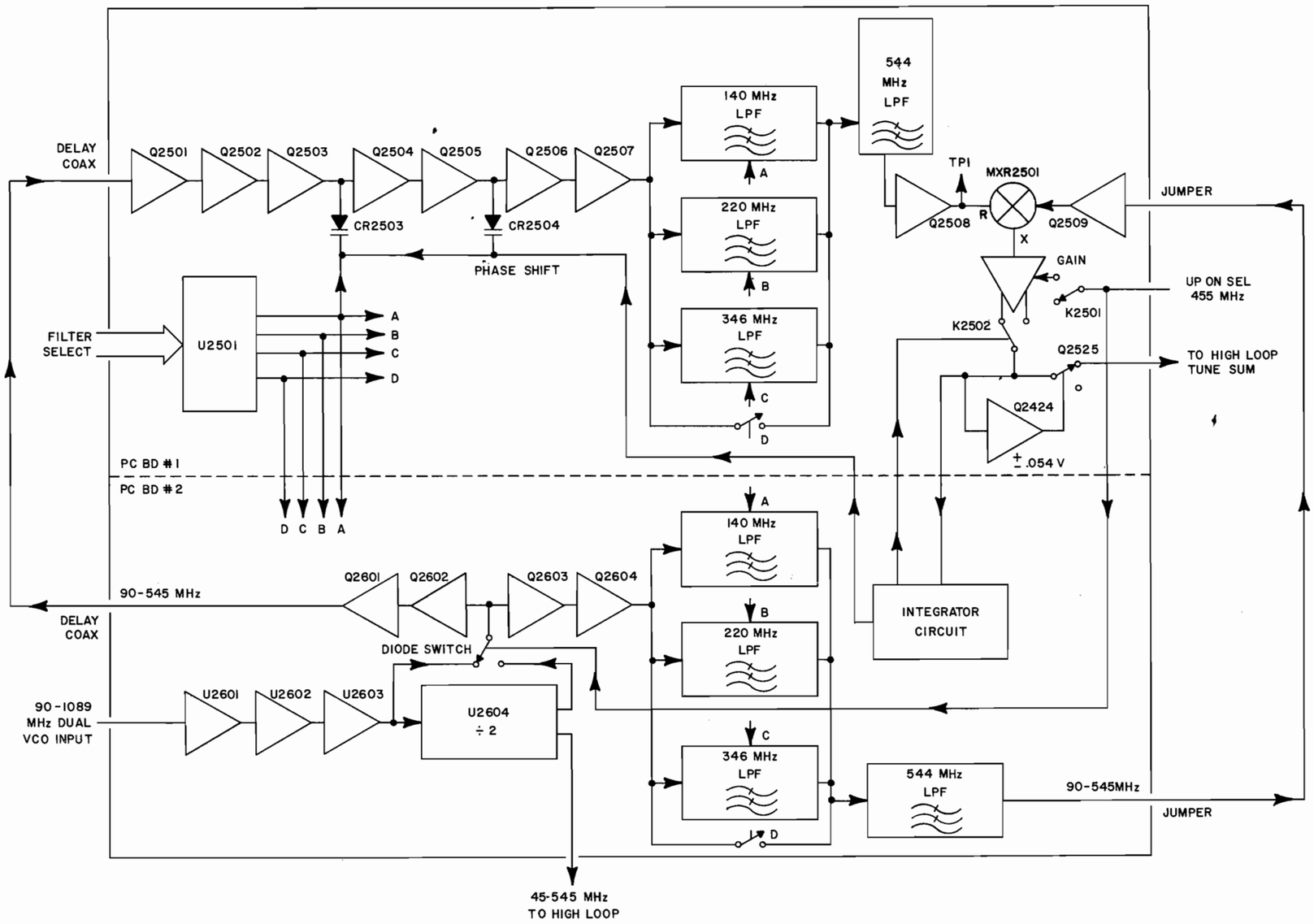


Figure 2-9 Delay Line Detailed Block Diagram

determine which of the signals from the differential amplifier is selected, by energizing or de-energizing relay K2502. The selected signal will be output through Q2525, which acts as a switch to prevent unwanted noise, and through J3004 to the High Loop Module. Op-Amps U2503A and U2503B, along with Q2524, shut off Q2525 if the noise level is too high.

If the 90-1089 MHz input signal at J3005 is perfectly still (i.e., no residual FM), the detected phase output will be a steady 0 VDC. If the phase of the input moves (due to residual FM caused by the thermal noise of the Dual VCO and other low-level system components), the disturbance will take longer to travel down the 75 feet of Delay Line Coax Cable (J3007 to J3001) than it will to travel over the jumper from J3008 to J3002. This will cause the detected phase voltage out of MXR2501 to move from either the 90° or the 270° operating point, as determined by the integrator circuit. The operating point selected will be 180° out of phase from any signal disturbances input at J3005. The selected operating point will then be sent to the High Loop Module to cancel any system residual disturbances.

Integrator Circuit

The integrator circuit receives the selected signal from K2502 at the junction of R2637 and R2642. U2607A is an inverting amp which drives the integrator amp, U2607B. The output of U2607B drives the collector of Q2610 from 0 to +30 V for the DC control voltage to the varactor diodes in the phase shift circuit. The collector voltage of Q2610 also is applied to op-amps U2609 and U2610. U2609 sets flip-flop U2606B high on pin 15 when the tune voltage goes above 30 V. This turns off flip-flop U2606A by putting a high at pin 4, the reset line of U2606A. Pin 15 of U2606B also pulls up on the integrator amp, U2607B, to force the integrator to slew downward.

Op-Amp U2610 sets flip-flop U2606A high on pin 1 when the tune voltage goes below 0 V. The high on pin 1 of U2606A resets flip-flop U2606A, and pulls down on the integrator amp, U2607B, to force the integrator to slew upward. This is done through Q2608, Q2609 and CR2618.

The Q outputs of both flip-flops, U2606A and U2606B, set and reset flip-flop U2605B. The Q line of U2605B is the control line for relay K2502. Also, when the Q lines of flip-flops U2606A and U2606B are high, their respective indicator LED's, CR2616 and CR2615, will be illuminated.

Op-Amp U2608A is the control for flip-flop U2606. If the input to U2608A, pin 2, crosses approximately 10 VDC in the proper phase direction, and either half of U2606 is still slewing the integrator voltage, pin 6 of U2608A goes high to clear the active half of U2606. Q2605 is an inverter for the signal to clear U2606B. Notice that pin 6 of U2608A must make a positive transition to clear U2606A, and a negative transition to clear U2606B. These transitions are necessary since the clear inputs of U2606 are positive edge triggered. They also prevent the integrator from locking the phase output into an "in phase" condition, which would add noise to the system instead of cancelling noise.

2-5-6 Buffer Amp Module Detailed Theory

The FM/AM-1500 contains two identical Buffer Amps. Buffer Amp A is in the 1300-2300 MHz output line of the Dual VCO, while Buffer Amp B is in the 1210 MHz output line. Both Buffer Amps serve to isolate the 1300 MHz IF Generator from the Dual VCO. Any amplification done by the Buffer Amps is of secondary importance. Typical input and output level for both Buffer Amps is +5 to +12 dBm. (See the Buffer Amp Schematic in Section 7 of this Manual.)

2-5-7 Low Loop Module Detailed Theory

The Low Loop Module is a phase-locked frequency synthesizer operating from 83.0001 to 93 MHz, depending on the setting of the lower four digits of the front panel RF frequency. (See Figure 2-10 and the Low Loop Schematic in Section 7 of this Manual).

Programmable Divider Circuit

U3101, U3102 and U3105A operate as a swallow counter for the 100 Hz line. When U3102 reaches its programmed count, pin 12 will go high and pull pin 14 of U3105A high. This causes an extra 100 Hz count of U3102, since one clock pulse is required for U3105A after U3102 has reached count zero.

U3108, U3109, U3110 and U3111 form a decade-upward counter in the programmable divider chain. The system senses count 9297 and loads a new number at count 9298 when pin 8 of flip-flop U3105B goes low. Pin 9 of U3105B goes low on count 9299, and the extra 100 Hz count in the swallow counter is required for the programmable divider before a new number count begins.

Phase Comparator Circuit

Flip-flop U3106 forms a charge pump phase comparator. When the set period of each section is equal, the charge on C3127 remains constant. If pin 12 is set longer than reset, the charge on C3127 will decrease, causing integrator U3113A to slew up to change the frequency of the voltage controlled oscillator. When the set periods of U3106 are not equal, C3128 will charge and pull up on the base of Q3108. The collector of Q3108 will pull low to indicate an out of phase-lock condition.

Oscillator Circuit

Q3101 and associated components form a voltage controlled oscillator, which ranges from 83.0001 to 93 MHz. L3102 is adjustable to set a tune voltage of +7 V at 93 MHz. Q3101 is operating properly when there is a voltage of -2 to -4 V on its gate (pin 3). Q3102 is a buffer for the oscillator output signal. Q3101 and Q3102 operate on +6.9 V, subregulated by zener diode CR3108.

Divide-By-10 Circuit

The amplifier stage of Q3103 and Q3104 increases the VCO signal to drive the input to the programmable divider. The amplifier stage of Q3105 and Q3106 increases the VCO signal to drive U3107 as a divide-by 10 circuit. The divided 8.3001 to 9.3 MHz signal is sent through a 15 MHz low-pass filter and output at J4001, at about -12 dBm, to the Low Loop Mixer Module.

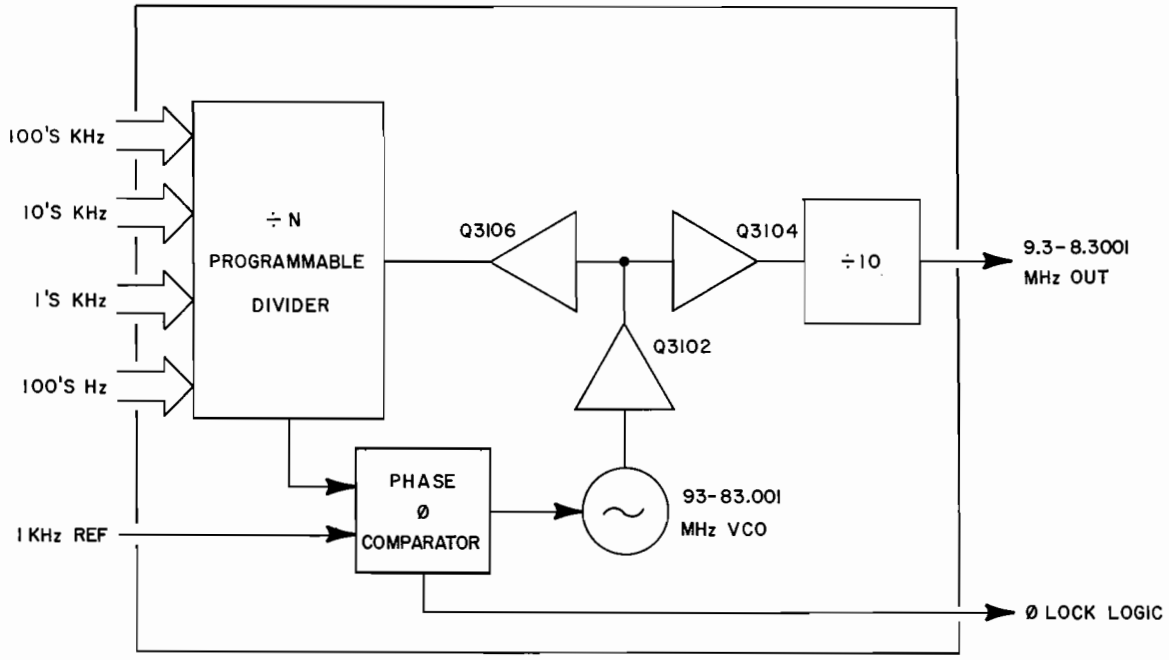


Figure 2-10 Low Loop Detailed Block Diagram

2-5-8 Low Loop Mixer Module Detailed Theory

The Low Loop Mixer Module multiplies a 10 MHz reference signal to 70 MHz and mixes it with the 8.3001 to 9.3 MHz signal from the Low Loop Module, resulting in an output signal of 78.3001 to 79.3 MHz. (See Figure 2-11 and the Low Loop Mixer Schematic in Section 7 of this Manual).

The 10 MHz reference signal, input at J1801, is amplified by Q1901 and Q1902. L1902 is used to adjust the frequency to exactly 70 MHz. The signal is band-pass filtered by L1904, L1905, L1906, L1907 and L1908, and then sent to MXR1901.

The mixer output frequency is band-pass filtered, centered on 78.8 MHz, by L1912, L1913, L1914, L1915 and L1916. The filters are tuned to pass a 1 MHz wide signal. The resulting 78.3001 to 79.3 MHz signal splits at Q1905 and is amplified by Q1906 and Q1907 for outputs to the FM Generator and Spectrum Analyzer L.O. Modules, respectively.

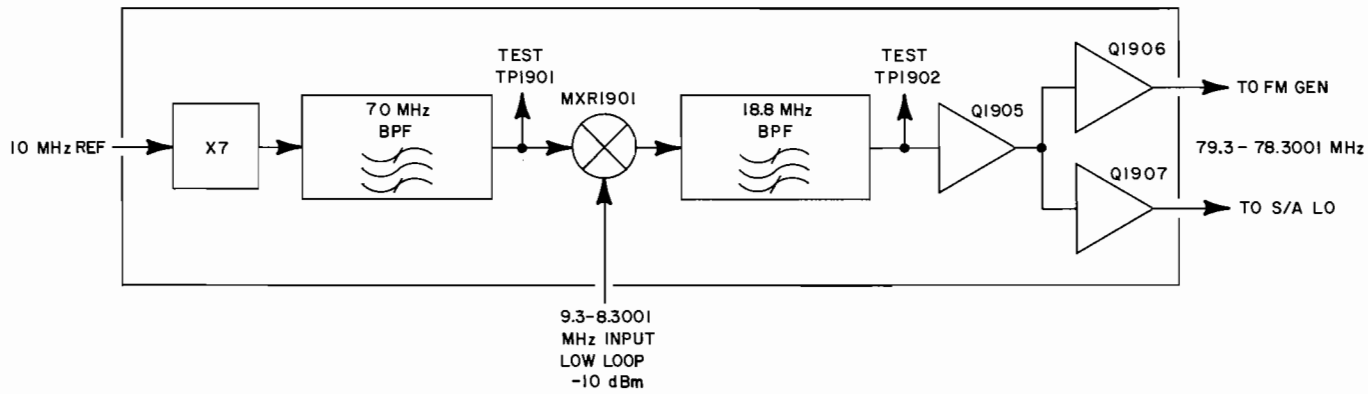


Figure 2-11 Low Loop Mixer Detailed Block Diagram

2-6 RECEIVER FUNCTIONAL THEORY (Refer to Figure 2-12)

The input to the receiver section of the FM/AM-1500 can be received at the front panel ANTENNA Connector through an antenna or received at the front panel TRANS/-40 dB DUPLEX Connector via direct cable connection (See Figure 2-12). If the signal is received at the ANTENNA Connector, it goes directly to the 1300 MHz IF Receiver Module. If the signal is received at the TRANS/-40 dB DUPLEX Connector, it is switched through the Power Termination Module (discussed under Generate Function). If the FM/AM-1500 is operating in the Generate Simplex mode, a crossfeed signal is fed through the Diode Switch to the 1300 MHz IF Receiver Module.

Whatever the source of the signal entering the 1300 MHz IF Receiver, it is up-converted twice as a result of mixing with the Dual VCO L.O. frequencies, and output as on 89.0001-90 MHz signal to the 89-90 MHz Receiver Module and to the Spectrum Analyzer Functional Block. The 89.0001-90 MHz IF signal is down-converted twice in the 89-90 MHz Receiver Module and output as a 700 kHz signal. The Low Loop section of the Frequency Synthesis Functional Block mixes with the received signal to produce the 700 kHz output. The 700 kHz signal is sent to the Oscilloscope AM display and to the DEMOD AUDIO PC Board, which drives the speaker, Oscilloscope FM and the front panel meter displays. The DEMOD AUDIO PC Board also performs AGC action on the 89-90 MHz Receiver.

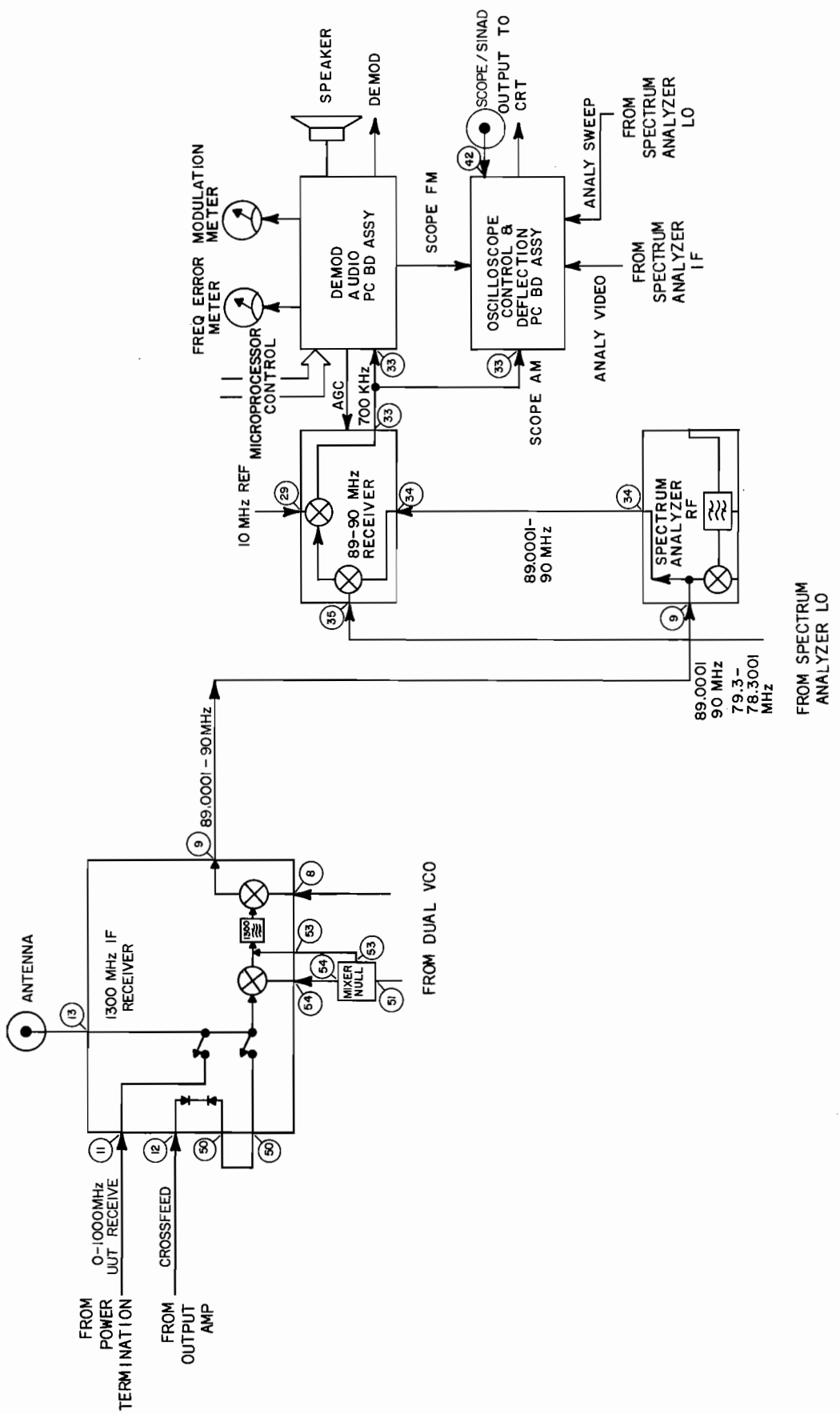


Figure 2-12 Receiver Functional Block Diagram

2-6-1 1300 MHz IF Receiver Module Detailed Theory

Serial Numbers 1005 thru 1406

If the received signal is input from the ANTENNA Connector, it enters at J1003 and is sent through a static protect circuit to the first mixer (See Figure 2-13 and the 1300 MHz IF Receiver Schematic in Section 7 of this Manual.) Relays K1101 and K1102 can be controlled from the front panel ATTENUATOR Switch to attenuate the signal by 0, 20 or 40 dB of attenuation.

If the received signal is input from the TRANS/-40 dB DUPLEX Connector, it enters at J1005 and is switched to the first mixer when its control line at FL1003 is pulled high.

NOTE

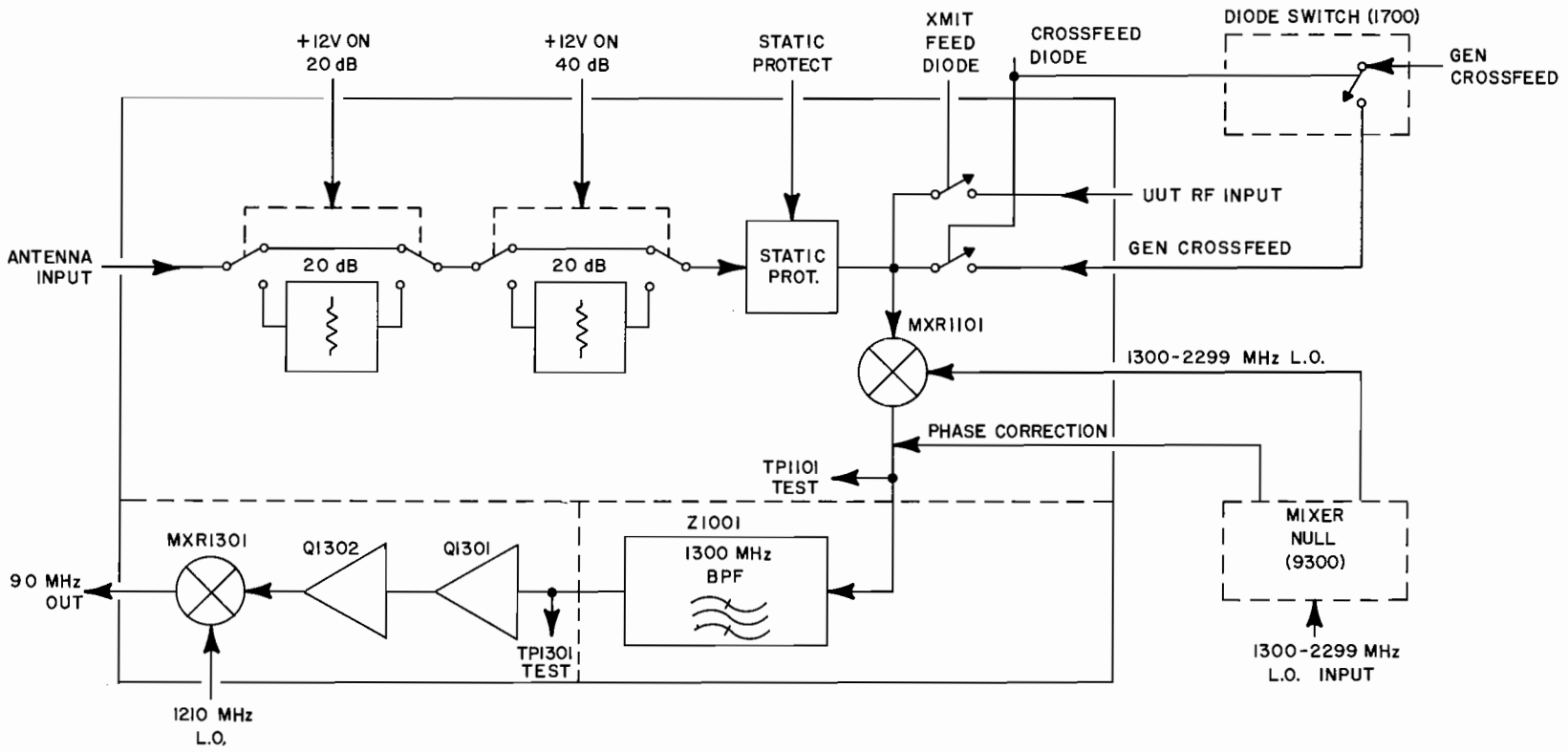
The control line logic for the Crossfeed Diode, XMIT Feed Diode and +12 V on Static Protect lines is located on the Demod Audio PC Board.

If the received (crossfeed) signal is input from the Generator Functional Block (in Generate Simplex mode of operation), it is input at J1004 and is switched to the first mixer when its control line at FL1002 is pulled high. Notice that the control line at FL1002 also controls the Diode Switch Module. The received signal is up-converted in the first-mixer, MXR1101, to the 1st IF Frequency of 1300-1300.9999 MHz, and is then fed through a 1300 MHz bandpass filter, Z1001. The up-conversion in the first mixer results from mixing the received frequency with a 1300-2299 MHz input, which enters at J1006 from the Dual VCO. For serial numbers 1235 and subsquent, a Mixer Null module has been added between the Dual VCO and the 1300 MHz IF Receiver for phase control. The phase control input at J1010 nulls out any unwanted signals produced in the first mixer.

The filtered 1300-1300.9999 MHz signal is amplified in two transistor stages, Q1301 and Q1302, and sent to the second mixer, MXR1301. A 1210 MHz signal, from the Dual VCO, is input at J1001 and mixed with the 1300-1300.9999 MHz signal to produce a second IF signal of 89.0001 to 90 MHz. The 89.0001-90 MHz IF is output at J1002 to the 89-90 MHz Receiver Module and to the Spectrum Analyzer RF Module.

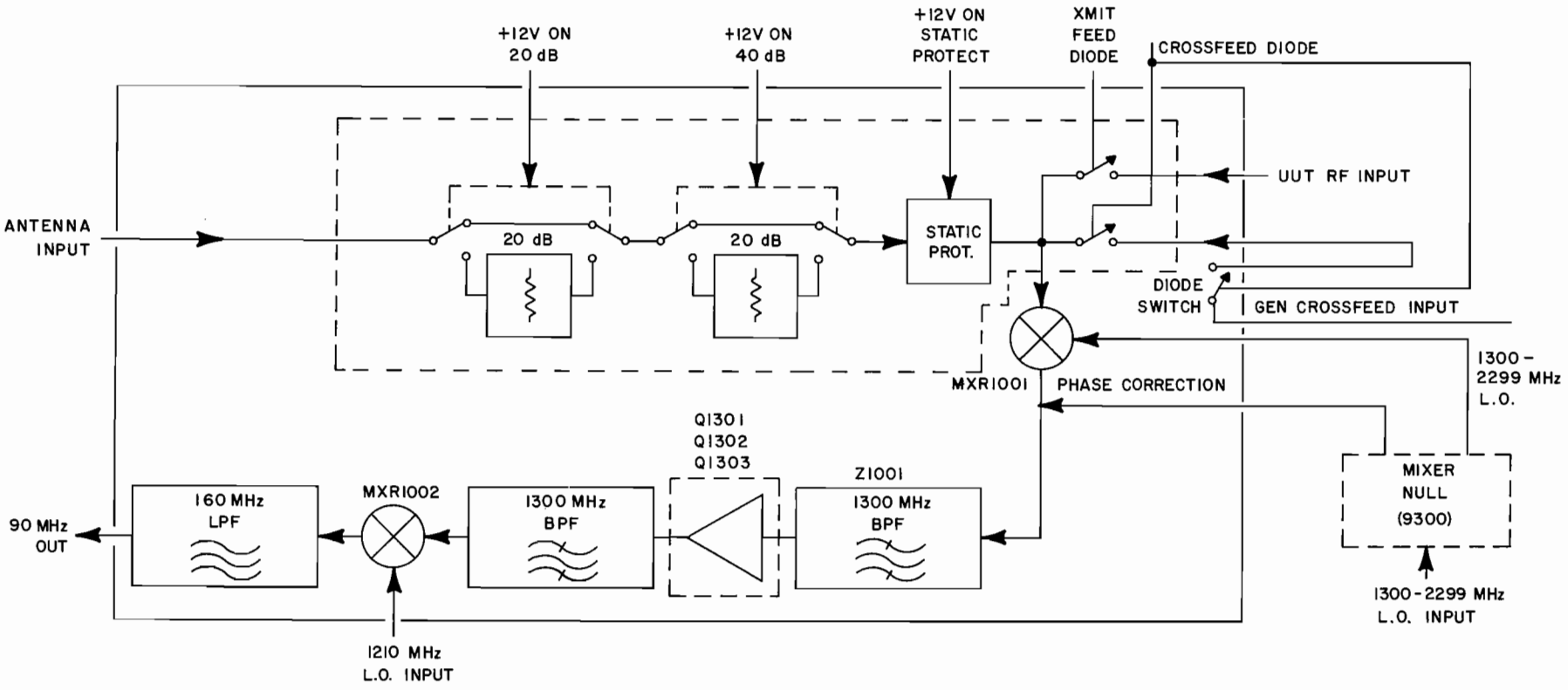
NOTE

The above discussion refers to the 1300 MHz IF Receiver installed in serial numbers 1005 thru 1406. At that time, the module was redesigned and the Diode Switch was incorporated into the new module. Serial numbers thru to 1406 use part number 7005-5041-300 for 1300 MHz IF Receiver modules. les. Serial numbers 1407 and on contain part number 7005-5041-400 for 1300 MHz IF Receiver modules.



Serial No. 1005 thru 1406

Figure 2-13 1300 MHz IF Receiver Detailed Block Diagram



Serial No. 1407 and On

Figure 2-13a 1300 MHz IF Receiver Detailed Block Diagram

Serial Numbers 1407 and On

If the received signal is input from the ANTENNA Connector, it enters at J1003 and is sent through a static protect to the first mixer (See Figure 12-13a). Relays K1101 and K1102 can be controlled from the front panel ATTENUATOR Switch to attenuate the signal by 0, 20 or 40 dB of attenuation.

If the received signal is input from the TRANS/-40 dB DUPLEX Connector, it enters at J1005 and is switched to the first mixer when its control line at FL1003 is pulled high.

NOTE

The control line logic for the Crossfeed Diode, XMIT Feed Diode and +12 V on Static Protect lines is located on the Demod Audio PC Board.

If the received (crossfeed) signal is input from the Generator Functional Block (in Generate Simplex mode of operation), it is input at J1008, switched through the Diode Switch when FL1007 goes high, and jumpered over to J1004 where it is then switched to the first mixer when FL1002 goes high. Notice that FL1007 and FL1002 are tied together and go high at the same time. Whatever the source, the received signal is up-converted in the first mixer, MXR1001, to the 1st IF Frequency of 1300-1300.9999 MHz, and is then fed through a 1300 MHz bandpass filter, Z1001. The up-conversion in the first mixer results from mixing the received frequency with a 1300-2299 MHz L.O. frequency, which is generated by the Dual VCO Module, phase controlled by the Mixer Null Module to null out any 90 MHz spikes, and then input at J1006 and J1010.

The filtered 1300-1300.9999 MHz signal is amplified in three transistor stages, Q1301, Q1302 and Q1303, and sent to the second mixer, MXR1002. A 1210 MHz L.O. signal, from the Dual VCO, is input at J1001 and mixed with the 1300-1300.9999 MHz signal to produce a second IF signal at 89.0001 to 90 MHz. L1001, C1001 and C1002 form a 160 MHz lowpass filter to remove unwanted harmonics. The 89.0001-90 MHz IF is output at J1002 to the 89-90 MHz Receiver Module and to the Spectrum Analyzer RF Module.

2-6-2 89-90 MHz Receiver Module Detailed Theory

The 89.0001 to 90 MHz second IF signal is input at J3802 (See Figure 2-14 and the 89-90 MHz Receiver Schematic in Section 7 of this Manual). It is then amplified by Q2901 and Q2902 and bandpass filtered in five stages, L2907 thru L2911. A 79.3 to 78.3001 MHz signal, from the Low Loop section of the Frequency Synthesis Functional Block, is mixed with the second IF frequency in MXR2901 to produce a third IF frequency of 10.7 MHz. The 10.7 MHz IF signal is amplified by Q2903 and Q2904 before passing through selected bandpass filters of 200 kHz, 15 kHz or 6 kHz.

NOTE

The desired bandpass filter is selected by the setting of the MODULATION Control on the front panel as follows:

AM1, SSB - 6 kHz
AM2, FM1 - 15 kHz
FM2, FM3, FM4 - 200 kHz

The 10.7 MHz IF is amplified by Q2910 before it is mixed in Q2911 with a 10 MHz reference signal. The resulting 700 kHz final IF is buffered by Q2912 and output at J3805 to the Demod Audio PC Board and to the Oscilloscope Control and Deflection PC Board.

Automatic Gain Control (AGC) is provided by the input at pin 5 of J3803, from the Demod Audio PC Board. The more negative this input goes, the smaller is the amplification done by Q2903, Q2904 and Q2910.

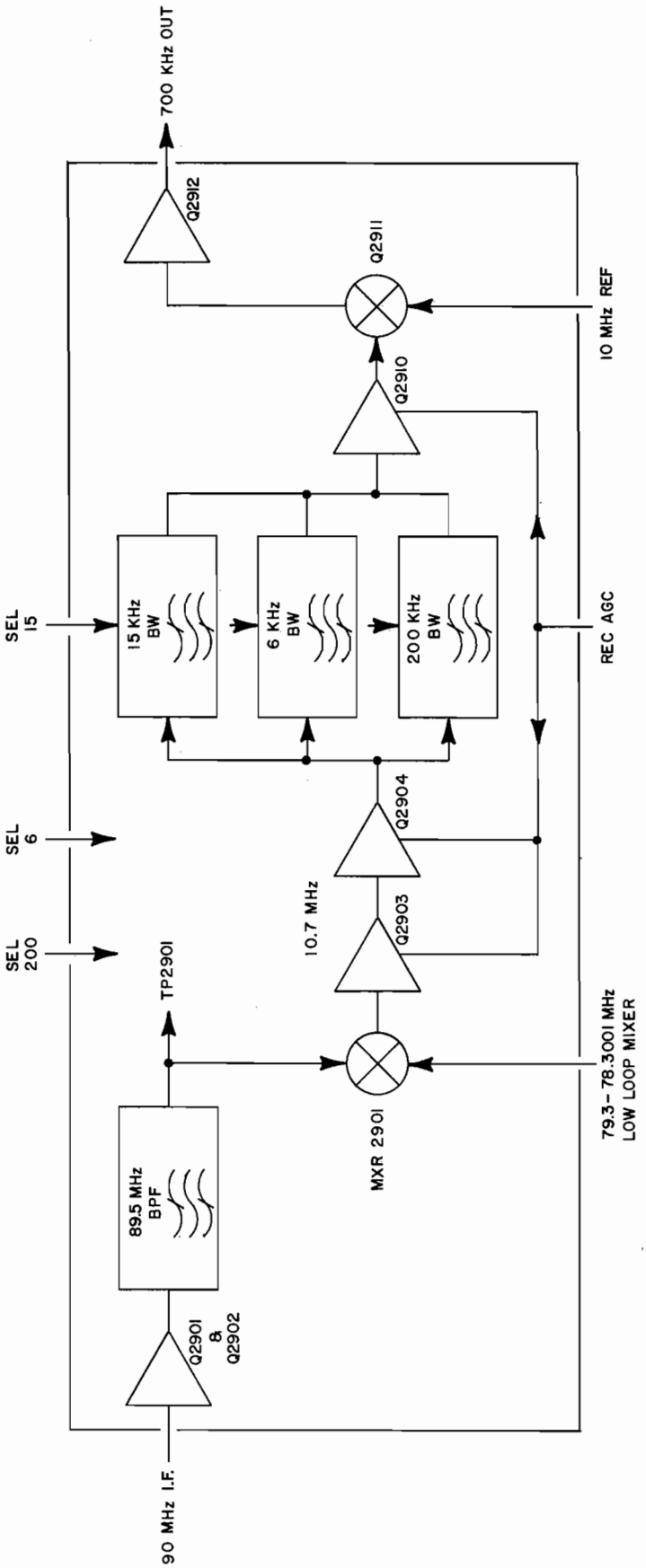


Figure 2-14 89-90 MHz Receiver Detailed Block Diagram

2-6-3 Demod Audio PC Board Detailed Theory

NOTE

Use paragraph 2-6-3 for Demod Audio PC Board 7010-5034-700 and Demod Audio PC Board Schematic 0000-5014-700. These drawings are effective for FM/AM-1500 serial numbers 1005 thru 1425.

FM Dectector Circuit

The 700 kHz IF input at J4704, from the 89-90 MHz Receiver Module, divides to go to the AM Detector circuit and to the FM detector circuit (See Figure 2-15a and the Demod Audio PC Board Schematic in Section 7 of this Manual.) The FM Detector Circuit consists of Q4701, Q4703 thru Q4707, U4701 and U4725A. Q4701 amplifies the 700 kHz signal before applying it to the squaring amp. The squaring amp, U4701, produces a square wave from the 700 kHz IF. The output of the squaring amp is applied to Q4703. Q4703 will turn on Q4704 during the rising edge of its square wave input, via R4714 and C4721. On the falling edge of the square wave, Q4703 will turn off, causing Q4705 to turn on via R4715, R4713 and C4720. When Q4705 turns on, C4731 is charged via Q4706. When Q4704 turns on, the charge on C4731 is dumped, via Q4707, into the low-pass filter, which consists of L4703, L4704, C4732, C4733 and C4744. The low-pass filter produces a positive DC voltage by averaging the energy which is dumped into it by C4731 and Q4707. This DC level will increase as the frequency of the incoming pulses increases. U4725A amplifies this DC level, and its output contains the demodulated FM audio.

AM Dectector Cirucit

The 700 kHz IF is applied to Q4702, which amplifies the 700 kHz IF and mixes it with any single sideband injection signal that is applied when in SSB. The output of Q4702 is applied to a detector consisting of CR4702 and U4725B. CR4702 charges C4725 on each positive half cycle of the IF input. U4725B buffers the charge on C4725. The output of U4725B contains the demodulated AM audio and the receiver AGC information. The demodulated AM audio is applied to U4751B, which selects between demodulated AM or FM.

U4744, U4751C and Q4708 process the AGC information. Q4708 increases charge current for the integrator when in AM, preventing the AGC from canceling out the AM audio. U4744A provides feedback for the integrator, U4744B. The output of U4744B is applied to the AGC input of the 89-90 MHz Receiver Module. The output of U4744B is also applied to U4743A. U4743A is the signal level amplifier for the squelch circuit. The output of U4743A, which is inverted, is applied to the squelch comparator, U4743B. U4743B compares the output of U4743A with the setting of the SQUELCH Control on the front panel. The output of U4743B is applied to the squelch switch, U4751A, and to Q4709 which drives the SIG Indicator (57) on the front panel. In addition, the squelch output is applied to U4703A to disable the FREQ ERROR Meter (41) and is also applied to the I/O PC Board to disable the digital FREQ ERROR Meter. The meters are disabled when squelch is not broken.

700 kHz SSB Generator Circuit

A 1 kHz reference frequency, input at pin 3 of P4701, clocks U4717 which is a phase lock loop (PLL) chip. U4709 is a divide-by 700 ripple counter. The 1 kHz output of U4709, at pin 14, is phase locked to the reference frequency. The 700 kHz output of U4717, at pin 4, is determined by R4723, R4732, C4729 and C4728. Only when the SSB line is high at the inputs to U4726A will the PLL chip not be inhibited.

SINAD Circuit

The SINAD signal, from the Oscilloscope Control and Deflection PC Board, enters at pin 18 of P4702. The SINAD circuit consists of U4775, U4766, U4765 and U4756. U4775A is a variable gain amplifier whose gain is controlled by an opto-isolator, U4783. The incoming audio is full-wave rectified by U4775B and U4765A and applied to an integrator, U4765B. U4765B smooths out the rectified audio signal. The output of U4765B is applied to U4783, the opto-isolator. As the signal under test increases, the gain of U4775A decreases, keeping the output level of U4775A constant.

The output of U4765B is also applied to a low level comparator, U4756A. U4756A compares the output of the integrator with a pre-determined value. If the output of the integrator is too low to accurately measure SINAD, the comparator forces the output line to the meter positive via CR4729. This causes the meter to peg to the right, indicating that the signal is unreliable.

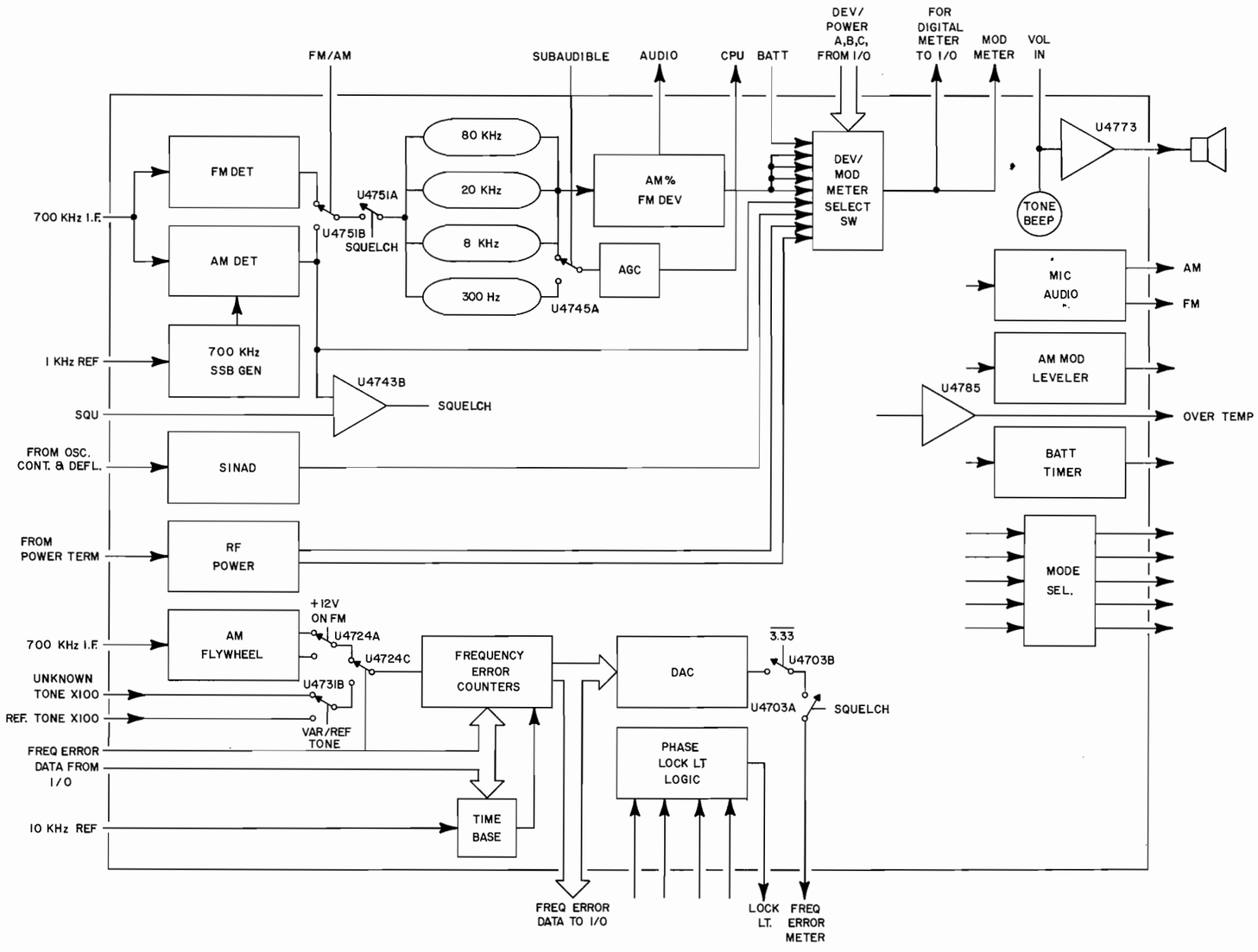
The output of U4775A is also applied to a 1 kHz notch filter, U4766A. U4766A removes the 1 kHz audio tone and leaves only noise and distortion in its output. The noise and distortion is full-wave rectified by U4766B and U4756B. The output of the rectifier is smoothed out to a DC level by R4862 and C4762 before being applied to the meter switch.

MIC Audio Circuit

Microphone audio, input at pin 20 of P4703, is amplified by U4757 and clipped by CR4740 and CR4739. R4897 is provided for AM level adjustment and R4896 is provided for FM level adjustment. Switch U4750 selects between AM and FM, as controlled by the AM/FM Swich. The selected output is sent to the Dual Tone Generator PC Board.

Mode Select Circuit

The Mode Select circuit is a logic array consisting of U4768B, U4768C, U4768D, U4786, U4777 and Q4721 thru Q4724. This logic array controls the crossfeed Diode Switch, Static Protect Relay, Power Termination Relay, XMTR Feed Diode Switch and the +12 V on Generate line. A truth table for this logic array is shown in Table 2-1a.



EFFECTIVE SER. NO. 1005 THRU 1425

Figure 2-15 Demod Audio PC Board Detailed Block Diagram

INPUTS					OUTPUTS				
(ACTIVE LOW) MIKE KEY	REC	DUPLEX	XMIT SENS	TRACK	CROSSFEED DIODE	STATIC PROTECT	PWR TERM. RELAY	XMTR FEED DIODE	GEN
0	0	0	0	0	1	0	1	0	1
1	0	0	0	0	1	0	1	0	1
0	1	0	0	0	1	0	1	0	1
1	1	0	0	0	0	1	1	0	0
0	0	1	0	0	0	1	0	0	1
1	0	1	0	0	0	1	0	0	1
0	1	1	0	0	0	1	0	0	1
1	1	1	0	0	0	1	0	0	0
0	0	0	1	0	1	0	0	1	1
1	0	0	1	0	1	0	0	1	1
0	1	0	1	0	1	0	0	1	1
1	1	0	1	0	0	0	0	1	1
0	0	1	1	0	0	0	0	1	1
1	0	1	1	0	0	0	0	1	1
0	1	1	1	0	0	0	0	1	1
1	1	1	1	0	0	0	0	1	1
0	X0	0	0	1	1	1	0	0	1
1	X0	0	0	1	0	1	0	0	1
0	1	0	0	1	1	1	0	0	1
1	1	0	0	1	0	1	0	0	1
0	X0	X1	0	1	1	1	0	0	1
1	X0	X1	0	1	0	1	0	0	1
0	1	X1	0	1	1	1	0	0	1
1	1	X1	0	1	0	1	0	0	1
0	X0	0	1	1	1	0	0	1	1
1	X0	0	1	1	0	0	0	1	1
0	1	0	1	1	1	0	0	1	1
1	1	0	1	1	0	0	0	1	1
0	X0	X1	1	1	1	0	0	1	1
1	X0	X1	1	1	0	0	0	1	1
0	1	X1	1	1	1	0	0	1	1
1	1	X1	1	1	0	0	0	1	1

NOTE: The microprocessor will override Duplex high and REC low when Track is high, as denoted by (X).

EFFECTIVE SER. NO. 1005 THRU 1425

Table 2-2 Demod Audio PC Board Mode Select Logic

RF Power Meter Drive Circuit

Detected power is input at pin 6 of P4702 from the Power Termination Module. U4747B amplifies the signal. R4830 (ZERO PWR ADJ) is provided to set the output of U4747B to zero, with no input signal. Switch U4754B is controlled by the AVG PEAK/PEAK Switch to add U4747A into the line when PEAK is selected. U4753A, U4753B and their respective resistor networks are selected for the 150 W and 15 W scales of the MODULATION Meter. R4829 is the 150 W adjustment, and R4838 is the 15 W adjustment.

% Mod Circuit

The Demod Audio from the selected filter is amplified by U4780A. The signal is then output to the DEMOD OUTPUT Connector, to the Oscilloscope and to the front panel controls. The signal also is switched through selected resistors by U4781, as controlled by the DEV/PWR Control. U4781 also switches in the FM Zero line or the AM Zero line, as selected by switch U4754A. Whenever pin 6 of U4781 is high, as controlled by the DEV/PWR Control, all channels of U4781 are off. When pin 6 of U4781 is low, one pair of channels out of U4781 is on. Pins 9 and 10 determine which pair of channels is on, as controlled by the DEV/PWR A and B lines.

When U4754A selects FM Zero, a preset zero is selected by U4734A, B and C and by U4745C. Only one of these switches will be on at any one time. The switches are driven by the FM1 thru FM4 lines to select a zero for each of the four FM bandwidths. R4771, R4770, R4762 and R4765 set the zero for the bandwidths.

The % Mod Scale part of the circuit consists of U4780B, U4761, U4746, U4752 and U4762B. U4762B buffers the offset signal. The offset signal is a DC level which is used to zero the % AM/kHz DEV level. U4780B amplifies the demodulated audio signal. U4761A and B form a precision full-wave rectifier. The output of the rectifier is smoothed out by R4814 and C4755. U4746B amplifies the charge on C4755. The output of U4746B is the average % Modulation/kHz Deviation. The output of the full-wave rectifier, at pin 7 of U4761B, is also applied to U4752, which is a peak detector. U4752 will charge C4768 via CR4715. The output voltage will be equal to the peak of the full-wave rectifier output. The output signal is applied to U4746A, which buffers the output of U4752 before applying it to U4754C. U4754C selects between Peak % AM/kHz DEV and Peak Average % AM/FM DEV. The output of U4754C is applied to the DEV/% Mod Meter Select Switch.

Phase Lock Light Logic Circuit

Three phase-lock control signals are input to the Demod Audio PC Board: High Loop lock, Low Loop lock and Duplex lock. When all three of these lines are high, pin 3 of U4776 is low. When any of these lines are low, their respective diode (CR4742, CR4744 or CR4745) will be reverse biased, causing pin 3 of U4776 to go high. U4776B and U4776C form an oscillator circuit to present alternating highs and lows to pin 12 of

U4776D. When pin 13 of U4776D is low, pin 11 will be high to turn on Q4718 and light the Freq LOCK Indicator Lamp on the front panel. When pin 13 of U4776D is high, the Freq LOCK Indicator Lamp will flash off and on at the same frequency as the oscillator at pin 12. Also, when pin 3 of U4776 is high, Q4719 will conduct to output a +12 V Unlock signal to the I/O PC Board.

When the GEN/LOCK Control is not in the Lock position, +12 V is input at pin 3 of P4703. This will cause the Freq LOCK Indicator Lamp to flash and +12 V to be output to the I/O board in the same manner as the phase-lock lines.

Battery Timer and Control Circuit

The Battery Timer and Control Circuit consists of Q4715, Q4716, Q4717, U4749, U4767A and U4748. Q4717 conducts when the front panel PWR/OFF/BATT Switch is set to BATT. When Q4717 conducts, U4767A changes states. CR4737, CR4738, C4774 and C4775 determine which input (S or R) to flip-flop U4767A will become active. If the flip-flop is set, C4774 will be fully charged, allowing the reset line to go high first. The set input cannot go high until C4775 charges. By the time C4775 charges, C4776 is charged and Q4717 is no longer able to drive an input of the flip-flop. If the flip-flop is reset when Q4717 conducts, the opposite actions occur. Thus, the flip-flop toggles each time Q4717 starts conducting.

The Q output of U4767A turns on Q4716, which outputs a control signal to put the FM/AM-1500 power supply into battery operation. The $\overline{Q}$ output, when low, turns on Q4715, causing power to be applied to the battery timer and to the low voltage cutoff. The battery timer, U4749, produces a logic 1 at pin 13 after 7 to 11 minutes. This logic 1 will reset flip-flop U4767A via CR4734. When the flip-flop is reset, the power supply, battery timer and low voltage cutoff circuits are turned off.

The low voltage cutoff circuit consists of a comparator, U4748, and a zener diode, CR4726. A sample of the battery voltage is applied to the negative input of the comparator via a voltage divider consisting of R4869, R4871 and R4872. The positive side of the comparator is connected to the zener diode, which regulates it to approximately 5 volts. When the battery voltage drops below a predetermined level, the negative input of the comparator will fall below the zener diode voltage. This causes the output of the comparator to go positive and reset flip-flop U4767A, turning the FM/AM-1500 off.

AM Modulation Leveler Circuit

AM modulation is input at pin 13 of P4702 from the Dual Tone Generator PC Board. U4784B amplifies the signal for output to the Output Amplifier Module, which controls the AM modulator level of the Duplex Offset Module. R4963 is provided for AM% modulation adjustment. R4959 is provided for RF level adjustment. R4961 is provided for RF level linearity adjustment.

AM Flywheel Circuit

The AM Flywheel circuit consists of Q4713, U4724A, U4724B, U4716, U4708 and U4733. Q4713 buffers the 700 kHz IF signal input at J4706 and applies this signal to a CMOS Switch, U4724B, and to a comparator, U4708. U4708 is used in FM only. The output of U4708 is a square wave with a frequency equal to the frequency of the 700 kHz IF. U4724B, along with U4716, operates as a phase/frequency detector. The output of the integrator, U4716, is a DC voltage which steers the output frequency of the VCO, U4733, in the appropriate direction to make the frequencies equal at pins 10 and 15 of U4724B. This phase-locked loop generates a square wave, at pin 4 of U4733, with a frequency equal to the 700 kHz IF input. When over-modulation of the carrier signal occurs, integrator U4716 holds its output at a relatively constant level during the interval when the carrier is suppressed. When the carrier is not suppressed, the phase-lock loop corrects for any drift which may have occurred during the time the carrier was suppressed. U4724A selects between the output of the phase-locked loop for AM demodulation and the output of the comparator, U4708, for FM demodulation.

Time Base Circuit

The Time Base circuit consists of Q4714, U4742, U4741, U4731, U4732, U4722, U4723, U4737B, U4737C, U4729C, U4740 and U4739. This circuit provides the time base frequency for the frequency error counter.

Q4714 buffers the 10 kHz input from the Clock Divider, at pin 18 of P4703, and applies this signal to U4742A and U4732A. U4742A, U4742B, U4741A and U4741B are decade counters which function as divide-by 10 frequency dividers. These dividers produce frequencies at 1 kHz, 100 Hz and 10 Hz. These outputs are applied to CMOS Switches U4732B, U4731C and U4731A, respectively. The four CMOS Switches (U4731A, U4731C, U4732B and U4732A) select one of the time base frequencies of 10 Hz, 100 Hz, 1 kHz and 10 kHz, respectively. The switches are driven by the time base select logic.

The time base select logic consists of U4715, U4722A, U4722B, U4722C, U4723A, U4723B and U4723C. Table 2-2a is a truth table which describes the operation of the time base logic. The time base select logic receives frequency error settings from the I/O PC Board and turns on the appropriate CMOS Switch. In addition, the time base select logic also produces a control line which informs the frequency error counter when to count in the audio mode. This control line is driven by pin 9 of U4722B.

U4729C, U4737C and U4737B drive control lines for the frequency error counter. These control lines are the 1.0 second, 0.1 second and 0.01 second time bases. When all three of these lines are inactive, the 0.001 second time base is selected. The selected time base line is applied to U4740 which, along with U4739A, produces the gate for the frequency error counter.

FREQ ERROR D C B A	U4722B Pin 9	U4723C Pin 10	U4722A Pin 6	U4723B Pin 9	U4723A Pin 6	U4715 Pin 2
0 0 0 0	1	1	0	1	1	0
0 0 0 1	1	1	1	0	1	0
0 0 1 0	1	1	1	1	1	1
0 0 1 1	0	0	1	1	1	0
0 1 0 0	0	0	1	1	0	0
0 1 0 1	0	1	0	1	1	0
0 1 1 0	0	1	0	1	0	0
0 1 1 1	0	1	1	0	1	0
1 0 0 0	0	1	1	0	0	0

Table 2-3 Time Base Logic
(Effective Ser.No. 1005 thru 1425)

Assume that U4739A is reset and that U4740 has just been loaded with $0000_{(2)}$. Under these conditions, the COUNT ENABLE line is high, stopping the frequency error counter from counting. On the next rising, edge of the clock, the counter decrements, reducing the contents of the counter by 1 and yielding a count of $1001_{(2)}$. When this happens, the output at pin 2 of U4740 goes high, causing U4739 to change states and the COUNT ENABLE line to go low (active state). The COUNT ENABLE line stays low for 10 counts. When the counter underflows from $0000_{(2)}$ to $1001_{(2)}$, pin 2 of U4740 again makes a low to high transition, causing U4739 to change states and the COUNT ENABLE line to go high (inactive state). When this line goes high, U4740 is set to $0000_{(2)}$ via C4747 and R4780. One count later, the counter again underflows from $0000_{(2)}$ to $1001_{(2)}$, causing U4739 to change states. The counter, U4740, is then allowed to decrement for ten counts and then the cycle repeats itself. The net result is a pulse which is high for one clock period and low for ten clock periods, and which appears on the COUNT ENABLE line.

Frequency Error Counter Circuit

The Frequency Error Counter Circuit consists of the following IC's:

U4705
U4707
U4710
U4711
U4713
U4718 A & B
U4719
U4720
U4721
U4724C
U4727
U4728
U4729 A, B, D, E & F
U4730
U4731B
U4732
U4736 A, B & D
U4737 A & D
U4738
U4739B

The frequency error counter is a 24 bit binary, presettable up/down counter. Only the lower 8 bits are available at its output. These 8 bits represent the frequency error. When the frequency error counter is in the audio mode, it functions as an up/down counter. At the beginning of each conversion, the frequency error counter is preset to C$\emptyset\emptyset 8\emptyset_{(H)}$. During the first gate, the counter counts up using the unknown tone. During the second gate, the counter counts down using the reference tone. If the two tones are equal, the resulting count is C$\emptyset\emptyset 8\emptyset_{(H)}$. The lower 8 bits ($8\emptyset_{(H)}$) are latched and applied to the digital to analog converter and to the I/O PC Board. $8\emptyset_{(H)}$ is interpreted as zero. Anything greater than this is interpreted as positive, while anything less is interpreted as negative. If the unknown tone is greater than the reference tone, the result will be positive since the counter counted up more than it counted down. If the unknown tone is less than the reference tone, the result will be negative since the counter counted down more counts than it counted up.

When operating in the RF mode, the counter counts up only. The counter is loaded with a preset value prior to each gate. The gate enables the counting of the 700 kHz IF. If the 700 kHz IF is exactly 700 kHz, the resulting count will be C$\emptyset\emptyset 8\emptyset_{(H)}$, which is interpreted as zero. If the 700 kHz IF is less than 700 kHz, the final count will be less than C$\emptyset\emptyset 8\emptyset_{(H)}$ and will be interpreted as a negative value. If the 700 kHz IF is greater than 700 kHz, the final count will be greater than C$\emptyset\emptyset 8\emptyset_{(H)}$ and will be interpreted as a positive value. In both audio and RF modes, the difference between $8\emptyset_{(H)}$ and the counter's 8 bit output represents the magnitude of the frequency error.

The up/down counter consists of U4712, U4721, U4720, U4711 and U4705. The lower 8 bits of this counter are applied to U4713, which latches the counters' output when the $\overline{\text{COUNT ENABLE}}$ line goes high. The output of U4713 is applied to U4707 and to U4714, a pair of demultiplexers which select between the counter outputs and the OVER/$\overline{\text{UNDER}}$ line.

When an overflow or underflow condition occurs, the upper 12 bits of the counter are applied to the overflow/underflow logic consisting of U4719, U4718A, U4736B, C & D, U4737 A & D and U4738. This logic checks for C$\emptyset\emptyset_{(H)}$ on the upper 12 bits of the counter. If the count is less than C$\emptyset\emptyset_{(H)}$, the logic will indicate an underflow (meter peg = 1; OVER/$\overline{\text{UNDER}}$ = $\emptyset$). If the count is greater than C$\emptyset\emptyset_{(H)}$, an overflow condition is generated (meter peg = $\emptyset$; OVER/$\overline{\text{UNDER}}$ = 1).

The preset logic, consisting of U4732C, U4730A and U4730B, controls the presetting of the counters. When counting RF, the CMOS Switch, U4732C, applies the $\overline{\text{COUNT ENABLE}}$ signal to the astable multivibrators, U4730 A & B. These astable multivibrators produce a delayed pulse to ensure that everything has settled before presetting the counters. The output of U4730B is applied to the reset inputs of the counters and to the reset input of U4739B. U4739B produces the UP/DOWN count signal and the VAR TONE/REF TONE signal. When in the RF mode, this flip-flop is reset everytime the gate goes high, forcing the counters to count up only.

In the audio mode, the output of U4739B is applied to U4730A by U4732C. In this mode, U4739B is reset on every other gate cycle. During the first cycle, U4731B selects the unknown tone and the UP/DOWN line is high. During the second gate cycle, U4731B selects the reference tone. The output of U4731B is applied to the clock input of the counters via U4729F. CR4746 disables the clock while the COUNT ENABLE line is high. U4724C selects between audio (output of U4731B) and RF (output of U4724A in the AM Flywheel circuit) as controlled by the UP ON AUDIO line.

Overtemp Circuit

When the thermistor in the Power Termination Module senses an overtemp condition, its signal is input at pin 24 of P4703. When pin 2 of U4785 reaches a pre-determined level, pin 6 will go high to turn on Q4720. This will turn on the OVERTEMP Indicator Lamp on the front panel and also send a +12 V on Overtemp signal to the I/O PC Board.

Tone Beep Circuit

The KEYDOWN line from the I/O PC Board enters at pin 4 of J4705. When this line is high, Q4712 is on. When this line is low, Q4712 is off to allow the oscillator to function. U4763 and associated components form a 1 kHz Beep Oscillator. R4842 sets the volume level of the Oscillator. The audio-in line at pin 4 of P4702 mixes with the oscillator output and is amplified by U4773, an audio amplifier, for output to the speaker.

2-6-3a Demod Audio PC Board Detailed Theory
(Effective Ser.No. 1426 and on)

NOTE

Use paragraph 2-6-3a for Demod Audio PC Board 7010-5037-300 and Demod Audio PC Board Schematic 0000- 5017-300.

FM Detector Circuit

The 700 kHz IF input at J4704, from the 89-90 MHz Receiver Module, divides to go to the AM detector circuit and to the FM detector circuit (See FIgure 2-15b and the Demod Audio Schematic in Section 7 of this Manual.) The FM Detector Circuit consists of Q4701, Q4704, Q4705, Q4706, Q4708, Q4709, U4701 and U4733A. Q4701 amplifies the 700 kHz signal before applying it to the squaring amp. The squaring amp, U4701, produces a square wave from the 700 kHz IF. The output of the squaring amp is applied to Q4704. Q4704 will turn on Q4706 during the rising edge of its square wave input, via R4751 and C4750. On the falling edge of the square wave, Q4704 will turn off, causing Q4705 to turn on via R4752, R4750 and C4749. When Q4705 turns on, C4755 is charged via Q4708. When Q4706 turns on, the charge on C4755 is dumped, via Q4709, into the low-pass filter, which consists of L4703, L4704, C4756, C4757 and C4772. The low-pass filter produces a positive DC voltage by averaging the energy which is dumped into it by C4755 and Q4709. This DC level will increase as the frequency of the incoming pulses increases. U4733A amplifies this DC level, and its output contains the demodulated FM audio.

AM Detector Circuit

The 700 kHz IF is applied to Q4702, which amplifies the 700 kHz IF and mixes it with any single sideband injection signal that is applied when in SSB. The output of Q4702 is applied to a detector consisting of CR4702 and U4733B. CR4702 charges C4754 on each positive half cycle of the IF input. U4733B buffers the charge on C4754. The output of U4733B contains the demodulated AM audio and the receiver AGC information. The demodulated AM audio is applied to U4749B, which selects between demodulated AM or FM.

U4750, U4749C and Q4710 process the AGC information. Q4710 increases charge current for the integrator when in AM, preventing the AGC from canceling out the AM audio. U4750A provides feedback for the integrator, U4750B. The output of U4750B is applied to the AGC input of the 89-90 MHz Receiver Module. The output of U4750B is also applied to U4751A. U4751A is the signal level amplifier for the squelch circuit. The output of U4743A, which is inverted, is applied to the squelch comparator, U4751B. U4751B compares the output of U4751A with the setting of the SQUELCH Control on the front panel. The output of U4751B is applied to the squelch switch, U4749A, and to Q4712 which drives the SIG Indicator Lamp on the front panel. In addition, the

squelch output is applied to U4730B to disable the FREQ ERROR Meter and is also applied to the I/O PC Board to disable the digital FREQ ERROR Meter. The meters are disabled when squelch is not broken.

700 kHz SSB Generator Circuit

A 1 kHz reference frequency, input at pin 3 of P4701, clocks U4782 which is a phase lock loop (PLL) chip. U4768 is a divide-by 700 ripple counter. The 1 kHz output of U4768, at pin 14, is phase locked to the reference frequency. The 700 kHz output of U4782, at pin 4, is determined by R4944, R4945, C4820 and C4821. Only when the SSB line is high at the inputs to U4783B will the PLL chip not be inhibited.

SINAD Circuit

The SINAD signal, from the Oscilloscope Control and Deflection PC Board, enters at pin 18 of P4702. The SINAD circuit consists of U4735, U4753, U4734 and U4752. U4735A is a variable gain amplifier whose gain is controlled by an opto-isolator, U4754. The incoming audio is full-wave rectified by U4735B and U4734A and applied to an integrator, U4734B. U4734B smooths out the rectified audio signal. The output of U4734B is applied to U4754, the opto-isolator. As the signal under test increases, the gain of U4735A decreases, keeping the output level of U4735A constant.

The output of U4734B is also applied to a low level comparator, U4752A. U4752A compares the output of the integrator with a pre-determined value. If the output of the integrator is too low to accurately measure SINAD, the comparator forces the output line to the meter positive via CR4716. This causes the meter to peg to the right, indicating that the signal is unreliable.

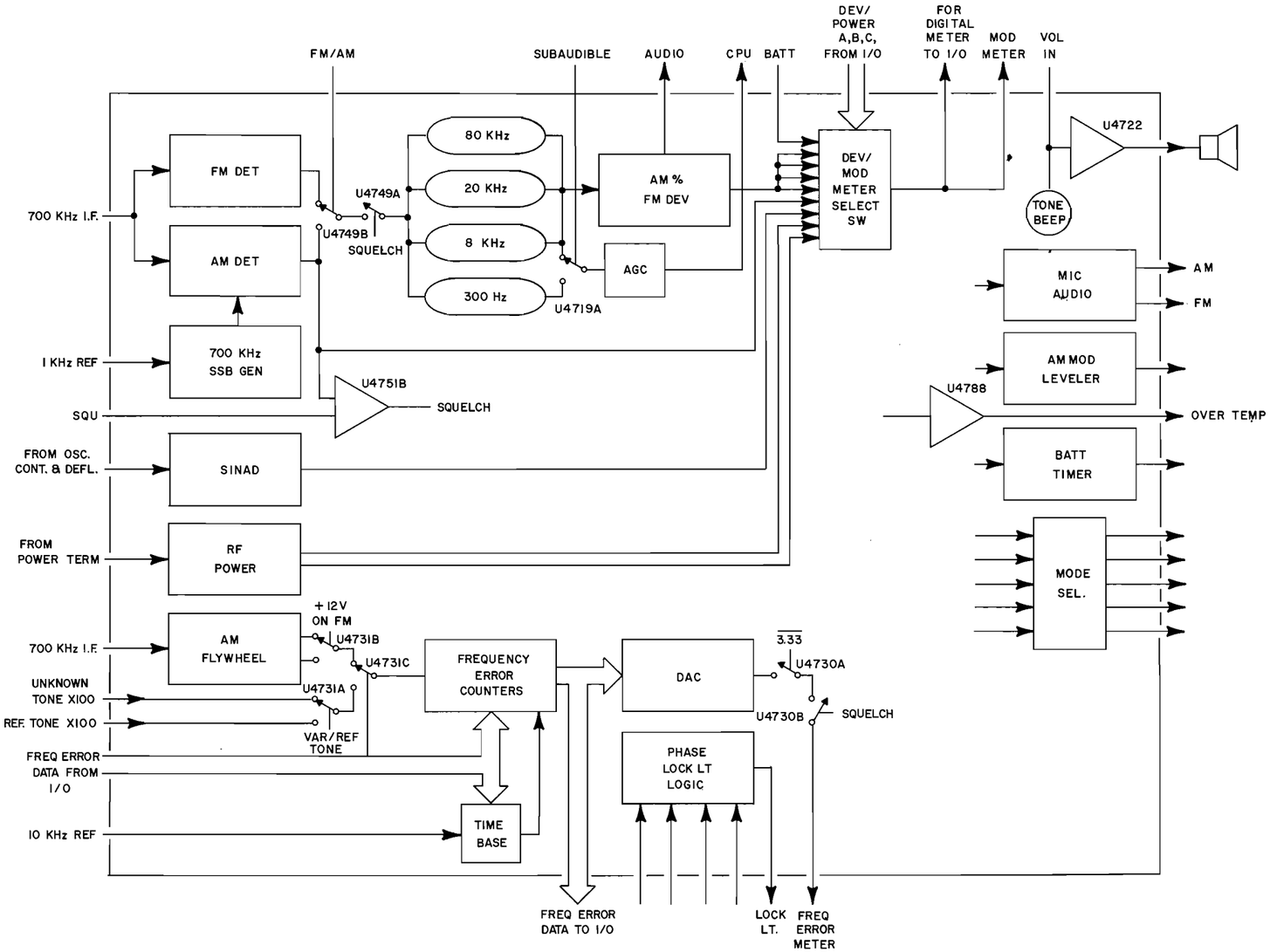
The output of U4735A is also applied to a 1 kHz notch filter, U4753A. U4753A removes the 1 kHz audio tone and leaves only noise and distortion in its output. The noise and distortion is full-wave rectified by U4753B and U4752B. The output of the rectifier is smoothed out to a DC level by R4852 and C4785 before being applied to the meter switch.

MIC Audio Circuit

Microphone audio, input at pin 20 of P4703, is amplified by U4778 and clipped by CR4739 and CR4738. R4933 is provided for AM level adjustment and R4932 is provided for FM level adjustment. Switch U4779 selects between AM and FM, as controlled by the AM/FM Swich. The selected output is sent to the Dual Tone Generator PC Board.

Mode Select Circuit

The Mode Select circuit is a logic array consisting of U4780, U4781, U4789 and Q4721 thru Q4724. This logic array controls the crossfeed Diode Switch, Static Protect Relay, Power Termination Relay, XMTR Feed Diode Switch and the +12 V on Generate line. A truth table for this logic array is shown in Table 2-1b.



EFFECTIVE SER. NO. 1426 AND ON

Figure 2-15a Demod Audio PC Board Detailed Block Diagram

INPUTS					OUTPUTS				
(ACTIVE LOW) MIKE KEY	REC	DUPLEX	XMIT SENS	TRACK	CROSSFEED DIODE	STATIC PROTECT	PWR TERM. RELAY	XMTR FEED DIODE	GEN
0	0	0	0	0	1	0	1	0	1
1	0	0	0	0	1	0	1	0	1
0	1	0	0	0	1	0	1	0	1
1	1	0	0	0	0	1	1	0	0
0	0	1	0	0	0	1	0	0	1
1	0	1	0	0	0	1	0	0	1
0	1	1	0	0	0	1	0	0	1
1	1	1	0	0	0	1	0	0	0
0	0	0	1	0	1	0	0	1	1
1	0	0	1	0	1	0	0	1	1
0	1	0	1	0	1	0	0	1	1
1	1	0	1	0	0	0	0	1	1
0	0	1	1	0	0	0	0	1	1
1	0	1	1	0	0	0	0	1	1
0	1	1	1	0	0	0	0	1	1
1	1	1	1	0	0	0	0	1	1
0	X0	0	0	1	1	1	0	0	1
1	X0	0	0	1	0	1	0	0	1
0	1	0	0	1	1	1	0	0	1
1	1	0	0	1	0	1	0	0	1
0	X0	X1	0	1	1	1	0	0	1
1	X0	X1	0	1	0	1	0	0	1
0	1	X1	0	1	1	1	0	0	1
1	1	X1	0	1	0	1	0	0	1
0	X0	0	1	1	1	0	0	1	1
1	X0	0	1	1	0	0	0	1	1
0	1	0	1	1	1	0	0	1	1
1	1	0	1	1	0	0	0	1	1
0	X0	X1	1	1	1	0	0	1	1
1	X0	X1	1	1	0	0	0	1	1
0	1	X1	1	1	1	0	0	1	1
1	1	X1	1	1	0	0	0	1	1

NOTE: The microprocessor will override Duplex high and REC low when Track is high, as denoted by (X).

Table 2-2a Demod Audio PC Board Mode Select Logic (Effective Ser. No. 1426 and on)

RF Power Meter Drive Circuit

Detected power is input at pin 6 of P4702 from the Power Termination Module. U4756B amplifies the signal. R4871 (ZERO PWR ADJ) is provided to set the output of U4756B to zero, with no input signal. Switch U4774A is controlled by the AVG PEAK/PEAK Switch to add U4756A into the line when PEAK is selected. U4757B, U4757A and their respective resistor networks are selected for the 150 W and 15 W scales of the MODULATION Meter. R4881 is the 150 W adjustment, and R4904 is the 15 W adjustment.

% Mod Circuit

The Demod Audio from the selected filter is amplified by U4784A. The signal is then output to the DEMOD OUTPUT Connector, to the Oscilloscope and to the front panel controls. The signal also is switched through selected resistors by U4790, as controlled by the DEV/PWR Control. U4790 also switches in the FM Zero line or the AM Zero line, as selected by switch U4774B. Whenever pin 6 of U4790 is high, as controlled by the DEV/PWR Control, all channels of U4790 are off. When pin 6 of U4790 is low, one pair of channels out of U4790 is on. Pins 9 and 10 determine which pair of channels is on, as controlled by the DEV/PWR A and B lines.

When U4774B selects FM Zero, a preset zero is selected by U4769A, B and C or by U4719C. Only one of these switches will be on at any one time. The switches are driven by the FM1 thru FM4 lines to select a zero for each of the four FM bandwidths. RN4702 - A thru D sets the zero for the bandwidths.

The % Mod Scale part of the circuit consists of U4784B, U4770, U4773, U4771 and U4785B. U4785B buffers the offset signal. The offset signal is a DC level which is used to zero the % AM/kHz DEV level. U4784B amplifies the demodulated audio signal. U4770A and B form a precision full-wave rectifier. The output of the rectifier is smoothed out by R4899 and C4813. U4773B amplifies the charge on C4813. The output of U4773B is the average % Modulation/kHz Deviation. The output of the full-wave rectifier, at pin 7 of U4770B, is also applied to U4771, which is a peak detector. U4771 will charge C4807 via CR4722. The output voltage will be equal to the peak of the full-wave rectifier output. The output signal is applied to U4773A, which buffers the output of U4771 before applying it to U4774C. U4774C selects between Peak % AM/kHz DEV and Peak Average % AM/FM DEV. The output of U4774C is applied to the DEV/% Mod Meter Select Switch.

Phase Lock Light Logic Circuit

Three phase-lock control signals are input to the Demod Audio PC Board: High Loop lock, Low Loop lock and Duplex lock. When all three of these lines are high, pin 3 of U4777 is low. When any of these lines are low, their respective diode (CR4741, CR4743 or CR4742) will be reverse biased, causing pin 3 of U4777 to go high. U4777B and U4777C form an oscillator circuit to present alternating highs and lows to pin 12 of

U4777D. When pin 13 of U4777D is low, pin 11 will be high to turn on Q4714 and light the Freq LOCK Indicator Lamp on the front panel. When pin 13 of U4777D is high, the Freq LOCK Indicator Lamp will flash off and on at the same frequency as the oscillator at pin 12. Also, when pin 3 of U4777 is high, Q4715 will conduct to output a +12 V Unlock signal to the I/O PC Board.

When the GEN/LOCK Control is not in the Lock position, +12 V is input at pin 3 of P4703. This will cause the Freq LOCK Indicator Lamp to flash and +12 V to be output to the I/O board in the same manner as the phase-lock lines.

Battery Timer and Control Circuit

The Battery Timer and Control Circuit consists of Q4713, Q4719, Q4716, U4791, U4776 and U4787. Q4716 conducts when the front panel PWR/OFF/BATT Switch is set to BATT. When Q4716 conducts, U4776A changes states. CR4733, CR4735, C4817 and C4829 determine which input (S or R) to flip-flop U4776A will become active. If the flip-flop is set, C4829 will be fully charged, allowing the reset line to go high first. The set input cannot go high until C4817 charges. By the time C4817 charges, C4833 is charged and Q4716 is no longer able to drive an input of the flip-flop. If the flip-flop is reset when Q4716 conducts, the opposite actions occur. Thus, the flip-flop toggles each time Q4716 starts conducting.

The Q output of U4776A turns on Q4719, which outputs a control signal to put the FM/AM-1500 power supply into battery operation. The $\overline{Q}$ output, when low, turns on Q4713, causing power to be applied to the battery timer and to the low voltage cutoff. The battery timer, U4791, produces a logic 1 at pin 13 after 7 to 11 minutes. This logic 1 will reset flip-flop U4776A via CR4738. When the flip-flop is reset, the power supply, battery timer and low voltage cutoff circuits are turned off.

The low voltage cutoff circuit consists of a comparator, U4787, and a zener diode, CR4736. A sample of the battery voltage is applied to the negative input of the comparator via a voltage divider consisting of R4982, R4981 and R4919. The positive side of the comparator is connected to the zener diode, which regulates it to approximately 5 volts. When the battery voltage drops below a predetermined level, the negative input of the comparator will fall below the zener diode voltage. This causes the output of the comparator to go positive and reset flip-flop U4776A, turning the FM/AM-1500 off.

AM Modulation Leveler Circuit

AM modulation is input at pin 13 of P4702 from the Dual Tone Generator PC Board. U4786A and U4786B amplify the signal for output to the Output Amplifier Module, which controls the AM modulator level of the Duplex Offset Module. R4973 is provided for AM% modulation adjustment. R4963 is provided for RF level adjustment. R4961 is provided for RF level linearity adjustment.

AM Flywheel Circuit

The AM Flywheel circuit consists of Q4703, U4715, U4716, U4717, U4731 and U4732. Q4703 buffers the 700 kHz IF signal input at J4706 and applies this signal to a CMOS Switch, U4715, and to a comparator, U4716. U4716 is used in FM only. The output of U4716 is a square wave with a frequency equal to the frequency of the 700 kHz IF. U4715, along with U4717, operates as a phase/frequency detector. The output of the integrator, U4717, is a DC voltage which steers the output frequency of the VCO, U4732, in the appropriate direction to make the frequencies equal at pins 1 and 13 of U4715. This phase-locked loop generates a square wave, at pin 4 of U4732, with a frequency equal to the 700 kHz IF input. When over-modulation of the carrier signal occurs, integrator U4717 holds its output at a relatively constant level during the interval when the carrier is suppressed. When the carrier is not suppressed, the phase-lock loop corrects for any drift which may have occurred during the time the carrier was suppressed. U4731B selects between the output of the phase-locked loop for AM demodulation and the output of the comparator, U4716, for FM demodulation.

Time Base Circuit

The Time Base circuit consists of Q4711, U4739, U4724, U4725, U4709, U4711, U4710, U4748B, U4748C, U4760D, U4740 and U4758. This circuit provides the time base frequency for the frequency error counter.

Q4711 buffers the 10 kHz input from the Clock Divider, at pin 18 of P4703, and applies this signal to U4739A and U4709B. U4739A, U4739B, U4724A and U4724B are decade counters which function as divide-by 10 frequency dividers. These dividers produce frequencies at 1 kHz, 100 Hz and 10 Hz. These outputs are applied to CMOS Switches U4725A, U4725C and U4725B, respectively. The four CMOS Switches (U4725B, U4725C, U4725A and U4709B) select one of the time base frequencies of 10 Hz, 100 Hz, 1 kHz and 10 kHz, respectively. The switches are driven by the time base select logic.

The time base select logic consists of U4713, U4710A, U4710B, U4710C, U4711A, U4711B and U4711C. Table 2-2b is a truth table which describes the operation of the time base logic. The time base select logic receives frequency error settings from the I/O PC Board and turns on the appropriate CMOS Switch. In addition, the time base select logic also produces a control line which informs the frequency error counter when to count in the audio mode. This control line is driven by pin 10 of U4710C.

U4760D, U4748B and U4748C drive control lines for the frequency error counter. These control lines are the 1.0 second, 0.1 second and 0.01 second time bases. When all three of these lines are inactive, the 0.001 second time base is selected. The selected time base line is applied to U4740 which, along with U4758A, produces the gate for the frequency error counter.

FREQ ERROR D C B A	U4710C Pin 10	U4711A Pin 8	U4711B Pin 6	U4710B Pin 6	U4710A Pin 8	U4713 Pin 2
0 0 0 0	1	1	0	1	1	0
0 0 0 1	1	1	1	0	1	0
0 0 1 0	1	1	1	1	1	1
0 0 1 1	0	0	1	1	1	0
0 1 0 0	0	0	1	1	0	0
0 1 0 1	0	1	0	1	1	0
0 1 1 0	0	1	0	1	0	0
0 1 1 1	0	1	1	0	1	0
1 0 0 0	0	1	1	0	0	0

Table 2-3a Time Base Logic
(Effective Ser. No. 1426 and on)

Assume that U4758A is reset and that U4740 has just been loaded with $\emptyset\emptyset\emptyset\emptyset_{(2)}$. Under these conditions, the COUNT ENABLE line is high, stopping the frequency error counter from counting. On the next rising, edge of the clock, the counter decrements, reducing the contents of the counter by 1 and yielding a count of $1\emptyset\emptyset1_{(2)}$. When this happens, the output at pin 2 of U4740 goes high, causing U4758 to change states and the COUNT ENABLE line to go low (active state). The COUNT ENABLE line stays low for 10 counts. When the counter underflows from $\emptyset\emptyset\emptyset\emptyset_{(2)}$ to $1\emptyset\emptyset1_{(2)}$, pin 2 of U4740 again makes a low to high transition, causing U4758 to change states and the COUNT ENABLE line to go high (inactive state). When this line goes high, U4740 is set to $\emptyset\emptyset\emptyset\emptyset_{(2)}$ via C4795 and R4883. One count later, the counter again underflows from $\emptyset\emptyset\emptyset\emptyset_{(2)}$ to $1\emptyset\emptyset1_{(2)}$, causing U4758 to change states. The counter, U4740, is then allowed to decrement for ten counts and then the cycle repeats itself. The net result is a pulse which is high for one clock period and low for ten clock periods, and which appears on the COUNT ENABLE line.

Frequency Error Counter Circuit

The Frequency Error Counter Circuit consists of the following IC's:

U4746
U4728
U4763
U4745
U4727
U4765
U4744
U4742
U4741
U4731C
U4764
U4761
U4759
U4775
U4731A
U4709
U4747
U4748
U4766
U4758B

The frequency error counter is a 24 bit binary, presettable up/down counter. Only the lower 8 bits are available at its output. These 8 bits represent the frequency error. When the frequency error counter is in the audio mode, it functions as an up/down counter. At the beginning of each conversion, the frequency error counter is preset to $C\emptyset\emptyset8\emptyset_{(H)}$. During the first gate, the counter counts up using the unknown tone. During the second gate, the counter counts down using the reference tone. If the two tones are equal, the resulting count is $C\emptyset\emptyset8\emptyset_{(H)}$. The lower 8 bits ($8\emptyset_{(H)}$) are latched and applied to the digital to analog converter and to the I/O PC Board. $8\emptyset_{(H)}$ is interpreted as zero. Anything greater than this is interpreted as positive, while anything less is interpreted as negative. If the unknown tone is greater than the reference tone, the result will be positive since the counter counted up more than it counted down. If the unknown tone is less than the reference tone, the result will be negative since the counter counted down more counts than it counted up.

When operating in the RF mode, the counter counts up only. The counter is loaded with a preset value prior to each gate. The gate enables the counting of the 700 kHz IF. If the 700 kHz IF is exactly 700 kHz, the resulting count will be $C\emptyset\emptyset8\emptyset_{(H)}$, which is interpreted as zero. If the 700 kHz IF is less than 700 kHz, the final count will be less than $C\emptyset\emptyset8\emptyset_{(H)}$ and will be interpreted as a negative value. If the 700 kHz IF is greater than 700 kHz, the final count will be greater than $C\emptyset\emptyset8\emptyset_{(H)}$ and will be interpreted as a positive value. In both audio and RF modes, the difference between $8\emptyset_{(H)}$ and the counter's 8 bit output represents the magnitude of the frequency error.

The up/down counter consists of U4743, U4741, U4742, U4745 and U4746. The lower 8 bits of this counter are applied to U4727, which latches the counters' output when the $\overline{\text{COUNT ENABLE}}$ line goes high. The output of U4727 is applied to U4726 and to U4728, a pair of demultiplexers which select between the counter outputs and the OVER/$\overline{\text{UNDER}}$ line.

When an overflow or underflow condition occurs, the upper 12 bits of the counter are applied to the overflow/underflow logic consisting of U4744, U4765B, U4747A, B & C, U4748 A & D and U4766. This logic checks for $C\emptyset\emptyset_{(H)}$ on the upper 12 bits of the counter. If the count is less than $C\emptyset\emptyset_{(H)}$, the logic will indicate an underflow (meter peg = 1; OVER/$\overline{\text{UNDER}}$ = $\emptyset$). If the count is greater than $C\emptyset\emptyset_{(H)}$, an overflow condition is generated (meter peg = $\emptyset$; OVER/$\overline{\text{UNDER}}$ = 1).

The preset logic, consisting of U4709C, U4775A and U4775B, controls the presetting of the counters. When counting RF, the CMOS Switch, U4709C, applies the $\overline{\text{COUNT ENABLE}}$ signal to the astable multivibrators, U4775 A & B. These astable multivibrators produce a delayed pulse to ensure that everything has settled before presetting the counters. The output of U4775B is applied to the reset inputs of the counters and to the reset input of U4758B. U4758B produces the UP/DOWN count signal and the VAR TONE/REF TONE signal. When in the RF mode, this flip-flop is reset everytime the gate goes high, forcing the counters to count up only.

In the audio mode, the output of U4758B is applied to U4775A by U4709C. In this mode, U4758B is reset on every other gate cycle. During the first cycle, U4731A selects the unknown tone and the UP/DOWN line is high. During the second gate cycle, U4731A selects the reference tone. The output of U4731A is applied to the clock input of the counters via U4760A. CR4721 disables the clock while the COUNT ENABLE line is high. U4731C selects between audio (output of U4731A) and RF (output of U4731B in the AM Flywheel circuit) as controlled by the UP ON AUDIO line.

Overtemp Circuit

When the thermistor in the Power Termination Module senses an overtemp condition, its signal is input at pin 24 of P4703. When pin 2 of U4788 reaches a pre-determined level, pin 6 will go high to turn on Q4720. This will turn on the OVERTEMP Indicator Lamp on the front panel and also send a +12 V on Overtemp signal to the I/O PC Board.

Tone Beep Circuit

The $\overline{\text{KEYDOWN}}$ line from the I/O PC Board enters at pin 4 of J4705. When this line is high, Q4707 is on. When this line is low, Q4707 is off to allow the oscillator to function. U4723 and associated components form a 1 kHz Beep Oscillator. R4782 sets the volume level of the Oscillator. The audio-in line at pin 4 of P4702 mixes with the oscillator output and is amplified by U4722, an audio amplifier, for output to the speaker.

2-6-4 Oscilloscope Control and Deflection PC Board Detailed Theory

Control Circuitry

The external input is at J5101 from the front panel SCOPE/SINAD Connector (See Figure 2-16 and the Oscilloscope Control and Deflection PC Board Schematic in Section 7 of this Manual). The setting of the DEV/VERT Control (V/div settings) and the DC/AC Switch determine which of relays K5101 thru K5104 will be energized. If K5101 is energized, a SINAD or DC input will be amplified by U5105A and output to the Demod Audio PC Board at pin 6 of P5103. The selected scope input is amplified by U5101 and sent to multiplexer U5109. External vertical gain is controlled by R5126. Opto-isolator U5112 couples the VERT VERNIER Control into the selected input when the VERT VERNIER Control is not in CAL position. DS 5101 and the front panel UNCAL Indicator Lamp (Vertical) will be illuminated if the VERT VERNIER Control is not in CAL.

The 700 kHz IF signal from the 89-90 MHz Receiver module is input at J5105 and is sent to three multiplexers. Multiplexer U5104C, when control line 9 is low, will route the 700 kHz IF to serve as a control line for multiplexers U5109 and U5110B. The DEV/VERT Control will add the logic level high to the 700 kHz IF in any kHz/DIV position. The logic high will forward bias CR5149 to input the 700 kHz IF through U5104C and out to U5109. The logic high will also serve as a control line for U5108C.

The Demod input at pin 13 of P5102 splits in two directions. One line goes to pin 3 of U5108C and is selected when pin 9 goes high, then sent to the sweep circuit. The other line is sent through a resistor network and U5102B, which is controlled by kHz/DIV positions of the DEV/VERT Control. The selected output of U5102B is amplified by U5103B and switched through U5104C, when pin 9 of U5104C goes high, to U5109.

The TONES position of the HORIZ Control has a control line for U5108A and U5108B. When the +12V on TONES line, input at pin 20 of P5102, is low, U5108B selects pin 2 as an input and channels the sweep circuit information to U5110B. U5108A will select pin 12 as an input when the +12V on TONES line goes low, thus allowing sweep circuit information to be passed to U5109.

The Sweep Control B and A inputs at pins 25 and 23 of P5102 are controlled by the HORIZ Control on the front panel. These lines are the control lines for U5107A in the sweep circuit.

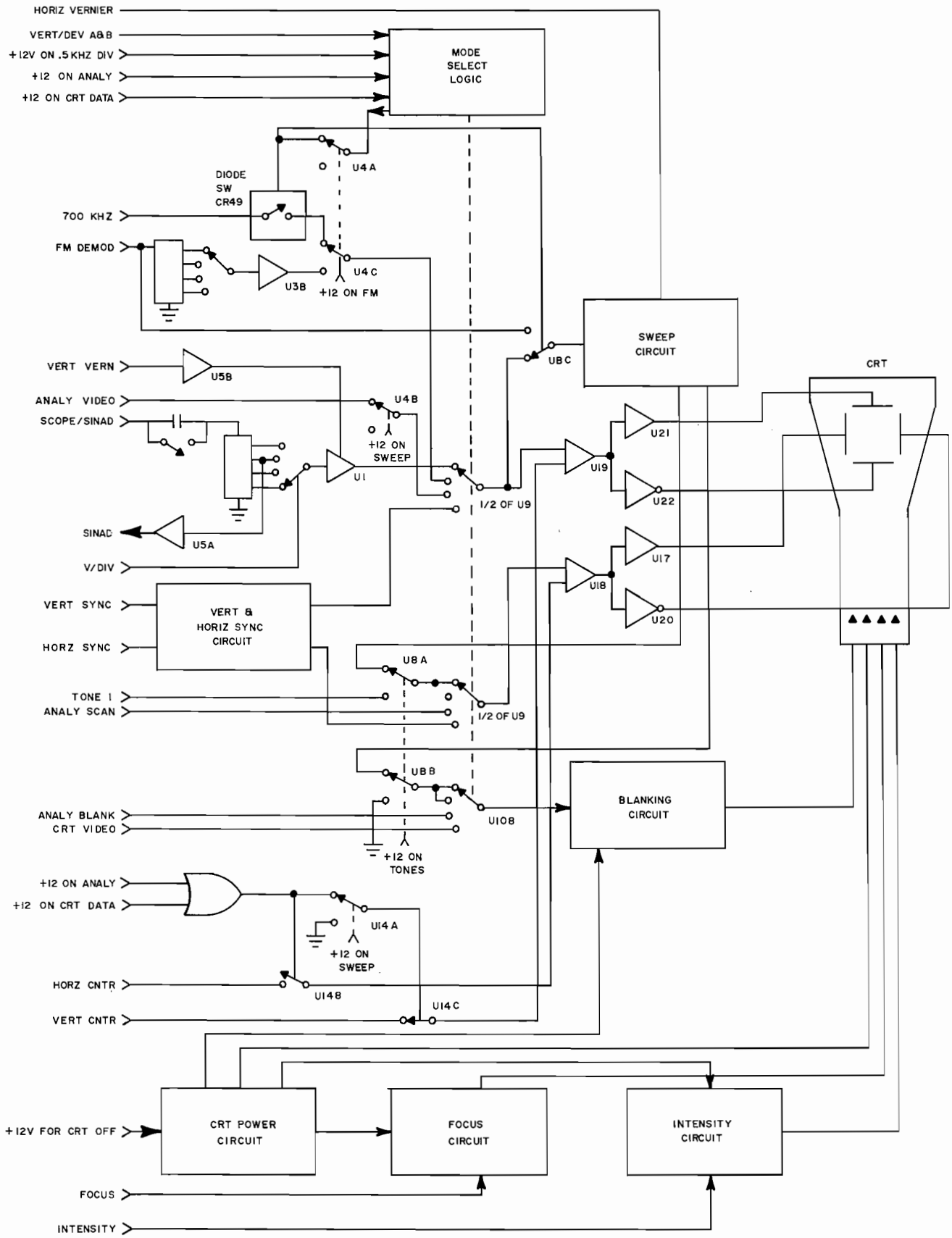


Figure 2-16 Oscilloscope Control and Deflection PC Board Detailed Block Diagram

Mode Select Logic

The Mode Select Logic controls the states of switches U5109, U5110 and U5104C. The Mode Select Logic consists of CR5147, CR5148, CR5115 thru CR5118, Q5113, R5151 and R5152. This logic selects the appropriate operating mode of the CRT, based upon the states of the Vert/Dev A, Vert/Dev B, +12 V on Analyzer, +12 V on CRT Data and +12 V on .5 kHz/DIV lines.

Sweep Circuit

Q5108 and Q5110 act as the control flip-flop for the sweep circuit. Q5107 and Q5111 are turned on and off by the flip-flop, and, in turn, discharge the selected capacitor on the input lines of U5107. U5107A selects the proper capacitor for the sweep rate selected by the setting of the front panel HORIZ Control (Sweep Control A and B lines) and by the sweep width adjustment, R5119. U5107B selects the proper capacitor for wait time as selected by the setting of the front panel HORIZ Control and by the Sweep Rate Adjustment, R5116. In "normal" operation, the sweep circuit is a free-running oscillator. When a sync signal is selected at pin 5 of U5108C, U5111 acts as the trigger for the oscillator. In this condition, Q5103 and Q5109 keep retriggering from occurring until the proper voltage is built up on the base of Q5103.

If the front panel HORIZ VERNIER Control is not in CAL position, the UNCAL Indicator Lamp (Horizontal) on the front panel will be illuminated thru U5106A. The HORIZ VERNIER Control must be in CAL for a calibrated signal.

When Q5108 of the flip-flop is low, a blanking signal is sent through CR5123 to U5108B, pin 2.

Blanking Circuit

When Q5137 turns on, Q5138 will turn on. This pulls down the collector voltage of Q5136 to about +50 V. Zeners CR5134 and CR5135 each provide 20 V of this drop. When Q5137 turns off, C5166 charges up, pulling the collector of Q5136 back up to about +100 V.

CRT Power Circuit

Q5131 thru Q5134, and associated components, form the CRT Power Circuit. Q5134 and Q5135, along with T5101, form an inverter circuit. To start the inverter circuit, a pulse is applied to the center tap of the base winding of T5101. This pulse turns on Q5134 and Q5135. When the pulse is removed, the return for the center tap is provided by Q5133, starting the oscillator circuit into oscillation. The output of the inverter is produced in the three secondary windings of T5101. The 2-turn winding provides filament voltage for the CRT, V6401. This winding is connected to the cathode to prevent internal arcing between the cathode and filaments of the CRT. The 80-turn winding passes thru a full-wave rectifier consisting of CR5141 thru CR5144. The output of this full-wave rectifier is approximately +200 VDC, which is used to supply the deflection amplifiers and the tube bias circuits. The 376-turn winding of T5701 is applied to a voltage doubler, which produces approximately -2100 VDC to the Intensity, Focus and Blanking Circuits.

The on/off control of the inverter is determined by the state of pin 22 of P5103. When this line is at +12 V, Q5132 is on, turning off Q5131. Q5133 is turned off, removing the return path for the currents which drive Q5135 and Q5134. As a result, the inverter shuts off. When pin 22 of P5103 goes low, Q5133 is turned on and Q5132 is turned off. When Q5132 turns off, Q5131 conducts and C5155 charges. When C5155 is fully charged, Q5131 will shut off. The output of Q5131 is the start pulse for the inverter.

Intensity Circuit

The front panel INTENSITY Control line is input at pin 21 of P5103. R51153 is provided to set line voltage. Op-amp U5126 is coupled into the circuit through opto-isolator U5128 which stabilizes any linearity and current drift. When +12 V is applied to pin 3 of U5126 through CR5146 from the CRT Data line, more brightness is added for raster scan. Opto-isolator U5116 turns on to turn Q5130 off. This allows a maximum voltage of +120 V to be applied to the CRT. CR5133, a +120 V Zener, sets this voltage.

Focus Circuit

The Focus Circuit operates in much the same fashion as the Intensity Circuit. The front panel FOCUS Control line is input at pin 23 of P5103. R5182 sets line voltage. Op-amp U5125 is coupled through opto-isolators U5127 and U5115 to turn Q5129 on or off.

Vertical Deflection Circuit

If the +12 V on Sweep line (pin 11 of U5114A) is low, U5114C selects pin 5 as the input line. The VERT POS Control on the front panel is then summed into Op-amp U5119 with the Vertical input line. R9561 is the Vert Centering Adjustment, and R5188 is the Vert Gain Adjustment. The output of U5119 feeds U5121 for the non-inverted deflection plate control line. U5122 inverts the output of U5119 for the inverted deflection plate control line. When relays K5105 and K5106 are energized by the +12 V on the CRT Data line, the circuit is slowed down for raster control.

Horizontal Deflection Circuit

The Horizontal Deflection Circuit operates similarly to the Vertical Deflection Circuit, but about twice as fast. When all three control lines at pin 10 of U5114B (+12 V on Analyzer, +12 V on CRT Data or +12 V on Sweep) are low, pin 2 is selected as the input line. The front panel HORIZ POS Control is summed in U5118 with the Horizontal input line. U5117 is the non-inverting control, while U5120 is the inverting control. Q5122 and Q5123 are constant-current transistors used in conjunction with R9528 to set astigmatism control.

Vertical and Horizontal Drive Circuit

The VERT SYNC and HORIZ SYNC inputs at pins 26 and 24 of P5102 are driven by the CPU/MEMORY PC Board to control menu displays on the CRT. Q5115 and Q5139 are current limiters which shape the vertical and horizontal pulses. U5103A inverts the VERT SYNC pulse. Both pulses are applied to U5109 and are selected when the +12 V on CRT DATA control line is high.

2-7 GENERATOR FUNCTIONAL THEORY

In "normal" operation (when the DISPLAY Control is in any position other than "SWEEP" or "TRACK"), the IF source for the Generator Functional Block is the 79.3 - 78.3001 MHz signal input into the FM Generator Module from the Low Loop section of the Frequency Synthesis Functional Block(See Figure 2-17). When the DISPLAY Control is in "TRACK" or "SWEEP", the IF source is the 84.3 - 73.3 MHz signal from the Spectrum Analyzer Functional Block. The IF source is mixed with a 10.7 MHz VCO signal and is output to the Generator Mixer Module as an approximate 68.6 MHz signal. The 10.7 MHz VCO signal contains FM information from the Dual Tone Generator PC Board and is either phase-locked with a 1 kHz reference signal or is controlled by the GEN/LOCK Control on the front panel. The GEN/LOCK Control allows the output frequency to be varied + or -10 kHz. A 158.6 MHz signal from the Generator Mixer Module is used as the source for the phase-locking of the 10.7 MHz VCO signal.

The Generator Mixer Module filters and converts the approximate 68.6 MHz IF and outputs it as a 90 MHz signal to the 1300 MHz IF Generator Module. The 90 MHz IF is converted three times in the 1300 MHz IF Generator Module: first, to 1120 MHz, by mixing with a 1210 MHz High Loop signal; second, to 1250 to 1350 MHz by mixing with a 130 to 230 MHz Duplex Offset signal; and third, to a 0 - 1000 MHz output signal by mixing with a 1300 to 2299 MHz High Loop Signal.

The 0 - 1000 MHz output signal is input to the Output Amp module, which boosts the output level to the Variable Attenuator, controls the Duplex Offset Module RF level (AM), and (when in Generate Simplex mode) outputs a crossfeed signal to the Receiver Functional Block.

From the Variable Attenuator, the output signal is channeled to the Power Termination Module. In the Generate Simplex mode of operation, the RF signal will be output to the TRANS/-40 dB DUPLEX Connector. In the Generate Duplex mode of operation, the RF signal will be output to the DUPLEX OUTPUT Connector and, at 40 dB down, to the TRANS/-40 dB DUPLEX Connector.

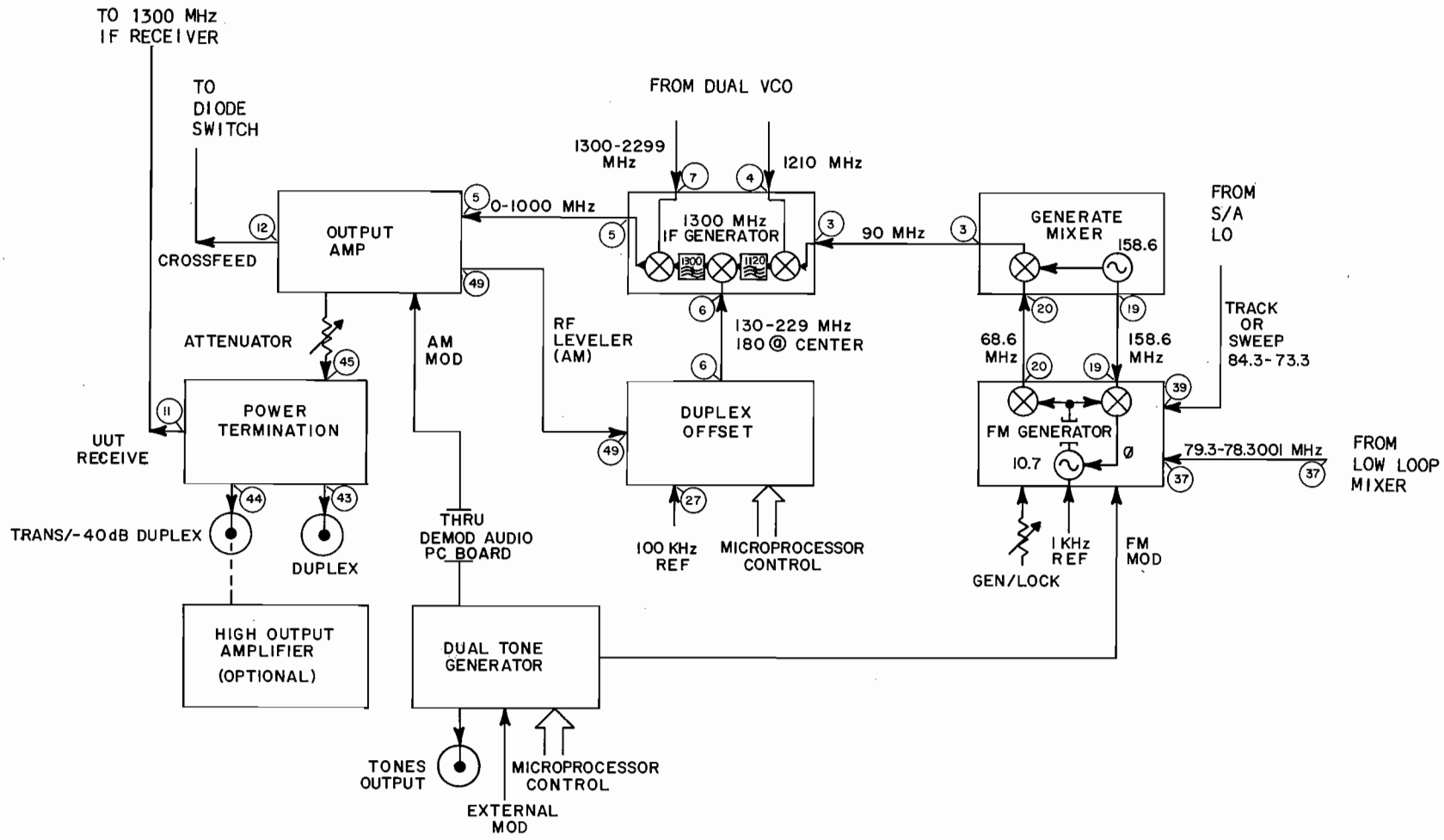


Figure 2-17 Generator Functional Block Diagram

2-7-1 FM Generator Module Detailed Theory

U3301A acts as a switch to select the input line as either 79.3-78.3001 MHz from the Low Loop Mixer Module or as 84.3-73.3 MHz from the Spectrum Analyzer LO Module (See Figure 2-18 and the FM Generator Schematic in Section 7 of this Manual). When +12 V is applied to pin 3 of U3301A, the Spectrum Analyzer LO input is selected. If +12 V is not present at pin 3 of U3301A, the Low Loop Mixer input is selected. The +12 V is active when the front panel DISPLAY Control is set to "SWEEP" or "TRACK".

The selected input signal is amplified by Q3301 and mixed in MXR3301 with a 10.7 MHz VCO signal. The difference frequency of approximately 68.6 MHz is amplified in Q3302 and output at J4206.

The 10.7 MHz VCO signal is also mixed, at MXR3302, with the 158.6 MHz signal input at J4205 from the Generator Mixer Module. The sum frequency of 169.3 MHz is filtered and amplified for driving the frequency divider chain U3305, U3306 and U3304. U3305 and U3306 are ÷10 frequency dividers and U3304 is a ÷1693 frequency divider. The resultant 1 kHz is applied to pin 3 of U3303 to phase-lock the 10.7 MHz VCO with a 1 kHz reference signal.

Transistor Q3308 and associated components form a 10.7 MHz voltage controlled oscillator (VCO). The adjustment of C3367 is used to set a tune voltage of approximately 3 volts at pin 15 of U3302B. Q3308 is operating properly when there is a negative 2 to 4 volts on its gate (pin 3).

Zener diode CR3311 subregulates the +12 volt supply voltage to +6.9 volts to operate Q3308, Q3303 and IC U3303.

IC U3302B acts as a switch control of the 10.7 MHz VCO between the phase-lock loop and the GEN/LOCK Control on the front panel. When the GEN/LOCK Control is switched out of detent, +12 V is applied to pin 10 of U3302B, causing control of the VCO to be assumed by the GEN/LOCK Control. This allows the output frequency to be manually varied +10 kHz and -10 kHz.

FM modulation, controlled by the Dual Tone Generator, is input at pin 9 of J4203. The FM modulation voltage is set by R3333 and applied to the VCO frequency through varactors CR3309 and CR3310.

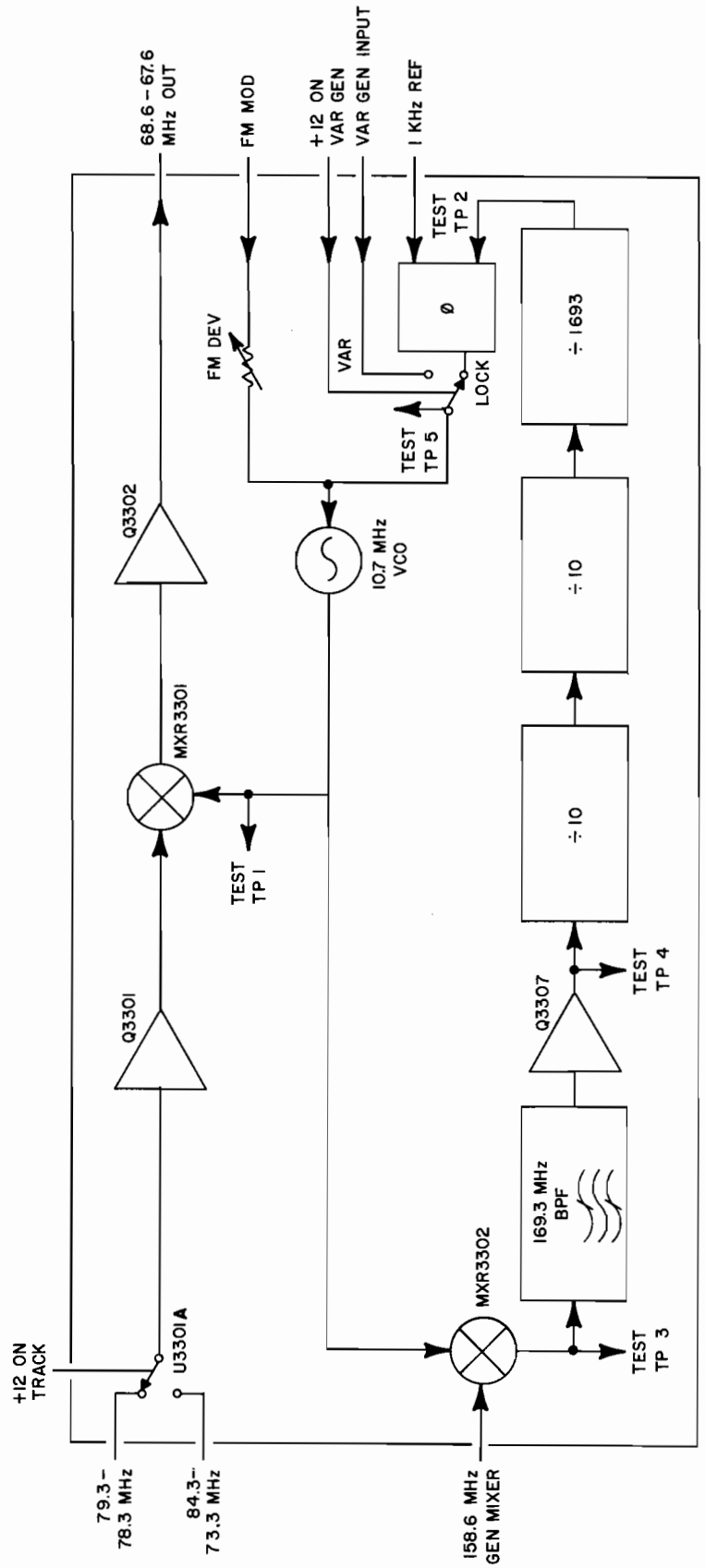


Figure 2-18 FM Generator Detailed Block Diagram

2-7-2 Generator Mixer Module Detailed Theory

A 68.6 MHz signal from the FM Generator Module is input at J4401, attenuated by the network of R3401, R3402 and R3403, and filtered before being applied to MXR3401. (See Figure 2-19 and the Generator Mixer Schematic in Section 7 of this Manual).

A 158.6 MHz crystal oscillator frequency, formed by Y3401 and associated components, is output at J4402 to the FM Generator Module and also applied to MXR3401. In MXR3401, the 158.6 MHz is mixed with the 68.6 MHz and the result is a 90 MHz signal that moves in the opposite direction of the 2nd I.F. Receive Frequency. The 90 MHz signal is band-pass filtered and output at J4403 to the 1300 MHz I.F. Generator Module. The DC control voltage for the 90 MHz filters is controlled by U3401, which acts as a switch. In "normal" operation, the DC control voltage is set by variable resistors R3412 and R3423. If the front panel DISPLAY Control is in "SWEEP" or "TRACK", +12 V switches U3401 to the control line at pin 7 of J4404, and the DC control voltage is set by U3402 and U3403, through their variable resistors.

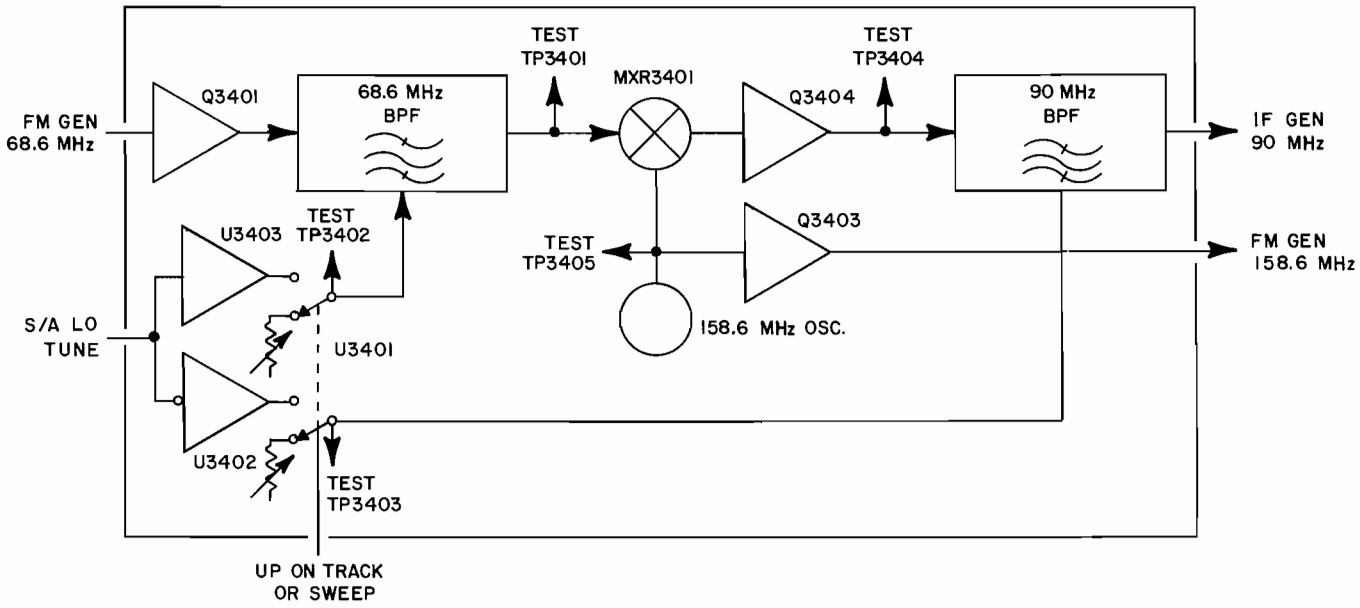


Figure 2-19 Generator Mixer Detailed Block Diagram

2-7-3 1300 MHz IF Generator Module Detailed Theory

The 90 MHz signal from the Generator Mixer Module enters at J1202 and is mixed in MXR1201 with a 1210 MHz signal, input at J1201, from the High Loop section of the Frequency Synthesis Functional Block (See Figure 2-20 and the 1300IF Generator Module Schematic in Section 7 of this Manual). The difference frequency of 1120 MHz is band-pass filtered in Z1201 and amplified in three stages consisting of Q1601, Q1602 and Q1603 and their associated components. The 1120 MHz signal is mixed in MXR1202 with the input, at J1203, from the Duplex Offset Module, which is normally 180 MHz. The input from the Duplex Offset Module may be 180 MHz + or -49.99 MHz if an offset frequency is desired.

The sum of the signals from MXR1202 is 1300 MHz (±49.99 MHz). The sum signal is band-pass filtered by Z1202, which must pass a 1250-1350 MHz offset signal. The filtered 1300 MHz signal is amplified by Q1501 and Q1502 and mixed in MXR1203 with a 1300-2300 MHz signal from the High Loop section of the Frequency Synthesis Block.

The 0-1000 MHz signal output of MXR1203 is filtered by a 1000 MHz low-pass filter, FL1203, and output at J1205 to the Output Amplifier Module.

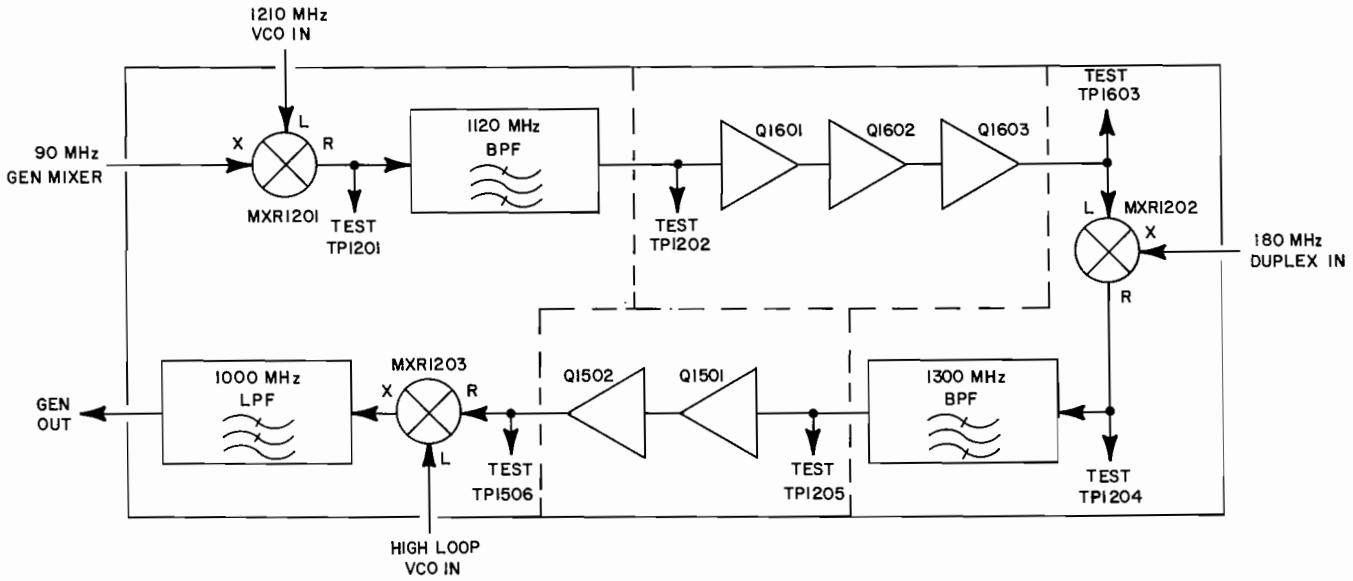


Figure 2-20 1300 MHz IF Generator Detailed Block Diagram

2-7-4 Duplex Offset Module Detailed Theory

The Duplex Offset Module generates an 130-229.99 MHz synthesized RF signal that is mixed in the 1300 MHz I.F. Generator Module to produce a 0 to ±49.99 MHz offset frequency.

The RF signal is generated in one of two VCO's. Transistors Q2701 and Q2702, and associated components, form a 130-179.99 MHz VCO when Q2704 is off. Transistor Q2703, and associated components, forms a 180-229.99 MHz VCO when Q2705 is off. The selected VCO signal is buffered by Q2706 before being sent to the output circuit and to the programmable divider circuit.

Programmable Divider Circuit

Q2713 amplifies the selected VCO signal to drive the programmable divider circuit. U2701 and U2702 together operate as a ÷100/÷101 swallow counter. U2701 by itself is a ÷10/÷11 prescaler. When U2703 and U2704 count down to 00, both pin 12's will go high, changing U2701 to a ÷10 and disabling U2703 from counting until the next load condition.

When U2706 and U2707 have reached count 000, U2705 will count down to 002. At count 002, the look-ahead circuit of U2713, U2714 and U2709A will set pin 14 of U2709A high. At count 001 on U2705, the clock pulse at pin 1 of U2709A will set the $\overline{Q}$ output at pin 13 low, pulling down the load lines of the counters (pin 11), allowing the counters to load the frequency select data. The Q output of U2709A (pin 12) goes high, causing U2701 to remain as a ÷10. At count 000 on U2705, U2709A will be reset to await a new load condition.

Phase/Frequency Detect Circuit

A 100 kHz reference frequency is input at J3203 from the Clock Divider Module. The 100 kHz is divided by 10 in U2708 to produce a 10 kHz reference signal at pin 12, which is compared with the 10 kHz clock of the programmable divider circuit. Pin 8 of U2708 is a ÷2, or 50 kHz output. U2709B is the slip flip-flop for the circuit. If the Q output at pin 9 of U2709B goes high, the logic gates of U2714A, U2711A and U2711B will shut off the 100 kHz reference signal at pin 1 of U2708. If the $\overline{Q}$ output of pin 8 of U2709B and the Q output at pin 12 of U2709A are not high at the same time, pin 8 of U2711C will go high, making pin 11 of U2711D go high. This condition causes Q2709 to turn on and, through the Demod Audio PC Board, turn off the Freq LOCK Indicator Lamp on the front panel.

The Q output at pin 12 of U2709A acts as the clear input at pin 6 of U2709B. When the Q output at pin 9 of U2709B and the 10 kHz reference line at pin 12 of U2708 are both high, the phase lock sample is taken. The 10 kHz reference pulse out of Q2711 forms a ramp from the leading edge of the square wave. The 10 kHz divider forms the sample pulse time at C2737 that gates the first sampler of U2715C. A second sample

pulse time is formed at C2742 that gates a second sampler at U2715A. The DC voltage from the sampler is integrated at Q2715 and Q2716 to control the tune voltage and slew the VCO frequency.

Output Circuit

The RF signal to the output circuit is amplified by Q2710 and Q2708 to drive the low-pass filter and the modulator. When the 130-179.99 MHz VCO range is selected, Q2718 is turned on to add more inductance into the low-pass filter. The RF signal out of the low-pass filter is passed through CR2705 and CR2704, which together act as a diode switch to add amplitude modulation (RF Leveler) from the Output Amp Module. The 130-230 MHz output at J3201 is sent to the 1300 MHz IF Generator Module.

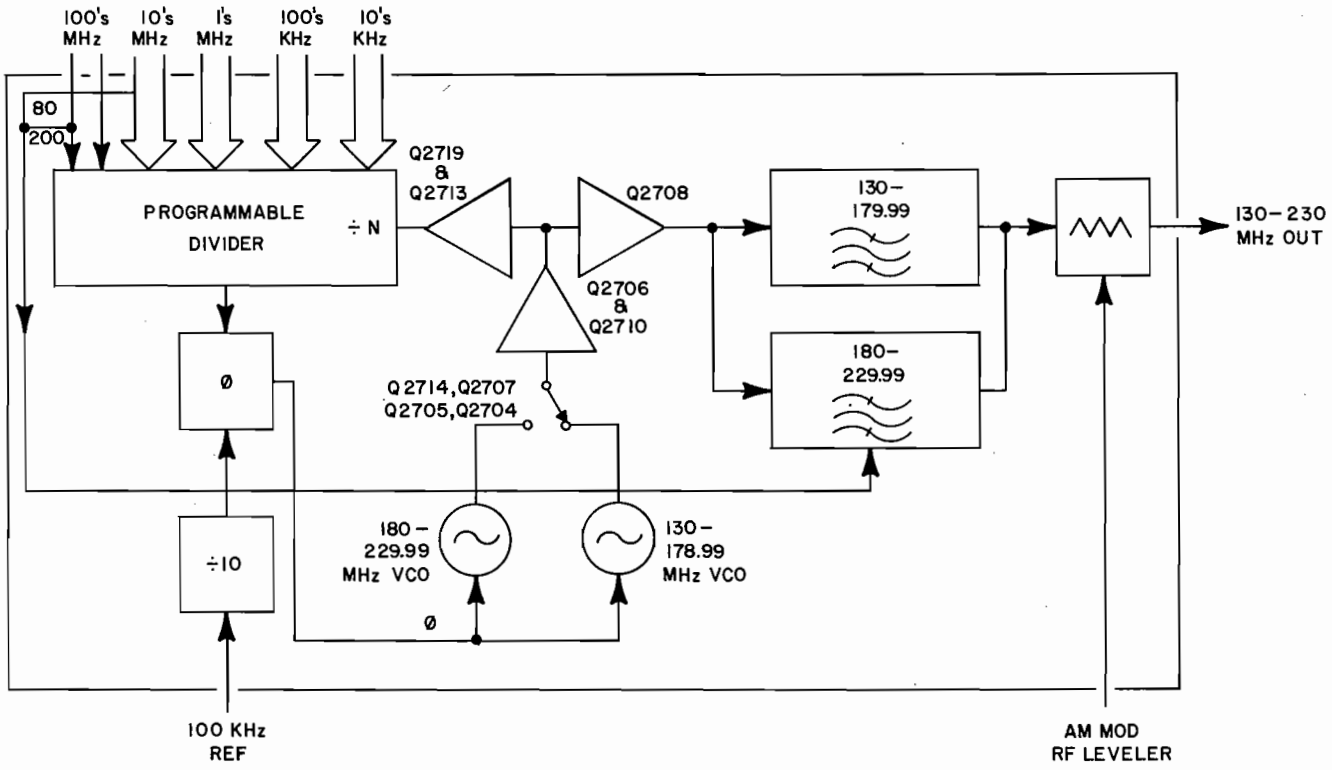


Figure 2-21 Duplex Offset Detailed Block Diagram

2-7-5 Output Amplifier Module Detailed Theory

The Output Amplifier Module receives the 0-1000 MHz signal from the 1300 MHz IF Generator Module at J801 (See Figure 2-22 and the Output Amplifier Schematic in Section 7 of this Manual). U901 amplifies the signal to drive three discrete stages consisting of Q901, Q903 and Q905. The output signal at J803 is +38 dBm above the input signal.

The output level is detected by CR906, CR907 and U902B. AM modulation (from the Demod Audio PC Board, as generated by the Dual Tone Generator PC Board) is added at pin 2 of U902A. The output at J802 is sent to the Duplex Offset Module for RF Leveler control.

In the Generate Simplex mode of operation, the +12 V applied at pin 3 of P805 reverse-biases CR903, CR904 and CR905 to output a -10 dBm crossfeed signal at J804 to the 1300 MHz IF Receiver Module.

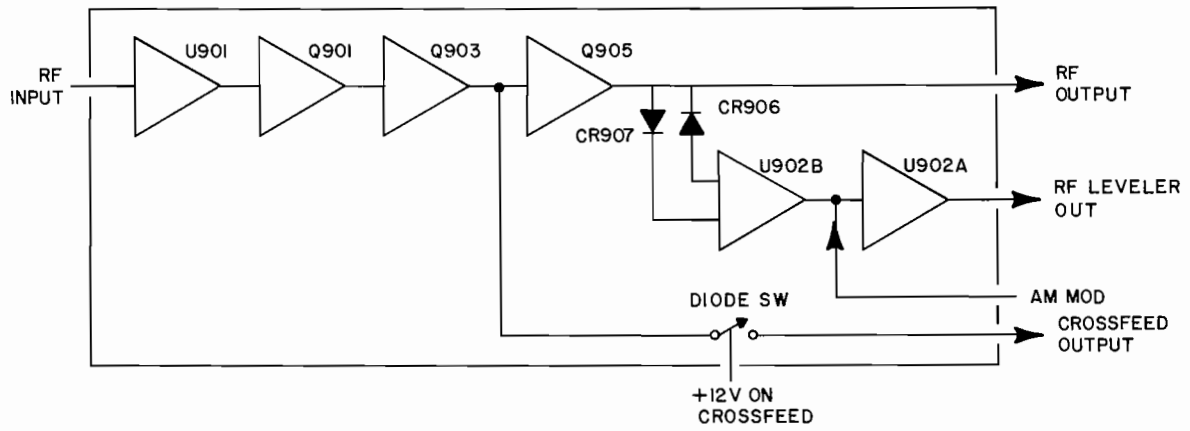


Figure 2-22 Output Amplifier Detailed Block Diagram

2-7-6 Power Termination Module Detailed Theory

The generator RF output signal from the Variable Attenuator is input at J9801(See Figure 2-23 and the Power Termination Schematic in Section 7 of this Manual). In the Generator Simplex mode of operation, the RF signal passes through energized K9801 and K9802 and out J9802 to the TRANS/-40 dB DUPLEX Connector. In the Generator Duplex mode of operation, K9801 and K9802 de-energize to allow the RF signal to be output at J9803 to the DUPLEX OUTPUT Connector. In this mode, the signal that passes through R9804, R9805, R9806 and AT9801 and out J9802 is 40 dB below the actual setting of the Variable Attenuator on the Front Panel.

NOTE

The control logic circuitry for control of the Power Termination relays is on the Demod Audio PC Board.

When the UUT (Unit Under Test) transmits into the TRANS/-40 dB DUPLEX Connector with a power level of 100 mW or greater, the power level is detected by CR9801. K9801 will be de-energized. When this happens, a UUT Receive signal is output at J9804 to the 1300 MHz IF Receiver through the Diode Switch. Diode CR9802 measures the RF power level and sends it to the metering circuitry.

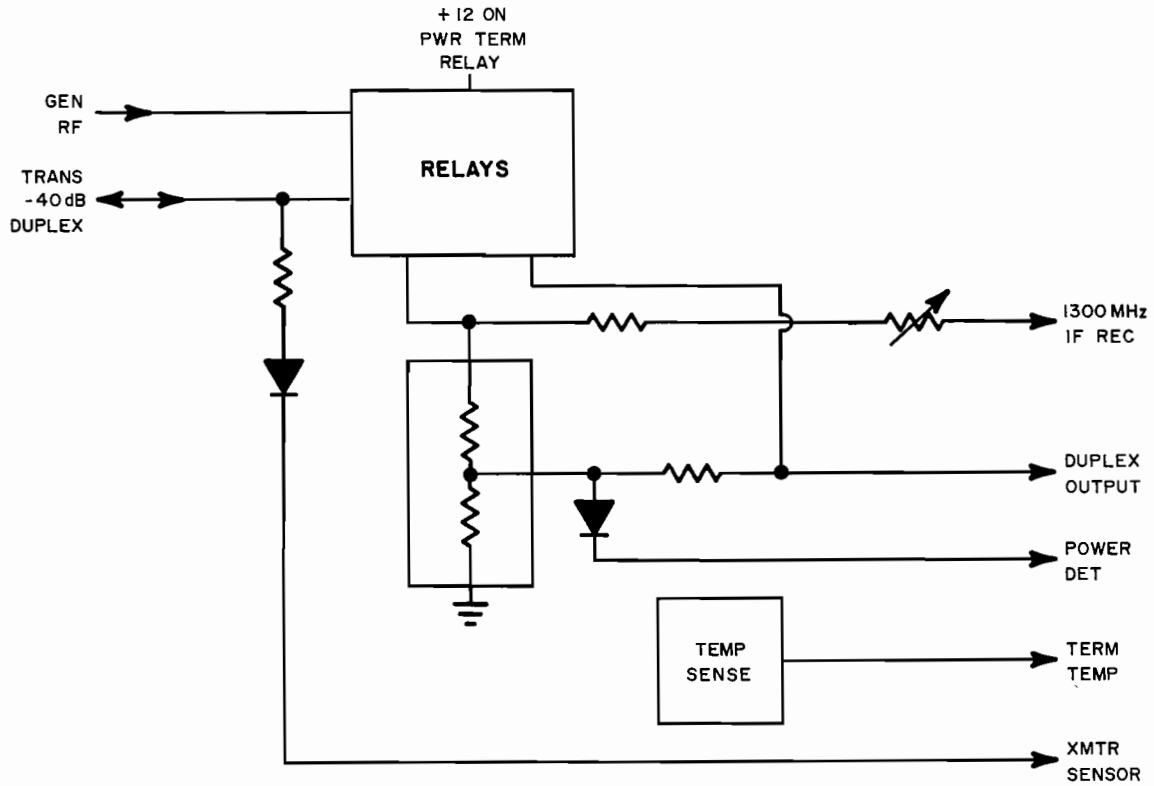


Figure 2-23 Power Termination Detailed Block Diagram

2-7-7 Dual Tone Generator PC Board Detailed Theory

The Dual Tone Generator PC Board can generate two separate synthesized tones, programmable from 2 Hz to 30 kHz. (See Figure 2-24 and the Dual Tone Generator PC Board Schematic in Section 7 of this Manual.)

Crystal Oscillator Circuit

Both tones are referenced to a 3.35544 MHz crystal oscillator frequency, formed by Y4501, Q4501 and associated components. C4505 is provided for oscillator frequency adjustment. The oscillator frequency is divided by two at U4525B, to clock both adder circuits at a rate of 1.67772 MHz. The oscillator also clocks U4529 and U4547 through Q4503, which sets a TTL level.

Address Select Circuit

The data bus inputs are buffered by U4501 and U4513A, and then sent to the latches. The address bus and write (BWR) inputs are decoded and demultiplexed by U4511 and U4512, then buffered by U4513B and U4554A. U4514, the tone control chip, controls the switch states for the control circuitry and the wave shapes of the ROMs.

Latches

U4502A, U4503 and U4504 are the Tone 2 latches. U4502B, U4505 and U4506 are the Tone 1 latches. The latches for both tones latch the information from the address select circuit to the adders. Information from the Tone 1 latches is also sent to the Tone Multiplier Circuit through logic gates to serve as control lines.

Adders

U4518, U4519, U4521, U4522 and U4524 are the Adders for Tone 2. U4536, U4537, R4539, R4540 and U4542 are the Adders for Tone 1. The inputs to the Adders are also used to control the low-pass filter control switches in the Low-Pass Filter Circuit. The Adders are latched together at a 1.67772 MHz rate. The up-counters U4525A and U4543B, are enabled by the carry-out of the last Adder. U4527 and U4545 are buffers. Q4504 and Q4505 are turned on when the up-counters reach end of count.

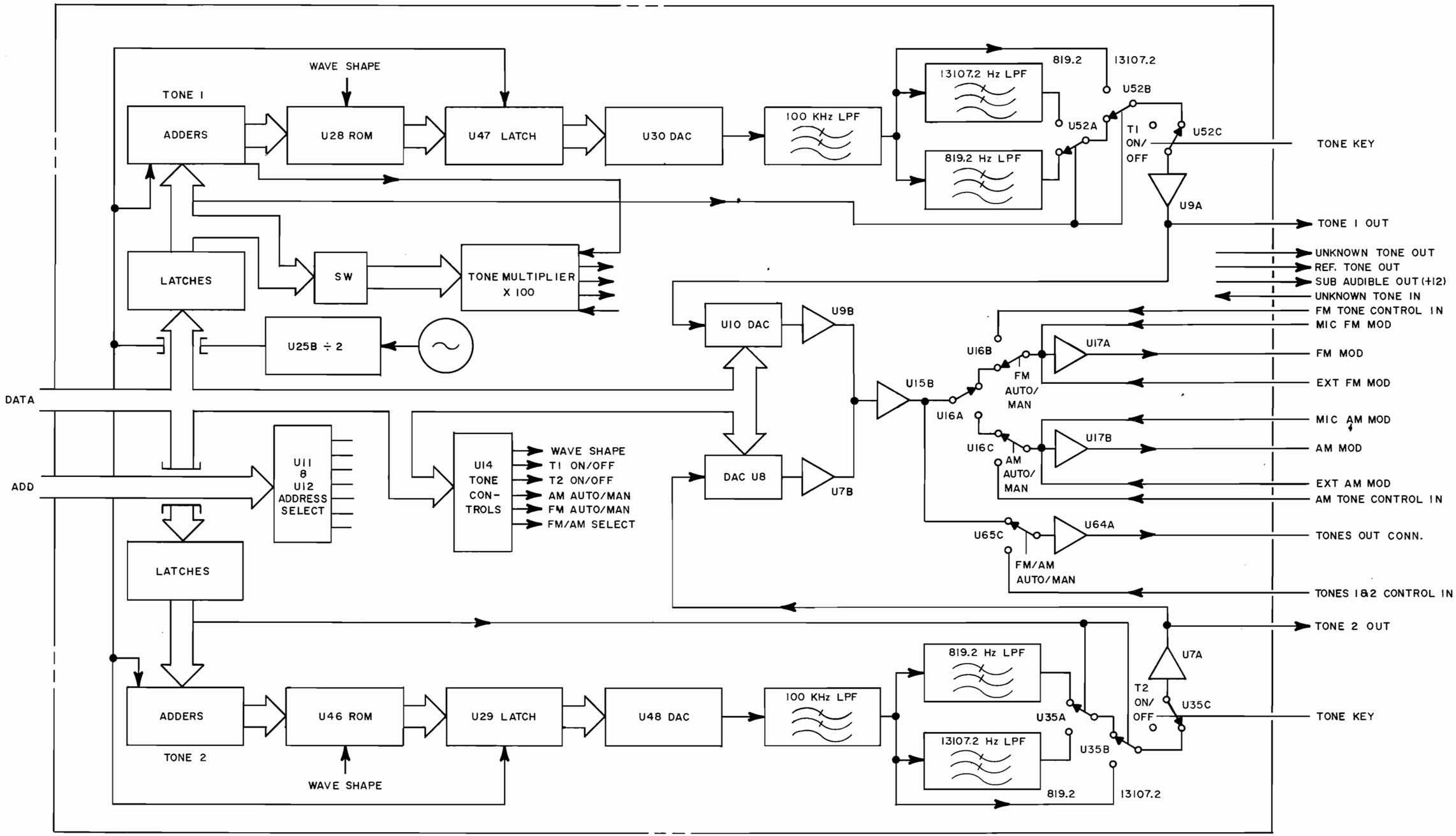


Figure 2-24 Dual Tone Generator PC Board Detailed Block Diagram

Low-Pass Filter Circuit

The sine signal is low-pass filtered to smooth the wave form. If the selected tone is 13,107.2 Hz or greater, only the first LPF section is switched in by U4535B and U4552B. If the selected tone is 819.2 Hz to 13,107.1 Hz, U4535A and U4552A select pin 2 as their input lines for a second LPF. If the selected line is less than 819.2 Hz, a third LPF is switched in place of the second LPF at pin 13 of U4535A and U4552A.

Control Circuitry

After the tone filtering, U4535C and U4552C are used to select whether the tones will be on or off. If their control lines are not active low, the tones will be routed to Op-Amps U4507A and U4509A.

The output of U4507A is routed to the V_{REF} input of DAC U4508 and to the Tone 1 output line at pin 26 of P4502. The output of U4509A is routed to the V_{REF} input of DAC U4510 and to the Tone 2 output line at pin 24 of P4502. The tones output lines are routed through the front panel controls for manual operation, and then passed back to the Dual Tone Generator PC Board for switching. The tones lines to the DAC, (U4508 and U4510) are used to convert digital bus information to analog information, which is then passed to the switches.

Switch U4565C selects automatic or manual tones routing to the Tones Output Connector on the front panel, through Op-Amp U4564A. Switch U4516A routes the tones to the AM or FM modulator. Switches U4516B and U4516C select the AM and FM modulation source between front panel control and internal bus control. Also, any external modulation or microphone audio is summed into the AM or FM modulation signal at U4517A and U4517B.

Tone Multiplier Circuit

The Tone 1 Adder Circuit provides the reference frequency for the Tone Multiplier Circuit at pin 14 of U4559. U4558 decodes its inputs at pins 9 and 10 to select the necessary capacitance for U4559 and U4560. U4559 and U4560 are phase lock loop (PLL) chips, which, together with up-counters U4561 and U4562, multiply the reference tone and the unknown tone by 100 for output to the Demod Audio PC Board.

U4563 outputs a +12 V signal to the Demod Audio PC Board if none of its inputs, from the Tone 1 latches, are high. U4555A and U4557 decode the latch lines for control inputs to U4558.

2-7-8 High Output Amplifier Module Detailed Theory

General

The High Output Amplifier is an optional amplifier device that connects to the TRANS/-40 dB DUPLEX Connector and the EXT AMP Connector on the front panel of the FM/AM-1500 (See the High Loop Amplifier Schematic in Section 7 of this Manual). The device boosts the gain of the generated output signal by +20 dB. In the Generate Mode, +12 VDC applied at P411 energizes relay K7201. The output signal is then coupled through the output connector (J7303), which may be connected directly to a UUT or to an antenna. In the Receive mode, the +12 VDC input goes low and opens the relay. The output connector of the High Output Amplifier is then connected to its antenna connector, J7304. A coax cable may then be connected between the antenna connector and the FM/AM-1500 front panel ANTENNA Connector.

CAUTION

NEVER TRANSMIT, THROUGH DIRECT CABLE CONNECTION, INTO THE OUTPUT OR ANTENNA CONNECTORS OF THE HIGH OUTPUT AMPLIFIER. TO DO SO WILL DAMAGE EITHER THE HIGH OUTPUT AMPLIFIER, THE FM/AM-1500, OR BOTH.

Circuit Description

The generate signal out of the FM/AM-1500 TRANS/-40 dB DUPLEX Connector is input at P402. Q7201 and Q7203 are signal amplifiers which are turned on by +12 VDC applied at P411. Q7202 and associated components act as a constant current source for Q7203, in order to maintain a constant amplification level. Inductors L7201 and L7202 inhibit stray RF from entering the FM/AM-1500 +12 VDC power distribution circuit. Relay K7201 performs the signal switching function.

2-8 SPECTRUM ANALYZER FUNCTIONAL THEORY

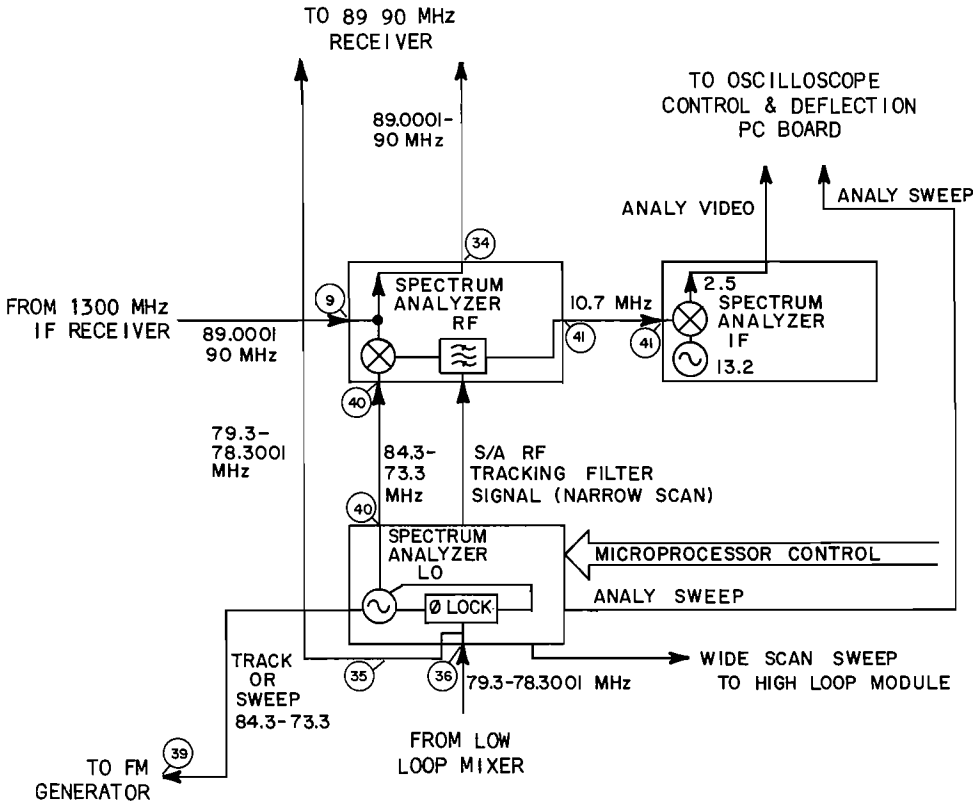


Figure 2-25 Spectrum Analyzer Functional Block Diagram

The Spectrum Analyzer Functional Block contains the Spectrum Analyzer RF, Spectrum Analyzer LO and Spectrum Analyzer IF Modules (See Figure 2-25). The Spectrum Analyzer LO Module is the key module in this Functional Block. It takes the Low Loop Mixer 78.3001 to 79.3 MHz frequency, phase-locks it and converts it to a 73.3001 to 84.3 MHz signal. This signal supplies the Spectrum Analyzer RF Module with its sweep signal. The signal will also take control of the Generator Functional Block in the tracking mode of operation. The LO Module also controls the switching of the tune lines in the High Loop Module and controls the switching of the tracking filter and the band-pass filters in the Spectrum Analyzer RF Module.

The Spectrum Analyzer RF Module mixes the second IF frequency (nominally 90 MHz) from the 1300 MHz IF Receiver and mixes it with the Spectrum Analyzer LO signal to form a 10.7 MHz signal to the Spectrum Analyzer IF Module. The IF Module converts its input, by mixing and down-converting, to a linear signal to drive the CRT, through the Oscilloscope Control and Deflection PC Board.

2-8-1 Spectrum Analyzer IF Module Detailed Theory

The Spectrum Analyzer IF Module converts the 10.7 MHz IF input signal to 2.5 MHz and outputs a detected linear video signal for the logarithmic RF level of the CRT (See Figure 2-26 and the Spectrum Analyzer IF Schematic in Section 7 of this Manual).

Y3901, Q3901 and associated components form a 13.2 MHz crystal oscillator. The oscillator frequency and the 10.7 MHz signal input at J5401 are mixed in MXR3901 to form a 2.5 MHz difference frequency. The 2.5 MHz signal divides for one of two selected filters. When the +12 V filter control line (pin 5 of J5402) is high, the 650 kHz bandwidth filter is selected. When the filter control line is low, an eight-pole filter of 30 kHz bandwidth is selected. The gain of the 650 kHz filter is set at R3919. The gain of the 30 kHz filter is set at R3938.

The filtered 2.5 MHz signal is amplified by U3901 and discrete amplifiers Q3909, Q3910, Q3912 and Q3913. The logarithmic signal is converted to a linear signal, which is detected by CR3909 and then amplified by U3902B for output to the Oscilloscope Control and Deflection PC Board. If pin 10 of U3903A goes high (when the 1 dB position is selected on the front panel dB/DIV Switch), U3902A is switched through U3903A. The VERT POS Control on the front panel will then control the gain of U3902A by its input at pin 8 of J5402.

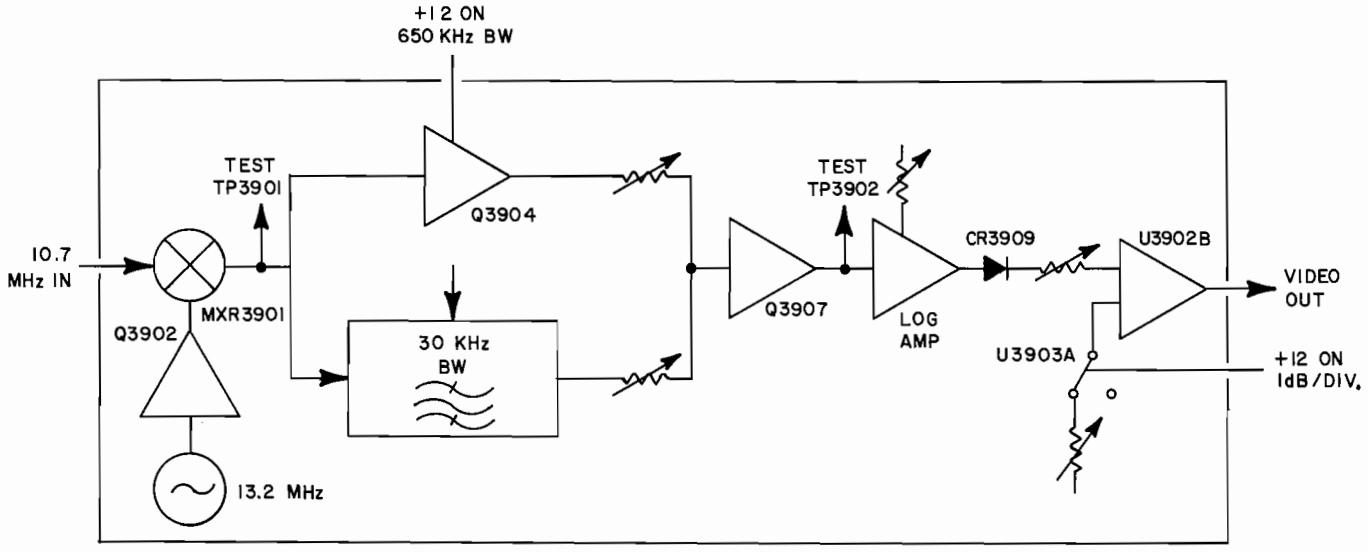


Figure 2-26 Spectrum Analyzer IF Detailed Block Diagram

2-8-2 Spectrum Analyzer LO Module Detailed Theory

NOTE

FM/AM-1500 serial numbers 1005 through 1351 use PC Board 7010-5033-500 (Revision B) and Schematic 7010-5013-500 (Revision B). FM/AM-1500 serial numbers 1352 and ON use PC Board 7010-5033-500 (Revision F) and Schematic 7010-5013-500 (Revision F). Many of the part numbers referred to in theory will be the same in both the B and the F versions. For those part numbers that are different, the first number given is the F version and the second part number (in parentheses) is the B version.

The Spectrum Analyzer LO Module supplies the Spectrum Analyzer RF Module with its tracking frequency while being phase-locked with the Low Loop Mixer Module frequency (See Figure 2-27 and the Spectrum Analyzer LO Schematic in Section 7 of this Manual). The 78.3001 to 79.3 MHz signal from the Low Loop Mixer Module is input at J4602 and splits into two parts. One part is output at J4601 to the 89-90 MHz Receiver Module. The other part is amplified by Q3503 to drive U3501 as a divide-by 10. The divided 7.83 to 7.93 MHz is used as the reference frequency for the high speed phase-lock compara-tor, U3509.

Transistor Q3501 and associated components operate as a 73.3 to 84.3 MHz voltage controlled oscillator (VCO). Q3502 buffers the VCO signal, which then splits in three directions. Q3505 amplifies the signal for output at J4605 to the Spectrum Analyzer RF Module. Q3504 amplifies the signal for output at J4604 to the FM Generator Module. Q3506 and Q3507 amplify the signal to drive U3506 as a divide-by 10. The divided VCO signal is compared at U3509A to phase-lock the VCO signal with the Low Loop Mixer reference frequency.

The divided VCO signal is further divided by 16 at U3507 and then divided by 512 at U3503 and U3504. The approximate 1 mS output pulse is used to gate the phase-lock signal at U3513B while the VCO frequency is sweeping. The phase-lock signal is integrated at U3508B (U3508A), and then sent to the VCO circuit and to the tracking filter on the Spectrum Analyzer RF Module.

A 100 Hz reference signal, input at pin 9 of J4603, is amplified by Q3510 to drive U3505 as a divide-by 10. The resulting 10 Hz is the analyzer sweep rate. The positive pulse through C3555 and CR3509 will cause pin 1 of U3514A (pin 7 of U3514B) to go high. Q3511 will then go high, unblanking the analyzer trace. Q3513 will conduct and begin charging C3556 and C3557 negative for the sweep ramp. When the ramp has reached -4.9 V, pin 7 of U3514B (pin 1 of U3514A) goes low to reset the sweep ramp.

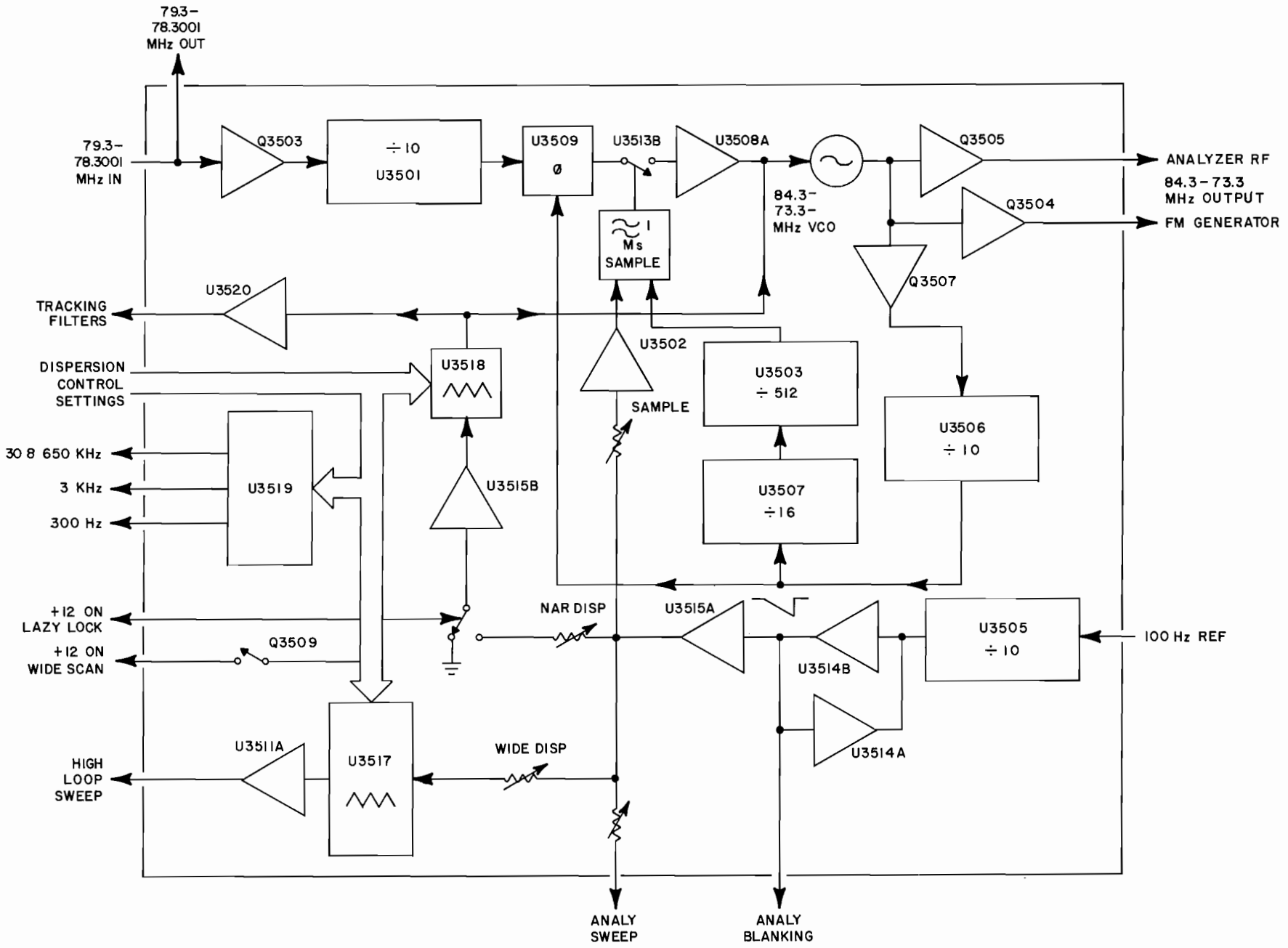


Figure 2-27 Spectrum Analyzer LO Detailed Block Diagram

The logic lines for the Spectrum Analyzer L.O. are controlled by the setting of the front panel ANALY DISPR Control as shown in Table 2-4. When pin 11 of U3510C is low, the dispersion gain of U3515A is increased for the 1 K and 2 K settings of the ANALY DISPR Control. At all other settings, the gain will be normal.

J4603, pin #	BCD Digit	ANALY DISPR Settings
16	1	2 K, 20 K, .2 M, 1 M, 5 M, Full
17	2	10 K, 20 K, .5 M, 1 M, 10 M, Full
1	4	100 K, .2 M, .5 M, 1 M
21	8	2 M, 5 M, 10 M, Full

Table 2-4 Logic Lines for Spectrum Analyzer L.O.

When pin 6 of U3516B goes low, U3517 will select one of the wide dispersion ranges. The wide dispersion range selected (2 M thru Full) is buffered at U3511A and output to the High Loop Module. The base of Q3516 will be pulled low through R3591, and +12 V will be output on the 650 kHz and 30 kHz bandwidth select line. The base of Q3509 also will be pulled low, causing a +12 V on wide scan signal to be output to the High Loop Module, which will select control for the tune ranges.

When pin 10 of U3510A goes low, the narrow dispersion ranges (1 K thru 1 M) will be selected by U3518, and the selected range will be sent to the tracking filters in the Spectrum Analyzer RF Module. When pins 2, 3 or 21 of U3519 go high, a narrow dispersion range will be selected to activate one of the bandwidth control lines. The 1 K and 2 K settings of the ANALY DISPR Control will select the 300 Hz bandwidth line. The 10 K and 20 K settings will select the 3 kHz bandwidth control line. The 100 K thru Full setting will select the 650 kHz and 30 kHz bandwidth control line.

When pin 10 of U3516A (pin 9 of U3516C) goes high, +12 V will be output to control the lazy lock circuit in the High Loop Module. This will occur at every ANALY DISPR setting except Full.

2-8-3 Spectrum Analyzer RF Module Detailed Theory

The Spectrum Analyzer RF Module receives the 89-90 MHz IF signal from the 1300 MHz IF Receiver Module at J5203 (See Figure 2-28 and the Spectrum Analyzer RF Schematic in Section 7 of this Manual). The signal is output at J5201 to the 89-90 MHz Receiver Module. The signal is also band-pass filtered in a 6-pole filter that will track from 84 to 95 MHz with the sweep signal, input at pin 5 of J5204, from the Spectrum Analyzer LO Module.

The filtered 84 to 95 MHz is mixed in MXR3701 with the input, at J5203, of 73.3 to 84.3 MHz (nominally 79.3 MHz). The resulting difference frequency of 10.7 MHz is band-pass filtered to 650 kHz in a six section filter. When +12 V is applied to pin 1 of J5204, to select 650 kHz or 30 kHz bandwidths, the 10.7 MHz IF will pass through Q3713 and be output at J5205 to the Spectrum Analyzer IF Module. Gain for the 650 kHz and 30 kHz bandwidths is set at R3777.

When +12 V is applied to pin 3 of J5204 to select the 3 kHz bandwidth, the 10.7 MHz IF will pass through three crystal filter stages and be output at J5205. Gain for the 3 kHz bandwidth is set at R3749. When +12 V is applied to pin 2 of J5204 to select the 300 Hz bandwidth, the 10.7 MHz IF will pass through four crystal filter stages and be output at J5205. Gain for the 300 Hz bandwidth is set at R3771.

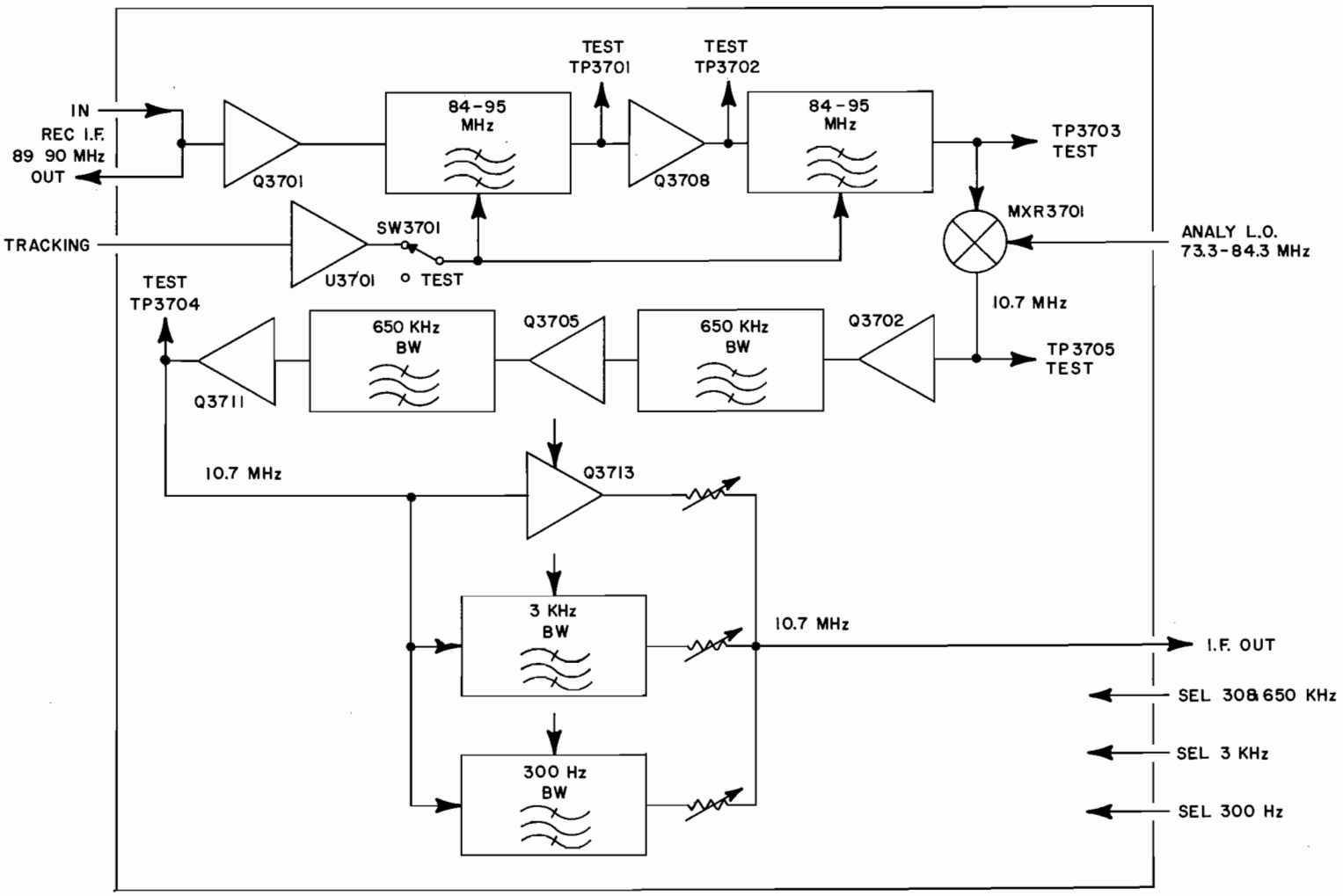


Figure 2-28 Spectrum Analyzer RF Module Detailed Block Diagram

2-9 MICROPROCESSOR FUNCTIONAL THEORY

The Microprocessor Functional Block contains the CPU/Memory PC Board and the I/O Interface PC Board (See Figure 2-29). If installed, the optional GPIB interface is also a part of this Functional Block. Refer to the GPIB supplement for information on the GPIB.

The CPU/Memory PC Board serves as the software controller for the FM/AM-1500 and generates the video for the menus. It communicates with the I/O Interface PC Board in a bi-directional mode and with the Dual Tone Generator in a write only mode.

The I/O Interface PC Board serves as the intermediary between the CPU bus and the hardware of the FM/AM-1500 as shown in Figure 2-29.

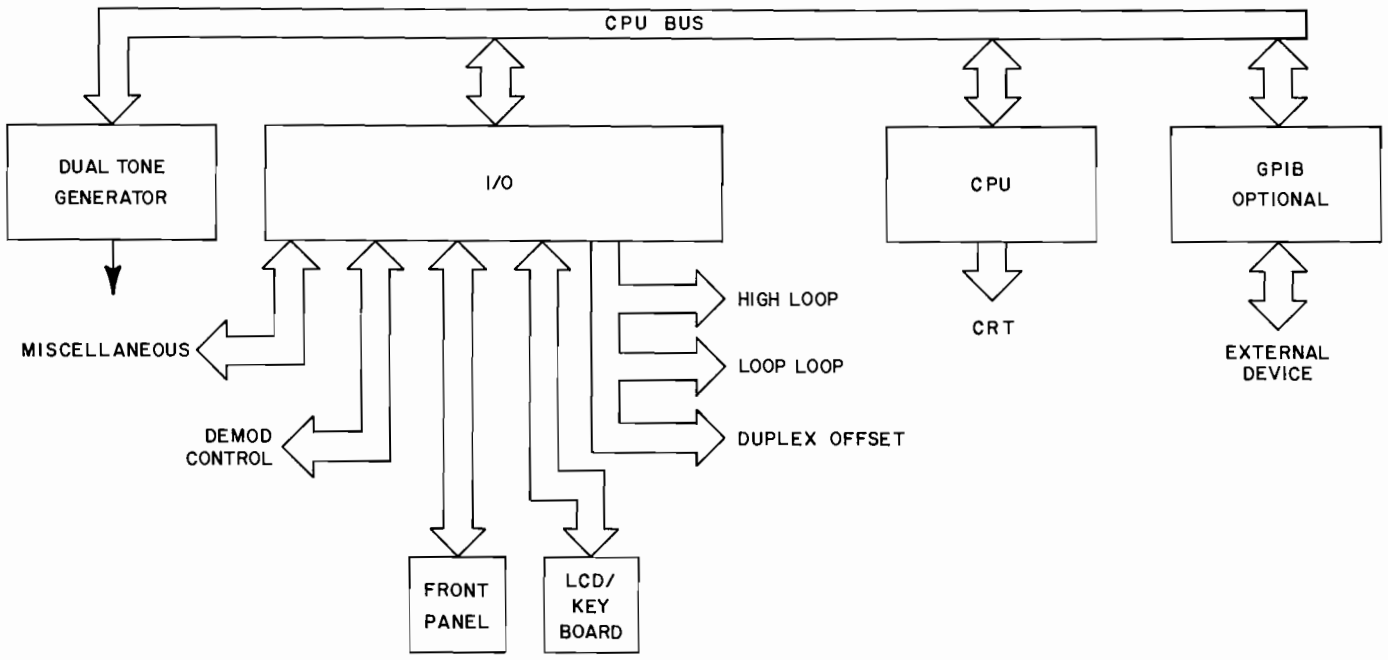


Figure 2-29 Microprocessor Functional Block Diagram

2-9-1 CPU/MEMORY PC Board Detailed Theory

CPU

The CPU used in the FM/AM-1500 is a Zilog Z-80 CPU, which is a fast 8-bit processor capable of addressing 65536 memory locations and 256 I/O devices (See Figure 2-30 and the CPU/MEMORY Schematic in Section 7 of this Manual). U9705 is the Z-80 CPU. The three buses used for communication are an 8-bit data bus, a 16-bit addresss bus and a 12-bit control bus. U4102 thru U4105 are the bus buffers for the CPU. U4108C and U4108D control the direction of the data bus. A 2 MHz system clock is input at pin 32 of P4101. U4106A inverts the clock, which is then referred to as Φ". U4127 divides Φ" down to a 20 kHz clock for the Timing and Interrupt circuit. Φ" is also sent over the control bus, where Q4103 and U4107F buffer/pull-up the clock to form Φ' and Φ. A 3.58 MHz crystal is used to clock the Z-80 and the CTCs. Φ' is used to clock all other CPU peripherals.

EPROM

U9704 is the processor's Programmed Memory Chip. Each chip position is jumper selectable either as EPROM or RAM. Normally, U9704 is jumper selected to EPROM configuration.

Non-Volatile RAM

U4117 and U4118 are the non-volatile RAMs which hold user-entered data in memory after the FM/AM-1500 is turned off, so that it is available upon power-up. The lithium battery, BT4101, provides +3 V, which is sufficient to hold the contents of the RAMs valid, even though +3 V is not sufficient for reading and writing.

+5 V Sense & Non-Volatile RAM Write Circuit

Q4106 and Q4107 form a differential amplifier to detect a power-off condition by monitoring the +5 V line. When the output of Q4106 goes below approximate +4.5 V, Q4105 turns off and Q4101 turns off. This disables U4119 and prevents any data in the non-volatile RAMs from being inadvertently changed. When the +5 V line drops below approximately +3 V, CR4103 becomes reverse biased and CR4102 becomes forward biased. When CR4102 is forward biased, the non-volatile RAMs are being powered by BT4101. This is the standby or power-off mode.

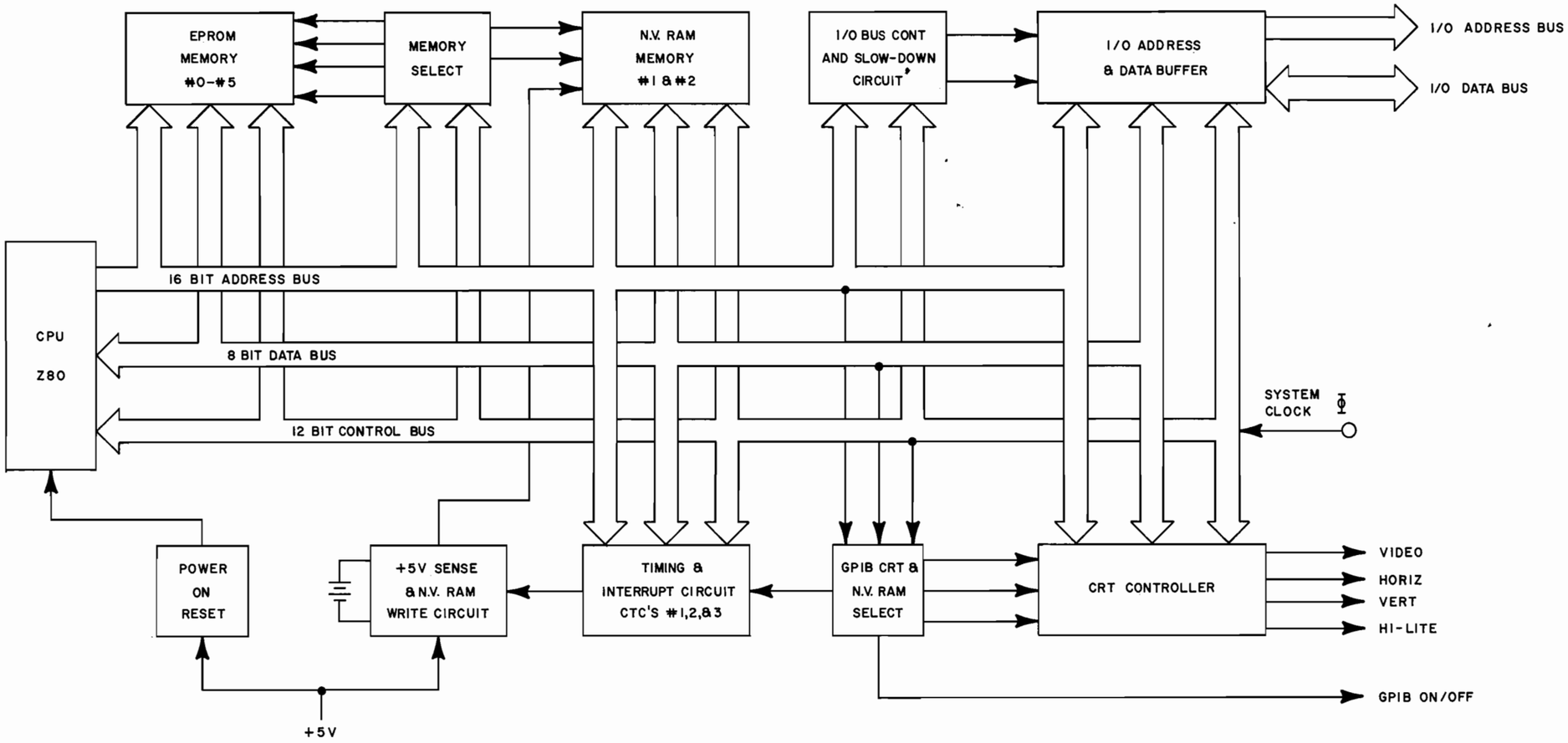


Figure 2-30 CPU/MEMORY PC BOARD
Detailed Block Diagram

Memory Select

U4112 is the memory select IC. When $\overline{MREQ}$ is active and $\overline{RFSH}$ is inactive, U4112 will select one of the RAM chips according to the binary code of address lines A13-A15. The memory REFRESH function of the Z-80 is not used in this configuration.

Timing and Interrupt Circuit

The timing and interrupt circuit consists of CTCs U4122, U4126 and U4137, along with U4120. CTC U4122 divides the 20 kHz signal derived from Φ" by a factor of 20 and outputs it as a 1 kHz (1 mS) line to CTCs U4126 and U4137. U4122 also controls the INT and BRDY lines to the CRT Controller Circuit. U4126 processes the GPIB, keyboard and DCS interrupts. These interrupt signals are also applied to the interrupt latch, U4120. U4120 is provided to allow the CPU to read the status of the interrupt lines from the data bus. U4123 is the address select chip for U4122, U4126 and U4120. U4137 acts as the Demod counter and is enabled by U4135.

GPIB, CRT & Non-Volatile RAM Select Circuit

U4135, U4136 and U4140 form this select circuit. U4135 enables CTC U4137. U4136 enables U4140 and the CRT Controller. U4140 disables the CRT Controller, enables the non-volatile RAM write (thru Q4104), and controls GPIB ON/OFF.

Watchdog Timer Circuit

The Watchdog Timer Circuit includes a Programmable Array Logic (PAL) device (U9701) and a Voltage Supervisor Chip (U9702). U9702 provides a signal to reset the Z80 CPU (U9705) and the Counter (U9703) during power-up operation or, during normal operation, if the +5 VDC source drops below nominal.

The PAL (U9701) initiates a reset if it detects an illegal write to non-volatile RAM or if the Counter (U9703) is allowed to time out. U9701 also provides chip selection for System ROM (U9704).

I/O Bus Control & Slow-Down Circuit

U4125 and U4124 are the bus control chips. U4125 turns off U4123 when the I/O bus is selected, and thus turns off the CTC's. U4125 also selects U4124, the data enable flip-flop, which outputs clock Φ' to the data buffer. At the same time, U4125 also triggers a slow-down circuit. The slow-down circuit is necessary because devices on the buffered buses require longer set-up times than devices tied directly to the Z-80 bus. U4121, U4107A, U4107D, U4106F, U4108A and U4108B form the slow-down circuit, which has a 3 μS time-out period. After the slow-down circuit times out, the Z-80 finishes its current machine cycle and disables U4125. On the first rising edge of the clock signal after U4125 is disabled, U4124 is set, disabling the I/O data bus. The I/O address bus is disabled when U4125 is disabled.

I/O Address & Data Buffer

U4130 and U4131 provide buffering for the I/O data and address buses, respectively. Notice that only five address lines are used, giving a possibility of 64 I/O devices, plus read and write.

CRT Controller Circuit

The CRT Controller circuit consists of U4141, U4142, U4139, U4143, U4134, U4132, U4133 and U4138. U4141 is a CRT Controller chip. It supplies a character address to the character EPROM, U4142. U4142 contains the dot pattern for each of the characters. U4141 also supplies a latch, U4139, with special function data (such as reverse video, hi-lite, sync, etc.) for each character. The output of the character EPROM is applied to a shift register, U4143, which shifts out each dot at a 2 MHz rate. U4134B, C and D, U4133 B and C and U4132C process the shifted video. The output of U4132C is the final video output of the CPU/MEMORY board. U4138, U4132 A and D, U4133A and U4134A generate the timing signals for the video generator. U4132A and D buffer the 2 MHz clock signal, and apply it to the shift register, U4143. U4138 is a divide-by 8 counter which supplies the character clock to the CRT Controller, U4141. Two interrupt outputs are provided from the CRT Controller to the Timing and Interrupt circuit. These outputs are BRDY (Buffer ReaDY) and INT (INTerrupt). The BRDY signal indicates that the CRT buffer is empty and may be filled with another character. The INT signal is used to generate an interrupt at the end of each frame.

2-9-2 I/O Interface PC Board Detailed Theory

General

The I/O Interface PC Board links the computer with hardware devices such as the High Loop Module, the Low Loop Module, Duplex Offset Module and the Front Panel (See Figure 2-31 and the I/O Interface Schematic in Section 7 of this Manual). In addition, the I/O Interface PC Board also performs analog to digital conversions for deviation and power information, and digital to analog conversions for the sweep (X-OUT) output.

Bus Buffer

The bus buffer consists of U4301 and U4302. U4302 is the address buffer. This chip buffers address lines A0/A5 and the read and write signals. U4302 is a single direction buffer and is a single direction buffer and is enabled continously.

U4301 is the data bus buffer, which buffers data lines DØ-D7. U4301 is a bi-directional buffer which is continuously enabled. The direction of buffering is controlled by the address decoder.

Address Decoder

The address decoder consists of U4305, U4306, U4307, U4308, U4323, U4324, U4334A and U4334B. U4306 decodes 8 byte blocks of addresses in the range of $ØØ_{(H)}$ thru $1F_{(H)}$ and $28_{(H)}$ thru $2F_{(H)}$, in the write mode. U4305 decodes each of the 8 individual addresses in the range of $18_{(H)}$ thru $1F_{(H)}$ in the write mode. U4323 decodes addresses $29_{(H)}$, $28_{(H)}$, $2A_{(H)}$ and $2C_{(H)}$.

U4307 decodes two 8 byte blocks, $ØØ_{(H)}$ thru $Ø7_{(H)}$ and $28_{(H)}$ thru $2F_{(H)}$ in the read mode. Diodes CR4301 and CR4302 along with R4301 form an OR gate, the output of which is used to control the direction of U4301, the data bus buffer. U4308 decodes each of the individual addresses between $28_{(H)}$ thru $2F_{(H)}$ in the read mode. U4324, along with U4334A and U4334B decodes addresses $ØØ_{(H)}$, $Ø1_{(H)}$, $Ø2_{(H)}$ and $Ø3_{(H)}$. U4334A and U4334B combine the decoded $Ø2_{(H)}$ and $Ø3_{(H)}$ outputs before applying them to U4329.

Talk-Back Circuit

The talk-back circuit is provided to check continuity of the data bus. During a write operation, information present on the address bus is latched into U4312. At the same time, information present on the data bus is latched into U4311. After a write operation, U4311 and U4312 can be read by the microprocessor and compared with the information sent during the write cycle. If the information which was read agrees with the information which was sent, the bus circuits are operating properly.

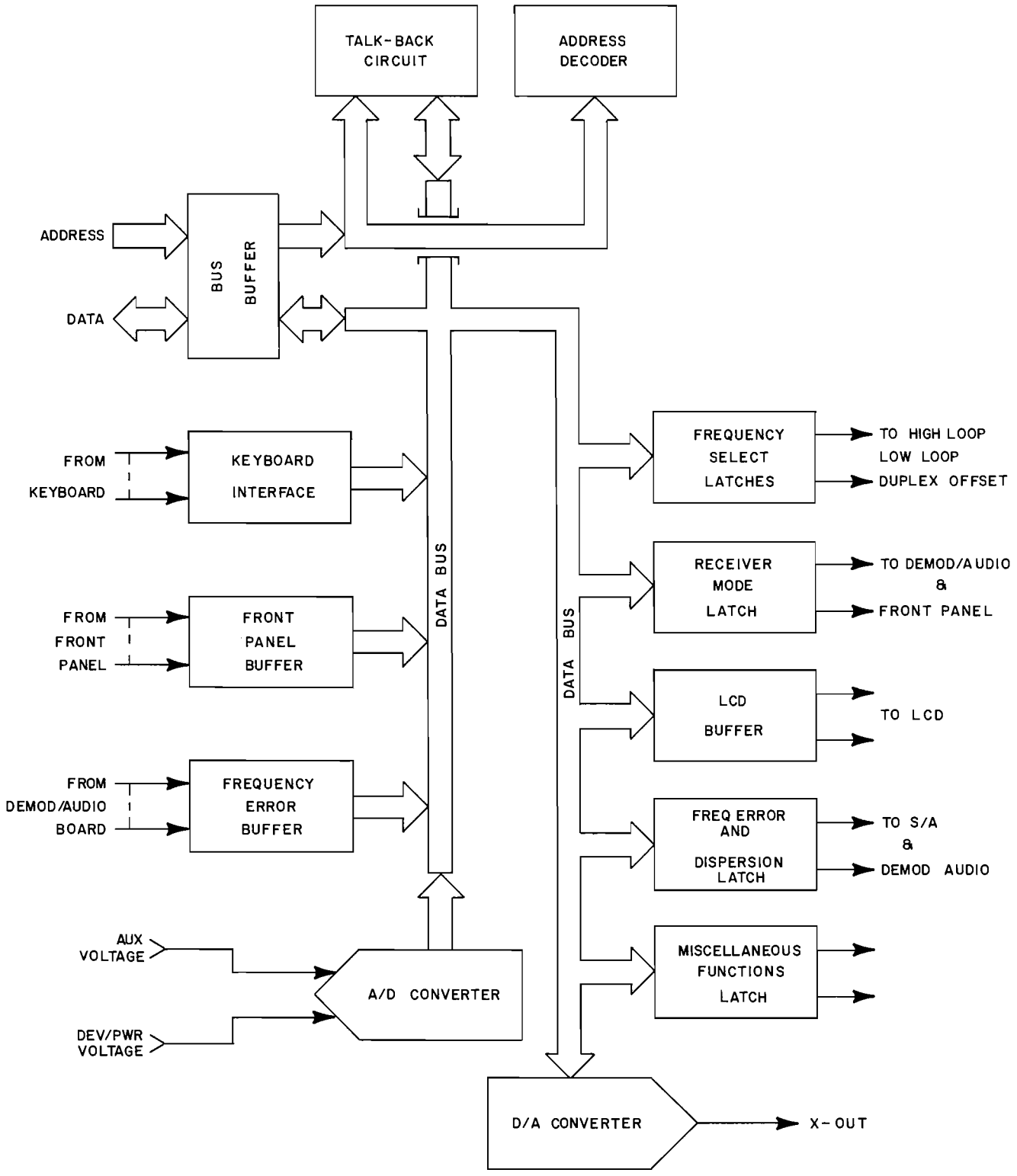


Figure 2-31 I/O Interface PC Board Detailed Block Diagram

Frequency Select Latches

The frequency select latches capture frequency data from the data bus when directed to do so by the address decoder. The captured data is stored and applied to the High Loop Module, Low Loop Module and Duplex Offset Module. U4303 and U4304 supply frequency information to the High Loop Module. U4309 and U4310 supply frequency information to the Low Loop Module. U4320 and U4321 supply frequency information to the Duplex Offset Module. U4303 also controls the low pass filters in the Delay Line Module and controls the 100 MHz and 200 MHz lines to the Duplex Offset Module.

Receiver Mode Latch

The receiver mode latch captures demodulation and bandwidth settings from the data bus when directed to do so by the address decoder. U4331 latches the data and presents this information to U4332, which is an open collector buffer. The output of U4332 is 0 volts for a logic low and +12 V for a logic high. Transistors Q4308 thru Q4314 invert and buffer the output of U4332. The current out of Q4308 thru Q4314 is sufficient for driving the front panel LED's and the Demod Audio PC Board.

LCD Buffer

The LCD buffer consists of U4314 and U4315. U4314 and U4315 are tri-state buffers. These buffers are continuously enabled and supply the LCD's with DØ-D5 of the data bus, along with AØ, A1 and A2 of the address bus and three lines from the address decoder which select one of three 8 byte blocks of I/O write locations.

These locations are $ØØ_{(H)}$ thru $Ø7_{(H)}$, $Ø8_{(H)}$ thru $ØF_{(H)}$ and $1Ø_{(H)}$ thru $17_{(H)}$. The LCD outputs are applied to the LCD displays on the front panel.

Freq Error and Dispersion Latch

The freq error and dispersion latch consists of U4339, U4340 and Q4315. U4339 captures freq error and dispersion settings from the data bus when directed to do so by the address decoder. The output of U4339 is applied to U4340 which is an open collector buffer. Its output swings between 0 V (for logic Ø) and +12 V (for logic 1). U4340 has seven open collector buffers. The eighth line (pin 5) out of U4340 is applied to R4367 and Q4315, which forms an open collector buffer. The output of U4340 and Q4315 is applied to the Demod Audio PC Board and to the Spectrum Analyzer LO Module.

Miscellaneous Functions Latch

The miscellaneous functions latch consists of U4325, U4326, Q4306 and Q4307. U4325 captures the applicable data from the data bus when directed to do so by the address decoder. U4326 is an open collector buffer. The output of U4326 swings between 0 V (logic Ø) and +12 V

(logic 1). The outputs of U4326 are applied to the following modules:

LINE	DESTINATION
GEN/$\overline{\text{REC}}$	Demod Audio PC Board
SIM/$\overline{\text{DUP}}$	Demod Audio PC Board
DEV POWER A	Demod Audio PC Board
DEV POWER B	Demod Audio PC Board
DEV POWER C	Demod Audio PC Board
PEAK/PEAK AVG.	Demod Audio PC Board
1 dB/10 dB	Spectrum Analyzer IF

Pin 5 of U4325 is applied to Q4307, which operates as an inverter. When the output of this inverter is low (i.e., track selected), Q4306 will be turned on to supply +12 V to the Demod Audio PC Board, the FM Generator Module and the Generate Mixer Module.

Keyboard Interface

The keyboard interface consists of U4313, U4316, U4317A and Q4301 thru Q4305. When no keys are depressed, the COL1 thru COL6 inputs to U4316 are open. With these lines open, they will be pulled up to +5 V by RN4301 and then applied to U4316. With no keys depressed, the ROW1 thru ROW4 inputs are also open. This causes Q4301 thru Q4304 to be turned off. Under these conditions, the outputs of Q4301 thru Q4304, which are applied to U4313 and U4317A, will be high. With all four inputs to U4317A high, its output will be low, causing Q4305 to be turned off. With Q4305 turned off, its output will be high (inactive). The above discussion describes the keyboard in its static state.

When a key is depressed, one of the "COL" (column) inputs is shorted to one of the "ROW" inputs. Which column input is applied to which row input is determined by which key is depressed (see keyboard schematic). When one of the column inputs are shorted to a row input, the applicable pull-up resistor in RN4301 will bias the applicable row transistor. When this happens, the column input is pulled down to approximately +0.65 V by the base-emitter drop, causing the applicable row transistor to be turned on and its output to go low. Therefore, when one of the keys are depressed, one column input to U4316 goes low and one row input to U4313 goes low. Also, when one of the outputs of the row transistors goes low, the output of U4317A goes high, causing Q4305 to turn on. When Q4305 turns on, its output goes low (active). This interrupts the computer, informing it that a key is pressed. When the interrupt occurs, the computer places the address of U4313 and U4316 on the address bus (these addresses are $28_{(H)}$ and $29_{(H)}$ respectively). The address decoder then gates the inputs of U4313 and U4316 onto the data bus to be read by the computer. Note that U4313 also gates information from the DISPLAY Control.

Front Panel Buffer

The front panel buffer consists of U4318, U4319 and U4327. Control settings from the front panel are presented to the inputs of these

buffers. The buffer gates these settings onto the data bus when directed to do so by the address decoder. It should be noted that U4322 also gates phase-lock and Overtemp flags from the Demod Audio PC Board.

Frequency Error Buffer

Frequency error information from the Demod Audio PC Board is presented to U4338, which gates this information onto the data bus when directed to do so by the address decoder.

Digital to Analog Converter

The digital to analog converter, U4330, is an 8 bit D/A converter with internal latches. Digital settings are latched into the D/A converter when directed to do so by the address decoder. The analog output is applied to the X-OUT connector on the rear panel of the FM/AM-1500. Two adjustments are provided to calibrate this D/A circuit. R4331 adjusts full scale voltage, while R4333 adjusts the offset.

Analog to Digital Converter

The analog to digital converter consists of U4337, U4335, U4336, U4333, U4327 and U4328. U4333 is the control latch for the A/D converter. 4 bits of this latch are used to control the CRT power, antenna attenuator and the key-depressed "BEEP". U4333 captures information off the data bus when directed to do so by the address decoder. Two lines out of U4333 are jumper programmable and may be connected to the RUN/HOLD and/or TEST inputs of U4337. Two other lines from U4333 are connected to U4336 to select the analog input to be measured. U4336 is a 4 input multiplexer which may select one of the following inputs:

INPUT	REMARKS
DEV/POWER	From Demod Audio PC Board
AUX	Not Currently Used
Reference Voltage	Self Test Purposes
GROUND	Self Test Purposes

The output of U4336 is applied to U4335, which is a sample and hold amplifier. The SAMPLE/HOLD input (pin 8) is controlled by the status output of U4337 via U4334D. The sample and hold amplifier prevents the voltage under test from changing while U4337 is going through a conversion cycle. R4350 is provided as an adjustment for the sample and hold amplifier. The output of the sample and hold amplifier is applied to U4337 for conversion via a low pass filter consisting of R4352 and C4354. U4337 is a 12 bit analog to digital converter. The A/D converter has one adjustment, R4354, provided for the reference voltage. The outputs of U4337, which is a digital representation of the voltage under test, are applied to U4327 and U4328. U4327 and U4328 gate the A/D outputs onto the data bus, when directed to do so by the address decoder.

SECTION 3 - PERFORMANCE EVALUATION

3-1 GENERAL

This section contains step-by-step test procedures for assessing the performance of the FM/AM-1500. These procedures should be performed as the first step in the troubleshooting/maintenance process, when the operating condition of the set is in question. All procedures in this section are performed using the FM/AM-1500 front and rear panels and do not require removal of the exterior case.

The following performance tests are included in this manual:

Each test procedure contains several common headings which are defined as follows:

3-2-1 Test procedure number followed by name of test procedure.

SPECIAL ACCESSORY EQUIPMENT REQ'D: List of any special accessory test equipment required to complete the test procedure.

TEST SET-UP DIAGRAM: A diagrammatic aid for making proper connections between the FM/AM-1500 and any special accessory equipment.

INITIAL FM/AM-1500
CONTROL SETTINGS: Initial FM/AM-1500 front panel control settings required to begin the test procedure. (Refer to Figure 3-1 for front panel control identification).

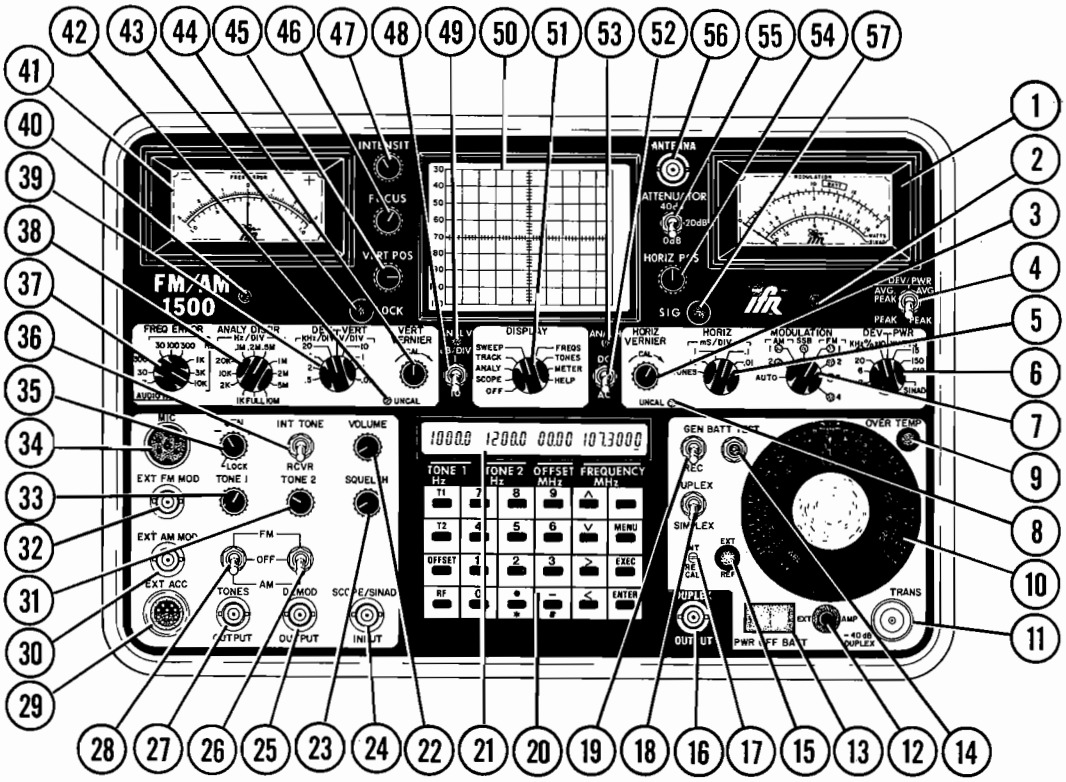
3-1-1 TEST EQUIPMENT REQUIREMENTS

Appendix E at the rear of this manual contains a comprehensive list of test equipment suitable for performing any of the procedures in this manual. Any other equipment meeting the specifications listed in Appendix E may be substituted in place of the recommended models.

3-1-2 CORRECTIVE MAINTENANCE PROCEDURES

The performance tests in this section will aid the operator/technician in determining whether the FM/AM-1500 is functioning properly or if a failure condition exists. A failure condition will normally be reflected as either a calibration error or a malfunction. A calibration error is defined as a measurement or reading (relating to the unit being tested) that is not within prescribed tolerances. In this condition, the set may outwardly appear to be functioning properly, despite the presence of a calibration error. A malfunction denotes a defective condition where a signal may be totally absent, grossly out of tolerance or where the unit itself (or any part thereof) is obviously not working properly.

In the event a failure condition is confirmed, the technician should take appropriate corrective maintenance action to return the set to its normal operating condition. The "CORRECTIVE MAINTENANCE FLOWCHART" shown in the Preface to this manual is intended to serve as a guide in directing the technician through the troubleshooting/maintenance process. By observing this general sequence, the technician will be able to use the troubleshooting/maintenance recommendations contained within this and other sections of this manual to return the FM/AM-1500 to normal operation.



1. MODULATION Meter
2. MODULATION Meter Mechanical Zero Adjustment
3. HORIZ VERNIER Control
4. AVG PEAK/PEAK Switch
5. HORIZ Control
6. DEV/PWR Control
7. MODULATION Control
8. UNCAL Indicator (Horizontal)
9. OVERTEMP Indicator
10. RF Output Level Control
11. TRANS/-40 dB DUPLEX Connector
12. EXT AMP Connector
13. PWR/OFF/BATT Switch
14. BATT TEST Button
15. EXT REF Indicator
16. DUPLEX OUTPUT Connector
17. INT REF CAL Adjustment
18. DUPLEX/SIMPLEX Switch
19. GEN/REC Switch
20. KEYBOARD
21. LCD
22. VOLUME Control
23. SQUELCH Control
24. SCOPE/SINAD INPUT Connector
25. DEMOD OUTPUT Connector
26. Tone 2 FM/OFF/AM Switch
27. TONES OUTPUT Connector
28. Tone 1 FM/OFF/AM Switch
29. EXT ACC Connector
30. EXT AM MOD Connector
31. TONE 2 Control
32. EXT FM MOD Connector
33. TONE 1 Control
34. MIC Connector
35. GEN/LOCK Control
36. INT TONE/RCVR Switch
37. FREQ ERROR Control
38. ANALY DISPR Control
39. DEV/VERT Control
40. FREQ ERROR Mechanical Zero
41. FREQ ERROR Meter
42. UNCAL Indicator (Vertical)
43. Freq LOCK Indicator
44. VERT VERNIER Control
45. VERT POS Control
46. FOCUS Control
47. INTENSITY Control
48. dB/DIV Switch
49. ANAL V Adjustment
50. CRT
51. DISPLAY Control
52. DC/AC Switch
53. ANAL H Adjustment
54. HORIZ POS Control
55. ATTENUATOR Switch (Antenna)
56. ANTENNA Connector
57. SIG Indicator

Figure 3-1 FM/AM-1500 Front Panel

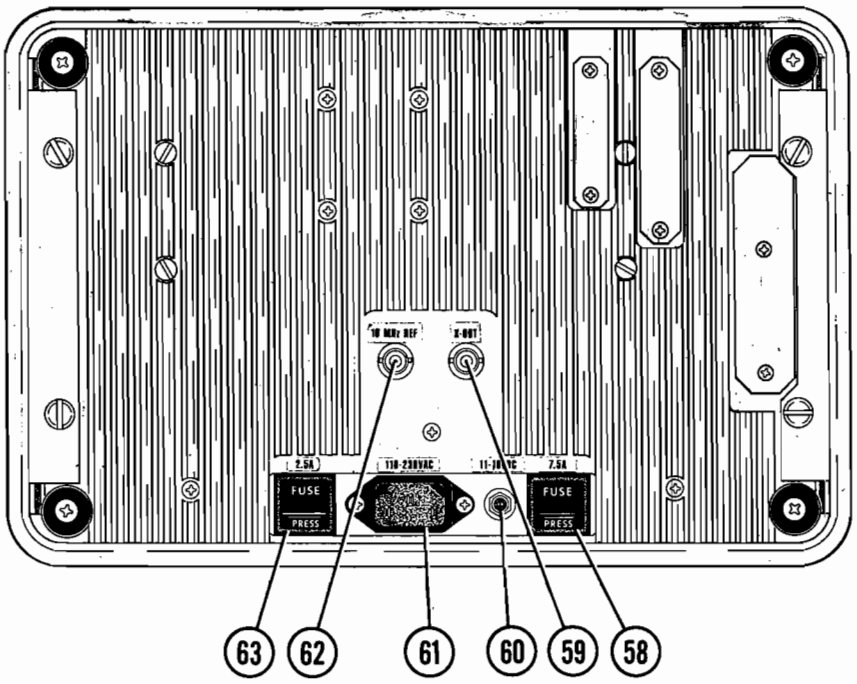


Figure 3-2 FM/AM-1500 Rear Panel

58. DC Fuse (7.5 Amp)

59. X-Out Connector
    Provides an output signal proportional to the FM/AM-1500 sweep signal when operating in the processor controlled sweep generator mode (RF Sweep or Tone Sweep Menus). The output amplitude at this connector is 0 to 10 volts, with 0 volts representing the start frequency and 10 volts representing the stop frequency.

60. DC Power Input Connector
    DC power input connector for 11 to 18 VDC supply.

61. AC Power Input Connector
    AC power input connector for 106 to 266 VAC supply at 50 to 400 Hz.

62. 10 MHz REF Connector
    Input/output connector for 10 MHz reference signal.

63. AC Line Fuse (2.5 Amp)

3-2 POWER SUPPLY FUNCTIONAL BLOCK

3-2-1 POWER SUPPLY VOLTAGE PERFORMANCE TEST

SPECIAL ACCESSORY EQUIPMENT REQ'D: 1 DC Voltmeter---Any

TEST SET-UP DIAGRAM: None

INITIAL FM/AM-1500 CONTROL SETTINGS:

CONTROL	SETTING
(13) PWR/OFF/BATT	"PWR"
(19) GEN/REC	"GEN"
(51) DISPLAY	Any position except "TRACK" or "SWEEP"

STEP PROCEDURE

1. Using Voltmeter, verify +12 VDC (±0.5) on pin 1 of MIC Connector (34).

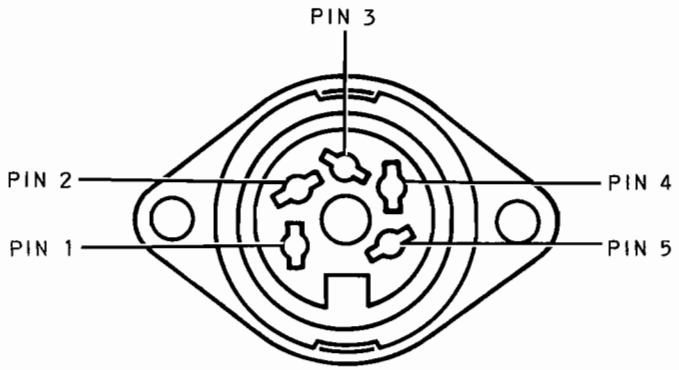


Figure 3-3 MIC Connector Pinouts

2. Using Voltmeter, verify voltages on EXT ACC Connector (29) as follows:

Pin 1	+12 VDC (±0.5)
Pin 3	+5 VDC (±0.3, -0.15)
Pin 2	-12 VDC (±0.5)

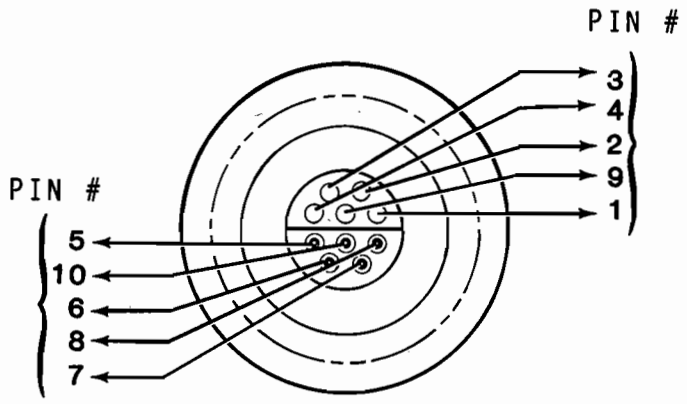


Figure 3-4 EXT ACC Connector Pinouts

3. Using voltmeter, verify +12 VDC (±0.5) on EXT AMP Connector (12).

4. Disconnect all test equipment.

NOTE

Front Panel voltages and tolerances only give an indication that the Power Supply output voltages are correct. If voltages are absent or grossly out of tolerance, refer to "SECTION 4 - CALIBRATION" for proper calibration procedure. If calibration is successful, problem is not in Power Supply, but is somewhere between Power Supply and Front Panel.

3-3 FREQUENCY STANDARD FUNCTIONAL BLOCK

3-3-1 FREQUENCY STANDARD PERFORMANCE TEST

SPECIAL ACCESSORY EQUIPMENT REQ'D:

1 50Ω Coax Cable, BNC to BNC

1 50Ω Termination (if necessary)

1 Oscilloscope---Capable of measuring 150 mVp-p

1 Frequency Counter---Capable of reading 10 MHz at 1 Hz resolution

1 10 MHz Frequency Standard

TEST SET-UP DIAGRAM: None

INITIAL FM/AM-1500 CONTROL SETTINGS:

CONTROL	SETTING
(13) PWR/OFF/BATT	"PWR"
(19) GEN/REC	"GEN"

STEP	PROCEDURE
1.	Connect a 50Ω coax cable between 10 MHz REF Connector (62) and input of an external Oscilloscope. Install a 50Ω termination if Oscilloscope does not have a 50Ω input. Verify amplitude of signal is > 75 mVp-P and < 150 mVp-p.
2.	Disconnect 50Ω coax cable from Oscilloscope. Connect coax to an external Frequency Counter. Install a 50Ω termination if Frequency Counter does not have a 50Ω input. Verify frequency is 10.000000 MHz (±5 Hz).
3.	Disconnect 50Ω coax cable from Frequency Counter. Connect coax to output of a 10 MHz frequency standard. Verify EXT REF (15) illuminates.
4.	Disconnect all test equipment from FM/AM-1500.

3-4 FREQUENCY SYNTHESIS FUNCTIONAL BLOCK

3-4-1 HIGH LOOP AND LOW LOOP PERFORMANCE TEST

SPECIAL ACCESSORY EQUIPMENT REQ'D: 1 50Ω Coax Cable, BNC to BNC

1 Frequency Counter---Capable of reading 1 GHz

TEST SET-UP DIAGRAM: None

INITIAL FM/AM-1500 CONTROL SETTINGS:

CONTROL	SETTING
(10) RF Output Level	As req'd for Frequency Counter (typically -20 dBm or greater)
(13) PWR/OFF/BATT	"PWR"
(18) DUPLEX/SIMPLEX	"SIMPLEX"
(19) GEN/REC	"GEN"
(21) LCD FREQUENCY READOUT	000.5000 MHz
(26) Tone 2 FM/OFF/AM	"OFF"
(28) Tone 1 FM/OFF/AM	"OFF"

STEP PROCEDURE

1. Connect 50Ω coax cable between TRANS/-40 dB DUPLEX Connector (11) and external Frequency Counter input. Verify external Frequency Counter reads 500 kHz (±1 Hz) and that Freq LOCK Indicator Lamp (43) illuminates.

2. Set LCD (21) to the following settings and verify frequency accuracy, depending on whether a TCXO or oven oscillator is installed. Verify Freq LOCK Indicator Lamp (43) illuminates at each setting.

LCD FREQ MHz	TCXO	OVEN
111.1111	±55 Hz	±6 Hz
222.2222	±111 Hz	±12 Hz
333.3333	±167 Hz	±17 Hz
444.4444	±223 Hz	±23 Hz
555.5555	±278 Hz	±28 Hz
666.6666	±334 Hz	±34 Hz
777.7777	±389 Hz	±39 Hz
888.8888	±444 Hz	±45 Hz
999.9999	±500 Hz	±50 Hz

3. Disconnect all test equipment from FM/AM-1500.

3-5 RECEIVER FUNCTIONAL BLOCK

3-5-1 RECEIVER SIGNAL PERFORMANCE TEST

SPECIAL ACCESSORY EQUIPMENT REQ'D:

1	Distortion Analyzer---Capable of measuring distortion at 1 kHz
1	50 Ω Coax Cable, BNC to BNC
1	Microphone
1	Signal Generator---Capable of generating 120.5000 MHz from -30 to -100 dBm

TEST SET-UP DIAGRAM: None

INITIAL FM/AM-1500 CONTROL SETTINGS:

CONTROL	SETTING
(7) MODULATION	"FM 2"
(10) RF Output Level	"0 dBm"
(13) PWR/OFF/BATT	"PWR"
(18) DUPLEX/SIMPLEX	"SIMPLEX"
(19) GEN/REC	"REC"
(21) LCD FREQUENCY READOUT	(Local FM Station) MHz
(36) INT TONE/RCVR	"RCVR"
(38) ANALY DISPR	"1 M"
(51) DISPLAY	"ANALY"

STEP PROCEDURE

RECEIVER

1. Connect an antenna to ANTENNA Connector (56). Rotate VOLUME Control (22) to a comfortable listening level and observe FM signal on FM/AM-1500 Spectrum Analyzer. Verify FM station can be clearly heard.

2. Rotate MODULATION Control (7) to "AM 2". Rotate ANALY DISPR Control (38) to "20 K". Set LCD (21) to the frequency of a local AM radio station. Observe AM signal on FM/AM-1500 Spectrum Analyzer. Verify AM station can be clearly heard.

3. Disconnect antenna from FM/AM-1500.

STEP PROCEDURE

SUB-AUDIBLE FILTER

1. Set FM/AM-1500 controls as follows:

CONTROL	SETTING
(6) DEV/PWR	"60 kHz"
(7) MODULATION	"FM 3"
(13) PWR/OFF/BATT	"PWR"
(19) GEN/REC	"GEN"
(21) LCD READOUT	0400.0 TONE 1 Hz 10000 TONE 2 Hz 120.5000 MHz
(26) Tone 2 FM/OFF/AM	"FM"
(28) Tone 1 FM/OFF/AM	"OFF"
(31) TONE 2	Fully ccw
(33) TONE 1	Fully ccw
(37) FREQ ERROR	"300 AUDIO Hz"
(51) DISPLAY	"METER"

2. Rotate TONE 2 Control (31) slowly cw until a DEMOD count of 10,000 Hz can be read on CRT (50), or until control is fully cw. Verify Deviation is $\geq$ 10 kHz.

3. Rotate TONE 2 Control (31) fully ccw.

4. Rotate DEV/PWR Control (6) to "2 kHz". Set LCD (21) to 0150.0 TONE 2 Hz. Rotate TONE 2 Control (31) slowly cw until a DEMOD count of 150 Hz can be read on CRT (50). Verify Deviation is $\leq$ 1.0 kHz. Verify both digital and analog meters read 250 Hz FREQ ERROR.

5. Set LCD (21) to 0410.0 TONE 1 Hz. Set LCD (21) to 10000 TONE 2 Hz. Rotate TONE 2 Control (31) slowly until lowest deviation level possible is reached, while still being able to read a 10 kHz DEMOD count on CRT (50). Verify deviation is $\leq$ 1.0 kHz. Verify both digital and analog FREQ ERROR meters are pegged.

RECEIVER SENSITIVITY

1. Set FM/AM-1500 controls as follows:

CONTROL	SETTING
(7) MODULATION	"FM 1"
(13) PWR/OFF/BATT	"PWR"
(19) GEN/REC	"REC"
(21) LCD FREQUENCY READOUT	120.5000 MHz
(37) FREQ ERROR	"300 Hz"
(51) DISPLAY	"METER"

STEP PROCEDURE

2. Set external Signal Generator to 120.5000 MHz at -50 dBm.

3. Connect 50Ω coax cable between ANTENNA Connector (56) and output of Signal Generator. Note and record frequency error on both analog and digital meters.

4. Decrease output level of Signal Generator until a difference of 100 Hz from reading recorded in Step 3 is reached. Verify output level of external Signal Generator is $\leq$ -99 dBm.

5. Rotate MODULATION Control (7) to "FM 2". Adjust output level of external Signal Generator until a difference of 100 Hz below reading recorded in Step 3 is reached. Verify output level of external Signal Generator is $\leq$ -90 dBm.

6. Disconnect test equipment from FM/AM-1500.

DIGITALLY CODED SQUELCH

1. Set FM/AM-1500 controls as follows:

CONTROL	SETTING
(7) MODULATION	"FM 2"
(13) PWR/OFF/BATT	"PWR"
(19) GEN/REC	"GEN"
(51) DISPLAY	"TONES"

2. Depress following keys: "MENU, V, MENU, ENTER, >, 1, 2, 6, >, >, ·, 5, ENTER".

NOTE

Make sure polarity (POL) is normal (NORM) on menu.

3. Connect Microphone to MIC Connector (34).

4. Depress following keys: "EXEC, 2nd, DCS, 1, ENTER". Verify the blank spaces under "Valid Code Numbers" on CRT (50) have "126 302 430 110" displayed continuously (no blinking). Speak into keyed Microphone and verify displayed numbers are stable.

5. Depress following keys: "RF, ENTER, >, >, ^, ENTER, EXEC, ENTER". Verify the numbers "755 752" are displayed continuously. Speak into keyed Microphone and verify the displayed numbers are stable.

6. Depress "RF, ENTER" to stop function.

7. Disconnect Microphone from FM/AM-1500.

STEP PROCEDURE

SIGNAL STRENGTH METER

NOTE:

This procedure gives a relative signal strength indication only. Failure to meet the ±10 dBm tolerance does not mean the FM/AM-1500 is faulty.

1. Set FM/AM-1500 controls as follows:

CONTROL	SETTING
(6) DEV/PWR	"SIG"
(13) PWR/OFF/BATT	"PWR"
(19) GEN/REC	"REC"
(21) LCD FREQUENCY READOUT	120.5000 MHz
(51) DISPLAY	"METER"

2. Set Signal Generator to 120.5000 MHz at approximately -30 dBm.

3. Connect 50Ω coax cable between output of Signal Generator and ANTENNA Connector (56).

4. Adjust output level of Signal Generator for a 100% (±0.1%) reading on digital (SIGNAL %) display. Verify dBm setting on Signal Generator is -30 dBm (±10 dBm).

5. Disconnect all test equipment from FM/AM-1500.

AUDIO DISTORTION

1. Set FM/AM-1500 controls as follows:

CONTROL	SETTING
(6) DEV/PWR	"6 kHz"
(7) MODULATION	"FM 1"
(13) PWR/OFF/BATT	"PWR"
(19) GEN/REC	"GEN"
(21) LCD TONE 1 READOUT	1000.0 Hz TONE 1
(26) Tone 2 FM/OFF/AM	"OFF"
(28) Tone 1 FM/OFF/AM	"FM"
(39) DEV/VERT	"2 kHz/DIV"
(51) DISPLAY	"SCOPE"

2. Rotate Tone 1 Control (33) until MODULATION Meter (1) indicates 5 kHz deviation.

3. Observe waveform on CRT (50) and verify no obvious distortion.

4. Connect 50Ω coax cable between DEMOD OUTPUT Connector (25) and input of an external Distortion Analyzer. Verify distortion is $\leq$ 5%.

STEP	PROCEDURE

5. Disconnect all test equipment from FM/AM-1500.

SINAD

1. Set FM/AM-1500 controls as follows:

CONTROL	SETTING
(5) HORIZ	"1 mS/DIV"
(6) DEV/PWR	"SINAD"
(13) PWR/OFF/BATT	"PWR"
(18) DUPLEX/SIMPLEX	"SIMPLEX"
(19) GEN/REC	"GEN"
(21) LCD TONE 1 READOUT	1000.0 Hz TONE 1
TONE 2 READOUT	1800.0 Hz TONE 2
(26) Tone 2 FM/OFF/AM	"OFF"
(28) Tone 1 FM/OFF/AM	"OFF"
(31) TONE 2	Fully ccw
(33) TONE 1	Fully cw
(39) DEV/VERT	"1 V/DIV"
(51) DISPLAY	"SCOPE"

2. Connect 50Ω coax cable between TONES OUTPUT Connector (27) and SCOPE/SINAD INPUT Connector (24).

3. Rotate VERT VERNIER Control (44) to make FM/AM-1500 CRT (50) display exactly 8 major vertical divisions.

4. Rotate TONE 1 Control (33) fully ccw.

5. Rotate TONE 2 Control (31) in a cw direction until CRT (50) display is exactly 2 major vertical divisions.

6. Rotate TONE 1 Control (33) fully cw.

7. Rotate DISPLAY Control (51) to "METER". Verify both digital meter display on CRT (50) and MODULATION Meter (1) display are reading -12 dB (±1 dB) on SINAD scales.

8. Rotate TONE 2 Control (31) fully ccw. Verify digital meter display on CRT (50) reads $\leq$ -26 dB.

9. Disconnect all test equipment from FM/AM-1500.

3-5-2 FREQUENCY ERROR PERFORMANCE TEST

SPECIAL ACCESSORY EQUIPMENT REQ'D:

1 Signal Generator---Capable of generating 120.5030 MHz at -50 dBm

2 50Ω Coax Cables, BNC to BNC

1 10 MHz Frequency Standard

TEST SET-UP DIAGRAM: None

INITIAL FM/AM-1500 CONTROL SETTINGS:

CONTROL	SETTING
(13) PWR/OFF/BATT	"PWR"
(18) DUPLEX/SIMPLEX	"SIMPLEX"
(19) GEN/REC	"REC"
(21) LCD FREQUENCY READOUT	120.5000 MHz
(37) FREQ ERROR	"1 kHz"
(51) DISPLAY	"METER"
(7) MODULATION	"FM2" (or "FM3" or "FM4")

STEP PROCEDURE

1. Connect 50Ω coax cable between 10 MHz standard and external time base input of Signal Generator.

2. Set Signal Generator to 120.5000 MHz at -50 dBm.

3. Connect 50Ω coax cable between output of Signal Generator and ANTENNA Connector (56). Verify FREQ ERROR is $\leq$ 100 Hz. Note and record reading.

4. Rotate INT REF CAL Adjustment (17) to both stops. Verify range is approximately equal in both directions. Rotate INT REF CAL Adjustment (17) back to setting recorded in Step 3.

5. Rotate FREQ ERROR Control (37) to "30 Hz".

6. Set external Signal Generator to 120.5001 MHz. Verify full deflection of FREQ ERROR Meter (41) and verify approximately 100 Hz ($\pm$ reading recorded in Step 3) on CRT (50) digital meter.

7. Set external Signal Generator to 120.4999 MHz and verify same results as in Step 6.

STEP	PROCEDURE
8.	Rotate FREQ ERROR Control (37) to "300 Hz". Set external Signal Generator first to 120.4997 MHz, then to 120.5003 MHz. Verify a 300 Hz (± 5%) frequency error on both the analog and digital meters at each setting.
9.	Rotate FREQ ERROR Control (37) to "1 kHz". Set external Signal Generator first to 120.5010 MHz, then to 120.4990 MHz. Verify a 1 kHz frequency error on both the analog and digital meters at each setting.
10.	Rotate FREQ ERROR Control (37) to "3 kHz". Set external Signal Generator first to 120.5030 MHz, then to 120.4970 MHz. Verify a 3 kHz frequency error on both the analog and digital meters at each setting.
11.	Rotate FREQ ERROR Control (37) to "10 kHz". Set external Signal Generator first to 120.5100 MHz, then to 120.4900 MHz. Verify a 10 kHz frequency error on both the analog and digital meters at each setting.
12.	Set GEN/REC Switch (19) to "GEN". Rotate GEN/LOCK Control (35) out of "LOCK". Verify by rotating the GEN/LOCK Control (35) to its - and + limits, that there is at least 10 kHz variation from 0 on both sides of the FREQ ERROR Meter (41).

3-5-3 MODULATION METER PERFORMANCE TEST

SPECIAL ACCESSORY EQUIPMENT REQ'D:

1 Signal Generator---Capable of generating 850 MHz at -50 dBm; 2 to 8 kHz Dev. at 1 to 10 kHz rate

1 Modulation Meter---Capable of measuring 2 to 8 kHz Dev.

1 50Ω Coax Cable, BNC to BNC

TEST SET-UP DIAGRAM: None

INITIAL FM/AM-1500 CONTROL SETTINGS:

CONTROL	SETTING
(4) AVG PEAK/PEAK	"AVG"
(6) DEV/PWR	"6 kHz"
(7) MODULATION	"FM 2"
(19) GEN/REC	"REC"
(21) LCD FREQUENCY READOUT	850.0000 MHz
(51) DISPLAY	"METER"

STEP PROCEDURE

1. Set external Signal Generator to 850 MHz at -50 dBm. Modulate its FM signal with 5 kHz Deviation at 1 kHz.

2. Set external Modulation Meter bandpass filters to 300 Hz and 3 kHz. Verify modulation level of Signal Generator by using external Modulation Meter.

3. Connect 50Ω coax cable between ANTENNA Connector (56) and output of Signal Generator. Verify digital meter on CRT (50) is accurate (±5%).

4. Change Signal Generator modulation to 2 kHz Deviation at 6 kHz. Change Modulation Meter bandpass filters to 300 Hz and 15 kHz. Verify modulation level of Signal Generator by using external Modulation Meter.

5. Repeat Step 3, but verify accuracy as ±3%.

6. Rotate MODULATION Control (7) to "FM 3". Rotate DEV/PWR Control (6) to "20 kHz". Change Modulation Meter low-pass filter to 120 kHz. Change Signal Generator modulation to 8 kHz Deviation at 10 kHz. Verify modulation level of Signal Generator by using external Modulation Meter.

STEP	PROCEDURE
7.	Repeat Step 3, verify accuracy as ±3%.
8.	Rotate DISPLAY Control (51) to "SCOPE". Rotate DEV/VERT Control (39) to "5 kHz/DIV". Verify 8 kHz Deviation (±10%) on CRT (50).
9.	Change Signal Generator modulation to 2 kHz Deviation at 6 kHz. Rotate DEV/VERT Control (39) to "2 kHz". Verify 2 kHz Deviation (±10%) on CRT (50).
10.	Change Signal Generator modulation to 5 kHz Deviation at 1 kHz. Verify 5 kHz Deviation (±10%) on CRT (50).

3-5-4 OSCILLOSCOPE PERFORMANCE TEST

SPECIAL ACCESSORY EQUIPMENT REQ'D:

1 Oscilloscope Calibrator Module (Plug-In)--- Capable of 0.5 to 50 VAC

1 50Ω Coax Cable, BNC to BNC

1 Audio Generator---Capable of generating 100 Hz to 100 kHz

TEST SET-UP DIAGRAM: None

INITIAL FM/AM-1500 CONTROL SETTINGS:

CONTROL	SETTING
(3) HORIZ VERNIER	"CAL"
(39) DEV/VERT	".01 V/DIV"
(44) VERT VERNIER	"CAL"
(51) DISPLAY	"SCOPE"

STEP	PROCEDURE
1.	Connect 50Ω coax cable between SCOPE/SINAD INPUT Connector (24) and output of Oscilloscope Calibrator.
2.	Set output of Oscilloscope Calibrator to 50 mVAC. Verify a 5 (±0.5) major division deflection.
3.	Rotate DEV/VERT Control (39) to ".1 V/DIV" and set output of Oscilloscope Calibrator to 0.5 VAC. Verify a 5 (±0.5) major division deflection.
4.	Rotate DEV/VERT Control (39) to "1 V/DIV" and set output of Oscilloscope Calibrator to 5 VAC. Verify a 5 (±0.5) major division deflection.
5.	Rotate DEV/VERT Control (39) to "10 V/DIV" and set output of Oscilloscope Calibrator to 50 VAC. Verify a 5 (±0.5) major division deflection.
6.	Rotate VERT VERNIER Control (44) fully ccw. Verify deflection is less than 2.5 major divisions.
7.	Disconnect 50Ω coax cable from Oscilloscope Calibrator and connect 50Ω coax cable to output of an Audio Generator.

STEP	PROCEDURE
8.	Rotate DEV/VERT Control (39) to "1 V/DIV". Set output of Audio Generator to 100 kHz at $\geq$ 2 Vp-p and rotate HORIZ Control (5) to ".01 mS/DIV". Verify CRT (50) displays 10 (±2) full cycles.
9.	Set output of Audio Generator to 10 kHz and rotate HORIZ Control (5) to ".1 mS/DIV". Verify CRT (50) displays 10 (±2) full cycles.
10.	Set output of Audio Generator to 1 kHz and rotate HORIZ Control (5) to "1 mS/DIV". Verify CRT (50) displays 10 (±2) full cycles.
11.	Set output of Audio Generator to 100 Hz and rotate HORIZ Control (5) to "10 mS/DIV". Verify CRT (50) displays 10 (±2) full cycles.
12.	Repeat Steps 8 thru 11 and verify that HORIZ VERNIER Control (3) will vary horizontal spacing on CRT (50) for each step.
13.	Disconnect all test equipment from FM/AM-1500.

3-5-5 POWER METER PERFORMANCE TEST

SPECIAL ACCESSORY EQUIPMENT REQ'D:
- 1 RF Power Source---Capable of generating 15.7 to 902 MHz at 10 to 30 W
- 1 50Ω Coax Cable, BNC to BNC

TEST SET-UP DIAGRAM: None

INITIAL FM/AM-1500 CONTROL SETTINGS:

CONTROL	SETTING
(6) DEV/PWR	"15 WATTS"
(13) PWR/OFF/BATT	"PWR"
(51) DISPLAY	"METER"

STEP	PROCEDURE
1.	Set RF Power Source to 860 MHz at 10 W.
2.	Connect 50Ω coax cable between output of RF Power Source and TRANS/-40 dB DUPLEX Connector (11). Verify power reading on digital and analog meters is 10 W (±1.15 W).
3.	Rotate DEV/PWR Control (6) to "150 WATTS". Verify same readings as in Step 2.
4.	Set RF Power Source to 30 W output power. Verify power reading on digital and analog meters is 30 W (±6.6 W).
5.	Disconnect 50Ω coax cable. Rotate DEV/PWR Control (6) to "15 WATTS". Set RF Power Source to 157 MHz at 10 W. Repeat Steps 2 thru 4.
6.	Disconnect all test equipment from FM/AM-1500.

3-6 GENERATOR FUNCTIONAL BLOCK

3-6-1 RF OUTPUT PERFORMANCE TEST

SPECIAL ACCESSORY EQUIPMENT REQ'D:

1 Spectrum Analyzer---Capable of measuring 0 dBm at 850 MHz

1 50Ω Coax Cable, BNC to BNC

1 Microphone

1 Modulation Meter---Capable of measuring residual FM at 850 MHz

1 Signal Generator---Capable of generating 850 MHz at 0 to -90 dBm

1 Power Meter---Capable of measuring 0 dBm at 850 MHz

TEST SET-UP DIAGRAM: None

INITIAL FM/AM-1500 CONTROL SETTINGS:

CONTROL	SETTING
(10) RF Output Level	"0 dBm"
(13) PWR/OFF/BATT	"PWR"
(18) DUPLEX/SIMPLEX	"SIMPLEX"
(19) GEN/REC	"GEN"
(21) LCD FREQUENCY READOUT	850.0000 MHz

STEP PROCEDURE

ATTENUATOR ACCURACY

1. Set external Spectrum Analyzer to log scale of 2 dB/division.

2. Connect 50Ω coax cable between TRANS/-40 dBm DUPLEX Connector (11) and external Spectrum Analyzer input. Set reference level of external Spectrum Analyzer so that top of applied signal exactly reaches a horizontal graticule. Note and record position of signal.

3. Disconnect 50Ω coax cable from TRANS/-40 dB DUPLEX Connector (11) and connect 50Ω coax cable to output of Signal Generator.

4. Set external Signal Generator to 850 MHz at output level in Table 3-1 corresponding to RF Output Level (10) setting.

STEP PROCEDURE

5. Set top of applied signal on external Spectrum Analyzer to same position as recorded in Step 2 by adjusting only output level of Signal Generator.

6. Disconnect 50Ω coax cable from Spectrum Analyzer and connect 50Ω coax cable to input of external Power Meter. Verify Power Meter reads as in Table 3-1 for corresponding RF Output Level (10).

7. Repeat Steps 2 thru 6 for each RF Output Level (10) setting in Table 3-1.

NOTE

For RF Output Level (10) settings of -50 dBm and below, it may be necessary to add attenuation pad(s) between Signal Generator and Spectrum Analyzer in Step 5 in order for Power Meter to operate properly in Step 6. For instance, if Power Meter will only read correctly at -50 dB or above and RF Output Level (1) is -70 dBm, a 20 dB pad plus a Signal Generator output of -50 dBm would result in an external Spectrum Analyzer reading of -70 dBm.

If it is necessary to add attenuation for proper attenuation reading into Power Meter, remove attenuation before performing Step 7 and add value of attenuation pad to resultant Power Meter reading.

RF OUTPUT LEVEL (dBm)	SIGNAL GENERATOR OUTPUT (dBm)	POWER METER READING (dBm)
0	0	0 (±4)
-10	-10	-10 (±2.0)
-30	-30	-30 (±2.0)
-50	-50	-50 (±2.0)
-70	-70	-70 (±2.0)
-90	-90	-90 (±2.5)

Table 3-1 Attenuator Accuracy Test Settings

8. Connect 50Ω coax cable between TRANS/-40 dB DUPLEX Connector (11) and input of external Spectrum Analyzer. Rotate RF Output Level (10) fully ccw and verify Spectrum Analyzer shows no RF leakage at TRANS/-40 dB DUPLEX Connector (11) of FM/AM-1500.

9. Disconnect all test equipment from FM/AM-1500.

STEP PROCEDURE

MODULATION

1. Set FM/AM-1500 controls as follows:

CONTROL	SETTING
(5) HORIZ	"1 mS/DIV"
(6) DEV/PWR	"20 kHz"
(7) MODULATION	"AM 2"
(13) PWR/OFF/BATT	"PWR"
(18) DUPLEX/SIMPLEX	"SIMPLEX"
(19) GEN/REC	"GEN"
(21) LCD TONE 1 READOUT	1000.0 Hz
(26) Tone 2 FM/OFF/AM	"OFF"
(28) Tone 1 FM/OFF/AM	"AM"
(36) INT TONE/RCVR	"RCVR"
(39) DEV/VERT	"5 kHz/DIV"
(51) DISPLAY	"SCOPE"

2. Rotate Tone 1 Control (33) until CRT (50) and MODULATION Meter (1) both display at least 90% AM.

3. Rotate DISPLAY Control (51) to "METER". Verify 90% AM (±7%).

4. Rotate MODULATION Control (7) to "FM 2". Set Tone 1 FM/OFF/AM Switch (28) to "FM". Rotate DEV/PWR Control (6) to "60 kHz". Rotate TONE 1 Control (33) fully cw. Verify $\geq$ 20 kHz deviation on MODULATION meter (1) and on CRT (50) digital display.

5. Set Tone 1 FM/OFF/AM Switch (28) to "OFF". Connect 50Ω coax cable between TONES OUTPUT Connector (27) and EXT FM MOD Connector (32). Verify $\geq$ 20 kHz deviation on CRT (50) digital display and MODULATION Meter (1).

6. Disconnect 50Ω coax cable from EXT FM MOD Connector (32) and connect it to EXT AM MOD Connector (30). Rotate MODULATION Control (7) to "AM 2". Verify modulation is present on CRT (50) digital display and MODULATION Meter (1).

7. Disconnect coax cable from FM/AM-1500. Connect a microphone to MIC Connector (34). Set GEN/REC Switch (19) to "REC".

8. Key microphone and whistle into it. Verify 100% AM (±50%) on CRT (50) digital display and MODULATION Meter (1) while whistling into microphone.

9. Rotate MODULATION Control (7) to "FM 2". Verify $\geq$3.50 kHz deviation while whistling into microphone.

10. Rotate DISPLAY Control (51) to "ANALY". Verify keying the microphone causes a signal to appear on CRT (50).

STEP PROCEDURE

11. Disconnect all test equipment from FM/AM-1500.

DELAY LINE

1. Set FM/AM-1500 controls as follows:

CONTROL	SETTING
(10) RF Output Level	"-30 dBm"
(13) PWR/OFF/BATT	"PWR"
(18) DUPLEX/SIMPLEX	"SIMPLEX"
(21) LCD FREQUENCY READOUT	001.0000 MHz
(26) Tone 2 FM/OFF/AM	"OFF"
(28) Tone 1 FM/OFF/AM	"OFF"
(51) DISPLAY	"ANALY"

2. Set external Spectrum Analyzer settings as follows:

   Dispersion - 200 kHz/division
   Log Scale - 10 dB/division
   Reference Level - as required to display entire signal

3. Connect 50Ω coax cable between TRANS/-40 dB DUPLEX Connector (11) and input of external Spectrum Analyzer.

4. Using KEYBOARD (20), press "RF,> ,> " to place cursor under 1 MHz digit on LCD (21).

5. By pressing "^" Key repeatedly, step MHz on LCD FREQUENCY READOUT (21) up to 100 MHz. At each step, observe the display on the external Spectrum Analyzer. The noise level around the base of the displayed signal should rise and immediately fall back to a low level (below -60 dBc). Verify the FM/AM-1500 does not have a rattling noise at each step in frequency.

6. Set LCD FREQUENCY (21) to 170.000 MHz. Repeat Steps 4 and 5, but stepping up to 180.0000 MHz.

7. Set LCD FREQUENCY (21) to 400.0000 FREQ MHz. Repeat Steps 4 and 5, but stepping up to 515.0000 FREQ MHz.

NOTE

Crossover distortion will produce noticeable sidebands around 515.0000 MHz.

8. Set LCD FREQUENCY (21) to 800.0000 MHz. Repeat Steps 4 and 5, but stepping up to 950.0000 FREQ MHz.

STEP PROCEDURE

9. Set LCD FREQUENCY (21) to 999.9999 MHz. Verify same results as in Step 5.

NOTE:

If FM/AM-1500 makes a rattling noise, or if noise level at base of each selected signal does not immediately decrease, the Delay Line is defective.

10. Disconnect all test equipment from FM/AM-1500.

RESIDUAL FM

1. Set FM/AM-1500 controls as follows:

CONTROL	SETTING
(4) AVG PEAK/PEAK	"PEAK"
(6) DEV/PWR	"2 kHz"
(7) MODULATION	"FM 2"
(10) RF Output Level	"0 dBm"
(13) PWR/OFF/BATT	"PWR"
(18) DUPLEX/SIMPLEX	"SIMPLEX"
(19) GEN/REC	"GEN"
(26) Tone 2 FM/OFF/AM	"OFF"
(28) Tone 1 FM/OFF/AM	"OFF"
(51) DISPLAY	"METER"

2. Set external Modulation Meter as follows:

FM - 10 kHz Range
High Pass Filters - 300 Hz
Low Pass Filters - 3 kHz

3. Connect 50Ω coax cable between TRANS/-40 dB DUPLEX Connector (11) and input of external Modulation Meter. Verify residual FM $\leq$ 50 Hz.

4. Rotate MODULATION Control (7) to "FM 2". Verify residual FM $\leq$ 50 Hz.

5. Rotate MODULATION Control (7) to "FM 3". Verify residual FM $\leq$ 50 Hz.

6. Rotate MODULATION Control (7) to "FM 4". Verify residual FM $\leq$ 200 Hz.

STEP	PROCEDURE
7.	Set LCD FREQUENCY (21) to 850.0000 FREQ MHz. Repeat Steps 3 thru 6 using following limits: FM1, FM2, and FM3 $\leq$ 200 Hz residual FM; FM4 $\leq$ 250 Hz residual FM
8.	Disconnect all test equipment from FM/AM-1500.

3-6-2 DUPLEX OFFSET PERFORMANCE TEST

SPECIAL ACCESSORY EQUIPMENT REQ'D:

1 50Ω Coax Cable, BNC to BNC

1 50Ω Termination, BNC

1 Spectrum Analyzer---Capable of measuring -10 dBm at 800 MHz

1 Frequency Counter---Capable of counting 850 MHz

TEST SET-UP DIAGRAM: None

INITIAL FM/AM-1500 CONTROL SETTINGS:

CONTROL	SETTING
(10) RF Output Level	"-10 dBm"
(13) PWR/OFF/BATT	"PWR"
(18) DUPLEX/SIMPLEX	"DUPLEX"
(19) GEN/REC	"GEN"
(21) LCD	800.0000 FREQ MHz

STEP	PROCEDURE
1.	Connect 50Ω coax cable between DUPLEX Output Connector (16) and external Spectrum Analyzer.
2.	Verify level on external Spectrum Analyzer is -10 dBm (±2 dB).
3.	Disconnect 50Ω coax cable from DUPLEX OUTPUT Connector (16) and connect it to TRANS/-40 dB DUPLEX Connector (11).
4.	Connect a 50Ω termination to DUPLEX OUTPUT Connector (16).
5.	Verify dB level on external Spectrum Analyzer is -50 dBm (±3 dB).
6.	Disconnect external Spectrum Analyzer from TRANS/-40 dB DUPLEX Connector (11) and disconnect 50Ω termination from DUPLEX OUTPUT Connector (16).
7.	Connect 50Ω coax cable between DUPLEX OUTPUT Connector (16) and external Frequency Counter input. Set external Frequency Counter resolution to 100 Hz.

STEP	PROCEDURE
8.	Press "OFFSET,1,1,1,1" on KEYBOARD (20) and verify external Frequency Counter reads 811.1100 MHz (± 1 kHz).
9.	Repeat Step 8 for OFFSET of 22.22, 33.33, 44.44 and 49.99 MHz. Verify external Frequency Counter reads 800 MHz + OFFSET value (± 1 kHz).
10.	Press "OFFSET,-,4,9,9,9" on KEYBOARD (20) and verify external Frequency Counter reads 750.0100 MHz (± 1 kHz).
11.	Repeat Step 10 for OFFSET of -44.44, -33.33, -22.22, -11.11, and -00.00 MHz. Verify external Frequency Counter reads 800 MHz - OFFSET value (± 1 kHz).

NOTE

OFFSET will not operate correctly if OFFSET is entered as $\geq$ 50.00 MHz.

12. Disconnect all test equipment from FM/AM-1500.

3-6-3 DUAL TONE GENERATOR PERFORMANCE TEST

SPECIAL ACCESSORY EQUIPMENT REQ'D:

1 50Ω Coax Cable, BNC to BNC

1 BNC Tee

1 Digital Voltmeter---Any

1 150Ω Load; See Appendix D

1 50Ω Coax Cable, BNC to Banana Jacks

1 Frequency Counter---Capable of counting from 6 Hz to 20 kHz

TEST SET-UP DIAGRAM:

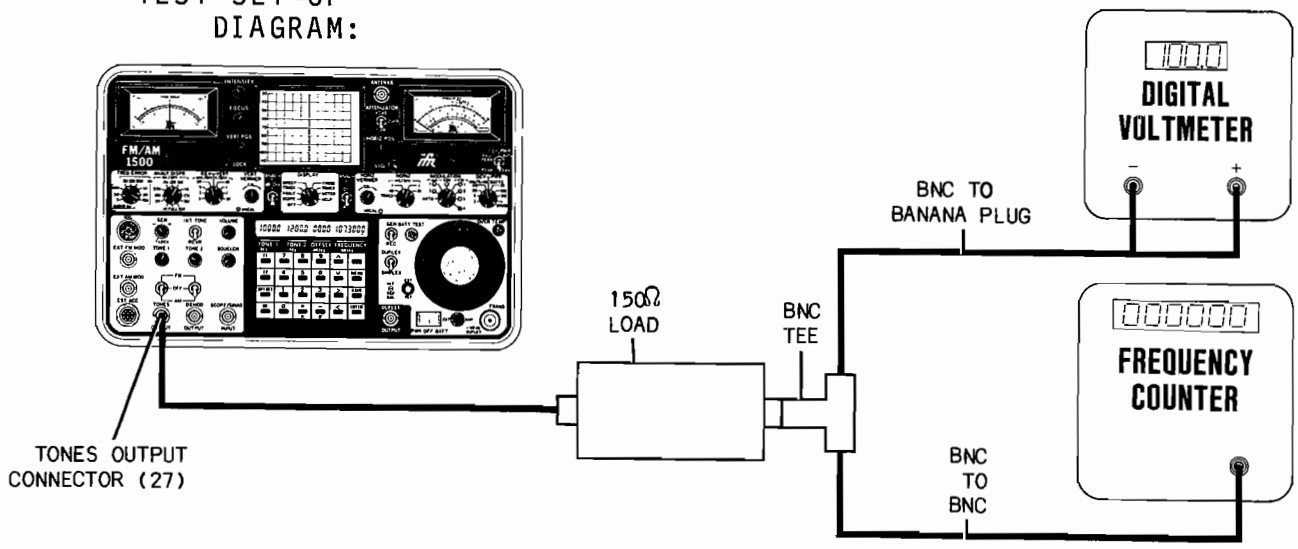


Figure 3-5 Dual Tone Generator Test Set-Up Diagram

INITIAL FM/AM-1500 CONTROL SETTINGS:

CONTROL	SETTING
(5) HORIZ	"10 mS/DIV"
(7) MODULATION	"FM 4"
(13) PWR/OFF/BATT	"PWR"
(21) LCD	0000.1 Hz TONE 1
	0000.1 Hz TONE 2
(22) VOLUME	Fully cw
(31) TONE 2	Fully ccw
(33) TONE 1	Fully ccw
(36) INT TONE/RCVR	"INT TONE"
(39) DEV/VERT	"2 kHz/DIV"
(51) DISPLAY	"SCOPE"

STEP PROCEDURE

AUDIO GENERATORS

1. Connect test equipment to FM/AM-1500 as shown in Figure 3-5.

2. Rotate TONE 1 Control (33) fully cw and verify that low-pitch audio chatter is heard and that CRT (50) displays a stair-step pattern.

3. Repeat Step 2 for TONE 1 Hz settings on LCD (21) of: 0.1, 0.4, 0.8, 1.6 and 3.2 Hz.

4. Rotate DISPLAY Control (51) to "METER".

5. Set TONE 1 Hz on LCD (21) to 6.4 Hz. Verify DVM reads $\geq$ 2.5 VRMS and that Frequency Counter is within 0.01% of TONE 1 Hz setting on LCD (21). Also verify the digital Demod Count meter on the CRT (50) displays the value of the TONE 1 Hz setting (±0.1%).

6. Rotate TONE 1 Control (33) fully ccw and verify that DVM reads approximately 0 VRMS and Frequency Counter reads 0 Hz.

7. Repeat Steps 5 and 6 for TONE 1 Hz settings on LCD (21) of: 12.8, 25.6, 51.2, 409.5, 409.6, 1000.0, 5000, 9999, 13107 and 20000 Hz.

8. Rotate TONE 1 Control (33) fully ccw. Rotate TONE 2 Control (31) fully cw and repeat Steps 2 thru 7, using TONE 2.

9. Disconnect all test equipment from FM/AM-1500.

TONE SWEEP, X-OUT AND DTMF

1. Set FM/AM-1500 controls as follows:

CONTROL	SETTING
(5) HORIZ	"10 mS/DIV"
(13) PWR/OFF/BATT	"PWR"
(19) GEN/REC	"GEN"
(22) VOLUME	Fully ccw
(26) Tone 2 FM/OFF/AM	"OFF"
(28) Tone 1 FM/OFF/AM	"OFF"
(33) TONE 1	Fully cw
(36) INT TONE/RCVR	"INT TONE"
(39) DEV/VERT	"1 V/DIV"
(51) DISPLAY	"TONES"
(52) DC/AC	"DC"

STEP PROCEDURE

2. Depress "MENU" and then "V" until "TONE SWEEP MENU" appears. Depress "MENU, ENTER, >, 1, 0, 0, >, 1, 0, 0, 0, >, >, 1, 0, 0, >, 5, ENTER, EXEC, 2nd, T. SWP., 1, ·, ENTER".

3. Rotate VOLUME Control (22) to a comfortable listening level and verify Tone Sweep operation.

NOTE

A "warbling" sound will be heard if Tone Sweep is operating.

4. Connect 50Ω coax cable between X-OUT Connector (59) and SCOPE/SINAD INPUT Connector (24).

5. Rotate DISPLAY Control (51) to "SCOPE". Verify a "stair-step" display on CRT (50).

6. Depress "RF, ENTER" to stop function. Disconnect coax cable.

7. Rotate TONE 1 Control (33) fully ccw.

8. Depress "EXEC, 2nd, DTMF, 1, ENTER". Verify DTMF ("touch-tone") is heard.

9. Depress "2nd, DTMF". Verify "touch-tone" is heard as each key (0, 1, 2, 3, 4, 5, 6, 7, 8, 9, *, #) is depressed and that frequencies are displayed on LCD (21) for each key selection.

10. Depress "ENTER" to stop function.

11. Disconnect all test equipment from FM/AM-1500.

TONE SEQUENCE

1. Set FM/AM-1500 controls as follows:

CONTROL	SETTING
(4) AVG PEAK/PEAK	"AVG PEAK"
(6) DEV/PWR	"6 kHz"
(7) MODULATION	"FM 2"
(13) PWR/OFF/BATT	"PWR"
(19) GEN/REC	"GEN"
(22) VOLUME	Midrange
(26) Tone 2 FM/OFF/AM	"OFF"
(28) Tone 1 FM/OFF/AM	"OFF"
(38) ANALY DISPR	≤ "1 MHz/DIV"
(51) DISPLAY	"TONES"

STEP	PROCEDURE
2.	On KEYBOARD (20), depress the following keys: "MENU, ENTER, >, 1, 0, 0, 0, >, 5, >, 9, 9, 9, 9, >, 0, >, 0, ENTER".
3.	Rotate Display Control (51) to "METER".
4.	Depress keys: "EXEC, 2nd, T.SEQ., 1, ENTER". Verify both digital and analog meters indicate 5.00 kHz (±5%) deviation.
5.	Rotate MODULATION Control (7) to "AM 2".
6.	Depress following keys: "EXEC, ENTER". Verify both digital and analog meters read beween 42.5% and 57.5% AM modulation.
7.	Disconnect all test equipment from FM/AM-1500.

3-7 SPECTRUM ANALYZER FUNCTIONAL BLOCK

3-7-1 SPECTRUM ANALYZER PERFORMANCE TEST

SPECIAL ACCESSORY EQUIPMENT REQ'D:

1 Signal Generator---Capable of generating -30 dBm at 120.5 MHz

1 50Ω Coax Cable, BNC to BNC

2 20 dB Attenuator Pads

TEST SET-UP DIAGRAM: None

INITIAL FM/AM-1500 CONTROL SETTINGS:

CONTROL	SETTING
(13) PWR/OFF/BATT	"PWR"
(19) GEN/REC	"REC"
(21) LCD FREQUENCY READOUT	120.5000 MHz
(38) ANALY DISPR	"20 kHz/DIV"
(48) dB/DIV	"10 dB/DIV"
(51) DISPLAY	"ANALY"
(55) ATTENUATOR	"0 dB"

STEP PROCEDURE

ANALYZER LEVEL

1. Set Signal Generator to 120.5 MHz at about -40 dBm.

2. Connect 50Ω coax cable between ANTENNA Connector (56) and output of Signal Generator.

3. Adjust output level of Signal Generator so that displayed signal on CRT (50) is exactly on the -40 dB graticule. Note and record output level of Signal Generator.

4. Step output level of Signal Generator in 10 dB steps from -30 dBm to -90 dBm. At each setting, verify displayed signal on CRT (50) is at corresponding graticule (±2 dB).

5. Set Signal Generator output level to -40 dBm. Set ATTENUATOR Switch (55) to "20 dB". Note and record position of signal on CRT (50).

6. Install a calibrated 20 dB pad between Signal Generator output and ANTENNA Connector (56). Set ATTENUATOR Switch (55) to "0 dB". Verify signal is in same position (±2 dB) as recorded in Step 5.

STEP PROCEDURE

7. Remove 20 dB pad. Set ATTENUATOR Switch (55) to "40 dB". Note and record position of signal on CRT (50).

8. Install two calibrated 20 dB pads between Signal Generator output and ANTENNA Connector (56). Set ATTENUATOR Switch (55) to "0 dB". Verify signal is in same position (±2 dB) as noted and recorded in Step 7.

9. Remove all test equipment from FM/AM-1500.

ANALYZER DISPERSION

1. Set FM/AM-1500 controls as follows:

CONTROL	SETTING
(19) GEN/REC	"REC"
(21) LCD FREQUENCY READOUT	120.5000 MHz
(38) ANALY DISPR	"1 kHz/DIV"
(51) DISPLAY	"ANALY"

2. Set Signal Generator to 120.5 MHz at -50 dBm.

3. Connect 50Ω coax cable between ANTENNA Connector (56) and output of Signal Generator.

4. Change Signal Generator frequency, in 1 kHz steps, up 4 kHz from 120.5000 MHz and then down 4 kHz from 120.5000 MHz. Verify signal on CRT (50) moves 4 (±0.3) major divisions in each direction.

5. Rotate ANALY DISPR Control (38) to "2 kHz/DIV". Step Signal Generator frequency, in 1 kHz steps, up 8 kHz from 120.5000 MHz and then down 8 kHz from 120.5000 MHz. Verify signal on CRT (50) moves 4 (±0.3) major divisions in each direction.

6. For all ANALY DISPR Control (38) settings in Table 3-2, vary the limits of the Signal Generator ±4 times ANALY DISPR Control (38) setting. Verify signal dsiplayed on CRT (50) at each ANALY DISPR Control (38) setting that displayed signal on CRT (5) moves 4 (±0.3) major divisions in each direction.

ANALY DISPR SETTING	LIMITS OF SIGNAL GENERATOR (From 120.5000 MHz)
10 K	+40 K, -40 K
20 K	+80 K, -80 K
.1 M	+.4 M, -.4 M
.2 M	+.8 M, -.8 M
.5 M	+2.0 M, -2.0 M
1 M	+4 M, -4 M
2 M	+8 M, -8 M
5 M	+20 M, -20 M
10 M	+40 M, -40 M

Table 3-2 Analyzer Dispersion Test Settings

7. Rotate ANALY DISPR Control (38) to "1 M". Set Signal Generator to 120.5000 MHz. Verify displayed signal on CRT (50) is centered (±1 minor division).

8. Rotate ANALY DISPR Control (38) to "2 M". Verify displayed signal on CRT (50) is centered (±1.5 minor divisions).

9. Set LCD FREQUENCY READOUT (21) to 500.0000 MHz. Rotate ANALY DISPR Control (38) to "FULL". Set external Signal Generator to 990.0000 MHz. Verify displayed signal on CRT (50) is displaced 9.9 (±0.5) major divisions from left side of display.

NOTE

If displayed signal goes off the screen, reduce Signal Generator frequency until signal is on far right of display. Minimum allowable setting of Signal Generator is 980.0000 MHz for a full scale display.

10. Disconnect all test equipment from FM/AM-1500.

TRACK

1. Set FM/AM-1500 controls as follows:

CONTROL	SETTING
(7) MODULATION	"AM 2"
(10) RF Output Level	"-40 dBm"
(13) PWR/OFF/BATT	"PWR"
(18) DUPLEX/SIMPLEX	"SIMPLEX"

STEP PROCEDURE

CONTROL	SETTING
(21) LCD TONE 1 READOUT	0400.0 Hz
FREQUENCY READOUT	120.5000 MHz
(26) Tone 2 FM/OFF/AM	"OFF"
(28) Tone 1 FM/OFF/AM	"AM"
(33) TONE 1	Fully ccw
(38) ANALY DISPR	"1 MHz/DIV"
(48) dB/DIV	"1 dB/DIV"
(51) DISPLAY	"TRACK"

2. Connect 50Ω coax cable between TRANS/-40 dB DUPLEX Connector (11) and ANTENNA Connector (56).

3. Adjust VERT POS Control (45) to display trace on CRT (50). Verify maximum slope of trace is $\leq$ 1.5 dB.

4. Rotate RF Output Level Control (10) to "-46 dBm". Verify trace on CRT moves 6 (±1) major divisions.

5. Set LCD (21) to 500.0000 MHz. Set dB/DIV Switch (48) to "10 dB/DIV". Rotate ANALY DISPR Control (38) to "FULL". Rotate TONE 1 Control (33) fully cw. Verify modulation is up $\geq$ 6 dB and down $\geq$ 20 dB from unmodulated trace across entire bandwidth.

6. Rotate TONE 1 Control (33) fully ccw. Set dB/DIV Switch (48) to "1 dB/DIV". Verify maximum slope is $\leq$ 4 dB for any major division and $\leq$ 6 dB for entire bandwidth.

7. Disconnect all test equipment from FM/AM-1500.

3-8 MICROPROCESSOR FUNCTIONAL BLOCK

3-8-1 FRONT PANEL PERFORMANCE TEST

SPECIAL ACCESSORY EQUIPMENT REQ'D: None

TEST SET-UP DIAGRAM: None

INITIAL FM/AM-1500 CONTROL SETTINGS:

CONTROL	SETTING
(13) PWR/OFF/BATT	"PWR"
(22) VOLUME	Midrange
(23) SQUELCH	Fully ccw

STEP	PROCEDURE
1.	Individually press each key on KEYBOARD (20). Verify an audible tone is generated each time a key is depressed.
2.	Verify Freq LOCK Indicator (43) and SIG Indicator (57) are illuminated.
3.	Verify UNCAL Indicator (Vertical) (42) illuminates as VERT VERNIER Control (44) is rotated ccw out of "CAL".
4.	Verify UNCAL Indicator (Horizontal) (8) illuminates as HORIZ VERNIER Control (3) is rotated ccw out of "CAL".
5.	Verify an indicator illuminates at each setting of MODULATION Control (7) except "AUTO".

NOTE:

One of the lights illuminates at "AUTO", but varies according to menus.

6.	Depress BATT TEST Button (14) and verify internal battery voltage is +11 V to +14 V as indicated on top scale of MODULATION Meter (1).
7.	Rotate DISPLAY Control (51) to "OFF". Verify CRT (50) is not illuminated.
8.	Rotate DISPLAY Control (51) to "HELP". Verify HELP Menus are displayed.

STEP	PROCEDURE

9. Press "MENU,V" sequentially on KEYBOARD (20). Verify LCD Manual Data, Memory Recall, Memory Storage and Self Test Menus are displayed.

10. Select Self Test Menu on CRT (50).

11. Press "EXEC,1,ENTER" on KEYBOARD (20). Verify LCD (21) readout displays as in Figure 3-6.

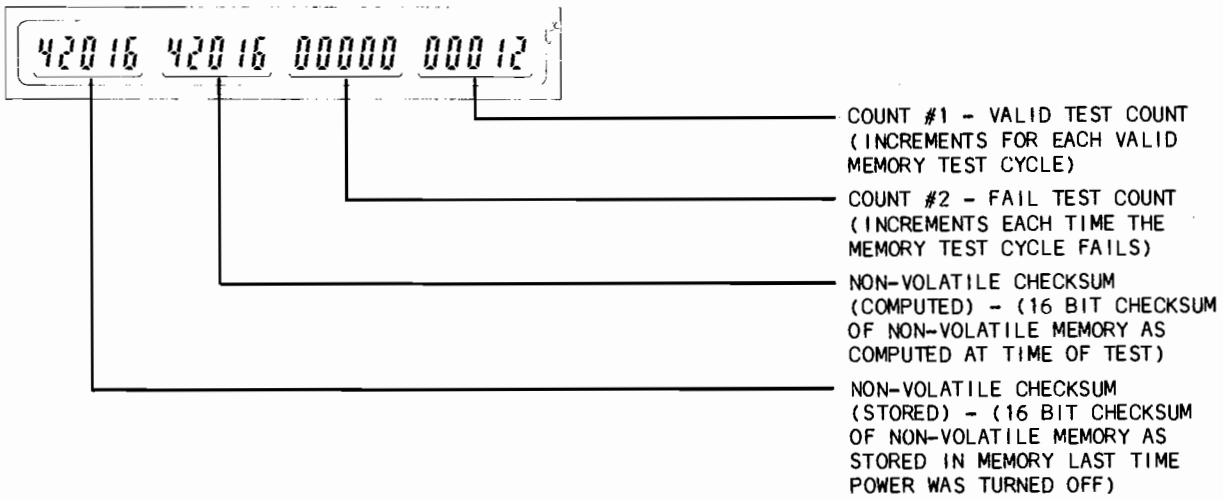


Figure 3-6 LCD Readout on Self Test 1

Press "ENTER" to exit from test.

12. Press "EXEC,2,ENTER" on KEYBOARD (20). Verify CRT (50) characters can be changed by depressing "v" or "^" Keys. Step completely through alphanumeric character set. Press "ENTER" to exit from test.

13. Press "EXEC,3,ENTER". Verify LCD (21) display scrolls from right to left. Press "ENTER" to exit test.

14. Press "EXEC,4,ENTER". Verify the LCD (21) flickers, the Freq LOCK Indicator (43) flashes, the LED's on the MODULATION Control (7) flash and the LCD (21) does not display an error message. Press "ENTER" to exit from test.

15. Press "EXEC,5,ENTER". Verify the cursor is displayed and, if applicable, the last stored menu. Press "ENTER" to exit from test.

STEP	PROCEDURE
16.	Rotate DISPLAY Control (51) to "METER". Verify Meter readout is displayed on CRT (50).
17.	Rotate DISPLAY Control (51) to "TONES". Press "MENU,V" sequentially and verify Tone Sequence, Digitally-Coded Squelch, Tone Sweep and DTMF Menus are displayed on CRT (50).
18.	Rotate DISPLAY Control (51) to "FREQS". Press "MENU,V" sequentially and verify RF Memory, Cable Fault, RF Scan and RF Sweep Menus are displayed on CRT (50).
19.	Rotate DISPLAY Control (51) to "SWEEP". Verify horizontal trace is displayed on major horizontal axis of CRT (50).
20.	Rotate DISPLAY Control (51) to "TRACK". Verify noise pattern is displayed at bottom of CRT (50).
21.	Rotate DISPLAY Control (51) to "ANALY". Verify noise pattern is displayed at bottom of CRT (50).
22.	Rotate DISPLAY Control (51) to "SCOPE". Verify noise pattern centered about the major horizontal axis is displayed on CRT (50) that the pattern changes shape as MODULATION Control (7) is rotated.
23.	Disconnect all test equipment.

3-8-2 DATA ENTRY PERFORMANCE TEST

SPECIAL ACCESSORY
EQUIPMENT REQ'D: Oscilloscope---Capable of measuring 0 to 10 VDC

TEST SET-UP
DIAGRAM: None

INITIAL FM/AM-1500
CONTROL SETTINGS:

CONTROL	SETTING
(7) MODULATION	"AUTO"
(13) PWR/OFF/BATT	"PWR"
(18) DUPLEX/SIMPLEX	"SIMPLEX"
(19) GEN/REC	"REC"
(22) VOLUME	Midrange
(51) DISPLAY	"FREQS"

STEP PROCEDURE

1. Verify IFR logo is dislayed on CRT (50).

2. Press any key. Verify that IFR logo disappears from CRT (50).

3. Verify that data can be entered into LCD (21) as follows:

   a. TONE 1 Hz - Press "T1, XXXXX, ENTER".
   b. TONE 2 Hz - Press "T2, XXXXX, ENTER".
   c. OFFSET MHz - Press "OFFSET, XX.XX, ENTER".
   d. FREQUENCY MHz - Press "RF, XXX.XXXX, ENTER".

4. Set DUPLEX/SIMPLEX Switch (18) to "DUPLEX". Verify OFFSET MHz data is displayed on LCD (21).

5. Set DUPLEX/SIMPLEX Switch (18) to "SIMPLEX". Verify OFFSET MHz is 00.00 on LCD (21).

6. Select RF Memory Menu. Change data for item 1 and execute menu by pressing "EXEC, RF, 1, ENTER". Verify LCD (21) displays new menu entries.

7. Select RF Sweep Menu. Change data in item 1 as follows:

   START FREQ = 100.0000 MHz
   STOP FREQ = 100.2550 MHz
   INCR. STEP = 000.0010 MHz
   INCR. STEP = 10 mS

STEP	PROCEDURE

8. Connect an external Oscilloscope to the X-Out Connector (59) on the rear panel of the FM/AM-1500. Execute the RF Sweep Menu by pressing "EXEC, 2nd, FSWP, 1, ., ENTER". Verify the X-Out signal steps once for each RF step and it sweeps from 0 to 10 Volts.

9. Press "2nd, STEP". Verify one forward step when "^" Key is pressed and one reverse step when "v" Key is pressed.

10. Verify sweep runs forward when ">" Key is pressed and sweep runs in reverse when "<" Key is pressed.

11. Select RF Scan Menu. Set FM/AM-1500 controls as follows:

CONTROL	SETTING
(7) MODULATION	"AUTO"
(19) GEN/REC	"REC"
(23) SQUELCH	Fully ccw

12. Connect an external antenna to ANTENNA Connector (56).

13. Enter data into the RF Scan Menu for different frequencies to be scanned. (Local radio stations are suggested for the frequencies.)

14. Execute RF Scan Menu by pressing "EXEC, 2nd, SCAN, 1-5, ., ENTER". Verify frequency dwell time (as programmed) on each received signal.

15. Rotate SQUELCH Control (23) cw to allow only the strongest signals to break squelch. Verify weak signals are skipped and strong signals still have frequency dwell time (as programmed).

16. Rotate SQUELCH Control (23) fully cw. Verify continuous scan with no frequency dwell time.

17. Press "2nd, STEP". Verify manual control works with the "^", "v", ">" and "<" Keys.

STEP PROCEDURE

18. Rotate DISPLAY Control (51) to "TONES". Select Tone Sequence Menu and enter data as follows:

ITEM (1-99)	TONES	Hz	DEV. kHz	TIME mS
01	T1	00020.0	05.0	5000
	T2	00020.0	05.0	
02	T1	00020.0	00.0	5000
	T2	00100.0	05.0	
03	T1	01000.0	05.0	5000
	T2	00100.0	00.0	
04	T1	01000.0	00.0	5000
	T2	05000.0	05.0	
05	T1	20000.0	05.0	5000
	T2	10000.0	00.0	

19. Set FM/AM-1500 Controls as follows:

CONTROL	SETTING
(4) AVG PEAK/PEAK	"PEAK"
(7) MODULATION	"FM 4"
(19) GEN/REC	"GEN"

20. Execute Tone Sequence Menu by pressing "EXEC, 2nd, TSEQ, 1, -, 5, ENTER". Verify peak deviation on items 1 thru 4 is 5.0 kHz (±250 Hz) and on item 5 is 5.0 kHz (±500 Hz).

21. Rotate MODULATION Control (7) to "AM 2". Verify modulation switches to AM.

22. Press "2nd, STEP". Verify manual control works with the "^", "v", ">" and "<" Keys.

23. Select DTMF Menu. Set FM/AM-1500 Controls as follows:

CONTROL	SETTING
(4) AVG PEAK/PEAK	"PEAK"
(7) MODULATION	"FM 4"
(19) GEN/REC	"GEN"

24. Enter data into DTMF Menu as follows:

MAN. DEV = 5.0 kHz
DTMF MARK = 5000 mS
DTMF SPACE = 10 mS

ITEM	NUMBER	kHz
01	0123456789#*	05.0

STEP	PROCEDURE

25. Execute DTMF Menu by pressing "EXEC, 2nd, DTMF, 1, ENTER". Verify peak deviation is 10 kHz (±500 Hz).

26. Rotate MODULATION Control (7) to "AM 2". Verify modulation switches to AM.

27. Press "2nd, STEP". Verify manual control works with the "∧", "v", ">" and "<" Keys.

28. Press "ENTER, 2nd, DTMF". As each key (0 thru 9, * and #) is pressed, verify audio tone is heard and there is a deviation of 10 kHz (±500 Hz). Press "ENTER" to exit function.

29. Select Tone Sweep Menu. Enter data into menu as follows:

ITEM #01	Hz
START FREQ	00100.0
STOP FREQ	00355.0
INCR STEP (+)	00001.0
INCR RATE (mS)	0010

30. Execute Tone Sweep function by pressing "EXEC, 2nd, TSWP, 1, ., ENTER".

31. Using an external Oscilloscope connected to X-Out Connector (59) on rear panel of FM/AM-1500, verify X-Out signal steps once for each step and it sweeps from 0 to 10 Volts as the menu steps through its function.

32. Change the INCR STEP sign to "X 00002.0". Verify the frequency of the X-Out signal doubles.

33. Press "2nd, STEP". Verify manual control works with the "∧", "v", ">" and "<" Keys.

34. Set FM/AM-1500 Controls as follows:

CONTROL	SETTING
(7) MODULATION	"FM 2"
(19) GEN/REC	"GEN"
(26) Tone 2 FM/OFF/AM	"OFF"
(28) Tone 1 FM/OFF/AM	"OFF"
(37) FREQ ERROR	"3 AUDIO Hz"

STEP	PROCEDURE

35. Select Digitally Coded Squelch Menu and enter data as follows:

GENERATE

ITEM	CODE #	POL	kHz DEV
01	000	NORM	0.7
02	006	NORM	0.7
03	146	NORM	0.7
04	777	NORM	0.7

36. Execute each item by pressing "EXEC, 2nd, DCS, N (where N = 1,2,3 or 4), ENTER". Verify a valid reception code for each item.

37. Change menu's RECEIVE DATA POLARITY to INVT and verify different reception codes for each item.

38. Set GENERATE POL to INVT and verify a valid reception code for each item.

39. Press "2nd, STEP". Verify a STOP code is sent and the reception code fields are blank. Press "ENTER" to restore normal operation.

40. Press "∧" and "v" Keys. Verify no change in the STOP code.

41. Press ">" and "<" Keys. Verify that the selected item code is generated as the key is depressed and that the STOP code is generated as the key is released.

42. Press "ENTER". Verify that the selected item code is generated.

43. Select "RF" Key. Verify that the STOP code is generated about 200 mS before the RF field is entered.

44. Disconnect all test equipment.

SECTION 4 - CALIBRATION

4-1 GENERAL

This section contains calibration procedures for the following assemblies and systems:

These procedures should be performed as a result of one or more of the following conditions:

1. If, during the course of normal operation, the FM/AM-1500 or any major function thereof fails to meet the performance specifications as provided in "SECTION 3 - PERFORMANCE EVALUATION".

2. If a module is found to be defective and requires replacement (see Table 4-1, Module Replacement & Calibration Requirements).

3. If the recommended 12 month calibration interval is due.

4-1-1 SAFETY PRECAUTIONS

As with any piece of electronic equipment, extreme caution should be taken when working on "live" circuits. Certain circuits and/or components within the FM/AM-1500 contain extremely high voltage potentials, CAPABLE OF CAUSING SERIOUS BODILY INJURY OR DEATH (see following WARNINGS)! When performing the calibration procedures in this section be sure to observe the following precautions:

WARNING

THE OSCILLOSCOPE CONTROL AND DEFLECTION PC BOARD AND THE CRT CARRY A VOLTAGE POTENTIAL OF OVER 2000 VDC WHEN THE FM/AM-1500 IS ENERGIZED. DO NOT CONTACT THESE OR ANY ASSOCIATED COMPONENTS DURING TROUBLESHOOTING.

WHEN WORKING WITH "LIVE" CIRCUITS OF HIGH POTENTIAL, KEEP ONE HAND IN POCKET OR BEHIND BACK, TO AVOID SERIOUS SHOCK HAZARD.

REMOVE ALL JEWELRY OR OTHER COSMETIC APPAREL BEFORE PERFORMING ANY CALIBRATION PROCEDURES INVOLVING LIVE CIRCUITS.

USE ONLY INSULATED TROUBLESHOOTING TOOLS WHEN WORKING WITH LIVE CIRCUITS.

FOR ADDED INSULATION, PLACE RUBBER BENCH MAT UNDERNEATH ALL POWERED BENCH EQUIPMENT, AND A RUBBER FLOOR MAT UNDERNEATH TECHNICIAN'S CHAIR.

HEED ALL WARNINGS AND CAUTIONS CONCERNING MAXIMUM VOLTAGES AND POWER INPUTS.

4-1-2 CALIBRATION EQUIPMENT REQUIREMENTS

Appendix E at the rear of this manual contains a comprehensive list of test equipment suitable for performing any of the procedures listed in this manual. Any other equipment meeting the specifications listed in Appendix E may be substituted in place of the recommended models.

NOTE

For certain procedures in this manual, the equipment listed in Appendix E may exceed the minimum required specifications; for this reason, minimum use specifications appear with all calibration procedures, where accessory test equipment is required.

4-1-3 DISASSEMBLY REQUIREMENTS

To perform any of the calibration procedures contained in this section, the exterior case must be removed from the FM/AM-1500. Refer to "SECTION 6 - MECHANICAL ASSEMBLIES/PC BOARDS" for illustrations of case removal or, if required, module disassembly. In the procedures, numbers in parentheses following any adjustable port refers to the designator assigned in Figures 3-1 and 3-2 of this Manual.

IF THIS MODULE IS REPAIRED OR REPLACED / THEN THE FOLLOWING CALIBRATION PROCEDURES MUST BE PERFORMED	PRELIMINARY	POWER SUPPLY	FREQUENCY STANDARD	FREQUENCY SYNTHESIS		RECEIVE					GENERATE			SPECTRUM ANALYZER	MICROPROCESSOR
				HIGH LOOP	LOW LOOP	RECEIVE SIGNAL	O'SCOPE	FREQUENY ERROR	MODULATION	INPUT/OUTPUT POWER	RF POWER	DUPLEX OFFSET	DUAL TONE GENERATOR		
CLOCK DIVIDER	●		●												
CPU / MEMORY PC BD	●			●											
DELAY LINE	●			●											
DEMOD AUDIO PC BD.	●	●				●		●	●	●	●				
DIODE SWITCH	●														
DUAL TONE GENERATOR PC BD	●												●		
DUAL VCO	●			●		●					●				
DUPLEX OFFSET	●											●			
FM GENERATOR	●								●		●				
GENERATE MIXER	●										●			●	
HIGH LOOP	●			●											
HIGH / LOW PASS FILTER	●			●											
I/O INTERFACE PC BD.	●					●					●				
LCD / KEYBOARD	●														
LOW PASS FILTER	●			●											
LOW LOOP	●				●										
LOW LOOP MIXER	●				●										
OSC. CONT. + DEFL. PC BD.	●						●		●						
OUTPUT AMP	●										●				
BUFFER AMP A or B	●			●											
POWER SUPPLY	●	●													
POWER TERMINATION	●										●				
SPECTRUM ANALYZER L.O.	●													●	
SPECTRUM ANALYZER I.F.	●													●	
SPECTRUM ANALYZER R.F.	●													●	
40 V POWER SUPPLY	●	●													
89-90 MHz RECEIVER	●					●									
1300 MHz I.F. GENERATOR	●										●				
1300 MHz I.F. RECEIVER	●					●									

Table 4-1 Module Replacement and Calibration Requirements

4-2 PRELIMINARY CALIBRATION

SPECIAL ACCESSORY EQUIPMENT REQ'D:

1	Small Slotted Screwdriver
1	Ohmmeter

FIGURE REFERENCES: None

TEST SET-UP DIAGRAM: N/A

STEP PROCEDURE

1. Set FM/AM-1500 in the position in which it is operated, to allow meters to be zeroed.

NOTE

The meter must be zeroed after unit is placed in the position it is operated.

2. Set PWR/OFF/BATT Switch (13) to "OFF".

3. Adjust MODULATION Meter Mechanical Zero Adjustment (2) for an indication of "0" on MODULATION Meter (1). Gently tap on Meter faceplate to ensure needle is not sticking and that it settles to "0".

4. Adjust FREQ ERROR Mechanical Zero Adjustment (40) for an indication as close as possible to "0" on FREQ ERROR Meter (41). Gently tap on Meter faceplate to ensure that the needle is not sticking and that it settles to "0".

5. Check all knobs on front panel for the following:

   a. Correct alignment to front panel.
   b. Correct range stops.
   c. Knobs are securely tightened to control shafts.
   d. Knobs are close to front panel, but do not bind.

6. Test resistance on Power Supply as follows:

Pin # of J6003	Function	Minimum Resistance
7 (yellow)	-12 V	200Ω
4 or 5 (orange)	+5 V	155Ω
1 (red)	+12 V	42Ω

NOTE

Ground (-) lead of Ohmmeter for positive voltage test points. Ground (+) lead of Ohmmeter for negative voltage test points.

4-3 POWER SUPPLY CALIBRATION

SPECIAL ACCESSORY EQUIPMENT REQ'D:
- 1 Small Slotted Screwdriver
- 1 DC Voltmeter
- 1 DC Power Supply---Variable from +10.9 V to +12 V

FIGURE REFERENCES:
- Rear Panel/Power Supply Module (Figure 6-8)
- Demod Audio PC Board (Figure 6-21)

TEST SET-UP DIAGRAM: N/A

STEP	PROCEDURE

1. Connect AC line cord to FM/AM-1500.

2. Set PWR/OFF Switch (13) to "PWR".

3. Connect Voltmeter between FL6002 (blue wire) and chassis ground. Verify voltage at FL6002 is +16 VDC (±0.5 V). If not, adjust R5741 on Power Supply PC Board #1.

4. Disconnect battery plug J6005.

NOTE

Through Serial Number 2134 (without cooling fan), both J6005 and J6004 must be disconnected.

5. Connect Battery Load Simulator to J6005.

6. Set PWR/OFF/BATT Switch (13) to "PWR".

7. Adjust load control on Battery Load Simulator for load of 0.3 Amps. Verify voltage on Battery Load Simulator is +14.5 VDC. If not, adjust R5706 on Power Supply PC Board #1 for correct voltage.

8. Depress BATT TEST Button (14) and verify that top scale on MODULATION Meter (1) reads the same as battery voltage in Step 8. If not, adjust R4887 on DEMOD AUDIO PC BOARD.

STEP	PROCEDURE

NOTE

Use an extender card to make adjustment or remove CPU/MEMORY PC Board and use extender ribbon cable.

9. Adjust load control on Battery Load Simulator for load of 1.3 Amps (±0.3). Verify voltage on Battery Load Simulator is 5 Vdc (±2 V). If not, repeat Step 8.

10. Set PWR/OFF/BATT Switch (13) to "OFF".

11. Disconnect Battery Load Simulator from J6005.

12. Set PWR/OFF/BATT Switch (13) to "PWR".

13. Connect Voltmeter between FL6005 (red wire) and chassis ground. Verify +12 Vdc (±0.5 V). If necessary, adjust R4851.

14. Connect Voltmeter between FL6006 (orange wire) and chassis ground. Verify +5.075 Vdc (±0.225 V). If not, return to Step 4.

15. Connect Voltmeter between FL6007 (yellow wire) and chassis ground. Verify -12 Vdc (±0.5 V). If not, return to Step 4.

16. Use Voltmeter to measure output of 40 V Power Supply at pin 3 of P5601. Verify +40.5 VDC (±4.5).

17. Disconnect AC Power cord and connect variable 12 Vdc Supply to EXT ACC connector (29).

18. Verify test set operates from 11 to 12 Vdc. If not, adjust R4919 on DEMOD AUDIO PC Board.

19. Set PWR/OFF/BATT Switch (13) to "OFF" and disconnect variable power supply.

4-4 FREQUENCY STANDARD CALIBRATION

SPECIAL ACCESSORY EQUIPMENT REQ'D:
- 1 Frequency Counter---Capable of reading 10 MHz
- 1 10 MHz Standard---Amplitude of 2 Vp-p
- 1 Oscilloscope---Capable of 10 MHz

FIGURE REFERENCES: Oven Oscillator (Figure 6-12)

TEST SET-UP DIAGRAM: N/A

STEP	PROCEDURE
1.	Set PWR/OFF/BATT Switch (13) to "PWR".
2.	Connect external Frequency Counter to 10 MHz REF Connector (62) on rear of FM/AM-1500. Allow UUT 20 minutes to stabilize.
3.	Adjust INT REF CAL Adjustment (17) cw and ccw while observing Frequency Counter. Verify frequency range of at least 3 Hz (±2 Hz). If out of tolerance, rotate frequency adjust screw on oven oscillator assembly to correct frequency range and leave frequency centered at 10 MHz.
4.	Observe Frequency Counter and adjust INT REF CAL Adjustment (17) for 10 MHz (±2 Hz).
5.	Using external Oscilloscope, connect 10 MHz Standard (WWV is suggested) to external input of Oscilloscope and connect a coax cable between Channel A of Oscilloscope and 10 MHz REF Connector (62) on FM/AM-1500.
6.	Adjust INT REF CAL Adjustment (17) on FM/AM-1500 for 10 MHz (±0.5 Hz) signal on Oscilloscope.
7.	Connect external 10 MHz Standard, with amplitude of 2 Vp-p or greater, to 10 MHz REF Connector (62). Verify EXT Reference Indicator (15) illuminates.
8.	Disconnect all test equipment from FM/AM-1500.

4-5 FREQUENCY SYNTHESIS FUNCTIONAL BLOCK

4-5-1 HIGH LOOP CALIBRATION

SPECIAL ACCESSORY EQUIPMENT REQ'D:

1 Frequency Counter---Capable of reading 1210 MHz

1 Spectrum Analyzer---Capable of measuring 1210 MHz

1 TF-30, Tune Fixture---Refer to Appendix D

1 Digital Multimeter

1 Oscilloscope

FIGURE REFERENCES:

FM/AM-1500 Interconnect (Figure 7-1)

High Loop Module #1 and #2 (Figures 7-12 & 7-13)

High Loop PC Boards 1 & 2 (Figure 6-13)

Dual VCO Module (Figure 6-14)

High/Low-Pass Filter Module (Figure 6-16)

Delay Line Module (Figure 6-17)

TEST SET-UP DIAGRAM:

N/A

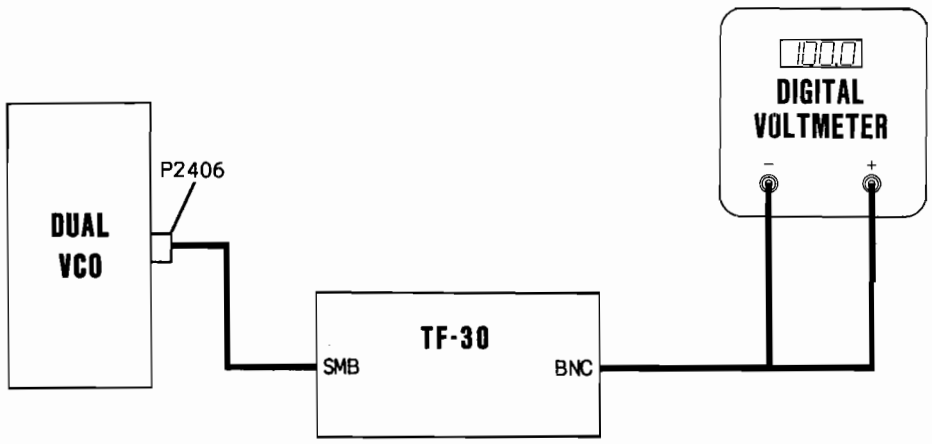


Figure 4-1 TF-30 Tune Fixture Hook-up

STEP	PROCEDURE

1. Place FM/AM-1500 in upright position. Disconnect Ribbon Cable and all coaxes from the HIGH LOOP Module.

2. Remove two screws securing HIGH LOOP Module in module rack and pull out. Reconnect all HIGH LOOP Module connectors.

CAUTION

BE CAREFUL TO INSULATE EXPOSED PC BOARDS FROM POSSIBLE SHORT-CIRCUITING.

3. Rotate ANALY DISPR Control (38) to "1 M".

4. Disconnect P601 and P602 from J601 and J602 on the HIGH/LOW-PASS FILTER Module and connect P601 to P602 using an SMB to SMB connector.

5. Disconnect P3004 from DELAY LINE Module output at J3004. Disconnect P2403 from J2403 on DUAL VCO.

6. Using an SMB to SMB tee, connect an external Frequency Counter to 1210 MHz output, J2402, of the DUAL VCO Module.

7. Set PWR/OFF/BATT Switch (13) to "PWR".

8. Adjust C2003 on DUAL VCO for 1210 MHz (±1 MHz).

NOTE

Dual VCO is a non-repairable module. If out of tolerance, return unit to Factory for repair.

9. Disconnect Frequency Counter.

10. Using external Spectrum Analyzer, verify RF levels of 1210 MHz L.O. at J2402 and J2401 on DUAL VCO are +5 to +12 dBm.

11. Disconnect Spectrum Analyzer and connect P2402 to J2402 and P2401 to J2401.

12. Reconnect external Spectrum Analyzer to verify RF level at OUTPUT BUFFER B (J6902B) is +5 to +12 dBm at 1210 MHz.

13. Disconnect Spectrum Analyzer and reconnect P6902B to J6902B.

STEP	PROCEDURE

14. Reset RF to 299.0000 MHz.

15. Disconnect P2806 from J2806 on HIGH LOOP Module.

16. Connect TF-30 to P2406 on Dual VCO and DVM to BNC connector on TF-30 as illustrated in Figure 4-1.

17. Using an external Frequency Counter and an SMB Tee connector, measure input frequency at J3005 on DELAY LINE Module.

18. Record voltage readings of DVM at listed frequencies.

    a. 50 MHz - _____ Volts
    b. 1120 MHz - _____ Volts

19. Adjust TF-30 for a frequency greater than 390 MHz.

20. Disconnect DVM from TF-30 and connect DVM to center contact of J2806 on HIGH LOOP Module. Adjust R2373 (LOW LIMIT) on Analog HIGH LOOP PC Board (#2) for same voltage recorded in Step 18a.

21. Adjust TF-30 for a frequency on less than 380 MHz. Adjust R2372 (HIGH LIMIT) on Analog HIGH LOOP PC Board (#2) for same voltage recorded in Step 18b.

22. Disconnect TF-30 from P2406 on Dual VCO and connect P2806 to J2806 on HIGH LOOP Module. Connect P2403 to J2403 on Dual VCO. Verify Freq LOCK Indicator (43) on front panel of FM/AM-1500 is illuminated, indicating phase-lock. If not, adjust R2341 (GAIN) on Analog HIGH LOOP PC Board (#2) until phase-lock is achieved.

NOTE

Logic for control of the Freq LOCK Indicator (43) is on the DEMOD AUDIO PC Board as explained in Section 2. If R2341 does not give desired results, the HIGH LOOP Module is not necessarily faulty.

23. Reset RF to 50.0000 MHz. Rotate ANALY DISPR Control (38) to "10 K".

24. Disconnect external Frequency Counter and connect external Spectrum Analyzer in its place.

STEP	PROCEDURE

25. While observing external Spectrum Analyzer, adjust R2341 (GAIN) on Analog HIGH LOOP PC Board (#2) for a flat RF noise floor on each side of 140 MHz display. Note and record level of noise floor (The noise should be flat approximately 20-60 kHz from the center of the band, @ 50 dBc).

26. Reset RF to 999.0000 MHz.

27. Rotate ANALY DISPR Control (38) to "500 K".

28. Observe displayed signal on external Spectrum Analyzer at about 1090 MHz. Adjust R2308 (NULL) on Analog HIGH LOOP PC Board (#2) for lowest RF levels on 500 kHz and 1 MHz sidebands.

29. Observe displayed signal on external Spectrum Analyzer for the following selected frequencies. Verify noise floor level rises no more than 5 dB (±1 dB) above floor level noted in Step 25, on each side of RF signal. Also verify sidebands at 500 kHz and 1 MHz remain nulled.

RF Setting	RF Displayed (on Spectrum Analyzer)
250.0000 MHz	340 MHz
450.0000 MHz	540 MHz
850.0000 MHz	940 MHz

30. Reset RF to 460.0000 MHz.

31. Rotate ANALY DISPR Control (38) to "1 M".

32. Connect a DVM, set to measure DC, to pin 1 of U2315A on Analog HIGH LOOP PC Board (#2).

33. Adjust R2387 on Analog HIGH LOOP PC Board (#2) until voltage on DVM switches from -10 to +10 Vdc as RF is changed from ≥440.0000 MHz to ≤480.0000 MHz.

NOTE

Actual switching point varies dependent on the crossover point of the HIGH/LOW PASS FILTER, which is now disconnected.

34. Disconnect fast tune line coax cable, P2805, from J2805 on HIGH LOOP Module. Verify Freq LOCK Indicator (43) on front panel blinks on and off.

STEP	PROCEDURE

35. Connect fast tune line coax cable, P2805, to J2805 on HIGH LOOP Module.

36. Connect P601 to J601 and P602 to J602 on the HIGH/LOW PASS FILTER Module.

37. Verify displayed signal on external Spectrum Analyzer changes for each of the following frequency settings.

RF Setting	RF Displayed (on Spectrum Analyzer)
000.0000 MHz	90.0000 MHz
111.1111 MHz	191.1111 MHz
222.2222 MHz	311.2222 MHz
333.3333 MHz	423.3333 MHz
444.4444 MHz	534.4444 MHz
555.5555 MHz	645.5555 MHz
666.6666 MHz	756.6666 MHz
777.7777 MHz	867.7777 MHz
888.8888 MHz	978.8888 MHz
999.9999 MHz	1089.9999 MHz

38. Connect coax cable, P3004 to DELAY LINE Module output at J3004. Verify RF noise level 100 kHz on both sides of displayed signal drops ≥5 dB.

39. Disconnect external Spectrum Analyzer from J3005 on DELAY LINE Module and connect P3005 to J3005.

40. Using external Spectrum Analyzer, measure output level at J2405 on DUAL VCO Module. Verify +5 to +12 dBm output level.

41. Disconnect Spectrum Analyzer from J2405 and connect P2405 to J2405.

42. Using external Spectrum Analyzer, measure output level at J2404 on DUAL VCO Module. Verify +5 to +12 dBm output level.

43. Disconnect Spectrum Analyzer from J2404 and connect P2404 to J2404.

44. Using external Spectrum Analyzer, measure output level at J6902A on BUFFER AMP A. Verify +5 to +12 dBm output level.

45. Disconnect Spectrum Analyzer from J6902A and reconnect P6902A to J6902A.

STEP	PROCEDURE

46. Set FM/AM-1500 controls as follows:

CONTROL	SETTING
(20) KEYBOARD	"RF, 10.0000 (MHz)"
(38) ANALY DISPR Control	"2 M"
(51) DISPLAY Control	"ANALY"

47. Connect external Oscilloscope to pin 1 Test Point of U2308A on Analog HIGH LOOP PC Board (#2). Adjust R2359 (ZERO) for 0 Vdc (±1 V) on Oscilloscope.

48. Reset RF to 999.0000 MHz.

49. Adjust R2330 (FREQUENCY) on Analog HIGH LOOP PC Board (#2) for 0 Vdc (±1 V) on Oscilloscope.

50. Repeat Steps 46 thru 49, then go to Step 51.

51. Select the following RF's and verify voltage level on external Oscilloscope is 0 Vdc (±5 V) for each setting.

RF Setting
900.0000 MHz
800.0000 MHz
700.0000 MHz
600.0000 MHz
500.0000 MHz
400.0000 MHz
300.0000 MHz
200.0000 MHz
100.0000 MHz
000.0000 MHz

52. Disconnect all test equipment and re-install all coaxes and modules.

4-5-2 LOW LOOP CALIBRATION

SPECIAL ACCESSORY EQUIPMENT REQ'D: 1 Spectrum Analyzer---Capable of measuring 79.3 MHz

FIGURE REFERENCES: FM/AM-1500 Interconnect (Figure 7-1)

Low Loop Module (Figure 6-19)

Low Loop Mixer Module (Figure 6-20)

Coax Running List (Table 5-1)

Coax Troubleshooting Chart (Table 5-2)

TEST SET-UP DIAGRAM: N/A

STEP PROCEDURE

1. Set PWR/OFF/BATT Switch (13) to "PWR".

2. Set RF to 000.0000 MHz.

3. Using external Spectrum Analyzer, measure output level at J4001 on Low Loop Module. Verify level is -10 to -15 dBm at 9.3 MHz.

4. Verify output frequency as displayed on external Spectrum Analyzer is equal to 9.3000 MHz minus selected RF as follows:

RF Setting	RF Displayed (on Spectrum Analyzer)
XXX.0000 MHz	9.3000 MHz
XXX.1111 MHz	9.1889 MHz
XXX.2222 MHz	9.0778 MHz
XXX.3333 MHz	8.9667 MHz
XXX.4444 MHz	8.8556 MHz
XXX.5555 MHz	8.7445 MHz
XXX.6666 MHz	8.6334 MHz
XXX.7777 MHz	8.5223 MHz
XXX.8888 MHz	8.4112 MHz
XXX.9999 MHz	8.3001 MHz

NOTE

"X" in step 4 is equal to any digit.

5. Disconnect Spectrum Analyzer from J4001 and connect P4001 to J4001 on LOW LOOP Module.

STEP	PROCEDURE
6.	Using external Spectrum Analyzer, measure output level at J1804 on LOW LOOP MIXER Module. Verify level is +4 to +12 dBm at approximately 79.3 MHz.
7.	Disconnect Spectrum Analyzer from J1804 and connect P1804 to J1804 on LOW LOOP MIXER Module.
8.	Using external Spectrum Analyzer, measure output level at J1803 on LOW LOOP MIXER Module. Verify level is +4 to +12 dBm at approximately 79.3 MHz.
9.	Disconnect test equipment and reconnect all coax cables.

4-6 RECEIVER FUNCTIONAL BLOCK

4-6-1 RECEIVER SIGNAL CALIBRATION

SPECIAL ACCESSORY EQUIPMENT REQ'D:

1 Audio Distortion Analyzer---HP8903A

1 Digital Voltmeter---Any

1 RF Generator---Capable of 125.5 MHz at -90 dBm

1 Frequency Counter---Capable of 10 kHz

1 10K Resistor---5%

1 1 µF Tantalum Capacitor---20%

1 Function Generator---Capable of 120 kHz sine wave

1 Oscilloscope---Any

FIGURE REFERENCES: Demod Audio PC Board (Figure 6-25)

I/O Interface PC Board (Figure 6-39)

TEST SET-UP DIAGRAM: N/A

STEP	PROCEDURE

1. Connect Digital Voltmeter (DVM) between pin 24 of J4701 on DEMOD AUDIO PC Board and pin 35 of U4337 on I/O INTERFACE PC Board.

2. Short pin 24 of P4701 to ground and adjust R4350 on I/O INTERFACE PC Board to indicate zero volts on DVM.

3. Remove short between pin 24 of P4701 and ground.

4. Connect DVM between Test Point 1 (TP1) and ground on I/O INTERFACE PC Board. Adjust R4354 on I/O INTERFACE PC Board for +2.0 Vdc on DVM.

5. Set FM/AM-1500 controls as follows:

CONTROL	SETTING
(6) DEV/PWR Control	"20 KHz"
(7) MODULATION Control	"FM2"
(20) KEYBOARD	"RF, 120.2000 (MHz)"
(51) DISPLAY Control	"METER"

STEP	PROCEDURE

6. Connect RF Generator to ANTENNA Connector (56). Set to 120.2 MHz at -30 dBm.

7. Connect DVM to pin 5 of U4733 on DEMOD AUDIO PC Board. Verify +1.6 to +2.5 Vdc.

8. Adjust RF Generator modulation at 1 kHz rate until CRT Meter reads 20 kHz deviation.

9. Adjust R4950 (DEV/MOD METER CAL) on DEMOD AUDIO PC Board for 20 kHz deviation on MODULATION Meter (1).

10. Turn RF Generator modulation off.

11. Rotate DEV/PWR Control (6) to "SIG". Adjust R4840 (SIG STR CAL) on DEMOD AUDIO PC Board for an indicated 99.9% on CRT Meter.

12. Disconnect RF Generator from FM/AM-1500.

13. Rotate MODULATION Control (7) to "SSB".

14. Adjust R4707 (SSB INJECTION LEVEL) on DEMOD AUDIO PC Board until MODULATION Meter (1) starts deflecting to right. At this point, slowly adjust R4707 so not to deflect needle to the right.

NOTE

This adjustment sets AM Detector beat frequency oscillation point when in SSB.

15. Connect RF Generator to ANTENNA Connector (56). Set to 120.2 MHz CW at -30 dBm.

16. Reset RF to 120.2010 MHz and verify 1 kHz demod tone is heard.

17. Connect TONES OUTPUT Connector (27) to the SCOPE/SINAD INPUT Connector (24).

18. Set FM/AM-1500 controls as follows:

CONTROL	SETTING
(6) DEV/PWR Control	"SINAD"
(20) KEYBOARD	"T1, 1000.0 (Hz)"
(31) TONE 2 Control	Fully ccw
(33) TONE 1 Control	Fully cw
(39) DEV/VERT Control	"1 V/DIV"

STEP	PROCEDURE

19. Adjust R4854 (SINAD NULL No. 1) and R4857 (SINAD NULL No. 2) on DEMOD AUDIO PC Board for maximum indication on CRT Meter and MODULATION Meter (1).

NOTE

Maximum SINAD on MODULATION Meter (1) is full scale to left.

20. Rotate DISPLAY Control (51) to "SCOPE". Rotate VERT VERNIER Control (44) for eight major divisions peak to peak.

21. Rotate TONE 1 Control (33) fully ccw. Set T2, using KEYBOARD (20), to 1800 Hz. Rotate TONE 2 Control (31) for 2 major divisions peak to peak.

22. Rotate TONE 1 Control (33) fully cw. Rotate DISPLAY Control (51) to "METER".

23. Adjust R4855 and R4861 (SINAD CAL) on DEMOD AUDIO PC Board until 12 dB SINAD is indicated on CRT Meter and MODULATION Meter (1) indicates 12 dB SINAD (±1 dB).

24. Rotate MODULATION Control (7) to "FM 3". Connect DEMOD OUTPUT Connector (25) to external Oscilloscope.

25. Connect external Frequency Counter to RF Generator FM output connector. Vary modulation rate of RF Generator from 500 Hz to 10 kHz. Verify displayed demod output level on external Oscilloscope remains constant and CRT Meter is within 1 Hz of external Frequency Counter.

26. Adjust CW output of RF Generator from -30 dBm to -50 dBm. Verify receiver of FM/AM-1500 remains quiet.

NOTE

Test Point 1 (TP1) is provided to allow Function Generator, connected in Steps 27 and 28, to be connected directly to unit.

27. Solder a 10 K resistor and a 1 µF tantalum capacitor in series. Connect (+) end of capacitor to pin 2 of U4733 on DEMOD AUDIO PC Board.

28. Connect Function Generator to free end of 10 K resistor. Set to 20 kHz sine wave.

STEP	PROCEDURE
29.	Rotate MODULATION Control (7) to "FM 4".
30.	Connect coax cable from DEMOD OUTPUT Connector (25) to SCOPE/SINAD INPUT Connector (24). Rotate DISPLAY Control (51) to "SCOPE". Adjust output of Function Generator to display signal height four major divisions (two positive, two negative) on CRT (50).
31.	Adjust Function Generator output frequency to 50 kHz. Verify display on CRT (50) is less than 10% smaller than display in Step 30 (less than two minor divisions down from positive peaks).
32.	Adjust Function Generator output frequency to 120 kHz. Verify display on CRT (50) is less than 30% smaller than display in Step 30 (less than six minor divisions down from positive peaks).
33.	Rotate MODULATION Control (7) to "FM 3".
34.	Adjust Function Generator for 10 kHz and adjust output level to display signal height on CRT (50) of four major divisions (two positive, two negative).
35.	Adjust Function Generator output frequency to 15 kHz. Verify display on CRT (50) is less than 10% smaller than display in Step 34 (less than two minor divisions down from positive peaks).
36.	Adjust Function Generator output frequency to 30 kHz. Verify display on CRT (50) is less than 30% smaller than display in Step 34 (less than six minor divisions down from positive peaks).
37.	Rotate MODULATION Control (7) to "FM 2".
38.	Adjust Function Generator for 1 kHz and adjust output level to display signal height of four major divisions (two positive, two negative) on CRT (50).
39.	Adjust Function Generator output frequency to 5 kHz. Verify display on CRT (50) is less than 10% smaller than display in Step 38 (less than two minor divisions down from positive peaks).
40.	Adjust Function Generator output frequency to 10 kHz. Verify display on CRT (50) is less than 20% smaller than display in Step 38 (less than four minor divisions down from positive peaks).

STEP	PROCEDURE

41. Adjust Function Generator output frequency to 15 kHz. Verify display on CRT is less than 30% smaller than display in Step 38 (less than six minor divisions down from positive peaks).

42. Rotate DEV/PWR Control (6) to "120 kHz".

43. Using external Oscilloscope and probe, verify full wave rectified signal with equal peaks is present on pin 7 of U4770 on DEMOD AUDIO PC Board.

44. Disconnect Function Generator from TP1.

45. Connect external RF Generator to ANTENNA Connector (56). Set at 120.2 MHz, -50 dBm with 25 kHz deviation at 1 kHz sine wave rate.

46. Rotate MODULATION Control (7) to "FM 4" and set RF to 120.2000 MHz.

47. Using Distortion Meter, measure distortion out of DEMOD OUTPUT Connector (25). Verify distortion is less than 2%.

48. Rotate MODULATION Control (7) to "FM 1".

49. Reduce deviation on RF Generator until distortion is less than 2%. Verify deviation on RF Generator is ≥5 kHz.

50. Adjust output of RF Generator to 125.5 MHz CW at -90 dBm.

51. Set FM/AM-1500 controls as follows:

CONTROL	SETTING
(6) DEV/PWR Control	"SIG"
(7) MODULATION Control	"FM 1"
(20) KEYBOARD	"RF, 125.5000 (MHz)"
(23) SQUELCH Control	Fully ccw
(51) DISPLAY Control	"METER"

52. Observe METER Display on CRT (50). Adjust input level on RF Generator until METER Display reads "20". Note and record input level of RF Generator.

53. Set RF to 125.5250 MHz.

54. Adjust output level of RF Generator until METER Display on CRT (50) reads "20". Verify output level of RF Generator is ≥ 25 dB above level noted in Step 52.

STEP	PROCEDURE
55.	Set RF to 125.5500 MHz.
56.	Adjust output level of RF Generator until METER Display on CRT (50) reads "20". Verify output level of RF Generator is ≥ 40 dB above level noted in Step 52.
57.	Disconnect all test equipment.

4-6-2 OSCILLOSCOPE CALIBRATION

SPECIAL ACCESSORY EQUIPMENT REQ'D:
- 1 Function Generator---Capable of 1 MHz sine wave and 10 kHz triangle wave
- 1 Power Supply---Variable from 0 to 40 Vdc

FIGURE REFERENCES: Oscilloscope Control and Deflection PC Board (Figure 6-26)

TEST SET-UP DIAGRAM: N/A

STEP PROCEDURE

1. Set FM/AM-1500 Controls as follows:

CONTROL	SETTING
(3) HORIZ VERNIER Control	Fully cw in "CAL"
(13) PWR/OFF/BATT Switch	"OFF"
(44) VERT VERNIER Control	Fully cw in "CAL"
(45) VERT POS Control	Centered
(46) FOCUS Control	Centered
(47) INTENSITY Control	Centered
(51) DISPLAY Control	"OFF"
(54) HORIZ POS Control	Centered

2. Remove Oscilloscope Control and Deflection PC Board, install extender board and connect Oscilloscope Control and Deflection PC Board to extender board.

3. Set FM/AM-1500 Controls as follows:

CONTROL	SETTING
(5) HORIZ Control	".01 ms/DIV"
(13) PWR/OFF/BATT Switch	"PWR"
(39) DEV/VERT Control	"1 V/DIV"
(51) DISPLAY Control	"SCOPE"

Verify Oscilloscope is illuminated.

4. Adjust R9553 (INTENSITY) for desired CRT intensity.

5. Adjust R5182 (FOCUS) for desired CRT focus.

6. Adjust R9565 and R9566 (TRACE ROTATION) until Oscilloscope trace is parallel to CRT horizontal graticules.

7. Rotate DISPLAY Control (51) to "ANALY".

STEP	PROCEDURE

8. Disconnect P5402 from Spectrum Analyzer IF Module and P4603 from Spectrum Analyzer LO Module.

9. Short pins 14 and 15 of J5102 to pin 3 (Gnd) of J5102 on Oscilloscope Control and Deflection PC Board. Verify analyzer sweep disappears from CRT (50).

10. Adjust R9559 (HORIZ CENTER) and R9561 (VERT CENTER) to place dot in center of CRT (50).

11. Remove short between pins 14 and 3 of J5102. Apply +0.800 Vdc to pin 14. Adjust R5188 (VERT GAIN) to position dot on CRT (50) at junction of major vertical graticule and uppermost horizontal graticule.

12. Short pin 14 of J5102 to pin 3 (Gnd) of J5102.

13. Remove short between pins 15 and 3 of J5102. Apply +2.00 Vdc to pin 15 of J5102. Adjust R5193 (HORIZ GAIN) to position dot on CRT at junction of major horizontal graticule and rightmost vertical graticule.

14. Again short pin 15 to pin 3 (Gnd) of J5102.

15. Repeat Steps 9 thru 14 until no further adjustments are required to achieve desired positions of dot on CRT (50), before proceeding to Step 16.

16. Remove shorts between pins 14, 15 and 3 (Gnd) of J5102.

17. Set FM/AM-1500 Controls as follows:

CONTROL	SETTING
(39) DEV/VERT Control	"1 V/DIV"
(51) DISPLAY Control	"SCOPE"
(52) DC/AC Switch	"DC"

18. Adjust VERT POS Control (45) and HORIZ POS Control (54) to center trace on CRT (50). Verify trace is 10.1 major divisions in length, centered on major horizontal axis. Adjust R5119 (SWEEP WIDTH) for correct length of trace.

19. Using external Power Supply and BNC cable, apply +4.00 Vdc to SCOPE/SINAD INPUT Connector (24). Adjust R5126 (EXTERNAL VERT GAIN) until trace is on uppermost major horizontal graticule of CRT.

20. Set DC/AC Switch (52) to "AC". Verify trace on CRT (50) goes to major (center) horizontal axis.

STEP	PROCEDURE
21.	Set DC/AC Switch (52) to "DC". Adjust external Power Supply to +40 Vdc and set DEV/VERT Control (39) to "10 V/DIV". Verify trace on CRT (50) is on uppermost major horizontal graticule.
22.	Set DEV/VERT Control (39) to ".1 V/DIV" and adjust output of external Power Supply to +0.4 Vdc. Verify trace on CRT (50) is on uppermost major horizontal graticule.
23.	Set DEV/VERT Control (39) to ".01 V/DIV" and adjust output of external Power Supply to +0.04 Vdc. Verify trace on CRT (50) is on uppermost major horizontal graticule.
24.	Set DEV/VERT Control (39) to "1 V/DIV" and rotate HORIZ Control (5) to ".1 mS/DIV".
25.	Disconnect external Power Supply from FM/AM-1500.
26.	Using external Function Generator and 50Ω BNC coax cable, inject a 1 kHz sine wave signal into SCOPE/SINAD INPUT Connector (24). Adjust Signal Generator output until trace on CRT (50) is six major divisions peak-to-peak.
27.	Adjust external Function Generator output to 1 MHz sine wave. Verify trace on CRT (50) is 4.2 to 7.8 major divisions in amplitude. If not, adjust C5115.
28.	Adjust external Function Generator output to 1 kHz sine wave. Rotate VERT VERNIER Control (44) ccw to verify UNCAL Indicator (Vertical) (42) illuminates and display does not oscillate.
29.	Repeat Steps 27 and 28 and then rotate VERT VERNIER Control (44) fully cw to "CAL".
30.	Rotate HORIZ VERNIER Control (3) fully ccw to verify display on CRT increases in frequency.
31.	Rotate HORIZ VERNIER Control (3) fully cw to "CAL".
32.	Adjust external Function Generator output to 1 kHz triangle wave. Adjust R5116 (SWEEP RATE) for five major horizontal divisions between positive and negative peaks of display.
33.	Adjust external Function Generator output to 10 kHz triangle wave. Rotate HORIZ Control (5) to ".01 mS/DIV". Verify one complete cycle (±20%) is displayed on CRT (50).

STEP	PROCEDURE
34.	Adjust external Function Generator output to 1 kHz triangle wave. Rotate HORIZ Control (5) to ".1 mS/DIV". Verify one complete cycle (±20%) is displayed on CRT (50).
35.	Adjust external Function Generator output to 100 Hz triangle wave. Rotate HORIZ Control (5) to "1.0 mS/DIV". Verify one complete cycle (±20%) is displayed on CRT (50).
36.	Adjust external Function Generator output to 10 Hz triangle wave. Rotate HORIZ Control (5) to "10 mS/DIV". Verify one complete cycle (±20%) is displayed on CRT (50).
37.	Rotate HORIZ Control (5) to "TONES". Set T1, using KEYBOARD (20) to 10 Hz. Rotate TONE 1 Control (33) cw to verify Lissajous pattern is available on CRT (50).
38.	Rotate DISPLAY Control (51) to "TONES" and adjust R9556 (BRIGHTNESS) to match brightness on CRT (50) in "SCOPE" position.
39.	Observe menu raster size on CRT (50). Adjust R5161 (VERTICAL RASTER) and R5169 (HORIZ RASTER) until display touches the bottom, right side of the CRT.
40.	Observe CRT (50) and adjust R9528 (ASTIGMATISM) for best focus across the screen.
41.	Disconnect Oscilloscope Control and Deflection PC Board from extender board. Remove extender board from FM/AM-1500 and install Oscilloscope Control and Deflection PC Board into FM/AM-1500.
42.	Connect P5402 to Spectrum Analyzer IF Module and P4603 to Spectrum Analyzer LO Module.

4-6-3 FREQUENCY ERROR CALIBRATION

SPECIAL ACCESSORY EQUIPMENT REQ'D:
- 1 RF Generator---Capable of 130 MHz at -110 dBm
- 1 Oscilloscope

FIGURE REFERENCES: Demod Audio PC Board (Figure 6-25)

TEST SET-UP DIAGRAM: N/A

STEP	PROCEDURE

1. Set FM/AM-1500 Controls as follows:

CONTROL	SETTING
(7) MODULATION Control	"FM2"
(19) GEN/REC Switch	"REC"
(20) KEYBOARD	"RF, 10.0000 (MHz)"
(37) FREQ ERROR Control	"300 Hz"

2. Connect BNC/BNC coax between 10 MHz REF Connector (62) and ANTENNA Connector (56). Adjust R4790 (FREQ ERROR ZERO) on DEMOD AUDIO PC Board for a zero indication on FREQ ERROR Meter (41).

3. Set FM/AM-1500 Controls as follows:

CONTROL	SETTING
(20) KEYBOARD	"RF, 10.0100 (MHz)"
(37) FREQ ERROR Control	"10 kHz"

4. Adjust R4838 (FREQ METER CAL) on DEMOD AUDIO PC Board for -1.0 on FREQ ERROR Meter (41).

5. Reset RF to 10.0030 MHz. Rotate FREQ ERROR Control (37) to "3 kHz". Verify FREQ ERROR Meter (41) reads -3.0.

6. Reset RF to 10.0010 MHz. Rotate FREQ ERROR Control (37) to "1 kHz". Verify FREQ ERROR Meter (41) reads -1.0.

7. Reset RF to 10.0003 MHz. Rotate FREQ ERROR Control (37) to "300 Hz". Verify FREQ ERROR Meter (41) reads -3.0.

8. Reset RF to 10.0001 MHz. Rotate FREQ ERROR Control (37) to "300 Hz". Verify FREQ ERROR Meter (41) reads -1.0.

STEP	PROCEDURE

9. Rotate FREQ ERROR Control to "30 Hz". Verify needle on FREQ ERROR Meter (41) is "pegged".

10. Set FM/AM-1500 Controls as follows:

CONTROL	SETTING
(7) MODULATION Control	"AM2"
(20) KEYBOARD	"RF, 120.2000 (MHz)"
(37) FREQ ERROR Control	"10 kHz"

11. Connect external RF Generator set at 120.2 MHz, CW, to ANTENNA Connector (56). Adjust R4798 (AM FLYWHEEL VOLTAGE) on DEMOD AUDIO PC Board until needle on FREQ ERROR Meter (41) is centered.

12. Set external RF Generator to 150% AM.

13. Connect external Oscilloscope to pin 6 of U4717 on DEMOD AUDIO PC Board. Adjust R4744 (AM FLYWHEEL OFFSET) on DEMOD AUDIO PC Board for null signal on external Oscilloscope.

14. Set external RF Generator for CW output.

15. Connect external Oscilloscope to pin 3 of U4717 on DEMOD AUDIO PC Board. Verify approximately +6 V on Oscilloscope. Note voltage.

16. Connect external Oscilloscope to pin 6 of U4717. Adjust R4798 (AM FLYWHEEL VOLTAGE) on DEMOD AUDIO PC Board for same voltage as noted in Step 15.

NOTE

If adjustment of R4798 does not achieve desired voltage, repeat Steps 12 thru 16 until desired voltage level is reached.

17. Set external RF Generator to 150% AM.

18. Connect external Oscilloscope to pin 6 of U4717. Adjust R4744 (AM FLYWHEEL OFFSET) on DEMOD AUDIO PC Board for a null signal on Oscilloscope.

19. Disconnect RF Generator from FM/AM-1500.

STEP	PROCEDURE

20. Set FM/AM-1500 Controls as follows:

CONTROL	SETTING
(7) MODULATION Control	"FM3"
(19) GEN/REC Switch	"REC"
(20) KEYBOARD	"T1, 1000.0 (Hz)"
	"T2, 1000.0 (Hz)"
(26) Tone 2 FM/OFF/AM Switch	"OFF"
(28) Tone 1 FM/OFF/AM Switch	"OFF"
(37) FREQ ERROR Control	"300 AUDIO Hz"
(51) DISPLAY Control	"METER"

21. Adjust TONE 2 Control (31) for a 450 Hz deviation indication on MODULATION Meter (1).

22. Connect an external Oscilloscope to pin 1 of U4738 on DEMOD AUDIO PC Board.

23. Using TONE 2 Control (31), vary deviation on MODULATION Meter (1) from 450 Hz to maximum and back to 450 Hz. Verify AGC level on Oscilloscope is constant over entire range.

24. Reset T1 to 710.0 Hz and T2 to 410.0 Hz. Verify FREQ ERROR Meter (41) reads -3.0 and CRT Meter indicates 410 Hz.

25. Reset T1 to 410.0 Hz and T2 to 710.0 Hz. Verify FREQ ERROR Meter (41) reads +3.0 and CRT Meter indicates 710 Hz.

26. Reset T1 to 409.0 Hz and T2 to 709.0 Hz. Verify FREQ ERROR Meter (41) and CRT Meter DO NOT read +3.0 and 709 Hz, respectively.

27. Rotate FREQ ERROR Control (37) to "300 Hz" and verify CRT Meter reads 709 Hz.

28. Rotate FREQ ERROR Control (37) to "30 AUDIO Hz" and reset T1 to 120.0 Hz and T2 to 150.0 Hz. Verify FREQ ERROR Meter (41) reads +3.0 and CRT Meter reads 150 Hz.

29. Rotate FREQ ERROR Control (37) to "3 AUDIO Hz". Reset T1 to 9997.0 Hz and T2 to 10,000 Hz. Rotate TONE 2 Control (31) for an indication of 1000 Hz deviation on MODULATION Meter (1). Verify FREQ ERROR Meter reads +3.0 and CRT Meter reads 10,000 Hz.

30. Connect external Oscilloscope to pin 9 of P4702 on DEMOD AUDIO PC Board.

STEP	PROCEDURE

31. Set FM/AM-1500 Controls as follows:

CONTROL	SETTING
(7) MODULATION Control	"FM2"
(18) DUPLEX/SIMPLEX Switch	"SIMPLEX"
(19) GEN/REC Switch	"GEN"
(20) KEYBOARD	"T1, 1000.0 (Hz)"

32. Rotate TONE 1 Control (33) to obtain 150 Hz deviation indication on MODULATION Meter (1).

33. Rotate TONE 1 Control (33) slowly until a square wave occurs on external Oscilloscope. Verify deviation indication is ≤450 Hz on MODULATION Meter (1).

34. Set FM/AM-1500 Controls as follows:

CONTROL	SETTING
(7) MODULATION Control	"FM1"
(19) GEN/REC Switch	"REC"
(20) KEYBOARD	"RF, 850.5000 (MHz)"
(23) SQUELCH Control	Fully ccw
(37) FREQ ERROR Control	"300 Hz"

35. Connect external RF Generator to ANTENNA Connector (56). Set RF Generator to 850.5000 MHz at -90 dBm.

36. Observe FREQ ERROR Meter (41) while slowly lowering external RF Generator output. Verify RF Generator output is -101 dBm or less when FREQ ERROR Meter (41) indicates 100 Hz.

37. Disconnect all test equipment.

4-6-4 MODULATION CALIBRATION

SPECIAL ACCESSORY EQUIPMENT REQ'D:
- 1 RF Generator---Capable of 130 MHz at -30 dBm
- 1 Modulation Meter---Capable of reading 15 kHz deviation; selectable filters
- 1 Digital Voltmeter
- 1 Function Generator---Capable of 8 Vp-p

FIGURE REFERENCES: Demod Audio PC Board (Figure 6-25)
Oscilloscope Control and Deflection PC Board (Figure 6-26)
FM Generator Module (Figure 6-27)

TEST SET-UP DIAGRAM: N/A

STEP	PROCEDURE

1. Set FM/AM-1500 controls as follows:

CONTROL	SETTING
(4) AVG PEAK/PEAK Switch	"PEAK"
(6) DEV/PWR Control	"2 kHz"
(7) MODULATION Control	"FM2"
(19) GEN/REC Switch	"REC"
(20) KEYBOARD	"RF, 120.2000 (MHz)"

2. Set Modulation Meter Filters to 300 Hz High-Pass and 15 kHz Low-Pass.

3. Set RF Generator to 120.2 kHz at -30 dBm with 1 kHz deviation rate.

4. Connect RF Generator to a Modulation Meter and adjust level to ±5 kHz deviation at 1 kHz deviation rate on Modulation Meter.

5. Disconnect RF Generator from Modulation Meter and connect output of RF Generator to ANTENNA Connector (56).

6. Connect Digital Voltmeter to DEMOD OUTPUT Connector (25).

7. Adjust R4803 (FM DEMOD LEVEL) on DEMOD AUDIO PC Board to 0.566 VRMS on Digital Voltmeter.

8. Set RF Generator output modulation to CW.

STEP	PROCEDURE

9. Set the following FM/AM-1500 Controls:

CONTROL	SETTING
(6) DEV/PWR Control	"60 kHz"
(7) MODULATION Control	"FM2"

10. Connect Digital Voltmeter to pin 7 of U4785.

11. Adjust R5012 (FM 2 ZERO) on DEMOD AUDIO PC Bd to 0 V on Digital Voltmeter.

12. Connect Digital Voltmeter to pin 1 of U4773.

13. Adjust R4897 (PEAK DETECTOR ZERO) on DEMOD AUDIO PC Board for 0 V on Digital Voltmeter.

14. Set Modulation Meter to 10 kHz Deviation. Set filters to 10 kHz High-pass and 3 kHz Low-pass. Set mode to PK-PK/2 with Automatic tuning.

15. Select -10 dBm CW on RF Generator.

16. Connect RF Generator to Modulation Meter and note Residual FM of the Modulation.

    RESIDUAL FM: _____

17. Set FM/AM-1500 Controls as follows:

CONTROL	SETTING
(4) AVG PEAK/PEAK Switch	"Peak"
(7) MODULATION Control	"FM1"
(39) DEV/VERT Control	"2 kHz/DEV"
(55) ATTENUATOR Switch	"40 dB"

18. Select "Meter" on DISPLAY (51) Control.

19. Verify CRT (50) measures same Residual FM as Modulation Meter (Step 16). Adjust R5009 (FM 1 ZERO) on DEMOD AUDIO PC Board, as needed.

20. Set Modulation Control (7) to "FM 2".

21. Verify Modulation Meter (1) measures same Residual FM as Modulation Meter (Step 16). Adjust R5012 (FM 2 ZERO) on DEMOD AUDIO PC Board, as needed.

STEP	PROCEDURE

22. Set Low-pass filter on Modulation Meter to 15 kHz.

23. Connect RF Generator to Modulation Meter and note Residual FM.

    RESIDUAL FM: _____

24. Set Modulation Control (7) to "FM 3".

25. Connect RF Generator to Antenna Connector (56).

26. Verify CRT (50) measures same Residual FM as Modulation Meter (Step 23). Adjust R5010 (FM 3 ZERO) on DEMOD AUDIO PC Board, as needed.

27. Set Modulation Control (7) to "FM 4".

28. Set Low-pass filter on Modulation Meter to 120 kHz.

29. Connect RF Generator to Modulation Meter and note Residual FM.

    RESIDUAL FM: _____

30. Connect RF Generator to Antenna Connector (56) of the FM/AM-1500.

31. Verify CRT (50) measures same Residual FM as Modulation Meter (Step 29). Adjust R5011 (FM 4 ZERO) on DEMOD AUDIO PC Board, as needed.

32. Set Modulation Meter filters to 300 Hz High-pass and 3 kHz Low-pass.

33. Set FM/AM-1500 controls as follows:

CONTROL	SETTING
(4) AVG PEAK/PEAK Switch	"AVG-PEAK"
(6) DEV/PWR Control	"2 kHz"
(7) MODULATION Control	"FM 2"
(51) DISPLAY Control	"METER"

34. Connect RF Generator to ANTENNA Connector (56) and note Residual FM.

    RESIDUAL FM: _____

STEP	PROCEDURE

35. Set AVG PEAK/PEAK Switch (4) to "PEAK" and note Residual FM.

    RESIDUAL FM: _____

36. Connect RF Generator to Modulation Meter and note Residual FM.

    RESIDUAL FM: _____

37. Adjust RF Generator to 5 kHz at 1 kHz rate of deviation.

    NOTE

    Signal must be adjusted to include Residual FM noted in Step 36 (i.e. 5 kHz + RESIDUAL in Step 36).

38. Connect RF Generator to ANTENNA Connector (56).

39. Set DEV/PWR Control (6) to "6 kHz DEV".

40. Adjust R4913 (PEAK DEV), as needed, to attain 5 kHz on CRT (50) and adjust R4950 (DEV MOD METER) to attain 5 kHz on MODULATION Meter (1).

    NOTE

    Signal must be adjusted to include Residual FM noted in Step 36 (i.e. 5 kHz + RESIDUAL in Step 36).

41. Set AVG PEAK/PEAK Switch (4) to "AVG PEAK".

42. Adjust R4914 (AVG DEV) to 5 kHz Deviation.

    NOTE

    Signal must be adjusted to include Residual FM noted in Step 36 (i.e. 5 kHz + RESIDUAL in Step 36).

43. Repeat Steps 14 through 42, to fine tune modulation, then proceed with Step 44.

44. Set FM/AM-1500 Controls as follows:

CONTROL	SETTING
(5) HORIZ Control	".1 ms/DIV"
(6) DEV/PWR Control	"2 kHz/DIV DEV"
(51) DISPLAY Control	"SCOPE"

STEP	PROCEDURE

45. Adjust R9573 (DEV CAL) on Oscilloscope Control and Deflection PC Board, as needed, to read five divisions peak to peak and center trace peaks on CRT.

46. Set Modulation Meter filters to 300 Hz High-pass and 3 kHz Low-pass.

47. Connect RF Generator to Modulation Meter and note Residual FM.

    RESIDUAL FM: _____

48. Select 1 kHz tone on RF Generator.

49. Adjust FM deviation on RF Generator to 1 kHz (±50 Hz).

NOTE

Signal must be adjusted to include the Residual FM noted in Step 47 (i.e. 1 kHz + RESIDUAL in Step 47).

50. Set FM/AM-1500 controls as follows:

CONTROL	SETTING
(4) AVG PEAK/PEAK Switch	"PEAK/DEV"
(6) DEV/PWR Control	"2 kHz DEV"
(7) MODULATION Control	"FM2"

51. Connect RF Generator to ANTENNA Connector (56).

52. Set Modulation Meter filters to 3 kHz High-pass and 15 kHz Low-pass.

53. Set RF Generator to no modulation at -10 dBm.

54. Connect RF Generator to Modulation Meter and note Residual FM.

    RESIDUAL FM: _____

55. Adjust RF Generator for 2 kHz deviation at 6 kHz rate.

NOTE

Signal must be adjusted to include Residual FM noted in Step 54 (i.e. 2 kHz + RESIDUAL in Step 54).

STEP	PROCEDURE

56. Set FM/AM-1500 Controls as follows:

CONTROL	SETTING
(4) AVG PEAK/PEAK Switch	"PEAK/DEV"
(6) DEV/PWR Control	"6 kHz"

57. Connect RF Generator to ANTENNA Connector (56).

58. Adjust R4768 (6 kHz DEV) on Demod Audio PC Board, as needed, for 2 kHz deviation.

NOTE

Signal must be adjusted to include Residual FM noted in Step 54 (i.e. 2 kHz + RESIDUAL in Step 54).

59. Set Modulation Meter filters to 120 kHz Low-Pass and 3 kHz High-Pass.

60. Set RF Generator modulation to CW.

61. Connect RF Generator to Modulation Meter and note Residual FM

RESIDUAL FM: _____

62. Adjust RF Generator for 8 kHz deviation at 10 kHz rate.

NOTE

Signal must be adjusted to include Residual FM noted in Step 61 (i.e. 8 kHz + RESIDUAL in Step 61).

63. Set FM/AM-1500 controls as follows:

CONTROL	SETTING
(6) DEV/PWR Control	"20 kHz DEV"
(7) MODULATION Control	"FM 3"

64. Connect RF Generator to ANTENNA Connector (56).

65. Adjust R4778 (10 kHz ADJ) on Demod Audio PC Board, as needed, for 8 kHz deviation.

NOTE

This signal must be adjusted to include the Residual FM noted in Step 16.

66. Set FM/AM-1500 controls as follows:

CONTROL	SETTING
(7) MODULATION Control	"FM 2", "FM 3" or "FM 4"
(51) DISPLAY Control	"SCOPE"
(39) DEV/Vert Control	"20 kHz/DIV"

67. Set RF Generator to 60 kHz Deviation at ±0.5 kHz deviation.

68. Connect RF Generator to ANTENNA Connector (56).

69. Verify no clipping of peaks (either positive or negative) on CRT display (50).

70. Set RF Generator output to CW.

71. Set FM/AM-1500 Controls as follows:

CONTROL	SETTING
(4) AVG PEAK/PEAK Switch	"PEAK"
(6) DEV/PWR Control	"2%"
(7) MODULATION Control	"AM 2"
(51) DISPLAY Control	"METER"

72. Adjust R4918 (AM ZERO) on DEMOD AUDIO PC Board to indicate zero on CRT (50) and MODULATION Meter (1).

73. Set RF Generator to 50% AM with 1 kHz tone.

74. Rotate DEV PWR Control (6) to 6%. Set AVG PEAK/PEAK Switch to PEAK. Adjust R4810 (AM% CAL) on DEMOD AUDIO PC Board for 50% on CRT (50) and MODULATION Meter (1).

75. Set FM/AM-1500 Controls as follows:

CONTROL	SETTING
(6) DEV/PWR Control	"20 kHz"
(7) MODULATION Control	"FM2"
(19) GEN/REC Switch	"GEN"
(51) DISPLAY Control	"TONES"

STEP	PROCEDURE

76. Use Keyboard (20) to display TONE SEQUENCE Menu on CRT (50) and enter following data as Item 01:

T1	1000.0	10.0	9000
T2	0000.0	0.0	

Then press "EXEC, 2ND, T.SEQ, 1, ., ENTER".

77. Adjust R3333 in FM Generator Module until CRT (50) reads 10 kHz deviation.

78. Connect microphone to MIC Connector (34). While talking into microphone, adjust R4932 (FM MIKE LEVEL) on DEMOD AUDIO PC Board for maximum 5 kHz deviation on MODULATION Meter (1).

79. Set FM/AM-1500 Controls as follows:

CONTROL	SETTING
(6) DEV/PWR Control	"6%"
(7) MODULATION Control	"AM 2"
(19) GEN/REC Switch	"GEN"

80. Select TONE SEQUENCE Menu on CRT (50) and enter following data as Item 01:

T1	1000.0	5.0	9000
T2	0000.0	0.0	

81. Press "EXEC, 2ND, T.SEQ, 1, ., ENTER"

82. Adjust R4973 (AM % MOD) on DEMOD AUDIO PC Board so MODULATION Meter (1) reads 50% modulation.

83. While keying microphone, adjust R4933 (AM MIKE LEVEL) on DEMOD AUDIO PC Board for maximum 95% AM on MODULATION Meter (1).

84. Rotate MODULATION Control (7) to FM 2.

85. Verify EXT ACC Connector (29) pins as follows (see Figure 3-4):

Pin #	Output/Input	Method
1	+12 V out	Voltage check
2	-12 V out	Voltage check
3	+5 V out	Voltage check
4	Tone Gen out	Signal check
5	Ext FM Mod in	Signal check
6	Tone Key in	Ground to test
7	Mike Key in	Ground to test
8	Demod out	Signal check
9	Power Ground	----------
10	Signal Ground	----------

STEP	PROCEDURE

86. Connect Function Generator into EXT FM MOD Connector (32).

87. Set FM/AM-1500 Controls as follows:

CONTROL	SETTING
(6) DEV/PWR Control	"20 kHz"
(7) MODULATION Control	"FM 2"
(19) GEN/REC Switch	"GEN"
(26) Tone 2 FM/OFF/AM Switch	"OFF"
(28) Tone 1 FM/OFF/AM Switch	"OFF"

88. Adjust Function Generator for 15 kHz deviation on MODULATION Meter (1). Verify output signal of Function Generator is between 4 and 8 Vp-p sine wave.

89. Connect Function Generator to EXT AM MOD Connector (30).

90. Rotate MODULATION Control (7) to AM 1.

91. Adjust Function Generator so 90% AM is indicated on MODULATION Meter (1). Verify Function Generator output is between 2 and 4 Vp-p sine wave.

92. Set FM/AM-1500 Controls as follows:

CONTROL	SETTING
(6) DEV/PWR Control	"6 kHz"
(7) MODULATION Control	"FM 2"
(19) GEN/REC Switch	"GEN"
(37) FREQ ERROR Control	"3 AUDIO Hz"

93. Press "Λ" or "V" key on KEYBOARD (20) until DCS Menu is displayed on CRT (50). Enter data as follows

1 - 4:

01	000	NORM	0.5
02	006	NORM	0.5
03	146	NORM	0.5
04	777	NORM	0.5

94. For each item in Step 93, push:

"EXEC, 2ND, DCS, (ITEM #), ENTER"

Verify valid reception code for each item while speaking into keyed microphone.

95. Disconnect all test equipment.

4-6-5 INPUT/OUTPUT POWER CALIBRATION

SPECIAL ACCESSORY EQUIPMENT REQ'D:
- 1 DC Power Supply---Capable of +1 VDC
- 1 RF Power Source---Capable of 10 W at 850 MHz
- 1 270Ω Resistor---5%

FIGURE REFERENCES: Demod Audio PC Board (Figure 6-25)

Power Termination Module (Figure 6-33)

TEST SET-UP DIAGRAM: N/A

STEP	PROCEDURE

1. Set FM/AM-1500 Controls as follows:

CONTROL	SETTING
(6) DEV/PWR Control	"15 WATTS"
(19) GEN/REC Switch	"GEN"
(20) KEYBOARD	"RF, 150.0 (MHz)"
(22) VOLUME Control	Fully cw
(31) TONE 2 Control	Fully ccw
(33) TONE 1 Control	Fully ccw

2. Using external Power Supply, apply +1 Vdc to FL9804 on Power Termination Module. Verify speaker output changes from no output to noise.

3. Disconnect external Power Supply from Power Termination Module.

4. Adjust MODULATION Meter (1) at PWR ZERO ADJ (R4871) to indicate zero watts on DEMOD AUDIO PC Board.

5. Using external RF Power Source, apply 10 watts RF power at 120.2 MHz to TRANS/-40 dB DUPLEX Connector (11). Adjust R4904 (15 W) on DEMOD AUDIO PC Board for following readings:

   a. CRT power meter reads 10 watts. Note level.

   b. MODULATION Meter (1) reads 9 to 11 watts. Note level.

   c. When DISPLAY Control (51) is rotated to "ANALY", the display indicates -40 to -50 dBm.

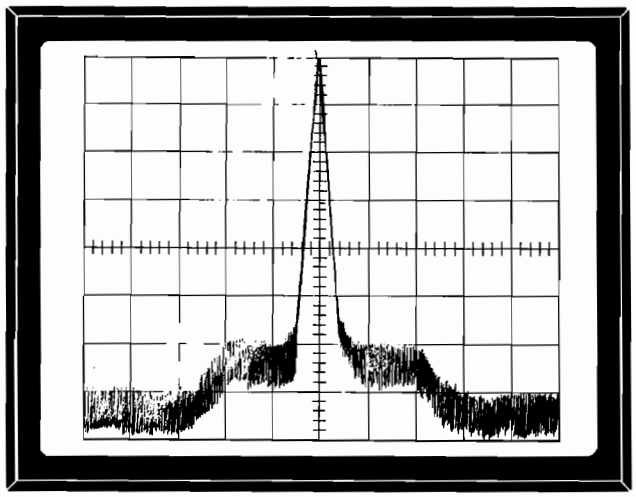


Figure 4-2 RF Output Display

6. Rotate DEV/PWR Control (6) to "150 WATTS". Adjust R4881 (150 W) on DEMOD AUDIO PC Board for following readings:

   a. CRT power meter reads 50 watts.

   b. MODULATION Meter (1) reads between 47 and 53 watts.

7. Set RF Power Source to 10 watts at 850 MHz to the TRANS/-40 DUPLEX Connector (11).

8. Rotate DEV/PWR Control (6) to "15 WATTS". Verify the following readings:

   a. CRT power meter reads within 0.5 watt of reading in Step 5.a.

   b. MODULATION Meter (1) reads within 0.5 watt of reading in Step 5.b.

9. Set RF Power Source to 0 watt at 850 MHz. Slowly increase RF Power Source and verify FM/AM-1500 switches from Generate mode to Receive mode at approximately 100 mW.

10. Connect 270Ω resistor between FL9802 on POWER TERMINATION Module and ground. Verify OVERTEMP Indicator (9) on front panel is illuminated.

11. Disconnect all test equipment.

4-7 GENERATOR FUNCTIONAL BLOCK

4-7-1 RF OUTPUT POWER CALIBRATION

SPECIAL ACCESSORY

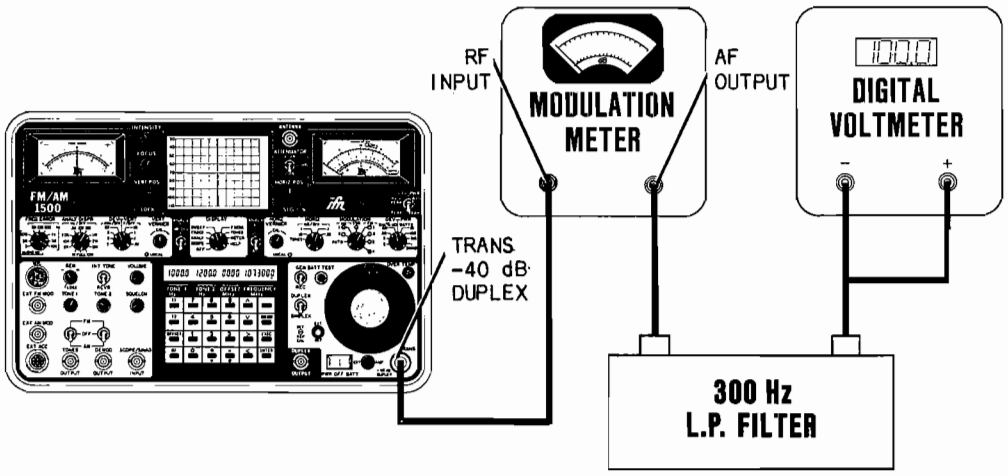


Figure 4-3 Residual FM Test Hookup

EQUIPMENT REQ'D:
- 1 Digital Voltmeter
- 1 Spectrum Analyzer---Capable of measuring 1000 MHz
- 1 Power Meter---Capable of reading -30 dBm
- 1 Modulation Meter---Capable of reading 3.3 kHz deviation at 1000 MHz input
- 1 Oscilloscope
- 300 Hz Low-Pass Filter---See Appendix D

FIGURE REFERENCES:
- FM Generator Module (Figure 6-27)
- Demod Audio PC Board (Figure 6-25)
- Generator Mixer Module (Figure 6-28)
- I/O Interface PC Board (Figure 6-39)

TEST SET-UP DIAGRAM: N/A

STEP	PROCEDURE

1. Set PWR/OFF/BATT Switch (13) to "PWR".

2. Connect DVM to EXT AMP Connector (12). Verify +11 to +12 Vdc present only when GEN/REC Switch (19) is in "GEN" or DISPLAY Control (51) is in "TRACK" or "SWEEP" position.

3. Set FM/AM-1500 Controls as follows:

CONTROL	SETTING
(10) RF Output Level Control	"-30 dBm"
(18) DUPLEX/SIMPLEX Switch	"SIMPLEX"
(19) GEN/REC Switch	"GEN"
(20) KEYBOARD	"RF, 500.0000 (MHz)"
(31) TONE 2 Control	Fully ccw
(33) TONE 1 Control	Fully ccw
(51) DISPLAY Control	Anywhere but on "TRACK" or "SWEEP"

4. Using external Spectrum Analyzer, measure RF output at J4206 on FM Generator Module. Verify output is -13 (+5, -6 dBm) at 68.6 MHz.

5. Using external Spectrum Analyzer, measure RF output at J4403 on Generator Mixer Module. Adjust R3412 (F1 FIXED) and R3423 (F2 FIXED) in Generator Mixer Module to peak display. Adjust R3436 (OUTPUT LEVEL) in Generator Mixer Module to set output level for -13 dBm (±1 dB) at 90 MHz.

6. Connect Power Meter to TRANS/-40 dB DUPLEX Connector (11). Adjust R4963 (RF LEVEL) on DEMOD AUDIO PC Board for -30 dBm (±2.0 dB) on Power Meter.

7. Repeat Step 6 for following frequencies:

100 kHz	400 MHz
10 MHz	500 MHz
50 MHz	600 MHz
100 MHz	700 MHz
200 MHz	800 MHz
300 MHz	900 MHz

8. Disconnect Power Meter and connect external Spectrum Analyzer to, TRANS/-40 dB DUPLEX Connector (11). Set external Spectrum Analyzer to 1 MHz/DIV dispersion, 300 kHz bandwidth and 10 dB/DIV.

9. Use KEYBOARD (20) to step FREQUENCY readings displayed on LCD (21) as follows:

1 MHz Steps	10 MHz Steps
0 - 50 MHz	50 - 88 MHz
88 - 176 MHz	177 - 407 MHz
407 - 500 MHz	500 - 850 MHz
850 - 950 MHz	950 - 999 MHz

Verify at each step:

a. Spectrum is rounded 2 MHz on each side of carrier and does not break into oscillations (refer to Figure 4-2).

b. Spectrum between 1 MHz and 1.8 MHz on each side of carrier is flat ±3 dB.

c. Delay line locks on each frequency - i.e. no excessive noise on Spectrum Analyzer.

10. Observe Spectrum Analyzer at the following frequencies:

30.2 MHz
175.2 MHz
450.2 MHz
850.2 MHz

Verify spectrum 100 kHz on each side of carrier is ≤-65 dBc.

11. Set FM/AM-1500 Controls as follows:

CONTROL	SETTING
(10) RF Output Level Control	"-10 dBm"
(18) DUPLEX/SIMPLEX Switch	"DUPLEX"
(20) KEYBOARD	"RF, 850.2000 (MHz)"

12. Using external Spectrum Analyzer, measure RF output at DUPLEX OUTPUT Connector (16). Verify level is -10 dBm (±2 dB). Disconnect coax to DUPLEX OUTPUT Connector (16).

13. Connect 50Ω Termination to DUPLEX OUTPUT Connector (16). Using external Spectrum Analyzer, measure RF output level at TRANS/-40 dB DUPLEX Connector (11). Verify output level is -50 dBm (±3 dB).

14. Repeat Steps 12 and 13 at 120.2000 MHz.

STEP	PROCEDURE

15. Connect Modulation Meter, 300 Hz Low-pass Filter and Digital Voltmeter to FM/AM-1500 as shown in Figure 4-3. Set Modulation Meter filters to 30 Hz High-pass and 3 kHz Low-pass.

16. Set FM/AM-1500 Controls as follows:

CONTROL	SETTING
(20) KEYBOARD	"T1, 120.2 (Hz)"
(28) Tone 1 FM/OFF/AM Switch	"AM"
(51) DISPLAY Control	"METER"

17. Adjust TONE 1 Control (33) for 10 kHz deviation.

18. Record VRMS reading on DVM as A.

19. Adjust TONE 1 Control fully ccw.

20. Record VRMS reading on DVM as B.

21. Calculate residual FM as follows:

    10 kHz/A = X/B (X = residual FM)

    Verify residual FM < 50 Hz.

22. Set Modulation Meter to 300 Hz High-pass and 3 kHz Low-pass. Disconnect 300 Hz Low-pass filter and connect DVM to AF Output of Modulation Meter.

23. Reset T1 to 1000.0 Hz. Adjust TONE 1 Control (33) for 3.3 kHz (±10 Hz) deviation.

24. Measure VRMS at Modulation Meter AF Output for following RF settings: 100.2 MHz, 850.2 MHz and 999 MHz. Record reading at each setting as A.

25. Adjust TONE 1 Control fully ccw. Record reading at 100.2 MHz, 850.2 MHz and 999 MHz as B. Calculate dB ratio for each setting as follows:

    Ratio = 20 * log (A/B)
    Verify ratio is ≥40 dB for each setting.

NOTE

If DVM has a Relative button, it may be used to give dB reading at each step.

STEP	PROCEDURE

26. Connect external Spectrum Analyzer to DUPLEX OUTPUT Connector (16).

27. Set RF to 0.1000 MHz. Verify second harmonic (±200 kHz)is ≤25 dB

28. Reset RF to 450.2000 MHz. Verify the following:

    a. Second harmonic (900.4 MHz) is ≤-25 dBc.

    b. Non-harmonics at 540.2 MHz and 850.4 MHz ≤-40 dBc. All other signals are ≤-60 dBc.

    c. Noise 20 kHz from 450.2000 MHz is ≤-55 dBc on 3 kHz bandwidth

29. Select 90.2000 thru 990.2000 MHz in 100 MHz steps. Verify:

    a. Second harmonics are ≤-25 dBc.

    b. All non-harmonics are ≤-40 dBc.

30. Set FM/AM-1500 Controls as follows:

CONTROL	SETTING
(18) DUPLEX/SIMPLEX Switch	"SIMPLEX"
(19) GEN/REC Switch	"GEN"
(20) KEYBOARD	"RF, 850.2000 (MHz)"

31. Connect external Spectrum Analyzer to TRANS/-40 dB DUPLEX Connector (11).

32. Rotate RF Output Level Control (10) from -10 dBm to -80 dBm. Verify output level is equal to RF Output Level Control setting (±2 dB) across the range.

33. Rotate RF Output Level Control (10) from -80 dBm to -127 dBm. Verify output level is equal to RF Output Level Control setting (±2.5 dB) across the range.

34. Rotate RF Output Level Control (10) to -30 dBm.

35. Select RF SWEEP Menu on CRT. Enter following data:

Start	0.1 MHz
Stop	990.1 MHz
Inc STEP	10.0 MHz
Inc RATE	1000 ms

Then press: "EXEC, 2nd, F.SWP, 1, ENTER, 2nd, STEP". Press "V" Key until 0.1 MHz (beginning) is reached.

STEP	PROCEDURE

36. Connect Oscilloscope and Voltmeter, with BNC Tee, to X-OUT Connector (59). Verify 0 Vdc. If necessary, adjust R4333 on I/O Interface PC Board.

37. Press: "EXEC, ENTER".

38. Observe RF SWEEP signal on external Spectrum Analyzer as it steps up each 10 MHz. Verify High Loop locks on each frequency, with no oscillations.

39. Observe Oscilloscope and verify voltage changes with each INC STEP of menu.

40. Observe Voltmeter when FREQ SWEEP Menu finishes sweeping. Verify voltage is +10 Vdc. If necessary, adjust R4331 on I/O INTERFACE PC Board.

41. Set FM/AM-1500 Controls as follows:

CONTROL	SETTING
(18) DUPLEX/SIMPLEX Switch	"DUPLEX"
(19) GEN/REC Switch	"GEN"
(20) KEYBOARD	"RF, 860.2000 (MHz)"

42. Connect external Spectrum Analyzer to DUPLEX OUTPUT Connector (16). Set Spectrum Analyzer center frequency to 10 MHz/DIV at 860.4 MHz.

43. Use KEYBOARD (20) to select OFFSET of +45 MHz and -45 MHz. While rotating RF Level Output Control (10) from -10 to -80 dBm, verify the following:

    a. RF output level on Spectrum Analyzer is ±2 dB of RF Output Level across the range.

    b. Spurious signals with -45 MHz OFFSET applied are ≤-60 dBc within +35 MHz to +55 MHz of carrier.

    c. Spurious signals with +45 MHz OFFSET applied are ≤-40 dBc within -35 MHz to -55 MHz of carrier.

4-7-2 DUPLEX OFFSET CALIBRATION

SPECIAL ACCESSORY EQUIPMENT REQ'D: 1 Spectrum Analyzer---Capable of measuring 230 MHz at -4 dBm

FIGURE REFERENCES: FM/AM-1500 Interconnect (Figure 7-1)

DUPLEX OFFSET Module (Figure 6-30)

TEST SET-UP DIAGRAM: N/A

STEP	PROCEDURE

1. Set FM/AM-1500 Controls as follows:

CONTROL	SETTING
(13) PWR/OFF/BATT Switch	"PWR"
(18) DUPLEX/SIMPLEX Switch	"DUPLEX"
(19) GEN/REC Switch	"GEN"
(20) KEYBOARD	"OFFSET, 00.00 (MHz)"

2. Using external Spectrum Analyzer and SMB to SMB tee, measure output level at J3201 on DUPLEX OFFSET Module. Verify level is -8 to 0 dBm at 180 MHz. Note level.

3. Observe external Spectrum Analyzer, and verify all keypad digits from 00.00 to 49.99 operate in both plus and minus, and output frequency steps from +49.99 MHz to -49.99 MHz on either side of 180 MHz as follows:

OFFSET Frequency Settings	RF Displayed (on Spectrum Analyzer)
-49.99 MHz	229.99 MHz
-48.88 MHz	228.88 MHz
-47.77 MHz	227.77 MHz
-46.66 MHz	226.66 MHz
-45.55 MHz	225.55 MHz
-44.44 MHz	224.44 MHz
-33.33 MHz	213.33 MHz
-22.22 MHz	202.22 MHz
-11.11 MHz	191.11 MHz
00.00 MHz	180.00 MHz
+11.11 MHz	168.89 MHz
+22.22 MHz	157.78 MHz
+33.33 MHz	146.67 MHz
+44.44 MHz	135.56 MHz
+45.55 MHz	134.45 MHz
+46.66 MHz	133.34 MHz
+47.77 MHz	132.23 MHz
+48.88 MHz	131.12 MHz
+49.99 MHz	130.01 MHz

STEP	PROCEDURE
4.	Set GEN/REC Switch (19) to "REC".
5.	Observe displayed signal on external Spectrum Analyzer. Verify RF level is ≥50 dB below level noted in Step 2.
6.	Disconnect all test equipment and reconnect all removed coax cables.

4-7-3 DUAL TONE GENERATOR CALIBRATION

SPECIAL ACCESSORY EQUIPMENT REQ'D:
- 1 Oscilloscope
- 1 Distortion Analyzer---Capable of measuring distortion at 20 kHz
- 1 150Ω, 1/4 W Resistor
- 1 Frequency Counter---Capable of reading 66 kHz

FIGURE REFERENCES: Dual Tone Generator PC Board (Figure 6-34)

TEST SET-UP DIAGRAM: N/A

STEP	PROCEDURE

1. Set FM/AM-1500 controls as follows:

CONTROL	SETTING
(13) PWR/OFF/BATT Switch	"PWR"
(20) KEYBOARD	"T1, 1000.0 (Hz)"
(31) TONE 2 Control	Fully ccw
(33) TONE 1 Control	Fully cw

2. Load TONES OUTPUT Connector (27) with 150 Ω, 1/4 W Resistor.

NOTE

Make connector box for Resistor and put BNC tee on the output as shown in Appendix D.

3. Connect external Oscilloscope to one side of BNC tee.
4. Connect external Distortion Analyzer to other side of BNC tee.
5. Verify sine wave output level is ≥7.1 Vp-p.
6. Verify audio distortion is ≥0.7% at 100 Hz.
7. Set T1 to 10000.0 Hz.
8. Disconnect Oscilloscope and connect Frequency Counter in its place. Verify output frequency is 10,000 Hz (±1 Hz). If not, adjust trimcap C4505 on DUAL TONE GENERATOR PC Board.
9. Set T1 to 2000.0 Hz.
10. Verify audio distortion is within 0.7% at 20,000 Hz.

STEP	PROCEDURE

11. Set T1 to 50.0 Hz.

12. Verify audio distortion is <2% at 10 Hz.

13. Repeat step 12 at T2 of 100 Hz.

14. Set FM/AM-1500 controls as follows:

CONTROL	SETTING
(20) KEYBOARD	"T2, 10.0 (Hz)"
(31) TONE 2 Control	Fully cw
(33) TONE 1 Control	Fully ccw

15. Verify audio distortion is <2% at 10 Hz.

16. Repeat step 15 at T2 of 100 Hz.

17. Set T2 to 20000.0 Hz.

18. Verify audio distortion is <0.7% at 20,000 Hz.

19. Set T2 to 1000.0 Hz.

20. Verify audio distortion is <0.7% at 1000 Hz.

21. Select the following frequencies. Verify output frequency is equal (±0.1 Hz) to selected frequency.

TONE 2 Frequency	
409.6 Hz	416.0 Hz
409.7 Hz	422.4 Hz
409.9 Hz	435.2 Hz
410.0 Hz	460.8 Hz
410.4 Hz	512.0 Hz
411.2 Hz	614.4 Hz
412.8 Hz	

22. Select the following frequencies. Verify output frequency is equal (±0.01%) to selected frequency.

TONE 2 Frequency	
2048 Hz	16384 Hz
4096 Hz	32768 Hz
8192 Hz	65536 Hz

23. Rotate TONE 1 Control (33) fully cw and rotate TONE 2 Control (31) fully ccw.

STEP	PROCEDURE

24. Select the following frequencies and verify output frequency is equal (±0.01%) to selected frequency.

TONE 1 Frequency	
2048 Hz	16384 Hz
4096 Hz	32768 Hz
8192 Hz	65536 Hz

25. Select the following frequencies and verify output frequency is equal (±0.1 Hz) to selected frequency.

TONE 1 Frequency	
409.6 Hz	416.0 Hz
409.7 Hz	422.4 Hz
409.9 Hz	435.2 Hz
410.0 Hz	460.8 Hz
410.4 Hz	512.0 Hz
411.2 Hz	614.4 Hz
412.8 Hz	

26. Disconnect all test equipment.

4-8 SPECTRUM ANALYZER FUNCTIONAL BLOCK

4-8-1 SPECTRUM ANALYZER CALIBRATION

SPECIAL ACCESSORY EQUIPMENT REQ'D:
1 Spectrum Analyzer---Capable of measuring 500 MHz at -30 dBm

1 RF Generator---Capable of generating 1000 MHz at -30 dBm

FIGURE REFERENCES:
FM/AM-1500 Interconnect (Figure 7-1)

Spectrum Analyzer LO Module (Figure 6-36)

Spectrum Analyzer IF Module (Figure 6-35)

Generator Mixer Module (Figure 6-28)

Spectrum Analyzer RF Module (Figure 6-37)

89-90 MHz Receiver Module (Figure 6-24)

Mixer Null Module (Figure 6-22)

TEST SET-UP DIAGRAM: N/A

STEP	PROCEDURE

1. Set FM/AM-1500 Controls as follows:

CONTROL	SETTING
(19) GEN/REC Switch	"REC"
(20) KEYBOARD	"RF, 120.2000 (MHz)"
(38) ANALY DISPR Control	"1 M"
(48) dB/DIV Switch	"10 dB/DIV"
(49) ANAL V Adjustment	Center pot
(51) DISPLAY Control	"ANALY"
(53) ANAL H Adjustment	Center pot

2. Using external Oscilloscope, observe voltage on pin 5 of J4603 on LO Module. Adjust ANAL H Adjustment (53) on front panel for ±0.3 Vdc from ground.

3. Observe base line sweep on CRT(50). Adjust R3560 (HORIZ GAIN) on Spectrum Analyzer LO Module until sweep ends 5.2 major divisions left of the major vertical axis.

STEP	PROCEDURE

4. Adjust R3547 (SYMMETRY) on Spectrum Analyzer LO Module to center trace on major vertical axis.

5. Repeat Steps 3 and 4 until no further adjustment is necessary.

6. Connect RF Generator set at 1000 MHz, -30 dBm, to ANTENNA Connector (56).

7. Reset RF to 500.0000 MHz and rotate ANALY DISPR Control (38) to "FULL".

8. Verify 1000 MHz signal is five major divisions right of the major vertical axis and 0 MHz signal is five major divisions (-1, +1.5 minor divisions) left of the major vertical axis. Adjust R3601 (WIDE DISPR) on Spectrum Analyzer LO Module for correct location of 1000 MHz signal.

NOTE

If R3601 is adjusted, repeat Steps 2 thru 5 to readjust centering and symmetry.

9. Set output frequency of RF Generator to 500.2 MHz at -30 dBm.

10. Rotate ANALY DISPR Control (38) to "10 M". Reset RF to 510.2000 MHz. Verify signal is 1 major division (±1 minor division) left of the major vertical axis.

11. Rotate ANALY DISPR Control (38) to "5 M". Reset RF to 505.2000 MHz. Verify signal is 1 major division (±1 minor division) left of the major vertical axis.

12. Rotate ANALY DISPR Control (38) to "2 M". For the following frequencies, verify signal is ±1.5 minor divisions of the major vertical axis.

RF Settings	RF Generator Settings
999.9999 MHz	1000 MHz
700.0000 MHz	700 MHz
000.0000 MHz	No RF

13. Reset RF to 500.2000 MHz. Set RF Generator to 500.2000 MHz at -40 dBm. Rotate ANALY DISPR Control (38) to "1 M". Adjust R3529 (FREQ CENTER) on LO Module until signal is centered on the vertical axis.

STEP	PROCEDURE

14. Set RF Generator to 497 MHz, then to 503 MHz. Verify signal is centered on third major division left and third major division right of the major vertical axis. Adjust R3567 (NARROW DISPERSION) on LO Module for proper centering.

15. For the following RF Generator frequencies and ANALY DISPR Control settings, verify signal is centered on the third major division left and third major division right of the major vertical axis.

ANALY DISPR (38) Setting	Tolerance Minor Divisions	RF Generator Setting (MHz)
.5 M	±1	501.5, 498.5
.2 M	±1	500.6,499.4
.1 M	±1	500.3,499.7
20 K	±1	500.06,499.04
10 K	±1	500.03,499.07
2 K	±7	500.006,499.004
1 K	±7	500.003,499.007

NOTE

Adjust R3615 (300 Hz BW ANALY CNTR) as needed to center tolerance (3 minor divisions) to dispersion settings at 2K and 1K. After completing narrow dispersion checks, repeat Steps 6 through 12 to recheck Wide Dispersion centering.

16. Rotate ANALY DISPR Control (38) to "1 M".

17. Disconnect RF Generator from ANTENNA Connector (56). Set RF Generator to 10.7 MHz at -20 dBm. Disconnect P5401 from J5401 on IF Module and connect RF Generator to J5401.

18. Connect external Spectrum Analyzer to Test Point 2 (TP2) on IF Module. Adjust R3938 (30 kHz BW GAIN) for 2.5 MHz signal at -22 dBm at TP2.

NOTE

External Spectrum Analyzer must be equipped with a DC Block for Steps 18 and 19.

19. Rotate ANALY DISPR Control (38) to "2 M". Adjust R3919 (650 kHz BW GAIN) for a 2.5 MHz signal at -19 dBm at TP2.

STEP	PROCEDURE
20.	Disconnect Spectrum Analyzer from TP2. Rotate ANALY DISPR Control (38) to ".1 M".
21.	Set RF Generator to 0 MHz output. Adjust R3961 (BASE LINE) on IF Module until base line is on -108 dB graticule.
22.	Set RF Generator to 10.7 MHz at -30 dBm. Adjust R3959 (DETECTOR GAIN) on IF Module until signal is on -40 dB graticule.
23.	Set RF Generator to 10.7 MHz at -20 dBm. Adjust R3941 (LOG LIN) on IF Module until signal is on -30 dB graticule.
24.	Set RF Generator to 10.7 MHz at -70 dBm. Adjust R3942 (AMP 1 GAIN) on IF Module until signal is on -80 dB graticule.
25.	Set RF Generator to 10.7 MHz at -90 dBm. Adjust R3951 (AMP 2 GAIN) on IF Module until signal is on -100 dB graticule.
26.	While stepping RF Generator output level from -20 dBm to -80 dBm, verify signal steps from -30 dB to -90 dB ±2 dB of each selected graticule. If tolerance is not met at each step, repeat Steps 20 thru 26.
27.	Set dB/DIV Switch (48) to "1". Rotate VERT POS Control (45) fully cw.
28.	Set RF Generator to 10.7 MHz at -20 dBm. Adjust R3963 (1 dBm OFFSET) on IF Module until signal is on -20 dB graticule.
29.	Set RF Generator to 10.7 MHz at -30 dBm. Adjust VERT POS Control (45) until signal is on top horizontal graticule.
30.	Set RF Generator to 10.7 MHz at -38 dBm. Adjust R3969 (1 dBm/DIV GAIN) on IF Module until signal is on bottom horizontal graticule.
31.	Repeat Steps 28 thru 30 and verify tolerance ±1 minor division can be met at each step without adjusting trimpots.
32.	Disconnect External Spectrum Analyzer.

STEP	PROCEDURE

33. Disconnect P4403 from J4403 on GENERATOR Mixer Module. Connect external Spectrum Analyzer to J4403. Center signal on external Spectrum Analyzer at 90 MHz and set external Analyzer controls to 1 MHz/DIV bandwidth.

34. Rotate DISPLAY Control to "ANALY". Adjust R3412 (F1 FIXED) and R3423 (F2 FIXED) on GENERATOR MIXER Module for maximum external Spectrum Analyzer signal gain. Adjust R3436 (OUTPUT) on GENERATOR MIXER Module for -13 dBm (±1 dB) at 90 MHz.

35. Observe external Spectrum Analyzer and verify sweep signal from 84 to 96 MHz is flat (±1 dB). If necessary, adjust R3413 (F1 GAIN), R3415 (F1 OFFSET), R3417 (F2 GAIN) and R3421 (F2 OFFSET) on GENERATOR MIXER Module.

NOTE

The above resistors are interactive and may need repeated adjustments to obtain the correct signal.

36. Disconnect Spectrum Analyzer from J4403. Connect P4403 to J4403 on GENERATOR MIXER Module.

37. Using BNC to BNC coax cable, connect ANTENNA Connector (56) to TRANS/-40 dB DUPLEX Connector (11). Rotate RF Output Level Control (10) to -40 dBm.

38. Observe signal on CRT. Adjust R3794 (TRACKING OFFSET) and R3791 (TRACKING GAIN) on RF Module for maximum level and flatness within 1 dB.

NOTE

Ensure S3701 on RF Module is in "RUN" position (to the left, looking from outside of assembly).

39. Use KEYBOARD (20) to select range (0-9) of 100 kHz digit on LCD (21). Verify displayed signal is flat (±1 dB).

STEP	PROCEDURE

40. Disconnect TRANS/-40 dB DUPLEX Connector (11) from ANTENNA Connector (56). Connect ANTENNA Connector (56) to DUPLEX OUTPUT Connector (16).

41. Set FM/AM-1500 Controls as follows:

CONTROL	SETTING
(10) RF Output Level Control	"-30 dBm"
(18) DUPLEX/SIMPLEX Switch	"DUPLEX"
(19) GEN/REC Switch	"GEN"
(20) KEYBOARD	"RF, 500.0000 (MHz)"
(38) ANALY DISPR Control	"10 K"
(51) DISPLAY Control	"ANALY"

42. Rotate ANALY DISPR Control (38) to "1 K". Adjust R3771 (300 kHz BW GAIN) on RF Module until signal is on -30 dBm graticule.

43. Rotate ANALY DISPR Control (38) to "1 M". Adjust R3777 (650 kHz BW GAIN) on RF Module until signal is on -30 dB graticule.

44. Set ATTENUATOR Switch (55) to "20 dB". Verify signal is on -50 dB graticule (±2 dB).

45. Set ATTENUATOR Switch (55) to "40 dB". Verify signal is on -70 dB graticule (±2 dB).

46. Set ATTENUATOR Switch (55) to "0 dB".

47. Rotate ANALY DISPR Control (38) to all settings except "2 K" and verify signal level on CRT is -30 dB (±2 dB).

48. Set FM/AM-1500 Controls as follows:

CONTROL	SETTING
(7) MODULATION Control	"AM 1"
(20) KEYBOARD	"RF, 500.0000 (MHz)"
	"T1, 1000.0 (Hz)"
(28) Tone 1 FM/OFF/AM Switch	"AM"
(38) ANALY DISPR Control	"FULL"
(51) DISPLAY Control	"TRACK"

49. Disconnect ANTENNA Connector (56) from DUPLEX OUTPUT Connector (16). Connect ANTENNA Connector (56) to TRANS/-40 dB DUPLEX Connector (11).

STEP	PROCEDURE
50.	Note position of carrier signal on CRT with TONE 1 Control (33) fully ccw. Verify, when TONE 1 Control (33) is rotated fully cw, RF envelope peaks at least +6 dBc and -26 dBc.
51.	Rotate TONE 1 Control (33) fully ccw. Rotate ANALY DISPR Control (38) to ".1 M". Reset RF to 000.0000 MHz. Disconnect ANTENNA Connector (56) from TRANS/-40 dB DUPLEX Connector (11). Adjust R9302 and R9303 in Mixer Null Module to put signal peak on top graticule.
52.	Rotate ANALY DISPR Control (38) to "FULL". Reset RF to 500.0000 MHz. Connect ANTENNA Connector (56) to TRANS/-40 dB DUPLEX Connector (11).
53.	Rotate TONE 1 Control (33) fully ccw. Set dB/DIV Switch (48) to "1". Verify tracking flatness on CRT (50) ±4 dB to 950 MHz or within 6 dB above 950 MHz.
54.	Rotate ANALY DISPR Control (38) to "10 M". Reset RF to 50.0000 MHz. Verify tracking flatness on CRT (50) of ≤2 dB from 0 to 50 MHz.
55.	Disconnect coax from ANTENNA Connector (56) and connect BNC tee to ANTENNA Connector (56); then connect coax to one side of tee. Connect open length of coax to other side of tee. Verify linear cable fault nulls across band.
56.	Disconnect open length of coax from tee.
57.	Rotate RF Output Level Control (10) to -100 dBm and verify cross-talk noise does not appear on CRT base line.
58.	Rotate DISPLAY Control (51) to "ANALY". Rotate ANALY DISPR Control (38) to "FULL".
59.	Observe base line on CRT (50). Verify straight base line with no signal present.
60.	Rotate ANALY DISPR Control (38) to "1 M". Note base line level.
61.	Reset RF to 15.0000 MHz. Verify base line rises ≤2 dB from level in Step 54.
62.	Reset RF to 5.0000 MHz. Verify base line rises ≤2 dB from 5 to 10 MHz with no extraneous signals present.

STEP	PROCEDURE

63. Set FM/AM-1500 Controls as follows:

CONTROL	SETTING
(18) DUPLEX/SIMPLEX Switch	"SIMPLEX"
(19) GEN/REC Switch	"GEN"
(38) ANALY DISPR Control	"10 K"
(51) DISPLAY Control	"ANALY"

64. Rotate GEN/LOCK Control (35) from fully (-) (not in "LOCK") to fully (+). Verify signal shifts at least ±10 kHz on each side of center frequency.

65. Rotate GEN/LOCK Control (35) to "LOCK". Verify signal level is between -35 and -65 dBm.

66. Disconnect all test equipment.

4-9 MICROPROCESSOR FUNCTIONAL BLOCK

There are no adjustments on the CPU/MEMORY PC Board. There are four adjustments on the I/O Interface PC Board: R4350, R4354, R4331 and R4333. R4350 and R4354 are adjusted during RECEIVER SIGNAL calibration (4-6-1). R4331 and R4333 are adjusted during RF OUTPUT POWER calibration (4-7-1).

SECTION 5 - TROUBLESHOOTING

5-1 GENERAL

This section contains detailed troubleshooting procedures for the following assemblies and systems in the FM/AM-1500:

Figure 5-1 shows an FM/AM-1500 System Block Diagram with keyed coax numbers. Table 5-1 is a troubleshooting aid which shows all coax numbers in the FM/AM-1500, corresponding reference connector numbers on the respective modules and signals expected at the respective connectors. For most Functional Blocks, Table 5-1 will enable the technician to isolate a faulty module. However, the Frequency Synthesis Functional Block requires interrupting the High Loop section in order to isolate a faulty module. See Paragraph 5-4 for the required procedure.

Figure 5-2 is an orthographic view of the FM/AM-1500 furnished as a quick reference aid to enable the technician to locate modules, coax connectors and plugs as they are located in the set. Notice that Figure 5-2 does not show any coax cables or ribbon cables.

5-1-1 TROUBLESHOOTING HINTS

In general, the recommended procedure for all modules, after the fault has been isolated to a particular module, is as follows:

a. Verify all power supply inputs are correct.
b. Verify all required reference frequencies are correct.
c. Verify all inputs and outputs controlled by Front Panel switches or controls operate in the required manner.
d. Verify test points have the proper signals as outlined in Module Troubleshooting Procedures.

The above steps should enable the technician to isolate a faulty circuit. It is left to the technician to isolate faulty components in that circuit.

5-1-2 TROUBLESHOOTING SAFETY

As with any piece of electronic equipment, extreme caution should be taken when troubleshooting "live" circuits. Certain circuits and/or components within the FM/AM-1500 contain extremely high voltage potentials, CAPABLE OF CAUSING BODILY INJURY OR DEATH (see WARNINGS below)! When troubleshooting the FM/AM-1500, be sure to observe the following precautions:

WARNING

THE OSCILLOSCOPE CONTROL AND DEFLECTION PC BOARD AND THE CRT CARRY A VOLTAGE OF 2000 VDC WHEN THE FM/AM-1500 IS ENERGIZED. DO NOT CONTACT THESE OR ANY ASSOCIATED COMPONENTS DURING TROUBLESHOOTING.

WHEN WORKING WITH "LIVE" CIRCUITS OF HIGH POTENTIAL, KEEP ONE HAND IN POCKET, OR BEHIND BACK, TO AVOID SERIOUS SHOCK HAZARD.

REMOVE ALL JEWELRY OR OTHER CONDUCTIVE APPAREL BEFORE TROUBLESHOOTING AND/OR REPAIRING LIVE CIRCUITS.

USE ONLY INSULATED TROUBLESHOOTING TOOLS WHEN WORKING WITH LIVE CIRCUITS.

FOR ADDED INSULATION, PLACE RUBBER BENCH MAT UNDERNEATH ALL POWERED BENCH EQUIPMENT, AS WELL AS A RUBBER FLOOR MAT UNDERNEATH TECHNICIAN'S CHAIR.

HEED ALL WARNINGS AND CAUTIONS CONCERNING MAXIMUM VOLTAGES AND POWER INPUTS.

5-1-3 TROUBLESHOOTING EQUIPMENT REQUIREMENTS

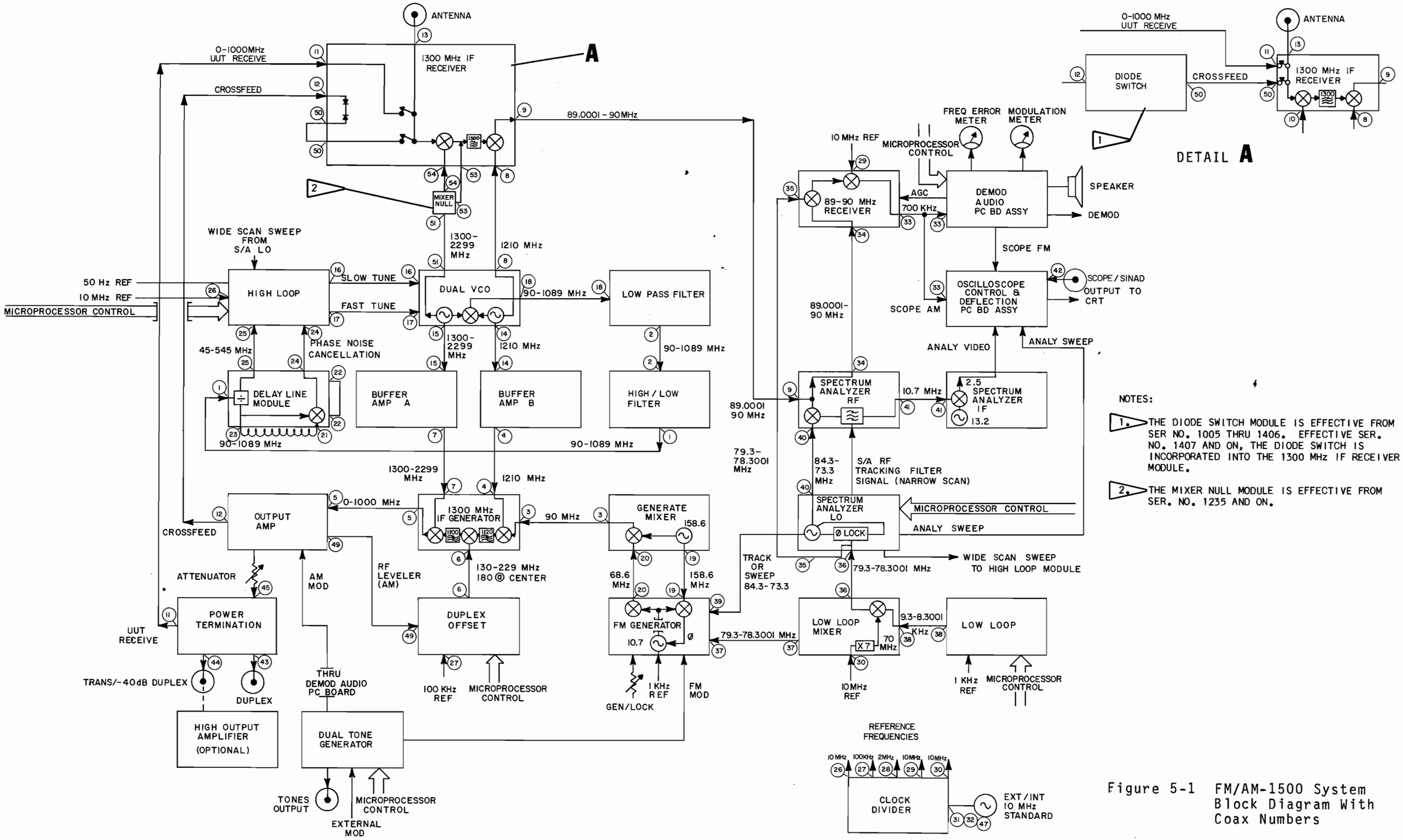
Appendix E at the rear of this manual contains a comprehensive list of test equipment suitable for performing any of the procedures in this manual. Any other equipment meeting the specifications listed in Appendix E may be substituted in place of the recommended models.

NOTE

For certain procedures in this manual, the equipment listed in Appendix E may exceed the minimum required specificatons; for this reason, minimum use specifications appear with all module troubleshooting procedures, where accessory test equipment is required.

5-1-4 DISASSEMBLY REQUIREMENTS

To perform any of the troubleshooting procedures contained in this section, the exterior case must be removed from the FM/AM-1500. Refer to "SECTION 6 - MECHANICAL ASSEMBLIES/PC BOARDS" for illustrations.



NOTES:

1. THE DIODE SWITCH MODULE IS EFFECTIVE FROM SER NO. 1005 THRU 1406. EFFECTIVE SER. NO. 1407 AND ON, THE DIODE SWITCH IS INCORPORATED INTO THE 1300 MHz IF RECEIVER MODULE.

2. THE MIXER NULL MODULE IS EFFECTIVE FROM SER. NO. 1235 AND ON.

Figure 5-1 FM/AM-1500 System Block Diagram With Coax Numbers

	COAX NO.	SIGNAL SOURCE	SIGNAL DESTINATION
9	1	J602, High/Low Filter	J3005, Delay Line
9	2	FL6401-P1, Low Pass Filter	J601, High/Low Filter
	3	J4403, Gen Mixer	J1202, 1300 MHz IF Gen
	4	J6902B, Buffer Amp B	J1201, 1300 MHz IF Gen
	5	J1205, 1300 MHz IF Gen	J801, Output Amp
9	6	J3201, Duplex Offset	J1203, 1300 MHz IF Gen
	7	J6902A, Buffer Amp A	J1204, 1300 MHz IF Gen
	8	J2402, Dual VCO	J1001, 1300 MHz IF Rcvr
	9	J1002, 1300 MHz IF Rcvr	J5202, S/A RF
5	10	J2404, Dual VCO	J1006, 1300 MHz IF Rcvr
11	11	J9804, Power Term.	J1005, 1300 MHz IF Rcvr
6	12	J804, Output Amp	J1008, 1300 MHz IF Rcvr
	13	J401, Front Panel (Ant.)	J1003, 1300 MHz IF Rcvr
	14	J2401, Dual VCO	J6901B, Buffer Amp B
	15	J2405, Dual VCO	J6901A, Buffer Amp A
	16	J2806, High Loop	J2406, Dual VCO
	17	J2805, High Loop	J2403, Dual VCO
9	18	J2407, Dual VCO	FL6401-J2, Low Pass Filter
	19	J4402, Gen Mixer	J4205, FM Gen
	20	J4206, FM Gen	J4401, Gen Mixer
Same	21	J3007, Delay Line	J3001, Delay Line
	22	J3008, Delay Line	J3002, Delay Line
Coax	23	J3007, Delay Line	J3001, Delay Line
	24	J3004, Delay Line	J2804, High Loop
9	25	J3006, Delay Line	J2801, High Loop
	26	J1405, Clock Divider	J2802, High Loop
	27	J1407, Clock Divider	J3203, Duplex Offset
	28	J1408, Clock Divider	J5313, Motherboard
			J5903, GPIB Interface
	29	J1404, Clock Divider	J3804, 89-90 MHz Rcvr
	30	J1403, Clock Divider	J1801, Low Loop Mxr
2	31	J1402, Clock Divider	J6401, Rear Panel
	32	J7001, TCXO	J14(Clock Divider
9	33	J3805, 89-90 MHz Rcvr	J4704, Demod Audio PC Bd
			J4706, Demod Audio PC Bd
			J5105, Osc. Cont. & Defl. PC Bd
	34	J5201, S/A RF	J3802, 89-90 MHz Rcvr
	35	J4601, S/A LO	J3801, 89-90 MHz Rcvr

Table 5-1 Coax Running List
(Sheet 1 of 2)

COAX NO.	SIGNAL SOURCE	SIGNAL DESTINATION
36	J1804, Low Loop Mxr	J4602, S/A LO
37	J1803, Low Loop Mxr	J4201, FM Gen
38	J4001, Low Loop	J1802, Low Loop Mxr
4 39	J4604, S/A LO	J4202, FM Gen
4 40	J4605, S/A LO	J5203, S/A RF
10 41	J5205, S/A RF	J5401, S/A IF
42	J403, Front Panel (Scope/Sinad)	J5101, Osc. Cont. & Defl. PC Bd
11 43	J9803, Power Term.	J407, Front Panel (Duplex)
11 3 44	J402, Front Panel (Trans/-40 dB)	J9802, Power Term.
11 45	AT401-J2, Manual Atten.	J9801, Power Term.
11 46	AT5901-J1, Prog. Atten.	J9801, Power Term.
47	J7403, Oven Osc.	J1401, Clock Divider
48	Not Used	
49	J802, Output Amp	J3204, Duplex Offset
7 50	J1009, 1300 MHz IF Rcvr	J1004, 1300 MHz IF Rcvr
8 51	J2404, Dual VCO	J9301, Mixer Null
52	J7304, High Output Amp	J401, Front Panel (ANT.)
8 53	J9303, Mixer Null	J1010, 1300 MHz IF Rcvr
8 54	J9302, Mixer Null	J1006, 1300 MHz IF Rcvr

NOTES:

1. DEFINITIONS:

   F_H = FIRST 3 DIGITS OF RF FREQUENCY SETTING (I.E.; F_H = 900 MHz FOR 900.XXXX SETTING)
   F_L = LAST 4 DIGITS OF RF FREQUENCY SETTING (I.E.; F_L = 999.9 kHz FOR XXX.9999 SETTING)
   F_{OFF} = OFFSET SETTING (I.E.; F_{OFF} = 25.50 MHz FOR 25.50 SETTING)
   F_C = CARRIER FREQUENCY INJECTED

2. J6301 IS ALSO THE INPUT CONNECTOR FOR AN EXTERNAL 10 MHz REFERENCE FREQUENCY.
3. IN GEN DUPLEX MODE, SIGNAL IS 40 dB LOWER THAN SIGNAL IN.
4. THE CENTER OF SWEEP RANGE IS 79.3 MHz - F_L.
5. DELETE ON SERIAL #1235 AND SUBSEQUENT.
6. CHANGE SIGNAL DESTINATION TO J1008, 1300 MHz IF RCVR, ON SERIAL #1407 AND SUBSEQUENT.
7. CHANGE SIGNAL SOURCE TO J7101, DIODE SWITCH PRIOR TO SERIAL #1407.
8. EFFECTIVE ON SERIAL #1235 AND SUBSEQUENT.
9. CONNECT A TEE AT SOURCE TO OBSERVE SIGNAL.
10. SIGNAL WILL "BOUNCE" IN ALL MODES.
11. EFFECTIVE THRU SER. NO. 1993. POWER TERMINATION REF DES SERIES WAS 6200.

Table 5-1 Coax Running List
(Sheet 2 of 2)

COAX NO.	DUPLEX		SIMPLEX GEN		SIMPLEX REC		TRACK NARROW		TRACK WIDE	
	LEVEL	FREQUENCY	LEVEL	FREQUENCY	LEVEL	FREQUENCY	LEVEL	FREQUENCY	LEVEL	FREQUENCY
1	-36 dBm	F_H + 90 MHz	-36 dBm	F_H + 90 MHz	-36 dBm	F_H +90 MHz	-36 dBm	F_H + 90 MHz	-36 dBm	(F_H + 90 MHz) ± Track Sweep
2	-30 dBm	F_H + 90 MHz	-30 dBm	F_H + 90 MHz	-30 dBm	F_H +90 MHz	-30 dBm	F_H + 90 MHz	-30 dBm	(F_H + 90 MHz) ± Track Sweep
3	-16 dBm	90 MHz	-16 dBm	90 MHz			-16 dBm	90 MHz ± Track Sweep	-16 dBm	90 MHz
4	+5 to +12 dBm	1210 MHz (±2 MHz)	+5 to +12 dBm	1210 MHz (±2 MHz)	+5 to +12 dBm	1210 MHz (±2 MHz)	+5 to +12 dBm	1210 MHz (±2 MHz)	+5 to +12 dBm	1210 MHz (±2 MHz)
5	-12 to -15 dBm	$F_H + F_L \pm F_{OFF}$	-12 to -15 dBm	$F_H + F_L$			-12 to -15 dBm	($F_H + F_L \pm F_{OFF}$) ± Track Sweep	-12 to -15 dBm	($F_H + F_L \pm F_{OFF}$) ± Track Sweep
6	-20 ±AM Mod	180 MHz ± F_{OFF}	-20 ±AM Mod	180 MHz		180 MHz	-20 ±AM Mod	180 MHz	-20 ±AM Mod	180 MHz
7	+5 to +12 dBm	1300 MHz + F_H (±2 MHz)	+5 to +12 dBm	1300 MHz + F_H (±2 MHz)	+5 to +12 dBm	1300 MHz + F_H (±2 MHz)	+5 to +12 dBm	1300 MHz + F_H (±2 MHz)	+5 to +12 dBm	1300 MHz + F_H ± Track Sweep
8	+5 to +12 dBm	1210 MHz (±2 MHz)	+5 to +12 dBm	1210 MHz (±2 MHz)	+5 to +12 dBm	1210 MHz (±2 MHz)	+5 to +12 dBm	1210 MHz (±2 MHz)	+5 to +12 dBm	1210 MHz (±2 MHz)
9			-30 dBm	$F_C - F_H$ + 90 MHz						
10	+5 to +12 dBm	1300 MHz + F_H (±2 MHz)	+5 to +12 dBm	1300 MHz + F_H (±2 MHz)	+5 to +12 dBm	1300 MHz + F_H (±2 MHz)	+5 to +12 dBm	1300 MHz + F_H (±2 MHz)	+5 to +12 dBm	1300 MHz + F_H ± Track Sweep
11		F_C			T/R -55 dB	F_C				
12	> -60 dBm	$F_H + F_L \pm F_{OFF}$	-40 dBm	$F_H + F_L \pm F_{OFF}$			> -60 dBm	$F_H + F_L$ ± Track Sweep	> -60 dBm	$F_H + F_L$ ± Track Sweep
13	Same as Input	F_C	Same as Input	F_C	Same as Input	F_C	Same as Input	F_C	Same as Input	F_C
14	+5 to +12 dBm	1210 MHz (±2 MHz)	+5 to +12 dBm	1210 MHz (±2 MHz)	+5 to +12 dBm	1210 MHz (±2 MHz)	+5 to +12 dBm	1210 MHz (±2 MHz)	+5 to +12 dBm	1210 MHz (±2 MHz)
15	+5 to +12 dBm	1300 MHz + F_H (±2 MHz)	+5 to +12 dBm	1300 MHz + F_H (±2 MHz)	+5 to +12 dBm	1300 MHz + F_H (±2 MHz)	+5 to +12 dBm	1300 MHz + F_H (±2 MHz)	+5 to +12 dBm	1300 MHz + F_H ± Track Sweep
16		DC Level		DC Level		DC Level		DC Level		DC Level
17		Noise Voltage		Noise Voltage		Noise Voltage		Noise Voltage		Noise Voltage
18	-25 to -30 dBm	F_H + 90 MHz	-25 to -30 dBm	F_H + 90 MHz	-25 to -30 dBm	F_H + 90 MHz	-25 to 30 dBm	F_H + 90 MHz	-25 to -30 dBm	Track Sweep
19	+2 dBm	158.6 MHz	+2 dBm	158.6 MHz			+2 dBm	158.6 MHz	+2 dBm	158.6 MHz
20	-16 dBm	68.6 MHz	-16 dBm	68.6 MHz			-16 dBm	90 MHz ± Track Sweep	-16 dBm	90 MHz ± Track Sweep
21	+8 dBm	(F_H + 90 MHz)/2	+8 dBm	(F_H + 90 MHz)/2	+8 dBm	(F_H + 90 MHz)/2	+8 dBm	(F_H + 90 MHz)/2	+8 dBm	Track Sweep
22	+8 dBm	(F_H + 90 MHz)/2	+8 dBm	(F_H + 90 MHz)/2	+8 dBm	(F_H + 90 MHz)/2	+8 dBm	(F_H + 90 MHz)/2	+8 dBm	RF ± Track Sweep
23	0 dBm	(F_H + 90 MHz)/2	0 dBm	(F_H + 90 MHz)/2	0 dBm	(F_H + 90 MHz)/2	0 dBm	(F_H + 90 MHz)/2	0 dBm	(F_H + 90 MHz)/2
24		Noise Voltage		Noise Voltage		Noise Voltage		Noise Voltage		Noise Voltage
25	-8 to -12 dBm	(F_H + 90 MHz)/2	-8 to -12 dBm	(F_H + 90 MHz)/2	-8 to -12 dBm	(F_H + 90 MHz)/2	-8 to -12 dBm	(F_H + 90 MHz)/2	-8 to -12 dBm	RF ± Track Sweep
26	-2 dBm	10 MHz	-2 dBm	10 MHz	-2 dBm	10 MHz	-2 dBm	10 MHz	-2 dBm	10 MHz
27	0 dBm	100 kHz	0 dBm	100 kHz	0 dBm	100 kHz	0 dBm	100 kHz	0 dBm	100 kHz
28	0 dBm	2 MHz	0 dBm	2 MHz	0 dBm	2 MHz	0 dBm	2 MHz	0 dBm	2 MHz
29	-2 dBm	10 MHz	-2 dBm	10 MHz	-2 dBm	10 MHz	-2 dBm	10 MHz	-2 dBm	10 MHz
30	-2 dBm	10 MHz	-2 dBm	10 MHz	-2 dBm	10 MHz	-2 dBm	10 MHz	-2 dBm	10 MHz
31	-18 dBm	10 MHz	-18 dBm	10 MHz	-18 dBm	10 MHz	-18 dBm	10 MHz	-18 dBm	10 MHz
32	0 dBm	10 MHz	0 dBm	10 MHz	0 dBm	10 MHz	0 dBm	10 MHz	0 dBm	10 MHz
33	-8 dBm	700 kHz	-8 dBm	700 kHz	-8 dBm	700 kHz		Noise		Noise
	-8 dBm	700 kHz	-8 dBm	700 kHz	-8 dBm	700 kHz		Noise		Noise
	-8 dBm	700 kHz	-8 dBm	700 kHz	-8 dBm	700 kHz		Noise		Noise
34	-30 dBm	$F_C - F_H$ + 90 MHz ± F_{OFF}	-30 dBm	$F_C - F_H$ + 90 MHz	-30 dBm	$F_C - F_H$ + 90 MHz	-30 dBm	90 MHz ± Track Sweep	-30 dBm	90 MHz
35	+4 to +12 dBm	79.3 MHz - F_L	+4 to +12 dBm	79.3 MHz - F_L	+4 to +12 dBm	79.3 MHz - F_L	+4 to +12 dBm	79.3 MHz - F_L	+4 to +12 dBm	79.3 MHz - F_L
36	+4 to +12 dBm	79.3 MHz - F_L	+4 to +12 dBm	79.3 MHz - F_L	+4 to +12 dBm	79.3 MHz - F_L	+4 to +12 dBm	79.3 MHz - F_L	+4 to +12 dBm	79.3 MHz - F_L
37	+4 to +12 dBm	79.3 MHz - F_L	+4 to +12 dBm	79.3 MHz - F_L	+4 to +12 dBm	79.3 MHz - F_L	+4 to +12 dBm	79.3 MHz - F_L	+4 to +12 dBm	79.3 MHz - F_L
38	-15 to -10 dBm	9.3 MHz - F_L	-15 to -10 dBm	9.3 MHz - F_L	-15 to -10 dBm	9.3 MHz - F_L	-15 to -10 dBm	9.3 MHz - F_L	-15 to -10 dBm	9.3 MHz - F_L
39	+5 dBm	(79.3 MHz - F_L) ±5 MHz	+5 dBm	(79.3 MHz - F_L) ±5 MHz	+5 dBm	(79.3 MHz - F_L) ±5 MHz	+5 dBm	(79.3 MHz - F_L) ±5 MHz	+5 dBm	79.3 MHz - F_L
40	+6 dBm	(79.3 MHz - F_L) ±5 MHz	+6 dBm	(79.3 MHz - F_L) ±5 MHz	+6 dBm	(79.3 MHz - F_L) ±5 MHz	+6 dBm	(79.3 MHz - F_L) ±5 MHz	+6 dBm	79.3 MHz - F_L

Table 5-2 Coax Troubleshooting Chart
(Sheet 1 of 2)

COAX NO.	DUPLEX		SIMPLEX GEN		SIMPLEX REC		TRACK NARROW		TRACK WIDE	
	LEVEL	FREQUENCY	LEVEL	FREQUENCY	LEVEL	FREQUENCY	LEVEL	FREQUENCY	LEVEL	FREQUENCY
41	-20 dB	10.7 MHz ±500 kHz Sweep	-38 dBm	10.7 MHz ±500 kHz Sweep	-2 dBm	10.7 MHz ±500 kHz Sweep	-20 dBm	10.7 MHz	-20 dBm	10.7 MHz
42	V_{IN}	F_{IN}	V_{IN}	F_{IN}	V_{IN}	F_{IN}	V_{IN}	F_{IN}	V_{IN}	F_{IN}
43	Atten. Setting	$F_H + F_L \pm F_{OFF}$				No Signal				
44	Atten. Set. -40 dB	$F_H + F_L \pm F_{OFF}$	Atten. Set.	$F_H + F_L$		No Signal	Atten. Set.	$F_H + F_L \pm$ Track Sweep	Atten. Set.	$F_H + F_L \pm$ Track Sweep
45	Atten. +6 dB	$F_H + F_L \pm F_{OFF}$	Atten. +6 dBm	$F_H + F_L$		No Signal	Atten. +6 dBm	$F_H + F_L \pm$ Track Sweep	Atten. +6 dBm	$F_H + F_L \pm$ Track Sweep
46	Atten. -40 dB	$F_H + F_L \pm F_{OFF}$	Atten. Set.	$F_H + F_L$		No Signal	Atten. Set.	$F_H + F_L \pm$ Track Sweep	Atten. Set.	$F_H + F_L \pm$ Track Sweep
47	0 dBm	10 MHz	0 dBm	10 MHz	0 dBm	10 MHz	0 dBm	10 MHz	0 dBm	10 MHz
48	Not Used									
49		DC Level		DC Level		DC Level		DC Level		DC Level
50		No Signal	-20 dBm	$F_H + F_L \pm F_{OFF}$		No Signal		No Signal		No Signal
51	+5 to +12 dBm	F_H + 1300 MHz	+5 to +12 dBm	F_H + 1300 MHz	+5 to +12 dBm	F_H + 1300 MHz	+5 to +12 dBm	F_H + 1300 MHz	+5 to +12 dBm	F_H + 1300 MHz ± Track Sweep
52										
53		No Signal		No Signal		No Signal		No Signal		No Signal
54	+5 to +12 dBm	F_H + 1300 MHz	+5 to +12 dBm	F_H + 1300 MHz	+5 to +12 dBm	F_H + 1300 MHz	+5 to +12 dBm	F_H + 1300 MHz	+5 to +12 dBm	F_H + 1300 MHz ± Track Sweep

CONTROL SETTINGS FOR TABLE 5-2

DUPLEX

Control	Setting
ANALY DISPR	1 MHz/DIV
GEN/REC	GEN
DUPLEX/SIMPLEX	DUPLEX
DISPLAY	ANALY
RF OUTPUT LEVEL	-30 dBm

Connect DUPLEX OUTPUT Connector to ANTENNA Connector

SIMPLEX GEN

Control	Setting
ANALY DISPR	1 MHz/DIV
GEN/REC	GEN
DUPLEX/SIMPLEX	SIMPLEX
DISPLAY	ANALY
RF OUTPUT LEVEL	-30 dBm

SIMPLEX REC

Control	Setting
ANALY DISPR	1 MHz/DIV
GEN/REC	REC
DISPLAY	ANALY
ATTENUATOR SW.	0 dB

Connect Signal Generator (-30 dBm at desired Frequency) to ANTENNA Connector

TRACK NARROW

Control	Setting
ANALY DISPR	1 K to 1 M
ATTENUATOR SW.	0 dB
RF OUTPUT LEVEL	-30 dBm

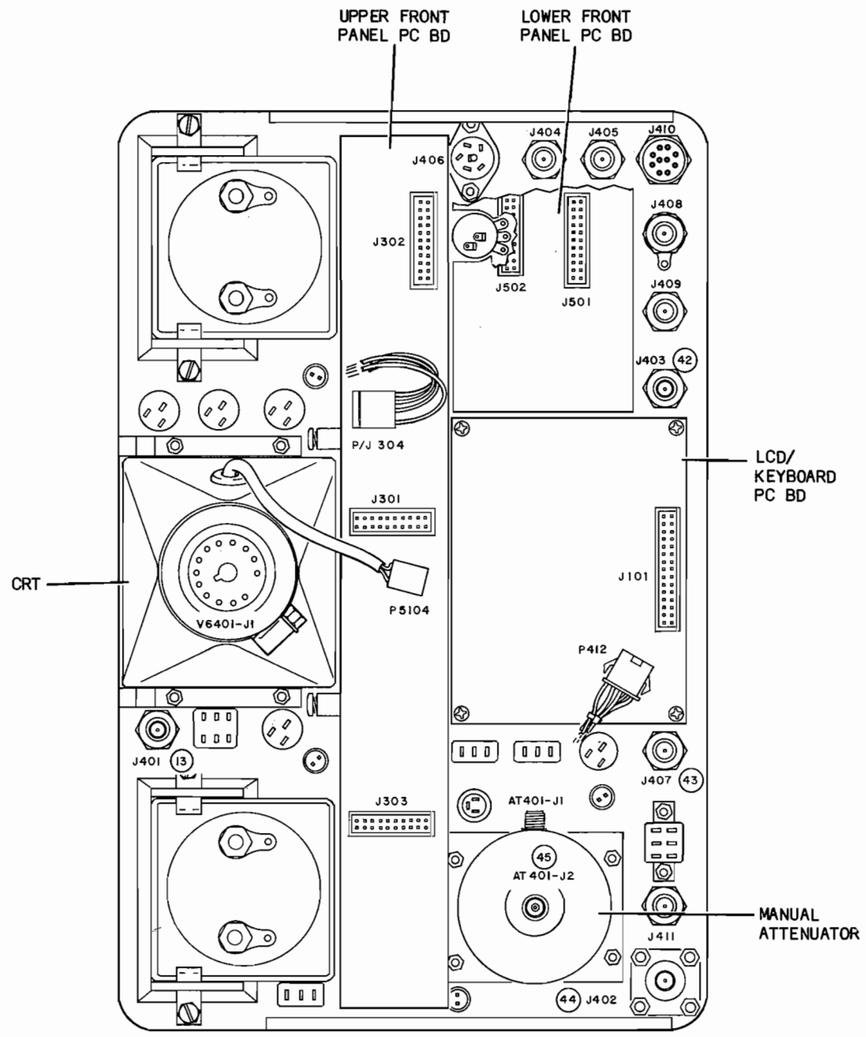
Connect TRANS/-40 dB DUPLEX Connector to ANTENNA Connector

TRACK WIDE

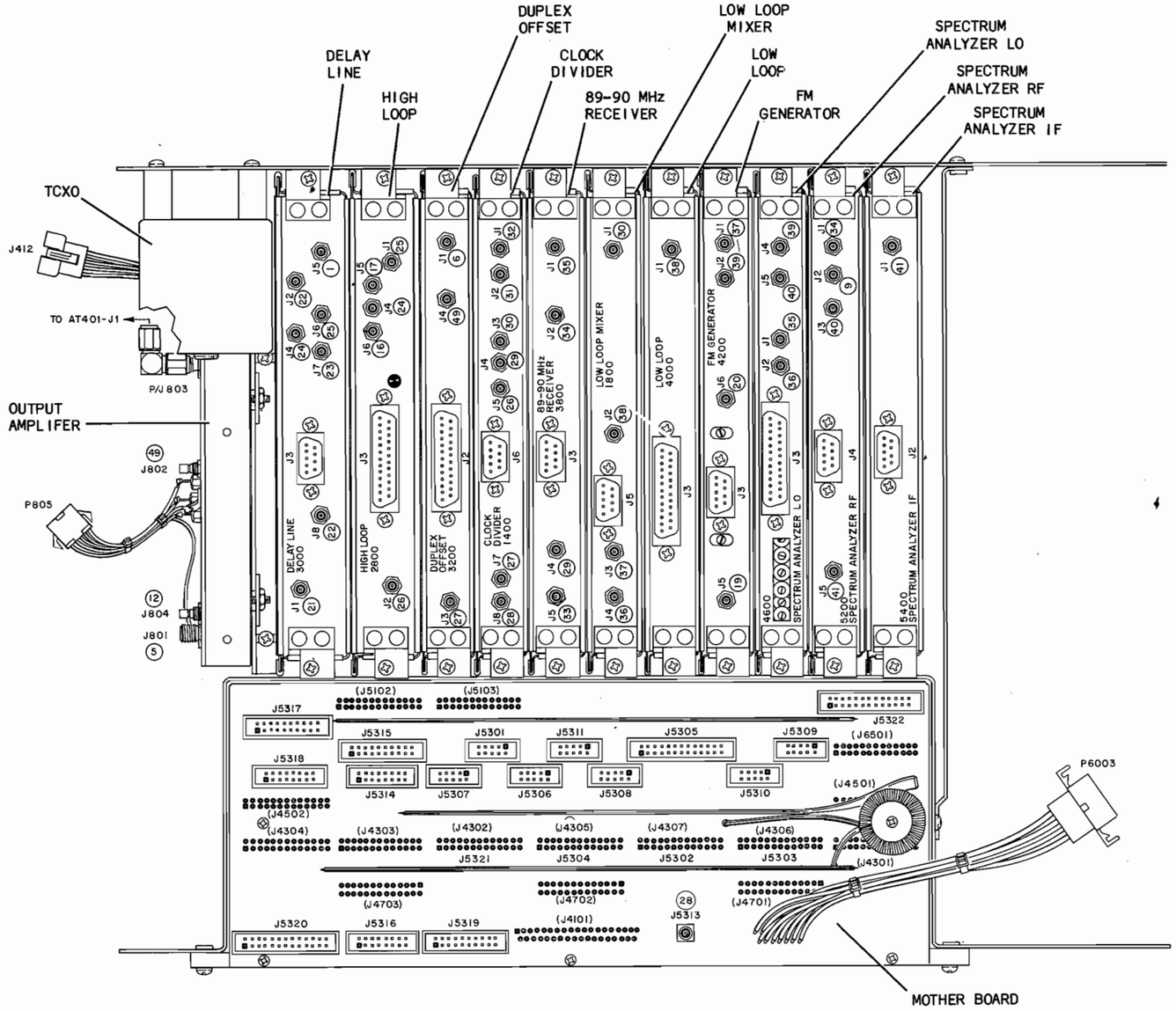
Control	Setting
ANALY DISPR	2 M TO FULL
ATTENUATOR SW.	0 dB
RF OUTPUT LEVEL	-30 dBm

Connect TRANS/-40 dB DUPLEX Connector to ANTENNA Connector

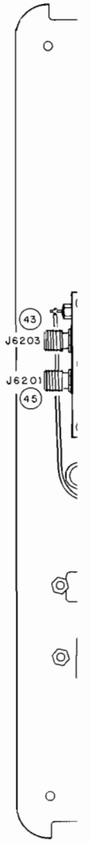
Table 5-2 Coax Troubleshooting Chart (Sheet 2 of 2)

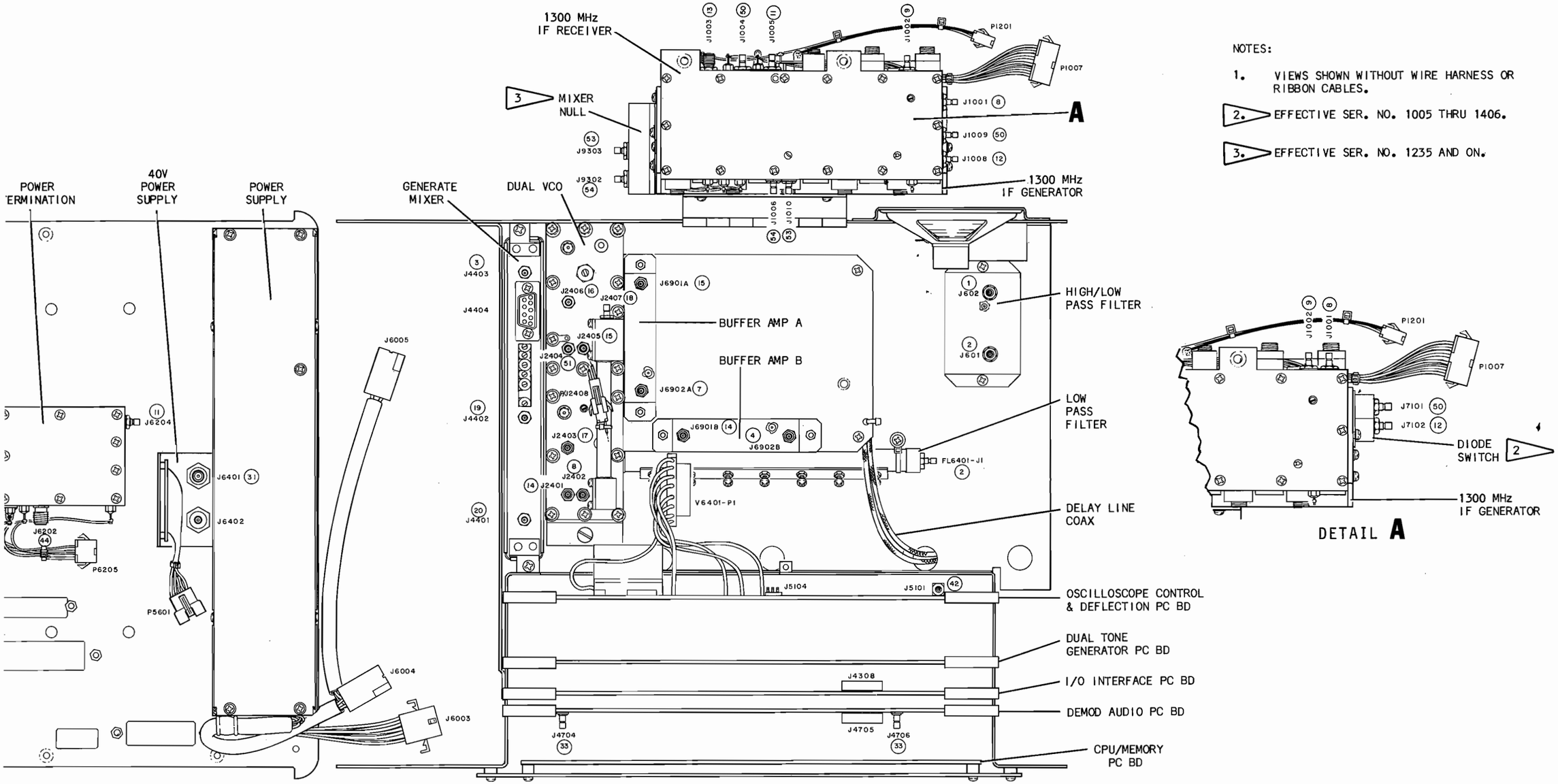


BACK VIEW OF FRONT PANEL



BOTTOM VIEW





FRONT VIEW OF REAR PANEL

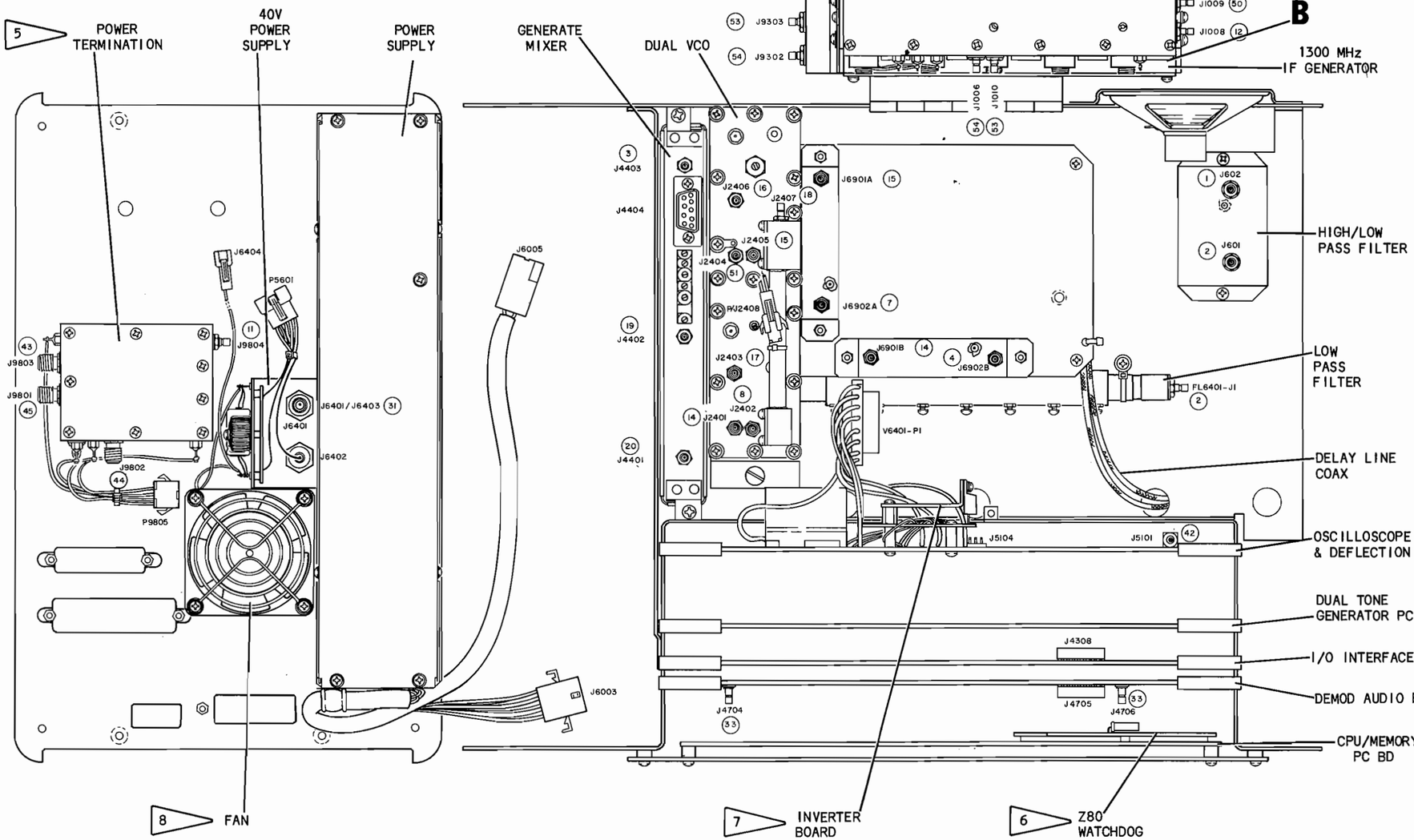
DETAIL **A**

NOTES:

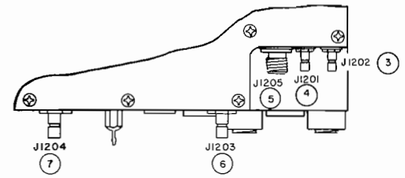
1. VIEWS SHOWN WITHOUT WIRE HARNESS OR RIBBON CABLES.
2. EFFECTIVE SER. NO. 1005 THRU 1406.
3. EFFECTIVE SER. NO. 1235 AND ON.

THRU SER. NO. 1931

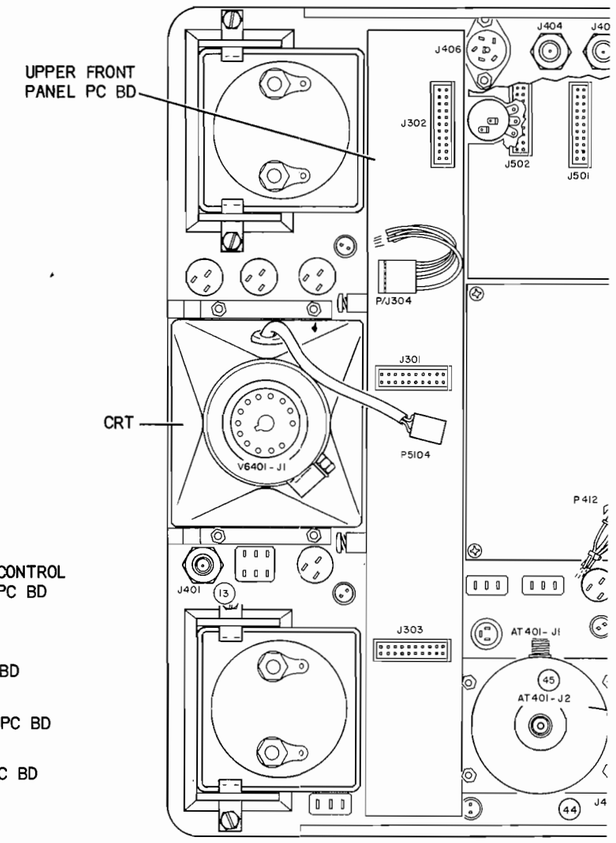
Figure 5-2 Orthographic View of FM/AM-1500 (Sheet 1 of 2)



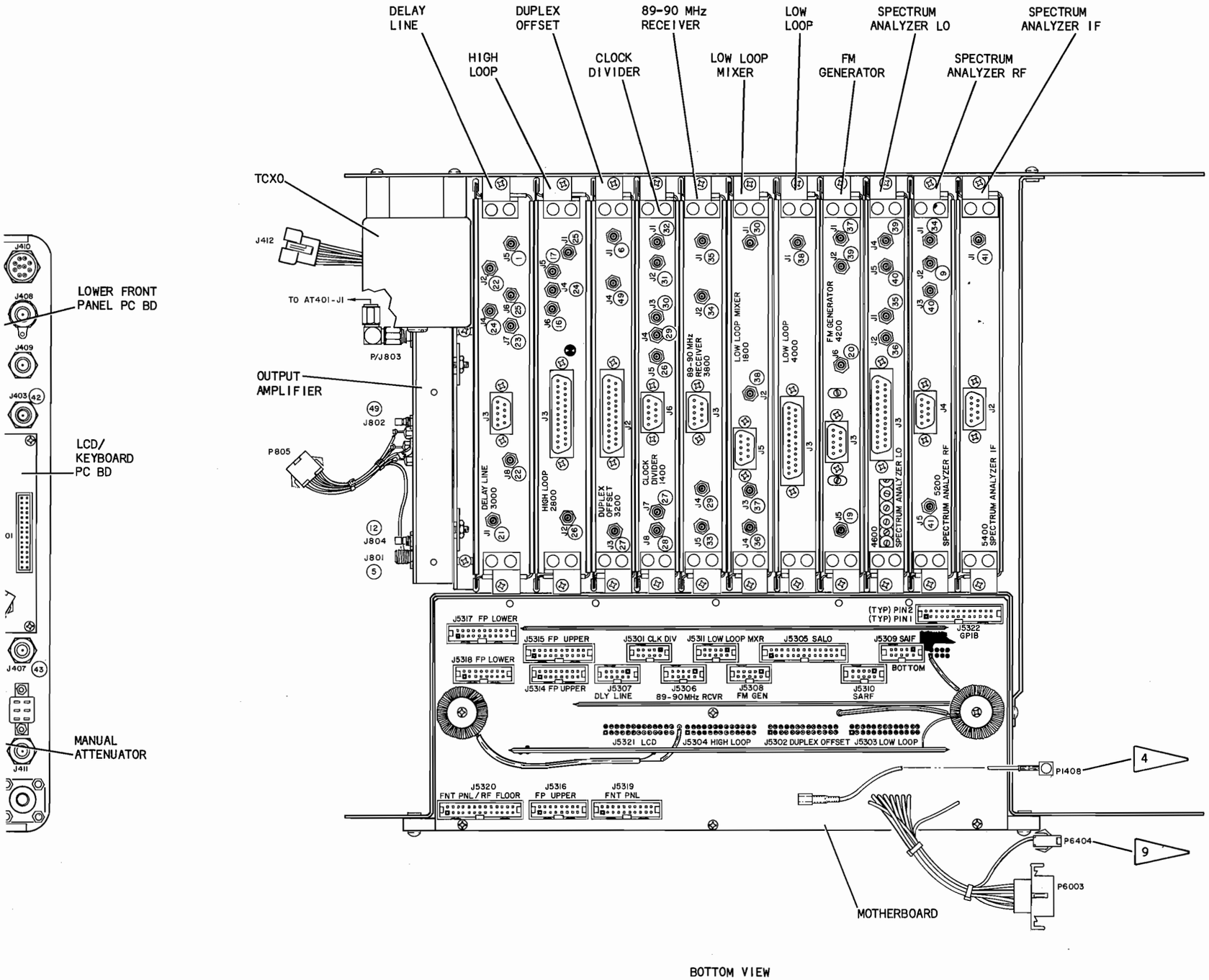
FRONT VIEW OF REAR PANEL
SER. NO. 1932 AND ON



DETAIL **B**



BACK VIEW OF FRONT PANEL



BOTTOM VIEW

NOTES (CONT.):

4. EFFECTIVE SER. NO. 1932, P1408 BECOMES P1409 WHEN GPIB IS INSTALLED.

5. THRU SER. NO. 1993, POWER TERMINATION REF DES SERIES WAS 6200; EFFECTIVE SER. NO. 1994, REF DES IS 9800.

6. EFFECTIVE SER. NO. 2061, ADD Z80 WATCHDOG PC BOARD TO CPU/MEMORY PC BOARD.

7. EFFECTIVE SER. NO. 2100, ADD INVERTER PC BOARD TO OSCILLOSCOPE CONTROL AND DEFLECTION PC BOARD.

8. EFFECTIVE SER. NO. 2134, ADD FAN TO BACK PANEL; J6004 NOT USED.

9. EFFECTIVE SER. NO. 2180, ADD P6404.

SER. NO. 1932 AND ON

Figure 5-2 Orthographic View of FM/AM-1500 (Sheet 2 of 2)

5-2 POWER SUPPLY FUNCTIONAL BLOCK TROUBLESHOOTING

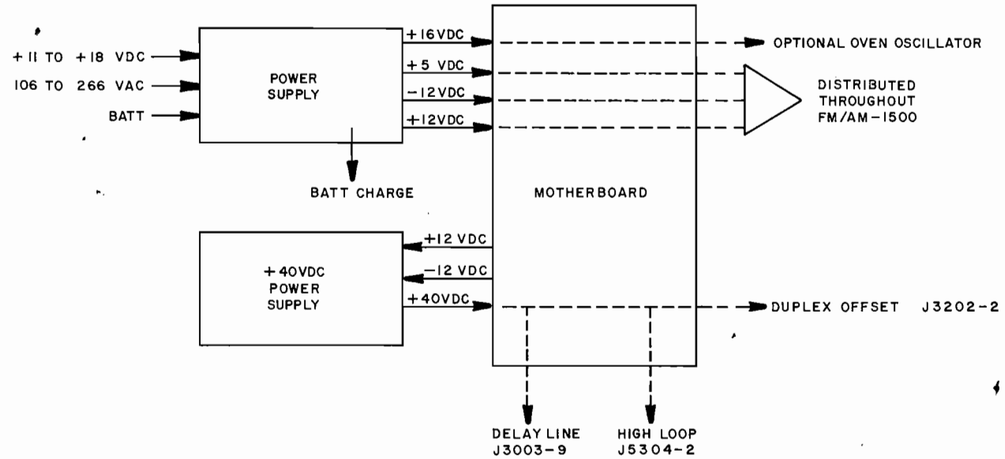


Figure 5-3 Power Supply Functional Block

5-2-1 POWER SUPPLY MODULE TROUBLESHOOTING

SPECIAL ACCESSORY EQUIPMENT REQ'D:
- 1 Variable Power Supply---Variable from 0 to +16 VDC
- 1 Digital Voltmeter---Any
- 1 Oscilloscope---Dual Trace
- 1 50 VDC Power Supply---Any
- 1 Battery Load Simulator (IFR Part No. 1003-9801-600)---See Appendix D

FIGURE REFERENCES:
- Power Supply Module (Section 6)
- Power Supply Schematic (Section 7)
- Power Supply Theory (Section 2)

TEST SET-UP DIAGRAM: N/A

STEP	PROCEDURE

<u>+10 V Regulator Circuit</u>

1. Remove Power Supply Module and remove cover from Module.
2. Apply +16 VDC at DC Power Input connector (J6001).
3. +10 V Regulator - verify +10 VDC at TP3.
4. 2nd Trapezoid Oscillator - verify 50 kHz square wave from -1 to +9 VDC at pin 6 of U5705.
5. 2nd Regulator - verify voltage is variable at pin 6 of U5707 as R5755 is adjusted.
6. 2nd Driver - verify an approximate 50 kHz square wave at emitters of Q5712 and Q5713. Leave probe connected.
7. 2nd MOS Switch - connect a second probe at drains of Q5708, Q5709 and Q5710 and verify square waves are 180° out of phase with 2nd Driver.
8. Move second probe to anode of CR5720 and verify the two square waves are 180° out of phase.
9. Move second probe to cathode of CR5722 and verify the two square waves are in phase.
10. Move second probe to anode of CR5721 and verify the two square waves are 180° out of phase and the second probe shows about one half the amplitude of the first.
11. Remove DC power input.

STEP PROCEDURE

+15 V Regulator Circuit

WARNING:

DO NOT USE AC POWER WHEN TROUBLESHOOTING THE POWER SUPPLY MODULE. THE DIFFERENCE OF POTENTIAL BETWEEN FLOATING GROUND AND CHASSIS GROUND CAN EXCEED 300 V PEAK. THIS POTENTIAL CAN CAUSE SERIOUS INJURY OR EVEN DEATH. IF IT IS ABSOLUTELY NECESSARY TO TROUBLESHOOT USING AC, ALWAYS USE AN ISOLATION TRANSFORMER AND TAKE EXTREME CARE WHEN WORKING INSIDE THE POWER SUPPLY MODULE.

1. Apply +50 VDC across L and N terminals of the AC Power Input Connector (J6002).

2. Check for about 50 VDC across C5803.

3. Reverse polarity of 50 VDC input. Again check voltage across C5803.

4. +15 V Regulator - verify voltage of about +15 VDC at TP1.

5. 1st Trapezoid Oscillator - verify approximately 50 kHz square wave from -2 to +15 VDC at pin 6 of U5701.

6. 1st Driver - verify approximately 50 kHz square wave at TP4. Leave probe connected.

7. Turn off 50 VDC Power Supply. Ground TP2. Connect Variable Power Supply set at 0 VDC to TP5.

8. Turn on 50 VDC Power Supply.

9. Vary Variable Power Supply from 0 to 1.5 VDC. Verify that square wave on scope collapses.

10. Set Variable Power Supply to 0 V. Remove ground from TP2. Vary Variable Power Supply from 0 to 1 VDC. Verify that scope display varies about 0.7 VDC.

11. Disconnect Variable Power Supply.

12. 1st MOS Switch - connect second probe to drain of Q5707. Verify that the two signals are 180° out of phase.

13. Turn off 50 VDC Power Supply.

STEP	PROCEDURE

Battery Charger Circuit

1. Connect Battery Load Simulator to the battery connector (J6004).

2. Turn on 50 VDC Power Supply.

3. Set Battery Load Simulator to 0.3 A. Verify voltage at FL6001 of 14.5 VDC. Adjust R5706 if necessary.

4. Set Battery Load Simulator to 1.3 A. Verify that charging voltage is reduced to 5 VDC (±2 V).

5. Disconnect 50 VDC Power Supply. Install Power Supply and calibrate per Section 4.

5-2-2 +40 V POWER SUPPLY MODULE TROUBLESHOOTING

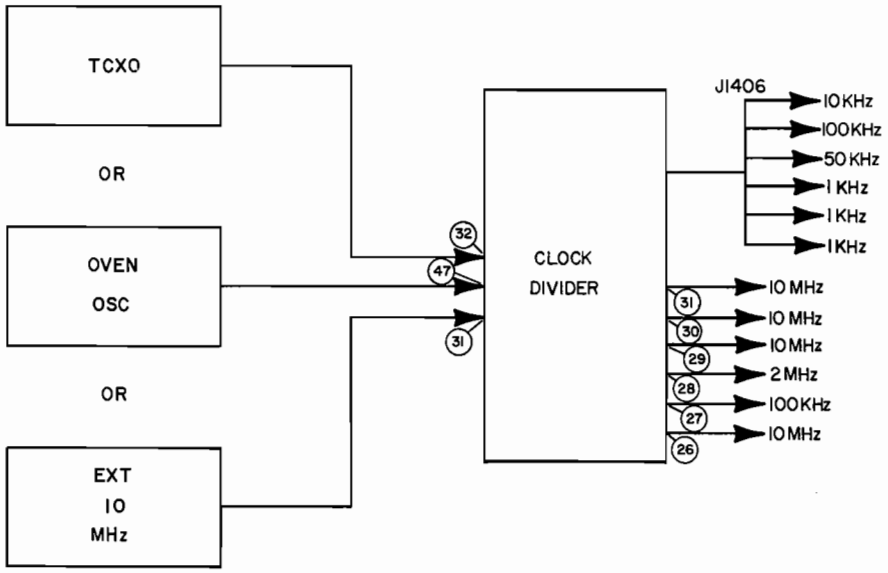
SPECIAL ACCESSORY EQUIPMENT REQ'D: 1 Digital Voltmeter---Any
1 Oscilloscope---Any

FIGURE REFERENCES: +40 V Power Supply Module (Section 6)
+40 V Power Supply Schematic (Section 7)
+40 V Power Supply Theory (Section 2)

TEST SET-UP DIAGRAM: N/A

STEP	PROCEDURE
1.	Verify +12 VDC and -12 VDC inputs at pins 1 and 2 of P5601.
2.	Verify frequency of approximately 38 kHz at pin 10 of U5601.
3.	Verify a 24 Vp-p square wave at collectors of Q5602 and Q5603.
4.	Verify +40 VDC (±4.5 V) at pin 3 of P5601.
5.	Disconnect all test equipment.

5-3 FREQUENCY STANDARD FUNCTIONAL BLOCK TROUBLESHOOTING



NOTE

Signals at coax connectors are provided in Table 5-1.

Figure 5-4 Frequency Standard Functional Block

5-3-1 CLOCK DIVIDER MODULE TROUBLESHOOTING

SPECIAL ACCESSORY EQUIPMENT REQ'D:
- 1 Oscilloscope---Any
- 1 Digital Voltmeter---Any
- 1 Signal Generator (Frequency Standard)---Capable of 10 MHz at 2V p-p
- 1 Frequency Counter---Capable of 10 MHz

FIGURE REFERENCES:
- Clock Divider Module (Section 6)
- Clock Divider Schematic (Section 7)
- Clock Divider Theory (Section 2)

TEST SET-UP DIAGRAM: N/A

STEP	PROCEDURE
1.	Verify +5 VDC at pin 8 of J1406.
2.	Verify 10 MHz input at J1401.
3.	Verify frequency outputs per schematic.
4.	Disconnect P1401 from J1401.
5.	Connect a 10 MHz signal of 2 Vp-p or greater to 10 MHz REF Connector on rear panel.
6.	Verify pin 9 of J1406 goes high.
7.	Disconnect 10 MHz signal from 10 MHz REF Connector. Reconnect P1401 to J1401.
8.	Using Frequency Counter and Oscilloscope verify reference frequency outputs as shown in Table 5-2.

Connection Points	Frequency Output	Signal Level (approximate)
J1402	10 MHz	.6 VDC, .2 VAC
J1403	10 MHz	1 VDC, 1.2 VAC
J1404	10 MHz	.8 VDC, 1.3 VAC
J1405	10 MHz	.8 VDC, 1.3 VAC
J1407	100 KHz	4V sq. wave
J1408	2 MHz	3.5 VAC
J1406-1	1 KHz	5V sq. wave
J1406-2	1 KHz	5V sq. wave
J1406-3	10 KHz	3.2V sq. wave
J1406-4	50 KHz	3.2V sq. wave
J1406-5	100 Hz	3.2V sq. wave
J1406-7	1 KHz	4.2V sq. wave

Table 5-3 Clock Divider Frequency Outputs

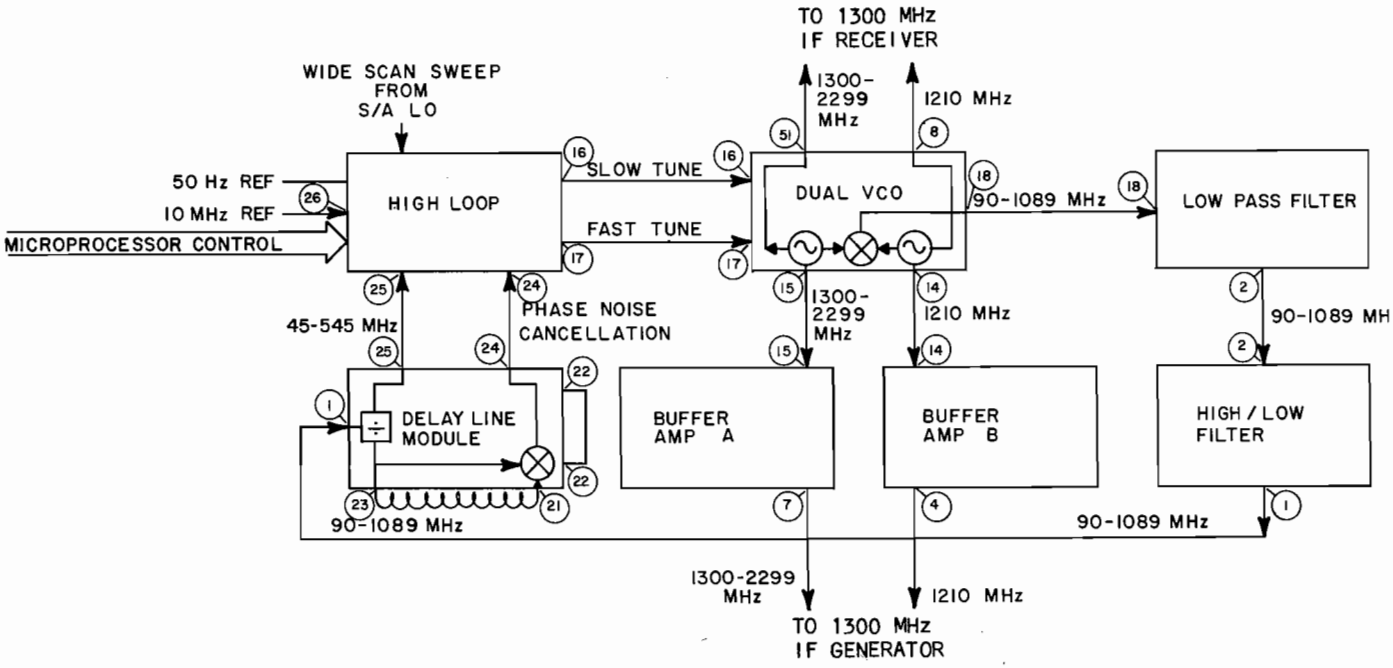
9. Disconnect all test equipment.

5-4 FREQUENCY SYNTHESIS FUNCTIONAL BLOCK TROUBLESHOOTING

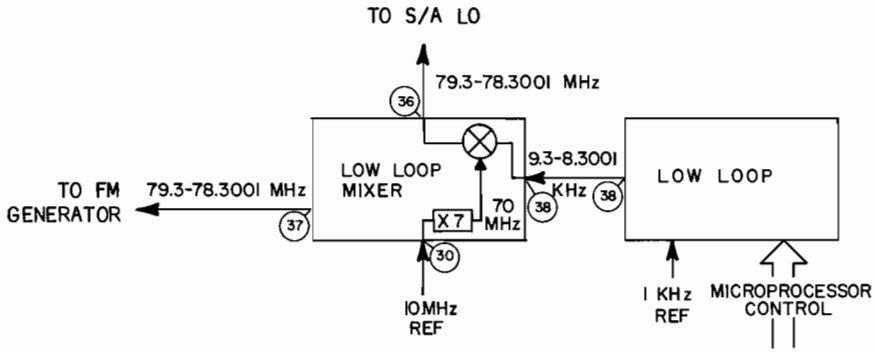
To troubleshoot the High Loop Section, the HIGH/LOW PASS FILTER Module must be bypassed. Therefore the best procedure to follow is to attempt the High Loop and Low Loop Calibration procedures in Section 4. After isolating the faulty module, proceed to Module troubleshooting.

NOTE

Signals at coax connectors are provided in Table 5-1.



High Loop Section



Low Loop Section

Figure 5-5 Frequency Synthesis Functional Block

5-4-1 HIGH LOOP MODULE TROUBLESHOOTING

SPECIAL ACCESSORY EQUIPMENT REQ'D:
- 1 Digital Voltmeter---Any
- 1 Oscilloscope---Any
- 1 Frequency Counter---Capable of 10 MHz

FIGURE REFERENCES:
- High Loop Module (Section 6)
- High Loop Schematic (Section 7)
- High Loop Theory (Section 2)

TEST SET-UP DIAGRAM: N/A

STEP	PROCEDURE
1.	Verify +12V, -12V, +5V and +40V inputs at appropriate pins of J2803.
2.	Verify 10 MHz and 50 Hz reference frequencies of J2802 and pin 11 of J2803, respectively.
3.	Verify 500 KHz at pin 12 of U2210 when ANALY DISPR Control is in 1k through 1M positions. Verify 500 KHz is not present in 2M through Full positions.
4.	Verify approximate 500 KHz at the collector of Q2220.
5.	If frequencies in Steps 3 and 4 are 500 KHz, voltage at pin 7 of U15B should be about 0V and voltage at pin 23 of J2803 should be +12V.
6.	The remainder of High Loop Module Troubleshooting consists of performing the High Loop Calibration procedure in Section 4 to isolate a faulty mode.

5-4-2 DUAL VCO MODULE TROUBLESHOOTING

The Dual VCO Module is deemed to be nonrepairable in the field. If the Dual VCO is confirmed as being faulty, it should be returned to IFR Systems Inc., factory for repair.

5-4-3 LOW PASS FILTER MODULE TROUBLESHOOTING

SPECIAL ACCESSORY EQUIPMENT REQ'D: 1 Tracking Generator---Capable of 1210 MHz at -20 dBm
1 Spectrum Analyzer---Capable of measuring 1210 MHz

FIGURE REFERENCES: Low Pass Filter Module (Section 6)
Low Pass Filter Theory (Section 2)

TEST SET-UP DIAGRAM: N/A

STEP	PROCEDURE
1.	Calibrate Spectrum Analyzer, set on 10 MHz/DIV dispersion, to Tracking Generator centered at 590 MHz at -20 dBm.
2.	Connect Low Pass Filter between Spectrum Analyzer and Tracking Generator.
3.	Adjust the seven screws on the side of the Low Pass Filter for the following: a. 3 dB cutoff at 1120 MHz (±10 MHz). b. Ripple less than 3 dB from 90 to 1090 MHz. c. 1210 MHz level is 45 dBc or more below carrier level.
4.	Reseal seven screws with Torque Seal or equivalent.
5.	Disconnect all test equipment.

5-4-4 HIGH/LOW PASS FILTER MODULE TROUBLESHOOTING

SPECIAL ACCESSORY EQUIPMENT REQ'D:
- 1 Function Generator---Capable of 1 KHz at ±10V
- 1 Spectrum Analyzer---Capable of measuring 1130 MHz
- 1 Tracking Generator---Capable of 1130 MHz at -30 dBm

FIGURE REFERENCES:
- High/Low Pass Filter Module (Section 6)
- High/Low Pass Filter Schematic (Section 7)
- High/Low Pass Filter Theory (Section 2)

TEST SET-UP DIAGRAM: N/A

STEP	PROCEDURE
1.	Calibrate Spectrum Analyzer to Tracking Generator at -30 dBm centered at 565 MHz on 50 MHz/Div dispersion.
2.	Connect Function Generator, set for a 1 kHz square wave at ±10 V, to FL601 on High/Low Pass Filter.
3.	Connect filter between Spectrum Analyzer and Tracking Generator.
4.	Verify that the crossover point is not more than 3 dB below the average level of the composite curve and that no point on the composite curve is more than 6 dB below the reference level of the Tracking Generator input.
5.	If necessary, identify the crossover point (it should be somewhere around 545 MHz) with an external Signal Generator. Mark the crossover point on the outside of the High/Low Pass Filter.

NOTE

The crossover point is marked on the module as calibrated at the IFR factory.

6.	Observe filter rolloff and verify that rolloff is at least 3 dB down from the crossover point at 50 MHz on either side of the crossover point.
7.	Set Spectrum Analyzer to 100 MHz/Div dispersion. Verify that composite curve is flat within 5 dB except at the crossover point.
8.	Disconnect all test equipment.

5-4-5 DELAY LINE MODULE TROUBLESHOOTING

SPECIAL ACCESSORY EQUIPMENT REQ'D:
- 1 Digital Voltmeter---Any
- 1 Tracking Generator---Capable of 634 MHz at -36 dBm
- 1 Spectrum Analyzer---Capable of 545 MHz at 0 dBm
- 1 Vector Voltmeter---Any (if available)
- 1 Oscilloscope---Any

FIGURE REFERENCES:
- Delay Line Module (Section 6)
- Delay Line Module Schematic (Section 7)
- Delay Line Module Theory (Section 2)

TEST SET-UP DIAGRAM: N/A

STEP PROCEDURE

1. Verify voltage inputs on J3003 as follows:

Pin # of J3003	Voltage
Pin 6	+12 V
Pin 1	-12 V
Pin 8	+5 V
Pin 9	+40 V

2. Verify +5 VDC at pin 5 of J3003 when 455 MHz or greater is selected on LCD and 0 V when 454 MHz or less is selected. Leave LCD set at 454 MHz or less.

3. Disconnect coax cables from J3005, J3002 and J3001.

4. Connect Tracking Generator, centered at 317 MHz at -36 dBm, to J3005.

5. Connect Spectrum Analyzer, set at 50 MHz/Div, to J3007. Verify a 0 dBm or greater output from 90 to 545 MHz.

6. Connect Spectrum Analyzer to J3008. Select low pass filters and verify output levels and cut-off points as listed below:

FREQ MHz ON LCD	CUT-OFF	OUTPUT LEVEL
0-50 MHz	140 MHz	0 dBm or greater
51-130 MHz	220 MHz	0 dBm or greater
131-256 MHz	346 MHz	0 dBm or greater
257-454 MHz	544 MHz	0 dBm or greater
455-477 MHz	346 MHz	Doesn't matter
478-999 MHz	544 MHz	Doesn't matter

STEP PROCEDURE

7. Connect delay line coax between J3007 and J3001.

8. Connect Spectrum Analyzer to Test Point TP2501 on board #1. Select low pass filters and verify output levels and cut-off points as listed below:

FREQ MHz ON LCD	CUT-OFF	OUTPUT LEVEL
0-50 MHz	140 MHz	-15 dBm or greater
51-130 MHz	220 MHz	-15 dBm or greater
131-256 MHz	346 MHz	-15 dBm or greater
257-454 MHz	544 MHz	-15 dBm or greater
455-477 MHz	Not critical	Doesn't matter
478-999 MHz	Not critical	Doesn't matter

9. Disconnect Tracking Generator from J3005.

NOTE

Many technicians will not have access to Vector Voltmeters. If this is the case, disregard Steps 10 through 12 and do the following to troubleshoot the phase-shift circuit:

(a) Leave all coaxes connected except J3006.

(b) Set SW2501 to TEST position.

(c) Observe TP2401 with Spectrum Analyzer and verify output level varies as R2530 is varied.

(d) Using Digital Voltmeter, observe output of MXR2501 (pin 3 or 4) and verify a voltage swing from approximately -0.5 VDC to +0.5 VDC.

(e) Verify the following approximate voltage levels on Q2503 and Q2505: collector - 11.3 VDC, base - 1.3 VDC, emitter - .6 VDC.

(f) Disconnect jumper coax between J3002 and J3008 and proceed with Step 13.

10. Connect equipment as shown in Figure 5-6.

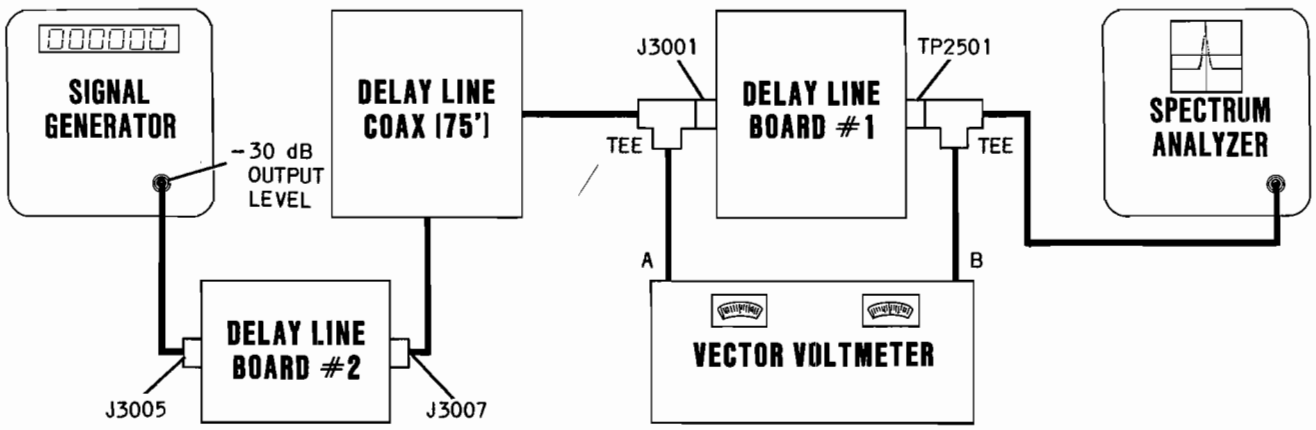


Figure 5-6 Phase-Shift Test Hookup

11. Set SW2501 to TEST position. Select each frequency given below and verify that the phase shift is variable over a 200° or greater range. Adjust phase test trimpot, R2530, from 0 to 30 VDC on wiper for phase test.

FREQ MHz ON LCD	SIGNAL GEN. FREQ	VECTOR VOLTMETER FREQ. RANGE
934 MHz	1024 MHz	300-600 MHz
500 MHz	590 MHz	175-350 MHz
454 MHz	544 MHz	300-600 MHz
50 MHz	140 MHz	100-200 MHz

12. Disconnect Vector Voltmeter and Spectrum Analyzer.

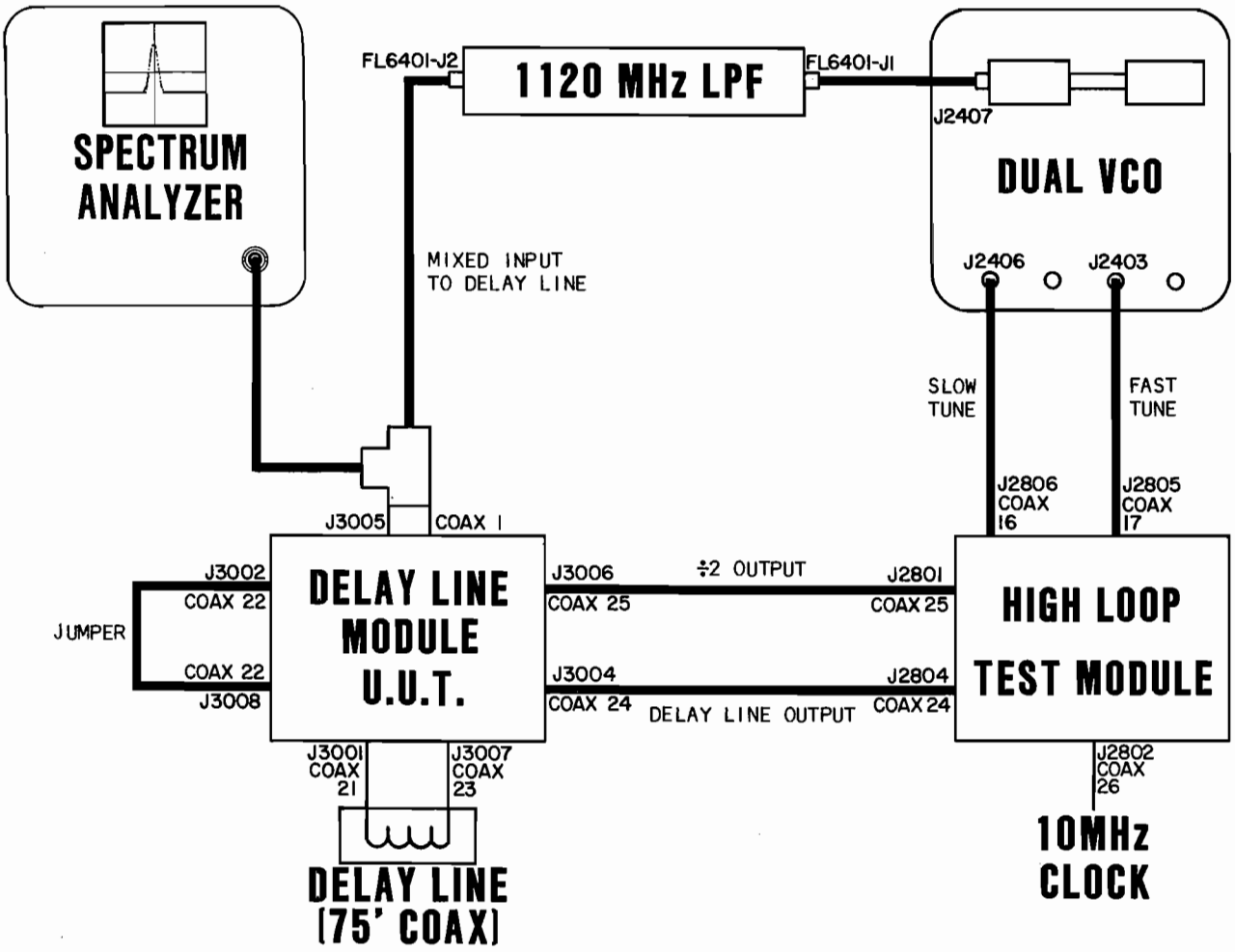


Figure 5-7 High Loop System Test Hookup

13. Connect Spectrum Analyzer to J3006. Set LCD to 50 MHz and Signal Generator to 140 MHz at -30dBm. Verify output on Spectrum Analyzer at 70 MHz is -5 dBm (±2dBm).

14. Connect jumper coax between J3008 and J3002.

15. Set SW2501 to RUN position. Verify voltage at base of Q2521 is 0 VDC (±5mV). Adjust R2565 if necessary.

16. Remove coax connectors from J3001 and J3002 and verify with Oscilloscope that collector of Q2610 goes from 0 to appproximately +30 VDC.

17. Connect High Loop System as shown in Figure 5-7. Set LCD to 50 MHz. Disconnect coax from J3004 and verify on Spectrum Analyzer that noise level 100 KHz from the 140 MHz signal jumps up 5dB or more.

18. Reconnect coax to J3004. Disconnect coax from J3001 and verify on Spectrum Analyzer that noise level 100 KHz from the 140 MHz signal jumps up 5dB or more.

19. Disconnect all test equipment.

5-4-6 BUFFER AMP A OR B TROUBLESHOOTING

SPECIAL ACCESSORY EQUIPMENT REQ'D: 1 Digital Voltmeter---Any
1 Spectrum Analyzer---Capable of 2300 MHz at +10 dBm

FIGURE REFERENCES: Buffer Amp Module (Section 6)
Buffer Amp Schematic (Section 7)

TEST SET-UP DIAGRAM: N/A

STEP	PROCEDURE
1.	Verify +12 VDC on FL1 of applicable Buffer Amp.
2.	Connect Spectrum Analyzer to output (J2) of applicable Buffer Amp.
3.	Set LCD to 000.0000 MHz and then step setting up through 990 MHz in 10 MHz steps. At each step, verify that the output of Buffer Amp A is at +4 to +10 dBm and that it steps in 10 MHz increments from 1300 to 2300 MHz. Verify that output of Buffer Amp B is +4 to +10 dBm at 1210 MHz for each step. Change S.A.T. resistor R6, if necessary, for proper amplitude.
4.	Disconnect all test equipment.

5-4-7 LOW LOOP MODULE TROUBLESHOOTING

SPECIAL ACCESSORY EQUIPMENT REQ'D:
1 Digital Voltmeter---Any
1 Frequency Counter---Capable of 9.3 MHz
1 Spectrum Analyzer---Capable of 9.3 MHz at -10 dBm

FIGURE REFERENCES:
Low Loop Module (Section 6)
Low Loop Schematic (Section 7)
Low Loop Theory (Section 2)

TEST SET-UP DIAGRAM: N/A

STEP	PROCEDURE
1.	Verify input voltages at J4003 as follows: pin 13 - +12 VDC pin 25 - -12 VDC pins 1 & 14 - +5 VDC
2.	Using Frequency Counter, verify a 1 KHz input at pin 11 of J4003.
3.	Connect DVM to R3103 (junction of R3103 and R3138).
4.	Set Front Panel LCD to XXX.0000 FREQ MHz. Verify 7.0 VDC (0.3V) on DVM. Tune L3102 if necessary.
5.	Set Front Panel LCD to XXX.9999 FREQ MHz. Verify 1.9 VDC (± 0.3V) on DVM. Tune L3102 if necessary. Repeat Step 4 if necessary. Repeat Step 4 if L3102 is tuned.
6.	Set Front Panel LCD to XXX.0000 FREQ MHz. Using Spectrum Analyzer connected to J4001, verify -10 to -12 dBm at 9.300 MHz.
7.	Disconnect Spectrum Analyzer from J4001. Connect Frequency Counter to J4001.
8.	At the following LCD settings (last four digits), verify the corresponding output frequency on Frequency Counter.

STEP PROCEDURE

LCD FREQ MHz Setting	Frequency Counter Reading
XXX.0000	9.3000 MHz
XXX.1111	9.1889 MHz
XXX.2222	9.0778 MHz
XXX.3333	8.9667 MHz
XXX.4444	8.8556 MHz
XXX.5555	8.7445 MHz
XXX.6666	8.6334 MHz
XXX.7777	8.5223 MHz
XXX.8888	8.4112 MHz
XXX.9999	8.3001 MHz

9. Disconnect all test equipment.

5-4-8 LOW LOOP MIXER MODULE TROUBLESHOOTING

SPECIAL ACCESSORY EQUIPMENT REQ'D:
- 1 Digital Voltmeter---Any
- 1 Spectrum Analyzer---Capable of 79.3 MHz at +12 dBm
- 1 Frequency Counter---Capable of 10 MHz

FIGURE REFERENCES:
- Low Loop Mixer Module (Section 6)
- Low Loop Mixer Schematic (Section 7)
- Low Loop Mixer Theory (Section 2)

TEST SET-UP DIAGRAM: N/A

STEP	PROCEDURE
1.	Verify +12 VDC at pin 6 of J1805.
2.	Using Frequency Counter, verify 10 MHz input at J1801.
3.	Using Spectrum Analyzer connected at TP1, verify approximate -20 dBm at 70 MHz.
4.	Set Front Panel LCD to XXX.0000 FREQ MHz.
5.	Using Spectrum Analyzer, verify approximate -12 dBm at 9.3 MHz input at J1802.
6.	Using Spectrum Analyzer connected at TP2, verify approximate -40 dBm at 79.3 MHz. Tune L1912, L1913, L1914, L1915 and L1916 for a maximum output level. Then detune L1908 as necessary to eliminate, or make as low as possible, the spur signal at 80.7 MHz.
7.	Using Spectrum Analyzer connected to J1803, verify a +4 to +12 dBm output at 79.3 MHz.
8.	Using Spectrum Analyzer connected to J1804, verify a +4 to +12 dBm output at 79.3 MHz.
9.	Disconnect all test equipment.

5-5 RECEIVER FUNCTIONAL BLOCK TROUBLESHOOTING

NOTE

Signals at coax connectors are provided in Table 5-1.

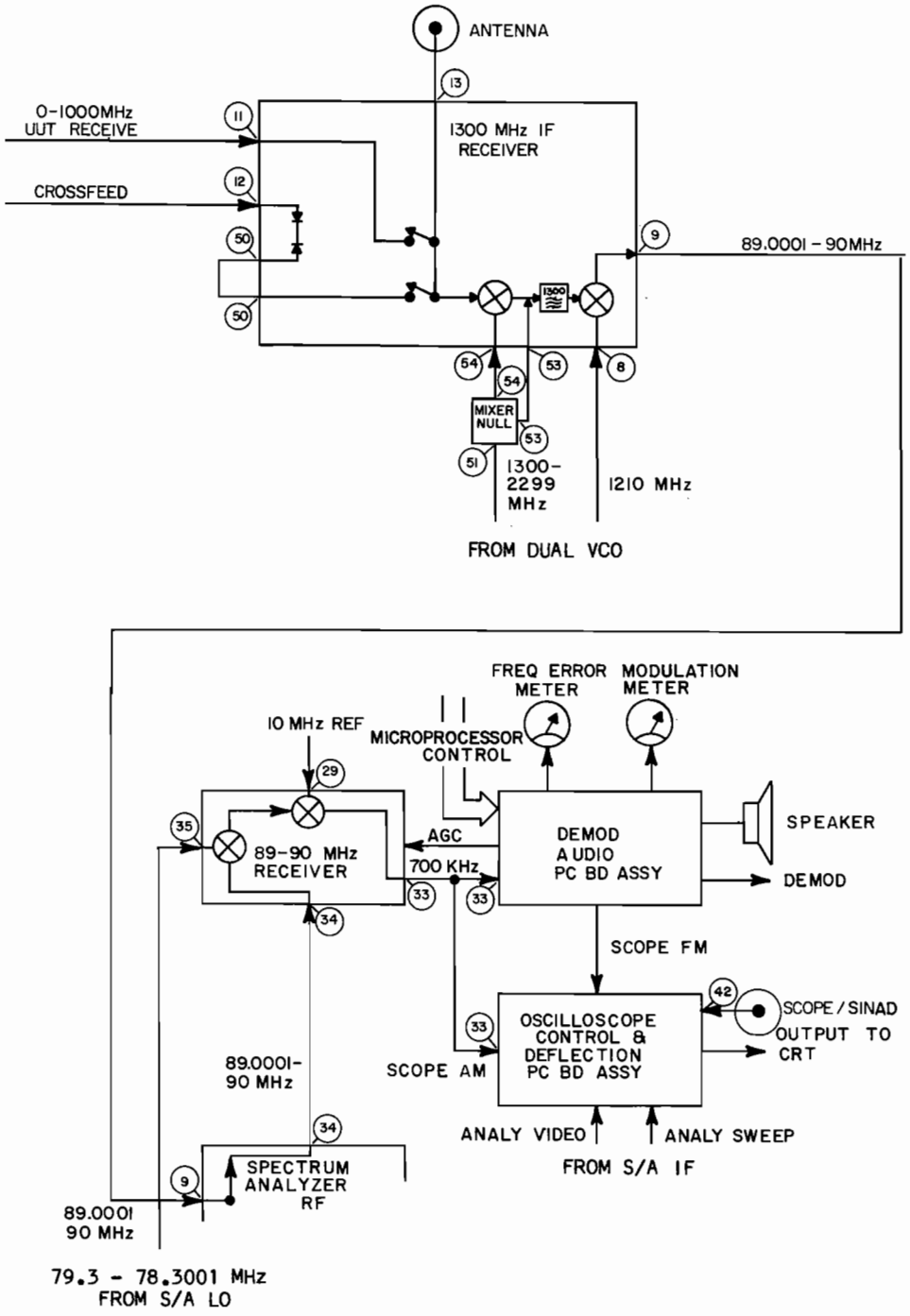


Figure 5-8 Receiver Functional Block

5-5-1 1300 MHz IF RECEIVER MODULE TROUBLESHOOTING

SPECIAL ACCESSORY EQUIPMENT REQ'D:
- 1 +12V Power Supply---Any
- 1 Digital Voltmeter---Any
- 1 Tracking Generator---Capable of 180 MHz at -20 dBm
- 1 Spectrum Analyzer---Capable of 1390 MHz
- 1 RF Generator---Capable of 850 MHz at -20 dBm
- 1 Frequency Counter---Capable of 1210 MHz

FIGURE REFERENCES:
- 1300 MHz IF Receiver Module (Section 6)
- 1300 MHz IF Receiver Schematic (Section 7)
- 1300 MHz IF Receiver Theory (Section 2)

TEST SET-UP DIAGRAM: N/A

STEP	PROCEDURE
1.	Verify +12V at FL1004.
2.	Set GEN/REC Switch to "GEN" and DUPLEX/SIMPLEX Switch to "DUPLEX". Verify +12 VDC on FL1006.
3.	Disconnect coax cable from J1006. Disconnect coax cable from input of Buffer Amp A and connect it to J1006. Verify inputs at J1001 and J1006 are +5 to +12 dBm at 1210 MHz.

NOTE

Inputs must be as close as possible to 1210 MHz for this procedure. Adjust C2003 on Dual VCO and use a Frequency Counter to verify 1210 MHz inputs (maximum tolerance of ± 0.5 MHz).

4.	Connect Tracking Generator, centered at 90 MHz at -20 dBm, to J1003.
5.	Connect Spectrum Analyzer, set at 5 MHz/Div, to J1002. Verify 90 MHz output at -14 to -17 dBm, and that bandwidth from 83 to 96 MHz is no more than 0.5 dB down from 90 MHz level. Tune 1300 MHz filter (Z1002) caps if necessary.
6.	Set DUPLEX/SIMPLEX Switch to "SIMPLEX". Verify OV on FL1006. Verify that output level on Spectrum Analyzer drops 20 dB or more.
7.	Set DUPLEX/SIMPLEX Switch to "DUPLEX". Verify +12VDC on FL1006.

8. Disconnect Tracking Generator from J1003. Disconnect Spectrum Analyzer from J1002. Connect Tracking Generator, still centered at 90 MHz at -20 dBm, to TP1301. Connect Spectrum Analyzer, centered at 1120 MHz and set at 5 MHz/Div dispersion, to J1001. Define 1120 MHz center accurately.

9. Connect +12VDC to J1002 through a 1 KΩ resistor. Verify that notch on Spectrum Analyzer is centered at 1120 MHz. Tune C1310 as necessary.

10. Disconnect Spectrum Analyzer from J1001. Disconnect Tracking Generator from TP1301. Disconnect +12VDC and 1 KΩ resistor from J1002. Disconnect coax cable from J1006 and reconnect it to buffer Amp A. Connect original coax cable (P1006) to J1006. Set LCD to 090.0000 FREQ MHz. Verify a 1390 MHz input at J1006 and a 1210 MHz input at J1001.

11. Connect RF Generator, set to 90 MHz at -20 dBm, to J1003. Connect Spectrum Analyzer to J1002 and verify a 90 MHz output. Note and record output level.

12. Set Front Panel ATTENUATOR Switch to 20 dB. Verify +12 VDC on FL1004. Verify that output level on Spectrum Analyzer at 90 MHz drops 20 dB (± 1.5 dB) from level in Step 11.

13. Set Front Panel ATTENUATOR Switch to 40 dB. Verify +12 VDC on FL1004 and FL1005. Verify that output level on Spectrum Analyzer at 90 MHz drops 20 dB (± 1.5 dB) from level in Step 12.

14. Set LCD to 850.0000 FREQ MHz. Set RF Generator to 850 MHz at -20 dBm. Repeat Steps 11 through 13.

15. Set ATTENUATOR Switch to 0 dB. Set DUPLEX/SIMPLEX Switch to "SIMPLEX". Verify 0V at FL1004, FL1005 and FL1006.

16. Disconnect RF Generator from J1003 and connect it, still set to 850 MHz at -20 dBm, to J1005. Apply +12 VDC to FL1003. Verify that output on Spectrum Analyzer at 90 MHz is -45 dB (± 3 dB).

17. Disconnect +12 VDC at FL1003. Verify that output on Spectrum Analyzer is at least 40 dB below level in Step 11.

18. Set RF Generator to 90 MHz at -20 dBm. Set LCD to 090.0000 FREQ MHz. Apply +12 VDC to FL1003. Verify that output on Spectrum Analyzer at 90 MHz is -45 dB (± 3 dB).

19. Disconnect +12 VDC at FL1003. Verify that output on Spectrum Analyzer at 90 MHz is at least 40 dB below level in Step 11.

20. Disconnect +12 VDC at FL1003 and connect to FL1002. Disconnect RF Generator from J1003 and connect it to J1004. Verify that output on Spectrum Analyzer at 90 MHz is -45 dB (± 3 dB.)

21. Disconnect +12 VDC from FL1002. Verify that output on Spectrum Analyzer at 90 MHz is at least 40 dB below level in Step 11.

22. Set RF Generator to 90 MHz at -20 dBm. Set LCD to 090.0000 FREQ MHz. Apply +12 VDC to FL1002. Verify that output on Spectrum Analyzer at 90 MHz is -45 dB (± 3 dB).

23. Disconnect +12 VDC from FL1002. Verify that output on Spectrum Analyzer at 90 MHz is at least 40 dB below level in Step 11.

24. Disconnect all test equipment.

5-5-2 89-90 MHZ RECEIVER TROUBLESHOOTING

SPECIAL ACCESSORY EQUIPMENT REQUIRED	1	Distortion Analyzer
	1	Digital Voltmeter – Any
	1	Tracking Generator – Capable of 180 MHz at -30 dBm
	1	Spectrum Analyzer – Capable fo 90 MHz at -30 dBm
	1	Frequency Counter – Capable of 10 MHz
	1	Signal Generator – Capable of 90 MHz at -110 dBm
FIGURE REFERENCES:		89-90 MHz Receiver Module (Section 6) 89-90 MHz Receiver Schematic (Section 7) 89-90 MHz Receiver Block Diagram (Section 2)
TEST SET-UP DIAGRAM:		N/A

STEP PROCEDURE

89.5 MHz Bandpass Test

1. Connect the 90 MHz Receiver module to the FM/AM-1500 frame at J3 and J4.

2. Set the following Spectrum Analyzer controls:

CONTROL	SETTING
Center Frequency	89.5 MHz
Scan Width	1 MHz/Div
Tracking Generator	ON (see
Tracking Generator Attenuation	-30 dBm

NOTE

If the Tracking Generator is an IFR A-7550 or A-8000 Spectrum Analyzer, the Tracking Generator is turned on through menu operation. See the A-7550 or A-8000 Operation Manual (IFR P/N: 1002-5301-000/1002-5401-000) for instructions.

3. Connect the Spectrum Analyzer to Test Point 1 (TP1).

4. Set the external Tracking Generator to the 89-90 MHz Receiver at J2.

5. Adjust L2907 through L2911 for maximum 89.5 MHz signal at ±1.5 MHz bandwidth 3 dB below peak on the Spectrum analyzer. Record this bandwidth in Table 5-5-2-1.

6. Verify level of 89.5 MHz is -44 dBm (±2 dB) for 6 dB IF Gain.

7. Connect the FM/AM-1500 LO (#35) to J1 on the 89-90 MHz Receiver.

STEP PROCEDURE

8. Set the following FM/AM-1500 Controls:

CONTROL	SETTING
(20) KEYBOARD	RF 300.5 (MHz) ENTER
(51) DISPLAY	METER
(6) DEV/PWR	SIG
(7) MODULATION	FM1

9. Adjust L2912 for maximum signal on the CRT display (50). the bandpass display on the Spectrum Analyzer should display a dip centered vertically on the CRT. Record the Maximum Signal level in Table 5-5-2-1.

Gain Test

10. Connect the Spectrum Analyzer output to J5 of the 89-90 MHz Receiver module.

11. Set the Spectrum Analyzer controls to the following:

CONTROL	SETTING
Center Frequency	700 kHz
SCAN WIDTH	100 kHz/Div
Input Attenuation	+10 dBm

12. Connect Signal Generator to J2 of the 89-90 MHz Receiver.

13. Set the following controls on the Signal Generator:

CONTROL	SETTING
Frequency	89.5 MHz
Amplitude	-60 dBm

14. Verify 700 kHz signal output at J5 is at least +2 dBm on the Spectrum Analyzer for AM1, AM2 and FM2. Verify no signal in SSB. Record the Signal level in each mode in Table 5-5-2-1.

IF Filter Selectivity

15. Connect J2 and J5 on the 89-90 MHz Receiver to the FM/AM-1500.

16. Connect the Audio Distortion Analyzer Input to the DEMOD OUTPUT Connector (25).

17. Connect the Audio Distortion generator output to the External FM Connector of the Signal Generator. the voltage level should be approximately 1.4 VRMS.

18. Set the following Signal Generator controls:

CONTROL	SETTING
Frequency	300.5 MHz
AMPLITUDE	-50 dBm
MODULATION	External FM

19. Connect the Signal Generator output to the ANTENNA Connector (56).

STEP	PROCEDURE

20. Set the following Audio Distortion Analyzer controls:

CONTROL	SETTING
MODULATION	1 kHz
LOW-PASS FILTER	80 kHz

21. Set the Deviation Control on the Signal Generator to 6 kHz.

22. Set the following FM/AM-1500 Controls:

CONTROL	SETTING
(7) MODULATION	FM1
(51) DISPLAY	ANALY
(38) ANALY DISPR	.1M Hz/DIV

23. Adjust L2913, L2915, C2954, C2956, C2958 and C2960 for less than 1% distortion through the 15 kHz Bandwidth filters. Record the distortion level at each adjustment point in Table 5-5-2-1.

24. Adjust L2905 and L2916 for maximum level on the SIG METER Display on the CRT (50).

25. Set the MODULATION CONTROL (7) to FM4.

26. Set the frequency on the Audio Distortion Analyzer to 20 kHz.

27. Set the deviation on the Signal Generator to 25 kHz.

28. Verify % distortion from the 200 kHz Bandwidth Filter. Record the distortion level in Table 5-5-2-1.

29. Set the MODULATION Control (7) to AM1.

30. Set the Modulation Frequency of the Audio Distortion Analyzer to 1 kHz.

31. Set the following Signal Generator controls:

CONTROL	SETTING
MODULATION	External AM.
MODULATION	80 %

32. Adjust C2962, C2964, C2966 and C2968 for 1.3% distortion through the 6 kHz Bandwidth Filters. Record the distortion level at each adjustment point in Table 5-5-2-1.

STEP PROCEDURE

Sensitivity Test

33. Set the MODULATION Control (7) to FM1.

34. Set the following Signal Generator controls:

CONTROL	SETTING
MODULATION	External FM.
DEVIATION	3.33 kHz
AMPLITUDE	-101 dBm

35. Set the following Audio Distortion Analyzer controls:

CONTROL	SETTING
MODULATION	1 kHz
LEVEL	SINAD

36. Verify at least 10 dB SINAD level on the Audio Distortion Analyzer. Record the Distortion Level in Table 5-5-2-1.

37. Disconnect all equipment from FM/AM-1500 and disconnect the 89-90 MHz Receiver.

5-5-3 DEMOD AUDIO PC BOARD TROUBLESHOOTING

SPECIAL ACCESSORY EQUIPMENT REQ'D:
1 Digital Voltmeter---Any
1 Frequency Counter---Capable of 10 KHz

FIGURE REFERENCES:
Demod Audio PC Board (Section 6)
Demod Audio PC Board Schematic (Section 7)
Demod Audio PC Board Theory (Section 2)

TEST SET-UP DIAGRAM: N/A

STEP	PROCEDURE
1.	Verify +12 VDC and -12 VDC at pins 1 and 26, respectively, of P4701. Also verify +5.1V at junction of R4733 and CR4706.
2.	Using Frequency Counter, verify 1 KHz input at pin 3 of P4701 and 10 KHz input at P4703.
3.	Since the Demod Audio PC Board is used in many calibration procedures, it would be redundant to include a separate listing of troubleshooting procedures here. The best method of troubleshooting the Demod Audio PC Board is to troubleshoot it during an applicable calibration procedure.

5-5-4 OSCILLOSCOPE CONTROL AND DEFLECTION PC BOARD

SPECIAL ACCESSORY EQUIPMENT REQ'D: 1 Digital Voltmeter---Any

FIGURE REFERENCES: Oscilloscope Control and Deflection PC Board (Section 6)
Oscilloscope Control and Deflection PC Board Schematic (Section 7)
Oscilloscope Control and Deflection PC Board Theory (Section 2)

TEST SET-UP DIAGRAM: N/A

STEP	PROCEDURE
1.	Using DVM, verify +12 VDC and -12 VDC at pins 2 and 4, respectively, of P5103.
2.	The remainder of Oscilloscope Control and Deflection PC Board troubleshooting consists of performing the Oscilloscope Calibration procedure in Section 4 to isolate a faulty mode.

5-6 GENERATE FUNCTIONAL BLOCK TROUBLESHOOTING

NOTE

Signals at coax connectors are provided in Table 5-1.

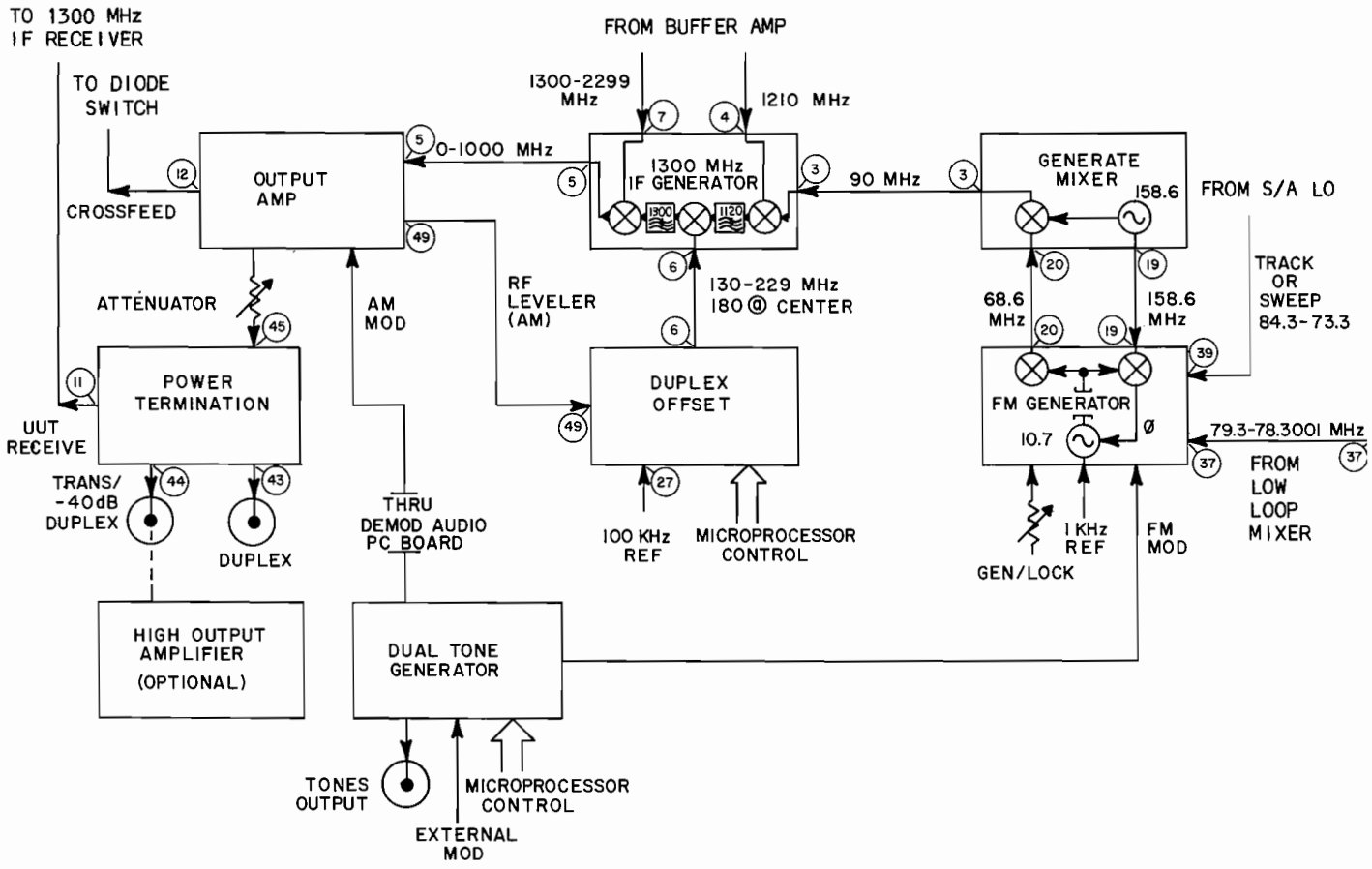


Figure 5-9 Generate Functional Block

5-6-1 FM GENERATOR MODULE TROUBLESHOOTING

SPECIAL ACCESSORY EQUIPMENT REQ'D:
1 Digital Voltmeter---Any
1 Frequency Counter---Capable of 10.7 MHz
1 Spectrum Analyzer---Capable of 169.3 MHz at -19 dBm

FIGURE REFERENCES:
FM Generator Module (Section 6)
FM Generator Schematic (Section 7)
FM Generator Theory (Section 2)

TEST SET-UP DIAGRAM: N/A

STEP	PROCEDURE
1.	Using DVM, verify +12 VDC, -12 VDC and +5 VDC at pins 6, 1 and 8 of J4203.
2.	Using Frequency Counter, verify 1 KHz at pin 5 of J4203.
3.	Rotate GEN/LOCK Control out of "LOCK" position to approximate mid-range. Using DVM, verify +2.9 VDC ($\pm$ 0.1V) at TP5. If necessary, adjust R3366.
4.	Using Frequency Counter, verify 10.7 MHz ($\pm$ 2 KHz) at TP1. If necessary, adjust C3367.
5.	Rotate GEN/LOCK Control fully cw and ccw (but not in "LOCK"). Verify a $\pm$ 30 KHz swing on VCO (10.7 MHz) frequency at TP1. If necessary, adjust R3366.
6.	Using Spectrum Analyzer, verify 10.7 MHz at approximately -35 dBm at TP1.
7.	Using DVM, verify $>$ -0.8 VDC at anode of CR3307.
8.	Set DISPLAY Control to any position except "TRACK" or "SWEEP".
9.	Using Spectrum Analyzer, verify a 68 MHz signal at approximately -13 dBm at J4206.
10.	Set DISPLAY Control to "TRACK" or "SWEEP".
11.	Disconnect coax from J4201.

12. Using Spectrum Analyzer, verify a 68 MHz output at approximately -13 dBm at J4206.

NOTE

This step verifies that the input switches from J4201 to J4202.

13. Set FM/AM-1500 controls as follows:

CONTROL	SETTING
(28) Tone 1 FM/OFF/AM	"FM"
(21) LCD	1000.0 Hz TONE 1
(33) TONE 1	Fully cw

14. Using Spectrum Analyzer at J4206, verify that FM deviation varies as TONE 1 Control is varied.

15. Using Spectrum Analyzer at TP3, verify a 169.3 MHz signal at approximately -40 dBm.

16. Using Spectrum Analyzer at TP4, verify a 169.3 MHz signal at approximately -19 dBm.

17. Rotate GEN/LOCK Control to "LOCK". Verify that VCO phase-locks at 10.7 MHz by observing TP1 with Spectrum Analyzer.

18. Using Frequency Counter, verify 1 KHz at TP2.

19. Disconnect all test equipment.

5-6-2 GENERATOR MIXER MODULE TROUBLESHOOTING

SPECIAL ACCESSORY EQUIPMENT REQ'D:
1 Digital Voltmeter---Any
1 Spectrum Analyzer---Capable of 158.6 MHz at +12 dBm
1 Tracking Generator---Capable of 192 MHz at -30 dBm

FIGURE REFERENCES:
Generator Mixer Module (Section 6)
Generator Mixer Schematic (Section 7)
Generator Mixer Theory (Section 2)

TEST SET-UP DIAGRAM: N/A

STEP	PROCEDURE
1.	Using DVM, verify +12 VDC on pin 6 of J4404.
2.	Set DISPLAY Control to any position except "TRACK" or "SWEEP".
3.	Using Spectrum Analyzer connected to TP5, verify a 158.6 MHz signal at approximately -15 dBm.
4.	Using Spectrum Analyzer connected to J4402, verify a 158.6 MHz signal at +5 to +12 dBm. Adjust C3436 if necessary.
5.	Connect a Tracking Generator centered on 74 MHz at -13 dBm to J4401.
6.	Using Spectrum Analyzer connected to TP1, verify maximum output level at 74 MHz and -40 dBm typical level. If necessary, adjust R3412 for maximum voltage level at TP2 and adjust L3402, L3404, L3406, L3408 and L3410 for maximum output level.
7.	Observe that filter tunes from 74 MHz to 63 MHz within ± 1 dB. Adjust R3412 if necessary.
8.	Set filter center frequency to 68.6 MHz. Adjust R3412 if necessary.
9.	Disconnect Tracking Generator from J4401.
10.	Adjust L3428 flush with the top of can of Generator Mixer Module.
11.	Connect Tracking Generator, centered at 96 MHz, at -30 dBm, to TP4.

12. Using Spectrum Analyzer connected to J4403, verify maximum output level of 96 MHz at -30 dBm typical. If necessary, adjust R3423 for maximum voltage on TP3 and adjust L3417, L3419, L3421, L3423, L3425 and L3427 for maximum output level.

13. Using Spectrum Analyzer, observe that filter tunes from 95 MHz to 84 MHz within ± 1 dB.

14. Set filter center frequency to 74 MHz by adjusting R3423.

15. Observe notch in center frequency and adjust L3428 to center it at 74 MHz.

16. Set filter center frequency to 90 MHz by adjusting R3423.

17. Disconnect Tracking Generator from TP4.

18. Connect coaxes to J4401 and J4402.

19. Using Spectrum Analyzer connected at J4403, verify output signal of 90 MHz at about -20 dBm. Adjust R3412, R3423 and R3436, if necessary.

20. Set DISPLAY Control to "SWEEP". Verify +12 VDC at pin 9 of J4404.

21. Using Spectrum Analyzer connected at J4403, verify signal is flat within 0.5 dB and output is within 1 dB of that in Step 19. Adjust R3413, R3415, R3417 and R3421, if necessary.

22. Disconnect all test equipment.

5-6-3 1300 MHz IF GENERATOR MODULE TROUBLESHOOTING

SPECIAL ACCESSORY EQUIPMENT REQ'D:
- 1 Digital Voltmeter---Any
- 1 Power Supply---Capable of +12 VDC
- 1 1 KΩ, ¼ W Resistor---Any
- 1 Spectrum Analyzer---Capable of 2600 MHz
- 1 Tracking Generator---Capable of 2300 MHz
- 1 20 dB removable test point---See Appendix D
- 2 Signal Generators---Capable of 90 MHz and 180 MHz

FIGURE REFERENCES:
- 1300 MHz IF Generator Module (Section 6)
- 1300 MHz IF Generator Schematic (Section 7)
- 1300 MHz IF Generator Theory (Section 2)

TEST SET-UP DIAGRAM: N/A

STEP PROCEDURE

1. Set FM/AM-1500 front panel controls as follows:

CONTROL	SETTING
(19) GEN/REC	"GEN"
(18) DUPLEX/SIMPLEX	"SIMPLEX"

2. Disconnect coax connectors from J1201, J1202, J1203, J1204 and J1205.

3. Using DVM, verify +12 VDC at FL1201 and FL1202.

4. Using external Power Supply, apply +12VDC through a 1 KΩ, ¼ W resistor to J1202.

5. Connect Tracking Generator, set at -30 dBm, to J1201.

6. Using a removable 20 dB test point and a Spectrum Analyzer, observe TP1603. Center Spectrum Analyzer on 1120 MHz. (Verify center against a known standard.) Verify 1120 MHz signal level is -25 dBm (+5dB) and the bandwidth is 22 MHz with ± 3 dB ripple. Adjust Z1201 bandpass filter as necessary.

7. Remove 1 KΩ resistor from J1202 and connect a Signal Generator, set at 90 MHz at -15 dBm, to J1202.

8. Remove Tracking Generator from J1201 and connect coax from Buffer Amp B to J1201. (Verify signal into J1201 is 1210 MHz at +5 to +10 dBm.)

9. Connect a second Signal Generator, set at 180 MHz at -15 dBm, to J1203.

10. Observe Spectrum Analyzer, still connected at TP1603 with a removable 20 dB test point, and verify an 1120 MHz output at -15 to -5 dBm.

11. Disconnect all test equipment.

12. Tune the two 1210 MHz outputs on the Dual VCO to 1120 MHz by adjusting C2003 on Dual VCO Module. Verify both outputs are greater than +5dBm. Connect one output to TP1603 and the other output to J1204.

13. Connect Tracking Generator, set at -12dBm, to J1203.

14. Center Spectrum Analyzer on 180 MHz (verify with known good source) and connect to J1205. Observe 180 MHz signal and verify level is -30 to -25 dBm. Verify bandwidth is 112 MHz with ± 2.5 dB ripple.

15. Disconnect all test equipment.

16. Tune the Dual VCO 1210 MHz outputs to 1210 MHz at +5 to +10 dBm. Connect one output to J1201.

17. Connect one Signal Generator, set at 90 MHz at -15 dBm, to J1202.

18. Connect second Signal Generator, set at 180 MHz at -15 dBm, to J1203.

19. Select 005.0000 FREQ MHz on LCD (21). Connect coax from Buffer Amp A to J1204. Verify signal input is 1305 MHz at +5 to +10 dBm.

20. Connect Spectrum Analyzer to J1205. Verify 5 MHz signal level is -25 to -20 dBm. Note level.

21. Observe the 1305 MHz signal at J1205. Verify signal level is 30 dBc, or greater, below the 5 MHz output level.

22. Select 999.0000 FREQ MHz on LCD (21). Verify signal input at J1204 is 2299 MHz.

23. Observe the 999 MHz signal output at J1205. Verify level is -28 dBm or greater.

24. Select 650.0000 FREQ MHz on LCD (21). Observe Spectrum Analyzer, still connected to J1205, signal at 650 MHz. Note level.

25. Observe 2600 MHz harmonic signal and verify that level is 35 dBc, or greater, below the 650 MHz level.

26. Disconnect all test equipment.

5-6-4 DUPLEX OFFSET MODULE TROUBLESHOOTING

SPECIAL ACCESSORY EQUIPMENT REQ'D:
1 Digital Voltmeter – Any
1 Spectrum Analyzer – Capable of 180 MHz at -4 dB
1 Frequency Counter – Capable of 100 kHz

FIGURE REFERENCES:
Duplex Offset Module (Section 6)
Duplex Offset Schematic (Section 7)
Duplex Offset Block Diagram (Section 2)

TEST SET-UP DIAGRAM: N/A

STEP PROCEDURE

1. Ensure 9-pin connector on the clock divider module is connected to the test High Lock Loop front panel clock.
2. Connect the 100 kHz reference (J7) on the Clock Divider to J3 on the Duplex Offset module.
3. Connect +12 VDC through a 1K ohm resistor to J4 on the Duplex Offset module.
4. Connect the 25-pin connector (J2) on the Duplex Offset module to the High Lock Loop Front Panel "DUPLEX OFFSET".
5. Connect J1 on the Duplex Offset module to the Spectrum Analyzer.
6. Connect the DVM between ground and the junction of R50 and R54 on the Duplex Offset board.

<u>VCO Tuning</u>

7. Switch on High Lock Loop power.
8. Set the 1500 High Lock Loop and Duplex Offset thumbwheels to '180.000'.
9. Adjust L5 on the Duplex Offset PC Board until the tune voltage on the Digital Voltmeter reads +1 VDC (+/-0.3 V).
10. Set the High Lock Loop and Duplex Offset thumbwheels to '130.01'.
11. Adjust L2 on the Duplex Offset PC Board until the tune voltage on the Digital Voltmeter reads +1.0 VDC (+/-0.3V).
12. Set the High Lock Loop and Duplex Offset thumbwheels to '179.99'.
13. Verify tune voltage on the Digital Voltmeter is .LE. +19 VDC.

VCO Output

14. Set the High Lock Loop and Duplex Offset thumbwheels to '180.00'.

15. Set the following controls on the Spectrum Analyzer:

CONTROL	SETTING
Center Frequency	180.0 MHz
Input Attenuator	30 dB
SCAN WIDTH	10 MHz/Div

16. Verify Duplex Offset RF output from J1 is .GE. -7 dBm.

17. Set the DUPLEX/SIMPLEX Switch (18) to SIMPLEX to remove the +12 VDC to the 1K resistor.

18. Verify RF level decreases at least 45 dB from level at Step 16.

19. Set the DUPLEX/SIMPLEX Switch (18) to DUPLEX.

20. Disconnect Spectrum Analyzer and connect J1 to the input on the Frequency Counter.

21. Step through each OFFSET DIGIT from '130.1' to '229.99' on the High Lock Loop.

22. Verify thumbwheel frequency setting matches Frequency Counter.

23. Verify phase lock light on High Lock Loop remains OFF as the frequency is changed.

24. Disconnect Digital Voltmeter and Frequency Counter..

Residual Output

25. Connect J1 to the input on the Modulation Meter.

26. Set the following controls on the Modulation Meter:

CONTROL	SETTING
HIGH-PASS	300 Hz
LOW-PASS	3 kHz
DEVIATION	10 kHz
TUNING	AUTO
PK-PK	2

27. Step '130.00' to '230.00' in 10 MHz steps and '179.99' and '229.99' on the High Lock Loop thumbwheels.

28. Verify deviation of Residual FM modulation is .LE. 0.04 kHz.

29. Disconnect all test equipment.

Environmental Testing

NOTE

Steps 30 and 31 must be done at both specified temperatures (0° C and 50° C).

30. Test the Duplex Offset module maintains phase lock of all digits at 0° C and 50° C.

31. Repeat Steps 1 through 29.

32. Install shields on the Duplex Offset PC Board assembly.

33. Repeat Steps 1 through 29 using installed shields.

Final Checkout

34. Verify Duplex Offset level on Coax #6 between -8 and -4 dBm at 180 MHz.

35. Verify Duplex Offset level in RECEIVE mode drops at least 45 dB.

36. Verify Duplex digits from 00 to ±49.99 MHz.

5-6-5 OUTPUT AMPLIFIER MODULE TROUBLESHOOTING

SPECIAL ACCESSORY EQUIPMENT REQ'D:
- 1 Tracking Generator---Capable of 1000 MHz at -30 dBm
- 1 Spectrum Analyzer---Capable of 1000 mHz at -10 dBm
- 1 Digital Voltmeter---Any

FIGURE REFERENCES:
- Output Amplifier Module (Section 6)
- Output Amplifier Schematic (Section 7)
- Output Amplifier Theory (Section 2)

TEST SET-UP DIAGRAM: N/A

STEP	PROCEDURE
1.	Using DVM, verify - 12 VDC at FL802.
2.	Check voltages at FL801 and FL803 per logic table 2-1 in Demod Audio PC Board Detailed Theory.
3.	Apply +12 VDC at FL801 and 0V at FL803.
4.	Connect a Tracking Generator, set at -30 dBm from 0 - 1000 MHz, to J801.
5.	Using Spectrum Analyzer connected to J803, verify +8 to +14 dBm from 0 - 100 MHz. Adjust R928, C915, C927 and C931 as necessary.
6.	Increase output level of Tracking Generator to -15 dBm. Verify output at J803 is greater than +20 dBm from 100 KHz to 1000 MHz.
7.	Adjust output of Tracking Generator to -25 dBm.
8.	Apply -12 VDC to FL804. While observing J802 with a Spectrum Analyzer, verify output level increases at least 6 dB.
9.	Apply +12 VDC to FL804. Verify output level drops at least 30 dB.
10.	Connect Spectrum Analyzer to J804. Apply +12 VDC to FL803 and verify a -10 to -32 dBm output from 100 KHz to 1000 MHz. Note and record level.
11.	Remove +12 VDC from FL803 and verify an output level at least 35 dB below level noted in Step 10.
12.	Disconnect all test equipment.

5-6-6 POWER TERMINATION MODULE TROUBLESHOOTING

SPECIAL ACCESSORY EQUIPMENT REQ'D:
- 1 Tracking Generator---Capable of 1000 MHz at 0 dBm
- 1 Spectrum Analyzer---Capable of 1000 MHz at 7 dBm
- 1 Signal Generator---Capable of 10 W at 806 MHz
- 1 Digital Voltmeter---Any

FIGURE REFERENCES:
- Power Termination Module (Section 6)
- Power Termination Schematic (Section 7)
- Power Termination Theory (Section 2)

TEST SET-UP DIAGRAM: N/A

STEP	PROCEDURE
1.	Connect Tracking Generator, set at 0 dBm over 0 - 1000 MHz range, to J6201.
2.	Using Spectrum Analyzer, observe output at J6203 and verify a -6.5 dBm (± 0.5 dB) level from 0 - 1000 MHz.
3.	Apply +12 VDC to FL6201. Using Spectrum Analyzer, observe output at J6202 and verify a 6.5 dBm (± 0.5 dB) output level from 0 - 1000 MHz.
4.	Remove +12 VDC from FL6201. Verify output level at J6202 is 40 dBm (± 0.5 dB) less than level observed in Step 3. If necessary, trim C6204 and R6208.
5.	Disconnect Tracking Generator from J6201. Connect Tracking Generator, set at 0 dBm from 0 - 1000 MHz, to J6202.
6.	Using Spectrum Analyzer, verify output at J6204 is -55 dBm (± 1.5 dB) from 0 - 1000 MHz. If necessary, trim C6203 and R6206.
7.	Disconnect Tracking Generator and Spectrum Analyzer.

8. Connect a Signal Generator to J6202 at the following frequencies and power levels. Using a DVM, verify approximate voltage levels at FL6203 and FL6204 as follows:

Input at J6202	Voltage at FL6203	Voltage at FL6204
10W @ 150 MHz	2.65 VDC	3.62 VDC
10W @ 806 MHz	2.65 VDC	2.73 VDC

NOTE

Voltages in step 8 are approximate and only give an indication that the circuit is operating properly.

9. Disconnect all test equipment.

5-6-7 DUAL TONE GENERATOR PC BOARD TROUBLESHOOTING

SPECIAL ACCESSORY EQUIPMENT REQ'D:
1 Digital Voltmeter---Any
1 Frequency Counter---Capable of 1.67772 MHz

FIGURE REFERENCES:
Dual Tone Generator PC Board (Section 6)
Dual Tone Generator Schematic (Section 7)
Dual Tone Generator PC Board Theory (Section 2)

TEST SET-UP DIAGRAM: N/A

STEP	PROCEDURE
1.	Verify +12 VDC, -12 VDC and +5 VDC at pins 25, 26 and 1, respectively of P4501.
2.	Using Frequency Counter, verify 1.67772 MHz at pin 11 of U4525 and at the collector of Q4503.
3.	The remainder of Dual Tone Generator PC Board troubleshooting consists of performing the Dual Tone Generator Calibration procedures in Section 4 to isolate a faulty mode.

5-6-8 HIGH OUTPUT AMPLIFIER MODULE TROUBLESHOOTING

SPECIAL ACCESSORY EQUIPMENT REQ'D: 1 Digital Voltmeter---Any
1 Spectrum Analyzer---Capable of 100 MHz at +20 dB

FIGURE REFERENCES: High Output Amplifier Module (Section 6)
High Output Amplifier Schematic (Section 7)
High Output Theory (Section 2)

TEST SET-UP DIAGRAM: N/A

STEP	PROCEDURE
1.	Set GEN/REC Switch to "GEN" and DISPLAY Control to any position except "TRACK" or "SWEEP". Verify +12 VDC at EXT AMP Connector.
2.	Connect High Output Amplifier to EXT AMP Connector and TRANS/-40 dB DUPLEX Connector.
3.	Select 100.0000 FREQ MHz on LCD. Rotate RF Output Control to 0 dBm. Using external Spectrum Analyzer connected to J7303, verify +20 dB (± 2 dB) output level at 100 MHz.
4.	Set GEN/REC Switch to "REC". Verify no output signal at J7303.
5.	Disconnect all test equipment.

5-7 SPECTRUM ANALYZER FUNCTIONAL BLOCK TROUBLESHOOTING

NOTE

Signals at coax connectors are provided in Table 5-1.

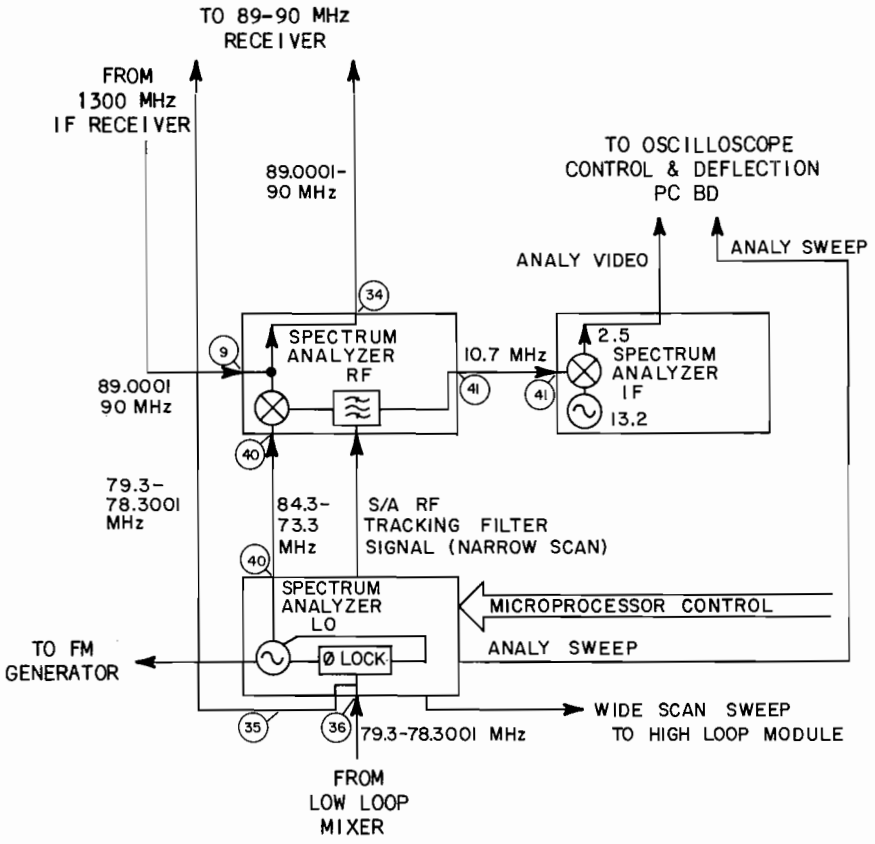


Figure 5-10 Spectrum Analyzer Functional Block

5-7-1 SPECTRUM ANALYZER IF MODULE TROUBLESHOOTING

SPECIAL ACCESSORY EQUIPMENT REQ'D:
- 1 Digital Voltmeter---Any
- 1 Spectrum Analyzer---Capable of 2.5 MHz at -19 dBm
- 1 Tracking Generator---Capable of 5 MHz at -20 dBm
- 1 RF Generator---Capable of 10.7 MHz at -20 dBm
- 1 Frequency Counter---Capable of 13.2 MHz

FIGURE REFERENCES:
- Spectrum Analyzer IF Module (Section 6)
- Spectrum Analyzer IF Schematic (Section 7)
- Spectrum Analyzer IF Theory (Section 2)

TEST SET-UP DIAGRAM: N/A

STEP	PROCEDURE
1.	Verify +12 VDC and -12 VDC at pins 6 and 1 of J5402.
2.	Verify +12 VDC at pin 5 of J5402 on wide scan (2M through FULL settings of ANALY DISPR Control).
3.	Verify that Q3904 and Q3905 switch on and off as pin 5 of J5402 goes high and low.
4.	Set dB/DIV Switch in 1 dB position and verify +12 VDC at pin 3 of J5402.
5.	Disconnect P5401 from J5401.
6.	Using Frequency Counter, verify 13.2 MHz at emitter of Q3902.
7.	Connect Tracking Generator, centered at 2.5 MHz to -20 dBm, to TP1.
8.	Connect Spectrum Analyzer to TP2 (use a DC block). Center Spectrum Analyzer at 2.5 MHz. Verify a -30 dBm level for 30 KHz (± 10 KHz) bandwidth. Tune L3905, L3906, L3907, L3908, L3911, L3912, L3913 and L3914. Adjust R3938 for maximum gain.
9.	Disconnect Tracking Generator from TP1.
10.	Connect RF Generator, set at -20 dBm at 10.7 MHz, to J5401. Verify output on Spectrum Analyzer of -22 dBm at 2.5 MHz. Adjust R3938 as necessary.
11.	Set ANALY DISPR Control to 2M. Verify output on Spectrum Analyzer of -19 dBm at 2.5 MHz. Adjust R3919 as necessary.

12. Disconnect Spectrum Analyzer. Set ANALY DISPR Control to 1M and dB/DIV Switch to 10 dB. In the following steps, set DISPLAY Control to ANALY or SCOPE depending on whether an analyzer level or scope display is desired.

13. Set RF Generator to OFF. Verify signal on CRT at -108 dB line or -0.78V on scope. Adjust R3961 as necessary.

14. Set RF Generator to -30 dBm at 10.7 MHz. Verify signal on CRT at -40 dB line or +0.6 VDC on scope. Adjust R3959 as necessary.

15. Set RF Generator to -20 dBm at 10.7 MHz. Verify signal on CRT at -30 dB line or +0.8 VDC on scope. Adjust R3941 as necessary.

16. Set RF Generator to -70 dBm at 10.7 MHz. Verify signal on CRT at -80 dB line or -0.2 VDC on scope. Adjust R3942 as necessary.

17. Set RF Generator to -90 dBm at 10.7 MHz. Verify signal at -100 dB line or -0.6 VDC on scope.

18. Repeat steps 12 through 17 and verify calibration within ± 1 dB.

19. Set dB/DIV Switch to 1 dB and the VERT POS Control fully cw.

20. Set RF Generator to -20 dBm at 10.7 MHz. Verify signal on CRT at -30 dB line. Adjust R3963 as necessary.

21. Set RF Generator to -30 dBm at 10.7 MHz. Adjust VERT POS Control so that signal is on -30 dB line on CRT.

22. Set RF Generator to -38 dBm at 10.7 MHz. Adjust R3969 so that signal is on -110 dB line on CRT.

23. Repeat Steps 19 through 22 and verify CRT calibration within ± 0.1 dB.

24. Disconnect all test equipment.

5-7-2 SPECTRUM ANALYZER LO MODULE TROUBLESHOOTING

SPECIAL ACCESSORY EQUIPMENT REQ'D:
1 Digital Voltmeter---Any
1 Oscilloscope---Dual Trace
1 RF Generator---Capable of 79.3 MHz at +5 dBm
1 Spectrum Analyzer---Capable of 79.3 MHz at +10 dBm
1 Frequency Counter---Capable of 100 Hz

FIGURE REFERENCES:
Spectrum Analyzer LO Module (Section 6)
Spectrum Analyzer LO Schematic (Section 7)
Spectrum Analyzer LO Theory (Section 2)

TEST SET-UP DIAGRAM: N/A

STEP PROCEDURE

1. Verify +12 VDC, -12 VDC and +5 VDC at pins 12, 18 and 14 of J4603.

2. Using Frequency Counter, verify 100 Hz reference input at pin 7 of J4603.

3. Verify ANALY DISPR Control inputs per Table 2-3 in Module Theory.

4. Verify outputs as follows:

ANALY DISPR Setting	Output (logic high)
2M thru FULL	J4603, pin 23
All but FULL	J4603, pin 7
1K, 2K	J4603, pin 19
10K, 20K	J4603, pin 20
100K thru FULL	J4603, pin 24
2M thru FULL	J4603, pin 15

5. Using Oscilloscope, connect probe to pin 1 of U3515. Verify a 10 Hz sweep ramp with equal positive and negative excursions. If necessary, adjust R3547.

6. Connect a second Oscilloscope probe to pin 1 of U3503. Sync on the ramp signal so that the 1 mS pulse is centered on the ramp negative retrace. If necessary, adjust R3529.

7. Connect RF Generator, set at +5 dBm at 79.3 MHz to J4602.

8. Measure DC voltage at pin 1 of U3508. Verify voltage is +5.6 VDC. If necessary, adjust L3501.

9. Using Spectrum Analyzer, measure output at J4604. Verify +3 to +10 dBm level at 79.3 MHz. Any side bands should be 75 dBc or lower.

NOTE

ANALY DISPR Control must be in "2 MHz" position or greater.

10. Using Spectrum Analyzer, measure output at J4605. Verify +4 to +10 dBm at 79.3 MHz. Any sidebands should be 75 dBc or lower.

11. Using Oscilloscope connected to pin 22 of J4603, verify that amplitude varies as ANALY DISPR Control is switched from "1K" through "1M". If necessary, adjust R3567.

12. Using Oscilloscope connected to pin 6 and then to pin 5 of J4603, observe that signal varies as ANALY DISPR Control is rotated. If necessary, adjust R3560.

13. Using Oscilloscope connected to pin 15 of J4603, observe that signal varies as ANALY DISPR Control is rotated from "2M" through "FULL". If necessary, adjust R3601.

14. Disconnect all test equipment.

5-7-3 SPECTRUM ANALYZER RF MODULE TROUBLESHOOTING

SPECIAL ACCESSORY EQUIPMENT REQ'D:
- 1 Digital Voltmeter---Any
- 1 Tracking Generator---Capable of 180 MHz at -20 dBm
- 1 Spectrum Analyzer---Capable of 95 MHz
- 1 RF Generator---Capable of 90 MHz at -30 dBm

FIGURE REFERENCES:
- Spectrum Analyzer RF Module (Section 6)
- Spectrum Analyzer RF Schematic (Section 7)
- Spectrum Analyzer RF Theory (Section 2)

TEST SET-UP DIAGRAM: N/A

STEP PROCEDURE

1. Verify +12 VDC at pin 9 of J5204.

2. Rotate ANALY DISPR Control and verify +12 VDC as follows:

ANALY DISPR Settings	+12V
1K, 2K	J5204, pin 2
10K, 20K	J5204, pin 3
.1M, .2M, .5M, 1M, 2M, 5M, 10M, FULL	J5204, pin 1

3. Set SW3701 to test position. Adjust R3796 for +3.5 VDC on switch output.

4. Disconnect coax cables from J5201, J5202, J5203 and J5205.

5. Connect Tracking Generator, centered at 90 MHz at -20 dBm, to J5202.

6. Connect Spectrum Analyzer, set at 1 MHz/div, to TP1. Tune L3701, L3703 and L3705 for maximum output.

7. Connect Spectrum Analyzer to TP3. Tune L3706, L3707 and L3708 for maximum output.

8. While varying tune voltage at R3796, observe Spectrum Analyzer for maximum gain and no more than ± 0.4 dB variation in amplitude from 95 MHz to 84 MHz. Tune L3701, L3703, L3705, L3706, L3707 and L3708 as needed. -27 dBm is a typical output level.

9. Readjust R3796 for 3.5 VDC tune voltage.

10. Connect Tracking Generator, centered at 10.7 MHz at -20 dBm, to TP5.

11. Connect Spectrum Analyzer to TP5. Center Spectrum Analyzer at 10.7 MHz. Tune for maximum output (typically -30 dB) and for a symmetrical frequency response by adjusting L3717, L3720, L3721, L3722, L3723 and L3724.

12. Set ANALY DISPR Control to "10K" or "20K" (for 3 KHz filter).

13. Connect Spectrum Analyzer to J5205. Set Spectrum Analyzer to 50 KHz/div. Tune for maximum output and flatness using C3714, C3715, C3716, C3717, C3735 and C3736.

14. Verify that output level is -5 dBm or greater with R3749 at maximum output.

15. With ANALY DISPR Control in "1K" and "2K" positions (for 300 Hz filter) and R3771 at maximum output, verify output level is -5 dBm or greater.

16. With ANALY DISPR Control in ".1M" and greater positions (for 650 KHz filter) and R3777 at maximum output, verify output level is -5 dBm or greater.

17. Disconnect Tracking Generator from J5202. Connect P5203 to J5203. Verify signal at J5203 of 79.3 MHz at +4 to +10 dBm.

18. Set ANALY DISPR Control to ".1M".

19. Connect RF Generator, set at -30 dBm at 90 MHz, to J5202.

20. Using Spectrum Analyzer connected at J5205, verify a -15 dBM typical output at 10.7 MHz. Adjust tune voltage at R3796 for maximum gain.

21. Verify an audio signal (or inject one) at pin 5 of J5204. Observe pin 6 of U3701 and verify that gain and offset levels are adjustable by varying R3791 and R3794.

22. Set SW3701 to RUN position before returning to service.

23. Disconnect all test equipment.

5-8 MICROPROCESSOR FUNCTIONAL BLOCK TROUBLESHOOTING

5-8-1 CPU/MEMORY PC BOARD TROUBLESHOOTING

SPECIAL ACCESSORY EQUIPMENT REQ'D:
- 1 Digital Voltmeter---Any
- 1 Extender Ribbon Cable---Available as part of Option 05 (Part No. 7001-5046-700)
- 1 Frequency Counter---Capable of 2 MHz

FIGURE REFERENCES:
- CPU/Memory PC Board (Section 6)
- CPU/Memory PC Board Schematic (Section 7)
- CPU/Memory PC Board Theory (Section 2)

TEST SET-UP DIAGRAM: N/A

STEP	PROCEDURE
1.	Set FM/AM-1500 PWR/OFF/BATT Switch to "OFF".
2.	Remove CPU/Memory PC Board from set by removing screws securing PC Board and shield assembly to set. Do not remove PC Board from shield. Install extender ribbon cable between P4101 on PC Board and J4101 on Mother Board.
3.	Measure the battery voltage at TP1. Verify voltage is 3.0 VDC (± 0.3 V).
4.	Measure the voltage at pin 24 of U4118. Verify voltage is no less than 0.4 VDC below the battery voltage.
5.	Measure the voltage across R4121 (between TP2 and TP1). Verify voltage does not exceed .001 VDC.
6.	Set PWR/OFF/BATT Switch to "ON". Again measure the voltage across R4121. Verify voltage does not exceed .0001 VDC.
7.	Measure voltage at pin 19 of U4119. Verify 0 volts.
8.	Set PWR/OFF/BATT Switch to "OFF". Verify 3 VDC at pin 19 of U4119.
9.	Set PWR/OFF/BATT Switch to "ON". Using Frequency Counter, verify a 2 MHz input at pin 32 of P4101. Verify 20 KHz at pin 3 of U4127.
10.	Disconnect all test equipment.

5-8-2 I/O INTERFACE PC BOARD TROUBLESHOOTING

SPECIAL ACCESSORY EQUIPMENT REQ'D:
- 1 Digital Voltmeter---Any
- 1 Extender Board and Extender Cable--- Available as part of Option 05 (Part No. 7001-5046-700)

FIGURE REFERENCES:
- I/O Interface PC Board (Section 6)
- I/O Interface PC Board Schematic (Section 7)
- I/O Interface PC Board Theory (Section 2)

TEST SET-UP DIAGRAM: N/A

STEP PROCEDURE

1. Install extender board and ribbon cable. Verify +5 VDC, +12 VDC and -12 VDC, respectively, at pins 1, 25 and 26 of P4301.

2. Test the bus (and thus, the talk-back circuit) by selecting the Self Test Menu on the CRT (50) and pressing "EXEC 4, ENTER". Verify no error message is displayed on LCD (21).

3. The Front Panel controls listed in Table 5-3 are controlled through the bus. Test each control by referring to the I/O PC Board schematic and checking that inputs and outputs are correct per the schematic.

   (37) FREQ ERROR Control
   (38) ANALY DISPR Control
   (51) DISPLAY Control
   (7) MODULATION Control
   (39) DEV/VERT Control
   (55) ATTENUATOR Switch
   (19) GEN/REC Switch
   (18) DUPLEX/SIMPLEX Switch
   (48) dB/DIV Switch
   (4) AVG PEAK/PEAK Switch

   Table 5-3 Microprocessor Controlled Controls

4. Verify that LCD/Keyboard control lines operate by entering data in each of the fields on the LCD (21). Troubleshoot control lines per schematic.

5. Verify that High Loop control lines operate by keying in applicable frequency on LCD (21). For example, when 040.XXXX FREQ MHz is keyed in on LCD, pin 1 of P4305 is high and the other High Loop control lines are low.

6. Verify that Low Loop control lines operate by keying in applicable frequency on LCD (21). For example, when XXX.4000 FREQ MHz is keyed in on LCD, pin 19 of P4306 is high and the other Low Loop control lines are low.

7. Verify that Duplex Offset control lines operate by keying in applicable frequency on LCD (21). For example, when +10.00 OFFSET MHz is keyed in on LCD, pins 19, 17, 16 and 15 of P4307 are high and the other Duplex Offset lines are low.

NOTE

Remember that Duplex Offset is centered at 180 MHz, that a positive offset is subtracted from 180 MHz and that a negative offset is added to 180 MHz.

8. Verify that low-pass filter lines on pins 15 and 17 of P4304 operate as follows:

FREQ MHz	pin 17 (LPF-A)	pin 15 (LPF-B)
000.XXXX - 050.XXXX	Low	Low
051.XXXX - 130.XXXX	High	Low
131.XXXX - 256.XXXX	Low	High
257.XXXX - 999.XXXX	High	High

9. Verify that 455 MHz Sw. output (pin 8 of P4304) is low at 454.XXXX FREQ MHz, and high at 455.XXXX FREQ MHz.

10. Disconnect all test equipment.

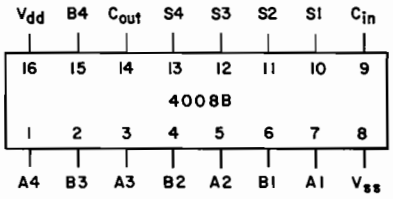
5-9 IC TRUTH TABLES

The following truth tables are provided to assist the technician in troubleshooting the FM/AM-1500. Many of these ICs are used repeatedly, while others are used only once. Not all ICs used in the FM/AM-1500 are illustrated, but careful study of the schematic of any assembly will show the function of non-listed ICs.

Table 5-5 IC Truth Table Index

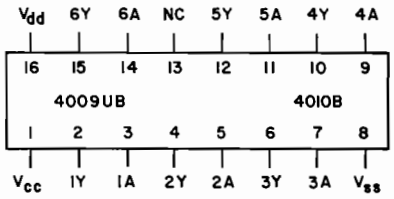
4008B

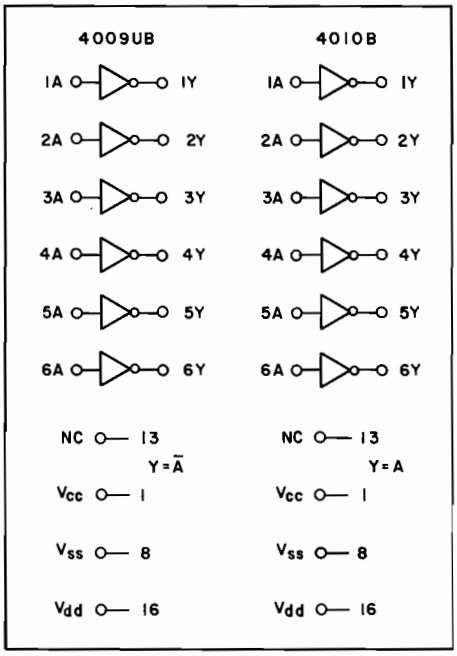
TRUTH TABLE
(ONE STAGE)



C_{IN}	B	A	C_{OUT}	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

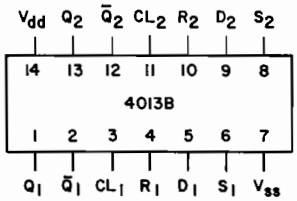
LOGIC DIAGRAMS





4013B

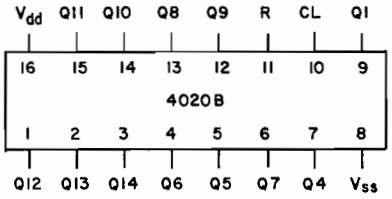
TRUTH TABLE



CL	D	R	S	Q	$\overline{Q}$
↑	0	0	0	0	1
↑	1	0	0	1	0
↓	X	0	0	Q	$\overline{Q}$ NO CHANGE
X	X	1	0	0	1
X	X	0	1	1	0
X	X	1	1	1	1

X = DON'T CARE

4020B

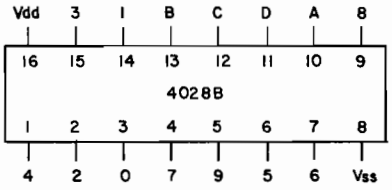


TRUTH TABLE

CLOCK	RESET	OUTPUT STATE
↑	0	NO CHANGE
↓	0	ADVANCE TO NEXT STATE
X	1	ALL OUTPUTS ARE LOW

X = DON'T CARE

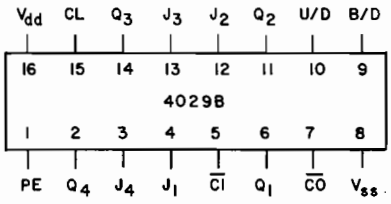
4028B



TRUTH TABLE

D	C	B	A	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	1
0	0	0	1	0	0	0	0	0	0	0	0	1	0
0	0	1	0	0	0	0	0	0	0	0	1	0	0
0	0	1	1	0	0	0	0	0	0	1	0	0	0
0	1	0	0	0	0	0	0	0	1	0	0	0	0
0	1	0	1	0	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	0	1	0	0	0	0	0	0
0	1	1	1	0	0	1	0	0	0	0	0	0	0
1	0	0	0	0	1	0	0	0	0	0	0	0	0
1	0	0	1	1	0	0	0	0	0	0	0	0	0
1	0	1	0	0	0	0	0	0	0	0	0	0	0
1	0	1	1	0	0	0	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0	0	0	0	0	0	0
1	1	0	1	0	0	0	0	0	0	0	0	0	0
1	1	1	0	0	0	0	0	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0	0	0	0

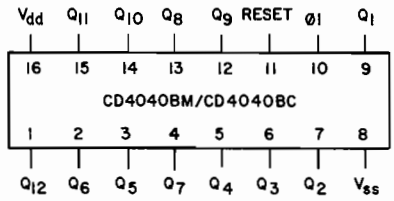
4029B



TRUTH TABLE

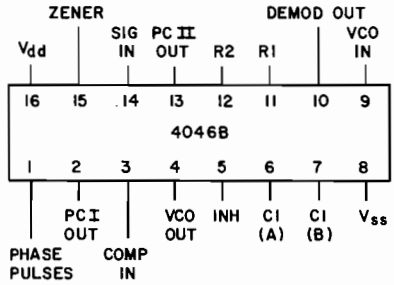
$\overline{CI}$	U/D	PE	B/D	ACTION
1	X	0	X	NO COUNT
0	1	0	0	COUNT UP (DECADE)
0	1	0	1	COUNT UP (BINARY)
0	0	0	0	COUNT DOWN (DECADE)
0	0	0	1	COUNT DOWN (BINARY)
X	X	1	X	PRESET

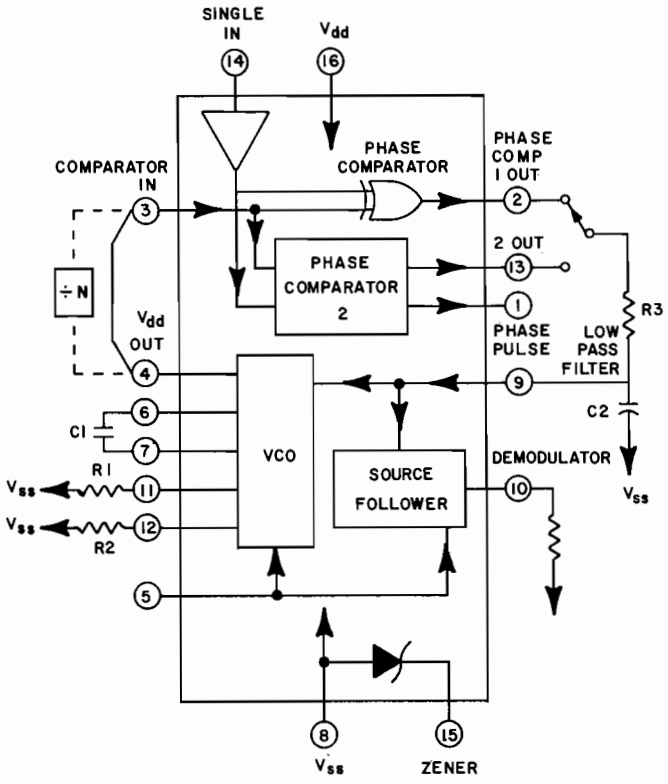
X = DON'T CARE

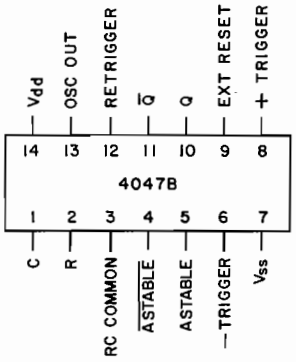


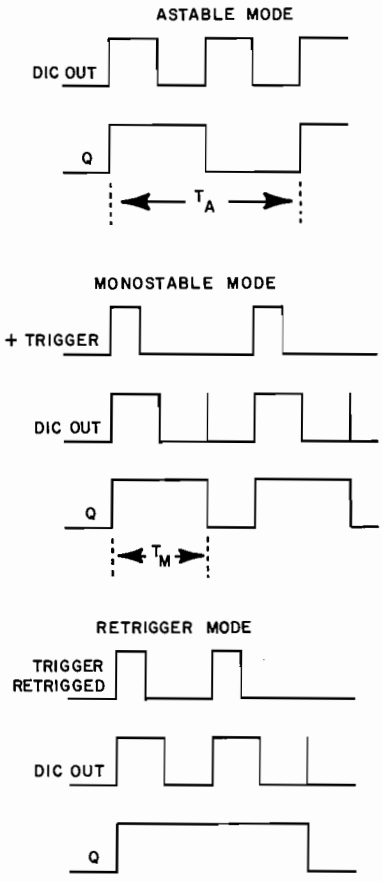
CD4040BM/CD4040BC

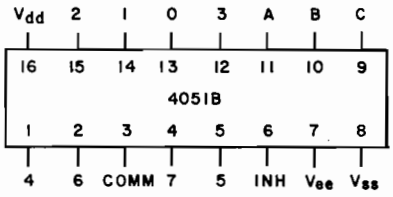
THE CD4040BM/CD4040BC IS A 12-STAGE RIPPLE CARRY BINARY COUNTER. THE COUNTER IS ADVANCED ONE COUNT ON THE NEGATIVE TRANSITION OF EACH CLOCK PULSE. THE COUNTER IS RESET TO THE ZERO STATE BY A LOGICAL "1" AT THE RESET INPUT INDEPENDENT OF CLOCK.

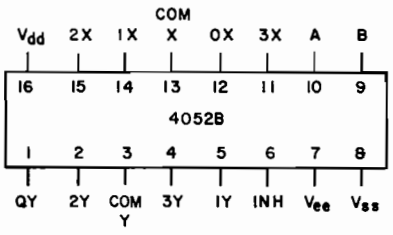


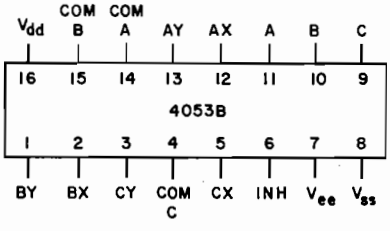








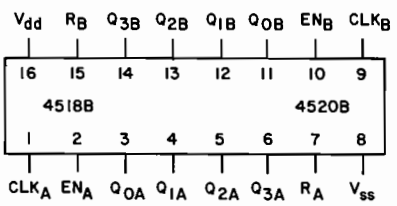




TRUTH TABLE

INPUT STATES				"ON" CHANNELS		
INHIBIT	C	B	A	4051	4052	4053
0	0	0	0	0	0X,0Y	CX,BX,AX
0	0	0	1	1	1X,1Y	CX,BX,AY
0	0	1	0	2	2X,2Y	CX,BY,AX
0	0	1	1	3	3X,3Y	CX,BY,AY
0	1	0	0	4		CY,BX,AX
0	1	0	1	5		CY,BX,AY
0	1	1	0	6		CY,BY,AX
0	1	1	1	7		CY,BY,AY
1	*	*	*	NONE	NONE	NONE

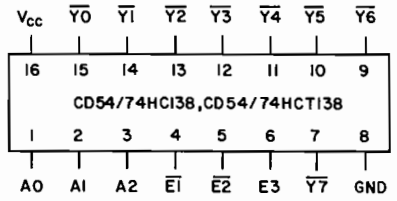
* = DON'T CARE



TRUTH TABLE

4518B 4520B

CLOCK	ENABLE	RESET	ACTION
↑	1	0	INCREMENT COUNTER
0	↓	0	INCREMENT COUNTER
↓	X	0	NO CHANGE
X	↑	0	NO CHANGE
↑	0	0	NO CHANGE
1	↓	0	NO CHANGE
X	X	1	Q0 THRU Q3 = 0



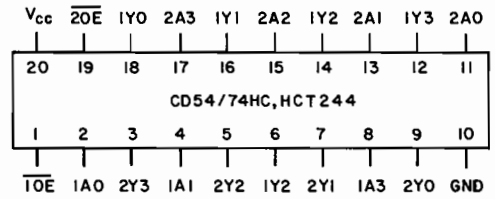
TRUTH TABLE

CD54/74HC138,CD54/74HCT138

INPUTS					OUTPUTS							
ENABLE		ADDRESS										
E_3	$*\overline{E0}$	A_2	A_1	A_0	$\overline{Y0}$	$\overline{Y1}$	$\overline{Y2}$	$\overline{Y3}$	$\overline{Y4}$	$\overline{Y5}$	$\overline{Y6}$	$\overline{Y7}$
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

H = HIGH LEVEL, L = LOW LEVEL, X = DON'T CARE

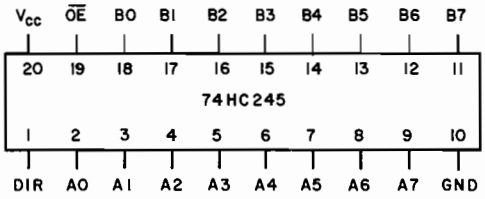
$*\overline{E}_0 = \overline{E}_1 + \overline{E}_2$



TRUTH TABLES

CD54/74HC,HCT244 TYPES

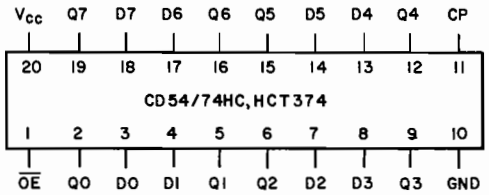
INPUTS		OUTPUT
$\overline{1OE,2OE}$	A	Y
L	L	L
L	H	H
H	X	Z



TRUTH TABLE

CONTROL INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B DATA TO A BUS
L	H	A DATA TO B BUS
H	X	ISOLATION

H = HIGH LEVEL, L = LOW LEVE
X = IRRELEVANT



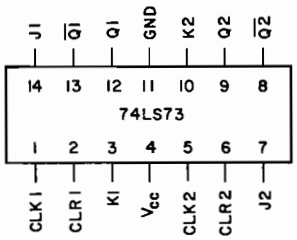
TRUTH TABLES

CD54/74HC, HCT374 TYPES
TERMINAL ASSIGNMENT

INPUTS			OUTPUTS
$\overline{OE}$	CP	DN	QN
L	↑	H	H
L	↑	L	L
L	L	X	Q0
H	X	X	Z

HC/HCT374,574

L = LOW LOGIC LEVEL
H = HIGH LOGIC LEVEL
↑ = LOW TO HIGH LOGIC LEVEL TRANSITION
Q = PREEXISTING OUTPUT LEVEL
HI-Z = HIGH IMPEDANCE OUTPUT STATE

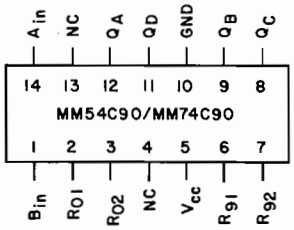


TRUTH TABLE

74LS73A

INPUTS				OUTPUTS	
CLR	CLK	J	K	Q	$\overline{Q}$
L	X	X	X	L	H
H	↓	L	L	Q0	$\overline{Q0}$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	Q0	$\overline{Q0}$

MM54C90/MM74C90 4-BIT DECADE COUNTER



BCD COUNT SEQUENCE

COUNT	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

OUTPUT Q_A IS CONNECTED TO INPUT B FOR BCD COUNT.

H = HIGH LEVEL

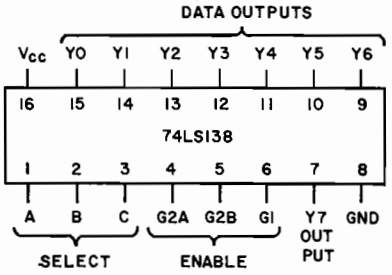
L = LOW LEVEL

X = IRRELEVANT

RESET/COUNT FUNCTION TABLE

RESET INPUTS				OUTPUT			
R_{01}	R_{02}	R_{91}	R_{92}	Q_D	Q_C	Q_B	Q_A
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L	COUNT			
L	X	L	X	COUNT			
L	X	X	L	COUNT			
X	L	L	X	COUNT			

'LS138, 'S138



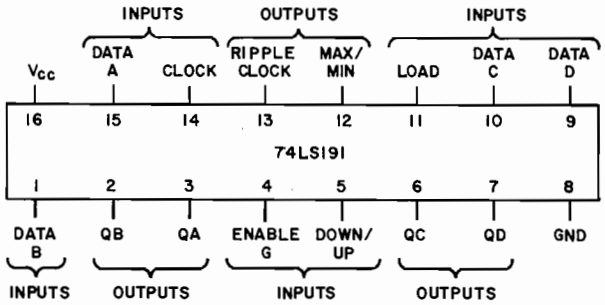
FUNCTION TABLE

74LS138

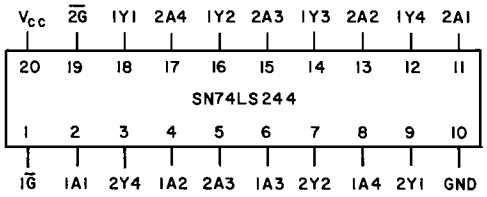
INPUTS					OUTPUTS							
ENABLE		SELECT										
G1	G2*	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

*G2 = G2A + G2B

H = HIGH LEVEL, L = LOW LEVEL, X = IRRELEVANT



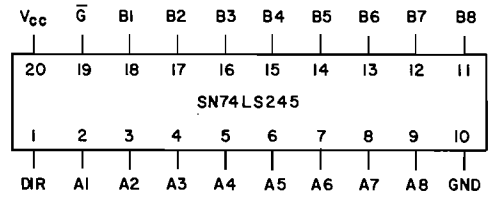
ASYNCHRONOUS INPUTS: LOW INPUT TO LOAD SETS Q_A=A, Q_B=B, Q_C=C, AND Q_D=D



TRUTH TABLE 74LS244

INPUTS				OUTPUTS	
$\overline{1G}$	1A	$\overline{2G}$	2A	1Y	2Y
L	L	L	L	L	L
L	H	L	H	H	H
H	X	H	X	(Z)	(Z)

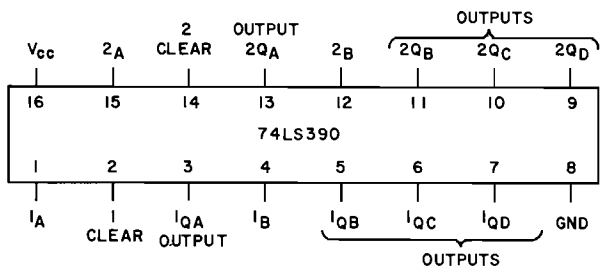
H = HIGH VOLTAGE LEVEL
L = LOW VOLTAGE LEVEL
X = DON'T CARE
(Z) = HIGH IMPEDANCE (OFF) STATE



FUNCTION TABLE SN74LS245

ENABLE $\overline{G}$	DIRECTION CONTROL DIR	OPERATION
L	L	B DATA TO A BUS
L	H	A DATA TO B BUS
H	X	ISOLATION

H = HIGH LEVEL, L = LOW LEVEL, X = IRRELEVANT



74LS390

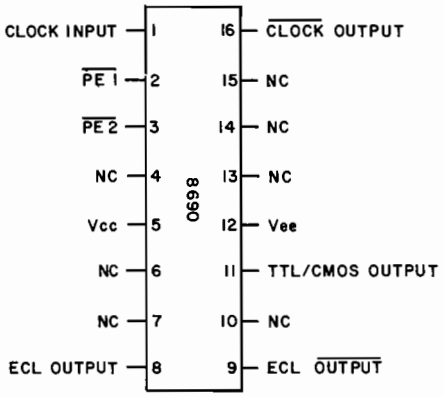
'390, 'LS390
BCD COUNT SEQUENCE
(EACH COUNTER)
(SEE NOTE A)

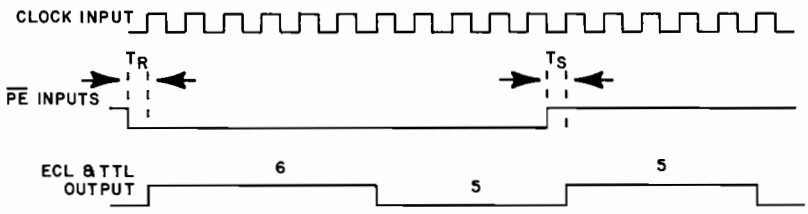
COUNT	OUTPUT Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

BI-QUINARY
(EACH COUNTER)
(SEE NOTE B)

COUNT	OUTPUT Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

NOTES: A. OUTPUT Q_A IS CONNECTED TO INPUT B FOR BCD COUNT.
B. OUTPUT Q_D IS CONNECTED TO INPUT A FOR BI-QUINARY COUNT.
C. H = HIGH LEVEL, L = LOW LEVEL.

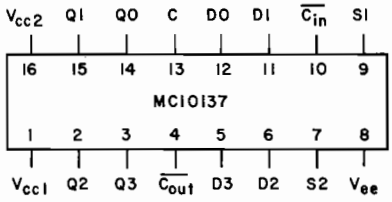




TRUTH TABLE FOR CONTROL INPUTS

PE1	PE2	DIVISION RATIO
L	L	11
H	L	10
L	H	10
H	H	10

MC10137



FUNCTION SELECTION TABLE

S1	S2	OPERATING MODE
L	L	PRESET (PROGRAM)
L	H	INCREMENT (COUNT UP)
H	L	DECREMENT (COUNT DOWN)
H	H	HOLD (STOP COUNT)

P_D = 625 MW TYP/PKG (NO LOAD)
F_{COUNT} = 150 MHZ TYP

SEQUENTIAL TRUTH TABLE *

INPUTS								OUTPUTS				
S1	S2	D0	D1	D2	D3	CARRY IN	CLOCK * *	Q0	Q1	Q2	Q3	CARRY OUT
L	L	H	H	H	L	X	H	H	H	H	L	H
L	H	X	X	X	X	L	H	L	L	L	H	H
L	H	X	X	X	X	L	H	H	L	L	H	L
L	H	X	X	X	X	L	H	L	L	L	L	H
L	H	X	X	X	X	L	H	H	L	L	L	H
L	H	X	X	X	X	H	H	H	L	L	L	H
L	H	X	X	X	X	H	H	H	L	L	L	H
H	H	X	X	X	X	X	H	H	L	L	L	H
L	L	H	H	L	L	X	H	H	H	L	L	H
H	L	X	X	X	X	L	H	L	H	L	L	H
H	L	X	X	X	X	L	H	H	L	L	L	H
H	L	X	X	X	X	L	H	L	L	L	L	L

X = DON'T CARE

* TRUTH TABLE SHOWS LOGIC STATES ASSUMING INPUTS VARY IN SEQUENCE SHOWN FROM TOP TO BOTTOM.

* * A CLOCK H IS DEFINED AS A CLOCK INPUT TRANSITION FROM A LOW TO A HIGH LOGIC LEVEL.

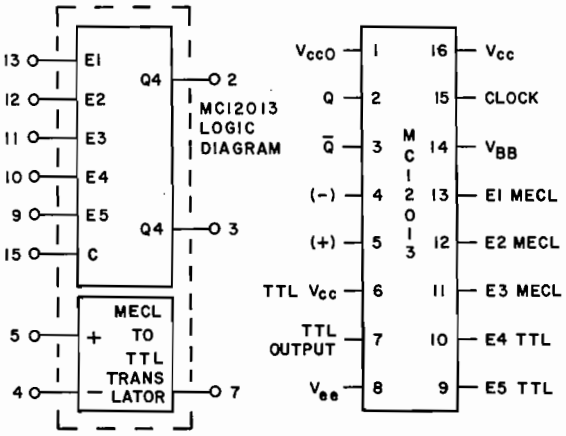
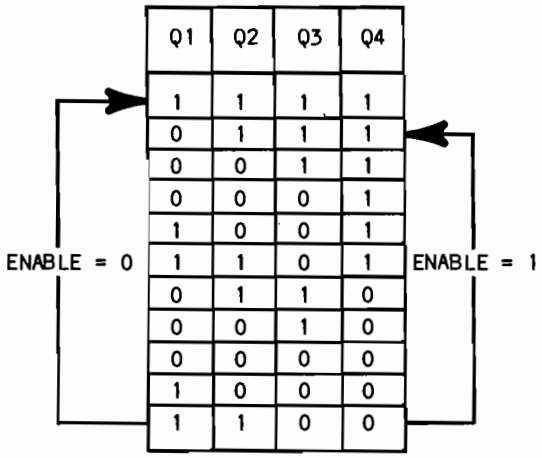


FIGURE 8 - DIVIDE BY 10/11 (MC12013/MC12513)



Q1	Q2	Q3	Q4
1	1	1	1
0	1	1	1
0	0	1	1
0	0	0	1
1	0	0	1
1	1	0	1
0	1	1	0
0	0	1	0
0	0	0	0
1	0	0	0
1	1	0	0

SECTION 6 - MECHANICAL ASSEMBLIES/PC BOARDS

6-1 GENERAL

This section contains mechanical assembly and PC Board drawings for all the assemblies contained within the FM/AM-1500. These drawings are provided for purposes of locating and identifying discrete components, connectors, test points and adjustments which are referenced in other sections of this manual. The drawings are sequenced in the order given in the index in paragraph 6-1-1.

NOTE

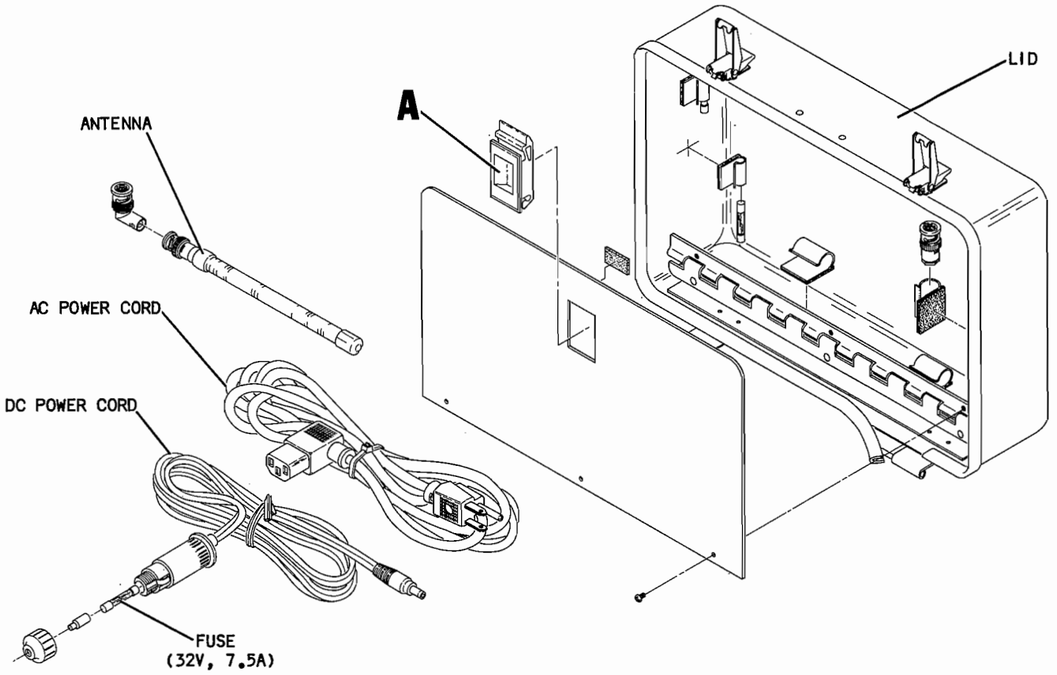
Drawings in this section take precedence over any existing labels installed in the FM/AM-1500.

Each figure in this section is accompanied by notes, which give reference designator series numbers, part numbers, applicable schematic numbers, wire running lists and any special assembly information.

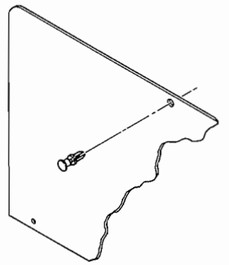
If a PC Board has components located on both sides, both a top and a bottom view of the PC Board will be provided. If, however, a PC Board has components only on one side, only the component side will be shown.

The drawings in this section are not intended for use in ordering spare or replacement parts. For parts ordering information, see the FM/AM-1500 Illustrated Parts Catalog.

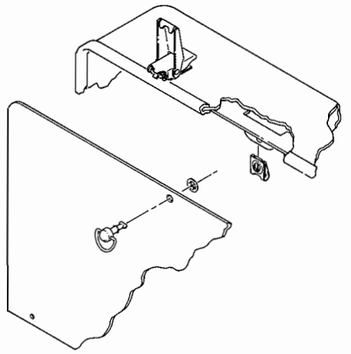
6-2 INDEX OF MECHANICAL ASSEMBLIES/PC BOARDS



SER. NO. 2052 AND ON

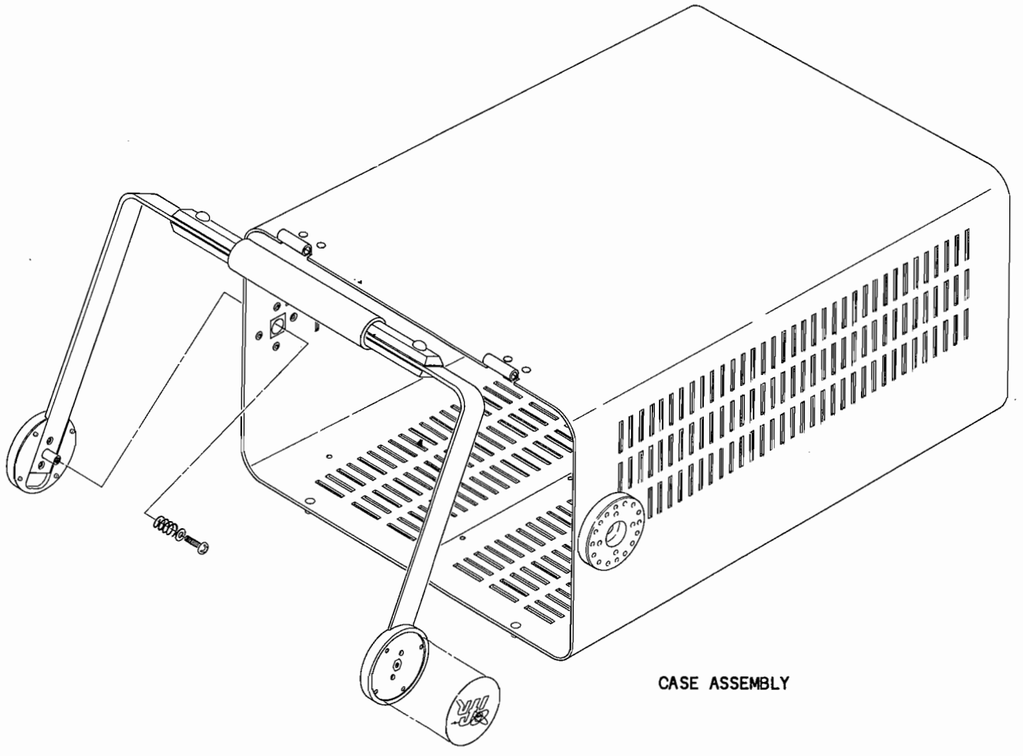


THRU SER. NO. 1967

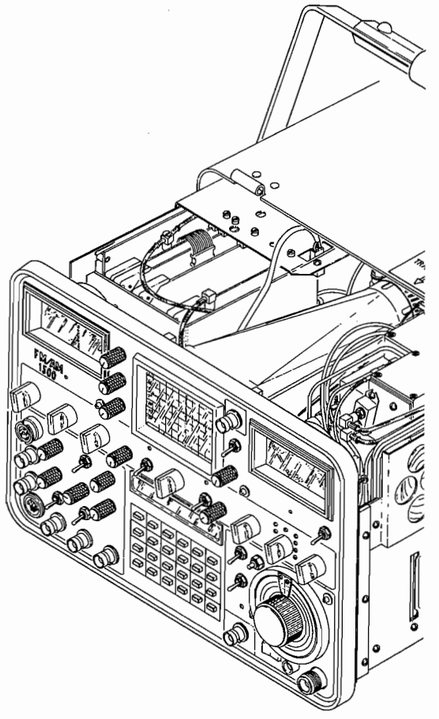


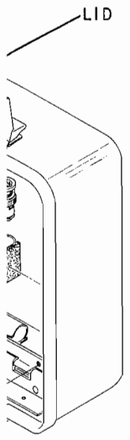
SER. NO. 1968 THRU 2051

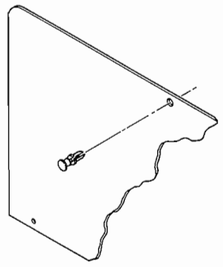
DETAIL **A**



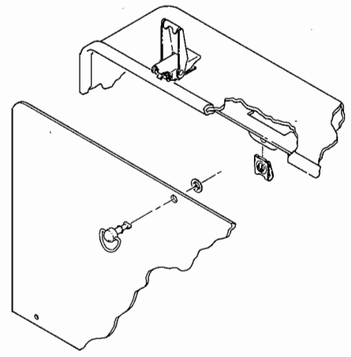
CASE ASSEMBLY







THRU SER. NO. 1967

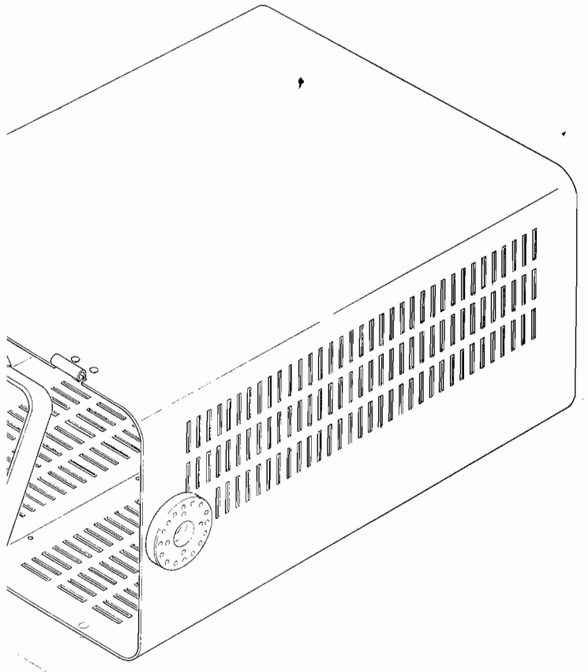


SER. NO. 1968 THRU 2051

DETAIL **A**

NOTES:

1. THE REF DES SERIES FOR THE COMPOSITE MECH ASSY IS 6400.
2. DATA PART NO. 7003-5040-000.



CASE ASSEMBLY

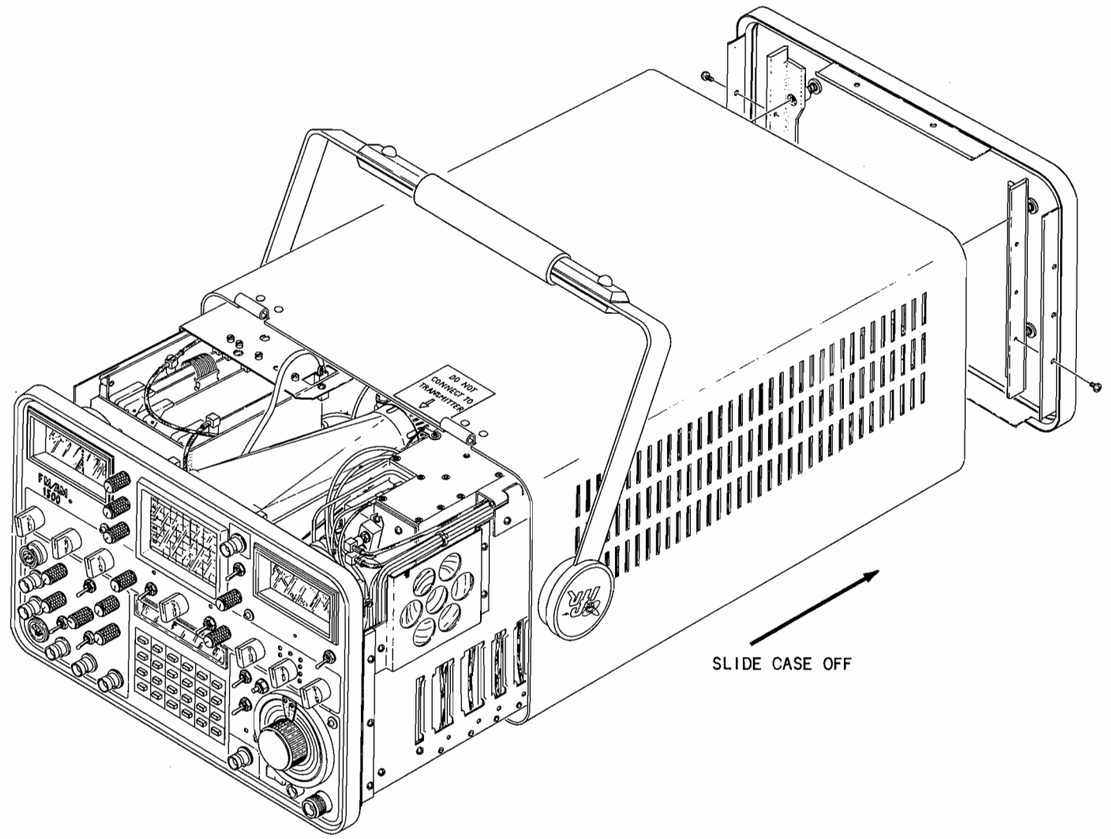
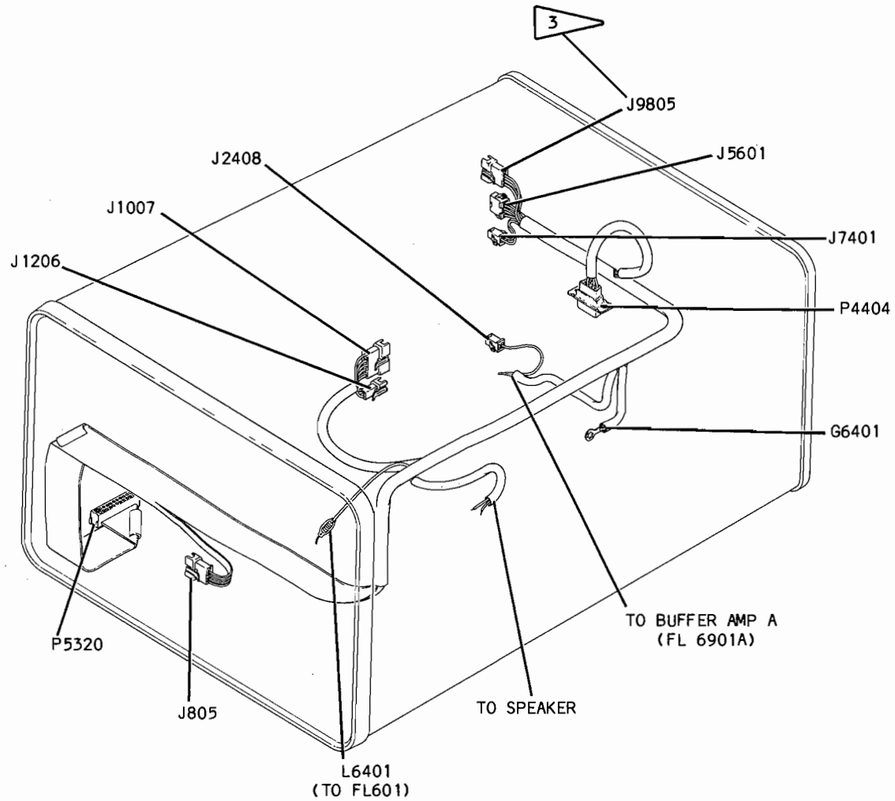
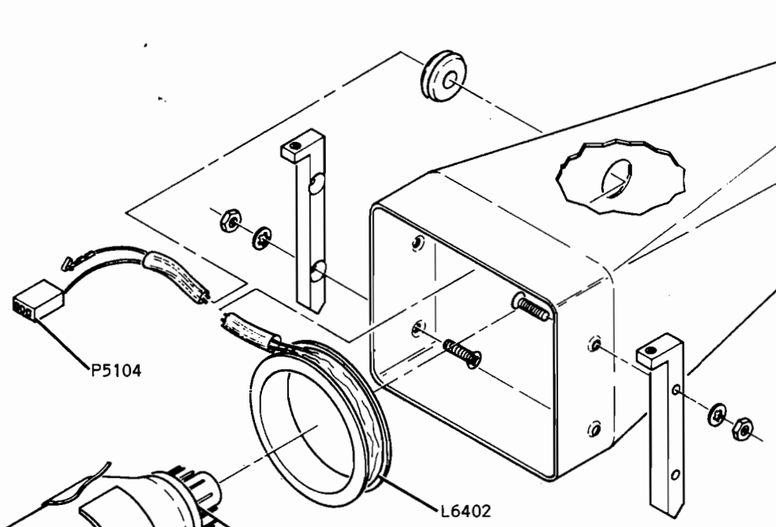
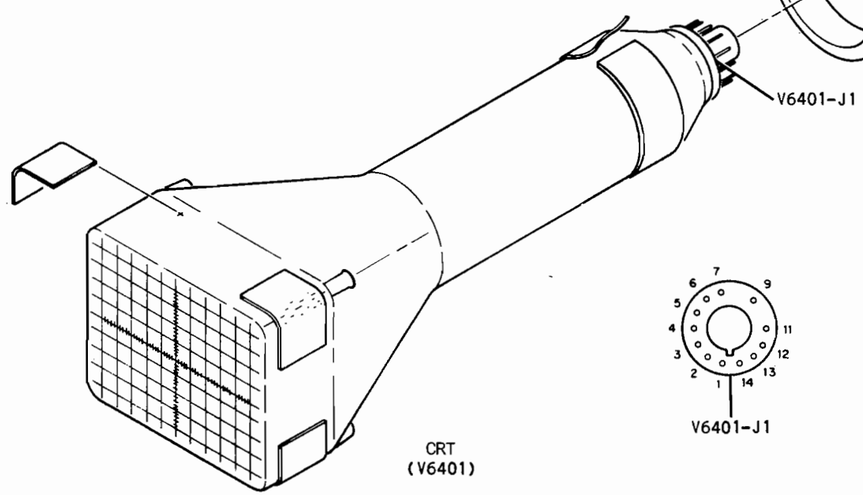


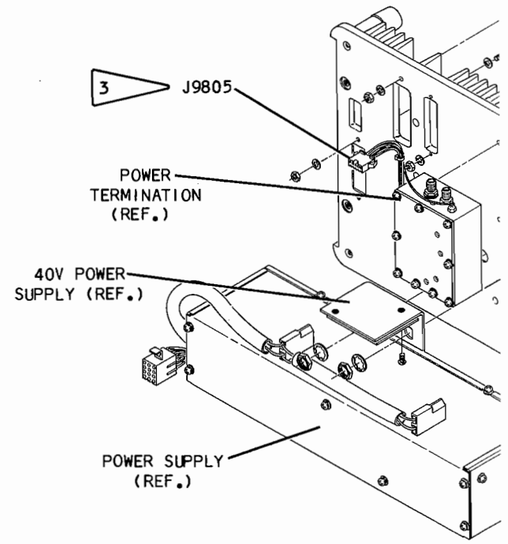
Figure 6-1 Composite Assembly (Sheet 1 of 2)



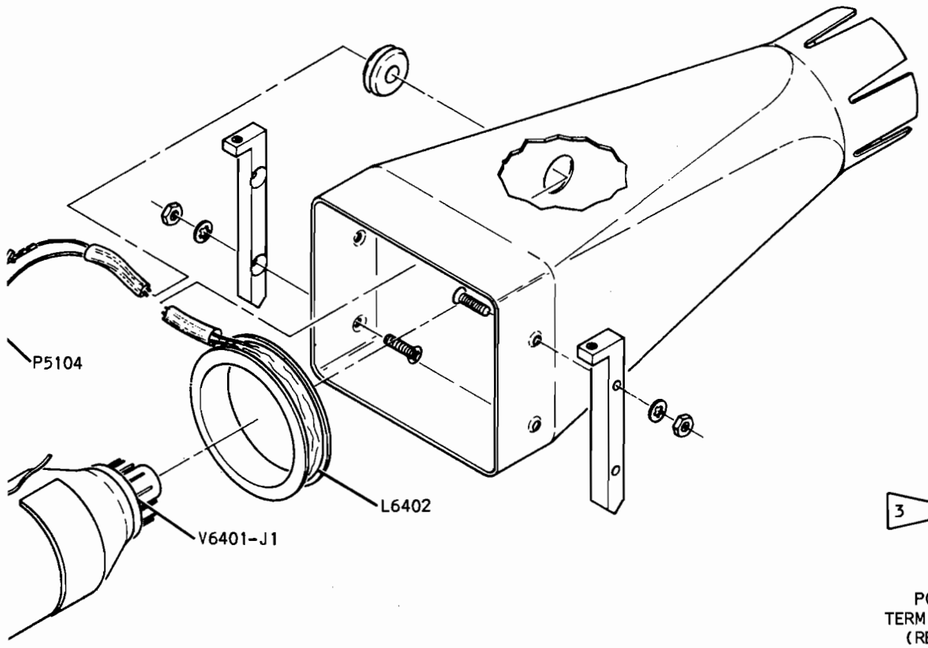
COMPOSITE WIRE HARNESS

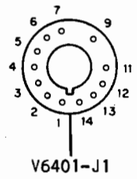


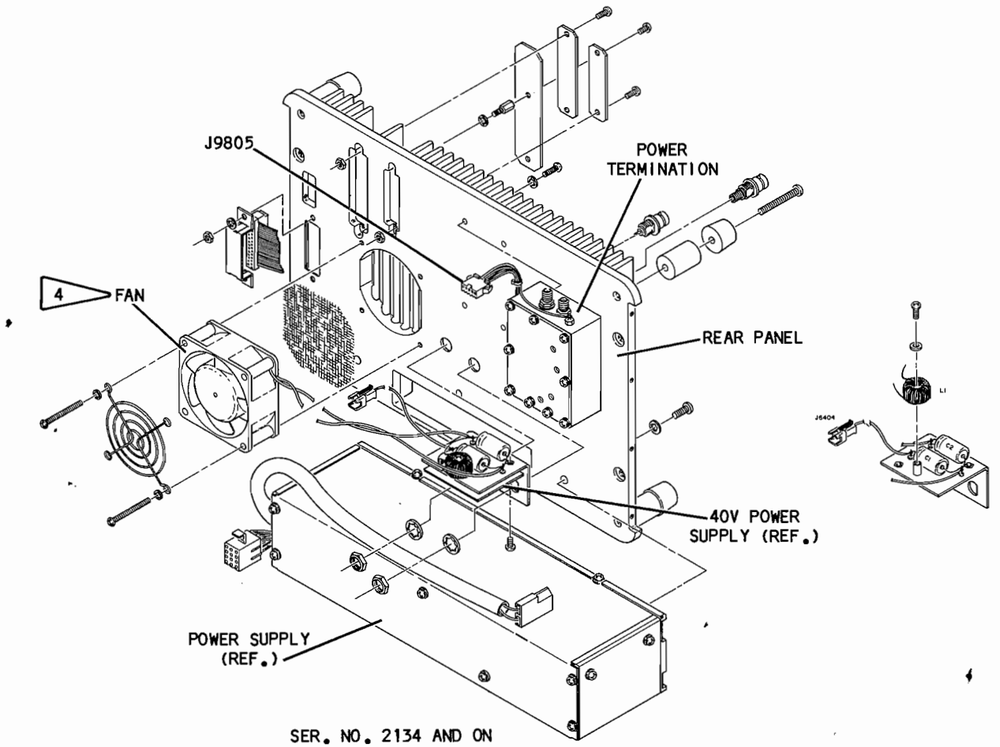




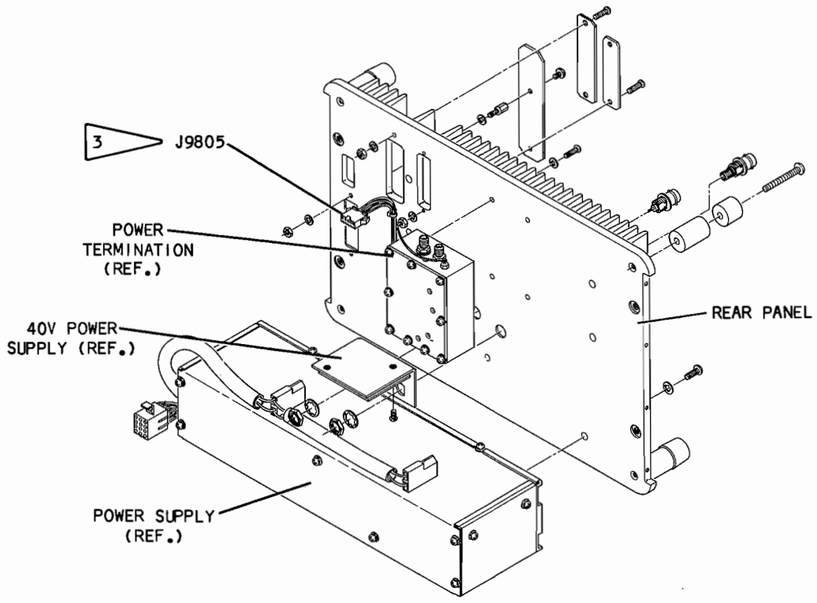
THRU SER. NO. 2133







SER. NO. 2134 AND ON



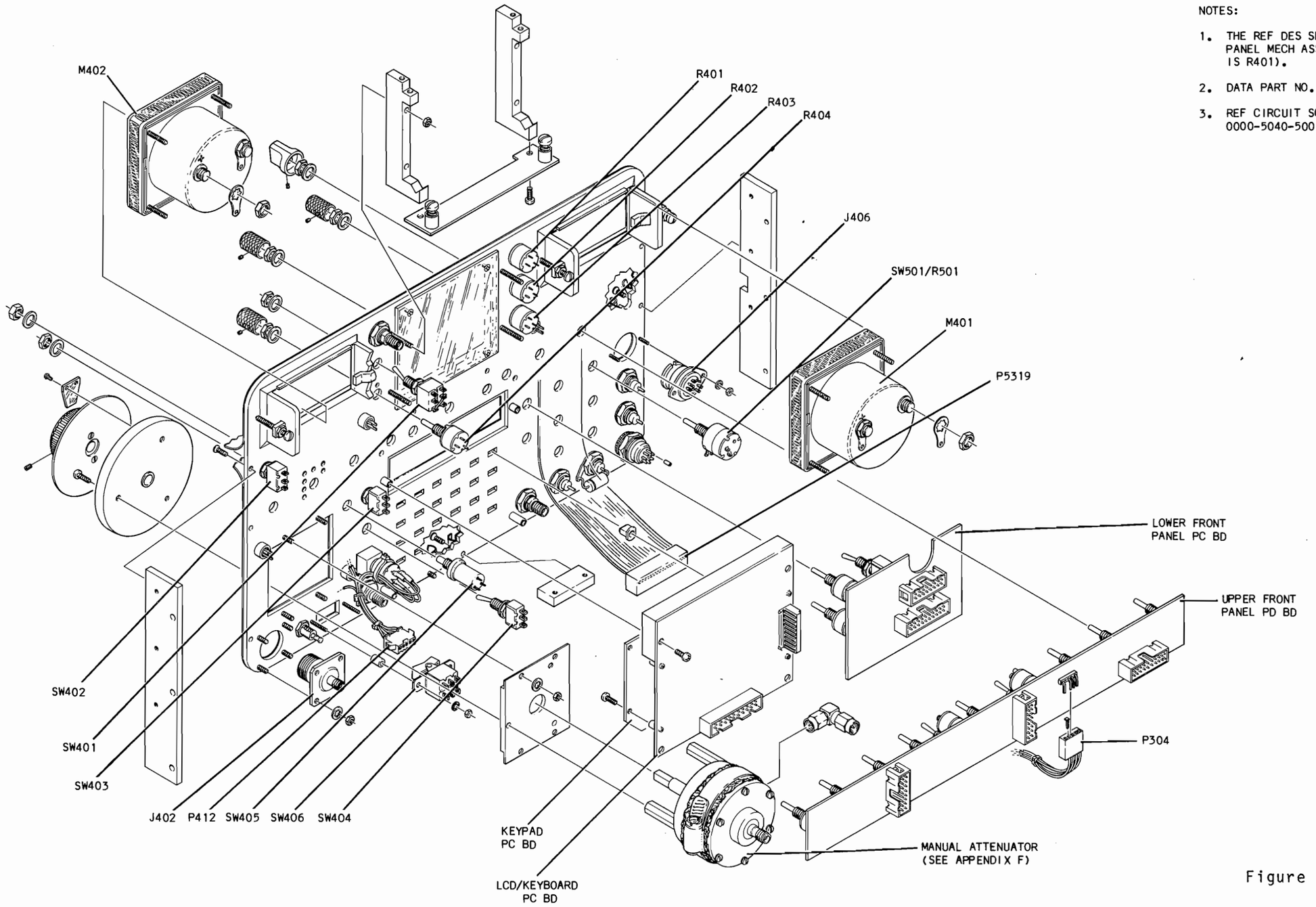
THRU SER. NO. 2133

NOTES (CONT.):

3. THRU SER. NO. 1993. REF. DES. WAS J6205.

4. EFFECTIVE SER. NO. 2134 AND ON, FAN ATTACHED.

Figure 6-1 Composite Assembly (Sheet 2 of 2)



NOTES:

1. THE REF DES SERIES FOR THE FRONT PANEL MECH ASSY IS 400 (I.E. R1 IS R401).
2. DATA PART NO. 7005-5040-500.
3. REF CIRCUIT SCHEMATIC 0000-5040-500.

Figure 6-2 Front Panel (Sheet 1 of 2)

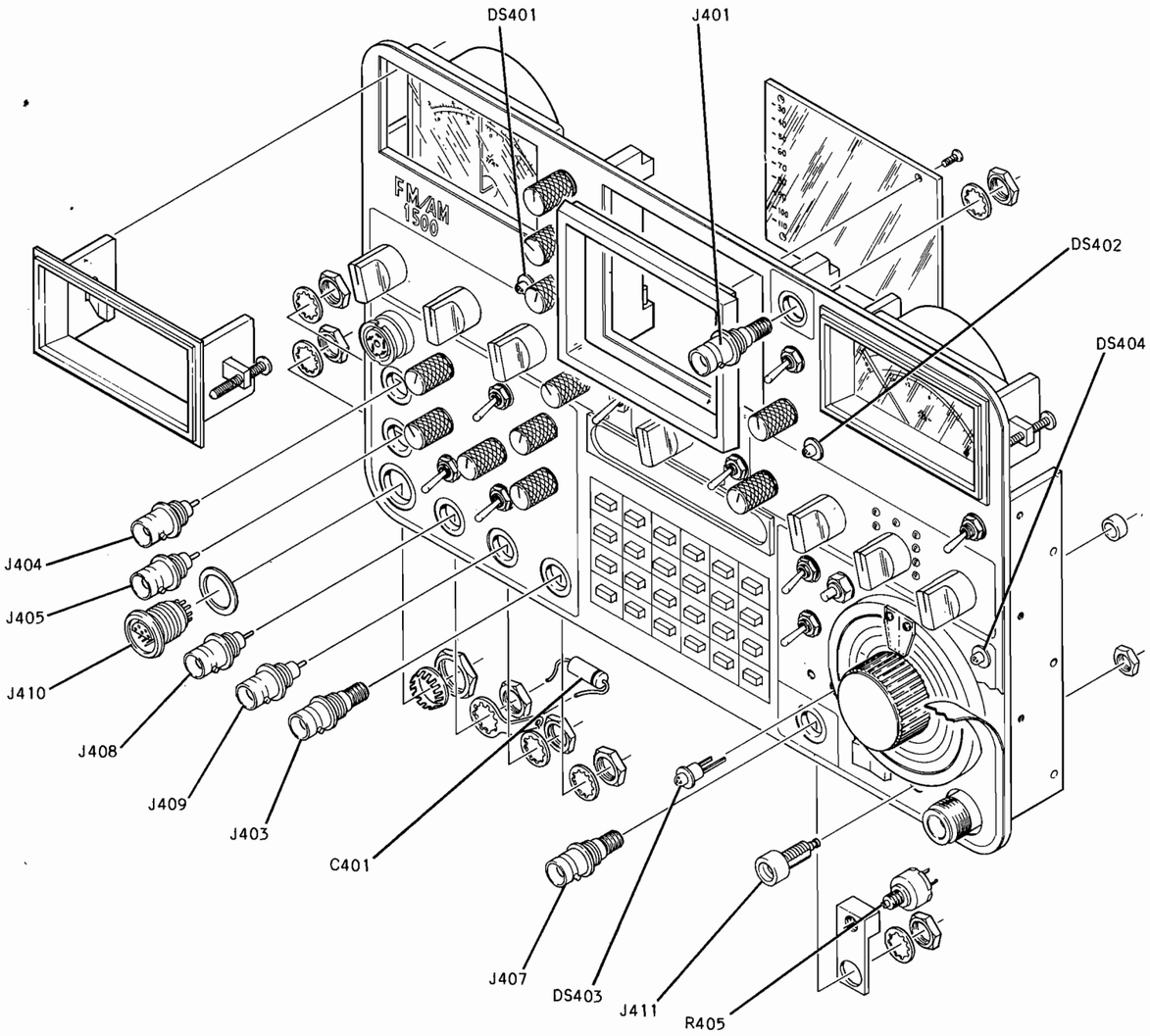
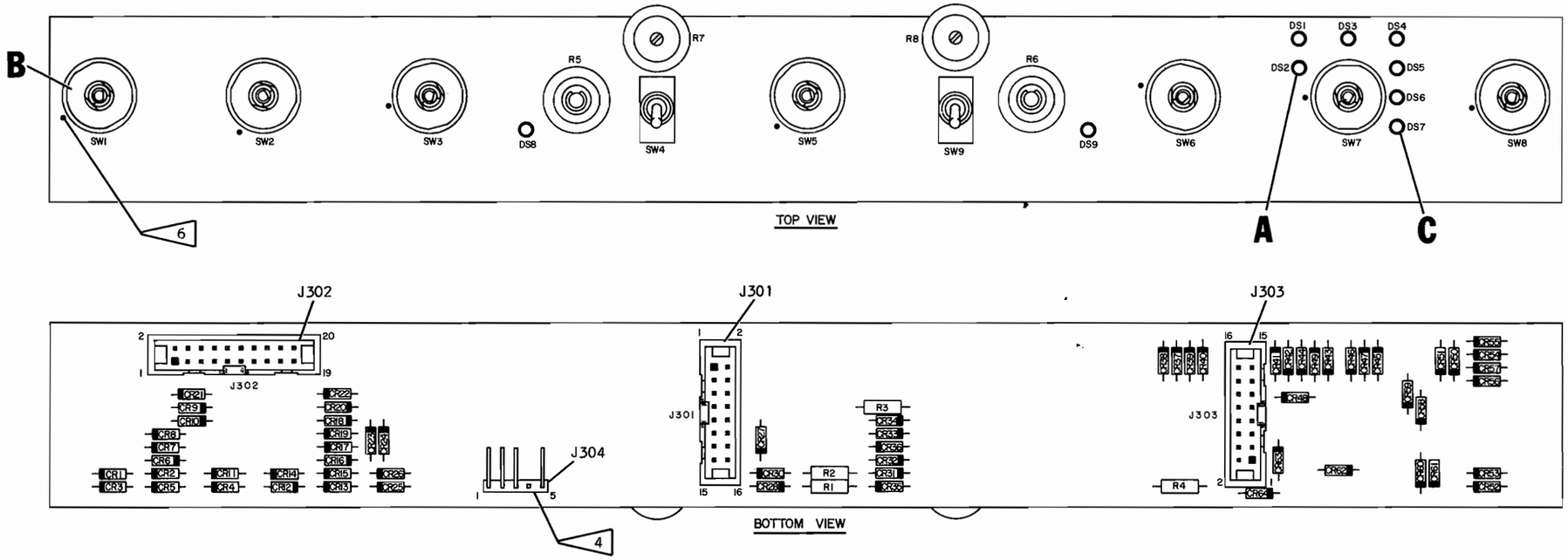
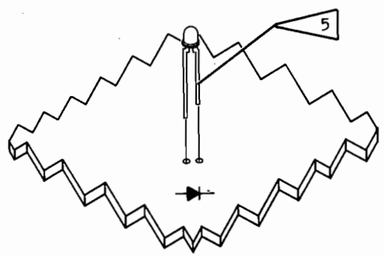


Figure 6-2 Front Panel (Sheet 2 of 2)



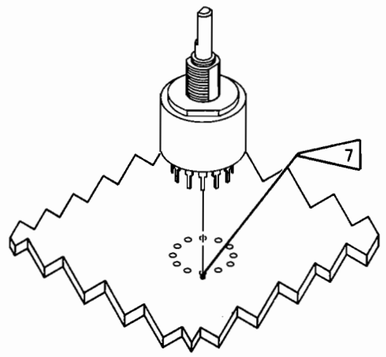
NOTES:

1. THE REF DES SERIES FOR UPPER FRONT PANEL PC BOARD ASSY IS 300 (I.E., R1 IS R301).
2. DATA PART NO. 7010-5030-300.
3. REF CIRCUIT SCHEMATIC 0000-5010-300.
4. PIN #4 TO BE REMOVED FROM TOP AND BOTTOM SIDE OF CONNECTOR J304, FOR KEYING, BEFORE SOLDERING TO PC BOARD.
5. SHORT LEAD OF LED LIGHT (DS1-DS9) IS CATHODE.
6. LOCATION OF PIN #1 IS REPRESENTED BY A DOT ON SW1-SW3 AND SW5-SW8.
7. PATHWORK WILL SHOW LOCATION OF PIN #1 ON PC BOARD.

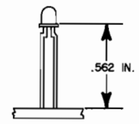


TYPICAL FOR DS1-DS9

DETAIL **A**



DETAIL **B**



TYPICAL FOR DS1-DS9

DETAIL **C**

FUNCTION	REF DESIG	GRAYHILL SW		STD GRIGSBY SW	
		1ST STOP	2ND STOP	1ST STOP	2ND STOP
FREQ. ERROR	SW301	12-1	9-10	2-3	11-12
ANALY. DISPR	SW302	12-1	NONE	2-3	---
DEV/VERT	SW303	12-1	8-9	2-3	10-11
DISPLAY	SW305	12-1	9-10	2-3	11-12
HORIZ	SW306	12-1	5-6	2-3	7-8
MODULATION	SW307	12-1	8-9	2-3	10-11
DEV/PWR	SW308	12-1	8-9	2-3	10-11

Figure 6-3 Upper Front Panel PC Board

NOTES:

1. THE REF DES SERIES FOR LOWER FRONT PANEL PC BOARD ASSY IS 500 (I.E., R1 IS R501).
2. DATA PART NO. 7010-5030-500.
3. REF CIRCUIT SCHEMATIC 0000-5010-500.

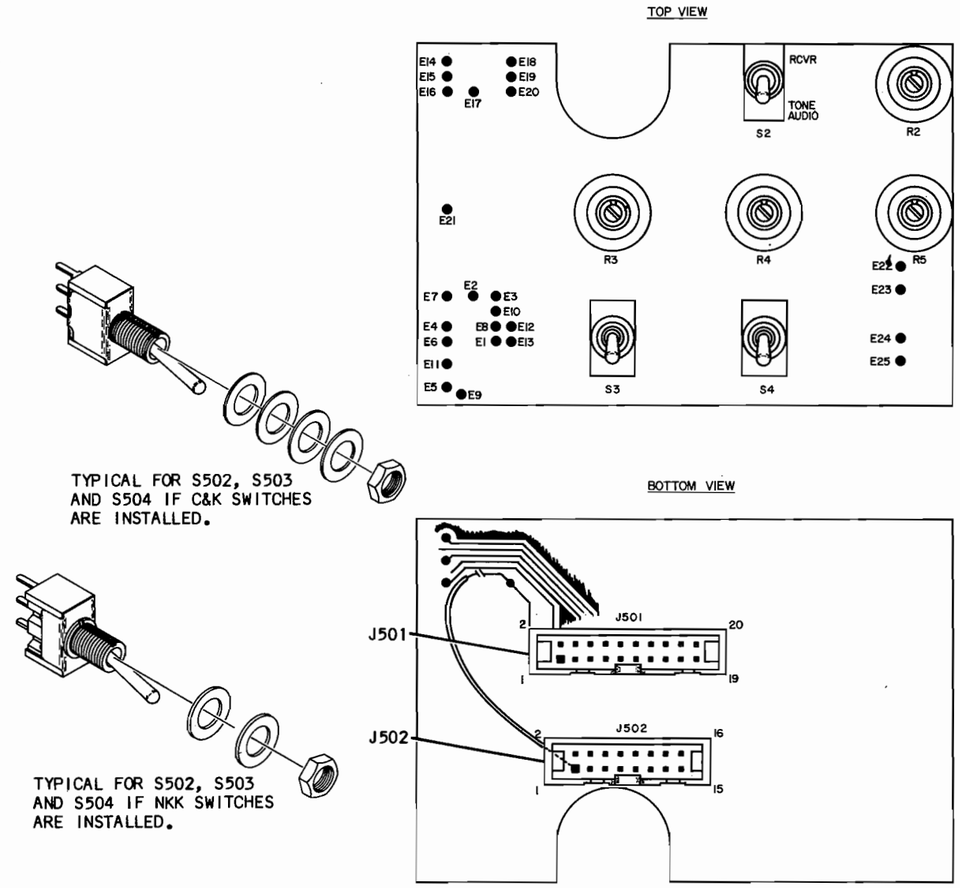


Figure 6-4 Lower Front Panel PC Board

NOTES:

1. THE REF DES SERIES FOR KEYPAD PC BOARD ASSY IS 200 (I.E. R1 IS R201).

2. DATA PART NO. IS 7010-5030-200.

3. REF CIRCUIT SCHEMATIC 0000-5010-200.

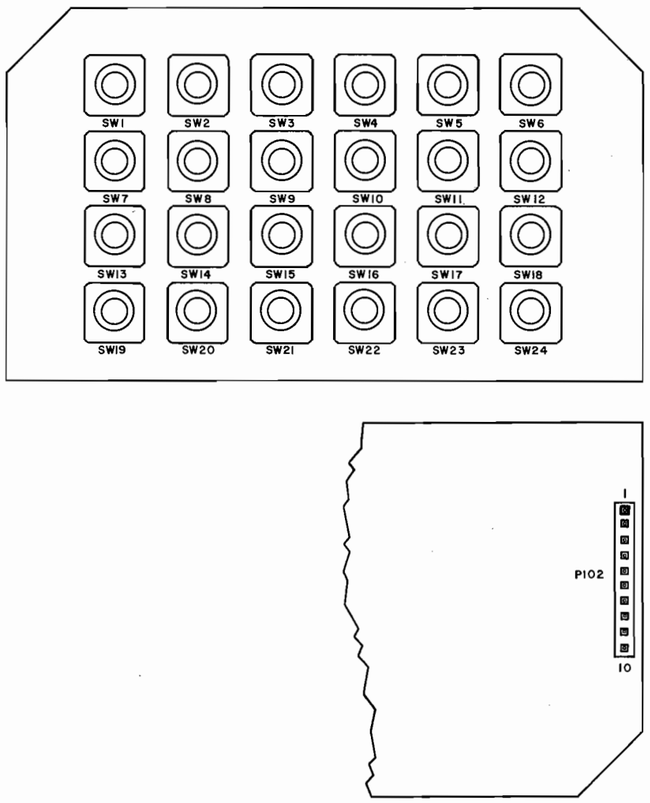
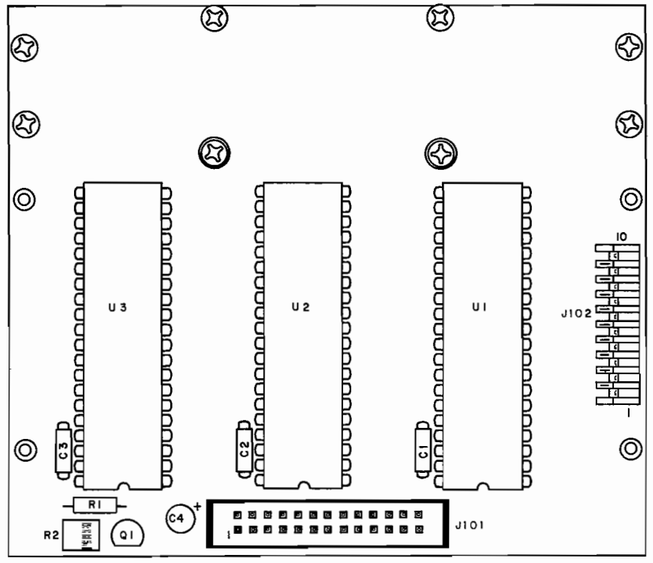
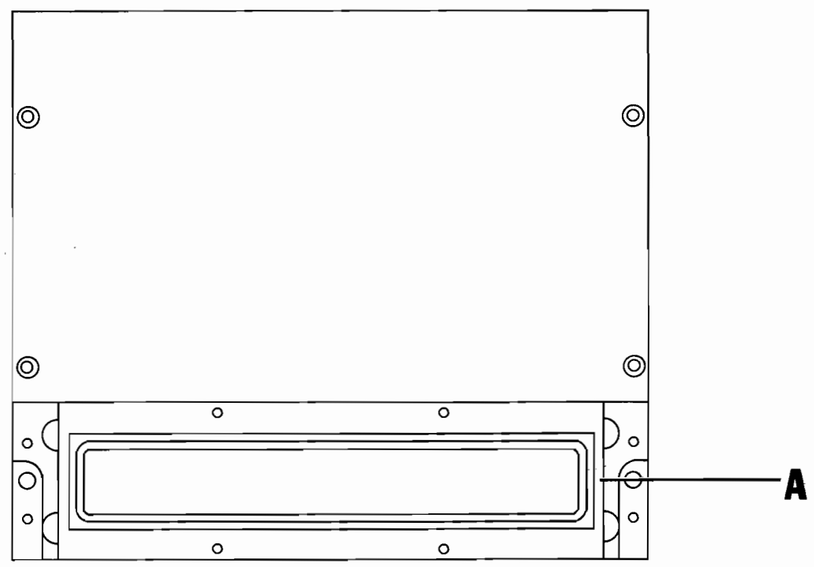


Figure 6-5 Keypad PC Board



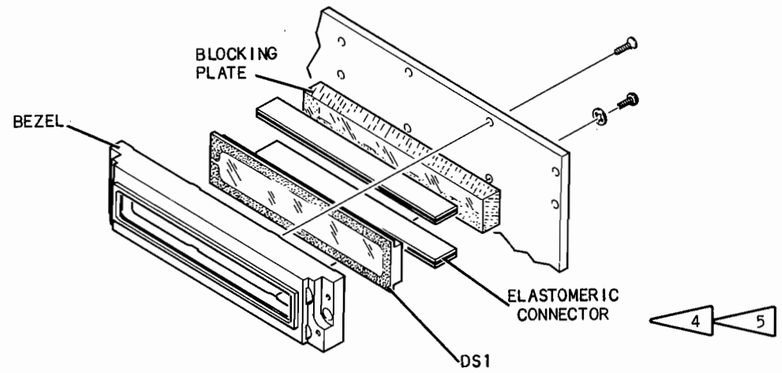
TOP VIEW



BOTTOM VIEW

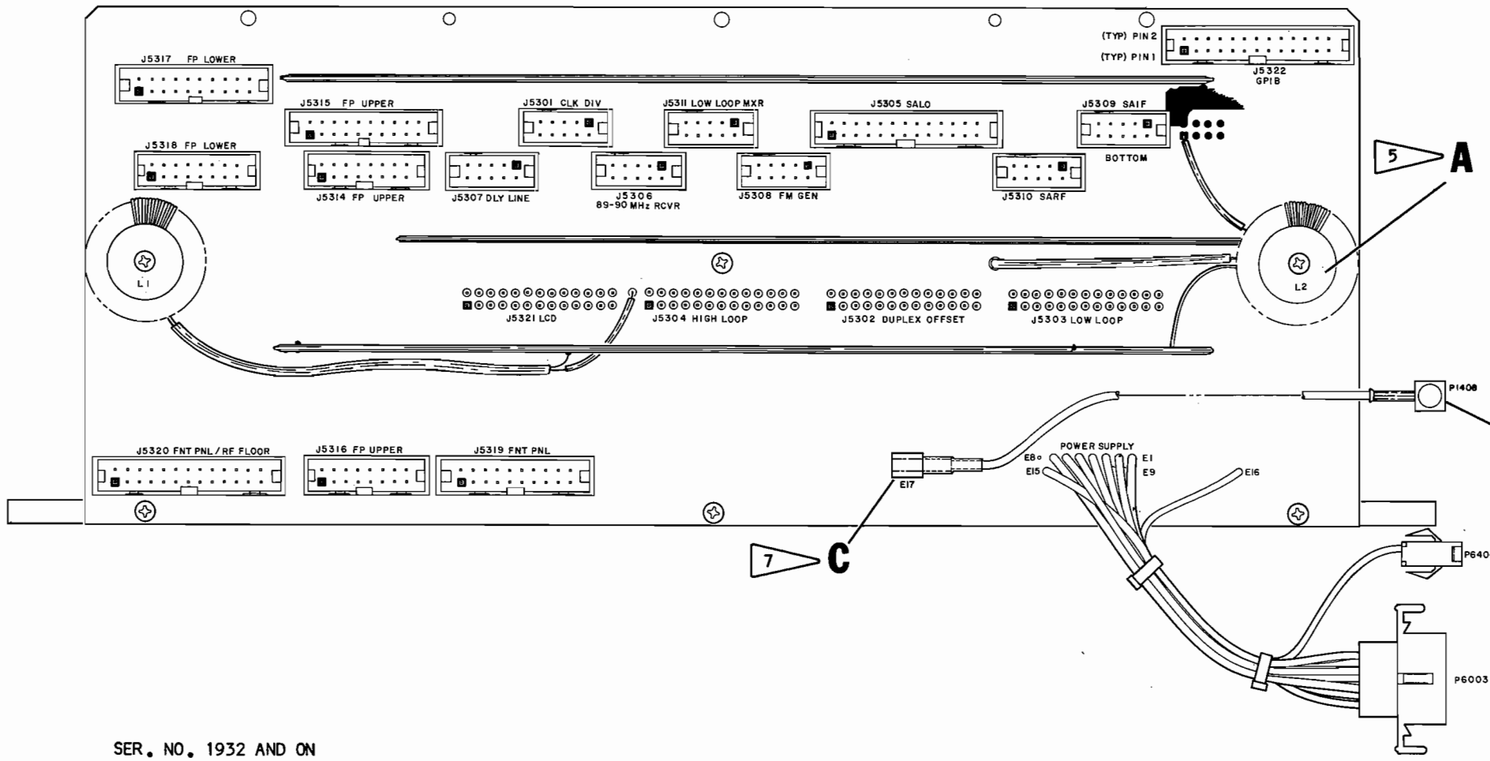
NOTES:

1. THE REF DES SERIES FOR LCD/KEYBOARD PC BOARD ASSY IS 100 (I.E., R1 IS R101).
2. DATA PART NO. 7010-5030-100.
3. REF CIRCUIT SCHEMATIC 0000-5010-100.
4. AVOID EXCESS HANDLING OF LCD ELASTOMERIC CONN AND PC BD BY THEIR CONN SURFACES.
5. TO ASSURE GOOD CLEAN CONTACT SURFACE FOR ELASTOMERIC CONN 2240-0140-042 USE TRICHLOR ON CONN SURFACE ON P.C. BD.

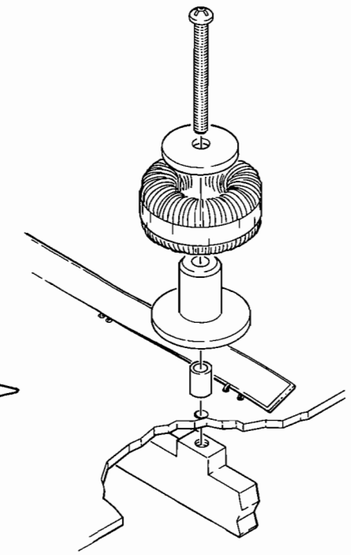


DETAIL **A**

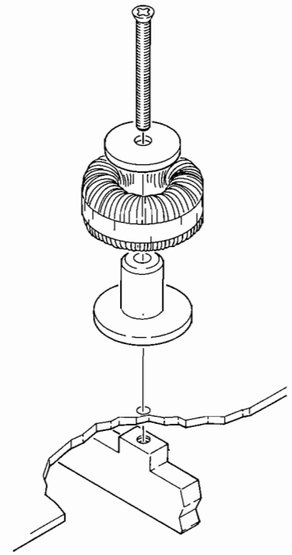
Figure 6-6 LCD/Keyboard PC Board



SER. NO. 1932 AND ON

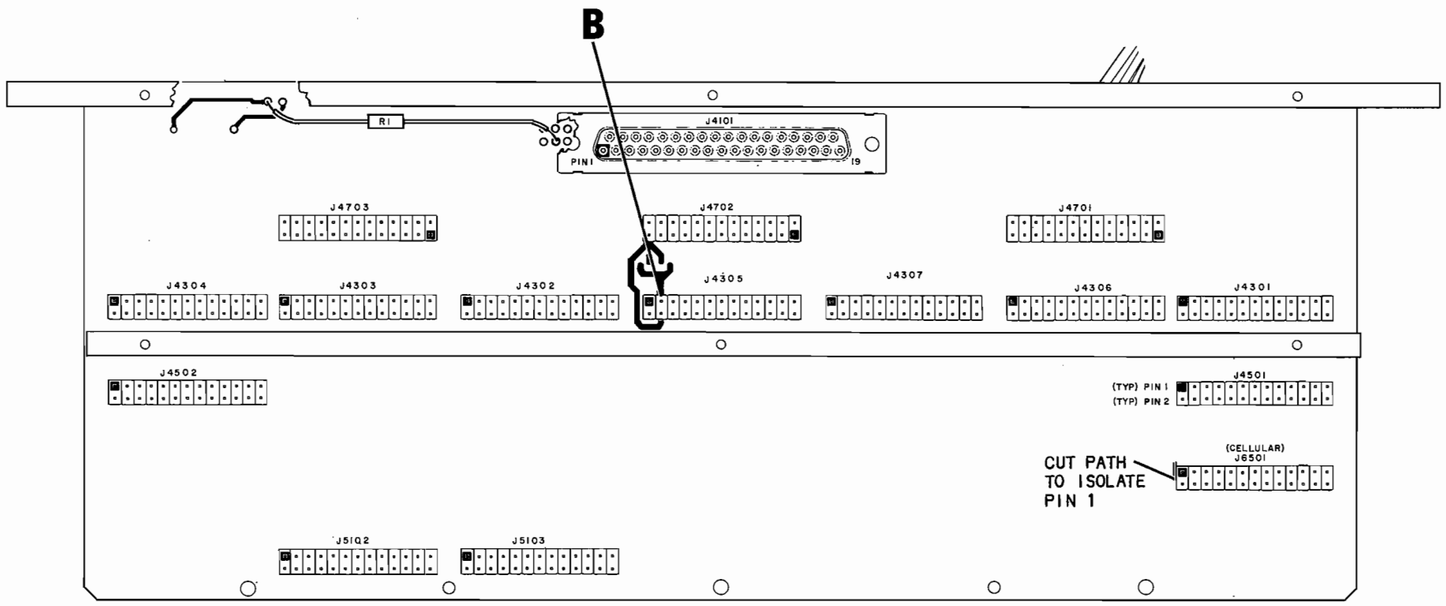


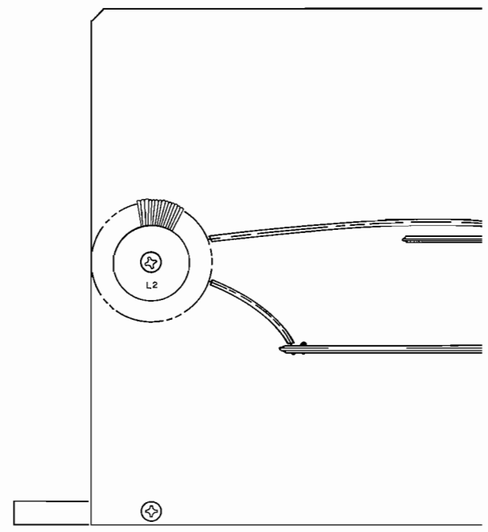
L1: SER. NO. THRU 1931
L2: ALL SER. NO.

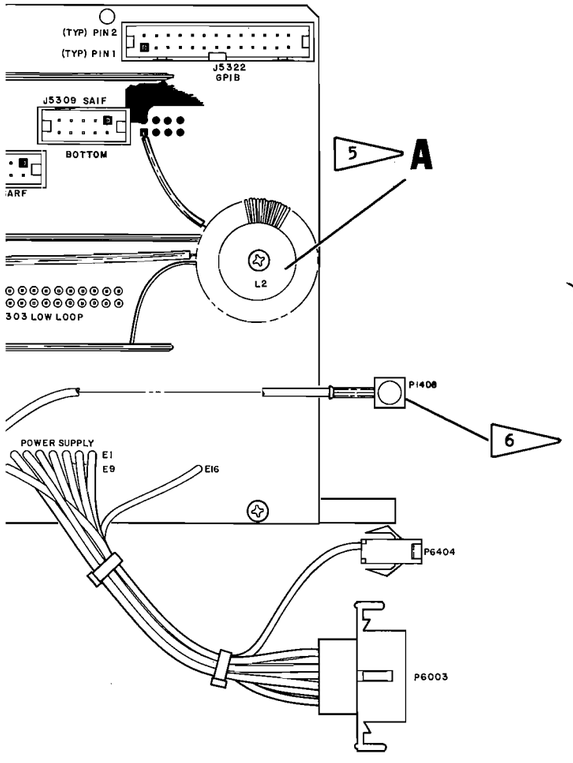


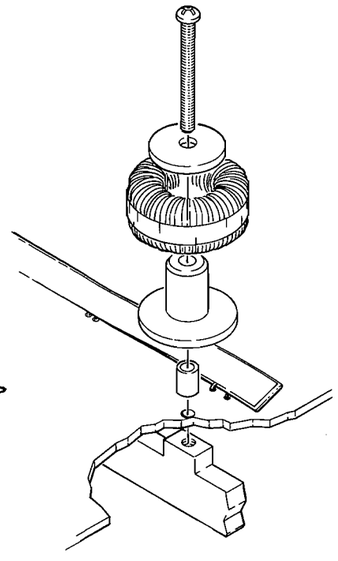
L1: SER. NO. 1932 AND ON

DETAIL A



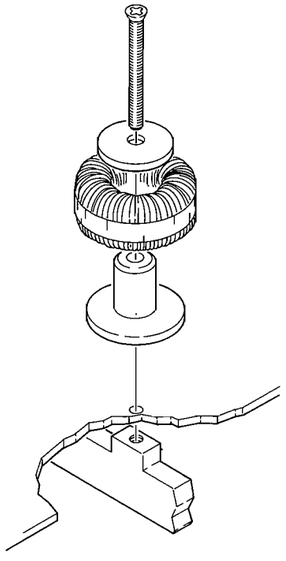




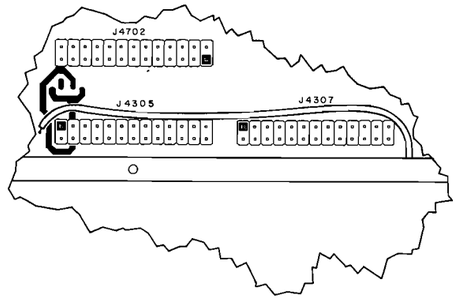


L1: SER. NO. THRU 1931
L2: ALL SER. NO.

DETAIL **A**

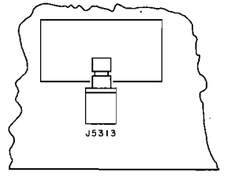


L1: SER. NO. 1932 AND ON



EFFECTIVE UNITS: SER. NO. THRU 1931

DETAIL **B**

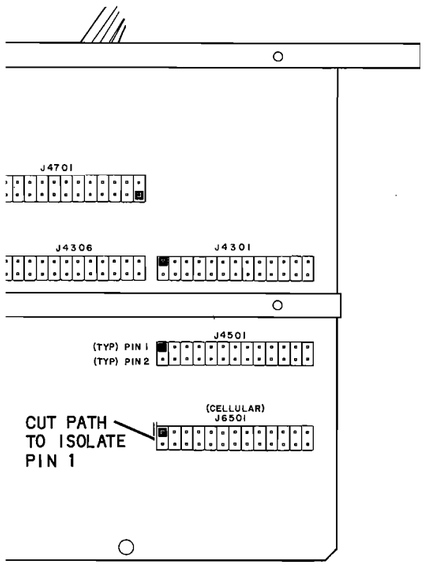


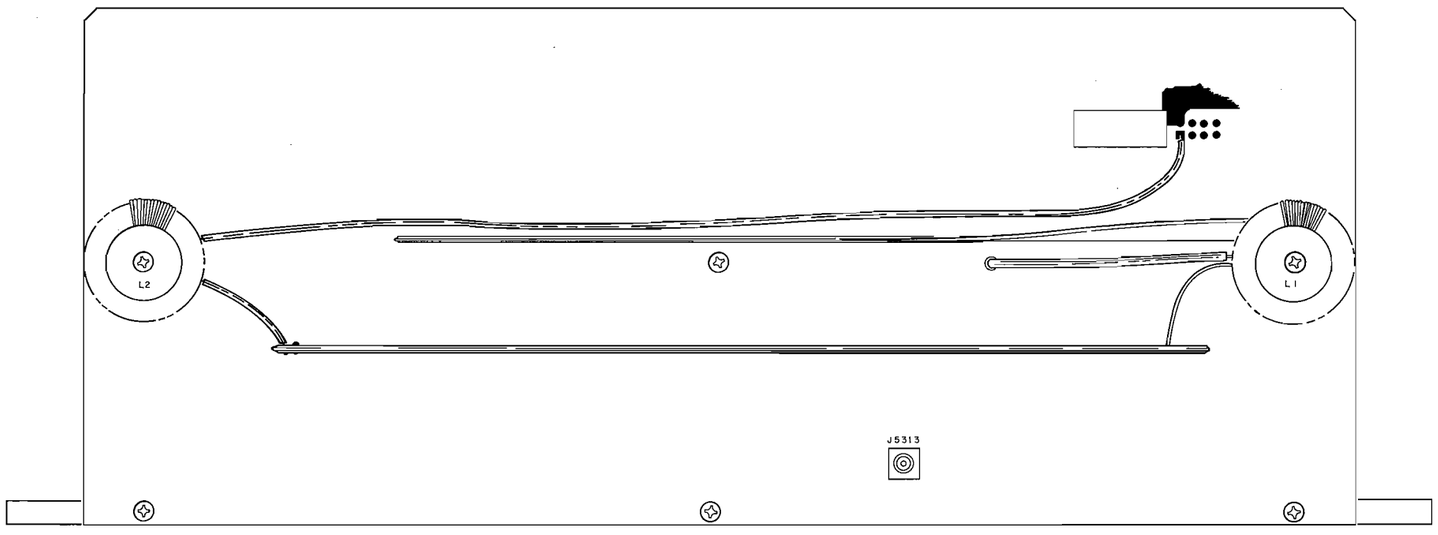
SER. NO. 1932 THRU 2179

DETAIL **C**

NOTES:

1. THE REF DES SERIES FOR MOTHER BOARD MECH ASSY IS 5300 (I.E., J1 IS J5301).
2. DATA PART NO. 7010-5035-300.
3. REF CIRCUIT SCHEMATIC 0000-5015-300.
4. THIS DRAWING TAKES PRECEDENCE OVER ANY EXISTING LABELS INSTALLED IN THE FM/AM-1500.
5. FOR BOARD CONFORMING TO CELLULAR (OPTION 08) REQUIREMENTS ONLY.
6. IF GPIB IS INSTALLED, P1408 BECOMES P1409.
7. EFFECTIVE THRU SER. NO. 2180, E1417 NOT USED.



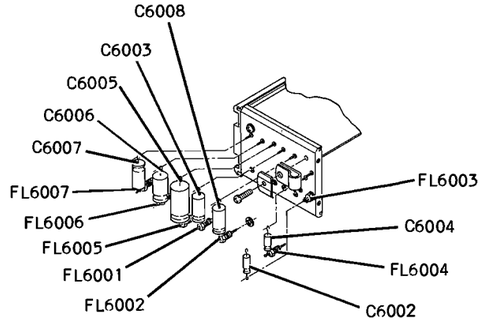


EFFECTIVE UNITS: SER. NO. THRU 1931

Figure 6-7 Motherboard

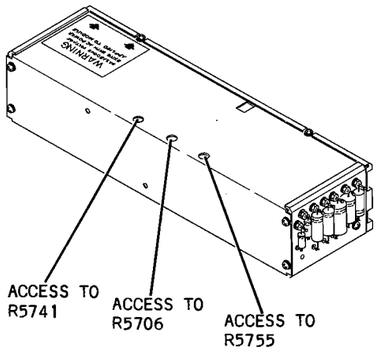
)2

— F6001

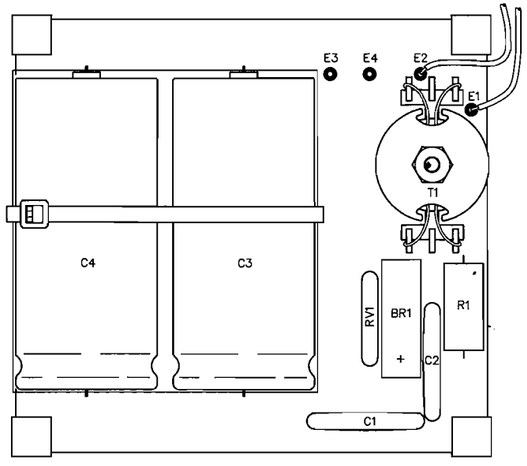


DETAIL **A**

-B

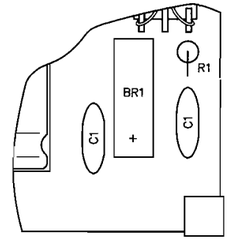


DETAIL **C**



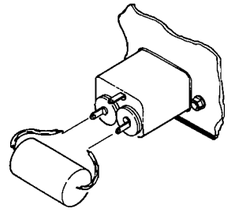
EFFECTIVE SER. NO. 1001
THRU SER. NO. 2656

LINE RECTIFIER PC BD
(5800)



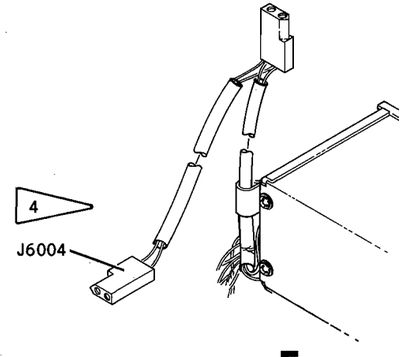
EFFECTIVE SER. NO. 2657 ON

DETAIL **B**



THRU SER. NO. 2270

DETAIL **D**



DETAIL **E**

NOTES:

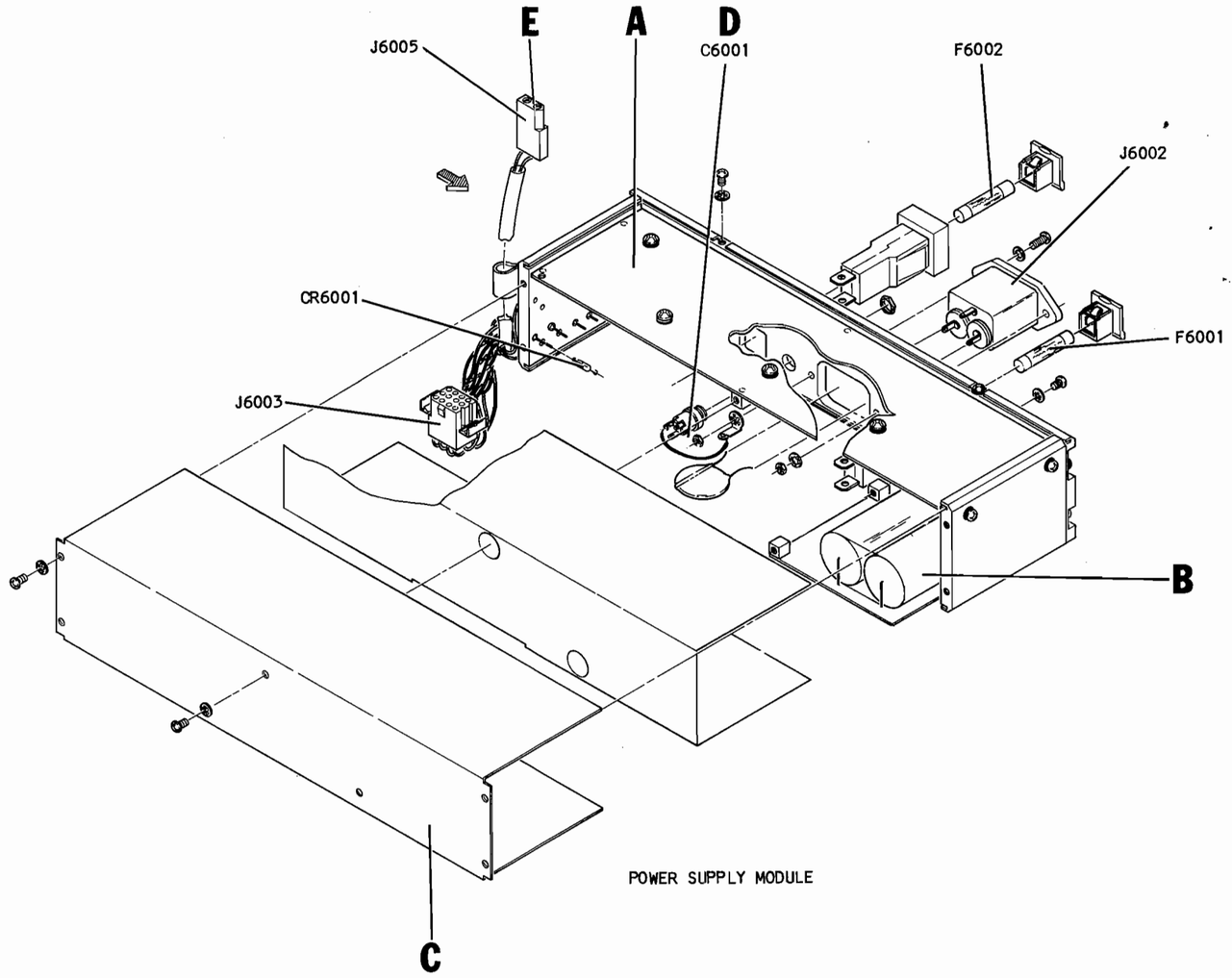
MECH ASSY

1. THE REF DES SERIES FOR THE POWER SUPPLY MECH ASSY IS 6000 (I.E., J1 IS J6001).
2. DATA PART NO. 7005-5045-700.
3. REF CIRCUIT SCHEMATIC 0000-5015-700.
4. EFFECTIVE SER. NO. 2134 AND ON, J6004 NOT USED.

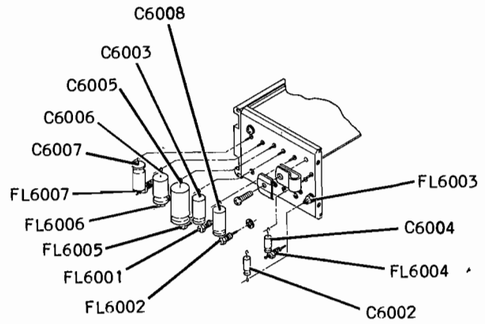
LINE RECTIFIER PC BOARD

1. THE REF DES SERIES FOR THE LINE RECTIFIER PC BOARD ASSY IS 5800, (I.E., C1 IS C5801).
2. DATA PART NO. 7010-5035-800-N2.
3. REF CIRCUIT SCHEMATIC 0000-5015-700.

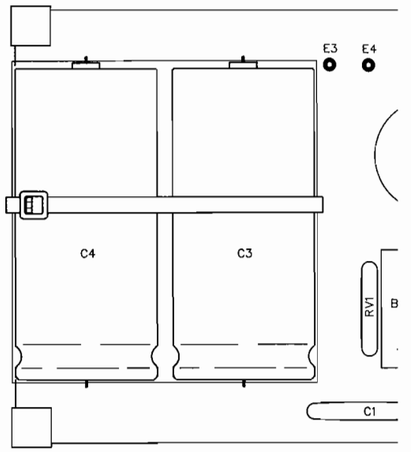
Figure 6-8 Power Supply Module (Sheet 1 of 2)



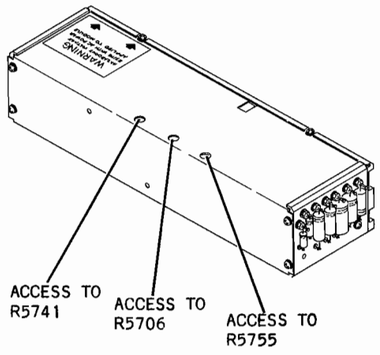
POWER SUPPLY MODULE



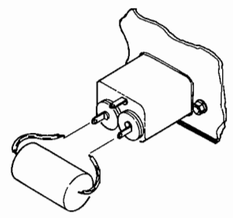
DETAIL **A**



EFFECTIVE SER. NO. 1001
THRU SER. NO. 2656

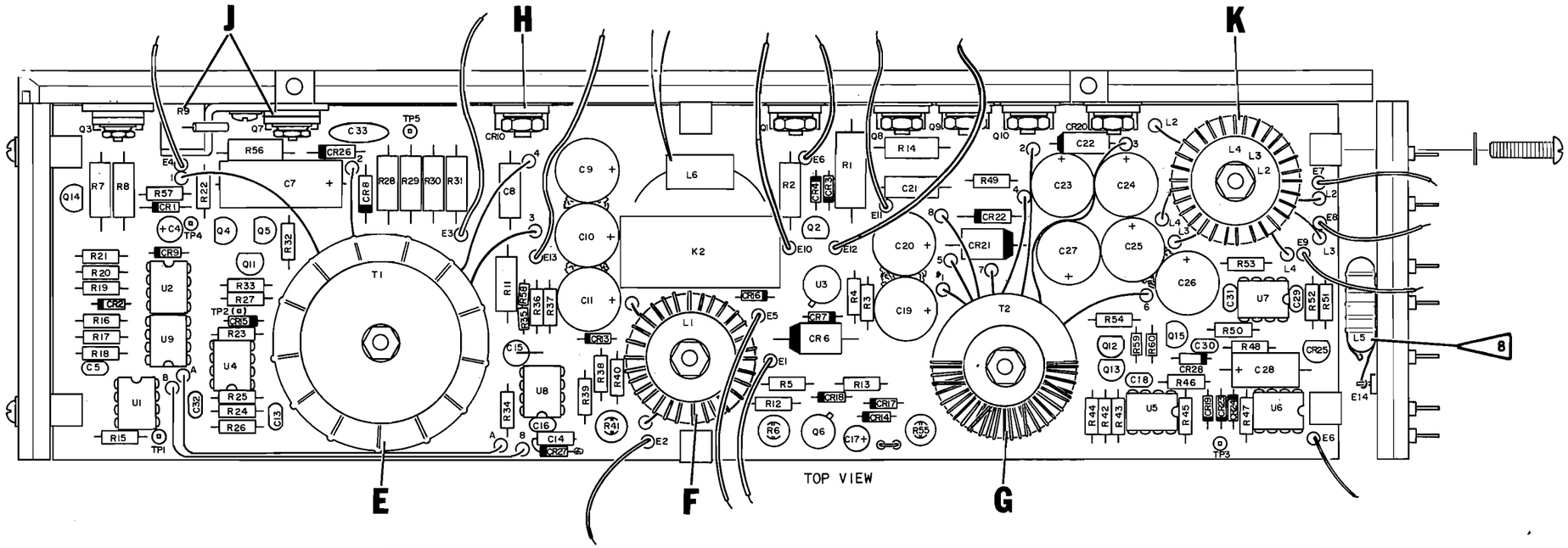


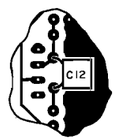
DETAIL **C**



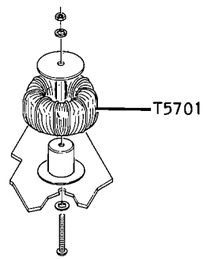
THRU SER. NO. 2270

DETAIL **D**

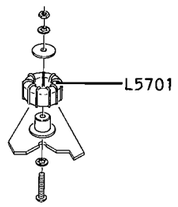




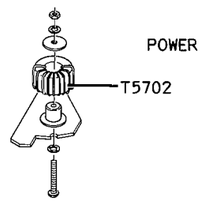
BOTTOM VIEW
POWER SUPPLY PC BOARD (5700)



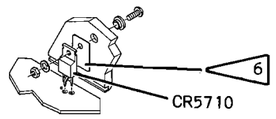
DETAIL **E**



DETAIL **F**

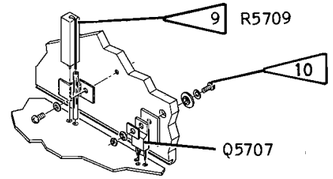


DETAIL **G**



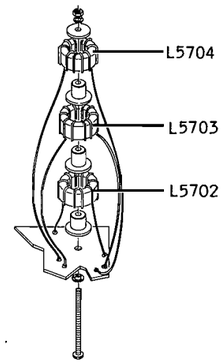
(TYPICAL FOR CR5720, Q5701, Q5708, Q5709, Q5710)

DETAIL **H**

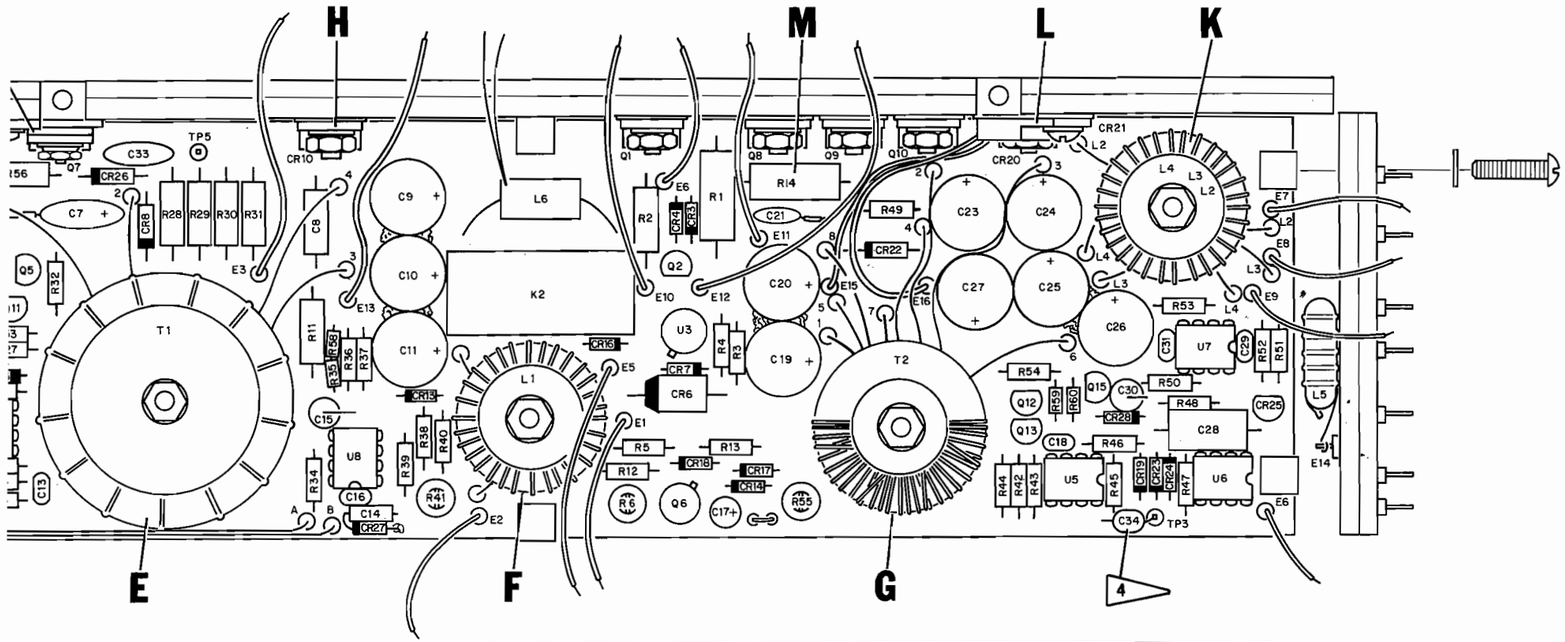


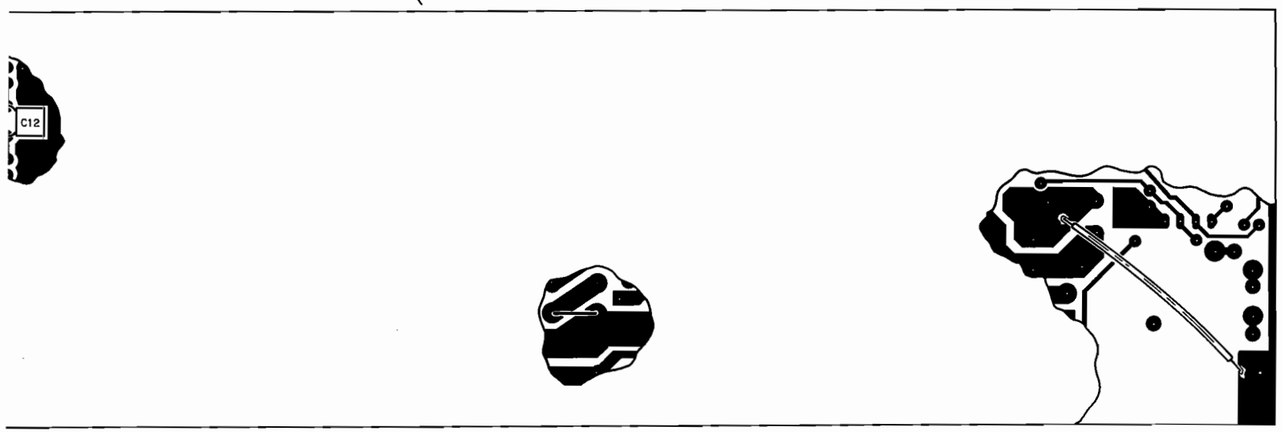
(TYPICAL FOR Q5703)

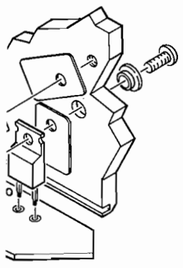
DETAIL **J**



DETAIL **K**

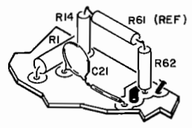






DETAIL **L**

EFFECTIVE SER. NO. 1968 & ON



SER. NO. 1968 THRU 2276

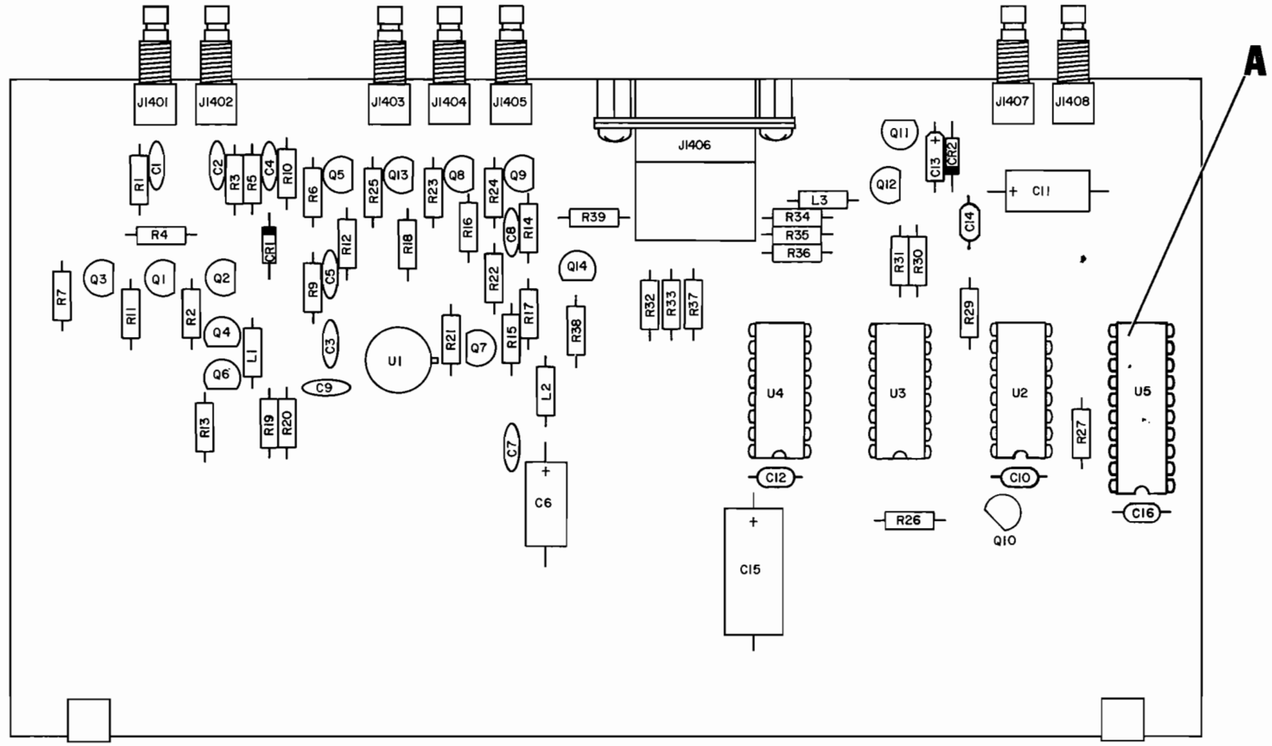
DETAIL **M**

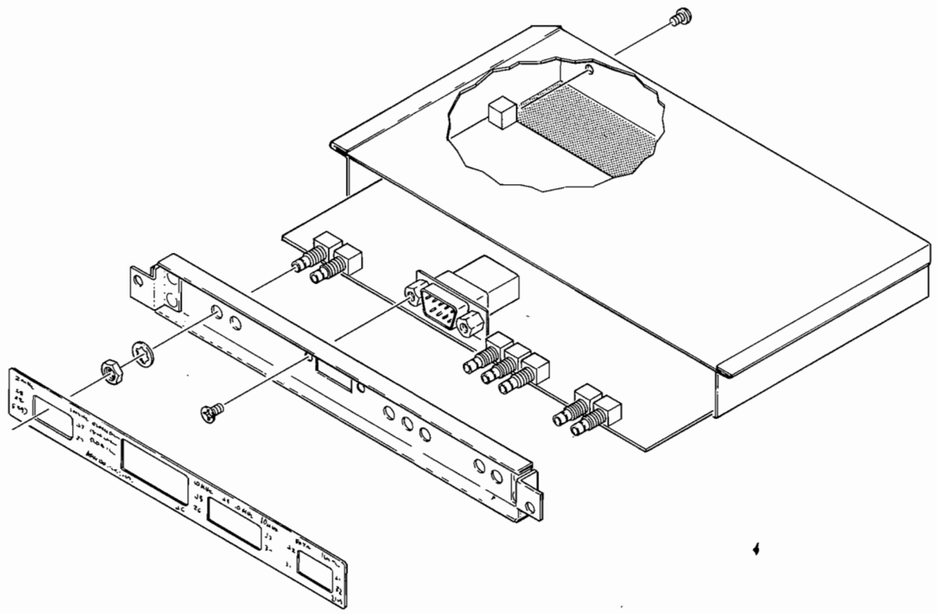
NOTES:

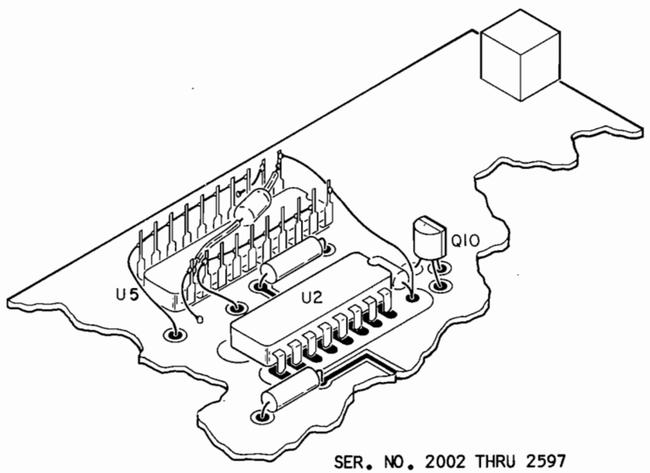
POWER SUPPLY PC BOARD

1. THE REF DES SERIES FOR POWER SUPPLY PC BOARD ASSY IS 5700 (I.E., R1 IS R5701).
2. DATA PART NO. 7010-5035-700.
3. REF CIRCUIT SCHEMATIC 0000-5015-700.
4. EFFECTIVE THRU SER. NO. 1967, C34, R61 AND R62 NOT USED. (SEE ALSO DETAIL M)
5. DO NOT USE ANY SILICONE GREASE OR THERMAL COMPOUND.
6. ASSEMBLE WITH SILICONE GREASE. DO NOT USE THE THERMAL COMPOUND.
7. NOT USED.
8. ATTACH L5 USING TAC-PAC ADHESIVE/ EQUIVALENT.
9. APPLY THERMAL COMPOUND BETWEEN RESISTOR AND POWER SUPPLY PLATE.
10. APPLY RTV SEALANT AROUND SCREW HEADS AFTER INSTALLATION.

Figure 6-8 Power Supply Module (Sheet 2 of 2)

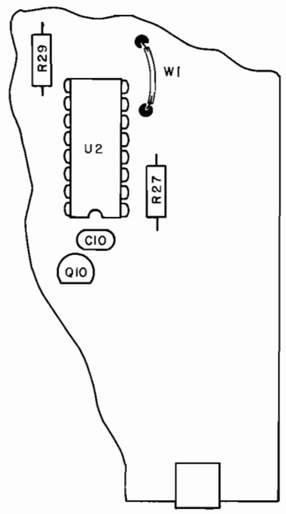




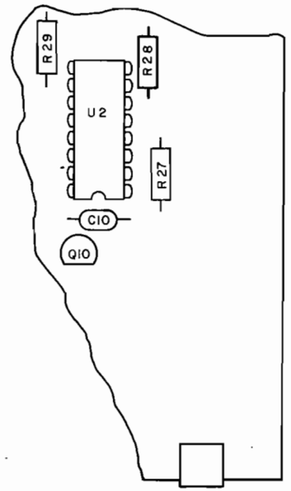


SER. NO. 2002 THRU 2597

DETAIL **A**



SER. NO. 1968 THRU 2001



THRU SER. NO. 1967

NOTES:

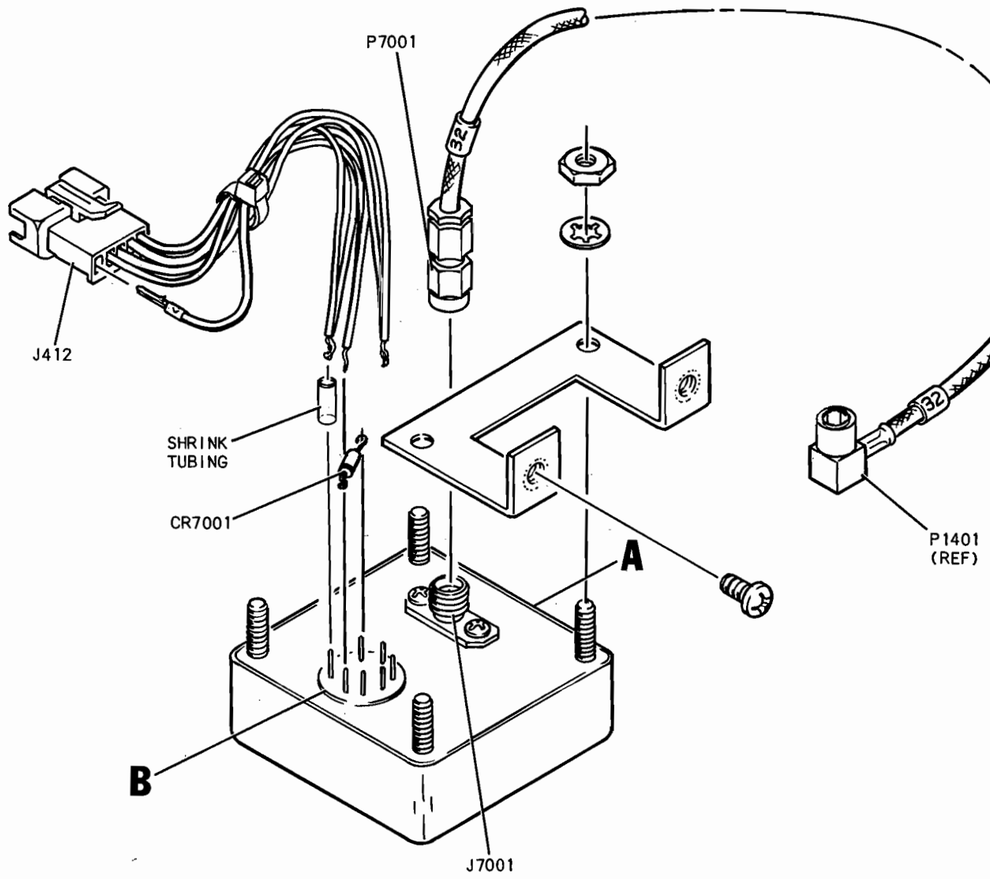
MECH ASSY

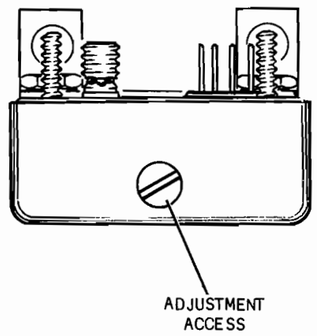
1. THE REF DES SERIES FOR THE CLOCK DIVIDER MECH ASSY IS 1400 (I.E., J1 IS J1401).
2. DATA PART NO. 7005-5041-700.
3. REF CIRCUIT SCHEMATIC 0000-5011-700.

PC BOARD

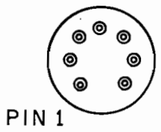
1. THE REF DES SERIES FOR THE CLOCK DIVIDER PC BOARD ASSY IS 1700 (I.E., R1 IS 1701).
2. DATA PART NO. 7010-5031-700.
3. THRU SER. NO. 2001: U5 AND C16 NOT USED. U2A PIN 1 AND 6 CONNECTED TO J1409, Q9 COLLECTOR AND R9 CONNECTED TO J1408.

Figure 6-10 Clock Divider Module





DETAIL **A**



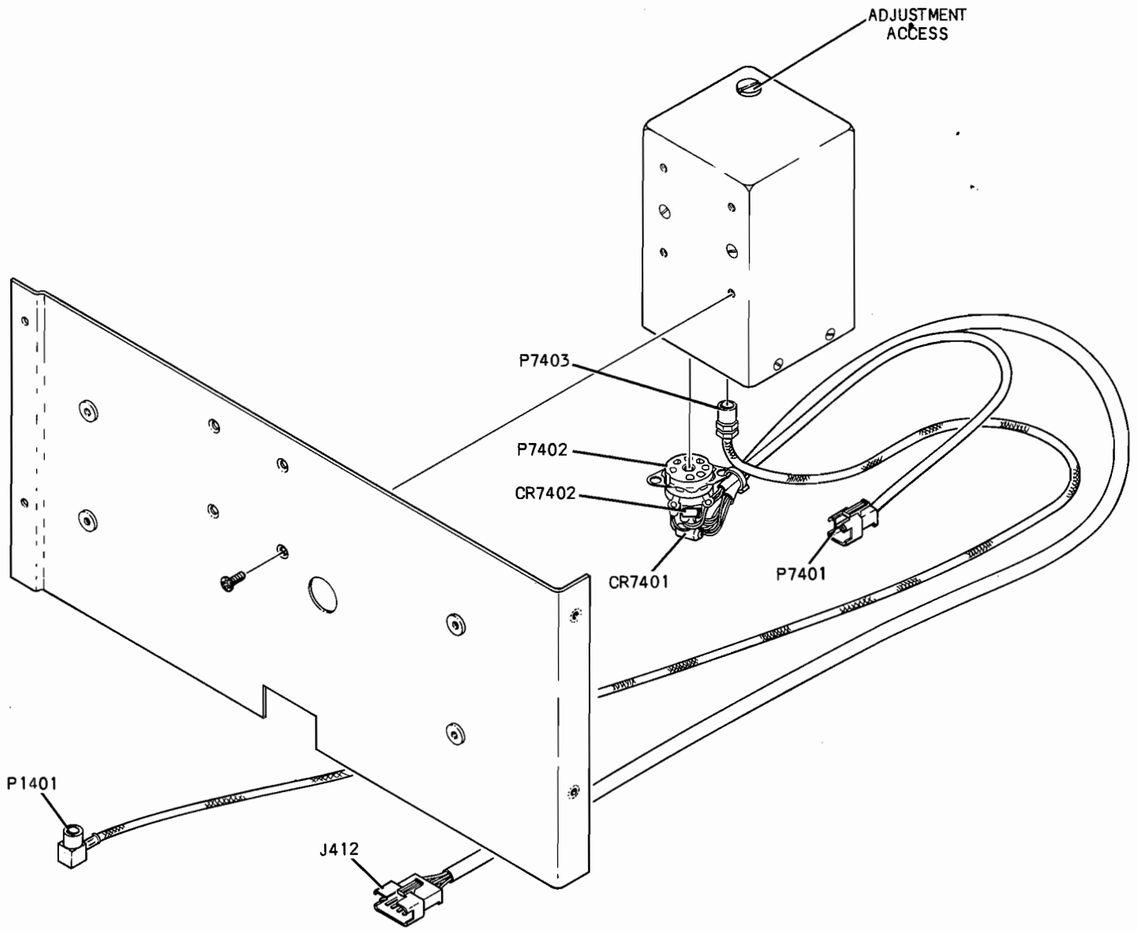
DETAIL **B**

NOTES:

1. THE REF DES SERIES FOR THE TCXO MECH ASSY IS 7000 (I.E., J1 IS J7001).
2. DATA PART NO. 7001-5086-800.
3. REF INTERCONNECT 0000-5017-400.

WIRE RUNNING LIST				
FROM	TO	COLOR	AWG	LENGTH
J412-1	E6	RED	26	3"
J412-2	E6	RED	26	3"
J412-3	E7	GRN	26	3"
J412-4	E3	BLK	26	3"
J412-5	E3	BLK	26	3"
N/C	E2	---	--	--
N/C	E4	---	--	--
N/C	E5	---	--	--
CR7001 GOES FROM E6(+) TO E1(-).				

Figure 6-11 TCXO



WIRE RUNNING LIST				
FROM	TO	COLOR	AWG	LENGTH
P7401-1	P7402-3	BLK	26	8.25
P7401-2	P7402-1	WHT/RED	26	8.25
J412-5	P7402-3	BLK	26	22
J412-3	P7402-4	YEL	26	22
J412-4	P7402-6	BLU	26	22
J412-2	P7402-5	ORN	26	22
J412-1	P7402-7	RED	26	22

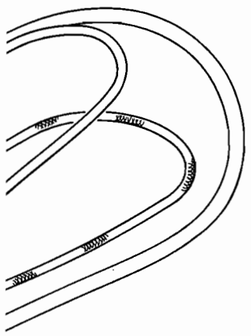
DIODE CR7402 GOES FROM P7402-1(+) TO P7402-2(-).
DIODE CR7401 GOES FROM P7402-2(-) TO P7402-7(+).

NOTES:

1. THE REF DES SERIES FOR THE OVEN OSCILLATOR MECH ASSY IS 7400 (I.E., J1 IS J7401).
2. DATA PART NO 7001-5046-500.
3. REF WIRE HARNESS SCHEMATIC/ INTERCONNECT 0000-5017-500.

JUSTMENT
\CCESS

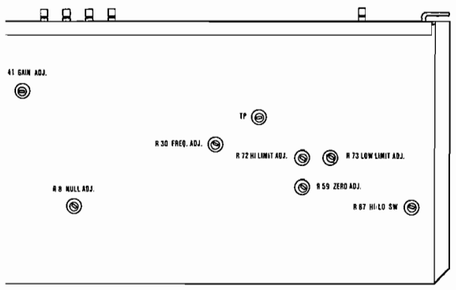
WIRE RUNNING LIST				
FROM	TO	COLOR	AWG	LENGTH
P7401-1	P7402-3	BLK	26	8.25
P7401-2	P7402-1	WHT/RED	26	8.25
J412-5	P7402-3	BLK	26	22
J412-3	P7402-4	YEL	26	22
J412-4	P7402-6	BLU	26	22
J412-2	P7402-5	ORN	26	22
J412-1	P7402-7	RED	26	22
DIODE CR7402 GOES FROM P7402-1(+) TO P7402-2(-). DIODE CR7401 GOES FROM P7402-2(-) TO P7402-7(+).				

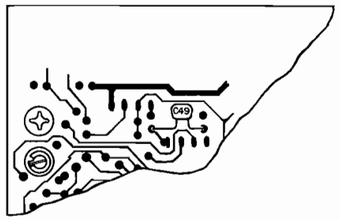


NOTES:

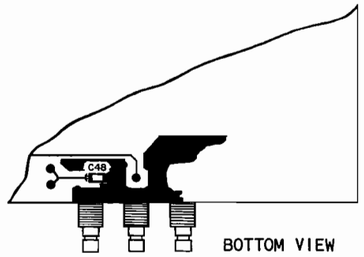
1. THE REF DES SERIES FOR THE OVEN OSCILLATOR MECH ASSY IS 7400 (I.E., J1 IS J7401).
2. DATA PART NO 7001-5046-500.
3. REF WIRE HARNESS SCHEMATIC/ INTERCONNECT 0000-5017-500.

Figure 6-12 Oven Oscillator (Option 02)

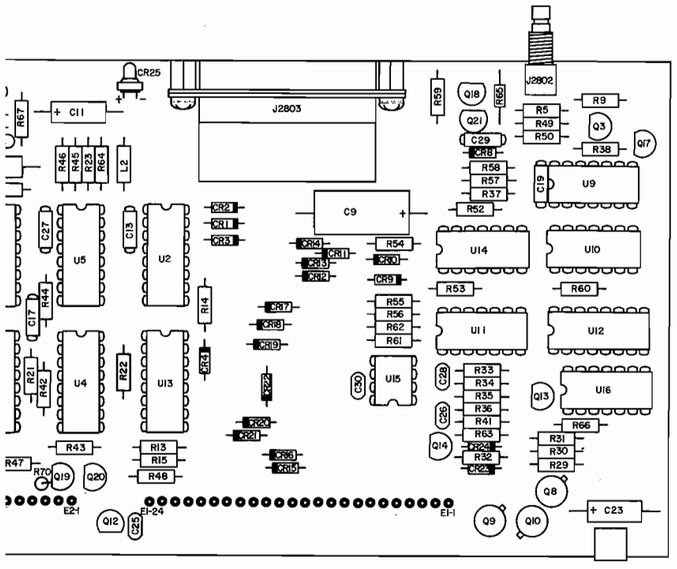


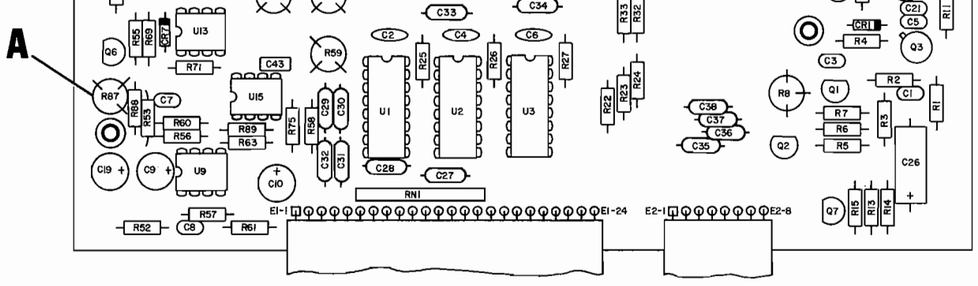


DETAIL **A**

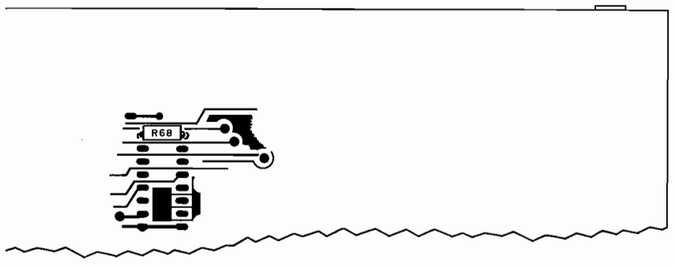


BOTTOM VIEW





HIGH LOOP #2 (ANALOG)



HIGH LOOP #1 (DIGITAL)

NOTES:

MECH ASSY

1. THE REF DES SERIES FOR THE HIGH LOOP MECH ASSY IS 2800, (I.E., J1 IS J2801).
2. DATA PART NO. 7005-5042-300.
3. REF CIRCUIT SCHEMATIC 0000-5012-100-D1 AND 0000-5012-300-J1.

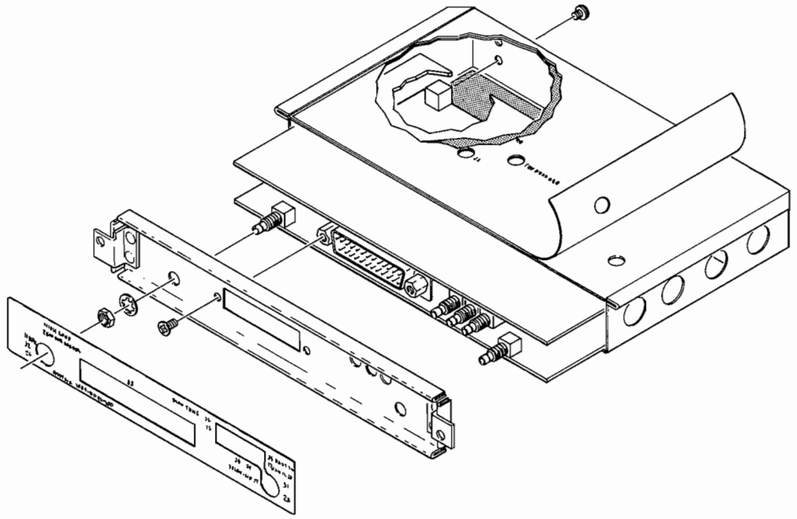
HIGH LOOP #1 (DIGITAL) PC BOARD

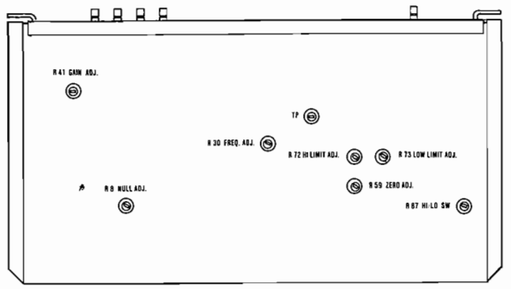
1. THE REF DES SERIES FOR HIGH LOOP #1 PC BOARD ASSY IS 2200 (I.E., R1 IS R2201).
2. DATA PART NO. 7010-5032-100.
3. REF CIRCUIT SCHEMATIC 0000-5012-100.
4. TRANSISTOR COLLECTOR LEAD INDICATED BY DOT ON Q1 AND Q2.

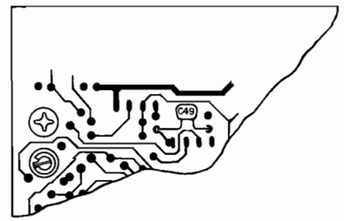
HIGH LOOP #2 (ANALOG) PC BOARD

1. THE REF DES SERIES FOR HIGH LOOP #2 PC BOARD ASSY IS 2300 (I.E., R1 IS R2301).
2. DATA PART NO. 7010-5032-300.
3. REF CIRCUIT SCHEMATIC 0000-5012-300.

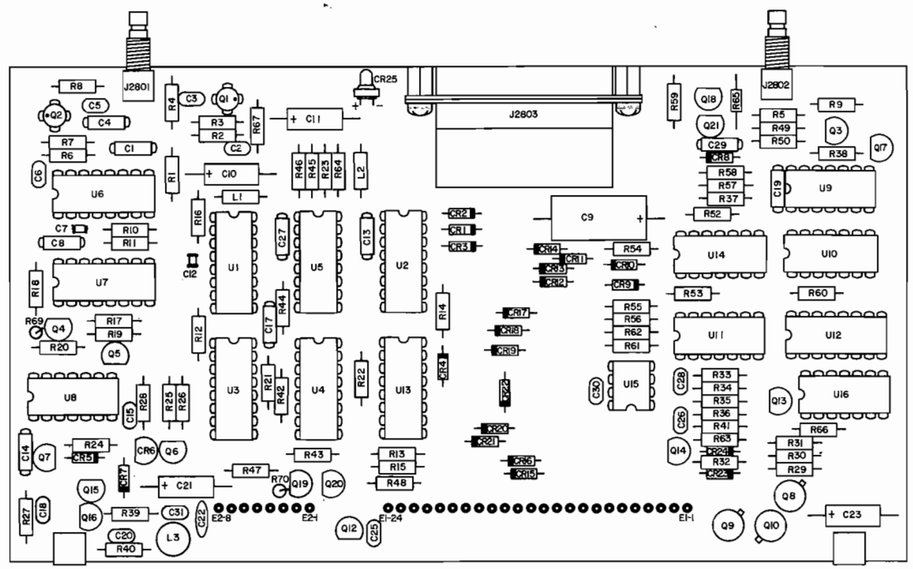
Figure 6-13 High Loop Module

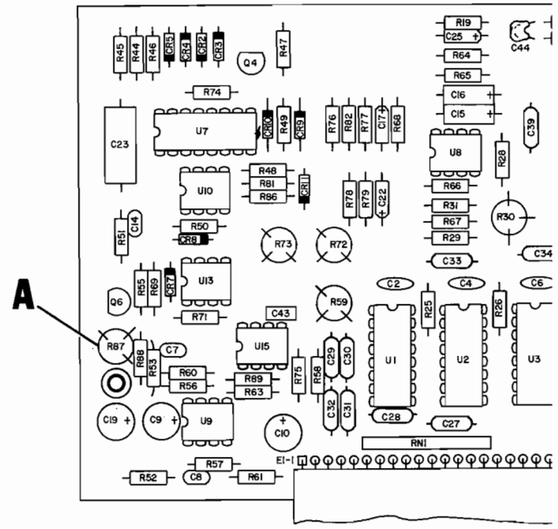




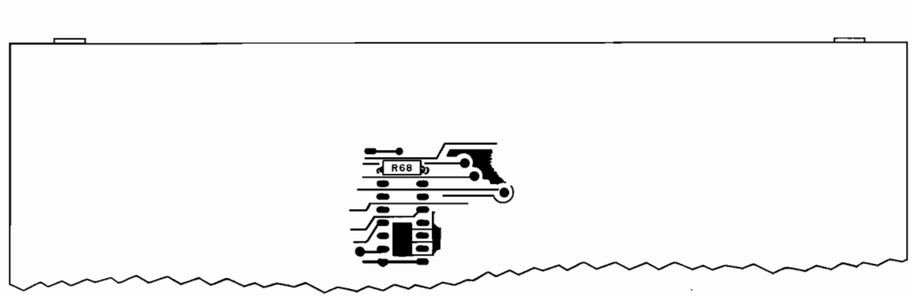


DETAIL **A**

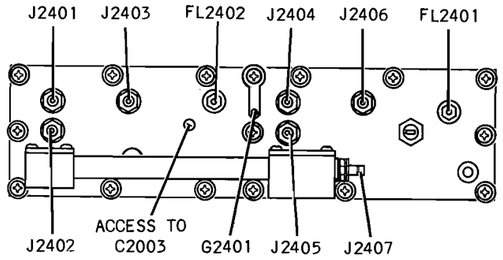


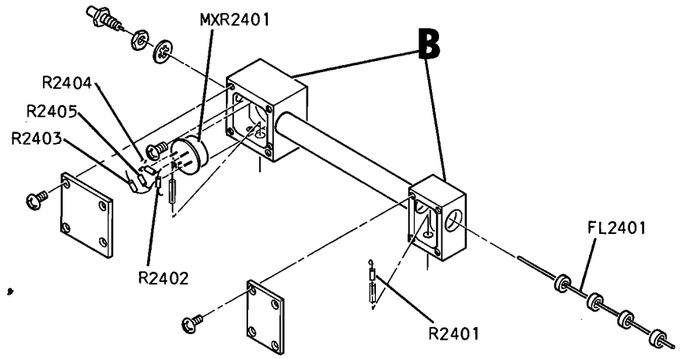


HIGH LOOP #2

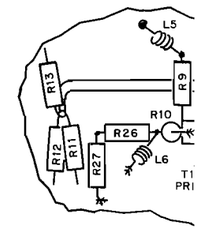


HIGH LOOP #1 (DIGITAL)

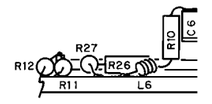


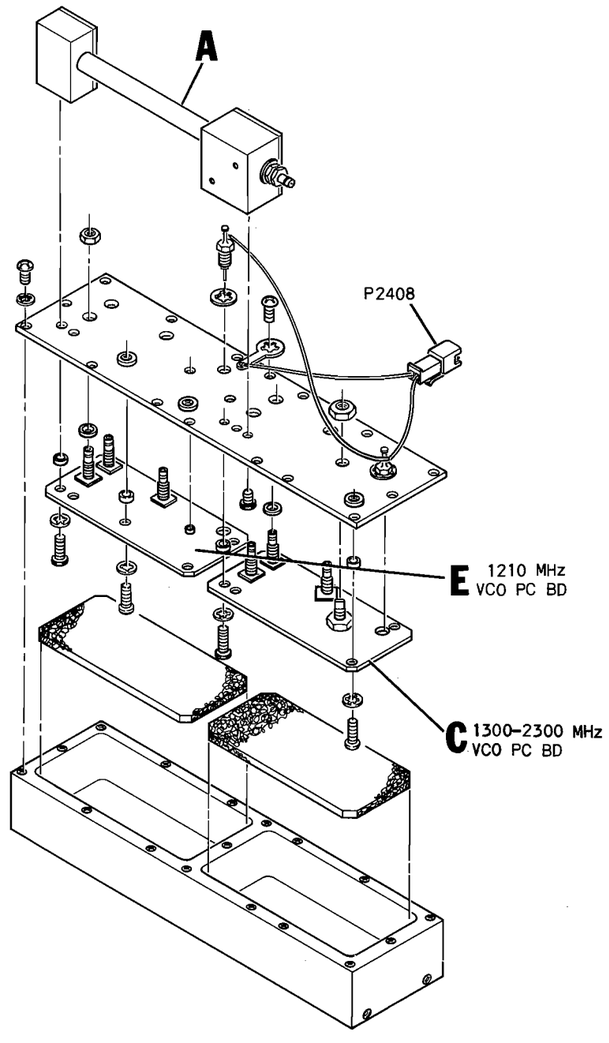


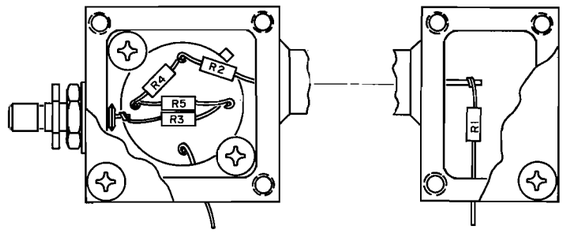
DETAIL **A**



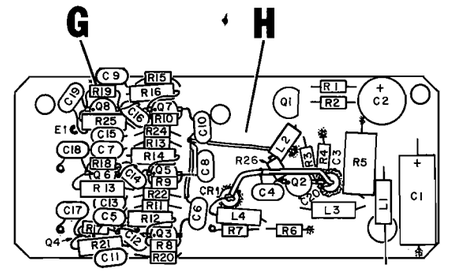
T1 { PRIMA
SECONDA

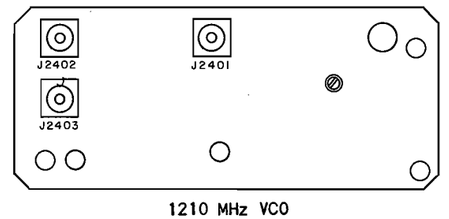






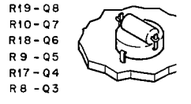
DETAIL **B**



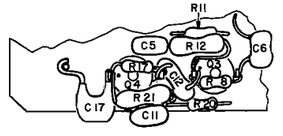


1210 MHz VCO

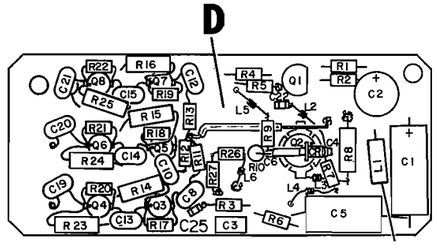
DETAIL **E**

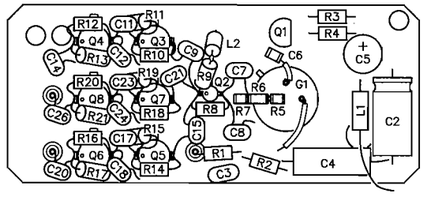


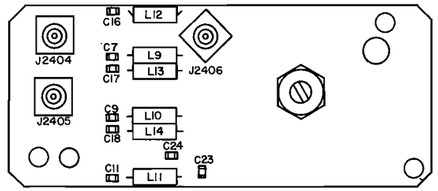
DETAIL **G**



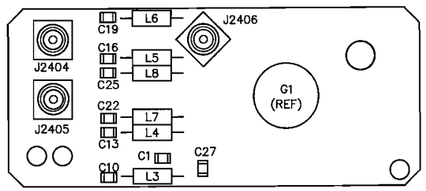
DETAIL **F**





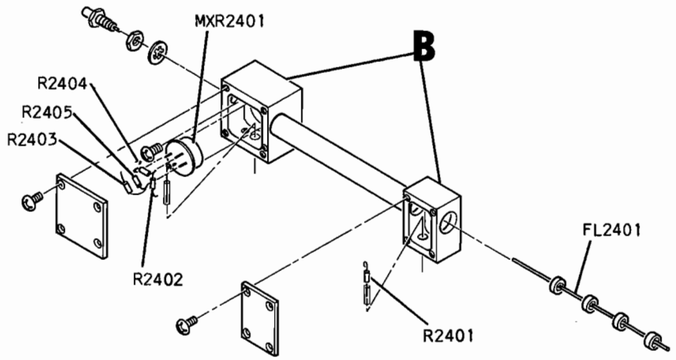


1300-2300 MHz VCO PC BD
THRU SER. NO. 2444

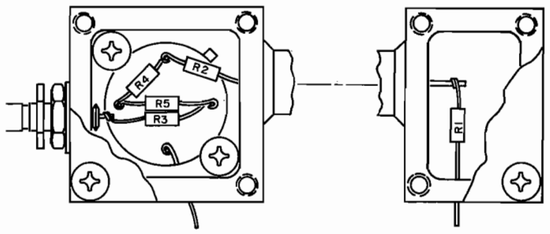


1300-2300 MHz VCO PC BD

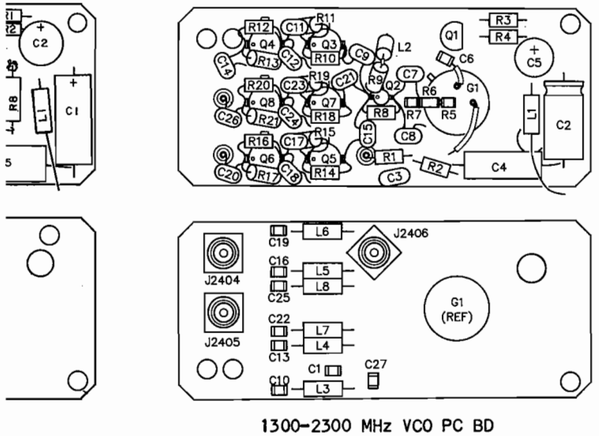
DETAIL **C**



DETAIL **A**

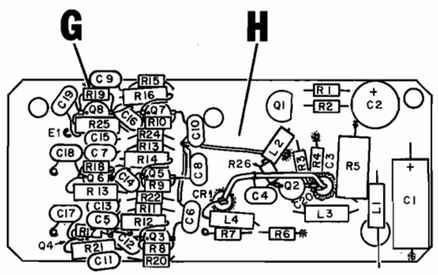


DETAIL **B**



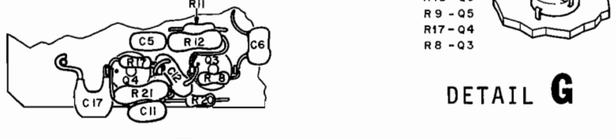
1300-2300 MHz VCO PC BD

DETAIL **C**



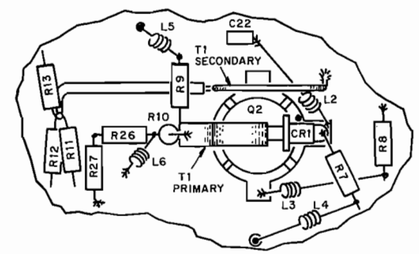
1210 MHz VCO

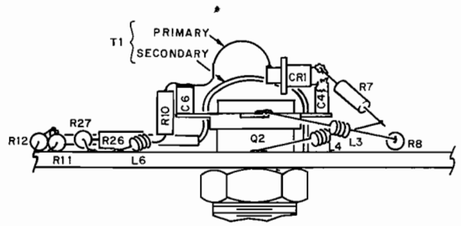
DETAIL **E**



DETAIL **F**

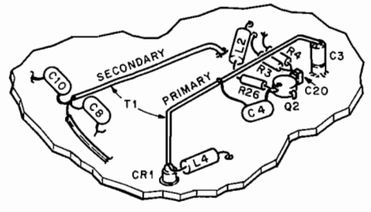
DETAIL **G**





DETAIL **D**

WIRE RUNNING LIST				
FROM	TO	COLOR	AWG	LENGTH
P2408-2	G2401	BLK	.26	3"
P2408-1	FL2401	RED	26	3"
FL2401	FL2402	RED	26	4"



DETAIL **H**

NOTES:

MECH ASSY

1. THE REF DES SERIES FOR THE DUAL VCO MECH ASSY IS 2400 (I.E., J1 IS J2401).
2. DATA PART NO. 7005-5242-101.
3. REF CIRCUIT SCHEMATIC 0000-5012-001-L3 AND 0000-5012-101-L2 (THRU SER. NO. 2444) OR 0000-5012-102-A1 (SER. NO. 2445 AND ON).

1210 MHz VCO PC BOARD

1. THE REF DES SERIES FOR THE 1210 MHz VCO PC BOARD IS 2000 (I.E., R1 IS R2001).
2. DATA PART NO. 7010-5232-001.
3. REF CIRCUIT SCHEMATIC 0000-5012-001-L3 AND 0000-5012-101-L2 (THRU SER. NO. 2444) OR 0000-5012-102-A1 (SER. NO. 2445 AND ON).

1300-2300 MHz VCO PC BOARD

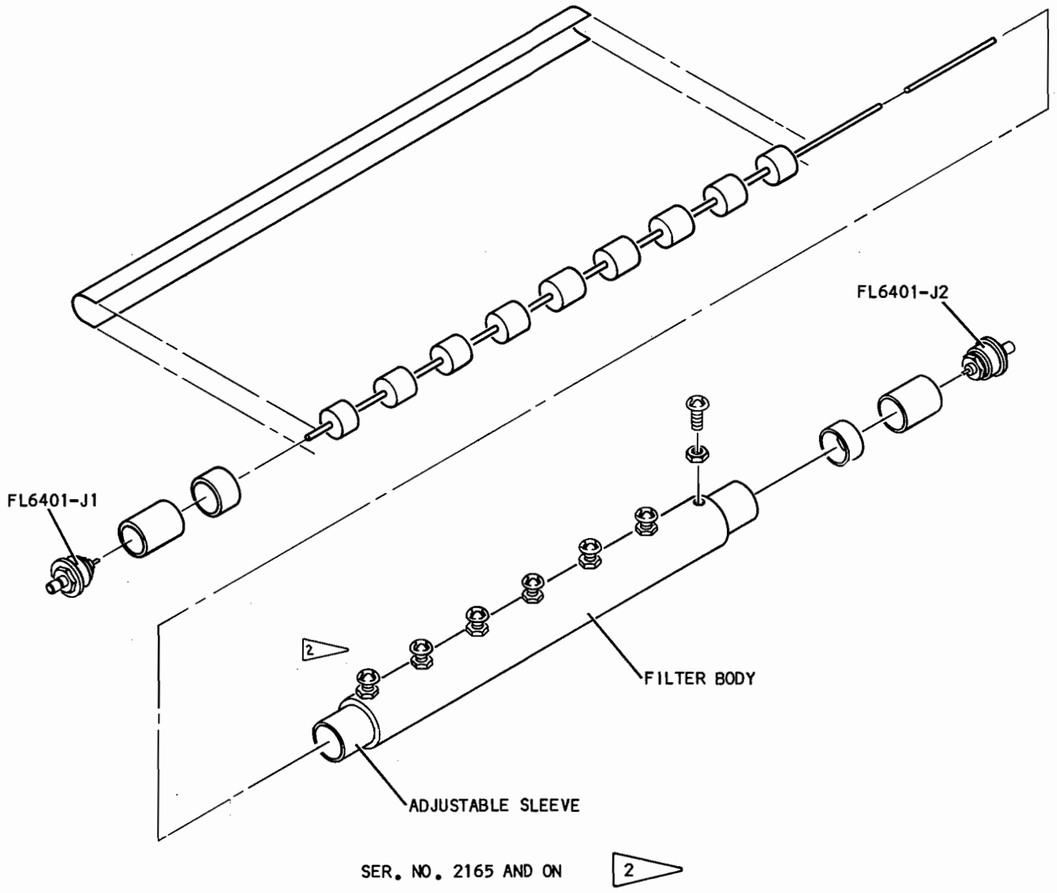
1. THE REF DES SERIES FOR 1300-2300 MHz VCO PC BOARD IS 2100 (I.E., R1 IS R2101).
2. DATA PART NO. THRU SER. NO. 2444 7010-5232-101, SER. NO. 2445 AND ON 7010-5232-102.
3. REF CIRCUIT SCHEMATIC 0000-5012-001-L3 AND 0000-5012-101-L2 (THRU SER. NO. 2444) OR 0000-5012-102-A1 (SER. NO. 2445 AND ON).

Figure 6-14 Dual VCO Module

NOTES:

1. THE LOW PASS FILTER IS PART OF THE COMPOSITE MECH ASSY. ITS REF DES SERIES IS FL6401 (I.E., J1 IS FL6401-J1).

2. DATA PART NO. THRU SER. NO. 2164 IS 7005-5241-800; EFFECTIVE SER. NO. 2165 AND ON, DATA PART NO. 7005-5241-801.



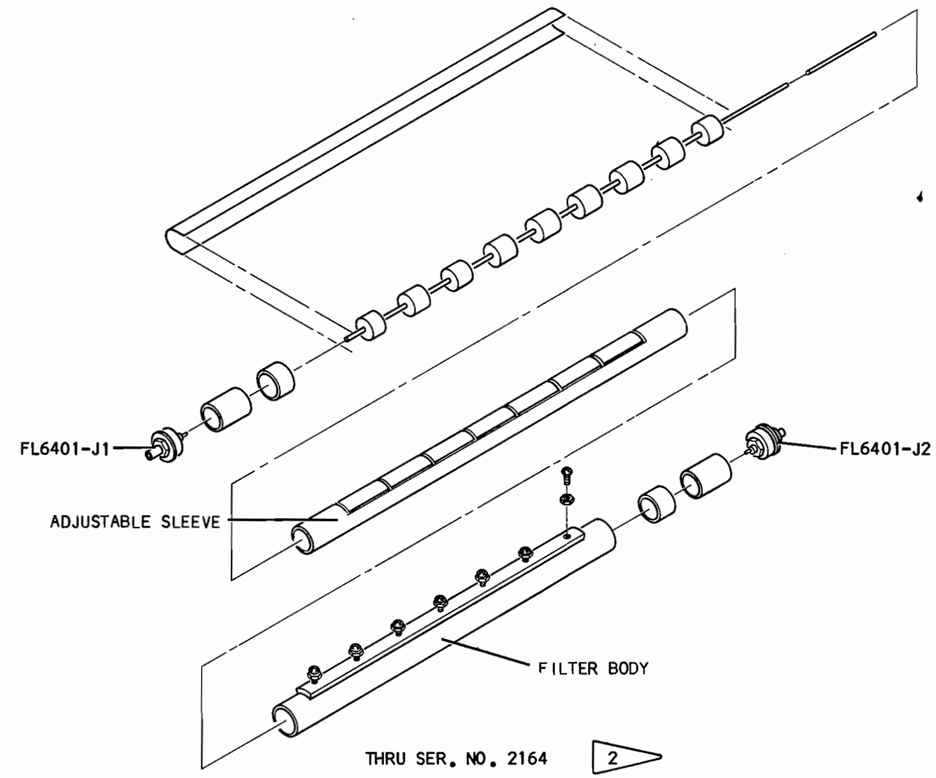
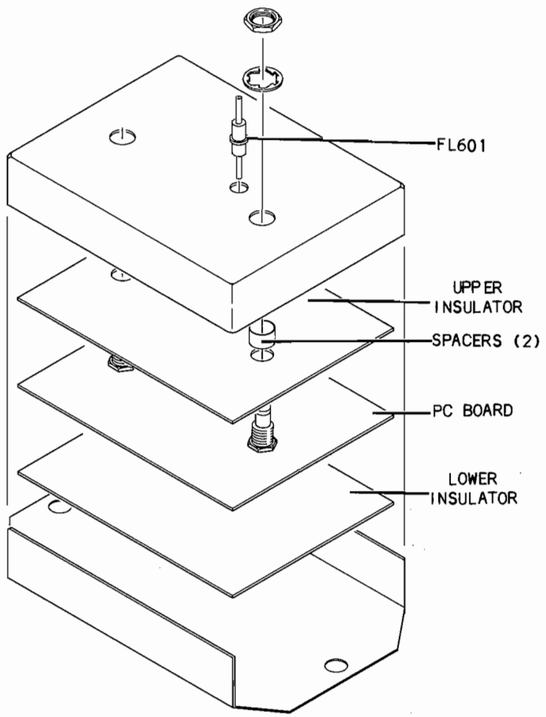
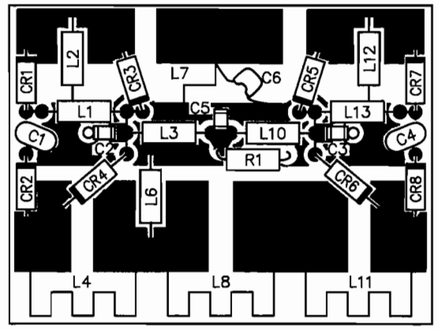
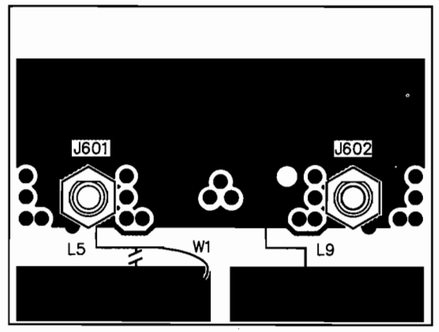


Figure 6-15 Low Pass Filter







NOTES:

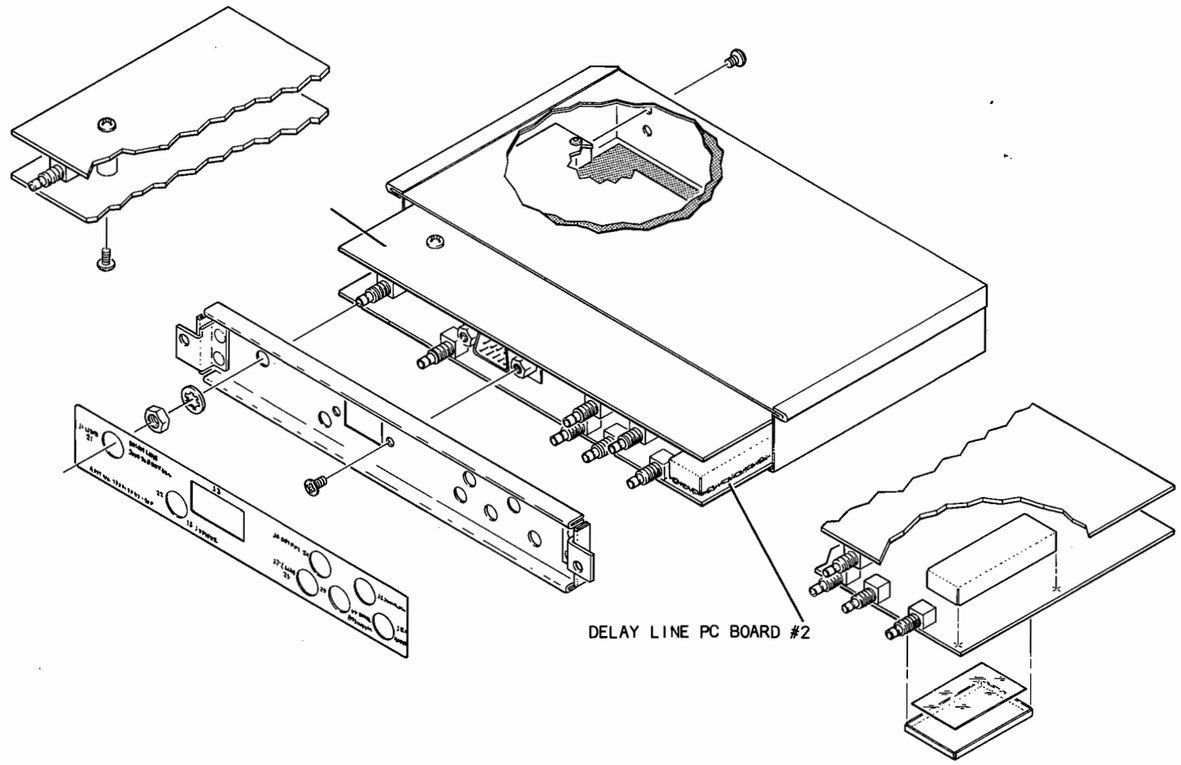
MECH ASSY

1. THE REF DES SERIES FOR THE HIGH/LOW PASS FILTER MECH ASSY IS 600 (I.E., J1 IS J601).
2. DATA PART NO. 7005-5040-700.
3. REF CIRCUIT SCHEMATIC 0000-5010-700.

PC BOARD

1. THE REF DES SERIES FOR THE HIGH/LOW PASS PC BOARD IS 700 (I.E., R1 IS R701).
2. DATA PART NO. 7010-5030-700.
3. REF CIRCUIT SCHEMATIC 0000-5010-700.

Figure 6-16 High/Low Pass Filter Module



NOTES:

MECH ASSY

1. THE REF DES SERIES FOR THE DELAY LINE MECH ASSY IS 3000 (I.E., J1 IS J3001).
2. DATA PART NO. 7005-5042-500.
3. REF CIRCUIT SCHEMATIC 0000-5012-400 AND 0000-5012-600.

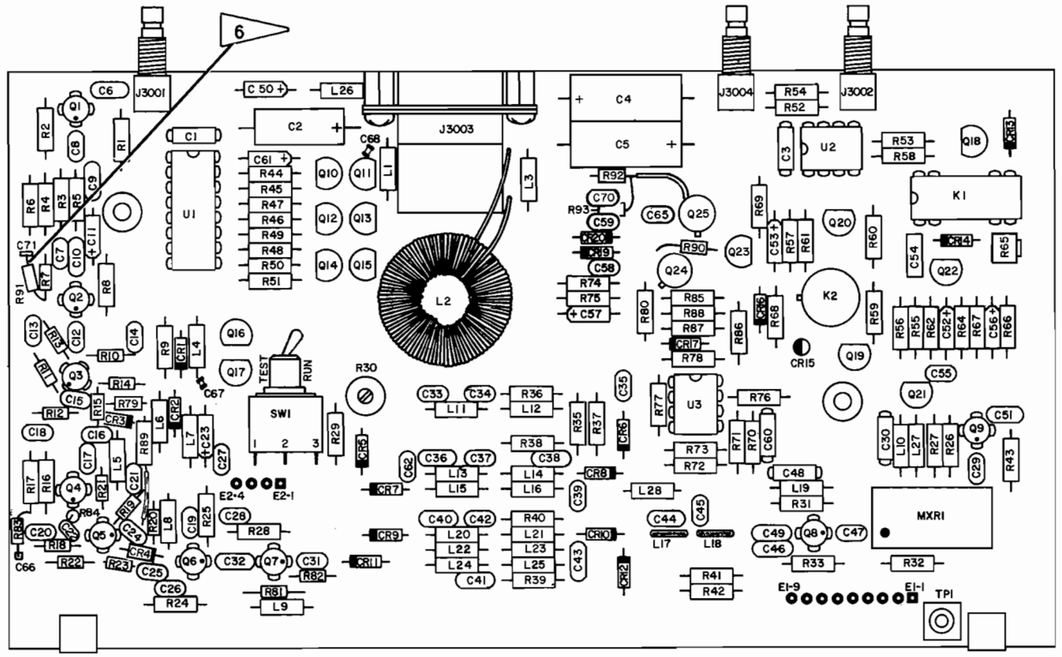
DELAY LINE PC BOARD #1

1. THE REF DES SERIES FOR THE DELAY LINE PC BOARD #1 IS 2500 (I.E., R1 IS R2501).
2. DATA PART NO. 7010-5032-400-H9.
3. REF CIRCUIT SCHEMATIC 0000-5012-400.
4. TRANSISTOR COLLECTOR LEAD INDICATED BY DOT ON Q1 THRU Q9.
5. C70 IS SAT (SELECTED AT TEST).
6. THRU SER. NO. 1953, C71, R91 NOT USED.

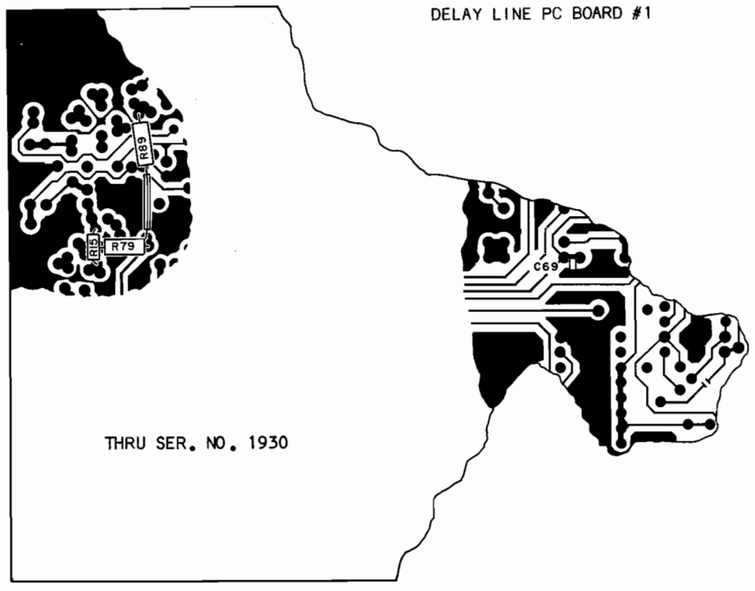
DELAY LINE PC BOARD #2

1. THE REF DES SERIES FOR THE DELAY LINE PC BOARD #2 IS 2600 (I.E., R1 IS R2601).
2. DATA PART NO. 7010-5032-600.
3. REF CIRCUIT SCHEMATIC 0000-5012-400-G1.
4. TRANSISTOR COLLECTOR LEAD INDICATED BY DOT ON Q1 THRU Q4.
5. THRU SER. NO. 1930, CR19, R52 NOT USED.
6. SER. NO. 2774 AND ON R51 NOT USED.

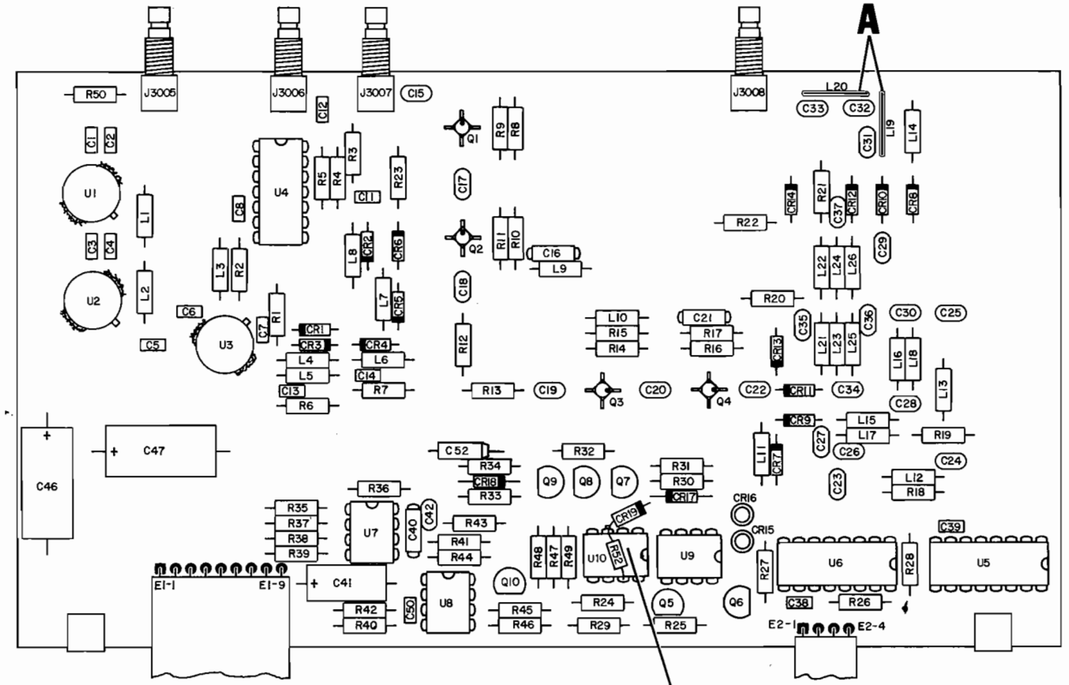
Figure 6-17 Delay Line Module (Sheet 1 of 2)



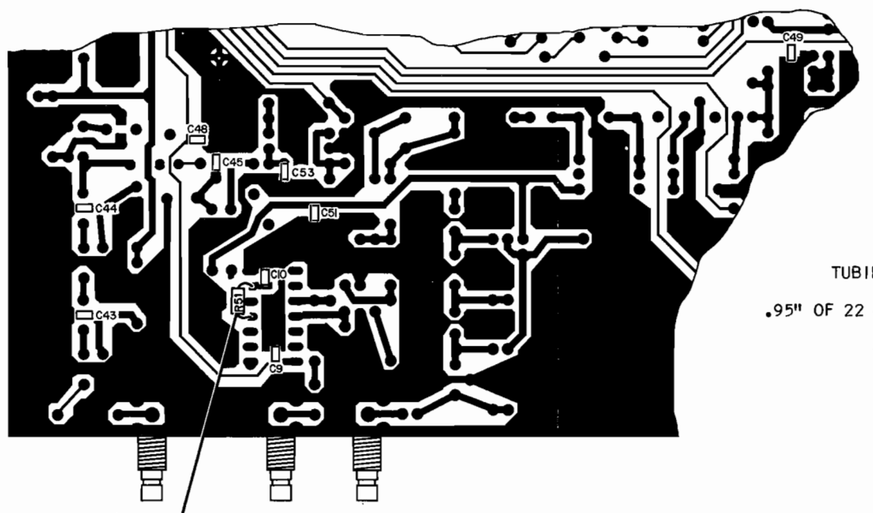
DELAY LINE PC BOARD #1

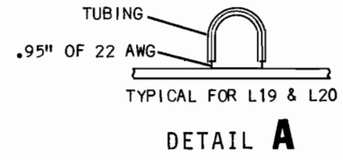


THRU SER. NO. 1930



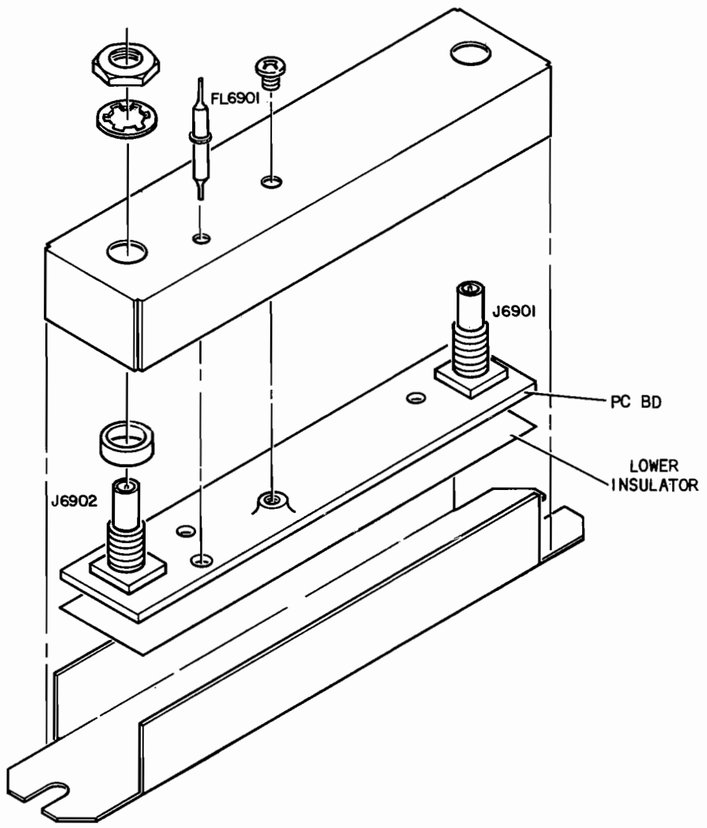
DELAY LINE PC BD #2

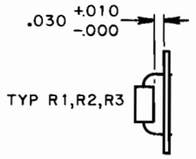




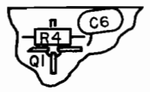
DETAIL **A**

Figure 6-17 Delay Line Module
(Sheet 2 of 2)



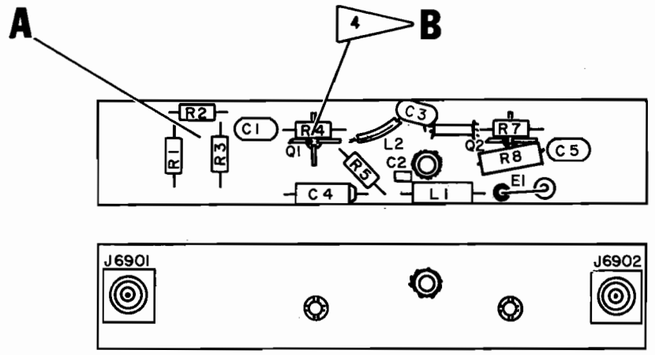


DETAIL **A**



THRU SER. NO. 2204

DETAIL **B**



NOTES:

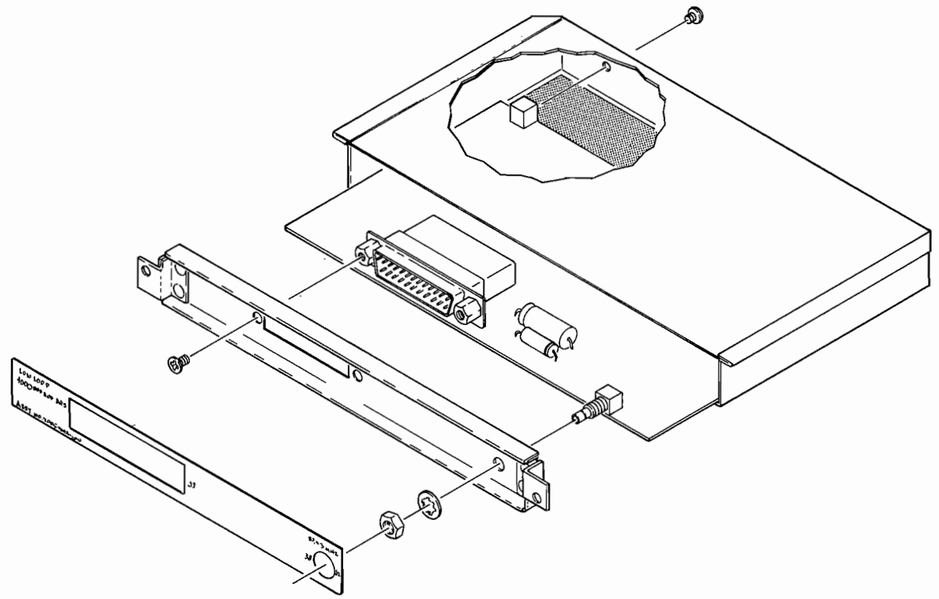
MECH ASSY

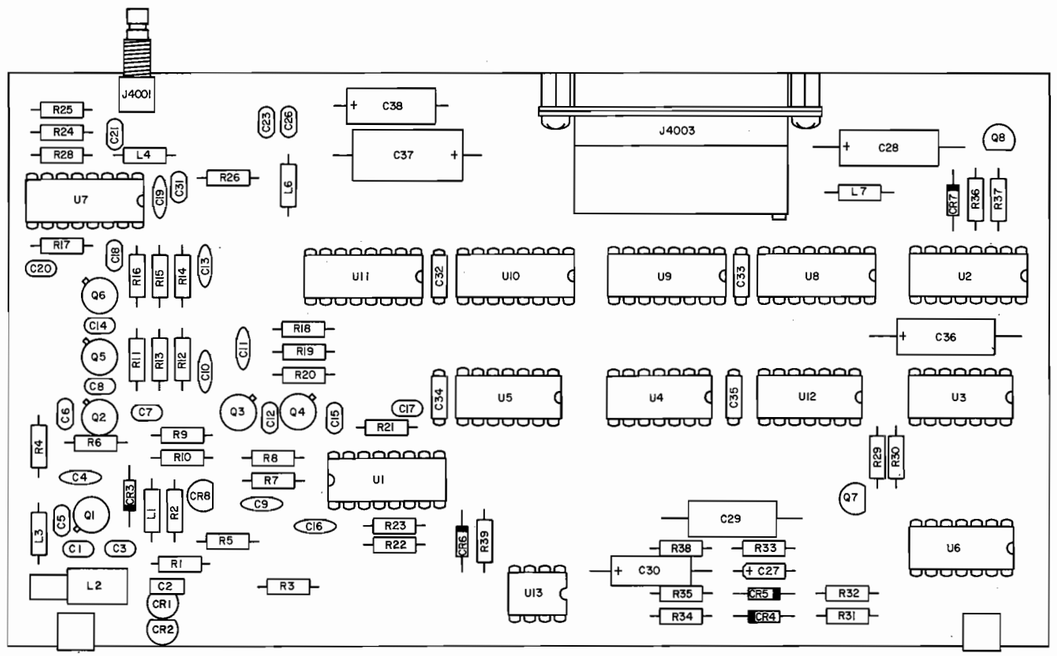
1. THE REF DES SERIES FOR BUFFER AMP "A" MECH ASSY IS 6900A. THE REF DES SERIES FOR BUFFER AMP "B" MECH ASSY IS 6900B (I.E., J1 IS J6901A FOR BUFFER AMP "A" AND J6901B FOR BUFFER AMP "B").
2. DATA PART NO. FOR BOTH BUFFER AMP "A" AND BUFFER AMP "B" IS 7005-5046-801.
3. REF CIRCUIT SCHEMATIC: 0000-5016-801.

PC BOARD

1. THE REF DES SERIES FOR BUFFER AMP "A" PC BOARD ASSY IS 6800A. THE REF DES SERIES FOR BUFFER AMP "B" IS 6800B (I.E., R1 IS R6801A ON BUFFER AMP "A" AND R6801B ON BUFFER AMP "B".
2. DATA PART NO. FOR BOTH BUFFER AMP "A" AND BUFFER AMP "B" PC BOARDS ARE 7010-5036-801.
3. REF CIRCUIT SCHEMATIC: 0000-5016-801.
4. USE C6806 THRU SER. NO. 2204 (SEE DETAIL B).

Figure 6-18 Buffer Amp Module (Typical for Buffer Amp A and B)





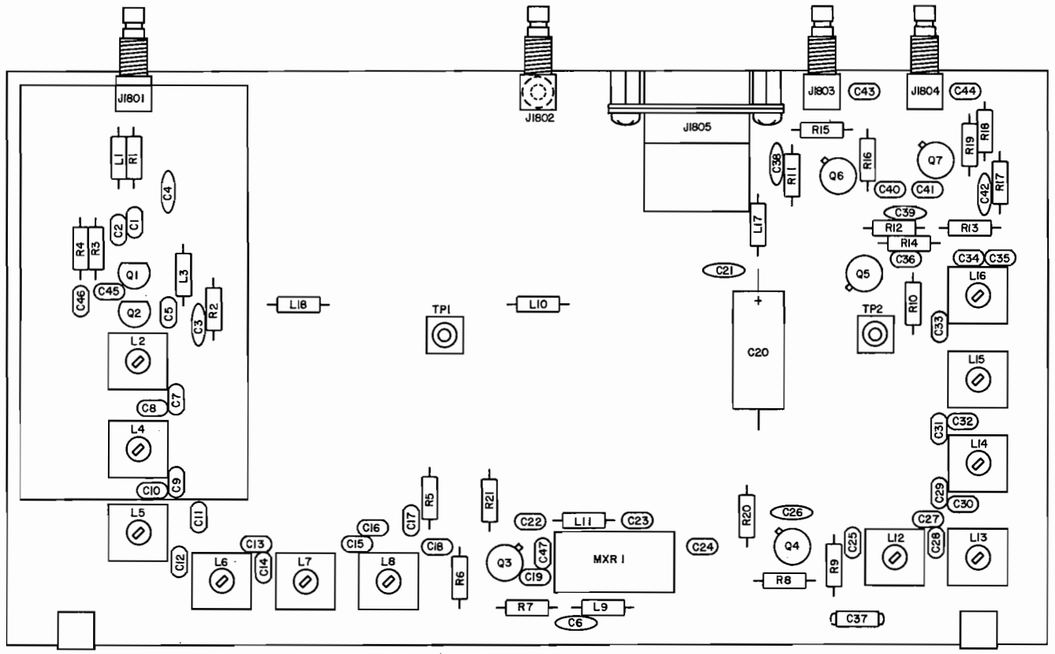
MECH ASSY

1. THE REF DES SERIES FOR LOW LOOP MECH ASSY IS 4000 (I.E., J4001).
2. DATA PART NO. 7005-5043-100.
3. REF CIRCUIT SCHEMATIC 0000-5013-100.
4. THIS DRAWING TAKES PRECEDENCE OVER ANY EXISTING LABELS INSTALLED IN THE FM/AM-1500.

PC BOARD

1. THE REF DES SERIES FOR LOW LOOP PC BOARD ASSY IS 3100 (I.E., R1 IS R3101).
2. DATA PART NO. 7010-5033-100.
3. REF CIRCUIT SCHEMATIC 0000-5013-100.

Figure 6-19 Low Loop Module



NOTES:

MECH ASSY

1. THE REF DES SERIES FOR LOW LOOP MIXER MECH ASSY IS 1800 (I.E., J1 IS J1801).
2. DATA PART NO. 7005-5041-900.
3. REF CIRCUIT SCHEMATIC 0000-5011-900.

PC BOARD

1. THE REF DES SERIES FOR LOW LOOP MIXER PC BOARD ASSY IS 1900 (I.E., R1 IS R1901).
2. DATA PART NO. 7010-5031-900.
3. REF CIRCUIT SCHEMATIC 0000-5011-900.

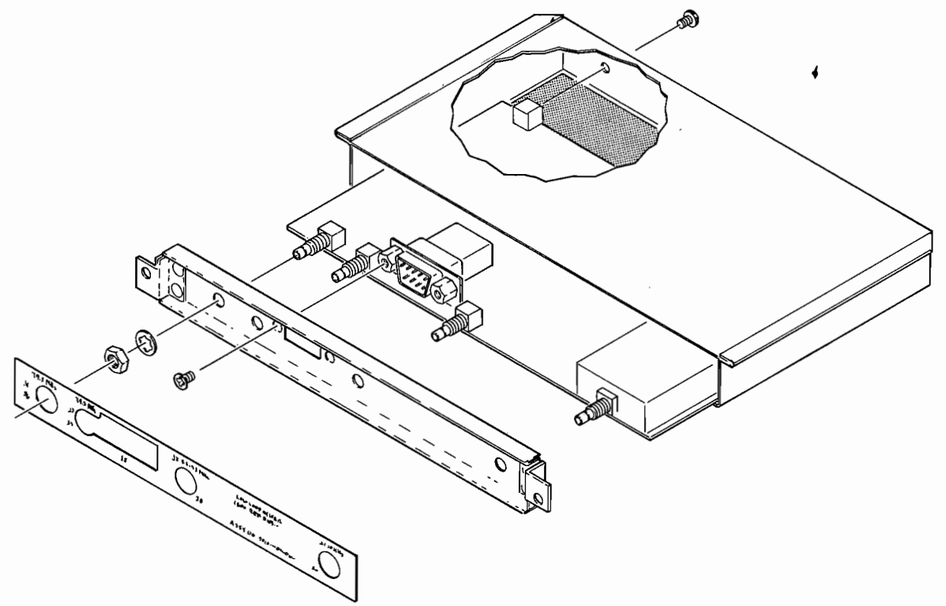
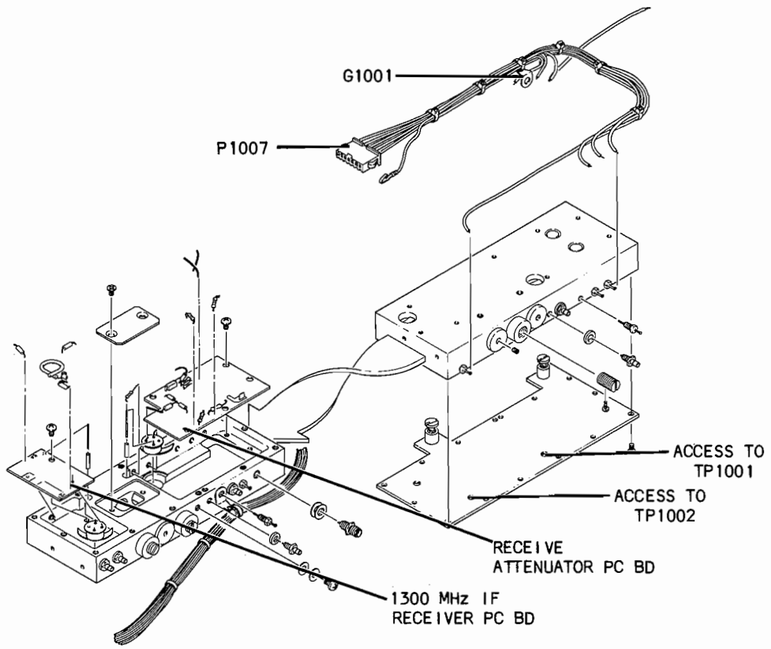
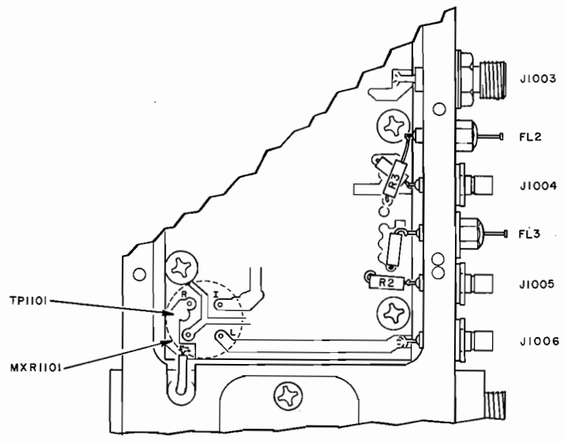


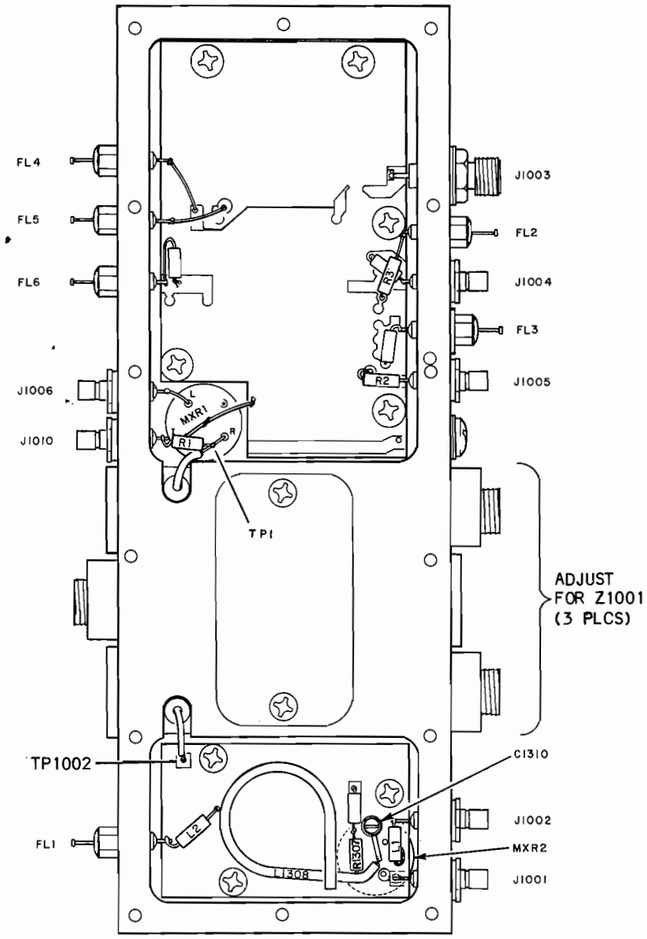
Figure 6-20 Low Loop Mixer Module



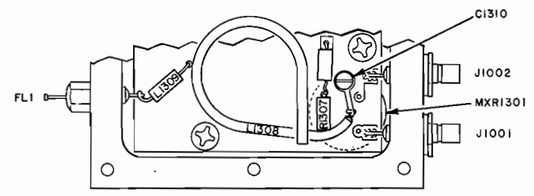
SER. NO. 1005 THRU 1406



SER NO. 1005 THRU 1234



SER. NO. 1235 THRU 1406



SER. NO. 1005 THRU 1234

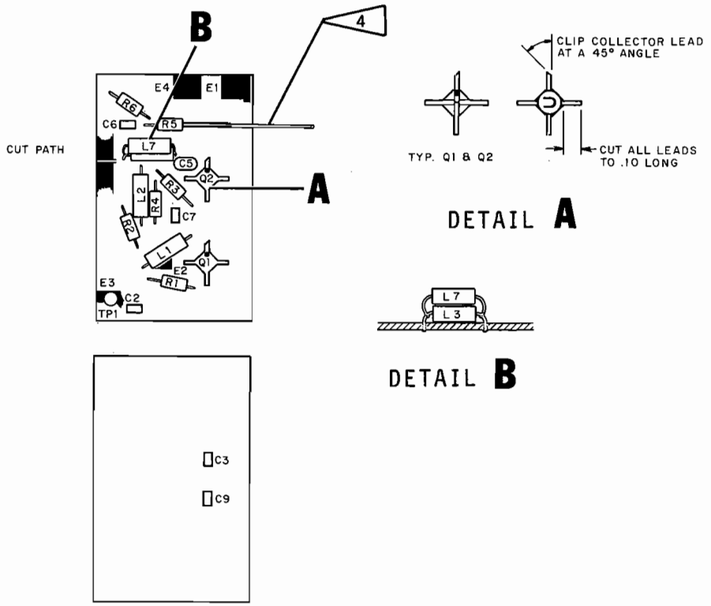
NOTES:

MECH ASSY

1. THE REF DES SERIES FOR 1300 MHz IF RECEIVER MECH ASSY IS 1000 (I.E., J1 IS J1001.)
2. DATA PART NO. 7005-5041-300.
3. REF CIRCUIT SCHEMATIC 0000-5011-300.

WIRE RUNNING LIST				
FROM	TO	COLOR	AWG	LENGTH
P1007-1	FL1002	WHT	26	6.00"
P1007-2	FL1003	BLU	26	5.50"
P1007-3	FL1004	YEL	26	10.50"
P1007-4	FL1005	GRN	26	10.00"
P1007-5	FL1006	VIO	26	10.50"
P1007-6	G1001	BLK	26	5.5"
P1007-7	FL1001	RED	26	15.00"
P1007-8	NC	---	--	----
FL7101	FL1002	WHT	26	8.00"

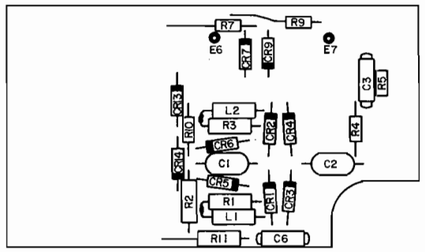
Figure 6-21 1300 MHz IF Receiver Module (Sheet 1 of 4)



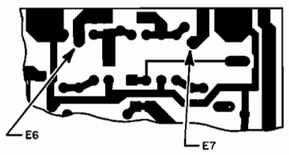
DETAIL **A**

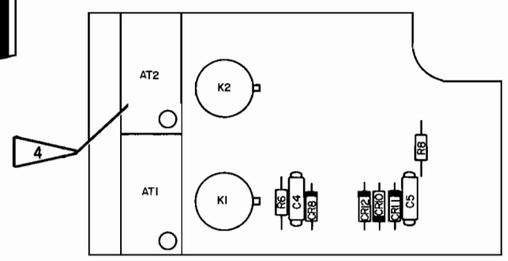
DETAIL **B**

SER. NO. 1005 THRU 1406
1300 MHz IF RECEIVER PC BD



TOP VIEW





BOTTOM VIEW

SER NO. 1005 THRU 1406
RECEIVE ATTENUATOR PC BD

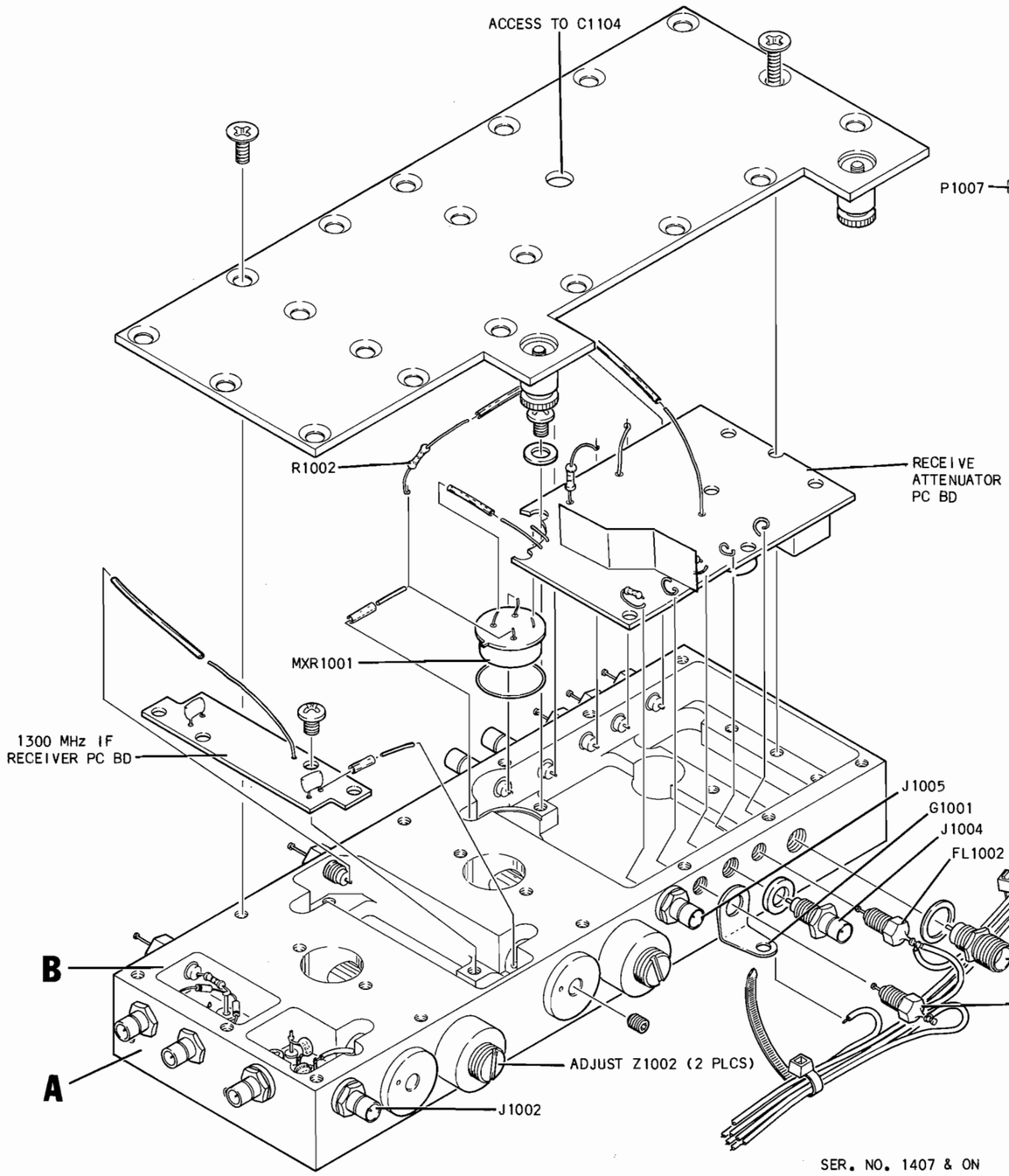
1300 MHz IF RECEIVER PC BOARD

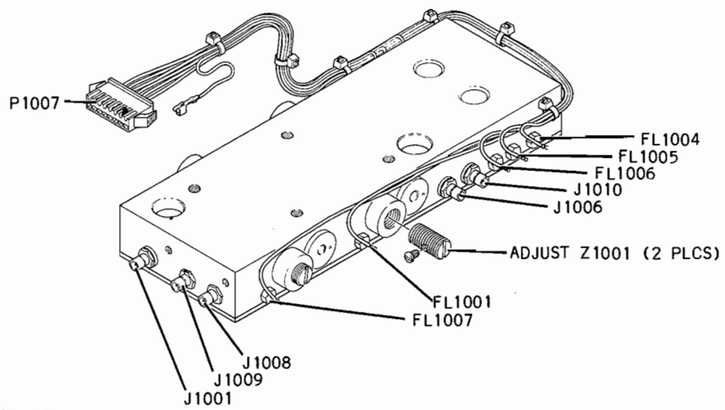
1. THE REF DES SERIES FOR 1300 MHz IF RECEIVER PC BOARD ASSY IS 1300 (I.E., R1 IS R1301).
2. DATA PART NO. 7010-5031-300.
3. REF CIRCUIT SCHEMATIC 0000-5011-300.
4. LEAD OF R5 TO BE CONNECTED AT NEXT ASSY.

RECEIVE ATTENUATOR PC BOARD

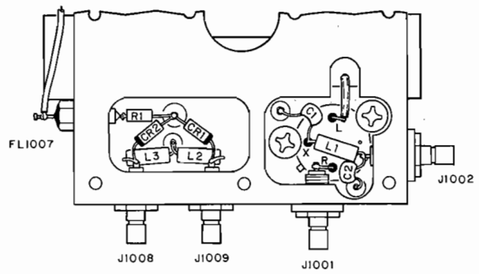
1. THE REF DES SERIES FOR RECEIVE ATTENUATOR PC BOARD IS 1100 (I.E., R1 IS R1101).
2. DATA PART NO. 7010-5031-100.
3. REF CIRCUIT SCHEMATIC 0000-5011-300.
4. BLUE DOT UNDER AT1 AND AT2 REPRESENTS PIN #1.

Figure 6-21 1300 MHz IF Receiver Module (Sheet 2 of 4)





DETAIL **A**



DETAIL **B**

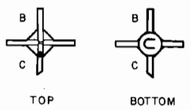
NOTES:

MECH ASSY

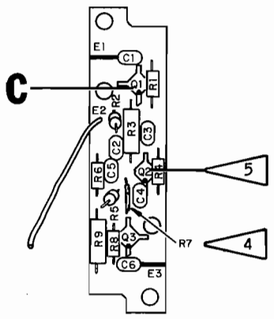
1. THE REF DES SERIES FOR 1300 MHz IF RECEIVER MECH ASSY IS 1000 (I.E., J1 IS J1001).
2. DATA PART NO. 7005-5041-400.
3. REF CIRCUIT SCHEMATIC 0000-5011-400.

WIRE RUNNING LIST				
FROM	TO	COLOR	AWG	LENGTH
P1007-1	FL1002	WHT	26	6.00"
P1007-2	FL1003	BLU	26	5.50"
P1007-3	FL1004	YEL	26	10.50"
P1007-4	FL1005	GRN	26	10.00"
P1007-5	FL1006	VIO	26	10.50"
P1007-6	G1001	BLK	26	5.50"
P1007-7	FL1001	RED	26	15.00"
P1007-8	N/C	---	--	------
FL1007	FL1002	WHT	26	8.00"

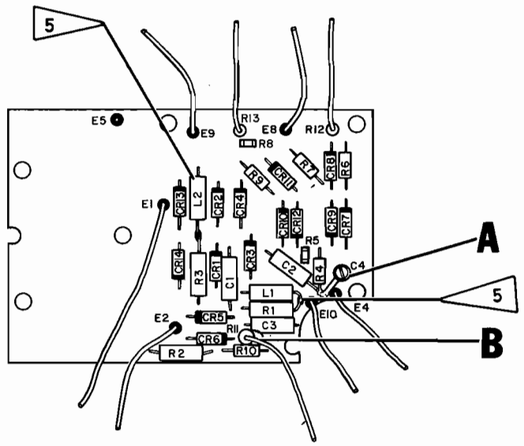
Figure 6-21 1300 MHz IF Receiver Module (Sheet 3 of 4)

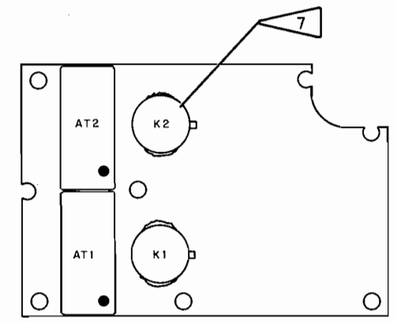


DETAIL **C**

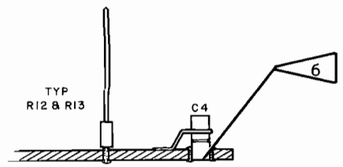


SER. NO. 1407 AND ON
1300 MHz IF RECEIVER PC BD

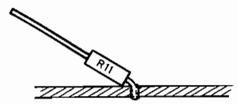




SER NO. 1407 AND ON
RECEIVE ATTENUATOR PC BD



DETAIL **A**



DETAIL **B**

NOTES:

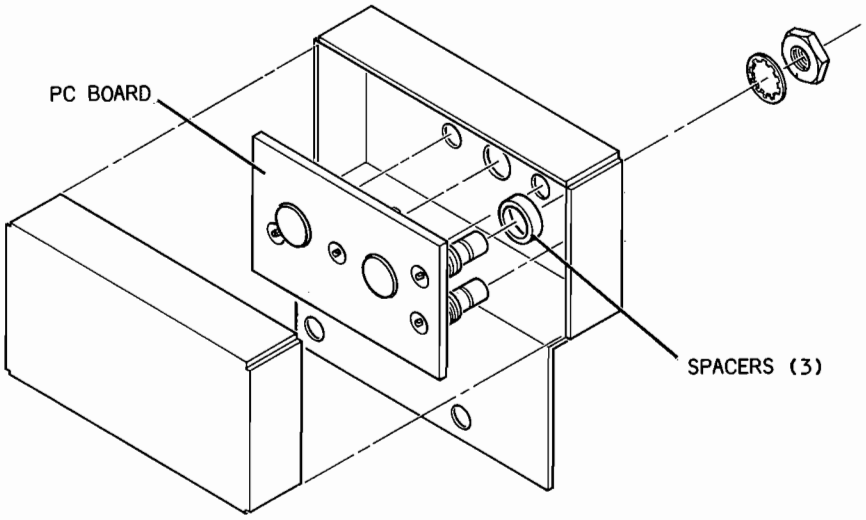
1300 MHZ IF RECEIVER PC BOARD

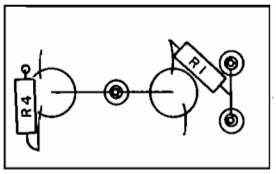
1. THE REF DES SERIES FOR 1300 MHz IF RECEIVER PC BOARD ASSY IS 1300 (I.E., R1 IS R1301).
2. DATA PART NO. 7010-5031-400.
3. REF CIRCUIT SCHEMATIC: 0000-5011-400.
4. R7 IS S.A.T.: NOMINAL VALUE 0 OHMS RANGE 0-100 OHMS
   IF NOMINAL VALUE IS REQUIRED USED 26 AWG BUS WIRE (SELECTED) AS JUMPER.
5. CUT LEAD OF Q2 FLUSH PRIOR TO INSTALLATION.

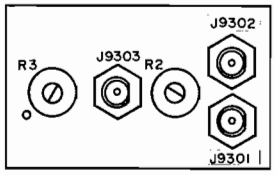
RECEIVE ATTENUATOR PC BOARD

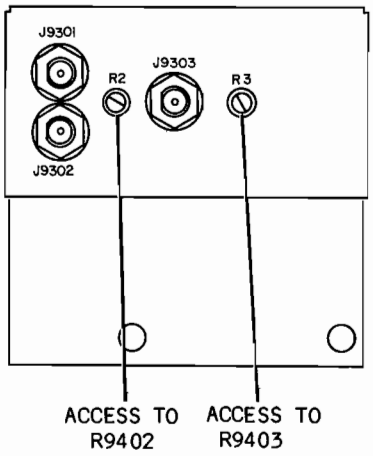
1. THE REF DES SERIES FOR RECEIVE ATTENUATOR PC BOARD ASSY IS 1100 (I.E., R1 IS R1101).
2. DATA PART NO. 7010-5031-200.
3. REF CIRCUIT SCHEMATIC 0000-5011-400.
4. R11, R12 AND R13 ARE SOLDERED AS CLOSE AS POSSIBLE TO PC BD (SHORT LEAD LENGTH).
5. MID-AIR CONNECTION OF L1 TO R1; ALSO L2 TO R3. MID-AIR CONNECTIONS MUST BE .10" ABOVE PC BOARD.
6. C4 IS SOLDERED FLUSH WITH BOTTOM OF PC BD.
7. K1 AND K2 ARE SOLDERED TO GROUND PLANE (2 PLCS EACH CAN).

Figure 6-21 1300 MHz IF Receiver Module (Sheet 4 of 4)









NOTES:

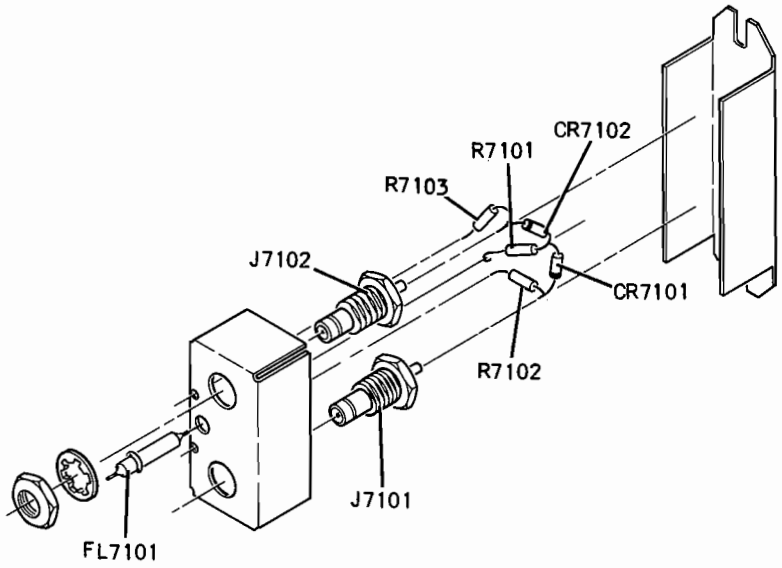
MECH ASSY

1. THE REF DES SERIES FOR MIXER NULL MECH ASSY IS 9300 (I.E., J1 IS J9301).
2. DATA PART NO. 7005-5047-600.
3. REF CIRCUIT SCHEMATIC 0000-5017-600.

PC BOARD

1. THE REF DES SERIES FOR MIXER NULL PC BOARD ASSY IS 9400 (I.E., R1 IS R9401).
2. DATA PART NO. 7010-5037-600.
3. REF CIRCUIT SCHEMATIC 0000-5017-600.

Figure 6-22 Mixer Null Module (Effective Ser. No. 1235 and On)



NOTES:

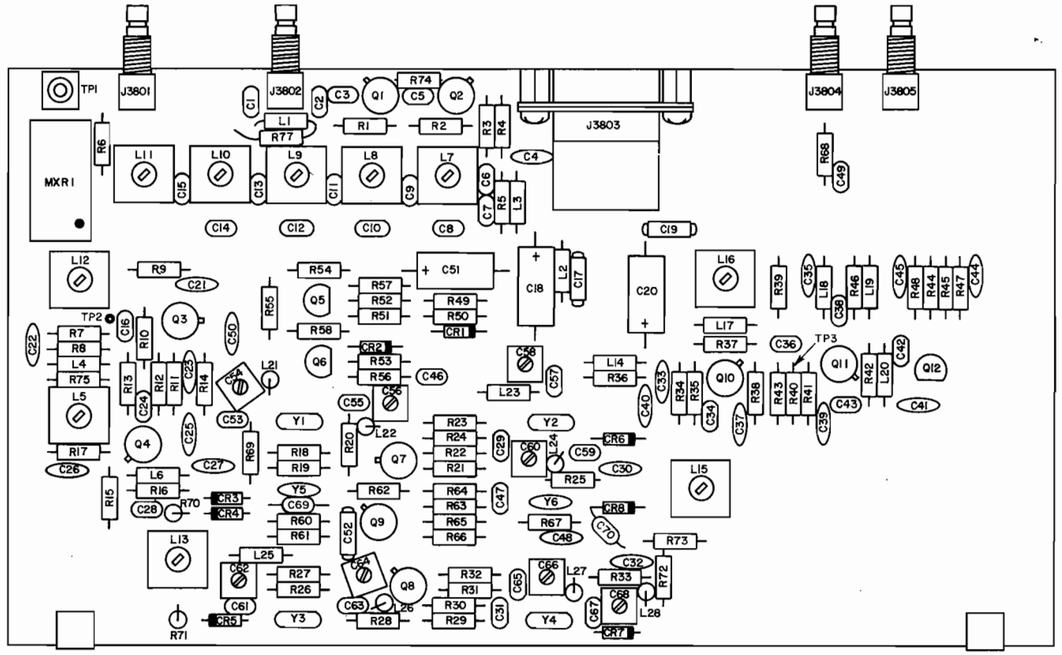
MECH ASSY

1. THE REF DES SERIES FOR DIODE SWITCH MECH ASSY IS 7100 (I.E., J1 IS J701).

2. DATA PART NO. 7005-5044-800.

3. REF CIRCUIT SCHEMATIC 0000-5014-800.

Figure 6-23 Diode Switch (Effective Ser. No. 1005 thru 1406)



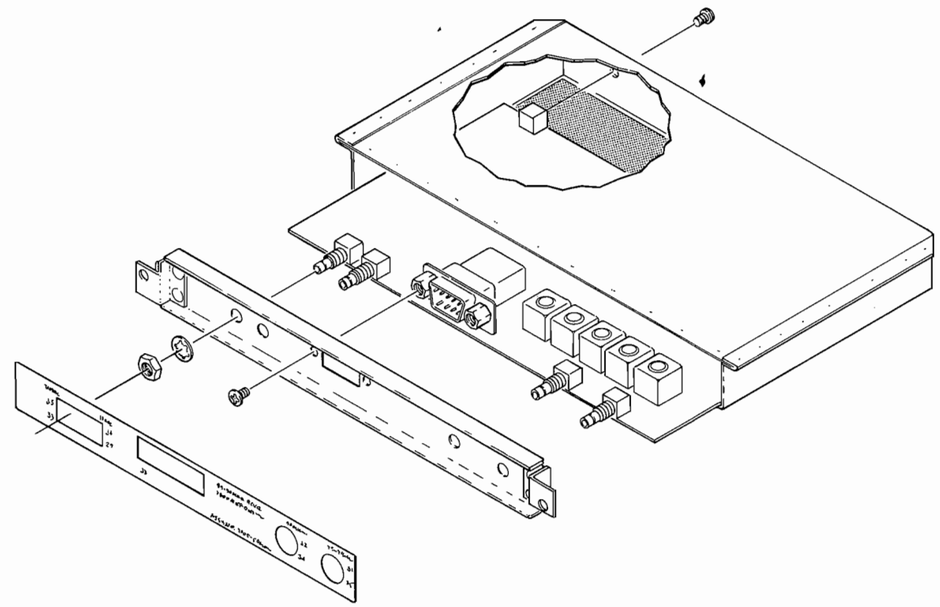
NOTES:

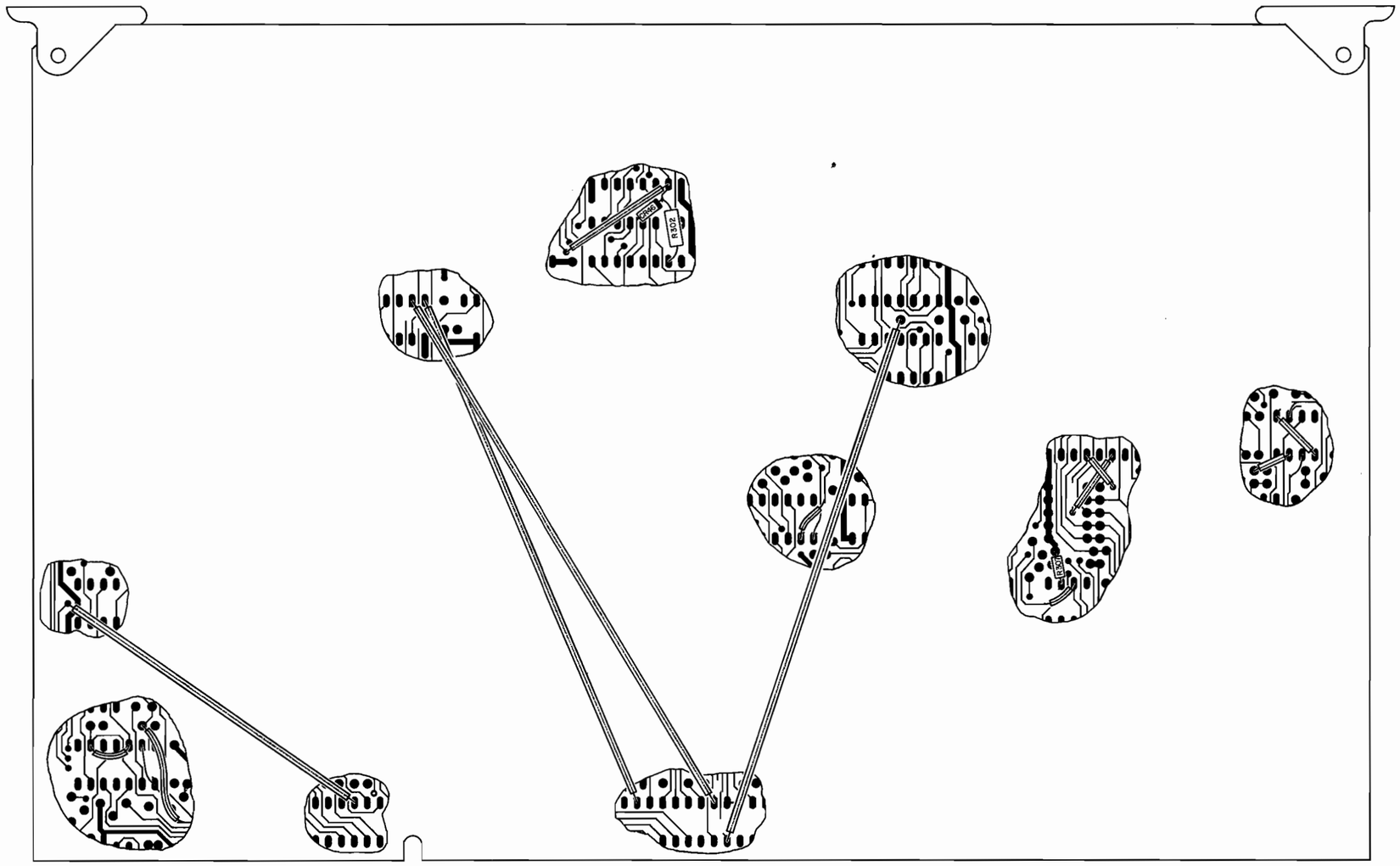
MECH ASSY

1. THE REF DES SERIES FOR 89-90 MHz RECEIVER MECH ASSY IS 3800 (I.E., J1 IS J3801).
2. DATA PART NO. 7005-5042-900.
3. REF CIRCUIT SCHEMATIC 0000-5012-900.

PC BOARD

1. THE REF DES SERIES FOR 89-90 MHz RECEIVER PC BOARD ASSY IS 2900 (I.E., R1 IS R2901).
2. DATA PART NO. 7010-5032-900.
3. REF CIRCUIT SCHEMATIC 0000-5012-900.

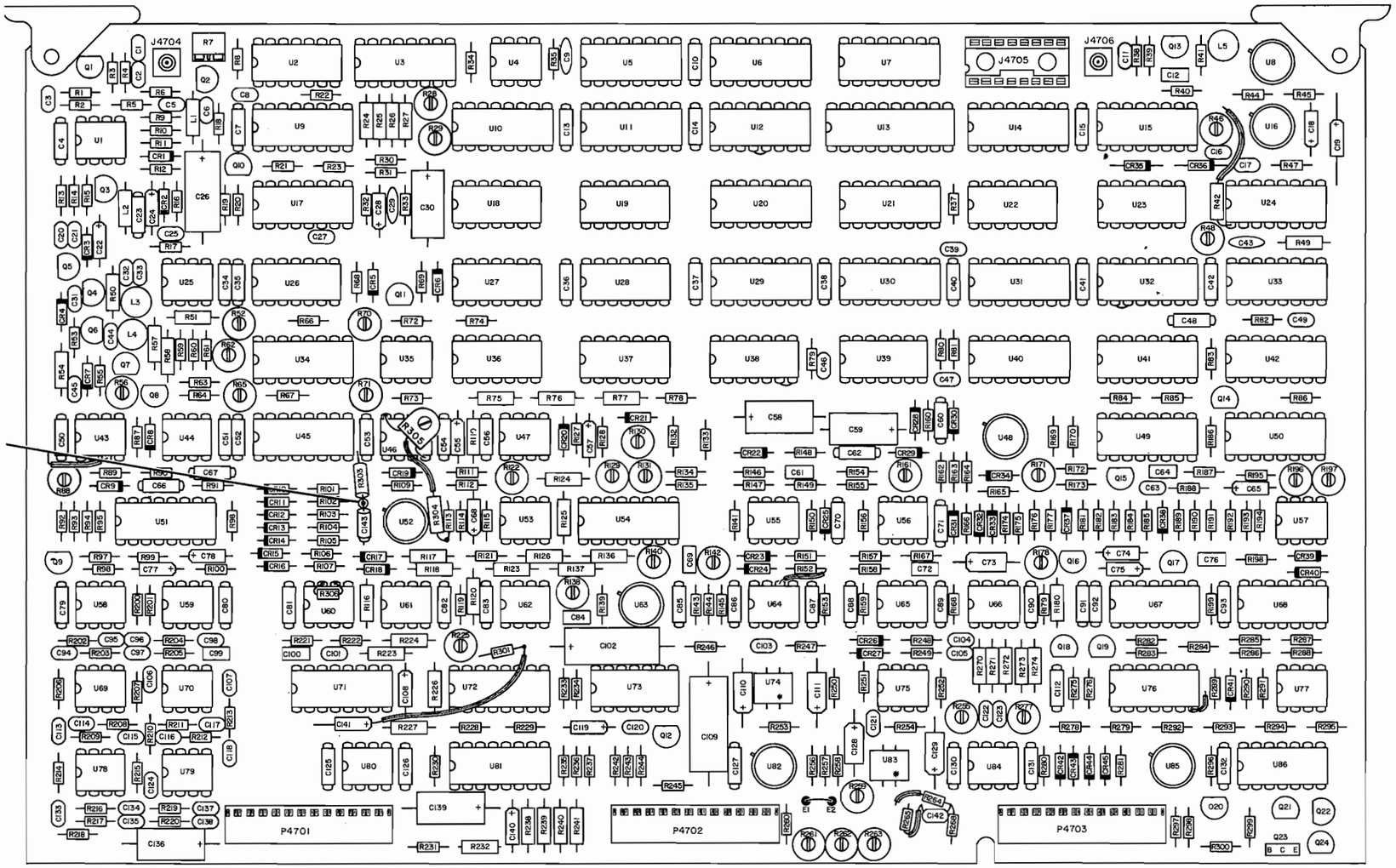




DETAIL **A**

BOTTOM VIEW

SER. NO. 1005 THROUGH 1425



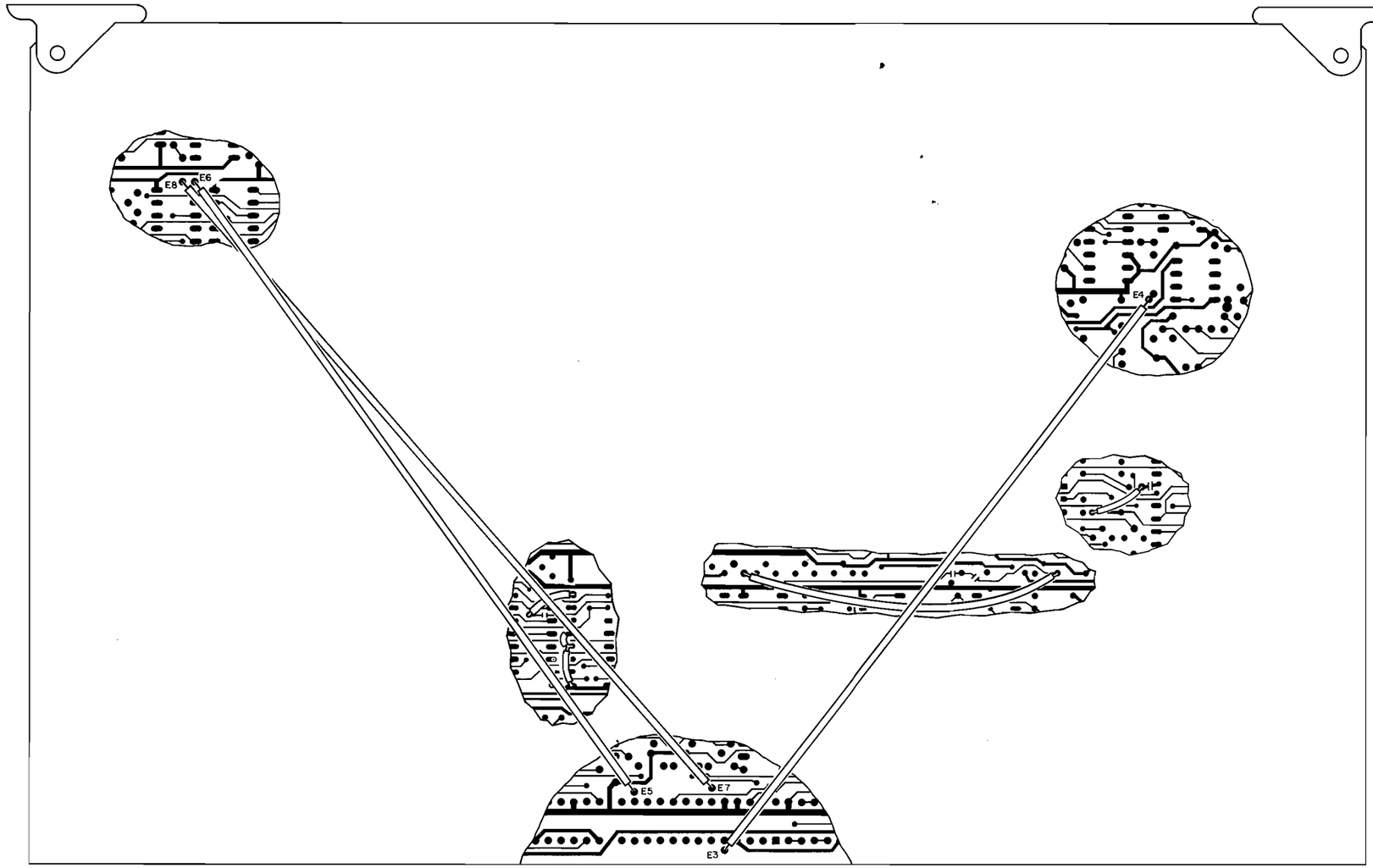
TOP VIEW

SER. NO. 1005 THRU 1425

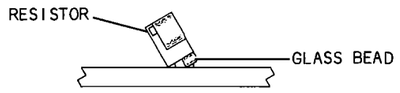
NOTES (SER. NO. 1005 THRU 1425):

1. REF CIRCUIT SCHEMATIC: 0000-5014-300.
2. THE REF DES SERIES FOR DEMOD AUDIO PC BOARD ASSY IS 4700, 4800, 4900 AND 5000 (I.E., R1 IS R4701, R101 IS R4801, R201 IS R4901, R301 IS R5001).
3. DATA PART NO. 7010-5014-700.
4. USE 26 AWG BUS WIRE WITH 26 AWG SLEEVING AS SHOWN: 3 PLACES TOPSIDE, 13 PLACES BOTTOMSIDE.
5. SLEEVE LEADS ON R42, R264 AND R265 WITH TUBING AS SHOWN.
6. POSITION U74 AND U83 SO THAT THE DOT ON THE CASE IS IN THE SAME PLACE AS THE LEAD MARKED WITH AN ASTERISK (*) ON THIS DRAWING.
7. SLEEVE LEADS ON C141 AND R304 WITH TUBING AS SHOWN.

Figure 6-25 Demod Audio PC Board (Sheet 1 of 3)

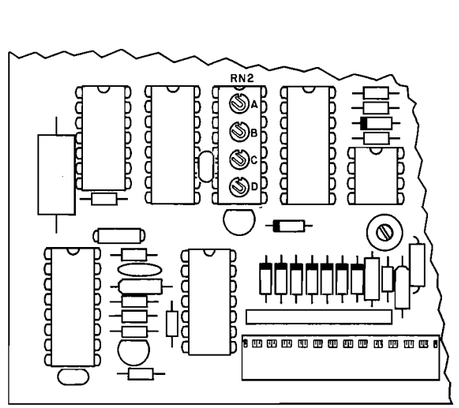


4 BOTTOM VIEW
SER. NO. 1426 THRU 1505



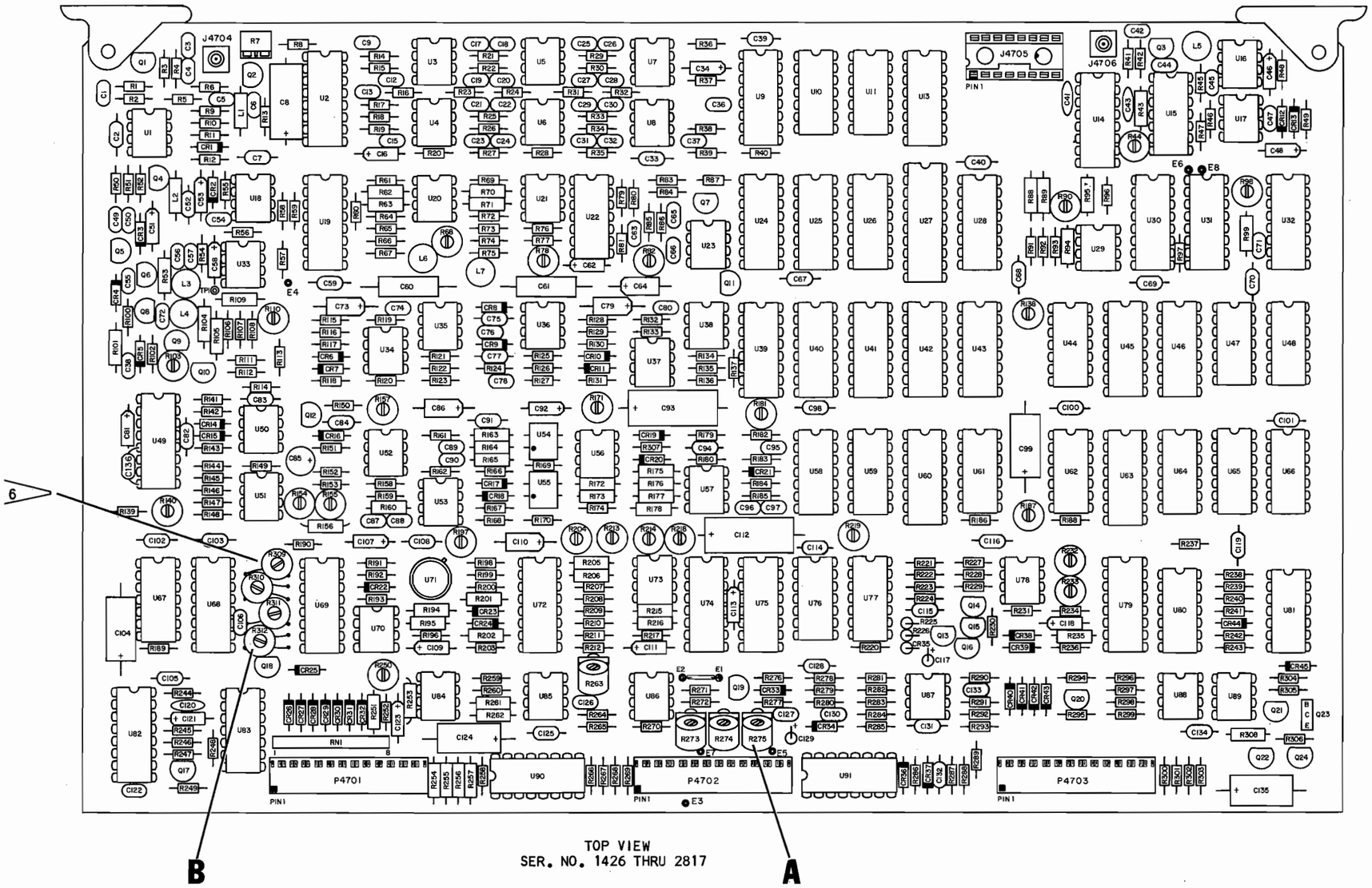
TYPICAL FOR R263, R273, R274 AND R275.

DETAIL **A**



SER. NO. 1426 THRU 1505

DETAIL **B**



TOP VIEW
SER. NO. 1426 THRU 2817

NOTES:

1. REF CIRCUIT SCHEMATIC: 0000-5017-300

2. REF DES SERIES ARE 4700, 4800, 4900 AND 5000 (I.E., R1 IS 4701, R100 IS R4800, R200 IS R4900, R300 IS R5000

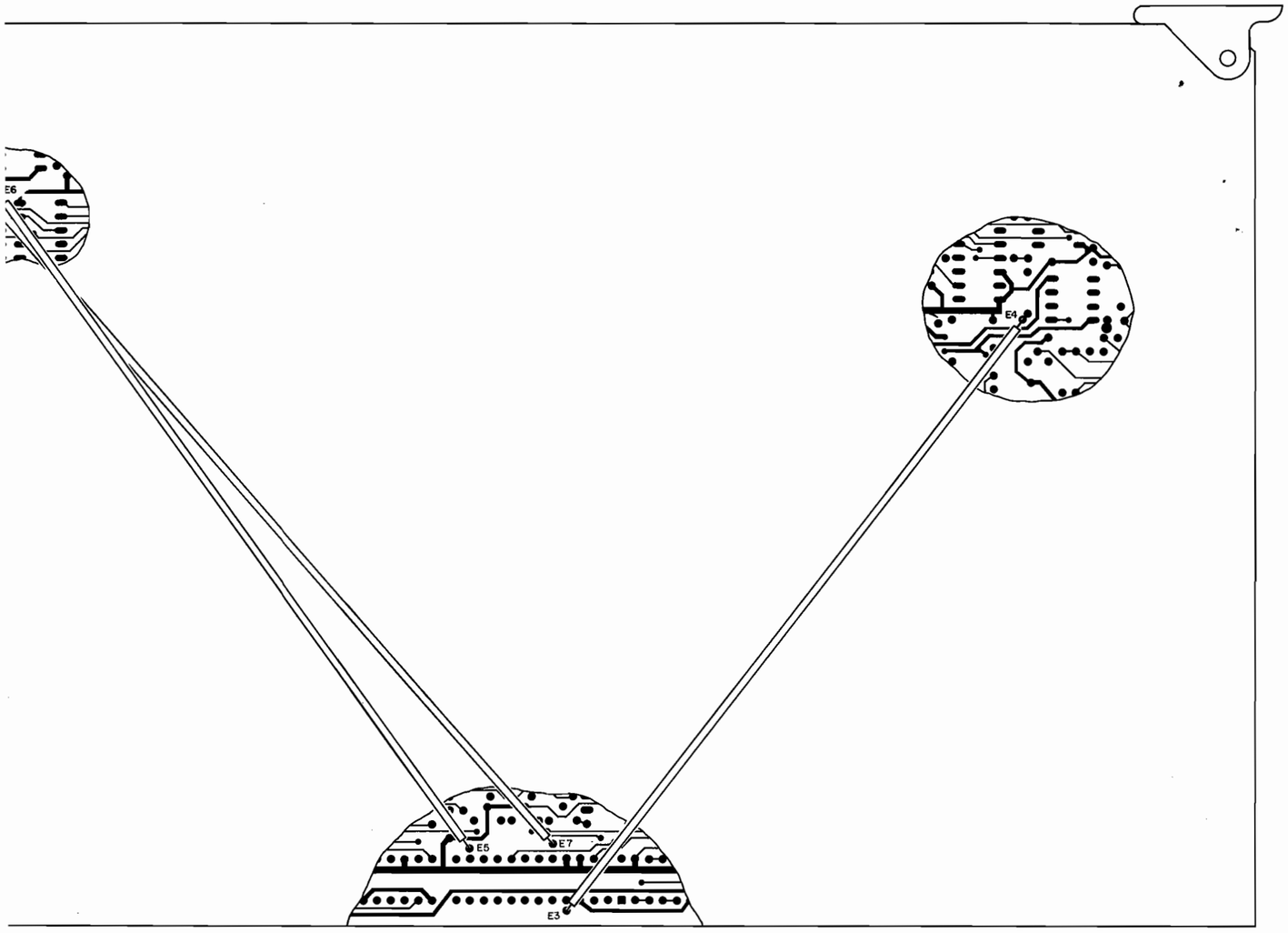
3. DATA PART NO. 7010-5037-300, EFFECTIVE SER. NO. 1426 THRU SER. NO. 2817

4. SER. NO. 1426 THRU 1505: USE 30 AWG WIRE WITH 30 AWG SLEEVING AS SHOWN (8 PLCS).

5. POSITION U54 AND U55 SO DOT ON CASE IS IN SAME PLACE AS THE LEAD MARKED WITH A DOT.

6. INSTALL WITH MYLAR TAPE® UNDER R309 R312 TO PREVENT LEADS FROM CONTACTING PATHWORK (FOR REV "B" BOARDS).

Figure 6-25 Demod Audio PC Board (Sheet 2 of 3)

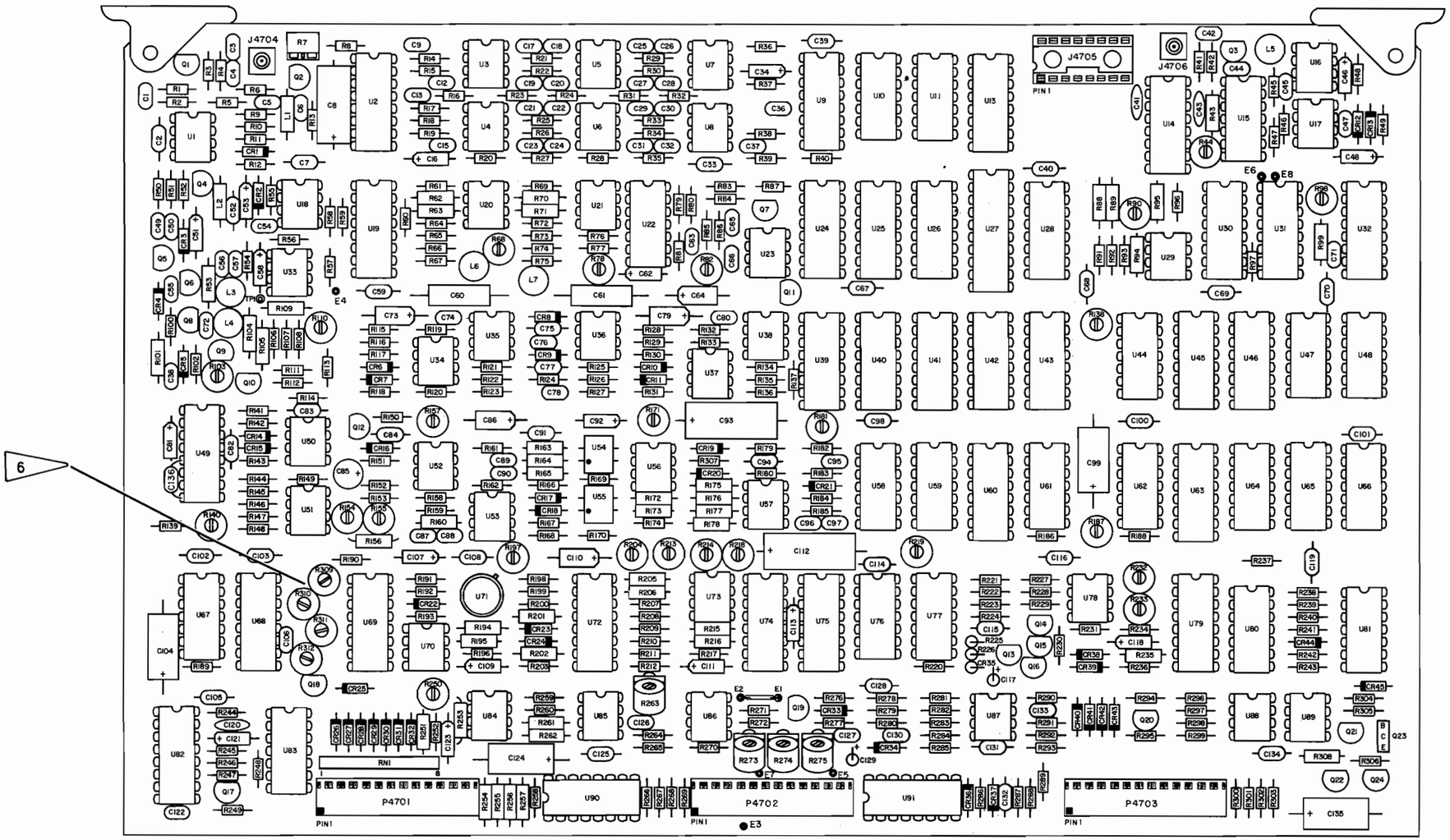


BOTTOM VIEW
SER. NO. 1506 AND ON

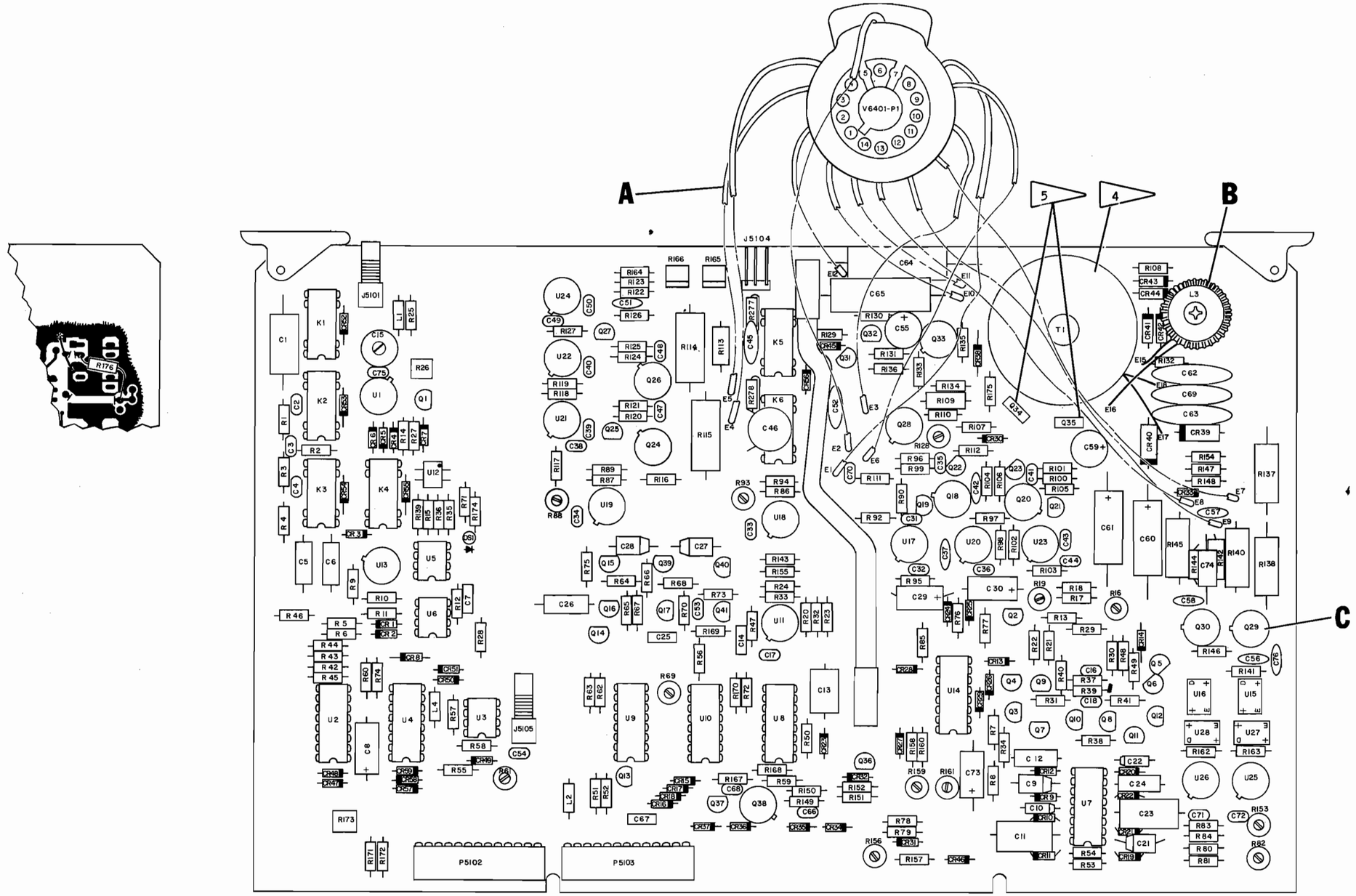
NOTES:

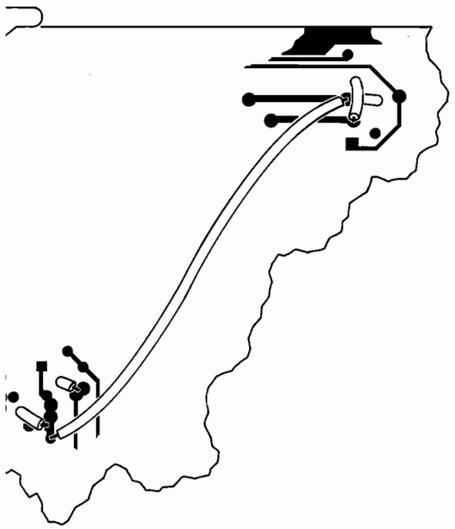
1. REF CIRCUIT SCHEMATIC: 0000-5017-900.
2. REF DES SERIES ARE 4700, 4800, 4900 AND 5000 (I.E., R1 IS R4701, R100 IS R4800, R200 IS R4900 AND R300 IS 85000).
3. DATA PART NO. 7010-5037-300, EFFECTIVE SER. NO. 2818 AND ON.
4. NOT USED.
5. POSITION U54 AND U55 SO DOT ON CASE IS IN THE SAME PLACE AS THE LEAD MARKED WITH A DOT.
6. INSTALL WITH MYLAR TAPE UNDER R309 THRU R312 TO PREVENT LEADS FROM CONTACTING PATHWORK (FOR REV "B" BOARDS).

Figure 6-25 Demod Audio PC Board (Sheet 3 of 3)



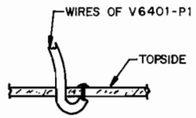
TOP VIEW
SER. NO. 2818 AND ON


A
B
C
5
4
V6401-P1
J5104
J5101
J5105
P5102
P5103
TOP VIEW
SER. NC

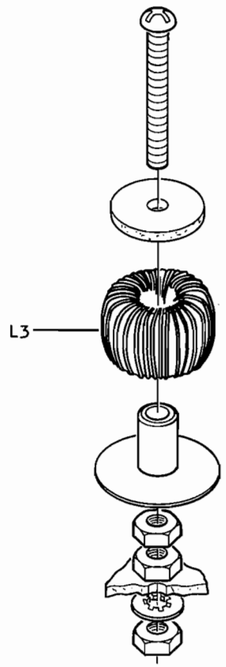


BOTTOM

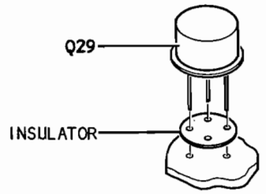
2002 THRU 2099



DETAIL **A**



DETAIL **B**



(TYPICAL FOR Q18, Q20, Q24, Q26, Q28, Q29, Q30 and Q38)

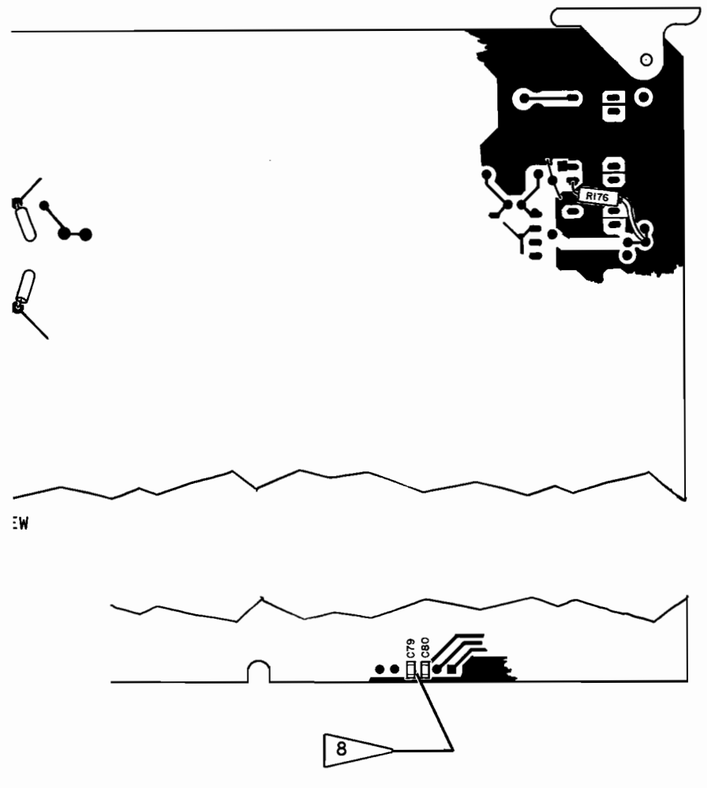
DETAIL **C**

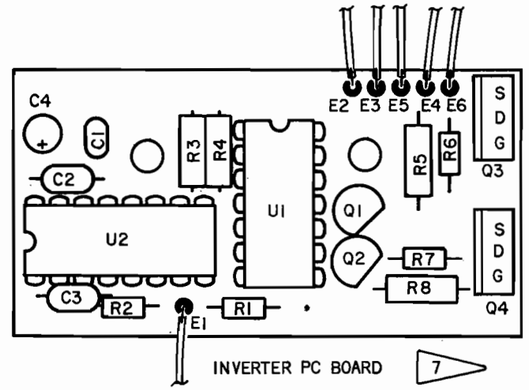
NOTES:

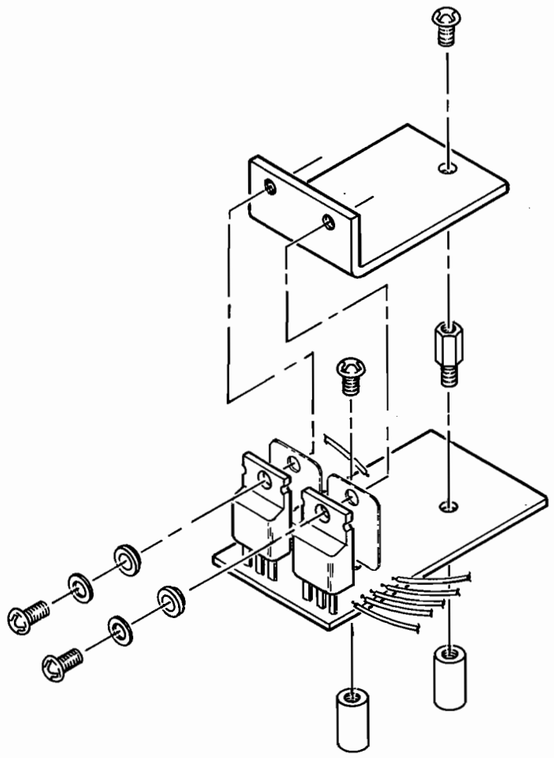
1. THE REF DES SERIES FOR OSCILLOSCOPE CONTROL AND DEFL. PC BD ASSY IS 5100 AND 9500 (I.E., R1 IS R5101 AND R101 IS R9501).
2. DATA PART NO. 7010-5035-100.
3. REF CIRCUIT SCHEMATIC 0000-5015-100.
4. FROM T1, WHITE WIRE CONNECTS TO E17; BLACK WIRE CONNECTS TO E18.
5. INSTALL Q34 AND Q35 SO THAT METAL SIDE FACES AWAY FROM T1.
6. R114, R115, R137, R138, R140 and R145 TO BE MOUNTED 0.10" FROM SURFACE OF PC BOARD.
7. ALL OTHER PARTS EXCEPT C32, C45, C55, C59, C62, C63, C69, Q34, Q35, T1 AND L3 TO BE MOUNTED WITH 0.40" MAX HEIGHT FROM SURFACE OF PC BOARD.

THRU SER. NO. 2099

Figure 6-26 Oscilloscope Control and Deflection PC Board (Sheet 1 of 2)







NOTES:

1. THE REF DES SERIES FOR OSCILLOSCOPE CONTROL AND DEFL. PC BD ASSY IS 5100 AND 9500 (I.E., R1 IS R5101 AND R101 IS R9501). FOR INVERTER PC BD REF DES SERIES IS 9900.

2. DATA PART NO.:
   A. OSCILLOSCOPE CONTROL AND DEFLECTION PC BD - 7010-5035-100.
   B. INVERTER PC BD - 7010-5036-600.

3. REFER TO CIRCUIT SCHEMATIC:
   A. OSCILLOSCOPE CONTROL AND DEFLECTION PC BD - 0000-5015-100.
   B. INVERTER PC BD - 0000-5016-600.

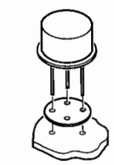
4. FROM T1, WIRE CONNECTS TO E17; BLACK WIRE CONNECTS TO E18.

5. R114, R115, R138, R140 AND R145 TO BE MOUNTED 0.10" FROM SURFACE OF PC BOARD.

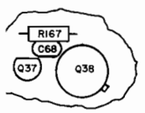
6. ALL OTHER PARTS EXCEPT C32, C45, C62, C63, C69, T1 AND L3 TO BE MOUNTED WITH 0.40" MAX HEIGHT FROM SURFACE OF PC BOARD.

7. INVERTER PC BD ADDED SER. NO. 2100, RETROFITTED TO SOME EARLIER UNITS.

8. EFFECTIVE SER. NO. 2768, C79 AND C80 ADDED.

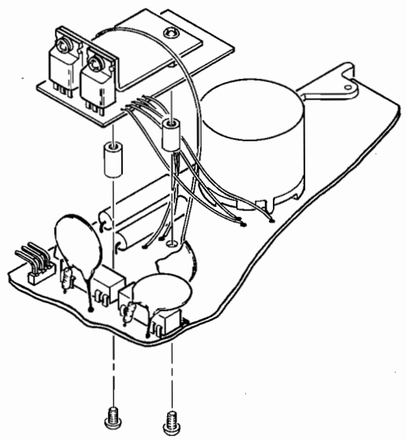


DETAIL **C**



U SER. NO. 2657

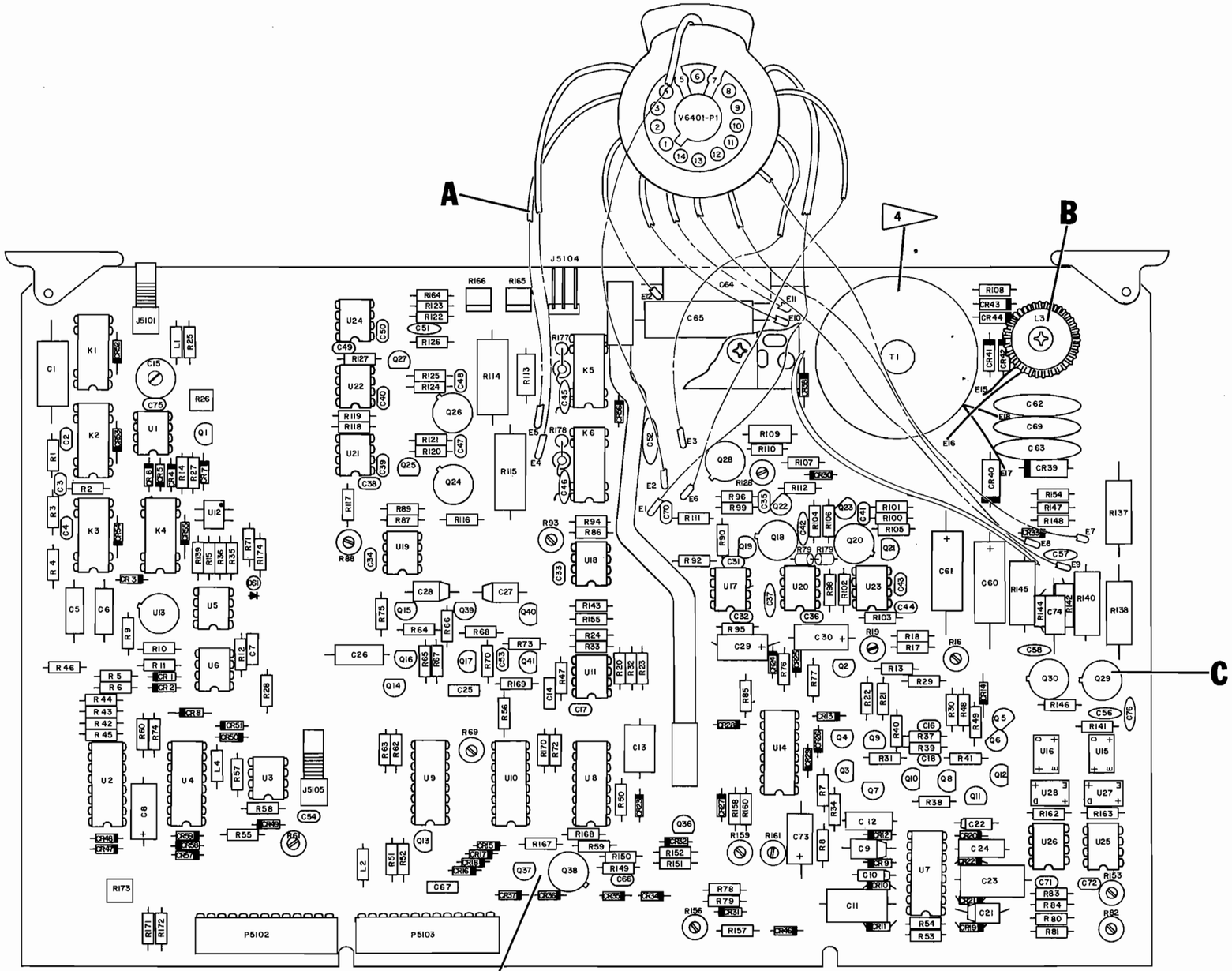
DETAIL **D**

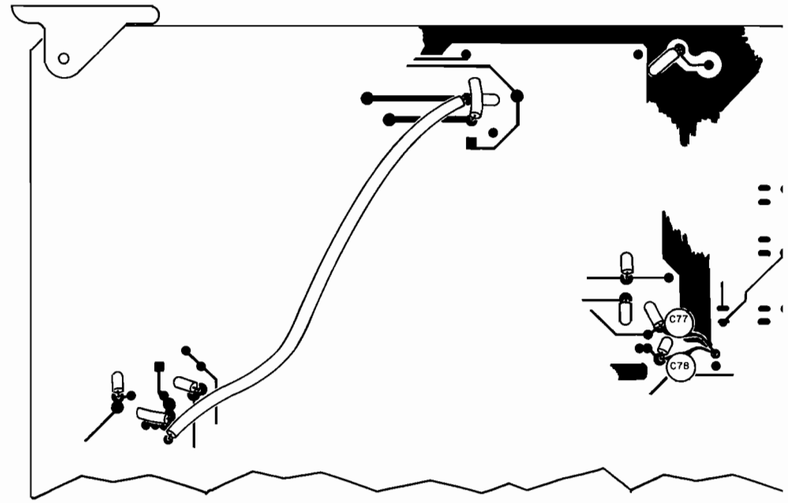


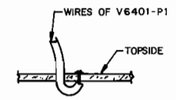
OSCILLOSCOPE CONTROL AND DEFLECTION PC BD WITH INVERTER ASSY 7

SER. NO. 2100 AND ON

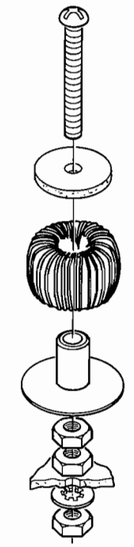
Figure 6-26 Oscilloscope Control and Deflection PC Board (Sheet 2 of 2)



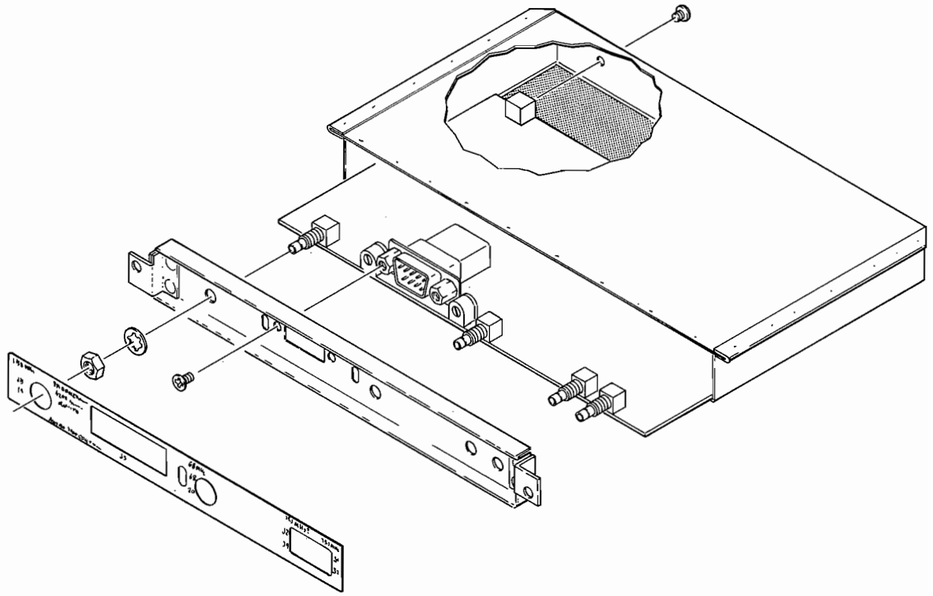




DETAIL **A**



DETAIL **B**



NOTES:

MECH ASSY

1. THE REF DES SERIES FOR FM GENERATOR MECH ASSY IS 4200 (I.E., J1 IS J4201).
2. DATA PART NO. 7005-5043-300.
3. REF CIRCUIT SCHEMATIC 0000-5013-300.

PC BOARD

1. THE REF DES SERIES FOR FM GENERATOR PC BOARD ASSY IS 3300 (I.E., R1 is R3301).
2. DATA PART NO. 7010-5033-300.
3. REF CIRCUIT SCHEMATIC 0000-5013-300.

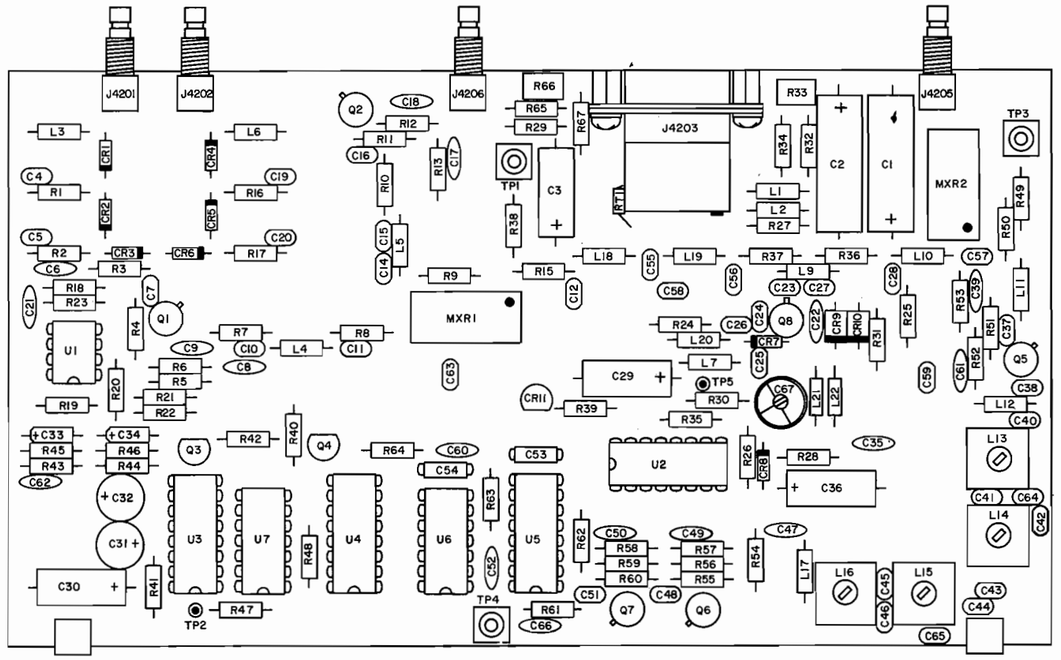
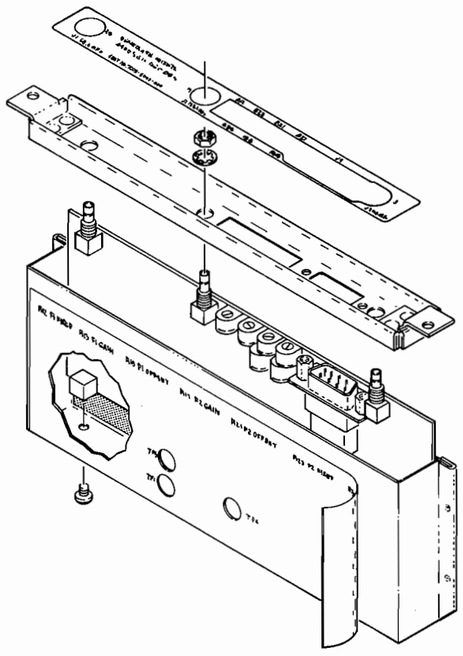


Figure 6-27 FM Generator Module



NOTES:

MECH ASSY

1. THE REF DES SERIES FOR GENERATOR MIXER MECH ASSY IS 4400 (I.E., J1 IS J4401).
2. DATA PART NO. 7005-5043-400.
3. REF CIRCUIT SCHEMATIC 0000-5013-400.

PC BOARD

1. THE REF DES SERIES FOR GENERATOR MIXER PC BOARD ASSY IS 3400 (I.E., R1 IS R3401).
2. DATA PART NO. 7010-5033-400.
3. REF CIRCUIT SCHEMATIC 0000-5013-400.

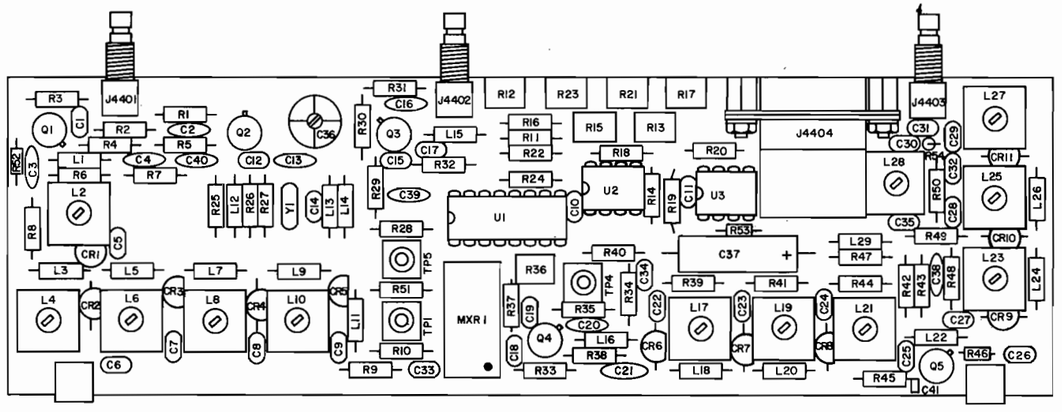
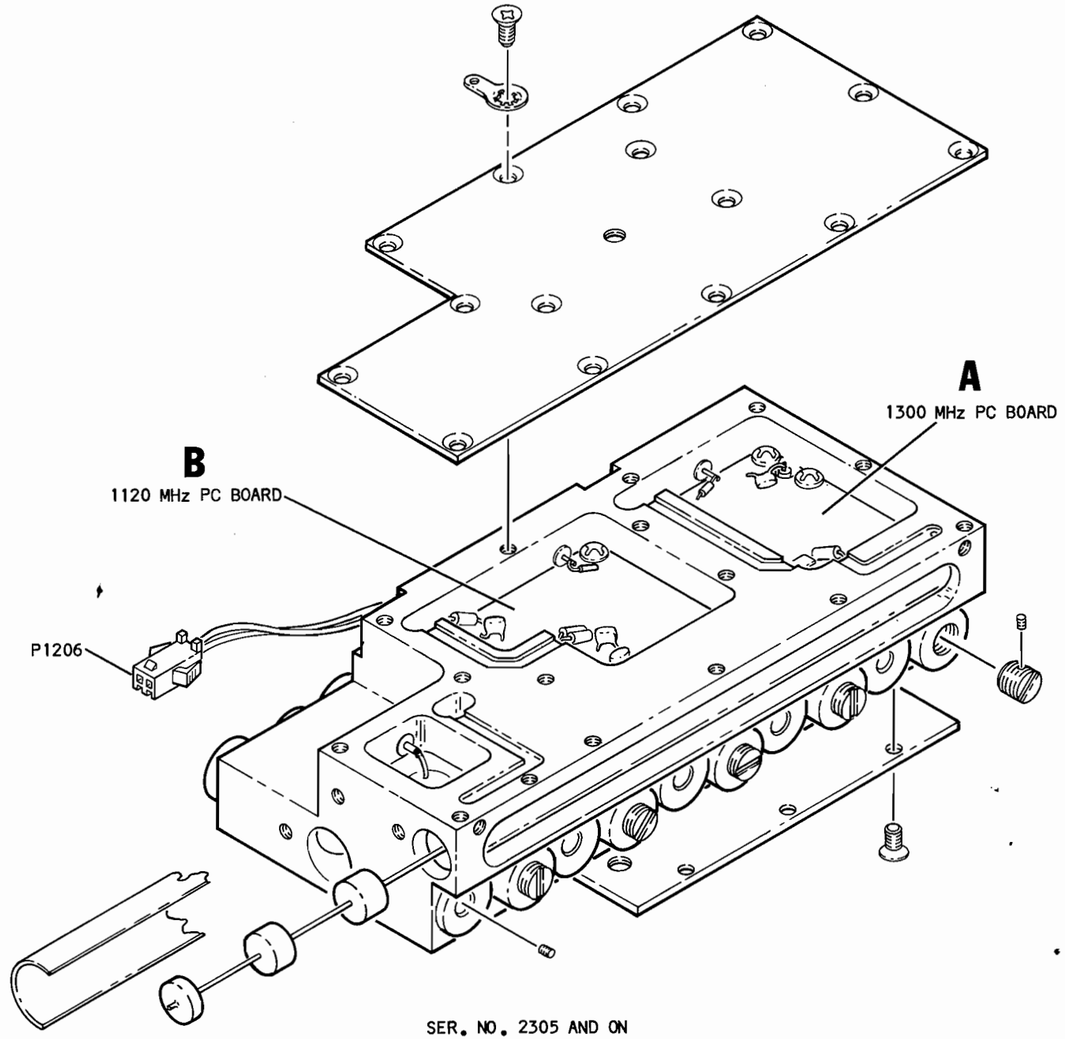
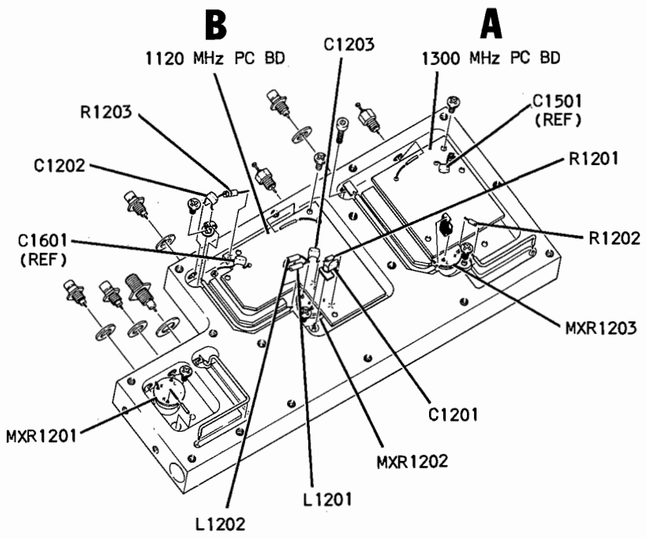


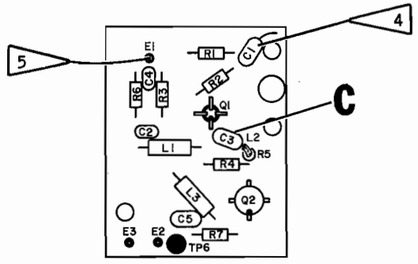
Figure 6-28 Generator Mixer Module



SER. NO. 2305 AND ON

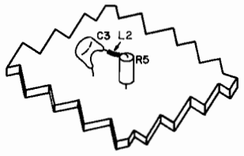


ALL UNITS

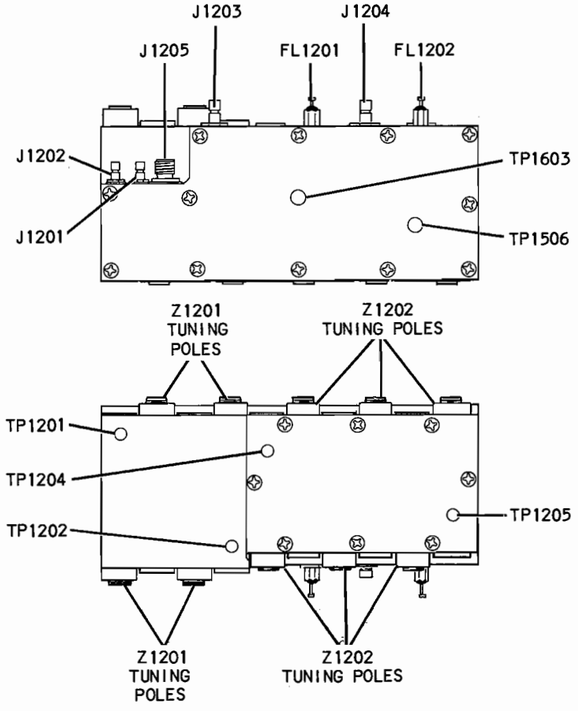


1300 MHz PC BOARD

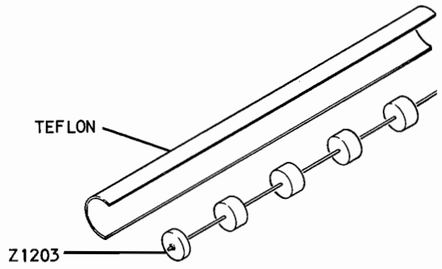
DETAIL **A**



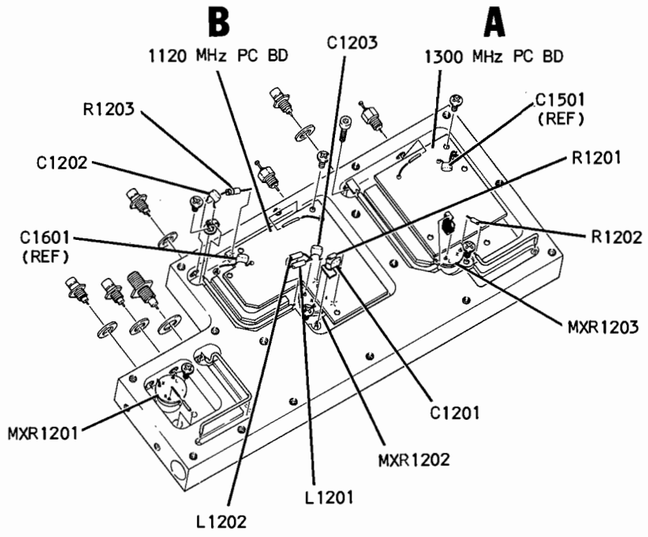
DETAIL **C**



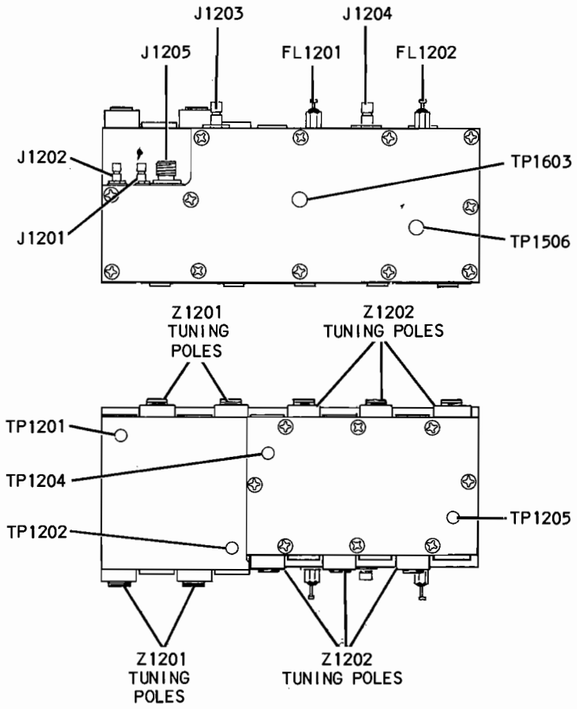
ALL UNITS



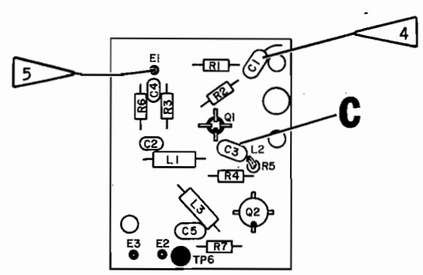
THR



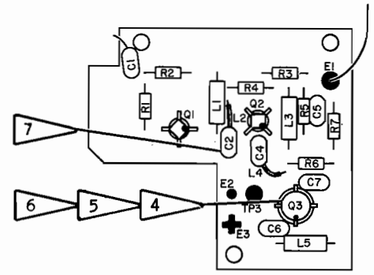
ALL UNITS



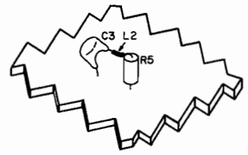
ALL UNITS



DETAIL **A**



DETAIL **B**



DETAIL **C**

NOTES:

MECH ASSY

1. THE REF DES SERIES FOR 1300 MHz IF GENERATOR MECH ASSY IS 1200 (I.E., J1 IS J1201).
2. DATA PART NO. 7005-5041-500.
3. REF CIRCUIT SCHEMATIC 0000-5011-500.

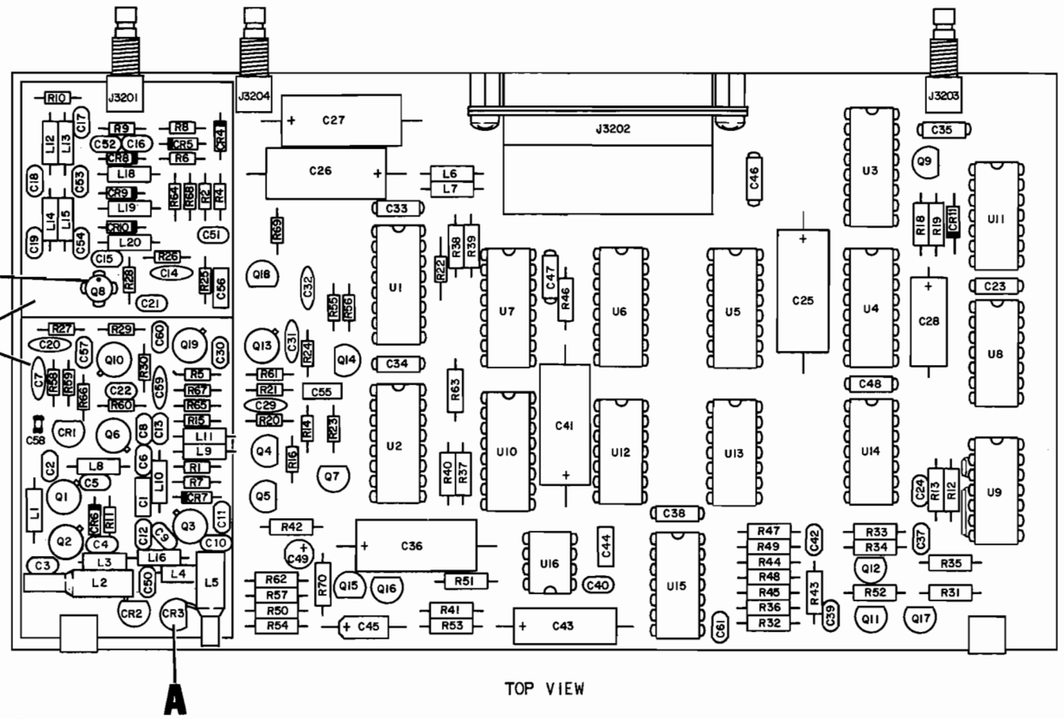
1300 MHz PC BOARD

1. THE REF DES SERIES FOR 1300 MHz PC BOARD ASSY IS 1500 (I.E., R1 IS R1501).
2. DATA PART NO. 7010-5031-500.
3. REF CIRCUIT SCHEMATIC 0000-5011-500.
4. THE LEAD ON C1 TO BE 3" LONG AND FLOATING UNTIL NEXT ASSEMBLY.
5. BUS WIRE TO BE 2.0" LONG AND FLOATING UNTIL NEXT ASSEMBLY.
6. L2 IS FORMED BY .3" LONG LEAD OF C3, SLEEVED.

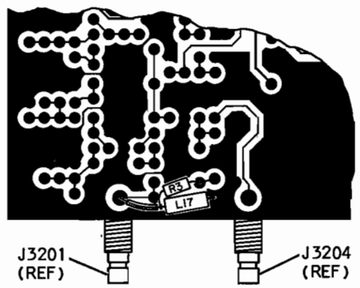
1120 MHz PC BOARD

1. THE REF DES SERIES FOR 1120 MHz PC BOARD ASSY IS 1600 (I.E., R1 IS R1601).
2. DATA PART NO. 7010-5031-600.
3. REF CIRCUIT SCHEMATIC 0000-5011-500.
4. Q1, Q2 AND Q3 TO MOUNT HOLES IN PC BOARD. Q1 AND Q2 TO BE MOUNTED SO THAT THE "U" (ON THE CASE OF THE TRANSISTOR) SHOWS THROUGH TO BOTTOM SIDE OF BOARD.
5. TRIM LEADS ON Q1, Q2 AND Q3 TO .100" FROM BODY.
6. TRANSISTOR COLLECTOR LEAD INDICATED BY DOT ON Q1, Q2 AND Q3.
7. TRIM LEADS OF C2 AND C4 TO .5" AND SLEEVE WITH TUBING TO FORM L2 AND L4.

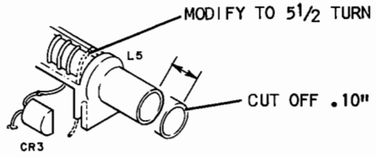
Figure 6-29 1300 MHz IF Generator Module



TOP VIEW



BOTTOM VIEW



EFFECTIVE SER. NO. 1183 & ON

DETAIL **A**

NOTES:

MECH ASSY

1. THE REF DES SERIES FOR DUPLEX OFFSET MECH ASSY IS 3200 (I.E., J1 IS J3210).
2. DATA PART NO. 7005-5042-700.
3. REF CIRCUIT SCHEMATIC 0000-5012-700.

PC BOARD

1. THE REF DES SERIES FOR DUPLEX OFFSET PC BOARD ASSY IS 2700 (I.E., R1 IS R2701).
2. DATA PART NO. 7010-5032-700.
3. REF CIRCUIT SCHEMATIC 0000-5012-700.
4. NOT USED.
5. ATTACH INSULATORS TO INSIDE OF SHIELDS ON BOTTOM OF PC BOARD.
6. TRANSISTOR COLLECTOR LEAD INDICATED BY DOT ON Q8.

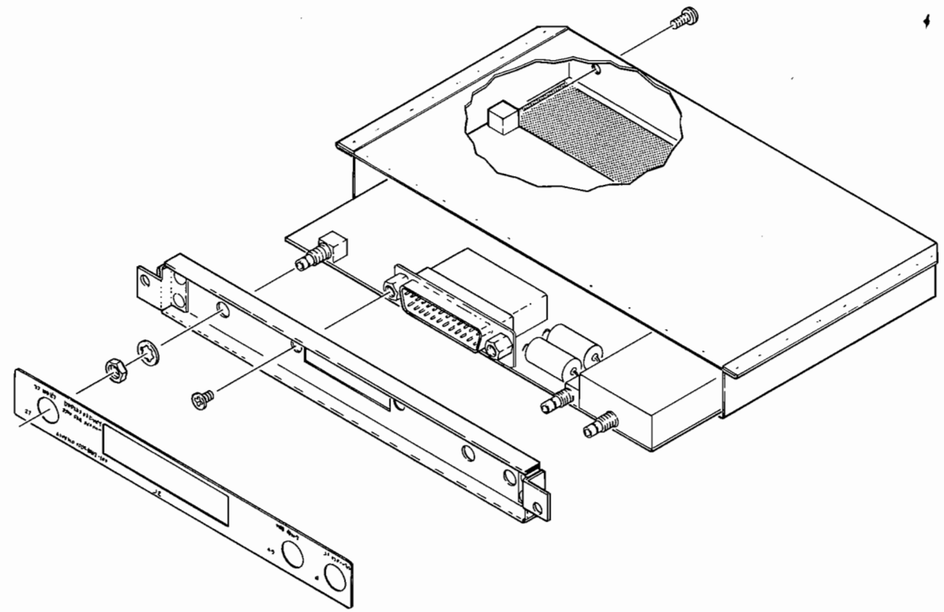
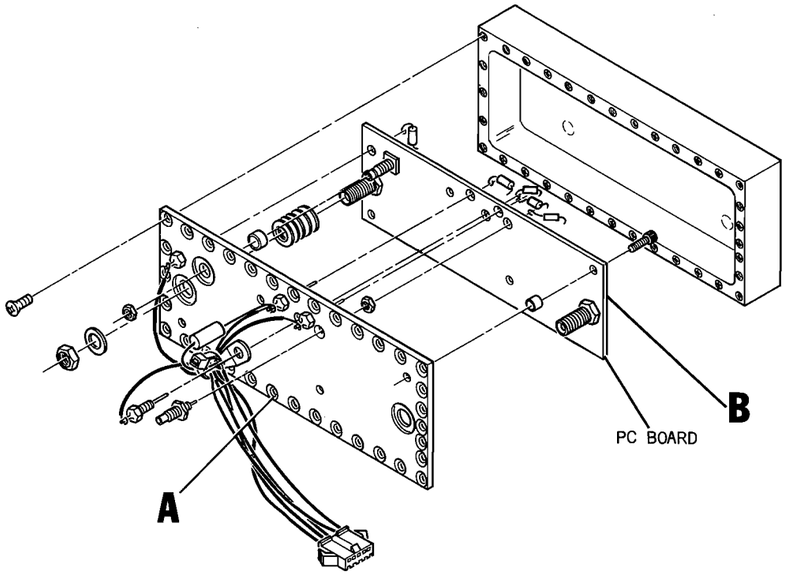
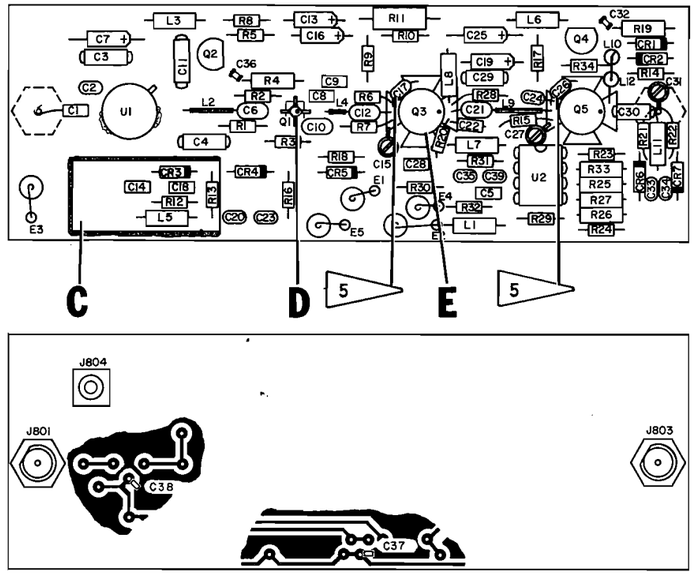


Figure 6-30 Duplex Offset Module





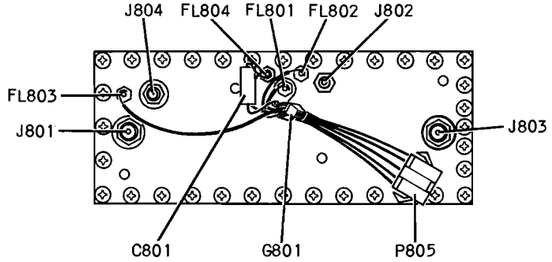
NOTES:

MECH ASSY

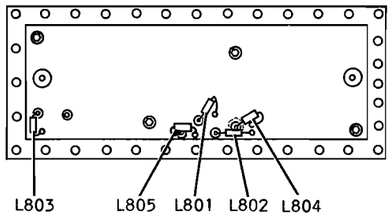
1. THE REF DES SERIES FOR OUTPUT MECH ASSY IS 800 (I.E., J1 IS J801).
2. DATA PART NO. 7005-5040-900, 7005-5040-901.
3. REF CIRCUIT SCHEMATIC 0000-5015-900.

PC BOARD

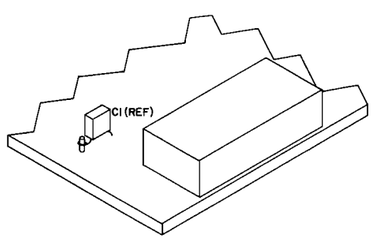
1. THE REF DES SERIES FOR OUTPUT AMPLIFIER PC BOARD ASSY IS 900 (I.E., R1 IS R901).
2. DATA PART NO. 7010-5030-900, 7010-5030-901.
3. REF CIRCUIT SCHEMATIC 0000-5010-900
4. TRANSISTOR COLLECTOR LEAD INDICATED BY DOT ON Q1, Q3 AND Q5.
5. SOLDER DIRECTLY TO TRANSISTOR. MAKE LEADS AS SHORT AS POSSIBLE.
6. USE 0.1 IN. SQUARE OF TAPE UNDER Q1.
7. L2 IS .6" LEAD OF C6
   L4 IS .5" LEAD OF C12
   L1 IS .6" LEAD OF C21
8. NO LEAD LENGTH ALLOWED ON NPO CAPS.
9. R1, R7 AND R28 ARE SAT (SELECTED AT TEST).



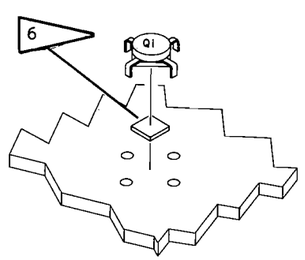
DETAIL **A**



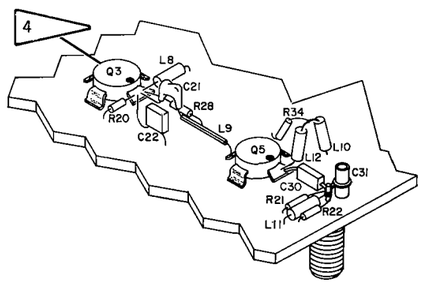
DETAIL **B**



DETAIL **C**



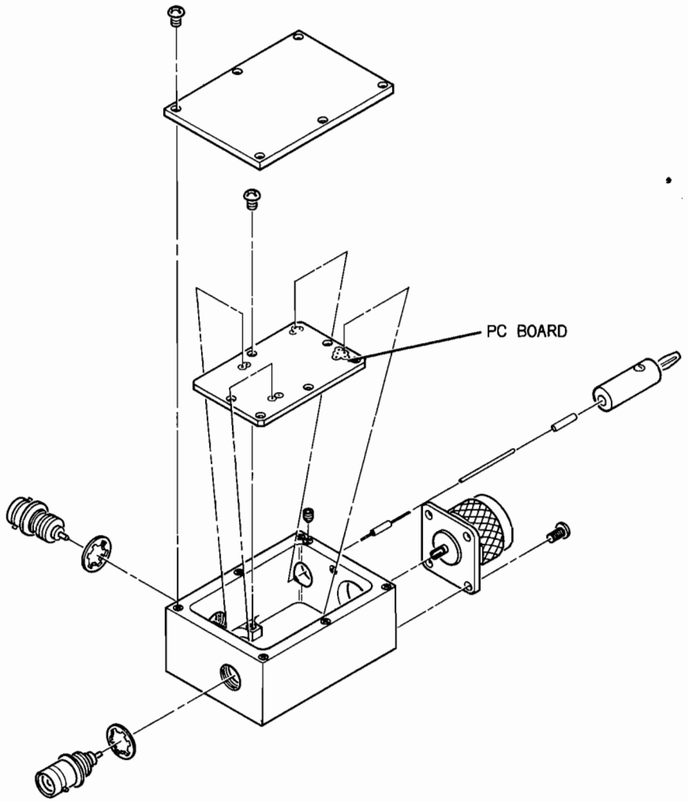
DETAIL **D**

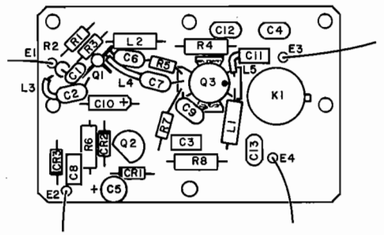


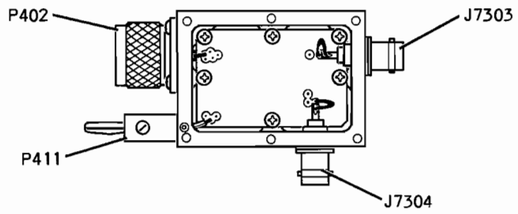
DETAIL **E**

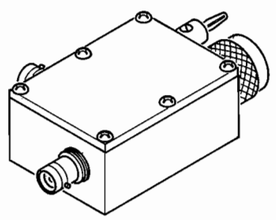
WIRE RUNNING LIST				
FROM	TO	COLOR	AWG	LENGTH
P805-1	FL802	YEL	26	4"
P805-2	FL804	GRN	26	3"
P805-3	FL803	BRN	26	5"
P805-4	FL801	RED	26	3"
P805-5	G801	BLK	26	3"
C801 GOES FROM FL804 TO G804.				

Figure 6-31 Output Amplifier Module









NOTES:

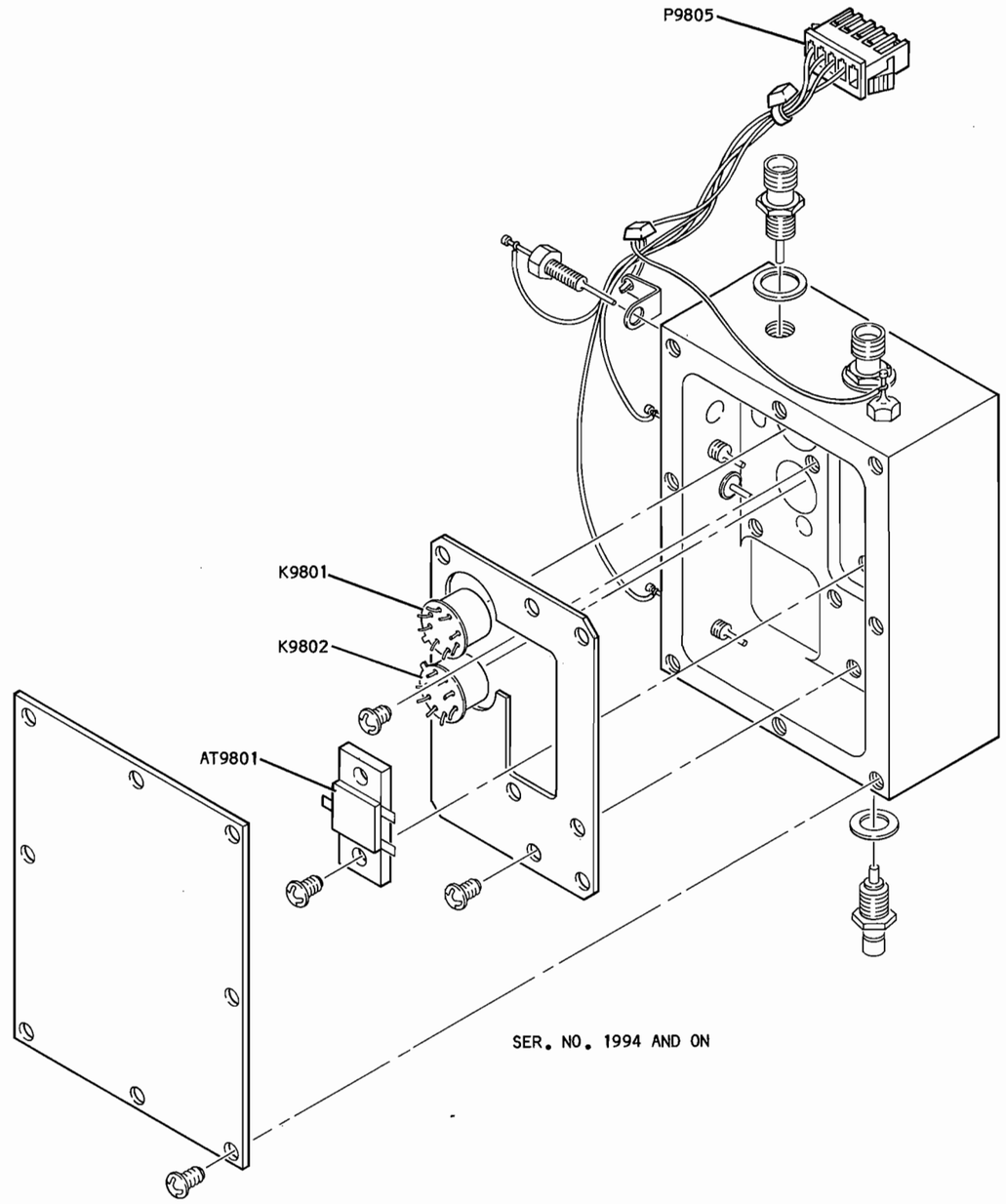
MECH ASSY

1. THE REF DES SERIES FOR HIGH OUTPUT AMPLIFIER MECH ASSY IS 7300 (I.E., J3 IS J7303).
2. DATA PART NO. 7001-5045-400.
3. REF CIRCUIT SCHEMATIC 0000-5015-400.

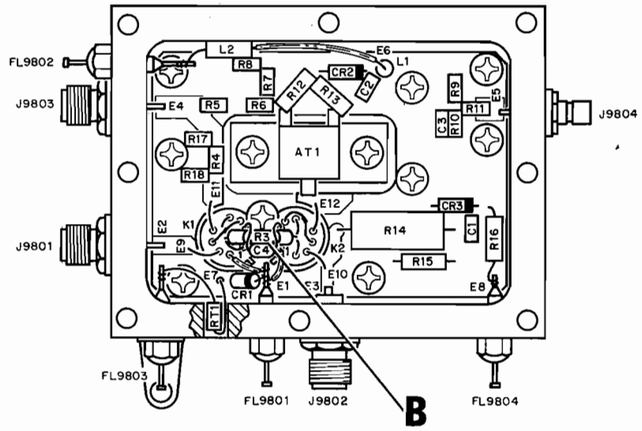
PC BOARD

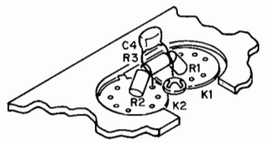
1. THE REF DES SERIES FOR HIGH OUTPUT AMPLIFIER PC BOARD ASSY IS 7200 (I.E., R1 IS R7201).
2. DATA PART NO. 7010-5035-400.
3. REF CIRCUIT SCHEMATIC 0000-5015-400.
4. DOT NEXT TO Q3 REP. COLLECTOR LEAD.

Figure 6-32 High Output Amplifier Module (Option 04)

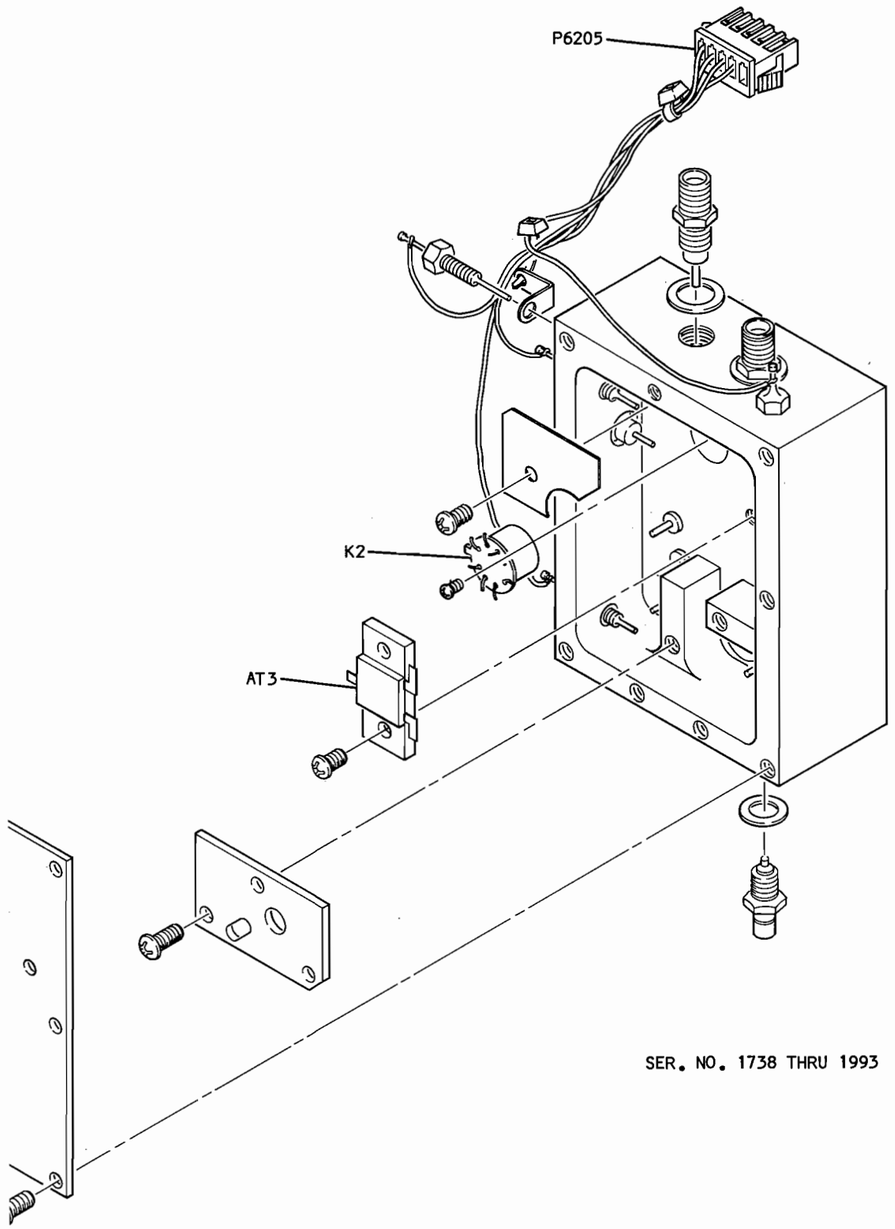


SER. NO. 1994 AND ON

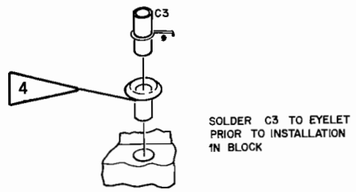




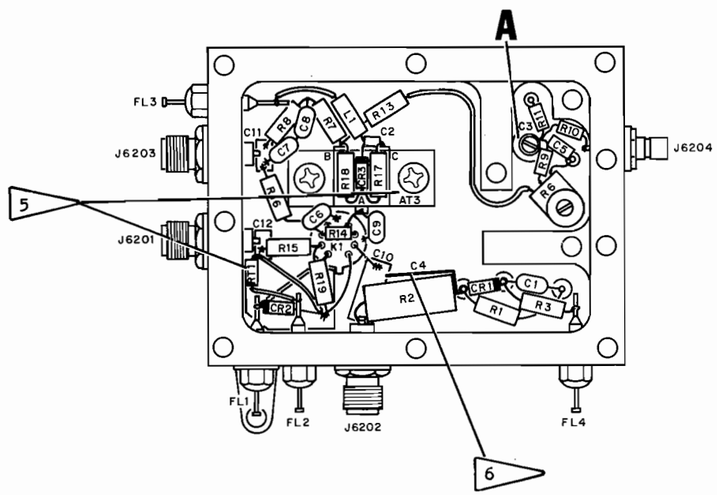
DETAIL **B**



SER. NO. 1738 THRU 1993



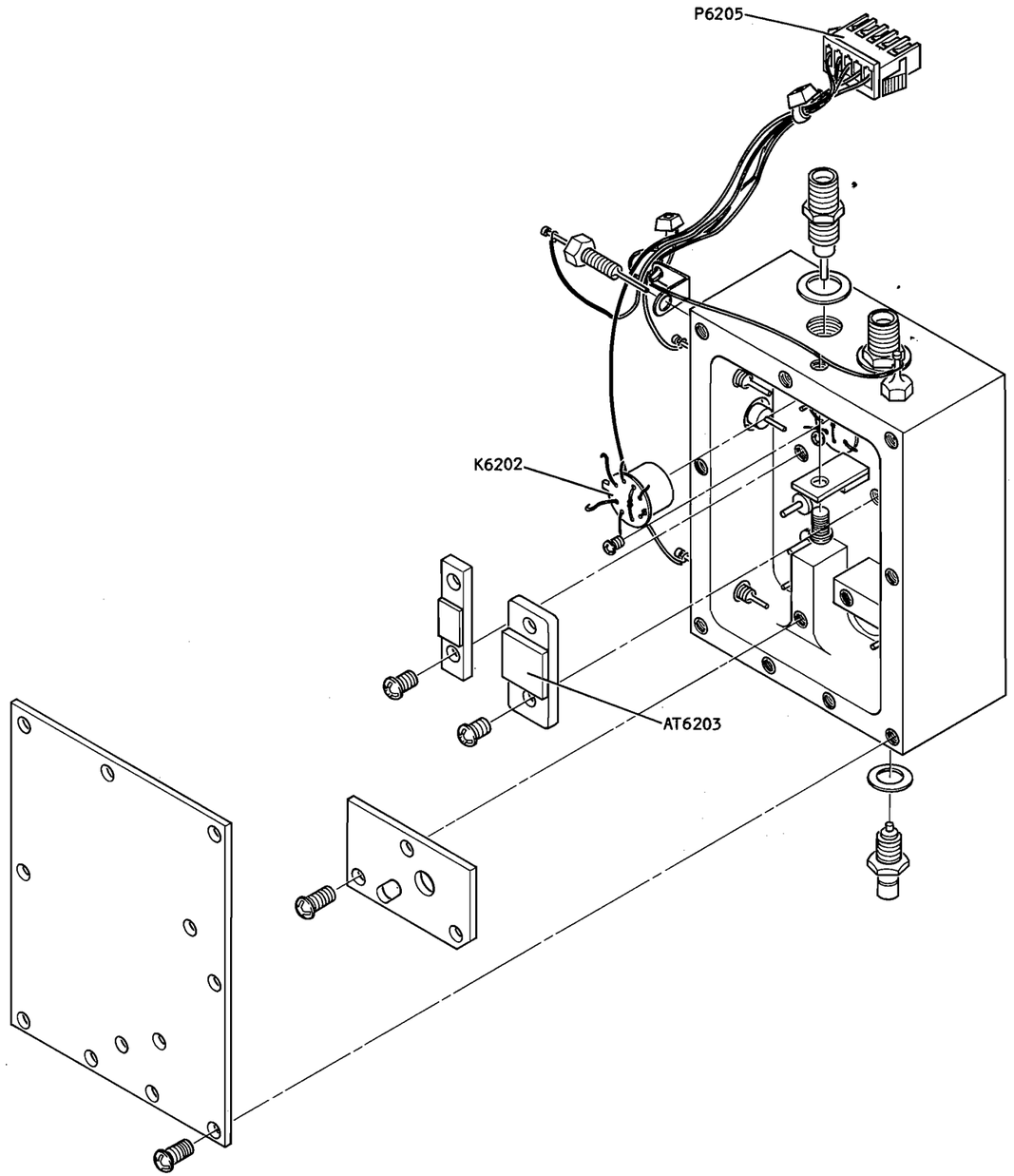
DETAIL **A**

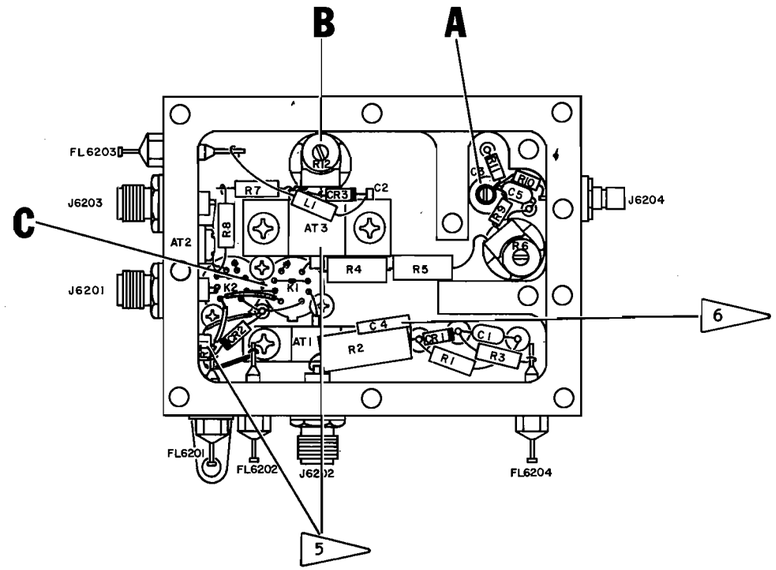


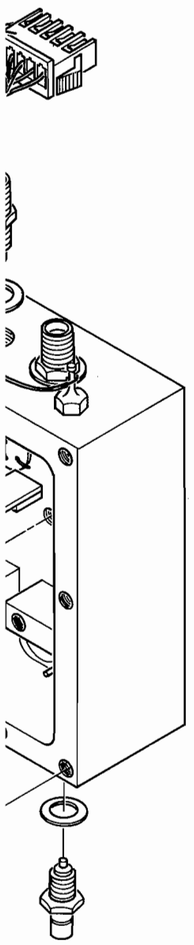
NOTES:

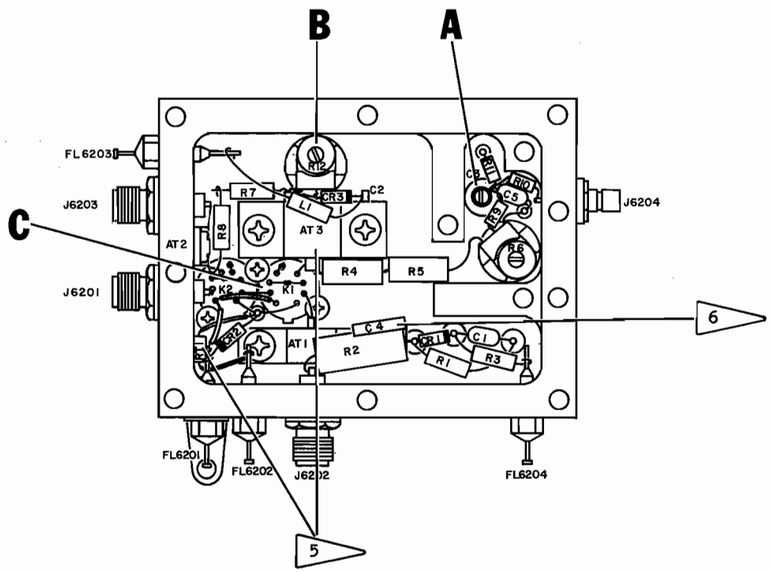
1. EFFECTIVE SER. NO. 1994, THE REF DES SERIES FOR POWER TERMINATION IS 9800; THIS WAS 6200 (E.G., J1 IS J9801, WAS J6201).
2. EFFECTIVE SER. NO. 1994, DATA PART NO. IS 7005-5048-400; WAS 7005-5046-100.
3. EFFECTIVE SER. NO. 1994, REF CIRCUIT SCHEMATIC IS 0000-5018-400, WAS 0000-5016-100.
4. THRU SER. NO. 1993, C3 MUST BE SOLDERED TO EYELET BEFORE INSTALLING EYELET INTO BLOCK.
5. THRU SER. NO. 1993, APPLY THERMAL COMPOUND UNDER AT3 AND RT1. (RT1 MUST LIE AGAINST BLOCK SURFACES.)
6. EFFECTIVE THRU SER. NO. 1993, C4 WAS A FABRICATED VARIABLE CAPACITOR. CAPACITANCE IS VARIED BY MOVING C4 RELATIVE TO R2.

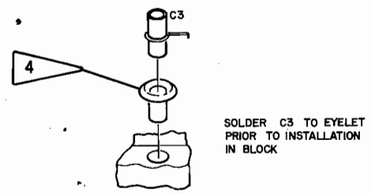
Figure 6-33 Power Termination Module (Sheet 1 of 2)


P6205
K6202
AT6203

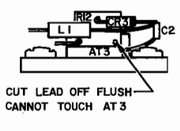

B
A
C
FL6203
J6203
J6201
J6204
FL6201
FL6202
FL6204
AT1
AT2
AT3
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
C1
C2
C3
C4
C5
C6
CR1
CR2
CR3
L1
K1
K2
5
6



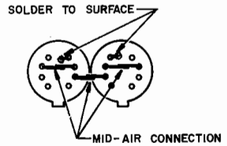




DETAIL **A**



DETAIL **B**



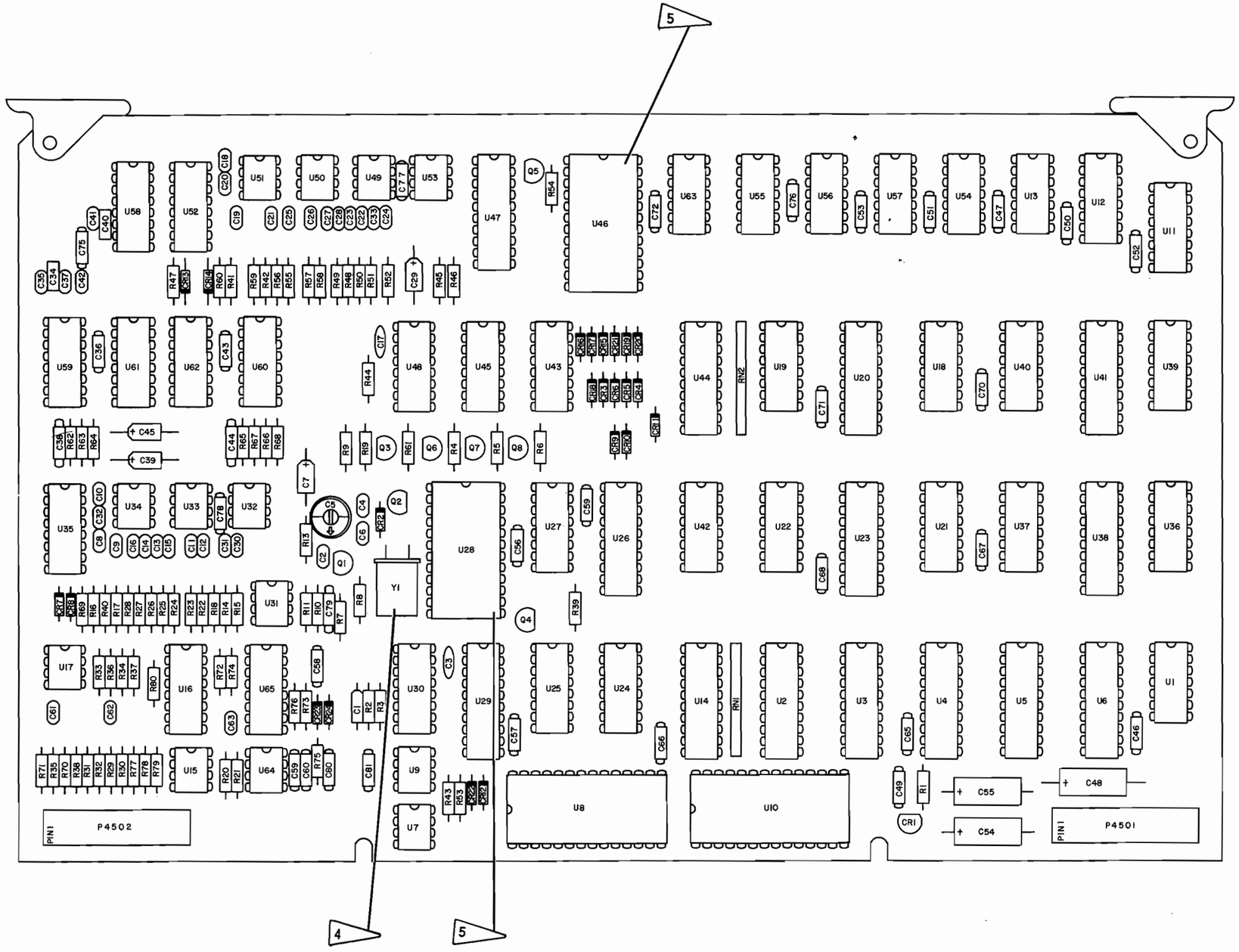
DETAIL **C**

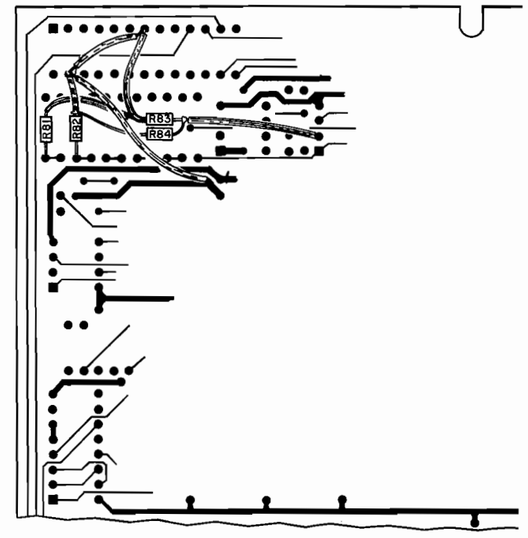
NOTES (THRU SER. NO. 1737):

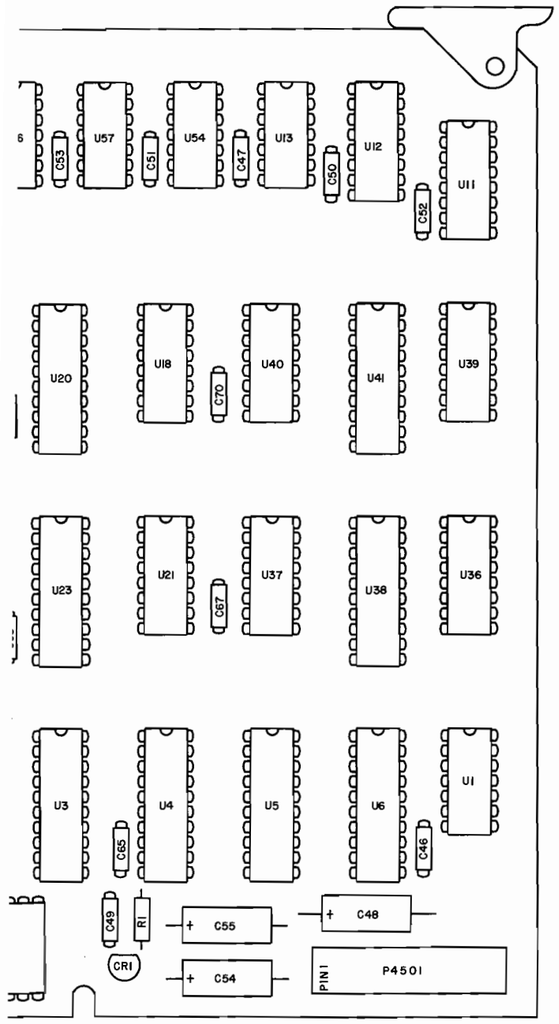
1. REF DES SERIES IS 6200 (E.G., J1 IS J6201).
2. DATA PART NO. IS 7005-5046-100.
3. REF CIRCUIT SCHEMATIC 7005-5016-100.
4. C3 MUST BE SOLDERED TO EYELET, BEFORE INSTALLING EYELET INTO BLOCK.
5. APPLY THERMAL COMPOUND UNDER AT3 AND RT1. (RT1 MUST LIE AGAINST BLOCK SURFACES).
6. C4 IS A FABRICATED VARIABLE CAPACITOR. CAPACITANCE IS VARIED BY MOVING C4 RELATIVE TO R2.

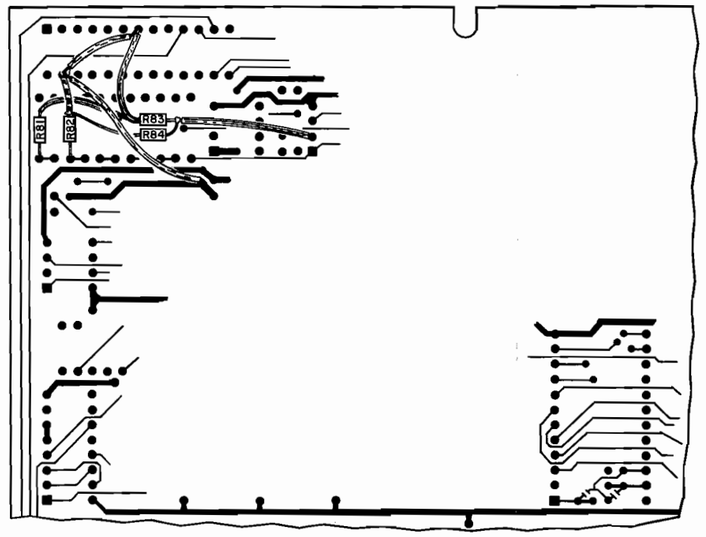
THRU SER. NO. 1737

Figure 6-33 Power Termination (Sheet 2 of 2)


5
U58
U52
U51
U50
U49
U53
U47
U46
U63
U55
U56
U57
U54
U13
U12
U11
U59
U61
U62
U60
U48
U45
U43
U44
U19
U20
U18
U40
U41
U39
U35
U34
U33
U32
U28
U27
U26
U42
U22
U23
U21
U37
U38
U36
U31
Y1
U17
U16
U65
U30
U29
U25
U24
U14
U2
U3
U4
U5
U6
U1
U15
U64
U9
U7
U8
U10
P4502
PIN1
P4501
PIN1
4
5


R81
R82
R83
R84

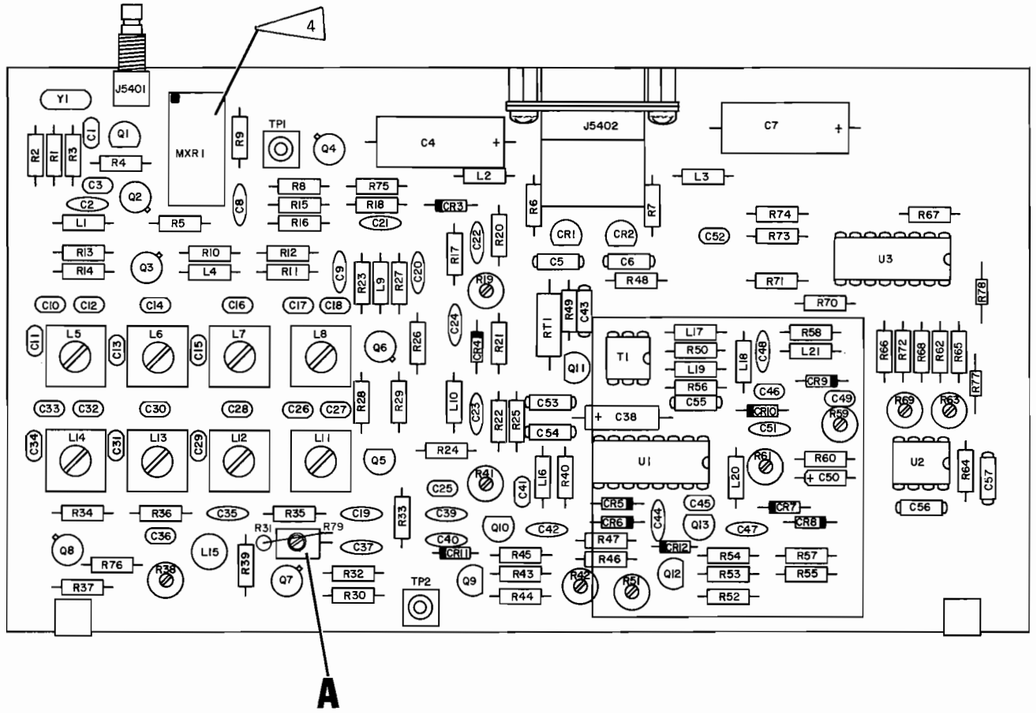


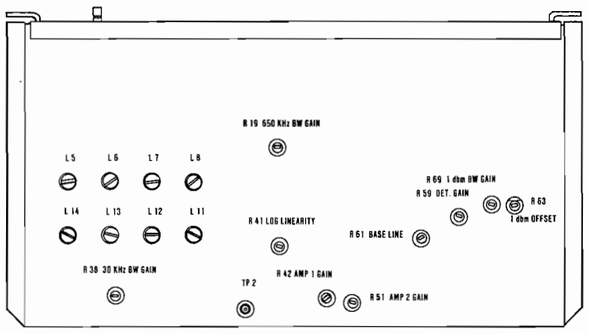


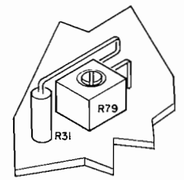
NOTES:

1. THE REF DES SERIES FOR DUAL TONE GENERATOR PC BOARD ASSY IS 4500 (I.E., J1 IS J4501)
2. DATA PART NO. 7010-5034-500
3. REF CIRCUIT SCHEMATIC 0000-5014-500
4. LAY Y1 ON ITS SIDE TO AVOID INTERFERENCE WITH OTHER PC BOARDS.
5. EFFECTIVE THRU SER. NO. 2639, U28 AND U46 SOCKET MOUNTED. EFFECTIVE SER. NO. 2640 AND ON. U28 AND U46 SURFACE MOUNTED PARTS.

Figure 6-34 Dual Tone Generator PC Board







EFFECTIVE SER. NO. 2931 AND ON

DETAIL **A**

NOTES:

MECH ASSY

1. THE REF DES SERIES FOR SPECTRUM ANALYZER IF MECH ASSY IS 5400 (I.E., J1 IS J5401).
2. DATA PART NO. 7005-5043-900.
3. REF CIRCUIT SCHEMATIC 0000-5013-900.

PC BOARD

1. THE REF DES SERIES FOR SPECTRUM ANALYZER IF PC BOARD ASSY IS 3900 (I.E., R1 IS R3901).
2. DATA PART NO. 7010-5033-900.
3. REF CIRCUIT SCHEMATIC 0000-5013-900.

4. > PIN WITH BLUE INSULATOR IS PIN 1.

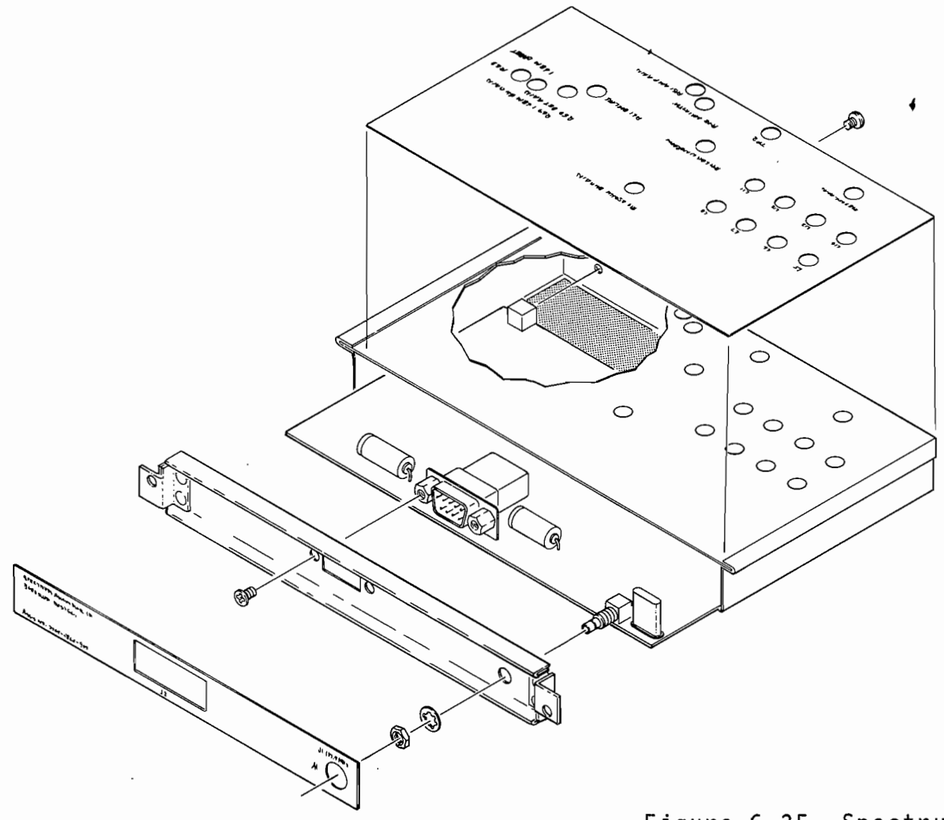
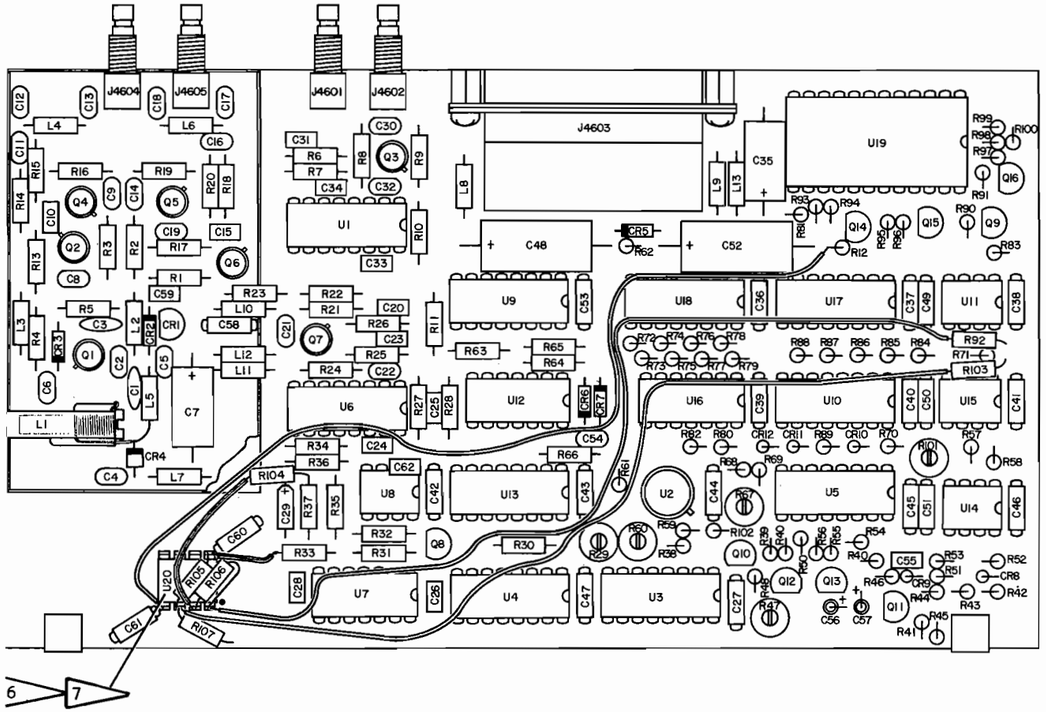
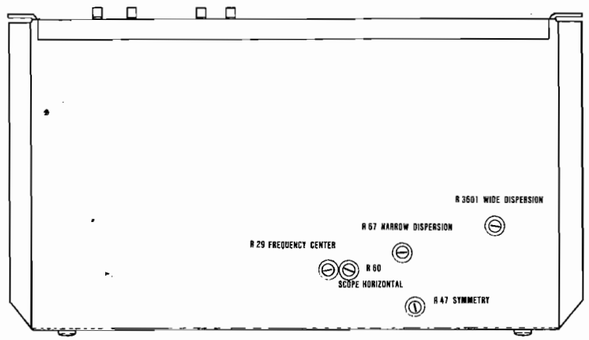
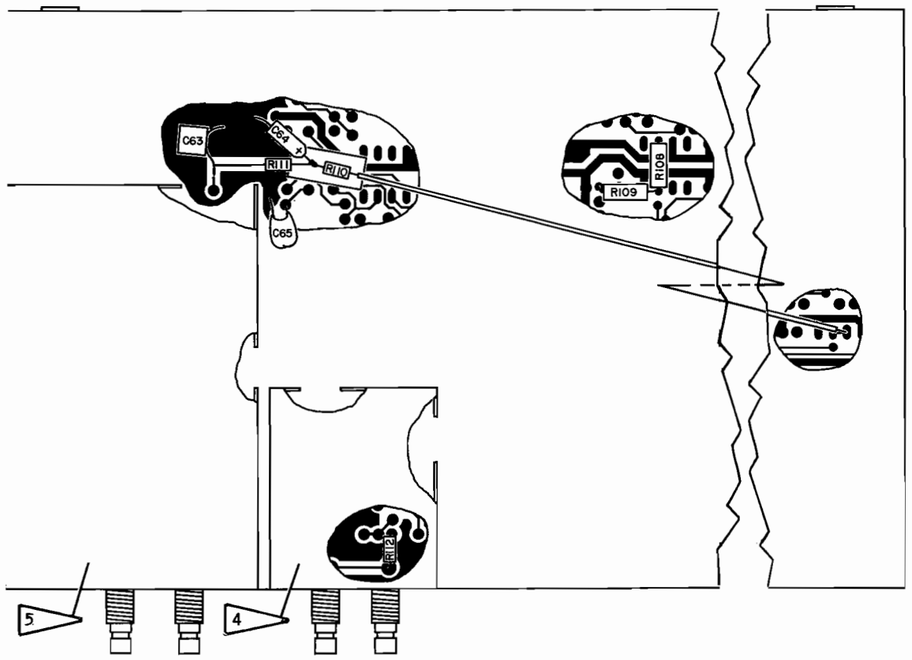
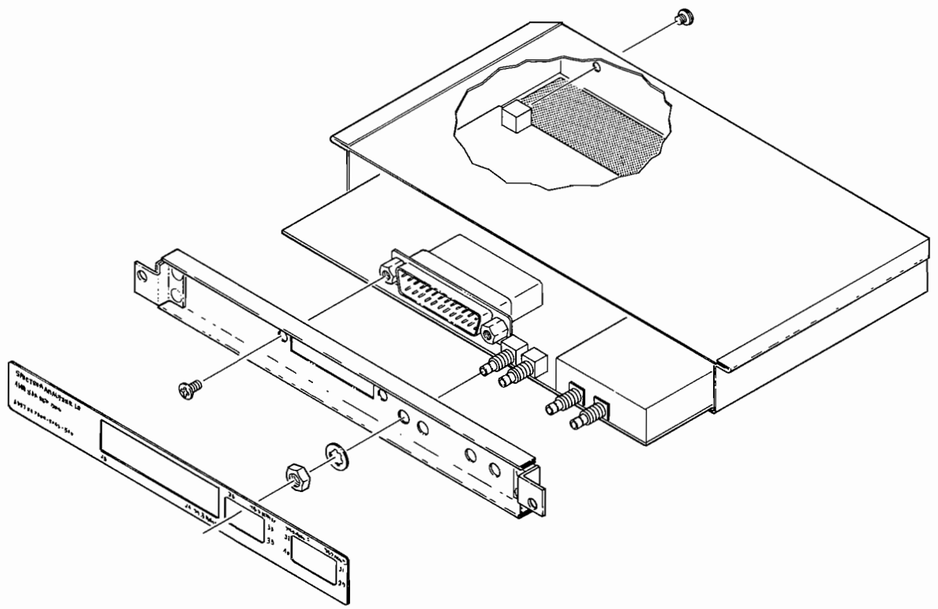


Figure 6-35 Spectrum Analyzer IF Module









NOTES:

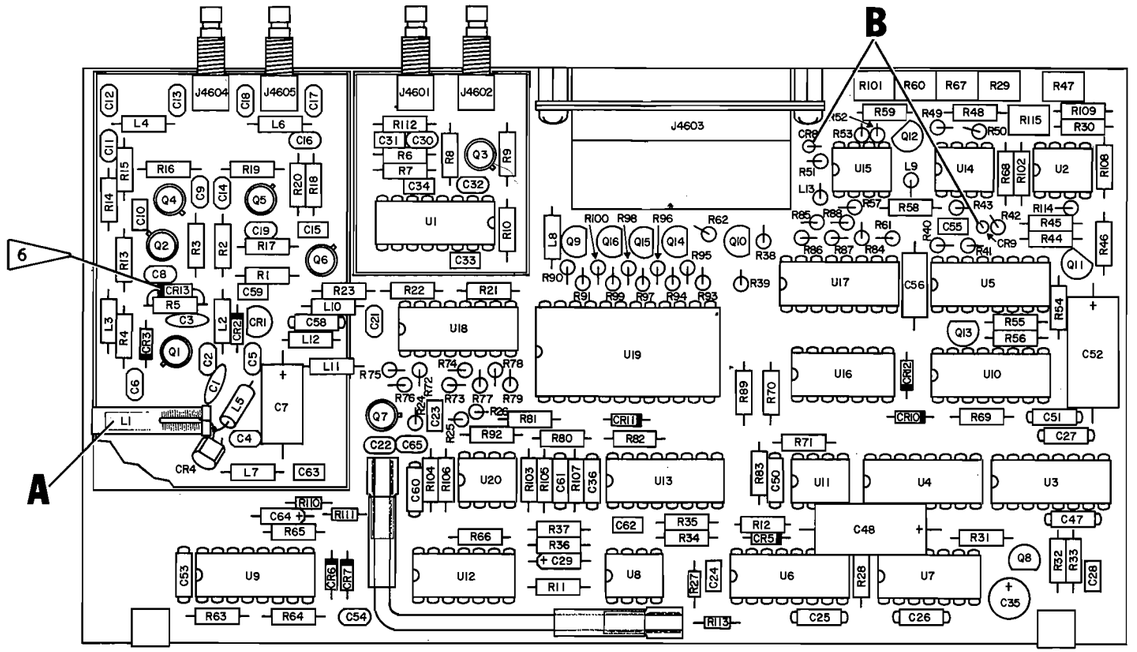
MECH ASSY

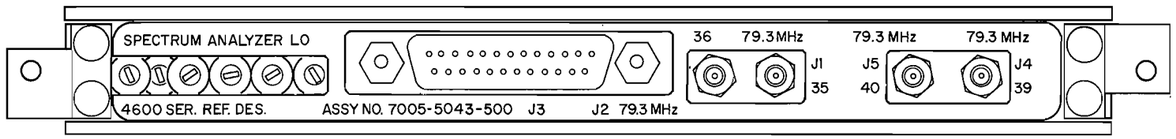
1. THE REF DES SERIES FOR SPECTRUM ANALYZER LO MECH ASSY IS 4600 (I.E., J1 IS J4601).
2. DATA PART NO. 7005-5043-500.
3. REF CIRCUIT SCHEMATIC 0000-5013-500.
4. THIS DRAWING TAKES PRECEDENCE OVER ANY EXISTING LABELS INSTALLED IN THE FM/AM-1500.

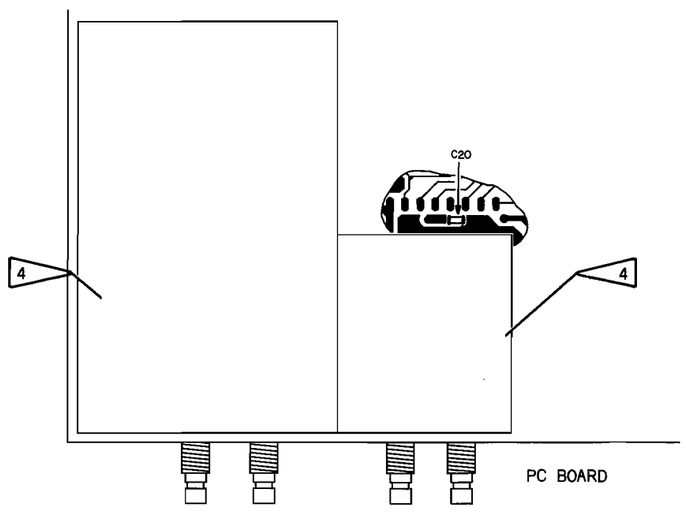
PC BOARD (1005 THRU 1351)

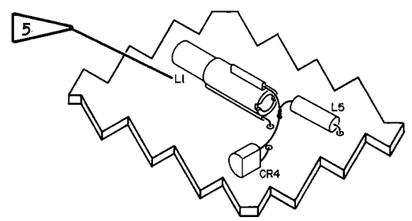
1. THE REF DES SERIES FOR SPECTRUM ANALYZER LO PC BOARD ASSY ARE 3500 AND 3600 (I.E., R1 IS R3501 AND R100 IS R3600).
2. DATA PART NO. 7010-5033-500.
3. REF CIRCUIT SCHEMATIC 0000-5013-500.
4. ATTACH INSULATOR TO THE INSIDE OF SHIELD.
5. ATTACHING INSULATOR TO THE INSIDE OF SHIELD.
6. THE ASTERISK (*) NEXT TO U20 REPRESENTS LOCATION OF PIN 1.
7. U20 TO BE MOUNTED UPSIDE DOWN ON PC BOARD.

Figure 6-36 Spectrum Analyzer LO Module (Sheet 1 of 2)
EFF. SER. NO. 1005 THRU 1351

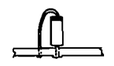




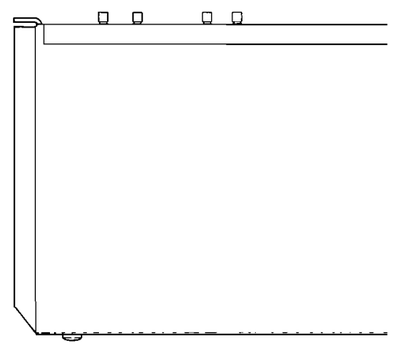


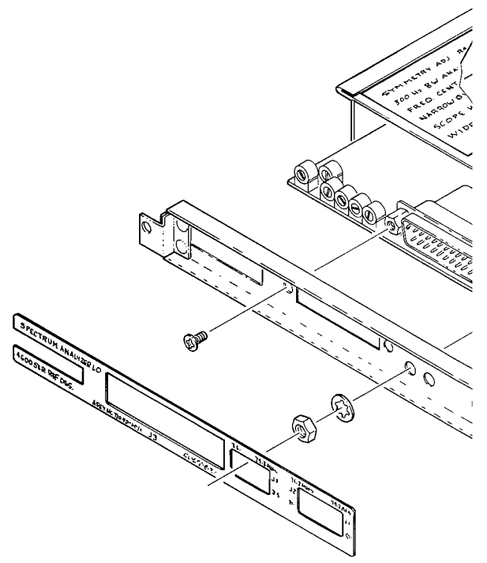


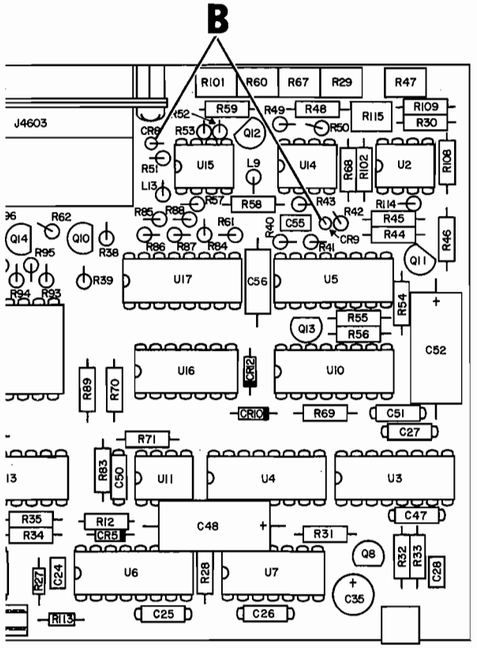
DETAIL **A**

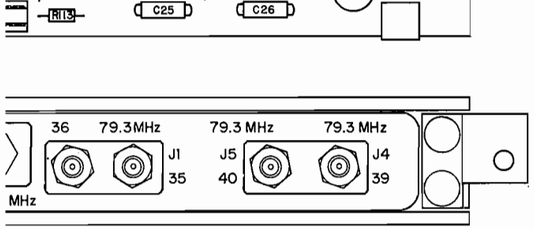


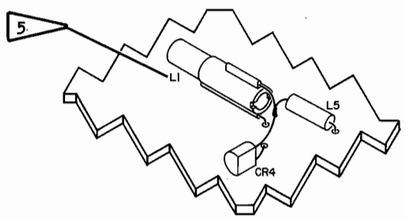
DETAIL **B**



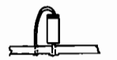




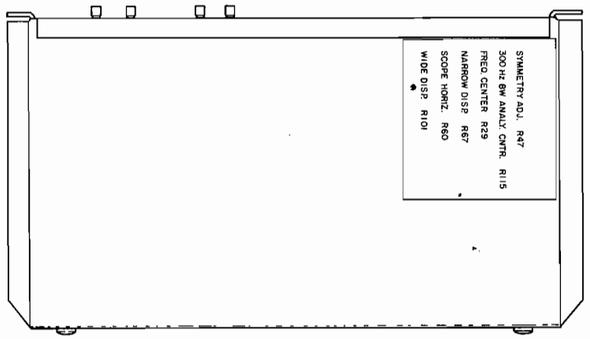


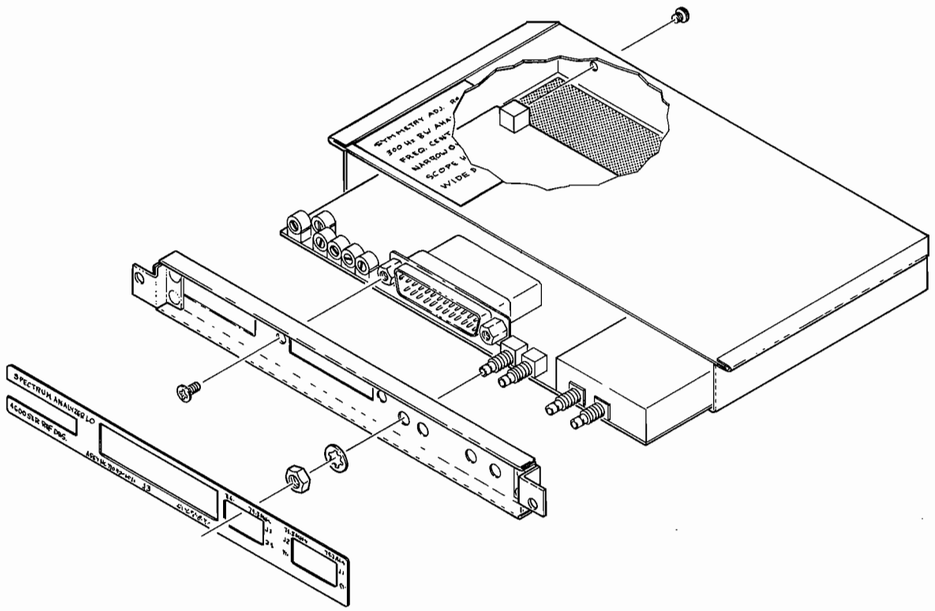


DETAIL **A**



DETAIL **B**





NOTES:

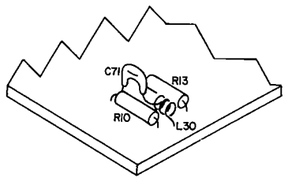
MECH ASSY

1. THE REF DES SERIES FOR SPECTRUM ANALYZER LO MECH ASSY IS 4600 (I.E., J1 IS J4601).
2. DATA PART NO. 7005-5043-500.
3. REF CIRCUIT SCHEMATIC 0000-5013-500.

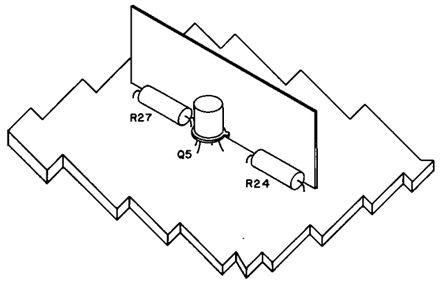
PC BOARD (1532 AND ON)

1. THE REF DES SERIES FOR SPECTRUM ANALYZER LO PC BOARD ASSY ARE 3500 AND 3600 (I.E., R1 IS R3501 AND R100 IS R3600).
2. DATA PART NO. 7010-5033-500.
3. REF CIRCUIT SCHEMATIC 0000-5013-500.
4. ATTACH INSULATOR TO INSIDE OF SHIELD.
5. SECURE L1 WITH RTV.
6. THRU SER. NO. 1939: CR13 NOT USED.

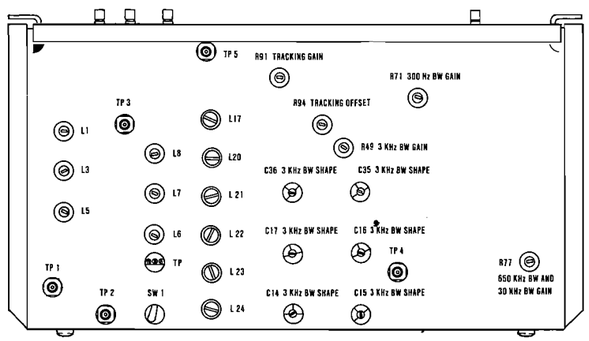
Figure 6-36 Spectrum Analyzer LO Module (Sheet 2 of 2) Eff. Ser. No. 1352 and On

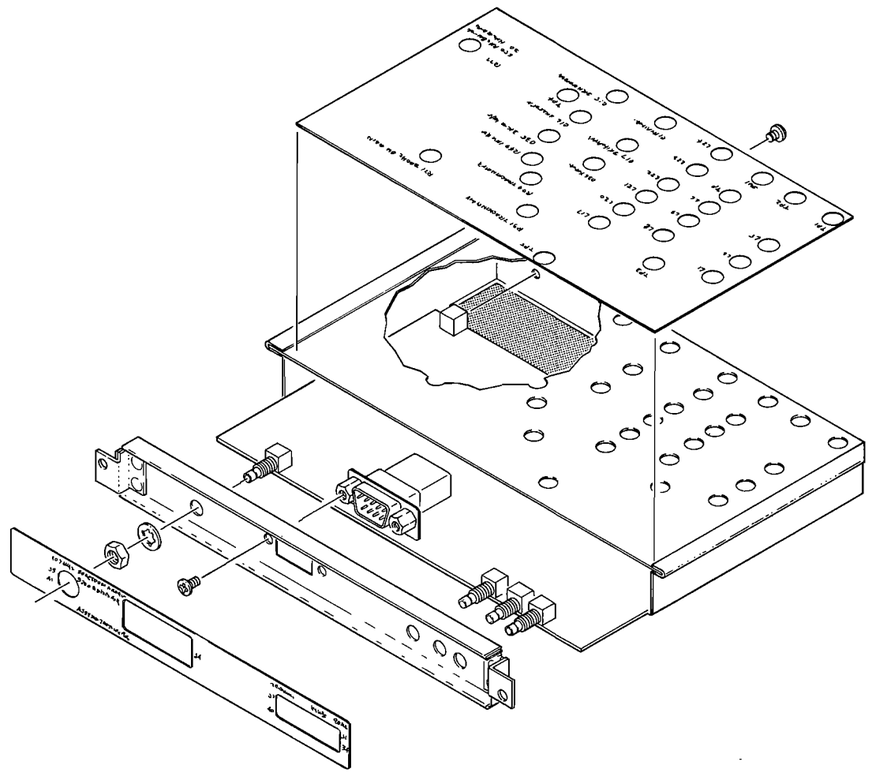


DETAIL **A**



DETAIL **B**





NOTES:

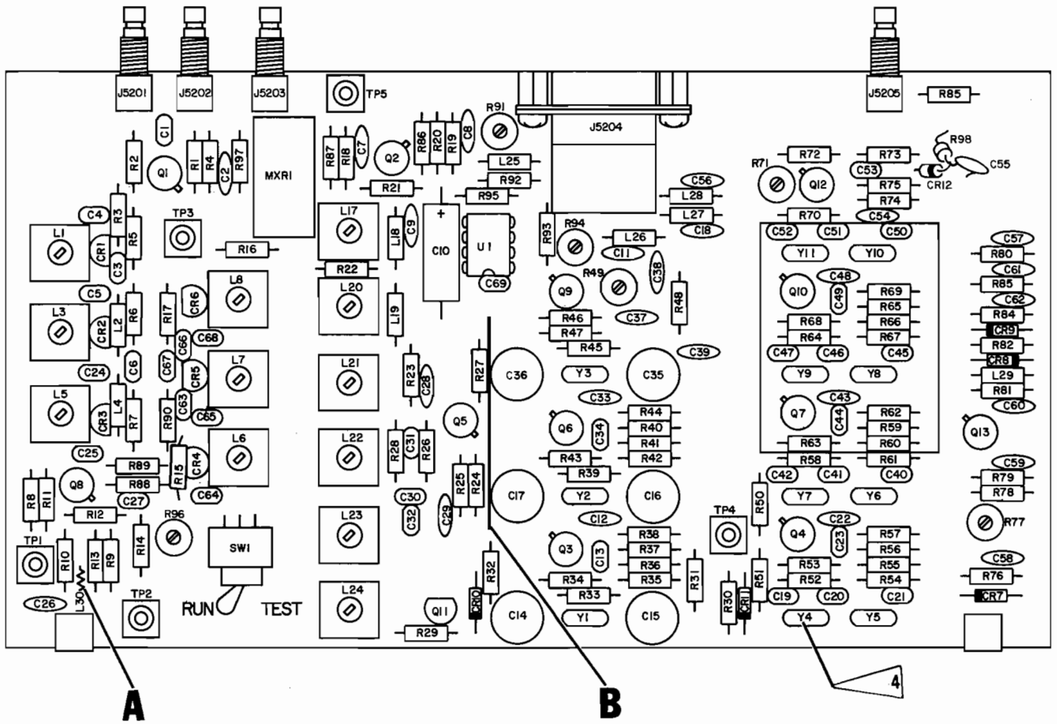
MECH ASSY

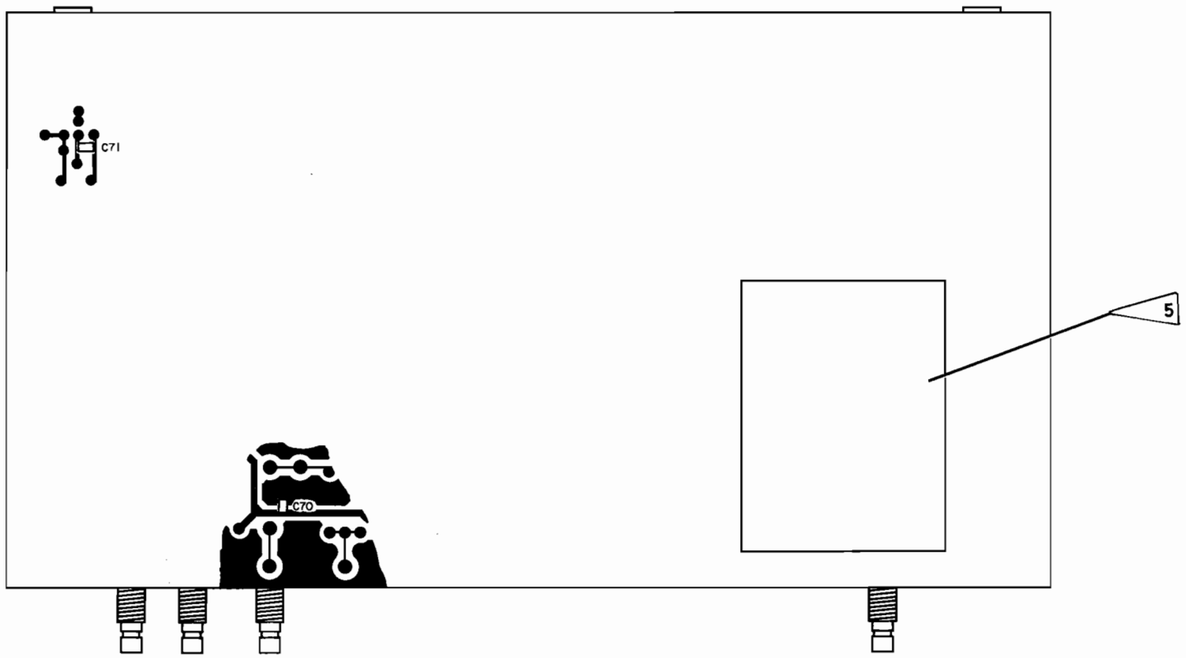
1. THE REF DES SERIES FOR SPECTRUM ANALYZER RF MCH ASSY IS 5200 (I.E., J1 IS J5201).
2. DATA PART NO. 7005-5043-700.
3. REF CIRCUIT SCHEMATIC 0000-5013-700.

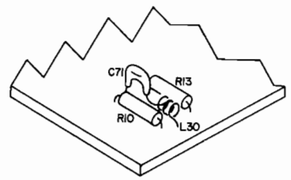
PC BOARD

1. THE REF DES SERIES FOR SPECTUM ANALYZER RF PC BOARD ASSY IS 3700 (I.E., R1 IS R3701).
2. DATA PART NO. 7010-5033-700.
3. REF CIRCUIT SCHEMATIC 0000-5013-700.
4. INSTALL INSULATOR UNDER Y4 THRU Y11.
5. ATTACH INSULATOR TO INSIDE OF SHIELD.

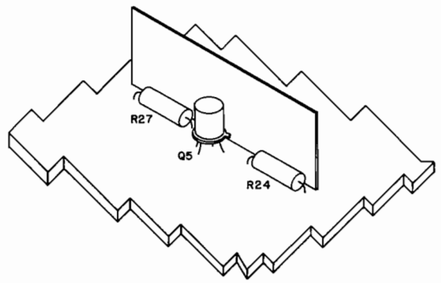
Figure 6-37 Spectrum Analyzer RF Module



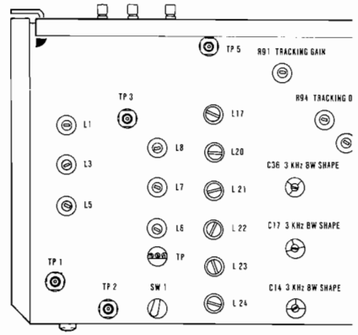


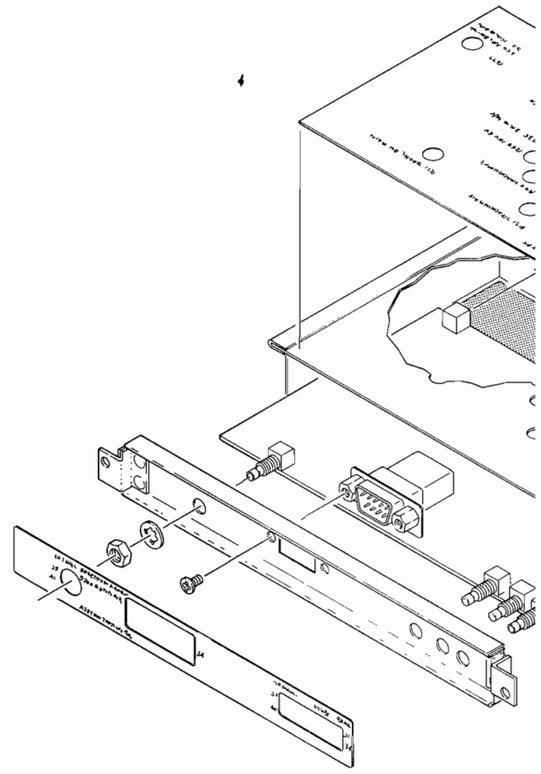


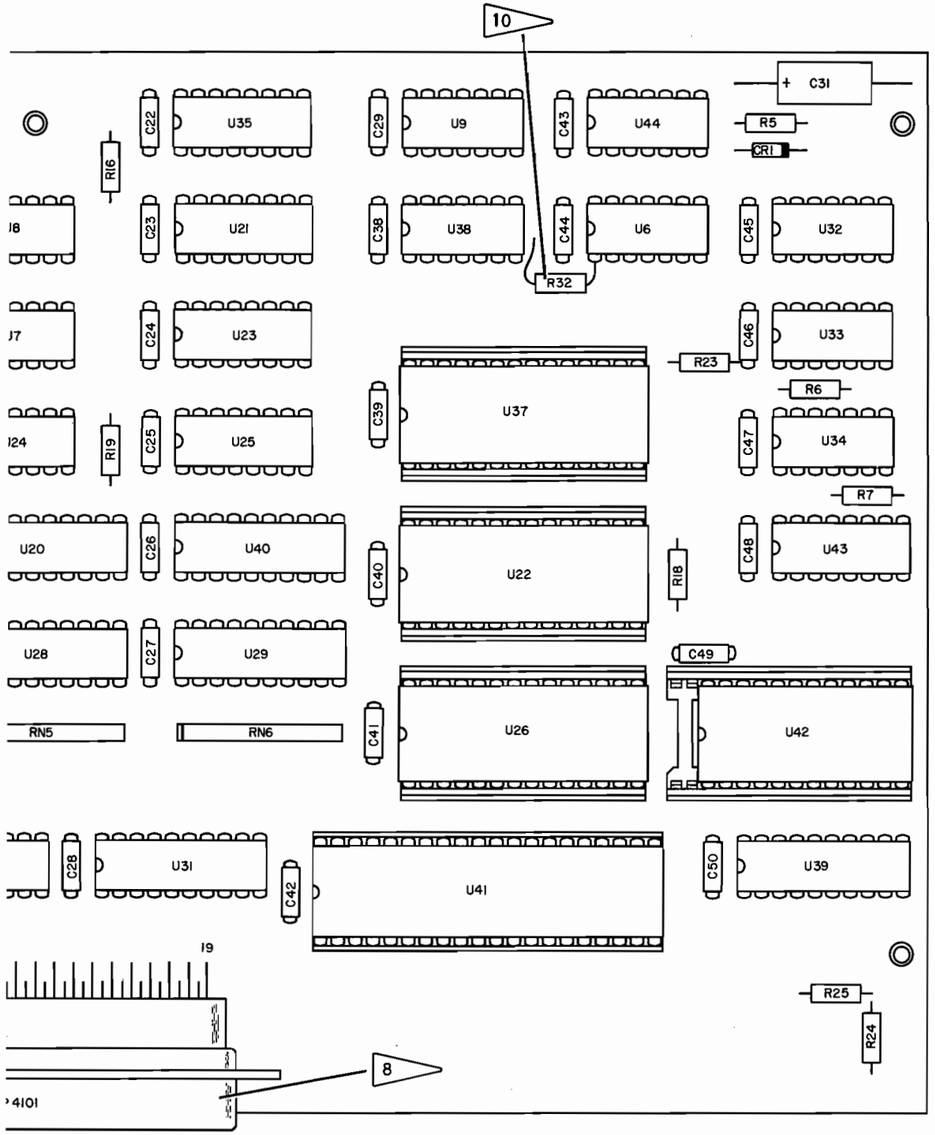
DETAIL **A**



DETAIL **B**

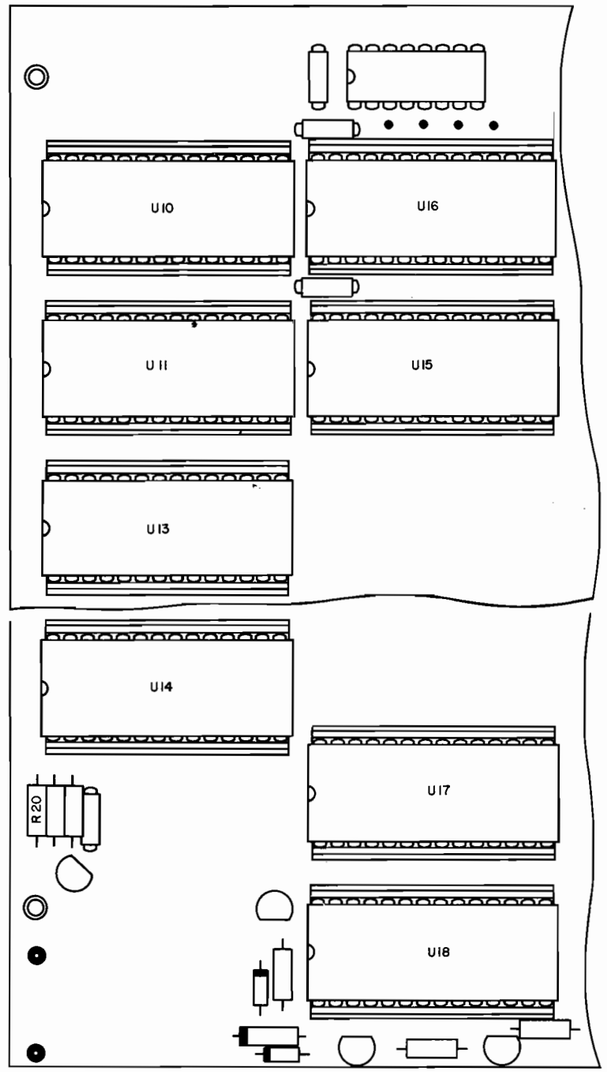




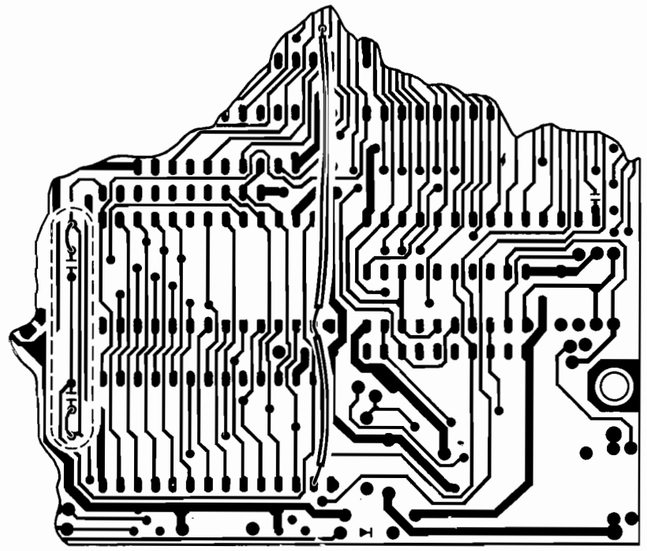


(THRU SER. NO. 2060)
(7010-5034-100-C3)

TOP VIEW



TOP VIEW



GPIB - CELLULAR OPTION (7010-5034-102)
THRU SER. NO. 2060

BOTTOM VIEW

6. CELLULAR VERSION IS EFFECTIVE FOR ALL SETS WITH THE CELLULAR OPTION AND DIFFERS FROM ILLUSTRATION SHOWN AS FOLLOWS:

   A. EPROMS U15 AND U16 ARE INSTALLED IN SOCKETS X1 AND X2.
   B. U17 AND U18 ARE 28-PIN IC's.
   C. JUMPERS AND CUT PATHS ON BOTTOM OF BOARD ARE SHOWN IN BOTTOM VIEW.

7. NOT USED.

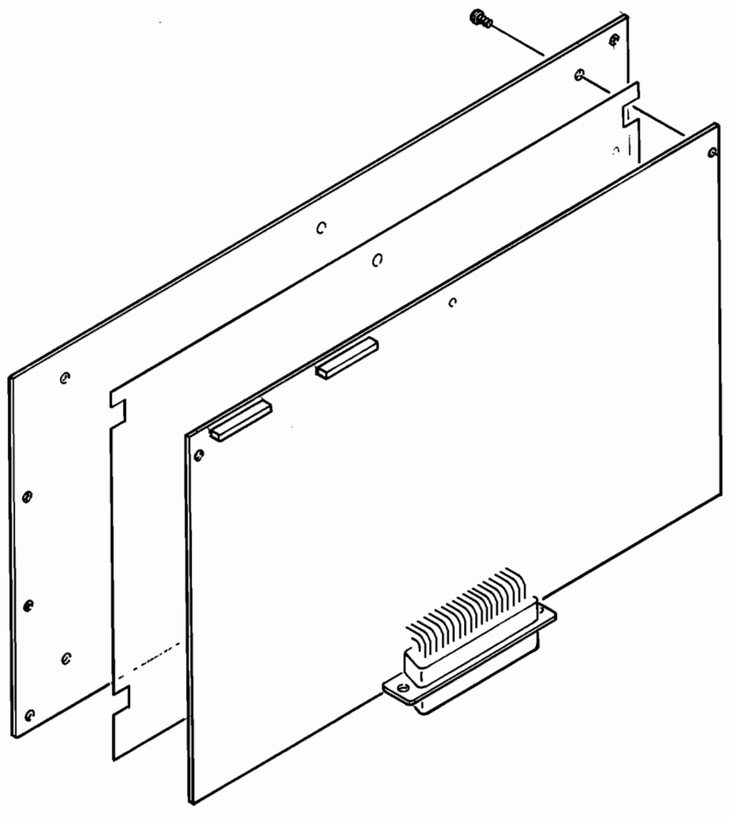
8. REMOVE MOUNTING BRACKET SUPPLIED WITH CONNECTOR BEFORE INSTALLATION TO KEEP IT FROM INTERFERING WITH C30.

9. EFFECTIVE THRU SER. NO. 1967, C51 THRU C53 NOT USED.

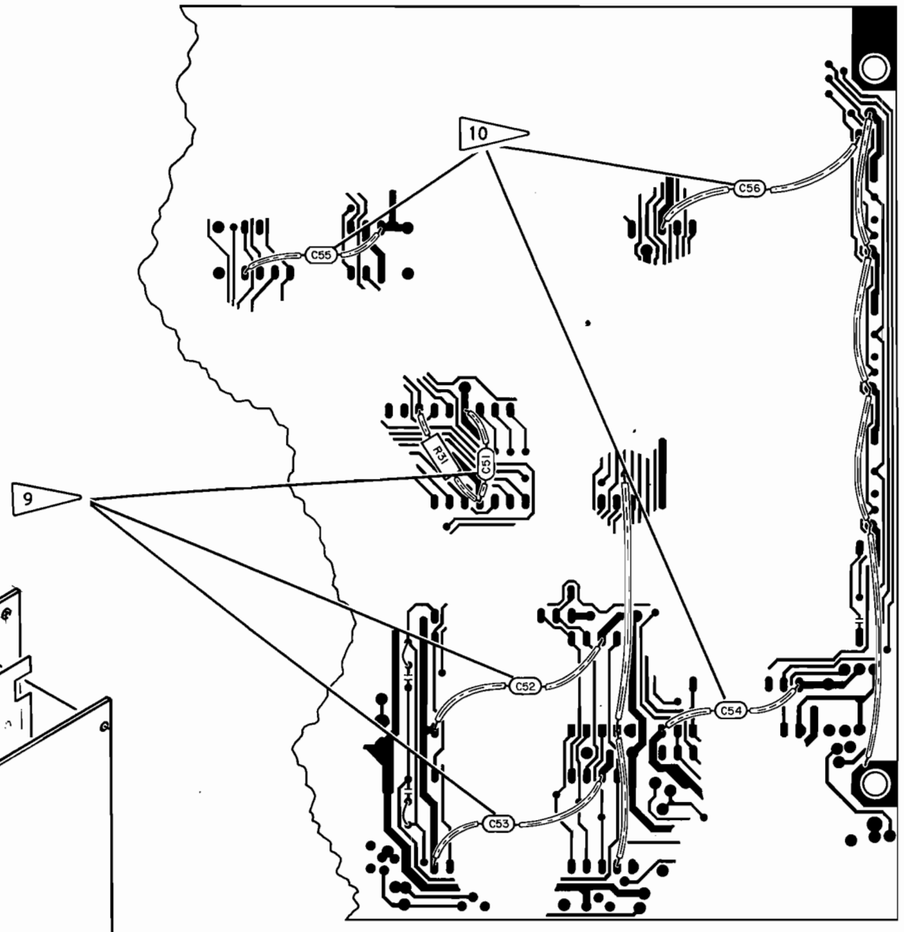
10. EFFECTIVE THRU SER. NO. 2001, C54 THRU C56, R31 AND R32 NOT USED. R1 AND R2 WERE 3.3 K.

11. EFFECTIVE THRU SER. NO. 1730, U17 AND U18 WERE 24-PIN IC'S INSTALLED IN 28-PIN SOCKETS. PIN 3 WAS PIN 1 OF THE 24-PIN IC'S.

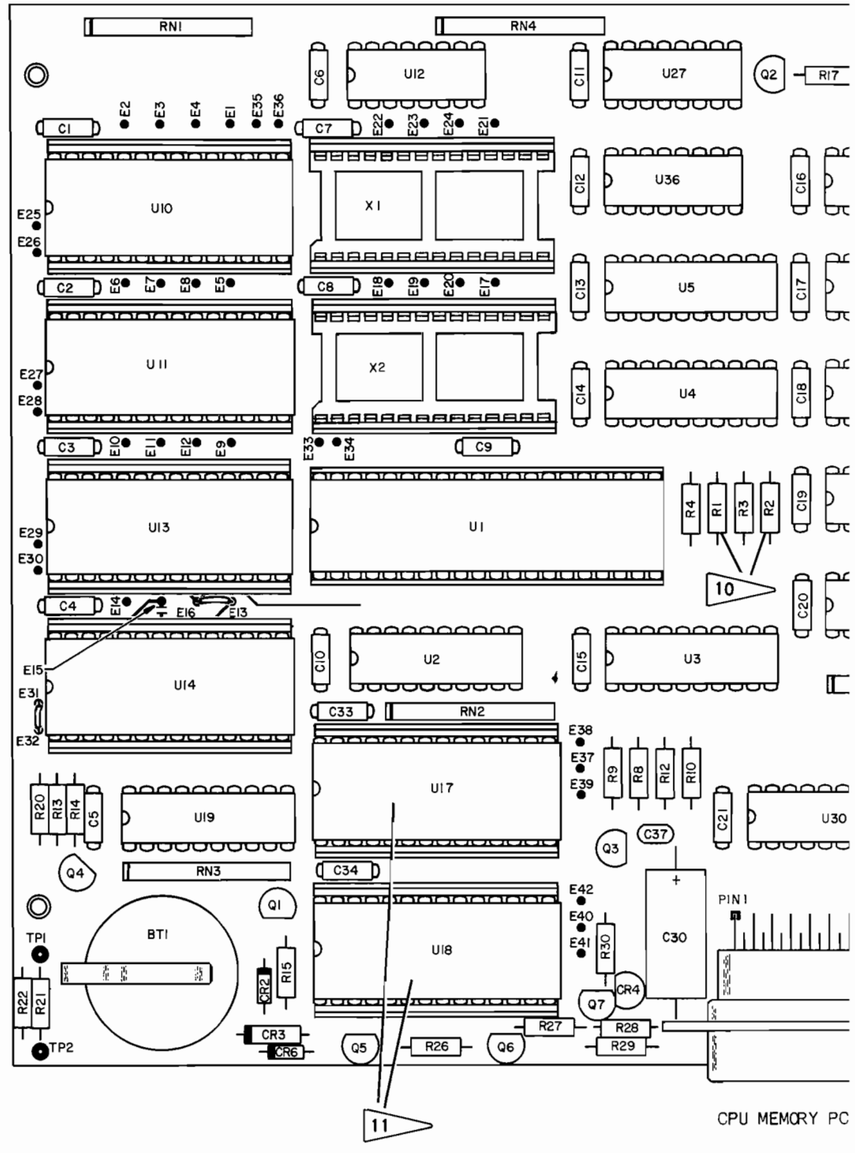
Figure 6-38 CPU/MEMORY PC Board (Sheet 1 of 2) (7010-5034-101-C5)



CPU MEMORY PC BD ASS'Y (THRU SER. NO. 2060)



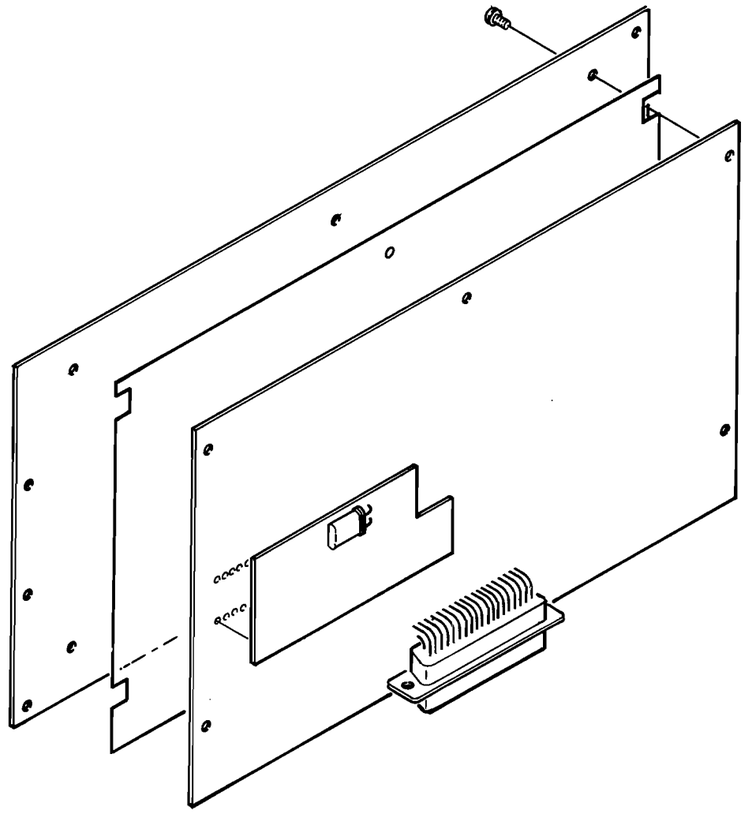
BOTTOM VIEW



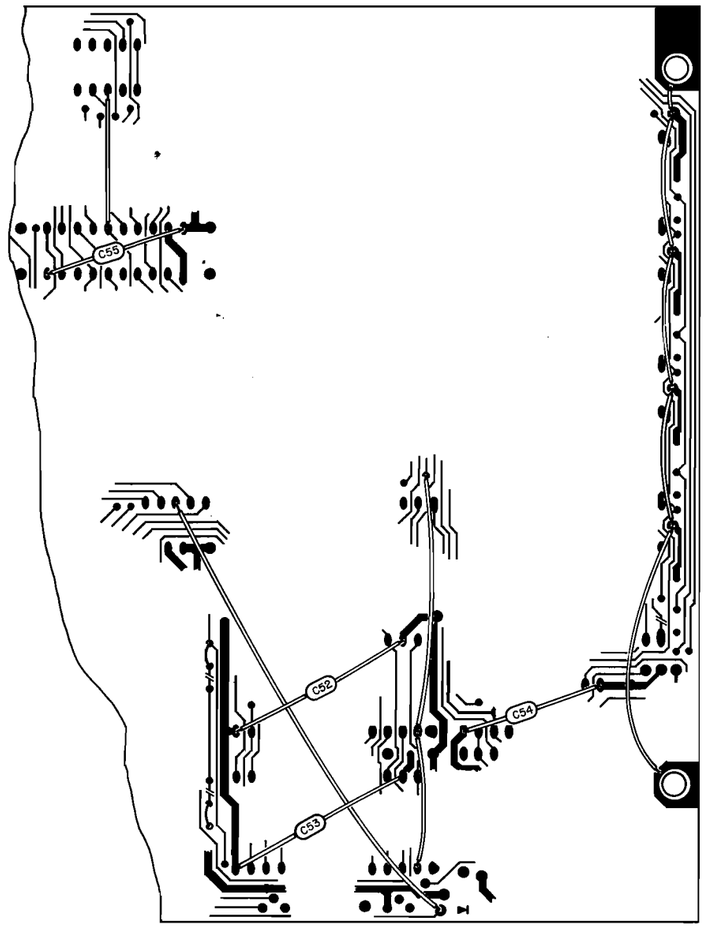
CPU MEMORY PC

NOTES:

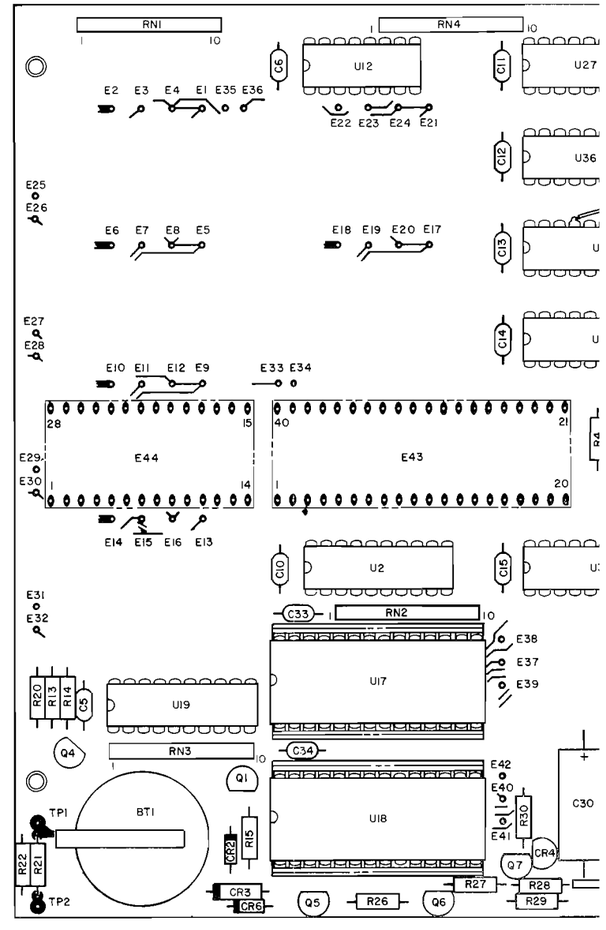
1. THE REF DES SERIES FOR CPU/MEMORY PC BD ASSY IS 4100 (I.E., J1 IS J4101).
2. DATA PART NO. FOR STANDARD VERSION IS 7010-5034-100; FOR GPIB VERSION IS 7010-5034-101; FOR CELLULAR VERSION IS 7010-5034-102.
3. REF CIRCUIT SCHEMATIC 0000-5014-101 WHICH HAS DETAILS FOR STANDARD AND CELLULAR VERSIONS.
4. STANDARD VERSION IS EFFECTIVE FOR NOS. 1005-1435 (APPROX.), AND DIFF FROM THE ILLUSTRATION SHOWN AS FOLLOWS:
   A. U15 IS NOT INSTALLED.
   B. JUMPERS FROM E31 TO E16 ARE NC INSTALLED.
   C. PATH-WORK TO E15 IS NOT CUT.
5. GPIB VERSION IS EFFECTIVE FOR ALL WITH GPIB OPTION FROM SER. NOS. 1C THRU 1435 AND IS THE GPIB/STANDARD VERSION FROM SER. NO. 1436 AND ON.

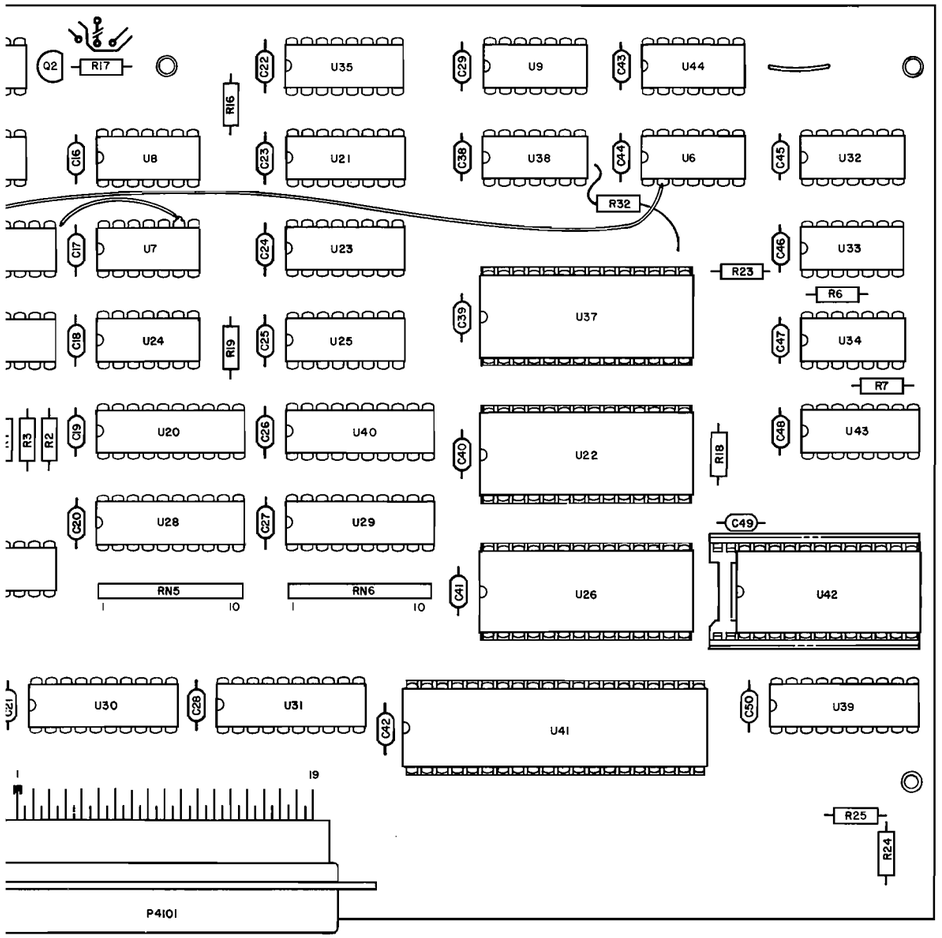


MECH ASSY - CPU PC BD
(SER. NO. 2061 AND ON)



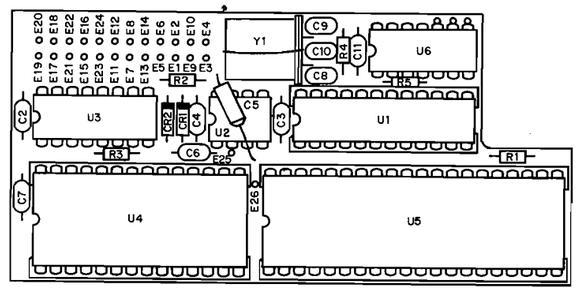
BOTTOM VIEW



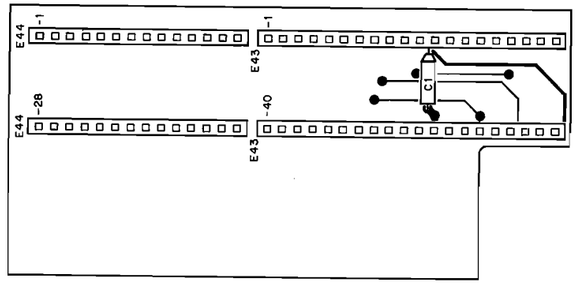


TOP VIEW

PC BD ASSY - CPU/MEMORY
(SER. NO. 2061 AND ON)



TOP VIEW



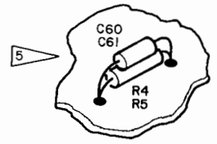
BOTTOM VIEW

Z80 WATCHDOG PC BD ASSY

NOTES:

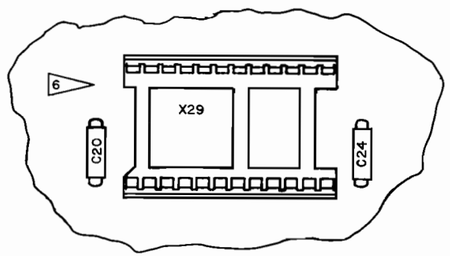
1. REF DES SERIES FOR THE CPU/MEMORY PC BD ASSY IS 4100 (I.E., R1 IS R4101).
2. DATA PART NO. IS 7010-5034-101
3. DATA PART NO. FOR Z80 WATCHDOG PC BD ASSY IS 7010-5038-500
4. REF CIRCUIT SCHEMATIC 0000-5014-100; FOR Z80 WATCHDOG SCHEMATIC, REF SCHEMATIC 0000-5018-500.
5. EFFECTIVE THRU SER. NO. 2626, U22, U26, U37 AND U41 WERE SOCKET MOUNTED. EFFECTIVE SER. NO. 2627 AND ON, U22, U26, U37 AND U41 ARE SURFACE MOUNTED PARTS.

Figure 6-38 CPU/MEMORY PC Board (Sheet 2 of 2)
(7010-5034-101-C5)
(Effective Ser. No. 2061 and On)



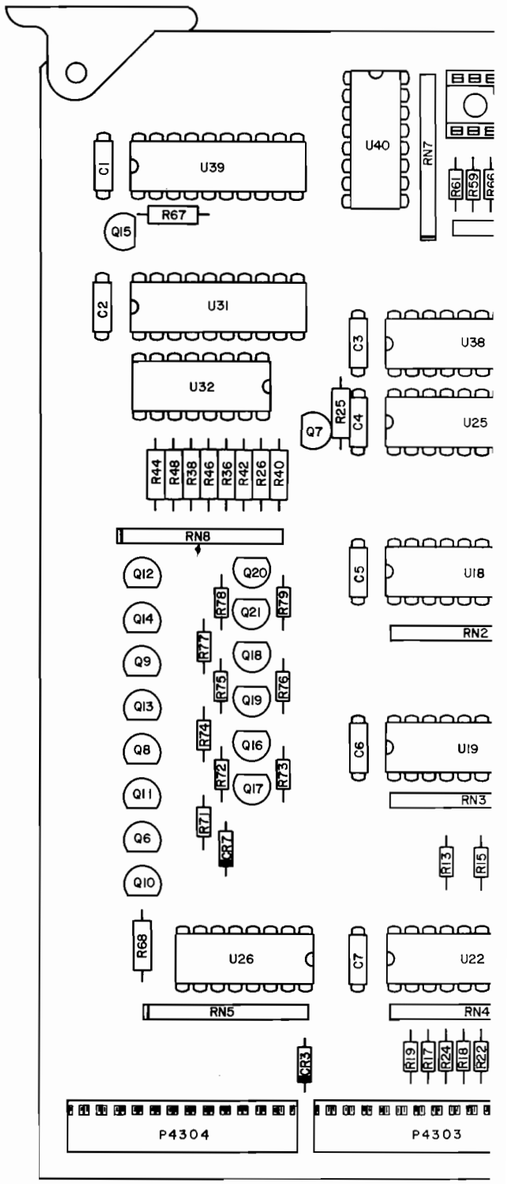
EFFECTIVE SER. NO. 2733 AND ON

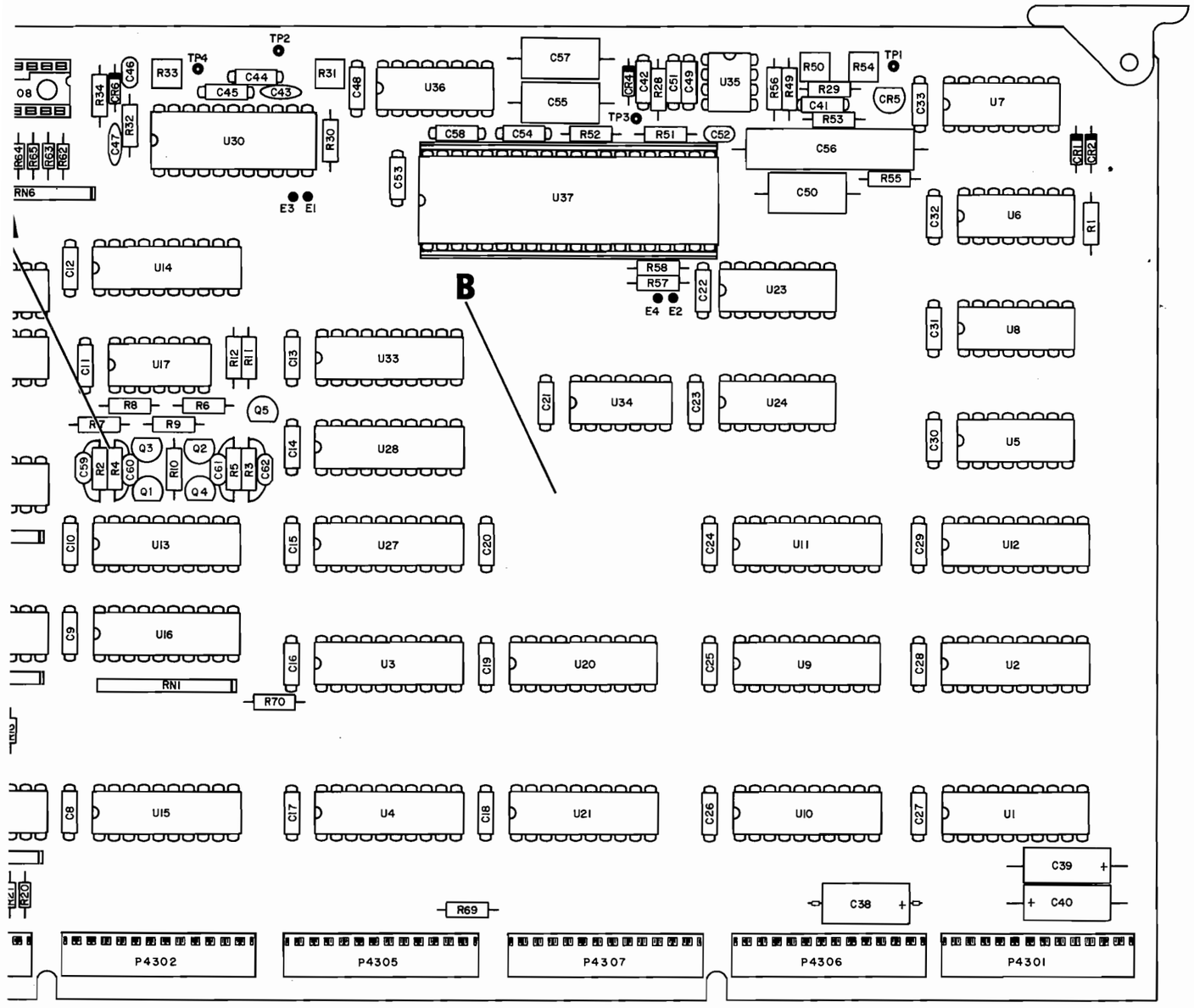
DETAIL **A**



EFFECTIVE THRU SER. NO. 2620

DETAIL **B**





NOTES:

1. THE REF DES SERIES FOR THE I/O PC BOARD IS 4300 (I.E., J1 IS J4301).
2. DATA PART NO. 7010-5034-300.
3. REF CIRCUIT SCHEMATIC 0000-5014-300.
4. THRU SER. NO. 2001, C59, C60, C61 AND C62 WERE NOT USED.
5. EFFECTIVE SER. NO. 2733 AND ON, C60 MOUNTS ON TOP OF R4 AND C61 MOUNTS ON TOP OF R5.
6. EFFECTIVE SER. NO. 2621 AND ON, X29 IS REMOVED.

Figure 6-39 I/O Interface PC Board

SECTION 7 - SCHEMATICS

7-1 GENERAL

This section contains circuit schematics and interconnect diagrams for the FM/AM-1500. Paragraph 7-3 is an index of these drawings.

NOTE

Drawings in this section reference schematic revision levels that are subject to change without notice.

7-2 HOW TO USE SCHEMATICS

To trace coaxial cables from one schematic to another, follow the procedures outlined in paragraph 7-2-1. To trace hard-wiring refer to paragraph 7-2-2.

7-2-1 COAXIAL CABLES

A. Locate desired module on FM/AM-1500 Interconnect (Figure 7-1, Sheet 2).

B. Locate desired coaxial cable on Interconnect. Coaxial connectors are identified both by a reference designator number (ref des) and by a two-digit number which corresponds to the number installed on the coaxial cable in the FM/AM-1500. The two-digit number is provided for quick tracing of coaxial cables. For example, coax number 38 is installed between J4001 on the Low Loop Module and J1802 on the Low Loop Mixer Module.

C. Locate schematic of desired module in index of circuit schematics.

D. Locate reference designator of coaxial connector on module schematic and continue tracing circuit.

7-2-2 MULTIPLE PIN CONNECTORS

A. Locate desired module on FM/AM-1500 Interconnect (Figure 7-1, Sheet 1) or on Wire Harness Schematic/Interconnect (Figure 7-2).

B. Locate desired multiple pin connector on applicable Interconnect. Note reference designator of the mating connector.

C. For module end of mating connector, locate schematic of desired module in index of circuit schematics and locate reference designator and pin number on circuit schematic. Continue tracing circuit.

D. For origination/destination end of mating connector, locate reference designator on Interconnect and note module to which connector is attached (most hard-wiring is routed through the Motherboard). Locate schematic of attached module in index and continue tracing circuits.

7-3 INDEX OF CIRCUIT SCHEMATICS AND INTERCONNECT DIAGRAMS

A B C D E F G H J K L

1 2 3 4 5 6 7

.05PPM OVEN OSCILLATOR (7400) — J7402 P7402 — 7001-5046-500

P/O 7007-5086-200

.2PPM TCXO (7000) — 7001-5086-800

FRONT PANEL (400) 7005-5040-500 (0000-5040-500) — J412 P412

P304 J304

J301 P301 6045-5085-600

FRONT PANEL (UPPER) (300) 7010-5030-300 (0000-5010-300)

J302 P302 6045-5085-700

J303 P303 6045-5085-800

FRONT PANEL (LOWER) (500) 7010-5030-500 (0000-5010-500)

J501 P501 6045-5086-000

J502 P502 6045-5086-100

LCD/KEYBOARD (100) 7010-5030-100 (0000-5010-100)

J101 P101 6045-5085-900

J102 P102

KEYPAD (200) 7010-5030-200 (0000-5010-200)

CRT V6401 — V6401-J1 — V6401-P1

P7401 J7401

IF GENERATOR (1200) 7005-5041-500 (0000-5011-500) — P1206 J1206

GENERATE/MIXER (4400) 7005-5043-400 (0000-5013-400) — J4404 P4404

1300MHz IF RCVR (1000) 7005-5041-400 (0000-5011-400) — P1007 J1007

OUTPUT AMP (800) 7005-5040-900 (0000-5010-900) — P805 J805

7007-5086-200 MAIN WIRE HARNESS (REF 0000-5017-500)

HI/LOW PASS FILTER (600) — FL601 — 7005-5040-700 (0000-5010-700)

BUFFER AMP A (6900A) — FL6901A — 7005-5046-801 (0000-5016-801)

L6401 165T 26GA.

BUFFER AMP B (6900B) — FL6901B — 7005-5046-801 (0000-5016-801)

J2408 P2408

DUAL VCO (2400) — 7005-5242-101 (0000-5012-101)

SP6401

POWER TERMINATION (9800) — 5. — 7005-5046-400 (0000-5018-400)

J9805 P9805

REAR PANEL (6000) — J6002

40V POWER SUPPLY (5600) — 7010-5035-600 (0000-5015-600)

J5601 P5601

POWER SUPPLY (6000) 7005-5045-700 (0000-5015-700) — J6001

J6002

6045-5086-900

P4308 J4308 — I/O INTERFACE (4300) 7010-5034-300 (0000-5014-300)

P4705 J4705 — DEMOD AUDIO (4700, 4800, 4900, & 5000) 7010-5038-900 (0000-5018-900) — 2.

CPU (4100) 7010-5034-101 (0000-5014-101) — P4101 J4101

DUAL TONE GENERATOR (4500) 7010-5034-500 (0000-5014-500) — P4501 J4501 P4502 J4502

P5320 J5320

P4301 J4301 P4302 J4302 P4303 J4303 P4304 J4304 P4305 J4305 P4306 J4306 P4307 J4307

P4701 J4701 P4702 J4702 P4703 J4703

CELLULAR OPTION (6500) — J6501 P6501

REFER TO SECTION 9 FOR OPTION INTERCONNECT

P5319 J5319 P5314 J5314 P5315 J5315 P5316 J5316 P5317 J5317 P5318 J5318 P5321 J5321 P5104 J5104

J5102 P5102 J5103 P5103 J5301 P5301 J5302 P5302 J5303 P5303 J5304 P5304 J5311 P5311 J5306 P5306 J5307 P5307 J5308 P5308 J5309 P5309 J5310 P5310 J5305 P5305 J5322 P5322

SCOPE CONTROL & DEFL 7010-5035-100 (5100 & 9500) (0000-5015-100)

6045-5083-100 6045-5083-000 6045-5083-400 6045-5082-900 6045-5083-300 6045-5083-200 6045-5082-800 6045-5083-500 6045-5083-800 6045-5083-700 6045-5083-600

MOTHERBOARD (5300) 7010-5035-300 (0000-5015-300)

P6003 J6003 J6004 P6004 — 6. — C6401 1000µF 16V — C6402 1000µF 16V — M B6401

J6005 P6005 — BATTERY 7001-5045-000

P1406 J1406 — CLOCK DIVIDER (1400) 7005-5041-700 (0000-5011-700)

P3202 J3202 — DUPLEX OFFSET (3200) 7005-5042-700 (0000-5012-700)

P4003 J4003 — LOW LOOP (4000) 7005-5043-100 (0000-5013-100)

P2803 J2803 — HIGH LOOP (2800) 7005-5042-300 (0000-5012-100 & 0000-5012-300)

P1805 J1805 — LOW LOOP MIXER (1800) 7005-5041-900 (0000-5011-900)

P3803 J3803 — 89-90MHz RCVR (3800) 7005-5042-900 (0000-5012-900)

P3003 J3003 — DELAY LINE (3000) 7005-5042-500 (0000-5012-400 & 0000-5012-600)

P4203 J4203 — FM GENERATOR (4200) 7005-5043-300 (0000-5013-300)

P5402 J5402 — SPEC ANALY. IF (5400) 7005-5043-900 (0000-5013-900)

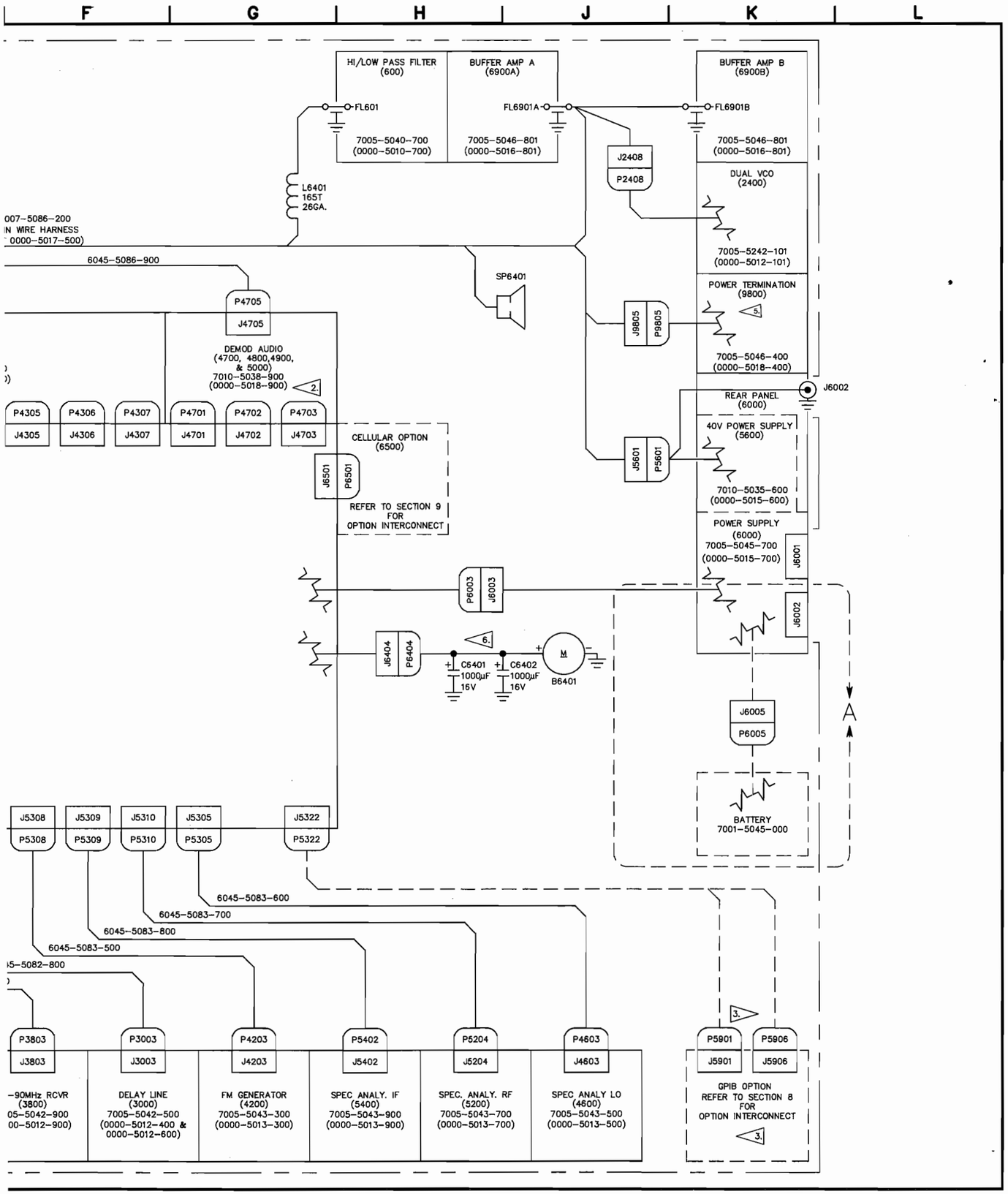
P5204 J5204 — SPEC. ANALY. RF (5200) 7005-5043-700 (0000-5013-700)

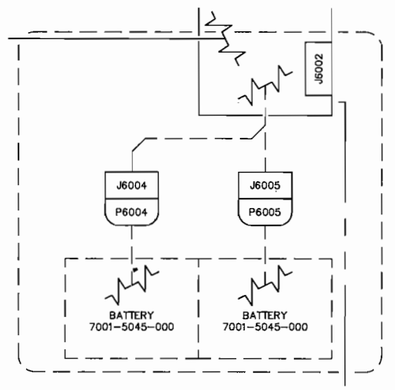
P4603 J4603 — SPEC ANALY LO (4600) 7005-5043-500 (0000-5013-500)

3. P5901 J5901 P5906 J5906 — GPIB OPTION REFER TO SECTION 8 FOR OPTION INTERCONNECT — 3.

A

FM/AM 1500 COMPOSITE (6400) SYTEM INTERCONNECT (CABLE)





EFFECTIVE THRU SER. NO. 2133

DETAIL **A**

NOTES:

1. ALL COAX SHIELDS ARE GROUNDED AT THE POINT OF TERMINATION.

2. APPLICABLE DEMOD AUDIO SCHEMATICS:
SER. NO. 2818 AND ON: 0000-5018-900
SER. NO. 1426 THRU 2817: 0000-5017-300
SER. NO. 1005 THRU 1425: 0000-5014-700.

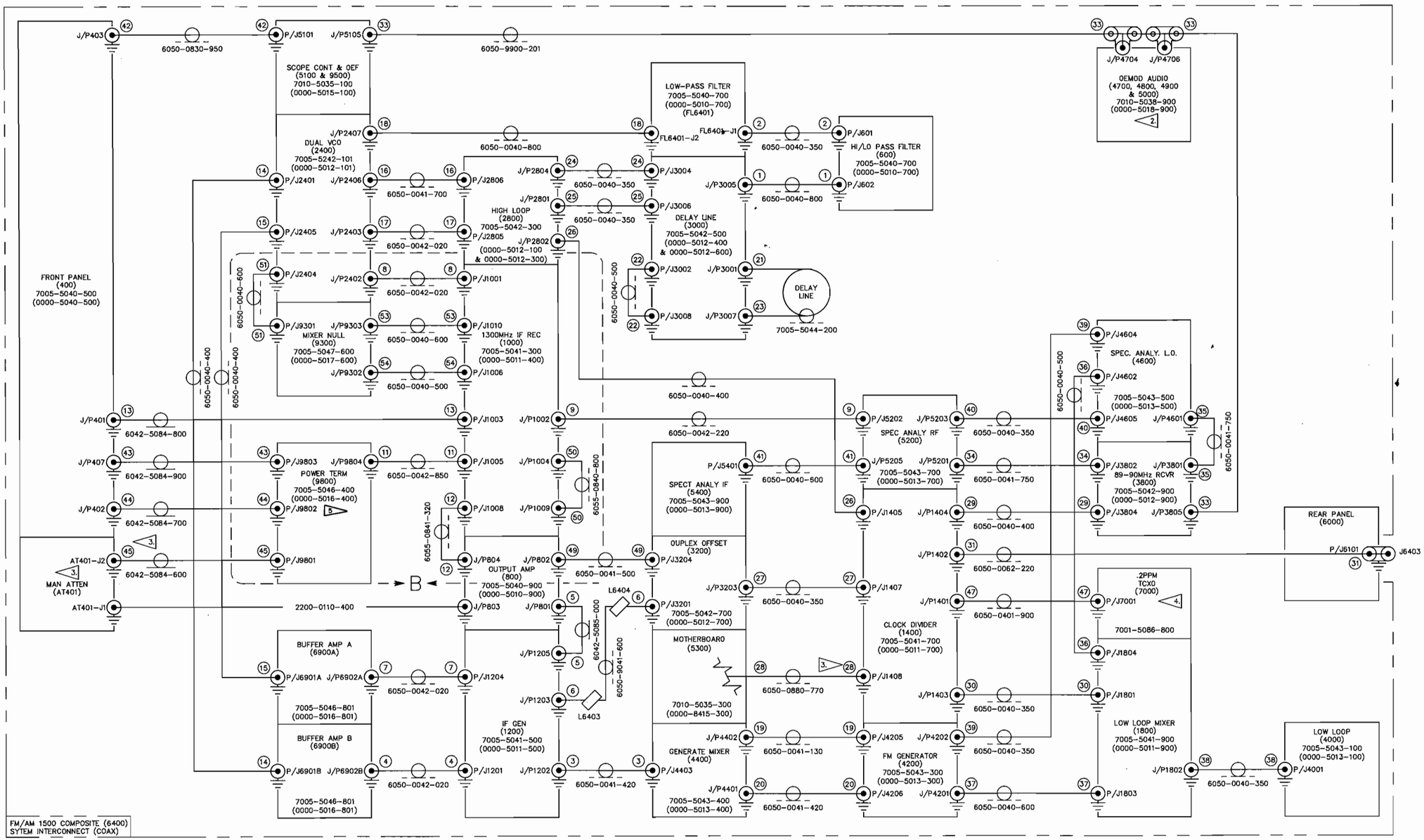
3. WHEN IEEE-488 INTERFACE OPTION (GPIB-- OPTION 1) IS NOT INSTALLED, P5906 IS MOUNTED TO THE REAR PANEL AT GPIB PORT AND P5901 IS NOT CONNECTED. WHEN IEEE-488 INTERFACE OPTION (GPIB--OPTION 1) IS INSTALLED, PROGRAMMABLE ATTENUATOR (AT 7501) REPLACES MANUAL ATTENUATOR (AT401), COAX #46 MATES DIRECTLY WITH COAX #45, TEE CONNECTOR MATES WITH J1408, P1408 BECOMES P1409.

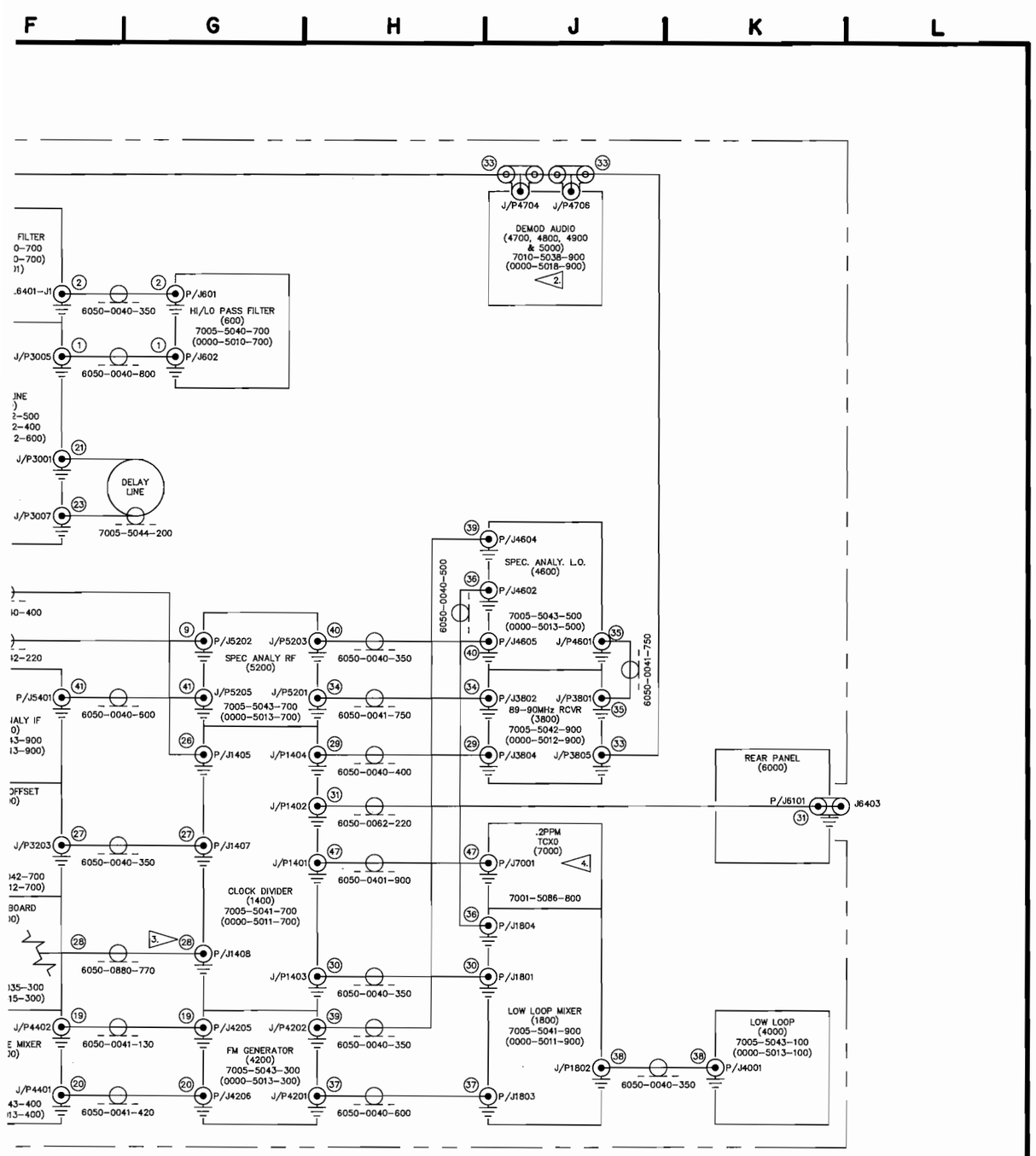
4. STANDARD OPTION IS .2PPM TCXO. OPTION INSTALLATION (OPTION 2) IS .05PPM OVEN OSCILLATOR.

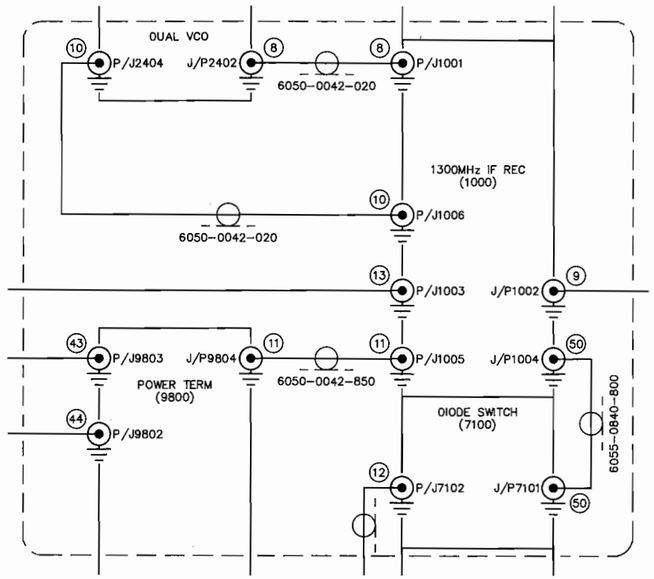
5. PRIOR TO SER. NO. 2134, POWER TERMINATION SCHEMATIC WAS 0000-5016-100 AND REF DES SERIES WAS 6200 (e.g., J9801 WAS J6200).

6. PRIOR TO SER. NO. 2134 LINE FEATURING P/J 6404, L6401 AND C6402 WAS NOT USED.

Figure 7-1 FM/AM 1500 Interconnect (Sheet 1 of 2) 0000-5017-400-D

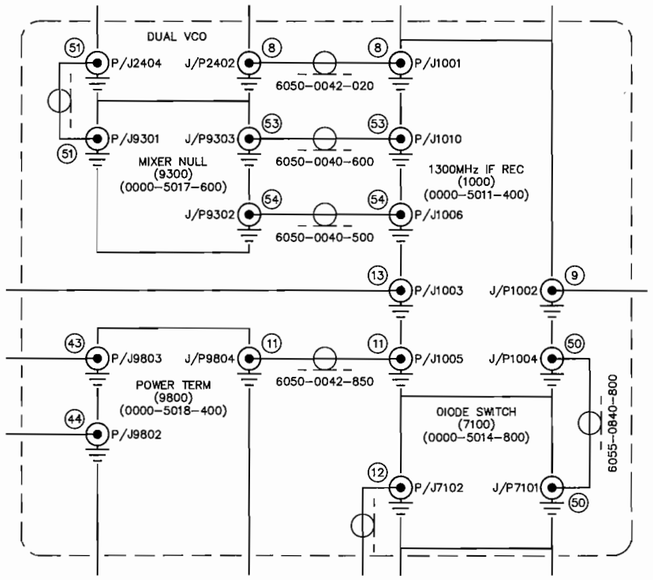

J/P403
6050-0830-950
P/J5101
J/P5105
6050-9900-201
SCOPE CONT & OEF
(5100 & 9500)
7010-5035-100
(0000-5015-100)
J/P4704
J/P4706
OEMOD AUDIO
(4700, 4800, 4900
& 5000)
7010-5038-900
(0000-5018-900)
LOW-PASS FILTER
7005-5040-700
(0000-5010-700)
(FL6401)
J/P2407
DUAL VCO
(2400)
7005-5242-101
(0000-5012-101)
6050-0040-800
FL6401-J2
FL6401-J1
6050-0040-350
P/J601
HI/LO PASS FILTER
(600)
7005-5040-700
(0000-5010-700)
P/J602
J/P3005
6050-0040-800
J/P2401
J/P2406
6050-0041-700
P/J2806
J/P2804
6050-0040-350
P/J3004
J/P2801
6050-0040-350
P/J3006
DELAY LINE
(3000)
7005-5042-500
(0000-5012-400
& 0000-5012-600)
HIGH LOOP
(2800)
7005-5042-300
J/P2405
J/P2403
6050-0042-020
P/J2805
J/P2802
(0000-5012-100
& 0000-5012-300)
FRONT PANEL
(400)
7005-5040-500
(0000-5040-500)
P/J2404
J/P2402
6050-0042-020
P/J1001
P/J3002
J/P3001
DELAY
LINE
P/J3008
J/P3007
7005-5044-200
6050-0040-600
6050-0040-500
P/J9301
J/P9303
MIXER NULL
(9300)
7005-5047-600
(0000-5017-600)
6050-0040-600
P/J1010
1300MHz IF REC
(1000)
7005-5041-300
(0000-5011-400)
J/P9302
6050-0040-500
P/J1006
6050-0040-400
6050-0040-400
6050-0040-400
J/P401
6042-5084-800
P/J1003
J/P1002
P/J5202
J/P5203
SPEC ANALY RF
(5200)
6050-0040-350
P/J4604
SPEC. ANALY. L.O.
(4600)
P/J4602
7005-5043-500
(0000-5013-500)
6050-0040-500
6050-0041-750
J/P407
6042-5084-900
P/J9803
J/P9804
6050-0042-850
P/J1005
J/P1004
6055-0840-800
POWER TERM
(9800)
7005-5046-400
(0000-5016-400)
P/J9802
P/J5401
6050-0040-600
SPECT ANALY IF
(5400)
7005-5043-900
(0000-5013-900)
P/J5205
J/P5201
7005-5043-700
(0000-5013-700)
6050-0041-750
P/J4605
J/P4601
P/J3802
J/P3801
89-90MHz RCVR
(3800)
7005-5042-900
(0000-5012-900)
J/P402
6042-5084-700
P/J1008
J/P1009
6055-0841-320
P/J1405
J/P1404
6050-0040-400
P/J3804
J/P3805
REAR PANEL
(6000)
P/J6101
J6403
AT401-J2
6042-5084-600
MAN ATTEN
(AT401)
AT401-J1
2200-0110-400
J/P804
J/P802
6050-0041-500
OUTPUT AMP
(800)
7005-5040-900
(0000-5010-900)
P/J3204
OUPLEX OFFSET
(3200)
J/P1402
6050-0062-220
J/P3203
6050-0040-350
P/J1407
J/P1401
6050-0401-900
.2PPM
TCXO
(7000)
P/J7001
7001-5086-800
P/J1804
B
L6404
J/P801
J/P803
P/J3201
7005-5042-700
(0000-5012-700)
MOTHERBOARD
(5300)
CLOCK DIVIDER
(1400)
7005-5041-700
(0000-5011-700)
BUFFER AMP A
(6900A)
J/P1205
6042-5085-000
6050-9041-600
P/J6901A
J/P6902A
6050-0042-020
P/J1204
J/P1203
L6403
7005-5046-801
(0000-5016-801)
6050-0880-770
P/J1408
J/P1403
6050-0040-350
P/J1801
7010-5035-300
(0000-8415-300)
BUFFER AMP B
(6900B)
IF GEN
(1200)
7005-5041-500
(0000-5011-500)
J/P4402
6050-0041-130
P/J4205
J/P4202
6050-0040-350
LOW LOOP MIXER
(1800)
7005-5041-900
(0000-5011-900)
GENERATE MIXER
(4400)
FM GENERATOR
(4200)
7005-5043-300
(0000-5013-300)
P/J6901B
J/P6902B
6050-0042-020
P/J1201
J/P1202
6050-0041-420
P/J4403
J/P4401
7005-5043-400
(0000-5013-400)
6050-0041-420
P/J4206
J/P4201
6050-0040-600
P/J1803
J/P1802
6050-0040-350
P/J4001
LOW LOOP
(4000)
7005-5043-100
(0000-5013-100)
FM/AM 1500 COMPOSITE (6400)
SYTEM INTERCONNECT (COAX)





EFFECTIVE SER. NO. 1005 THRU SER. NO. 1234

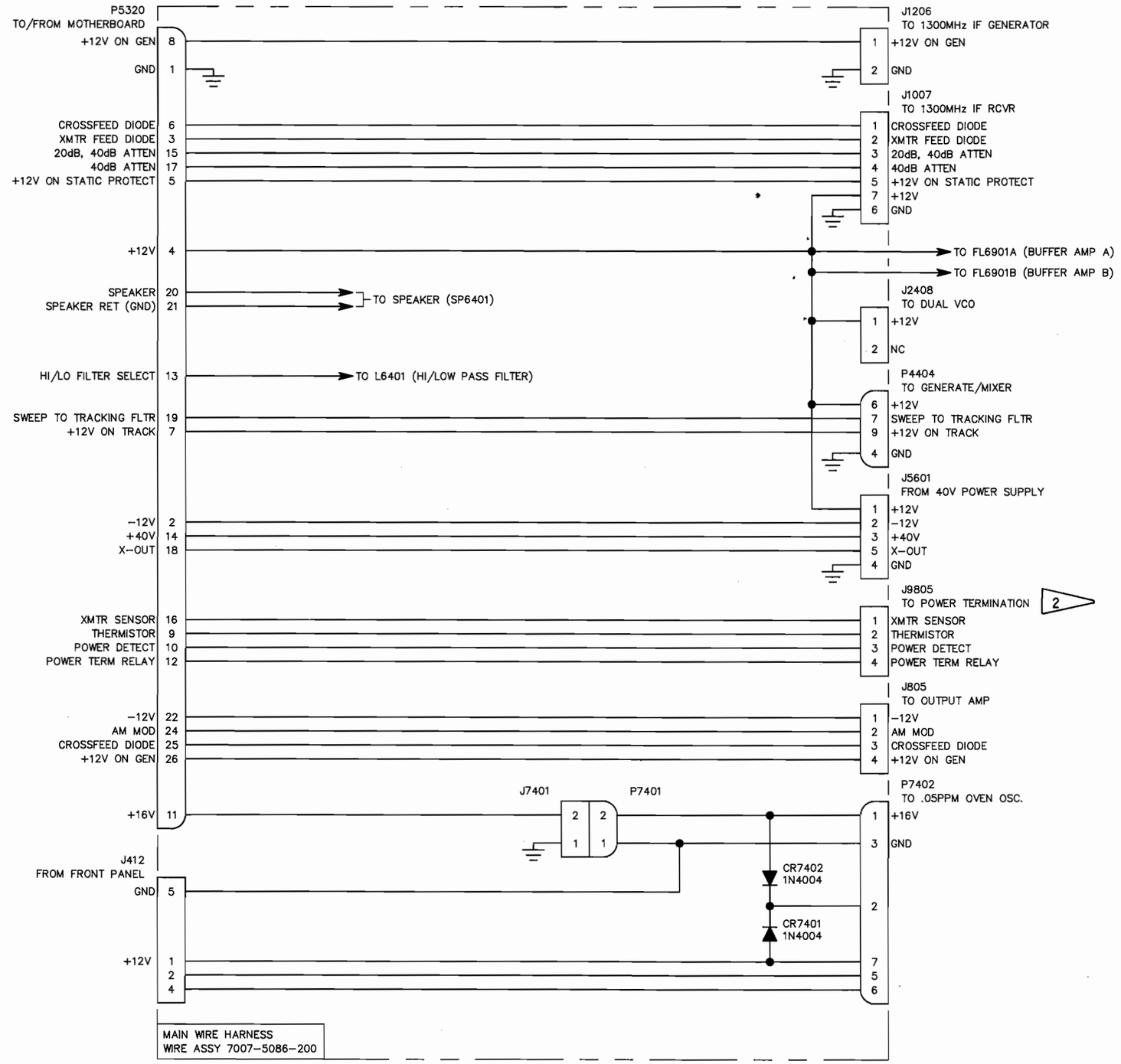
DETAIL **B**



EFFECTIVE SER. NO. 1235 THRU SER. NO. 1406

DETAIL **B**

Figure 7-1 FM/AM-1500 Interconnect (Sheet 2 of 2)
0000-5017-400-D

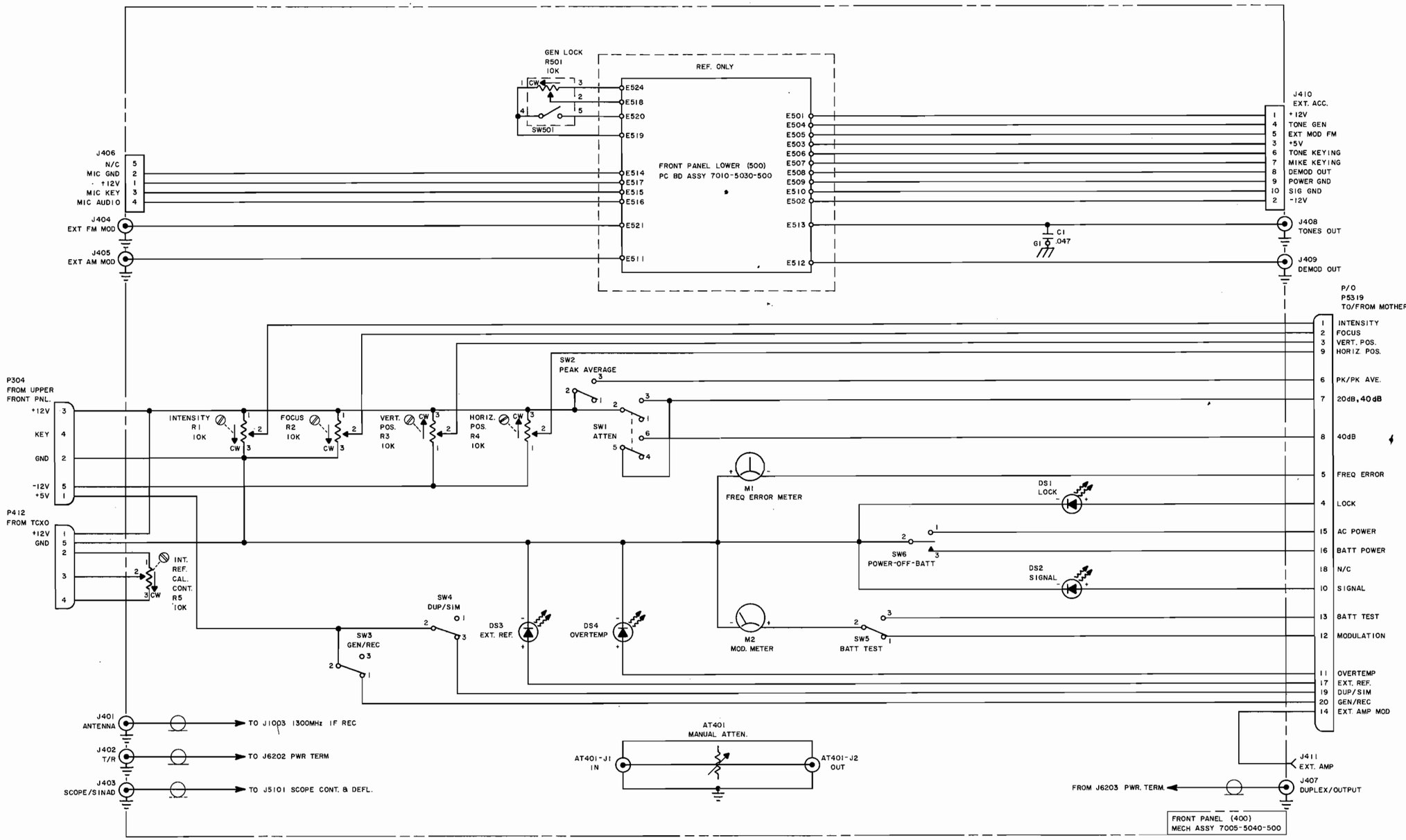


NOTES:

1. THIS DRAWING TAKES PRECEDENCE OVER ANY EXISTING LABELS INSTALLED IN THE FM/AM-1500.

2. THRU SER. NO. 1993, REF DES SERIES FOR THE POWER TERMINATION MODULE WAS 6200; SER. NO. 1994 AND ON, REF DES SERIES IS 9800 (E.G., J9805 WAS J6205).

Figure 7-2 Wire Harness Schematic Interconnect 0000-5017-500-D



STANDARDS:
(UNLESS OTHERWISE NOTED)

1. ALL REF NOS CARRY AN ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES:

   A. MECH - (400) E.G., SW1 IS SW401

2. ALL RESISTANCE IS EXPRESSED IN OHMS.

3. ALL CAPACITANCE IS EXPRESSED IN MICRO-FARADS.

NOTES:

1. LAST REF NOS USED:
   J11, DS4, C1, M2, R5, SW6, R501, AT401.

Figure 7-3 Front Panel Schematic
0000-5040-500-T

STANDARDS:
(UNLESS OTHERWISE NOTED)

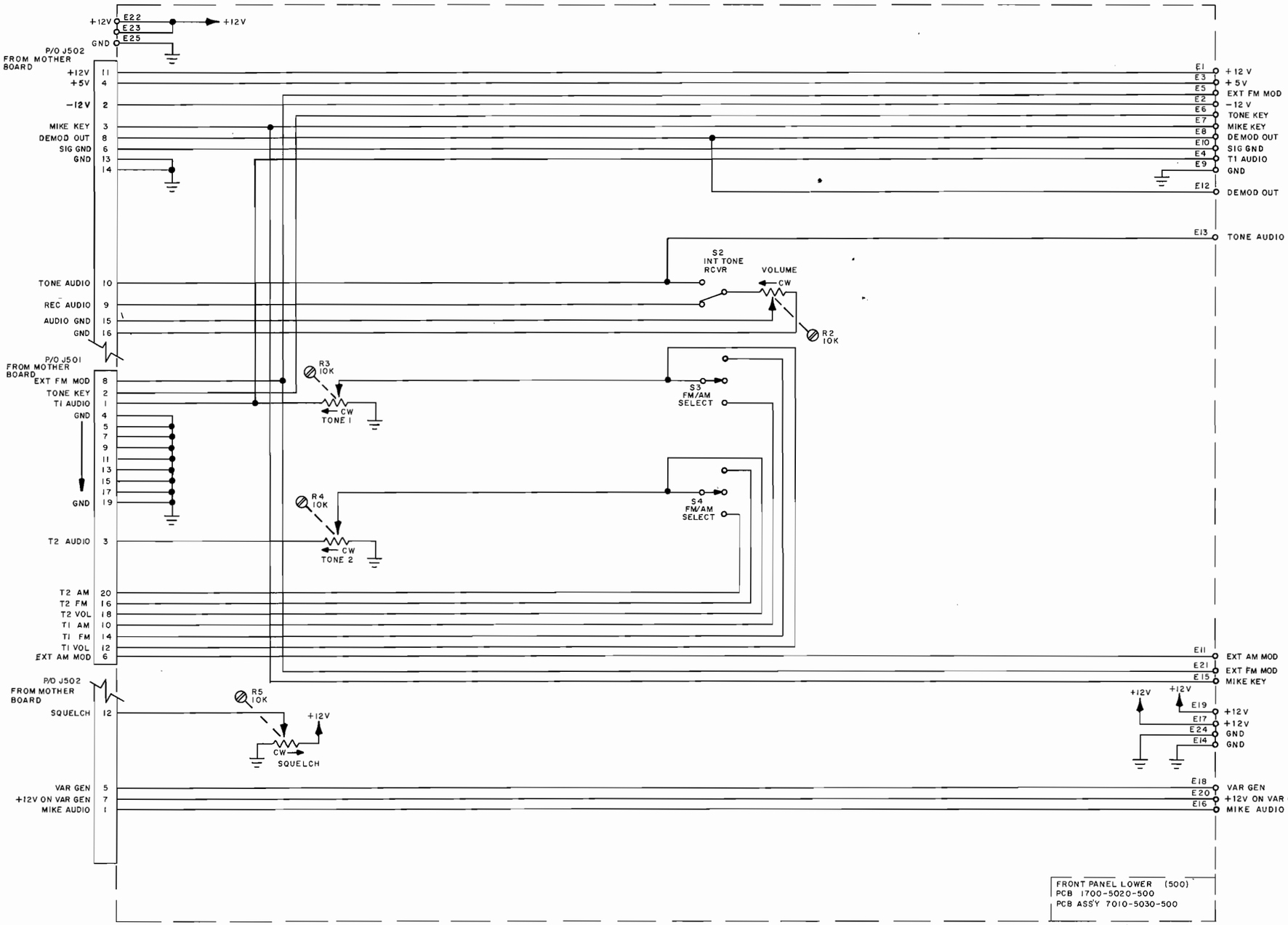
1. ALL REF NOS CARRY AN ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES 300 (I.E., R1 IS R301).
2. ALL RESISTORS ARE 1/4 W, 10%.
3. ALL RESISTANCE IS EXPRESSED IN OHMS.

NOTES:

1. LAST REF NOS USED: J4, CR64, C59, R8, S9
2. REF NOS NOT USED: CR29

UPPER FRONT PANEL ASSY (300)
PC BD 1700-5020-300
PC BD ASSY 7010-5030-300

Figure 7-4 Upper Front Panel PC Board Schematic 0000-5010-300-D



STANDARDS:
(UNLESS OTHERWISE NOTED)

1. ALL REF NOS CARRY AN ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES: 500 (E.G., R1 IS R501, ETC.).

   A. MECH ASSY.
   B. PCB ASSY 7010-5030-500

2. ALL RESISTORS ARE 1/4 W, ±5% TOLERANCE.
3. ALL RESISTANCE IS EXPRESSED IN OHMS.
4. ALL CAPACITANCE IS EXPRESSED IN MICROFARADS.
5. ALL INDUCTANCE IS EXPRESSED IN MICROHENRYS.

NOTES:

1. LAST REF NOS USED:
   R5, J502, E25, S4

Figure 7-5 Lower Front Panel PC Board Schematic 0000-5010-500-D

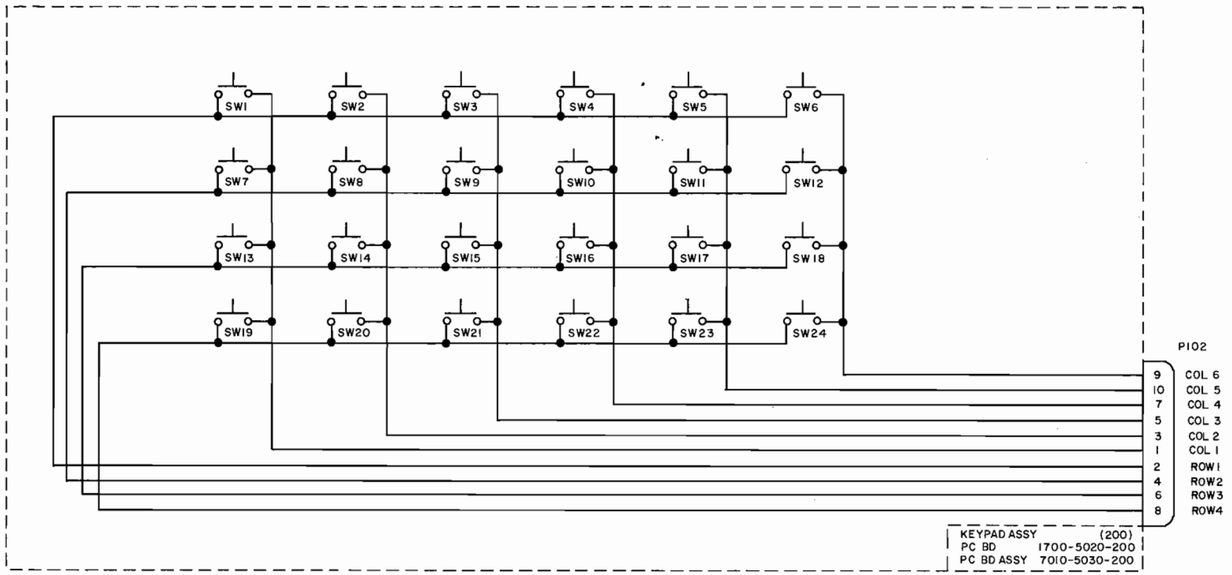
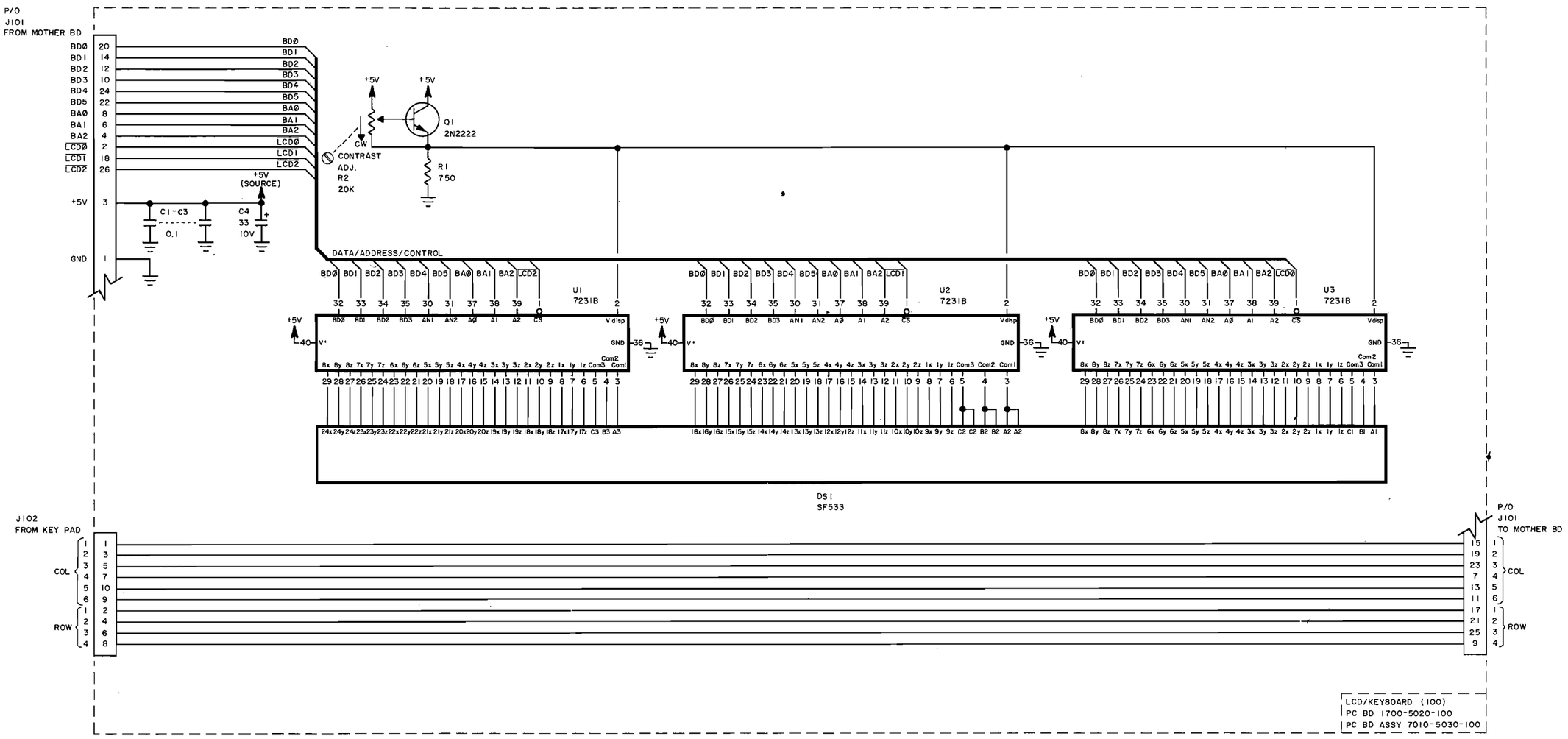


Figure 7-6 Keypad Schematic
0000-5010-200-B1



STANDARDS:
(UNLESS OTHERWISE NOTED)

1. ALL REF NOS CARRY AN ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES:

   A. MECH
   B. PC BD - 100 (E.G., R1 IS R101)

2. ALL RESISTORS ARE 1/4 W, 1% TOLERANCE.

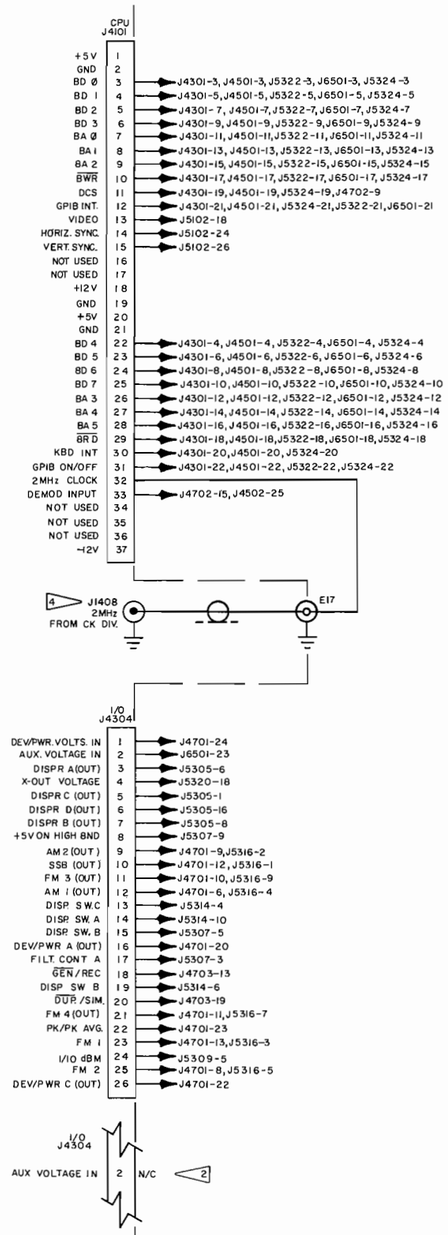
3. ALL RESISTANCE IS EXPRESSED IN OHMS.

4. ALL CAPACITANCE IS EXPRESSED IN MICRO-FARADS.

NOTES:

1. LAST REF NOS USED:
   J102, DS1, Q1, U3, C4, R2

Figure 7-7 LCD/Keyboard Schematic 0000-5010-100-D



STANDARDS:
(UNLESS OTHERWISE NOTED)

1. ALL REF NOS CARRY AN ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES: E5300 (E.G., E1 IS E5301, ETC).

NOTES:

1. LAST REF NOS USED:
   J4307, J4101, J4502, J4703, J5324, J6501
   J5103.

2. FOR BOARDS CONFORMING TO GPIB REQUIREMENTS (NOTED FOR REF ONLY).

3. FOR BOARDS CONFORMING TO CELLULAR OPT 8 REQUIREMENTS ONLY.

4. WHEN GPIB OPTION IS INSTALLED, J1408 BECOMES J1409.

Figure 7-8 Motherboard Schematic
(Sheet 1 of 5)
0000-5015-300-H4

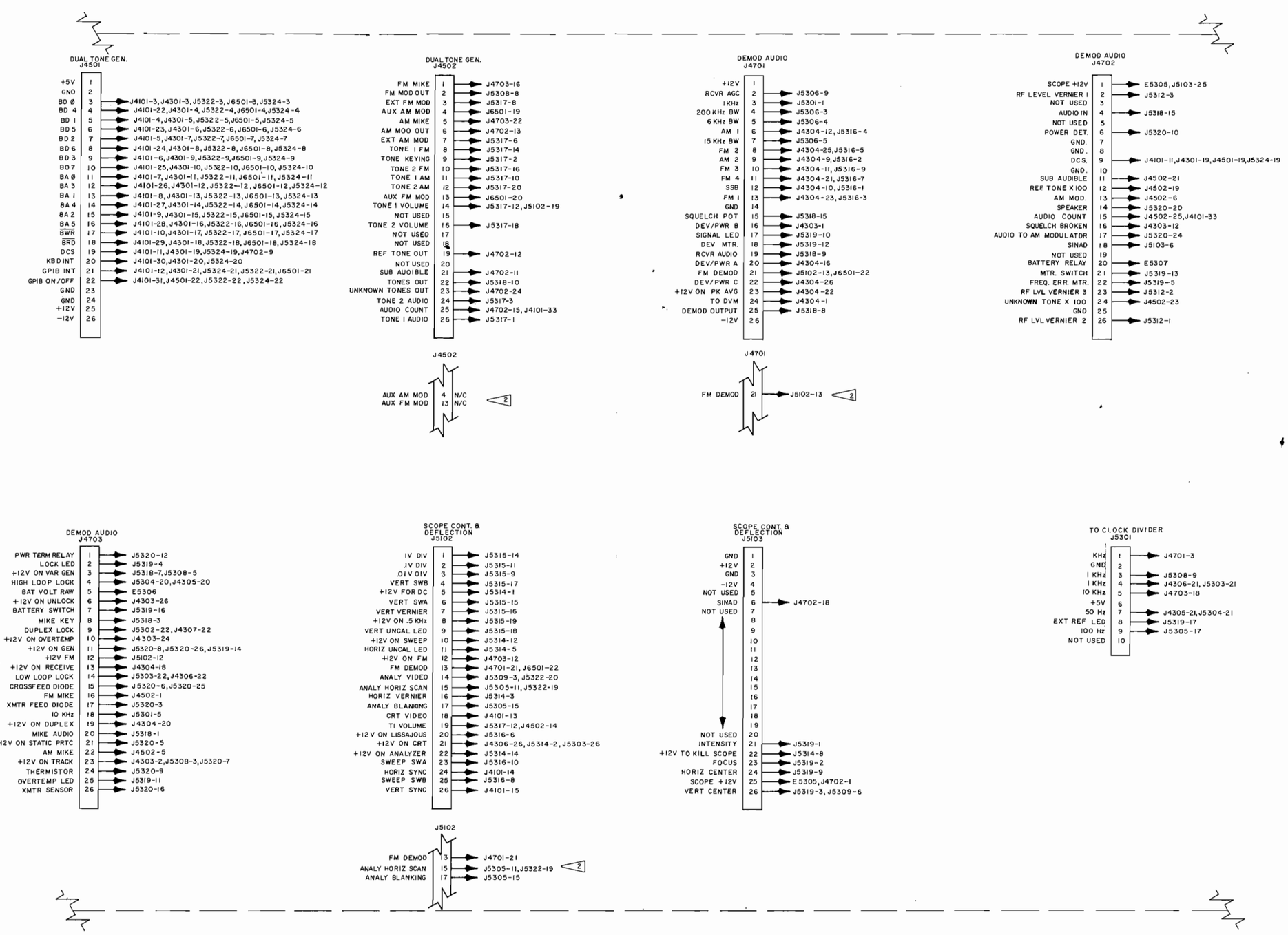


Figure 7-8 Motherboard Schematic (Sheet 2 of 5) 0000-5015-300-H4

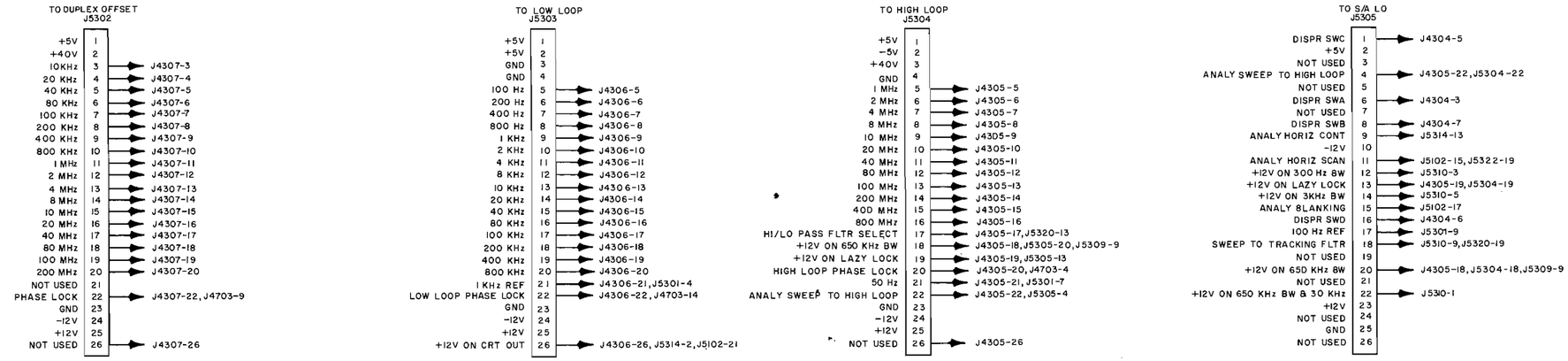
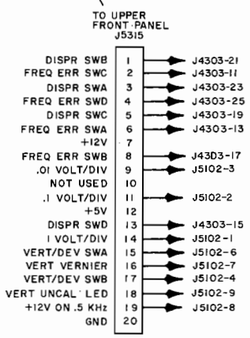
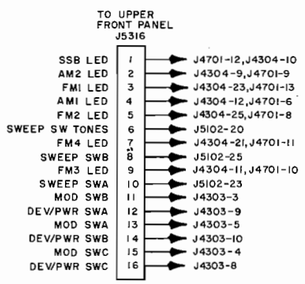
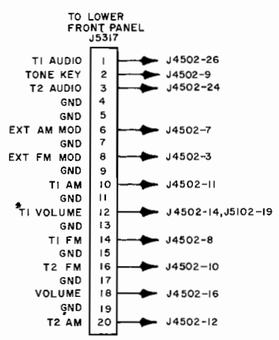
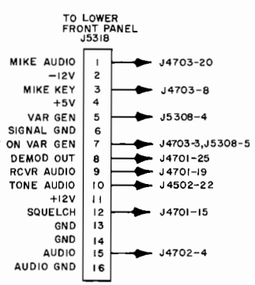


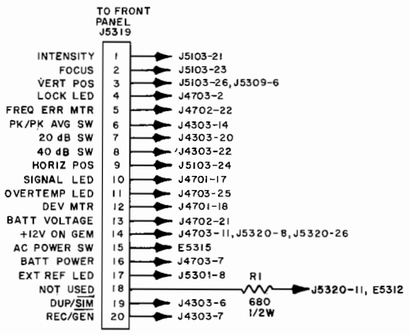
Figure 7-8 Motherboard Schematic (Sheet 3 of 5) 0000-5015-300-H4

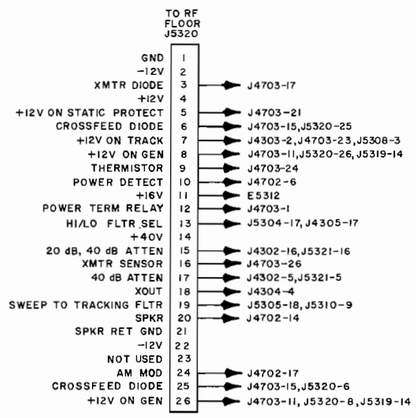


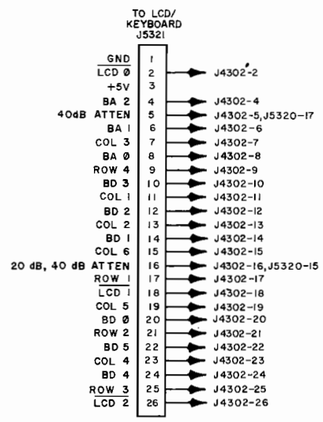












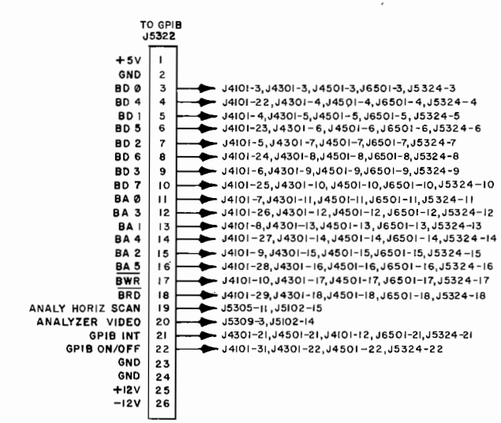
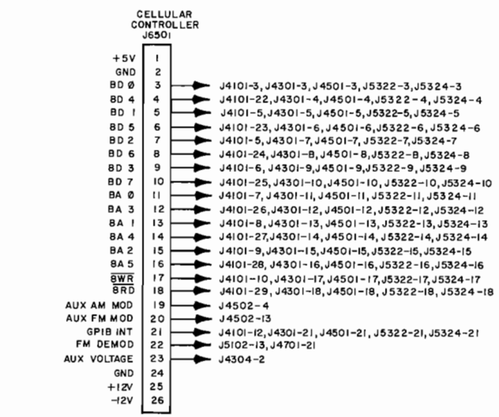
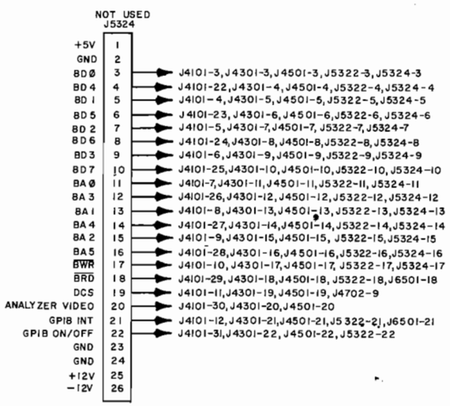
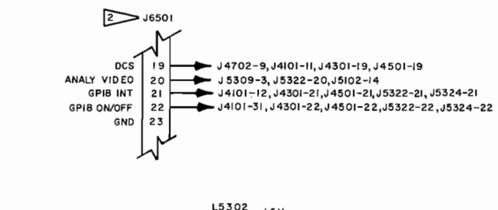
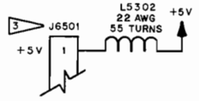


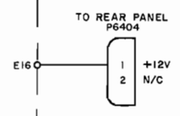
Figure 7-8 Motherboard Schematic (Sheet 4 of 5) 0000-5015-H4

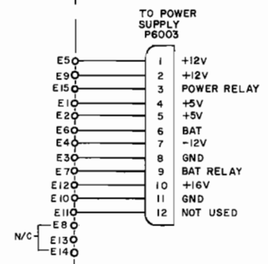




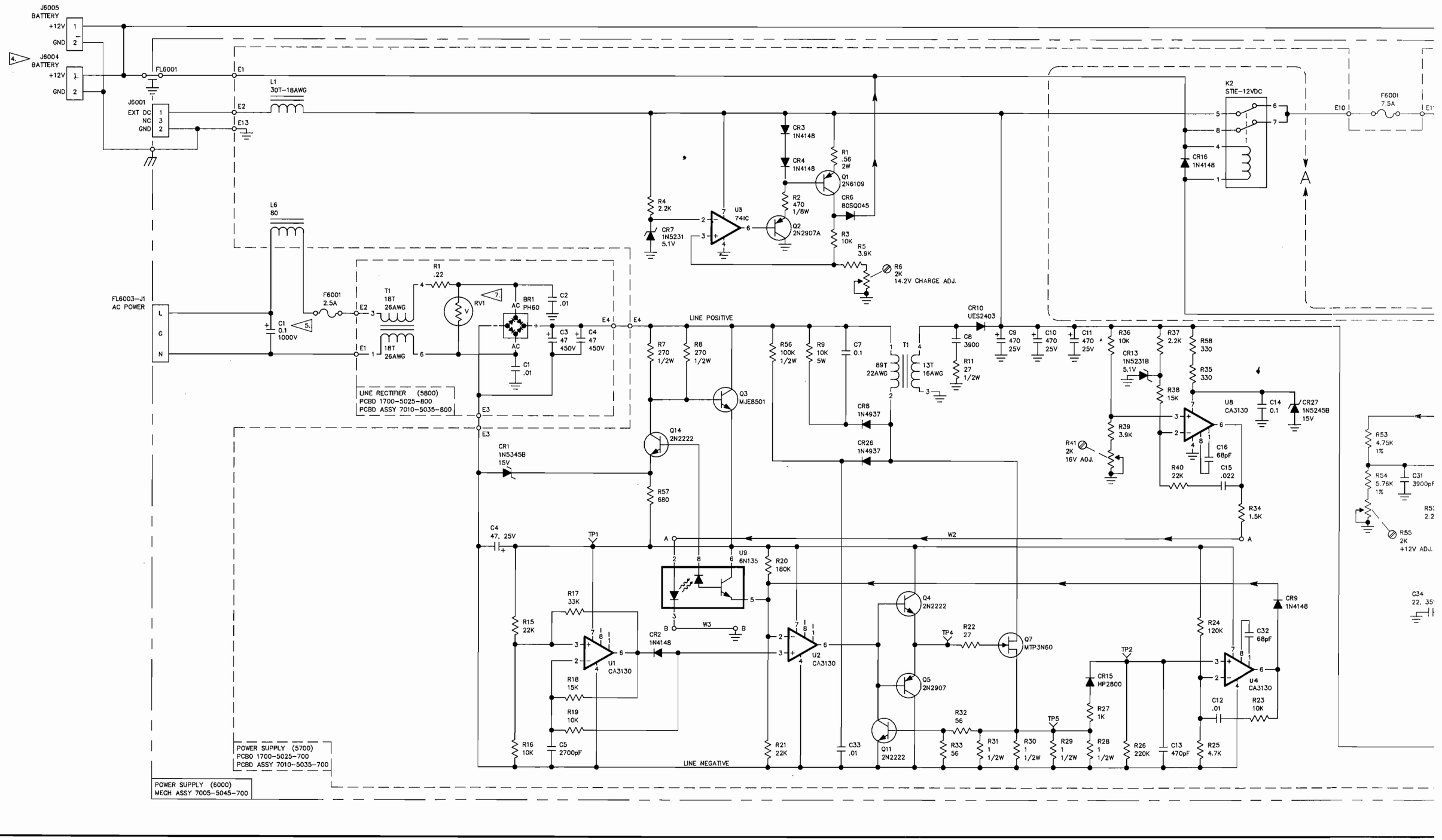


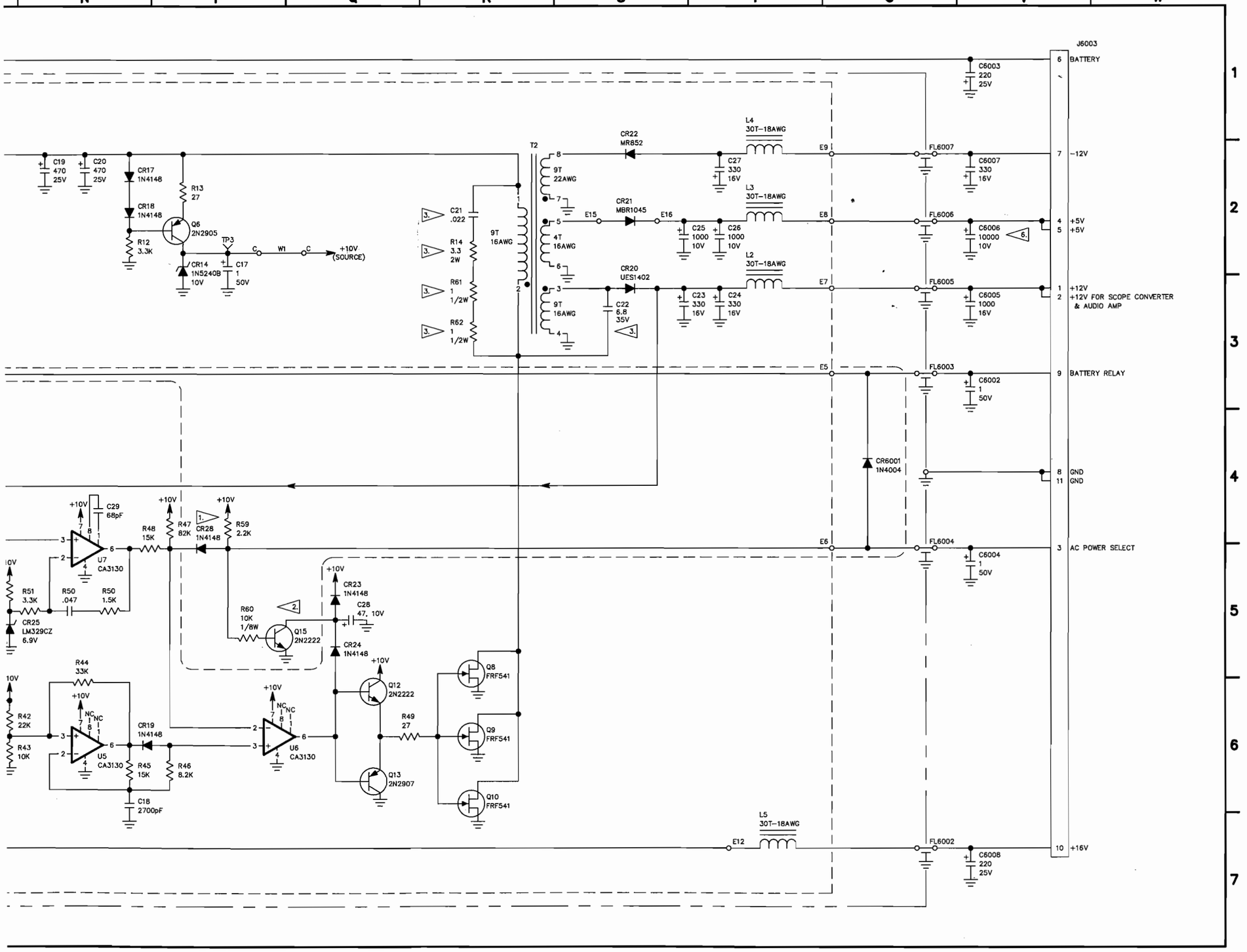


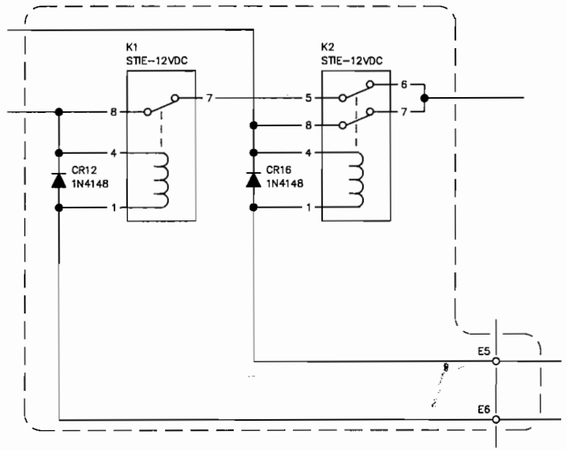




MOTHER BOARD PCB ASS'Y (5300)
PCB 1700-5025-300
PCB ASS'Y 7010-5035-300


J6005 BATTERY +12V 1 GND 2
J6004 BATTERY +12V 1 GND 2
FL6001
J6001 EXT DC 1 NC 3 GND 2
E1
E2
E13
L1 30T-18AWG
L6 80
FL6003-J1 AC POWER L G N
C1 0.1 1000V
F6001 2.5A
T1 18T 26AWG
18T 26AWG
R1 .22
RV1
BR1 AC PH60
C2 .01
C3 47 450V
C4 47 450V
C1 .01
E4
LINE RECTIFIER (5800)
PCBD 1700-5025-800
PCBD ASSY 7010-5035-800
E3
CR1 1N5345B 15V
Q14 2N2222
R57 680
C4 47, 25V
TP1
A
U9 6N135
W3
B
R17 33K
R15 22K
R18 15K
R19 10K
R16 10K
C5 2700pF
U1 CA3130
CR2 1N4148
U2 CA3130
R20 180K
R21 22K
LINE NEGATIVE
POWER SUPPLY (5700)
PCBD 1700-5025-700
PCBD ASSY 7010-5035-700
POWER SUPPLY (6000)
MECH ASSY 7005-5045-700
LINE POSITIVE
R7 270 1/2W
R8 270 1/2W
Q3 MJE8501
R56 100K 1/2W
R9 10K 5W
C7 0.1
CR8 1N4937
CR26 1N4937
CR3 1N4148
CR4 1N4148
R1 .56 2W
Q1 2N6109
R2 470 1/8W
Q2 2N2907A
CR6 80SQ045
R3 10K
R4 2.2K
CR7 1N5231 5.1V
U3 741C
R5 3.9K
R6 2K 14.2V CHARGE ADJ.
T1 89T 22AWG
13T 16AWG
CR10 UES2403
C8 3900
R11 27 1/2W
C9 470 25V
C10 470 25V
C11 470 25V
R36 10K
CR13 1N5231B 5.1V
R37 2.2K
R58 330
R35 330
R38 15K
U8 CA3130
C14 0.1
CR27 1N5245B 15V
R39 3.9K
R41 2K 16V ADJ.
C16 68pF
R40 22K
C15 .022
R34 1.5K
K2 STIE-12VDC
CR16 1N4148
F6001 7.5A
E10
E11
W2
R53 4.75K 1%
R54 5.76K 1%
C31 3900pF
R55 2K +12V ADJ.
C34 22, 35
Q4 2N2222
Q5 2N2907
Q11 2N2222
TP4
R22 27
Q7 MTP3N60
CR9 1N4148
R24 120K
C32 68pF
U4 CA3130
TP2
CR15 HP2800
R27 1K
C12 .01
R23 10K
TP5
R32 56
R33 56
R31 1 1/2W
R30 1 1/2W
R29 1 1/2W
R28 1 1/2W
R26 220K
C13 470pF
R25 4.7K





THRU SER. NO. 1141

DETAIL **A**

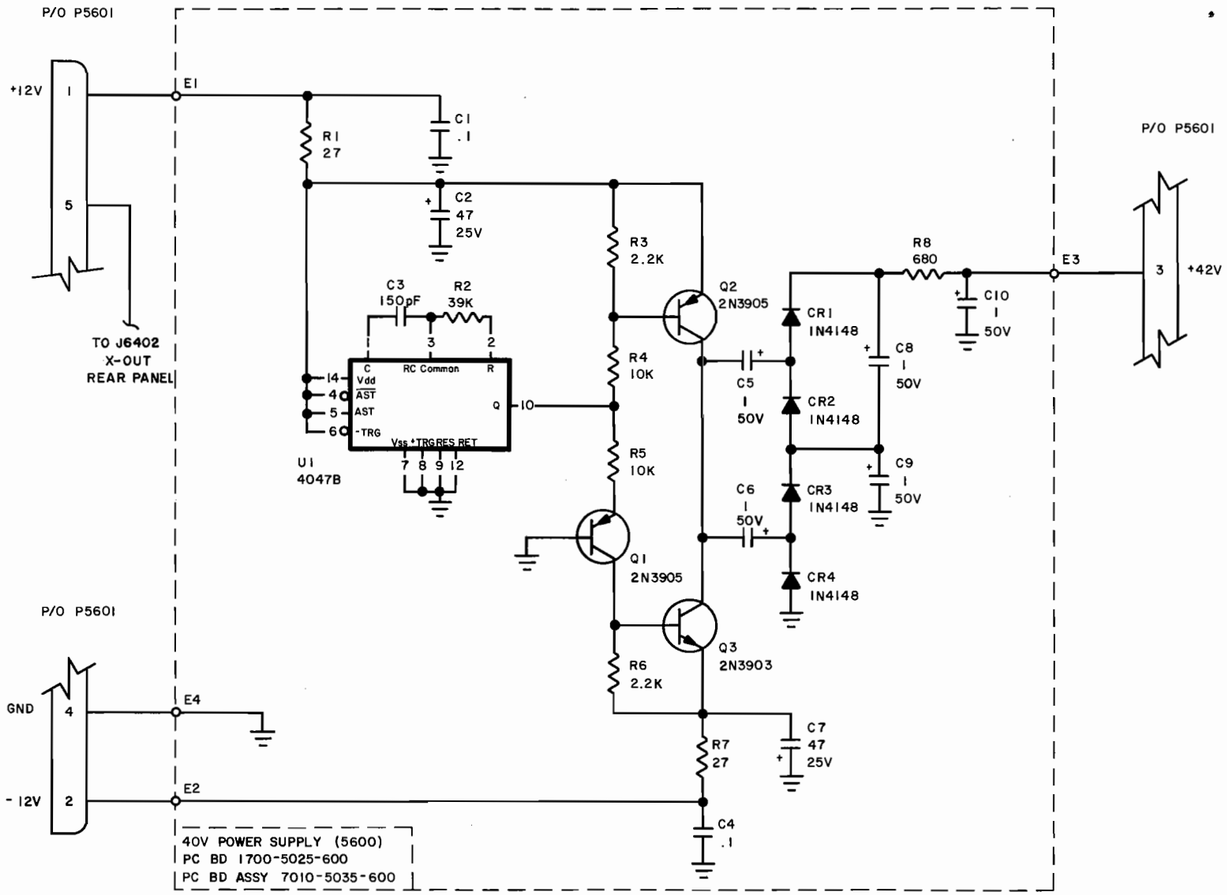
STANDARDS:
(UNLESS OTHERWISE NOTED)

1. ALL REF NOS CARRY AN ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES:
   A. MECH - 6000
   B. LINE RECTIFIER -- 5800 (E.G., R1 IS R5801)
   C. POWER SUPPLY -- 5700 (E.G., R1 IS R5701)

NOTES:

1. EFFECTIVE SER. NO. 1142 AND ON.
2. EFFECTIVE SER. NO. 1172 AND ON.
3. THRU SER. NO. 1967:
   C4 WAS 1 MICROFARAD; C7 WAS 10 MICROFARADS; C21 WAS .01 MICROFARADS; C30 WAS .01 MICROFARADS; CR21 WAS 80SQORT; R50 WAS 33K; R14 WAS 2.7 OHMS .
   SER. NO. 1968 AND ON:
   C22 NOT USED
   SER. NO. 1968 THRU 2234:
   R14 USED IN SERIES WITH R61 AND R62 (R14, R61, R62 EACH 1 OHM, 1/2 W)
   SER. NO. 2235 AND ON:
   R61, R62 NOT USED; R14 IS 3.3W, 2W
4. EFFECTIVE SER. NO. 2134 AND ON, NOT USED.
5. THRU SER. NO. 2270, C6001 WAS 0.47, 1000 V.
6. THRU SER. NO. 2598, C6006 WAS 1000 MICROFARADS.
7. EFFECTIVE SER. NO. 2547 AND ON.

Figure 7-9 Power Supply Module Schematic 0000-5015-700-D7



STANDARDS:
(UNLESS OTHERWISE NOTED)

1. ALL REF NOS CARRY AN ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES:

   A. MECH
   B. PC BD ASSY - (5600)
   C.
   D.

2. ALL RESISTORS ARE 1/4 W, 5% TOLERANCE.

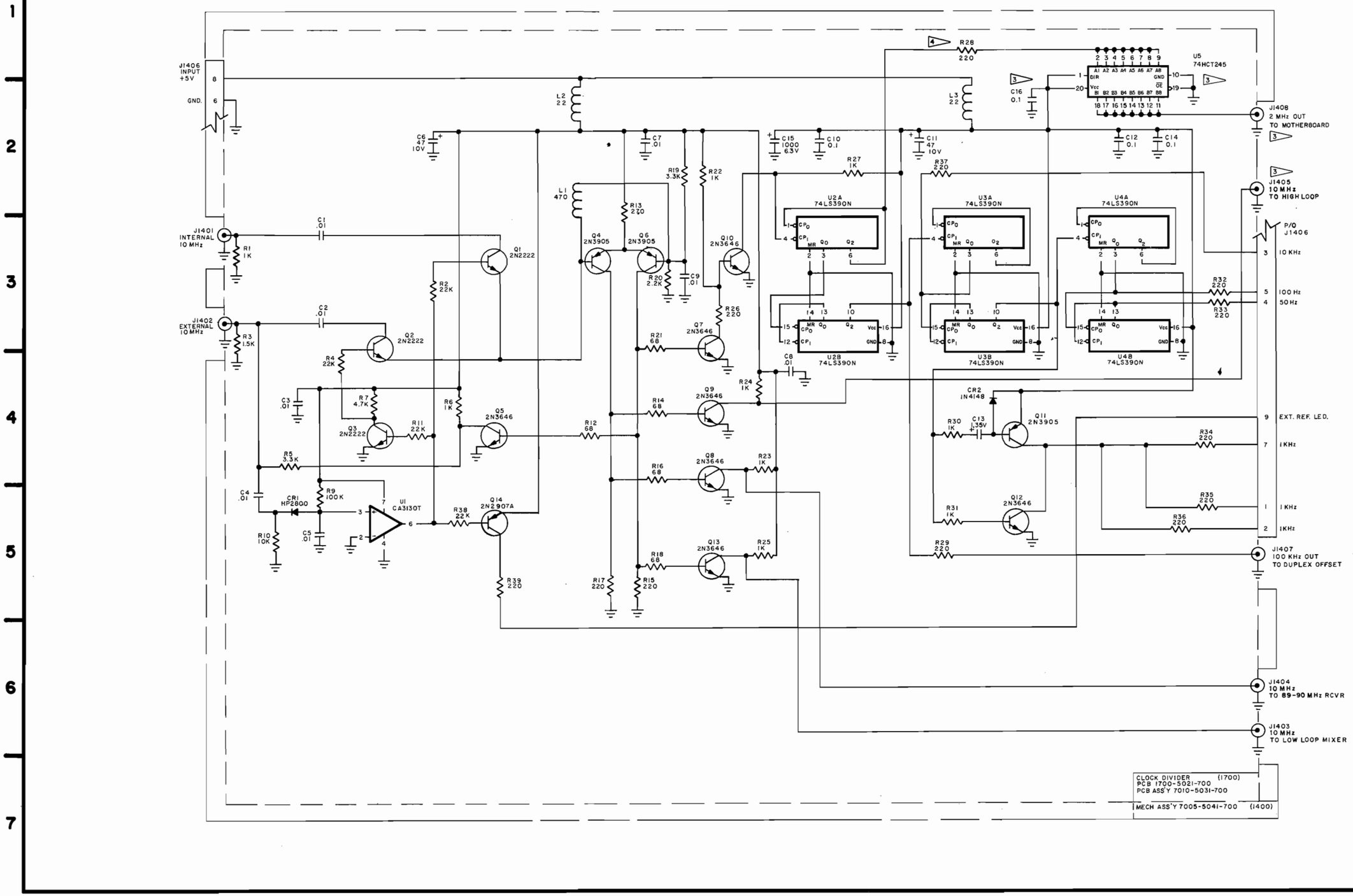
3. ALL RESISTANCE IS EXPRESSED IN OHMS.

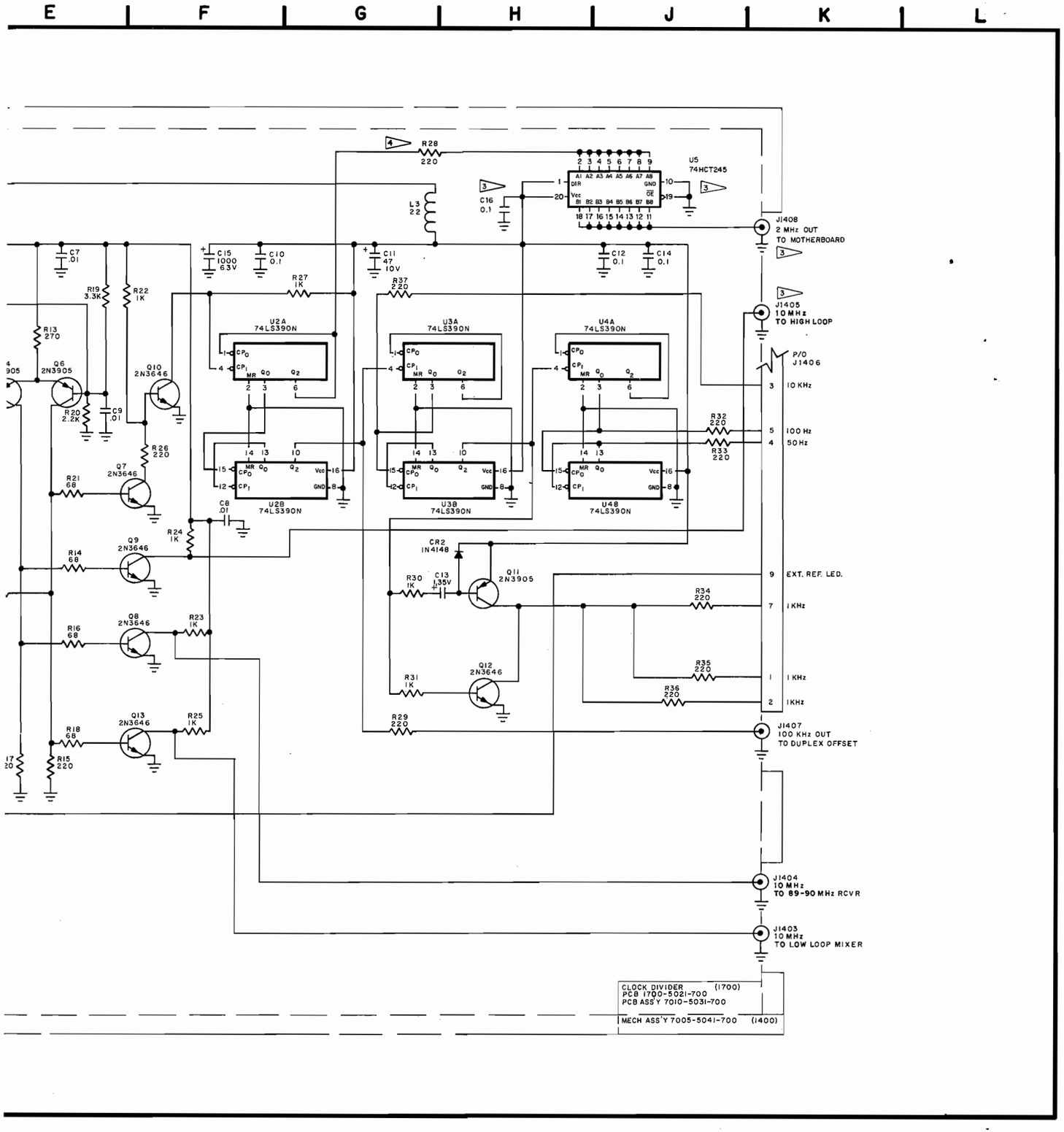
4. ALL CAPACITANCE IS EXPRESSED IN MICROFARADS.

NOTES:

1. LAST REF NOS USED:
   E4, C10, R8, CR4, Q3, U1, P5601

Figure 7-10 40V Power Supply PC Board Schematic 0000-5015-(


J1406 INPUT +5V
GND.
J1401 INTERNAL 10 MHz
J1402 EXTERNAL 10 MHz
R1 1K
R2 22K
R3 1.5K
R4 22K
R5 3.3K
R6 1K
R7 4.7K
R9 100K
R10 10K
R11 22K
R12 68
R13 220
R14 68
R16 68
R18 68
R19 3.3K
R20 2.2K
R21 68
R22 1K
R23 1K
R24 1K
R25 1K
R26 220
R27 1K
R28 220
R29 220
R30 1K
R31 1K
R32 220
R33 220
R34 220
R35 220
R36 220
R37 220
R38 22K
R39 220
R17 220
R15 220
C1 .01
C2 .01
C3 .01
C4 .01
C5 .01
C6 47 10V
C7 .01
C8 .01
C9 .01
C10 0.1
C11 47 10V
C12 0.1
C13 1.35V
C14 0.1
C15 1000 6.3V
C16 0.1
L1 470
L2 22
L3 22
Q1 2N2222
Q2 2N2222
Q3 2N2222
Q4 2N3905
Q5 2N3646
Q6 2N3905
Q7 2N3646
Q8 2N3646
Q9 2N3646
Q10 2N3646
Q11 2N3905
Q12 2N3646
Q13 2N3646
Q14 2N2907A
CR1 HP2800
CR2 IN4148
U1 CA3130T
U2A 74LS390N
U2B 74LS390N
U3A 74LS390N
U3B 74LS390N
U4A 74LS390N
U4B 74LS390N
U5 74HCT245
J1408 2 MHz OUT TO MOTHERBOARD
J1405 10 MHz TO HIGH LOOP
P/O J1406
10 KHz
100 Hz
50 Hz
EXT. REF. LED.
1 KHz
1 KHz
1 KHz
J1407 100 KHz OUT TO DUPLEX OFFSET
J1404 10 MHz TO 89-90 MHz RCVR
J1403 10 MHz TO LOW LOOP MIXER
CLOCK DIVIDER (1700)
PCB 1700-5021-700
PCB ASS'Y 7010-5031-700
MECH ASS'Y 7005-5041-700 (1400)



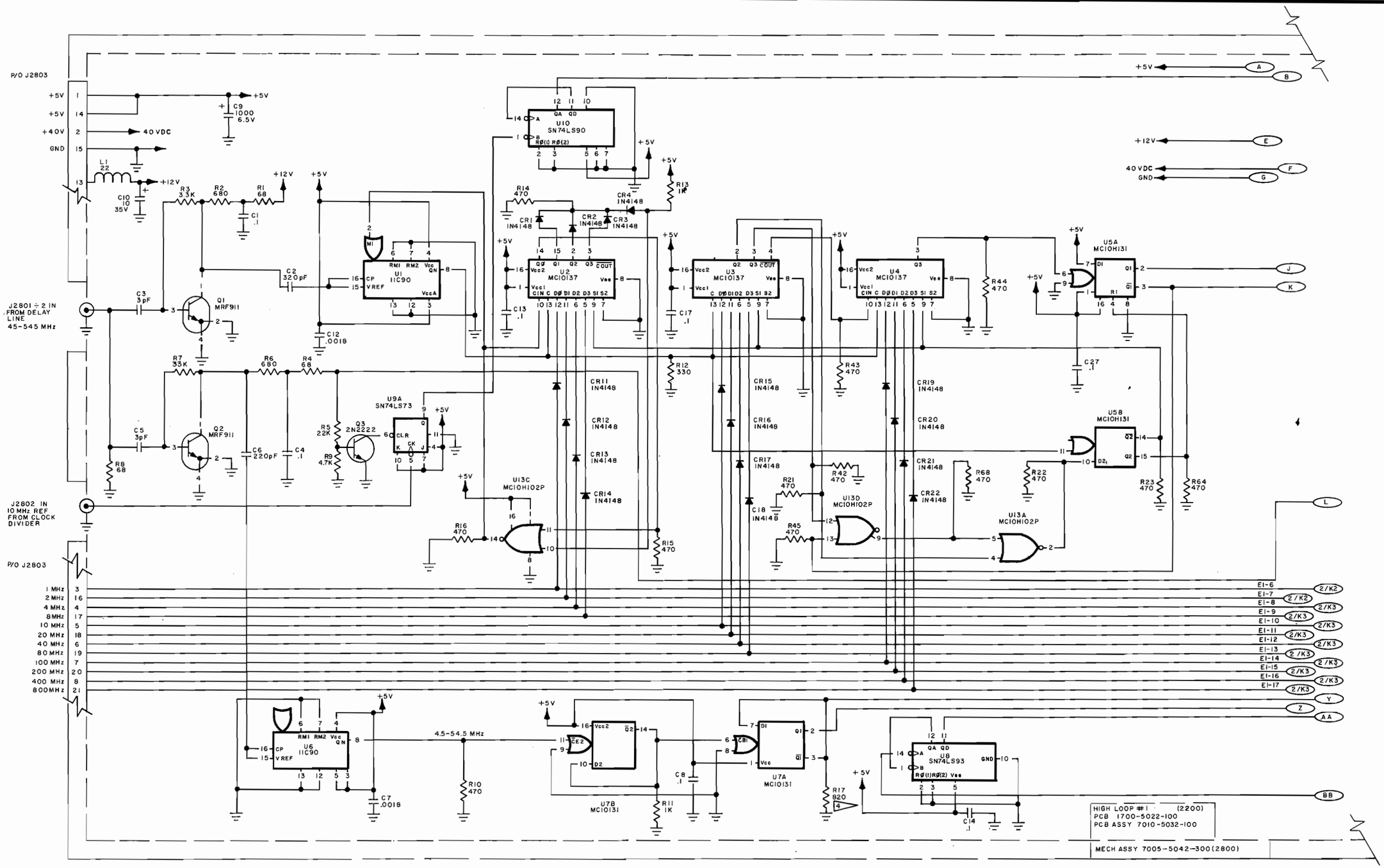
STANDARDS:
(UNLESS OTHERWISE NOTED)

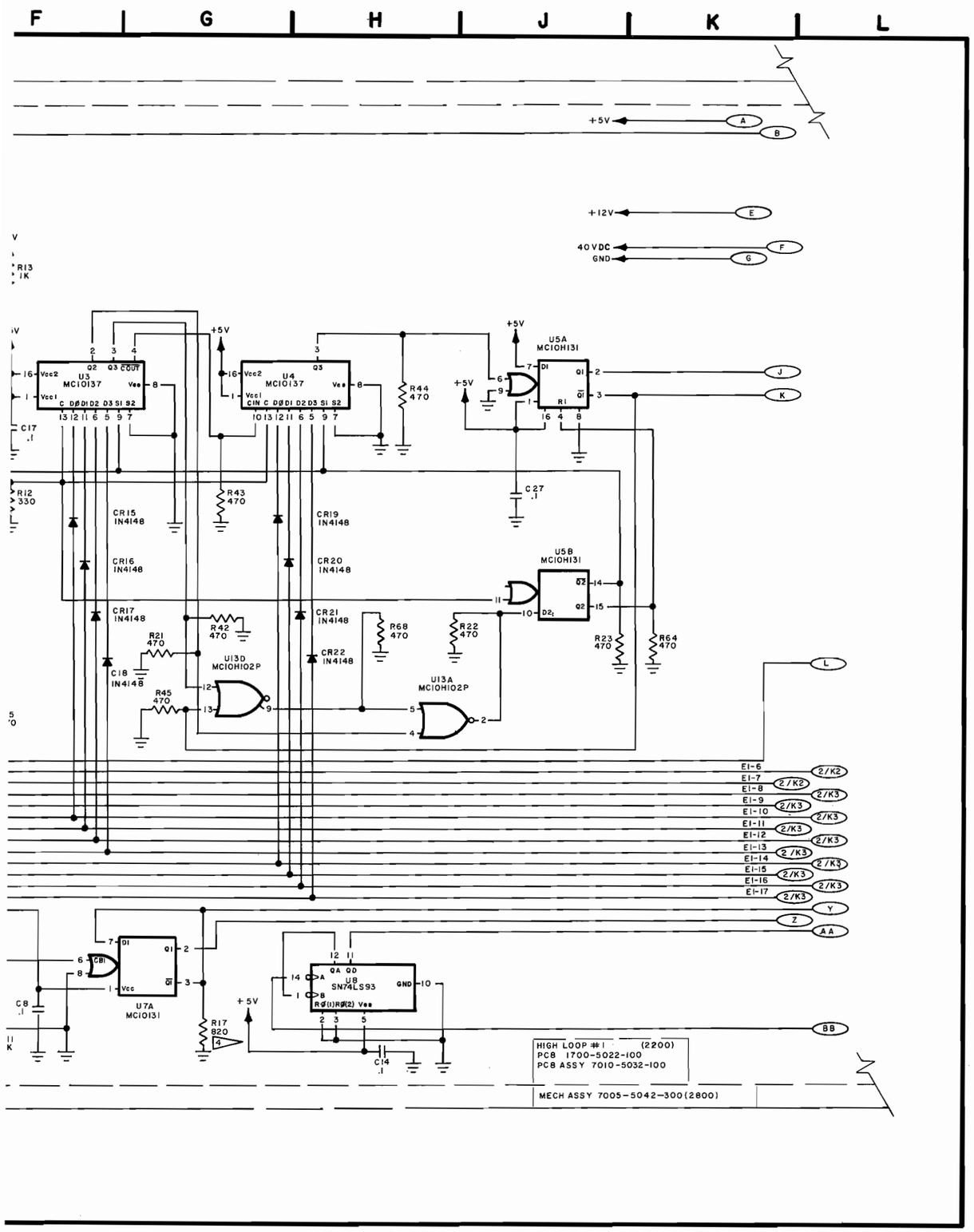
1. ALL REF NOS CARRY AN ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES 1400 AND 1700.
   A. MECH ASSY - 7005-5041-700 (1400)
   B. PC BOARD ASSY - 7010-5031-700 (1700; E.G., R1 IS R1701)
2. ALL RESISTORS ARE 1/4 W, 5% TOLERANCE.
3. ALL RESISTANCE IS EXPRESSED IN OHMS.
4. ALL CAPACITANCE IS EXPRESSED IN MICROFARADS.
5. ALL INDUCTANCE IS EXPRESSED IN MICROHENRYS.

NOTES:

1. LAST REF NOS USED:
   J8, Q14, U5, CR2, L3, R29, C16.
2. REF NOS NOT USED: R1708.
3. EFFECTIVE THRU SER. NO. 2001, U5 AND C16 WERE NOT USED. U2A PINS 1 AND 6 WERE CONNECTED TO J1405, Q9 COLLECTOR AND R24 WERE CONNECTED TO J1408.
4. EFFECTIVE THRU SER. NO. 1967, R28 220 WAS USED. SER. NO. 1968 THRU 2001, W1 WAS USED.

Figure 7-11 Clock Divider Module Schematic 0000-5011-700-C


P/O J2803
+5V
+40V
GND
40 VDC
+12V
J2801 ÷ 2 IN FROM DELAY LINE 45-545 MHz
J2802 IN 10 MHz REF FROM CLOCK DIVIDER
P/O J2803
1 MHz
2 MHz
4 MHz
8MHz
10 MHz
20 MHz
40 MHz
80 MHz
100 MHz
200 MHz
400 MHz
800MHz
4.5-54.5 MHz
U1 11C90
U2 MC10137
U3 MC10137
U4 MC10137
U5A MC10H131
U5B MC10H131
U6 11C90
U7A MC10131
U7B MC10131
U8 SN74LS93
U9A SN74LS73
U10 SN74LS90
U13A MC10H102P
U13C MC10H102P
U13D MC10H102P
Q1 MRF911
Q2 MRF911
Q3 2N2222
E1-6
E1-7
E1-8
E1-9
E1-10
E1-11
E1-12
E1-13
E1-14
E1-15
E1-16
E1-17
HIGH LOOP #1 (2200)
PCB 1700-5022-100
PCB ASSY 7010-5032-100
MECH ASSY 7005-5042-300(2800)



STANDARDS:

(UNLESS OTHERWISE NOTED)

1. ALL REF NOS CARRY AN ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES 2200 AND 2800.
   A. MECH ASSY - 7005-5042-300 (2800)
   B. PC BOARD ASSY - 7010-5032-100 (2200; E.G., R1 IS R2201)
2. ALL RESISTORS ARE 1/4 W, 5% TOLERANCE.
3. ALL RESISTANCE IS EXPRESSED IN OHMS.
4. ALL CAPACITANCE IS EXPRESSED IN MICROFARADS.
5. ALL INDUCTANCE IS EXPRESSED IN MICROHENRYS.

NOTES:

1. LAST REF NOS USED: J2803, R68, U16, C31, Q21, CR 25, L3.
2. REF NOS NOT USED: C16, C24, R51, Q11.
3. I.C. FUNCTIONS NOT USED: U13B, U15A, U10B.
4. PRIOR TO SER. NO. 2774, R17, R18, R19, R45 WERE 1K; R48 WAS 330 W.

Figure 7-12 High Loop #1 Schematic (Sheet 1 of 2) 0000-5012-100-D1

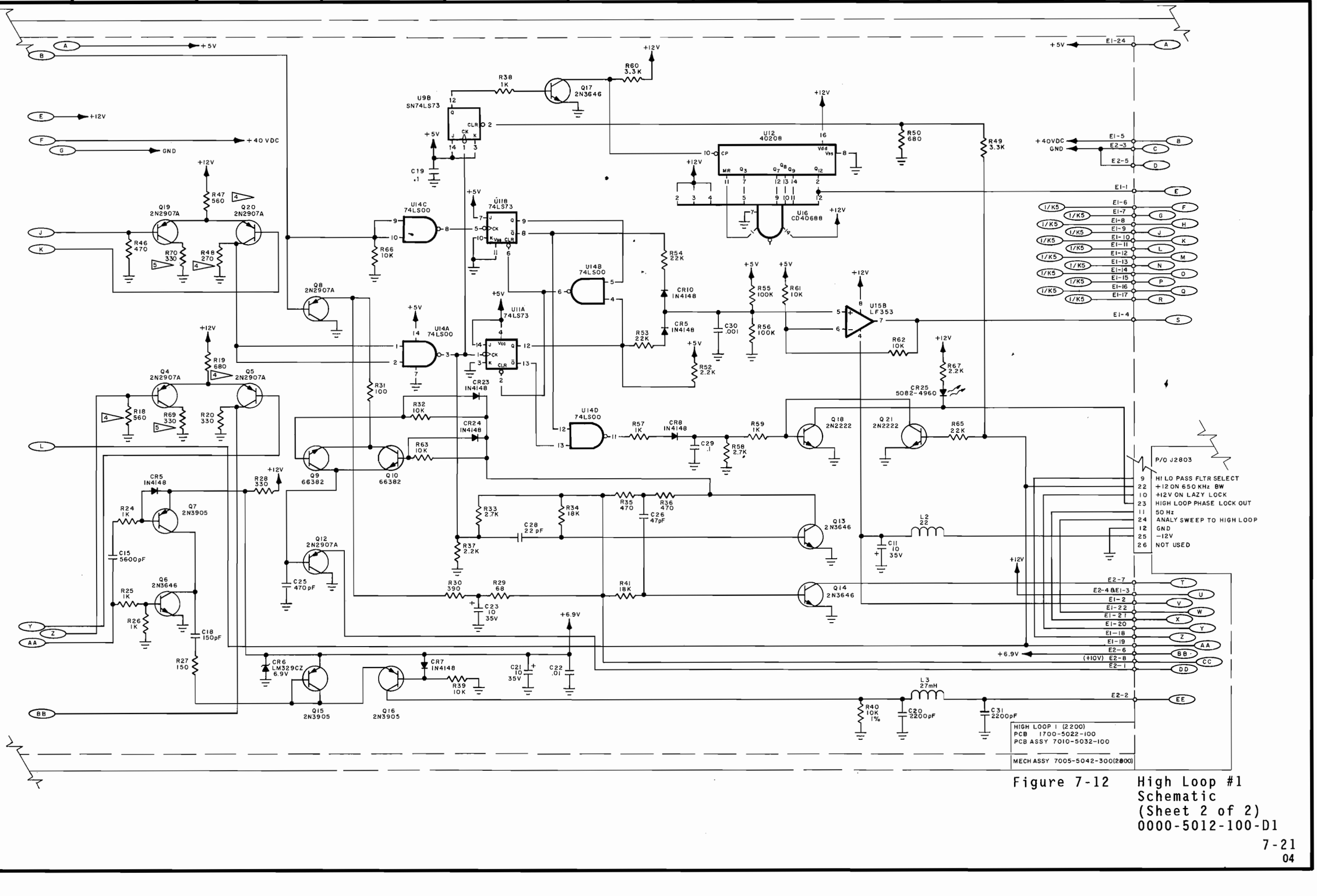
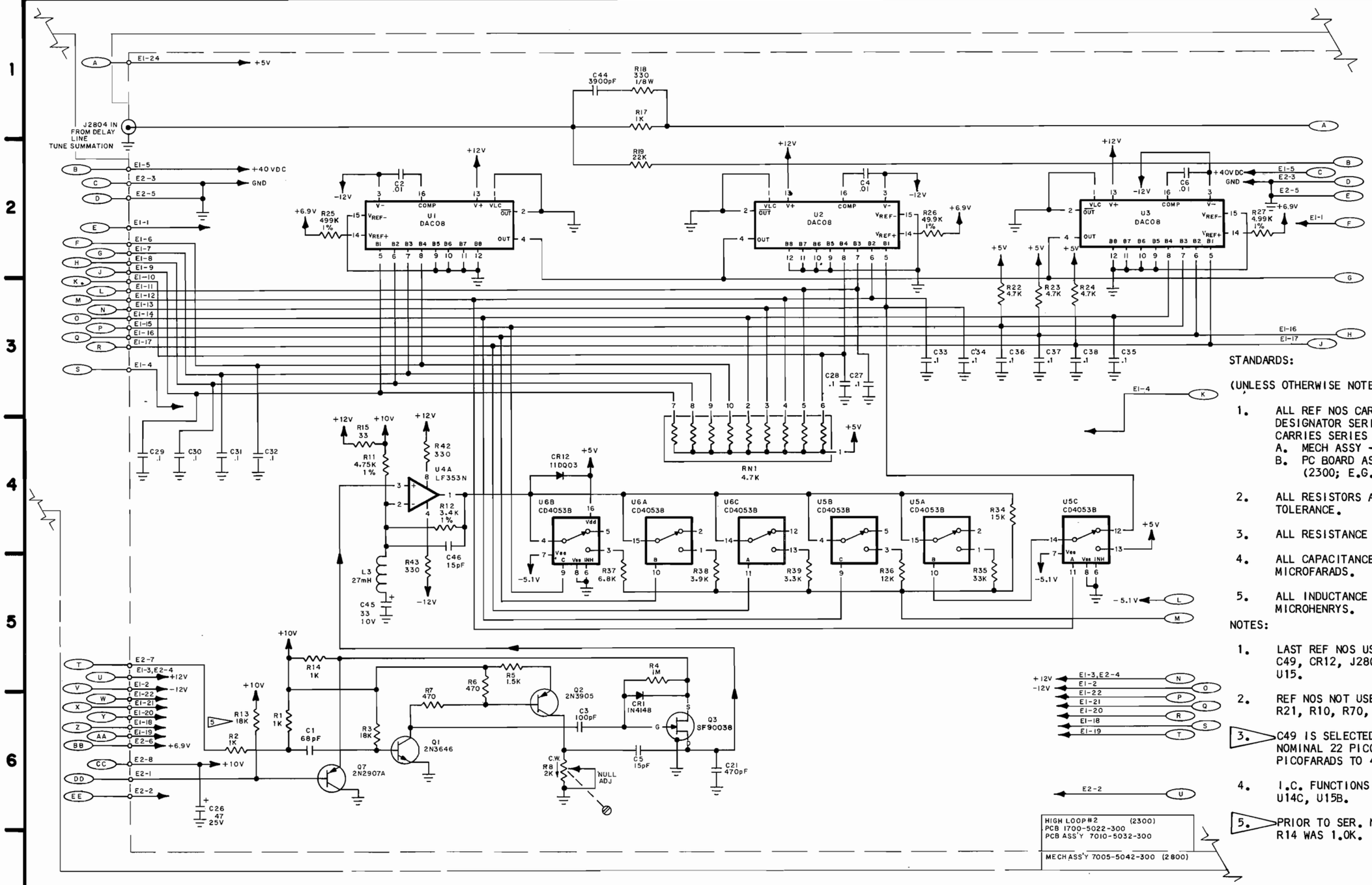


Figure 7-12 High Loop #1 Schematic (Sheet 2 of 2) 0000-5012-100-D1



STANDARDS:

(UNLESS OTHERWISE NOTED)

1. ALL REF NOS CARRY AN ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES 2300 AND 2800.
   A. MECH ASSY — 7005-5042-300 (2800)
   B. PC BOARD ASSY — 7010-5032-300 (2300; E.G., R1 IS R2301).
2. ALL RESISTORS ARE 1/4 W, 5% TOLERANCE.
3. ALL RESISTANCE IS EXPRESSED IN OHMS.
4. ALL CAPACITANCE IS EXPRESSED IN MICROFARADS.
5. ALL INDUCTANCE IS EXPRESSED IN MICROHENRYS.

NOTES:

1. LAST REF NOS USED: C49, CR12, J2806, E2, L3, Q7, R90, RN1, U15.
2. REF NOS NOT USED: R21, R10, R70, R16, U12, C40, R20.
3. C49 IS SELECTED AT TEST (SAT): NOMINAL 22 PICOFARADS, RANGE 10 PICOFARADS TO 47 PICOFARADS.
4. I.C. FUNCTIONS NOT USED: U10B, U14B, U14C, U15B.
5. PRIOR TO SER. NO. 2868, R13 WAS 33K, R14 WAS 1.0K.

Figure 7-13 High Loop #2 Schematic (Sheet 1 of 2)
0000-5012-300-J1

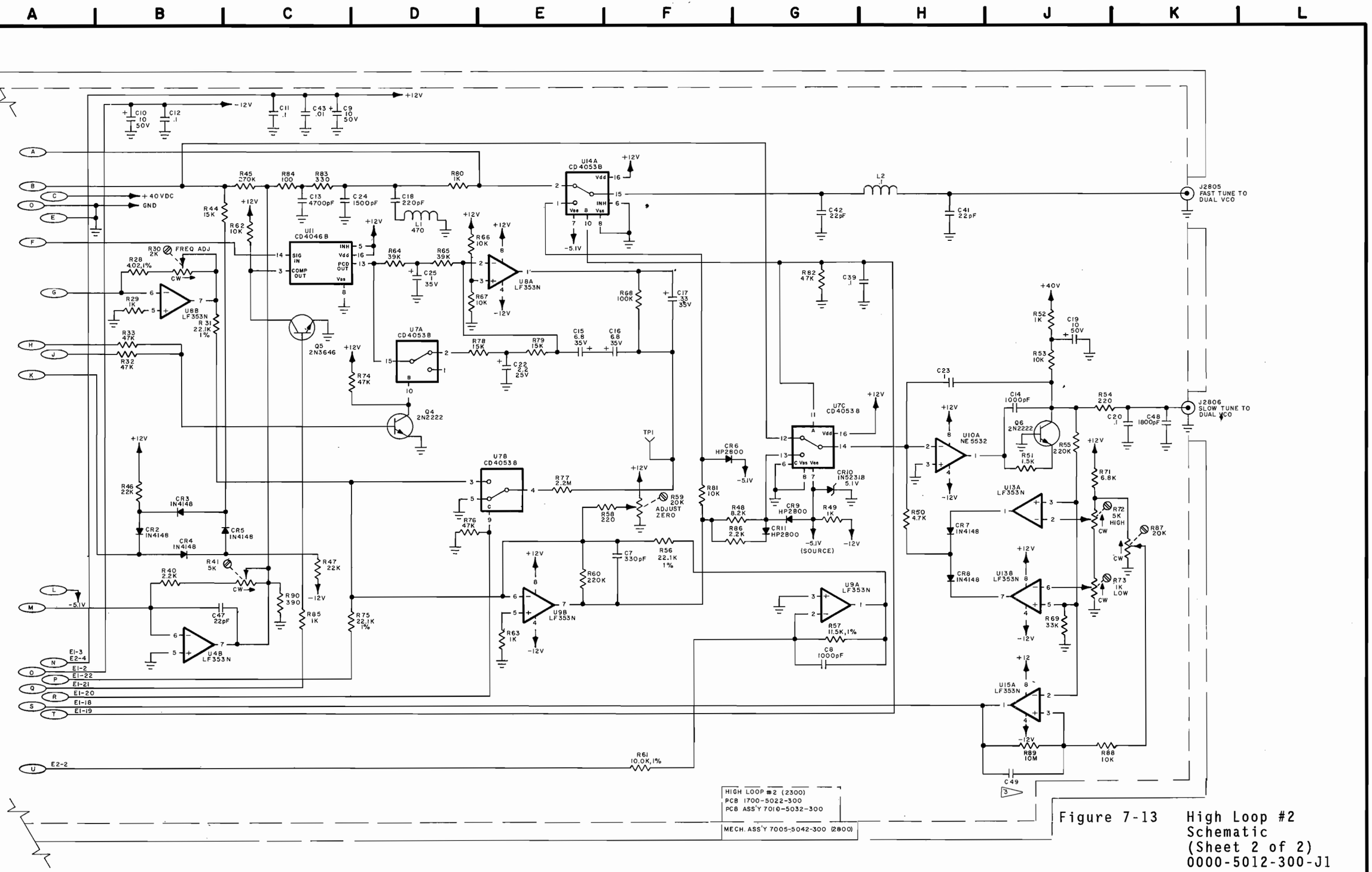
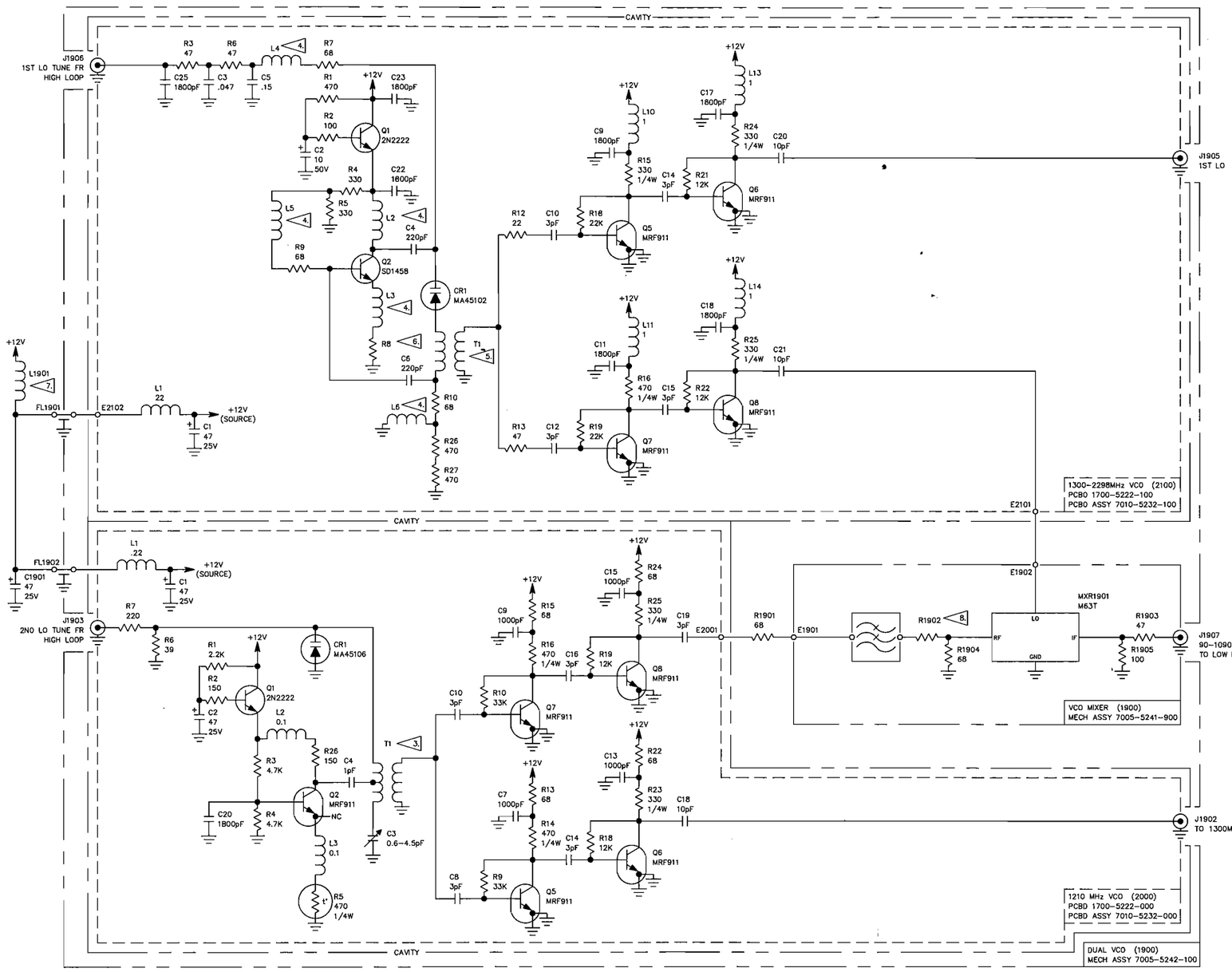


Figure 7-13 High Loop #2 Schematic (Sheet 2 of 2) 0000-5012-300-J1



STANDARDS:

(UNLESS OTHERWISE NOTED)

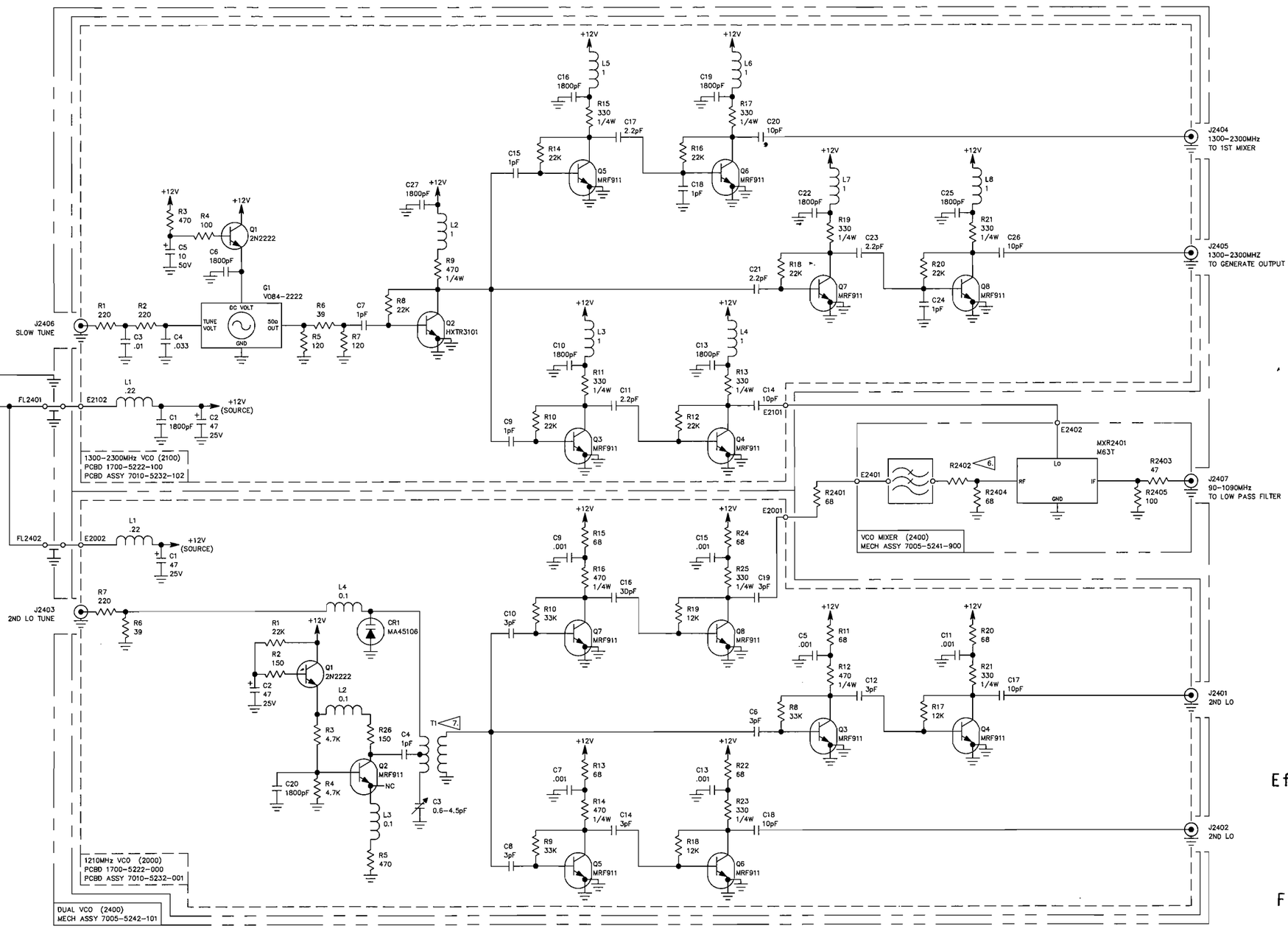
1. ALL REF NOS CARRY AN ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES:
   - A. VCO MIXER MECH ASSY (1900)
   - B. 1210 MHZ PC BOARD ASSY (2000) (E.G., R1 IS R2001)
   - C. 1300-2298 MHZ VCOPC BOARD ASSY (2100) (E.G. R1 IS R2101)
2. ALL RESISTORS ARE 1/8 W, 5% TOLERANCE
3. ALL RESISTANCE IS EXPRESSED IN OHMS.
4. ALL CAPACITANCE IS EXPRESSED IN MICROFARADS.
5. ALL INDUCTANCE IS EXPRESSED IN MICROHENRYS.

NOTES:

1. NOT USED
2. NOT USED
3. PRIMARY (T2001) IS FORMED BY LEAD OF C2004 PLACED 0.38 DEGREES FROM SECONDARY. SECONDARY IS FORMED BY 22 GA. WIRE, 0.8" LONG.
4. INDUCTORS ARE MADE OF 10 TURNS OF 38 GA. WIRE, 0.014" DIA.
5. PRIMARY (T2101) IS FORMED BY LEAD OF C2106 SOLDERED TO CR2101, LENGTH SELECTED AT TEST (SAT). SECONDARY IS 22 GA. WIRE BENT TO WITHIN 0.4" OF BOARD SURFACE THEN BACK TO WITHIN 0.2" OF PRIMARY.
6. R2108 IS SELECTED AT TEST (SAT). NOMINAL IS 180 OHMS, RANGE IS 47 OHMS TO 220 OHMS.
7. TOROID IS 18 GA., 30 TURNS.
8. R1902 IS SELECTED AT TEST (SAT) NOMINAL IS 150 OHMS, RANGE IS 68 OHMS TO 330 OHMS.

Effective thru Ser. No. 2444

Figure 7-14 Dual VCO Module Schematic 0000-5012-101-L2

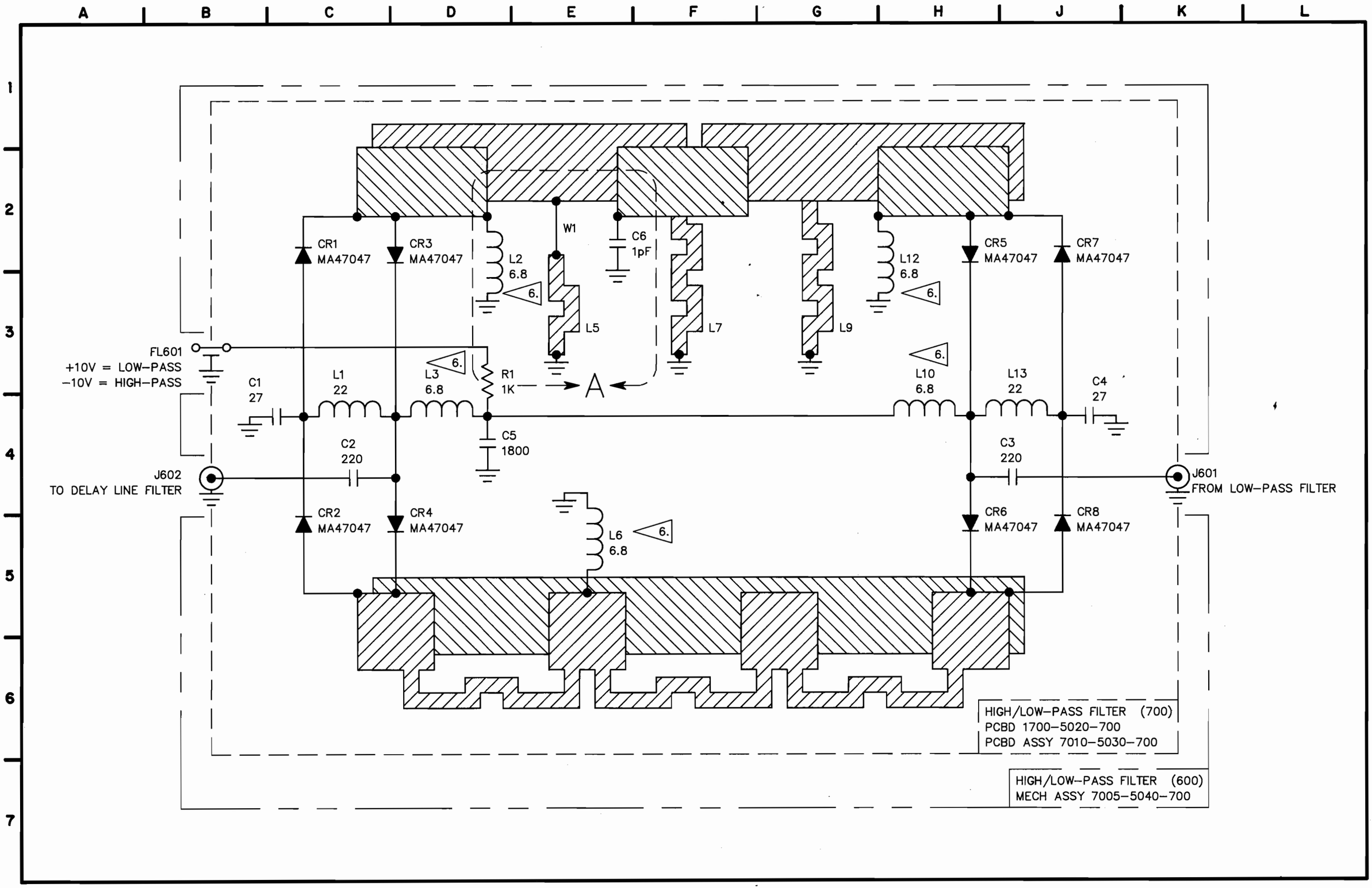


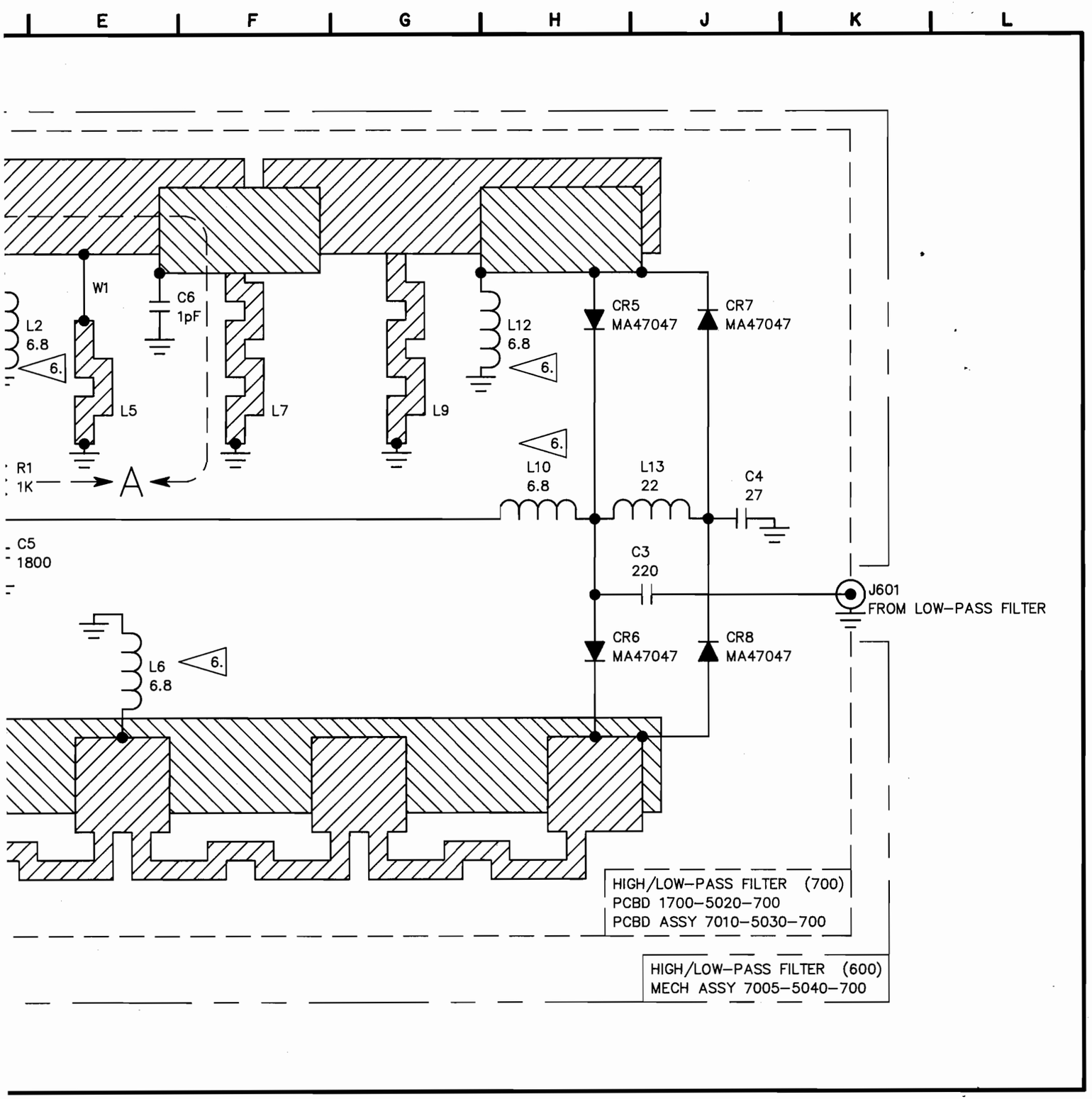
NOTES:
(UNLESS OTHERWISE NOTED)

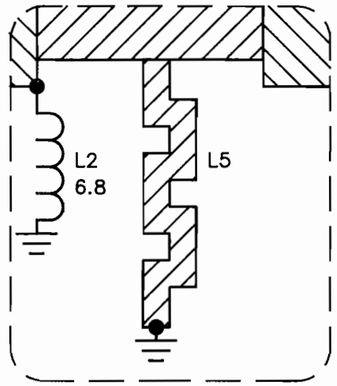
1. ALL REF NOS CARRY AN ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES:
   - A. MECH ASSY 7005-5242-101 (2400)
   - B. 1300-2298 MHz VCO PCB ASSY 7010-5232-001 (2000)
   - C. 1210 MHz PCB ASSY 7010-5232-100 (2100)
2. ALL RESISTORS ARE 1/8 W, ±5%.
3. ALL RESISTANCE IS EXPRESSED IN OHMS.
4. ALL CAPACITANCE IS EXPRESSED IN MICROFARADS.
5. ALL INDUCTANCE IS EXPRESSED IN MICROHENRYS.
6. EFFECTIVE SER. NO. 2166:
   VCO MIXER -
   R2402 IS S.A.T., NOMINAL = 150Ω, RANGE = 68 Ω thru 330 Ω;
   THRU SER. NO. 2165:
   1300-2300 MHz VCO -
   R16 WAS 330 Ω, R11 AND R12 WERE 47 Ω;
   1210 MHz VCO -
   C19 WAS 10 pF.
7. PRIMARY OF T2001 IS FORMED BY 18 GA BUS WIRE, .9" LONG WITH LEAD OF C2004 SOLDERED TO APPROXIMATE CENTER OF WIRE (EXACT LOCATION OF C2004 ON WIRE IS SELECTED AT TEST). SECONDARY OF T2001 IS FORMED BY 22 GA BUS WIRE, .8" LONG.

Effective Ser. No. 2445 and ON

Figure 7-14a Dual VCO Module Schematic 0000-5012-001-L3 0000-5212-102-A1


A
B
C
D
E
F
G
H
J
K
L
1
2
3
4
5
6
7
CR1
MA47047
CR3
MA47047
L2
6.8
6.
W1
C6
1pF
L5
L7
L9
L12
6.8
6.
CR5
MA47047
CR7
MA47047
FL601
+10V = LOW–PASS
–10V = HIGH–PASS
C1
27
L1
22
6.
L3
6.8
R1
1K
A
6.
L10
6.8
L13
22
C4
27
C2
220
C5
1800
C3
220
J602
TO DELAY LINE FILTER
J601
FROM LOW–PASS FILTER
CR2
MA47047
CR4
MA47047
L6
6.8
6.
CR6
MA47047
CR8
MA47047
HIGH/LOW–PASS FILTER (700)
PCBD 1700–5020–700
PCBD ASSY 7010–5030–700
HIGH/LOW–PASS FILTER (600)
MECH ASSY 7005–5040–700





DETAIL **A**

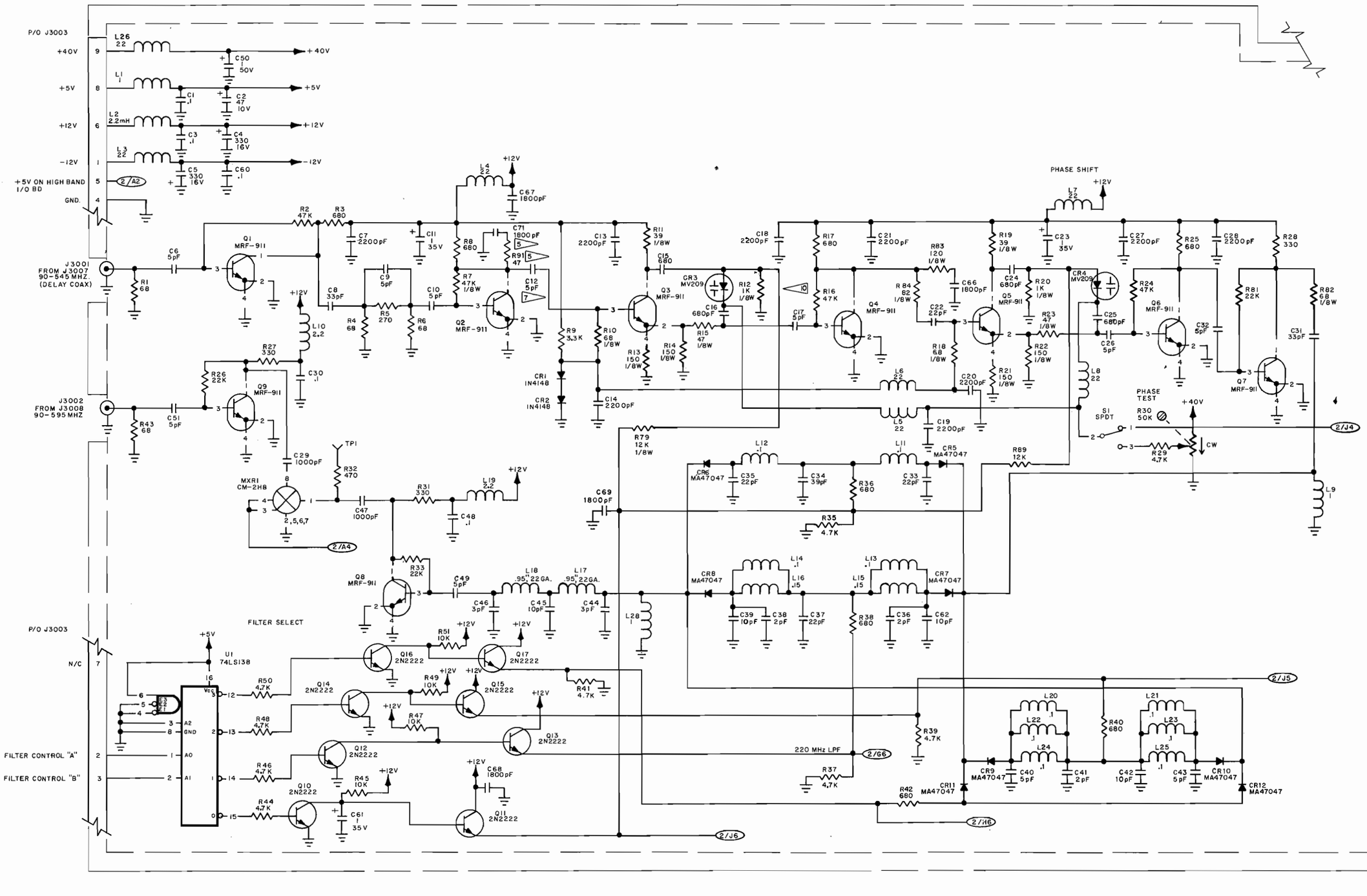
THRU SER. NO. 2696

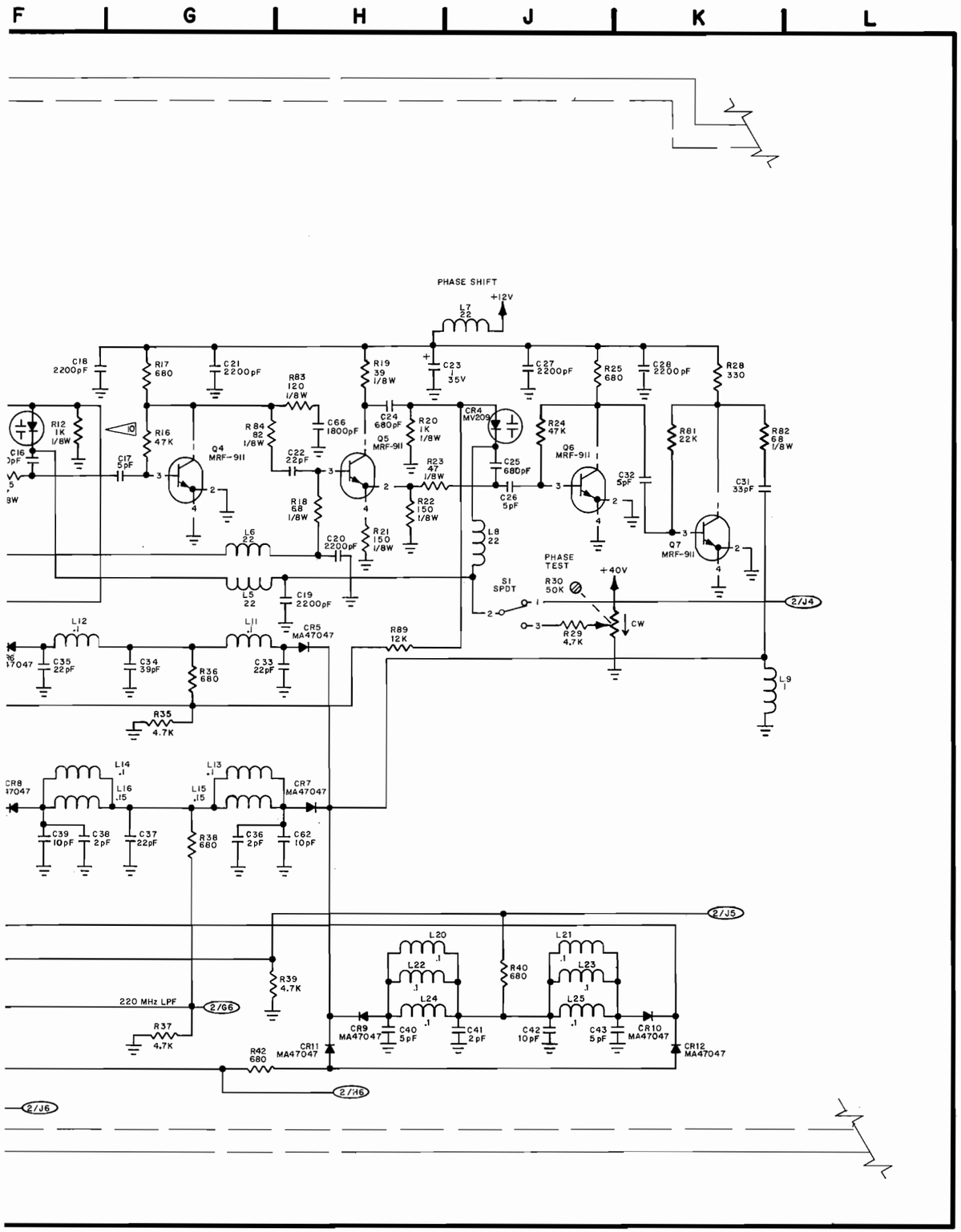
NOTES:

1. ALL REF NOS CARRY AN ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES: 600 AND 700.
   A. MECH ASSY 7005-5040-700 (600)
   B. PC BOARD ASSY 7010-5030-700 (700; E.G., R1 IS R701).
2. ALL RESISTORS ARE 1/4 W, 5% TOLERANCE.
3. ALL RESISTANCE IS EXPRESSED IN OHMS.
4. ALL CAPACITANCE IS EXPRESSED IN MICROFARADS.
5. ALL INDUCTANCE IS EXPRESSED IN MICROHENRYS.

6. THRU SER. NO. 2220; L2, L3, L6, L10, L12 WERE 1 MICROHENRY.

Figure 7-15 High/Low Pass Filter Module Schematic 0000-5010-700-D1


P/O J3003
+40V
+5V
+12V
-12V
+5V ON HIGH BAND I/O BD
GND.
L26 22
L1
L2 2.2mH
L3 22
C50 1 50V
C1 .1
C2 47 10V
C3 .1
C4 330 16V
C5 330 16V
C60 .1
2/A2
J3001 FROM J3007 90-545 MHZ. (DELAY COAX)
J3002 FROM J3008 90-595 MHZ
R1 68
R43 68
C6 5pF
C51 5pF
Q1 MRF-911
Q9 MRF-911
R2 47K
R3 680
C7 2200pF
C11 1 35V
C8 33pF
C9 5pF
C10 5pF
R4 68
R5 270
R6 68
Q2 MRF-911
L4 22
C67 1800pF
R8 680
R7 47K 1/8W
C71 1800pF
R91 47
C12 5pF
C13 2200pF
R9 3.3K
R10 68 1/8W
CR1 IN4148
CR2 IN4148
C14 220pF
R11 39 1/8W
C15 680
Q3 MRF-911
R13 150 1/8W
R14 150 1/8W
CR3 MV209
R12 1K 1/8W
C16 680pF
R15 47 1/8W
C17 5pF
C18 2200pF
R17 680
R16 47K
Q4 MRF-911
C21 2200pF
R83 120 1/8W
R84 82 1/8W
C22 22pF
R18 6.8 1/8W
C66 1800pF
C20 2200pF
L6 22
L5 22
C19 2200pF
R19 39 1/8W
C24 680pF
Q5 MRF-911
R21 150 1/8W
R20 1K 1/8W
R23 47 1/8W
R22 150 1/8W
L7 22
C23 1 35V
PHASE SHIFT
CR4 MV209
C25 680pF
C26 5pF
L8 22
C27 2200pF
R24 47K
Q6 MRF-911
C32 5pF
R25 680
C28 2200pF
R81 22K
Q7 MRF-911
R28 330
R82 68 1/8W
C31 33pF
PHASE TEST
S1 SPDT
R30 50K
+40V
CW
R29 4.7K
2/J4
L9
L10 2.2
R27 330
C30 .1
R26 22K
TP1
C29 1000pF
R32 470
MXR1 CM-2H8
2,5,6,7
C47 1000pF
R31 330
L19 2.2
C48 .1
2/A4
R79 12K 1/8W
C69 1800pF
L12
L11
CR6 MA47047
C35 22pF
C34 39pF
R36 680
C33 22pF
CR5 MA47047
R89 12K
R35 4.7K
R33 22K
Q8 MRF-911
C49 5pF
L18 .95" 22GA.
L17 .95" 22GA.
C46 3pF
C45 10pF
C44 3pF
L28
CR8 MA47047
L14 .1
L16 .15
L13 .1
L15 .15
CR7 MA47047
C39 10pF
C38 2pF
C37 22pF
R38 680
C36 2pF
C62 10pF
FILTER SELECT
P/O J3003
N/C
+5V
U1 74LS138
FILTER CONTROL "A"
FILTER CONTROL "B"
R50 4.7K
R48 4.7K
R46 4.7K
R44 4.7K
Q14 2N2222
Q12 2N2222
Q10 2N2222
Q16 2N2222
Q17 2N2222
Q15 2N2222
Q13 2N2222
Q11 2N2222
R51 10K
R49 10K
R47 10K
R45 10K
R41 4.7K
C61 1 35V
C68 1800pF
2/J6
2/J5
220 MHz LPF
2/G6
R39 4.7K
R37 4.7K
L20
L22
L24
L21
L23
L25
R40 680
C40 5pF
C41 2pF
C42 10pF
C43 5pF
CR9 MA47047
CR10 MA47047
CR11 MA47047
CR12 MA47047
R42 680
2/H6



STANDARDS (FIGURE 7-16 AND FIGURE 7-16a):

(UNLESS OTHERWISE NOTED)

1. ALL REF NOS CARRY AN ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES AS FOLLOWS:
   A. MECH ASSY -- 7005-5042-500 (3000)
   B. PC BOARD ASSY #1 -- 7010-5032-400 (2500; E.G., R1 IS R2501)
   C. PC BOARD ASSY #2 -- 7010-5032-600 (2600; E.G., R1 IS R2601)

2. ALL RESISTORS ARE 1/4 W, 5% TOLERANCE.

3. ALL RESISTANCE IS EXPRESSED IN OHMS.

4. ALL CAPACITANCE IS EXPRESSED IN MICROFARADS.

5. ALL INDUCTANCE IS EXPRESSED IN MICROHENRYS.

NOTES (FIGURE 7-16 AND FIGURE 7-16a)

1. NOT USED.

2. NOT USED

3. (DELAY LINE #1) THRU SER. NO. 2232: C70 IS SELECTED AT TEST (SAT) AND MAY OR MAY NOT BE INSTALLED; NOMINAL 3300 PICOFARADS, RANGE 0 PICOFARADS TO 5600 PICOFARADS. SER. NO. 2233 AND ON, C70 SAT NOMINAL 0.01 MICROFARADS RANGE 0 TO 0.01 MICROFARADS.

4. E1-1 THRU E1-9 AND E2-1 THRU E2-4 ARE FLEX STRIP CONNECTIONS BETWEEN BOARDS 1 AND 2.

5. (DELAY LINE #1) THRU SER. NO. 1953, C71 AND R91 WERE NOT USED.

6. (DELAY LINE #2 THRU SER.NO. 1949: CR19 AND CR52 WERE NOT USED; U10 PIN #3 TO GROUND.

7. (DELAY LINE #1) THRU SER. NO. 1930, C12 WAS 33 PICOFARADS, 200V.

8. (DELAY LINE #1) THRU SER. NO. 2111, R70 AND R73 WERE 100K.

9. NOT USED.

10. (DELAY LINE #1) THRU SER. NO. 2533, R12 WAS 1.0K.

11. (DELAY LINE #1) EFFECTIVE SER. NO. 2810 AND ON.

12. (DELAY LINE #2) SER. NO. 2774 AND ON, R51 NOT USED.

Figure 7-16 Delay Line Module Schematic Board #1 (Sheet 1 of 2) 0000-5012-400-H2

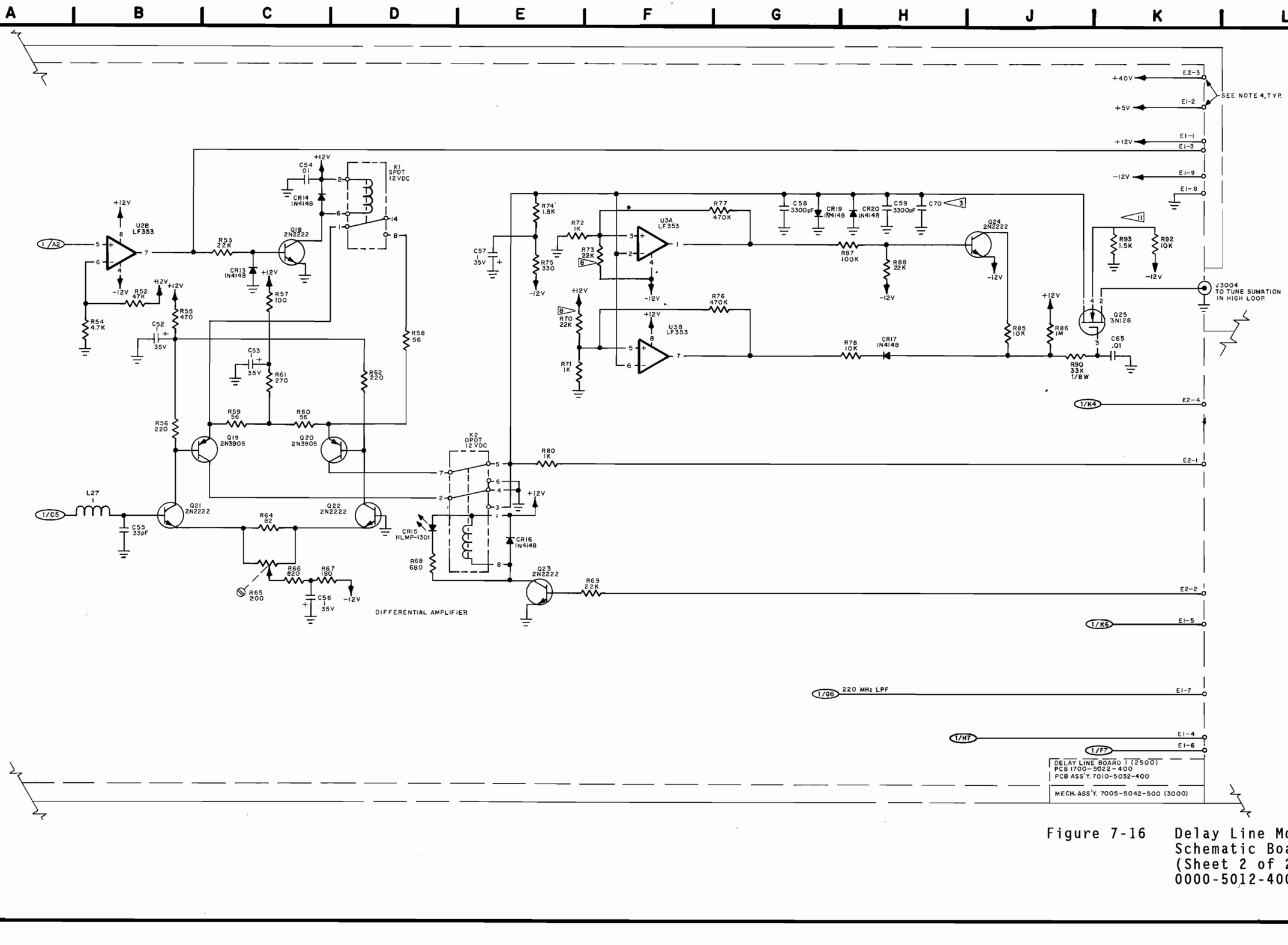


Figure 7-16 Delay Line Module Schematic Board #1 (Sheet 2 of 2) 0000-5012-400-H2

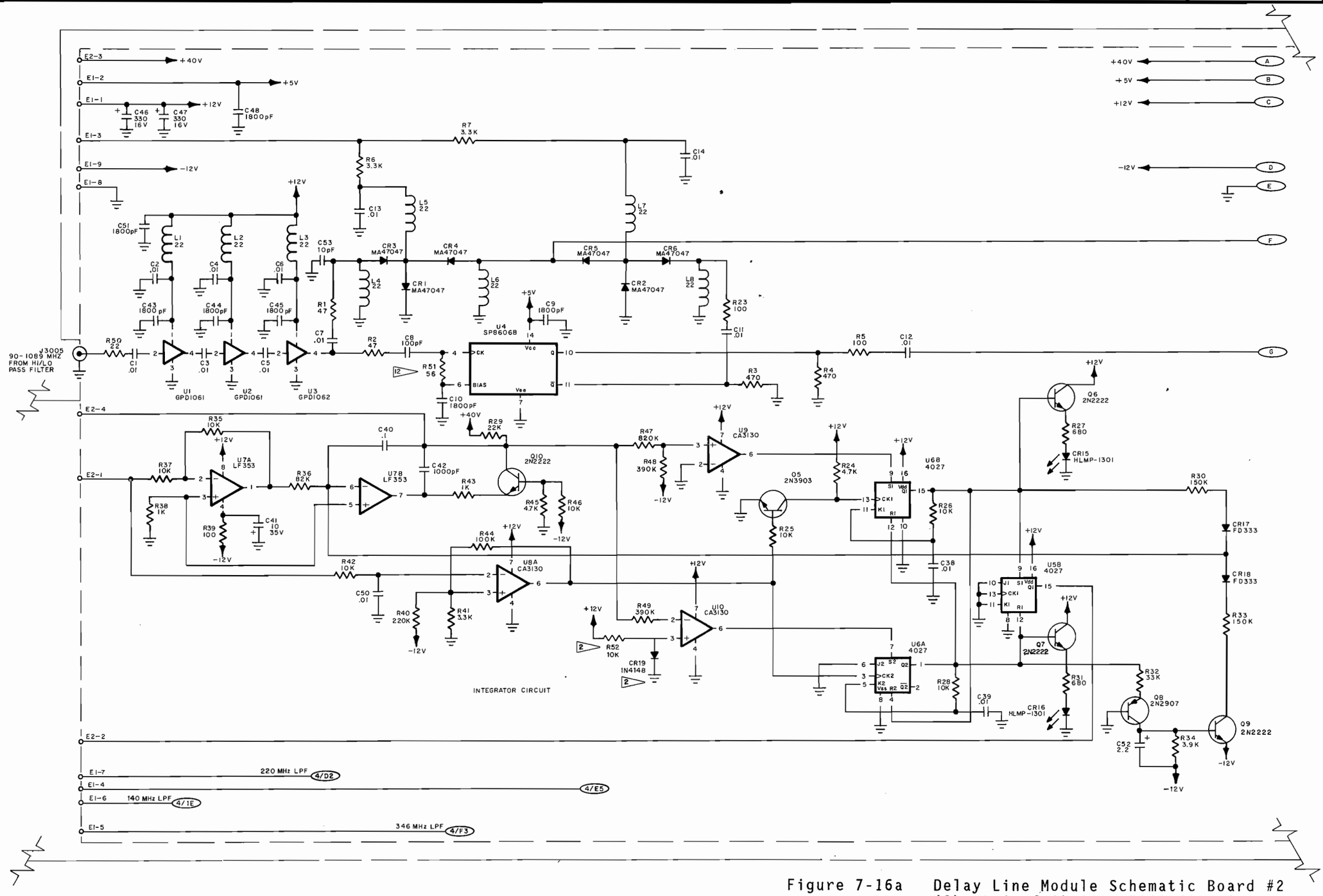


Figure 7-16a Delay Line Module Schematic Board #2 (Sheet 1 of 2) 0000-5012-600-G1

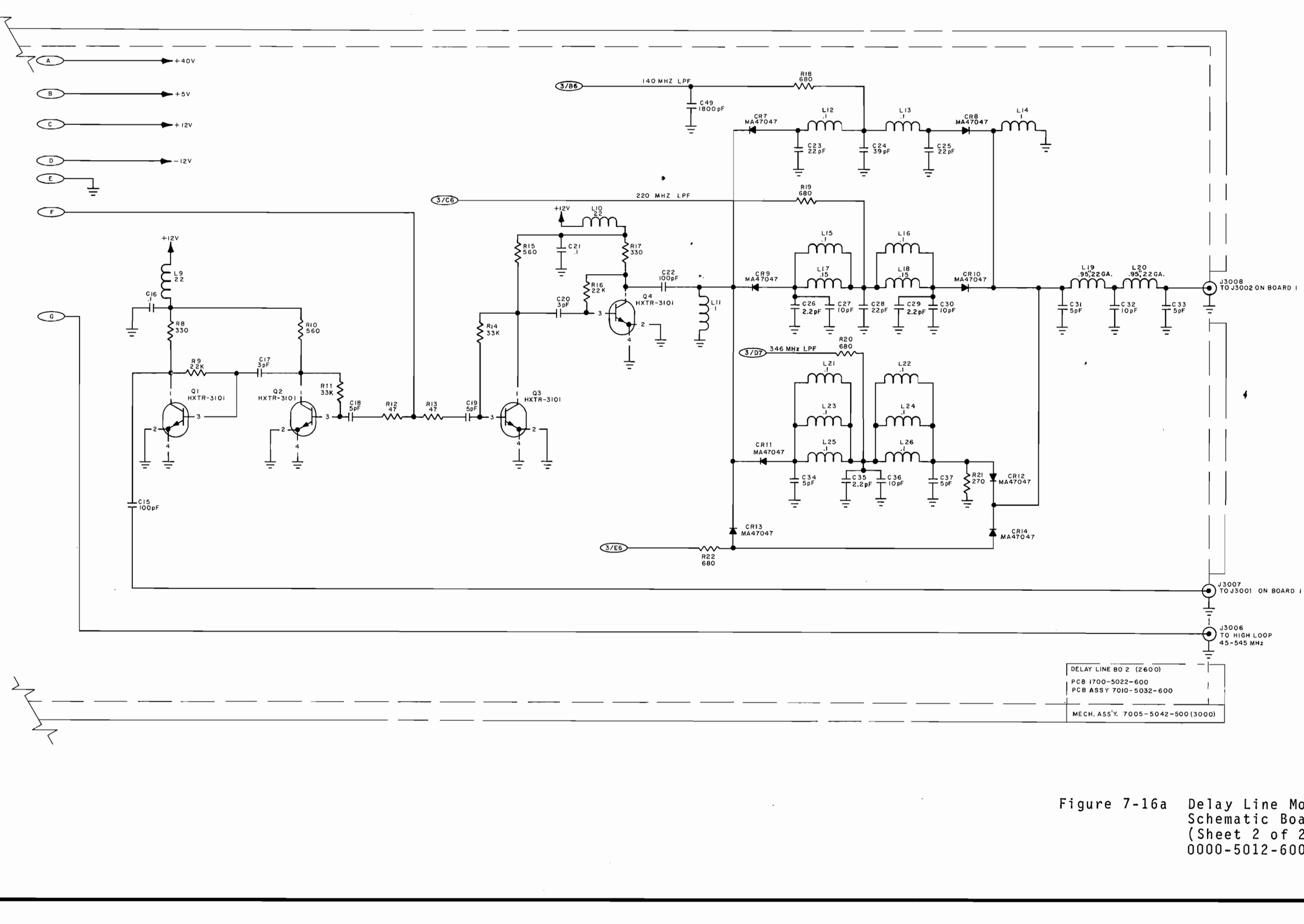
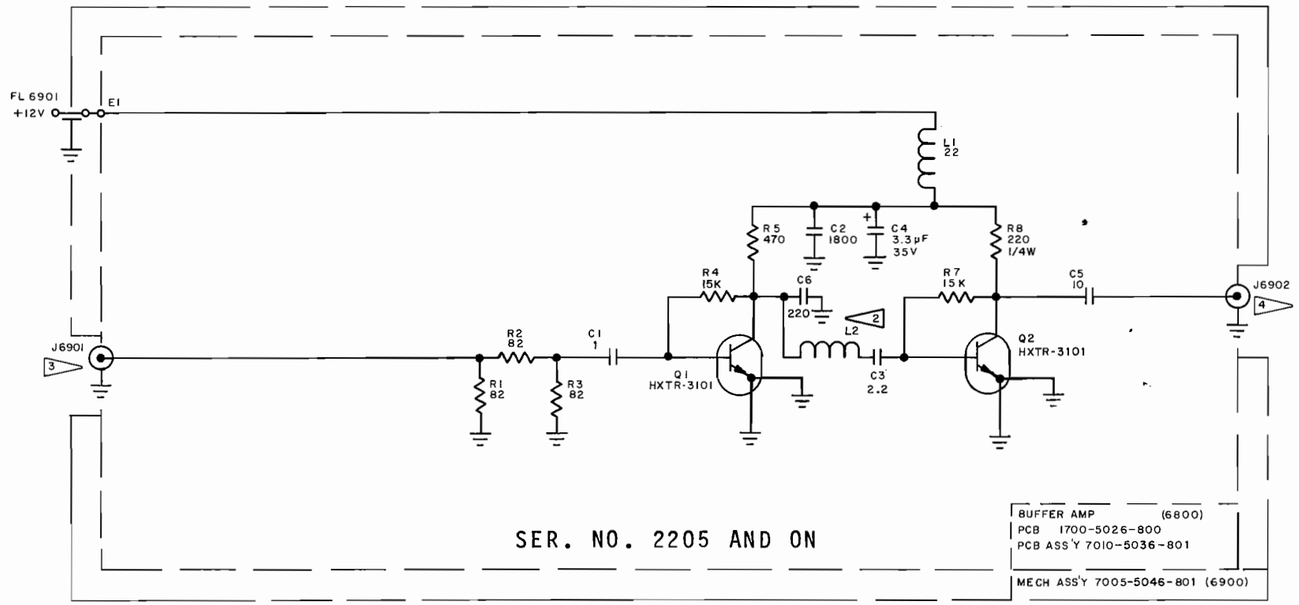
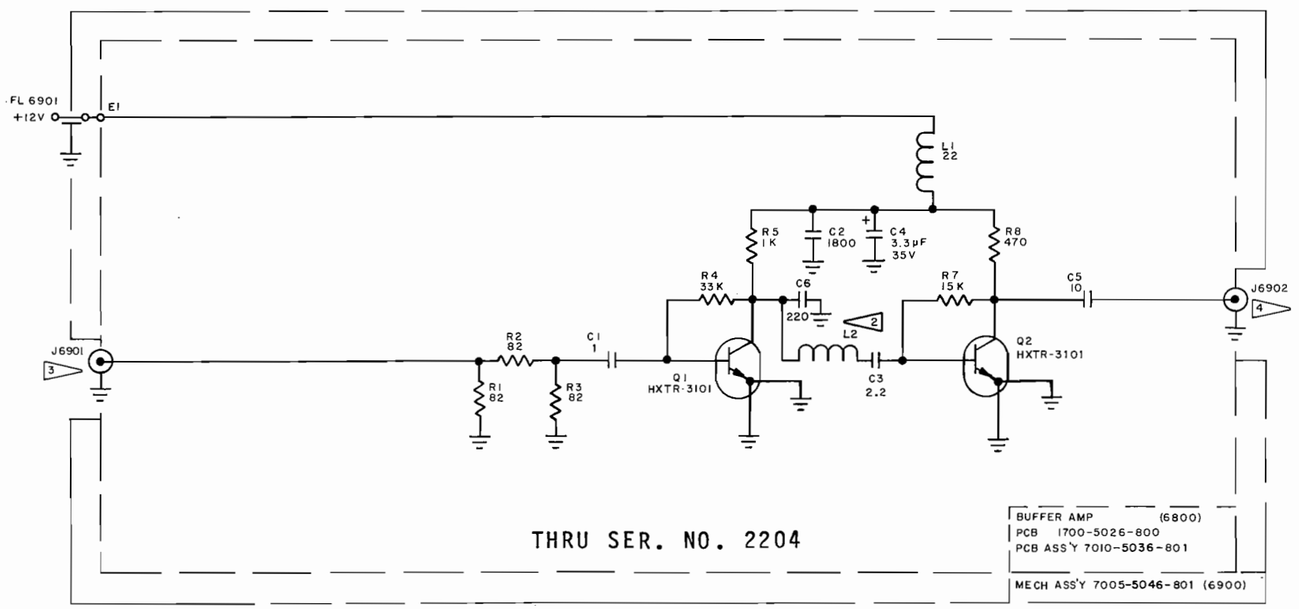


Figure 7-16a Delay Line Module Schematic Board #2 (Sheet 2 of 2) 0000-5012-600-G1





STANDARDS:
(UNLESS OTHERWISE NOTED)

1. ALL REF NOS CARRY AN ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES: 6800 & 6900 (E.G., R1 IS R6801, ETC.)

   A. MECH ASSY 7005-5036-801 (6900)
   B. PCB ASSY 7010-5046-801 (6800)
   C.
   D.

2. ALL RESISTORS ARE 1/8 W, 5% TOLERANCE.

3. ALL RESISTANCE IS EXPRESSED IN OHMS.

4. ALL CAPACITANCE IS EXPRESSED IN PICO-FARADS.

5. ALL INDUCTANCE IS EXPRESSED IN MICRO-HENRY'S.

NOTES:

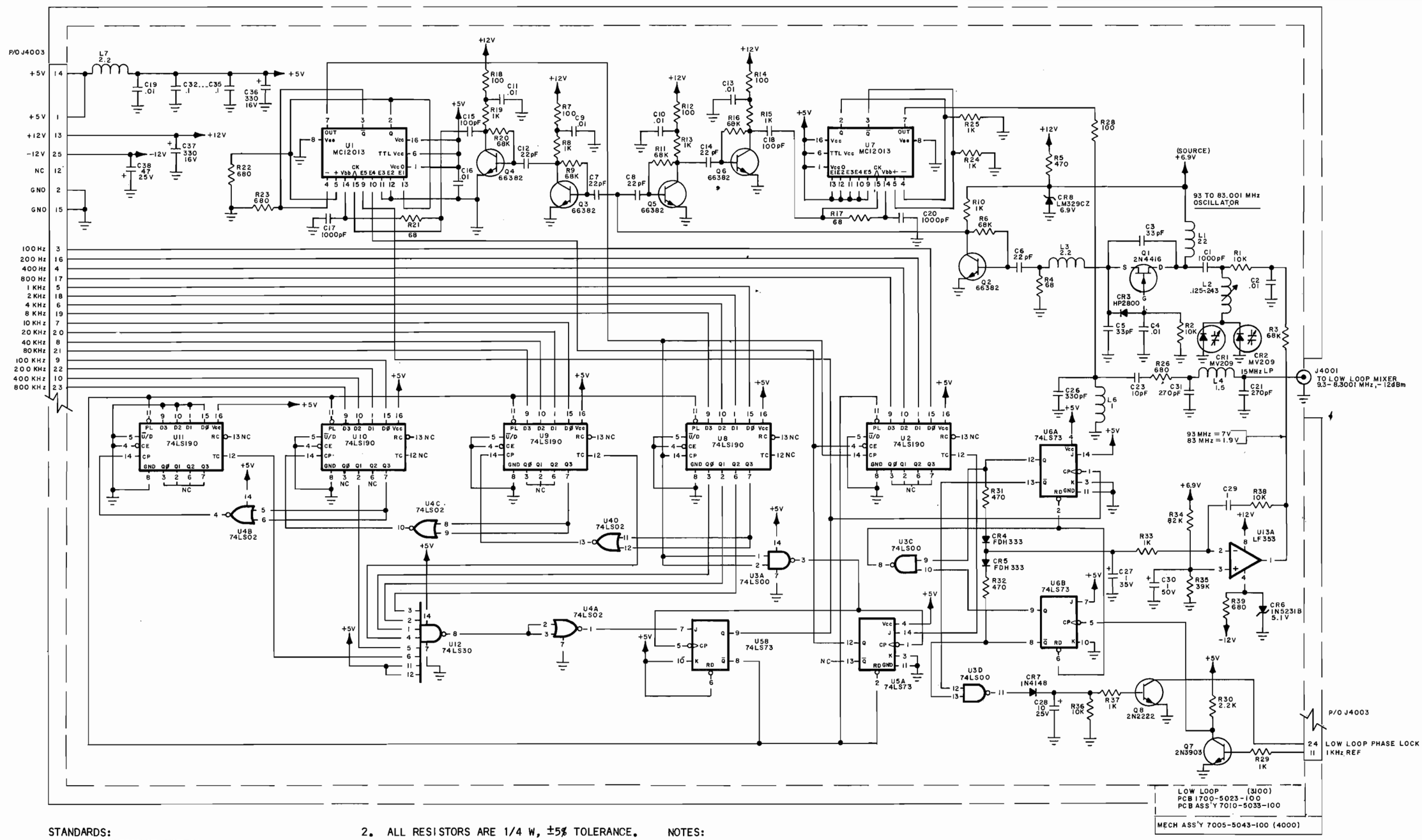
1. LAST REF NOS USED:
   C5, Q2, R8, J6902, L2, FL1

2. L2 IS .35" LEAD LENGTH OF C3.

3. J6901 IS 1300-2300 MHz FROM DUAL VCO FOR BUFFER AMP "A" & 1210 MHz FOR BUFFER AMP "B".

4. J6902 IS 1300-2300 MHz TO 1300 MHz IF GENERATOR FOR BUFFER AMP "A" & 1210 MHz FOR BUFFER AMP "B".

Figure 7-17 Buffer Amp Schematic 0000-5016-801-A2



STANDARDS:
(UNLESS OTHERWISE NOTED)

1. ALL REF NOS CARRY AN ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES: (E.G. R1 IS R3100, ETC.)

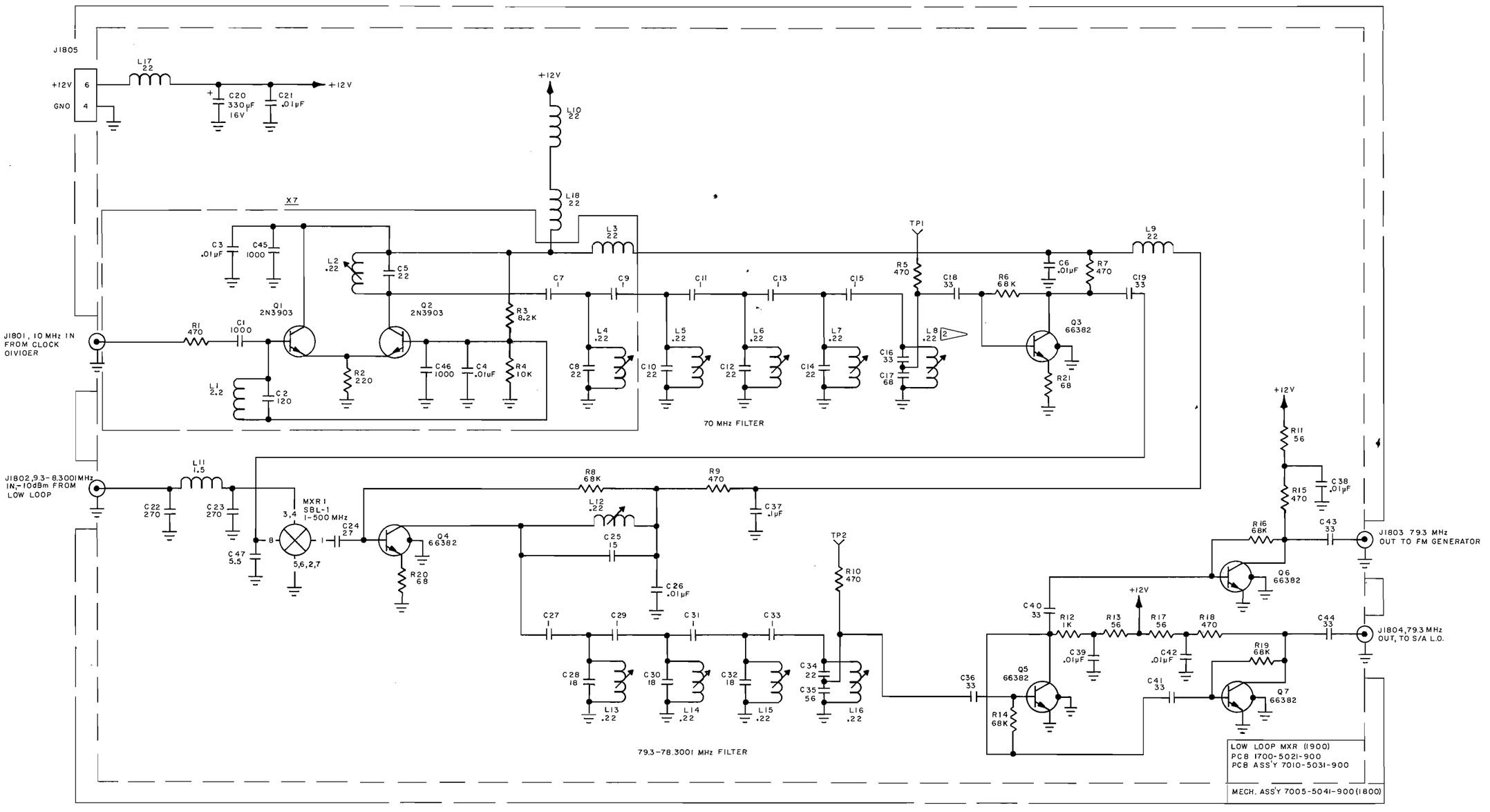
   A. MECH ASSY 7005-5043-100 (4000)
   B. PCB ASSY 7010-5033-100 (3100)

2. ALL RESISTORS ARE 1/4 W, ±5% TOLERANCE.
3. ALL RESISTANCE IS EXPRESSED IN OHMS.
4. ALL CAPACITANCE IS EXPRESSED IN MICROFARADS.
5. ALL INDUCTANCE IS EXPRESSED IN MICROHENRYS.

NOTES:

1. LAST REF NOS USED:
   J3, R39, C38, CR8, L7, Q8, U13
2. REF NOS NOT USED:
   L5, J2, R27, C22, C24, C25

Figure 7-18 Low Loop Module Schematic 0000-5013-100-B2



STANDARDS:
(UNLESS OTHERWISE NOTED)

1. ALL REF NOS CARRY AN ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES: 1900 (E.G., R1 IS R1901, ETC.).

   A. MECH ASSY 7005-5041-900
   B. PCB ASSY 7010-5031-900

2. ALL RESISTORS ARE 1/4 W, 10% TOLERANCE.

3. ALL RESISTANCE IS EXPRESSED IN OHMS.

4. ALL CAPACITANCE IS EXPRESSED IN PICOFARADS.

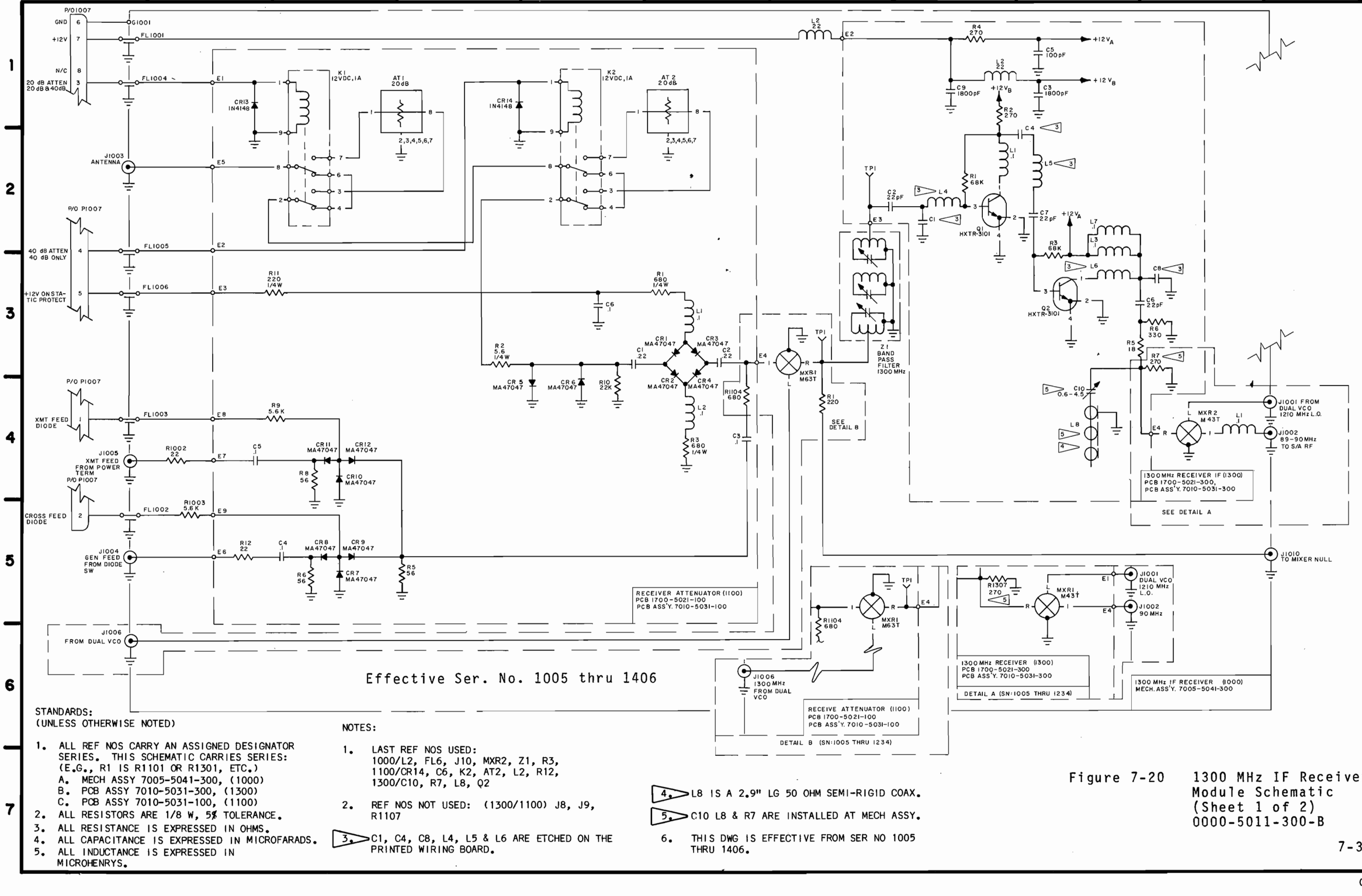
5. ALL INDUCTANCE IS EXPRESSED IN MICROHENRYS.

NOTES:

1. LAST REF NOS USED:
   C47, L18, MXR1, Q7, R21, TP2 & J1805.

2. DETUNE SLIGHTLY AS NECESSARY TO DELETE 80.7 MHz SIGNAL AT TP2.

Figure 7-19 Low Loop Mixer Module Schematic 0000-5011-900-F



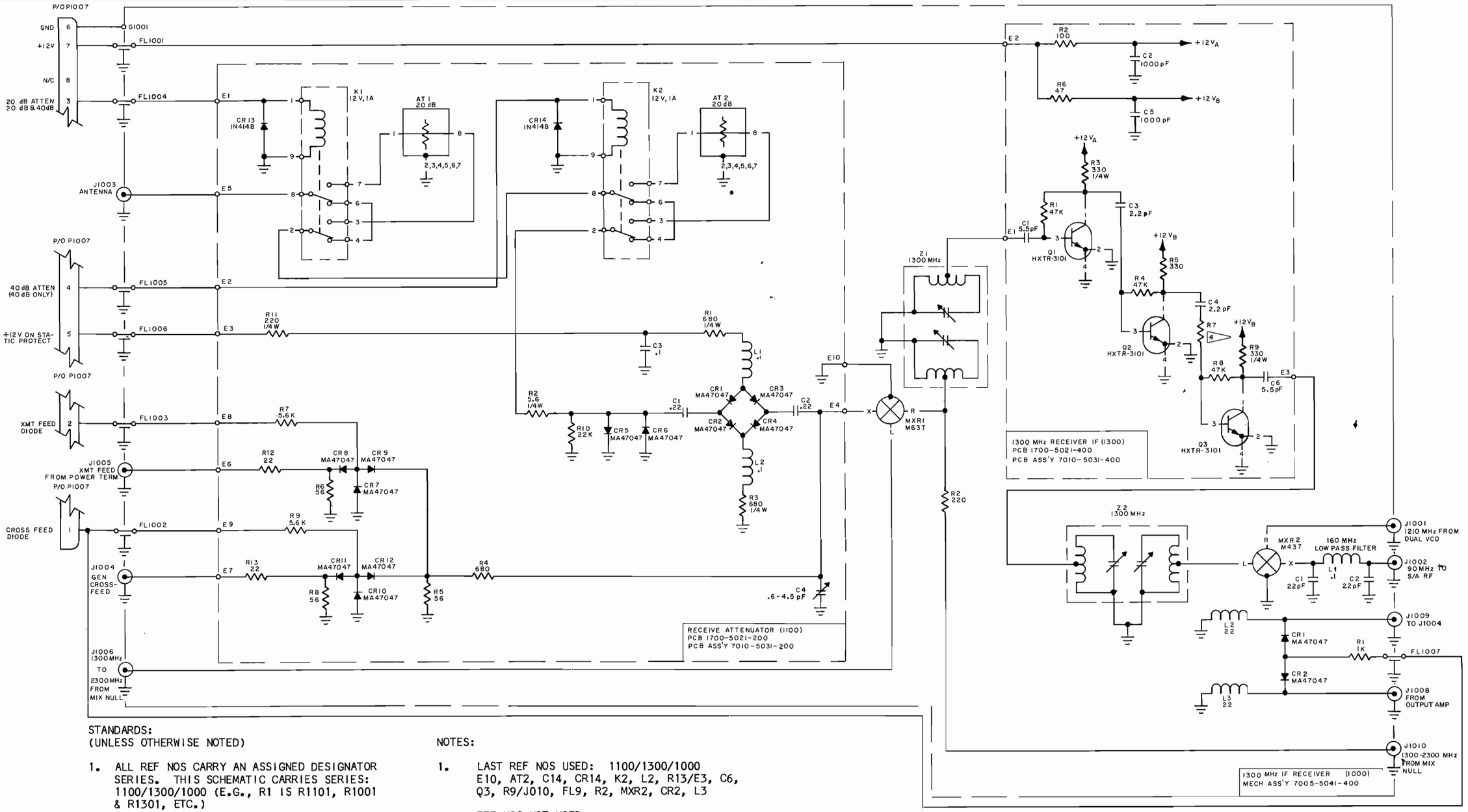
STANDARDS:
(UNLESS OTHERWISE NOTED)

1. ALL REF NOS CARRY AN ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES: (E.G., R1 IS R1101 OR R1301, ETC.)
   A. MECH ASSY 7005-5041-300, (1000)
   B. PCB ASSY 7010-5031-300, (1300)
   C. PCB ASSY 7010-5031-100, (1100)
2. ALL RESISTORS ARE 1/8 W, 5% TOLERANCE.
3. ALL RESISTANCE IS EXPRESSED IN OHMS.
4. ALL CAPACITANCE IS EXPRESSED IN MICROFARADS.
5. ALL INDUCTANCE IS EXPRESSED IN MICROHENRYS.

NOTES:

1. LAST REF NOS USED:
   1000/L2, FL6, J10, MXR2, Z1, R3,
   1100/CR14, C6, K2, AT2, L2, R12,
   1300/C10, R7, L8, Q2
2. REF NOS NOT USED: (1300/1100) J8, J9, R1107
3. C1, C4, C8, L4, L5 & L6 ARE ETCHED ON THE PRINTED WIRING BOARD.
4. L8 IS A 2.9" LG 50 OHM SEMI-RIGID COAX.
5. C10 L8 & R7 ARE INSTALLED AT MECH ASSY.
6. THIS DWG IS EFFECTIVE FROM SER NO 1005 THRU 1406.

Figure 7-20 1300 MHz IF Receiver Module Schematic (Sheet 1 of 2) 0000-5011-300-B



Effective Ser. No. 1407 and ON

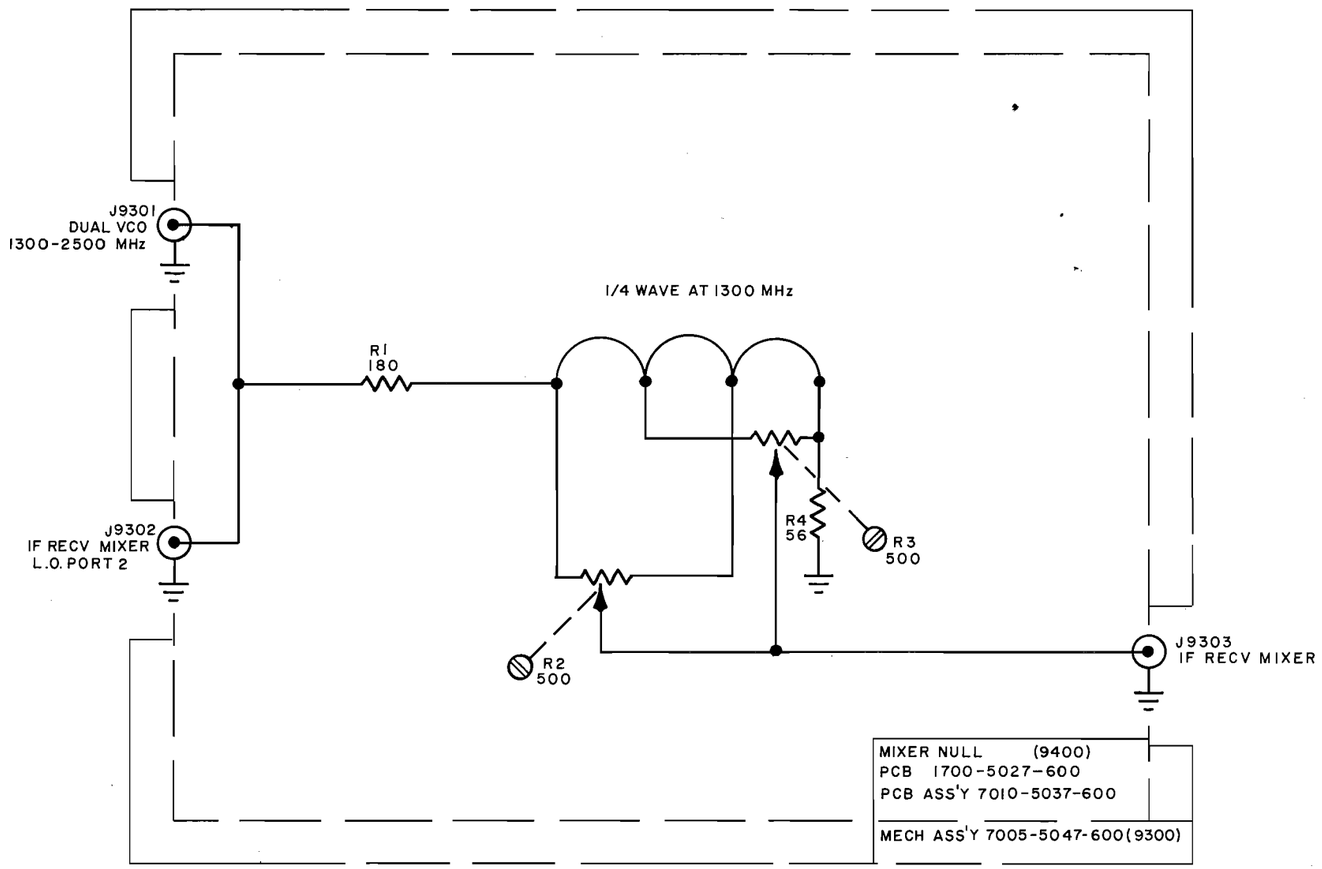
STANDARDS:
(UNLESS OTHERWISE NOTED)

1. ALL REF NOS CARRY AN ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES: 1100/1300/1000 (E.G., R1 IS R1101, R1001 & R1301, ETC.)
   - A. MECH ASSY 7005-5041-400 (1000)
   - B. PCB ASSY 7010-5031-200 (1100)
   - C. PCB ASSY 7010-5031-400 (1300)
2. ALL RESISTORS ARE 1/8 W, ±5% TOLERANCE.
3. ALL RESISTANCE IS EXPRESSED IN OHMS.
4. ALL CAPACITANCE IS EXPRESSED IN MICROFARADS.
5. ALL INDUCTANCE IS EXPRESSED IN MICROHENRYS.

NOTES:

1. LAST REF NOS USED: 1100/1300/1000 E10, AT2, C14, CR14, K2, L2, R13/E3, C6, Q3, R9/J010, FL9, R2, MXR2, CR2, L3
2. REF NOS NOT USED: J1007, P1001-P1006
3. THIS DWG IS EFFECTIVE FROM SER NO 1407 & ON.
4. R1307 IS SET AT TEST (SAT)
   NOMINAL = 0 OHMS
   RANGE = 0 TO 100 OHMS
   WHEN NOMINAL VALUE IS APPLICABLE, USE 26 AWG BUS WIRE WITH 26 AWG TEFLON SLEEVING AS A JUMPER.

Figure 7-20a 1300 MHz IF Receiver Module Schematic (Sheet 2 of 2) 0000-5011-400-G



STANDARDS:
(UNLESS OTHERWISE NOTED)

1. ALL REF NOS CARRY AN ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES: 9400 PC AND 9300 MECH (E.G., R1 IS R9301, ETC.).

   A. MECH ASS'Y. 7005-5047-600
   B. PCB ASS'Y. 7010-5037-600
   C.
   D.

2. ALL RESISTORS ARE 1/8 W, 5% TOLERANCE.

3. ALL RESISTANCE IS EXPRESSED IN OHMS.

4. ALL CAPACITANCE IS EXPRESSED IN MICROFARADS.

5. ALL INDUCTANCE IS EXPRESSED IN MICROHENRYS.

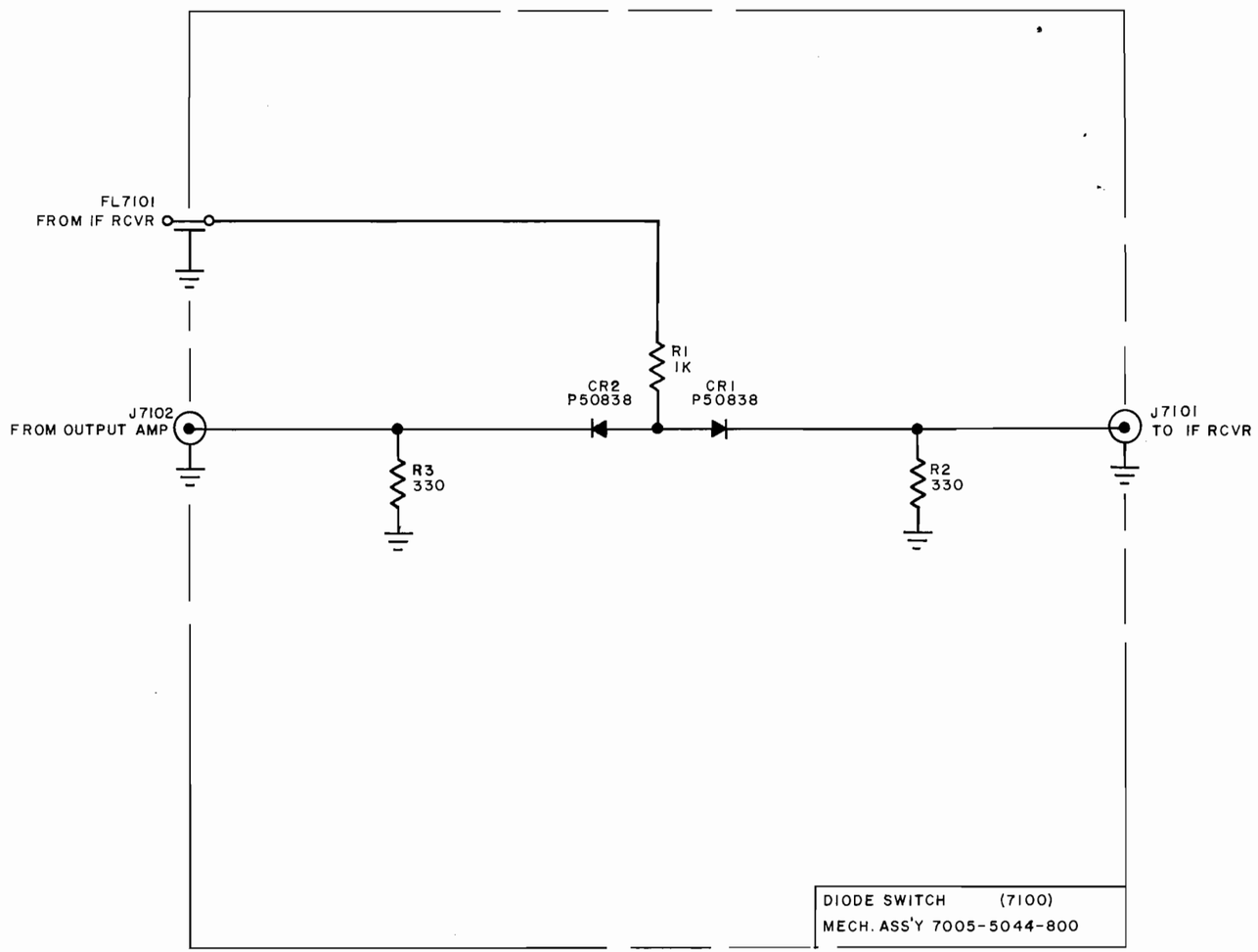
NOTES:

1. LAST REF NOS USED:
   R4, J3

2. CRITICAL LENGTH CONDUCTOR: 1/4 WAVE AT 1300 MHz.

3. THE MIXER NULL WAS ADDED TO ALL UNITS FROM SER NO 1235 AND ON.

Figure 7-21 Mixer Null Module Schematic 0000-5017-600-A1



STANDARDS:
(UNLESS OTHERWISE NOTED)

1. ALL REF NOS CARRY AN ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES: 7100 (E.G., R1 IS R7101, ETC.).

   A. MECH ASS'Y. 7005-5044-800
   B. PCB ASS'Y
   C.
   D.

2. ALL RESISTORS ARE 1/8 W, 5% TOLERANCE.

3. ALL RESISTANCE IS EXPRESSED IN OHMS.

4. ALL CAPACITANCE IS EXPRESSED IN MICROFARADS.

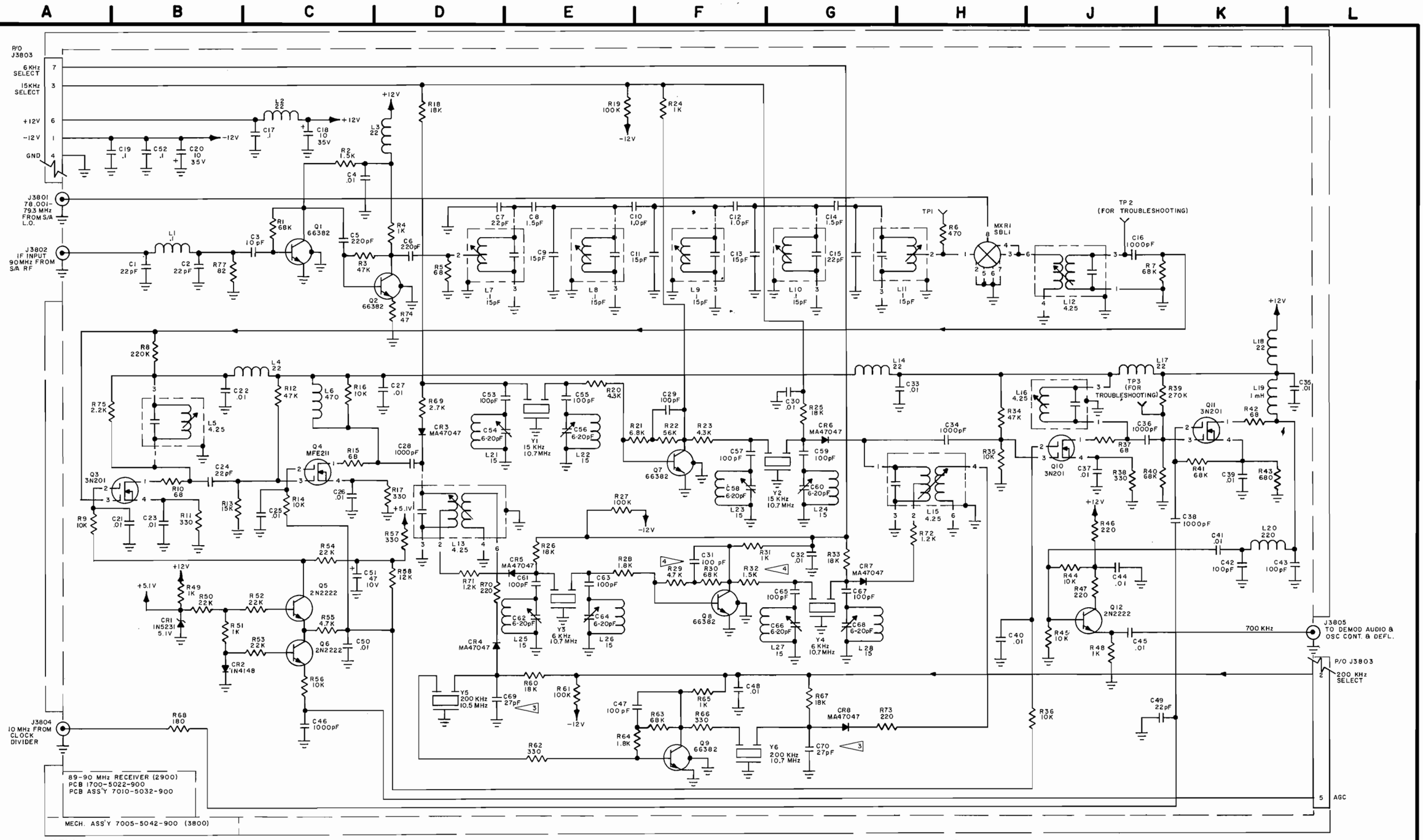
5. ALL INDUCTANCE IS EXPRESSED IN MICROHENRYS.

NOTES:

1. LAST REF NOS USED:
   R3, FL1, J2, CR2

2. EFFECTIVE S/N: 1005 THRU 1406. THE DIODE SWITCH FROM SER NO 1407 AND ON IS INCORPORATED IN THE 1300 MHz IF RCVR, (REF SCHEMATIC 0000-5011-400).

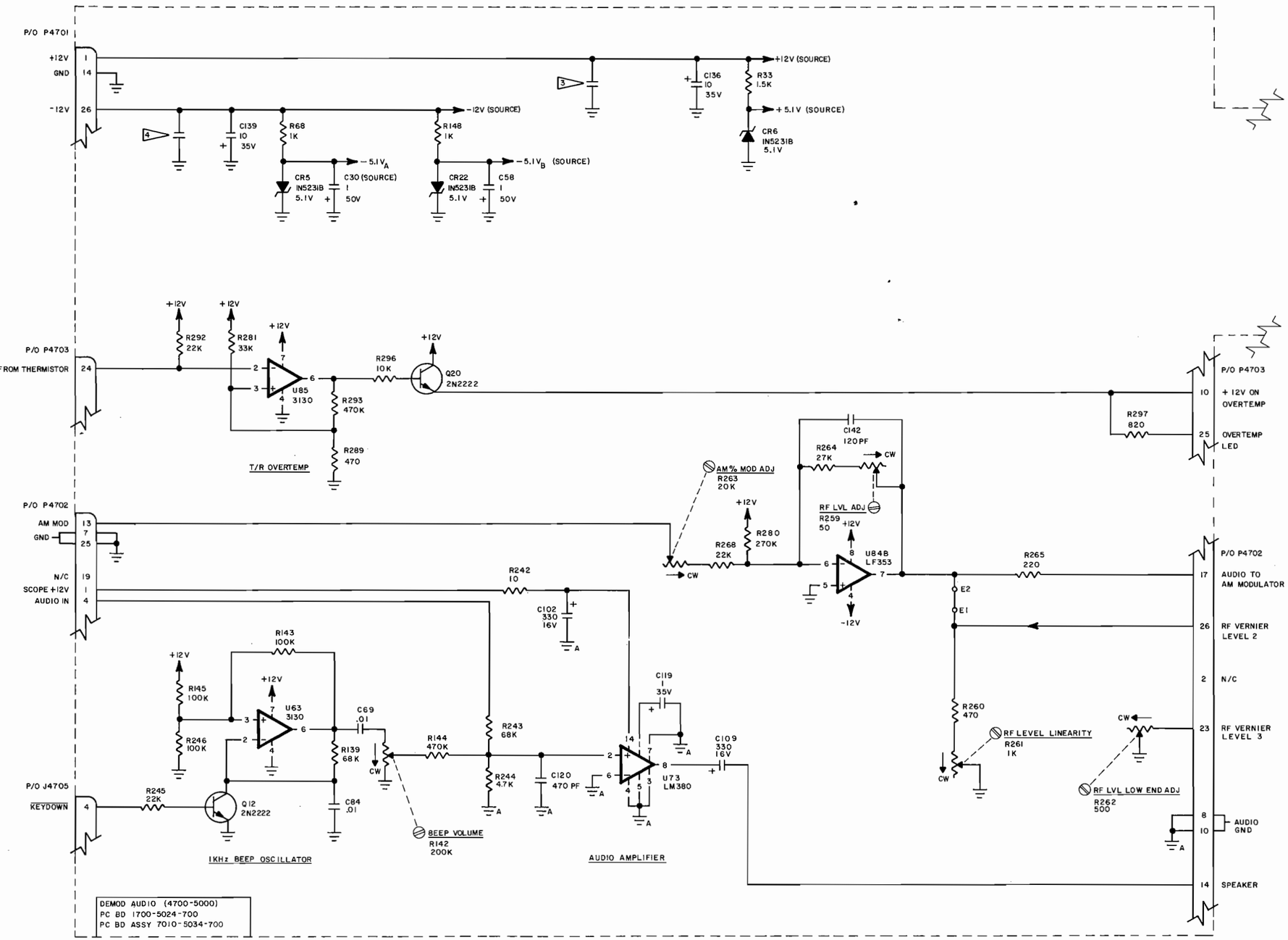
Figure 7-22 Diode Switch Schematic 0000-5014-800-A



NOTES:

1. ALL REF NOS CARRY AN ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARREIS SERIES 2900 and 3800.
   - A. MECH ASSY, 7005-5042-900 (3800) (E.G., R1 IS R3801)
   - B. PC BOARD ASSY, 7010-5032-900 (2900) (E.G., R1 IS R2901)
2. NOT USED
3. EFFECTIVE SER. NO. 2467 AND ON.
4. THRU SER. NO. 2466, R29 WAS 2.7K R32 WAS 1.8K.

Figure 7-23 89-90 MHz Receiver Module Schematic 0000-5012-900-G1



STANDARDS:
(UNLESS OTHERWISE NOTED)

1. ALL REF NOS CARRY AN ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES 4700 (E.G., R1 IS R4701, R101 IS R4801, R201 IS R4901, R301 IS R5001).
2. ALL RESISTORS ARE 1/8 W, 5%.
3. ALL RESISTANCE IS EXPRESSED IN OHMS.
4. ALL CAPACITANCE IS EXPRESSED IN MICROFARADS.
5. ALL INDUCTANCE IS EXPRESSED IN MICROHENRYS.

NOTES:

1. LAST REF NOS USED:
   J3, U86, Q24, C143, E2, R807, CR46, L5, P3
2. REF NOS NOT USED:
   R266, R267, R269, R43

3. 0.1 µF CAPACITORS ON +12V LINE INCLUDE: C4, C7, C13, C14, C15, C35, C36, C37, C38, C40, C41, C42, C48, C50, C51, C53, C56, C79, C81, C83, C85, C86, C88, C92, C93, C125, C127, C130, C132, C10

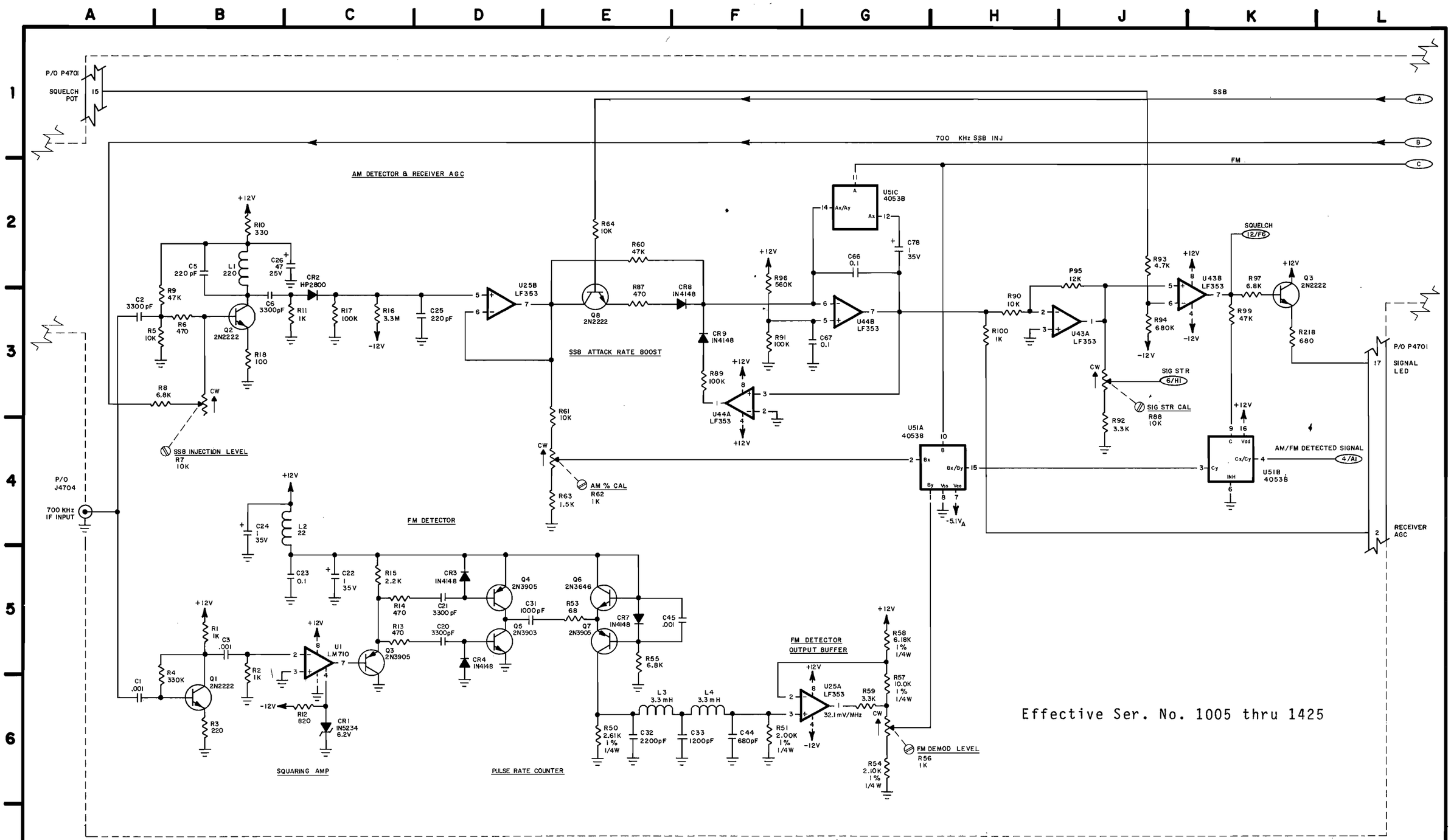
4. 0.1 µF CAPACITORS ON -12V LINE INCLUDE: C34, C52, C54, C80, C82, C87, C89, C90, C126, C131, C139

5. IC FUNCTIONS NOT USED:
   U58A, U67B, U84A

6. EFFECTIVE FM/AM-1500 SN: 1005 THRU 1425

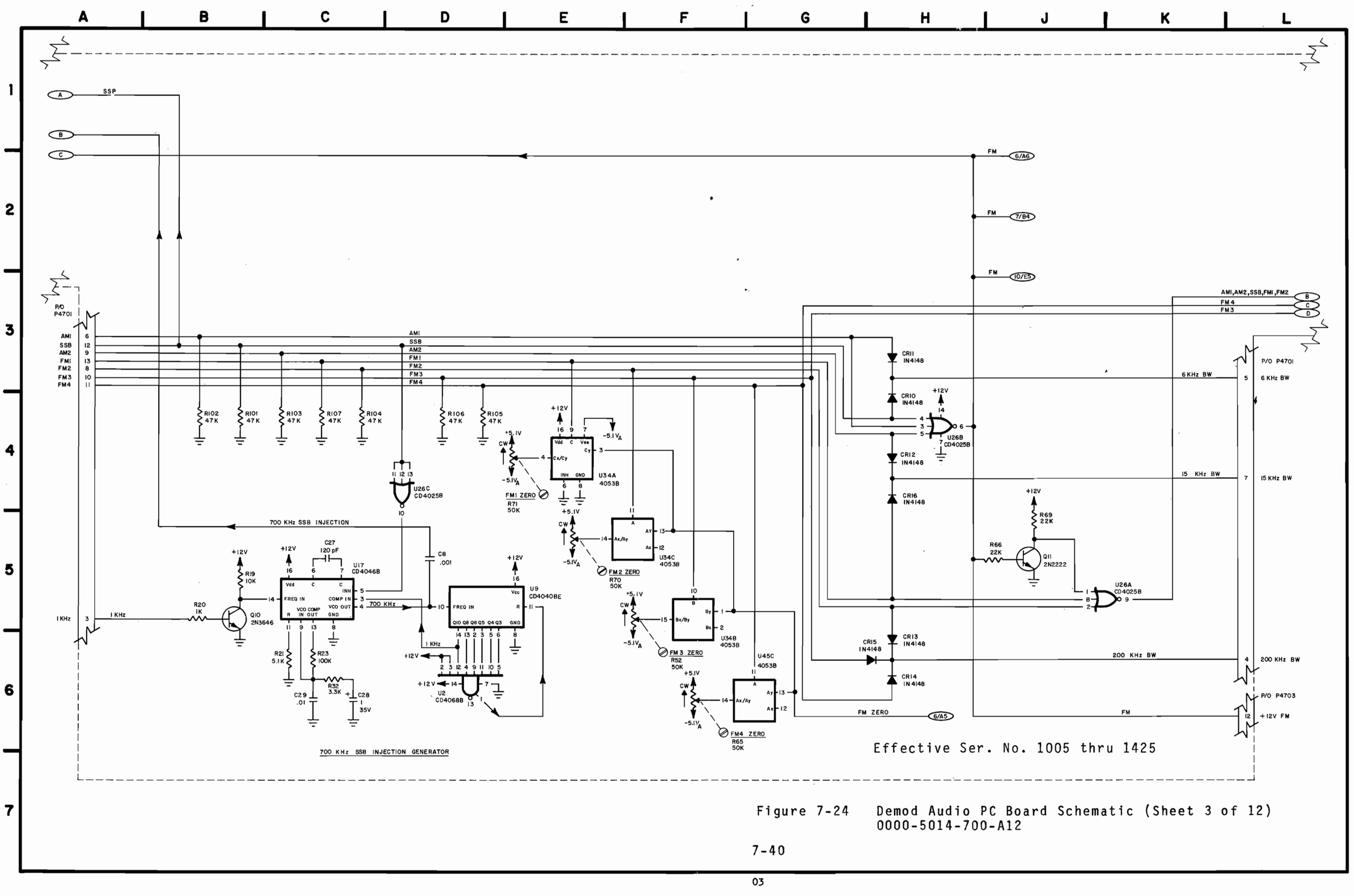
Effective Ser. No. 1005 thru 1425

Figure 7-24 Demod Audio PC Board Schematic (Sheet 1 of 12)
0000-5014-700-A12



Effective Ser. No. 1005 thru 1425

Figure 7-24 Demod Audio PC Board Schematic (Sheet 2 of 12) 0000-5014-700-A12

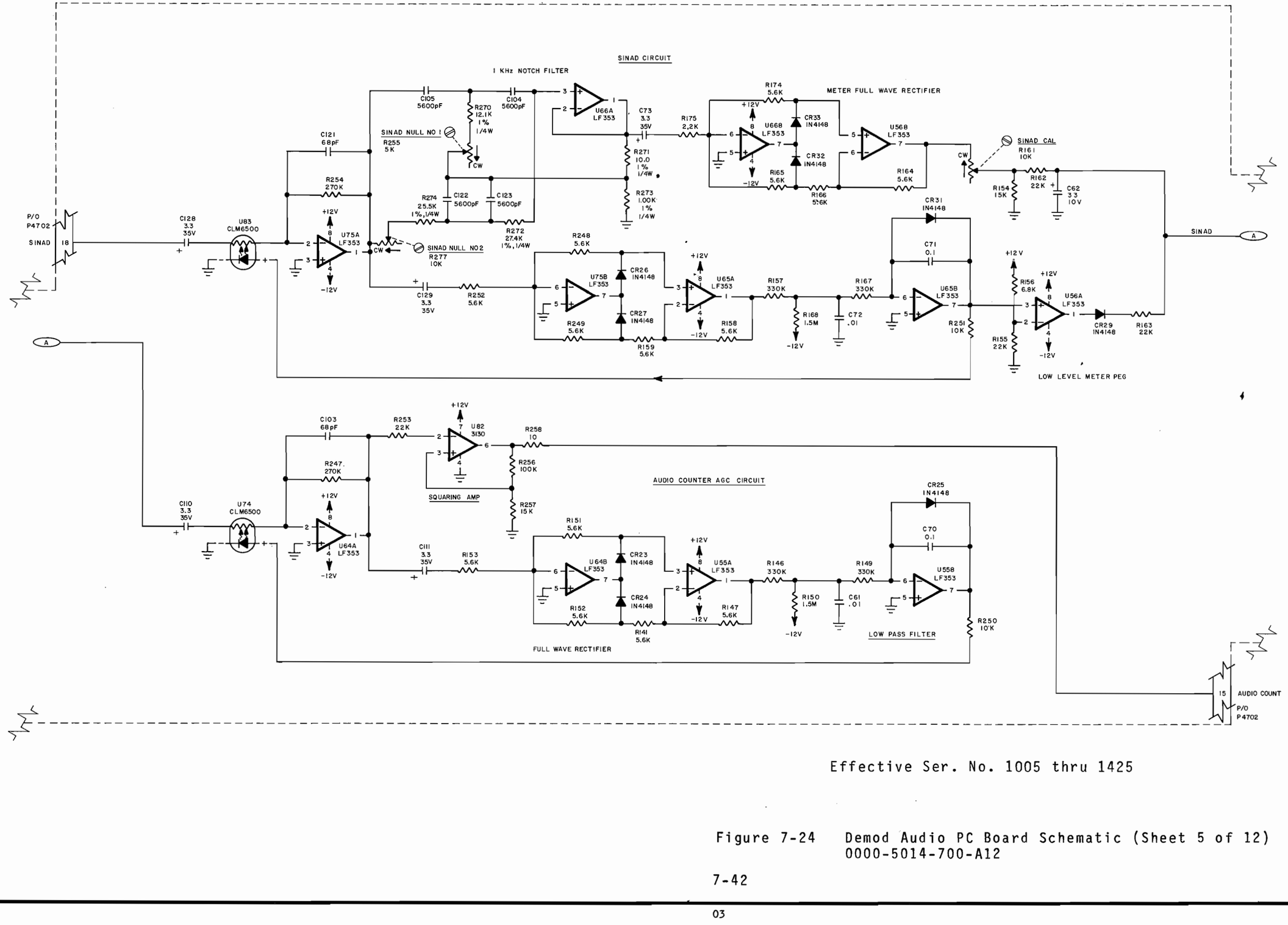


Effective Ser. No. 1005 thru 1425

Figure 7-24 Demod Audio PC Board Schematic (Sheet 3 of 12)
0000-5014-700-A12

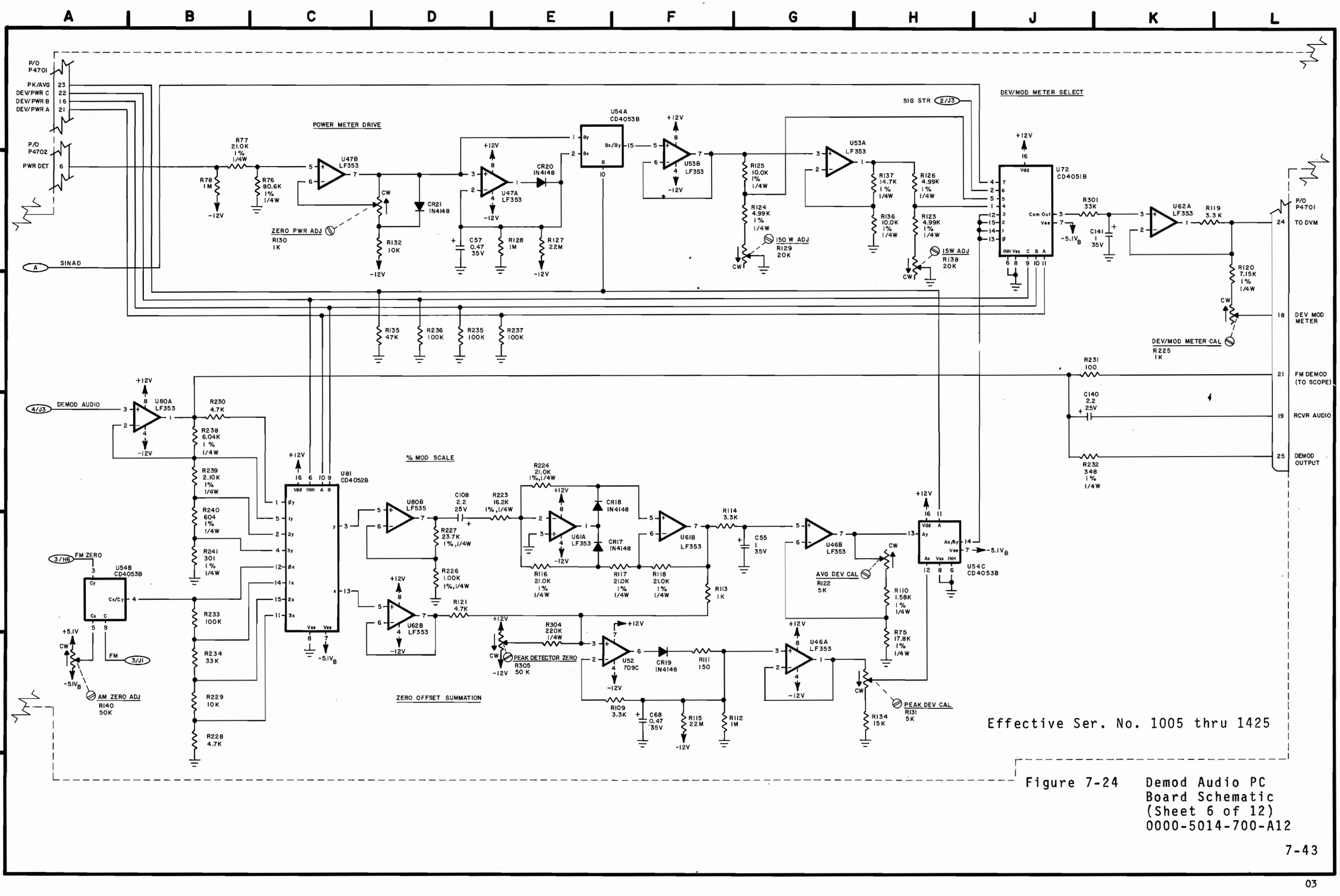
Effective Ser. No. 1005 thru 1425

Figure 7-24 Demod Audio PC Board Schematic (Sheet 4 of 12) 0000-5014-700-A12



Effective Ser. No. 1005 thru 1425

Figure 7-24 Demod Audio PC Board Schematic (Sheet 5 of 12)
0000-5014-700-A12



Effective Ser. No. 1005 thru 1425

Figure 7-24 Demod Audio PC Board Schematic (Sheet 6 of 12) 0000-5014-700-A12

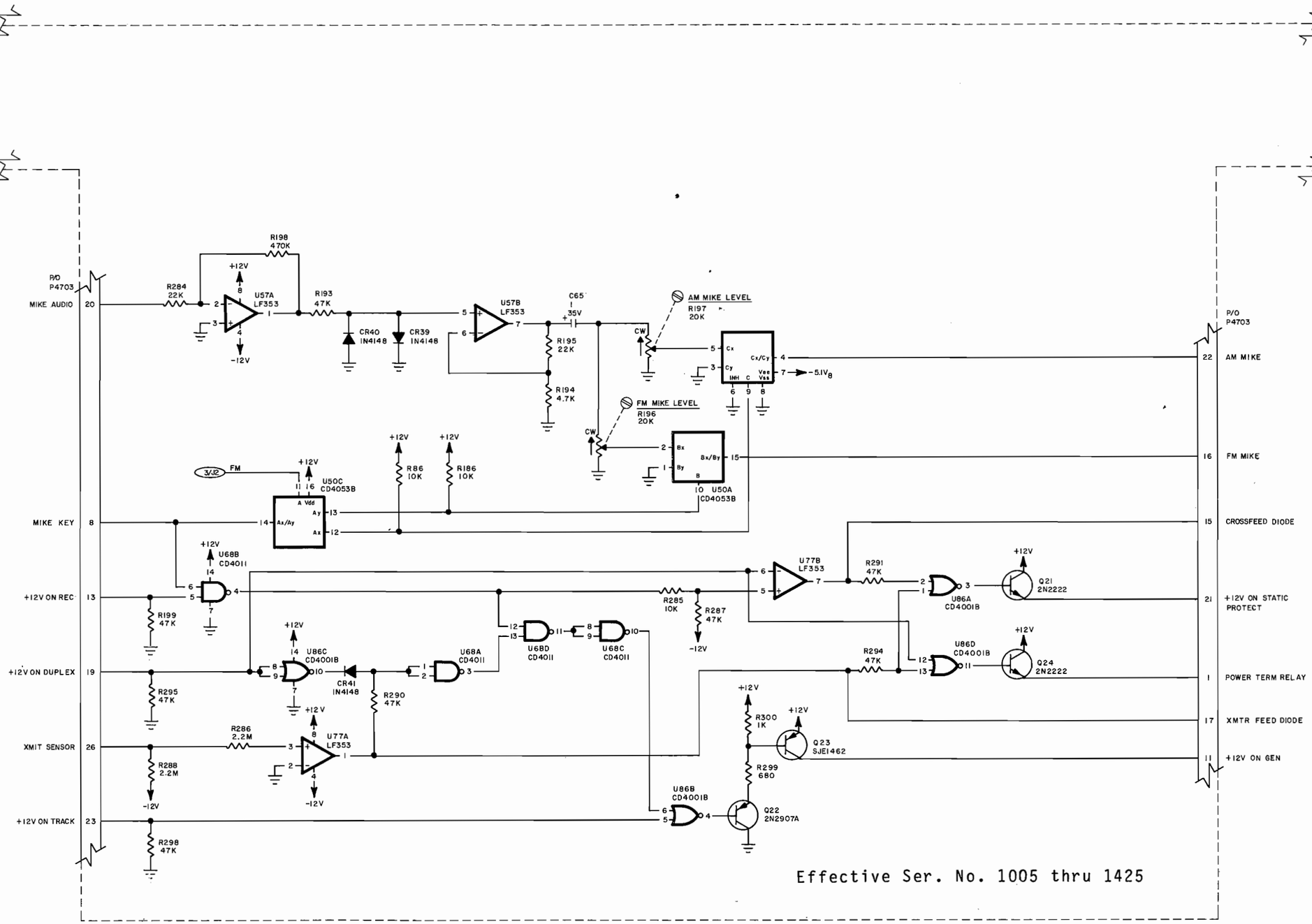
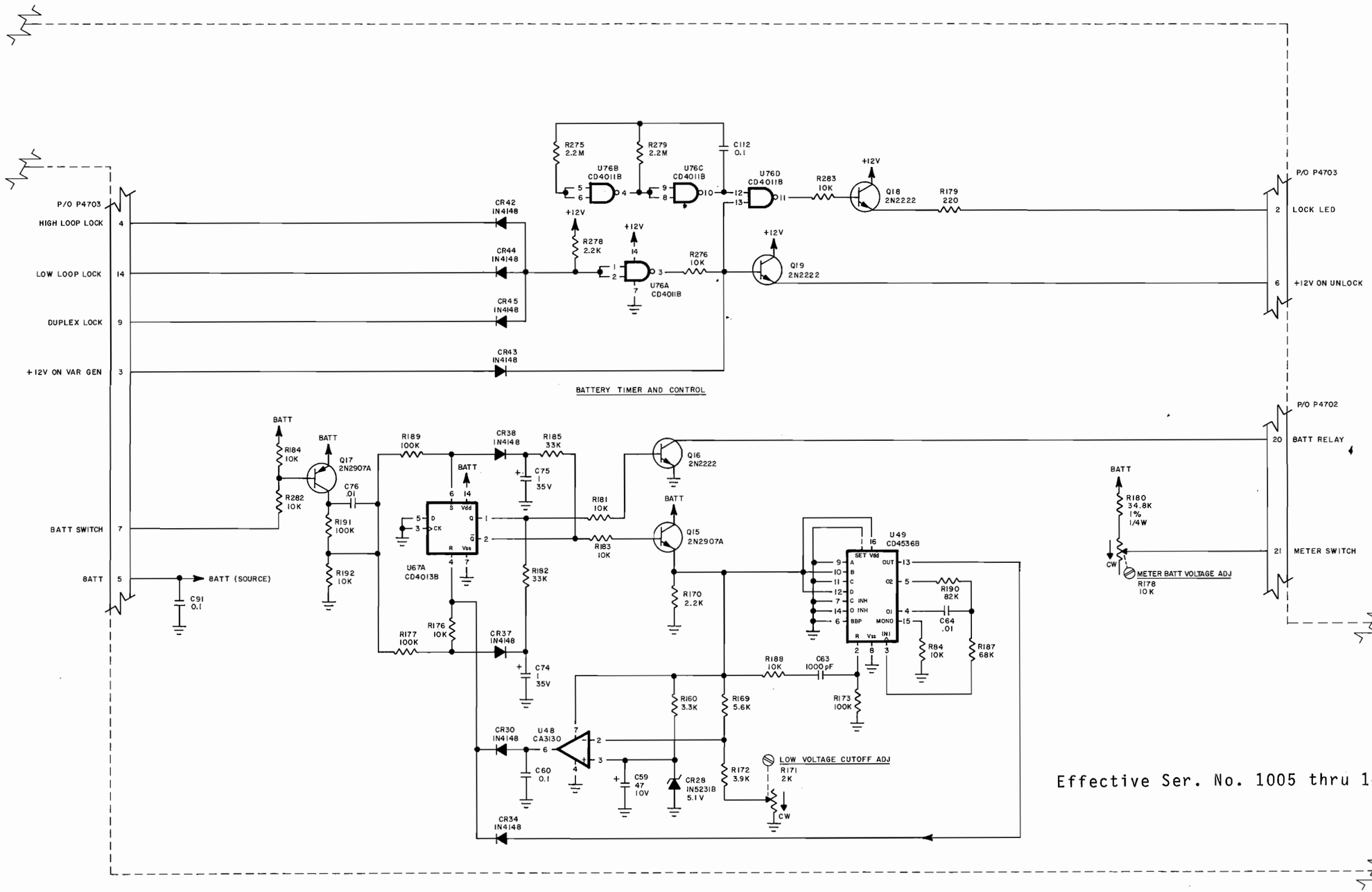
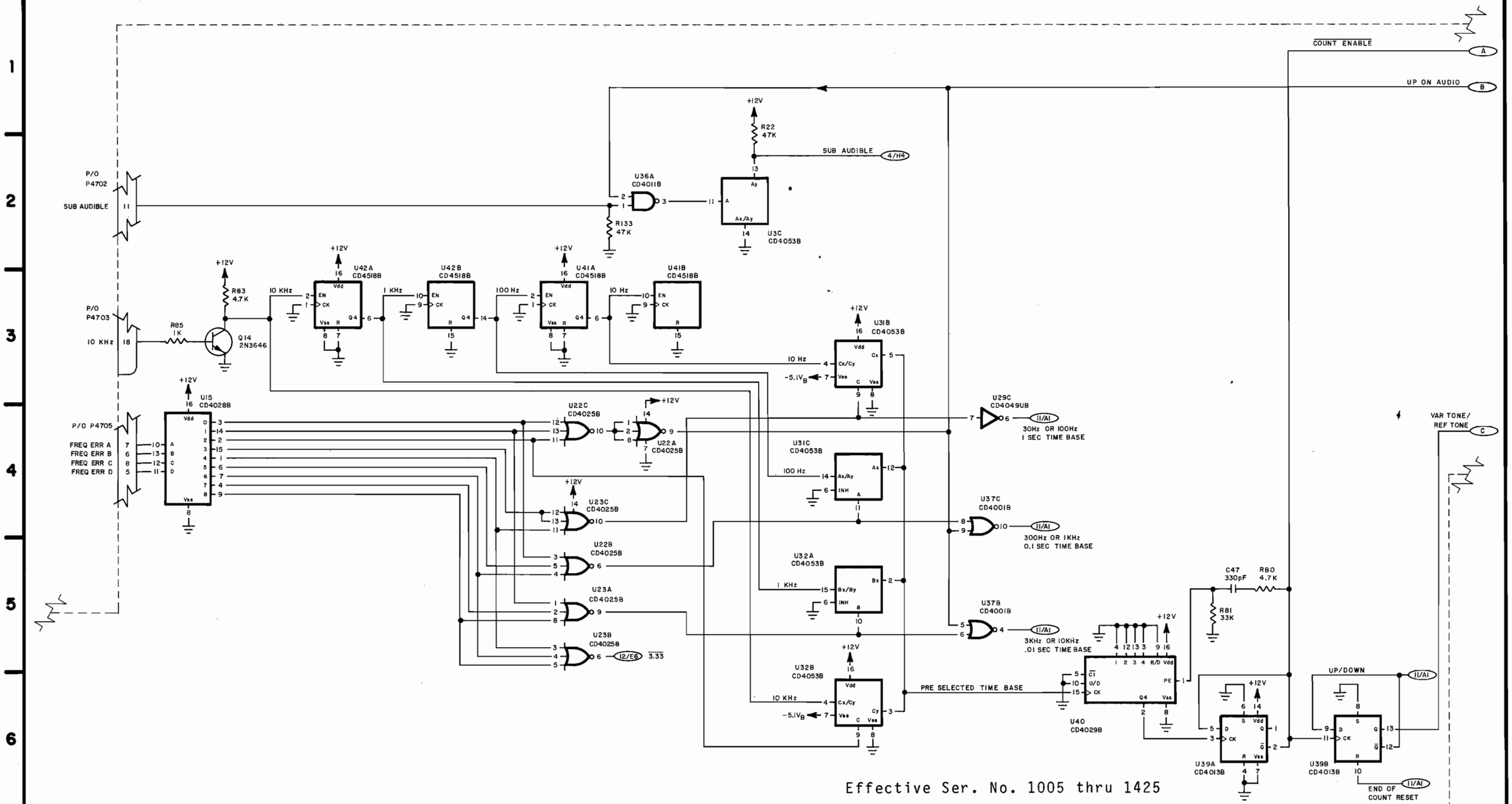


Figure 7-24 Demod Audio PC Board Schematic (Sheet 7 of 12)
0000-5014-700-A12



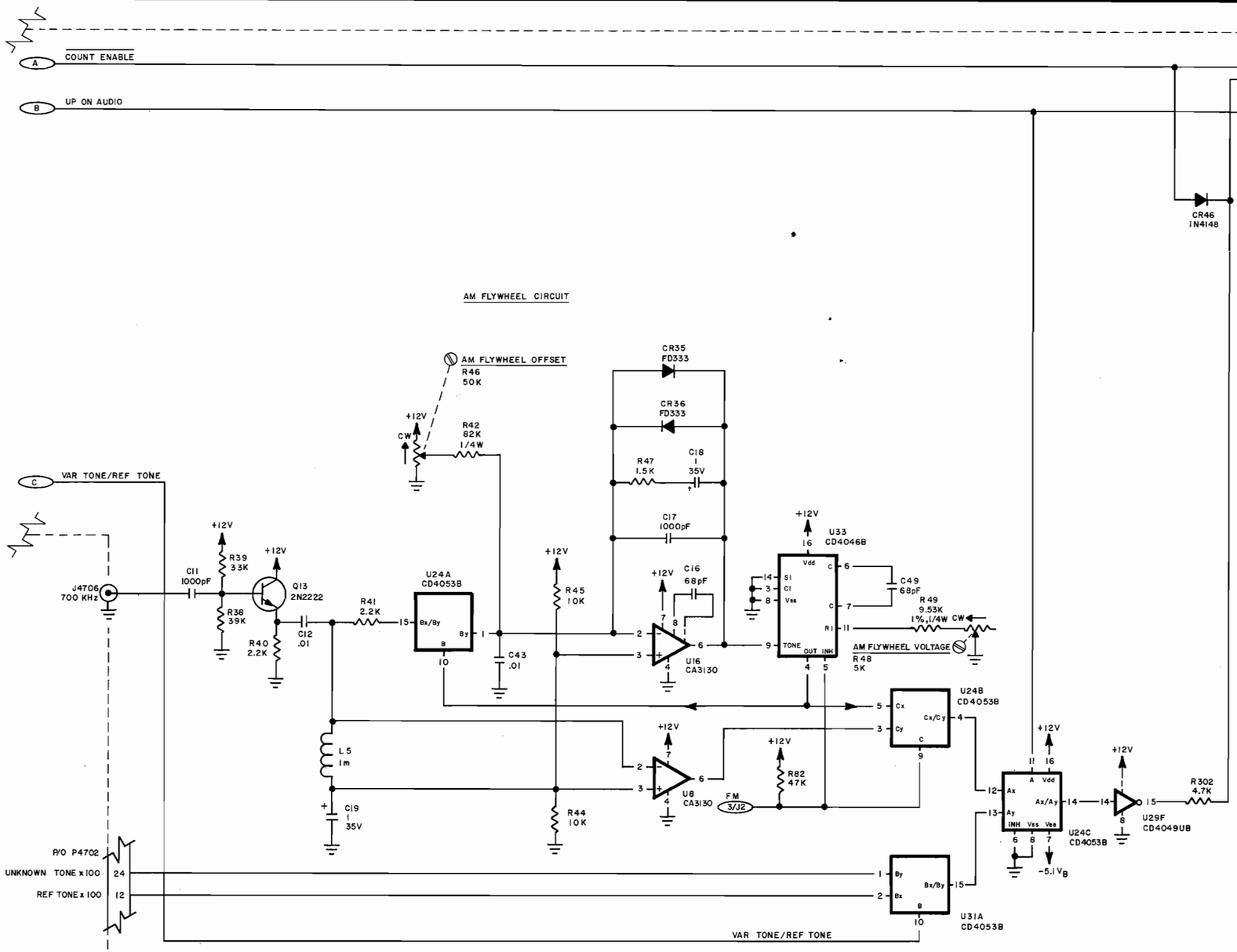
Effective Ser. No. 1005 thru 1425

Figure 7-24 Demod Audio PC Board Schematic (Sheet 8 of 12) 0000-5014-700-A12



Effective Ser. No. 1005 thru 1425

Figure 7-24 Demod Audio PC Board Schematic (Sheet 9 of 12)
0000-5014-700-A12



Effective Ser. No. 1005 thru 1425

Figure 7-24 Demod Audio PC Board Schematic (Sheet 10 of 12) 0000-5014-700-A12

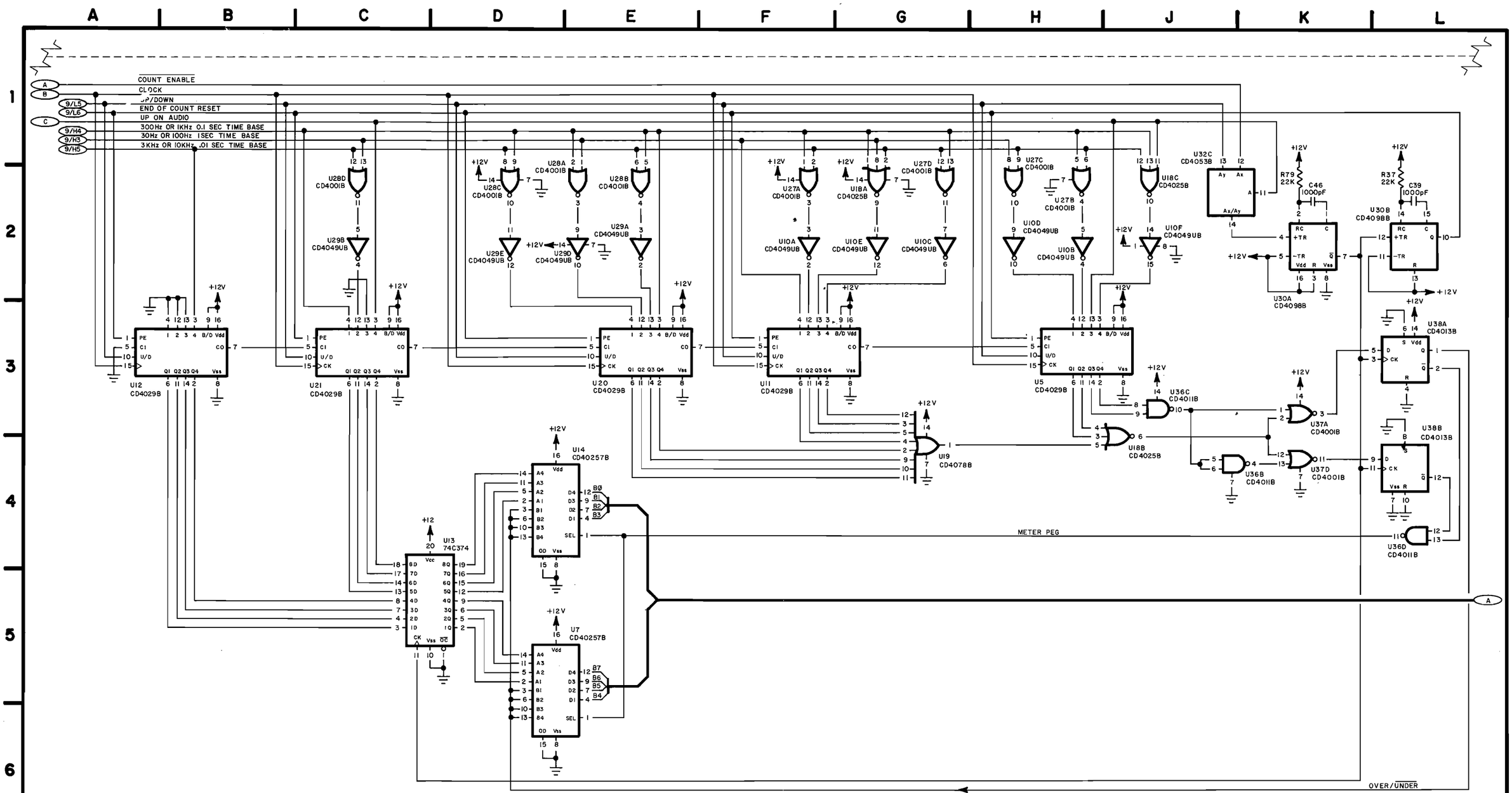
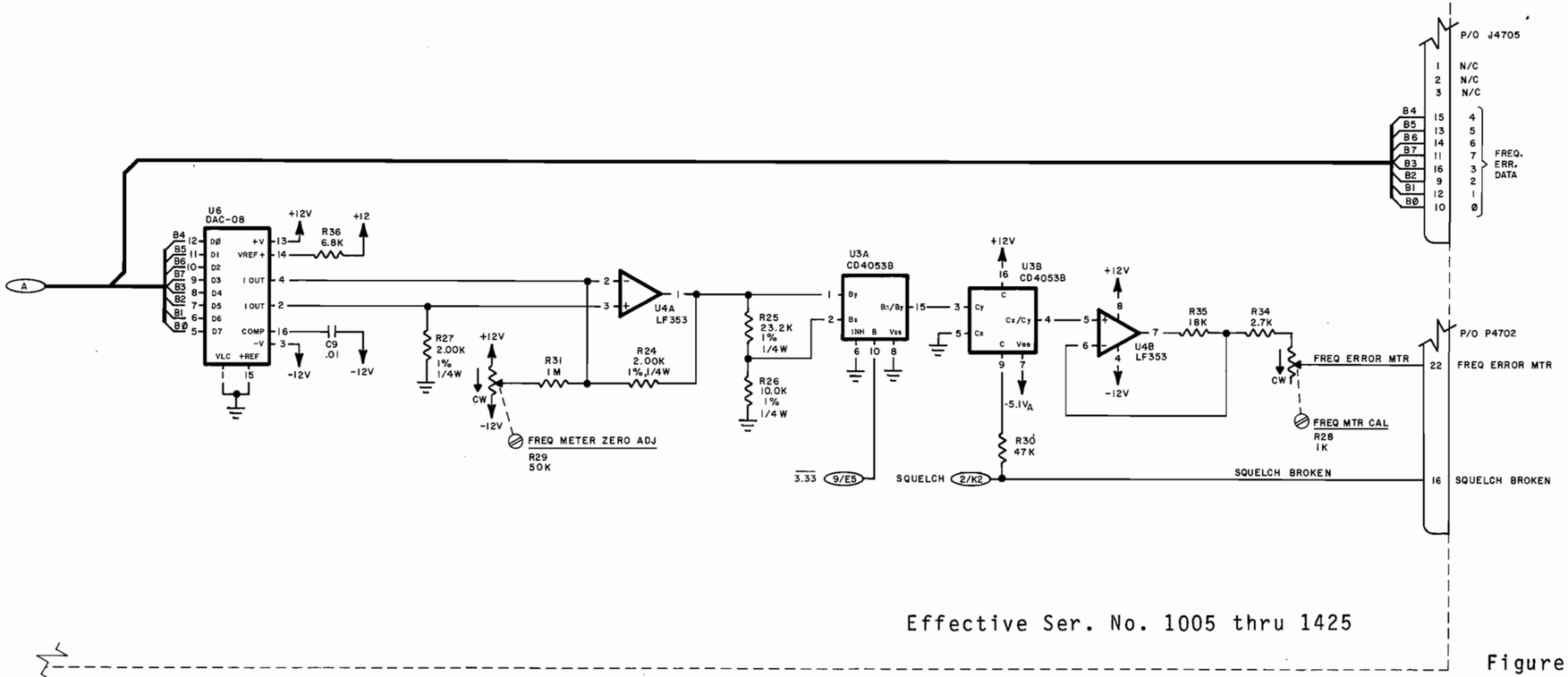
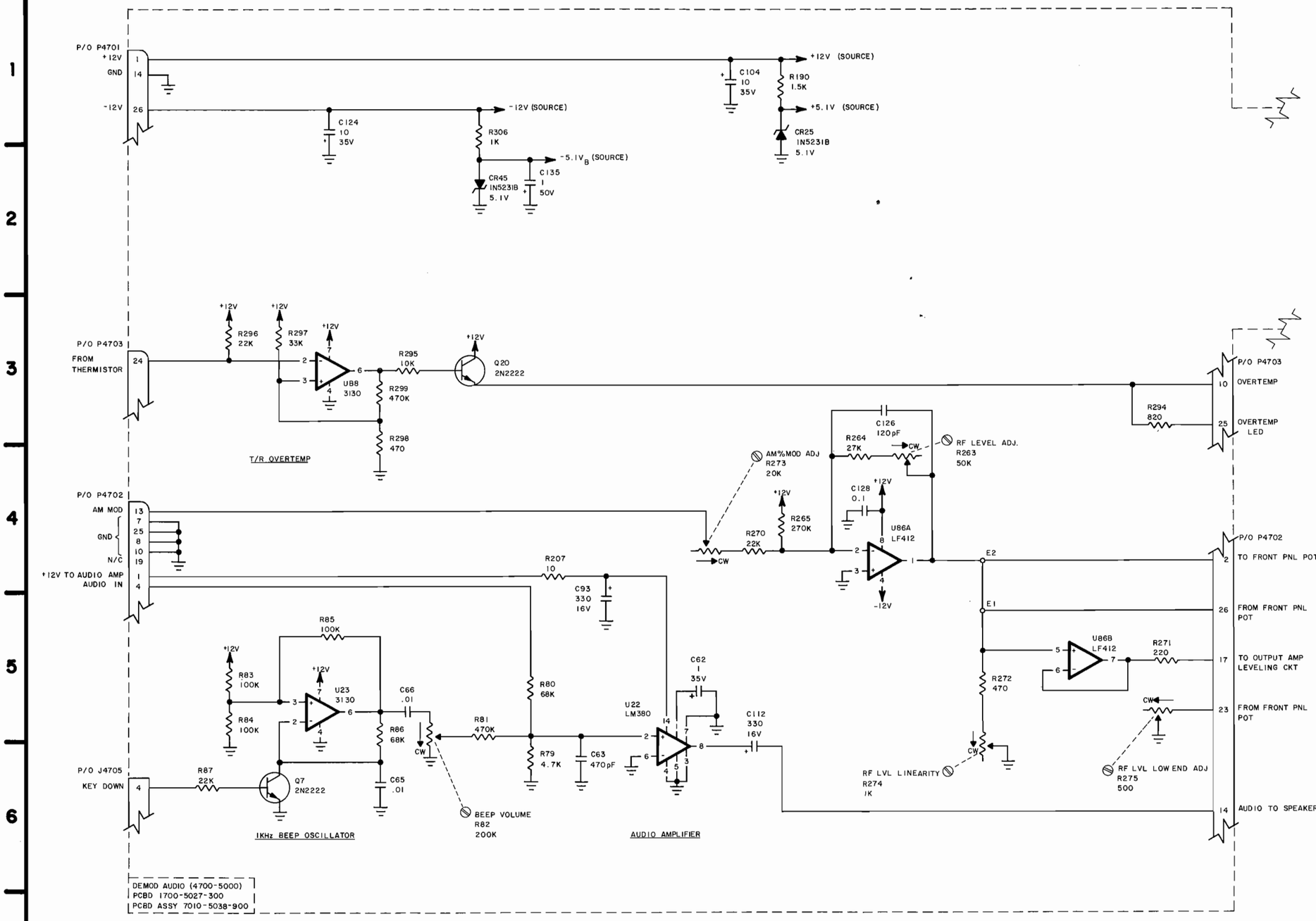


Figure 7-24 Demod Audio PC Board Schematic (Sheet 11 of 12)
0000-5014-700-A12



Effective Ser. No. 1005 thru 1425

Figure 7-24 Demod Audio PC Board Schematic (Sheet 12 of 12) 0000-5014-700-A12



STANDARDS:

(UNLESS OTHERWISE NOTED)

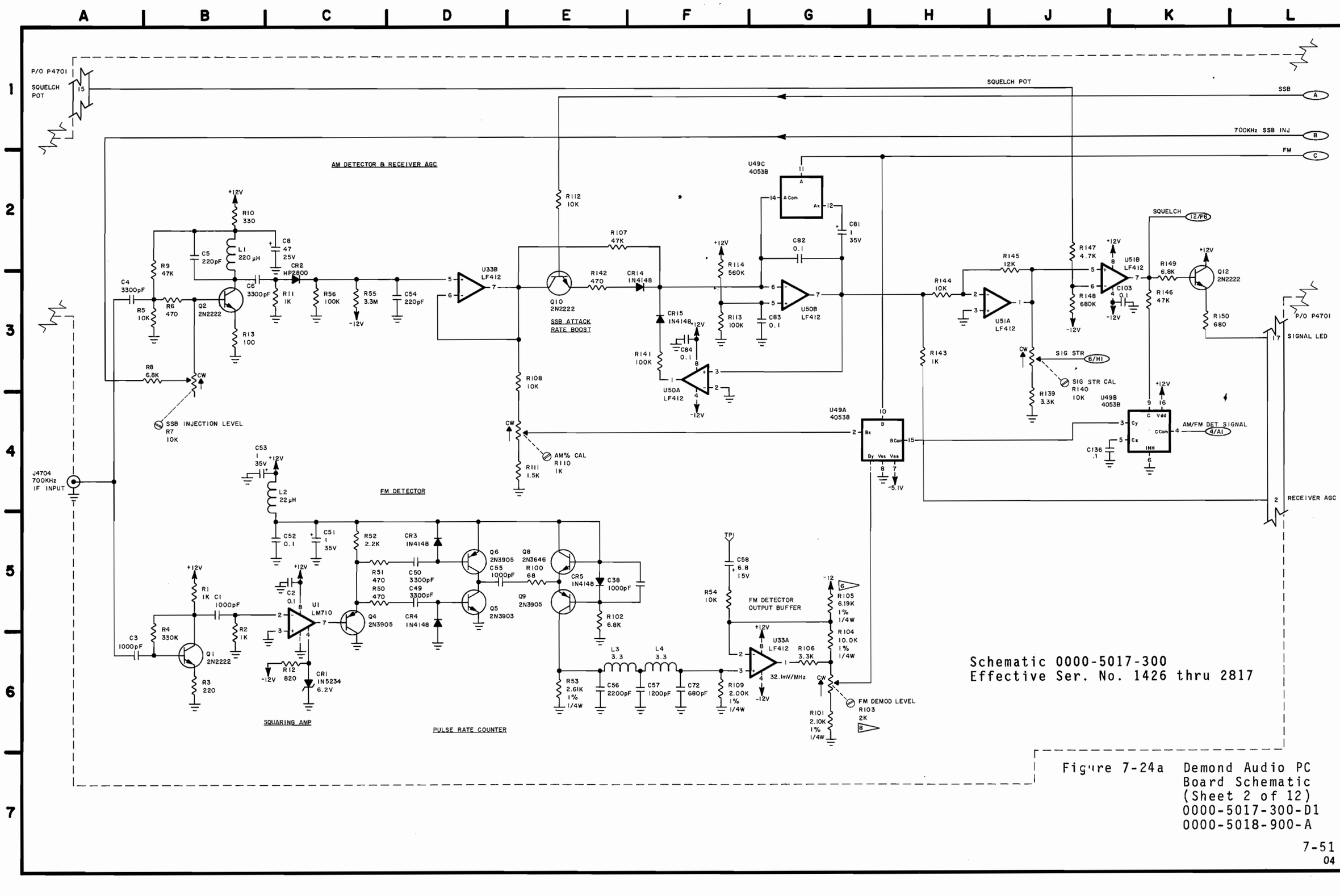
1. ALL REF NOS CARRY AN ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES 4700, 4800, 4900 AND 5000.
   A. PC BOARD ASSY 7010-5038-900; EFFECTIVE SER. NO. 2818 AND ON (4700, 4800, 4900, 5000; E.G., R1 IS R4701, R101 IS R4801, R201 IS R4901, R301 IS R50010.
   B. PC BOARD ASSY 7010-5037-300; EFFECTIVE SER. NO. 1426 THRU 2817, (4700, 4800, 4900, 5000; E.G., R1 IS R4701, R101 IS R4801, R201 IS R4901, R301 IS R5001).
2. ALL RESISTORS ARE 1/8 W, 5% TOLERANCE.
3. ALL RESISTANCE IS EXPRESSED IN OHMS.
4. ALL CAPACITANCE IS EXPRESSED IN MICROFARADS.
5. ALL INDUCTANCE IS EXPRESSED IN MICROHENRYS.

NOTES:

1. LAST REF NOS USED: J4706, C13, CR45, U91, E8, L7, Q24, R313, RN1, TP1, P4703.
2. REF NOS NOT USED: C10, C11, C14, c35, U12, R44, R250, J4701, J4702, J4703.
3. REF NOS NOT USED: U15B, U15D, U20B, U24B, U30C, U59B, U59C, U61B, U61C, U62B, U62C, U64B, U64C, U76B.
4. SCHEMATIC 0000-5017-300 (EFFECTIVE SER. NO. 1426 THRU 2817), R91 WAS 2.7K, R92 WAS 18K, R253 WAS 7.15K.
5. R25 IS 640 OHMS, 1/4W, 1% ON FM/AM-1500 MODELS EQUIPPED WITH MM-100E.
6. THRU SER. NO. 2165, R105 WAS 6.18K.
7. EFFECTIVE THRU SER. NO. 2225; R70, R71, R62, R63 WERE 10%, 1.8 W.
8. EFFECTIVE SER. NO. 1426 THRU 2748, R103 WAS 1K.

Schematic 0000-5017-300
Effective Ser. No. 1426 thru 2817

Figure 7-24a Demond Audio PC Board Schematic (Sheet 1 of 12)
0000-5017-300-D1
0000-5018-900-A



Schematic 0000-5017-300
Effective Ser. No. 1426 thru 2817

Figure 7-24a Demond Audio PC Board Schematic (Sheet 2 of 12) 0000-5017-300-D1 0000-5018-900-A

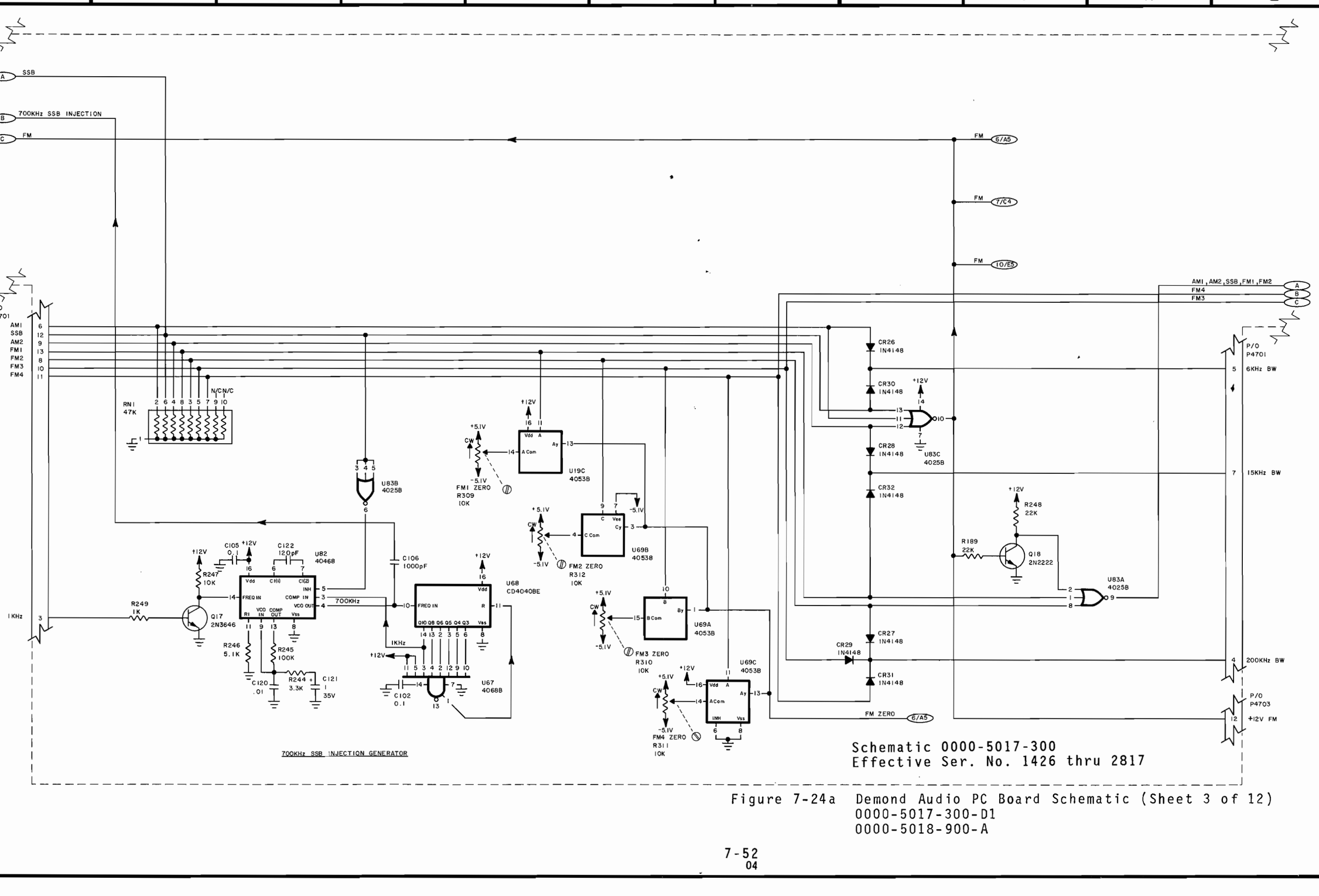
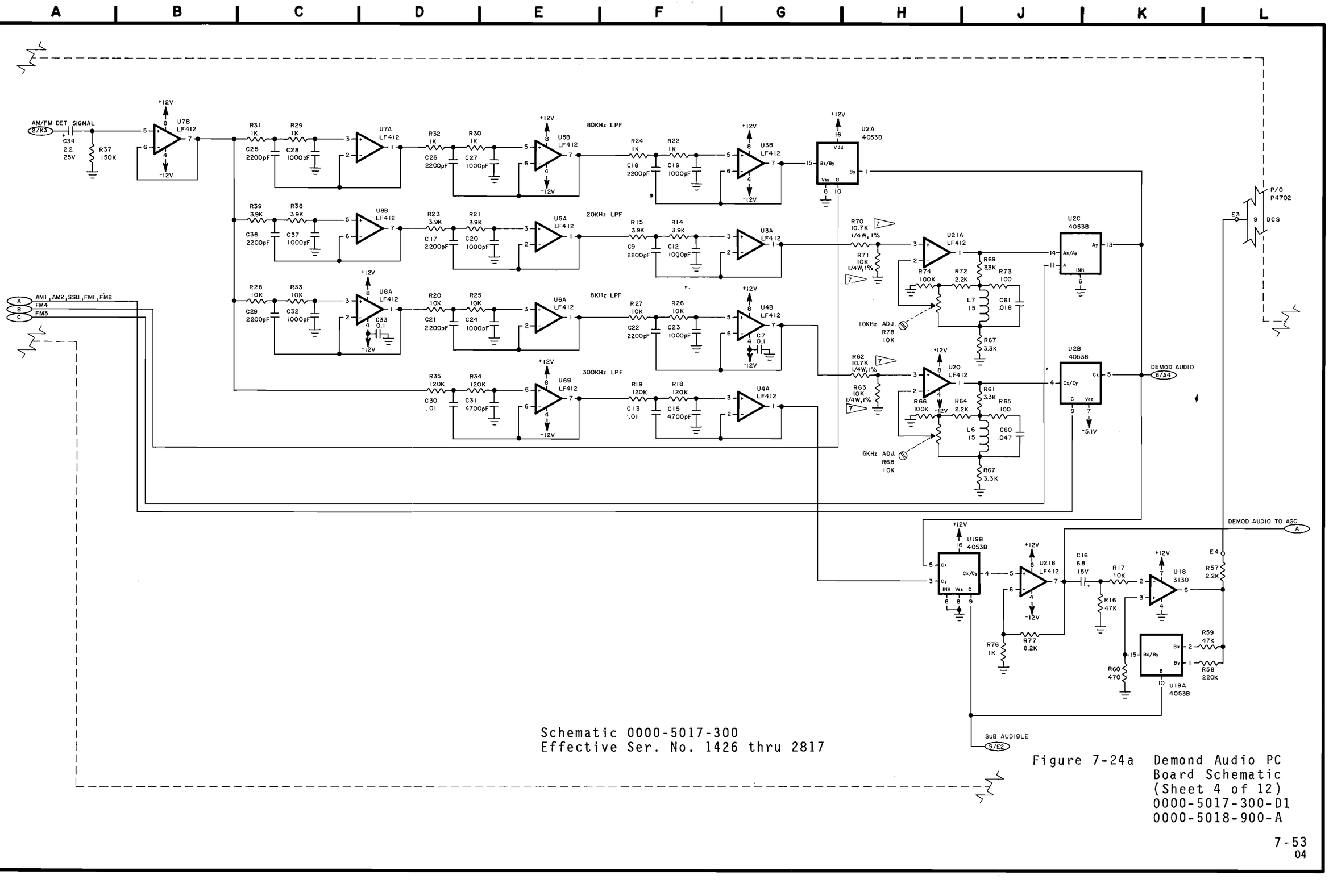
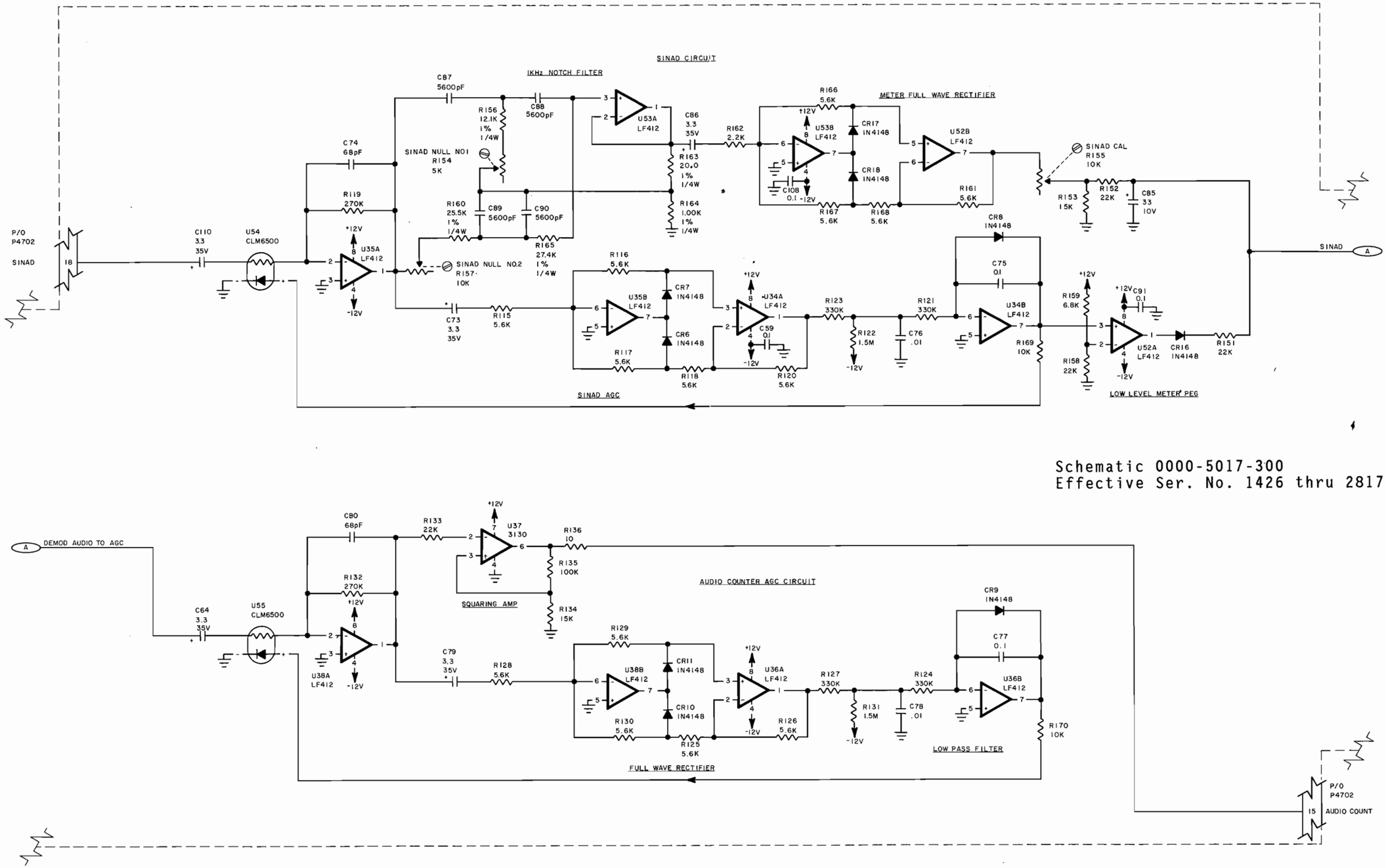


Figure 7-24a Demond Audio PC Board Schematic (Sheet 3 of 12)
0000-5017-300-D1
0000-5018-900-A



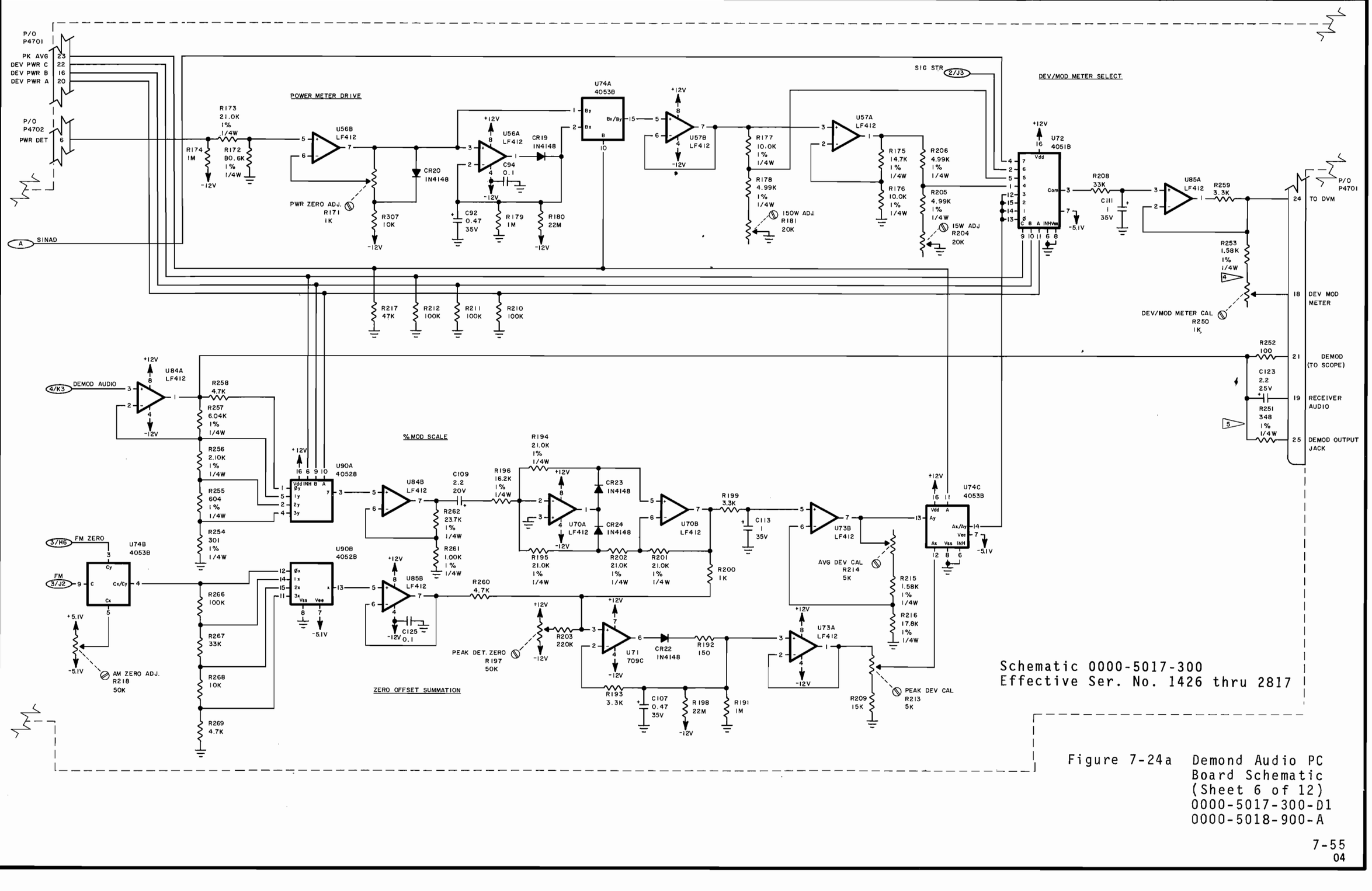
Schematic 0000-5017-300
Effective Ser. No. 1426 thru 2817

Figure 7-24a Demond Audio PC Board Schematic (Sheet 4 of 12)
0000-5017-300-D1
0000-5018-900-A



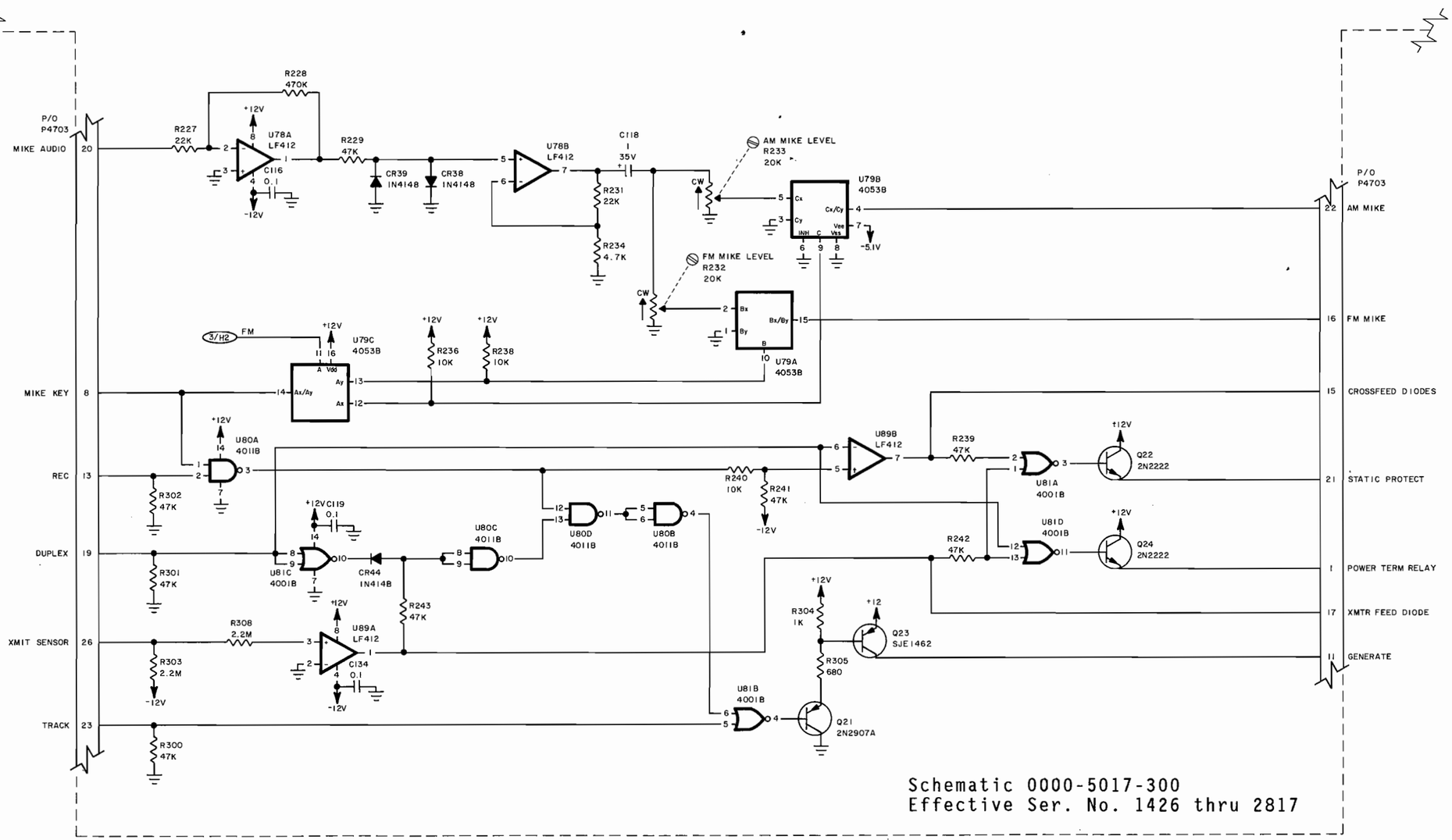
Schematic 0000-5017-300
Effective Ser. No. 1426 thru 2817

Figure 7-24a Demond Audio PC Board Schematic (Sheet 5 of 12)
0000-5017-300-D1
0000-5018-900-A



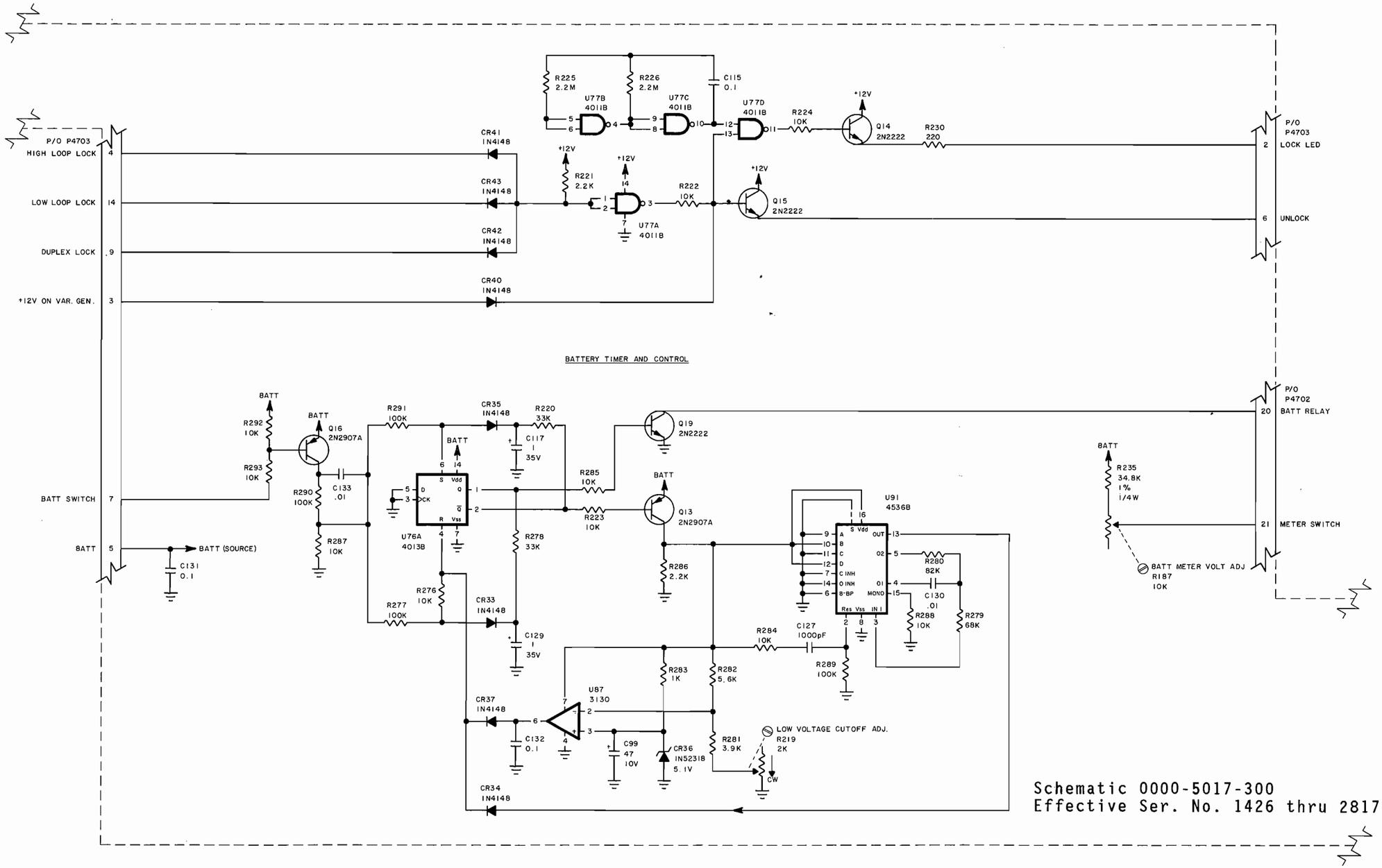
Schematic 0000-5017-300
Effective Ser. No. 1426 thru 2817

Figure 7-24a Demond Audio PC Board Schematic (Sheet 6 of 12) 0000-5017-300-D1 0000-5018-900-A



Schematic 0000-5017-300
Effective Ser. No. 1426 thru 2817

Figure 7-24a Demond Audio PC Board Schematic (Sheet 7 of 12)
0000-5017-300-D1
0000-5018-900-A

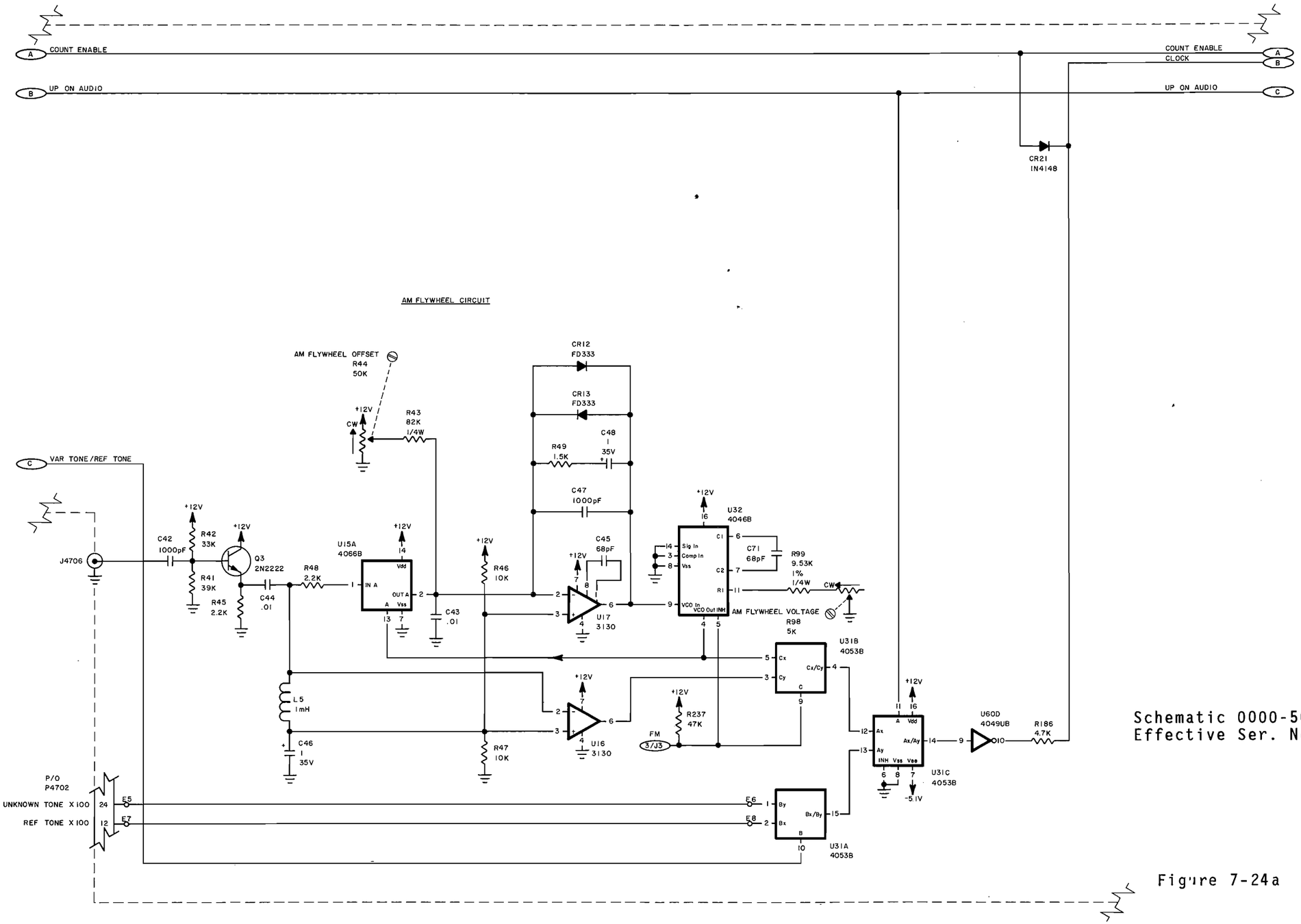


Schematic 0000-5017-300
Effective Ser. No. 1426 thru 2817

Figure 7-24a Demond Audio PC Board Schematic (Sheet 8 of 12) 0000-5017-300-D1 0000-5018-900-A

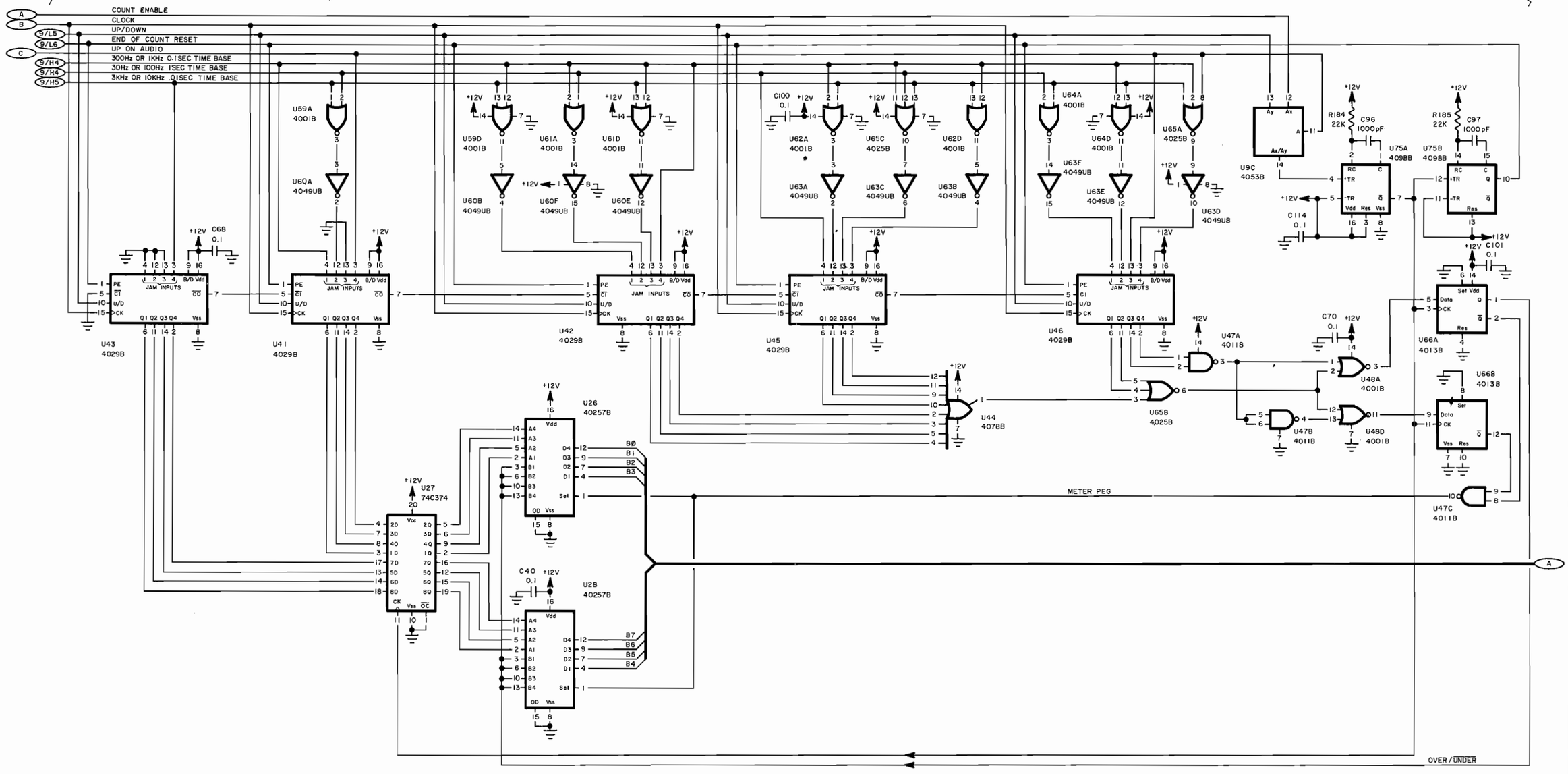
Schematic 0000-5017-300
Effective Ser. No. 1426 thru 2817

Figure 7-24a Demond Audio PC Board Schematic (Sheet 9 of 12)
0000-5017-300-D1
0000-5018-900-A



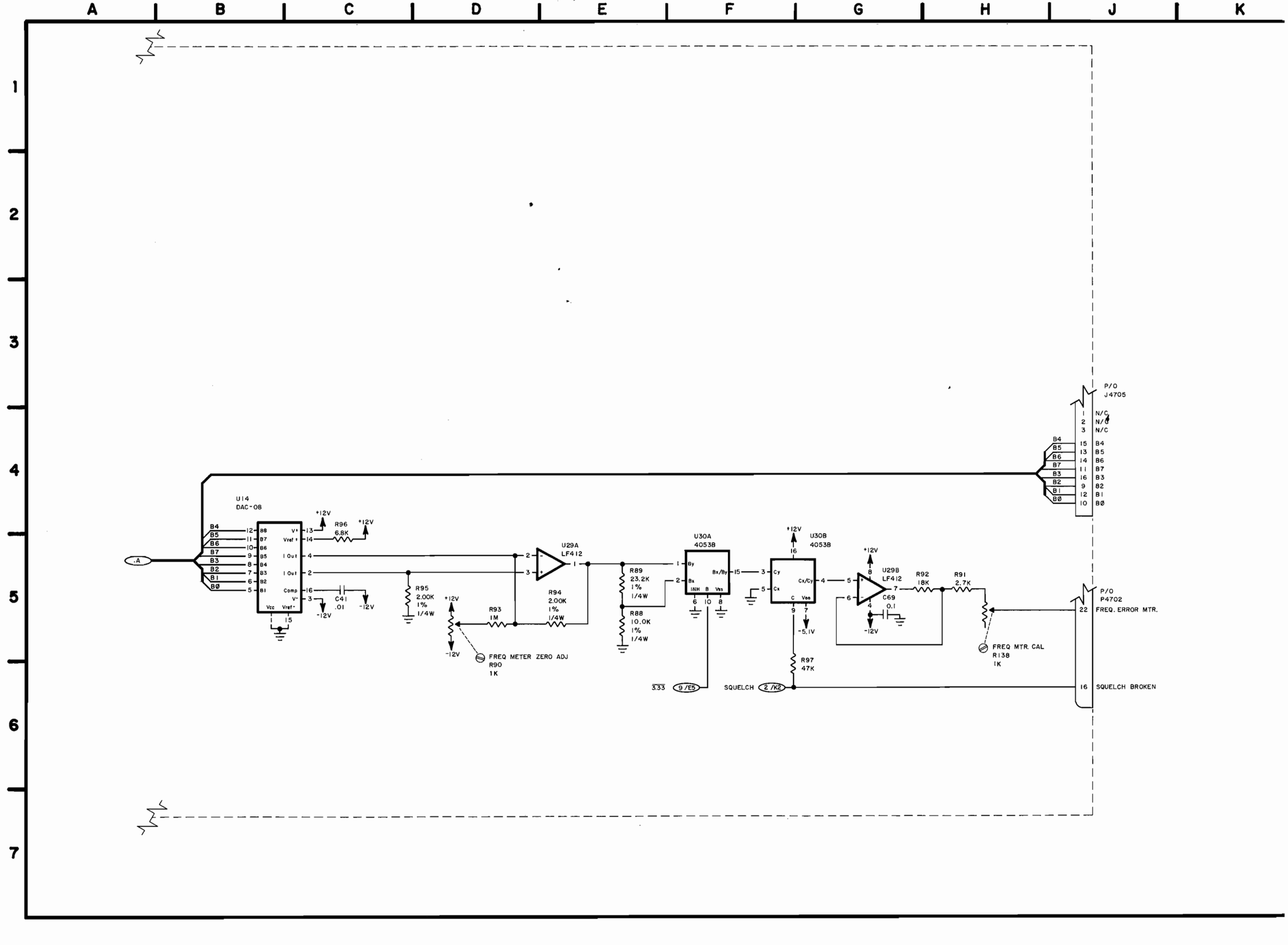
Schematic 0000-5017-300
Effective Ser. No. 1426 thru 2817

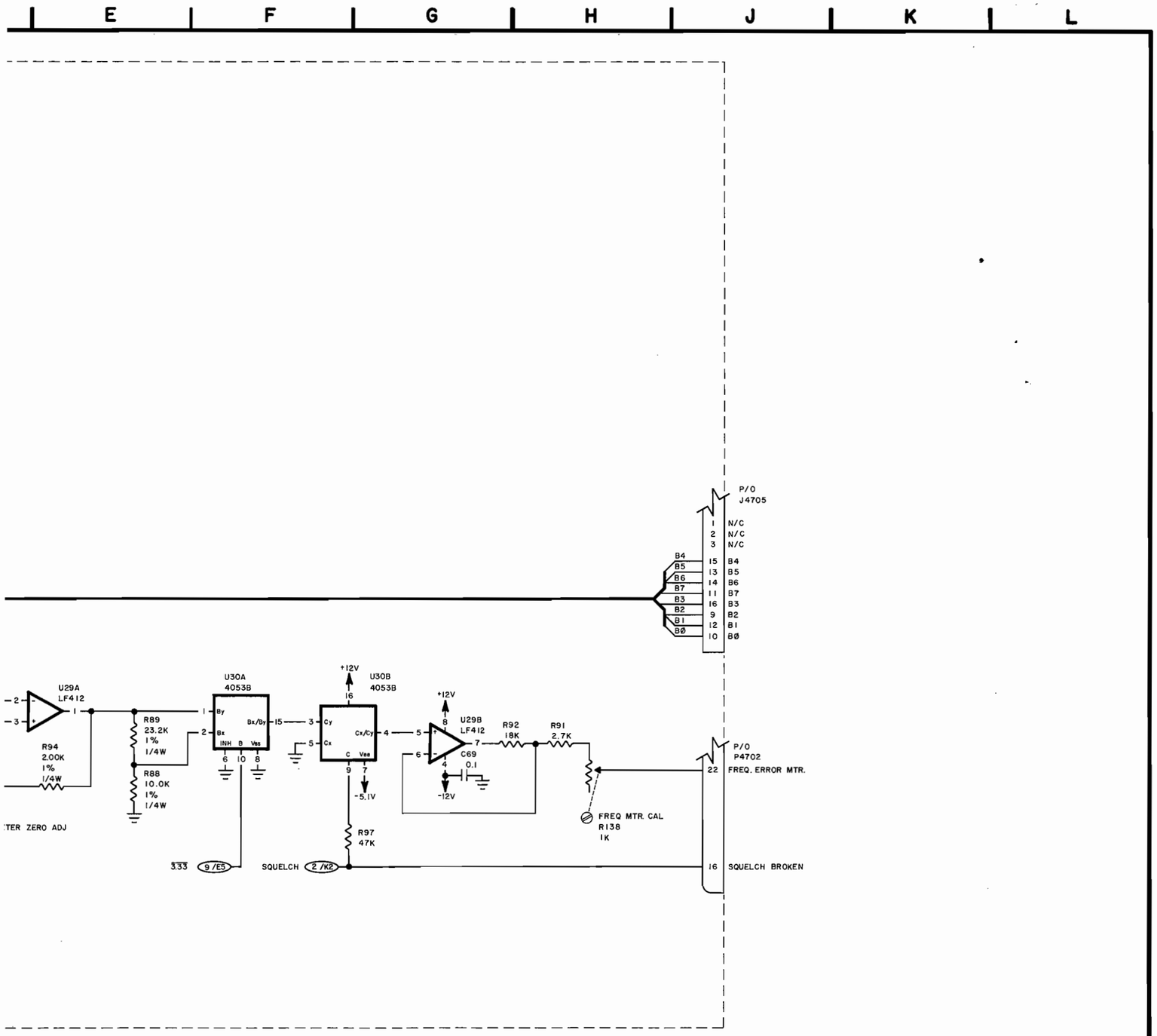
Figure 7-24a Demond Audio PC Board Schematic (Sheet 10 of 12) 0000-5017-300-D1 0000-5018-900-A



Schematic 0000-5017-300
Effective Ser. No. 1426 thru 2817

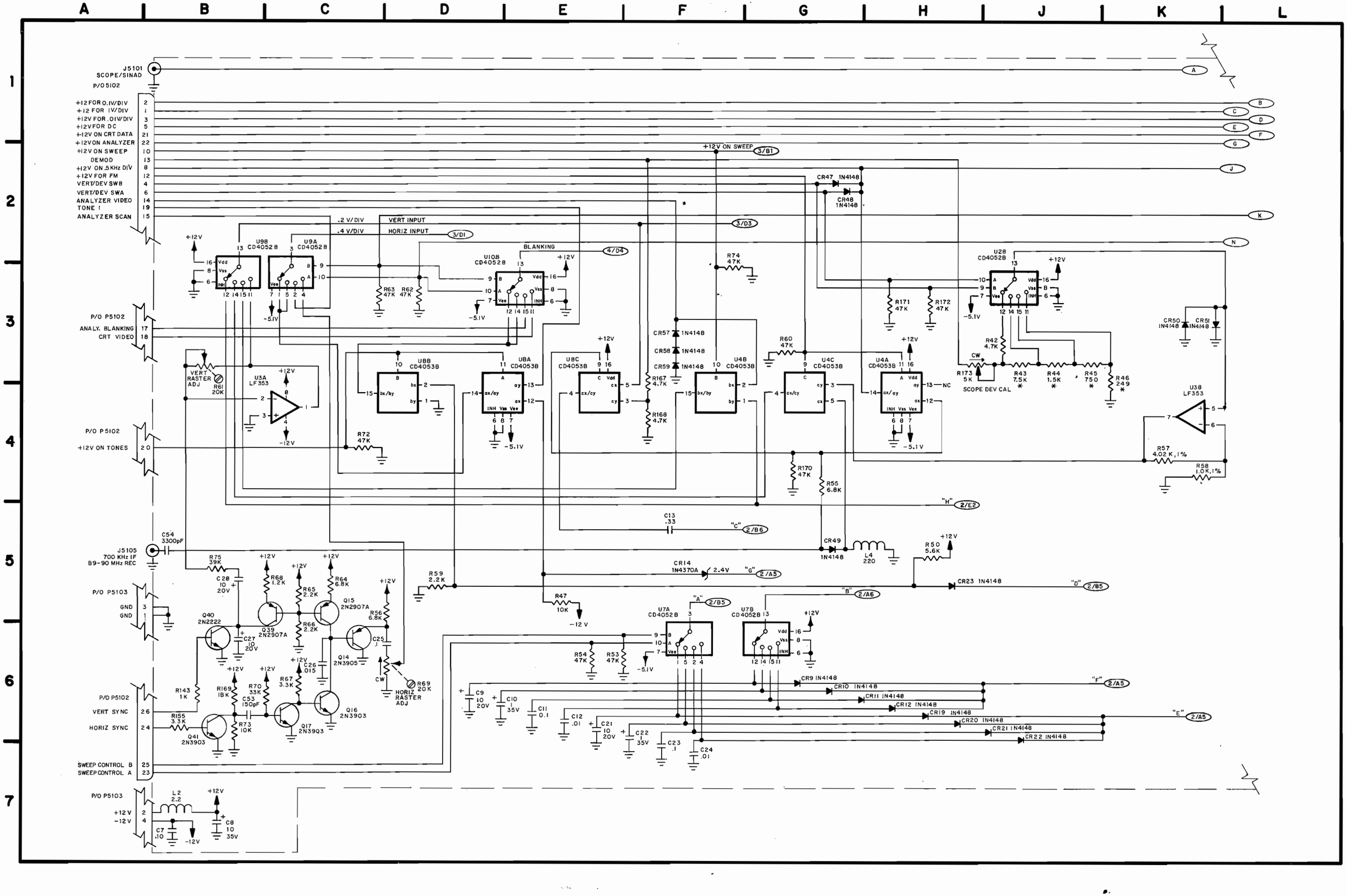
Figure 7-24a Demond Audio PC Board Schematic (Sheet 11 of 12)
0000-5017-300-D1
0000-5018-900-A

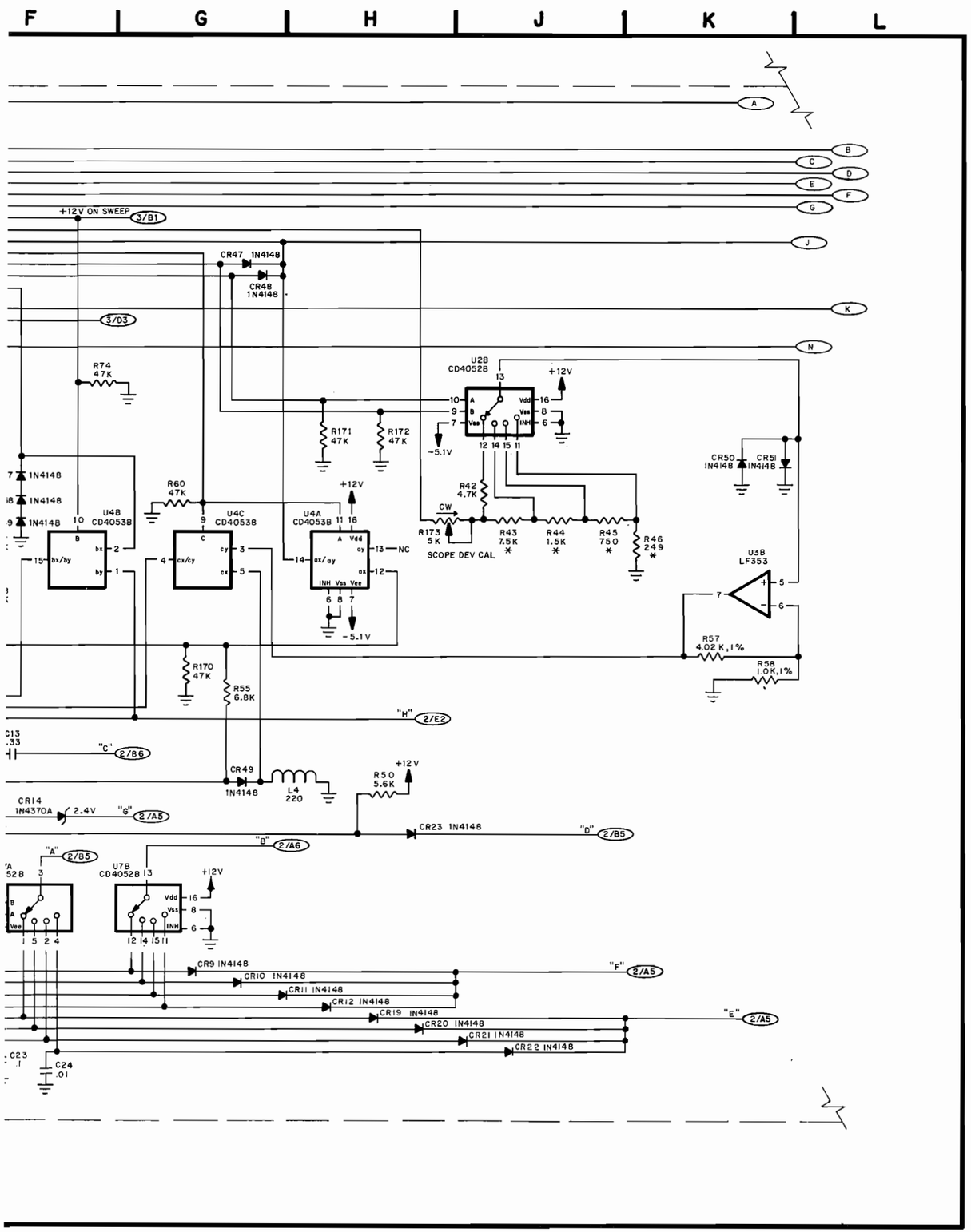

A
B
C
D
E
F
G
H
J
K
1
2
3
4
5
6
7
P/O
J4705
N/C
N/C
N/C
B4
B5
B6
B7
B3
B2
B1
B0
U14
DAC-08
+12V
R96
6.8K
C41
.01
-12V
R95
2.00K
1%
1/4W
R93
1M
FREQ METER ZERO ADJ
R90
1K
U29A
LF412
R94
2.00K
1%
1/4W
R89
23.2K
1%
1/4W
R88
10.0K
1%
1/4W
U30A
4053B
U30B
4053B
-5.1V
R97
47K
C69
0.1
U29B
LF412
R92
18K
R91
2.7K
FREQ MTR. CAL
R138
1K
P/O
P4702
22
FREQ. ERROR MTR.
16
SQUELCH BROKEN
SQUELCH
2 /K2
3.33
9 /E5



Schematic 0000-5017-300
Effective Ser. No. 1426 thru 2817

Figure 7-24a Demond Audio PC Board Schematic (Sheet 12 of 12) 0000-5017-300-D1 0000-5018-900-A


J5101 SCOPE/SINAD P/O P5102
+12 FOR 0.1V/DIV
+12 FOR 1V/DIV
+12V FOR .01V/DIV
+12V FOR DC
+12V ON CRT DATA
+12V ON ANALYZER
+12V ON SWEEP
DEMOD
+12V ON .5KHz DIV
+12V FOR FM
VERT/DEV SW B
VERT/DEV SW A
ANALYZER VIDEO
TONE !
ANALYZER SCAN
+12V ON SWEEP 3/B1
.2 V/DIV VERT INPUT
.4 V/DIV HORIZ INPUT 3/D1
BLANKING 4/D4
3/D3
CR47 1N4148
CR48 1N4148
U9B CD4052B
U9A CD4052B
U10B CD4052B
U28 CD4052B
R63 47K
R62 47K
R74 47K
R171 47K
R172 47K
P/O P5102
ANALY. BLANKING
CRT VIDEO
VERT RASTER ADJ R61 20K
U3A LF353
U8B CD4053B
U8A CD4053B
U8C CD4053B
U4B CD4053B
U4C CD4053B
U4A CD4053B
CR57 1N4148
CR58 1N4148
CR59 1N4148
R167 4.7K
R168 4.7K
R60 47K
R42 4.7K
R173 5K
SCOPE DEV CAL
R43 7.5K *
R44 1.5K *
R45 750 *
R46 249 *
CR50 IN4148
CR51 IN4148
U38 LF353
R57 4.02K,1%
R58 1.0K,1%
P/O P5102
+12V ON TONES
R72 47K
R170 47K
R55 6.8K
"H" 2/E2
C13 .33
"C" 2/B6
C54 3300pF
J5105 700 KHz IF B9-90 MHz REC
R75 39K
C28 10 20V
R68 1.2K
R65 2.2K
R64 6.8K
R66 2.2K
R56 6.8K
Q40 2N2222
Q39 2N2907A
Q15 2N2907A
Q14 2N3905
C27 10 20V
C25 .1
C26 .015
R69 20K HORIZ RASTER ADJ
P/O P5103
GND
GND
P/O P5102
VERT SYNC
HORIZ SYNC
R143 1K
R169 18K
R70 33K
R67 3.3K
C53 150pF
R155 3.3K
R73 10K
Q41 2N3903
Q17 2N3903
Q16 2N3903
SWEEP CONTROL B
SWEEP CONTROL A
P/O P5103
+12V
-12V
L2 2.2
C7 .10
C8 10 35V
CR49 1N4148
L4 220
R50 5.6K
CR14 1N4370A 2.4V
"G" 2/A5
R59 2.2K
R47 10K
-12 V
CR23 1N4148
"D" 2/B5
"B" 2/A6
"A" 2/B5
U7A CD4052B
U7B CD4052B
R54 47K
R53 47K
C9 10 20V
C10 1 35V
C11 0.1
C12 .01
C21 10 20V
C22 1 35V
C23 .1
C24 .01
CR9 IN4148
CR10 IN4148
CR11 IN4148
CR12 IN4148
CR19 IN4148
CR20 IN4148
CR21 IN4148
CR22 IN4148
"F" 2/A5
"E" 2/A5



STANDARDS:

(UNLESS OTHERWISE NOTED)

1. ALL REF NOS CARRY AN ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES:
   A. 0000-5015-100, COMPONENTS 01 THRU 99 (5100; E.G., R1 IS R5101).
   B. 0000-5015-100, COMPONENTS 100 THRU 199 (9500; E.G., R101 IS R9501).
   C. 0000-5-15-600, ALL COMPONENTS (9900; E.G., R1 IS R9901).

2. ALL RESISTORS ARE 1/4 W, 5% TOLERANCE.

3. ALL RESISTANCE IS EXPRESSED IN OHMS.

4. ALL CAPACITANCE IS EXPRESSED IN MICROFARADS.

5. ALL INDUCTANCE IS EXPRESSED IN MICROHENRYS.

NOTES:

1 THRU 3, NOT USED.

4. THRU SER. NO. 2001, HUMPER FROM E9 TO E10 NOT USED (E10 WENT ONLY TO TI-6, E9 WENT TO C74, C57, R142, R144, C133).

5. THRU SER. NO. 2102,CR4, CR5, CR6 WERE IN4148.

6. THRU SER. NO. 2089, R28 WAS 1K, R76 WAS 470 OHMS, R137 AND R138 WERE 820 OHMS, 1/2 W.

7. EFFECTIVE SER. NO. 2146 AND ON, USE C77 AND C78.

8. THRU SER. NO. 2099:
   E19 THRU E24 NOT USED (E23 AND E24 NOT SHOWN ON SCHEMATIC
   ISOLATED GROUNDS ON C60 AND C61 NOT USED
   E19 THRU E24
   T1-8, -9, AND -10 NOT CONNECTED
   TI-1 CONNECTS TO E21
   TI-3 CONNECTS TO E22
   THE FOLLOWING COMPONENTS NOT USED: C55, C59, CR45, Q31 THRU Q35, R129 THRU R136 AND R175.

   REFER TO CIRCUIT SCHEMATIC 0000-5018-600.

9. SER. NO. 2503 AND ON, ADD R179 AND CHANGE R97 FROM 301K TO 150K.

10. SER. NO. 2586 AND ON, ADD R180.

11. SER. NO. 2657 AND ON, DELETE C68, CHANGE R150 FROM 470 TO 1K.

12. SER. NO. 2768 AND ON, ADD C79 AND C80.

Figure 7-25 Oscilloscope Control and Deflection PC Board Schematic (Sheet 1 of 4) 0000-5015-100-G1

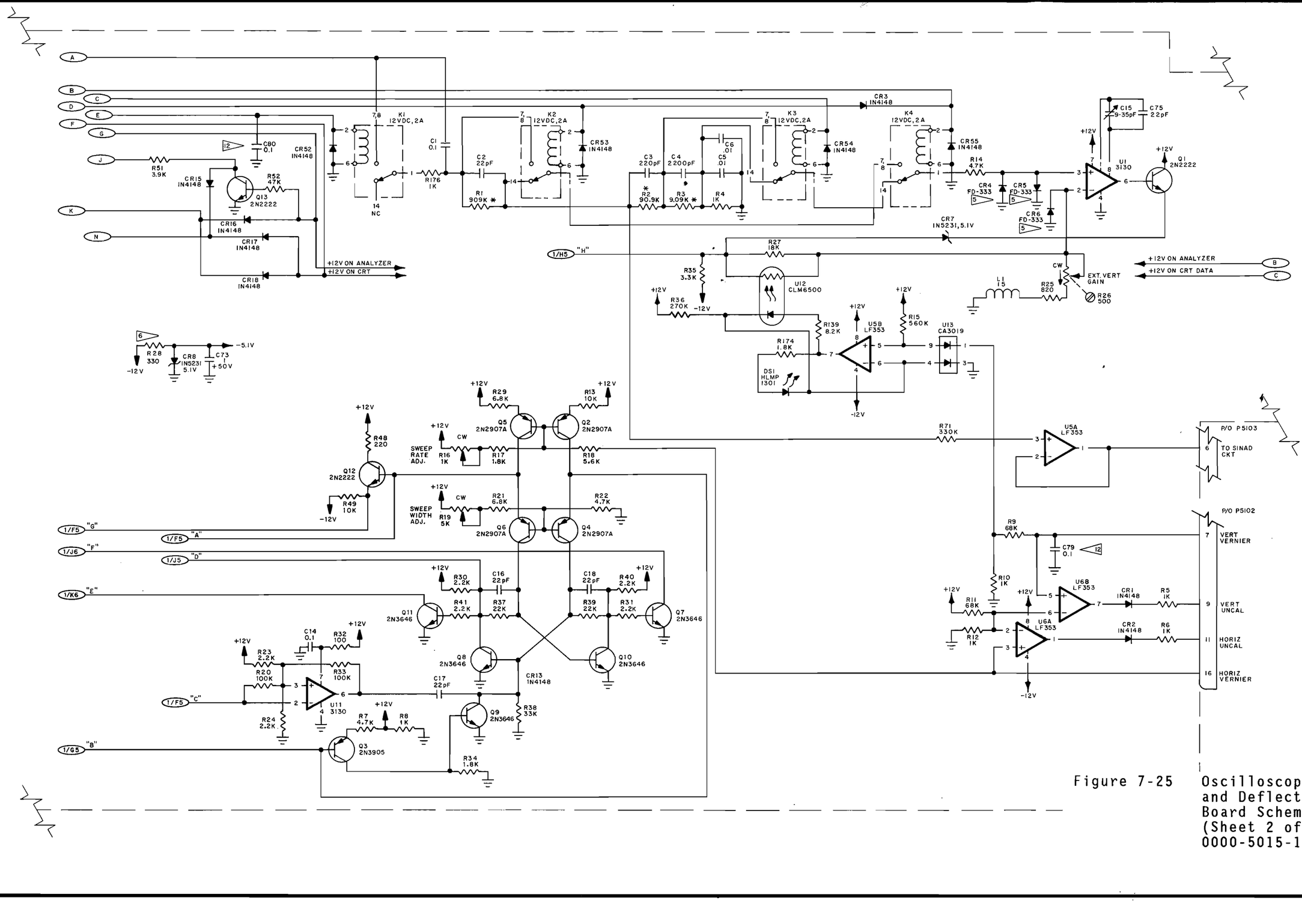


Figure 7-25 Oscilloscope Control and Deflection PC Board Schematic (Sheet 2 of 4) 0000-5015-100-G1

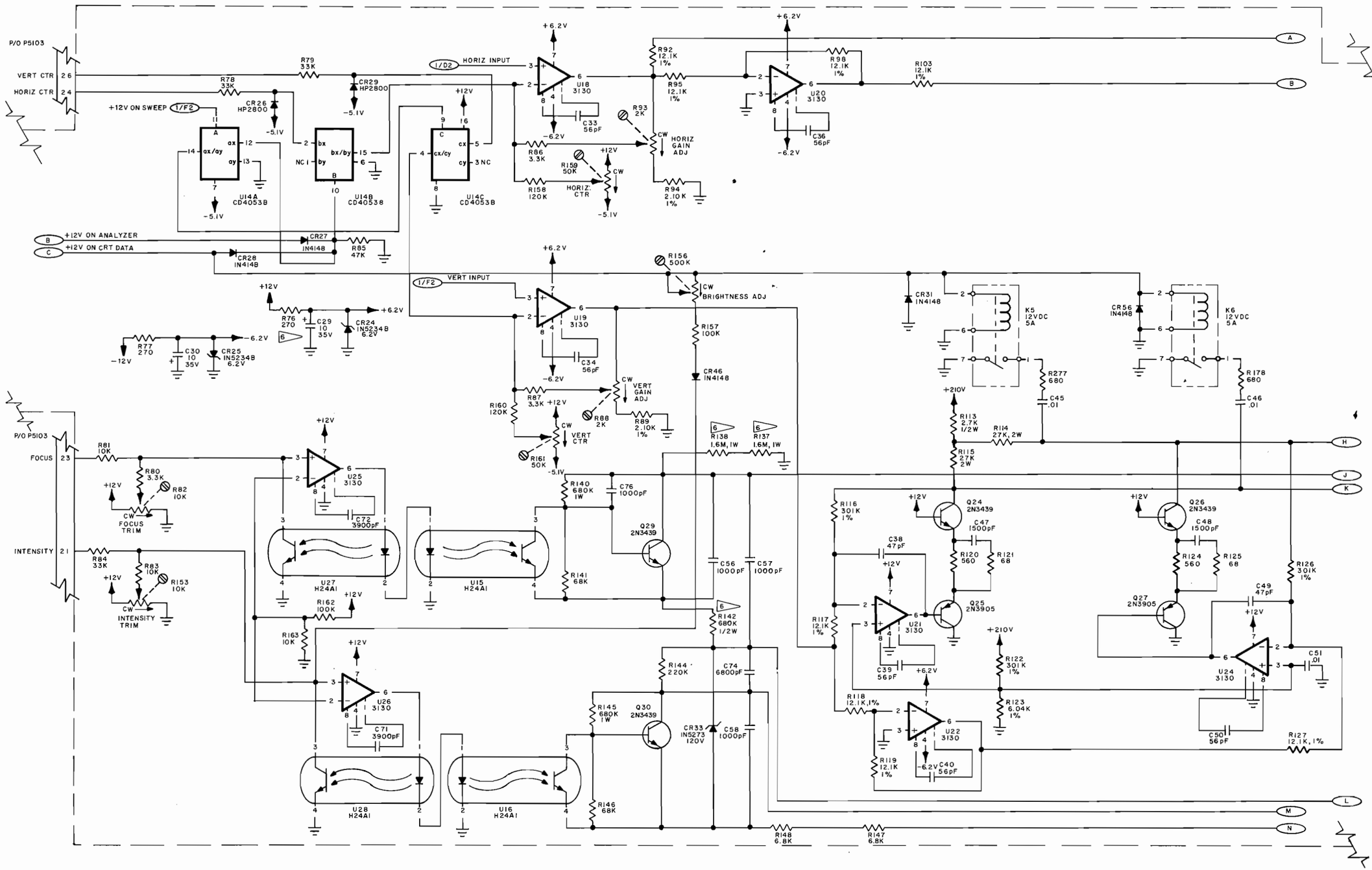
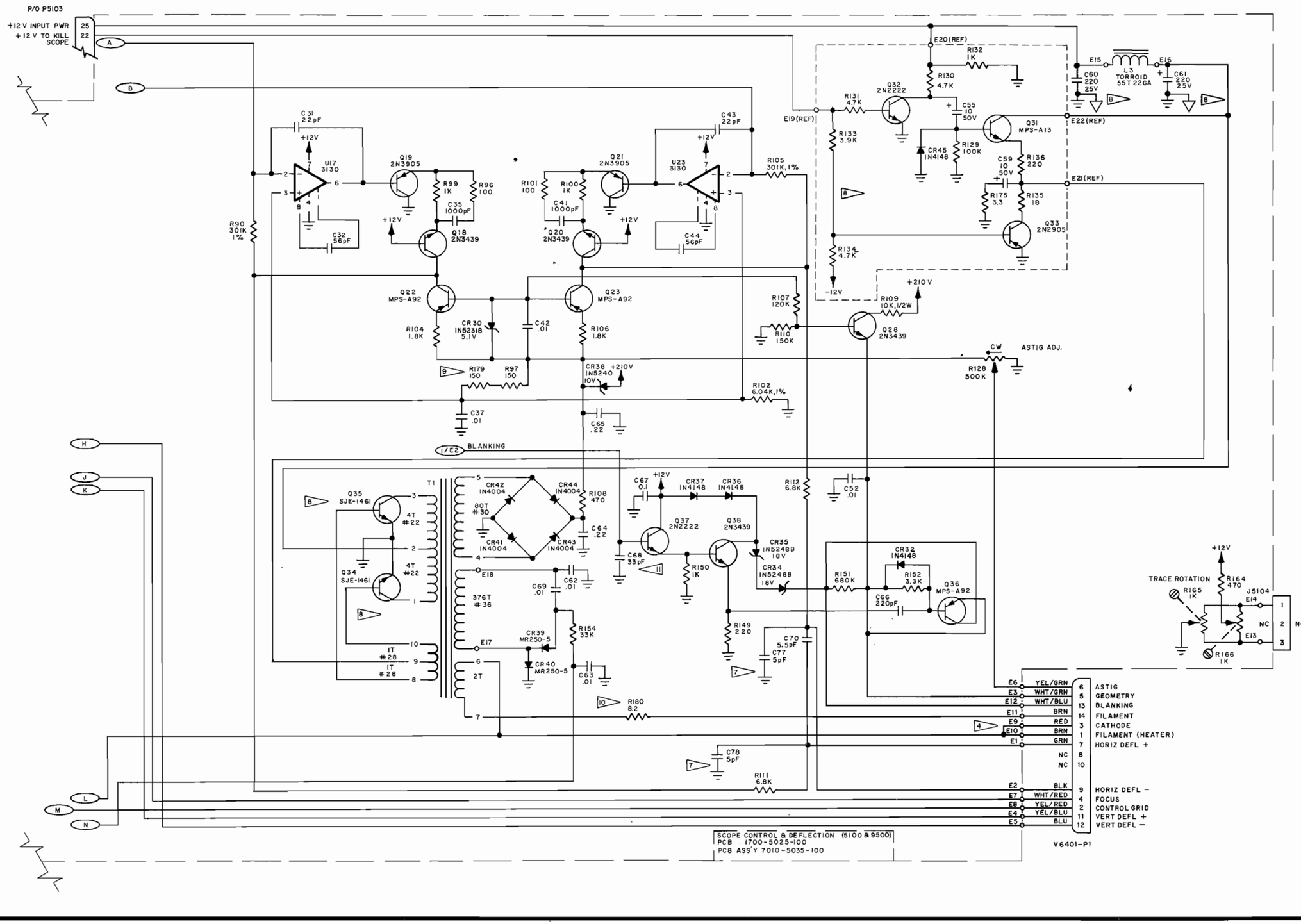
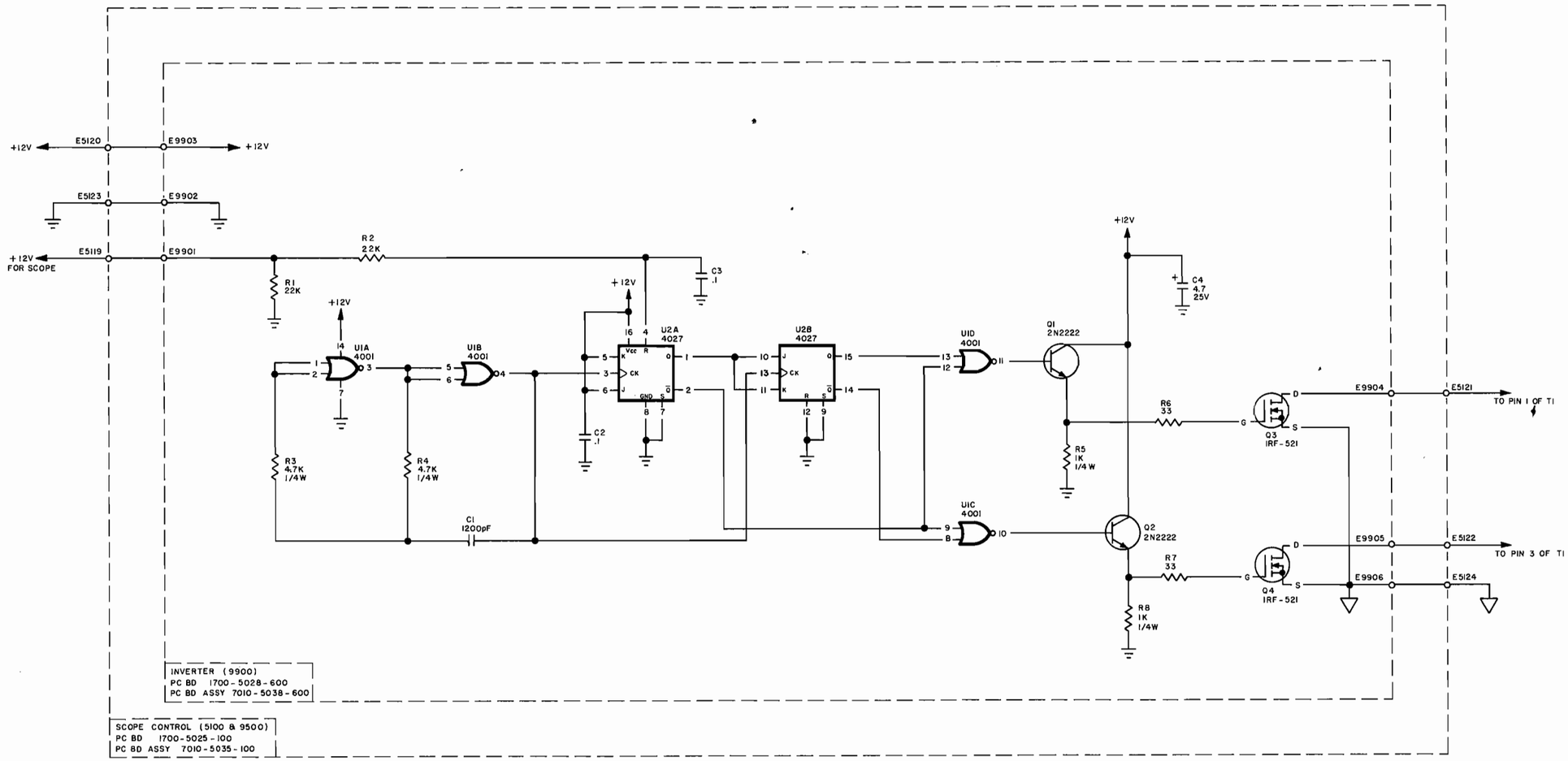


Figure 7-25 Oscilloscope Control and Deflection PC Board Schematic (Sheet 3 of 4) 0000-5015-100-G1

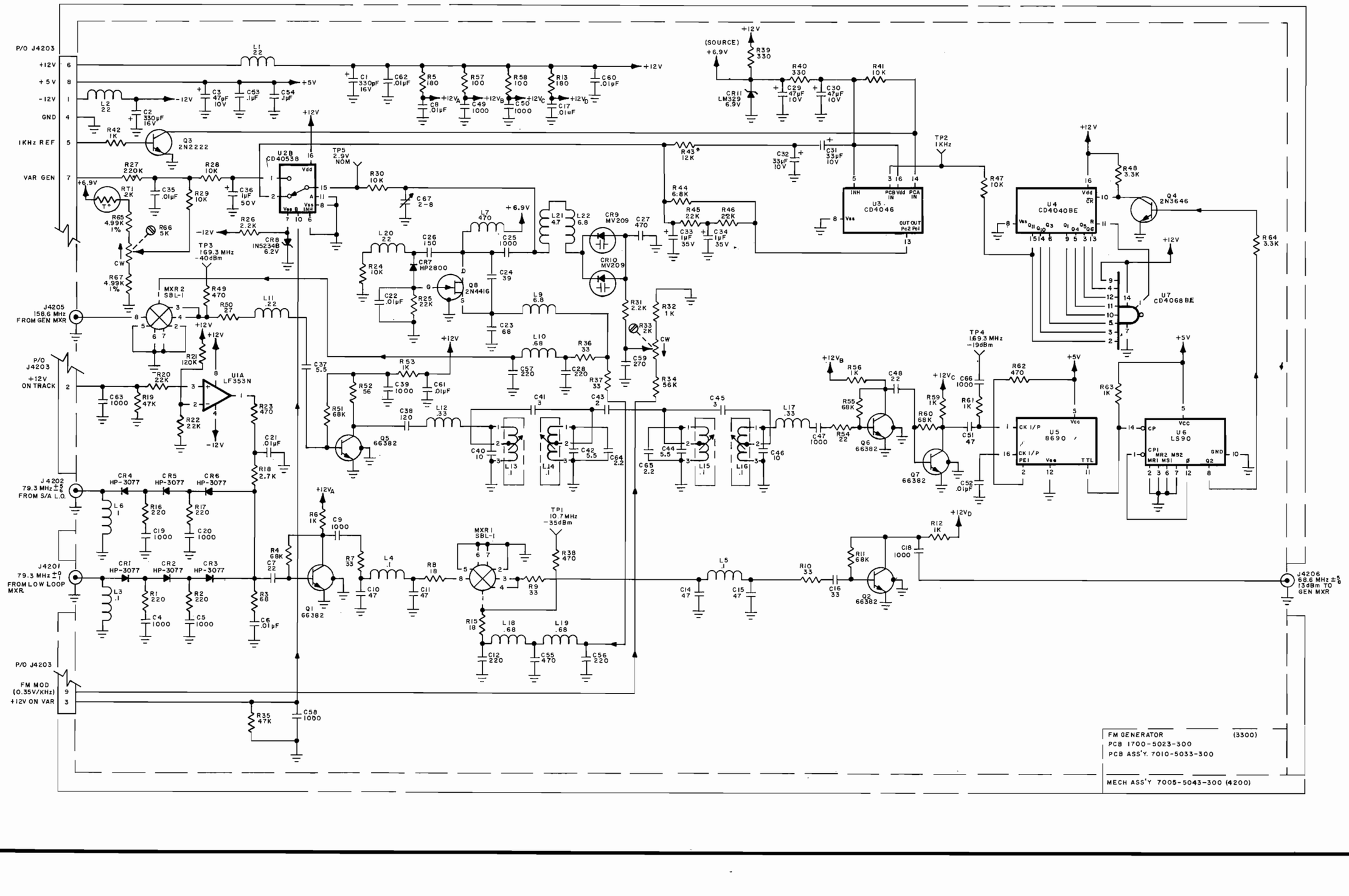

P/O P5103
+12 V INPUT PWR 25
+12 V TO KILL SCOPE 22
A
B
C31 22pF
+12V
U17 3130
Q19 2N3905
R99 1K
R96 100
C35 1000pF
C32 56pF
R90 301K 1%
Q18 2N3439
Q22 MPS-A92
R104 1.8K
CR30 IN52318 5.1V
C42 .01
Q23 MPS-A92
R106 1.8K
R101 100
R100 1K
C41 1000pF
Q21 2N3905
Q20 2N3439
U23 3130
C43 22pF
C44 56pF
R105 301K,1%
R107 120K
R110 150K
Q28 2N3439
+210V
R109 10K,1/2W
E19(REF)
E20(REF)
R132 1K
R130 4.7K
R131 4.7K
Q32 2N2222
C55 10 50V
Q31 MPS-A13
R133 3.9K
CR45 IN4148
R129 100K
C59 10 50V
R136 220
R175 3.3
R135 18
Q33 2N2905
R134 4.7K
-12V
E22(REF)
E21(REF)
E15
L3 TORROID 55T 22GA
E16
C60 220 25V
C61 220 25V
CW
ASTIG ADJ.
R128 500K
R179 150
R97 150
CR38 IN5240 10V
R102 6.04K,1%
C37 .01
C65 .22
H
J
K
L
M
N
1/E2
BLANKING
T1
Q35 SJE-146I
Q34 SJE-146I
4T #22
4T #22
80T #30
376T #36
IT #28
IT #28
2T
CR42 IN4004
CR44 IN4004
CR41 IN4004
CR43 IN4004
R108 470
C64 .22
E18
E17
C69 .01
C62 .01
CR39 MR250-5
CR40 MR250-5
R154 33K
C63 .01
R180 8.2
C67 0.1
+12V
CR37 IN4148
CR36 IN4148
Q37 2N2222
Q38 2N3439
C68 33pF
R150 1K
CR35 IN5248B 18V
CR34 IN5248B 18V
R112 6.8K
C52 .01
R151 680K
CR32 IN4148
R152 3.3K
Q36 MPS-A92
C66 220pF
R149 220
C70 5.5pF
C77 5pF
C78 5pF
R111 6.8K
R164 470
TRACE ROTATION
R165 1K
R166 1K
J5104
E14
E13
NC
NC
E6 YEL/GRN 6 ASTIG
E3 WHT/GRN 5 GEOMETRY
E12 WHT/BLU 13 BLANKING
E11 BRN 14 FILAMENT
E9 RED 3 CATHODE
E10 BRN 1 FILAMENT (HEATER)
E1 GRN 7 HORIZ DEFL +
NC 8
NC 10
E2 BLK 9 HORIZ DEFL –
E7 WHT/RED 4 FOCUS
E8 YEL/RED 2 CONTROL GRID
E4 YEL/BLU 11 VERT DEFL +
E5 BLU 12 VERT DEFL –
V6401-P1
SCOPE CONTROL & DEFLECTION (5100 & 9500)
PCB 1700-5025-100
PCB ASS'Y 7010-5035-100

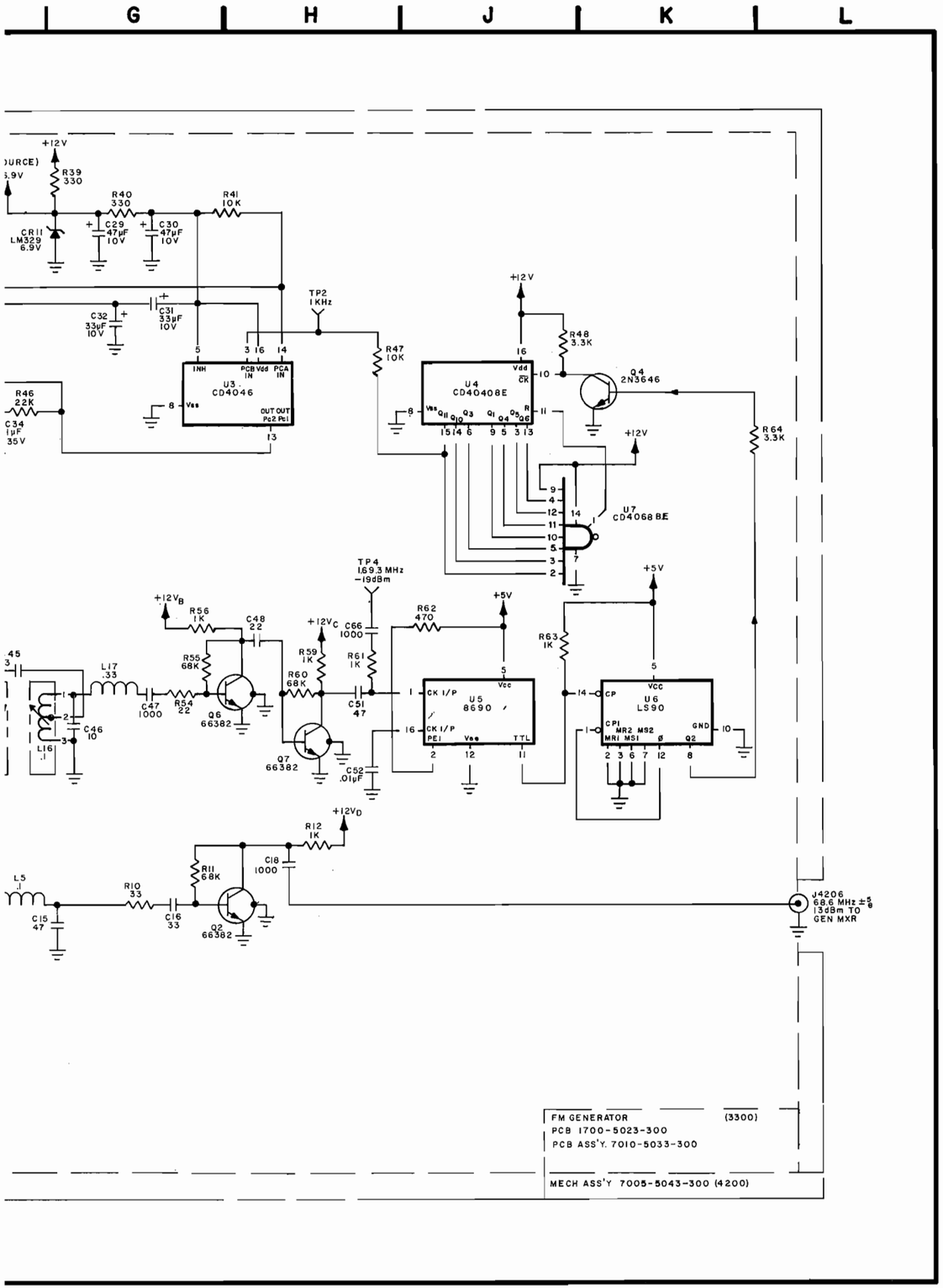


INVERTER SCHEMATIC
0000-5018-600 REV B
SER. NO. 2100 AND ON

DETAIL **A**

Figure 7-25 Oscilloscope Control and Deflection PC Board Schematic (Sheet 4 of 4) 0000-5015-100-G1


P/O J4203
+12V 6
+5V 8
-12V 1
GND 4
1KHz REF 5
VAR GEN 7
L1 22
L2 22
C1 330pF 16V
C2 330µF 16V
C3 47µF 10V
C53 .1µF
C54 .1µF
C62 .01µF
C60 .01pF
R5 180
R57 100
R58 100
R13 180
C8 .01µF
C49 1000
C50 1000
C17 .01uF
+12V
+5V
-12V
+12V_A
+12V_B
+12V_C
+12V_D
(SOURCE) +6.9V
R39 330
CR11 LM329 6.9V
R40 330
C29 47µF 10V
C30 47µF 10V
R41 10K
R42 1K
Q3 2N2222
U2B CD40538
TP5 2.9V NOM
R30 10K
C67 2-8
R43 12K
C32 33µF 10V
C31 33µF 10V
TP2 1KHz
R27 220K
R28 10K
C36 1µF 50V
C35 .01µF
R29 10K
RT1 2K
R65 4.99K 1%
R66 5K
R67 4.99K 1%
CW
R26 2.2K
CR8 IN5234B 6.2V
TP3 169.3 MHz -40dBm
R44 6.8K
R45 22K
R46 22K
C33 1µF 35V
C34 1µF 35V
U3 CD4046
R47 10K
U4 CD4040BE
R48 3.3K
Q4 2N3646
R64 3.3K
L7 470
L20 2.2
C26 150
C25 1000
L21 4.7
L22 6.8
CR9 MV209
CR10 MV209
C27 470
R24 10K
CR7 HP2800
C22 .01µF
R25 22K
Q8 2N4416
C24 39
L9 6.8
C23 68
R31 2.2K
R32 1K
R33 2K
C59 270
R34 56K
U7 CD4068BE
J4205 158.6 MHz FROM GEN MXR
MXR2 SBL-1
R49 470
R50 27
L11 .22
R21 120K
R20 22K
R19 47K
R22 22K
R23 470
C21 .01µF
R18 2.7K
P/O J4203 +12V ON TRACK
C63 1000
UIA LF353N
C37 5.5
R53 1K
C39 1000
C61 .01µF
R52 56
R51 68K
C38 120
L12 .33
L10 .68
R36 33
C57 220
C28 220
R37 33
C41 3
C43 2
C45 3
C40 10
C42 5.5
C64 2.2
C44 5.5
C65 2.2
C46 10
L13 .1
L14 .1
L15 .1
L16 .1
L17 .33
C47 1000
R54 22
Q5 66382
Q6 66382
Q7 66382
TP4 169.3 MHz -19dBm
R56 1K
C48 22
R55 68K
R59 1K
R60 68K
C66 1000
R61 1K
C51 47
C52 .01µF
R62 470
R63 1K
U5 8690
U6 LS90
J4202 79.3 MHz +0 -1 FROM S/A L.O.
CR4 HP-3077
CR5 HP-3077
CR6 HP-3077
L6 1
R16 220
R17 220
C19 1000
C20 1000
J4201 79.3 MHz +0 -1 FROM LOW LOOP MXR
CR1 HP-3077
CR2 HP-3077
CR3 HP-3077
L3 .1
R1 220
R2 220
C4 1000
C5 1000
R3 68
C6 .01µF
R4 68K
C7 22
Q1 66382
R6 1K
C9 1000
R7 33
L4 .1
C10 47
R8 18
C11 47
MXR1 SBL-1
TP1 10.7MHz -35dBm
R38 470
R9 33
R15 18
L18 .68
L19 .68
C12 220
C55 470
C56 220
L5 .1
C14 47
C15 47
R10 33
C16 33
R11 68K
Q2 66382
R12 1K
C18 1000
J4206 68.6 MHz ±5 13.8Bm TO GEN MXR
P/O J4203
FM MOD (0.35V/KHz) 9
+12V ON VAR 3
R35 47K
C58 1000
FM GENERATOR (3300)
PCB 1700-5023-300
PCB ASS'Y. 7010-5033-300
MECH ASS'Y 7005-5043-300 (4200)



STANDARDS:
(UNLESS OTHERWISE NOTED)

1. ALL REF NOS CARRY AN ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES: 3300 & 4200 (E.G., R1 IS R3301, ETC.).

   A. MECH ASSY 7005-5043-300 (4200)
   B. PCB ASSY 7010-5033-300 (3300)

2. ALL RESISTORS ARE 1/4 W, ±5% TOLERANCE.

3. ALL RESISTANCE IS EXPRESSED IN OHMS.

4. ALL CAPACITANCE IS EXPRESSED IN PICO-FARADS.

5. ALL INDUCTANCE IS EXPRESSED IN MICRO-HENRYS.

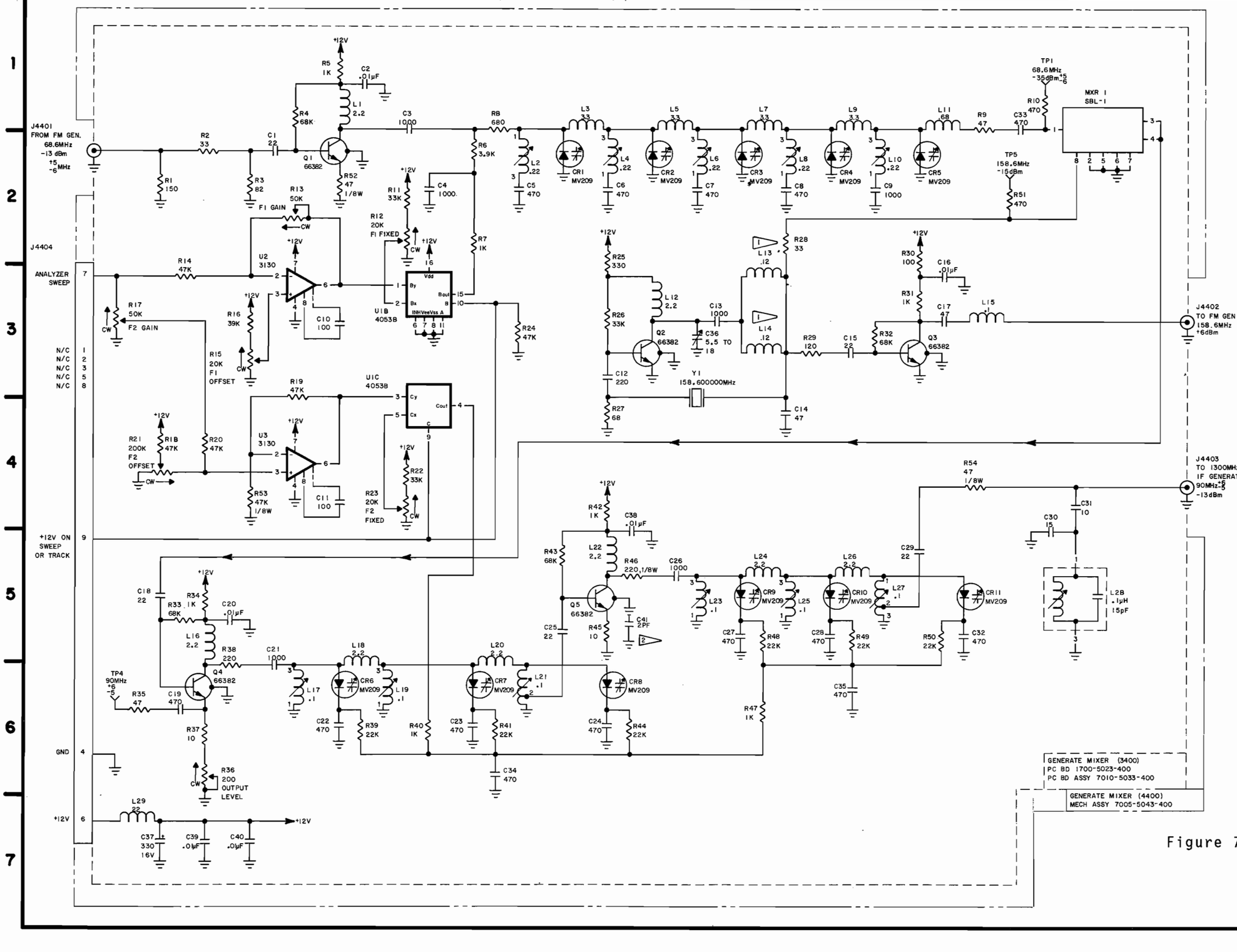
NOTES:

1. LAST REF NOS USED:
   R67, Q8, C67, MXR2, U7, TP5, J420, L22, CR11, RT1.

2. REF NOS NOT USED:
   J4204, R14, L8, C13.

3. IC FUNCTIONS NOT USED:
   U1B, U2A, U2C.

Figure 7-26 FM Generator Module Schematic 0000-5013-300-D6



STANDARDS:

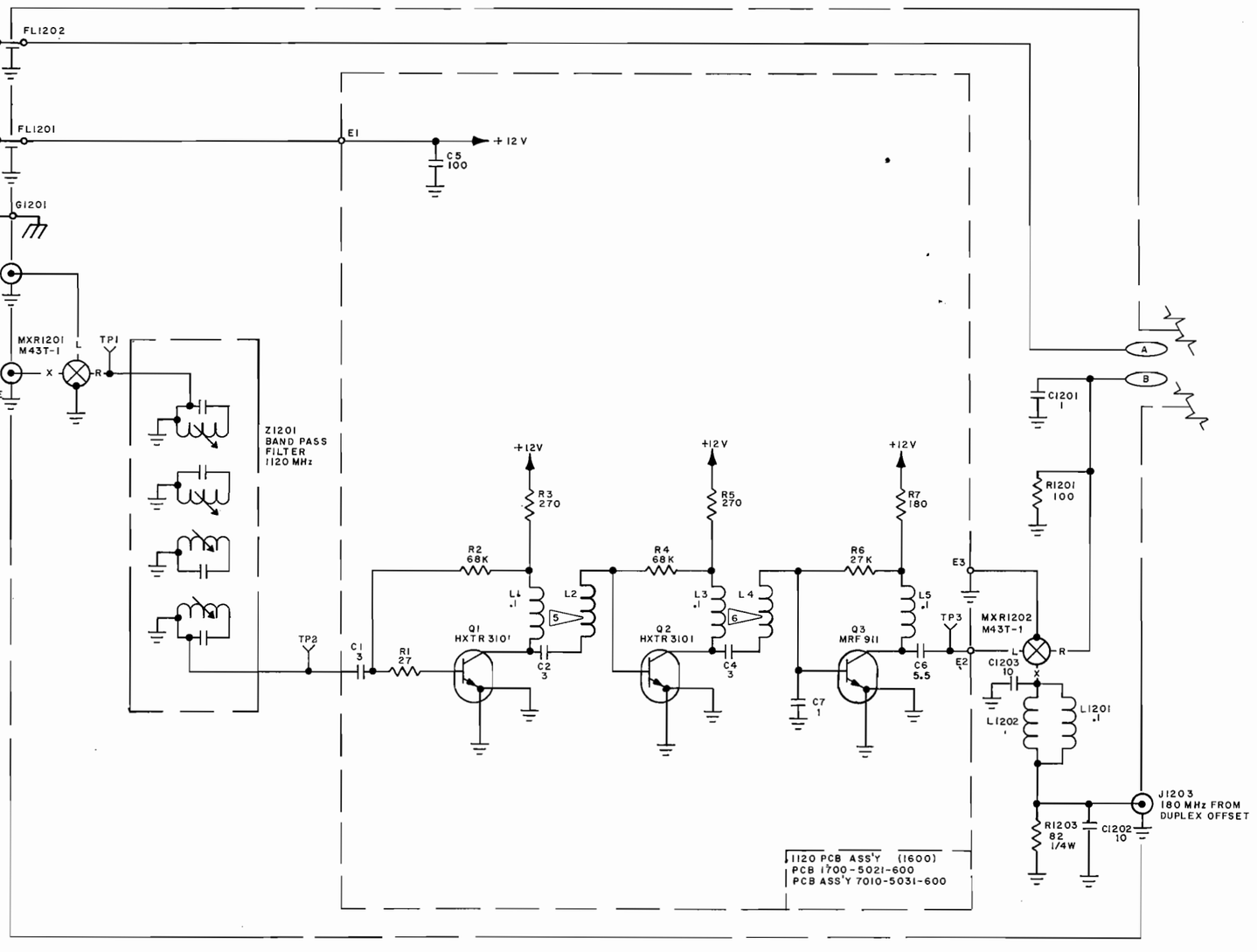
(UNLESS OTHERWISE NOTED)

1. ALL REF NOS CARRY AN ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES:
   A. MECH ASSY
      7005-5043-400 (4400)
      (E.G., R1 IS R4401)
   B. PC BD ASSY 7010-5033-400
      7010-5033-400 (3400)
      (E.G., R1 IS R3401)
2. ALL RESISTORS ARE 1/4 W, 5% TOLERANCE.
3. ALL RESISTANCE IS EXPRESSED IN OHMS.
4. ALL CAPACITANCE IS EXPRESSED IN MICROFARADS.
5. ALL INDUCTANE IS EXPRESSED IN MICROHENRYS.

NOTES:

1. THRU SER. NO. 2133, L13, AND L14 were .1 MICROHENRYS.
2. EFFECTIVE SER. NO. 2519 AND ON.

Figure 7-27 Generator Mixer Module Schematic 0000-5013-400-H2



STANDARDS:
(UNLESS OTHERWISE NOTED)

1. ALL REF NOS CARRY AN ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES:

   1200, 1500, 1600 (E.G., R1 IS R1201, ETC.)

   A. 1300 IF GEN MECH ASSY 7005-5041-500 (1200)
   B. 1300 MHZ PCB ASSY 7010-5031-500 (1500)
   C. 1120 MHZ PCB ASSY 7010-5031-600 (1600)
2. ALL RESISTORS ARE 1/4 W, +/-5% TOLERANCE.
3. ALL RESISTANCE IS EXPRESSED IN OHMS.
4. ALL CAPACITANCE IS EXPRESSED IN PICO-FARADS.
5. ALL INDUCTANCE IS EXPRESSED IN MICRO-HENRYS.

NOTES:

1. NOT USED
2. NOT USED
3. L1502 IS FORMED BY LEAD OF C1503, TRIMMED .3" LONG.
4. L1504 IS FORMED BY LEAD OF C1501, TRIMMED .3" LONG.
5. L1602 IS FORMED BY LEAD OF C1602, TRIMMED .5" LONG.
6. L1604 IS FORMED BY LEAD OF C1604, TRIMMED .5" LONG.
7. R1505 IS SELECT AT TEST (SAT)
   NOMINAL = 18 OHMS
   RANGE = 10 OHMS THRU 100 OHMS.

Figure 7-28 1300 MHz IF Generator Module Schematic (Sheet 1 of 2) 0000-5011-500-C1

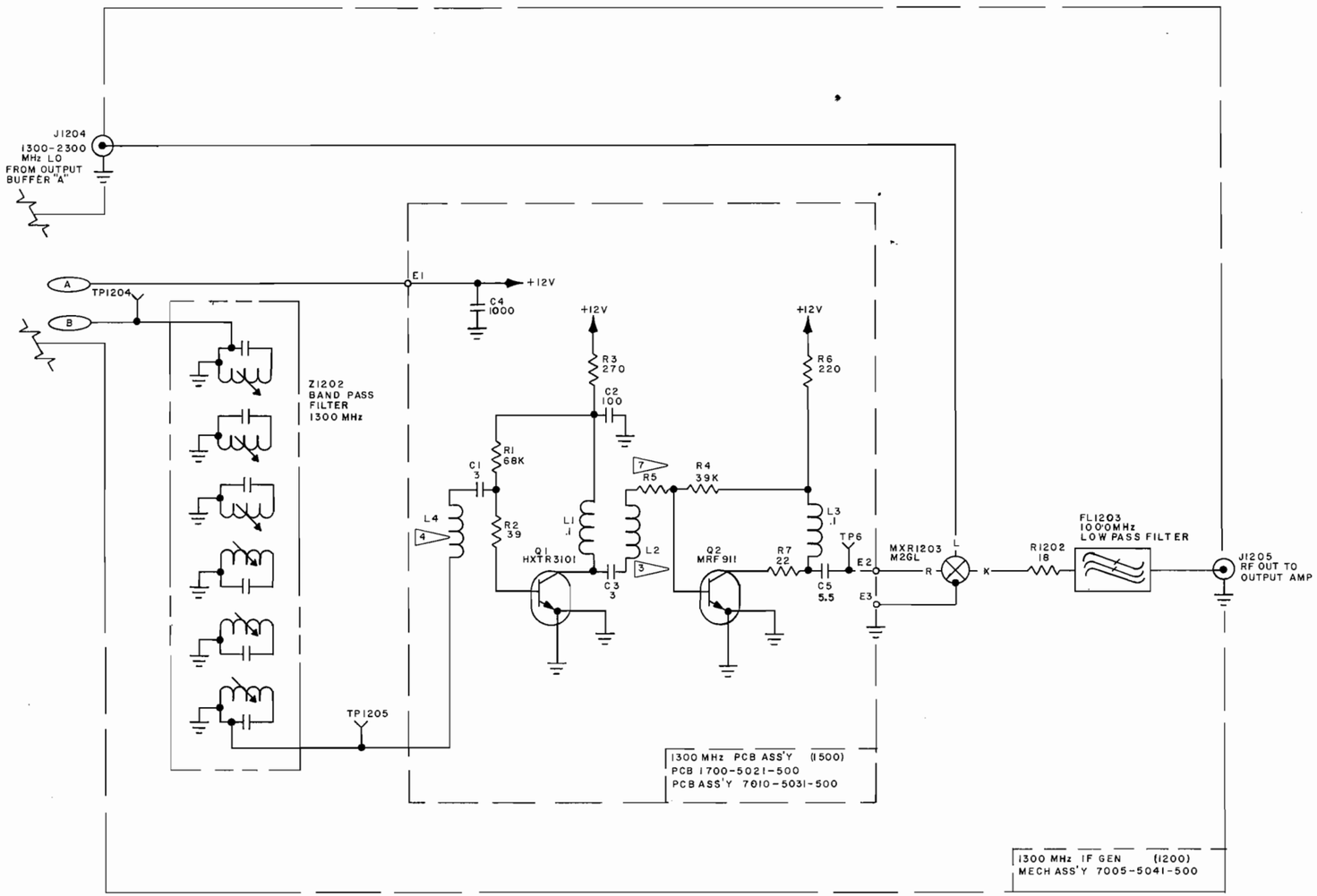
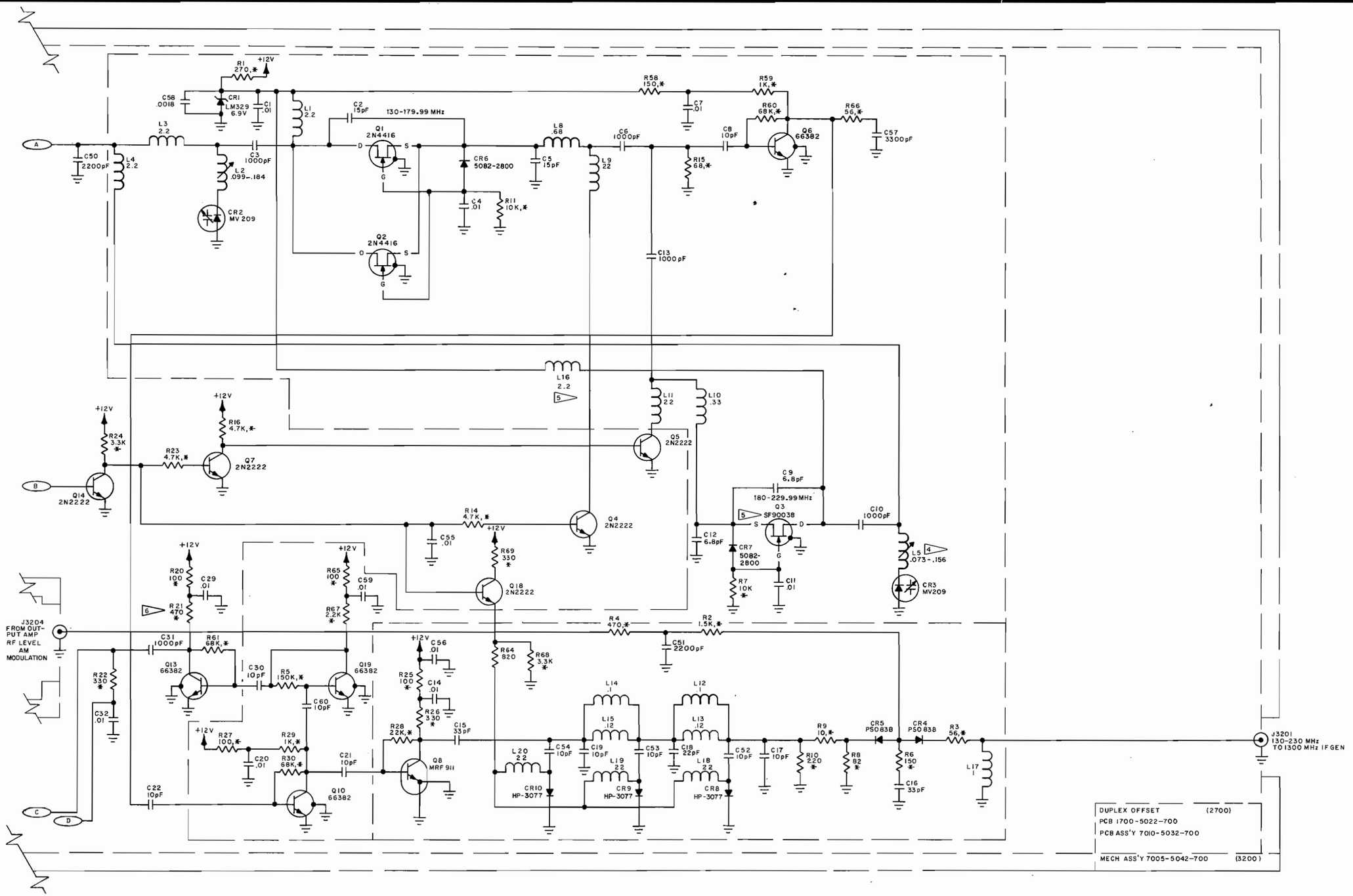
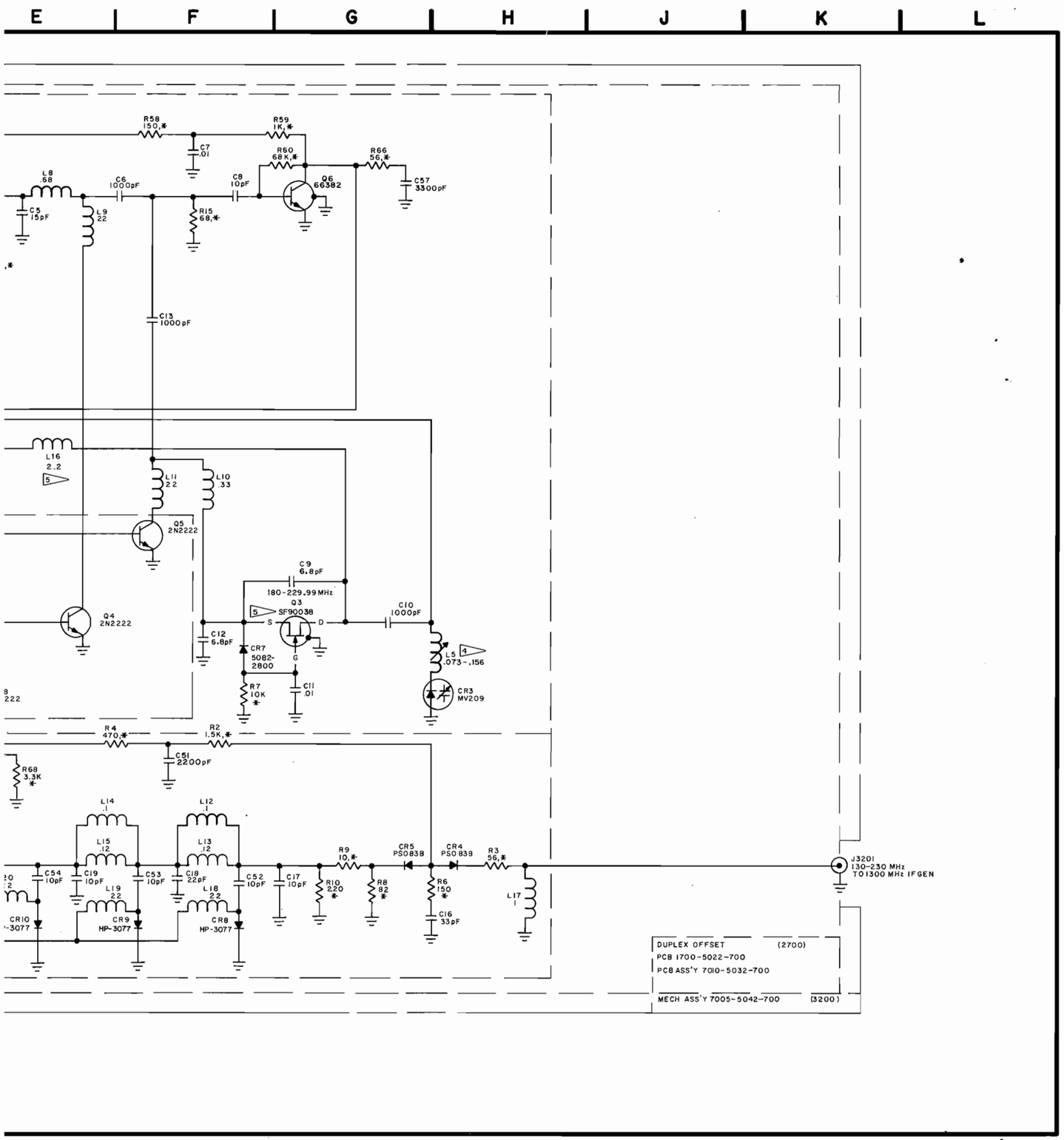


Figure 7-28 1300 MHz IF Generator Module Schematic (Sheet 2 of 2) 0000-5011-500-C1

Figure 7-29 Duplex Offset Module Schematic (Sheet 1 of 2)
0000-5012-700-F2


R1 270,* +12V
C58 .0018
CR1 LM329 6.9V
C1 .01
L1 2.2
C2 15pF
130-179.99 MHz
Q1 2N4416
L3 2.2
C50 2200pF
L4 2.2
C3 1000pF
L2 .099-.184
CR2 MV209
CR6 5082-2800
C4 .01
R11 10K,*
Q2 2N4416
L8 .68
C5 15pF
C6 1000pF
L9 22
C13 1000pF
R58 150,*
C7 .01
R59 1K,*
R60 68K,*
R66 56,*
C8 10pF
Q6 66382
C57 3300pF
R15 68,*
L16 2.2
L11 22
L10 .33
Q5 2N2222
+12V
R24 3.3K,*
R23 4.7K,*
R16 4.7K,*
Q7 2N2222
Q14 2N2222
R14 4.7K,*
Q4 2N2222
C55 .01
C9 6.8pF
180-229.99MHz
Q3 SF90038
C10 1000pF
C12 6.8pF
CR7 5082-2800
R7 10K,*
C11 .01
L5 .073-.156
CR3 MV209
R69 330,*
Q18 2N2222
R20 100,*
C29 .01
R21 470,*
R65 100,*
C59 .01
R67 2.2K,*
J3204 FROM OUTPUT AMP RF LEVEL AM MODULATION
C31 1000pF
R61 68K,*
R4 470,*
R2 1.5K,*
C51 2200pF
R64 820
R68 3.3K,*
C56 .01
R25 100,*
C14 .01
R26 330,*
R22 330,*
C32 .01
Q13 66382
C30 10pF
R5 150K,*
Q19 66382
C60 10pF
R27 100,*
R29 1K,*
C20 .01
R30 68K,*
C21 10pF
C22 10pF
Q10 66382
R28 22K,*
C15 33pF
Q8 MRF 911
L14 .1
L15 .12
L19 .22
L12 .1
L13 .12
L18 .22
L20 .22
C54 10pF
C19 10pF
C53 10pF
C18 22pF
C52 10pF
C17 10pF
CR10 HP-3077
CR9 HP-3077
CR8 HP-3077
R9 10,*
R10 220,*
R8 82,*
CR5 PS083B
CR4 PS083B
R3 56,*
R6 150,*
C16 33pF
L17 .1
J3201 130-230 MHz TO 1300 MHz IF GEN
DUPLEX OFFSET (2700)
PCB 1700-5022-700
PCB ASS'Y 7010-5032-700
MECH ASS'Y 7005-5042-700 (3200)



STANDARDS:

(UNLESS OTHERWISE NOTED)

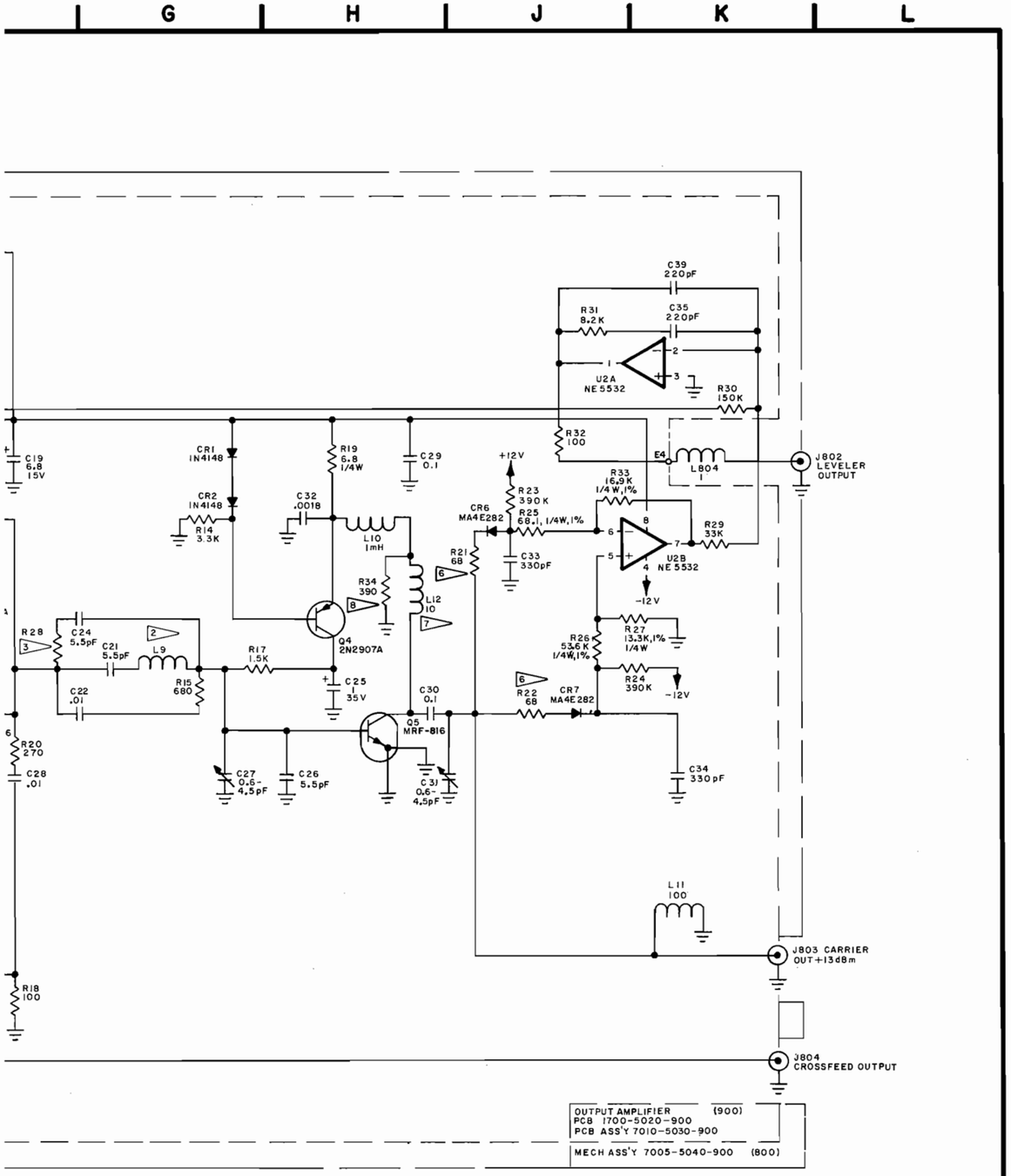
1. ALL REF NOS CARRY AN ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES:
   A. MECH ASSY 7005-5042-700 (3200)
   B. PC BOARD ASSY 7010-5032-700 (2700; E.G., R1 IS R2701).
2. ALL RESISTORS MARKED WITH AN * ARE 1/8 W.
3. ALL RESISTORS ARE 1/4 W, 5% TOLERANCE.
4. ALL RESISTANCE IS EXPRESSED IN OHMS.
5. ALL CAPACITANCE IS EXPRESSED IN MICROFARADS.
6. ALL INDUCTANCE IS EXPRESSED IN MICROHENRYS.

NOTES:

1. NOT USED.
2. NOT USED.
3. EFFECTIVE THRU SER. NO. 2034, U9 PINS 2 AND 7 WERE NOT CONNECTED. R13 WAS 1 KILOHM.
4. THRU SER. NO. 2007, L5 WAS .099 TO .184 MICROHENRYS.
5. THRU SER. NO. 2147, L16 WAS 6.8 MICROHENRYS AND Q3 WAS 2N4416. CR8, CR9, CR10 WERE MA 47047.
6. PRIOR TO SER. NO. 2768 R21 WAS 680 OHMS.

Figure 7-29 Duplex Offset Module Schematic (Sheet 2 of 2) 0000-5012-700-F2

P/O P805
+12V ON GEN
-12V
AM MOD INPUT
FL801
FL802
FL804
L801
L802
L805
E1
E2
E5
L1 22
C5 .01
-12V
C801 .047
L7 2.2
C39 220pF
R31 8.2K
C35 220pF
U2A NE5532
R30 150K
R32 100
E4
L804
J802 LEVELER OUTPUT
C2 .001
C3 0.1
C7 6.8 15V
R4 220 1/4W
C36 .0018
L3 22
C11 0.1
R8 2.2K
C13 6.8 15V
C37 .0018
R11 33 1/2W
L6 22
C19 6.8 15V
CR1 IN4148
CR2 IN4148
R14 3.3K
R19 6.8 1/4W
C29 0.1
C32 .0018
L10 1mH
+12V
R23 390 K
R25 68.1, 1/4W, 1%
CR6 MA4E282
R33 16.9K 1/4W, 1%
R29 33K
U2B NE5532
C33 330pF
R21 68
C38 .0018
L8 .47
R10 680
Q2 2N2907A
R34 390
L12 10
Q4 2N2907A
C8 .01
C9 .01
R2 330
R3 2.2K
L4
C12 3pF
R6 1.5K
C10 3pF
R7 100
R9 1.5K
R5 3.3K
C16 0.1
R28
C24 5.5pF
C21 5.5pF
L9
R17 1.5K
C22 .01
R15 680
C25 1 35V
R27 13.3K, 1% 1/4W
R26 53.6K 1/4W, 1%
R24 390K
-12V
R22 68
CR7 MA4E282
C30 0.1
C34 330 pF
J801 CARRIER IN -25 dBm
C1 .01
U1 GPD 1062
L2
C6 3pF
C4 0.1
R1
Q1 HXTR-3101
Q3 MRF-816
R20 270
C28 .01
C15 0.6-4.5pF
C17 5.5pF
C27 0.6-4.5pF
C26 5.5pF
Q5 MRF-816
C31 0.6-4.5pF
L11 100
P/O P805
+12V ON CROSSFEED
GND
FL803
G801
L803
E3
L5 22
R12 3.3K
C18 .01
C14 .01
CR3 MA47047
CR4 MA47047
CR5 MA47047
R13 220
C20 470pF
R16 220
C23 470pF
R18 100
J803 CARRIER OUT +13dBm
J804 CROSSFEED OUTPUT
OUTPUT AMPLIFIER (900)
PCB 1700-5020-900
PCB ASS'Y 7010-5030-900
MECH ASS'Y 7005-5040-900 (800)



STANDARDS:

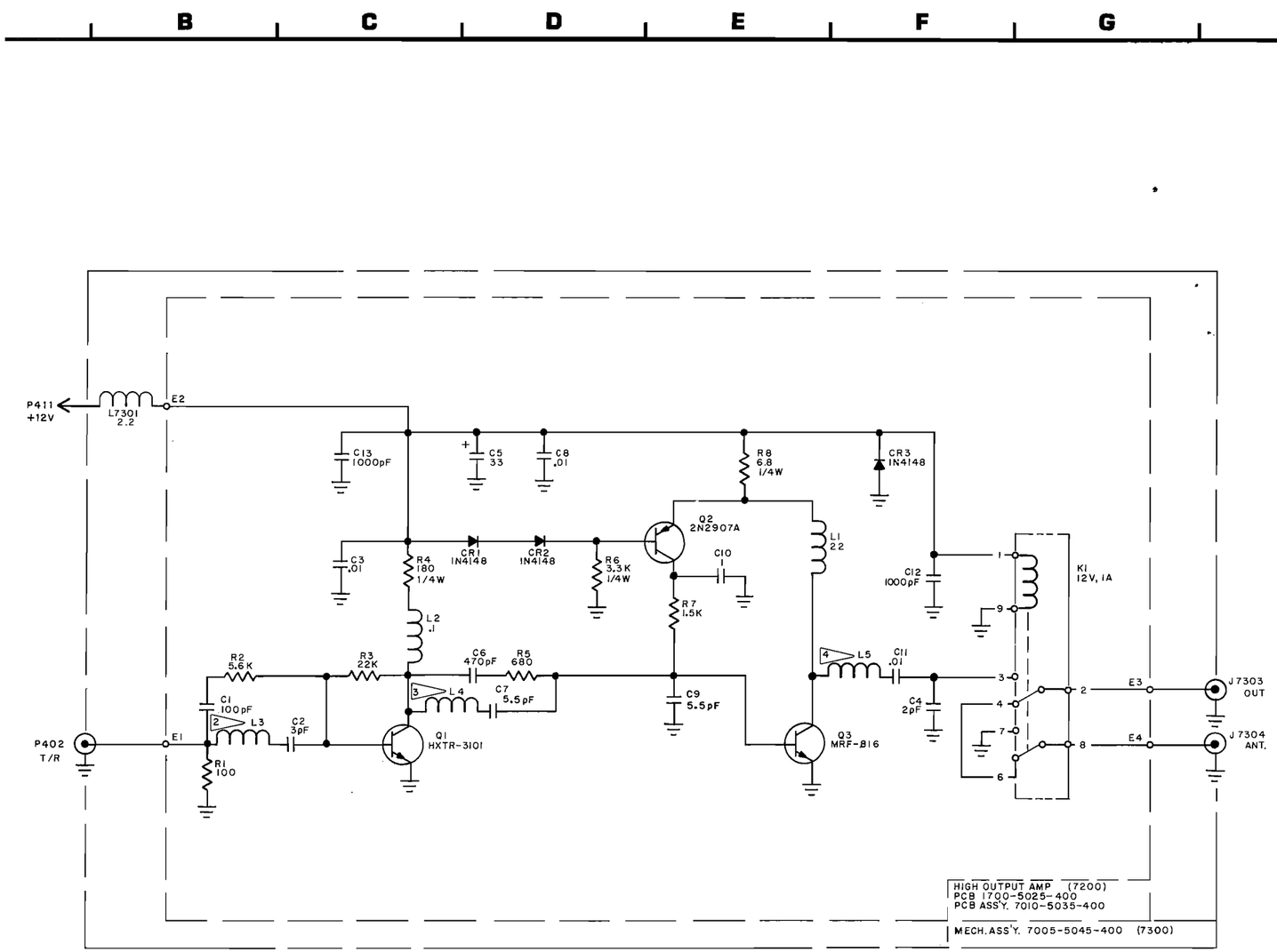
(UNLESS OTHERWISE NOTED)

1. ALL REF NOS CARRY AN ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES:
   A. MECH ASSY 7005-5040-900 (800)
   B. PC BOARD ASSY 7010-5030-900 (900)
2. ALL RESISTORS ARE 1/8 W, 5% TOLERANCE.
3. ALL RESISTANCE IS EXPRESSED IN OHMS.
4. ALL CAPACITANCE IS EXPRESSED IN MICROFARADS.
5. ALL INDUCTANCE IS EXPRESSED IN MICROHENRYS.

NOTES:

1. NOT USED.
2. REF NOS USED W/O PART NOS:
   L2 IS .6" LG FORMED FROM LEAD OF C6,
   L4 IS .5" LG FORMED FROM LEAD OF C12,
   L9 IS .6" LG FORMED FROM LEAD OF C21.
3. R28 IS SELECTED AT TEST (SAT)
   NOMINAL = 100 OHMS
   RANGE = 47 TO 330 OHMS
4. THRU SER. NO. 2166:
   R1 IS SELECTED AT TEST (SAT)
   NOMINAL = 150 OHMS
   RANGE = 47 TO 220 OHMS
   EFFECTIVE SER. NO. 2167 AND ON:
   R1 IS SAT
   NOMINAL = 120 OHMS
   RANGE = 47 TO 220 OHMS
5. R7 IS SAT
   NOMINAL = 100 OHMS
   RANGE = 47 TO 220 OHMS
6. FOR OPTION 1 (7010-5030-901), R21 AND R22 ARE 150 OHMS, 5%, 1/8 W
7. THRU SER. NO. 2582, L12 WAS 1.5 MICROHENRYS
8. EFFECTIVE SER. NO. 2783 AND ON

Figure 7-30 Output Amplifier Module Schematic 0000-5010-900-D4



STANDARDS:
(UNLESS OTHERWISE NOTED)

1. ALL REF NOS CARRY AN ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES: 7200, 7300 (E.G., R1 IS R7201, ETC.).

   A. MECH ASSY 7005-5045-400 (7300)
   B. PCB ASSY 7010-5035-400 (7200)
   C.
   D.

2. ALL RESISTORS ARE 1/8 W, 5% TOLERANCE.

3. ALL RESISTANCE IS EXPRESSED IN OHMS.

4. ALL CAPACITANCE IS EXPRESSED IN MICROFARADS.

5. ALL INDUCTANCE IS EXPRESSED IN MICROHENRYS.

NOTES:

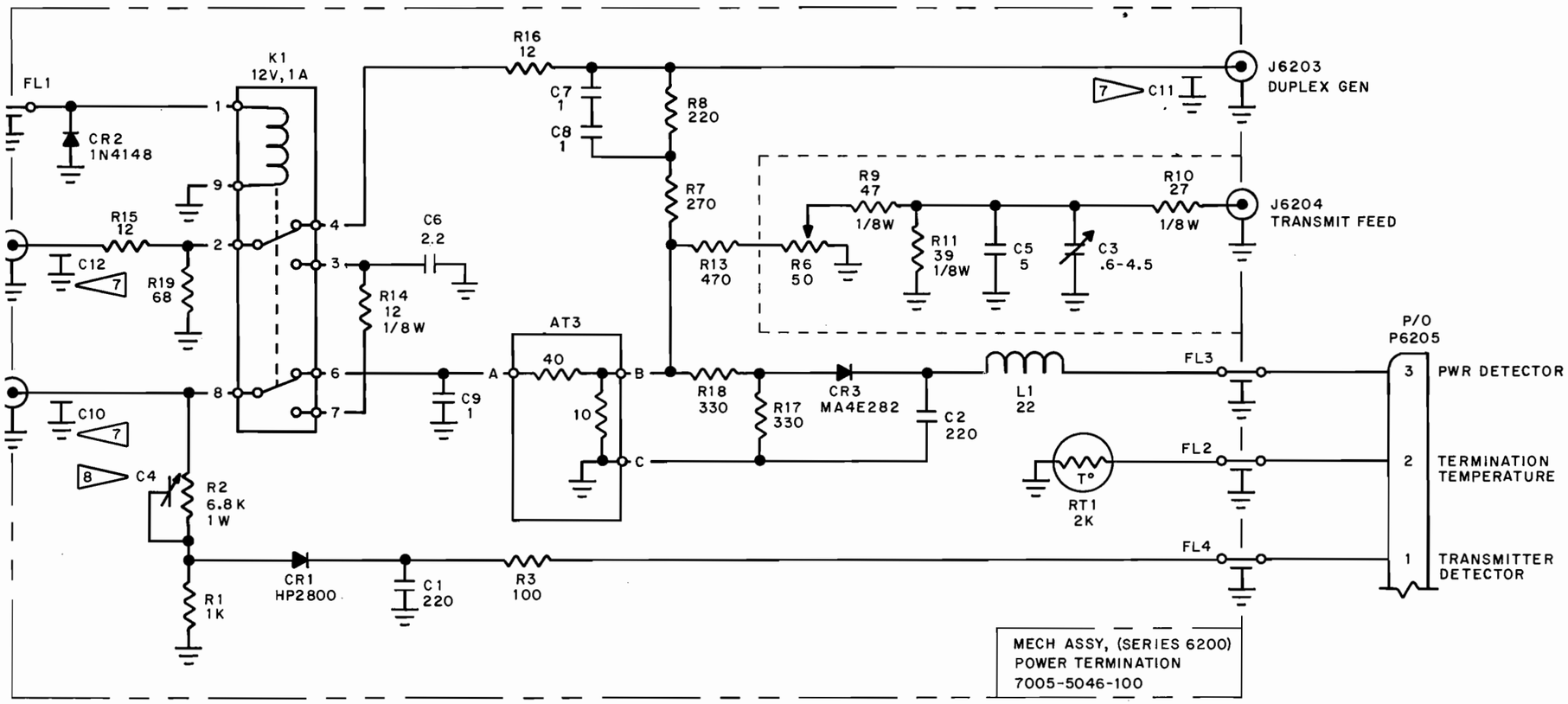
1. LAST REF NOS USED:
   C13, CR3, L5, Q3, E4, J7304, R8, K1

2. L3 IS A .4" LENGTH OF LEAD FROM C2.

3. L4 IS A .5" LENGTH OF LEAD FROM C7.

4. L5 IS A .5" LENGTH OF LEAD FROM C11.

Figure 7-31 High Output Amplifier Module Schematic 0000-5015-400-B3

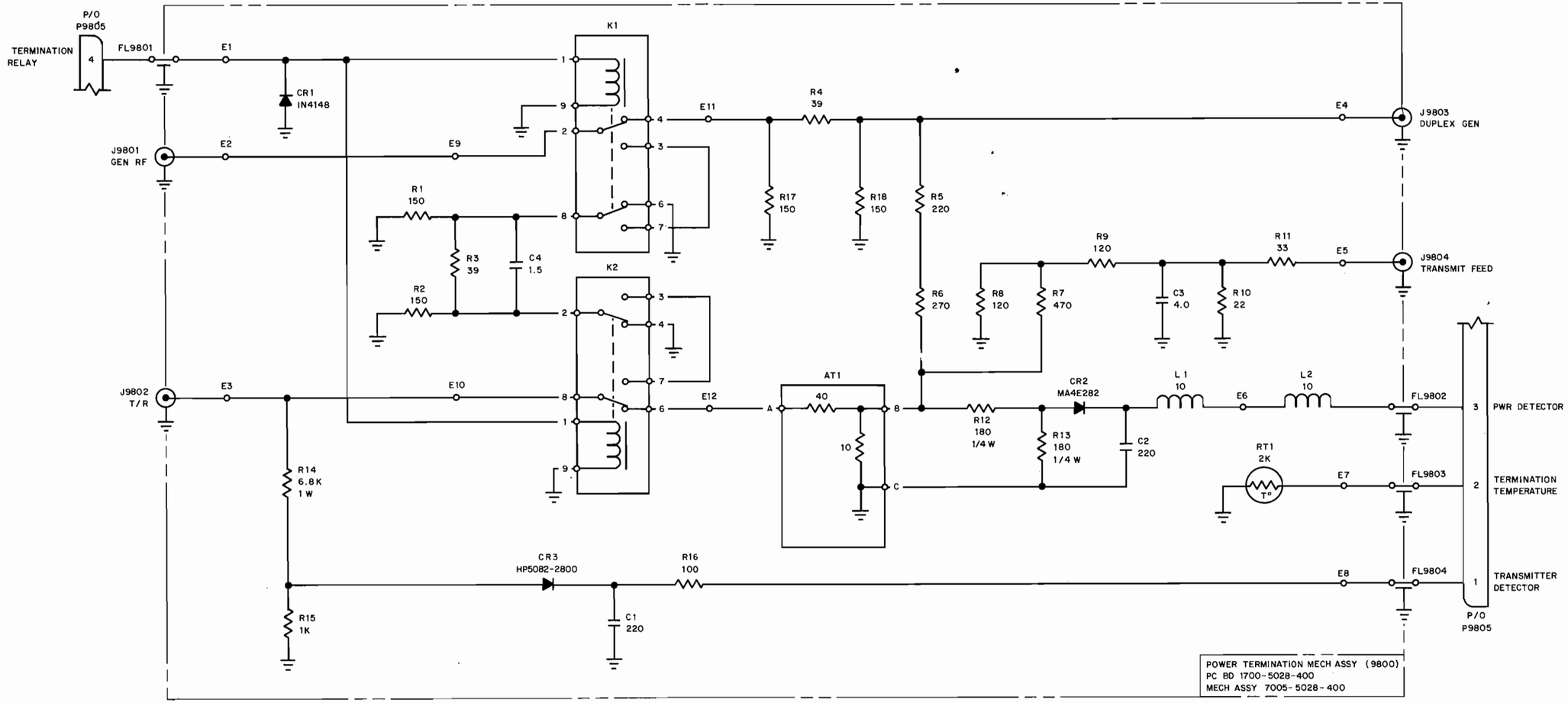


EFFECTIVE SER. NO. 1738 THRU 1993

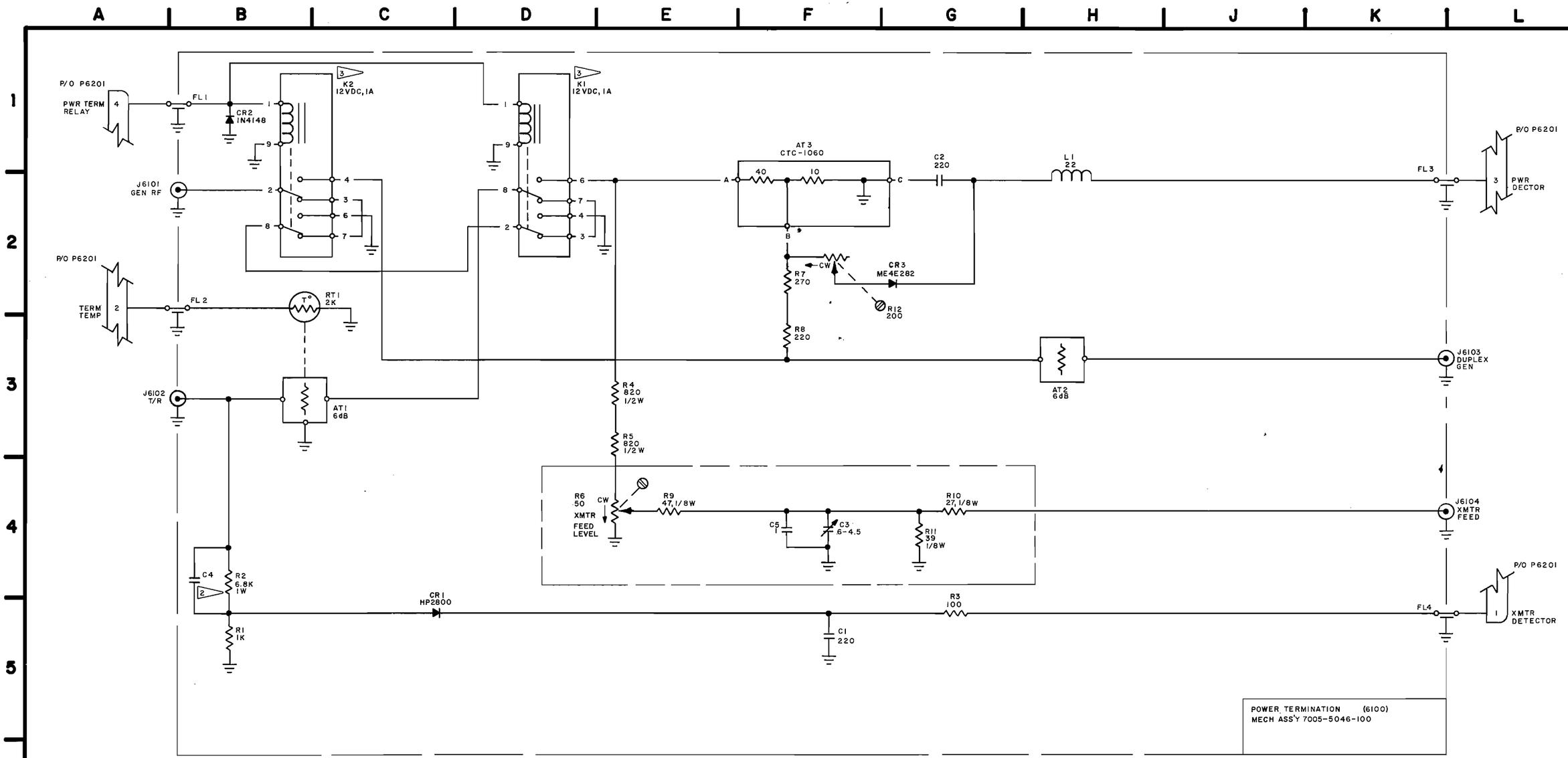
STANDARDS & NOTES:

1. ALL REF NOS CARRY AN ASSIGNED DESIGNATOR SERIES. EFFECTIVE SER. NO. 1994, THIS SCHEMATIC CARRIES SERIES 9800 (E.G., R1 IS R9801). THRU SER. NO. 1993, THIS SERIES WAS 6200 (E.G, R1 WAS R6201).
2. MECH ASSY EFFECTIVE SER. NO. 1994 AND ON IS 7005-5048-400. THRU SER. NO. 1993, THIS WAS 7005-5016-100.
3. ALL RESISTORS ARE 1/4 W, ±5% TOLERANCE.
4. ALL RESISTANCE IS EXPRESSED IN OHMS.
5. ALL CAPACITANCE IS EXPRESSED IN PICO-FARADS.
6. ALL INDUCTANCE IS EXPRESSED IN MICRO-HENRYS.
7. THRU SER. NO. 1993, C10, C11 AND C12 ARE NON-VALUED FABRICATED CAPACITORS.
8. THRU SER. NO. 1993, C4 IS A NON-VALUED FABRICATED VARIABLE CAPACITOR. CAPACITANCE IS VARIED BY MOVING C4 RELATIVE TO R2.

Figure 7-32 Power Termination Module Schematic
0000-5018-400-A1/0000-5016-100-G5



EFFECTIVE SER. NO. 1994 AND ON



STANDARDS
(UNLESS OTHERWISE NOTED):

1. ALL REF NOS CARRY AN ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES 6100 (I.E., R1 IS R6101).

   A. MECH ASSY - 7005-5046-100
   B. PCB ASSY - 7010-5036-100

2. ALL RESISTORS ARE 1/4 W, ±5%.

3. ALL RESISTANCE IS EXPRESSED IN OHMS.

4. ALL CAPACITANCE IS EXPRESSED IN PICOFARADS.

5. ALL INDUCTANCE IS EXPRESSED IN MICROHENRYS.

NOTES:

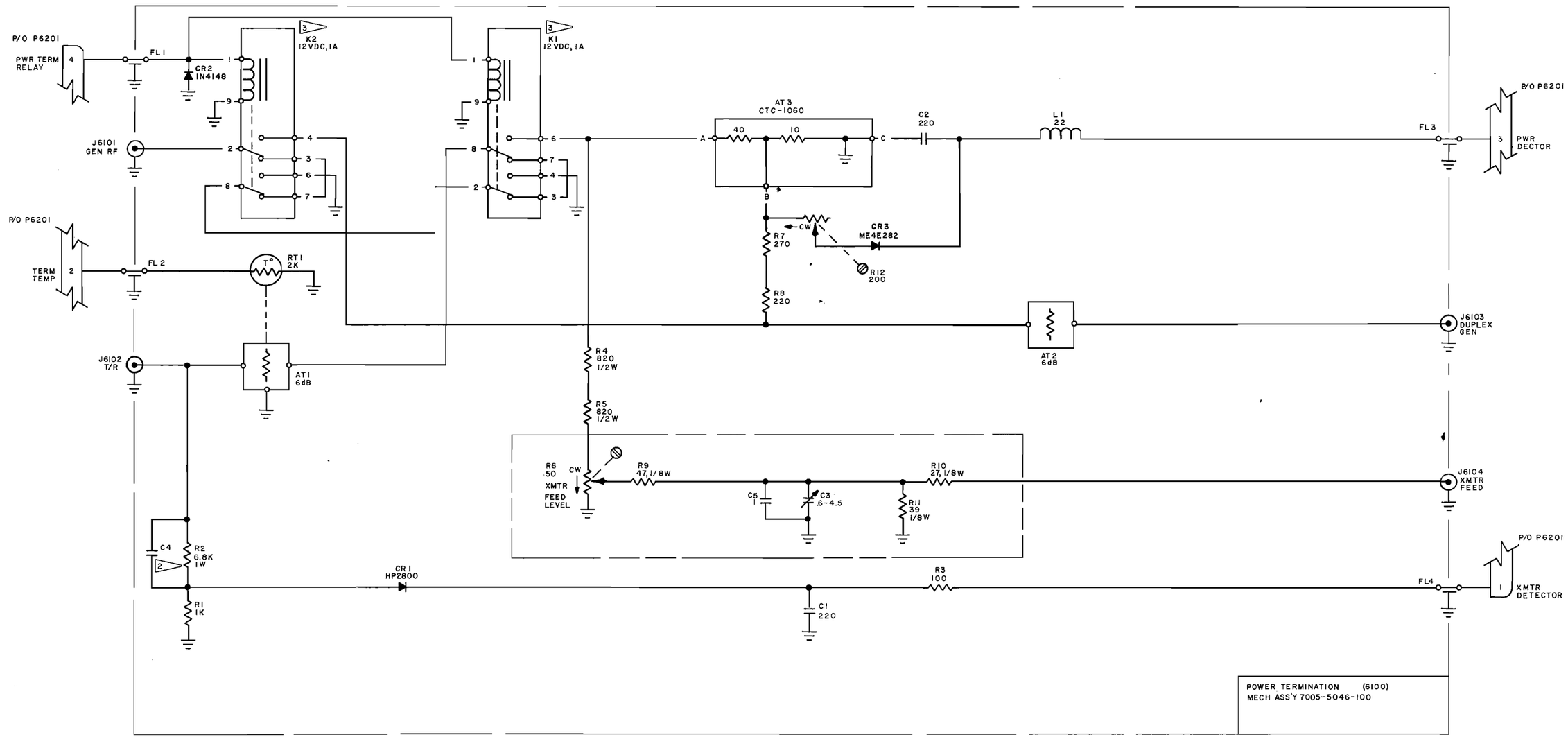
1. NOT USED.

2. C4 IS A NON-VALUED FABRICATED CAPACITOR.

3. K1 AND K2 ARE SHOWN IN ENERGIZED STATE.

THRU SER. NO. 1737

Figure 7-32a Power Termination Module Schematic 0000-5016-100-G1



STANDARDS
(UNLESS OTHERWISE NOTED):

1. ALL REF NOS CARRY AN ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES 6100 (I.E., R1 IS R6101).

   A. MECH ASSY - 7005-5046-100
   B. PCB ASSY - 7010-5036-100

2. ALL RESISTORS ARE 1/4 W, ±5%.

3. ALL RESISTANCE IS EXPRESSED IN OHMS.

4. ALL CAPACITANCE IS EXPRESSED IN PICOFARADS.

5. ALL INDUCTANCE IS EXPRESSED IN MICROHENRYS.

NOTES:

1. NOT USED.

2. C4 IS A NON-VALUED FABRICATED CAPACITOR.

3. K1 AND K2 ARE SHOWN IN ENERGIZED STATE.

THRU SER. NO. 1737

Figure 7-32a Power Termination Module Schematic 0000-5016-100-G1

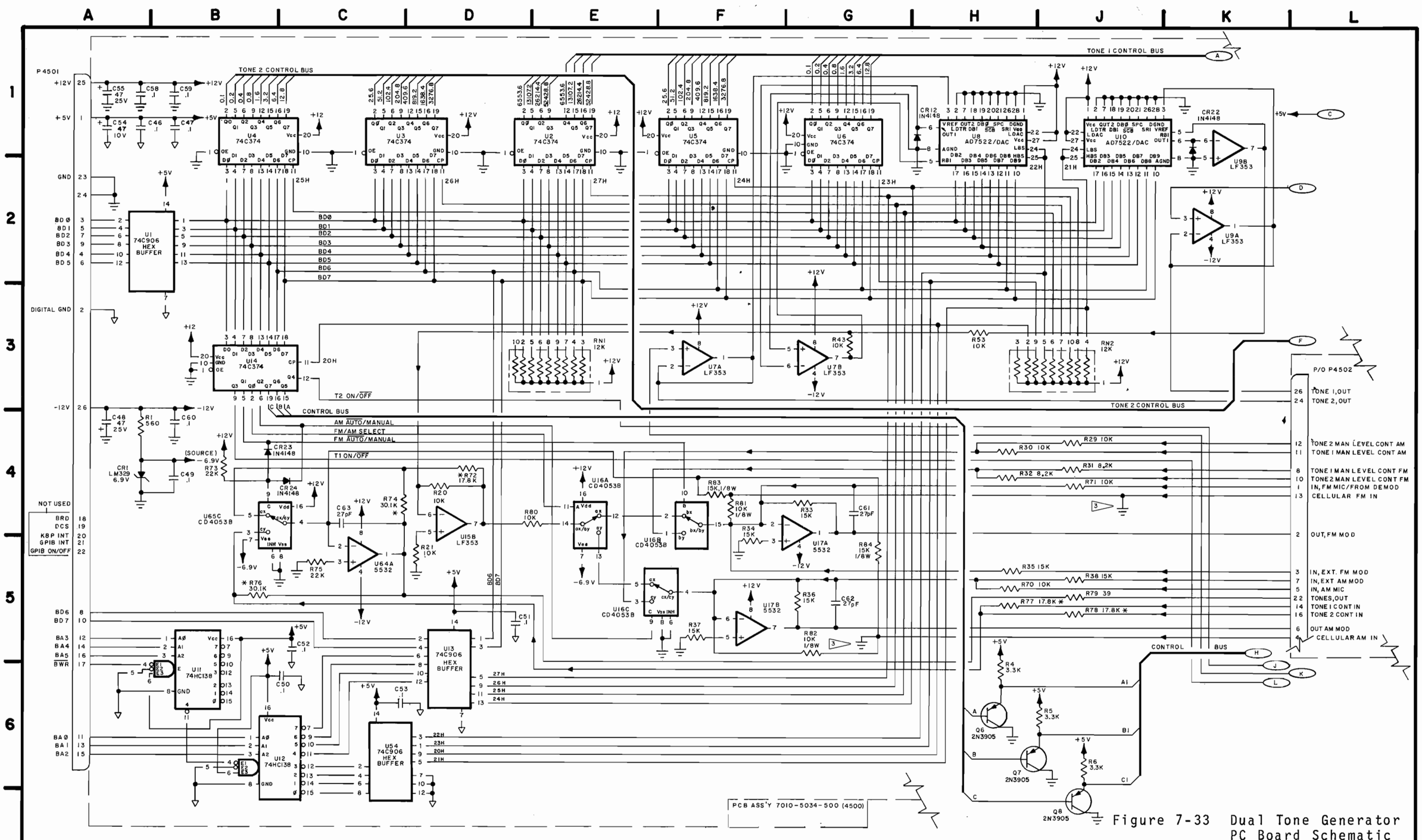
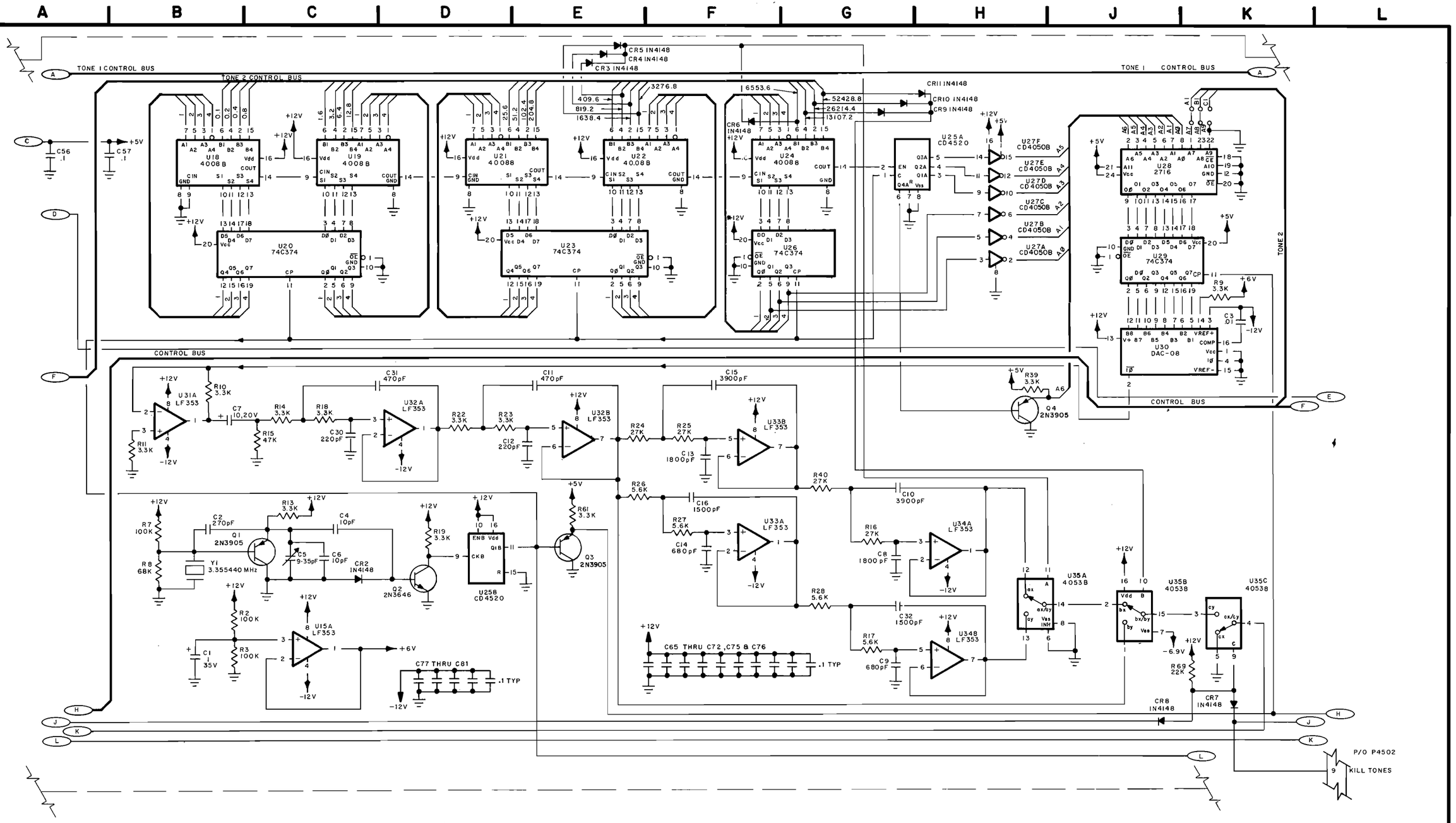


Figure 7-33 Dual Tone Generator PC Board Schematic (Sheet 1 of 3) 0000-5014-500-D



STANDARDS:
(UNLESS OTHERWISE NOTED)

1. ALL REF NOS CARRY AN ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES: 4500 (E.G., R1 IS R4501, ETC).
   - A. MECH ASSY
   - B. PCB ASSY 7010-5034-500
2. ALL RESISTORS ARE 1/4 W, ±5% TOLERANCE.
2a. RESISTORS WITH * ARE ±1% TOLERANCE.
3. ALL RESISTANCE IS EXPRESSED IN OHMS.
4. ALL CAPACITANCE IS EXPRESSED IN MICROFARADS.
5. ALL INDUCTANCE IS EXPRESSED IN MICROHENRYS.

NOTES:

1. NOT USED.
2. NOT USED.
3. CIRCUIT IS GROUNDED ONLY WHEN CELLULAR OPTION IS NOT INSTALLED.

Figure 7-33 Dual Tone Generator PC Board Schematic (Sheet 2 of 3) 0000-5014-500-D

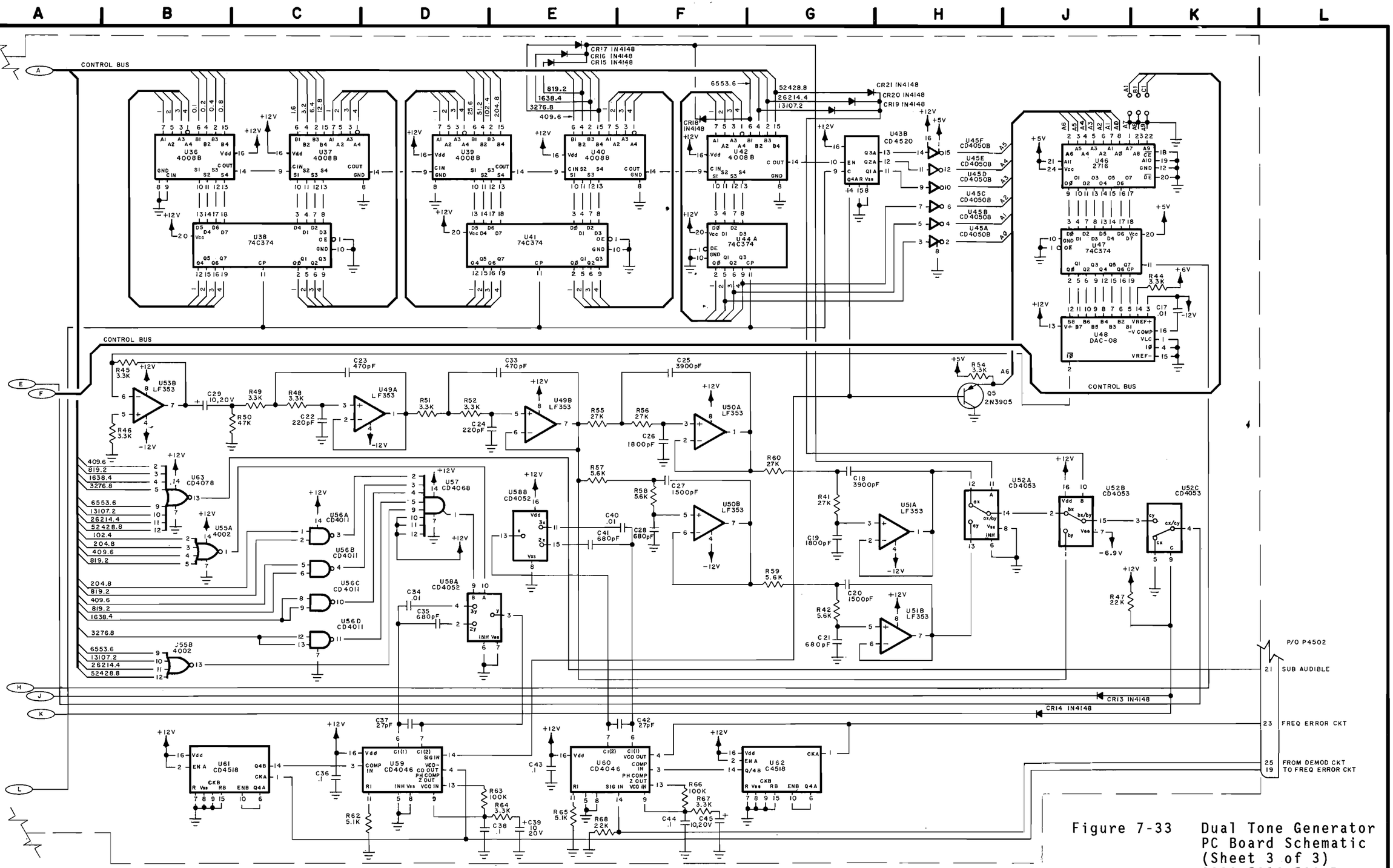
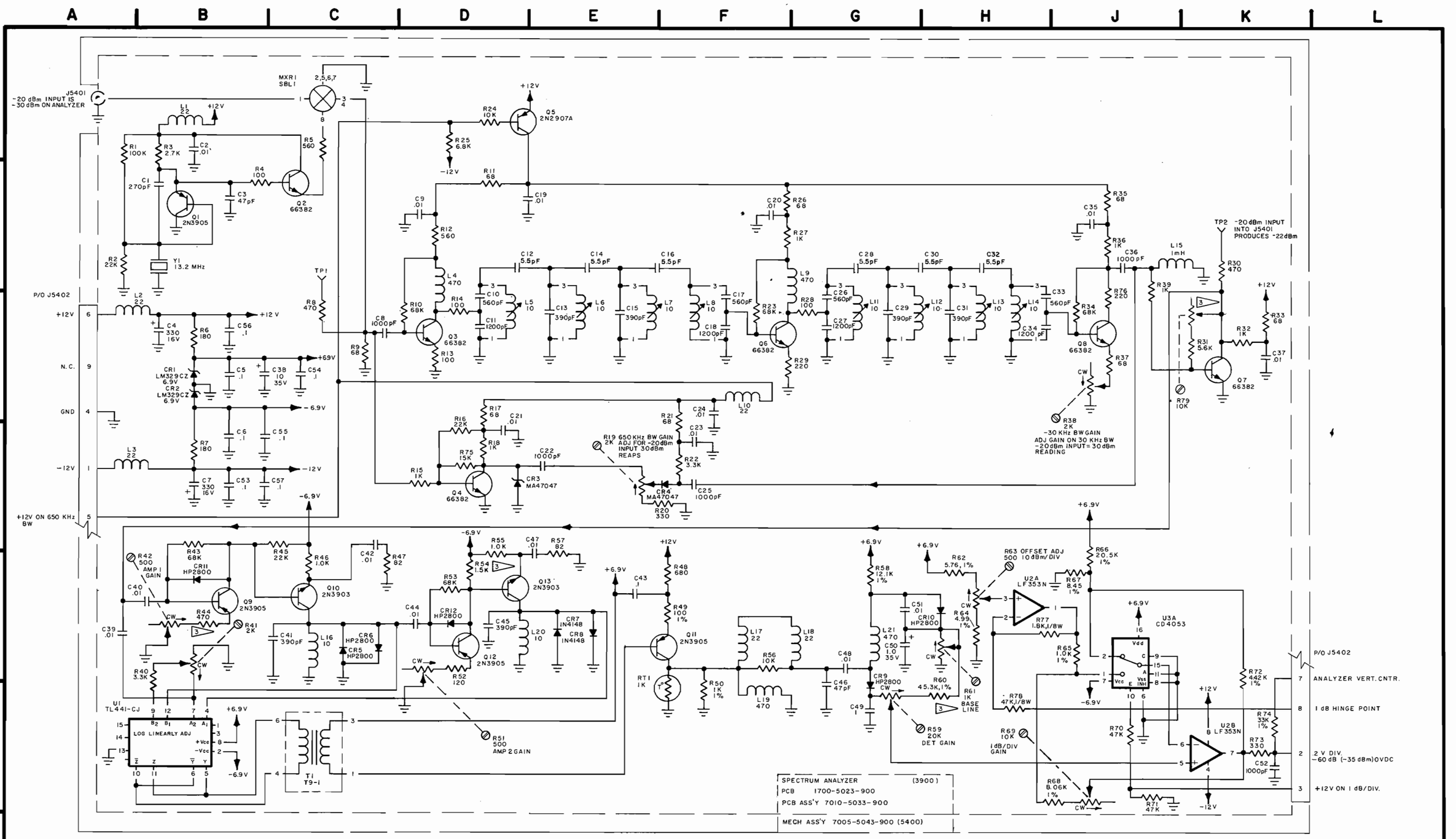


Figure 7-33 Dual Tone Generator PC Board Schematic (Sheet 3 of 3) 0000-5014-500-D

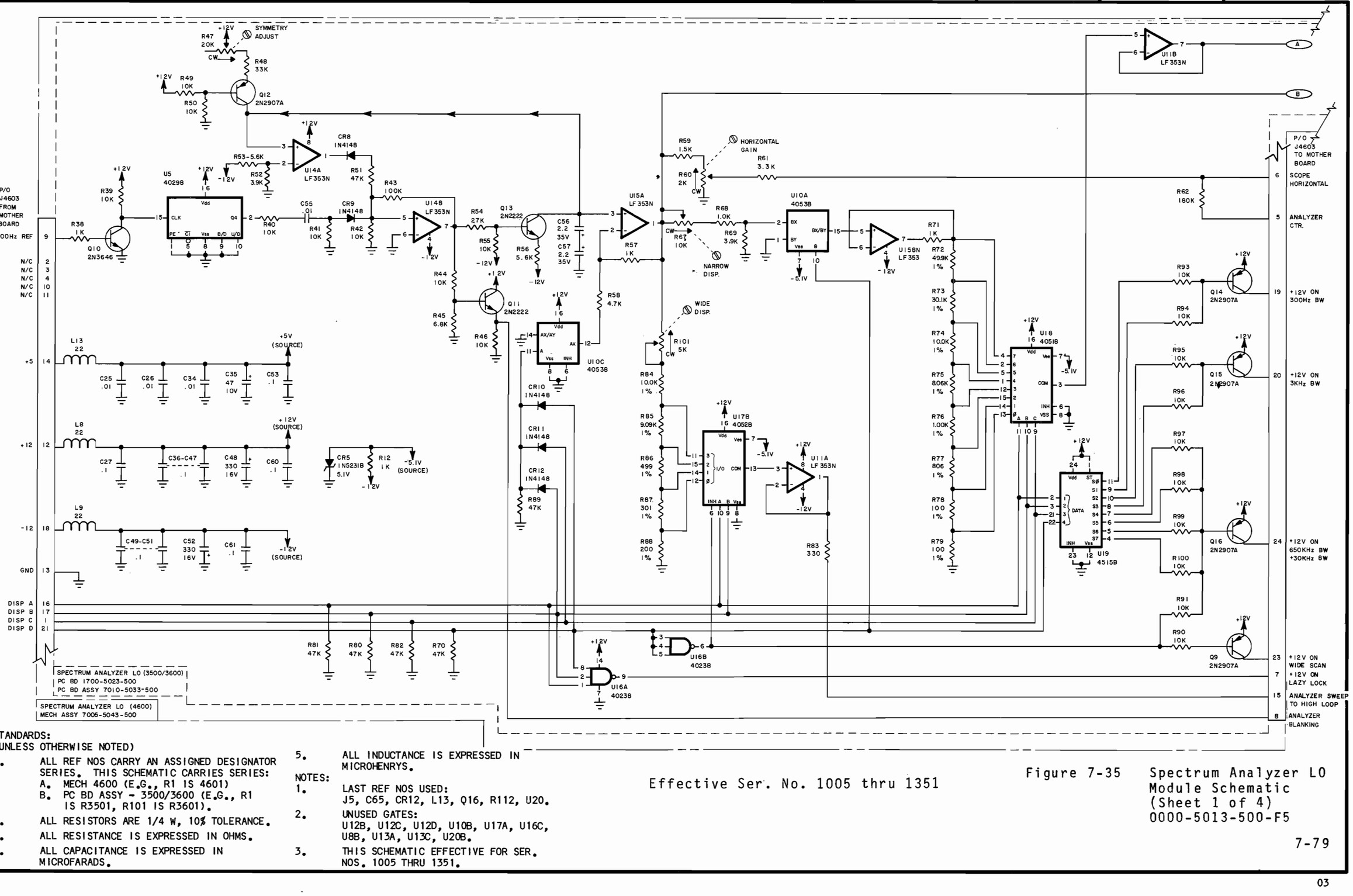


NOTES:

1. ALL REF NOS CARRY AN ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES:
   A. MECH ASSY 7005-5043-900 (5400)
   B. PC BOARD ASSY 7010-5033-900 (3900) (E.G., R1 IS R3901)
2. NOT USED

3. PRIOR TO SER. NO. 2391, R54 WAS 2.2K AND R44 WAS 180 OHMS.

Figure 7-34 Spectrum Analyzer IF Module Schematic 0000-5013-900-D



STANDARDS:
(UNLESS OTHERWISE NOTED)

1. ALL REF NOS CARRY AN ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES:
   A. MECH 4600 (E.G., R1 IS 4601)
   B. PC BD ASSY - 3500/3600 (E.G., R1 IS R3501, R101 IS R3601).
2. ALL RESISTORS ARE 1/4 W, 10% TOLERANCE.
3. ALL RESISTANCE IS EXPRESSED IN OHMS.
4. ALL CAPACITANCE IS EXPRESSED IN MICROFARADS.
5. ALL INDUCTANCE IS EXPRESSED IN MICROHENRYS.

NOTES:

1. LAST REF NOS USED:
   J5, C65, CR12, L13, Q16, R112, U20.
2. UNUSED GATES:
   U12B, U12C, U12D, U10B, U17A, U16C, U8B, U13A, U13C, U20B.
3. THIS SCHEMATIC EFFECTIVE FOR SER. NOS. 1005 THRU 1351.

Effective Ser. No. 1005 thru 1351

Figure 7-35 Spectrum Analyzer LO Module Schematic (Sheet 1 of 4) 0000-5013-500-F5

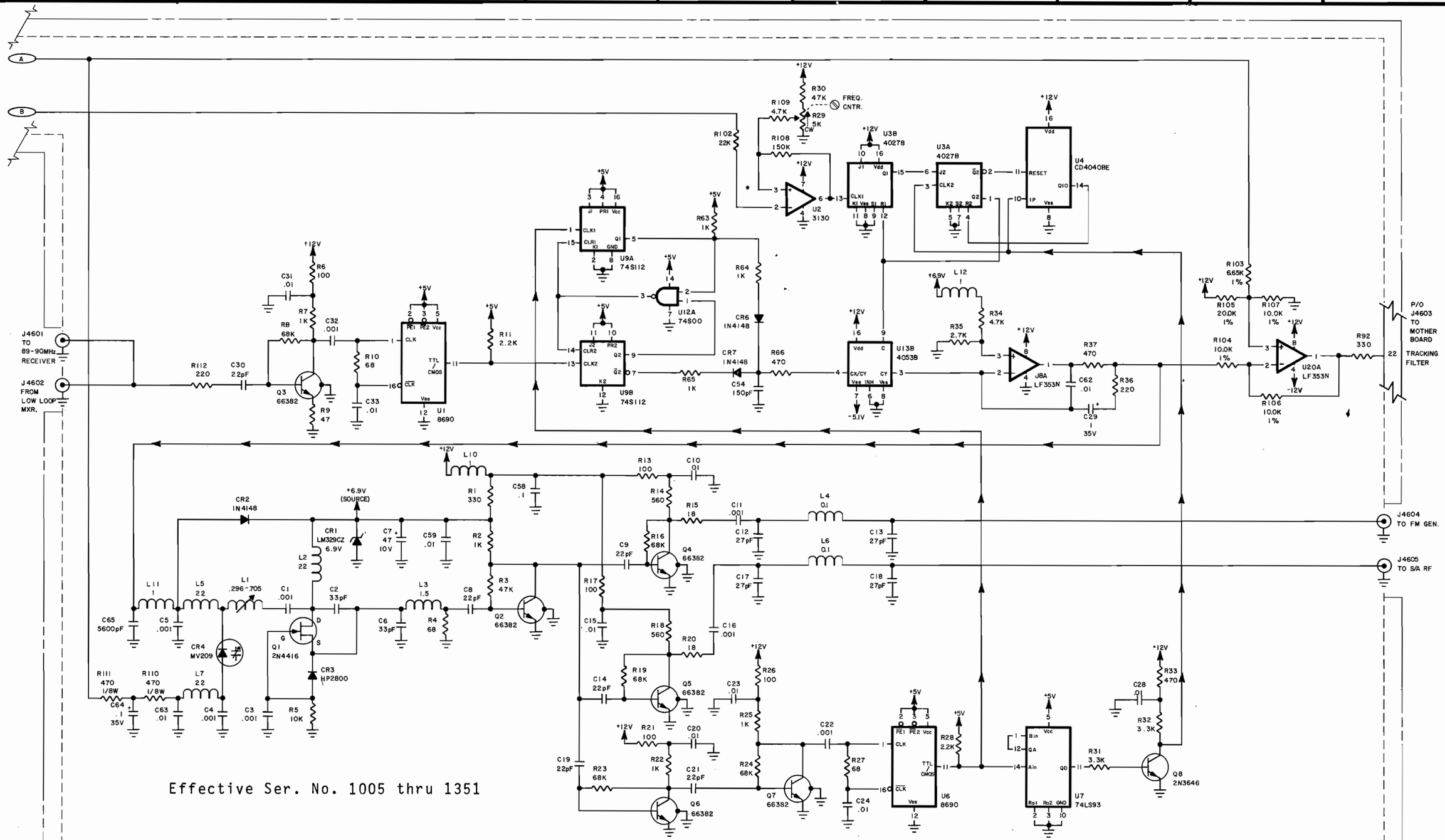
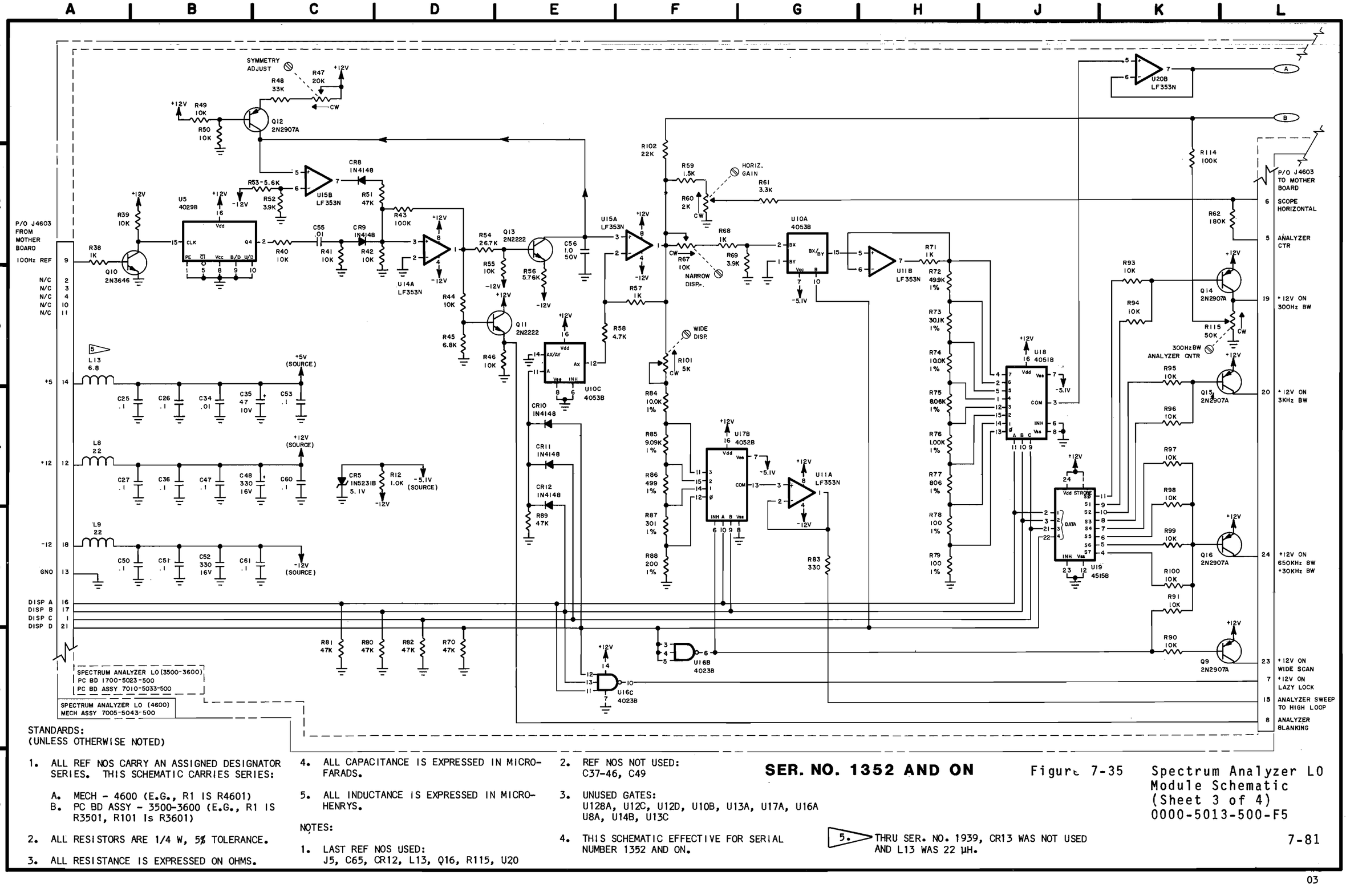


Figure 7-35 Spectrum Analyzer LO Module Schematic (Sheet 2 of 4)
0000-5013-500-F5



STANDARDS:
(UNLESS OTHERWISE NOTED)

1. ALL REF NOS CARRY AN ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES:
   A. MECH - 4600 (E.G., R1 IS R4601)
   B. PC BD ASSY - 3500-3600 (E.G., R1 IS R3501, R101 Is R3601)
2. ALL RESISTORS ARE 1/4 W, 5% TOLERANCE.
3. ALL RESISTANCE IS EXPRESSED ON OHMS.
4. ALL CAPACITANCE IS EXPRESSED IN MICROFARADS.
5. ALL INDUCTANCE IS EXPRESSED IN MICROHENRYS.

NOTES:

1. LAST REF NOS USED:
   J5, C65, CR12, L13, Q16, R115, U20
2. REF NOS NOT USED:
   C37-46, C49
3. UNUSED GATES:
   U128A, U12C, U12D, U10B, U13A, U17A, U16A
   U8A, U14B, U13C
4. THIS SCHEMATIC EFFECTIVE FOR SERIAL NUMBER 1352 AND ON.

5. THRU SER. NO. 1939, CR13 WAS NOT USED AND L13 WAS 22 µH.

SER. NO. 1352 AND ON

Figure 7-35 Spectrum Analyzer LO Module Schematic (Sheet 3 of 4) 0000-5013-500-F5

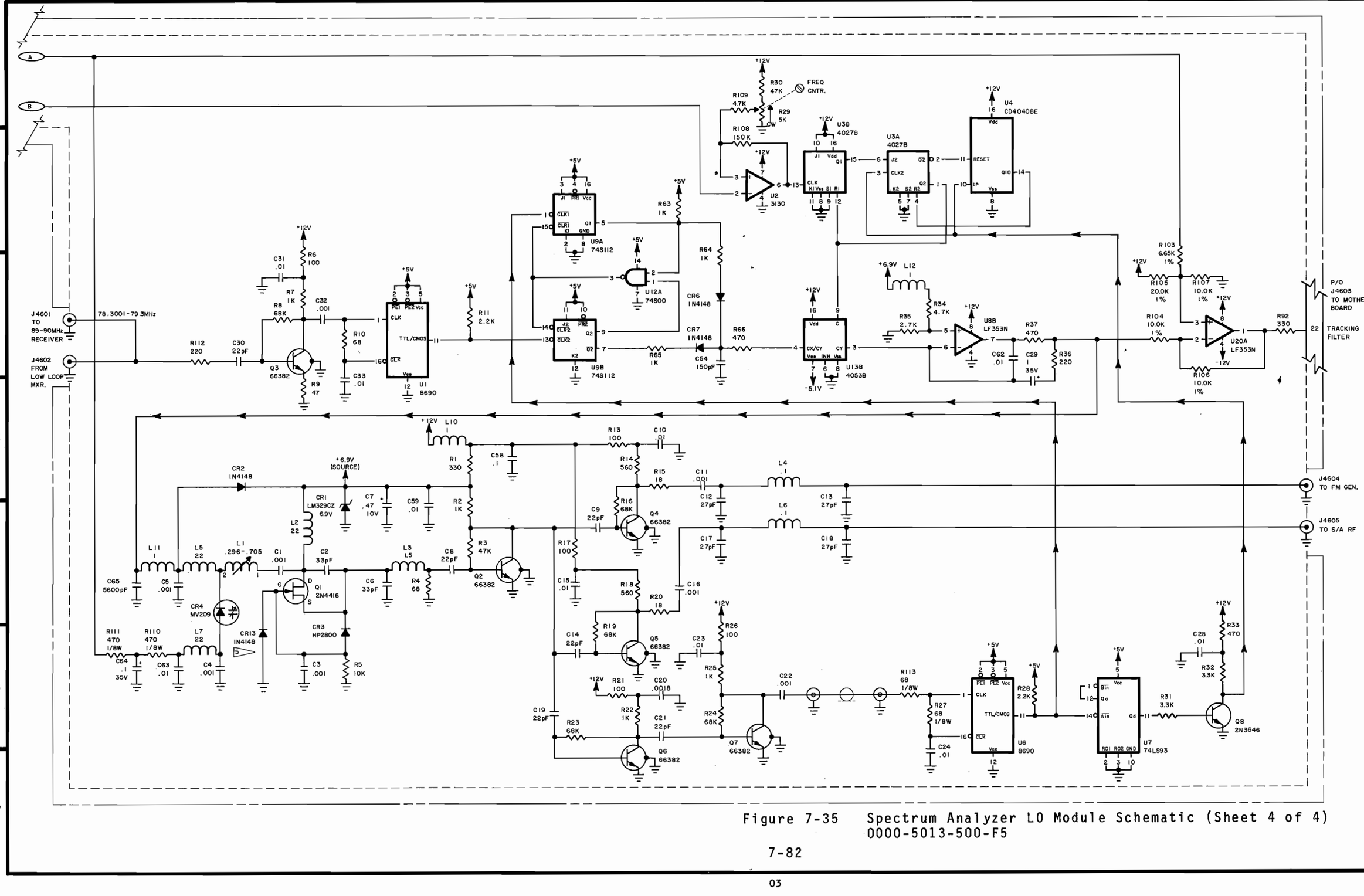
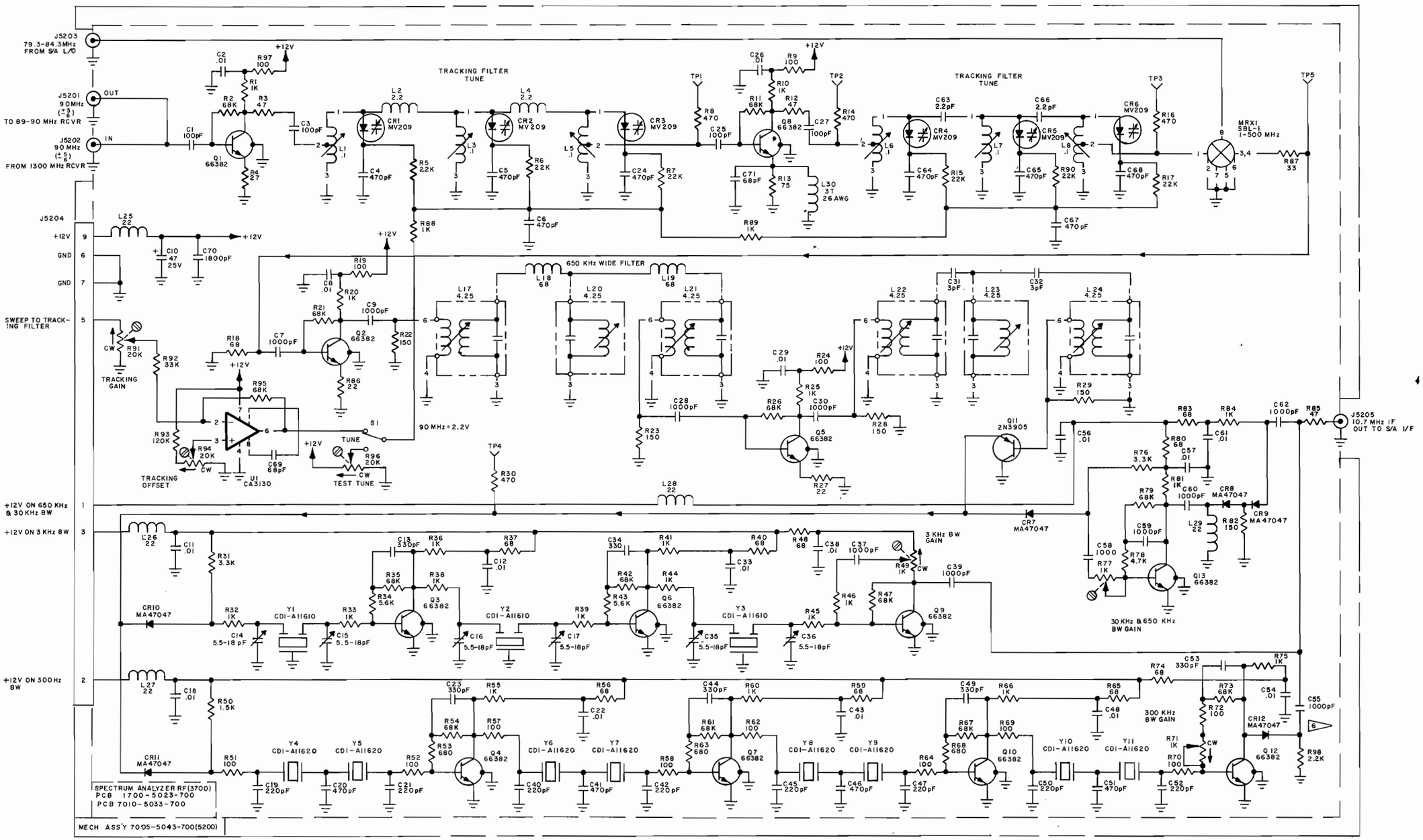
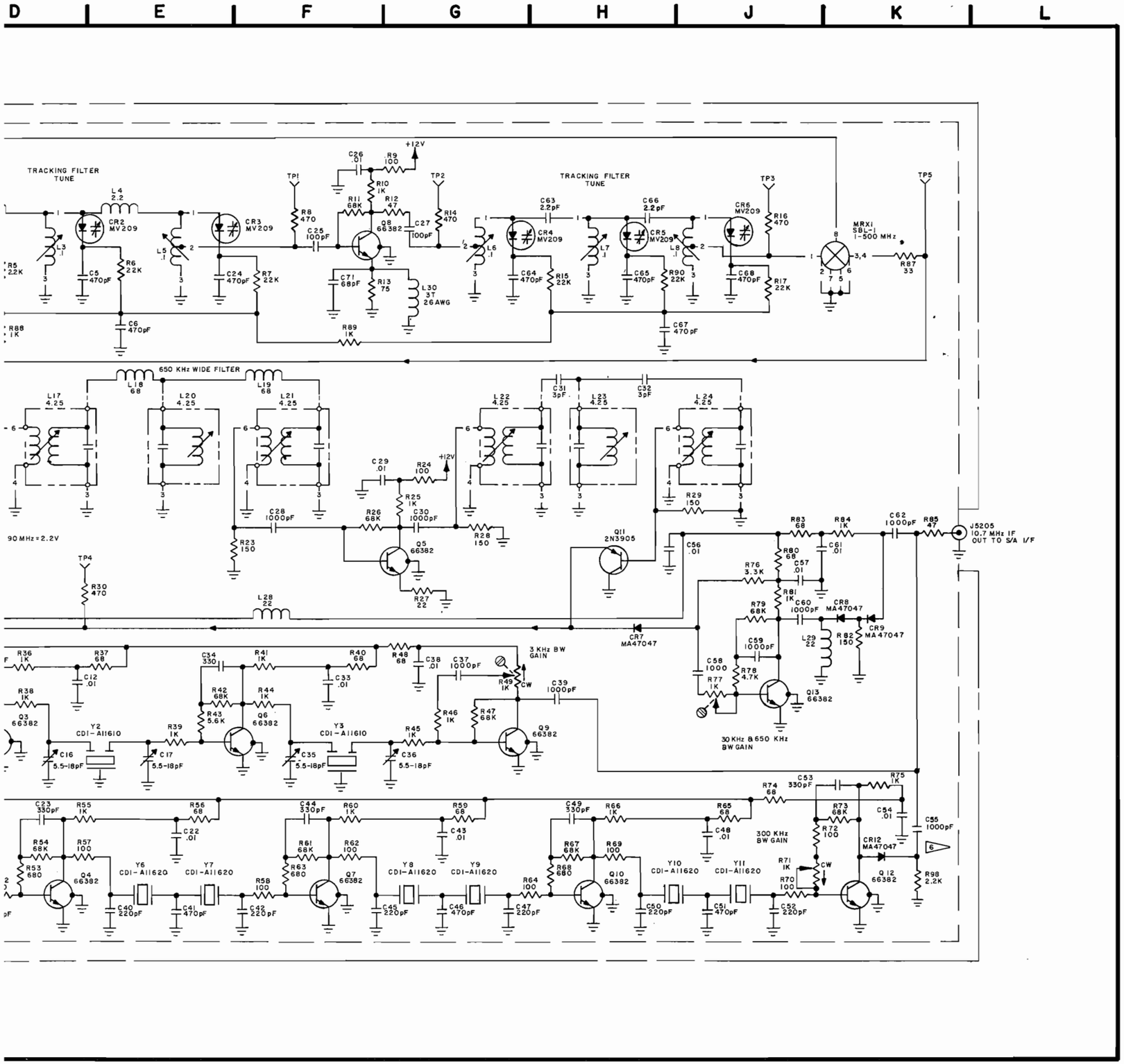


Figure 7-35 Spectrum Analyzer LO Module Schematic (Sheet 4 of 4)
0000-5013-500-F5


J5203
79.3-84.3MHz
FROM S/A L/O
J5201
90MHz
TO 89-90 MHz RCVR
OUT
J5202
90 MHz
FROM 1300 MHz RCVR
IN
TRACKING FILTER TUNE
TRACKING FILTER TUNE
650 KHz WIDE FILTER
J5204
SWEEP TO TRACKING FILTER
TRACKING GAIN
TRACKING OFFSET
TEST TUNE
90 MHz = 2.2V
3 KHz BW GAIN
30 KHz & 650 KHz BW GAIN
300 KHz BW GAIN
MRX1 SBL-1 1-500 MHz
J5205
10.7 MHz IF OUT TO S/A I/F
+12V ON 650 KHz & 30 KHz BW
+12V ON 3 KHz BW
+12V ON 300 Hz BW
SPECTRUM ANALYZER RF(3700)
PCB 1700-5023-700
PCB 7010-5033-700
MECH ASS'Y 7005-5043-700(5200)

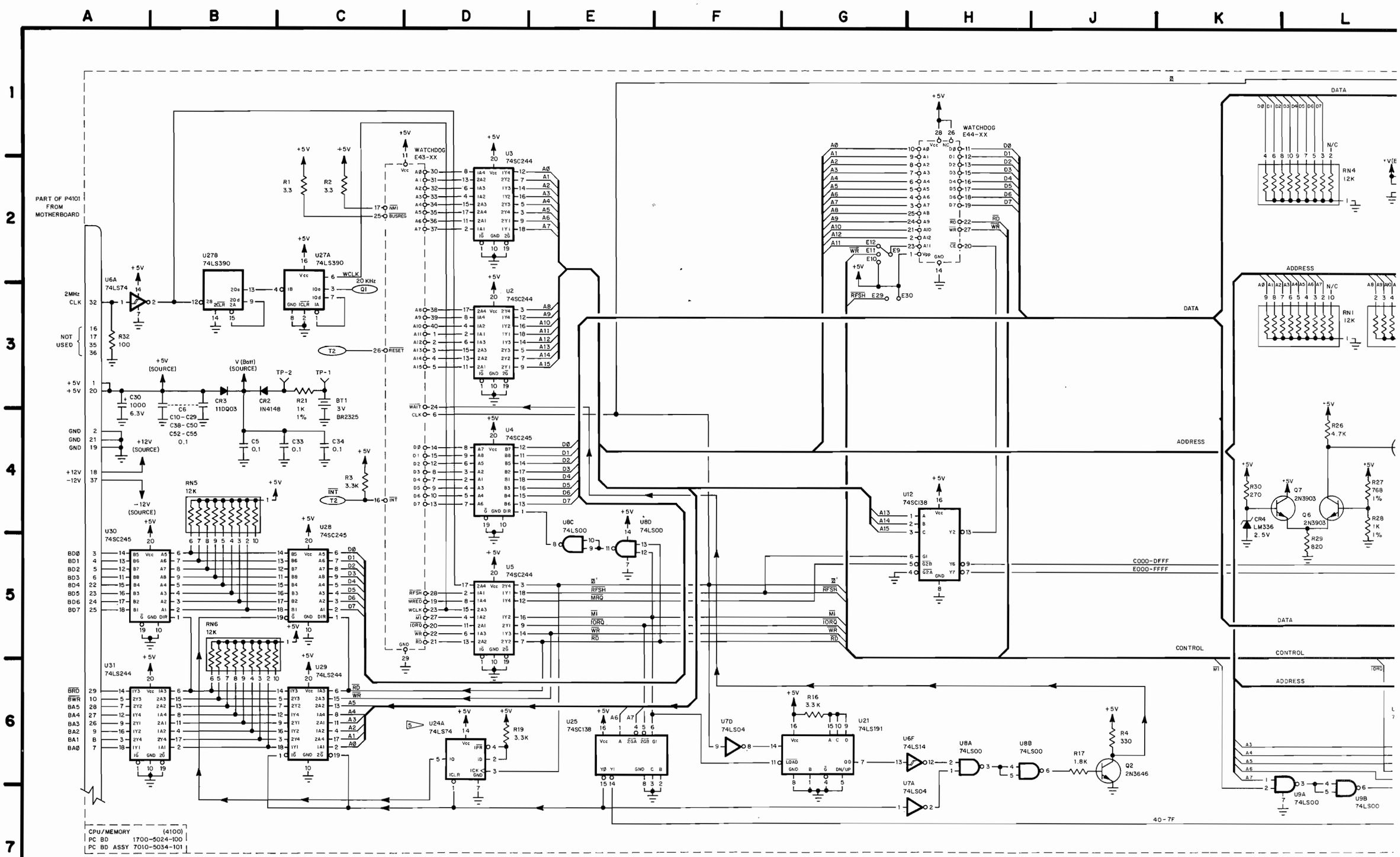


NOTES AND STANDARDS:

(UNLESS OTHERWISE NOTED)

1. ALL REF NOS CARRY AN ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES:
   A. MECH ASSY 7005-5043-700 (5200)
   B. PC BOARD ASSY 7010-5033-700 (3700; E.G., R1 IS R3701)
2. ALL RESISTORS ARE 1/4 W, 5% TOLERANCE.
3. ALL RESISTANCE IS EXPRESSED IN OHMS.
4. ALL CAPACITANCE IS EXPRESSED IN MICROFARADS.
5. ALL INDUCTANCE IS EXPRESSED IN MICROHENRYS.
6. EFFECTIVE SER. NO. 2445 AND ON.

Figure 7-36 Spectrum Analyzer RF Module Schematic 0000-5013-700-D1


PART OF P4101 FROM MOTHERBOARD
2MHz CLK
NOT USED
+5V +5V
GND GND GND
+12V
-12V
+5V (SOURCE)
V (Batt) (SOURCE)
+12V (SOURCE)
-12V (SOURCE)
U6A 74LS74
R32 100
C30 1000 6.3V
C6 C10-C29 C38-C50 C52-C55 0.1
CR3 11DQ03
CR2 IN4148
TP-2
TP-1
R21 1K 1%
BT1 3V BR2325
C5 0.1
C33 0.1
C34 0.1
R1 3.3
R2 3.3
U278 74LS390
U27A 74LS390
WCLK
20 KHz
Q1
T2
RESET
WATCHDOG E43-XX
NMI
BUSREQ
U3 74SC244
U2 74SC244
U4 74SC245
WAIT
CLK
INT
R3 3.3K
RN5 12K
RN6 12K
U30 74SC245
U28 74SC245
U31 74LS244
U29 74LS244
BD0 BD1 BD2 BD3 BD4 BD5 BD6 BD7
BRD BWR BA5 BA4 BA3 BA2 BA1 BA0
U24A 74LS74
R19 3.3K
U8C 74LS00
U8D 74LS00
U5 74SC244
RFSH MREQ WCLK IORQ WR RD
U25 74SC138
U7D 74LS04
R16 3.3 K
U21 74LS191
U6F 74LS14
U7A 74LS04
U8A 74LS00
U8B 74LS00
R17 1.8K
R4 330
Q2 2N3646
WATCHDOG E44-XX
RFSH E29
E30
U12 74SC138
C000-DFFF
E000-FFFF
DATA
ADDRESS
CONTROL
RN4 12K
RN1 12K
R26 4.7K
R30 270
Q7 2N3903
Q6 2N3903
CR4 LM336 2.5V
R29 820
R27 768 1%
R28 1K 1%
U9A 74LS00
U9B 74LS00
40-7F
CPU/MEMORY (4100)
PC BD 1700-5024-100
PC BD ASSY 7010-5034-101

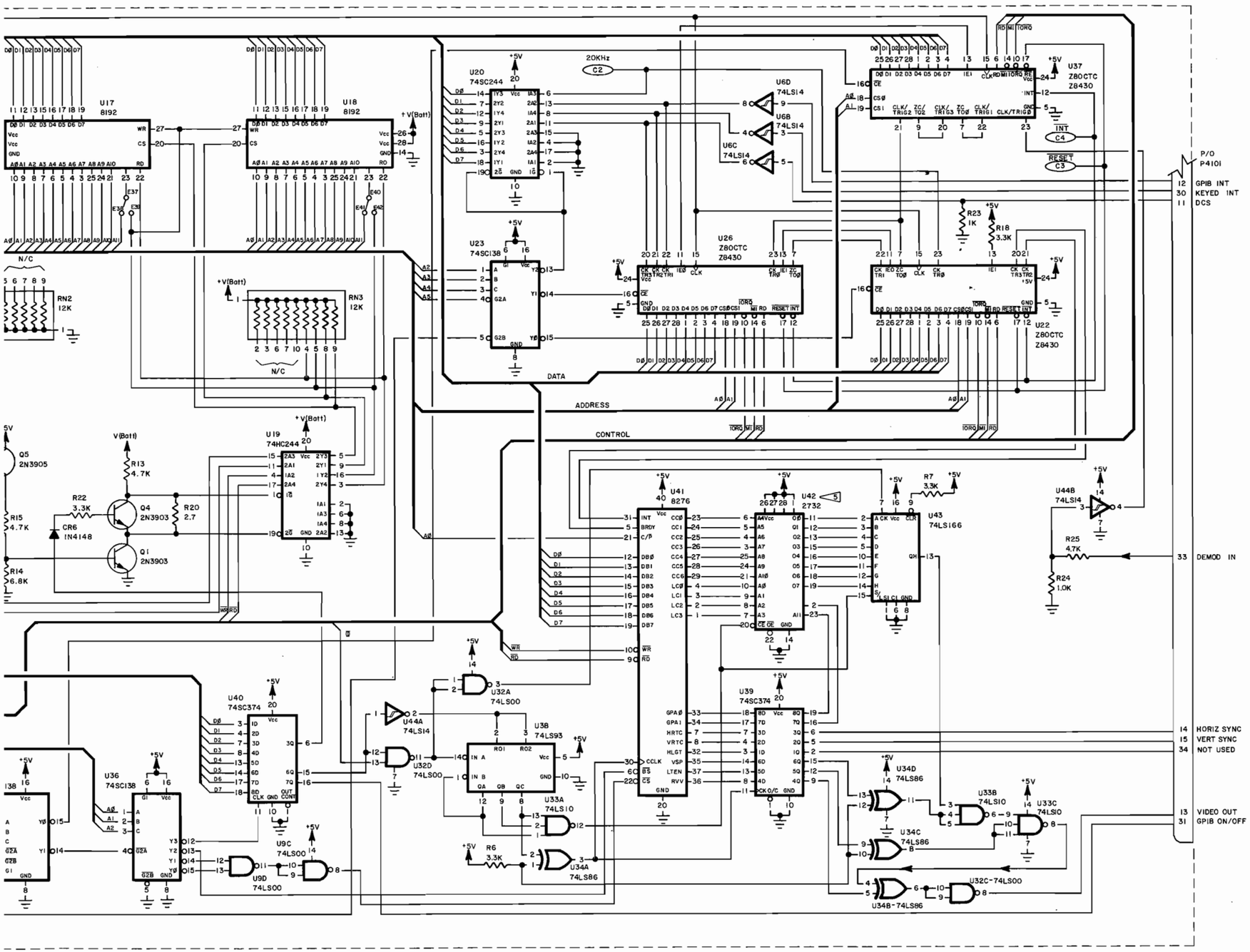
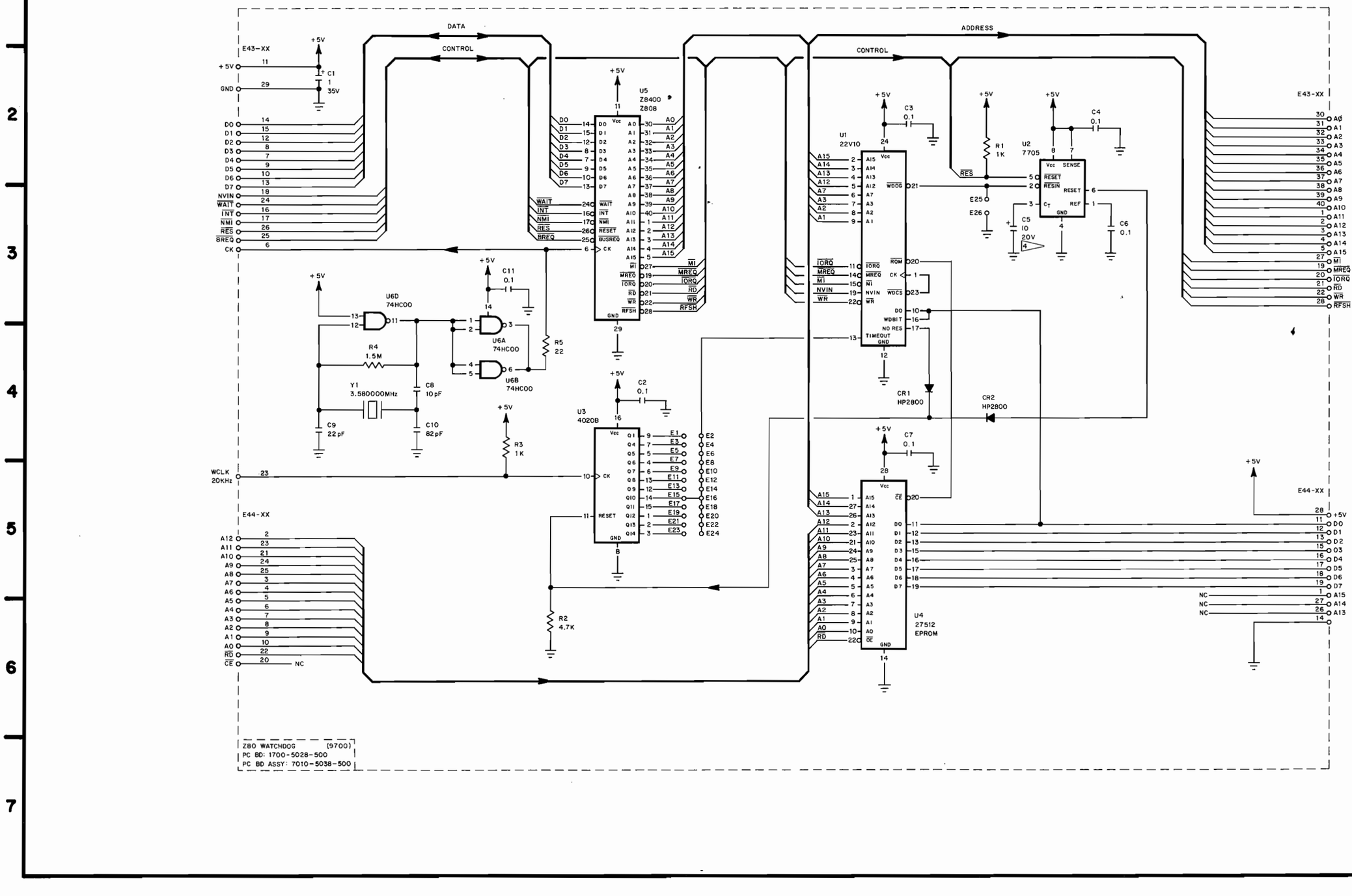


Figure 7-37 CPU/Memory PC Board Schematic (Sheet 1 of 3)
0000-5014-101-C5

SER. NO. 2061 AND ON


DATA
CONTROL
ADDRESS
CONTROL
E43-XX
+5V
C1
1
35V
U5
Z8400
Z808
U1
22V10
U2
7705
R1
1K
C3
0.1
C4
0.1
C5
10
20V
C6
0.1
E25
E26
RES
U6D
74HC00
U6A
74HC00
U6B
74HC00
R4
1.5M
R5
22
C8
10pF
C9
22pF
C10
82pF
Y1
3.580000MHz
C11
0.1
C2
0.1
U3
4020B
R3
1K
R2
4.7K
WCLK
20KHz
E44-XX
CR1
HP2800
CR2
HP2800
C7
0.1
U4
27512
EPROM
NC
Z80 WATCHDOG (9700)
PC BD: 1700-5028-500
PC BD ASSY: 7010-5038-500

STANDARDS
(UNLESS OTHERWISE NOTED):

1. ALL REF. NOS. CARRY AN ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC SERIES 4100 (E.G., R1 IS R4101).

2. ALL RESISTORS ARE 1/4 W, ±5%.

3. ALL RESISTANCE IS EXPRESSED IN OHMS.

4. ALL CAPACITANCE IS EXPRESSED IN MICROFARADS.

5. ALL INDUCTANCE IS EXPRESSED IN MICROHENRYS.

NOTES
(ALL SCHEMATICS):

1. A. REF DES SERIES FOR CPU/MEMORY PC BD ASSY IS 4100 (E.G., R1 IS R4101).
   B. REF DES SERIES FOR Z80 WATCH DOG CIRCUIT IS 9800 (E.G., R1 IS R9801).

2. DATA PART NO. IS 7010-5034-101.

3. DATA PART NO. FOR Z80 WATCHDOG PC BD ASSY IS 7010-5038-500.

4. ON Z80 WATCHDOG CIRCUIT, U4 IS ADDED AT A HIGHER ASSEMBLY LEVEL. IT IS SHOWN FOR REFERENCE ONLY.

NOTES:
SER. NO. 1436 THRU 2060

1. THIS SCHEMATIC COVERS PC BD VERSIONS FOR GPIB/STD (7010-5034-102) AND CELLULAR UNITS (7010-5034-102) EFFECTIVE SER. NOS. 1436 THRU 2060.

2. LAST REF NOS. USED.
   PCB ASSY 7010-5034-101 (GPIB/STD):
   P1, BT1, TP2, C56, R32, Q7, RN6, CR6, U44.
   PCB ASSY 7010-5034-102 (CELLULAR):
   P1, BT1, TP2, C56, R32, CR6, Q7, RN6, U44.

3. REF NOS. NOT USED.
   PCB ASSY 7010-5034-101 (GPIB/STD):
   C1 - C4, C7 - C9, C31, C32, C35 - C37, C51, C56, CR1, CR5, Q3, R5, R8 -R12, CR1, CR5, Q3, R5, R8 - R12, R31, U1, U10, U11, U134 - U16.
   PCB ASSY 7010-5034-102 (CELLULAR):
   C1 - C4, C7 - C9, C31, C32, C35 - C37, C51, C56, CR1, CR5, Q3, R5, R8 - R12, R31, U1, U10, U11, U13, U14.

4. JUMPER CONFIGURATION SHOWN IS FOR GPIB/STD (7010-534-101). CELLULAR JUMPER CONFIGURATION IS SHOWN IN DETAIL A.

DETAIL A

5. U24 AND U42 ARE 24-PIN IC'S IN A 28-PIN SOCKET. PIN NUMBERS SHOWN ARE RELATIVE TO THE SOCKET, NOT A 24-PIN IC (I.E., PIN 3 IS PIN 1 OF THE 24-PIN IC).

6. U15 AND U16 ARE INSTALLED ON CELLULAR CONFIGURATION ONLY (7010-5034-102). SOCKETS ARE X1 AND X2 ON GPIB/STD CONFIGURATIONS (7010-5034-101).

7. EFFECTIVE THROUGH SER. NO. 2001: C54, C55, C56, R31 AND R32 NOT USED. R1 AND R2 WERE 3.3K.

8. EFFECTIVE THROUGH SER. NO. 1730: U17 AND U18 ARE 24-PIN IC'S INSTALLED IN 28-PIN SOCKETS. PIN NUMBERS SHOWN ARE RELATIVE TO THE SOCKET, NOT THE 24-PIN IC (I.E., PIN 3 IS PIN 1 OF THE 24-PIN IC).

9. EFFECTIVE THROUGH SER. NO. 1967, C31, C32 AND C53 WERE NOT USED.

EFFECTIVE SER. NO. 2061 AND ON

NOTES:

1. THIS SCHEMATIC COVERS PC BD VERSIONS FOR GPIB/STD (7010-5034-101) AND CELLULAR UNITS (7010-5034-102) EFFECTIVE SER. NO. 2061 AND ON.

2. LAST REF. DES. NOS. USED (PCB ASSY'S 7010-5034-101 AND 7010-5034-102): BT1, C56, CR6, P1, Q7, R32, RN6, TP2, U44.

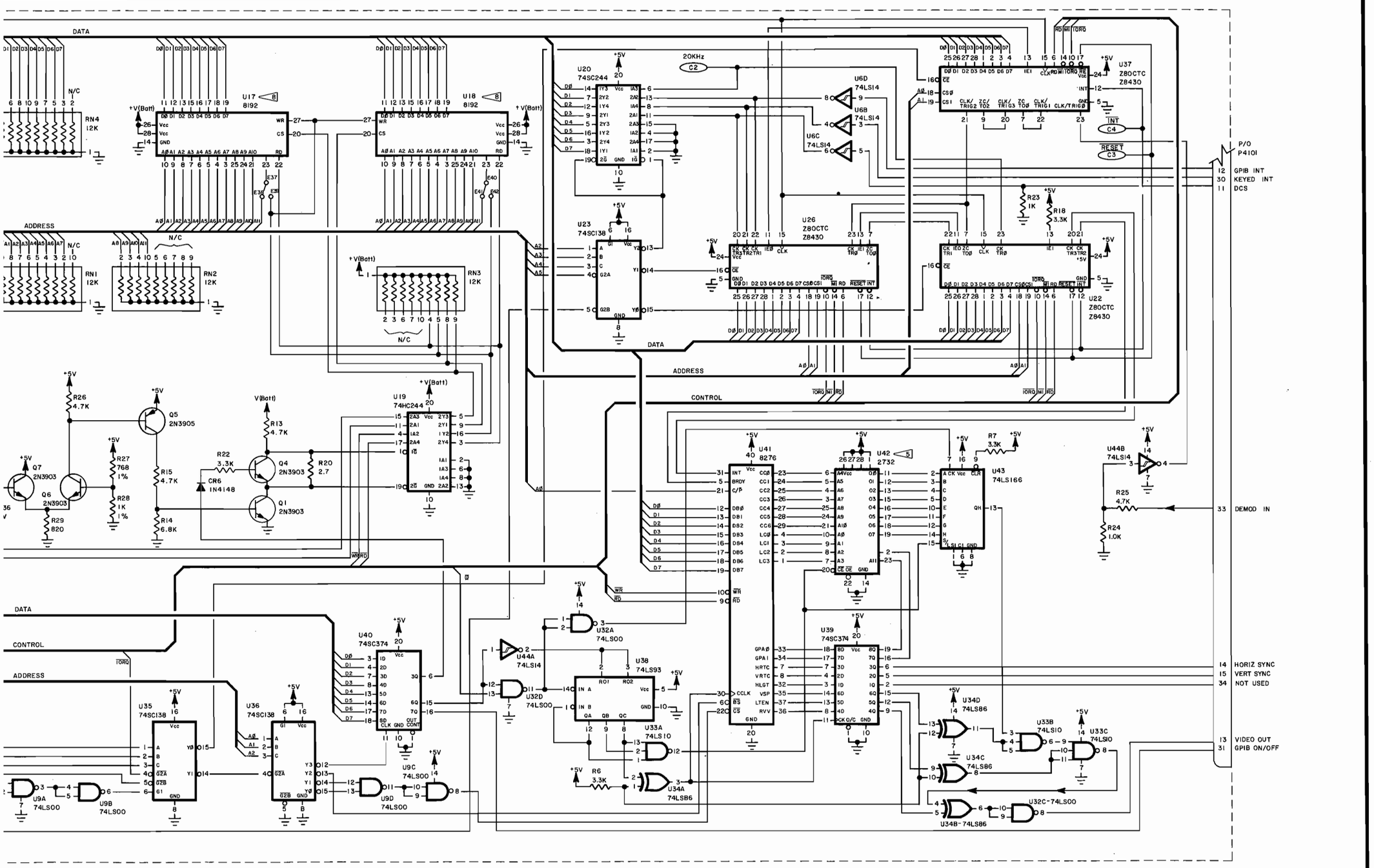
3. REF. NOS. NOT USED (PCB ASSY'S 7010-5034-101 AND 7010-5034-102): C1 - C4, C7 - C9, C31, C32, C35 - C37, C51, C56, CR1, CR5, Q3, R5, R8 - R12, R31, U1, U10, U11, U13 - U16.

4. JUMPER CONFIGURATION SHOWN IS FOR GPIB/STD UNIT (7010-5034-101). CELLULAR JUMPER CONFIGURATION (7010-5034-102) IS SHOWN IN DETAIL A.

5. U24 AND U42 ARE 24-PIN IC's INSTALLED IN 28-PIN SOCKETS. PIN NUMBERS ARE SHOWN RELATIVE TO SOCKET, NOT 24-PIN IC (I.E., PIN 3 IS PIN 1 OF 24-PIN IC).

Figure 7-37 CPU/Memory PC Board Schematic (Sheet 2 of 3) 0000-5014-101-C5

CPU/MEMORY (4100)
PC BD 1700-5024-100
PC BD ASSY 7010-5034-101 (GPIB/STD)
PC BD ASSY 7010-5034-102 (CELLULAR)



SER. NO. 1436 THRU 2060

Figure 7-37 CPU/Memory PC Board Schematic (Sheet 3 of 3) 0000-5014-101-C5

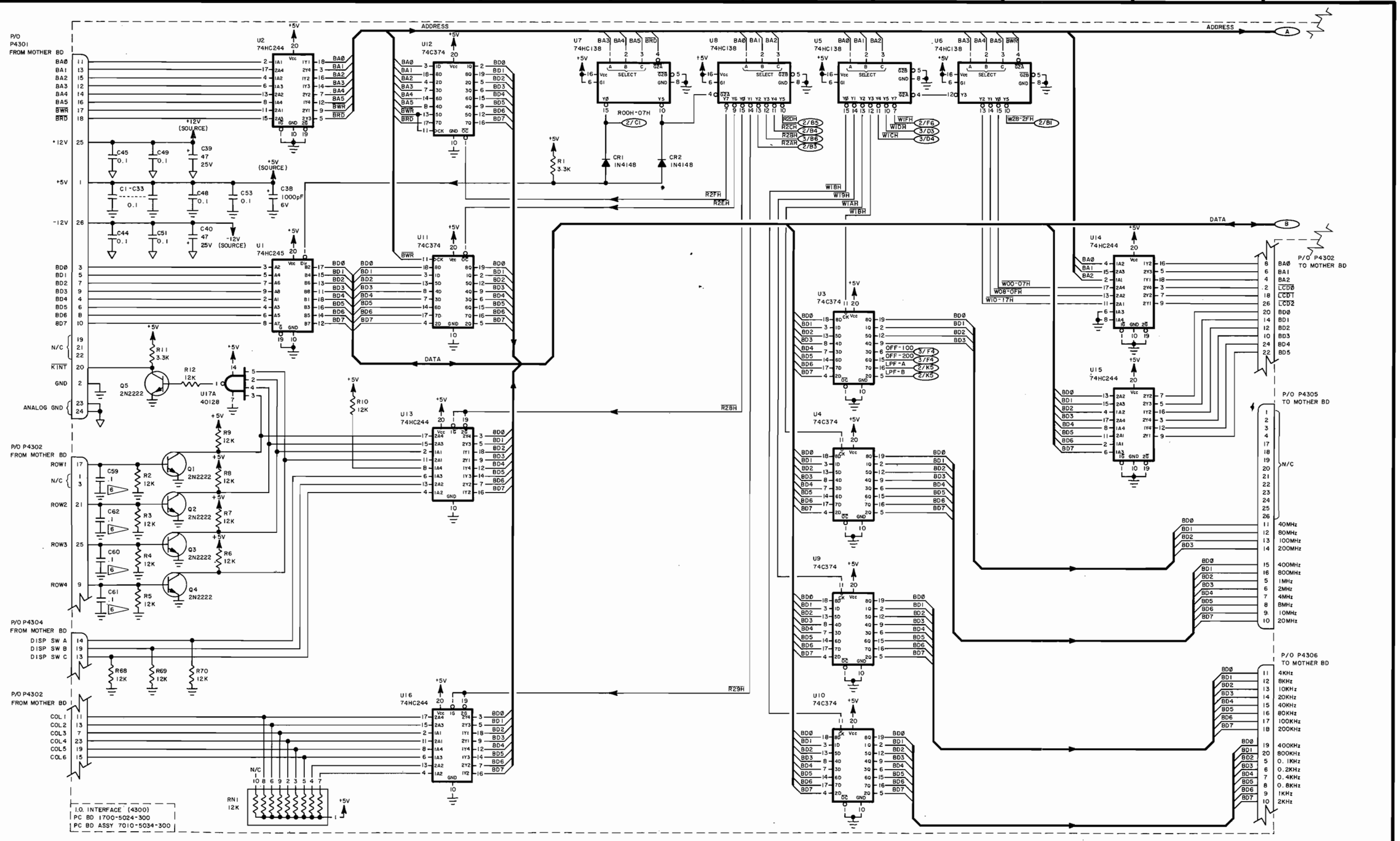


Figure 7-38 I/O Interface PC Board Schematic (Sheet 1 of 3) 0000-5014-300-C6

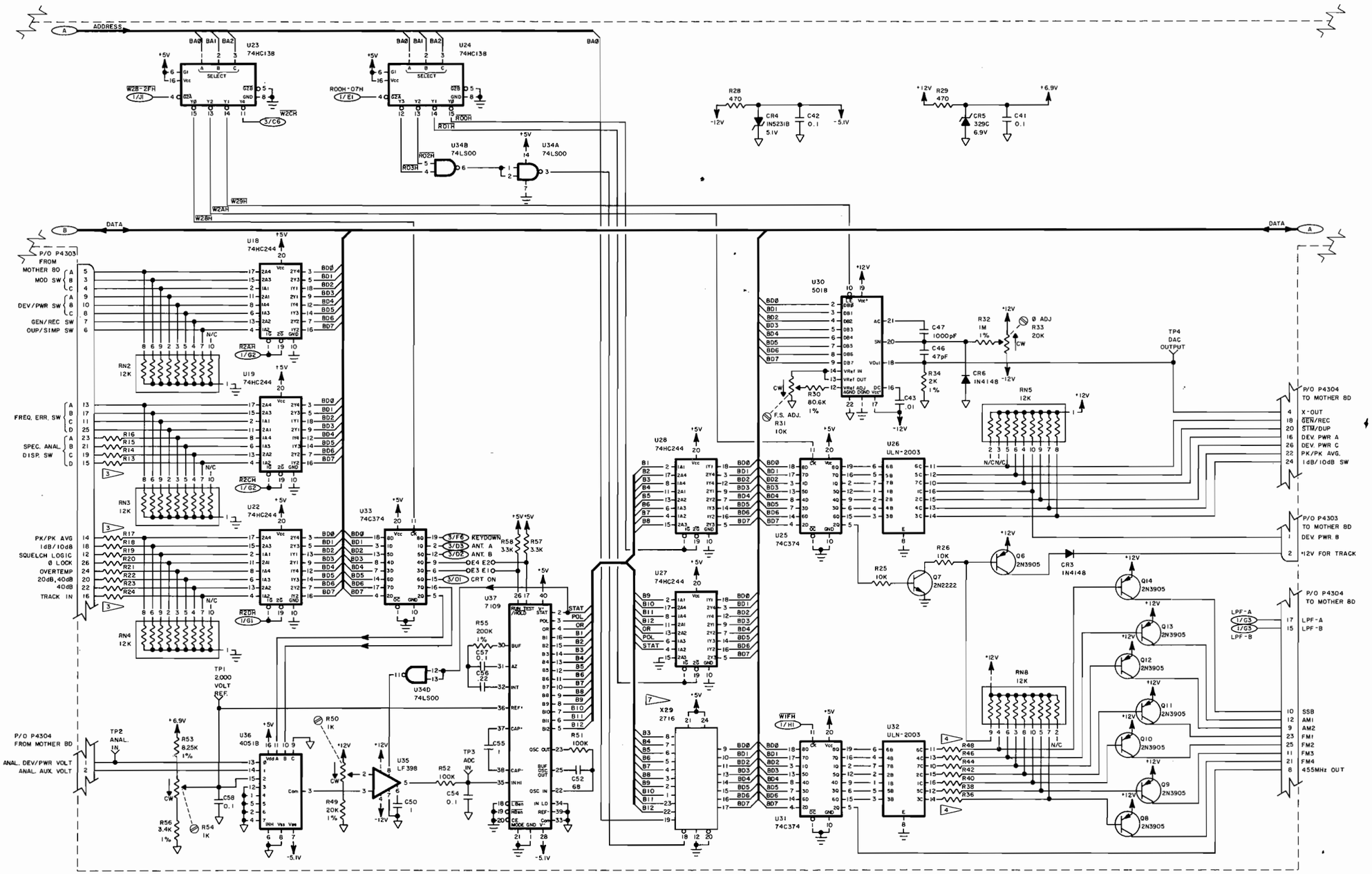
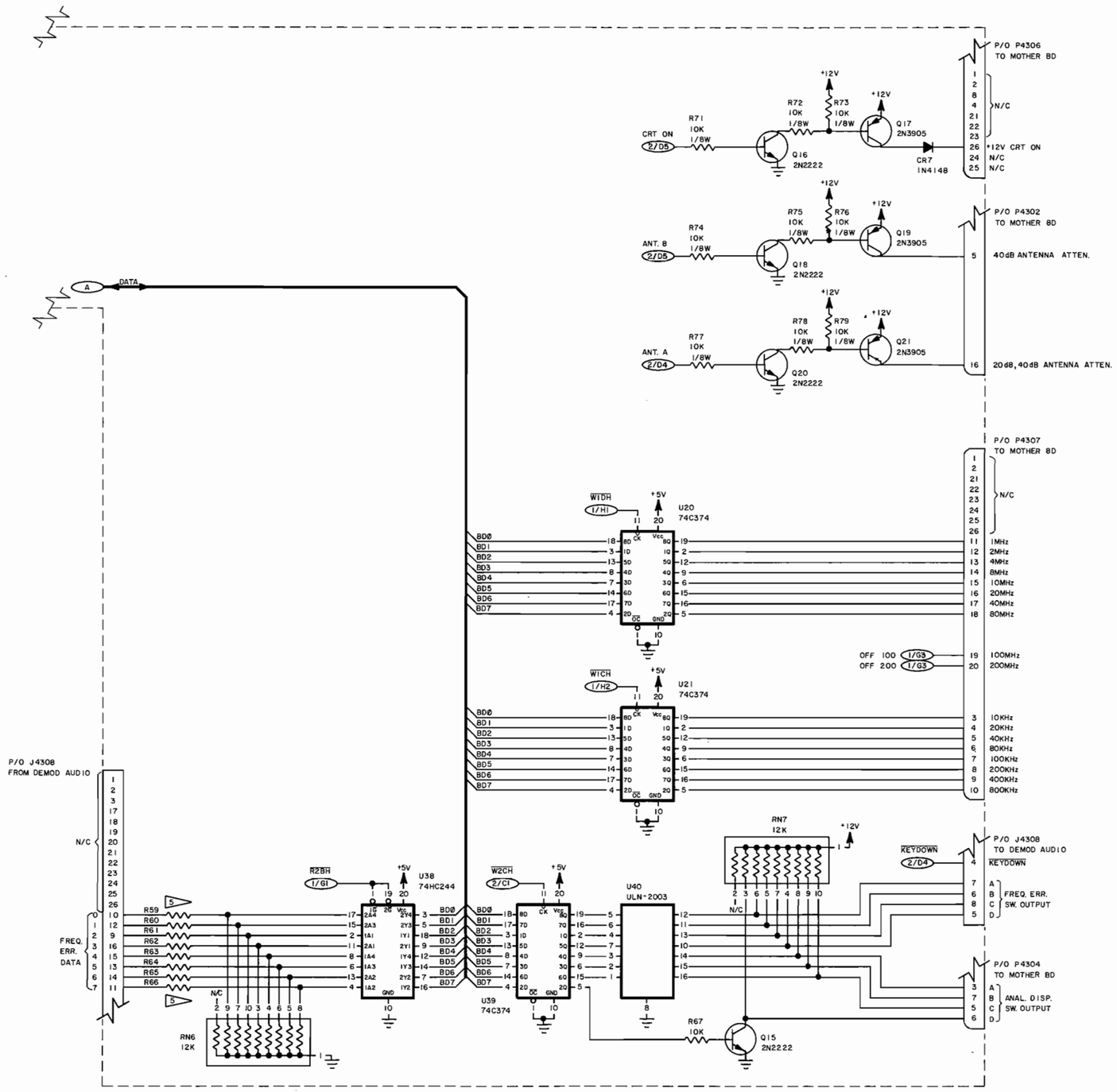


Figure 7-38 I/O Interface PC Board Schematic (Sheet 2 of 3) 0000-5014-300-C6



STANDARDS:

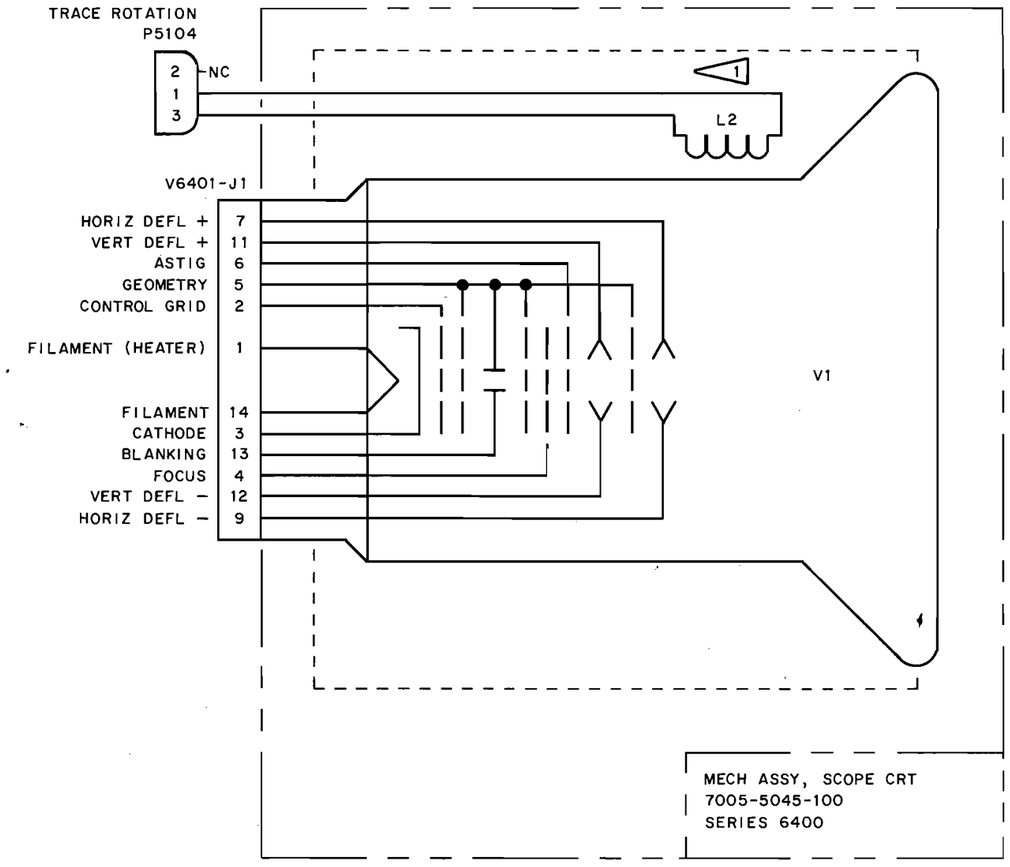
(UNLESS OTHERWISE NOTED)

1. ALL REF NOS CARRY AN ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES 4300 (E.G., R1 IS R4301).
2. ALL RESISTORS ARE 1/4 W, 5% TOLERANCE.
3. ALL RESISTANCE IS EXPRESSED IN OHMS.
4. ALL CAPACITANCE IS EXPRESSED IN MICROFARADS.
5. ALL INDUCTANCE IS EXPRESSED IN MICROHENRYS.

NOTES:

1. LAST REF NOS USED: TP4, PR307, J4308, C58, Q21, CR7, U40, R79, RN8.
2. REF NOS NOT USED: C34-C37, R27, R35, R37, R39, R41, R43, R45, R47.
3. R13-R24 ARE 15K, 1/8 W, 5% RESISTORS.
4. R36, R38, R40, R42, R44, R46, R48 ARE 10K, 1/8 W, 5% resistors.
5. R59-R66 ARE 15K, 1/8 W, 5% RESISTORS.
6. SER. NO. 2002 AND ON USE C59 THRU C62.
7. SER. NO. 2621 AND ON, X29 IS REMOVED.

Figure 7-38 I/O Interface PC Board Schematic (Sheet 3 of 3) 0000-5014-300-C6



STANDARDS:

1. ALL REF NOS CARRY AN ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES: 6400 (E.G., V1 IS V6401, ETC.)

NOTES:

1. L2 IS 850 TURNS OF #36 AWG INSULATED WIRE.

Figure 7-39 Scope CRT Schematic 0000-5015-200

SECTION 8 - GPIB INTERFACE (OPTION 01)

8-1 INTRODUCTION

The GPIB Interface option provides a means to partially control the FM/AM-1500 with an external controller. Hardware changes in the FM/AM-1500 to accommodate the GPIB option are shown in Figure 8-1. The LCD Display Assy and the RF Attenuator Driver Assy take the place of the manual attenuator (RF Output Level Control) on the standard FM/AM-1500. The GPIB Interface Module Assy (which contains the Attenuator Control and Display PC Board, the GPIB Analyzer Digitizer PC Board and the GPIB Interface PC Board) provides the means for remote communication between an external controller and the FM/AM-1500. This option also provides the capability for a hard copy record of the analyzer trace.

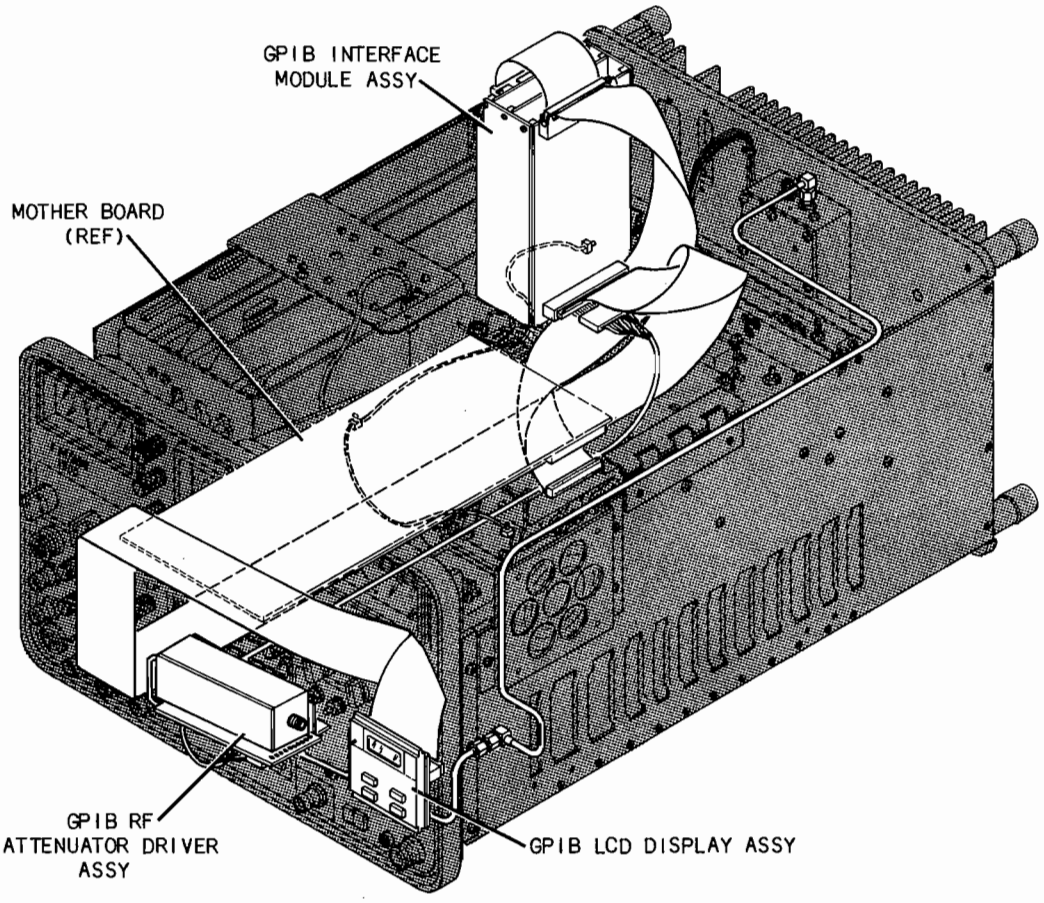


Figure 8-1 GPIB Option Installation

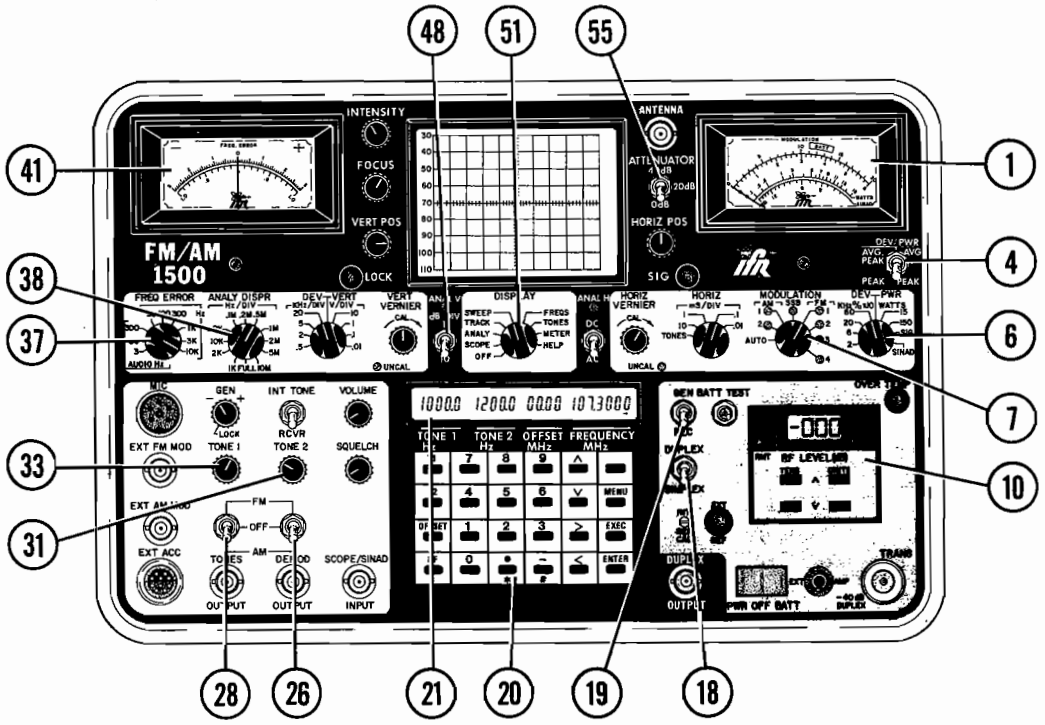
8-1-1 FRONT PANEL CONTROLS CONTROLLED BY GPIB

The front panel controls listed in Figure 8-2 are controlled by the GPIB and thus may be in any position at initial set-up, with the exception of the DISPLAY Control (51). The DISPLAY Control must be in "ANALY" whenever GPIB control is selected. This position allows "ANALY", "TRACK", "FREQS", "TONES" and "METER" functions to be controlled by the GPIB.

NOTE

"OFF", "SCOPE", "SWEEP" and "HELP" positions of the DISPLAY Control must be manually selected.

Ref. Nos. correspond to Figure 3-1 in Section 3.



1. MODULATION Meter
4. AVG PEAK/PEAK Switch
6. DEV/PWR Control
7. MODULATION Control
10. RF Output Level Control
18. DUPLEX/SIMPLEX Switch
19. GEN/REC Switch
20. KEYBOARD
21. LCD
26. Tone 2 FM/OFF/AM Switch
28. Tone 1 FM/OFF/AM Switch
31. TONE 2 Control
33. TONE 1 Control
37. FREQ ERROR Control
38. ANALY DISPR Control
41. FREQ ERROR Meter
48. dB/DIV Switch
51. DISPLAY Control (see text)
55. ATTENUATOR Switch

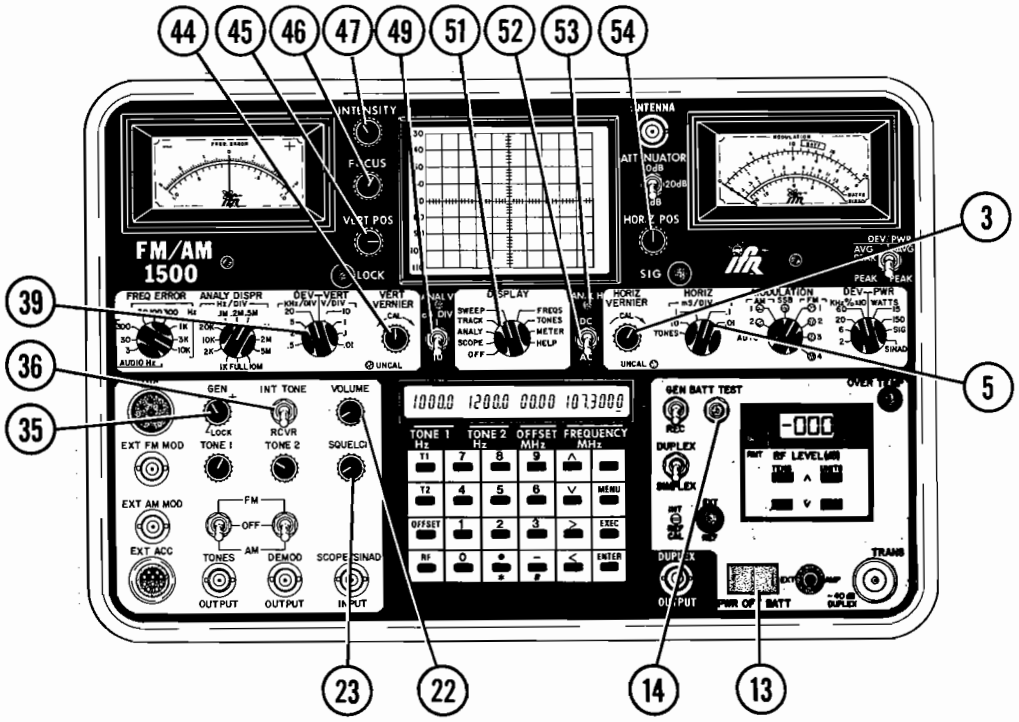
Figure 8-2 FM/AM-1500 Controls Controlled by GPIB

8-1-2 FRONT PANEL CONTROLS NOT CONTROLLED BY GPIB

The front panel controls listed in Figure 8-3 are not controllable by the GPIB and therefore must be controlled manually by the technician, with the exception of the DISPLAY Control (51). The DISPLAY Control is manually selected for "OFF", "SCOPE" and "HELP" positions, but must be in "ANALY" for GPIB control, as noted in Paragraph 8-1-1.

NOTE

Ref. Nos. correspond to Figure 3-1 in Section 3.



3. HORIZ VERNIER Control
5. HORIZ Control
13. PWR/OFF/BATT Switch
14. BATT TEST Button
22. VOLUME Control
23. SQUELCH Control
35. GEN/LOCK Control
36. INT TONE/RCVR Switch
39. DEV/VERT Control
44. VERT VERNIER Control
45. VERT POS Control
46. FOCUS Control
47. INTENSITY Control
49. Vertical Centering Adjustment (Analyzer)
51. DISPLAY Control (see text)
52. DC/AC Switch
53. Horizontal Centering Adjustment (Analyzer)
54. HORIZ POS Control

Figure 8-3 FM/AM-1500 Controls NOT Controlled by GPIB

8-1-3 REAR PANEL GPIB CONNECTIONS AND SWITCHES

1. GPIB Connector

   The GPIB Connector (J5902), on the Rear Panel of the FM/AM-1500, conforms to IEEE Standard 488-1978 configuration as shown in Figure 8-4.

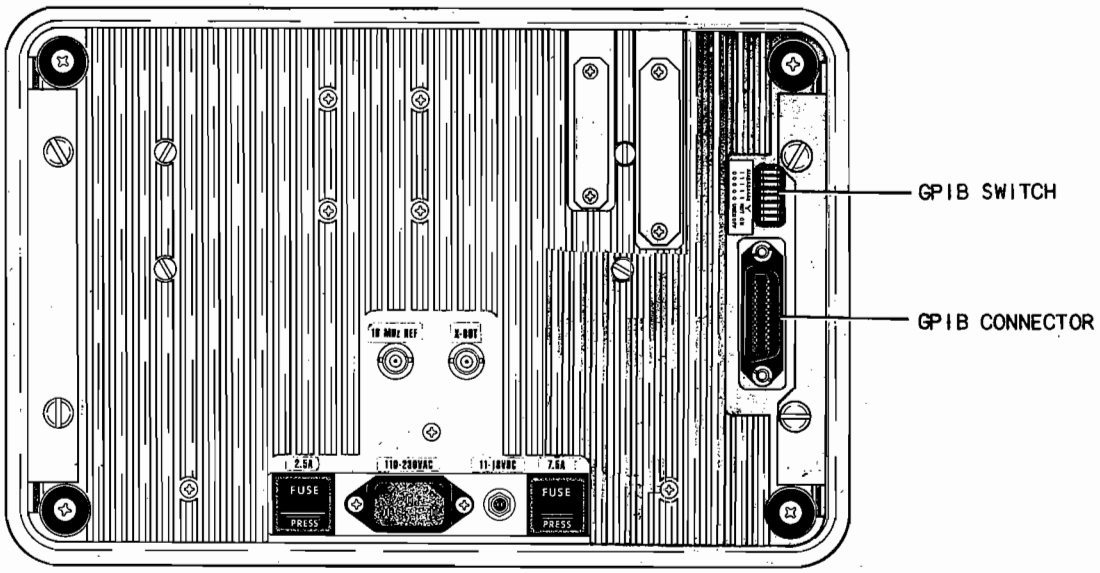
2. GPIB Switch

   The GPIB Switch (SW5901), on the Rear Panel of the FM/AM-1500, must be set in the desired configuration prior to powering up the FM/AM-1500. This is necessary because once the microprocessor in the FM/AM-1500 is initialized, it cannot read a change of a switch setting change on the GPIB Switch until it is powered down and subsequently powered back up.

   Dip switches A1 thru A5 are used for the user-selected address of the FM/AM-1500. The DIP switches are binary coded, with A1 being the least significant digit. For example, if the desired address of the FM/AM-1500 is 9, configure switches A1 thru A5 as follows:

   A1 = ON = 1
   A2 = OFF = Ø
   A3 = OFF = Ø
   A4 = ON = 8
   A5 = OFF = Ø

   DIP Switch A8 on the GPIB Switch is the ENABLE/DISABLE Switch for the GPIB operation. When A8 is ON, the GPIB control is operable. When A8 is OFF, the GPIB control is not operable.



GPIB Switch (SW5901)

A1	User-Selected Address
A2	User-Selected Address
A3	User-Selected Address
A4	User-Selected Address
A5	User-Selected Address
A6	Not Used
A7	Not Used
A8	ENABLE/DISABLE GPIB

GPIB Connector (J5902)

1.	DIO 1	13.	DIO 5
2.	DIO 2	14.	DIO 6
3.	DIO 3	15.	DIO 7
4.	DIO 4	16.	DIO 8
5.	EOI	17.	REN
6.	DAV	18.	GND
7.	NFRD	19.	GND
8.	NDAC	20.	GND
9.	IFC	21.	GND
10.	SRQ	22.	GND
11.	ATN	23.	GND
12.	GND	24.	GND

Figure 8-4 Rear Panel Connectors and Switches for GPIB

8-2 THEORY OF OPERATION

8-2-1 Attenuator Control & Display PC Board Detailed Theory of Operation

General

The Attenuator Control & Display PC Board allows the microprocessor to read the states of the units up, units down, tens up and tens down switches on the front panel LCD Display, as well as to control the programmable attenuator, attenuator LCD and the Remote LED (See Figure 8-5 and GPIB Interface Module Schematic).

Bi-Directional/Uni-Directional Buffer

U8201 is an 8-bit, bi-directional, tri-state buffer which transfers data between the microprocessor bus and the peripheral bus. U8201 is continuously enabled and normally kept in the send mode (microprocessor bus to peripheral bus). When the 8-bit buffer is selected by the address decoder, the bi-directional buffer is placed in the receive mode. U8202 is a single direction buffer which buffers address and control information from the microprocessor bus to the peripheral bus.

Address Decoder

U8204, U8205 and U8206 form the address decoder. The address decoder selects the 8 bit buffer, 8 bit latch or the LCD decoder/driver when the appropriate address and control signals are present on the bus.

8-Bit Buffer

U8203 is the 8-bit buffer. When U8203 is selected by the address decoder, U8203 will gate 4 bits from the units up, units down, tens up and tens down switches. The four most significant bits are tied low.

8-Bit Latch

The 8-bit latch, U8207, captures the programmable attenuator setting and the state of the Remote LED from the peripheral bus when directed to do so by the address decoder. The 7 attenuator-setting bits are applied to the 7-bit driver, and the remote bit is applied to the Remote LED.

7-Bit Driver

The 7-bit driver, U8208, is a transistor array configured as an open-collector, inverting buffer. The output of the 7-bit driver is applied to the programmable attenuator.

LCD Decoder/Driver

The LCD Decoder/Driver, U8209, contains four 4-bit latches, four BCD to decimal decoders and four LCD drivers. Each of the BCD digits is

loaded into its appropriate 4-bit latch. The decoding circuitry associated with a 4-bit latch converts the BCD number to a 7-segment code, which determines which segments will be illuminated. The LCD driver produces the square waves which drive the LCD segments and backplane. An LCD segment is off when the square wave on the applicable segment line is in phase with the square wave on the backplane line. An LCD segment is on when the square wave on the applicable segment line is 180° out of phase with the backplane line. There are 28 segment lines out of U8209. Each line corresponds to one of 7 segments in one of the 4 digits on the programmable attenuator LCD.

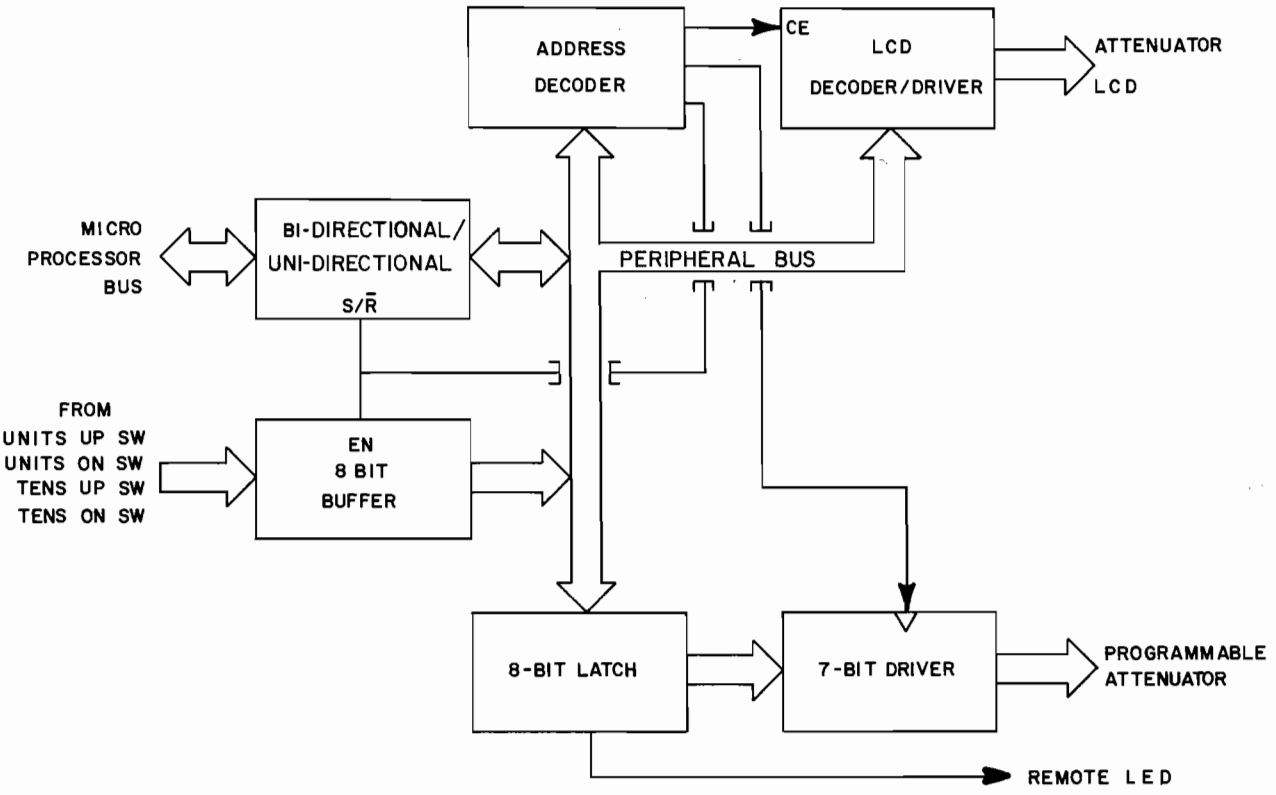


Figure 8-5 Attenuator Control & Display PC Board Detailed Block Diagram

8-2-2 GPIB Interface PC Board Detailed Theory of Operation (Refer to

General

The GPIB Interface PC Board allows the microprocessor in the FM/AM-1500 to communicate over an IEEE-488 bus as a talker or as a listener. The FM/AM-1500 does not operate as a controller (See Figure 8-6 and GPIB Interface Module Schematic).

Power Switch

Q7901 and K7901 form the power switch. When pin 22 of J5901 goes high, Q7901 will turn on and energize relay K7901. K7901, when energized, supplies +5 V to the GPIB Interface. When Q7901 is conducting, the address buffer and the bi-directional buffer are enabled. When Q7901 is off, a high is applied to the enable lines of the address buffer and the data buffer to disable these buffers.

Address Buffer

The address buffer consists of U7902. U7902 is an 8-bit tri-state buffer which supplies address and control information to the address decoder and to the GPIB talker/listener.

Bi-Directional Buffer

U7901 is the bi-directional buffer. It gates data to and from the microprocessor bus and the peripheral bus. U7901 is in the send mode unless the 8-bit address DIP switches (SW7901) or one of the optional addresses are selected.

Address Decoder

The address decoder consists of U7904, U7905 and U7906. It selects the specific device whose address is present on the address bus. It may select the 8-bit buffer (address DIP switches), or the GPIB talker/listener, as well as two other devices which may be connected to J5904.

8-Bit Address DIP Switches

The 8-bit address DIP switches, SW7901, are used to select the IEEE-488 address of the FM/AM-1500. When a switch is closed (ON), a logic low is present on the output. When a switch is open (OFF), a logic high is present on the output.

8-Bit Buffer

U7903 is the 8-bit buffer. It gates the address DIP switch settings to the peripheral bus when directed to do so by the address decoder.

GPIB Talker/Listener

U7908 is the GPIB talker/listener. This IC controls the IEEE-488 bus. All timing, control and protocol for the GPIB is automatically encoded or decoded by this IC. It also provides the line drivers/receivers with a direction signal which determines the direction of the driver/receiver. For additional information concerning U7908, see Intel's data sheet for the 8291A or consult the Intel component data book.

Line Drivers/Receivers

U7909, U7910, U7911 and U7912 are the line drivers/receivers for the IEEE-488 bus. These IC's are bi-directional, open-collector buffers with Schmitt trigger inputs. These IC's provide hysteresis to improve noise immunity when in the receive mode and to provide enough drive to support 15 connecting devices in the output mode.

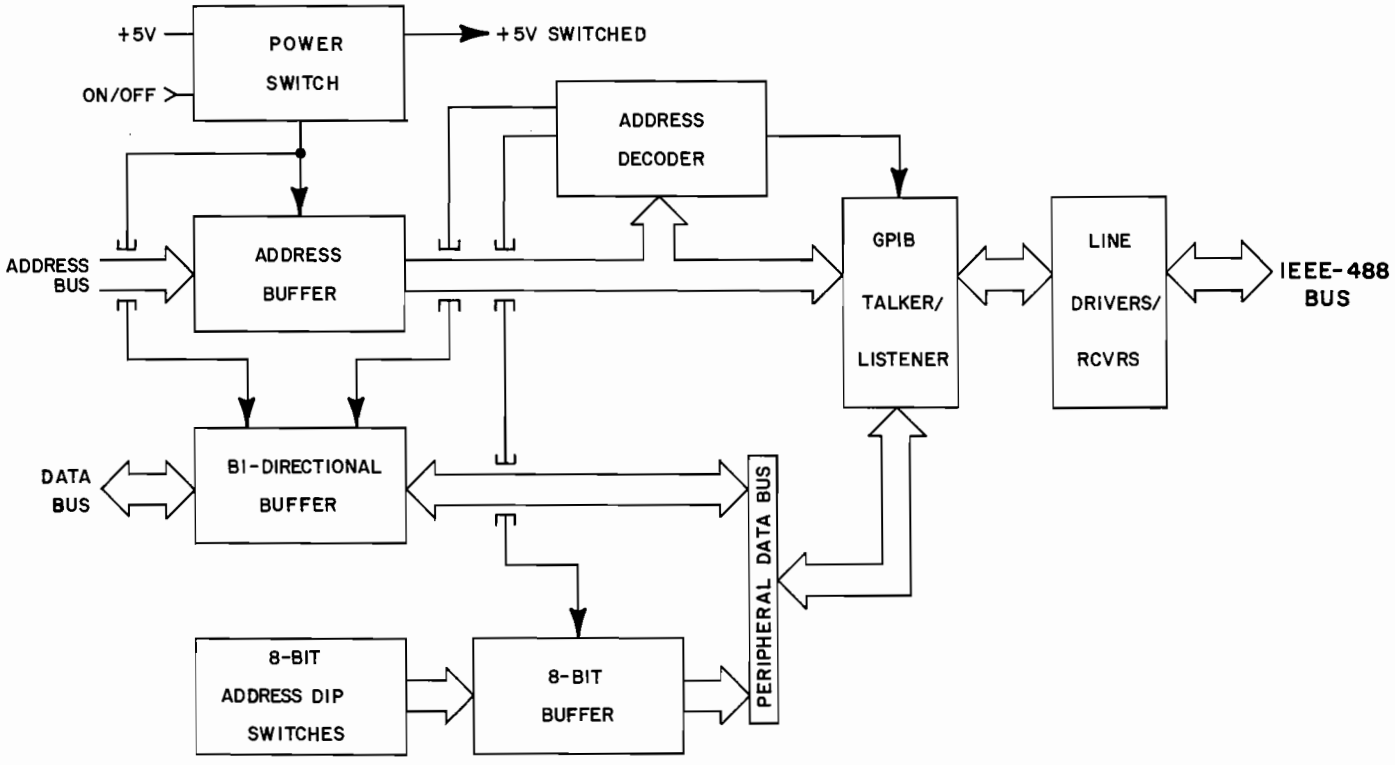


Figure 8-6 GPIB Interface PC Board Detailed Block Diagram

8-2-3 GPIB ANALYZER DIGITIZER PC BOARD DETAILED THEORY OF OPERATION

General

The GPIB Analyzer Digitizer provides the capability for a hard record copy of the analyzer trace (See Figure 8-7 and GPIB Interface Module Schematic).

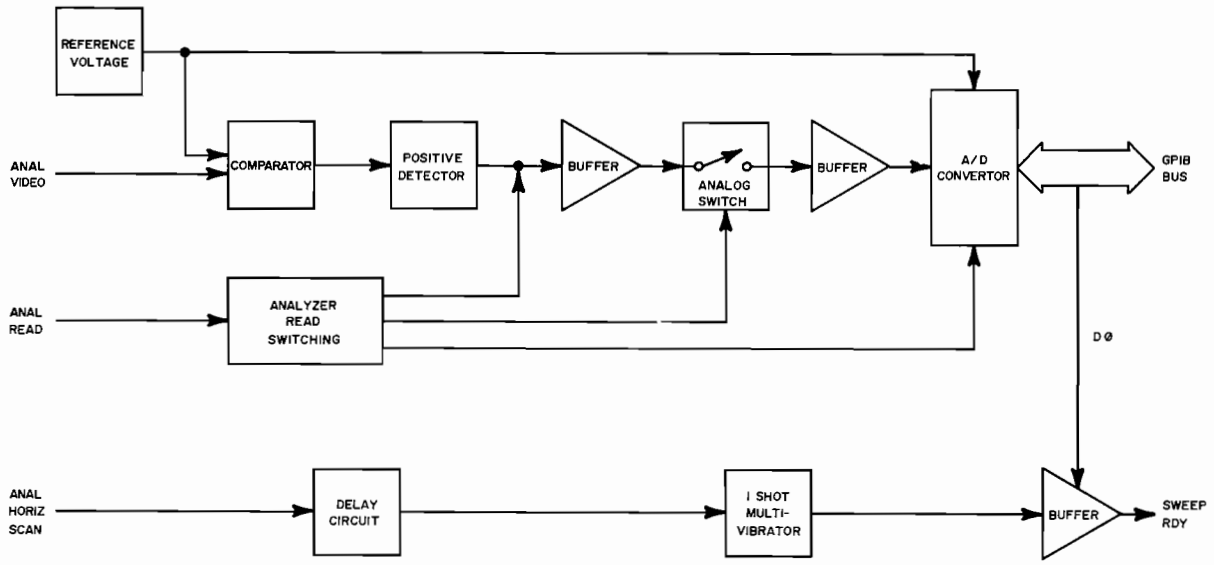


Figure 8-7 GPIB Analyzer Digitizer PC Board Detailed Block Diagram

Reference Voltage

CR1 maintains a reference voltage of 6.9 V to U8005A which inverts that to -9.5 V. This voltage is provided to U8007 and U8005B as reference voltage.

Anal Video

The analyzer video signal enters at pin 4 of P5905, is buffered by U8005B, and limited by U8009B. U8009A is an emitter follower which feeds the signal to bilateral switch U8008A.

Anal Horiz Scan

The analyzer horizontal scan enters at pin 5 of P5905 and fed through the delay circuitry which consists of U8001, U8002, U8003 and associated components. This signal is then fed to Q8001 which activates U8004. U8004 is a one-shot multivibrator, for the sweep ready status.

Anal Read

The analyzer read signal enters at pin 9 of P5904. This signal determines when the analog to digital conversion will commence. This signal enters the A/D converter at $\overline{RD}$ to give the start command.

A/D Converter

The analog to digital converter provides an 8-bit digital output. This process begins conversion when input is received from analyzer read. The digitized trace is fed out via the GPIB bus.

8-2-4 GPIB RF Attenuator Driver Detailed Theory of Operation

The input to AT7501 from the Output Amp is attenuated over an actual range of 0 to -127 dB, and an effective range of 0 to -120 dB (See Figure 8-7a and Programmable RF Attenuator Schematic). Because the programmable attenuator replaced the standard manual attenuator, which had a dB drop of approximately 6 to 7 dB, a software correction factor has been incorporated. The correction factor is as follows:

Over 910 MHz	= 0 dB
760 to 910 MHz	= 1 dB
560 to 760 MHz	= 2 dB
260 to 560 MHz	= 3 dB
30 to 260 MHz	= 4 dB
10 to 30 MHz	= 5 dB
Below 10 MHz	= 6 dB

The 7-bit input from the Attenuator Control & Display PC Board is active low. When any or all of these inputs go low, the output of its respective driver transistor (Q7501 thru Q7507) goes high, selecting a corresponding amount of resistance in AT7501.

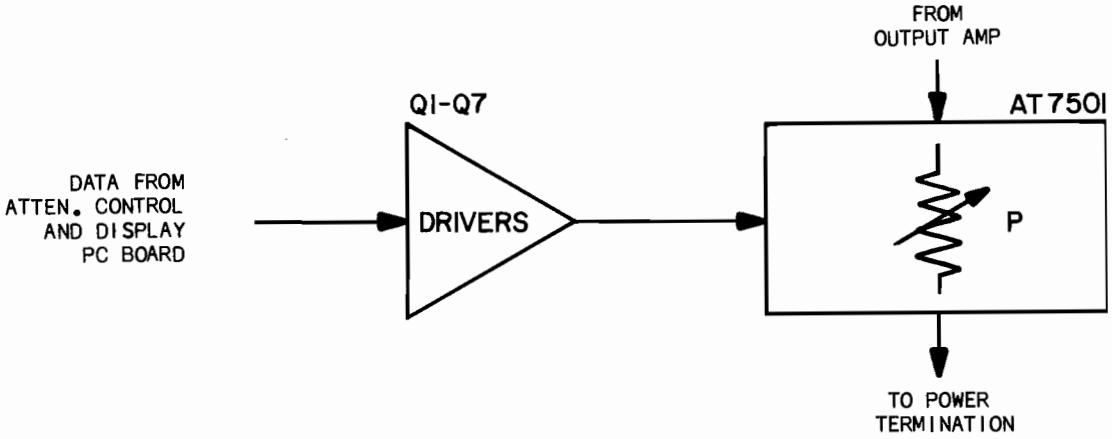


Figure 8-7a GPIB RF Attenuator Driver Block Diagram

8-3 PERFORMANCE EVALUATION

Since an external controller communicates with the FM/AM-1500 over the GPIB bus, performance evaluations will vary according to the programs written for different controllers. In general, performance evaluation involves the execution of an applicable program.

8-4 CALIBRATION

There are no specific calibration adjustments for the GPIB option.

8-5 TROUBLESHOOTING

8-5-1 GPIB RF ATTENUATOR DRIVER ASSY

SPECIAL ACCESSORY EQUIPMENT REQ'D: 1 Spectrum Analyzer---Capable of 920 Mhz at -64 dB
1 Logic Probe (or Digital Voltmeter)---Any

FIGURE REFERENCES: GPIB RF Attenuator Driver Assembly

TEST SET-UP DIAGRAM: N/A

STEP PROCEDURE

1. Set Front Panel controls as follows:

Control	Setting
(21) LCD	920.0000 FREQ MHz
(19) GEN/REC	GEN
(18) DUPLEX/SIMPLEX	SIMPLEX
(55) ATTENUATOR	0 dB
(13) PWR/OFF/BATT	PWR
(10) RF Output Level	0 dB

2. Verify +12V at pin 1 of J7501.

3. Connect external Spectrum Analyzer to TRANS/-40 dB DUPLEX connector (11).

4. Set RF Output Level Control (10) to set each of the inputs, one at a time, given in Table 8-1. For each selected input, verify that the corresponding input line goes low, the driver line goes high and that the display on external Spectrum Analyzer drops to a corresponding level.

J7501 Inputs (Active TTL Low)	Drivers (Active CMOS High)	Trans/-40 dB Duplex Output
1 dB (pin 2)	Q2	-1 dB (± 2)
2 dB (pin 3)	Q3	-2 dB (± 2)
4 dB (pin 4)	Q5	-4 dB (± 2)
8 dB (pin 5)	Q6	-8 dB (± 2)
16 dB (pin 6)	Q7	-16 dB (± 2)
32 dB (pin 7)	Q1	-32 dB (± 2)
64 dB (pin 8)	Q4	-64 dB (± 2)

Table 8-1 Programmable Attenuator Troubleshooting

5. Disconnect all test equipment.

8-5-2 GPIB LCD DISPLAY ASSY AND ATTENUATOR CONTROL DISPLAY PC BOARD

SPECIAL ACCESSORY EQUIPMENT REQ'D:
- 1 Dual Trace Oscilloscope
- 2 Oscilloscope Probes
- 1 Digital Voltmeter---Any

FIGURE REFERENCES:
- GPIB LCD Display Schematic
- GPIB Interface Module Schematic

TEST SET-UP DIAGRAM: N/A

STEP	PROCEDURE
1.	Remove GPIB Interface Module to gain access to PC Boards in Module. Leave all connectors connected to GPIB Interface Module.
2.	Verify TTL High at pins 17, 21, 27 and 23 of J5908 when respective keys on RF Level Control are depressed.
3.	Verify TTL low at pin 36 of J5908 (GPIB disabled).
4.	Connect Channel 1 of Oscilloscope to pin 5 of U8209 on Attenuator Control and Display PC Board.
5.	Using Channel 2 of Oscilloscope, verify that applicable outputs of U8209 are either in phase or 180 degrees out of phase with channel 1. If Channel 2 is 180 degrees out of phase with Channel 1, a corresponding segment on the LCD should be illuminated. See Figure 8-8.

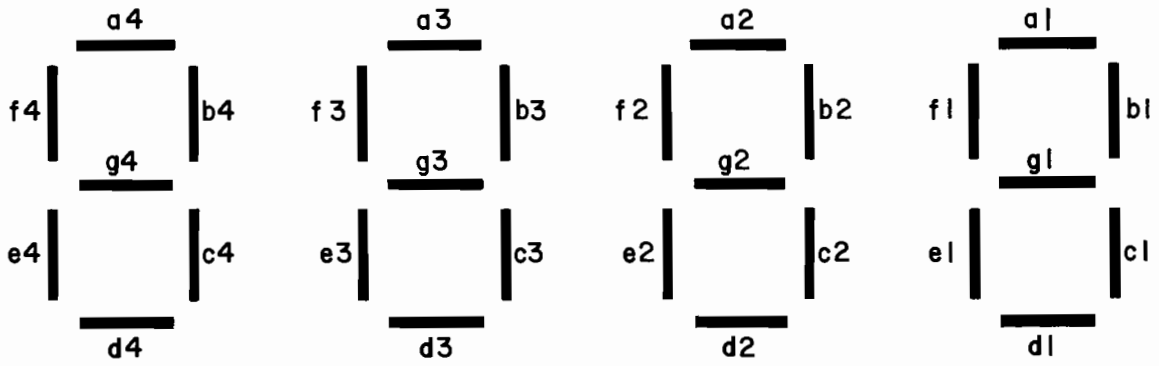


Figure 8-8 LCD Display Segment Lines

8-5-3 GPIB INTERFACE PC BOARD

SPECIAL ACCESSORY EQUIPMENT REQ'D:
- 1 Digital Voltmeter---Any
- 1 Frequency Counter---Capable of 2 MHz

FIGURE REFERENCES:
- GPIB Interface Module Assembly
- GPIB Interface Module Schematic

TEST SET-UP DIAGRAM: N/A

STEP PROCEDURE

1. Remove GPIB Interface Module to gain access to PC Boards in Module. Leave all connectors connected to GPIB Interface Module.

2. Set DIP Switch A8 on GPIB ON/OFF Switch (SW5901) to ON before powering up the FM/AM-1500.

3. Turn on the FM/AM-1500 and verify +5 V at pin 7 of K7901. Also verify that collector of Q7901 goes low.

4. Using Frequency Counter, verify a 2 MHz clock input at J5903.

5. Figure 8-9 shows the handshaking diagram for the Intel 8291A GPIB Talker/Listener (U8 on schematic). Notice that the 8291A uses positive logic, while IEEE-488-1978 convention is negative logic. Verify handshaking by verifying that data is transferred when the states of the handshake lines are correct. For further information on the 8291A, refer to Intel's Data Book.

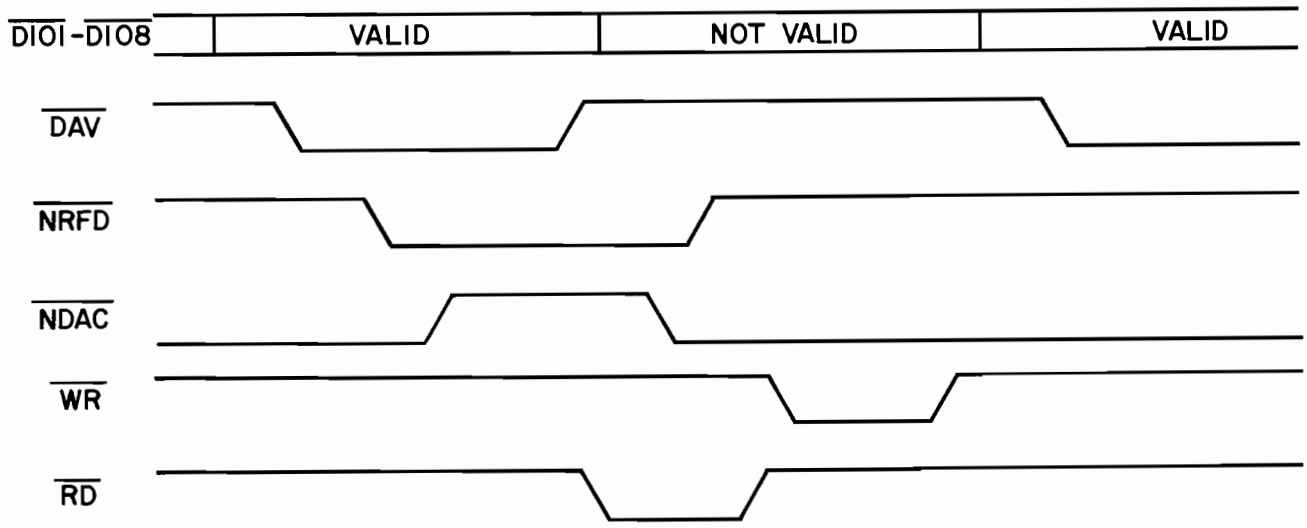
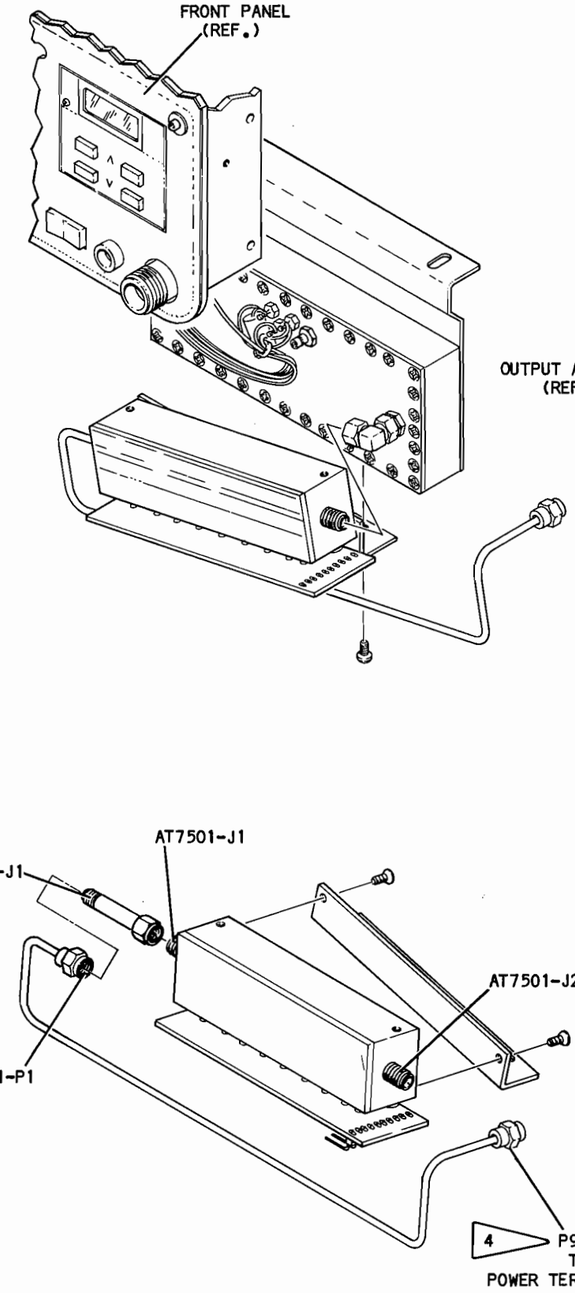
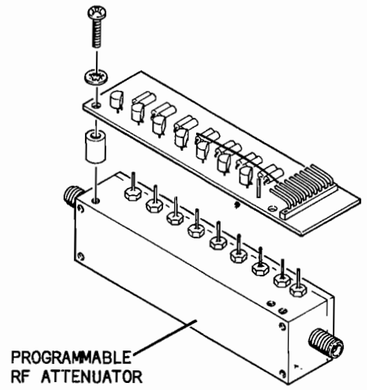


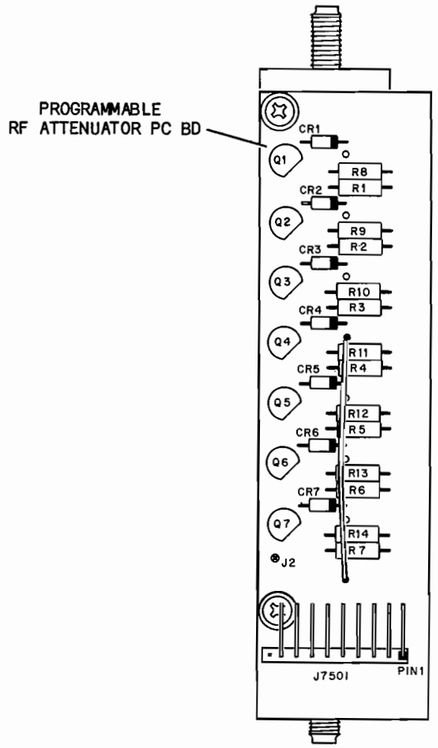
Figure 8-9 Handshaking Between GPIB Controller and FM/AM-1500

8-6 MECHANICAL ASSEMBLY/PC BOARDS

The following mechanical assemblies/PC Boards constitute the GPIB option:







NOTES:

MECH ASSY

1. THE REF DES SERIES FOR THE RF ATTENUATOR DRIVE MECH ASSY IS 7500 (I.E., J1 IS J7501).
2. DATA PART NO. 7005-5040-400.
3. REF CIRCUIT SCHEMATIC 0000-3612-501.
4. THRU SER. NO. 1993, P9801 WAS P6201.

PC BOARD

1. THE REF DES SERIES FOR THE RF ATTENUATOR PC BOARD IS 7500 (I.E., R1 IS R7501).
2. DATA PART NO. 7010-3632-501.
3. REF CIRCUIT SCHEMATIC 0000-3612-501.

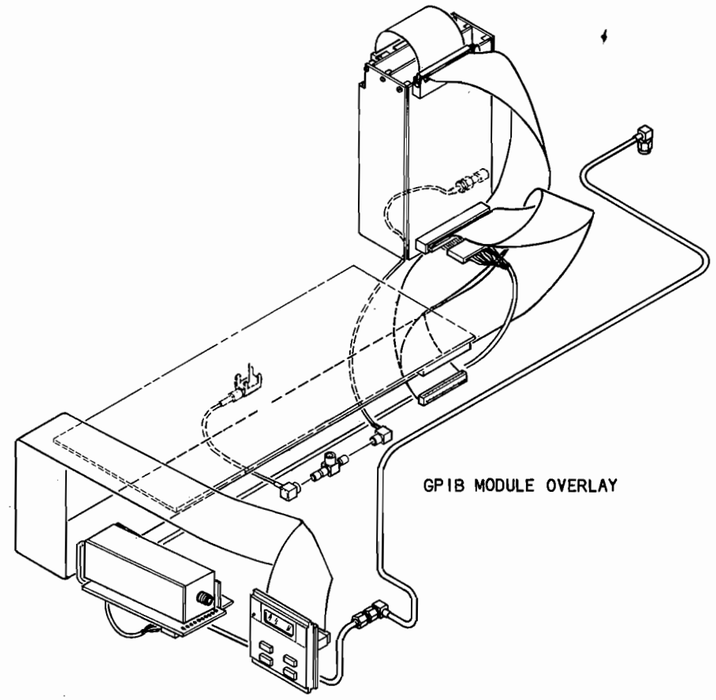
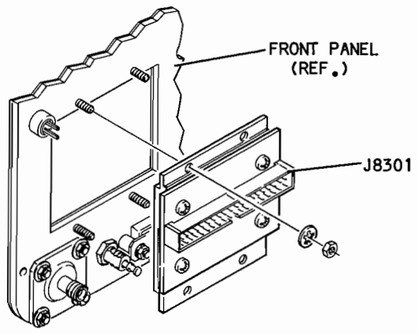
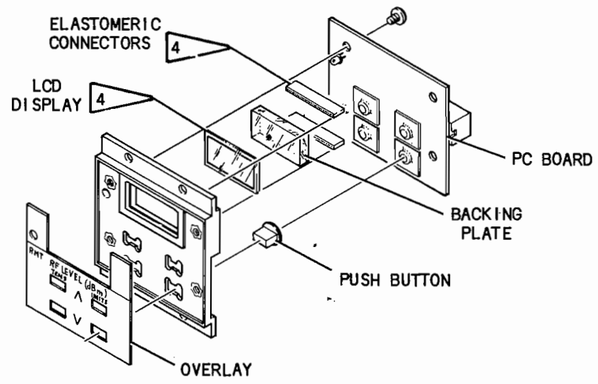


Figure 8-10 GPIB RF Attenuator Driver Assembly



LCD DISPLAY ASSEMBLY



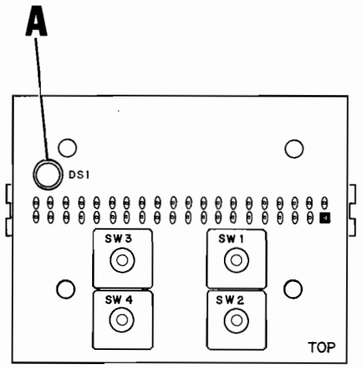
NOTES:

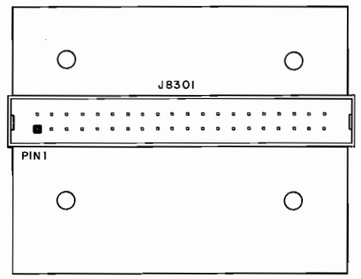
MECH ASSY

1. THE REF DES SERIES FOR THE LCD DISPLAY MECH ASSY IS 8300 (I.E., J1 IS J8301).
2. DATA PART NO. 7005-5046-200.
3. REF CIRCUIT SCHEMATIC 0000-5016-200.
4. USE EXTREME CARE WHEN HANDLING AND INSTALLING LCD AND ELASTOMERIC CONNECTORS.

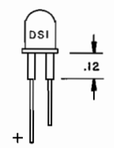
PC BOARD

1. THE REF DES SERIES FOR THE LCD DISPLAY PC BOARD IS 8100 (I.E., SW1 IS SW8101).
2. DATA PART NO. 7010-5036-200.
3. REF CIRCUIT SCHEMATIC 0000-5016-200.



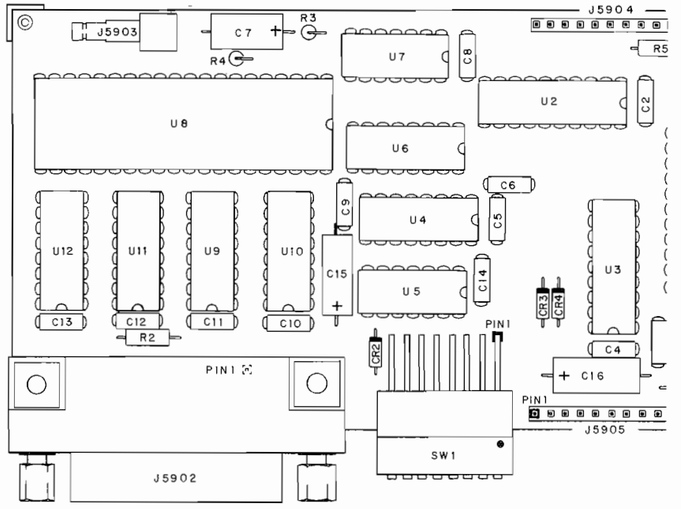


LCD DISPLAY PC BD

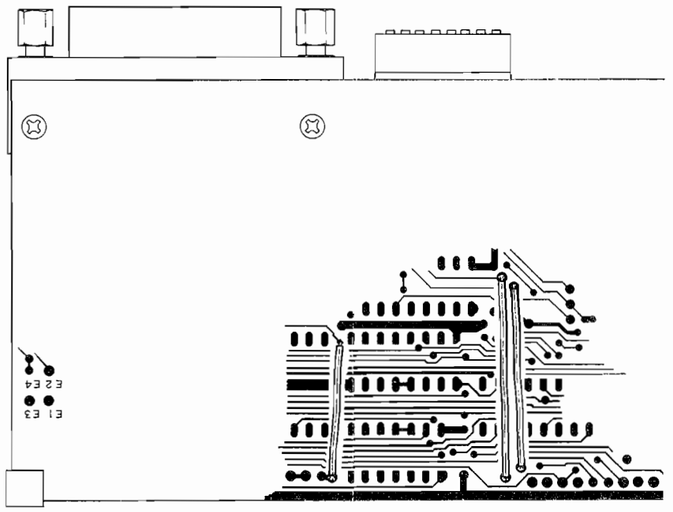


DETAIL **A**

Figure 8-11 GPIB LCD Display Assembly

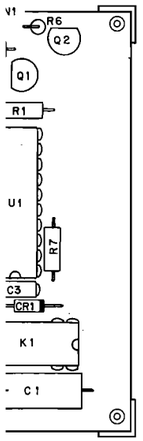


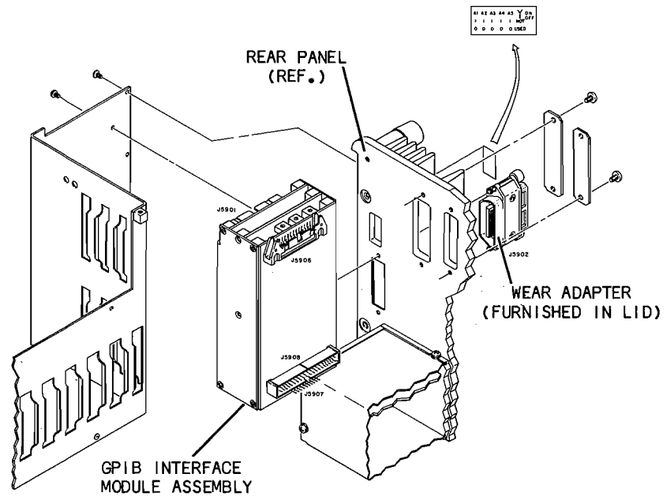
TOP VIEW

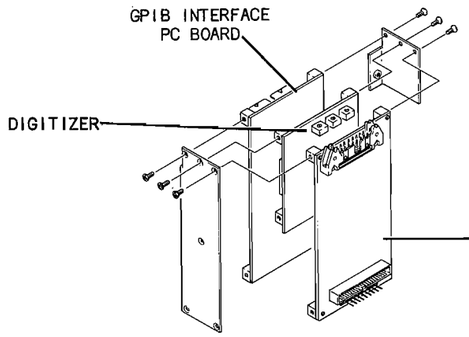


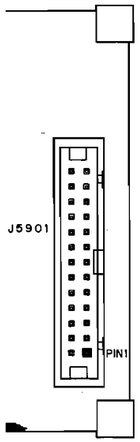
BOTTOM VIEW

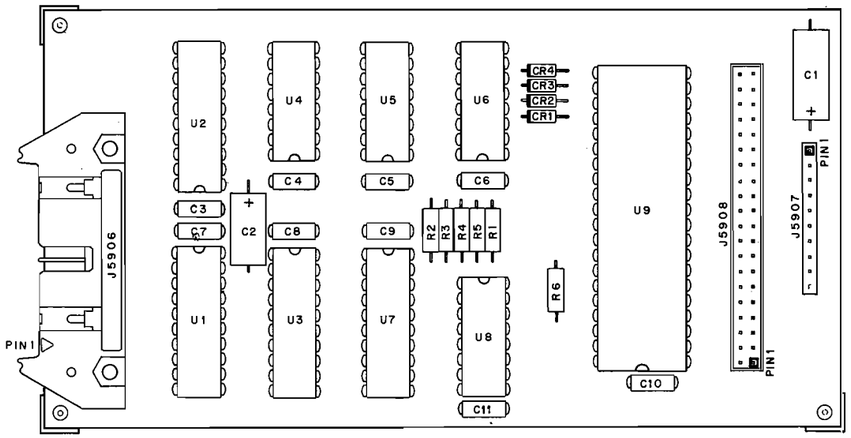
GPIB INTERFACE PC BOARD











ATTENUATOR CONTROL AND DISPLAY PC BOARD

NOTES:

MECH ASSY

1. THE REF DES SERIES FOR THE INTERFACE MODULE MECH ASSY IS 5900 (I.E., J1 IS J5901).
2. DATA PART NO. 7005-5045-900.
3. REF CIRCUIT SCHEMATIC 0000-5015-900.

ATTENUATOR CONTROL AND DISPLAY PC BOARD

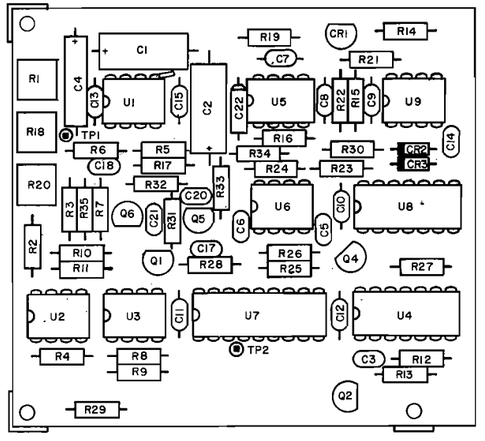
1. THE REF DES SERIES FOR THE ATTENUATOR CONTROL AND DISPLAY PC BOARD IS 8200 (I.E., R1 IS R8201).
2. DATA PART NO. 7010-5036-300.
3. REF CIRCUIT SCHEMATIC 0000-5015-900.

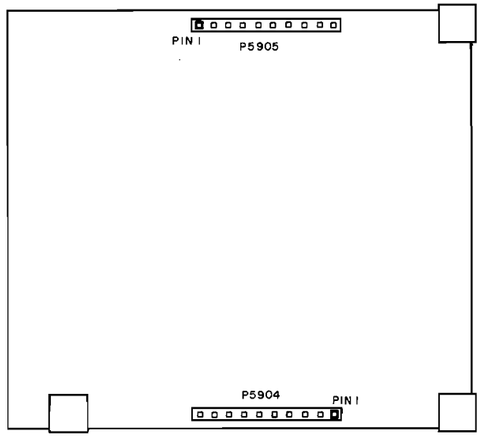
ANALYZER DIGITIZER PC BOARD

1. THE REF DES SERIES FOR THE ANALYZER DIGITIZER PC BOARD IS 8000 (I.E., R1 IS R8001).
2. DATA PART NO. 7010-5036-000.
3. REF CIRCUIT SCHEMATIC 0000-5015-900.

INTERFACE PC BOARD

1. THE REF DES SERIES FOR THE INTERFACE PC BOARD IS 7900 (I.E., R1 IS R7901).
2. DATA PART NO. 7010-5035-900.
3. REF CIRCUIT SCHEMATIC 0000-5015-900.



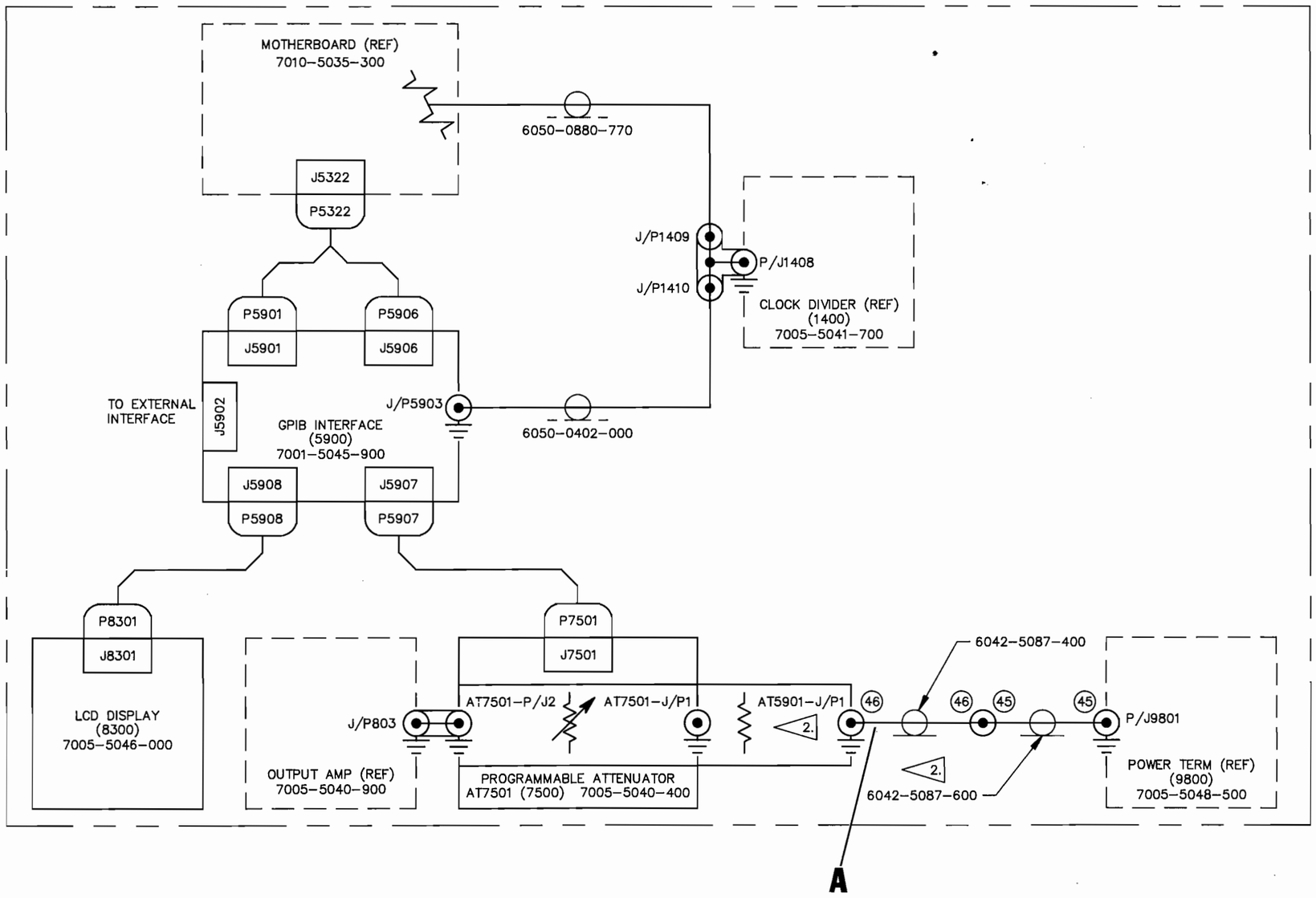


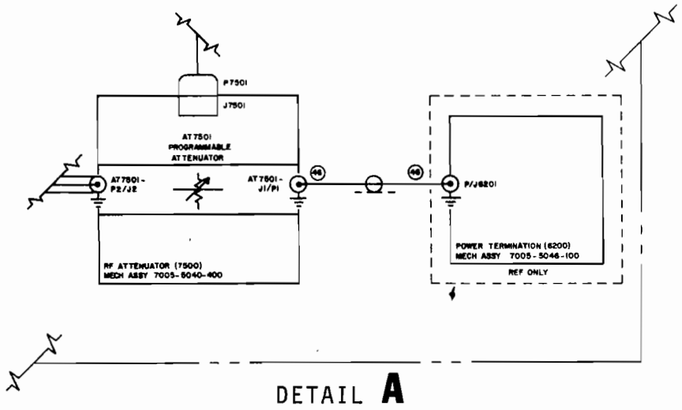
GPIB ANALYZER DIGITIZER PC BOARD

Figure 8-12 GPIB Interface Module Assembly

8-7 SCHEMATICS

The following schematics/interconnects are provided for the GPIB option:





DETAIL **A**

THRU SER. NO. 1993

NOTES:

1. ALL COAX SHIELDS ARE GROUNDED AT POINT OF TERMINATION.

2. THRU SER. NO. 1994:
AT5901 AND COAX (TAG #45) NOT USED. COAX (TAG #46) CONNECTED FROM AT 7501-J1 TO J9801.

Figure 8-13 GPIB Interface Assembly Interconnect 0000-5017-900-C3

STANDARDS:
(UNLESS OTHERWISE NOTED)

1. ALL REF NOS CARRY AN ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES:

   A. MECH - (7500)
   B. PC BD ASSY - (7500)
   C.
   D.

2. ALL RESISTORS ARE 1/4 W, 5% TOLERANCE.

3. ALL RESISTANCE IS EXPRESSED IN OHMS.

4. FOR INTERCONNECTIONS REFER TO COAX INTERCONNECT AND GPIB INTERFACE INTERCONNECT.

5. LAST REF NOS USED:
   AT1, R14, J2, Q7, CR7

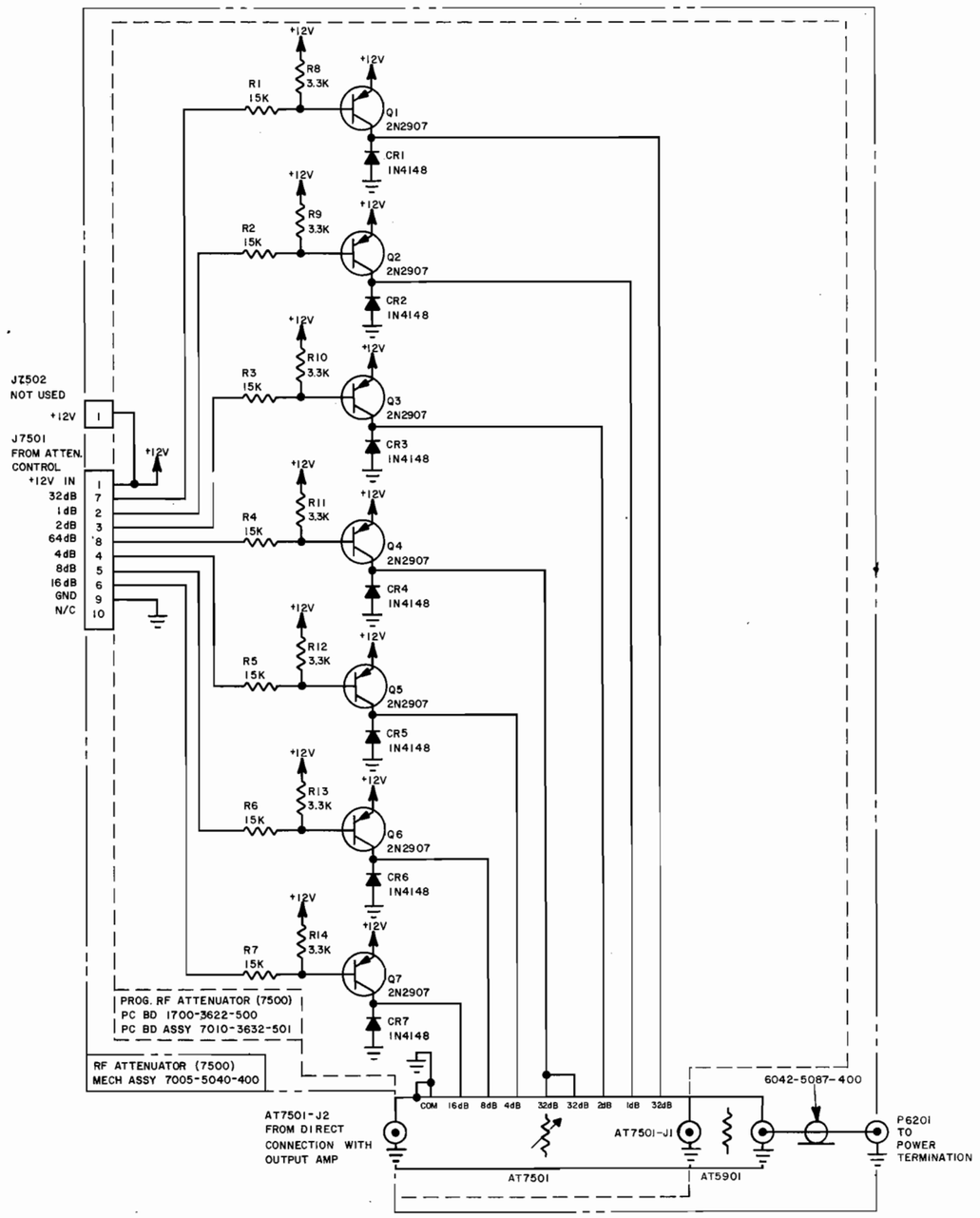
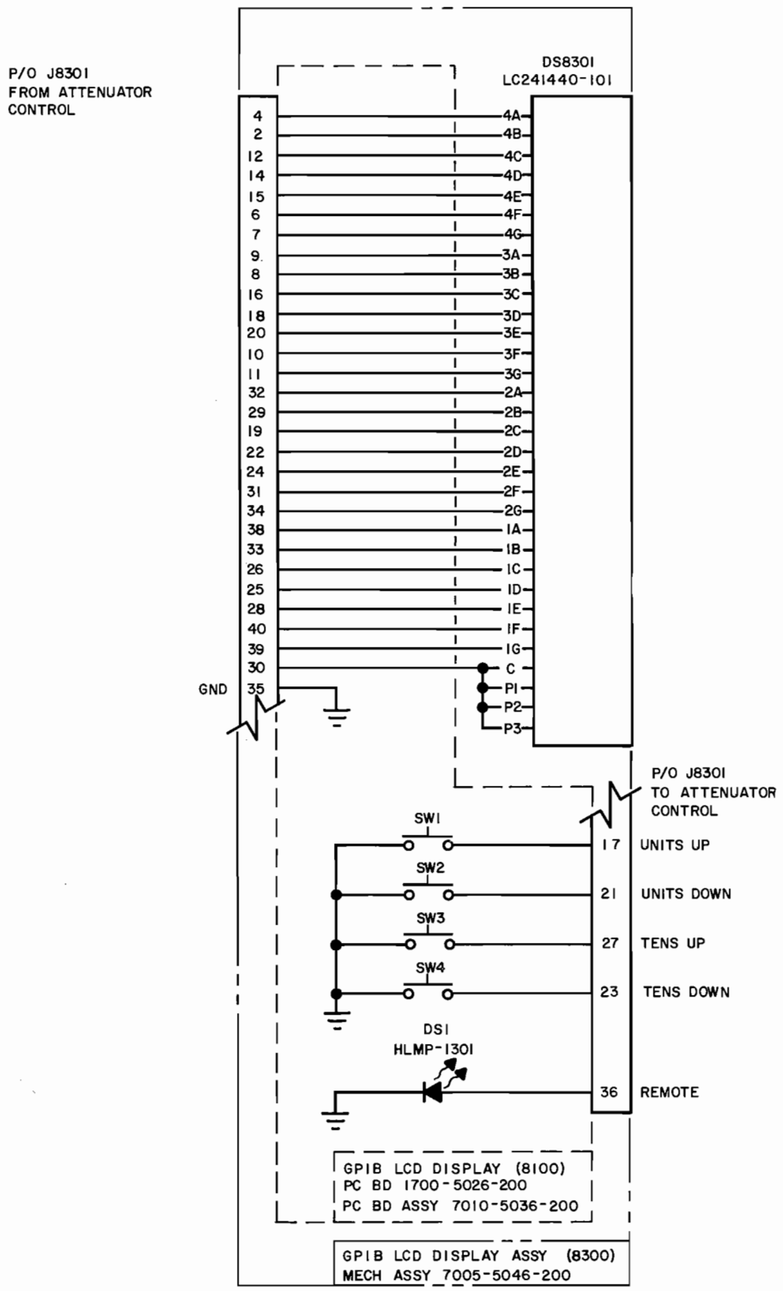


Figure 8-14 GPIB RF Attenuator Driver Schematic (0000-3612-501)



STANDARDS:
(UNLESS OTHERWISE NOTED)

1. ALL REF NOS CARRY AN ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES:

   A. MECH - 8300
   B. PC BD ASSY - 8100 (E.G., SW1 IS SW8101)

2. LAST REF NO USED:
   DS1, SW4, J8301, DS8301

Figure 8-15 GPIB LCD Display Assembly Schematic (0000-5016-200)

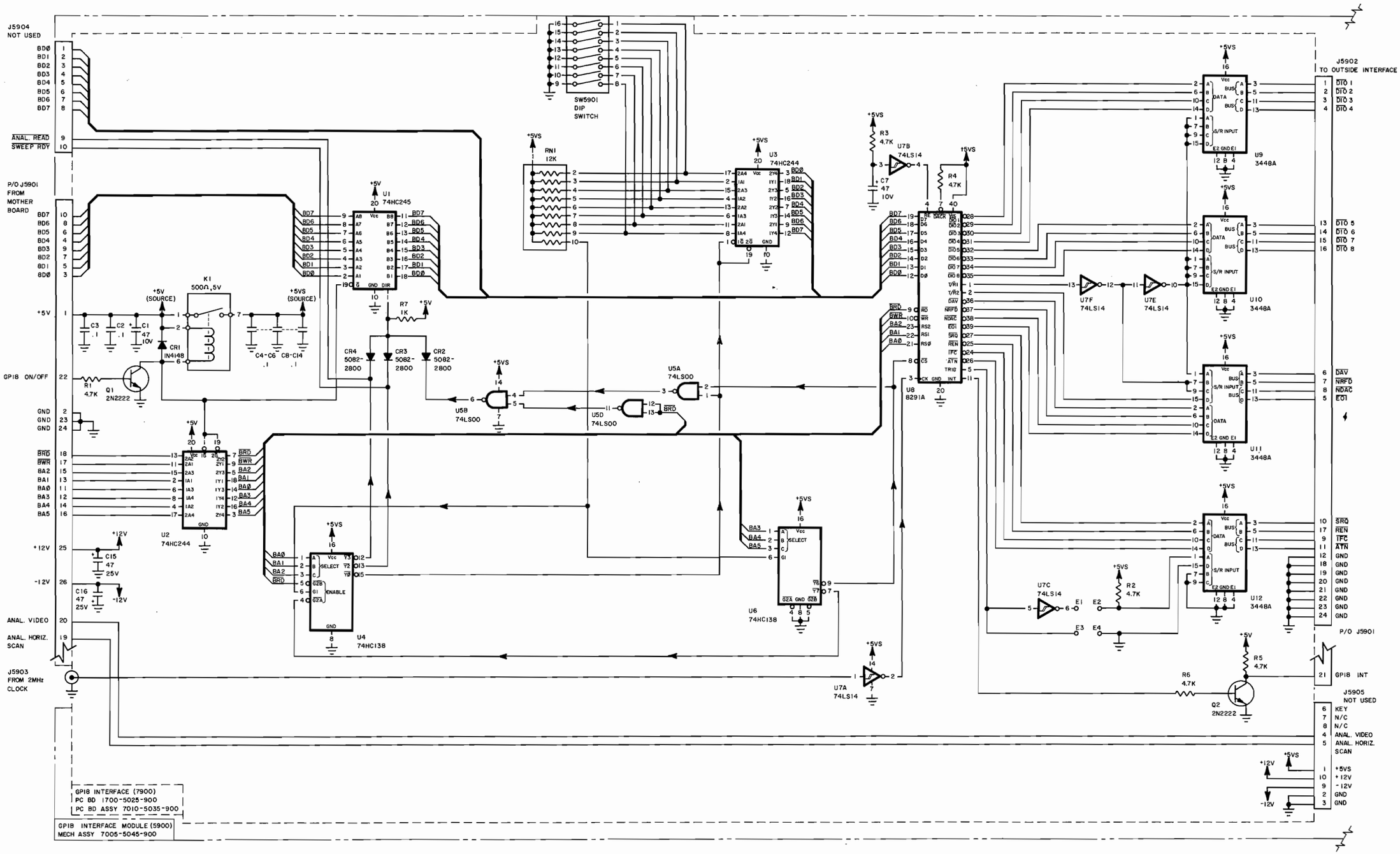


Figure 8-16 GPIB Interface Module Schematic (Sheet 1 of 3)
0000-5015-900-C

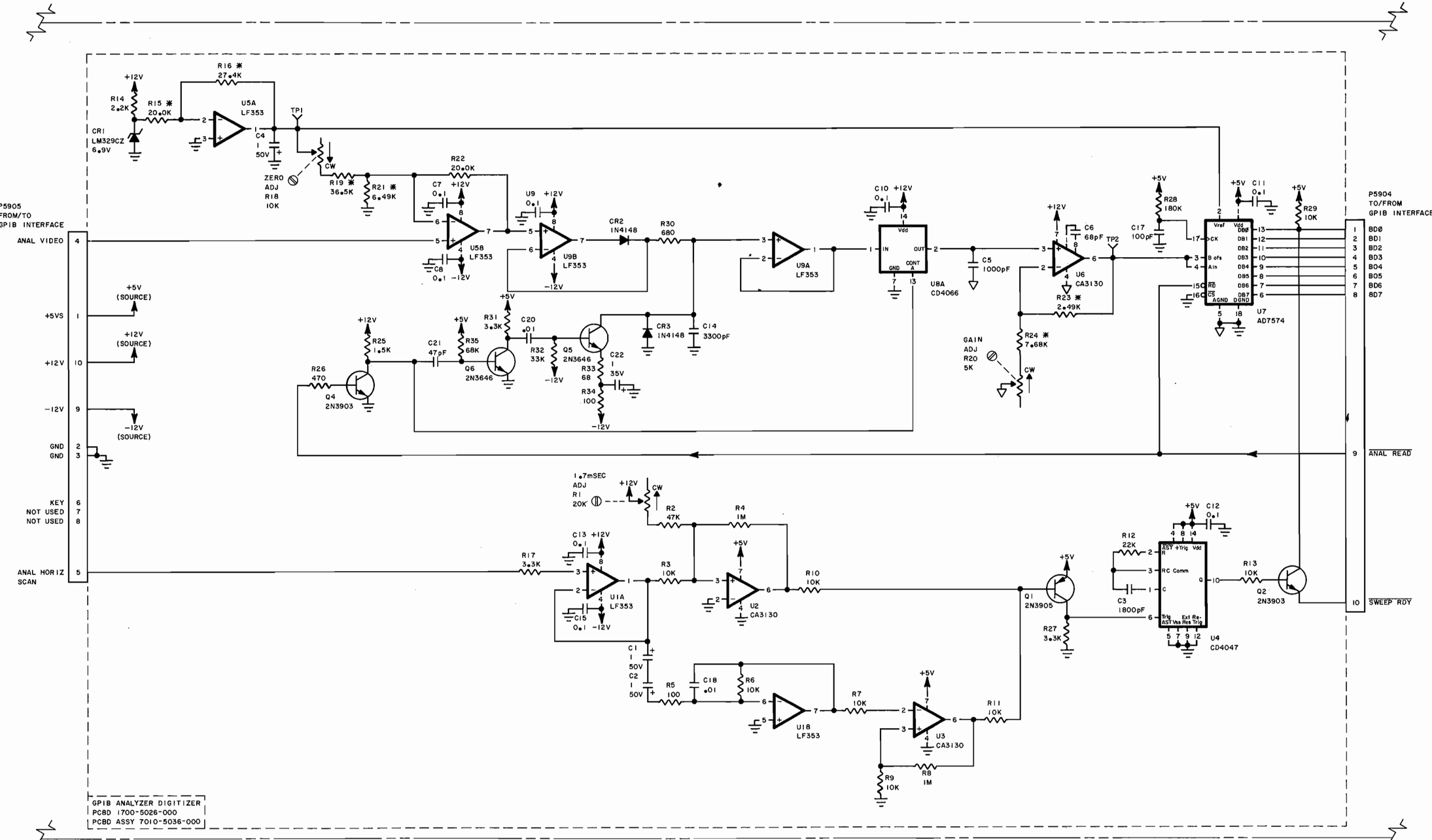


Figure 8-16 GPIB Interface Module Schematic (Sheet 2 of 3) 0000-5015-900-C

STANDARDS:
(UNLESS OTHERWISE NOTED)

1. ALL REF NOS CARRY AN ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES:

   A. MECH - 5900
   B. ATTEN. CONT. PC BD ASSY 8200 (E.G., R1 IS R8201).
   C. GPIB INTERFACE PC BD ASSY 7900 (E.G., R1 IS R7901).
   D.

2. ALL RESISTORS ARE 1/4 W, 5% TOLERANCE.

3. ALL RESISTANCE IS EXPRESSED IN OHMS.

4. ALL CAPACITANCE IS EXPRESSED IN MICROFARADS.

NOTES:

1. LAST REF NOS USED:
   J5908, K7901
   C8211, Q7902
   U8209, RN7901
   R8206, SW7901
   CA8204, CR7904
   R7907
   C7916
   U7912

2. I.C. FUNCTION NOT USED:
   U7905C, U7907D

Figure 8-16 GPIB Interface Module Schematic (Sheet 3 of 3)
0000-5015-900-C

SECTION 9 - CELLULAR OPTION

9-1 INTRODUCTION

The cellular option enables the FM/AM-1500 to test cellular mobile radios using "manual" tests and cell site simulation tests. To accomplish this task, a Cellular Controller PC Board has been added to the basic FM/AM-1500. With this new board installed, the FM/AM-1500 still maintains its capabilities as a communications service monitor, but also will simulate cell sites and act as an MTSO (Mobile Telephone Switching Office). In addition to the new PC Board, two new connectors are provided on the rear panel for the mobile test interface cable and the printer interface cable. An optional ICD-1500 interconnect box is available for use as an external device capable of monitoring each of the mobile radio test points.

9-2 THEORY OF OPERATION

The FM/AM-1500 communicates with a mobile radio via both digital and RF signals. Communication within the FM/AM-1500 is accomplished between a 6809 CPU on the Cellular Controller PC Board and a Z80 CPU on the CPU/MEMORY PC Board. The communication modes are explained as follows:

A. Mobile Digital Interface

The mobile digital interface is the circuitry which allows the Cellular Controller PC Board to communicate with the mobile over the AMPS - configured interface bus. This port (J9102) is an 8-bit data bus, with three control lines for handshaking: DCL (Direction Control Line), TCL (Test Control Line), and CL (Clock Line). Circuitry on the Cellular Controller PC Board for this interface consists of a 6522 VIA and IEEE-488 bus drivers. The handshake control is software controlled, and the bus drivers provide the necessary bus termination and drive to meet IEEE-488 specifications.

Functions for this port include:

1. Allow the FM/AM-1500 to send test commands to the mobile.

2. Allow the FM/AM-1500 to request status from the mobile.

3. Allow the FM/AM-1500 to test an AMPS-compatible mobile control unit.

B. Mobile RF Interface

The mobile RF interface is used to communicate with the mobile for cell site simulation, data verification, command/response tasks and signalling purposes. This function is bi-directional in that the FM/AM-1500 must generate and receive data and tones. Each of these two aspects are discussed as follows:

FM/AM-1500 generated data/tones

The FM/AM-1500 must communicate through the RF port (TRANS/-40 dB DUPLEX Connector) in the following cases:

1. Overhead messages (system control messages) sent to the mobile

2. Page messages (contact the mobile) sent to the mobile

3. Order messages (ring phone, change frequency, hang-up, etc.) sent to the mobile

4. SAT (Supervisory Audio Tone) transmission to the mobile

5. Audio to mobile for call completion

Items 1, 2 and 3 above refer to the digital data sent serially to the mobile. This data is 10 kHz, Manchester serial data which the mobile monitors and interprets as control data from a cell site. The circuitry on the Cellular Controller PC Board to accomplish the generate data stream consists of a 6522 VIA, a multiplying digital to analog converter for level adjustment, and switching for AM or FM modulation selection (cellular operation uses FM modulation only).

Item numbers 4 and 5 above refer to tones and/or voice sent to the mobile whenever the mobile is on a voice channel. The mobile expects the SAT frequency to be present on the FOVC (Forward Voice Channel) and the operator of the FM/AM-1500 will want to verify audio function when a call is completed. The tones sent (SAT and test tones) will be generated by the tone generators within the basic FM/AM-1500 (tone #2 is the SAT generator).

FM/AM-1500 received data/tones

The FM/AM-1500 must receive data/tones in the following cases:

1. Page response from the mobile

2. Reverse control data channel responses

3. Test transmissions over the RF port from the mobile

4. SAT and ST (Signaling Tone) transmission for call signaling

5. DTMF (Dual Tone, Multiple Frequency) tone signaling from the mobile

6. Audio from the mobile after call is completed

Items 1, 2 and 3 above refer to the data stream from the mobile to the FM/AM-1500. The mobile will respond to commands sent from the FM/AM-1500 by sending data back on the RCC (Reverse Control Channel) and the RVC (Reverse Voice Channel). The circuitry on the Cellular Controller PC Board required to decode the data from the demodulated audio consists of a programmable level control (MDAC), a programmable filter, a data clock generator, and a serial to parallel converter. The 6809 CPU will configure this hardware to the 10 kHz

Manchester data, and the serial to parallel circuitry will generate an interrupt after every 8 bits of data have been received.

Items 4, 5 and 6 above refer to the tone/voice received from the mobile. The SAT will be transponded from the mobile whenever the mobile is on a voice channel. The ST is sent as an "on-hook" indication and a "flash" signal. The DTMF tones are used for end-to-end signaling from the mobile. The circuitry to detect SAT, ST and DTMF is similar to the data detection. The demod audio is put through a level circuit and a programmable filter, and is then sent to a counter circuit for frequency measurement. Also, a signal is produced which may be used as a "valid tone" indication (active if signal gets through the filter).

C. CPU-CPU Interface

To allow bi-directional communication between the cellular CPU (6809) and the existing CPU (Z80), a CPU-CPU interface is required. On the cellular side, the parallel ports of a VIA are used for data and handshake control. On the FM/AM-1500 side, bus latches and bus buffers are used to allow bi-directional data and handshaking to occur. The interface consists of 8 data bits (zd0-zd7), direction control line (zdir), test control line (ztcl), and a clock line (zcl). The function and use of each of these lines is as follows:

zd0 thru zd7 - bi-directional data lines, the direction of which is controlled by the zdir line. When zdir = 0, data direction is from the Z80 to the 6809.

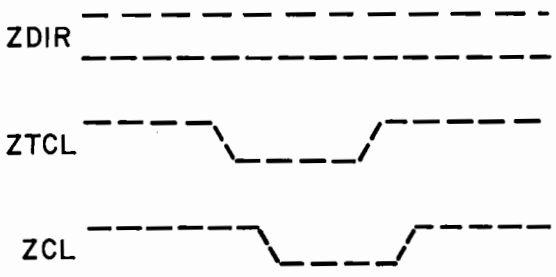
zdir - unidirection control line that determines data direction of zd0 thru zd7. This line is driven by the 6809.

ztcl - unidirectional control line used to signal that data sent by the Z80 is valid and data received by the Z80 has been read. This line is driven by the Z80.

zcl - unidirectional control line used to signal that data sent by the 6809 has been read. This line is driven by the 6809.

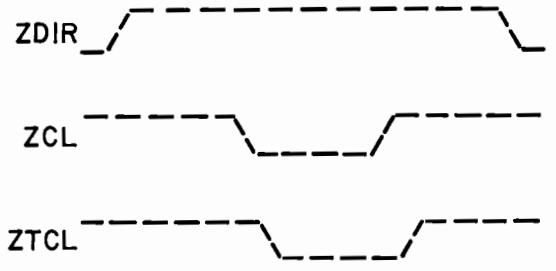
Bus timing diagrams for the different modes are as follows:

---1500 TO CELLULAR CONTROLLER COMMAND OR DATA TRANSFER---



1 - z80 checks for zdir low, zcl hi
2 - z80 sets ztcl hi
3 - z80 sets data on zd0-zd7
4 - z80 sets ztcl low to signal data ready
5 - 6809 detects ztcl low
6 - 6809 reads byte from zd0-zd7
7 - 6809 sets zcl low to signal data accepted
8 - z80 detects zcl low
9 - z80 sets ztcl hi to signal data handshake
10 - 6809 sets zcl hi to complete transfer

---CELLULAR CONTROLLER TO 1500 DATA TRANSFER---



1 - 6809 checks for ztcl high
2 - 6809 sets zdir high (reverse data direction)
3 - 6809 sets data on zd0-zd7
4 - 6809 sets zcl low
5 - z80 detects zdir high and zcl low
6 - z80 reads data byte from zd0-zd7
7 - z80 sets ztcl low
8 - 6809 detects ztcl low, sets zcl high
9 - z80 detects zcl high, sets ztcl high
10 - 6809 sets zdir low

9-2-1 Cellular Controller PC Board Detailed Theory of Operation

CPU

The 6809 CPU (U6525) controls the devices on the Cellular Controller PC Board (See Figure 9-1 and Cellular Controller Schematic). The CPU fetches an instruction from the ROM and then takes appropriate action, which may be changes in the data in its internal registers, in the RAM or in the I/O devices. After the appropriate action is executed, the next instruction is fetched from the ROM. This process continues as long as power is applied to the Cellular Controller PC Board.

Three control lines are used to interrupt the CPU: the $\overline{\text{RESET}}$ line (pin 37), the $\overline{\text{IRQ}}$ line (pin 3) and the $\overline{\text{FIRQ}}$ line (pin 4). The $\overline{\text{RESET}}$ line goes low when power is first applied to the PC Board. This is accomplished by U6516 A and B, R6520, CR6503 and C6534. When the $\overline{\text{RESET}}$ line goes low, the CPU is initialized and starts fetching instructions from the initialization routine in the ROM. After initialization is complete, the task rou-tines are accessed. When the $\overline{\text{IRQ}}$ line goes low, the CPU accesses the interrupt routine after the current instruction is completed. The interrupt routine determines the source of the interrupt and services the device that sent the interrupt. Optionally, the $\overline{\text{IRQ}}$ function may be disabled by setting the appropriate bit in the CPU's internal status register. The $\overline{\text{FIRQ}}$ line acts in a manner similar to the $\overline{\text{IRQ}}$ line, except that the $\overline{\text{FIRQ}}$ has priority over $\overline{\text{IRQ}}$. For more information on the 6809, refer to the manufacturer's data sheet or data book.

ROM

U6527 and U6532 (if installed in the X1 slot) are the ROM (Read Only Memory) ICs. These ICs contain instructions and look-up tables for the CPU. Jumpers are provided (JTB6505 and JTB6507) to allow expansion to larger ROMs. There are no provisions for writing to the ROMs. The ROMs are non-volatile, which means they retain their memory when power is removed.

RAM

U6530 is the RAM (Random Access Memory). The RAM contains data which may be altered at will by the CPU. The RAM is a volatile device, which means its memory will be lost when power is removed.

Address Decoder

The Address Decoder consists of U6526, U6533, U6534 and U6535. U6526 selects either one of three 16 K blocks of memory or one of the I/O devices. The $8000_{(H)}$ to $BFFF_{(H)}$ output is used to enable U6533. U6533, in turn, may select one of the two VIA (Versatile Interface Adapters), one of the two counter/timers or it may enable U6534 and U6535. U6534 and U6535 select one of the remaining I/O devices. The appropriate device, or memory, is selected when its address is present on the address bus.

Control Logic

The control logic consists of U6529 A, B and D and U6528 A, B and C. The control logic produces the $\overline{\text{RD}}$, $\overline{\text{WR}}$ and MEMEN signals, depending on the states of the R/$\overline{\text{W}}$, E and Q lines from the CPU. See Table 9-1 for control logic operation.

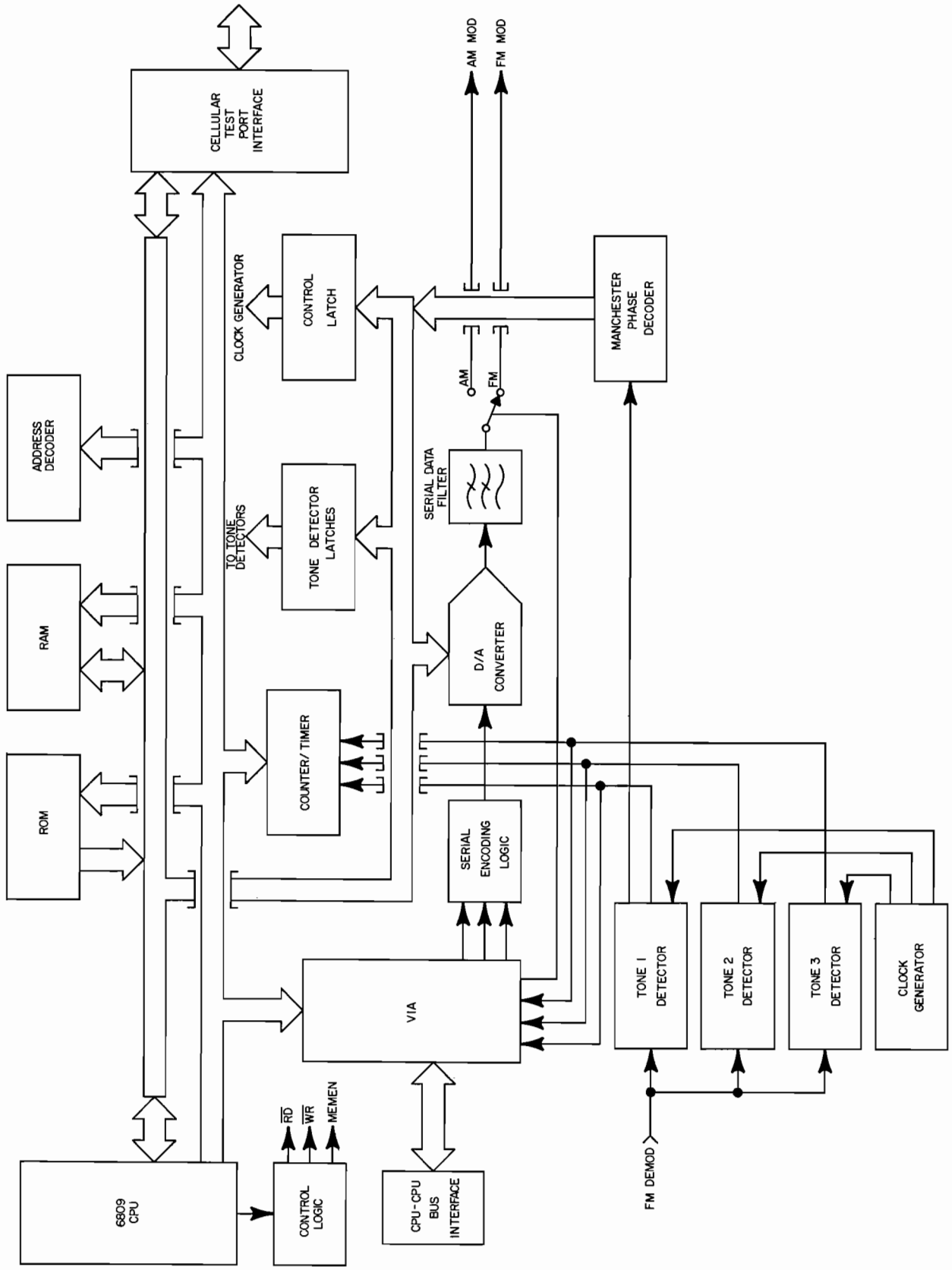


Figure 9-1 Cellular Controller PC Board Detailed Block Diagram

E U6525, pin 34	Q U6525, pin 35	MEMEN U6528C, pin 8	R/$\overline{W}$ U6525, pin 32	$\overline{RD}$ U6529D, pin 11	$\overline{WR}$ U6529B, pin 6
0	0	0	0	1	1
0	1	1	0	1	0
1	0	1	0	1	0
1	1	1	0	1	0
0	0	0	1	1	1
0	1	1	1	0	1
1	0	1	1	0	1
1	1	1	1	0	1

Table 9-1 Control Logic Truth Table

CPU-CPU Bus Interface

The CPU-CPU Bus Interface consists of U6501, U6502, and U6504 thru U6509. U6505 and U6506 interface data, while U6507, U6508 and U6509 interface control information. U6501 and U6502 are address decoders for the Z80 CPU (on the CPU/MEMORY PC Board) side of the interface. The interface is accessed by the 6809 CPU through U6511, a 6522 VIA.

U6505 and U6506 are 8-bit latches which temporarily store data to be transferred between the CPUs. U6505 stores data which is transferred from the Z80 to the 6809. U6506 stores data which is transferred from the 6809 to the Z80.

U6507, U6508 and U6509 interface the control signals. U6507 and U6509 store control information which is transferred from the Z80 to the 6809. U6508 stores control information which is transferred from the 6809 to the Z80.

Cellular Test Port Interface

The Cellular Test Port Interface consists of U6516D, U6516E, U6519, U6512A, U6523, U6524, U6520, U6521 and U6522. U6520, U6521 and U6522 are line drivers/receivers. Each of these line drivers/receivers have four driver/receiver gates for a total of twelve driver/receivers. The mode (driver output or receiver input) is determined by U6516E, U6516F, Q6501, U6512A and U6519. U6519 is a VIA which interfaces the twenty I/O lines and the counter and shift register. U6524 is a line receiver for the serial port and U6523 is a line driver for the serial port.

VIA

U6511, the VIA (Versatile Interface Adapter), interfaces the 6809 side of the interface adapter with the 6809 processor bus. The VIA also performs the serial data conversion, detects tones 1 thru 3 and selects AM or FM modulation for the serial data (cellular operation uses FM modulation only). The VIA also contains a parallel to serial converter and a 16-bit timer. For more information concerning the VIA, see the manufacturer's data sheet or data book.

Serial Encoding Logic

U6512 B, C and D, U6513A and U6514A form the serial encoding logic. U6513A selects either the output of U6512D (NRZ data) or the output of U6512B (Manchester phase encoding). The output of U6513A is applied to a non-inverting amplifier, U6514A. The selected serial data is applied to the reference input of the D/A converter.

D/A Converter

The D/A converter determines the modulation level of the serial data. The digital to analog converter, U6515, captures 8 bits of level information from the 6809 bus when instructed to do so by the address decoder. The D/A converter scales down the level of the serial data by a factor determined by the 8 bits of level information. U6514B converts the current out of U6515 to a voltage level which is fed to the serial data filter.

Serial Data Filter

The serial data filter consists of R6510, R6508, R6507, C6518, C6519 and C6520. This filter shapes the rising and falling edge of the serial data before it is modulated. U6513B routes the filtered serial data to the AM or FM modulator.

Counter/Timer Circuit

The counter/timer circuit consists of U6531, U6517 and U6518. U6531 divides the 2 MHz processor clock by 2, 4, 8 or 16. The division factor is jumper programmable and is normally set to divide by 4. This setting produces a clock frequency of 500 kHz which is fed to U6517 and U6518. U6517 measures the duration of Tone 3 and counts the number of clock shifts for the Manchester phase decoder. U6518 measures the duration of Tone 1 and Tone 2. For more information concerning U6517 and U6518, see the manufacturer's data sheet or data book.

Tone Detector Latches

The tone detector latches consist of U6562, U6563, U6564, U6565 and U6567. These latches capture tone detector information from the data bus when instructed to do so by the Address Decoder. U6562, U6563, U6564 and U6565 latch active filter frequency and circuit Q parameters. U6567 latches response time information for the tone detectors. U6568 converts the TTL output of U6567 to a 0 to 12 V swing.

Control Latch

The control latch, U6566, captures clock information from the data bus when instructed to do so by the Address Decoder. The output of the control latch is applied to the clock generator.

Clock Generator

The clock generator consists of U6569 thru U6572. U6569 is a 14-stage binary counter which produces output frequencies of 500 kHz, 250 kHz, 125 kHz, 62.5 kHz, 31.25 kHz, 15.625 kHz and 7.8125 kHz. CMOS switches U6570, U6571 and U6572 select one of these frequencies and apply the selected frequency to the applicable tone detector. U6570 selects a frequency for Tone detector #1. U6571 selects a frequency for Tone detector #2. U6572 selects a frequency for Tone detector #3. These CMOS switches are controlled by the control latch.

Tone Detector #2 and #3

Tone detector #2 is used for SAT detection (5970, 6000 or 6030 Hz). Tone detector #3 is used for detection of a 1 KHz tone and is provided for future use. Tone detectors #2 and #3 are identical in operation. Therefore, only Tone detector #2 will be discussed. Tone detector #2 consists of U6552, U6553, U6541 A and C, U6554, U6555 and U6556. U6552 is a multiplying digital to analog converter, which controls the relative level into the active filter for minimum level detection. The active filter, U6553, is configured as a programmable bandpass filter. The output of U6553, pin 12, is applied to U6554 and U6555. U6554 is a squaring amplifier, the output of which is applied to the counter/timers. U6555 is a detector, the output (pin 7) of which is applied to CMOS switches U6541 A and C. These switches select the time constant of the detector. The output of the CMOS switches is applied to a comparator, U6556A. The comparator provides the VIA with a digital signal which indicates the presence of a tone.

Tone Detector #1

Tone detector #1 is used for 10 KHz ST (Signalling Tone) detection. Tone detector #1 operates in the same manner as Tone detectors #2 and #3, with a few exceptions. The active filter, U6540, is configured as a bandpass filter when it is being driven by U6538. When the active filter is driven by U6537, the filter is configured as a lowpass filter. At the present time, software prevents U6537 from changing, keeping U6540 configured as a bandpass filter. The output of U6540 is applied to the detector, U6543. The unfiltered serial data is applied to the Manchester phase detector. The squaring amp for Tone detector #1 is in the Manchester phase decoding circuitry. All other aspects of Tone detector #1 are the same as Tone detectors #2 and #3.

Manchester Phase Detector

The Manchester phase detector consists of U6541B, U6542, U6546A, U6547, U6548, U6549, U6550 and U6538. Serial data enters the Manchester phase detector at pin 15 of U6541B. U6541B selects a slow or fast time constant, depending on the baud rate. U6542 is a squaring amp, the output of which is applied to the shift register, U6549, to the clock separator, U6546A and U6547, and to the counter/timers. U6546A and U6547 form a clock separator and produce a data clock signal which is applied to the shift register, U6549, to the bit counter, U6548, and to the counter/timer through Q6502. The counter/timer will interrupt the processor every 8 bits so that the contents of the shift register can be latched into U6550. The latch signal is generated by the bit counter, U6548. The microprocessor can preset U6548 in order to synchronize it with the data stream. U6551 is provided to adjust the clock separator for a particular baud rate.

9-3 PERFORMANCE EVALUATION

Performance evaluation for the Cellular option consists of accessing the Cellular Menu and executing all 50 commands. Procedures to be used are given in the Cellular Operator's Guide. If the Cellular commands fail to perform as specified, calibration should be checked and then troubleshooting should be undertaken.

9-4 CALIBRATION

9-4-1 CELLULAR CONTROLLER PC BOARD

SPECIAL ACCESSORY EQUIPMENT REQ'D:
1 Oscilloscope---Dual Trace
2 Oscilloscope Probes
1 Frequency Counter---Capable of 0.1 Hz resolution at 10 KHz

FIGURE REFERENCES: Cellular Controller PC Board

TEST SET-UP DIAGRAM: N/A

STEP PROCEDURE

1. Connect Frequency Counter to TP 1-24 test point (or to pin 18 of U6511).

2. Transmit cellular data by executing the RCVS1 command (#26) i.e., call up the cellular DIRECTORY menu and execute the RCVS1 command by pressing "EXEC, 2nd, CELL, 2, 6, ENTER".

3. Adjust trim capacitor C6574 for a reading on Frequency Counter of 10000.0 Hz (±0.5 Hz).

4. Exit the RCVS1 command.

5. Set FM/AM front panel controls as follows:

CONTROL	SETTING
(6) DEV/PWR	"20 KHz"
(7) MODULATION	"FM 4"
(19) GEN/REC	"GEN"
(35) GEN/LOCK	"LOCK"
(4) AVG PEAK/PEAK	"PEAK"
(38) ANALY DISPR	1 MHz or lower
(51) DISPLAY	Any position EXCEPT TRACK or SWEEP
(18) DUPLEX/SIMPLEX	"SIMPLEX"
(21) LCD	TONE 2 Hz = 10000 FREQ MHz = 835.0200
(28) TONE 1 FM/OFF/AM	"OFF"
(26) TONE 2 FM/OFF/AM	"FM"
(31) TONE 2	Adjust for 8 KHz deviation level on MODULATION METER (1)
(23) SQUELCH	Adjust so that SIG INDICATOR LAMP (57) is illuminated.

6. Connect Channel 1 Probe of Oscilloscope to junction of R6594 and R6553. Connect Channel 2 Probe of Oscilloscope to junction of collector of Q6502 and R6550. (See Figure 9-2).

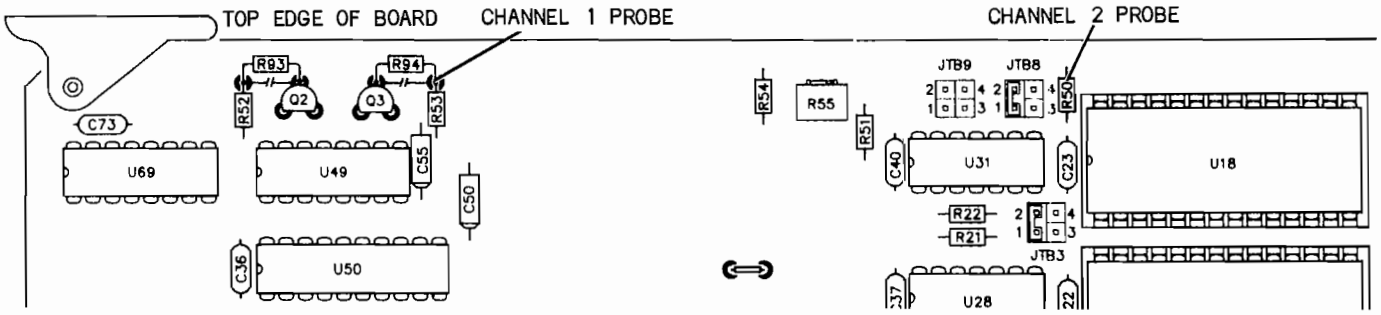


Figure 9-2 Cellular Calibration Test Points (Effective Ser. No. 2771 and on)

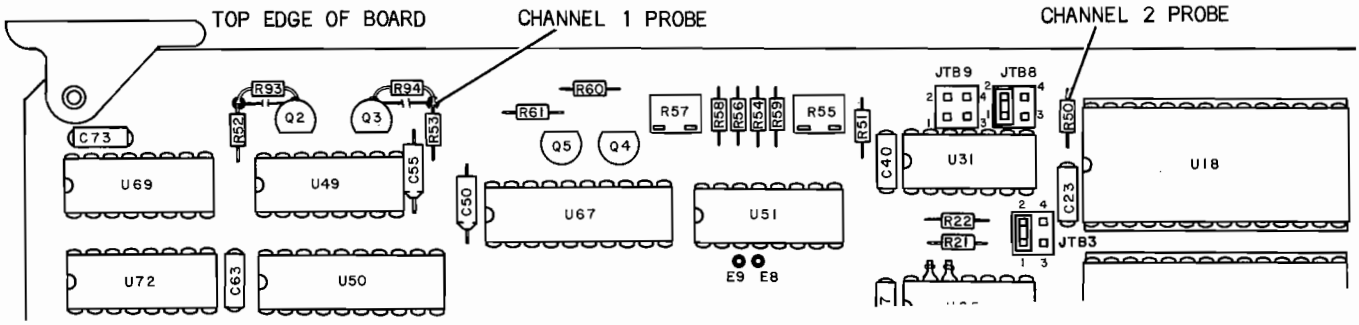


Figure 9-2a Cellular Calibration Test Points (Effective Ser. No. 1194 thru 2770)

7. Trigger on positive edge of Channel 1 signal. Adjust R6555 so that duration of positive pulse on Channel 2 is 75 uS. (See Figure 9-3).

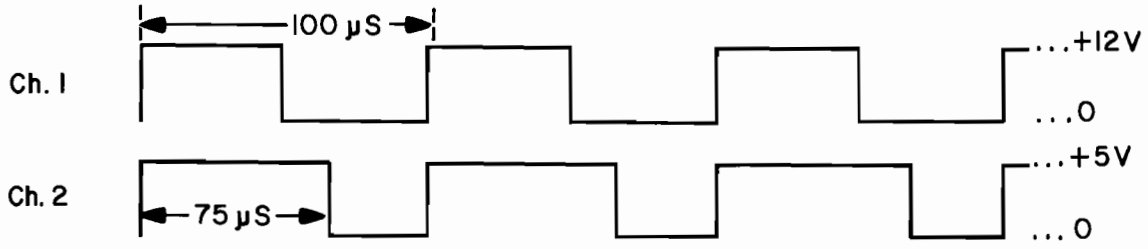


Figure 9-3 Cellular Pulse - Width Calibration

8. Disconnect all test equipment.

9-5 TROUBLESHOOTING

Troubleshooting the Cellular Controller PC Board requires that the technician have a thorough knowledge of cellular theory. For convenience, two test ports (TP1 and TP2) have been provided on the PC Board. Pin numbers and the signals expected are given in Table 9-2. For those technicians having access to a storage Oscilloscope or a Logic Analyzer, Table 9-3 shows the data states to be expected for each of the 50 commands available in the Cellular Menu (refer to the Cellular Operator's Guide for discussion of the commands). Values of the data in Table 9-3 are given in hexadecimal form.

Cellular Controller PC Board		
Test Points	Signal	Notes
TP1-1	+12V power	
-2	1 MHz Clock	
-3	0 to +5V	Tone 2 Square Wave
-4	0 to +5V	Tone 3 Square Wave
-5	0 to +12V	Tone 2 Square Wave
-6	0 to +12V	Tone 3 Square Wave
-7	0 to +5V	Read Enable ($\overline{RD}$)
-8	0 to 5V	Tone 1 Square Wave
-9	0 to +5V (active Low)	6 KHz Bandpass SAT detected
-10	0 to +12V	Tone 1 Square Wave
-11	0 to +12V	Tone 2 Detected
-12	0 to +5V (active Low)	10 KHz Bandpass ST detected
-13	0 to +5V (active Low)	1 KHz Bandpass (initialization only)
-14	0 to +12V	Tone 1 Detected
-15	0 to +12V	Tone 3 Detected
-16	0 to +5V	Write Enable ($\overline{WR}$)
-17	10 Vp-p @ 8 KHz Dev.	Tone 2 Filter Output
-18	0 to +5V	Memory Enable (MEMEN)
-19	0 to +5V, 75 uS pulse	Received data clock
-20	0 to +5V	Manchester encoded data
-21	Variable from 0 to ± 2.5V	Leveled, Filtered AM Data
-22	0 to +5V	Generated Serial Data
-23	Variable from 0 to ± 2.5V	Leveled, Filtered FM Data
-24	10 KHz	Shift Clock for Generated Data
-25	0 to +5V	NRZ
-26	0 to +5V	Either Manchester or NRZ

Table 9-2 Cellular Controller PC Board Test Points

Cellular Controller PC Board		
Test Points	Signal	Notes
TP2-1	0 to +5V	Rectified Tone 3
-2	@ +1.5V is change state	Frequency Selector (Tone 3)
-3	10 Vp-p @ 5 KHz Dev.	Tone 3 Filter Output
-4	@ +1.5V is change state	Frequency Selector (Tone 1)
-5	Not Used	
-6	0 to +5V	Rectified Tone 1
-7	Not Used	
-8	HI-Cellular; LO-future use	Data Rate Select
-9	125 KHz	Tone 3 Filter Clock
-10	0 to +5V	Rectified Tone 2
-11	1 MHz	Tone 2 Filter Clock
-12	0 to +5V	Tone 1 Square Wave Inverted
-13	80 mV per KHz	Buffered FM Demod
-14	@ +1.5V is change state	Frequency Selector (Tone 2)
-15	0 to +5V (High Active)	Data Detect Low Pass Level Output (not used)
-16	10 Vp-p @ 8 KHz Dev.	Tone 1 Filter Output
-17	0 to +5V (High Active)	Data Detect Bandpass Level Output
-18	Variable from 0 to ± 2.5V	Level Controlled Data
-19	+5V power	
-20	1 MHz	Tone 1 Filter Clock
-21	GND	
-22	+12V pulses	Edge Detector
-23	80 mV per KHz	FM Demod from Demod Audio PC Bd
-24	Mobile Under Test RSSI Voltage	Proportional Voltage
-25	-12V power	
-26	@ -2.5 to +2.5V	Level Shifted Data

Table 9-2 (Continued) Cellular Controller PC Board Test Points

Test Command Number	(command, number, ndbs, ndbr)	(OP, AB, RB)
	Z80 to 6809	6809 to Mobile
1	Ø1,ØØ,ØØ	1F,ØØ,ØØ
2	Ø2,ØØ,ØØ	3F,ØØ,ØØ
3	Ø3,ØØ,Ø4	5F,ØØ,Ø3
4	Ø4,ØØ,ØØ	7F,ØØ,ØØ
5	Ø5,Ø1,Ø2	FF,Ø1,Ø1
6	Ø6,ØØ,ØØ	8Ø,ØØ,ØØ
7	Ø7,ØØ,ØØ	81,ØØ,ØØ
8	Ø8,ØØ,ØØ	82,ØØ,ØØ
9	Ø9,Ø2,ØØ	83,Ø2,ØØ
10	ØA,Ø1,ØØ	84,Ø1,ØØ
11	ØB,ØØ,ØØ	85,ØØ,ØØ
12	ØC,ØØ,ØØ	86,ØØ,ØØ
13	ØD,ØØ,ØØ	87,ØØ,ØØ
14	ØE,ØØ,ØØ	88,ØØ,ØØ
15	ØF,ØØ,ØØ	89,ØØ,ØØ
16	1Ø,ØØ,ØØ	8F,ØØ,ØØ
17	11,ØØ,ØØ	9Ø,ØØ,ØØ
18	12,ØØ,Ø1	91,ØØ,ØØ
19	13,ØØ,Ø1	9C,ØØ,ØØ
20	14,ØØ,Ø1	92,ØØ,ØA
21	15,ØØ,Ø1	93,ØØ,Ø5
22	16,ØØ,21	94,ØØ,2Ø
23	17,ØØ,Ø3	95,ØØ,Ø2
24	18,ØØ,Ø5	96,ØØ,Ø4
25	19,Ø2,Ø2	97,Ø2,Ø1
26	1A,OØ,ØØ	98,ØØ,ØØ
27	1B,ØØ,ØØ	99,ØØ,ØØ
28	1C,ØØ,ØØ	9A,ØØ,ØØ
29	1D,ØØ,ØØ	9B,ØØ,ØØ
30	1E,ØØ,ØØ	9D,ØØ,Ø1
31	1F,ØØ,Ø3	9E,ØØ,Ø2
32	2Ø,Ø1,ØØ	AØ,Ø1,ØØ
33	21,ØØ,ØØ	A1,ØØ,ØØ
34	22,Ø6,Ø1	A2,Ø6,ØØ
35	23,ØØ,ØØ	A3,ØØ,ØØ
36	24,ØØ,ØØ	A4,ØØ,ØØ
37	25,ØØ,ØØ	A5,ØØ,ØØ
38	26,ØØ,ØØ	A6,ØØ,ØØ
39	27,ØØ,ØØ	A7,ØØ,ØØ
40	28,ØØ,66	A8,ØØ,65
41	29,65,ØØ	A9,65,ØØ
42	2A,Ø1,ØØ	AA,Ø1,ØØ

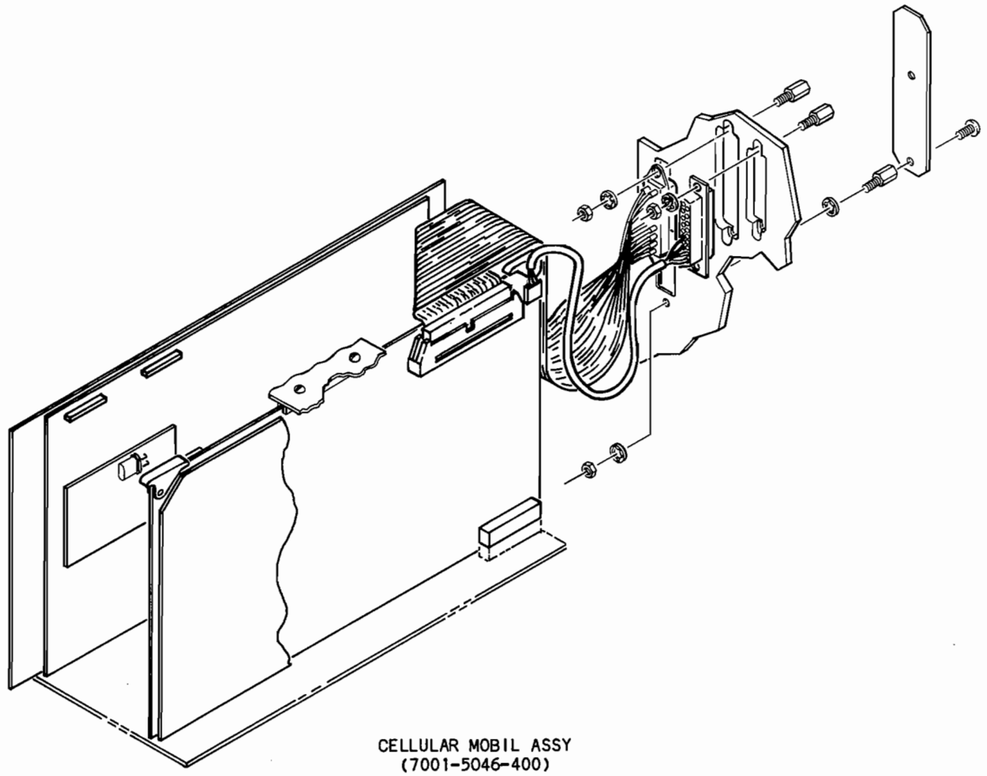
Table 9-3 Data States for Cellular Commands

43	2B,ØØ,ØØ	AB,ØØ,ØØ
44	2C,ndbs,ndbr,(data)	(OP,AB,RB)
The data is dependent upon whether a response is required (ndbr > Ø) and/or whether data is to be sent to the mobile (ndbs > Ø). The (data) for this command is as follows: data #1 - OP for auxiliary command data #2 - AB for auxiliary command (additional bytes) data #3 - RB for auxiliary command (returned bytes) The ndbs is equal to the AB plus 3 (OP,AB,RB). The ndbr is equal to the RB (return all data to the Z80).		
45	initiate - 2D,ØD,ØØ status - 4D,ØØ,Ø1 halt - 6D,ØØ,ØØ	none none none
46	initiate - 2E,ØD,ØØ status - 4E,ØØ,Ø1 halt - 6E,ØØ,ØØ	none none none
47	initiate - 2F,ØD,ØØ status - 4F,ØØ,Ø1 halt - 6F,ØØ,ØØ	none none none
48	3Ø,19,ØØ	none
49	initiate - 31,ØØ,ØØ halt - 51,ØØ,ØØ	none none
50	32,Ø1,ØØ	none

Table 9-3 (Continued) Data States for Cellular Commands

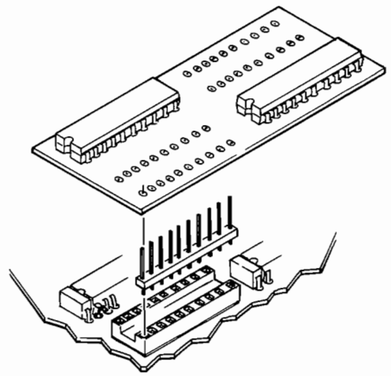
9-6 MECHANICAL ASSEMBLIES/PC BOARDS

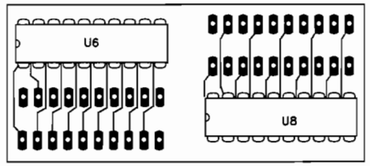
The following mechanical assemblies/PC Boards constitute the cellular option:



CELLULAR MOBIL ASSY
(7001-5046-400)

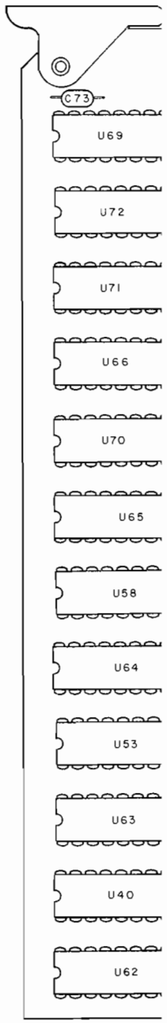
DETAIL **A**

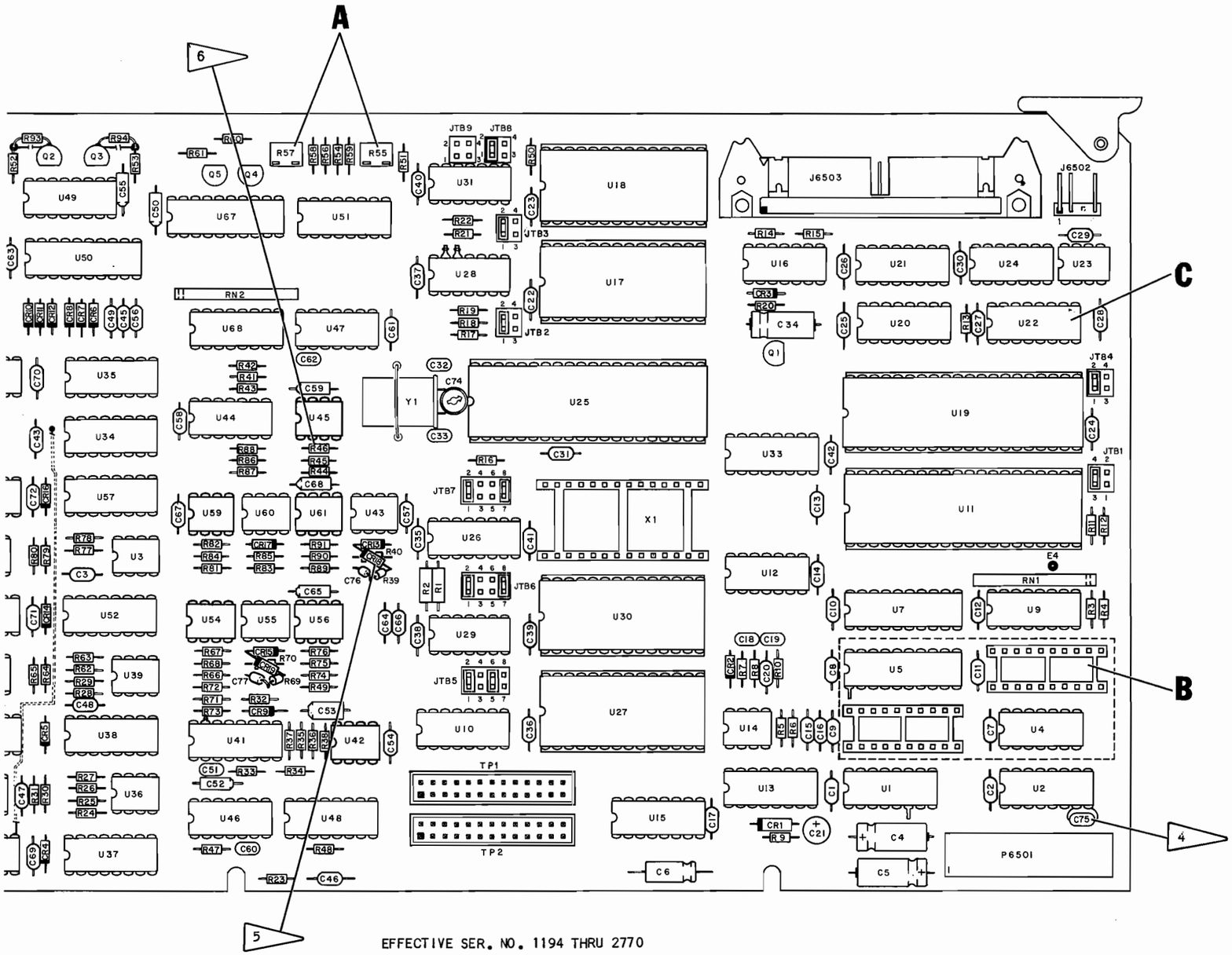




DETAIL **B**

DETAIL **C**



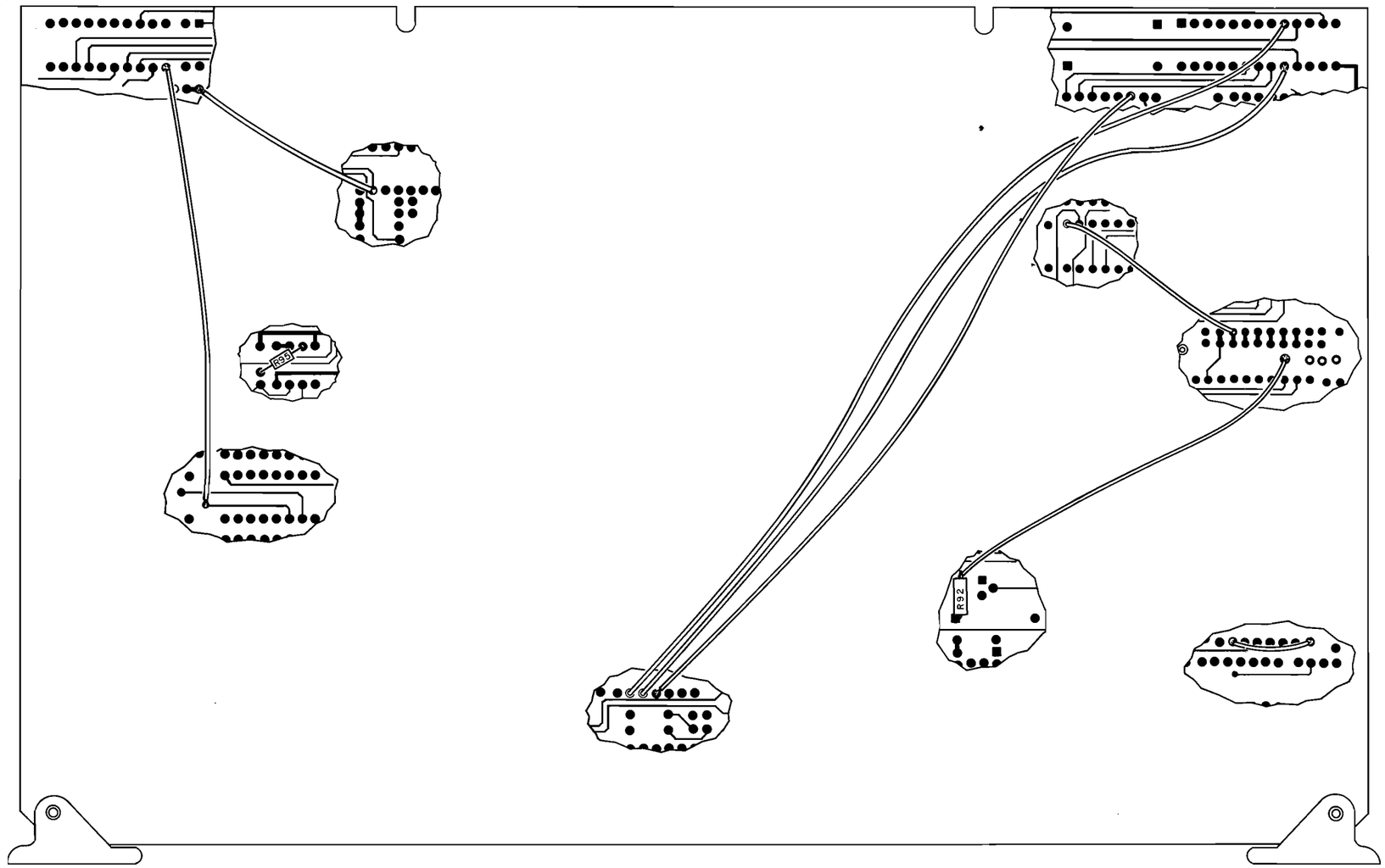


NOTES:

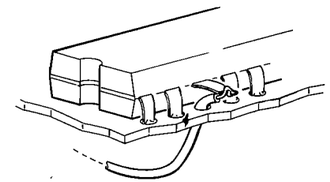
PC BOARD

1. THE REF DES SERIES FOR THE CELLULAR CONTROLLER PC BOARD IS 6500 AND 6600 (E.G., R1 IS R6501 AND R100 IS R6601).
2. DATA PART NO. 7010-5036-600.
3. REF CIRCUIT SCHEMATIC 0000-5016-600.
4. EFFECTIVE SER. NO. 2002, C75 ADDED.
5. EFFECTIVE SER. NO. 2334, CR18, CR19, C76 AND C77 ADDED.
6. R46 SELECTED AT TEST (SAT); NOMINAL 680 OHMS, RANGE 560 THRU 1K OHMS.

Figure 9-4 Cellular Controller PC Board (Sheet 1 of 4)



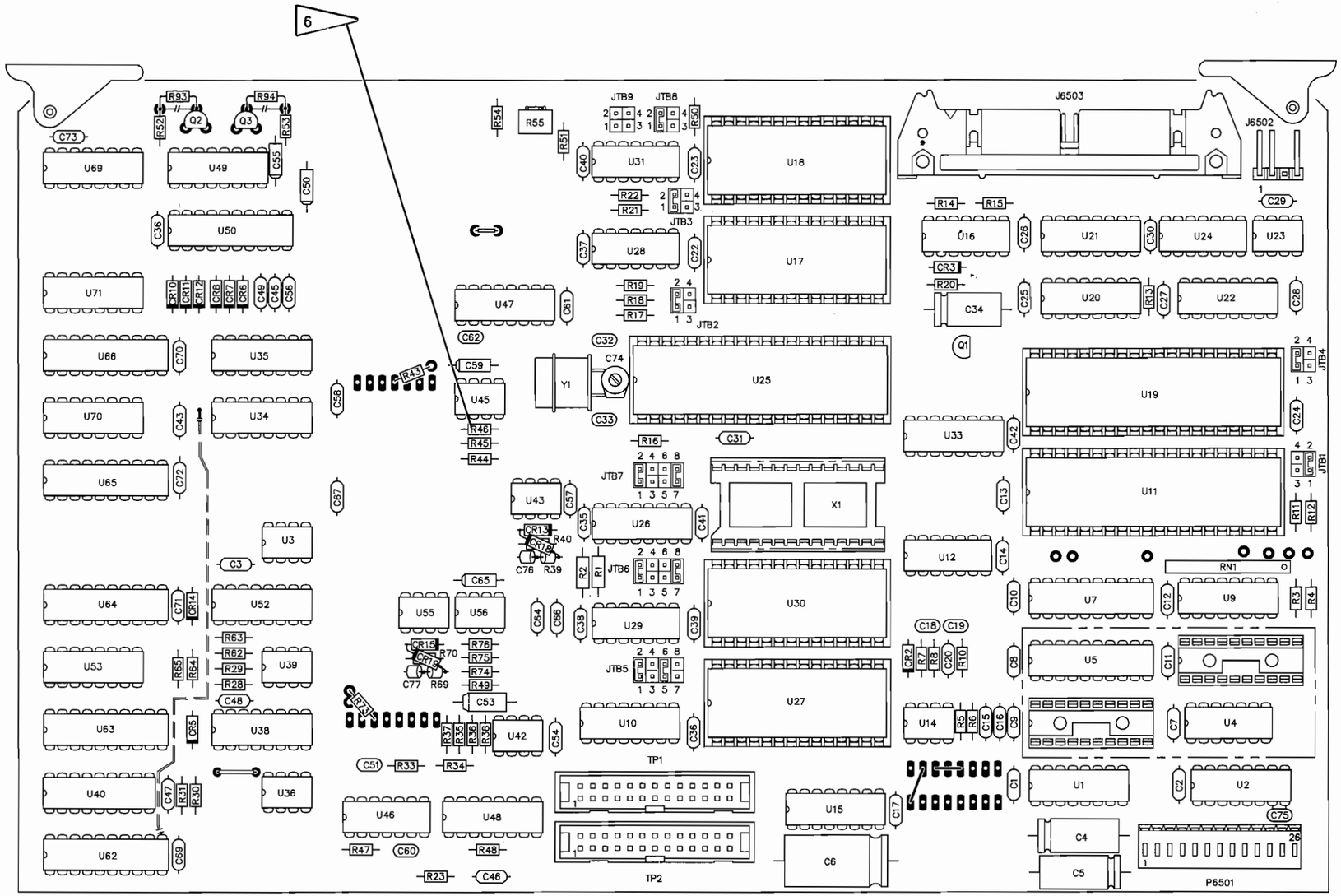
EFFECTIVE SER. NO. 1194 THRU 2770



TYPICAL FOR THRU-BOARD JUMPERS

DETAIL **A**

Figure 9-4 Cellular Controller PC Boar
(Sheet 2 of 4)



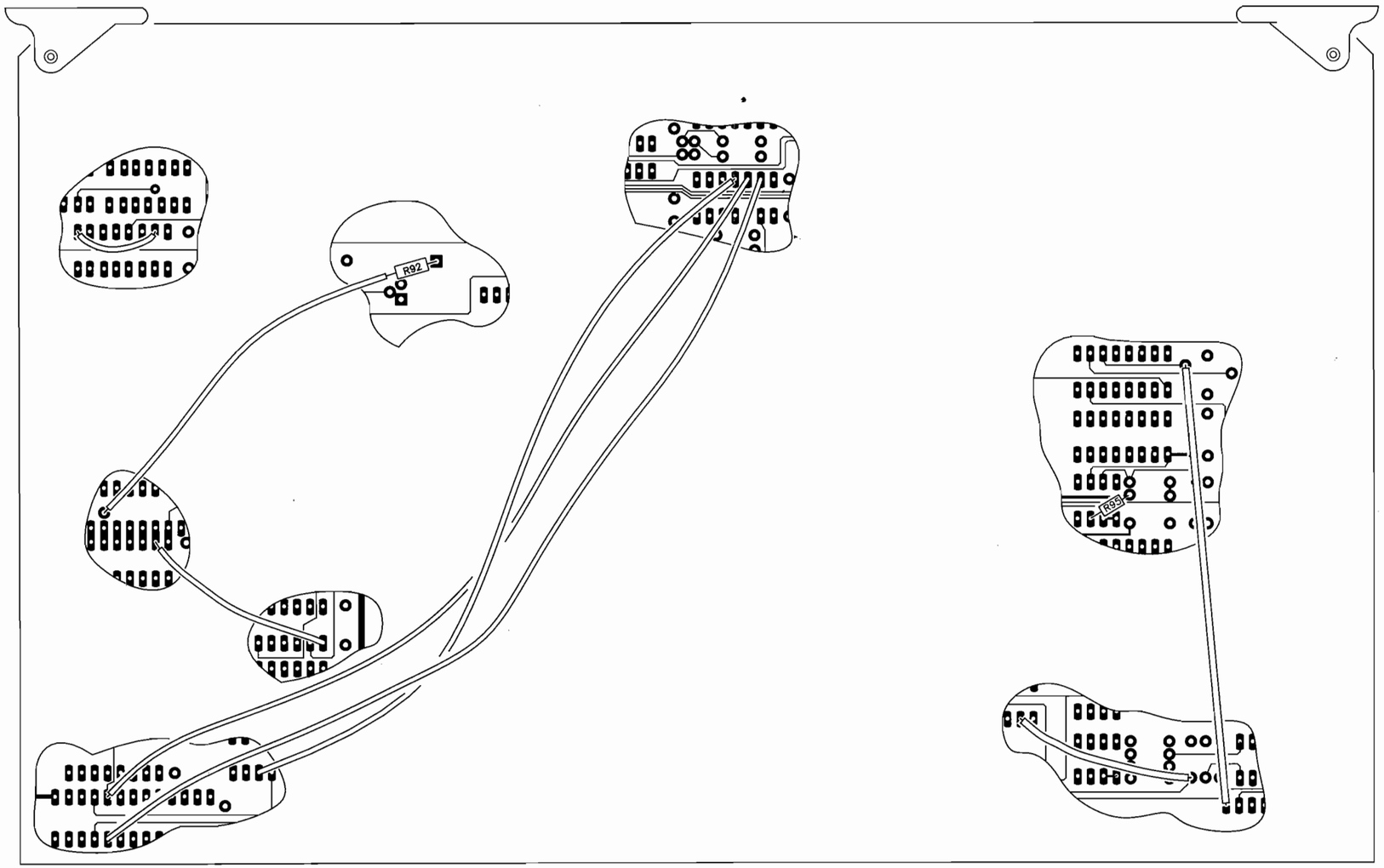
EFFECTIVE SER. NO. 2771 AND ON

NOTES:

PC BOARD

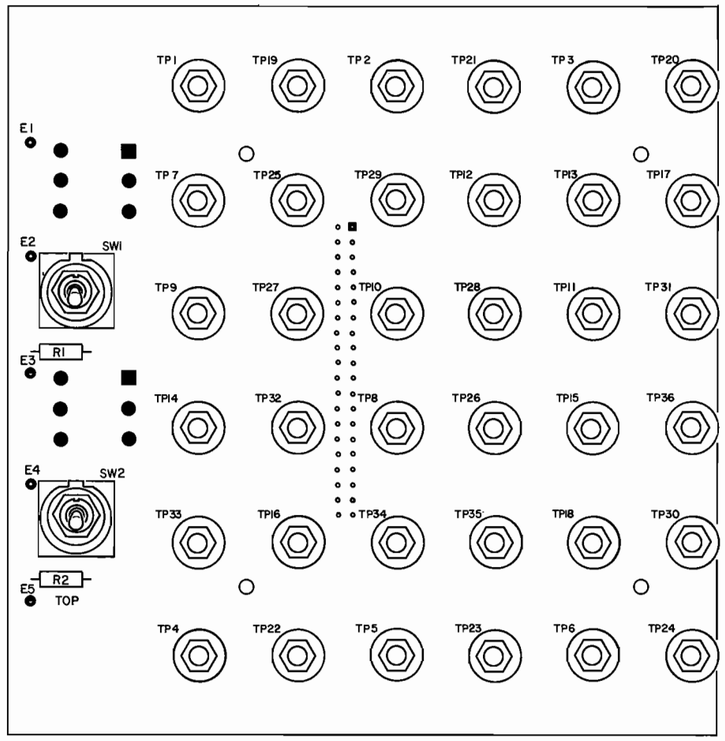
1. THE REF DES SERIES FOR THE CELLULAR CONTROLLER PC BOARD IS 6500 AND 6600 (E.G., R1 IS R6501 AND R100 Is R6601).
2. DATA PART NO. 7010-5036-600.
3. REF CIRCUIT SCHEMATIC 0000-5016-600.
4. NOT USED.
5. NOT USED.
6. R46 SELECTED AT TEST (SAT): NOMINAL 680 OHMS, RANGE 560 THRU 1K OHMS.

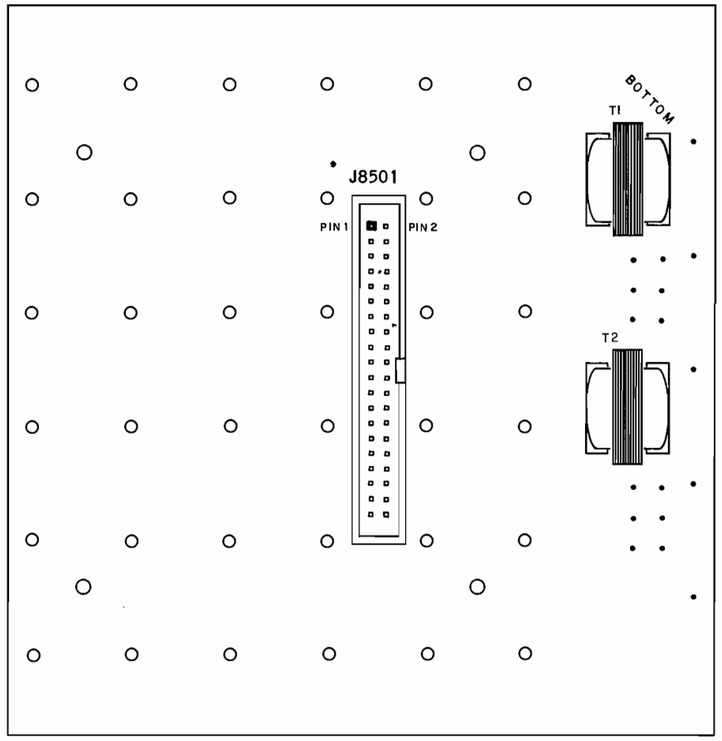
Figure 9-4 Cellular Controller PC Board (Sheet 3 of 4)

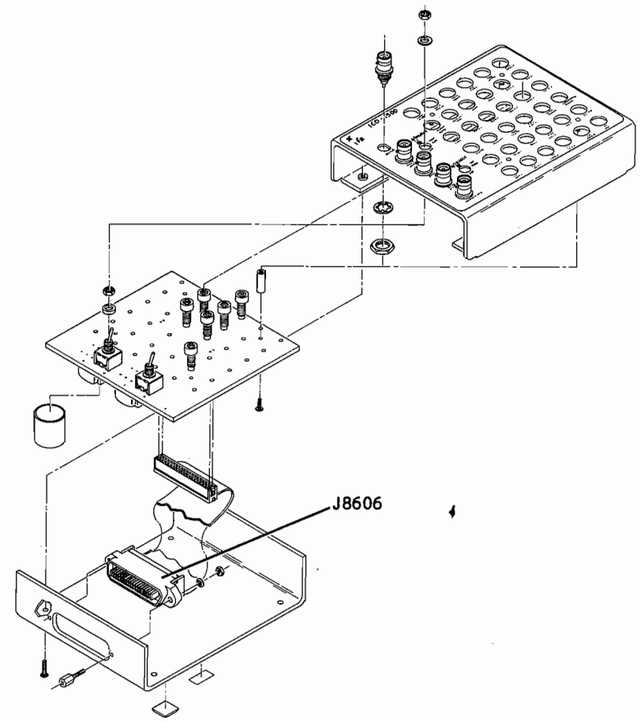


EFFECTIVE SER. NO. 2771 AND ON

Figure 9-4 Cellular Controller PC Board
(Sheet 4 of 4)







NOTES:

MECH ASSY

1. THE REF DES SERIES FOR THE ICD-1500 TEST BOX IS 8600 (I.E., J1 IS J8601).
2. DATA PART NO. 7005-5047-100.
3. REF CIRCUIT SCHEMATIC 0000-5017-100.

PC BOARD

1. THE REF DES SERIES FOR THE ICD-1500 PC BOARD ASSY IS 8500 (I.E., R1 IS R8501).
2. DATA PART NO. 7010-5037-100.
3. REF CIRCUIT SCHEMATIC 0000-5017-100.

Figure 9-5 ICD-1500 Test Box (Part of Option 10)

9-7 SCHEMATICS

The following schematics/interconnects are provided for the cellular option:

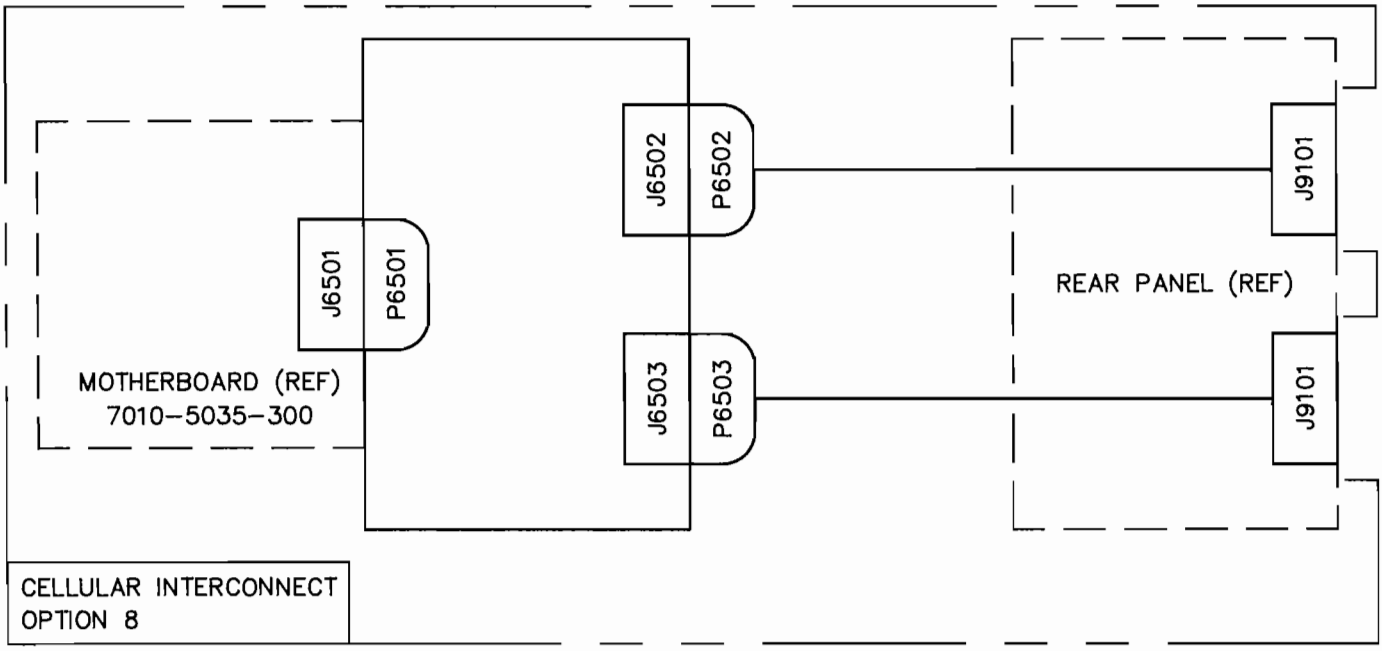
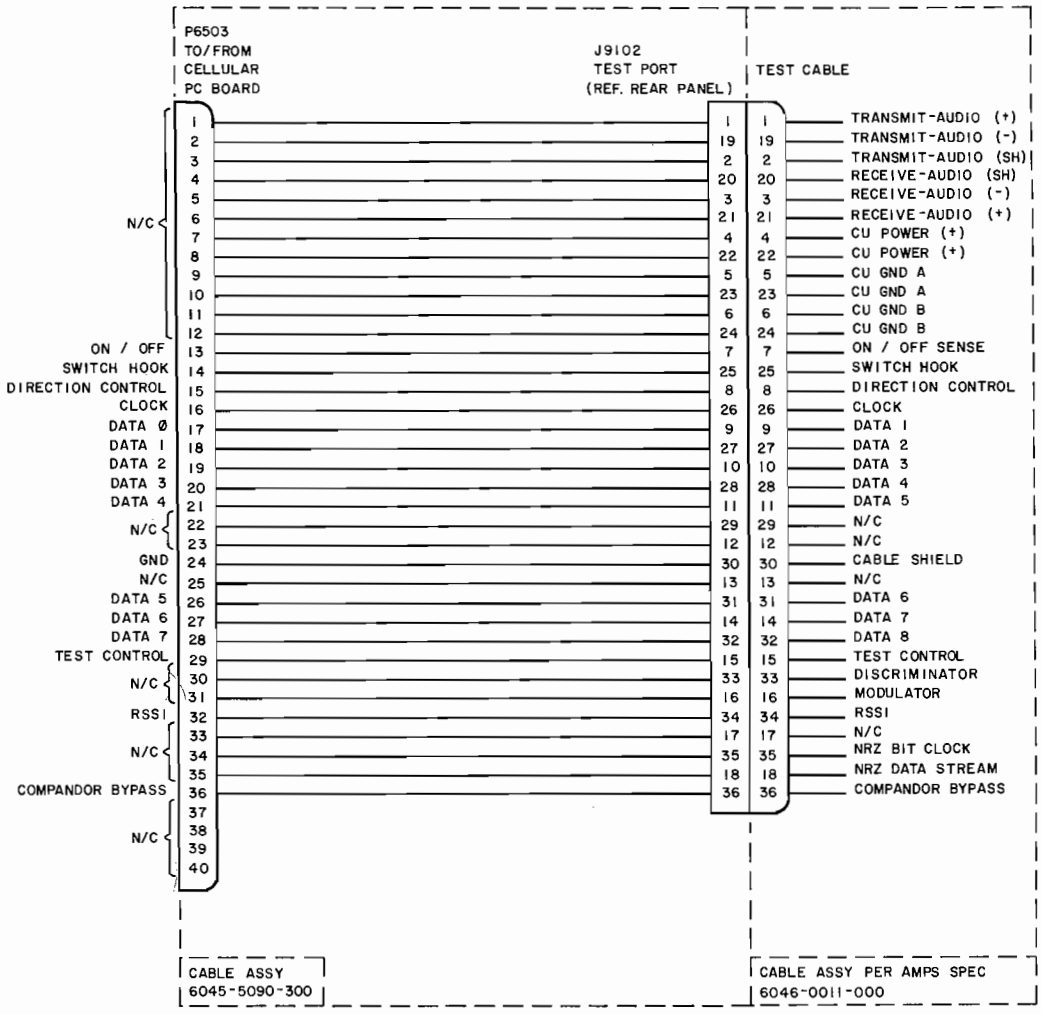


Figure 9-6 Cellular Interconnect (0000-5018-000)



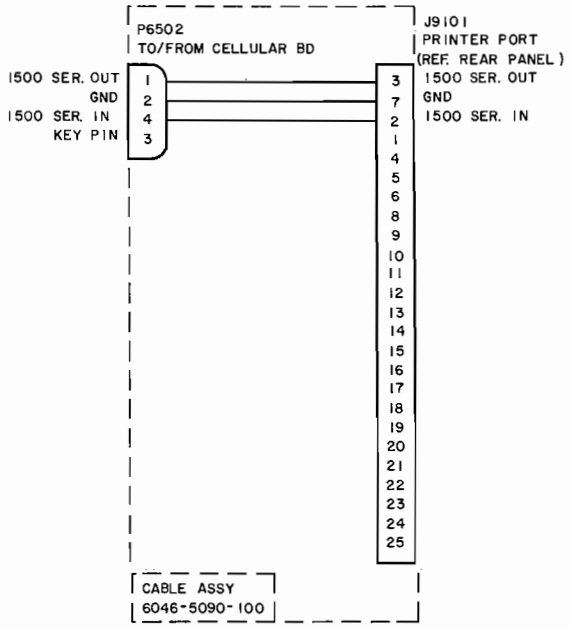
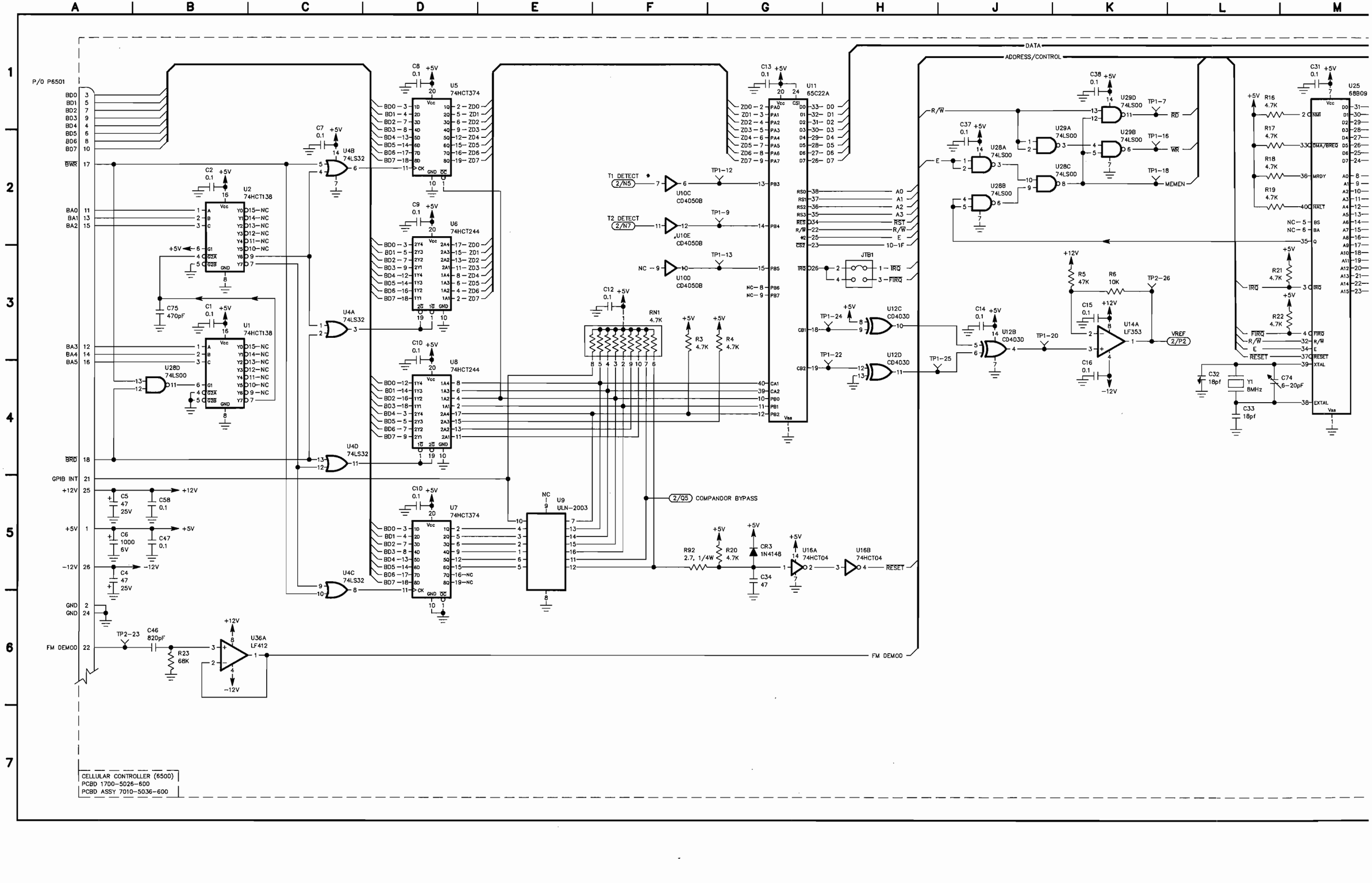


Figure 9-7 Cellular Ribbon Cable Schematic (0000-5018-000)


A
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1
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4
5
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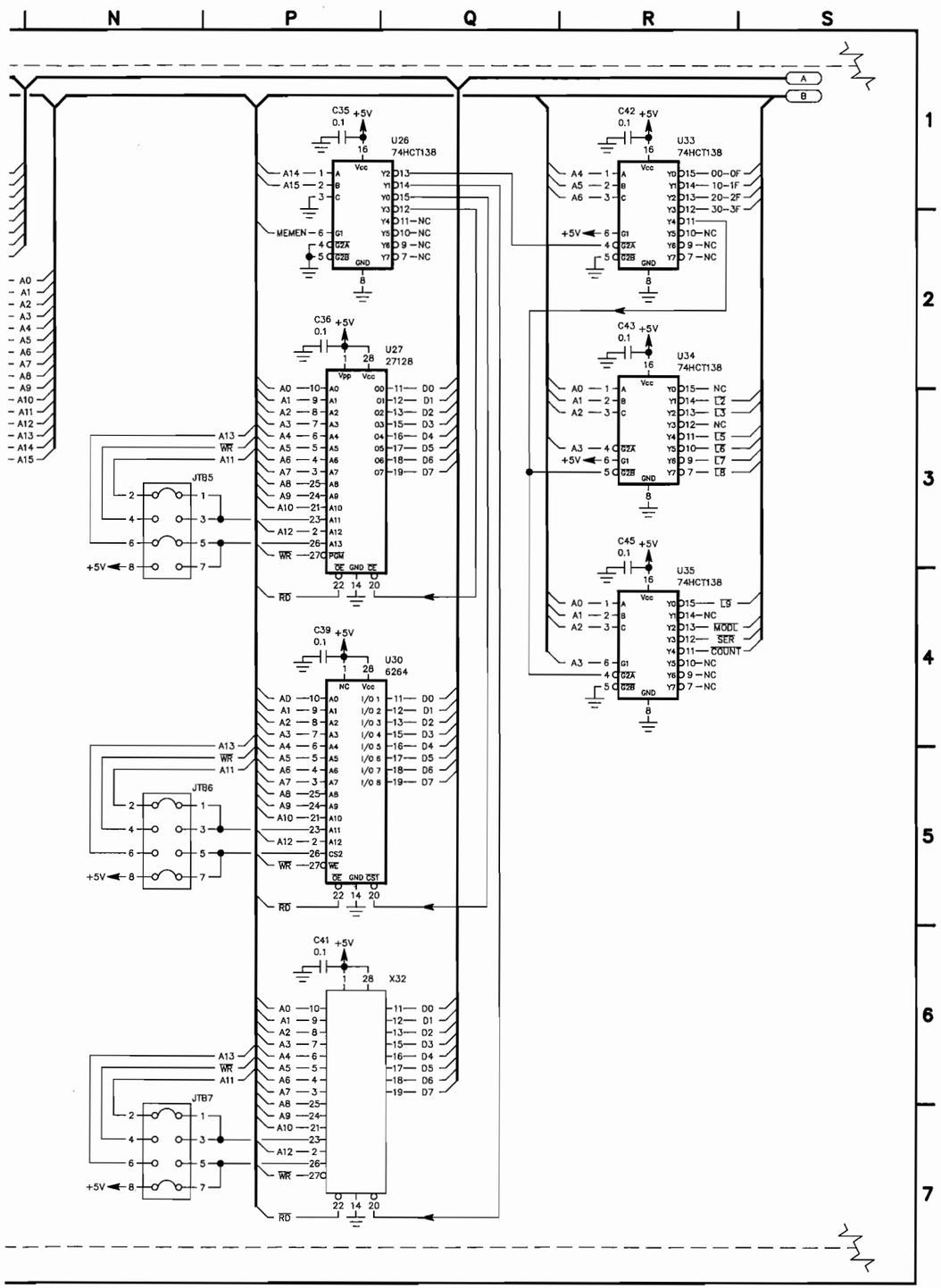
7
P/O P6501
BD0 3
BD1 5
BD2 7
BD3 9
BD4 4
BD5 6
BD6 8
BD7 10
BWR 17
BA0 11
BA1 13
BA2 15
BA3 12
BA4 14
BA5 16
BRD 18
GPIB INT 21
+12V 25
+5V 1
-12V 26
GND 2
GND 24
FM DEMOD 22
U1 74HCT138
U2 74HCT138
U4A 74LS32
U4B 74LS32
U4C 74LS32
U4D 74LS32
U5 74HCT374
U6 74HCT244
U7 74HCT374
U8 74HCT244
U28D 74LS00
C1 0.1
C2 0.1
C7 0.1
C8 0.1
C9 0.1
C10 0.1
C75 470pF
C5 47 25V
C6 1000 6V
C4 47 25V
C58 0.1
C47 0.1
TP2-23
C46 820pF
R23 68K
U36A LF412
+12V
-12V
+5V
RN1 4.7K
R3 4.7K
R4 4.7K
T1 DETECT 2/N5
T2 DETECT 2/N7
U10C CD4050B
U10E CD4050B
U10D CD4050B
TP1-12
TP1-9
TP1-13
NC
U9 ULN-2003
U11 65C22A
ZD0 ZD1 ZD2 ZD3 ZD4 ZD5 ZD6 ZD7
PA0 PA1 PA2 PA3 PA4 PA5 PA6 PA7
PB3 PB4 PB5 PB6 PB7
CA1 CA2 CB1 CB2
RS0 RS1 RS2 RS3 RES R/W Φ2 CS2 IRQ
A0 A1 A2 A3 RST R/W E 1D-1F
JTB1
IRQ
FIRQ
DATA
ADDRESS/CONTROL
R/W
E
U28A 74LS00
U28B 74LS00
U28C 74LS00
U29A 74LS00
U29B 74LS00
U29D 74LS00
TP1-7 RD
TP1-16 WR
TP1-18 MEMEN
C37 0.1
C38 0.1
U12C CD4030
U12D CD4030
U12B CD4030
TP1-24
TP1-22
TP1-25
TP1-20
C14 0.1
R5 47K
R6 10K
TP2-26
U14A LF353
VREF 2/P2
C15 0.1
C16 0.1
C31 0.1
U25 68B09
R16 4.7K
R17 4.7K
R18 4.7K
R19 4.7K
R21 4.7K
R22 4.7K
NMI
DMA/BREQ
MRDY
HALT
BS
BA
Q
IRQ
FIRQ
R/W
E
RESET
XTAL
EXTAL
C32 18pf
Y1 8MHz
C74 6-20pF
C33 18pf
2/Q5 COMPANDOR BYPASS
R92 2.7, 1/4W
R20 4.7K
CR3 1N4148
C34 47
U16A 74HCT04
U16B 74HCT04
RESET
CELLULAR CONTROLLER (6500)
PCBD 1700-5026-600
PCBD ASSY 7010-5036-600

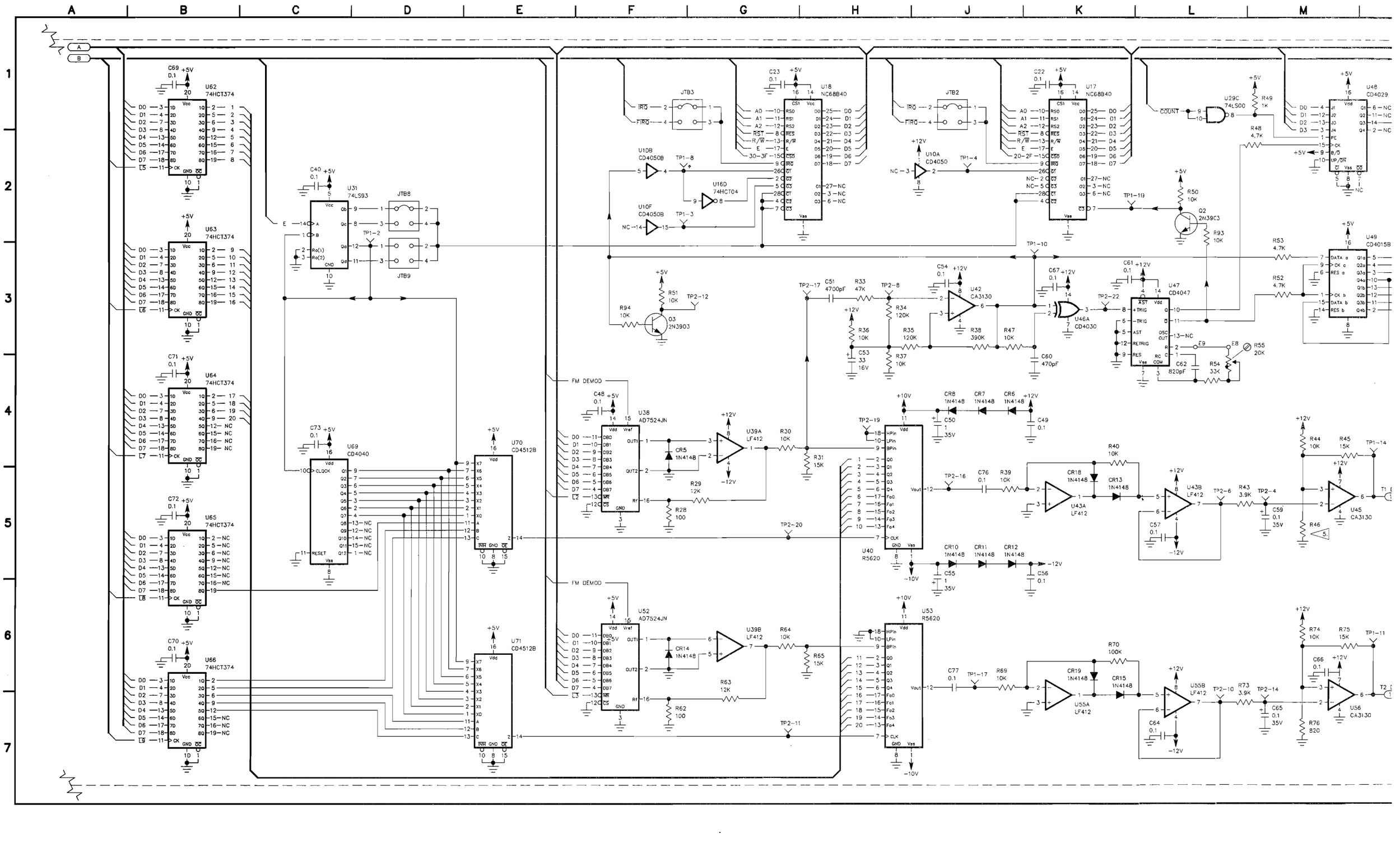


NOTES:
(UNLESS OTHERWISE NOTED)

1. ALL REFERENCE NUMBERS CARRY AN ASSIGNED DESIGNATOR SERIES.
   THIS SCHEMATIC CARRIES SERIES: 6500.
2. ALL RESISTORS ARE 1/8 W, 5% TOLERANCE.
3. ALL RESISTANCE IS EXPRESSED IN OHMS.
4. ALL CAPACITANCE IS EXPRESSED IN MICROFARADS.
5. R46 IS SELECT AT TEST (S.A.T.)
   NOMINAL VALUE = 680 OHMS.
   RANGE = 1K.
6. IC GATES NOT USED:

   U3B, U16C, U24B, U24C, U24D, U36B, U46B, U46C, U46D

Figure 9-8 Cellular Controller Circuit Schematic (Sheet 1 of 2)
0000-5016-600-C3


A
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J
K
L
M
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6
7
U62 74HCT374
U63 74HCT374
U64 74HCT374
U65 74HCT374
U66 74HCT374
U31 74LS93
U69 CD4040
U70 CD4512B
U71 CD4512B
JTB3
JTB2
JTB8
JTB9
U18 NC68B40
U17 NC68B40
U10A CD4050
U10B CD4050B
U10F CD4050B
U160 74HCT04
U29C 74LS00
U48 CD4029
U49 CD4015B
U47 CD4047
U46A CD4030
U42 CA3130
U45 CA3130
U56 CA3130
U38 AD7524JN
U52 AD7524JN
U39A LF412
U39B LF412
U43A LF412
U43B LF412
U55A LF412
U55B LF412
U40 R5620
U53 R5620
Q2 2N3903
Q3 2N3903
TP1-2
TP1-3
TP1-4
TP1-8
TP1-10
TP1-11
TP1-14
TP1-19
TP2-6
TP2-8
TP2-10
TP2-11
TP2-12
TP2-14
TP2-16
TP2-17
TP2-19
TP2-20
TP2-22
FM DEMOD
FM DEMOD
COUNT
+5V
+12V
-12V
+10V
-10V
R28 100
R29 12K
R30 10K
R31 15K
R33 47K
R34 120K
R35 120K
R36 10K
R37 10K
R38 390K
R40 10K
R43 3.9K
R44 10K
R45 15K
R46 5.
R47 10K
R48 4.7K
R49 1K
R50 10K
R51 10K
R52 4.7K
R53 4.7K
R54 33K
R55 20K
R62 100
R63 12K
R64 10K
R65 15K
R69 10K
R70 100K
R73 3.9K
R74 10K
R75 15K
R76 820
R93 10K
R94 10K
C48 0.1
C49 0.1
C50 1 35V
C51 4700pF
C53 33 16V
C54 0.1
C55 1 35V
C56 0.1
C57 0.1
C59 0.1 35V
C60 470pF
C61 0.1
C62 820pF
C64 0.1
C65 0.1 35V
C66 0.1
C67 0.1
C69 0.1
C70 0.1
C71 0.1
C72 0.1
C73 0.1
C76 0.1
C77 0.1
CR5 1N4148
CR6 1N4148
CR7 1N4148
CR8 1N4148
CR10 1N4148
CR11 1N4148
CR12 1N4148
CR13 1N4148
CR14 1N4148
CR15 1N4148
CR18 1N4148
CR19 1N4148
E8
E9
NC

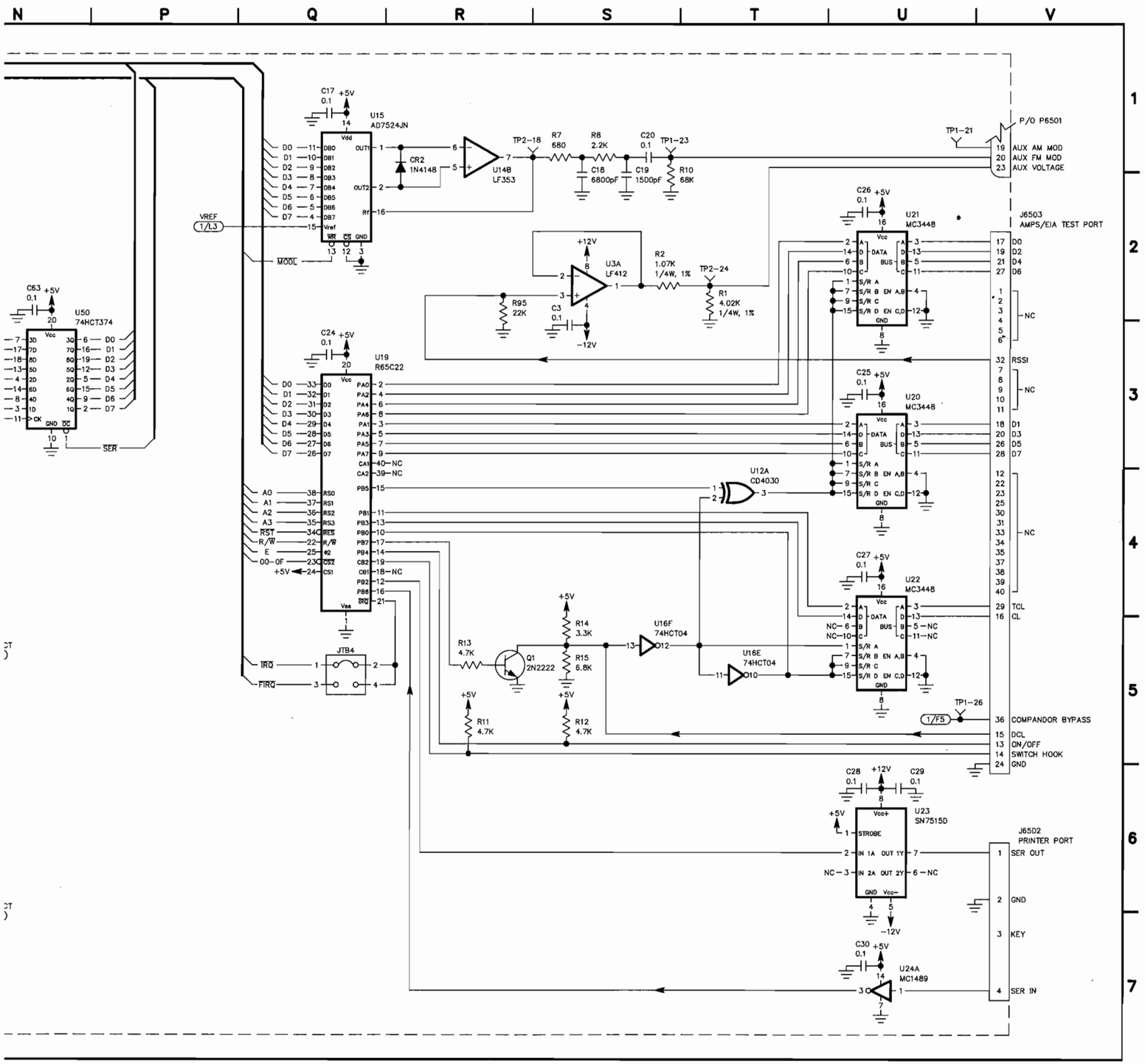
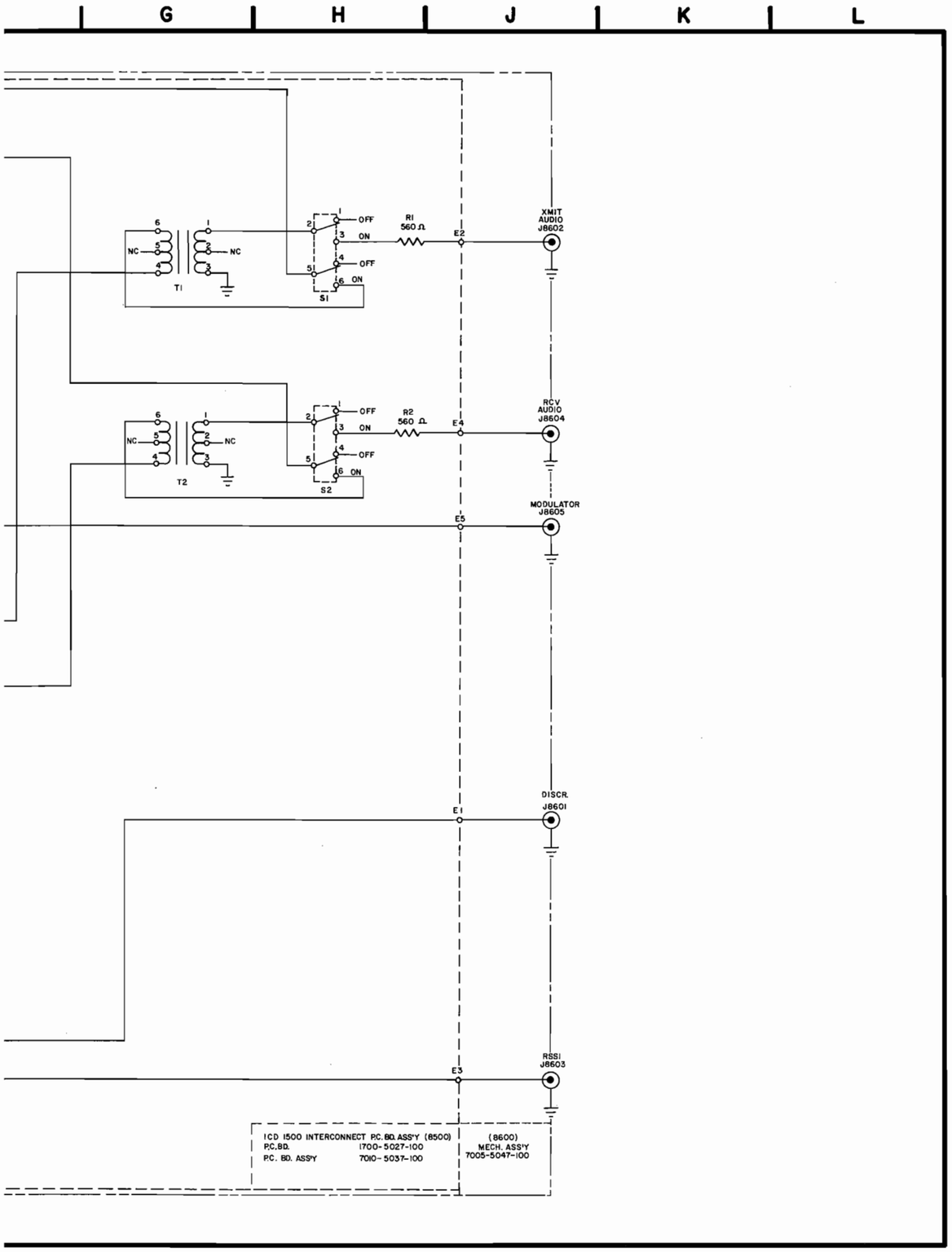


Figure 9-8 Cellular Controller Circuit Schematic (Sheet 2 of 2) 0000-5016-600-C3

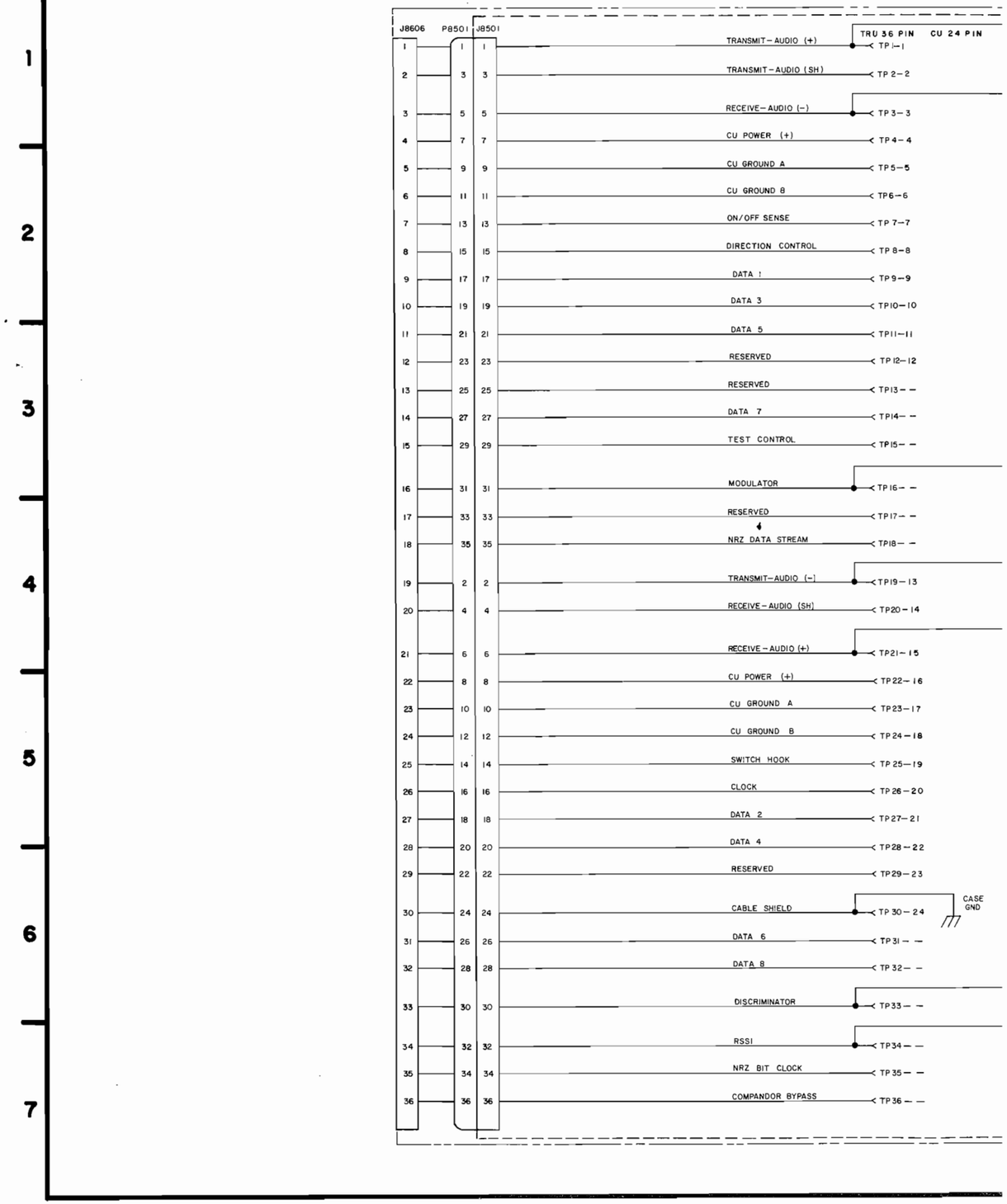


NOTES:

1. ALL REF NOS CARRY AN ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES 8500 AND 8600.
2. ALL RESISTORS ARE 10%, 1/4 W.
3. LAST REF NO USED:

J8501	J8606
T8502	SW8502
E8505	R8502
P8501	TP8537

Figure 9-9 ICD-1500 Schematic
0000-5017-100-B


A
B
C
D
E
1
2
3
4
5
6
7
J8606
P8501
J8501
TRU 36 PIN
CU 24 PIN
TRANSMIT – AUDIO (+)
TP1 – 1
TRANSMIT – AUDIO (SH)
TP2 – 2
RECEIVE – AUDIO (–)
TP3 – 3
CU POWER (+)
TP4 – 4
CU GROUND A
TP5 – 5
CU GROUND B
TP6 – 6
ON/OFF SENSE
TP7 – 7
DIRECTION CONTROL
TP8 – 8
DATA 1
TP9 – 9
DATA 3
TP10 – 10
DATA 5
TP11 – 11
RESERVED
TP12 – 12
RESERVED
TP13 – –
DATA 7
TP14 – –
TEST CONTROL
TP15 – –
MODULATOR
TP16 – –
RESERVED
TP17 – –
NRZ DATA STREAM
TP18 – –
TRANSMIT – AUDIO (–)
TP19 – 13
RECEIVE – AUDIO (SH)
TP20 – 14
RECEIVE – AUDIO (+)
TP21 – 15
CU POWER (+)
TP22 – 16
CU GROUND A
TP23 – 17
CU GROUND B
TP24 – 18
SWITCH HOOK
TP25 – 19
CLOCK
TP26 – 20
DATA 2
TP27 – 21
DATA 4
TP28 – 22
RESERVED
TP29 – 23
CABLE SHIELD
TP30 – 24
CASE GND
DATA 6
TP31 – –
DATA 8
TP32 – –
DISCRIMINATOR
TP33 – –
RSSI
TP34 – –
NRZ BIT CLOCK
TP35 – –
COMPANDOR BYPASS
TP36 – –

APPENDICES

APPENDIX A : FM/AM-1500 SPECIFICATIONS

A-1 RF SIGNAL GENERATOR

Frequency Range:	100 kHz to 999.9999 MHz in 100 Hz increments.
Frequency Accuracy	(See TCXO Master Oscillator)
Residual FM:	50 Hz RMS (typical 30 Hz RMS) (Post detection 50-300 Hz)
RF Output Power:	0 dBm to -128 dBm continuously adjustable into 50Ω. (No range changing)
Accuracy:	±2 dB, -10 to -80 dBm ±2.5 dB, -80 to -128 dBm (-80 to -120 on IEEE version)
Attenuator Dial:	One continuous dial with μV and dBm.
Modulation:	FM: 2 Hz to 30 kHz rate at 0 to ±25 kHz deviation. For external inputs DC to 30 kHz rate. (DC, if generator lock control is in the variable position). Flat to ±2 dB DC to 30 kHz 6 Vp-p ±2 Vp-p produce ±15 kHz deviation AM: 10 Hz to 5 kHz rate at 0-90% 6 kHz to 30 kHz rate at 0-30% 3 Vp-p ±1 Vp-p produces 90% modulation External Mod impedance 600
Freq. Shift with Modulation:	When the generator is in the "lock" position, the center frequency is phase-locked to the system clock.

NOTE

FM1, FM2, FM3 and FM4 are all FM modulation. SSB, AM1, and AM2 are AM modulation. SSB has no function other than AM in the generator mode.

A-1 RF SIGNAL GENERATOR (Cont'd)

Modulation Distortion:	The FM modulation distortion plus noise at ±25 kHz deviation is less than 2% from 200 Hz to 20 kHz.
Generator Freq. Control:	When in the "locked" position, the generator is phase-locked to the master clock. When switched off from the "locked" position, the generator may be varied ±10 kHz. The FM modulation input is DC coupled for this unlocked function. (Internal or external modulation.)
Microphone Input:	Generator can be switched on by an external microphone. It has internal preamp with adjustable level.
SSB Noise:	90 dBc/Hz at ±20 kHz from carrier.
Deviation Accuracy of Processor controlled audio levels:	±5% from 20 Hz to 5 kHz and ±10% from 5 kHz to 20 kHz.
Generator Spurious:	
Harmonics:	> -25 dBc
Non Harmonics:	> -40 dBc
Typically:	> -60 dBc
In-Band, typically:	> -70 dBc

A-2 DUPLEX GENERATOR

Freq Range:	±49.99 MHz from receive frequency (as indicated on front panel (LCD) in 10 kHz increments.
Freq Accuracy:	See TXCO Master Oscillator.
Output Level:	
DUPLEX Connector:	0 dBm to -128 dBm continuously adjustable into 50Ω. (No range changing.)

TRANS Connector:	40 dB (±3 dB) below Attenuator Setting for Attenuator Settings from -10 to -80 dBm. 40 dB (±3.5 dB) below Attenuator Setting for Attenuator Settings from -80 to -128 dBm.

A-3 RECEIVER/MONITOR

Frequency Range:	300 kHz to 999.9999 MHz.
Resolution:	100 Hz
10 dB Sinad Sensitivity (typical):	2 µV (1 MHz to 1 GHz). Sensitivity reduced below 1 MHz (for 15 kHz RF bandwidth and 8 kHz post detection bandwidth)
Selectivity: (3 dB):	6 kHz; SSB and AM_1, 15 kHz; AM_2 and FM_1, 200 kHz, FM_2, FM_3 and FM_4 FM_1 and FM_2 has post demodulation bandwidth of 8 kHz. FM_3 has a post demodulation bandwidth of 20 kHz. FM_4 has a post demodulation bandwidth of 80 kHz. FM_1 has a demodulation flatness of ±2 dB referenced to 1 kHz from 10 Hz to 20 kHz. AM_1 and SSB have an RF bandwidth of 6 kHz and post detection bandwidth of 8 kHz. AM_2 has an RF bandwidth of 15 kHz and a post detection bandwidth of 8 kHz.
Antenna Attenuator:	Selectable 0, -20 dB, and -40 dB (±2 dB each)
Quieting:	Deviation measurements can be made down to 0.1 kHz in post detection bandwidth of 8 kHz.
Adjacent Channel Rejection:	>25 dB at ±25 kHz (when in 15 kHz RF bandwidth) >40 dB at ±50 kHz (when in 15 kHz RF bandwidth)
Beat Frequency Oscillator (BFO):	Fixed at center frequency.
Demodulation Output Level: (600Ω Load)	AM: 100% = 0.5 Vp-p nominal (selectable by modulation switch) FM: ±10 kHz deviation = 1.0 Vp-p nominal

A-3 RECEIVER/MONITOR (Cont'd)

Demodulation Output Level Impedance:	600 ohms
Receiver Antenna Input Protection:	0.25 Watts maximum level without damage
FM Demodulation Noise + Distortion:	Less than 2% at ±25 kHz deviation for modulation frequencies from 200 Hz to 20 kHz with a receiver input level of -50 dBm. (RF bandwidth = 200 kHz, post detection bandwidth = 80 kHz)
Image Rejection:	+ 1.4 MHz, 50 dB + 21.4 MHz, 50 dB + 238.6 MHz, 50 dB + 2500 MHz ±10 MHz, 5 dB
Deviation Monitor Meter: (max peak either polarity)	Scales: 2 kHz, 6 kHz, 20 kHz, 60 kHz Accuracy ±5% full scale for modulation frequencies of 30 Hz to 10 kHz at a signal level of -50 dBm.
AM Modulation Digital Display: (max peak, positive or negative)	0.1% resolution on 20% and 60% ranges, 1% on 200% and 600% ranges. Accuracy 5% reading ±20 counts at received signal of -50 dBm for modulation frequencies 300 Hz to 10 kHz. (10% to 90% depth)
Digital Deviation Display (CRT):	Range is 0.00 to 60.0 kHz Accuracy is ±3% at these two points: 1. 6 kHz rate at ±2 kHz with 8 kHz post detection BW. 2. 10 kHz rate at ±8 kHz with 20 kHz post detection BW.
AM Modulation Monitor Meter:	Scales 0-20%, 0-60%, 0-200% Accuracy ±7% of reading, ±5% full scale.

A-4 SPECTRUM ANALYZER

Inputs:	Transmitter:	Transmitter under test when power exceeds 0.1 watt. A 100 watt signal produces a top graticule reading. (marked -30 dBm)
	Antenna Jack:	The log scale is marked for dBm for this input when the antenna attenuator is set for "0". The signal can be attenuated by 20 dB or 40 dB by the antenna attenuator switch.
Log Scale:		Within ±2 dB linearity from -30 dBm to -90 dBm indication. Switchable between 1 dB/DIV and 10 dB/DIV.
Dynamic Range:		70 dB, additional 40 dB selectable by input attenuator.

Modes:

Full Scan:	1 MHz to 1000 MHz; 650 kHz bandwidth
10 MHz/DIV:	Center frequency as selected; 650 kHz bandwidth
5 MHz/DIV:	Center frequency as selected; 650 kHz bandwidth
2 MHz/DIV:	Center frequency as selected; 650 kHz bandwidth
*1 MHz/DIV:	Center frequency as selected; 30 kHz bandwidth
*0.5 MHz/DIV:	Center frequency as selected; 30 kHz bandwidth
*0.2 MHz/DIV:	Center frequency as selected; 30 kHz bandwidth
*0.1 MHz/DIV:	Center frequency as selected; 30 kHz bandwidth
*20 kHz/DIV:	Center frequency as selected; 3 kHz bandwidth
*10 kHz/DIV:	Center frequency as selected; 3 kHz bandwidth
*2 kHz/DIV:	Center frequency as selected; 300 Hz bandwidth
*1 kHz/DIV:	Center frequency as selected; 300 Hz bandwidth

* The receiver is fixed on the center frequency for monitoring while the analyzer scans as specified. On wider scans, the receiver and monitor portion are not usable.

A-5 TRACKING GENERATOR

Frequency Range:	1.0 MHz to 1000 MHz as selected by the frequency control.
Output Level:	Same as RF generator; 0 dBm to -128 dBm.
Sweep Mode:	The oscilloscope is switchable to external vertical input when in the tracking generate mode.

A-6 OSCILLOSCOPE

Display Size:	2" x 2½"
Vertical Bandwidth:	DC to 1 MHz (at 3 dB bandwidth)
External Vertical Input Ranges:	10 mV, 100 mV, 1 V, 10 V per division
Horizontal Sweep Rate:	10 mSec, 1 mSec, 100 μSec, 10 μSec per division

A-7 AUDIO GENERATORS

Operating Modes:	Internal:	Variable frequency generators, one or both.
	External plus Internal:	Any external tone(s) plus either or both internal tones simultaneously.
Frequency Range:	Variable from 2 Hz to 30 kHz.	
Accuracy:	0.01%	
Resolution:	0.1 Hz; 2 Hz to 9999.9 Hz; 1 Hz, 10.000 kHz to 30 kHz.	
Output Level:	Variable from 0 to 2.5 VRMS minimum either tone into 150Ω.	
Distortion:	<2% (10 Hz to 100 Hz) <0.7% typical 100 Hz to 30 kHz Some frequencies have a measured distortion of less than 1.5% as measured on a typical null type distortion analyzer.	

A-7 AUDIO GENERATORS (Cont'd)

Output Distribution:	Each tone selectable OFF or into either AM or FM modulator when not under processor sequence control. Each tone level variable through "Tones Out" jack regardless of selection of "FM", "AM" or "OFF" by the manual switches.
Speaker:	Selectable from receiver or same signal as "Tone Out" jack.

A-8 FREQUENCY ERROR METER MEASUREMENT CAPABILITY

RF Signals

Sensitivity:	Typically 1.5 µV above 1 MHz (sensitivity is reduced below 1 MHz)
Ranges:	±30 Hz, ±100 Hz, ±300 Hz, ±1 kHz, ±3 kHz, ±10 kHz
Resolution:	±1 Hz on the ±30 Hz and ±100 Hz ranges

Demodulated Audio Signals

Ranges:	±3 Hz, ±30 Hz, ±300 Hz as referenced to frequency of Tone Generator #1.
Resolution:	±0.1 Hz on ±3 Hz scale
Frequency Range:	20 Hz to 10 kHz

A-9 DEMODULATED AUDIO FREQUENCY COUNTER

Range:	10 Hz to 20 kHz
Resolution:	1 Hz
Accuracy:	±2 counts

A-10 INTERNAL SINAD METER

Input:	0.5 to 10 VRMS
Frequency:	1 kHz
Range:	0 to 20 dB
Accuracy:	±1.5 dB at 12 dB reading

A-11 POWER MONITOR

Frequency Range:	1 MHz to 1000.00 MHz (wideband detector circuit)
Power Ranges:	0 to 15 and 0 to 150 Watts
Accuracy:	1 to 600 MHz, ±7% of reading ±3% of full scale.
	600 to 1000 MHz ±17% of reading ±3% of full scale
	821 MHz to 896 MHz ±7% reading, ±3% of full scale
Input Power:	50 watts continuous 150 watts until "over temp" lamp illuminates

Changeover from generate to monitor mode occurs at nominally 100 mW input level to the TRANS/-40 dB DUPLEX Connector.

A-12 TXCO MASTER OSCILLATOR

Accuracy:	5×10^{-7} = 0.00005% (typically 2×10^{-7}). Greater accuracy is attainable with front panel adjustment.
Aging Stability:	2 to 3 PPM during first year ... 1 PPM per year thereafter.
EXT. Clock:	BNC Connector for EXT 10 MHz STD.
Optional Oven:	
Accuracy:	0.05 PPM (0-50°C)
Aging:	0.25 PPM per year

A-13 PHYSICAL CHARACTERISTICS

Dimensions:	12.5" wide, 9" high, 19.5" deep (31.8 cm W, 22.9 cm H, 49.5 cm D)
Weight:	46 lbs. (20.9 kg)
Temperature Range:	0° to 50° C

A-14 POWER

Conveniently portable. Self-contained battery automatically recharges when AC line is connected. Operates on 106 to 266 VAC without switching, 50-400 Hz, 85 watts, or 11 to 18 VDC. Typical DC currents 6.0 A at 12 V.

APPENDIX B : PINOUT/CONTACT ASSIGNMENTS FOR EXTERNAL ACCESSORY AND MICROPHONE CONNECTORS

B-1 PINOUT TABLE FOR EXTERNAL ACCESSORY CONNECTORS

The table below provides pin assignments for the EXT ACC Connector located on the front panel of the FM/AM-1500. This connector provides power and signal sources for external accessory equipment used with the FM/AM-1500.

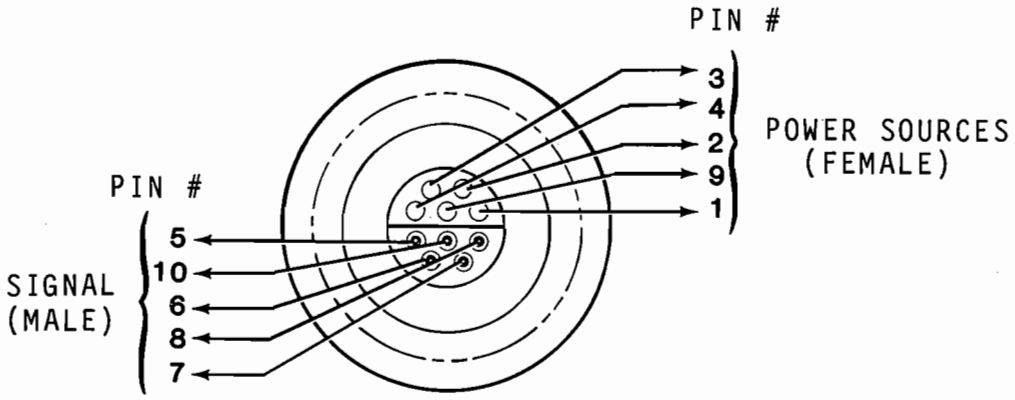


Figure B-1 External Accessory Connector (Front View)

CONNECTOR PIN ASSIGNMENTS			
Pin No.	Power Source	Pin No.	Signal Source
1	+12 V	5	External FM Modulation
2	-12 V	6	Tone Keying *
3	+5 V	7	Microphone Keying **
4	Tone Gen	8	Demodulated Signal Out
9	Power Ground	10	Signal Ground

* Open enables TONE 1 generator; short to ground disables TONE 1 generator.
** Short to ground places FM/AM-1500 into generate mode.

B-2 PINOUT TABLE FOR MICROPHONE CONNECTOR

The table below provides pin assignments for the MIC Connector located on the front panel of the FM/AM-1500. This connector provides power for an external microphone and an input point for microphone audio.

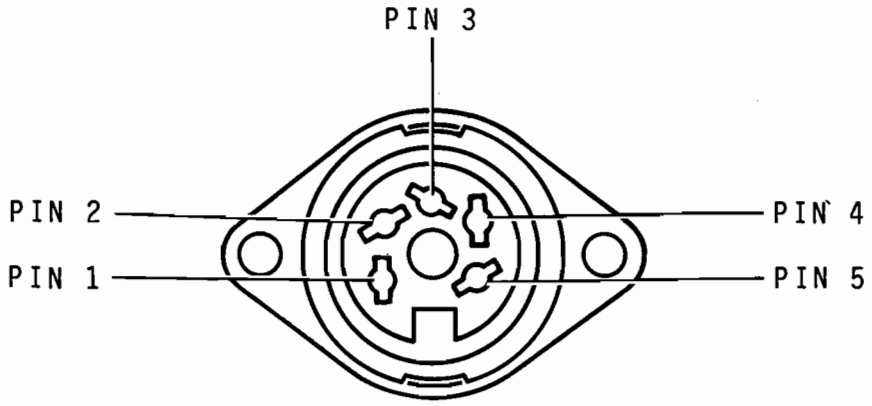


Figure B-2 Microphone Connector (Front View)

CONNECTOR PIN ASSIGNMENTS	
Pin No.	Assignment
1	+12 V
2	Ground
3	Microphone Keying *
4	Microphone Audio
5	No Connection

* Short to ground places FM/AM-1500 into generate mode.

APPENDIX C : PREVENTIVE MAINTENANCE RECOMMENDATIONS

Preventive maintenance on FM/AM-1500 test sets consists primarily of cleaning and visual inspection of internal/external components. External cleaning of the test set is recommended as often as necessary, depending on the environmental conditions to which the set is exposed. Internal cleaning should be performed on a more limited basis, preferably when the set is in a disassembled state for routine calibration, troubleshooting and/or repair. Test set disassembly for the sole purpose of internal cleaning is not recommended.

C-1 EXTERNAL CLEANING

1. Clean front panel and case with a soft lint-free cloth moistened with rubbing alcohol.

2. To remove tar or oil from outside case, safety solvent may be used.

CAUTION

DO NOT ALLOW SAFETY SOLVENT TO CONTACT FRONT PANEL CONTROL AREA. SOLVENT CAN CAUSE DAMAGE TO FRONT PANEL CONTROLS, MARKINGS ETC.

C-2 INTERNAL CLEANING AND INSPECTION

NOTE

The following procedures require external case to be removed from test set.

CAUTION

DELIBERATE MOVING (HOWEVER SLIGHT) OF DISCRETE COMPONENTS ON CIRCUIT BOARDS, ETC. SHOULD BE AVOIDED.

DO NOT OPEN INTERNAL MODULES FOR SOLE PURPOSES OF CLEANING.

1. Remove dust with hand-controlled dry air jet of 15 psi (1.054 kg/cm^2) and wipe internal chassis parts and frame with soft lint-free cloth moistened with alcohol.

1. (Continued)

WARNING

DO NOT USE COMPRESSED AIR IN EXCESS OF 15 PSI. USE EXTREME CARE WHEN USING COMPRESSED AIR IN THE VICINITY OF CRT, IN ORDER TO MINIMIZE POSSIBILITY OF CRT IMPLOSION. OBSERVE FOLLOWING PRECAUTIONS:

a. REMOVE ANY LARGE DIRT/DUST PARTICLES FROM CRT MANUALLY, AS OPPOSED TO USING COMPRESSED AIR.

b. DO NOT USE COMPRESSED AIR IN A DIRTY, CLUTTERED ENVIRONMENT. REMOVE ANY DEBRIS OR SMALL OBJECTS IN THE IMMEDIATE WORK AREA THAT MAY BECOME AIRBORNE DUE TO PRESSURIZED AIRFLOW.

c. IF POSSIBLE, USE AN AIR HOSE NOZZLE EQUIPPED WITH A SPRING LOADED ON/OFF VALVE, AS OPPOSED TO ONE THAT REMAINS OPEN OR CLOSED CONTINUOUSLY.

d. MAKE SURE COMPRESSED AIR HOSE IS FILTERED, TO PREVENT POSSIBLE OIL OR WATER DROPLETS FROM STRIKING CRT AT HIGH SPEEDS.

2. Inspect CHASSIS for:

   a. Tightness of subassemblies and chassis mounted connectors.

   b. Corrosion or damage to metal surfaces.

3. Inspect CAPACITORS for:

   a. Loose mounting, deformities or obvious physical damage.

   b. Leakage or corrosion around leads.

4. Inspect CONNECTORS for:

   a. Loose or broken parts, cracked insulation and bad contacts. DO NOT disassemble connectors needlessly within test set.

5. Inspect POTENTIOMETER CONTROLS for:

   a. Free rotation. If rotation feels rough, check control with an ohmmeter.

6. Inspect readily accessible PRINTED CIRCUIT BOARDS for:

   a. Corrosion or damage to connectors.

6. (Continued)

   b. Damage to all mounted components including crystals and I.C.'s.

   c. Accumulation of dirt, dust or other foreign material.

7. Inspect RESISTORS for:

   a. Cracked, broken, charred or blistered bodies.

   b. Loose or corroded solder connections.

8. Inspect SEMICONDUCTORS for:

   a. Cracked, broken, charred or discolored bodies.

   b. Seals around leads being in place and in good condition.

9. Inspect TOGGLE SWITCHES for:

   a. Loose levers or terminals and switch body contact to frame.

   b. Bent or loose line switch contacts.

10. Inspect TRANSFORMER for:

    a. Signs of excessive heating.

    b. Broken or charred insulation and loose mounting hardware.

11. Inspect WIRING for:

    a. Broken or loose ends and connections.

    b. Proper dress relative to other chassis parts.

NOTE

All laced wiring should be tight with ends securely tied.

APPENDIX D : SPECIAL ACCESSORY TEST EQUIPMENT

D-1 GENERAL

This appendix contains recommendations for constructing special equipment necessary for performing certain test procedures in this manual.

D-2 BATTERY LOAD SIMULATOR

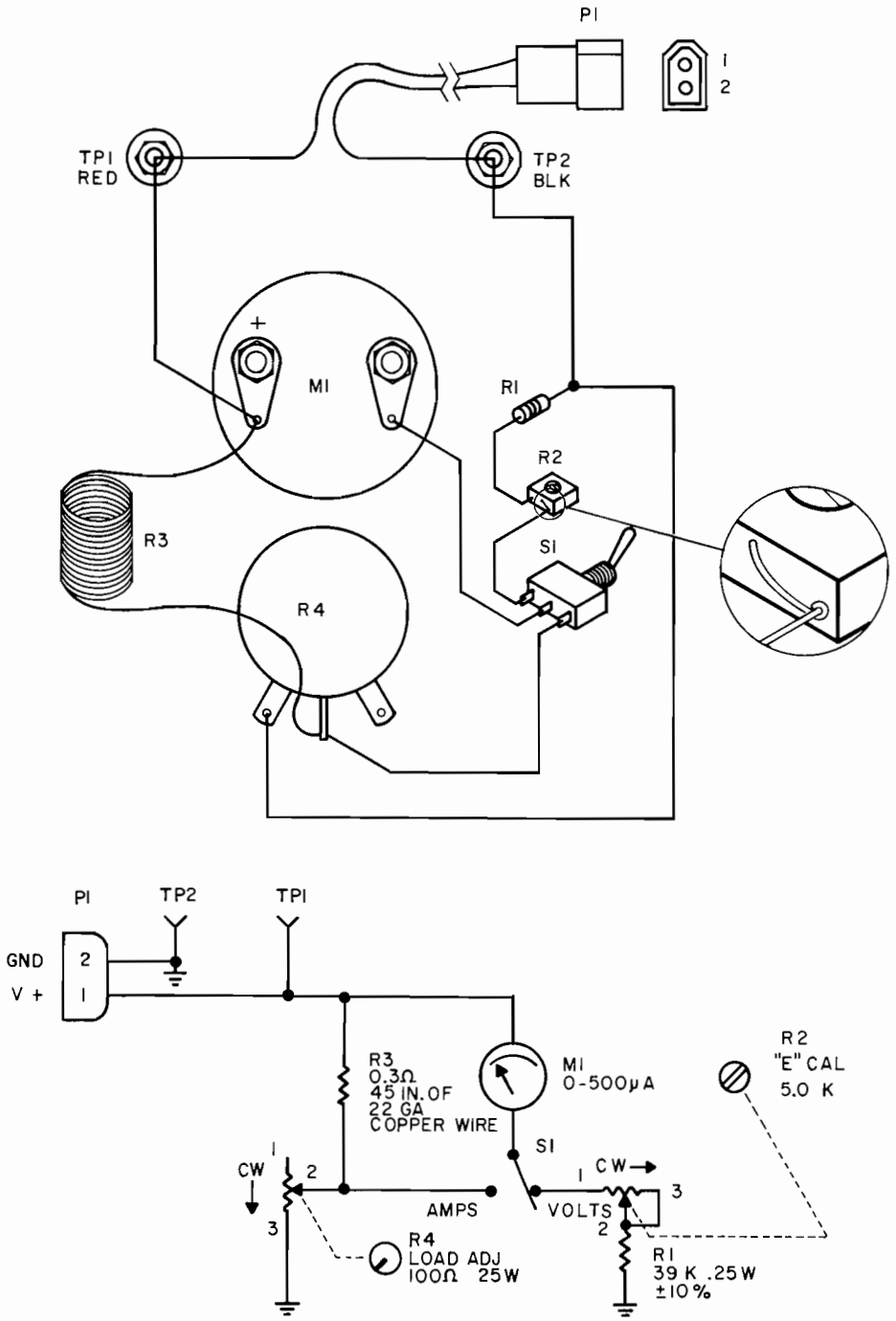
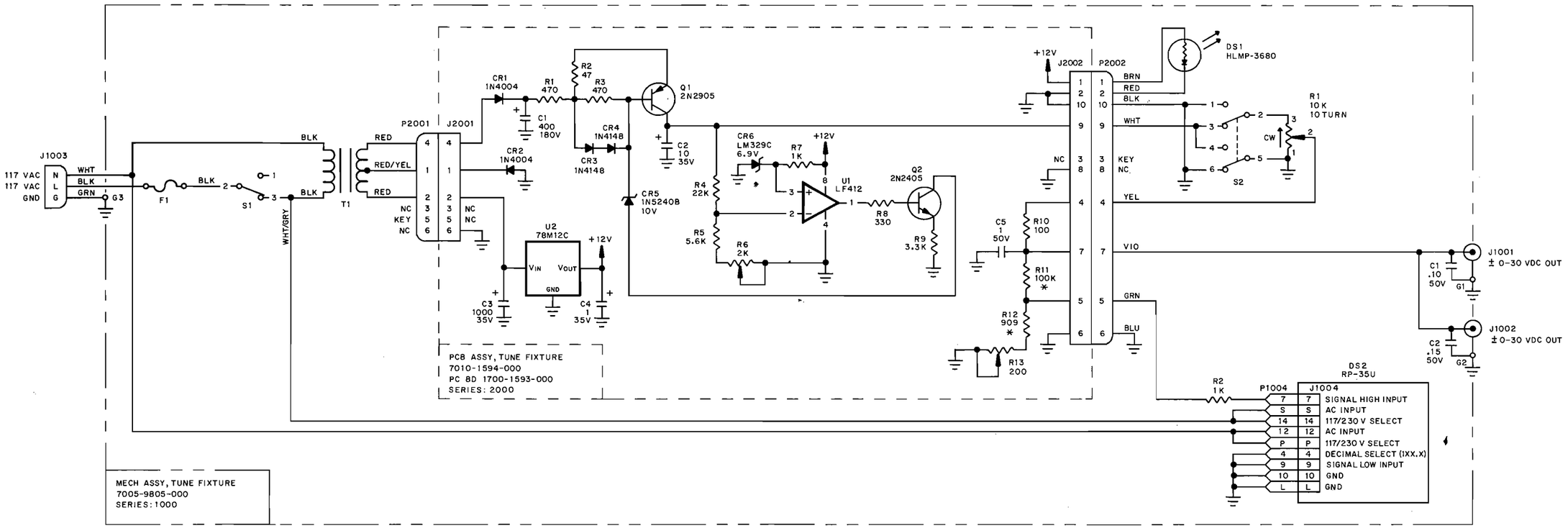
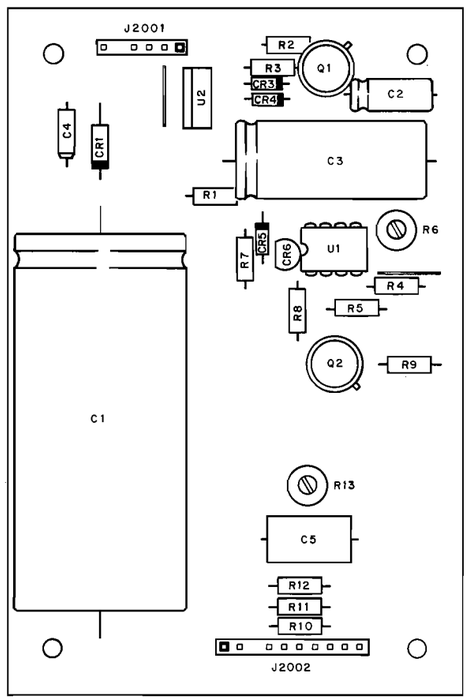
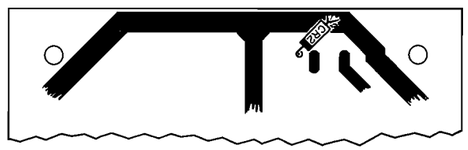


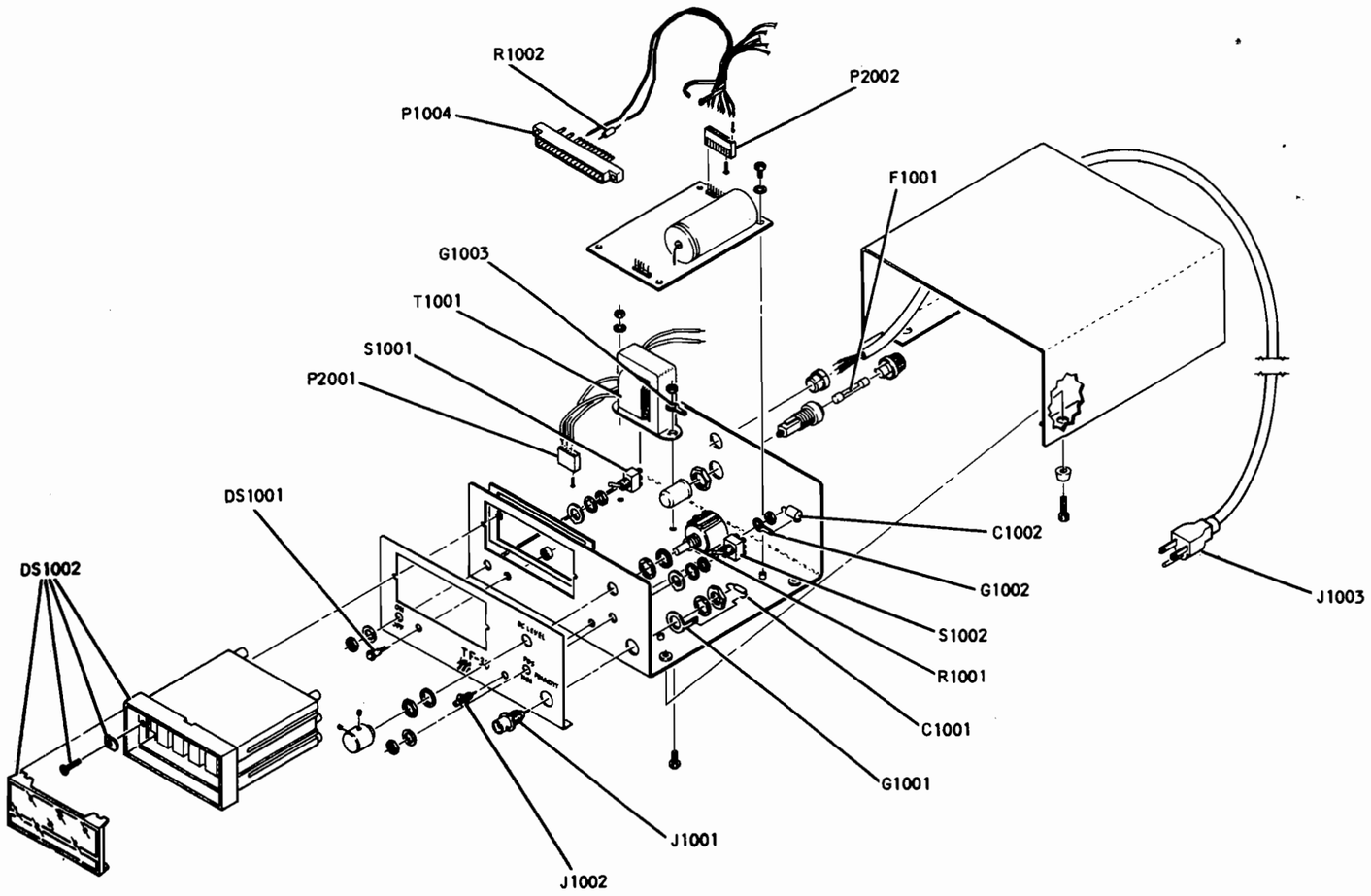
Figure D-1 Circuit Schematic and Diagram of Battery Load Simulator

TF-30 TUNE FIXTURE ASSEMBLY





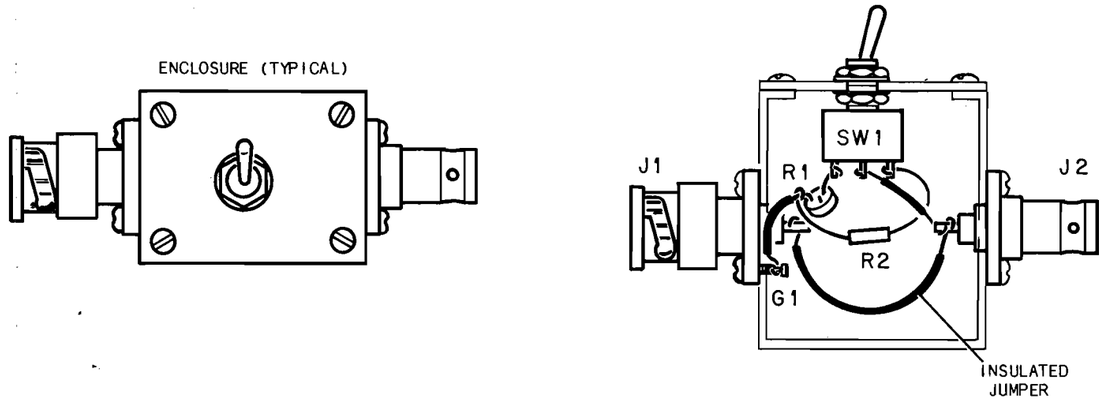




REF DES	DESCRIPTION	IFR PART NO.	QTY
	TUNE FIXTURE ASSEMBLY		
J1001	CONNECTOR, BNC	2113-0000-020	1
J1002	CONNECTOR, SMB	2123-0000-038	1
J1003	CABLE ASSY, AC POWER	6041-0000-001	1
P1004	CONNECTOR, CARD EDGE	2122-0000-018	1
P2001	CONNECTOR, WAFER	2115-0000-006	1
P2002	CONNECTOR, WAFER	2115-0000-013	1
C1001	CAPACITOR .10 µF, 50 V	1521-0000-008	1
C1002	CAPACITOR .15 µF, 50 V	1646-1540-098	1
DS1001	LED GRN	4950-0300-200	1
DS1002	DISPLAY, DIGITAL VOLTMETER	4600-0000-006	1
F1001	FUSE, FAST BLO 1 A, 250 V		1
G1001	LUG, GND 3/8"	2850-0000-025	1
G1002	LUG, GND 3/8"	2850-0000-041	1
G1003	LUG, GND #4 INT TOOTH	2850-0000-014	1
R1001	RESISTOR, VAR 10 K	4770-8810-300	1
R1002	RESISTOR 5%, 1/4 W, 1 K	4702-0102-003	1
S1001	SWITCH, TOGGLE	5114-0000-001	1
S1002	SWITCH, TOGGLE	5114-0000-004	1
T1001	TRANSFORMER	5604-0000-002	1
	TUNE FIXTURE, PC BD	7010-9806-900	1
J2001	CONNECTOR, WAFER	2115-1001-006	1
J2002	CONNECTOR, WAFER	2115-0000-016	1
C2001	CAPACITOR 400 µF, 180 V	1580-4010-800	1
C2002	CAPACITOR 10 µF, 35 V	1580-1000-350	1
C2003	CAPACITOR 1000 µF, 35 V	1580-1020-358	1
C2004	CAPACITOR 1 µF, 35 V	1507-0105-118	1
C2005	CAPACITOR 1 µF, 50 V	1502-0105-007	1
CR2001	DIODE, RECT IN4004	4815-0000-002	1
CR2002	DIODE, RECT IN4004	4815-0000-002	1
CR2003	DIODE, SIGNAL IN4148	4815-0000-003	1
CR2004	DIODE, SIGNAL IN4148	4815-0000-003	1
CR2005	DIODE, ZENER 10 V	4818-0000-001	1
CR2006	DIODE, ZENER 6.9 V	4818-0000-015	1
Q2001	TRANSISTOR 2N2905	4801-0000-004	1
Q2002	TRANSISTOR 2M2405	4801-0000-002	1
R2001	RESISTOR 5%, 1/4 W, 470 OHM	4702-0471-003	1
R2002	RESISTOR 5%, 1/4 W, 47 OHM	4702-0470-003	1
R2003	RESISTOR 5%, 1/4 W, 470 OHM	4702-0471-003	1
R2004	RESISTOR 5%, 1/4 W, 22 K	4702-0223-003	1
R2005	RESISTOR 5%, 1/4 W, 5.6 K	4702-0562-003	1
R2006	RESISTOR, VAR 2 K	4752-0202-002	1
R2007	RESISTOR 5%, 1/4 W, 1 K	4702-0102-003	1
R2008	RESISTOR 5%, 1/4 W, 330 OHM	4702-0331-003	1
R2009	RESISTOR 5%, 1/4 W, 3.3 K	4702-0332-003	1
R2010	RESISTOR 5%, 1/4 W, 100 OHM	4702-0101-003	1
R2011	RESISTOR 1%, 1/4 W, 100.00 OHM	4706-1003-001	1
R2012	RESISTOR 1%, 1/4 W, 909.00 OHM	4706-9090-001	1
R2013	RESISTOR, VAR 200 OHM	4752-0201-002	1
U2001	IC, DUAL J-FET OP AMP LF412	3135-0000-054	1
U2002	IC, REGULATOR 78M12C	5750-0000-010	1
	WIRE, BUS 22 GA	1050-0000-073	

Figure D-2 Circuit Schematic and Diagram of TF-30 Tune Fixture Assembly

D-4 50 OHM/150 OHM LOAD CONNECTOR



PART	TYPE	IFR PART NO.
J1	UG12094/U	2113-0000-020
J2	UG1104 A/U	2113-0000-019
R1	200Ω, VAR.	4752-0201-002
R2	47Ω, 5%	----
SW1	C&K 7103	5114-0000-002
ENCLOSURE	ANY	----

Figure D-3 Circuit Schematic and Diagram of 50Ω/150Ω Load Connector

D-5 REMOVABLE 20 dB TEST POINT

FABRICATE 20 dB TEST POINT AS FOLLOWS:

1. SOLDER RESISTOR TO FIRST SMB CONNECTOR.

2. SOLDER RF SHIELD TO FIRST SMB CONNECTOR.

3. USING ACCESS HOLE, SOLDER RESISTOR TO SECOND SMB CONNECTOR.

4. SOLDER SECOND SMB CONNECTOR TO RF SHIELD.

5. SOLDER BUS WIRE TO FIRST SMB CONNECTOR.

6. TRIM BUS WIRE TO LENGTH REQUIRED TO CONTACT TEST POINT BEING ACCESSED.

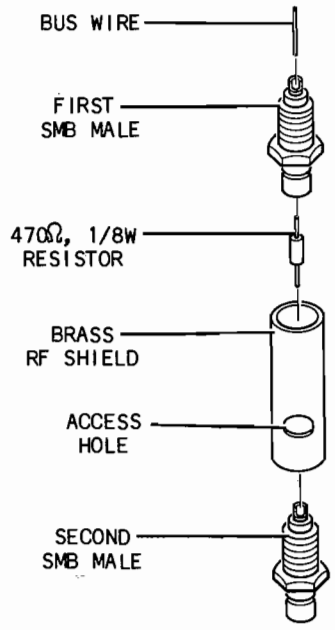
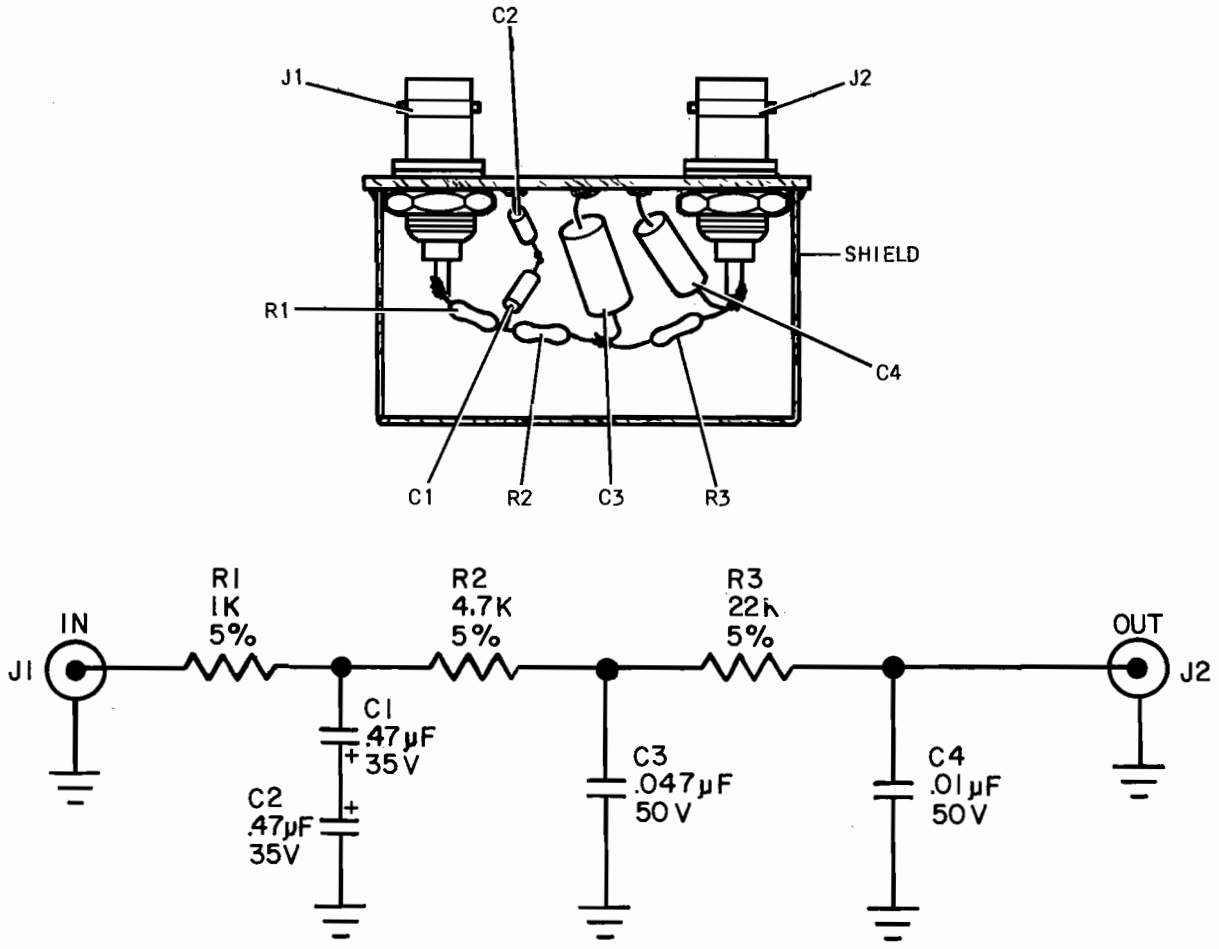


Figure D-4 20 dB Test Point

D-6 300 Hz LOW PASS FILTER



PART	TYPE	IFR PART NO.
J1	UG1104 A/U	2113-0000-019
J2	UG1104 A/U	2113-0000-019
R1	1 KΩ, 5%	4701-0102-003
R2	4.7 KΩ, 5%	4701-0472-003
R3	22 KΩ, 5%	4701-0223-003
C1	.47µF, 35V Tant	1507-0474-018
C2	.47µF, 35V Tant	1507-0474-018
C3	.047µF, 50V Poly Carb	1502-0473-010
C4	.01µF, 50V Poly Carb	1502-0103-010

Figure D-5 Circuit Schematic and Diagram of 300 Hz Low Pass Filter

APPENDIX E : TEST EQUIPMENT REQUIREMENTS

E-1 GENERAL

This appendix contains a list of test equipment suitable for performing all of the maintenance procedures contained in this manual. Any other equipment meeting the specifications listed in this appendix may be substituted in place of the recommended models. It should be noted that the equipment listed in this appendix may exceed the minimum required specifications for some of the procedures contained in this manual.

E-2 RECOMMENDED TEST EQUIPMENT

TYPE	MANUFACTURER & MODEL	SPECIFICATIONS
Oscilloscope	Tektronix 465B	DC to 100 MHz 5 mV/div vertical trace 2 nS/div sweep rate Dual Trace
Spectrum Analyzer	Tektronix 7613 Frame Tektronix 7L13/U Spectrum Analyzer	Variable Persistance Storage Oscilloscope Frequency Range: 1 kHz to 2.5 GHz Resolution Bandwidth: 30 Hz to 3 MHz
Tracking Generator	Tektronix TM503 Frame Tektronix TR502 Tracking Generator	Three-wide Mainframe Frequency Range: 100 kHz to 1.8 GHz Output Level: 0 dBm, ±0.5 dB Power Range: 0 to -59 dBm in 10 and 1 dB steps
Frequency Counter	Fluke Model 1910A	Frequency Range: 5 Hz to 125 MHz
Digital Multimeter	Fluke Model 8010A	3½ digit, ±0.1% basic DC accuracy
Distortion Analyzer	Sound Technology Model 1700B	Frequency Range: 10 Hz to 110 kHz Accuracy: .002% distortion AC Voltage Accuracy: 2%

TYPE	MANUFACTURER & MODEL	SPECIFICATIONS
Function Generator	Wavetek 182A	Frequency Range: .004 Hz to 4 MHz Functions: Sine, Triangle & Square High Level Output: 20 Vp-p (10 Vp-p into 50Ω)
Signal Generator	Hewlett Packard 8640B	Frequency Range: 1 to 1000 MHz Resolution: 0.1 to 100 Hz Accuracy: 2×10^{-6} RF Output: +20 to -130 dBm
Wattmeter	Sierra 174A-1	Frequency Range: 25 to 1000 MHz VSWR: 25-512 MHz: 1.10 max 512-1000 MHz: 1.20 max Accuracy Incident Power: 25-512 MHz: ±5% of full scale 512-1000 MHz: ±7% of full scale
FM/AM Modulation Meter	Boonton Model 82AD	Frequency Range: 10 MHz to 1.2 GHz Accuracy: FM: ±2% of reading from 30 Hz to 100 kHz Accuracy: AM: ±2% of reading from 10 Hz to 90% AM and 5% of reading below 10% and above 90%; from 30 Hz to 100 kHz Resolution: 0.1% of full scale for FM and AM

TYPE	MANUFACTURER & MODEL	SPECIFICATIONS
RF Power Source	MCL 15122 Main Frame 6048 Oscillator Module	Frequency Range: 50 to 200 MHz Power Range: 0 to 65 W
RF Power Meter with Power Detector	Boonton RF Microwatt-meter Model 42 BD	Frequency Range: 200 kHz to 18 GHz Power Range: 1.0 nW to 10 mW Accuracy: ±0.25% fs ±0.15 dB >10 nW
	Boonton Power Sensor Model 41-4A	Frequency Range: 200 kHz to 7 GHz Power Range: 1 nW to 10 mW Accuracy: ±0.3 dB >10 nW
Triple Output Power Supply	LAMBDA LPT-7202-FM	Regulation: 0.01% + 1 mV Ripple: 500μV Voltage Ranges: 0-7 VDC @ 5.0 A 0-20 VDC @ 1.5 A 0-20 VDC @ 1.5 A
Power Supply	LAMBDA LK-351-FM	Regulation: .015% or 1 mV Ripple: 500μV Voltage Range: 0-36 VDC @ 25.0 A
Oscilloscope Calibrator	Tektronix PG 506 Module	Accuracy: 0.25%, ±1μV Voltage Range: 50 mV to 50V minimum

APPENDIX F : MECHANICAL ALIGNMENT OF FM/AM-1500 RF OUTPUT LEVEL CONTROL

F-1 GENERAL

In certain maintenance operations it may be necessary to disassemble the front panel RF OUTPUT LEVEL Control (or Variable Attenuator). Upon reassembly, the atttenuator assembly must be properly aligned in order to reflect the true output power levels as indicated on the outer dial. The procedure for this alignment is as follows:

NOTE

The Variable Attenuator and outer dial are individually calibrated to each other at the factory. Do not interchange outer dials and attenuators from different sets.

F-2 ALIGNMENT PROCEDURE

REQUIRED TOOLS:

.050" Allen Wrench
Phillips Screwdriver

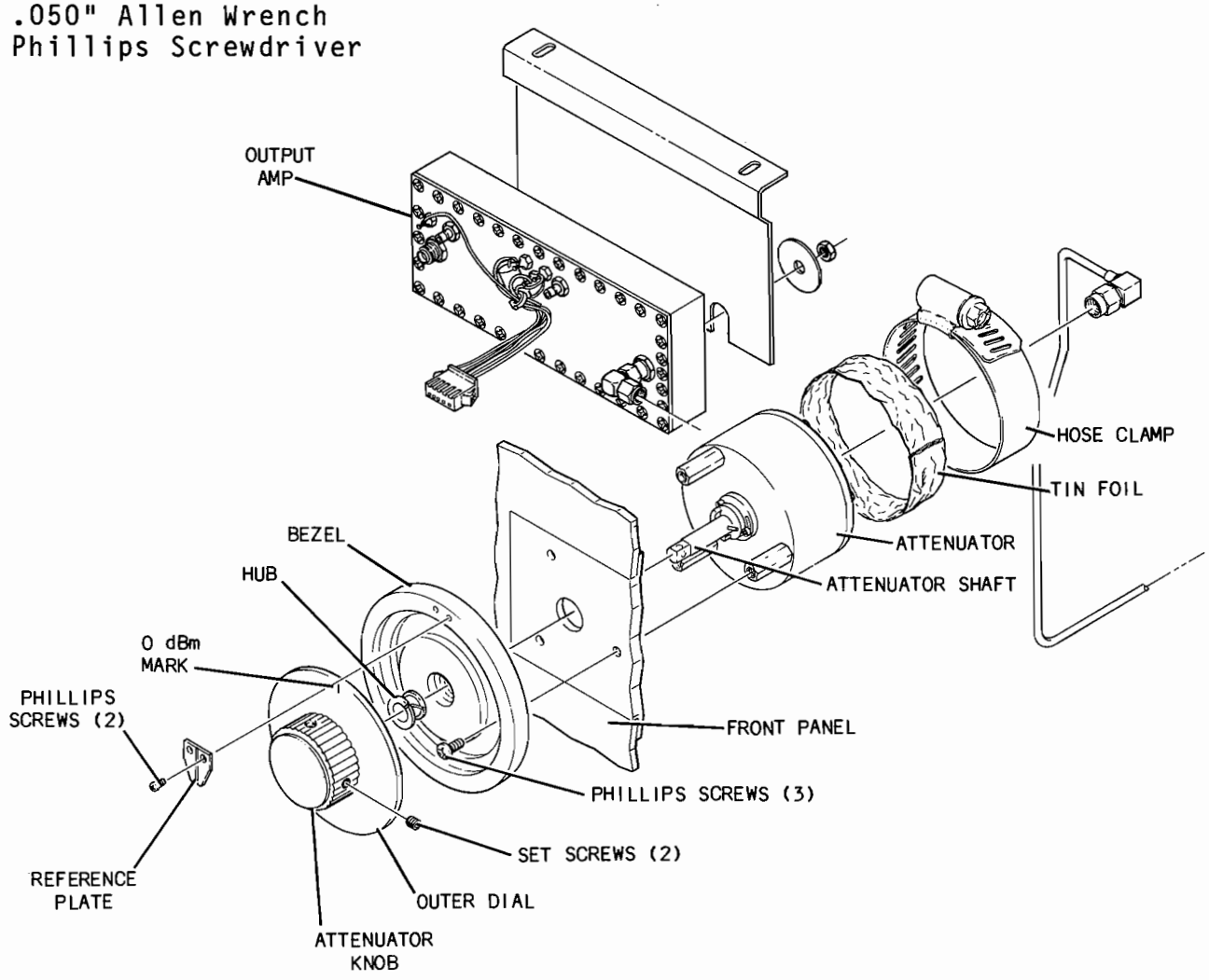


Figure F-1 Identification of Attenuator Components

STEP	PROCEDURE
1.	Rotate attenuator shaft fully cw until stop is reached.
2.	Insert attenuator shaft through front panel and position attenuator so that J1 is to the left (looking from front of FM/AM-1500).
3.	Position bezel against front panel so that reference plate screw holes are at the top. Secure bezel to attenuator with three Phillips screws provided.
4.	Position knob and outer dial on attenuator shaft so that the 0 dBm mark is midway between the two reference plate screw holes.
5.	Secure reference plate to bezel with two Phillips screws provided.
6.	At this point the 0 dBm mark on the outer dial should be directly aligned with the index mark on the reference plate. Secure knob and outer dial to attenuator shaft with two set screws provided.
7.	Rotate knob ccw and then fully cw. Verify that when knob is fully cw, the index mark on the reference plate is directly aligned with the 0 dBm mark on the outer dial.

APPENDIX G : dBm TO MICROVOLT CONVERSION CHART

dBm	µV	dBm	µV	dBm	µV
0	224,000	-47	1,000	-94	4.47
-1	200,000	-48	891	-95	3.99
-2	178,000	-49	795	-96	3.55
-3	159,000	-50	709	-97	3.17
-4	141,000	-51	633	-98	2.82
-5	126,000	-52	563	-99	2.52
-6	112,000	-53	501	-100	2.24
-7	100,000	-54	447	-101	2.00
-8	89,100	-55	399	-102	1.78
-9	79,500	-56	355	-103	1.59
-10	70,900	-57	317	-104	1.41
-11	63,300	-58	282	-105	1.26
-12	56,300	-59	252	-106	1.12
-13	50,100	-60	224	-107	1.00
-14	44,700	-61	200	-108	0.891
-15	39,900	-62	178	-109	0.795
-16	35,500	-63	159	-110	0.709
-17	31,700	-64	141	-111	0.633
-18	28,200	-65	126	-112	0.563
-19	25,200	-66	112	-113	0.501
-20	22,400	-67	100	-114	0.447
-21	20,000	-68	89.1	-115	0.399
-22	17,800	-69	79.5	-116	0.355
-23	15,900	-70	70.9	-117	0.317
-24	14,100	-71	63.3	-118	0.282
-25	12,600	-72	56.3	-119	0.252
-26	11,200	-73	50.1	-120	0.224
-27	10,000	-74	44.7	-121	0.200
-28	8,900	-75	39.9	-122	0.178
-29	7,950	-76	35.5	-123	0.159
-30	7,090	-77	31.7	-124	0.141
-31	6,330	-78	28.2	-125	0.126
-32	5,630	-79	25.2	-126	0.112
-33	5,010	-80	22.4	-127	0.100
-34	4,470	-81	20.0	-128	0.0891
-35	3,990	-82	17.8	-129	0.0795
-36	3,550	-83	15.9	-130	0.0709
-37	3,170	-84	14.1	-131	0.0633
-38	2,820	-85	12.6	-132	0.0563
-39	2,520	-86	11.2	-133	0.0501
-40	2,240	-87	10.0	-134	0.0447
-41	2,000	-88	8.91	-135	0.0399
-42	1,780	-89	7.95	-136	0.0355
-43	1,590	-90	7.09	-137	0.0317
-44	1,410	-91	6.33	-138	0.0282
-45	1,260	-92	5.63	-139	0.0252
-46	1,120	-93	5.01	-140	0.0224

APPENDIX H : FM/AM-1500 REFERENCE DESIGNATOR ASSIGNMENT CHART

REF DES	DESCRIPTION	DATA PART NO.
100	LCD/KEYBOARD PC BD ASSY	7010-5030-100
200	KEYPAD PC BD ASSY	7010-5030-200
300	FRONT PANEL UPPER PC BD ASSY	7010-5030-300
400	FRONT PANEL MECH ASSY	7005-5040-500
500	FRONT PANEL LOWER PC BD ASSY	7010-5030-500
600	HIGH/LOW PASS FILTER MECH ASSY	7005-5040-700
700	HIGH/LOW PASS FILTER PC BD ASSY	7010-5030-700
800	OUTPUT AMP MECH ASSY	7005-5040-900
900	OUTPUT AMP PC BD ASSY	7010-5030-900
1000	1300 MHz IF RECEIVER MECH ASSY (1005 thru 1406)	7005-5041-300
1000	1300 MHz IF RECEIVER MECH ASSY (1407 & ON)	7005-5041-400
1100	RECEIVE ATTENUATOR PC BD ASSY (1005 thru 1406)	7010-5031-100
1100	RECEIVE ATTENUATOR PC BD ASSY (1407 & ON)	7010-5031-200
1200	1300 MHz IF GENERATOR MECH ASSY	7005-5041-500
1300	1300 MHz RECEIVER IF PC BD ASSY (1005 thru 1406)	7010-5031-300
1300	1300 MHz RECEIVER IF PC BD ASSY (1407 & ON)	7010-5031-400
1400	CLOCK DIVIDER MECH ASSY	7005-5041-700
1500	1300 MHz IF GENERATOR PC BD ASSY	7010-5031-500
1600	1120 MHz IF GENERATOR PC BD ASSY	7010-5031-600
1700	CLOCK DIVIDER PC BD ASSY	7010-5031-700
1800	LOW LOOP MIXER MECH ASSY	7005-5041-900
1900	LOW LOOP MIXER PC BD ASSY	7010-5031-900
2000	1210 MHz VCO PC BD ASSY	7010-5232-000
2100	1300-2300 MHz VCO PC BD ASSY	7010-5232-100
2200	HIGH LOOP #1 PC BD ASSY	7010-5032-100
2300	HIGH LOOP #2 PC BD ASSY	7010-5032-300
2400	DUAL VCO MECH ASSY	7005-5042-101
2500	DELAY LINE #1 PC BD ASSY	7010-5032-400
2600	DELAY LINE #2 PC BD ASSY	7010-5032-600
2700	DUPLEX OFFSET PC BD ASSY	7010-5032-700
2800	HIGH LOOP MECH ASSY	7005-5042-300
2900	89-90 MHz RECEIVER PC BD ASSY	7010-5032-900
3000	DELAY LINE MECH ASSY	7005-5042-500
3100	LOW LOOP PC BD ASSY	7010-5033-100
3200	DUPLEX OFFSET MECH ASSY	7005-5042-700
3300	FM GENERATOR PC BD ASSY	7010-5033-300
3400	GENERATE MIXER PC BD ASSY	7010-5033-400
3500	SPECTRUM ANALYZER L.O. PC BD ASSY	7010-5033-500
3600		
3700	SPECTRUM ANALYZER R.F. PC BD ASSY	7010-5033-700
3800	89-90 MHz RECEIVER MECH ASSY	7005-5042-900
3900	SPECTRUM ANALYZER IF PC BD ASSY	7010-5033-900
4000	LOW LOOP MECH ASSY	7005-5043-100
4100	CPU/MEMORY PC BD ASSY	7010-5034-1XX
4200	FM GENERATOR MECH ASSY	7005-5043-300
4300	I/O INTERFACE PC BD ASSY	7010-5034-300
4400	GENERATE MIXER MECH ASSY	7005-5043-400
4500	DUAL TONE GENERATOR PC BD ASSY	7010-5034-500
4600	SPECTRUM ANALYZER L.O. MECH ASSY	7005-5043-500

REF DES	DESCRIPTION	DATA PART NO.
4700 4800 4900 5000	DEMOD AUDIO PC BD ASSY (1005 thru 1425)	7010-5034-700
4700 4800 4900 5000	DEMOD AUDIO PC BD ASSY (1426 & ON)	7010-5037-300
5100 9500	OSCILLOSCOPE CONTROL & DEFLECTION PC BD ASSY	7010-5035-100
5200	SPECTRUM ANALYZER RF MECH ASSY	7005-5043-700
5300	MOTHERBOARD PC BD ASSY	7010-5035-300
5400	SPECTRUM ANALYZER IF MECH ASSY	7005-5043-900
5600	40 V POWER SUPPLY PC BD ASSY	7010-5035-600
5700	POWER SUPPLY PC BD ASSY	7010-5035-700
5800	LINE RECTIFIER PC BD ASSY	7010-5035-800
5900	GPIB INTERFACE MODULE	7005-5045-900
6000	POWER SUPPLY MECH ASSY	7005-5045-700
6200	POWER TERMINATION MECH ASSY (THRU S/N 1993)	7005-5046-100
6400	COMPOSITE MECH ASSY	7003-5040-000
6500 6600	CELLULAR CONTROLLER PC BD ASSY	7010-5036-600
6700	CARD EXTENDER OPTIONAL ASSY (OPTION-05)	7001-5046-700
6800A	BUFFER AMP PC BD ASSY	7010-5036-800
6800B	BUFFER AMP PC BD ASSY	7010-5036-800
6900A	BUFFER AMP MECH ASSY	7005-5046-800
6900B	BUFFER AMP MECH ASSY	7005-5046-800
7000	TCXO ASSY	7001-5086-800
7100	DIODE SWITCH MECH ASSY (1005 thru 1406)	7005-5044-800
7200	HIGH OUTPUT AMP PC BD ASSY	7010-5035-400
7300	HIGH OUTPUT AMP MECH ASSY (OPTION-04)	7001-5045-400
7400	OVEN OSCILLATOR OPTIONAL ASSY (OPTION-02)	7001-5046-500
7500	RF ATTENUATOR DRIVER MECH ASSY	7005-5040-400
AT7500	PROGRAMMABLE ATTENUATOR	7010-3632-501
7900	GPIB INTERFACE PC BD ASSY	7010-5035-900
8000	GPIB ANALYZER DIGITIZER PC BD ASSY	7010-5036-000
8100	GPIB LCD PC BD ASSY	7010-5036-200
8200	ATTEN CONTROL & DISPLAY PC BD ASSY	7010-5036-300
8300	GPIB LCD DISPLAY ASSY	7005-5046-000
8400	GPIB WEAR ADAPTER MECH ASSY	7005-5046-200
8500	ICD-1500 PC BD ASSY	7010-5037-100
8600	ICD-1500 TEST BOX OPTIONAL ASSY (OPTION-10)	7005-5047-100
9100	CELLULAR MECH ASSY (OPTION-08)	7001-5046-600
9300	MIXER NULL MECH ASSY (1235 & ON)	7005-5047-600
9400	MIXER NULL PC BD ASSY	7010-5037-600
9800	POWER TERMINATION MECH ASSY (S/N 1994 & ON)	7005-5048-400
9900	INVERTER BOARD FOR OSCILLOSCOPE CONTROL & DEFLECTION PC BD	7010-5038-600

APPENDIX J : REPACKING FOR SHIPMENT

J-1 SHIPPING INFORMATION

IFR test sets returned to factory for calibration, service or repair must be repackaged and shipped subject to the following conditions:

Do not return any products to factory without first receiving authorization from IFR Customer Service Department.

CONTACT:

Customer Service Dept.
IFR, Inc.
10200 West York Street
Wichita, Kansas 67215

Telephone: (800)-835-2350
TWX: 910-741-6952

All test sets must be tagged with:

a. Owner's identification and address.
b. Nature of service or repair required.
c. Model No.
d. Serial No.

Sets must be repackaged in original shipping containers using IFR packing molds. If original shipping containers and materials are not available, contact IFR Customer Service Dept. for shipping instructions.

All freight costs on non-warranty shipments are assumed by customer. (See "Warranty Packet" for freight charge policy on warranty claims.)

J-2 REPACKING PROCEDURE (Reference - Figure J-1):

1. Make sure bottom packing mold is seated on floor of shipping container.

2. Carefully wrap test set with polyethylene sheeting to protect finish.

3. Place test set into shipping container, making sure set is securely seated in bottom packing mold.

4. Place top packing mold over top of set and press down until mold rests solidly on bottom packing mold.

5. Close shipping container lids and seal with shipping tape or an industrial stapler. Tie all sides of container with break resistant rope, twine or equivalent.

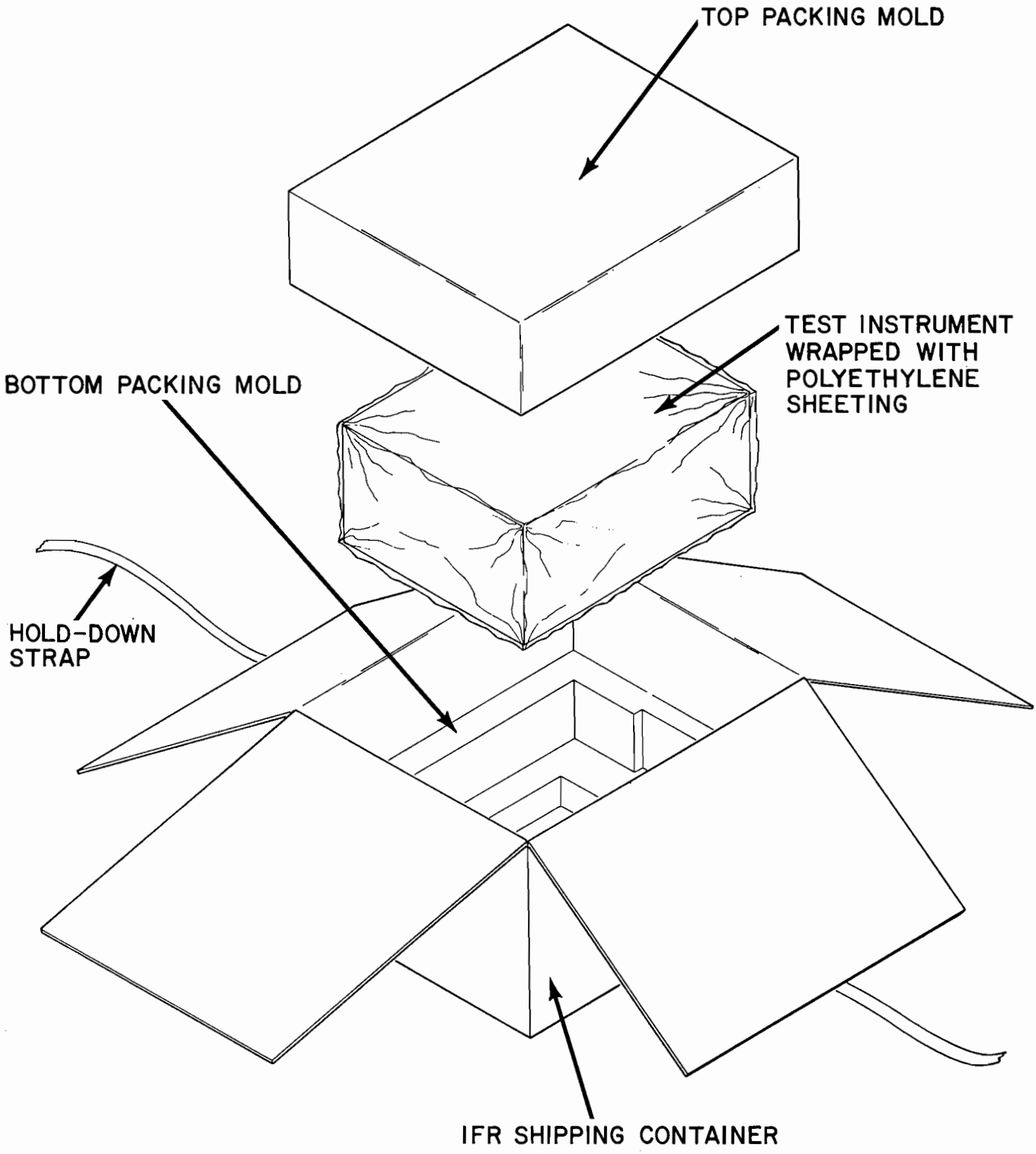


Figure J-1 Repacking for Shipment

APPENDIX K : ABBREVIATIONS & SYMBOLS

K-1 GENERAL

Defined below are various abbreviations and symbols which are commonly used throughout the FM/AM-1500 Maintenance Manual text.

K-2 GENERAL ABBREVIATIONS

A	- Ampere
AC or ac	- Alternating Current
Adj	- Adjustment
AGC	- Automatic Gain Control
AM	- Amplitude Modulation
Amp	- Ampere
ANALY DISP.	- Analyzer Dispersion
Assy	- Assembly
BATT	- Battery
BCD	- Binary Coded Decimal
BFO	- Beat Frequency Oscillator
°C	- Degrees Celsius
CAL	- Calibration
ccw	- Counterclockwise
CRT	- Cathode Ray Tube
cw	- Clockwise
CW	- Carrier Wave
DAC	- Digital to Analog Converter
dB	- decibels
dBc	- decibels above or below carrier level
dBm	- decibels above (or below) 1 milliwatt
DC or dc	- Direct Current
DCR	- Duty Cycle Regulator
DEFLEC AMP	- Deflection Amplifier
DEMOD	- Demodulation, demodulate or demodulated
DEV	- Deviation
DMM	- Digital Multimeter
DVM	- Digital Voltmeter
ECL	- Emitter Coupled Logic
EXT ACC	- External Accessory
EXT MOD	- External Modulation
EXT DC	- External Direct Current
°F	- Degrees Fahrenheit
FET	- Field Effect Transistor
FILT	- Filter
FM	- Frequency Modulation
FREQ	- Frequency
GEN	- Generate
GHz	- Gigahertz
GND	- Ground
HI LVL	- High Level
HORIZ	- Horizontal

Hz	- Hertz
IC	- Integrated Circuit
IF	- Intermediate Frequency
INT MOD	- Internal Modulation
IPC	- Illustrated Parts Catalog
Kg/cm^3	- Kilogram per cubic centimeter
kHz	- kilohertz
L/H	- Left-hand
LOG LIN	- Logarithmic Linearity
LO	- Local Oscillator
mA	- Milliamperes
MAX DISP	- Maximum Dispersion
Mech	- Mechanical
MHz	- Megahertz
MON	- Monitor
µs	- microsecond
µV	- microvolt
ms or mSec	- millisecond
mV	- millivolt
mW	- milliwatt
MULT	- Multiplier
N/A	- Not Applicable
NORM	- Normal
OSC	- Oscillator
para	- paragraph
PC Bd	- Printed Circuit Board
PLL	- Phase Lock Loop
Preamp	- Preamplifier
psi	- pounds per square inch
PWR	- Power
PWR MON	- Power Monitor
RCVR	- Receiver
REF	- Reference
RF	- Radio Frequency
R/H	- Right-hand
RMS	- Root Mean Square
ROM	- Read Only Memory
sec	- Seconds
Scope Dev	- Oscilloscope Deviation
SIG	- Signal
SSB	- Single Sideband
SW	- Switch
TCXO	- Temperature Compensated Crystal Oscillator
TRANS	- Transmitter or Transceiver
TTL	- Transistor Transistor Logic
V	- Volts
Vp	- Volts Peak
Vp-p	- Volts Peak-to-Peak
VAC	- Volts Alternating Current
VCO	- Voltage Controlled Oscillator

VDC - Volts Direct Current
VHF - Very High Frequency
VOL - Volume
VRMS - Volts Root Mean Square
VSWR - Voltage Standing Wave Ratio
W - Watts
XMTR - Transmitter
XTAL - Crystal

K-3 ABBREVIATIONS FOR REFERENCE DESIGNATORS

BR - Bridge Rectifier
C - Capacitor
CR - Diode
DS - Display Lamps
E - Terminal
FL - Feed-thru Filter
G or GL - Ground
J - Connector (Fixed)
K - Relay
L - Inductor
M - Meter
MXR - Mixer
P - Connector (Movable)
Q - Transistor
R - Resistor
SW or S - Switch
T - Transformer
U - Integrated Circuit
VR - Voltage Regulator
Y - Crystal
YFL - Crystal Filter
Z - Tuned Cavity