

# MAINTENANCE MANUAL



## FM/AM-1500 COMMUNICATIONS SERVICE MONITOR



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# SECTION 1 - INTRODUCTION

## 1-1 GENERAL

This section provides a brief description of the internal electrical and mechanical configuration of the FM/AM-1500. An "exploded" composite drawing of the FM/AM-1500 is provided in Figure 1-1 to aid the technician in identifying and locating the major assemblies and modules which comprise the set.

## 1-2 ELECTRICAL DESCRIPTION

The FM/AM-1500 is a microprocessor-controlled, digitally synthesized communications service monitor. The signal generator is capable of generating modulated or unmodulated carrier signals within a range of 100 kHz to 999.9999 MHz (in 100 Hz steps), at a continuously variable output level of 0 to -128 dBm.

### NOTE

+20 dBm output may be achieved with an optional High Output Amplifier which attaches to the TRANS/-40 dB DUPLEX Connector (11) on the front panel.

The receiver is a quadruple conversion, super-heterodyne type, capable of monitoring communications signals within a range of 300 kHz to 999.9999 MHz (in 100 Hz steps). The individual modules which make up each major circuit are listed in Table 1-1.

|  |   |
|--|---|
| <u>POWER DISTRIBUTION CIRCUITS</u><br>Power Supply<br>+40 V Power Supply   | <u>FREQUENCY STANDARD CIRCUITS</u><br>Clock Divider<br>TCXO (optional)<br>Oven Oscillator (optional)  |
| <u>FREQUENCY SYNTHESIS CIRCUITS</u><br>High Loop<br>Dual VCO<br>Low Pass Filter<br>High/Low Pass Filter<br>Delay Line<br>Buffer Amplifiers A & B |   |
| <u>RECEIVER CIRCUITS</u><br>1300 MHz IF Receiver<br>89-90 MHz Receiver<br>Demod Audio PC Board<br>Oscilloscope Control & Deflection PC Board     | <u>GENERATOR CIRCUITS</u><br>FM Generator<br>Generate Mixer<br>1300 MHz IF Generator<br>Output Amplifier<br>Duplex Offset<br>Power Termination<br>Dual Tone Generator<br>High Output Amplifier (Optional) |
| <u>SPECTRUM ANALYZER CIRCUITS</u><br>Spectrum Analyzer LO<br>Spectrum Analyzer RF<br>Spectrum Analyzer IF  | <u>MICROPROCESSOR CIRCUITS</u><br>CPU/Memory PC Board<br>I/O Interface PC Board   |

NOTE: Thru Ser. No. 1406, a Diode Switch was included in the Receiver Circuit. Ser. No. 1407 and on, Diode Switch is part of the 1300 MHz Receiver Module.

Table 1-1 FM/AM-1500 Major Electrical Systems

## 1-3 MECHANICAL DESCRIPTION

Mechanically, the FM/AM-1500 consists of the major groupings listed in Table 1-2. Refer to Figure 1-1 for location of each module.

### CASE ASSEMBLY

#### UPPER FLOOR MODULES

|                       |                      |
|-----------------------|----------------------|
| 1300 MHz IF Receiver  | Output Buffers       |
| 1300 MHz IF Generator | High/Low Pass Filter |
| Output Amplifier      | Low Pass Filter      |
| Generate/Mixer        | TCXO (optional)      |
| Dual VCO              |                      |

#### REAR PANEL MODULES

|                            |                           |
|----------------------------|---------------------------|
| Power Supply               | +40 V Power Supply        |
| Power Termination          | Batteries                 |
| Oven Oscillator (optional) | GPIO Interface (optional) |

#### MOTHER BOARD MODULES

|                           |                            |
|---------------------------|----------------------------|
| I/O Interface PC Bd.      | Demod Audio PC Bd.         |
| Osc. Cont. & Defl. PC Bd. | Dual Tone Generator PC Bd. |
|                           | CPU/Memory PC Bd.          |

#### LOWER FLOOR MODULES

|                    |                |
|--------------------|----------------|
| S/A L.O.           | High Loop      |
| S/A I.F.           | Low Loop       |
| S/A R.F.           | Clock Divider  |
| 89-90 MHz Receiver | Delay Line     |
|                    | Low Loop Mixer |
|                    | FM Generator   |
|                    | Duplex Offset  |

Note: Thru Ser. No. 1406, a Diode Switch was included in the Upper Floor Modules. Ser. No. 1407 and on, the Diode Switch is part of the 1300 MHz Receiver Module.

Table 1-2 FM/AM-1500 Mechanical Structure

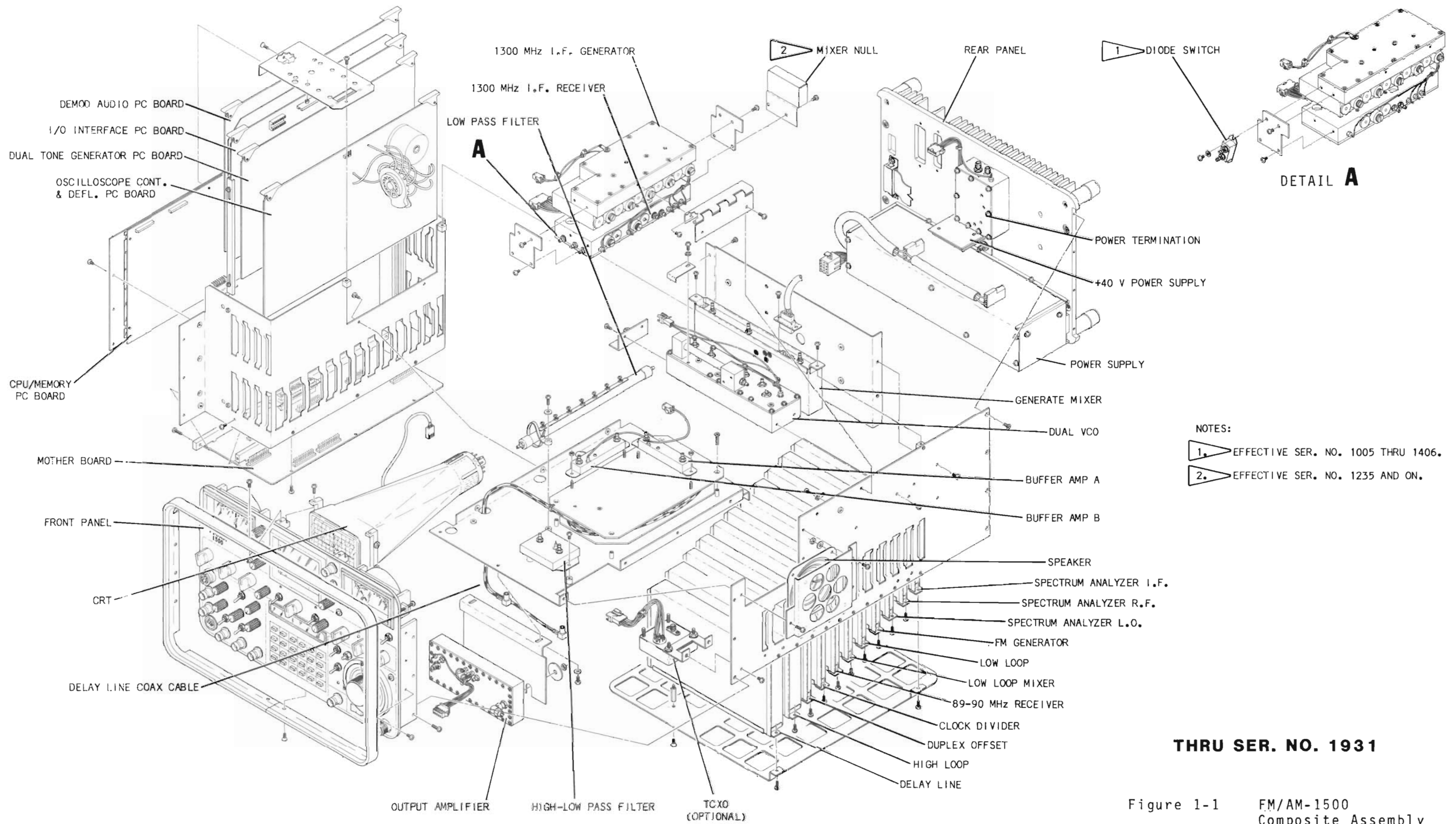
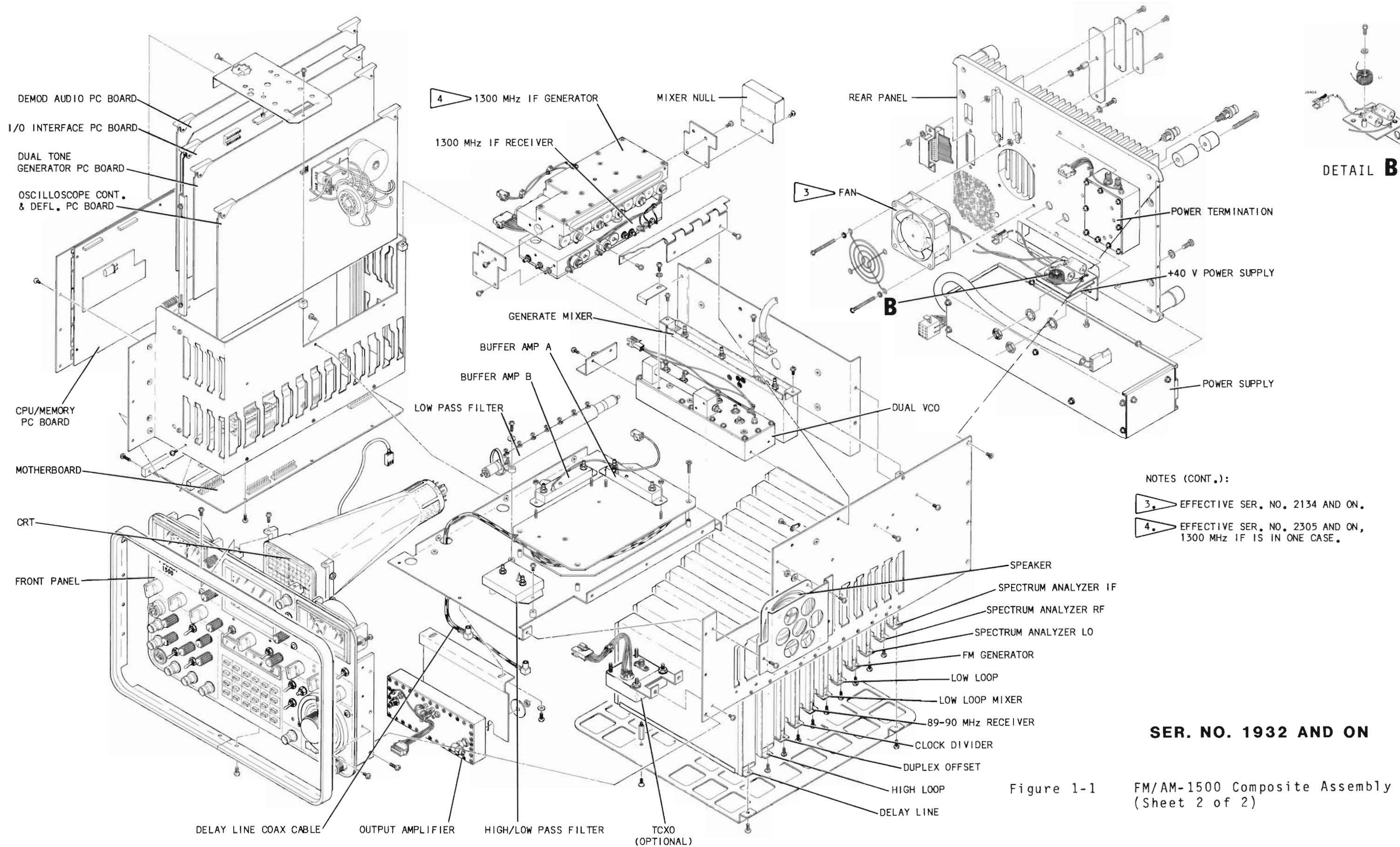


Figure 1-1 FM/AM-1500 Composite Assembly (Sheet 1 of 2)



DEMOD AUDIO PC BOARD  
 I/O INTERFACE PC BOARD  
 DUAL TONE GENERATOR PC BOARD  
 OSCILLOSCOPE CONT. & DEFL. PC BOARD

CPU/MEMORY PC BOARD  
 MOTHERBOARD

CRT  
 FRONT PANEL

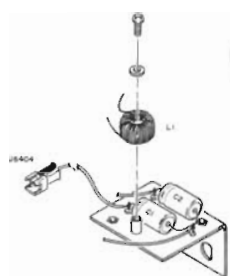
DELAY LINE COAX CABLE  
 OUTPUT AMPLIFIER  
 HIGH/LOW PASS FILTER  
 TCX0 (OPTIONAL)

4 1300 MHz IF GENERATOR  
 MIXER NULL  
 1300 MHz IF RECEIVER

GENERATE MIXER  
 BUFFER AMP A  
 BUFFER AMP B  
 LOW PASS FILTER

REAR PANEL  
 3 FAN  
 POWER TERMINATION  
 +40 V POWER SUPPLY  
 POWER SUPPLY  
 DUAL VCO

SPEAKER  
 SPECTRUM ANALYZER IF  
 SPECTRUM ANALYZER RF  
 SPECTRUM ANALYZER LO  
 FM GENERATOR  
 LOW LOOP  
 LOW LOOP MIXER  
 89-90 MHz RECEIVER  
 CLOCK DIVIDER  
 DUPLEX OFFSET  
 HIGH LOOP  
 DELAY LINE



DETAIL B

NOTES (CONT.):

- 3. EFFECTIVE SER. NO. 2134 AND ON.
- 4. EFFECTIVE SER. NO. 2305 AND ON, 1300 MHz IF IS IN ONE CASE.

**SER. NO. 1932 AND ON**

Figure 1-1 FM/AM-1500 Composite Assembly (Sheet 2 of 2)

# SECTION 2 - THEORY OF OPERATION

## 2-1 GENERAL

This section contains three levels of Theory of Operation and is organized as follows:

### 1. SYSTEM THEORY OF OPERATION

Paragraph 2-2 provides a simplified description of signal flow through the FM/AM-1500, for both signal generator and receiver operation. This description is based on the System Block Diagram shown in Figure 2-1.

### 2. FUNCTIONAL AND DETAILED THEORY OF OPERATION

Paragraphs 2-3 thru 2-9 provide a description of the major functional groupings in the FM/AM-1500. Following each discussion of a major function are detailed discussions of each module contained in the functional group just discussed. All functional groups are accompanied by block diagrams, as are the individual modules (where necessary).

## 2-2 SYSTEM THEORY OF OPERATION

### 2-2-1 GENERAL

The FM/AM-1500 is a microprocessor controlled, digitally synthesized communications service monitor. The receiver is a quadruple conversion, superheterodyne receiver, capable of monitoring communications signals within a range of 300 kHz to 999.9999 MHz. The signal generator is capable of generating modulated or unmodulated carrier signals within the range of 100 kHz to 999.9999 MHz, at an output level which is continuously variable from 0 to -128 dBm. (The output level may be increased up to +20 dBm with the use of an optional High Output Amplifier.) See Figure 2-1, FM/AM-1500 System Block Diagram.

### 2-2-2 RECEIVER OPERATION

The frequency of the signal to be received is determined by the FREQUENCY MHz setting of the LCD on the front panel. The input signal can be received at the TRANS/-40 dB DUPLEX Connector or at the ANTENNA Connector. If applied at the ANTENNA Connector, the received signal is sent to the 1300 MHz IF Receiver Module to begin up-conversion. If applied at the TRANS/-40 dB DUPLEX Connector, the received signal (if 100 mW or greater) is sent to the 1300 MHz IF Receiver Module at a -40 dB level.

In the 1300 MHz IF Receiver, the received signal is mixed with a VCO signal to produce a 1st IF of 1300 MHz. The signal is filtered and amplified, before again being mixed with a VCO signal to produce a 2nd IF of 90 MHz.



The 2nd IF is sent to the 89-90 MHz receiver and mixed with a Low Loop signal to produce a 10.7 MHz 3rd IF signal. The 3rd IF is mixed with a 10 MHz reference signal to produce the 4th IF of 700 kHz, which is fed to the audio processing portions of the set for demodulation and display on meters and readouts.

### 2-2-3 GENERATOR OPERATION

The frequency of the signal to be generated is determined by the FREQUENCY MHz setting of the LCD on the front panel. Signal Generation begins in the FM Generator, where an IF source signal, from either the Spectrum Analyzer LO or from the Low Loop, is mixed with a 10.7 MHz VCO signal to form a 1st IF of approximately 68.6 MHz. The 1st IF is mixed and converted, in the Generate Mixer, to a 90 MHz 2nd IF signal.

The 2nd IF is converted three times in the 1300 MHz IF Generator Module: first, to 1120 MHz, by mixing with a 1210 MHz High Loop signal; second, to 1250 to 1350 MHz by mixing with a 180 MHz injection frequency, which can be offset  $\pm 49.99$  MHz to create a generate duplex offset; and third, to 0-1000 MHz output signal by mixing with a 1300 to 2299 MHz High Loop signal.

The output signal is routed through the Output Amp and Power Termination Modules. It is output at the TRANS/-40 dB DUPLEX Connector and/or DUPLEX OUTPUT Connector, depending on mode of operation.

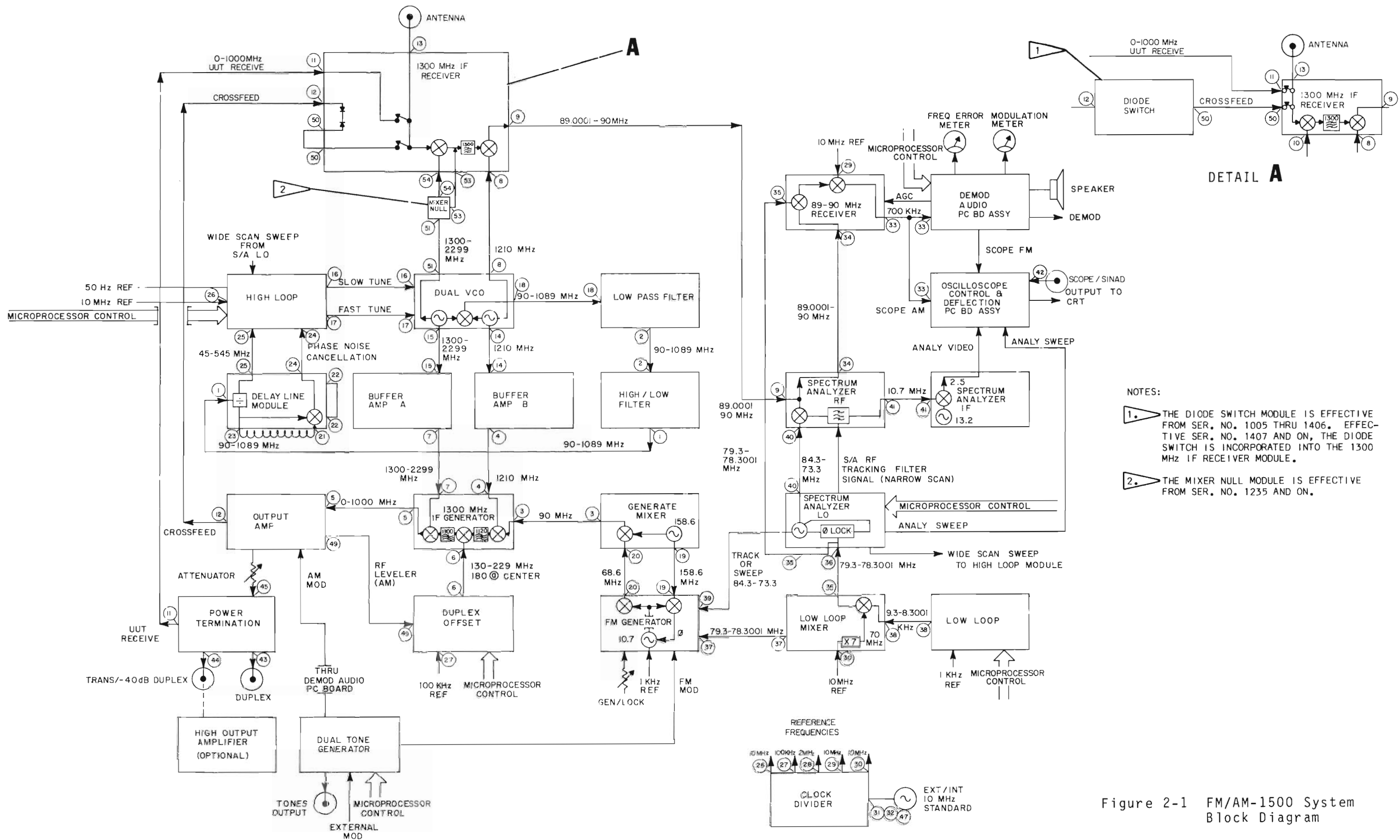


Figure 2-1 FM/AM-1500 System Block Diagram

- NOTES:
1. THE DIODE SWITCH MODULE IS EFFECTIVE FROM SER. NO. 1005 THRU 1406. EFFECTIVE SER. NO. 1407 AND ON, THE DIODE SWITCH IS INCORPORATED INTO THE 1300 MHz IF RECEIVER MODULE.
  2. THE MIXER NULL MODULE IS EFFECTIVE FROM SER. NO. 1235 AND ON.

## 2-3 POWER DISTRIBUTION FUNCTIONAL THEORY

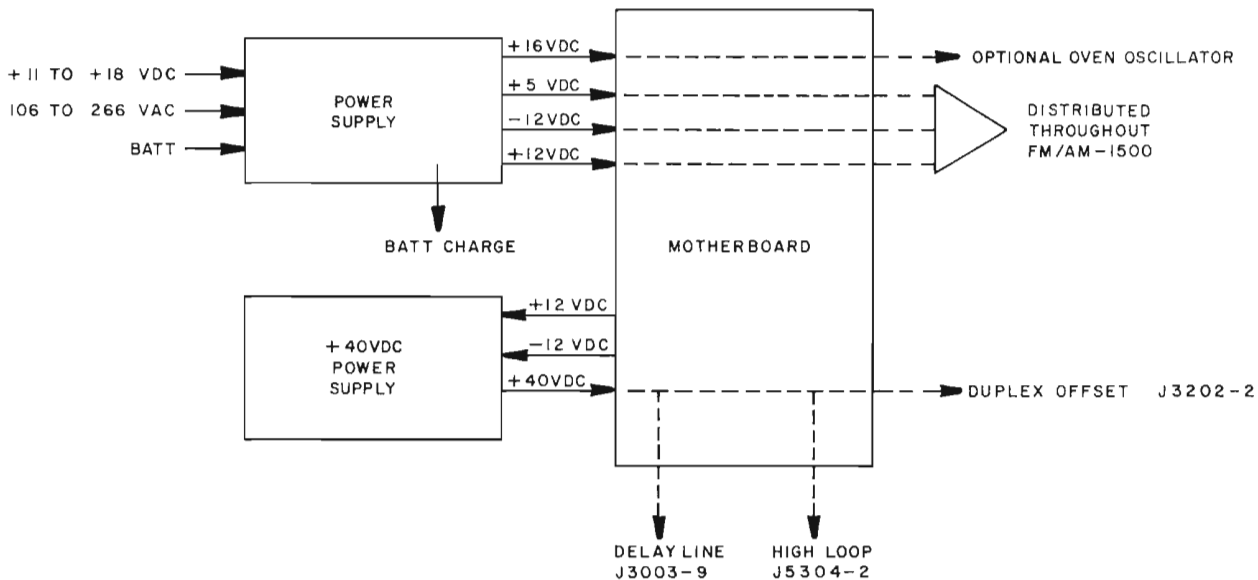


Figure 2-2 Power Distribution Functional Block Diagram

Power Distribution in the FM/AM-1500 is chiefly through the Mother Board. (See Figure 2-2). Power inputs to the Power Supply are converted to +5, +12, -12 and +16 VDC outputs. The +16 VDC output is available to power an optional Oven Oscillator (10 MHz standard, discussed in Frequency Reference Functional Theory). The remaining three outputs are distributed through the Motherboard to the individual modules, switches and controls throughout the FM/AM-1500. The +40 V Power Supply uses the +12 VDC and -12 VDC lines to develop a +40 VDC output which is distributed through the Motherboard to the High Loop Module, where it is used to develop tune voltages and to the Duplex Offset Module where it is used to control the tune voltages. The +40 V is also used by the Delay Line Module for phase-shift purposes.

## 2-3-1 Power Supply Module Detailed Theory

The Power Supply Module can operate on AC or DC (See Figure 2-3). The AC input can be 106 to 266 VAC and can be 50 to 400 Hz. The DC input can be an external 11 to 18 VDC source or it can be the internal battery source. When the front panel PWR/OFF/BATT Switch is set to PWR or to BATT, +12, +5 and -12 VDC voltages are output to the Motherboard. A +16 VDC output is also sent to the Motherboard where it is available to power an optional Oven Oscillator.

The AC Line voltage is filtered and rectified by T5801 and bridge rectifier BR5801. The output of the rectifier, several hundred volts DC, is filtered by C5803 and C5804. The negative output is floating common which serves the:

- 1st Trapezoid Oscillator
- 1st Comparator
- 1st Driver
- 1st MOS Switch
- Current Sense Resistors
- Fast Current Limiter
- Slow Current Limiter

### **WARNING**

THE DIFFERENCE OF POTENTIAL BETWEEN THE FLOATING GROUND AND CIRCUIT, OR CHASSIS, GROUND CAN EXCEED 300 V PEAK. THIS POTENTIAL CAN CAUSE SERIOUS INJURY OR EVEN DEATH. ALWAYS USE AN ISOLATION TRANSFORMER AND TAKE EXTREME CARE WHEN WORKING INSIDE THE POWER SUPPLY MODULE.

The several hundred volts DC out of the rectifier is applied to one end of the step-down transformer T5701 and to the +15 V floating regulator (Q5703 and Q5714). The +15 V floating regulator provides power for:

- 1st Trapezoid Oscillator
- 1st Comparator
- 1st Driver
- Opto Isolator
- Slow Current Limiter

The 1st Trapezoid Oscillator (U5701) produces a trapezoidal waveform which is applied to the positive side of the 1st Comparator (U5702). The negative side of the comparator is driven by the opto isolator U5709. The opto isolator provides a DC level which is controlled by the 1st Regulator (U5708). The output of the 1st Comparator is a rectangular wave whose duty cycle is controlled by the 1st Regulator. This rectangular wave is applied to the 1st Driver (Q5704 and Q5705) which provides the necessary drive current to give the first MOS Switch (Q5707) fast turn-on and turn-off characteristics.

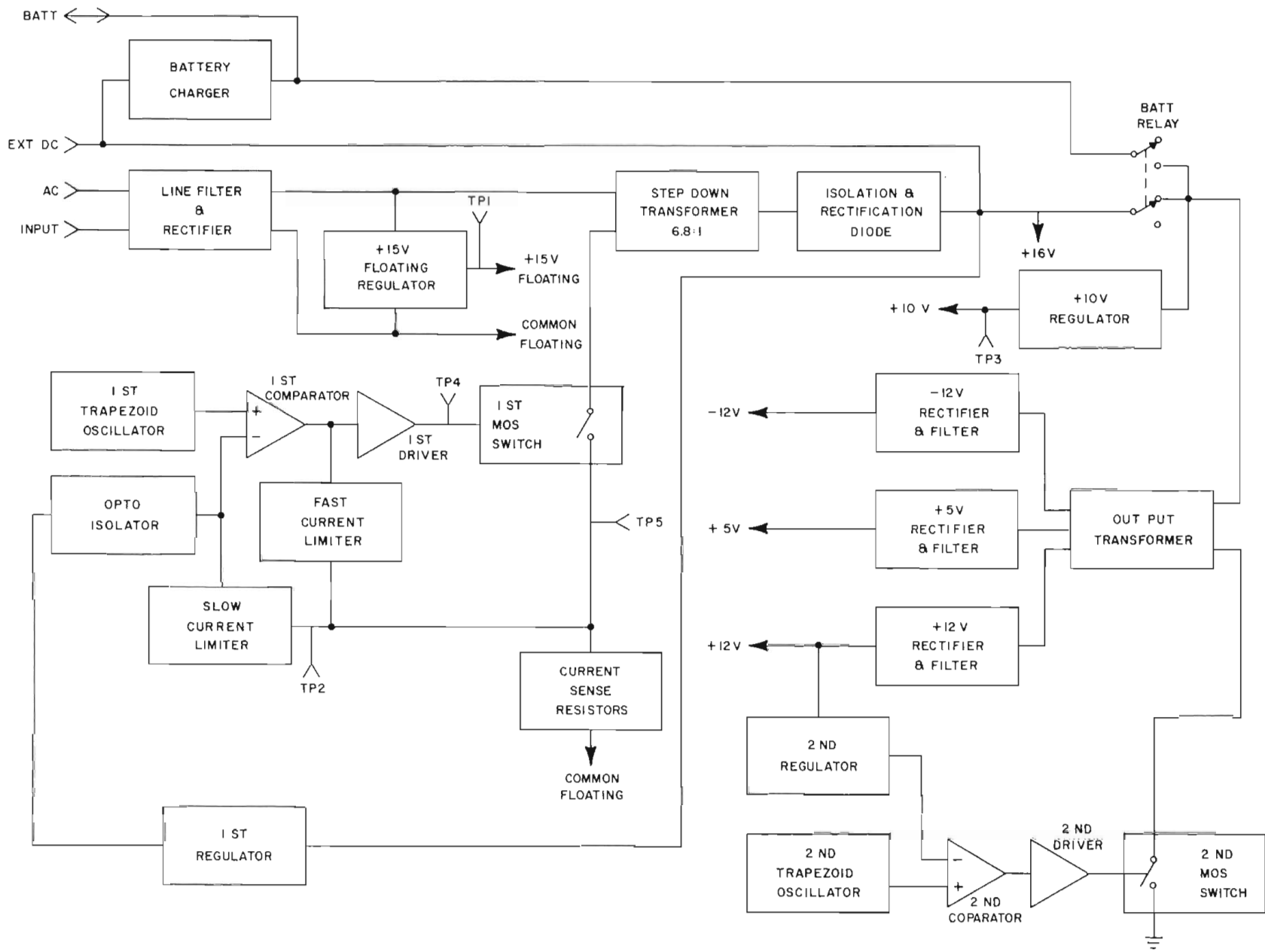


Figure 2-3 Power Supply Detailed Block Diagram

The 1st MOS Switch essentially grounds one side of the step-down transformer during the time that the rectangular wave from the 1st Driver is high. The output of the step-down transformer is rectified by the isolation and rectification diode CR5710. The output of the isolation and rectification diode is applied to the 1st Regulator which adjusts the output of the opto isolator and the duty cycle of the rectangular wave to produce +16 VDC at the output of the Isolation and Rectification Diode.

The current sense resistors, R5728 thru R5731, produce a voltage proportional to the current passing thru the 1st MOS Switch. This voltage is applied to the fast and slow current limiters. The fast current limiter (Q5711) reduces the output of the 1st Driver if the current exceeds approximately 5A. The fast current limiter limits the peak current. The slow current limiter (U5704) integrates the voltage sample from the current sense resistors and applies its output to the negative side of the 1st Comparator, which causes the duty cycle to be reduced if the average current thru the 1st VMOS Switch exceeds a pre-determined value.

The output of the Isolation and Rectification Diode is applied to the Battery Charger and to the Line Relay. The Battery Charger (U5703, Q5701, Q5702) provides 14.2 VDC to charge the internal 12 V battery. The Battery Charger also limits charging current to a safe level. Notice that external DC is also applied to the Battery Charger and to the Line Relay. When using external DC, the Isolation and Rectification Diode prevents the external DC from flowing thru the secondary of the step-down transformer. The battery is then charged by external DC (providing that the external DC is above approximately 13 VDC).

When the Line Relay (K5701) is energized, the output of the Isolation and Rectification Diode or external DC (whichever is applicable) is applied to the +10 V Regulator and to one side of the primary of the output transformer T5702.

#### **NOTE**

On FM/AM-1500 serial numbers 1142 and subsequent, the Line Relay (K5701) and its associated diode (CR5712) have been deleted. R5701 and CR5728 were added, thus making a solid state means of switching the FM/AM-1500 on and off. CR6001 was also added between pins 9 and 3 of J6003. For AC operation, a ground is applied to the junction of R5759 and CR5728, putting the 2nd Comparator (U5706) and the 2nd Driver (Q5712 and Q5713) into operation. For battery operation, a ground applied at pin 9 of J6003 closes relay K5702 and puts the internal battery on-line to supply DC current. CR6001 serves to ground the junction of R5759 and CR5728, to again place the 2nd Comparator and the 2nd Driver into operation. For DC operation, the 2nd Comparator is held high, causing the 2nd Driver and the 2nd MOS Switch (Q5708, Q5709 and Q5710) to be off.

When the Battery Relay (K5702) is energized, the battery voltage is applied to the +10 V regulator and one side of the primary of the output transformer. When the set is off, both the Battery and Line Relays are de-energized.

The +10 V Regulator (Q5706 and CR5714) supplies power for:

- 2nd Trapezoid Oscillator
- 2nd Comparator
- 2nd Driver
- 2nd Regulator

The 2nd Trapezoid Oscillator (U5705) produces a trapezoidal waveform which is applied to the positive side of the 2nd Comparator (U5706). The negative side of the 2nd Comparator is driven by the 2nd Regulator (U5707) which controls the DC level at the negative input and therefore the duty cycle of the output of the 2nd Comparator. The output of the 2nd Comparator is applied to the 2nd Driver (Q5712 and Q5713). The 2nd Driver supplies the necessary current to give the 2nd MOS Switch fast turn-on and turn-off characteristics. The 2nd MOS Switch (Q5708, Q5709, and Q5710) grounds the other side of the primary of T5702 when the output of the 2nd Driver is high. T5702 has three secondaries which are rectified to produce +12, -12, and +5 VDC. The output of the +12 V rectifier is applied to the 2nd Regulator which adjusts the duty cycle of the Comparator to produce +12 V at the output of the +12 V rectifier.

### 2-3-2 +40 V Power Supply Module Detailed Theory

The +40 V Power Supply converts +12 and -12 VDC inputs to an output voltage of approximately +40 volts (See +40V Power Supply Schematic in Section 7 of this Manual). U5601 is an astable multivibrator of approximately 39 kHz, creating a square wave from the outputs of Q5602 and Q5603. The 24 Vp-p square wave is applied to the voltage doubler of CR5601, CR5602, CR5603 and CR5604. The output of the voltage doubler is approximately +40 VDC.

## 2-4 FREQUENCY STANDARD FUNCTIONAL THEORY

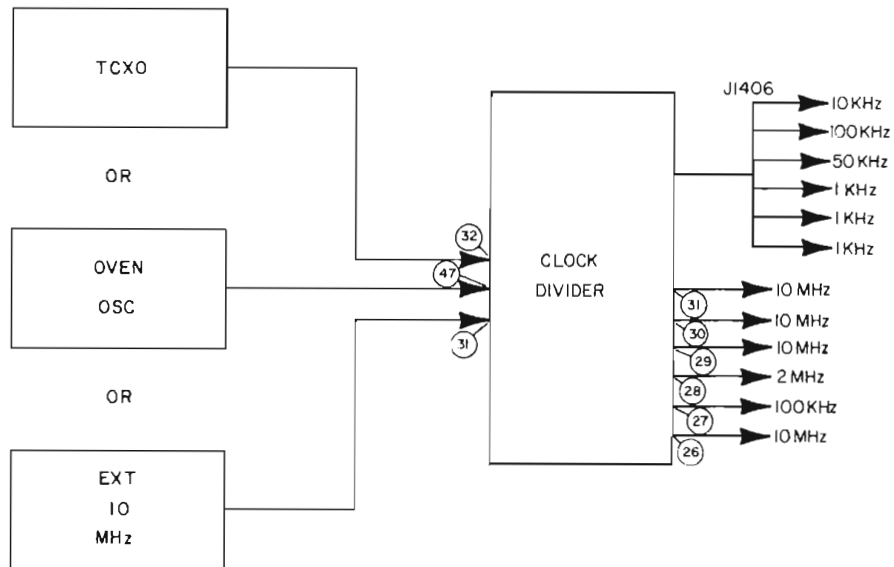


Figure 2-4 Frequency Standard Functional Block Diagram

The 10 MHz reference standard used in the FM/AM-1500 may be one of three sources (See Figure 2-4): an optional TCXO (Temperature Compensated Crystal Oscillator), an optional Oven Oscillator or an external 10 MHz standard (input through 10 MHz REF Connector on the rear panel). Regardless of whether or not an internal 10 MHz standard is installed, the FM/AM-1500 will switch over to the external 10 MHz standard, if connected. The 10 MHz standard is input to the Clock Divider Module where it is converted to the reference frequencies used by other modules of the FM/AM-1500.



## 2-4-1 Clock Divider Module Detailed Theory

The 10 MHz internal standard signal is input at J1401 and sent through Q1701 when its base is biased high (See Figure 2-5). Transistors Q1704 and Q1706 buffer the 10 MHz sent to the individual driver transistors. Transistor Q1705 provides a 10 MHz test signal of approximately 0.8 Vp-p which is available at the 10 MHz REF Connector on the rear panel.

When an external 10 MHz TTL signal of approximately 2 Vp-p or greater is input from the 10 MHz REF Connector on the rear panel, it is input at J1402 and detected at CR1701. U1701 will then switch off the internal input at Q1701 and switch the external signal through at Q1702 to the buffer transistors. Transistor Q1714 will also conduct, causing the EXT REF Indicator Lamp on the front panel to illuminate.

The 10 MHz signal is split and buffered by Q1704, then output through Q1708 to J1404 for use by the 89-90 MHz Receiver and through Q1709 to J1402 for use by the High Loop PC Board.

The output of Q1706 goes to Q1705, Q1707 and Q1713. Q1713 buffers the output to J1403 for use by the Low Loop Mixer module. When the external reference is not used, Q1705 buffers the 10MHz to J1402. Q1707 buffers the 10 MHz to Q1710, where it is amplified to a level needed by U1702A. U1702, U1703 and U1704 each contain two "Divide-by-Two" and two "Divide-by-Five" circuits. Table 2-1 shows the input and output pins for each frequency. U1705 buffers the divider output before sending it to the CPU and the optional GPIB.

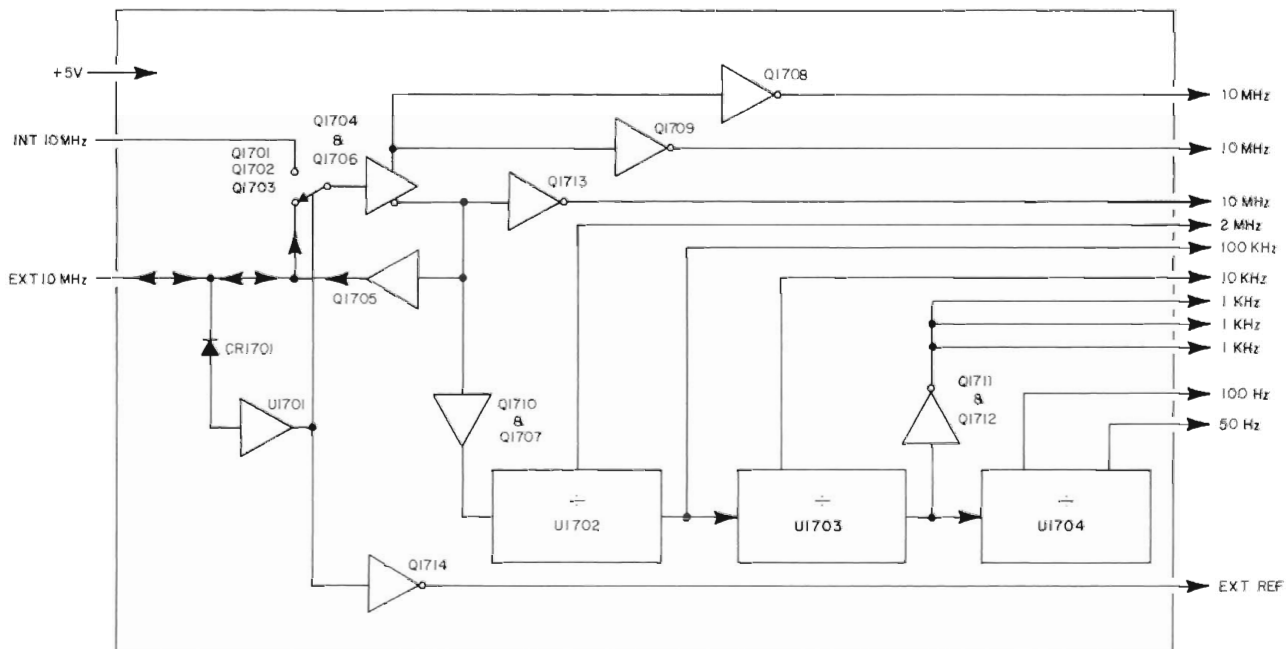


Figure 2-5 Clock Divider Detailed Block Diagram

| IC    | INPUT   | PIN (FROM)<br>/PIN (TO) | FACTOR | OUTPUT<br>FREQUENCY |
|-------|---------|-------------------------|--------|---------------------|
| U1702 | 10 MHz  | 4/1                     | 5      | 2 MHz               |
|       | 2 MHz   | 6/3                     | 2      | 1 MHz               |
|       | 1 MHz   | 15/13                   | 2      | 500 kHz             |
|       | 500 kHz | 12/10                   | 5      | 100 kHz             |
| U1703 | 100 kHz | 4/1                     | 5      | 20 kHz              |
|       | 20 kHz  | 6/3                     | 2      | 10 kHz              |
|       | 10 kHz  | 15/13                   | 2      | 5 kHz               |
|       | 5 kHz   | 12/10                   | 5      | 1 kHz               |
| U1704 | 1 kHz   | 4/1                     | 5      | 200 kHz             |
|       | 200 Hz  | 6/3                     | 2      | 100 kHz             |
|       | 100 Hz  | 15/13                   | 2      | 50 Hz               |

Table 2-1 Clock Divider Frequencies (U1702, U1703, U1704)

## **2-5 FREQUENCY SYNTHESIS FUNCTIONAL THEORY**

The Frequency Synthesis Functional Block is divided into two major sections: High Loop and Low Loop (See Figure 2-6).

### High Loop Section

The function of the High Loop Section is to phase-lock the two VCO's in the Dual VCO Module with a 10 MHz reference frequency that is input into the High Loop Module. The High Loop Section consists of the following modules:

- High Loop
- Dual VCO
- Low Pass Filter
- High/Low Pass Filter
- Delay Line
- Buffer Amplifiers A & B

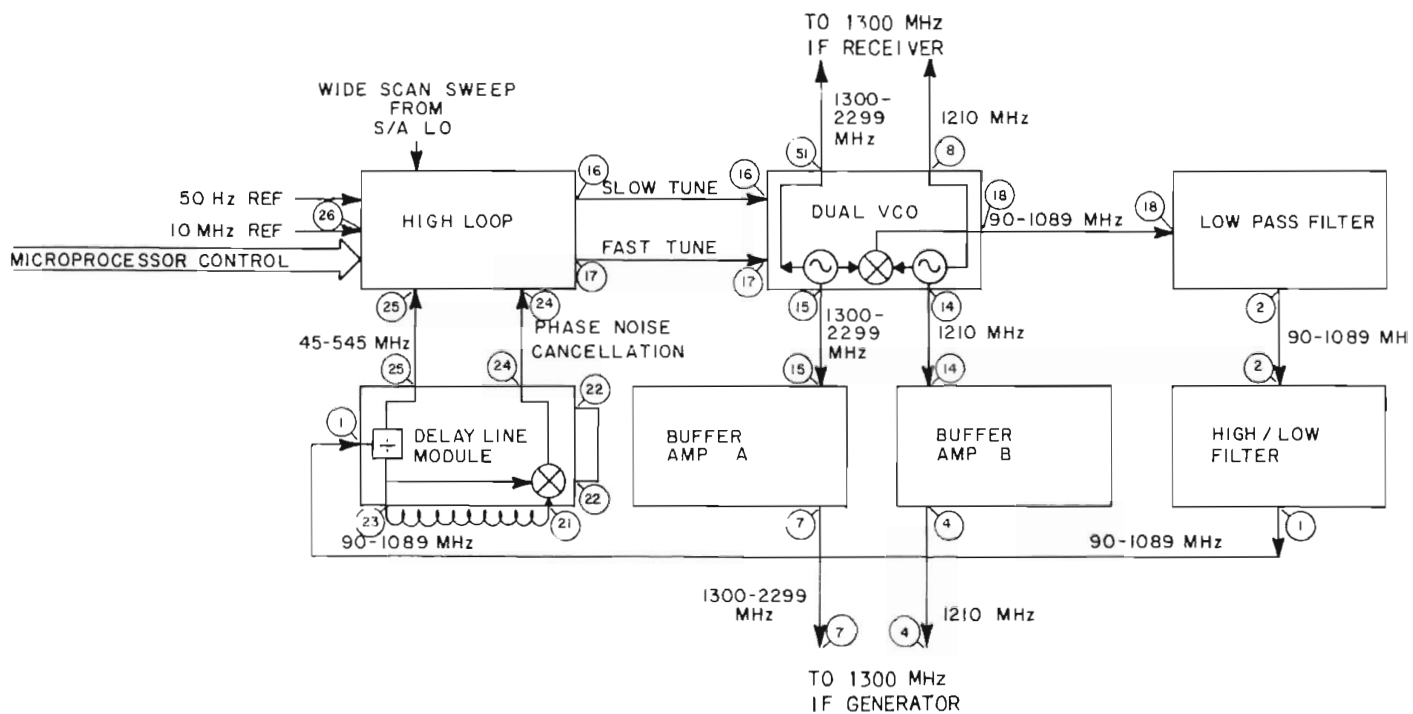
Failure of any of these modules will result in the failure of High Loop Section.

### Low Loop Section

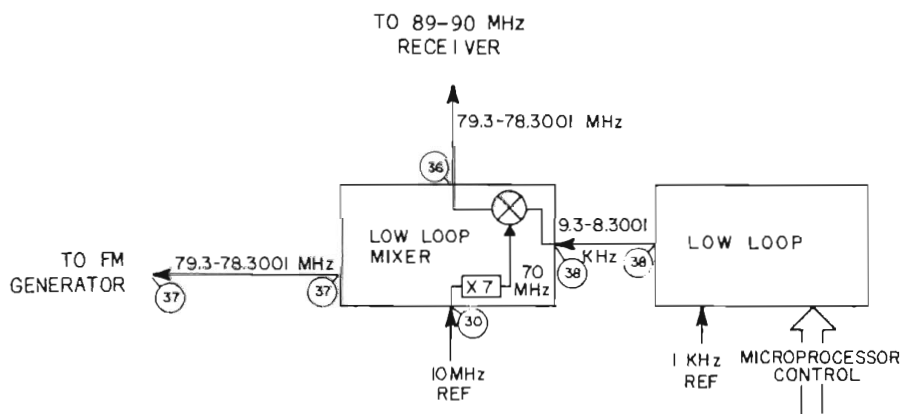
The function of the Low Loop Section is to phase-lock the frequency generated by the four lower digits of the RF frequency setting on the front panel with the VCO in the Low Loop Module. The resulting phase-locked frequency will then be fed to the Generator Functional Block, the Spectrum Analyzer Functional Block and to the Receiver Functional Block. The Low Loop Section consists of the following modules:

- Low Loop
- Low Loop Mixer

Failure of any of these modules will result in the failure of the Low Loop Section.



HIGH LOOP SECTION



LOW LOOP SECTION

Figure 2-6 Frequency Synthesis Functional Block Diagram

## 2-5-1 High Loop Module Detailed Theory

### General

The High Loop Module provides phase-locked frequency control of the Dual VCO Module as the operating frequency is selected between 000 and 999 MHz (the three upper digits of the selected frequency). Operation of the High Loop Module can be divided into two major sections: the normal phase-lock loop, and the wide scan mode. These modes are controlled by the setting of the front panel ANALY DISPR Control. Settings from 1 K thru 1 M are "normal". Settings from 2 M thru FULL are "wide scan". In normal settings, the system goes into a fixed mode of operation, placing the 1300-2300 MHz VCO (in the Dual VCO Module) on the commanded frequency. In wide scan settings, the 1300-2300 MHz VCO is swept and slaved to the analyzer sweep, and is centered about the commanded frequency. (See Figure 2-7 and the High Loop Schematic in Section 7 of this manual.)

### NORMAL (FIXED) MODE

#### Programmable Divider Circuit

The 45 to 545 MHz frequency from the Delay Line Module enters at J2801 on the digital board to drive the programmable divider circuit and a fixed divider chain. IC's U2201, U2202, U2203, U2204 and associated components form the programmable divider. The programmable divider operates from 45 - 544 counts, depending on the frequency selected on the keypad. IC's U2201 and U2202 operate as a  $\div 10/\div 11$  swallow counter. U2201 will divide by 11 until U2202 reaches zero count. At zero count, pin 14 of U2213A goes high, stopping U2202 from counting, and pulling pin 2 of U2201 high. U2201 will now divide by 10 until the next load condition.

The output of U2201, pin 8, synchronously clocks down the divider chain. When U2203 and U2204 have counted down through counts 00 to 99, flip-flop U2205A will be set, enabling the end-of-counts gate at pin 13 of U2213C. Forty-five more counts are needed to clear the counter. When counter U2203 has counted down to two counts before zero, pin 10 of U2205B is enabled. The next clock pulse at pin 11 of U2205B will set the flip-flop, causing a new number to be loaded into the programmable dividers. Flip-flop U2205A is reset at pin 1, and then pin 10 of U2205B is returned to a low condition. The next clock pulse at pin 11 of U2205B will clear the flip-flop and end the load condition to begin a new count cycle. The output frequency of the programmable divider should be 500 kHz. The 500 kHz signal is sent to an ECL to TTL level translator composed of Q2219 and Q2220. The TTL output at the collector of Q2220 is buffered by U2214A. The output of U2214A is sent to the Frequency Comparator and Phase Correction Circuits, and also sent to a  $\div 10,000$  circuit to develop a 50 Hz reference signal used in the wide scan mode (to be discussed later).

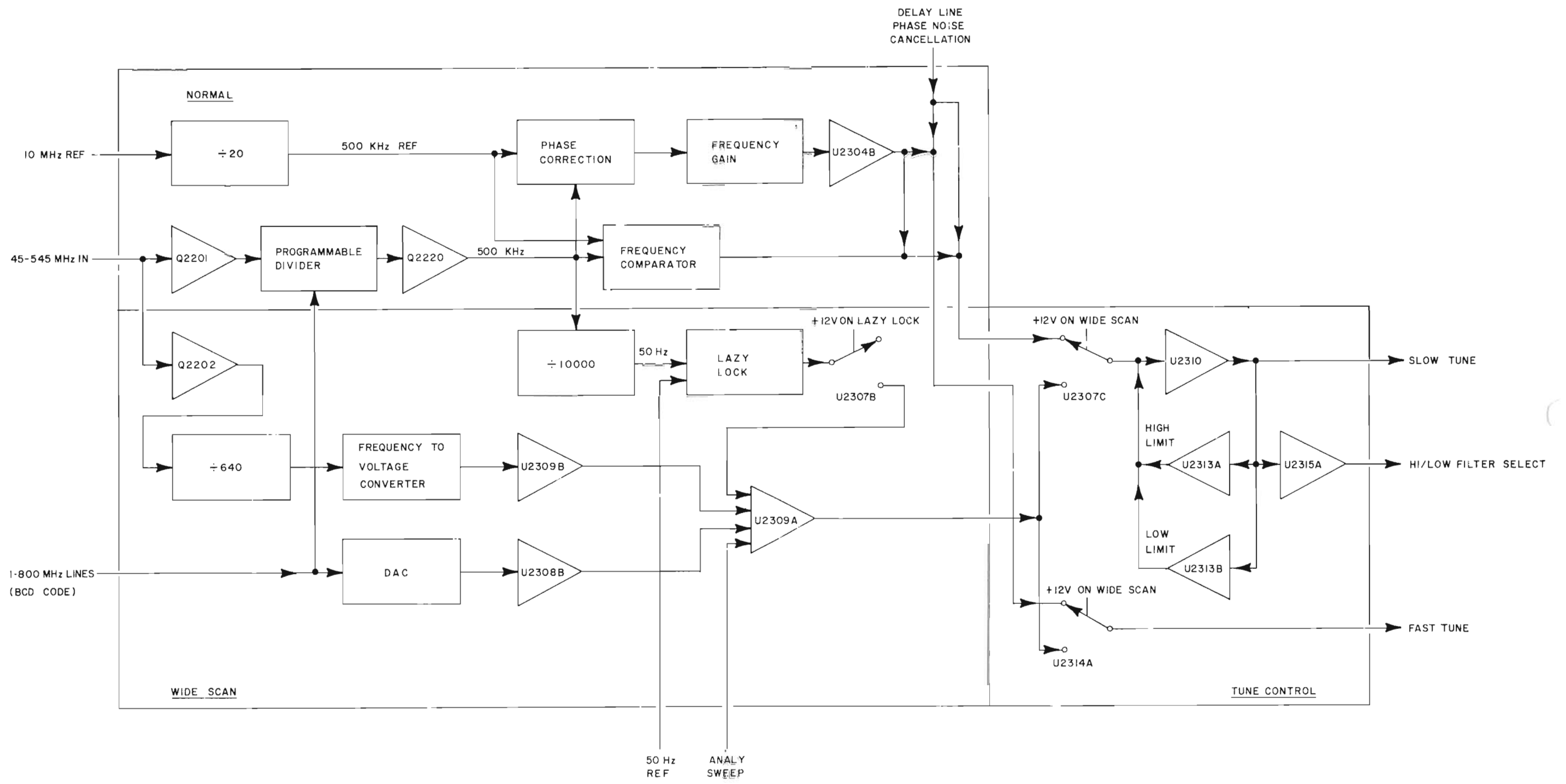


Figure 2-7 High Loop Detailed Block Diagram

## Frequency Comparator Circuit

A 10 MHz reference input at J2802 is divided by two in U2209A and then by 10 in U2210 to yield a 500 kHz reference frequency. When wide scan (2M, 5M, 10M and full positions of the front panel ANALY DISPR Control) is selected, Q2203 is turned on to disable U2209A by pulling pin 6 low. This removes the reference frequency from the circuit for tracking analyzer operation.

The frequency comparator system is composed of U2211A, U2211B, U2214C, CR2209, CR2210, C2230 and U2215B. The reference 500 kHz is presented to U2211B (pin 5) and the divider chain output is presented to U2211A (pin 1). If the frequency at U2211A is less than 500 kHz, U2211B (pin 8) will be discharging the voltage at C2230 (through CR2210). A low voltage at U2215B (pin 5) will force the output (pin 7) low. Similarly, if the frequency at U2211A is greater than 500 kHz, U2211A (pin 12) will be charging C2230 through CR2209, and U2215B (pin 7) will be forced high.

If both frequencies at U2211A and U2211B are 500 kHz (normal phase lock condition), U2211A (pin 12) and U2211B (pin 9) will both be high, enabling gate U2214C which resets U2211A and U2211B. During this condition, U2211A (pin 12) and U2211B (pin 8) will be equal and opposite, maintaining a static condition at C2230 and approximately zero volts at the output of U2215B (pin 7).

When the set periods of U2211 are not equal, C2229 will charge up and pull up on the base of Q2218 to indicate an out of phase-lock condition. However, if wide scan is selected, Q2221 will turn on and Q2218 will turn off to disable CR2225 and to supply a +12 V signal to the LOCK Logic on the Demod Audio PC Board.

The control voltage developed by the frequency comparator goes to the Analog board through E1 (pin 4) to a diode network (CR2302, CR2303, CR2304 and CR2305). This network is activated when the control voltage moves 2 diode gaps either positive or negative from its normal zero reference. This circuit exists so that the frequency comparator cannot prematurely take control of the High Loop. This allows an extremely limited amount of frequency tuning to be done through the 1210 MHz oscillator (fast tune line). Output from this network is summed through R2344 at U2307C (pin 12) with the frequency gain information, and with a phase noise cancellation from the Delay Line (through R2345).

## Phase Correction Circuit

The first sample and hold circuit is composed of Q2208, Q2209, Q2210 and Q2213. C2225 is the hold capacitor. The reference 500 kHz is buffered by Q2208 and presented to Q2209 and Q2210. The 500 kHz programmable divider output is presented to Q2213 which develops a sample pulse. The sample pulse controls the conduction of Q2209 and Q2210. Sampling at the peak (or high condition) results in Q2209 being turned off and Q2210 being turned on, increasing the voltage on C2225. Sampling at the low point of the 500 kHz results in Q2210 being turned

off and Q2209 on. The collector voltage at Q2209 pulls down, decreasing the voltage at C2225. The increasing or decreasing voltage at C2225 slews the Dual VCO frequency such that the sampling pulse occurs at the 500 kHz transition point, achieving the phase lock condition.

The voltage at C2225 is buffered by Q2212 and Q2307 (on the analog board) and presented to the second sampler Q2203. The second sample pulse is developed through Q2214 and Q2301 (on the analog board). These two transistors provide a fixed delay to separate the second sample pulse away from the first sample pulse. When the gate of Q2303 goes high, voltage at the source is coupled to the drain and held by C2321 (the second hold capacitor). Q2302 provides a signal 180° out of phase with the signal at Q2301 and is coupled through C2305 to C2321 to null 500 kHz transition noise. The voltage at C2321 goes to U2304A where gain is adjusted such that zero volts occur at the output of U2304A (pin 1).

### Frequency Gain Circuit

The output of U2304A is presented to the frequency gain circuit which is composed of switches U2305A, U2305B, U2305C, U2306A, U2306B and U2306C. The switches are controlled by the 6 frequency select lines (from 40 MHz through 800 MHz). The gain of op-amp U2304B is controlled by the resistance ratios of the frequency gain control, along with R2341 and R2340.

The output of U2304B (pin 7) is summed, through R2345, with the frequency comparator and the phase noise cancellation from the Delay Line at U2307C (pin 12). The output of U2304B (pin 7) is also presented to U2314A (pin 2) where it is summed with phase noise cancellation from the Delay Line. Operation of U2314A is similar to U2307C in that it is switched according to the wide scan control line. The output of U2314A goes to the fast tune line (J2805).

### WIDE SCAN MODE

In the wide scan condition, the VCO is swept such that the average center frequency is maintained by the High Loop Module and the sweep width is controlled by the dispersion setting of the Spectrum Analyzer.

The slow tune voltage and a limited amount of fast tune voltage on wide scan can be the sum of 4 signals. One source is the frequency to voltage converter. Another source is the frequency find signal from the DAC's. A third source is the tracking analyzer sweep ramp voltage. A fourth is the lazy lock signal except it is not active in the full scan condition.

### ±640 Circuit

Q2202 and Q2203 are switched on by the +12 V in wide scan. Q2203 pulls the reset line of U2209A low, removing the 500 kHz reference signal. This disables the frequency comparator and phase correction circuits of the normal (fixed) phase lock system.



The 45-545 MHz input from the Delay Line Module is buffered by Q2202 and sent to a fixed divider circuit composed of U2206, U2207 and U2208. Q2204 and Q2205 translate the output of U2207 from ECL to TTL. The output of Q2205 clocks U2208.

#### Frequency to Voltage Converter Circuit

The frequency to voltage converter relative to the commanded DAC voltage is analogous to the frequency detector of the normal (fixed) mode of operation. It is responsible for steering the frequency of the 1300-2300 MHz VCO over a wide range.

The output of U2208 is conditioned by Q2206 and Q2207 into a sharply defined square wave. The upward transition of the square wave turns on Q2216, and a current proportional to the frequency is supplied to C2220 and R2240. Q2215 limits the lower control voltage on the emitter of Q2216 to approximately 6.2 V. The upward limits on the emitter of Q2216 are controlled by its base being held to about 6 V. The output voltage of this circuit is approximately 0-5 V (when the ANALY DISPR Control is in FULL). The output voltage is fed to U2309 for amplitude adjustment and then fed through R2356 to be summed with other correction voltages at U2309B (pin 6) for wide scan operation.

#### DAC Circuit

The 1-800 MHz (BCD coded) lines are converted in DAC's U2301, U2302 and U2303 to a control voltage for the tune lines. The output currents of the DAC's are summed at U2308B (pin 6). R2330 is provided for gain adjustment (according to the center frequency). The resulting voltage out of U2308B (pin 7) is fed through R2231 to U2309B (pin 6) for summing with the other correction voltages. The voltage is normally positive in approximately the same magnitude as the average negative contribution from U2309A.

#### Tracking Analyzer Sweep Ramp Voltage

The S/A sweep ramp voltage is input at pin 24 of J2803, from the Spectrum Analyzer L.O. Module. The voltage is routed through R2375 for summation at U2309B (pin 6).

#### Lazy Lock Phase Detector Circuit

The lazy lock information is analogous to the phase detector information in the normal (fixed) mode. It is responsible for maintaining the center frequency in a phase-locked condition.

The "Lazy lock" contribution begins with the 500 kHz output of the divider chain of the normal (fixed) mode. This output is buffered by U2214A and divided by two at U2209B. The TTL output of U2209B is converted to CMOS level by Q2217 and divided by 5000 by U2212. When the count reaches 50 Hz at pin 2, U2216 is enabled, resetting U2212. This 50 Hz signal is presented to U2311 on the analog board, where it is compared with the 50 Hz reference signal coming from the Clock Divider

module. The error signal at U2311 (pin 13) is filtered through R2364, C2325 and R2365 to an average DC level. A gain adjust circuit, controlled by U2307A and Q2304, which parallel R2378, R2379 and C2322 with the filter, is enabled when the 400 MHz or 800 MHz line is selected. The average correction voltage is integrated by U2308A and fed to U2307B (pin 4) through R2377. U2307B is controlled from the +12 V lazy lock line developed in the Spectrum Analyzer L.O. assembly. This line will go low only in the FULL setting of the ANALY DISPR Control. The voltage correction from the lazy lock is fed through U2307B and summed directly at U2309B (pin 6).

The resultant output voltage of the summed inputs to U2309B is fed to the fast tune and slow tune switches (U2314A and U2307C respectively). The diode network of CR2311 and CR2309 allow a faster resetting of the slow tune voltage to the sweep start condition. In wide scan, pins 13 and 14 of U2307C are connected to integrator U2310 and Q2306 and to the slow tune line. Also, pins 1 and 15 of U2314A are connected allowing wide scan information to the fast tune line.

### Output Selection

U2307C is a FET switch whose control line is pin 11. In the normal (fixed) mode, pin 11 is low connecting pins 12 and 14. When wide scan is selected, pin 11 is high connecting pins 13 and 14. The control voltage at pin 14 of U2307C is presented to a system composed of an Integrator (U2310, Q2306 and C2323) a high and low limiter (U2313A and U2313B) and a switch control for the Hi/Lo Pass Filter (U2315A).

When a high condition is sensed at U2310A (pin 2), the output of U2310A (pin 1) pulls down, increasing conduction through Q2306 and lowering the collector voltage which is fed through R2354 to the slow tune line (J2806).

When the low condition is sensed at U2310A (pin 2), the output goes high, reducing conduction through Q2306, and allowing the collector voltage to increase.

The limiting circuit is used to prevent the 1300-2300 MHz VCO from being driven either too high (above 2330 MHz) or too low (below 1275 MHz). When the integrator commands the VCO to go to a frequency above 2330 MHz (U2310A, pin 2, senses low voltage), U2313A (pin 1) goes positive. This positive voltage sums at U2310A (pin 2) through CR2207 and R2350 to prevent the integrator from further increasing the slow tune voltage. This voltage is set according to the individual VCO requirements by R2372. Similarly, a too high condition at U2310A (pin 2) will force U2313B (pin 7) down, limiting further decreasing of the slow tune voltage. This limit is set by R2373.

Switching of the Hi/Lo Pass Filter Module occurs at the specific frequency required by the Hi/Lo Pass Filter and is set by R2387 to switch at + or -10 V.

## 2-5-2 Dual VCO Module Detailed Theory

### **NOTE**

The Dual VCO Module is designated by IFR Systems, Inc. as being non-repairable in the field. It should be returned to the factory for repair.

The Dual VCO Module supplies the first and second L.O. signals to the 1300 MHz IF Receiver and the 1300 MHz IF Generator Modules, as controlled by the High Loop Module. (See Figure 2-8 and the Dual VCO Schematic in Section 7 of this Manual).

#### First VCO

The first VCO frequency of 1300 to 2299 MHz is controlled by the slow tune line input at J2406 from the High Loop Module. The tune voltage can vary from 0 to +40 V, depending on the frequency selected. The +12 V power applied at FL2401 is subregulated to approximately +11 V at Q2101 for the oscillator transistor, Q2102. Q2103 and Q2104 amplify the oscillator signal for a +7 to +12 dBm output at J2404 to the 1300 MHz IF Receiver. Q2105 and Q2106 amplify the oscillator signal for a +7 to +12 dBm output at J2405 to the Output Buffer A module. Q2107 and Q2108 amplify the oscillator signal for a +7 to +12 dBm signal to MXR2401.

#### Second VCO

The second VCO frequency of 1210 MHz is controlled by the fast tune line input at J2403 from the High Loop Module. The +12 V power applied at FL2402 is subregulated to approximately +11 V at Q2001 for the oscillator transistor, Q2002. Q2003 and Q2004 amplify the oscillator signal for a +7 to +12 dBm signal output at J2401 to the Output Buffer B Module. Q2005 and Q2006 amplify the oscillator signal for a +7 to +12 dBm signal output at J2402 to the 1300 MHz IF Receiver Module. Q2007 and Q2008 amplify the oscillator signal for a +7 to +12 dBm signal to a 1400 MHz low-pass filter, FL2403. The second harmonic of 1210 MHz is eliminated by FL2403.

The two VCO signals are mixed in MXR2401 to produce a difference frequency of 90 to 1089 MHz, which is output at J2407 to the Low Pass Filter Module.

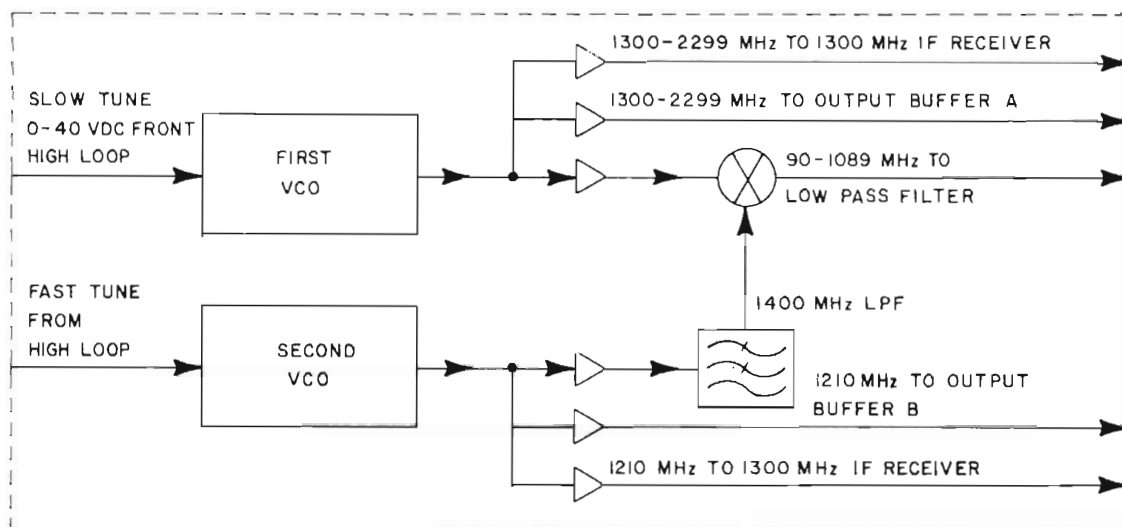


Figure 2-8 Dual VCO Detailed Block Diagram

### 2-5-3 Low Pass Filter Module Detailed Theory

The Low Pass Filter Module is a tubular, in line low-pass filter connected between the Dual VCO Module and the High/Low Pass Filter Module. The Low Pass Filter must pass 90-1089 MHz, and attenuate the 1210 MHz signal by approximately 40 dB (See the Low Pass Filter Mechanical Assembly Detail in Section 6 of this Manual.)

### 2-5-4 High/Low Pass Filter Module Detailed Theory

The High/Low Pass Filter Module is controlled from the High Loop Module to act as either a high-pass or low-pass filter. The 90-1089 MHz signal from the Low Pass Filter Module is input at J601. If the control line at FL601 is approximately +10 V, the module acts as a high-pass filter from approximately 450 MHz to 1089 MHz. If the control line at FL601 is approximately -10 V, the module acts as a low pass filter from 90 to 520 MHz. The crossover frequency varies from module to module, but is marked on the outside of each module as calibrated at the factory. (See the High/Low Pass Filter Schematic in Section 7 of the Manual.)

#### **NOTE**

The actual crossover frequency to be used in calibration is 90 MHz less than the frequency marked on the module. This is because the actual operating frequency is 90 MHz above the frequency selected on the Keyboard.

## 2-5-5 Delay Line Module Detailed Theory

The Delay Line Module creates a residual component cancellation signal to clean the High Loop Section Composite Spectrum. It also divides the 90-1089 MHz signal from the Dual VCO by two for input to the High Loop Module. (See Figure 2-9 and the Delay Line Schematic in Section 7 of this Manual.)

### RF Source

The 90-1089 MHz RF input at J3005 is amplified by U2601, U2602 and U2603 to drive U2604 as a divide-by two. One 45-545 MHz signal, out of pin 10 of U2604 is output at J3006 to the High Loop Module.

The RF source for the phase control circuitry is switched from two sources. A +5 V control line (if 455 MHz or greater is selected on the Keyboard) at pin 5 of J3003 enables the output of pin 11 of U2604 (90-545 MHz) to be the source. If the +5 V control line goes to 0 V (when 454 MHz or less is selected on the Keyboard), the source is pin 4 of U2603.

The selected RF source (90-544 MHz if 0-454 MHz is selected on the keyboard, or 228-499 MHz if 455-999 MHz is selected on the keyboard) then splits in two directions. The RF in one direction is amplified by Q2602 and Q2601 and output from J3007 on Board #2 through the Delay Line Coax Cable (75' of coax) to J3001 on Board #1. The RF in the other direction is amplified by Q2603 and Q2604, and then low-pass filtered in selectable filters, as controlled by U2501. The output at J3008 is then sent through a jumper coax to J3002 on Board #1.

### Phase Shift Circuit

The jumpered input at J3002 is amplified by Q2509 and sent to one port of MXR2501. The input signal at J3001, through the Delay Line Coax Cable, is amplified in a series of amplifiers which includes two stages of phase shifting (Q2403 and Q2405). As the voltage on varactor diodes CR2403 and CR2404 is varied (SW2501 switches between integrator control or manual control, for test purposes) from 0-30 V, the impedance of the varactors becomes significantly smaller or significantly larger than R2515 and R2523, respectively. This produces a theoretical phase shift of  $180^\circ$  per stage of phase shifting (although realistic limitations won't permit this). The output of the amplifiers is subsequently low-pass filtered in selectable filters, as controlled by U2501. The output of the filters is amplified by Q2508 and sent to an input port of MXR2501. The phase difference between the two inputs to MXR2501 is  $90^\circ$  or  $270^\circ$ , depending on which way K2502 is set by the integrator circuit.

### Differential Amplifier Circuit

The differential amplifier consists of Q2519, Q2520, Q2521 and Q2522. The gain of the differential amplifier is increased through relay K2501, if 455 MHz or greater is selected. The integrator circuit will

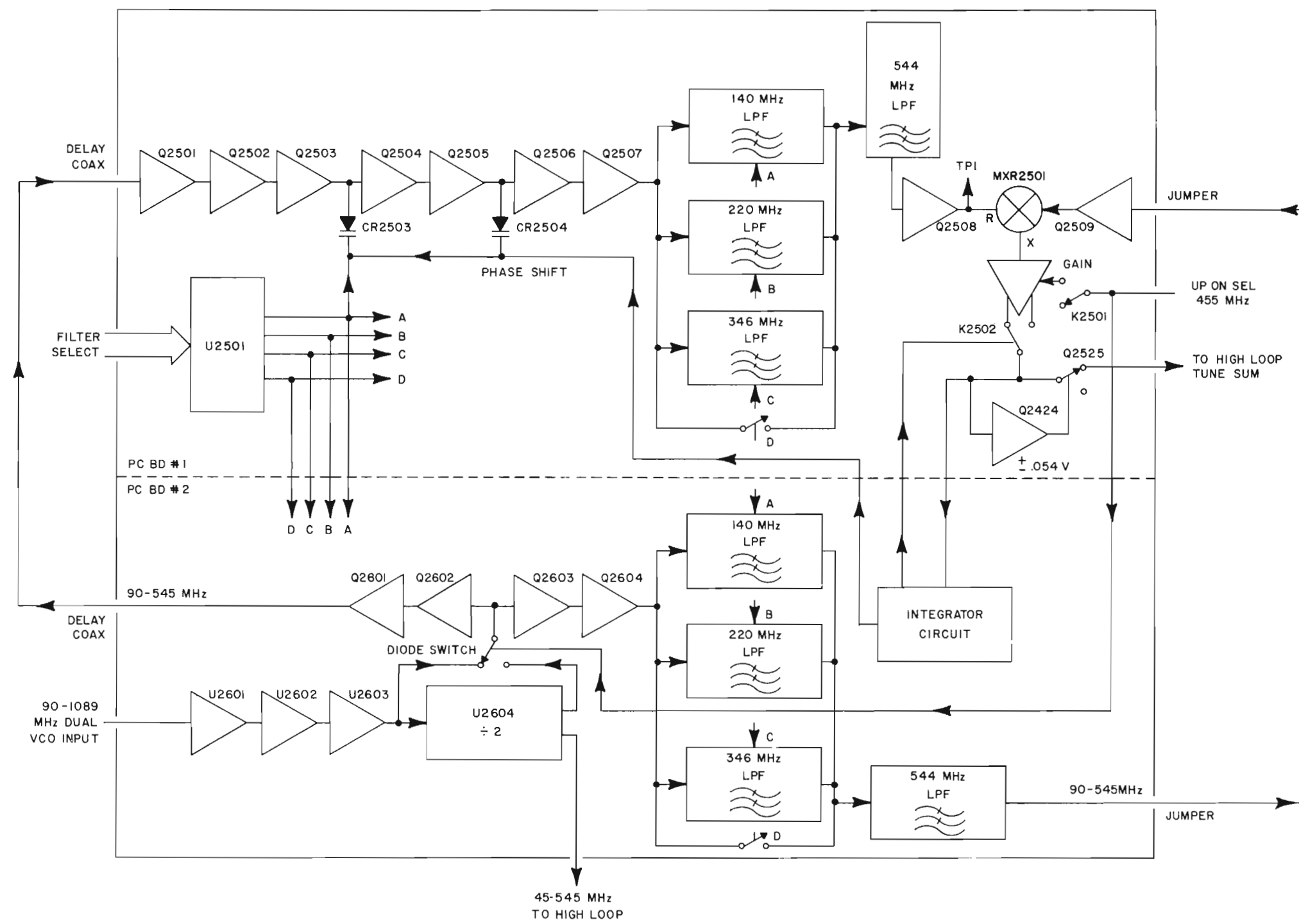


Figure 2-9 Delay Line Detailed Block Diagram

determine which of the signals from the differential amplifier is selected, by energizing or de-energizing relay K2502. The selected signal will be output through Q2525, which acts as a switch to prevent unwanted noise, and through J3004 to the High Loop Module. Op-Amps U2503A and U2503B, along with Q2524, shut off Q2525 if the noise level is too high.

If the 90-1089 MHz input signal at J3005 is perfectly still (i.e., no residual FM), the detected phase output will be a steady 0 VDC. If the phase of the input moves (due to residual FM caused by the thermal noise of the Dual VCO and other low-level system components), the disturbance will take longer to travel down the 75 feet of Delay Line Coax Cable (J3007 to J3001) than it will to travel over the jumper from J3008 to J3002. This will cause the detected phase voltage out of MXR2501 to move from either the 90° or the 270° operating point, as determined by the integrator circuit. The operating point selected will be 180° out of phase from any signal disturbances input at J3005. The selected operating point will then be sent to the High Loop Module to cancel any system residual disturbances.

### Integrator Circuit

The integrator circuit receives the selected signal from K2502 at the junction of R2637 and R2642. U2607A is an inverting amp which drives the integrator amp, U2607B. The output of U2607B drives the collector of Q2610 from 0 to +30 V for the DC control voltage to the varactor diodes in the phase shift circuit. The collector voltage of Q2610 also is applied to op-amps U2609 and U2610. U2609 sets flip-flop U2606B high on pin 15 when the tune voltage goes above 30 V. This turns off flip-flop U2606A by putting a high at pin 4, the reset line of U2606A. Pin 15 of U2606B also pulls up on the integrator amp, U2607B, to force the integrator to slew downward.

Op-Amp U2610 sets flip-flop U2606A high on pin 1 when the tune voltage goes below 0 V. The high on pin 1 of U2606A resets flip-flop U2606A, and pulls down on the integrator amp, U2607B, to force the integrator to slew upward. This is done through Q2608, Q2609 and CR2618.

The Q outputs of both flip-flops, U2606A and U2606B, set and reset flip-flop U2605B. The Q line of U2605B is the control line for relay K2502. Also, when the Q lines of flip-flops U2606A and U2606B are high, their respective indicator LED's, CR2616 and CR2615, will be illuminated.

Op-Amp U2608A is the control for flip-flop U2606. If the input to U2608A, pin 2, crosses approximately 10 VDC in the proper phase direction, and either half of U2606 is still slewing the integrator voltage, pin 6 of U2608A goes high to clear the active half of U2606. Q2605 is an inverter for the signal to clear U2606B. Notice that pin 6 of U2608A must make a positive transition to clear U2606A, and a negative transition to clear U2606B. These transitions are necessary since the clear inputs of U2606 are positive edge triggered. They also prevent the integrator from locking the phase output into an "in phase" condition, which would add noise to the system instead of cancelling noise.

## 2-5-6 Buffer Amp Module Detailed Theory

The FM/AM-1500 contains two identical Buffer Amps. Buffer Amp A is in the 1300-2300 MHz output line of the Dual VCO, while Buffer Amp B is in the 1210 MHz output line. Both Buffer Amps serve to isolate the 1300 MHz IF Generator from the Dual VCO. Any amplification done by the Buffer Amps is of secondary importance. Typical input and output level for both Buffer Amps is +5 to +12 dBm. (See the Buffer Amp Schematic in Section 7 of this Manual.)

## 2-5-7 Low Loop Module Detailed Theory

The Low Loop Module is a phase-locked frequency synthesizer operating from 83.0001 to 93 MHz, depending on the setting of the lower four digits of the front panel RF frequency. (See Figure 2-10 and the Low Loop Schematic in Section 7 of this Manual).

### Programmable Divider Circuit

U3101, U3102 and U3105A operate as a swallow counter for the 100 Hz line. When U3102 reaches its programmed count, pin 12 will go high and pull pin 14 of U3105A high. This causes an extra 100 Hz count of U3102, since one clock pulse is required for U3105A after U3102 has reached count zero.

U3108, U3109, U3110 and U3111 form a decade-upward counter in the programmable divider chain. The system senses count 9297 and loads a new number at count 9298 when pin 8 of flip-flop U3105B goes low. Pin 9 of U3105B goes low on count 9299, and the extra 100 Hz count in the swallow counter is required for the programmable divider before a new number count begins.

### Phase Comparator Circuit

Flip-flop U3106 forms a charge pump phase comparator. When the set period of each section is equal, the charge on C3127 remains constant. If pin 12 is set longer than reset, the charge on C3127 will decrease, causing integrator U3113A to slew up to change the frequency of the voltage controlled oscillator. When the set periods of U3106 are not equal, C3128 will charge and pull up on the base of Q3108. The collector of Q3108 will pull low to indicate an out of phase-lock condition.

### Oscillator Circuit

Q3101 and associated components form a voltage controlled oscillator, which ranges from 83.0001 to 93 MHz. L3102 is adjustable to set a tune voltage of +7 V at 93 MHz. Q3101 is operating properly when there is a voltage of -2 to -4 V on its gate (pin 3). Q3102 is a buffer for the oscillator output signal. Q3101 and Q3102 operate on +6.9 V, sub-regulated by zener diode CR3108.



## Divide-By-10 Circuit

The amplifier stage of Q3103 and Q3104 increases the VCO signal to drive the input to the programmable divider. The amplifier stage of Q3105 and Q3106 increases the VCO signal to drive U3107 as a divide-by 10 circuit. The divided 8.3001 to 9.3 MHz signal is sent through a 15 MHz low-pass filter and output at J4001, at about -12 dBm, to the Low Loop Mixer Module.

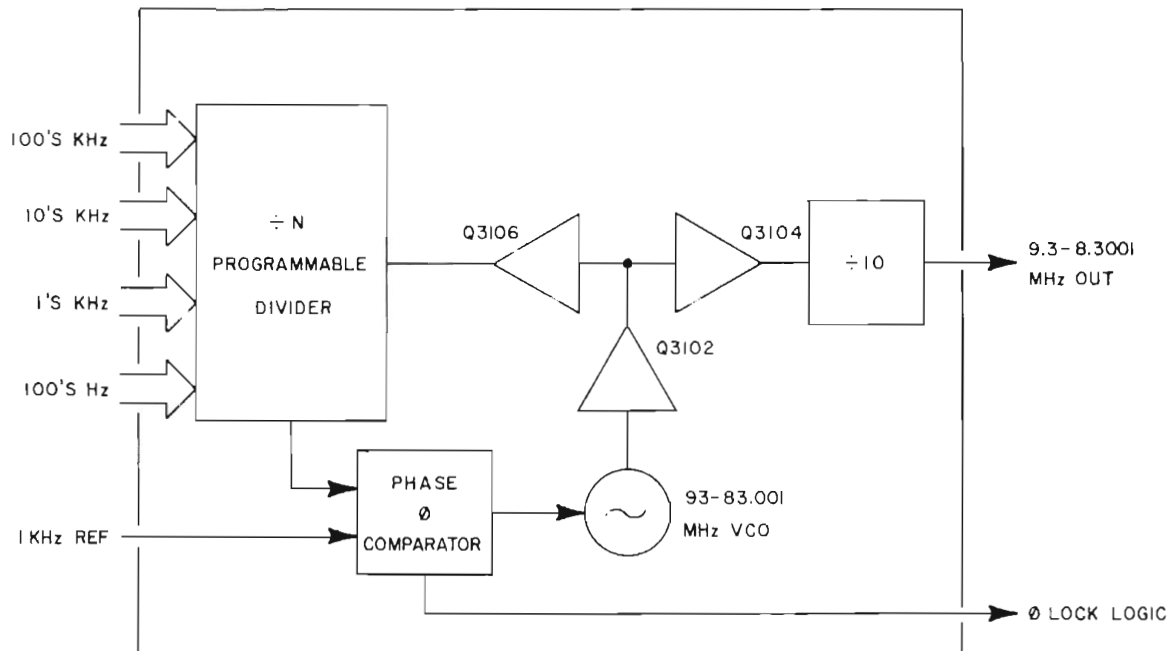


Figure 2-10 Low Loop Detailed Block Diagram

## 2-5-8 Low Loop Mixer Module Detailed Theory

The Low Loop Mixer Module multiplies a 10 MHz reference signal to 70 MHz and mixes it with the 8.3001 to 9.3 MHz signal from the Low Loop Module, resulting in an output signal of 78.3001 to 79.3 MHz. (See Figure 2-11 and the Low Loop Mixer Schematic in Section 7 of this Manual).

The 10 MHz reference signal, input at J1801, is amplified by Q1901 and Q1902. L1902 is used to adjust the frequency to exactly 70 MHz. The signal is band-pass filtered by L1904, L1905, L1906, L1907 and L1908, and then sent to MXR1901.

The mixer output frequency is band-pass filtered, centered on 78.8 MHz, by L1912, L1913, L1914, L1915 and L1916. The resulting 78.3001 to 79.3 MHz signal splits at Q1905 and is amplified by Q1906 and Q1907 for outputs to the FM Generator and Spectrum Analyzer L.O. Modules, respectively.

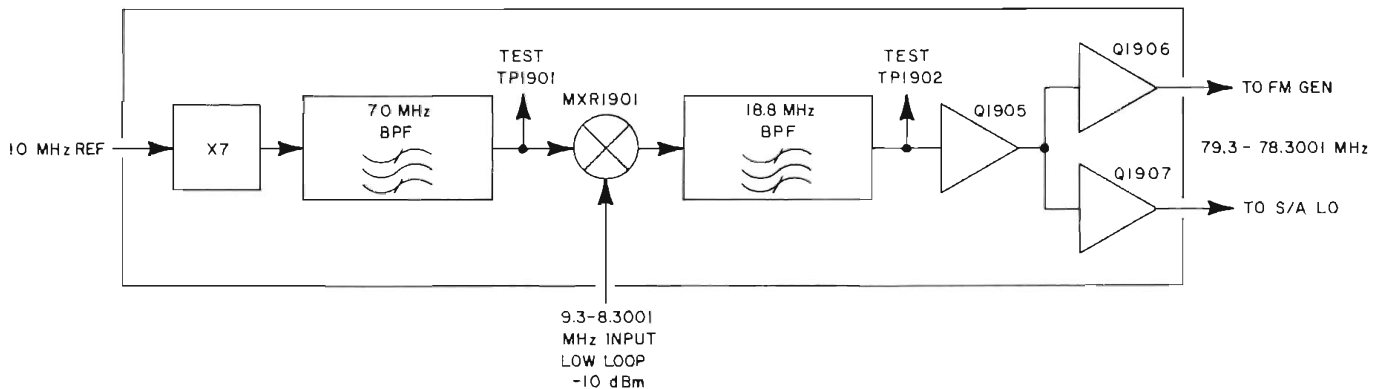


Figure 2-11 Low Loop Mixer Detailed Block Diagram

## 2-6 RECEIVER FUNCTIONAL THEORY (Refer to Figure 2-12)

The input to the receiver section of the FM/AM-1500 can be received at the front panel ANTENNA Connector through an antenna or received at the front panel TRANS/-40 dB DUPLEX Connector via direct cable connection (See Figure 2-12). If the signal is received at the ANTENNA Connector, it goes directly to the 1300 MHz IF Receiver Module. If the signal is received at the TRANS/-40 dB DUPLEX Connector, it is switched through the Power Termination Module (discussed under Generate Function). If the FM/AM-1500 is operating in the Generate Simplex mode, a crossfeed signal is fed through the Diode Switch to the 1300 MHz IF Receiver Module.

Whatever the source of the signal entering the 1300 MHz IF Receiver, it is up-converted twice as a result of mixing with the Dual VCO L.O. frequencies, and output as an 89.0001-90 MHz signal to the 89-90 MHz Receiver Module and to the Spectrum Analyzer Functional Block. The 89.0001-90 MHz IF signal is down-converted twice in the 89-90 MHz Receiver Module and output as a 700 kHz signal. The Low Loop section of the Frequency Synthesis Functional Block mixes with the received signal to produce the 700 kHz output. The 700 kHz signal is sent to the Oscilloscope AM display and to the DEMOD AUDIO PC Board, which drives the speaker, Oscilloscope FM and the front panel meter displays. The DEMOD AUDIO PC Board also performs AGC action on the 89-90 MHz Receiver.

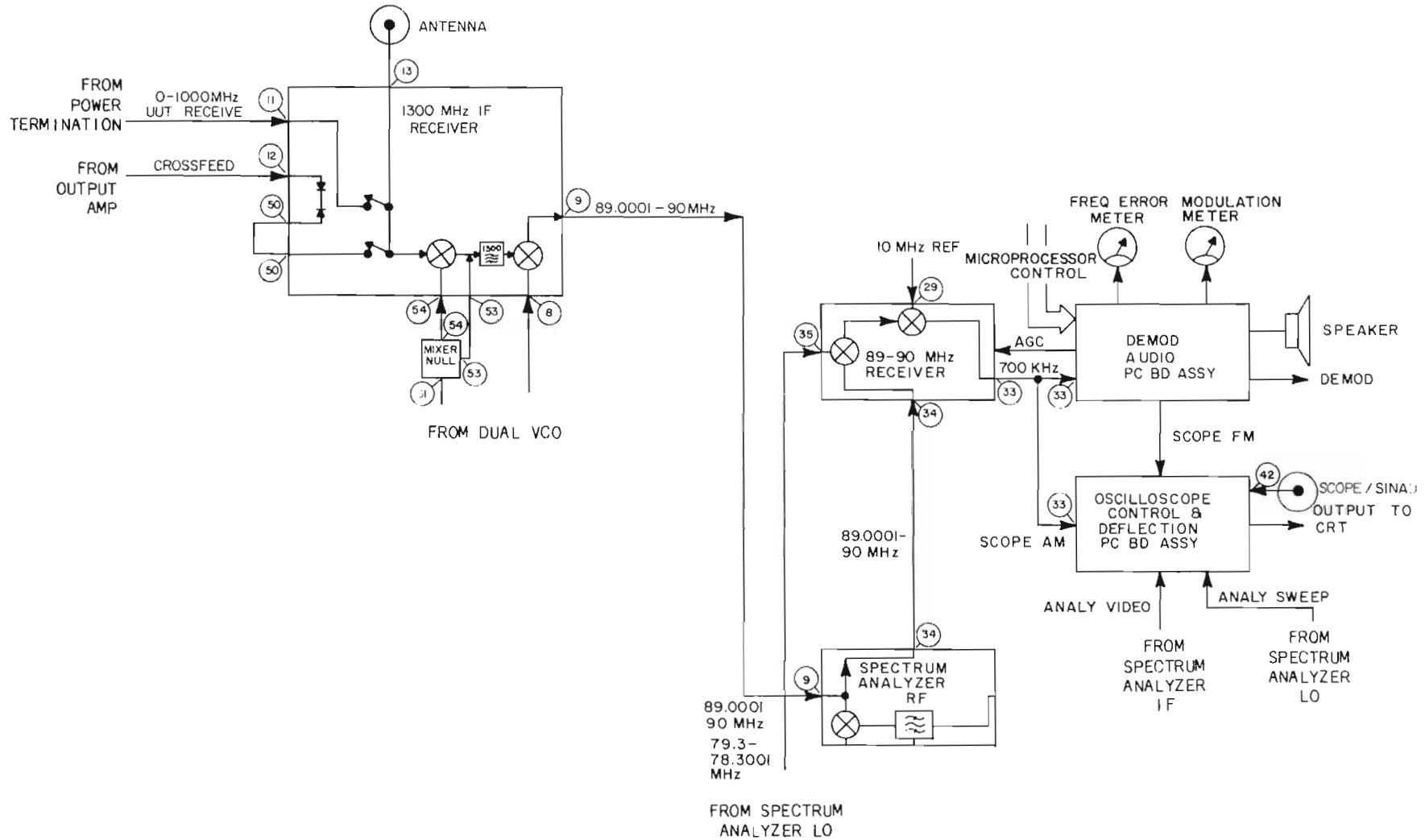


Figure 2-12 Receiver Functional Block Diagram

## 2-6-1 1300 MHz IF Receiver Module Detailed Theory

### Serial Numbers 1005 thru 1406

If the received signal is input from the ANTENNA Connector, it enters at J1003 and is sent through a static protect circuit to the first mixer (See Figure 2-13 and the 1300 MHz IF Receiver Schematic in Section 7 of this Manual.) Relays K1101 and K1102 can be controlled from the front panel ATTENUATOR Switch to attenuate the signal by 0, 20 or 40 dB of attenuation.

If the received signal is input from the TRANS/-40 dB DUPLEX Connector, it enters at J1005 and is switched to the first mixer when its control line at FL1003 is pulled high.

### **NOTE**

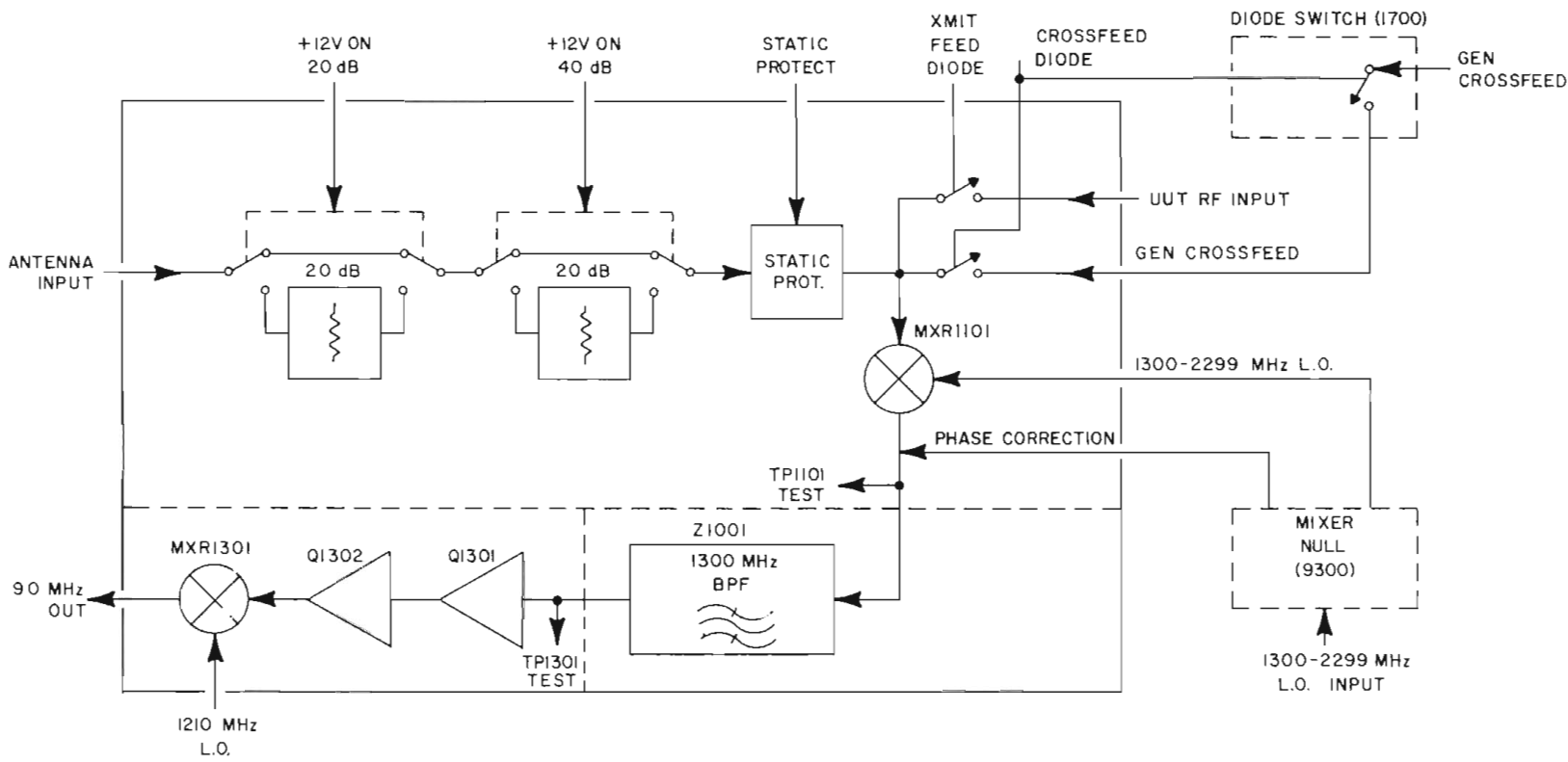
The control line logic for the Crossfeed Diode, XMIT Feed Diode and +12 V on Static Protect lines is located on the Demod Audio PC Board.

If the received (crossfeed) signal is input from the Generator Functional Block (in Generate Simplex mode of operation), it is input at J1004 and is switched to the first mixer when its control line at FL1002 is pulled high. Notice that the control line at FL1002 also controls the Diode Switch Module. The received signal is up-converted in the first-mixer, MXR1101, to the 1st IF Frequency of 1300-1300.9999 MHz, and is then fed through a 1300 MHz bandpass filter, Z1001. The up-conversion in the first mixer results from mixing the received frequency with a 1300-2299 MHz input, which enters at J1006 from the Dual VCO. For serial numbers 1235 and subsequent, a Mixer Null module has been added between the Dual VCO and the 1300 MHz IF Receiver for phase control. The phase control input at J1010 nulls out any unwanted signals produced in the first mixer.

The filtered 1300-1300.9999 MHz signal is amplified in two transistor stages, Q1301 and Q1302, and sent to the second mixer, MXR1301. A 1210 MHz signal, from the Dual VCO, is input at J1001 and mixed with the 1300-1300.9999 MHz signal to produce a second IF signal of 89.0001 to 90 MHz. The 89.0001-90 MHz IF is output at J1002 to the 89-90 MHz Receiver Module and to the Spectrum Analyzer RF Module.

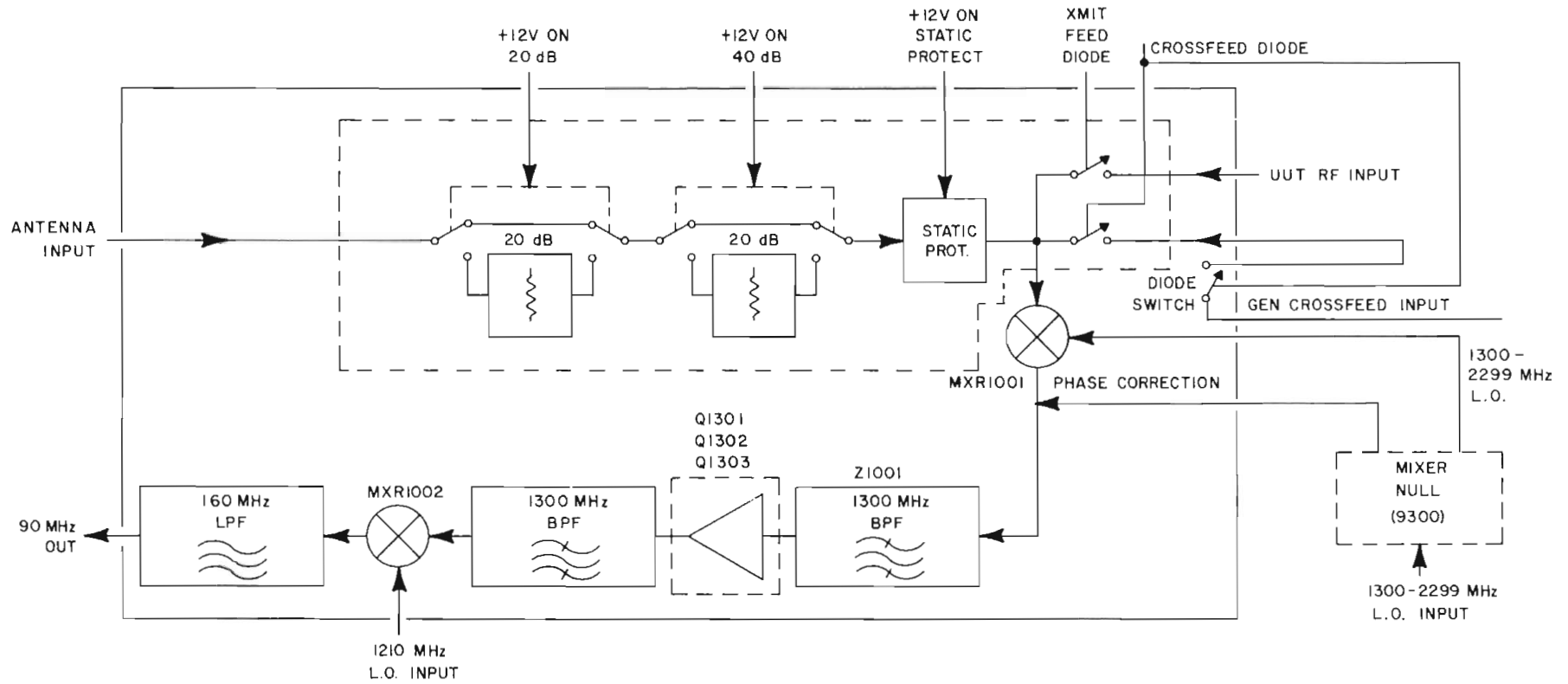
### **NOTE**

The above discussion refers to the 1300 MHz IF Receiver installed in serial numbers 1005 thru 1406. At that time, the module was redesigned and the Diode Switch was incorporated into the new module. Serial numbers thru to 1406 use part number 7005-5041-300 for 1300 MHz IF Receiver modules. Serial numbers 1407 and on contain part number 7005-5041-400 for 1300 MHz IF Receiver modules.



Serial No. 1005 thru 1406

Figure 2-13 1300 MHz IF Receiver Detailed Block Diagram



Serial No. 1407 and On

Figure 2-13a 1300 MHz IF Receiver Detailed Block Diagram

### Serial Numbers 1407 and On

If the received signal is input from the ANTENNA Connector, it enters at J1003 and is sent through a static protect to the first mixer (See Figure 12-13a). Relays K1101 and K1102 can be controlled from the front panel ATTENUATOR Switch to attenuate the signal by 0, 20 or 40 dB of attenuation.

If the received signal is input from the TRANS/-40 dB DUPLEX Connector, it enters at J1005 and is switched to the first mixer when its control line at FL1003 is pulled high.

### **NOTE**

The control line logic for the Crossfeed Diode, XMIT Feed Diode and +12 V on Static Protect lines is located on the Demod Audio PC Board.

If the received (crossfeed) signal is input from the Generator Functional Block (in Generate Simplex mode of operation), it is input at J1008, switched through the Diode Switch when FL1007 goes high, and jumpered over to J1004 where it is then switched to the first mixer when FL1002 goes high. Notice that FL1007 and FL1002 are tied together and go high at the same time. Whatever the source, the received signal is up-converted in the first mixer, MXR1001, to the 1st IF Frequency of 1300-1300.9999 MHz, and is then fed through a 1300 MHz band-pass filter, Z1001. The up-conversion in the first mixer results from mixing the received frequency with a 1300-2299 MHz L.O. frequency, which is generated by the Dual VCO Module, phase controlled by the Mixer Null Module to null out any 90 MHz spikes, and then input at J1006 and J1010.

The filtered 1300-1300.9999 MHz signal is amplified in three transistor stages, Q1301, Q1302 and Q1303, and sent to the second mixer, MXR1002. A 1210 MHz L.O. signal, from the Dual VCO, is input at J1001 and mixed with the 1300-1300.9999 MHz signal to produce a second IF signal at 89.0001 to 90 MHz. L1001, C1001 and C1002 form a 160 MHz lowpass filter to remove unwanted harmonics. The 89.0001-90 MHz IF is output at J1002 to the 89-90 MHz Receiver Module and to the Spectrum Analyzer RF Module.



## 2-6-2 89-90 MHz Receiver Module Detailed Theory

The 89.0001 to 90 MHz second IF signal is input at J3802 (See Figure 2-14 and the 89-90 MHz Receiver Schematic in Section 7 of this Manual). It is then amplified by Q2901 and Q2902 and bandpass filtered in five stages, L2907 thru L2911. A 79.3 to 78.3001 MHz signal, from the Low Loop section of the Frequency Synthesis Functional Block, is mixed with the second IF frequency in MXR2901 to produce a third IF frequency of 10.7 MHz. The 10.7 MHz IF signal is amplified by Q2903 and Q2904 before passing through selected bandpass filters of 200 kHz, 15 kHz or 6 kHz.

### **NOTE**

The desired bandpass filter is selected by the setting of the MODULATION Control on the front panel as follows:

AM1, SSB - 6 kHz  
AM2, FM1 - 15 kHz  
FM2, FM3, FM4 - 200 kHz

The 10.7 MHz IF is amplified by Q2910 before it is mixed in Q2911 with a 10 MHz reference signal. The resulting 700 kHz final IF is buffered by Q2912 and output at J3805 to the Demod Audio PC Board and to the Oscilloscope Control and Deflection PC Board.

Automatic Gain Control (AGC) is provided by the input at pin 5 of J3803, from the Demod Audio PC Board. The more negative this input goes, the smaller is the amplification done by Q2903, Q2904 and Q2910.

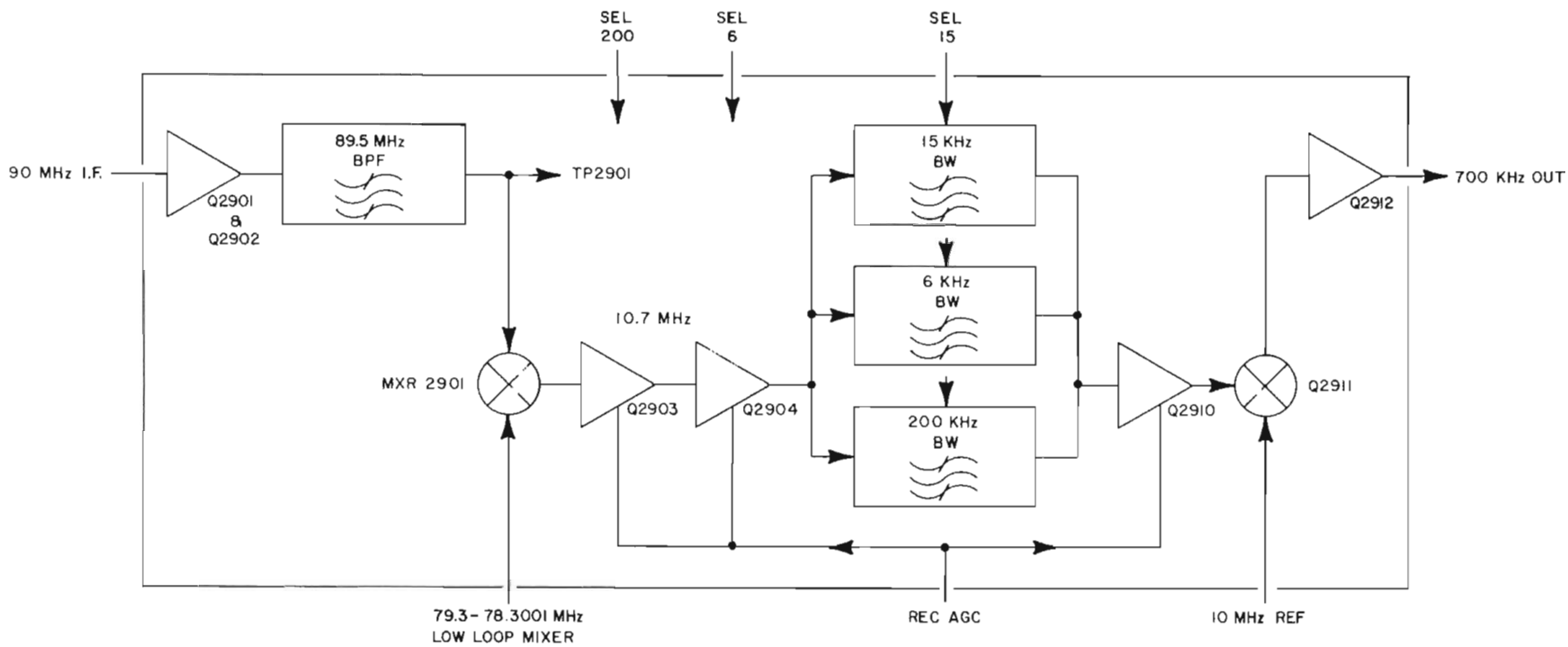


Figure 2-14 89-90 MHz Receiver Detailed Block Diagram

## 2-6-3 Demod Audio PC Board Detailed Theory

### **NOTE**

Use paragraph 2-6-3 for Demod Audio PC Board 7010-5034-700 and Demod Audio PC Board Schematic 0000-5014-700. These drawings are effective for FM/AM-1500 serial numbers 1005 thru 1425.

### FM Dectector Circuit

The 700 kHz IF input at J4704, from the 89-90 MHz Receiver Module, divides to go to the AM Detector circuit and to the FM detector circuit (See Figure 2-15a and the Demod Audio PC Board Schematic in Section 7 of this Manual.) The FM Detector Circuit consists of Q4701, Q4703 thru Q4707, U4701 and U4725A. Q4701 amplifies the 700 kHz signal before applying it to the squaring amp. The squaring amp, U4701, produces a square wave from the 700 kHz IF. The output of the squaring amp is applied to Q4703. Q4703 will turn on Q4704 during the rising edge of its square wave input, via R4714 and C4721. On the falling edge of the square wave, Q4703 will turn off, causing Q4705 to turn on via R4715, R4713 and C4720. When Q4705 turns on, C4731 is charged via Q4706. When Q4704 turns on, the charge on C4731 is dumped, via Q4707, into the low-pass filter, which consists of L4703, L4704, C4732, C4733 and C4744. The low-pass filter produces a positive DC voltage by averaging the energy which is dumped into it by C4731 and Q4707. This DC level will increase as the frequency of the incoming pulses increases. U4725A amplifies this DC level, and its output contains the demodulated FM audio.

### AM Dectector Cirucit

The 700 kHz IF is applied to Q4702, which amplifies the 700 kHz IF and mixes it with any single sideband injection signal that is applied when in SSB. The output of Q4702 is applied to a detector consisting of CR4702 and U4725B. CR4702 charges C4725 on each positive half cycle of the IF input. U4725B buffers the charge on C4725. The output of U4725B contains the demodulated AM audio and the receiver AGC information. The demodulated AM audio is applied to U4751B, which selects between demodulated AM or FM.

U4744, U4751C and Q4708 process the AGC information. Q4708 increases charge current for the integrator when in AM, preventing the AGC from canceling out the AM audio. U4744A provides feedback for the integrator, U4744B. The output of U4744B is applied to the AGC input of the 89-90 MHz Receiver Module. The output of U4744B is also applied to U4743A. U4743A is the signal level amplifier for the squelch circuit. The output of U4743A, which is inverted, is applied to the squelch comparator, U4743B. U4743B compares the output of U4743A with the setting of the SQUELCH Control on the front panel. The output of U4743B is applied to the squelch switch, U4751A, and to Q4709 which drives the SIG Indicator (57) on the front panel. In addition, the squelch output is applied to U4703A to disable the FREQ ERROR Meter (41) and is also applied to the I/O PC Board to disable the digital FREQ ERROR Meter. The meters are disabled when squelch is not broken.

## 700 kHz SSB Generator Circuit

A 1 kHz reference frequency, input at pin 3 of P4701, clocks U4717 which is a phase lock loop (PLL) chip. U4709 is a divide-by 700 ripple counter. The 1 kHz output of U4709, at pin 14, is phase locked to the reference frequency. The 700 kHz output of U4717, at pin 4, is determined by R4723, R4732, C4729 and C4728. Only when the SSB line is high at the inputs to U4726A will the PLL chip not be inhibited.

## SINAD Circuit

The SINAD signal, from the Oscilloscope Control and Deflection PC Board, enters at pin 18 of P4702. The SINAD circuit consists of U4775, U4766, U4765 and U4756. U4775A is a variable gain amplifier whose gain is controlled by an opto-isolator, U4783. The incoming audio is full-wave rectified by U4775B and U4765A and applied to an integrator, U4765B. U4765B smooths out the rectified audio signal. The output of U4765B is applied to U4783, the opto-isolator. As the signal under test increases, the gain of U4775A decreases, keeping the output level of U4775A constant.

The output of U4765B is also applied to a low level comparator, U4756A. U4756A compares the output of the integrator with a pre-determined value. If the output of the integrator is too low to accurately measure SINAD, the comparator forces the output line to the meter positive via CR4729. This causes the meter to peg to the right, indicating that the signal is unreliable.

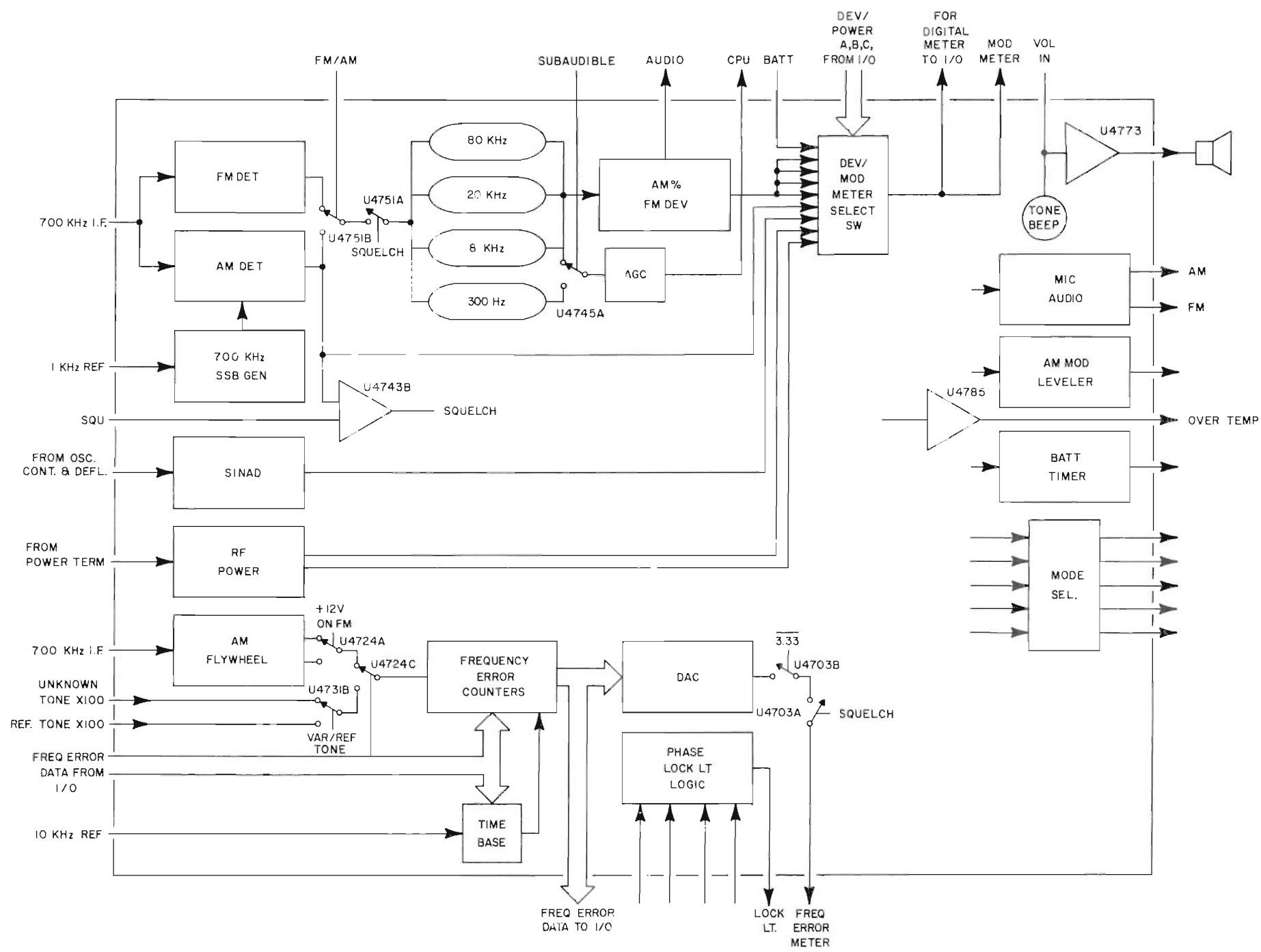
The output of U4775A is also applied to a 1 kHz notch filter, U4766A. U4766A removes the 1 kHz audio tone and leaves only noise and distortion in its output. The noise and distortion is full-wave rectified by U4766B and U4756B. The output of the rectifier is smoothed out to a DC level by R4862 and C4762 before being applied to the meter switch.

## MIC Audio Circuit

Microphone audio, input at pin 20 of P4703, is amplified by U4757 and clipped by CR4740 and CR4739. R4897 is provided for AM level adjustment and R4896 is provided for FM level adjustment. Switch U4750 selects between AM and FM, as controlled by the AM/FM Switch. The selected output is sent to the Dual Tone Generator PC Board.

## Mode Select Circuit

The Mode Select circuit is a logic array consisting of U4768B, U4768C, U4768D, U4786, U4777 and Q4721 thru Q4724. This logic array controls the crossfeed Diode Switch, Static Protect Relay, Power Termination Relay, XMTR Feed Diode Switch and the +12 V on Generate line. A truth table for this logic array is shown in Table 2-1a.



EFFECTIVE SER. NO. 1005 THRU 1425

Figure 2-15 Demod Audio PC Board Detailed Block Diagram

| INPUTS                   |     |        |              |       | OUTPUTS            |                   |                       |                       |     |
|--------------------------|-----|--------|--------------|-------|--------------------|-------------------|-----------------------|-----------------------|-----|
| (ACTIVE LOW)<br>MIKE KEY | REC | DUPLEX | XM'T<br>SENS | TRACK | CROSSFEED<br>DIODE | STATIC<br>PROTECT | PWR<br>TERM.<br>RELAY | XMTR<br>FEED<br>DIODE | GEN |
| 0                        | 0   | 0      | 0            | 0     | 1                  | 0                 | 1                     | 0                     | 1   |
| 1                        | 0   | 0      | 0            | 0     | 1                  | 0                 | 1                     | 0                     | 1   |
| 0                        | 1   | 0      | 0            | 0     | 1                  | 0                 | 1                     | 0                     | 1   |
| 1                        | 1   | 0      | 0            | 0     | 0                  | 1                 | 1                     | 0                     | 0   |
| 0                        | 0   | 1      | 0            | 0     | 0                  | 1                 | 0                     | 0                     | 1   |
| 1                        | 0   | 1      | 0            | 0     | 0                  | 1                 | 0                     | 0                     | 1   |
| 0                        | 1   | 1      | 0            | 0     | 0                  | 1                 | 0                     | 0                     | 1   |
| 1                        | 1   | 1      | 0            | 0     | 0                  | 1                 | 0                     | 0                     | 0   |
| 0                        | 0   | 0      | 1            | 0     | 1                  | 0                 | 0                     | 1                     | 1   |
| 1                        | 0   | 0      | 1            | 0     | 1                  | 0                 | 0                     | 1                     | 1   |
| 0                        | 1   | 0      | 1            | 0     | 1                  | 0                 | 0                     | 1                     | 1   |
| 1                        | 1   | 0      | 1            | 0     | 0                  | 0                 | 0                     | 1                     | 1   |
| 0                        | 0   | 1      | 1            | 0     | 0                  | 0                 | 0                     | 1                     | 1   |
| 1                        | 0   | 1      | 1            | 0     | 0                  | 0                 | 0                     | 1                     | 1   |
| 0                        | 1   | 1      | 1            | 0     | 0                  | 0                 | 0                     | 1                     | 1   |
| 1                        | 1   | 1      | 1            | 0     | 0                  | 0                 | 0                     | 1                     | 1   |
| 0                        | X0  | 0      | 0            | 1     | 1                  | 1                 | 0                     | 0                     | 1   |
| 1                        | X0  | 0      | 0            | 1     | 0                  | 1                 | 0                     | 0                     | 1   |
| 0                        | 1   | 0      | 0            | 1     | 1                  | 1                 | 0                     | 0                     | 1   |
| 1                        | 1   | 0      | 0            | 1     | 0                  | 1                 | 0                     | 0                     | 1   |
| 0                        | X0  | X1     | 0            | 1     | 1                  | 1                 | 0                     | 0                     | 1   |
| 1                        | X0  | X1     | 0            | 1     | 0                  | 1                 | 0                     | 0                     | 1   |
| 0                        | 1   | X1     | 0            | 1     | 1                  | 1                 | 0                     | 0                     | 1   |
| 1                        | 1   | X1     | 0            | 1     | 0                  | 1                 | 0                     | 0                     | 1   |
| 0                        | X0  | 0      | 1            | 1     | 1                  | 0                 | 0                     | 1                     | 1   |
| 1                        | X0  | 0      | 1            | 1     | 0                  | 0                 | 0                     | 1                     | 1   |
| 0                        | 1   | 0      | 1            | 1     | 1                  | 0                 | 0                     | 1                     | 1   |
| 1                        | 1   | 0      | 1            | 1     | 0                  | 0                 | 0                     | 1                     | 1   |
| 0                        | X0  | X1     | 1            | 1     | 1                  | 0                 | 0                     | 1                     | 1   |
| 1                        | X0  | X1     | 1            | 1     | 0                  | 0                 | 0                     | 1                     | 1   |
| 0                        | 1   | X1     | 1            | 1     | 1                  | 0                 | 0                     | 1                     | 1   |
| 1                        | 1   | X1     | 1            | 1     | 0                  | 0                 | 0                     | 1                     | 1   |

NOTE: The microprocessor will override Duplex high and REC low when Track is high, as denoted by (X).

EFFECTIVE SER. NO. 1005 THRU 1425

Table 2-2 Demod Audio PC Board Mode Select Logic

## RF Power Meter Drive Circuit

Detected power is input at pin 6 of P4702 from the Power Termination Module. U4747B amplifies the signal. R4830 (ZERO PWR ADJ) is provided to set the output of U4747B to zero, with no input signal. Switch U4754B is controlled by the AVG PEAK/PEAK Switch to add U4747A into the line when PEAK is selected. U4753A, U4753B and their respective resistor networks are selected for the 150 W and 15 W scales of the MODULATION Meter. R4829 is the 150 W adjustment, and R4838 is the 15 W adjustment.

## % Mod Circuit

The Demod Audio from the selected filter is amplified by U4780A. The signal is then output to the DEMOD OUTPUT Connector, to the Oscilloscope and to the front panel controls. The signal also is switched through selected resistors by U4781, as controlled by the DEV/PWR Control. U4781 also switches in the FM Zero line or the AM Zero line, as selected by switch U4754A. Whenever pin 6 of U4781 is high, as controlled by the DEV/PWR Control, all channels of U4781 are off. When pin 6 of U4781 is low, one pair of channels out of U4781 is on. Pins 9 and 10 determine which pair of channels is on, as controlled by the DEV/PWR A and B lines.

When U4754A selects FM Zero, a preset zero is selected by U4734A, B and C and by U4745C. Only one of these switches will be on at any one time. The switches are driven by the FM1 thru FM4 lines to select a zero for each of the four FM bandwidths. R4771, R4770, R4762 and R4765 set the zero for the bandwidths.

The % Mod Scale part of the circuit consists of U4780B, U4761, U4746, U4752 and U4762B. U4762B buffers the offset signal. The offset signal is a DC level which is used to zero the % AM/kHz DEV level. U4780B amplifies the demodulated audio signal. U4761A and B form a precision full-wave rectifier. The output of the rectifier is smoothed out by R4814 and C4755. U4746B amplifies the charge on C4755. The output of U4746B is the average % Modulation/kHz Deviation. The output of the full-wave rectifier, at pin 7 of U4761B, is also applied to U4752, which is a peak detector. U4752 will charge C4768 via CR4715. The output voltage will be equal to the peak of the full-wave rectifier output. The output signal is applied to U4746A, which buffers the output of U4752 before applying it to U4754C. U4754C selects between Peak % AM/kHz DEV and Peak Average % AM/FM DEV. The output of U4754C is applied to the DEV/% Mod Meter Select Switch.

## Phase Lock Light Logic Circuit

Three phase-lock control signals are input to the Demod Audio PC Board: High Loop lock, Low Loop lock and Duplex lock. When all three of these lines are high, pin 3 of U4776 is low. When any of these lines are low, their respective diode (CR4742, CR4744 or CR4745) will be reverse biased, causing pin 3 of U4776 to go high. U4776B and U4776C form an oscillator circuit to present alternating highs and lows to pin 12 of

U4776D. When pin 13 of U4776D is low, pin 11 will be high to turn on Q4718 and light the Freq LOCK Indicator Lamp on the front panel. When pin 13 of U4776D is high, the Freq LOCK Indicator Lamp will flash off and on at the same frequency as the oscillator at pin 12. Also, when pin 3 of U4776 is high, Q4719 will conduct to output a +12 V Unlock signal to the I/O PC Board.

When the GEN/LOCK Control is not in the Lock position, +12 V is input at pin 3 of P4703. This will cause the Freq LOCK Indicator Lamp to flash and +12 V to be output to the I/O board in the same manner as the phase-lock lines.

#### Battery Timer and Control Circuit

The Battery Timer and Control Circuit consists of Q4715, Q4716, Q4717, U4749, U4767A and U4748. Q4717 conducts when the front panel PWR/OFF/BATT Switch is set to BATT. When Q4717 conducts, U4767A changes states. CR4737, CR4738, C4774 and C4775 determine which input (S or R) to flip-flop U4767A will become active. If the flip-flop is set, C4774 will be fully charged, allowing the reset line to go high first. The set input cannot go high until C4775 charges. By the time C4775 charges, C4776 is charged and Q4717 is no longer able to drive an input of the flip-flop. If the flip-flop is reset when Q4717 conducts, the opposite actions occur. Thus, the flip-flop toggles each time Q4717 starts conducting.

The Q output of U4767A turns on Q4716, which outputs a control signal to put the FM/AM-1500 power supply into battery operation. The  $\bar{Q}$  output, when low, turns on Q4715, causing power to be applied to the battery timer and to the low voltage cutoff. The battery timer, U4749, produces a logic 1 at pin 13 after 7 to 11 minutes. This logic 1 will reset flip-flop U4767A via CR4734. When the flip-flop is reset, the power supply, battery timer and low voltage cutoff circuits are turned off.

The low voltage cutoff circuit consists of a comparator, U4748, and a zener diode, CR4726. A sample of the battery voltage is applied to the negative input of the comparator via a voltage divider consisting of R4869, R4871 and R4872. The positive side of the comparator is connected to the zener diode, which regulates it to approximately 5 volts. When the battery voltage drops below a predetermined level, the negative input of the comparator will fall below the zener diode voltage. This causes the output of the comparator to go positive and reset flip-flop U4767A, turning the FM/AM-1500 off.

#### AM Modulation Leveler Circuit

AM modulation is input at pin 13 of P4702 from the Dual Tone Generator PC Board. U4784B amplifies the signal for output to the Output Amplifier Module, which controls the AM modulator level of the Duplex Offset Module. R4963 is provided for AM modulation adjustment. R4959 is provided for RF level adjustment. R4961 is provided for RF level linearity adjustment.



## AM Flywheel Circuit

The AM Flywheel circuit consists of Q4713, U4724A, U4724B, U4716, U4708 and U4733. Q4713 buffers the 700 kHz IF signal input at J4706 and applies this signal to a CMOS Switch, U4724B, and to a comparator, U4708. U4708 is used in FM only. The output of U4708 is a square wave with a frequency equal to the frequency of the 700 kHz IF. U4724B, along with U4716, operates as a phase/frequency detector. The output of the integrator, U4716, is a DC voltage which steers the output frequency of the VCO, U4733, in the appropriate direction to make the frequencies equal at pins 10 and 15 of U4724B. This phase-locked loop generates a square wave, at pin 4 of U4733, with a frequency equal to the 700 kHz IF input. When over-modulation of the carrier signal occurs, integrator U4716 holds its output at a relatively constant level during the interval when the carrier is suppressed. When the carrier is not suppressed, the phase-lock loop corrects for any drift which may have occurred during the time the carrier was suppressed. U4724A selects between the output of the phase-locked loop for AM demodulation and the output of the comparator, U4708, for FM demodulation.

## Time Base Circuit

The Time Base circuit consists of Q4714, U4742, U4741, U4731, U4732, U4722, U4723, U4737B, U4737C, U4729C, U4740 and U4739. This circuit provides the time base frequency for the frequency error counter.

Q4714 buffers the 10 kHz input from the Clock Divider, at pin 18 of P4703, and applies this signal to U4742A and U4732A. U4742A, U4742B, U4741A and U4741B are decade counters which function as divide-by 10 frequency dividers. These dividers produce frequencies at 1 kHz, 100 Hz and 10 Hz. These outputs are applied to CMOS Switches U4732B, U4731C and U4731A, respectively. The four CMOS Switches (U4731A, U4731C, U4732B and U4732A) select one of the time base frequencies of 10 Hz, 100 Hz, 1 kHz and 10 kHz, respectively. The switches are driven by the time base select logic.

The time base select logic consists of U4715, U4722A, U4722B, U4722C, U4723A, U4723B and U4723C. Table 2-2a is a truth table which describes the operation of the time base logic. The time base select logic receives frequency error settings from the I/O PC Board and turns on the appropriate CMOS Switch. In addition, the time base select logic also produces a control line which informs the frequency error counter when to count in the audio mode. This control line is driven by pin 9 of U4722B.

U4729C, U4737C and U4737B drive control lines for the frequency error counter. These control lines are the 1.0 second, 0.1 second and 0.01 second time bases. When all three of these lines are inactive, the 0.001 second time base is selected. The selected time base line is applied to U4740 which, along with U4739A, produces the gate for the frequency error counter.

| FREQ ERROR |   |   |   | U4722B | U4723C | U4722A | U4723B | U4723A | U4715 |
|------------|---|---|---|--------|--------|--------|--------|--------|-------|
| D          | C | B | A | Pin 9  | Pin 10 | Pin 6  | Pin 9  | Pin 6  | Pin 2 |
| 0          | 0 | 0 | 0 | 1      | 1      | 0      | 1      | 1      | 0     |
| 0          | 0 | 0 | 1 | 1      | 1      | 1      | 0      | 1      | 0     |
| 0          | 0 | 1 | 0 | 1      | 1      | 1      | 1      | 1      | 1     |
| 0          | 0 | 1 | 1 | 0      | 0      | 1      | 1      | 1      | 0     |
| 0          | 1 | 0 | 0 | 0      | 0      | 1      | 1      | 0      | 0     |
| 0          | 1 | 0 | 1 | 0      | 1      | 0      | 1      | 1      | 0     |
| 0          | 1 | 1 | 0 | 0      | 1      | 0      | 1      | 0      | 0     |
| 0          | 1 | 1 | 1 | 0      | 1      | 1      | 0      | 1      | 0     |
| 1          | 0 | 0 | 0 | 0      | 1      | 1      | 0      | 0      | 0     |

Table 2-3 Time Base Logic  
(Effective Ser.No. 1005 thru 1425)

Assume that U4739A is reset and that U4740 has just been loaded with  $0000(2)$ . Under these conditions, the COUNT ENABLE line is high, stopping the frequency error counter from counting. On the next rising edge of the clock, the counter decrements, reducing the contents of the counter by 1 and yielding a count of  $1001(2)$ . When this happens, the output at pin 2 of U4740 goes high, causing U4739 to change states and the COUNT ENABLE line to go low (active state). The COUNT ENABLE line stays low for 10 counts. When the counter underflows from  $0000(2)$  to  $1001(2)$ , pin 2 of U4740 again makes a low to high transition, causing U4739 to change states and the COUNT ENABLE line to go high (inactive state). When this line goes high, U4740 is set to  $0000(2)$  via C4747 and R4780. One count later, the counter again underflows from  $0000(2)$  to  $1001(2)$ , causing U4739 to change states. The counter, U4740, is then allowed to decrement for ten counts and then the cycle repeats itself. The net result is a pulse which is high for one clock period and low for ten clock periods, and which appears on the COUNT ENABLE line.

#### Frequency Error Counter Circuit

The Frequency Error Counter Circuit consists of the following IC's:

|             |                      |
|-------------|----------------------|
| U4705       | U4727                |
| U4707       | U4728                |
| U4710       | U4729 A, B, D, E & F |
| U4711       | U4730                |
| U4713       | U4731B               |
| U4718 A & B | U4732                |
| U4719       | U4736 A, B & D       |
| U4720       | U4737 A & D          |
| U4721       | U4738                |
| U4724C      | U4739B               |

The frequency error counter is a 24 bit binary, presettable up/down counter. Only the lower 8 bits are available at its output. These 8 bits represent the frequency error. When the frequency error counter is in the audio mode, it functions as an up/down counter. At the beginning of each conversion, the frequency error counter is preset to  $C0080(H)$ . During the first gate, the counter counts up using the unknown tone. During the second gate, the counter counts down using the reference tone. If the two tones are equal, the resulting count is  $C0080(H)$ . The lower 8 bits ( $80(H)$ ) are latched and applied to the digital to analog converter and to the I/O PC Board.  $80(H)$  is interpreted as zero. Anything greater than this is interpreted as positive, while anything less is interpreted as negative. If the unknown tone is greater than the reference tone, the result will be positive since the counter counted up more than it counted down. If the unknown tone is less than the reference tone, the result will be negative since the counter counted down more counts than it counted up.

When operating in the RF mode, the counter counts up only. The counter is loaded with a preset value prior to each gate. The gate enables the counting of the 700 kHz IF. If the 700 kHz IF is exactly 700 kHz, the resulting count will be  $C0080(H)$ , which is interpreted as zero. If the 700 kHz IF is less than 700 kHz, the final count will be less than  $C0080(H)$  and will be interpreted as a negative value. If the 700 kHz IF is greater than 700 kHz, the final count will be greater than  $C0080(H)$  and will be interpreted as a positive value. In both audio and RF modes, the difference between  $80(H)$  and the counter's 8 bit output represents the magnitude of the frequency error.

The up/down counter consists of U4712, U4721, U4720, U4711 and U4705. The lower 8 bits of this counter are applied to U4713, which latches the counters' output when the COUNT ENABLE line goes high. The output of U4713 is applied to U4707 and to U4714, a pair of demultiplexers which select between the counter outputs and the OVER/UNDER line.

When an overflow or underflow condition occurs, the upper 12 bits of the counter are applied to the overflow/underflow logic consisting of U4719, U4718A, U4736B, C & D, U4737 A & D and U4738. This logic checks for  $C00(H)$  on the upper 12 bits of the counter. If the count is less than  $C00(H)$ , the logic will indicate an underflow (meter peg = 1; OVER/UNDER = 0). If the count is greater than  $C00(H)$ , an overflow condition is generated (meter peg = 0; OVER/UNDER = 1).

The preset logic, consisting of U4732C, U4730A and U4730B, controls the presetting of the counters. When counting RF, the CMOS Switch, U4732C, applies the COUNT ENABLE signal to the astable multivibrators, U4730 A & B. These astable multivibrators produce a delayed pulse to ensure that everything has settled before presetting the counters. The output of U4730B is applied to the reset inputs of the counters and to the reset input of U4739B. U4739B produces the UP/DOWN count signal and the VAR TONE/REF TONE signal. When in the RF mode, this flip-flop is reset everytime the gate goes high, forcing the counters to count up only.

In the audio mode, the output of U4739B is applied to U4730A by U4732C. In this mode, U4739B is reset on every other gate cycle. During the first cycle, U4731B selects the unknown tone and the UP/DOWN line is high. During the second gate cycle, U4731B selects the reference tone. The output of U4731B is applied to the clock input of the counters via U4729F. CR4746 disables the clock while the COUNT ENABLE line is high. U4724C selects between audio (output of U4731B) and RF (output of U4724A in the AM Flywheel circuit) as controlled by the UP ON AUDIO line.

### Overtemp Circuit

When the thermistor in the Power Termination Module senses an overtemp condition, its signal is input at pin 24 of P4703. When pin 2 of U4785 reaches a pre-determined level, pin 6 will go high to turn on Q4720. This will turn on the OVERTEMP Indicator Lamp on the front panel and also send a +12 V on Overtemp signal to the I/O PC Board.

### Tone Beep Circuit

The KEYDOWN line from the I/O PC Board enters at pin 4 of J4705. When this line is high, Q4712 is on. When this line is low, Q4712 is off to allow the oscillator to function. U4763 and associated components form a 1 kHz Beep Oscillator. R4842 sets the volume level of the Oscillator. The audio-in line at pin 4 of P4702 mixes with the oscillator output and is amplified by U4773, an audio amplifier, for output to the speaker.

2-6-3a Demod Audio PC Board Detailed Theory  
(Effective Ser.No. 1426 and on)

**NOTE**

Use paragraph 2-6-3a for Demod Audio PC Board  
7010-5037-300 and Demod Audio PC Board Schematic  
0000- 5017-300.

FM Detector Circuit

The 700 kHz IF input at J4704, from the 89-90 MHz Receiver Module, divides to go to the AM detector circuit and to the FM detector circuit (See Figure 2-15b and the Demod Audio Schematic in Section 7 of this Manual.) The FM Detector Circuit consists of Q4701, Q4704, Q4705, Q4706, Q4708, Q4709, U4701 and U4733A. Q4701 amplifies the 700 kHz signal before applying it to the squaring amp. The squaring amp, U4701, produces a square wave from the 700 kHz IF. The output of the squaring amp is applied to Q4704. Q4704 will turn on Q4706 during the rising edge of its square wave input, via R4751 and C4750. On the falling edge of the square wave, Q4704 will turn off, causing Q4705 to turn on via R4752, R4750 and C4749. When Q4705 turns on, C4755 is charged via Q4708. When Q4706 turns on, the charge on C4755 is dumped, via Q4709, into the low-pass filter, which consists of L4703, L4704, C4756, C4757 and C4772. The low-pass filter produces a positive DC voltage by averaging the energy which is dumped into it by C4755 and Q4709. This DC level will increase as the frequency of the incoming pulses increases. U4733A amplifies this DC level, and its output contains the demodulated FM audio.

AM Detector Circuit

The 700 kHz IF is applied to Q4702, which amplifies the 700 kHz IF and mixes it with any single sideband injection signal that is applied when in SSB. The output of Q4702 is applied to a detector consisting of CR4702 and U4733B. CR4702 charges C4754 on each positive half cycle of the IF input. U4733B buffers the charge on C4754. The output of U4733B contains the demodulated AM audio and the receiver AGC information. The demodulated AM audio is applied to U4749B, which selects between demodulated AM or FM.

U4750, U4749C and Q4710 process the AGC information. Q4710 increases charge current for the integrator when in AM, preventing the AGC from canceling out the AM audio. U4750A provides feedback for the integrator, U4750B. The output of U4750B is applied to the AGC input of the 89-90 MHz Receiver Module. The output of U4750B is also applied to U4751A. U4751A is the signal level amplifier for the squelch circuit. The output of U4743A, which is inverted, is applied to the squelch comparator, U4751B. U4751B compares the output of U4751A with the setting of the SQUELCH Control on the front panel. The output of U4751B is applied to the squelch switch, U4749A, and to Q4712 which drives the SIG Indicator Lamp on the front panel. In addition, the

squelch output is applied to U4730B to disable the FREQ ERROR Meter and is also applied to the I/O PC Board to disable the digital FREQ ERROR Meter. The meters are disabled when squelch is not broken.

### 700 kHz SSB Generator Circuit

A 1 kHz reference frequency, input at pin 3 of P4701, clocks U4782 which is a phase lock loop (PLL) chip. U4768 is a divide-by 700 ripple counter. The 1 kHz output of U4768, at pin 14, is phase locked to the reference frequency. The 700 kHz output of U4782, at pin 4, is determined by R4944, R4945, C4820 and C4821. Only when the SSB line is high at the inputs to U4783B will the PLL chip not be inhibited.

### SINAD Circuit

The SINAD signal, from the Oscilloscope Control and Deflection PC Board, enters at pin 18 of P4702. The SINAD circuit consists of U4735, U4753, U4734 and U4752. U4735A is a variable gain amplifier whose gain is controlled by an opto-isolator, U4754. The incoming audio is full-wave rectified by U4735B and U4734A and applied to an integrator, U4734B. U4734B smooths out the rectified audio signal. The output of U4734B is applied to U4754, the opto-isolator. As the signal under test increases, the gain of U4735A decreases, keeping the output level of U4735A constant.

The output of U4734B is also applied to a low level comparator, U4752A. U4752A compares the output of the integrator with a pre-determined value. If the output of the integrator is too low to accurately measure SINAD, the comparator forces the output line to the meter positive via CR4716. This causes the meter to peg to the right, indicating that the signal is unreliable.

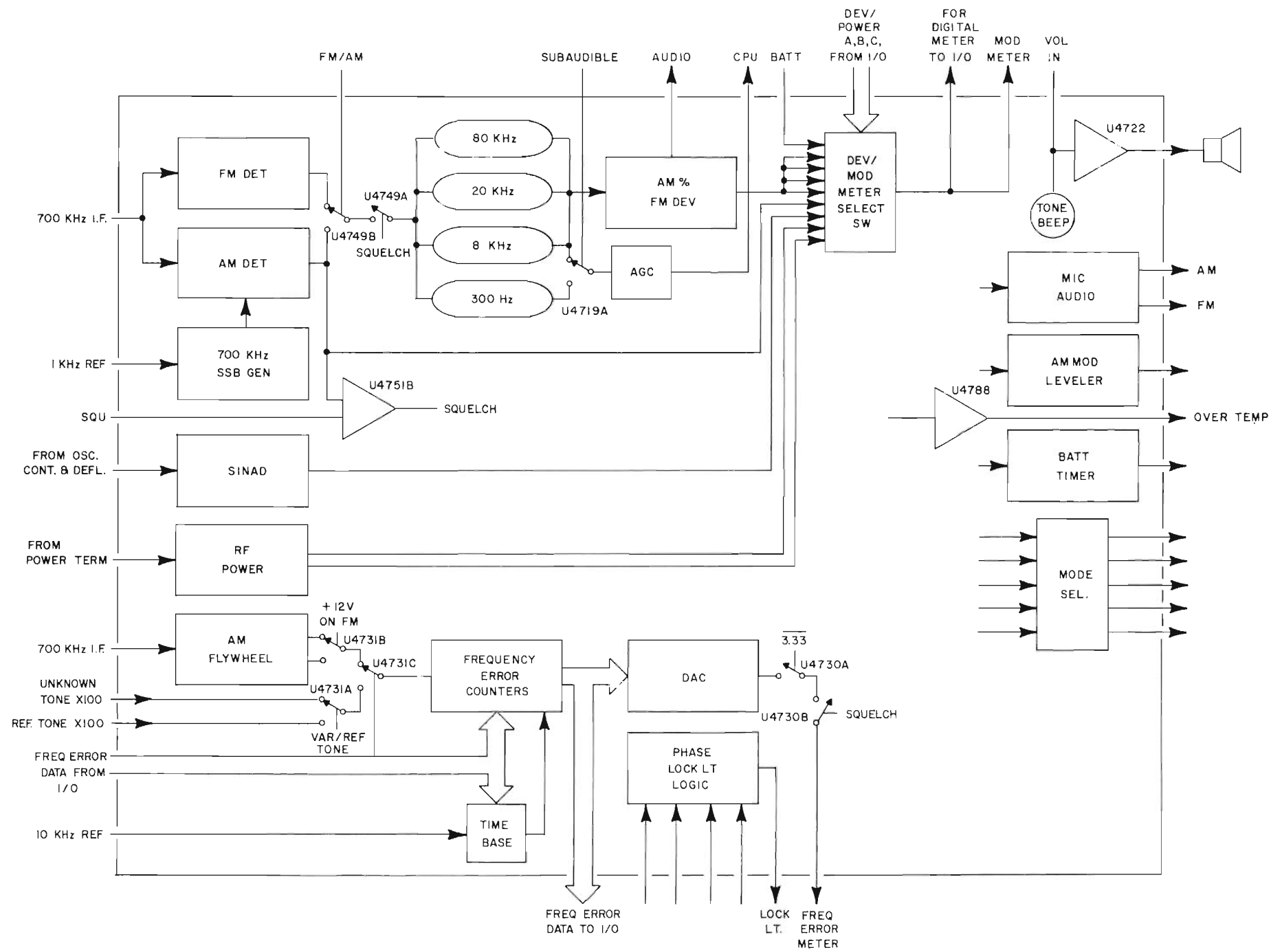
The output of U4735A is also applied to a 1 kHz notch filter, U4753A. U4753A removes the 1 kHz audio tone and leaves only noise and distortion in its output. The noise and distortion is full-wave rectified by U4753B and U4752B. The output of the rectifier is smoothed out to a DC level by R4852 and C4785 before being applied to the meter switch.

### MIC Audio Circuit

Microphone audio, input at pin 20 of P4703, is amplified by U4778 and clipped by CR4739 and CR4738. R4933 is provided for AM level adjustment and R4932 is provided for FM level adjustment. Switch U4779 selects between AM and FM, as controlled by the AM/FM Switch. The selected output is sent to the Dual Tone Generator PC Board.

### Mode Select Circuit

The Mode Select circuit is a logic array consisting of U4780, U4781, U4789 and Q4721 thru Q4724. This logic array controls the crossfeed Diode Switch, Static Protect Relay, Power Termination Relay, XMTR Feed Diode Switch and the +12 V on Generate line. A truth table for this logic array is shown in Table 2-1b.



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Figure 2-15a Demod Audio PC Board Detailed Block Diagram

| INPUTS                   |     |        |              |       | OUTPUTS            |                   |                       |                       |     |
|--------------------------|-----|--------|--------------|-------|--------------------|-------------------|-----------------------|-----------------------|-----|
| (ACTIVE LOW)<br>MIKE KEY | REC | DUPLEX | XMIT<br>SENS | TRACK | CROSSFEED<br>DIODE | STATIC<br>PROTECT | PWR<br>TERM.<br>RELAY | XMTR<br>FEED<br>DIODE | GEN |
| 0                        | 0   | 0      | 0            | 0     | 1                  | 0                 | 1                     | 0                     | 1   |
| 1                        | 0   | 0      | 0            | 0     | 1                  | 0                 | 1                     | 0                     | 1   |
| 0                        | 1   | 0      | 0            | 0     | 1                  | 0                 | 1                     | 0                     | 1   |
| 1                        | 1   | 0      | 0            | 0     | 0                  | 1                 | 1                     | 0                     | 0   |
| 0                        | 0   | 1      | 0            | 0     | 0                  | 1                 | 0                     | 0                     | 1   |
| 1                        | 0   | 1      | 0            | 0     | 0                  | 1                 | 0                     | 0                     | 1   |
| 0                        | 1   | 1      | 0            | 0     | 0                  | 1                 | 0                     | 0                     | 1   |
| 1                        | 1   | 1      | 0            | 0     | 0                  | 1                 | 0                     | 0                     | 0   |
| 0                        | 0   | 0      | 1            | 0     | 1                  | 0                 | 0                     | 1                     | 1   |
| 1                        | 0   | 0      | 1            | 0     | 1                  | 0                 | 0                     | 1                     | 1   |
| 0                        | 1   | 0      | 1            | 0     | 1                  | 0                 | 0                     | 1                     | 1   |
| 1                        | 1   | 0      | 1            | 0     | 0                  | 0                 | 0                     | 1                     | 1   |
| 0                        | 0   | 1      | 1            | 0     | 0                  | 0                 | 0                     | 1                     | 1   |
| 1                        | 0   | 1      | 1            | 0     | 0                  | 0                 | 0                     | 1                     | 1   |
| 0                        | 1   | 1      | 1            | 0     | 0                  | 0                 | 0                     | 1                     | 1   |
| 1                        | 1   | 1      | 1            | 0     | 0                  | 0                 | 0                     | 1                     | 1   |
| 0                        | X0  | 0      | 0            | 1     | 1                  | 1                 | 0                     | 0                     | 1   |
| 1                        | X0  | 0      | 0            | 1     | 0                  | 1                 | 0                     | 0                     | 1   |
| 0                        | 1   | 0      | 0            | 1     | 1                  | 1                 | 0                     | 0                     | 1   |
| 1                        | 1   | 0      | 0            | 1     | 0                  | 1                 | 0                     | 0                     | 1   |
| 0                        | X0  | X1     | 0            | 1     | 1                  | 1                 | 0                     | 0                     | 1   |
| 1                        | X0  | X1     | 0            | 1     | 0                  | 1                 | 0                     | 0                     | 1   |
| 0                        | 1   | X1     | 0            | 1     | 1                  | 1                 | 0                     | 0                     | 1   |
| 1                        | 1   | X1     | 0            | 1     | 0                  | 1                 | 0                     | 0                     | 1   |
| 0                        | X0  | 0      | 1            | 1     | 1                  | 0                 | 0                     | 1                     | 1   |
| 1                        | X0  | 0      | 1            | 1     | 0                  | 0                 | 0                     | 1                     | 1   |
| 0                        | 1   | 0      | 1            | 1     | 1                  | 0                 | 0                     | 1                     | 1   |
| 1                        | 1   | 0      | 1            | 1     | 0                  | 0                 | 0                     | 1                     | 1   |
| 0                        | X0  | X1     | 1            | 1     | 1                  | 0                 | 0                     | 1                     | 1   |
| 1                        | X0  | X1     | 1            | 1     | 0                  | 0                 | 0                     | 1                     | 1   |
| 0                        | 1   | X1     | 1            | 1     | 1                  | 0                 | 0                     | 1                     | 1   |
| 1                        | 1   | X1     | 1            | 1     | 0                  | 0                 | 0                     | 1                     | 1   |

NOTE: The microprocessor will override Duplex high and REC low when Track is high, as denoted by (X).

Table 2-2a Demod Audio PC Board Mode Select Logic  
(Effective Ser. No. 1426 and on)



## RF Power Meter Drive Circuit

Detected power is input at pin 6 of P4702 from the Power Termination Module. U4756B amplifies the signal. R4871 (ZERO PWR ADJ) is provided to set the output of U4756B to zero, with no input signal. Switch U4774A is controlled by the AVG PEAK/PEAK Switch to add U4756A into the line when PEAK is selected. U4757B, U4757A and their respective resistor networks are selected for the 150 W and 15 W scales of the MODULATION Meter. R4881 is the 150 W adjustment, and R4904 is the 15 W adjustment.

## % Mod Circuit

The Demod Audio from the selected filter is amplified by U4784A. The signal is then output to the DEMOD OUTPUT Connector, to the Oscilloscope and to the front panel controls. The signal also is switched through selected resistors by U4790, as controlled by the DEV/PWR Control. U4790 also switches in the FM Zero line or the AM Zero line, as selected by switch U4774B. Whenever pin 6 of U4790 is high, as controlled by the DEV/PWR Control, all channels of U4790 are off. When pin 6 of U4790 is low, one pair of channels out of U4790 is on. Pins 9 and 10 determine which pair of channels is on, as controlled by the DEV/PWR A and B lines.

When U4774B selects FM Zero, a preset zero is selected by U4769A, B and C or by U4719C. Only one of these switches will be on at any one time. The switches are driven by the FM1 thru FM4 lines to select a zero for each of the four FM bandwidths. RN4702 - A thru D sets the zero for the bandwidths.

The % Mod Scale part of the circuit consists of U4784B, U4770, U4773, U4771 and U4785B. U4785B buffers the offset signal. The offset signal is a DC level which is used to zero the % AM/kHz DEV level. U4784B amplifies the demodulated audio signal. U4770A and B form a precision full-wave rectifier. The output of the rectifier is smoothed out by R4899 and C4813. U4773B amplifies the charge on C4813. The output of U4773B is the average % Modulation/kHz Deviation. The output of the full-wave rectifier, at pin 7 of U4770B, is also applied to U4771, which is a peak detector. U4771 will charge C4807 via CR4722. The output voltage will be equal to the peak of the full-wave rectifier output. The output signal is applied to U4773A, which buffers the output of U4771 before applying it to U4774C. U4774C selects between Peak % AM/kHz DEV and Peak Average % AM/FM DEV. The output of U4774C is applied to the DEV/% Mod Meter Select Switch.

## Phase Lock Light Logic Circuit

Three phase-lock control signals are input to the Demod Audio PC Board: High Loop lock, Low Loop lock and Duplex lock. When all three of these lines are high, pin 3 of U4777 is low. When any of these lines are low, their respective diode (CR4741, CR4743 or CR4742) will be reverse biased, causing pin 3 of U4777 to go high. U4777B and U4777C form an oscillator circuit to present alternating highs and lows to pin 12 of

U4777D. When pin 13 of U4777D is low, pin 11 will be high to turn on Q4714 and light the Freq LOCK Indicator Lamp on the front panel. When pin 13 of U4777D is high, the Freq LOCK Indicator Lamp will flash off and on at the same frequency as the oscillator at pin 12. Also, when pin 3 of U4777 is high, Q4715 will conduct to output a +12 V Unlock signal to the I/O PC Board.

When the GEN/LOCK Control is not in the Lock position, +12 V is input at pin 3 of P4703. This will cause the Freq LOCK Indicator Lamp to flash and +12 V to be output to the I/O board in the same manner as the phase-lock lines.

### Battery Timer and Control Circuit

The Battery Timer and Control Circuit consists of Q4713, Q4719, Q4716, U4791, U4776 and U4787. Q4716 conducts when the front panel PWR/OFF/BATT Switch is set to BATT. When Q4716 conducts, U4776A changes states. CR4733, CR4735, C4817 and C4829 determine which input (S or R) to flip-flop U4776A will become active. If the flip-flop is set, C4829 will be fully charged, allowing the reset line to go high first. The set input cannot go high until C4817 charges. By the time C4817 charges, C4833 is charged and Q4716 is no longer able to drive an input of the flip-flop. If the flip-flop is reset when Q4716 conducts, the opposite actions occur. Thus, the flip-flop toggles each time Q4716 starts conducting.

The Q output of U4776A turns on Q4719, which outputs a control signal to put the FM/AM-1500 power supply into battery operation. The  $\bar{Q}$  output, when low, turns on Q4713, causing power to be applied to the battery timer and to the low voltage cutoff. The battery timer, U4791, produces a logic 1 at pin 13 after 7 to 11 minutes. This logic 1 will reset flip-flop U4776A via CR4738. When the flip-flop is reset, the power supply, battery timer and low voltage cutoff circuits are turned off.

The low voltage cutoff circuit consists of a comparator, U4787, and a zener diode, CR4736. A sample of the battery voltage is applied to the negative input of the comparator via a voltage divider consisting of R4982, R4981 and R4919. The positive side of the comparator is connected to the zener diode, which regulates it to approximately 5 volts. When the battery voltage drops below a predetermined level, the negative input of the comparator will fall below the zener diode voltage. This causes the output of the comparator to go positive and reset flip-flop U4776A, turning the FM/AM-1500 off.

### AM Modulation Leveler Circuit

AM modulation is input at pin 13 of P4702 from the Dual Tone Generator PC Board. U4786A and U4786B amplify the signal for output to the Output Amplifier Module, which controls the AM modulator level of the Duplex Offset Module. R4973 is provided for AM% modulation adjustment. R4963 is provided for RF level adjustment. R4961 is provided for RF level linearity adjustment.

## AM Flywheel Circuit

The AM Flywheel circuit consists of Q4703, U4715, U4716, U4717, U4731 and U4732. Q4703 buffers the 700 kHz IF signal input at J4706 and applies this signal to a CMOS Switch, U4715, and to a comparator, U4716. U4716 is used in FM only. The output of U4716 is a square wave with a frequency equal to the frequency of the 700 kHz IF. U4715, along with U4717, operates as a phase/frequency detector. The output of the integrator, U4717, is a DC voltage which steers the output frequency of the VCO, U4732, in the appropriate direction to make the frequencies equal at pins 1 and 13 of U4715. This phase-locked loop generates a square wave, at pin 4 of U4732, with a frequency equal to the 700 kHz IF input. When over-modulation of the carrier signal occurs, integrator U4717 holds its output at a relatively constant level during the interval when the carrier is suppressed. When the carrier is not suppressed, the phase-lock loop corrects for any drift which may have occurred during the time the carrier was suppressed. U4731B selects between the output of the phase-locked loop for AM demodulation and the output of the comparator, U4716, for FM demodulation.

## Time Base Circuit

The Time Base circuit consists of Q4711, U4739, U4724, U4725, U4709, U4711, U4710, U4748B, U4748C, U4760D, U4740 and U4758. This circuit provides the time base frequency for the frequency error counter.

Q4711 buffers the 10 kHz input from the Clock Divider, at pin 18 of P4703, and applies this signal to U4739A and U4709B. U4739A, U4739B, U4724A and U4724B are decade counters which function as divide-by 10 frequency dividers. These dividers produce frequencies at 1 kHz, 100 Hz and 10 Hz. These outputs are applied to CMOS Switches U4725A, U4725C and U4725B, respectively. The four CMOS Switches (U4725B, U4725C, U4725A and U4709B) select one of the time base frequencies of 10 Hz, 100 Hz, 1 kHz and 10 kHz, respectively. The switches are driven by the time base select logic.

The time base select logic consists of U4713, U4710A, U4710B, U4710C, U4711A, U4711B and U4711C. Table 2-2b is a truth table which describes the operation of the time base logic. The time base select logic receives frequency error settings from the I/O PC Board and turns on the appropriate CMOS Switch. In addition, the time base select logic also produces a control line which informs the frequency error counter when to count in the audio mode. This control line is driven by pin 10 of U4710C.

U4760D, U4748B and U4748C drive control lines for the frequency error counter. These control lines are the 1.0 second, 0.1 second and 0.01 second time bases. When all three of these lines are inactive, the 0.001 second time base is selected. The selected time base line is applied to U4740 which, along with U4758A, produces the gate for the frequency error counter.

| FREQ ERROR |   |   |   | U4710C<br>Pin 10 | U4711A<br>Pin 8 | U4711B<br>Pin 6 | U4710B<br>Pin 6 | U4710A<br>Pin 8 | U4713<br>Pin 2 |
|------------|---|---|---|------------------|-----------------|-----------------|-----------------|-----------------|----------------|
| D          | C | B | A |                  |                 |                 |                 |                 |                |
| 0          | 0 | 0 | 0 | 1                | 1               | 0               | 1               | 1               | 0              |
| 0          | 0 | 0 | 1 | 1                | 1               | 1               | 0               | 1               | 0              |
| 0          | 0 | 1 | 0 | 1                | 1               | 1               | 1               | 1               | 1              |
| 0          | 0 | 1 | 1 | 0                | 0               | 1               | 1               | 1               | 0              |
| 0          | 1 | 0 | 0 | 0                | 0               | 1               | 1               | 0               | 0              |
| 0          | 1 | 0 | 1 | 0                | 1               | 0               | 1               | 1               | 0              |
| 0          | 1 | 1 | 0 | 0                | 1               | 0               | 1               | 0               | 0              |
| 0          | 1 | 1 | 1 | 0                | 1               | 1               | 0               | 1               | 0              |
| 1          | 0 | 0 | 0 | 0                | 1               | 1               | 0               | 0               | 0              |

Table 2-3a Time Base Logic  
(Effective Ser. No. 1426 and on)

Assume that U4758A is reset and that U4740 has just been loaded with 0000(2). Under these conditions, the COUNT ENABLE line is high, stopping the frequency error counter from counting. On the next rising edge of the clock, the counter decrements, reducing the contents of the counter by 1 and yielding a count of 1001(2). When this happens, the output at pin 2 of U4740 goes high, causing U4758 to change states and the COUNT ENABLE line to go low (active state). The COUNT ENABLE line stays low for 10 counts. When the counter underflows from 0000(2) to 1001(2), pin 2 of U4740 again makes a low to high transition, causing U4758 to change states and the COUNT ENABLE line to go high (inactive state). When this line goes high, U4740 is set to 0000(2) via C4795 and R4883. One count later, the counter again underflows from 0000(2) to 1001(2), causing U4758 to change states. The counter, U4740, is then allowed to decrement for ten counts and then the cycle repeats itself. The net result is a pulse which is high for one clock period and low for ten clock periods, and which appears on the COUNT ENABLE line.

#### Frequency Error Counter Circuit

The Frequency Error Counter Circuit consists of the following IC's:

|        |        |
|--------|--------|
| U4746  | U4764  |
| U4728  | U4761  |
| U4763  | U4759  |
| U4745  | U4775  |
| U4727  | U4731A |
| U4765  | U4709  |
| U4744  | U4747  |
| U4742  | U4748  |
| U4741  | U4766  |
| U4731C | U4758B |

The frequency error counter is a 24 bit binary, presettable up/down counter. Only the lower 8 bits are available at its output. These 8 bits represent the frequency error. When the frequency error counter is in the audio mode, it functions as an up/down counter. At the beginning of each conversion, the frequency error counter is preset to  $C0080(H)$ . During the first gate, the counter counts up using the unknown tone. During the second gate, the counter counts down using the reference tone. If the two tones are equal, the resulting count is  $C0080(H)$ . The lower 8 bits ( $80(H)$ ) are latched and applied to the digital to analog converter and to the I/O PC Board.  $80(H)$  is interpreted as zero. Anything greater than this is interpreted as positive, while anything less is interpreted as negative. If the unknown tone is greater than the reference tone, the result will be positive since the counter counted up more than it counted down. If the unknown tone is less than the reference tone, the result will be negative since the counter counted down more counts than it counted up.

When operating in the RF mode, the counter counts up only. The counter is loaded with a preset value prior to each gate. The gate enables the counting of the 700 kHz IF. If the 700 kHz IF is exactly 700 kHz, the resulting count will be  $C0080(H)$ , which is interpreted as zero. If the 700 kHz IF is less than 700 kHz, the final count will be less than  $C0080(H)$  and will be interpreted as a negative value. If the 700 kHz IF is greater than 700 kHz, the final count will be greater than  $C0080(H)$  and will be interpreted as a positive value. In both audio and RF modes, the difference between  $80(H)$  and the counter's 8 bit output represents the magnitude of the frequency error.

The up/down counter consists of U4743, U4741, U4742, U4745 and U4746. The lower 8 bits of this counter are applied to U4727, which latches the counters' output when the COUNT ENABLE line goes high. The output of U4727 is applied to U4726 and to U4728, a pair of demultiplexers which select between the counter outputs and the OVER/UNDER line.

When an overflow or underflow condition occurs, the upper 12 bits of the counter are applied to the overflow/underflow logic consisting of U4744, U4765B, U4747A, B & C, U4748 A & D and U4766. This logic checks for  $C00(H)$  on the upper 12 bits of the counter. If the count is less than  $C00(H)$ , the logic will indicate an underflow (meter peg = 1; OVER/UNDER = 0). If the count is greater than  $C00(H)$ , an overflow condition is generated (meter peg = 0; OVER/UNDER = 1).

The preset logic, consisting of U4709C, U4775A and U4775B, controls the presetting of the counters. When counting RF, the CMOS Switch, U4709C, applies the COUNT ENABLE signal to the astable multivibrators, U4775 A & B. These astable multivibrators produce a delayed pulse to ensure that everything has settled before presetting the counters. The output of U4775B is applied to the reset inputs of the counters and to the reset input of U4758B. U4758B produces the UP/DOWN count signal and the VAR TONE/REF TONE signal. When in the RF mode, this flip-flop is reset everytime the gate goes high, forcing the counters to count up only.

In the audio mode, the output of U4758B is applied to U4775A by U4709C. In this mode, U4758B is reset on every other gate cycle. During the first cycle, U4731A selects the unknown tone and the UP/DOWN line is high. During the second gate cycle, U4731A selects the reference tone. The output of U4731A is applied to the clock input of the counters via U4760A. CR4721 disables the clock while the COUNT ENABLE line is high. U4731C selects between audio (output of U4731A) and RF (output of U4731B in the AM Flywheel circuit) as controlled by the UP ON AUDIO line.

#### Overtemp Circuit

When the thermistor in the Power Termination Module senses an overtemp condition, its signal is input at pin 24 of P4703. When pin 2 of U4788 reaches a pre-determined level, pin 6 will go high to turn on Q4720. This will turn on the OVERTEMP Indicator Lamp on the front panel and also send a +12 V on Overtemp signal to the I/O PC Board.

#### Tone Beep Circuit

The KEYDOWN line from the I/O PC Board enters at pin 4 of J4705. When this line is high, Q4707 is on. When this line is low, Q4707 is off to allow the oscillator to function. U4723 and associated components form a 1 kHz Beep Oscillator. R4782 sets the volume level of the Oscillator. The audio-in line at pin 4 of P4702 mixes with the oscillator output and is amplified by U4722, an audio amplifier, for output to the speaker.

## 2-6-4 Oscilloscope Control and Deflection PC Board Detailed Theory

### Control Circuitry

The external input is at J5101 from the front panel SCOPE/SINAD Connector (See Figure 2-16 and the Oscilloscope Control and Deflection PC Board Schematic in Section 7 of this Manual). The setting of the DEV/VERT Control (V/div settings) and the DC/AC Switch determine which of relays K5101 thru K5104 will be energized. If K5101 is energized, a SINAD or DC input will be amplified by U5105A and output to the Demod Audio PC Board at pin 6 of P5103. The selected scope input is amplified by U5101 and sent to multiplexer U5109. External vertical gain is controlled by R5126. Opto-isolator U5112 couples the VERT VERNIER Control into the selected input when the VERT VERNIER Control is not in CAL position. DS 5101 and the front panel UNCAL Indicator Lamp (Vertical) will be illuminated if the VERT VERNIER Control is not in CAL.

The 700 kHz IF signal from the 89-90 MHz Receiver module is input at J5105 and is sent to three multiplexers. Multiplexer U5104C, when control line 9 is low, will route the 700 kHz IF to serve as a control line for multiplexers U5109 and U5110B. The DEV/VERT Control will add the logic level high to the 700 kHz IF in any kHz/DIV position. The logic high will forward bias CR5149 to input the 700 kHz IF through U5104C and out to U5109. The logic high will also serve as a control line for U5108C.

The Demod input at pin 13 of P5102 splits in two directions. One line goes to pin 3 of U5108C and is selected when pin 9 goes high, then sent to the sweep circuit. The other line is sent through a resistor network and U5102B, which is controlled by kHz/DIV positions of the DEV/VERT Control. The selected output of U5102B is amplified by U5103B and switched through U5104C, when pin 9 of U5104C goes high, to U5109.

The TONES position of the HORIZ Control has a control line for U5108A and U5108B. When the +12V on TONES line, input at pin 20 of P5102, is low, U5108B selects pin 2 as an input and channels the sweep circuit information to U5110B. U5108A will select pin 12 as an input when the +12V on TONES line goes low, thus allowing sweep circuit information to be passed to U5109.

The Sweep Control B and A inputs at pins 25 and 23 of P5102 are controlled by the HORIZ Control on the front panel. These lines are the control lines for U5107A in the sweep circuit.

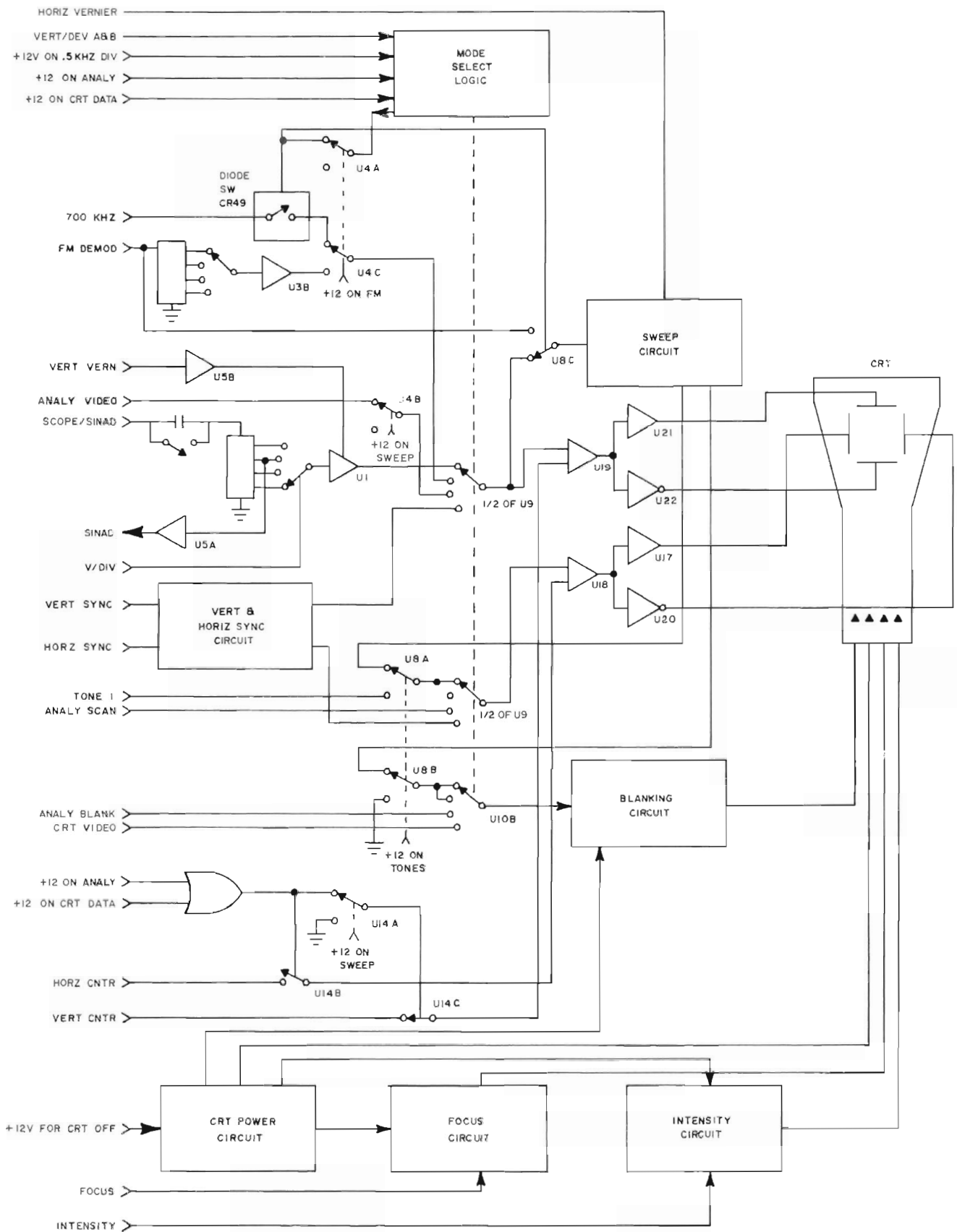


Figure 2-16 Oscilloscope Control and Deflection PC Board Detailed Block Diagram



### Mode Select Logic

The Mode Select Logic controls the states of switches U5109, U5110 and U5104C. The Mode Select Logic consists of CR5147, CR5148, CR5115 thru CR5118, Q5113, R5151 and R5152. This logic selects the appropriate operating mode of the CRT, based upon the states of the Vert/Dev A, Vert/Dev B, +12 V on Analyzer, +12 V on CRT Data and +12 V on .5 kHz/DIV lines.

### Sweep Circuit

Q5108 and Q5110 act as the control flip-flop for the sweep circuit. Q5107 and Q5111 are turned on and off by the flip-flop, and, in turn, discharge the selected capacitor on the input lines of U5107. U5107A selects the proper capacitor for the sweep rate selected by the setting of the front panel HORIZ Control (Sweep Control A and B lines) and by the sweep width adjustment, R5119. U5107B selects the proper capacitor for wait time as selected by the setting of the front panel HORIZ Control and by the Sweep Rate Adjustment, R5116. In "normal" operation, the sweep circuit is a free-running oscillator. When a sync signal is selected at pin 5 of U5108C, U5111 acts as the trigger for the oscillator. In this condition, Q5103 and Q5109 keep retriggering from occurring until the proper voltage is built up on the base of Q5103.

If the front panel HORIZ VERNIER Control is not in CAL position, the UNCAL Indicator Lamp (Horizontal) on the front panel will be illuminated thru U5106A. The HORIZ VERNIER Control must be in CAL for a calibrated signal.

When Q5108 of the flip-flop is low, a blanking signal is sent through CR5123 to U5108B, pin 2.

### Blanking Circuit

When Q5137 turns on, Q5138 will turn on. This pulls down the collector voltage of Q5136 to about +50 V. Zeners CR5134 and CR5135 each provide 20 V of this drop. When Q5137 turns off, C5166 charges up, pulling the collector of Q5136 back up to about +100 V.

## CRT Power Circuit

Q5131 thru Q5134, and associated components, form the CRT Power Circuit. Q5134 and Q5135, along with T5101, form an inverter circuit. To start the inverter circuit, a pulse is applied to the center tap of the base winding of T5101. This pulse turns on Q5134 and Q5135. When the pulse is removed, the return for the center tap is provided by Q5133, starting the oscillator circuit into oscillation. The output of the inverter is produced in the three secondary windings of T5101. The 2-turn winding provides filament voltage for the CRT, V6401. This winding is connected to the cathode to prevent internal arcing between the cathode and filaments of the CRT. The 80-turn winding passes thru a full-wave rectifier consisting of CR5141 thru CR5144. The output of this full-wave rectifier is approximately +200 VDC, which is used to supply the deflection amplifiers and the tube bias circuits. The 376-turn winding of T5701 is applied to a voltage doubler, which produces approximately -2100 VDC to the Intensity, Focus and Blanking Circuits.

The on/off control of the inverter is determined by the state of pin 22 of P5103. When this line is at +12 V, Q5132 is on, turning off Q5131. Q5133 is turned off, removing the return path for the currents which drive Q5135 and Q5134. As a result, the inverter shuts off. When pin 22 of P5103 goes low, Q5133 is turned on and Q5132 is turned off. When Q5132 turns off, Q5131 conducts and C5155 charges. When C5155 is fully charged, Q5131 will shut off. The output of Q5131 is the start pulse for the inverter.

## Intensity Circuit

The front panel INTENSITY Control line is input at pin 21 of P5103. R51153 is provided to set line voltage. Op-amp U5126 is coupled into the circuit through opto-isolator U5128 which stabilizes any linearity and current drift. When +12 V is applied to pin 3 of U5126 through CR5146 from the CRT Data line, more brightness is added for raster scan. Opto-isolator U5116 turns on to turn Q5130 off. This allows a maximum voltage of +120 V to be applied to the CRT. CR5133, a +120 V Zener, sets this voltage.

## Focus Circuit

The Focus Circuit operates in much the same fashion as the Intensity Circuit. The front panel FOCUS Control line is input at pin 23 of P5103. R5182 sets line voltage. Op-amp U5125 is coupled through opto-isolators U5127 and U5115 to turn Q5129 on or off.

### Vertical Deflection Circuit

If the +12 V on Sweep line (pin 11 of U5114A) is low, U5114C selects pin 5 as the input line. The VERT POS Control on the front panel is then summed into Op-amp U5119 with the Vertical input line. R9561 is the Vert Centering Adjustment, and R5188 is the Vert Gain Adjustment. The output of U5119 feeds U5121 for the non-inverted deflection plate control line. U5122 inverts the output of U5119 for the inverted deflection plate control line. When relays K5105 and K5106 are energized by the +12 V on the CRT Data line, the circuit is slowed down for raster control.

### Horizontal Deflection Circuit

The Horizontal Deflection Circuit operates similarly to the Vertical Deflection Circuit, but about twice as fast. When all three control lines at pin 10 of U5114B (+12 V on Analyzer, +12 V on CRT Data or +12 V on Sweep) are low, pin 2 is selected as the input line. The front panel HORIZ POS Control is summed in U5118 with the Horizontal input line. U5117 is the non-inverting control, while U5120 is the inverting control. Q5122 and Q5123 are constant-current transistors used in conjunction with R9528 to set astigmatism control.

### Vertical and Horizontal Drive Circuit

The VERT SYNC and HORIZ SYNC inputs at pins 26 and 24 of P5102 are driven by the CPU/MEMORY PC Board to control menu displays on the CRT. Q5115 and Q5139 are current limiters which shape the vertical and horizontal pulses. U5103A inverts the VERT SYNC pulse. Both pulses are applied to U5109 and are selected when the +12 V on CRT DATA control line is high.

## 2-7 GENERATOR FUNCTIONAL THEORY

In "normal" operation (when the DISPLAY Control is in any position other than "SWEEP" or "TRACK"), the IF source for the Generator Functional Block is the 79.3 - 78.3001 MHz signal input into the FM Generator Module from the Low Loop section of the Frequency Synthesis Functional Block (See Figure 2-17). When the DISPLAY Control is in "TRACK" or "SWEEP", the IF source is the 84.3 - 73.3 MHz signal from the Spectrum Analyzer Functional Block. The IF source is mixed with a 10.7 MHz VCO signal and is output to the Generator Mixer Module as an approximate 68.6 MHz signal. The 10.7 MHz VCO signal contains FM information from the Dual Tone Generator PC Board and is either phase-locked with a 1 kHz reference signal or is controlled by the GEN/LOCK Control on the front panel. The GEN/LOCK Control allows the output frequency to be varied + or -10 kHz. A 158.6 MHz signal from the Generator Mixer Module is used as the source for the phase-locking of the 10.7 MHz VCO signal.

The Generator Mixer Module filters and converts the approximate 68.6 MHz IF and outputs it as a 90 MHz signal to the 1300 MHz IF Generator Module. The 90 MHz IF is converted three times in the 1300 MHz IF Generator Module: first, to 1120 MHz, by mixing with a 1210 MHz High Loop signal; second, to 1250 to 1350 MHz by mixing with a 130 to 230 MHz Duplex Offset signal; and third, to a 0 - 1000 MHz output signal by mixing with a 1300 to 2299 MHz High Loop Signal.

The 0 - 1000 MHz output signal is input to the Output Amp module, which boosts the output level to the Variable Attenuator, controls the Duplex Offset Module RF level (AM), and (when in Generate Simplex mode) outputs a crossfeed signal to the Receiver Functional Block.

From the Variable Attenuator, the output signal is channeled to the Power Termination Module. In the Generate Simplex mode of operation, the RF signal will be output to the TRANS/-40 dB DUPLEX Connector. In the Generate Duplex mode of operation, the RF signal will be output to the DUPLEX OUTPUT Connector and, at 40 dB down, to the TRANS/-40 dB DUPLEX Connector.

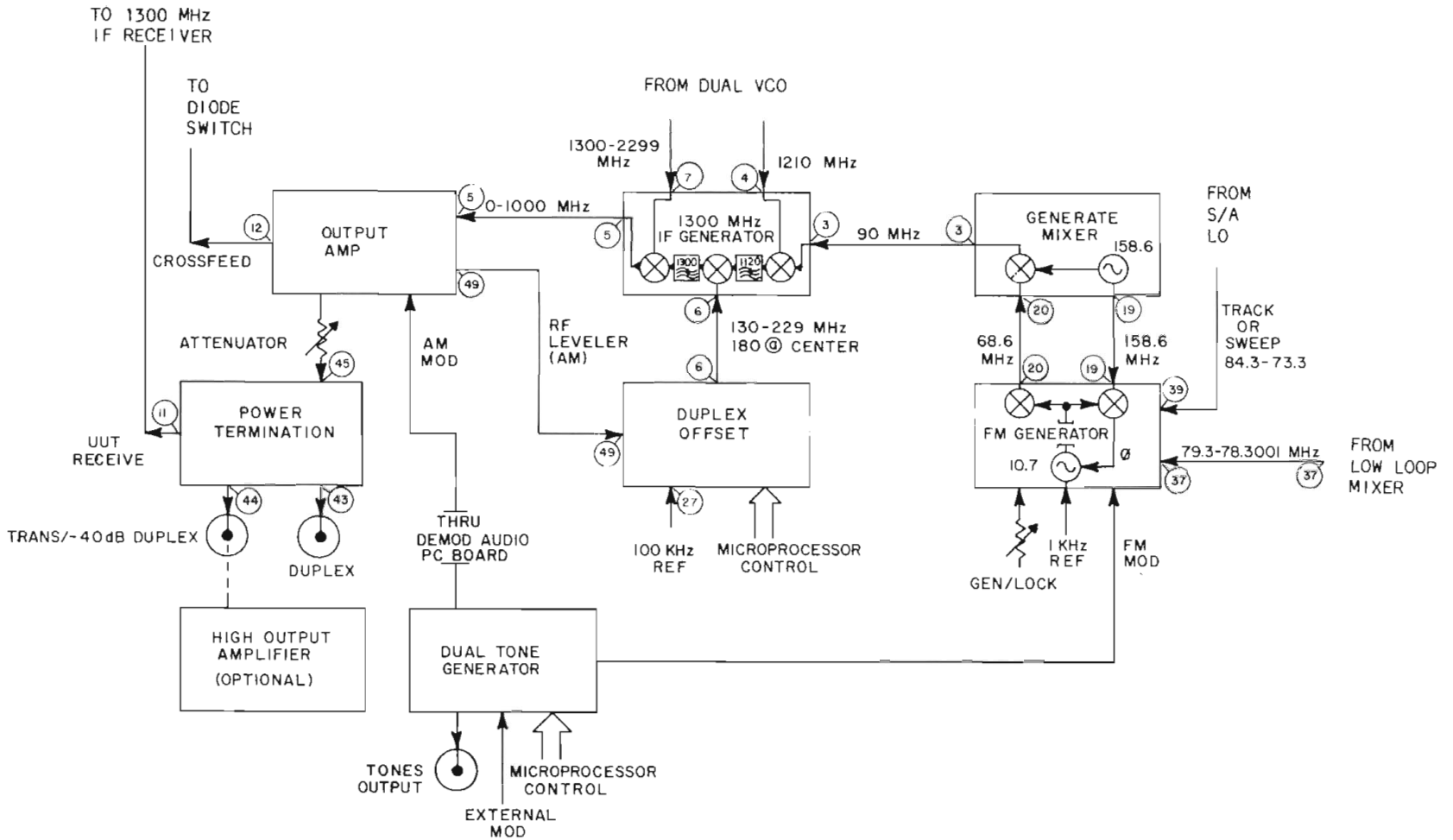


Figure 2-17 Generator Functional Block Diagram

## 2-7-1 FM Generator Module Detailed Theory

U3301A acts as a switch to select the input line as either 79.3-78.3001 MHz from the Low Loop Mixer Module or as 84.3-73.3 MHz from the Spectrum Analyzer LO Module (See Figure 2-18 and the FM Generator Schematic in Section 7 of this Manual). When +12 V is applied to pin 3 of U3301A, the Spectrum Analyzer LO input is selected. If +12 V is not present at pin 3 of U3301A, the Low Loop Mixer input is selected. The +12 V is active when the front panel DISPLAY Control is set to "SWEEP" or "TRACK".

The selected input signal is amplified by Q3301 and mixed in MXR3301 with a 10.7 MHz VCO signal. The difference frequency of approximately 68.6 MHz is amplified in Q3302 and output at J4206.

The 10.7 MHz VCO signal is also mixed, at MXR3302, with the 158.6 MHz signal input at J4205 from the Generator Mixer Module. The sum frequency of 169.3 MHz is filtered and amplified for driving the frequency divider chain U3305, U3306 and U3304. U3305 and U3306 are  $\div 10$  frequency dividers and U3304 is a  $\div 1693$  frequency divider. The resultant 1 kHz is applied to pin 3 of U3303 to phase-lock the 10.7 MHz VCO with a 1 kHz reference signal.

Transistor Q3308 and associated components form a 10.7 MHz voltage controlled oscillator (VCO). The adjustment of C3367 is used to set a tune voltage of approximately 3 volts at pin 15 of U3302B. Q3308 is operating properly when there is a negative 2 to 4 volts on its gate (pin 3).

Zener diode CR3311 subregulates the +12 volt supply voltage to +6.9 volts to operate Q3308, Q3303 and IC U3303.

IC U3302B acts as a switch control of the 10.7 MHz VCO between the phase-lock loop and the GEN/LOCK Control on the front panel. When the GEN/LOCK Control is switched out of detent, +12 V is applied to pin 10 of U3302B, causing control of the VCO to be assumed by the GEN/LOCK Control. This allows the output frequency to be manually varied +10 kHz and -10 kHz.

FM modulation, controlled by the Dual Tone Generator, is input at pin 9 of J4203. The FM modulation voltage is set by R3333 and applied to the VCO frequency through varactors CR3309 and CR3310.

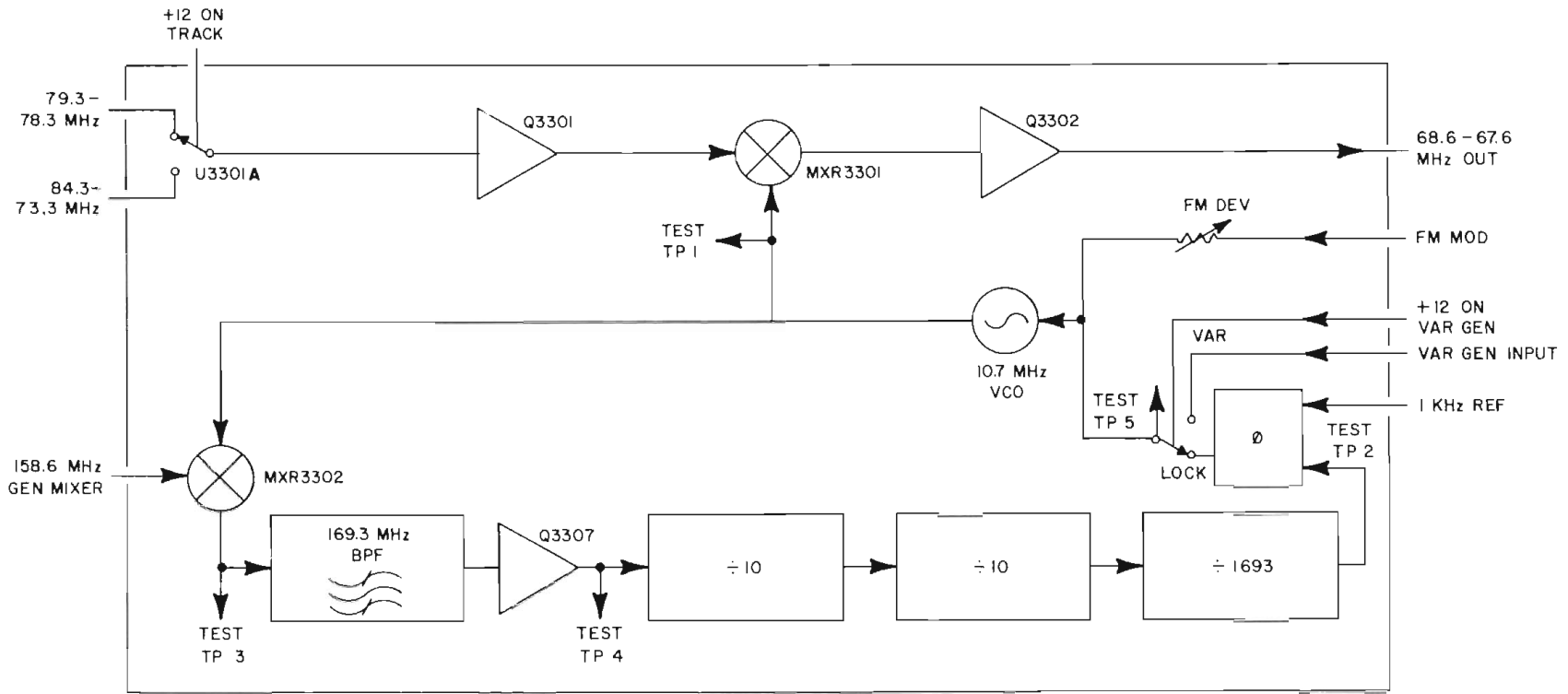


Figure 2-18 FM Generator Detailed Block Diagram

## 2-7-2 Generator Mixer Module Detailed Theory

A 68.6 MHz signal from the FM Generator Module is input at J4401, attenuated by the network of R3401, R3402 and R3403, and filtered before being applied to MXR3401. (See Figure 2-19 and the Generator Mixer Schematic in Section 7 of this Manual).

A 158.6 MHz crystal oscillator frequency, formed by Y3401 and associated components, is output at J4402 to the FM Generator Module and also applied to MXR3401. In MXR3401, the 158.6 MHz is mixed with the 68.6 MHz and the result is a 90 MHz signal that moves in the opposite direction of the 2nd I.F. Receive Frequency. The 90 MHz signal is band-pass filtered and output at J4403 to the 1300 MHz I.F. Generator Module. The DC control voltage for the 90 MHz filters is controlled by U3401, which acts as a switch. In "normal" operation, the DC control voltage is set by variable resistors R3412 and R3423. If the front panel DISPLAY Control is in "SWEEP" or "TRACK", +12 V switches U3401 to the control line at pin 7 of J4404, and the DC control voltage is set by U3402 and U3403, through their variable resistors.

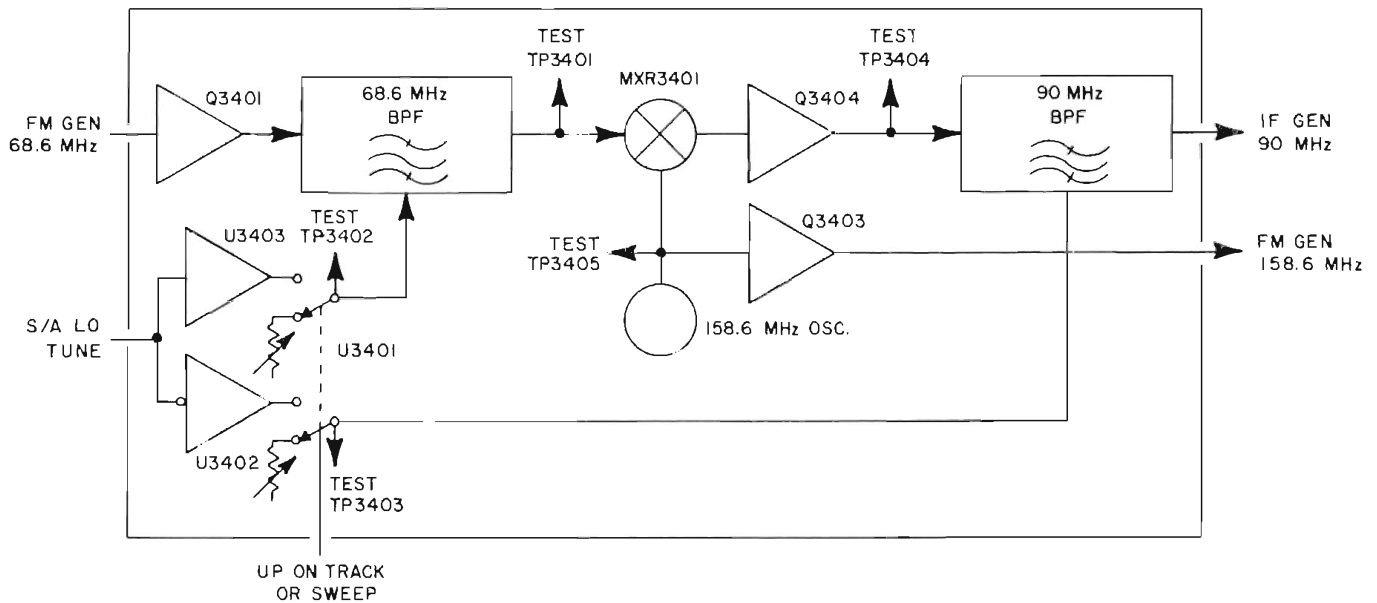


Figure 2-19 Generator Mixer Detailed Block Diagram



### 2-7-3 1300 MHz IF Generator Module Detailed Theory

The 90 MHz signal from the Generator Mixer Module enters at J1202 and is mixed in MXR1201 with a 1210 MHz signal, input at J1201, from the High Loop section of the Frequency Synthesis Functional Block (See Figure 2-20 and the 1300IF Generator Module Schematic in Section 7 of this Manual). The difference frequency of 1120 MHz is band-pass filtered in Z1201 and amplified in three stages consisting of Q1601, Q1602 and Q1603 and their associated components. The 1120 MHz signal is mixed in MXR1202 with the input, at J1203, from the Duplex Offset Module, which is normally 180 MHz. The input from the Duplex Offset Module may be 180 MHz + or -49.99 MHz if an offset frequency is desired.

The sum of the signals from MXR1202 is 1300 MHz ( $\pm 49.99$  MHz). The sum signal is band-pass filtered by Z1202, which must pass a 1250-1350 MHz offset signal. The filtered 1300 MHz signal is amplified by Q1501 and Q1502 and mixed in MXR1203 with a 1300-2300 MHz signal from the High Loop section of the Frequency Synthesis Block.

The 0-1000 MHz signal output of MXR1203 is filtered by a 1000 MHz low-pass filter, FL1203, and output at J1205 to the Output Amplifier Module.

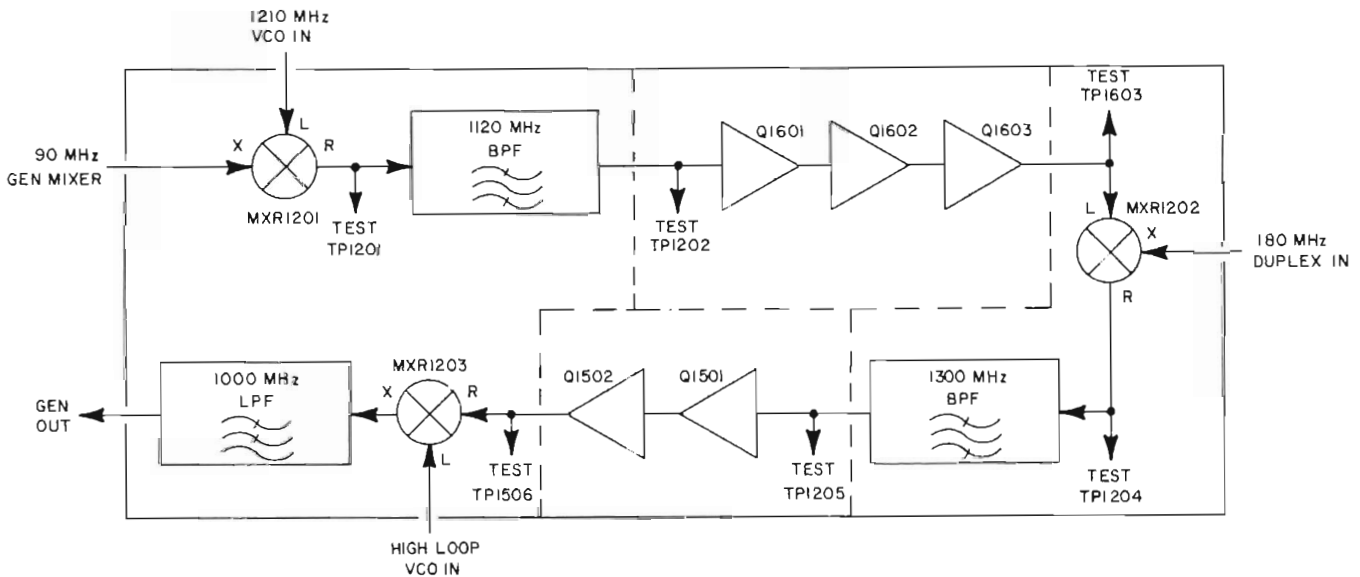


Figure 2-20 1300 MHz IF Generator Detailed Block Diagram

## 2-7-4 Duplex Offset Module Detailed Theory

The Duplex Offset Module generates an 130-229.99 MHz synthesized RF signal that is mixed in the 1300 MHz I.F. Generator Module to produce a 0 to  $\pm 49.99$  MHz offset frequency.

The RF signal is generated in one of two VCO's. Transistors Q2701 and Q2702, and associated components, form a 130-179.99 MHz VCO when Q2704 is off. Transistor Q2703, and associated components, forms a 180-229.99 MHz VCO when Q2705 is off. The selected VCO signal is buffered by Q2706 before being sent to the output circuit and to the programmable divider circuit.

### Programmable Divider Circuit

Q2713 amplifies the selected VCO signal to drive the programmable divider circuit. U2701 and U2702 together operate as a  $\div 100/\div 101$  swallow counter. U2701 by itself is a  $\div 10/\div 11$  prescaler. When U2703 and U2704 count down to 00, both pin 12's will go high, changing U2701 to a  $\div 10$  and disabling U2703 from counting until the next load condition.

When U2706 and U2707 have reached count 000, U2705 will count down to 002. At count 002, the look-ahead circuit of U2713, U2714 and U2709A will set pin 14 of U2709A high. At count 001 on U2705, the clock pulse at pin 1 of U2709A will set the  $\bar{Q}$  output at pin 13 low, pulling down the load lines of the counters (pin 11), allowing the counters to load the frequency select data. The Q output of U2709A (pin 12) goes high, causing U2701 to remain as a  $\div 10$ . At count 000 on U2705, U2709A will be reset to await a new load condition.

### Phase/Frequency Detect Circuit

A 100 kHz reference frequency is input at J3203 from the Clock Divider Module. The 100 kHz is divided by 10 in U2708 to produce a 10 kHz reference signal at pin 12, which is compared with the 10 kHz clock of the programmable divider circuit. Pin 8 of U2708 is a  $\div 2$ , or 50 kHz output. U2709B is the slip flip-flop for the circuit. If the Q output at pin 9 of U2709B goes high, the logic gates of U2714A, U2711A and U2711B will shut off the 100 kHz reference signal at pin 1 of U2708. If the  $\bar{Q}$  output of pin 8 of U2709B and the Q output at pin 12 of U2709A are not high at the same time, pin 8 of U2711C will go high, making pin 11 of U2711D go high. This condition causes Q2709 to turn on and, through the Demod Audio PC Board, turn off the Freq LOCK Indicator Lamp on the front panel.

The Q output at pin 12 of U2709A acts as the clear input at pin 6 of U2709B. When the Q output at pin 9 of U2709B and the 10 kHz reference line at pin 12 of U2708 are both high, the phase lock sample is taken. The 10 kHz reference pulse out of Q2711 forms a ramp from the leading edge of the square wave. The 10 kHz divider forms the sample pulse time at C2737 that gates the first sampler of U2715C. A second sample

pulse time is formed at C2742 that gates a second sampler at U2715A. The DC voltage from the sampler is integrated at Q2715 and Q2716 to control the tune voltage and slew the VCO frequency.

### Output Circuit

The RF signal to the output circuit is amplified by Q2710 and Q2708 to drive the low-pass filter and the modulator. When the 130-179.99 MHz VCO range is selected, Q2718 is turned on to add more inductance into the low-pass filter. The RF signal out of the low-pass filter is passed through CR2705 and CR2704, which together act as a diode switch to add amplitude modulation (RF Leveler) from the Output Amp Module. The 130-230 MHz output at J3201 is sent to the 1300 MHz IF Generator Module.

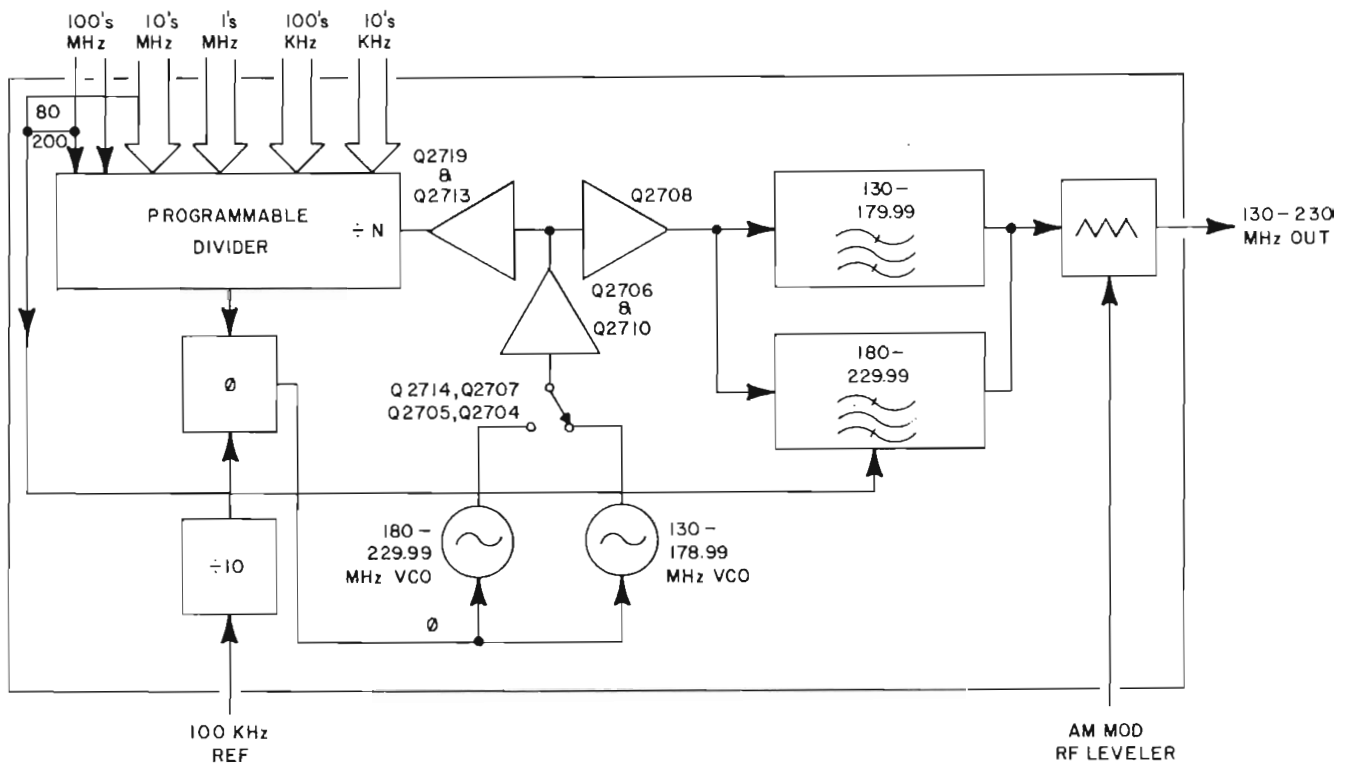


Figure 2-21 Duplex Offset Detailed Block Diagram

### 2-7-5 Output Amplifier Module Detailed Theory

The Output Amplifier Module receives the 0-1000 MHz signal from the 1300 MHz IF Generator Module at J801 (See Figure 2-22 and the Output Amplifier Schematic in Section 7 of this Manual). U901 amplifies the signal to drive three discrete stages consisting of Q901, Q903 and Q905. The output signal at J803 is +38 dBm above the input signal.

The output level is detected by CR906, CR907 and U902B. AM modulation (from the Demod Audio PC Board, as generated by the Dual Tone Generator PC Board) is added at pin 2 of U902A. The output at J802 is sent to the Duplex Offset Module for RF Leveler control.

In the Generate Simplex mode of operation, the +12 V applied at pin 3 of P805 reverse-biases CR903, CR904 and CR905 to output a -10 dBm crossfeed signal at J804 to the 1300 MHz IF Receiver Module.

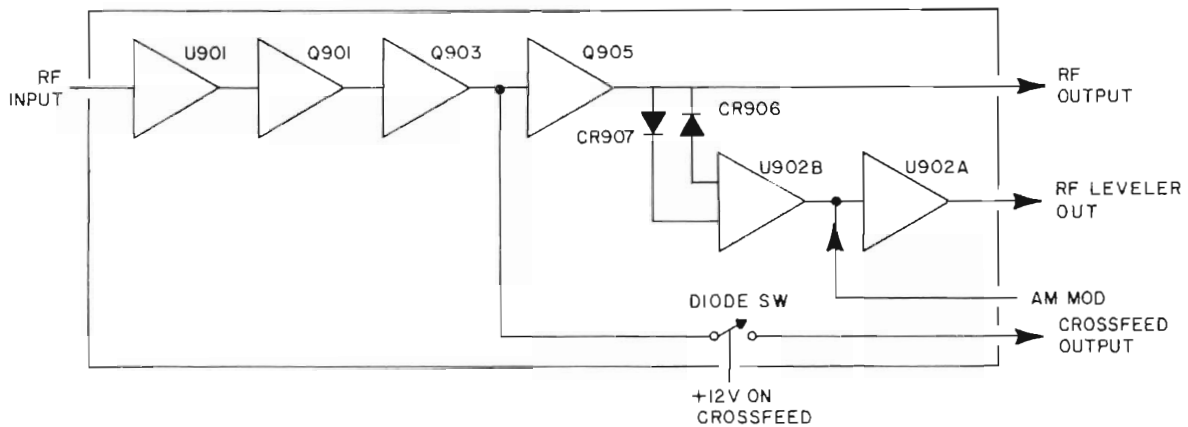


Figure 2-22 Output Amplifier Detailed Block Diagram

## 2-7-6 Power Termination Module Detailed Theory

The generator RF output signal from the Variable Attenuator is input at J9801 (See Figure 2-23 and the Power Termination Schematic in Section 7 of this Manual). In the Generator Simplex mode of operation, the RF signal passes through energized K9801 and K9802 and out J9802 to the TRANS/-40 dB DUPLEX Connector. In the Generator Duplex mode of operation, K9801 and K9802 de-energize to allow the RF signal to be output at J9803 to the DUPLEX OUTPUT Connector. In this mode, the signal that passes through R9804, R9805, R9806 and AT9801 and out J9802 is 40 dB below the actual setting of the Variable Attenuator on the Front Panel.

### **NOTE**

The control logic circuitry for control of the Power Termination relays is on the Demod Audio PC Board.

When the UUT (Unit Under Test) transmits into the TRANS/-40 dB DUPLEX Connector with a power level of 100 mW or greater, the power level is detected by CR9801. K9801 will be de-energized. When this happens, a UUT Receive signal is output at J9804 to the 1300 MHz IF Receiver through the Diode Switch. Diode CR9802 measures the RF power level and sends it to the metering circuitry.

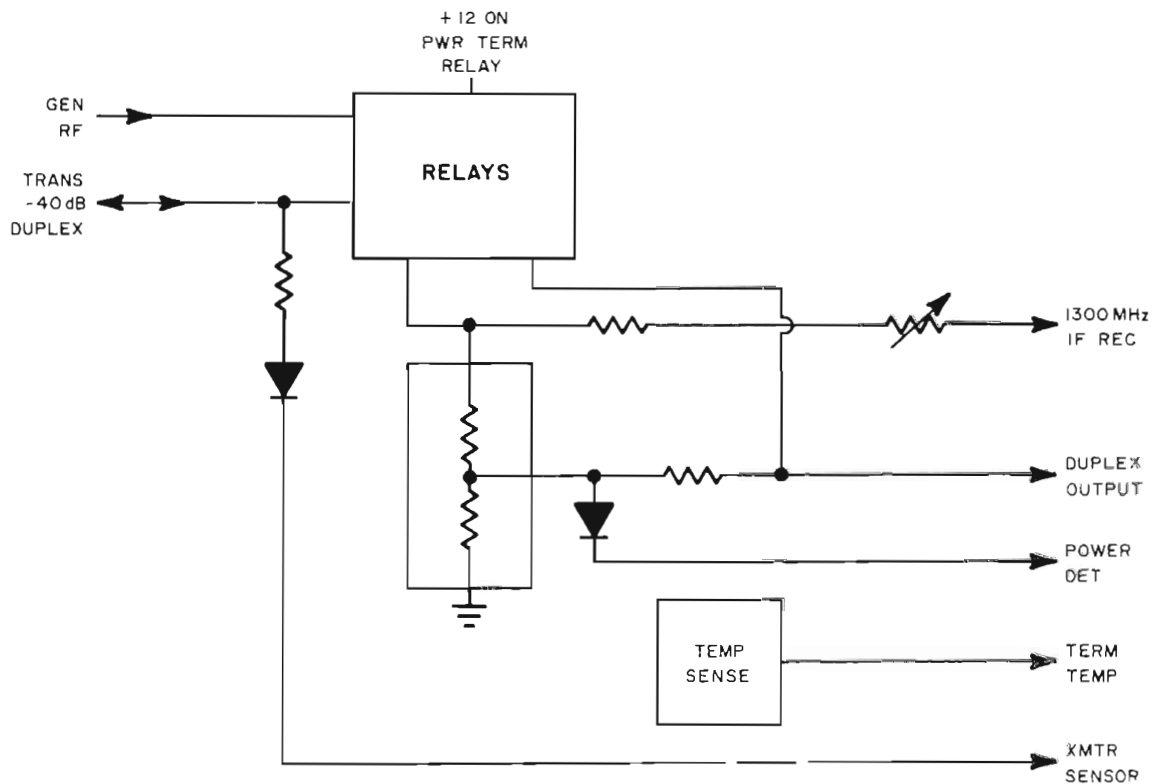


Figure 2-23 Power Termination Detailed Block Diagram

## 2-7-7 Dual Tone Generator PC Board Detailed Theory

The Dual Tone Generator PC Board can generate two separate synthesized tones, programmable from 2 Hz to 30 kHz. (See Figure 2-24 and the Dual Tone Generator PC Board Schematic in Section 7 of this Manual.)

### Crystal Oscillator Circuit

Both tones are referenced to a 3.35544 MHz crystal oscillator frequency, formed by Y4501, Q4501 and associated components. C4505 is provided for oscillator frequency adjustment. The oscillator frequency is divided by two at U4525B, to clock both adder circuits at a rate of 1.67772 MHz. The oscillator also clocks U4529 and U4547 through Q4503, which sets a TTL level.

### Address Select Circuit

The data bus inputs are buffered by U4501 and U4513A, and then sent to the latches. The address bus and write (BWR) inputs are decoded and demultiplexed by U4511 and U4512, then buffered by U4513B and U4554A. U4514, the tone control chip, controls the switch states for the control circuitry and the wave shapes of the ROMs.

### Latches

U4502A, U4503 and U4504 are the Tone 2 latches. U4502B, U4505 and U4506 are the Tone 1 latches. The latches for both tones latch the information from the address select circuit to the adders. Information from the Tone 1 latches is also sent to the Tone Multiplier Circuit through logic gates to serve as control lines.

### Adders

U4518, U4519, U4521, U4522 and U4524 are the Adders for Tone 2. U4536, U4537, R4539, R4540 and U4542 are the Adders for Tone 1. The inputs to the Adders are also used to control the low-pass filter control switches in the Low-Pass Filter Circuit. The Adders are latched together at a 1.67772 MHz rate. The up-counters U4525A and U4543B, are enabled by the carry-out of the last Adder. U4527 and U4545 are buffers. Q4504 and Q4505 are turned on when the up-counters reach end of count.

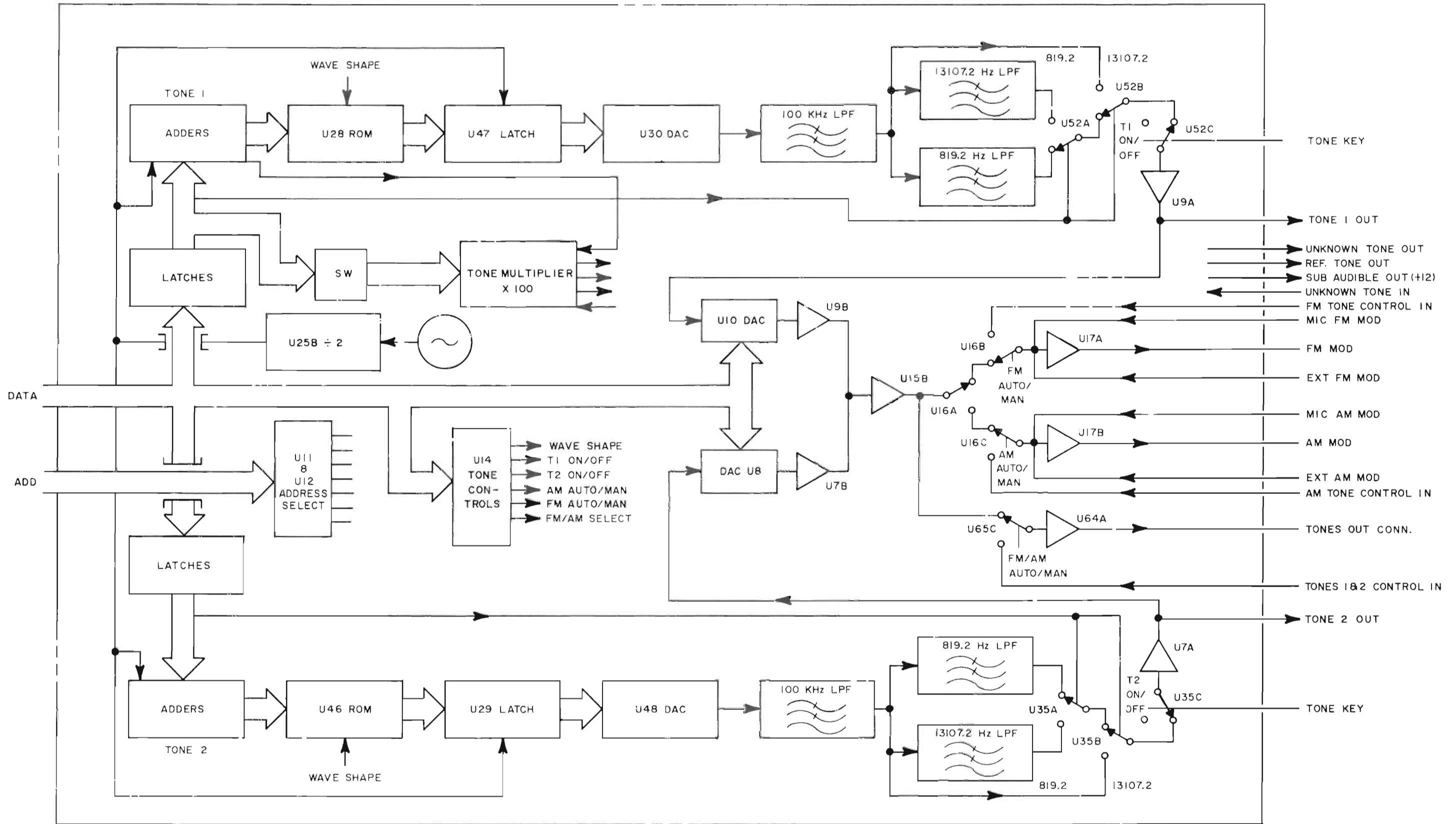


Figure 2-24 Dual Tone Generator  
PC Board Detailed  
Block Diagram

### Low-Pass Filter Circuit

The sine signal is low-pass filtered to smooth the wave form. If the selected tone is 13,107.2 Hz or greater, only the first LPF section is switched in by U4535B and U4552B. If the selected tone is 819.2 Hz to 13,107.1 Hz, U4535A and U4552A select pin 2 as their input lines for a second LPF. If the selected line is less than 819.2 Hz, a third LPF is switched in place of the second LPF at pin 13 of U4535A and U4552A.

### Control Circuitry

After the tone filtering, U4535C and U4552C are used to select whether the tones will be on or off. If their control lines are not active low, the tones will be routed to Op-Amps U4507A and U4509A.

The output of U4507A is routed to the  $V_{REF}$  input of DAC U4508 and to the Tone 1 output line at pin 26 of P4502. The output of U4509A is routed to the  $V_{REF}$  input of DAC U4510 and to the Tone 2 output line at pin 24 of P4502. The tones output lines are routed through the front panel controls for manual operation, and then passed back to the Dual Tone Generator PC Board for switching. The tones lines to the DAC, (U4508 and U4510) are used to convert digital bus information to analog information, which is then passed to the switches.

Switch U4565C selects automatic or manual tones routing to the Tones Output Connector on the front panel, through Op-Amp U4564A. Switch U4516A routes the tones to the AM or FM modulator. Switches U4516B and U4516C select the AM and FM modulation source between front panel control and internal bus control. Also, any external modulation or microphone audio is summed into the AM or FM modulation signal at U4517A and U4517B.

### Tone Multiplier Circuit

The Tone 1 Adder Circuit provides the reference frequency for the Tone Multiplier Circuit at pin 14 of U4559. U4558 decodes its inputs at pins 9 and 10 to select the necessary capacitance for U4559 and U4560. U4559 and U4560 are phase lock loop (PLL) chips, which, together with up-counters U4561 and U4562, multiply the reference tone and the unknown tone by 100 for output to the Demod Audio PC Board.

U4563 outputs a +12 V signal to the Demod Audio PC Board if none of its inputs, from the Tone 1 latches, are high. U4555A and U4557 decode the latch lines for control inputs to U4558.



## 2-7-8 High Output Amplifier Module Detailed Theory

### General

The High Output Amplifier is an optional amplifier device that connects to the TRANS/-40 dB DUPLEX Connector and the EXT AMP Connector on the front panel of the FM/AM-1500 (See the High Loop Amplifier Schematic in Section 7 of this Manual). The device boosts the gain of the generated output signal by +20 dB. In the Generate Mode, +12 VDC applied at P411 energizes relay K7201. The output signal is then coupled through the output connector (J7303), which may be connected directly to a UUT or to an antenna. In the Receive mode, the +12 VDC input goes low and opens the relay. The output connector of the High Output Amplifier is then connected to its antenna connector, J7304. A coax cable may then be connected between the antenna connector and the FM/AM-1500 front panel ANTENNA Connector.

### **CAUTION**

NEVER TRANSMIT, THROUGH DIRECT CABLE CONNECTION,  
INTO THE OUTPUT OR ANTENNA CONNECTORS OF THE  
HIGH OUTPUT AMPLIFIER. TO DO SO WILL DAMAGE  
EITHER THE HIGH OUTPUT AMPLIFIER, THE FM/AM-1500,  
OR BOTH.

### Circuit Description

The generate signal out of the FM/AM-1500 TRANS/-40 dB DUPLEX Connector is input at P402. Q7201 and Q7203 are signal amplifiers which are turned on by +12 VDC applied at P411. Q7202 and associated components act as a constant current source for Q7203, in order to maintain a constant amplification level. Inductors L7201 and L7202 inhibit stray RF from entering the FM/AM-1500 +12 VDC power distribution circuit. Relay K7201 performs the signal switching function.

## 2-8 SPECTRUM ANALYZER FUNCTIONAL THEORY

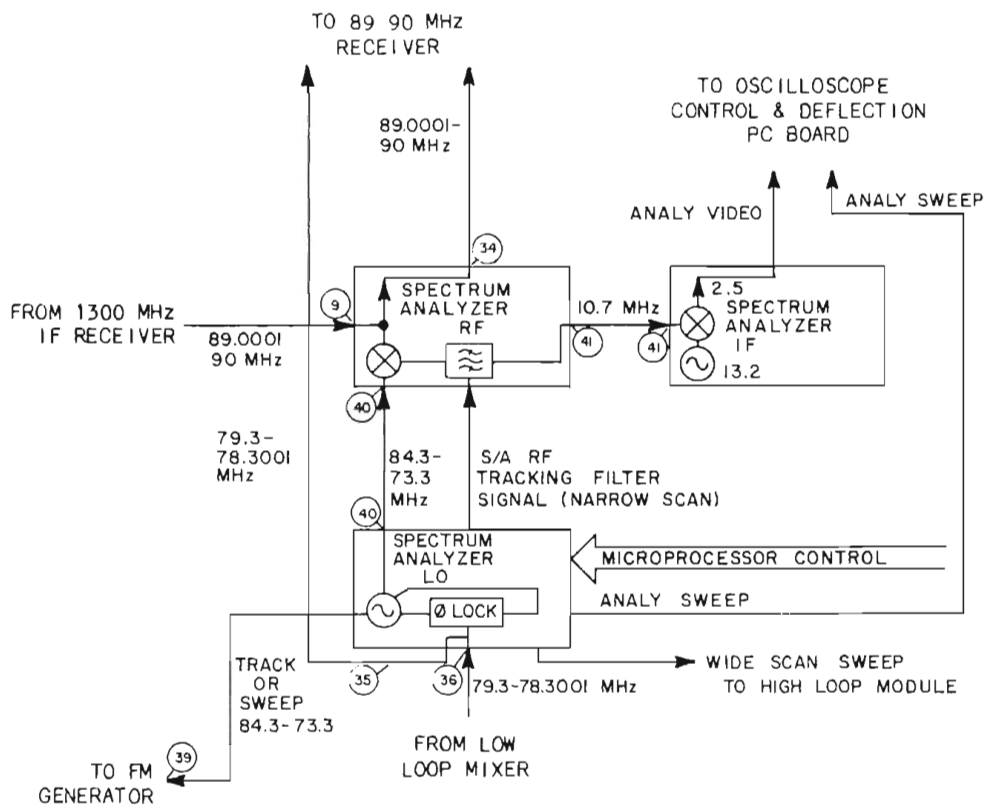


Figure 2-25 Spectrum Analyzer Functional Block Diagram

The Spectrum Analyzer Functional Block contains the Spectrum Analyzer RF, Spectrum Analyzer LO and Spectrum Analyzer IF Modules (See Figure 2-25). The Spectrum Analyzer LO Module is the key module in this Functional Block. It takes the Low Loop Mixer 78.3001 to 79.3 MHz frequency, phase-locks it and converts it to a 73.3001 to 84.3 MHz signal. This signal supplies the Spectrum Analyzer RF Module with its sweep signal. The signal will also take control of the Generator Functional Block in the tracking mode of operation. The LO Module also controls the switching of the tune lines in the High Loop Module and controls the switching of the tracking filter and the band-pass filters in the Spectrum Analyzer RF Module.

The Spectrum Analyzer RF Module mixes the second IF frequency (nominally 90 MHz) from the 1300 MHz IF Receiver and mixes it with the Spectrum Analyzer LO signal to form a 10.7 MHz signal to the Spectrum Analyzer IF Module. The IF Module converts its input, by mixing and down-converting, to a linear signal to drive the CRT, through the Oscilloscope Control and Deflection PC Board.

## 2-8-1 Spectrum Analyzer IF Module Detailed Theory

The Spectrum Analyzer IF Module converts the 10.7 MHz IF input signal to 2.5 MHz and outputs a detected linear video signal for the logarithmic RF level of the CRT (See Figure 2-26 and the Spectrum Analyzer IF Schematic in Section 7 of this Manual).

Y3901, Q3901 and associated components form a 13.2 MHz crystal oscillator. The oscillator frequency and the 10.7 MHz signal input at J5401 are mixed in MXR3901 to form a 2.5 MHz difference frequency. The 2.5 MHz signal divides for one of two selected filters. When the +12 V filter control line (pin 5 of J5402) is high, the 650 kHz bandwidth filter is selected. When the filter control line is low, an eight-pole filter of 30 kHz bandwidth is selected. The gain of the 650 kHz filter is set at R3919. The gain of the 30 kHz filter is set at R3938.

The filtered 2.5 MHz signal is amplified by U3901 and discrete amplifiers Q3909, Q3910, Q3912 and Q3913. The logarithmic signal is converted to a linear signal, which is detected by CR3909 and then amplified by U3902B for output to the Oscilloscope Control and Deflection PC Board. If pin 10 of U3903A goes high (when the 1 dB position is selected on the front panel dB/DIV Switch), U3902A is switched through U3903A. The VERT POS Control on the front panel will then control the gain of U3902A by its input at pin 8 of J5402.

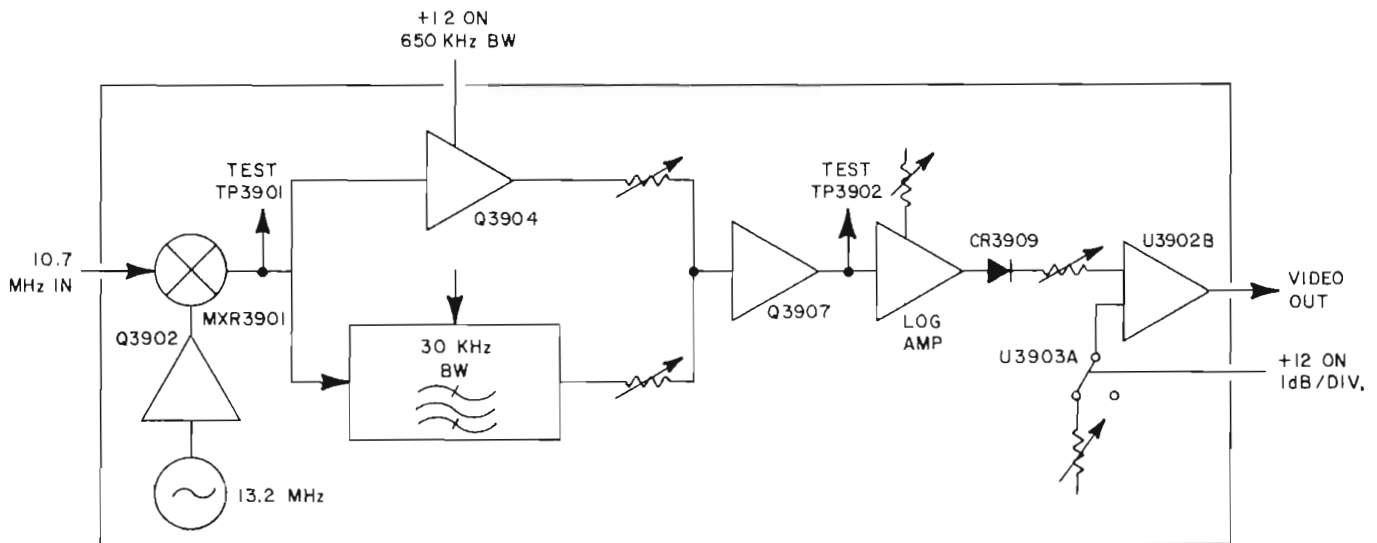


Figure 2-26 Spectrum Analyzer IF Detailed Block Diagram

## 2-8-2 Spectrum Analyzer LO Module Detailed Theory

### **NOTE**

FM/AM-1500 serial numbers 1005 through 1351 use PC Board 7010-5033-500 (Revision B) and Schematic 7010-5013-500 (Revision B). FM/AM-1500 serial numbers 1352 and ON use PC Board 7010-5033-500 (Revision F) and Schematic 7010-5013-500 (Revision F). Many of the part numbers referred to in theory will be the same in both the B and the F versions. For those part numbers that are different, the first number given is the F version and the second part number (in parentheses) is the B version.

The Spectrum Analyzer LO Module supplies the Spectrum Analyzer RF Module with its tracking frequency while being phase-locked with the Low Loop Mixer Module frequency (See Figure 2-27 and the Spectrum Analyzer LO Schematic in Section 7 of this Manual). The 78.3001 to 79.3 MHz signal from the Low Loop Mixer Module is input at J4602 and splits into two parts. One part is output at J4601 to the 89-90 MHz Receiver Module. The other part is amplified by Q3503 to drive U3501 as a divide-by 10. The divided 7.83 to 7.93 MHz is used as the reference frequency for the high speed phase-lock comparator, U3509.

Transistor Q3501 and associated components operate as a 73.3 to 84.3 MHz voltage controlled oscillator (VCO). Q3502 buffers the VCO signal, which then splits in three directions. Q3505 amplifies the signal for output at J4605 to the Spectrum Analyzer RF Module. Q3504 amplifies the signal for output at J4604 to the FM Generator Module. Q3506 and Q3507 amplify the signal to drive U3506 as a divide-by 10. The divided VCO signal is compared at U3509A to phase-lock the VCO signal with the Low Loop Mixer reference frequency.

The divided VCO signal is further divided by 16 at U3507 and then divided by 512 at U3503 and U3504. The approximate 1 mS output pulse is used to gate the phase-lock signal at U3513B while the VCO frequency is sweeping. The phase-lock signal is integrated at U3508B (U3508A), and then sent to the VCO circuit and to the tracking filter on the Spectrum Analyzer RF Module.

A 100 Hz reference signal, input at pin 9 of J4603, is amplified by Q3510 to drive U3505 as a divide-by 10. The resulting 10 Hz is the analyzer sweep rate. The positive pulse through C3555 and CR3509 will cause pin 1 of U3514A (pin 7 of U3514B) to go high. Q3511 will then go high, unblanking the analyzer trace. Q3513 will conduct and begin charging C3556 and C3557 negative for the sweep ramp. When the ramp has reached -4.9 V, pin 7 of U3514B (pin 1 of U3514A) goes low to reset the sweep ramp.

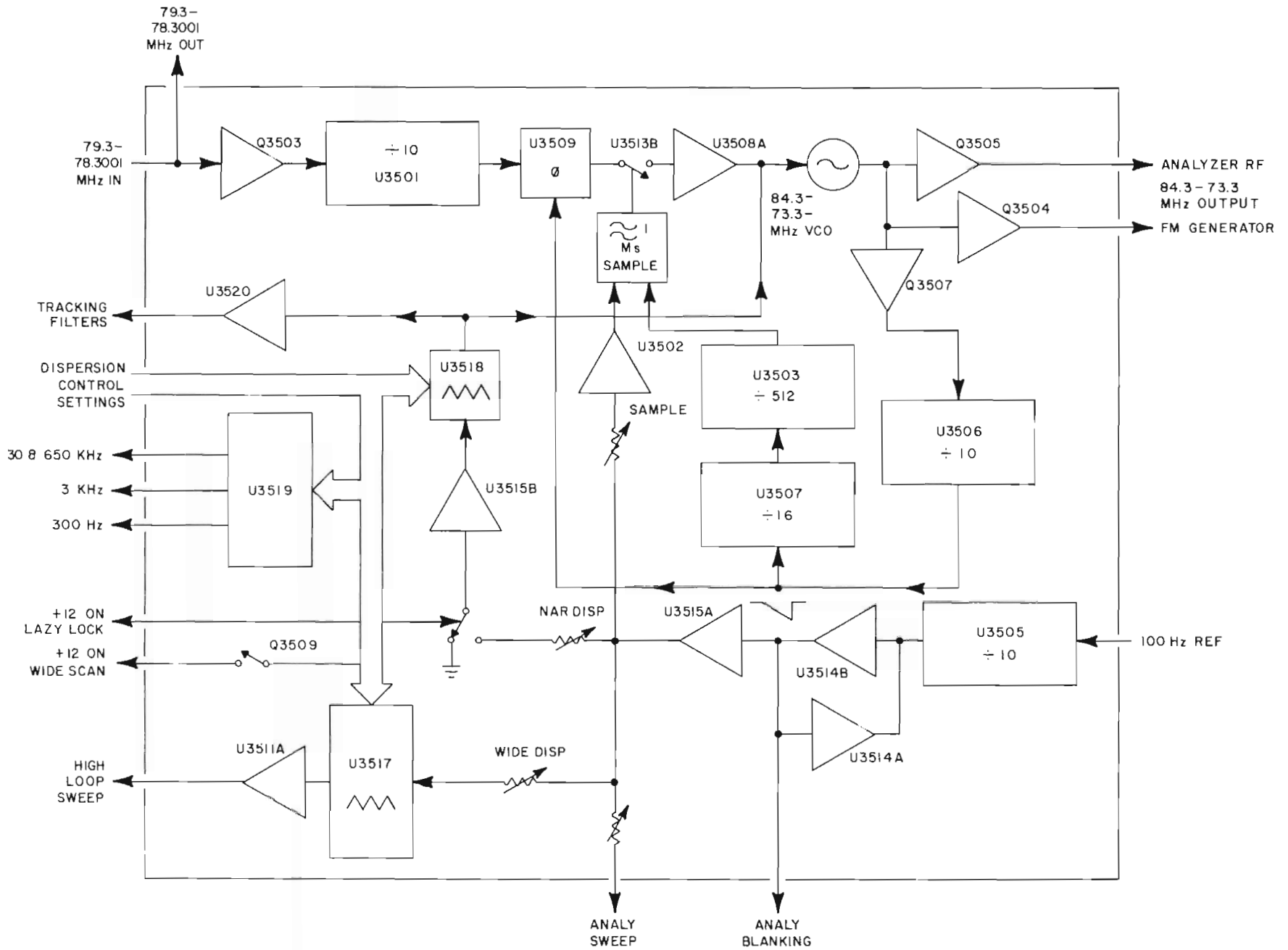


Figure 2-27 Spectrum Analyzer LO Detailed Block Diagram

The logic lines for the Spectrum Analyzer L.O. are controlled by the setting of the front panel ANALY DISPR Control as shown in Table 2-4. When pin 11 of U3510C is low, the dispersion gain of U3515A is increased for the 1 K and 2 K settings of the ANALY DISPR Control. At all other settings, the gain will be normal.

| J4603, pin # | BCD Digit | ANALY DISPR Settings              |
|--------------|-----------|-----------------------------------|
| 16           | 1         | 2 K, 20 K, .2 M, 1 M, 5 M, Full   |
| 17           | 2         | 10 K, 20 K, .5 M, 1 M, 10 M, Full |
| 1            | 4         | 100 K, .2 M, .5 M, 1 M            |
| 21           | 8         | 2 M, 5 M, 10 M, Full              |

Table 2-4 Logic Lines for Spectrum Analyzer L.O.

When pin 6 of U3516B goes low, U3517 will select one of the wide dispersion ranges. The wide dispersion range selected (2 M thru Full) is buffered at U3511A and output to the High Loop Module. The base of Q3516 will be pulled low through R3591, and +12 V will be output on the 650 kHz and 30 kHz bandwidth select line. The base of Q3509 also will be pulled low, causing a +12 V on wide scan signal to be output to the High Loop Module, which will select control for the tune ranges.

When pin 10 of U3510A goes low, the narrow dispersion ranges (1 K thru 1 M) will be selected by U3518, and the selected range will be sent to the tracking filters in the Spectrum Analyzer RF Module. When pins 2, 3 or 21 of U3519 go high, a narrow dispersion range will be selected to activate one of the bandwidth control lines. The 1 K and 2 K settings of the ANALY DISPR Control will select the 300 Hz bandwidth line. The 10 K and 20 K settings will select the 3 kHz bandwidth control line. The 100 K thru Full setting will select the 650 kHz and 30 kHz bandwidth control line.

When pin 10 of U3516A (pin 9 of U3516C) goes high, +12 V will be output to control the lazy lock circuit in the High Loop Module. This will occur at every ANALY DISPR setting except Full.

### 2-8-3 Spectrum Analyzer RF Module Detailed Theory

The Spectrum Analyzer RF Module receives the 89-90 MHz IF signal from the 1300 MHz IF Receiver Module at J5203 (See Figure 2-28 and the Spectrum Analyzer RF Schematic in Section 7 of this Manual). The signal is output at J5201 to the 89-90 MHz Receiver Module. The signal is also band-pass filtered in a 6-pole filter that will track from 84 to 95 MHz with the sweep signal, input at pin 5 of J5204, from the Spectrum Analyzer LO Module.

The filtered 84 to 95 MHz is mixed in MXR3701 with the input, at J5203, of 73.3 to 84.3 MHz (nominally 79.3 MHz). The resulting difference frequency of 10.7 MHz is band-pass filtered to 650 kHz in a six section filter. When +12 V is applied to pin 1 of J5204, to select 650 kHz or 30 kHz bandwidths, the 10.7 MHz IF will pass through Q3713 and be output at J5205 to the Spectrum Analyzer IF Module. Gain for the 650 kHz and 30 kHz bandwidths is set at R3777.

When +12 V is applied to pin 3 of J5204 to select the 3 kHz bandwidth, the 10.7 MHz IF will pass through three crystal filter stages and be output at J5205. Gain for the 3 kHz bandwidth is set at R3749. When +12 V is applied to pin 2 of J5204 to select the 300 Hz bandwidth, the 10.7 MHz IF will pass through four crystal filter stages and be output at J5205. Gain for the 300 Hz bandwidth is set at R3771.

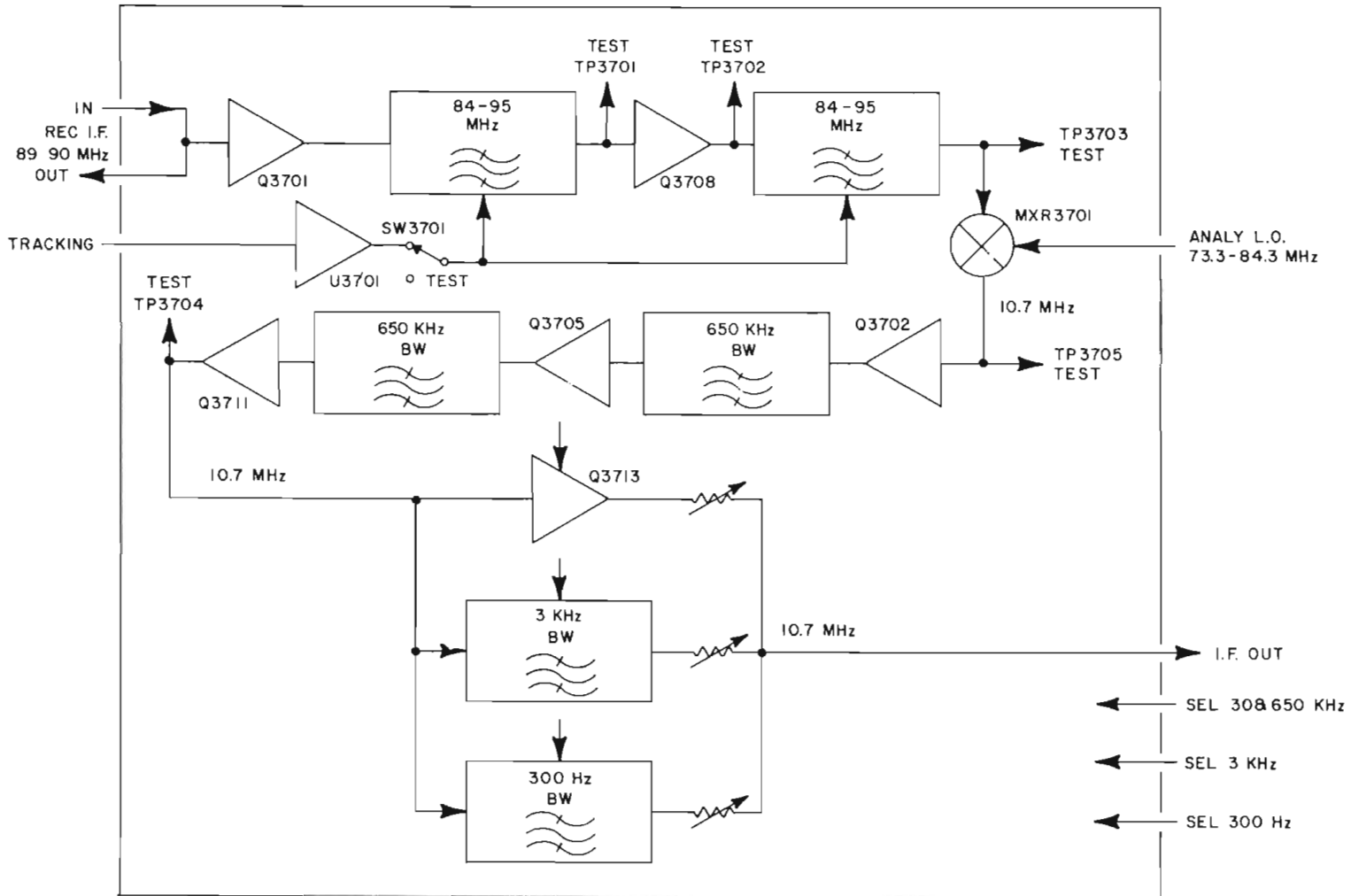


Figure 2-28 Spectrum Analyzer RF Module Detailed Block Diagram



## 2-9 MICROPROCESSOR FUNCTIONAL THEORY

The Microprocessor Functional Block contains the CPU/Memory PC Board and the I/O Interface PC Board (See Figure 2-29 ). If installed, the optional GPIB interface is also a part of this Functional Block. Refer to the GPIB supplement for information on the GPIB.

The CPU/Memory PC Board serves as the software controller for the FM/AM-1500 and generates the video for the menus. It communicates with the I/O Interface PC Board in a bi-directional mode and with the Dual Tone Generator in a write only mode.

The I/O Interface PC Board serves as the intermediary between the CPU bus and the hardware of the FM/AM-1500 as shown in Figure 2-29.

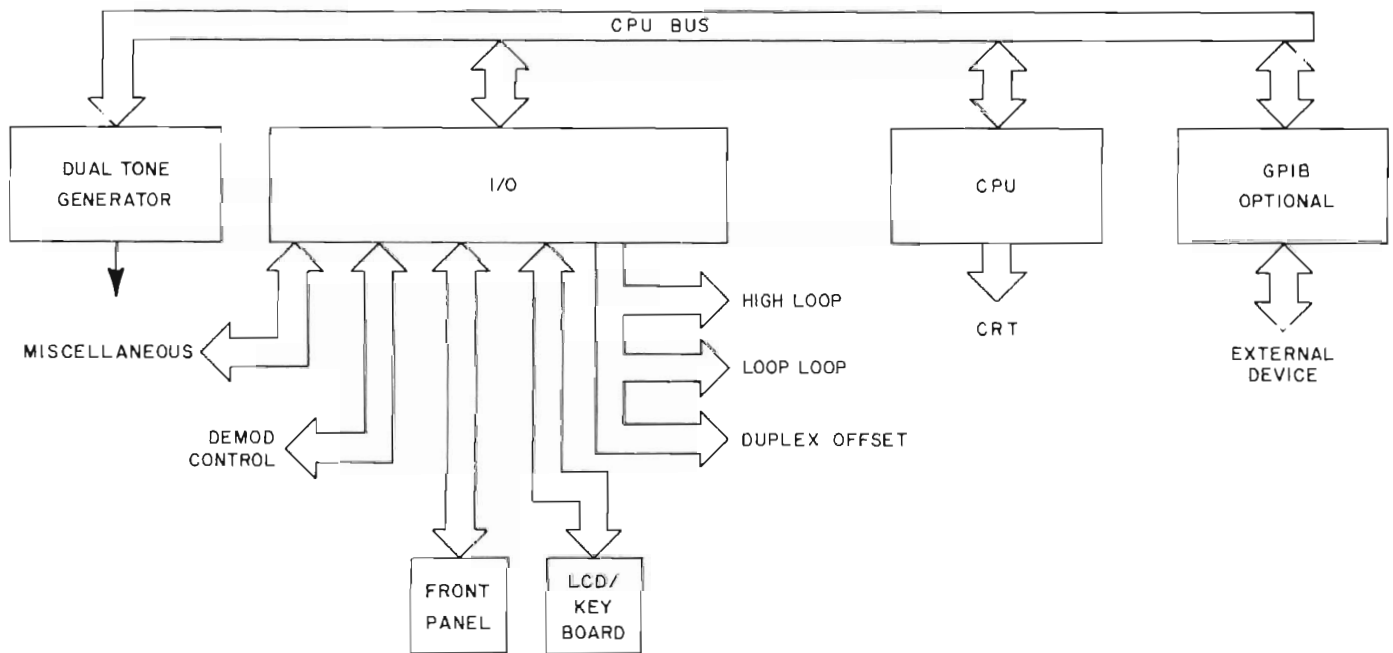


Figure 2-29 Microprocessor Functional Block Diagram

## 2-9-1 CPU/MEMORY PC Board Detailed Theory

### CPU

The CPU used in the FM/AM-1500 is a Zilog Z-80 CPU, which is a fast 8-bit processor capable of addressing 65536 memory locations and 256 I/O devices (See Figure 2-30 and the CPU/MEMORY Schematic in Section 7 of this Manual). U9705 is the Z-80 CPU. The three buses used for communication are an 8-bit data bus, a 16-bit address bus and a 12-bit control bus. U4102 thru U4105 are the bus buffers for the CPU. U4108C and U4108D control the direction of the data bus. A 2 MHz system clock is input at pin 32 of P4101. U4106A inverts the clock, which is then referred to as  $\Phi''$ . U4127 divides  $\Phi''$  down to a 20 kHz clock for the Timing and Interrupt circuit.  $\Phi''$  is also sent over the control bus, where Q4103 and U4107F buffer/pull-up the clock to form  $\Phi'$  and  $\Phi$ . A 3.58 MHz crystal is used to clock the Z-80 and the CTCs.  $\Phi'$  is used to clock all other CPU peripherals.

### EPROM

U9704 is the processor's Programmed Memory Chip. Each chip position is jumper selectable either as EPROM or RAM. Normally, U9704 is jumper selected to EPROM configuration.

### Non-Volatile RAM

U4117 and U4118 are the non-volatile RAMs which hold user-entered data in memory after the FM/AM-1500 is turned off, so that it is available upon power-up. The lithium battery, BT4101, provides +3 V, which is sufficient to hold the contents of the RAMs valid, even though +3 V is not sufficient for reading and writing.

### +5 V Sense & Non-Volatile RAM Write Circuit

Q4106 and Q4107 form a differential amplifier to detect a power-off condition by monitoring the +5 V line. When the output of Q4106 goes below approximate +4.5 V, Q4105 turns off and Q4101 turns off. This disables U4119 and prevents any data in the non-volatile RAMs from being inadvertently changed. When the +5 V line drops below approximately +3 V, CR4103 becomes reverse biased and CR4102 becomes forward biased. When CR4102 is forward biased, the non-volatile RAMs are being powered by BT4101. This is the standby or power-off mode.

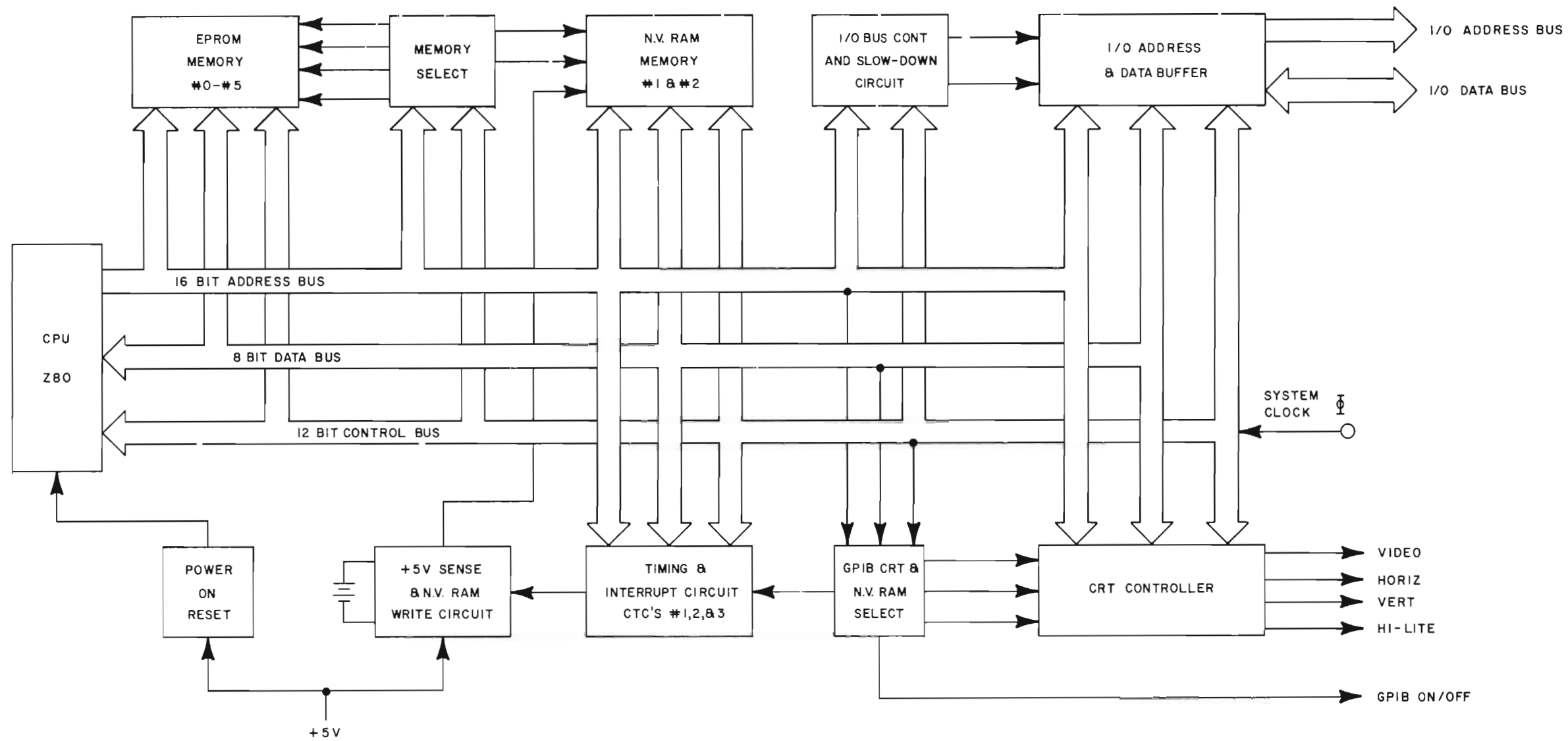


Figure 2-30 CPU/MEMORY PC BOARD  
Detailed Block Diagram

## Memory Select

U4112 is the memory select IC. When  $\overline{MREQ}$  is active and  $\overline{RFSH}$  is inactive, U4112 will select one of the RAM chips according to the binary code of address lines A13-A15. The memory REFRESH function of the Z-80 is not used in this configuration.

## Timing and Interrupt Circuit

The timing and interrupt circuit consists of CTCs U4122, U4126 and U4137, along with U4120. CTC U4122 divides the 20 kHz signal derived from  $\phi$ " by a factor of 20 and outputs it as a 1 kHz (1 mS) line to CTCs U4126 and U4137. U4122 also controls the INT and BRDY lines to the CRT Controller Circuit. U4126 processes the GPIB, keyboard and DCS interrupts. These interrupt signals are also applied to the interrupt latch, U4120. U4120 is provided to allow the CPU to read the status of the interrupt lines from the data bus. U4123 is the address select chip for U4122, U4126 and U4120. U4137 acts as the Demod counter and is enabled by U4135.

## GPIB, CRT & Non-Volatile RAM Select Circuit

U4135, U4136 and U4140 form this select circuit. U4135 enables CTC U4137. U4136 enables U4140 and the CRT Controller. U4140 disables the CRT Controller, enables the non-volatile RAM write (thru Q4104), and controls GPIB ON/OFF.

## Watchdog Timer Circuit

The Watchdog Timer Circuit includes a Programmable Array Logic (PAL) device (U9701) and a Voltage Supervisor Chip (U9702). U9702 provides a signal to reset the Z80 CPU (U9705) and the Counter (U9703) during power-up operation or, during normal operation, if the +5 VDC source drops below nominal.

The PAL (U9701) initiates a reset if it detects an illegal write to non-volatile RAM or if the Counter (U9703) is allowed to time out. U9701 also provides chip selection for System ROM (U9704).

## I/O Bus Control & Slow-Down Circuit

U4125 and U4124 are the bus control chips. U4125 turns off U4123 when the I/O bus is selected, and thus turns off the CTC's. U4125 also selects U4124, the data enable flip-flop, which outputs clock  $\Phi'$  to the data buffer. At the same time, U4125 also triggers a slow-down circuit. The slow-down circuit is necessary because devices on the buffered buses require longer set-up times than devices tied directly to the Z-80 bus. U4121, U4107A, U4107D, U4106F, U4108A and U4108B form the slow-down circuit, which has a 3  $\mu$ S time-out period. After the slow-down circuit times out, the Z-80 finishes its current machine cycle and disables U4125. On the first rising edge of the clock signal after U4125 is disabled, U4124 is set, disabling the I/O data bus. The I/O address bus is disabled when U4125 is disabled.

## I/O Address & Data Buffer

U4130 and U4131 provide buffering for the I/O data and address buses, respectively. Notice that only five address lines are used, giving a possibility of 64 I/O devices, plus read and write.

## CRT Controller Circuit

The CRT Controller circuit consists of U4141, U4142, U4139, U4143, U4134, U4132, U4133 and U4138. U4141 is a CRT Controller chip. It supplies a character address to the character EPROM, U4142. U4142 contains the dot pattern for each of the characters. U4141 also supplies a latch, U4139, with special function data (such as reverse video, hi-lite, sync, etc.) for each character. The output of the character EPROM is applied to a shift register, U4143, which shifts out each dot at a 2 MHz rate. U4134B, C and D, U4133 B and C and U4132C process the shifted video. The output of U4132C is the final video output of the CPU/MEMORY board. U4138, U4132 A and D, U4133A and U4134A generate the timing signals for the video generator. U4132A and D buffer the 2 MHz clock signal, and apply it to the shift register, U4143. U4138 is a divide-by 8 counter which supplies the character clock to the CRT Controller, U4141. Two interrupt outputs are provided from the CRT Controller to the Timing and Interrupt circuit. These outputs are BRDY (Buffer ReaDY) and INT (INTerrupt). The BRDY signal indicates that the CRT buffer is empty and may be filled with another character. The INT signal is used to generate an interrupt at the end of each frame.

## 2-9-2 I/O Interface PC Board Detailed Theory

### General

The I/O Interface PC Board links the computer with hardware devices such as the High Loop Module, the Low Loop Module, Duplex Offset Module and the Front Panel (See Figure 2-31 and the I/O Interface Schematic in Section 7 of this Manual). In addition, the I/O Interface PC Board also performs analog to digital conversions for deviation and power information, and digital to analog conversions for the sweep (X-OUT) output.

### Bus Buffer

The bus buffer consists of U4301 and U4302. U4302 is the address buffer. This chip buffers address lines A0/A5 and the read and write signals. U4302 is a single direction buffer and is a single direction buffer and is enabled continuously.

U4301 is the data bus buffer, which buffers data lines D0-D7. U4301 is a bi-directional buffer which is continuously enabled. The direction of buffering is controlled by the address decoder.

### Address Decoder

The address decoder consists of U4305, U4306, U4307, U4308, U4323, U4324, U4334A and U4334B. U4306 decodes 8 byte blocks of addresses in the range of 00(H) thru 1F(H) and 28(H) thru 2F(H), in the write mode. U4305 decodes each of the 8 individual addresses in the range of 18(H) thru 1F(H) in the write mode. U4323 decodes addresses 29(H), 28(H), 2A(H) and 2C(H).

U4307 decodes two 8 byte blocks, 00(H) thru 07(H) and 28(H) thru 2F(H) in the read mode. Diodes CR4301 and CR4302 along with R4301 form an OR gate, the output of which is used to control the direction of U4301, the data bus buffer. U4308 decodes each of the individual addresses between 28(H) thru 2F(H) in the read mode. U4324, along with U4334A and U4334B decodes addresses 00(H), 01(H), 02(H) and 03(H). U4334A and U4334B combine the decoded 02(H) and 03(H) outputs before applying them to U4329.

### Talk-Back Circuit

The talk-back circuit is provided to check continuity of the data bus. During a write operation, information present on the address bus is latched into U4312. At the same time, information present on the data bus is latched into U4311. After a write operation, U4311 and U4312 can be read by the microprocessor and compared with the information sent during the write cycle. If the information which was read agrees with the information which was sent, the bus circuits are operating properly.

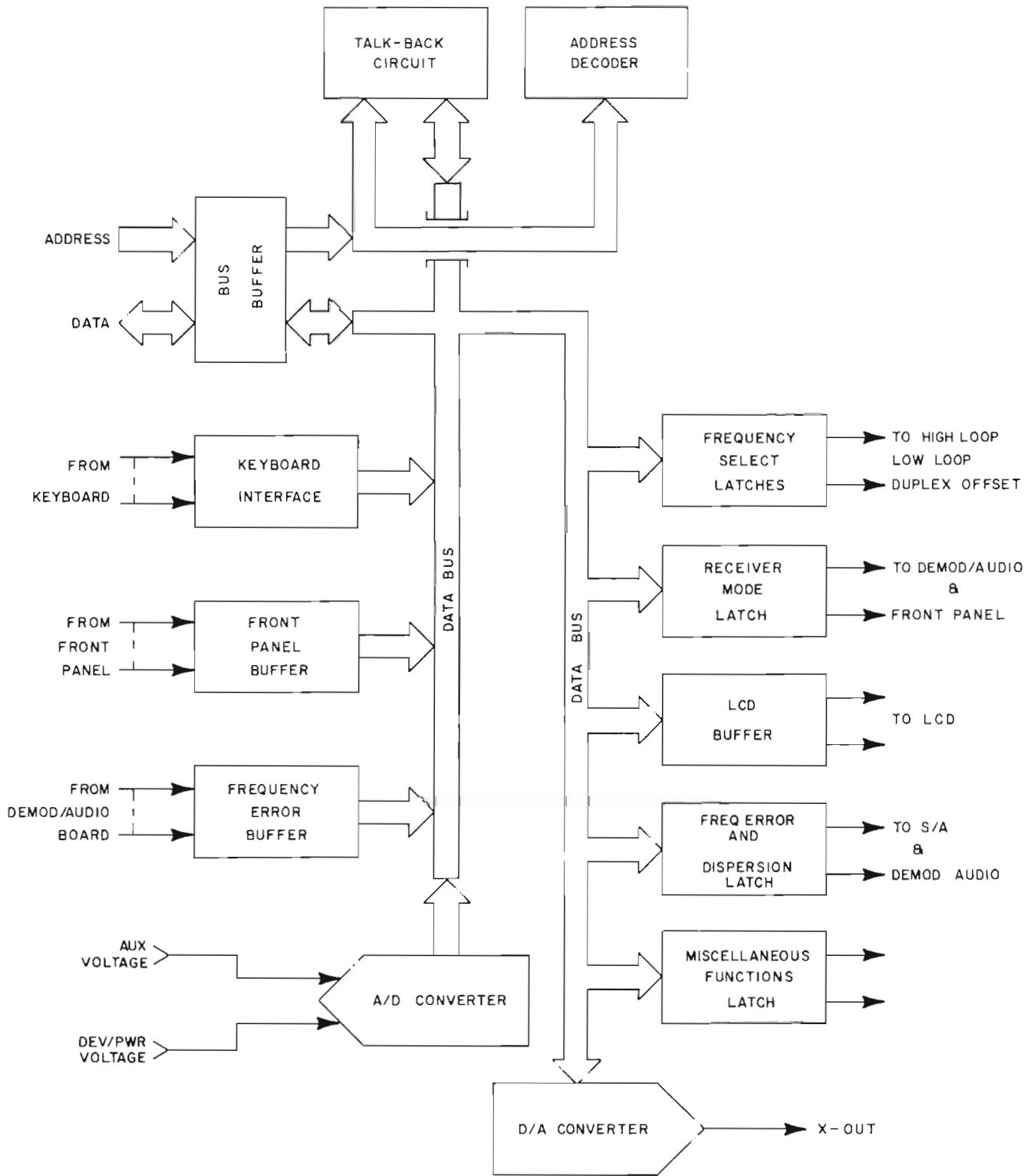


Figure 2-31 I/O Interface PC Board Detailed Block Diagram

### Frequency Select Latches

The frequency select latches capture frequency data from the data bus when directed to do so by the address decoder. The captured data is stored and applied to the High Loop Module, Low Loop Module and Duplex Offset Module. U4303 and U4304 supply frequency information to the High Loop Module. U4309 and U4310 supply frequency information to the Low Loop Module. U4320 and U4321 supply frequency information to the Duplex Offset Module. U4303 also controls the low pass filters in the Delay Line Module and controls the 100 MHz and 200 MHz lines to the Duplex Offset Module.

### Receiver Mode Latch

The receiver mode latch captures demodulation and bandwidth settings from the data bus when directed to do so by the address decoder. U4331 latches the data and presents this information to U4332, which is an open collector buffer. The output of U4332 is 0 volts for a logic low and +12 V for a logic high. Transistors Q4308 thru Q4314 invert and buffer the output of U4332. The current out of Q4308 thru Q4314 is sufficient for driving the front panel LFD's and the Demod Audio PC Board.

### LCD Buffer

The LCD buffer consists of U4314 and U4315. U4314 and U4315 are tri-state buffers. These buffers are continuously enabled and supply the LCD's with D0-D5 of the data bus, along with A0, A1 and A2 of the address bus and three lines from the address decoder which select one of three 8 byte blocks of I/O write locations.

These locations are 00(H) thru 07(H), 08(H) thru 0F(H) and 10(H) thru 17(H). The LCD outputs are applied to the LCD displays on the front panel.

### Freq Error and Dispersion Latch

The freq error and dispersion latch consists of U4339, U4340 and Q4315. U4339 captures freq error and dispersion settings from the data bus when directed to do so by the address decoder. The output of U4339 is applied to U4340 which is an open collector buffer. Its output swings between 0 V (for logic 0) and +12 V (for logic 1). U4340 has seven open collector buffers. The eighth line (pin 5) out of U4340 is applied to R4367 and Q4315, which forms an open collector buffer. The output of U4340 and Q4315 is applied to the Demod Audio PC Board and to the Spectrum Analyzer LO Module

### Miscellaneous Functions Latch

The miscellaneous functions latch consists of U4325, U4326, Q4306 and Q4307. U4325 captures the applicable data from the data bus when directed to do so by the address decoder. U4326 is an open collector buffer. The output of U4326 swings between 0 V (logic 0) and +12 V



(logic 1). The outputs of U4326 are applied to the following modules:

| LINE            | DESTINATION          |
|-----------------|----------------------|
| GEN/ <u>REC</u> | Demod Audio PC Board |
| SIM/DUP         | Demod Audio PC Board |
| DEV POWER A     | Demod Audio PC Board |
| DEV POWER B     | Demod Audio PC Board |
| DEV POWER C     | Demod Audio PC Board |
| PEAK/PEAK AVG.  | Demod Audio PC Board |
| 1 dB/10 dB      | Spectrum Analyzer IF |

Pin 5 of U4325 is applied to Q4307, which operates as an inverter. When the output of this inverter is low (i.e., track selected), Q4306 will be turned on to supply +12 V to the Demod Audio PC Board, the FM Generator Module and the Generate Mixer Module.

### Keyboard Interface

The keyboard interface consists of U4313, U4316, U4317A and Q4301 thru Q4305. When no keys are depressed, the COL1 thru COL6 inputs to U4316 are open. With these lines open, they will be pulled up to +5 V by RN4301 and then applied to U4316. With no keys depressed, the ROW1 thru ROW4 inputs are also open. This causes Q4301 thru Q4304 to be turned off. Under these conditions, the outputs of Q4301 thru Q4304, which are applied to U4313 and U4317A, will be high. With all four inputs to U4317A high, its output will be low, causing Q4305 to be turned off. With Q4305 turned off, its output will be high (inactive). The above discussion describes the keyboard in its static state.

When a key is depressed, one of the "COL" (column) inputs is shorted to one of the "ROW" inputs. Which column input is applied to which row input is determined by which key is depressed (see keyboard schematic). When one of the column inputs are shorted to a row input, the applicable pull-up resistor in RN4301 will bias the applicable row transistor. When this happens, the column input is pulled down to approximately +0.65 V by the base-emitter drop, causing the applicable row transistor to be turned on and its output to go low. Therefore, when one of the keys are depressed, one column input to U4316 goes low and one row input to U4313 goes low. Also, when one of the outputs of the row transistors goes low, the output of U4317A goes high, causing Q4305 to turn on. When Q4305 turns on, its output goes low (active). This interrupts the computer, informing it that a key is pressed. When the interrupt occurs, the computer places the address of U4313 and U4316 on the address bus (these addresses are 28(H) and 29(H) respectively). The address decoder then gates the inputs of U4313 and U4316 onto the data bus to be read by the computer. Note that U4313 also gates information from the DISPLAY Control.

### Front Panel Buffer

The front panel buffer consists of U4318, U4319 and U4327. Control settings from the front panel are presented to the inputs of these

buffers. The buffer gates these settings onto the data bus when directed to do so by the address decoder. It should be noted that U4322 also gates phase-lock and Overtemp flags from the Demod Audio PC Board.

Frequency Error Buffer

Frequency error information from the Demod Audio PC Board is presented to U4338, which gates this information onto the data bus when directed to do so by the address decoder.

Digital to Analog Converter

The digital to analog converter, U4330, is an 8 bit D/A converter with internal latches. Digital settings are latched into the D/A converter when directed to do so by the address decoder. The analog output is applied to the X-OUT connector on the rear panel of the FM/AM-1500. Two adjustments are provided to calibrate this D/A circuit. R4331 adjusts full scale voltage, while R4333 adjusts the offset.

Analog to Digital Converter

The analog to digital converter consists of U4337, U4335, U4336, U4333, U4327 and U4328. U4333 is the control latch for the A/D converter. 4 bits of this latch are used to control the CRT power, antenna attenuator and the key-depressed "BEEP". U4333 captures information off the data bus when directed to do so by the address decoder. Two lines out of U4333 are jumper programmable and may be connected to the RUN/HOLD and/or TEST inputs of U4337. Two other lines from U4333 are connected to U4336 to select the analog input to be measured. U4336 is a 4 input multiplexer which may select one of the following inputs:

| INPUT             | REMARKS                   |
|-------------------|---------------------------|
| DEV/POWER         | From Demod Audio PC Board |
| AUX               | Not Currently Used        |
| Reference Voltage | Self Test Purposes        |
| GROUND            | Self Test Purposes        |

The output of U4336 is applied to U4335, which is a sample and hold amplifier. The SAMPLE/HOLD input (pin 8) is controlled by the status output of U4337 via U4334D. The sample and hold amplifier prevents the voltage under test from changing while U4337 is going through a conversion cycle. R4350 is provided as an adjustment for the sample and hold amplifier. The output of the sample and hold amplifier is applied to U4337 for conversion via a low pass filter consisting of R4352 and C4354. U4337 is a 12 bit analog to digital converter. The A/D converter has one adjustment, R4354, provided for the reference voltage. The outputs of U4337, which is a digital representation of the voltage under test, are applied to U4327 and U4328. U4327 and U4328 gate the A/D outputs onto the data bus, when directed to do so by the address decoder.

# SECTION 3 - PERFORMANCE EVALUATION

## 3-1 GENERAL

This section contains step-by-step test procedures for assessing the performance of the FM/AM-1500. These procedures should be performed as the first step in the troubleshooting/maintenance process, when the operating condition of the set is in question. All procedures in this section are performed using the FM/AM-1500 front and rear panels and do not require removal of the exterior case.

The following performance tests are included in this manual:

| <u>Test Number</u> | <u>Title</u>                            | <u>Page</u> |
|--------------------|---|-------------|
| 3-2                | Power Supply Functional Block           | 3-5         |
| 3-2-1              | Power Supply Voltage Performance Test   | 3-5         |
| 3-3                | Frequency Standard Functional Block     | 3-7         |
| 3-3-1              | Frequency Standard Performance Test     | 3-7         |
| 3-4                | Frequency Synthesis Functional Block    | 3-9         |
| 3-4-1              | High Loop and Low Loop Performance Test | 3-9         |
| 3-5                | Receiver Functional Block               | 3-11        |
| 3-5-1              | Receiver Signal Performance Test        | 3-11        |
| 3-5-2              | Frequency Error Performance Test        | 3-17        |
| 3-5-3              | Modulation Meter Performance Test       | 3-19        |
| 3-5-4              | Oscilloscope Performance Test           | 3-21        |
| 3-5-5              | Power Meter Performance Test            | 3-23        |
| 3-6                | Generate Functional Block               | 3-25        |
| 3-6-1              | RF Output Performance Test              | 3-25        |
| 3-6-2              | Duplex Offset Performance Test          | 3-31        |
| 3-6-3              | Dual Tone Generator Performance Test    | 3-33        |
| 3-7                | Spectrum Analyzer Functional Block      | 3-37        |
| 3-7-1              | Spectrum Analyzer Performance Test      | 3-37        |
| 3-8                | Microprocessor Control Functional Block | 3-41        |
| 3-8-1              | Front Panel Performance Test            | 3-41        |
| 3-8-2              | Data Entry Performance Test             | 3-45        |

Each test procedure contains several common headings which are defined as follows:

3-2-1 Test procedure number followed by name of test procedure.

SPECIAL ACCESSORY EQUIPMENT REQ'D: List of any special accessory test equipment required to complete the test procedure.

TEST SET-UP DIAGRAM: A diagrammatic aid for making proper connections between the FM/AM-1500 and any special accessory equipment.

## INITIAL FM/AM-1500

CONTROL SETTINGS: Initial FM/AM-1500 front panel control settings required to begin the test procedure. (Refer to Figure 3-1 for front panel control identification).

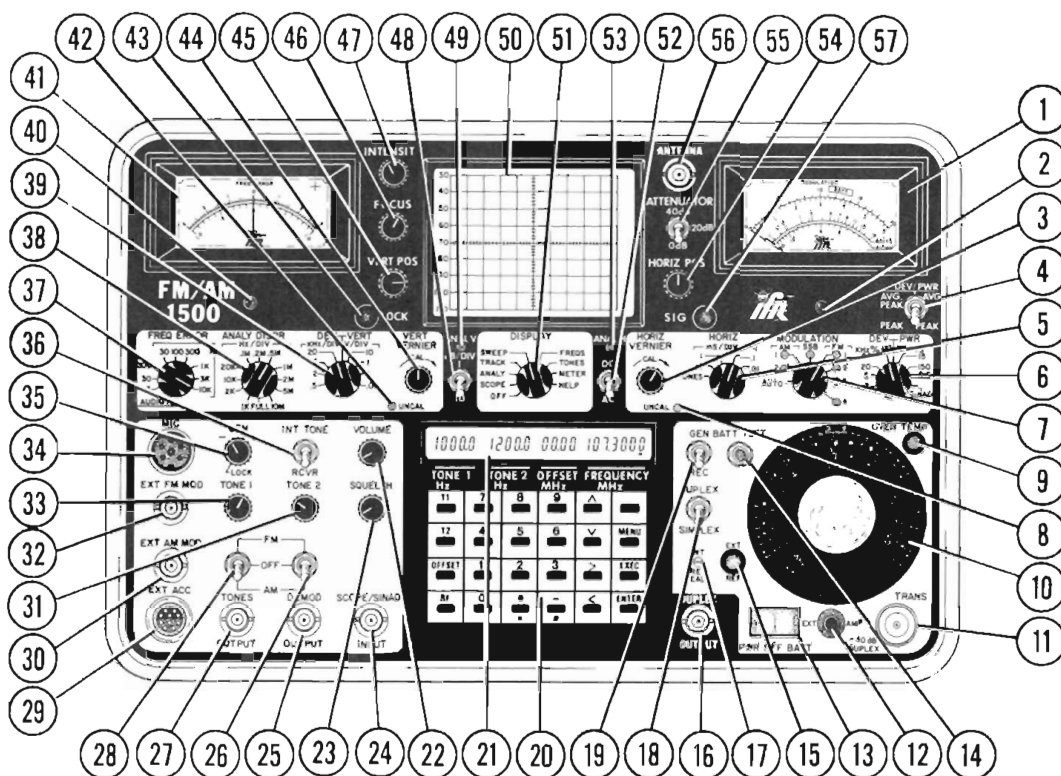
### 3-1-1 TEST EQUIPMENT REQUIREMENTS

Appendix E at the rear of this manual contains a comprehensive list of test equipment suitable for performing any of the procedures in this manual. Any other equipment meeting the specifications listed in Appendix E may be substituted in place of the recommended models.

### 3-1-2 CORRECTIVE MAINTENANCE PROCEDURES

The performance tests in this section will aid the operator/technician in determining whether the FM/AM-1500 is functioning properly or if a failure condition exists. A failure condition will normally be reflected as either a calibration error or a malfunction. A calibration error is defined as a measurement or reading (relating to the unit being tested) that is not within prescribed tolerances. In this condition, the set may outwardly appear to be functioning properly, despite the presence of a calibration error. A malfunction denotes a defective condition where a signal may be totally absent, grossly out of tolerance or where the unit itself (or any part thereof) is obviously not working properly.

In the event a failure condition is confirmed, the technician should take appropriate corrective maintenance action to return the set to its normal operating condition. The "CORRECTIVE MAINTENANCE FLOWCHART" shown in the Preface to this manual is intended to serve as a guide in directing the technician through the troubleshooting/maintenance process. By observing this general sequence, the technician will be able to use the troubleshooting/maintenance recommendations contained within this and other sections of this manual to return the FM/AM-1500 to normal operation.



- |  |                                 |
|--|---------------------------------|
| 1. MODULATION Meter                            | 29. EXT ACC Connector           |
| 2. MODULATION Meter Mechanical Zero Adjustment | 30. EXT AM MOD Connector        |
| 3. HORIZ VERNIER Control                       | 31. TONE 2 Control              |
| 4. AVG PEAK/PEAK Switch                        | 32. EXT FM MOD Connector        |
| 5. HORIZ Control                               | 33. TONE 1 Control              |
| 6. DEV/PWR Control                             | 34. MIC Connector               |
| 7. MODULATION Control                          | 35. GEN/LOCK Control            |
| 8. UNCAL Indicator (Horizontal)                | 36. INT TONE/RCVR Switch        |
| 9. OVERTEMP Indicator                          | 37. FREQ ERROR Control          |
| 10. RF Output Level Control                    | 38. ANALY DISPR Control         |
| 11. TRANS/-40 dB DUPLEX Connector              | 39. DEV/VERT Control            |
| 12. EXT AMP Connector                          | 40. FREQ ERROR Mechanical Zero  |
| 13. PWR/OFF/BATT Switch                        | 41. FREQ ERROR Meter            |
| 14. BATT TEST Button                           | 42. UNCAL Indicator (Vertical)  |
| 15. EXT REF Indicator                          | 43. Freq LOCK Indicator         |
| 16. DUPLEX OUTPUT Connector                    | 44. VERT VERNIER Control        |
| 17. INT REF CAL Adjustment                     | 45. VERT POS Control            |
| 18. DUPLEX/SIMPLEX Switch                      | 46. FOCUS Control               |
| 19. GEN/REC Switch                             | 47. INTENSITY Control           |
| 20. KEYBOARD                                   | 48. dB/DIV Switch               |
| 21. LCD  | 49. ANAL V Adjustment           |
| 22. VOLUME Control                             | 50. CRT                         |
| 23. SQUELCH Control                            | 51. DISPLAY Control             |
| 24. SCOPE/SINAD INPUT Connector                | 52. DC/AC Switch                |
| 25. DEMOD OUTPUT Connector                     | 53. ANAL H Adjustment           |
| 26. Tone 2 FM/OFF/AM Switch                    | 54. HORIZ POS Control           |
| 27. TONES OUTPUT Connector                     | 55. ATTENUATOR Switch (Antenna) |
| 28. Tone 1 FM/OFF/AM Switch                    | 56. ANTENNA Connector           |
|  | 57. SIG Indicator               |

Figure 3-1 FM/AM-1500 Front Panel

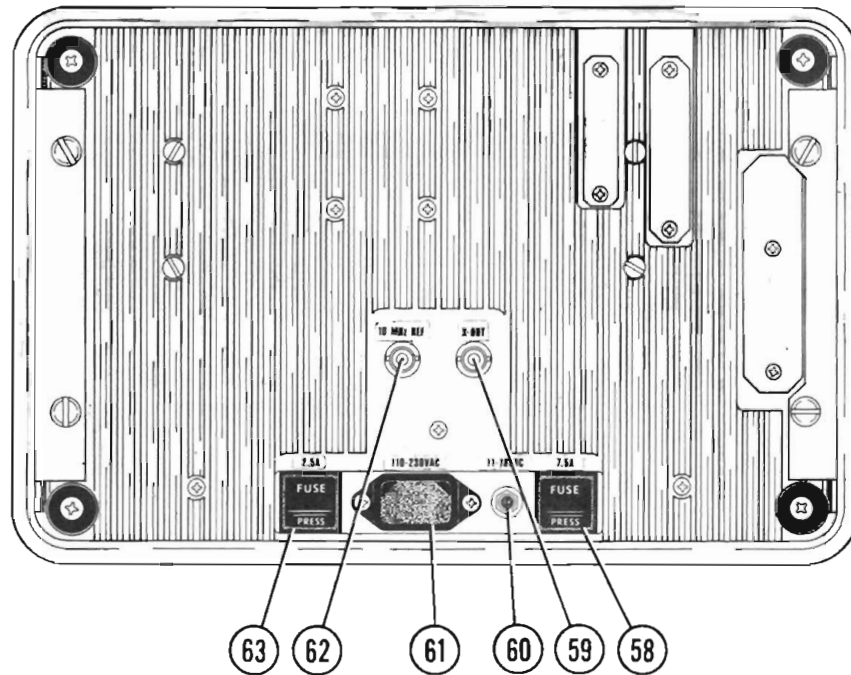


Figure 3-2 FM/AM-1500 Rear Panel

- 58. DC Fuse (7.5 Amp)
- 59. X-Out Connector  
Provides an output signal proportional to the FM/AM-1500 sweep signal when operating in the processor controlled sweep generator mode (RF Sweep or Tone Sweep Menus). The output amplitude at this connector is 0 to 10 volts, with 0 volts representing the start frequency and 10 volts representing the stop frequency.
- 60. DC Power Input Connector  
DC power input connector for 11 to 18 VDC supply.
- 61. AC Power Input Connector  
AC power input connector for 106 to 266 VAC supply at 50 to 400 Hz.
- 62. 10 MHz REF Connector  
Input/output connector for 10 MHz reference signal.
- 63. AC Line Fuse (2.5 Amp)

## 3-2 POWER SUPPLY FUNCTIONAL BLOCK

### 3-2-1 POWER SUPPLY VOLTAGE PERFORMANCE TEST

#### SPECIAL ACCESSORY

EQUIPMENT REQ'D: 1 DC Voltmeter---Any

#### TEST SET-UP

DIAGRAM: None

#### INITIAL FM/AM-1500

#### CONTROL SETTINGS:

| CONTROL           | SETTING                                   |
|-------------------|---|
| (13) PWR/OFF/BATT | "PWR"                                     |
| (19) GEN/REC      | "GEN"                                     |
| (51) DISPLAY      | Any position except "TRACK"<br>or "SWEEP" |

#### STEP

#### PROCEDURE

1. Using Voltmeter, verify +12 VDC ( $\pm 0.5$ ) on pin 1 of MIC Connector (34).

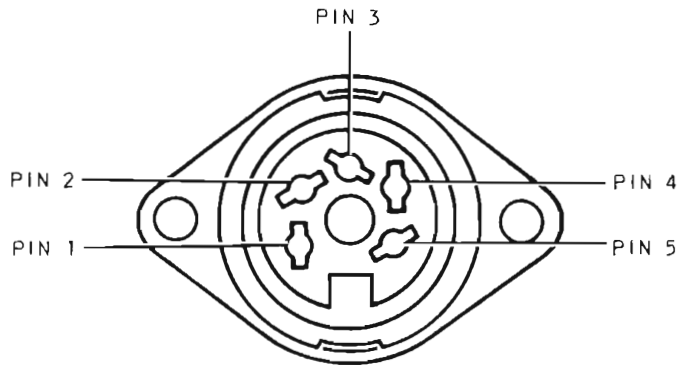


Figure 3-3 MIC Connector Pinouts

2. Using Voltmeter, verify voltages on EXT ACC Connector (29) as follows:

|       |                             |
|-------|-----------------------------|
| Pin 1 | +12 VDC ( $\pm 0.5$ )       |
| Pin 3 | +5 VDC ( $\pm 0.3, -0.15$ ) |
| Pin 2 | -12 VDC ( $\pm 0.5$ )       |

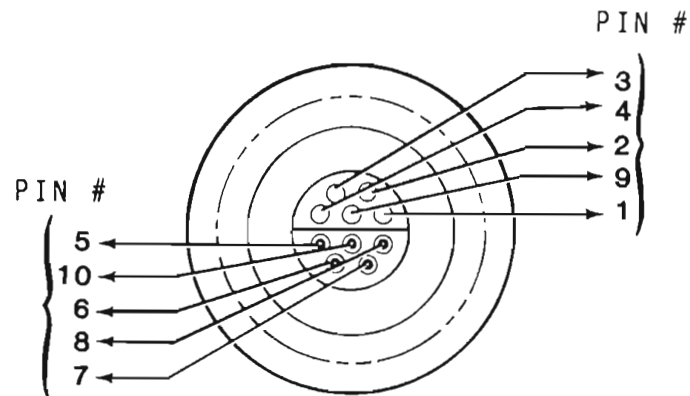


Figure 3-4 EXT ACC Connector Pinouts

3. Using voltmeter, verify +12 VDC ( $\pm 0.5$ ) on EXT AMP Connector (12).
4. Disconnect all test equipment.

**NOTE**

Front Panel voltages and tolerances only give an indication that the Power Supply output voltages are correct. If voltages are absent or grossly out of tolerance, refer to "SECTION 4 - CALIBRATION" for proper calibration procedure. If calibration is successful, problem is not in Power Supply, but is somewhere between Power Supply and Front Panel.



### 3-3 FREQUENCY STANDARD FUNCTIONAL BLOCK

#### 3-3-1 FREQUENCY STANDARD PERFORMANCE TEST

##### SPECIAL ACCESSORY

- EQUIPMENT REQ'D:
- 1 50 $\Omega$  Coax Cable, BNC to BNC
  - 1 50 $\Omega$  Termination (if necessary)
  - 1 Oscilloscope---Capable of measuring 150 mVp-p
  - 1 Frequency Counter---Capable of reading 10 MHz at 1 Hz resolution
  - 1 10 MHz Frequency Standard

##### TEST SET-UP

DIAGRAM: None

##### INITIAL FM/AM-1500

##### CONTROL SETTINGS:

| CONTROL           | SETTING |
|-------------------|---------|
| (13) PWR/OFF/BATT | "PWR"   |
| (19) GEN/REC      | "GEN"   |

##### STEP

##### PROCEDURE

1. Connect a 50 $\Omega$  coax cable between 10 MHz REF Connector (62) and input of an external Oscilloscope. Install a 50 $\Omega$  termination if Oscilloscope does not have a 50 $\Omega$  input. Verify amplitude of signal is > 75 mVp-P and < 150 mVp-p.
2. Disconnect 50 $\Omega$  coax cable from Oscilloscope. Connect coax to an external Frequency Counter. Install a 50 $\Omega$  termination if Frequency Counter does not have a 50 $\Omega$  input. Verify frequency is 10.000000 MHz ( $\pm 5$  Hz).
3. Disconnect 50 $\Omega$  coax cable from Frequency Counter. Connect coax to output of a 10 MHz frequency standard. Verify EXT REF (15) illuminates.
4. Disconnect all test equipment from FM/AM-1500.

### 3-4 FREQUENCY SYNTHESIS FUNCTIONAL BLOCK

#### 3-4-1 HIGH LOOP AND LOW LOOP PERFORMANCE TEST

SPECIAL ACCESSORY

- EQUIPMENT REQ'D: 1 50Ω Coax Cable, BNC to BNC  
 1 Frequency Counter---Capable of reading 1 GHz

TEST SET-UP

DIAGRAM: None

INITIAL FM/AM-1500

CONTROL SETTINGS:

| CONTROL                    | SETTING   |
|----------------------------|---|
| (10) RF Output Level       | As req'd for Frequency Counter (typically -20 dBm or greater) |
| (13) PWR/OFF/BATT          | "PWR"   |
| (18) DUPLEX/SIMPLEX        | "SIMPLEX"   |
| (19) GEN/REC               | "GEN"   |
| (21) LCD FREQUENCY READOUT | 000.5000 MHz  |
| (26) Tone 2 FM/OFF/AM      | "OFF"   |
| (28) Tone 1 FM/OFF/AM      | "OFF"   |

STEP

PROCEDURE

1. Connect 50Ω coax cable between TRANS/-40 dB DUPLEX Connector (11) and external Frequency Counter input. Verify external Frequency Counter reads 500 kHz ( $\pm 1$  Hz) and that Freq LOCK Indicator Lamp (43) illuminates.
2. Set LCD (21) to the following settings and verify frequency accuracy, depending on whether a TCX0 or oven oscillator is installed. Verify Freq LOCK Indicator Lamp (43) illuminates at each setting.

| <u>LCD FREQ MHz</u> | <u>TCX0</u>  | <u>OVEN</u> |
|---------------------|--------------|-------------|
| 111.1111            | $\pm 55$ Hz  | $\pm 6$ Hz  |
| 222.2222            | $\pm 111$ Hz | $\pm 12$ Hz |
| 333.3333            | $\pm 167$ Hz | $\pm 17$ Hz |
| 444.4444            | $\pm 223$ Hz | $\pm 23$ Hz |
| 555.5555            | $\pm 278$ Hz | $\pm 28$ Hz |
| 666.6666            | $\pm 334$ Hz | $\pm 34$ Hz |
| 777.7777            | $\pm 389$ Hz | $\pm 39$ Hz |
| 888.8888            | $\pm 444$ Hz | $\pm 45$ Hz |
| 999.9999            | $\pm 500$ Hz | $\pm 50$ Hz |

3. Disconnect all test equipment from FM/AM-1500.

### 3-5 RECEIVER FUNCTIONAL BLOCK

#### 3-5-1 RECEIVER SIGNAL PERFORMANCE TEST

##### SPECIAL ACCESSORY

- EQUIPMENT REQ'D: 1 Distortion Analyzer---Capable of measuring distortion at 1 kHz
- 1 50  $\Omega$  Coax Cable, BNC to BNC
- 1 Microphone
- 1 Signal Generator---Capable of generating 120.5000 MHz from -30 to -100 dBm

##### TEST SET-UP

DIAGRAM: None

##### INITIAL FM/AM-1500

##### CONTROL SETTINGS:

| CONTROL                    | SETTING                |
|----------------------------|------------------------|
| (7) MODULATION             | "FM 2"                 |
| (10) RF Output Level       | "0 dBm"                |
| (13) PWR/OFF/BATT          | "PWR"                  |
| (18) DUPLEX/SIMPLEX        | "SIMPLEX"              |
| (19) GEN/REC               | "REC"                  |
| (21) LCD FREQUENCY READOUT | (Local FM Station) MHz |
| (36) INT TONE/RCVR         | "RCVR"                 |
| (38) ANALY DISPR           | "1 M"                  |
| (51) DISPLAY               | "ANALY"                |

##### STEP

##### PROCEDURE

##### RECEIVER

1. Connect an antenna to ANTENNA Connector (56). Rotate VOLUME Control (22) to a comfortable listening level and observe FM signal on FM/AM-1500 Spectrum Analyzer. Verify FM station can be clearly heard.
2. Rotate MODULATION Control (7) to "AM 2". Rotate ANALY DISPR Control (38) to "20 K". Set LCD (21) to the frequency of a local AM radio station. Observe AM signal on FM/AM-1500 Spectrum Analyzer. Verify AM station can be clearly heard.
3. Disconnect antenna from FM/AM-1500.

## STEP

## PROCEDURE

SUB-AUDIBLE FILTER

1. Set FM/AM-1500 controls as follows:

| CONTROL               | SETTING   |
|-----------------------|---|
| (6) DEV/PWR           | "60 kHz"  |
| (7) MODULATION        | "FM 3"  |
| (13) PWR/OFF/BATT     | "PWR"   |
| (19) GEN/REC          | "GEN"   |
| (21) LCD READOUT      | 0400.0 TONE 1 Hz<br>10000 TONE 2 Hz<br>120.5000 MHz |
| (26) Tone 2 FM/OFF/AM | "FM"  |
| (28) Tone 1 FM/OFF/AM | "OFF"   |
| (31) TONE 2           | Fully ccw   |
| (33) TONE 1           | Fully ccw   |
| (37) FREQ ERROR       | "300 AUDIO Hz"                                      |
| (51) DISPLAY          | "METER"   |

2. Rotate TONE 2 Control (31) slowly cw until a DEMOD count of 10,000 Hz can be read on CRT (50), or until control is fully cw. Verify Deviation is  $\geq 10$  kHz.
3. Rotate TONE 2 Control (31) fully ccw.
4. Rotate DEV/PWR Control (6) to "2 kHz". Set LCD (21) to 0150.0 TONE 2 Hz. Rotate TONE 2 Control (31) slowly cw until a DEMOD count of 150 Hz can be read on CRT (50). Verify Deviation is  $\leq 1.0$  kHz. Verify both digital and analog meters read 250 Hz FREQ ERROR.
5. Set LCD (21) to 0410.0 TONE 1 Hz. Set LCD (21) to 10000 TONE 2 Hz. Rotate TONE 2 Control (31) slowly until lowest deviation level possible is reached, while still being able to read a 10 kHz DEMOD count on CRT (50). Verify deviation is  $\leq 1.0$  kHz. Verify both digital and analog FREQ ERROR meters are pegged.

RECEIVER SENSITIVITY

1. Set FM/AM-1500 controls as follows:

| CONTROL                    | SETTING      |
|----------------------------|--------------|
| (7) MODULATION             | "FM 1"       |
| (13) PWR/OFF/BATT          | "PWR"        |
| (19) GEN/REC               | "REC"        |
| (21) LCD FREQUENCY READOUT | 120.5000 MHz |
| (37) FREQ ERROR            | "300 Hz"     |
| (51) DISPLAY               | "METER"      |

## STEP

## PROCEDURE

2. Set external Signal Generator to 120.5000 MHz at -50 dBm.
3. Connect 50Ω coax cable between ANTENNA Connector (56) and output of Signal Generator. Note and record frequency error on both analog and digital meters.
4. Decrease output level of Signal Generator until a difference of 100 Hz from reading recorded in Step 3 is reached. Verify output level of external Signal Generator is  $\leq$  -99 dBm.
5. Rotate MODULATION Control (7) to "FM 2". Adjust output level of external Signal Generator until a difference of 100 Hz below reading recorded in Step 3 is reached. Verify output level of external Signal Generator is  $\leq$  -90 dBm.
6. Disconnect test equipment from FM/AM-1500.

DIGITALLY CODED SQUELCH

1. Set FM/AM-1500 controls as follows:

| CONTROL           | SETTING |
|-------------------|---------|
| (7) MODULATION    | "FM 2"  |
| (13) PWR/OFF/BATT | "PWR"   |
| (19) GEN/REC      | "GEN"   |
| (51) DISPLAY      | "TONES" |

2. Depress following keys: "MENU, V, MENU, ENTER, >, 1, 2, 6, >, >, ., 5, ENTER".

**NOTE**

Make sure polarity (POL) is normal (NORM) on menu.

3. Connect Microphone to MIC Connector (34).
4. Depress following keys: "EXEC, 2nd, DCS, 1, ENTER". Verify the blank spaces under "Valid Code Numbers" on CRT (50) have "126 302 430 110" displayed continuously (no blinking). Speak into keyed Microphone and verify displayed numbers are stable.
5. Depress following keys: "RF, ENTER, >, >, ^, ENTER, EXEC, ENTER". Verify the numbers "755 752" are displayed continuously. Speak into keyed Microphone and verify the displayed numbers are stable.
6. Depress "RF, ENTER" to stop function.
7. Disconnect Microphone from FM/AM-1500.

## STEP

## PROCEDURE

SIGNAL STRENGTH METERNOTE:

This procedure gives a relative signal strength indication only. Failure to meet the  $\pm 10$  dBm tolerance does not mean the FM/AM-1500 is faulty.

1. Set FM/AM-1500 controls as follows:

| CONTROL                    | SETTING      |
|----------------------------|--------------|
| (6) DEV/PWR                | "SIG"        |
| (13) PWR/OFF/BATT          | "PWR"        |
| (19) GEN/REC               | "REC"        |
| (21) LCD FREQUENCY READOUT | 120.5000 MHz |
| (51) DISPLAY               | "METER"      |

2. Set Signal Generator to 120.5000 MHz at approximately -30 dBm.
3. Connect 50 $\Omega$  coax cable between output of Signal Generator and ANTENNA Connector (56).
4. Adjust output level of Signal Generator for a 100% ( $\pm 0.1\%$ ) reading on digital (SIGNAL %) display. Verify dBm setting on Signal Generator is -30 dBm ( $\pm 10$  dBm).
5. Disconnect all test equipment from FM/AM-1500.

AUDIO DISTORTION

1. Set FM/AM-1500 controls as follows:

| CONTROL                 | SETTING          |
|-------------------------|------------------|
| (6) DEV/PWR             | "6 kHz"          |
| (7) MODULATION          | "FM 1"           |
| (13) PWR/OFF/BATT       | "PWR"            |
| (19) GEN/REC            | "GEN"            |
| (21) LCD TONE 1 READOUT | 1000.0 Hz TONE 1 |
| (26) Tone 2 FM/OFF/AM   | "OFF"            |
| (28) Tone 1 FM/OFF/AM   | "FM"             |
| (39) DEV/VERT           | "2 kHz/DIV"      |
| (51) DISPLAY            | "SCOPE"          |

2. Rotate Tone 1 Control (33) until MODULATION Meter (1) indicates 5 kHz deviation.
3. Observe waveform on CRT (50) and verify no obvious distortion.
4. Connect 50 $\Omega$  coax cable between DEMOD OUTPUT Connector (25) and input of an external Distortion Analyzer. Verify distortion is  $\leq 5\%$ .

## STEP

## PROCEDURE

5. Disconnect all test equipment from FM/AM-1500.

SINAD

1. Set FM/AM-1500 controls as follows:

| CONTROL                 | SETTING          |
|-------------------------|------------------|
| (5) HORIZ               | "1 mS/DIV"       |
| (6) DEV/PWR             | "SINAD"          |
| (13) PWR/OFF/BATT       | "PWR"            |
| (18) DUPLEX/SIMPLEX     | "SIMPLEX"        |
| (19) GEN/REC            | "GEN"            |
| (21) LCD TONE 1 READOUT | 1000.0 Hz TONE 1 |
| TONE 2 READOUT          | 1800.0 Hz TONE 2 |
| (26) Tone 2 FM/OFF/AM   | "OFF"            |
| (28) Tone 1 FM/OFF/AM   | "OFF"            |
| (31) TONE 2             | Fully ccw        |
| (33) TONE 1             | Fully cw         |
| (39) DEV/VERT           | "1 V/DIV"        |
| (51) DISPLAY            | "SCOPE"          |

2. Connect 50 $\Omega$  coax cable between TONES OUTPUT Connector (27) and SCOPE/SINAD INPUT Connector (24).
3. Rotate VERT VERNIER Control (44) to make FM/AM-1500 CRT (50) display exactly 8 major vertical divisions.
4. Rotate TONE 1 Control (33) fully ccw.
5. Rotate TONE 2 Control (31) in a cw direction until CRT (50) display is exactly 2 major vertical divisions.
6. Rotate TONE 1 Control (33) fully cw.
7. Rotate DISPLAY Control (51) to "METER". Verify both digital meter display on CRT (50) and MODULATION Meter (1) display are reading -12 dB ( $\pm 1$  dB) on SINAD scales.
8. Rotate TONE 2 Control (31) fully ccw. Verify digital meter display on CRT (50) reads  $\leq$  -26 dB.
9. Disconnect all test equipment from FM/AM-1500.

### 3-5-2 FREQUENCY ERROR PERFORMANCE TEST

#### SPECIAL ACCESSORY

- EQUIPMENT REQ'D: 1 Signal Generator---Capable of generating  
120.5030 MHz at -50 dBm
- 2 50Ω Coax Cables, BNC to BNC
- 1 10 MHz Frequency Standard

#### TEST SET-UP

DIAGRAM: None

#### INITIAL FM/AM-1500

#### CONTROL SETTINGS:

| CONTROL                    | SETTING                   |
|----------------------------|---------------------------|
| (13) PWR/OFF/BATT          | "PWR"                     |
| (18) DUPLEX/SIMPLEX        | "SIMPLEX"                 |
| (19) GEN/REC               | "REC"                     |
| (21) LCD FREQUENCY READOUT | 120.5000 MHz              |
| (37) FREQ ERROR            | "1 kHz"                   |
| (51) DISPLAY               | "METER"                   |
| (7) MODULATION             | "FM2" (or "FM3" or "FM4") |

#### STEP

#### PROCEDURE

1. Connect 50Ω coax cable between 10 MHz standard and external time base input of Signal Generator.
2. Set Signal Generator to 120.5000 MHz at -50 dBm.
3. Connect 50Ω coax cable between output of Signal Generator and ANTENNA Connector (56). Verify FREQ ERROR is  $\leq 100$  Hz. Note and record reading.
4. Rotate INT REF CAL Adjustment (17) to both stops. Verify range is approximately equal in both directions. Rotate INT REF CAL Adjustment (17) back to setting recorded in Step 3.
5. Rotate FREQ ERROR Control (37) to "30 Hz".
6. Set external Signal Generator to 120.5001 MHz. Verify full deflection of FREQ ERROR Meter (41) and verify approximately 100 Hz ( $\pm$  reading recorded in Step 3) on CRT (50) digital meter.
7. Set external Signal Generator to 120.4999 MHz and verify same results as in Step 6.



## STEP

## PROCEDURE

8. Rotate FREQ ERROR Control (37) to "300 Hz". Set external Signal Generator first to 120.4997 MHz, then to 120.5003 MHz. Verify a 300 Hz ( $\pm 5\%$ ) frequency error on both the analog and digital meters at each setting.
9. Rotate FREQ ERROR Control (37) to "1 kHz". Set external Signal Generator first to 120.5010 MHz, then to 120.4990 MHz. Verify a 1 kHz frequency error on both the analog and digital meters at each setting.
10. Rotate FREQ ERROR Control (37) to "3 kHz". Set external Signal Generator first to 120.5030 MHz, then to 120.4970 MHz. Verify a 3 kHz frequency error on both the analog and digital meters at each setting.
11. Rotate FREQ ERROR Control (37) to "10 kHz". Set external Signal Generator first to 120.5100 MHz, then to 120.4900 MHz. Verify a 10 kHz frequency error on both the analog and digital meters at each setting.
12. Set GEN/REC Switch (19) to "GEN". Rotate GEN/LOCK Control (35) out of "LOCK". Verify by rotating the GEN/LOCK Control (35) to its - and + limits, that there is at least 10 kHz variation from 0 on both sides of the FREQ ERROR Meter (41).

3-5-3 MODULATION METER PERFORMANCE TEST

SPECIAL ACCESSORY

- EQUIPMENT REQ'D: 1 Signal Generator---Capable of generating 850 MHz at -50 dBm; 2 to 8 kHz Dev. at 1 to 10 kHz rate
- 1 Modulation Meter---Capable of measuring 2 to 8 kHz Dev.
- 1 50Ω Coax Cable, BNC to BNC

TEST SET-UP

DIAGRAM: None

INITIAL FM/AM-1500

CONTROL SETTINGS:

| CONTROL                    | SETTING      |
|----------------------------|--------------|
| (4) AVG PEAK/PEAK          | "AVG"        |
| (6) DEV/PWR                | "6 kHz"      |
| (7) MODULATION             | "FM 2"       |
| (19) GEN/REC               | "REC"        |
| (21) LCD FREQUENCY READOUT | 850.0000 MHz |
| (51) DISPLAY               | "METER"      |

STEP

PROCEDURE

1. Set external Signal Generator to 850 MHz at -50 dBm. Modulate its FM signal with 5 kHz Deviation at 1 kHz.
2. Set external Modulation Meter bandpass filters to 300 Hz and 3 kHz. Verify modulation level of Signal Generator by using external Modulation Meter.
3. Connect 50Ω coax cable between ANTENNA Connector (56) and output of Signal Generator. Verify digital meter on CRT (50) is accurate ( $\pm 5\%$ ).
4. Change Signal Generator modulation to 2 kHz Deviation at 6 kHz. Change Modulation Meter bandpass filters to 300 Hz and 15 kHz. Verify modulation level of Signal Generator by using external Modulation Meter.
5. Repeat Step 3, but verify accuracy as  $\pm 3\%$ .
6. Rotate MODULATION Control (7) to "FM 3". Rotate DEV/PWR Control (6) to "20 kHz". Change Modulation Meter low-pass filter to 120 kHz. Change Signal Generator modulation to 8 kHz Deviation at 10 kHz. Verify modulation level of Signal Generator by using external Modulation Meter.

## STEP

## PROCEDURE

7. Repeat Step 3, verify accuracy as  $\pm 3\%$ .
8. Rotate DISPLAY Control (51) to "SCOPE". Rotate DEV/VERT Control (39) to "5 kHz/DIV". Verify 8 kHz Deviation ( $\pm 10\%$ ) on CRT (50).
9. Change Signal Generator modulation to 2 kHz Deviation at 6 kHz. Rotate DEV/VERT Control (39) to "2 kHz". Verify 2 kHz Deviation ( $\pm 10\%$ ) on CRT (50).
10. Change Signal Generator modulation to 5 kHz Deviation at 1 kHz. Verify 5 kHz Deviation ( $\pm 10\%$ ) on CRT (50).

### 3-5-4 OSCILLOSCOPE PERFORMANCE TEST

#### SPECIAL ACCESSORY

- EQUIPMENT REQ'D: 1 Oscilloscope Calibrator Module (Plug-In)---  
Capable of 0.5 to 50 VAC
- 1 50 $\Omega$  Coax Cable, BNC to BNC
- 1 Audio Generator---Capable of generating 100 Hz  
to 100 kHz

#### TEST SET-UP

DIAGRAM: None

#### INITIAL FM/AM-1500

##### CONTROL SETTINGS:

| CONTROL           | SETTING     |
|-------------------|-------------|
| (3) HORIZ VERNIER | "CAL"       |
| (39) DEV/VERT     | ".01 V/DIV" |
| (44) VERT VERNIER | "CAL"       |
| (51) DISPLAY      | "SCOPE"     |

#### STEP

#### PROCEDURE

1. Connect 50 $\Omega$  coax cable between SCOPE/SINAD INPUT Connector (24) and output of Oscilloscope Calibrator.
2. Set output of Oscilloscope Calibrator to 50 mVAC. Verify a 5 ( $\pm 0.5$ ) major division deflection.
3. Rotate DEV/VERT Control (39) to ".1 V/DIV" and set output of Oscilloscope Calibrator to 0.5 VAC. Verify a 5 ( $\pm 0.5$ ) major division deflection.
4. Rotate DEV/VERT Control (39) to "1 V/DIV" and set output of Oscilloscope Calibrator to 5 VAC. Verify a 5 ( $\pm 0.5$ ) major division deflection.
5. Rotate DEV/VERT Control (39) to "10 V/DIV" and set output of Oscilloscope Calibrator to 50 VAC. Verify a 5 ( $\pm 0.5$ ) major division deflection.
6. Rotate VERT VERNIER Control (44) fully ccw. Verify deflection is less than 2.5 major divisions.
7. Disconnect 50 $\Omega$  coax cable from Oscilloscope Calibrator and connect 50 $\Omega$  coax cable to output of an Audio Generator.

## STEP

## PROCEDURE

8. Rotate DEV/VERT Control (39) to "1 V/DIV". Set output of Audio Generator to 100 kHz at  $\geq 2$  Vp-p and rotate HORIZ Control (5) to ".01 mS/DIV". Verify CRT (50) displays 10 ( $\pm 2$ ) full cycles.
9. Set output of Audio Generator to 10 kHz and rotate HORIZ Control (5) to ".1 mS/DIV". Verify CRT (50) displays 10 ( $\pm 2$ ) full cycles.
10. Set output of Audio Generator to 1 kHz and rotate HORIZ Control (5) to "1 mS/DIV". Verify CRT (50) displays 10 ( $\pm 2$ ) full cycles.
11. Set output of Audio Generator to 100 Hz and rotate HORIZ Control (5) to "10 mS/DIV". Verify CRT (50) displays 10 ( $\pm 2$ ) full cycles.
12. Repeat Steps 8 thru 11 and verify that HORIZ VERNIER Control (3) will vary horizontal spacing on CRT (50) for each step.
13. Disconnect all test equipment from FM/AM-1500.

3-5-5 POWER METER PERFORMANCE TEST

SPECIAL ACCESSORY

EQUIPMENT REQ'D: 1 RF Power Source---Capable of generating 15.7  
to 902 MHz at 10 to 30 W

1 50Ω Coax Cable, BNC to BNC

TEST SET-UP

DIAGRAM: None

INITIAL FM/AM-1500

CONTROL SETTINGS:

| CONTROL           | SETTING    |
|-------------------|------------|
| (6) DEV/PWR       | "15 WATTS" |
| (13) PWR/OFF/BATT | "PWR"      |
| (51) DISPLAY      | "METER"    |

STEP

PROCEDURE

1. Set RF Power Source to 860 MHz at 10 W.
2. Connect 50Ω coax cable between output of RF Power Source and TRANS/-40 dB DUPLEX Connector (11). Verify power reading on digital and analog meters is 10 W ( $\pm 1.15$  W).
3. Rotate DEV/PWR Control (6) to "150 WATTS". Verify same readings as in Step 2.
4. Set RF Power Source to 30 W output power. Verify power reading on digital and analog meters is 30 W ( $\pm 6.6$  W).
5. Disconnect 50Ω coax cable. Rotate DEV/PWR Control (6) to "15 WATTS". Set RF Power Source to 157 MHz at 10 W. Repeat Steps 2 thru 4.
6. Disconnect all test equipment from FM/AM-1500.

### 3-6 GENERATOR FUNCTIONAL BLOCK

#### 3-6-1 RF OUTPUT PERFORMANCE TEST

##### SPECIAL ACCESSORY

- EQUIPMENT REQ'D: 1 Spectrum Analyzer---Capable of measuring 0 dBm at 850 MHz
- 1 50Ω Coax Cable, BNC to BNC
- 1 Microphone
- 1 Modulation Meter---Capable of measuring residual FM at 850 MHz
- 1 Signal Generator---Capable of generating 850 MHz at 0 to -90 dBm
- 1 Power Meter---Capable of measuring 0 dBm at 850 MHz

##### TEST SET-UP

DIAGRAM: None

##### INITIAL FM/AM-1500

##### CONTROL SETTINGS:

| CONTROL                    | SETTING      |
|----------------------------|--------------|
| (10) RF Output Level       | "0 dBm"      |
| (13) PWR/OFF/BATT          | "PWR"        |
| (18) DUPLEX/SIMPLEX        | "SIMPLEX"    |
| (19) GEN/REC               | "GEN"        |
| (21) LCD FREQUENCY READOUT | 850.0000 MHz |

##### STEP

##### PROCEDURE

##### ATTENUATOR ACCURACY

1. Set external Spectrum Analyzer to log scale of 2 dB/division.
2. Connect 50Ω coax cable between TRANS/-40 dBm DUPLEX Connector (11) and external Spectrum Analyzer input. Set reference level of external Spectrum Analyzer so that top of applied signal exactly reaches a horizontal graticule. Note and record position of signal.
3. Disconnect 50Ω coax cable from TRANS/-40 dB DUPLEX Connector (11) and connect 50Ω coax cable to output of Signal Generator.
4. Set external Signal Generator to 850 MHz at output level in Table 3-1 corresponding to RF Output Level (10) setting.

## STEP

## PROCEDURE

5. Set top of applied signal on external Spectrum Analyzer to same position as recorded in Step 2 by adjusting only output level of Signal Generator.
6. Disconnect 50 $\Omega$  coax cable from Spectrum Analyzer and connect 50 $\Omega$  coax cable to input of external Power Meter. Verify Power Meter reads as in Table 3-1 for corresponding RF Output Level (10).
7. Repeat Steps 2 thru 6 for each RF Output Level (10) setting in Table 3-1.

**NOTE**

For RF Output Level (10) settings of -50 dBm and below, it may be necessary to add attenuation pad(s) between Signal Generator and Spectrum Analyzer in Step 5 in order for Power Meter to operate properly in Step 6. For instance, if Power Meter will only read correctly at -50 dB or above and RF Output Level (1) is -70 dBm, a 20 dB pad plus a Signal Generator output of -50 dBm would result in an external Spectrum Analyzer reading of -70 dBm.

If it is necessary to add attenuation for proper attenuation reading into Power Meter, remove attenuation before performing Step 7 and add value of attenuation pad to resultant Power Meter reading.

| RF OUTPUT LEVEL (dBm) | SIGNAL GENERATOR OUTPUT (dBm) | POWER METER READING (dBm) |
|-----------------------|-------------------------------|---------------------------|
| 0                     | 0                             | 0 ( $\pm 4$ )             |
| -10                   | -10                           | -10 ( $\pm 2.0$ )         |
| -30                   | -30                           | -30 ( $\pm 2.0$ )         |
| -50                   | -50                           | -50 ( $\pm 2.0$ )         |
| -70                   | -70                           | -70 ( $\pm 2.0$ )         |
| -90                   | -90                           | -90 ( $\pm 2.5$ )         |

Table 3-1 Attenuator Accuracy Test Settings

8. Connect 50 $\Omega$  coax cable between TRANS/-40 dB DUPLEX Connector (11) and input of external Spectrum Analyzer. Rotate RF Output Level (10) fully ccw and verify Spectrum Analyzer shows no RF leakage at TRANS/-40 dB DUPLEX Connector (11) of FM/AM-1500.
9. Disconnect all test equipment from FM/AM-1500.



## STEP

## PROCEDURE

MODULATION

1. Set FM/AM-1500 controls as follows:
 

| CONTROL                 | SETTING     |
|-------------------------|-------------|
| (5) HORIZ               | "1 mS/DIV"  |
| (6) DEV/PWR             | "20 kHz"    |
| (7) MODULATION          | "AM 2"      |
| (13) PWR/OFF/BATT       | "PWR"       |
| (18) DUPLEX/SIMPLEX     | "SIMPLEX"   |
| (19) GEN/REC            | "GEN"       |
| (21) LCD TONE 1 READOUT | 1000.0 Hz   |
| (26) Tone 2 FM/OFF/AM   | "OFF"       |
| (28) Tone 1 FM/OFF/AM   | "AM"        |
| (36) INT TONE/RCVR      | "RCVR"      |
| (39) DEV/VERT           | "5 kHz/DIV" |
| (51) DISPLAY            | "SCOPE"     |
2. Rotate Tone 1 Control (33) until CRT (50) and MODULATION Meter (1) both display at least 90% AM.
3. Rotate DISPLAY Control (51) to "METER". Verify 90% AM ( $\pm 7\%$ ).
4. Rotate MODULATION Control (7) to "FM 2". Set Tone 1 FM/OFF/AM Switch (28) to "FM". Rotate DEV/PWR Control (6) to "60 kHz". Rotate TONE 1 Control (33) fully cw. Verify  $\geq 20$  kHz deviation on MODULATION meter (1) and on CRT (50) digital display.
5. Set Tone 1 FM/OFF/AM Switch (28) to "OFF". Connect 50 $\Omega$  coax cable between TONES OUTPUT Connector (27) and EXT FM MOD Connector (32). Verify  $\geq 20$  kHz deviation on CRT (50) digital display and MODULATION Meter (1).
6. Disconnect 50 $\Omega$  coax cable from EXT FM MOD Connector (32) and connect it to EXT AM MOD Connector (30). Rotate MODULATION Control (7) to "AM 2". Verify modulation is present on CRT (50) digital display and MODULATION Meter (1).
7. Disconnect coax cable from FM/AM-1500. Connect a microphone to MIC Connector (34). Set GEN/REC Switch (19) to "REC".
8. Key microphone and whistle into it. Verify 100% AM ( $\pm 50\%$ ) on CRT (50) digital display and MODULATION Meter (1) while whistling into microphone.
9. Rotate MODULATION Control (7) to "FM 2". Verify  $\geq 3.50$  kHz deviation while whistling into microphone.
10. Rotate DISPLAY Control (51) to "ANALY". Verify keying the microphone causes a signal to appear on CRT (50).

## STEP

## PROCEDURE

11. Disconnect all test equipment from FM/AM-1500.

DELAY LINE

1. Set FM/AM-1500 controls as follows:

| CONTROL                    | SETTING      |
|----------------------------|--------------|
| (10) RF Output Level       | "-30 dBm"    |
| (13) PWR/OFF/BATT          | "PWR"        |
| (18) DUPLEX/SIMPLEX        | "SIMPLEX"    |
| (21) LCD FREQUENCY READOUT | 001.0000 MHz |
| (26) Tone 2 FM/OFF/AM      | "OFF"        |
| (28) Tone 1 FM/OFF/AM      | "OFF"        |
| (51) DISPLAY               | "ANALY"      |

2. Set external Spectrum Analyzer settings as follows:

Dispersion - 200 kHz/division  
 Log Scale - 10 dB/division  
 Reference Level - as required to display entire signal

3. Connect 50 $\Omega$  coax cable between TRANS/-40 dB DUPLEX Connector (11) and input of external Spectrum Analyzer.
4. Using KEYBOARD (20), press "RF,> ,> " to place cursor under 1 MHz digit on LCD (21).
5. By pressing "^" Key repeatedly, step MHz on LCD FREQUENCY READOUT (21) up to 100 MHz. At each step, observe the display on the external Spectrum Analyzer. The noise level around the base of the displayed signal should rise and immediately fall back to a low level (below -60 dBc). Verify the FM/AM-1500 does not have a rattling noise at each step in frequency.
6. Set LCD FREQUENCY (21) to 170.000 MHz. Repeat Steps 4 and 5, but stepping up to 180.0000 MHz.
7. Set LCD FREQUENCY (21) to 400.0000 FREQ MHz. Repeat Steps 4 and 5, but stepping up to 515.0000 FREQ MHz.

**NOTE**

Crossover distortion will produce noticeable sidebands around 515.0000 MHz.

8. Set LCD FREQUENCY (21) to 800.0000 MHz. Repeat Steps 4 and 5, but stepping up to 950.0000 FREQ MHz.

## STEP

## PROCEDURE

9. Set LCD FREQUENCY (21) to 999.9999 MHz. Verify same results as in Step 5.

NOTE:

If FM/AM-1500 makes a rattling noise, or if noise level at base of each selected signal does not immediately decrease, the Delay Line is defective.

10. Disconnect all test equipment from FM/AM-1500.

RESIDUAL FM

1. Set FM/AM-1500 controls as follows:

| CONTROL               | SETTING   |
|-----------------------|-----------|
| (4) AVG PEAK/PEAK     | "PEAK"    |
| (6) DEV/PWR           | "2 kHz"   |
| (7) MODULATION        | "FM 2"    |
| (10) RF Output Level  | "0 dBm"   |
| (13) PWR/OFF/BATT     | "PWR"     |
| (18) DUPLEX/SIMPLEX   | "SIMPLEX" |
| (19) GEN/REC          | "GEN"     |
| (26) Tone 2 FM/OFF/AM | "OFF"     |
| (28) Tone 1 FM/OFF/AM | "OFF"     |
| (51) DISPLAY          | "METER"   |

2. Set external Modulation Meter as follows:

FM - 10 kHz Range  
High Pass Filters - 300 Hz  
Low Pass Filters - 3 kHz

3. Connect 50Ω coax cable between TRANS/-40 dB DUPLEX Connector (11) and input of external Modulation Meter. Verify residual FM  $\leq$  50 Hz.
4. Rotate MODULATION Control (7) to "FM 2". Verify residual FM  $\leq$  50 Hz.
5. Rotate MODULATION Control (7) to "FM 3". Verify residual FM  $\leq$  50 Hz.
6. Rotate MODULATION Control (7) to "FM 4". Verify residual FM  $\leq$  200 Hz.

STEP

PROCEDURE

7. Set LCD FREQUENCY (21) to 850.0000 FREQ MHz. Repeat Steps 3 thru 6 using following limits:  
FM1, FM2, and FM3  $\leq$  200 Hz residual FM;  
FM4  $\leq$  250 Hz residual FM
8. Disconnect all test equipment from FM/AM-1500.

### 3-6-2 DUPLEX OFFSET PERFORMANCE TEST

#### SPECIAL ACCESSORY

- EQUIPMENT REQ'D: 1 50 $\Omega$  Coax Cable, BNC to BNC  
1 50 $\Omega$  Termination, BNC  
1 Spectrum Analyzer---Capable of measuring  
-10 dBm at 800 MHz  
1 Frequency Counter---Capable of counting 850 MHz

#### TEST SET-UP

DIAGRAM: None

#### INITIAL FM/AM-1500

#### CONTROL SETTINGS:

| CONTROL              | SETTING           |
|----------------------|-------------------|
| (10) RF Output Level | "-10 dBm"         |
| (13) PWR/OFF/BATT    | "PWR"             |
| (18) DUPLEX/SIMPLEX  | "DUPLEX"          |
| (19) GEN/REC         | "GEN"             |
| (21) LCD             | 800.0000 FREQ MHz |

#### STEP

#### PROCEDURE

1. Connect 50 $\Omega$  coax cable between DUPLEX Output Connector (16) and external Spectrum Analyzer.
2. Verify level on external Spectrum Analyzer is -10 dBm ( $\pm 2$  dB).
3. Disconnect 50 $\Omega$  coax cable from DUPLEX OUTPUT Connector (16) and connect it to TRANS/-40 dB DUPLEX Connector (11).
4. Connect a 50 $\Omega$  termination to DUPLEX OUTPUT Connector (16).
5. Verify dB level on external Spectrum Analyzer is -50 dBm ( $\pm 3$  dB).
6. Disconnect external Spectrum Analyzer from TRANS/-40 dB DUPLEX Connector (11) and disconnect 50 $\Omega$  termination from DUPLEX OUTPUT Connector (16).
7. Connect 50 $\Omega$  coax cable between DUPLEX OUTPUT Connector (16) and external Frequency Counter input. Set external Frequency Counter resolution to 100 Hz.

## STEP

## PROCEDURE

8. Press "OFFSET,1,1,1,1" on KEYBOARD (20) and verify external Frequency Counter reads 811.1100 MHz ( $\pm 1$  kHz).
9. Repeat Step 8 for OFFSET of 22.22, 33.33, 44.44 and 49.99 MHz. Verify external Frequency Counter reads 800 MHz + OFFSET value ( $\pm 1$  kHz).
10. Press "OFFSET,-,4,9,9,9" on KEYBOARD (20) and verify external Frequency Counter reads 750.0100 MHz ( $\pm 1$  kHz).
11. Repeat Step 10 for OFFSET of -44.44, -33.33, -22.22, -11.11, and -00.00 MHz. Verify external Frequency Counter reads 800 MHz - OFFSET value ( $\pm 1$  kHz).

**NOTE**

OFFSET will not operate correctly if OFFSET is entered as  $\geq 50.00$  MHz.

12. Disconnect all test equipment from FM/AM-1500.

### 3-6-3 DUAL TONE GENERATOR PERFORMANCE TEST

#### SPECIAL ACCESSORY

- EQUIPMENT REQ'D:
- 1 50Ω Coax Cable, BNC to BNC
  - 1 BNC Tee
  - 1 Digital Voltmeter---Any
  - 1 150Ω Load; See Appendix D
  - 1 50Ω Coax Cable, BNC to Banana Jacks
  - 1 Frequency Counter---Capable of counting from 6 Hz to 20 kHz

TEST SET-UP  
DIAGRAM:

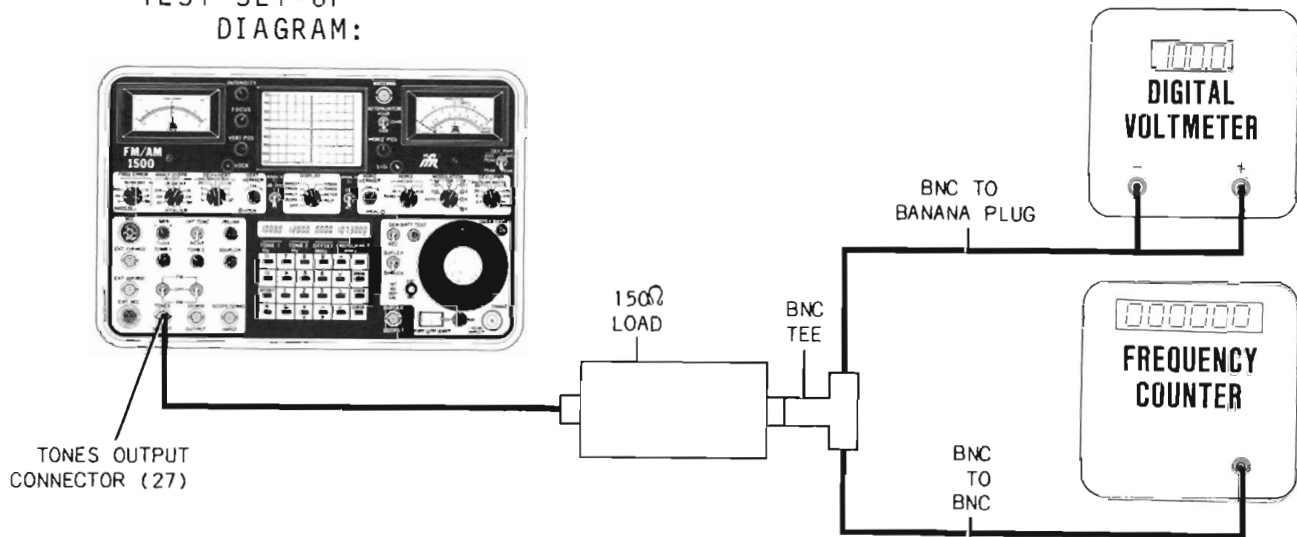


Figure 3-5 Dual Tone Generator Test Set-Up Diagram

#### INITIAL FM/AM-1500 CONTROL SETTINGS:

| CONTROL            | SETTING          |
|--------------------|------------------|
| (5) HORIZ          | "10 mS/DIV"      |
| (7) MODULATION     | "FM 4"           |
| (13) PWR/OFF/BATT  | "PWR"            |
| (21) LCD           | 0000.1 Hz TONE 1 |
|                    | 0000.1 Hz TONE 2 |
| (22) VOLUME        | Fully cw         |
| (31) TONE 2        | Fully ccw        |
| (33) TONE 1        | Fully ccw        |
| (36) INT TONE/RCVR | "INT TONE"       |
| (39) DEV/VERT      | "2 kHz/DIV"      |
| (51) DISPLAY       | "SCOPE"          |

## STEP

## PROCEDURE

AUDIO GENERATORS

1. Connect test equipment to FM/AM-1500 as shown in Figure 3-5.
2. Rotate TONE 1 Control (33) fully cw and verify that low-pitch audio chatter is heard and that CRT (50) displays a stair-step pattern.
3. Repeat Step 2 for TONE 1 Hz settings on LCD (21) of: 0.1, 0.4, 0.8, 1.6 and 3.2 Hz.
4. Rotate DISPLAY Control (51) to "METER".
5. Set TONE 1 Hz on LCD (21) to 6.4 Hz. Verify DVM reads > 2.5 VRMS and that Frequency Counter is within 0.01% of TONE 1 Hz setting on LCD (21). Also verify the digital Demod Count meter on the CRT (50) displays the value of the TONE 1 Hz setting ( $\pm 0.1\%$ ).
6. Rotate TONE 1 Control (33) fully ccw and verify that DVM reads approximately 0 VRMS and Frequency Counter reads 0 Hz.
7. Repeat Steps 5 and 6 for TONE 1 Hz settings on LCD (21) of: 12.8, 25.6, 51.2, 409.5, 409.6, 1000.0, 5000, 9999, 13107 and 20000 Hz.
8. Rotate TONE 1 Control (33) fully ccw. Rotate TONE 2 Control (31) fully cw and repeat Steps 2 thru 7, using TONE 2.
9. Disconnect all test equipment from FM/AM-1500.

TONE SWEEP, X-OUT AND DTMF

1. Set FM/AM-1500 controls as follows:

| CONTROL               | SETTING     |
|-----------------------|-------------|
| (5) HORIZ             | "10 mS/DIV" |
| (13) PWR/OFF/BATT     | "PWR"       |
| (19) GEN/REC          | "GEN"       |
| (22) VOLUME           | Fully ccw   |
| (26) Tone 2 FM/OFF/AM | "OFF"       |
| (28) Tone 1 FM/OFF/AM | "OFF"       |
| (33) TONE 1           | Fully cw    |
| (36) INT TONE/RCVR    | "INT TONE"  |
| (39) DEV/VERT         | "1 V/DIV"   |
| (51) DISPLAY          | "TONES"     |
| (52) DC/AC            | "DC"        |



## STEP

## PROCEDURE

2. Depress "MENU" and then "V" until "TONE SWEEP MENU" appears. Depress "MENU, ENTER, >, 1, 0, 0, >, 1, 0, 0, 0, >, >, 1, 0, 0, >, 5, ENTER, EXEC, 2nd, T. SWP., 1, ., ENTER".
3. Rotate VOLUME Control (22) to a comfortable listening level and verify Tone Sweep operation.

**NOTE**

A "warbling" sound will be heard if Tone Sweep is operating.

4. Connect 50 $\Omega$  coax cable between X-OUT Connector (59) and SCOPE/SINAD INPUT Connector (24).
5. Rotate DISPLAY Control (51) to "SCOPE". Verify a "stair-step" display on CRT (50).
6. Depress "RF, ENTER" to stop function. Disconnect coax cable.
7. Rotate TONE 1 Control (33) fully ccw.
8. Depress "EXEC, 2nd, DTMF, 1, ENTER". Verify DTMF ("touch-tone") is heard.
9. Depress "2nd, DTMF". Verify "touch-tone" is heard as each key (0, 1, 2, 3, 4, 5, 6, 7, 8, 9, \*, #) is depressed and that frequencies are displayed on LCD (21) for each key selection.
10. Depress "ENTER" to stop function.
11. Disconnect all test equipment from FM/AM-1500.

TONE SEQUENCE

1. Set FM/AM-1500 controls as follows:

| CONTROL               | SETTING       |
|-----------------------|---------------|
| (4) AVG PEAK/PEAK     | "AVG PEAK"    |
| (6) DEV/PWR           | "6 kHz"       |
| (7) MODULATION        | "FM 2"        |
| (13) PWR/OFF/BATT     | "PWR"         |
| (19) GEN/REC          | "GEN"         |
| (22) VOLUME           | Midrange      |
| (26) Tone 2 FM/OFF/AM | "OFF"         |
| (28) Tone 1 FM/OFF/AM | "OFF"         |
| (38) ANALY DISPR      | < "1 MHz/DIV" |
| (51) DISPLAY          | "TONES"       |

STEP

PROCEDURE

2. On KEYBOARD (20), depress the following keys: "MENU, ENTER, >, 1, 0, 0, 0, >, 5, >, 9, 9, 9, 9, >, 0, >, 0, ENTER".
3. Rotate Display Control (51) to "METER".
4. Depress keys: "EXEC, 2nd, T.SEQ., 1, ENTER". Verify both digital and analog meters indicate 5.00 kHz ( $\pm 5\%$ ) deviation.
5. Rotate MODULATION Control (7) to "AM 2".
6. Depress following keys: "EXEC, ENTER". Verify both digital and analog meters read between 42.5% and 57.5% AM modulation.
7. Disconnect all test equipment from FM/AM-1500.

### 3-7 SPECTRUM ANALYZER FUNCTIONAL BLOCK

#### 3-7-1 SPECTRUM ANALYZER PERFORMANCE TEST

##### SPECIAL ACCESSORY

- EQUIPMENT REQ'D: 1 Signal Generator---Capable of generating  
-30 dBm at 120.5 MHz
- 1 50 $\Omega$  Coax Cable, BNC to BNC
- 2 20 dB Attenuator Pads

##### TEST SET-UP

DIAGRAM: None

##### INITIAL FM/AM-1500

##### CONTROL SETTINGS:

| CONTROL                    | SETTING      |
|----------------------------|--------------|
| (13) PWR/OFF/BATT          | "PWR"        |
| (19) GEN/REC               | "REC"        |
| (21) LCD FREQUENCY READOUT | 120.5000 MHz |
| (38) ANALY DISPR           | "20 kHz/DIV" |
| (48) dB/DIV                | "10 dB/DIV"  |
| (51) DISPLAY               | "ANALY"      |
| (55) ATTENUATOR            | "0 dB"       |

##### STEP

##### PROCEDURE

##### ANALYZER LEVEL

1. Set Signal Generator to 120.5 MHz at about -40 dBm.
2. Connect 50 $\Omega$  coax cable between ANTENNA Connector (56) and output of Signal Generator.
3. Adjust output level of Signal Generator so that displayed signal on CRT (50) is exactly on the -40 dB graticule. Note and record output level of Signal Generator.
4. Step output level of Signal Generator in 10 dB steps from -30 dBm to -90 dBm. At each setting, verify displayed signal on CRT (50) is at corresponding graticule ( $\pm 2$  dB).
5. Set Signal Generator output level to -40 dBm. Set ATTENUATOR Switch (55) to "20 dB". Note and record position of signal on CRT (50).
6. Install a calibrated 20 dB pad between Signal Generator output and ANTENNA Connector (56). Set ATTENUATOR Switch (55) to "0 dB". Verify signal is in same position ( $\pm 2$  dB) as recorded in Step 5.

## STEP

## PROCEDURE

7. Remove 20 dB pad. Set ATTENUATOR Switch (55) to "40 dB". Note and record position of signal on CRT (50).
8. Install two calibrated 20 dB pads between Signal Generator output and ANTENNA Connector (56). Set ATTENUATOR Switch (55) to "0 dB". Verify signal is in same position ( $\pm 2$  dB) as noted and recorded in Step 7.
9. Remove all test equipment from FM/AM-1500.

ANALYZER DISPERSION

1. Set FM/AM-1500 controls as follows:

| CONTROL                    | SETTING      |
|----------------------------|--------------|
| (19) GEN/REC               | "REC"        |
| (21) LCD FREQUENCY READOUT | 120.5000 MHz |
| (38) ANALY DISPR           | "1 kHz/DIV"  |
| (51) DISPLAY               | "ANALY"      |

2. Set Signal Generator to 120.5 MHz at -50 dBm.
3. Connect 50 $\Omega$  coax cable between ANTENNA Connector (56) and output of Signal Generator.
4. Change Signal Generator frequency, in 1 kHz steps, up 4 kHz from 120.5000 MHz and then down 4 kHz from 120.5000 MHz. Verify signal on CRT (50) moves 4 ( $\pm 0.3$ ) major divisions in each direction.
5. Rotate ANALY DISPR Control (38) to "2 kHz/DIV". Step Signal Generator frequency, in 1 kHz steps, up 8 kHz from 120.5000 MHz and then down 8 kHz from 120.5000 MHz. Verify signal on CRT (50) moves 4 ( $\pm 0.3$ ) major divisions in each direction.
6. For all ANALY DISPR Control (38) settings in Table 3-2, vary the limits of the Signal Generator  $\pm 4$  times ANALY DISPR Control (38) setting. Verify signal displayed on CRT (50) at each ANALY DISPR Control (38) setting that displayed signal on CRT (5) moves 4 ( $\pm 0.3$ ) major divisions in each direction.

## STEP

## PROCEDURE

| ANALY<br>DISPR<br>SETTING | LIMITS OF<br>SIGNAL GENERATOR<br>(From 120.5000 MHz) |
|---------------------------|--|
| 10 K                      | +40 K, -40 K   |
| 20 K                      | +80 K, -80 K   |
| .1 M                      | +.4 M, -.4 M   |
| .2 M                      | +.8 M, -.8 M   |
| .5 M                      | +2.0 M, -2.0 M                                       |
| 1 M                       | +4 M, -4 M   |
| 2 M                       | +8 M, -8 M   |
| 5 M                       | +20 M, -20 M   |
| 10 M                      | +40 M, -40 M   |

Table 3-2 Analyzer Dispersion Test Settings

7. Rotate ANALY DISPR Control (38) to "1 M". Set Signal Generator to 120.5000 MHz. Verify displayed signal on CRT (50) is centered ( $\pm 1$  minor division).
8. Rotate ANALY DISPR Control (38) to "2 M". Verify displayed signal on CRT (50) is centered ( $\pm 1.5$  minor divisions).
9. Set LCD FREQUENCY READOUT (21) to 500.0000 MHz. Rotate ANALY DISPR Control (38) to "FULL". Set external Signal Generator to 990.0000 MHz. Verify displayed signal on CRT (50) is displaced 9.9 ( $\pm 0.5$ ) major divisions from left side of display.

**NOTE**

If displayed signal goes off the screen, reduce Signal Generator frequency until signal is on far right of display. Minimum allowable setting of Signal Generator is 980.0000 MHz for a full scale display.

10. Disconnect all test equipment from FM/AM-1500.

TRACK

1. Set FM/AM-1500 controls as follows:

| CONTROL              | SETTING   |
|----------------------|-----------|
| (7) MODULATION       | "AM 2"    |
| (10) RF Output Level | "-40 dBm" |
| (13) PWR/OFF/BATT    | "PWR"     |
| (18) DUPLEX/SIMPLEX  | "SIMPLEX" |

## STEP

## PROCEDURE

|    | CONTROL  | SETTING      |
|----|--|--------------|
|    | (21) LCD TONE 1 READOUT  | 0400.0 Hz    |
|    | FREQUENCY READOUT  | 120.5000 MHz |
|    | (26) Tone 2 FM/OFF/AM  | "OFF"        |
|    | (28) Tone 1 FM/OFF/AM  | "AM"         |
|    | (33) TONE 1  | Fully ccw    |
|    | (38) ANALY DISPR   | "1 MHz/DIV"  |
|    | (48) dB/DIV  | "1 dB/DIV"   |
|    | (51) DISPLAY   | "TRACK"      |
| 2. | Connect 50Ω coax cable between TRANS/-40 dB DUPLEX Connector (11) and ANTENNA Connector (56).  |              |
| 3. | Adjust VERT POS Control (45) to display trace on CRT (50). Verify maximum slope of trace is $\leq 1.5$ dB.   |              |
| 4. | Rotate RF Output Level Control (10) to "-46 dBm". Verify trace on CRT moves 6 ( $\pm 1$ ) major divisions.   |              |
| 5. | Set LCD (21) to 500.0000 MHz. Set dB/DIV Switch (48) to "10 dB/DIV". Rotate ANALY DISPR Control (38) to "FULL". Rotate TONE 1 Control (33) fully cw. Verify modulation is up $\geq 6$ dB and down $\geq 20$ dB from unmodulated trace across entire bandwidth. |              |
| 6. | Rotate TONE 1 Control (33) fully ccw. Set dB/DIV Switch (48) to "1 dB/DIV". Verify maximum slope is $\leq 4$ dB for any major division and $\leq 6$ dB for entire bandwidth.   |              |
| 7. | Disconnect all test equipment from FM/AM-1500.   |              |

### 3-8 MICROPROCESSOR FUNCTIONAL BLOCK

#### 3-8-1 FRONT PANEL PERFORMANCE TEST

SPECIAL ACCESSORY  
EQUIPMENT REQ'D: None

TEST SET-UP  
DIAGRAM: None

INITIAL FM/AM-1500  
CONTROL SETTINGS:

| CONTROL           | SETTING   |
|-------------------|-----------|
| (13) PWR/OFF/BATT | "PWR"     |
| (22) VOLUME       | Midrange  |
| (23) SQUELCH      | Fully ccw |

- | STEP | PROCEDURE   |
|------|---|
| 1.   | Individually press each key on KEYBOARD (20). Verify an audible tone is generated each time a key is depressed. |
| 2.   | Verify Freq LOCK Indicator (43) and SIG Indicator (57) are illuminated.   |
| 3.   | Verify UNCAL Indicator (Vertical) (42) illuminates as VERT VERNIER Control (44) is rotated ccw out of "CAL".    |
| 4.   | Verify UNCAL Indicator (Horizontal) (8) illuminates as HORIZ VERNIER Control (3) is rotated ccw out of "CAL".   |
| 5.   | Verify an indicator illuminates at each setting of MODULATION Control (7) except "AUTO".                        |

NOTE:

One of the lights illuminates at "AUTO", but varies according to menus.

- |    |  |
|----|--|
| 6. | Depress BATT TEST Button (14) and verify internal battery voltage is +11 V to +14 V as indicated on top scale of MODULATION Meter (1). |
| 7. | Rotate DISPLAY Control (51) to "OFF". Verify CRT (50) is not illuminated.  |
| 8. | Rotate DISPLAY Control (51) to "HELP". Verify HELP Menus are displayed.  |

## STEP

## PROCEDURE

9. Press "MENU,V" sequentially on KEYBOARD (20). Verify LCD Manual Data, Memory Recall, Memory Storage and Self Test Menus are displayed.
10. Select Self Test Menu on CRT (50).
11. Press "EXEC,1,ENTER" on KEYBOARD (20). Verify LCD (21) readout displays as in Figure 3-6.

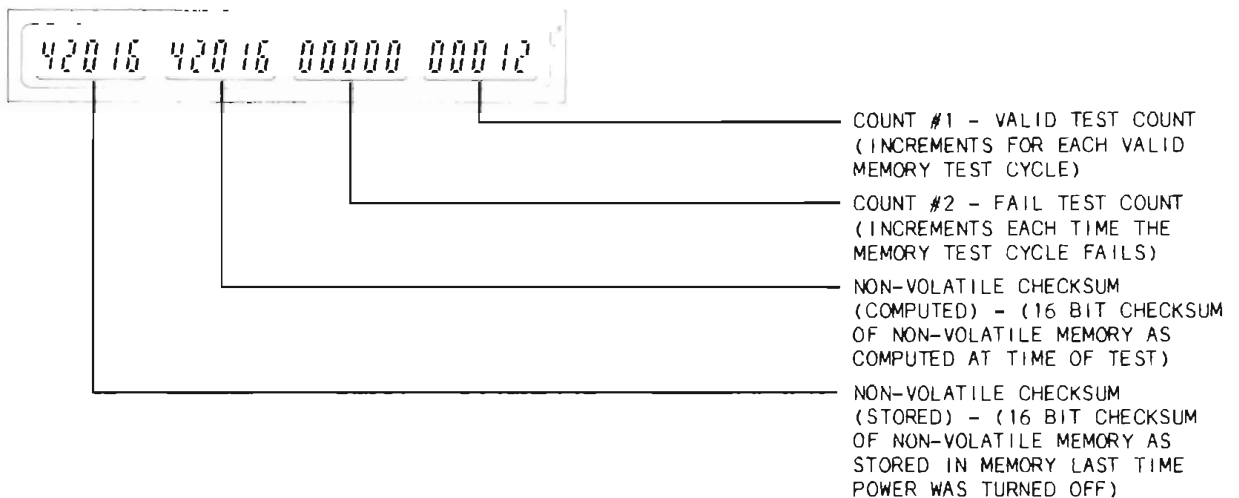


Figure 3-6 LCD Readout on Self Test 1

Press "ENTER" to exit from test.

12. Press "EXEC,2,ENTER" on KEYBOARD (20). Verify CRT (50) characters can be changed by depressing "v" or "Λ" Keys. Step completely through alphanumeric character set. Press "ENTER" to exit from test.
13. Press "EXEC,3,ENTER". Verify LCD (21) display scrolls from right to left. Press "ENTER" to exit test.
14. Press "EXEC,4,ENTER". Verify the LCD (21) flickers, the Freq LOCK Indicator (43) flashes, the LED's on the MODULATION Control (7) flash and the LCD (21) does not display an error message. Press "ENTER" to exit from test.
15. Press "EXEC,5,ENTER". Verify the cursor is displayed and, if applicable, the last stored menu. Press "ENTER" to exit from test.



## STEP

## PROCEDURE

16. Rotate DISPLAY Control (51) to "METER". Verify Meter readout is displayed on CRT (50).
17. Rotate DISPLAY Control (51) to "TONES". Press "MENU,V" sequentially and verify Tone Sequence, Digitally-Coded Squelch, Tone Sweep and DTMF Menus are displayed on CRT (50).
18. Rotate DISPLAY Control (51) to "FREQS". Press "MENU,V" sequentially and verify RF Memory, Cable Fault, RF Scan and RF Sweep Menus are displayed on CRT (50).
19. Rotate DISPLAY Control (51) to "SWEEP". Verify horizontal trace is displayed on major horizontal axis of CRT (50).
20. Rotate DISPLAY Control (51) to "TRACK". Verify noise pattern is displayed at bottom of CRT (50).
21. Rotate DISPLAY Control (51) to "ANALY". Verify noise pattern is displayed at bottom of CRT (50).
22. Rotate DISPLAY Control (51) to "SCOPE". Verify noise pattern centered about the major horizontal axis is displayed on CRT (50) that the pattern changes shape as MODULATION Control (7) is rotated.
23. Disconnect all test equipment.

### 3-8-2 DATA ENTRY PERFORMANCE TEST

#### SPECIAL ACCESSORY

EQUIPMENT REQ'D: Oscilloscope---Capable of measuring 0 to 10 VDC

#### TEST SET-UP

DIAGRAM: None

#### INITIAL FM/AM-1500

#### CONTROL SETTINGS:

| CONTROL             | SETTING   |
|---------------------|-----------|
| (7) MODULATION      | "AUTO"    |
| (13) PWR/OFF/BATT   | "PWR"     |
| (18) DUPLEX/SIMPLEX | "SIMPLEX" |
| (19) GEN/REC        | "REC"     |
| (22) VOLUME         | Midrange  |
| (51) DISPLAY        | "FREQS"   |

#### STEP

#### PROCEDURE

1. Verify IFR logo is displayed on CRT (50).
2. Press any key. Verify that IFR logo disappears from CRT (50).
3. Verify that data can be entered into LCD (21) as follows:
  - a. TONE 1 Hz - Press "T1, XXXXX, ENTER".
  - b. TONE 2 Hz - Press "T2, XXXXX, ENTER".
  - c. OFFSET MHz - Press "OFFSET, XX.XX, ENTER".
  - d. FREQUENCY MHz - Press "RF, XXX.XXXX, ENTER".
4. Set DUPLEX/SIMPLEX Switch (18) to "DUPLEX". Verify OFFSET MHz data is displayed on LCD (21).
5. Set DUPLEX/SIMPLEX Switch (18) to "SIMPLEX". Verify OFFSET MHz is 00.00 on LCD (21).
6. Select RF Memory Menu. Change data for item 1 and execute menu by pressing "EXEC, RF, 1, ENTER". Verify LCD (21) displays new menu entries.
7. Select RF Sweep Menu. Change data in item 1 as follows:

START FREQ = 100.0000 MHz  
STOP FREQ = 100.2550 MHz  
INCR. STEP = 000.0010 MHz  
INCR. STEP = 10 mS

## STEP

## PROCEDURE

8. Connect an external Oscilloscope to the X-Out Connector (59) on the rear panel of the FM/AM-1500. Execute the RF Sweep Menu by pressing "EXEC, 2nd, FSWP, 1, ., ENTER". Verify the X-Out signal steps once for each RF step and it sweeps from 0 to 10 Volts.
9. Press "2nd, STEP". Verify one forward step when "Λ" Key is pressed and one reverse step when "v" Key is pressed.
10. Verify sweep runs forward when ">" Key is pressed and sweep runs in reverse when "<" Key is pressed.
11. Select RF Scan Menu. Set FM/AM-1500 controls as follows:
 

| CONTROL        | SETTING   |
|----------------|-----------|
| (7) MODULATION | "AUTO"    |
| (19) GEN/REC   | "REC"     |
| (23) SQUELCH   | Fully ccw |
12. Connect an external antenna to ANTENNA Connector (56).
13. Enter data into the RF Scan Menu for different frequencies to be scanned. (Local radio stations are suggested for the frequencies.)
14. Execute RF Scan Menu by pressing "EXEC, 2nd, SCAN, 1-5, ., ENTER". Verify frequency dwell time (as programmed) on each received signal.
15. Rotate SQUELCH Control (23) cw to allow only the strongest signals to break squelch. Verify weak signals are skipped and strong signals still have frequency dwell time (as programmed).
16. Rotate SQUELCH Control (23) fully cw. Verify continuous scan with no frequency dwell time.
17. Press "2nd, STEP". Verify manual control works with the "Λ", "v", ">" and "<" Keys.

STEP

PROCEDURE

18. Rotate DISPLAY Control (51) to "TONES". Select Tone Sequence Menu and enter data as follows:

| ITEM<br>(1-99) | TONES<br>Hz | DEV.<br>kHz | TIME<br>mS |
|----------------|-------------|-------------|------------|
| 01             | T1 00020.0  | 05.0        | 5000       |
|                | T2 00020.0  | 05.0        |            |
| 02             | T1 00020.0  | 00.0        | 5000       |
|                | T2 00100.0  | 05.0        |            |
| 03             | T1 01000.0  | 05.0        | 5000       |
|                | T2 00100.0  | 00.0        |            |
| 04             | T1 01000.0  | 00.0        | 5000       |
|                | T2 05000.0  | 05.0        |            |
| 05             | T1 20000.0  | 05.0        | 5000       |
|                | T2 10000.0  | 00.0        |            |

19. Set FM/AM-1500 Controls as follows:

| CONTROL           | SETTING |
|-------------------|---------|
| (4) AVG PEAK/PEAK | "PEAK"  |
| (7) MODULATION    | "FM 4"  |
| (19) GEN/REC      | "GEN"   |

20. Execute Tone Sequence Menu by pressing "EXEC, 2nd, TSEQ, 1, -, 5, ENTER". Verify peak deviation on items 1 thru 4 is 5.0 kHz ( $\pm 250$  Hz) and on item 5 is 5.0 kHz ( $\pm 500$  Hz).

21. Rotate MODULATION Control (7) to "AM 2". Verify modulation switches to AM.

22. Press "2nd, STEP". Verify manual control works with the "Λ", "v", ">" and "<" Keys.

23. Select DTMF Menu. Set FM/AM-1500 Controls as follows:

| CONTROL           | SETTING |
|-------------------|---------|
| (4) AVG PEAK/PEAK | "PEAK"  |
| (7) MODULATION    | "FM 4"  |
| (19) GEN/REC      | "GEN"   |

24. Enter data into DTMF Menu as follows:

MAN. DEV = 5.0 kHz  
 DTMF MARK = 5000 mS  
 DTMF SPACE = 10 mS

| ITEM | NUMBER       | kHz  |
|------|--------------|------|
| 01   | 0123456789#* | 05.0 |

## STEP

## PROCEDURE

25. Execute DTMF Menu by pressing "EXEC, 2nd, DTMF, 1, ENTER". Verify peak deviation is 10 kHz ( $\pm 500$  Hz).
26. Rotate MODULATION Control (7) to "AM 2". Verify modulation switches to AM.
27. Press "2nd, STEP". Verify manual control works with the " $\wedge$ ", " $\vee$ ", ">" and "<" Keys.
28. Press "ENTER, 2nd, DTMF". As each key (0 thru 9, \* and #) is pressed, verify audio tone is heard and there is a deviation of 10 kHz ( $\pm 500$  Hz). Press "ENTER" to exit function.
29. Select Tone Sweep Menu. Enter data into menu as follows:

| ITEM #01       | Hz      |
|----------------|---------|
| START FREQ     | 00100.0 |
| STOP FREQ      | 00355.0 |
| INCR STEP (+)  | 00001.0 |
| INCR RATE (mS) | 0010    |

30. Execute Tone Sweep function by pressing "EXEC, 2nd, TSWP, 1, ., ENTER".
31. Using an external Oscilloscope connected to X-Out Connector (59) on rear panel of FM/AM-1500, verify X-Out signal steps once for each step and it sweeps from 0 to 10 Volts as the menu steps through its function.
32. Change the INCR STEP sign to "X 00002.0". Verify the frequency of the X-Out signal doubles.
33. Press "2nd, STEP". Verify manual control works with the " $\wedge$ ", " $\vee$ ", ">" and "<" Keys.
34. Set FM/AM-1500 Controls as follows:

| CONTROL               | SETTING      |
|-----------------------|--------------|
| (7) MODULATION        | "FM 2"       |
| (19) GEN/REC          | "GEN"        |
| (26) Tone 2 FM/OFF/AM | "OFF"        |
| (28) Tone 1 FM/OFF/AM | "OFF"        |
| (37) FREQ ERROR       | "3 AUDIO Hz" |

## STEP

## PROCEDURE

35. Select Digitally Coded Squelch Menu and enter data as follows:

GENERATE

| <u>ITEM</u> | <u>CODE #</u> | <u>POL</u> | <u>kHz DEV</u> |
|-------------|---------------|------------|----------------|
| 01          | 000           | NORM       | 0.7            |
| 02          | 006           | NORM       | 0.7            |
| 03          | 146           | NORM       | 0.7            |
| 04          | 777           | NORM       | 0.7            |

36. Execute each item by pressing "EXEC, 2nd, DCS, N (where N = 1,2,3 or 4), ENTER". Verify a valid reception code for each item.
37. Change menu's RECEIVE DATA POLARITY to INVT and verify different reception codes for each item.
38. Set GENERATE POL to INVT and verify a valid reception code for each item.
39. Press "2nd, STEP". Verify a STOP code is sent and the reception code fields are blank. Press "ENTER" to restore normal operation.
40. Press "^" and "v" Keys. Verify no change in the STOP code.
41. Press ">" and "<" Keys. Verify that the selected item code is generated as the key is depressed and that the STOP code is generated as the key is released.
42. Press "ENTER". Verify that the selected item code is generated.
43. Select "RF" Key. Verify that the STOP code is generated about 200 mS before the RF field is entered.
44. Disconnect all test equipment.

# SECTION 4 - CALIBRATION

## 4-1 GENERAL

This section contains calibration procedures for the following assemblies and systems:

| Calibration Procedure | Title                                      | Page |
|-----------------------|--|------|
| 4-2                   | Preliminary Calibration .....              | 4-5  |
| 4-3                   | Power Supply Calibration .....             | 4-7  |
| 4-4                   | Frequency Standard Calibration .....       | 4-11 |
| 4-5                   | Frequency Synthesis Functional Block ..... | 4-13 |
| 4-5-1                 | High Loop Calibration .....                | 4-13 |
| 4-5-2                 | Low Loop Calibration .....                 | 4-19 |
| 4-6                   | Receiver Functional Block .....            | 4-21 |
| 4-6-1                 | Receiver Signal Calibration .....          | 4-21 |
| 4-6-2                 | Oscilloscope Calibration .....             | 4-26 |
| 4-6-3                 | Frequency Error Calibration .....          | 4-30 |
| 4-6-4                 | Modulation Calibration .....               | 4-34 |
| 4-6-5                 | Input/Output Power Calibration .....       | 4-43 |
| 4-7                   | Generator Functional Block .....           | 4-45 |
| 4-7-1                 | RF Output Power Calibration .....          | 4-45 |
| 4-7-2                 | Duplex Offset Calibration .....            | 4-51 |
| 4-7-3                 | Dual Tone Generator Calibration .....      | 4-53 |
| 4-8                   | Spectrum Analyzer Functional Block .....   | 4-55 |
| 4-8-1                 | Spectrum Analyzer Calibration .....        | 4-55 |
| 4-9                   | Microprocessor Functional Block .....      | 4-62 |

These procedures should be performed as a result of one or more of the following conditions:

1. If, during the course of normal operation, the FM/AM-1500 or any major function thereof fails to meet the performance specifications as provided in "SECTION 3 - PERFORMANCE EVALUATION".
2. If a module is found to be defective and requires replacement (see Table 4-1, MODULE REPLACEMENT & CALIBRATION REQUIREMENTS).
3. If the recommended 12 month calibration interval is due.

### 4-1-1 SAFETY PRECAUTIONS

As with any piece of electronic equipment, extreme caution should be taken when working on "live" circuits. Certain circuits and/or components within the FM/AM-1500 contain extremely high voltage potentials, CAPABLE OF CAUSING SERIOUS BODILY INJURY OR DEATH (see following WARNINGS)! When performing the calibration procedures in this section be sure to observe the following precautions:

## **WARNING**

THE OSCILLOSCOPE CONTROL AND DEFLECTION PC BOARD AND THE CRT CARRY A VOLTAGE POTENTIAL OF MORE THAN 2000 VDC WHEN THE FM/AM-1500 IS ENERGIZED. DO NOT CONTACT THESE OR ANY ASSOCIATED COMPONENTS DURING TROUBLESHOOTING.

WHEN WORKING WITH "LIVE" CIRCUITS OF HIGH POTENTIAL, KEEP ONE HAND IN POCKET OR BEHIND BACK, TO AVOID SERIOUS SHOCK HAZARD.

REMOVE ALL JEWELRY OR OTHER COSMETIC APPAREL BEFORE PERFORMING ANY CALIBRATION PROCEDURES INVOLVING LIVE CIRCUITS.

USE ONLY INSULATED TROUBLESHOOTING TOOLS WHEN WORKING WITH LIVE CIRCUITS.

FOR ADDED INSULATION, PLACE A RUBBER BENCH MAT UNDERNEATH ALL POWERED BENCH EQUIPMENT, AND A RUBBER FLOOR MAT UNDERNEATH THE TECHNICIAN'S CHAIR.

HEED ALL WARNINGS AND CAUTIONS CONCERNING MAXIMUM VOLTAGES AND POWER INPUTS.

### 4-1-2 CALIBRATION EQUIPMENT REQUIREMENTS

Appendix E at the rear of this manual contains a comprehensive list of test equipment suitable for performing any of the procedures listed in this manual. Any other equipment meeting the specifications listed in Appendix E may be substituted in place of the recommended models.

## **NOTE**

For certain procedures in this manual, the equipment listed in Appendix E may exceed the minimum required specifications; for this reason, minimum use specifications appear with all calibration procedures, where accessory test equipment is required.

### 4-1-3 DISASSEMBLY REQUIREMENTS

To perform any of the calibration procedures contained in this section, the exterior case must be removed from the FM/AM-1500. Refer to "SECTION 6 - MECHANICAL ASSEMBLIES/PC BOARDS" for illustrations of case removal or, if required, module disassembly. In the procedures, numbers in parentheses following any adjustable port refers to the designator assigned in Figures 3-1 and 3-2 of this Manual or the Reference Designator assigned to the component on that Assembly or Schematic (see Sections 6 and 7 of this manual).



| IF THIS MODULE IS REPAIRED OR REPLACED | THEN THE FOLLOWING CALIBRATION PROCEDURES MUST BE PERFORMED |          | PRELIMINARY | POWER SUPPLY | FREQUENCY STANDARD | FREQUENCY SYNTHESIS |        |              | RECEIVE         |            |           |       |    | GENERATE |        |        |           | SPECTRUM ANALYZER | MICROPROCESSOR |           |  |
|--|---|----------|-------------|--------------|--------------------|---------------------|--------|--------------|-----------------|------------|-----------|-------|----|----------|--------|--------|-----------|-------------------|----------------|-----------|--|
|  | HIGH LOOP   | LOW LOOP |             |              |                    | RECEIVE             | SIGNAL | OSCILLOSCOPE | FREQUENCY ERROR | MODULATION | IMPEDANCE | POWER | TR | POWER    | DUPLEX | OFFSET | DUAL TONE |                   |                | GENERATOR |  |
| CLOCK DIVIDER                          | ●   |          |             |              | ●                  |                     |        |              |                 |            |           |       |    |          |        |        |           |                   |                |           |  |
| CPU/MEMORY PC BD                       | ●   |          |             |              |                    | ●                   |        |              |                 |            |           |       |    |          |        |        |           |                   |                |           |  |
| DELAY LINE                             | ●   |          |             |              |                    | ●                   |        |              |                 |            |           |       |    |          |        |        |           |                   |                |           |  |
| DEMOD AUDIO PC BD                      | ●   | ●        |             |              |                    |                     |        | ●            |                 | ●          | ●         | ●     | ●  |          |        |        |           |                   |                |           |  |
| DIODE SWITCH                           | ●   |          |             |              |                    |                     |        |              |                 |            |           |       |    |          |        |        |           |                   |                |           |  |
| DUAL TONE GENERATOR PC BD              | ●   |          |             |              |                    |                     |        |              |                 |            |           |       |    |          |        | ●      |           |                   |                |           |  |
| DUAL VCO                               | ●   |          |             |              |                    | ●                   |        | ●            |                 |            |           |       |    | ●        |        |        |           |                   |                |           |  |
| DUPLEX OFFSET                          | ●   |          |             |              |                    |                     |        |              |                 |            |           |       |    |          | ●      |        |           |                   |                |           |  |
| FM GENERATOR                           | ●   |          |             |              |                    |                     |        |              |                 | ●          |           |       |    | ●        |        |        |           |                   |                |           |  |
| GENERATE MIXER                         | ●   |          |             |              |                    |                     |        |              |                 |            |           |       |    | ●        |        |        |           | ●                 |                |           |  |
| HIGH LOOP                              | ●   |          |             |              |                    | ●                   |        |              |                 |            |           |       |    |          |        |        |           |                   |                |           |  |
| HIGH/LOW PASS FILTER                   | ●   |          |             |              |                    | ●                   |        |              |                 |            |           |       |    |          |        |        |           |                   |                |           |  |
| I/O INTERFACE PC BD                    | ●   |          |             |              |                    |                     |        | ●            |                 |            |           |       |    | ●        |        |        |           |                   |                |           |  |
| LCD/KEYBOARD                           | ●   |          |             |              |                    |                     |        |              |                 |            |           |       |    |          |        |        |           |                   |                |           |  |
| LOW PASS FILTER                        | ●   |          |             |              |                    | ●                   |        |              |                 |            |           |       |    |          |        |        |           |                   |                |           |  |
| LOW LOOP                               | ●   |          |             |              |                    |                     |        | ●            |                 |            |           |       |    |          |        |        |           |                   |                |           |  |
| LOW LOOP MIXER                         | ●   |          |             |              |                    |                     |        | ●            |                 |            |           |       |    |          |        |        |           |                   |                |           |  |
| OSC. CONT. + DEFL. PC BD               | ●   |          |             |              |                    |                     |        |              | ●               |            | ●         |       |    |          |        |        |           |                   |                |           |  |
| OUTPUT AMP                             | ●   |          |             |              |                    |                     |        |              |                 |            |           |       |    | ●        |        |        |           |                   |                |           |  |
| BUFFER AMP A or B                      | ●   |          |             |              |                    | ●                   |        |              |                 |            |           |       |    |          |        |        |           |                   |                |           |  |
| POWER SUPPLY                           | ●   | ●        |             |              |                    |                     |        |              |                 |            |           |       |    |          |        |        |           |                   |                |           |  |
| POWER TERMINATION                      | ●   |          |             |              |                    |                     |        |              |                 |            |           |       |    | ●        |        |        |           |                   |                |           |  |
| SPECTRUM ANALYZER L.O.                 | ●   |          |             |              |                    |                     |        |              |                 |            |           |       |    |          |        |        |           |                   | ●              |           |  |
| SPECTRUM ANALYZER I.F.                 | ●   |          |             |              |                    |                     |        |              |                 |            |           |       |    |          |        |        |           |                   | ●              |           |  |
| SPECTRUM ANALYZER R.F.                 | ●   |          |             |              |                    |                     |        |              |                 |            |           |       |    |          |        |        |           |                   | ●              |           |  |
| 40 V POWER SUPPLY                      | ●   | ●        |             |              |                    |                     |        |              |                 |            |           |       |    |          |        |        |           |                   |                |           |  |
| 89-90 MHz RECEIVER                     | ●   |          |             |              |                    |                     |        | ●            |                 |            |           |       |    |          |        |        |           |                   |                |           |  |
| 1300 MHz I.F. GENERATOR                | ●   |          |             |              |                    |                     |        |              |                 |            |           |       |    | ●        |        |        |           |                   |                |           |  |
| 1300 MHz I.F. RECEIVER                 | ●   |          |             |              |                    |                     |        | ●            |                 |            |           |       |    |          |        |        |           |                   |                |           |  |

Table 4-1 Module Replacement and Calibration Requirements

## 4-2 PRELIMINARY CALIBRATION

SPECIAL ACCESSORY  
EQUIPMENT REQ'D: 1 Small Slotted Screwdriver  
1 Ohmmeter—Any

FIGURE REFERENCES: None

TEST SET-UP  
DIAGRAM: N/A

| STEP | PROCEDURE |
|------|-----------|
|------|-----------|

1. Set FM/AM-1500 in the position in which it will be operating, to allow the meters to be zeroed.

**NOTE**

The meter must be zeroed after the unit is placed in the position it will be operating.

2. Set PWR/OFF/BATT Switch (13) to "OFF".
3. Adjust MODULATION Meter Mechanical Zero Adjustment (2) for an indication as close as possible to "0" on MODULATION Meter: (1). Gently tap on Meter faceplate to ensure that the needle is not sticking and that it settles to "0".
4. Adjust FREQ ERROR Mechanical Zero Adjustment (40) for an indication as close as possible to "0" on FREQ ERROR Meter (41). Gently tap on Meter faceplate to ensure that the needle is not sticking and that it settles to "0".
5. Check all knobs on front panel for the following:
  - a. Correct alignment to front panel.
  - b. Correct range stops.
  - c. Knobs are securely tightened to control shafts.
  - d. Knobs are close to front panel, but do not bind.
6. Test resistance on Power Supply as follows:

| <u>Pin # of J6003</u> | <u>Function</u> | <u>Minimum Resistance</u> |
|-----------------------|-----------------|---------------------------|
| 7                     | -12 V           | 200 $\Omega$              |
| 4 or 5                | +5 V            | 155 $\Omega$              |
| 1                     | +12 V           | 42 $\Omega$               |

**NOTE**

Ground positive (+) lead of Ohmmeter for positive voltage test points. Ground negative (-) lead of Ohmmeter for negative voltage test points.

## 4-3 POWER SUPPLY CALIBRATION

SPECIAL ACCESSORY  
EQUIPMENT REQ'D: 1 Small Slotted Screwdriver  
1 DC Voltmeter - Any  
1 DC Power Supply - Variable from +10.9 V to +12 V

FIGURE REFERENCES: Rear Panel/Power Supply Module (Figure 6-8)  
Demod Audio PC Board (Figure 6-25)

TEST SET-UP  
DIAGRAM: N/A

### **WARNING**

THE DIFFERENCE IN POTENTIAL BETWEEN THE FLOATING GROUND AND CIRCUIT OR CHASSIS GROUND CAN EXCEED 300 VOLTS PEAK. THIS POTENTIAL CAN CAUSE SERIOUS INJURY OR EVEN DEATH. ALWAYS USE AN ISOLATION TRANSFORMER AND TAKE EXTREME CARE WHEN WORKING INSIDE THE POWER SUPPLY MODULE.

### **NOTE**

FM/AM-1500 Serial Numbers 1005 thru 1425 contain DEMOD AUDIO PC Board 7010-5034-700. FM/AM-1500 Serial Numbers 1426 thru 2817 contain DEMOD AUDIO PC Board 7010-5037-300. FM/AM-1500 Serial Numbers 2818 and on contain DEMOD AUDIO PC Board 7010-5038-900. All adjustments and test points referenced in the following calibration procedure are for the 7010-5037-300 and 7010-5038-900 PC Boards only. For adjustments and test points on 7010-5034-700 PC Boards, see FM/AM-1500 Maintenance Manual Rev. 0 thru Rev. 3.

- | STEP | PROCEDURE  |
|------|--|
| 1.   | Connect AC line cord to FM/AM-1500.  |
| 2.   | Set PWR/OFF/BATT Switch (13) to "PWR".   |
| 3.   | Measure 16 VDC output at FL6002 on Power Supply. Verify voltage is +16 VDC ( $\pm 0.5$ V). If not, adjust R5741 on Power Supply PC Board #1 for correct voltage. |
| 4.   | Set PWR/OFF/BATT Switch (13) to "OFF".   |

STEP                      PROCEDURE

---

5. Disconnect battery plug J6005.

**NOTE**

Thru Serial Number 2134 (without cooling fan), both J6005 and J6004 must be disconnected.

6. Connect Battery Load Simulator to J6005.
7. Set PWR/OFF/BATT Switch (13) to "PWR".
8. Adjust load control on Battery Load Simulator for load of 0.3 Amps. Verify voltage on Battery Load Simulator is +14.5 VDC. If not, adjust R5706 on Power Supply PC Board #1 for correct voltage.
9. Depress BATT TEST Button (14) and verify that top scale on the MODULATION Meter (1) reads the same as the battery voltage in Step 8. If not, adjust R4887 on the DEMOD AUDIO PC Board.

**NOTE**

Use an extender card to make adjustment or remove CPU/MEMORY PC Board and use extender ribbon cable.

10. Adjust load on Battery Load Simulator for load of 1.3 ( $\pm 0.3$ ) Amps. Verify voltage on Battery Load Simulator is 5 VDC ( $\pm 2$  V). If not, repeat Step 8.
11. Set PWR/OFF/BATT Switch (13) to "OFF".
12. Disconnect Battery Load Simulator from J6005.
13. Set PWR/OFF/BATT Switch (13) to "OFF".
14. Connect Voltmeter between FL6005 and chassis ground. Verify voltage indication is +12 VDC ( $\pm 0.5$  V). If out of tolerance adjust R4851.
15. Connect Voltmeter between FL6006 and chassis ground. Verify voltage indication is +5.075 VDC ( $\pm 0.225$  V). If out of tolerance, return to Step 4.
16. Connect Voltmeter between FL6007 and chassis ground. Verify voltage indication is -12 VDC ( $\pm 0.5$  V). If out of tolerance, return to Step 4.
17. Use a Voltmeter to measure the output of the 40 V Power Supply at pin 3 of P5601. Verify voltage is +40.5 VDC ( $\pm 4.5$  V).
18. Set PWR/OFF/BATT Switch (13) to "OFF".
19. Connect an external +12 VDC Power Supply to Battery Plug J6005
20. Set PWR/OFF/Batt switch (13) to "BATT".

| STEP | PROCEDURE   |
|------|---|
| 21.  | Reduce external Power Supply to 10.9 VDC. Verify FM/AM-1500 shuts off at input of 10.9 VDC. If not, adjust R4919 on DEMOD AUDIO PC Board. |
| 22.  | Adjust external Power Supply to +12 VDC.  |
| 23.  | Set PWR/OFF/BATT Switch (13) to "OFF" and then back to "BATT". Verify that FM/AM-1500 shuts off in 7 to 11 minutes.                       |

## 4-4 FREQUENCY STANDARD CALIBRATION

### SPECIAL ACCESSORY

- EQUIPMENT REQ'D: 1 Frequency Counter – Capable of reading 10 MHz
- 1 10 MHz Standard – Amplitude of 2 Vp-p
- 1 Oscilloscope – Capable of 10 MHz

FIGURE REFERENCES: Oven Oscillator Assembly (Figure 6-12)

TEST SET-UP DIAGRAM: N/A

- | STEP | PROCEDURE  |
|------|--|
| 1.   | Set PWR/OFF/Batt switch to "PWR".  |
| 2.   | Connect external Frequency Counter to 10 MHz REF Connector (62) on rear of FM/AM-1500.   |
| 3.   | Adjust INT REF CAL Adjustment (17) CW and CCW while observing Frequency Counter. Verify a frequency range of at least 3 Hz ( $\pm 2$ Hz). If out of tolerance, adjust the screw for the oven oscillator to correct frequency range and leave the frequency centered at 10 MHz. |

### **NOTE**

If the optional Oven Oscillator is installed, the variable frequency will be approximately 3 Hz.

- |    |   |
|----|---|
| 4. | Observe Frequency Counter and adjust INT REF CAL Adjustment (17) for a reading of 10 MHz ( $\pm 2$ Hz).   |
| 5. | Using external Oscilloscope, connect a 10 MHz Standard (WWV is suggested) to external input of Oscilloscope and connect a coax cable between Channel A of Oscilloscope and 10 MHz REF Connector (62) on FM/AM-1500. |
| 6. | Adjust INT REF CAL Adjustment (17) on FM/AM-1500 until displayed signal on Oscilloscope "stops".  |
| 7. | Connect an external 10 MHz Standard, with amplitude of 2 Vp-p or greater, to 10 MHz REF Connector (62). Verify EXT REF Indicator (14) illuminates.  |
| 8. | Disconnect all test equipment from FM/AM-1500.  |

## 4-5 FREQUENCY SYNTHESIS FUNCTIONAL BLOCK

### 4-5-1 HIGH LOOP CALIBRATION

#### SPECIAL ACCESSORY EQUIPMENT REQ'D:

- 1 Frequency Counter – Capable of reading 1210 MHz
- 1 Spectrum Analyzer – Capable of measuring 1210 MHz
- 1 TF-30, Tune Fixture – See Appendix D
- 1 Digital Multimeter – Any
- 1 Oscilloscope – Any

#### FIGURE REFERENCES:

- FM/AM-1500 Interconnect (Figure 7-1)
- High Loop #1 and #2 Schematics (Figures 7-12 and 7-13))
- High Loop PC Boards #1 and #2 (Figure 6-13)
- Dual VCO Mechanical Assembly (Figure 6-14)

#### TEST SET-UP DIAGRAM:

N/A

#### STEP

#### PROCEDURE

1. Place FM/AM-1500 in upright position.
2. Remove two screws securing HIGH LOOP Module in module rack and pull module out, then reconnect all connectors.

#### **CAUTION**

BE CAREFUL TO INSULATE EXPOSED PC BOARDS FROM POSSIBLE SHORT-CIRCUITING.

3. Rotate ANALY DISPR Control (38) to "1 M".
4. Disconnect coax cables P601 and P602 from J601 and J602 on the HIGH/LOW PASS FILTER Module and connect P601 to P602 using a SMB to SMB connector.
5. Disconnect P3004 from DELAY LINE Module output at J3004. Disconnect P2403 from J2403 on DUAL VCO.
6. Using an SMB to SMB tee, connect an external Frequency Counter to the 1210 MHz output (J2402) of the DUAL VCO Module.
7. Set PWR/OFF/BATT Switch (13) to "PWR".

- | STEP | PROCEDURE  |
|------|--|
| 8.   | Adjust C2003 on DUAL VCO for an indicated frequency of 1210 MHz ( $\pm 1$ MHz).  |
| 9.   | Disconnect Frequency Counter.  |
| 10.  | Using an external Spectrum Analyzer, measure the RF level of the 1210 MHz LO at J2402 and at J2401 on the DUAL VCO. Verify both RF levels are +5 to +12 dBm. |
| 11.  | Disconnect Spectrum Analyzer and connect P2402 to J2402 and P2401 to J2401.  |
| 12.  | Using an external Spectrum Analyzer, measure the RF level at the output of OUTPUT BUFFER B, J6902B. Verify RF level is +5 to +12 dBm at 1210 MHz.            |
| 13.  | Disconnect Spectrum Analyzer and reconnect P6902B to J6902B.   |
| 14.  | Use Keyboard (20 to select 299.0000 MHz on LCD (21) FREQUENCY Readout.   |
| 15.  | Disconnect P2806 from J2806 on HIGH LOOP Module.   |
| 16.  | Connect TF-30 to P2406 on Dual VCO and DVM to BNC connector on TF-30 as illustrated in Figure 4-1.   |

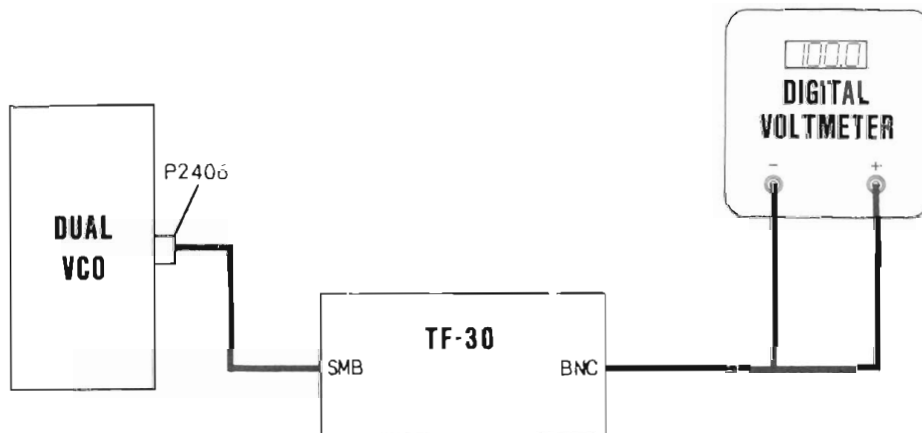


Figure 4-1 TF-30 Tune Fixture Hook-Up

17. Using an external Frequency Counter and an SMB Tee connector, measure the input frequency at J3005 on DELAY LINE Module.
18. Counter as listed below. Record voltage readings of DVM at listed frequencies.
  - a. 50 MHz = \_\_\_\_\_ Volts
  - b. 1120 MHz = \_\_\_\_\_ Volts



- | STEP | PROCEDURE   |
|------|---|
| 19.  | Adjust TF-30 for a displayed frequency on external Frequency Counter of greater than 390 MHz.   |
| 20.  | Disconnect DVM from TF-30 and connect DVM to center contact of J2806 on HIGH LOOP Module. Adjust R2373 (LOW LIMIT) on HIGH LOOP PC Board #2 for the same voltage as recorded in Step 18a.   |
| 21.  | Adjust TF-30 for a displayed frequency on external Frequency Counter of less than 380 MHz. Adjust R2372 (HIGH LIMIT) on HIGH LOOP PC Board #2 for the same voltage as recorded in Step 18b.   |
| 22.  | Disconnect TF-30 from P2406 on Dual VCO and connect P2806 to J2806 on HIGH LOOP Module. Connect P2403 to J2403 on Dual VCO. Verify that Freq LOCK Indicator (43) on front panel of FM/AM-1500 is illuminated, indicating phase-lock. If not, adjust R2341 (GAIN) on HIGH LOOP PC Board #2 until phase-lock is achieved. |

**NOTE**

The logic for control of the Freq LOCK Indicator is on the DEMOD AUDIO PC Board, as explained in Section 2 of this Manual. If adjusting R2341 does not give desired results, the HIGH LOOP Module is not necessarily faulty.

23. Using Keyboard (20) select RF 050.0000 MHz on LCD (21) FREQUENCY Readout. Rotate ANALY DISPR Control (38) to "10 K".
24. Disconnect external Frequency Counter and connect external Spectrum Analyzer in its place.
25. While observing external Spectrum Analyzer, adjust R2341 (GAIN) on HIGH LOOP PC Board #2 for a flat RF noise floor on each side of 140 MHz display. Note and record level of noise floor (The noise should be flat approximately 20-60 kHz from the center of the band, @ 50 dBc).
26. Using Keyboard (20) select RF 999.0000 MHz on LCD (21) FREQUENCY Readout.
27. Rotate ANALY DISPR Control (38) to "500 K".
28. Observe displayed signal on external Spectrum Analyzer at about 1090 MHz. Adjust R2308 (NULL) on HIGH LOOP PC Board #2 for lowest possible RF levels on 500 kHz and 1 MHz sidebands.

STEP                      PROCEDURE

---

29. Observe displayed signal on external Spectrum Analyzer for the selected frequencies. Verify noise floor level rises no more than 5 dB ( $\pm 1$  dB) above floor level noted and recorded in Step 25, on each side of RF signal. Also verify sidebands at 500 kHz and 1 MHz remain nulled.

| Selected RF<br>(Using Keyboard 20<br>for LCD (21) Display) | Displayed RF<br>(On External Spectrum<br>Analyzer) |
|--|--|
| 250.0000 MHz   | 340 MHz  |
| 450.0000 MHz   | 540 MHz  |
| 850.0000 MHz   | 940 MHz  |

30. Using Keyboard (21), select RF 460.0000 MHz on LCD (21) FREQUENCY Readout.

31. Rotate ANALY DISPR Control (38) to "1 M".

32. Connect a DVM, set to measure DC, to pin 1 of U2315A on HIGH LOOP PC Board #2.

33. Adjust R2387 on HIGH LOOP PC Board #2 so voltage on DVM switches from -10 VDC to +10 VDC as LCD (21) FREQUENCY Readout is changed from  $\geq$  approximately 440.0000 MHz to  $\leq$  approximately 480.0000 MHz.

**NOTE**

The actual switching point varies from set to set and is basically dependent on the crossover point of the HIGH/LOW PASS FILTER, which is now disconnected.

34. Disconnect fast tune line coax cable, P2805, from J2805 on HIGH LOOP Module. Verify Freq LOCK Indicator (43) on front panel blinks on and off.

35. Connect fast tune line coax cable, P2805, to J2805 on HIGH LOOP Module.

36. Connect P601 to J601 and P602 to J602 on the HIGH/LOW PASS FILTER Module.

STEP                      PROCEDURE

---

37. Verify displayed signal on external Spectrum Analyzer changes for each corresponding frequency entered on Keyboard (20 and displayed on LCD (21) FREQUENCY Readout.

| LCD (21) FREQUENCY<br>Display | External Spectrum<br>Analyzer Displayed RF |
|-------------------------------|--|
| 000.0000 MHz                  | 90.0000 MHz                                |
| 111.1111 MHz                  | 201.1111 MHz                               |
| 222.2222 MHz                  | 312.2222 MHz                               |
| 333.3333 MHz                  | 423.3333 MHz                               |
| 444.4444 MHz                  | 534.4444 MHz                               |
| 555.5555 MHz                  | 645.5555 MHz                               |
| 666.6666 MHz                  | 756.6666 MHz                               |
| 777.7777 MHz                  | 867.7777 MHz                               |
| 888.8888 MHz                  | 978.8888 MHz                               |
| 999.9999 MHz                  | 1089.9999 MHz                              |

38. Connect coax cable, P3004 to DELAY LINE Module output at J3004. Verify RF noise level 100 kHz on both sides of displayed signal drops  $\geq 5$  dB.

39. Disconnect external Spectrum Analyzer from J3005 on DELAY LINE Module and connect P3005 to J3005.

40. Using an external Spectrum Analyzer, measure output level at J2405 on DUAL VCO Module. Verify +5 to +12 dBm output level.

41. Disconnect Spectrum Analyzer from J2405 and connect P2405 to J2405.

42. Using an external Spectrum Analyzer, measure output level at J2404 on DUAL VCO Module. Verify a +5 to +12 dBm output level.

43. Disconnect Spectrum Analyzer from J2404 and connect P2404 to J2404.

44. Using an external Spectrum Analyzer, measure output level at J6902A on BUFFER AMP A. Verify a +5 to +12 dBm output level.

45. Disconnect Spectrum Analyzer from J6902A and reconnect P6902A to J6902A.

46. Set FM/AM-1500 controls as follows:

| CONTROL          | SETTING                                 |
|------------------|---|
| Keyboard (20)    | 010.0000 MHz<br>(LCD FREQUENCY Display) |
| ANALY DISPR (38) | "2 M"                                   |
| DISPLAY (51)     | "ANALY"                                 |

47. Connect an external Oscilloscope to pin 1 Test Point of U2308A on HIGH LOOP PC Board #2. Adjust R2359 (ZERO) for 0 VDC ( $\pm 1$  VDC) on Oscilloscope.

48. Using Keyboard (20) select RF 999.0000 MHz to display on LCD (21) FREQUENCY Readout.

- | STEP | PROCEDURE  |
|------|--|
| 49.  | Adjust R2330 (FREQUENCY) on HIGH LOOP PC Board #2 for 0 VDC ( $\pm 1$ VDC) on Oscilloscope.  |
| 50.  | Repeat Steps 46 thru 49, then go to Step 51.   |
| 51.  | Using Keyboard (20), select the following settings for display on LCD (21) FREQUENCY Readout and verify voltage level on external Oscilloscope is 0 VDC ( $\pm 5$ VDC) for each setting.<br>LCD (21) FREQUENCY Readout<br>900.2000 MHz<br>800.2000 MHz<br>700.2000 MHz<br>600.2000 MHz<br>500.2000 MHz<br>400.2000 MHz<br>300.2000 MHz<br>200.2000 MHz<br>100.2000 MHz<br>000.2000 MHz |
| 52.  | Disconnect all test equipment and re-install all coaxes and modules.   |

4-5-2 LOW LOOP CALIBRATION

SPECIAL ACCESSORY  
EQUIPMENT REQ'D: 1 Spectrum Analyzer – Capable of measuring  
79.3 MHz

FIGURE REFERENCES: FM/AM-1500 Interconnect (Figure 7-1)  
Low Loop Module (Figure 6-19)  
Low Loop Mixer Module (Figure 6-20)

TEST SET-UP DIAGRAM: N/A

- | STEP | PROCEDURE  |
|------|--|
| 1.   | Set PWR/OFF/BATT switch (13) to "PWR".   |
| 2.   | Use Keyboard (20) to select 000.0000 MHz on LCD (21) FREQUENCY Readout.  |
| 3.   | Using external Spectrum Analyzer, measure output level at J4001 on Low Loop Module. Verify level is -12 dBm (+2, -3 dBm) at 9.3 MHz.             |
| 4.   | Verify output frequency as displayed on external Spectrum Analyzer is equal to 9.3000 MHz minus the decimal portion of the selected RF as shown: |

| Selected LCD (21)<br>FREQUENCY Readout | Spectrum Analyzer<br>Displayed RF |
|--|-----------------------------------|
| XXX.0000 MHz                           | 9.3000 MHz (9.3000-.0000)         |
| XXX.1111 MHz                           | 9.1889 MHz (9.3000-.1111)         |
| XXX.2222 MHz                           | 9.0778 MHz (9.3000-.2222)         |
| XXX.3333 MHz                           | 8.9667 MHz (9.3000-.3333)         |
| XXX.4444 MHz                           | 8.8556 MHz (9.3000-.4444)         |
| XXX.5555 MHz                           | 8.7445 MHz (9.3000-.5555)         |
| XXX.6666 MHz                           | 8.6334 MHz (9.3000-.6666)         |
| XXX.7777 MHz                           | 8.5223 MHz (9.3000-.7777)         |
| XXX.8888 MHz                           | 8.4112 MHz (9.3000-.8888)         |
| XXX.9999 MHz                           | 8.3001 MHz (9.3000-.9999)         |

**NOTE**

"X" in the above examples is equal to any digit.

5. Disconnect Spectrum Analyzer from J4001 and connect P4001 to J4001 on LOW LOOP Module.
6. Using external Spectrum Analyzer, measure output level at J1804 on LOW LOOP MIXER Module. Verify level is +4 to +12 dBm at approximately 79.3 MHz.
7. Disconnect Spectrum Analyzer from J1804 and connect P1804 to J1804 on LOW LOOP MIXER Module.

STEP

PROCEDURE

---

8. Using external Spectrum Analyzer, measure output level at J1803 on LOW LOOP MIXER Module. Verify level is +4 to +12 dBm at approximately 79.3 MHz.
9. Disconnect all test equipment and connect all removed coax cables.

## 4-6 RECEIVER FUNCTIONAL BLOCK

### 4-6-1 RECEIVER SIGNAL CALIBRATION

#### SPECIAL ACCESSORY

- EQUIPMENT REQ'D:
- 1 Audio Distortion Analyzer - HP8903A
  - 1 Digital Voltmeter - Any
  - 1 RF Signal Generator - Capable of generating 125.5 MHz at -90 dBm
  - 1 Frequency Counter - Capable of reading 10 kHz
  - 1 10K Resistor - 5%
  - 1 1  $\mu$ F Tantalum Capacitor - 20%
  - 1 Function Generator - Capable of 120 kHz sine wave
  - 1 Oscilloscope - Any

FIGURE REFERENCES: Demod Audio PC Board (Figure 6-25)  
I/O Interface PC Board (Figure 6-39)

TEST SET-UP DIAGRAM: N/A

#### **NOTE**

FM/AM-1500 Serial Numbers 1005 thru 1425 contain DEMOD AUDIO PC Board 7010-5034-700. FM/AM-1500 Serial Numbers 1426 thru 2817 contain DEMOD AUDIO PC Board 7010-5037-300. FM/AM-1500 Serial Numbers 2818 and on contain DEMOD AUDIO PC Board 7010-5038-900. All adjustments and test points referenced in the following calibration procedure are for the 7010-5037-300 and 7010-5038-900 PC Boards only. For adjustments and test points on 7010-5034-700 PC Boards, see FM/AM-1500 Maintenance Manual Rev. 0 thru Rev. 3.

#### STEP

#### PROCEDURE

1. Connect a Digital Voltmeter (DVM) between pin 24 of J4701 on DEMOD AUDIO PC Board and pin 35 of U4337 on I/O INTERFACE PC Board.
2. Short pin 24 of J4701 to ground and adjust R4350 on I/O INTERFACE PC Board to give an indicated zero volts on DVM.
3. Remove short between pin 24 of J4701 and ground.

STEP                      PROCEDURE

---

4. Connect DVM between Test Point 1 (TP1) and ground on I/O INTERFACE PC Board. Adjust R4354 on I/O INTERFACE PC Board for an indicated +2.00 VDC on DVM.

5. Set FM/AM-1500 controls as follows:

| CONTROL        | SETTING                                       |
|----------------|---|
| (6) DEV/PWR    | "20 KHz"                                      |
| (7) MODULATION | "FM2"   |
| (20) Keyboard  | RF 120.2000 MHz<br>(on LCD FREQUENCY Readout) |
| (51) DISPLAY   | "METER"                                       |

6. Connect an RF Generator, set at 120.2 MHz at -30 dBm, to ANTENNA Connector (56).

7. Connect DVM to pin 5 of U4733 on DEMOD AUDIO PC BOARD. Verify a voltage reading on DVM of +1.6 to +2.5 VDC.

8. Adjust modulation, at a 1 kHz rate, on RF Generator until CRT Meter reads 20 kHz deviation.

9. Adjust R4950 (DEV/MOD METER CAL) on DEMOD AUDIO PC Board for an indicated 20 kHz deviation on MODULATION Meter (1).

10. Turn off modulation of RF Generator signal.

11. Rotate DEV/PWR Control (6) to "SIG". Adjust R4840 (SIG STR CAL) on DEMOD AUDIO PC Board for an indicated 99.9% on CRT Meter.

12. Disconnect RF Generator from FM/AM-1500.

13. Rotate MODULATION Control (7) to "SSB".

14. Adjust R4707 (SSB INJECTION LEVEL) on DEMOD AUDIO PC Board until needle on MODULATION Meter (1) just barely deflects to the right. At this point, slowly adjust R4707 so not to deflect needle to the right.

**NOTE**

This adjustment sets the beat frequency oscillation point of the AM Detector when in SSB.

15. Connect RF Generator, set at 120.2 MHz CW at -30 dBm, to ANTENNA Connector (56).

16. Select RF of 120.2010 MHz to display on LCD (21) FREQUENCY Readout and verify a 1 kHz demod tone is heard.

17. Connect the TONES OUTPUT Connector (27) to the SCOPE/SINAD INPUT Connector (24).



## STEP

## PROCEDURE

18. Set FM/AM-1500 controls as follows:

| CONTROL       | SETTING                        |
|---------------|--------------------------------|
| (6) DEV/PWR   | "SINAD"                        |
| (20) Keyboard | TONE 1 1000.0 Hz (LCD Display) |
| (31) TONE 2   | Fully ccw                      |
| (33) TONE 1   | Fully cw                       |
| (39) DEV/VERT | "1 V/DIV"                      |

19. Adjust R4854 (SINAD NULL No. 1) and R4857 (SINAD NULL No. 2) on DEMOD AUDIO PC Board for maximum indication on CRT Meter and MODULATION Meter (1).

**NOTE**

Maximum SINAD on MODULATION Meter (1) is full scale to the left.

20. Rotate DISPLAY Control (51) to "SCOPE". Rotate VERT VERNIER Control (44) for a display on CRT eight major divisions peak to peak.
21. Rotate TONE 1 Control (33) fully ccw. Set LCD (21) to 1800 Hz TONE 2. Rotate TONE 2 Control (31) for a display on CRT 2 major divisions peak to peak.
22. Rotate TONE 1 Control (33) fully cw. Rotate DISPLAY Control (51) to "METER".
23. Adjust R4855 (R4861) (SINAD CAL) on DEMOD AUDIO PC Board until 12 dB SINAD is indicated on CRT Meter and MODULATION Meter (1) indicates 12 dB SINAD ( $\pm 1$  dB).
24. Rotate MODULATION Control (7) to "FM 3". Connect DEMOD OUTPUT Connector (25) to external Oscilloscope.
25. Connect an external Frequency Counter to FM output connector of RF Generator. Vary the modulation rate of the RF Generator from 500 Hz to 10 kHz to verify displayed demod output level on external Oscilloscope remains constant and the CRT Meter reads within 1 count of external Frequency Counter.
26. Adjust CW output of RF Generator from -30 dBm to -50 dBm. Verify receiver of FM/AM-1500 remains quiet.

**NOTE**

Test Point 1 (TP1) is provided to allow Function Generator, connected in Steps 27 and 28, to be connected directly to the unit.

27. Solder a 10 K resistor and a 1  $\mu$ F tantalum capacitor in series. Connect the (+) end of the capacitor to pin 2 of U4733 on DEMOD AUDIO PC Board.
28. Connect a Function Generator, set to 20 kHz sine wave, to the free end of the 10 K resistor.

| STEP | PROCEDURE  |
|------|--|
| 29.  | Rotate MODULATION Control (7) to "FM 4".   |
| 30.  | Connect a coax cable between the DEMOD OUTPUT Connector (25) and the SCOPE/SINAD INPUT Connector (24). Rotate DISPLAY Control (51) to "SCOPE". Adjust output of Function Generator so displayed signal height on CRT is four major divisions (two positive, two negative). |
| 31.  | Adjust the Function Generator output frequency to 50 kHz. Verify display on CRT is less than 10% smaller than display in Step 30 (less than two minor divisions down from positive peaks).   |
| 32.  | Adjust the Function Generator output frequency to 120 kHz. Verify display on CRT is less than 30% smaller than display in Step 30 (less than six minor divisions down from positive peaks).  |
| 33.  | Rotate MODULATION Control (7) to "FM 3".   |
| 34.  | Adjust Function Generator for 10 kHz and adjust output level so displayed signal height on CRT is four major divisions (two positive, two negative).   |
| 35.  | Adjust the Function Generator output frequency to 15 kHz. Verify display on CRT is less than 10% smaller than display in Step 34 (less than two minor divisions down from positive peaks).   |
| 36.  | Adjust the Function Generator output frequency to 30 kHz. Verify display on CRT is less than 30% smaller than display in Step 34 (less than six minor divisions down from positive peaks).   |
| 37.  | Rotate MODULATION Control (7) to "FM 2".   |
| 38.  | Adjust Function Generator for 1 kHz and adjust output level so displayed signal height on CRT is four major divisions (two positive, two negative).  |
| 39.  | Adjust the Function Generator output frequency to 5 KHz. Verify display on CRT is less than 10% smaller than display in Step 38 (less than two minor divisions down from positive peaks).  |
| 40.  | Adjust the Function Generator output frequency to 10 KHz. Verify display on CRT is less than 20% smaller than display in Step 38 (less than four minor divisions down from positive peaks).  |
| 41.  | Adjust the Function Generator output frequency to 15 KHz. Verify display on CRT is less than 30% smaller than display in Step 38 (less than six minor divisions down from positive peaks).   |
| 42.  | Rotate DEV/PWR Control (6) to "120 KHz".   |

- | STEP           | PROCEDURE  |         |         |             |       |                |        |               |   |              |           |              |         |
|----------------|--|---------|---------|-------------|-------|----------------|--------|---------------|---|--------------|-----------|--------------|---------|
| 43.            | Using an external Oscilloscope and probe, verify full wave rectified signal with equal peaks is present on pin 7 of U4770 on DEMOD AUDIO PC Board.   |         |         |             |       |                |        |               |   |              |           |              |         |
| 44.            | Disconnect Function Generator from TP1.  |         |         |             |       |                |        |               |   |              |           |              |         |
| 45.            | Connect external RF Generator, set at 120.2 MHz, -50 dBm with 25 kHz deviation at 1 kHz sine wave rate, to ANTENNA Connector (56).   |         |         |             |       |                |        |               |   |              |           |              |         |
| 46.            | Rotate MODULATION Control (7) to "FM 4" and use Keyboard (20 to set 120.2000 MHz as LCD (21) FREQUENCY Readout.  |         |         |             |       |                |        |               |   |              |           |              |         |
| 47.            | Using a Distortion Meter, measure distortion out of DEMOD OUTPUT Connector (25). Verify distortion is less than 2%.  |         |         |             |       |                |        |               |   |              |           |              |         |
| 48.            | Rotate MODULATION Control (7) to "FM 1".   |         |         |             |       |                |        |               |   |              |           |              |         |
| 49.            | Reduce the deviation on RF Generator until indicated distortion on Distortion Meter is less than 2%. Verify deviation on RF Generator is $\geq 5$ kHz.   |         |         |             |       |                |        |               |   |              |           |              |         |
| 50.            | Adjust output of RF Generator to 125.5 MHz CW at -90 dBm.  |         |         |             |       |                |        |               |   |              |           |              |         |
| 51.            | Set FM/AM-1500 controls as follows:  |         |         |             |       |                |        |               |   |              |           |              |         |
|                | <table border="1"> <thead> <tr> <th>CONTROL</th> <th>SETTING</th> </tr> </thead> <tbody> <tr> <td>(6) DEV/PWR</td> <td>"SIG"</td> </tr> <tr> <td>(7) MODULATION</td> <td>"FM 1"</td> </tr> <tr> <td>(20) Keyboard</td> <td>125.5000 MHz<br/>(LCD FREQUENCY Readout)</td> </tr> <tr> <td>(23) SQUELCH</td> <td>Fully ccw</td> </tr> <tr> <td>(51) DISPLAY</td> <td>"METER"</td> </tr> </tbody> </table> | CONTROL | SETTING | (6) DEV/PWR | "SIG" | (7) MODULATION | "FM 1" | (20) Keyboard | 125.5000 MHz<br>(LCD FREQUENCY Readout) | (23) SQUELCH | Fully ccw | (51) DISPLAY | "METER" |
| CONTROL        | SETTING  |         |         |             |       |                |        |               |   |              |           |              |         |
| (6) DEV/PWR    | "SIG"  |         |         |             |       |                |        |               |   |              |           |              |         |
| (7) MODULATION | "FM 1"   |         |         |             |       |                |        |               |   |              |           |              |         |
| (20) Keyboard  | 125.5000 MHz<br>(LCD FREQUENCY Readout)  |         |         |             |       |                |        |               |   |              |           |              |         |
| (23) SQUELCH   | Fully ccw  |         |         |             |       |                |        |               |   |              |           |              |         |
| (51) DISPLAY   | "METER"  |         |         |             |       |                |        |               |   |              |           |              |         |
| 52.            | Observe SIGNAL Meter on CRT. Adjust input level on RF Generator until SIGNAL Meter reads "20". Note and record input level of RF Generator.  |         |         |             |       |                |        |               |   |              |           |              |         |
| 53.            | Set 125.5250 MHz as LCD (21) FREQUENCY Readout.  |         |         |             |       |                |        |               |   |              |           |              |         |
| 54.            | Adjust output level of RF Generator until SIGNAL Meter on CRT reads "20". Verify the output level of RF Generator is at least 25 dB greater than level noted and recorded in Step 52.  |         |         |             |       |                |        |               |   |              |           |              |         |
| 55.            | Set 125.5500 MHz as LCD (21) FREQUENCY Readout.  |         |         |             |       |                |        |               |   |              |           |              |         |
| 56.            | Adjust output level of RF Generator until SIGNAL Meter on CRT reads "20". Verify output level of RF Generator is at least 40 dB greater than level noted and recorded in Step 52.  |         |         |             |       |                |        |               |   |              |           |              |         |
| 57.            | Disconnect all test equipment.   |         |         |             |       |                |        |               |   |              |           |              |         |

## 4-6-2 OSCILLOSCOPE CALIBRATION

### SPECIAL ACCESSORY EQUIPMENT REQ'D:

- 1 Function Generator – Capable of 1 MHz sine wave and 10 KHz triangle wave
- 1 Power Supply – Variable from 0 to 40 VDC

FIGURE REFERENCES: Oscilloscope Control and Deflection PC Board (Figure 6-26)

TEST SET-UP DIAGRAM: N/A

### STEP PROCEDURE

1. Set FM/AM-1500 Controls as follows:

| CONTROL           | SETTING           |
|-------------------|-------------------|
| (3) HORIZ VERNIER | Fully cw in "CAL" |
| (13) PWR/OFF/BATT | "OFF"             |
| (44) VERT VERNIER | Fully cw in "CAL" |
| (45) VERT POS     | Centered          |
| (46) FOCUS        | Centered          |
| (47) INTENSITY    | Centered          |
| (51) DISPLAY      | "OFF"             |
| (54) HORIZ POS    | Centered          |

2. Remove Oscilloscope Control and Deflection PC Board, install extender board and install Oscilloscope Control and Deflection PC Board on extender board.

3. Set FM/AM-1500 Controls as follows:

| CONTROL       | SETTING      |
|---------------|--------------|
| (5) HORIZ     | ".01 mS/DIV" |
| (13) PWR/OFF  | "PWR"        |
| (39) DEV/VERT | "1 V/DIV"    |
| (51) DISPLAY  | "SCOPE"      |

4. Verify Oscilloscope is illuminated.
5. Adjust R9553 (INTENSITY) for desired intensity of CRT.
6. Adjust R5182 (FOCUS) for desired focus of CRT.
7. Adjust R9565 and R9566 (TRACE ROTATION) until Oscilloscope trace is parallel to the horizontal graticules on the CRT.
8. Rotate Display Control (51) to "ANALY".
9. Disconnect P5402 from Spectrum Analyzer IF Module and P4603 from Spectrum Analyzer LO Module.
10. Short pins 14 and 15 to pin 3 (Gnd) of J5102 on Oscilloscope Control and Deflection PC Board. Verify analyzer sweep disappears from CRT.

- | STEP          | PROCEDURE  |         |         |               |           |              |         |            |      |
|---------------|--|---------|---------|---------------|-----------|--------------|---------|------------|------|
| 11.           | Adjust R9559 (HORIZ CENTER) and R9561 (VERT CENTER) to center dot in exact center of CRT.  |         |         |               |           |              |         |            |      |
| 12.           | Remove short between pin 14 and pin 3 of J5102. Apply +0.800 VDC to pin 14. Adjust R5188 (VERT GAIN) to position dot on CRT at junction of major vertical graticule and uppermost horizontal graticule.  |         |         |               |           |              |         |            |      |
| 13.           | Again short pin 14 to pin 3 (Gnd) of J5102.  |         |         |               |           |              |         |            |      |
| 14.           | Remove short between pin 15 and pin 3 of J5102. Apply +2.00 VDC to pin 15 of J5102. Adjust R5193 (HORIZ GAIN) to position dot on CRT at junction of major horizontal graticule and rightmost vertical graticule.   |         |         |               |           |              |         |            |      |
| 15.           | Again short pin 15 to pin 3 (Gnd) of J5102.  |         |         |               |           |              |         |            |      |
| 16.           | Repeat sequence of Steps 10 thru 15 until no further adjustments are required to achieve desired positions of dot on CRT before continuing.  |         |         |               |           |              |         |            |      |
| 17.           | Remove shorts between pins 14 and 15 and pin 3 (Gnd) of J5102.   |         |         |               |           |              |         |            |      |
| 18.           | Set FM/AM-1500 Controls as follows:  |         |         |               |           |              |         |            |      |
|               | <table border="1"> <thead> <tr> <th>CONTROL</th> <th>SETTING</th> </tr> </thead> <tbody> <tr> <td>(39) DEV/VERT</td> <td>"1 V/DIV"</td> </tr> <tr> <td>(51) DISPLAY</td> <td>"SCOPE"</td> </tr> <tr> <td>(52) DC/AC</td> <td>"DC"</td> </tr> </tbody> </table> | CONTROL | SETTING | (39) DEV/VERT | "1 V/DIV" | (51) DISPLAY | "SCOPE" | (52) DC/AC | "DC" |
| CONTROL       | SETTING  |         |         |               |           |              |         |            |      |
| (39) DEV/VERT | "1 V/DIV"  |         |         |               |           |              |         |            |      |
| (51) DISPLAY  | "SCOPE"  |         |         |               |           |              |         |            |      |
| (52) DC/AC    | "DC"   |         |         |               |           |              |         |            |      |
| 19.           | Adjust VERT POS Control (45) and HORIZ POS Control (54) to center trace on CRT. Verify trace is 10.1 major divisions in length, centered on the major horizontal axis. Adjust R5119 (SWEEP WIDTH) for correct length of trace.                                 |         |         |               |           |              |         |            |      |
| 20.           | Using external Power Supply and BNC cable, apply +4.00 VDC to SCOPE/SINAD INPUT Connector (24). Adjust R5126 (EXTERNAL VERT GAIN) until trace is on uppermost major horizontal graticule of CRT.   |         |         |               |           |              |         |            |      |
| 21.           | Set DC/AC Switch (52) to "AC". Verify trace on CRT goes to major (center) horizontal axis.   |         |         |               |           |              |         |            |      |
| 22.           | Set DC/AC Switch (52) back to "DC". Adjust output of external Power Supply to +40 VDC and rotate DEV/VERT Control (39) to "10 V/DIV". Verify trace on CRT is on uppermost major horizontal graticule.  |         |         |               |           |              |         |            |      |
| 23.           | Rotate DEV/VERT Control (39) to ".1 V/DIV" and adjust output of external Power Supply to +0.4 VDC. Verify trace on CRT is on uppermost major horizontal graticule.   |         |         |               |           |              |         |            |      |
| 24.           | Rotate DEV/VERT Control (39) to ".01 V/DIV" and adjust output of external Power Supply to +0.04 VDC. Verify trace on CRT is on uppermost major horizontal graticule.   |         |         |               |           |              |         |            |      |

| STEP | PROCEDURE  |
|------|--|
| 25.  | Rotate DEV/VERT Control (39) to "1 V/DIV" and rotate HORIZ Control (5) to ".1 mS/DIV".   |
| 26.  | Disconnect external Power Supply from FM/AM-1500.  |
| 27.  | Using external Function Generator and 50 BNC coax cable, inject a 1 kHz sine wave signal into SCOPE/SINAD INPUT Connector (24). Adjust Signal Generator output power until trace on CRT is six major divisions peak-to-peak. |
| 28.  | Adjust output of external Function Generator to a 1 MHz sine wave. Verify trace on CRT is 4.2 to 7.8 major divisions in amplitude. If not, adjust C5115 for correct amplitude.   |
| 29.  | Adjust output of external Function Generator back to 1 kHz sine wave. Rotate VERT VERNIER Control (44) ccw and verify UNCAL Indicator (Vertical) (42) illuminates and that display on CRT does not oscillate.                |
| 30.  | Repeat Steps 27 and 28 and then rotate VERT VERNIER Control (44) fully cw to "CAL".  |
| 31.  | Rotate HORIZ VERNIER Control (3) fully ccw and verify display on CRT increases in frequency.   |
| 32.  | Rotate HORIZ VERNIER Control (3) fully cw to "CAL".  |
| 33.  | Adjust output of external Function Generator to a 1 kHz triangle wave. Adjust R5116 (SWEEP RATE) for five major horizontal divisions between positive and negative peaks of display.   |
| 34.  | Adjust output of external Function Generator to a 10 kHz triangle wave. Rotate HORIZ Control (5) to ".01 mS/DIV". Verify one complete cycle ( $\pm 20\%$ ) is displayed on CRT.  |
| 35.  | Adjust output of external Function Generator to a 1 kHz triangle wave. Rotate HORIZ Control (5) to ".1 mS/DIV". Verify one complete cycle ( $\pm 20\%$ ) is displayed on CRT.  |
| 36.  | Adjust output of external Function Generator to a 100 Hz triangle wave. Rotate HORIZ Control (5) to "1.0 mS/DIV". Verify one complete cycle ( $\pm 20\%$ ) is displayed on CRT.  |
| 37.  | Adjust output of external Function Generator to a 10 Hz triangle wave. Rotate HORIZ Control (5) to "10 mS/DIV". Verify one complete cycle ( $\pm 20\%$ ) is displayed on CRT (50).   |
| 38.  | Rotate HORIZ Control (5) to "TONES". Set LCD (21) to 10 Hz TONE 1. Rotate TONE 1 Control (33) cw and verify Lissajous pattern is available on CRT (50).  |
| 39.  | Rotate DISPLAY Control (51) to "TONES" and adjust R9556 (BRIGHTNESS) for approximately the same brightness as was displayed on CRT (50) in "SCOPE".  |

| STEP | PROCEDURE  |
|------|--|
| 40.  | Observe the size of the menu raster displayed on CRT and adjust R5161 (VERTICAL RASTER) and R5169 (HORIZ RASTER) until display touches the bottom and the right sides of the CRT (50). |
| 41.  | Observe the display on CRT and adjust R9528 (ASTIGMATISM) for best focus across the screen.  |
| 42.  | Remove Oscilloscope Control and Deflection PC Board from extender board, remove extender board from FM/AM-1500 and install Oscilloscope Control and Deflection PC Board in FM/AM-1500. |
| 43.  | Connect P5402 to Spectrum Analyzer IF Module and P4603 to Spectrum Analyzer LO Module.   |

### 4-6-3 FREQUENCY ERROR CALIBRATION

#### SPECIAL ACCESSORY

- EQUIPMENT REQ'D: 1 RF Signal Generator – Capable of 130 MHz at -110 dBm  
1 Oscilloscope – Any

FIGURE REFERENCES: Demod Audio PC Board (Figure 6-25)

TEST SET-UP DIAGRAM: N/A

#### NOTE

FM/AM-1500 Serial Numbers 1005 thru 1425 contain DEMOD AUDIO PC Board 7010-5034-700. FM/AM-1500 Serial Numbers 1426 thru 2817 contain DEMOD AUDIO PC Board 7010-5037-300. FM/AM-1500 Serial Numbers 2818 and on contain DEMOD AUDIO PC Board 7010-5038-900. All adjustments and test points referenced in the following calibration procedure are for the 7010-5037-300 and 7010-5038-900 PC Boards only. For adjustments and test points on 7010-5034-700 PC Boards, see FM/AM-1500 Maintenance Manual Rev. 0 thru Rev. 3.

#### STEP

#### PROCEDURE

1. Set FM/AM-1500 Controls as follows:

#### CONTROL

#### SETTING

- |                 |   |
|-----------------|---|
| (7) MODULATION  | "FM2"                                   |
| (19) GEN/REC    | "REC"                                   |
| (20) Keyboard   | 010.0000 MHz<br>(LCD FREQUENCY Readout) |
| (37) FREQ ERROR | "300 Hz"                                |

2. Connect a BNC/BNC coax between 10 MHz REF Connector (62) and ANTENNA Connector (56). Adjust R4790 (FREQ ERROR ZERO) on DEMOD AUDIO PC Board for a zero indication on FREQ ERROR Meter (41).

3. Set FM/AM-1500 Controls as follows:

#### CONTROL

#### SETTING

- |                 |   |
|-----------------|---|
| (20) Keyboard   | 010.0100 MHz<br>(LCD FREQUENCY Readout) |
| (37) FREQ ERROR | "10 kHz"                                |

4. Adjust R4838 (FREQ METER CAL) on DEMOD AUDIO PC Board for an indication of -1.0 on FREQ ERROR Meter (41).
5. Set RF 010.0030 MHz on LCD (21) FREQUENCY Readout. Rotate FREQ ERROR Control (37) to "3 kHz". Verify FREQ ERROR Meter (41) reads -3.0.



STEP                      PROCEDURE

---

- 6. Set RF 010.0010 MHz on LCD (21) FREQUENCY Readout. Rotate FREQ ERROR Control (37) to "1 kHz". Verify FREQ ERROR Meter (41) reads -1.0.
- 7. Set RF 010.0003 MHz on LCD (21) FREQUENCY Readout. Rotate FREQ ERROR Control (37) to "300 Hz". Verify FREQ ERROR Meter (41) reads -3.0.
- 8. Set RF 010.0001 MHz on LCD (21) FREQUENCY Readout. Rotate FREQ ERROR Control (37) to "300 Hz". Verify FREQ ERROR Meter (41) reads -1.0.
- 9. Rotate FREQ ERROR Control to "30 Hz". Verify needle on FREQ ERROR Meter (41) is pegged.

10. Set FM/AM-1500 Controls as follows:

| CONTROL         | SETTING      |
|-----------------|--------------|
| (7) MODULATION  | "AM2"        |
| (21) LCD        | 120.2000 MHz |
| (37) FREQ ERROR | "10 kHz"     |

- 11. Connect an external RF Generator set at 120.2 MHz, CW, to ANTENNA Connector (56). Adjust R4798 (AM FLYWHEEL VOLTAGE) on DEMOD AUDIO PC Board until needle on FREQ ERROR Meter (41) is centered.
- 12. Set external RF Generator to 150% AM.
- 13. Connect an external Oscilloscope to pin 6 of U4717 on DEMOD AUDIO PC Board. Adjust R4744 (AM FLYWHEEL OFFSET) on DEMOD AUDIO PC Board for a null signal on external Oscilloscope.
- 14. Set external RF Generator for a CW output.
- 15. Connect external Oscilloscope to pin 3 of U4717 on DEMOD AUDIO PC Board. Verify approximately +6 V on Oscilloscope. Note and record voltage.
- 16. Connect external Oscilloscope to pin 6 of U4717. Adjust R4798 (AM FLYWHEEL VOLTAGE) on DEMOD AUDIO PC Board for same voltage as noted and recorded in Step 15.

**NOTE**

If R4798 does not allow desired voltage to be achieved, adjust it as close as possible and then repeat Steps 12 thru 16.

- 17. Set external RF Generator to 150% AM.
- 18. Connect external Oscilloscope to pin 6 of U4717. Adjust R4744 (AM FLYWHEEL OFFSET) on DEMOD AUDIO PC Board for a null signal on Oscilloscope.
- 19. Disconnect RF Generator from FM/AM-1500.

## STEP

## PROCEDURE

20. Set FM/AM-1500 Controls as follows:

| CONTROL               | SETTING  |
|-----------------------|--|
| (7) MODULATION        | "FM3"  |
| (19) GEN/REC          | "REC"  |
| (20) Keyboard         | 1000.0 Hz LCD TONE 1 Readout<br>1000.0 Hz LCD TONE 2 Readout |
| (26) Tone 2 FM/OFF/AM | "OFF"  |
| (28) Tone 1 FM/OFF/AM | "OFF"  |
| (37) FREQ ERROR       | "300 AUDIO Hz"   |
| (51) DISPLAY          | "METER"  |

21. Adjust TONE 2 Control (31) for a 450 Hz deviation indication on MODULATION Meter (1).
22. Connect an external Oscilloscope to pin 1 of U4738 on DEMOD AUDIO PC Board.
23. Using TONE 2 Control (31), vary indicated deviation on MODULATION Meter (1) from 450 Hz to maximum indication and back to 450 Hz. Verify AGC level on Oscilloscope is constant over entire range.
24. Use Keyboard (20) to set TONE 1 LCD (21) Readout to 0710.0 Hz and TONE 2 LCD (21) Readout to 0410.0 Hz. Verify FREQ ERROR Meter (41) reads -3.0 and CRT Meter indicates 410 Hz.
25. Use Keyboard (20) to set TONE 1 LCD (21) Readout to 0410.0 Hz and TONE 2 LCD (21) Readout to 0710.0 Hz. Verify FREQ ERROR Meter (41) reads +3.0 and CRT (50) Meter indicates 710 Hz.
26. Use Keyboard (20) to set TONE 1 LCD (21) Readout to 0409.0 Hz and TONE 2 LCD (21) Readout to 0709.0 Hz. Verify FREQ ERROR Meter (41) and CRT (50) Meter DO NOT read +3.0 and 709 Hz, respectively.
27. Rotate FREQ ERROR Control (37) to "300 Hz" and verify CRT (50) Meter reads 709 Hz.
28. Rotate FREQ ERROR Control (37) to "30 AUDIO Hz" and set LCD (21) to 0120.0 Hz TONE 1 and 0150.0 Hz TONE 2. Verify FREQ ERROR Meter (41) reads +3.0 and CRT (50) reads 150 Hz.
29. Rotate FREQ ERROR Control (37) to "3 AUDIO Hz" and set LCD (21) to 9997.0 Hz TONE 1 and 10000 Hz TONE 2. Rotate TONE 2 Control (31) for an indication of 1000 Hz deviation on MODULATION Meter (1). Verify FREQ ERROR Meter reads +3.0 and CRT (50) reads 10,000 Hz.
30. Connect external Oscilloscope to pin 9 of P4702 on DEMOD AUDIO PC Board.

| STEP | PROCEDURE |
|------|-----------|
|------|-----------|

31. Set FM/AM-1500 Controls as follows:

| CONTROL             | SETTING                  |
|---------------------|--------------------------|
| (7) MODULATION      | "FM2"                    |
| (18) DUPLEX/SIMPLEX | "SIMPLEX"                |
| (19) GEN/REC        | "GEN"                    |
| (20) Keyboard       | 1000.0 Hz TONE 1 Readout |

32. Rotate TONE 1 Control (33) to obtain a 150 Hz deviation indication on MODULATION Meter (1).

33. Rotate TONE 1 Control (33) slowly until a square wave occurs on external Oscilloscope. Verify deviation indication is  $\leq 450$  Hz on MODULATION Meter (1).

34. Set FM/AM-1500 Controls as follows:

| CONTROL         | SETTING                                    |
|-----------------|--|
| (7) MODULATION  | "FM1"                                      |
| (19) GEN/REC    | "REC"                                      |
| (20) Keyboard   | RF 850.5000 MHz<br>(LCD FREQUENCY Readout) |
| (23) SQUELCH    | Fully ccw                                  |
| (37) FREQ ERROR | "300 Hz"                                   |

35. Connect external Signal Generator to ANTENNA Connector (56). Set RF Generator to 850.5000 MHz at -90 dBm.

36. Observe the FREQ ERROR Meter (41) while slowly lowering the RF level output of external RF Generator. Verify RF Generator output is -101 dBm or less when FREQ ERROR Meter (41) indicates 100 Hz.

37. Disconnect all test equipment.

4-6-4 MODULATION CALIBRATION

SPECIAL ACCESSORY

- EQUIPMENT REQ'D:
- 1 RF Generator – Capable of 130 MHz at -30 dBm
  - 1 Boonton Modulation Meter – Capable of reading 15 kHz deviation; selectable filters
  - 1 Digital Voltmeter – Any
  - 1 Function Generator – Capable of 8 Vp-p Sine Wave.

FIGURE REFERENCES: Demod Audio PC Board (Figure 6-25)  
 Oscilloscope Control and Deflection PC Board (Figure 6-26)

TEST SET-UP DIAGRAM: N/A

**NOTE**

FM/AM-1500 Serial Numbers 1005 thru 1425 contain DEMOD AUDIO PC Board 7010-5034-700. FM/AM-1500 Serial Numbers 1426 thru 2817 contain DEMOD AUDIO PC Board 7010-5037-300. FM/AM-1500 Serial Numbers 2818 and on contain DEMOD AUDIO PC Board 7010-5038-900. All adjustments and test points referenced in the following calibration procedure are for the 7010-5037-300 and 7010-5038-900 PC Boards only. For adjustments and test points on 7010-5034-700 PC Boards, see FM/AM-1500 Maintenance Manual Rev. 0 thru Rev. 3.

STEP PROCEDURE

1. Set FM/AM-1500 controls as follows:

| CONTROL           | SETTING                                    |
|-------------------|--|
| (4) AVG PEAK/PEAK | PEAK                                       |
| (6) DEV/PWR       | 2 KHz                                      |
| (7) MODULATION    | FM2  |
| (19) GEN/REC      | REC  |
| (20) Keyboard     | RF 120.2000 MHz<br>(LCD FREQUENCY Readout) |

2. Set the following controls on the Modulation Meter:

| CONTROL          | SETTING |
|------------------|---------|
| High-Pass Filter | 300 Hz  |
| Low-Pass Filter  | 15 kHz  |

STEP                      PROCEDURE

---

3. Set the following controls on the RF Generator:

| CONTROL   | SETTING   |
|-----------|-----------|
| FREQUENCY | 120.2 kHz |
| AMPLITUDE | -30 dBm   |
| RATE      | 1 kHz     |

4. Connect the RF Generator to a BOONTON Modulation Meter and adjust level to 10 kHz deviation at 1 kHz rate as indicated on Modulation Meter.

5. Disconnect RF Generator from Modulation Meter and connect output of RF Generator to ANTENNA Connector (56).

6. Connect a Digital Voltmeter to DEMOD OUTPUT Connector (25).

7. Adjust R4803 (FM DEMOD LEVEL) on DEMOD AUDIO PC Board to give an indicated 0.566 VRMS on Digital Voltmeter.

8. Set output modulation of RF Generator to CW.

9. Set the following FM/AM-1500 Controls:

| CONTROL        | SETTING |
|----------------|---------|
| (6) DEV/PWR    | 60 kHz  |
| (7) MODULATION | FM2     |

10. Connect Digital Voltmeter to pin 7 of U4785.

11. Adjust R4912 (FM 2 ZERO) on DEMOD AUDIO PC Bd to give an indicated zero voltage reading on Digital Voltmeter.

12. Connect Digital Voltmeter to pin 1 of U4773.

13. Adjust R4897 (PEAK DETECTOR ZERO) on DEMOD AUDIO PC Board for an indicated zero voltage reading on Digital Voltmeter.

14. Set the following controls on the BOONTON Modulation Meter:

| CONTROL          | SETTING         |
|------------------|-----------------|
| FUNCTION         | kHz - DEVIATION |
| HIGH-PASS FILTER | 10 kHz          |
| LOW-PASS FILTER  | 3 kHz           |
| RANGE            | 10              |
| PEAK             | PK - PK/2       |
| TUNING           | Auto            |

15. Select -10 dBm CW on RF Generator.

16. Connect RF Generator to BOONTON Modulation Meter and note the Residual FM of the Modulation.

RESIDUAL FM: \_\_\_\_\_

STEP                   PROCEDURE

---

17. Select the following FM/AM-1500 Controls:

| CONTROL                          | SETTING   |
|----------------------------------|-----------|
| (4) AVG PEAK/PEAK Switch         | Peak      |
| (7) MODULATION                   | FM1       |
| (39) DEV/VERT Control            | 2 kHz/DEV |
| (55) ATTENUATOR SWITCH (Antenna) | 40 dB     |

18. Select "Meter" on DISPLAY (51) Control.

19. Verify Residual FM on CRT (50) is same as on BOONTON Modulation Meter (Step 16). Adjust R5009 (FM 1 ZERO) on DEMOD AUDIO PC Board, as needed.

20. Set Modulation Control (7) to "FM 2".

21. Verify Modulation Meter (1) measures same Residual FM as BOONTON Modulation Meter (Step 16). Adjust R5012 (FM 2 ZERO) on DEMOD AUDIO PC Board, as needed.

22. Set Low-pass filter on BOONTON Modulation Meter to 15 kHz.

23. Connect RF Generator to BOONTON Modulation Meter and note Residual FM displayed on Modulation Meter.

RESIDUAL FM: \_\_\_\_\_

24. Set Modulation Control (7) to "FM 3".

25. Connect RF Generator to Antenna Connector (56).

26. Verify CRT (50) measures same Residual FM as BOONTON Modulation Meter (Step 23). Adjust R5010 (FM 3 ZERO) on DEMOD AUDIO PC Board, as needed.

27. Set Modulation Control (7) to "FM 4".

28. Set Low-pass filter on BOONTON Modulation Meter to 120 kHz.

29. Connect RF Generator to BOONTON Modulation Meter and note the Residual FM displayed on the Modulation Meter.

RESIDUAL FM: \_\_\_\_\_

30. Connect RF Generator to Antenna Connector (56) of the FM/AM-1500.

31. Verify CRT (50) measures same Residual FM as Boonton Modulation Meter (Step 29). Adjust R5011 (FM 4 ZERO) on DEMOD AUDIO PC Board, as needed.

32. Set the following BOONTON Modulation Meter controls:

| CONTROL          | SETTING |
|------------------|---------|
| HIGH-PASS FILTER | 300 Hz  |
| LOW-PASS FILTER  | 3 kHz   |

STEP                   PROCEDURE

---

33. Set the following FM/AM-1500 controls:

| CONTROL                  | SETTING  |
|--------------------------|----------|
| (4) AVG PEAK/PEAK Switch | AVG-PEAK |
| (6) DEV/PWR Control      | 2 kHz    |
| (7) MODULATION Control   | FM 2     |
| (51) DISPLAY Control     | Meter    |

34. Connect RF Generator to ANTENNA Connector (56) and note Residual FM.

RESIDUAL FM: \_\_\_\_\_

35. Set AVG PEAK/PEAK Switch (4) to "PEAK" and note Residual FM shown on CRT display (50).

RESIDUAL FM: \_\_\_\_\_

36. Connect RF Generator to BOONTON Modulation Meter and note Residual FM.

RESIDUAL FM: \_\_\_\_\_

37. Adjust RF Generator to 5 kHz at 1 kHz rate.

**NOTE**

This signal must be adjusted to include the Residual FM noted in Step 36.

38. Connect RF Generator to ANTENNA Connector (56).

39. Set DEV/PWR Control (6) to "6 kHz DEV".

40. Adjust R4913 (PEAK DEV), as needed, to attain 5 kHz on CRT (50) and adjust R4950 to attain 5 kHz on MODULATION Meter (1).

**NOTE**

This signal must be adjusted to include the Residual FM noted in Step 36 (i.e., 5 kHz + RESIDUAL in Step 36).

41. Set AVG PEAK/PEAK Switch (4) to "AVG PEAK".

42. Adjust R4914 (AVG DEV) to 5 kHz Deviation.

**NOTE**

This signal must be adjusted to include the Residual FM noted in Step 36 (i.e., 5 kHz + RESIDUAL in Step 36).

43. Repeat Steps 14 through 42 to fine tune the set, before proceeding.

STEP                      PROCEDURE

---

44. Set the following FM/AM-1500 Controls:

| CONTROL              | SETTING       |
|----------------------|---------------|
| (5) HORIZ Control    | .1 ms/DIV     |
| (6) DEV/PWR          | 2 kHz/DIV DEV |
| (51) DISPLAY Control | SCOPE         |

45. Adjust R4873 (DEV CAL) pot on Oscilloscope Control and Deflection PC Board, as needed, to read five divisions peak to peak, centering the scope trace peaks on the CRT.

46. Set the following controls on the BOONTON Modulation Meter.

| CONTROL          | SETTING |
|------------------|---------|
| HIGH-PASS FILTER | 300 Hz  |
| LOW-PASS FILTER  | 3 kHz   |

47. Connect RF Generator to BOONTON Modulation Meter and note Residual FM.

RESIDUAL FM: \_\_\_\_\_

48. Select 1 kHz tone on RF Generator.

49. Adjust FM deviation on RF Generator to 1 kHz ( $\pm 1$  kHz).

**NOTE**

This signal must be adjusted to include the Residual FM noted in Step 36.

50. Set the following FM/AM-1500 controls:

| CONTROL                  | SETTING   |
|--------------------------|-----------|
| (4) AVG PEAK/PEAK Switch | PEAK/DEV  |
| (6) DEV/PWR Control      | 2 kHz DEV |
| (7) MODULATION Control   | FM2       |

51. Connect RF Generator to ANTENNA Connector (56).

52. Set the following BOONTON Modulation Meter Controls:

| CONTROL          | SETTING |
|------------------|---------|
| HIGH-PASS FILTER | 3 kHz   |
| LOW-PASS FILTER  | 15 kHz  |

53. Set the following RF Generator controls:

| CONTROL    | SETTING                |
|------------|------------------------|
| MODULATION | NONE (CONTINUOUS WAVE) |
| AMPLITUDE  | -10 dBm                |

54. Connect RF Generator to BOONTON Modulation Meter and note Residual FM.

RESIDUAL FM: \_\_\_\_\_



STEP                      PROCEDURE

---

55. Adjust RF Generator for 2 kHz deviation at 6 kHz rate.

**NOTE**

This signal must be adjusted to include the Residual FM noted in Step 54.

56. Set the following FM/AM-1500 Controls:

| CONTROL                  | SETTING  |
|--------------------------|----------|
| (4) AVG PEAK/PEAK Switch | PEAK/DEV |
| (6) DEV/PWR Control      | 6 kHz    |

57. Connect RF Generator to ANTENNA Connector (56).

58. Adjust R4768 (6 kHz DEV), as needed, for 2 kHz deviation.

**NOTE**

This signal must be adjusted to include the Residual FM noted in Step 54.

59. Set the following controls on the BOONTON Modulation Meter.

| CONTROL          | SETTING |
|------------------|---------|
| LOW-PASS FILTER  | 120 kHz |
| HIGH-PASS FILTER | 3 kHz   |

60. Set the RF Generator modulation to CW.

61. Connect the RF Generator to the BOONTON Modulation Meter and note the Residual FM

RESIDUAL FM: \_\_\_\_\_

62. Adjust the RF Generator for 8 kHz deviation at 10 kHz rate.

**NOTE**

This signal must be adjusted to include the Residual FM noted in Step 61.

63. Set the following FM/AM-1500 controls:

| CONTROL                | SETTING    |
|------------------------|------------|
| (6) DEV/PWR Control    | 20 kHz DEV |
| (7) MODULATION Control | FM 3       |

64. Connect RF Generator to ANTENNA Connector (56).

65. Adjust R4778 (10 kHz ADJ), as needed, for 8 kHz deviation.

**NOTE**

This signal must be adjusted to include the Residual FM noted in Step 16.

STEP                   PROCEDURE

---

66. Set the following FM/AM-1500 controls:

| CONTROL                | SETTING            |
|------------------------|--------------------|
| (7) MODULATION Control | FM 2, FM 3 or FM 4 |
| (51) DISPLAY Control   | SCOPE              |
| (39) DEV/Vert Control  | 20 kHz/DIV         |

67. Set RF Generator to 60 kHz Deviation at 1 kHz Rate.

68. Connect RF Generator to ANTENNA Connector (56).

69. Verify no clipping of peaks (either positively or negatively) on CRT display (50).

70. Set output of RF Generator to CW.

71. Set FM/AM-1500 Controls as follows:

| CONTROL           | SETTING |
|-------------------|---------|
| (4) AVG PEAK/PEAK | PEAK    |
| (6) DEV/PWR       | 2%      |
| (7) MODULATION    | AM 2    |
| (51) DISPLAY      | METER   |

72. Adjust R4918 (AM ZERO) on DEMOD AUDIO PC Board an indication of zero on CRT (50) and on MODULATION Meter (1).

73. Set RF Generator to 50% AM with a 1 kHz tone.

74. Rotate DEV PWR Control (6) to 6%. Set AVG PEAK/PEAK Switch to PEAK. Adjust R4810 (AM% CAL) on DEMOD AUDIO PC Board for an indicated 50% on CRT (50) and on MODULATION Meter (1).

75. Set FM/AM-1500 Controls as follows:

| CONTROL        | SETTING |
|----------------|---------|
| (6) DEV/PWR    | 20 kHz  |
| (7) MODULATION | FM2     |
| (19) GEN/REC   | GEN     |
| (51) DISPLAY   | TONES   |

76. Select TONE SEQUENCE Menu on CRT (50) and enter following data as Item 01:

|    |        |      |      |
|----|--------|------|------|
| T1 | 1000.0 | 10.0 | 9000 |
| T2 | 0000.0 | 0.0  |      |

Then press "EXEC, 2ND, T.SEQ, 1, ., ENTER".

77. Adjust R3333 in FM Generator Module until CRT (50) reads 10 kHz deviation.

78. Connect a microphone to MIC Connector (34). While talking into microphone, adjust R4932 (FM MIKE LEVEL) on DEMOD AUDIO PC Board for maximum 5 kHz deviation on MODULATION Meter (1).

STEP                    PROCEDURE

---

79. Set FM/AM-1500 Controls as follows:

| CONTROL        | SETTING |
|----------------|---------|
| (6) DEV/PWR    | 6%      |
| (7) MODULATION | AM 2    |
| (19) GEN/REC   | GEN     |

80. Select TONE SEQUENCE Menu on CRT (50) and enter following data as Item 01:

|    |        |     |      |
|----|--------|-----|------|
| T1 | 1000.0 | 5.0 | 9000 |
| T2 | 0000.0 | 0.0 |      |

81. Press "EXEC, 2ND, T.SEQ, 1, ., ENTER"

82. Adjust R7983 (AM % MOD) on DEMOD AUDIO PC Board so MODULATION Meter (1) reads 50% modulation.

83. While keying microphone, adjust R4933 (AM MIKE LEVEL) on DEMOD AUDIO PC Board for maximum 95% AM on MODULATION Meter (1).

84. Rotate MODULATION Control (7) to FM 2.

85. Check the pins on the EXT ACC Connector (29) (see Figure 3-4):

| Pin # | Output/Input  | Method         |
|-------|---------------|----------------|
| 1     | +12 V out     | Voltage check  |
| 2     | -12 V out     | Voltage check  |
| 3     | +5 V out      | Voltage check  |
| 4     | Tone Gen out  | Signal check   |
| 5     | Ext FM Mod in | Signal check   |
| 6     | Tone Key in   | Ground to test |
| 7     | Mike Key in   | Ground to test |
| 8     | Demod out     | Signal check   |
| 9     | Power Ground  | -----          |
| 10    | Signal Ground | -----          |

86. Connect a Function Generator into EXT FM MOD Connector (32).

87. Set FM/AM-1500 Controls as follows:

| CONTROL               | SETTING |
|-----------------------|---------|
| (6) DEV/PWR           | 20 kHz  |
| (7) MODULATION        | FM 2    |
| (19) GEN/REC          | GEN     |
| (26) Tone 2 FM/OFF/AM | OFF     |
| (28) Tone 1 FM/OFF/AM | OFF     |

88. Adjust Function Generator so 15 kHz of deviation is indicated on MODULATION Meter (1). Verify output signal of Function Generator is between 4 and 8 Vp-p sine wave.

89. Connect Function Generator to EXT AM MOD Connector (30).

90. Rotate MODULATION Control (7) to AM 1.

STEP                    PROCEDURE

---

91. Adjust Function Generator so 90% AM is indicated on MODULATION Meter (1). Verify output signal of Function Generator is between 2 and 4 Vp-p sine wave.

92. Set FM/AM-1500 Controls as follows:

| CONTROL         | SETTING    |
|-----------------|------------|
| (6) DEV/PWR     | 6 kHz      |
| (7) MODULATION  | FM 2       |
| (19) GEN/REC    | GEN        |
| (37) FREQ ERROR | 3 AUDIO Hz |

93. Select DCS Menu on CRT (50) and enter following data into Items 1 thru 4:

|    |     |      |     |
|----|-----|------|-----|
| 01 | 000 | NORM | 0.5 |
| 02 | 006 | NORM | 0.5 |
| 03 | 146 | NORM | 0.5 |
| 04 | 777 | NORM | 0.5 |

94. For each item in previous step, push:

"EXEC, 2ND, DCS, (ITEM #), ENTER"

Verify valid reception code for each item while speaking into a keyed microphone.

95. Disconnect all test equipment.

#### 4-6-5 INPUT/OUTPUT POWER CALIBRATION

##### SPECIAL ACCESSORY

- EQUIPMENT REQ'D: 1 DC Power Supply - Capable of +1 VDC  
1 RF Power Source - Capable of 10 W at 850 MHz  
1 270 $\Omega$  Resistor - 5%

FIGURE REFERENCES: Demod Audio PC Board (Figure 6-25)  
Power Termination Mechanical Assembly (Figure 6-33)

TEST SET-UP DIAGRAM: N/A

##### STEP

##### PROCEDURE

1. Set FM/AM-1500 Controls as follows:

| CONTROL      | SETTING    |
|--------------|------------|
| (6) DEV/PW   | "15 WATTS" |
| (19) GEN/REC | "GEN"      |
| (22) VOLUME  | Fully cw   |
| (31) TONE 2  | Fully ccw  |
| (33) TONE 1  | Fully ccw  |

2. Using external Power Supply, apply +1 VDC to FL6204 on Power Termination Module. Verify speaker output changes from no output to noise.
3. Disconnect external Power Supply from Power Termination Module.
4. Zero MODULATION Meter (1) to give an indication of zero watts by adjusting R4871 (ZERO PWR) on the DEMOD AUDIO PC Board.
5. Using an external RF Power Source, apply 10 watts of RF power at 120.2 MHz to the TRANS/-40 dB DUPLEX Connector (11). Adjust R4904 (15 W) on DEMOD AUDIO PC Board for following indications:
- CRT power meter reads 10 watts. Note and record.
  - MODULATION Meter (1) reads between 9 and 11 watts. Note and record.
  - When DISPLAY Control (51) is rotated to "ANALY", the display on the CRT is approximately at the -40 dB level.
6. Rotate DEV/PWR Control (6) to "150 WATTS". Adjust R4881 (150 W) on DEMOD AUDIO PC Board for following indications:
- CRT power meter reads 10 watts.
  - MODULATION Meter (1) reads between 9 and 11 watts.
7. Change RF Power Source to apply 10 watts at 850 MHz.

| STEP | PROCEDURE   |
|------|---|
| 8.   | Rotate DEV/PWR Control (51) to "15 WATTS". Adjust R6212 (DET FLATNESS) in POWER TERMINATION Module for following indications:                                 |
| a.   | CRT power meter reads within 0.5 watts of reading in Step 5.a.  |
| b.   | MODULATION Meter (1) reads within 0.5 watts of reading in Step 5.b.   |
| 9.   | Change RF Power Source to 0 watts. Slowly increase RF Power Source and verify FM/AM-1500 switches from Generate mode to Receive mode at approximately 100 mW. |
| 10.  | Connect a 270 $\Omega$ resistor between FL6202 on POWER TERMINATION Module and ground. Verify OVERTEMP Indicator (9) on front panel is illuminated.           |
| 11.  | Disconnect all test equipment.  |

## 4-7 GENERATOR FUNCTIONAL BLOCK

### 4-7-1 RF OUTPUT POWER CALIBRATION

#### SPECIAL ACCESSORY

- EQUIPMENT REQ'D:
- 1 Digital Voltmeter - Any
  - 1 Spectrum Analyzer - Capable of measuring 1000 MHz
  - 1 BOONTON Power Meter - Capable of reading -30 dBm
  - 1 BOONTON Modulation Meter - Capable of reading 3.3 kHz deviation at 1000 MHz input
  - 1 Oscilloscope - Any
  - 300 Hz Low Pass Filter - See Appendix D

- FIGURE REFERENCES:
- FM Generator Mechanical Assembly (Figure 6-27)
  - Demod Audio PC Board (Figure 6-25)
  - Generator Mixer PC Board (Figure 6-28)
  - I/O Interface PC Board (Figure 6-39)

TEST SET-UP DIAGRAM: N/A

#### **NOTE**

FM/AM-1500 Serial Numbers 1005 thru 1425 contain DEMOD AUDIO PC Board 7010-5034-700. FM/AM-1500 Serial Numbers 1426 thru 2817 contain DEMOD AUDIO PC Board 7010-5037-300. FM/AM-1500 Serial Numbers 2818 and on contain DEMOD AUDIO PC Board 7010-5038-900. All adjustments and test points referenced in the following calibration procedure are for the 7010-5037-300 and 7010-5038-900 PC Boards only. For adjustments and test points on 7010-5034-700 PC Boards, see FM/AM-1500 Maintenance Manual Rev. 0 thru Rev. 3.

#### STEP

#### PROCEDURE

1. Set PWR/OFF/Batt switch (13) to "PWR".
2. Present only under the following conditions:  
GEN/REC Switch (19) is in "GEN" or DISPLAY Control (51) is in "TRACK" or "SWEEP".

STEP                      PROCEDURE

---

3. Set FM/AM-1500 Controls as follows:

| CONTROL              | SETTING                                    |
|----------------------|--|
| (10) RF Output Level | "-30 dBm"                                  |
| (18) DUPLEX/SIMPLEX  | "SIMPLEX"                                  |
| (19) GEN/REC         | "GEN"                                      |
| (20) Keyboard        | RF 500.0000 MHz<br>(LCD FREQUENCY Readout) |
| (31) TONE 2          | Fully ccw                                  |
| (33) TONE 1          | Fully ccw                                  |
| (51) DISPLAY         | Anywhere but on "TRACK"<br>or "SWEEP"      |

4. Using external Spectrum Analyzer, measure the RF output at J4206 on the FM Generator Module. Verify output is -13 (+5, -6) dBm at 68.6 MHz.

5. Using external Spectrum Analyzer, measure the RF output at J4403 on the Generator Mixer Module. Adjust R3412 (F1 FIXED) and R3423 (F2 FIXED) in Generator Mixer Module to peak display. Adjust R3436 (OUTPUT LEVEL) in Generator Mixer Module to set output level to -12 to -16 dBm.

6. Connect a BOONTON Power Meter to TRANS/-40 dB DUPLEX Connector (11). Adjust R4963 (RF LEVEL) on DEMOD AUDIO PC Board for a reading of -30 dBm ( $\pm 2.0$  dB) on Power Meter.

7. Repeat Step 6 for following selected RF frequencies:

SECECTED FREQUENCIES

|         |         |
|---------|---------|
| 100 kHz | 400 MHz |
| 10 MHz  | 500 MHz |
| 50 MHz  | 600 MHz |
| 100 MHz | 700 MHz |
| 200 MHz | 800 MHz |
| 300 MHz | 900 MHz |

8. Disconnect Power Meter from, and connect external Spectrum Analyzer to TRANS/-40 dB DUPLEX Connector (11). Set external Spectrum Analyzer to 1 MHz/DIV dispersion, 300 kHz bandwidth and 10 dB/DIV.



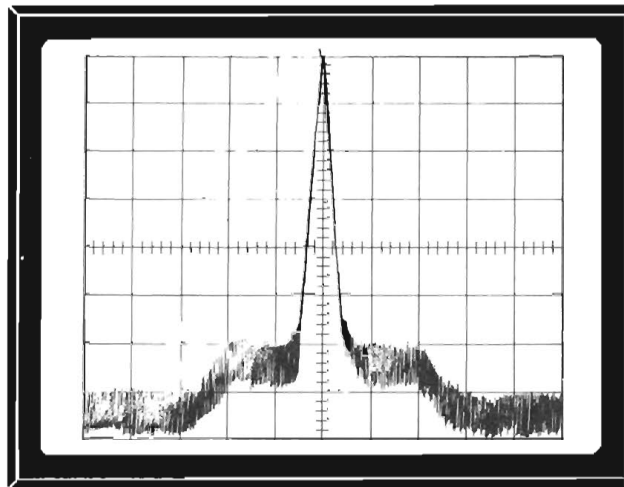
| STEP | PROCEDURE |
|------|-----------|
|------|-----------|

9. Step FREQUENCY readings on LCD (21) as follows:

| 1 MHz Steps   | 10 MHz Steps  |
|---------------|---------------|
| 0 - 50 MHz    | 50 - 88 MHz   |
| 88 - 176 MHz  | 177 - 400 MHz |
| 400 - 500 MHz | 500 - 850 MHz |
| 850 - 950 MHz | 950 - 999 MHz |

Verify at each step:

- The spectrum 2 MHz on each side of carrier is rounded and does not break into oscillations (refer to Figure 4-2).
- The spectrum between 1 MHz and 1.8 MHz on each side of carrier varies no more than 3 dB.
- The delay line locks on each frequency - i.e., there is no excessive noise on Spectrum Analyzer.



1 MHz/DIV  
300 KHz BW  
10 dB/DIV

Figure 4-2 RF Output Display

10. Observe Spectrum Analyzer at following frequency settings:

- 30.2 MHz
- 175.2 MHz
- 450.2 MHz
- 850.2 MHz

Verify the spectrum 100 kHz on each side of the carrier is 65 dBc or lower.

11. Set FM/AM-1500 Controls as follows:

| CONTROL               | SETTING      |
|-----------------------|--------------|
| (10) RF Output Level" | 10 dBm"      |
| (18) DUPLEX/SIMPLEX   | "DUPLEX"     |
| (21) LCD              | 850.2000 MHz |

12. Using external Spectrum Analyzer, measure the RF output at the DUPLEX OUTPUT Connector (16). Verify level is -10 dBm (2 dB). Disconnect coax to DUPLEX OUTPUT Connector (16).

STEP                      PROCEDURE

---

13. Connect a 50Ω Termination to DUPLEX OUTPUT Connector (16). Using external Spectrum Analyzer, measure RF output level at TRANS/-40 dB DUPLEX Connector (11). Verify output level is -50 dBm (3 dB).
14. Repeat Steps 12 and 13 for a 120.2000 MHz setting on LCD (21).
15. Connect Modulation Meter, 300 Hz Low-pass Filter and Digital Voltmeter to FM/AM-1500 as shown in Figure 4-3. Set Modulation Meter filters to 30 Hz high-pass and 3 KHz low-pass.

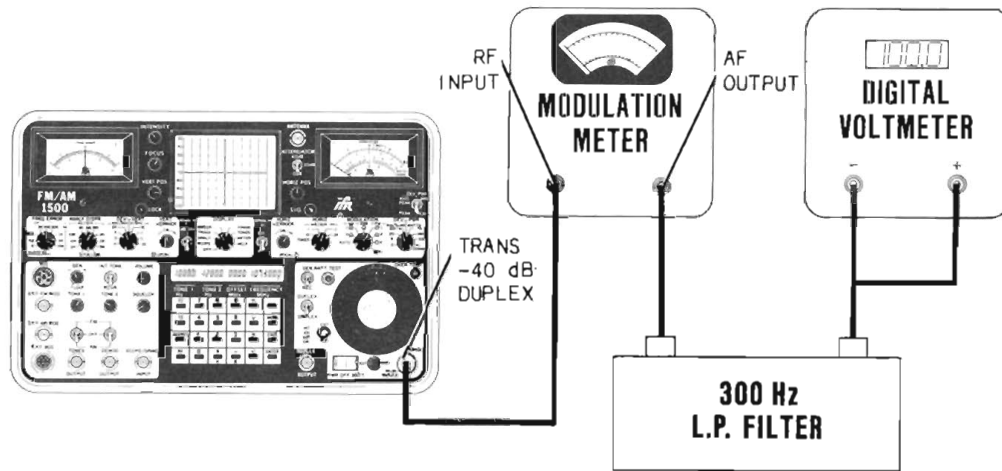


Figure 4-3 Residual FM Test Hookup

16. Set FM/AM-1500 Controls as follows:

| CONTROL               | SETTING                 |
|-----------------------|-------------------------|
| (20) Keyboard         | 120.2 Hz TONE 1 Readout |
| (28) Tone 1 FM/OFF/AM | "AM"                    |
| (51) DISPLAY          | "METER"                 |

17. Adjust TONE 1 Control (33) for 10 KHz deviation.
18. Record VRMS reading on DVM as A.
19. Adjust TONE 1 Control fully CCW.
20. Record VRMS reading on DVM as B.
21. Calculate residual FM as follows:  

$$10 \text{ kHz}/A = X/B \text{ (X = residual FM)}$$
 Verify residual FM < 50 Hz.
22. Set Modulation Meter to 300 Hz high-pass and 3 kHz low-pass. Disconnect 300 Hz low-pass filter and connect DVM to AF Output of Modulation Meter.
23. Set TONE 1 LCD (21) Readout to 1000.0 Hz. Adjust TONE 1 Control (33) for 3.3 KHz (±10 Hz) deviation.

STEP                      PROCEDURE

---

24. Measure the VRMS out of the Modulation Meter AF Output at the following FREQUENCY settings on the LCD (21): 100.2 MHz, 850.2 MHz and 999 MHz. Record reading at each setting as A.
25. Adjust TONE 1 Control fully ccw. Record reading at 100.2 MHz, 850.2 MHz and 999 MHz as B. Calculate dB ratio for each setting as follows:

$$\text{Ratio} = 20 \times \log (A/B)$$

Verify ratio is 40 dB or greater for each setting.

**NOTE:**

If DVM has a Relative button, it may be used to give a dB reading at each step.

26. Connect external Spectrum Analyzer to DUPLEX OUTPUT Connector (16).
27. Select 000.1000 MHz on LCD (21). Verify second harmonic ( $\pm 200$  kHz) is 25 dBc or lower.
28. Select 450.2000 MHz on LCD (21). Verify:
  - a. Second harmonic (900.4 MHz) is 25 dBc or lower.
  - b. Non-harmonics at 540.2 MHz and 850.4 MHz are at most -40 dBc and all other signals are 60 dBc or lower.
  - c. Noise 20 KHz from 450.2000 MHz is 55 dBc or lower when on 3 KHz bandwidth.
29. Select 090.2000 thru 990.2000 MHz on LCD (21) in 100 MHz steps. Verify:
  - a. Second harmonics in all cases are 25 dBc or lower.
  - b. All non-harmonics are 40 dBc or lower.
30. Set FM/AM-1500 Controls as follows:

| CONTROL             | SETTING                                    |
|---------------------|--|
| (18) DUPLEX/SIMPLEX | "SIMPLEX"                                  |
| (19) GEN/REC        | "GEN"                                      |
| (20) Keyboard       | RF 850.2000 MHz<br>(LCD FREQUENCY Readout) |

31. Connect external Spectrum Analyzer to TRANS/-40 dB DUPLEX Connector (11).
32. Rotate RF Output Level Control (10) from -10 dBm to -80 dBm. Verify output level on display of Spectrum Analyzer is equal ( $\pm 2$  dB) to RF Output Level Control setting across the range.
33. Rotate RF Output Level Control (10) from -80 dBm to -127 dBm. Verify output level on display of Spectrum Analyzer is equal ( $\pm 2.5$  dB) to RF Output Level Control setting across the range.
34. Rotate RF Output Level Control (10) to -30 dBm.

- | STEP                | PROCEDURE  |         |         |                     |          |              |       |          |              |
|---------------------|--|---------|---------|---------------------|----------|--------------|-------|----------|--------------|
| 35.                 | Select RF SWEEP Menu on CRT. Enter following data:<br>Start                    0.1 MHz<br>Stop                     990.1 MHz<br>Inc STEP                10.0 MHz<br>Inc RATE                1000 ms<br>Then press: "EXEC, 2nd, FSWP, 1, ENTER, 2nd, STEP". Press "v"<br>Key until 0.1 MHz (beginning) is reached.  |         |         |                     |          |              |       |          |              |
| 36.                 | Connect Oscilloscope and Voltmeter, with a BNC Tee, to X-OUT Connector (59) on rear panel of FM/AM-1500. Verify voltage of 0 VDC. If not, adjust R4333 on I/O Interface PC Board for 0 VDC.  |         |         |                     |          |              |       |          |              |
| 37.                 | Press: "EXEC, ENTER".  |         |         |                     |          |              |       |          |              |
| 38.                 | Observe RF SWEEP signal on external Spectrum Analyzer as it steps up each 10 MHz. Verify High Loop locks on each frequency, with no oscillations.  |         |         |                     |          |              |       |          |              |
| 39.                 | Observe Oscilloscope and verify voltage changes with each INC STEP of menu.  |         |         |                     |          |              |       |          |              |
| 40.                 | Observe Voltmeter when FREQ SWEEP Menu finishes sweeping. Verify voltage is +10 VDC. Adjust R4331 on I/O INTERFACE PC Board for +10 VDC, if necessary.   |         |         |                     |          |              |       |          |              |
| 41.                 | Set FM/AM-1500 Controls as follows:<br><table border="1"> <thead> <tr> <th>CONTROL</th> <th>SETTING</th> </tr> </thead> <tbody> <tr> <td>(18) DUPLEX/SIMPLEX</td> <td>"DUPLEX"</td> </tr> <tr> <td>(19) GEN/REC</td> <td>"GEN"</td> </tr> <tr> <td>(21) LCD</td> <td>860.2000 MHz</td> </tr> </tbody> </table>   | CONTROL | SETTING | (18) DUPLEX/SIMPLEX | "DUPLEX" | (19) GEN/REC | "GEN" | (21) LCD | 860.2000 MHz |
| CONTROL             | SETTING  |         |         |                     |          |              |       |          |              |
| (18) DUPLEX/SIMPLEX | "DUPLEX"   |         |         |                     |          |              |       |          |              |
| (19) GEN/REC        | "GEN"  |         |         |                     |          |              |       |          |              |
| (21) LCD            | 860.2000 MHz   |         |         |                     |          |              |       |          |              |
| 42.                 | Connect external Spectrum Analyzer to DUPLEX OUTPUT Connector (16). Set Spectrum Analyzer to 10 MHz/DIV at 860.4 MHz center frequency.   |         |         |                     |          |              |       |          |              |
| 43.                 | Select both (+) and (-) 45 MHz OFFSET on LCD (21), and verify while rotating RF Level Output Control (10) from -10 to -80 dBm that:<br>a. RF output level on Spectrum Analyzer is within 2 dB of RF Output Level over the range.<br>b. Spurs on signal with -45 MHz OFFSET applied are 60 dBc or lower within +35 MHz to +55 MHz of carrier.<br>c. Spurs on signal with +45 MHz OFFSET applied are 40 dBc or lower within -35 MHz to -55 MHz of carrier. |         |         |                     |          |              |       |          |              |

#### 4-7-2 DUPLEX OFFSET CALIBRATION

SPECIAL ACCESSORY

EQUIPMENT REQ'D: 1 Spectrum Analyzer – Capable of measuring 230 MHz at -4 dBm

FIGURE REFERENCES: FM/AM-1500 Interconnect (Figure 7-1)

DUPLEX OFFSET Mechanical Assembly  
(Figure 6-30)

TEST SET-UP DIAGRAM: N/A

STEP PROCEDURE

1. Set FM/AM-1500 Controls as follows:

| CONTROL             | SETTING          |
|---------------------|------------------|
| (13) PWR/OFF        | "PWR"            |
| (18) DUPLEX/SIMPLEX | "DUPLEX"         |
| (19) GEN/REC        | "GEN"            |
| (21) LCD            | 00.00 MHz OFFSET |

2. Using an external Spectrum Analyzer and an SMB to SMB tee, measure output level at J3201 on DUPLEX OFFSET Module. Verify level is -8 to -4 dBm at 180 MHz. Note and record level.

3. While observing external Spectrum Analyzer, verify all keypad digits from 00.00 to 49.99 operate in both plus and minus and that the output frequency steps from +49.99 MHz to -49.99 MHz on either side of 180 MHz as follows:

| LCD (21) Setting  | Displayed RF |
|-------------------|--------------|
| -49.99 MHz OFFSET | 229.99 MHz   |
| -48.88 MHz OFFSET | 228.88 MHz   |
| -47.77 MHz OFFSET | 227.77 MHz   |
| -46.66 MHz OFFSET | 226.66 MHz   |
| -45.55 MHz OFFSET | 225.55 MHz   |
| -44.44 MHz OFFSET | 224.44 MHz   |
| -33.33 MHz OFFSET | 213.33 MHz   |
| -22.22 MHz OFFSET | 202.22 MHz   |
| -11.11 MHz OFFSET | 191.11 MHz   |
| 00.00 MHz OFFSET  | 180.00 MHz   |
| +11.11 MHz OFFSET | 168.89 MHz   |
| +22.22 MHz OFFSET | 157.78 MHz   |
| +33.33 MHz OFFSET | 146.67 MHz   |
| +44.44 MHz OFFSET | 135.56 MHz   |
| +45.55 MHz OFFSET | 134.45 MHz   |
| +46.66 MHz OFFSET | 133.34 MHz   |
| +47.77 MHz OFFSET | 132.23 MHz   |
| +48.88 MHz OFFSET | 131.12 MHz   |
| +49.99 MHz OFFSET | 130.01 MHz   |

| STEP | PROCEDURE |
|------|-----------|
|------|-----------|

---

4. Set GEN/REC Switch (19) to "REC".
5. Observe displayed signal on external Spectrum Analyzer. Verify RF level is at least 50 dB below level noted and recorded in Step 2.
6. Disconnect all test equipment and reconnect all removed coax cables.

### 4-7-3 DUAL TONE GENERATOR CALIBRATION

#### SPECIAL ACCESSORY

- EQUIPMENT REQ'D:
- 1 Oscilloscope – Any
  - 1 Distortion Analyzer – Capable of measuring distortion at 20 kHz
  - 1 150 $\Omega$ , 1/4 W Resistor
  - 1 Frequency Counter – Capable of reading 66 kHz

FIGURE REFERENCES: Dual Tone Generator PC Board (Figure 6-34)

TEST SET-UP DIAGRAM: N/A

#### STEP PROCEDURE

1. Set FM/AM-1500 controls as follows:

| CONTROL       | SETTING                   |
|---------------|---------------------------|
| (13) PWR/OFF  | "PWR"                     |
| (20) Keyboard | 1000.0 Hz, TONE 1 Readout |
| (31) TONE 2   | Fully ccw                 |
| (33) TONE 1   | Fully cw                  |

2. Load the TONES OUTPUT Connector (27) with a 150 $\Omega$ , 1/4 W Resistor.

#### **NOTE**

Make a connector box for Resistor and put a BNC tee on the output as shown in Appendix D.

3. Connect external Oscilloscope to one side of BNC tee.
4. Connect external Distortion Analyzer to other side of BNC tee.
5. Verify sine wave output level is  $\geq 7.1$  Vp-p.
6. Verify audio distortion is  $\geq 0.7\%$  at 1000 Hz.
7. Select 10000.0 Hz TONE 1 on LCD (21).
8. Disconnect Oscilloscope and connect Frequency Counter in its place. Verify output frequency is 10,000 Hz ( $\pm 1$  Hz). If not, adjust trimcap C4505 on DUAL TONE GENERATOR PC Board.
9. Select 2000.0 Hz TONE 1 on LCD (21).
10. Verify audio distortion is within 0.7% at 20,000 Hz.
11. Select 50.0 Hz TONE 1 on LCD (21).
12. Verify audio distortion is  $< 2\%$  at 50 Hz.

## STEP

## PROCEDURE

13. Set FM/AM-1500 controls as follows:

| CONTROL       | SETTING                |
|---------------|------------------------|
| (21) Keyboard | 50.0 Hz TONE 2 Readout |
| (31) TONE 2   | Fully cw               |
| (33) TONE 1   | Fully ccw              |

14. Verify audio distortion is <2% at 50 Hz.
15. Select 20000.0 Hz TONE 2 on LCD (21).
16. Verify audio distortion is <0.7% at 20,000 Hz.
17. Select 1000.0 Hz TONE 2 on LCD (21).
18. Verify audio distortion is <0.7% at 1000 Hz.
19. Select each of the following frequencies and verify output frequency is equal ( $\pm 0.1$  Hz) to selected frequency.

## TONE 2 on LCD (21)

|          |          |
|----------|----------|
| 409.6 Hz | 416.0 Hz |
| 409.7 Hz | 422.4 Hz |
| 409.9 Hz | 435.2 Hz |
| 410.0 Hz | 460.8 Hz |
| 410.4 Hz | 512.0 Hz |
| 411.2 Hz | 614.4 Hz |
| 412.8 Hz |          |

20. Select each of the following frequencies and verify output frequency is equal ( $\pm 0.01\%$ ) to selected frequency.

## TONE 2 on LCD (21)

|         |          |
|---------|----------|
| 2048 Hz | 16384 Hz |
| 4096 Hz | 32768 Hz |
| 8192 Hz | 65536 Hz |

21. Rotate TONE 1 Control (33) fully cw and rotate TONE 2 Control (31) fully ccw.
22. Select each of the following frequencies and verify output frequency is equal ( $\pm 0.01\%$ ) to selected frequency.

## TONE 1 on LCD (21)

|         |          |
|---------|----------|
| 2048 Hz | 16384 Hz |
| 4096 Hz | 32768 Hz |
| 8192 Hz | 65536 Hz |

23. Select the following frequencies and verify output frequency is equal ( $\pm 0.1$  Hz) to selected frequency.

## TONE 1 on LCD (21)

|          |
|----------|
| 409.6 Hz |
| 409.7 Hz |
| 409.9 Hz |
| 410.0 Hz |

24. Disconnect all test equipment.



## 4-8 SPECTRUM ANALYZER FUNCTIONAL BLOCK

### 4-8-1 SPECTRUM ANALYZER

SPECIAL ACCESSORY  
EQUIPMENT REQ'D: 1 Spectrum Analyzer – Capable of measuring  
500 MHz at -30dBm  
1 RF Generator – Capable of generating  
1000 MHz at -30dBm

FIGURE REFERENCES: FM/AM-1500 Interconnect (Figure 7-1)  
Spectrum Analyzer LO Mechanical Assembly  
(Figure 6-36)  
Spectrum Analyzer IF Mechanical Assembly  
(Figure 6-35)  
Generator Mixer Mechanical Assembly  
(Figure 6-28)  
Spectrum Analyzer RF Mechanical Assembly  
(Figure 6-37)  
89-90 MHz Receiver Mechanical Assembly  
(Figure 6-24)

TEST SET-UP DIAGRAM: N/A

#### STEP

#### PROCEDURE

1. Set FM/AM-1500 Controls as follows:  
CONTROLSETTING

|                  |   |
|------------------|---|
| (19) GEN/REC     | "REC"                                   |
| (21) Keyboard    | 120.2000 MHz<br>(LCD FREQUENCY Readout) |
| (38) ANALY DISPR | "1 M"                                   |
| (48) dB/DIV      | "10 dB/DIV"                             |
| (49) ANAL V      | Center pot                              |
| (51) DISPLAY     | "ANALY"                                 |
| (53) ANAL H      | Center pot                              |

- Using external Oscilloscope, observe voltage on pin 5 of J4603 on Spectrum Analyzer LO Module. Adjust ANAL H Adjustment (53) on front panel for a voltage indication within 0.3 VDC from ground.
- Observe base line sweep on CRT. Adjust R3560 (HORIZ GAIN) on Spectrum Analyzer LO Module until sweep ends 5.2 major divisions to the left of the major vertical axis.
- Adjust R3547 (SYMMETRY) on Spectrum Analyzer LO Module to center trace equally on both sides of major vertical axis.
- Repeat Steps 3 and 4 until no further adjustment is necessary.

STEP                   PROCEDURE

---

6. Connect an RF Generator set at 1000 MHz, -30 dBm, to ANTENNA Connector (56).
7. Set LCD (21) to 500.0000 MHz and rotate ANALY DISPR Control (38) to "FULL".
8. Verify 1000 MHz signal on CRT is five major divisions to the right of the major vertical axis and that the 0 MHz signal is five major divisions (-1 minor division, +1.5 minor divisions) to the left of the major vertical axis. Adjust R3601 (WIDE DISPR) on Spectrum Analyzer LO Module for correct location of 1000 MHz signal.

**NOTE**

If it is necessary to adjust R3601, it may be necessary to repeat Steps 2 thru 5 to readjust centering and symmetry.

9. Set output frequency of RF Generator to 500.2 MHz at -30 dBm.
10. Rotate ANALY DISPR Control (38) to "10 M". Set LCD (21) to 510.2000 MHz. Verify displayed signal on CRT is 1 major division ( $\pm 1$  minor division) to the left of the major vertical axis.
11. Rotate ANALY DISPR Control (38) to "5 M". Set LCD (21) to 505.2000 MHz. Verify displayed signal on CRT is 1 major division ( $\pm 1$  minor division) to the left of the major vertical axis.
12. Rotate ANALY DISPR Control (38) to "2 M". For the following frequencies, verify signal on CRT is within 1.5 minor divisions of the major vertical axis.

| LCD (21) FREQUENCY | RF Generator Setting |
|--------------------|----------------------|
| 999.9999 MHz       | 1000 MHz             |
| 700.0000 MHz       | 700 MHz              |
| 000.0000 MHz       | No RF                |

13. Set LCD (21) to 500.2000 MHz. Set RF Generator to 500.2000 MHz at -40 dBm. Rotate ANALY DISPR Control (38) to "1 M". Adjust R3529 (FREQ CENTER) on Spectrum Analyzer LO Module until displayed signal is centered on major vertical axis of CRT.
14. Set RF Generator to 497 MHz and then to 503 MHz. Verify displayed signal on CRT is centered, first, on the third major division to the left, and likewise to the right, of the major vertical axis. Adjust R3567 (NARROW DISPERSION) on Spectrum Analyzer LO Module for proper centering.

STEP                      PROCEDURE

---

15. For the following RF Generator frequencies and ANALY DISPR Control settings, verify displayed signal on CRT is centered on the third major division to the left, and likewise to the right of the major vertical axis.

| ANALY DISPR (38)<br>Setting | Tolerance<br>Minor Divisions | RF Generator<br>Setting (MHz) |
|-----------------------------|------------------------------|-------------------------------|
| .5 M                        | ±1                           | 501.5      498.5              |
| .2 M                        | ±1                           | 500.6      499.4              |
| .1 M                        | ±1                           | 500.3      499.7              |
| 20 K                        | ±1                           | 500.06     499.04             |
| 10 K                        | ±1                           | 500.03     499.07             |
| 2 K                         | ±7                           | 500.006    499.004            |
| 1 K                         | ±7                           | 500.003    499.007            |

**NOTE**

Adjust R3615 (300 Hz BW ANALY CNTR) as needed to center tolerance (3 minor divisions) to the dispersion settings at 2K and 1K. After completing narrow dispersion checks, repeat Steps 6 through 12 to recheck Wide Dispersion centering.

16. Rotate ANALY DISPR Control (38) to "1 M".
17. Disconnect RF Generator from ANTENNA Connector (56). Set RF Generator to 10.7 MHz at -20 dBm. Disconnect P5401 from J5401 on the Spectrum Analyzer IF Module. Connect RF Generator to J5401.
18. Connect an external Spectrum Analyzer to Test Point 2 (TP2) on Spectrum Analyzer IF Module. Adjust R3938 (30 kHz BW GAIN) on Spectrum Analyzer IF Module for a 2.5 MHz signal at -22 dBm at TP2.

**NOTE**

External Spectrum Analyzer must be equipped with a DC Block for Steps 18 and 19.

19. Rotate ANALY DISPR Control (38) to "2 M". Adjust R3919 (650 kHz BW GAIN) for a 2.5 MHz signal at -19 dBm at TP2.
20. Disconnect Spectrum Analyzer from TP2. Rotate ANALY DISPR Control (38) to ".1 M".
21. Set RF Generator to 0 MHz output. Adjust R3961 (BASE LINE) on Spectrum Analyzer IF Module until base line on CRT is on the -108 dB graticule.
22. Set RF Generator to 10.7 MHz at -30 dBm. Adjust R3959 (DETECTOR GAIN) until displayed signal on CRT is on the -40 dB graticule.
23. Set RF Generator to 10.7 MHz at -20 dBm. Adjust R3941 (LOG LIN) until displayed signal on CRT is on the -30 dB graticule.

- | STEP | PROCEDURE   |
|------|---|
| 24.  | Set RF Generator to 10.7 MHz at -70 dBm. Adjust R3942 (AMP 1 GAIN) until displayed signal on CRT is on the -80 dB graticule.  |
| 25.  | Set RF Generator to 10.7 MHz at -90 dBm. Adjust R3951 (AMP 2 GAIN) until displayed signal on CRT is on the -100 dB graticule.   |
| 26.  | While stepping the output level of the RF Generator from -20 dBm to -80 dBm, verify displayed signal on CRT steps from -30 dB to -90 dB and is within 2 dB of each selected graticule. If tolerance is not met at each step, repeat Steps 20 thru 26.                     |
| 27.  | Set dB/DIV Switch (48) to "1". Rotate VERT POS Control (45) fully cw.   |
| 28.  | Set RF Generator to 10.7 MHz at -20 dBm. Adjust R3963 (OFFSET) until displayed signal on CRT is on the -20 dB graticule.  |
| 29.  | Set RF Generator to 10.7 MHz at -30 dBm. Adjust VERT POS Control (45) until displayed signal on CRT is on the top horizontal graticule.   |
| 30.  | Set RF Generator to 10.7 MHz at -38 dBm. Adjust R3969 (1 dBm/DIV GAIN) until displayed signal on CRT is on the bottom horizontal graticule.   |
| 31.  | Repeat Steps 28 thru 30 and verify a tolerance of 1 minor division can be met at each step without having to adjust the trimpots.   |
| 32.  | Disconnect P4403 from J4403 on GENERATOR Mixer Module. Connect external Spectrum Analyzer to J4403. Center signal on external Spectrum Analyzer at 90 MHz and set external Analyzer controls to 1 MHz/DIV and 1 ms/DIV sweep.   |
| 33.  | Rotate DISPLAY Control to "ANALY". Adjust R3412 (F1 FIXED) and R3423 (F2 FIXED) on GENERATOR MIXER Module for maximum gain of signal on external Spectrum Analyzer. Then adjust R3436 (OUTPUT) on GENERATOR MIXER Module for an output level of -11 to -16 dBm at 90 MHz. |
| 34.  | Rotate DISPLAY Control to "ANALY". Adjust R3412 (F1 FIXED) and R3423 (F2 FIXED) on GENERATOR MIXER Module for maximum gain of signal on external Spectrum Analyzer. Then adjust R3436 (OUTPUT) on GENERATOR MIXER Module for an output level of -11 to -16 dBm at 90 MHz. |
| 35.  | Observe external Spectrum Analyzer and verify sweep signal from 84 to 96 MHz is flat (within 1 dB). If not, adjust R3413 (F1 GAIN), R3415 (F1 OFFSET), R3417 (F2 GAIN) and R3421 (F2 OFFSET) on GENERATOR MIXER Module.   |

**NOTE**

The above mentioned resistors are interactive and may need repeated adjustments to obtain the correct signal.

STEP                      PROCEDURE

---

- 36. Disconnect Spectrum Analyzer from J4403. Connect P4403 to J4403 on GENERATOR MIXER Module.
- 37. Using a BNC to BNC coax cable, connect ANTENNA Connector (56) to TRANS/-40 dB DUPLEX Connector (11). Rotate RF Output Level Control (10) to -40 dB.
- 38. Observe displayed signal on CRT. Adjust R3794 (TRACKING OFFSET) and R3791 (TRACKING GAIN) on Spectrum Analyzer RF Module for maximum level and flatness within 1 dB.

NOTE:

Ensure S3701 on Spectrum Analyzer RF Module is in "RUN" position (to the left, looking from outside of Module).

- 39. Select the entire range (0-9) of the 100 kHz digit on LCD (21). Verify displayed signal is flat ( $\pm 1$  dB) for entire range.
- 40. Disconnect TRANS/-40 dB DUPLEX Connector (11) from ANTENNA Connector (56). Connect ANTENNA Connector (56) to DUPLEX OUTPUT Connector (16).
- 41. Set FM/AM-1500 Controls as follows:
 

| CONTROL              | SETTING                                 |
|----------------------|---|
| (10) RF Output Level | -30 dBm                                 |
| (18) DUPLEX/SIMPLEX  | "DUPLEX"                                |
| (19) GEN/REC         | "GEN"                                   |
| (21) Keyboard        | 500.0000 MHz<br>(LCD FREQUENCY Readout) |
| (38) ANALY DISPR     | "10 K"                                  |
| (51) DISPLAY         | "ANALY"                                 |
- 42. Rotate ANALY DISPR Control (38) to "1 K". Adjust R3771 (300 kHz BW GAIN) on Spectrum Analyzer RF Module until signal level on CRT is on the -30 dB graticule.
- 43. Rotate ANALY DISPR Control (38) to "1 M". Adjust R3777 (650 kHz BW GAIN) on Spectrum Analyzer RF Module until signal level on CRT is on the -30 dB graticule.
- 44. Set ATTENUATOR Switch (55) to "20 dB". Verify signal level on CRT is on -50 dB graticule ( $\pm 2$  dB).
- 45. Set ATTENUATOR Switch (55) to "40 dB". Verify signal level on CRT is on -70 dB graticule ( $\pm 2$  dB).
- 46. Set ATTENUATOR Switch (55) to "0 dB". Rotate RF Output Level Control (10) to -30 dBm.
- 47. Rotate ANALY DISPR Control (38) to all settings except "2 K" and verify signal level on CRT is -30 dB ( $\pm 2$  dB) for each setting.

STEP                      PROCEDURE

---

48. Set FM/AM-1500 Controls as follows:

| CONTROL               | SETTING           |
|-----------------------|-------------------|
| (7) MODULATION        | "AM 1"            |
| (21) LCD              | 500.0000 MHz      |
| (28) Tone 1 FM/OFF/AM | 1000.0 Hz, TONE 1 |
| (38) ANALY DISPR      | "AM"              |
| (51) DISPLAY          | "FULL"            |
|                       | "TRACK"           |

49. Disconnect ANTENNA Connector (56) from DUPLEX OUTPUT Connector (16). Connect ANTENNA Connector (56) to TRANS/-40 dB DUPLEX Connector (11).

50. Note the position of the carrier signal on CRT with TONE 1 Control (33) fully ccw. Verify, when TONE 1 Control (33) is rotated fully cw, the RF envelope peaks at least +6 dBc and -26 dBc.

51. Rotate TONE 1 Control (33) fully ccw. Rotate ANALY DISPR Control (38) to ".1 M". Select 000.0000 MHz on LCD (21). Disconnect ANTENNA Connector (56) from TRANS/-40 dB DUPLEX Connector (11). Adjust R9302 and R9303 in Mixer Null Module to put top of signal on CRT on the top graticule, or as near as possible.

52. Rotate ANALY DISPR Control (38) to "FULL". Select 500.0000 MHz on LCD (21). Connect ANTENNA Connector (56) to TRANS/-40 dB DUPLEX Connector (11).

53. Rotate TONE 1 Control (33) fully ccw. Set dB/DIV Switch (48) to "1". Verify tracking flatness on CRT  $\pm 4$  dB (to 950 MHz), or within 6 dB above 950 MHz.

54. Rotate ANALY DISPR Control (38) to "10 M". Select 050.0000 MHz on LCD (21). Verify tracking flatness on CRT of  $\leq 2$  dB from 0 to 50 MHz.

55. Disconnect coax from ANTENNA Connector (56) and connect a BNC tee to ANTENNA Connector. Then connect coax to one side of tee. Connect an open length of coax to the other side of tee. Verify linear cable fault nulls across the band.

56. Disconnect open length of coax from tee.

57. Rotate RF Output Level Control (10) to -100 dBm and verify cross-talk noise does NOT appear on the base line on CRT.

58. Rotate DISPLAY Control (51) to "ANALY". Rotate ANALY DISPR Control (38) to "FULL".

59. Observe base line on CRT display. Verify a straight base line with no signal present.

60. Rotate ANALY DISPR Control (38) to "1 M". Note and record base line level.

| STEP                | PROCEDURE  |         |         |                     |           |              |       |                  |        |              |         |
|---------------------|--|---------|---------|---------------------|-----------|--------------|-------|------------------|--------|--------------|---------|
| 61.                 | Select 015.0000 MHz on LCD (21). Verify base line rises $\leq 2$ dB from level in Step 63.   |         |         |                     |           |              |       |                  |        |              |         |
| 62.                 | Select 005.0000 MHz on LCD (21). Verify base line rises $\leq 2$ dB from 5 to 10 MHz and no extraneous signals are present.  |         |         |                     |           |              |       |                  |        |              |         |
| 63.                 | Set FM/AM-1500 Controls as follows:  |         |         |                     |           |              |       |                  |        |              |         |
|                     | <table border="0"> <thead> <tr> <th>CONTROL</th> <th>SETTING</th> </tr> </thead> <tbody> <tr> <td>(18) DUPLEX/SIMPLEX</td> <td>"SIMPLEX"</td> </tr> <tr> <td>(19) GEN/REC</td> <td>"GEN"</td> </tr> <tr> <td>(38) ANALY DISPR</td> <td>"10 K"</td> </tr> <tr> <td>(51) DISPLAY</td> <td>"ANALY"</td> </tr> </tbody> </table> | CONTROL | SETTING | (18) DUPLEX/SIMPLEX | "SIMPLEX" | (19) GEN/REC | "GEN" | (38) ANALY DISPR | "10 K" | (51) DISPLAY | "ANALY" |
| CONTROL             | SETTING  |         |         |                     |           |              |       |                  |        |              |         |
| (18) DUPLEX/SIMPLEX | "SIMPLEX"  |         |         |                     |           |              |       |                  |        |              |         |
| (19) GEN/REC        | "GEN"  |         |         |                     |           |              |       |                  |        |              |         |
| (38) ANALY DISPR    | "10 K"   |         |         |                     |           |              |       |                  |        |              |         |
| (51) DISPLAY        | "ANALY"  |         |         |                     |           |              |       |                  |        |              |         |
| 64.                 | Rotate GEN/LOCK Control (35) from fully (-) (not in "LOCK") to fully (+). Verify signal on CRT shifts at least $\pm 10$ kHz on each side of center frequency.  |         |         |                     |           |              |       |                  |        |              |         |
| 65.                 | Rotate GEN/LOCK Control (35) to "LOCK". Verify signal level on CRT is between -35 and -65 dBm.   |         |         |                     |           |              |       |                  |        |              |         |
| 66.                 | Disconnect all test equipment.   |         |         |                     |           |              |       |                  |        |              |         |

## **4-9 MICROPROCESSOR FUNCTIONAL BLOCK**

There are no adjustments on the CPU/MEMORY PC Board. There are four adjustments on the I/O Interface PC Board: R4350, R4354, R4331 and R4333. R4350 and R4354 are adjusted during RECEIVER SIGNAL calibration (4-6-1). R4331 and R4333 are adjusted during RF OUTPUT POWER calibration (4-7-1).



# SECTION 9 - CELLULAR OPTION

## 9-1 INTRODUCTION

The cellular option enables the FM/AM-1500 to test cellular mobile radios using "manual" tests and cell site simulation tests. To accomplish this task, a Cellular Controller PC Board has been added to the basic FM/AM-1500. With this new board installed, the FM/AM-1500 still maintains its capabilities as a communications service monitor, but also will simulate cell sites and act as an MTSO (Mobile Telephone Switching Office). In addition to the new PC Board, two new connectors are provided on the rear panel for the mobile test interface cable and the printer interface cable. An optional ICD-1500 interconnect box is available for use as an external device capable of monitoring each of the mobile radio test points.

## 9-2 THEORY OF OPERATION

The FM/AM-1500 communicates with a mobile radio via both digital and RF signals. Communication within the FM/AM-1500 is accomplished between a 6809 CPU on the Cellular Controller PC Board and a Z80 CPU on the CPU/MEMORY PC Board. The communication modes are explained as follows:

### A. Mobile Digital Interface

The mobile digital interface is the circuitry which allows the Cellular Controller PC Board to communicate with the mobile over the AMPS - configured interface bus. This port (J9102) is an 8-bit data bus, with three control lines for handshaking: DCL (Direction Control Line), TCL (Test Control Line), and CL (Clock Line). Circuitry on the Cellular Controller PC Board for this interface consists of a 6522 VIA and IEEE-488 bus drivers. The handshake control is software controlled, and the bus drivers provide the necessary bus termination and drive to meet IEEE-488 specifications.

Functions for this port include:

1. Allow the FM/AM-1500 to send test commands to the mobile.
2. Allow the FM/AM-1500 to request status from the mobile.
3. Allow the FM/AM-1500 to test an AMPS-compatible mobile control unit.

### B. Mobile RF Interface

The mobile RF interface is used to communicate with the mobile for cell site simulation, data verification, command/response tasks and signalling purposes. This function is bi-directional in that the FM/AM-1500 must generate and receive data and tones. Each of these two aspects are discussed as follows:

#### FM/AM-1500 generated data/tones

The FM/AM-1500 must communicate through the RF port (TRANS/-40 dB DUPLEX Connector) in the following cases:

1. Overhead messages (system control messages) sent to the mobile
2. Page messages (contact the mobile) sent to the mobile
3. Order messages (ring phone, change frequency, hang-up, etc.) sent to the mobile
4. SAT (Supervisory Audio Tone) transmission to the mobile
5. Audio to mobile for call completion

Items 1, 2 and 3 above refer to the digital data sent serially to the mobile. This data is 10 kHz, Manchester serial data which the mobile monitors and interprets as control data from a cell site. The circuitry on the Cellular Controller PC Board to accomplish the generate data stream consists of a 6522 VIA, a multiplying digital to analog converter for level adjustment, and switching for AM or FM modulation selection (cellular operation uses FM modulation only).

Item numbers 4 and 5 above refer to tones and/or voice sent to the mobile whenever the mobile is on a voice channel. The mobile expects the SAT frequency to be present on the FOVC (Forward Voice Channel) and the operator of the FM/AM-1500 will want to verify audio function when a call is completed. The tones sent (SAT and test tones) will be generated by the tone generators within the basic FM/AM-1500 (tone #2 is the SAT generator).

#### FM/AM-1500 received data/tones

The FM/AM-1500 must receive data/tones in the following cases:

1. Page response from the mobile
2. Reverse control data channel responses
3. Test transmissions over the RF port from the mobile
4. SAT and ST (Signaling Tone) transmission for call signaling
5. DTMF (Dual Tone, Multiple Frequency) tone signaling from the mobile
6. Audio from the mobile after call is completed

Items 1, 2 and 3 above refer to the data stream from the mobile to the FM/AM-1500. The mobile will respond to commands sent from the FM/AM-1500 by sending data back on the RCC (Reverse Control Channel) and the RVC (Reverse Voice Channel). The circuitry on the Cellular Controller PC Board required to decode the data from the demodulated audio consists of a programmable level control (MDAC), a programmable filter, a data clock generator, and a serial to parallel converter. The 6809 CPU will configure this hardware to the 10 kHz

Manchester data, and the serial to parallel circuitry will generate an interrupt after every 8 bits of data have been received.

Items 4, 5 and 6 above refer to the tone/voice received from the mobile. The SAT will be transponded from the mobile whenever the mobile is on a voice channel. The ST is sent as an "on-hook" indication and a "flash" signal. The DTMF tones are used for end-to-end signaling from the mobile. The circuitry to detect SAT, ST and DTMF is similar to the data detection. The demod audio is put through a level circuit and a programmable filter, and is then sent to a counter circuit for frequency measurement. Also, a signal is produced which may be used as a "valid tone" indication (active if signal gets through the filter).

### C. CPU-CPU Interface

To allow bi-directional communication between the cellular CPU (6809) and the existing CPU (Z80), a CPU-CPU interface is required. On the cellular side, the parallel ports of a VIA are used for data and handshake control. On the FM/AM-1500 side, bus latches and bus buffers are used to allow bi-directional data and handshaking to occur. The interface consists of 8 data bits (zd0-zd7), direction control line (zdir), test control line (ztcl), and a clock line (zcl). The function and use of each of these lines is as follows:

zd0 thru zd7 - bi-directional data lines, the direction of which is controlled by the zdir line. When zdir = 0, data direction is from the Z80 to the 6809

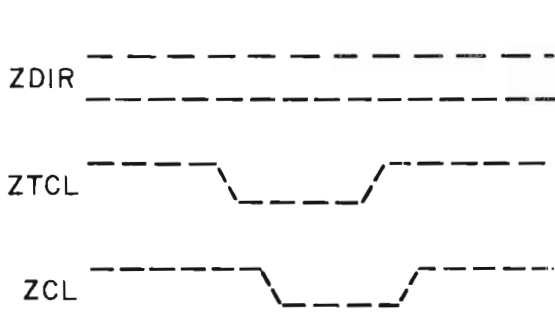
zdir - unidirection control line that determines data direction of zd0 thru zd7. This line is driven by the 6809.

ztcl - unidirectional control line used to signal that data sent by the Z80 is valid and data received by the Z80 has been read. This line is driven by the Z80.

zcl - unidirectional control line used to signal that data sent by the 6809 has been read. This line is driven by the 6809.

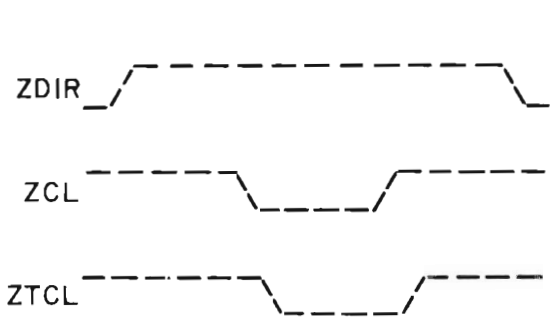
Bus timing diagrams for the different modes are as follows:

---1500 TO CELLULAR CONTROLLER COMMAND OR DATA TRANSFER---



- 1 - z80 checks for zdir low, zcl hi
- 2 - z80 sets ztci hi
- 3 - z80 sets data on zd0-zd7
- 4 - z80 sets ztcl low to signal data ready
- 5 - 6809 detects ztcl low
- 6 - 6809 reads byte from zd0-zd7
- 7 - 6809 sets zcl low to signal data accepted
- 8 - z80 detects zcl low
- 9 - z80 sets ztcl hi to signal data handshake
- 10 - 6809 sets zcl hi to complete transfer

---CELLULAR CONTROLLER TO 1500 DATA TRANSFER---



- 1 - 6809 checks for ztcl high
- 2 - 6809 sets zdir high (reverse data direction)
- 3 - 6809 sets data on zd0-zd7
- 4 - 6809 sets zcl low
- 5 - z80 detects zdir high and zcl low
- 6 - z80 reads data byte from zd0-zd7
- 7 - z80 sets ztcl low
- 8 - 6809 detects ztcl low, sets zcl high
- 9 - z80 detects zcl high, sets ztcl high
- 10 - 6809 sets zdir low

## 9-2-1 Cellular Controller PC Board Detailed Theory of Operation

### CPU

The 6809 CPU (U6525) controls the devices on the Cellular Controller PC Board (See Figure 9-1 and Cellular Controller Schematic). The CPU fetches an instruction from the ROM and then takes appropriate action, which may be changes in the data in its internal registers, in the RAM or in the I/O devices. After the appropriate action is executed, the next instruction is fetched from the ROM. This process continues as long as power is applied to the Cellular Controller PC Board.

Three control lines are used to interrupt the CPU: the  $\overline{\text{RESET}}$  line (pin 37), the  $\overline{\text{IRQ}}$  line (pin 3) and the  $\overline{\text{FIRQ}}$  line (pin 4). The  $\overline{\text{RESET}}$  line goes low when power is first applied to the PC Board. This is accomplished by U6516 A and B, R6520, CR6503 and C6534. When the  $\overline{\text{RESET}}$  line goes low, the CPU is initialized and starts fetching instructions from the initialization routine in the ROM. After initialization is complete, the task routines are accessed. When the  $\overline{\text{IRQ}}$  line goes low, the CPU accesses the interrupt routine after the current instruction is completed. The interrupt routine determines the source of the interrupt and services the device that sent the interrupt. Optionally, the  $\overline{\text{IRQ}}$  function may be disabled by setting the appropriate bit in the CPU's internal status register. The  $\overline{\text{FIRQ}}$  line acts in a manner similar to the  $\overline{\text{IRQ}}$  line, except that the  $\overline{\text{FIRQ}}$  has priority over  $\overline{\text{IRQ}}$ . For more information on the 6809, refer to the manufacturer's data sheet or data book.

### ROM

U6527 and U6532 (if installed in the X1 slot) are the ROM (Read Only Memory) ICs. These ICs contain instructions and look-up tables for the CPU. Jumpers are provided (JTB6505 and JTB6507) to allow expansion to larger ROMs. There are no provisions for writing to the ROMs. The ROMs are non-volatile, which means they retain their memory when power is removed.

### RAM

U6530 is the RAM (Random Access Memory). The RAM contains data which may be altered at will by the CPU. The RAM is a volatile device, which means its memory will be lost when power is removed.

### Address Decoder

The Address Decoder consists of U6526, U6533, U6534 and U6535. U6526 selects either one of three 16 K blocks of memory or one of the I/O devices. The 8000(H) to BFFF(H) output is used to enable U6533. U6533, in turn, may select one of the two VIA (Versatile Interface Adapters), one of the two counter/timers or it may enable U6534 and U6535. U6534 and U6535 select one of the remaining I/O devices. The appropriate device, or memory, is selected when its address is present on the address bus.

### Control Logic

The control logic consists of U6529 A, B and D and U6528 A, B and C. The control logic produces the  $\overline{\text{RD}}$ ,  $\overline{\text{WR}}$  and MEMEN signals, depending on the states of the R/ $\overline{\text{W}}$ , E and Q lines from the CPU. See Table 9-1 for control logic operation.

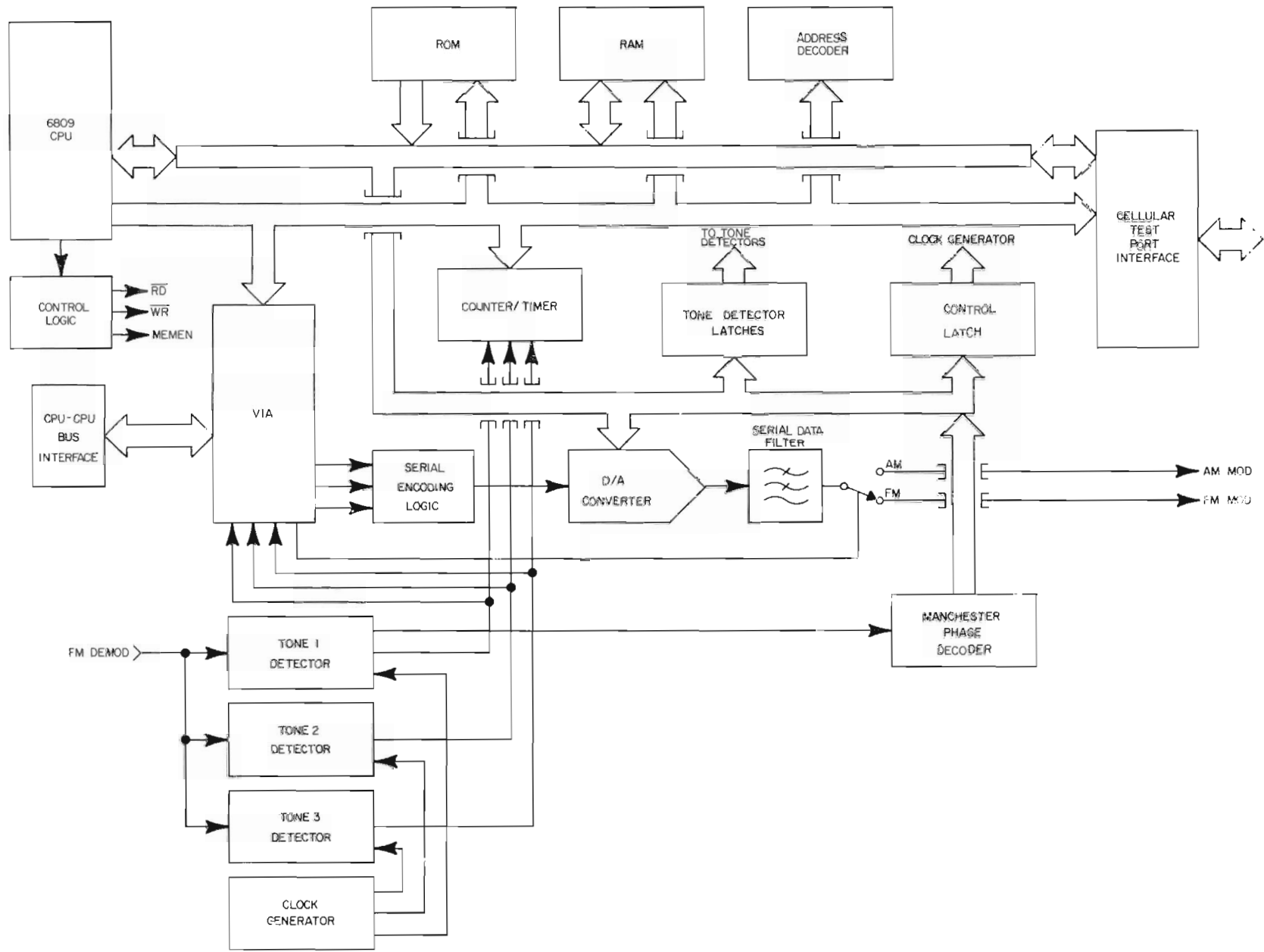


Figure 9-1 Cellular Controller PC Board Detailed Block Diagram

| E<br>U6525,<br>pin 34 | Q<br>U6525,<br>pin 35 | MEMEN<br>U6528C,<br>pin 8 | R/ $\bar{W}$<br>U6525,<br>pin 32 | $\bar{RD}$<br>U6529D,<br>pin 11 | $\bar{WR}$<br>U6529B,<br>pin 6 |
|-----------------------|-----------------------|---------------------------|----------------------------------|---------------------------------|--------------------------------|
| 0                     | 0                     | 0                         | 0                                | 1                               | 1                              |
| 0                     | 1                     | 1                         | 0                                | 1                               | 0                              |
| 1                     | 0                     | 1                         | 0                                | 1                               | 0                              |
| 1                     | 1                     | 1                         | 0                                | 1                               | 0                              |
| 0                     | 0                     | 0                         | 1                                | 1                               | 1                              |
| 0                     | 1                     | 1                         | 1                                | 0                               | 1                              |
| 1                     | 0                     | 1                         | 1                                | 0                               | 1                              |
| 1                     | 1                     | 1                         | 1                                | 0                               | 1                              |

Table 9-1 Control Logic Truth Table

#### CPU-CPU Bus Interface

The CPU-CPU Bus Interface consists of U6501, U6502, and U6504 thru U6509. U6505 and U6506 interface data, while U6507, U6508 and U6509 interface control information. U6501 and U6502 are address decoders for the Z80 CPU (on the CPU/MEMORY PC Board) side of the interface. The interface is accessed by the 6809 CPU through U6511, a 6522 VIA.

U6505 and U6506 are 8-bit latches which temporarily store data to be transferred between the CPUs. U6505 stores data which is transferred from the Z80 to the 6809. U6506 stores data which is transferred from the 6809 to the Z80.

U6507, U6508 and U6509 interface the control signals. U6507 and U6509 store control information which is transferred from the Z80 to the 6809. U6508 stores control information which is transferred from the 6809 to the Z80.

#### Cellular Test Port Interface

The Cellular Test Port Interface consists of U6516D, U6516E, U6519, U6512A, U6523, U6524, U6520, U6521 and U6522. U6520, U6521 and U6522 are line drivers/receivers. Each of these line drivers/receivers have four driver/receiver gates for a total of twelve driver/receivers. The mode (driver output or receiver input) is determined by U6516E, U6516F, U6501, U6512A and U6519. U6519 is a VIA which interfaces the twenty I/O lines and the counter and shift register. U6524 is a line receiver for the serial port and U6523 is a line driver for the serial port.

#### VIA

U6511, the VIA (Versatile Interface Adapter), interfaces the 6809 side of the interface adapter with the 6809 processor bus. The VIA also performs the serial data conversion, detects tones 1 thru 3 and selects AM or FM modulation for the serial data (cellular operation uses FM modulation only). The VIA also contains a parallel to serial converter and a 16-bit timer. For more information concerning the VIA, see the manufacturer's data sheet or data book.

### Serial Encoding Logic

U6512 B, C and D, U6513A and U6514A form the serial encoding logic. U6513A selects either the output of U6512D (NRZ data) or the output of U6512B (Manchester phase encoding). The output of U6513A is applied to a non-inverting amplifier, U6514A. The selected serial data is applied to the reference input of the D/A converter.

### D/A Converter

The D/A converter determines the modulation level of the serial data. The digital to analog converter, U6515, captures 8 bits of level information from the 6809 bus when instructed to do so by the address decoder. The D/A converter scales down the level of the serial data by a factor determined by the 8 bits of level information. U6514B converts the current out of U6515 to a voltage level which is fed to the serial data filter.

### Serial Data Filter

The serial data filter consists of R6510, R6508, R6507, C6518, C6519 and C6520. This filter shapes the rising and falling edge of the serial data before it is modulated. U6513B routes the filtered serial data to the AM or FM modulator.

### Counter/Timer Circuit

The counter/timer circuit consists of U6531, U6517 and U6518. U6531 divides the 2 MHz processor clock by 2, 4, 8 or 16. The division factor is jumper programmable and is normally set to divide by 4. This setting produces a clock frequency of 500 kHz which is fed to U6517 and U6518. U6517 measures the duration of Tone 3 and counts the number of clock shifts for the Manchester phase decoder. U6518 measures the duration of Tone 1 and Tone 2. For more information concerning U6517 and U6518, see the manufacturer's data sheet or data book.

### Tone Detector Latches

The tone detector latches consist of U6562, U6563, U6564, U6565 and U6567. These latches capture tone detector information from the data bus when instructed to do so by the Address Decoder. U6562, U6563, U6564 and U6565 latch active filter frequency and circuit Q parameters. U6567 latches response time information for the tone detectors. U6568 converts the TTL output of U6567 to a 0 to 12 V swing.

### Control Latch

The control latch, U6566, captures clock information from the data bus when instructed to do so by the Address Decoder. The output of the control latch is applied to the clock generator.

### Clock Generator

The clock generator consists of U6569 thru U6572. U6569 is a 14-stage binary counter which produces output frequencies of 500 kHz, 250 kHz, 125 kHz, 62.5 kHz, 31.25 kHz, 15.625 kHz and 7.8125 kHz. CMOS switches U6570, U6571 and U6572 select one of these frequencies and apply the selected frequency to the applicable tone detector. U6570 selects a frequency for Tone detector #1. U6571 selects a frequency for Tone detector #2. U6572 selects a frequency for Tone detector #3. These CMOS switches are controlled by the control latch.



### Tone Detector #2 and #3

Tone detector #2 is used for SAT detection (5970, 6000 or 6030 Hz). Tone detector #3 is used for detection of a 1 KHz tone and is provided for future use. Tone detectors #2 and #3 are identical in operation. Therefore, only Tone detector #2 will be discussed. Tone detector #2 consists of U6552, U6553, U6541 A and C, U6554, U6555 and U6556. U6552 is a multiplying digital to analog converter, which controls the relative level into the active filter for minimum level detection. The active filter, U6553, is configured as a programmable bandpass filter. The output of U6553, pin 12, is applied to U6554 and U6555. U6554 is a squaring amplifier, the output of which is applied to the counter/timers. U6555 is a detector, the output (pin 7) of which is applied to CMOS switches U6541 A and C. These switches select the time constant of the detector. The output of the CMOS switches is applied to a comparator, U6556A. The comparator provides the VIA with a digital signal which indicates the presence of a tone.

### Tone Detector #1

Tone detector #1 is used for 10 KHz ST (Signalling Tone) detection. Tone detector #1 operates in the same manner as Tone detectors #2 and #3, with a few exceptions. The active filter, U6540, is configured as a bandpass filter when it is being driven by U6538. When the active filter is driven by U6537, the filter is configured as a lowpass filter. At the present time, software prevents U6537 from changing, keeping U6540 configured as a bandpass filter. The output of U6540 is applied to the detector, U6543. The unfiltered serial data is applied to the Manchester phase detector. The squaring amp for Tone detector #1 is in the Manchester phase decoding circuitry. All other aspects of Tone detector #1 are the same as Tone detectors #2 and #3.

### Manchester Phase Detector

The Manchester phase detector consists of U6541B, U6542, U6546A, U6547, U6548, U6549, U6550 and U6538. Serial data enters the Manchester phase detector at pin 15 of U6541B. U6541B selects a slow or fast time constant, depending on the baud rate. U6542 is a squaring amp, the output of which is applied to the shift register, U6549, to the clock separator, U6546A and U6547, and to the counter/timers. U6546A and U6547 form a clock separator and produce a data clock signal which is applied to the shift register, U6549, to the bit counter, U6548, and to the counter/timer through Q6502. The counter/timer will interrupt the processor every 8 bits so that the contents of the shift register can be latched into U6550. The latch signal is generated by the bit counter, U6548. The microprocessor can preset U6548 in order to synchronize it with the data stream. U6551 is provided to adjust the clock separator for a particular baud rate.

### **9-3 PERFORMANCE EVALUATION**

Performance evaluation for the Cellular option consists of accessing the Cellular Menu and executing all 50 commands. Procedures to be used are given in the Cellular Operator's Guide. If the Cellular commands fail to perform as specified, calibration should be checked and then troubleshooting should be undertaken.



- Connect Channel 1 Probe of Oscilloscope to junction of R6594 and R6553. Connect Channel 2 Probe of Oscilloscope to junction of collector of Q6502 and R6550. (See Figure 9-2).

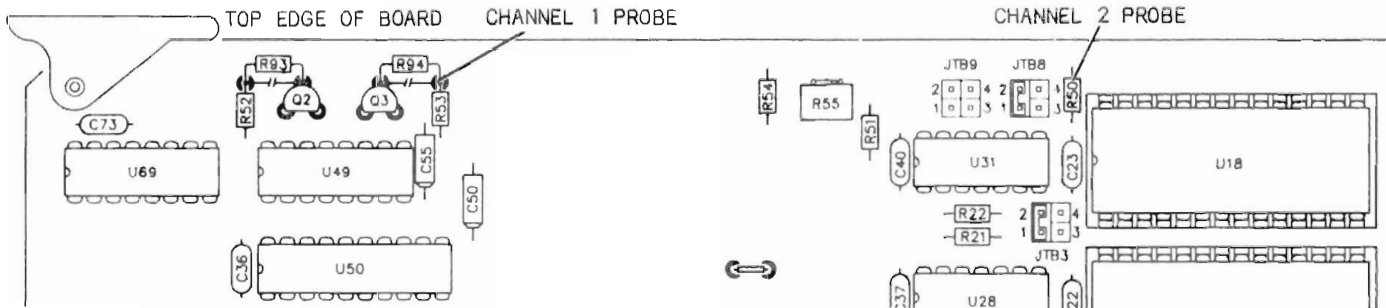


Figure 9-2 Cellular Calibration Test Points  
(Effective Ser. No. 2771 and on)

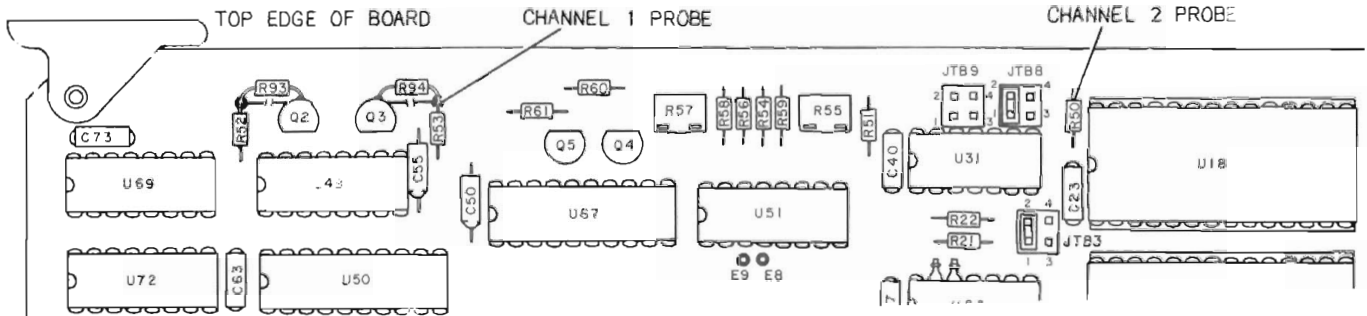


Figure 9-2a Cellular Calibration Test Points  
(Effective Ser. No. 1194 thru 2770)

- Trigger on positive edge of Channel 1 signal. Adjust R6555 so that duration of positive pulse on Channel 2 is 75  $\mu$ S. (See Figure 9-3).

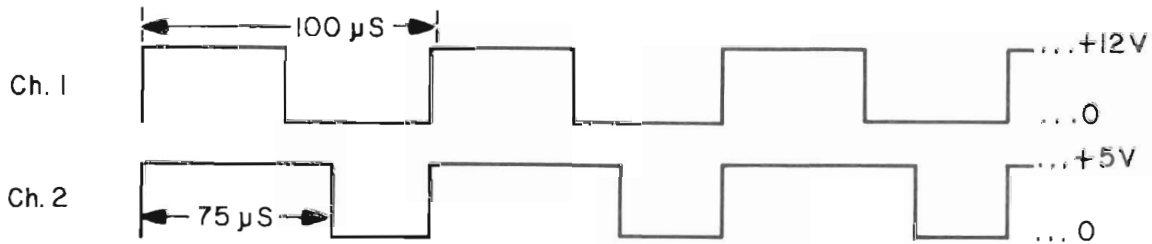


Figure 9-3 Cellular Pulse - Width Calibration

- Disconnect all test equipment.

## 9-5 TROUBLESHOOTING

Troubleshooting the Cellular Controller PC Board requires that the technician have a thorough knowledge of cellular theory. For convenience, two test ports (TP1 and TP2) have been provided on the PC Board. Pin numbers and the signals expected are given in Table 9-2. For those technicians having access to a storage Oscilloscope or a Logic Analyzer, Table 9-3 shows the data states to be expected for each of the 50 commands available in the Cellular Menu (refer to the Cellular Operator's Guide for discussion of the commands). Values of the data in Table 9-3 are given in hexadecimal form.

| Cellular Controller PC Board |                               |                                      |
|------------------------------|-------------------------------|--------------------------------------|
| Test Points                  | Signal                        | Notes                                |
| TP1-1                        | +12V power                    |                                      |
| -2                           | 1 MHz Clock                   |                                      |
| -3                           | 0 to +5V                      | Tone 2 Square Wave                   |
| -4                           | 0 to +5V                      | Tone 3 Square Wave                   |
| -5                           | 0 to +12V                     | Tone 2 Square Wave                   |
| -6                           | 0 to +12V                     | Tone 3 Square Wave                   |
| -7                           | 0 to +5V                      | Read Enable ( $\overline{RD}$ )      |
| -8                           | 0 to 5V                       | Tone 1 Square Wave                   |
| -9                           | 0 to +5V (active Low)         | 6 KHz Bandpass SAT detected          |
| -10                          | 0 to +12V                     | Tone 1 Square Wave                   |
| -11                          | 0 to +12V                     | Tone 2 Detected                      |
| -12                          | 0 to +5V (active Low)         | 10 KHz Bandpass ST detected          |
| -13                          | 0 to +5V (active Low)         | 1 KHz Bandpass (initialization only) |
| -14                          | 0 to +12V                     | Tone 1 Detected                      |
| -15                          | 0 to +12V                     | Tone 3 Detected                      |
| -16                          | 0 to +5V                      | Write Enable ( $\overline{WR}$ )     |
| -17                          | 10 Vp-p @ 8 KHz Dev.          | Tone 2 Filter Output                 |
| -18                          | 0 to +5V                      | Memory Enable (MEMEN)                |
| -19                          | 0 to +5V, 75 uS pulse         | Received data clock                  |
| -20                          | 0 to +5V                      | Manchester encoded data              |
| -21                          | Variable from 0 to $\pm 2.5V$ | Leveled, Filtered AM Data            |
| -22                          | 0 to +5V                      | Generated Serial Data                |
| -23                          | Variable from 0 to $\pm 2.5V$ | Leveled, Filtered FM Data            |
| -24                          | 10 KHz                        | Shift Clock for Generated Data       |
| -25                          | 0 to +5V                      | NRZ                                  |
| -26                          | 0 to +5V                      | Either Manchester or NRZ             |

Table 9-2 Cellular Controller PC Board Test Points

| Cellular Controller PC Board |                                |  |
|------------------------------|--------------------------------|--|
| Test Points                  | Signal                         | Notes  |
| TP2-1                        | 0 to +5V                       | Rectified Tone 3                             |
| -2                           | @ +1.5V is change state        | Frequency Selector (Tone 3)                  |
| -3                           | 10 Vp-p @ 5 KHz Dev.           | Tone 3 Filter Output                         |
| -4                           | @ +1.5V is change state        | Frequency Selector (Tone 1)                  |
| -5                           | Not Used                       |  |
| -6                           | 0 to +5V                       | Rectified Tone 1                             |
| -7                           | Not Used                       |  |
| -8                           | HI-Cellular; LO-future use     | Data Rate Select                             |
| -9                           | 125 KHz                        | Tone 3 Filter Clock                          |
| -10                          | 0 to +5V                       | Rectified Tone 2                             |
| -11                          | 1 MHz                          | Tone 2 Filter Clock                          |
| -12                          | 0 to +5V                       | Tone 1 Square Wave Inverted                  |
| -13                          | 80 mV per KHz                  | Buffered FM Demod                            |
| -14                          | @ +1.5V is change state        | Frequency Selector (Tone 2)                  |
| -15                          | 0 to +5V (High Active)         | Data Detect Low Pass Level Output (not used) |
| -16                          | 10 Vp-p @ 8 KHz Dev.           | Tone 1 Filter Output                         |
| -17                          | 0 to +5V (High Active)         | Data Detect Bandpass Level Output            |
| -18                          | Variable from 0 to $\pm 2.5V$  | Level Controlled Data                        |
| -19                          | +5V power                      |  |
| -20                          | 1 MHz                          | Tone 1 Filter Clock                          |
| -21                          | GND                            |  |
| -22                          | +12V pulses                    | Edge Detector                                |
| -23                          | 80 mV per KHz                  | FM Demod from Demod Audio PC Bd              |
| -24                          | Mobile Under Test RSSI Voltage | Proportional Voltage                         |
| -25                          | -12V power                     |  |
| -26                          | @ -2.5 to +2.5V                | Level Shifted Data                           |

Table 9-2 (Continued) Cellular Controller PC Board Test Points

| Test Command Number | (command, number, ndbs, ndbr) | (OP, AB, RB)   |
|---------------------|-------------------------------|----------------|
|                     | Z80 to 6809                   | 6809 to Mobile |
| 1                   | 01,00,00                      | 1F,00,00       |
| 2                   | 02,00,00                      | 3F,00,00       |
| 3                   | 03,00,04                      | 5F,00,03       |
| 4                   | 04,00,00                      | 7F,00,00       |
| 5                   | 05,01,02                      | FF,01,01       |
| 6                   | 06,00,00                      | 80,00,00       |
| 7                   | 07,00,00                      | 81,00,00       |
| 8                   | 08,00,00                      | 82,00,00       |
| 9                   | 09,02,00                      | 83,02,00       |
| 10                  | 0A,01,00                      | 84,01,00       |
| 11                  | 0B,00,00                      | 85,00,00       |
| 12                  | 0C,00,00                      | 86,00,00       |
| 13                  | 0D,00,00                      | 87,00,00       |
| 14                  | 0E,00,00                      | 88,00,00       |
| 15                  | 0F,00,00                      | 89,00,00       |
| 16                  | 10,00,00                      | 8F,00,00       |
| 17                  | 11,00,00                      | 90,00,00       |
| 18                  | 12,00,01                      | 91,00,00       |
| 19                  | 13,00,01                      | 9C,00,00       |
| 20                  | 14,00,01                      | 92,00,0A       |
| 21                  | 15,00,01                      | 93,00,05       |
| 22                  | 16,00,21                      | 94,00,20       |
| 23                  | 17,00,03                      | 95,00,02       |
| 24                  | 18,00,05                      | 96,00,04       |
| 25                  | 19,02,02                      | 97,02,01       |
| 26                  | 1A,00,00                      | 98,00,00       |
| 27                  | 1B,00,00                      | 99,00,00       |
| 28                  | 1C,00,00                      | 9A,00,00       |
| 29                  | 1D,00,00                      | 9B,00,00       |
| 30                  | 1E,00,00                      | 9D,00,01       |
| 31                  | 1F,00,03                      | 9E,00,02       |
| 32                  | 20,01,00                      | A0,01,00       |
| 33                  | 21,00,00                      | A1,00,00       |
| 34                  | 22,06,01                      | A2,06,00       |
| 35                  | 23,00,00                      | A3,00,00       |
| 36                  | 24,00,00                      | A4,00,00       |
| 37                  | 25,00,00                      | A5,00,00       |
| 38                  | 26,00,00                      | A6,00,00       |
| 39                  | 27,00,00                      | A7,00,00       |
| 40                  | 28,00,66                      | A8,00,65       |
| 41                  | 29,65,00                      | A9,65,00       |
| 42                  | 2A,01,00                      | AA,01,00       |

Table 9-3 Data States for Cellular Commands



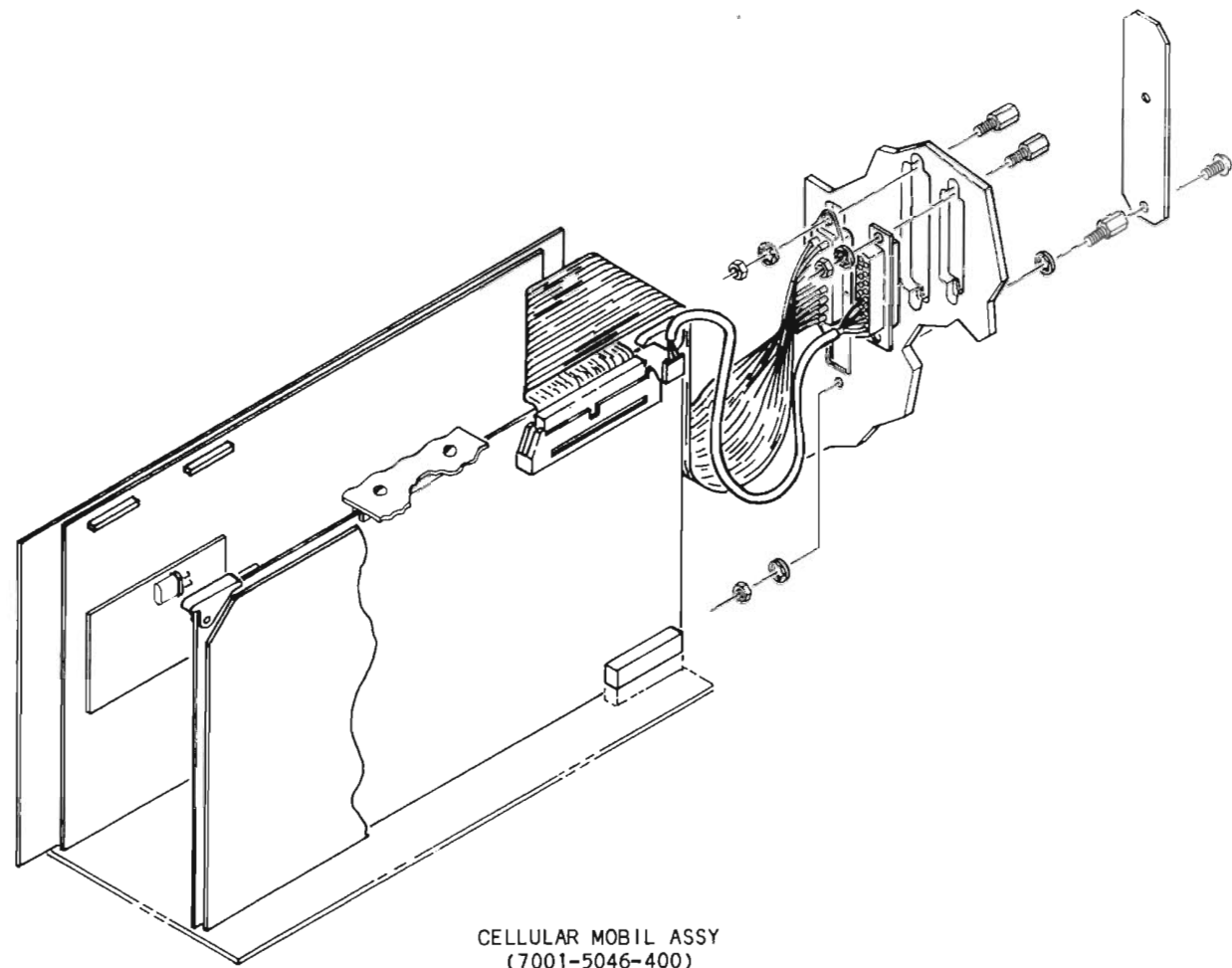
|   |   |                      |
|---|---|----------------------|
| 43  | 2B,00,00  | AB,00,00             |
| 44  | 2C,ndbs,ndbr,(data)   | (OP,AB,RB)           |
| <p>The data is dependent upon whether a response is required (ndbr &gt; 0) and/or whether data is to be sent to the mobile (ndbs &gt; 0). The (data) for this command is as follows:</p> <p>data #1 - OP for auxiliary command<br/> data #2 - AB for auxiliary command (additional bytes)<br/> data #3 - RB for auxiliary command (returned bytes)</p> <p>The ndbs is equal to the AB plus 3 (OP,AB,RB).<br/> The ndbr is equal to the RB (return all data to the Z80).</p> |   |                      |
| 45  | initiate - 2D,0D,00<br>status - 4D,00,01<br>halt - 6D,00,00 | none<br>none<br>none |
| 46  | initiate - 2E,0D,00<br>status - 4E,00,01<br>halt - 6E,00,00 | none<br>none<br>none |
| 47  | initiate - 2F,0D,00<br>status - 4F,00,01<br>halt - 6F,00,00 | none<br>none<br>none |
| 48  | 30,19,00  | none                 |
| 49  | initiate - 31,00,00<br>halt - 51,00,00                      | none<br>none         |
| 50  | 32,01,00  | none                 |

Table 9.3 (Continued) Data States for Cellular Commands

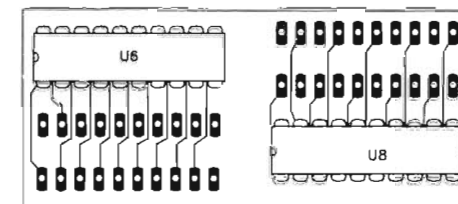
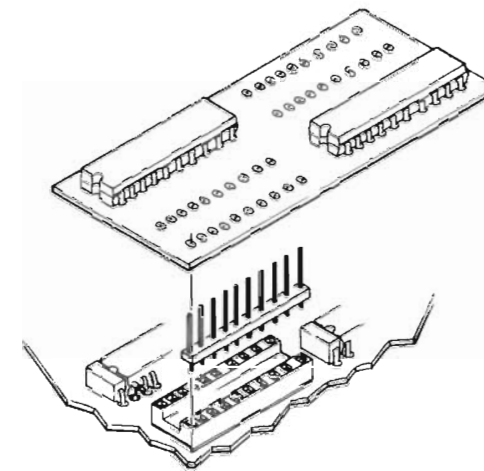
## 9-6 MECHANICAL ASSEMBLIES/PC BOARDS

The following mechanical assemblies/PC Boards constitute the cellular option:

| Figure | Title                        | Page |
|--------|------------------------------|------|
| 9-4    | Cellular Controller PC Board | 9-19 |
| 9-5    | ICD-1500 Test Box            | 9-21 |



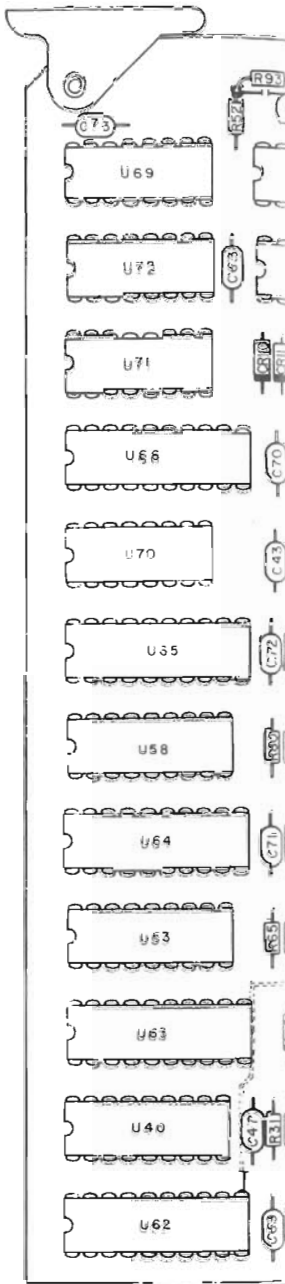
DETAIL **A**



DETAIL **B**

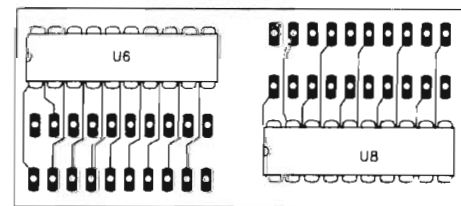
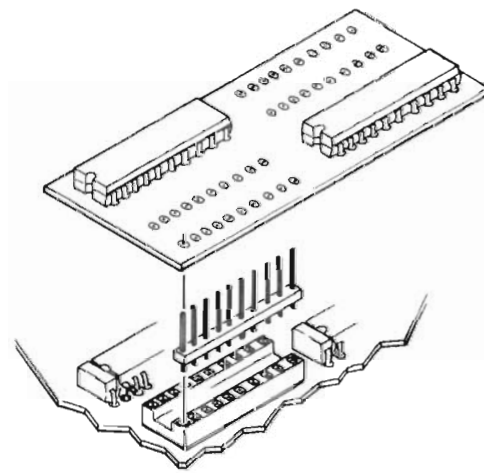


DETAIL **C**

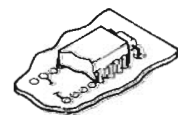




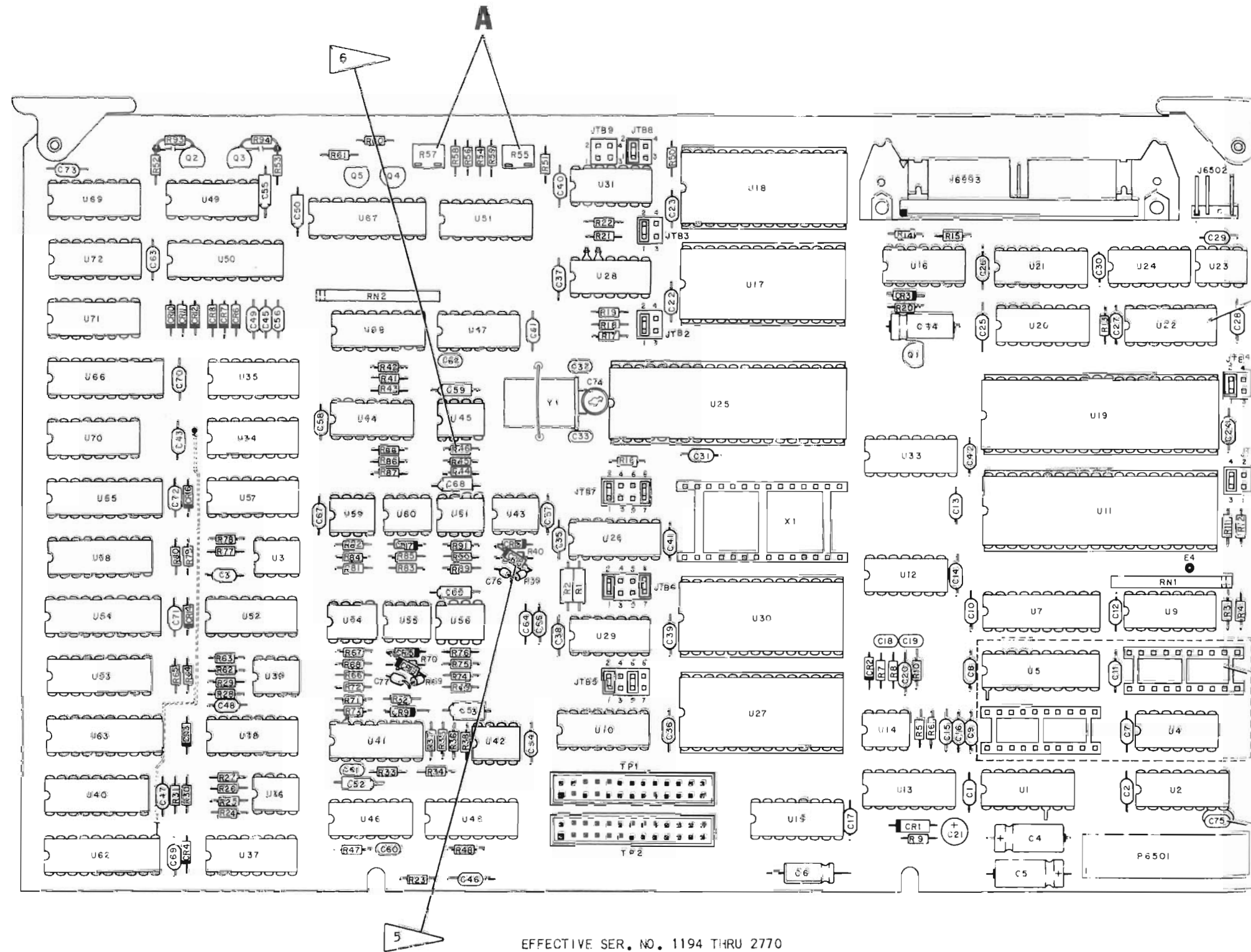
DETAIL A



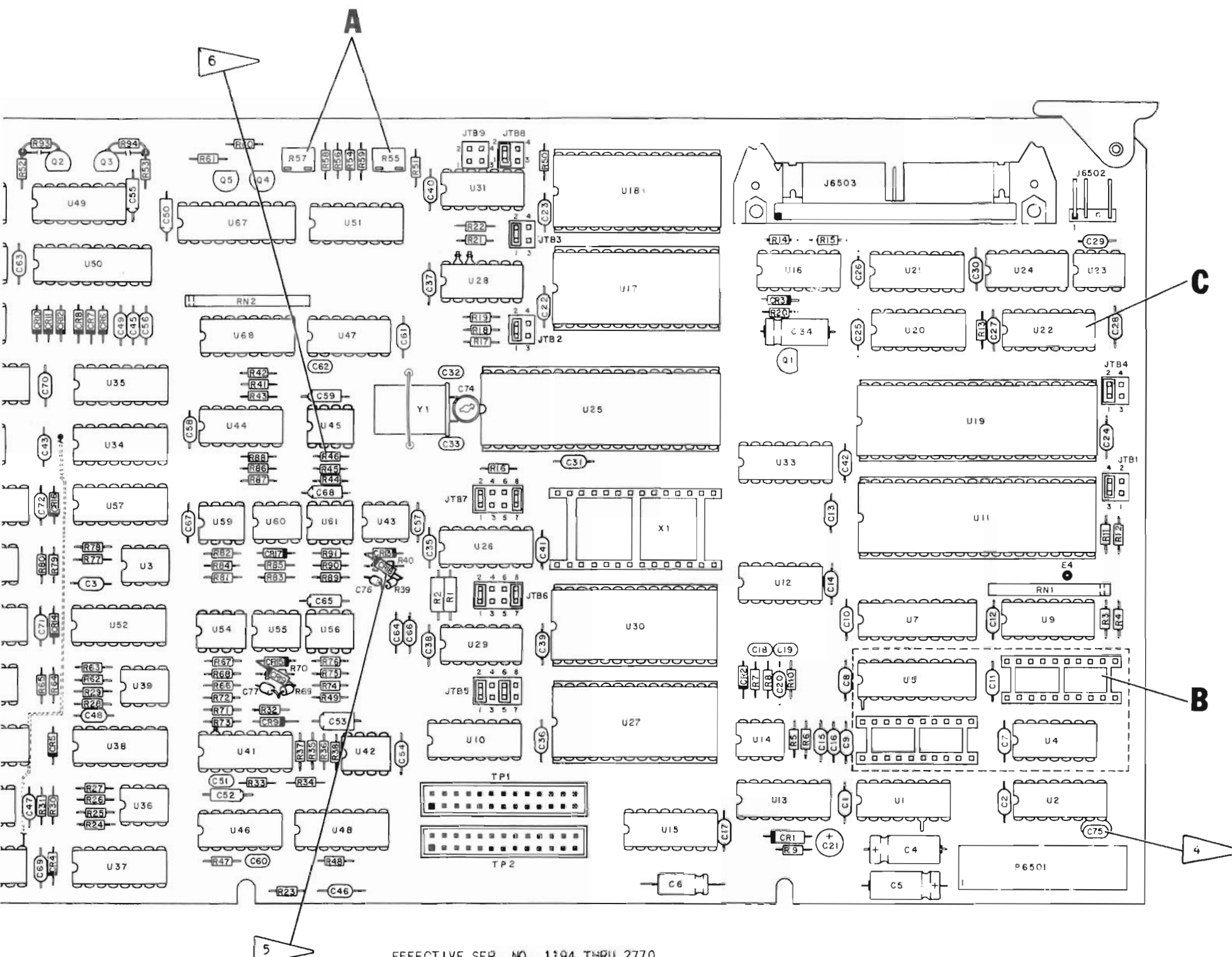
DETAIL B



DETAIL C



EFFECTIVE SER. NO. 1194 THRU 2770



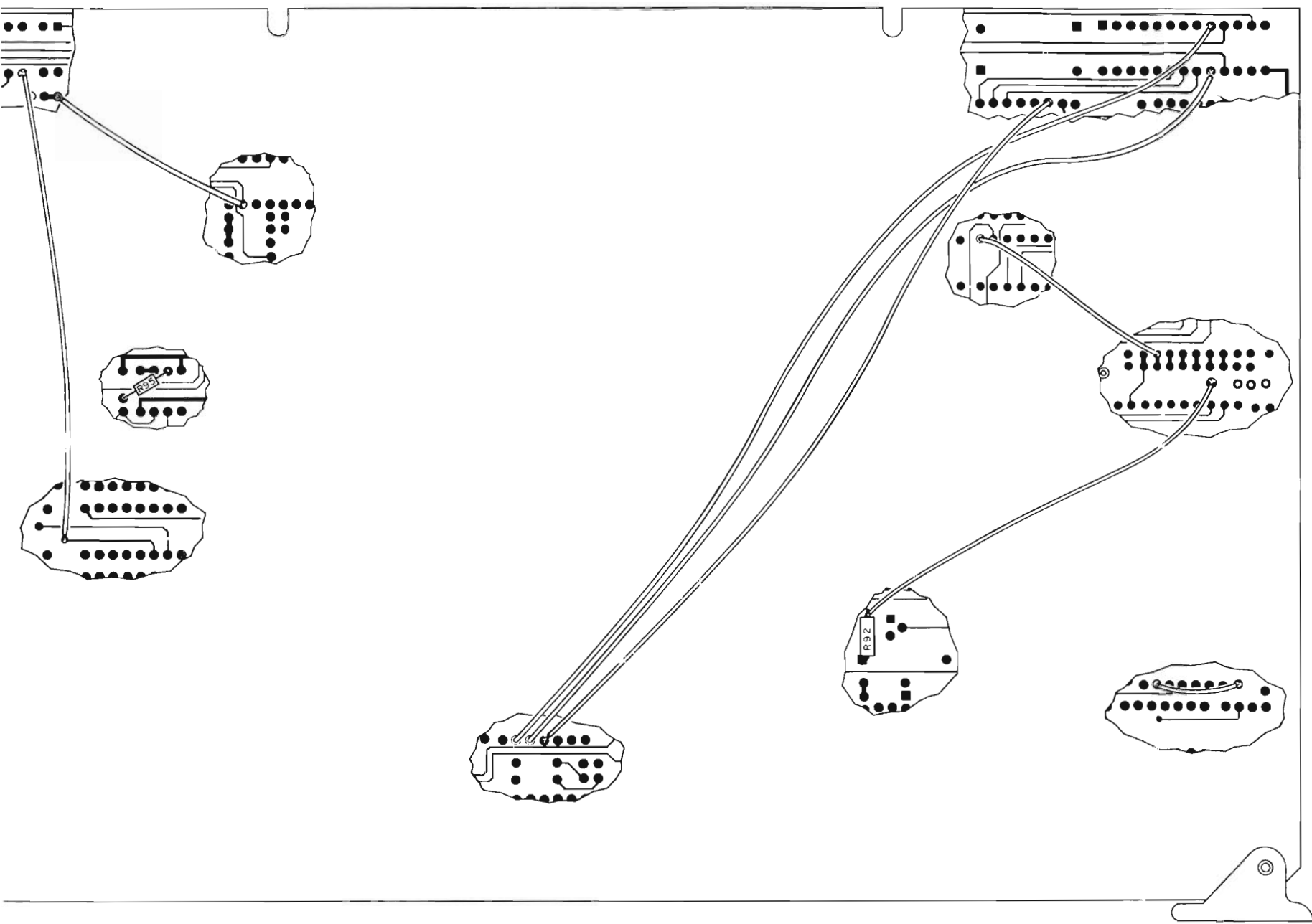
EFFECTIVE SER. NO. 1194 THRU 2770

NOTES:

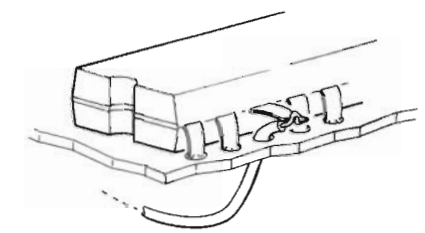
PC BOARD

1. THE REF DES SERIES FOR THE CELLULAR CONTROLLER PC BOARD IS 6500 AND 6600 (E.G., R1 IS R6501 AND R100 IS R6601).
2. DATA PART NO. 7010-5036-600.
3. REF CIRCUIT SCHEMATIC 0000-5016-600.
4. EFFECTIVE SER. NO. 2002, C75 ADDED.
5. EFFECTIVE SER. NO. 2334, CR18, CR19, C76 AND C77 ADDED.
6. R46 SELECTED AT TEST (SAT); NOMINAL 680 OHMS, RANGE 560 THRU 1K OHMS.

Figure 9-4 Cellular Controller PC Board (Sheet 1 of 4)

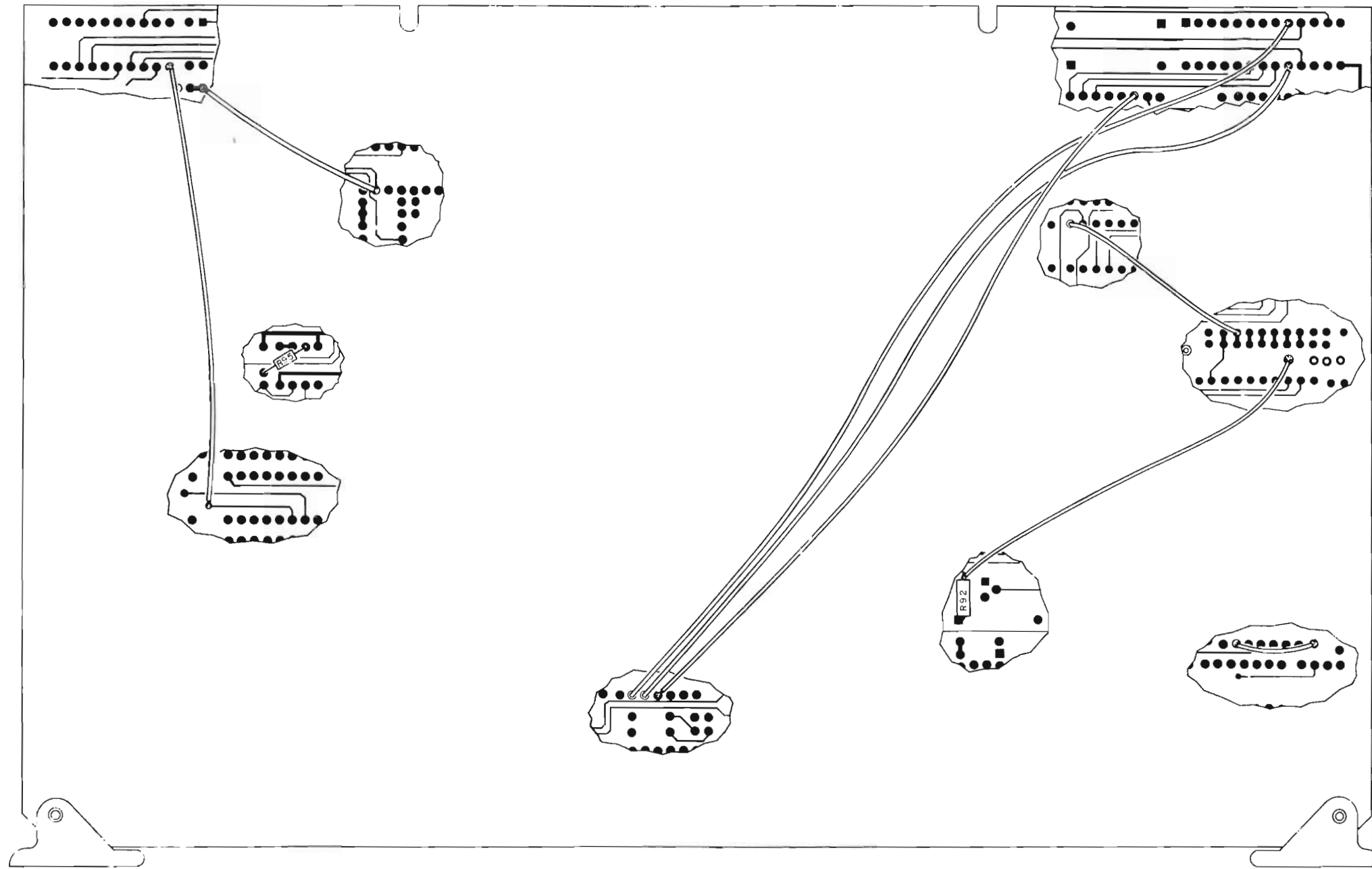


EFFECTIVE SER. NO. 1194 THRU 2770



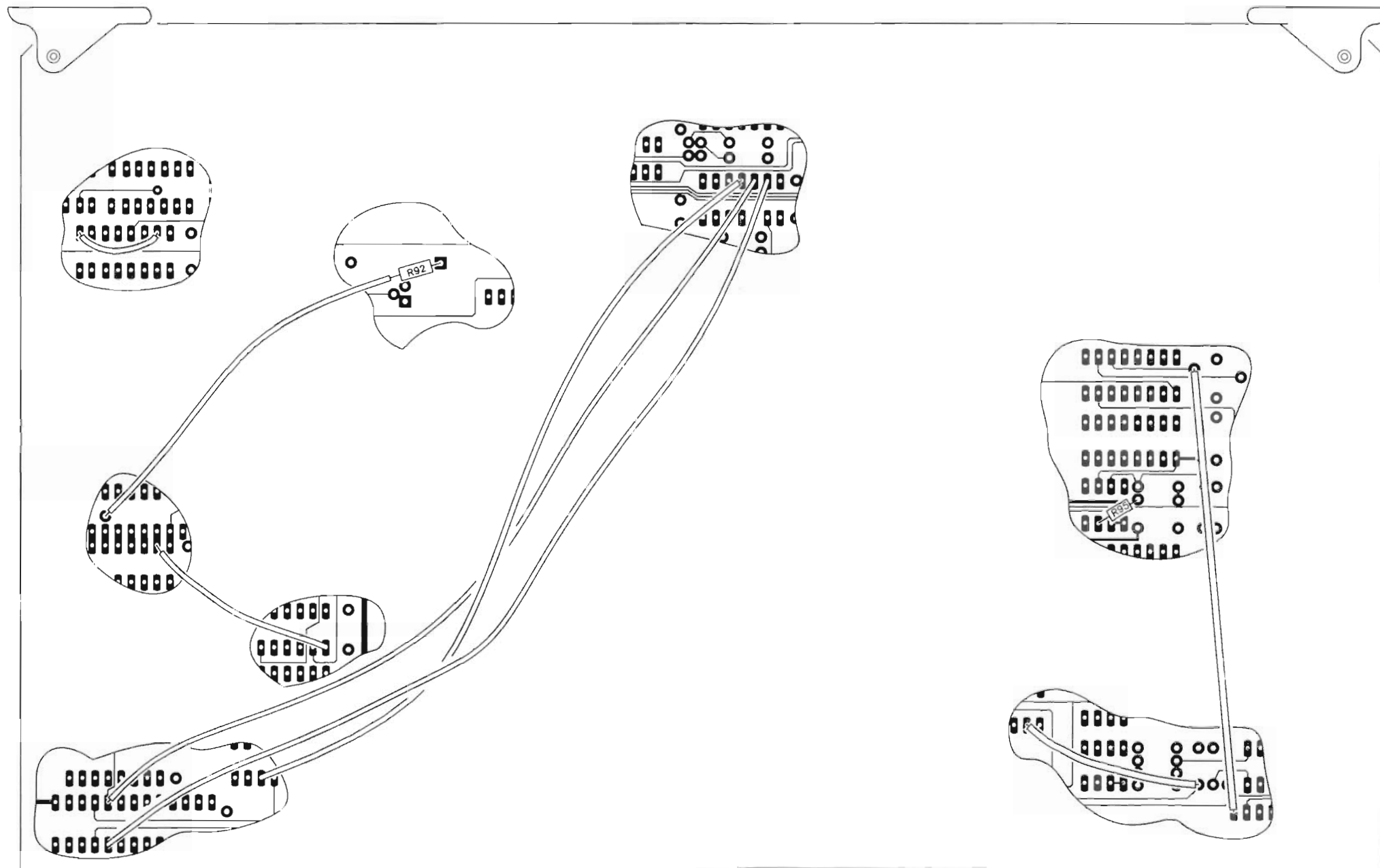
TYPICAL FOR THRU-BOARD JUMPERS  
**DETAIL A**

Figure 9-4 Cellular Controller PC Board  
 (Sheet 2 of 4)



EFFECTIVE SER. NO. 1194 THRU 2770

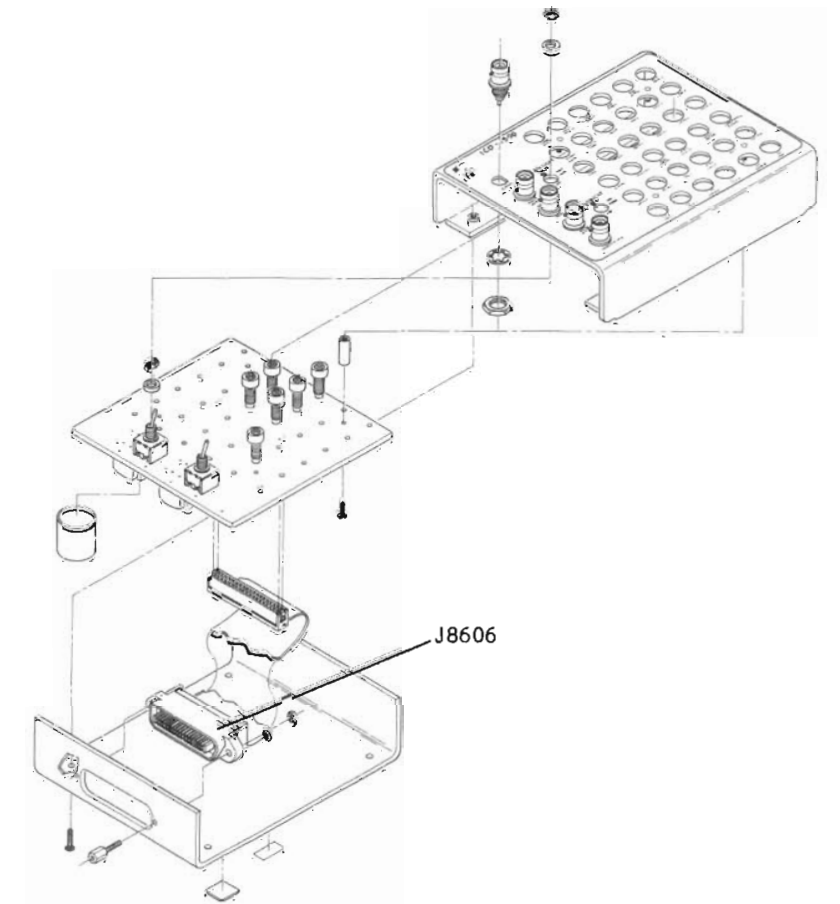
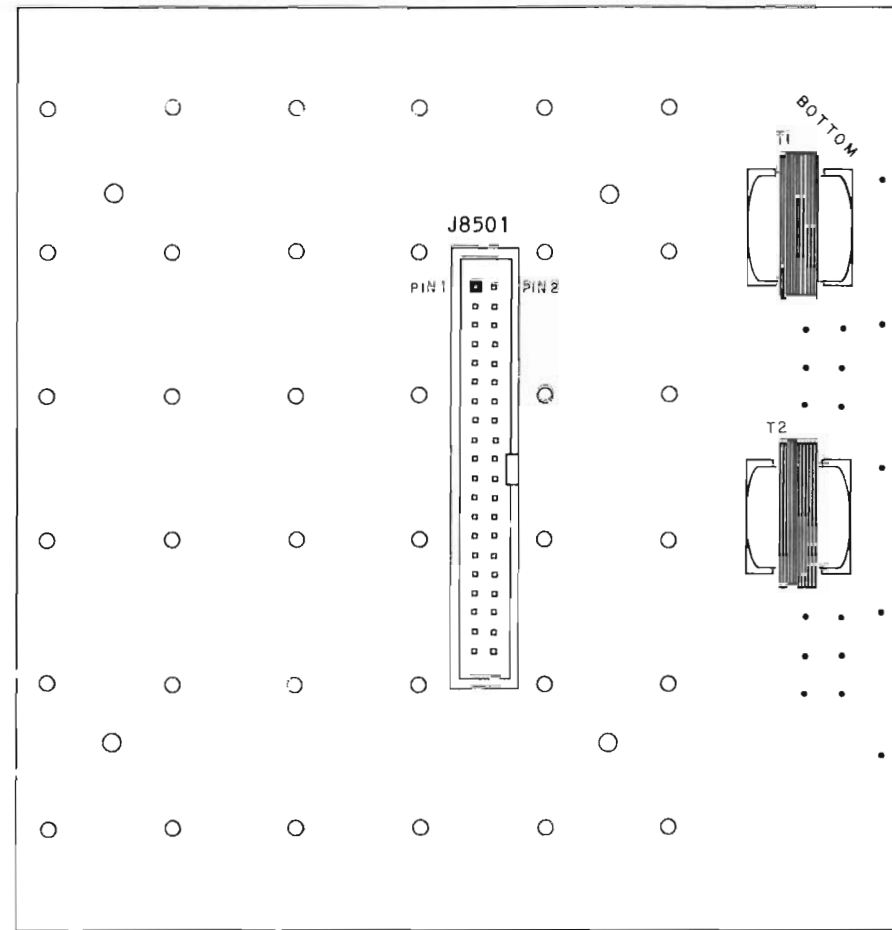
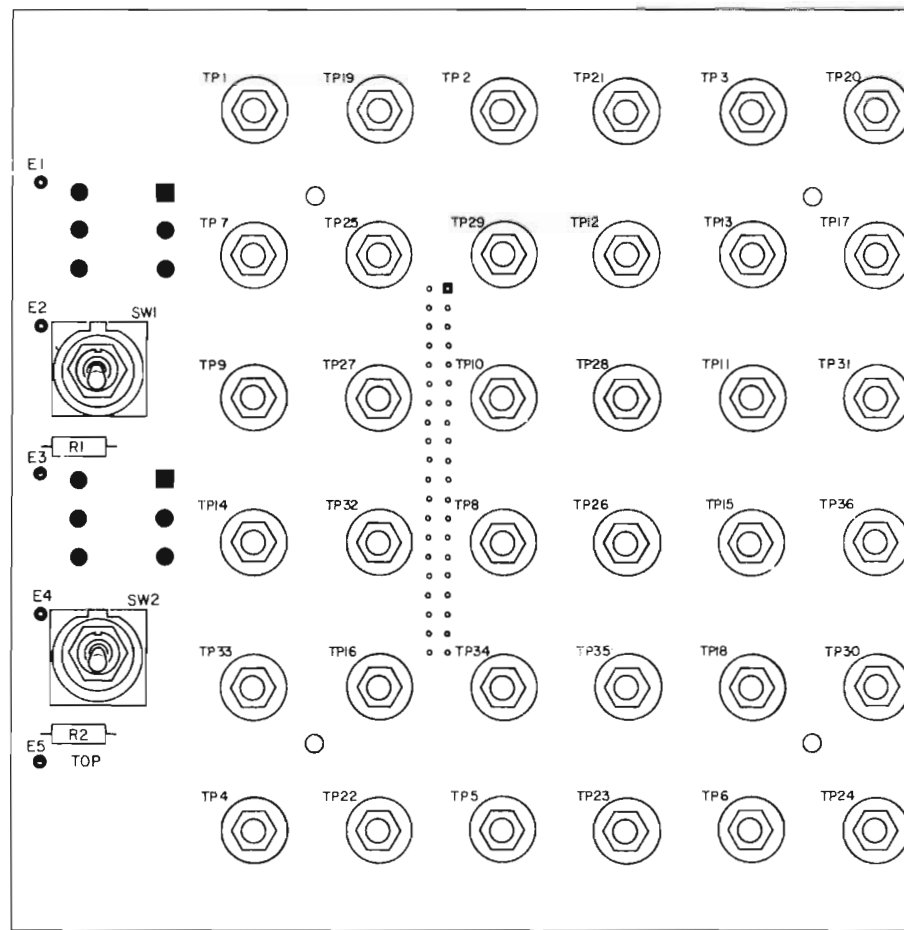
Figure 9-4 Cell (St)



EFFECTIVE SER. NO. 2771 AND ON

Figure 9-4 Cellular Controller PC Board  
(Sheet 4 of 4)





NOTES:

MECH ASSY

1. THE REF DES SERIES FOR THE ICD-1500 TEST BOX IS 8600 (I.E., J1 IS J8601).
2. DATA PART NO. 7005-5047-100.
3. REF CIRCUIT SCHEMATIC 0000-5017-100.

PC BOARD

1. THE REF DES SERIES FOR THE ICD-1500 PC BOARD ASSY IS 8500 (I.E., R1 IS R8501).
2. DATA PART NO. 7010-5037-100.
3. REF CIRCUIT SCHEMATIC 0000-5017-100.

Figure 9-5 ICD-1500 Test Box (Part of Option 10)