10 Volt Programmable Josephson Voltage Standard Circuits Using NbSi-Barrier Junctions

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***Abstract*—Programmable Josephson voltage standard (PJVS) circuits were developed that operate at 16 GHz to 20 GHz with operating margins larger than 1 mA. Two circuit designs were demonstrated, each having a total of ∼ 300,000 junctions, which were divided into either 16 or 32 sub-arrays. Triple-stacked junctions were used in order to fit the ∼300,000 junctions on each circuit. The amorphous Nb_xSi_{1-x}-barrier junction technology provided a high degree of uniformity of the barrier and junction electrical properties, which was necessary to achieve the 1 mA operating margin. Although the margins on both the 16-array and 32-array circuits were much greater than 1 mA, the circuit yield for the 16-array design was lower because the longer arrays are more sensitive to defects. The use of lumped-element microwave splitters and tapered arrays significantly reduced the microwave input power and increased the operating margins of these designs. In addition, the broadband microwave response of the designs allowed the PJVS output voltage to be continuously adjusted by using the microwave frequency while remaining on margins.**

***Index Terms*—Josephson arrays, SNS devices, superconducting device fabrication.**

I. Introduction

THE programmable Josephson voltage standard (PJVS) is becoming the building block of electrical metrology because of its flexibility, features, and inherent voltage stability. New applications for Josephson voltage metrology, including power calibrations and Watt balance experiments, have augmented voltage standard calibrations as PJVS measurement techniques have developed [1]. Because of the large number of junctions and their dissipative nature, the PJVS circuit is also one of the more challenging superconductive electronic circuits to produce.

The basis of PJVS operation is that arrays of microwave-biased Josephson junctions (JJs) are dc-current-biased from the zero-voltage step to the first constant-voltage step with a set of programmable sources. The microwaves are split to capacitively drive the arrays in parallel, while the arrays are series connected through low-pass superconductive filters to sum their respective voltages. There is a limit to the maximum number of JJs in a single array, which is based on the attenuation and/or distortion of the incoming microwaves; this limit is typically several thousand JJs and depends on junction normal-state resistance and transmission line impedance [2], [3]. There is also a limit to the maximum number of microwave splits that is based on the chip area needed for the splits and the total input power available.

Manuscript received August 03, 2010; accepted September 14, 2010. Date of publication October 28, 2010; date of current version May 27, 2011. This work was supported by the National Institute of Standards and Technology.

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Digital Object Identifier 10.1109/TASC.2010.2079310

TABLE I
DESIGN SUMMARY

Parameter	16-way	32-way
Junctions	249,600	268,800
JJs/array	15,600	8,400
Splitter Stages	4	5
Frequency (10V)	19.37 GHz	17.99 GHz
Taper Z (start)	85 Ω	50 Ω
Taper Z (end)	18.5Ω	23 Ω

II. Design

There are presently three different laboratories working on 10 V PJVS systems, each with their own design: a PTB design with 69,632 junctions based on 70 GHz microwaves [4], an AIST system with 327,680 junctions biased at 16 GHz and 10 K with NbN [5], and a NIST system using 268,800 junctions that operates at 18 GHz [6]. All of these systems balance various design considerations to maximize the operating margins, which is the dc current range over which the array maintains a constant voltage, or "flat step". An array should have the largest possible number of junctions in order to maximize the total voltage produced by the array. Unfortunately, an array with too many junctions leads to reduced current margins, from either undesirable attenuation of the microwave power within the array, or nonuniformity in the junctions.

An important design consideration is the number of arrays and splitters used to divide the microwave power, which will depend on the available power, the power required to achieve the largest current range, and the junction attenuation. Because the total number of JJs required to produce 10 V is inversely proportional to the chosen bias frequency, the number of JJs per array can be reduced to increase the current margin, but this requires more splitters and simultaneously increases the total power required.

NIST has designed two 10 V PJVS circuits that use either 16-way or 32-way division of the microwaves. Both designs were fabricated to experimentally determine the design that would produce the system with the best performance. The designs are summarized in Table I. For the microwave splitting stage, each design uses a two-way Wilkinson divider [7] to drive coplanar waveguide (CPW) transmission lines. The CPW transmission line has tapered impedance such that each junction

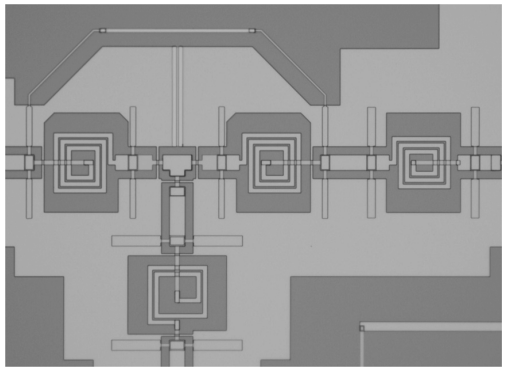

Fig. 1. Micrograph of a lumped element Wilkinson splitter. The microwaves enter through the bottom and are split equally. The section on the right is a 90° phase shifter.

in the transmission line receives a nearly identical microwave current—partially compensating for the loss from junction dissipation [8].

Because a JJ is a current-driven device, it is important to keep the microwave current, but not necessarily the power, constant for each JJ in the array. The maximum 85 Ω impedance, which should be as large as possible for the 16-way circuit, is limited by the largest practical impedance for a CPW on a Si substrate. Since the 32-way design required fewer JJs per array, the taper impedance range was smaller than that of the 16-way design. By starting the 32-way design at 50 Ω, the applied microwave power to the chip is nearly the same as the power required to drive a 16-way design. Even though there are half as many arrays in the 16-way design, the applied power to the entire circuit is only 85% of the input power to the 32-way circuit, because of the higher 85 Ω input impedance.

In an effort to reduce the required microwave power while still maintaining an operating current range greater than 1 mA, we have reduced from 13 mA to 9 mA the critical current of the JJs compared with lower-voltage NIST PJVS designs. Larger critical currents lead to a larger current range on the constant-voltage step. However, the required microwave power also scales as the square of the critical current. For these circuits, the critical current was kept below 10 mA.

At some point, the applied power is too much for the circuit to operate at the 4 K bath temperature. For our circuits, this power is on the order of 300 mW, and includes both DC and microwave power dissipated on chip. At applied powers greater than this, the chip warms above the bath temperature, and the current range of the voltage step decreases. To reduce the circuit temperature, we have maximized the thermal transfer from the circuit to the chip by fabricating the junctions directly on the Si by use of trenches in the wafer native oxide [9].

The heart of the microwave design is the lumped-element Wilkinson splitter shown in Fig. 1 [10], [11]. The 50 Ω input CPW goes through a 42 Ω quarter-wave section before being split into two 60 Ω quarter-wave sections. Rather than using valuable chip area on quarter-wave sections, lumped element C-L-C pi sections are used for the characteristic impedance and phase shift. There is also a 100 Ω shunt across the outputs to absorb out-of-phase reflections from the output.

Another microwave trick is the use of 90° phase shifters on one of the arms of the Wilkinson splitter to cancel any reflections from down-stream elements. If both arms of the splitter drive identical elements, any reflection from mismatches will arrive back at the Wilkinson splitter 180° out of phase and cancel. This phase shifter is also implemented as a C-L-C pi section with 50Ω impedance.

III. Fabrication

The fabrication of these devices is similar to that previously published [12]. Three inch wafers are oxidized with 150 nm of dry oxide to form the substrate. Holes in the oxide are lithographically patterned and etched to form trenches that enhance the heat transfer from the junction arrays to the substrate. After stripping the resist and *in situ* argon plasma cleaning, a multilayer film is sputtered with Nb electrodes and $\mathrm{Nb_xSi_{1-x}}$ barriers. The barriers may be tuned from an insulator to a metal by changing the Nb content, x [12]. For PJVS circuits we tune the junctions to work at either 70 GHz for the PTB PJVS system [13], or 20 GHz for the NIST designs. For the circuits described here, we used a 3-junction stack with barrier composition of approximately 20 at.% Nb, resulting in a low temperature barrier resistivity of $\sim 700\,\mu\Omega\cdot\mathrm{cm}$. The base Nb electrode is designed to be 380 nm thick, the middle Nb electrodes are each 70 nm, and the Nb counter electrode is 195 nm. The barriers are each 31 nm thick to yield junctions with a critical current density of $0.2\mathrm{mA}/\mu\mathrm{m}^2$. The planar junction geometry is a $3.5\,\mu\mathrm{m}\times 11\,\mu\mathrm{m}$ rectangle on a $16\,\mu\mathrm{m}$ wide base electrode embedded in a tapered CPW with a stack spacing of $6.5\,\mu\mathrm{m}$. The exact composition and thickness of the barrier were tuned slightly from these values to produce lower and higher critical current JJs, in order to find the optimal junction parameters.

The junctions are lithographically patterned and etched in an inductively coupled plasma reactive ion etcher with $\mathrm{SF_6}$ and $\mathrm{C_4F_8}$ plasma to give a vertical etch profile. An optical reflectance endpoint monitor is used to stop when the Nb base electrode is reached. The base electrode is separately patterned and etched. This base electrode-junction structure is covered in 380 nm of electron cyclotron resonance plasma vapor deposited $\mathrm{SiO_2}$. Vias are etched in the $\mathrm{SiO_2}$ to the junctions and base electrode. A 650 nm Nb wiring layer is deposited and patterned to define the CPWs and connect the junctions and a 120 nm thick PdAu resistor layer is deposited for shunts and terminations. The entire wafer is then covered with 300 nm of $\mathrm{SiO_2}$ for passivation. Vias are etched in the passivation for 250 nm thick PdAu pads, which are then deposited. Other than the junction stacks, all of the Nb films are etched in 100 % $\mathrm{SF_6}$ plasma with optical endpoint detection, which stops the etch when the reflectance changes upon reaching the underlying material. The $\mathrm{SiO_2}$ films are etched in a $\mathrm{CHF_3/O_2}$ mixture such that the sidewalls are sloped for higher critical current densities in the wiring layer. The PdAu films are deposited on the wafer with photoresist on the areas not to be metalized; these areas are subsequently lifted off.

IV. Measurements

Once chips are diced, preliminary measurements are done in a spring-finger probe at room temperature to determine whether the coupling and termination capacitors are not short-circuited. The chips are then cooled to 4 K and measured with and without

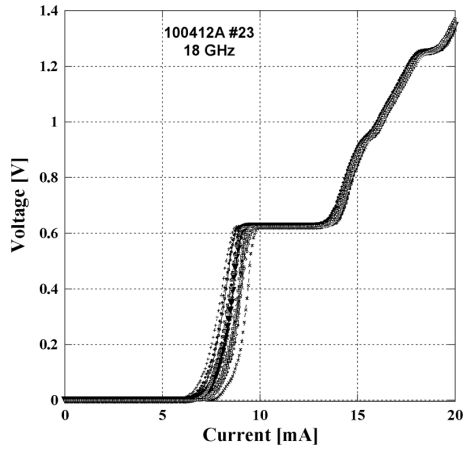

Fig. 2. Current-Voltage characteristics for all 16 array pairs of a 32-way 10 V PJVS chip driven with 18 GHz microwaves. All of the arrays show a broad constant voltage step at this microwave power. The critical current for this chip was 12 mA, which is larger than optimal.

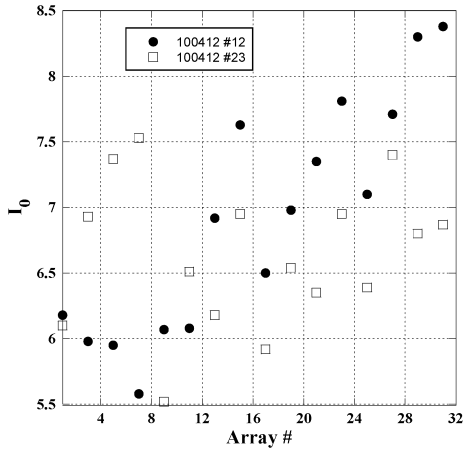

Fig. 3. The maxima of the zero-voltage steps for all pairs of arrays in two different chips from the same wafer. The distribution in the suppression of the critical current corresponds to approximately 2 dB in power.

microwave radiation to electrically characterize the JJs and arrays. High quality chips for 10 V PJVS are then flex-bonded [14], which are then mounted in the PJVS system cryoprobe.

A typical set of current-voltage (IV) characteristics for a 32-way design with 18 GHz microwave power applied is shown in Fig. 2. The constant-voltage step appears for all of the arrays with a broad current margin making this device suitable for a 10 V PJVS. In order to simplify the wiring of the test system and the data presentation, the figure shows 16 curves, each trace for two arrays in series. For this device, the critical current is 12 mA, and the normal-state resistance is 5.0 $\mathrm{m}\Omega$ per junction. Note that the constant-voltage steps significantly overlap, which demonstrates junction uniformity. However, overlapping the steps is not necessary for circuit operation because each array is independently biased with the 10V PJVS electronics.

In order to estimate the uniformity of microwave distribution across the chip, it is useful to extract the current range of the zero-voltage steps, which is a metric of the power driving a given array. The maximum current extent of the zero-voltage step, I_0, is plotted in Fig. 3 for each pair of arrays shown in Fig. 2 (open boxes) and another chip from the same wafer (closed circles). There is clearly some uneven distribution of power across the chip, with some arrays receiving more power than others, and there is an additional chip-to-chip variation. The apparent variation could be due to critical current uniformity, but that is measured from the dc IV curves to be better than 1% for all arrays. Nonetheless, the distribution is good enough to realize large steps throughout the entire chip.

As the power is increased, the zero-voltage step is further suppressed, and the one-step grows to some maximum. It is important to have enough power to maximize the one-step for optimum performance. For these devices with a 10 mA critical current, it takes nearly 500 mW applied power at the probe head to maximize the constant-voltage steps. Fortunately, this power is not hard to generate in the 20 GHz band. The microwave structures also are designed to handle the high applied power, particularly the first Wilkinson splitter in the divider chain. If the microwave current exceeds the critical current for the wiring, the structure will go normal and no longer deliver sufficient power to the arrays.

Because the voltage scales linearly with frequency, it is useful to have a design which has frequency agility. These circuits should work over a large bandwidth; the circuits are designed to work from 15 GHz to 25 GHz, although the semi-rigid coax that is used in the measurement probe attenuates strongly above 22 GHz. Fig. 4 shows the current margin of the constant-voltage step for all of the arrays on a chip as the frequency of the microwaves is stepped from 19 GHz to 21.5 GHz with a constant power of 26.9 dBm measured at the probe head. For this figure, we have defined the range of the constant voltage step as the current range over which the measured voltage is within 5 μV of the correct value. An indication that the microwave design of our circuit is optimized over the frequency range of this measurement is that there are no frequencies at which the margin suddenly decreases. However, the maximum current margin in an array is less than 2 mA for 9 mA critical current junctions, which indicates that further increases in operating margin may be possible.

V. Discussion

Our criterion for a "good" device is that the entire circuit must have at least 1 mA of current margin. Thus, the device in Fig. 4 is only "good" over a narrow frequency range around 19.8 GHz. One of the biggest challenges in making 10 V PJVS circuits is the yield of fabrication. Our approach to increasing yield is to first optimize the circuit design and junction design before attempting to fabricate large numbers of identical circuits. Clearly, if the maximum constant-voltage steps in Fig. 4 were larger, the current margins, the "good" operational bandwidth could be increased and the PJVS system would be more robust, but this should be done without increasing the critical current. Since each wafer produces 8 chips with two separate designs, we have been yielding nearly 2 "good" chips per wafer. This is expected to at least double when we eliminate one of the two circuit designs. The most common defects are either a small barrier defect or a microwave distribution defect that cause one of the arrays to have a non-flat step. The source of these defects is still under investigation.

Both designs, the 16-way and 32-way microwave split, have been fabricated and measured. It was found that both designs produced arrays with large (greater than 2 mA) constant

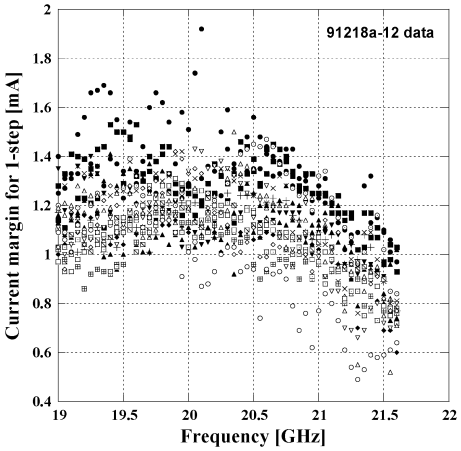

Fig. 4. The extent of the constant-voltage step for all pairs of arrays as a function of frequency. There is a narrow band over which the entire device has over 1 mA of margin, but a large band over which many of the arrays have margins greater than 1 mA. The different symbols correspond to 20 different arrays on the chip.

voltage steps. However, the likelihood of getting an entire chip of working arrays was much higher for the 32-way microwave split. We assume that this implies that the likelihood of a small defect causing catastrophic problems is greater in the 16-way designs because there are nearly twice as many junctions in the array. For this reason we have terminated the use of the 16-way design.

As seen in Figs. 2 and 3, another challenge in this circuit is the equal distribution of microwave power to each array. If arrays on one side of the chip are getting more power than the other, the optimized power will necessarily be somewhere in the middle so that the ends will not be optimal. More importantly, it will mean that the microwave power applied will need to be increased, which is undesirable and can approach the power limit of the input splitter. Because the splitters are designed from lumped-element microwave sections, we assume that the major difference between the designed elements and those fabricated is the targeting of the specific capacitance.

The original microwave designs were realized assuming a 300 nm thick SiO_2 layer, but were tested for reflection and transmission with a 350 nm oxide in a splitter/combiner structure that is not sensitive to distribution. Presently, we are fabricating chips with a 380 nm oxide to minimize the probability of short-circuited capacitors. This oxide has a specific capacitance that is too small for optimal microwave distribution. Initial attempts to simply scale the capacitor area have not worked. A redesign must be done using a full microwave simulation of the thicker oxide.

Work is also needed to optimize the current margins for a single array. For a critical current of 10 mA, we should be able to optimize the array for at least 3 mA of current margin on the constant-voltage step. This improved margin will translate directly into improving the current margins for the entire chip. Preliminary results have given over 2.5 mA for an 11 mA critical current junctions.

Another limitation of these designs for practical PJVS operation is that the minimum programmable voltage step is from a single array of 8400 JJs; there are no smaller subarrays. A new PJVS circuit design has been completed in which two of the 8400 JJ arrays are subdivided into seven smaller sections in a ternary division, such that the smallest subarray is six junctions. This new circuit will have 1400-times finer voltage resolution. By having two identical subdivided arrays, we retain the symmetry of the chip, which is useful for testing purposes. This design has not yet been fabricated.

VI. Conclusion

We have designed and fabricated 10V PJVS circuits, and demonstrated their operation with current margins greater than 1 mA. In order to simplify the microwave operation, we have designed these circuits to work with commercial sources over a frequency range of 16 GHz to 20 GHz. Challenges with microwave distribution, occasional non-flat steps, and fabrication yield have limited our present circuit yield to $\sim$25%. New designs with optimized microwave performance and arrays should increase the production yield. New designs with least significant bits will increase the system usability.

Acknowledgment

The authors thank A. Rüfenacht for assistance with software and instrumentation, and Zoya Popoviæ for microwave advice and graduate student guidance.

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