PIM1
Pulse and Frequency Input Module

The PIM1 Pulse and Frequency Input Module provides eight frequency or event counter inputs. Eight software-controlled ranges allow frequency measurements up to a maximum of 8MHz and down to a resolution of 1Hz. Seven of the inputs provide isolated (to 400V) or non-isolated TTL-compatible inputs, while an eighth channel has a non-isolated sensitivity of 200mV.

As a frequency counter, the seven TTL-compatible inputs provide measurements to 8MHz in the non-isolated mode, and to 2MHz in the isolated mode. The eighth input, which has 200mV sensitivity, measures frequencies up to 1MHz, non-isolated only.

As an event counter, the P1M1 module can count pulses at a maximum rate of 250kHz. Anti-coincidence circuitry ensures that the counter is not read in an undefined state and that no pulses will be lost. Inputs may also be configured as four dual input channels to allow events to be gated by external sources.

Software control selects input channel, input gating, gate times, and frequency/event mode. Gate times between 1048.576msec and 8.192msec allow a wide range of frequencies to be measured. Signals are connected directly to the module via on-card screw terminals.

The PIM1 module may be placed in any available slot in the system. To install the module, remove the baseboard cover and install it with the component side facing the power supply.

CAUTION: Always turn off the system power before installing or removing modules. To avoid possible EMI radiation, never operate the system with the top cover removed.

User-Configured Components

Switches S101-S107 independently select isolated or non-isolated inputs for channels 1 through 7 respectively.

All input connections are made to screw terminals on P172. Two terminals are provided for each channel (+ and −). All terminals accept 16-24 gage wire stripped to 3/16 of an inch. See Table 1 and Figure 1 for a list of user-configured components and their locations on the PCM1 board.

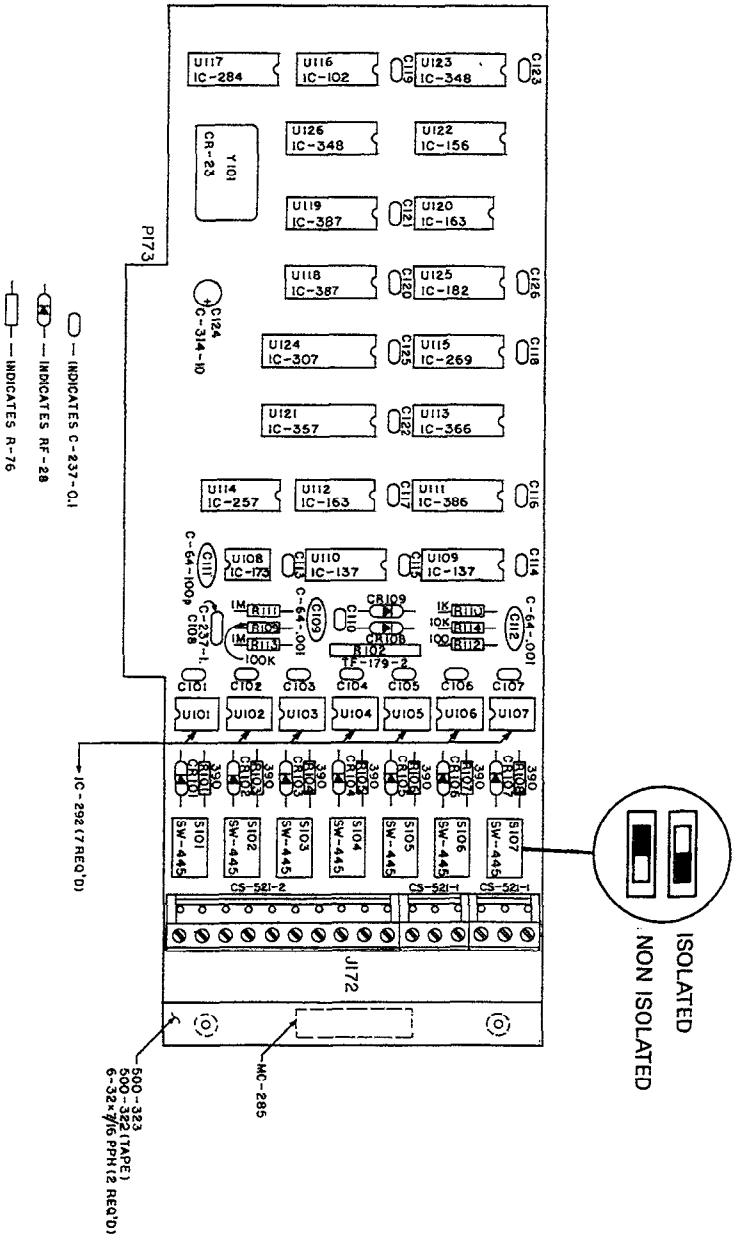


Figure 1. PIM1 Module

Table 1. User-Configured Components on the PIM1

Name	Designation	Function
Switch 101	S101	Chan 1 Isolated/Non-isolated Selection
Switch 102	S102	Chan 2 Isolated/Non-isolated Selection
Switch 103	S103	Chan 3 Isolated/Non-isolated Selection
Switch 104	S104	Chan 4 Isolated/Non-isolated Selection
Switch 105	S105	Chan 5 Isolated/Non-isolated Selection
Switch 106	S106	Chan 6 Isolated/Non-isolated Selection
Switch 107	S107	Chan 7 Isolated/Non-isolated Selection
Screw Terminals	P172	Input connections, Channels 0-7

Connections

Connecting terminals for the PIM1 module are shown in Figure 2 which illustrates a typical connecting scheme. Note that connections will be the same whether an isolated or non-isolated configuration is used. See below for more information on the isolated and nonisolated modes.

Figure 3 shows a possible connecting scheme for cases in which PIM1 module is software configured to accept gated inputs. For more information on gated inputs see the discussion of the CONTROL REGISTER command below.

When making any connection to the PIM1, keep in mind that channels 1-7 are designed for TTL compatible inputs, while channel 0 has 200mV sensitivity. Also, the use of shielded cable is recommended to minimize the possibility of EMI radiation. Connect one end of the shield to a rear chassis ground post and leave the other end disconnected. Do not use the shield as a signal-carrying lead.

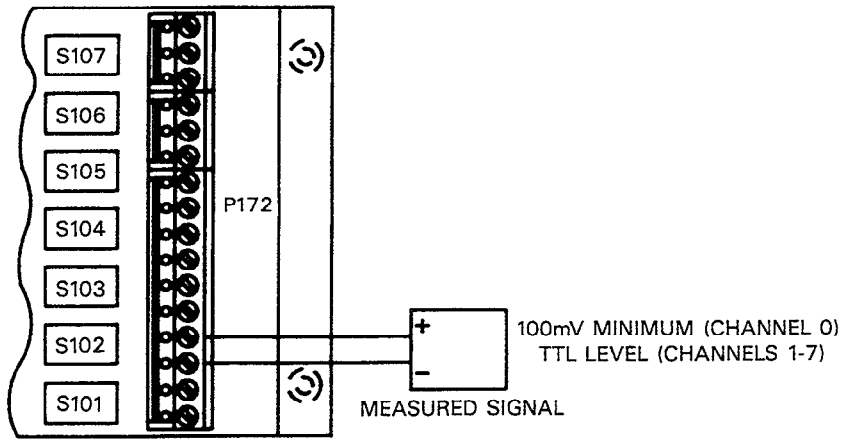


Figure 2. Typical PIM1 Connections

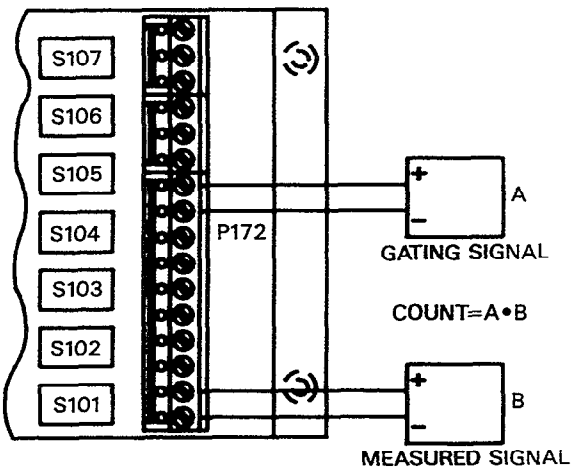


Figure 3. Typical Connections for Gated Mode

Isolated/Non-isolated Input Mode Selection

Channels 1 through 7 of the PIM1 module may be operated in either isolated or non-isolated TTL-compatible modes. Switches S101-S107 select the input mode for channels 1 through 7 respectively (see Figure 1). When in the isolated mode, the input signals may be floated up to 400V above chassis ground. Note that the maximum frequency that can be measured is reduced to 2MHz when an input channel is used in the isolated mode, regardless of the selected frequency range.

When an input channel is configured as an isolated input, the minimum input current for rated frequency is 6.5mA, and the maximum input current is 15mA. The driving device can be configured to either source or sink the input current. Typically, the device sinks current, as shown in Figure 4. With this configuration, the maximum value of V is 8.7V. For higher voltages, a resistor can be inserted in series between the supply voltage and the + terminal. Compute the value of this resistor with the following formula:

$$R = \frac{V-1.7}{0.01} - 330$$

Note that this value will result in a nominal current of about 10mA.

For example, assume that a supply of 24V is used for V+. The resistor value is then computed as follows:

$$R = \frac{24\text{-}1.7}{0.01} - 330$$

$$R = 1900$$

CAUTION: Do not exceed the isolation voltage value as stated in the PIM1 specifications.

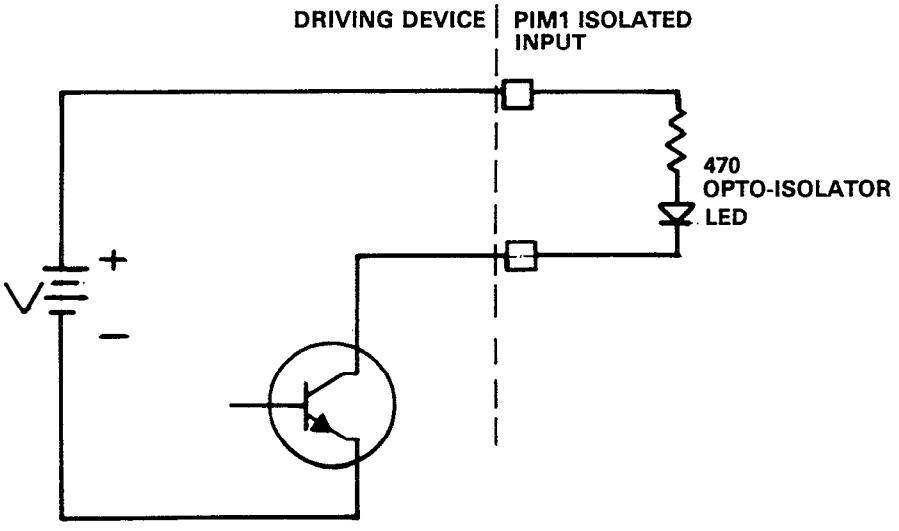


Figure 4. Typical Sinking PIM1 Isolated Connections

Commands

PIM1 Commands provide software control of selected input channel and input gating, frequency range, frequency/event mode, and triggering and reset functions. Commands are also used to read low and high bytes of frequency or event data. PIM1 commands are summarized in Table 2. Table 3 lists the location for the slot-dependent commands.

Table 2. Commands used with the PIM1 Module

Command	Location
CONTROL REGISTER	Slot-dependent CMDA (write)
TRIGGER/RESET	Slot-dependent CMDB (write)
LOW DATA	Slot-dependent CMDA (read)
HIGH DATA	Slot-dependent CMDB (read)

Table 3. Locations for Slot-Dependent Commands

Slot	CMDA*	CMDB**
Slot 1	CFF80	CFF81
Slot 2	CFF82	CFF83
Slot 3	CFF84	CFF85
Slot 4	CFF86	CFF87
Slot 5	CFF88	CFF89
Slot 6	CFF8A	CFF8B
Slot 7	CFF8C	CFF8D
Slot 8	CFF8E	CFF8F
Slot 9	CFF90	CFF91
Slot 10	CFF92	CFF93

* CONTROL REGISTER (write) or LOW DATA (read)
**TRIGGER/RESET (write) or HIGH DATA (read)

CONTROL REGISTER

Location: Slot-dependent CMDA

Values written to the CONTROL REGISTER location are constituted by eight bits of information that specify the desired input channel (or pair of channels for input gating), gate time (and thus frequency range), and whether the module will be monitoring frequencies or counting events (see Figure 5). CONTROL REGISTER is a write-only location that depends on the slot in which the PIM1 board is placed, as summarized in Table 3.

The lowest four bits (D0-D3) of the value written to CONTROL REGISTER select which of the eight input channels (0-7) on the PIM1 are to be read, It is also possible to select a pair of input channels (channel n and channel n + 4) in instances where input gating is desired (used only when the module is configured as an event counter). If this mode is selected, channel n + 4 will act as a gate for channel n, allowing that channel to be read only when channel n + 4 is high (on). In other words, the paired inputs perform the logical AND function. A complete list of values assigned to bits D0-D3 is given in Table 4.

Bits D4-D6 of the value written to the CONTROL REGISTER location are used to select a gate time, when the PIM1 module is configured to measure frequencies. When the module is configured to count events (pulses), the values assigned to these bits are unimportant, Table 5 lists the available times and the maximum frequencies which can be measured. Note that the frequencies given assume the channels are being operated in the non-isolated mode; maximum input frequency in the isolated mode for channels

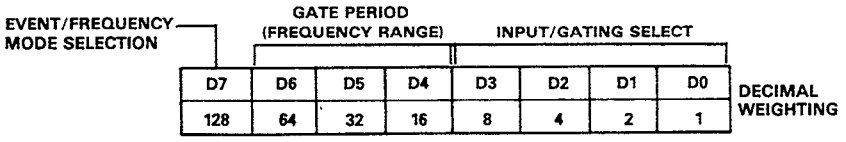


Figure 5. CONTROL REGISTER Bit Configuration

1 through 7 is limited to 2MHz. Also, channel 0 is limited to 1MHz because of input signal conditioning.

Bit D7 selects the mode of the PIM1, configuring that module to either count events or measure frequency, When D7 is set to logical, the event mode is selected; the frequency mode is selected when D7 is set to logic 0 (see Table 6).

Table 4. Input Channel Selection (Bits D0-D3)

D3	D2	D1	D0	Input Description
0	0	0	0	CH #0 gated with CH #4
0	0	0	1	CH #1 gated with CH #5
0	0	1	0	CH #2 gated with CH #6
0	0	1	1	CH #3 gated with CH #7
0	1	0	0	CH #0
0	1	0	1	CH #1
0	1	1	0	CH #2
0	1	1	1	CH #3
1	0	0	0	CH #4
1	0	0	1	CH #5
1	0	1	0	CH #6
1	0	1	1	CH #7

Table 5. Frequency Counter Software Selectable Gate Times (Bits D4-D6)

D6	D5	D4	Gate Time	Frequency	Resolution
0	0	0	8.192msec	8MHz	122.0Hz
0	0	1	16.384msec	4MHz	61.0Hz
0	1	0	32.768msec	2MHz	30.0Hz
0	1	1	65.536msec	1MHz	15.0Hz
1	0	0	131.072msec	500kHz	7.5Hz
1	0	1	262.144msec	250kHz	3.7Hz
1	1	0	524.288msec	125kHz	1.9Hz
1	1	1	1048.576msec	62.5kHz	1.0Hz

Table 6. Frequency/Event Mode Selection (Bit D7)

D7 Value	Mode
0	Frequency
1	Event

TRIGGER/RESET

Location: Slot-dependent CMDB

TRIGGER/RESET is a write-only location whose function varies slightly, depending on whether the module is configured to count events or measure frequencies. In the event mode, writing any value to the TRIGGER/RESET location resets the PIM1 hardware counter to zero, preparing the counter for a new set of pulse inputs. In the frequency mode, writing to this location triggers a measurement. Any value written to the TRIGGER/RESET location will effect the indicated functions. It is the act of writing, rather than the value itself, that triggers or resets the counter.

Note that powering-on will not automatically reset the PIM1 hardware counter to zero. The TRIGGER/RESET command must be issued to ensure that the counter is properly reset.

When operating in the frequency mode, the TRIGGER/RESET command should be followed by a software delay to ensure that sufficient time has elapsed from the time the counter is triggered until the data is read. This delay period must be longer than the selected gate time.

LOW DATA

Location: Slot-dependent CMDA

Because the PIM1 counter is 16 bits wide, the count it contains will be 16 bits long. The memory locations of the computer, however, can hold only 8 bits. For this reason, the count is broken up into two bytes - high byte and low byte - and stored in two different memory locations. Reading the LOW DATA location provides the low byte of the current count, To obtain the complete count, the HIGH DATA location should be read immediately after reading LOW DATA, and the two bytes combined as described below.

In the event mode, the count is latched at the time that LOW DATA is read, This ensures that the low byte does not overflow before the high byte is accessed with the HIGH DATA command. Note that reading the count does not interrupt the counter, which continues until reset by the TRIGGER/RESET command.

In the frequency mode, the count is latched automatically at the conclusion of the specified gate time.

HIGH DATA

Location: Slot-dependent CMDB

Reading the HIGH DATA location provides the high byte of the current count. The LOW DATA location should always be read before reading HIGH DATA. This ensures that the count is latched, preventing the low byte from overflowing before the high byte is read.

Once both the low byte and high byte of the count have been obtained, the total count can be calculated as follows:

CO=LB+256*HB

Where CO is the number of counts, and LB and HB are low and high bytes respectively. Since the PIM1 uses a 16-bit counter, the total possible counts is 65,536 - with a range of 0-65,535 counts.

In the pulse mode, the counter will overflow (return to zero and begin counting again) if the count exceeds 65,535. A software overflow counter can be employed to increase the maximum event count.

In frequency mode, the counter will simply stop counting at 65,535. Therefore, a reading of 65,535 should be taken as an indication that the counter has overflowed. To convert counts to frequency, use the formula:

F=CO/P

Where F is the frequency in Hz, CO the number of counts, and P is the gate period in seconds. Note that the gate times listed in Table 5 are given in milliseconds.

Theory of Operation

Circuitry on the PIM1 module, which is shown on schematic drawing number 500-296, may be divided into five groups: input circuitry, command-development circuitry, control circuitry, counter circuitry, and data buffering circuitry.

The counter itself is made up of U118 and U119, which are 8 bit binary counters (74LS590), U118 counts the lower eight bits, while U119 contains the count of the upper eight bits. The input signal is applied to the CCK terminals of both counters through U113, a transparent data latch (74LS75). U113 is controlled by the gate period control circuitry. Output gating of the counter ICs is controlled by CMDAR and CMDBA for U118 and U119 respectively.

The two counter outputs as well as the control register inputs are all connected to a common data bus. Buffering between the internal PIM1 data bus and the baseboard data bus is provided by U133 (74LS245), an octal bus transceiver. Baseboard R/W, CMDA and CMDB lines control data transmission through this IC. When both R/W and CMDA are low, data is fed through U133 from the baseboard data bus and latched

in the control register. If R/W is high, U133 is configured to feed data out over the baseboard bus from either U118 or U119 depending on the status of CMDA and CMDB.

PIM1 Specifications

As a frequency counter:

Eight multiplexed software-selectable inputs are provided. Channels 1-7 are TTL compatible and channel 0 is AC coupled with a 200mV peak sensitivity. Eight different software-programmable gate times are available which provide resolution from 1Hz per bit to a full scale of 8MHz. Counter resolution is 1 part in 65536 (0.0015%. Overrange is detected by a maximum count of 65535.

Inputs:

Ch1 to Ch7 are TTL compatible to 8MHz (non-isolated) or 2MHz (isolated). CH0 is nonisolated and AC coupled for 200mV peak sensitivity to 1MHz.

Maximum Input Frequency:
  2MHz (Isolated)
  8MHz (TTL Non-isolated)
  1MHz (200mV Non-isolated)
Absolute Maximum Inputs:
  Ch1 thru Ch7
    Non-isolated TTL: +5,5V/−0.3V
    Common Mode Isolation:
      400V (DC to 60Hz)
      10^7 V*Hz Max
    Isolation Input: <20mA Max
  Ch0
    Non-isolated LO Level; 50V DC and/or peak AC

Range	Gate Time	Reading	Resolution	Accuracy
8MHz	8192ms	8MHz	122.0Hz	±(0.4% + 122.0Hz)
4MHz	16.384ms	4MHz	61.0Hz	±004% + 61.0Hz)
2MHz	32.768ms	2MHz	30.0Hz	±(0.03% + 30.0Hz)
1MHz	65.536ms	1MHz	15.0Hz	±(0.03% + 15.0Hz)
500kHz	131.072ms	500kHz	7.5Hz	±(0.03% + 7.5Hz)
250kHz	262.144ms	250kHz	3.7Hz	±(0.03% + 3.7Hz)
125kHz	524.288ms	125kHz	1.9Hz	±(0.03% + 1.9Hz)
62.5kHz	1048.576ms	62.5kHz	1.0Hz	±(0.03% + 1.0Hz)

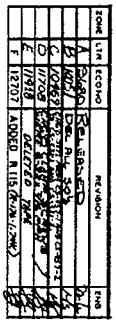
As An Event Counter:

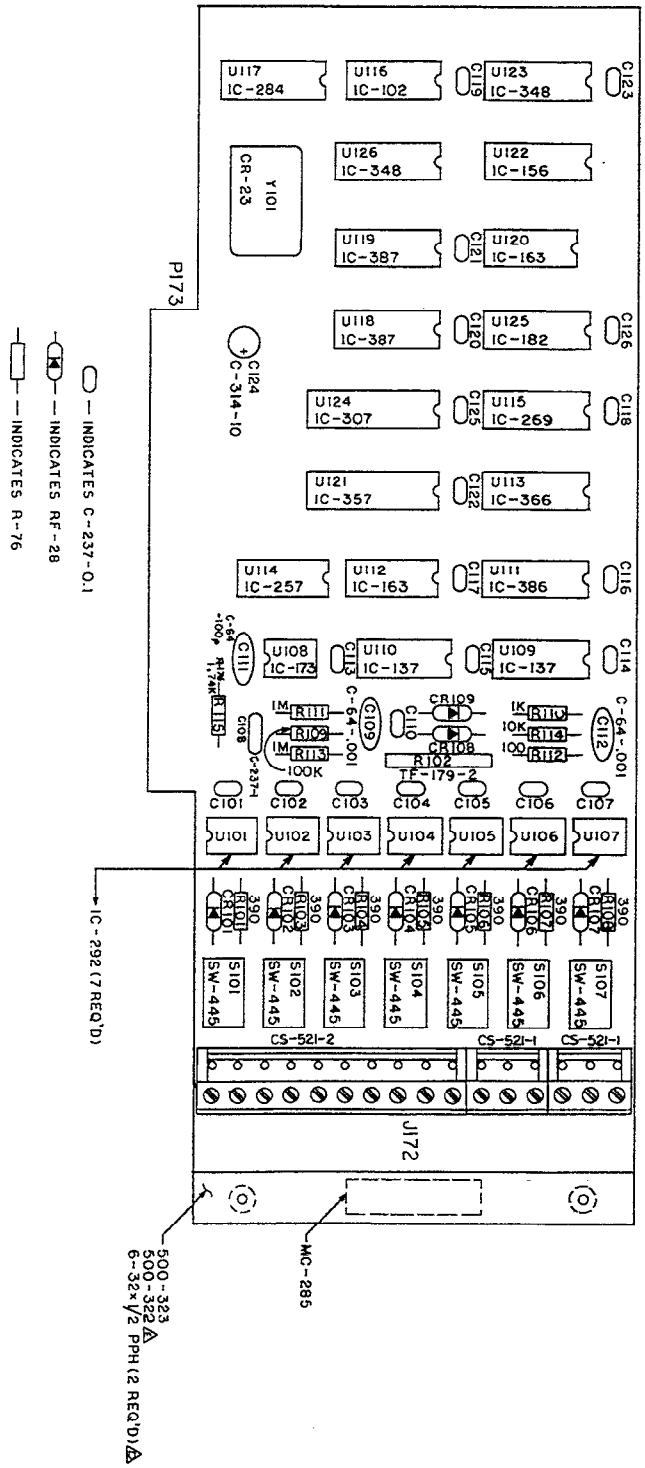
The PIM1 can be configured under software control to count events (pulses). The hardware counter is 16 bits wide with an additional 16- bit over-flow counter in software. This provides a maximum event count of greater than 4 billion. The PIM1 can be software-selected to count events on one of eight inputs. The counter can be read without effecting the counter contents and reset under software control. Due to the

anti-coincidence circuitry, reading the counter contents will not occur in an undefined state. In addition, no pulses will be missed if the maximum event frequency is less than 250kHz.

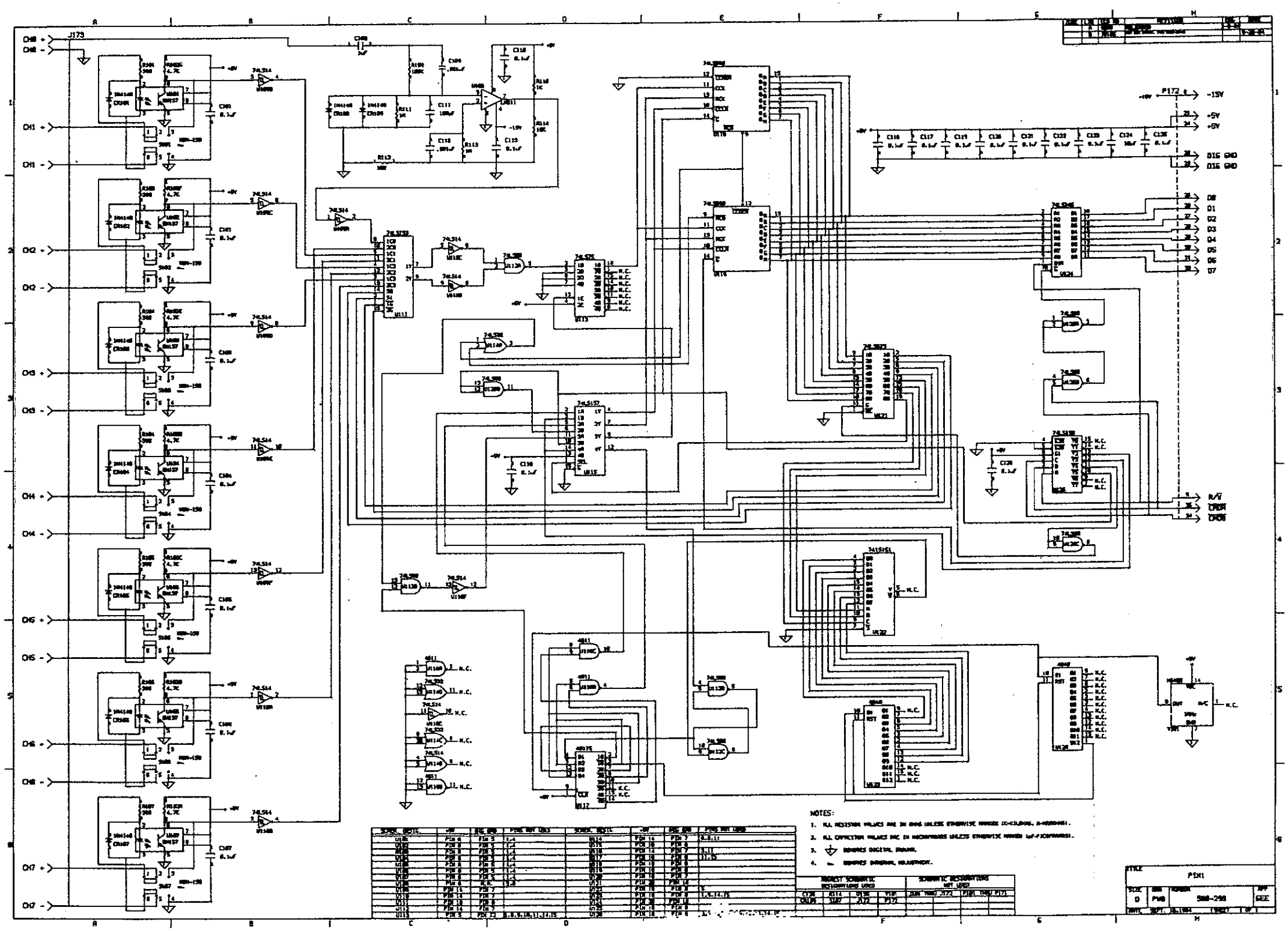
The inputs may also be configured as four dual input channels. This allows events to be gated by external sources.

Maximum Input Frequency: 250kHz (anti-coincidence non-isolated or isolated)





PIM1 COMPONENT LAYOUT



PIM1 SCHEMATIC DIAGRAM