KEITHLEY

KPCMCIA-12AI/16AI PCMCIA

Data Acquisition System

User's Manual

A GREATER MEASURE OF CONFIDENCE

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Keithley Instruments, Inc. warrants that, for a period of one (1) year from the date of shipment (3 years for Models 2000, 2001, 2002, 2010 and 2700), the Keithley Hardware product will be free from defects in materials or workmanship. This warranty will be honored provided the defect has not been caused by use of the Keithley Hardware not in accordance with the instructions for the product. This warranty shall be null and void upon: (1) any modification of Keithley Hardware that is made by other than Keithley and not approved in writing by Keithley or (2) operation of the Keithley Hardware outside of the environmental specifications therefore.

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User's Manual

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Safety Precautions

The following safety precautions should be observed before using this product and any associated instrumentation. Although some instruments and accessories would normally be used with non-hazardous voltages, there are situations where hazardous conditions may be present.

This product is intended for use by qualified personnel who recognize shock hazards and are familiar with the safety precautions required to avoid possible injury. Read and follow all installation, operation, and maintenance information carefully before using the product. Refer to the manual for complete product specifications.

If the product is used in a manner not specified, the protection provided by the product may be impaired.

The types of product users are:

Responsible body is the individual or group responsible for the use and maintenance of equipment, for ensuring that the equipment is operated within its specifications and operating limits, and for ensuring that operators are adequately trained.

Operators use the product for its intended function. They must be trained in electrical safety procedures and proper use of the instrument. They must be protected from electric shock and contact with hazardous live circuits.

Maintenance personnel perform routine procedures on the product to keep it operating properly, for example, setting the line voltage or replacing consumable materials. Maintenance procedures are described in the manual. The procedures explicitly state if the operator may perform them. Otherwise, they should be performed only by service personnel.

Service personnel are trained to work on live circuits, and perform safe installations and repairs of products. Only properly trained service personnel may perform installation and service procedures.

Keithley products are designed for use with electrical signals that are rated Installation Category I and Installation Category II, as described in the International Electrotechnical Commission (IEC) Standard IEC 60664. Most measurement, control, and data I/O signals are Installation Category I and must not be directly connected to mains voltage or to voltage sources with high transient over-voltages. Installation Category II connections require protection for high transient over-voltages often associated with local AC mains connections. Assume all measurement, control, and data I/O connections are for connection to Category I sources unless otherwise marked or described in the Manual.

Exercise extreme caution when a shock hazard is present. Lethal voltage may be present on cable connector jacks or test fixtures. The American National Standards Institute (ANSI) states that a shock hazard exists when voltage levels greater than 30V RMS, 42.4V peak, or 60VDC are present. **A good safety practice is to expect that hazardous voltage is present in any unknown circuit before measuring.**

Operators of this product must be protected from electric shock at all times. The responsible body must ensure that operators are prevented access and/or insulated from every connection point. In some cases, connections must be exposed to potential human contact. Product operators in these circumstances must be trained to protect themselves from the risk of electric shock. If the circuit is capable of operating at or above 1000 volts, **no conductive part of the circuit may be exposed.**

Do not connect switching cards directly to unlimited power circuits. They are intended to be used with impedance limited sources. NEVER connect switching cards directly to AC mains. When connecting sources to switching cards, install protective devices to limit fault current and voltage to the card.

Before operating an instrument, make sure the line cord is connected to a properly grounded power receptacle. Inspect the connecting cables, test leads, and jumpers for possible wear, cracks, or breaks before each use.

When installing equipment where access to the main power cord is restricted, such as rack mounting, a separate main input power disconnect device must be provided, in close proximity to the equipment and within easy reach of the operator.

For maximum safety, do not touch the product, test cables, or any other instruments while power is applied to the circuit under test. ALWAYS remove power from the entire test system and discharge any capacitors before: connecting or disconnecting cables or jumpers, installing or removing switching cards, or making internal changes, such as installing or removing jumpers.

Do not touch any object that could provide a current path to the common side of the circuit under test or power line (earth) ground. Always make measurements with dry hands while standing on a dry, insulated surface capable of withstanding the voltage being measured.

The instrument and accessories must be used in accordance with its specifications and operating instructions or the safety of the equipment may be impaired.

Do not exceed the maximum signal levels of the instruments and accessories, as defined in the specifications and operating information, and as shown on the instrument or test fixture panels, or switching card.

When fuses are used in a product, replace with same type and rating for continued protection against fire hazard.

Chassis connections must only be used as shield connections for measuring circuits, NOT as safety earth ground connections.

If you are using a test fixture, keep the lid closed while power is applied to the device under test. Safe operation requires the use of a lid interlock.

If  or  is present, connect it to safety earth ground using the wire recommended in the user documentation.

The  symbol on an instrument indicates that the user should refer to the operating instructions located in the manual.

The  symbol on an instrument shows that it can source or measure 1000 volts or more, including the combined effect of normal and common mode voltages. Use standard safety precautions to avoid personal contact with these voltages.

The **WARNING** heading in a manual explains dangers that might result in personal injury or death. Always read the associated information very carefully before performing the indicated procedure.

The **CAUTION** heading in a manual explains hazards that could damage the instrument. Such damage may invalidate the warranty.

Instrumentation and accessories shall not be connected to humans.

Before performing any maintenance, disconnect the line cord and all test cables.

To maintain protection from electric shock and fire, replacement components in mains circuits, including the power transformer, test leads, and input jacks, must be purchased from Keithley Instruments. Standard fuses, with applicable national safety approvals, may be used if the rating and type are the same. Other components that are not safety related may be purchased from other suppliers as long as they are equivalent to the original component. (Note that selected parts should be purchased only through Keithley Instruments to maintain accuracy and functionality of the product.) If you are unsure about the applicability of a replacement component, call a Keithley Instruments office for information.

To clean an instrument, use a damp cloth or mild, water based cleaner. Clean the exterior of the instrument only. Do not apply cleaner directly to the instrument or allow liquids to enter or spill on the instrument. Products that consist of a circuit board with no case or chassis (e.g., data acquisition board for installation into a computer) should never require cleaning if handled according to instructions. If the board becomes contaminated and operation is affected, the board should be returned to the factory for proper cleaning/servicing.

Table of Contents

5 Optional Accessories

A Specifications

B PCMCIA Interface

C I/O Registers

List of Illustrations

3 Theory of Operation

4 I/O Connections

5 Optional Accessories

C I/O Registers

List of Tables

4 I/O Connections

B PCMCIA Interface

C I/O Registers

1
Introduction

Getting started

The KPCMCIA-12AI/16AI PC cards are PCMCIA type II data acquisition systems with eight differential or 16 single-ended analog input channels. The number of input channels can be expanded to 256 with input expansion cards. Each channel has a bipolar input range of ±10V, ±5V, ±2.5V, or ±1.25V (programmable gains of 1, 2, 4, or 8). These PC cards support sampling rates up to 100kHz at either 12-bit or 16-bit resolution.

Equipped with a data FIFO (first in first out) of 2048 samples, the KPCMCIA-12AI/16AI PC cards can achieve full-speed data acquisition under Windows 95/98 and Windows NT. The cards have a scan FIFO of the same size that supports full-speed, random-order channel scanning and gain selection for all the input channels (up to 256 channels when using the input expansion cards).

These PC cards also include a 24-bit pacer clock and a programmable divided-by-2, by-10, or by -100 pre-scaler. The pacer clock can also be used with an external clock source. With the 10MHz internal clock source, the pacer clock can generate accurate sampling rate from 0.006Hz to 100kHz.

Both cards have four digital inputs and four digital output channels, which are all TTL compatible and may be used for control or monitoring in addition to analog data acquisition.

The DriverLINX software drivers provided support various programming languages including Visual C/C++, Visual Basic and Delphi. A Dynamic Link Library (DLL) is provided for all programming languages under Microsoft Windows, as well as the Visual Basic Controls (VBX). The KPCMCIA-12AI/16AI PC card also has turn-key software supports for TestPoint and LabView.

The KPCMCIA-12AI/16AI is provided with a KCAB-AI cable with an industry standard D-37 female connector for interfacing to optional terminal blocks and expansion boards. These optional accessories are described in Section 5.

Features

The KPCMCIA-12AI/16AI PC card offers the following features:

- 12- or 16-bit resolution
- Eight differential or 16 single-ended analog input channels, expandable to 256 channels
- Bipolar input range up to ±10V
- Truly programmable gains of 1, 2, 4, or 8
- Full-speed channel scanning and gain selection for all analog input channels
- Data FIFO of 2048 samples
- Sampling rate up to 100kHz
- 24-bit pacer clock with variable pre-scalers and external clock source*
- Digital input/output channels
- Flexible trigger mode (internal/external*, one-shot/continuous, rising/falling edge)
- Software drivers for Windows 95/98 and Windows NT as well as canned software packages for TestPoint. An optional LabView driver is available.

**NOTE In "Paced" mode, the same input pin is shared between external clock and external trigger, therefore only one function can be used (not both simultaneously).*

Technical support

Before returning any equipment for repair, call Keithley Instruments, Inc., for technical support at:

1-888-KEITHLEY
Monday - Friday, 8:00 a.m. - 5:00 p.m., Eastern Time

An applications engineer will help you diagnose and resolve your problem over the telephone.

If a telephone resolution is not possible, the applications engineer will issue you a Return Material Authorization (RMA) number and ask you to return the equipment. Include the RMA number with any documentation regarding the equipment.

When returning equipment for repair, include the following information:

- Your name, address, and telephone number.
- The invoice or order number and date of equipment purchase.
- A description of the problem or its symptoms.
- The RMA number on the outside of the package.

Repackage the equipment using the original anti-static wrapping, if possible, and handle it with ground protection. Ship the equipment to:

ATTN: RMA # _____
Repair Department
Keithley Instruments, Inc.
28775 Aurora Road
Cleveland, OH 44139

Telephone 1-888-KEITHLEY
FAX (440) 248-6168

NOTES *If you are submitting your equipment for repair under warranty, you must include the invoice number and date of purchase.*

To enable Keithley Instruments, Inc., to respond as quickly as possible, you must include the RMA number on the outside of the package.

2
Installation

Hardware setup

To install the KPCMCIA-12AI/16AI PC card, insert the adapter into any type II PCMCIA socket. All other configuration options are determined by the DriverLINX Software operating system as discussed in your DriverLINX manuals.

Software setup

Refer to your DriverLINX documentation for a detailed description of the software installation procedure.

3
Theory of Operation

Introduction

The KPCMCIA-12AI/16AI PC card consists of eight differential or 16 single-ended analog input channels. Each channel has a bipolar input range from –0.01V (gain = 1000), –0.1V (gain = 100), –1V (gain = 10), and –10V (gain = 1) with programmable gains of 1, 10, 100, and 1000. The A/D converter, either 12-bit or 16-bit, can be operated at its top speed of 100,000 samples per second (10µs per sample).

The A/D converter uses left-justified 2 s complement coding. For the 16-bit version, its output ranges from -32768 to 32767. However, the 12-bit version will have its 12-bit result occupying the most significant 12 bits and will pad its least significant four bits with all zeroes to make a 16-bit output word for each converted input sample.

The KPCMCIA-12AI/16AI PC card can be operated as an I/O device, occupying eight consecutive bytes in the I/O address space. It can also be configured to operate via a memory mapped I/O. It fully complies with the PCMCIA standard 2.10 as a type II card. The card does not have any jumpers or DIP switches; all of its configurable features are programmable.

Functionally, the KPCMCIA-12AI/16AI PC card consists of the following components: the DC/DC power supply, analog input multiplexer, programmable gain control, A/D converter, data FIFO, scan list, trigger control, pacer clock, interrupt and status, digital I/O, as well as the associated control circuits.

DC/DC power supply

The KPCMCIA-12AI/16AI PC card uses a standard 5V power supply for its digital circuit. The –15V power supplies are used for the analog front end, and the analog +5V power supply is used for the A/D converter. All are generated by a DC/DC converter off the +5 digital input power supply from the PCMCIA connector. The DC/DC converter takes 140mA, 78% of the 180mA total load current, from the input power supply.

According to the new PCMCIA specification, any card that takes more than 100mA cannot be turned on when the card is inserted until it is intentionally accessed. The KPCMCIA-12AI/16AI PC card will support the new specification by providing a unique power-down mode control. When the card is first plugged in, powered up, or reset, the DC/DC converter shuts off. Only the digital portion is up and running, taking only 40mA from the input +5V power supply. Full-powered mode can then be activated by software.

Analog input multiplexer

The differential or single-ended configuration is selected by software. The expansion cards can only be used on single-ended channels. The single-ended/differential selection should be the same for all the internal channels (e.g., all eight channels as differential or all 16 channels as single-ended). Having some channels configured as single-ended and others as differential could cause confusion and unexpected signal errors.

In a differential configuration, there are at most eight channels. However, if you specify channel 8 to 15 in the differential configuration, the inputs will be shorted to ground for the system offset measurement. The readings taken under these circumstances can be used for offset correction.

The input multiplexers have built-in protection against overvoltage when the board is powered on and off. The protection mechanism will isolate the input from the rest of the board as long as the input voltage is within the protection range of –30V.

Programmable gain control

The KPCMCIA-12AI/16AI PC card has an internal gain of 1, 10, 100, and 1000. The gain can be changed from channel to channel when scanning through the channels. There is a programmable gain instrumentation amplifier with gains of 1, 10, 100, and 1000. The internal gain selection is specified in the scan list entry by software. The internal gain selection determines the gain of the analog front end.

The settling time of the analog front end meets the speed requirement. However, if the amplifier is saturated, it may need a longer amount of time to recover, which may cause distortion in the input signal to the A/D converter. Amplifier saturation should be avoided (use low gains or attenuate the input signal).

Scan list

One entry to the scan list contains a 16-bit word or two eight-bit bytes. It specifies the internal channel selection and gain selection (in the high byte or MSB), the external channel and gain selection (in the low byte or LSB), as well as other control and configuration settings.

The external selections are used for channels on the expansion cards, while internal ones are used for channels on the KPCMCIA-12AI/16AI PC card.

The expansion cards are not included as part of the KPCMCIA-12AI/16AI data acquisition system. However, they can be purchased separately from Keithley.

The number of entries in the scan list ranges from 1 to 2048. There are no dependencies implied among the entries of the scan list. You may choose any valid gain combination for any channel, internal or external. The channels can be scanned in any order as required, repeated or not, with the same or different gain for each entry.

The differential/single-ended selection should be the same for all the entries in the scan list. The single-ended configuration should be selected if one or more expansion cards are connected to the KPCMCIA-12AI/16AI PC card.

The synchronous sample and hold selection is reserved for the expansion cards.

Trigger circuit

The KPCMCIA-12AI/16AI PC card can be triggered by the software (or an internal trigger as compared to that coming from an external TTL signal), the external TTL signal*, or the pacer clock. For the external TTL trigger, an active trigger edge can be selected for either the low-to-high transition or the high-to-low transition.

In one-shot trigger mode, one trigger, either internal or external, starts one scan of all the channels specified in the scan list. The pacer clock does not have any effect in this mode. Multiple scans can be realized by issuing (or receiving) multiple triggers.

In continuous trigger mode, the software or TTL trigger starts a series of scans in which the first is initiated immediately upon receiving the trigger, while the rest are carried out each time the pacer clock fires. The process continues until software issues an A/D stop command.

If the internal trigger (or the software trigger) is selected, a trig/arm command from software serves as a trigger as soon as it is received by the PC card. For the external trigger source, the same command is taken as an arm command, which arms the PC card so the first proper trigger edge since receiving the arm command serves as the trigger. Any trigger edges before the first one are ignored. Unexpected edge transitions during the configuration of the trigger source and edge will not be taken as triggers as long as the PC card is not armed.

**NOTE In "Paced" mode, the same input pin is shared between external clock and external trigger, therefore only one function can be used (not both simultaneously).*

A/D converter and data FIFO

The KPCMCIA-12AI/16AI PC card always assumes a bipolar input range of –10V if the gain is one. The output data format will always be in 2 s complement (and left justified for 12-bit versions). The data acquisition time of the A/D converter is 2µs, and its conversion time is no more than 8µs. The output of the A/D converter is fed into the data FIFO, providing 2048 samples for data buffering.

The hardware design guarantees that the A/D converter, once triggered, will do a conversion for every analog input channel specified in the scan list at the specified scan speed and feed the results into the data FIFO. In between scans, the PC card waits until another trigger occurs (one-shot mode) or the pacer clock fires (continuous mode).

The data FIFO has two programmable thresholds, one for almost full and the other for almost empty. The KPCMCIA-12AI/16AI PC card only uses the almost-full threshold and ignores the almost-empty one. Upon power-up or reset, the almost-full threshold defaults to 7 bytes to full (3.5 samples).

When the FIFO is full, no more samples can be written into the FIFO. At the end of each scan, the KPCMCIA-12AI/16AI PC card sets a data-lost flag if the data FIFO is already full.

Interrupt and status

The KPCMCIA-12AI/16AI PC card has two interrupt sources: the end-of-scan (EOS) interrupt and the FIFO threshold interrupt. These interrupts are used as follows:

- When the EOS interrupt is enabled, an interrupt is sent to the host at the end of each scan of the channel list. If there is only one channel in the scan list, the EOS interrupt is reduced to an EOC (end-of-conversion) interrupt.
- The FIFO threshold interrupt, when enabled, is sent to the host when the almost-full flag is set. The host can then move a block of samples from the FIFO.

Digital I/O

The KPCMCIA-12AI/16AI PC card has one digital input port (base + 3, read only) of four bits (bits 0 through 3) and one digital output port (base + 3, write only) of four output bits (bits 0 through 3). The output port is latched, but the input port is not.

Four input lines are connected to the digital input port; each represents one bit in the port. When reading the digital input port, the CURRENT status of the digital input lines are returned to the host.

All of the four input lines are shared with other functions. Bit 0 will be shared as the external trigger and external paced clock input, while bit 2 is shared as the external burst clock input. Bits 1 and 3 are taken over as the external gain selection lines if one or more expansion cards are connected and an expansion bit is set by software. Nevertheless, the current status of the digital input lines will always be returned when the host reads the digital input port. It does not matter if the lines are shared or not.

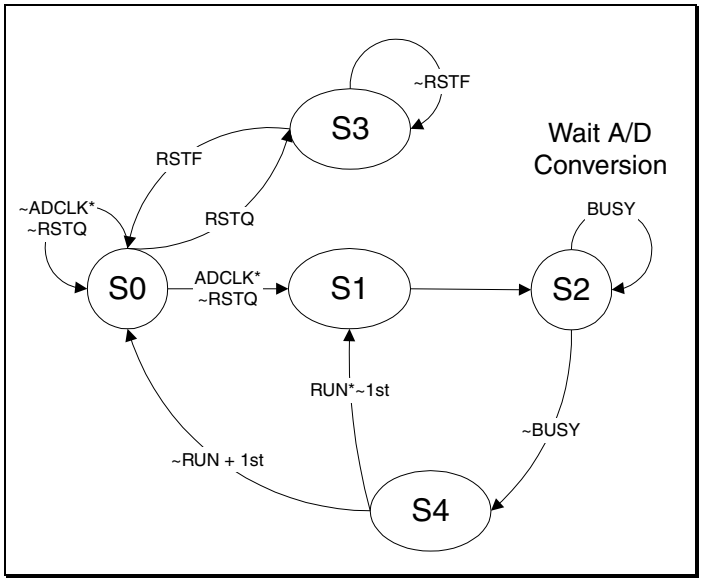
The four digital output lines will be taken over as the external channel selection lines if an expansion bit is set by software. In that case, the digital output lines will be driven by the external channel selection bits of the current scan list entry. Otherwise, they will be connected to the latched bits 0 through 3 of the digital output port.

A/D state machine

The KPCMCIA-12AI/16AI PC card has an internal state machine (Figure 3-1) that controls the A/D operation.

The state machine defaults to state S0 after power-up or reset. The normal state of flow is first from S0 to S3, initiated by a scan list (queue) flush command (RSTQ). Then, the queue is programmed. Thereafter, state machine moves from S3 back to S0. The S3-to-S0 step initiated by issuing a flush-data FIFO command (RSTF) which sets up the gain and channel selections for the first channel in the scan list and then waiting for a trigger to start the scan. When the trigger (ADCLK) comes, the state machine moves from S0 to S1, and the A/D conversion starts once it moves to S1. The state machine waits at S2 until the conversion is done. At that time, it moves to S4 where the A/D conversion result is written into the data FIFO. The scan rate is determined by the time the state machine moves from S1 to S4, which can be set to 10, 20, or 40µs. If there are more channels to scan in the list, the state machine goes to S1 for another conversion loop. Otherwise, it returns to S0 and waits for another trigger (or a sampling pulse from the pacer clock if it is in the continuous trigger mode). Any time during data acquisition, an A/D stop command will clear RUN to zero and eventually stop the data acquisition by moving the state machine back to S0.

Figure 3-1
State transition diagram of A/D conversion process



4
I/O Connections

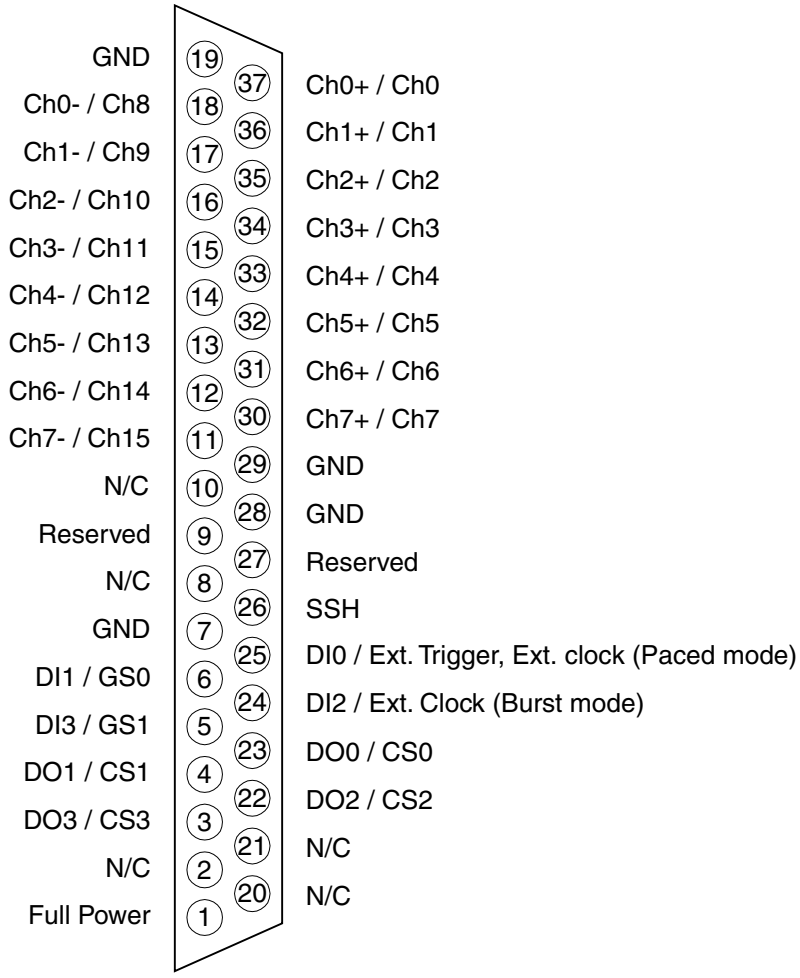
Cable assembly

The KPCMCIA-12AI/16AI is provided with an 18 in. cable terminating in a 37-pin D-type female connector as defined in Table 4-1 and Figure 4-1. Also shown is the corresponding PC card 32-pin connector pinout.

Table 4-1
KPCMCIA-12AI/16AI PC card cable mapping

PC card 32-pin connector	D-37 pin connector	Name		Description
32	37	Channel 0 (+)	Channel 0	A/D input, differential/single-ended
31	18	Channel 0 (-)	Channel 8	A/D input, differential/single-ended
30	36	Channel 1 (+)	Channel 1	A/D input, differential/single-ended
29	17	Channel 1 (-)	Channel 9	A/D input, differential/single-ended
28	35	Channel 2 (+)	Channel 2	A/D input, differential/single-ended
27	16	Channel 2 (-)	Channel 10	A/D input, differential/single-ended
26	34	Channel 3 (+)	Channel 3	A/D input, differential/single-ended
25	15	Channel 3 (-)	Channel 11	A/D input, differential/single-ended
24	33	Channel 4 (+)	Channel 4	A/D input, differential/single-ended
23	14	Channel 4 (-)	Channel 12	A/D input, differential/single-ended
22	32	Channel 5 (+)	Channel 5	A/D input, differential/single-ended
21	13	Channel 5 (-)	Channel 13	A/D input, differential/single-ended
20	31	Channel 6 (+)	Channel 6	A/D input, differential/single-ended
19	12	Channel 6 (-)	Channel 14	A/D input, differential/single-ended
18	30	Channel 7 (+)	Channel 7	A/D input, differential/single-ended
17	11	Channel 7 (-)	Channel 15	A/D input, differential/single-ended
16	29	GND		
15	1	Full power (org. D/A 0 ref. in)		1/0 : Full power/Power down
14	26	SSH (org. D/A 1 ref. in)		Synchronous sample hold
13	25	Digital in bit 0 (shared)		External trigger (same as in DAS-16)
12	6	Digital in bit 1 (normal mode)		External gain, LSB (expansion mode)
11	24	Digital in bit 2 (shared)		External clock (org. DAS-16 Ctr 0 Gate)
10	5	Digital in bit 3 (normal mode)		External gain, MSB (expansion mode)
9	23	Digital out bit 0 (normal mode)		External channel bit 0 (expansion mode)
8	4	Digital out bit 1 (normal mode)		External channel bit 1 (expansion mode)
7	22	Digital out bit 2 (normal mode)		External channel bit 2 (expansion mode)
6	3	Digital out bit 3 (normal mode)		External channel bit 3 (expansion mode)
5	7	GND		
4	28	GND		
3	19	GND		
2	19	GND		
1	27	Reserved		D/A output channel 1

Figure 4-1
KPCMCIA-12AI/16AI PC card D-37 output connector, KCAB-AI



5
Optional Accessories

Introduction

This section describes how to attach accessories to the KPCMCIA-12AI/16AI PC card.

Attaching accessories

You can use an STP-37 screw terminal panel or an EXP-1600 expansion accessory with the KPCMCIA-12AI/16AI PC card. The following paragraphs describe how to attach these accessories.

Attaching an STP-37 screw terminal panel

The screw terminals on the STP-37 screw terminal panel let you connect field wiring to a KPCMCIA-12AI/16AI PC card. In addition, the STP-37 contains CJC circuitry for measuring thermocouple input when interfaced to high gain cards and/or expansion boards.

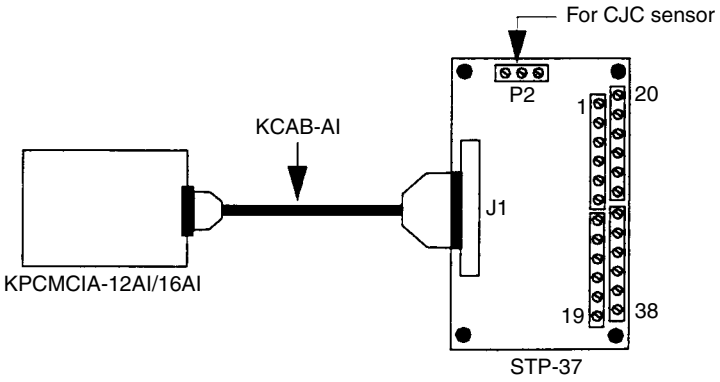
The STP-37 contains 41 screw terminals. Screw terminals 1 to 37 are used to access KPCMCIA-12AI/16AI PC card functions. Note that screw terminal 38 is not used. The three screw terminals in the screw terminal block labeled P2 are used to access the CJC sensor on the panel.

To attach an STP-37 to a KPCMCIA-12AI/16AI PC card, refer to Figure 5-1 and perform the following steps:

1. Attach the 32-pin (smaller) end of the KCAB-AI cable to the 32-pin connector on the KPCMCIA-12AI/16AI PC card.
2. Attach the 37-pin (larger) end of the KCAB-AI cable to the J1 connector on the STP-37.

NOTE *The cables are keyed so you only can connect them one way.*

Figure 5-1
Attaching an STP-37 screw terminal panel



Attaching an EXP-1600 expansion accessory

Each EXP-1600 expansion accessory provides up to 16 different analog input channels (0 to 15). Screw terminals are provided on the following removable field wiring accessories:

- **FWA-EXP** — Attach the FWA-EXP directly to the J1 connector on the EXP-1600; it provides 48 screw terminals, two screw terminals for each channel (CHxx HI and CHxx LO where xx is the number of the analog input channel) and 16 screw terminals for miscellaneous functions. Connect one FWA-EXP to each EXP-1600 you are using.
- **FWA-37U** — Attach the FWA-37U directly to the P4 connector on the EXP-1600; it provides 40 screw terminals that let you access the other functions of the KPCMCIA-12AI/16AI PC card. Connect an FWA-37U to the first EXP-1600 only.

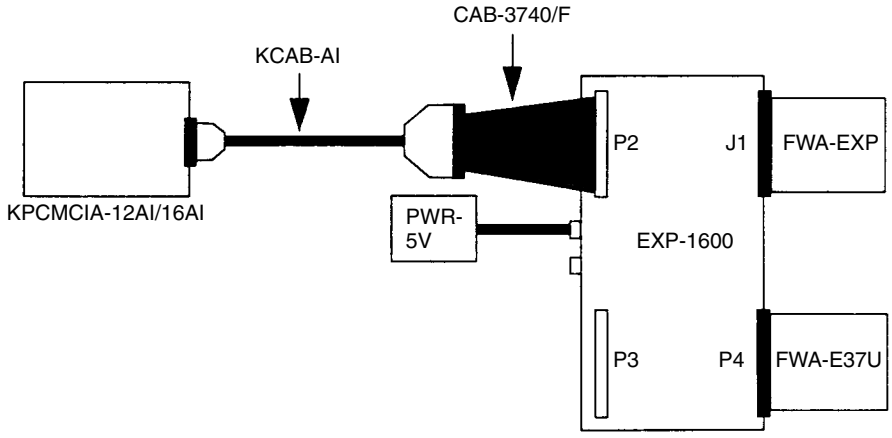
To connect an EXP-1600 to a KPCMCIA-12AI/16AI PC card, refer to Figure 5-2 and perform the following steps:

1. Attach the 32-pin (smaller) end of the KCAB-AI cable to the 32-pin connector on the KPCMCIA-12AI/16AI PC card.
2. Attach the 37-pin (larger) end of the KCAB-AI cable to the 37-pin end of the CAB-3740/F cable.
3. Attach the 40-pin end of the CAB-3740/F cable to the P2 connector on EXP-1600.
4. Attach an external +5V power supply (such as the PWR-5V or PWR-5V/E) to one of the external power connectors on the EXP-1600. The switch signal located on the EXP-1600 board must be set to external (EXT). If you set them to internal (INT), the EXP-1600 will not function and the KPCMCIA-12AI/16AI PC card may be damaged.

NOTE *The cables are keyed so you only can connect them one way.*

NOTE *EXP-1600 expansion boards have been modified so the current demand from the KPCMCIA-12AI/16AI is 300nA or less. To resume proper operation of the PC card, use revision H or later expansion boards. EXP-1600 boards previous to revision H demand excessive current from the KPCMCIA-12AI/16AI PC card. Refer to the EXP-800/1600 User's Guide for more information.*

Figure 5-2
Attaching an EXP-1600 expansion accessory



Attaching multiple EXP-1600 expansion accessories

You can attach up to 16 EXP-1600 expansion accessories to provide up to 256 analog input channels by attaching the expansion accessories in a daisy-chain configuration using a CAB-40 or CAB-40/1 cable.

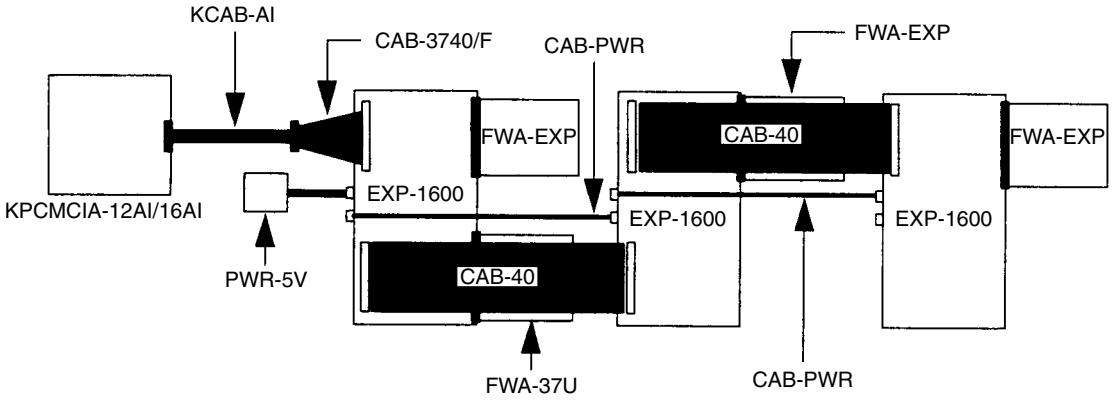
The first expansion accessory in the daisy chain is associated with on-card channel 0, the next expansion accessory is associated with on-card channel 1, etc. Specify the associated on-card channel by setting the jumper on each expansion accessory. Use a unique jumper setting for each expansion accessory.

You can access any unused on-card channels by attaching an FWA-37U field wiring accessory to the first EXP-1600 expansion accessory in the daisy-chain configuration.

To attach multiple EXP-1600 expansion accessories to the KPCMCIA-12AI/16AI PC card, refer to Figure 5-3 and perform the following steps:

1. Connect the first EXP-1600 to the KPCMCIA-12AI/16AI PC card as described in the previous paragraph. To connect additional EXP-1600 expansion accessories, attach one end of the CAB-40 (4 in. long) or CAB-40/1 (18 in. long) cable to either the P2 or P3 connector on the previous expansion accessory and attach the other end of the cable to either the P2 or P3 connector on the next expansion accessory in the chain. Note that P2 and P3 are identical connectors.
2. Attach +5V power to all the EXP-1600 expansion accessories. If desired, you can connect multiple EXP-1600s to a single PWR-5V or PWR-5V/E power supply using CAB-PWR or CAB-PWR/1 cables; attach one end of a CAB-PWR or CAB-PWR/1 cable to the unused power connector on the first expansion accessory and the other end of the cable to either power connector on the next expansion accessory in the chain. Note that the two power connectors are identical.

Figure 5-3
Attaching multiple EXP-1600 expansion accessories



A
Specifications

A/D converter	**12-Bit version**	**16-Bit version**
Acquisition + conversion	2µs + 8µs	2µs + 8µs
Monotonicity	No missing codes	No missing codes
Integral linearity error	±1 LSB	±3 LSB
Differential linearity error	±1 LSB	+3/-2 LSB
Full-scale error	±0.5%	±0.5%
Aperture delay	40ns	40ns

Analog input	
Number of input channels	Eight differential/16 single-ended, expandable to 256
Input range	±10, ±5, ±2.5, ±1.25V
Programmable gain	1, 2, 4, 8
Maximum overvoltage	±30V
Input impedance	100MΩ (DC)

A/D miscellaneous specifications	
Data FIFO depth	2048 samples
Scan list length	2048 entries
Scan speed	10µs, 20µs, 40µs
Trigger source	Internal (software)/External (TTL)
Trigger mode	Continuous/One-shot
External (TTL) trigger*	0.8V (low)/2.2V (high), rising/falling edges Latency to A/D scan < 1µs
Sampling Rate	0.006Hz to 100kHz (with internal clock source)
External clock rate*	DC-5MHz

**NOTE In "Paced" mode, the same input pin is shared between external clock and external trigger, therefore only one function can be used (not both simultaneously).*

Digital I/O	
Digital input channels	4 (no latch)
Digital output channels	4 (latched)
Maximum source current	0.5mA
Maximum sinking current	2.5mA
Minimum logic 1 level	2.4V
Maximum logic 0 level	0.8V

General specifications	
Power consumption	160mA (full power), 40mA (power down)
Operating temperature	0˚ to 50˚C
Storage temperature	0˚ to 70˚C
Humidity	0˚ to 95%, non-condensing
Size (cable not included)	Standard PCMCIA type II
Weight	1.5 oz (for reference only)

B
PCMCIA Interface

NOTE *A typical user of this manual does not need to read the material in this section. If you write a custom program, write it to work through DriverLINX, using the many interface and support features of DriverLINX. Register-level programming of the card is not recommended. This section is provided only for an advanced programmer who must write a specialized driver.*

Introduction

Information in this section is provided for those who need low-level PCMCIA interface details to the KPCMCIA-12AI/16AI PC card. The client driver or the enabler that comes with the PC card is sufficient for most applications.

The KPCMCIA-12AI/16AI PC card performs data acquisition for all host computers equipped with a version 2.1 compliant PCMCIA interface. The PC card, a name given to all PCMCIA interface cards, has a form factor of type II (5mm thick).

Due to the PCMCIA interface, the PC card is highly flexible with respect to addressing and interrupt level use. It can be configured either as a memory only interface or as an I/O interface and can be powered up or down with the help of the PCMCIA card and socket services software. The KPCMCIA-12AI/16AI PC card provides a single interrupt that can be routed to any system interrupt via the PCMCIA socket controller.

There are two sets of registers on the KPCMCIA-12AI/16AI PC card: the configuration registers and program registers.

The configuration registers are those as defined in the PCMCIA 2.1 specification. The PCMCIA configuration registers are located in the PC card's configuration space at offset 8000H. Configuration space also contains the Card Information Structure (CIS). This memory is located at offset 0000H in the configuration space. The CIS memory contains information about the PC card as defined by the PCMCIA 2.1 specification. Using the standard card and socket services software is the recommended method for setting up the configuration and power-up/down control of the PC card even though an enabler can be used.

Program registers are the registers that fall under program control and belong to the KPCMCIA-12AI/16AI PC card. The I/O location of these registers are controlled by the PCMCIA socket configuration and by the contents of the PCMCIA configuration registers. Refer to Appendix C for more information.

Two PCMCIA configuration registers are supported by the KPCMCIA-12AI/16AI PC card: the Configuration Option Register (COR) and the Card Configuration and Status Register (CCSR), as shown in Table B-1.

Table B-1
PCMCIA configuration registers

Offset	Access	Description
0x8000	R/W	Configuration option register
0x8002	R/W	Card configuration and status register

Configuration and option register (COR)

Refer to Table B-2. Bits 7 and 6 of the COR are defined by the PCMCIA standard as the SRESET and the LevlREQ bits. A 1 written into the SRESET bit puts the card into a reset state, while a 0 moves it out of the reset state. When the card is in the reset state, it behaves as if a hardware reset is received from the host. The LevlREQ bit controls the type of interrupt signal generated by the PC card. Setting the configuration index bits to 0 makes the PC card a memory only card (accessed only by memory read/write operations), while setting the bits to 1 makes the card a standard I/O card.

Table B-2
COR bit definitions

Bit	Name	Description
7	SRESET	1 = Put the card into reset state 0 = Get out of reset state
6	LevlREQ	1 = Level mode interrupt 0 = Edge mode interrupt
5-0	Index Bits	000000 = Memory mode 000001 = I/O mode

Card configuration and status register (CCSR)

Refer to Table B-3. The KPCMCIA-12AI/16AI PC card uses two bits in this register. When bit 1 is set to 1, it indicates a pending interrupt. The bit remains as 1 until the software clears the interrupt source. Bit 2 is used for power-down control. Setting this bit to 1 puts the card into power-down mode, while a 0 brings it back to full-powered mode. The rest of the bits are not used.

Table B-3
CCSR bit definitions

Bit	Name	Description
7-3	Not used	Reserved, all 0 when writing and reading
2	PwrDwn	1 = Power-down mode 0 = Full-powered mode
1	Intr	1 = Interrupt pending 0 = No interrupt pending
0	Reserved	Reserved as 0

The first S0-S3-S0 trip must be followed as described above. These two commands to the PC card must be issued: the flush scan list command (RSTQ) and then the flush data FIFO command (RSTF). The scan list is programmed after the RSTQ command and before the RSTF command. Once the flush data FIFO command is issued, the PC card prepares the first channel in the scan list, and then returns to state S0 to wait for the first trigger. This setup guarantees that the scan list and the data FIFO are flushed properly for the expected data acquisition.

NOTE *Any time the data FIFO is flushed, the default threshold setting will be restored (7 bytes to full) by the hardware. Always program the data FIFO threshold after the flushing if the required threshold is different from the default.*

C
I/O Registers

NOTE *A typical user of this manual does not need to read the material in this section. If you write a custom program, write it to work through DriverLINX, using the many interface and support features of DriverLINX. Register-level programming of the card is not recommended. This section is provided only for an advanced programmer who must write a specialized driver.*

Introduction

The KPCMCIA-12AI/16AI PC card uses eight consecutive I/O locations within the system I/O address space. The eight I/O locations used by the PC card are summarized in Table C-1.

Table C-1
KPCMCIA-12AI/16AI PC card register map

Address lines (A2A1A0)	I/O address	Port access	Register description
000	base + 0	Read/Write	Data FIFO
001	base + 1	Write only	Scan list (queue)
010	base + 2	Write Read	Control register Status register
011	base + 3	Write Read	Digital output register Digital input register
100	base + 4	Write only	Pacer clock, low byte
101	base + 5	Write only	Pacer clock, middle byte
110	base + 6	Write only	Pacer clock, high byte
111	base + 7	Write only	Auxiliary control register

All registers are 8-bit wide. Each register is discussed in detail in the following paragraphs.

Data FIFO register (base + 0)

The data FIFO register is the access port to the data FIFO, which can hold up to 2048 data words of the A/D conversion result. The port is also used to program the data FIFO thresholds, as explained later in this section.

NOTE *Although the data FIFO register is 8-bit wide, the register must be accessed as a 16-bit word to guarantee integrity. The low byte (LSB, or the least significant byte) should always be accessed first followed by the high byte (MSB, or the most significant byte).*

Two consecutive bytes should be read from (written into) the port each time it is accessed. Table C-2 illustrates the bit allocation.

Table C-2
Data FIFO register bit allocation

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LSB	D7	D6	D5	D4	D3	D2	D1	D0
MSB	D15	D14	D13	D12	D11	D10	D9	D8

Data FIFO operation modes

Depending on the mode of operation, the 16-bit word read from or written into the register has different meanings, as described in Table C-3.

Table C-3
Data FIFO operation mode

Mode	Selection bit	A/D	Access	Operation
0	0, threshold	Idle	Read Write	Verify data FIFO threshold Program data FIFO threshold
1	1, data FIFO	Idle	Read Write	Read data FIFO Write data FIFO (diagnosis)
2	0, threshold	Run	Read Write	Verify data FIFO threshold Not allowed
3	1, data FIFO	Run	Read Write	Read data FIFO Not allowed

The selection bit is also called the program/access control bit, as defined in the auxiliary control register (base + 7). Refer to "Auxiliary control register (base + 7, write only)" for more information about setting the bit and issuing commands to change the status of the A/D conversion (from scan to idle or vice versa).

Mode 0 is the FIFO program mode under which the two consecutive words (four bytes) written into the register address set the almost-full and almost-empty thresholds (in bytes). The first word specifies the almost-empty threshold (not used; can be set to anything), while the second word determines the almost-full threshold. The threshold should be set to a value from 1 to FIFO size minus 1 (default is 7 when reset or power up). Refer to Table C-4.

Table C-4
Data FIFO threshold setting

Threshold	Default	Threshold range	Suggested value
Almost empty	7	Irrelevant	Irrelevant
Almost full	7	1..4095 bytes	2048 bytes

Mode 1 is the FIFO test mode in which the data bytes are written into the data FIFO and read back from it. The FIFO flags change according to the data bytes available in the data FIFO and the configured threshold. Refer to "Status register (base + 2, read)" for information about the FIFO empty, almost-full, and full flags.

Mode 2 should be avoided. The data bytes cannot be written into the FIFO under this mode. The bytes read from the FIFO will be the same as in mode 0.

Mode 3 is the data transfer mode. Data bytes are written into the FIFO by the A/D converter, while the data byte read from the address is the first available byte in the data FIFO if it is not empty. Otherwise, the most recent byte written into the FIFO will be returned. The data FIFO register is read-only under this mode; i.e., you cannot write data bytes into the data FIFO through I/O instructions.

Mode setting

The FIFO operation mode setting is always initiated with the data FIFO flush command refer to "Auxiliary control register (base + 7, write only" with the access/program bit set to 0 (bit 0 at base + 7) before the data acquisition is started. This setting brings it to mode 0 (threshold setting mode). After the threshold is programmed or verified, set the bit to 1 so the following read/write operation to the FIFO is the data access operation.

The KPCMCIA-12AI/16AI PC card is in idle mode before it is triggered into the run mode. For one-shot operation, the PC card is set to run mode after it receives the trigger signal. It does not return to the idle mode until the specified scan list is completed or an A/D stop command is received. Refer to "Stop A/D command" for more information. For continuous trigger operation, the PC card will stay in run mode after being triggered until an A/D stop command is received.

FIFO flags

When reading the register under mode 1 or 3, the first available data byte from the data FIFO is returned if it is not empty. Otherwise, the returned byte is not defined. The FIFO empty flag will be set immediately after the last byte is read from the FIFO, while the FIFO full flag will be cleared after reading the data FIFO register provided there are no more data bytes written into the FIFO by the A/D converter under mode 1 or 3. The same happens to the FIFO almost-full flag if the data bytes available in the FIFO are less than the almost-full threshold. Refer to Table C-5. In the first column of Table C-5, threshold is the almost-full threshold as explained before, and FIFO size is measured in bytes, 4096.

Table C-5
Data FIFO flag status

Data bytes in FIFO	Empty	Almost full	Full
0	True	False	False
1 to (Threshold - 1)	False	False	False
Threshold to (FIFO size - 1)	False	True	False
FIFO size (4096 bytes)*	False	True	True

* 2048 samples/data words.

Scan list queue register (base + 1, write only)

The scan list queue register is the access port to the scan list queue, which can hold up to 2048 entries (each has two bytes). Each entry specifies an analog input channel and its associated gain as well as other settings.

NOTE *Although the scan list queue register is eight bits wide, the register must be accessed as a 16-bit word to guarantee integrity. The low byte (LSB, or the least significant byte) should always be accessed first followed by the high byte (MSB, or the most significant byte).*

The bit definitions of entries to the scan list queue are explained in Table C-6.

Table C-6
Scan list queue entry bit definitions

Bit	Byte	Definition	Explanation
15	MSB	Reserved	as 0
14	MSB	Analog input mode	1/0 : differential/single-ended
13-12	MSB	Internal gain selection	00/01/10/11 : 1/2/4/8
11-8	MSB	Internal channel selection	0000..1111 : channel 0..15
7	LSB	Starting channel mark	Set to 1 for the first entry in the list Set to 0 for all the rest entries
6	LSB	Reserved	for expansion cards (as SSH)
5-4	LSB	External gain selection	00/01/10/11 : 1/2/4/8 (or 1/10/100/1000)
3-0	LSB	External channel selection	0000..1111 : channel 0..15

Scan list queue programming

The scan list queue must be programmed when the KPCMCIA-12AI/16AI PC card is idle. Each queue entry contains two bytes as described previously. The integrity of the entry must be guaranteed. The scan list queue is write only.

The scan list queue should be flushed before writing any entries into it. Refer to "Auxiliary control register (base + 7, write only)" for scan list queue reset information.

The first entry of the queue should have bit 7 (LSB) set to 1 as the first channel mark. All the rest of the entries, if any, should have the bit set to 0.

The synchronous sample hold bit (LSB) is not used by the PC card. It is reserved for the expansion cards.

Example 1

In Table C-7, the following entries to the queue specify a scan list of three single-ended internal channels, 0, 12, and 7, with a gain of 2 for channel 0 and a gain of 4 for channel 12 and 7.

Table C-7
Scan list queue programming example 1

Entry	Binary	Hex	Explanation
1	0001 0000 1000 0000	0180	Select channel 0, gain 2, first entry
2	0010 1100 0000 0000	2C00	Select channel 12, gain 4
3	0010 0111 0000 0000	2700	Select channel 7, gain 4

Example 2

In Table C-8, the following entries to the queue specify a scan list of four differential internal channels, 2, 1, 6, and 7, with a gain of 1 for all the channels.

Table C-8
Scan list queue programming example 2

Entry	Binary	Hex	Explanation
1	0100 0010 1000 0000	4280	Select channel 2, gain 1, first entry
2	0100 0001 0000 0000	4100	Select channel 1, gain 1
3	0100 0110 0000 0000	4600	Select channel 6, gain 1
4	0100 0111 0000 0000	4700	Select channel 7, gain 1

Channel configuration

Bits 5 and 4 (LSB) in a queue entry specify the gain on the external expansion card for the external channel selected by bits 3 through 0 of the same byte. Each expansion card has up to 16 channels (0, 1, 2, ..., 15). Each channel may have a gain of 1, 2, 4, or 8 if it is a low gain expansion card or 1, 10, 100, or 1000 if it is a high gain expansion card.

If there is no expansion card for the specified internal channel, the external channel and gain selection in the LSB is ignored. However, the first channel mark on bit 7 should always be set properly.

The internal channel is selected by bits 8 through 11 (MSB), while the internal gain for the selected channel is specified by bit 12 and 13 (MSB). The internal gain can only be 1, 2, 4, or 8.

Bit 14 (MSB) determines whether the input is differential (1) or single-ended (0). There are 16 singled-ended channels but only eight differential channels. This bit should always be set to 0 if the selected internal channel is connected to an expansion card because the output from the expansion cards is always single-ended.

Bit 15 (MSB) is not used by the KPCMCIA-12AI/16AI PC card. It should be set to 0.

Analog input offset correction

The input to the A/D converter will be shorted to ground if bit 14 (MSB) is set to 1 while the internal channel selection of bits 8 through 11 specifies internal channel 8 or above. This can be used for analog input offset correction.

Control register (base + 2, write)

The control register specifies the pacer clock source and pre-scaler, the expansion mode, interrupt enable control, and the trigger control as shown in Table C-9.

Table C-9
Control register bit definitions

Bit	Function	Explanation
7-6	Pacer clock source and pre-scaler	00 : External clock 01 : Internal, 5MHz 10 : Internal, 1MHz 11 : Internal, 100kHz
5	Expansion mode	0/1 : disable/enable
4	EOS interrupt	0/1 : disable/enable
3	FIFO interrupt	0/1 : disable/enable
2	Trigger mode	0/1 : one-shot/continuous
1	Trigger source	0/1 : internal/external
0	Trigger edge	0/1 : rising/falling

Clock source

The external clock source, if selected, must not exceed 5MHz with a minimum pulse width of 200ns. The external clock frequency can be as low as DC, and there is no limit on maximum pulse width.

Expansion mode

Bit 5 has to be set to 1 if there is one (or more) expansion cards connected to the KPCMCIA-12AI/16AI PC card. This setting also means that all the digital output lines (bits 0 to 3) will be used for external channel selection and two of the four digital input lines (bits 1 and 3) will be used for external gain selection.

Interrupt enable

Bits 4 and 3 are used for interrupt enable control. The end-of-scan (EOS) interrupt is enabled (disabled) by setting bit 4 to 1 (0). Setting bit 3 to 1 (0) enables (disables) the data FIFO interrupt when the A/D data FIFO becomes almost full (data available in the FIFO passes the almost-full threshold). Since the EOS and FIFO threshold events are latched into the status register, temporarily disabling the interrupt and then enabling it will not lose an interrupt as long as no repeated events occur during the time the interrupt is disabled.

Trigger mode

Bit 2 determines the trigger mode. It is set to 0 for the one-shot mode in which each trigger signal, internal or external starts one scan of input analog channels specified by the scan list. Bit 2 should be set to 1 for the continuous trigger mode in which the trigger signal, internal or external, starts the first scan of the input analog channels specified by the scan list. The pacer clock then initiates the subsequent scans each time it fires until the stop A/D command is received.

Trigger source

Bit 1 specifies the trigger source. It is set to 1 for external trigger (TTL trigger) and 0 for internal trigger (software trigger). When it is set to internal trigger, the trigger edge selection can be ignored. The external trigger signal shares the same pin on the interface connector with the digital input bit 0.

Trigger edge

Bit 0 selects the external trigger edge. The falling edge of the external trigger signal is chosen as the trigger edge if the bit is set to 1. Otherwise, the rising edge is selected. The edge selection is ignored if the internal trigger source is specified.

Status register (base + 2, read)

The status register is read only. It shares the same offset as the control register. It reports data FIFO flag status, interrupt status, and A/D conversion status as shown in Table C-10.

Table C-10
Status register bit definitions

Bit	Status	Explanation
7	Scanning status	0/1 : busy/idle
6	Triggered status	0/1 : no/yes
5	Data lost event	0/1 : no/yes
4	End of scan event	0/1 : no/yes
3	FIFO threshold event	0/1 : no/yes
2	Data FIFO full	0/1 : false/true
1	Data FIFO almost full	0/1 : false/true
0	Data FIFO empty	0/1 : false/true

Bit 7 shows the scanning status. It is 0 when the PC card is in the process of scanning the input channels specified by the scan list and 1 when it is done.

A 1 at bit 6 indicates that the PC card has been triggered and is doing the data acquisition (busy). Bit 6 is 0 means it is waiting for a trigger (idle).

Bits 3, 4, and 5 are the event latches. When an event is detected, the corresponding bit is set to 1 until the host reads the status register, which clears all the event bits to 0. Bit 5 is used for data lost event, bit 4 for end-of-scan (EOS), and bit 3 for the FIFO threshold event. When the corresponding interrupt is enabled, a 1 in bit 3 (or bit 4) also causes an interrupt.

Bits 0, 1, and 2 are the data FIFO flags.

Digital output register (base + 3, write)

The four digital output lines share the same pins on the interface connector with the four external channel selection bits. When using the expansion cards, bit 5 of the control register (base + 2) should be set to 1, so the four lines are driven by the external channel selection bits from the scan FIFO. On the other hand, the four output lines will be driven by the values in bits 0 to 3 latched during the last write operation if bit 5 of the control register is set to 0 (default after reset). In other words, the digital output bits are only valid when KPCMCIA-12AI/16AI PC card is not in expansion mode. They will be ignored otherwise. Refer to Table C-11 for bit definitions.

Table C-11
Digital output register bit definitions

Bits	Normal mode	Expansion mode
0-3	Digital output bit 0-3	Ignored. The four output lines will be driven by the external channel selection bits in the scan list FIFO.
4-7	Reserved as all 0	Ignored.

Digital input register (base + 3, read)

As mentioned before, two of the digital input lines are shared with external trigger (bit 0) and external clock (bit 2). The other two lines are also used for external gain control in the expansion mode. If bit 2 of the control register is set to 1, refer to "Control register (base + 2, write)." The digital input lines are not latched. Table C-12 shows what is returned when reading this port.

Although the digital input lines are also used as external trigger, external clock, and the external gain selection, the current status of these lines is always returned when reading the port. However, the line status has nothing to do with the digital output register whose contents cannot be read back directly even though they share the same port offset with the digital input register.

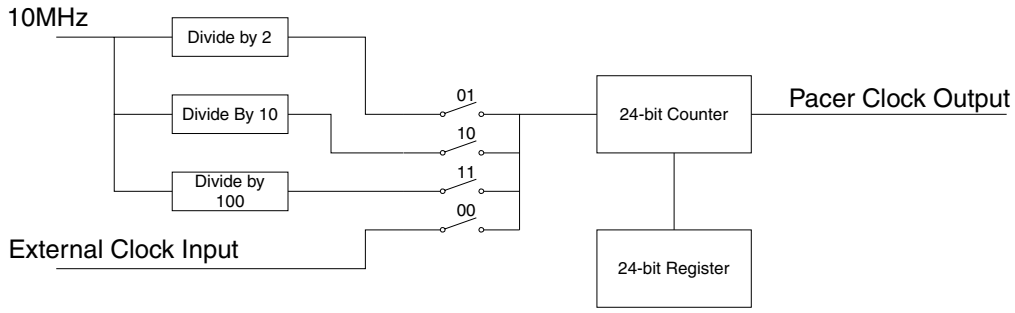
Table C-12
Digital input register bit definitions

Bits	Normal mode	Expansion mode
0	Digital input bit 0, also serve as external trigger	The same as in normal mode
1	Digital input bit 1	External gain select, low bit
2	Digital input bit 2, also serve as external clock	The same as in normal mode
3	Digital input bit 3	External gain select, high bit
4-7	All 0	All 0

Pacer clock (base + 4, + 5, + 6, write only)

The pacer clock is actually a 24-bit auto-reload frequency divider. It contains a 24-bit divisor register, a 24-bit counter, an internal clock pre-scaler and a clock source multiplexer, as shown in Figure C-1.

Figure C-1
Pacer clock block diagram



The clock source selection is specified by bit 6 and 7 in the control register. Refer to the paragraph, "Control register (base + 2, write)." The 24-bit register occupies three ports in which the low byte is located at base + 3, the middle byte at base + 4, and the high byte at base + 5. All three registers are write only. The pacer clock will not generate any clock pulse output until it is triggered (either by an internal software trigger or an external TTL trigger signal) and the trigger mode is not one-shot. In continuous mode, the trigger serves as the first clock output pulse and loads the counter from the register. The counter counts down the input clock pulse until it reaches zero. An output clock pulse is generated and the counter is reloaded. The pacer clock generation continues until the KPCMCIA-12AI/16AI PC card receives the stop command, represented by writing a 1 at bit 4 of the auxiliary control register. Refer to the following paragraph for further auxiliary control register information.

The clock rate generated can be determined by the equation, (Source Frequency) / (Divisor Count + 1). For example, if the clock source is 100kHz (internal clock, control register bit 7,6 = 11), and the divisor count is 49, then the pacer clock output frequency will be 2kHz. If an external clock source (control register bit 7,6 = 00) of 120kHz is applied, and the divisor count is 39, the pacer clock will then be set at 3kHz.

Auxiliary control register (base + 7, write only)

The auxiliary control register is used to send control commands to the KPCMCIA-12AI/16AI PC card. It also sets the data program/access mode for the data FIFO. The command bits (bits 4 to 7) are actually monostable or self-cleared after the specified command function is completed. They do not need to be cleared. However, the data FIFO program/access bit is latched each time it is written. Refer to Table C-13 for these bit definitions.

Table C-13
Auxiliary control register bit definitions

Bit	Function	Explanation
7	Trigger/Arm command	1 = send trigger/arm, 0 = no action
6	Flush data FIFO command	1 = flush, 0 = no action
5	Flush scan list command	1 = flush, 0 = no action
4	Stop A/D command	1 = stop, 0 = no action
3	Reserved	as 0
2-1	Scan rate selection	00 = 100, 01 = 50, 10 = 25 (kHz)
0	Data FIFO program/access	1 = data access, 0 = program threshold

Trigger/arm command

If the trigger source is internal (software trigger), writing a 1 at bit 7 will send a trigger to the PC card and start the A/D conversion process. If the trigger source is external (TTL trigger), writing a 1 to bit 7 will serve as an ARM command, which tells the PC card to look for the specified external trigger edge from the moment the ARM command is received. This command should never be issued with the stop A/D command. The data acquisition will be initiated after this command is received. Only the stop A/D command can terminate the acquisition.

Flush data FIFO command

The data FIFO should be flushed before the data acquisition can be initiated by the trigger/arm command but after the scan list is set up. The flush command may also be followed by FIFO threshold programming. After the FIFO is flushed, the FIFO empty flag will be set to 1 and the almost-full and full flag reset to 0. The flush FIFO command always sets the FIFO thresholds to the default setting (7 bytes to full) at power up or reset.

NOTE *Any time the data FIFO is flushed, the default threshold setting will be restored (7 bytes to full) by the hardware. The data FIFO threshold should always be programmed after the flushing if the required threshold is different from the default one.*

Flush scan list queue command

The scan list queue needs to be flushing before it can be programmed. This command should be issued before the flush data FIFO command. The queue may have up to 2048 word entries, each containing two bytes. It is your responsibility to guarantee the integrity of the entries. Refer to "Scan list queue register (base + 1)" for more information about the scan list queue.

Stop A/D command

Once the data acquisition is started by the trigger/arm command, it can only be stopped by receiving this command. As mentioned before, the two commands are exclusive. The stop A/D command should be issued as soon as the required data points are collected to prevent data FIFO overflow, which is the only flag to indicate data lost during the data acquisition process. Without the stop command, the A/D may still be running and filling data into the data FIFO whether it is filled or not. When the data FIFO is full, it will ignore the data samples coming from the A/D converter.

Data FIFO program/access control

The A/D data FIFO has two programmable thresholds, almost empty and almost full, and two associated flags. The almost-empty threshold and the almost-empty flag are not used. By default, the thresholds are set to 7 bytes (7 to full and 7 to empty) when reset, powered up, or any time the FIFO is flushed. It can be programmed to any value in between 1 and FIFO size - 1 (in bytes), according to the application. For example, it can be set to the length of the scan list, half to full or quarter to full, etc.

To program the FIFO threshold, make sure the A/D has been stopped. Set this bit to 0 by writing an all-zero byte to the auxiliary control register. Then, send a flush A/D FIFO command with the same bit setting by writing a byte of 40H (hex 40) to the same register. This setting will put the FIFO into program mode. The following read/write operation will be directed to the threshold registers when accessing the data FIFO at base + 1. The 4-byte threshold setting should be written into the data FIFO by doing four consecutive write operations. Optionally, the threshold setting can be read back for verification by doing four consecutive read operations. The 4-byte threshold setting has the following format as shown in Table C-14.

Table C-14
Data FIFO threshold setting

Byte no.	Definition	Valid range
0	Low byte of the almost empty threshold	0..255
1	High byte of the almost empty threshold	0..15
2	Low byte of the almost full threshold	0..255
3	High byte of the almost full threshold	0..15

After the thresholds are programmed, set the access control bit to 1 by writing a byte of 01H into the auxiliary control register. This will make the following read/write operation access the data bytes in the FIFO instead of its thresholds. The access control bit must be set to 1 when sending other commands (flush scan list, stop A/D, or trig/arm) to the KPCMCIA-12AI/16AI PC card by writing into the auxiliary control register after programming the thresholds. For safe operation, set the bit to 0 only when flushing and programming the FIFO thresholds.

Although the almost-empty threshold is never used, it has to be programmed because the four configuration bytes must be accessed as a whole entity.

Scan rate selection

Depending on the input mode and the gain selection, the analog front end may have different settling times. To keep the best performance, the KPCMCIA-12AI/16AI PC card lets you choose three different scanning rates by setting bit 2 and bit 3 while the start A/D command is issued. The default scanning rate is 100kHz (bit 3-2 set to 00). 50kHz rate can be selected by setting the bits to 01, and 25kHz can be selected by setting the bits to 10. Setting the bits as 11 is the same as 01.

The scan rate setting must be issued together with the trigger/arm command and not changed during data acquisition. For example, writing 81H to the auxiliary control register will start the data acquisition with the scan rate set to 100kHz (use 83H for 50kHz and 85H for 25kHz).

Index

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Specifications are subject to change without notice.

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4/02