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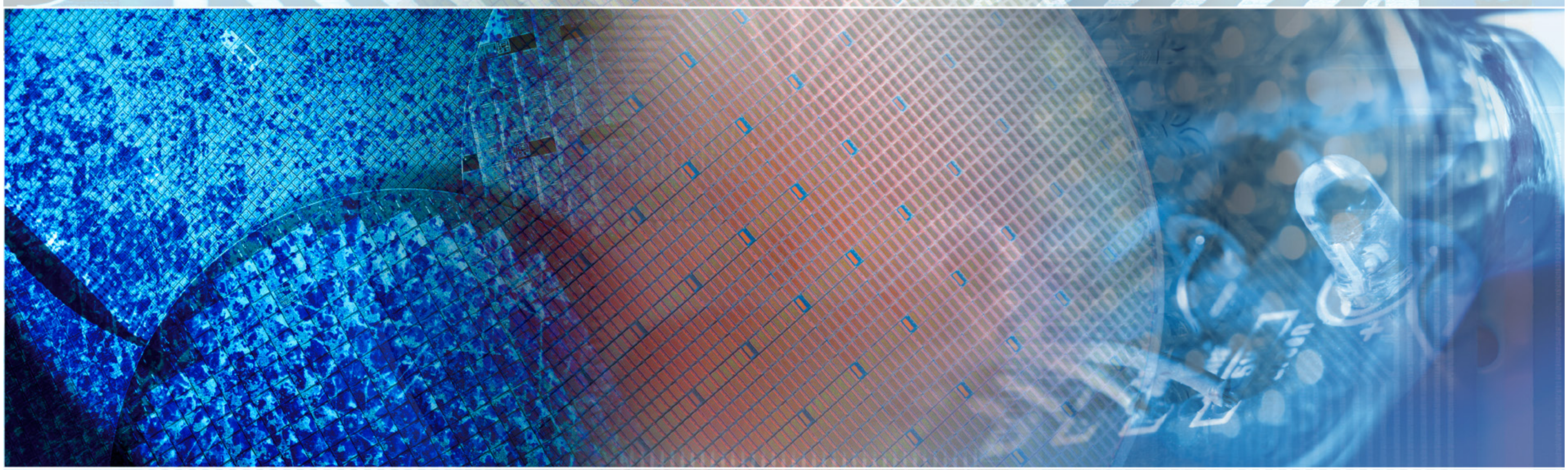
A GREATER MEASURE OF CONFIDENCE

Learn how to solve today's semiconductor device characterization challenges.



INSIDE:* *Instant online access to application notes, webinars, demos, and more

Accurate Channel Effective Mobility Analysis Using the Ultra-Fast Single Pulse (UFSP) Technique

The channel effective mobility (μeff) influences the MOSFET performance through the carrier velocity and the driving current. It is one of the key parameters for complementary metal-oxide-semiconductor (CMOS) technologies. It is widely used for benchmarking differences in technology development and material selection. It is also a fundamental parameter for device modeling. With device scaling down to nano-size regime and the introduction of new dielectric materials, the conventional measurement technique for mobility does not address these issues, leading to significant measurement errors. As a result, an ultra-fast single pulse technique (UFSP) has been developed to overcome these shortcomings. **Learn more.**

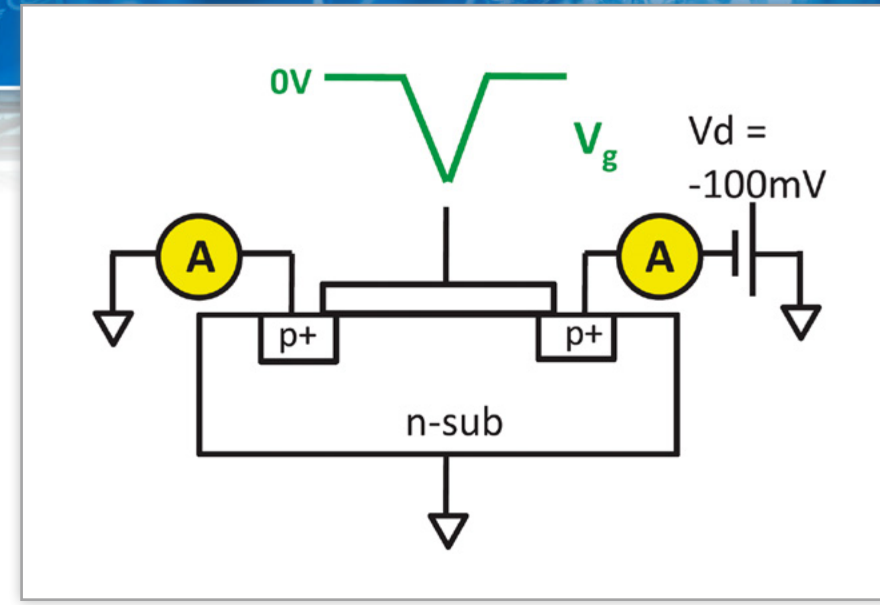
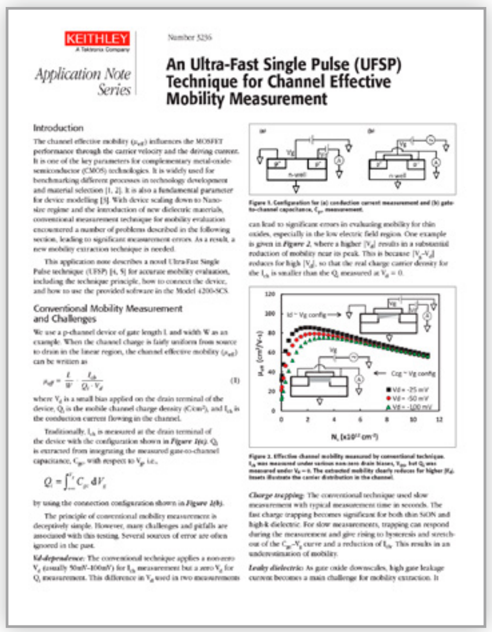
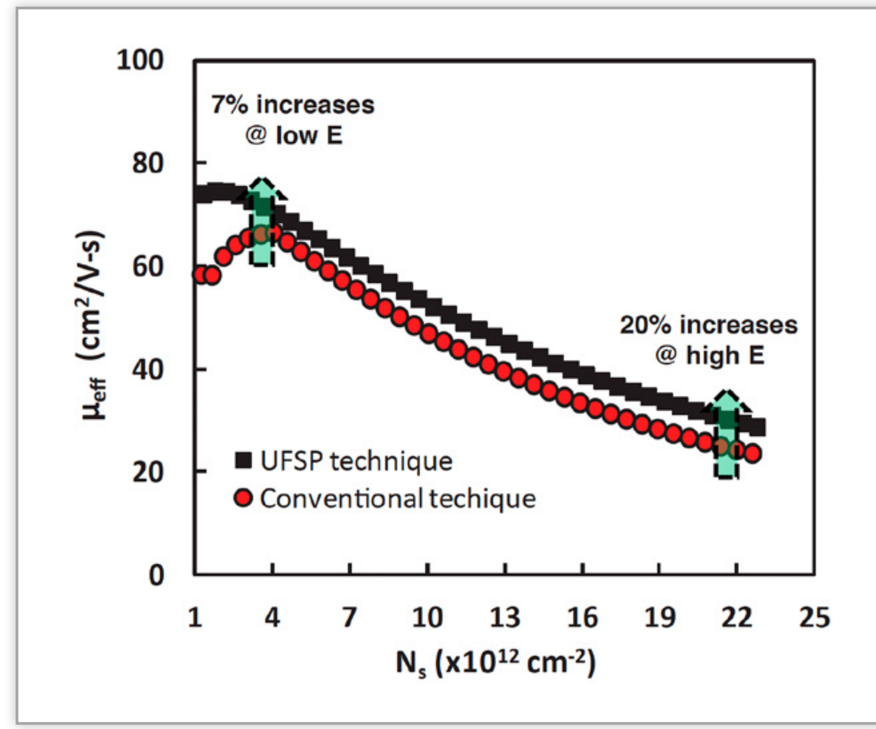


Illustration of the working principle of UFSP Technique.



Want to learn more?

Download our free online application note to learn how to use the UFSP Technique.



A comparison of mobility extracted by UFSP and conventional technique for a device with HfO2/SiON dielectric of considerable fast trapping.

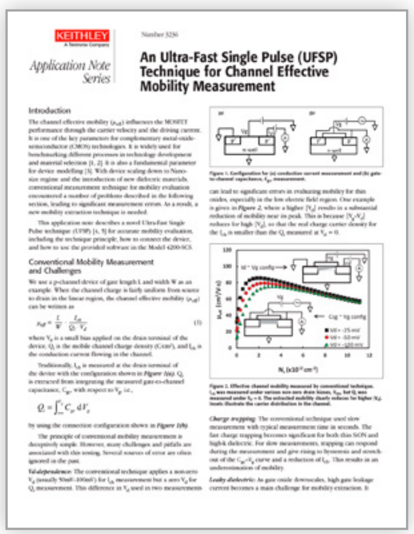
Get advice for your application.

Send us your question or **join the discussion on our application forum.**

A Solution with Everything You Need for Precise, Expedient, and Easy Mobility Evaluation

Channel carrier mobility is a key parameter for material selection and process development. But, the conventional technique poses several challenges, such as slow speed and vulnerability to fast trapping, Vd-dependence, cable-changing, and sensitivity to gate leakage, in addition to being a complex procedure. But, with the combination of a Keithley's **Model 4200-SCS Semiconductor Parameter**, two **Model 4225-PMU Ultra-Fast I-V modules**, and four **Model 4225-RPM Remote Amplifier/Switch** units, ultra-fast I-V sourcing and measurement is as easy as making DC measurements with a traditional high resolution source measure unit (SMU) instrument. This complete solution provides everything needed for robust and accurate and convenient mobility evaluation, as well as a tool for process development, material selection, and device modeling for CMOS technologies.

Photo of the UFSP Technique setup using Keithley instruments.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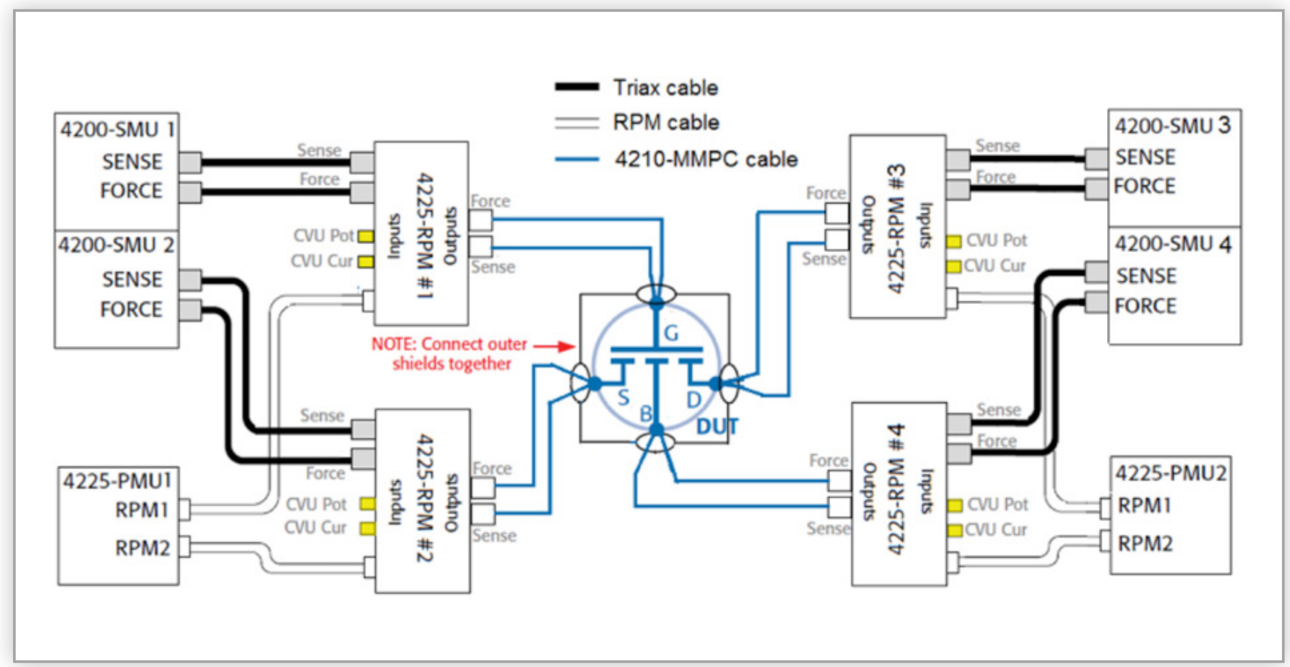
Application Note Series
An Ultra-Fast Single Pulse (UFSP) Technique for Channel Effective Mobility Measurement

Want to learn more?

Download our free online application note to learn how to use the UFSP Technique.



Experiment connection for the Ultra-fast Single Pulse (UFSP) Technique. Two Keithley dual-channel Model 4225-PMUs are used for performing transient measurements. Four Keithley Model 4225-RPMs are used to reduce cable capacitance effect and achieve accurate measurement below 100nA.

Want assistance, a quote, or to place an order?

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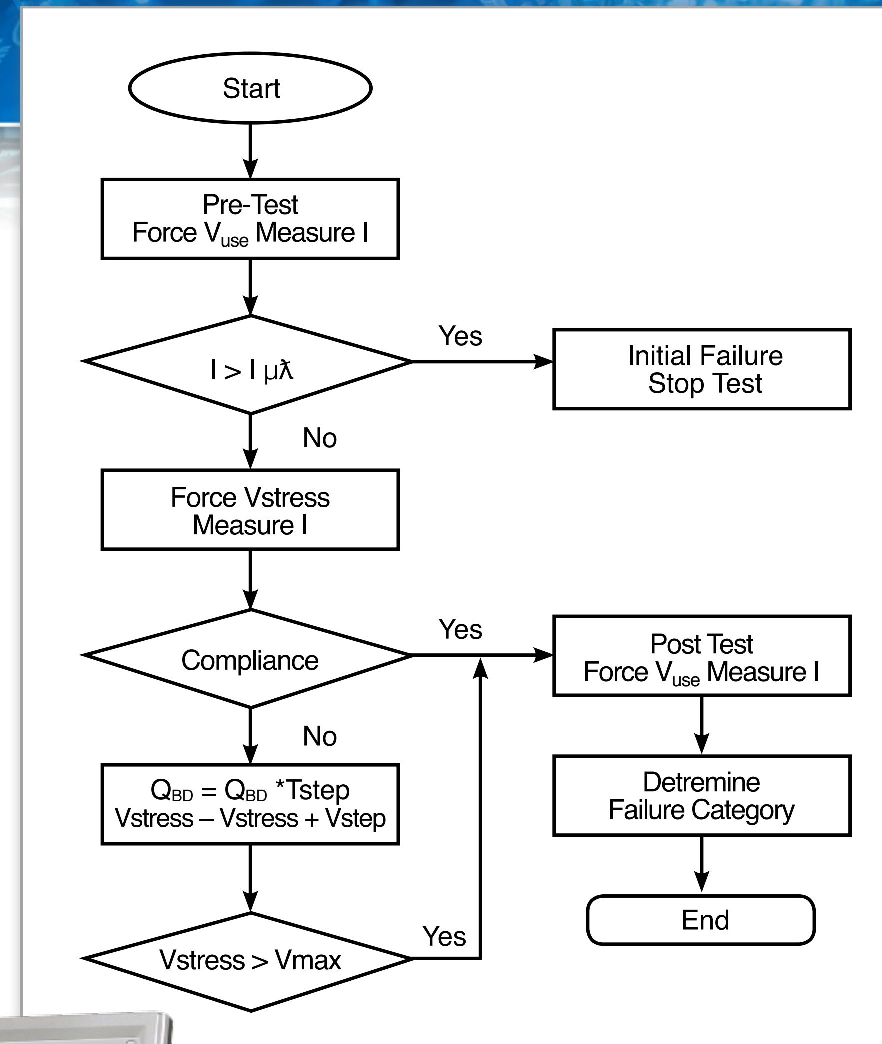
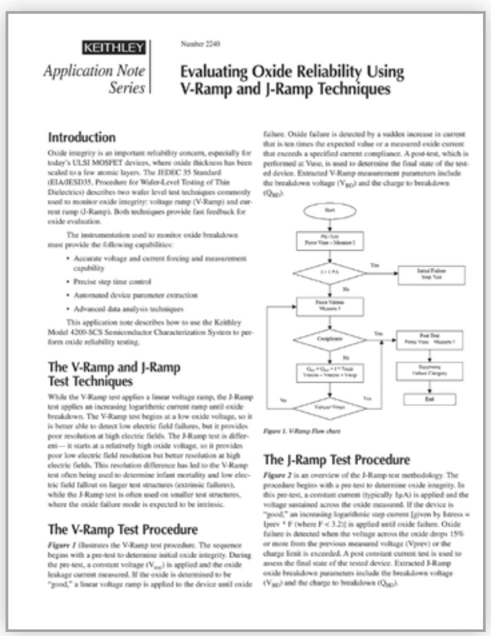
Monitor oxide breakdown with confidence.

Oxide integrity is an important reliability concern, especially for modern ULSI MOSFET devices, where oxide thickness has been scaled to a few atomic layers. The JEDEC 35 Standard (EIA/JESD35, Procedure for Wafer-Level Testing of Thin Dielectrics) describes two wafer level test techniques commonly used to monitor oxide integrity: voltage ramp (V-Ramp) and current ramp (J-Ramp). Both techniques provide fast feedback for oxide evaluation. **Learn more.**



A V-Ramp test procedure begins with a pre-test to determine initial oxide integrity. During the pre-test, a constant voltage (V_{use}) is applied and the oxide leakage current measured. If the oxide is determined to be "good," a linear voltage ramp is applied to the device until oxide failure. Oxide failure is detected by a sudden increase in current that is ten times the expected value or a measured oxide current that exceeds a specified current compliance. A post-test, performed at V_{use}, is used to determine the final state of the tested device. Extracted V-Ramp measurement parameters include the breakdown voltage (V_{BD}) and the charge to breakdown (Q_{BD}).



Want to learn more?

Download our free online application note.

Keithley's Model 4200-SCS Semiconductor Characterization System offers a cost-effective solution for oxide reliability testing.

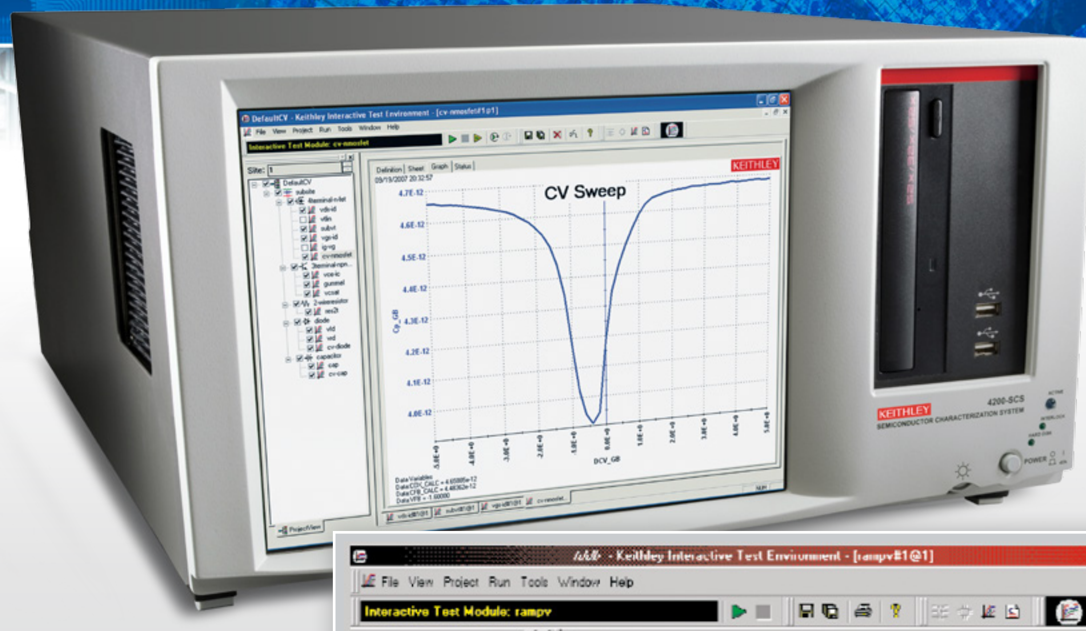
Learn more about the Model 4200-SCS.

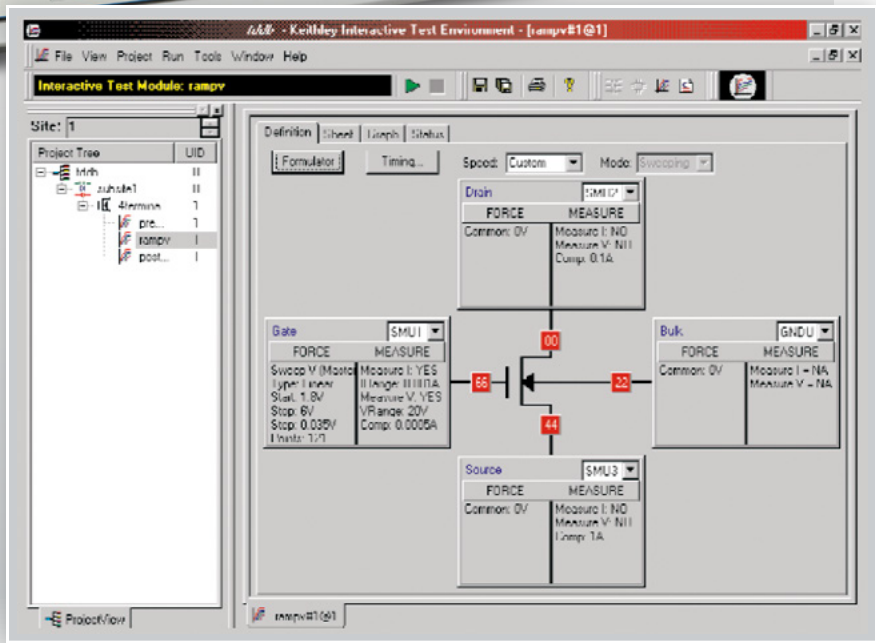
Get advice for your application.

Send us your question or join the discussion on our application forum.

Get the accurate oxide integrity data you need easily with the Model 4200-SCS Semiconductor Characterization System.

Monitoring oxide breakdown demands instrumentation capable of providing accurate voltage and current forcing and measurement, precise step time control, automated device parameter extraction, and advanced data analysis techniques. The **Model 4200-SCS's** built-in test sequencer and Interactive Test Module (ITM) capability simplify implementing both V-Ramp and J-Ramp test algorithms, as illustrated in V-Ramp test sequence shown below. The Project Navigator window displays the test sequence, which begins with a pre-test, followed by a linear voltage ramp to oxide breakdown. A post-test determines the final device state.





V-Ramp project test sequence and test definition.

Need more details about the Model 4200-SCS Semiconductor Characterization System?
Download the datasheet.

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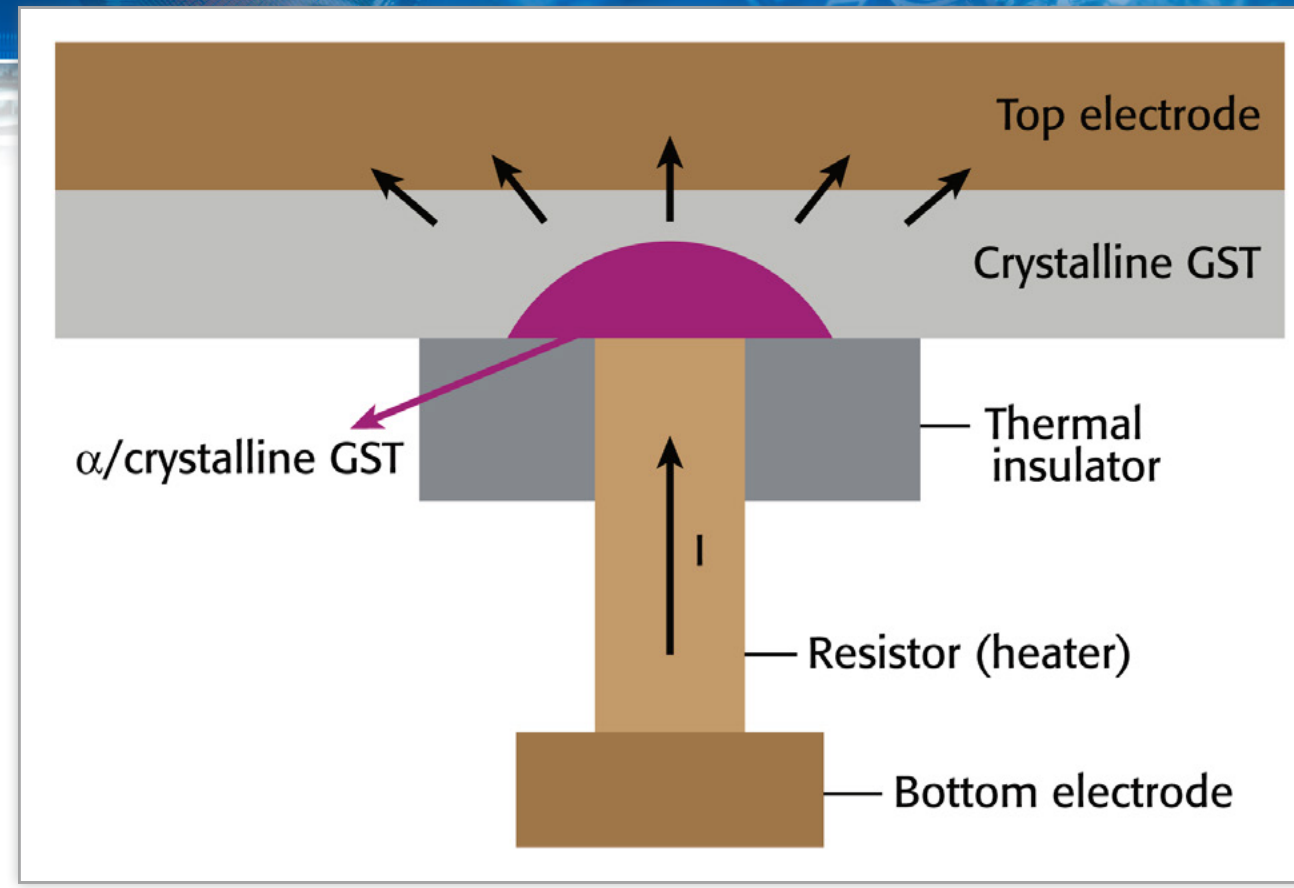
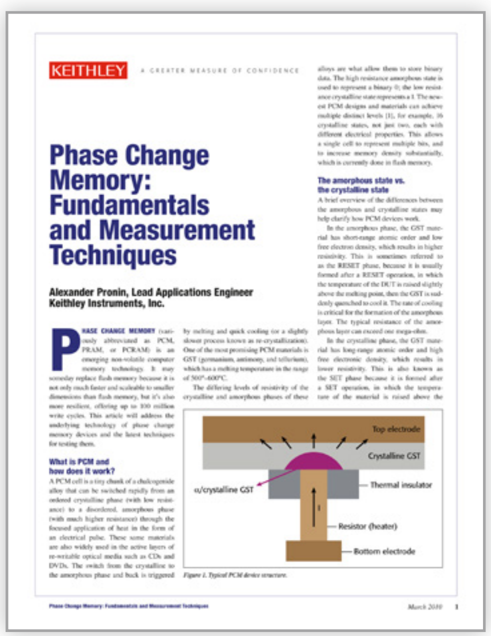
Characterize highly advanced phase change memory devices.

A phase change memory (PCM) cell is a tiny chunk of a chalcogenide alloy that can be switched rapidly from an ordered crystalline phase (with low resistance) to a disordered, amorphous phase (with much higher resistance) through the focused application of heat in the form of an electrical pulse. The differing levels of resistivity of the crystalline and amorphous phases are what allow them to store binary data. The ability to develop new PCM materials and refine device designs will depend largely on manufacturers' ability to characterize several parameters accurately, including recrystallization rate, data retention, cycling endurance, drift of the cell's resistance over time, impact of the "read" procedure on the stored state, and resistance-current (RI) and I-V curves. **Learn more.**



GST (germanium, antimony, and tellurium) is one of the most promising PCM materials: in its amorphous phase, its typical resistance can exceed 1MΩ; in the crystalline phase, it ranges from 1 to 10kΩ.



Want to learn more?

Download our free online article.

View our webinar, **Phase Change Memory - Fundamentals and Measurement Techniques.**

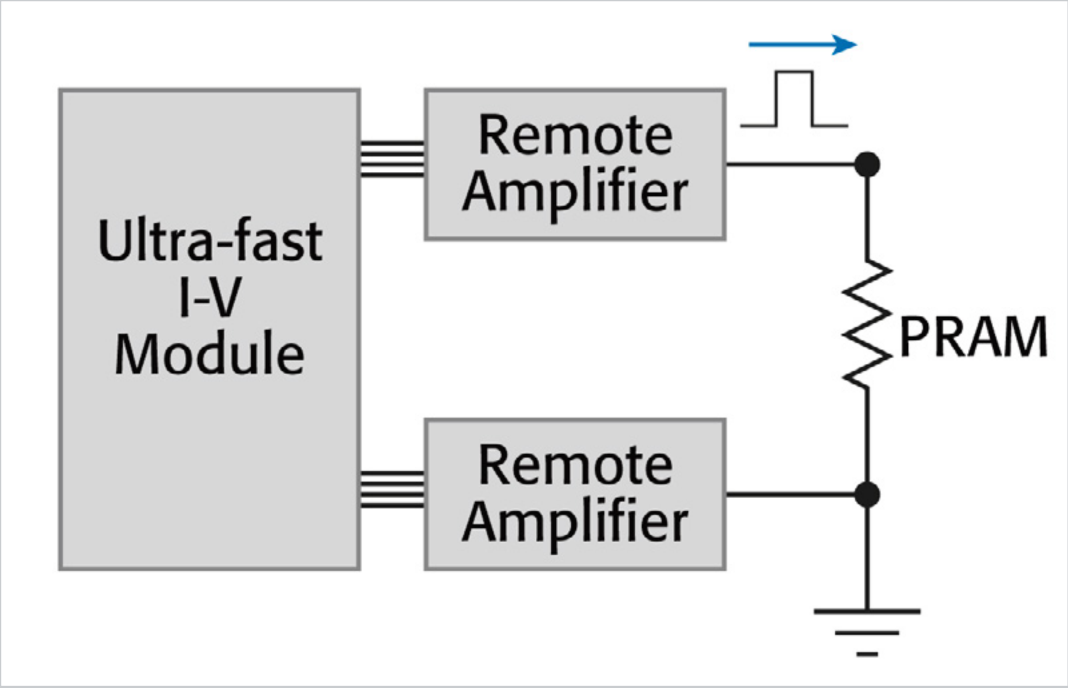
Get advice for your application.

Send us your question or **join the discussion on our application forum.**

Shorten PCM test times with the Model 4225-PMU Ultra-Fast I-V Module.

The **Model 4225-PMU Ultra-Fast I-V Module** offers the ideal solution for testing single memory cells or a small array of cells, such as when isolated cells need to be tested in research and development or for process verification. Because the 4225-PMU can be used for both the pulsing and measurement, total test time is reduced. The **Model 4225-PMU** and the **Model 4225-RPM Remote Amplifier/Switches** that extend its sensitivity are designed to integrate with the Model 4200-SCS Semiconductor Characterization System, which not only provides a wide range of other measurement functions necessary to characterize a PCM device but offers the ability to automate the entire testing process.

The dynamic switch from a high- to a low-resistive state in the presence of a load resistor produces a characteristic RI curve with a snapback, an area of negative resistance. Snapback itself is not a feature of PCMs or of PCM testing but rather a side effect of the R-load technique long used to obtain both RI and I-V curves. The Model 4225-PMU eliminates the need for the load resistor, as well as the snapback side effect problem, and provides tight control over the level of current sourced for more accurate characterization of low currents in the RI curve. The Model 4225-PMU can source voltage and simultaneously measure both voltage and current responses with high accuracy, with rise and fall times as short as 20ns.



Want to learn more about the Model 4225-PMU?

To learn more about ultra-fast I-V sourcing and measurement techniques, download our Ultra-Fast I-V applications e-book.

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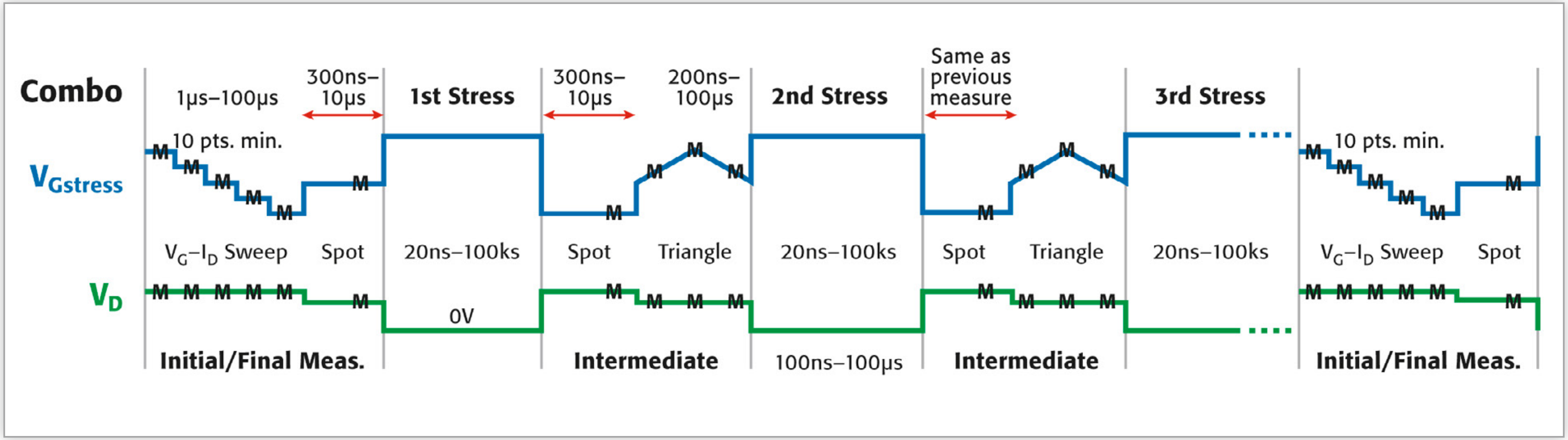
Model and monitor Bias Temperature Instability (BTI) for CMOS transistors.

Modeling negative bias temperature instability (NBTI) is a challenge when developing deeply scaled silicon CMOS transistor designs. Over time, NBTI effects cause a transistor's threshold voltage (V_T) to shift and its sub-threshold drain current to increase significantly, severely limiting transistor lifetime and circuit performance. These effects must be accurately modeled during device development and monitored during process integration and production. During BTI characterization, the transistor is alternately stressed and characterized. However, the BTI mechanism is susceptible to relaxation effects, which means that the instant the stress is removed, the transistor starts to recover and the degradation fades. Characterizing the degradation prior to relaxation demands the use of ultra-fast I-V techniques. **Learn more.**



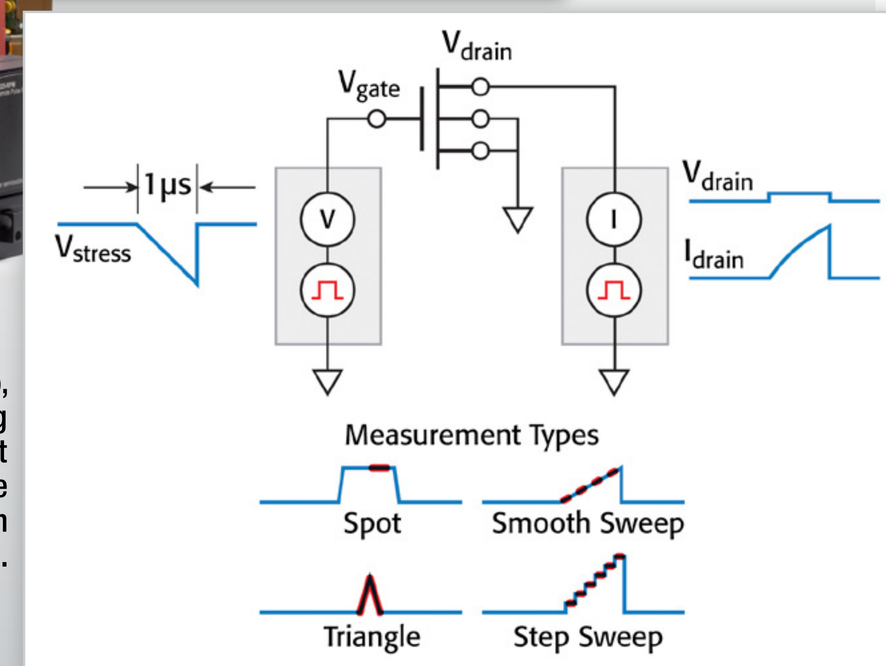
A typical stress/measure waveform that can be used to characterize BTI.

Get advice for your application.

Send us your question or **join the discussion on our application forum.**

Discover everything you need for NBTI and PBTI measurements in the Model 4200-BTI-A Ultra-Fast BTI Package.

The **Model 4200-BTI-A Ultra-Fast BTI Package** is the industry's most advanced NBTI/PBTI test platform, with everything needed to make sophisticated NBTI and PBTI measurements on leading-edge silicon CMOS technology: a Model 4225-PMU Ultra-Fast I-V Module, two Model 4225-RPM Remote Amplifier/Switches, Automated Characterization Suite (ACS) software, an Ultra-Fast BTI Test Project Module, and cabling. The test software module makes it easy to define stress timing, stress conditions, and a wide range of measurement sequences from spot I_D, On-The-Fly (OTF), or I_D-V_G sweeps. It allows measuring recovery effects as well as degradation and offers prestress and poststress measurement options that incorporate the Model 4200-SCS's DC SMUs for precision low-level measurements.



The Ultra-Fast BTI test software module supports spot, step sweep, smooth sweep, and sample measurement types. Each type's timing is defined by the test sample rate and the individual measurement settings. The software module also provides control over the voltage conditions between each element in the test sequence, for maximum flexibility and ease of use, even when defining complex test sequences.

Want to learn more about the Model 4200-BTI-A Package?

Discover ultra-fast I-V sourcing and measurement techniques being used for NBTI/PBTI measurements by downloading our Ultra-Fast I-V applications e-book.

Want assistance, a quote, or to place an order?

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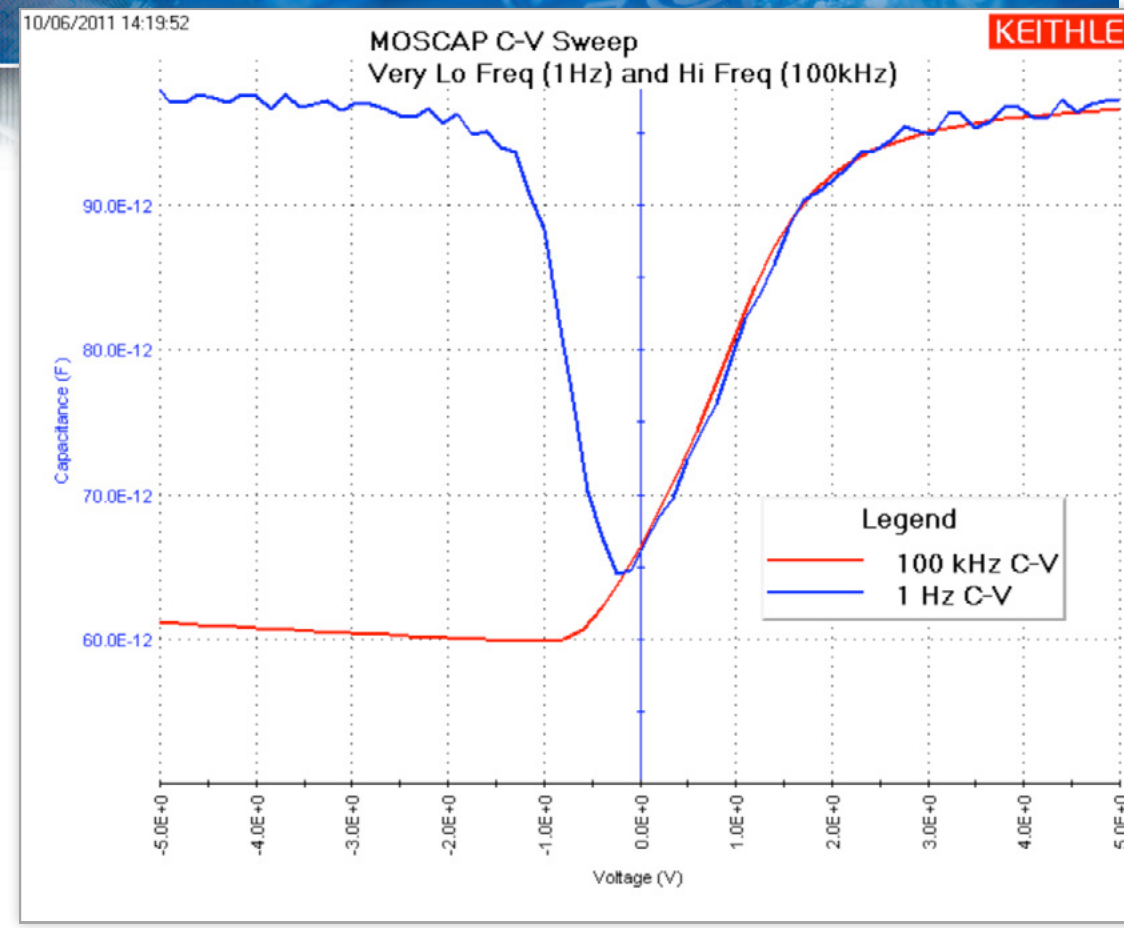
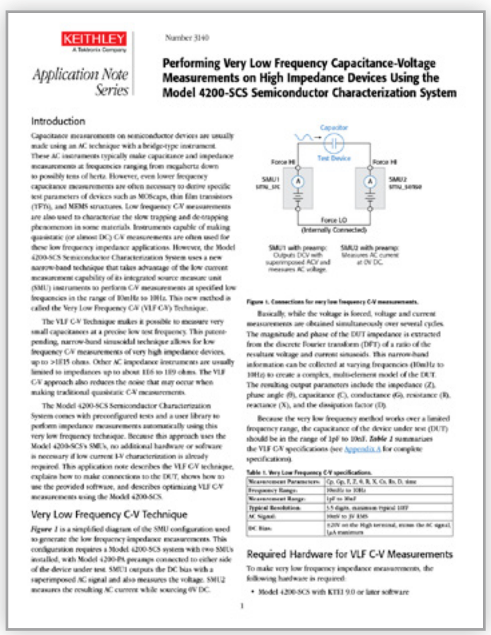
Characterize devices with very low frequency C-V measurements.



This graph is from the CVU_moscap_Vsweep test, showing the high frequency data from the Model 4210-CVU module with the VLF C-V data from the VLF_moscap_Vsweep test.

Capacitance measurements on semiconductor devices are usually made using an AC technique with a bridge-type instrument. These AC instruments typically make capacitance and impedance measurements at frequencies ranging from megahertz down to possibly tens of hertz. However, even lower frequency capacitance measurements are often necessary to derive specific test parameters of devices such as MOScaps, thin film transistors (TFTs), and MEMS structures. Low frequency C-V measurements are also used to characterize the slow trapping and de-trapping phenomenon in some materials. Instruments capable of making quasistatic (or almost DC) C-V measurements are often used for these low frequency impedance applications. However, the Model 4200-SCS Semiconductor Characterization System uses a new narrow-band technique that takes advantage of the low current measurement capability of its integrated source measure unit (SMU) instruments to perform C-V measurements at specified low frequencies in the range of 10mHz to 10Hz. This new method is called the Very Low Frequency C-V (VLF C-V) Technique. **Learn more.**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Application Note Series
Performing Very Low Frequency Capacitance-Voltage Measurements on High Impedance Devices Using the Model 4200-SCS Semiconductor Characterization System
Introduction
Very Low Frequency C-V Technique
Required Hardware for VLF C-V Measurements

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Download our free online application note.

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View our webinar,

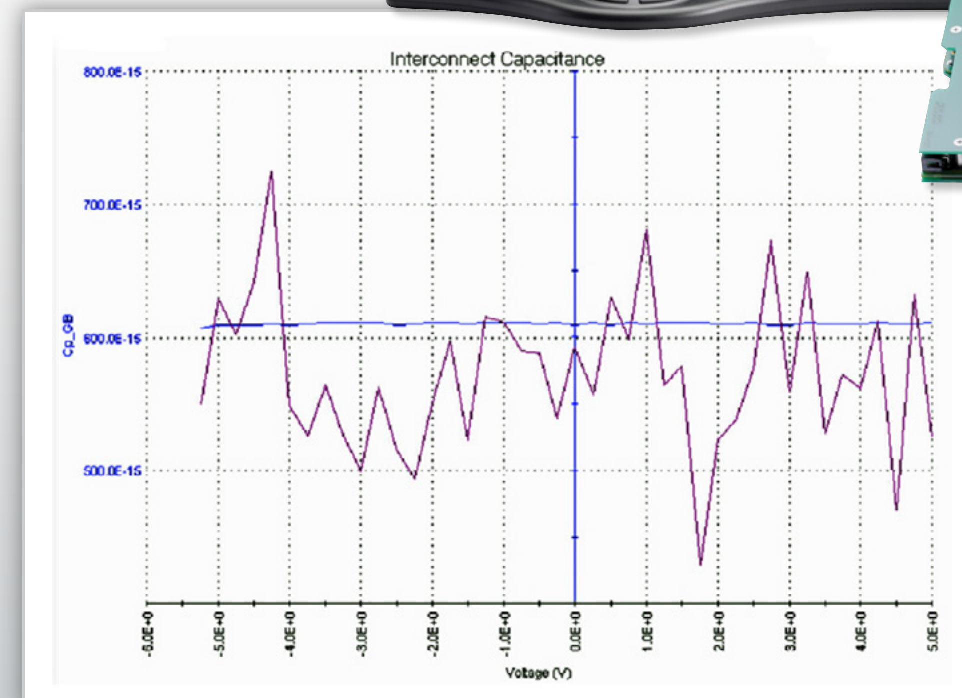
4 Things You Might Not Know About Making C-V Measurements

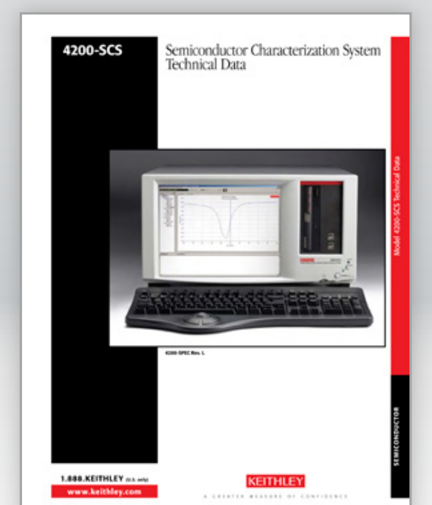
Make multi-frequency C-V measurements as easily as I-V with the Model 4210-CVU C-V module.

The **Model 4210-CVU** plugs directly into one of the nine slots in the Model 4200-SCS chassis. It simplifies measuring capacitances from femtofarads (fF) to nanofarads (nF) at frequencies from 1kHz to 10MHz. The system's user-friendly GUI makes it simple to configure linear or custom C-V, C-f, and C-t sweeps with up to 4096 data points. A special project optimized for I-V, C-V, and resistivity testing is provided for characterizing photovoltaic cells of all types, including crystalline, amorphous, and thin film.

The easy-to-use GUI has built-in features, including:

- Confidence check to ensure the validity of your C-V results
- Easily switch AC ammeter to minimize noise levels without changing cables
- Move the DC bias source to precisely control the electric field on the device under test
- Cable compensation
- Real-time C-V measurements to assist in troubleshooting





Need more detail?

Download the Model 4200-SCS Technical Data Book.

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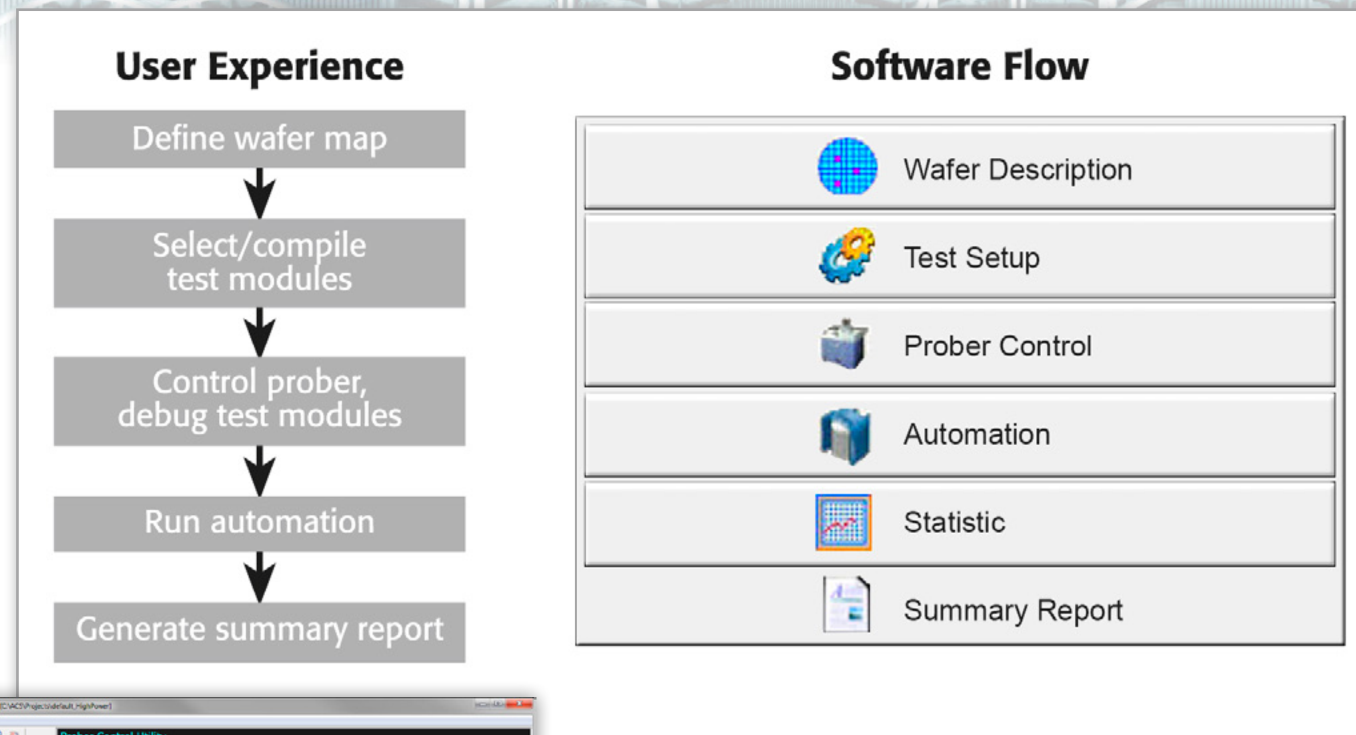
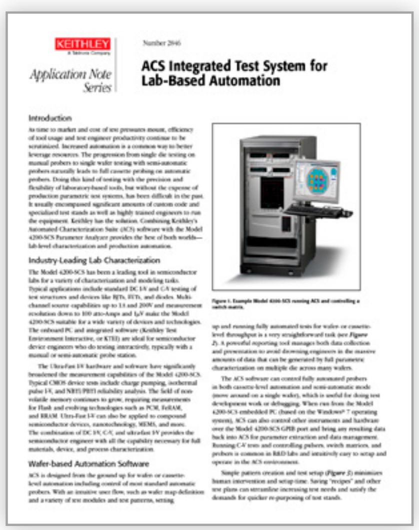
Bring wafer level automation to your lab measurements.

Time-to-market and competitive pressure in the semiconductor industry is very high. And, as engineers move device designs and process changes toward process integration, higher volume lab measurements must be performed to ensure statistical significance. Keithley's Automated Characterization Suite (ACS) provides lab-based automation, enabling wafer or cassette level test plan development and fully-automated prober control to drive lab productivity to new levels. Use the same instrumentation with manual probers and individual device measurements as used with fully automated measurement, assuring consistent measurement results and better use of precious capital. **Learn more.**

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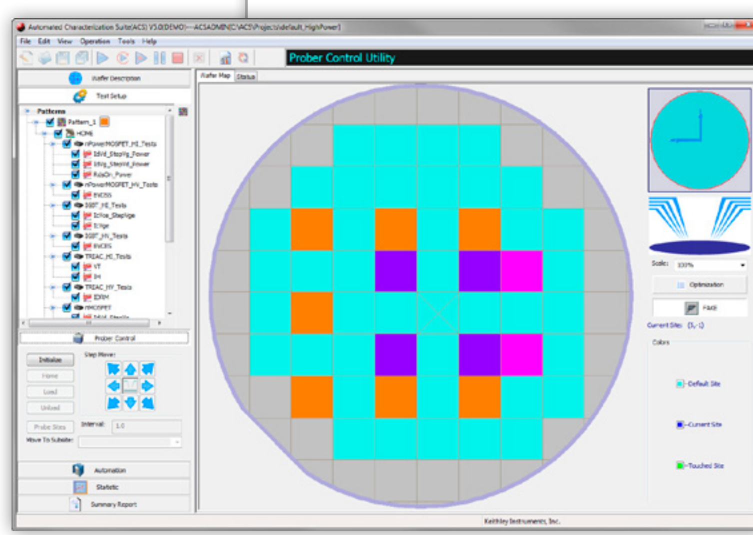
Application Note Series

ACS Integrated Test System for Lab-Based Automation



The Automated Characterization Suite (ACS) Software that controls Keithley S500 Integrated Test systems is designed from the ground up for cassette-level automation, including control of most standard automatic probers. With an intuitive user flow, such as wafer map definition and a variety of test modules and test patterns, setting up and running fully automated tests for cassette-level throughput is a very straightforward task.

Want to learn more?

Download our free online application note: ACS Integrated Test System for Lab-Based Automation

Get advice for your application.

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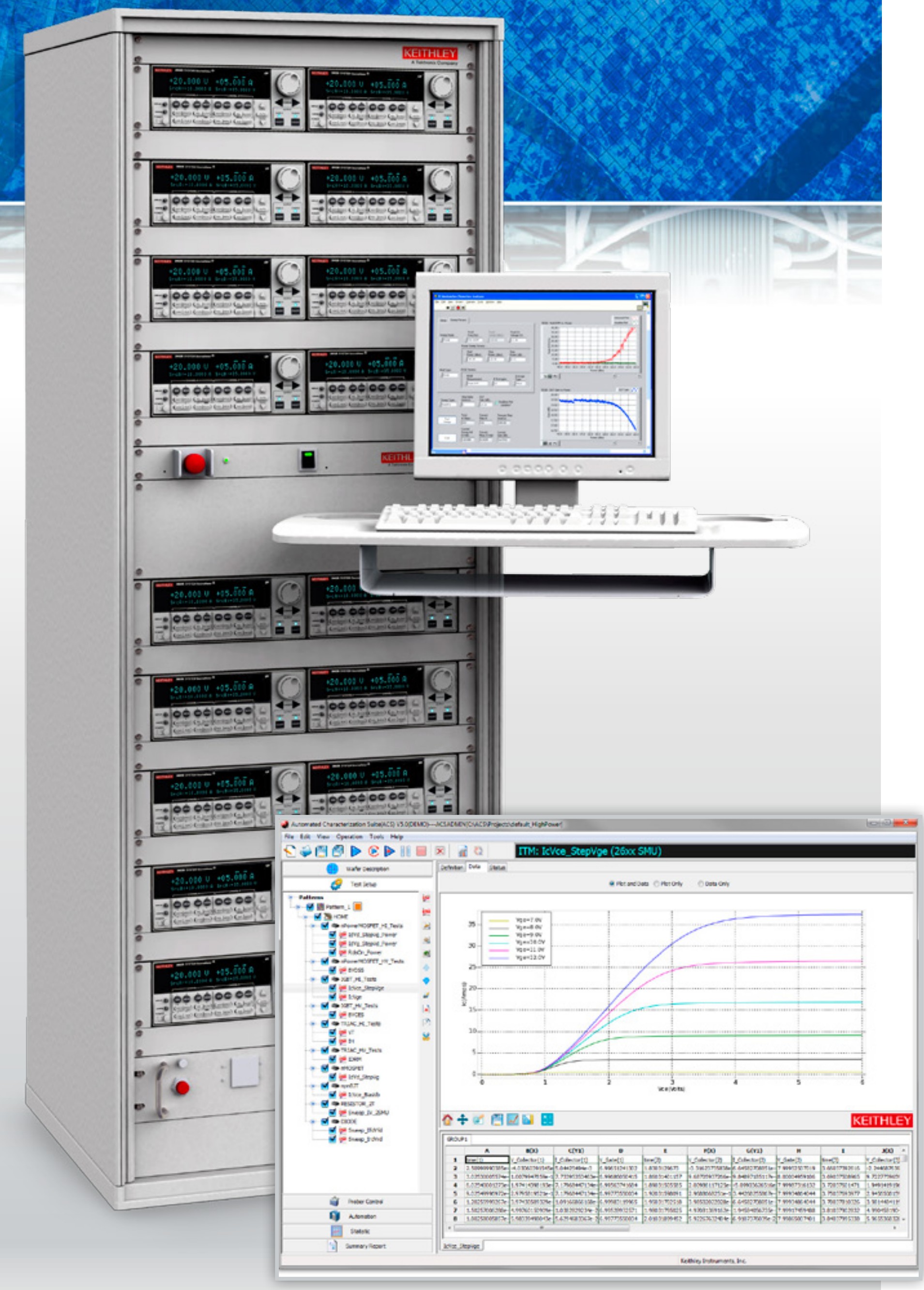
Turnkey systems for lab automation, wafer level reliability, and more.



S500 Integrated Test systems are highly configurable, instrument-based systems for semiconductor characterization at the device, wafer, or cassette level. Built on proven Keithley instrumentation, S500 Integrated Test systems provide innovative measurement features and system flexibility, scalable to your needs. Unique measurement capability, combined with powerful and flexible Automated Characterization Suite (ACS) Software, provides a comprehensive range of applications and features not offered on other comparable systems on the market. Specific capabilities and system configurations include:

- Full-range source measure unit (SMU) instrument specifications, including sub-femtoamp measurement, ensure a wide range of measurements on almost any device.
- Pulse generation and ultra-fast I-V for memory characterization, charge pumping, single-pulse PIV (charge trap analysis), and PIV sweeps (self-heating avoidance.)
- Low or high channel-count systems, including parallel test, with Keithley's system-enabling and scalable SMU instruments.
- High voltage, current, and power source-measure instrumentation for testing devices such as power MOSFETs and display drivers.
- Switching, probe cards, and cabling take the system all the way to your DUT.

Learn more.

Experience full turnkey solutions with Keithley's S500 Integrated Test systems. These highly configurable systems can incorporate a wide range of measurement capability for technology development test stations. Or, use the automation of ACS with S500 systems for high throughput, multi-device testing with automated wafer probers.

Need more detail?

Download the S500 data sheet.

Want assistance, a quote, or to place an order?

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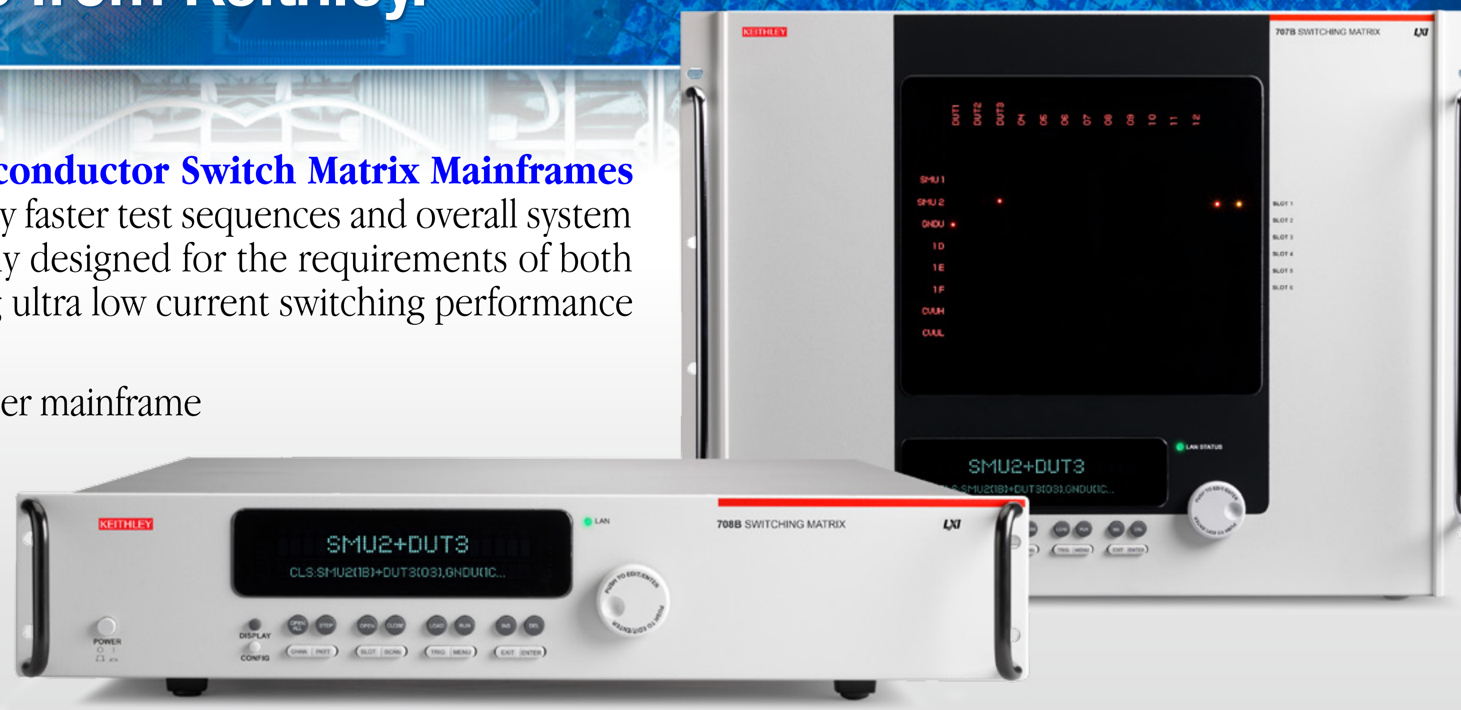
Tie it all together with your choice of high speed, high integrity switching solutions from Keithley.



The **six-slot Model 707B** and **single-slot Model 708B Semiconductor Switch Matrix Mainframes** slash the time from command to connection, offering significantly faster test sequences and overall system throughput than earlier mainframe designs. They are specifically designed for the requirements of both semiconductor lab and production test environments, delivering ultra low current switching performance using standard triax connectors and cables.

- Low-leakage matrix configurations with up to 576 crosspoints per mainframe
- Switch I-V and C-V instruments while maintaining maximum low-level performance
- Source and measure up to 1300V or 1A without reconfiguring cables between tests
- Compatible with all semiconductor parametric analyzers
- Compatible with the popular plug-in cards designed for the 707A/708A mainframes
- Support for both remote (via LXI, USB, and GPIB interfaces) and manual (via front panel) programming
- Embedded TSP® processor and TSP-Link® interface simplify integrating Series 2600B System SourceMeter instruments into a high speed, self-contained tester

Get advice for your application.

Send us your question or **join the discussion on our application forum.**

Model 707B/708B Switching Card Selector Guide

	No. of Channels	Card Config.	Contact Config.	Max. Voltage	Max. Current	Max. Power	Contact Potential	Offset Current	Max. Recomm. Freq.	Connection Type	CE	Comments
LOW CURRENT												
7072	8×12	Matrix	2 form A	200 V	1 A	10 VA	< 20 µV	<1 pA	15 MHz	3-lug triax	Yes	Optimized for semiconductor applications.
7072-HV	8×12	Matrix	2 form A	1300 V	1 A	10 VA	< 20 µV	<1 pA	4 MHz	3-lug triax		Optimized for semiconductor applications.
7174A	8×12	Matrix	2 form A	200 V	2 A			<100 fA	30 MHz	3-lug triax	Yes	Optimized for semiconductor applications.
HIGH FREQUENCY												
7173-50	4×12	Matrix	2 form C	30 V	0.5 A	10 VA	< 15 µV	<200 pA	200 MHz	BNC	Yes	

Need more details about the Model 707B or 708B Switch Matrix Mainframe? Download the data sheet.

Get switching and measurement in one economical enclosure.

Keithley's **Model 3706A System Switch/Multimeter** is a scalable, instrument-grade switching and multi-channel measurement solutions that's optimized for automated testing of electronic products and components. The Model 3706A provides six slots for plug-in cards in a compact 2U high (3.5 inches/89mm) enclosure that easily accommodates the needs of medium to high channel count applications. When fully loaded, a mainframe can support up to 576 two-wire multiplexer channels for unrivaled density and economical per channel costs. The high performance multimeter provides a tightly integrated switch and measurement system that meets the demanding application requirements in a functional test system or provides the flexibility needed in stand-alone data acquisition and measurement applications. Embedded test script processor (TSP®) processor and TSP-Link® interface simplify building larger systems by making it easy to integrate the Model 3706A with Series 2600B System SourceMeter® instruments.

Series 3700A Plug-In Card Selector Guide

	No. of Channels	Card Configuration	Type of Relay	Contact Configuration	Maximum Voltage	Maximum Current Switched
3720	60 (Dual 1×30)	Multiplexer	Latching electromechanical	2 Form A	300 V	1 A
3721	40 (dual 1×20)	Multiplexer	Latching electromechanical	2 Form A	300 V (ch 1–40), 60 V (ch 41–42)	2 A (ch 1–40), 3 A (ch 41–42)
3722	96 (dual 1×48)	Multiplexer	Latching electromechanical	2 Form A	300 V	1 A
3723	60 (dual 1×30) or 120 single pole (dual 1×60)	Multiplexer	Dry reed	1 Form A	200 V	1 A
3724	60 (dual 1×30)	Multiplexer	FET solid-state	2 Form A	200 V	0.1 A
3730	6×16	Matrix	Latching electromechanical	2 Form A	300 V	1 A
3731	6×16	Matrix	Dry reed	2 Form A	200 V	1 A
3732	448 crosspoints (Quad 4×28)	Matrix	Dry reed	1 Form A	200 V	0.75 A
3740	32	Independent	Latching electromechanical	28 Form C, 4 Form A	300 VDC/250 VAC (Form A)	2 A (Form C), 7 A (Form A)
3750	40 digital I/O, 4 counter/ totalizers, and 2 isolated analog outputs	Independent	N/A	N/A	N/A	N/A

Need more detail?
Download the Series 3700A data sheet.

Get advice for your application.
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Printed in the U.S.A. No. 3103 10.13