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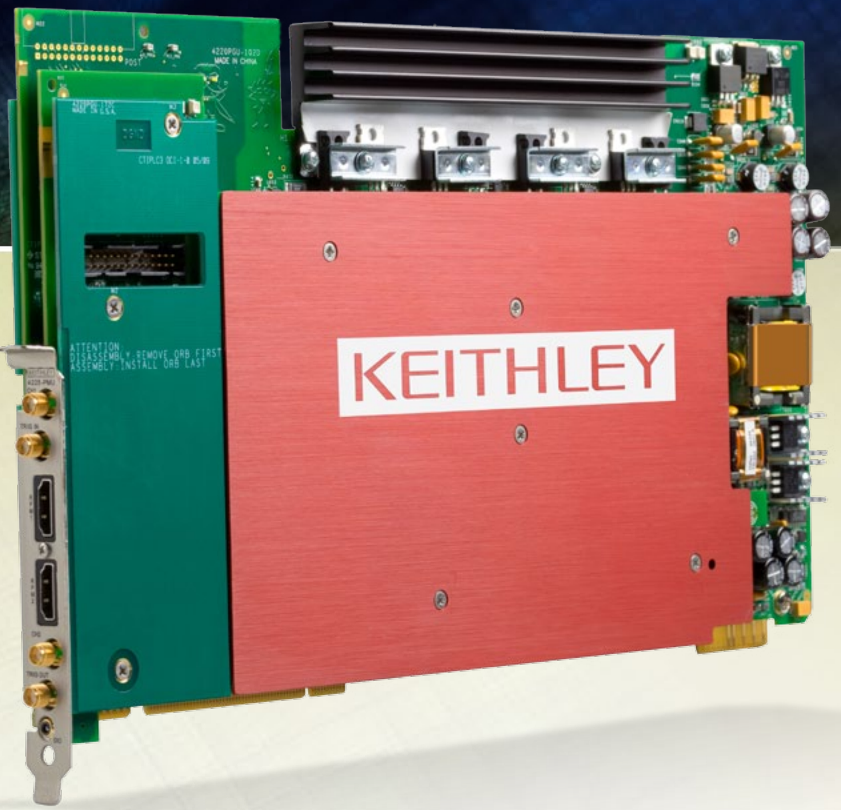
# Ultra-Fast I-V Applications

## *for the Model 4225-PMU Ultra-Fast I-V Module*

# Ultra-Fast I-V Applications

## *for the Model 4225-PMU Ultra-Fast I-V Module*



### INTRODUCTION

Ultra-fast I-V sourcing and measurement have become increasingly important capabilities for many technologies, including compound semiconductors, medium power devices, non-volatile memory, MEMs (micro-electro-mechanical devices), nanodevices, solar cells, and CMOS devices. Using pulsed I-V signals to characterize devices rather than DC signals makes it possible to study or reduce the effects of self-heating (joule heating) or to minimize current drift or degradation in measurements due to trapped charge. Transient I-V measurements allow scientists and engineers to capture ultra high speed current or voltage waveforms in the time domain or to study dynamic test circuits. Pulsed sourcing can be used to stress test a device using an AC signal during reliability cycling or in a multi-level waveform mode to program/erase memory devices. The Model 4225-PMU Ultra-Fast I-V Module for the Model 4200-SCS Semiconductor Characterization System supports many of these high speed source/measure applications.

### Key Features and Specifications

Each Model 4225-PMU Ultra-Fast I-V Module can provide two channels of high speed, multi-level voltage pulse output while simultaneously measuring current and voltage. It replaces traditional pulse/measure hardware configurations, which typically included an external pulse generator, a multi-channel oscilloscope, specially designed interconnect hardware, and integrated software.

The Model 4225-PMU has a number of key features:

- Integrated high speed sourcing and measurement capabilities, which allow for ultra-fast I-V testing
- Wide dynamic range of voltage sourcing, current measurement (with auto-ranging), and timing parameters
- Broad array of applications
- Built-in interactive software for easy control

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## INTEGRATED HIGH SPEED SOURCING AND MEASUREMENT

Each module has two independent channels. Each channel can measure both voltage and current simultaneously with parallel 14-bit A/D converters with deep memory allowing up to one million samples at 5ns per sample.

These high speed measurement and storage capabilities support a wide range of high speed applications, such as characterizing isothermal pulsed I-V and transient effects of trapped charges on a device. Each channel can output high accuracy voltage pulses as short as 60ns with a rise time as short as 20ns. When the instrument's Segment ARB® mode is used for multi-level pulsing, individual voltage segments can be as short as 20ns and waveforms can have up to 2048 unique segments per channel, which provides the flexibility necessary to build waveforms for characterizing flash devices and other non-volatile memory technologies.

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## WIDE PARAMETER RANGES

The Model 4225-PMU provides broad ranges of voltage sourcing, current measurement, and timing parameters:

- **Voltage source range:** Pulse amplitudes as large as ±40V can be programmed with millivolt resolution. This wide range provides both low voltages for characterizing emerging silicon technologies and higher voltages for multi-bit flash, LDMOS, and lower power compound semiconductor devices made of materials such as gallium nitride (GaN) and gallium arsenide (GaAs).
- **Current measurement ranges:** The Model 4225-PMU has current measurement ranges from ±100μA to 800mA (full scale) with <12nA current measurement resolution (without averaging) with a noise floor of about 10nA. The Model 4225-RPM Remote Preamplifier/Switch Module option provides six measurement ranges from ±100nA to 10mA (full scale) with current measurement resolution of <200pA (without averaging) and a noise floor of about 10pA. (See **Figure 1** for an illustration of the offset current vs. time.) The higher current capability allows testing relatively high powered devices, while the lower ranges support more challenging applications, such as bias temperature instability (BTI) characterization of leading-edge scaled CMOS devices. **Figure 2** compares the Model 4225-PMU's current measurement capability with that of other Keithley DC and pulsed I-V measurement instruments.
- **Timing parameters:** The Model 4225-PMU provides two-level pulse widths from 60ns to 999ms. Multi-level waveforms can be programmed with segments as short as 20ns and as long as 40s. Pulse periods ranging from 120ns to 1s can also be programmed. Multiple segments can be looped up to $10^{12}$ times for demanding reliability applications, such as BTI and non-volatile memory endurance tests, which typically require extensive stress/measure looping.

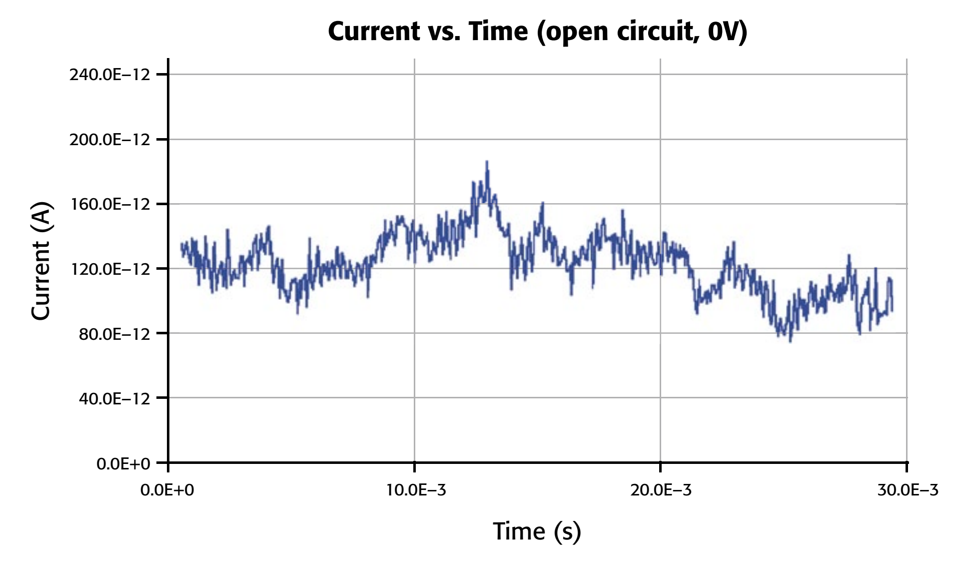

Figure 1. Offset current for the 1μA range at 0V

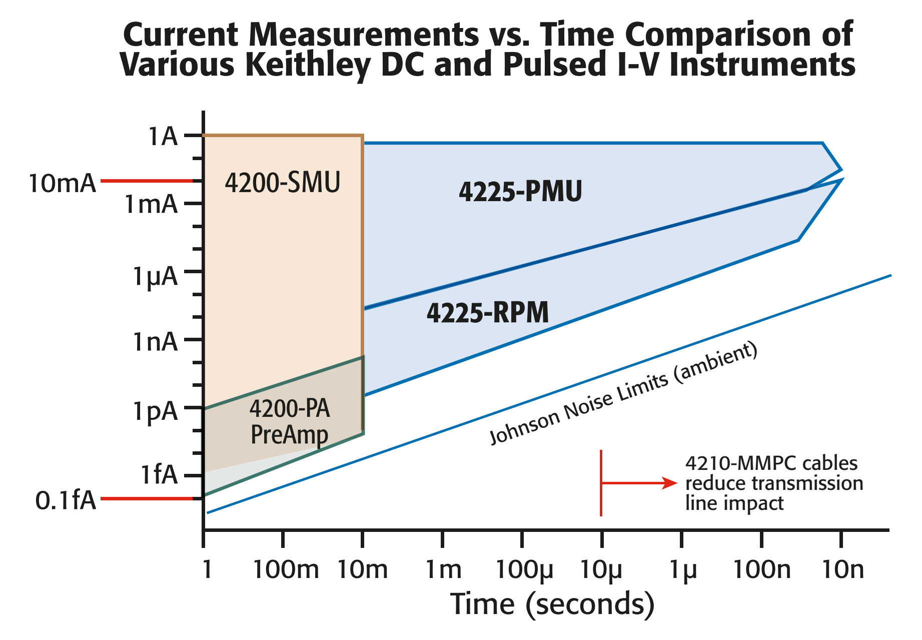

Figure 2. Current measurement window as a function of time for DC and pulsed I-V instruments

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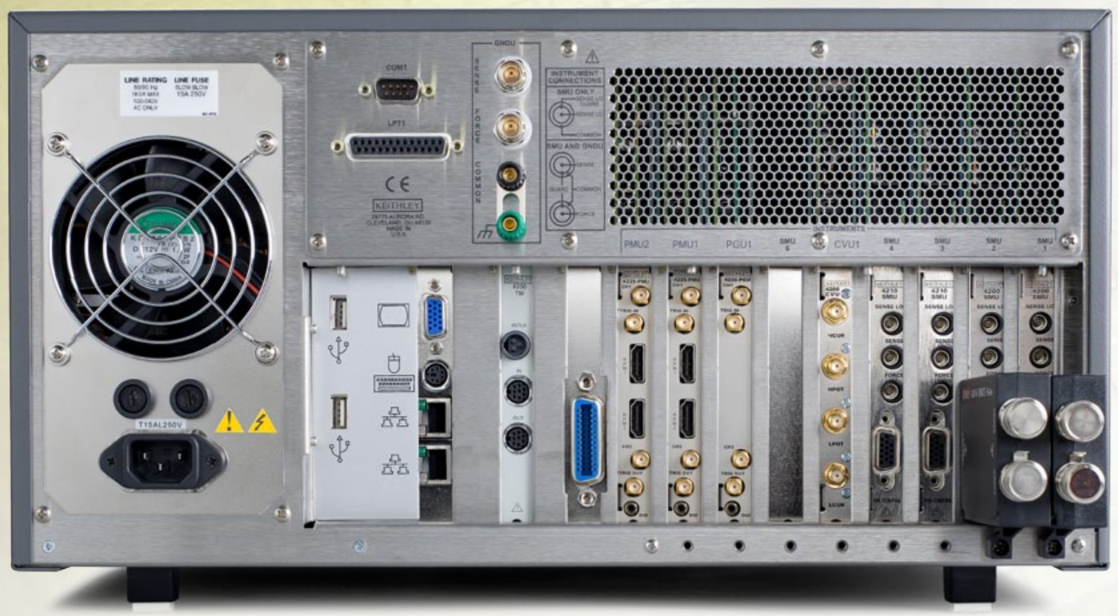
### BROAD RANGE OF APPLICATIONS

The Model 4225-PMU is useful for a wide range of high speed applications, including basic pulsed I-V measurements on devices, testing non-volatile memory such as flash and PCRAM devices, CMOS device characterization (including charge pumping and self-heating effects), reliability testing, nanodevice measurements, solar cell testing, and organic TFT display measurements. The section titled ***"Example Applications of Ultra-Fast I-V"*** provides an overview of some of the typical applications for the Model 4225-PMU.

- **General Pulsed I-V Testing of Devices**
- **CMOS Device Characterization**
  - Charge Pumping
  - Self-Heating Effects
  - Charge trapping
  - NBTI and PBTI Characterization, Modeling, and Monitoring
- **Non-Volatile Memory Device Testing**
  - Flash Memory
  - Phase Change Random Access Memory (PRAM or PCRAM)
  - Ferro-electric Memory (FeRAM)
- **Compound Semiconductor Devices and Materials**
  - Laser Diode
  - Thermal Impedance Measurements
- **Nanotechnology and MEMs Devices**
- **Solar Cells**
- **Other Tests**

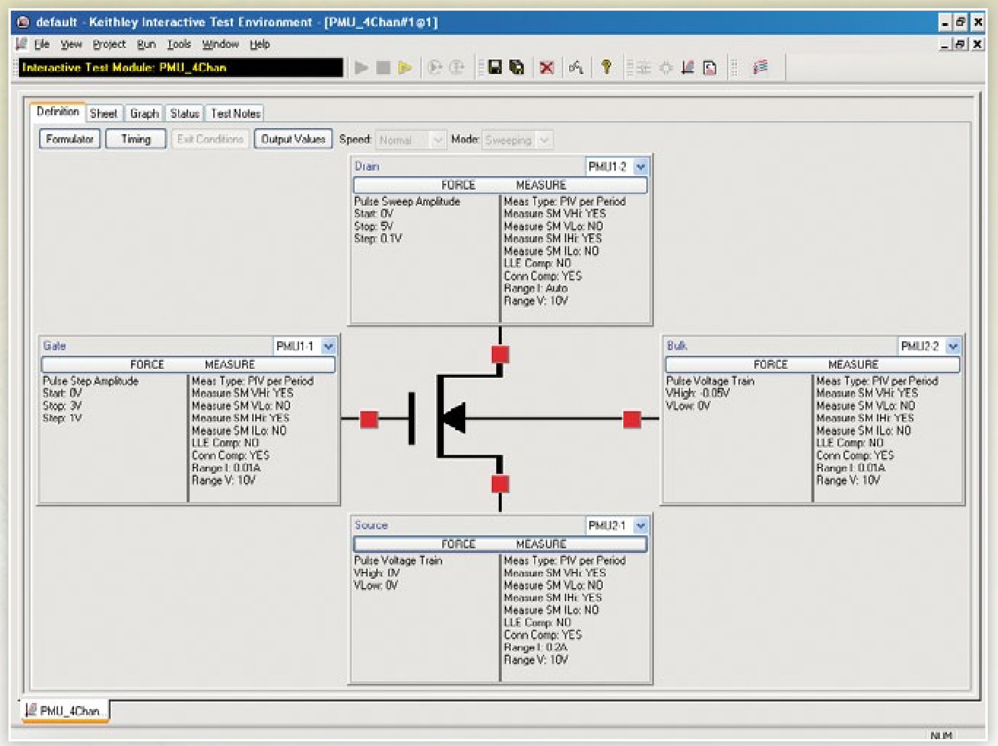


# Ultra-Fast I-V Applications
## *for the Model 4225-PMU Ultra-Fast I-V Module*

## BUILT-IN INTERACTIVE SOFTWARE

The Model 4200-SCS's interactive software, **KTEI (Keithley Test Environment Interactive)**, provides intuitive, point-and-click control of the system's instrumentation, as well as a growing array of graphics and analysis tools. This test software, which has been used successfully for many years in DC and C-V characterization, has been leveraged to provide the same look and feel for the system's ultra-fast I-V capability. Users can easily create their own tests or use one of the many test projects included, which address some of the most common high speed I-V test applications, including charge pumping, charge trapping, and non-volatile memory testing.

For additional applications, **Automated Characterization Suite (ACS)** software is available as an option for the Model 4200-SCS. ACS Version 4.4 includes ultra-fast I-V libraries that support development of user test modules, as well as support for wafer- and cassette-level automation, wafer mapping, or large data sets. In conjunction with the test libraries provided with the Model 4200-SCS, ACS 4.4 can be used to develop test projects that employ both the Model 4225-PMU and Model 4225-RPM Remote Amplifier/Switch. The ultra-fast BTI test project provides a powerful but easy-to-use interface that simplifies performing advanced ultra-fast bias temperature instability tests.



Speed: Normal
Mode: Sweeping

Drain — PMU1-2
FORCE: Pulse Sweep Amplitude
Start: 0V
Stop: 5V
Step: 0.1V
MEASURE: Meas Type: PIV per Period
Measure SM VHi: YES
Measure SM VLo: NO
Measure SM IHi: YES
Measure SM ILo: NO
LLE Comp: NO
Conn Comp: YES
Range I: Auto
Range V: 10V

Gate — PMU1-1
FORCE: Pulse Step Amplitude
Start: 0V
Stop: 3V
Step: 1V
MEASURE: Meas Type: PIV per Period
Measure SM VHi: YES
Measure SM VLo: NO
Measure SM IHi: YES
Measure SM ILo: NO
LLE Comp: NO
Conn Comp: YES
Range I: 0.01A
Range V: 10V

Bulk — PMU2-2
FORCE: Pulse Voltage Train
VHigh: -0.05V
VLow: 0V
MEASURE: Meas Type: PIV per Period
Measure SM VHi: YES
Measure SM VLo: NO
Measure SM IHi: YES
Measure SM ILo: NO
LLE Comp: NO
Conn Comp: YES
Range I: 0.01A
Range V: 10V

Source — PMU2-1
FORCE: Pulse Voltage Train
VHigh: 0V
VLow: 0V
MEASURE: Meas Type: PIV per Period
Measure SM VHi: YES
Measure SM VLo: NO
Measure SM IHi: YES
Measure SM ILo: NO
LLE Comp: NO
Conn Comp: YES
Range I: 0.2A
Range V: 10V

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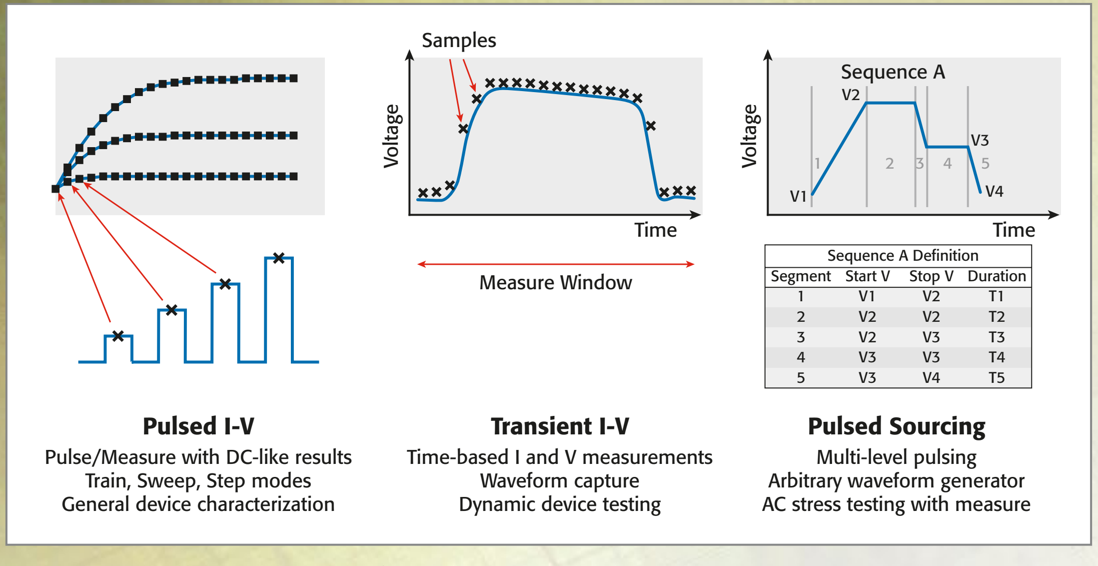


| Sequence A Definition | | | |
|---|---|---|---|
| Segment | Start V | Stop V | Duration |
| 1 | V1 | V2 | T1 |
| 2 | V2 | V2 | T2 |
| 3 | V2 | V3 | T3 |
| 4 | V3 | V3 | T4 |
| 5 | V3 | V4 | T5 |

**Pulsed I-V**
Pulse/Measure with DC-like results
Train, Sweep, Step modes
General device characterization

**Transient I-V**
Time-based I and V measurements
Waveform capture
Dynamic device testing

**Pulsed Sourcing**
Multi-level pulsing
Arbitrary waveform generator
AC stress testing with measure

Figure 3. The three modes of the Model 4225-PMU Ultra-Fast I-V Module

The Model 4225-PMU can be used to perform three types of ultra-fast I-V tests: pulsed I-V, transient I-V, and pulsed sourcing. These three modes are illustrated in **Figure 3.**

**"Pulsed I-V"** refers to any test with a pulsed source and a corresponding high speed, timed-based measurement that provides DC-like results. The current and/or voltage measurement is an average of readings taken in a predefined measurement window on the pulse. This average of readings is called the "spot mean." The user defines the parameters of the pulse, including the pulse width, duty cycle, rise/fall times, amplitude, etc.

**"Transient I-V"** or waveform capture is a time-based current and/or voltage measurement that is typically the capture of a pulsed waveform. A transient test is typically a single pulse waveform that is used to study time-varying parameters, such as the drain current degradation versus time due to charge trapping or self-heating. Transient I-V measurements can be made to test a dynamic test circuit or can be used as a diagnostic tool for choosing the appropriate pulse settings in the pulsed I-V mode.

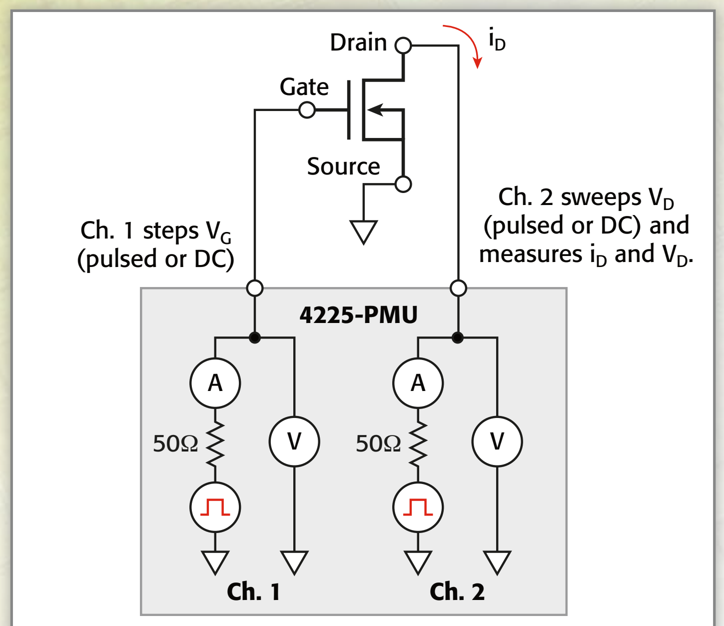
**"Pulsed sourcing"** can involve outputting user-defined two-level pulses, outputting multi-level pulses using the built-in Segment ARB function, or outputting an arbitrarily defined waveform using the arbitrary waveform generator in the KPULSE software included with the Model 4200-SCS. The Segment ARB® feature allows users to create waveforms from segments defined with separate voltages and time durations. In addition to its pulse generator capabilities, the Model 4225-PMU can measure AC or DC voltage and current, thereby reducing the need for additional measurement hardware and more complicated programming. The Model 4220-PGU is a two-channel pulse generator with output capabilities identical to the Model 4225-PMU's but without its measurement functions.

# Example Applications of Ultra-Fast I-V

Because of its wide range of measurement capability and the interactive software built into the Model 4200-SCS, the **Model 4225-PMU** covers a broad range of applications, including general pulsed I-V measurements on devices, compound semiconductor testing, CMOS device characterization, non-volatile memory device (flash, PCRAM, etc.) verification, nanotechnology and MEMs measurements, AC stress and reliability testing, organic TFT displays, and solar cell testing.

## GENERAL PULSED I-V TESTING OF DEVICES

Pulsed I-V testing can be performed on a variety of devices for many different purposes, including preventing device self-heating by using narrow pulses and/or low duty cycle pulses rather than DC signals. Another common reason to use pulsed I-V signals is to minimize the effects of trapped charges on device performance during characterization. The Model 4225-PMU module can be used to make pulsed I-V measurements on many devices, including transistors, diodes, resistors, capacitors, etc. Each module has two channels, so only one module is needed to test a three-terminal device if one of the terminals can be connected to common. **Figure 4** shows the two-channel Model 4225-PMU connected to a MOSFET. In this example, Channel 1 is connected to the gate of the MOSFET and Channel 2 is connected to the drain. Channel 1 steps a pulsed or DC voltage on the gate ($V_G$) while Channel 2 sweeps the drain voltage ($V_D$) using either pulsed or DC voltage and measures the resulting drain current ($I_D$). The resulting pulsed $V_{DS}$-$I_D$ family of curves is shown in **Figure 5**.



Note: Unlike earlier systems, the 4225-PMU can simultaneously measure both current and voltage.

Figure 4. Model 4225-PMU connections to a MOSFET

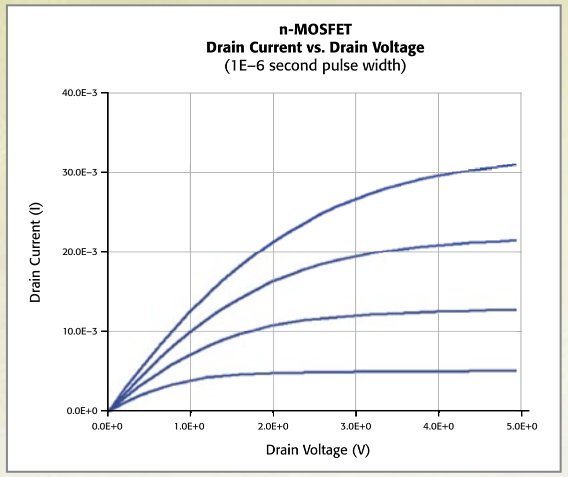


Figure 5. Pulsed I-V family of curves of n-channel MOSFET

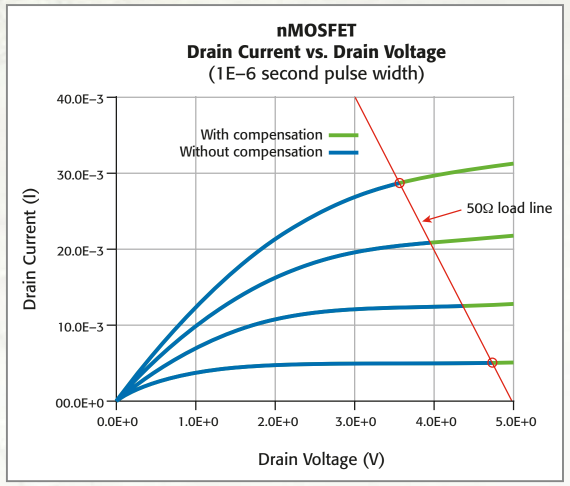


Figure 6. Family of curves generated with and without load line effect compensation

The curves in Figure 5 were generated using the Load Line Effect Compensation (LLEC) feature, which employs a mathematical algorithm that compensates for the voltage drop across the 50Ω output impedance of the pulser, as well as for the voltage drop across the lead resistance and connections to the device under test. Load Line Effect Compensation is especially important for high current or low resistance measurements. **Figure 6** shows the resulting curves with LLEC (green lines) and without LLEC (blue lines). Note the 50Ω load line displayed on the graph.

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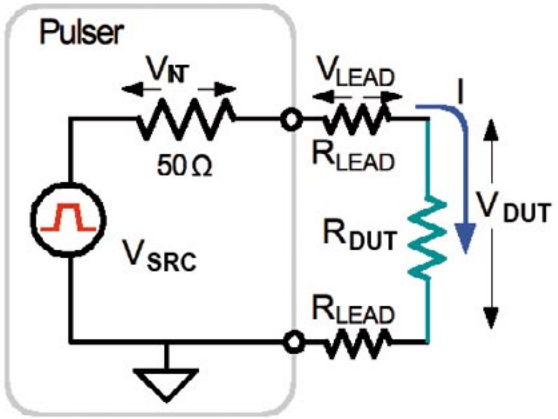
# Example Applications of Ultra-Fast I-V

### What is Load Line Effect Compensation?



Load Line Effect Compensation (LLEC) is an algorithm that compensates for unwanted voltage drops in the test circuit.

Resistances causing unwanted voltage drops:
- 50 Ω output impedance of pulser
- lead/cable resistance
- probes and pin resistance

Without LLEC:
$V_{DUT} = V_{SRC} - V_{50\Omega} - V_{LEAD}$

With LLEC:
$V_{DUT} = V_{SRC}$

Besides using the LLEC feature to make more accurate measurements, the Connection Compensation feature “zeros out” the voltage drops due to cables, adapters, and probe pin-to-pad resistances. The Connection Compensation procedure, just done once during the initial setup, measures the voltage drops across the entire card to device interconnection, enabling the user to optimize measurement performance.

In addition to making measurements on three-terminal devices, the Model 4225-PMU can be used on devices that have two or three terminals (one Model 4225-PMU) or up to eight terminals (four Model 4225-PMUs).

The resistor shown in **Figure 7** is an example of a two-terminal device connected to the PMU. A two-terminal device can be measured using either one or two channels of the PMU. When using only one channel, one end of the device is connected to the output terminal of Channel 1 and the other end of the device is connected to the common terminal of the PMU, which is the outside shell of the coax cable. The pulsed I-V sweep of a 1GΩ resistor is shown in **Figure 8**. Note that the measured high speed current is in the nanoamp range.

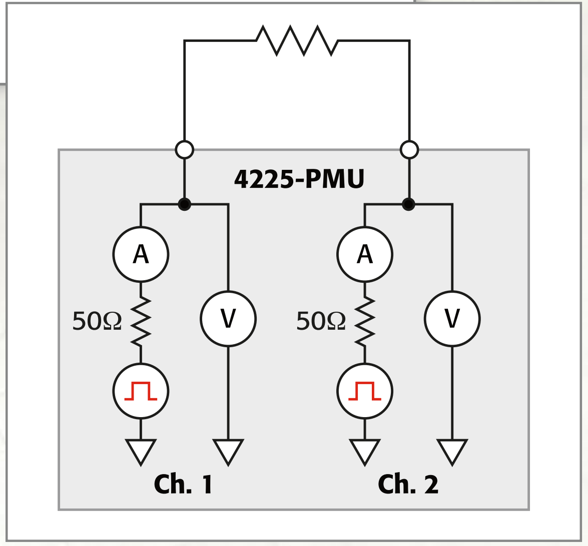


Figure 7. Connecting a resistor to the Model 4225-PMU

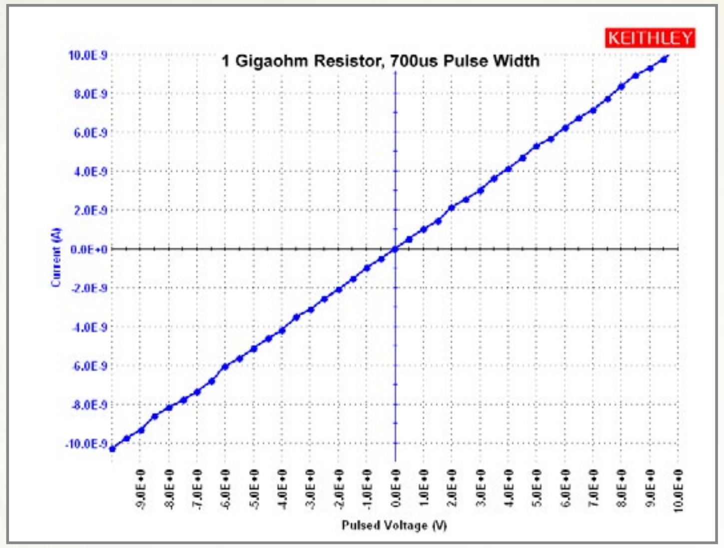


Figure 8. Pulsed I-V curve of 1GΩ resistor

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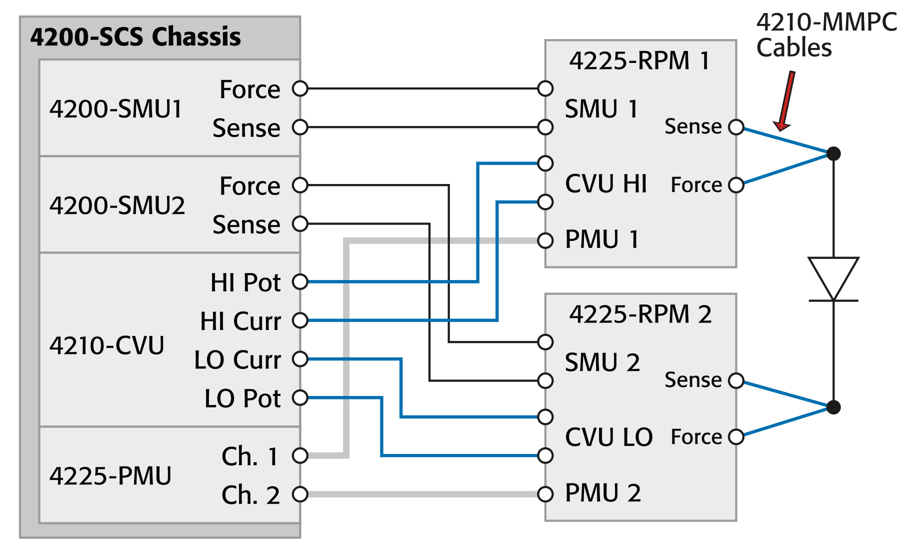
The PMU can be used to make pulsed I-V measurements over a wide range of resistances, from <1Ω to >1GΩ. With the optional Model 4225-RPM Remote Amplifier/Switch, resistances >1GΩ can be measured. The PMU's built-in auto-ranging capability can be very useful for characterizing resistances that may vary as a function of an external stimulus, such as when measuring the output of sensors.

For some devices, multiple types of electrical measurements are required, such as pulsed I-V, DC I-V, and C-V tests. This usually requires an external switch matrix capable of switching the various types of signals to the device under test. However, the optional Model 4225-RPM Remote Preamplifier/Switch allows for switching automatically between DC I-V, C-V, and pulsed I-V measurements. This greatly simplifies the connections to the device. **Figure 9** shows how the Model 4225-RPM reduces the amount of cabling needed to make DC I-V, C-V, and pulsed I-V measurements on a diode. Users can perform all the electrical measurements on the device without having to disconnect and reconnect cabling for each test, which ultimately saves valuable test time and reduces frustration. An optional multi-measurement performance (Model 4210-MMPC) cable kit connects the Model 4200-SCS to a prober manipulator. In addition to eliminating the need for recabling, this kit helps maximize signal fidelity by eliminating the measurement errors that often result from cabling errors.



The 4225-RPM Remote Amplifier/Switch enables automatic switching between DC, C-V, and pulsed I-V signals, simplifying measurements.

Figure 9. Automatically switching between DC I-V, C-V, and pulsed I-V using the Model 4225-RPM Remote Preamplifier/Switch

The Model 4225-RPM also serves as a preamp to extend the lower current ranges on the PMU. This is especially important for devices, like diodes, that have I-V characteristics that extend over several decades of current. The pulsed I-V measurements of the diode through the Model 4225-RPM Remote Amplifier/Switch is shown in **Figure 10**. Its unique auto-range feature enables automatic range selection while the pulsed I-V sweep is in progress. That means the user isn't forced to select a fixed range, which can reduce measurement resolution.

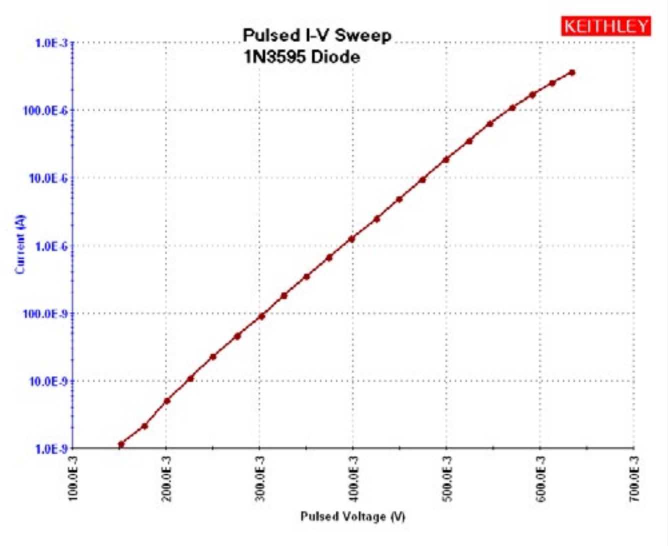


Figure 10. Pulsed I-V characteristics of a diode by the Model 4225-PMU with the 4225-RPM.

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## CMOS DEVICE CHARACTERIZATION

High speed sourcing and measuring are increasingly important for CMOS device characterization, including high κ devices and advanced CMOS technologies like Silicon-on-Insulator (SOI). In addition to the general pulsed I-V and transient I-V measurements discussed previously showing results from a MOSFET, applications that are commonly performed on CMOS devices include charge pumping, charge trapping, self-heating tests, transient I-V tests, and negative bias temperature instability (NBTI) and reliability tests.

### Charge Pumping

Charge pumping (CP) is a well-known measurement technique for analyzing the semiconductor-dielectric interface of MOS structures. Important parameters about the quality and degradation of the device can be extracted from the charge pumping current ($I_{CP}$), including the interface trap density and the mean capture cross section. Pulsing a gate voltage while simultaneously measuring a DC substrate current is the basis of the various charge pumping methods. Therefore, a pulse generator and a very sensitive ammeter are required. The Model 4200-SCS is an ideal choice for these measurements because it can be configured with the Model 4225-PMU or Model 4220-PGU pulser and the Model 4200-SMU with preamp. The system's integrated software (KTEI) provides application tests for many of the common charge pumping methods.

**Figure 11** illustrates a charge pumping measurement circuit based on the Model 4200-SCS. Essentially, the gate of the MOSFET is connected to the pulse generator, which is used to switch the transistor from accumulation to inversion repeatedly. While the gate is pulsed, a recombination process of majority/minority carriers occurs on the pulses' rising and falling edges. This causes a small current to flow in the opposite direction of the normal drain-to-source current. This induced current, which is known as the charge pumping current ($I_{CP}$), is measured with the Model 4200-SMU with preamp connected to the substrate, or bulk terminal, of the MOSFET.

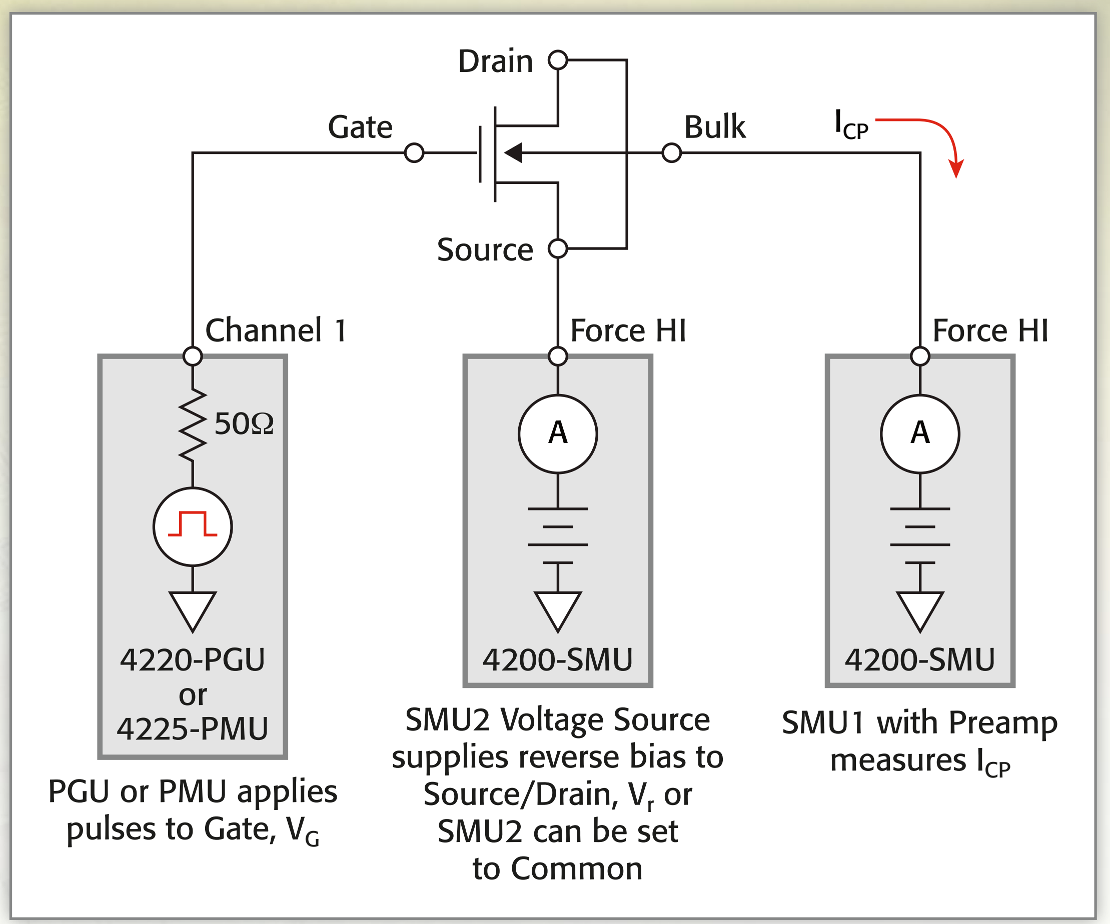

Figure 11. Model 4200-SCS configuration for charge pumping measurements

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## *Charge Pumping*

The Model 4200-SCS is supplied with a project that includes tests for performing many of the common charge pumping methods, including the Fixed Amplitude/Voltage Base Sweep and the Fixed Base/Variable Amplitude Sweep tests. The pulsed waveforms and the corresponding charge pumping curves for these two tests are shown in **Figure 12**. The results of executing the Fixed Amplitude/Voltage Base Sweep test are shown in **Figure 13**. These measurements were made at multiple test frequencies.

Further information on using the Model 4200-SCS for charge pumping measurements can be found in Keithley **Application Note #3066,** ***"Performing Charge Pumping Measurements with the Model 4200-SCS Semiconductor Characterization System."***

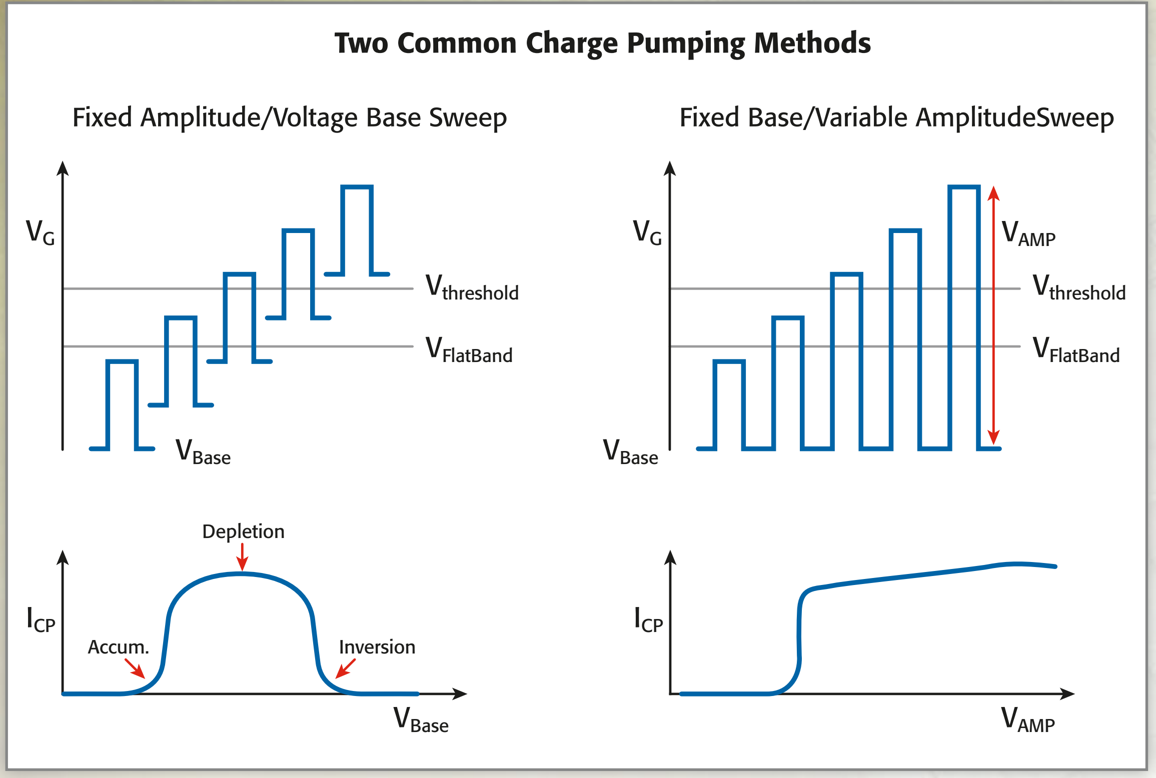


Figure 12. Pulse waveforms for two common charge pumping methods with the corresponding charge pumping curves

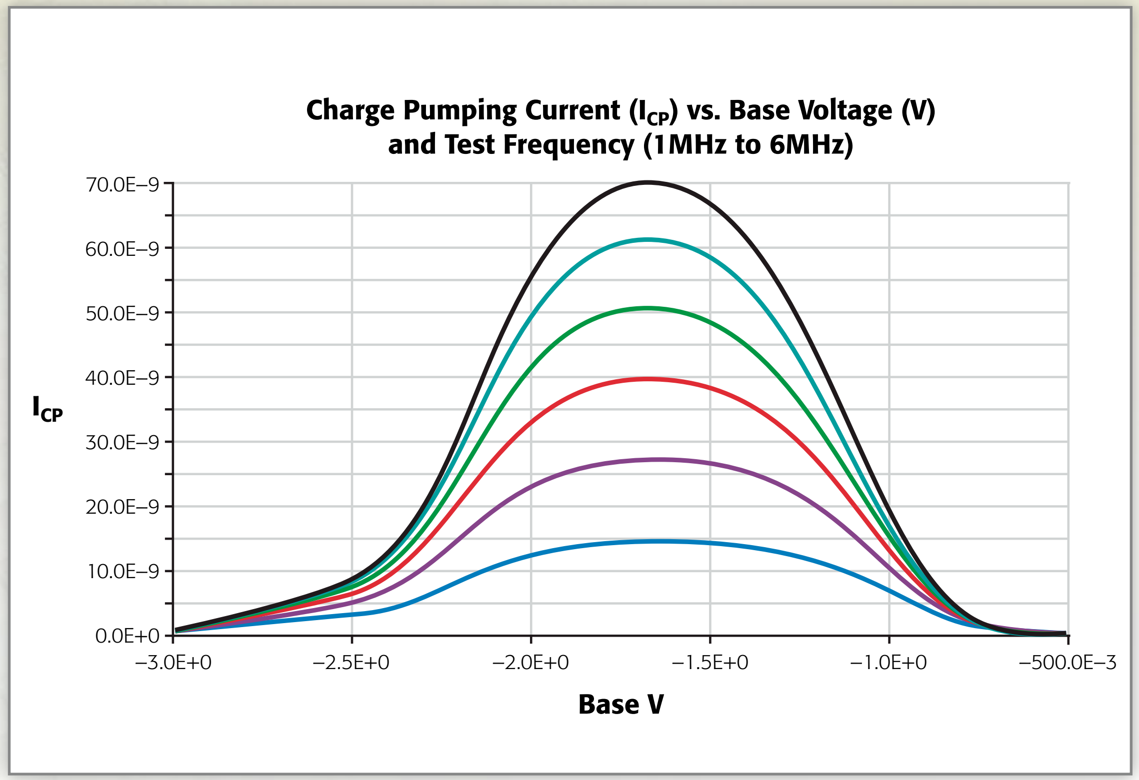


Figure 13. Charge pumping current measurement results at multiple test frequencies

# Example Applications of Ultra-Fast I-V

## Self-Heating Effects

In addition to performing pulsed I-V tests on MOSFETs, transient I-V measurements can be performed to characterize devices from a time domain perspective. An example of a curve taken using the transient I-V, or waveform capture mode is shown in **Figure 14**. In this curve, the drain current is measured as a function of time at a fixed drain and gate voltage. Notice the heating effects on the drain current.

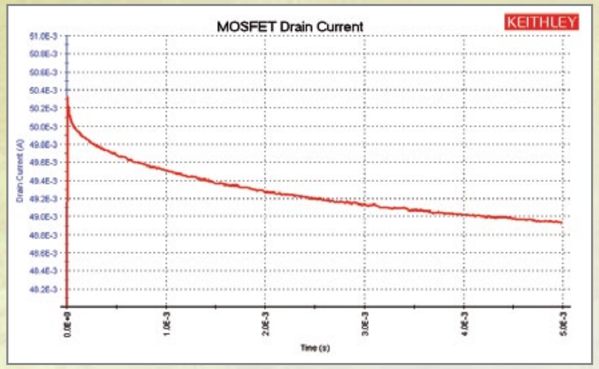
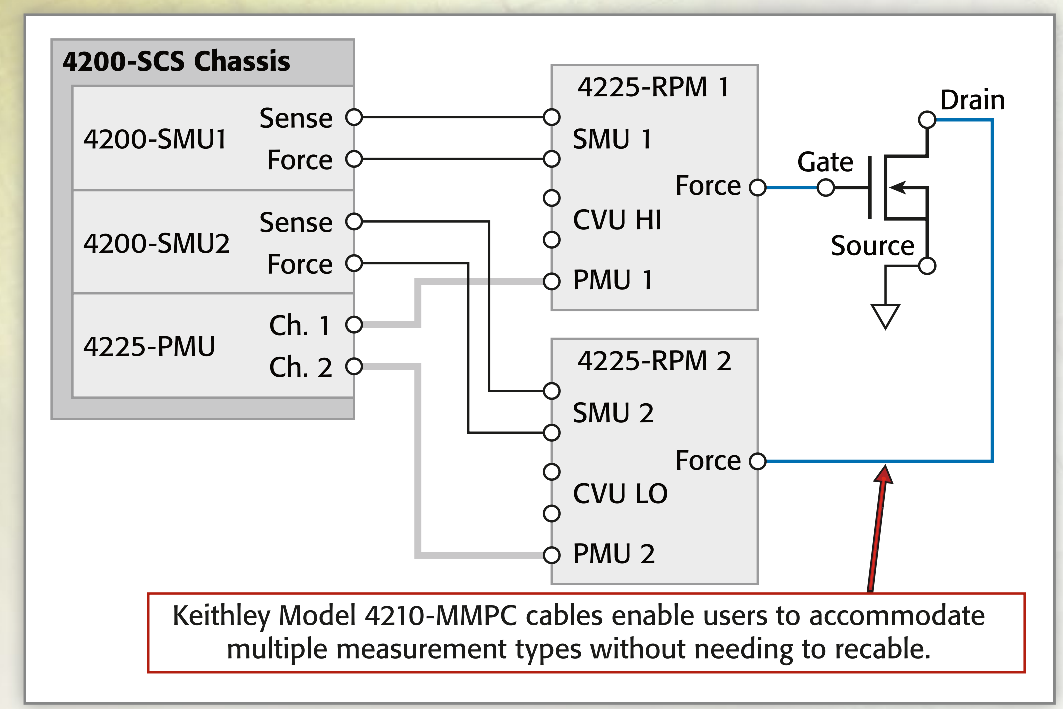


Figure 14. Waveform capture of MOSFET drain current



Keithley Model 4210-MMPC cables enable users to accommodate multiple measurement types without needing to recable.

Figure 15. Test circuit showing both the PMU and SMUs connected to a MOSFET

Self-heating tests can be performed using either the DC I-V technique or the pulsed I-V technique. However, the self-heating and charging effects of transistors will cause the pulsed I-V and DC I-V measurement results to look very different. The optional Model 4225-RPM Remote Amplifier/Switch Module can be used to switch in the Model 4225-PMU (pulsed I-V) or the Model 4200-SMU (DC I-V) to measure the device under test. **Figure 15** shows a test circuit showing both the PMU and SMUs connected to a MOSFET.

The results of generating both the pulsed I-V (dashed line) and the DC I-V (straight line) family of curves on a MOSFET are illustrated in **Figure 16**. Note the heating effects apparent in the curves of the DC measurements taken at higher gate and drain voltage levels. Remember that the pulsed I-V curve is made up of current measurements taken at discrete voltage pulses. To increase accuracy, each current measurement can be the average of measurements taken over a user-defined number of pulses.

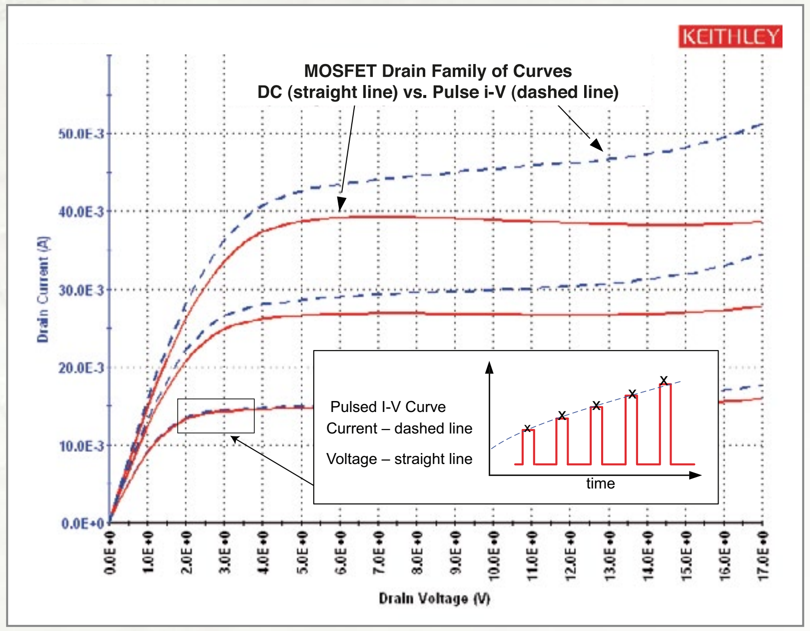


Figure 16. Self-heating effects on MOSFET shown with both pulsed I-V and DC I-V tests

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## Charge trapping

High dielectric constant (high κ) materials have drawn a great deal of attention recently for their applications as replacements for conventional $SiO_2$ in gate dielectrics. One of the reliability issues associated with high κ transistors is trapped charge. Several techniques have been developed to measure this trapped charge, including methods that involve DC I-V, C-V, and pulsed I-V measurements. One pulsed I-V technique is the slow single-pulse charge trapping method, which is used to investigate the charge trapping and de-trapping behavior of high κ gate structures. As shown in **Figure 17**, the gate pulse usually starts in a position that discharges the gate capacitor before the voltage ramp begins. This is intended to clean up any residual charges that might be trapped in the gate. Then, during the rise time of the voltage ramp, the corresponding drain current response is captured. Measuring the drain current over the entire gate voltage pulse allows generating a $V_{GS}$-$I_D$ curve over the pulse's rise time and fall time.

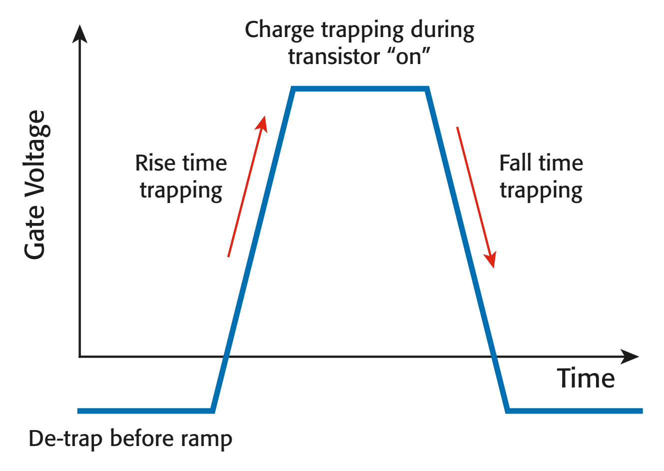

Figure 17. Trapping and de-trapping in a single gate voltage pulse

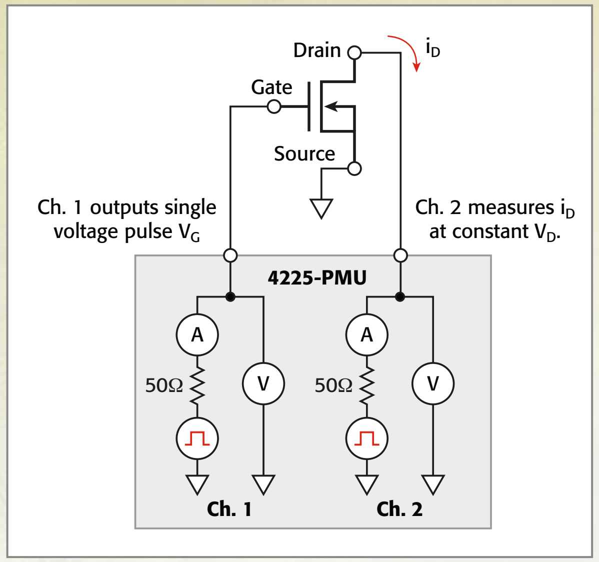

Figure 18. Single-pulse charge trapping measurement circuit using Model 4225-PMU

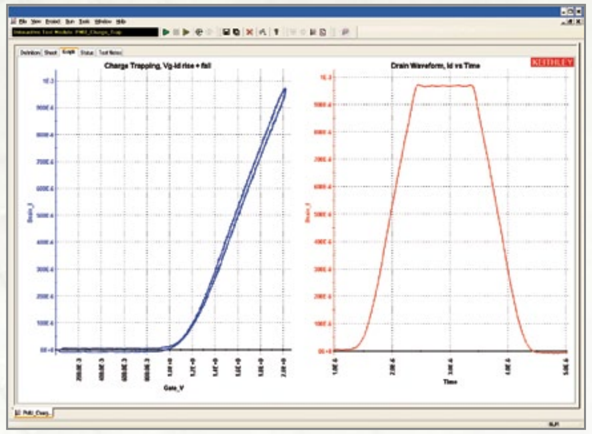

Figure 19. Drain current vs. gate voltage curve of single voltage pulse. The hysteresis curve is shown on the left (drain current versus gate voltage), and the current waveform (drain current versus time) used to capture the data is the right graph.

This single-pulse charge trapping method can be performed using one Model 4225-PMU under the control of the system's KTEI 8.2 software. **Figure 18** shows the single-pulse charge trapping measurement circuit. Channel 1 outputs a single gate voltage pulse; Channel 2 measures the drain current and outputs a constant drain voltage.

The measurement curves resulting from executing the test are shown in **Figure 19**. The left graph is the drain current vs. gate voltage measurements over a single pulse. The right graph shows the measured drain current as a function of time. As the pulse width is in-creased, the amount of trapped charge should also increase, producing a substantial difference between the rise and fall time data.

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## NBTI and PBTI Characterization, Modeling, and Monitoring

The characterization, modeling, and control of NBTI continue to challenge developers of deeply scaled silicon CMOS transistor designs. Over time, NBTI effects cause a transistor's threshold voltage ($V_T$) to shift and its sub-threshold drain current to increase significantly. These factors directly and severely limit the lifetime of the transistor, as well as the circuit performance. These effects must be accurately modeled for use in high speed logic circuits under conditions similar to those experienced by the device during actual usage. Additionally, NBTI and PBTI (which affects nMOS transistors) are process and materials dependent. Consequently, BTI (i.e., either positive or negative BTI) must be monitored during process integration and production.

During BTI characterization, the transistor is alternately stressed and characterized. The stress phase uses either a DC or AC stress on the gate; the other transistor terminals are grounded. During characterization, the gate and drain are simulated while the drain current is measured. While this seems simple enough, the BTI mechanism is susceptible to relaxation effects. This means that the instant the stress is removed, the transistor starts to recover and the degradation fades. Because it is crucial to characterize the degradation prior to relaxation, ultra-fast I-V techniques are required. The Model 4200-BTI-A Ultra-Fast BTI Package for the Model 4200-SCS provides the best possible combination of speed and sensitivity for ultra-fast BTI testing. This package includes one Model 4225-PMU, two Model 4225-RPMs, and Automated Characterization Suite (ACS) software. **Figure 20** illustrates this package combined with the Keithley Model 4210-MMPC cables, which enable the user to make multiple measurement types without recabling.

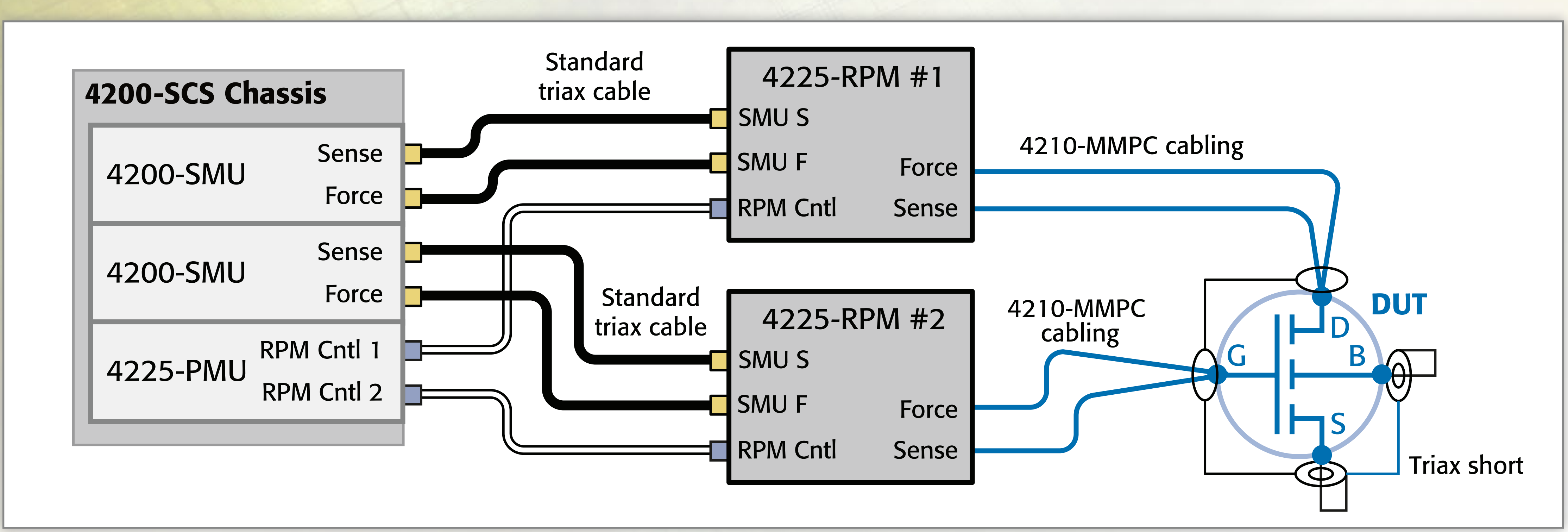

Figure 20. The Model 4200-BTI-A Package for the Model 4200-SCS includes instrumentation and software required to characterize nMOS and pMOS devices

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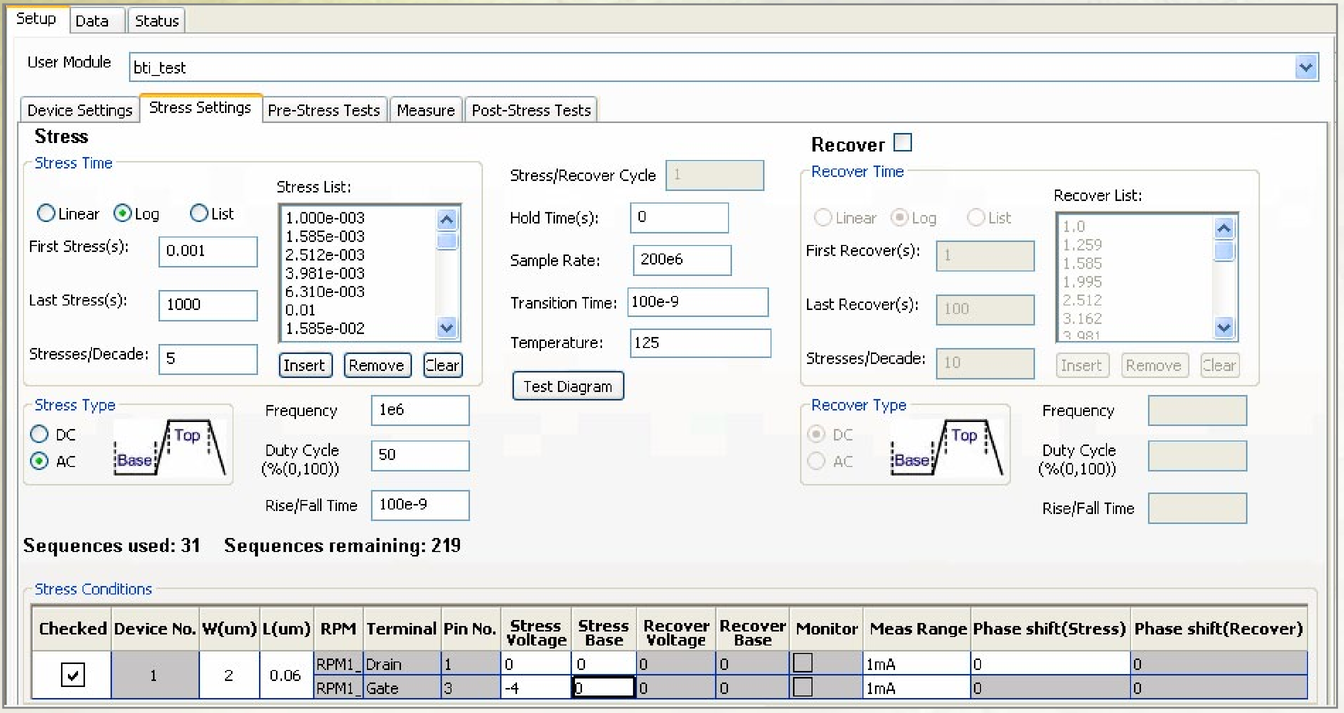
## NBTI and PBTI Characterization, Modeling, and Monitoring

Bias temperature instability is well documented as a highly dynamic phenomenon that requires sensitive, high-speed measurements for accurate characterization. Measurement physics largely defines the relationship between measurement speed and sensitivity, assuming all other factors are constant. Given that fact, in sub-millisecond measurement regimes, it's critical to consider all sources of noise; in sub-microsecond regimes, quantum effects cannot be ignored. The Model 4200-BTI-A has been painstakingly designed to approach the limits of measurement physics while maximizing ease of use in BTI test applications.

To avoid hot carrier injection effects or unwanted charge displacement during BTI testing, it is critical to minimize drain-to-source fields. All BTI characterization techniques rely on measuring drain current with a voltage applied to the drain. Because the drain current is proportional to the drain-to-source field, the more sensitive the drain current measurement is, the lower the required drain voltage will be. The Model 4200-BTI-A package's superior low current measurement capability allows the use of lower drain voltages to produce superior results.

In addition to the low current and high speed capabilities of the hardware configuration, the ACS software enables the user to easily configure the specific BTI tests, such as the one shown in the Stress Settings window shown in **Figure 21a**. The BTI test software module supports spot, step, sweep, smooth sweep and sample measurement types. These measurement types allow for common BTI measurement approaches such as on-the-fly or triangle sweeps. The timing for each type is defined by the test sample rate and the individual measurement settings. A schematic of a typical test is shown in **Figure 21b.**



User Module: bti_test

**Stress**

Stress Time

○ Linear ● Log ○ List

First Stress(s): 0.001

Last Stress(s): 1000

Stresses/Decade: 5

Stress List:
1.000e-003
1.585e-003
2.512e-003
3.981e-003
6.310e-003
0.01
1.585e-002

Stress/Recover Cycle: 1

Hold Time(s): 0

Sample Rate: 200e6

Transition Time: 100e-9

Temperature: 125

Stress Type

○ DC
● AC

Frequency: 1e6

Duty Cycle (%(0,100)): 50

Rise/Fall Time: 100e-9

**Recover** ☐

Recover Time

○ Linear ● Log ○ List

First Recover(s): 1

Last Recover(s): 100

Stresses/Decade: 10

Recover List:
1.0
1.259
1.585
1.995
2.512
3.162
3.981

Recover Type

● DC
○ AC

Frequency:

Duty Cycle (%(0,100)):

Rise/Fall Time:

**Sequences used: 31 Sequences remaining: 219**

Stress Conditions

| Checked | Device No. | W(um) | L(um) | RPM | Terminal | Pin No. | Stress Voltage | Stress Base | Recover Voltage | Recover Base | Monitor | Meas Range | Phase shift(Stress) | Phase shift(Recover) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ☑ | 1 | 2 | 0.06 | RPM1_ | Drain | 1 | 0 | 0 | 0 | 0 | ☐ | 1mA | 0 | 0 |
| | | | | RPM1_ | Gate | 3 | -4 | 0 | 0 | 0 | ☐ | 1mA | 0 | 0 |

Figure 21a. Define stress timing and stress conditions easily using familiar parameters like timing - log, linear, custom list; measurements per decade; AC or DC stress; optional recovery test sequence; and test sample rate (speed)

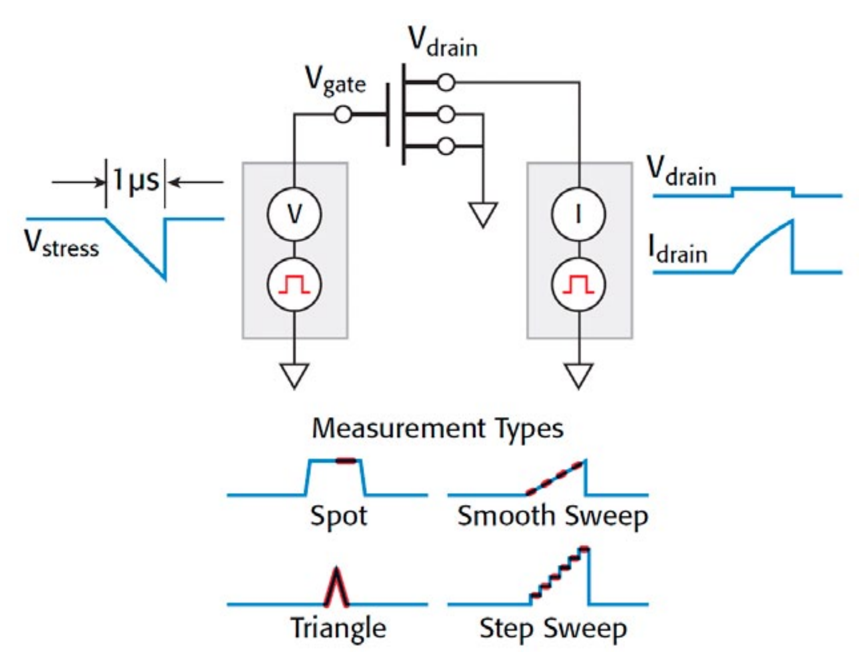


Figure 21b. Schematic of typical BTI test

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## NON-VOLATILE MEMORY DEVICE TESTING

The Model 4225-PMU is the ideal instrument for testing single memory cells or a small array of cells, such as when isolated cells need to be tested in research and development or for process verification. Because the Model 4225-PMU can be used for both the pulsing and measurement, total test time is reduced. The Model 4200-SCS provides built-in stress/measure looping capability that's useful for performing lifetime and reliability tests on non-volatile memory devices. Its software also includes projects created for testing flash, phase change memory (PCRAM) and ferro-electric memory (FeRAM) devices.

### Flash Memory

A flash memory cell is basically a MOSFET except that it has two gates: a control gate (CG) and a floating gate (FG). The control gate reads, programs, and erases the floating gate. The floating gate stores charge that represents data stored in the memory. Voltage pulses are used to move charge to or from the floating gate. The presence of charge on the floating gate shifts the voltage threshold ($V_T$) to a higher voltage. A pulse generator is used to output pulses to program and erase the cell; SMUs measure the DC threshold voltage after programming and erasing the cell. **Figure 22** is a basic schematic of a Model 4200-SCS-based flash memory test system. In this circuit, each terminal of the cell is connected to both an SMU and a pulse generator (either the Model 4225-PMU or the Model 4220-PGU).

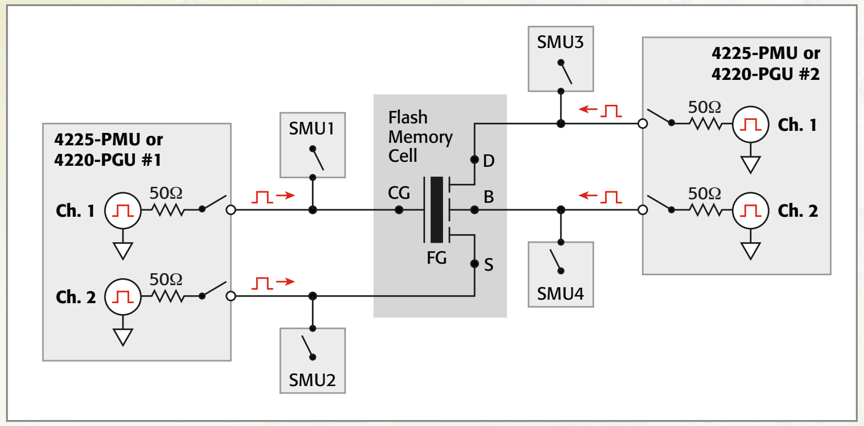

Figure 22. Basic interconnect schematic for floating gate flash memory testing

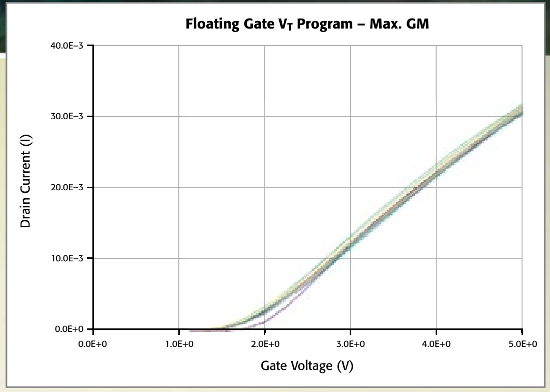

Figure 23. Measurement results of cycle testing of floating gate $V_T$ in program mode

The Model 4200-SCS comes with software to perform the three most important tests related to flash memory testing: characterization, disturb testing, and endurance testing. The Model 4225-PMU or Model 4220-PGU are used to program and erase the device and the Model 4200-SMUs make the $V_T$ measurements. The software automatically opens and closes the output relays of the SMUs and pulse generators, which eliminates the need for bias tees or an external switch matrix. The software can also cycle the system through the program-erase-measure process. The results of measuring the threshold voltage each time after twenty program cycles are shown in **Figure 23**. During each cycle, a new curve is appended to the graph and a separate Excel-like spreadsheet is added to a notebook of data, which can be saved as an .xls or .csv file.

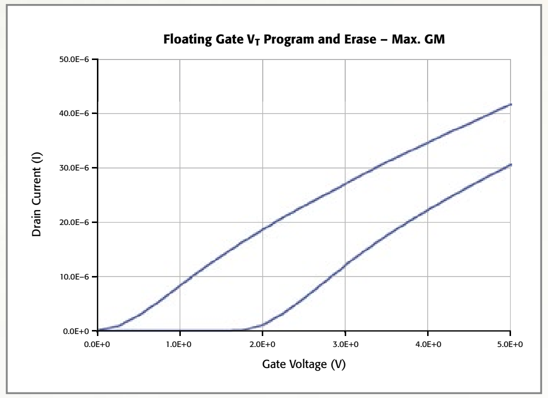

Figure 24. Threshold voltage measurement in erased and programmed states

The difference between the $V_T$ curves in the erased and programmed state is shown in **Figure 24**.

For testing multiple devices or for measuring adjacent cells used for the disturb tests, a Model 707B or Model 708B Switch Matrix with the Model 7174A 8x12 Matrix Card(s) can be used. The software also includes drivers for using this switch matrix in these tests.

For additional information on NVM characterization, download a **FREE** copy of **Keithley Application Note #3141:** ***"Pulse I-V Characterization of Non-Volatile Memory Technologies"***.

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## Phase Change Random Access Memory (PRAM or PCRAM)

Phase change memory is a type of non-volatile memory device that has a reversible state based on a change in the resistance of the cell. When a voltage pulse is applied to the cell, its state changes from an ordered (crystalline) structure to a disordered (amorphous) structure or vice versa. The data storage, based on this phase change, can be measured as a change of resistance of the cell. Pulsed voltage is used to 'set' and 'reset' the cell.

For PCRAM testing, one Model 4225-PMU replaces the traditional memory test circuit, which consists of a two-channel digital scope, a pulse generator, a load resistor, a bias tee, and a DC measuring instrument. The Model 4225-PMU outputs voltage pulses to set and reset the cell; simultaneously, it is used to measure the DC current, voltage, and resistance. **Figure 25** shows how simple it is to connect a single Model 4225-PMU to a PCRAM device. Channel 1 outputs the voltage pulses; Channel 2 measures the resulting current.

**Table 1** lists some of the basic tests performed on PCRAM devices. Basically, the measuring instruments must be able to place the cell in a known condition, reset the cell, measure DC current and calculate resistance, and set the cell. To simplify testing, the Model 4200-SCS comes with software and tests that perform the various test modes listed.

The typical voltage output and measurement results of the reset and set tests are shown in **Figure 26**. Users can easily define the voltage waveforms using the supplied interactive software, which is based on the Model 4225-PMU's Segment ARB function.

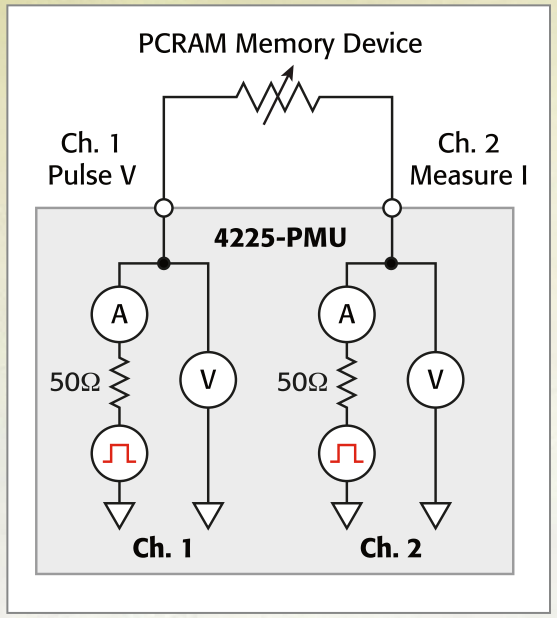

Figure 25. Connecting the Model 4225-PMU to a PCRAM cell

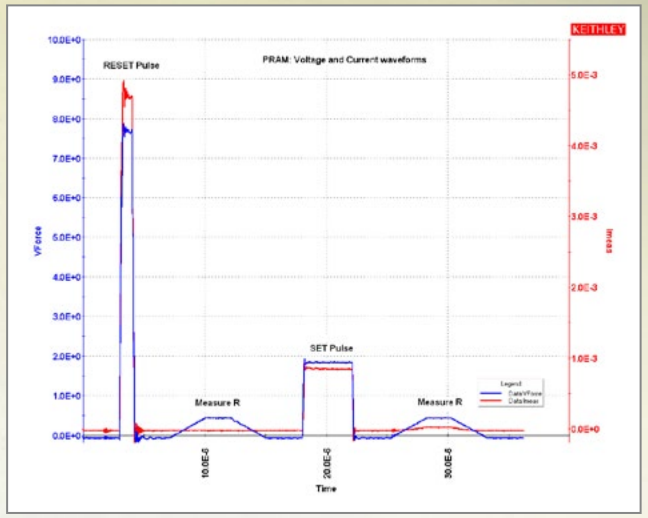

Figure 26. PRAM voltage (blue) and current (red) waveforms that apply the RESET and SET voltage pulses, as well as measures the resistance before and after the SET pulse.

| Test Mode | Description |
|---|---|
| Initial Conditions | Outputs user-defined number of pulses in order to place device in known condition. |
| Reset | Outputs user-defined pulse (amplitude, pulse width, rise/fall times, etc.) and captures waveform of current, voltage, and resistance. |
| Measure Current and Resistance | Test performed after reset and set modes. Performs waveform capture of current, voltage, and resistance. Calculates a "spot mean" value for both current and resistance. |
| Set | Outputs user-defined pulse (amplitude, pulse width, rise/fall times, etc.) and captures waveform of current, voltage, and resistance. |

Table 1. PCRAM test modes and descriptions

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## Ferro-electric Random Access Memory (FeRAM)

FeRAM memory effect relies on charge storage in a capacitor using a ferro-electric layer instead of the dielectric layer of a typical capacitor. The memory mechanism for FeRAM is based on polarization shift in ferro-electric materials, which have strong non-linear dependency between applied electrical field (E) and polarization (P). When the electric field reaches a critical level, the ions inside the crystalline structure move from one stable location to another. Electrically, the shift is represented by the hysteresis chart (**Figure 27**), showing the dependency between electrical field and polarization (or charge). The switch between one state and another is characterized by the area of hysteresis, which represents the amount of charge moved during re-polarization.

For FeRAM testing, one Model 4225-PMU (similar to Figure 25 connections) replaces the traditional FeRAM test setup, which consists of an oscilloscope, sense/load capacitor and a pulse generator. The challenge for FeRAM characterization is to measure the charge transferred during the test. The traditional setup does this indirectly, by measuring the voltage across the sense capacitor with the oscilloscope. The PMU samples the current flowing versus time, and avoids the problems of the oscilloscope trying to accurately measure a small voltage and the voltage drop due to the sense capacitor.

The included project has tests for hysteresis, PUND and endurance. The PUND test applies 4 pulses sequentially to the device (Positive, Up, Negative, Down), which characterizes the polarity change of the ferro-electric material. The charge (current) is taken from the initial rise time of the 4 pulses to calculate the polarization charge or memory effect (**Figure 28**). The timing and voltages for the tests can be easily modified by the user, while the software calculates the total charge and polarization parameters.

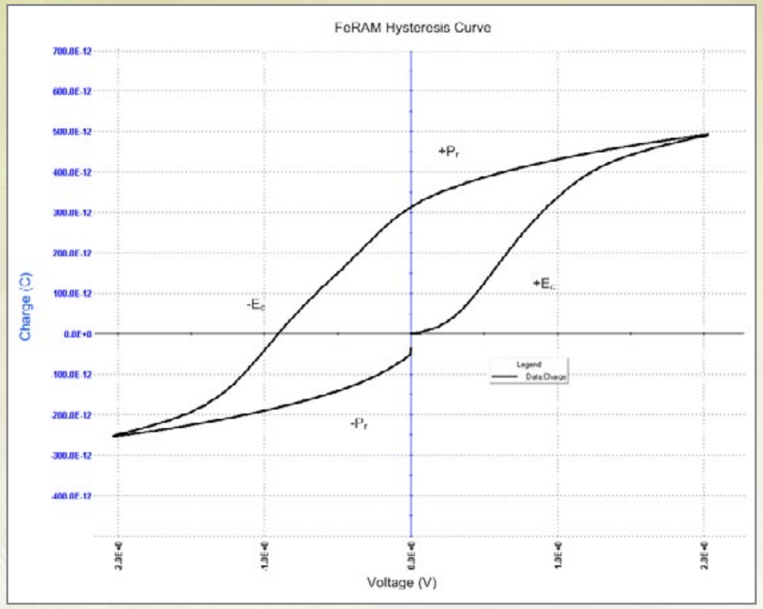
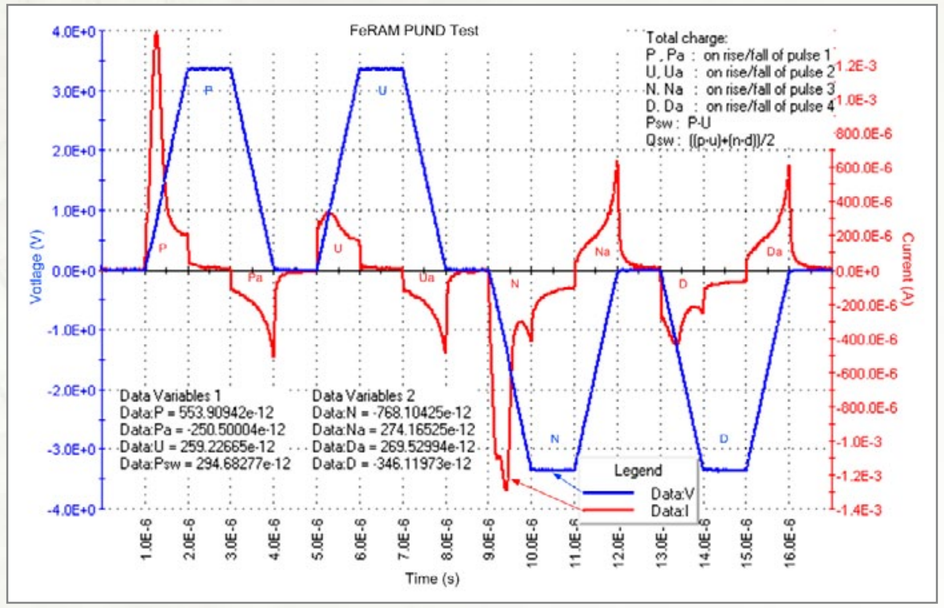


Figure 27. Example FeRAM Hysteris curve



Total charge:
P , Pa : on rise/fall of pulse 1
U, Ua : on rise/fall of pulse 2
N. Na : on rise/fall of pulse 3
D. Da : on rise/fall of pulse 4
Psw : P-U
Qsw : [(p-u)+(n-d)]/2

Data Variables 1
Data:P = 553.90942e-12
Data:Pa = -250.50004e-12
Data:U = 259.22665e-12
Data:Psw = 294.68277e-12

Data Variables 2
Data:N = -768.10425e-12
Data:Na = 274.16525e-12
Data:Da = 269.52994e-12
Data:D = -346.11973e-12

Figure 28. PUND test showing the applied pulses (blue waveform) and the resulting current (red waveform). The graph is labeled with the P, U, N, D pulses and the charge (red P, U, N, D).

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## COMPOUND SEMICONDUCTOR DEVICES AND MATERIALS

Pulsed I-V testing is often performed on devices made from III-V materials, such as GaN, GaAs, and other compound semiconductor materials. These larger band gap devices are often used in higher power and RF devices. Pulsed I-V measurements make it possible to manage or investigate the effects of dispersion during electrical characterization. Sometimes it is necessary to test devices at higher frequencies in order to simulate the conditions the actual device will encounter in regular use. The Model 4225-PMU allows setting a pulse offset voltage so that measurements can be made from a non-zero value, which can be used to investigate the amplifier gain or linearity of a device. Laser diodes and power MOSFETs are two common compound semiconductor devices that often require pulse I-V measurements for characterization.

### Laser Diode

To manage heating effects, laser diodes are often characterized using pulsed I-V techniques. In some cases, a photodiode is built in to serve as an output monitor of the laser diode. If this is the case, the two-channel 4225-PMU can sweep the pulsed voltage and measure the laser diode current from one channel while simultaneously measuring the photodiode current with the other channel. A circuit diagram for performing these measurements is shown in **Figure 29**. The user can add an optional load resistor in series with the laser diode to better mimic a current source.

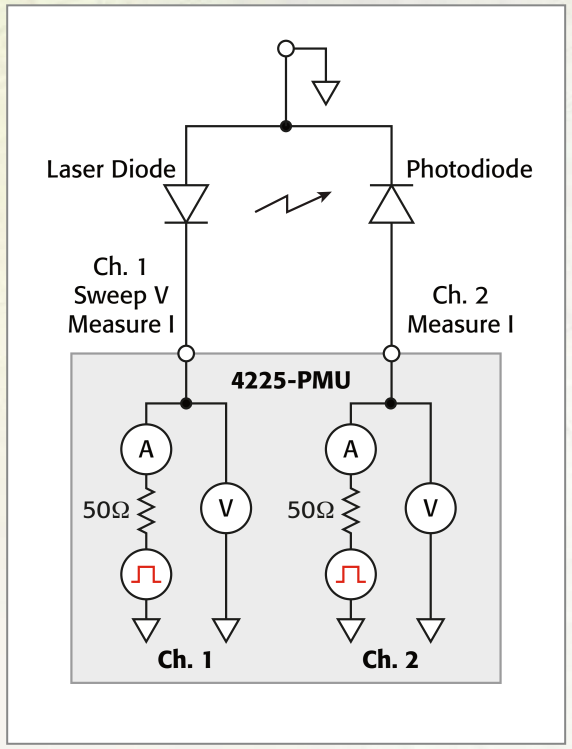

Figure 29. Laser diode test configuration

### Thermal Impedance Measurements

Evaluating the thermal performance of power MOSFETs and other semiconductor devices is important because a device's junction temperature can affect its operational parameters and lifetime. The transient thermal impedance measures the behavior of a device when pulsed power is applied to it. Depending on the particular application, this may involve applying a single pulse, a series of repetitive pulses, or a series of pulses of increasing pulse width. The transient thermal impedance is derived from the pulsed power, pulse duration, and duty cycle. The impedance is often plotted as a function of the pulse duration.

The Model 4225-PMU is useful for making thermal impedance measurements because it can simultaneously measure both the current and voltage, can sweep pulsed voltages as a function of the pulse width, and calculate the power and impedance using its built-in mathematical tool called the Formulator.

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## NANOTECHNOLOGY AND MEMS DEVICES

High speed I-V testing can be performed on a variety of devices made from carbon nanotubes (CNTs), semiconductor nanowires, graphene-based devices, molecular-based electronics, and MEMs structures such as switches. Characterizing the electrical properties of these delicate nanoelectronic components and materials requires instruments and measurement techniques optimized for low power measurements. Low temperature materials, nanodevices, and sub-micron silicon structures can easily be altered or destroyed by the heat generated when making traditional DC measurements. Pulsed electrical testing reduces the total energy dissipated in a device, and thus the potential for damage. Pulsed I-V measurements can also prevent current drifting in measurements that can occur during traditional DC measurements. For testing CNT FET-based sensors, gate pulsing allows faster refreshing of the sensor.

To make the pulsed I-V measurements, the nanodevice under test is excited for a very short time interval with a voltage pulse high enough to produce a quality measurement. This pulse width can range from tens of nanoseconds to milliseconds in length, depending on the impedance and capacitance of the device or the application. The waveform capture mode can be used to verify an appropriate pulse width prior to the actual pulsed I-V sweep.

A pulsed I-V measurement configuration for a carbon nanotube-based FET is shown in **Figure 30**. In this diagram, Channel 1 is connected to the drain of the CNT FET and Channel 2 is connected to the gate. The source terminal of the FET is connected to the PMU common terminal, which is the outside shell of the coax cable. If measurements must be made between any three of the terminals, then a second Model 4225-PMU must be added to the system.

The results of performing a pulse I-V family of curves on a CNT FET using the Model 4225-PMU is shown in **Figure 31**. In this particular test, the current measurements were taken on the 100 µA range, but a threshold level was set to 20 µA so that the test stops if the threshold current is reached.

More information about performing electrical characterization on CNT FETs can be found in Keithley's **Application Note #3092:** *Electrical Characterization of Carbon Nanotube Transistors (CNT FETs) with the Model 4200-SCS*

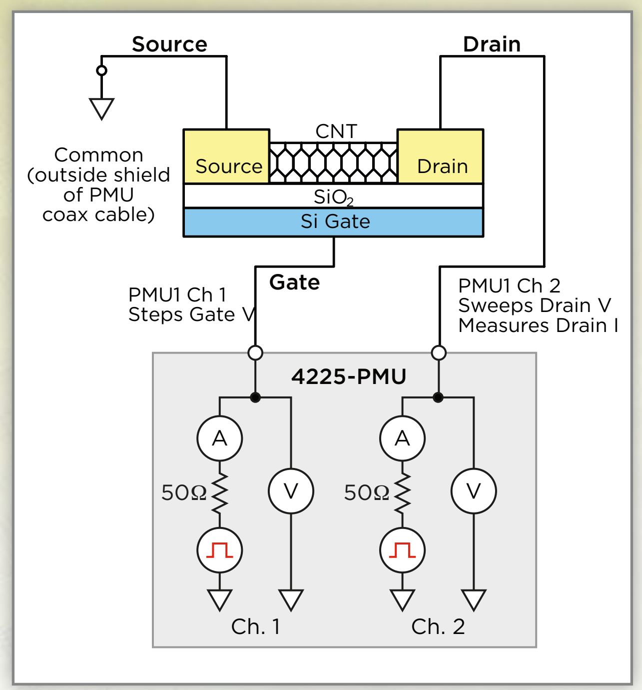

Figure 30. Circuit diagram for measuring the pulsed I-V characteristics of a CNT FET

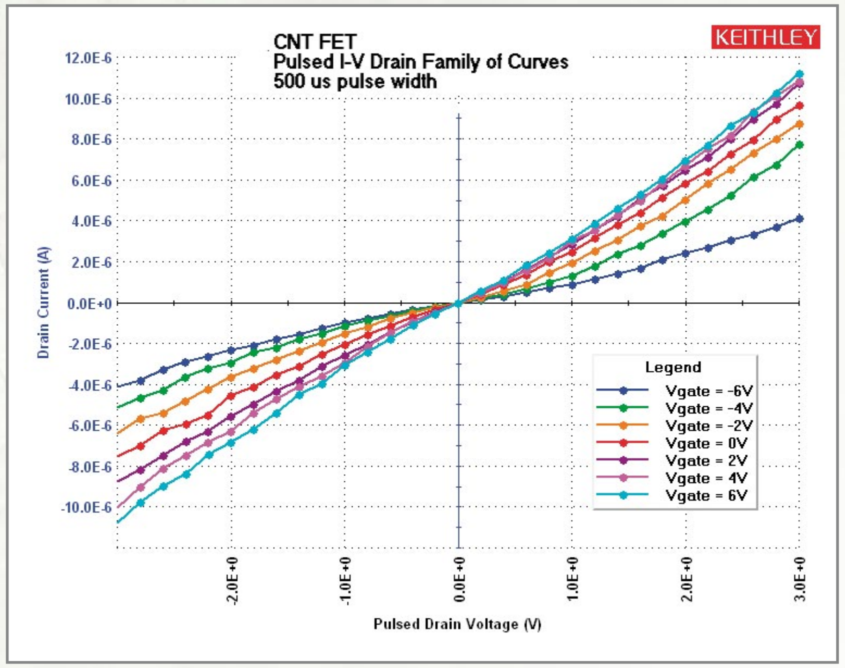

Figure 31. Graph of a CNT FET drain family of curves for various gate voltages

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## SOLAR CELLS

The demand for solar cells, which convert sunlight directly into electricity, is growing as the demand for alternative sources of energy increases. A variety of electrical measurements are made on solar cells to characterize their performance, including their output and efficiency. A variety of important parameters are derived from DC I-V and C-V measurements, including the cell output current, maximum power output, conversion efficiency, resistivity, doping density, etc.

Using the Model 4225-PMU, pulsed I-V measurements can also be made on solar cells (**Figure 32**). Given that solar cell conversion efficiency is influenced by the time of the applied voltage, making pulsed I-V measurements allows for shorter bias times. In addition to sourcing a pulsed voltage, the PMU can sink current so it can measure a solar cell's current output. Because solar cells are fairly capacitive, it is important to ensure the pulse width is long enough for the pulsed I-V sweep. The waveform capture mode should be used to verify the pulse width prior to generating the pulsed I-V sweep. The results of generating a pulsed I-V sweep on a silicon solar cell are shown in **Figure 33**. Note that the current is in the fourth quadrant of the curve. This indicates that the PMU is sinking current; in other words, the current is flowing out of the solar cell and into the PMU.

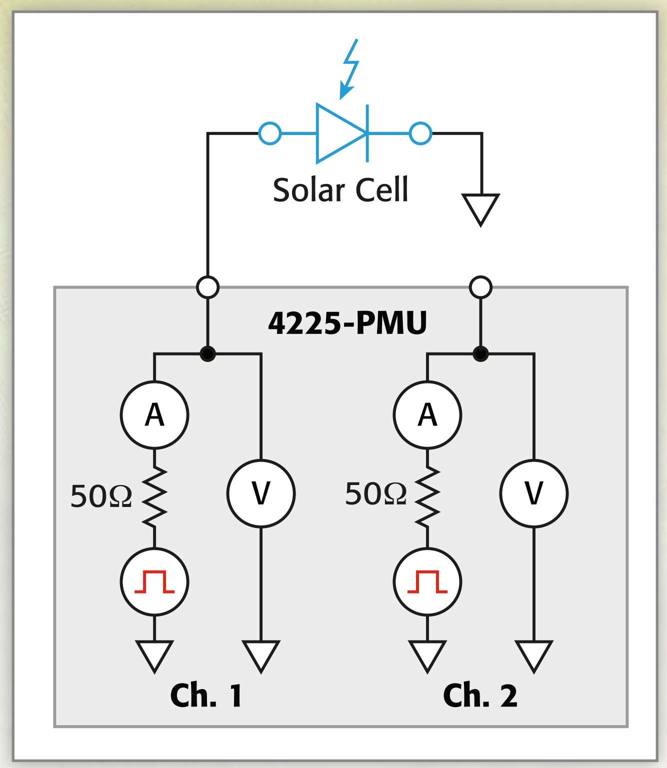

Figure 32. Connections of a solar cell to the Model 4225-PMU

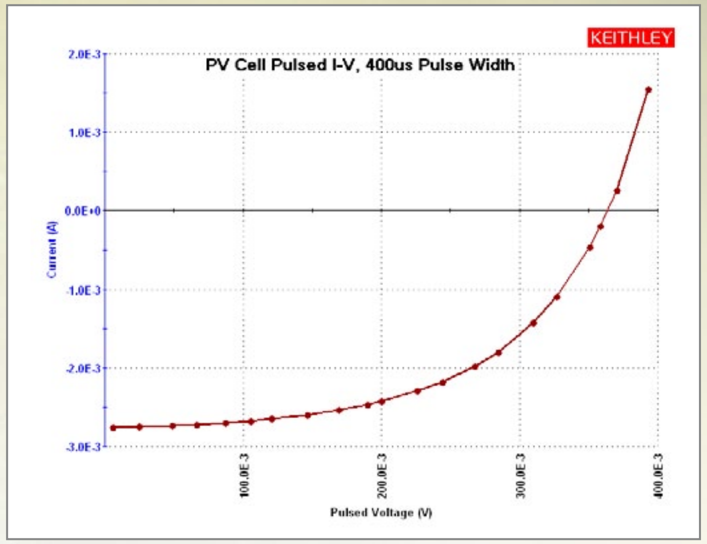

Figure 33. Pulsed I-V curve of a silicon solar cell

More information about performing electrical measurements on solar cells can be found in Keithley **Application Note #3026**, ***"Electrical Characterization of Photovoltaic Materials and Solar Cells with the Model 4200-SCS Semiconductor Characterization System".***

## OTHER TESTS

The wide dynamic range and sensitivity of the Model 4225-PMU make it an ideal solution for other applications, including measurements on organic TFT displays, fast TDDB, 1/f noise, and random telegraph signals (RTS).

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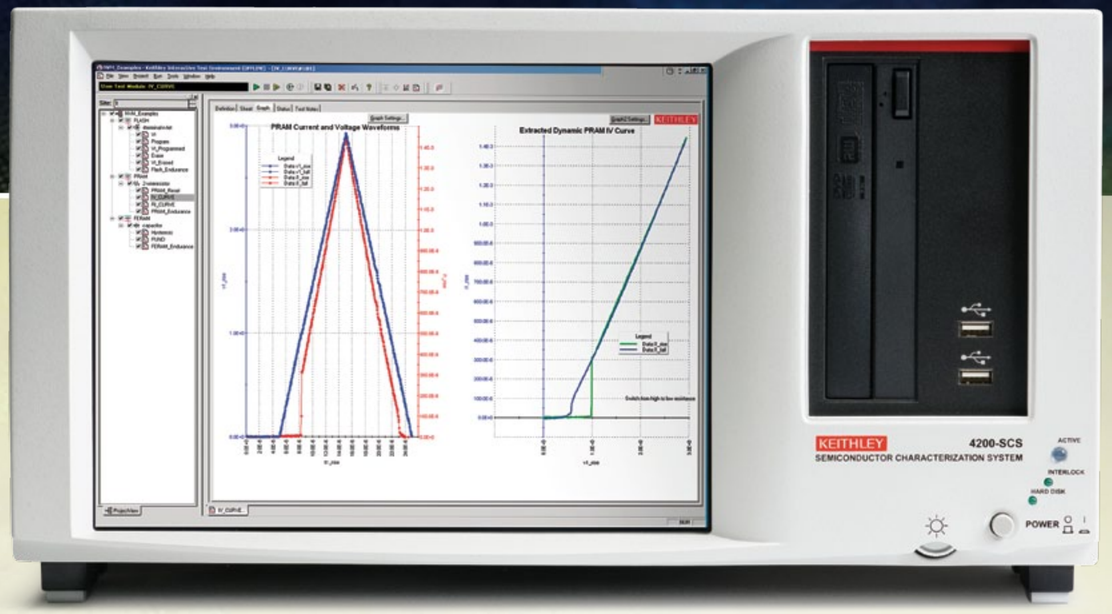

A broad range of applications can be performed by the Model 4225-PMU Ultra-Fast I-V Module because of its high speed, wide current measurement range, waveform capture mode, Segment ARB function, point-and-click interactive software control, built-in projects for specific tests, and the many other features described here. Its applications include MOSFET device characterization, general pulsed I-V testing of devices, CMOS characterization including charge pumping and charge trapping, non-volatile memory testing, compound semiconductor device testing, nanodevice measurements, solar cell evaluation, and many others.

The Model 4225-PMU is only one of several modules available for the Model 4200-SCS Semiconductor Characterization System. Depending on the application's requirements, the system can be configured to include precision DC SMUs, DC PreAmps, a multi-frequency C-V meter, and a pulse generator, making the Model 4200-SCS a complete, all-in-one-box characterization tool.

**Contact US:**
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