Applications for a New Power Buffer

Jim Williams

A frequent requirement in systems involves driving analog signals into non-linear or reactive loads. Cables, transformers, actuators, motors and sample-hold circuits are examples where the ability to drive difficult loads is required. Although several power buffer amplifiers are available, none have been optimized for driving difficult loads. The LT®1010 can isolate and drive almost any reactive load. It also offers current limiting and thermal overload protection which protect the device against output fault conditions. The combination of good speed, output protection, and reactive load driving capability (see box section, "The LT1010 at a Glance") make the device useful in a variety of practical situations.

Buffered Output Line Driver

Figure 1 shows the LT1010 placed within the feedback loop of an operational amplifier. At lower frequencies, the buffer is within the feedback loop and its offset voltage and gain error are negligible. At higher frequencies, feedback is through C_F so that phase shift from load capacitance acting against the buffer's output resistance does not cause loop instability.

UPDATE
Higher speed buffers are available on new monolithic processes

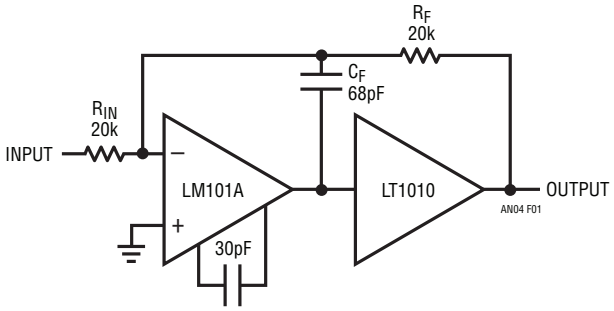


Figure 1. Practical LT1010 Based Boosted Op Amp

Figure 2 shows this configuration driving a 50Ω-0.33µF load. The waveform is clean, with controlled damping. With C load increased to a brutal 2µF, the circuit is still stable (Trace A, Figure 3), even though the large capacitance requires substantial current (Trace B) from the LT1010. Adjustment of the R_F-C_F time constant would allow improved damping.

Although this circuit is useful, its speed is limited by the op amp.

Fast, Stabilized Buffer Amplifier

Figure 4 shows a way to eliminate this restriction, while maintaining good DC characteristics. Here, the LT1010 is combined with a wideband gain stage, Q1-Q3, to form a fast inverting configuration. The LT1008 op amp DC stabilizes this stage by biasing the Q2-Q3 emitters to force a zero DC potential at the circuit's summing junction. The roll-offs of the fast stage and the op amp are arranged to provide smooth overall circuit response.

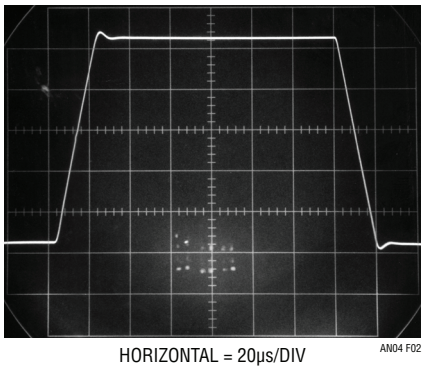


Figure 2

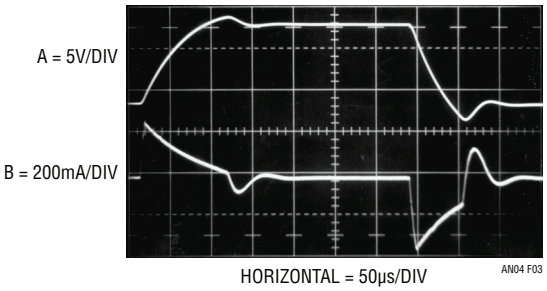


Figure 3

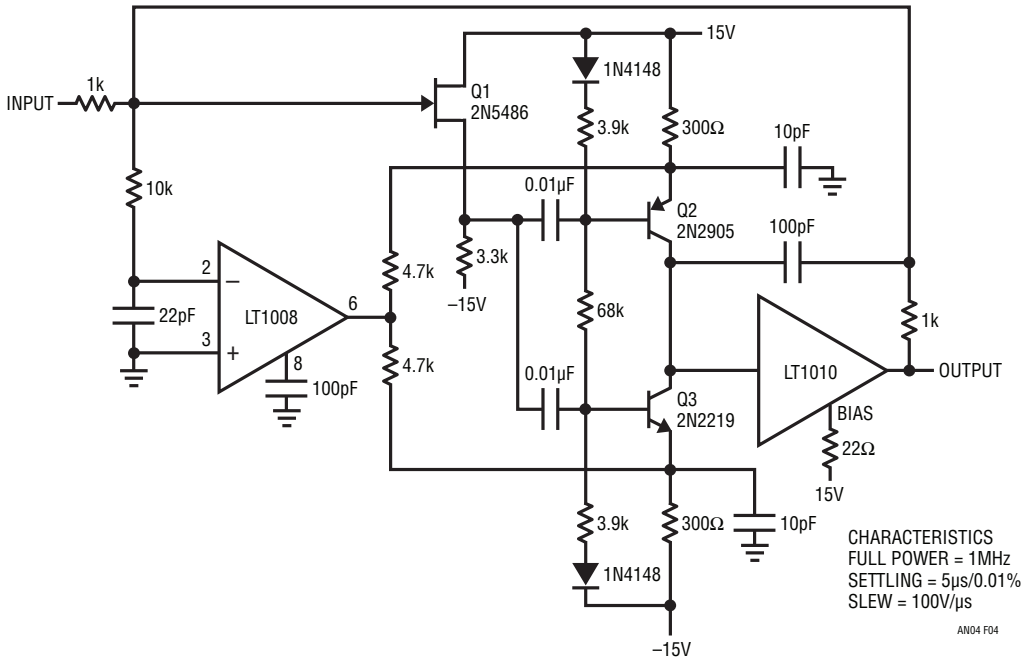


Figure 4. Fed Forward. Wideband DC-Stabilized Buffer

Because the circuit's DC stabilization path occurs in parallel with the buffer, higher speed is obtainable. Figure 5 shows the circuit driving a 600Ω-2500pF load. Despite the heavy load, the output (Trace B) does a good job of following the input (Trace A) at a gain of –1.

Video Line Driving Amplifier

In many applications, DC stability is unimportant and AC gain is required. Figure 6 shows how to combine the LT1010's load handling capability with a fast, discrete gain stage. Q1 and Q2 form a differential stage which single ends into the LT1010. The capacitively terminated feedback divider gives the circuit a DC gain of 1, while allowing AC gains up to 10. Using a 20Ω bias resistor (see box section), the circuit delivers $1V_{P-P}$ into a typical 75Ω video load. For applications sensitive to NTSC requirements, dropping the bias resistor value will aid performance.

At A = 2, the gain is within 0.5dB to 10MHz with the –3dB point occurring at 16MHz. At A = 10, the gain is flat (±0.5dB to 4MHz) with a –3dB point at 8MHz. The peaking adjustment should be optimized under loaded output conditions.

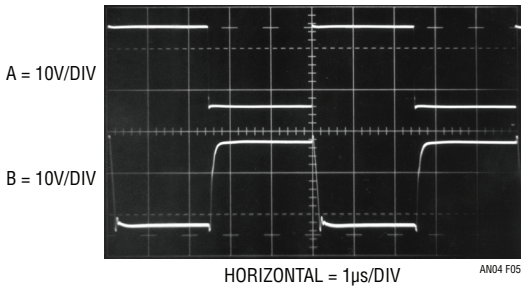


Figure 5

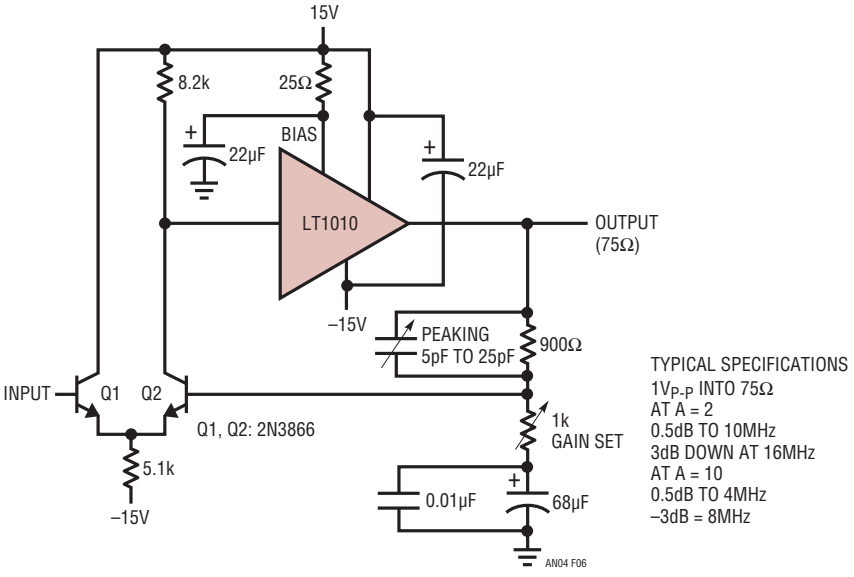


Figure 6. Video Line Driving Amplifier

Figure 7 shows a video distribution amplifier. In this example, resistors are included in the output line to isolate reflections from unterminated lines. If the line characteristics are known, the resistors may be deleted. To meet NTSC gain-phase requirements, a small value boost resistor is used. Each $1V_{P-P}$ channel output is essentially flat through 6MHz into a 75Ω load.

Fast, Precision Sample-Hold Circuit

Sample-hold circuits require high capacitive load driving capability to achieve fast acquisition times. Additionally, other trade-offs must be considered to achieve a good design. The conceptual circuit of Figure 8 illustrates some of the issues encountered. Fast acquisition requires high charge currents and dynamic stability, which the LT1010 can

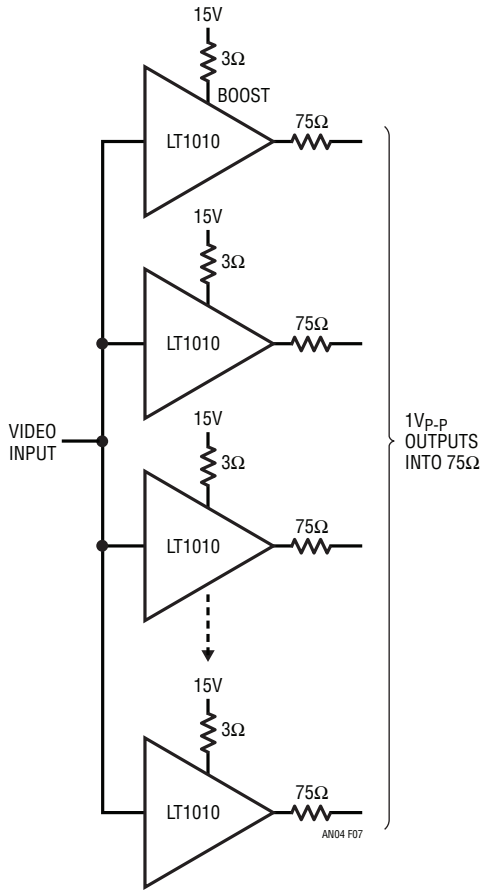


Figure 7. Video Distribution Amplifier

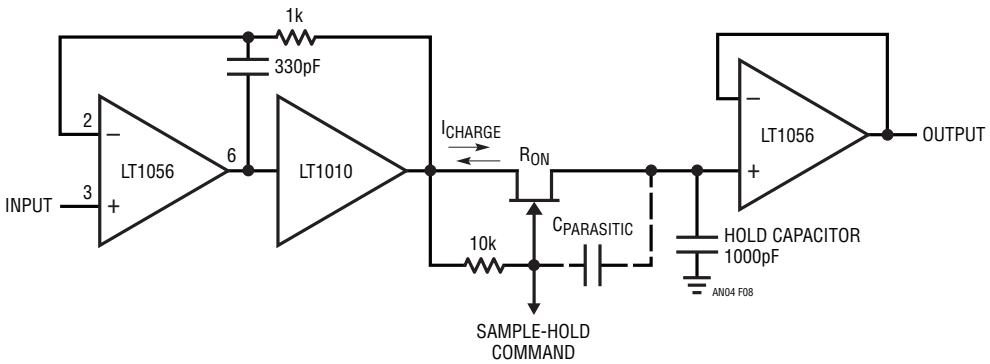


Figure 8. Conceptual Sample-Hold

provide. To get reasonable droop rate, the hold capacitor must be appropriately sized, but too large a value means FET switch on-resistance will effect acquisition time. If very low on-resistance FETs are used, the parasitic gate-source capacitance becomes significant and a substantial amount of charge is removed from the hold capacitor when the gate is switched off. This charge removal causes the stored voltage to abruptly change with the circuit is switched into the hold mode. This phenomenon, called "hold step", limits accuracy. It can be combatted by increasing the hold capacitor's value, but then acquisition time suffers. Finally, since a TTL compatible input is desirable, the FET requires a level shift. This level shift must provide adequate pinch-off voltage over the entire range of circuit inputs and must also be fast. Delays will result in aperture errors, introducing dynamic sampling inaccuracies.

Figure 9 shows a circuit which combines the LT1010 with some techniques to produce a fast, precise sample-hold circuit. Q1 through Q4 constitute a very fast TTL compatible level shift. Total delay from the TTL input switching into hold to Q6 turning off is 16ns. Baker clamped Q1 biases Q3's emitter to switch level shifter Q4. Q2 drives a heavy feedforward network, speeding Q4's switching. This stage affords low aperture errors, while providing the necessary level shift for Q6's gate. The hold step error due to Q6's parasitic gate-source capacitance is compensated for by Q5 and the LT318A amplifier (A3).

The amount of charge removed by Q6's parasitic capacitance is signal dependent (Q = CV). To compensate this error, A2 measures the circuit output and biases the Q5 switch. Each time the circuit switches into hold mode, an appropriate amount of charge is delivered through the

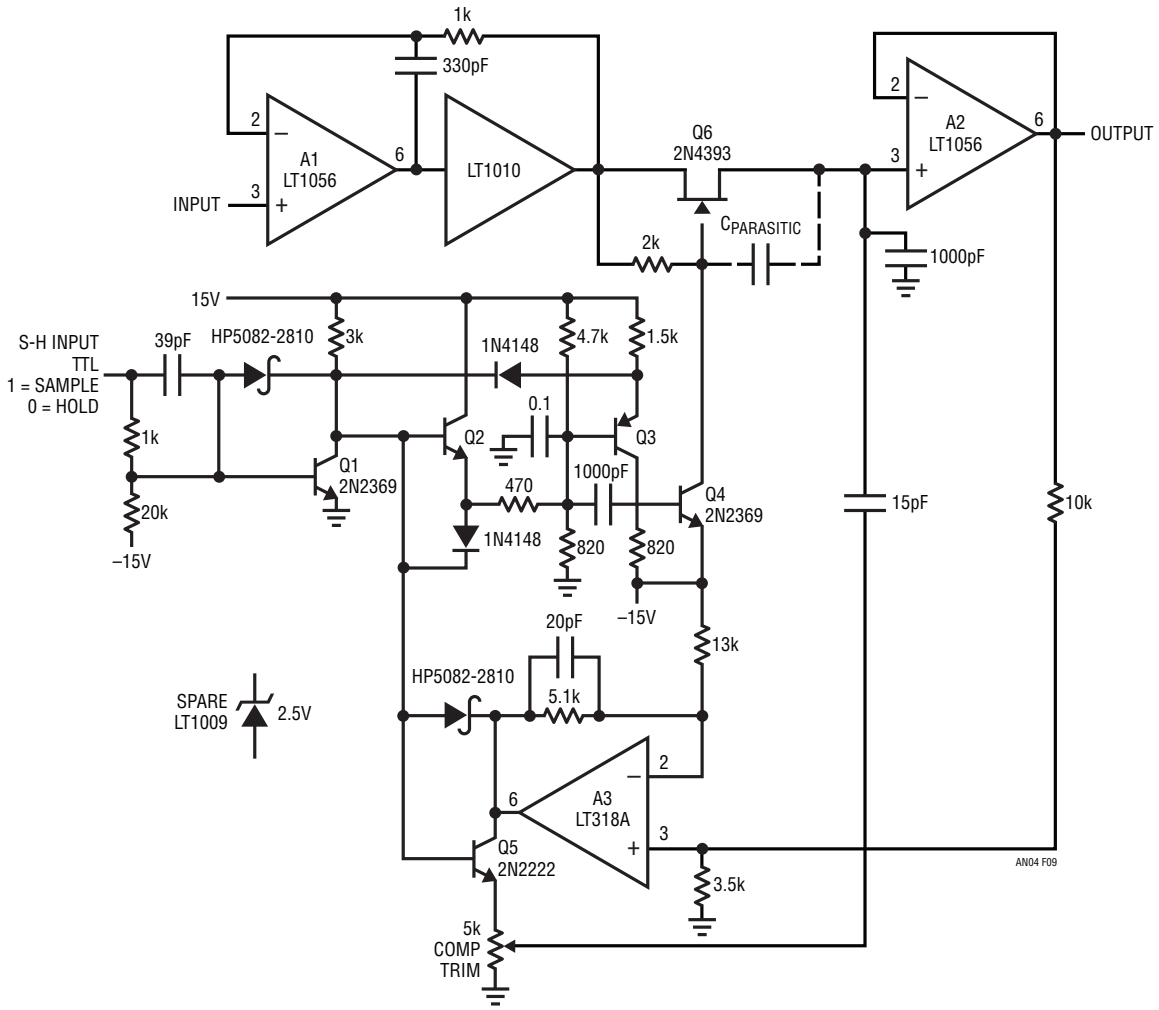


Figure 9. Fast Sample-Hold with Hold Step Compensation

potentiometer—15pF network in Q5's emitter. The amount of charge is scaled to compensate for charge removal due to Q6's parasitic term. A3's inverting input is biased so that negative supply shifts, which alter the charge removed through C parasitic, are accounted for in the compensating charge. Compensation is set by grounding the signal input, clocking the S-H line and adjusting the potentiometer for minimum disturbance at the circuit's output.

Figure 10 shows the circuit at work. When the sample-hold input (Trace A, Figure 10) goes into hold, charge cancellation occurs and the output (Trace B) sees less than 250µV of hold step error within 100ns. Without compensation, the error would be 50mV (Trace B, Figure 11—Trace A is the sample-hold input).

Figure 12 shows the LT1010's contribution to fast acquisition. The circuit acquires a 10V signal in this photograph. Trace A is the sample-hold input. Trace B shows the LT1010 delivering over 100mA to the hold capacitor and Trace C depicts the output value slewing and settling to final value. Note that the acquisition time is limited by amplifier settling time and not capacitor charge time. Pertinent specifications include:

Acquisition time: 2µs to 0.01%

Hold settling time: <100ns to 1mV

Aperture time: 16ns

Motor Speed Control

The LT1010's ability to drive difficult loads is exploited in Figure 13's circuit. Here, the buffer drives a motor-tachometer combination. The tachometer signal is fed back and compared to a reference current and the LM301A amplifier closes a control loop. The 0.47µF capacitor provides stable compensation. Because the tachometer output is bipolar, the speed is controllable in both directions, with clean transitions through zero. The LT1010's thermal protection is particularly useful in this application, preventing device destruction in the event of mechanical overload or malfunction.

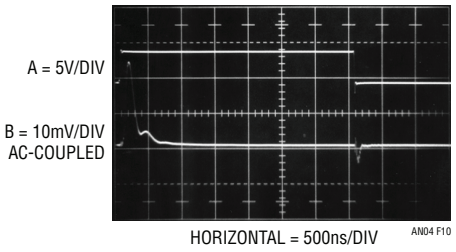


Figure 10

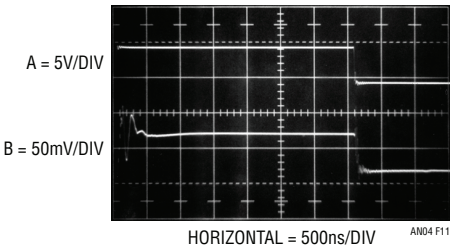


Figure 11

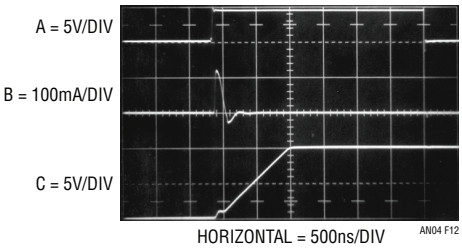


Figure 12

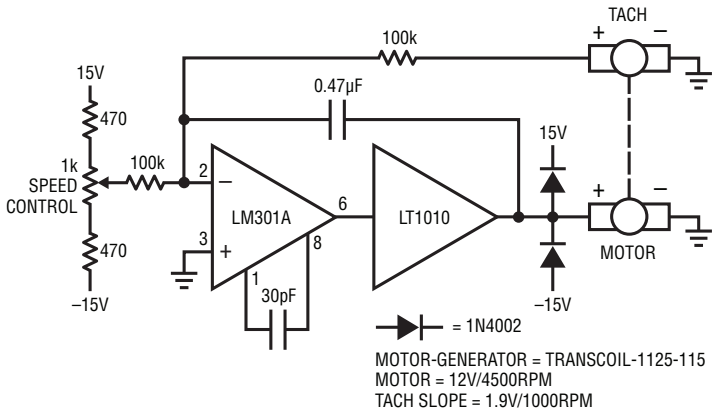


Figure 13. Overload Protected Motor Speed Controller

Fan-Based Temperature Controller

Figure 14 shows a way to use the LT1010 to control a fan motor's speed to regulate instrument temperature. The fan employed is one of the new electrostatic types which has very high reliability because it contains no wearing parts. These devices require high voltage drive. When power is applied, the thermistor (located in the fan's exhaust stream) is at a high value. This unbalances the A3 amplifier-driven bridge, A1 receives no power, and the fan does not run. As the instrument enclosure warms, the thermistor value decreases until A3 begins to oscillate. A2 provides isolation and gain and A4 drives the transformer to generate high voltage for the fan. In this fashion, the loop acts to maintain a stable instrument temperature by controlling the fan's exhaust rate. The 100µF time constant across the error amplifier pins is typical of such configurations. Fast time constants will produce audibly annoying "hunting" in the servo. Optimal values for this time constant and gain depend upon the thermal and airflow characteristics of the enclosure being controlled.

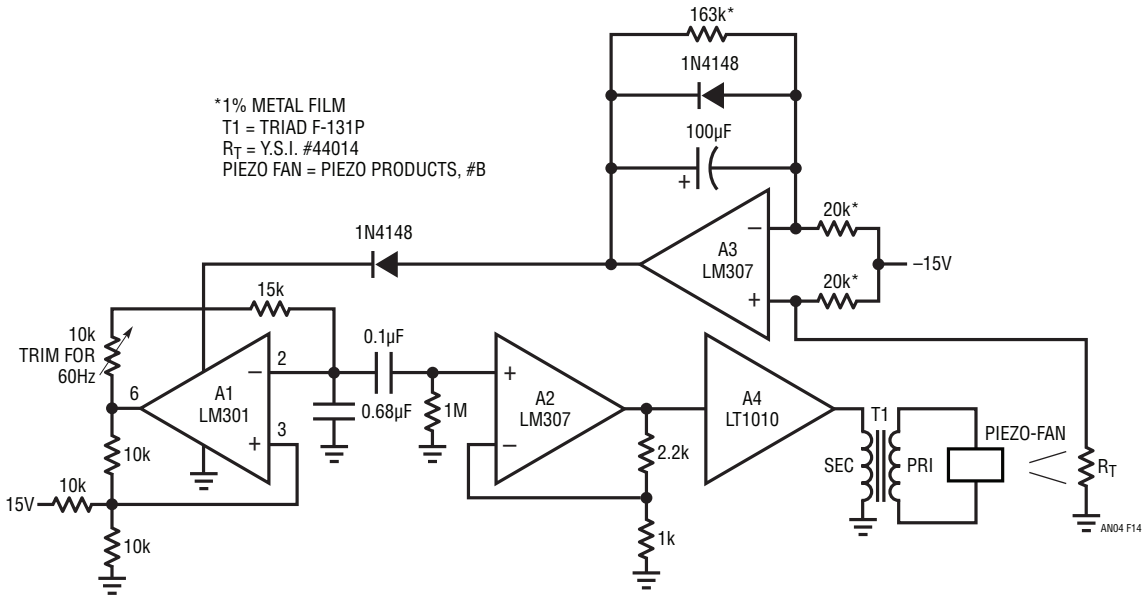


Figure 14. Piezo-Electric Fan Servo

The LT1010 at a Glance

by R. J. Widlar

The schematic describes the basic elements of the buffer design. The op amp drives the output sink transistor, Q3, such that the collector current of the output follower never drops below the quiescent value (determined by I and the area ratio of D1 and D2). As a result, the high frequency response is essentially that of a simple follower, even when Q3 is supplying the load current. The internal feedback loop is isolated from the effects of capacitive loading in the output lead.

The scheme is not perfect in that the rate of rise of sink current is noticeably less than for source current. This can be mitigated by connecting a resistor between the bias terminal at V^+, raising quiescent current. A feature of the final design is that the output resistance is largely independent of the follower quiescent current or the output load current. The output will also swing to the negative rail, which is particularly useful with single supply operation.

The buffer is no more sensitive to supply bypassing than slower op amps as far as stability is concerned. The 0.1µF disc ceramic capacitors usually recommended for op amps are certainly adequate or low frequency work. As always, keeping the capacitor leads short and using a ground plane are prudent, especially when operating at high frequencies.

The buffer slew rate can be reduced by inadequate supply bypass. With output current changes much above 100mA/µs, using 10µF solid tantalum capacitors on both supplies is good practice, although bypassing from the positive to the negative supply may suffice.

When used in conjunction with an op amp and heavily loaded (resistive or capacitive), the buffer can couple into supply leads common to the op amp, causing stability problems with the overall loop. Adequate bypassing can usually be provided by 10µF solid tantalum capacitors. Alternately, smaller capacitors could be used with decoupling resistors. Sometimes the op amp has much better high frequency rejection on one supply, so bypass requirements are less on this supply.

Power Dissipation

In many applications, the LT1010 will require heat sinking. Thermal resistance, junction to still air, is 150°C/W for the TO-39 package and 60°C/W for the TO-3 package. Circulating air, a heat sink or mounting the TO-3 package to a printed circuit board will reduce thermal resistance.

In DC circuits, buffer dissipation is easily computed. In AC circuits, signal wave shape and the nature of the load determine dissipation. Peak dissipation can be several times average with reactive loads. it is particularly important to determine dissipation when driving large load capacitance.

Overload Protection

The LT1010 has both instantaneous current limit and thermal overload protection. Foldback current limiting has not been used, enabling the buffer to drive complex loads without limiting. Because of this, it is capable of power dissipation in excess of its continuous ratings.

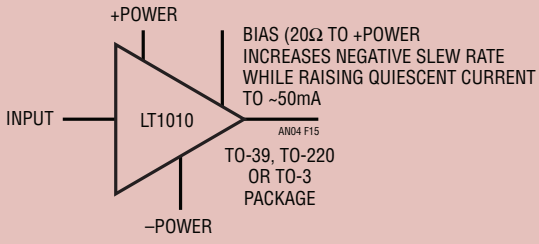
Normally, thermal overload protection will limit dissipation and prevent damage. However, with more than 30V across the conducting output transistor, thermal limiting is not quick enough to ensure protection in current limit. The thermal protection is effective with 40V across the conducting output transistor as long as the load current is otherwise limited to 150mA.

Drive Impedance

When driving capacitive loads, the LT1010 likes to be driven from a low source impedance at high frequencies. Some low power op amps are marginal in this respect. Some care may be required to avoid oscillations, especially at low temperatures.

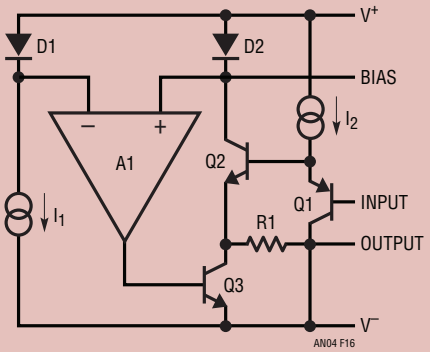
Bypassing the buffer input with more than 200pF will solve the problem. Raising the operating current also works, but this can be done only on the TO-3 package.

The LT1010 at a Glance



15MHz BANDWIDTH
100V/µs SLEW RATE
DRIVE ±10V INTO 75Ω
5mA QUIESCENT CURRENT
DRIVE CAPACITIVE LOADS > 1µF
CURRENT/THERMAL LIMIT
4.5V→40V SUPPLY RANGE

The LT1010 Conceptual Schematic



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