LINEAR TECHNOLOGY

IN THIS ISSUE…

1.2A Buck Converters Draw Only 2.8µA When Regulating Zero Load, Accept 38V$_{IN}$ or 55V$_{IN}$

by John Gardner

Introduction

In modern battery-powered systems, extending battery life and intelligently managing power is paramount. To conserve power, these systems actively switch between idle and active states. The voltage regulators in these systems should be able to do the same. A regulator must also maintain a well-regulated output voltage during low current idle states so it can quickly and automatically adjust to changing load conditions and provide voltage for keep-alive functions.

For example, remote monitoring systems spend most of their time in a low power idle state, but require bursts of high power for transmitting data. Microcontrollers and memory require a regulated voltage, even when idling, to hold state. These types of applications require minimal current consumption in the idle state to maximize battery life, and a seamless transition to active mode when called on to supply several watts of power.

The LT®3971 and LT3991 are ultralow quiescent current monolithic, step-down regulators that maintain high performance at both heavy and light loads. They draw only 1.7µA of quiescent current when in light load situations, but can also source up to

One way to demonstrate the low current performance of the LT3971 is to drive it from a charged bulk input capacitor. A 1000µF capacitor, charged to 16V, is enough for the LT3971 to regulate a 3.3V output with no load for over an hour.

1.2A and include many features of a high performance 1.2A buck regulator, including programmable fixed frequency operation, the ability to be synchronized to an external clock, soft-start, and a shutdown/enable pin. The wide input voltage ranges of these parts—4.3V–38V for the LT3971 and 4.3V–55V for the LT3991—satisfy the requirements of automotive, industrial, and distributed supplies.

Ultralow 1.7µA Quiescent Current in Light Load

When the output load is low, the LT3971 and LT3991 decrease the switching frequency to deliver power to the output only when needed.

LINEAR TECHNOLOGY

Linear in the News…

On the Road in Europe

This quarter, Linear took its message on the road to one of the company's key markets in Europe. On October 15, Linear Technology Executive Chairman Bob Swanson and CEO Lothar Maier met with a dozen electronics magazine editors in Munich, Germany to provide an overview of the company's direction. Editors took advantage of the opportunity to get an update on the state of the business and technology at Linear, asking questions and discussing the company's performance.

Some of the highlights included:

❑ Discussion of Linear's strategy to focus solely on high performance analog products. This laser-like focus enables the company to maintain excellence in this market, build on prior technology developments and deliver value to designers.

❑ An update on the company's repositioning, with increased focus on core markets including industrial, communications infrastructure and automotive, while reducing exposure to consumer and cell phone handset markets.

❑ A report on the recent September quarter, in which Linear grew revenues 14% quarter over quarter in a challenging market environment.

❑ Focus on leveraging internal manufacturing capability to hold product lead times to less than four weeks, much shorter than competitors.

❑ Continuation of Linear's highly successful strategy of providing designers with a broad range of analog products for diverse applications, across North American, European and Asian markets.

Linear Expands Video Channel

Linear continues to expand its library of video design ideas available for download. These are technical presentations on video by Linear's design engineers and applications engineers, presenting solutions to common analog design challenges. To date, there are 18 videos on the Linear Video Channel at www.linear.com/designtools/video/. The video design ideas cover a broad range of topics, including:

❑ "775 Nanovolt Noise Measurement for a Low Noise Voltage Reference" with Jim Williams, Staff Scientist

❑ "IC Current Sources" with Robert Dobkin, Vice President, Engineering and Chief Technical Officer

❑ "The Simple Way to Match to a High Speed ADC Input" with Todd Nelson, Manager, Module Development

❑ "How to Make a Thermocouple Meter with the LTC®2492"with Mark Thoren, Applications Engineering Manager, Mixed Signal Products

Linear is also translating the audio from selected videos into Japanese, Korean, simplified and traditional Chinese subtitles and posting videos on the EE Times Asia web-

sites. Already, four Linear translated Linear videos are running on EE Times Asia sites in China, Taiwan and Korea, and two videos are translated and running on EE Times Japan site.

Linear Enters the Energy Harvesting Market

In the search for improved energy efficiency and new energy sources, a new market is emerging for systems that capture ambient energy from various sources and harvest it to power remote sensors and other systems. This market, known as energy harvesting, has until recently been addressed by cumbersome systems that were expensive and difficult to implement.

There is plenty of ambient energy in the world around us, and the conventional approach for energy harvesting has been through solar panels and wind generators. New harvesting tools allow us to produce electrical energy from a wide variety of ambient sources. For instance thermoelectric generators convert heat to electricity, Piezo elements convert mechanical vibration, photovoltaics convert sunlight and galvanics convert energy from moisture. This makes it possible to power remote sensors, or to charge a storage device, such as a capacitor or thin film battery, so that a microprocessor or transmitter can be powered from a remote location without a local main power source.

Linear's first energy harvesting product, introduced this month, is the LTC3108 ultralow voltage step-up converter and power manager, which is ideal for harvesting and managing surplus energy from extremely low input voltage sources such as thermoelectric generators (TEG), thermopiles and small solar cells. Using a small step-up transformer, the LTC3108 provides a complete power management solution for wireless sensing and data acquisition. Look for other innovative energy harvesting products from Linear Technology in the coming months. *LT*
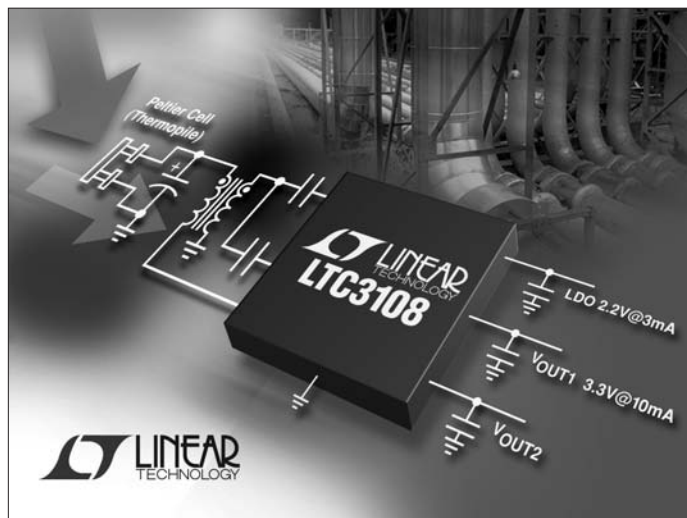
Between current pulses, most of the part's internal circuitry is turned off, to reduce the quiescent current to only 1.7µA. Even with no load current, the feedback resistors and the leakage of the Schottky catch diode act as a load current of a few µA, increasing the quiescent current of the application circuit. By using a few MΩ of feedback divider resistance and a Schottky catch diode with low leakage, only 2.8µA of input current is consumed when regulating a 3.3V output with no load from a 12V input. The application in Figure 1 achieves low input current over the entire input voltage range when regulating a 3.3V output with no load.

One way to demonstrate the low current performance of the LT3971 is to drive the part from a charged bulk input capacitor. Using a 1000µF, 35V electrolytic capacitor, with leakage less than 1µA, charged to 16V, the LT3971 can regulate a 3.3V output with no load for over an hour. The 1000µF capacitor drains at a rate of about 1V every five minutes until the part drops out at an input voltage of 4V. This type of performance shows the LT3971's potential in energy harvesting systems and back-up systems.

Hook It Up and Forget About It

The quiescent current of the LT3971 is exceptionally low even when compared to the self-discharge of a battery. Rechargeable batteries have significant self-discharge. Nickel cadmium (NiCd) batteries lose about 15% to 20% of their charge in a month and nickel metal hydride (NiMH) batteries are even worse. There are several types of low self-discharge NiMH batteries available, such as the SANYO Eneloop, which lose about 15% to 30% of its charge per year. Lead acid batteries discharge several percent of their charge a month and lithium secondary batteries discharge about half as fast.

These discharge rates correspond to over 100µA of self-discharge in the worst case and tens of µA in the best case. Primary batteries have much lower self-discharge rates. Alkaline and lithium primaries can take up to five to fifteen years to lose 20% of their charge. This corresponds to only a few micro-amps of self-discharge current.

Compared to these numbers, the LT3971's quiescent current is over an order of magnitude less than the self-discharge of rechargeable batteries, so the LT3971's impact on battery life is
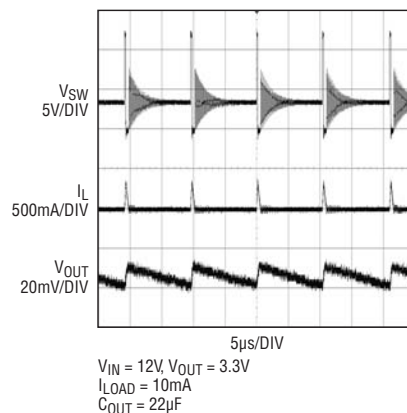
so small, you can hook it up and forget about it. Primary batteries have self-discharge comparable to the LT3971's quiescent current, so the battery only drains about twice as fast as it would if it was just sitting on a shelf.

Less Than 15mV of Output Voltage Ripple

The output voltage ripple of the LT3971 is less than 15mV across the full load range. During light load situations, the regulator enters Burst Mode® operation where single current pulses are used to recharge the output capacitor when the part detects the output voltage has drooped below the regulation value. Single pulse operation is critical to controlling output voltage ripple, because multiple pulses would quickly charge the output capacitor excessively. The peak of each current pulse is set to about 330mA, generating consistent ripple performance across the Burst Mode operation load range. The switching waveforms in Figure 2 show the ripple performance for a 10mA load.

Figure 1. The LT3971 can achieve ultralow input current while regulating a 3.3V output with no load.

Figure 2. During light loads, the output voltage ripple is controlled by single pulse burst mode. For a 12V$_{IN}$ to 3.3V$_{OUT}$ application with 10mA of load, the output voltage ripple is below 15mV with a 22µF output capacitor.
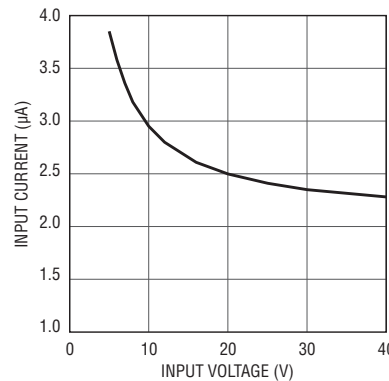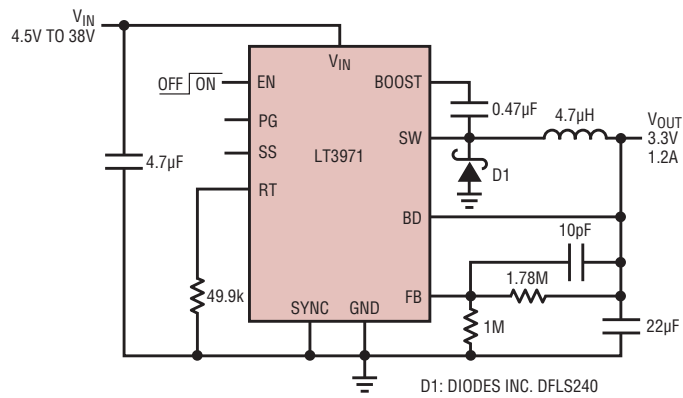
In typical hysteretic Burst Mode implementations, the peak-to-peak voltage of the output ripple is a fixed value. In contrast, with the single pulse Burst Mode implementation used in the LT3971, the output ripple voltage can be adjusted by changing the output capacitance. The peak current of the pulses is independent of the output capacitor size because a single, 330mA pulse is always delivered. The total charge delivered with each switching pulse is constant, so the output voltage ripple in Burst Mode operation can be reduced by increasing the output capacitance. Figure 3 shows how the output ripple in Burst Mode operation decreases proportionally to increases in the output capacitance. The peak current in each switching pulse was set so as to yield less than 15mV of ripple even with a 22µF output capacitor.

Uncompromised Fast Transient Response and Full Feature Set

No compromises were made to achieve the LT3971's low quiescent current. The part has good transient performance and a full feature set. The peak current mode control scheme with internal compensation maintains good stability across load and temperature; the user just has to include a 10pF phase lead capacitor between the output and the FB pin. The response to a 0.5A load step starting from both a 0.5A load and a 25mA load are shown in Figure 4. The regulator displays smooth transitions between Burst
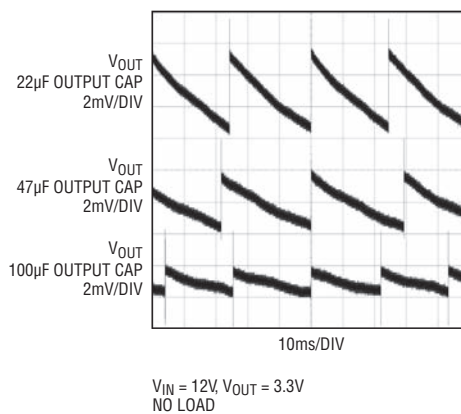

V_{IN} = 12V, V_{OUT} = 3.3V
NO LOAD

Figure 3. Output voltage ripple decreases with increasing capacitor size in burst mode. The output ripple is about 6mV$_{P-P}$ with a 22µF, 4mV$_{P-P}$ with a 47µF, and 2mV$_{P-P}$ with a 100µF output capacitor. A 0.5 inch lead to a 1µF capacitor is used to help filter the ESL spike on the output and care is taken to measure the ripple directly across the capacitor.

FIGURE 1 APPLICATION
V_{IN} = 12V, V_{OUT} = 3.3V
C_{OUT} = 47µF

FIGURE 1 APPLICATION
V_{IN} = 12V, V_{OUT} = 3.3V
C_{OUT} = 47µF
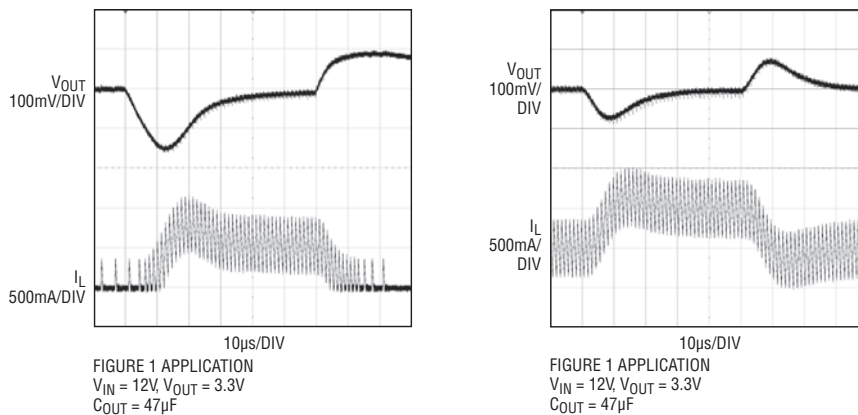
Figure 4. Transient responses for a 25mA to 525mA load step and a 0.5A to 1A load step. The transition between burst mode and full frequency operation is smooth.

Mode operation and full switching frequency.

The LT3971 switching frequency can be programmed between 200kHz and 2MHz with an external resistor. By connecting an external clock to the SYNC pin, the switching frequency can be synchronized as fast as 2MHz. A soft-start feature limits the inrush current of the part by throttling the switch current limit during start-up. The SS pin is actively pulled down
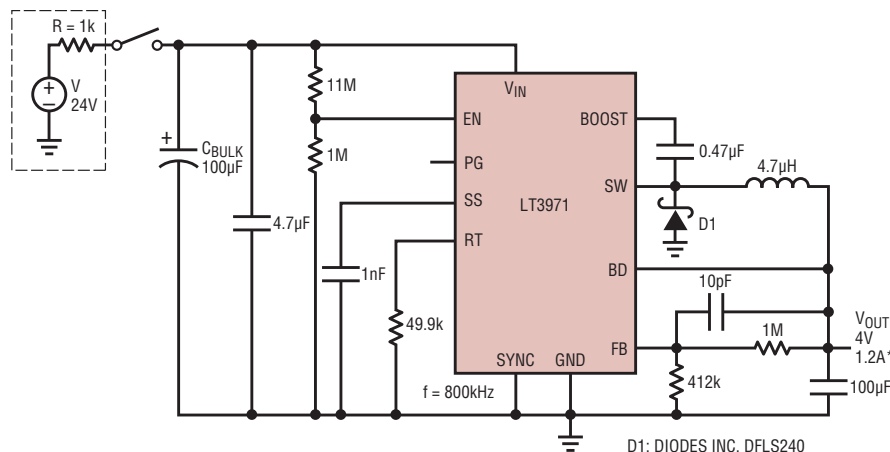
* AVERAGE OUTPUT POWER CANNOT EXCEED THAT WHICH CAN BE PROVIDED BY HIGH IMPEDANCE SOURCE. NAMELY,

$$P_{OUT(MAX)} = \frac{V^2}{4R} \cdot \eta$$

WHERE V IS VOLTAGE OF SOURCE, R IS INTERNAL SOURCE IMPEDANCE, AND η IS LT3971 EFFICIENCY. MAXIMUM OUTPUT CURRENT OF 1.2A CAN BE SUPPLIED FOR A SHORT TIME BASED ON THE ENERGY WHICH CAN BE SOURCED BY THE BULK INPUT CAPACITANCE.

Figure 5. A LT3971 application circuit where the 1MΩ and 11MΩ resistor divider sets a 12V input voltage enable threshold to prevent the 24V, 1kΩ impedance source from collapsing.

Figure 6. As the output charges to 4V on start-up, the 12V V$_{IN(EN)}$ threshold temporarily shuts down the part to prevent the high impedance input source from collapsing.

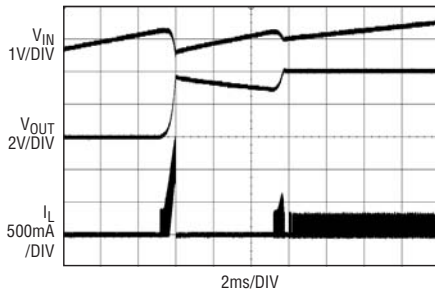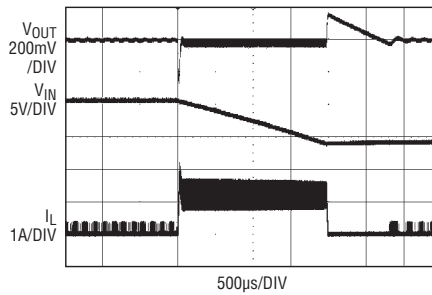**Figure 7. Even though the high impedance source can not provide the power to supply 1.2A to the output, energy from the bulk input capacitance can supply brief high current output pulses.**

when the EN pin is low. Then a 1µA current source into an external capacitor connected to the SS pin sets the soft-start ramp rate when the part starts-up. The LT3971 comes in a 10-pin MSOP package or a 10-pin 3mm × 3mm DFN package. Both package types have an exposed pad that provides lower thermal resistance and a ground connection.

Accurate Enable Pin

The quiescent current of the LT3971 is so low that in shutdown mode the internal bandgap reference can still operate, consuming only 700nA of input current. This allows an accurate 1V enable pin threshold when V$_{IN}$ is above 4.3V. When the enable pin is above 1V, the part is enabled and can switch, and when the enable pin is below 1V, the part is shutdown and cannot switch.

The accurate enable pin threshold can be used to program an input voltage enable threshold (V$_{IN(EN)}$) by connecting a simple resistor divider

between V$_{IN}$ and EN. When the input voltage is greater than the V$_{IN(EN)}$ threshold the LT3971 regulates the output voltage, and when the input voltage is below the V$_{IN(EN)}$ threshold the part stops regulating the output voltage.

High Impedance Input Source

A programmable input voltage enable threshold is very useful when driving the LT3971 with a high impedance input source. These types of sources could be distributed supplies, lines used for both power and signaling, or types of energy harvesting devices. A buck regulator draws constant power from the input, thus appearing to the input as a negative impedance. When the converter starts to draw current from a high impedance source, the voltage at the input pin starts to drop, and the converter then draws even more current. If the regulator draws more power than the input supply can provide, for example during start-up when the output capacitor is being

charged, than the converter can collapse the input supply. An input voltage enable threshold solves this problem by shutting the part down when the input voltage collapses to the V$_{IN(EN)}$ threshold. Figure 5 shows an application where the LT3971 is being driven by a 24V source with a 1kΩ series resistance. The 1MΩ and 11MΩ resistor divider sets a 12V V$_{IN(EN)}$ threshold on the input. As the output capacitor charges to its regulation value of 4V, the V$_{IN(EN)}$ threshold prevents the input voltage from collapsing below 12V, as seen in Figure 6.

The output cannot, *on average*, draw more power than the input can supply with its high impedance. However, the LT3971 can source up to the 1.2A maximum output current for a brief time, as long as the energy is supplied by the input capacitance. Figure 7 shows 1.2A of output current being supplied for 2ms from the 100µF bulk input capacitance. The ability of the LT3971 to supply this type of pulsed load is very important for satisfying low duty cycle sensor applications and energy harvesting applications, which take advantage of both the low quiescent current performance and 1.2A maximum load of the LT3971.

LT3991 48V to 3.3V 300kHz Application

The LT3991 has the same low quiescent current performance and 1.2A maximum output current as the LT3971, but can operate with input voltages up to 55V. It also includes soft-start
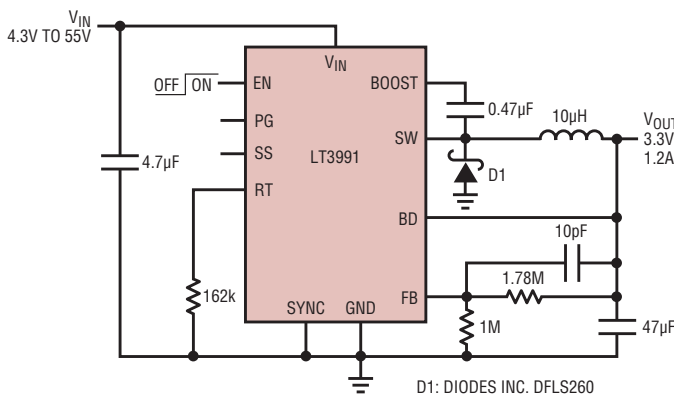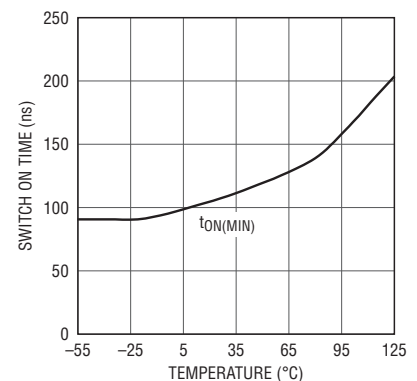
Figure 8. The low minimum switch on time of the LT3991 allows the high step-down ratio, 48V$_{IN}$ to 3.3V$_{OUT}$, at 300kHz switching frequency. This yields a small solution size with a 10µH inductor and a 47µF ceramic output capacitor.

775 Nanovolt Noise Measurement for a Low Noise Voltage Reference
Quantifying Silence

by Jim Williams

Introduction

Frequently, voltage reference stability and noise define measurement limits in instrumentation systems. In particular, reference noise often sets stable resolution limits.

Reference voltages have decreased with the continuing drop in system power supply voltages, making reference noise increasingly important. The compressed signal processing range mandates a commensurate reduction in reference noise to maintain resolution. Noise ultimately translates into quantization uncertainty in ADCs, introducing jitter in applications such as scales, inertial navigation systems, infrared thermography, DVMs and medical imaging apparatus.

A new low voltage reference, the LTC6655, has only 0.3ppm (775nV) noise at $2.5V_{OUT}$. Table 1 lists salient specifications in tabular form. Accuracy and temperature coefficient are characteristic of high grade, low voltage references. 0.1Hz to 10Hz noise, particularly noteworthy, is unequalled by any low voltage electronic reference.

Noise Measurement

Special techniques are required to verify the LTC6655's extremely low noise. Figure 1's approach appears innocently straightforward but practical
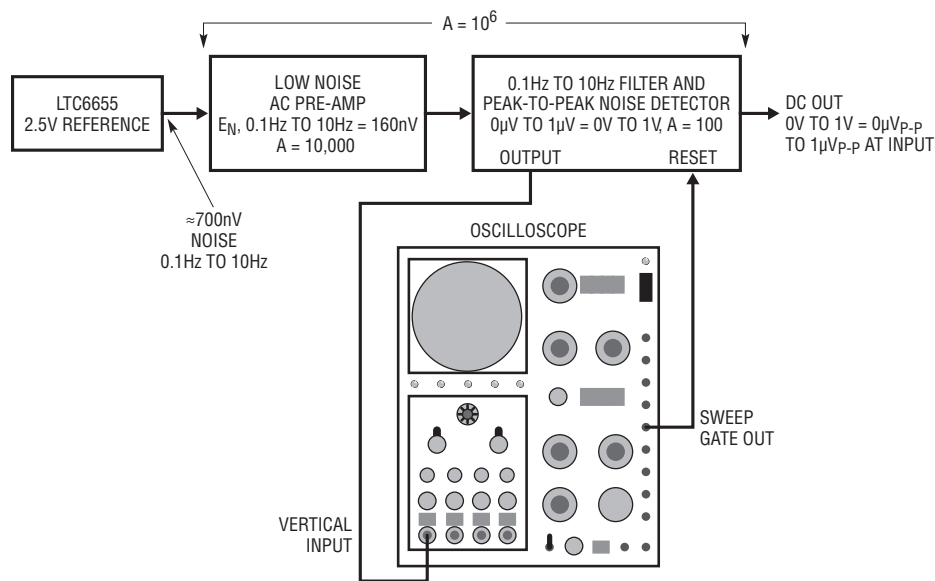

Figure 1. Conceptual 0.1Hz to 10Hz noise testing scheme includes low noise preamplifier, filter and peak-to-peak noise detector. Pre-amplifier's 160nV noise floor, enabling accurate measurement, requires special design and layout techniques.

implementation represents a high order difficulty measurement. This 0.1Hz to 10Hz noise testing scheme includes a low noise preamplifier, filters and a peak-to-peak noise detector. The pre-amplifiers 160nV noise floor, enabling accurate measurement, requires special design and layout techniques. A forward gain of 10^6 permits readout by conventional instruments.

Figure 2's detailed schematic reveals some considerations required to achieve the 160nV noise floor. The references' DC potential is stripped by the 1300µF, 1.2k resistor combination; AC content is fed to Q1. Q1-Q2, extraordinarily low noise JFETs, are DC stabilized by A1, with A2 providing a single-ended output. Resistive feedback from A2 stabilizes the configuration at a gain of 10,000. A2's

Table 1. LTC6655 reference tabular specifications. The LTC6655 accuracy and temperature coefficient are characteristic of high grade, low voltage references. 0.1Hz to 10Hz noise, particularly noteworthy, is unequalled by any low voltage electronic reference.

SPECIFICATION	LIMITS
Output Voltages	1.250, 2.048, 2.500, 3.000, 3.300, 4.096, 5.000
Initial Accuracy	0.025%, 0.05%
Temperature Coefficient	2ppm/°C, 5ppm/°C
0.1Hz to 10Hz Noise	0.775µV at V_{OUT} = 2.500V, Peak-to-Peak Noise is within this Figure in 90% of 1000 10-Second Measurement Intervals
Additional Characteristics	5ppm/V Line Regulation, 500mV Dropout, Shutdown Pin, I_{SUPPLY} = 5mA, $V_{IN} = V_O$ + 0.5V to $13.2V_{MAX}$, $I_{OUT(SINK/SOURCE)}$ = ±5mA, $I_{SHORT-CIRCUIT}$ = 15mA.

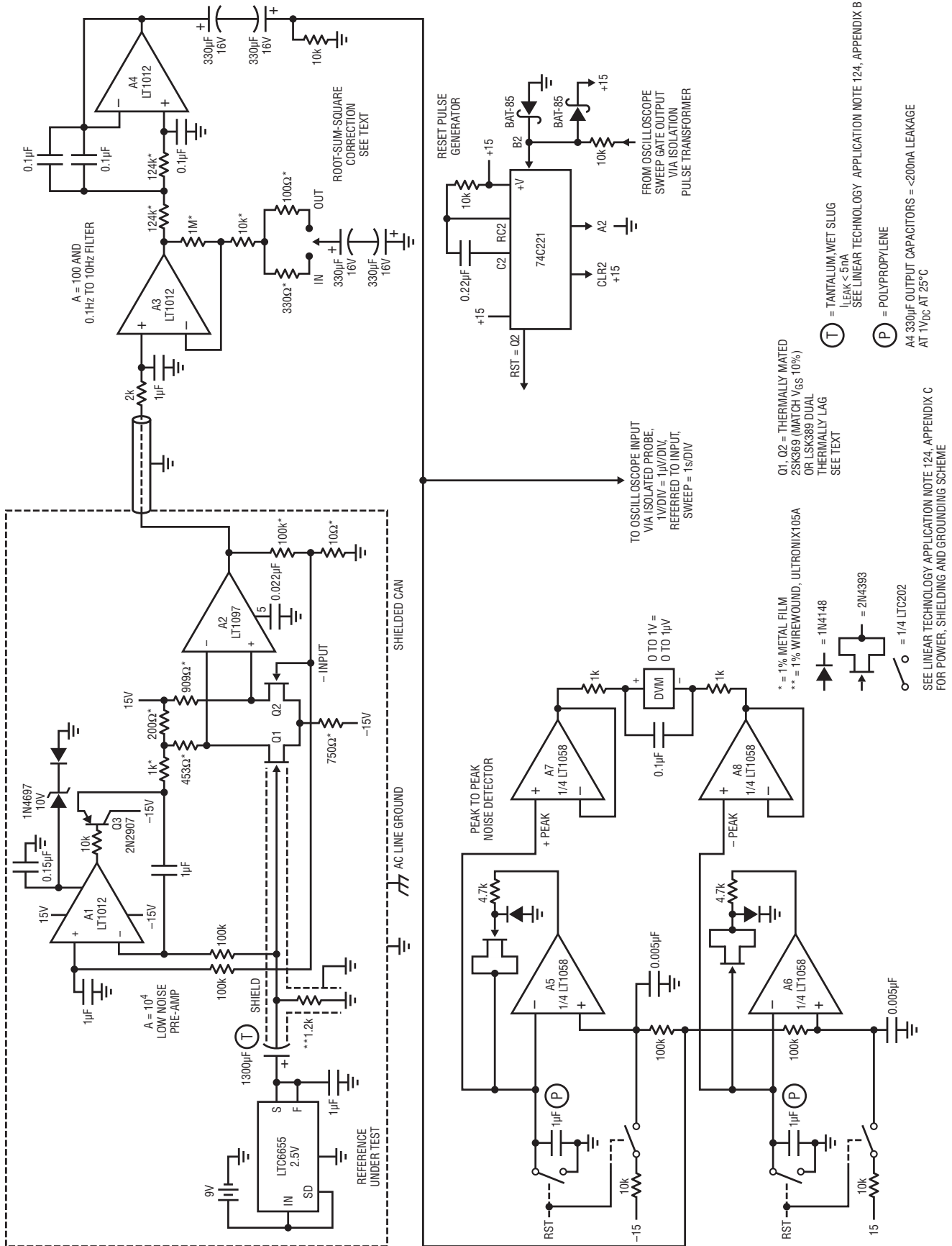**Figure 2. Detailed noise test circuitry. Thermally lagged Q1-Q2 low noise JFET pair is DC stabilized by A1-Q3; A2 delivers A = 10,000; A2 delivers A = 10,000 preamplifier output. A3-A4 form 0.1Hz to 10Hz, A = 100, bandpass filter; total gain referred to pre-amplifier input is 10⁶. Peak-to-peak noise detector, reset by monitoring oscilloscope sweep gate, supplies DVM output.**
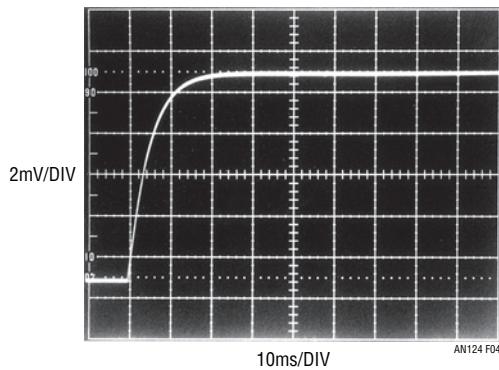
Figure 3. Preamplifier rise time measures 10ms; indicated 35Hz bandwidth ensures entire 0.1Hz to 10Hz noise spectrum is supplied to succeeding filter stage.

Figure 4. Waveforms for peak-to-peak noise detector include A3 input noise signal (trace A), A7 (trace B) positive/A8 (trace C) negative peak detector outputs and DVM differential input (trace D). Trace E's oscilloscope supplied reset pulse lengthened for photographic clarity.

output is routed to amplifier-filter A3-A4 which provides 0.1Hz to 10Hz response at a gain of 100. A5-A8 comprise a peak-to-peak noise detector read out by a DVM at a scale factor of 1 volt/microvolt. The peak-to-peak noise detector provides high accuracy measurement, eliminating tedious interpretation of an oscilloscope display. Instantaneous noise value is supplied by the indicated output to a monitoring oscilloscope. The 74C221 one-shot, triggered by the oscilloscope sweep gate, resets the peak-to-peak noise detector at the end of each oscilloscope 10-second sweep.

Numerous details contribute to the circuit's performance. The 1300µF capacitor, a highly specialized type, is selected for leakage in accordance with the procedure given in Appendix B. Furthermore, it, and its associ-

ated low noise 1.2k resistor, are fully shielded against pick-up. FETs Q1 and Q2 differentially feed A2, forming a simple low noise op amp. Feedback, provided by the 100k-10Ω pair, sets closed loop gain at 10,000. Although Q1 and Q2 have extraordinarily low noise characteristics, their offset and drift are uncontrolled. A1 corrects these deficiencies by adjusting Q1's channel current via Q3 to minimize the Q1-Q2 input difference. Q1's skewed drain values ensure that A1 is able to capture the offset. A1 and Q3 supply whatever current is required into Q1's channel to force offset within about 30µV. The FETs' V_{GS} can vary over a 4:1 range. Because of this, they must be selected for 10% V_{GS} matching. This matching allows A1 to capture the offset without introducing significant noise. Q1 and Q2 are thermally

mated and lagged in epoxy at a time constant much greater than A1's DC stabilizing loop roll-off, preventing offset instability and hunting. The entire A1-Q1-Q2-A2 assembly and the reference under test are completely enclosed within a shielded can.[1] The reference is powered by a 9V battery to minimize noise and insure freedom from ground loops.

Peak-to-peak detector design considerations include JFETs used as peak trapping diodes to obtain lower leakage than afforded by conventional diodes. Diodes at the FET gates clamp reverse voltage, further minimizing leakage.[2] The peak storage capacitors highly asymmetric charge-discharge profile necessitates the low dielectric absorption polypropelene capacitors specified.[3] Oscilloscope connections via galvanically isolated links prevent
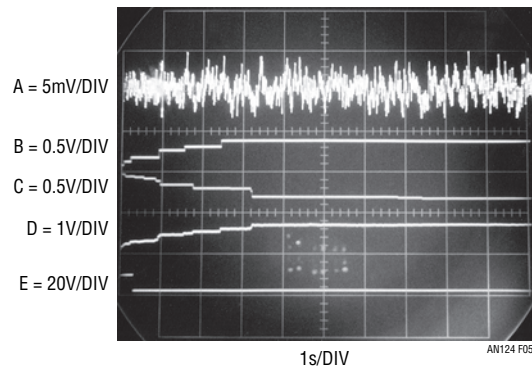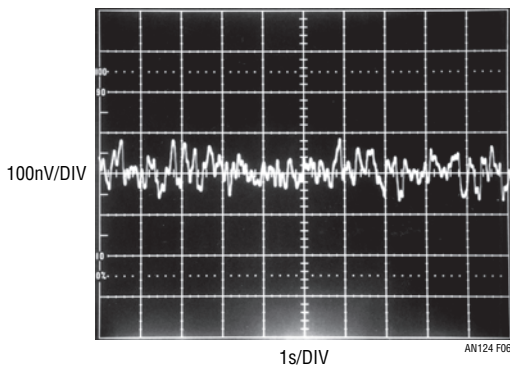
Figure 5. Low noise circuit/layout techniques yield 160nV 0.1Hz to 10Hz noise floor, ensuring accurate measurement. Photograph taken at Figure 3's oscilloscope output with 3V battery replacing LTC6655 reference. noise floor adds ≈2% error to expected LTC6655 noise figure due to root-sum-square noise addition characteristic; correction is implemented at Figure 2's A3.
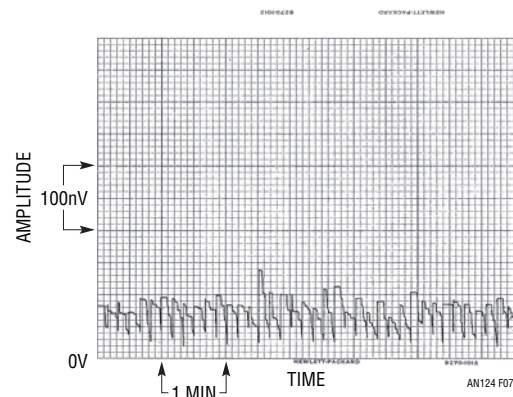
Figure 6. Peak-to-peak noise detector output observed over six minutes shows <160nv test circuit noise. Resets occur every 10 seconds. 3V battery biases input capacitor, replacing LTC6655 for this test.
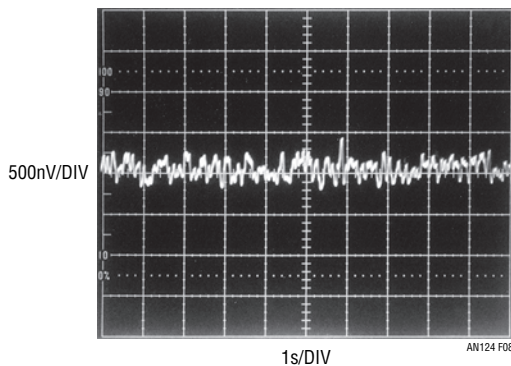
Figure 7. LTC6655 0.1Hz to 10Hz noise measures 775nV in 10-second sample time.

ground loop induced corruption. The oscilloscope input signal is supplied by an isolated probe; the sweep gate output is interfaced with an isolation pulse transformer. For more details, see Linear Technology Application Note 124, Appendix C.

Noise Measurement Circuit Performance

Circuit performance must be characterized prior to measuring LTC6655 noise. The preamplifier stage is verified for >10Hz bandwidth by applying a 1µV step at its input (reference disconnected) and monitoring A2's output. Figure 3's 10ms rise time indicates 35Hz response, insuring the entire 0.1Hz to 10Hz noise spectrum is supplied to the succeeding filter stage.

Figure 4 describes peak-to-peak noise detector operation. Waveforms include A3's input noise signal (Trace A), A7 (Trace B) positive/A8 (Trace C) negative peak detector outputs and

DVM differential input (Trace D). Trace E's oscilloscope supplied reset pulse has been lengthened for photographic clarity.

Circuit noise floor is measured by replacing the LTC6655 with a 3V battery stack. Dielectric absorption effects in the large input capacitor require a 24-hour settling period before measurement. Figure 5, taken at the circuit's oscilloscope output, shows 160nV 0.1Hz to 10Hz noise in a 10 second sample window. Because noise adds in root-sum-square fashion, this represents about a 2% error in the LTC6655's expected 775nV noise figure. This term is accounted for by placing Figure 2's "root-sum-square correction" switch in the appropriate position during reference testing. The resultant 2% gain attenuation first order corrects LTC6655 output noise reading for the circuit's 160nV noise floor contribution. Figure 6, a strip-chart recording of the peak-to-

peak noise detector output over six minutes, shows less than 160nV test circuit noise.[4] Resets occur every 10 seconds. A 3V battery biases the input capacitor, replacing the LTC6655 for this test.

Figure 7 is LTC6655 noise after the indicated 24-hour dielectric absorption soak time. Noise is within 775nV peak-to-peak in this 10 second sample window with the root-sum-square correction enabled. The verified, extremely low circuit noise floor makes it highly likely this data is valid. In closing, it is worth mention that the approach taken is applicable to measuring any 0.1Hz to 10Hz noise source, although the root-sum-square error correction coefficient should be re-established for any given noise level. ⊿⊤

Notes

[1] The preamplifier structure must be carefully prepared. See Appendix A in Linear Technology Application Note 124, "Mechanical and Layout Considerations," for detail on preamplifier construction.

[2] Diode-connected JFETs' superior leakage derives from their extremely small area gate-channel junction. In general, JFETs leak a few picoamperes (25°C) while common signal diodes (e.g. 1N4148) are about 1,000× worse (units of nanoamperes at 25°C).

[3] Teflon and polystyrene dielectrics are even better but the Real World intrudes. Teflon is expensive and excessively large at 1µF. Analog types mourn the imminent passing of the polystyrene era as the sole manufacturer of polystyrene film has ceased production.

[4] That's right, a *strip-chart recording.* Stubborn, locally based aberrants persist in their use of such archaic devices, forsaking more modern alternatives. Technical advantage could account for this choice, although deeply seated cultural bias may be indicated.

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and external clock synchronization features, and comes in a 10-pin MSOP or 3mm × 3mm DFN package, both with an exposed ground pad.

The LT3991 has a typical minimum switch on time of 110ns at room and 150ns at 85°C, which allow higher switching frequencies for large stepdown ratios when compared to other parts with similar high input voltage ratings. Figure 8 shows a 48V input to a 3.3V output application with a switching frequency of 300kHz. The 10µH inductor and 47µF output capacitor yield a small overall solution

size. The output capacitor can be a small ceramic capacitor, as opposed to a tantalum capacitor, because the LT3991 does not need any output capacitor ESR for stability.

Conclusion

The LT3971 and LT3991 are ultralow quiescent current regulators that can regulate a 12V input to a 3.3V output during no load conditions with only 2.8µA of input current. Light load operation with single current pulses keeps the output voltage ripple to less than 15mV. These buck regulators can also provide up to 1.2A of output

current. The LT3971 and LT3991 are well suited for keep-alive and remote monitoring systems with low duty cycle, high current, pulsed outputs. The wide input range from 4.3V up to 38V for the LT3971, and 55V for the LT3991, along with the programmable input voltage enable threshold feature, allow these converters to be driven from a wide range of input sources. The ultralow quiescent current performance of the LT3971 and LT3991 make them great choices for battery-operated systems where power conservation is critical. ⊿⊤

Monolithic Synchronous Step-Down Regulator Sources 3A or Sinks 1.5A in TSSOP or 3mm × 4mm QFN

by Genesia Bertelle

Introduction

The LTC3612 monolithic synchronous buck regulator can source 3A and sink 1.5A from a tiny 3mm × 4mm QFN or 20-lead TSSOP package with exposed pads for improved thermal performance. This device saves space, minimizes external components and is highly efficient. It employs a constant frequency, current mode architecture that operates from an input range of 2.25V to 5.5V—suitable for a single Li-Ion battery or low voltage input applications. The LTC3612 provides an adjustable regulated output down to 0.6V.

The LTC3612 uses Burst Mode® operation to increase efficiency at light loads, consuming less than 100µA of supply current at no load. Adjustable compensation allows the transient response to be optimized over a wide range of loads and output capacitors. The internal synchronous switch increases efficiency and eliminates the need for an external catch diode, saving external components and board space.

Design Versatility

Depending on the application requirements, a designer can either prioritize light load efficiency or minimize supply noise by choosing from three light load operating modes: Burst Mode operation, pulse-skipping, or forced continuous modes. Burst Mode operation provides high efficiency over the entire load range by reducing gate charge losses at light loads. Burst Mode operation is an efficient solution for low current applications, but in some applications noise suppression is a higher priority. Forced continuous operation, though not as efficient as Burst Mode operation at light loads, maintains a constant switching frequency, making it easier to reduce
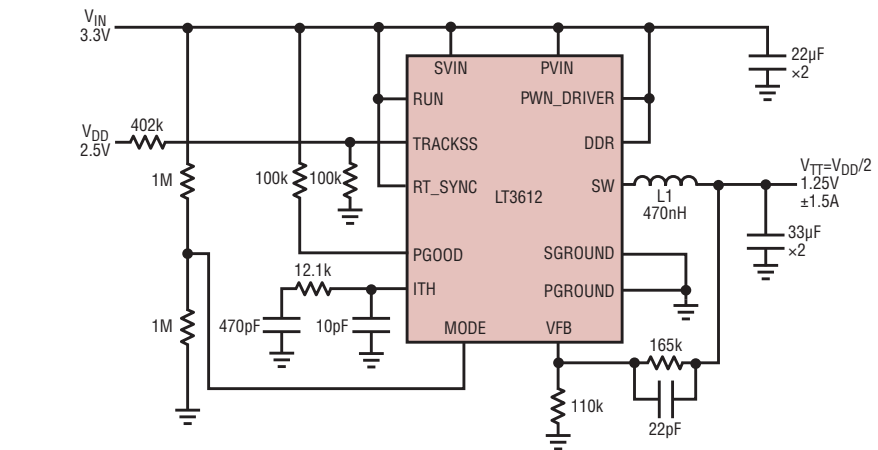

Figure 1. High efficiency and very compact 1.5A LTC3612 V_{TT} power supply with 3.3V input

noise and RF interference. In forced continuous operation, the LTC3612 can source and sink current. Pulse-skipping mode is similar to Burst Mode operation. It reduces output voltage ripple, but incurs more gate charge losses, compromising light load efficiency. Although not as efficient as Burst Mode operation at low currents, pulse-skipping mode still provides high efficiency for moderate loads.

The default frequency of 2.25MHz is chosen by tying the RT/SYNC pin to V_{IN}. This high frequency allows the use of tiny inductors and ceramic output

Figure 2. Efficiency vs load current, 2.25MHz switching frequency, in various operating modes

capacitors without compromising efficiency. The switching frequency can be set from 300kHz to 4MHz with an external resistor or synchronized to an external clock, where each switching cycle begins at the falling edge of the external clock signal. All operating modes (Burst Mode operation, pulse-skipping and forced continuous mode) can be selected in combination with the default 2.25MHz frequency, a frequency defined by an external resistor or synchronization with external clock.

The LTC3612 offers a power good indicator (PGOOD pin), which monitors the output voltage. The PGOOD pin is an open-drain output which is pulled down to ground during shut down, start-up and while the output voltage is outside the power good voltage window (±7.5% of the final programmed output voltage). If the output voltage stays inside the power good window for more than 100µs, the PGOOD pin is released. If the output voltage remains outside the power good window for more than 100µs, the PGOOD pin is pulled down.

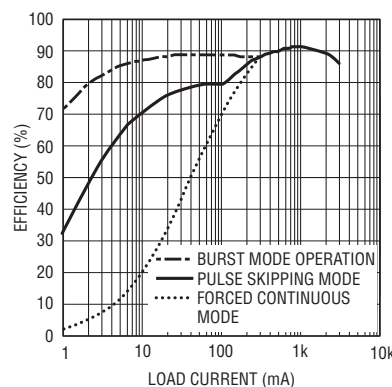The 100% duty cycle capability for low dropout conditions allows maxi-

V_OUT 200mV/DIV

I_L 1A/DIV

50µs/DIV

V_OUT = 1.8V
I_LOAD = 100mA TO 3A
V_MODE = 1.5V

V_OUT 100mV/DIV

I_L 1A/DIV

50µs/DIV

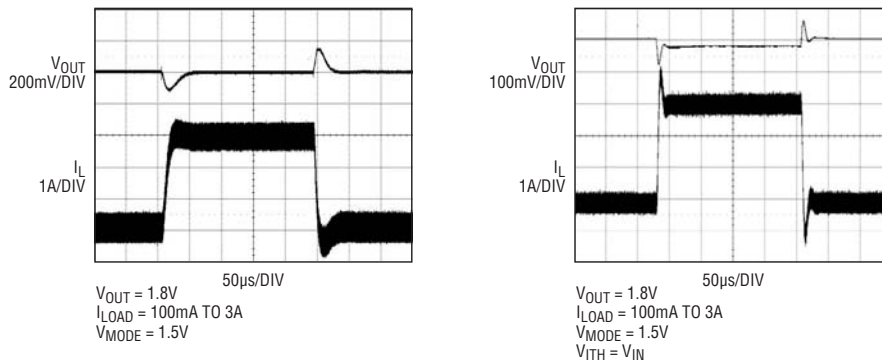V_OUT = 1.8V
I_LOAD = 100mA TO 3A
V_MODE = 1.5V
V_ITH = V_IN

Figure 3. Load step transient in forced continuous mode

mum energy to be extracted from a Li-Ion battery. In dropout, the output voltage is determined by the input voltage minus the voltage drop across the internal P-channel MOSFET (only 70mΩ) and the inductor resistance.

Power Supply Tracking and DDR Applications

The LTC3612 supports coincidental or ratiometric ramp-up and ramp-down tracking of another supply via the TRACK/SS pin. For TRACK/SS voltages lower than 0.2V, the switching frequency is reduced to ensure that the minimum duty cycle limit does not prevent the output voltage from following the TRACK/SS pin.

Start-up behavior can be programmed in one of three ways via the TRACK/SS pin. Tying TRACK/SS to SVIN selects the internal soft-start circuit (1ms ramp time). Alternately, external soft-start timing can be programmed with a TRACK/SS capacitor to ground and a resistor to SVIN. Finally, the TRACK/SS pin can be used to force the LTC3612 to track the start-up behavior of another supply.

When running in DDR mode, the TRACK/SS pin can be used as an external reference input, allowing the

LTC3612 to power DDR memory. In this mode, the power good window moves in relation to the actual TRACK/SS pin voltage.

Typically DDR memory needs at least two main power supplies: V_{DD} and V_{TT}, where V_{TT} must always track the V_{DD} supply with $V_{TT} = V_{DD}/2$. Since the termination resistors can carry current in either direction, the V_{TT} power supply must be able to both source and sink current while tracking the V_{DD} supply.

Two LTC3612 converters can be used to generate both V_{DD} and V_{TT}, as shown in the circuit in Figure 1. V_{TT} voltages range from 1.25V down to 0.75V for different DDR standards. LTC3612 can be used for all DDR standards because the TRACK/SS voltage can accept a reference voltage from 0.6V down to 0.3V (although TRACK/SS voltage values from 0.4V to 0.5V are the most accurate).

Optional AVP Mode with Internal Compensation

Fast load current transient response is an important feature in microprocessor power supplies. Normally, several capacitors in parallel are required to meet microprocessor transient re-

quirements, where capacitor ESR and ESL primarily determine the amount of droop or overshoot in the output voltage. If a load step with very fast slew rate occurs, an output voltage excursion is seen for transients in both directions: that is for full load to minimum load and for the minimum load to full load.

If the ITH pin is tied to SVIN, the active voltage positioning (AVP) mode and internal compensation are selected. AVP mode intentionally compromises output voltage regulation by reducing the gain of the feedback circuit, resulting in an output voltage that varies with load current.

When the load current suddenly increases, the output voltage starts from a level slightly higher than nominal so the output voltage can droop and stay within the specified voltage range. When the load current suddenly decreases the output voltage starts at a level lower than nominal so the output voltage can overshoot and stay within the specified voltage range. In AVP mode the external compensation at ITH pin is not needed, reducing external components.

Short-Circuit Protection

The LTC3612 is protected against an output short to ground. When the output is shorted to ground, the inductor current decays very slowly during a single switching cycle. The LTC3612 uses two techniques to prevent inductor current runaway from occurring.

First, if the output voltage drops below 50% of its nominal value, the peak current clamp is decreased, reducing the maximum inductor current. When the output voltage reaches 0V, the clamp voltage at the ITH pin drops to 40% of the clamp voltage during normal operation. The short-circuit peak inductor current is determined by the minimum on-time of the LTC3612, the input voltage and the inductor value. This foldback behavior helps in limiting the peak inductor current when the output is shorted to ground.

Secondly, a limit is also imposed on the valley inductor current. If the

V_OUT 200mV/DIV

I_LOAD 1A/DIV

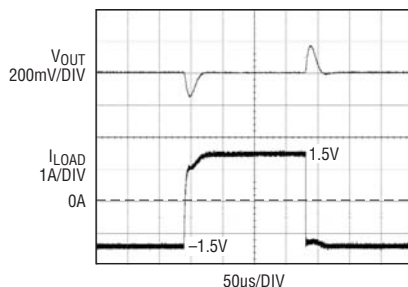0A

1.5V

−1.5V

50µs/DIV

Figure 4. Load transient response for ±1.5A load applied to the circuit shown in Figure 1
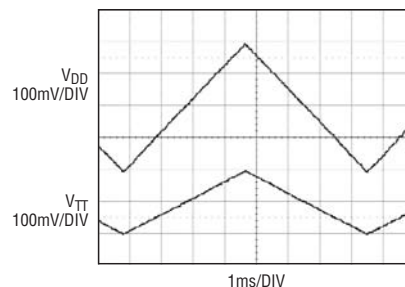

V_DD 100mV/DIV

V_TT 100mV/DIV

1ms/DIV

Figure 5. V_{TT} responding to a change in V_{DD} for the circuit shown in Figure 1

Designing a Solar Cell Battery Charger

by Jim Drew

Introduction

The market for portable solar powered electronic devices continues to grow as consumers look for ways to reduce energy consumption and spend more time outdoors. Because solar power is a variable and unreliable, nearly all solar-powered devices feature rechargeable batteries. The goal is to extract as much solar power as possible to charge the batteries quickly and maintain the charge.

Solar cells are inherently inefficient devices, but they do have a point of maximum power output, so operating at that point seems an obvious design goal. The problem is that the IV characteristic of maximum output power changes with illumination. A monocrystalline solar cell's output current is proportional to light intensity, while its voltage at maximum power output is relatively constant (see Figure 1). Maximum power output for a given light intensity occurs at the knee of each curve, where the cell transitions from a constant voltage device to a constant current device. A charger design that efficiently extracts power from a solar panel must be able to steer the panel's output voltage to the point of maximum power when illumination levels cannot support the charger's full power requirements.

The LT3652 is a multi-chemistry 2A battery charger designed for solar power applications. The LT3652 employs an input voltage regulation loop that reduces the charge current if the input voltage falls below a programmed level set by a simple voltage divider network. When powered by a solar panel, the input voltage regulation loop is used to maintain the panel at near peak power output.

LT3652 Input Voltage Regulation Loop

The input voltage regulation loop of the LT3652 acts over a specific input voltage range. When V_{IN}, as measured via a resistor divider at the V_{IN_REG} pin, falls
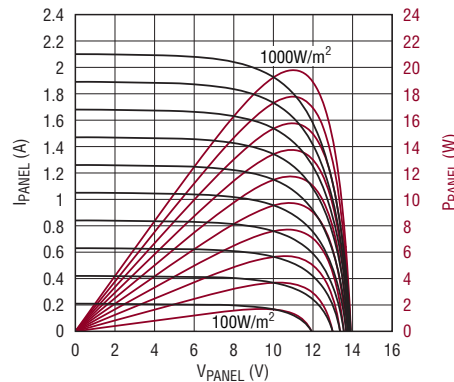

Figure 1. A solar cell produces current in proportion to the amount of sunlight falling on it, while the cell's open-circuit voltage remains relatively constant. Maximum power output occurs at the knee of each curve, where the cell transitions from a constant voltage device to a constant current device, as shown by the power curves.

below a certain set point, the charge current is reduced. The charging current is adjusted via a control voltage across a current sensing resistor in series with the inductor of the buck regulator charging circuit. Decreased illumination (and/or increased charge current demands) can both cause the input voltage (panel voltage) to fall, pushing the panel away from its point of maximum power output. With the LT3652, when the input voltage falls below a certain set point, as defined by the resistor divider connected between the V_{IN} and V_{IN_REG} pins, the current control voltage is reduced, thus reducing the charging current. This action causes the voltage from the solar panel

to increase along its characteristic VI curve until a new peak power operating point is found.

If the solar panel is illuminated enough to provide more power than is required by the LT3652 charging circuit, the voltage from the solar panel increases beyond the control range of the voltage regulation loop, the charging current is set to its maximum value and a new operation point is found based entirely on the maximum charging current for the battery's point in the charge cycle.

If the electronic device is operating directly from solar power and the input voltage is above the minimum level of the input voltage regulation
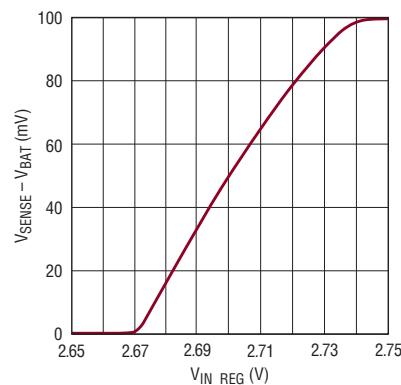

Figure 2. Charger current control voltage ($V_{SENSE} - V_{BAT}$) vs proportional input voltage, as measured via voltage divider at V_{IN_REG} pin. V_{IN} (solar panel voltage) only affects charging current when V_{IN_REG} is between 2.67V and 2.74V. In this range, the charger will reduce the charging current if necessary to run the panel at peak power output.

loop's control range, the excess power available is used to charge the battery at a lower charging rate. The power from the solar panel is adjusted to its maximum operating power point for the intensity level.

Figure 2 shows a typical V_{IN_REG} control characteristic curve. As the voltage on the V_{IN_REG} pin increases beyond 2.67V, the voltage $V_{SENSE} - V_{BAT}$, across the current sensing resistor, increases until it reaches a maximum of 100mV, when V_{IN_REG} is above 2.74V. As V_{IN_REG} increases further, $V_{SENSE} - V_{BAT}$ remains at 100mV. The expression for the input voltage control range is:

$$\frac{2.67 \bullet (R_{IN1} + R_{IN2})}{R_{IN2}}$$

$$< V_{IN} \text{ CONTROL RANGE } < \qquad \text{Eq.1}$$

$$\frac{2.74 \bullet (R_{IN1} + R_{IN2})}{R_{IN2}}$$

If we linearize the portion of the curve in Figure 2 for V_{IN_REG} between 2.67V and 2.74V, the following expression describes the current sensing voltage $V_{SENSE} - V_{BAT}$:

$$V_{SENSE} - V_{BAT} =$$
$$1.43 \bullet (V_{IN\_REG} - 2.67V) \qquad \text{Eq.2}$$

$$V_{SENSE} - V_{BAT} =$$
$$1.43 \bullet \left(\frac{V_{IN} \bullet R_{IN2}}{R_{IN1} + R_{IN2}} - 2.67V \right) \qquad \text{Eq.3}$$

The charging current for the battery would then be:

$$I_{CHARGE} =$$
$$\frac{1.43}{R_{SENSE}} \bullet \left(\frac{V_{IN} \bullet R_{IN2}}{R_{IN1} + R_{IN2}} - 2.67V \right) \qquad \text{Eq.4}$$

Since the charging circuit of the LT3652 is a current controlled buck regulator, the input current relates to the charging current by the following expression:

$$I_{IN} = I_{CHARGE} \bullet \frac{V_{BAT}}{\eta \bullet V_{IN}} \qquad \text{Eq. 5}$$

where η is the efficiency of the charger

The input power can now be determined by combining Equations 4 and 5 with the input voltage, resulting in the following:

$$P_{IN} =$$
$$\frac{1.43 \bullet V_{BAT}}{R_{SENSE} \bullet \eta} \bullet \left(\frac{V_{IN} \bullet R_{IN2}}{R_{IN1} + R_{IN2}} - 2.67V \right) \qquad \text{Eq. 6}$$

Once R_{SENSE} is selected for the maximum charging current and R_{IN1} and R_{IN2} are determined to select the input voltage current control range, Equation 6 can be plotted against the solar panels power curves to determine the charger's operating point for various battery voltages. An example follows.

Design Example

Figure 3 shows a 2A, solar powered, 2-cell Li-Ion battery charger using the LT3652.

First step is to determine the minimum requirements for the solar panel. Important parameters include the open circuit voltage, V_{OC}, peak power voltage, $V_{P(MAX)}$, and peak power current, $I_{P(MAX)}$. The short circuit current, I_{SC}, of the solar panel falls out of the calculations based on the other three parameters.

The open circuit voltage must be 3.3V plus the forward voltage drop of D1 above the float voltage of the 2-cell Li-ion battery plus an additional 15% for low intensity start-up and operation.

$$V_{OC} =$$
$$(V_{BAT(FLOAT)} + V_{FORWARD(D1)} + 3.3V) \bullet 1.15$$

The peak power voltage must be 0.75V plus the forward drop of D1 above the float voltage plus an additional 15% for low intensity operation.
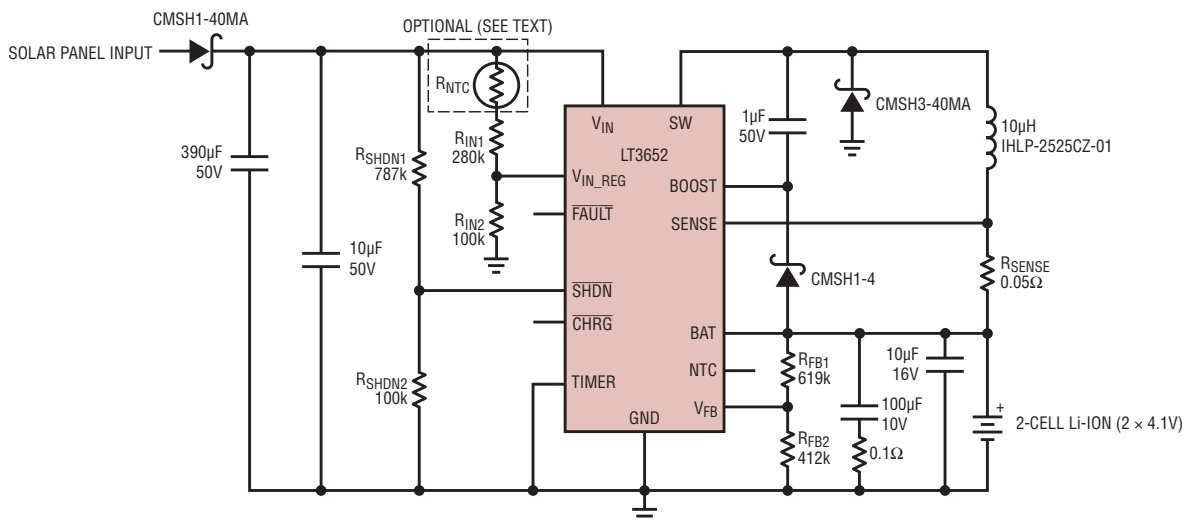

Figure 3. 2A Solar-powered battery charger

$V_{P(MAX)} =$

$(V_{BAT(FLOAT)} + V_{FORWARD(D1)} + 0.75V) \cdot 1.15$

The peak input power current is the product of the float voltage and the maximum charging current divided by the peak power input voltage and the efficiency of the charging circuit.

$$I_{P(MAX)} = I_{CHARGE} \cdot \frac{V_{BAT(FLOAT)}}{\eta \cdot V_{P(MAX)}}$$

Solving for these three equations, we can define the minimum requirements of the solar panel:

$V_{OC} = 13.8V$
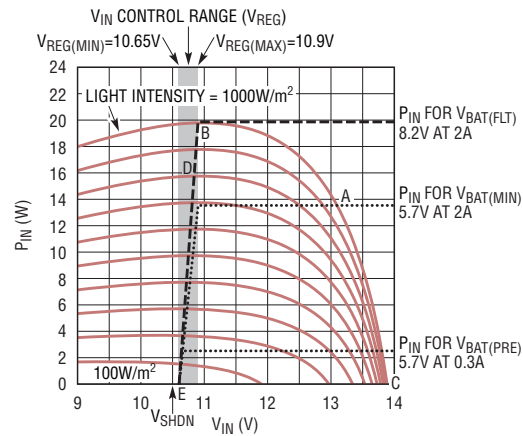
$V_{P(MAX)} = 10.9V$

$I_{P(MAX)} = 1.8A$

Figure 4. Action of the solar battery charger circuit in Figure 3. Power-intensity curves for various illumination levels are shown for $100W/m^2$ to $1000W/m^2$ in $100W/m^2$ steps. The V_{IN} control range (V_{REG}) is also shown. The V_{IN} control loop extracts maximum possible power from the solar panel by steering V_{IN} to the top of the panel's power-intensity curve when V_{IN} is in the V_{REG} range.

The solar panel characteristics can be seen in Figure 4.

The current sensing resistor, R_{SENSE}, is determined from the maximum $V_{SENSE} - V_{BAT}$ of 100mV divided by the maximum charging current of 2A

$R_{SENSE} = 0.05\Omega$

The output feedback voltage divider network of R_{FB1} and R_{FB2} are determined next. The voltage divider network must have a Thevenin's equivalent resistance of 250k to compensate for input bias current error. The V_{FB} pin reference voltage is 3.3V.

$$R_{FB1} = \frac{V_{BAT(FLOAT)} \cdot 250k}{3.3V}$$

$$= \frac{8.2V \cdot 250k}{3.3V}$$

$$= 621.2k$$

Let $R_{FB1} = 619k$

$$R_{FB2} = \frac{R_{FB2} \cdot 250k}{R_{FB2} - 250k}$$

$$= \frac{619k \cdot 250k}{619k - 250k}$$

$$= 419.2k$$

Let $R_{FB2} = 412k$

The next step is to set the peak power tracking voltage using the volt-age divider network of R_{IN1} and R_{IN2} connected between the V_{IN} and the V_{IN_REG} pins.

Let $R_{IN2} = 100k$

$R_{IN1} =$

$$\frac{V_{P(MAX)} - V_{FORWARD(D1)} - 2.74V}{2.74V} \cdot R_{IN2}$$

$$= \frac{10.9V - 0.5V - 2.74V}{2.74V} \cdot 100k$$

$$= 279.6k$$

Let $R_{IN1} = 280k$

Verify the minimum and maximum peak power input tracking voltages.

$$V_{REG(MIN)} = 2.67V \cdot \frac{R_{IN1} + R_{IN2}}{R_{IN2}} + V_{F(D1)}$$

$$= 10.65V$$

$$V_{REG(MAX)} = 2.74V \cdot \frac{R_{IN1} + R_{IN2}}{R_{IN2}} + V_{F(D1)}$$

$$= 10.9V$$

The final step in selecting resistor values is to determine the V_{SHDN} voltage divider network consisting of R_{SHDN1} and R_{SHDN2}. The V_{SHDN} rising threshold is 1.2V ± 50mV with a hysteresis of 120mV. The voltage divider network wants to be set such that, when the voltage on the V_{IN} pin is at $V_{REG(MIN)}$, V_{SHDN} is at its maximum possible value.

$$R_{SHDN1} = R_{SHDN2} \cdot$$

$$\frac{\left(V_{REG(MIN)} - V_{F(D1)}\right) - \left(V_{SHDN(MAX)} - V_{SHDN(HYST)}\right)}{V_{SHDN(MAX)} - V_{SHDN(HYST)}}$$

Let $R_{SHDN2} = 100k$

$$R_{SHDN1} =$$

$$\frac{\left(10.65V - 0.5V\right) - \left(1.25V - 0.12V\right)}{1.25V - 0.12V} \cdot 100k$$

$$= 798.2k$$

Let $R_{SHDN1} = 787k$

The V_{SHDN} limits are now determined as:

V_{SHDN} Rising Threshold

$V_{SHDN(MIN)} = 10.7V$

$V_{SHDN(MAX)} = 11.6V$

V_{SHDN} Falling Threshold

$V_{SHDN(MIN)} = 9.6V$

$V_{SHDN(MAX)} = 10.5V$

The LT3652 automatically enters a battery precondition mode if the sensed battery voltage is very low. In this mode, the charge current is reduced to 15% of the programmed maximum, as set by the current sensing resistor, R_{SENSE}. Once the battery voltage reaches 70% of the fully charged float voltage ($V_{FB} = 2.3V$), the LT3652 automatically increases maximum charge current to the full programmed value. The battery voltage threshold level between precondition

mode and maximum charge current is determined as follows:

$$V_{BAT(PRE)} < V_{BAT(MIN)} = V_{BAT(FLOAT)} \bullet \frac{2.3V}{3.3V}$$

$V_{BAT(MIN)} = 5.7V$

$V_{BAT(PRE)} < 5.7V$

$V_{CHRG(PRE)} = 0.15 \bullet I_{CHRG}$

$V_{CHRG(PRE)} = 0.3A$

Using and efficiency of 0.85, plot P_{IN} over the range of V_{IN} that is current controlled. This is the regulated V_{IN}, or V_{REG}, power line. The intersection of the V_{REG} power line with the solar panel power curve is the operating point. As the battery charges, the slope of the V_{REG} power line increases, indicating the increase in input power required to support the increasing output power. The intersection of the V_{REG} power line continues to follow up the solar panel's power curves until the charger exits constant current mode.

The resulting plots are shown in Figure 4.

The Circuit in Action

Figure 4 shows the power output of the solar panel plotted at light intensity levels from $100W/m^2$ to $1000W/m^2$ in $100W/m^2$ steps. At maximum light intensity (top curve in Figure 4) and the battery voltage just above the pre-conditioning level ($V_{BAT(MIN)}$ at 2A), the solar panel is producing more power than the charger needs. The solar panel voltage rises above the V_{REG} control voltage and travels across the constant power line until it intersects the light-power-intensity curve for that intensity level (point A in Figure 4). As the battery charges, the input power increases and the solar panel operating point moves up the light-power-intensity curve until the battery

approaches full charge (point B). The LT3652 transitions from constant current mode to constant voltage mode and the charging current is reduced. The solar panel operating point moves back down the light-power-intensity curve to the open circuit voltage (point C) when the battery reaches its final float voltage.

During the charging of the battery, if the light intensity diminishes, the operation point moves across a constant

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The input voltage regulation loop of the LT3652 has the ability to seek out the maximum power operating point of a solar panel's power characteristic, thus utilizing the full capacity of the solar panel.

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power line for the battery voltage until it reaches the new power-intensity curve. If the light intensity level continues to diminish, the operating point travels along this constant power line until it reaches the V_{REG} power line. At this point the charging current is reduced until the operating point is at the intersection of the light-power-intensity curve and the V_{REG} power line (point D for constant current charging at $V_{BAT(FLOAT)}$ with $800W/m^2$ illumination). As the battery continues to charge at this light intensity level, the operating point moves along the new light-power-intensity curve until the battery approaches full charge.

As darkness approaches, the operating point moves down the V_{REG} power line until charging current ceases (point E) and the solar panel output voltage drops below the SHDN

falling threshold at which point the LT3652 turns off.

The remaining elements of the design, selection of output inductor, catch rectifier and timer capacitor, are outlined in the design procedure in the LT3652 datasheet along with PCB layout considerations.

The maximum power voltage, for a monocrystalline solar cell, has a temperature coefficient of –0.37%/K while the maximum power level is –0.47%/K. This may be compensated for by letting R_{IN1} be a combination of a series resistor and a series NTC thermistor. The ratio of the two elements that comprise R_{IN1} and the value of R_{IN2} need to be adjusted to achieve the correct negative temperature of V_{IN} while still maintaining the control range of V_{IN}.

$$\Delta V_{IN(NTC)} = \frac{V_{REG}}{R_{IN2}} \bullet \frac{R_{NTC} \bullet \Delta R_{NTC}}{R_{IN1} \bullet R_{NTC}}$$

Conclusion

The input voltage regulation loop of the LT3652 has the ability to seek out the maximum power operating point of a solar panel's power characteristic, thus utilizing the full capacity of the solar panel. The float voltage regulation loop and its adjustable charging current enable the LT3652 to be used with many battery chemistries, making it a versatile battery charger. The added features of a wide input voltage range, an auto-recharge cycle to maintain a fully charged battery, a battery pre-conditioning mode, NTC temperature sensing, selectable C/10 or timed charging termination, a $\overline{FAULT}$ and a charging status pins fills out the full feature set of the LT3652. The LT3652 is available in a 3mm × 3mm 12-lead plastic DFN, package with an exposed pad. *LT*

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inductor current measured through the bottom MOSFET increases beyond 6A, the top power MOSFET is held off and switching cycles are skipped until the inductor current is reduced.

Conclusion

The LTC3612 is well suited for a wide range of low voltage step-down converter applications, including DDR memory termination applications requiring ±1.5A of output current. Its

high switching frequency and internal low $R_{DS(ON)}$ power switches allow the LTC3612 to offer a compact, high efficiency design solution supplying up to 3A output current. *LT*

High Current/High Speed LED Driver Revolutionizes PWM Dimming

by Josh Caldwell

Introduction

Power drivers that can produce regulated high current pulses are used in a number of lighting applications, ranging from high current LEDs in DLP projectors to high power laser diodes. For instance, in high end video projectors, high power LEDs are used to produce color illumination. The RGB LEDs in these projectors require precise dimming control for accurate color mixing—in this case, more control than simple PWM dimming can offer. Typically, to achieve the wide dynamic range required in color mixing, LED drivers must be able to rapidly switch between the two disparate regulated peak current states, *and* overlay PWM dimming without disruption. The LT3743 has the ability to meet these demanding accuracy and speed requirements.

The LT3743 is a synchronous buck DC/DC controller that utilizes fixed-frequency, average current mode control to accurately regulate the inductor current through a sense resistor in series with the inductor. The LT3743 regulates the current in any load with an output voltage range from 0V to 2V below the input rail with ±6% accuracy.

Precision, broad-range LED current control is achieved by combining accurate analog dimming (high and low states) with PWM dimming. Analog dimming is controlled via the CTRL_L, CTRL_H, and CTRL_T pins; PWM dimming via the PWM and CTRL_SEL pins. A rapid transition between the high and low analog states is made possible with the LT3743's unique use of externally switched load capacitors, which allows the LT3743 to change regulated LED current levels within several microseconds. The switching frequency may be programmed from 200kHz to 1MHz using an external resistor and synchronized to an external clock from 300kHz to 1MHz.
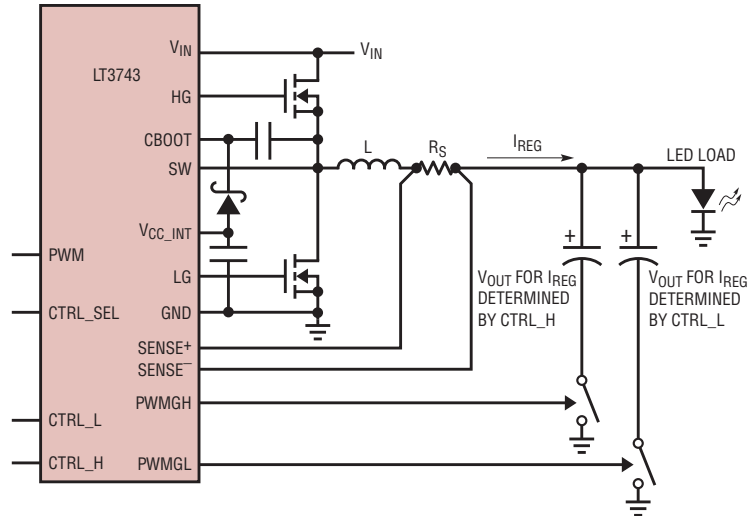

Figure 1. Basic switched-capacitor topology

Switched Output Capacitor Topology

In traditional current regulators, the voltage across the load is stored in the output capacitor. If the load current is suddenly changed, the voltage in the output capacitor must charge or discharge to match the new regulated current. During the transition, current in the load is poorly controlled, resulting in slow load current response time.

The LT3743 solves this problem with a unique switched output capacitor topology, which enables ultrafast load current rise and fall times. The basic idea behind the topology is that the LT3743 acts as a regulated current source driving into the load. The voltage drop across the load for a given current is stored in the first switched output capacitor. When a different regulated current state is desired, the first output capacitor is switched off and a second capacitor is switched in. This allows each capacitor to store the voltage drop for the load corresponding to the desired regulated current.

Figure 1 shows the basic topology with the various control pins. The PWM and CTRL_SEL pins are digital control pins that determine the state of the regulated current. The CTRL_H and CTRL_L pins are analog inputs with a
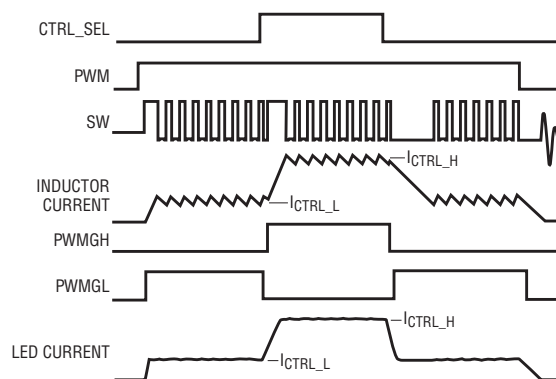

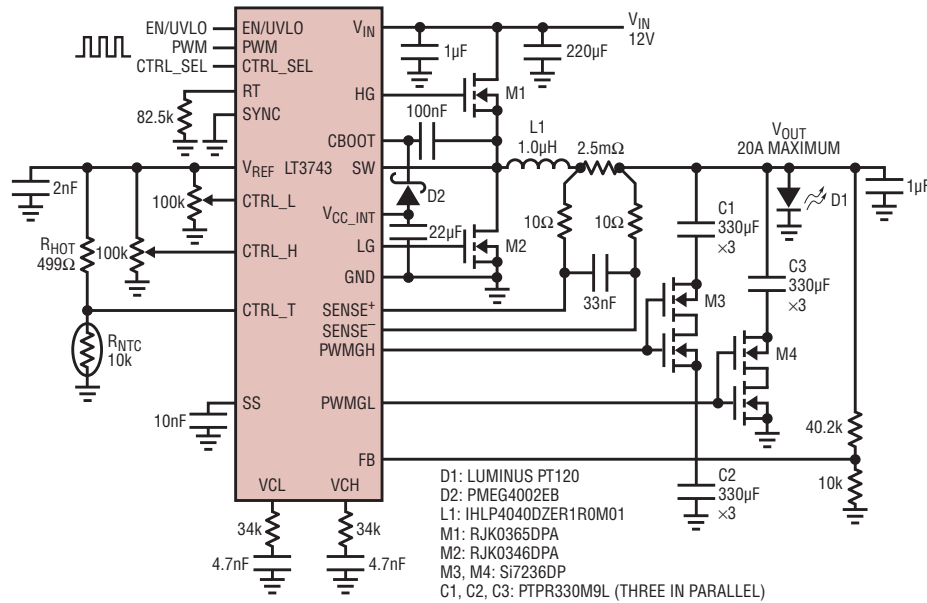Figure 2. LED current PWM and CTRL_SEL dimming

Figure 3. A 24V, 20A LED driver using switched output capacitors

full-scale range of 0 to 1.5V, producing a regulated voltage of 0mV to 50mV across the current sense resistor.

Figure 2 shows the timing waveforms in response to the various states of the PWM and CTRL_SEL pins. When PWM is low, all switching is terminated and both output capacitors are disconnected from the load.

Although the LT3743 may be configured with switched output capacitors, it is easily adapted to any traditional analog and/or PWM dimming scheme.

Switching Cycle Synchronization

The LT3743 synchronizes all switching edges to the PWM and CTRL_SEL rising edges. Synchronization gives system designers the freedom to use any periodic or non-periodic PWM-dimming pulse width and duty cycle. This is an essential feature for high current LED drivers during recovery from a zero or low current state to a high current state. By restarting the clock whenever the CTRL_SEL or PWM signals go high, the inductor current begins ramping up immediately without having to wait for a rising edge of the clock. Without synchronization, the phase relationship of the clock edge and the PWM edge would be uncontrolled, possibly resulting in

visible jitter in the LED light output. When using an external clock with the SYNC pin, the switching cycle resynchronizes to the external clock within eight switching cycles.

A 24V, 20A LED Driver Using Switched Output Capacitors for High End DLP Projectors

High end DLP projectors demand the highest quality image and color reproduction. To achieve high color accuracy, variations in the color of individual LEDs are corrected by mixing in the other two color LEDs. For example, when the red LED is on at full current, the blue and green LEDs are turned on at low current levels so they can be mixed in to produce accurate red. This technique requires the ability

to rapidly transition between relatively low (~2A) and high (~20A) LED currents so that PWM dimming edges are preserved. Figure 3 shows a 24V/20A LED driver for use specifically with high end DLP projectors.

The relatively low switching frequency of 450kHz allows for a very small 1.0µH inductor. With 25% ripple current, the transition times between the high and low current states is about two microseconds. The large 1mF output capacitors store the voltage drop across the LED for the two different current states and provide instantaneous current when the MOSFET dimming switches are turned on. Use of several low ESR capacitors in parallel is critical to providing rapid LED current transitions.
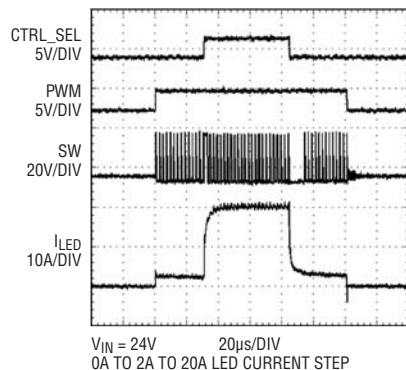

V_{IN} = 24V 20µs/DIV
0A TO 2A TO 20A LED CURRENT STEP

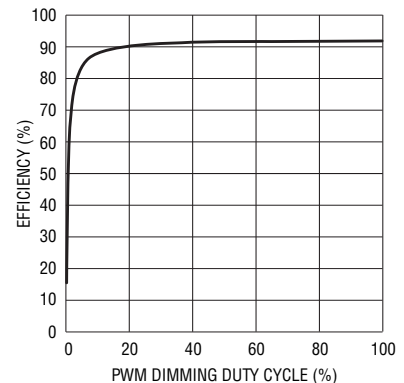**Figure 4. Zero to 2A to 20A LED current steps**

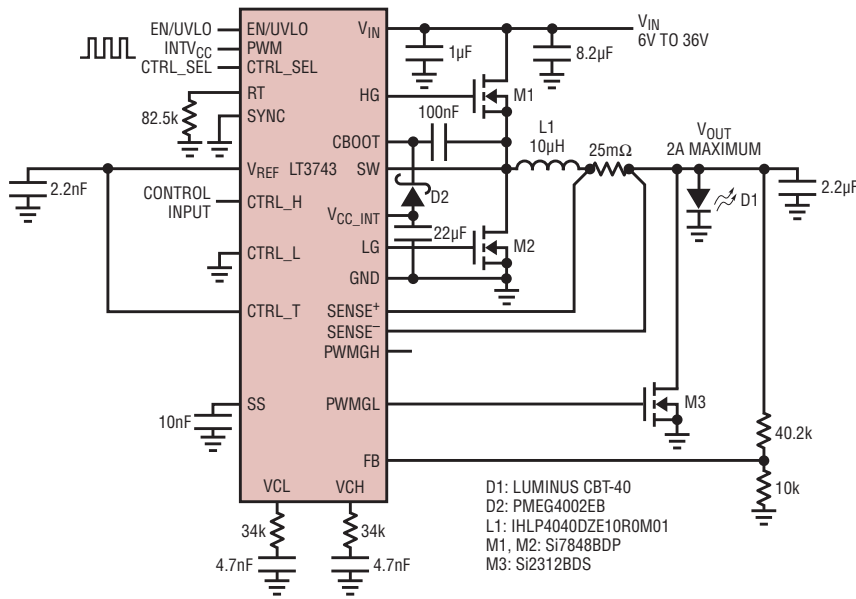**Figure 5. 12V, 20A PWM dimming efficiency using a green LED**

Figure 6. A 6V to 36V input, 2A LED driver with current limited shunted output
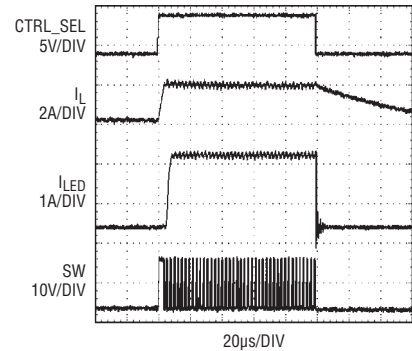

Figure 7. 0A to 2A current limited shunted output PWM dimming

The regulated high and low currents are set by voltage dividers from the V_{REF} pin to the CTRL_L and CTRL_H pins. The ±2%, 2V reference at V_{REF} is also used to provide the reference signal the temperature derating circuit applied at CTRL_T (see "Thermally Derating the LED Current" below).

To reduce potentially large start-up currents, the LT3743 uses a unique soft-start circuit that throttles back the regulated currents, providing full drive when the soft-start pin is charged to 1.5V. To minimize the transition time between current levels, the LT3743 employs individual compensation for each level so that the current control loop may return to steady-state operation as quickly as possible. Figure 4 shows the LED current step from 0A to 2A to 20A.

High Efficiency Over a Wide Range of PWM Duty Cycles

Power dissipation is a critical design parameter in portable DLP projectors.

Unlike many shunt-type high current LED drivers currently available, the LT3743 has excellent efficiency over a wide range of PWM duty cycles. By delivering power only to the load instead of either shunting power away or charging the output capacitor, most of the energy lost in common traditional PWM-dimmed drivers is conserved. Figure 5 shows the efficiency with V_{IN} = 12V, driving a green LED between 0A and 20A over the entire duty cycle range.
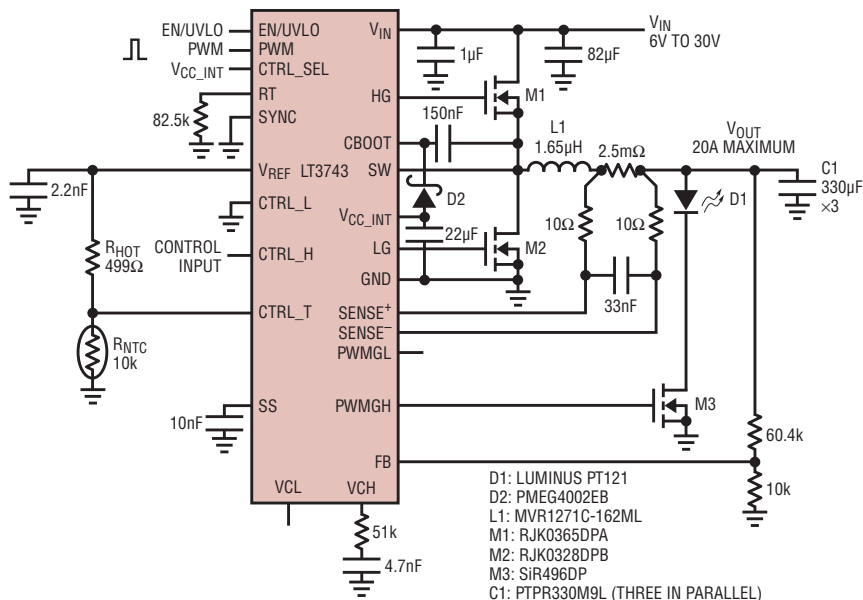

Figure 8. A 6V to 30V input, 20A LED driver with switched cathode PWM dimming

Shutdown and Precision Enable

When delivering high load currents, the amount of supply undervoltage lock-out (UVLO) hysteresis required for proper operation is highly dependent on board layout. For maximum flexibility, the LT3743 incorporates a precision enable threshold with a 5.5µA current source flowing into the pin when the EN/UVLO pin is lower than 1.55V. Using a voltage divider from the input supply to ground any amount of hysteresis may be added to the system. To conserve power in portable applications, the LT3743 is completely disabled and supply current drops below 1µA when the EN/UVLO pin is lower than 0.5V.

Thermally Derating the LED Current

Proper thermal management is vital with any high current load to protect expensive high current LEDs and prevent system-wide damage. The LT3743 uses the CTRL_T pin to reduce the effective regulated current in the load for both the high and low control currents. Whenever CTRL_T is lower than the control voltage on the CTRL_L or CTRL_H pins, the regulated current is reduced. The temperature derating is programmed using a temperature dependent resistor divider from the V_{REF} pin to ground.

Output Voltage Protection

Voltage protection is important to prevent damaging expensive projector LEDs. The LT3743 utilizes the FB pin to provide a regulated voltage point for the output. To simplify system design, the LT3743 uses an internal 1V reference, softly reducing the regulated current when the FB voltage reaches 900mV.

Powerful Gate Drivers

To provide adequate drive and reduce switching losses in high current power MOSFETs, the LT3743 uses very strong switching MOSFET drivers. The on-resistance of the LG and HG PMOS pull-up drivers is typically 2.5Ω. The LG and HG NMOS pull-down drivers on-resistance is typically less than

1.3Ω. With on-resistance this low, two high current MOSFETs may be used in parallel for applications exceeding 20A. Most currently available LED drivers do not provide adequate gate drive for dimming MOSFETs and as a result need an additional external gate driver. The LT3743 integrates this into the PWMGL and PWMGH drivers and has a 2Ω typical NMOS pull-down and a 3.7Ω typical PMOS pull-up to drive any 5V dimming MOSFET.

Traditional PWM Dimming

The LT3743 adapts to any traditional PWM dimming method. Shunted output dimming used by competing LED drivers wastes energy and has poor efficiency for LED duty cycles below

> *The LT3743 produces ultrafast high current LED rise times while providing accurate current regulation. Its ability to support multiple current states meets the demands of high performance theater-quality DLP projectors by allowing LED colors to be easily mixed. In addition to speed, the LT3743's switched capacitor topology reduces board size by allowing the use of a compact, low value inductor. Additional features include switching cycle synchronization, overvoltage protection, high efficiency and easy adaptability for varied application needs.*

approximately 50%. Since the LT3743 has two levels of current regulation, the regulated current can to drop to zero when the shunt is engaged. This provides excellent efficiency even for low LED duty cycles.

Figure 6 shows a 2A LED driver configured with a current-limited shunted output. Note that the CTRL_L pin is tied to ground, PWMGL is used to drive
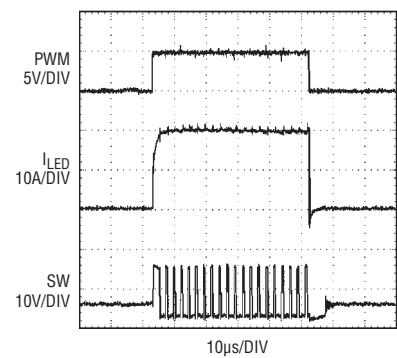

Figure 9. 0A to 20A switched cathode PWM dimming

the shunting MOSFET, and CTRL_SEL is used for dimming. With CTRL_L tied to ground, when the CTRL_SEL pin is low, the shunt is engaged and the current in the inductor is regulated at 0A. When CTRL_SEL is high, the shunting MOSFET is turned off, and the regulated current is determined by the voltage at the CTRL_H pin. Figure 7 shows the current-limited shunted PWM dimming with a 12V input.

In addition to the shunt, the LT3743 is readily configured to driving the dimming MOSFET in series with the cathode of the LED. When multiple current states are not required, this is the preferred method of PWM dimming. Figure 8 illustrates a 6V to 30V, 20A LED driver with switched cathode PWM dimming. Figure 9 shows switched cathode, PWM dimming with a 0A to 20A current step and a dimming ratio of 100:1.

Conclusion

The LT3743 produces ultrafast high current LED rise times while providing accurate current regulation. Its ability to support multiple current states meets the demands of high performance theater-quality DLP projectors by allowing LED colors to be easily mixed. In addition to speed, the LT3743's switched capacitor topology reduces board size by allowing the use of a compact, low value inductor. Additional features include switching cycle synchronization, overvoltage protection, high efficiency and easy adaptability for varied application needs. ⎿⎾

Produce High DC/DC Step-Down Ratios in Tight Spaces with 30ns Minimum On-Time Controller in 3mm × 3mm QFN

by Theo Phillips

Introduction

It can be a challenge to design a DC/DC converter that takes a high voltage automotive or industrial power supply down to the 1.5V or lower voltages required by today's microprocessors and programmable logic chips.

To maintain efficiency and performance, designers are often forced to create a 2-stage solution, which first steps down to an intermediate voltage and uses another converter to produce the low voltage from there. 2-stage solutions can perform well, and are handy if the application can use the intermediate voltage elsewhere, but 2-stage solutions always take more space and are more costly than a single stage solution.

Many regulators can produce high step-down ratios in a single stage if the switching frequency of the step-down converter is slowed considerably. However, this option sacrifices efficiency and requires larger, more expensive external components, doing little to solve the space and cost problems incurred in 2-stage solutions.

The LTC3775 is a voltage mode DC/DC regulator with a very low minimum on-time of 30ns, allowing very wide step-down ratios at high switching frequencies without sacrificing performance. Unlike most voltage mode controllers, the LTC3775 offers cycle-by-cycle programmable current limit, excellent short circuit protection and fast transient response over a wide input voltage range.

A 1.2V Converter Operating from 5V–28V$_{IN}$ at 350kHz

The LTC3775 is ideal for generating low output voltages from high input voltages, a common requirement for powering CPUs from wide-ranging

Current mode controllers are often favored for their continuous monitoring of current through the inductor or switches. While a typical voltage mode controller requires additional circuitry to monitor current in the power stage, the LTC3775 requires no ancillary circuits to oversee the entire switching cycle.

rails such as those found in automotive applications. Figure 1 shows an application providing a continuous 15A from an 5V–26V input.

Current mode controllers are often favored for their continuous monitoring of current through the inductor or switches, protecting these components and the load against short circuits and pre-biased outputs during start-up. To avoid these difficulties, a typical voltage mode controller requires additional circuitry to monitor current in the power stage. The LTC3775 requires no ancillary circuits to oversee the entire switching cycle.

The current limit is programmed with two resistors (as shown in the block diagram of Figure 2), corresponding to the current measured through the top and bottom switches
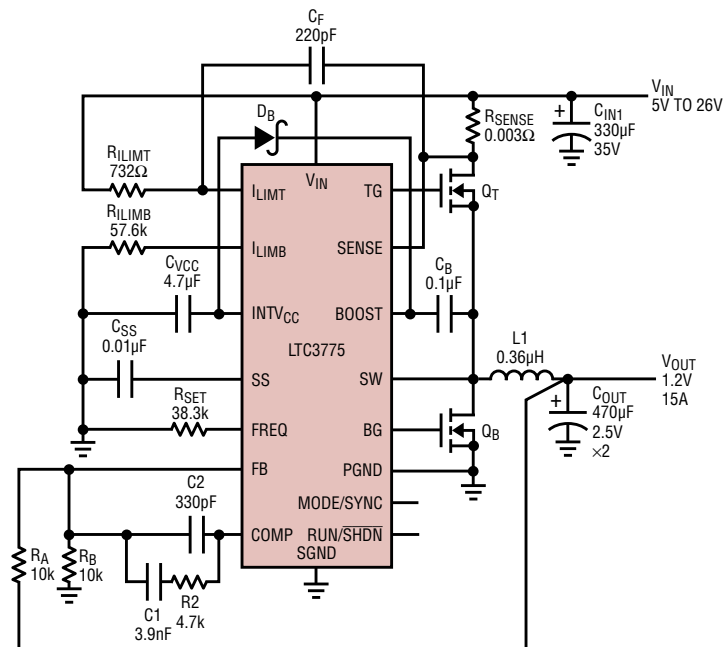
C$_{OUT}$: SANYO 2R5TPD470M5
D$_B$: CMDSH4E
L1: IHLP-4040DZ-ER-R36-M11
Q$_B$: RJK0301DPB-00-J0
Q$_T$: RJK0305DPB-00-J0

Figure 1. A 1.2V, 15A converter

during their respective on times. This arrangement allows cycle-by-cycle current limit, regardless of the duty cycle, and ensures that the inductor is not saturated.

In a current mode converter, the voltage on the output of the error amplifier controls the peak switch current, such that the switch current must always be monitored, allowing the introduction of noise. This may be most pronounced around 50% duty cycle in some current mode designs. Contrast this with a voltage mode converter, where the error voltage on V_{OUT} is compared to a saw-tooth ramp, which in turn controls duty cycle; the larger the error voltage, the longer the top switch stays on. The LTC3775 senses current through both MOSFETs to assure that they do not exceed programmed limits. During normal operation, these limits do not come into play, and noise-free operation is assured.

A high side current limit would be of little value if the circuit was operated at its maximum V_{IN}, since the bottom switch would be on most of the time, and nothing would protect the synchronous MOSFET. Fortunately, the low side current limit, programmed by I_{LIMB}, can limit the current through the bottom switch. Conversely, a fault at low V_{IN} during the on-time of the top switch requires a high side current limit for immediate response. The LTC3775 uses both top- and bottom-side current limit circuits to provide
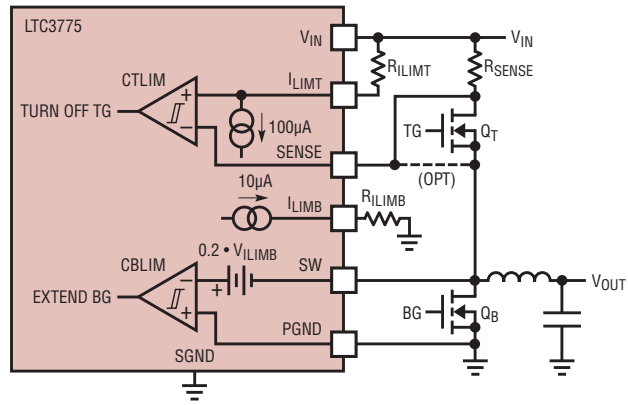

Figure 2. The LTC3775 features high and low side programmable current limits, for cycle-by-cycle short circuit protection.

optimum protection for the MOSFETs and inductor.

This current limit approach is effective, as shown by the short circuit behavior in Figure 3. A hard short could spell disaster for an unprotected voltage mode converter. But here, the inductor does not saturate, and the input rail maintains its integrity while the output gracefully drops.

Output voltage is monitored using an inverting summing amplifier topology, with the FB pin configured as a virtual ground. The reference voltage is accurate to within ±0.75% over temperature. The LTC3775 uses a true operational error amplifier with 80dB of open loop gain, and a 25MHz gain-bandwidth product. Feedback gain can be tightly controlled by external components, allowing the use of "Type 3" compensation, which provides a phase boost at the LC double pole frequency and significantly improves

control loop phase margin. Figure 4 shows a characteristically fast load transient response.

The modulator consists of the PWM generator, the output MOSFET drivers and the external MOSFETs themselves. The modulator gain varies linearly with the input voltage. The line feedforward circuit compensates for this change in gain, and provides a constant gain from the error amplifier output to the inductor input regardless of input voltage.

The application in Figure 1 demands a minimum on time of just 86ns at the maximum input voltage of 28V. Many controllers turn the top gate on at the beginning of the clock cycle and must wait for the response time of the PWM comparator before turning off the top gate. This response time is typically around 100ns or more. In addition, those controllers would make the decision at a noisy interval,
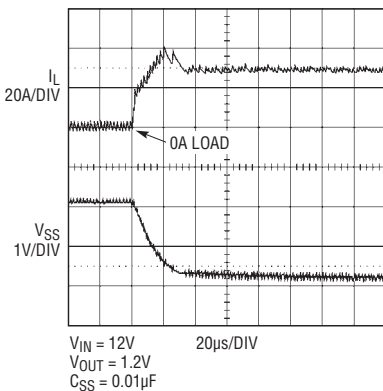

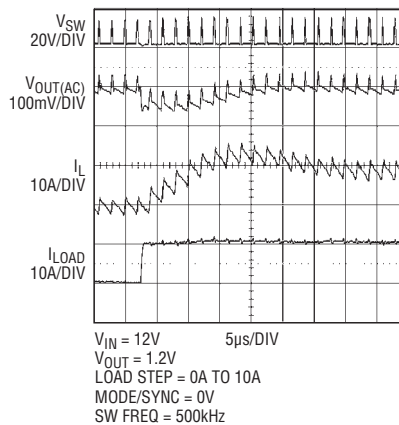Figure 3. Short circuit behavior for the converter of Figure 1

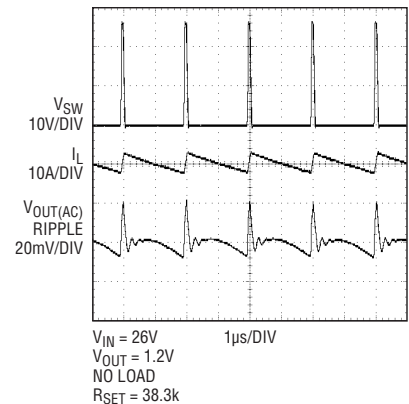Figure 4. Load transient response for the converter of Figure 1

Figure 5. The converter of Figure 1 demonstrates a clean switching waveform with a razor-thin on-time.
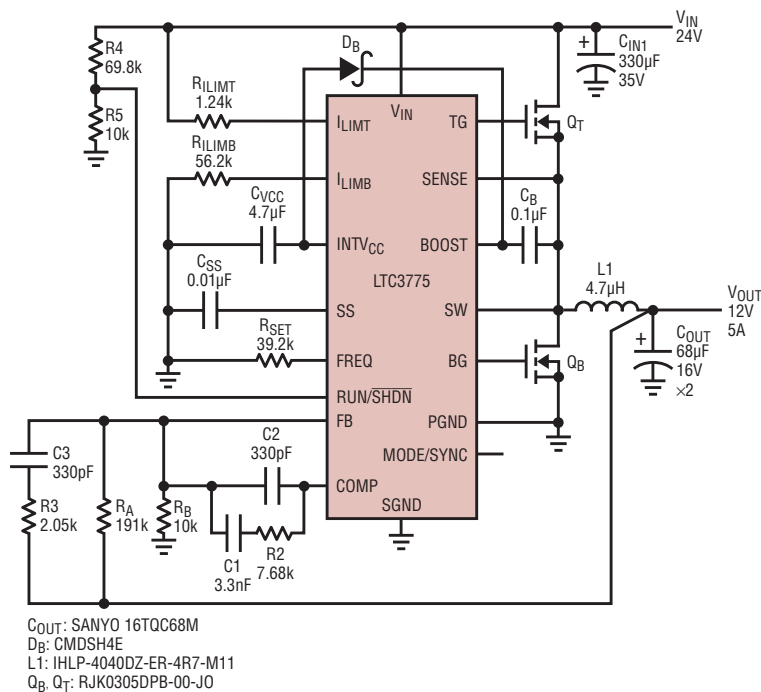
Figure 6. A 12V, 5A converter operating at 500kHz from 24V_IN.

C_OUT: SANYO 16TQC68M
D_B: CMDSH4E
L1: IHLP-4040DZ-ER-4R7-M11
Q_B, Q_T: RJK0305DPB-00-J0

Figure 7. Efficiency for the converter of Figure 6

because ringing persists for some time after the top gate turns on. Thus even though the minimum on-time could be as low as 100ns, practical design considerations such as noise and jitter would require a nominal on-time of no less than 150ns to guarantee that there will be no pulse-skipping mode at maximum input voltage.

The LTC3775's leading-edge voltage mode architecture and very low minimum on-time of 30ns makes it practical to run with on-times as low as 40ns, even in noisy environments. The LTC3775's leading edge modulation architecture turns on the top gate when the PWM comparator trips and turns off the top gate when the clock signal goes high. The switching waveform shows no skipped pulses and is free from erratic behavior, even with very short on-times. Figure 5 illustrates waveforms for a 36V input, 1.2V output converter operating in continuous conduction mode (CCM) at 350kHz with no load. The waveform shows constant frequency operation and extremely low switch node jitter.

A 12V Converter Operating from 24V_IN at 500kHz

Because the LTC3775 separately monitors the current through the top and bottom switches, its comparators do not need extended common mode ranges. Some current mode converters use a sense resistor in series with the inductor, restricting the range of V_OUT due to the common mode range of their current comparators. Without this restriction, the LTC3775 is useful for powering higher output voltages, as exemplified by the 12V converter of Figure 6. Also, the absence of a sense resistor means no loss in efficiency, and no low amplitude current mode sense signal which can be a source of jitter in the SW node waveform.
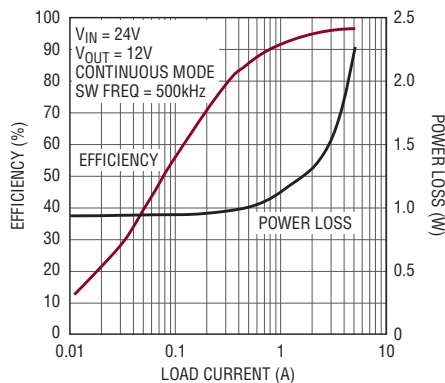
Current sensing through the top MOSFET can be measured across a sense resistor for the highest possible accuracy. To boost efficiency and save a component, just omit the sense resistor and measure directly across the top MOSFET. Figure 6 demonstrates a high efficiency 12V converter that uses this arrangement. When using the top MOSFET $R_{DS(ON)}$ to measure current, care must be taken to Kelvin-connect the V_{IN} pin of the IC to the drain terminal of the power MOSFET and the SENSE pin to the source of the MOSFET. Likewise, when a sense resistor is used for improved current limit accuracy, Kelvin-connect the V_{IN} and SENSE pins of the IC to the positive and negative terminals of the sense resistor, respectively.

The circuits featured here operate in forced continuous mode, for constant frequency operation at any load. If higher light-load efficiency is desired, the MODE/SYNC pin can be tied to a voltage above 1.2V (typically INTV_CC) for pulse skippin operation. This pin can also be the input for a sync signal, from 250kHz to 1MHz. No external PLL components are required for syncing. The synchronization feature operates within ±20% of the free-running frequency defined by R_{SET}.

Conclusion

The LTC3775 provides unprecedented performance for today's demanding high current, low voltage power supply systems. With a minimum on-time of 30ns and a high bandwidth true operational amplifier, the controller can operate at frequencies up to 1MHz, maintaining a very small power supply PCB footprint and reducing output ripple.

The LTC3775 offers numerous features in a tiny 3mm × 3mm QFN, including cycle-by-cycle current limit, synchronization capability over a ±20% range, a wide input and output operating voltage range, internal line feed-forward compensation, a high bandwidth operational error amplifier, strong internal gate drivers and very tight output voltage tolerance (±0.75% over temperature). *LT*

New Generation of 14-Bit 150Msps ADCs Dissipates a Third the Power of the Previous Generation without Sacrificing AC Performance

by Clarence Mayott

Introduction

The LTC2262 family of ultralow power, high speed analog-to-digital converters dissipates less than one third the power of comparable earlier-generation ADCs while maintaining excellent AC performance. Ultralow power makes it possible to add features to and improve the performance of power-limited applications while remaining within the power budget. Of course, improved operating efficiency also reduces recurring operating costs in applications found in 3G/4G LTE and WiMAX basestation equipment.

In addition to offering considerably lower power, the ADCs in the LTC2262 family incorporate a unique set of digital output features that help to simplify layout and reduce digital feedback. The low power core of the LTC2262 is also integrated into multichannel parts, including 4-channel ADCs and 2-channel ADCs. For a complete list of the ultralow-power ADC family, see Table 1.

Low Power, High Performance

The LTC2262 family includes 14- and 12-bit ADCs that span sampling rates from 25Msps (which can sample down to 1Msps) to 150Msps, while consuming approximately 1mW for every megasample-per-second. For instance, the LTC2262-14 is a 14-bit, 150Msps ADC that consumes only 149mW of power from a 1.8V supply.

It is important to note that the ultralow power dissipation for this pipelined ADC architecture comes without sacrificing performance. The LTC2262-14 has a typical signal-to-noise ratio (SNR) of 72.8dB and SFDR of 88dB at baseband. Figure 1 shows the typical AC performance of
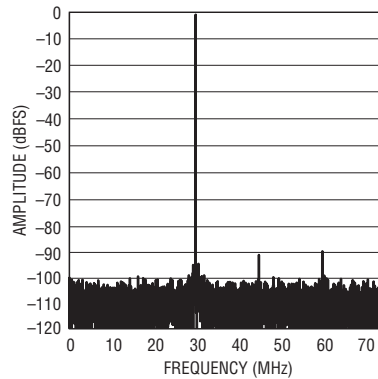

Figure 1. Typical performance of the LTC2262-14

the LTC2262-14 sampling a 30MHz sine wave at 150Msps (data from the circuit of Figure 2). The exceptional low power operation improves thermal performance in compact enclosures, where high temperatures can degrade SNR.

Digital Outputs

The LTC2262 family also offers some unique digital features to simplify overall design in a wide variety of applications. The LTC2262 can be configured to run in one of three data output modes: full rate CMOS, double data rate (known as DDR) CMOS, and DDR LVDS.

Full rate CMOS presents the data on all 14 lines and consumes the lowest power. This mode is identical across Linear's parallel CMOS output ADCs so designers can use a much lower power ADC without changing FPGA code or ASIC design.

| Sample Rate	Resolution	Single Channel	Two Channel	Four Channel
25Msps	12-Bit	LTC2256-12	LTC2263-12	LTC2170-12
	14-Bit	LTC2256-14	LTC2263-14	LTC2170-14
40Msps	12-Bit	LTC2257-12	LTC2264-12	LTC2171-12
	14-Bit	LTC2257-14	LTC2264-14	LTC2171-14
65Msps	12-Bit	LTC2258-12	LTC2265-12	LTC2172-12
	14-Bit	LTC2258-14	LTC2265-14	LTC2172-14
80Msps	12-Bit	LTC2259-12	LTC2266-12	LTC2173-12
	14-Bit	LTC2259-14	LTC2266-14	LTC2173-14
105Msps	12-Bit	LTC2260-12	LTC2267-12	LTC2174-12
	14-Bit	LTC2260-14	LTC2267-14	LTC2174-14
125Msps	12-Bit	LTC2261-12	LTC2268-12	LTC2175-12
	14-Bit	LTC2261-14	LTC2268-14	LTC2175-14
150Msps	12-Bit	LTC2262-12	N/A	N/A
	14-Bit	LTC2262-14	N/A	N/A

Table 1. The new generation of ultralow-power ADCs
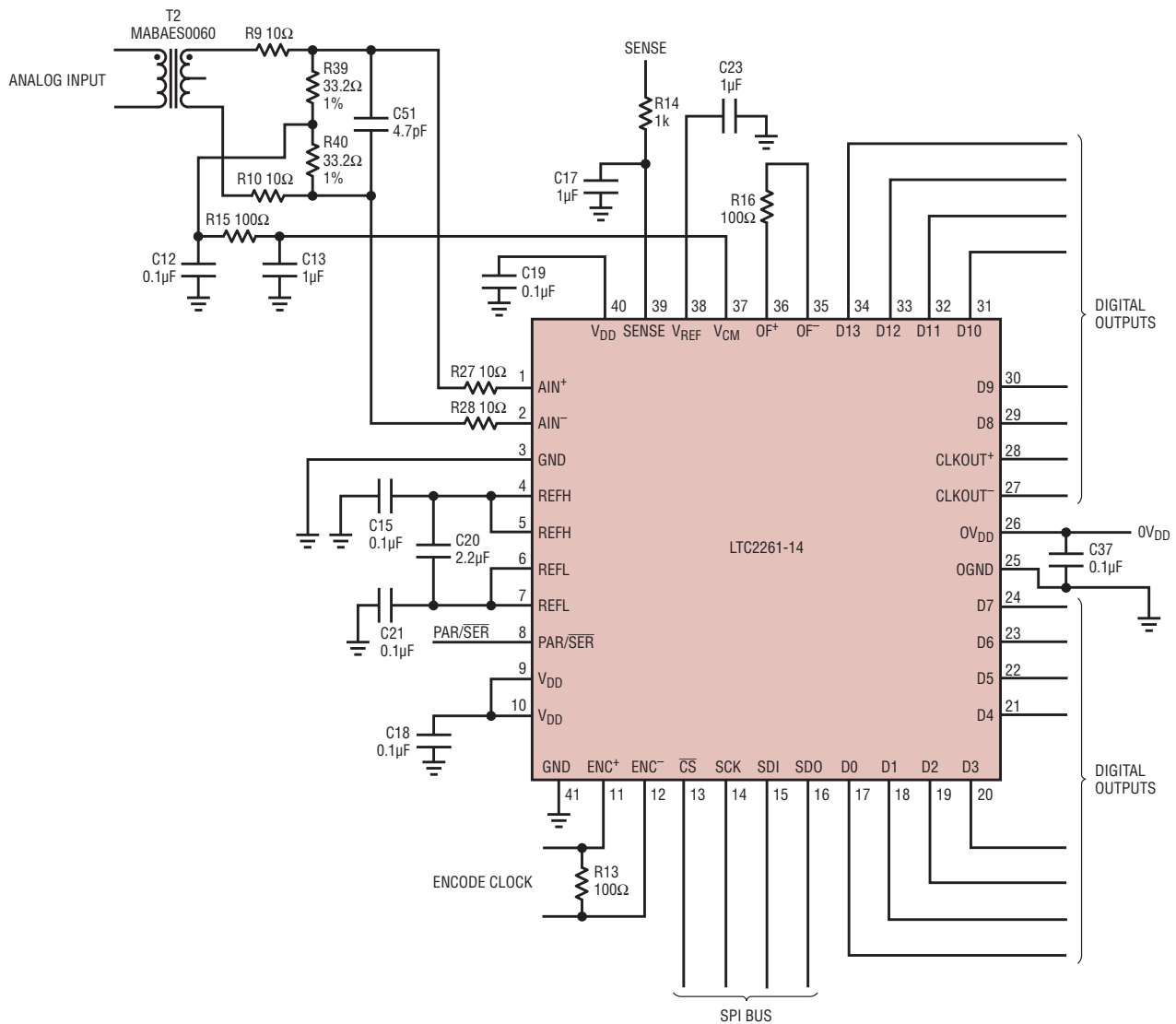
Figure 2. Typical application of the LTC2261-14

If board space or FPGA GPIO is limited, then the DDR CMOS mode can be used reduce the number of data lines. In double data rate LVDS mode, two data bits are multiplexed and output on each differential output pair, one valid on the rising edge of the clock, the other on the falling edge. This allows the data to be clocked out on half the data lines, which reduces the number of lines to seven for the 14-bit ADCs, and six for the 12-bit ADCs.

DDR LVDS mode functions in a similar fashion, with two bits clocked out on each data line on each clock cycle, but because it is a differential signal it uses 14 data lines, versus the 28 lines required for standard LVDS signaling. DDR LVDS uses an additional 10mW but the differential signaling provides some rejection of digital noise, also known as digital feedback.

Digital Feedback

Digital feedback occurs when energy from ADC outputs couples back into the analog section, causing interaction that appears as odd shaping in the noise floor and spurs in the ADC output spectrum. The worst situation is at midscale, where all outputs are changing from ones to zeroes, or vice versa, generating large ground currents that couple back into the input.

Digital feedback at both the device level and the system level can be made worse by poor layout choices. Long output busses, routing at low characteristic impedance and heavy capacitive loading at the receiving device all conspire to produce higher pulse currents in the output stages.

The use of the maximum digital output supply voltage (OV_{DD}) similarly maximizes digital currents. Placement of OV_{DD} bypass on the bottom of the board, with added lead inductance, large bodied capacitors, small diameter vias, thick boards, and thermal relief all raise the impedance of the supply rails to the output section, increasing the potential for noise sources. Returning OGND to a poorly grounded paddle makes things worse. These layout conditions together conspire to increase ground bounce on the substrate, which leads to digital feedback.

Digital feedback manifests itself in the ADC output spectrum. Figure 3 shows the noise floor of the LTC2261-14, a 14-bit 125Msps ADC. To produce this result, a demo board was modified to maximize digital feedback. In this case the digital feedback causes peaks in the noise floor of about 8dB.

The layout techniques used on the LTC2261-14 demo board are designed to help minimize digital feedback, but some is still unavoidable. The layout of the demo board area around the LTC2261 is shown in Figure 4. The use of barriers around the analog input, and clock help to reduce digital feedback effects. Also proper grounding of the reference bypass and OV_{DD} bypass help to mitigate digital feedback. A proper layout helps reduce the digital feedback seen in the output spectrum.

With a poor layout, and with low signal levels, digital feedback can appear as an exaggeration of odd harmonics, as shaping of the noise floor related to the delayed feedback and as some exaggeration of the noise floor. In severe cases, localized regions of the noise floor may be elevated by 20dB. If a narrow band application happens to collide with the elevated region of the noise floor, the result is a real loss of SNR on the order of 20dB. While good layout can help reduce the effects of digital feedback, it may not be enough to eliminate the problem.

The LTC2262 includes a unique digital feedback mitigation feature called "alternate bit polarity mode." Digital feedback is likely to occur when sampling a small input signal that is
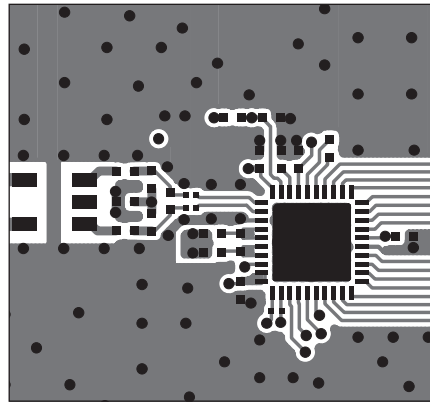

Figure 4. Layout of the LTC2261-14 application shown in Figure 2

exercising a few codes around midscale. On each sample, all of the high order data bits are swinging from zero to one, which generates large ground

The LTC2262 ultralow power core is also available in 2- and 4-channel ADCs. The LTC2175-14 is a quad, 14-bit ADC that samples at 125Msps. The LTC2175 dissipates only 558mW of total power—only 139.5mW per ADC. At 125Msps, each channel outputs two bits at a time, using only two lines per ADC. This reduces the number of data lines used by the LTC2175, and allows it to be packaged in a space-saving 7mm × 8mm QFN package.

currents that can couple back into the analog inputs, maximizing digital feedback. When alternate bit polarity mode is used, every odd data line is inverted. So, instead of 14 data lines simultaneously switching between 0 and 1, half are switching in one direction, half in the other direction. This produces a cancellation of fields, significantly reducing the resulting ground currents, and minimizing digital feedback. To decode this data, simply apply an inverter on each odd data line in the receiver.

In addition to the alternate bit polarity mode, an optional data output randomizer is available to further reduce interference from the digital outputs. The least significant bit (LSB) is combined using an exclusive-OR function with the other outputs before transmission. The received digital output bus can then be easily decoded by performing the reverse operation in the FPGA. Using this data encode scheme reduces the residual tone caused by digital feedback by 10dB to 15dB. Using the output randomizer and alternate bit polarity together can significantly decrease the effects of digital feedback.

For comparison, Figure 5 shows an image of the noise floor of the LTC2261-14 taken using the same board and on the same scale as before, but with alternate bit polarity and the data output randomizer enabled. The shaping of the noise floor is reduced, which improves SNR and SFDR. Using alternate bit polarity mode helps to reduce digital feedback on boards with poor layout, and can improve results in designs with low level input signal.

Multiple Channel Versions

The LTC2262 ultralow power core is also available in 2- and 4-channel ADCs. The LTC2175-14 is a quad, 14-bit ADC that samples at 125Msps. The LTC2175 dissipates only 558mW of total power—only 139.5mW per ADC. At 125Msps, each channel outputs two bits at a time, using only two lines per ADC. This reduces the number of data

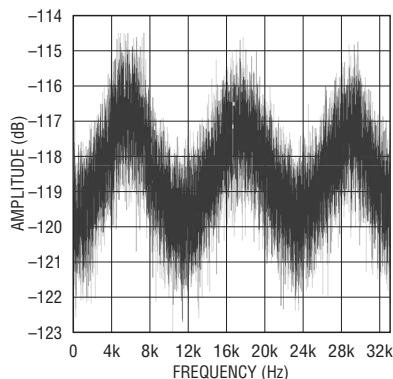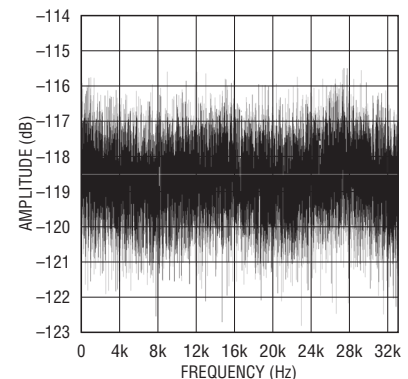**Figure 3. LTC2261 noise floor in normal operation**

Figure 5. Noise floor with alternate bit polarity and data output randomizer enabled

Robust, Quiet, Stable Power Supply for Active Antenna Systems with Built-In Protection and Diagnostic Capabilities

by Sam Rankin and Steve Knoth

Introduction

The days of the simple car radio, like the Mercedes dashboard shown in Figure 1, are over, supplanted by the era of the automobile infotainment system (see Figure 2). The venerable AM/FM radio still holds a place at the infotainment table, but it now shares space with digital audio broadcasting (DAB), digital and high-definition television (HDTV), satellite radio, integrated cell phones, CD/DVD/MP3 players, global positioning system (GPS) navigation and video game systems.

Behind the dashboard, fueling this wealth of information, are active antenna systems. As infotainment centers have expanded in complexity, the number of active antennas needed to feed music and data into the infotainment center has multiplied. It is now common for an automobile to have on average, three to five active antenna systems, from a combination of AM, FM, DAB, HDTV, satellite radio, traffic alerts, cellular, WiMax and GPS—sometimes with multiple antennas per band to improve reception quality. The sensitive circuits in these active antenna systems require protection and isolation from the harsh automotive environment and a way to provide antenna status and diagnostic feedback to a host system.

The LT3050 is an innovative regulator with precision current limit and diagnostic functions. It combines the robust performance, reliability and durability common to Linear Technology linear regulators with an enhanced feature set geared towards active antenna systems, including:

❏ Programmable current limit
❏ Soft-start
❏ Open-circuit detection
❏ Output current monitor

Figure 1. Old school dashboard; one passive antenna for AM/FM reception

❏ Open-collector fault signal

The LT3050 is a single IC solution that replaces a complex arrangement of current sense amplifiers, operational amplifiers and discrete components and other ICs that would otherwise be needed to meet the demanding combination of protection requirements and diagnostic features required in automobile antenna systems.

The LT3050 delivers up to 100mA continuous output current with a 340mV typical dropout voltage at full load. The IC features a wide input voltage range of 2V to 45V, delivering adjustable output voltages down to 0.6V. A single capacitor provides both ultralow noise operation—only $30\mu V_{RMS}$ across a wide bandwidth of 10Hz to 100kHz—and reference soft-start functionality, eliminating large inrush currents and output voltage overshoot at turn-on. The LT3050's output voltage tolerance is highly accurate at ±2% over line, load and temperature. The LT3050's low operating quiescent current of 50µA allows it to idle continuously with

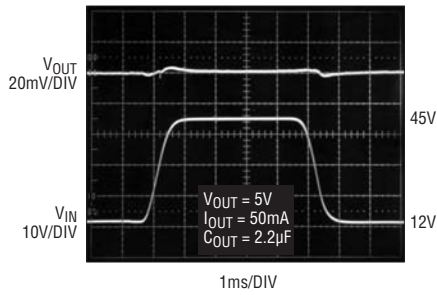Figure 2. New school dashboard; high performance, active multi-antenna system

Figure 3. LT3050 transient response to load dump condition (AC coupled)

minimal battery drain and drops to <1µA in shutdown. The IC is housed in a 12-lead 2mm × 3mm DFN and 12-lead thermally enhanced MSOP packages, respectively, offering a compact footprint.

Single IC Antenna Power Supply with Protection and Diagnostic Features

The 12V car battery, the starting point for many active antenna voltage supplies, is far from the quiet, stable supply required by these systems. In addition to noise, this 12V "supply" can be subjected to reverse battery conditions or load dumps where the voltage can range or spike anywhere from –36V to 80V. The LT3050 protects both itself and the antenna in this demanding electrical environment, while providing a stable, low noise output voltage. The LT3050 also protects active antenna supply circuitry in the event of a short circuit within the antenna supply itself with an accurate and programmable current limit. Thermal conditions in automotive environments are equally challenging, requiring the supply to be stable over a –40 to 125°C temperature range with robust overtemperature protection.

In addition to these difficult protection requirements, the LT3050 simplifies the gathering of diagnostic information required to report antenna status. Programmable open circuit detection monitors the antenna supply current in case it should drop below a specified minimum operating condition. Programmable short circuit detection monitors the antenna supply current in case it should exceed a defined maximum and protects the antenna, and its supply, by limiting

current flow. In addition, an analog current monitor creates a signal proportional to the antenna supply current. This is handy as a diagnostic input, or for signaling the system as to which antenna type is mounted.

Protection Features in an Accurate, Stable and Quiet Power Supply

The LT3050 generates a stable and low noise supply for active antenna systems, isolating and protecting the antenna system from the car's noisy and volatile 12V supply. The IC can withstand input voltages of ±50V and reverse battery conditions potentially generated from the 12V supply as well as output reversals to ±50V (see Figure 3).

The LT3050 provides excellent power supply noise rejection, effectively isolating the antenna supply from noise on the 12V supply line or from an intermediate step-down regulator (see Figure 4). A single capacitor provides both reference soft-start and noise bypass, enabling a programmable start-up time and ultralow noise operation.

A precision programmable current limit provides additional protection by allowing the user to set current limit as low as 110% of maximum load, without affecting load regulation during normal operation. In addition, the combination of a backup current limit, current limit fold-back, and robust thermal shutdown with hysteresis allow for indefinite output shorts from a 50V input supply without damaging the IC. The output can be pulled 50V above the input with minimal cur-
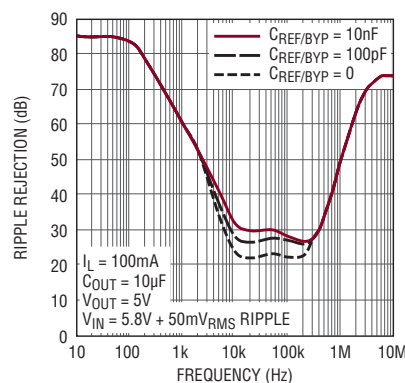
rent flow into the input and without damaging the IC.

Diagnostic Capabilities

The LT3050 provides diagnostic information to the car's control systems. An open-collector fault indicator, capable of sinking 100µA, asserts if open-circuit or short-circuit conditions are detected, or if the IC enters thermal shutdown. The LT3050 also features an integrated current monitor that sources (via the I_{MON} pin) about 1/100 of the output current for use in antenna system monitoring and protection. See the block diagram in Figure 5. Simply connecting a resistor from I_{MON} to GND creates a ground-referenced voltage proportional to output current.

Programmable short-circuit detection and current limit is provided at the I_{MAX} pin and once set, varies less than 5% over line and temperature. The I_{MAX} pin is the collector of a specially designed current mirror device that sources about 1/200 of output current. This pin is also the input to the precision current limit amplifier. Connecting a resistor ($R_{I(MAX)}$) between I_{MAX} and GND sets the short-circuit detection and programmable current limit thresholds. The current limit amplifier circuitry performs two functions. First, it asserts the open-collector $\overline{FAULT}$ pin logic if the I_{MAX} pin voltage reaches 600mV. Second, it regulates the output drive current such that the I_{MAX} pin voltage does not exceed 600mV, thus limiting the output current to 0.6V • $200/R_{I(MAX)}$.

The programmable open-circuit detection threshold is provided at the I_{MIN} pin. The I_{MIN} pin is the collector of a specially designed current mirror device that sources about 1/200 of output current. This pin is also the input to the open-circuit detection comparator, referenced to the 600mV internal reference. Connecting a resistor between I_{MIN} and GND sets the open-circuit detection threshold. If the I_{MIN} pin voltage falls below 600mV, the comparator trips and the $\overline{FAULT}$ pin asserts. The comparator uses a small amount of hysteresis to prevent $\overline{FAULT}$ pin glitches.

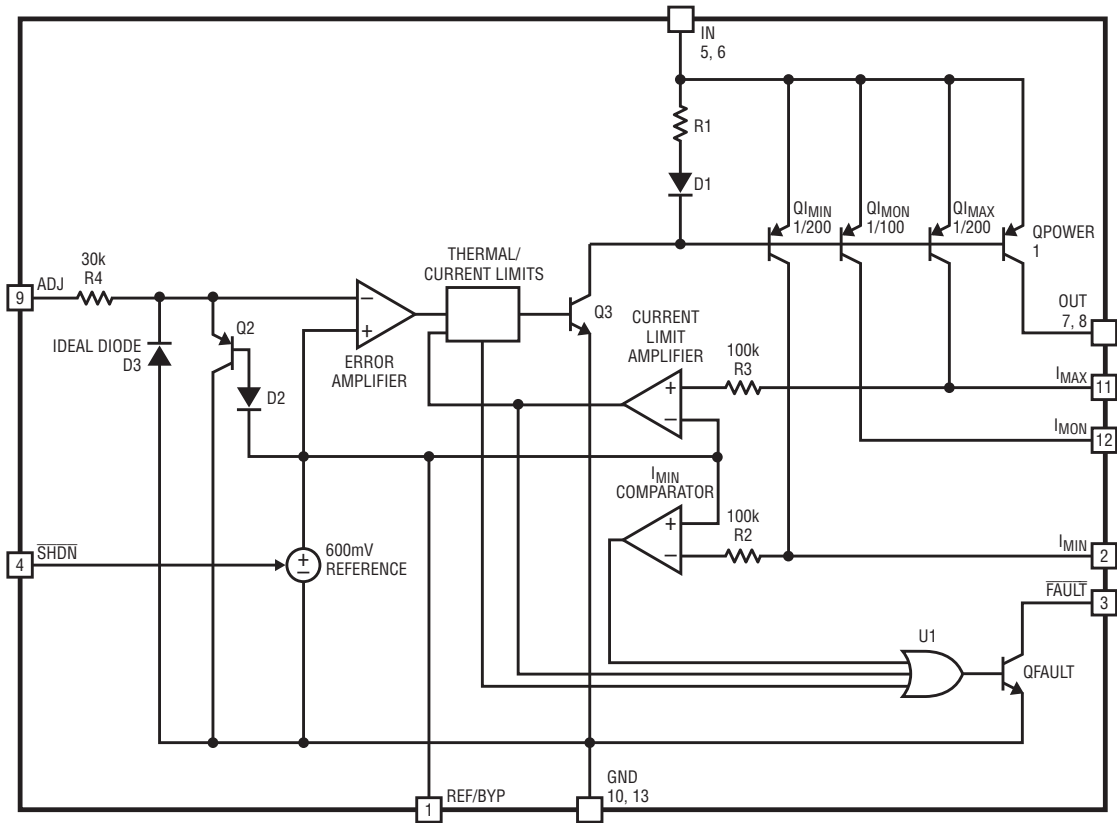**Figure 4. LT3050 ripple rejection**

Figure 5. LT3050 block diagram

Figure 6 shows a typical LT3050 application circuit set up as an active antenna supply. Current limit, open-circuit fault threshold values, output voltage, etc. were chosen arbitrarily for illustrative purposes. In this example, the open circuit detection threshold is set by the 11.3k I_{MIN} resistor to 10mA. The 1.15k I_{MAX} resistor sets the short circuit fault threshold and current limit to 100mA (a 10nF I_{MAX} capacitor is required for current limit amplifier stability). The 3k I_{MON} resistor provides a full-scale 3V signal when output current equals 100mA. The 10nF REF/BYP capacitor provides a

5.5ms soft-start time and low noise operation.

Conclusion

As car infotainment components have grown more complex, the number of active antenna systems has grown as well. Sensitive circuitry in these active antenna systems requires protection and isolation from the harsh automotive environment as well as diagnostic feedback to report antenna status.

The LT3050 active antenna supply and diagnostics linear regulator addresses active antenna design issues with features such as programmable

current limit, soft-start, open-circuit detection, output current monitor, and an open-collector fault signal. The LT3050 also features a wide input voltage range, low quiescent current, low output noise over a wide bandwidth, high output voltage accuracy, low dropout voltage and ability to withstand input and output voltage reversal.

The LT3050's stability and low noise output benefits the end user as well, with clearer and more reliable antenna transmission/receive signals to enhance the modern automotive infotainment experience. *LT*
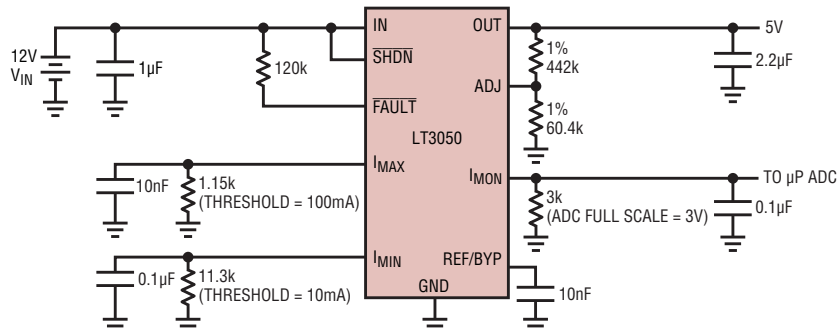

Figure 6. LT3050 active antenna supply circuit

Battery Conditioner Extends the Life of Li-Ion Batteries

by George H. Barbehenn

Introduction

Li-Ion batteries naturally age, with an expected lifetime of about three years, but that life can be cut very short—to under a year—if the batteries are mishandled. It turns out that the batteries are *typically* abused in applications where intelligent conditioning would otherwise significantly extend the battery lifetime. The LTC4099 battery charger and power manager contains an I^2C controlled battery conditioner that maximizes battery operating life, while also optimizing battery run time and charging speed (see Figure 1).

The Underlying Aging Process in Li-Ion Batteries

Modern Li-Ion batteries are constructed of a graphite battery cathode, cobalt, manganese or iron phosphate battery anode and an electrolyte that transports the lithium ions.

The electrolyte may be a gel, a polymer (Li-Ion/Polymer batteries)

or a hybrid of a gel and a polymer. In practice, no suitable polymer has been found that transports lithium ions effectively at room temperature. Most 'pouch' Li-Ion/Polymer batteries are in fact hybrid batteries containing a combination of polymer and gel electrolytes.

The charge process involves lithium ions moving out of the battery cathode material, through the electrolyte and into the battery anode material. Discharging is the reverse process. Both terminals either release or absorb lithium ions, depending on whether the battery is being charged or discharged.

The lithium ions do not bond with the terminals, but rather enter the terminals much like water enters a sponge; this process is called "intercalation." So, as is often the case with charge-based devices such as electrolytic capacitors, the resulting charge storage is a function of both the materials used and the physical structure of the material. In the case of the electrolytic capacitor, the foil is etched to increase its surface area. In the case of the Li-Ion battery the terminals must have a sponge-like physical makeup to accept the lithium ions.

The choice of battery anode material (cobalt, manganese or iron phosphate) determines the capacity, safety and aging properties of the battery. In particular, cobalt provides superior

capacity and aging characteristics, but it is relatively unsafe compared to the other materials. Metallic lithium is flammable and the cobalt battery anode tends to form metallic lithium during the discharge process. If several safety measures fail or are defeated, the resulting metallic lithium can fuel a "vent with flame" event.

Consequently, most modern Li-Ion batteries use a manganese or iron phosphate-based battery anode. The price for increased safety is slightly reduced capacity and increased aging.

Aging is caused by corrosion, usually oxidation, of the battery anode by the electrolyte. This reduces both the effectiveness of the electrolyte in lithium-ion transport and the sponge-like lithium-ion absorption capability of the battery anode. Battery aging results an increase of the battery series resistance (BSR) and reduced capacity, as the battery anode is progressively less able to absorb lithium ions.

The aging process begins from the moment the battery is manufactured and cannot be stopped. However, battery handling plays an important role in how quickly aging progresses.

Conditions that Affect the Aging Process

The corrosion of the battery anode is a chemical process and this chemical process has an activation energy probability distribution function (PDF). The
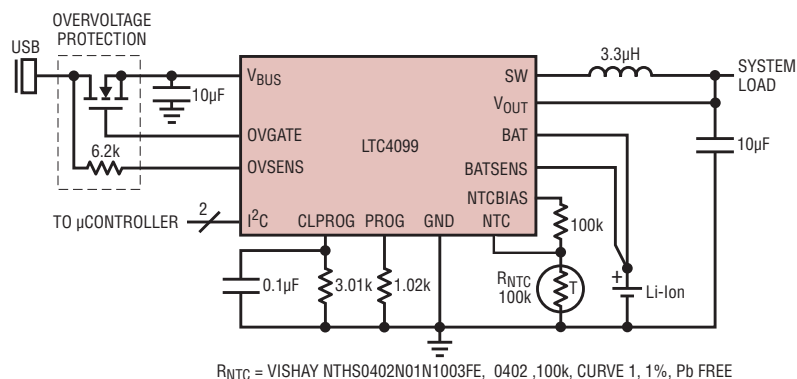
Figure 1. The LTC4099 with I^2C controlled battery conditioner

activation energy can come from heat or the terminal voltage. The more activation energy available from these two sources the greater the chemical reaction rate and the faster the aging.

Li-Ion batteries that are used in the automotive environment must last 10 to 15 years. So, suppliers of automotive Li-Ion batteries do not recommend charging the batteries above 3.8V. This does not allow the use of the full capacity of the battery, but is low enough on the activation energy PDF to keep corrosion to a minimum. The iron phosphate battery anode has a shallower discharge curve, thus retaining more capacity at 3.8V.

Battery manufacturers typically store batteries at 15°C (59°F) and a 40% state of charge (SoC), to minimize aging. Ideally, storage would take place at 4% or 5% SoC, but it must never reach 0%, or the battery may be damaged. Typically, a battery pack protection IC prevents a battery from reaching 0% SoC. But pack protection cannot prevent self-discharge and the pack protection IC itself consumes some current. Although Li-Ion batteries have less self-discharge than most other secondary batteries, the storage time is somewhat open-ended. So, 40% SoC represents a compromise between minimizing aging and preventing damage while in storage (see Figure 2).

In portable applications, the reduction in capacity from such a reduced SoC strategy is viewed negatively in marketing specifications. But it is sufficient to detect the combination
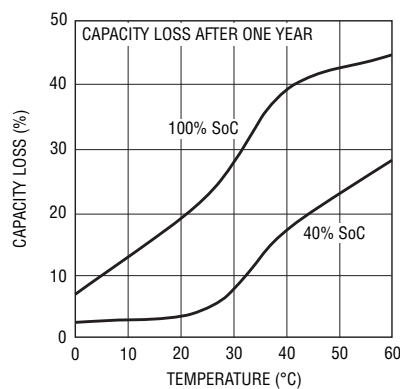

Figure 2. Yearly capacity loss vs temperature and SoC for Li-Ion batteries

of high ambient heat and high battery SoC to implement an algorithm that minimizes aging while ensuring maximum capacity availability to the user.

Battery Conditioner Avoids Conditions that Accelerate Aging

The LTC4099 has a built-in battery conditioner that can be enabled or disabled (default) via the I^2C interface. If the battery conditioner is enabled and the LTC4099 detects that the battery temperature is higher than ~60°C, it gently discharges the battery to minimize the effects of aging. The LTC4099 NTC temperature measurement is always on and available to monitor the battery temperature. This circuit is a micropower circuit, drawing only 50nA while still providing full functionality.
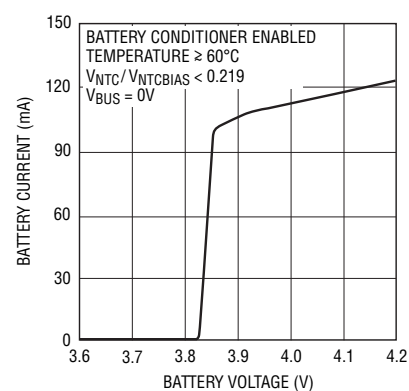

Figure 3. Battery discharge current vs voltage for the LTC4099 battery conditioning function

The amount of current used to discharge the battery follows the curve shown in Figure 3, reaching zero when the battery terminal voltage is ~3.85V. If the temperature of the battery pack drops below ~40°C and a source of energy is available, the LTC4099 once again charges the battery. Thus, the battery is protected from the worst-case battery aging conditions.

Conclusion

Although the aging of Li-Ion batteries cannot be stopped, the LTC4099's battery conditioner ensures maximum battery life by preventing the battery-killing conditions of simultaneous high voltage and high temperature. Further, the micropower, always on NTC monitoring circuit ensures that the battery is protected from life-threatening conditions at all times. *LT*

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lines used by the LTC2175, and allows it to be packaged in a space saving 7mm × 8mm QFN package.

The dual version of the LTC2262 is the LTC2268. It dissipates 299mW of total power, or 150mW per ADC. It also has LVDS serial output lines that reduce space, and allow the LTC2268 to be in a 6mm × 6mm QFN package.

The dual and quad versions of LTC2262 are available in 12- and 14-bit versions, in speed grades from 25Msps up to 125Msps. A complete list of the variant is shown in Table 1.

Each device shares the excellent AC performance of the LTC2262, and features better than 90dB of channel-to-channel isolation. The serial outputs of the multiple channel parts mitigate the effect of digital feedback, producing a clean output spectrum. In sum, the performance of LTC2262 is not sacrificed when migrating into multiple channel parts.

Conclusion

The LTC2262 ultralow-power ADC simplifies design with a unique combi-

nation of features. Digital noise can be reduced by using DDR LVDS signaling, alternate bit polarity mode, or the data randomizer. The number of data lines needed to transmit 14 bits of data can be reduced to seven with DDR CMOS signaling, which simplifies layout. The LTC2262 is part of a pin-compatible family of 12-bit and 14-bit ADCs with sample rates from 25Msps to 150Msps, with power consumption ranging from 35mW at 25Msps up to 149mW at 150Msps while maintaining excellent AC performance characteristics. *LT*

EMI Certified Step-Down Converter in 15mm × 9mm µMPackage Produces 1A, 0.8V$_{OUT}$ –10V$_{OUT}$ from 3.6V$_{IN}$ – 36V$_{IN}$

by David Ng

Introduction

The LTM8031 is a low noise DC/DC step-down µModule regulator that operates from input voltages from 3.6V to 36V and is independently certified to be compliant with the stringent requirements of EN55022 class B. Its output can be programmed to provide voltages from 0.8V to 10V at up to 1A. A nearly complete converter solution is contained in the 15mm × 9mm × 2.82mm package. As seen in Figure 1, the LTM8031 just requires one resistor to set the output voltage, another resistor to set the operating frequency, and some input and output capacitance.

LTM8031 Features

The LTM8031 comes with many of the features often required in modern power supplies. It can be sequenced via its RUN/SS pin, which also serves to allow the user to control the output behavior at turn on. A PGOOD pin indicates when the output is within 10% of the target regulation voltage. The SYNC pin is used to synchronize the LTM8031 to a desired system frequency.
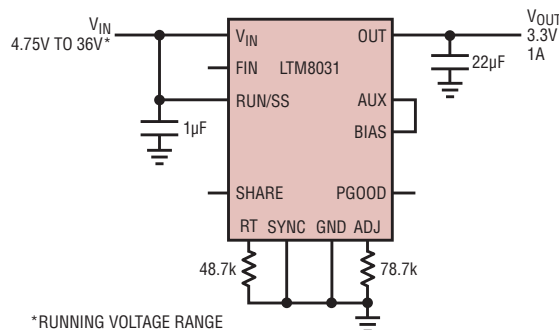
Figure 1. The LTM8031 needs just two resistors and some capacitance to get it running.

Table 1. Low noise µModule DC/DC step down converters

Product	V$_{IN}$ Range	V$_{OUT}$ Range	I$_{LOAD(MAX)}$
LTM8020	4V to 36V	1.25V to 5V	200mA
LTM8021	3.6V to 36V	0.8V to 5V	500mA
LTM8031	3.6V to 36V	0.8V to 10V	1A
LTM8032	3.6V to 36V	0.8V to 10V	2A

Through the incorporation of a high Q pi filter and electromagnetic interference reduction design techniques, the LTM8031 is purpose built with low radiated emissions in mind. It has been independently verified to be compliant with EN55022:2006 (Information Technology Equipment – Radio Disturbance Characteristics – Limits and Methods of Measurement). EN55022 has two classes, A and B. The LTM8031 is certified compliant with class B, the more stringent of the two. More than that, the LTM8031 beats the
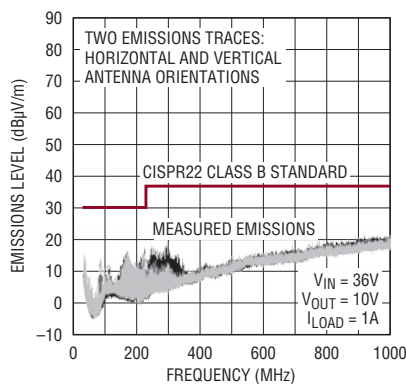
Figure 2. The LTM8031 meets EN55022 Class B while producing 10V$_{OUT}$ at 1A from 36V$_{IN}$.
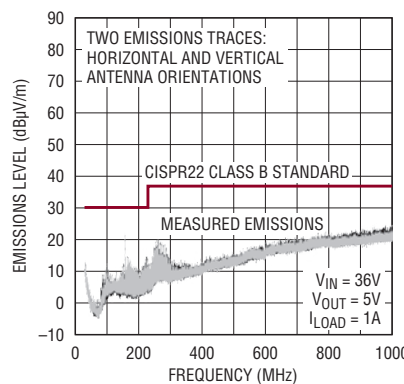
Figure 3. The LTM8031 is EN55022 Class B compliant with 5V$_{OUT}$ at 1A from 36V$_{IN}$.
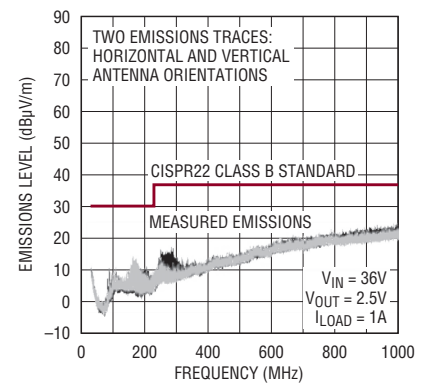
Figure 4. The LTM8031 beats the EN55022 Class B limits by a wide margin with 2.5V$_{OUT}$ at 1A from 36V$_{IN}$.

Using a Differential I/O Amplifier in Single-Ended Applications

<div align="right">by Glen Brisebois</div>

Introduction

Recent advances in low voltage silicon germanium and BiCMOS processes have allowed the design and production of very high speed amplifiers. Because the processes are low voltage, most of the amplifier designs have incorporated differential inputs and outputs to regain and maximize total output signal swing. Since many low voltage applications are single-ended, the questions arise, "How can I use a differential I/O amplifier in a single-ended application?" and "What are the implications of such use?" This article addresses some of the practical implications and demonstrates specific single-ended applications using the 3GHz gain-bandwidth LTC6406 differential I/O amplifier.

Background

A conventional op amp has two differential inputs and an output. The gain is nominally infinite, but control is maintained by virtue of feedback from the output to the negative "inverting" input. The output does not go to infinity, but rather the differential input is kept to zero (divided by infinity, as it were). The utility, variety and beauty of conventional op amp applications are well documented, yet still appear inexhaustible. Fully differential op amps have been less well explored.

Figure 1 shows a differential op amp with four feedback resistors. In this case the differential gain is still nominally infinite, and the inputs kept together by feedback, but this is not adequate to dictate the output voltages. The reason is that the common mode output voltage can be anywhere and still result in a "zero" differential input voltage because the feedback is symmetric. Therefore, for any fully differential I/O amplifier, there is always another control voltage to dictate the output common mode voltage. This is the purpose of the V_{OCM} pin, and explains why fully dif-
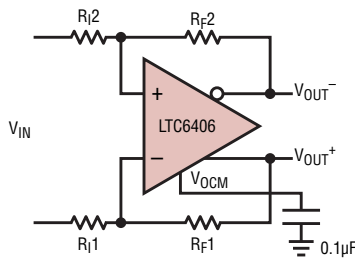

Figure 1. Fully differential I/O amplifier showing two outputs and an additional V_{OCM} pin

ferential amplifiers are at least 5-pin devices (not including supply pins) rather than 4-pin devices. The differential gain equation is $V_{OUT(DM)} = V_{IN(DM)} \cdot R2/R1$. The common mode output voltage is forced internally to the voltage applied at V_{OCM}. One final observation is that there is no longer a single inverting input: both inputs are inverting and noninverting depending on which output is considered. For the purposes of circuit analysis, the inputs are labeled with "+" and "–" in the conventional manner and one output receives a dot, denoting it as the inverted output for the "+" input.

Anybody familiar with conventional op amps knows that noninverting applications have inherently high input impedance at the noninverting input,
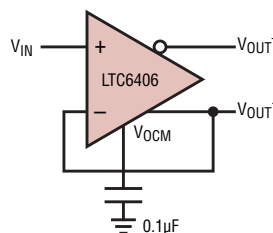
approaching GΩ or even TΩ. But in the case of the fully differential op amp in Figure 1, there is feedback to both inputs, so there is no high impedance node. Fortunately this difficulty can be overcome.

Simple Single-Ended Connection of a Fully Differential Op amp

Figure 2 shows the LTC6406 connected as a single-ended op amp. Only one of the outputs has been fed back and only one of the inputs receives feedback. The other input is now high impedance.

The LTC6406 works fine in this circuit and still provides a differential output. However, a simple thought experiment reveals one of the downsides of this configuration. Imagine that all of the inputs and outputs are sitting at 1.2V, including V_{OCM}. Now imagine that the V_{OCM} pin is driven an additional 0.1V higher. The only output that can move is V_{OUT}^- because V_{OUT}^+ must remain equal to V_{IN}, so in order to move the common mode output higher by 100mV the amplifier has to move the V_{OUT}^- output a total of 200mV higher. That's a 200mV differential output shift due to

Figure 2. Feedback is single-ended only. This circuit is stable, with a Hi-Z input like the conventional op amp. the closed loop output (V_{OUT}^+ in this case) is low noise. Output is best taken single-ended from the closed loop output, Providing a 3dB bandwidth Of 1.2GHz. The Open Loop Output (V_{OUT}^-) has a noise gain of two from V_{OCM}, but is well behaved to about 300MHz, above which it has significant passband ripple.
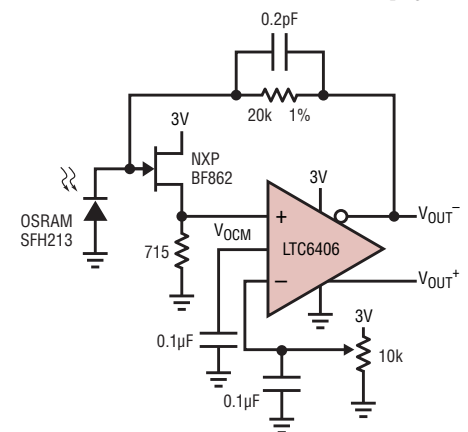

Figure 3. Transimpedance amplifier. Ultralow noise JFET buffers the current noise of the bipolar LTC6406 input trim the pot for 0V differential output under no-light conditions.

Dual Output µModule DC/DC Regulator Produces High Efficiency 4A Outputs from a 4.5V to 26.5V Input

by Alan Chern

Dual System-in-a-Package Regulator

Systems and PC boards that use FP-GAs and ASICs are often very densely populated with components and ICs. This dense real estate (especially the supporting circuitry for FPGAs, such as DC/DC regulators) puts a burden on system designers who aim to simplify layout, improve performance and reduce component count. A new family of DC/DC µModule regulator systems with multiple outputs is designed to dramatically reduce the number of components and their associated costs. These regulators are designed to eliminate layout errors and to offer a ready-made complete solution. Only a few external components are needed since the switching controllers, power MOSFETs, inductors, compensation and other support components are all integrated within the compact surface mount 15mm × 15mm × 2.82mm LGA package. Such easy layout saves board space and design time by implementing high density point-of-load regulators.

The LTM4619 switching DC/DC µModule converter regulates two 4A outputs from a single wide 4.5V to 26.5V input voltage range. Each out-
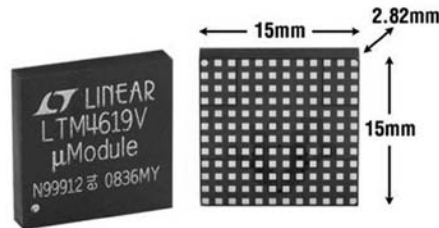

Figure 1. The LTM4619 LGA package is only 15mm × 15mm × 2.82mm, yet it houses dual DC/DC switching circuitry, inductors, MOSFETs and support components.

put can be set between 0.8V and 5V with a single resistor. In fact, only a few components are needed to build a complete circuit (see Figure 2).

Figure 2 shows the LTM4619 µModule regulator in an application with 3.3V and 1.2V outputs. The out-

put voltages can be adjusted with a value change in RSET1 and RSET2. Thus, the final design requires nothing more than a few resistors and capacitors. Flexibility is achieved by pairing outputs, allowing the regulator to form different combinations such as single input/dual independent outputs or single input/parallel single output for higher maximum current output.

The efficiency of the system design for Figure 2 is shown in Figure 3 and power loss is shown in Figure 4, both at various input voltages. Efficiency at light load operation can be improved with selective pulse-skipping mode or Burst Mode® operation by tying the mode pin high or leaving it floating.
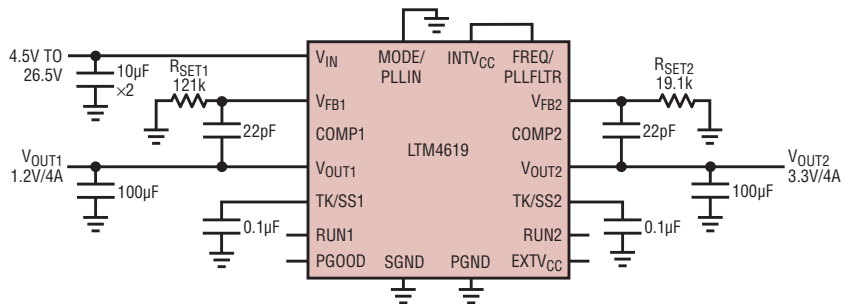
Figure 2. µModule regulator converts a 4.5V to 26.5V input to dual 3.3V and 1.2V outputs, each with 4A maximum output current.

Figure 3. Efficiency of the circuit in Figure 2 at different input voltage ranges for 3.3V and 1.2V outputs

Figure 4. Power loss of the circuit in Figure 2 at different input voltages for 3.3V and 1.2V outputs

Figure 5. Exceptional thermal performance of a paralleled output LTM4619 µModule regulator (12V$_{IN}$ with two channels paralleled to 1.5V$_{OUT}$ at 8A load)

All-in-One Power for Portables:
Single IC Replaces Battery Charger, Pushbutton Controller, LED Driver and Five Voltage Regulator ICs   by Marty Merchant
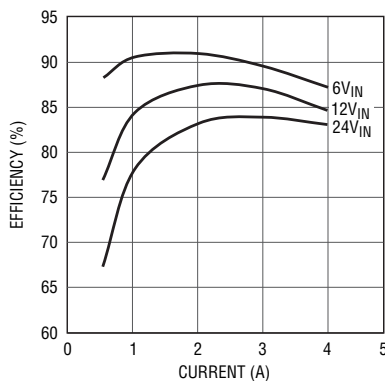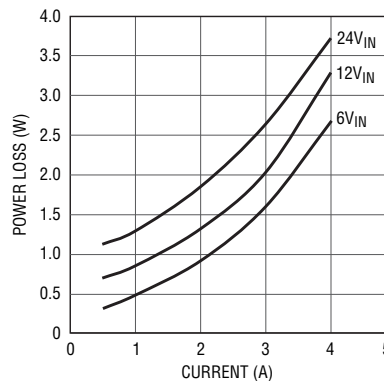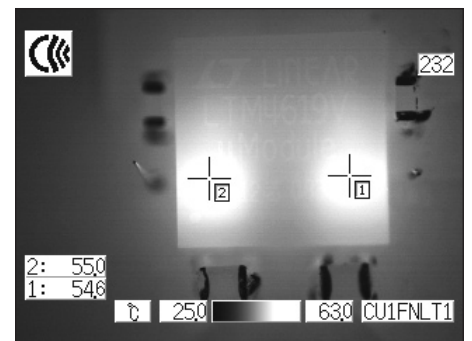
Introduction

The LTC3577/LTC3577-1 integrates a number of portable device power management functions into one IC, reducing complexity, cost and board area in handheld devices. The major functions include:

❑ Five voltage regulators to power memory, I/O, PLL, CODEC, DSP or a touch-screen controller

❑ A battery charger and PowerPath™ manager

❑ An LED driver for backlighting an LCD display, keypad and/or buttons

❑ Pushbutton control for debouncing the on/off button, supply sequencing and allowing end-users to force a hard reset when the microcontroller is not responding

By combining these functions, the LTC3577/LTC3577-1 does more than just reduce the number of required ICs; it solves the problems of functional interoperability—where otherwise separate features operate together for improved end-product performance. For instance, when the power input is from USB, the limited input current is logically distributed among the power supply outputs and the battery charger.

The LTC3577/LTC3577-1 offers other important features, including PowerPath control with instant-on operation, input overvoltage protection for devices that operate in harsh environments and adjustable slew rates on the switching supplies, making it possible to reduce EMI while optimizing efficiency. The LTC3577-1 features a 4.1V battery float voltage for improved battery cycle life and additional high temperature safety margin, while the LTC3577 includes a standard 4.2V battery float voltage for maximum battery run time.

Pushbutton Control

The built in pushbutton control circuitry of the LTC3577/LTC3577-1 eliminates the need to debounce the pushbutton and includes power-up sequence functionality. A PB Status output indicates when the pushbutton is depressed, allowing the microprocessor to alter operation or begin the power-down sequence. Holding the pushbutton down for five seconds produces a hard reset. The hard reset shuts down the three bucks, the two LDOs and the LED driver, allowing the user to power down the device when the microprocessor is no longer responding.

Battery, USB, Wall and High Voltage Input Sources

The LTC3577/LTC3577-1 is designed to direct power from two power supply inputs and/or a Li-Ion/Polymer battery. The V_{BUS} input has selectable input current limit control, designed to deliver 100mA or 500mA for USB applications, or 1A for higher power applications. A high power voltage source such as a 5V supply can be connected via an externally controlled FET. The voltage control (V_C) pin can be used to regulate the output of a high voltage buck, such as the LT3480, LT3563 or LT3505 at a voltage slightly above the battery for optimal battery charger efficiency.

Figure 1 shows a system block diagram of the LTC3577/LTC3577-1. An overvoltage protection circuit enables one or both of the input supplies to be protected against high voltage surges. The LTC3577/LTC3577-1 can provide power from a 4.2V/4.1V Li-Ion/Polymer battery when no other power is available or when the V_{BUS} input current limit has been exceeded.
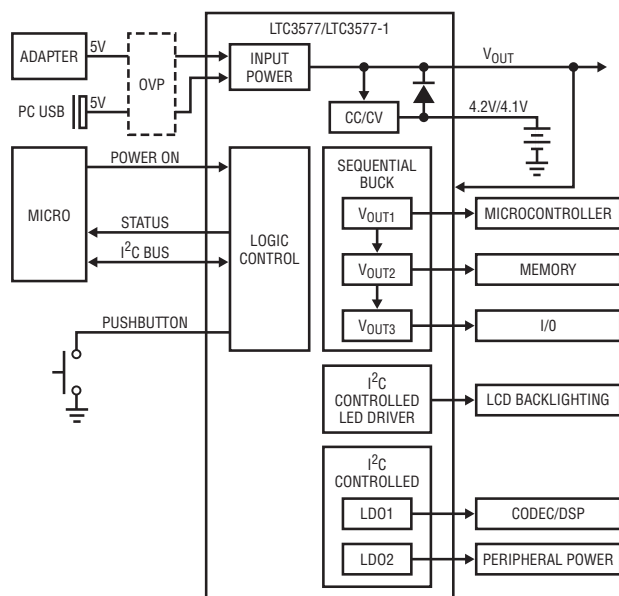
Figure 1. Portable device power distribution block diagram featuring the LTC3577/LTC3577-1

Battery Charger

The LTC3577/LTC3577-1 battery charger can provide a charge current up to 1.5A via V_{BUS} or wall adapter when available. The charger also has an automatic recharge and a trickle charge function. The battery charge/ no-charge status, plus the NTC status can be read via the I[2]C bus. Since Li-Ion/Polymer batteries quickly lose capacity when both hot and fully charged, the LTC3577/LTC3577-1 reduces the battery voltage when the battery heats up, extending battery life and improving safety.

Three Bucks, Two LDOs and a Boost/LED Driver

The LTC3577/LTC3577-1 contains five resistor-adjustable step-down regulators: two bucks, which can provide up to 500mA each, a third buck, which can provide up to 800mA, and two LDO regulators, which provide up to 150mA each and are enabled via the I[2]C interface. Individual LDO supply inputs allow the regulators to be connected to low voltage buck regulator outputs to improve efficiency. All regulators are capable of low voltage operation, adjustable down to 0.8V.

The three buck regulators are sequenced at power up (V_{OUT1}, V_{OUT2} then V_{OUT3}) via the pushbutton controller or via a static input pin. Each buck can be individually selected to run in Burst Mode operation to optimize efficiency or pulse-skipping mode for lower output ripple at light loads.
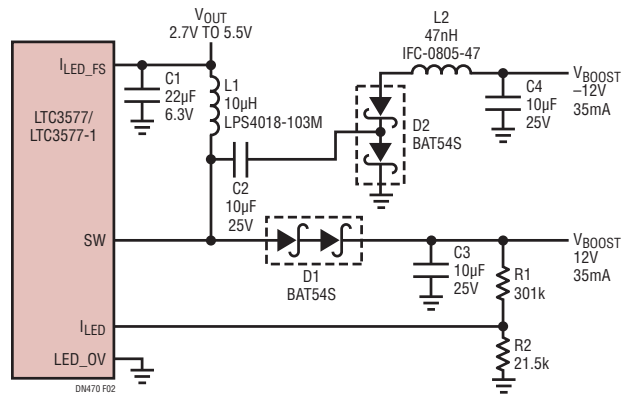

Figure 2. Dual polarity boost converter

A patented switching slew rate control feature, set via the I[2]C interface, allows the reduction of EMI noise in exchange for efficiency.

The LTC3577/LTC3577-1 LED boost driver can be used to drive up to 10 series white LEDs at up to 25mA or be configured as a constant voltage boost converter. As a LED driver, the current is controlled by a 6-bit, 60dB logarithmic DAC, which can be further reduced via internal PWM control. The LED current smoothly ramps up and down at one of four different rates. Overvoltage protection prevents the internal power transistor from damage if an open circuit fault occurs. Alternatively, the LED boost driver can be configured as a fixed voltage boost, providing up to 0.75W at 36V.

Many circuits require a dual polarity voltage to bias op amps or other analog devices. A simple charge pump circuit,

as shown in Figure 2, can be added to the boost converter switch node to provide a dual polarity supply. Two forward diodes are used to account for the two diode voltage drops in the inverting charge pump circuit and provide the best cross-regulation. For circuits where cross-regulation is not important, or with relatively light negative loads, using a single forward diode for the boost circuit provides the best efficiency.

Conclusion

The high level of integration of the LTC3577/LTC3577-1 reduces the number of components, required board real estate and overall cost of power systems for portable electronics. It greatly simplifies power path design with built-in solutions to a number of complex power flow logic and control problems. **LT**

Multiphase Operation

For a 4-phase, 4-rail output voltage system, use two LTM4619s and drive their MODE_PLLIN pins with a LTC6908-2 oscillator, such that the two µModule devices are synchronized 90° out of phase. Reference Figure 21 in the LTM4619 data sheet. Synchronization also lowers voltage ripple, reducing the need for high voltage capacitors whose bulk size consumes board space. The design delivers four different output voltage rails (5V, 3.3V, 2.5V and 1.8V) all with 4A maximum load.

Thermal Performance

Exceptional thermal performance is shown in Figure 5 where the unit is operating in parallel output mode; single 12VIN to a single 1.5VOUT at 8A. Both outputs tied together create a combined output current of 8A with both channels running at full load (4A each). Heat dissipation is even and minimal, yielding good thermal results. If additional cooling is needed, add a heat sink on top of the part or use a metal chassis to draw heat away.

Conclusion

The LTM4619 dual output µModule regulator makes it easy to convert a wide input voltage range (4.5V to 26.5V) to two or more 4A output voltage rails (0.8V to 5V) with high efficiency and good thermal dissipation. Simplicity and performance are achieved through dual output voltage regulation from a single package, making the LTM4619 an easy choice for system designs needing multiple voltage rails. **LT**

Maximize the Performance of 16-Bit, 105Msps ADC with Careful IF Signal Chain Design
by Clarence Mayott and Derek Redmayne

Introduction

Modern communication systems require an ADC to receive an analog signal and then convert it into a digital signal that can be processed with an FPGA. The job of a mixed signal engineer is to optimize the signal at the input of the ADC to maximize overall system performance. This usually requires a signal chain comprised of multiple gain and filtering sections. An ADC is only as good as the signal it is measuring.

For instance, the LTC2274 provides excellent AC performance with an appropriate IF signal chain. The LTC2274 is a 16-bit, 105Msps ADC that serially transmits 8B/10B encoded output data compliant with the JESD204 specification. It uses a single differential transmission line pair to reduce the number of IO lines
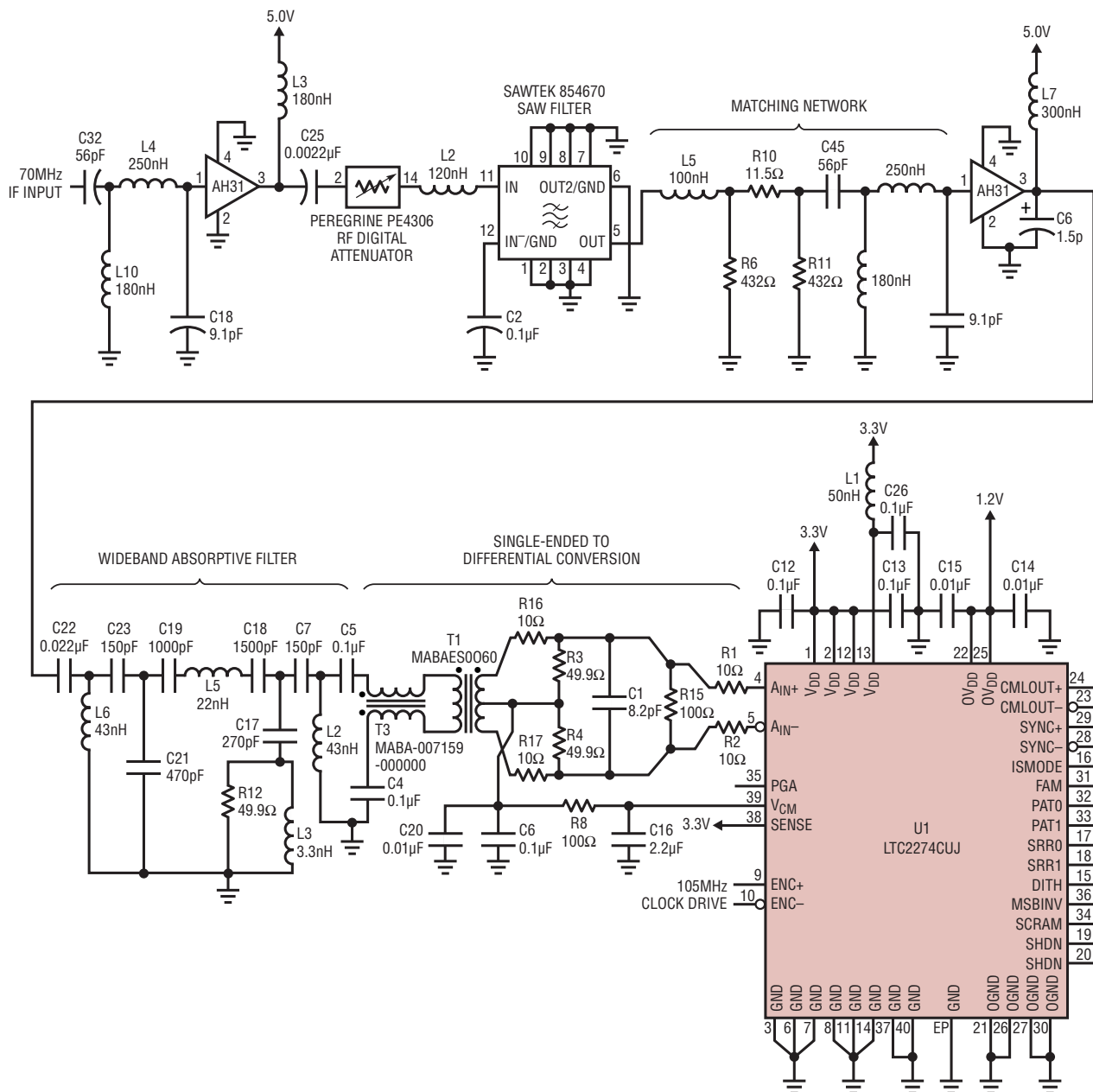

Figure 1. IF receiver chain

required to transmit output data. The LTC2274 has 77dB of SNR, and 100dB of spurious free dynamic range.

Signal Chain Topology

Figure 1 details a signal chain optimized for a 70MHz center frequency and a 20MHz bandwidth driving the LTC2274. The final filter and circuitry around the ADC are shown in detail. The earlier stages of the chain can be changed to suit a target application.

The first stage of amplification in the chain uses an AH31 from TriQuint Semiconductor. This GaAs FET amplifier offers a low noise figure and high IP3 point, which minimizes distortion caused by the amplifier stage. It provides 14dB of gain over a wide frequency region. The high IP3 prevents intermodulation distortion between frequencies outside the passband of the surface acoustic wave (SAW) filter.

A SAW filter follows the amplification stage for band selection. The SAW filter offers excellent selectivity and a flat passband if matched correctly. Gain before the SAW must not be
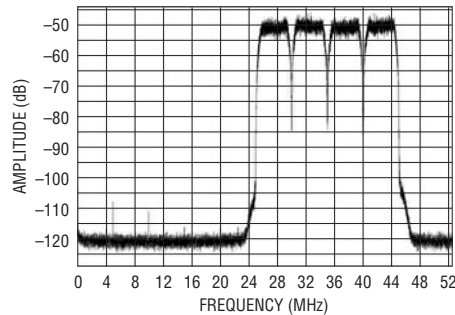

Figure 2. Typical spread spectrum performance

higher than the maximum input power rating of the SAW; otherwise it leads to distortion. A digitally controlled step attenuator may be required in the signal path to control the power going into the SAW filter.

The second stage of amplification is used to recover the loss in the SAW filter. The insertion loss of the SAW filter is about –15dB, so the final amplifier should have at least this much gain, plus enough gain to accommodate the final filter. By splitting the gain between two amplifiers, the noise and distortion can be optimized without overdriving the SAW filter. It also allows for a final filter with better suppres-

sion of noise from the final amplifier, improving SNR and selectivity.

The output stage of the final filter needs to be absorptive to accommodate the ADC front end. This suppresses glitches reflected back from the direct sampling process.

This signal chain will not degrade the performance of the LTC2274. When receiving a 4-channel WCDMA signal with a 20MHz bandwidth, centered at 70MHz, the ACPR is 71.5dB (see Figure 2).

Conclusion

The LTC2274 can be used to receive high IF frequencies, but getting the most out of this high performance ADC requires a carefully designed analog front end. The performance of the LTC2274 is such that it is possible to dispense with the automatic gain control and build a receiver with a low fixed gain. The LTC2274 is a part of a family of 16-bit converters that range in sample rate from 65Msps to 105Msps. For complete schematics of this receiver network, visit www. linear.com. ⨆⨅

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a 100mV V_{OCM} shift. This illustrates the fact that single-ended feedback around a fully differential amplifier introduces a noise gain of two from the V_{OCM} pin to the "open" output. In order to avoid this noise, simply do not use that output, resulting in a fully single-ended application. Or, you can take the slight noise penalty and use both outputs.

A Single-Ended Transimpedance Amplifier

Figure 3 shows the LTC6406 connected as a single-ended transimpedance amplifier with 20kΩ of transimpedance gain. The BF862 JFET buffers the LTC6406 input, drastically reducing the effects of its bipolar input transistor current noise. The V_{GS} of the JFET is now included as an offset, but this is typically 0.6V so the circuit still functions well on a 3V single supply and
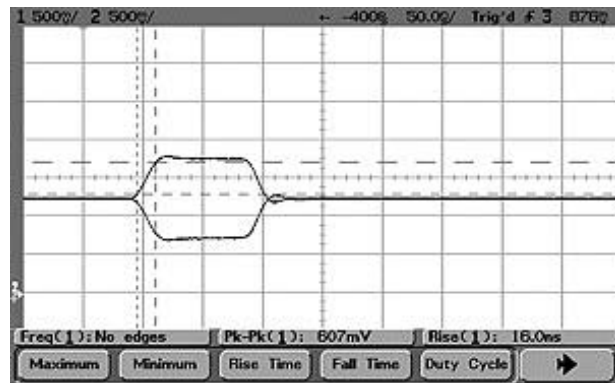
Figure 4. Time domain response of circuit of Figure 3, showing both outputs each with 20kΩ of TIA gain. Rise time is 16ns, indicating a 20MHz bandwidth.

the offset can be dialed out with the 10k potentiometer. The time domain response is shown in Figure 4. Total output noise on 20MHz bandwidth measurements shows $0.8mV_{RMS}$ on $V_{OUT}+$ and $1.1mV_{RMS}$ on $V_{OUT}-$. Taken differentially, the transimpedance gain is 40kΩ.

Conclusion

New families of fully differential op amps like the LTC6406 offer unprecedented bandwidths. Fortunately, these op amps can also function well in single-ended and 100% feedback applications. ⨆⨅

New Device Cameos

Low Voltage Hot Swap Controllers Provide Extended Fault Timers

The LTC4215-2 and LTC4215-3 are low voltage Hot Swap™ controllers with onboard ADCs and I^{2}C compatible interfaces. Functionally, the LTC4215-2 and LTC4215-3 are similar to the LTC4215 and LTC4215-1, respectively, with the overcurrent fault timers extended from 20µs to 420µs.

Some Hot Swap applications require more than the 20µs overcurrent fault filter time provided by the LTC4215 and LTC4215-1. For example, some loads draw brief surge currents and fast input voltage steps cause high transient charging currents into bulk output capacitance. Increasing the overcurrent fault filter time from 20µs to 420µs allows applications to ride out such current surges, while still turning off before MOSFET safe operating area limits have been reached.

The LTC4215-2 also defaults to auto-retry after experiencing an overcurrent fault, making the LTC4215-2 the only part in the LTC4215 family that will auto-retry by default after an overcurrent fault.

The LTC4215-2 and LTC4215-3 work in applications from 12V (with transients to 24V) down to 3.3V and are available in 4mm × 5mm QFN packages.

Isolated RS485 µModule Transceiver Integrates Isolated Power

The LTM2881 is an isolated RS485 µModule transceiver that guards against large ground-to-ground differentials and common mode transients. In practical RS485 systems, ground potentials vary widely from node to node, often exceeding the tolerable range, which can result in an interruption of communications or destruction of a transceiver. The LTM2881 breaks ground loops by isolating the logic level interface and line transceiver using internal inductive signal isolation that allows for a much larger common mode voltage range plus superior common mode rejection of >30kV/µs. A low EMI DC/DC converter powers the transceiver and provides an isolated 5V supply output for powering any supporting external components. With 2,500V$_{RMS}$ of galvanic isolation, onboard secondary power and a fully compliant RS485 transmitter and receiver, the LTM2881 requires no external components, ensuring a complete, compact µModule solution for isolated serial data communications.

Two versions of the LTM2881 are available for 3.3V and 5V input supplies, in low profile 11.25 × 15mm × 2.8mm surface mount LGA and BGA packages. *LT*

EN55022B limits by a wide margin, better than 20dB in some bands. This is shown in Figures 2, 3 and 4, where the LTM8031 is operated from 36V$_{IN}$ to produce 10V$_{OUT}$, 5V$_{OUT}$ and 2.5V$_{OUT}$ at 1A, respectively. The 36V$_{IN}$, 10V$_{OUT}$ at 1A configuration is a worst case radiated emissions scenario, because the LTM8031 is operating with both maximum rated switching voltage and output power.

The LTM8031 is rated to provide 1A, but what about other load currents? Linear Technology offers three other EN55022 class B compliant µModule DC/DC converters, as well: the LTM8020 for 200mA loads, the LTM8021 for 500mA, and the LTM8032 for 2A loads. These are summarized in Table 1, and the worst case emissions for each are given in Figures 5, 6, and 7, respectively

Conclusion

It is not uncommon to have to design a power system that requires numerous power rails at different load currents, low radiated emissions, and small size. For ease of design, take a look at the LTM8031 and its family of low noise µModule DC/DC step-down converters. *LT*
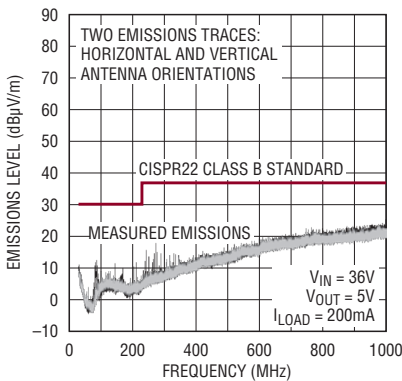

Figure 5. The LTM8020 is our quietest EMC µModule converter, providing 5V at 200mA from 36V$_{IN}$.
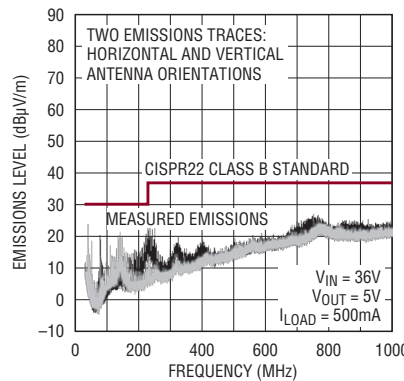

Figure 6. The LTM8021 is another EN55022B compliant device, capable of outputting 5V at 500mA from 36V$_{IN}$.
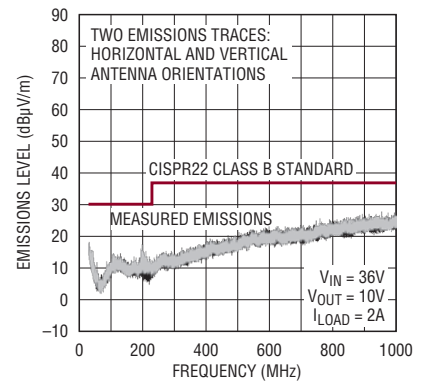

Figure 7. The LTM8032, weighing in at 10V$_{OUT}$ at 2A from 36V$_{IN}$, meets EN55022 class B.

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Fax: (713) 463-5009

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ASIA

AUSTRALIA / NEW ZEALAND
Linear Technology Corporation
133 Alexander Street
Crows Nest NSW 2065
Australia
Tel: +61 (0)2 9432 7803
Fax: +61 (0)2 9439 2738

CHINA
Linear Technology Corp. Ltd.
Units 1503-04, Metroplaza
Tower 2
223 Hing Fong Road
Kwai Fong, N.T., Hong Kong
Tel: +852 2428-0303
Fax: +852 2348-0885

Linear Technology Corp. Ltd.
Room 2701, City Gateway
No. 398 Cao Xi North Road
Shanghai, 200030, PRC
Tel: +86 (21) 6375-9478
Fax: +86 (21) 5465-5918

Linear Technology Corp. Ltd.
Room 816, 8/F
China Electronics Plaza B
No. 3 Dan Ling Rd., Hai Dian
District
Beijing, 100080, PRC
Tel: +86 (10) 6801-1080
Fax: +86 (10) 6805-4030

Linear Technology Corp. Ltd.
Room 2604, 26/F
Excellence Times Square Building
4068 YiTian Road, Futian District
Shenzhen, 518048, PRC
Tel: +86 755-8236-6088
Fax: +86 755-8236-6008

JAPAN
Linear Technology KK
8F Shuwa Kioicho Park Bldg.
3-6 Kioicho Chiyoda-ku
Tokyo, 102-0094, Japan
Tel: +81 (3) 5226-7291
Fax: +81 (3) 5226-0268

Linear Technology KK
6F Kearny Place Honmachi Bldg.
1-6-13 Awaza, Nishi-ku
Osaka-shi, 550-0011, Japan
Tel: +81 (6) 6533-5880
Fax: +81 (6) 6543-2588

Linear Technology KK
7F, Sakuradori Ohtsu KT Bldg.
3-20-22 Marunouchi, Naka-ku
Nagoya-shi, 460-0002, Japan
Tel: +81 (52) 955-0056
Fax: +81 (52) 955-0058

KOREA
Linear Technology Korea Co., Ltd.
Yundang Building, #1002
Samsung-Dong 144-23
Kangnam-Ku, Seoul 135-090
Korea
Tel: +82 (2) 792-1617
Fax: +82 (2) 792-1619

SINGAPORE
Linear Technology Pte. Ltd.
507 Yishun Industrial Park A
Singapore 768734
Tel: +65 6753-2692
Fax: +65 6752-0108

TAIWAN
Linear Technology Corporation
8F-1, 77, Nanking E. Rd., Sec. 3
Taipei, Taiwan
Tel: +886 (2) 2505-2622
Fax: +886 (2) 2516-0702

EUROPE

FINLAND
Linear Technology AB
Teknobulevardi 3-5
P.O. Box 35
FIN-01531 Vantaa
Finland
Tel: +358 (0)46 712 2171
Fax: +358 (0)46 712 2175

FRANCE
Linear Technology S.A.R.L.
Parc Tertiaire Silic
2 Rue de la Couture, BP10217
94518 Rungis Cedex
France
Tel: +33 (1) 56 70 19 90
Fax: +33 (1) 56 70 19 94

GERMANY
Linear Technology GmbH
Osterfeldstrasse 84, Haus C
D-85737 Ismaning
Germany
Tel: +49 (89) 962455-0
Fax: +49 (89) 963147

Linear Technology GmbH
Haselburger Damm 4
D-59387 Ascheberg
Germany
Tel: +49 (2593) 9516-0
Fax: +49 (2593) 951679

Linear Technology GmbH
Jesinger Strasse 65
D-73230 Kirchheim/Teck
Germany
Tel: +49 (0)7021 80770
Fax: +49 (0)7021 807720

ITALY
Linear Technology Italy Srl
Orione 3, C.D. Colleoni
Via Colleoni, 17
I-20041 Agrate Brianza (MI)
Italy
Tel: +39 039 596 5080
Fax: +39 039 596 5090

SWEDEN
Linear Technology AB
Electrum 204
Isafjordsgatan 22
SE-164 40 Kista
Sweden
Tel: +46 (8) 623 16 00
Fax: +46 (8) 623 16 50

UNITED KINGDOM
Linear Technology (UK) Ltd.
3 The Listons, Liston Road
Marlow, Buckinghamshire
SL7 1FD
United Kingdom
Tel: +44 (1628) 477066
Fax: +44 (1628) 478153

LINEAR TECHNOLOGY

Linear Technology Corporation
1630 McCarthy Blvd.
Milpitas, CA 95035-7417
1-800-4-LINEAR ● 408-432-1900 ● 408-434-0507 (fax)
www.linear.com

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