BFO system and LF output stage (10 kHz – 62.5 MHz)

88. When frequencies between 0.01 – 62.5 MHz are required, point (G) is at logic 'high' causing relay RLA to be de–energized. The relay has two contacts, one contact completes the +12 V supply to the oscillator, modulator, mixer and LF amplifier, the second contact connects the LF amplifier to the output attenuator AC0 via PLAE.

89. TR1 and its associated components form a Colpitts oscillator operating at 160 MHz. D1 provides the means of phase locking the oscillator. The phase lock loop is mounted on AA1/1 synthesizer board and control is effected via PLAD pin 1. TR2 provides a reasonably constant 3 mA bias current.

90. The output is buffered by IC1, both this and the oscillator components are contained within pockets in the on–board screening. The output from IC1 drives IC2 providing further isolation for a synchronizing output to AA1/1 board. IC1 also drives the fixed frequency amplitude modulator, TR3 and TR4.

91. These are configured as a long–tailed pair with TR4 collector components providing a tuned load. Current of both transistors is varied by the AM signal from A2/2 and at the same time both are switched at 160 MHz by the input applied to TR3 base. An amplitude modulated signal at 160 MHz is thus developed across L2, C18. Subsequent mixing and levelling operations do not affect the AM depth but serve merely to alter the carrier frequency and the overall signal level.

92. D2,D3 and D4 form a current–controlled attenuator, D3 provides a reasonably constant load and D4/C20 maintain effective attenuation of harmonics. L3,L4, C24–C26 form a 160 MHz low–pass filter. This together with the tuned load in TR4 ensures that the 160 MHz signal fed to X1 has a very low level of harmonics therefore ensuring good intermodulation performance.

93. The local oscillator drive to X1 covers the frequency range 160.01 to 222.5 MHz, this produces 10 kHz to 62.5 MHz at X1 mixer output. This local oscillator drive is derived from the output of the first frequency divider IC11a, and IC13 is utilized to boost the signal level. Point (D) is taken 'high' turning D16 off. D25 is turned on by the +12 V supply to the BFO circuit. This routes the signal from IC13 to X1.

94. The output of X1 is fed through a low–pass filter. Part of this, R70, C79 and L20 presents a termination to the mixer in the stop band. The complete filter (including C92, C93 and L23) passes 62.5 MHz but rejects 97.5 MHz (the lowest third order inter–modulation product). This filter is terminated by R83 and is followed by the LF output amplifier, TR14 to TR17.

95. The LF output amplifier provides a voltage gain of 33 dB. The output level is detected by D33 which, with C106, forms a peak detector. The lowest carrier frequency is 10 kHz so the detector time–constant required is a long one. When AM is present the detector measures the peak of the AM envelope; at 100% depth this will be double the voltage at 0% depth. To ensure that the RF level is still correct the reference voltage is increased by an amount equal to the detector voltage increase due to the AM.

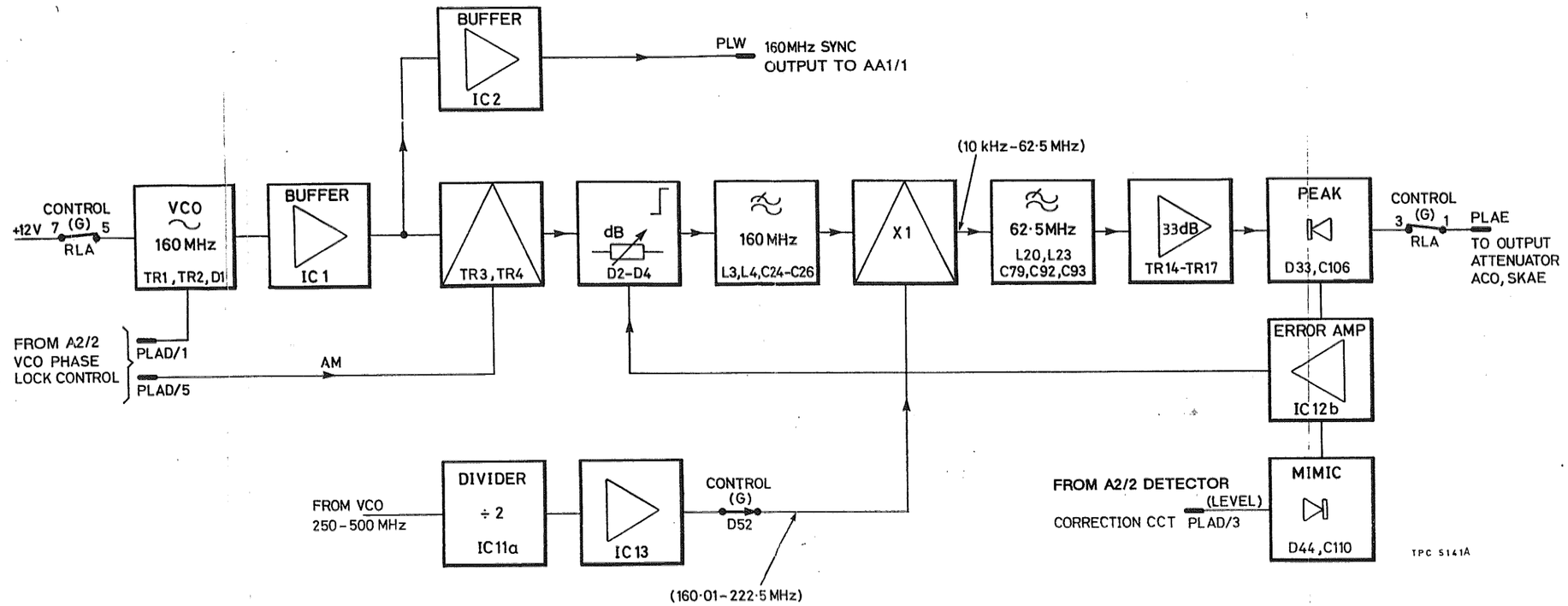
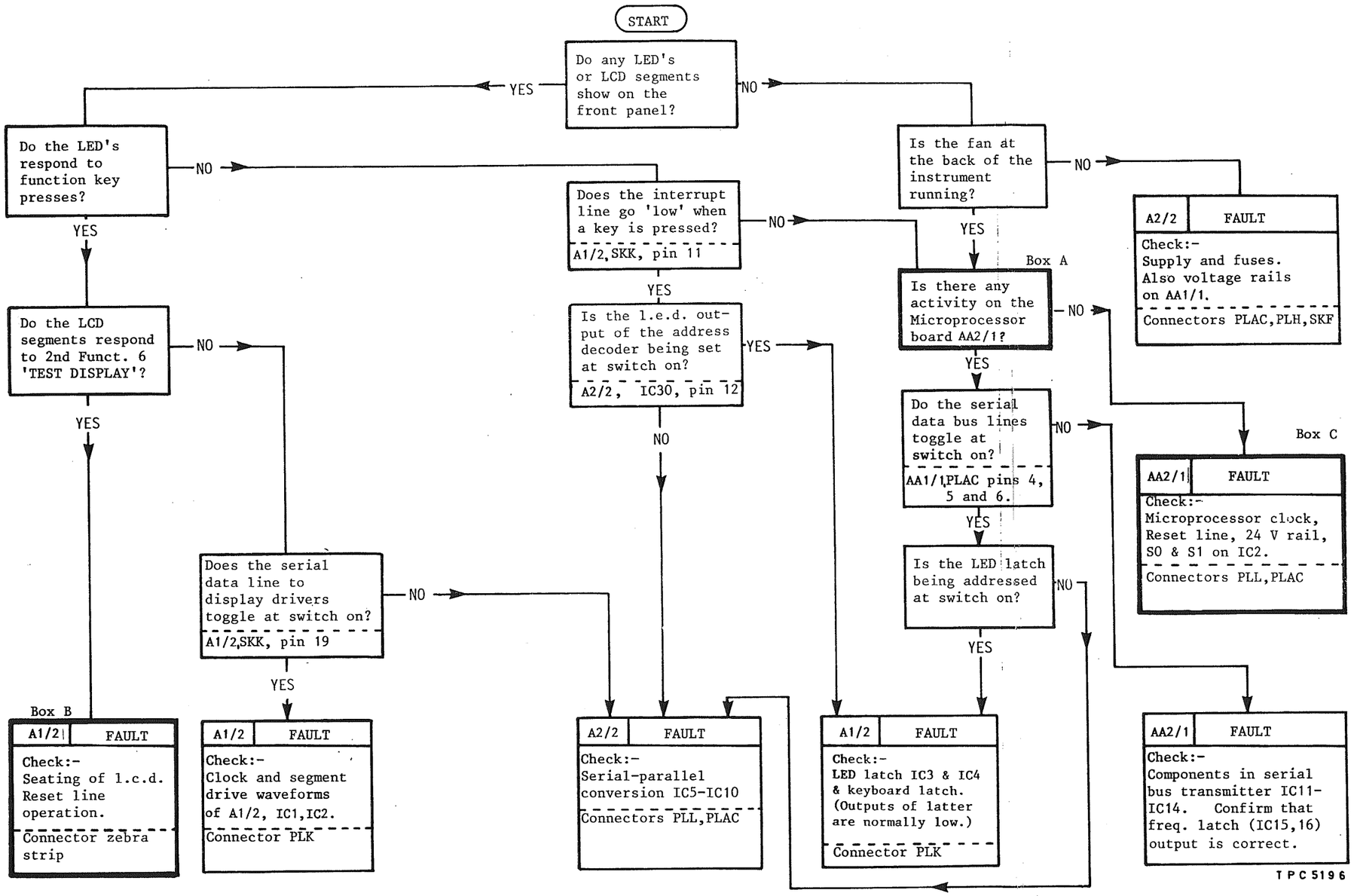
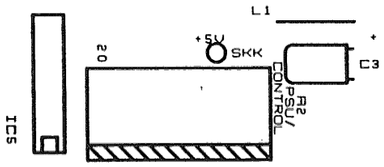


Fig. 4–11 BFO system & LF output stage (10 kHz – 62.5 MHz) simplified block diagram (AB1/2)

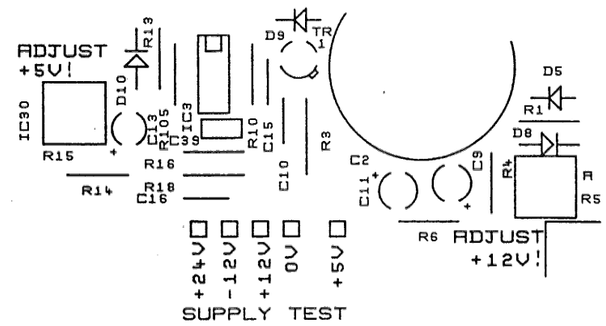
TABLE 5-11 FRONT PANEL FAILURES



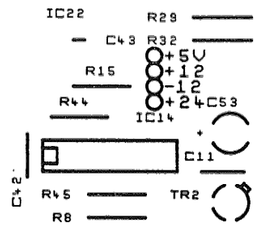
A1/2 KEYBOARD



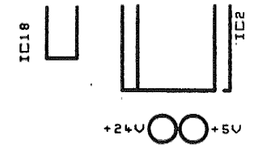
A2/2 PSU/CONTROL



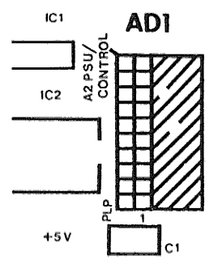
AA1/1 SYNTHESIZER



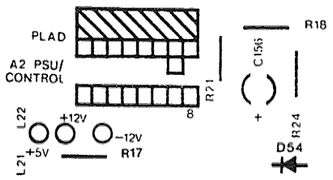
AA2/1 MICROPROCESSOR



AD1 GPIB MODULE



AB1/2 RF PROCESSING



AA1 SYNTH. PLAB

Fig. 5–14 Voltage test points

11. **Box A (see Table 5–11) Microprocessor activity.** If the display is blank or there is no response from the keyboard, it will be necessary to gain access to AA2/1 board. At switch on, data to set up all the latches is sent over the serial bus. The processor then goes into a loop WAITING FOR AN INTERRUPT. Examination of the low order address/data lines from the processor with a logic probe should reveal activity in both cases. Data, clock and strobe lines should be checked immediately after switch on.

12. **Box B (Abnormal LCD presentation).** If the reset line to the LCD drivers fails to operate it is likely that the left and the right sides of the display will be different in appearance, with the contrast on the right–hand side poorer than that on the left–hand side.

13. **Box C (No microprocessor activity).** Although an error number may not be displayed this does not preclude the possibility of either a RAM or an EPROM fault. If the microprocessor is unable to run the system and fails to respond at all, first check for obvious faults e.g. ICs running hot, clock input (5 MHz at IC2 pin 1) and clock output (2.5 MHz at pin 37), RESET 'L' on pin 36 (this will be 'low' if +5 V rail falls below +4.5 V) and the Memory protection circuit (+4.5 V at test point 1).

14. If no address/data lines are active, check the state of IC2 S0 pin 29 and S1, pin 33 advanced timing signals. Because these have no direct application on 2022E they are not shown on the circuit diagram. It is possible that the processor has misinterpreted the address or data lines and as a consequence performs a halt instruction. Confirm this by checking for logic 'low' level on both S0 and S1 lines. Table 5–13 shows the machine cycle status for the states available from which other possible errors can be determined.

TABLE 5–13 PROCESSOR MACHINE CYCLE STATUS (AA2/1)

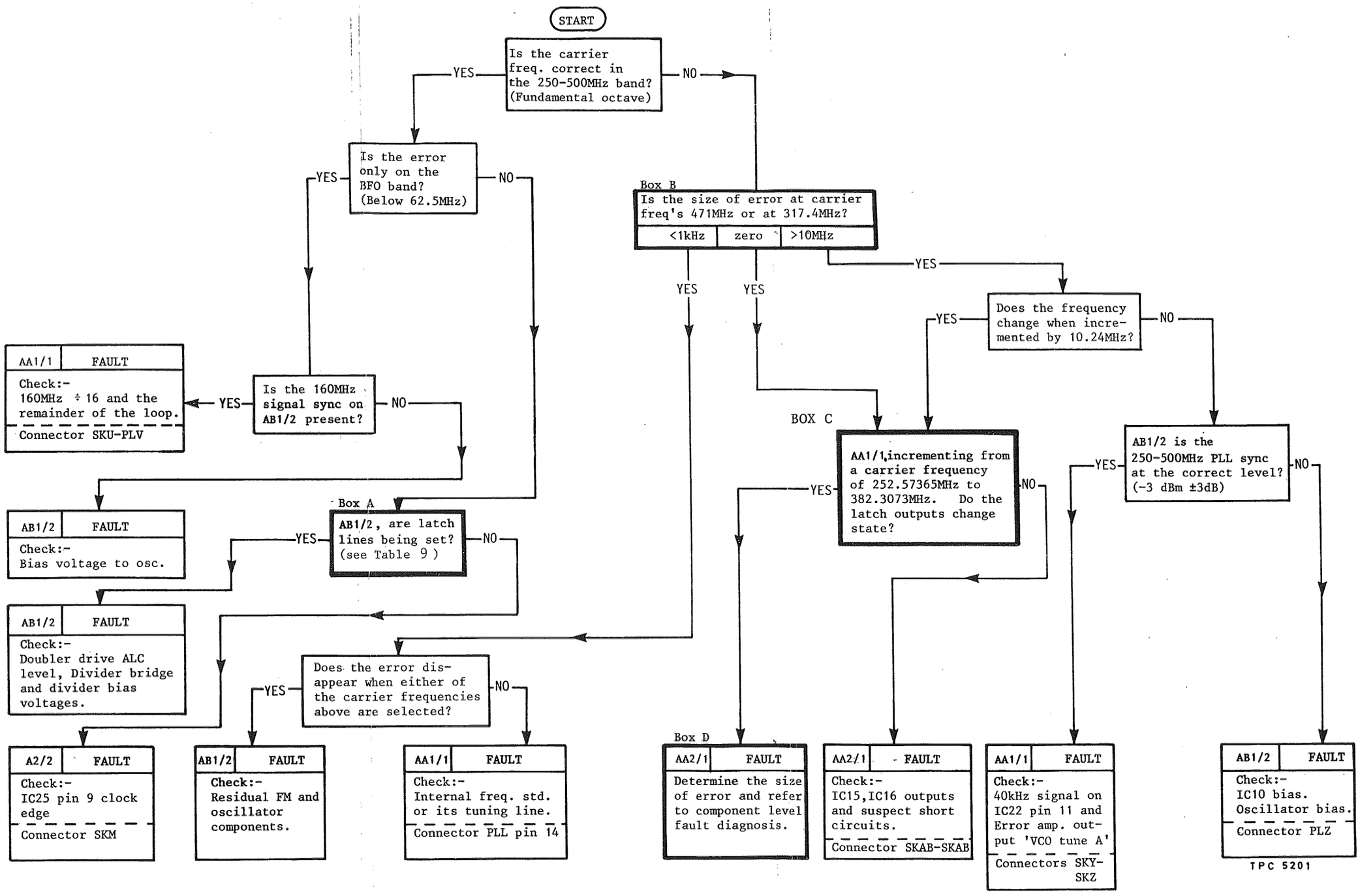
S_0	S_1	States
0	0	Halt
0	1	Memory read
1	0	Memory write
1	1	Op code fetch

Output frequency error

15. Assistance in finding an output frequency error is given in Table 5–14. An output frequency error is defined as a fault in which the frequency, when measured using a frequency counter operating from the same frequency standard as the instrument, indicates that the output differs from the value set.

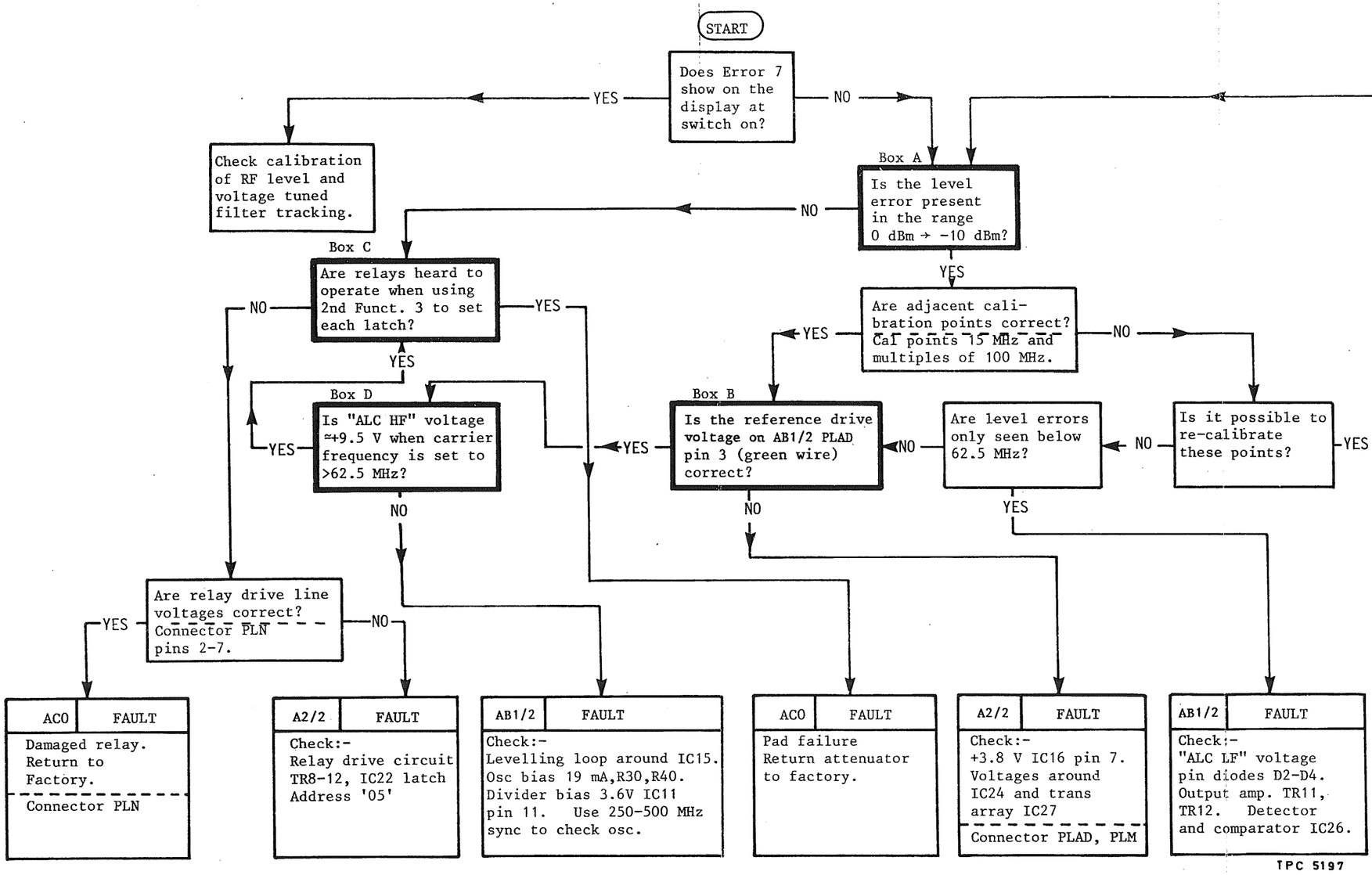
16. When the instrument is using an external frequency standard ensure that this is of the correct level (greater than 1 V RMS) and the correct frequency (1, 5 or 10 MHz). Check Second function 1 'Status' to determine which of the three is internally selected. Instructions on changing the internal selection, normally set to receive a 10 MHz standard, are given in Chap. 5–2, para. 11.

TABLE 5-14 OUTPUT FREQUENCY ERROR



TPC 5201

TABLE 5-17 RF LEVEL ERRORS



TPC 5197

RF level errors

23. A chart to aid fault finding in this area is given in Table 5–17. An RF level fault is defined as a failure which results in the RF level being out of specification but the carrier frequency is correct. In assessing that the RF level is out of specification the RF level offset facility (second function 15) should be switched off. It is also assumed that the error is such that the instrument does not simply require recalibration.

24. If error number 07 (EAROM CHECKSUM FAILURE) is displayed at switch–on it is possible that a mistake has occurred during calibration or that data in the non–volatile memory AA2/1 IC13 has been corrupted, or is not storing data. Usually (but not always) such faults will also be accompanied by FM tracking, AM calibration and tuned filter tracking errors.

25. Because the attenuator unit is a possible source of trouble it simplifies fault finding to initially set this to be out of circuit. This may be done by selecting an RF level setting of 0 dBm. All of the pad relays will then be de–energized. The fault is likely to be one of three boards or the interconnections between these.

Suspect boards	Interconnections	
A2/2 Power supply and control	A2/2 (SKM)	– AB1/2 (SKAD)
AB1/2 RF processing	A2/2 (SKM)	– AB1/2 (SKAD)
AC1 RF attenuator	SKN	– Power supply to AC1
	PLAE	– RF signal to AC1
	PLAF	– RF signal AC1 to front panel SKB

26. **Box A (see Table 5–17) Attenuator/fine level control errors.** If the fault is confined to level selections below –7 dBm it is possible to differentiate between attenuator or fine level control faults by adding multiples of 10 dB to the level. As the level is increased it may become obvious that a gross error is present with a particular pad in circuit. If however the error is present when the attenuator is no longer contributing to the insertion loss the fine level control is suspect.

27. **Box B (AB1/2 Reference drive voltage).** Check that, with a carrier frequency of 200 MHz selected, the following nominal voltages are present on AB1/2 PLAD pin 3.

RF level setting	Drive voltage
+10 dBm	2.13 V
+7 dBm	1.4 V
0 dBm	0.62 V
–7 dBm	0.24 V

28. **Box C (Attenuator relay function).** Each of the relays can be selected individually by utilizing the second function 3 mode of operation. Details of this procedure is given in "Use of second function 3 (Manual latch setting)". Each relay is accessed by the method described in Chap. 5–1, para. 6.

29. Further use of the second function 3 control can be made to select each relay in turn and listen for them to de–energize and re–energize. Data is set to '1' logic high, then returned to '0' logic low. Press the STORE key after each bit of data is set to '1' or reset to '0'. Begin with D0 – D4 all set to '0', all relays should now be energized. Set each data bit in turn to logic '1', STORE, then reset to '0' and STORE again.

D0 set to '1' de–energizes RLA
D1 set to '1' de–energizes RLB
D2 set to '1' de–energizes RLC
D3 set to '1' de–energizes RLD
D4 set to '1' de–energizes RLE

If the attenuator unit is suspected, remove AB0 unit; the attenuator can then be detached from this without further dismantling by removing the four securing screws and the conhex connector from AB1/2.

Note ...

When refitting AB0 unit take care to prevent damage to GPIB board AD1 if this is fitted.

30. **Reverse power failure.** A TO5 relay in the attenuator unit (RLF) gives protection for the attenuator's resistive elements by presenting an open circuit to the output connector SKAF if excessive voltages are detected on the signal line. Testing of this circuit is described in Chap. 5–1. If a fault is suspected, it is safer to set the RF level to 0 dBm to give protection to the pads.

31. Should the RPP not trip, check for correct operation of the detectors D1 and D2. This can be achieved by raising the rear of unit AB0 slightly to give access to PLN, see Fig. 5–1. Set the RF level to 0 dBm, then apply +5 V between earth and the centre pin of the output connector. Connect a voltmeter between earth and PLN pin 9; this should read approximately +0.25 V. Reverse the polarity of the applied voltage. Now apply the voltmeter positive terminal to earth and the negative terminal to PLN pin 10. The voltage should be approximately –0.25 V.

Note ...

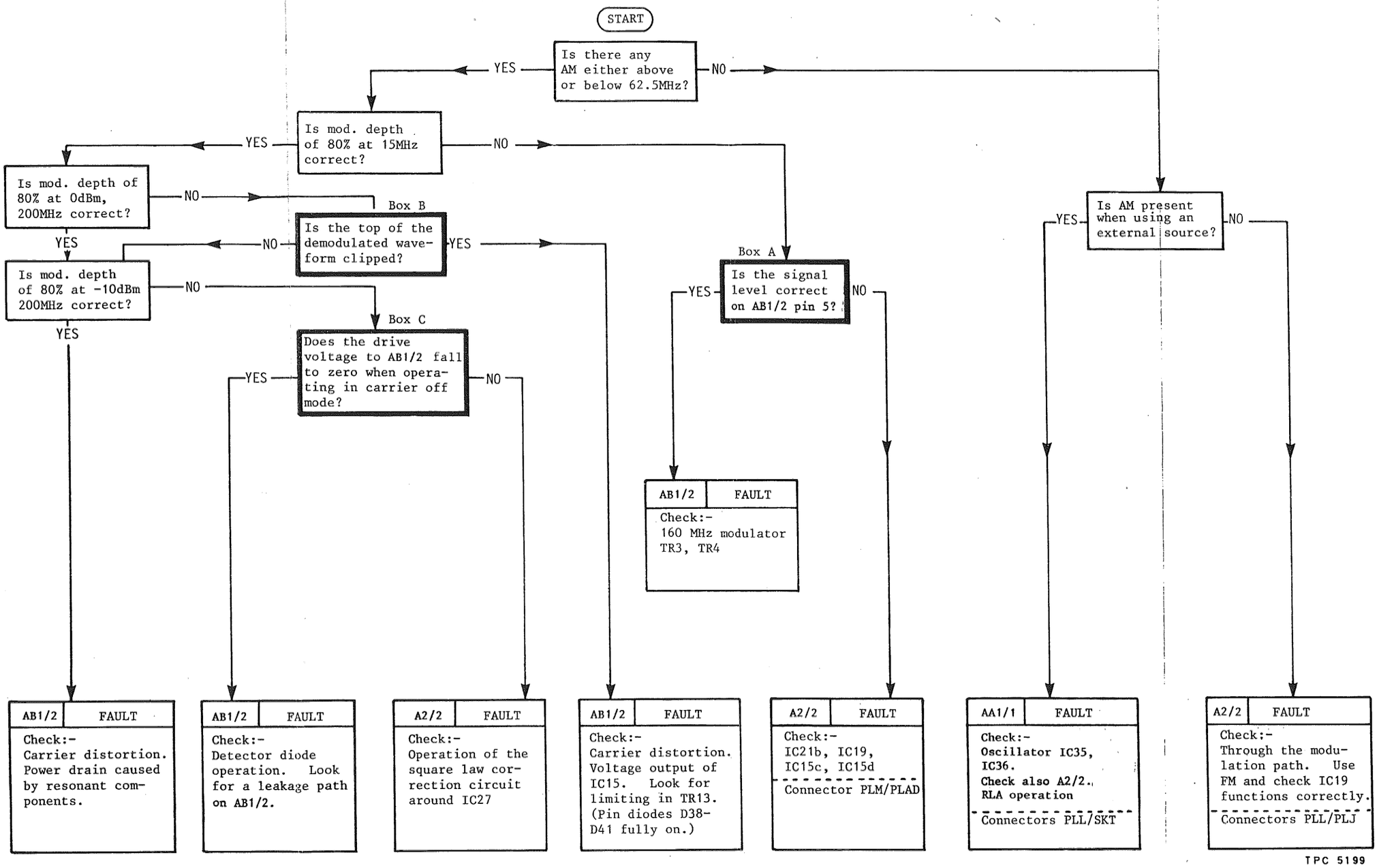
If a very high impedance voltmeter is used it is possible that hum picked up from surrounding connectors will be peak detected. This will give a standing reading of voltage even when a voltage is not applied to the output connector. Either subtract this offset from the reading obtained when carrying out the test or alternately shunt the voltmeter with a 100 kΩ resistor.

32. Most faults are likely to be confined to either AC1 attenuator board or A2/2 Power supply and control board. The most likely suspect interconnection is PLN on AC0 attenuator to A2/2 control.

33. **Attenuator accuracy.** The only electrical adjustment provided on AC1 is a series of flags which may be used to adjust the calibration of each pad. In the 0 dBm attenuation condition the attenuator has an insertion loss which is dependent upon the frequency selected. This insertion loss is compensated for by RF level calibration. The flags are used to adjust the attenuation of each pad so that the difference between the attenuation of each pad being in or out of circuit is equal to the nominal attenuation of the pad at 1 GHz.

34. To carry out comprehensive attenuator accuracy checks and realignment requires each pad to be set up separately using specialized measuring facilities. It is therefore recommended that this be carried out only by the nearest Marconi Instruments agent or Service Division. (A spectrum analyzer may be used to check levels down to –90 dBm with limited accuracy.)

TABLE 5-18 AM DEPTH ERRORS



TPC 5199

AM faults

35. Two systems are used to achieve the required modulation. The first system employs a fixed frequency modulator when carrier frequencies up to 62.5 MHz are selected. The second system (for carrier frequencies above 62.5 MHz) uses envelope feedback operating around the output amplifier.

36. If the fault is such that the AM fails completely it should be possible to locate this by following the AM path from the modulation source. If some AM is present but with the incorrect depth, check to see which of the two systems described above are defective. It is assumed that it is not possible to carry out the normal recalibration procedure.

37. The following boards and connectors are possibly connected with an AM fault.

Suspect boards		Interconnections	
A2/2	Modulation control	A2/2 (PLM)	– AB1/2 (SKAD)
A2/2	Modulation control	A2/2 (PLJ)	– Front panel (SKA)
AB1/2	RF signal processing	AB1/2 (SKAD)	– A2/2 (PLM)
AA1/1	Internal mod. source	AA1/1 (PLT)	– A2/2 (PLL)

38. **Box A (see Table 5–18) 160 MHz amplitude modulator fault.** Select a carrier frequency of 15 MHz, modulation depth of 80% and an RF level of 0 dBm. Check at AB1/2 PLAD pin 5 (white wire) for a sine wave with a zero mean and peak amplitude of 5.5 V.

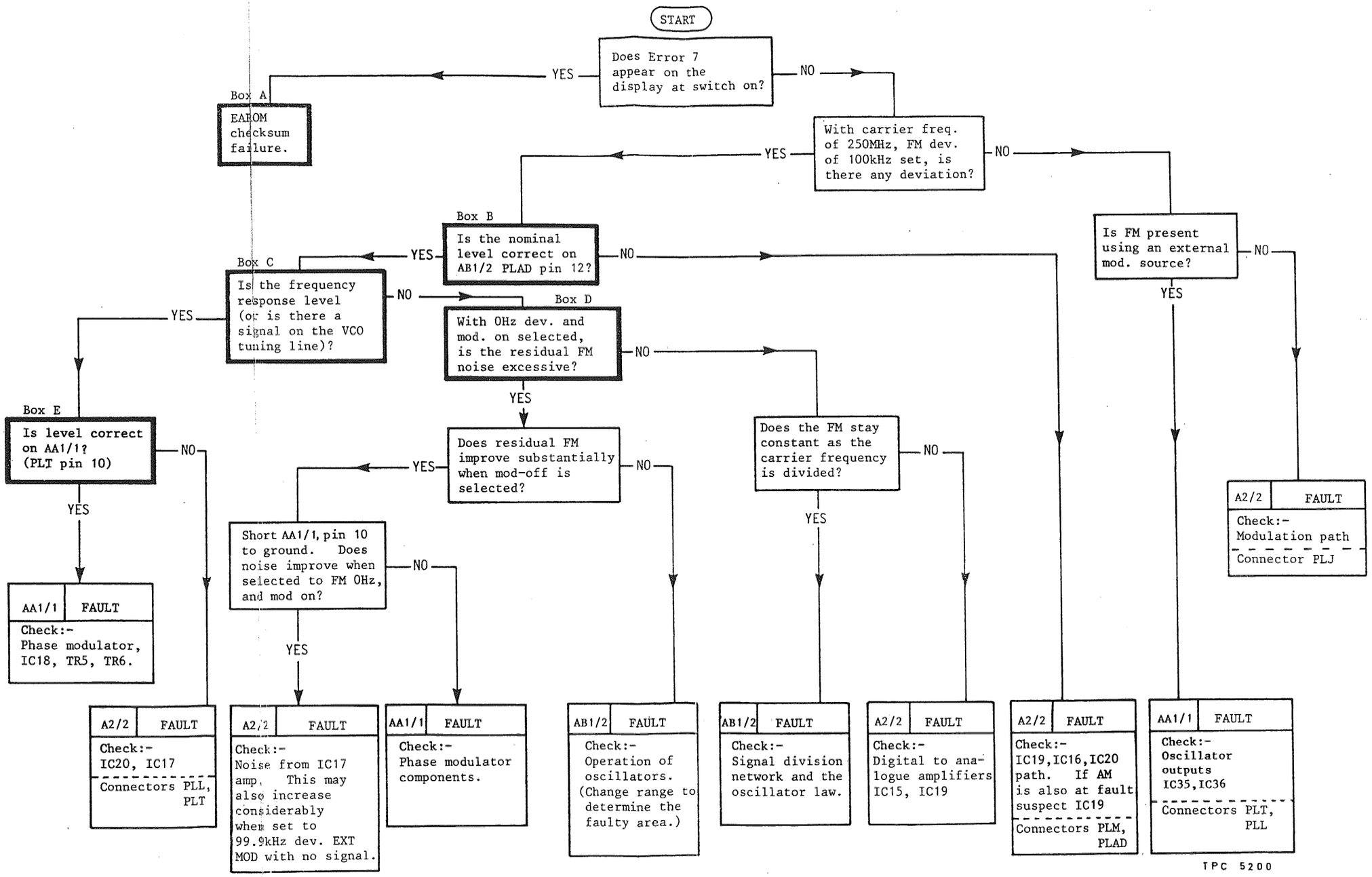
Note ...

When AB1/2 unit is disconnected from A2/2 board there is a slight loading effect on the voltage seen on A2/2, approximately 0.5 V.

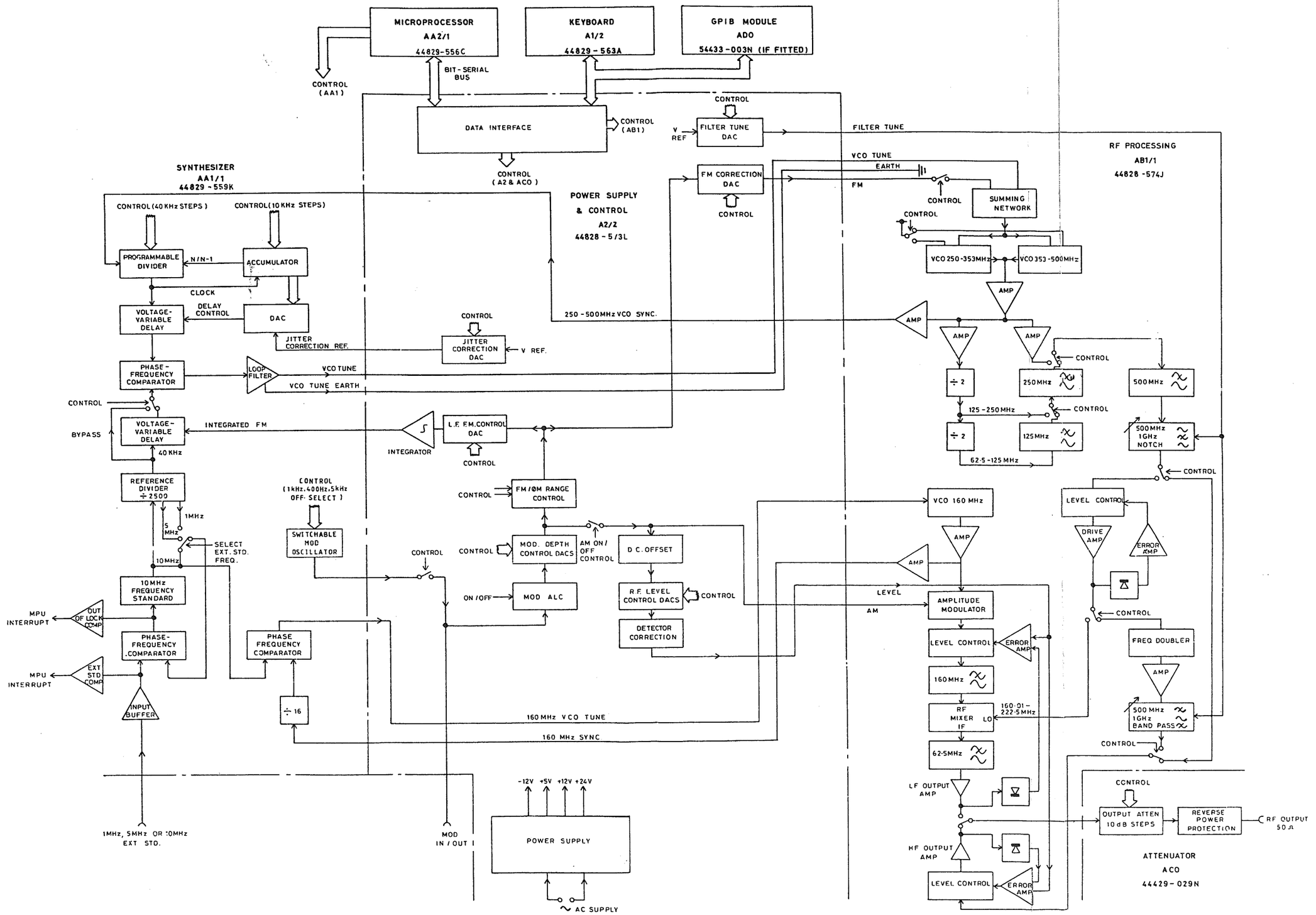
39. **Box B (Envelope feedback fault).** Envelope distortion may occur if there is a restriction on the level range. Using the internal modulation output as a sync signal it should be possible to determine whether the peak power is limited. AM is applied in the same sense as the voltage on the MOD IN/OUT socket, where a positive voltage means a greater power level.

40. **Box C (Square law correction error).** If the trough of the modulation envelope is at fault it is possible that the square law correction circuit on A2/2 board is malfunctioning. A further possible cause is a severe leakage to earth on AB1/2 board. Check the voltage on AB1/2 PLAD pin 3 (green wire); this should fall to 0 V, or slightly negative depending on the setting of the detector correction potentiometer A2/2 R90.

TABLE 5-19 FM DEVIATION ERRORS



TPC 5200



Drg. No. Y52022-950J Sht. 1 of 1, Issue 1

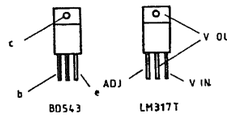
Fig. 7–1 2022E Frequency synthesis and signal processing simplified block diagram

NOTES
1. MATING PLUGS AND SOCKETS HAVE SAME IDENTITY, FOR EXAMPLE, SKF CONNECTS TO PLF CONNECTOR. NUMBERS CORRESPOND IF SOCKETS AT BOTH ENDS OF A CONNECTOR ASSEMBLY HAVE THE SAME IDENTITY. (I.E. PIN 1 CONNECTS TO PIN 1, PIN 2 TO PIN 2 ETC.)

2. WIRE TYPES 6^a 15410-227T, 6^b 15410-222G, 6^c 15420-276U, 6^d 15410-187W 6^e 15410-202C, 6^f M15410-181, 6^g 15110-222S.

3. VIEWED FROM FRONT OF INSTRUMENT, SWITCH SB IS TO THE RIGHT OF SC. CONTACT POSITIONS MARKED ALSO REFER TO VIEW FROM FRONT OF INSTRUMENT. SB IS DRAWN FOR 210-240V SUPPLY (ALTERNATIVE POSITION IS FOR 105-120V). SC IS DRAWN FOR 115/120V OR 230/240V (ALTERNATIVE POSITION IS FOR 105/110V OR 219/220V).

4. LEAD CONFIGURATIONS.



5. ≡≡≡ INDICATES FERRITE BEAD
6. THE NEGATIVE TERMINAL OF FAN IS CONNECTED TO POSITIVE SUPPLY SO THAT AIR FLOWS OUT OF REAR PANEL.

Fig. 7-2 Basic module interconnections, A0/1

Fig. 7-2
46881-891U
Oct. 88

Drg. No. Z52022-950J Sht. 1 of 1, Issue 1

Fig. 7-2

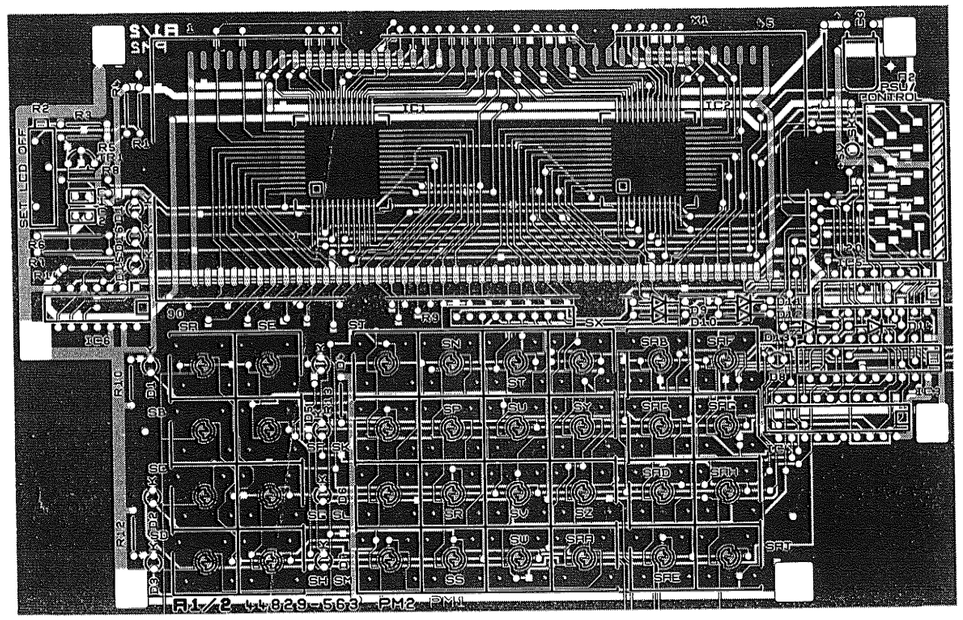
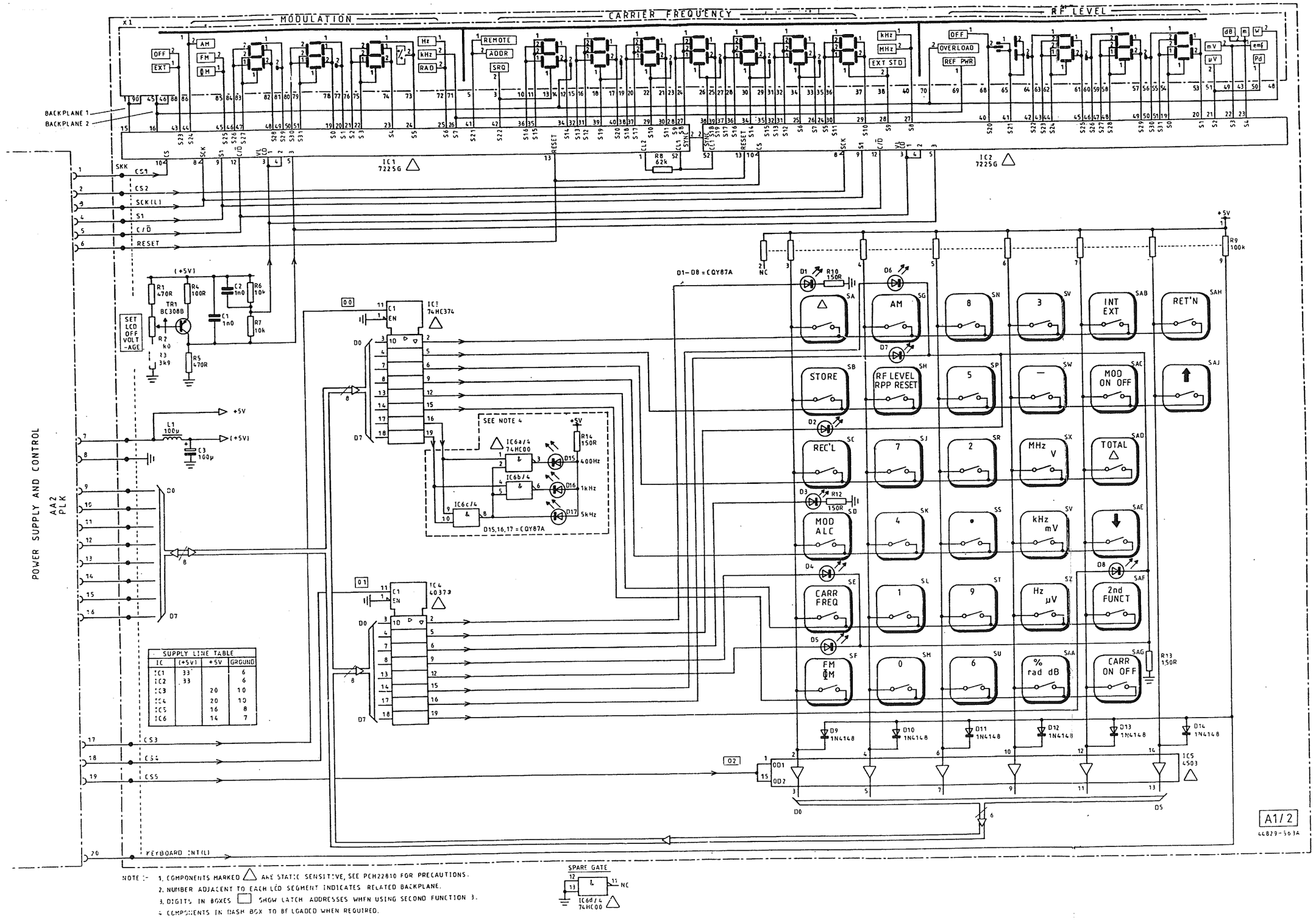


Fig. 7–3a Keyboard component layout, A1/2



NOTE :-
1. COMPONENTS MARKED △ ARE STATIC SENSITIVE, SEE PCH22810 FOR PRECAUTIONS.
2. NUMBER ADJACENT TO EACH LED SEGMENT INDICATES RELATED BACKPLANE.
3. DIGITS IN BOXES ☐ SHOW LATCH ADDRESSES WHEN USING SECOND FUNCTION S.
4. COMPONENTS IN DASH BOX TO BE LOADED WHEN REQUIRED.

Fig. 7–3 Display and keyboard, A1/2

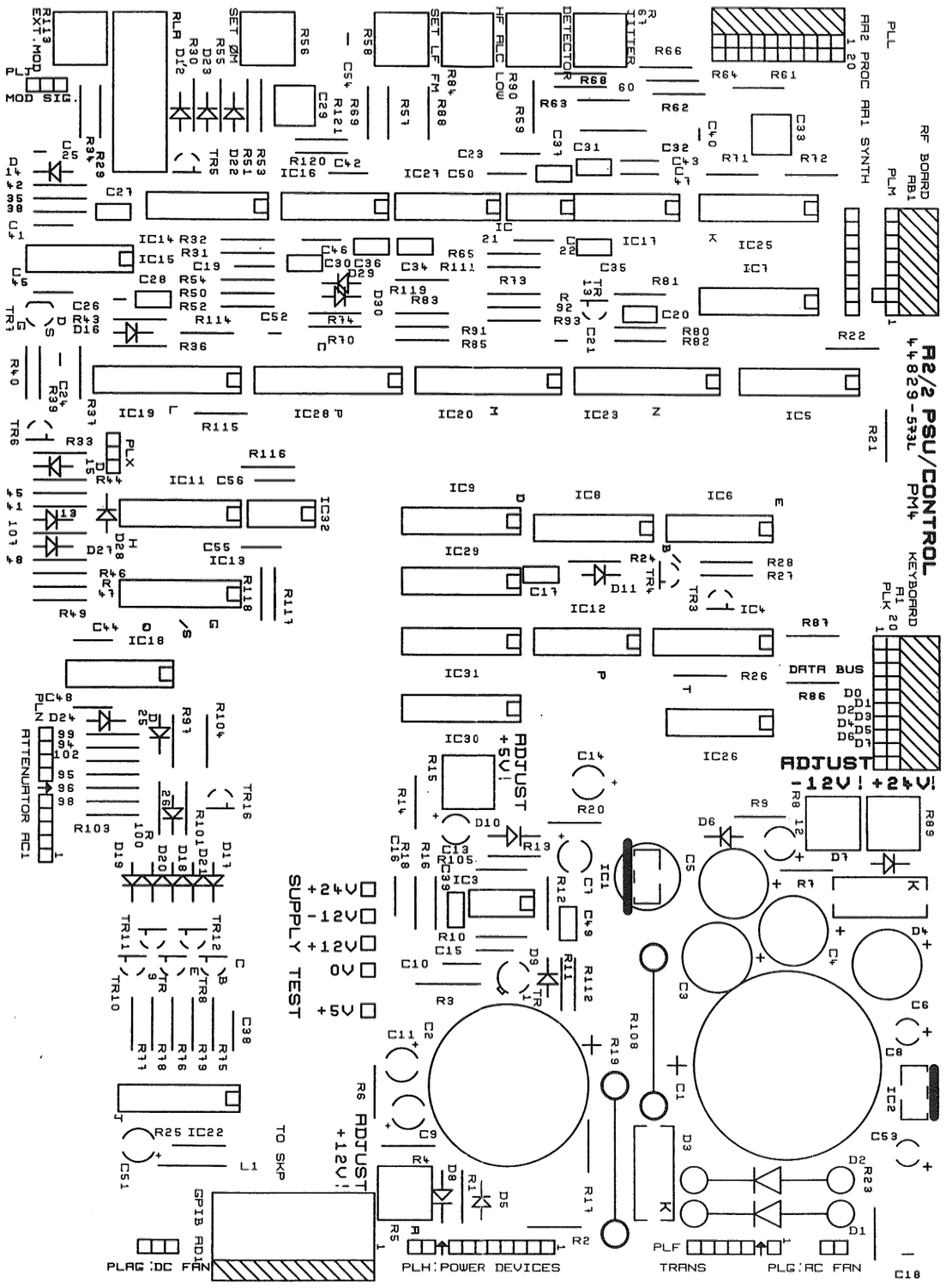


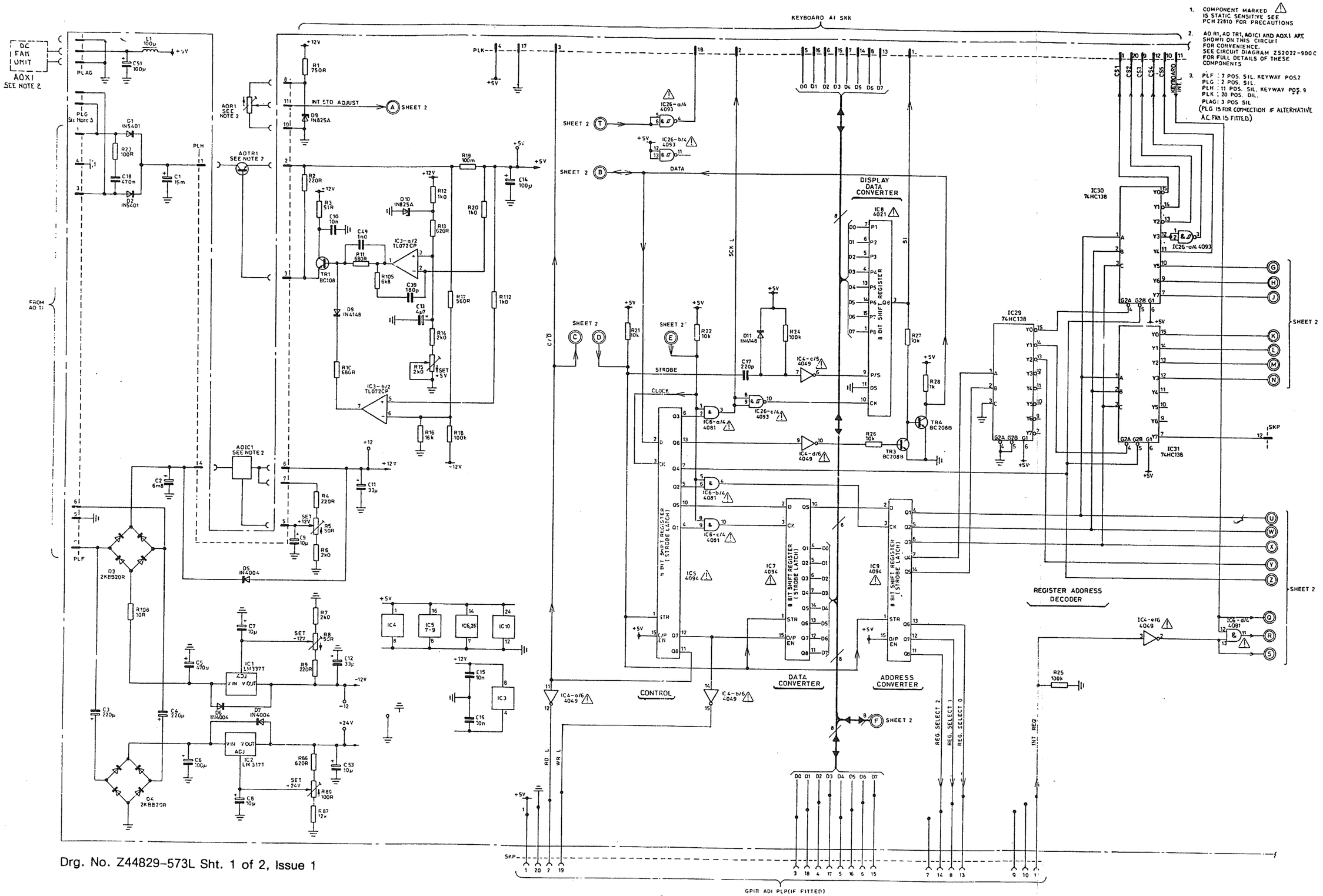
Fig. 7–4a

Fig. 7–4a Power supply & control, component layout, A2/2

Fig. 7–4a
46881–891U
Oct. 88

NOTES

1. COMPONENT MARKED ⚠ IS STATIC SENSITIVE SEE PCM 22810 FOR PRECAUTIONS
2. AO R1, AO TR1, AOIC1 AND AOX1 ARE SHOWN ON THIS CIRCUIT FOR CONVENIENCE. SEE CIRCUIT DIAGRAM Z52022-900C FOR FULL DETAILS OF THESE COMPONENTS
3. PLF : 7 POS. SIL. KEYWAY POS.2
   PLG : 2 POS. SIL.
   PLH : 11 POS. SIL. KEYWAY POS. 9
   PLK : 20 POS. DIL.
   PLAG: 3 POS SIL
   (PLG 15 FOR CONNECTION IF ALTERNATIVE A.C. FAN IS FITTED)



Drg. No. Z44829-573L Sht. 1 of 2, Issue 1

Fig. 7-4 Power supply & control (Sheet 1), A2/2

NOTES

1. COMPONENT MARKED ⚠ IS STATIC SENSITIVE SEE PCH 22810 FOR PRECAUTIONS
2.
   RELAY 80-1-A-5/1 CONNECTIONS VIEWED FROM PIN SIDE. RELAY IS SHOWN IN NON-ENERGISED CONDITION
3. INTEGRATED CIRCUIT SWITCHES ARE SHOWN FOR CONTROLS IN LOGIC LOW CONDITION.
4. PLJ : 3 POS SIL.
   PLL : 20 POS. DIL.
   PLM : 16 POS. DIL.
   PLN : 10 POS. SIL.
   KEYWAY POS. 5.
5. DIGITS IN BOXES ☐ SHOW LATCH ADDRESSES WHEN USING SECOND FUNCTION 3.

Fig. 7-5 Drg. No. Z44829-573L Sht. 2 of 2, Issue 1
46881-891U
Oct. 08

Fig. 7-5 Power supply & control (Sheet 2), A2/2

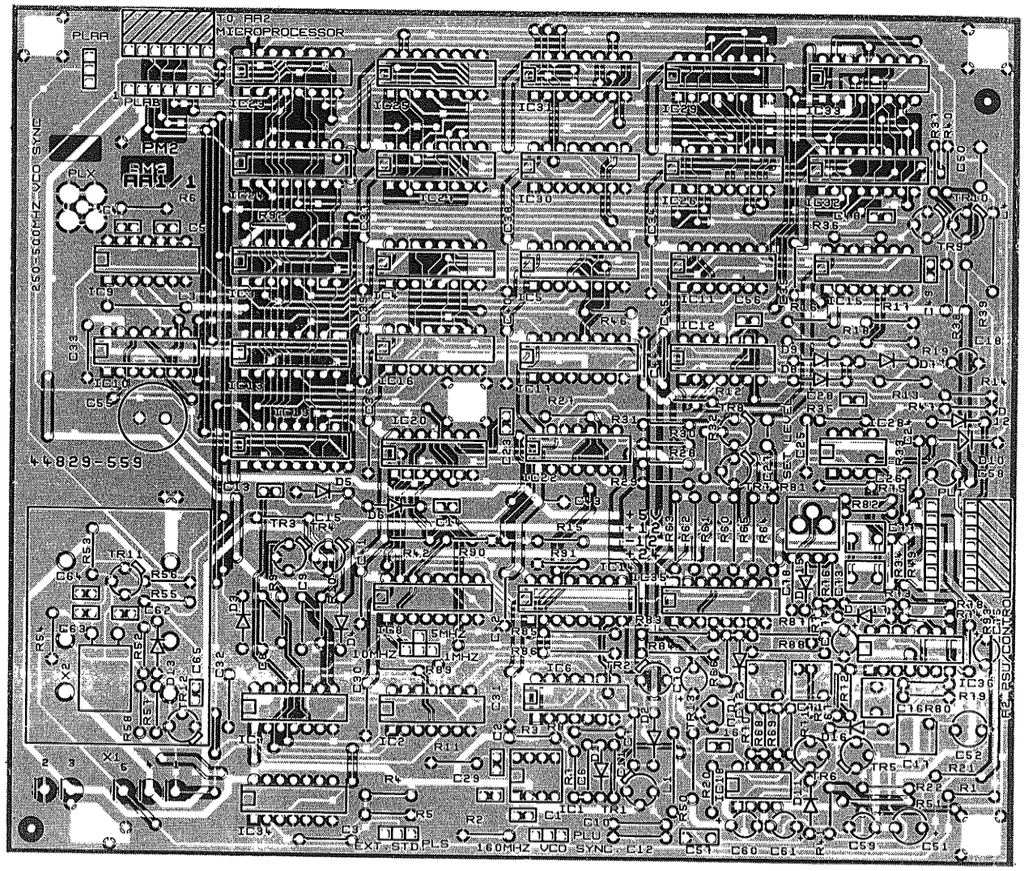
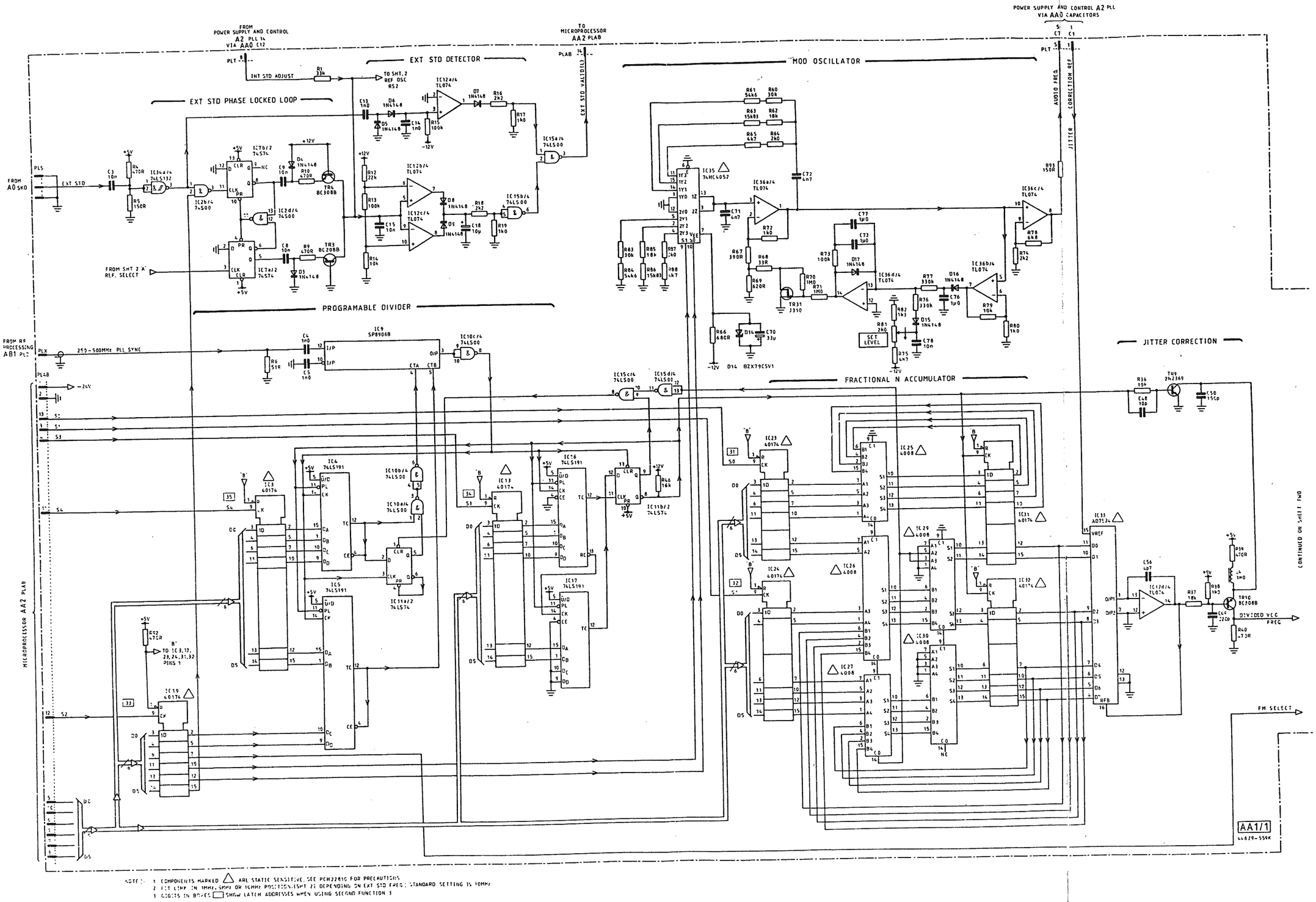


Fig. 7–6a Synthesizer, component layout, AA1/1

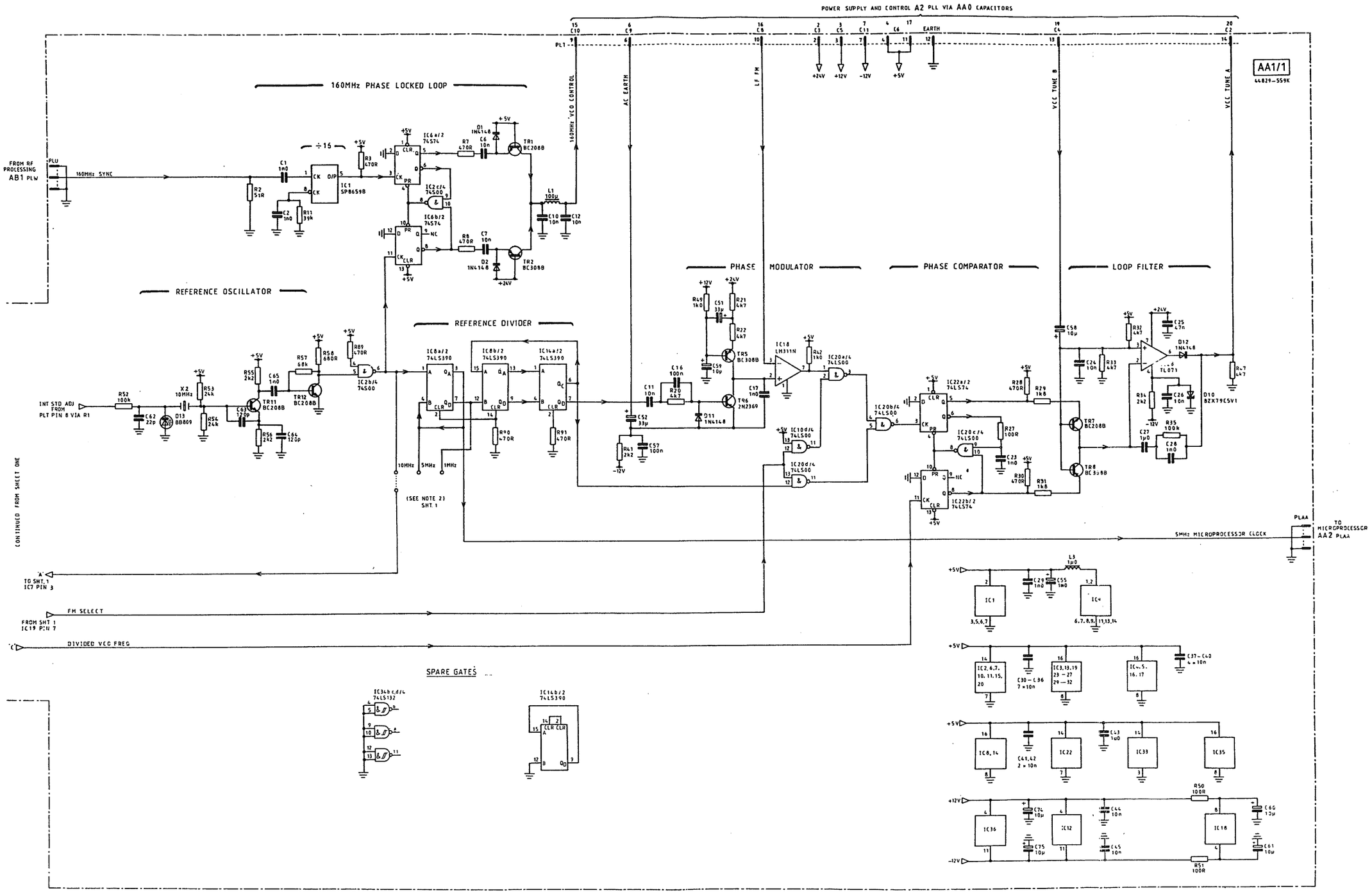


Drg. No. Z44829-559K Sht. 1 of 2, Issue 1

Fig. 7–6 Synthesizer,(Sheet 1) AA1/1

Fig. 7–6
46881–891U
Oct. 88

Fig. 7–6



Drg. No. Z44829-559K Sht. 2 of 2, Issue 1

Fig. 7–7 Synthesizer,(Sheet 2) AA1/1

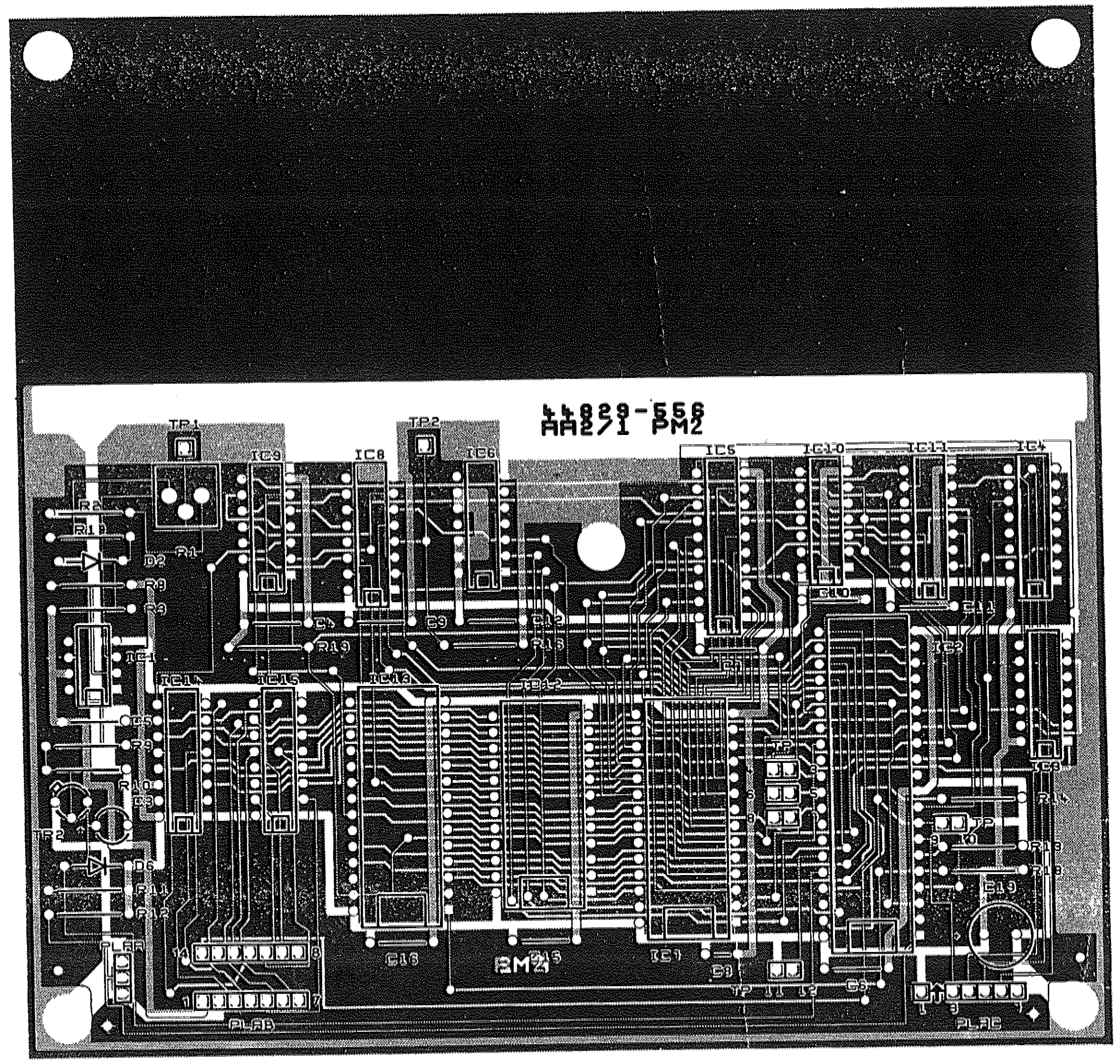
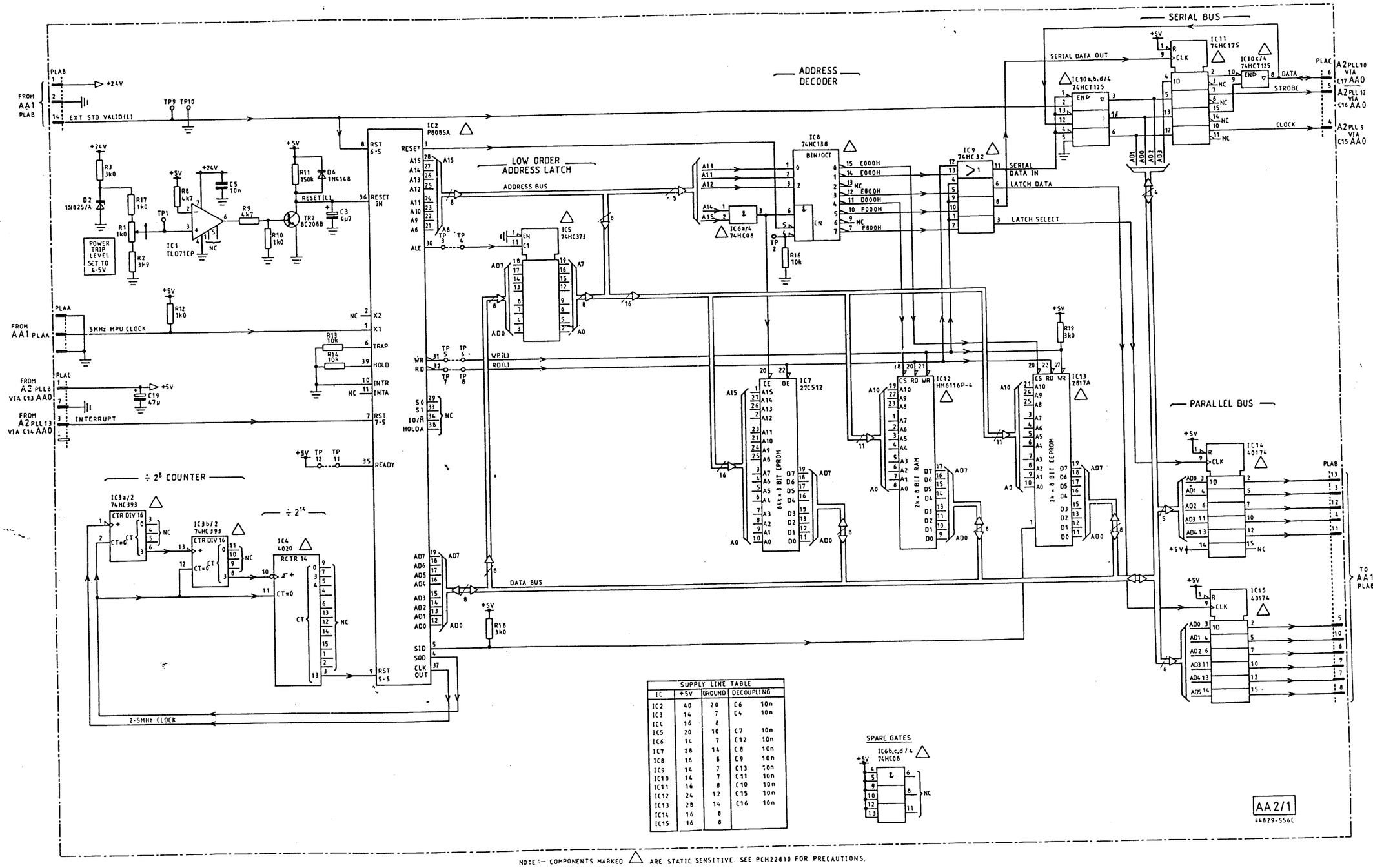
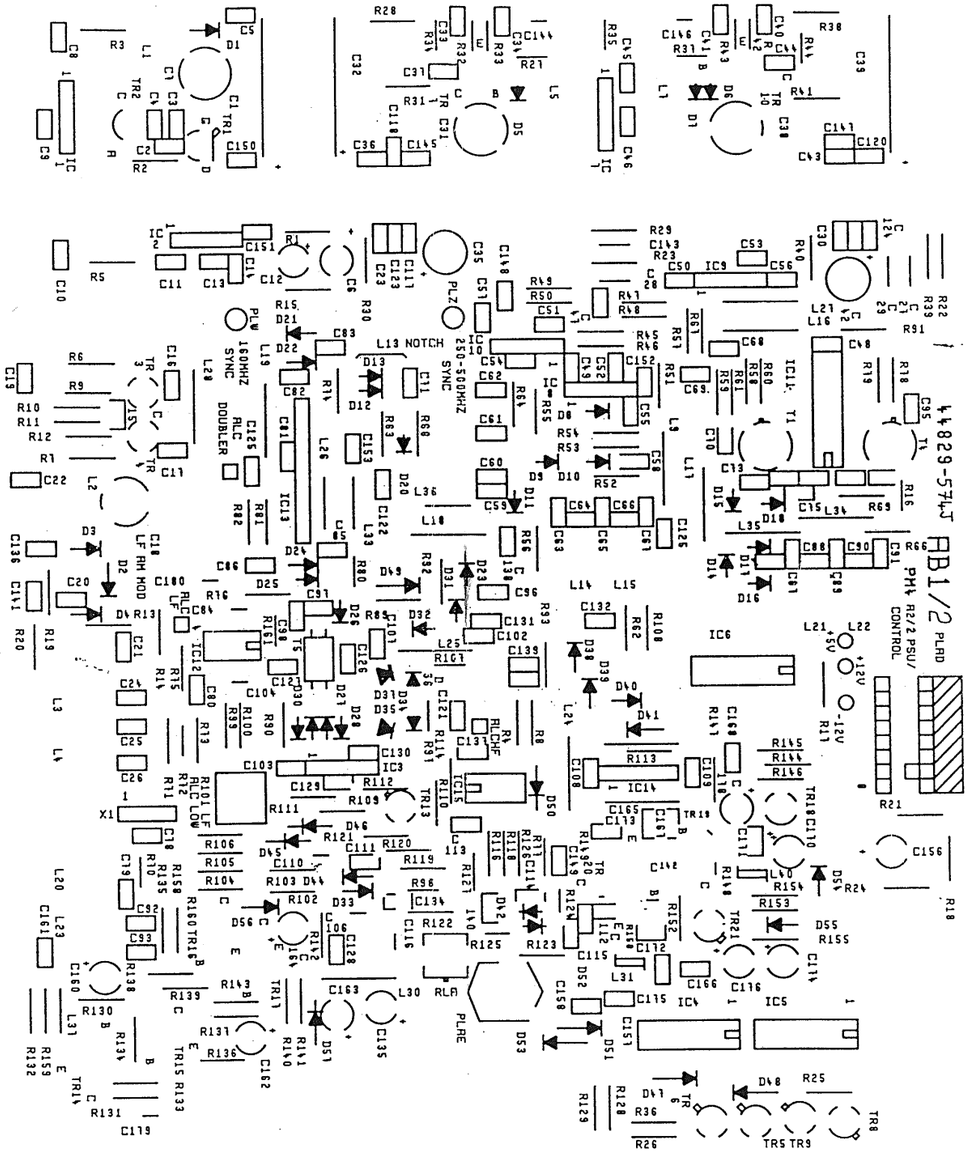


Fig. 7–8a Microprocessor, component layout, (AA2/1)



Drg. No. Z44829-556C Sht. 1 of 1, Issue 1

Fig. 7-8 Microprocessor, AA2/1



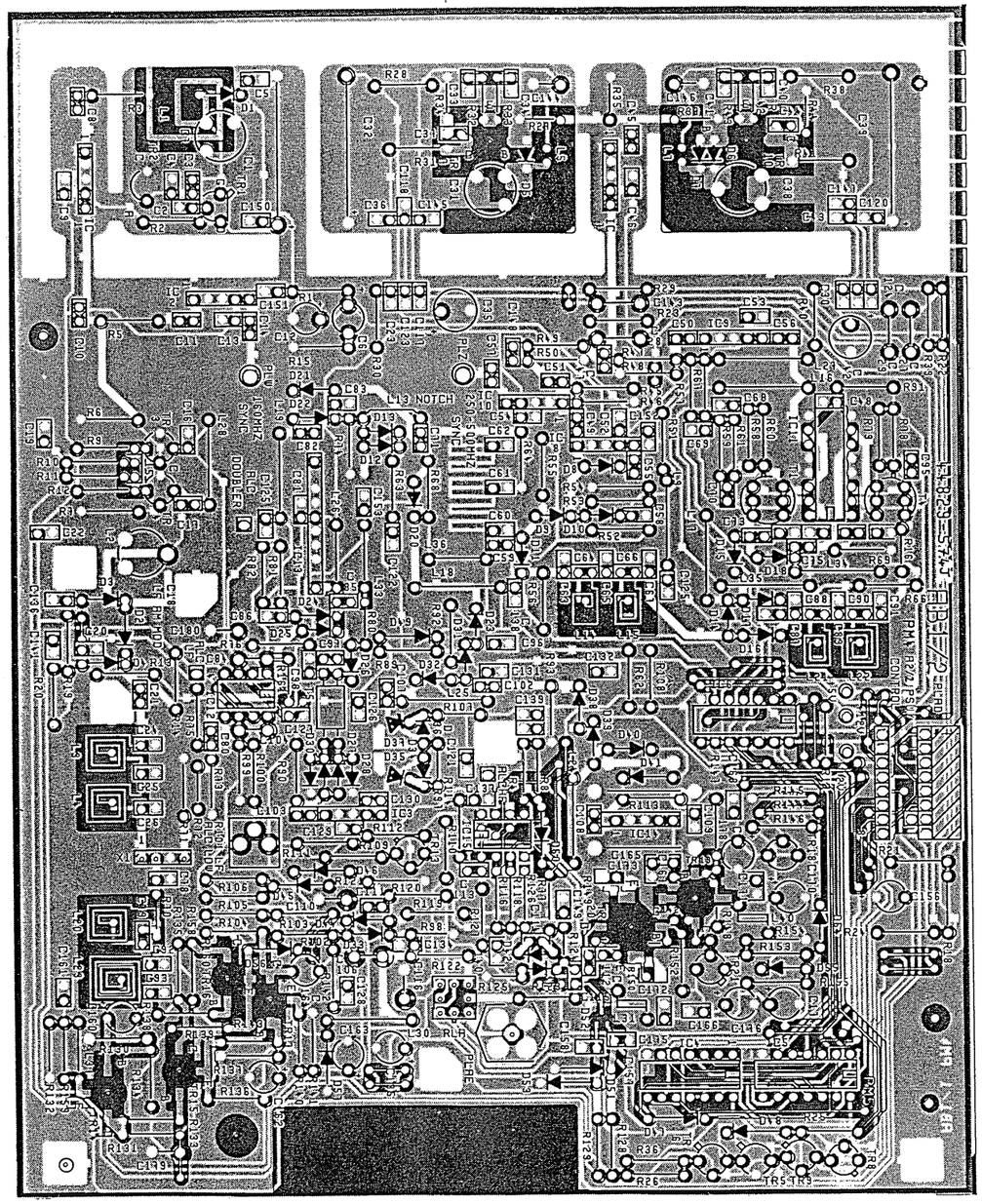
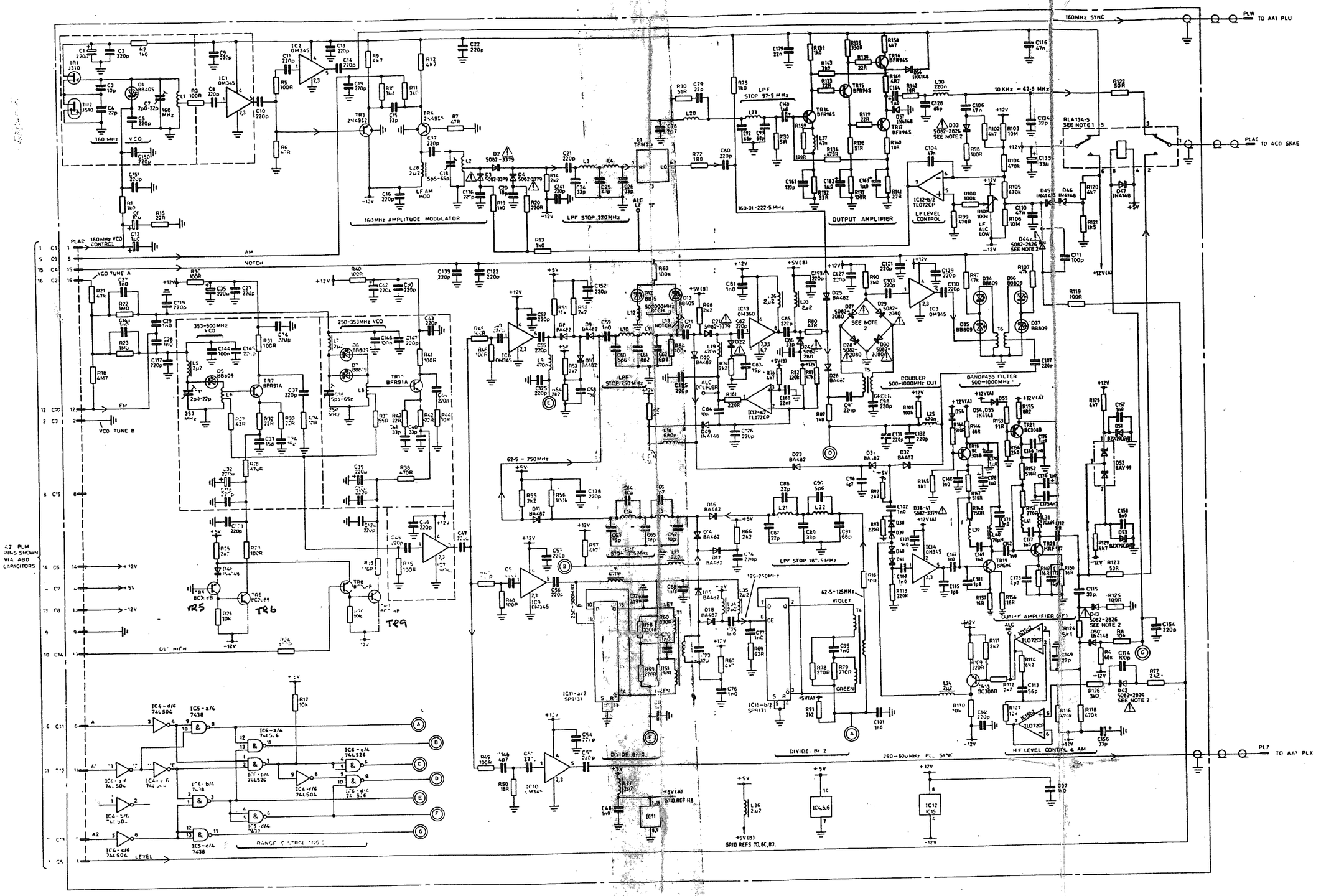


Fig. 7–9a RF processing, component layout, AB1/2

Fig.7– 9a

Fig. 7–9a
46881–891U
Oct. 88



NOTES:–
1. RELAY 3 SHOWN IN A NON-ENERGIZED CONDITION.
2. IC27 - D36 ARE MATCHED DIODE QUAD. D33, D44 AND D42, D41 ARE MATCHED DIODE PAIRS.
3. P. AND 16 POS DIL.
4. COMPONENT MARKED 1 ARE STATIC SENSITIVE
5. +12V(A) SOURCE GRID REF 11C

Drg. No. Z44829-574J Sht. 1 of 1, Issue 1

Fig. 7–9 RF Processing, AB1/2

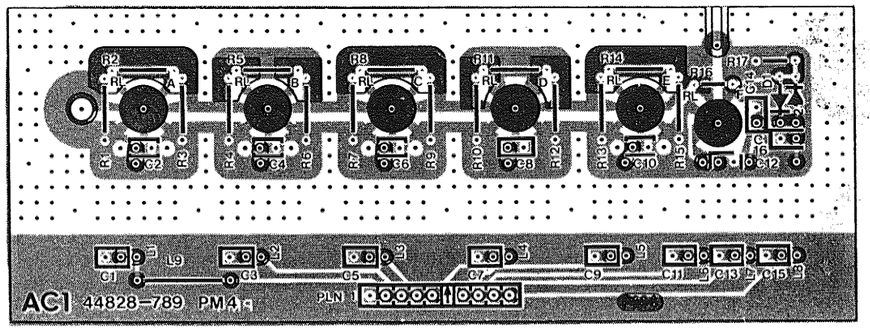
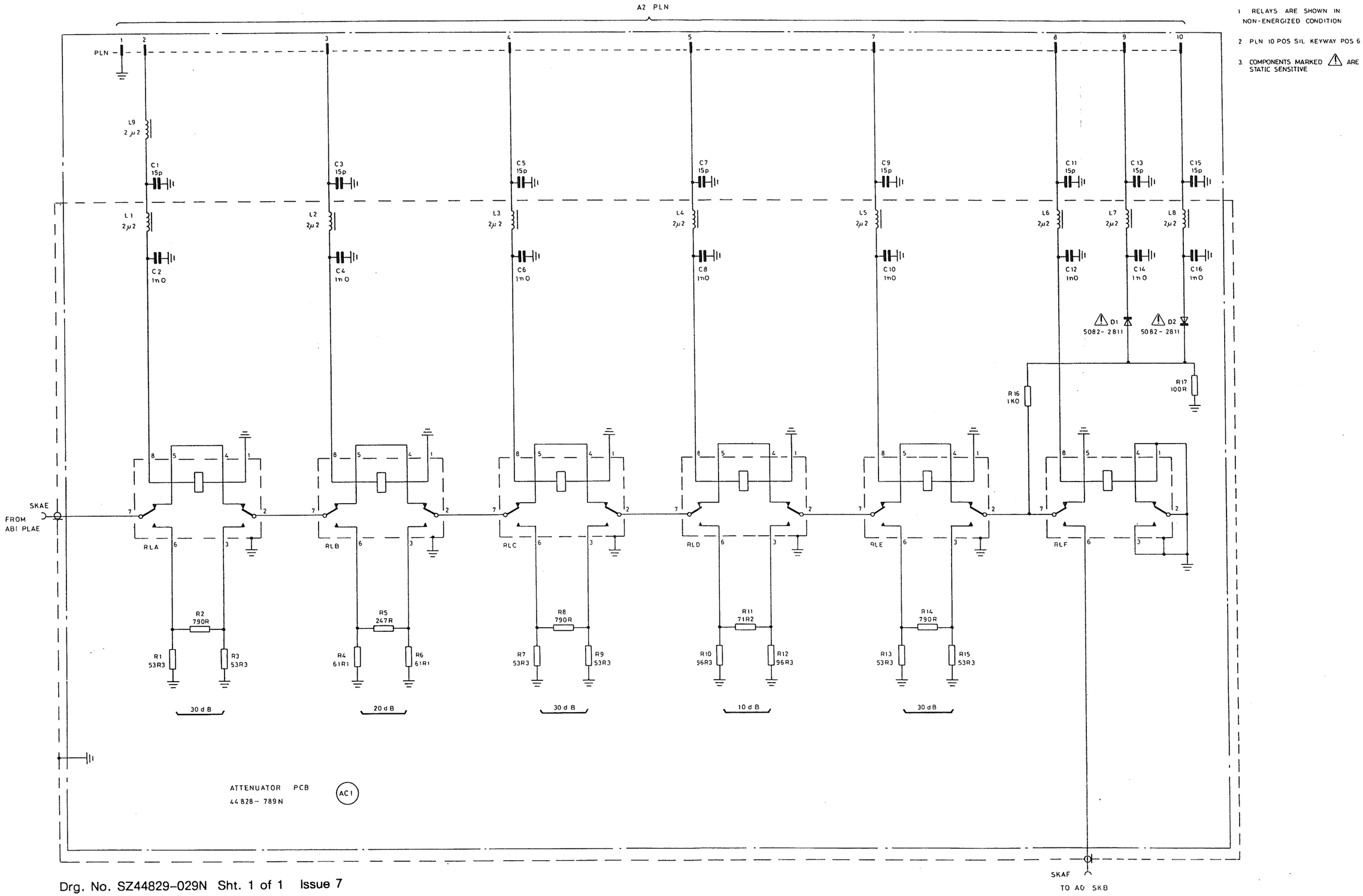


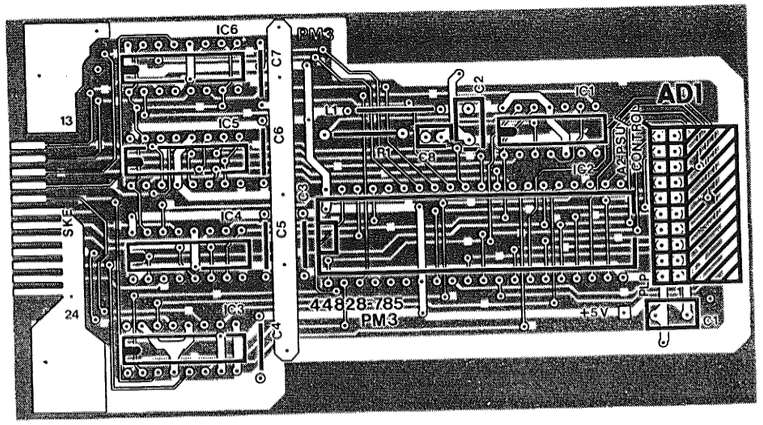
Fig. 7-10a Attenuator, component layout, AC1



1. RELAYS ARE SHOWN IN NON-ENERGIZED CONDITION
2. PLN 10 POS SIL KEYWAY POS 6
3. COMPONENTS MARKED ⚠ ARE STATIC SENSITIVE

Drg. No. SZ44829-029N Sht. 1 of 1 Issue 7

Fig. 7-10 Attenuator, AC0



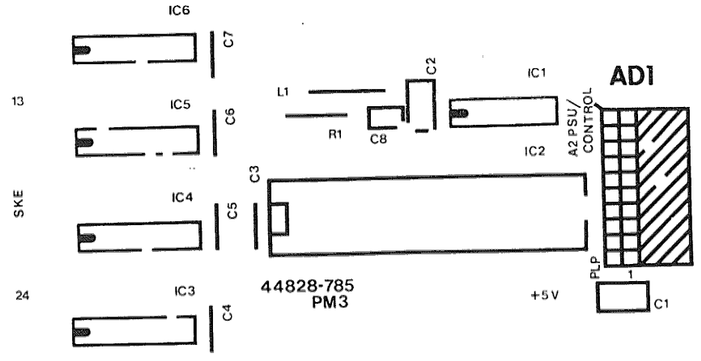
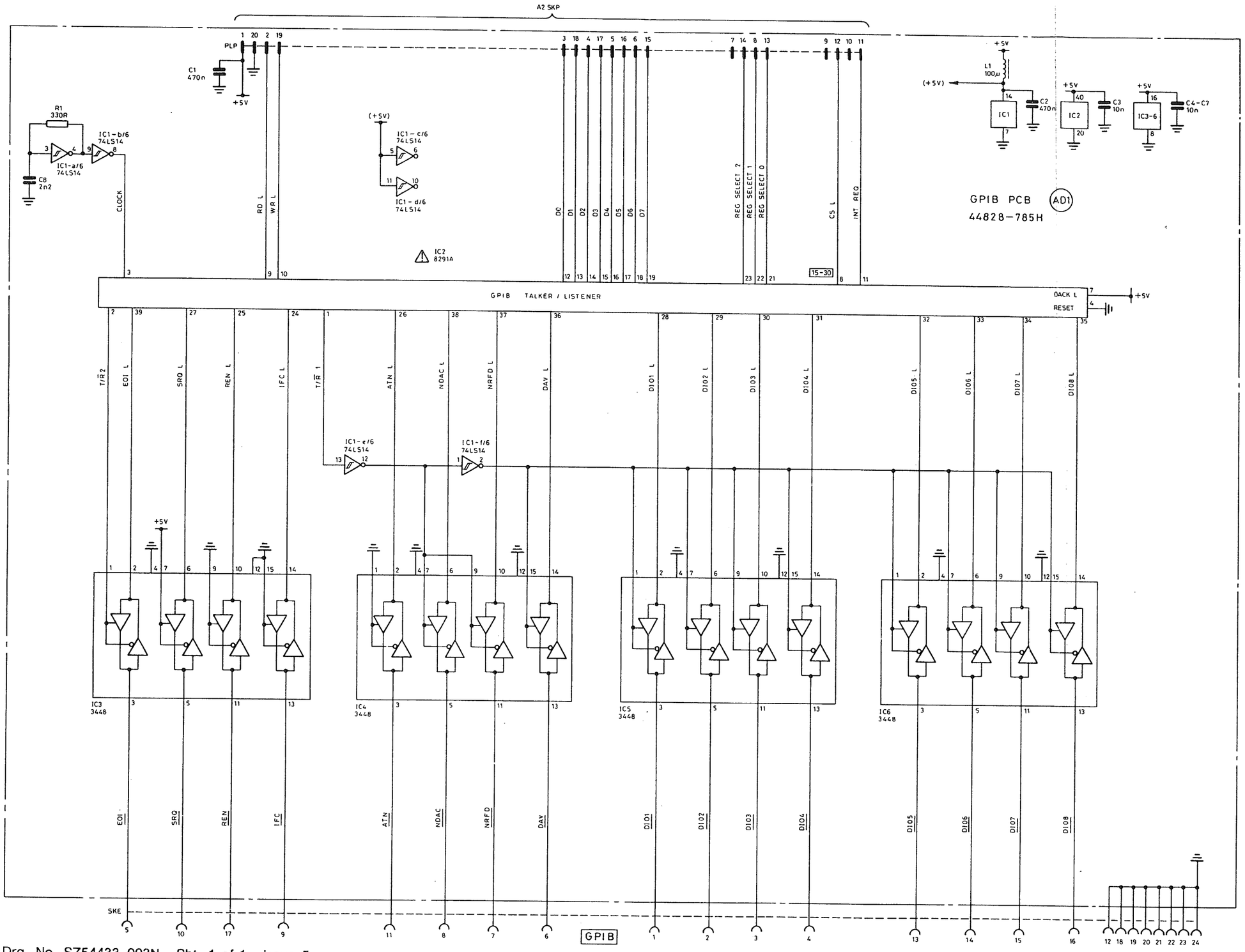


Fig. 7–11a GPIB module, component layout, AD1

1. COMPONENT MARKED ⚠ IS STATIC SENSITIVE, SEE PCH 22810 FOR PRECAUTIONS.
2. UNDERLINED LABELS REFER TO GPIB TERMS WHICH ARE NEGATIVE TRUE. ALL OTHER LABELS ARE POSITIVE TRUE.
3. PLP: 20 POS. DIL.
4. DIGITS IN BOX ▭ SHOW LATCH ADDRESSES WHEN USING SECOND FUNCTION 3.



Drg. No. SZ54433-003N Sht. 1 of 1 Issue 5

Fig. 7-11 GPIB module, AD0

Fig. 7-11
46881-891U
Oct. 88