CONTENTS

HAZARD WARNING SYMBOLS

The following symbols appear on the equipment

Symbol	Type of hazard	Reference in manual
⚠	Static sensitive device	Page (iv)
⚠	Component containing beryllia	Page (iv)

Note ...

Each page bears the date of the original issue or the code number and date of the latest amendment (Am. 1, Am. 2 etc.). New or amended material of technical importance introduced by the latest amendment is indicated by triangles positioned thus >.....< to show the extent of the change. When a chapter is reissued the triangles do not appear. Any changes subsequent to the latest amendment state of the manual are included on inserted sheets coded C1, C2 etc.

SECURITY NOTICE

Second functions are grouped into three levels of operation. Access to the first two groups, Normal and First level operation can be freely gained by carrying out the unlocking procedures described in both Operating manual and Service Manual. Details for accessing the Second level operation however, is only included in the Service manual. Some user units may wish to further restrict the distribution of this information to selected calibration areas only. To enable this, an alternative Chapter 4, page 39a/40a has been included which has the unlocking procedure deleted. Users may then withdraw either page 39/40 or 39a/40a as required.

AM/FM SYNTHESIZED SIGNAL GENERATOR

2018A (Code No. 52018-910P)
80 kHz - 520 MHz

and

2019A (Code No. 52019-910E)
80 kHz - 1040 MHz

AMENDMENT RECORD

The following amendments are incorporated in this manual.

Amendment No.	Date	Issued at Serial Number
Commencing	June 84	118443-001
Am. 1	Jan. 85	118444-001
Am. 2	Apr. 85	118445-001
Am. 3	Mar. 88	351153/4

Part No. 46881-512Z
Print code : H-3/88, MI 1.c

CAUTION : STATIC SENSITIVE COMPONENTS

Components identified with the symbol ⚠ on the circuit diagrams and/or parts lists are static sensitive devices. The presence of such devices is also indicated in the equipment by orange disks, flags or labels bearing the same symbol. Certain handling precautions must be observed to prevent these components being permanently damaged by static charges or fast surges.

(1) If a printed board containing static sensitive components (as indicated by a warning disk or flag) is removed, it must be temporarily stored in a conductive plastic bag.

(2) If a static sensitive component is to be removed or replaced the following anti-static equipment must be used.

A work bench with an earthed conductive surface.

Metallic tools earthed either permanently or by repeated discharges.

A low-voltage earthed soldering iron

An earthed wrist strap and a conductive earthed seat cover for the operator, whose outer clothing must not be of man-made fibre.

(3) As a general precaution, avoid touching the leads of a static sensitive component. When handling a new one, leave it in its conducting mount until it is required for use.

(4) If using a freezer aerosol in fault finding, take care not to spray programmable ICs as this may affect their contents.

CAUTION : LCD HANDLING

When operating or servicing this equipment take care not to depress the front or rear faces of the display module as this may damage the liquid crystal display elements.

WARNING : HANDLING HAZARDS

This equipment is formed from metal pressings and although every endeavour has been made to remove sharp points and edges care should be taken, particularly when servicing the equipment, to avoid minor cuts.

WARNING : TOXIC HAZARD

Many of the electronic components used in this equipment employ resins and other chemicals which give off toxic fumes on incineration. Appropriate precautions should therefore be taken in the disposal of these items.

Beryllia (beryllium oxide) is used in the construction of the following components in this equipment :

⚠ Unit AC4 : Transistor TR10

This material, when in the form of fine dust or vapour and inhaled into the lungs, can cause a respiratory disease. In its solid form, as used here, it can be handled quite safely although it is prudent to avoid handling conditions which promote dust formation by surface abrasion.

Because of this hazard you are advised to be very careful in removing and disposing of these components. Do not put them in the general industrial or domestic waste or despatch them by post. They must be separately and securely packed and clearly identified to show the nature of the hazard and then disposed of in a safe manner by an authorized toxic waste contractor.

Chapter 4

TECHNICAL DESCRIPTION

CONTENTS

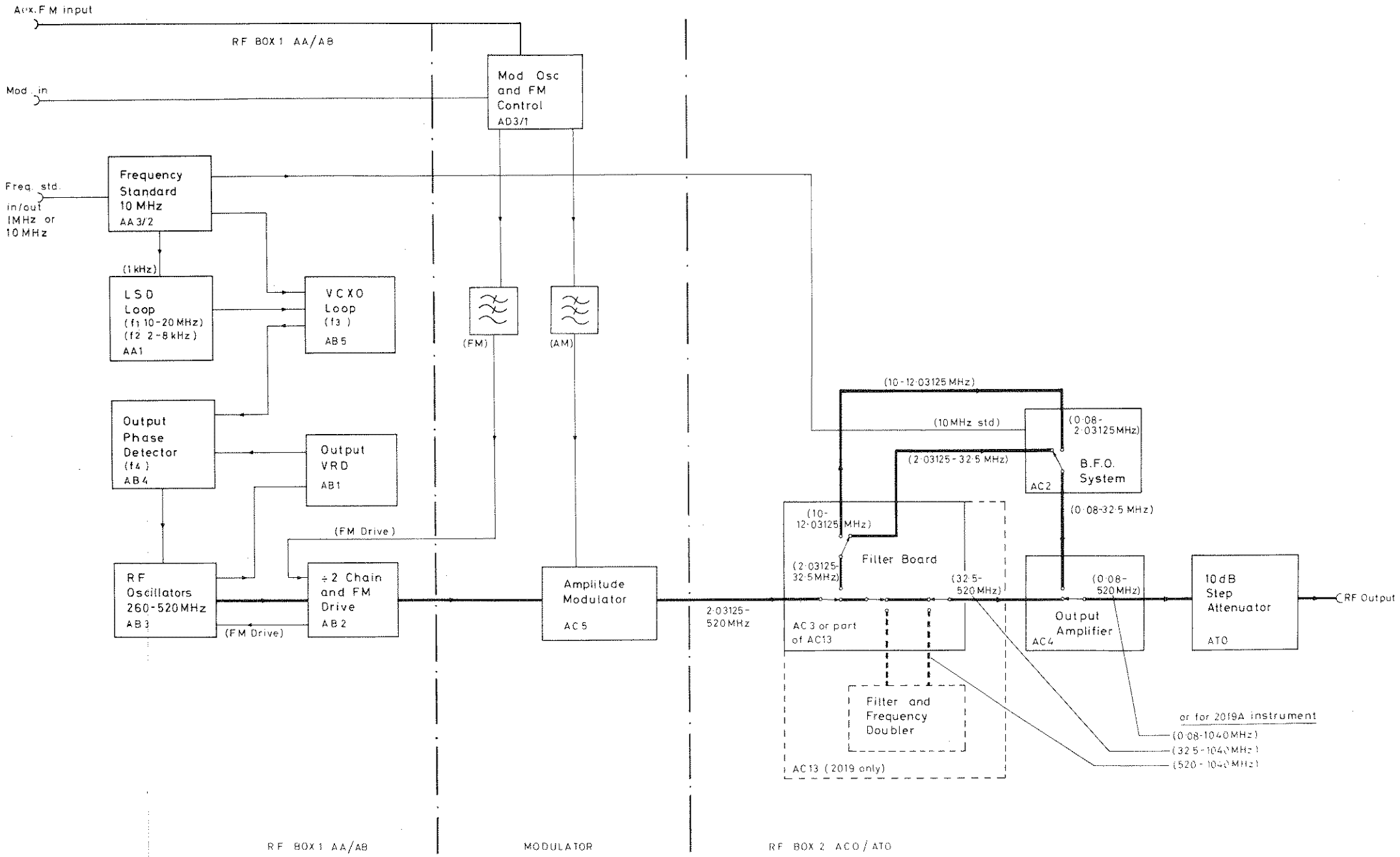


Fig. 1 Simplified block diagram of 2018A/2019A frequency synthesis and signal processing

INTRODUCTION

1. The 2018A is an 80 kHz to 520 MHz synthesized signal generator providing calibrated output levels from -127 dBm to +13 dBm. 2019A is an 80 kHz to 1040 MHz synthesized signal generator similar to 2018A except that a frequency doubler circuit enables it to cover frequencies up to 1040 MHz with the same output level range. The output frequency of both 2018A and 2019A is phase locked to a frequency standard and can be set to a resolution of 10 Hz at frequencies up to 520 MHz and to a resolution of 20 Hz above 520 MHz (2019A only).

2. Both instruments can be frequency, phase or amplitude modulated from external or internal modulation sources. The internal modulation source provides six fixed modulation frequencies; re-selection of components within the instrument allows alternative frequencies to be set if required.

3. Calibrated output levels from -127 dBm to +13 dBm (0.2 μV to 2 V e.m.f.) in the c.w., ϕ.m. and f.m. modes and up to +7 dBm (1 V e.m.f.) in the a.m. mode are provided. A choice of nine output level calibration units can be obtained on the front panel. The r.f. output level can be set to a resolution of 0.1 dB or better over the entire output voltage range and features a total cumulative accuracy of ±1 dB up to 520 MHz (±2 dB, 520 MHz - 1040 MHz). Protection against the accidental application of up to 50 W of reverse power is provided by a fast responding reed relay.

4. Front panel operation is carried out by direct entry of required settings via the keyboard. Microprocessor control ensures maximum flexibility and allows programming by the General Purpose Interface Bus (GPIB). This facility is offered as an optional accessory enabling the instrument to be used both as a manually operated bench instrument or as part of a fully automated test system. Facility is also made for the use of an external standard reference when this is preferred.

5. A second function mode of operation includes means of setting the GPIB address, selection of alternative r.f. level calibration units, access to various calibration routines and a facility to aid diagnostic fault finding and a measure of the total number of hours that the instrument has been switched on.

OVERALL TECHNICAL DESCRIPTION

6. The 2018A/2019A Signal Generator is divided into three main areas. The first area is the digital control system by which the microprocessor board AA2/1 receives and sends data to the various p.c.b's in the instrument. This is accomplished by means of an internal instrument bus.

7. The second area consists of a frequency synthesizer and the analogue signal conditioning circuits that are controlled by the data bus in order to produce the required output signal.

8. The third area is the modulation control system controlling the audio signals used to amplitude modulate (a.m.), frequency modulate (f.m.) or phase modulate (ϕ.m.) the carrier output.

Digital control system

Circuit diagram : Chap. 7, Fig. 3

9. The internal data bus consists of a total of 17 control lines. The first eight lines (D0 to D7), are data lines. The data bus is bi-directional e.g. data may be input into the microprocessor via the front panel keyboard or control data can be sent to the data latches from the microprocessor.

10. The next four lines (A0 to A3), are address lines. These are used to control the address of the latch to which the data is to be sent or from which data is being read.

11. The next four lines (A4 to A7) are data valid lines. A0 to A3 lines are fed to address decoders and with it one of the data valid lines A4, A5, A6 or A7 is connected to each address decoder. Only when this line is activated '0' low is the decoder enabled, and its decoded output then activates the required data latch.

12. The last control line (A8) is the GPIB interrupt line. This line calls for the microprocessor to service the GPIB module.

13. Bus interconnections are shown in Chap. 7, Fig. 5 Servicing diagrams. The microprocessor AA2/1 serves as the motherboard in the top r.f. box. Some of the data is latched on AA2/1 in order to minimize the number of interconnections. The addresses of the other latches are also decoded on AA2/1 to minimize interconnections. The entire 17 line data bus is connected to AD2 motherboard via an r.f. filter box. The filter box ensures that r.f. signals are not conducted down the data bus. From the motherboard the data bus is distributed to the boards outside the top r.f. box. A further connection is made to the lower r.f. box containing AC2, AC3, AC4 and AC5 via a second filter box.

Frequency synthesizer and signal processing

Circuit diagram : Chap. 7, Fig. 1

14. The frequency synthesizer provides a stable frequency source at the output of AB3 RF oscillators board covering the frequency range 260 MHz to 520 MHz that is phase locked to the internal frequency standard, board AA3/2 with a resolution of 10 Hz. As an aid to deriving the frequency at any point in the synthesizer the output frequency from AB3 is considered to be of the form

$$fo = m \times 100000 + n \times 10$$

where m is between 2600 and 5200
n is between 0000 and 9999

If an output frequency of 512.34567 MHz is selected then m = 5123 and n = 4567 and the cutput

$$fo = \frac{2\,(m-1)}{200}\left[10^7 + \frac{(10^4 + n)\ 10^3}{m-1}\right]$$

Intermediate frequencies at significant points within the synthesizer are given as f1, f2, f3 and f4 and are shown on the simplified block diagram Chap. 7, Fig. 1. Each frequency can be determined by applying one of the following formulae :

$$f1 = (10^4 + n)\ 10^3 = 14.567000 \text{ MHz}$$

$$f2 = \frac{(10^4 + n)\ 10^3}{m-1} = 2.844006 \text{ MHz}$$

$$f3 = 10^7 + \frac{(10^4 + n)\ 10^3}{m-1} = 10.002844 \text{ MHz}$$

$$f4 = \frac{10^7 + \dfrac{(10^4 + n)\ 10^3}{m-1}}{200} = 0.05001422 \text{ MHz}$$

$$fo = \frac{2\ (5122)}{200}\left[10^7 + \frac{(10^4 + 4567)\ 10^3}{5122}\right] = 512.34567 \text{ MHz}$$

15. The internal frequency standard is derived from a temperature controlled crystal oscillator on AA3/2 which is free running when internal standard is selected. If external standard is selected a 1 MHz signal derived from the internal oscillator is phase compared with a 1 MHz signal derived from the external standard. The phase detector output corrects the internal standard frequency such that it is phase locked to the external standard. When internal standard is selected the output from the phase detector is an open circuit.

16. The least significant digit (l.s.d.) loop, board AA1 phase locks an oscillator covering the frequency range 10 to 20 MHz to multiples of 1 kHz. The resulting signal is divided by m-1 in a variable ratio divider (v.r.d.) before being fed to the voltage controlled crystal oscillator (v.c.x.o.) board AB5. Its frequency is then between 2 and 8 kHz. VCXO board AB5 then phase locks to the sum frequency of 10 MHz and the 2 to 8 kHz signal from AA1. The resulting 10.002 to 10.008 MHz signal is divided by 100 before being fed to AB4 Output phase detector board. The phase detector on AB4 is used to lock the oscillators on AB3 to the required output frequency. AB3 output is divided by 2(m-1) by a v.r.d. on board AB1. The resulting signal has a frequency of between 50.01 and 50.04 kHz and is fed to AB4.

17. If the instrument has not been set to provide f.m. the phase detector system operates at the frequency of 50.01 to 50.04 kHz. However if f.m. is selected, the phase locked loop bandwidth is reduced to avoid the loop removing the required f.m. The frequencies are then divided by 5 before phase comparison and an alternative phase detector and loop filter is used with a lower gain. The resulting signal from AB3 is therefore a 260 to 520 MHz carrier phase locked to the internal frequency standard and is frequency modulated if required. The divide-by-two system on AB2 divides the output from AB3 so that it can provide output frequencies of between 2.03125 MHz and 520 MHz. The output at this point is a nominal square wave.

18. The output from AB2 is connected via a semi-rigid cable to AC5 Amplitude modulator in the lower r.f. box. AC5 contains a double balanced mixer that is used as an amplitude modulator. The resulting amplitude modulated signal is then passed on to AC3 or AC13 board. These are different versions of the same board, AC3 Filter board in 2018A, or AC13 Filter and frequency doubler board in 2019A. If the output signal level from the instrument is required to be greater than +7 dBm then AC5 is set to give its peak envelope power of nominally -5 dBm provided the amplitude modulation is <u>off</u>. The output from AC5 is nominally a square wave.

19. The signal into AC3/AC13 is divided into two main paths. Frequencies from 2.03125 MHz to 32.5 MHz are routed via a buffer amplifier to a bank of filters operating in a 200 Ω characteristic impedance system. The filters convert the square wave into a sinusoidal signal. In order to generate a 0.08 to 2.03125 MHz band a 10 MHz to 12.03125 MHz signal is routed to AC2 BFO system where the signal is mixed with 10 MHz from the internal frequency standard and filtered to produce an 80 kHz to 2.03125 MHz sine wave. Frequencies below 80 kHz may be selected but the accuracy of the r.f. level output may be impaired.

20. The output from AC2 is a nominal 40 mV, 80 kHz to 32.5 MHz sine wave operating in a 200 Ω system. This signal is fed to AC4 Output amplifier board where it is amplified by a variable gain amplifier, the gain of which is controlled by two j.f.e.t's used as voltage controlled variable resistors. The output from the variable gain amplifier is connected to the output stage amplifier where the output signal level is detected by an r.f. detector. The resulting d.c. signal is compared to a variable reference voltage by a comparator. The comparator output controls the gain of the j.f.e.t. variable amplifier so as to obtain the correct output level from AC4.

21. The 32.5 MHz to 520 MHz signal on AC3/AC13 is switched to an amplifier and a 520 MHz low-pass filter. If the instrument is a 2019A the signal can then be switched to a frequency doubler and filter system to generate a 520 to 1040 MHz signal.

22. In both 2018A and 2019A the signal from the 520 MHz low-pass filter goes through a filter bank to produce a sinusoidal output signal which is then fed to AC4 output amplifier.

23. The 32.5 to 520 MHz (or 1040 MHz for 2019A) signal is amplified by a pin diode controlled variable gain amplifier and is then connected to the output stage. The output level from AC4 is controlled by an a.l.c. system consisting of an r.f. detector, comparator and two variable gain amplifiers (j.f.e.t. and pin diode controlled). The level is normally varied over the range +7 dBm to -3 dBm by controlling the reference voltage to the a.l.c. If levels greater than +7 dBm are requested and the a.m. is off the level is increased up to a maximum of +13 dBm. The reference voltage to the a.l.c. is also varied to compensate for the insertion loss of the attenuator, cables and connectors that connect the output signal to the front panel.

24. The attenuator provides electro-mechanical attenuation of the output signal from AC4. Provision is made to attenuate the output signal in 10 dB increments from 0 dB to 120 dB. The attenuator output is connected to a reverse power protection system (RPP) which protects the attenuator pads from the accidental application of reverse power. The RPP uses a coaxial reed relay to open circuit the output of the signal generator and can be reset from the front panel or by the GPIB.

Modulation control and AF level system

Circuit diagram : Chap. 7, Fig. 1

25. The internal modulation oscillator is a j.f.e.t. stabilized Wien bridge oscillator which can be programmed to one of six frequencies. These frequencies can be altered by the user by changing two resistor values for each frequency.

26. The AF Level output is derived from the modulation oscillator using a system of digital-to-analogue converters and attenuators to provide audio level and range control. The external modulation input is optionally levelled by an audio ALC system which uses a j.f.e.t. as a variable resistor in an attenuator.

27. A switch system enables either the internal or external modulation source to be selected. Further switches enable either AM, FM or ϕM to be generated. With AM selected the signal is routed via the motherboard, AD2, and the lower RF filter box to a digital-to-analogue converter on AC5. This controls the level of audio applied to the amplitude modulator according to the required AM depth.

28. With FM selected the modulating signal level is first modified by a digital-to-analogue converter in accordance with the FM tracking data. This data is stored in the non-volatile store on the microprocessor board AA2/1. The FM tracking data is stored at 84 frequencies across the fundamental octave band of the instrument (260 to 520 MHz). The microprocessor provides straight line interpolation between these carrier points and sends the resulting 8-bit data to the tracking D-A.

29. The signal is then processed by a 10-bit D-A, this controls the signal level in accordance with the required f.m. deviation. The 10-bit D-A also takes account of the scaling factors introduced by following D-A's and the frequency division of the carrier by the r.f. signal conditioning circuit. The f.m. drive signal is attenuated by an 8-bit D-A which divides the audio signal level by successive factors of two. This effectively sets the f.m. range. The signal is then fed to a filter box on the upper r.f. box, and from there to AB2 Divide-by-two chain and f.m. drive board. This board provides further variable division of the signal level by factors of four using reed relay switches to provide further scaling of the f.m. range. The output of AB2 is then connected to AB3 RF oscillators to frequency modulate the oscillator.

30. Phase modulation is derived by switching a differentiating circuit into the FM system. Since phase modulation is the differential of frequency modulation this converts the frequency modulation system into an apparent phase modulation system.

DETAILED TECHNICAL DESCRIPTION (BOARD LEVEL)

(AA1) - LSD loop

Circuit diagram : Chap. 7, Fig. 6

31. This board contains the circuits which control the four least significant digits (l.s.d.) of the carrier wave output frequency. The board provides the reference input to the phase detector on the voltage controlled crystal oscillator (v.c.x.o.) loop AB5. Control data for the l.s.d. loop is brought to four 8-bit latches IC8 to IC11 via the instrument bus.

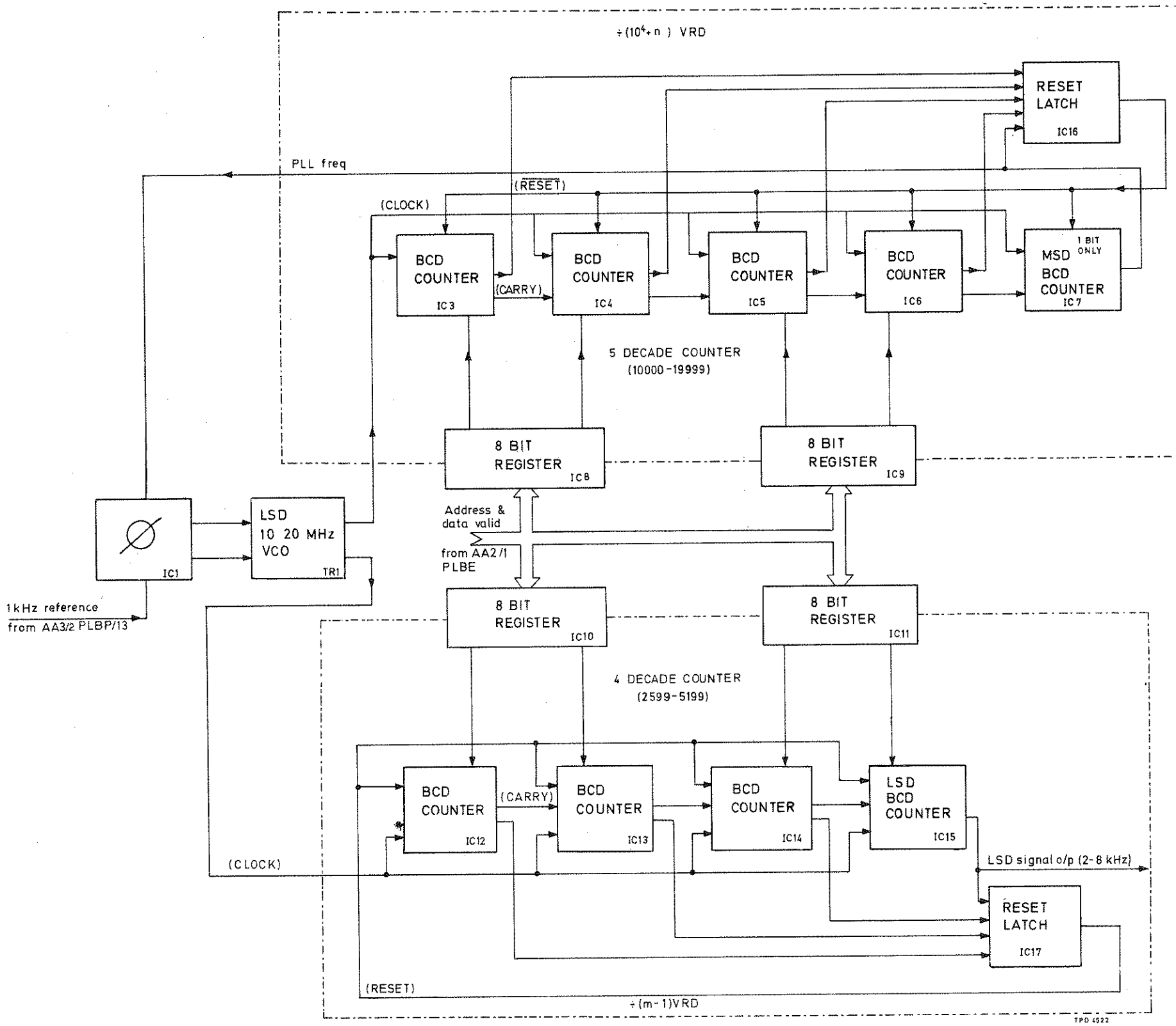


Fig. 2 LSD loop (AA1)

32. The LSD loop consists of a phase locked loop built around a 10-20 MHz voltage controlled oscillator (v.c.o.) whose output is divided by a five decade variable ratio divider (v.r.d.) and then fed to a phase detector where it is phase compared with a 1 kHz reference signal derived from the frequency standard board AA3/2. The output from the phase detector is filtered and the resulting d.c. signal is used to control the v.c.o. The control voltage changes the v.c.o. frequency so as to annul any phase error at the phase detector, and establish phase lock. The modulus of the v.r.d. controls the frequency of the v.c.o..

33. After buffering, the v.c.o. signal is fed to each clock input of the five decade counters IC3 to IC7 comprising the v.r.d. The v.r.d. will count upwards whilst the 8 (QD) and 1 (QA) output of each counter are monitored by a multi-input NAND gate IC16. When all the monitored outputs reach the high state the $\overline{\text{RESET}}$ line will go low '0'. On the arrival of the next clock pulse, the data held in the latches IC8 and IC9 is loaded into the counters. The data consists of the nines complement of the required division ratio (IC7 is hardwired to load in 8). Because a clock pulse is required for reloading the counter this pulse does not increment the counter. To compensate for this missed pulse the NAND gate IC16 is wired to detect the v.r.d. state 99998 for the end of each count sequence rather than 99999. The v.r.d. is capable of dividing by any integer value between 10000 and 19999.

34. The $\overline{\text{RESET}}$ line in the v.r.d. also drives one input of the phase detector, IC1, the other being driven by the 1 kHz reference signal. If the $\overline{\text{RESET}}$ frequency is below 1 kHz, a stream of current pulses will be driven into the loop filter (C1, C2, R1) by transistor TR2, this raises the v.c.o. control voltage causing the $\overline{\text{RESET}}$ frequency to rise towards 1 kHz. Similarly if the $\overline{\text{RESET}}$ frequency is above 1 kHz, a stream of current pulses will be drawn from the loop filter by transistor TR3 to lower the control voltage. When phase coincidence is obtained, equal but opposite pulses by TR2 and TR3 are produced thus maintaining the correct control voltage; these pulses are typically 30 nanoseconds wide.

35. Another buffered output from the v.c.o. goes to a four decade v.r.d. (IC12 to IC15) which works in a similar manner to the one described above. The microprocessor ensures that the modulus of this v.r.d. falls between 2599 and 5199, according to the required carrier wave output frequency. The l.s.d. signal output is available at PLBN and has a frequency range of approximately 2 kHz to 8 kHz.

AA2/1 - Microprocessor system

Circuit diagram : Chap. 7, Fig. 7

36. The microprocessor board AA2/1 contains the whole system necessary to drive both address and data bus lines which control the instrument. The 8085A Microprocessor IC9 has an 8-bit multiplexed data/low order address bus which is demultiplexed by the latch IC21.

37. The program is contained in IC1, 2, 3 and 4, all of which are ultra -violet erasable PROMs. These are enabled by IC17 which decodes A13, A14, & A15 of the address bus. The program space is contiguous from address 0000 to 7FFF.

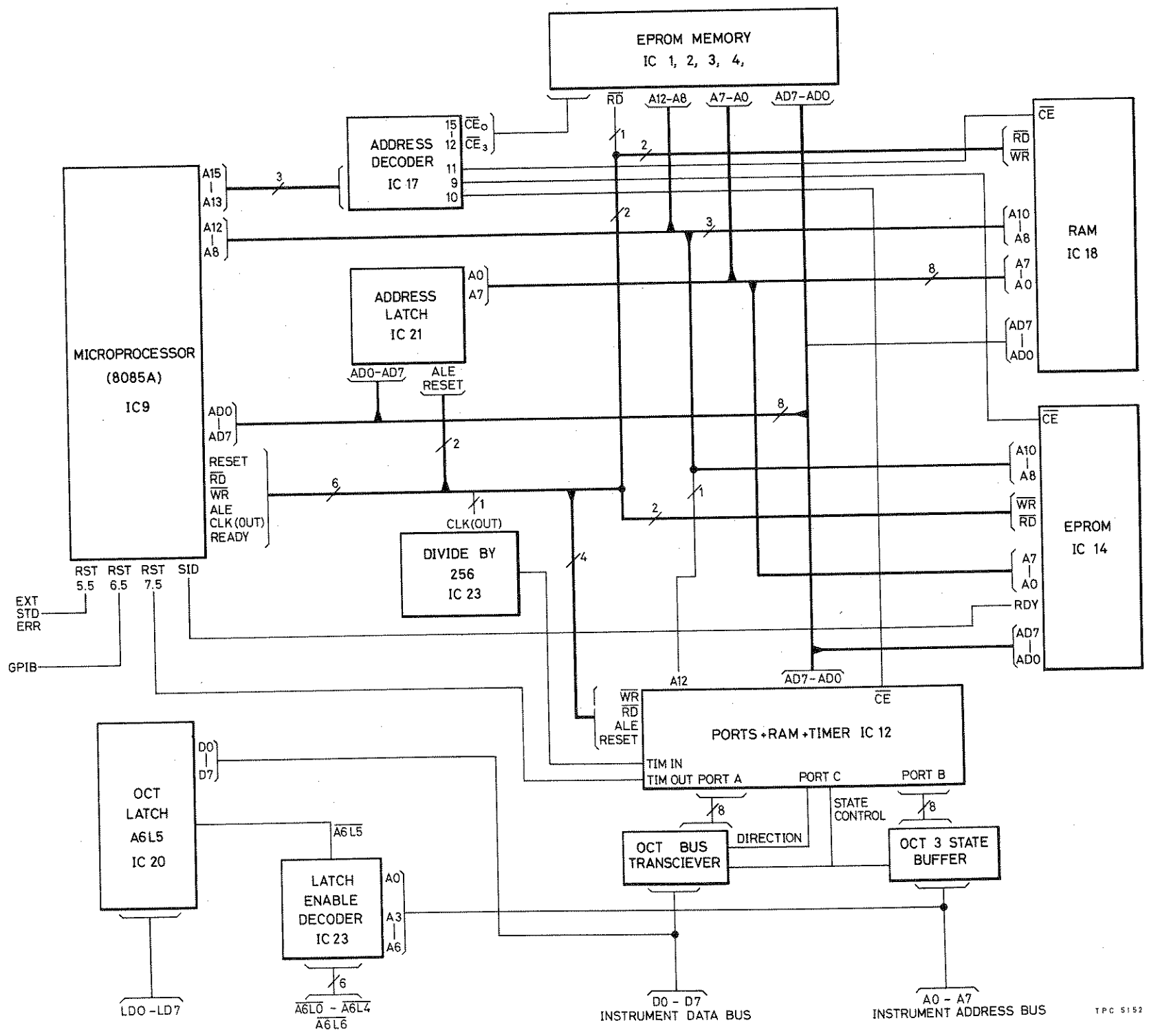


Fig. 3 Microprocessor system (AA2/1)

38. IC14 contains 2 K bytes of RAM at addresses 8000 - 8FFF. This is the instrument's primary RAM. IC12 contains 256 bytes of RAM (read/write), with addresses 0A000 to 0A0FF. This contains the stack. Port A (pins 21 - 28) in IC12 carries the instrument's 8-bit bi-directional data bus via a bus transceiver IC10, and Port B (pins 29 - 36), via IC11, the instrument's address bus. This is in the form of 4 address lines (bits A0 - A3) and uncoded data valid lines (bits A4 - A7) giving a total of 64 available latch addresses.

39. The mode of operation of the address bus is that the required address is presented to the bus with bits A4 - A7 high and the bus is allowed to settle. Then the required data valid line is activated by pulling it low, which either latches the information on the data bus onto the addressed latch (for outputs from the microprocessor) or allows the addressed data source to drive the data bus (for inputs to the microprocessor: either from keyboard or GPIB board). The data valid lines are thus only activated when a valid (and stable) address is present on the other 4 address lines. The direction of the data bus buffer is controlled by a line on Port C of IC12 (pin 39).

40. IC13 is the decoder for the first 7 addresses served by data valid line A6 (i.e. it supplies chip enables corresponding to bus addresses A6L0 to A6L6), and IC20 is the A6L5 data latch, used to hold the information which selects which oscillator is in use via AB4, and other signal routeing information on AA3/2.

41. IC14 contains 2 kbytes of non-volatile electrically alterable ROM which holds calibration data in the address range C000 to C7FF. To ensure that the integrity of data in the non-volatile memory is maintained, it is essential that there is no risk of writing to it whilst the microprocessor is not completely functional. This can occur if the +5 V rail falls to some undefined level. In this event, IC19 and its essential circuit will come into operation. IC19 is a comparator that compares the +5 V rail with a stabilized voltage derived from the +24 V rail. If the +5 V rail falls below 4.5 V the RESET LINE of the microprocessor (IC9) will be held low due to TR2 being turned on. This inhibits operation of the microprocessor until the +5 V rail rises above the +4.5 V at which time the 2022 will re-initialize itself. This circuit is in addition to the initial protection against low supply volts present in EPROM IC14.

42. The time elapse system is generated by dividing the microprocessor clock output by a factor of 256 in IC23 and using this to drive the timer function in IC12. The timer output from IC12 drives the RST 7.5 interrupt on IC9 at a rate of approximately 0.8 Hz. The interrupts are software counted to provide a time elapse function, using the non-volatile store, to update the stored value every 15 minutes elapsed time. A software coding system is used to minimize wearout mechanisms in the non-volatile store.

Circuit diagram : Chap. 7, Fig. 8

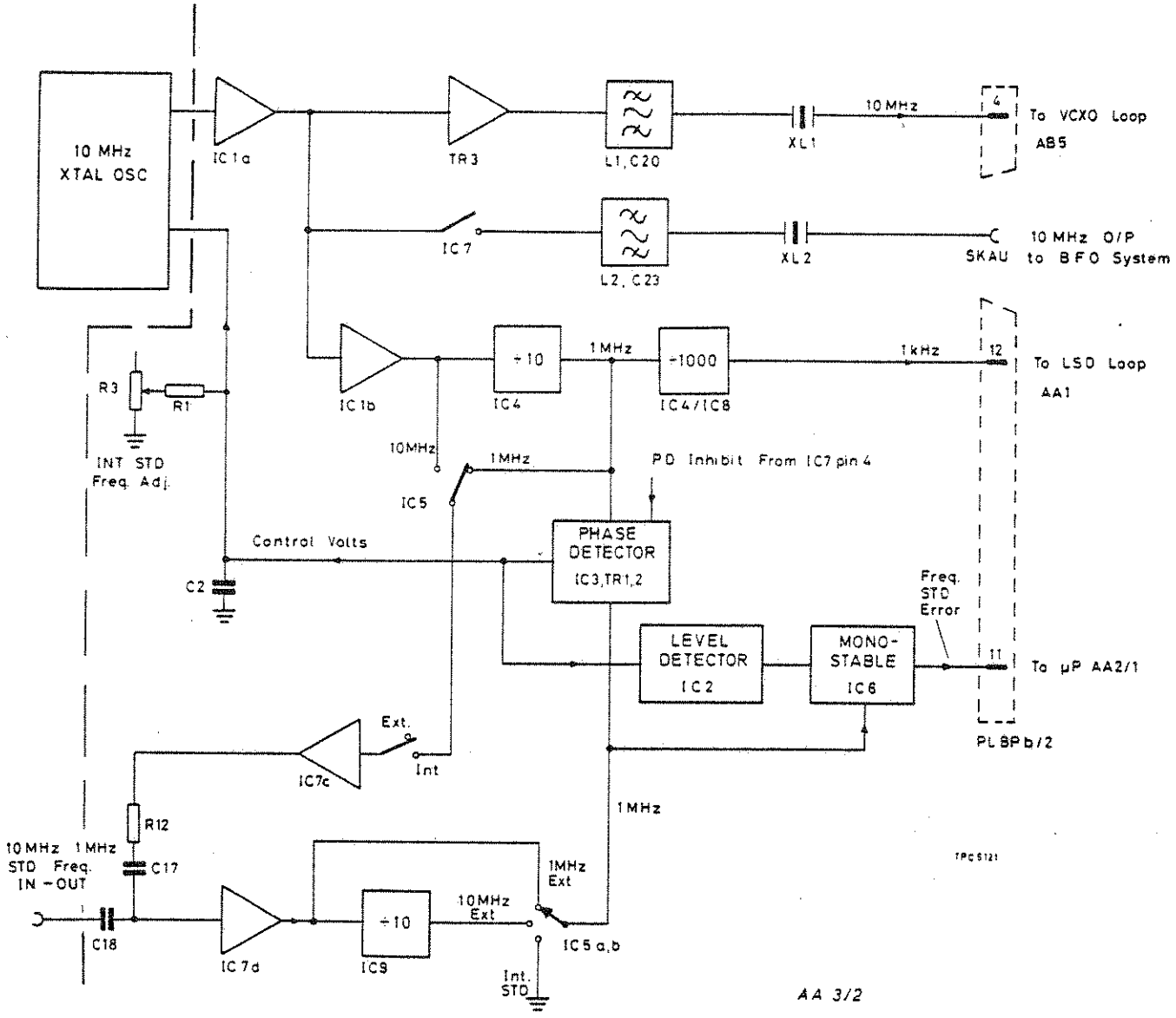


Fig. 4 Internal/external frequency standard (AA3/2)

43. AA3/2 provides the frequency standard required as a master frequency reference for the synthesizer. Control data is brought from the latch on AA2/1 via feed-through capacitors to PLBPa/2. If INT standard is selected (INT/EXT STD high) the phase detector IC1d Q/4 is cleared and TR1, TR2 are turned off. The frequency of the crystal osc. is controlled by the setting of R3. The 10 MHz output from the crystal osc. is distributed as reference for the instrument. TR3, L1, C20 produce a nominal 10 MHz sine wave which is further filtered by XL1 and routed via PLBPb/2 to AB5 VCXO loop.

44. A 1 kHz reference is generated for use on AA1 by dividing the 10 MHz by 10000 using IC4 and IC8. If carrier frequencies below 2.03125 MHz are selected the BFO ON line is low and a 10 MHz signal, filtered by L2, C23 and XL2, is supplied to SKAU for use in the BFO system on AC2.

45. If the instrument has been set to operate on a 10 MHz frequency standard the 10 MHz/$\overline{1\ \text{MHz}}$ line is set high and the 10 MHz frequency standard signal on IC5 pin 3 is routed to IC5 pin 4. If INT STD has been selected the signal is then routed via SKAR to the rear panel. If a 1 MHz standard has been selected then the 1 MHz signal on IC5 pin 2 is routed to IC5 pin 4. If INT STD has been selected the 1 MHz signal is routed via SKAR to the rear panel.

46. If EXT STD is selected the internal standard output is turned off by IC7c/4 and the external standard is enabled by IC7d/4. If the instrument is set to work from a 10 MHz standard a 1 MHz external standard is passed on to IC5 pin 7 via the divider IC9. If the instrument is set to a 1 MHz standard the 1 MHz external standard is passed directly to IC5 pin 7 via IC5 pin 5. IC3 compares the phase of the internal 1 MHz on pin 3 with the external 1 MHz on pin 11. The phase detector transistors TR1, TR2 drive the phase locked loop filter, C2 and R1, to phase lock the internal reference crystal osc. to the external reference.

47. IC2 and IC6 are used to generate an interrupt signal for the microprocessor on PLBPb/2 pin 11. If the voltage supplied to pin 5 of the crystal osc. is out of limits (that is <0 V or >5 V), then IC6 is cleared (pin 5 low) and IC6 pin 6 is set high (interrupt enabled). Similarly if the 1 MHz external standard frequency is not present on IC6 pin 1 then IC6 pin 6 is again set high. If everything is correct then IC6 is constantly retriggered by pin 1 and pin 6 is low. If the interrupt on pin 11 PLBPb/2 is high and external standard is selected then the microprocessor displays an error message on the front panel.

AB1 - Output v.r.d.

Circuit diagram : Chap. 7, Fig. 9

48. The board AB1 contains the high speed variable ratio divider (v.r.d.) which is used in the output phase locked loop to control the four most significant digits of the carrier wave output frequency. The v.r.d. is driven by a signal from the r.f. oscillator board, AB3, and provides the signal for the output phase detector, AB4. Control data for the v.r.d. is fed to two eight bit latches IC4 and IC5 via the instrument bus.

49. The r.f. input signal of approximately -6 dBm is amplified by TR1 and fed to a divide-by-two prescaler, IC1, to produce a frequency between 130 - 260 MHz at the input to IC2, pin 1. To operate at such a high speed a dual modulus (divide-by-10/$\overline{11}$) counter system is used. The dual modulus counter, IC2, initially divides by 11 its control line ÷10/$\overline{11}$ low, when the control line is high its modulus is 10. The state of this control line can change at any time whilst counting, but before the arrival of the eleventh pulse. Thus the time period available for a change of the control line is approximately ten times the input clock period.

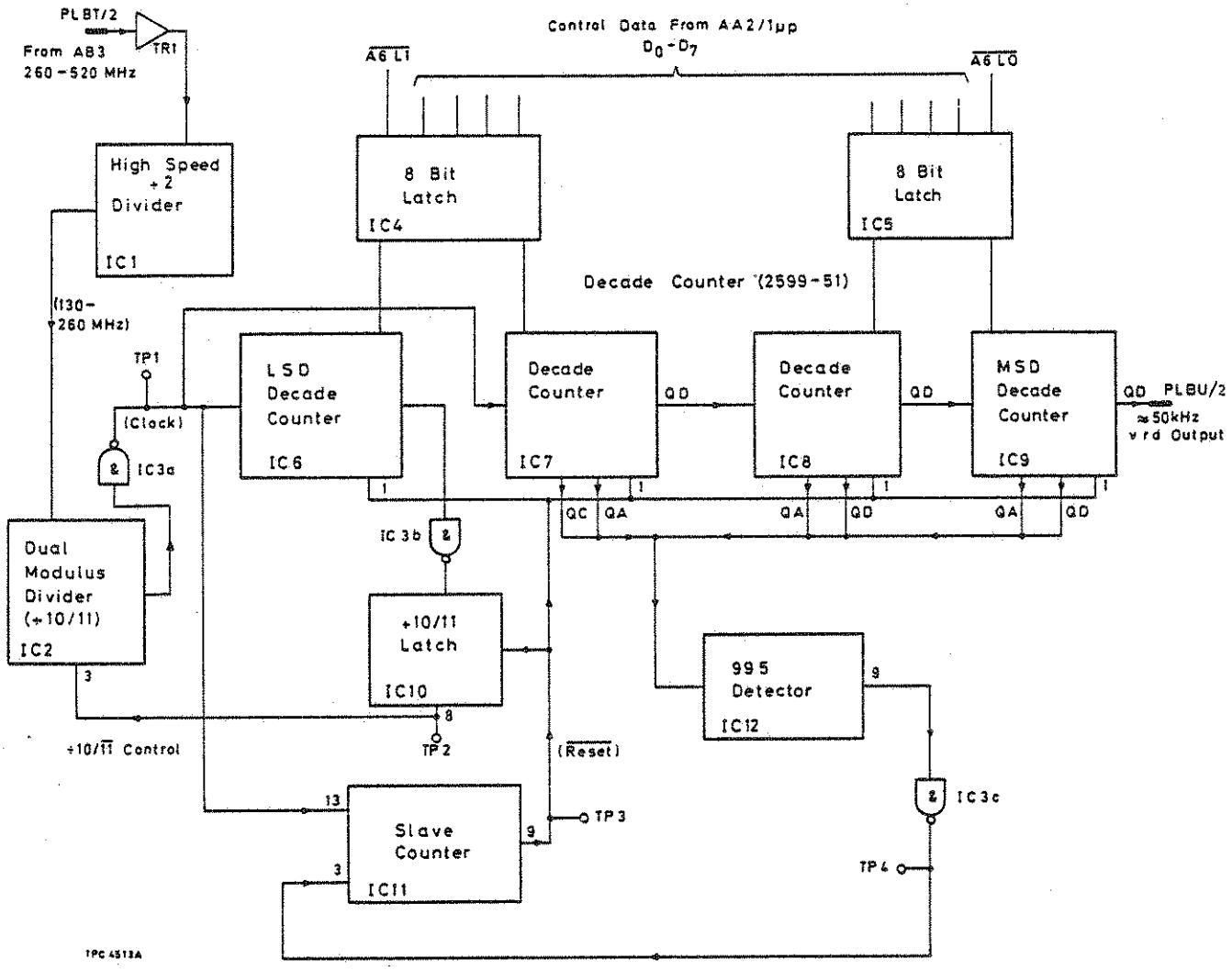


Fig. 5 Output v.r.d. simplified block diagram (AB1)

50. The output from the 10/11 counter drives the clock line, (TP1), for the chain of the presettable decade counters. Each counter is loaded with a nines complement number and counts upward with each pulse (falling edge at each pin no. 8). The two least significant counters, IC6 and IC7 are incremented simultaneously.

51. The 10/11 counter IC2 starts in the modulus 11 mode. After every 11 input pulses IC6 and IC7 are both incremented. When IC6 output reaches 9 (1001 in b.c.d.) a low level appears at IC3b, pin 3 causing TP2 to go high to set the 10/11 counter to divide by 10. IC7 is then incremented every 10 input pulses.

52. IC8 and IC9 are driven in cascade from IC7. IC6 will continue to count but there will be no further change at TP2 until the $\overline{\text{RESET}}$ pulse occurs. "The early decode" method is used at the end of each v.r.d. sequence in order to reset the decade counters for the next sequence. When the counters IC7, IC8 and IC9 reach the state 995, TP4 is asserted high, and the last four pulses at TP1 are counted by IC11 slave counter.

53. The pulse 997 will cause the $\overline{\text{RESET}}$ control line TP3 to be asserted low. This reloads the four decade counters to the nines complement data held in the 8-bit latches IC4 and IC5. Pulse 999 will cause TP3 to assert high once more to enable the counters and also to clock the flip-flop IC10 resetting TP2 low. This reverts IC2, the dual modulus counter to the modulus 11 mode and so the v.r.d. is ready for the next count sequence.

54. The microprocessor AA2/1 ensures that the modulus of the v.r.d. falls between 2599 and 5199 according to the required carrier wave output frequency. The v.r.d. output is taken from the "8" output (QD) of IC9 to PLBU, pin 2 and has a frequency of just over 50 kHz.

AB2 - Divide-by-two chain and f.m. drive

Circuit diagram : Chap. 7, Fig. 10

55. Board AB2 has two functions, the majority section is used for the divide-by-two chain and a minor section for the f.m. drive. The purpose of the divide-by-two chain is to divide the carrier frequency from AB3 down to the carrier frequency selected by the front panel keyboard or via the GPIB. The input frequency to AB2 is between 260 MHz and 520 MHz. Up to seven divide-by-two elements can be switched in to provide frequency cover from 260 MHz down to 2.01325 MHz.

56. If no division of the basic frequency is required (frequencies in the range 260 MHz - 520 MHz) the signal is instead routed directly to the output socket SKBX. Frequencies below 2.01325 MHz are derived on a different board, for details see (AC2) BFO system.

57. Seven bits of control data from AA2/1 microprocessor D0 - D6 are used to control the dividers, these are fed to IC8 octal latch via the instrument bus. Different logic technologies are used to implement the chain of dividers and consequently different methods are used to switch elements in and out.

58. The input signal of approximately -6 dBm comes in on SKBW and is amplified by TR1. It is then routed according to the state of latch output LD6 either

(1) To the output socket SKBX via TR4, other control lines ensure that TR6 is held off, or

(2) The state of LD5 controls the divided signal of IC1 which is either routed through TR8 and TR6 to the output (TR4 and TR7 both held off) or alternatively, used to clock the second divider IC2.

(3) Similarly, LD4 determines whether the output from IC2 is routed through IC6, TR7 and TR6 to the output or is used to clock the next divider IC3 and so on. Transistors TR12 and TR13 form an e.c.l. to t.t.l. interface. The two flip-flops in IC4 are driven synchronously with the control lines setting the division to divide-by-two or four as required. IC5 operates in a similar way.

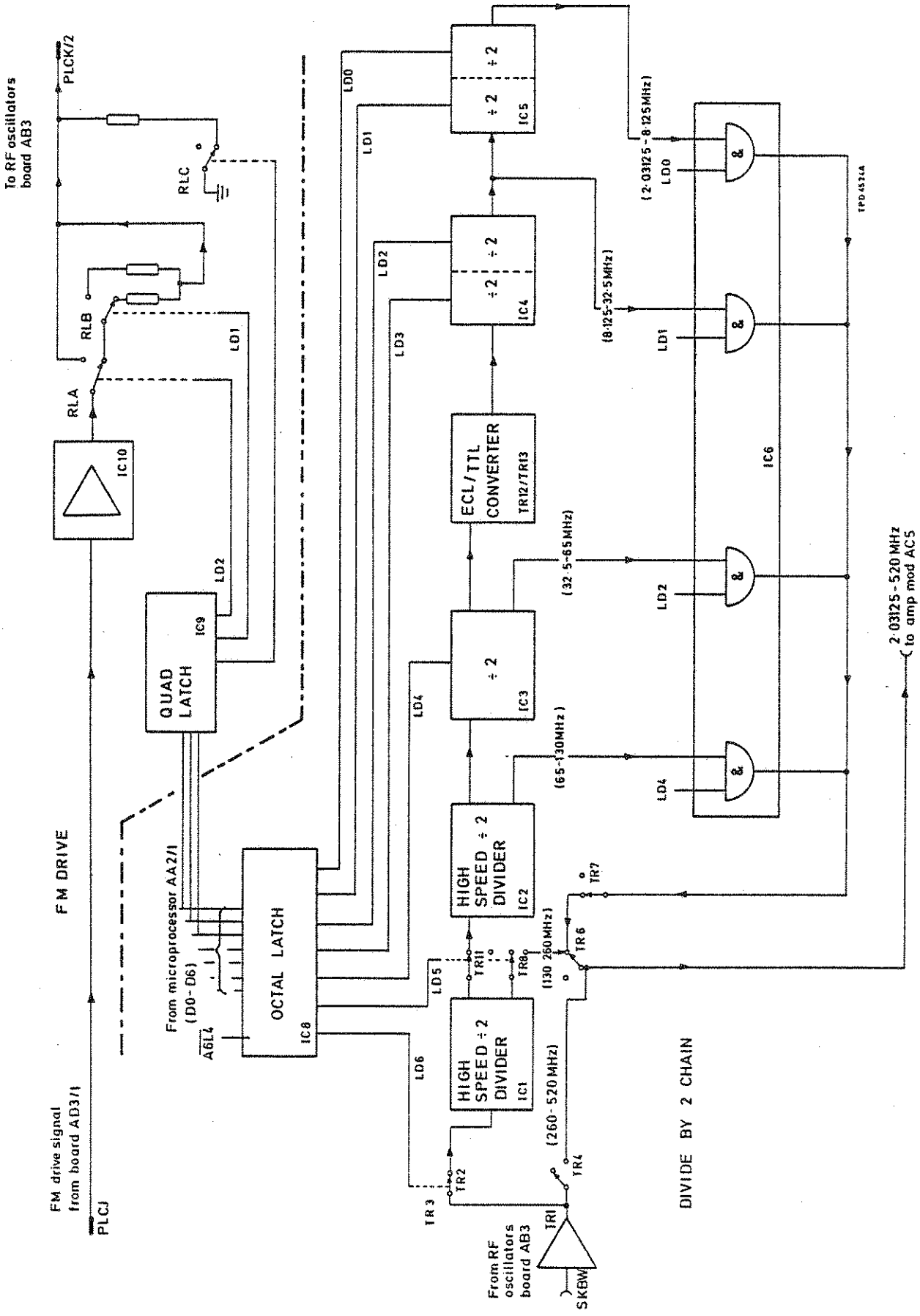


Fig. 6 Divide-by-two chain and f.m. drive (AB2)

59. The divider outputs are gathered together in an e.c.l. wired-OR configuration (IC6, TR7, TR8) so that at the output socket SKBX, all frequencies from 2.03126 - 520 MHz are available the nominal level being 0 dBm.

60. The f.m. drive circuit on AB2 provides the coarse adjustment of the f.m. drive voltage delivered to the r.f. oscillators on AB3. Three bits of control data D0 - D2 are used and brought to the quad latch IC9 via the instrument bus. The f.m. drive signal is on PLCJ from where it is fed to IC10 voltage follower which in turn drives a network of switched resistors. These are operated by relays RLA, RLB and RLC. With all the relays energized, maximum f.m. drive signal is applied to the r.f. oscillators AB3, and each relay de-energized decreases the drive by a factor of four.

AB3 - RF oscillators board

Circuit diagram : Chap. 7, Fig. 11

61. Board AB3 contains the main oscillators for the instrument. Four oscillators each one covering a quarter octave frequency range between 260 MHz and 520 MHz. Only one oscillator is ever turned on at any time and its output frequency is phase locked to the required output frequency by the phase detector AB4. Each oscillator can be frequency modulated by a signal from AB2. The board is contained in a solid aluminium box to reduce microphony to a minimum.

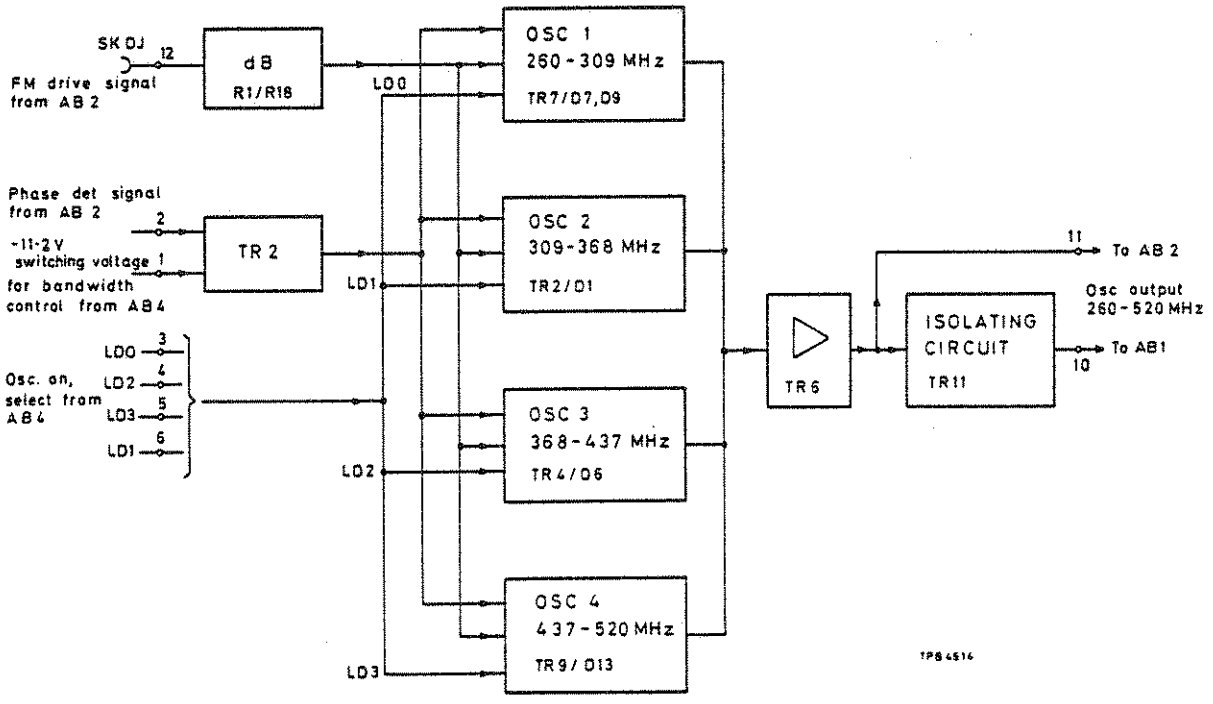


Fig. 7 RF oscillators board (AB3)

62. Each oscillator uses a resonant circuit with a maintaining transistor capacitively coupled to maintain oscillation. The tuning inductor is a printed track which can be adjusted using a sliding link. Varactor diodes are used to voltage tune the oscillator. Chip capacitors are used to tap the transistors TR2, 4, 7, 9, into the tuned circuit. This avoids spurious resonances. Care must be taken when attempting to solder chip components, for details see Chap. 5, Maintenance, Introduction. Each oscillator is designed to have a substantially linear f.m. tracking curve which is instrumental in reducing f.m. distortion and noise.

63. The required oscillator is turned on by connecting tag 3, 4, 5 or 6 to a negative voltage on AB4. This supplies emitter current to the required maintaining transistor. The collector current of the transistor forward biases diodes connected to its collector and therefore connects the r.f. signal to the amplifier TR6. Two outputs from TR6 are taken, one direct via tag 11 to AB2 board for frequency division, the second is via isolating transistor TR11 and tag 10 to the output v.r.d., AB1, to phase lock the carrier frequency. The nominal output from both tag 10 and tag 11 is -6 dBm.

64. The oscillators are frequency modulated by a signal appearing on tag 12. This signal is attenuated by R18 and R1 and is then applied to the anode of each varactor diode via r.f. chokes L2, L5, L7 and L11. The main frequency control is achieved by the phase detector signal on tag 2. It is connected to the cathode of each varactor via an R-C network consisting of R2, R3, TR1 and C8. When the f.m. is on the phase locked loop bandwidth is low and TR1 is switched off by connecting tag 1 to -11.2 V on AB4. R2 and C8 then have a long time constant and filter signals appearing on tag 2.

65. When the f.m. is off the loop bandwidth is increased in order to reduce the frequency settling time. The j.f.e.t. TR1 is then turned on so that the R-C time constant is formed by R3 and C8. This prevents potential feedback instability.

AB4 - Output phase detector

Circuit diagram : Chap. 7, Fig. 12

66. Board AB4 contains the phase comparator used to lock the output frequency from AB3 output oscillators to the selected frequency. It also contains voltage regulators to provide low noise power supplies for AB3 and transistor switches TR1 - TR4 with IC8, to switch the required AB3 oscillator on.

67. The output from AB5 v.c.x.o. loop inputs on PLCC, pin 2. Its frequency is approximately 100 kHz. The frequency is then divided by two in part of IC1. The resulting 50 kHz square wave is then routed to the phase comparator IC5 by one of two routes. If the f.m. is off the phase locked loop bandwidth is high and the 50 kHz signal is routed via IC4 to IC5.

68. If the f.m. is on, the loop bandwidth should be lower in order to avoid the loop interfering with the required f.m. This is reduced by several methods. The phase detector current is reduced by a factor of 50 and the loop filter time constants are altered by switching in resistors R41, R42. In addition the phase detector operating frequency is changed from 50 kHz to 10 kHz. When the f.m. is on, the divide-by-five circuit in IC3a is enabled by IC1, pin 5 and its output is routed via IC4 to the phase comparator IC5.

69. Similarly the nominal 50 kHz signal from AB1 - Output v.r.d. is routed to the phase comparator, IC5 via IC4 also, and if the f.m. is on its frequency is divided by five in IC3b before reaching IC5 via IC4.

70. In order to minimize any transient frequency change when switching the f.m. on or off the f.m. on/off instruction on PLBY, pin 5 is latched by IC1 so that the divide-by-five circuits of IC3 are synchronously enabled.

71. Phase comparator. IC5 compares the phase of the signals on pins 3 and 11. If the frequency on pin 3 is higher than that on pin 11, IC5 will produce a string of pulses on pin 6. If the frequency on pin 3 is lower than that on pin 11, IC5 will produce a string of pulses on pin 8. When the signals are phase locked by the loop IC5, pins 6 and 8 are normally low except for a 30 ns pulse.

72. Phase detectors, there are two, TR12 to TR17 and TR18 to TR23, these differ only in that the first phase detector operates at 3 mA and the second at 0.06 mA. If the f.m. is off both the phase detectors operate. If the f.m. is on the 3 mA detector (TR12 - TR17) is turned off by IC6 and so the gain of the phase locked loop is reduced. Because both phase detectors operate in a similar manner only one is described.

73. The signal on IC6, pin 11 is level shifted by TR12 and used to control a differential pair formed by TR14 and TR15. The signal on TP1 switches either TR15 or TR14 on. When TR15 is switched on its base voltage is established by the Zener diode D1 and current flows from R21 into TR15. This current charges up the loop filter formed by C14, R42, R41, TR24 and C13. Similarly TR13 level shifts the waveform on IC6, pin 6, in order to control the differential pair TR16, TR17. When TR17 is on charge is drawn out of the loop filter.

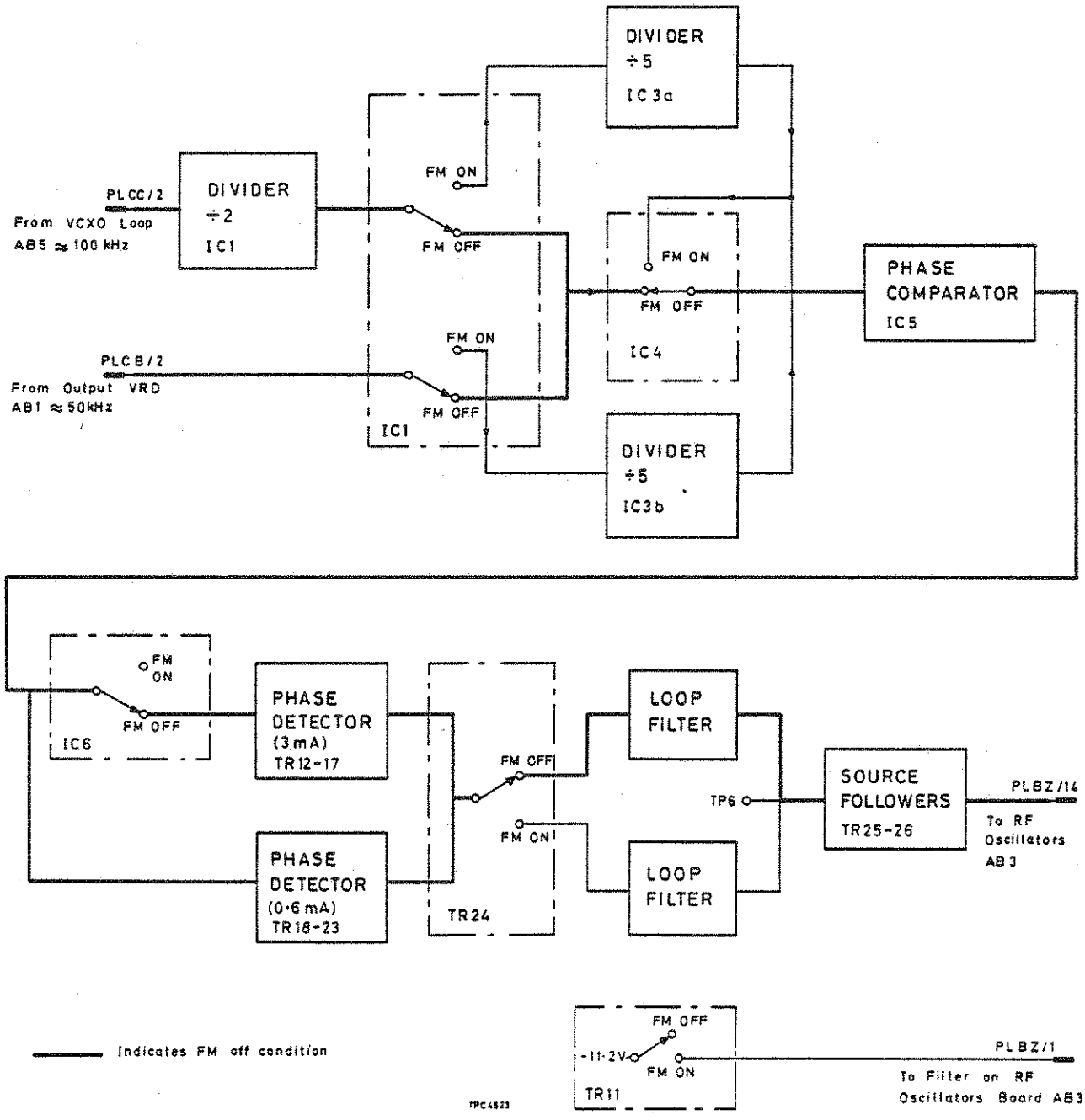


Fig. 8 Output phase detector (AB4)

74. If the loop looses lock either TR15 or TR17 (assuming f.m. is off) is switched on by the pulses from IC5 and either increases or decreases the charge on the loop filter and hence changes the voltage on TP6 in the direction required to regain phase lock. At phase lock TR15 and TR17 are off except for a nominal 30 ns time interval when both transistors are on. If the f.m. is on TR15 and TR14 are held off and TR21 and TR23 control the loop filter.

75. Loop filter time constants, these are switched by TR24 according to whether the f.m. is on or off. When the f.m. is on TR24 is switched on by TR9. This makes the time constants of C14, C13 short to ensure stability in the loop. If the f.m. is off the loop bandwidth is reduced and the time constants of C13, C14 are increased by turning TR24 off. The loop filter is earthed on the box containing AB3 via PLBZ pin 5. This reduces mains hum and phase detector related interference.

76. The phase detector output on TP6 is buffered by the source follower TR25, transistor TR26 is a second source follower that ensures the source-drain voltage of TR25 is low in order to minimize gate leakage current (j.f.e.t's suffer leakage due to impact ionization if their drain-source voltage is high). The output from TR25 source is then fed to AB3 via PLBZ pin 14 to control AB3 oscillators.

77. The signal on PLBZ, pin 1 controls a filter time constant on AB3 board. When the f.m. is on PLBZ, pin 1 is connected to -11.2 V via TR11. If the f.m. is off, TR11 is switched off and PLBZ, pin 1 is pulled to the same voltage as PLBZ, pin 14 by R49. Note that PLBZ, pin 1 is a high impedance point and can only be monitored by a high impedance probe.

78. IC2 and IC7 are voltage regulators that produce -11.2 V and +11.5 V supplies for use on AB3 and AB4. This ensures that the supplies to oscillators are free from hum and noise.

79. The required oscillator on AB3 is switched on by the circuits formed by TR1 to TR4 and IC8 as determined by the lines LD0 to LD3 derived from AA2 microprocessor board.

AB5 - Voltage controlled crystal oscillator (VCXO) loop

Circuit diagram : Chap. 7, Fig. 13

80. The board AB5 phase locks a v.c.x.o. to a frequency equal to the 10 MHz frequency standard plus the output frequency from AA1, LSD loop. The output from AB5 is used as the reference by AB4 output phase detector.

81. TR1 is the maintaining transistor for a v.c.x.o. using tuning elements L1,L2,D2,XL1,C3 and C4. The Zener diode D1 provides a regulated +12 V supply to the oscillator. The varactor diode, D2, enables the oscillator to be voltage tuned over the frequency range 10.002 MHz to 10.008 MHz.

82. The output signal from TR1 collector is connected to IC1 where the signal is converted to t.t.l. levels. The output from IC1 pin 13 is used to drive IC3 which divides the frequency by 100. The output from IC3, pin 9 is then fed to AB4 via PLCF, pin 2.

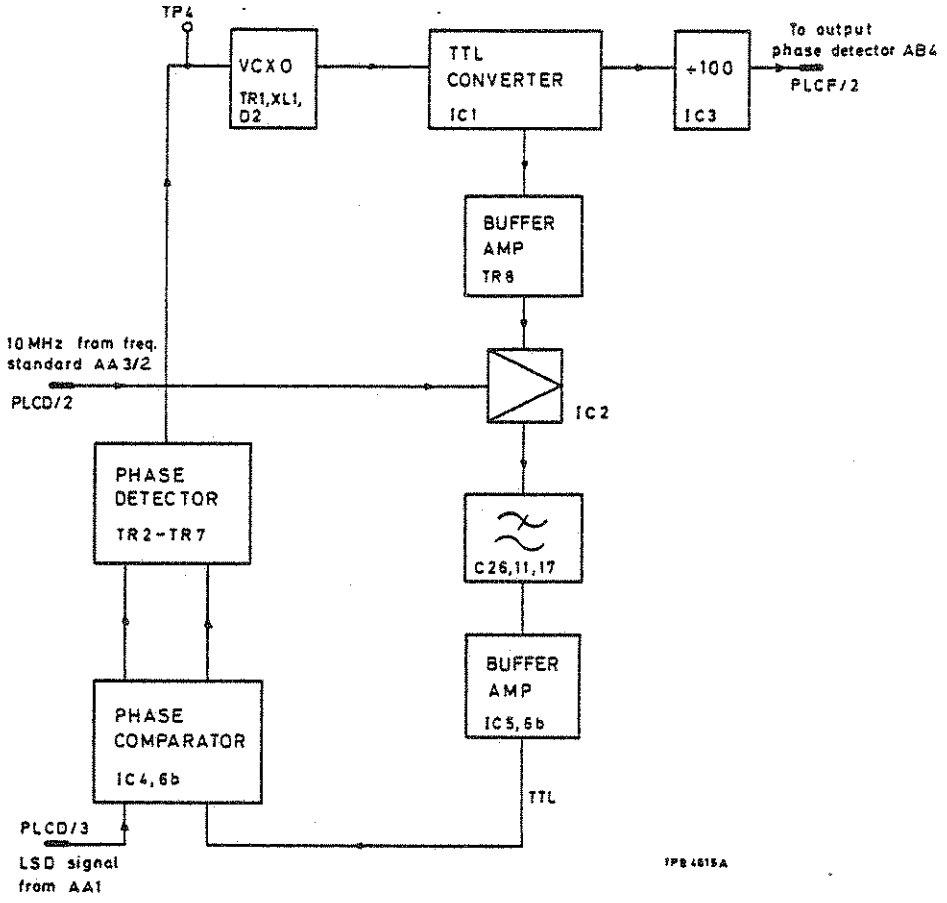


Fig. 9 VCXO loop (AB5)

83. The output from IC1, pin 10 is used to drive the phase locked loop to lock the v.c.x.o. to the selected frequency. The output is level shifted and buffered by TR8 and the signal on the collector of TR8 is used to drive a double balanced mixer, IC2. Pin 10 of IC2 is a.c. coupled to ground by C9 so the v.c.x.o. frequency appears across pins 8 and 10, this serves as the local oscillator for the mixer. The linear input for IC2 mixer is developed across pins 1 and 4 and is a 10 MHz sinusoidal signal derived from AA3/2 frequency standard via PLCD, pin 2.

84. IC2 mixes the 10 MHz signal with the v.c.x.o. frequency to produce an audio difference frequency on IC2, pin 6. IC2, pin 12 is also connected to pin 6 via C26, this is an anti-phase component and provides cancellation of the sum product and possible local oscillator breakthrough (at high frequencies) further filtering is provided by C11.

85. The resulting signal is then a.c. coupled by C17 in order to produce a signal referenced to ground at IC5, pin 3. R20, R21, C20, C25 provide further filtering of the audio signal. The comparator IC5 converts the audio signal into a nominal t.t.l. compatible square wave at IC5, pin 7. This signal is fed to phase comparator IC4 via IC6a.

86. The phase comparator is formed by IC4 and IC6b comparing the phase of the signals on pins 3 and 11. The signal on pin 3 is the output frequency from AA1, LSD loop. If the frequency at pin 11 is higher than that at pin 3 a series of pulses will appear at pin 8. If the frequency at pin 11 is lower than at pin 3 a series of pulses will appear at pin 5.

87. The outputs from IC4 drive a phase detector and loop filter to control the v.c.x.o. TR6 and TR7 are level shifting transistors that drive two differential pairs TR3, TR2 and TR4, TR5. The differential pairs inject current pulses into the loop filter formed by C1, R35, C2. If the v.c.x.o. frequency is low TR5 is turned on by the pulses from IC4, pin 5 and the voltage on TP4 will be increased to regain phase lock. Similarly if the v.c.x.o. frequency is high TR2 will be turned on by the pulses on pin 8 and the voltage on TP4 will be decreased to attain phase lock. At phase lock both TR2 and TR5 are normally off except for a short interval of about 30 ns when both transistors are switched on by narrow pulses from IC4.

88. IC7 is a voltage follower that buffers the voltage on TP4. The resulting d.c. signal is used to control the varactor diode D2 and hence the frequency of the v.c.x.o.

AC2 - Beat frequency oscillator (BFO) system

Circuit diagram : Chap. 7, Fig. 15

89. Carrier frequencies below 2.03126 MHz are generated in a b.f.o. on this board by mixing a signal of 10 - 12.03125 MHz with the 10 MHz standard. The resulting signal is filtered leaving only the difference frequency, which is then fed to the output amplifier AC4.

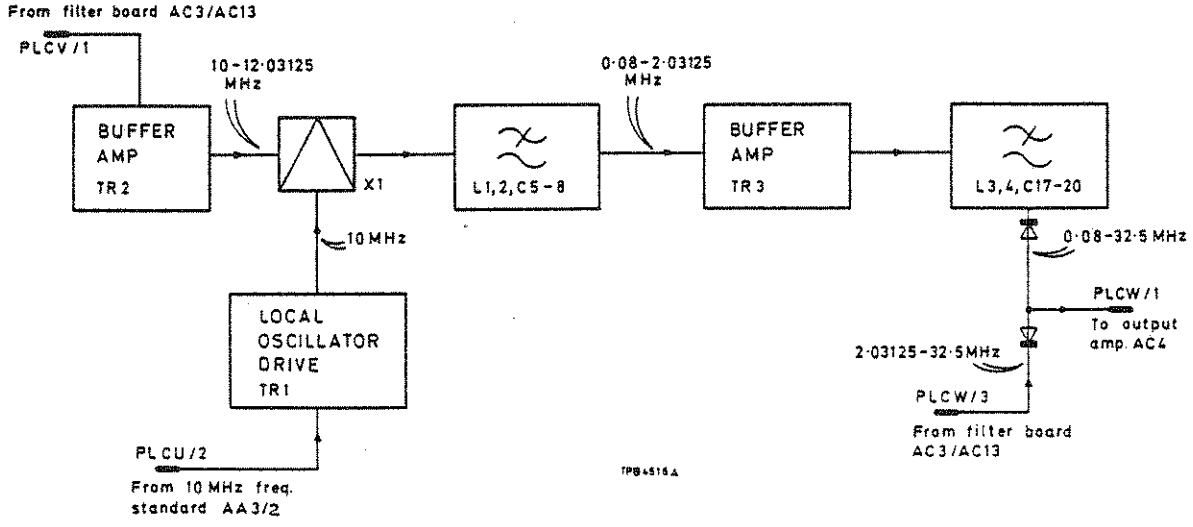


Fig. 10 BFO system (AC2)

90. The 10 - 12.03125 MHz signal input at PLCV, pin 1 is buffered by TR2 and applied to the linear port, pin 1 of mixer X1. The 10 MHz signal, from the frequency standard, at PLCU, pin 2 is amplified by TR1 and applied to the local oscillator port, pin 8 of the mixer. The process of mixing produces sum and difference signals at the i.f. port, pins 3, 4. A low-pass filter (2.1 MHz) L1, L2, C5 - C8 suppresses the sum component so that TR3 is fed with a signal of 80 kHz - 203125 MHz. T1 transformer prevents breakthrough of mixer input frequencies (particularly 10 MHz) on the b.f.o. output, and allows the earth plane to be split; this helps to contain the r.f. earth currents. After T1 the signal passes through a second 2.1 MHz low-pass filter, L3, L4, C17 - C20, to join a common l.f. channel output to AC4 via D1, C21 and PLCW, pin 1.

91. For b.f.o. operation the d.c. voltage on PLCW, pin 3 is high (controlled from AC3/AC13) so that D2 is off and D1 is on. D2, together with other diodes on AC3/AC13, prevent 10 - 12.03125 MHz signal breakthrough on the output from AC2. If b.f.o. operation is not required (carrier frequency >2.03125 MHz) PLCW, pin 3 is low, consequently D2 is on and D1 is off. This allows the l.f. channel input at PLCW, pin 3 to be routed direct to AC4 via PLCW, pin 1. At the same time the 10 MHz and 10 - 12.03125 MHz signals are turned off.

AC3/AC13 - Filter and frequency doubler board

Circuit diagrams : Chap. 7, Figs. 16 and 19

92. The same printed circuit board is used for AC3 and AC13. AC13 is used in 2019A and has both filter and frequency doubler circuits; AC3 is used in 2018A having only the filter circuits (the components for the frequency doubler not fitted). A dashed line in the board legend marks the boundary between the two circuit areas.

93. The filter circuits provide harmonic filtering of the r.f. signal from AC5 by means of switched low-pass filters. The frequency doubler circuit doubles the input frequencies 260 - 520 MHz supplied to it to provide frequency cover for the 2019A up to 1040 MHz. The output signals from AC3/AC13 are fed to the output amplifier, AC4. (Frequencies below 32.5 MHz are fed via AC2).

94. AC3/AC13 also performs the bus address decoding for r.f. box 2 ('C' Deck), and the decoded address lines (A7L0 - A7L6 from IC1) are routed to their respective latches on AC5, AC4, AC3/AC13. The power supplies for AC5, AC4 and AC2 are distributed from AC3/AC13. The control data for AC3/AC13 is brought to IC2, IC3 and IC6 via the instrument bus.

95. Filters. The r.f. signal at PLDF is switched into the h.f. channel (32.5 - 520 MHz) by D1 if the $\overline{\text{HF}}$/LF line, IC3, pin 2 is low, or into the l.f. channel (2.03126 - 32.5 MHz) by D2 if the line is high. The h.f. channel input is amplified by TR1 and TR2 (+10 dB gain) and then filtered by the 520 MHz low-pass filter L6, L7, C20-C22. If the FREQUENCY DOUBLER $\overline{\text{IN}}$/OUT line, IC3, pin 12, is high, D6 is turned on and the r.f. signal passes to the main h.f. filter bank.

96. If the carrier frequency is between 32.5 and 260 MHz one of the half-octave low-pass filters in the main h.f. filter bank (L13 - L24) will be selected according to the data latched on IC2, pins 12, 15, 16, 19 and IC3, pin 5. If the frequency is between 260 and 520 MHz the bypass, D16, D17 is selected. The main h.f. filter bank output passes through C50.

97. For frequencies between 260 and 368 MHz the 368 MHz low-pass filter is switched in by turning on D25,D27 by the 368 and 23 MHz l.p.f's IN-$\overline{\text{OUT}}$ 'high' instruction on IC3, pin 6. For all other frequencies this line is 'low' and signals pass through D24,D28. If the frequency doubler is not included D30 is turned on by the FREQUENCY DOUBLER $\overline{\text{IN}}$/OUT 'high' instruction, this is inverted by IC5e and the output is then taken from SKCS.

98. The h.f. channel operates in a 50 Ω system, but the l.f. channel operates in a 200 Ω system. The necessary impedance transfer in the l.f. channel is accomplished by the buffer TR3. LF channel signals from TR3 are first filtered by the 32.5 MHz low-pass filter L63, L64, C96 - C98 and then pass to the main l.f. filter bank. This operates in a similar manner to the h.f. filter bank but uses the data on IC2 pins 2,5,6,9 and IC3, pin 5. The 23 MHz low-pass filter is switched by IC3, pin 6, and the common output routed through C95.

99. For carrier frequencies of 2.03126 MHz - 32.5 MHz the b.f.o. line, IC3 pin 9, is high, turning D52 on and D51 and D53 off, connecting the output from C95 through to PLCT, pin 2.

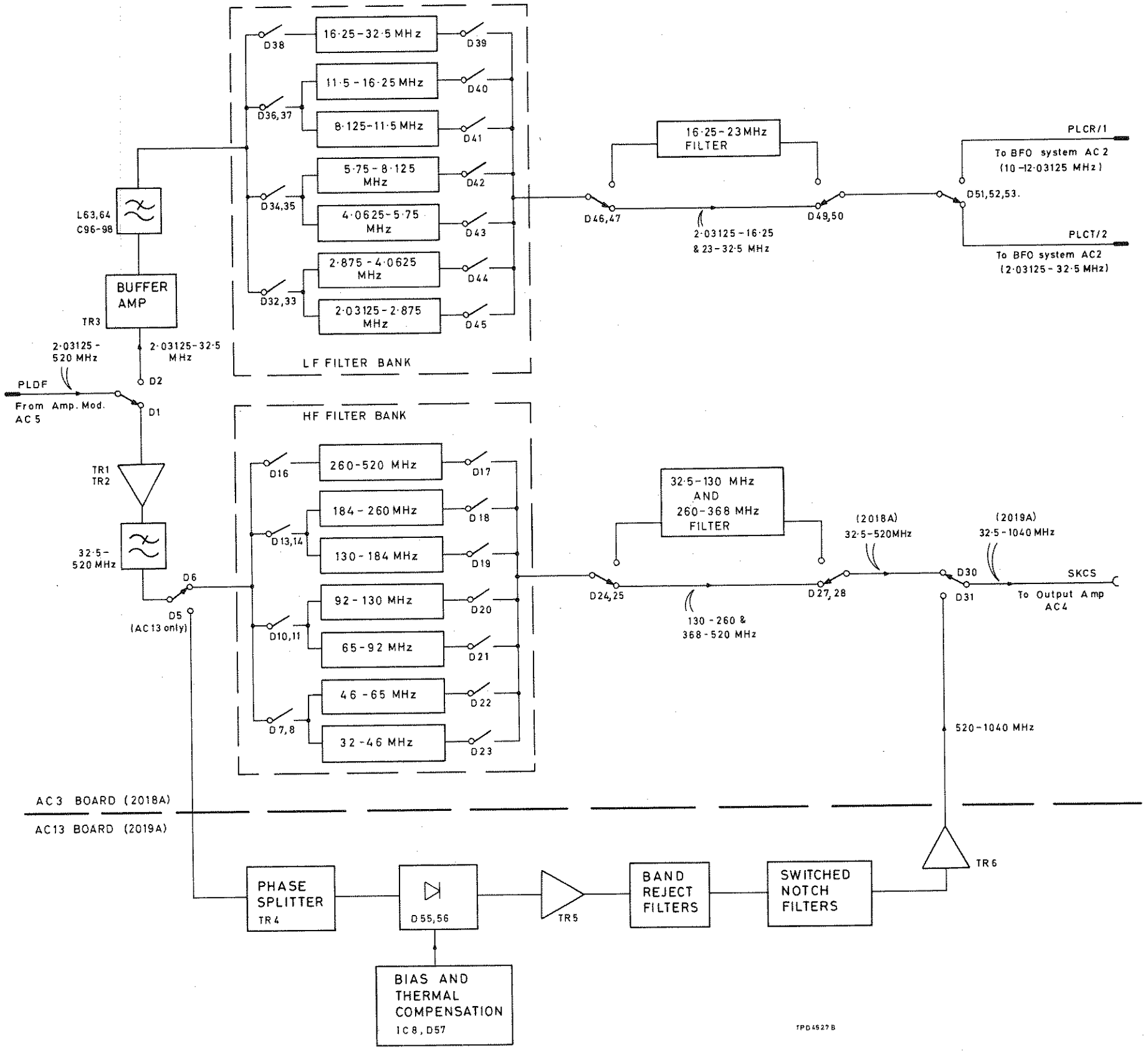


Fig. 11 Filter and frequency doubler board (AC3/AC13)

100. For carrier frequencies below 2.03126 MHz the b.f.o. line is low turning D51 and D53 on and D52 off. The b.f.o. board, AC2, is supplied with a 10 - 12.03125 MHz signal via PLCR, pin 1 which is mixed on AC2 with the 10 MHz standard to give the required carrier frequency. D53 helps to prevent breakthrough of l.f. channel frequencies on the b.f.o. output.

101. Frequency doubler (520.00002 MHz - 1040 MHz). The input to phase splitter and frequency doubler is taken from after the 520 MHz low-pass filter. A transistor phase splitter, TR4, feeds the matched pair of diodes D55 and D56 in full wave rectification configuration. A bias supply is derived from a third diode (D57), matched with the other two. This ensures thermal compensation and a sensibly linear output over a wide range of level. Thus a.m. will be virtually unaffected by the doubler. The output from the frequency doubler is then amplified by TR5.

102. The output from the frequency doubler contains both sub-harmonics and harmonics which must be improved by filtering. The filter must reject the sub-harmonic and harmonics while allowing the required frequency to pass with low insertion loss. This is affected by a series of band reject filters. Switching between capacitive elements is carried out with diodes and at two break frequencies, 660 MHz and 820 MHz, in order to give the frequency responses required. Capacitors C119, C120, C123, C124, C135, C136 form switched notch filters that attenuate the sub-harmonic components in the output. The output from the frequency doubler is then amplified by TR6 before being routed to the output connector, SKCS, via the diode switch D31.

AC4 - Output amplifier

Circuit diagram : Chap. 7, Fig. 17

103. This board contains the r.f. output amplifiers, the automatic level control (a.l.c.) circuits, the electronic fine attenuator, and the insertion loss control (i.l.c.). It receives h.f. channel signals from AC3/AC13, l.f. channel and b.f.o. signals from AC2, and delivers a levelled and calibrated output signal with a 50 Ω source impedance to the coarse attenuator ATO/1. Control data for the amplifier switching, fine attenuator and i.l.c. is brought to AC4 via the instrument bus.

104. HF channel and a.l.c. This is selected by a 'high' instruction on IC2, pin 5, and a 'low' on IC2, pin 9. TR5 is then turned on and supplies current to the h.f. channel amplifiers, whilst TR16 is off. The h.f. input (frequencies greater than 32.5 MHz) at PLCS is amplified by four r.f. transistor stages. The first two, TR2, TR4, give +6 dB each but the gain can be trimmed at the 1 GHz end by moving R9, R19 along L2, L4 respectively. The last two stages (common with the l.f. channel) have a combined gain of +10 dB. At high frequencies the gain of TR10 tends to fall; to compensate for this the gain of TR8 is held down at low frequencies but allowed to rise with frequency.

105. High frequency gain can be trimmed by moving R34, R35 along L7. Diodes D8 - D10 protect TR10 from voltage transients. All four stages use active bias networks, TR1, 3, 7 and 9.

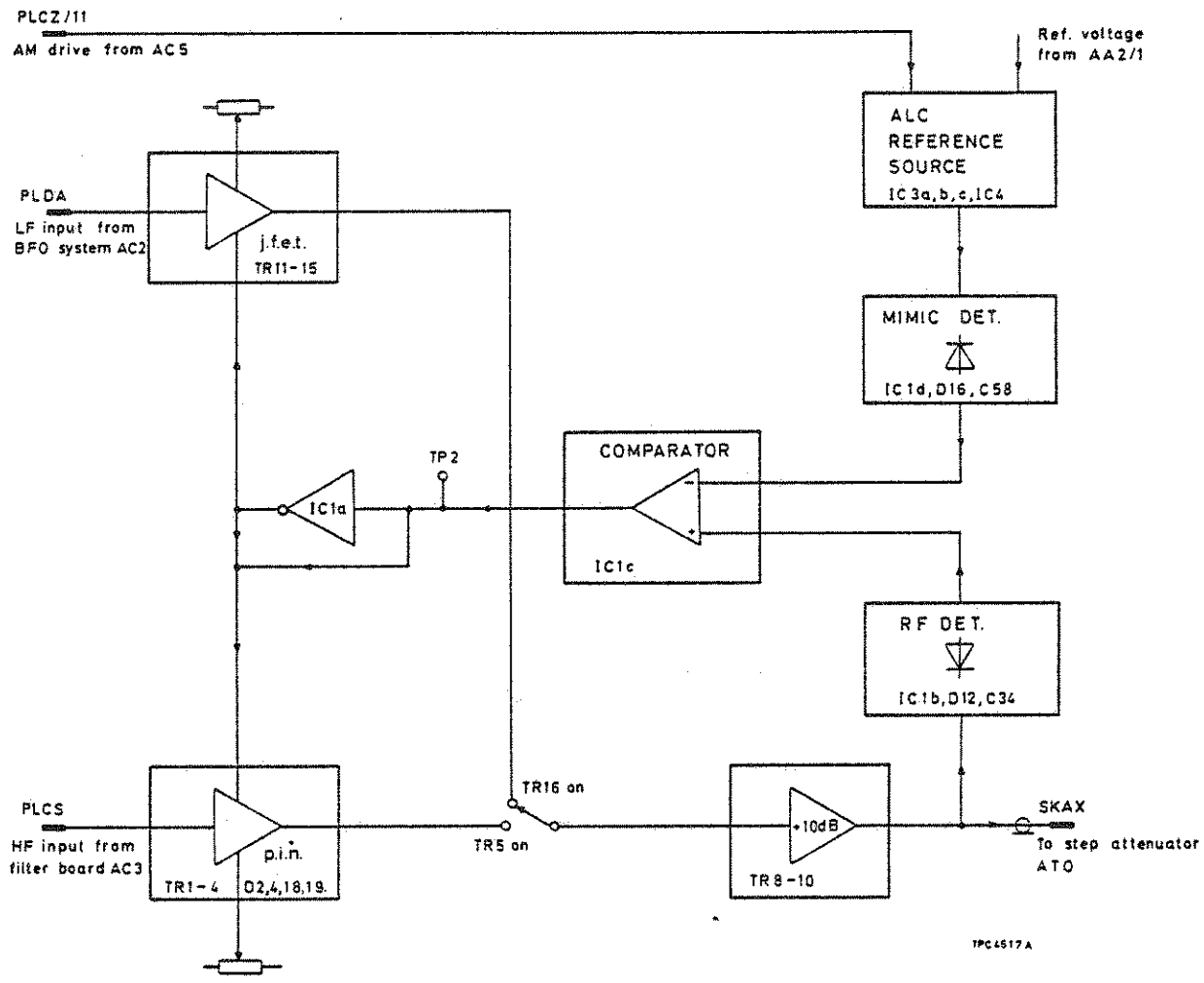


Fig. 12 Output amplifier (AC4)

106. RF level control for the h.f. channel is accomplished using pin diode attenuators in the r.f. amplifier chain. The two fixed-gain stages, TR2 and TR4 are placed between three pin diode attenuator elements, D18-D19, D2 and D4. The attenuation produced by these diodes is determined by the control voltage applied to them; the smaller the magnitude of the control voltage, the higher the attenuation. This control voltage is derived by comparing, at the voltage comparator IC1c, a d.c. reference voltage from IC1d with the r.f. detector voltage from IC1b. The voltage from IC1c (TP2) controls D2, and the inverted voltage from IC1a (TP1) controls D18, D19 and D4. If the r.f. detector voltage differs from the reference voltage, the pin diodes will be driven so as to annul this difference. TR16 is off, and providing D4 is forward biased D5 will also be turned off disconnecting the l.f. channel drive.

107. The r.f. detector measures the peak voltage at the output of the fixed gain transistor pair, TR8, TR10, immediately before the 50 Ω resistor, R47. Thus the voltage can be precisely controlled behind a 50 Ω source impedance. D12, C34 form the negative-peak detector whose voltage is buffered by IC1b. D13 provides temperature compensation for the detector diode. D11, C33 act as a mimic positive-peak detector to help equalize the loading on TR10.

108. LF channel and a.l.c. The l.f. channel is selected by a 'high' instruction on IC2, pin 9, and a 'low' on IC2, pin 5. TR16 is then turned on supplying current to the l.f. amplifiers, whilst TR5 is turned off. The l.f. channel input (frequencies less than 32.5 MHz) at PLDA is amplified by three transistor stages, TR11, 13, 15, operating in a 200 Ω system, and then by the common output transistor pair, TR8, TR10, operating in a 50 Ω system. The transfer from 200 to 50 Ω is accomplished with a consequential signal loss of 12 dB, this is however compensated for by the ample gain in the amplifier chain. When the l.f. channel is on, D5 is forward biased and D4 reverse biased allowing signals to be routed from TR15 to TR8.

109. LF channel levelling is implemented by making the first two amplifiers variable-gain stages. JFETs are used in the emitter circuits of TR11 and TR13 for this purpose. The drain-source resistance of the f.e.t's and hence the gain of each stage, is controlled by the control voltage on TP1; the more negative this voltage is, the lower the gain. The control voltage is derived in the same way as for the h.f. channel, except that because TR16 is on, the voltage on TP1 is offset by -7.5 V (due to R69).

110. ALC reference voltage. The d.c. reference voltage to the comparator IC1c is the means through which accurate control of the output r.f. signal level is obtained. The actual d.c. voltage required for any given frequency and output level is influenced by a number of different circumstances. Further complications are present when amplitude modulation (a.m.) is applied which are compensated for by the circuits described below.

Electronic fine attenuator

111. ATO/1 attenuator unit provides the coarse attenuation of the output signal from AC4 in multiple steps of 10 dB. An electronic attenuator on AC4 is used to give fine control of the output over a range of 10 dB, with a resolution of 1 mV (r.m.s., p.d.). This is achieved by supplying an accurate d.c. reference voltage to the a.l.c. comparator IC1c.

112. In the normal mode AC4 is required to give an output between 158 mV and 500 mV, rising to 1000 mV in the +6 dB mode. For a maximum figure of 1000 and a resolution of 1 a 10 bit binary number is needed i.e. 1000 decimal = 1111101000 binary. This requirement is implemented in IC6, IC3d where IC6 is the 10-bit digital-to-analogue (D/A) converter to which the binary number is sent. The D/A has its own internal data latches.

113. The least significant digits are sent first to address A7L2, followed by the 2 most significant digits to A7L3. The number in the D/A determines the gain of IC3d, and hence the output on pin 14 in relation to the input on IC6, pin 3. A change of 1 in the 10-bit number will give rise to a voltage change from IC3d which in turn causes a change in the reference voltage applied to the comparator. When calibrated this will change the output level from AC4 by 1 mV. In calibration the voltage on IC6, pin 3 is set to give a certain r.f. output; R89 is used to calibrate the fine attenuator across its working range. (The purpose of D16, IC1c etc. is explained under a.m. processing.)

Insertion loss control (i.l.c.)

114. After the point at which levelling occurs, (TR10 collector) the r.f. signal is subject to the insertion loss of coaxial cables, connectors, ATO coarse attenuator, etc. before the output socket. The insertion loss is frequency dependent, and becomes more pronounced the higher the frequency. To compensate for this AC4 output is increased by an amount equal to the insertion loss at the selected frequency. This is achieved by adding a small offset to the reference voltage applied to the a.l.c. comparator. Clearly the amount of offset needed will increase with frequency.

115. This is achieved by IC4 8-bit D/A converter, to which the microprocessor sends a number (address A7L1) representing the correction required. At low frequencies where insertion loss is low, the number sent to the D/A gives IC3b a gain close to -1, and the output on IC3c, pin 8 will have a certain value (depending on the setting of R86). As the frequency is increased the number sent to the D/A reduces the gain towards 0 and consequently the output from IC3c increases in magnitude. This increase in voltage at the input to the fine attenuator is amplified according to the r.f. output level required and fed to the a.l.c. comparator to bring about the insertion loss compensation.

116. The number sent out to IC4 is calculated by the microprocessor from data stored in its memory. A sufficiently accurate approximation to the real insertion loss is obtained using just three calibration frequencies 10, 520 and 1040 MHz. At 10 MHz a code number 050 is stored (using Second function 6) and R86 adjusted for the correct r.f. output level. The frequency is then set to 520 MHz and the stored code number increased until the level is again correct. Finally the process is repeated at 1040 MHz (2019A only). When a carrier frequency is selected the microprocessor calculates the required code number from a straight line graph drawn between neighbouring calibration points. The actual binary number sent to the D/A is 255.

AM processing

117. The r.f. detector D12, C34 measures the peak voltage of the r.f. signal. When a.m. is present the detector measures the peak of the a.m. envelope; at 100% depth this will be double the voltage at 0% depth. To ensure that the r.f. level is still correct the reference voltage applied to the comparator must be increased by an amount equal to the detector voltage increase due to the a.m. If this is not done there will be an r.f. level error introduced depending on the a.m. depth.

118. This is overcome by adding to the d.c. reference processing chain an a.m. drive signal derived from AC5 via PLCZ, pin 11 and including a mimic detector, D16, C58. The mimic detector measures the peak voltage of the a.m. drive signal superimposed on the d.c. reference which - when calibrated - will produce the correct r.f. output level.

119. In practise the r.f. detector has a finite time constant (R45/C34) and so that changes in r.f. level can take place quickly, the time constant must not be too long. Consequently at low modulation frequencies the detector output will decay between envelope peaks at a rate depending on this time constant. In order to preserve the a.m. the reference voltage applied to the comparator must match the r.f. detector voltage exactly. If this is not done the comparator will produce a control signal that will tend to remove the a.m. from the r.f. signal. To make the reference behave in the same way as the r.f. detector voltage the mimic detector is set to have the same time constant

as the r.f. detector by means of the det. trim control R95. Temperature compensation for the mimic detector is provided with D17 (similar to D13).

120. The loop bandwidth of the a.l.c. system is approximately 50 Hz (C47/R74) so at very low modulation frequencies the comparator has appreciable gain and the a.l.c. loop acts as an envelope feedback system. This means there will be a modulation frequency signal on the comparator output which will further modulate the carrier unless the two inputs to the comparator are accurately matched. This is done by applying a calibrated a.m. input of low modulation frequency and adjusting R77, set low mod. freq. until the output from AC4 is correct.

121. For the a.m. to be correct at low modulation frequencies the audio drive level on the reference to the comparator must be exactly equal to the audio level from the r.f. detector. Setting this condition also eliminates the r.f. level error occurring at higher modulation frequencies caused by the uncalibrated peak level of the a.m. drive signal on the reference signal.

AC5 - Amplitude modulator

Circuit diagram : Chap. 7, Fig. 18

122. AC5 board provides amplitude modulation of the output signal from AB2, divide-by-two chain (frequency range 2.03125-520 MHz). The modulated signal is then routed to the Filter board, AC3/AC13. AM depth from 0 to 99% is programmable in 1% steps, using seven bits of control data which are brought to the internal latch in the D/A converter, IC4, via the instrument bus. An eighth bit of data is used to activate the "+6 dB mode", in which the r.f. output level from AC5 is doubled. Under this condition no a.m. is allowed, and the microprocessor instructs 0% a.m. depth.

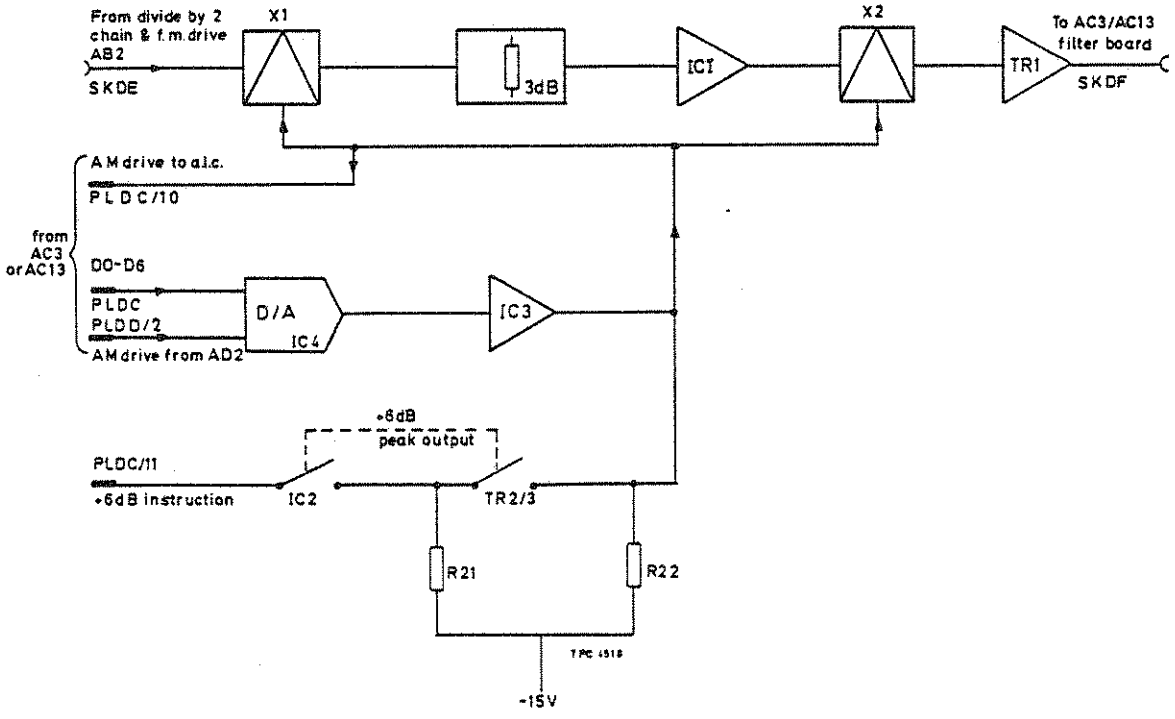


Fig. 13 Amplitude modulator (AC5)

123. The modulator consists of two double-balanced mixers, X1 and X2, in cascade, with a 3 dB pad (R2-R4) and a recovery amplifier, IC1, between them. X2 is responsible for the main part of the modulation, with X1 providing a lower level of pre-modulation at large envelope depths. The pre-modulator can be adjusted by varying the a.m. drive signal to X1 using preset R23. The output from X2 is amplified by TR1 and fed to SKDF.

124. The audio input is fed to the linear port of the D/A converter, IC4, from PLDD, and is amplified by IC3 whose gain depends on the control data latched into the D/A. The resulting a.m. signal is fed to X1 and X2, and also to the a.l.c. system on AC4 output amplifier via PLDC, pin 10. If the +6 dB mode line is high, TR3 is turned on thus doubling the bias current in X2. This causes an increase in the r.f. output at SKDF of 6 dB.

AD11 - Display board

Circuit diagram : Chap. 7, Figs. 20 and 21

125. The display board incorporates the three liquid crystal displays (l.c.d.) that are used to show the current settings of the instrument. The displays are driven using c.m.o.s. logic ICs to apply square waves to the segments of the display. Each l.c.d. has a backplane (b.p.) which is connected to the backplane drive (b.p.d.). The b.p.d. is a 50 Hz square wave.

126. The segments are driven by a similar square wave that is either in phase or out of phase with the b.p.d. If the segment drive is in phase with the b.p.d. there is no voltage applied between the segment and the backplane and the segment remains clear. If the segment drive is out of phase with the b.p.d. then a square wave voltage is applied between the segment and the b.p.d. and the segment darkens. It should be noted that d.c. voltages should not be applied to the l.c.d's since this can result in permanent damage to the display. A nominal -5 V supply for the board is generated using the Zener diode D1.

127. The backplane drive is generated by the astable multivibrator IC19. The output from IC19, pin 10 is a 50 Hz square wave switching between 0 V and +5 V. Before being applied to the displays the level of the square wave is translated to be between +5 V and -5 V at the outputs on IC18, pin 3 and IC26, pin 3.

128. Information to control the displays enters the board via PLAL. The D0 to D7 lines and the A0 to A3 logic levels are made c.m.o.s. compatible by IC1 and IC2 open collector buffers and the pull up resistors in R1. IC13, 15 and 16 decode the address lines to provide control lines to instruct the latches on the board. When the A5 line is held low the output from IC15, IC16 corresponding to the address set on A0 - A3 lines goes high (+5 V). These output lines, labelled A5L0 to A5L12, control which latch latches the data on the D0 to D7 lines.

129. With the exception of the decimal point driving system the data lines and the latch control lines are connected to the respective 4056 and 4054 l.c.d. drivers. The 4056 drivers are used to drive the seven segment displays. Each IC latches four input data lines, either D0 to D3 or D4 to D7, and decode the data to drive the seven segment display. The 4056 also level shifts the decoded information and converts it into a square wave between +5 V and -5 V suitable for driving the display. If a binary 15 instruction is latched in the display will remain blank.

130. The 4054 display drivers also latch the data line inputs when instructed but these drivers simply convert the input information into a square wave between +5 V and -5 V without decoding the data. This type of drive circuit is used to drive the annunciators on the display where one input line is required to control one annunciator.

131. In order to reduce the number of addresses and drivers required the decimal points are driven by a different system. Use is made of the fact that only one decimal point on each display is required to be set at one time. The frequency display decimal point is derived by IC14, 17 and 18. IC17 is a 1 out of 8 decoder which decodes the data lines D0 to D2 and its outputs are latched by IC14, 18. Since only one of the output lines of IC17 can be high one of the decimal points can be set. If the number decoded by IC17 is a binary 7 (i.e. D0 = 1, D1 = 1, D2 = 1) then no decimal point is set since pin 4 of IC17 is not connected. The decimal points for the modulation and r.f. level displays work in a similar manner on D3, D4 and D5, D6 lines respectively.

AD2 - Motherboard

Circuit diagram : Chap. 7, Fig. 22

132. The primary purpose of AD2 motherboard is to serve as a means of interconnecting the various areas of the instrument that require access to the microprocessor via the internal instrument bus. The interconnections are generally made by means of plugs on the motherboard that connect to ribbon cable and socket assemblies. The plugs on the board consist of arrays of machine inserted square wire wrap posts arranged in a dual in-line configuration. The p.c.b. AD3 is connected to the motherboard by an edge connector socket SKAH mounted on the motherboard.

133. The motherboard also latches the control data for the attenuator. IC1 is an octal latch on address A6L10 that latches the data used to control the attenuator pads and the r.p.p. reset. The outputs from IC1 are connected to the open collector driver, IC2, to directly drive the solenoids that operate the attenuator pads.

134. In order to simplify the interconnections in the lower r.f. box its data valid line, A7, is gated with the A3 line by IC3, thus saving a further line through the filter box. The resulting A3 + A7 output line goes 'low' only when both are held low, i.e., when information is being sent to addresses between A 7L0 and A7L7.

AD3/1 AF oscillator and f.m. control

135. AD3/1 controls the modulation system and contains the internal AF oscillator for the instrument. The signal paths are controlled by CMOS analogue gates operating between a +5 V supply and a -7.5 V supply developed across the Zener diode D8. The AF oscillator is a j.f.e.t. stabilized Wien bridge oscillator. IC7a/4 is the maintaining amplifier, TR2 is the stabilizing element and C6, C1 the tuning capacitors.

136. The frequency of oscillation is determined by the analogue gates in IC1,2,3,4 which select the frequency determining resistors R6 to R17. D6,C8 detect the output level from the AF oscillator and this is compared with a reference voltage on D5 cathode by IC7b/4. The output from IC7b/4 controls the effective resistance of TR2 which in turn controls the level of oscillation.

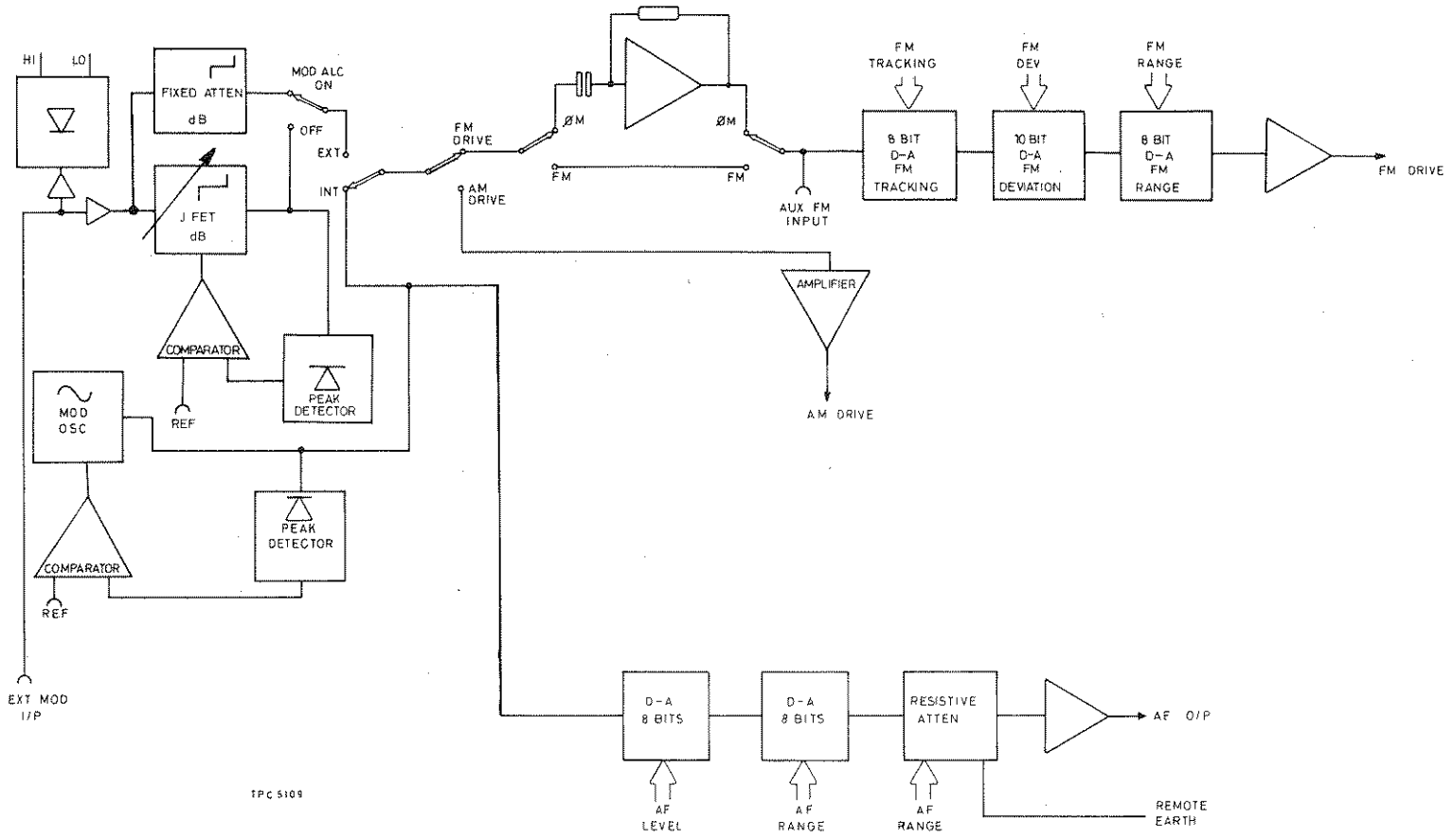


Fig. 14 AF oscillator and f.m. control (AD3/1)

137. The AF level output is obtained by first amplifying the AF oscillator output using IC7d/4 and then using two D-A converters, IC15 and IC18, to manipulate the signal level. IC15 provides fine control of the level and IC18 sets the AF level range. Additional range control is obtained using R78 to R81 as an attenuator network and IC22 as a selector switch. The final amplifier, IC24, and the resistors R78 to R81, are earthed at the front panel to minimize earth loop currents.

138. External modulation is applied on PLDX pin 3. The input is buffered and detected by IC6a/4, IC8 and IC9. If the input signal level is low (<0.95 V r.m.s.) the monostables in IC10 are not triggered. IC10 pin 13 is low so the "LO" l.e.d. on the front panel is on. If the input signal level is high (>1.05 V r.m.s.) both outputs from IC8 will generate pulses which constantly trigger the monostables in IC10. Since IC10 pin 12 is low (pin 13 high) the "HI" l.e.d. on the front panel is displayed. At intermediate levels IC10 pin 1 is constantly retriggered but not pin 9 and so both l.e.d's are off.

139. IC6b/4 buffers the external modulation input. The audio voltage level at the junction of R34 and R35 is levelled on ALC system using TR1 as a variable resistor, D3 and C21 as a detector and IC6 as a comparator. R37 is used to set the level with the ALC on. R32 calibrates the input with 1 V r.m.s. applied and the levelling off. IC11a selects whether the levelled or the unlevelled signal is used according to the status of the MOD ALC key. IC12a/3 selects whether the internal or external modulation source is used. IC11b/3 and IC3c/3 improve the isolation of the INT/EXT switch.

140. If a.m. is selected IC12b/3 passes the signal on to IC31a/2 which amplifies the signal and routes the signal via AD2 Motherboard to the Amplitude Modulator AC5. If f.m. is selected IC12c/3 passes the signal on to IC3b/2. If ϕm is selected the signal is routed through the differentiator circuit IC4b/2 to IC3b/2. R70 is used to calibrate the ϕ.m. deviation without influencing the f.m. calibration.

141. An auxiliary f.m. signal is added into the signal at the output of IC3b/2 from the AUX FM INPUT on the front panel. R75 is used to set the output of IC3b/2 to 12 V p-p on internal modulation. A series of 3 CMOS D-A converters are used to control the FM signal level. IC20 modifies the signal level in accordance with the FM tracking data. IC26 modifies the signal level in accordance with the FM deviation set and IC28 divides the signal level by factors of 2 to provide range scaling.

142. The data required by IC26 is a 10-bit binary number and is loaded into the D-A in two bytes. The first byte is the 8 least significant bits while the second byte consists of the 2 most significant bits. The D/A setting only changes when the most significant bits are loaded in.

AD4/1 - Keyboard

Circuit diagram : Chap. 7, Fig. 24

143. Keyboard AD4/1 carries all the front panel key switches, the l.e.d. indicators for the modulation oscillator frequency and the control logic required to interface the switches and the l.e.d's to the internal data bus.

144. The key switches are arranged as an array organized in rows and columns. The latch IC5 is initially set to give logic 'low' on its D0-D4 outputs and 'high' on D5. The pull up resistors in R7 set the logic levels at the inputs to IC6 to a logic 'high'. When the microprocessor is monitoring the keyboard IC6 buffer is enabled to drive the internal data bus and so the microprocessor is able to monitor the state of the keyboard. For convenience the inputs to IC6 are referred to as columns and the outputs from IC4 are referred to as rows.

145. When a key is pressed it shorts that column to one of the rows. In order to find which key in a column has been pressed the microprocessor sets all but the top row (connected to IC5 pin 2) of mechanical switches to the high state. If the key pressed was in the top row then the column will remain in the 'low' state. If not, the column returns to the 'high' state and the microprocessor sets a 'low' to the next row down (IC5 pin 5) with all other rows set 'high'. This is repeated until the correct row is located. Having determined which row and which column the key was in this uniquely identifies the key pressed.

146. IC7 forms an electronic switch extension to the keyboard. In normal keyboard operation IC5 pin 15 (D5) is set 'high'. If the RPP is tripped IC7 pin 3 pulls the first column low in the same way as a switch would. The keyboard is scanned in the normal way with D5 low, thus disconnecting the electronic switch. After interrogating D4 row, D5 row is interrogated by setting IC5 pin 15 high to confirm that the RPP has tripped. The electronic switches formed at pin 6 and pin 8 of IC7 are normally disabled by setting IC5 pin 19 low. If the GPIB requests that "HI" "LO" l.e.d. status on the front panel is interrogated IC5 pin 19 is set 'high' and all other rows are disabled (pin 15 low, pins 2,5,6,9,12 high).

147. The l.e.d's in the key switches and the group of l.e.d's indicating the modulation oscillator frequency are controlled by the latches IC2 and IC3. The resistors R1 and R2 control the current flowing in the l.e.d's.

AE1 - Power supply board

Circuit diagram : Chap. 7, Fig. 2

148. The mains supply range is set by two selector switches, SAR and SAS, whose position is locked by a cover plate. The mains transformer is located in a steel box underneath board AE1.

149. The power supply is required to generate regulated +24 V, +15 V, +5 V and -15 V d.c. voltage lines. The +5 V supply is derived from secondary 1 of the mains transformer. This is rectified by bridge D1 of AM0 and is located on the power supply chassis under the board AE1. The rectifier bridges for the other supplies (D1, D2, D3 or AE1) are located on the board AE1 together with the reservoir capacitors C1, C6, C7 and C10.

150. The d.c. from the reservoir capacitors is regulated by three terminal adjustable regulators. The regulators for the +5 V and +15 V supplies are IC1 and IC2 of AM0 and are located on the heatsink on the rear of the instrument. The potentiometers R2, R5, R8 and R11 enable the output voltages of each supply to be adjusted. Each of the regulator's ICs is protected against accidental shorts causing high discharge currents by 1N4004 rectifier diodes. The bypass capacitors C3, C5, C8 and C11 improve the ripple rejection of the regulators. Each regulator also has an internal thermal protection circuit.

151. The board AE1 has been carefully arranged such that the earth point of the resistor chain at the output of the regulator has been terminated on the chassis by a separate route to that of the reservoir capacitors. This ensures that the outputs from the regulators are free of mains supply ripple.

AT0/AT1 - 10 dB step attenuator

Circuit diagram : Chap. 7, Fig. 25

152. The p.c.b. AT1 is located in a casting and the board is made of a low loss p.t.f.e. based material. Screens are added to provide signal isolation at high frequencies. The lid of the attenuator uses beryllia copper springs to provide an r.f. connection between attenuator screen and the lid.

153. The board AT1 provides precision 10 dB steps in the output level and incorporates a reed relay to provide reverse power protection. Each attenuator pad consists of 3 precision chip resistors that provide attenuation of 10 dB, 20 dB or 30 dB. Each pad is switched in or out of circuit by microswitches actuated by a solenoid. When a pad is switched out the r.f. signal is connected to a direct bypass route. The insertion loss of the direct route and the pad (excluding the intended attenuation) is set up to be identical by the adjustment of small flags. These are adjusted by means of nylon screws in the screens. Each pad is separately set up and requires the use of specialist measuring facilities and it is recommended that this is carried out by the nearest Marconi Instruments agent or Marconi Instruments Service Division.

RPP - Reverse power protection

154. Resistors R16 to R20 form a high impedance r.f. signal divider at the output of the attenuator which is used to sense the r.f. present at the output of the attenuator. Diodes D1 and D2 detect the signal level and the resulting d.c. is connected for use in the r.p.p. system. If the signal level exceeds a preset limit the reed relay RLF is set to the open circuit condition in order to protect the attenuator from excessive power dissipation. The decoupling capacitors C1, C2 result in the detector being more sensitive to very low frequencies than to r.f. This ensures that it is not possible to damage the attenuator with externally applied d.c.

155. The reed relay RLF is mounted in a coaxial tube to ensure that the v.s.w.r. of the reed assembly is very low. It should be noted that the reed should be handled very carefully since it is fragile and is particularly prone to damage around the glass seals at each end. The reed is operated by the magnetic field from the inductor L1. L1 is wound on a bobbin and the reed relay, surrounded by its coaxial tube, is slid up the centre of the bobbin.

AT2 - Attenuator control

Circuit diagram : Chap. 7, Fig.. 26

156. Board AT2 controls the attenuator pads and the r.p.p. detector system. The board is located directly above the attenuator casting. The control lines that energize the attenuator pad solenoids come onto the board via PLAE from the motherboard AD2. When one of the solenoid connections is grounded by the open collector drivers IC5,IC6, current flows through the corresponding solenoid and the solenoid armature moves across and operates the attenuator microswitch.

157. When a solenoid is energized (control line grounded) the attenuator pad is switched out of circuit. The diodes D4 to D8 act as clamps to protect the open collector drivers on IC5,IC6. When a solenoid is de-energized the stored magnetic field causes a voltage spike on the control lines whose amplitude is clamped to a voltage approximately 0.7 V above the voltage on PLM, pin 5.

158. The power for the solenoids is supplied by PLP, pin 1. Normally this supply is at approximately +9 V. This, by itself, is not adequate to pull in the solenoids, therefore when the microprocessor updates the attenuator setting, supply to the solenoids is temporarily increased to approximately 20 V for 35 ms after a delay of 17 ms. This is accomplished by the monostable IC4 and transistors TR2 and TR3. When the attenuator setting is updated by an A6L10 instruction solenoids which are being de-energized have their input power immediately removed. Solenoids which are to be energized are connected to the +9 V supply via D11 during this time. After 17 ms the monostable IC4 is triggered on pin 9 and sets pin 5 high for 35 ms. This in turn switches TR3 on and connects the solenoids to a 20 V unregulated supply. This voltage then fully energizes the solenoids. After the 35 ms interval TR3 is turned off and the supply returns to 9 V unregulated. Sequencing the power to the solenoids in this fashion ensures that they de-energize quicker than they are magnetized, hence ensuring that large positive r.f. level transients are not generated.

159. The r.p.p. is also controlled on AT2. The output from the peak detectors used to detect the application of reverse power to the attenuator board AT1 is fed in to AT2 at PLN, pins 1, 3 and 4. IC1 detects the difference voltage between these detector outputs. The output on IC1, pin 6 is then compared with a reference on IC2.

160. If the detected signal level is excessive IC2, pin 7 is asserted 'high' resetting the R-S flip-flop formed by IC3. This results in IC3, pin 13 going 'high' turning off TR1. The voltage on PLN, pin 1 then falls to zero and the reed relay on AT1 attenuator is open circuited. The reaction time between the application of reverse power and the reed relay going open circuit is typically 80 µs. The Zener diode, D3, protects TR1 against the voltage transient when power is removed from the reed relay's operating inductor (i.e.d. D10 is on when the reed relay is closed to indicate that operation is normal).

161. When the reed relay goes open circuit the RPP ACTIVE line on PLV, pin 9 is asserted 'high'. This line is connected to the keyboard AD4 where the microprocessor detects its operation and responds accordingly. The r.p.p. is reset when the microprocessor sets the RPP RESET line on PLV, pin 12 to the 'low' state and then subsequently sets to 'high' again.

AG0 - GPIB adapter module

Circuit diagram : Chap. 7, Fig. 27

162. This module is an optional item and only fitted to 2018A/2019A when remote facilities are required. The module when connected to the rear panel, allows direct connection from a GPIB talker/listener device and implements the full IEEE 488 specifications (no control function).

163. IC2 (8291) GPIB talker/listener integrated circuit is connected to AA2 microprocessor via SKAK and AD2 motherboard providing both talker and listener capabilities, details of these are given in Chapter 3 of the Operating Manual. IC3a and IC8 determine the read and write address decoding cycle. IC1 operates as an independent clock whose frequency (between 1 and 2 MHz) is used to time out an approximate 2 µs delay allowing the bus to settle after sending data.

164. IC4 - IC7 transceivers are used to translate the negative true logic and act as drivers. IC3b provides the logic 'low' level for the receive instruction TR/1 to IC5, pins 7,9; or the talker 'high' level for IC5, IC6 and IC7 and also provides the additional buffering necessary for the three ICs in line.

165. PLDW is an auxiliary plug which is externally accessed to provide the means of controlling external relays or similar. Eight data outputs (D0-D7) are driven by IC10 which can supply up to 50 mA to the load. An enable input (pin 10) is internally connected to +5 V by R2 so that when the enable line is open circuit the data lines will all remain enabled. If the outputs are to be connected to a load that has an integral power supply with a +5 V line available it is preferable to connect the enable pin to this. In the event of an external power failure the enable pin will be set 'low' and the data lines will be disabled. Setting data on each line is achieved by means of Second function 18.

SECOND FUNCTION OPERATIONS

166. Second function operations provide the means of controlling various secondary features and calibrations within the instrument. There are three levels of operation, two of which require unlocking in order to gain access. Each level of operation and method of access is described below.

167. Normal operation

2nd functions	'0'	Unlock	These functions are unprotected and may be accessed directly:- Press SECOND FUNCT followed by the appropriate numeral(s).
	'1'	Status information	
	'2'	GPIB address setting	
	'3'	Manual latch setting	
	'4'	SRQ mask setting	
	'9'	Elapsed time display	
	'11'	Read identity string	
	'12'	Write user-definable string	
	'13'	Read user-definable string	
	'18'	Set data on GPIB Aux. output pins.	

168. First level operation

2nd functions	˝5˝	RF level units setting	These functions have first degree protection and are accessed by the following procedure:- Press SECOND FUNCT, 0 then the MOD ALC and AF ON/OFF keys simultaneously, holding these down until a ˝1˝ appears in the carrier frequency window indicating access to first level operations. Follow this by pressing SECOND FUNCT and the numeral(s) required.
	˝6˝	RF level offset	
	˝14˝	1 or 10 MHz standard setting	
	˝15˝	Old/new GPIB command set	
	˝16˝	Recall STORE 10 at switch on	

169. Second level operation

2nd functions	˝7˝	RF level calibration	These functions have second degree protection and are accessed by the following procedure:- Press SECOND FUNCT, 0 then in the rotation given first MOD ALC then AF ON-OFF and finally CARRIER FREQ key, hold down all three keys until a ˝2˝ appears in the carrier frequency window indicating access to second level operations. Follow this by pressing SECOND FUNCT and the appropriate numeral(s) required.
	˝8˝	FM calibration	
	˝9˝	Reset of elapsed time display	
	˝10˝	Read total instrument operating time	
	˝17˝	Calibration and storage of amended EAROM checksum	
	˝190˝	Write - Identify string setting	
	˝191˝	Protection of store settings	
	˝192˝	Display blanking of recalled stores	

170. Second function ˝3˝ Manual latch setting. Second functions that are used in normal operation of the instrument are described in the Operating Manual Vol. 1. Second function 3 Manual latch setting however is used only in maintenance applications and is therefore described here. Second function 3 allows the operator to direct an 8-bit binary instruction to any of the instrument˝s internal latches for testing and fault finding. The latch is selected first by selecting SECOND FUNCT 3 mode then entering the number of the data valid line (1 digit 4 to 7), this is displayed in the Modulation display window. This should be followed by the number of the latch (2 digits 00 to 15), this is displayed in the RF level window.

171. The current value of data normally applied to the latch is then displayed in the Carrier frequency window. New data can then be entered in binary (8 binary digits 00000000 to 11111111), most significant bit first. The decimal point indicates the division between the changed data and that entered initially. Where a latch location serves several miscellaneous functions and only one bit needs to be amended considerable time is saved in not having to specify other irrelevant bits that are present in the same latch location. The decimal point key allows the moving of the displayed decimal point without actually changing data.

AG0 - GPIB adapter module

Circuit diagram : Chap. 7, Fig. 27

162. This module is an optional item and only fitted to 2018A/2019A when remote facilities are required. The module when connected to the rear panel, allows direct connection from a GPIB talker/listener device and implements the full IEEE 488 specifications (no control function).

163. IC2 (8291) GPIB talker/listener integrated circuit is connected to AA2 microprocessor via SKAK and AD2 motherboard providing both talker and listener capabilities, details of these are given in Chapter 3 of the Operating Manual. IC3a and IC8 determine the read and write address decoding cycle. IC1 operates as an independent clock whose frequency (between 1 and 2 MHz) is used to time out an approximate 2 µs delay allowing the bus to settle after sending data.

164. IC4 - IC7 transceivers are used to translate the negative true logic and act as drivers. IC3b provides the logic "low" level for the receive instruction TR/1 to IC5, pins 7,9; or the talker "high" level for IC5, IC6 and IC7 and also provides the additional buffering necessary for the three ICs in line.

165. PLDW is an auxiliary plug which is externally accessed to provide the means of controlling external relays or similar. Eight data outputs (D0-D7) are driven by IC10 which can supply up to 50 mA to the load. An enable input (pin 10) is internally connected to +5 V by R2 so that when the enable line is open circuit the data lines will all remain enabled. If the outputs are to be connected to a load that has an integral power supply with a +5 V line available it is preferable to connect the enable pin to this. In the event of an external power failure the enable pin will be set "low" and the data lines will be disabled. Setting data on each line is achieved by means of Second function 18.

SECOND FUNCTION OPERATIONS

166. Second function operations provide the means of controlling various secondary features and calibrations within the instrument. There are three levels of operation, two of which require unlocking in order to gain access. Each level of operation and method of access is described below.

167. Normal operation

2nd functions	"0"	Unlock	These functions are unprotected and may be accessed directly:- Press SECOND FUNCT followed by the appropriate numeral(s).
	"1"	Status information	
	"2"	GPIB address setting	
	"3"	Manual latch setting	
	"4"	SRQ mask setting	
	"9"	Elapsed time display	
	"11"	Read identity string	
	"12"	Write user-definable string	
	"13"	Read user-definable string	
	"18"	Set data on GPIB Aux. output pins.	

168. First level operation

2nd functions	"5"	RF level units setting	These functions have first degree protection and are accessed by the following procedure:- Press SECOND FUNCT, 0 then the MOD ALC and AF ON/OFF keys simultaneously, holding these down until a "1" appears in the carrier frequency window indicating access to first level operations. Follow this by pressing SECOND FUNCT and the numeral(s) required.
	"6"	RF level offset	
	"14"	1 or 10 MHz standard setting	
	"15"	Old/new GPIB command set	
	"16"	Recall STORE 10 at switch on	

169. Second level operation

2nd functions	"7"	RF level calibration	These functions have second degree protection and access to Second level operation is restricted to authorized calibration units only. Interference with these second functions could invalidate the instrument's calibration.
	"8"	FM calibration	
	"9"	Reset of elapsed time display	
	"10"	Read total instrument operating time	
	"17"	Calibration and storage of amended EAROM checksum	
	"190"	Write - Identify string setting	
	"191"	Protection of store settings	
	"192"	Display blanking of recalled stores	

170. Second function "3" Manual latch setting. Second functions that are used in normal operation of the instrument are described in the Operating Manual Vol. 1. Second function 3 Manual latch setting however is used only in maintenance applications and is therefore described here. Second function 3 allows the operator to direct an 8-bit binary instruction to any of the instrument's internal latches for testing and fault finding. The latch is selected first by selecting SECOND FUNCT 3 mode then entering the number of the data valid line (1 digit 4 to 7), this is displayed in the Modulation display window. This should be followed by the number of the latch (2 digits 00 to 15), this is displayed in the RF level window.

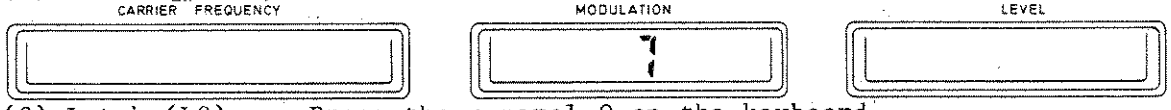
171. The current value of data normally applied to the latch is then displayed in the Carrier frequency window. New data can then be entered in binary (8 binary digits 00000000 to 11111111), most significant bit first. The decimal point indicates the division between the changed data and that entered initially. Where a latch location serves several miscellaneous functions and only one bit needs to be amended considerable time is saved in not having to specify other irrelevant bits that are present in the same latch location. The decimal point key allows the moving of the displayed decimal point without actually changing data.

172. The amended data when set, can be sent to the latch by pressing the STORE key. New data can also be sent without re-entering the latch address if required. Pressing any orange function key other than the STORE key will result in the data being overwritten and the instrument being returned to normal operation.

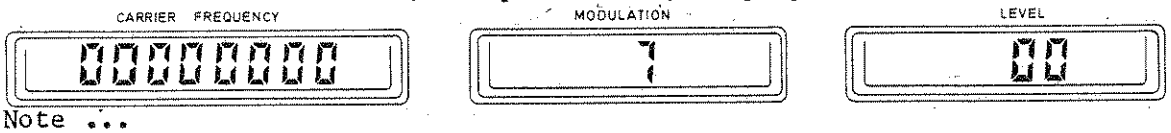
173. Further details of the control data used for individual boards is given in Chap. 5, Maintenance. The example following illustrates the procedure for setting the control data to a board such as AC5, Amplitude modulator. To set 30% modulation on the board carry out the steps (1) to (3) as follows:-

Latch address for AC5 board is A7L0

(1) Address (A7); Press the numeral 7 on the keyboard, display shows:-



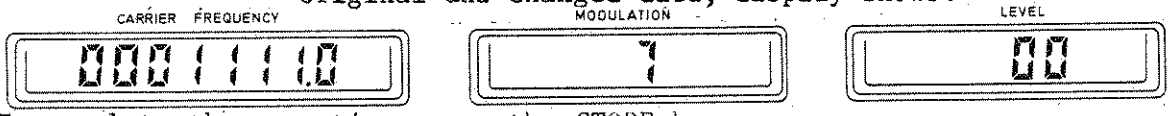
(2) Latch (L0); Press the numeral 0 on the keyboard twice (L0 implies L00), display shows:-



Note ...

Current value of AM is 0% and the +6 dB mode is off.

(3) 30% Modulation; To obtain 30% modulation, set a binary 30 in the Carrier Frequency display by entering either 1's or 0's from the keyboard, the decimal point indicates the division between original and changed data, display shows:-



To complete the operation press the STORE key.

174. Second function '7' RF level calibration setting. The output level is calibrated by setting a control number (0 - 255) at 10 MHz, 260 MHz and 520 MHz (780 MHz and 1040 MHz for 2019A) via second function 7. At all other frequencies the required control data is calculated from these numbers. The instrument allows access to one of these numbers at a time, according to the current carrier frequency. The current value is shown in the RF level display window when second function 7 is selected: a new number may be entered via the keyboard, (or GPIB) or the displayed number changed using the UP and DOWN keys. The output level changes accordingly: to store the new number press the 'STORE' key. It is necessary to ensure that offsets are "off" before using this facility.

175. Second function '8' FM tracking. The frequency deviation when f.m. is selected is calibrated at 84 frequencies: at other frequencies the required data is calculated internally from the adjacent tracking point data. In order to set a calibration figure at a tracking point, the generator must first be set to the required frequency, with f.m. on, in the normal way. Second function 8 will then display the current calibration number in the RF level display window. This number may be changed by entering a new number, or incremented using the UP and DOWN keys for convenient fine control: the

change is effective immediately. The STORE key is used to overwrite the old number with the new: until this happens no permanent change to the calibration data is effected.

176. Should the generator be tuned to a frequency which does not correspond to a tracking point, second function 8 will display the "---" (retuning required) message.

177. Second function '9'. Reset of elapsed time display. Selection of second function 9 without unlocking the instrument to the second level of operation will result in an elapsed time since last reset display. To reset this to zero overcome the second degree protection and allow second level operation, then select SECOND FUNCT 9. Follow this by pressing the '0' and STORE keys.

178. Second function '10'. Read - total instrument operating time. This read only facility gives the total number of operating hours since instrument manufacture and is used to establish mean time before repair (MTBR) figures. Selection of second function 10 after first unlocking the instrument to allow second level operation will give a record of the elapsed time (in hours), this is displayed in the carrier frequency window with a resolution of 0.5 hrs. When first receiving the instrument a display of elapsed time will be evident, this reflects the factory's initial calibration period.

179. Second function '17'. Calibration and storage of amended EAROM checksum. The initial operating mode of the instrument should be shown on the front panel display at switch on. This is carrier frequency 520 MHz (1040 MHz, 2019A) internal mod. osc. 1kHz, no modulation and minimum r.f. level (-127 dBm or equivalent). Before this occurs a check on the serviceability of the PROM and RAM is carried out and a checksum is initiated on the EAROM stored data. If either PROM or RAM checks are in error the instrument will be unable to take up the initial operating mode and error message 10,12,13 or 14 will be displayed in the carrier frequency window instead. Details of error messages are to be found in the Operating Manual Vol. 1.

180. Likewise if for any reason the non-volatile EAROM on AA2/1 board has failed or been replaced or if new RF level calibration or FM tracking data has been entered (as a result of recalibration) the checksum will not agree. Error number 06 will be displayed in the carrier frequency window until any front panel key is pressed, or any GPIB instruction is received.

181. A new checksum can be calculated and stored by invoking SECOND FUNCT 17 and pressing the store key. Suitable calibration procedures should, however, precede this operation. Details of this procedure are given in Chapter 5 Maintenance.

182. Second function '190' Write - Identity string setting. This facility will normally only be required to initialize the instrument. The identity string shows the instrument type number and serial number. This information can be read via the GPIB. A typical instrument display is shown in the Operating Manual Vol. 1 Chap. 3 under second function 11. The instrument type number and software issue number is shown first, e.g. 52019-910, 001, followed by the instrument serial number. Type and serial number can be reset but the software issue number is built into the software and cannot be changed.

183. After unlocking the instrument to allow second level operation select SECOND FUNCT 190 keys and entering digits (only) from the left set the first part of the identity string (instrument type number) then terminate the entry by pressing the STORE key. Press the decimal point key to access and set the second part of the string (instrument serial number) and enter digits as before. Again terminate the entry by pressing the STORE key.

184. Second function ´191´ Protection of store setting. This facility disables the operation of the STORE key in the normal mode of operation in order to provide protection against inadvertent alteration. Unlock the instrument to second level operation then SECOND FUNCT 191 keys followed either by the numeral ´1´ (protection of stores) or ´0´ (protection released) then terminate the entry with the STORE key. Attempts to overwrite the store contents when protected will result in Error message 11 being displayed in the carrier frequency window.

185. Second function ´192´ Display blanking of recalled stores. This facility enables restrictions to be exercised on the display of data set in stores should this be of a classified nature. Front panel display information is blanked when any store (other than 00) is recalled. All information concerning the existing status, with the exception of error messages and total shift data is prevented from reaching the display. Select SECOND FUNCT 192 then the numeral ´1´ followed by the STORE key to enable the facility. To disable the facility select ´0´ and STORE keys. Recall of store 00 will give a valid display of that stores contents and return the instrument to the normal display mode.

Chapter 5

MAINTENANCE

CONTENTS

INTRODUCTION

1. This chapter contains information for keeping the equipment in good working order, checking overall performance, fault finding and realignment procedures. Before attempting any maintenance on the equipment you are advised to read the preceding chapter containing the technical description.

2. Test procedures described in this chapter may be simplified and of restricted range compared with those that relate to the generally more comprehensive factory test facilities, which are necessary to demonstrate complete compliance with the specifications.

3. Performance limits quoted are for guidance and should be taken as guaranteed performance specifications unless they are also quoted in the performance data in Chap. 1. When making tests to verify that the instrument meets the stated performance limits, allowance must always be made for the uncertainty of the test equipment used.

4. In case of difficulties which cannot be resolved with the aid of this book, please contact our Sales Division at the address given inside the rear cover, or your nearest Marconi Instruments representative. Always quote the type and serial number found on the data plate at the rear of the instrument.

5. Integrated circuit and semiconductor devices are used throughout this instrument and, although these have inherent long term reliability and mechanical ruggedness, they are susceptible to damage by overloading, reverse polarity and excessive heat or radiation and the use of insulation testers.

6. Numerous chip capacitors and resistors are fitted in this equipment. These have silver palladium end cap terminations. When soldering these devices the following precautions should be observed.

(i) Use solder containing 2% silver, and a temperature controlled 45 watt soldering iron set to 315^{0}C (600^{0}F). The use of a high wattage soldering iron will minimize the time taken to solder the device.

(ii) When soldering chip components to printed circuit boards a long fillet of solder should be laid on the track leading up to each end cap termination. This reduces the otherwise adverse inductive effects at high frequencies.

7. **Static sensitive components.** The c.m.o.s. integrated circuits used in this instrument have extremely high input resistance and can be damaged by accumulation of static charges (see preliminary pages, Notes and Cautions). Boards that have such integrated circuits all carry warning notices against damage by static discharge. Care must also be taken when using freezer sprays to aid fault finding. These can create a static charge likely to change the programmed memory of (E)PROMS.

8. **Beryllia health hazard.** This material is used in the construction of transistor TR10 in Unit AC4. Warning notices are displayed and extreme care must be exercised when wishing to disturb this transistor (see preliminary pages, Notes and Cautions).

9. Bulkhead connectors and gaskets. Special care should be taken to ensure that no r.f. leakage occurs. To this end all bulkhead connectors and lid sealing gaskets should be secure. It is essential that the unit lids be correctly relocated in their slotted recesses after removal.

10. Fault location. Some aid to fault finding is provided by the typical d.c. voltage and signal levels. Tables given are not extensive but are intended as a pointer to further investigation. It is emphasized that each fault table should be studied having regard for the others, since incorrect operation of a circuit may be caused by malfunction of an associated circuit.

PERFORMANCE CHECKS

Overall tests and adjustments

11. Many of the tests described in this chapter are simplified and of restricted range compared with those which would demonstrate compliance with the specification as described in paras. 1 to 4. If the results quoted in the following paragraphs are not obtainable refer to the related fault finding section and tables, and after repair ensure that realignment is carried out in accordance with the Instrument Calibration section, if applicable.

Frequency accuracy

Test equipment : items d, Digital frequency meter
n, Standard frequency source (10 MHz)

12. (1) Connect the frequency meter to the output of the instrument.

(2) It is advisable to synchronize the frequency meter with an external standard frequency accuracy 2 parts in 10^8 if possible.

(3) With the 2018A in any mode of operation and the INT standard selected carry out spot checks throughout the range of the instrument and ensure that frequencies are within specifications.

(4) Check that the output from the rear panel STD FREQ IN-OUT socket is a nominal 3 V p-p frequency signal at 10 MHz ±1 Hz. The standard frequency trim R1 can be accessed through the upper right-hand side outer cover and enables the internal standard to be set against a primary external standard.

CAUTION

Incorrect adjustment of this preset will impair the frequency accuracy of the generator. Allow at least 10 minutes warm-up and switch the frequency counter to Select 'B' 1 Hz resolution. Adjust R1 for a reading of 10 MHz ±1 Hz then switch the frequency counter to 0.1 Hz resolution and check the indication is the same after five counter gates.

TABLE 1 TEST EQUIPMENT

Item	Description	Minimum use specifications	Recommended model
b	T connector	VSWR ≯ 1.2:1 at 1500 MHz, terminated in 50 Ω	TM 7948
c	N type 50 Ω	VSWR ≯ 1.05:1 up to 1500 MHz	TM 7967
d	Digital frequency meter	Frequency range: 10 Hz to 2 GHz Sensitivity: 56 mV r.m.s. p.d. into 50 Ω Input impedance: LF 1 MHz in parallel with less than 25 pF. Nominal 50 Ω	2435
e	Multimeter	Greater than 20 kΩ/V	GEC Selectest
f	Power meter	Power range measurement: -30 to +13 dBm Accuracy: ±0.15 dB Frequency range: 80 kHz to 1040 MHz	6960 Series & 6912 Sensor
g	Distortion factor meter	Fundamental range: 20 Hz to 20 kHz Fundamental rejection: 80 dB Measurement accuracy: ±2% of full-scale ±2% of reading	TF 2331A or 2305
h	AM/FM modulation meter		2305
i	AF oscillator	Frequency range: 10 Hz to 110 kHz Accuracy: ±3% of reading Distortion: Better than -100 dB from 10 Hz to 30 kHz Level: 0 to 3 V	TF 2104
j	Digital voltmeter	DC volts. Ranges: ±10 mV to ±1000 V Resolution: 0.01% of range (10 µV on 100 mV range). Accuracy: ±100 mV range ±(0.05% of input + 0.02% of range ±1 V to 1000 V range ±(0.02% o input +0.01% of range)	
k	(i) Spectrum analyzer (ii) Frequency extender (iii) Zero loss probe	Frequency range: 10 kHz to 1.25 GHz Variable persistance/storage display	TF 2370/ TK 2373 & TK 2374

TABLE 1 TEST EQUIPMENT (continued)

Item	Description	Minimum use specifications	Recommended model
l	AF voltmeter	Range: 1 mV to 100 V f.s.d. Frequency range: 10 Hz to 10 MHz Accuracy: ±1%	TF 2600B
m	Oscilloscope with dual trace capability	Bandwidth: 50 MΩ Volts/division: 5 mV to 20 V	TELEQUIPMENT D83 with V4 dual channel wide band amp. plug in
n	Standard frequency source (10 MHz)	Output level: 4 V p-p Frequency accuracy: 2 parts in 10^8	Rubidium or Caesium reference unit
o	Variable d.c. power supply	0 to 30 V d.c. at 1 A	TF 2155/1
p	Sweep oscillator & RF plug-in unit	Frequency range: 5 MHz to 2 GHz Sweep output: +2 V to +10 V Markers, amplitude -5 V F1-F2 symmetrical sweep	6700B/6730A
q	Rho-bridge with two standard 50 Ω loads and calibrated mismatched loads	Frequency range: 1 MHz to 1 GHz Residual v.s.w.r.: ⩾ 1.01:1 from 5 MHz to 1 GHz Characteristic impedance: 50 Ω Calibrated mismatched loads: 1.2:1,1.5:1 Two standard 50 Ω loads, v.s.w.r. better than 1.02:1 from 1 MHz to 1 GHz.	

TABLE 2 DECIBEL CONVERSION TABLE

Ratio Down			Ratio Up	
VOLTAGE	POWER	DECIBELS	VOLTAGE	POWER
1·0	1·0	0	1·0	1·0
·9886	·9772	·1	1·012	1·023
·9772	·9550	·2	1·023	1·047
·9661	·9333	·3	1·035	1·072
·9550	·9120	·4	1·047	1·096
·9441	·8913	·5	1·059	1·122
·9333	·8710	·6	1·072	1·148
·9226	·8511	·7	1·084	1·175
·9120	·8318	·8	1·096	1·202
·9016	·8128	·9	1·109	1·230
·8913	·7943	1·0	1·122	1·259
·8710	·7586	1·2	1·148	1·318
·8511	·7244	1·4	1·175	1·380
·8318	·6918	1·6	1·202	1·445
·8128	·6607	1·8	1·230	1·514
·7943	·6310	2·0	1·259	1·585
·7762	·6026	2·2	1·288	1·660
·7586	·5754	2·4	1·318	1·738
·7413	·5495	2·6	1·349	1·820
·7244	·5248	2·8	1·380	1·905
·7079	·5012	3·0	1·413	1·995
·6683	·4467	3·5	1·496	2·239
·6310	·3981	4·0	1·585	2·512
·5957	·3548	4·5	1·679	2·818
·5623	·3162	5·0	1·778	3·162
·5309	·2818	5·5	1·884	3·548
·5012	·2512	6	1·995	3·981
·4467	·1995	7	2·239	5·012
·3981	·1585	8	2·512	6·310
·3548	·1259	9	2·818	7·943
·3162	·1000	10	3·162	10·000
·2818	·07943	11	3·548	12·59
·2512	·06310	12	3·981	15·85
·2239	·05012	13	4·467	19·95
·1995	·03981	14	5·012	25·12
·1778	·03162	15	5·623	31·62

TABLE 2 DECIBEL CONVERSION TABLE (continued)

Ratio Down			Ratio Up	
VOLTAGE	POWER	DECIBELS	VOLTAGE	POWER
·1585	·02512	16	6·310	39·81
·1413	·01995	17	7·079	50·12
·1259	·01585	18	7·943	63·10
·1122	·01259	19	8·913	79·43
·1000	·01000	20	10·000	100·00
·07943	$6{\cdot}310 \times 10^{-3}$	22	12 59	158·5
·06310	$3{\cdot}981 \times 10^{-3}$	24	15·85	251·2
·05012	$2{\cdot}512 \times 10^{-3}$	26	19·95	398·1
·03981	$1{\cdot}585 \times 10^{-3}$	28	25 12	631 0
·03162	$1{\cdot}000 \times 10^{-3}$	30	31·62	1,000
·02512	$6{\cdot}310 \times 10^{-4}$	32	39·81	$1{\cdot}585 \times 10^{3}$
·01995	$3{\cdot}981 \times 10^{-4}$	34	50·12	$2{\cdot}512 \times 10^{3}$
·01585	$2{\cdot}512 \times 10^{-4}$	36	63·10	$3{\cdot}981 \times 10^{3}$
·01259	$1\ 585 \times 10^{-4}$	38	79·43	$6{\cdot}310 \times 10^{3}$
·01000	$1{\cdot}000 \times 10^{-4}$	40	100·00	$1{\cdot}000 \times 10^{4}$
$7{\cdot}943 \times 10^{-3}$	$6{\cdot}310 \times 10^{-5}$	42	125·9	$1{\cdot}585 \times 10^{4}$
$6{\cdot}310 \times 10^{-3}$	$3\ 981 \times 10^{-5}$	44	158·5	$2{\cdot}512 \times 10^{4}$
$5{\cdot}012 \times 10^{-3}$	$2{\cdot}512 \times 10^{-5}$	46	199·5	$3{\cdot}981 \times 10^{4}$
$3\ 981 \times 10^{-3}$	$1{\cdot}585 \times 10^{-5}$	48	251·2	$6{\cdot}310 \times 10^{4}$
$3{\cdot}162 \times 10^{-3}$	$1{\cdot}000 \times 10^{-5}$	50	316·2	$1{\cdot}000 \times 10^{5}$
$2{\cdot}512 \times 10^{-3}$	$6{\cdot}310 \times 10^{-6}$	52	398·1	$1{\cdot}585 \times 10^{5}$
$1{\cdot}995 \times 10^{-3}$	$3{\cdot}981 \times 10^{-6}$	54	501·2	$2{\cdot}512 \times 10^{5}$
$1{\cdot}585 \times 10^{-3}$	$2{\cdot}512 \times 10^{-6}$	56	631·0	$3{\cdot}981 \times 10^{5}$
$1{\cdot}259 \times 10^{-3}$	$1{\cdot}585 \times 10^{-6}$	58	794·3	$6{\cdot}310 \times 10^{5}$
$1{\cdot}000 \times 10^{-3}$	$1{\cdot}000 \times 10^{-6}$	60	1,000	$1{\cdot}000 \times 10^{6}$
$5{\cdot}623 \times 10^{-4}$	$3{\cdot}162 \times 10^{-7}$	65	$1{\cdot}778 \times 10^{3}$	$3{\cdot}162 \times 10^{6}$
$3{\cdot}162 \times 10^{-4}$	$1{\cdot}000 \times 10^{-7}$	70	$3{\cdot}162 \times 10^{3}$	$1{\cdot}000 \times 10^{7}$
$1{\cdot}778 \times 10^{-4}$	$3{\cdot}162 \times 10^{-8}$	75	$5{\cdot}623 \times 10^{3}$	$3{\cdot}162 \times 10^{7}$
$1{\cdot}000 \times 10^{-4}$	$1{\cdot}000 \times 10^{-8}$	80	$1{\cdot}000 \times 10^{4}$	$1{\cdot}000 \times 10^{8}$
$5{\cdot}623 \times 10^{-5}$	$3{\cdot}162 \times 10^{-9}$	85	$1{\cdot}778 \times 10^{4}$	$3{\cdot}162 \times 10^{8}$
$3{\cdot}162 \times 10^{-5}$	$1{\cdot}000 \times 10^{-9}$	90	$3{\cdot}162 \times 10^{4}$	$1{\cdot}000 \times 10^{9}$
$1{\cdot}000 \times 10^{-5}$	$1{\cdot}000 \times 10^{-10}$	100	$1{\cdot}000 \times 10^{5}$	$1{\cdot}000 \times 10^{10}$
$3{\cdot}162 \times 10^{-6}$	$1{\cdot}000 \times 10^{-11}$	110	$3{\cdot}162 \times 10^{5}$	$1{\cdot}000 \times 10^{11}$
$1{\cdot}000 \times 10^{-6}$	$1{\cdot}000 \times 10^{-12}$	120	$1{\cdot}000 \times 10^{6}$	$1{\cdot}000 \times 10^{12}$
$3{\cdot}162 \times 10^{-7}$	$1{\cdot}000 \times 10^{-13}$	130	$3\ 162 \times 10^{6}$	$1{\cdot}000 \times 10^{13}$
$1{\cdot}000 \times 10^{-7}$	$1{\cdot}000 \times 10^{-14}$	140	$1{\cdot}000 \times 10^{7}$	$1{\cdot}000 \times 10^{14}$

TABLE 3 dBµV CONVERSION TABLE

dBm	EMF (r.m.s.)	dBµV (e.m.f.)	dBm	EMF (r.m.s.)	dBµV (e.m.f.)	dBm	EMF (r.m.s.)	dBµV (e.m.f.)
-130	.141µV	-17	-80	44.7µV	+33	-30	14.1mV	+83
-129	.159	-16	-79	50.2	+34	-29	15.9	+84
-128	.178	-15	-78	56.3	+35	-28	17.8	+85
-127	.200	-14	-77	63.2	+36	-27	20.0	+86
-126	.224	-13	-76	70.9	+37	-26	22.4	+87
-125	.251	-12	-75	79.5	+38	-25	25.1	+88
-124	.282	-11	-74	89.2	+39	-24	28.2	+89
-123	.317	-10	-73	100	+40	-23	31.7	+90
-122	.355	-9	-72	112	+41	-22	35.5	+91
-121	.399	-8	-71	126	+42	-21	39.9	+92
-120	.447	-7	-70	141	+43	-20	44.7	+93
-119	.502	-6	-69	159	+44	-19	50.2	+94
-118	.563	-5	-68	178	+45	-18	56.3	+95
-117	.632	-4	-67	200	+46	-17	63.2	+96
-116	.700	-3	-66	224	+47	-16	70.9	+97
-115	.795	-2	-65	251	+48	-15	79.5	+98
-114	.892	-1	-64	282	+49	-14	89.2	+99
-113	1.00	0	-63	317	+50	-13	100	+100
-112	1.12	+1	-62	355	+51	-12	112	+101
-111	1.20	+2	-61	399	+52	-11	126	+102
-110	1.41	+3	-60	447	+53	-10	141	+103
-109	1.59	+4	-59	502	+54	-9	159	+104
-108	1.78	+5	-58	563	+55	-8	178	+105
-107	2.00	+6	-57	632	+56	-7	200	+106
-106	2.24	+7	-56	709	+57	-6	224	+107
-105	2.51	+8	-55	795	+58	-5	251	+108
-104	2.82	+9	-54	892	+59	-4	282	+109
-103	3.17	+10	-53	1.00mV	+60	-3	317	+110
-102	3.55	+11	-52	1.12	+61	-2	355	+111
-101	3.99	+12	-51	1.26	+62	-1	399	+112
-100	4.47	+13	-50	1.41	+63	0	447	+113
-99	5.02	+14	-49	1.59	+64	+1	502	+114
-98	5.63	+15	-48	1.78	+65	+2	563	+115
-97	6.32	+16	-47	2.00	+66	+3	632	+116
-96	7.09	+17	-46	2.24	+67	+4	709	+117
-95	7.95	+18	-45	2.51	+68	+5	795	+118
-94	8.92	+19	-44	2.82	+69	+6	892	+119
-93	10.0	+20	-43	3.17	+70	+7	1.00V	+120
-92	11.2	+21	-42	3.55	+71	+8	1.12	+121
-91	12.6	+22	-41	3.99	+72	+9	1.26	+122
-90	14.1	+23	-40	4.47	+73	+10	1.41	+123
-89	15.9	+24	-39	5.02	+74	+11	1.59	+124
-88	17.8	+25	-38	5.63	+75	+12	1.78	+125
-87	20.0	+26	-37	6.32	+76	+13	2.00	+126
-86	22.4	+27	-36	7.09	+77	+14	2.24	+127
-85	25.1	+28	-35	7.95	+78	+15	2.51	+128
-84	28.2	+29	-34	8.92	+79	+16	2.82	+129
-83	31.7	+30	-33	10.0	+80	+17	3.17	+130
-82	35.5	+31	-32	11.2	+81	+18	3.55	+131
-81	39.9	+32	-31	12.6	+82	+19	3.99	+132
						+20	4.47	+133

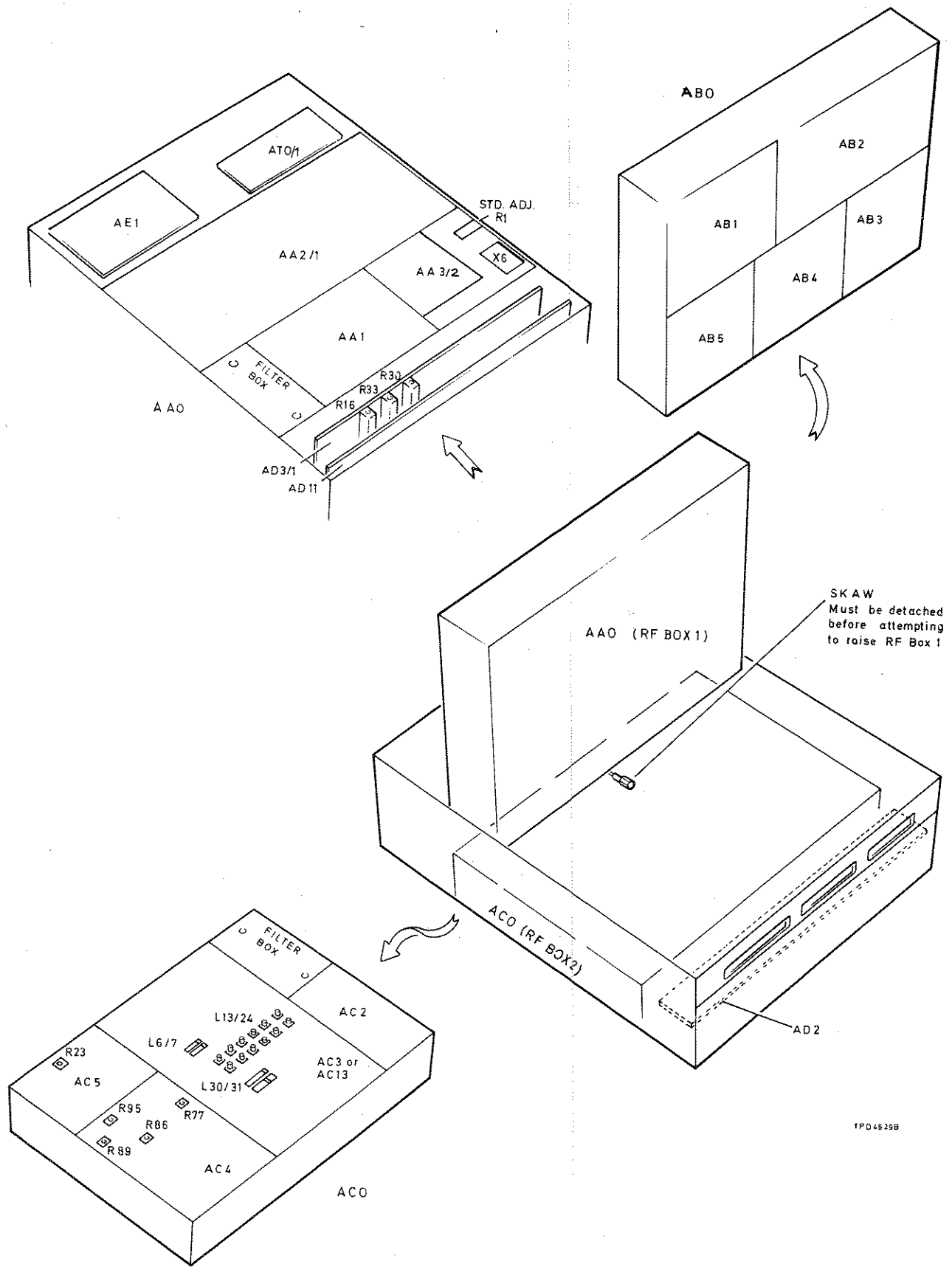


Fig. 1a Board location, access and preset adjustments

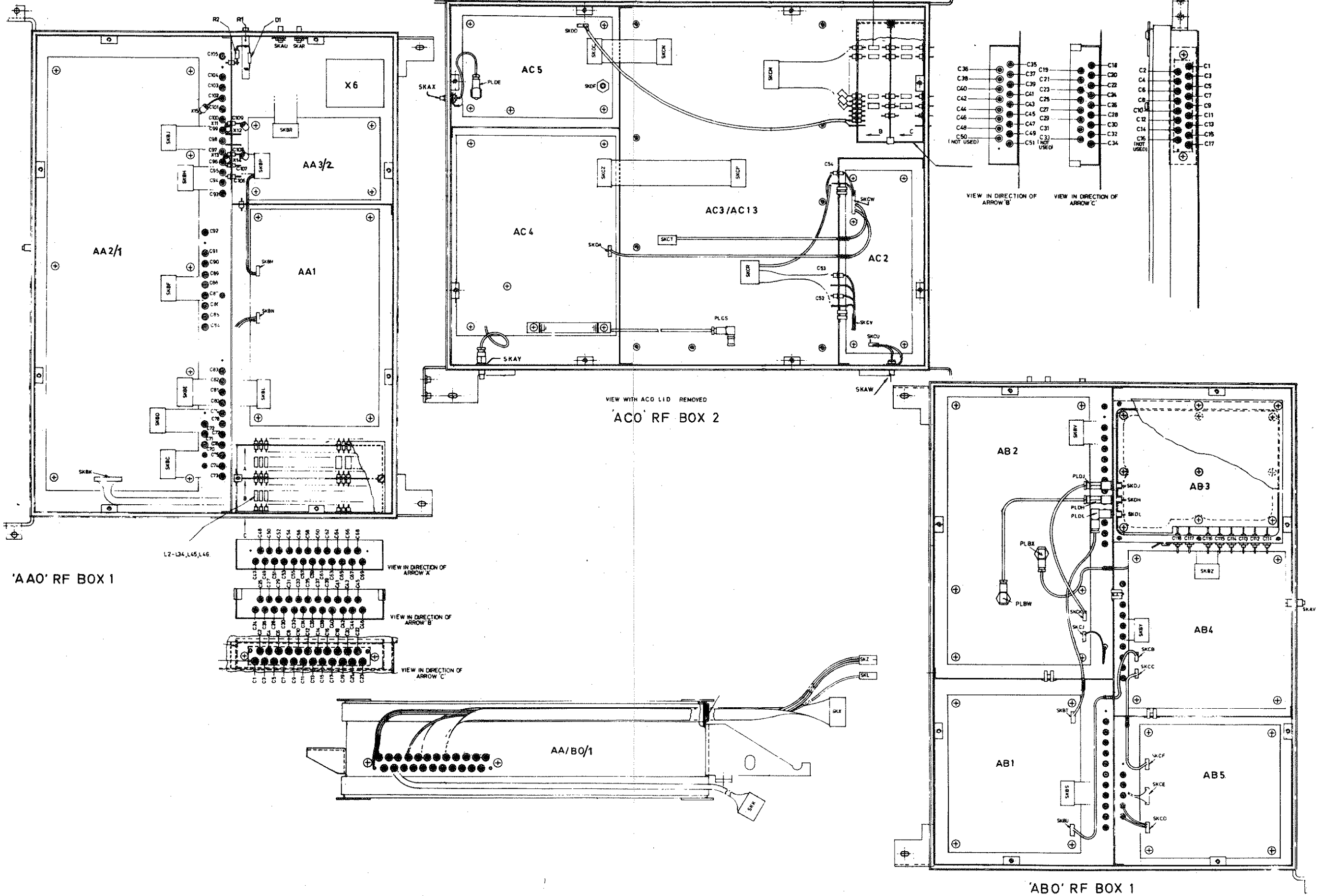


Fig. 1b Location of components, connectors, plugs and sockets

RF output

Test equipment a, power meter	minimum specification 80 kHz to 1040 MHz -30 to +13 dBm with accuracy better than ±0.15 dB	Example Marconi 6960 with 6912 power sensor

Performance specification: ±2 dB from 80 kHz to 520 MHz.
±2 dB from 520 MHz to 1040 MHz.

Procedure: connect the equipment as shown.

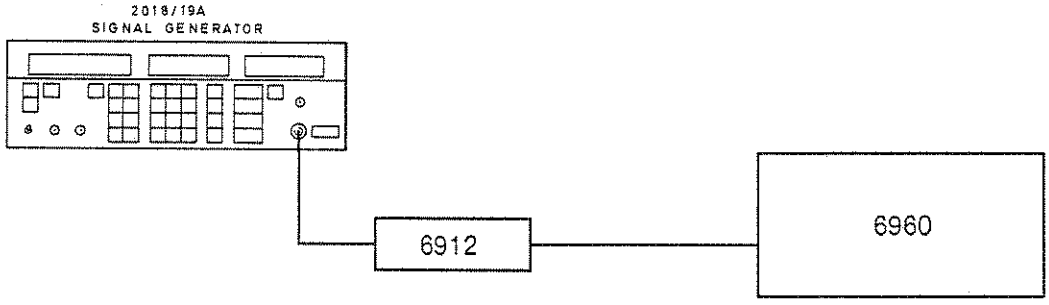


Fig. 2 Test gear arrangement for r.f. output measurements

Set the 2018A/19A to give a carrier frequency of 10 MHz and an r.f. level of 0 dBm.

Check that he indication on the power meter is within ±1 dB of that selected.

Repeat for random carrier frequencies from 80 kHz to 520 MHz and random levels between -30 dBm and ±13 dBm.

If the instrument being checked is a 2019A, repeat for random carrier frequencies between 520 MHz and 1040 MHz, this time checking that the level displayed on the power meter is within ±2 dB of that selected on the 2019A.

Coarse attenuator functional check

Test equipment : item k, Spectrum analyzer

15. The 10 dB step attenuator contains three 30 dB pads, one 20 dB pad and one 10 dB pad. Each of these may be selected individually by utilizing the second function 3 mode. Connect the spectrum analyzer to the RF OUTPUT socket and select +7 dBm on the 2018A. The coarse attenuator AT0/AT1 is controlled from AD2 motherboard, address A6L10. To select each of the relays in turn carry out the following procedure:-

(1) Select SECOND FUNCT 3.

(2) Enter by means of the instrument keyboard, the address valid, (6), followed by the address latch number (10). The modulation display window will indicate 06 and the level display window 10.

(3) Enter the data in binary 1 or 0 from the keyboard, numbers are rotated in from the right and are displayed in the carrier frequency window. Each relay may be selected by the binary number shown below in Table 4.

TABLE 4 ATO/AT1 ATTENUATOR FUNCTIONAL CHECK

Binary No.								Relay de-energized	Attenuator pad	RF output
D7	D6	D5	D4	D3	D2	D1	D0			
0	0	1	1	1	1	0	1	RLE	10 dB	-3 dBm
0	0	1	1	1	0	1	1	RLD	20 dB	-13 dBm
0	0	1	1	0	1	1	1	RLC	30 dB	-23 dBm
0	0	1	0	1	1	1	1	RLB	30 dB	-23 dBm
0	0	0	1	1	1	1	1	RLA	30 dB	-23 dBm

(4) Check that the output level falls to the appropriate level on the Spectrum Analyzer as each attenuator pad is selected.

16. The only electrical adjustment provided on AT1 board is a series of flags which may be used to adjust the calibration of each pad. In the 0 dB attenuation condition the attenuator has an insertion loss which is dependent upon the frequency selected. This insertion loss is compensated for by the ALC system on AC4. The flags are used to adjust the attenuation of each pad so that the difference between the attenuation of each pad being in or out is equal to the nominal attenuation of the pad at 1 GHz. To carry out comprehensive attenuator accuracy checks and realignment requires each pad to be separately set up using specialized measuring facilities and it is recommended that this be carried out only by the nearest Marconi Instruments agent or Service Division.

AF oscillator and AF level performance

Test equipment : items d, Digital frequency meter
g, Distortion factor meter
l, AF voltmeter

17. To test the frequency, distortion and output of the AF oscillator proceed as follows:-

(1) Connect the frequency meter to the AF OUTPUT socket of the instrument using a BNC type connector. Set the AF level to 1 V r.m.s. (normal switch-on condition).

(2) Select by successive presses of the AF OSC key each of the six pre-set modulation frequencies checking that the frequency indicated corresponds to the one selected ±5% and that each l.e.d. indicator on the instrument is lit as appropriate.

(3) Disconnect the frequency meter and connect the distortion factor meter. The measured distortion should not exceed 0.1% at 1 kHz.

(4) Select AF level on the 2018A to 1 V r.m.s. (default mode) and connect the AF voltmeter to the AF OUTPUT. Check that the level is accurate to within ±5%. Set the AF level for an output of 3 mV and check that level accuracy is within ±10%.

FM & ΦM deviation

Test equipment : item h, AM/FM modulation meter

18. To check the deviation accuracy proceed as follows:-

(1) Select CARRIER FREQ 100 MHZ, AF OSC 1 kHz, FM 100 kHz.

(2) Connect the 2305 to the RF OUTPUT socket and tune to the carrier frequency.

(3) Measure the f.m. deviation and check that it is within ±5% of the selected deviation. Now select ϕ.m., 10 radians and measure the deviation, check that the accuracy is within ±5%.

(4) Repeat the test for other deviation frequencies within the range of the instrument (1% of the carrier frequency in use).

FM tracking

Test equipment : item h, AM/FM modulation meter

19. To check the f.m. tracking proceed as follows:-

(1) Connect the modulation meter to the RF OUTPUT socket.

(2) Set to FM 100 kHz, AF OSC 1 kHz, RF LEVEL +1 dBm.

(3) Tune modulation meter to various carrier frequencies between 261 and 520 MHz and check that the output deviation remains at 100 kHz ±5%.

External f.m. modulation sensitivity (ALC)

Test equipment : item h, AM/FM modulation meter

20. The modulation level should remain reasonably constant for a given change in external modulation voltage and frequency. This sensitivity is checked as follows:

(1) Connect the test equipment as shown in Fig. 3.

(2) Select by successive presses of the AF OSC key each of the six

(2) Set 2018A to FM EXT, ALC ON, set the AF OUTPUT to give a 1 kHz, 1 V amplitude output and check that the f.m. deviation is the same as that for internal modulation.

(3) Vary the AF OUTPUT between 0.8 and 1.2 V and check that the deviation remains constant.

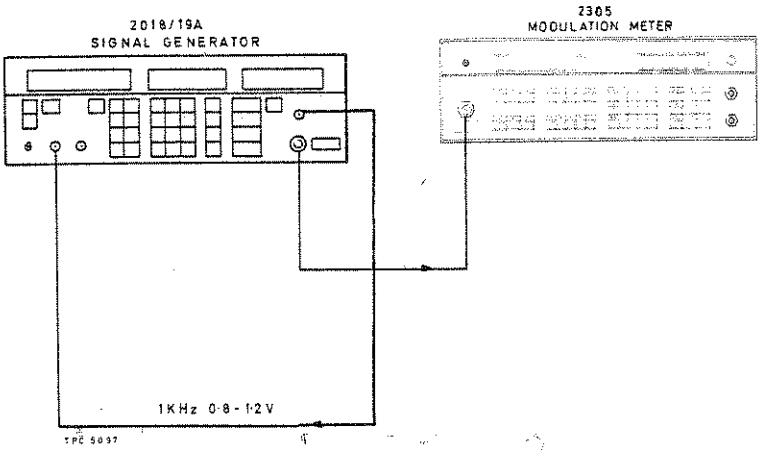


Fig. 3 Test gear arrangement for the checking of external modulation sensitivity

FM distortion

Test equipment : items g, Distortion factor meter
h, AM/FM modulation meter

21. To check the f.m. distortion proceed as follows:-

(1) Connect the test equipment as shown in Fig. 5. Select CARRIER FREQ 30 MHz, AF OSC 1 kHz, FM 200 kHz.

(2) Tune the modulation meter to the instrument and check that the distortion is not in excess of 3%.

(3) Repeat the test for other amounts of deviation. The distortion over the total range should not exceed 3% for deviations of up to 70% of the maximum available at any carrier frequency.

Aux f.m. input

Test equipment: item h, AM/FM modulation meter

22. To check the auxiliary f.m. input proceed as follows:-

(1) Select the 2018A to FM, 100 kHz, EXT with no input applied to the MOD INPUT socket.

(2) Set AF OUTPUT to 1 kHz and the level to 1 V r.m.s. Apply this signal to the 2018A, AUX FM INPUT socket.

(3) Check using the modulation meter that an output of 10 kHz ±10% deviation is obtained.

(4) Select 2018A to ΦM and repeat the test. The application of 1 V r.m.s. should result in an f.m. deviation in kHz equal to the phase deviation in radians shown in the modulation display.

AM depth

Test equipment : item h, AM/FM modulation meter

23. To check the a.m. depth proceed as follows:-

(1) Select CARRIER FREQ 100 MHz, AM 80%, AF OSC 1 kHz, RF LEVEL +7 dBm.

(2) Connect the modulation meter r.f. input to the 2018A RF OUTPUT socket.

(3) Check that the a.m. depth is accurate to within ±4% of depth setting +1%.

(4) Check the a.m. depth at other carrier frequencies up to 400 MHz.

24. If a modulation meter is not available the a.m. depth can be assessed by using an oscilloscope to measure the peak and trough values of the modulation envelope. The a.m. depth is then determined by

$$\text{AM depth } \% = \frac{Vp - Vt}{Vp + Vt} \times 100$$

where Vp and Vt are the measured peak-to-peak and trough-to-trough amplitudes respectively.

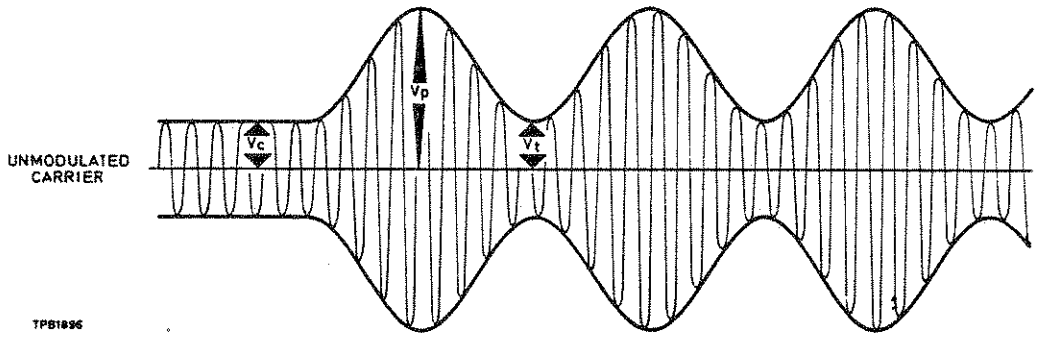


Fig. 4 Modulation depth measurement

AM distortion

Test equipment : items g, Distortion factor meter
h, AM/FM modulation meter

25. To check the internal a.m. distortion proceed as follows:-

(1) Connect the test equipment as shown in Fig. 5 below.

(2) Select CARRIER FREQ 100 MHz, AF OSC 1 kHz, AM 80%, RF LEVEL 7 dBm.

(3) Tune the modulation meter to the 100 MHz signal, checking that the distortion factor does not exceed an indicated 3% reading.

(4) Repeat the test with CARRIER FREQ set to 400 MHz.

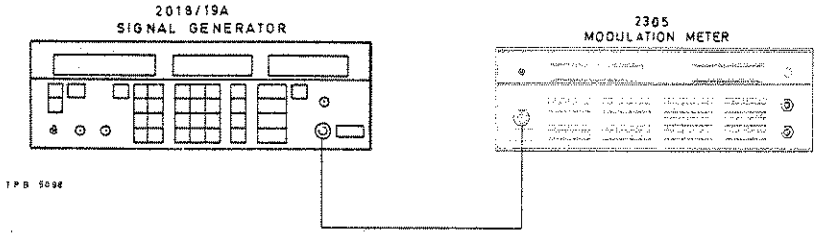


Fig. 5 Test gear arrangement for checking f.m. and a.m. distortion

VSWR (5 MHz to 1 GHz)

Test equipment : items m, Oscilloscope with dual trace capability
p, Sweep oscillator & RF plug-in unit
q, RHo-bridge with standard loads and calibrated mismatches

26. The impedance measurement may be carried out over almost all the frequency range of the instrument. Connect the test equipment as shown in Fig. 6 below.

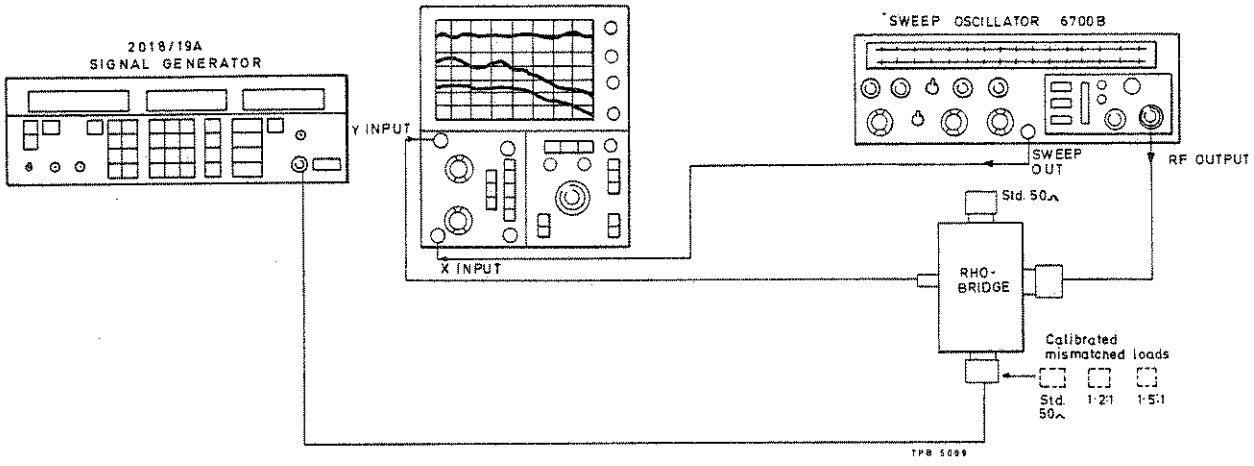


Fig. 6 Test gear arrangement to check v.s.w.r.

(1) Set the sweep oscillator to F1-F2 and sweep from 5 MHz to 520 MHz, insert standard 50 Ω loads into the rho-bridge and set datum point near the top of the oscilloscope display. Replace one 50 Ω with a 1.2:1 mismatched load and adjust the d.c. output of the rho-bridge so that the vertical deflection of the oscilloscope occupies 5 or 6 c.m.s. for the mismatch change. Using a chinagraph draw the pattern on the oscilloscope graticule.

(2) Remove the mismatched load and connect the 2018A, 2019A to the rho-bridge instead. Check that the v.s.w.r. does not exceed 1.2:1 with the RF LEVEL selected to -4 dBm or less.

(3) For 2019A Signal Generators repeat steps (1) and (2) sweeping this time from 5 MHz to 1 GHz and using the 1.5:1 mismatched load to check that the v.s.w.r. does not exceed 1.5:1.

Carrier harmonics and spurious signals

Test equipment : item k, Spectrum analyzer

27. To check the level of harmonics of the carrier frequency in a c.w. output proceed as follows:-

(1) Connect the spectrum analyzer to the RF OUTPUT socket and set the instrument to give a c.w. output at a convenient level below +7 dBm (1 V e.m.f.)

(2) Tune the instrument through its r.f. range and check that the amplitude of any harmonic is greater than 30 dB down on the fundamental for carrier frequencies from 80 kHz to 520 MHz, and 20 dB down on carrier frequencies 520 MHz to 1040 MHz (2019A).

Reverse power protection

Test equipment : items e, Multimeter
o, Variable d.c. power supply

28. Set the d.c. power supply to +5 V and apply this to the 2018A RF OUTPUT 50 Ω socket causing the RPP circuit to trip.

(1) An indication that the REV PWR LIMIT has been exceeded is given in the RF LEVEL display window, a further indication of trip is given by the RF LEVEL function keys integral l.e.d. This will continually flash until the reset is operated.

(2) Remove the +5 V source and check that there is no continuity between the 'N' type connector centre pin and earth (taking care not to damage the connector pin).

(3) Reset the RPP by pressing the RF LEVEL key and ensure that both trip indications are turned off. Set the d.c. power supply to -5 V and apply this again to the RF OUTPUT 50 Ω socket checking that the RPP once more trips. Remove the d.c. source and reset the RPP.

FAULT LOCATION

Introduction

29. The following section consists of fault finding procedures, charts and tests to aid identifying faults. To assist with fault finding it is advisable to study the description of the overall instrument contained in Chap. 4. The functions of the various boards are generally well defined and independent of each other as far as possible and the parameters of the signals exchanged between them are not critical. All boards/modules are interconnected by a variety of connectors. A useful method of confirming if board or module is faulty is to substitute the unit with a unit that is known to be good (e.g. from a spare working instrument). This can save considerable fault finding time.

30. When disconnecting an r.f. connection between two units ensure that the metal clad connector cannot accidentally cause short circuits on the printed boards and create additional faults. If any of the ribbon cable connectors are unplugged ensure that when they are reconnected they are correctly positioned since the connectors do not incorporate polarizing plugs. Layout of boards, plugs, sockets and connectors in the RF boxes are shown on Fig. 1a and 1b.

31. If any rectification work is carried out in areas containing chip components certain precautions should be taken. Always use solder containing 2% silver and use a high wattage temperature controlled soldering iron set to 315^0C (600^0F). The temperature controller should preferably directly sense and control the temperature of the soldering iron bit. The soldering iron tip should also be earthed in order to avoid potential damage to static sensitive devices. The chip resistors used in areas other than the 10 dB step attenuator have nickel barrier terminations and are virtually immune to

termination leaching problems. The ceramic chip capacitors used have palladium silver terminations that can dissolve or weaken in molten solder. If there is any possibility that a termination has been weakened during rectification work the suspect device should be replaced.

32. A useful technique for checking the soundness of chip capacitor terminations is to set the carrier frequency as low as applicable to the relevant circuit and then GENTLY tap the printed board (not the chip component) with a blunt non-metallic object (e.g. the handle of a screwdriver) checking the circuit for any intermittent level changes. Chip components can be mechanically damaged by rough handling or excessive flexing of the printed boards.

Use of second function 3

33. Second function 3 can be used as a diagnostic aid under certain circumstances. Its use requires that the microprocessor system and the keyboard is working normally. Second function 3 may then be used to send data to any specified latch. This will enable the operator to establish that the correct data is arriving at the input to the latch by using a storage oscilloscope triggered from the clock input of the latch and observing the data at the latch input as the latch is clocked. Each latch is identified on the circuit diagram by a data valid line and an address e.g. on AC5 the address of the D-A converter, IC4, is given as A7L0. The data valid line is 7 and the latch address is 00 (2 digits are required L0 implies 00, L1 implies 01 etc.). Data can be sent to this latch by pressing the keys "SECOND FUNCT", "3", followed by the data valid line "7" and the latch address "0", "0", (2 digits). The data valid line will be displayed in the modulation display and the address is displayed in the r.f. level display. This is followed by entering a string eight binary digits (1's and 0's) corresponding to the data to be sent (D7 first). Pressing the store key will cause the microprocessor to send the data to the specified latch. If the data that is being sent needs to be sent again pressing the STORE key again will send the same data. If the data is to be modified this can be accomplished by entering a new string of data and then pressing the STORE key again.

34. Where data is to be sent to the 10 bit D-A type AD7522 the data has to be sent in two bytes. The least significant eight digits are sent first to one latch address (as specified in the control data information), this is stored in a buffer (inside the D-A chip). A new latch address is then entered corresponding to the most significant bits, followed by the required binary data. On pressing the STORE key this data is sent to the D-A and the D-A in turn is set to data specified by the whole 10 bit number. Any data sent via second function 3 remains in the receiving latch until one of the orange function keys is pressed. The microprocessor will then overwrite any data sent and restore the instrument to normal operation.

Maintenance kit

35. The maintenance kit contains the following items which may be used for fault finding and servicing.

(1) RF lead part number 43129-835R. A 20 cm long SMC female to SMC male connector assembly. Intended to be used when the upper r.f. box is raised for servicing. This lead enables the operator to reconnect the free end of the semi-rigid cable assembly PLAV to PLAX (which connects the synthesizer output from the upper r.f. box to the lower r.f. box) to SKAV in the upper r.f. box.

(2) RF lead part number 43129-834C. A 70 cm SMC to BNC lead to enable the output from SMC connectors to be monitored.

(3) RF lead number 43129-836B. A 70 cm SMB to BNC lead to enable the output from SMB connectors to be monitored.

(4) Connector assembly part number 54129-833M. A 70 cm crimp to BNC lead to enable the output from a p.c.b. to be monitored where the output is on .025 in square wrap posts.

(5) Adapter part number 44828-753H. A 50 to 200 Ω adapter which can be used in conjunction with 43129-833 to monitor a 200 Ω output from a board on .025 in square wrap posts. The adapter introduces a 12 dB insertion loss.

(6) LCD extraction tool, part number 46883-530G.

(7) LCD insertion tool, part number 46883-529S.

FAULT FINDING TO BOARD LEVEL

36. The following section describes fault finding routines and algorithms which may be used to help diagnose faults down to board level. The fault finding routines start from a generalized fault condition and guide the operator to the most likely area of the fault. The generalized fault conditions used as a starting point are as follows:

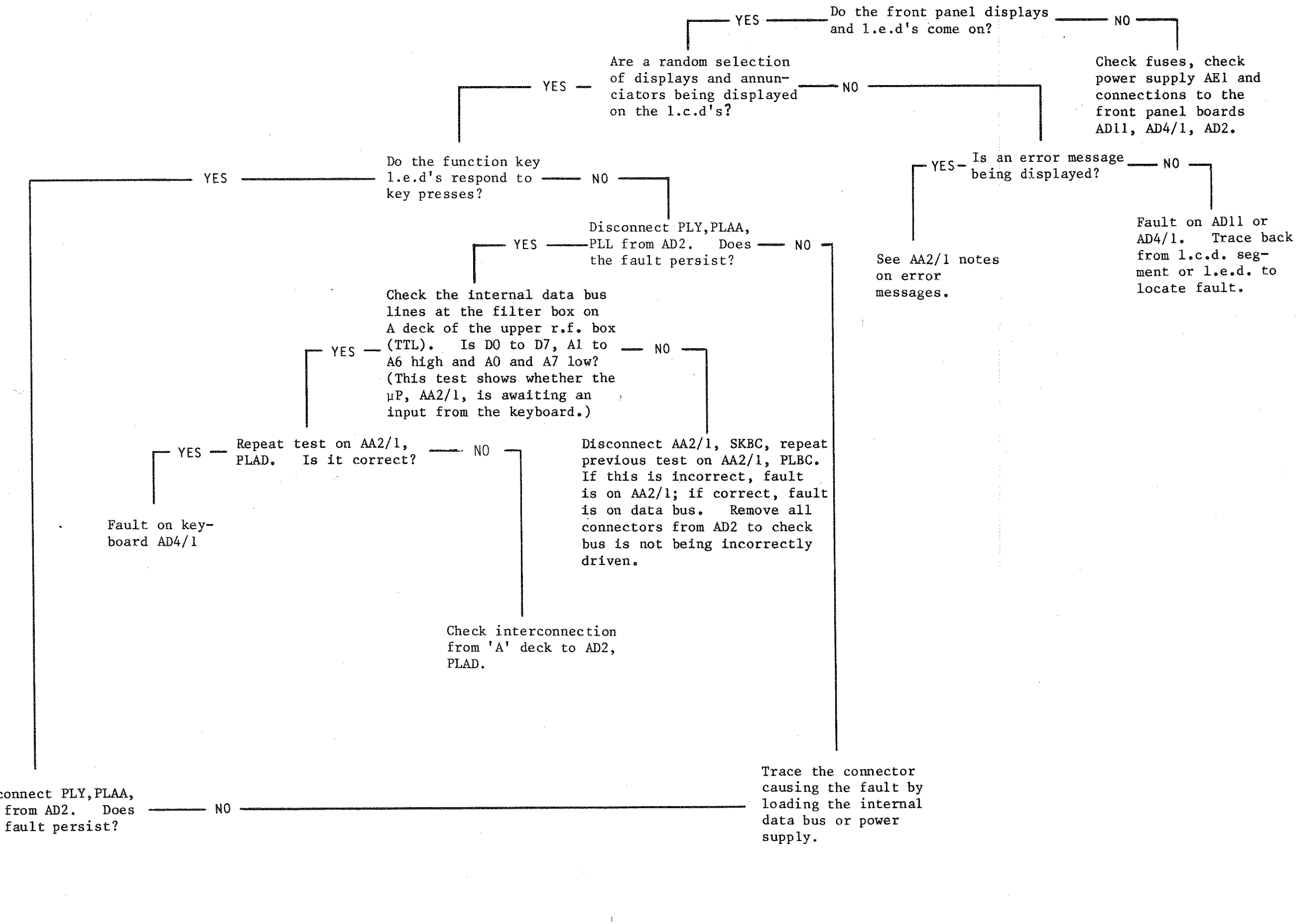
(a) Front panel failure
(b) Output frequency error
(c) Output r.f. level error
(d) Carrier harmonic problem
(e) AM fault
(f) FM or ϕ.m. fault
(g) Residual f.m. problems
(h) RPP failure

Choose the description that most closely describes the fault condition and use the fault finding guide to establish the area of the fault. Before using the fault finding tables read the notes that accompany the tables.

Front panel failure

37. A chart to aid fault finding a front panel failure is given in Table 5. A front panel failure is defined as a fault in which the keyboard or the display is not operating correctly. One of the first objectives is to establish if the display or keyboard is causing the fault or whether the microprocessor system is not operating. If the microprocessor system is functioning but has a memory fault an error message will be displayed. This appears as two numerals in the centre of the carrier frequency display with minus signs on either side. Error number 10 is displayed in the event of a PROM error. Errors 12,13 or 14 indicate a RAM error. Error numbers 18 or 24 indicate an EAROM read or write failure, 06 an EAROM data checksum failure and 17 an invalid stored data recall. A complete list of all error messages are given in Chap. 3 of the Operating Manual Vol. 1. In the event of a microprocessor failure in which the microprocessor cannot run the checksum no error message will be displayed. In this case testing to see if the microprocessor board is waiting for a keyboard press should indicate if the microprocessor program is running.

TABLE 5 FRONT PANEL FAILURE



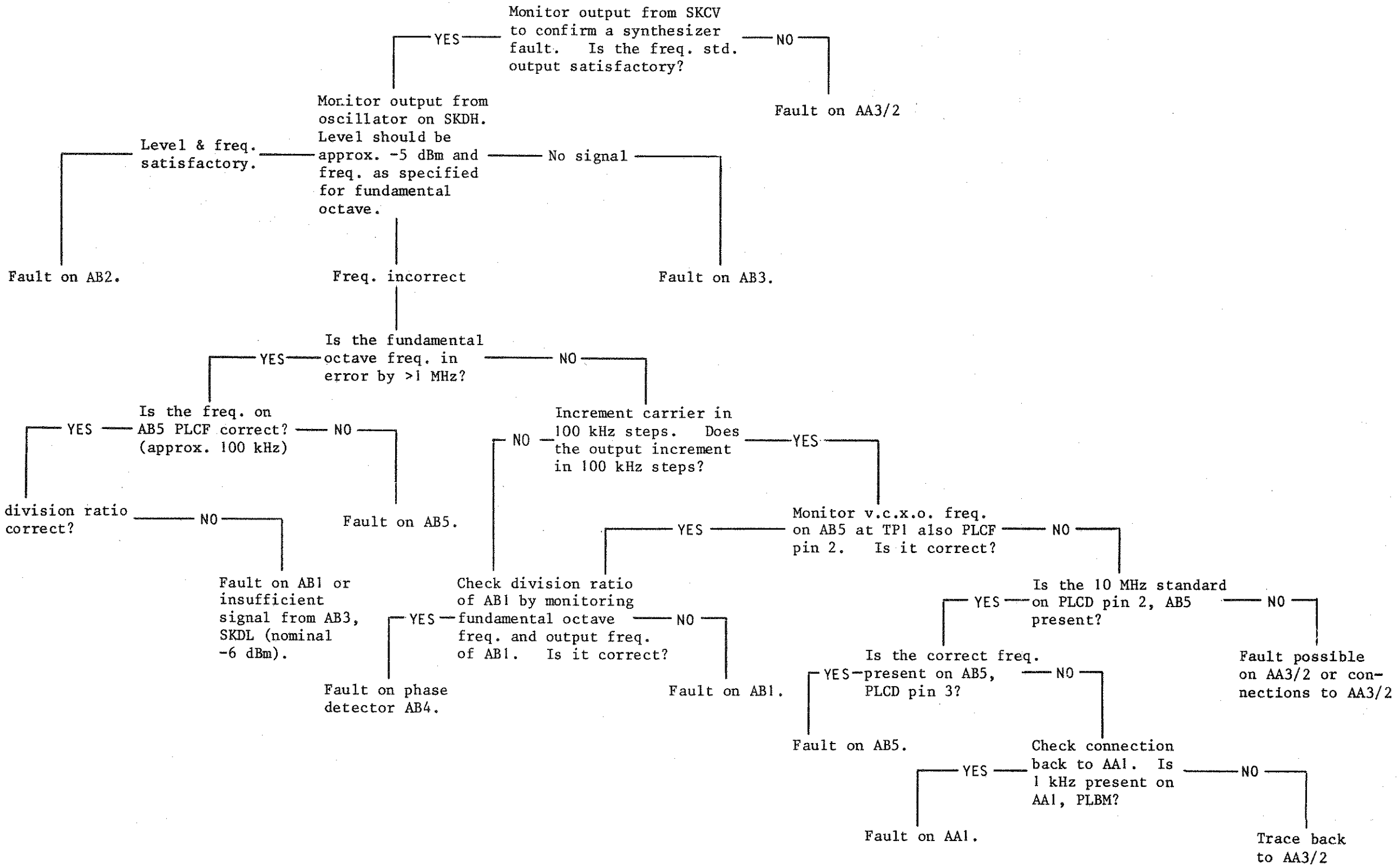
Output frequency error

38. A chart to aid fault finding an output frequency error is given in Table 6. An output frequency error is defined as a fault in which the output carrier frequency, when measured using a frequency counter operating from the same frequency standard as the instrument, indicates that the output frequency differs from the value set.

39. If the instrument has been set to operate from an external frequency standard, ensure that an external standard of 10 MHz at 1 V r.m.s. across 50 Ω is applied to the external standard input on the rear panel. Since the output frequency is synthesized in the upper r.f. box any frequency synthesis fault is likely to be in the upper r.f. box with the exception of frequencies below 3.03125 MHz. Faults confined to this b.f.o. band are covered in the section relating to r.f. level faults. For ease of fault finding the r.f. output from the SMC connector, SKAV, at the rear of the upper r.f. box should be used to monitor the output frequency. The output level from this connector should be approximately 0 dBm but its absolute level and flatness is not critical. The waveform is nominally a square wave and so it has a high harmonic content. Certain frequency counters and modulation analyzers may be prone to acquiring harmonic frequencies of the output.

40. The carrier frequency is synthesized over the frequency range 260 to 520 MHz (the fundamental octave) and then divided down by factors of two. If the fault exists on the fundamental octave it is always easier to locate the fault with the instrument set on this range, since it is easier to calculate the intermediate frequencies used to generate the output. Before starting to fault find, read and understand the description of the synthesizer given in Chap. 4 since it may be necessary to calculate the intermediate frequencies very precisely in order to locate the fault. When dealing with small frequency errors it is advisable to operate the counter measuring the output frequency from the same frequency standard as the instrument.

TABLE 6 OUTPUT FREQUENCY ERROR



RF level fault

41. A chart to aid fault finding an r.f. level fault is given in Table 7. An r.f. level fault is defined as a failure which results in the r.f. level being out of specification but the carrier frequency is correct and the output signal is not unduly distorted. In assessing if the r.f. level is out of specification the r.f. offset facility should be switched off (second function 7). It is also assumed that the error is such that the instrument does not just require recalibrating.

42. The r.f. level accuracy is set up using second function 7. If it is found that the instrument is out of calibration but can be recalibrated using second function 7 it is possible that the fault is due to the EAROM store on AA2/1 not permanently storing data (see fault finding AA2/1). Usually (but not always) such faults will also be accompanied by f.m. tracking faults and failure to store instrument settings, r.f. level units or GPIB address. RF level errors are only likely to originate in the lower r.f. box, the attenuator module, or the associated control systems and connectors. The lower r.f. box derives its input from the upper r.f. box via SKAW as a nominal 0 dBm square ware. Because the Amplitude Modulator AC5 acts as a signal limiter the input level to AC5 is not critical.

43. For carrier frequencies above 32.5 MHz the square wave output from AC5 is routed through a low-pass filter bank on AC3/13. The filters convert the signal into a sine wave at SKCS of AC3/13. Frequencies above 520 MHz are generated by a frequency doubler on AC13 (20919A only) and also appear on SKCS of AC13. The signal then goes to AC4 via PLCS and is amplified by a variable gain amplifier before going onto the output stages of AC4. RF level faults which are confined to frequencies above 32.5 MHz are most likely to arise because of faults in the filters of AC3/13 or the r.f. amplifiers on AC4.

44. Frequencies below 32.5 MHz are routed through a bank of low-pass filters on AC3/13. If the output frequency is above 2.03125 MHz it is then routed to AC2 via PLCT and then to a variable gain amplifier on AC4. If the required output frequency is below 2.03125 MHz a 10 MHz to 12.03125 MHz signal is routed to AC2 via PLCW in order to be mixed with 10 MHz to produce the low frequency signal. RF level faults which are confined to frequencies below 32.5 MHz can therefore originate anywhere along this signal path. It should be noted that much of this low frequency signal path is operating in a 200 Ω system and not the more usual 50 Ω system. For this reason when using a 500 Ω probe to fault find along the signal path some allowance must be made for the loading effects of the probe. If it is required to monitor the output from PLCT of AC3/13 with a 50 Ω spectrum analyzer or modulation meter with SKCT disconnected then a series 150 Ω resistor should be used (at the SKCT end) to convert the load into 200 Ω and due allowance made for the resulting insertion loss of 12 dB.

45. RF level faults can be caused if the amplifier system has too much or too little gain and the a.l.c. is therefore unable to control the signal level correctly. The 2018A has been designed to have a considerable gain margin and a typical instrument will have a margin of 8 dB at its worst frequency. The gain margin can be checked if necessary by first setting the output level to 7 dBm and then shorting the junction of R44 and R45 of AC5 to ground using a screwdriver or similar implement. The output level should rise by at least 3 dB (typically a minimum of 8 dB). The signal chain can then be tested for having too much gain by setting the output level to -2.9 dBm and then shorting the junction of R87 and R90 on AC4 to ground. The output level should fall by at least 4 dB.

TABLE 7 RF LEVEL FAULT

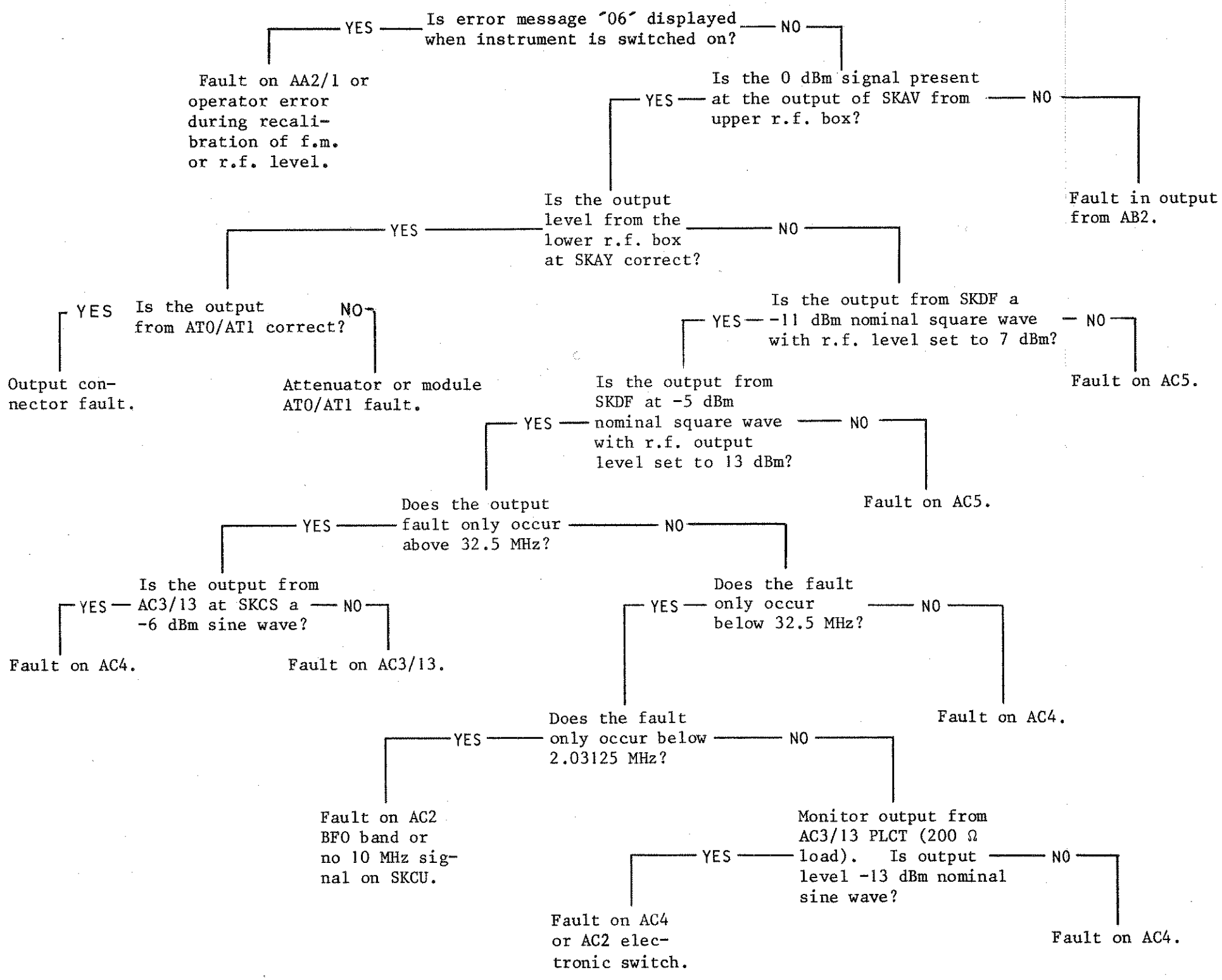
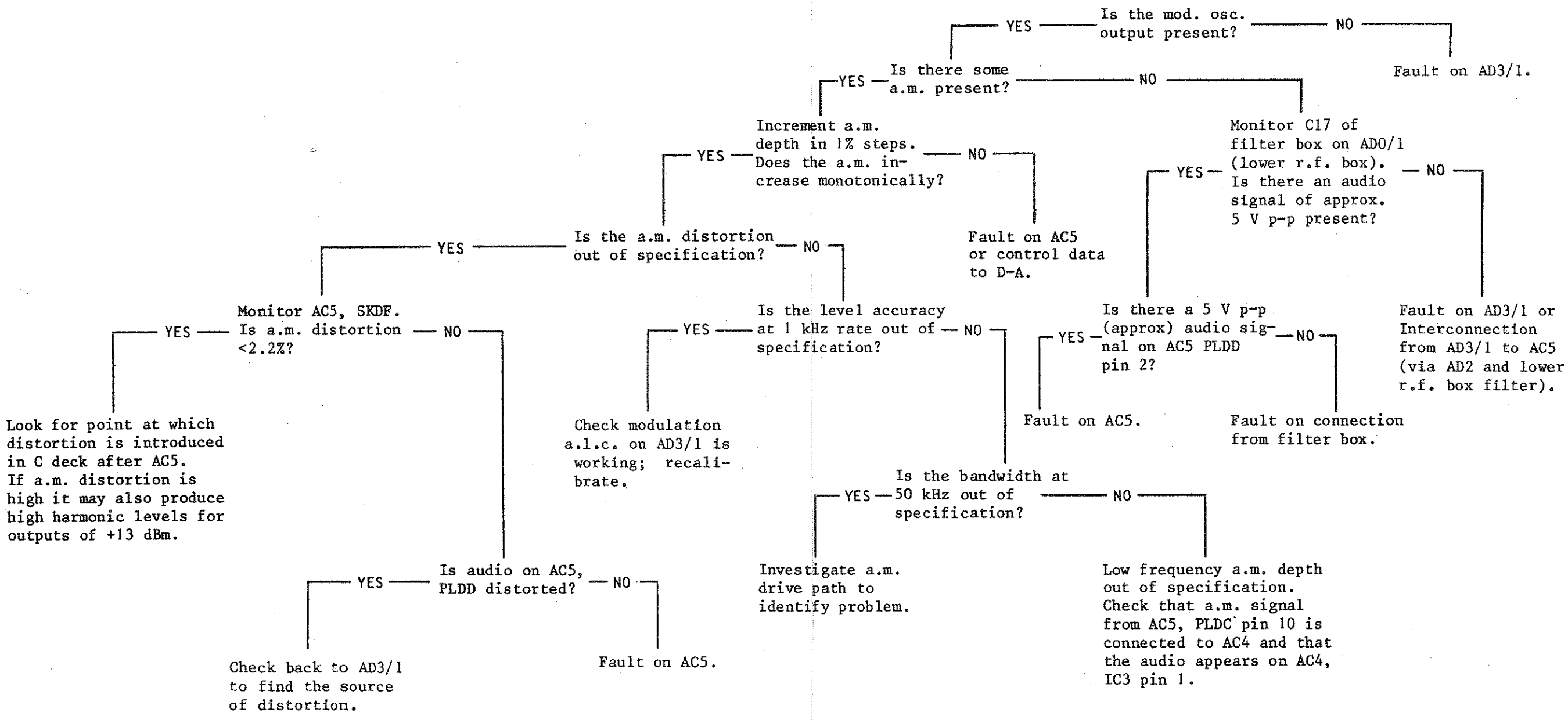


TABLE 8 AM FAULT



Harmonic distortion fault

46. Investigating harmonic distortion faults is usually a straightforward problem so a fault finding algorithm has not been provided. Until the signal arrives on AC3/13 its harmonic content has little effect on the performance of the instrument. On AC3/13 the nominal square wave is filtered by a bank of low-pass filters which converts the signal into a sine wave.

47. For problems above 32.5 MHz monitor the nominal -6 dBm signal from SKCS of AC3/13. If the harmonic content is high the fault is on AC3/13. If the harmonics are -40 dBc or better the fault is on AC4. For problems below 32.5 MHz trace the signal path from the filters on AC3/13 to AC2 and AC4 and identify where the harmonic problems start. Much of the low frequency channel operates in a 200 Ω transmission system so care must be taken not to load the system with less than 500 Ω when probing the signal path. The 50 to 200 Ω adapter in the maintenance kit can be used to break into the signal path.

AM fault

48. An a.m. fault finding algorithm is given in Table 8. It is assumed that the output frequency is correct and the r.f. level accuracy and harmonic distortion is in specification. The fault finding algorithm first establishes if the fault is inside the lower r.f. box or is on AD2 or AD3/1.

49. When monitoring the output from SKDF AC5 it should be remembered that the output signal is a square wave and the modulation meter used must be capable of rejecting the high level of carrier harmonics present. If the modulation meter is automatically tuned care should be taken to ensure that the instrument tunes to the fundamental and not a harmonic.

FM or ΦM fault

50. An f.m. or ϕ.m. fault finding algorithm is given in Table 10. The f.m. drive system is complicated by the requirement to provide f.m. tracking and range scaling to account for the division or multiplication by two of the fundamental octave as well as providing fine control of the deviation. Most of the algorithm is therefore devoted to identifying which part of the control system is at fault. The ϕ.m. and f.m. paths are common with the exception of a differentiator circuit on AD3/1. The control system will be set to the same conditions as ϕ.m. (except the differentiator is in circuit) if f.m. is set to a deviation given by:

$$FM = \phi.m.\ dev. \times 10\ kHz$$

e.g. 10 radians of ϕ.m. uses the same control settings as 100 kHz f.m. at any given carrier frequency.

51. Information on the use of second function 8 is given in the calibration section. In addition second function 3 can be used to check that the various digital-to-analogue converters are working. A digital a.c. voltmeter can be used to check the input and output levels of a D-A converter and hence establish if the gain of the converter is correct. If the divide-by-two system dividing the f.m. deviation is at fault it should be remembered that the division is accomplished using a divide-by-four system on AB2 as well as a divide-by-two, IC28, on AD3/1.

52. As an aid to diagnosing a fault in the f.m. tracking store Table 9 gives a list of the carrier frequencies used as f.m. tracking points together with the typical values of f.m. tracking data. Typically instruments will be within approximately 20% of the listed values.

TABLE 9 TYPICAL FM TRACKING DATA

OSC 1		OSC 2		OSC 3		OSC 4	
Frequency	Data	Frequency	Data	Frequency	Data	Frequency	Date
260.00001	164	309.00001	157	368.00001	136	437.00001	113
262.45	182	311.95	166	371.45	142	441.15	118
264.9	186	314.9	180	374.9	150	445.3	125
267.35	183	317.85	178	378.35	150	449.45	125
269.8	187	320.8	182	381.8	151	453.6	127
272.25	189	323.75	183	385.25	150	457.75	127
274.7	189	326.7	183	388.7	150	461.9	127
277.15	189	329.65	182	392.15	145	466.05	123
279.6	189	332.6	174	395.6	142	470.2	123
282.05	187	335.55	169	399.05	142	474.35	117
284.5	182	338.5	171	402.5	134	478.5	117
286.95	183	341.45	167	405.95	131	482.65	112
289.4	180	344.4	157	409.4	131	486.8	113
291.85	178	347.35	159	412.85	125	490.95	110
294.3	175	350.3	155	416.3	125	495.1	107
296.75	175	353.25	150	419.75	123	499.25	107
299.2	175	356.2	151	423.2	121	503.4	106
301.65	175	359.15	150	426.65	121	507.55	106
304.1	176	362.1	152	430.1	121	511.7	106
306.55	175	365.05	155	433.35	121	515.85	109
309	177	368	154	437	121	520.0	108

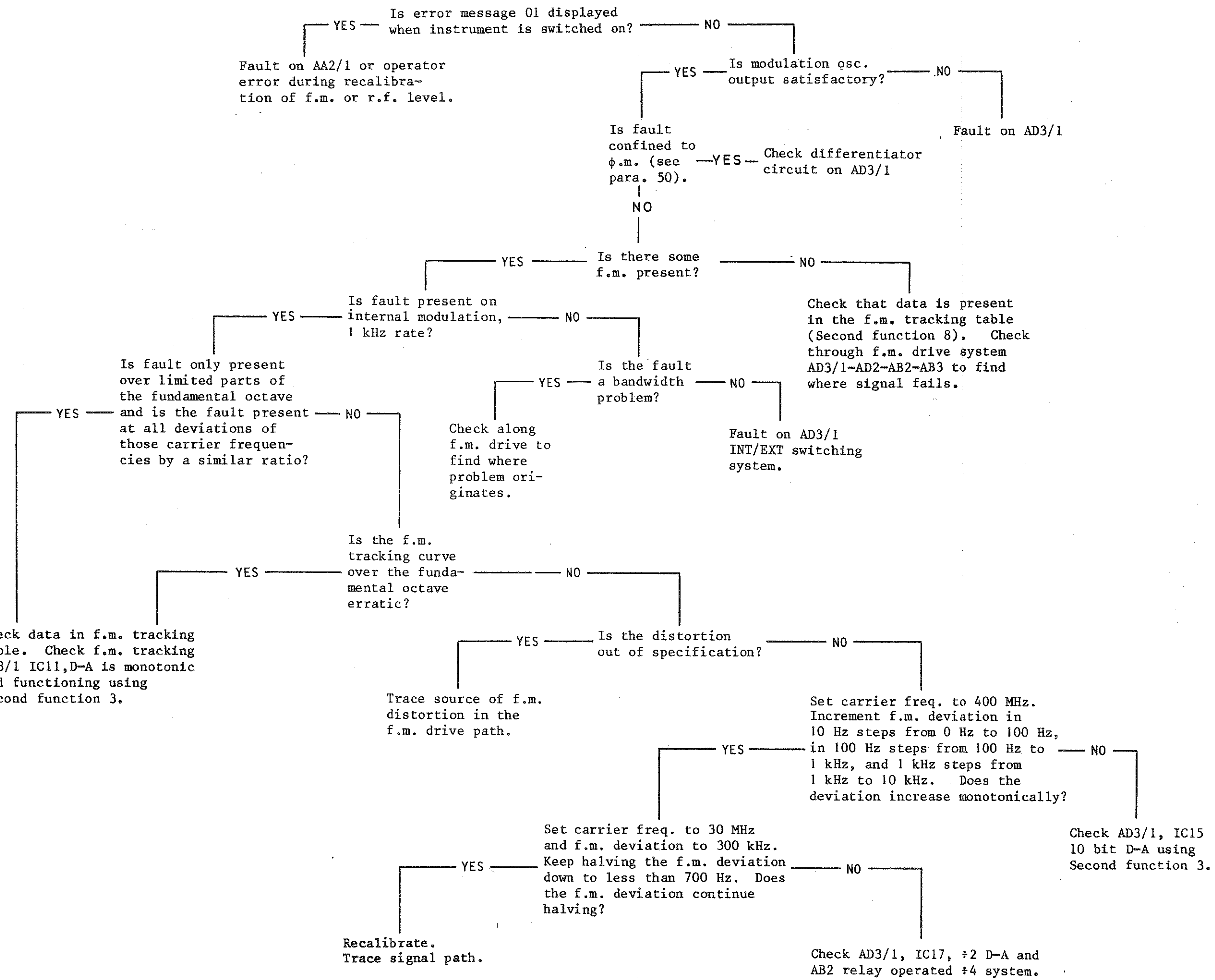


TABLE 10 FM or ΦM FAULT

Residual f.m. problems

53. This section provides guidance for identifying the source of residual f.m. problems. No fault finding algorithm is provided. Residual f.m. problems are usually the result of spurious modulation of the oscillators in the upper r.f. box. The internal frequency standard should be checked first for spurious modulation. The most sensitive oscillator is the bank of four oscillators on AB3 (only one is in use at any given time) whose varactor diode sensitivity can be up to 10 MHz/V. Even very low level signals can cause spurious signals.

54. If the spurious signal is related to the mains frequency check that the d.c. power supplies do not have high levels of ripple. Typically the +5 V supply has 100 µV of 100 Hz (or 120 Hz) and the +15, -15 and +24 V supplies have 30 µV or less. Check that the regulators on AB4 (+11.5 and -11.2) are within 12% of their nominal value. Check that the +5 regulator IC1 on AA0 is operating correctly. Noisy +11.5 V or -11.2 V power supplies can cause residual f.m. problems.

55. Instability in a phase locked loop can cause coherent spurious signals to be generated. This can be checked by observing the varactor diode voltages on AA1, AB5 and AB4 with an a.c. coupled oscilloscope and checking for coherent signals. Phase locked loop instability will normally produce significant signal excursions while maintaining the average frequency of the loop at the correct frequency. It should be noted that the input to the oscilloscope must be a.c. coupled since the loading of even quite high impedances (10 MΩ) can result in the phase detector having to produce a significant output at the phase detector rate.

56. The output phase locked loop can be made unstable in the f.m. off mode if the loop filter control lines on AB4 and AB3 are not operating correctly. A similar problem can exist in the f.m. mode but normally one of the modes will operate if the fault is due to the loop filter control lines. Phase locked loop instability, where the average output frequency is correct, but the frequency is very unstable, is most likely to be caused by faulty components in the analogue part of the phase detector where the output current pulses are directed to the loop filter and the resulting d.c. is fed to the varactor diodes.

57. If the amount of residual f.m. is small (though not out of specification) and no obvious fault can be found the problem may originate in AB3. More fault finding data for AB3 is given in the board level fault finding section.

RPP failure

58. The RPP system uses a reed to protect the output of the attenuator from the accidental application of reverse power (d.c. or r.f. power). The RPP can be tested by applying ±5 V d.c. to the r.f. output connector. If the l.e.d. in the RF LEVEL key flashes and the REV PWR LIMIT annunciator is set but the RPP relay does not go open circuit, first check to see if the yellow l.e.d. D10, on AT2 is on. If it is on this indicates that although the detector has alerted the keyboard the RPP delay has been left on and the fault is on AT2. If D10, AT2 is not on check that the voltage on C1, AT0/AT1 is at approximately 0 V. If it is, relay assembly RLF, AT1 has been damaged.

59. If applying ±5 V to the r.f. output fails to produce a front panel response and the RPP relay remains closed check that approximately 0.75 V is present on C2, AT0/AT1 if +5 V has been applied, or that -0.75 V appears on C3, AT0/AT1 if -5 V is applied. If this voltage is not present the fault is on AT1 and if the voltage is present the fault is on AT2.

60. If the front panel does not respond but the RPP relay is open circuit this will indicate that the control line from AT2 to the keyboard AD4/1 is not operating the electronic switch on AD4/1 and the fault can be traced from AT2 to AD4/1 via AD2.

61. If the front panel responds as soon as the instrument is switched on and without reverse power being applied, this indicates that there is a fault in the detector system on AT0/AT1 or the RPP is not being reset when the instrument is switched on. The RPP reset line can be traced using second function 3. It should be noted that if AD3/1 is not plugged into its edge connector, the RPP will not be reset because the attenuator address latch (A6L10) is decoded on AD3/1.

BOARD LEVEL FAULT FINDING

62. The following section gives guidance on fault finding at board level. Where appropriate, guidance is given on how to fault find on the printed board; the control data generated by the microprocessor; information on the waveforms that can be expected at various points on the circuit, and how to realign the board before recalibrating the instrument.

AA1 : LSD loop

63. AA1 includes a complete phase locked loop and an additional variable ratio divider (VRD). Phase locked loop faults can be traced by checking each element in the system i.e., the oscillator, the VRD and the phase detector.

64. First check that the oscillator is working (not necessarily at the correct frequency) by monitoring TP1. In a functioning loop, its frequency will be between 10 and 19.999 MHz. A fault elsewhere on the board may result in the frequency being incorrect in which case the voltage on TP2 should be checked to see if it is giving the expected varactor voltage for the observed oscillator frequency. If the frequency on TP1 is correct the fault will be the VRD formed by IC10 - IC17 and fault finding can be carried out in the same way as when fault finding on the phase locked loop's VRD.

65. If the oscillator is functioning correctly but is not at the correct frequency, check the division ratio of the VRD by measuring its input and output frequency and calculating the ratio. If the VRD is at fault check that the data latched by IC8 and IC9 is correct. If no fault is found check that each of the counters IC3 to 7 have clock input pulses on pin 2 and that the QA and QD outputs (pins 14 and 11) have pulses which reduce in frequency by factors of approximately 10 as the signal progresses down the counter chain. Failure of a device to produce these pulses would indicate that either the RESET line is low (fault IC16) the relevant IC is faulty or there is a fault with the carry out pulse from pin 15 of the previous counter IC.

66. If the VRD is not at fault check the phase detector circuit for faults. As a further aid to fault finding the mini-jump linking TP3,4 may be removed and a variable positive voltage applied to TP4 in order to directly control

the oscillator frequency. If the oscillator frequency (on TP1) is adjusted just above the correct frequency, TP2 should be pulled down to 0.2 V by the phase detector. If the frequency is pulled too low then TP2 should be driven to 14.8 V by the phase detector.

67. Control data AA1. To calculate the control data for AA1 first calculate the carrier frequency generated by AB3 using the block diagram. This will equal the output frequency if it is between 260.00001 MHz and 520 MHz. Consider the frequency to be ABC.DEFGH MHz. Data sent is then as shown in Table 11 below.

TABLE 11 CONTROL DATA AA1

Latch address	IC numbers	Data lines	Data
A6L0	IC11	D0-D3	Second m.s.b. of (10000 - ABCD)
		D4-D7	m.s.b. of (10000 - ABCD)
A6L1	IC10	D0-D3	l.s.b. of (10000 - ABCD)
	IC10	D4-D7	Second l.s.b. of (10000 - ABCD)
A6L2	IC9	D0-D3	Nines complement of F
	IC9	D4-D7	Nines complement of E
A6L2	IC9	D0-D3	Nines complement of F
	IC8	D4-D7	Nines complement of G

68. Test data AA1

TP1 — Output from l.s.d. oscillator. Frequency between 10 and 20 MHz. Waveform amplitude is typically 5 V p-p at 10 MHz and 4 V p-p at 19.999 MHz.

TP2 — Varactor voltage for l.s.d. oscillator. DC level 2.28 V at 10 MHz, 10.1 V at 19.999 MHz.

TP3,4 — Mini jump may be removed and a d.c. voltage applied to TP4 to control the l.s.d. oscillator while fault finding.

TP5,6,7,8 — Used by Marconi Instruments Autotest only.

IC16, pin 9 — Normally high with a 50 ns pulse to low state with a p.r.f. of 1 kHz if the l.s.d. is working. An additional very narrow pulse may be present 400 to 800 ns previous to this pulse - this is not a fault.

IC7, pin 14 — Pulse waveform with p.r.f. of 1 kHz. Mark to space ratio is variable, being low for 100 ns when the l.s.d. is at 10 MHz and approximately a square wave.

IC1, pin 11 — Pulse waveform 1 kHz p.r.f.

IC1, pin 5 When phase locked normally high with low 60 ns pulses at a p.r.f. of 1 kHz. If l.s.d. loop oscillator frequency is high (not phase locked) it should produce wider pulses to try to pull the oscillator frequency lower.

IC1, pin 8 When phase locked normally low with high 50 ns pulses at a p.r.f. of 1 kHz. If the l.s.d. loop oscillator frequency is low (not phase locked) it should produce wider pulses to try to pull the oscillator frequency higher.

AA2/1 Microprocessor system

69. The board AA2/1 contains the microprocessor and its peripheral circuits and an interconnection system for distributing control data. All the l.s.i. circuits are mounted in IC sockets to assist fault finding. At switch-on the microprocessor carries out a series of tests on its RAM, PROM and stored data (EAROM). If an error is found an error message is displayed in the carrier frequency display. The error messages are indicated in the centre of the carrier frequency window as a two digit number as shown below. The following table gives details of error messages available.

TABLE 12 ERROR MESSAGES AA2/1

Error		
10	PROM	Checksum error - will not run
06	CAL	Data checksum - will reset
12	RAM	IC18 checksum - will not run
13	RAM	IC12 checksum - will not run
14	RAM	Both checksums - will not run
01	RPP	Tripped - "REV PWR" annunciator
16	Illegal store number	
17	Invalid data recall (checksum on each individual instrument store)	
18	EAROM write failure - failed to store correctly	
19	Invalid first character	
20	Invalid second character	
03	Invalid GPIB character	
21	Incomplete character pair	
04	Option not fitted	

(1) Errors 10, 12, 13, 14 indicate fundamental faults are present in the instrument and the microprocessor will not operate any further instructions.

(2) Error 06 indicates that the calibration data stored in the EAROM, IC14, is in error. The instrument will start operating if any front panel key is pressed.

(3) Errors 17,18 indicate that the Store/Recall facility is inoperative. Error 18 indicates that store is not functioning at all and 17 indicates that the stored data has been corrupted. The instrument operates normally with the exception of Store and Recall operations.

(4) Errors 19,20,03,21 are GPIB errors, usually resulting from invalid GPIB instructions. The error message is displayed on the carrier frequency window and is cleared by the next GPIB character.

70. The manufacturer of the EAROM store guarantees a retention time of greater than 10 years for the first 10,000 write/erase cycles so loss of valid data in the non-volatile store is usually due to hardware faults. Failure to display an error message does not eliminate RAM or PROM faults if the microprocessor is unable to run the system. In the event that the instrument fails to respond at all and no obvious fault can be found (e.g. ICs running hot) first check the voltage on IC9 pin 36, if it is a logic low (or below 2.5 V) this normally indicates that the EAROM protection circuit around IC19 has stopped the microprocessor. This will happen if the 5 V supply drops below the 4.5 V reference on TP15. The EAROM protection circuit can be tested by monitoring IC9 pin 36. If R8 is adjusted so that TP15 is more positive then the 5 V supply pin 36 of IC9 should be forced low. Return R8 to setting required to generate 4.5 V on TP15. Toggle the supply on/off switch rapidly. The microprocessor should restart again after a few seconds. Monitor TP16 with an oscilloscope. On switching the instrument off the voltage on TP16 should fall within a few tens of ms to less than 5 V. If the microprocessor board is replaced the calibration and stored data may be transferred from the old to the new board provided that none of the stored data has been corrupted.

71. Test data AA2/1

IC9 pin 37	Microprocessor clock 3.072 MHz
TP15	+4.5 V d.c. (set by R8)
TP16	+21 V d.c.

AA3/2 : Frequency standard

72. Control data AA3/2. The control data for AA3/2 is latched on AA2/1 as shown in Table 13 below.

73. Test data AA3/2

IC1, pin 3	3 V p-p 10 MHz standard.
IC7, pin 4	Low for INT STD. High for EXT STD.
IC5, pin 7	On EXT STD t.t.l. level 1 MHz signal.
IC5, pin 2	TTL level 1 MHz signal.

IC8, pin 1	TTL level 100 kHz signal.
IC8, pin 9	TTL level 1 kHz signal.
IC7, pin 13	For carrier frequencies from 2.03126 MHz logic low. For carrier frequencies up to 2.03125 MHz t.t.l. level 10 MHz signal.
R1, C2 junction	DC voltage between 0 and 5 V.
PLBP, pin 4	Nominal sine wave 0.6 V p-p with spurious amplitude modulation caused by the v.c.x.o. frequency on AB5.

TABLE 13 CONTROL DATA AA3/2

Latch address and data line	PLBP pin no.	Data
A6L5 D4	7	Logic high if INT STD. low if EXT STD.
A6L5 D6	10	Logic high if output frequency is >2.03125 MHz
A6L5 D7	6	Logic high if 10 MHz STD. low if 1 MHz STD.

AB1 : Output v.r.d.

74. If a fault on AB1 has been diagnosed first check that the r.f. voltage on the collector of TR1 is correct. If the fault results in there being no output from PLBU this normally indicates a catastrophic failure of one of the components in the divider chain. Use an oscilloscope to check that there is a clock pulse on TP1. If there is not this indicates a fault in one of the dividers IC1, IC2 or the buffer stage IC3a. Then use the oscilloscope to check that the QA and QD outputs of IC7,8,9 are toggling. If none are toggling check that TP3 is generally high. If it is not, this indicates a fault in the subsidiary counter system formed by IC11,12. If TP3 is high and none of the ICs toggle the fault is likely to be in IC7.

75. If the v.r.d. is functioning and the division ratio is controllable (though the ratio is wrong) check that the correct data has been latched on IC4,5. If the correct division ratio seems to be related to one decade of the division ratio only, replace the respective counter (IC6 for 100 kHz decade, IC7 for 1 MHz decade, IC8 for 10 MHz decade and IC9 for 100 MHz decade of the fundamental frequency). When the 100 kHz decade (IC6) is suspected it is possible that a fault exists in the 10 or 11 divider, IC2, or its associated control circuit.

76. If the v.r.d. produces an output signal but the division ratio is not controllable this indicates a fault in one of the devices that reset the

counter chain. Check that all the inputs to IC12 are toggling and that periodically there is an output pulse on TP4 which enables the subsidiary counter IC11.

77. Control data AB1. AB1 uses two latch addresses to receive control data. These addresses are identical with two addresses on AA1. As with AA1 assume the output frequency from AB3 is of the form ABC.DEFGH MHz where ABCD is between 2600 and 5200. The data sent to AB1 is then as shown in Table 14 below.

TABLE 14 CONTROL DATA AB1

Address	IC No.	Data lines	Data
A6L0	IC5	D4 - D7 D0 - D3	MSB of (10000 - ABCD) Second m.s.b. of (10000 - ABCD)
A6L1	IC4	D4 - D7	Third m.s.b. of (10000 - ABCD) LSB of (10000 - ABCD)

78. Test data AB1

TR1 collector	0 dBm signal at fundamental frequency.
TP1	TTL level signal. Frequency approx. 13 to 26 MHz according to fundamental frequency set.
TP2	TTL level. Normally high with a low pulse of between 0 ns (non-existent) and 750 ns according to the fundamental frequency set and the setting of the l.s.d. (100 kHz decade of fundamental freq.) of v.r.d. setting.
TP3	TTL level. Normally high with low pulse of 75 ns to 150 ns duration according to fundamental frequency setting.
TP4	TTL level. Normally low with two high pulses close together. The first and only significant pulse is between 40 ns and 80 ns wide according to the fundamental frequency. Frequency is approximately 50 kHz.
TP5	For Marconi Instruments Autotest use.
IC9,pin 12	TTL level. Output from v.r.d. Frequency approx. 50 kHz.

AB2 - Divide-by-two chain and f.m. drive

79. The r.f. divide-by two system on AB2 is generally straightforward. A fault will normally result in a failure to frequency divide the signal over one or more octaves and either produce the wrong output frequency or no output

latched by IC8 is correct and check the input and output circuits of the divide-by-two that normally generates the required octave of frequency. The relevant dividers are listed below :

Output frequency range	Output IC No.
260-520 MHz	-
130-260 MHz	1
65-130 MHz	2
32.5-65 MHz	3
16.25-32.5 MHz	4
8.125-16.25 MHz	4
4.0625-8.125 MHz	5
2.03125-4.0625 MHz	5

If all frequencies below 130 MHz are affected, check that IC6 is not faulty.

80. Control data AB2. Two sets of control data are required for AB2. The data sent to the octal latch IC8 control the circuits that divide the output from AB2 by factors of two as shown in Table 15 below.

TABLE 15 DIVIDE-BY-TWO CONTROL DATA AB2

Output frequency of instrument (MHz)	Data sent to latch A6L4 IC8 of AB2 D7	D6	D5	D4	D3	D2	D1	D0
1040 - 520.00002	1	1	0	0	0	1	1	1
520 - 260.00001	1	1	0	0	0	1	1	1
260 - 130.00001	1	0	1	0	0	1	1	1
130 - 65.00001	1	0	0	1	0	1	1	1
65 - 32.50001	1	0	0	0	0	0	1	1
32.5 - 16.25001	1	0	0	0	0	1	0	0
16.25 - 8.12501	1	0	0	0	1	1	0	0
8.125 - 4.06251	1	0	0	0	1	1	0	1
4.0625 - 2.03126	1	0	0	0	1	1	1	1
0.08 - 2.03125	1	0	0	0	1	1	0	0

at all. The fault will normally be found in the highest frequency circuit that fails to operate correctly. Check that when the fault occurs the data

81. The second set of control data is required to provide range data for the f.m. drive circuits. From the f.m. deviation the instrument is set to first calculate the f.m. deviation required from AB3. This calculated deviation has to take into account the fact that if AB2 has to be set to divide the frequency from AB3 then it will also divide the f.m. deviation. The frequency multiplier in 2019A that generates the 520 to 1040 MHz band doubles the f.m. deviation and the b.f.o. band of 0.08 - 2.03125 MHz is generated from 10 to 12 MHz. From this deviation, called the fundamental deviation, the control data required is as shown in Table 16 below.

TABLE 16 RANGE CONTROL DATA AB2

Fundamental deviation (kHz)	Data sent to A6L6 IC9 of AB2							
	D7	D6	D5	D4	D3	D2	D1	D0
1280 - 5200	*	*	*	*	*	1	1	1
320 - 1280	*	*	*	*	*	0	1	1
80 - 320	*	*	*	*	*	0	0	1
0 - 80	*	*	*	*	*	0	0	0

Note * indicates a "don't care" state.

82. Test data AB2

TR1 collector	Approximately 0 dBm at fundamental frequency.
TR2 emitter	For output freq. >260 MHz signal level -14 dBm. For output freq. <260 MHz signal level 0 dBm with some sub-harmonics present.
IC1, pin 7	For output freq. >130 MHz signal level less than -20 dBm. For output freq. <130 MHz signal level 0 dBm covering octave 130 MHz to 260 MHz. Some sub-harmonics present.
TR8 base	For output freq. <130 MHz signals are at -15 dBm. For output freq. 130 to 260 MHz signal -5 dBm. For output freq. >260 MHz only low level signals.
PLCJ, pin 2	With carrier frequency 520 MHz, f.m. deviation 5.2 MHz at 1 kHz rate. Audio signal typically 8 V p-p. As above at 2.6 MHz deviation audio signal 4 V p-p. As above at 1.2 MHz deviation audio signal 7.7 V p-p.

AB3 : RF oscillators

83. Faults on AB3 which result in one or more of the oscillators not operating can generally be found by first identifying which oscillator is at fault and then checking the d.c. bias conditions of the active and off oscillators. If the active device is not at fault it will be necessary to check or replace each element of the tuned circuit.

84. Residual f.m. problems are generally more difficult to find. There are many possible causes but the most likely ones are noisy varactors, noisy transistors or intermittent capacitors. The decoupling capacitors C9,C10,C25,C26 can cause residual f.m. problems even when the oscillator to which they are connected is not on. This is because they cause an additional coupling diode, D3,D4,D10 or D11 to be partially turned on.

85. Microphony can be caused if the inductors L1,L2,L5,L6,L7,L8,L11,L12 are not securely varnished to the printed circuit board.

86. Test data AB3

SKDL	(Output from pin 1). Output level varies from approximately -3 dBm according to fundamental frequency selected. Frequency is that of the fundamental octave.
C112	(Input from pin 1). Between 3 V and 15 V according to the frequency selected.
TR6 base	Approximately 6 dBm varying with fundamental octave frequency.
TR11 collector	Approximately -3 dBm. May have significant levels of harmonics present.

87. The following data applies with a carrier frequency of 520 MHz set:

TR2 collector	11.5 V d.c.
TR4 collector	11.5 V d.c.
TR7 collector	11.5 V d.c.
TR9 collector	8.5 V d.c.

88. Realignment data AB3. Each of the 4 oscillators incorporates a sliding link on its tuning inductor which may be used to set up the oscillator. During adjustment the heat of the soldering iron used to move the link will cause some reaction from the oscillator frequency. Excessive heating should be avoided in order to avoid long settling times.

(1) On oscillator 1, adjust the sliding link such that at an output frequency of 260.00001 MHz, the voltage on tag 2, is nominally 3.6 V without the lid of the oscillator on.

(2) On oscillator 2, adjust the sliding link such that at an output frequency of 309.00001 MHz, the voltage on tag 2, is nominally 3.3 V without the lid of the oscillator on.

(3) On oscillator 3, adjust the sliding link such that at an output frequency of 368.00001 MHz, the voltage on tag 2, is nominally 3.3 V without the lid of the oscillator on.

(4) On oscillator 4, adjust the sliding link such that an an output frequency of 437.00001 MHz, the voltage on tag 2, is nominally 3.3 V without the lid of the oscillator on.

AB4 : Output phase detector

89. Digital faults on AB4 are generally easy to find using the test data provided. If necessary the mini-jump linking TP6,7 can be removed and a voltage applied to TP7 to control the oscillators on AB3, but most faults can be found without using this method. Faults in the digital part of the phase comparator are also relatively easy to find.

90. If the fault is in the analogue part of the phase detector first check all the d.c. voltages given in the test data. If the fault has not been located, remove the mini-jump and connect 0 V to TP7. IC5, pin 8 should produce pulses which will pull TP7 to 18 V. Check that this happens. If it does not, the fault is in the current pulse generator (TR12 to TR23) part of the phase detector. Repeat the test while applying 15 V to TP7. IC5, pin 6 should generate pulses which pull TP6 down to -8 V.

91. Diagnosing which transistor in the current pulse generator is at fault can be time consuming and as a result, it is often quicker to replace all the transistors.

92. If the phase locked loop sets the output frequency to approximately the correct value but the frequency is unstable, check that the p.l.l. filter control lines are working. If the fault cannot be found, replace the components in the loop filter. If TR6 develops a drain to source short circuit it may result in TR25 developing excessive input leakage current (because of impact ionization) and cause excessive phase detector breakthrough on the output carrier signal.

93. Control data AB4. The control data for AB4 is latched on the microprocessor board AA2/1. The latch address is A6L5. It should be noted that the latch address A6L5 also controls the frequency standard on AA3/2.

PLBY Pin No.	Line	Data
3	LD0	High for fundamental frequencies of 260.00001 to 309 MHz.
12	LD1	High for fundamental frequencies of 309.00001 to 368 MHz.
4	LD2	High for fundamental frequencies of 368.00001 to 437 MHz.
11	LD3	High for fundamental frequencies of 437.00001 to 520 MHz.
5	LD5	High if f.m. is not on.

If data to latch A6L5 is being sent under second function control ensure that the data sent on D4 and D6 is also correct (see AA3/2).

94. Test data AB4

IC1, pin 8	TTL signal. Approx. 50 kHz square wave.
IC4, pin 8	TTL signal. FM OFF Approx. 50 kHz square wave. FM ON Approx. 10 kHz signal.
IC4, pin 6	TTL signal. If output loop is locked then with f.m. off p.r.f. is approx. 50 kHz, and with the f.m. on it is 10 kHz.
IC5, pin 9	TTL signal. Normally high with a 50 ns low pulse at p.r.f. of approx. 50 kHz (FM OFF) or 10 kHz (FM ON). If the loop is out of lock and the oscillator (AB3) frequency is low, wider pulses should be produced to increase the oscillator frequency.
TR10 collector	With FM ON : 0 V. FM OFF : -11.2 V.
TR9 collector	With FM OFF : 0 V. FM ON : -11.2 V.
TP1	DC level approx. 17.5 V. When locked and the f.m. is off it has a 1 V positive pulse 50 ns wide. With the f.m. on the pulse should disappear.
TP2	DC level approx. -8 V. When locked and the f.m. is off it has a 0.7 V negative pulse 50 ns wide. No pulse when f.m. is on.
TP3	DC level approx. 17.5 V. When locked it has a 1 V positive pulse 50 ns wide with a p.r.f. of 50 kHz with the f.m. off and 10 kHz with the f.m. on.

TP4	DC level approx. -8 V. When locked it has a 0.7 V negative pulse 50 ns wide with a p.r.f. of 50 kHz with the f.m. off and 10 kHz with the f.m. on.
TP6,7	Mini-jump may be removed to control the oscillators on AB3 directly by applying a variable d.c. voltage to TP7.

AB5 : Voltage controlled crystal oscillator (v.c.x.o.) loop

95. AB5 contains the complete v.c.x.o. phase locked loop. There is a potential latch up condition which can occur only under fault conditions, whereby the phase locked loop can lock to a frequency less than 10 MHz. To avoid any possible confusion it is often easier to fault find with the mini-jump linking TP2,3 removed and the v.c.x.o. frequency controlled by a voltage applied to TP3. With link fitted and a carrier frequency of 520 MHz selected, the voltage at TP4 should be <2.3 V and >1.4 V, if not select L2 to obtain this.

96. An unusual fault can be caused if the capacitor C19 is open circuit. The spurious pick-up on pin 7, IC5, can cause multiple transitions on the output of IC6a and result in erratic failure to lock. This fault can be diagnosed by checking the output from IC6a for spurious edges on pulse transitions.

97. Test data AB5

TR1 collector	Distorted 3 V p-p signal. When phase locked frequency is between approx. 10.002 and 10.008 MHz (v.c.x.o. freq.).
TP1	TTL signal. VCXO frequency.
TR8 collector	Distorted signal at v.c.x.o. frequency 1 V p-p.
IC2, pin 1	10 MHz sine wave 0.6 V p-p. Some spurious a.m. from the v.c.x.o. frequency.
IC2, pin 6	DC level 9 V. Audio signal approximately 1.5 V p-p. Frequency (when locked) of approx. 2 to 8 kHz.
IC5, pin 3	Audio signal about ground. Approx. 1.5 V p-p.
IC5, pin 7	Square wave signal 5 V p-p. TTL compatible, freq. approx. 2 to 8 kHz.
IC4, pin 3	TTL signal. Freq. of 2 to 8 kHz.
IC4, pin 11	TTL signal. Freq. 2 to 8 kHz if v.c.x.o. is locked.
IC4, pin 8	TTL signal. Normally low with a 60 ns positive pulse. If the v.c.x.o. frequency is too low it produces wider pulses to pull the v.c.x.o. frequency lower.
IC4, pin 5	TTL signal. Normally high with a negative 60 ns pulse. If the v.c.x.o. frequency is too high it produces wider pulses to pull the v.c.x.o. frequency higher.

TP4	With carrier frequency set to 520 MHz (v.c.x.o. approx. 10.002 MHz) d.c. level 3.6 V. With carrier frequency set to 260.09999 MHz (v.c.x.o. approx. 10.008 MHz) d.c. level 10 V.
TP2,3	Mini-jump may be removed and an external d.c. voltage applied to TP3 to control the v.c.x.o. frequency.

AC2 : Beat frequency oscillator (BFO) system

98. Test data AC2. The following data applies at a carrier output frequency of 2 MHz.

PLCU, pin 2	10 MHz square wave 0.6 V p-p
TR1 collector	10 MHz square wave 0.6 V p-p
PLCV, pin 1	12 MHz sine wave 90 mV p-p
TR2 collector	Very distorted signal approx. 80 mV p-p
L4,L5 junction	-20 dBm 2 MHz signal and 2 V d.c.
PLCW, pin 3	4 V d.c.
PLCW, pin 1	-20 dBm at 2 MHz

99. The following data applies at an output frequency of 10 MHz

PLCU, pin 2	0 V
L4,5 junction	No signal
PLCW, pin 3	+0.05 V d.c. RF signal level -15 dBm
PLCW, pin 1	RF signal -15 dBm.

AC3/13 : Filter and frequency doubler

100. Faults in the filter sections of AC3 or AC13 will usually result in the signal faults occurring over specific half octaves of frequency cover. The half octaves involved will usually give some idea of where the fault is. If the error occurs only at frequencies greater than 32.5 MHz, check the d.c. voltages at the output of IC4 against the test data. These d.c. voltages control the diodes that switch the filters. Faults in the frequency doubler section of AC13 (2019A only) can be difficult to trace because of the high frequencies involved. The recommended procedure is to first establish that the active stages are working (TR4, TR5, TR6). Check that the filter control outputs from IC7 are correct. If the fault is diagnosed as being in the filter circuits it may be necessary to replace the components one at a time, in order to find the fault.

TABLE 17 IC2 CONTROL DATA AC3/13

Output frequency (MHz)	Data sent to A7L4 IC2 of AC3/13 D7	D6	D5	D4	D3	D2	D1	D0
520.00002 - 1040	1	1	1	1	1	1	1	1
260.00001 - 520	0	1	1	1	1	1	1	1
130.00001 - 260	1	0	1	1	1	1	1	1
65.00001 - 130	1	1	0	1	1	1	1	1
32.50001 - 65	1	1	1	0	1	1	1	1
16.25001 - 32.5	1	1	1	1	0	1	1	1
8.12501 - 16.25	1	1	1	1	1	0	1	1
4.06251 - 8.125	1	1	1	1	1	1	0	1
2.03126 - 4.0625	1	1	1	1	1	1	1	0
0.08 - 2.03125	1	1	1	1	1	0	1	1

Data line	Data sent to A7L5 IC3 of AC3/13
D4	High for frequencies less than or equal to 520 MHz (2019A only).
D3	High for frequencies of 2.03126 to 1040 MHz.
D2	High for frequencies of 16.25001 to 23 MHz and for frequencies of 260.00001 to 368 MHz, and for frequencies of 32.50001 to 130 MHz, (Program versions 012 and later).
D1	High for frequencies of 260.00001 to 1040 MHz, 16.25001 to 32.5 MHz and fundamental frequencies of 368.00001 to 520 MHz.
D0	High for frequencies of 0.08 MHz to 32.5 MHz.

Note: Fundamental frequency is defined as the output frequency from AB3.

TABLE 18 IC6 CONTROL DATA AC13

Output frequency (MHz)	Data sent to A7L6 IC6 of AC13 D7	D6	D5	D4	D3	D2	D1	D0
520.00002 - 660	*	*	*	*	1	0	1	0
660.00002 - 820	*	*	*	*	1	0	0	1
820.00002 - 1040	*	*	*	*	0	1	1	1

Note: * indicates a "don't care" condition.

102. Test data AC3/13. The following data applies to conditions where the output frequency has been set to be >32.5 MHz. Measurements have been taken with a carrier frequency of 100 MHz unless otherwise stated. RF levels quoted are with the output level set to 7 dBm unless otherwise noted.

TR1 base RF level -15 dBm, nominal square wave

TR2 collector RF level -2 dBm

D24 cathode RF level -4 dBm

SKCS RF level -5 dBm

103. Table 19 gives a list of the expected output voltages on the open collector outputs of IC4.

TABLE 19 DC VOLTAGES ON IC4 OUTPUTS AC3/13

Carrier frequency	IC4 pin numbers 2	4	12	10	8
1040 MHz	15	15	15	15	0.13
520 MHz	0.15	4.81	6.87	9.16	11.67
260 MHz	15	0.15	5.18	7.76	10.79
130 MHz	15	15	0.15	5.97	9.53
65 MHz	15	15	15	0.15	7.77

104. The following data applies to conditions where the output frequency has been set to <32.5 MHz. Measurements generally refer to a carrier of 10 MHz unless otherwise stated.

TR3 collector RF level -14 dBm

PLCT RF level -15 dBm

105. The following data applies to AC13 (2019A) only.

C10	Carrier 530 MHz -5 dBm, sub-harmonic -24 dB Carrier 1040 MHz -3 dBm, sub-harmonic -10 dB
TR5 collector	Carrier 530 MHz 3 dBm, sub-harmonic -27 dB Carrier 1040 MHz 0 dBm, sub-harmonic -7 dB
TR6 base	Carrier 530 MHz -8 dBm, sub-harmonic -40 dB Carrier 1040 MHz -9 dBm, sub-harmonic -33 dB

106. Realignment procedure. Connect an r.f. signal source to PLDF, level -11 dBm.

LF Channel:

Monitor output from PLCT (providing a 200 Ω load impedance). Select each of the low-pass filters in turn by keying-in the SET FREQ on the 2018A/19A keyboard, and check the PASS BAND ripple and relative attenuation at the 2*f (min) FREQ.

Nominal output level: 40 mV (r.m.s. p.d.) into 200 Ω *
PASS BAND ripple: not greater than 4 dB
2*f (min) level: better than -18 dBc for 32.5 - 4.0625 MHz,
better than -15 dBc for 4.0625 - 2.03126 MHz.

TABLE 20 LF LOW-PASS FILTER ALIGNMENT (1 - 32 MHz) AC3

SET FREQ MHz	PASS BAND MHz	2*f (min) FREQ MHz
32	23 - 32.5	46
23	16.25 - 23	32.5
16	11.5 - 16.25	23
11	8.125 - 11.5	16.25
8	5.75 - 8.125	11.5
5	4.0625 - 5.75	8.125
4	2.875 - 4.0625	5.75
2.8	2.03126 - 2.875	4.0625
Monitor the output from PLCR pin 1 (200 Ω load impedance) to check the output to the b.f.o. board. Same conditions as above.		
2	11.5 - 12.03125 MHz	23
1	10.08 - 11.5	20

*NOTE: If 200 Ω load is made up by including a 150 Ω resistor in series with the 50 Ω input of the measuring instrument a 12 dB insertion loss will be introduced. This will result in a level of 10 mV across 50 Ω, or -27 dBm.

105. The following data applies to AC13 (2019A) only.

HF Channel:

107. Monitor output from SKCS (load impedance 50 Ω). Tests similar to those for the LF Channel are performed, but the HF Channel filters need to be individually adjusted to meet the following conditions:

Nominal output level:	-6 dBm
PASS BAND ripple:	not greater than 4 dB
2*f (min) level:	better than -20 dBc.

(1) To trim the 520 and 368 MHz low-pass filters, unsolder sliders on printed coils and re-position as required. (There is no need to switch off the power supplies.) Moving the sliders towards the filter capacitors will reduce the inductance and so raise band edge frequency. Providing the PASS BAND ripple and 2*f (min) level are correct the actual band edge frequency is unimportant.

(2) To trim the "turret" low-pass filters, start with the ferrite slugs flush with the turret tops. Wind the slug in the lower numbered coil downwards until the filter band edge drops by 1 dB; then unwind 1 full turn. Repeat this operation for the second coil. Finally check the conditions above and make further minor adjustments as necessary.

TABLE 21 HF LOW-PASS FILTER ALIGNMENT (46 - 520 MHz) AC13

SET FREQ MHz	PASS BAND MHz	2*f (min) FREQ MHz
520	260 - 520	736 **
368	260 - 368	520
260	184 - 260	368
184	130 - 184	260
130	92 - 130	184
92	65 - 92	130
65	46 - 65	92
46	32.5 - 46	65

** NOTE: 520 MHz low-pass filter is checked down to 260 MHz (rather than 368 MHz) to ensure correct operation of frequency doubler (2019A only).

108. Frequency doubler. Monitor the output from SKCS. Select the three SET FREQ points in turn and check the level of "doubled" signal, its sub-harmonics and harmonics (up to about 1.2 GHz) across the appropriate INPUT FREQ range. The following conditions should be met for the "doubled" signal:

Nominal output level: -6 dBm (±3 dB)
Level of sub-harmonics/harmonics: Better than -35 dBc.

TABLE 22 FREQUENCY DOUBLER AC13

SET FREQ MHz	INPUT FREQ RANGE MHz	OUTPUT FREQ RANGE MHz
660	260 - 330	520 - 660
820	330 - 410	660 - 820
1040	410 - 520	820 - 1040

AC4 : Output amplifier ⚠

109. If, for any reason, it is necessary to remove the board AC4 from the instrument take care not to damage the integral Beryllium Oxide washer in TR10. The device is robust but it should be protected from accidental damage. If it is necessary to remove the heatsink from the stud, ensure that the nut is not overtightened. A tightening torque of 0.8 Nm is recommended by the manufacturer. See Notes and Cautions re the disposal of defective devices.

110. Control data AC4

Address	IC No.	Data lines	Data sent
A7L1	4	D0-D7	Insertion loss control data. Binary number of between 0 and 255 provides fine control level, 255 gives minimum level and 0 gives maximum level. Data to be sent is calculated by the microprocessor from the data entered to compensate for insertion loss.
A7L2	6	D0-D7	The 8 l.s.b's of a 10 bit number used to control the r.f. output level from AC4. The 10 bit number is a number between 0 and 1000 which can control the output level with a 1 mV p.d. resolution. The number IC6 is set to is not updated until the m.s.b. is sent on A7L3.
A7L3	6	D0-D1	The m.s.b's of the number sent to A7L2.
	2	D6	High for frequencies of 32.50001 to 1040 MHz.
	2	D7	High for frequencies of 32.5 MHz or less.

111. Test data AC4. All test data results are with the a.m. off unless otherwise stated.

IC3, pin 1	+2 V d.c. If 99% a.m. is set an audio signal should be present whose negative peaks almost reach 0 V.
IC3, pin 7	DC voltage typically -1.5 V at 10 MHz, -1.2 V at 520 MHz, -0.66 V at 1040 MHz. DC level at intermediate carrier frequencies is linearly interpolated between these voltages.
IC3, pin 8	DC voltage typically -2.9 V at 10 MHz, 13.4 V at 520 MHz, -4.1 V at 1040 MHz.
IC3, pin 14	DC voltage at 520 MHz carrier typically 1.69 V at 7 dBm, 3.37 V at 13 dBm, 0.546 V at -2.9 dBm.
IC1, pin 8	DC voltage at 520 MHz carrier typically 1.61 V at 7 dBm, 3.28 V at 13 dBm, 0.471 V at -2.9 dBm.
IC2, pin 9	Logic high for carriers >32.5 MHz.
IC2, pin 5	Logic high for carriers <32.5 MHz.
TP2	ALC voltage. Will be between 0 V and -8 V if the a.l.c. system is operating.

AC5 : Amplitude modulator

112. If, during the course of fault finding on AC5, it is necessary to remove or replace X2 ensure that when it is replaced the metal case is soldered to the printed board in the same way as originally manufactured. Failure to do so will result in poor a.m. performance.

113. Control data AC5

Latch Address	IC No.	Data Lines	Data sent
A7L0	4	D0-D6	7 bit binary number between 0 and 99 corresponding to the modulation depth set in %.
	2	D7	Single bit instruction that is set high for r.f. levels of 7.1 dBm or greater. In this mode the a.m. is set off and the mod. depth is set to 0%.

114. Test data AC5

IC4, pin 4	With a.m. on typically 6.5 V p-p audio.
IC3, pin 6	With a.m. set to 99% audio signal 5 V p-p decreasing linearly with reducing a.m. depth.
TR3 collector	-0.2 V for r.f. levels <7 dBm, -15 V for r.f. levels >7 dBm.
X1, pin 1	RF signal -6 dBm square wave.
X2, pin 5	RF signal 0 dBm square wave.
X2, pin 1	RF signal -18 dBm square wave.
TR1 collector	RF signal -12 dBm square wave.

AD11 : Display

115. The l.c.d. units are driven by square waves which are either in phase or out of phase in order to avoid generating any d.c. component across the display. In order to fault find on parts of the circuit where the drive wave-form has been converted to a square wave use a dual channel oscilloscope. Connect one input to the backplane drive on pin 1 or pin 80 of the carrier frequency display X1. Connect the second input to the point being tested and then observe the second input square wave is in phase or out of phase with the backplane drive. An in phase signal will result in a clear segment and an out of phase signal will result in a dark segment. The maintenance kit contains information on the use of the l.c.d. insertion and extraction tools.

116. Control data AD11

TABLE 23 CONTROL DATA AD11

Address	Data Lines	IC No.	Data sent
A5L0	D4-D7	4	Frequency display m.s.d.
	D0-D3	5	Frequency display second m.s.d.
A5L1	D4-D7	6	Frequency display third m.s.d.
	D0-D3	7	Frequency display fourth m.s.d.
A5L2	D4-D7	8	Frequency display fifth m.s.d.
	D0-D3	9	Frequency display sixth m.s.d.
A5L3	D4-D7	10	Frequency display seventh m.s.d.
	D0-D3	11	Frequency display l.s.d.
A5L4	D0-D3	21	Modulation display m.s.d.
A5L5	D4-D7	22	Modulation display second m.s.d.
	D0-D3	23	Modulation display l.s.d.

continued ...

TABLE 23 CONTROL DATA AD11 (continued)

Address	Data Lines	IC No.	Data sent
A5L6	D4	27	Level display m.s.d.
	D0-D3	29	Level display second m.s.d.
A5L7	D4-D7	30	Level display third m.s.d.
	D0-D3	31	Level display l.s.d.
A5L8	D0-D2	14 & 18	Frequency display decimal point. Lines decoded as 1 out of 8. An output of 0 gives a decimal point to the right of the m.s.d. and this moves to the right with increasing decoded output. An output of 7 gives no decimal point.
	D3-D4	26	Modulation display decimal point. Lines decoded as 1 out of 4. An output of 0 gives a decimal point to the right of the m.s.d. and this moves to the right with increasing decoded output. An output of 7 gives no decimal point.
	D5-D6	27	Level display decimal point. Lines decoded as 1 out of 4. An output of 0 gives a decimal point to the right of the m.s.d. and this moves to the right with increasing decoded output. An output of 3 gives no decimal points.
A5L9	D0	3	Frequency display REMOTE annunciator.
	D1	3	Frequency display ADDR annunciator.
	D2	3	Frequency display LIMIT.
	D3	3	Frequency display MHz.
	D4	12	Frequency display kHz.
	D5	12	Frequency display Hz.
	D6	12	Frequency display EXT STD.
	D7	12	Modulation display OFF.
A5L10	D0	20	Modulation display EXT.
	D1	20	Modulation display LIMIT.
	D2	20	Modulation display AM.
	D3	20	Modulation display FM.
	D4	24	Modulation display %.
	D5	24	Modulation display MHz.
	D6	24	Modulation display kHz.
	D7	24	Modulation display Hz.
A5L11	D0	28	Level display OFF.
	D1	28	Level display REV PWR.
	D2	28	Level display LIMIT.
	D3	28	Level display - (minus sign).

continued ...

TABLE 23 CONTROL DATA AD11 (continued)

Address	Data Lines	IC No.	Data sent
	D4	32	Level display + (vertical bar of + sign).
	D5	32	Level display dBm.
	D6	32	Level display dB.
	D7	32	Level display V.
A5L12	D0	33	Level display mV.
	D1	33	Level display µV.
	D2	33	Level display e.m.f.
	D3	33	Level display p.d.
A5L12	D4	34	Modulation display ΦM
	D5	34	Modulation display RAD

AD2 : Motherboard

117. Control data AD2. The data to control the 10 dB step attenuator and the RPP is latched on AD2 by IC1 address A6L10. The 10 dB step attenuator control data is as in Table 24 below.

TABLE 24 10 dB STEP ATTENUATOR CONTROL DATA AD2

Required attenuation dB	Data sent D5	D4	D3	D2	D1	D0
0	1	1	1	1	1	1
10	1	1	1	1	0	1
20	1	1	1	0	1	1
30	1	1	1	0	0	1
40	0	1	1	1	0	1
50	0	1	1	0	1	1
60	0	1	1	0	0	1
70	0	1	0	1	0	1
80	0	1	0	0	1	1
90	0	1	0	0	0	1
100	0	0	0	0	1	1
110	0	0	0	0	1	1
120	0	0	0	0	0	1

If the RPP is tripped it can reset by sending a logic 0 on A6L10 D0 followed by a logic 1 on the same address. Sending a logic 0 on A6L10 D0 will cause the RPP reed relay to go open circuit.

AD3/1 : AF oscillator and f.m. control

118. Control data AD3/1. The latch A6L15 controls the AF oscillator and partly the type of modulation being used. The data sent to A6L15 is as follows:

TABLE 25 AF OSC CONTROL DATA AD3/1

AF OSC FREQ Hz	Data on D0-D4 IC5 D4	D3	D2	D1	D0
300		0	0	0	0
400		0	0	0	1
500		0	0	1	0
1000		0	0	1	1
3000		1	1	0	0
6000	1	0	1	0	0

D5 High if f.m. is on
D6 High if INT MOD
D7 High if a.m. is on

119. The latches A6L14, A6L12 and A6L13 control the f.m. deviation. The data sent is calculated by first determining the deviation required of the oscillators on AB3 after allowing for division by AB2 and frequency translation by the b.f.o. band. This deviation is referred to as the fundamental deviation. The data sent to A6L14 is given in Table 26 below.

120. The multiplier shown in the right-hand column above is used to derive the data sent to A6L12 and A6L13. If the multiplier is multiplied by the fundamental deviation in kHz the resulting number is between 0 and 1023 and can be expressed as a 10 bit binary number. This number is sent as 2 bytes. The eight least significant digits are sent to A6L12 followed by the two most significant digits to A6L13 on D0 and D1. The setting of the 10 bit D-A reviewing this data, IC26 is only updated when the most significant bit is sent. Some of the other data lines on A6L13 are latched by IC16 as shown below. The data sent to A6L11 is an 8-bit number, usually between binary 80 and 200, which is calculated from information stored in the EAROM store. It is instrument dependent and therefore has no unique values. Further control

of the modulation is provided by the data latched by IC16 on address A6L13 as follows:

D0	}	Used to control IC26
D1		
D2		High if ϕ.m. is on Low if ϕ.m. is off
D4	}	Used to control AF level
D5		(see Table 27 below)
D6		High if mod. a.l.c. is on

TABLE 26 FM DEVIATION CONTROL DATA AD3/1

Fundamental deviation kHz	Data sent to A6L14 IC28 of AD3/1								
	D7	D6	D5	D4	D3	D2	D1	D0	Multiplier
5120 - 5200	1	1	1	1	1	1	1	1	0.1
5120 - 2560	1	0	0	0	0	0	0	0	0.2
2560 - 1280	0	1	0	0	0	0	0	0	0.4
1280 - 640	1	0	0	0	0	0	0	0	0.8
640 - 320	0	1	0	0	0	0	0	0	1.6
320 - 160	1	0	0	0	0	0	0	0	3.2
160 - 80	0	1	0	0	0	0	0	0	6.4
80 - 40	1	0	0	0	0	0	0	0	12.8
40 - 20	0	1	0	0	0	0	0	0	25.6
20 - 10	0	0	1	0	0	0	0	0	51.2
0 - 10	0	0	0	1	0	0	0	0	102.4

121. The AF level is controlled by an eight bit D-A which provides a scale, an eight bit D-A which provides range selection, and a c.m.o.s. multiplexer which provides further range scaling. The required data is given in Table 27 below.

TABLE 27 AF LEVEL CONTROL DATA

AF LEVEL	A6L8 D7	D6	D5	D4	D3	D2	D1	D0	A6L13 D5	D4	MULTIPLIER
2.56 to 5 V	1	1	1	1	1	1	1	1	1	1	.05
1.28 V to 2.55 V	1	0	0	0	0	0	0	0	1	1	0.1
.64 V to 1.27 V	0	1	0	0	0	0	0	0	1	1	0.2
.32 V to .639 V	1	0	0	0	0	0	0	0	1	0	0.4
.16 to .319 V	0	1	0	0	0	0	0	0	1	0	0.8
.08 V to .159 V	1	0	0	0	0	0	0	0	0	1	1.6
40 mV to 79.9 mV	0	1	0	0	0	0	0	0	0	1	3.2
20 mV to 39.9 mV	1	0	0	0	0	0	0	0	0	0	6.4
10 mV to 19.9 mV	0	1	0	0	0	0	0	0	0	0	12.8
5 mV to 9.99 mV	0	0	1	0	0	0	0	0	0	0	25.6
2.5 mV to 4.99 mV	0	0	0	1	0	0	0	0	0	0	51.2
1.25 mV to 2.49 mV	0	0	0	0	1	0	0	0	0	0	102.4
0 to 1.24 mV	0	0	0	0	0	1	0	0	0	0	204.8

Note ...

The multiplier listed in the right-hand column of Table 27 is used to calculate the number sent to A6L9 to provide the required scale. Multiplying the AF level in millivolts required by the prescribed multiplier will produce a number less or equal to 255. This number is rounded off and sent to A6L9 as an eight bit binary number.

122. Test data AD3/1

D8 anode	-7.5 V d.c.
IC7, pin 1	Audio signal at modulation frequency set to 0.9 V p-p.
IC7, pin 8	Audio signal 2.6 V r.m.s.
IC12, pin 15	INT MOD, 0.9 V p-p audio EXT MOD, audio signal corresponding to the external modulation input.
R34,R35 junct.	Audio signal 900 mV p-p from EXT MOD, level of which should be independent of input level for external inputs of 800 mV to 1.2 V r.m.s.

123. All the following data assumes INT MOD is selected.

IC31, pin 1	With FM ON 12 V p-p audio, FM OFF - no signal.
IC31, pin 7	With AM ON - typically 6.7 V p-p, AM OFF - no signal.
IC21, pin 6	FM ON, carrier 520 MHz (typically) 5 V p-p audio. FM ON, carrier 260.1 MHz (typically) 7.4 V p-p audio.
IC27, pin 6	FM ON, carrier 520 MHz, f.m. deviation 9.9 kHz typically 4.9 V p-p audio. FM ON, carrier 520 MHz, f.m. deviation 5.2 MHz typically 2.5 V p-p audio.
IC30, pin 6	FM ON, carrier 520 MHz, f.m. deviation 5.2 MHz typically 9.8 V p-p audio.
IC17, pin 6	AF level 1 V typically 2.0 V r.m.s. AF level 0.1 mV typically 0.2 V r.m.s.
IC19, pin 6	AF level 1 V typically 0.5 V r.m.s. AF level 0.1 mV typically 3.25 V r.m.s.

AT0/AT1 : 10 dB step attenuator

124. Except for simple faults which do not affect the main r.f. path on AT1, it is not recommended that repairs are attempted on AT1 unless very accurate attenuator measuring equipment is available. It is generally not advisable to attempt to remove the r.f. cover over AT1, but if the cover is removed do not attempt to adjust or remove AT1 since to do so can alter the calibration of the pads. If it is established that one of the micro-switches requires adjustment this can be accomplished by the following procedure:

(1) Adjust the large nylon nut so that the armature of the solenoid pulls in when between 13.5 V and 15 V d.c. is applied to the coil. The d.c. must be applied with SKLP disconnected from AT2.

(2) Energize all the solenoids except the one being adjusted.

(3) Connect a short circuit across SKAZ and an ohmmeter across SKBA. As the armature is manually closed a change of resistance should be observed when the micro-switch nearest SKBA operates. Adjust the corresponding adjustment screw so the switch operates at mid-travel.

(4) Repeat (3) with the short circuit across SKBA and the meter across SKAZ for the other micro-switch of the pad being adjusted.

(5) Lock the adjustment nut and screws with locking varnish.

125. Test data AT2

IC4, pin 8	TTL level. Normally low but on pressing the r.f. level key goes high for 40 ms.
TR3 collector	Normally unregulated 10 V. Goes to unregulated 25 V for 40 ms when r.f. level key is pressed.
IC3, pin 8	TTL level. Low except when attempting to reset the RPP.
IC3, pin 2	TTL level. Low unless reverse power has been applied.
IC3, pin 13	TTL level. Low unless RPP has been tripped.

TABLE 28 VOLTAGES ON PLP, AT2

RF LEVEL	PLP pin numbers 1	3	4	5	6	7
0 dBm	10 V	0 V	0 V	0 V	0 V	0 V
-10 dBm	10 V	0 V	0 V	0 V	0 V	10 V
-20 dBm	10 V	0 V	0 V	0 V	10 V	0 V
-30 dBm	10 V	0 V	0 V	0 V	10 V	10 V
-40 dBm	10 V	10 V	0 V	0 V	0 V	10 V
-50 dBm	10 V	10 V	0 V	0 V	10 V	0 V
-60 dBm	10 V	10 V	0 V	0 V	10 V	10 V
-70 dBm	10 V	10 V	0 V	10 V	0 V	10 V
-80 dBm	10 V	10 V	0 V	10 V	10 V	0 V
-90 dBm	10 V	10 V	0 V	10 V	10 V	10 V
-100 dBm	10 V	10 V	10 V	10 V	0 V	10 V
-110 dBm	10 V	10 V	10 V	10 V	10 V	0 V
-120 dBm	10 V	10 V	10 V	10 V	10 V	10 V

Where the above table shows a voltage of 10 V this is taken as being the nominal unregulated voltage that appears on pin 1. Where 0 V is shown there will be a small positive voltage, not exceeding 0.4 V, due to the saturation voltage of the drivers IC5, IC6 on AT2.

EAROM Initialization

126. In the event of the EAROM AA2/1, IC14 being replaced or accidentally erased the EAROM must be given certain initial information for correct operation of the program. Data should be entered in a sensible order indicated in the following steps and in conjunction with second function 17.

(1) By means of second function 190 enter the identity string settings; instrument type and serial number can be found on the rear panel.

(2) Select the GPIB command set to 2018A "0", or 2018 "1" by means of second function 15. Unless compatibility is required with 2018 commands it is recommended that the 2018A command set is chosen.

(3) Set the frequency standard to either 10 MHz "0" or 1 MHz "1" as required via second function 14.

(4) Enter the required r.f. level units required via second function 5.

(5) Set the r.f. level offsets off "0" via second function 6. The offset facility must not be used until the instrument is calibrated.

(6) Remove the store protection if implemented via second function 191 and the "0" key. Store values can now be entered. Each store has a separate checksum which is automatically entered on storing a valid setting. Stores not having a value entered will initiate an error 17 message when recalled.

(7) Select second function 192 and set the "Display blanking of recalled stores" to the required state, off "0", or on "1".

(8) If the optional GPIB facility is fitted set the GPIB address as required via second function 2.

The non-volatile store is normally supplied with all "1"s stored. Complete the operation by selecting SECOND FUNCT 17 and STORE keys.

Notes ...

(1) The flags on most second functions referred to above have been arranged such that the most useful settings are selected when a replacement EAROM store is installed. The above steps however should each be checked to determine individual user requirements.

(2) The total instrument operating time indicator, if accessed with second function 10 will probably read 131,071 hours. After approximately 15 minutes instrument running time this will overflow and reset to 0 hours.

Internal frequency standard

127. Using a frequency counter operated from a high accuracy frequency standard monitor the frequency standard output from the rear panel. The frequency standard may be adjusted without removing the external covers by adjusting R1 on AA/B0/1. Access to R1 is gained using a small screwdriver inserted through the circular hole in the group of vents on the right-hand side of the instrument at the top front corner.

128. Calibration of the output level requires the access to second function operations. An accurate power meter is required to set up the r.f. level calibration. The 10 dB step attenuator contributes significantly to level errors for outputs below -3.0 dBm. Specialized equipment is required to set up the attenuator and is not covered in detail in this procedure. The following procedure is used to set up the r.f. level at levels greater than -3.1 dBm. If the recalibration is required only on a routine basis (i.e. there has been no major fault in the level control system) step (2) should be omitted and step (3) may be omitted if the difference in r.f. level between 7 dBm and -2.9 dBm is 9.9 dB ±0.15 dB.

(1) Enter SECOND FUNCT "0" and overcome the second degree protection by carrying out the Second level operation unlocking procedure. Details of this procedure are given in Chap. 4, page 40.

(2) Set the carrier to 10 MHz and enter SECOND FUNCT "7". Enter the number 050 on the keypad followed by the STORE key. Repeat this procedure at 260 MHz, 520 MHz, 780 MHz and 1040 MHz (only if it is a 2019A) and entering the numbers 75,100 and 135,170 respectively.

(3) Set the carrier to 10 MHz and the level to 7 dBm. Adjust R86 on AC4 for an output of 7 dBm measured on a power meter at the r.f. output connector. Set the output level to -2.9 dBm. Adjust R89 on AC4 to obtain the correct output level. Repeat steps 2 and 3 until levels are correct to within 0.1 dB.

(4) The output level can now be accurately set up from the front panel alone by adjusting the calibration at 3 carrier frequencies using the second function operation. Set the carrier to 10 MHz and the level to 7 dBm. Enter SECOND FUNCT "7". The output level may be adjusted by entering a 3 digit number between 000 and 255 followed by the STORE key.

Note ...

Do not exceed the number entered at 260 MHz - in this case 075.

Increasing the number entered will increase the output level. When a satisfactory entry is obtained this procedure is repeated at a carrier frequency of 260 MHz. In this case the number entered should not be less than that stored at 10 MHz and should not be more than that stored at 520 MHz. After completing the entry at 260 MHz repeat the same procedure at 520 MHz. The number entered should not be less than that entered at 260 MHz. Repeat this procedure again at 780 MHz and 1040 MHz if the instrument is a 2019A.

(5) Check the r.f. level accuracy at 7 dBm and -2.9 dBm is better than ±0.4 dB from 10 MHz to 520 MHz, and better than 0.8 dB from 520 MHz to 1040 MHz. On 2019A, if necessary, the calibration number at 1040 MHz can be adjusted to give the best average accuracy from 780 MHz to 1040 MHz.

(6) On completion of step (5) select SECOND FUNCT 17 to recalculate and store the amended EAROM sum data.

(7) Relock the second function by entering SECOND FUNCT "0".

(8) After calibrating the r.f. level it is advisable to check the a.m. calibration.

AM calibration

129. An accurate modulation meter and a distortion meter are required to calibrate the a.m.

(1) Set R23 on AC5 (PRE-MOD) fully clockwise.

(2) Set the instrument to give 0 dBm at 100 MHz with the a.m. set to internal modulation at 1 kHz rate and 80% depth. Adjust R64 on AD3/1 to give 80% modulation depth as measured by the modulation meter.

(3) Adjust R23 on AC5 to give minimum a.m. distortion. Recheck step (2).

(4) Set the carrier frequency to 400 MHz and check that the a.m. distortion and level accuracy is within specification.

(5) Monitor pin 14 of IC3 on AC4 with a d.c. coupled oscilloscope. Set the modulation depth to 99%. Switch the a.m. off temporarily and note the d.c. voltage level observed on the oscilloscope. Switch the a.m. back on and adjust R77 on AC4 such that the negative tips of the sine wave on pin 14 of IC3 come to a voltage, with respect to ground, of 1% of that noted previously.

(6) Set the instrument to give 80% depth at 300 Hz rate internal modulation. Adjust R95 on AC4 to give the minimum ripple at the modulation frequency on IC1, pin 1 on AC4 (TP2).

FM calibration

130. An accurate modulation meter is required to calibrate the f.m. Calibration adjustments can take one of two forms. If the f.m. is out of calibration at all carrier frequencies and deviations by a consistent percentage the calibration can be adjusted using R75 on AD3/1. If, however, recalibration is necessary because of work carried out which may result in less predictable changes (e.g. to AB3) the f.m. should be recalibrated as follows under second function control. This recalibration can be easily accomplished using the GPIB if the modulation meter and 2018A, 2019A have a GPIB fitted and a controller with a suitable program is available.

(1) Set the instrument to 520 MHz at 0 dBm. Set the f.m. to 100 kHz deviation at 1 kHz rate in the internal mode. Set the carrier frequency increment size to 4.15 MHz. Enter SECOND FUNCT "0" and overcome the second degree protection by carrying out the Second level operation unlocking procedure. Details of this procedure are given in Chap. 4, page 40.

(2) Using an accurate a.c., d.v.m. monitor the voltage on IC31 pin 1 (a test pad marked 4.24 V r.m.s. located immediately above IC21 can be used for this purpose). Adjust AD3/1, R75 for 4.24 V r.m.s. (12 V p.p.). R75 adjusts the overall f.m. level.

(3) Enter SECOND FUNCT "8". The r.f. level display will show a number corresponding to the tracking data at 520 MHz. This number is changed in order to obtain 100 kHz deviation as measured by the modulation meter. The number can be changed by entering a new 3 digit number or by using the increment keys. When the best value is found pressing the STORE key will store the data in the non-volatile memory. If the store key is not pressed the number will return to its previous setting when you exit from the second function mode.

(4) Enter CARRIER FREQ and increment down in frequency by pressing the increment key. Then repeat the procedure given in step 3 at the new carrier frequency. Keep repeating this procedure until a carrier frequency of 437 MHz is reached. Then reset the carrier to 437.00001 MHz and repeat the procedure for entering new tracking data. This will complete the tracking oscillator 4 on AB3.

(5) The above procedure has to be repeated for the other 3 oscillators on AB3. Oscillator 3 is tracked by setting an incremental carrier of 3.45 MHz and starting at a carrier of 437 MHz. On reaching 368 MHz the carrier is reset to 368.00001 MHz and the last tracking point for oscillator 3 can be entered. Oscillator 2 is tracked by setting an incremental carrier of 2.95 MHz and starting at a carrier of 368 MHz. On reaching 309 MHz the carrier is set to 309.00001 MHz and the last tracking point for oscillator 2 can be entered. Oscillator 1 is tracked by setting an incremental carrier of 2.45 MHz and starting at a carrier of 309 MHz. On reaching 260 MHz the carrier is reset to 260.00001 MHz and the last tracking point for oscillator 1 can be entered.

(6) On completion select SECOND FUNCT 17, STORE to recalculate and store the amended EAROM checksum data.

(7) Relock the second function by entering SECOND FUNCT "0".

Phase modulation

131. An accurate modulation meter is required to calibrate the phase modulation. As the instrument uses the FM system to provide phase modulation it is only necessary to set the calibration at one carrier frequency and deviation.

(1) Set the instrument to provide 100 radians deviation at 520 MHz carrier and a modulation rate of 1 kHz internal. Adjust R70 AD3/1 to provide calibrated phase modulation.

(2) If the modulation meter does not have a phase modulation measurement mode then the phase modulation can be calibrated by first measuring the modulation frequency in kHz using a counter. The required FM deviation under the above conditions (100 radians), is then 100 times the modulation frequency in kHz.

External phase modulation calibration

132. Set the instrument to give 100 kHz FM deviation at 520 MHz with the internal oscillator at 1 kHz and carry out the following procedure:

(1) Apply an accurate 1 V p.d. 1 kHz signal to the external mod I/P. Use a modulation meter to measure the FM deviation. With the instrument set to INT FM, note the FM deviation.

(2) Set the instrument to EXT FM and MOD ALC off, adjust R37 AD3/1 to give the same deviation.

(3) Set the instrument to EXT FM and MOD ALC on. Then adjust R32 AD3/1 to give the same deviation.

Threshold l.e.d. setting

133. Apply an accurate 1.022 V p.d. 1 kHz signal to the MOD INPUT socket. Adjust R23, AD3/1 so that the HI l.e.d. is just extinguished. Now reset signal source to 0.98 V p.d. and check that the LO l.e.d. is off. Further reset the signal source, first to 0.975 V p.d. to check the LO l.e.d. lights then to 1.025 V p.d. to check that the HI l.e.d. lights. At 1 V both l.e.d's should be off.

AF level

134. Set the internal AF oscillator to 1 kHz and the AF O/P to 1 V p.d. Using an accurate AC voltmeter measure the AF O/P level. Adjust R60 AD3/1 to obtain a level of 1 V p.d.

Chapter 5, Annex A

MEASUREMENT OF PHASE NOISE IN SIGNAL GENERATORS

CONTENTS

Side band noise

1. Side band noise measurements require the use of specialized equipment which is not always available to the user. Some methods of measuring side band noise are contained in this annex.

discriminator methods. The calibration of each system is explained in terms of simple narrow band modulation theory and a minimum of mathematics is used throughout.

Measurement of phase noise in signal generators

D. P. Owen, B.Sc. (Hons)

All signal sources exhibit some degree of randomness in their frequency and amplitude due to the effects of random noise, interference, temperature fluctuations and other physical influences. For convenience these effects can be considered as being equivalent to a combination of amplitude modulation and angle modulation, i.e. phase or frequency. The amplitude modulation component is generally much less troublesome in signal generators since its magnitude is usually much smaller than the random angle modulation.

Over the years many methods of measuring random phase modulation have been used. For f.m. applications the most convenient measurement technique is to measure the equivalent f.m. deviation recovered by a low noise receiver tuned to the carrier frequency. The residual demodulated f.m. is measured in a specified audio band, or a weighted band such as that used for telephones, and represents the average peak f.m. deviation. Alternatively in phase modulation applications the equivalent residual phase modulation expressed in radians or degrees can be measured. As with f.m. measurement, the measurement is taken in a specified bandwidth and represents the average peak phase deviation, though occasionally the peak-to-peak value is quoted. These results, however, only give a limited idea of the characteristics of a generator and for many applications the single figure is not adequate. A more convenient method of defining phase noise modulation is to express the noise as the noise power contained in a single sideband in a 1 Hz bandwidth, at a specified offset frequency from the carrier, relative to the carrier power. If the noise at various frequency offsets is measured an s.s.b. noise plot such as that shown in Fig. 1 can be drawn. The ratio of phase noise power to carrier power is generally expressed as a logarithmic ratio and therefore has units of dBc/Hz, where dBc is decibels relative to carrier power.

In general, phase noise is highest at low offset frequencies and falls with increasing offset frequency until the amplifier noise floor is reached. The white noise added to the carrier signal by the amplifiers in the signal source effectively contributes equal amounts of phase and amplitude noise modulation and hence will contribute a phase noise power of −3 dB relative to the white noise power in a 1 Hz bandwidth. Provided that the total equivalent phase modulation (ph.m.) deviation is much less than 1 radian the phase noise plot may be used to derive an approximation to the residual ph.m. or f.m. deviation using a fairly simple if somewhat tedious algebraic routine.

For phase modulation the band of interest can be split in sub-bands of frequency each having roughly constant phase noise power. The total phase noise power, N, in a sub-band can then be calculated from the general formula

$$N_1 = N_A \log B_1 \text{ dBc}$$

where N_A is the average noise power/Hz in the sub-band of bandwidth B_1.

From this the equivalent ph.m. deviation in each band can be calculated by noting that narrow band modulation theory gives the result that 1 radian deviation gives a −6 dB carrier sideband. Hence if the noise in a given sub-band is −66 dB this is equivalent to a deviation of 0·001 radian (−60 dB relative to 1 radian). The total ph.m. deviation is then found by taking the square root of the sum of the squares of the deviations in each band.

The residual f.m. deviation can be found using the same technique but the sideband power in each sub-band is converted into an equivalent f.m. deviation using narrow band modulation theory. If the sub-band power is −66 dB and the average offset frequency of the sub-band is 1 kHz the equivalent f.m. deviation is 1 Hz, i.e. −60 dB relative to 1 kHz. Again the total f.m. deviation is found by taking the square root of the sum of the squares of the deviations in the sub-bands. This method will only give an approximate idea of the residual modulation but it can be a useful technique if the manufacturers information does not give the residual modulation in the required bandwidth.

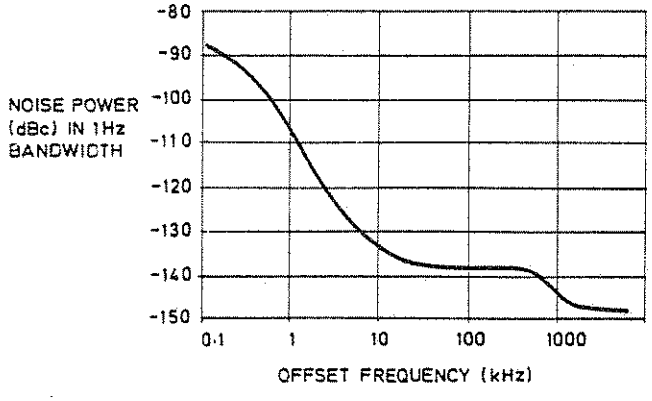


Fig. 1. A typical phase noise plot for the 50 kHz – 520 MHz Synthesized Signal Generator type TF 2020.

In recent years there has been considerable interest in the measurement of the phase characteristics of frequency sources. Two methods of measuring phase noise are presented, the quadrature and the f.m.

of the beat note as before.

When the system is phase locked the p.l.l. bandwidth can be checked by injecting a low level variable frequency at TP1 in Fig. 3 and varying the frequency of the source until the amplitude of the signal appearing on TP2 is within 3 dB of the signal level at TP2. This frequency will be approximately equal to the loop bandwidth and phase noise measurements should only be taken at frequencies at least an octave above this.

Quadrature measurement capability

The measurement capability of the system is determined by the beat note level recovered from the mixer and the noise and dynamic range of the selective analyser used. In most cases the resolution may be improved by using a low noise preamplifier to amplify the signal from the mixer as shown in Fig. 4. When the system is being calibrated the preamplifier is removed to prevent overloading the preamplifier and the selective analyser. When the noise is being measured the preamplifier is switched in and an oscilloscope is used to check that the maximum input level to the analyser is not exceeded and that phase quadrature has been set. The gain of the preamplifier has to be corrected for when calculating the measured phase noise.

If the preamplifier has a gain sufficiently high so that the noise of the analyser has no effect on the system resolution the noise floor capability of the system can be estimated if the equivalent input noise voltage of the preamplifier is known and the amplitude of the beat note is measured. In practice the best discrete audio amplifiers will have an equivalent input noise voltage of approximately 2 nV/Hz at frequencies greater than 4 kHz which is roughly equivalent to the thermal noise of a 250 Ω resistor. For a recovered beat note of 30 mV r.m.s. the noise floor is then given by

$$N = -6 + 20 \log \frac{2 \times 10^{-9}}{30 \times 10^{-3}} = -149 \text{ dBc/Hz.}$$

Most common operational amplifiers have an input noise voltage of 15 nV/Hz so the system floor noise using one of these devices as a preamplifier would be around −132 dB/Hz. A low noise operational amplifier such as the TDA1034N with a typical performance of 3·5 nV/Hz would give a noise floor of around −144 dB/Hz. Clearly, increasing the drive level to the mixer will improve these results in proportion to the increased beat note derived from the mixer, provided that the reference source does not contribute any significant noise to the system.

The main drawbacks of the quadrature technique are that the signal sources have to be very stable, or a phase locked loop has to be used, and that the system calibration changes every time the recovered level from mixer is changed. There are methods of automating the measurements[3] but these techniques add significantly to the cost and the complexity of the system.

FM discriminator method

Marconi Instruments has used the f.m. discriminator technique shown in Fig. 5 for the last 7 years to check the phase noise characteristics of low noise signal generators. The outputs of the reference source and the signal generator are combined in a double balanced mixer to derive a nominal 1·5 MHz i.f. frequency. This is filtered to remove the unwanted components from the mixer and then amplified by a low noise amplifier before passing to a high gain limiting amplifier. This is followed by an f.m. discriminator that demodulates the spurious f.m. present in the 1·5 MHz i.f. The demodulated signal is then amplified and measured on a wave analyser.

The f.m. discriminator is designed such that it has a large change of output voltage with a small change of input frequency and has an f.m. bandwidth of 40 kHz. The high slope of the discriminator means that the i.f. frequency has to be tuned to within approximately 5 kHz of 1·5 MHz in order to remain in the linear portion of the discriminator characteristics. As an aid to this adjustment the tuned voltmeter that detects the i.f. level has a Q such that if the

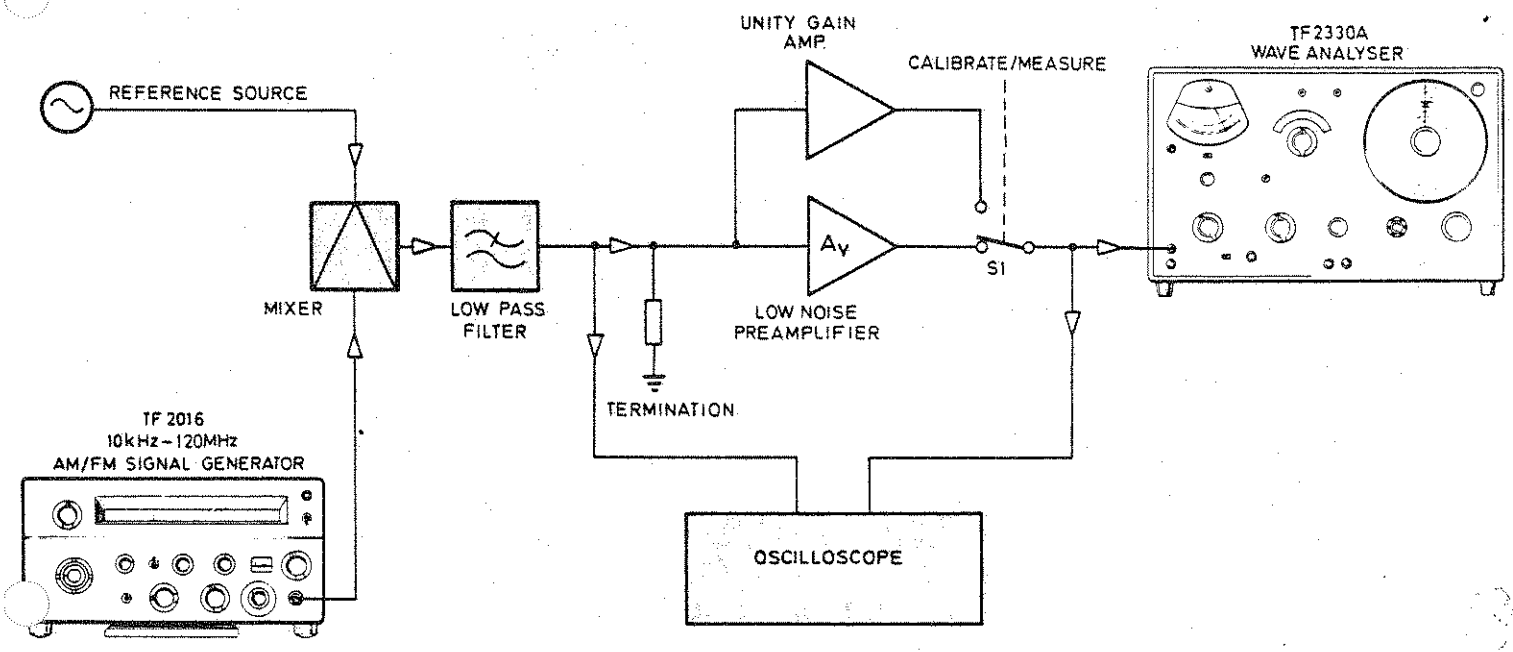


Fig. 4. Quadrature technique with a low noise preamplifier.

by removing the phase lock and measuring the amplitude

level recovered from the mixer since the limiter ensures that the drive level to the discriminator is always the same. Another advantage with this system is that when it is used for non-synthesized sources slow changes in the free running frequency of the generator will have no effect on the measurement accuracy provided that the drift is not sufficient to cause the l.f. frequency to drift outside the linear part of the discriminator characteristics.

When using the system it is important to realise that the demodulated output is the demodulated f.m. noise and not the phase noise and hence an additional correction factor is required which is dependent upon offset frequency.

The system is calibrated using a standardized f.m. source. With the amplifier gain set to unity the signal generator is replaced with an f.m. source modulated at 1 kHz to give 1 kHz deviation. The demodulated audio output is then

In practice, the system only has to have an occasional calibration check since all the factors above are dependent upon the system characteristics and not the r.f. input level. A table of correction factors is provided on the front panel of the instrument which gives correction figures for various offset frequencies of interest. The correction factors include the wave analyser characteristics and hence the phase noise of the signal generator is given by adding the correction factor for the offset frequency being measured to the measured output voltage in dB referred to a fixed datum level.

The input level to the wave analyser is monitored by an oscilloscope in order to ensure that the wave analyser is not overloaded. In this respect, however, the system has a further advantage over the quadrature technique. The lower

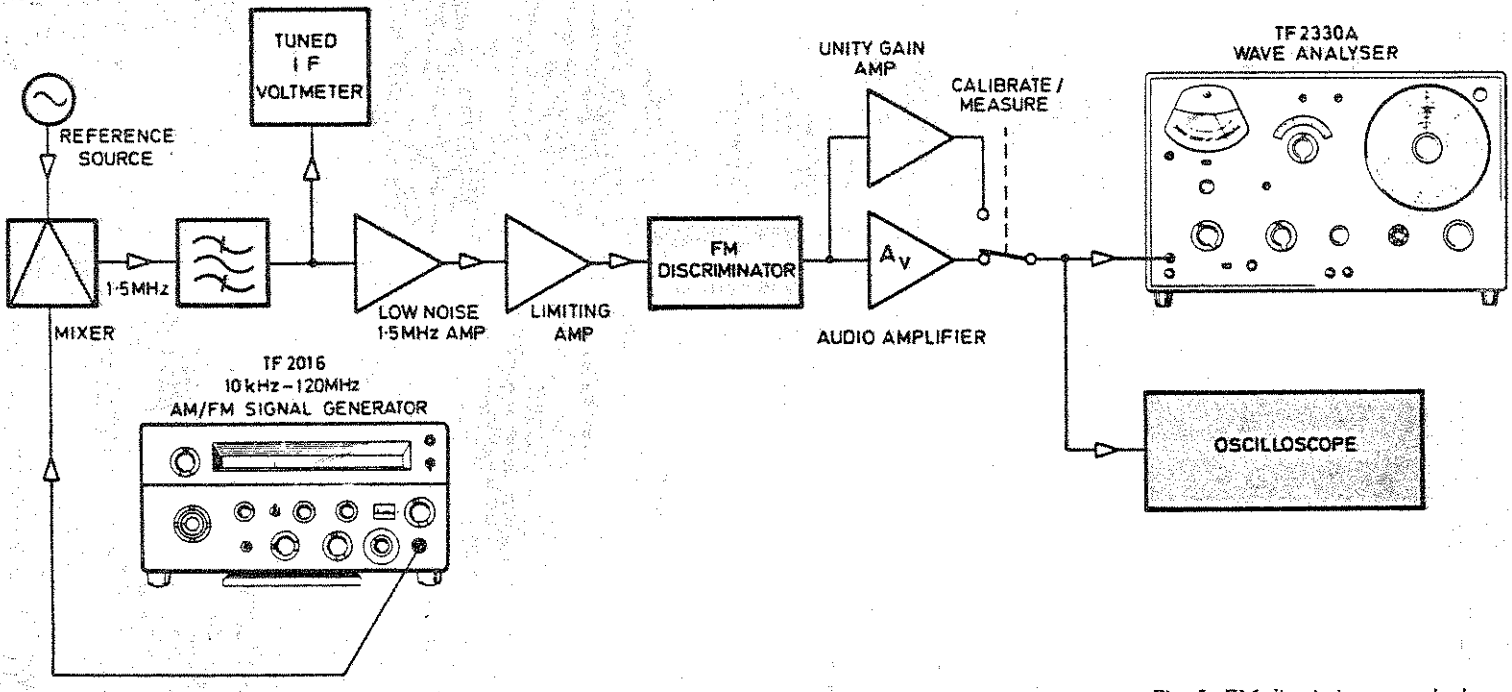


Fig. 5. FM discriminator method.

measured by the wave analyser. This level is again equivalent to a phase sideband at −6 dB. As in the quadrature method if a TF 2330A Wave Analyser is used there is a correction factor of +1·05 dB for the detector and −8·5 dB for the analyser bandwidth. In addition there is another correction factor dependent on the offset frequency being measured. The discriminator effectively has a linearly increasing phase gain as the offset frequency is increased. Hence the phase noise is given by the expression

$$N = -6 + 1{\cdot}05 - 10 \log B - A_V - 20 \log f_0/10^3 + 20 \log V_0/V_R \text{ dBc/Hz.}$$

where B is the noise bandwidth of the wave analyser,

A_V is the audio preamplifier gain,

f_0 is the offset frequency at which the noise is being measured,

V_0 is the measured output noise voltage,

and V_R is the output voltage measured in the calibration described previously.

frequency phase noise sidebands are not amplified as much as the high frequency components, by the discriminator, and hence the dynamic range required in the analyser is less. This can be an important advantage when measuring the characteristics of valve generators. Such sources frequently have very good phase noise characteristics at a 20 kHz offset but can have strong mains hum and low frequency phase noise components which could overload the measurement system.

If required, the output of the discriminator can be converted to be directly proportional to phase noise, as opposed to frequency noise, by using a suitable amplifier as shown in Fig. 6.

Measurement capability

The system noise floor of a discriminator system in use at Marconi Instruments is shown in Fig. 7 for a recovered i.f. level of 30 mV. The floor noise at 20 kHz offset is −153 dB and is due to the noise generated at the input to the 1·5 MHz amplifier. This low noise floor is fairly easily

signal generator frequency is tuned to obtain a peak reading on the i.f. voltmeter the i.f. frequency accuracy is adequate.

The calibration of the system is independent of the i.f.

If coherent signals are being measured the formula is reduced to

$$N = -6 - A_V - 20 \log f_0/10^3 + 20 \log V_0/V_R \text{ dBc/Hz}$$

signal generators is the phase noise at offset frequencies greater than 100 Hz from the carrier frequency and up to frequency offsets where the white noise of the amplifiers used contributes most of the noise. This amplifier noise floor should ideally be at least −140 dBc/Hz in a high quality signal generator and so any useful measurement system should have a residual noise floor of better than −150 dBc/Hz at offsets greater than 10 kHz.

It is technically not practical to measure this level of phase noise directly with a spectrum analyser because of the required dynamic range and so measurement techniques usually rely on first removing the carrier power.

There are two useful techniques for signal generator measurement – the quadrature and the f.m. discriminator method. Both of these systems rely on the availability of a reference source to effectively help to remove the carrier signal. In the following discussion it is assumed that the reference source contributes a negligible amount of phase noise to the signal generator. This is normally the case if a low noise crystal oscillator is used as the reference source.

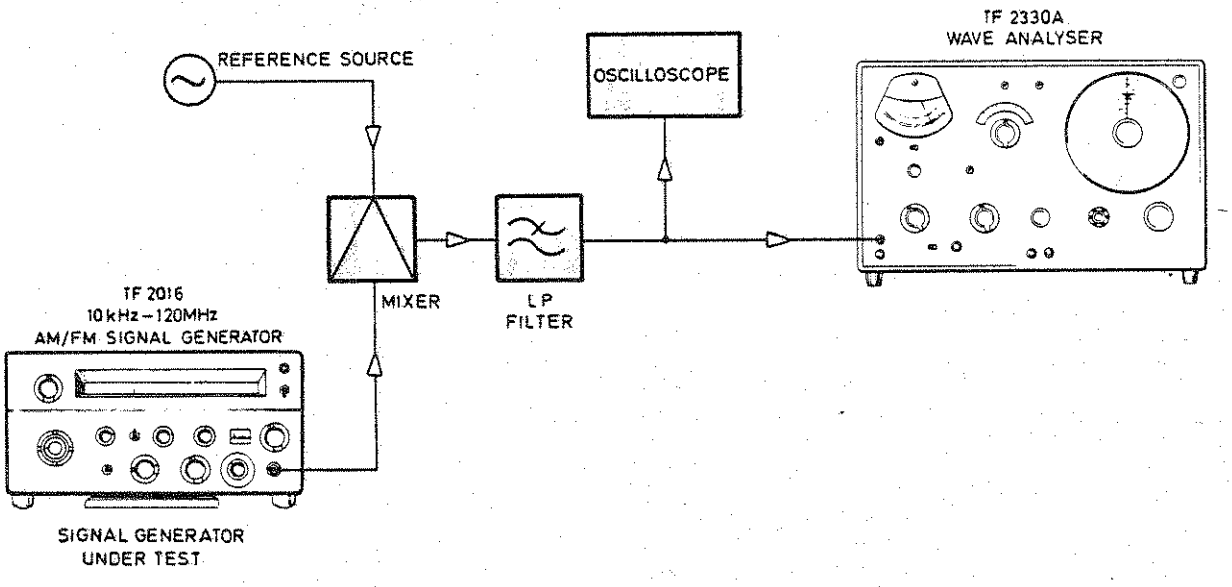


Fig. 2. Basic quadrature technique.

The quadrature technique

Fig. 2 shows the basic quadrature technique. The frequency source under test is mixed with a signal from a reference source in a double balanced mixer with a d.c. coupled output point. The output signal is then filtered to remove the high frequency signals from the mixer, amplified, if necessary, by an optional preamplifier and is then measured by a selective analyser such as a wave analyser or a spectrum analyser. The input frequencies to the mixer are adjusted such that the output from the mixer is a low frequency beat note. As the two frequencies are adjusted to be successively closer the output frequency from the mixer becomes lower until when the two frequencies are identical the output is just a d.c. level. If the two frequencies are in phase the d.c. level is a maximum and if they are in phase quadrature, i.e. 90° out of phase, the output level is approximately zero. The quadrature condition corresponds to the point at which the mixer is behaving as a phase detector since if the phase of one signal was changed by a small amount the d.c. level from the mixer would change. In a similar manner the in-phase condition corresponds to the mixer behaving as an amplitude detector. Clearly if the input signals are set to phase quadrature any phase noise on the signals would appear at the output of the mixer as a baseband noise signal and hence the selective analyser will measure a noise signal which is directly proportional to the phase noise of the source under test at an offset frequency corresponding to the frequency at which the selective analyser is set.

The system may be calibrated by offsetting the two input signals such that a beat note is generated at the output of the mixer. The r.m.s. beat note amplitude, V_B, is then measured by the selective analyser and this level is used as a reference level that is equivalent to a coherent phase sideband 6 dB below the carrier. This can be intuitively understood by noting that the peak voltage output from the mixer is equivalent to the phase sensitivity of the mixer at quadrature in radians/volt. Hence the beat note can be considered as corresponding to an equivalent narrow band phase modulation of 1 radian and narrow band modulation theory tells us that this is equivalent to a sideband level of −6 dB.

There are further correction factors which have to be taken into account for the selective analyser characteristics, which are dependent on the type of analyser used. If the TF 2330A Wave Analyser is used its bandwidth and detector characteristics must be accounted for. The detector uses an averaging technique which is calibrated to show the r.m.s. value of a sine wave. If the analyser is measuring a noise signal rather than a coherent sine wave it can be shown[1] that it is necessary to add 1·05 dB to the reading in order to

Measurement of phase noise

The most significant area of phase noise performance in

bandwidth. The wave analyser therefore gives a reading approximately 8·5 dB higher than the noise in a 1 Hz bandwidth. The meter indication on the wave analyser will exhibit a significant amount of jitter and so the meter indication has to be averaged visually or the meter movement has to be damped by adding capacitance in parallel. Alternatively a damped meter may be connected to the external monitor jack providing the constraints on loading the monitor are observed.

The TF 2370 Spectrum Analyser[2] may also be used as a tuned voltmeter. The noise bandwidth of the filter being used in the spectrum analyser should be checked if accurate noise measurements are required but generally the effective noise bandwidth of most analysers is approximately 15% greater than the 3 dB bandwidth of the filter. The correction factor for the bandwidth of the spectrum analyser is given by the general formula: $-10 \log B$
where B is the analyser noise bandwidth.

The detector correction factor for the 5, 50 and 500 Hz filters of the TF 2370 is the same as that for the wave analyser, i.e. +1·05 dB, provided that the analyser is used in the linear mode. If the analyser is used in the logarithmic mode the peaks of the noise waveform are effectively 'crushed' and the correction factor has to be changed to +2·5 dB.

TF 2370 should be used in the manual scan mode since in this mode a 1·5 Hz video filter is automatically incorporated. The frequency setting of the analyser may be manually scanned and a permanently stored display of the frequency characteristics of the phase noise sidebands is obtained. The internal frequency counter can also be used to accurately identify the frequency of any spurious signals that are present.

obtain the correct noise level. As the wave analyser noise bandwidth is approximately 7 Hz, it is necessary to weight the analyser reading to give the equivalent noise in a 1 Hz

For a wave analyser or a spectrum analyser in the linear mode the phase noise, N, at the offset frequency, f_0, of the analyser is

$$N = -6 + 1{\cdot}05 - 10 \log B + 20 \log V_0/V_B \text{ dBc/Hz}$$

where B is the analyser noise bandwidth,

V_0 is the measured output voltage from the mixer at phase quadrature,

and V_B is the measured beat note amplitude.

For coherent sidebands it is not necessary to correct for the analyser characteristics and the phase sideband level is given by

$$N = -6 + 20 \log V_0/V_B \text{ dBc/Hz}$$

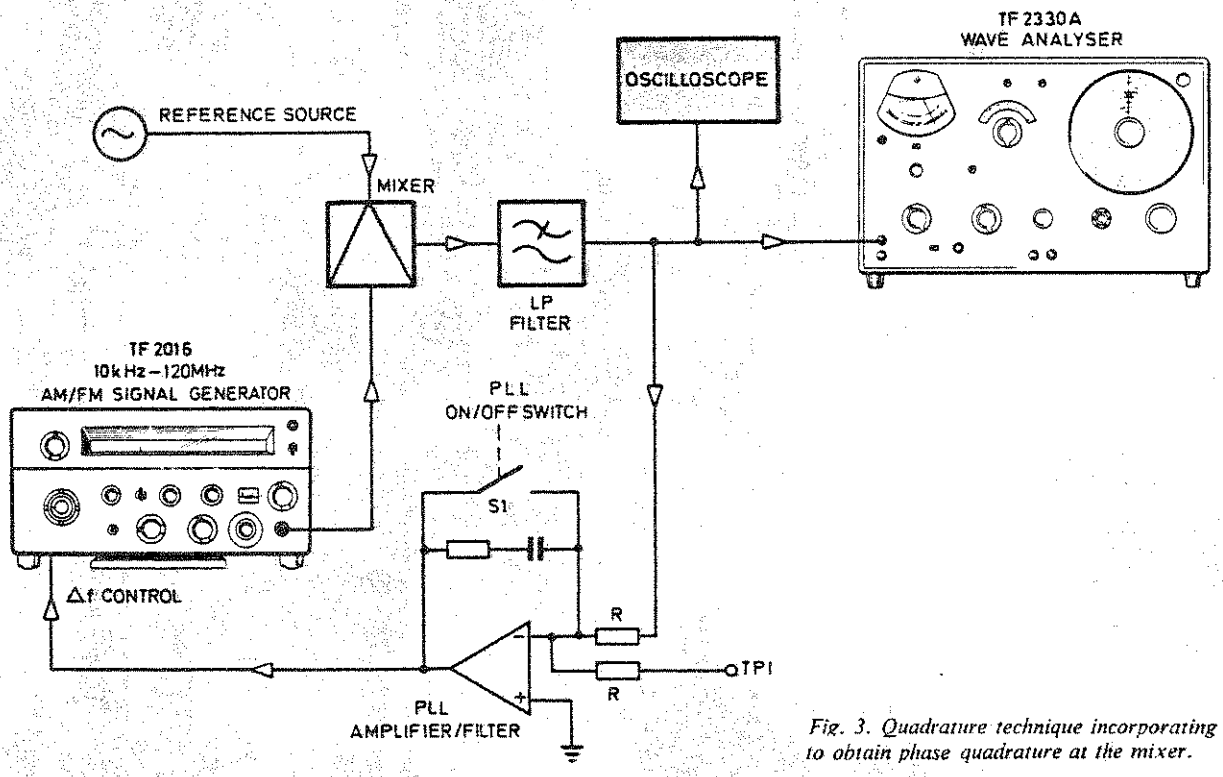


Fig. 3. Quadrature technique incorporating a p.l.l. to obtain phase quadrature at the mixer.

For a spectrum analyser in the logarithmic mode the phase noise is given by

$$N = -6 + 2{\cdot}5 - 10 \log B + 20 \log V_0/V_B \text{ dBc/Hz.}$$

Obtaining phase quadrature

The principal problem in using the quadrature technique for measurements on signal generators is to establish phase quadrature. Unless the generator has a synthesized frequency source it is unlikely that its frequency will remain in quadrature for a sufficient length of time for a measurement to be taken. If this is the case the only solution is to use a phase locked loop as shown in Fig. 3. The phase locked loop (p.l.l.) uses the electronic Δf control of the signal generator to control the output frequency of the generator. The phase locked loop bandwidth has to be designed to be significantly less than the lowest offset frequency at which the phase noise is to be measured since the loop will modify the in-band phase noise characteristics. The system is calibrated

Summary of calibration factors

In the quadrature method the required calibration factors can be summarized as follows.

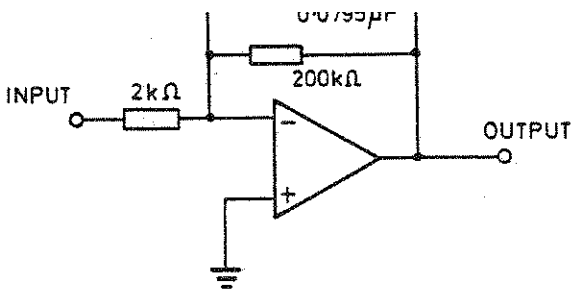


Fig. 6. An amplifier configuration capable of converting f.m. noise into phase noise. The gain at the calibration frequency of 1 kHz is unity and its lower 3 dB bandwidth is 10 Hz.

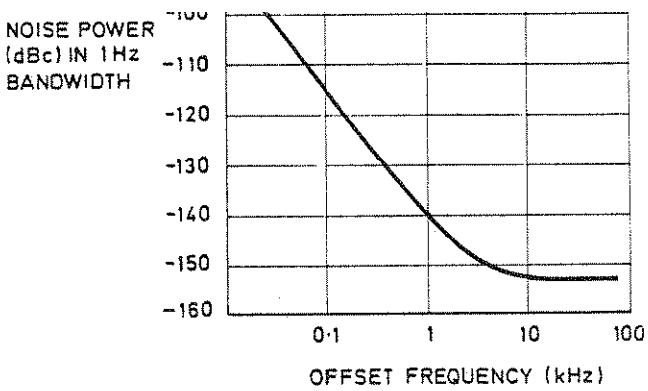


Fig. 7. Residual phase noise characteristics of the f.m. discriminator system used for a recovered i.f. level of 30 mV r.m.s. This was measured at r.f. input frequencies of 10 and 11·5 MHz, 140 and 141·5 MHz and 420 and 421·5 MHz using low noise crystal oscillators.

achieved since transformer techniques can be used to optimize the operating conditions of the amplifier. The audio amplifier after the discriminator is driven from a 100 kΩ source impedance, which is the output impedance of the discriminator, and as a result a j.f.e.t. source follower followed by an operational amplifier, such as the μA 741, is perfectly adequate for recovering the output signal. The high gain of the discriminator ensures that the noise performance of the amplifier is not critical.

The noise floor at 20 kHz is directly dependent upon the i.f. level but below 1 kHz it is independent of i.f. level for levels greater than 15 mV. Its source is believed to be in either the discriminator or the limiters but so far no attempt has been made to minimize it since the noise floor is more than adequate for signal generator applications.

The principal limitation on the technique is that the offset frequency that can be measured is limited to 40 kHz by the f.m. bandwidth of the discriminator. However, in many applications this does not reduce the usefulness of the system.

References

1. Broderick, P.: 'Noise measurements with electronic voltmeters'; *Marconi Instrumentation*, August 1965, 10, p.18.

2. Middleton, J. D. et al: '110 MHz Spectrum Analyser'; *Marconi Instrumentation*, December 1973, 14, p.50.

3. Lance, A. L. et al: 'Automated phase noise measurements'; *Microwave Journal*, June 1977, 20, No. 6, p.87.

Chapter 6

REPLACEABLE PARTS

CONTENTS

INTRODUCTION

1. Each sub-assembly or printed circuit board in this equipment has been allocated a reference designator code, e.g. A0, A1, A2 etc.

2. The complete component reference includes its reference designator as a prefix e.g. A2C1 (capacitor C1 on sub-assembly A2) but for convenience in the text and diagrams the prefix is omitted unless it is needed to avoid confusion. However when ordering replacements or in correspondence the complete component reference must be quoted.

3. Electrical components are listed in alpha-numerical order of their complete circuit reference and the following standard abbreviations are used in the 'Description' column :

ADC	analogue-digital converter
CAP	capacitor
CARR	carrier
CARB	carbon
CC	carbon composition
CDE CNV	code converter
CER	ceramic
CERM	cermet
CF	carbon film
COAX	coaxial
CON	connector
CTR	counter
DAC	digital-analogue converter
DEC/DMX	decoder/demultiplexer
DECOD	decoder
DIL	dual in-line
DIV	divider
DRIV	driver
ELEC	electrolytic
ENCOD	encoder
FEM	female
FF	flip-flop (bistable)
FILTERCON	filtering capacitor
GER	germanium
GP	general purpose
ICA	integrated circuit, analogue
ICD	integrated circuit, digital
IND	inductor
INV	inverter
LD/T	lead through
MF	metal film
MG	metal glaze
MISC	miscellaneous
MO	metal oxide
MP	microprocessor
MP SUPP	microprocessor support
MUX	multiplexer
NET	network
PC	polycarbonate
PETP	(polyester)polyethelene terephthalate
PS	polystyrene
PLL	phase-locked loop

Q/ACT	quick acting
RECT	rectifier
RES	resistor
RV	resistor, variable
RX	receiver
SAPPH	sapphire
SEC	secondary
SH REG	shift register
SIL	silicon
SW	switch
T/LAG	time lag
TANT	tantalum
TOG	toggle
TRANS	transistor
TX	transmitter
VAR	variable
VREG	voltage regulator
W	watts at 70^0C
WW	wirewound
X	miscellaneous item
XL	crystal
!	static sensitive component
% +	asymmetric tolerance

COMPONENT VALUES

4. One or more of the components fitted in the equipment may differ from those listed in this chapter for any of the following reasons:

(a) Components indicated by a * have their values selected during test to achieve particular performance limits.

(b) Owing to supply difficulties, components of different value or type may be substituted provided the overall performance of the equipment is maintained.

(c) As part of a policy of continuous development, components may be changed in value or type to obtain detail improvements in performance.

5. When there is a difference between the component fitted and the one listed, always use as a replacement the same type and value as found in the equipment.

6. When ordering replacements, address the order to our Service Division (address on rear cover) or nearest agent and specify the following for each component required:-

(1) Type# and serial number of equipment.

(2) Complete circuit reference.

(3) Description.

(4) Part number.

#As given on the serial number label at the rear of the equipment; if this is superseded by a model number label, quote the model number instead of the type number.

Circuit Ref	Description	Part Number

ELECTRICAL COMPONENTS

Unit AA0/1 - RF BOX 1 AA/B0/1 (44990-489T)

7. When ordering, prefix circuit reference with AA0/1

C1	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C2	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C3	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C4	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C5	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C6	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C7	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C8	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C9	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C10	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C11	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C12	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C13	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C14	CAP CER 1NO 300V 20%+ L/T SOL	26273-733K
C15	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C16	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C17	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C18	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C19	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C20	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C21	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C22	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C23	CAP CER 50PF 300V 10%+ L/T SOL	26333-229U
C24	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C25	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C26	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C27	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C28	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C29	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C30	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C31	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C32	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C33	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C34	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C35	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K

Circuit Ref	Description	Part Number
Unit AA0/1	- RF BOX 1 AA/B0/1 (continued)	
C36	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C37	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C38	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C39	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C40	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C41	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C42	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C43	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C44	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C45	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C46	CAP CER 50PF 300V 10%+ L/T SOL	26333-229U
C47	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C48	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C49	CAP CER 50PF 300V 10%+ L/T SOL	26333-229U
C50	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C51	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C52	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C53	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C54	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C55	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C56	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C57	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C58	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C59	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C60	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C61	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C62	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C63	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C64	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C65	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C66	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
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C70	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C71	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C72	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C73	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C74	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C75	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K

Circuit Ref	Description	Part Number
Unit AA0/1	- RF BOX 1 AA/B0/1 (continued)	
C76	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C77	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C78	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C79	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C80	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C81	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C82	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C83	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C84	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C85	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C86	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C87	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C88	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
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C102	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C103	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C104	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C105	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C106	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C107	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C108	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C109	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C111	CAP CER 1NO 500V 20%+ L/T SCR	26373-714F
C112	CAP CER 1NO 500V 20%+ L/T SCR	26373-714F
C113	CAP CER 1NO 500V 20%+ L/T SCR	26373-714F
C114	CAP CER 1NO 500V 20%+ L/T SCR	26373-714F
C115	CAP CER 1NO 500V 20%+ L/T SCR	26373-714F
C116	CAP CER 1NO 500V 20%+ L/T SCR	26373-714F

Circuit Ref	Description	Part Number
Unit AA0/1	- RF BOX 1 AA/B0/1 (continued)	
C117	CAP CER 1N0 500V 20%+ L/T SCR	26373-714F
C118	CAP CER 1N0 500V 20%+ L/T SCR	26373-714F
C121	CAP ELEC 47U 10V 20%+ AX	26415-809E
C122	CAP PETP 220N 63V 10% RAD MIN	26582-430L
C123	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C124	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C125	CAP CER 1N0 100V 5% PLATE	26343-556X
C126	CAP CER 1N0 100V 5% PLATE	26343-556X
C127	CAP CER 1N0 100V 5% PLATE	26343-556X
C128	CAP CER 100N 100V 20%+ M/LAYER	26383-532E
IC1	ICA VREG+ 7805 5V 1A TO220	28461-707G
L1	IND CHOKE 100UH 10% LAQ	23642-561W
L2	IND CHOKE 100UH 10% LAQ	23642-561W
L3	IND CHOKE 100UH 10% LAQ	23642-561W
L4	IND CHOKE 100UH 10% LAQ	23642-561W
L5	IND CHOKE 100UH 10% LAQ	23642-561W
L6	IND CHOKE 100UH 10% LAQ	23642-561W
L7	IND CHOKE 100UH 10% LAQ	23642-561W
L8	IND CHOKE 100UH 10% LAQ	23642-561W
L9	IND CHOKE 100UH 10% LAQ	23642-561W
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L12	IND CHOKE 100UH 10% LAQ	23642-561W
L13	IND CHOKE 100UH 10% LAQ	23642-561W
L14	IND CHOKE 100UH 10% LAQ	23642-561W
L15	IND CHOKE 100UH 10% LAQ	23642-561W
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L26	IND CHOKE 100UH 10% LAQ	23642-561W
L27	IND CHOKE 100UH 10% LAQ	23642-561W
L28	IND CHOKE 100UH 10% LAQ	23642-561W
L29	IND CHOKE 100UH 10% LAQ	23642-561W
L30	IND CHOKE 100UH 10% LAQ	23642-561W
L31	IND CHOKE 100UH 10% LAQ	23642-561W
L32	IND CHOKE 100UH 10% LAQ	23642-561W

Circuit Ref	Description	Part Number
Unit AA0/1	- RF BOX 1 AA/B0/1 (continued)	
L45	IND CHOKE 100UH 10% LAQ	23642-561W
L46	IND CHOKE 100UH 10% LAQ	23642-561W
PLBW	CABLE COAX 17CM SMB-FM/SMB-FM	43129-692X
PLBX	CABLE COAX 28CM SMC-ML/SMB-FEM	43129-664B
R1	RES MF 100R 1/4W 2% 100PPM	24773-249J
R2	RES MF 100R 1/4W 2% 100PPM	24773-249J
R5-R36	RES MF 220R 1/4W 2% 100PPM	24773-257W
SKK	CON ASSY SKK	43129-647G
SKL	CABLE WIR 92CM 1 MIN-1ROW-2P/-	43129-651V
SKX	CABLE RIB 87CM 16 IDC-FM-DIL/-	43129-650G
SKZ	CABLE WIR 91CM 3 MIN-1ROW-3P/-	43129-644L
SKBC	CABLE RIB .2M 16 IDC-FEM-DIL/-	43129-669E
SKBD	CABLE RIB 13CM 14 IDC-FM-DIL/-	43129-671H
SKBE	CABLE RIB .1M 16 IDC-FEM-DIL/-	43129-670Z
SKBF	CABLE RIB 13CM 14 IDC-FM-DIL/-	43129-671H
SKBH	CABLE RIB 13CM 14 IDC-FM-DIL/-	43129-671H
SKBJ	CABLE RIB 13CM 14 IDC-FM-DIL/-	43129-671H
SKBK	CABLE WIR 27CM 8 MIN-1ROW-8P/-	43129-659C
SKBM	CON ASSY SKBM-SKBP	43130-191N
SKBN	CABLE COAX 23CM 1ROW-3P/MN-SKT	43129-661M
SKBS	CABLE RIB 13CM 14 IDC-FM-DIL/-	43129-671H
SKBT	CABLE COAX 23CM 1ROW-3P/SMB-FM	43129-663R
SKBU	CABLE COAX 22CM MIN-1ROW-3PX2	43129-662C
SKBV	CABLE RIB 13CM 14 IDC-FM-DIL/-	43129-671H
SKBY	CABLE RIB 12CM 14 IDC-FM-DIL/-	43129-678F
SKBZ	CABLE RIB 13CM 14 IDC-FM-DIL/-	43129-671H
SKCC	CABLE COAX 12CM MIN-1ROW-3PX2	43129-665K
SKCD	CABLE COAX 33CM MIN-SKTX1/-	43129-693M
SKCE	CABLE WIR 0.1M 4 MIN-1ROW-5P/-	43129-666A
SKCJ	CABLE COAX 33CM MIN-SKTX1/-	43129-693M
SKCK	CABLE COAX 14CM 1ROW-3P/SMB-FM	43129-667Z
SKDH	CON RF SMB MALE 50 BKHD SOLDER	23444-331H
SKDJ	CON RF SMB MALE 50 BKHD SOLDER	23444-331H
SKDL	CON RF SMB MALE 50 BKHD SOLDER	23444-331H
X11	FERRITE BEAD	41372-006T
X12	FERRITE BEAD	41372-006T
X13	FERRITE BEAD	41372-006T
X14	FERRITE BEAD	41372-006T
X15	FERRITE BEAD	41372-006T
X16	FERRITE BEAD	41372-006T
X17	FERRITE BEAD	41372-006T
X131	CON PART MIN HOUSING 1ROW 3P	23435-171R
X310	CON PART MIN HOUSING 1ROW 3P	23435-171R

Circuit Ref	Description	Part Number
Unit AA1	- LSD LOOP AA1	
8. When ordering, prefix circuit reference with AA1		
	Complete unit	44828-426W
C1	CAP PETP 100N 100V 10% RAD	26582-211B
C2	CAP PETP 1U0 100V 10% RAD	26582-217U
C3	CAP CER 470P 63V 10% PLATE	26383-582T
C4	CAP CER 10N 100V 20%+ DISC	26383-055L
C5	CAP CER 10N 100V 20%+ DISC	26383-055L
C6	CAP ELEC 470N 50V 20% SUBMIN	26421-104C
C7	CAP ELEC 470N 50V 20% SUBMIN	26421-104C
C8	CAP CER 10N 100V 20%+ DISC	26383-055L
C9	CAP CER 10N 100V 20%+ DISC	26383-055L
C10	CAP CER 10N 100V 20%+ DISC	26383-055L
C11	CAP CER 10N 100V 20%+ DISC	26383-055L
C12	CAP CER 10N 100V 20%+ DISC	26383-055L
C13	CAP CER 10N 100V 20%+ DISC	26383-055L
C14	CAP CER 10N 100V 20%+ DISC	26383-055L
C15	CAP CER 10N 100V 20%+ DISC	26383-055L
C16	CAP CER 10N 100V 20%+ DISC	26383-055L
C17	CAP CER 10N 100V 20%+ DISC	26383-055L
C18	CAP CER 10N 100V 20%+ DISC	26383-055L
C19	CAP CER 10N 100V 20%+ DISC	26383-055L
C20	CAP CER 10N 100V 20%+ DISC	26383-055L
C21	CAP CER 10N 100V 20%+ DISC	26383-055L
C22	CAP CER 10N 100V 20%+ DISC	26383-055L
C23	CAP CER 10N 100V 20%+ DISC	26383-055L
C24	CAP CER 1N5 63V 10% PLATE	26383-593A
C25	CAP PETP 220N 63V 10% RAD MIN	26582-430L
C26	CAP CER 10N 100V 20%+ DISC	26383-055L
C27	CAP CER 1N0 63V 10% PLATE	26383-585M
C28	CAP CER 47P 63V 5% PLATE	26343-473L
D1	DI V/CAP MVAM125 1V 500PF	28381-340V
D2	DI SIL 1N4148 75V JUNC	28336-676J
D3	DI SIL 1N4148 75V JUNC	28336-676J
D4	DI H/CARR HP5082-2835	28349-006H
IC1	ICD FF D 74LS74 DUAL +EDG TR	28462-611A
IC2	ICD NAND 74LS10 TRIP 3INP	28466-351Y
IC3	ICD CTR 74LS160 4BIT DEC PRE	28464-123P
IC4	ICD CTR 74LS160 4BIT DEC PRE	28464-123P
IC5	ICD CTR 74LS160 4BIT DEC PRE	28464-123P

Circuit Ref	Description	Part Number
Unit AA1	- LSD LOOP AA1 (continued)	
IC6	ICD CTR 74LS160 4BIT DEC PRE	28464-123P
IC7	ICD CTR 74LS160 4BIT DEC PRE	28464-123P
IC8	ICD FF D 74LS273 OCT +EDG TR	28462-615U
IC9	ICD FF D 74LS273 OCT +EDG TR	28462-615U
IC10	ICD FF D 74LS273 OCT +EDG TR	28462-615U
IC11	ICD FF D 74LS273 OCT +EDG TR	28462-615U
IC12	ICD CTR 74LS160 4BIT DEC PRE	28464-123P
IC13	ICD CTR 74LS160 4BIT DEC PRE	28464-123P
IC14	ICD CTR 74LS160 4BIT DEC PRE	28464-123P
IC15	ICD CTR 74LS160 4BIT DEC PRE	28464-123P
IC16	ICD NAND 74S133 13INP	28466-357V
IC17	ICD NAND 74S133 13INP	28466-357V
L1	IND CHOKE .47UH 10% LAQ	23642-547Y
L2	IND CHOKE .47UH 10% LAQ	23642-547Y
R1	RES MF 6K8 1/4W 2% 100PPM	24773-293D
R2	RES MF 2K2 1/4W 2% 100PPM	24773-281Y
R3	RES MF 3K3 1/4W 2% 100PPM	24773-285F
R4	RES MF 1KO 1/4W 2% 100PPM	24773-273A
R5	RES MF 2K2 1/4W 2% 100PPM	24773-281Y
R6	RES MF 3KO 1/4W 2% 100PPM	24773-284J
R7	RES MF 1KO 1/4W 2% 100PPM	24773-273A
R8	RES RV CERM 1KO LIN .5W 10% HORZ	25711-638G
R9	RES MF 3K9 1/4W 2% 100PPM	24773-287V
R10	RES MF 3K6 1/4W 2% 100PPM	24773-286G
R11	RES MF 1KO 1/4W 2% 100PPM	24773-273A
TR1	TR NSI BC209C 20V 150M - GEN	28452-771P
TR2	TR PSI BC308B 20V 130M - GEN	28433-455R
TR3	TR NSI BC209C 20V 150M - GEN	28452-771P
X6	CON JUMP FEM 2 1 ROW	23435-990X
Unit AA2/1	- MICROPROCESSOR SYSTEM	
9. When ordering, prefix circuit reference with AA2/1		
	Complete unit	44828-801F
C1	CAP CER 100N 30V 20% DISC	26383-031S
C2	CAP CER 100N 30V 20% DISC	26383-031S
C3	CAP CER 100N 30V 20% DISC	26383-031S
C4	CAP CER 100N 30V 20% DISC	26383-031S
C11	CAP ELEC 4U7 35V 20% SUBMIN	26421-108A

Circuit Ref	Description			Part Number
Unit AA2/1	- MICROPROCESSOR SYSTEM (continued)			
C12	CAP ELEC 100U 25V 20%+ PCB			26423-243M
C13	CAP ELEC 100U 25V 20%+ PCB			26423-243M
C14	CAP ELEC 100U 25V 20%+ PCB			26423-243M
C15	CAP ELEC 100U 25V 20%+ PCB			26423-243M
C16	CAP CER 10N 100V 20%+ DISC			26383-055L
C17	CAP CER 10N 100V 20%+ DISC			26383-055L
C18	CAP CER 10N 100V 20%+ DISC			26383-055L
C19	CAP CER 10N 100V 20%+ DISC			26383-055L
C20	CAP ELEC 100U 25V 20%+ PCB			26423-243M
C21	CAP CER 10N 100V 20%+ DISC			26383-055L
C23	CAP CER 10N 100V 20%+ DISC			26383-055L
C25	CAP CER 10N 100V 20%+ DISC			26383-055L
C26	CAP CER 10N 100V 20%+ DISC			26383-055L
C28	CAP CER 10N 100V 20%+ DISC			26383-055L
C29	CAP CER 10N 100V 20%+ DISC			26383-055L
C31	CAP ELEC 4U7 35V 20% SUBMIN			26421-108A
D1	DI SIL 1N4148 75V JUNC			28336-676J
D2	DI ZEN 1N825/A 6.2V 5%			28371-494Z
IC1	ICD PROM 2764 8KX8 250NS UV		!	
IC2	ICD PROM 2764 8KX8 250NS UV	} Set of 4	!	44533-184S
IC3	ICD PROM 2764 8KX8 250NS UV		!	
IC4	ICD PROM 2764 8KX8 250NS UV		!	
IC9	ICD MP P8085A 8BIT NMOS		!	28469-396K
IC10	ICD BUFF 74LS245 OCT TXRX			28469-188B
IC11	ICD BUFF 74LS244 OCT 3ST			28469-182T
IC12	ICD MP SUP 8155 2KRAM+I/O+TIM		!	28469-304E
IC13	ICD DEC/DMX 74LS138 3-8			28465-027F
IC14	ICD PROM 2817A-2 2KX8 EA DIL28		!	28471-025D
IC17	ICD DEC/DMX 74LS138 3-8			28465-027F
IC18	ICD RAM HM6116P-4 2KX8 200NS		!	28469-307N
IC19	ICA AMP TL071CP DUAL FET I/P			28461-347A
IC20	ICD FF D 74LS273 OCT +EDG TR			28462-615U
IC21	ICD LATCH 74LS373 OCT 3ST			28462-410E
IC23	ICD CTR 74LS393 DUAL 4BIT BIN			28464-130R

Circuit Ref	Description	Part Number
Unit AA2/1	- MICROPROCESSOR SYSTEM (continued)	
R1	RES MF 10K 1/4W 2% 100PPM	24773-297M
R2	RES MF 10K 1/4W 2% 100PPM	24773-297M
R3	RES MF 47K 1/4W 2% 100PPM	24773-313H
R4	RES MF 10K 1/4W 2% 100PPM	24773-297M
R6	RES MF 3KO 1/4W 2% 100PPM	24773-284J
R7	RES MF 1KO 1/4W 2% 100PPM	24773-273A
R8	RV CERM 1KO LIN .5W 10% HORZ	25711-638G
R9	RES MF 3K9 1/4W 2% 100PPM	24773-287V
R14	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R15	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R16	RES MF 1KO 1/4W 2% 100PPM	24773-273A
R17	RES MF 3KO 1/4W 2% 100PPM	24773-284J
R18	RES MF 3KO 1/4W 2% 100PPM	24773-284J
R24	RES MF 10K 1/4W 2% 100PPM	24773-297M
R25	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R26	RES MF 10K 1/4W 2% 100PPM	24773-297M
TR2	TR NSI BC208B 20V 150M - GEN	28452-781A
X4	CON JUMP FEM 2 1 ROW	23435-990X
X5	S/C ACC SKT DIL40 LOW PROFILE	28488-046J
X6	S/C ACC SKT DIL24 LOW PROFILE	28488-044N
X7	S/C ACC SKT DIL28 LOW PROFILE	28488-045L
XL1	XTAL 6.144M P30P 75R	28312-054J
Unit AA3/2	- FREQUENCY STANDARD AA3/2	
10. When ordering, prefix circuit reference with AA3/2		
	Complete unit	44828-873D
C1	CAP ELEC 10U 35V 20% SUBMIN	26421-112Z
C2	CAP PETP 10N 63V 10% RAD MIN	26582-426N
C3	CAP CER 220P 63V 2% PLATE	26343-481S
C4	CAP CER 10N 25V 20% DISC	26383-006C
C5	CAP CER 220P 63V 2% PLATE	26343-481S
C6	CAP CER 10N 25V 20% DISC	26383-006C
C7	CAP CER 10N 25V 20% DISC	26383-006C
C8	CAP CER 10N 25V 20% DISC	26383-006C
C9	CAP CER 10N 25V 20% DISC	26383-006C
C11	CAP CER 10N 25V 20% DISC	26383-006C

Circuit Ref	Description	Part Number
Unit AA3/2	- FREQUENCY STANDARD AA3/2 (continued)	
C12	CAP ELEC 4U7 35V 20% SUBMIN	26421-108A
C13	CAP CER 1NO 63V 10% PLATE	26383-585M
C14	CAP CER 10N 25V 20% DISC	26383-006C
C15	CAP CER 10N 25V 20% DISC	26383-006C
C16	CAP CER 10N 25V 20% DISC	26383-006C
C17	CAP CER 10N 25V 20% DISC	26383-006C
C18	CAP CER 10N 25V 20% DISC	26383-006C
C19	CAP ELEC 10U 35V 20% SUBMIN	26421-112Z
C20	CAP PS 820P 63V 1% RAD	26538-900J
C21	CAP CER 15P 63V 5% PLATE	26343-467U
C22	CAP CER 15P 63V 5% PLATE	26343-467U
C23	CAP PS 820P 63V 1% RAD	26538-900J
C24	CAP CER 15P 63V 5% PLATE	26343-467U
C25	CAP CER 15P 63V 5% PLATE	26343-467U
D1	DI SIL 1N4148 75V JUNC	28336-676J
D2	DI SIL 1N4148 75V JUNC	28336-676J
D3	DI ZEN 1N825/A 6.2V 5%	28371-494Z
D4	DI SIL BA482 35V JUNC	28335-675R
D5	DI SIL HP5082-2835	28349-006H
IC1	ICD NAND 74LS00 QUAD 2INP	28466-345H
IC2	ICA COMP LM339N QUAD	28461-693H
IC3	ICD FF D 74LS74 DUAL +EDG TR	28462-611A
IC4	ICD CTR 74LS390 DUAL 4BIT DEC	28464-127R
IC5	ICD MUX 74LS157 QUAD 2INP	28469-707B
IC6	ICD MONO 74LS122 RETR	28468-310C
IC7	ICD DRIV 74128 QUAD 2NOR 50OHM	28466-224S
IC8	ICD CTR 74LS390 DUAL 4BIT DEC	28464-127R
IC9	ICD CTR 74LS90 4BIT DEC 2,5,10	28464-014S
L1	IND CHOKE .33UH 10% LAQ	23642-546U
L2	IND CHOKE .33UH 10% LAQ	23642-546U
R1	RES MF 33K 1/4W 2% 100PPM	24773-309Z
R2	RES MF 1K1 1/4W 2% 100PPM	24773-274Z
R3	RV CERM 10K LIN .5W 10% BKHD	25748-518H
R4	RES MF 1KO 1/4W 2% 100PPM	24773-273A
R5	RES MF 1KO 1/4W 2% 100PPM	24773-273A
R6	RES MF 150R 1/4W 2% 100PPM	24773-253F
R7	RES MF 10K 1/4W 2% 100PPM	24773-297M
R8	RES MF 150R 1/4W 2% 100PPM	24773-253F
R9	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R11	RES MF 150R 1/4W 2% 100PPM	24773-253F

Circuit Ref	Description	Part Number
Unit AA3/2	- FREQUENCY STANDARD AA3/2 (continued)	
R12	RES MF 100R 1/4W 2% 100PPM	24773-249J
R13	RES MF 2K7 1/4W 2% 100PPM	24773-283L
R14	RES MF 1KO 1/4W 2% 100PPM	24773-273A
R15	RES MF 10K 1/4W 2% 100PPM	24773-297M
R16	RES MF 150R 1/4W 2% 100PPM	24773-253F
SKAR	CON RF SMB MALE 50 PCB ELBOW	23444-359Z
SKAU	CON RF SMB MALE 50 PCB ELBOW	23444-359Z
TR1	TR NSI BC209C 20V 150M - GEN	28452-771P
TR2	TR PSI BC308B 20V 130M - GEN	28433-455R
TR3	TR NSI BC209C 20V 150M - GEN	28452-771P
XL1	XTAL 10M P30P 20R	28312-047U
XL2	XTAL 10M P30P 20R	28312-047U
	10 MHZ OSCILLATOR (HS) OCXO	44990-418V
Unit AB1	- OUTPUT LOOP VRD AB1	
11. When ordering, prefix circuit reference with AB1		
	Complete unit	44828-429P
C1	CAP CER 1NO 63V 10% PLATE	26383-585M
C2	CAP CER 10N 100V 20%+ DISC	26383-055L
C3	CAP CER 1NO 63V 10% PLATE	26383-585M
C4	CAP CER 1NO 63V 10% PLATE	26383-585M
C5	CAP CER 1NO 63V 10% PLATE	26383-585M
C6	CAP CER 1NO 63V 10% PLATE	26383-585M
C7	CAP CER 10N 100V 20%+ DISC	26383-055L
C8	CAP CER 10N 100V 20%+ DISC	26383-055L
C9	CAP CER 10N 100V 20%+ DISC	26383-055L
C10	CAP CER 10N 100V 20%+ DISC	26383-055L
C11	CAP CER 10N 100V 20%+ DISC	26383-055L
C12	CAP CER 10N 100V 20%+ DISC	26383-055L
C13	CAP CER 10N 100V 20%+ DISC	26383-055L
C14	CAP CER 10N 100V 20%+ DISC	26383-055L
C15	CAP CER 10N 100V 20%+ DISC	26383-055L
C16	CAP CER 10N 100V 20%+ DISC	26383-055L
C17	CAP CER 10N 100V 20%+ DISC	26383-055L
C18	CAP CER 2P2 63V .5PF PLATE	26343-457R
C19	CAP ELEC 22U 25V 20% SUBMIN	26421-114E
D1	DI SIL 1N4148 75V JUNC	28336-676J
D4	DI SIL 1N4148 75V JUNC	28336-676J

Circuit Ref	Description	Part Number
Unit AB1	- OUTPUT LOOP VRD AB1 (continued)	
IC1	ICD DIV SP8607BCM/2 600MHZ	28462-023B
IC2	ICD DIV SP8647B/10,11 TTL O/P	28464-015W
IC3	ICD NAND 74S00N QUAD 2INP	28466-331D
IC4	ICD FF D 74LS273 OCT +EDG TR	28462-615U
IC5	ICD FF D 74LS273 OCT +EDG TR	28462-615U
IC6	ICD CTR 74LS196 4BIT DEC PRE	28464-016D
IC7	ICD CTR 74196 4BIT DEC PR	28464-004Y
IC8	ICD CTR 74LS196 4BIT DEC PRE	28464-016D
IC9	ICD CTR 74LS196 4BIT DEC PRE	28464-016D
IC10	ICD FF D 74S74 DUAL +EDG TR	28462-607K
IC11	ICD FF JK 74S112 DUAL -EDG TR	28462-015P
IC12	ICD NAND 74S133 13INP	28466-357V
R1	RES CC 51R 1/8W 5%	24331-989P
R2	RES MF 10K 1/4W 2% 100PPM	24773-297M
R3	RES MF 1K8 1/4W 2% 100PPM	24773-279N
R4	RES CC 22R 1/8W 5%	24331-988T
R5	RES CC 100R 1/8W 5%	24331-997B
R6	RES MF 20K 1/4W 2% 100PPM	24773-304C
R7	RES MF 2K7 1/4W 2% 100PPM	24773-283L
R8	RES MF 1K5 1/4W 2% 100PPM	24773-277U
R9	RES MF 91R 1/4W 2% 100PPM	24773-248L
R10	RES MF 750R 1/4W 2% 100PPM	24773-270R
R11	RES MF 1K5 1/4W 2% 100PPM	24773-277U
R12	RES MF 680R 1/4W 2% 100PPM	24773-269K
R13	RES MF 2K2 1/4W 2% 100PPM	24773-281Y
R14	RES MF 2K2 1/4W 2% 100PPM	24773-281Y
TR1	TR NSI BFR90 15V 5G - AMP	28452-167U
X3	S/C ACC PAD TO5 TO DIL8	28488-102R
Unit AB2	- DIVIDE-BY-TWO CHAIN & FM DRIVE	
12. When ordering, prefix circuit reference with AB2		
	Complete unit	44828-430D
C1	CAP CER 1N0 63V 10% PLATE	26383-585M
C2	CAP CER 1N0 63V 10% PLATE	26383-585M
C3	CAP CER 1N0 63V 10% PLATE	26383-585M
C4	CAP CER 10N 100V 20%+ DISC	26383-055L
C5	CAP CER 10N 100V 20%+ DISC	26383-055L

Circuit Ref	Description	Part Number
Unit AB2	- DIVIDE-BY-TWO CHAIN & FM DRIVE (continued)	
C6	CAP CER 1NO 63V 10% PLATE	26383-585M
C7	CAP CER 10N 100V 20%+ DISC	26383-055L
C8	CAP CER 1NO 63V 10% PLATE	26383-585M
C9	CAP CER 1NO 63V 10% PLATE	26383-585M
C10	CAP CER 1NO 63V 10% PLATE	26383-585M
C11	CAP CER 10N 100V 20%+ DISC	26383-055L
C12	CAP CER 10N 100V 20%+ DISC	26383-055L
C13	CAP CER 39N 50V 20% CHIP	26386-757H
C14	CAP CER 1P8 63V .5PF PLATE	26343-456C
C15	CAP CER 10N 100V 20%+ DISC	26383-055L
C16	CAP CER 1NO 63V 10% PLATE	26383-585M
C17	CAP CER 1NO 63V 10% PLATE	26383-585M
C18	CAP CER 1NO 63V 10% PLATE	26383-585M
C19	CAP CER 1NO 63V 10% PLATE	26383-585M
C20	CAP CER 10N 100V 20%+ DISC	26383-055L
C21	CAP CER 10N 100V 20%+ DISC	26383-055L
C22	CAP CER 10N 100V 20%+ DISC	26383-055L
C23	CAP CER 10N 100V 20%+ DISC	26383-055L
C24	CAP CER 10N 100V 20%+ DISC	26383-055L
C25	CAP CER 10N 100V 20%+ DISC	26383-055L
C26	CAP PETP 1UO 50V 10% RAD MIN	26582-432F
C27	CAP CER 10N 100V 20%+ DISC	26383-055L
C28	CAP CER 10N 100V 20%+ DISC	26383-055L
C29	CAP ELEC 100U 63V 20% SUBMIN	26421-118L
C30	CAP ELEC 4U7 35V 20% SUBMIN	26421-108A
C31	CAP ELEC 4U7 35V 20% SUBMIN	26421-108A
C32	CAP CER 22P 63V 5% PLATE	26343-469N
D1	DI SIL 1N4148 75V JUNC	28336-676J
D2	DI SIL 1N4148 75V JUNC	28336-676J
D3	DI SIL 1N4148 75V JUNC	28336-676J
D4	DI SIL 1N4148 75V JUNC	28336-676J
D5	DI SIL 1N4148 75V JUNC	28336-676J
D6	DI SIL 1N4148 75V JUNC	28336-676J
D7	DI SIL 1N4148 75V JUNC	28336-676J
D8	DI SIL 1N4148 75V JUNC	28336-676J
D9	DI SIL 1N4148 75V JUNC	28336-676J
IC1	ICD DIV SP8607BCM/2 600MHZ	28462-023B
IC2	ICD DIV SP8604BCM/2 300MHZ	28462-022R
IC3	ICD FF D 10231 M/SLAVE	28462-610K
IC4	ICD FF JK 74S112 DUAL -EDG TR	28462-015P
IC5	ICD FF JK 74LS112 DUAL -EDG TR	28462-020M

Circuit Ref	Description	Part Number
Unit AB2	- DIVIDE-BY-TWO CHAIN & FM DRIVE (continued)	
IC6	ICD AND 10104 QUAD 2INP ECL	28466-015G
IC7	ICD NAND 74LS00 QUAD 2INP	28466-345H
IC8	ICD FF D 74LS273 OCT +EDG TR	28462-615U
IC9	ICD FF D 74LS175 QUAD +EDG TR	28462-614E
IC10	ICA AMP SE5534	28461-346K
L1	IND CHOKE 4.7UH 10% LAQ	23642-553J
L2	IND CHOKE 4.7UH 10% LAQ	23642-553J
L3	IND CHOKE 4.7UH 10% LAQ	23642-553J
R1	RES CC 100R 1/8W 5%	24331-997B
R2	RES MF 1K5 1/4W 2% 100PPM	24773-277U
R3	RES MF 150R 1/4W 2% 100PPM	24773-253F
R4	RES MF 51R 1/4W 2% 100PPM	24773-242Z
R5	RES CHIP 10R 5%	24681-042H
R6	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R7	RES MF 10K 1/4W 2% 100PPM	24773-297M
R8	RES MF 470R 1/4W 2% 100PPM	24773-265M
R9	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R10	RES MF 51R 1/4W 2% 100PPM	24773-242Z
R11	RES MF 470R 1/4W 2% 100PPM	24773-265M
R12	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R13	RES CC 51R 1/8W 5%	24331-989P
R14	RES CC 100R 1/8W 5%	24331-997B
R15	RES MF 10K 1/4W 2% 100PPM	24773-297M
R16	RES MF 2K7 1/4W 2% 100PPM	24773-283L
R17	RES MF 10K 1/4W 2% 100PPM	24773-297M
R18	RES MF 1K2 1/4W 2% 100PPM	24773-275H
R19	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R20	RES MF 51R 1/4W 2% 100PPM	24773-242Z
R21	RES MF 220R 1/4W 2% 100PPM	24773-257W
R22	RES MF 51R 1/4W 2% 100PPM	24773-242Z
R23	RES CC 51R 1/8W 5%	24331-989P
R24	RES CC 270R 1/8W 5%	24331-992P
R25	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R26	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R27	RES MF 470R 1/4W 2% 100PPM	24773-265M
R28	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R29	RES MF 51R 1/4W 2% 100PPM	24773-242Z
R30	RES MF 10K 1/4W 2% 100PPM	24773-297M
R31	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R32	RES MF 10K 1/4W 2% 100PPM	24773-297M
R33	RES MF 10K 1/4W 2% 100PPM	24773-297M
R34	RES MF 51R 1/4W 2% 100PPM	24773-242Z
R35	RES MF 10K 1/4W 2% 100PPM	24773-297M

Circuit Ref	Description	Part Number
Unit AB2	- DIVIDE-BY-TWO CHAIN & FM DRIVE (continued)	
R36	RES MF 680R 1/4W 2% 100PPM	24773-269K
R37	RES MF 1K5 1/4W 2% 100PPM	24773-277U
R38	RES MF 1K5 1/4W 2% 100PPM	24773-277U
R39	RES MF 1K5 1/4W 2% 100PPM	24773-277U
R40	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R41	RES MF 91R 1/4W 2% 100PPM	24773-248L
R42	RES MF 1K5 1/4W 2% 100PPM	24773-277U
R43	RES MF 2K7 1/4W 2% 100PPM	24773-283L
R44	RES MF 3K0 1/4W 2% 100PPM	24773-284J
R45	RES MF 5K6 1/4W 2% 100PPM	24773-291S
R46	RES MF 330R 1/4W 2% 100PPM	24773-261D
R47	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R48	RES MF 3K0 1/4W 2% 100PPM	24773-284J
R49	RES MF 5K6 1/4W 2% 100PPM	24773-291S
R50	RES MF 330R 1/4W 2% 100PPM	24773-261D
R51	RES MF 1K2 1/4W 2% 100PPM	24773-275H
R52	RES MF 3K0 1/4W 2% 100PPM	24773-284J
R53	RES MF 5K6 1/4W 2% 100PPM	24773-291S
R54	RES MF 330R 1/4W 2% 100PPM	24773-261D
R55	RES MF 51R 1/4W 2% 100PPM	24773-242Z
R56	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R57	RES MF 900R 1/4W 0.25% 25PPM	24732-270N
R58	RES MF 3K78 0.25W 0.25% 25PPM	24732-267N
R59	RES MF 75R0 1/4W .25% 25PPM	24732-313V
R61	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R62	RES MF 150R 1/4W 2% 100PPM	24773-253F
R63	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R64	RES MF 150R 1/4W 2% 100PPM	24773-253F
R65	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R66	RES MF 150R 1/4W 2% 100PPM	24773-253F
R67	RES MF 2K2 1/4W 2% 100PPM	24773-281Y
R68	RES MF 2K2 1/4W 2% 100PPM	24773-281Y
R69	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R70	RES MF 51R 1/4W 2% 100PPM	24773-242Z
R71	RES MF 33R 1/4W 2% 100PPM	24773-237K
RLA	RELAY REED 1CO 12V 890R	23486-427A
RLB	RELAY REED 1CO 12V 890R	23486-427A
RLC	RELAY REED 1CO 12V 890R	23486-427A
SKBW	CON RF SMB MALE 50 PCB STR	23444-334Y
SKBX	CON RF SMB MALE 50 PCB STR	23444-334Y
TR1	TR NSI BFR90 15V 5G - AMP	28452-167U
TR2	TR NSI BFR90 15V 5G - AMP	28452-167U
TR3	TR PSI BC308B 20V 130M - GEN	28433-455R

Circuit Ref	Description	Part Number
Unit AB2	- DIVIDE-BY-TWO CHAIN & FM DRIVE (continued)	
TR4	TR NSI BFR90 15V 5G - AMP	28452-167U
TR5	TR PSI BC308B 20V 130M - GEN	28433-455R
TR6	TR NSI BFR90 15V 5G - AMP	28452-167U
TR7	TR NSI BFR90 15V 5G - AMP	28452-167U
TR8	TR NSI BFR90 15V 5G - AMP	28452-167U
TR9	TR NSI BC209C 20V 150M - GEN	28452-771P
TR10	TR PSI BC308B 20V 130M - GEN	28433-455R
TR11	TR PSI BC308B 20V 130M - GEN	28433-455R
TR12	TR NSI 2N2369 15V 500M - SW	28452-197H
TR13	TR PNP 2N4959 30 V LG - LN AMP	28433-836K
TR14	TR NSI BC209C 20V 150M - GEN	28452-771P
TR15	TR NSI BC209C 20V 150M - GEN	28452-771P
TR16	TR NSI BC209C 20V 150M - GEN	28452-771P
X2	S/C ACC PAD TO18, ETC TO .1"GRD	28488-115L
X3	S/C ACC PAD TO5 TO DIL8	28488-102R
Unit AB3	- OSCILLATORS BOARD AB3	
13. When ordering, prefix circuit reference with AB3		
	Complete unit	44828-431T
C1	CAP CER 100P 63V 2% PLATE	26343-477V
C2	CAP ELEC 470N 50V 20% SUBMIN	26421-104C
C3	CAP CER 2P7 50V 0.5P CHIP	26343-756W
C4	CAP CER 22P 50V 5% CHIP	26386-762V
C5	CAP CER 33P 50V 5% CHIP	26386-763Y
C6	CAP CER 33P 50V 5% CHIP	26386-763Y
C7	CAP CER 1N0 63V 10% PLATE	26383-585M
C8	CAP TANT 470N 35V 20% BEAD	26486-207L
C9	CAP CER 10N 50V 20% CHIP	26386-754K
C10	CAP CER 10N 50V 20% CHIP	26386-754K
C11	CAP CER 1N0 63V 10% PLATE	26383-602E
C12	CAP CER 33P 50V 5% CHIP	26386-763Y
C13	CAP CER 22P 50V 5% CHIP	26386-762V
C14	CAP CER 22P 50V 5% CHIP	26386-762V
C15	CAP CER 1N0 63V 10% PLATE	26383-585M
C16	CAP CER 1N0 63V 10% PLATE	26383-585M
C18	CAP CER 39N 50V 20% CHIP	26386-757H
C19	CAP CER 2P2 50V 0.5P CHIP	26343-786V
C20	CAP CER 5P6 50V 0.5P CHIP	26343-759P
C21	CAP CER 68P 50V 5% CHIP	26386-765L
C22	CAP CER 47P 50V 5% CHIP	26386-764N

Circuit Ref	Description	Part Number
Unit AB3	- OSCILLATORS BOARD AB3 (continued)	
C23	CAP CER 47P 50V 5% CHIP	26386-764N
C24	CAP CER 1N0 63V 10% PLATE	26383-602E
C25	CAP CER 10N 50V 20% CHIP	26386-754K
C26	CAP CER 10N 50V 20% CHIP	26386-754K
C27	CAP CER 1N0 63V 10% PLATE	26383-585M
C28	CAP CER 22P 50V 5% CHIP	26386-762V
C29	CAP CER 22P 50V 5% CHIP	26386-762V
C30	CAP CER 33P 50V 5% CHIP	26386-763Y
C31	CAP CER 3P3 50V 0.5P CHIP	26343-757D
C32	CAP CER 39N 50V 20% CHIP	26386-757H
C33	CAP CER 1N0 63V 10% PLATE	26383-585M
C37	CAP ELEC 470N 50V 20% SUBMIN	26421-104C
D1	DI V/CAP BB809 3V 29PF	28381-132G
D3	DI SIL BA482 35V JUNC	28335-675R
D4	DI SIL BA482 35V JUNC	28335-675R
D6	DI V/CAP BB809 3V 29PF	28381-132G
D7	DI V/CAP BB809 3V 29PF	28381-132G
D9	DI V/CAP BB405B 3V 11.5PF	28381-101V
D10	DI SIL BA482 35V JUNC	28335-675R
D11	DI SIL BA482 35V JUNC	28335-675R
D12	DI SIL BA482 35V JUNC	28335-675R
D13	DI V/CAP BB809 3V 29PF	28381-132G
D15	DI SIL 1N4148 75V JUNC	28336-676J
L1	COIL RF 10UH	44290-805W
L2	COIL RF 10UH	44290-805W
L3	PRINTED COIL	
L4	PRINTED COIL	
L5	COIL RF 10UH	44290-805W
L6	COIL RF 10UH	44290-805W
L7	COIL RF 10UH	44290-805W
L8	COIL RF 10UH	44290-805W
L9	PRINTED COIL	
L10	PRINTED COIL	
L11	COIL RF 10UH	44290-805W
L12	COIL RF 10UH	44290-805W
R1	RES MF 50R 1/4W 0.1% 50PPM	24723-388Y
R2	RES MF 5K6 1/4W 2% 100PPM	24773-291S
R3	RES MF 470R 1/4W 2% 100PPM	24773-265M
R4	RES CHIP 22R 5%	24681-044U
R5	RES MF 330R 1/4W 2% 100PPM	24773-261D
R6	RES MF 10R 1/4W 2% 100PPM	24773-225W
R7	RES MF 10K 1/4W 2% 100PPM	24773-297M

Circuit Ref	Description	Part Number
Unit AB3	- OSCILLATORS BOARD AB3 (continued)	
R8	RES MF 10K 1/4W 2% 100PPM	24773-297M
R9	RES CHIP 22R 5%	24681-044U
R10	RES MF 330R 1/4W 2% 100PPM	24773-261D
R11	RES MF 10R 1/4W 2% 100PPM	24773-225W
R12	RES MF 100R 1/4W 2% 100PPM	24773-249J
R13	RES MF 10K 1/4W 2% 100PPM	24773-297M
R14	RES MF 200R 1/4W 2% 100PPM	24773-256S
R15	RES MF 470R 1/4W 2% 100PPM	24773-265M
R16	RES MF 620R 1/4W 2% 100PPM	24773-268B
R17	RES CC 33R 1/8W 5%	24331-978J
R18	RES MF 250R 1/4W 0.25% 50PPM	24723-389N
R19	RES CHIP 22R 5%	24681-044U
R20	RES MF 330R 1/4W 2% 100PPM	24773-261D
R21	RES MF 10R 1/4W 2% 100PPM	24773-225W
R22	RES MF 10K 1/4W 2% 100PPM	24773-297M
R23	RES MF 10K 1/4W 2% 100PPM	24773-297M
R24	RES CHIP 16R 5%	24681-043E
R25	RES MF 330R 1/4W 2% 100PPM	24773-261D
R26	RES MF 10R 1/4W 2% 100PPM	24773-225W
R27	RES MF 820R 1/4W 2% 100PPM	24773-271B
R28	RES CC 51R 1/8W 5%	24331-989P
R29	RES CHIP 10R 5%	24681-042H
R30	RES CHIP 10R 5%	24681-042H
R31	RES CHIP 10R 5%	24681-042H
R32	RES CHIP 10R 5%	24681-042H
R35	RES MF 100R 1/4W 2% 100PPM	24773-249J
R36	RES CC 100R 1/8W 5%	24331-997B
TR1	TR NJF 2N4858 40V - 8MA SW	28459-037F
TR2	TR NSI BFR91A 12V 5G - AMP	28451-694H
TR4	TR NSI BFR91A 12V 5G - AMP	28451-694H
TR6	TR NSI BFR90 5V 5G - AMP	28452-167U
TR7	TR NSI BFR91A 12V 5G - AMP	28451-694H
TR9	TR NSI BFR91A 12V 5G - AMP	28451-694H
TR11	TR NSI BFR90 15V 5G - AMP	28452-167U
X1	S/C ACC PAD TO18,ETC TO .1"GRD	28488-115L
Unit AB4	- O/P PHASE DETECTOR AB4	
14. When ordering, prefix circuit reference with AB4		
	Complete unit	44828-432P
C1	CAP ELEC 4U7 35V 20% SUBMIN	26421-108A
C2	CAP ELEC 22U 25V 20% SUBMIN	26421-114E

Circuit Ref	Description	Part Number
Unit AB4	- O/P PHASE DETECTOR AB4 (continued)	
C3	CAP ELEC 4U7 35V 20% SUBMIN	26421-108A
C4	CAP CER 10N 100V 20%+ DISC	26383-055L
C5	CAP CER 10N 100V 20%+ DISC	26383-055L
C6	CAP CER 10N 100V 20%+ DISC	26383-055L
C7	CAP CER 10N 100V 20%+ DISC	26383-055L
C8	CAP CER 10N 100V 20%+ DISC	26383-055L
C9	CAP CER 10N 100V 20%+ DISC	26383-055L
C10	CAP CER 10N 100V 20%+ DISC	26383-055L
C11	CAP CER 10N 100V 20%+ DISC	26383-055L
C12	CAP CER 10N 100V 20%+ DISC	26383-055L
C13	CAP PETP 680N 100V 10% RAD	26582-216E
C14	CAP PETP 5U6 63V 10% RAD	26582-423E
C15	CAP ELEC 4U7 35V 20% SUBMIN	26421-108A
C16	CAP CER 47P 63V 5% PLATE	26343-473L
C17	CAP CER 10N 100V 20%+ DISC	26383-055L
C18	CAP CER 10N 100V 20%+ DISC	26383-055L
C19	CAP CER 10N 100V 20%+ DISC	26383-055L
C20	CAP ELEC 220U 16V 20% SUBMIN	26421-124G
C21	CAP CER 10N 100V 20%+ DISC	26383-055L
C22	CAP CER 10N 100V 20%+ DISC	26383-055L
C23	CAP CER 220P 63V 2% PLATE	26343-481S
C24	CAP CER 220P 63V 2% PLATE	26343-481S
C25	CAP CER 220P 63V 2% PLATE	26343-481S
C26	CAP CER 47P 63V 5% PLATE	26343-473L
C27	CAP ELEC 22U 25V 20% SUBMIN	26421-114E
C28	CAP CER 10N 100V 20% +DISC	26383-055L
C29	CAP ELEC 100U 25V 20% +AX	26415-813U
D1	DI ZEN BZX79C6V2 6.2V 5%	28371-481D
D2	DI ZEN BZX79C6V2 6.2V 5%	28371-481D
D3	DI ZEN BZX79C6V2 6.2V 5%	28371-481D
D4	DI ZEN BZX79C6V2 6.2V 5%	28371-481D
IC1	CD FF D 74LS74 DUAL +EDG TR	28462-611A
IC2	ICA VREG- LM304H PROG 25MA	28461-723R
IC3	ICD CTR 74LS390 DUAL 4BIT DEC	28464-127R
IC4	ICD AND/OR 74LS51 DUAL 2-3INP	28466-454N
IC5	ICD FF D 74LS74 DUAL +EDG TR	28462-611A
IC6	ICD NAND 74LS00 QUAD 2INP	28466-345H
IC7	ICA VREG+ LM376N PROG 0A045	28461-725K

Circuit Ref	Description	Part Number
Unit AB4	- O/P PHASE DETECTOR AB4 (continued)	
R1	RES MF 820R 1/4W 2% 100PPM	24773-271B
R2	RES MF 820R 1/4W 2% 100PPM	24773-271B
R3	RES MF 820R 1/4W 2% 100PPM	24773-271B
R4	RES MF 820R 1/4W 2% 100PPM	24773-271B
R5	RES MF 2K4 1/4W 2% 100PPM	24773-282N
R6	RES MF 5K6 1/4W 2% 100PPM	24773-291S
R7	RES MF 8R2 1/4W 2% 100PPM	24773-223V
R8	RES MF 10K 1/4W 2% 100PPM	24773-297M
R9	RES MF 62K 1/4W 2% 100PPM	24773-316Y
R10	RES MF 100K 1/4W 2% 100PPM	24773-321L
R11	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R12	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R13	RES MF 10K 1/4W 2% 100PPM	24773-297M
R14	RES MF 62K 1/4W 2% 100PPM	24773-316Y
R15	RES MF 47K 1/4W 2% 100PPM	24773-313H
R16	RES MF 100K 1/4W 2% 100PPM	24773-321L
R17	RES MF 1K3 1/4W 2% 100PPM	24773-276E
R18	RES MF 1K8 1/4W 2% 100PPM	24773-279N
R19	RES MF 5K6 1/4W 2% 100PPM	24773-291S
R20	RES MF 430R 1/4W 2% 100PPM	24773-264X
R21	RES MF 2K0 1/4W 2% 100PPM	24773-280U
R22	RES MF 100R 1/4W 2% 100PPM	24773-249J
R23	RES MF 100R 1/4W 2% 100PPM	24773-249J
R24	RES MF 10K 1/4W 2% 100PPM	24773-297M
R25	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R26	RES MF 5K6 1/4W 2% 100PPM	24773-291S
R27	RES MF 430R 1/4W 2% 100PPM	24773-264X
R28	RES MF 2K0 1/4W 2% 100PPM	24773-280U
R29	RES MF 5K6 1/4W 2% 100PPM	24773-291S
R30	RES MF 430R 1/4W 2% 100PPM	24773-264X
R31	RES MF 100K 1/4W 2% 100PPM	24773-321L
R32	RES MF 1K3 1/4W 2% 100PPM	24773-276E
R33	RES MF 1K8 1/4W 2% 100PPM	24773-279N
R34	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R35	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R36	RES MF 10K 1/4W 2% 100PPM	24773-297M
R37	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R38	RES MF 5K6 1/4W 2% 100PPM	24773-291S
R39	RES MF 430R 1/4W 2% 100PPM	24773-264X
R40	RES MF 100K 1/4W 2% 100PPM	24773-321L
R41	RES MF 390R 1/4W 2% 100PPM	24773-263P

Circuit Ref	Description	Part Number
Unit AB4	- O/P PHASE DETECTOR AB4 (continued)	
R42	RES MF 3K9 1/4W 2% 100PPM	24773-287V
R43	RES MF 1KO 1/4W 2% 100PPM	24773-273A
R44	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R45	RES MF 8R2 1/4W 2% 100PPM	24773-223V
R46	RES MF 12K 1/4W 2% 100PPM	24773-299R
R47	RES MF 2K2 1/4W 2% 100PPM	24773-281Y
R49	RES MF 1MO 1/4W 2% 100PPM	24773-346E
R50	RES MF 10K 1/4W 2% 100PPM	24773-297M
R51	RES MF 10K 1/4W 2% 100PPM	24773-297M
R52	RES MF 10K 1/4W 2% 100PPM	24773-297M
R53	RES MF 10K 1/4W 2% 100PPM	24773-297M
R54	RES MF 100R 1/4W 2% 100PPM	24773-249J
R55	RES MF 8R2 1/4W 2% 100PPM	24773-223V
R56	RES MF 100R 1/4W 2% 100PPM	24773-249J
TR1	TR PSI BC307A 45V 130M - GEN	28435-227H
TR2	TR PSI BC307A 45V 130M - GEN	28435-227H
TR3	TR PSI BC307A 45V 130M - GEN	28435-227H
TR4	TR PSI BC307A 45V 130M - GEN	28435-227H
TR9	TR PSI BC307A 45V 130M - GEN	28435-227H
TR10	TR PSI BC307A 45V 130M - GEN	28435-227H
TR11	TR NSI BC237A 45V 150M - GEN	28455-421X
TR12	TR NSI BC237A 45V 150M - GEN	28455-421X
TR13	TR PSI BC307A 45V 130M - GEN	28435-227H
TR14	TR PSI BC307A 45V 130M - GEN	28435-227H
TR15	TR PSI BC307A 45V 130M - GEN	28435-227H
TR16	TR NSI BC237A 45V 150M - GEN	28455-421X
TR17	TR NSI BC237A 45V 150M - GEN	28455-421X
TR18	TR NSI BC237A 45V 150M - GEN	28455-421X
TR19	TR PSI BC307A 45V 130M - GEN	28435-227H
TR20	TR PSI BC307A 45V 130M - GEN	28435-227H
TR21	TR PSI BC307A 45V 130M - GEN	28435-227H
TR22	TR NSI BC237A 45V 150M - GEN	28455-421X
TR23	TR NSI BC237A 45V 150M - GEN	28455-421X
TR24	TR NJF J310 25V - 24MA	28459-028E
TR25	TR NJF J310 25V - 24MA	28459-028E
TR26	TR NJF J310 25V - 24MA	28459-028E
TR27	TR NSI BC237A 45V 150M - GEN	28455-421X
TR28	TR NSI BC237A 45V 150M - GEN	28455-421X
TR29	TR NSI BC237A 45V 150M - GEN	28455-421X
TR30	TR NSI BC237A 45V 150M - GEN	28455-421X
X2	CON JUMP FEM 2 1 ROW	23435-990X
X4	S/C ACC PAD TO5 TO DIL10	28488-101C

Circuit Ref	Description	Part Number
Unit AB5	- VCXO LOOP	
15. When ordering, prefix circuit reference with AB5		
	Complete unit	44828-433X
C1	CAP PETP 1U0 100V 10% RAD	26582-217U
C2	CAP PETP 220N 100V 10% RAD	26582-226G
C3	CAP PS 100P 63V 2PF RAD	26538-557S
C4	CAP PS 100P 63V 2PF RAD	26538-557S
C5	CAP CER 10N 100V 20%+ DISC	26383-055L
C6	CAP CER 10N 100V 20%+ DISC	26383-055L
C7	CAP CER 10N 100V 20%+ DISC	26383-055L
C8	CAP CER 10N 100V 20%+ DISC	26383-055L
C9	CAP CER 10N 100V 20%+ DISC	26383-055L
C10	CAP CER 10N 100V 20%+ DISC	26383-055L
C11	CAP CER 1N0 63V 10% PLATE	26383-585M
C12	CAP CER 10N 100V 20%+ DISC	26383-055L
C13	CAP CER 10N 100V 20%+ DISC	26383-055L
C14	CAP CER 10N 100V 20%+ DISC	26383-055L
C15	CAP CER 10N 100V 20%+ DISC	26383-055L
C17	CAP PETP 220N 100V 10% RAD	26582-226G
C18	CAP CER 10N 100V 20%+ DISC	26383-055L
C19	CAP CER 1N0 63V 10% PLATE	26383-585M
C20	CAP PETP 10N 63V 10% SUB MIN	26582-426N
C21	CAP CER 10N 100V 20%+ DISC	26383-055L
C22	CAP CER 10N 100V 20%+ DISC	26383-055L
C23	CAP CER 10N 100V 20%+ DISC	26383-055L
C24	CAP PS 100P 63V 2PF RAD	26538-557S
C25	CAP PETP 10N 63V 10% SUB MIN	26582-426N
C26	CAP CER 1N0 63V 10% PLATE	26383-585M
C27	CAP CER 47P 63V 5% PLATE	26343-473L
C28	CAP CER 5P6 63V .5PF PLATE	26343-462K
D1	DI ZEN BZX79C12 12V 5%	28372-149G
D2	DI V/CAP BB809 3V 29PF	28381-132G
D3	DI H/CARR HP5082-2835	28349-006H
D4	DI ZEN BZX79C3V6 3.6V 5%	28371-224H
IC1	ICD NOR 74LS02 QUAD 2INP	28466-214Y
IC2	ICA MOD/DMOD MC1496N BAL DIL14	28461-924X
IC3	ICD CTR 74LS390 DUAL 4BIT DEC	28464-127R
IC4	ICD FF D 74LS74 DUAL +EDG TR	28462-611A
IC5	ICA COMP LM311N DIL8	28461-695U
IC6	ICD NAND 74LS13 DUAL 4INP	28469-206L
IC7	ICA AMP TL071CP FET I/P DIL8	28461-347A

Circuit Ref	Description	Part Number
Unit AB5	- VCXO LOOP (continued)	
L1	IND CHOKE 15UH 5%	23642-469A
*L2	IND CHOKE 1.5UH 10% LAQ	23642-550Y
R1	RES MF 150R 1/4W 2% 100PPM	24773-253F
R2	RES MF 10K 1/4W 2% 100PPM	24773-297M
R3	RES MF 10K 1/4W 2% 100PPM	24773-297M
R4	RES MF 10K 1/4W 2% 100PPM	24773-297M
R5	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R6	RES MF 2K0 1/4W 2% 100PPM	24773-280U
R7	RES MF 2K0 1/4W 2% 100PPM	24773-280U
R8	RES MF 2K0 1/4W 2% 100PPM	24773-280U
R9	RES MF 7K5 1/4W 2% 100PPM	24773-294T
R10	RES MF 12K 1/4W 2% 100PPM	24773-299R
R11	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R12	RES MF 150R 1/4W 2% 100PPM	24773-253F
R13	RES MF 300R 1/4W 2% 100PPM	24773-260W
R14	RES MF 3K9 1/4W 2% 100PPM	24773-287V
R15	RES MF 3K9 1/4W 2% 100PPM	24773-287V
R16	RES MF 12K 1/4W 2% 100PPM	24773-299R
R17	RES MF 10K 1/4W 2% 100PPM	24773-297M
R18	RES MF 2K4 1/4W 2% 100PPM	24773-282N
R19	RES MF 68R 1/4W 2% 100PPM	24773-245U
R20	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R21	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R22	RES MF 1K5 1/4W 2% 100PPM	24773-277U
R23	RES MF 1K5 1/4W 2% 100PPM	24773-277U
R24	RES MF 8K2 1/4W 2% 100PPM	24773-295P
R25	RES MF 2K4 1/4W 2% 100PPM	24773-282N
R26	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R27	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R28	RES MF 39K 1/4W 2% 100PPM	24773-311A
R29	RES MF 8K2 1/4W 2% 100PPM	24773-295P
R30	RES MF 300R 1/4W 2% 100PPM	24773-260W
R31	RES MF 300R 1/4W 2% 100PPM	24773-260W
R33	RES MF 3K9 1/4W 2% 100PPM	24773-287V
R35	RES MF 2K0 1/4W 2% 100PPM	24773-280U
R36	RES MF 10K 1/4W 2% 100PPM	24773-297M
R37	RES MF 10K 1/4W 2% 100PPM	24773-297M
R38	RES MF 6K8 1/4W 2% 100PPM	24773-293D
TR1	TR NSI BC209C 20V 150M - GEN	28452-771P
TR2	TR NSI BC209C 20V 150M - GEN	28452-771P
TR3	TR NSI BC209C 20V 150M - GEN	28452-771P

Circuit Ref	Description	Part Number
Unit AB5	- VCXO LOOP (continued)	
TR4	TR PSI BC308B 20V 130M - GEN	28433-455R
TR5	TR PSI BC308B 20V 130M - GEN	28433-455R
TR6	TR PSI BC308B 20V 130M - GEN	28433-455R
TR7	TR NSI BC209C 20V 150M - GEN	28452-771P
TR8	TR NSI BC209C 20V 150M - GEN	28452-771P
X2	CON JUMP FEM 2 1 ROW	23435-990X
XL1	XTAL 10.01MHZ FLYING LEADS	28312-072R
Unit AC0	- RF BOX 2 (44990-352S)	
16. When ordering, prefix circuit reference with AC0		
C1	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C2	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C3	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C4	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C5	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C6	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C7	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C8	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C9	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C10	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C11	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C12	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C13	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C14	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C15	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C16	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C17	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C18	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C19	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C20	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C21	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C22	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C23	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C24	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C25	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C26	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C27	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C28	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C29	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K

Circuit Ref	Description	Part Number
Unit AC0	- RF BOX 2 (continued)	
C30	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C31	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C32	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C33	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C34	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C35	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C36	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C37	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C38	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C39	CAP CER 1NO 300V 20%+ L/T SOL	26273-733K
C40	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C41	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C42	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C43	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C44	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C45	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C46	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C47	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C48	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C49	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C50	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C51	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C52	CAP CER 50P 300V 20%+ L/T SOL	26333-229K
C53	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C54	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C55	CAP CER 10N 25V 20% DISC	26383-006L
L1	IND CHOKE 100UH 10% LAQ	23642-561W
L2	IND CHOKE 100UH 10% LAQ	23642-561W
L3	IND CHOKE 100UH 10% LAQ	23642-561W
L4	IND CHOKE 100UH 10% LAQ	23642-561W
L5	IND CHOKE 100UH 10% LAQ	23642-561W
L6	IND CHOKE 100UH 10% LAQ	23642-561W
L7	IND CHOKE 100UH 10% LAQ	23642-561W
L8	IND CHOKE 100UH 10% LAQ	23642-561W
L9	IND CHOKE 100UH 10% LAQ	23642-561W
L10	IND CHOKE 100UH 10% LAQ	23642-561W
L11	IND CHOKE 100UH 10% LAQ	23642-561W
L12	IND CHOKE 100UH 10% LAQ	23642-561W
L13	IND CHOKE 100UH 10% LAQ	23642-561W
L14	IND CHOKE 100UH 10% LAQ	23642-561W
L15	IND CHOKE 100UH 10% LAQ	23642-561W

Circuit Ref	Description	Part Number
Unit AC0	- RF BOX 2 (continued)	
L16	IND CHOKE 100UH 10% LAQ	23642-561W
L17	IND CHOKE 100UH 10% LAQ	23642-561W
L18	IND CHOKE 100UH 10% LAQ	23642-561W
L19	IND CHOKE 100UH 10% LAQ	23642-561W
L20	IND CHOKE 100UH 10% LAQ	23642-561W
L21	IND CHOKE 100UH 10% LAQ	23642-561W
L22	IND CHOKE 100UH 10% LAQ	23642-561W
L23	IND CHOKE 100UH 10% LAQ	23642-561W
L24	IND CHOKE 100UH 10% LAQ	23642-561W
L33	IND CHOKE 100UH 10% LAQ	23642-561W
L34	IND CHOKE 100UH 10% LAQ	23642-561W
PLDE	CABLE COAX 0.1M SMB-FEM/-	43129-687T
R1-R24	RES MF 220R 1/4W 2% 100 PPM	24773-257W
SKJ	CABLE WIR 31CM 4 MIN-1ROW-6P/-	43129-646F
SKAA	CABLE RIB 57CM 16 IDC-FM-DIL/-	43129-652S
SKAW	CON RF SMB MALE 50 BKHD SOLDER	23444-331H
SKAX	CON RF SMC MALE 50 BKHD S/TAG	23444-382T
SKCM	CABLE RIB .1M 16 IDC-FEM-DIL/-	43129-680J
SKCN	CABLE RIB 7CM 14 IDC-FEM-DILX2	43129-683V
SKCP	CABLE RIB 12CM 16 IDC-FM-DILX2	43129-682G
SKCR	CABLE WIR 0.1M 6 MIN-1ROW-7P/-	43129-681F
SKCU	CABLE WIR 6CM 2 MIN-1ROW-3P/-	43129-685W
SKCV	CABLE WIR 8CM 3 MIN-1ROW-4P/-	43129-686D
SKDA	CON ASSY SKDA-SKCT-SKCW	43129-684S
SKDD	CABLE COAX 34CM MIN-1ROW-3P/-	43129-688P
X1	FERRITE BEAD	41372-006T
X2	FERRITE BEAD	41372-006T
X3	FERRITE BEAD	41372-006T
X4	FERRITE BEAD	41372-006T
X5	FERRITE BEAD	41372-006T
Unit AC2	- BFO SYSTEM AC2	
17. When ordering, prefix circuit reference with AC2		
	Complete unit	44828-435C
C1	CAP CER 10N 100V 20%+ DISC	26383-055L
C2	CAP CER 10N 100V 20%+ DISC	26383-055L
C3	CAP CER 10N 100V 20%+ DISC	26383-055L
C4	CAP CER 10N 100V 20%+ DISC	26383-055L
C5	CAP CER 560P 63V 10% PLATE	26383-581D

Circuit Ref	Description	Part Number
Unit AC2	- BFO SYSTEM AC2 (continued)	
C6	CAP CER 100P 63V 2% PLATE	26343-477V
C7	CAP CER 1N0 63V 10% PLATE	26383-585M
C8	CAP CER 560P 63V 10% PLATE	26383-581D
C9	CAP ELEC 470N 50V 20% SUBMIN	26421-104C
C10	CAP CER 10N 100V 20%+ DISC	26383-055L
C11	CAP CER 10N 100V 20%+ DISC	26383-055L
C12	CAP ELEC 470N 50V 20% SUBMIN	26421-104C
C13	CAP ELEC 470N 50V 20% SUBMIN	26421-104C
C14	CAP CER 10N 100V 20%+ DISC	26383-055L
C15	CAP CER 10N 100V 20%+ DISC	26383-055L
C16	CAP CER 10N 100V 20%+ DISC	26383-055L
C17	CAP CER 560P 63V 10% PLATE	26383-581D
C18	CAP CER 1N0 63V 10% PLATE	26383-585M
C19	CAP CER 100P 63V 2% PLATE	26343-477V
C20	CAP CER 560P 63V 10% PLATE	26383-581D
C21	CAP ELEC 470N 50V 20% SUBMIN	26421-104C
C22	CAP ELEC 470N 50V 20% SUBMIN	26421-104C
C23	CAP ELEC 470N 50V 20% SUBMIN	26421-104C
D1	DI SIL BA482 35V JUNC	28335-675R
D2	DI SIL BA482 35V JUNC	28335-675R
L1	IND CHOKE 15UH 10% LAQ	23642-556V
L2	IND CHOKE 15UH 10% LAQ	23642-556V
L3	IND CHOKE 15UH 10% LAQ	23642-556V
L4	IND CHOKE 15UH 10% LAQ	23642-556V
L5	IND CHOKE 1000UH 10% LAQ	23642-567C
R1	RES MF 51R 1/4W 2% 100PPM	24773-242Z
R2	RES MF 10K 1/4W 2% 100PPM	24773-297M
R3	RES MF 10K 1/4W 2% 100PPM	24773-297M
R4	RES MF 270R 1/4W 2% 100PPM	24773-259T
R5	RES MF 470R 1/4W 2% 100PPM	24773-265M
R6	RES MF 18R 1/4W 2% 100PPM	24773-231P
R7	RES MF 10K 1/4W 2% 100PPM	24773-297M
R8	RES MF 10K 1/4W 2% 100PPM	24773-297M
R9	RES MF 1K8 1/4W 2% 100PPM	24773-279N
R10	RES MF 220R 1/4W 2% 100PPM	24773-257W
R11	RES MF 680R 1/4W 2% 100PPM	24773-269K
R12	RES MF 51R 1/4W 2% 100PPM	24773-242Z
R13	RES MF 560R 1/4W 2% 100PPM	24773-267R
R14	RES MF 62R 1/4W 2% 100PPM	24773-244E
R15	RES MF 10K 1/4W 2% 100PPM	24773-297M

Circuit Ref	Description	Part Number
Unit AC2	- BFO SYSTEM AC2 (continued)	
R16	RES MF 1K5 1/4W 2% 100PPM	24773-277U
R17	RES MF 220R 1/4W 2% 100PPM	24773-257W
R18	RES MF 1KO 1/4W 2% 100PPM	24773-273A
R19	RES MF 330R 1/4W 2% 100PPM	24773-261D
R20	RES MF 1KO 1/4W 2% 100PPM	24773-273A
TR1	TR NSI 2N2369 15V 500M - SW	28452-197H
TR2	TR NSI 2N2369 15V 500M - SW	28452-197H
TR3	TR NSI 2N2369 15V 500M - SW	28452-197H
T1	CORE BEAD .079X.158X.197"LG A1	23635-833X
X1	MOD RF SBL-1 DOUBLE BAL MIXER	28531-002A
X2	S/C ACC PAD TO18,ETC TO .1"GRD	28488-115L
Unit AC3	- FILTER BOARD	
18.	When ordering, prefix circuit reference with AC3	
	Complete unit	44828-436R
C1	CAP CER 39N 50V 20% CHIP	26386-757H
C2	CAP CER 10N 100V 20%+ DISC	26383-055L
C3	CAP CER 39N 50V 20% CHIP	26386-757H
C4	CAP CER 39N 50V 20% CHIP	26386-757H
C5	CAP CER 39N 50V 20% CHIP	26386-757H
C6	CAP CER 39N 50V 20% CHIP	26386-757H
C7	CAP CER 39N 50V 20% CHIP	26386-757H
C8	CAP CER 39N 50V 20% CHIP	26386-757H
C9	CAP CER 39N 50V 20% CHIP	26386-757H
C10	CAP CER 10N 100V 20%+ DISC	26383-055L
C11	CAP CER 47N 25V 20% DISC	26383-017U
C12	CAP CER 10N 100V 20%+ DISC	26383-055L
C13	CAP CER 10N 100V 20%+ DISC	26383-055L
C14	CAP CER 10N 100V 20%+ DISC	26383-055L
C15	CAP CER 10N 100V 20%+ DISC	26383-055L
C16	CAP CER 10N 100V 20%+ DISC	26383-055L
C18	CAP CER 10N 100V 20%+ DISC	26383-055L
C19	CAP CER 10N 100V 20%+ DISC	26383-055L
C20	CAP CER 8P2 63V .5PF PLATE	26343-488C
C21	CAP CER 12P 63V 5% PLATE	26343-497H
C22	CAP CER 8P2 63V .5PF PLATE	26343-488C
C23	CAP CER 1NO 63V 10% PLATE	26383-585M
C24	CAP CER 1NO 63V 10% PLATE	26383-585M

Circuit Ref	Description	Part Number
Unit AC3	- FILTER BOARD (continued)	
C25	CAP CER 1NO 63V 10% PLATE	26383-585M
C26	CAP CER 1NO 63V 10% PLATE	26383-585M
C27	CAP CER 1NO 63V 10% PLATE	26383-585M
C28	CAP CER 6P8 63V .5PF PLATE	26343-463A
C29	CAP CER 18P 63V 5% PLATE	26343-468Y
C30	CAP CER 22P 63V 5% PLATE	26343-469N
C31	CAP CER 18P 63V 5% PLATE	26343-468Y
C32	CAP CER 22P 63V 5% PLATE	26343-469N
C33	CAP CER 33P 63V 5% PLATE	26343-471Y
C34	CAP CER 22P 63V 5% PLATE	26343-469N
C35	CAP CER 33P 63V 5% PLATE	26343-471Y
C36	CAP CER 47P 63V 5% PLATE	26343-473L
C37	CAP CER 33P 63V 5% PLATE	26343-471Y
C38	CAP CER 47P 63V 5% PLATE	26343-473L
C39	CAP CER 68P 63V 2% PLATE	26343-475F
C40	CAP CER 47P 63V 5% PLATE	26343-473L
C41	CAP CER 68P 63V 2% PLATE	26343-475F
C42	CAP CER 100P 63V 2% PLATE	26343-477V
C43	CAP CER 68P 63V 2% PLATE	26343-475F
C44	CAP CER 82P 63V 2% PLATE	26343-476G
C45	CAP CER 150P 63V 2% PLATE	26343-479W
C46	CAP CER 82P 63V 2% PLATE	26343-476G
C47	CAP CER 1NO 63V 10% PLATE	26383-585M
C48	CAP CER 1NO 63V 10% PLATE	26383-585M
C49	CAP CER 1NO 63V 10% PLATE	26383-585M
C50	CAP CER 1NO 63V 10% PLATE	26383-585M
C51	CAP CER 12P 63V 5% PLATE	26343-497H
C52	CAP CER 18P 63V 5% PLATE	26343-498E
C53	CAP CER 12P 63V 5% PLATE	26343-497H
C54	CAP CER 1NO 63V 10% PLATE	26383-585M
C55	CAP CER 1P8 63V .5PF PLATE	26343-456C
C56	CAP CER 1NO 63V 10% PLATE	26383-585M
C58	CAP CER 1NO 63V 10% PLATE	26383-585M
C59	CAP CER 10N 100V 20%+ DISC	26383-055L
C60	CAP CER 10N 100V 20%+ DISC	26383-055L
C61	CAP CER 10N 100V 20%+ DISC	26383-055L
C62	CAP CER 10N 100V 20%+ DISC	26383-055L
C63	CAP CER 2P2 63V .5PF PLATE	26343-457R
C64	CAP CER 100P 63V 2% PLATE	26343-477V
C65	CAP CER 120P 63V 2% PLATE	26343-478S
C66	CAP CER 33P 63V 5% PLATE	26343-471Y
C67	CAP CER 100P 63V 2% PLATE	26343-477V

Circuit Ref	Description	Part Number
Unit AC3	- FILTER BOARD (continued)	
C68	CAP CER 22P 63V 5% PLATE	26343-469N
C69	CAP CER 150P 63V 2% PLATE	26343-479W
C70	CAP CER 180P 63V 2% PLATE	26343-480V
C71	CAP CER 150P 63V 2% PLATE	26343-479W
C72	CAP CER 22P 63V 5% PLATE	26343-469N
C73	CAP CER 180P 63V 2% PLATE	26343-480V
C74	CAP CER 270P 63V 2% PLATE	26343-482W
C75	CAP CER 180P 63V 2% PLATE	26343-480V
C76	CAP CER 270P 63V 2% PLATE	26343-482W
C77	CAP CER 390P 63V 10% PLATE	26383-598Y
C78	CAP CER 270P 63V 2% PLATE	26343-482W
C79	CAP CER 470P 63V 10% PLATE	26383-582T
C80	CAP CER 560P 63V 10% PLATE	26383-581D
C81	CAP CER 470P 63V 10% PLATE	26383-582T
C82	CAP CER 560P 63V 10% PLATE	26383-581D
C83	CAP CER 820P 63V 10% PLATE	26383-584X
C84	CAP CER 47P 63V 5% PLATE	26343-473L
C85	CAP CER 560P 63V 10% PLATE	26383-581D
C86	CAP CER 10N 100V 20%+ DISC	26383-055L
C87	CAP CER 10N 100V 20%+ DISC	26383-055L
C88	CAP CER 10N 100V 20%+ DISC	26383-055L
C89	CAP CER 10N 100V 20%+ DISC	26383-055L
C90	CAP CER 68P 63V 2% PLATE	26343-475F
C91	CAP CER 82P 63V 2% PLATE	26343-476G
C92	CAP CER 68P 63V 2% PLATE	26343-475F
C93	CAP CER 33P 63V 5% PLATE	26343-471Y
C94	CAP CER 2P2 63V .5PF PLATE	26343-457R
C95	CAP CER 10N 100V 20%+ DISC	26383-055L
C96	CAP CER 47P 63V 5% PLATE	26343-473L
C97	CAP CER 68P 63V 2% PLATE	26343-475F
C98	CAP CER 47P 63V 5% PLATE	26343-473L
C99	CAP CER 10N 100V 20%+ DISC	26383-055L
C100	CAP CER 10N 100V 20%+ DISC	26383-055L
C101	CAP CER 1N0 63V 10% PLATE	26383-585M
C102	CAP ELEC 4U7 35V 20% SUBMIN	26421-108A
C103	CAP ELEC 4U7 35V 20% SUBMIN	26421-108A
C104	CAP ELEC 4U7 35V 20% SUBMIN	26421-108A
C132	CAP CER 1N0 63V 10% PLATE	26383-585M
C144	CAP CER 10N 100V 20%+ DISC	26383-055L

Circuit Ref	Description	Part Number
Unit AC3	- FILTER BOARD (continued)	
D1	DI SIL BA482 35V JUNC	28335-675R
D2	DI SIL BA482 35V JUNC	28335-675R
D3	DI SIL 1N4148 75V JUNC	28336-676J
D4	DI SIL 1N4148 75V JUNC	28336-676J
D6	DI SIL BA482 35V JUNC	28335-675R
D7	DI SIL BA482 35V JUNC	28335-675R
D8	DI SIL BA482 35V JUNC	28335-675R
D9	DI SIL BA482 35V JUNC	28335-675R
D10	DI SIL BA482 35V JUNC	28335-675R
D11	DI SIL BA482 35V JUNC	28335-675R
D12	DI SIL BA482 35V JUNC	28335-675R
D13	DI SIL BA482 35V JUNC	28335-675R
D14	DI SIL BA482 35V JUNC	28335-675R
D15	DI SIL BA482 35V JUNC	28335-675R
D16	DI SIL BA482 35V JUNC	28335-675R
D17	DI SIL BA482 35V JUNC	28335-675R
D18	DI SIL BA482 35V JUNC	28335-675R
D19	DI SIL BA482 35V JUNC	28335-675R
D20	DI SIL BA482 35V JUNC	28335-675R
D21	DI SIL BA482 35V JUNC	28335-675R
D22	DI SIL BA482 35V JUNC	28335-675R
D23	DI SIL BA482 35V JUNC	28335-675R
D24	DI SIL BA482 35V JUNC	28335-675R
D25	DI SIL BA482 35V JUNC	28335-675R
D26	DI SIL BA482 35V JUNC	28335-675R
D27	DI SIL BA482 35V JUNC	28335-675R
D28	DI SIL BA482 35V JUNC	28335-675R
D30	DI SIL BA482 35V JUNC	28335-675R
D32	DI SIL BA482 35V JUNC	28335-675R
D33	DI SIL BA482 35V JUNC	28335-675R
D34	DI SIL BA482 35V JUNC	28335-675R
D35	DI SIL BA482 35V JUNC	28335-675R
D36	DI SIL BA482 35V JUNC	28335-675R
D37	DI SIL BA482 35V JUNC	28335-675R
D38	DI SIL BA482 35V JUNC	28335-675R
D39	DI SIL BA482 35V JUNC	28335-675R
D40	DI SIL BA482 35V JUNC	28335-675R
D41	DI SIL BA482 35V JUNC	28335-675R
D42	DI SIL BA482 35V JUNC	28335-675R
D43	DI SIL BA482 35V JUNC	28335-675R
D44	DI SIL BA482 35V JUNC	28335-675R
D45	DI SIL BA482 35V JUNC	28335-675R
D46	DI SIL BA482 35V JUNC	28335-675R
D47	DI SIL BA482 35V JUNC	28335-675R

Circuit Ref	Description	Part Number
Unit AC3	- FILTER BOARD (continued)	
D49	DI SIL BA482 35V JUNC	28335-675R
D50	DI SIL BA482 35V JUNC	28335-675R
D51	DI SIL BA482 35V JUNC	28335-675R
D52	DI SIL BA482 35V JUNC	28335-675R
D53	DI SIL BA482 35V JUNC	28335-675R
D74	DI H/CARR HP5082-2835	28349-006H
D75	DI H/CARR HP5082-2835	28349-006H
IC1	ICD DEC/DMX 74LS138 3-8	28465-027F
IC2	ICD FF D 74LS273 OCT +EDG TR	28462-615U
IC3	ICD FF D 74LS273 OCT +EDG TR	28462-615U
IC4	ICD BUFF 7407 HEX O/C	28469-703X
IC5	ICD BUFF 7406 HEX O/C INV 30V	28469-158A
L1	IND CHOKE 68UH 10% LAQ	23642-560S
L2	IND CHOKE 4.7UH 10% LAQ	23642-553J
L3	IND CHOKE 68UH 10% LAQ	23642-560S
L4	IND CHOKE - 1.5TURNS	23642-908P
L5	IND CHOKE - 1.5TURNS	23642-908P
L6	PRINTED COIL	
L7	PRINTED COIL	
L8	IND CHOKE 4.7UH 10% LAQ	23642-553J
L9	IND CHOKE 4.7UH 10% LAQ	23642-553J
L10	IND CHOKE 4.7UH 10% LAQ	23642-553J
L11	IND CHOKE 4.7UH 10% LAQ	23642-553J
L12	IND CHOKE 4.7UH 10% LAQ	23642-553J
L13	ADJ. IND. 30NH 1 3/4 T	44290-799W
L14	ADJ. IND. 30NH 1 3/4 T	44290-799W
L15	ADJ. IND. 43NH 2 1/4 T	44290-800J
L16	ADJ. IND. 43NH 2 1/4 T	44290-800J
L17	ADJ, IND. 61NH 2 3/4 T	44290-801F
L18	ADJ, IND. 61NH 2 3/4 T	44290-801F
L19	ADJ. IND. 86NH 3 3/4 T	44290-802G
L20	ADJ. IND. 86NH 3 3/4 T	44290-802G
L21	ADJ. IND. 121NH 4 3/4 T	44290-803V
L22	ADJ. IND. 121NH 4 3/4 T	44290-803V
L23	ADJ. IND. 172NH 6 3/4 T	44290-804S
L24	ADJ. IND. 172NH 6 3/4 T	44290-804S
L25	IND CHOKE 4.7UH 10% LAQ	23642-553J
L26	IND CHOKE 4.7UH 10% LAQ	23642-553J
L27	IND CHOKE 4.7UH 10% LAQ	23642-553J
L28	IND CHOKE 4.7UH 10% LAQ	23642-553J
L30	PRINTED COIL	
L31	PRINTED COIL	

Circuit Ref	Description	Part Number
Unit AC3	- FILTER BOARD (continued)	
L33	IND CHOKE 4.7UH 10% LAQ	23642-553J
L34	IND CHOKE 4.7UH 10% LAQ	23642-553J
L36	IND CHOKE 4.7UH 10% LAQ	23642-553J
L37	IND CHOKE 68UH 10% LAQ	23642-560S
L38	IND CHOKE 68UH 10% LAQ	23642-560S
L39	IND CHOKE 68UH 10% LAQ	23642-560S
L40	IND CHOKE 68UH 10% LAQ	23642-560S
L41	IND CHOKE 1.8UH 5%	23642-495X
L42	IND CHOKE 1.8UH 5%	23642-495X
L43	IND CHOKE 3.0UH 5%	23642-474H
L44	IND CHOKE 3.0UH 5%	23642-474H
L45	IND CHOKE 4.3UH 5%	23642-466R
L46	IND CHOKE 4.3UH 5%	23642-466R
L47	IND CHOKE 6.2UH 5%	23642-455S
L48	IND CHOKE 6.2UH 5%	23642-455S
L49	IND CHOKE 8.2UH 5%	23642-468K
L50	IND CHOKE 8.2UH 5%	23642-468K
L51	IND CHOKE 12UH 5%	23642-456W
L52	IND CHOKE 12UH 5%	23642-456W
L53	IND CHOKE 68UH 10% LAQ	23642-560S
L54	IND CHOKE 68UH 10% LAQ	23642-560S
L55	IND CHOKE 68UH 10% LAQ	23642-560S
L56	IND CHOKE 68UH 10% LAQ	23642-560S
L57	IND CHOKE 68UH 10% LAQ	23642-560S
L58	IND CHOKE 1.5UH 5%	23642-494P
L59	IND CHOKE 1.5UH 5%	23642-494P
L60	IND CHOKE 68UH 10% LAQ	23642-560S
L61	IND CHOKE 68UH 10% LAQ	23642-560S
L62	IND CHOKE 68UH 10% LAQ	23642-560S
L63	IND CHOKE .82UH 5%	23642-454V
L64	IND CHOKE .82UH 5%	23642-454V
L65	IND CHOKE 68UH 10% LAQ	23642-560S
L66	IND CHOKE 68UH 10% LAQ	23642-560S
L90	IND CHOKE - 1.5TURNS	23642-908P
L91	RES. LEAD LENGTH	
L92	RES. LEAD LENGTH	
PLDF	CABLE COAX 12CM SMB-FEM/-	43129-537Y
R1	RES MF 360R 1/4W 2% 100PPM	24773-262T
R2	RES MF 1KO 1/4W 2% 100PPM	24773-273A
R3	RES MF 470R 1/4W 2% 100PPM	24773-265M
R4	RES MF 3KO 1/4W 2% 100PPM	24773-284J
R5	RES MF 3KO 1/4W 2% 100PPM	24773-284J

Circuit Ref	Description	Part Number
Unit AC3	- FILTER BOARD (continued)	
R6	RES MF 75R 1/4W 2% 100PPM	24773-246Y
R7	RES MF 1K5 1/4W 2% 100PPM	24773-277U
R8	RES CC 150R 1/8W 5%	24331-990D
R9	RES CC 150R 1/8W 5%	24331-990D
R10	RES CHIP 16R 5%	24681-043E
R11	RES CHIP 16R 5%	24681-043E
R12	RES MF 51R 1/4W 2% 100PPM	24773-242Z
R13	RES MF 51R 1/4W 2% 100PPM	24773-242Z
R14	RES MF 6K8 1/4W 2% 100PPM	24773-293D
R15	RES MF 6K8 1/4W 2% 100PPM	24773-293D
R16	RES MF 200R 1/4W 2% 100PPM	24773-256S
R17	RES MF 820R 1/4W 2% 100PPM	24773-271B
R18	RES MF 75R 1/4W 2% 100PPM	24773-246Y
R19	RES MF 2K4 1/4W 2% 100PPM	24773-282N
R20	RES MF 820R 1/4W 2% 100PPM	24773-271B
R21	RES MF 820R 1/4W 2% 100PPM	24773-271B
R22	RES MF 3K9 1/4W 2% 100PPM	24773-287V
R23	RES MF 360R 1/4W 2% 100PPM	24773-262T
R24	RES MF 470R 1/4W 2% 100PPM	24773-265M
R25	RES MF 5K6 1/4W 2% 100PPM	24773-291S
R26	RES MF 300R 1/4W 2% 100PPM	24773-260W
R27	RES MF 300R 1/4W 2% 100PPM	24773-260W
R28	RES MF 6K8 1/4W 2% 100PPM	24773-293D
R29	RES MF 270R 1/4W 2% 100PPM	24773-259T
R30	RES MF 240R 1/4W 2% 100PPM	24773-258D
R31	RES MF 10K 1/4W 2% 100PPM	24773-297M
R32	RES MF 240R 1/4W 2% 100PPM	24773-258D
R33	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R34	RES MF 470R 1/4W 2% 100PPM	24773-265M
R35	RES MF 1K5 1/4W 2% 100PPM	24773-277U
R36	RES MF 470R 1/4W 2% 100PPM	24773-265M
R37	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R38	RES MF 470R 1/4W 2% 100PPM	24773-265M
R39	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R40	RES MF 470R 1/4W 2% 100PPM	24773-265M
R42	RES MF 470R 1/4W 2% 100PPM	24773-265M
R43	RES MF 680R 1/4W 2% 100PPM	24773-269K
R44	RES MF 680R 1/4W 2% 100PPM	24773-269K
R45	RES MF 680R 1/4W 2% 100PPM	24773-269K
R46	RES MF 680R 1/4W 2% 100PPM	24773-269K
R47	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R48	RES MF 470R 1/4W 2% 100PPM	24773-265M
R50	RES MF 470R 1/4W 2% 100PPM	24773-265M
R51	RES MF 1K0 1/4W 2% 100PPM	24773-273A

Circuit Ref	Description	Part Number
Unit AC3	- FILTER BOARD (continued)	
R52	RES MF 470R 1/4W 2% 100PPM	24773-265M
R53	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R54	RES MF 1K5 1/4W 2% 100PPM	24773-277U
R55	RES MF 470R 1/4W 2% 100PPM	24773-265M
R56	RES MF 470R 1/4W 2% 100PPM	24773-265M
R57	RES MF 470R 1/4W 2% 100PPM	24773-265M
R92	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R93	RES MF 470R 1/4W 2% 100PPM	24773-265M
SKCS	CON RF SMB MALE 50 PCB STR	23444-334Y
TR1	TR NSI BFR96S 15V 5G - AMP	28452-172N
TR2	TR NSI BFR96S 15V 5G - AMP	28452-172N
TR3	TR NSI 2N2369 15V 500M - SW	28452-197H
Unit AC4	- OUTPUT AMPLIFIER	
19. When ordering, prefix circuit reference with AC4		
	Complete unit	44828-439A
C1	CAP CER 39N 50V 20% CHIP	26386-757H
C2	CAP ELEC 4U7 35V 20% SUBMIN	26421-108A
C3	CAP CER 1N0 63V 10% PLATE	26383-585M
C4	CAP CER 39N 50V 20% CHIP	26386-757H
C5	CAP CER 39N 50V 20% CHIP	26386-757H
C6	CAP CER 2P2 63V .5PF PLATE	26343-491C
C7	CAP CER 100P 63V 2% PLATE	26343-477V
C8	CAP CER 39N 50V 20% CHIP	26386-757H
C9	CAP ELEC 4U7 35V 20% SUBMIN	26421-108A
C10	CAP CER 1N0 63V 10% PLATE	26383-585M
C11	CAP CER 39N 50V 20% CHIP	26386-757H
C12	CAP CER 39N 50V 20% CHIP	26386-757H
C13	CAP CER 2P2 63V .5PF PLATE	26343-491C
C14	CAP CER 100P 63V 2% PLATE	26343-477V
C15	CAP CER 4P7 63V .5PF PLATE	26343-485P
C16	CAP CER 1N0 63V 10% PLATE	26383-585M
C17	CAP ELEC 4U7 35V 20% SUBMIN	26421-108A
C18	CAP ELEC 470N 50V 20% SUBMIN	26421-104C
C19	CAP CER 39N 50V 20% CHIP	26386-757H
C20	CAP CER 39N 50V 20% CHIP	26386-757H

Circuit Ref	Description	Part Number
Unit AC4	- OUTPUT AMPLIFIER (continued)	
C21	CAP CER 1P8 63V .5PF PLATE	26343-490M
C22	CAP CER 220N 50V 10% CHIP	26340-356D
C23	CAP CER 10P 50V 5% CHIP	26343-767B
C24	CAP CER 100P 63V 2% PLATE	26343-477V
C25	CAP ELEC 4U7 35V 20% SUBMIN	26421-108A
C26	CAP ELEC 470N 50V 20% SUBMIN	26421-104C
C27	CAP CER 4P7 63V .5PF PLATE	26343-485P
C28	CAP CER 4P7 63V .5PF PLATE	26343-485P
C29	CAP ELEC 4U7 35V 20% SUBMIN	26421-108A
C30	CAP CER 220N 50V 10% CHIP	26340-356D
C31	CAP CER 4P7 63V .5PF PLATE	26343-485P
C32	CAP CER 4P7 63V .5PF PLATE	26343-485P
C33	CAP CER 10N 50V 20% CHIP	26386-754K
C34	CAP CER 10N 50V 20% CHIP	26386-754K
C35	CAP CER 10N 100V 20%+ DISC	26383-055L
C36	CAP ELEC 470N 50V 20% SUBMIN	26421-104C
C37	CAP ELEC 470N 50V 20% SUBMIN	26421-104C
C38	CAP CER 10N 100V 20%+ DISC	26383-055L
C39	CAP ELEC 470N 50V 20% SUBMIN	26421-104C
C40	CAP CER 10N 100V 20%+ DISC	26383-055L
C41	CAP CER 10N 100V 20%+ DISC	26383-055L
C42	CAP ELEC 470N 50V 20% SUBMIN	26421-104C
C43	CAP CER 10N 100V 20%+ DISC	26383-055L
C44	CAP CER 10N 100V 20%+ DISC	26383-055L
C45	CAP ELEC 470N 50V 20% SUBMIN	26421-104C
C46	CAP CER 10N 100V 20%+ DISC	26383-055L
C47	CAP PETP 100N 100V 10% RAD	26582-211B
C48	CAP CER 1N0 63V 10% PLATE	26383-585M
C49	CAP ELEC 4U7 35V 20% SUBMIN	26421-108A
C50	CAP ELEC 4U7 35V 20% SUBMIN	26421-108A
C51	CAP ELEC 4U7 35V 20% SUBMIN	26421-108A
C52	CAP CER 10N 100V 20%+ DISC	26383-055L
C53	CAP CER 10N 100V 20%+ DISC	26383-055L
C54	CAP CER 10N 100V 20%+ DISC	26383-055L
C55	CAP CER 10N 100V 20%+ DISC	26383-055L
C56	CAP CER 10N 100V 20%+ DISC	26383-055L
C57	CAP CER 10N 100V 20%+ DISC	26383-055L
C58	CAP PETP 10N 400V 10% RAD	26582-232W
C59	CAP CER 39N 50V 20% CHIP	26386-757H
C60	CAP CER 1N0 63V 10% PLATE	26383-585M
C61	CAP CER 2P2 63V .5PF PLATE	26343-491C
C62	CAP CER 1P8 63V .5PF PLATE	26343-490M
C63	CAP CER 68P 63V 2% PLATE	26343-475F
C64	CAP CER 1N0 63V 10% PLATE	26383-585M

Circuit Ref	Description	Part Number
Unit AC4	- OUTPUT AMPLIFIER (continued)	
D1	DI SIL 1N4448 75V JUNC	28336-246M
D2	DI PIN 5082-3379 50V	28383-997T
D3	DI SIL 1N4448 75V JUNC	28336-246M
D4	DI PIN 5082-3379 50V	28383-997T
D5	DI SIL BA482 35V JUNC	28335-675R
D6	DI SIL 1N4448 75V JUNC	28336-246M
D7	DI SIL 1N4448 75V JUNC	28336-246M
D8	DI SIL 1N4448 75V JUNC	28336-246M
D9	DI SIL 1N4448 75V JUNC	28336-246M
D10	DI SIL 1N4448 75V JUNC	28336-246M
D11-D13 D16,D17	} DIODE HOT CARR HP 5082-2826 (Matched set of 5)	44529-105P
D14	DI SIL 1N4448 75V JUNC	28336-246M
D15	DI SIL 1N4448 75V JUNC	28336-246M
D18	DI PIN 5082-3379 50V	28383-997T
D19	DI PIN 5082-3379 50V	28383-997T
IC1	ICA AMP TL074CN QUAD FET I/P	28461-349H
IC2	ICD FF D 7474 DUAL +EDG TR	28462-002N
IC3	ICA AMP TL074CN QUAD FET I/P	28461-349H
IC4	ICA DAC AD7524JN 8BIT !	28469-400R
IC5	ICD INV 74LS04 HEX	28469-171L
IC6	ICA DAC AD7522LN 10BIT MOS !	28469-402K
L1	RES. LEAD LENGTH	
L2	PRINTED COIL	
L3	RES. LEAD LENGTH	
L4	PRINTED COIL	
L5	RES. LEAD LENGTH	
L6	IND CHOKE - 1.5TURNS	23642-908P
L7	PRINTED COIL	
L8	IND CHOKE 1000UH 10% .18A	23642-620Y
L9	IND CHOKE - 1.5TURNS	23642-908P
L10	IND CHOKE - 1.5TURNS	23642-908P
L11	IND CHOKE 1000UH 10% LAQ	23642-567C
L12	IND CHOKE 1000UH 10% LAQ	23642-567C
L13	IND CHOKE 1000UH 10% LAQ	23642-567C
PLCS	CABLE COAX 18CM SMB-FEM/-	43129-668H

Circuit Ref	Description	Part Number
Unit AC4	- OUTPUT AMPLIFIER (continued)	
R1	RES MF 750R 1/4W 2% 100PPM	24773-270R
R2	RES MF 10K 1/4W 2% 100PPM	24773-297M
R3	RES MF 620R 1/4W 2% 100PPM	24773-268B
R4	RES MF 2K7 1/4W 2% 100PPM	24773-283L
R5	RES MF 33R 1/4W 2% 100PPM	24773-237K
R6	RES MF 240R 1/4W 2% 100PPM	24773-258D
R7	RES CC 200R 1/8W 5%	24331-999A
R8	RES CHIP 16R 5%	24681-043E
R9	RES CHIP 22R 5%	24681-044U
R10	RES MF 750R 1/4W 2% 100PPM	24773-270R
R11	RES MF 10K 1/4W 2% 100PPM	24773-297M
R12	RES MF 620R 1/4W 2% 100PPM	24773-268B
R13	RES MF 620R 1/4W 2% 100PPM	24773-268B
R14	RES MF 2K7 1/4W 2% 100PPM	24773-283L
R15	RES MF 33R 1/4W 2% 100PPM	24773-237K
R16	RES MF 240R 1/4W 2% 100PPM	24773-258D
R17	RES CC 200R 1/8W 5%	24331-999A
R18	RES CHIP 16R 5%	24681-043E
R19	RES CHIP 22R 5%	24681-044U
R20	RES MF 620R 1/4W 2% 100PPM	24773-268B
R21	RES MF 620R 1/4W 2% 100PPM	24773-268B
R22	RES MF 3K3 1/4W 2% 100PPM	24773-285F
R23	RES MF 10K 1/4W 2% 100PPM	24773-297M
R24	RES MF 10K 1/4W 2% 100PPM	24773-297M
R25	RES MF 150R 1/4W 2% 100PPM	24773-253F
R26	RES CHIP 22R 5%	24681-044U
R27	RES MF 750R 1/4W 2% 100PPM	24773-270R
R28	RES MF 10K 1/4W 2% 100PPM	24773-297M
R29	RES MF 2K7 1/4W 2% 100PPM	24773-283L
R30	RES CC 82R 1/8W 5%	24331-996R
R31	RES MF 22R 1/4W 2% 100PPM	24773-233M
R32	RES MO 150R 1/2W 2% 250PPM	24573-053K
R33	RES CHIP 16R 5%	24681-043E
R34	RES CHIP 16R 5%	24681-043E
R35	RES CHIP 16R 5%	24681-043E
R36	RES MF 1KO 1/4W 2% 100PPM	24773-273A
R37	RES MF 15K 1/4W 2% 100PPM	24773-301P
R38	RES MF 1KO 1/4W 2% 100PPM	24773-273A
R39	RES MF 10R 1/4W 2% 100PPM	24773-225W
R40	RES CHIP 16R 5%	24681-043E

Circuit Ref	Description	Part Number
Unit AC4	- OUTPUT AMPLIFIER (continued)	
R41	RES CHIP 16R 5%	24681-043E
R42	RES MF 200R 1/4W 2% 100PPM	24773-256S
R43	RES MG 4M7 1/4W 5%	24321-881F
R44	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R45	RES MG 4M7 1/4W 5%	24321-881F
R46	RES MG 4M7 1/4W 5%	24321-881F
R47	RES MF 50R0 1/4W 1% 100PPM NI	24762-558R
R48	RES MF 10K 1/4W 2% 100PPM	24773-297M
R49	RES MF 200R 1/4W 2% 100PPM	24773-256S
R50	RES MF 10K 1/4W 2% 100PPM	24773-297M
R51	RES MF 820R 1/4W 2% 100PPM	24773-271B
R52	RES MF 27R 1/4W 2% 100PPM	24773-235R
R53	RES MF 100K 1/4W 2% 100PPM	24773-321L
R54	RES MF 200R 1/4W 2% 100PPM	24773-256S
R55	RES MF 10K 1/4W 2% 100PPM	24773-297M
R56	RES MF 10K 1/4W 2% 100PPM	24773-297M
R57	RES MF 100K 1/4W 2% 100PPM	24773-321L
R58	RES MF 820R 1/4W 2% 100PPM	24773-271B
R59	RES MF 27R 1/4W 2% 100PPM	24773-235R
R60	RES MF 100K 1/4W 2% 100PPM	24773-321L
R61	RES MF 100K 1/4W 2% 100PPM	24773-321L
R62	RES MF 10K 1/4W 2% 100PPM	24773-297M
R63	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R64	RES MF 200R 1/4W 2% 100PPM	24773-256S
R65	RES MF 3K3 1/4W 2% 100PPM	24773-285F
R66	RES MF 150R 1/4W 2% 100PPM	24773-253F
R67	RES MF 51R 1/4W 2% 100PPM	24773-242Z
R68	RES MF 15K 1/4W 2% 100PPM	24773-301P
R69	RES MF 30K 1/4W 2% 100PPM	24773-308A
R70	RES MF 15K 1/4W 2% 100PPM	24773-301P
R71	RES MF 10K 1/4W 2% 100PPM	24773-297M
R72	RES MF 3K3 1/4W 2% 100PPM	24773-285F
R73	RES MF 10K 1/4W 2% 100PPM	24773-297M
R74	RES MF 68K 1/4W 2% 100PPM	24773-317N
R75	RES MF 68K 1/4W 2% 100PPM	24773-317N
R76	RES NET 10K 5% 8DIL	24681-511P
R77	RV CERM 1K0 LIN .5W 10% HORZ	25711-638G
R78	RES MF 2K0 1/4W 2% 100PPM	24773-280U
R79	RES MF 15K 1/4W 2% 100PPM	24773-301P
R80	RES MF 2K0 1/4W 2% 100PPM	24773-280U
R81	RES MF 10K 1/4W 2% 100PPM	24773-297M
R82	RES MF 1K5 1/4W 2% 100PPM	24773-277U

Circuit Ref	Description	Part Number
Unit AC4	- OUTPUT AMPLIFIER (continued)	
R84	RES MF 3KO 1/4W 2% 100PPM	24773-284J
R85	RES MF 3K3 1/4W 2% 100PPM	24773-285F
R86	RV CERM 500R LIN .5W 10% HORZ	25711-637F
R87	RES MF 150R 1/4W 2% 100PPM	24773-253F
R89	RV CERM 50K LIN .5W 10% HORZ	25711-643S
R90	RES MF 22K 1/4W 2% 100PPM	24773-305R
R91	RES MG 3M3 1/4W 5%	24321-879G
R92	RES MG 3M3 1/4W 5%	24321-879G
R93	RES MF 1KO 1/4W 2% 100PPM	24773-273A
R94	RES MF 10K 1/4W 2% 100PPM	24773-297M
R95	RV CERM 10K LIN .5W 10% HORZ	25711-641G
R96	RES MF 8K2 1/4W 2% 100PPM	24773-295P
R97	RES MF 2K7 1/4W 2% 100PPM	24773-283L
R98	RES MF 620R 1/4W 2% 100PPM	24773-268B
*R99	RES MF 68K 1/4W 2% 100PPM	24773-317N
SKAY	CABLE COAX 12CM SMC-MALE/-	43129-679G
TR1	TR PSI BC308B 20V 130M - GEN	28433-455R
TR2	TR NSI BFR91A 12V 5G - AMP	28451-694H
TR3	TR PSI BC308B 20V 130M - GEN	28433-455R
TR4	TR NSI BFR91A 12V 5G - AMP	28451-694H
TR5	TR PSI BC308B 20V 130M - GEN	28433-455R
TR6	TR NSI BC209C 20V 150M - GEN	28452-771P
TR7	TR PSI BC308B 20V 130M - GEN	28433-455R
TR8	TR NSI BFR96S 15V 5G - AMP	28452-172N
TR9	TR PSI BC308B 20V 130M - GEN	28433-455R
TR10	TR NSI BFQ34 18V 3G - 2.25W	28452-247V
TR11	TR NSI 2N2369 15V 500M - SW	28452-197H
TR12,TR14	TR NJF J310 25V - 24MA (MATCHED PAIR)	44529-114K
TR13	TR NSI 2N2369 15V 500M - SW	28452-197H
TR15	TR NSI 2N2369 15V 500M - SW	28452-197H
TR16	TR PSI BC308B 20V 130M - GEN	28433-455R
TR17	TR NSI BC209C 20V 150M - GEN	28452-771P
X1	FERRITE BEAD	23635-404Y
Unit AC5	- AMPLITUDE MODULATOR AC5	

20. When ordering, prefix circuit reference with AC5

	Complete unit	44828-440B
C1	CAP CER 1NO 63V 10% PLATE	26383-585M
C2	CAP CER 39N 50V 20% CHIP	26386-757H
C3	CAP CER 10N 100V 20%+ DISC	26383-055L

Circuit Ref	Description	Part Number
Unit AC5	- AMPLITUDE MODULATOR AC5 (continued)	
C4	CAP CER 39N 50V 20% CHIP	26386-757H
C5	CAP CER 1NO 63VV 10% PLATE	26383-585M
C6	CAP CER 10N 100V 20%+ DISC	26383-055L
C7	CAP CER 39N 50V 20% CHIP	26386-757H
C8	CAP CER 39N 50V 20% CHIP	26386-757H
C9	CAP CER 39N 50V 20% CHIP	26386-757H
C10	CAP ELEC 4U7 35V 20% SUBMIN	26421-108A
C11	CAP ELEC 4U7 35V 20% SUBMIN	26421-108A
C12	CAP ELEC 4U7 35V 20% SUBMIN	26421-108A
C13	CAP CER 10N 100V 20%+ DISC	26383-055L
C14	CAP CER 10N 100V 20%+ DISC	26383-055L
C15	CAP CER 10N 100V 20%+ DISC	26383-055L
C16	CAP CER 10N 100V 20%+ DISC	26383-055L
IC1	MOD HYB ON345 VHF/UHF AMP SIL	28461-351Z
IC2	ICD FF D 7474 DUAL +EDG TR	28462-002N
IC3	ICA AMP TL071CP FET I/P DIL8	28461-347A
IC4	DAC AD7524JN 8-BIT !	28469-400R
R1	RES CC 51R 1/8W 5%	24331-989P
R2	RES CC 270R 1/8W 5%	24331-992P
R3	RES CHIP 16R 5%	24681-043E
R4	RES CC 270R 1/8W 5%	24331-992P
R5	RES MF 330R 1/$W 2% 100PPM	24773-261D
R6	RES CC 22R 1/8W 5%	24331-988T
R7	RES CC 51R 1/8W 5%	24331-989P
R8	RES MF 5K1 1/4W 2% 100PPM	24773-290V
R9	RES MF 10K 1/4W 2% 100PPM	24773-297M
R10	RES MF 240R 1/4W 2% 100PPM	24773-258D
R11	RES MF 240R 1/4W 2% 100PPM	24773-258D
R12	RES CHIP 16R 5%	24681-043E
R13	RES MF 3K6 1/4W 2% 100PPM	24773-286G
R14	RES MF 510R 1/4W 2% 100PPM	24773-266C
R15	RES MF 330R 1/4W 2% 100PPM	24773-261D
R16	RES MET 10K 5% SDIL	24681-511P
R17	RES MF 10K 1/4W 2% 100PPM	24773-297M
R18	RES MF 3KO 1/4W 2% 100PPM	24773-284J
R20	RES MF 10K 1/4W 2% 100PPM	24773-297M
R21	RES MF 18K 1/4W 2% 100PPM	24773-303M
R22	RES MF 18K 1/4W 2% 100PPM	24773-303M
R23	RV CERM 500R LIN .5W 10% HORZ	25711-637F
SKDE	CON RF SMB MALE 50 PCB STR	23444-334Y
SKDF	CON RF SMB MALE 50 PCB STR	23444-334Y

Circuit Ref	Description	Part Number
Unit AC5	- AMPLITUDE MODULATOR AC5 (continued)	
TR1	TR NSI BFR90 15V 5G - AMP	28452-167U
TR2	TR PSI BC308B 20V 130M - GEN	28433-455R
TR3	TR NSI BC209C 20V 150M - GEN	28452-771P
X1	MOD RF SBL-1 DOUBLE BAL MIXER	28531-002A
X2	MOD RF TFM2 DOUBLE BAL MIXER	28531-003Z
	S/C ACC SKT DIL 16 LOW PROFILE	28488-041E
Unit AC13	- FILTER & FREQ DOUBLER BOARD (2019A ONLY)	
21. When ordering, prefix circuit reference with AC13		
	Complete unit	44828-437B
C1	CAP CER 39N 50V 20% CHIP	26386-757H
C2	CAP CER 10N 100V 20%+ DISC	26383-055L
C3	CAP CER 39N 50V 20% CHIP	26386-757H
C4	CAP CER 39N 50V 20% CHIP	26386-757H
C5	CAP CER 39N 50V 20% CHIP	26386-757H
C6	CAP CER 39N 50V 20% CHIP	26386-757H
C7	CAP CER 39N 50V 20% CHIP	26386-757H
C8	CAP CER 39N 50V 20% CHIP	26386-757H
C9	CAP CER 39N 50V 20% CHIP	26386-757H
C10	CAP CER 10N 100V 20%+ DISC	26383-055L
C11	CAP CER 47N 25V 20% DISC	26383-017U
C12	CAP CER 10N 100V 20%+ DISC	26383-055L
C13	CAP CER 10N 100V 20%+ DISC	26383-055L
C14	CAP CER 10N 100V 20%+ DISC	26383-055L
C15	CAP CER 10N 100V 20%+ DISC	26383-055L
C16	CAP CER 10N 100V 20%+ DISC	26383-055L
C18	CAP CER 10N 100V 20%+ DISC	26383-055L
C19	CAP CER 10N 100V 20%+ DISC	26383-055L
C20	CAP CER 8P2 63V .5PF PLATE	26343-488C
C21	CAP CER 12P 63V 5% PLATE	26343-497H
C22	CAP CER 8P2 63V .5PF PLATE	26343-488C
C23	CAP CER 1NO 63V 10% PLATE	26383-585M
C24	CAP CER 1NO 63V 10% PLATE	26383-585M
C25	CAP CER 1NO 63V 10% PLATE	26383-585M
C26	CAP CER 1NO 63V 10% PLATE	26383-585M
C27	CAP CER 1NO 63V 10% PLATE	26383-585M
C28	CAP CER 6P8 63V .5PF PLATE	26343-463A
C29	CAP CER 18P 63V 5% PLATE	26343-468Y
C30	CAP CER 22P 63V 5% PLATE	26343-469N
C31	CAP CER 18P 63V 5% PLATE	26343-468Y

Circuit Ref	Description	Part Number
Unit AC13	- FILTER & FREQ DOUBLER BOARD (continued)	
C32	CAP CER 22P 63V 5% PLATE	26343-469N
C33	CAP CER 33P 63V 5% PLATE	26343-471Y
C34	CAP CER 22P 63V 5% PLATE	26343-469N
C35	CAP CER 33P 63V 5% PLATE	26343-471Y
C36	CAP CER 47P 63V 5% PLATE	26343-473L
C37	CAP CER 33P 63V 5% PLATE	26343-471Y
C38	CAP CER 47P 63V 5% PLATE	26343-473L
C39	CAP CER 68P 63V 2% PLATE	26343-475F
C40	CAP CER 47P 63V 5% PLATE	26343-473L
C41	CAP CER 68P 63V 2% PLATE	26343-475F
C42	CAP CER 100P 63V 2% PLATE	26343-477V
C43	CAP CER 68P 63V 2% PLATE	26343-475F
C44	CAP CER 82P 63V 2% PLATE	26343-476G
C45	CAP CER 150P 63V 2% PLATE	26343-479W
C46	CAP CER 82P 63V 2% PLATE	26343-476G
C47	CAP CER 1N0 63V 10% PLATE	26383-585M
C48	CAP CER 1N0 63V 10% PLATE	26383-585M
C49	CAP CER 1N0 63V 10% PLATE	26383-585M
C50	CAP CER 1N0 63V 10% PLATE	26383-585M
C51	CAP CER 12P 63V 5% PLATE	26343-497H
C52	CAP CER 18P 63V 5% PLATE	26343-498E
C53	CAP CER 12P 63V 5% PLATE	26343-497H
C54	CAP CER 1N0 63V 10% PLATE	26383-585M
C55	CAP CER 1P8 63V .5PF PLATE	26343-456C
C56	CAP CER 1N0 63V 10% PLATE	26383-585M
C57	CAP CER 1N0 63V 10% PLATE	26383-585M
C58	CAP CER 1N0 63V 10% PLATE	26383-585M
C59	CAP CER 10N 100V 20%+ DISC	26383-055L
C60	CAP CER 10N 100V 20%+ DISC	26383-055L
C61	CAP CER 10N 100V 20%+ DISC	26383-055L
C62	CAP CER 10N 100V 20%+ DISC	26383-055L
C63	CAP CER 2P2 63V .5PF PLATE	26343-457R
C64	CAP CER 100P 63V 2% PLATE	26343-477V
C65	CAP CER 120P 63V 2% PLATE	26343-478S
C66	CAP CER 33P 63V 5% PLATE	26343-471Y
C67	CAP CER 100P 63V 2% PLATE	26343-477V
C68	CAP CER 22P 63V 5% PLATE	26343-469N
C69	CAP CER 150P 63V 2% PLATE	26343-479W
C70	CAP CER 180P 63V 2% PLATE	26343-480V
C71	CAP CER 150P 63V 2% PLATE	26343-479W
C72	CAP CER 22P 63V 5% PLATE	26343-469N
C73	CAP CER 180P 63V 2% PLATE	26343-480V

Ref	Description	Number
Unit AC13	- FILTER & FREQ DOUBLER BOARD (continued)	
C74	CAP CER 270P 63V 2% PLATE	26343-482W
C75	CAP CER 180P 63V 2% PLATE	26343-480V
C76	CAP CER 270P 63V 2% PLATE	26343-482W
C77	CAP CER 390P 63V 10% PLATE	26383-598Y
C78	CAP CER 270P 63V 2% PLATE	26343-482W
C79	CAP CER 470P 63V 10% PLATE	26383-582T
C80	CAP CER 560P 63V 10% PLATE	26383-581D
C81	CAP CER 470P 63V 10% PLATE	26383-582T
C82	CAP CER 560P 63V 10% PLATE	26383-581D
C83	CAP CER 820P 63V 10% PLATE	26383-584X
C84	CAP CER 47P 63V 5% PLATE	26343-473L
C85	CAP CER 560P 63V 10% PLATE	26383-581D
C86	CAP CER 10N 100V 20%+ DISC	26383-055L
C87	CAP CER 10N 100V 20%+ DISC	26383-055L
C88	CAP CER 10N 100V 20%+ DISC	26383-055L
C89	CAP CER 10N 100V 20%+ DISC	26383-055L
C90	CAP CER 68P 63V 2% PLATE	26343-475F
C91	CAP CER 82P 63V 2% PLATE	26343-476G
C92	CAP CER 68P 63V 2% PLATE	26343-475F
C93	CAP CER 33P 63V 5% PLATE	26343-471Y
C94	CAP CER 2P2 63V .5PF PLATE	26343-457R
C95	CAP CER 10N 100V 20%+ DISC	26383-055L
C96	CAP CER 47P 63V 5% PLATE	26343-473L
C97	CAP CER 68P 63V 2% PLATE	26343-475F
C98	CAP CER 47P 63V 5% PLATE	26343-473L
C99	CAP CER 10N 100V 20%+ DISC	26383-055L
C100	CAP CER 10N 100V 20%+ DISC	26383-055L
C101	CAP CER 1N0 63V 10% PLATE	26383-585M
C102	CAP ELEC 4U7 35V 20% SUBMIN	26421-108A
C103	CAP ELEC 4U7 35V 20% SUBMIN	26421-108A
C104	CAP ELEC 4U7 35V 20% SUBMIN	26421-108A
C106	CAP CER 39N 50V 20% CHIP	26386-757H
C107	CAP CER 39N 50V 20% CHIP	26386-757H
C108	CAP CER 39N 50V 20% CHIP	26386-757H
C109	CAP CER 39N 50V 20% CHIP	26386-757H
C110	CAP CER 39N 50V 20% CHIP	26386-757H
C111	CAP CER 1N0 63V 10% PLATE	26383-585M
C112	CAP CER 39N 50V 20% CHIP	26386-757H
C113	CAP CER 10P 63V .5PF PLATE	26343-492R
C114	CAP CER 39N 50V 20% CHIP	26386-757H
C115	CAP CER 2P2 63V .5PF PLATE	26343-491C
C116	CAP CER 10N 100V 20%+ DISC	26383-055L
C117	CAP CER 10N 100V 20%+ DISC	26383-055L

Circuit Part

Circuit Ref	Description	Part Number
Unit AC13	- FILTER & FREQ DOUBLER BOARD (continued)	
C118	CAP CER 2P7 63V .5PF PLATE	26343-458B
C119	CAP CER 15P 63V 5% PLATE	26343-467U
C120	CAP CER 8P2 63V .5PF PLATE	26343-464Z
C121	CAP CER 1P0 63V .5P PLATE	26343-502Z
C122	CAP CER 1N0 63V 10% PLATE	26383-585M
C123	CAP CER 10P 63V .5PF PLATE	26343-465H
C124	CAP CER 5P6 63V .5PF PLATE	26343-462K
C125	CAP CER 1P0 63V .5P PLATE	26343-502Z
C126	CAP CER 39N 50V 20% CHIP	26386-757H
C127	CAP CER 39N 50V 20% CHIP	26386-757H
C128	CAP CER 1N0 63V 10% PLATE	26383-585M
C129	CAP CER 39N 50V 20% CHIP	26386-757H
C130	CAP CER 1N0 63V 10% PLATE	26383-585M
C131	CAP CER 39N 50V 20% CHIP	26386-757H
C132	CAP CER 1N0 63V 10% PLATE	26383-585M
C135	CAP CER 3P3 63V .5PF PLATE	26343-459K
C137	CAP CER 5P6 63V .5PF PLATE	26343-462K
C138	CAP CER 2P7 63V .5PF PLATE	26343-458B
C139	CAP CER 1N0 63V 10% PLATE	26383-585M
C140	CAP CER 3P9 63V .5PF PLATE	26343-460R
C141	CAP CER 2P2 63V .5PF PLATE	26343-457R
C142	CAP CER 10N 100V 20%+ DISC	26383-055L
C143	CAP CER 10N 100V 20%+ DISC	26383-055L
C144	CAP CER 10N 100V 20%+ DISC	26383-055L
C145	CAP CER 1N0 63V 10% PLATE	26383-585M
C146	CAP CER 1N0 63V 10% PLATE	26383-585M
C147	CAP CER 1N0 63V 10% PLATE	26383-585M
C148	CAP CER 1N0 63V 10% PLATE	26383-585M
C149	CAP CER 2P7 63V .5PF PLATE	26343-484T
C151	CAP CER 4P7 63V .5PF PLATE	26343-461B
C152	CAP CER 1N0 63V 10% PLATE	26383-585M
D1	DI SIL BA482 35V JUNC	28335-675R
D2	DI SIL BA482 35V JUNC	28335-675R
D3	DI SIL 1N4148 75V JUNC	28336-676J
D4	DI SIL 1N4148 75V JUNC	28336-676J
D5	DI SIL BA482 35V JUNC	28335-675R
D6	DI SIL BA482 35V JUNC	28335-675R
D7	DI SIL BA482 35V JUNC	28335-675R
D8	DI SIL BA482 35V JUNC	28335-675R
D9	DI SIL BA482 35V JUNC	28335-675R
D10	DI SIL BA482 35V JUNC	28335-675R

Circuit Ref	Description	Part Number
Unit AC13	- FILTER & FREQ DOUBLER BOARD (continued)	
D11	DI SIL BA482 35V JUNC	28335-675R
D12	DI SIL BA482 35V JUNC	28335-675R
D13	DI SIL BA482 35V JUNC	28335-675R
D14	DI SIL BA482 35V JUNC	28335-675R
D15	DI SIL BA482 35V JUNC	28335-675R
D16	DI SIL BA482 35V JUNC	28335-675R
D17	DI SIL BA482 35V JUNC	28335-675R
D18	DI SIL BA482 35V JUNC	28335-675R
D19	DI SIL BA482 35V JUNC	28335-675R
D20	DI SIL BA482 35V JUNC	28335-675R
D21	DI SIL BA482 35V JUNC	28335-675R
D22	DI SIL BA482 35V JUNC	28335-675R
D23	DI SIL BA482 35V JUNC	28335-675R
D24	DI SIL BA482 35V JUNC	28335-675R
D25	DI SIL BA482 35V JUNC	28335-675R
D26	DI SIL BA482 35V JUNC	28335-675R
D27	DI SIL BA482 35V JUNC	28335-675R
D28	DI SIL BA482 35V JUNC	28335-675R
D29	DI SIL BA482 35V JUNC	28335-675R
D30	DI SIL BA482 35V JUNC	28335-675R
D31	DI SIL BA482 35V JUNC	28335-675R
D32	DI SIL BA482 35V JUNC	28335-675R
D33	DI SIL BA482 35V JUNC	28335-675R
D34	DI SIL BA482 35V JUNC	28335-675R
D35	DI SIL BA482 35V JUNC	28335-675R
D36	DI SIL BA482 35V JUNC	28335-675R
D37	DI SIL BA482 35V JUNC	28335-675R
D38	DI SIL BA482 35V JUNC	28335-675R
D39	DI SIL BA482 35V JUNC	28335-675R
D40	DI SIL BA482 35V JUNC	28335-675R
D41	DI SIL BA482 35V JUNC	28335-675R
D42	DI SIL BA482 35V JUNC	28335-675R
D43	DI SIL BA482 35V JUNC	28335-675R
D44	DI SIL BA482 35V JUNC	28335-675R
D45	DI SIL BA482 35V JUNC	28335-675R
D46	DI SIL BA482 35V JUNC	28335-675R
D47	DI SIL BA482 35V JUNC	28335-675R
D49	DI SIL BA482 35V JUNC	28335-675R
D50	DI SIL BA482 35V JUNC	28335-675R
D51	DI SIL BA482 35V JUNC	28335-675R
D52	DI SIL BA482 35V JUNC	28335-675R
D53	DI SIL BA482 35V JUNC	28335-675R
D54	DI SIL 1N4148 75V JUNC	28336-676J

Circuit Ref	Description		Part Number
Unit AC13	- FILTER & FREQ DOUBLER BOARD (continued)		
D55	DIODE MATCHED SET OF 3	!	44529-058G
D56	DIODE MATCHED SET OF 3	!	44529-058G
D57	DIODE MATCHED SET OF 3	!	44529-058G
D58	DI SIL 1N4148 75V JUNC		28336-676J
D59	DI SIL BA482 35V JUNC		28335-675R
D60	DI SIL BA482 35V JUNC		28335-675R
D61	DI SIL BA482 35V JUNC		28335-675R
D62	DI SIL BA482 35V JUNC		28335-675R
D63	DI SIL 1N4148 75V JUNC		28336-676J
D64	DI SIL BA482 35V JUNC		28335-675R
D65	DI SIL BA482 35V JUNC		28335-675R
D66	DI SIL BA482 35V JUNC		28335-675R
D67	DI SIL BA482 35V JUNC		28335-675R
D68	DI SIL BA482 35V JUNC		28335-675R
D69	DI SIL BA482 35V JUNC		28335-675R
D70	DI SIL BA482 35V JUNC		28335-675R
D71	DI SIL BA482 35V JUNC		28335-675R
D72	DI SIL BA482 35V JUNC		28335-675R
D73	DI SIL BA482 35V JUNC		28335-675R
D74	DI H/CARR HP 5082-2835		28349-006H
D75	DI H/CARR HP 5082-2835		28349-006H
IC1	ICD DEC/DMX 74LS138 3-8		28465-027F
IC2	ICD FF D 74LS273 OCT +EDG TR		28462-615U
IC3	ICD FF D 74LS273 OCT +EDG TR		28462-615U
IC4	ICD BUFF 7407 HEX O/C		28469-703X
IC5	ICD BUFF 7406 HEX O/C INV 30V		28469-158A
IC6	ICD FF D 74LS175 QUAD +EDG TR		28462-614E
IC7	ICD BUFF 7407 HEX O/C		28469-703X
IC8	ICA AMP UA741CN GP DIL8		28461-304T
L1	IND CHOKE 68UH 10% LAQ		23642-560S
L2	IND CHOKE 4.7UH 10% LAQ		23642-553J
L3	IND CHOKE 68UH 10% LAQ		23642-560S
L4	IND CHOKE - 1.5TURNS		23642-908P
L5	IND CHOKE - 1.5TURNS		23642-908P
L6	PRINTED COIL		
L7	PRINTED COIL		
L8	IND CHOKE 4.7UH 10% LAQ		23642-553J
L9	IND CHOKE 4.7UH 10% LAQ		23642-553J
L10	IND CHOKE 4.7UH 10% LAQ		23642-553J
L11	IND CHOKE 4.7UH 10% LAQ		23642-553J
L12	IND CHOKE 4.7UH 10% LAQ		23642-553J
L13	ADJ. IND. 30NH 1 3/4 T		44290-799W

Circuit Ref	Description	Part Number
Unit AC13	- FILTER & FREQ DOUBLER BOARD (continued)	
L14	ADJ. IND. 30NH 1 3/4 T	44290-799W
L15	ADJ. IND. 43NH 2 1/4 T	44290-800J
L16	ADJ. IND. 43NH 2 1/4 T	44290-800J
L17	ADJ, IND. 61NH 2 3/4 T	44290-801F
L18	ADJ, IND. 61NH 2 3/4 T	44290-801F
L19	ADJ. IND. 86NH 3 3/4 T	44290-802G
L20	ADJ. IND. 86NH 3 3/4 T	44290-802G
L21	ADJ. IND. 121NH 4 3/4 T	44290-803V
L22	ADJ. IND. 121NH 4 3/4 T	44290-803V
L23	ADJ. IND. 172NH 6 3/4 T	44290-804S
L24	ADJ. IND. 172NH 6 3/4 T	44290-804S
L25	IND CHOKE 4.7UH 10% LAQ	23642-553J
L26	IND CHOKE 4.7UH 10% LAQ	23642-553J
L27	IND CHOKE 4.7UH 10% LAQ	23642-553J
L28	IND CHOKE 4.7UH 10% LAQ	23642-553J
L30	PRINTED COIL	
L31	PRINTED COIL	
L33	IND CHOKE 4.7UH 10% LAQ	23642-553J
L34	IND CHOKE 4.7UH 10% LAQ	23642-553J
L36	IND CHOKE 4.7UH 10% LAQ	23642-553J
L37	IND CHOKE 68UH 10% LAQ	23642-560S
L38	IND CHOKE 68UH 10% LAQ	23642-560S
L39	IND CHOKE 68UH 10% LAQ	23642-560S
L40	IND CHOKE 68UH 10% LAQ	23642-560S
L41	IND CHOKE 1.8UH 5%	23642-495X
L42	IND CHOKE 1.8UH 5%	23642-495X
L43	IND CHOKE 3.0UH 5%	23642-474H
L44	IND CHOKE 3.0UH 5%	23642-474H
L45	IND CHOKE 4.3UH 5%	23642-466R
L46	IND CHOKE 4.3UH 5%	23642-466R
L47	IND CHOKE 6.2UH 5%	23642-455S
L48	IND CHOKE 6.2UH 5%	23642-455S
L49	IND CHOKE 8.2UH 5%	23642-468K
L50	IND CHOKE 8.2UH 5%	23642-468K
L51	IND CHOKE 12UH 5%	23642-456W
L52	IND CHOKE 12UH 5%	23642-456W
L53	IND CHOKE 68UH 10% LAQ	23642-560S
L54	IND CHOKE 68UH 10% LAQ	23642-560S
L55	IND CHOKE 68UH 10% LAQ	23642-560S
L56	IND CHOKE 68UH 10% LAQ	23642-560S
L57	IND CHOKE 68UH 10% LAQ	23642-560S
L58	IND CHOKE 1.5UH 5%	23642-494P
L59	IND CHOKE 1.5UH 5%	23642-494P
L60	IND CHOKE 68UH 10% LAQ	23642-560S

Circuit Ref	Description	Part Number
Unit AC13	- FILTER & FREQ DOUBLER BOARD (Contd.)	
L61	IND CHOKE 68UH 10% LAQ	23642-560S
L62	IND CHOKE 68UH 10% LAQ	23642-560S
L63	IND CHOKE .82UH 5%	23642-454V
L64	IND CHOKE .82UH 5%	23642-454V
L65	IND CHOKE 68UH 10% LAQ	23642-560S
L66	IND CHOKE 68UH 10% LAQ	23642-560S
L67	PRINTED COIL	
L68	PRINTED COIL	
L69	PRINTED COIL	
L70	RES. LEAD LENGTH	
L72	PRINTED COIL	
L73	PRINTED COIL	
L74	COIL RF 10UH	44290-805W
L75	COIL RF 10UH	44290-805W
L76	COIL RF 10UH	44290-805W
L77	RES. LEAD LENGTH	
L79	PRINTED COIL	
L80	PRINTED COIL	
L83	PRINTED COIL	
L84	PRINTED COIL	
L90	IND CHOKE - 1.5TURNS	23642-908P
L91	RES. LEAD LENGTH	
L92	RES. LEAD LENGTH	
PLDF	CABLE COAX 12CM SMB-FEM/-	43129-537Y
R1	RES MF 360R 1/4W 2% 100PPM	24773-262T
R2	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R3	RES MF 470R 1/4W 2% 100PPM	24773-265M
R4	RES MF 3K0 1/4W 2% 100PPM	24773-284J
R5	RES MF 3K0 1/4W 2% 100PPM	24773-284J
R6	RES MF 75R 1/4W 2% 100PPM	24773-246Y
R7	RES MF 1K5 1/4W 2% 100PPM	24773-277U
R8	RES CC 150R 1/8W 5%	24331-990D
R9	RES CC 150R 1/8W 5%	24331-990D
R10	RES CHIP 16R 5%	24681-043E
R11	RES CHIP 16R 5%	24681-043E
R12	RES MF 51R 1/4W 2% 100PPM	24773-242Z
R13	RES MF 51R 1/4W 2% 100PPM	24773-242Z
R14	RES MF 6K8 1/4W 2% 100PPM	24773-293D
R15	RES MF 6K8 1/4W 2% 100PPM	24773-293D
R16	RES MF 200R 1/4W 2% 100PPM	24773-256S
R17	RES MF 820R 1/4W 2% 100PPM	24773-271B
R18	RES MF 75R 1/4W 2% 100PPM	24773-246Y

Circuit Ref	Description	Part Number
Unit AC13	- FILTER & FREQ DOUBLER BOARD (continued)	
R19	RES MF 2K4 1/4W 2% 100PPM	24773-282N
R20	RES MF 820R 1/4W 2% 100PPM	24773-271B
R21	RES MF 820R 1/4W 2% 100PPM	24773-271B
R22	RES MF 3K9 1/4W 2% 100PPM	24773-287V
R23	RES MF 360R 1/4W 2% 100PPM	24773-262T
R24	RES MF 470R 1/4W 2% 100PPM	24773-265M
R25	RES MF 5K6 1/4W 2% 100PPM	24773-291S
R26	RES MF 300R 1/4W 2% 100PPM	24773-260W
R27	RES MF 300R 1/4W 2% 100PPM	24773-260W
R28	RES MF 6K8 1/4W 2% 100PPM	24773-293D
R29	RES MF 270R 1/4W 2% 100PPM	24773-259T
R30	RES MF 240R 1/4W 2% 100PPM	24773-258D
R31	RES MF 10K 1/4W 2% 100PPM	24773-297M
R32	RES MF 240R 1/4W 2% 100PPM	24773-258D
R33	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R34	RES MF 470R 1/4W 2% 100PPM	24773-265M
R35	RES MF 1K5 1/4W 2% 100PPM	24773-277U
R36	RES MF 470R 1/4W 2% 100PPM	24773-265M
R37	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R38	RES MF 470R 1/4W 2% 100PPM	24773-265M
R39	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R40	RES MF 470R 1/4W 2% 100PPM	24773-265M
R41	RES MF 240R 1/4W 2% 100PPM	24773-258D
R42	RES MF 470R 1/4W 2% 100PPM	24773-265M
R43	RES MF 680R 1/4W 2% 100PPM	24773-269K
R44	RES MF 680R 1/4W 2% 100PPM	24773-269K
R45	RES MF 680R 1/4W 2% 100PPM	24773-269K
R46	RES MF 680R 1/4W 2% 100PPM	24773-269K
R47	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R48	RES MF 470R 1/4W 2% 100PPM	24773-265M
R50	RES MF 470R 1/4W 2% 100PPM	24773-265M
R51	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R52	RES MF 470R 1/4W 2% 100PPM	24773-265M
R53	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R54	RES MF 1K5 1/4W 2% 100PPM	24773-277U
R55	RES MF 470R 1/4W 2% 100PPM	24773-265M
R56	RES MF 470R 1/4W 2% 100PPM	24773-265M
R57	RES MF 470R 1/4W 2% 100PPM	24773-265M
R58	RES MF 10K 1/4W 2% 100PPM	24773-297M
R59	RES MF 10K 1/4W 2% 100PPM	24773-297M
R60	RES MF 10K 1/4W 2% 100PPM	24773-297M
R61	RES MF 10K 1/4W 2% 100PPM	24773-297M
R62	RES MF 2K7 1/4W 2% 100PPM	24773-283L
R63	RES MF 680R 1/4W 2% 100PPM	24773-269K

Circuit Ref	Description	Part Number
Unit AC13	- FILTER & FREQ DOUBLER BOARD (continued)	
R64	RES CHIP 51R 5%	24681-045Y
R65	RES CHIP 51R 5%	24681-045Y
R66	RES MF 18R 1/4W 2% 100PPM	24773-231P
R67	RES MF 470R 1/4W 2% 100PPM	24773-265M
R68	RES MF 1KO 1/4W 2% 100PPM	24773-273A
R69	RES CC 51R 1/8W 5%	24331-989P
R70	RES MF 3K9 1/4W 2% 100PPM	24773-287V
R71	RES MF 680R 1/4W 2% 100PPM	24773-269K
R72	RES CHIP 16R 5%	24681-043E
R73	RES CC 100R 1/8W 5%	24331-997B
R74	RES CHIP 10R 5%	24681-042H
R75	RES CC 100R 1/8W 5%	24331-997B
R76	RES MF 2K4 1/4W 2% 100PPM	24773-282N
R77	RES MF 2K4 1/4W 2% 100PPM	24773-282N
R78	RES MF 2K4 1/4W 2% 100PPM	24773-282N
R79	RES MF 2K4 1/4W 2% 100PPM	24773-282N
R80	RES MF 47K 1/4W 2% 100PPM	24773-313H
R81	RES MF 36R 1/4W 2% 100PPM	24773-238A
R82	RES MF 2K4 1/4W 2% 100PPM	24773-282N
R83	RES MF 2K4 1/4W 2% 100PPM	24773-282N
R84	RES CC 82R 1/8W 5%	24331-996R
R85	RES MF 3K9 1/4W 2% 100PPM	24773-287V
R86	RES MF 680R 1/4W 2% 100PPM	24773-269K
R87	RES CHIP 16R 5%	24681-043E
R88	RES CC 68R 1/8W 5%	24331-979F
R89	RES MF 240R 1/4W 2% 100PPM	24773-258D
R90	RES CC 150R 1/8W 5%	24331-990D
R91	RES MF 470R 1/4W 2% 100PPM	24773-265M
R92	RES MF 1KO 1/4W 2% 100PPM	24773-273A
R93	RES MF 470R 1/4W 2% 100PPM	24773-265M
R99	RES MF 3K9 1/4W 2% 100PPM	24773-287V
R100	RES MF 3K9 1/4W 2% 100PPM	24773-287V
R101	RES MF 3K9 1/4W 2% 100PPM	24773-287V
R102	RES MF 3K9 1/4W 2% 100PPM	24773-287V
R103	RES MF 3K9 1/4W 2% 100PPM	24773-287V
R104	RES MF 1KO 1/4W 2% 100PPM	24773-273A
R105	RES MF 470R 1/4W 2% 100PPM	24773-265M
R106	RES MF 3K9 1/4W 2% 100PPM	24773-287V
R107	RES MF 3K9 1/4W 2% 100PPM	24773-287V
R108	RES MF 470R 1/4W 2% 100PPM	24773-265M
R109	RES MF 470R 1/4W 2% 100PPM	24773-265M
R110	RES CHIP 10R 5%	24681-042H
R111	RES CC 100R 1/8W 5%	24331-997B

Circuit Ref	Description		Part Number
Unit AC13	- FILTER & FREQ DOUBLER BOARD (continued)		
SKCS	CON RF SMB MALE 50 PCB STR		23444-334Y
TR1	TR NSI BFR96S 15V 5G - AMP		28452-172N
TR2	TR NSI BFR96S 15V 5G - AMP		28452-172N
TR3	TR NSI 2N2369 15V 500M - SW		28452-197H
TR4	TR NSI BFR96S 15V 5G - AMP		28452-172N
TR5	TR NSI BFR90 15V 5G - AMP		28452-167U
TR6	TR NSI BFR91 12V 5G - AMP		28451-696U
X6	S/C ACC PAD TO18,ETC TO .1"GRD		28488-115L
Unit AD11	- DISPLAY BOARD AD11		
22. When ordering, prefix circuit reference with AD11			
	Complete unit		44828-773P
C1	CAP ELEC 4U7 35V 20% SUBMIN		26421-108A
C2	CAP ELEC 10U 35V 20% SUBMIN		26421-112Z
C3	CAP PETP 22N 250V 10% RAD		26582-204X
C4	CAP ELEC 10U 35V 20% SUBMIN		26421-112Z
C5	CAP ELEC 10U 35V 20% SUBMIN		26421-112Z
D1	DI ZEN BZX79C12 12V 5%		28372-149G
IC1	ICD BUFF 7407 HEX O/C		28469-703X
IC2	ICD BUFF 7407 HEX O/C		28469-703X
IC3	ICD DRIV 4054 LCD	!	28469-398Z
IC4	ICD DECOD 4056 BCD-7SEG LCD	!	28469-401B
IC5	ICD DECOD 4056 BCD-7SEG LCD	!	28469-401B
IC6	ICD DECOD 4056 BCD-7SEG LCD	!	28469-401B
IC7	ICD DECOD 4056 BCD-7SEG LCD	!	28469-401B
IC8	ICD DECOD 4056 BCD-7SEG LCD	!	28469-401B
IC9	ICD DECOD 4056 BCD-7SEG LCD	!	28469-401B
IC10	ICD DECOD 4056 BCD-7SEG LCD	!	28469-401B
IC11	ICD DECOD 4056 BCD-7SEG LCD	!	28469-401B
IC12	ICD DRIV 4054 LCD	!	28469-398Z
IC13	ICD NOR 74LS02 QUAD 2INP		28466-214Y
IC14	ICD DRIV 4054 LCD	!	28469-398Z
IC15	ICD DECOD 4028 BCD-DEC BI	!	28465-013B
IC16	ICD DECOD 4028 BCD-DEC BI	!	28465-013B
IC17	ICD DECOD 4028 BCD-DEC BI	!	28465-013B
IC18	ICD DRIV 4054 LCD	!	28469-398Z
IC19	ICD MONO 4047 AST MULTI BI	!	28468-307C
IC20	ICD DRIV 4054 LCD	!	28469-398Z

Circuit Ref	Description		Part Number
Unit AD11	- DISPLAY BOARD AD11 (continued)		
IC21	ICD DECOD 4056 BCD-7SEG LCD	!	28469-401B
IC22	ICD DECOD 4056 BCD-7SEG LCD	!	28469-401B
IC23	ICD DECOD 4056 BCD-7SEG LCD	!	28469-401B
IC24	ICD DRIV 4054 LCD	!	28469-398Z
IC25	ICD DEC/DMX 4555 DUAL 2-4	!	28465-017H
IC26	ICD DRIV 4054 LCD	!	28469-398Z
IC27	ICD DRIV 4054 LCD	!	28469-398Z
IC28	ICD DRIV 4054 LCD	!	28469-398Z
IC29	ICD DECOD 4056 BCD-7SEG LCD	!	28469-401B
IC30	ICD DECOD 4056 BCD-7SEG LCD	!	28469-401B
IC31	ICD DECOD 4056 BCD-7SEG LCD	!	28469-401B
IC32	ICD DRIV 4054 LCD	!	28469-398Z
IC33	ICD DRIV 4054 LCD	!	28469-398Z
IC34	ICD DRIV 4054 LCD	!	28469-398Z
L1	IND CHOKE 4.7UH 10% LAQ		23642-553J
L2	IND CHOKE 4.7UH 10% LAQ		23642-553J
R1	RES NET 6K8 5% 15DIL		24681-514C
R2	RES MF 220K 1/4W 2% 100PPM		24773-329T
X1	LCD 4575-363-060		44990-361M
X2	LCD 4811-363-360		44990-420G
X3	LCD 4577-363-060		44990-363R

Unit AD2 - MOTHER BOARD AD2

23. When ordering, prefix circuit reference with AD2

	Complete unit	44828-442A
C1	CAP CER 10N 100V 20%+ DISC	26383-055L
C2	CAP CER 10N 100V 20%+ DISC	26383-055L
D1	DI HOT CARR BAT29 5V	28349-014L
IC1	ICD FF D 74LS273 OCT +EDG TR	28462-615U
IC2	ICD BUFF 7406 HEX O/C INV 30V	28469-158A
IC3	ICD DRIV 74128 QUAD 2NOR 500HM	28466-224S
SKAH	CON EDGE D/SIDED 13 WAY 0.15"	23435-714T

Circuit Ref	Description	Part Number
Unit AD3/1	- AF OSC & MOD CONTROL	
24. When ordering, prefix circuit reference with AD3/1		
	Complete unit	44828-772T
C1	CAP PS 10NO 63V 1% RAD	26538-926Y
C2	CAP PETP 1UO 50V 10% RAD MIN	26582-432F
C3	CAP ELEC 10U 35V 20% SUBMIN	26421-112Z
C4	CAP ELEC 10U 35V 20% SUBMIN	26421-112Z
C5	CAP CER 150P 63V 2% PLATE	26343-479W
C6	CAP PS 10NO 63V 1% RAD	26538-926Y
C7	CAP PETP 1UO 50V 10% RAD MIN	26582-432F
C8	CAP PETP 470N 63V 10% RAD MIN	26582-427L
C9	CAP PS 3N6 63V 1% RAD	26538-915R
C10	CAP CER 470P 63V 10% PLATE	26383-582T
C11	CAP CER 33P 63V 5% PLATE	26343-471Y
C12	CAP CER 33P 63V 5% PLATE	26343-471Y
C13	CAP CER 4P7 63V .5PF PLATE	26343-461B
C14	CAP CER 10N 25V 20% DISC	26383-006C
C15	CAP CER 10P 63V .5PF PLATE	26343-465H
C16	CAP CER 10N 25V 20% DISC	26383-006C
C17	CAP CER 4P7 63V .5PF PLATE	26343-461B
C18	CAP ELEC 10U 35V 20% SUBMIN	26421-112Z
C19	CAP ELEC 10U 35V 20% SUBMIN	26421-112Z
C20	CAP ELEC 10U 35V 20% SUBMIN	26421-112Z
C21	CAP PETP 470N 63V 10% RAD MIN	26582-427L
C22	CAP CER 10N 25V 20% DISC	26383-006C
C23	CAP CER 10N 25V 20% DISC	26383-006C
C24	CAP CER 10N 100V 20%+ DISC	26383-055L
C25	CAP ELEC 10U 35V 20% SUBMIN	26421-112Z
C26	CAP ELEC 10U 35V 20% SUBMIN	26421-112Z
C27	CAP ELEC 10U 35V 20% SUBMIN	26421-112Z
C28	CAP CER 10N 25V 20% DISC	26383-006C
C29	CAP CER 10N 25V 20% DISC	26383-006C
C30	CAP CER 10N 25V 20% DISC	26383-006C
C31	CAP CER 10N 25V 20% DISC	26383-006C
C32	CAP ELEC 10U 35V 20% SUBMIN	26421-112Z
C33	CAP CER 10N 25V 20% DISC	26383-006C
C34	CAP CER 10N 25V 20% DISC	26383-006C
C35	CAP CER 10N 25V 20% DISC	26383-006C
C36	CAP CER 10N 25V 20% DISC	26383-006C
C37	CAP CER 10N 25V 20% DISC	26383-006C
C38	CAP PETP 150N 100V 10% RAD	26582-212K
C39	CAP PETP 1UO 50V 10% RAD MIN	26582-432F
C40	CAP CER 2P7 63V .5PF PLATE	26343-458B

Circuit Ref	Description		Part Number
Unit AD3/1	- AF OSC & MOD CONTROL (continued)		
C41	CAP CER 2P7 63V .5PF PLATE		26343-458B
D1	DI SIL 1N4148 75V JUNC		28336-676J
D2	DI SIL 1N4148 75V JUNC		28336-676J
D3	DI SIL 1N4148 75V JUNC		28336-676J
D4	DI SIL 1N4148 75V JUNC		28336-676J
D5	DI SIL 1N4148 75V JUNC		28336-676J
D6	DI SIL 1N4148 75V JUNC		28336-676J
D7	DI SIL 1N4148 75V JUNC		28336-676J
D8	DI ZEN BZX79C7V5 7.5V 5%		28371-602Z
IC1	ICA MUX 4053 TRIP 2INP	!	28469-714H
IC2	ICA MUX 4053 TRIP 2INP	!	28469-714H
IC3	ICA MUX 4053 TRIP 2INP	!	28469-714H
IC4	ICA MUX 4052 DUAL 4INP	!	28469-713Z
IC5	ICD FF D 74LS273 OCT +EDG TR		28462-615U
IC6	ICA AMP TL074CN QUAD FET I/P		28461-349H
IC7	ICA AMP LM348N QUAD GP DIL14		28461-321E
IC8	ICA COMP LM311N DIL8		28461-695U
IC9	ICA COMP LM311N DIL8		28461-695U
IC10	ICD MONO 74LS123 DUAL RETR		28468-309B
IC11	ICA MUX 4053 TRIP 2INP	!	28469-714H
IC12	ICA MUX 4053 TRIP 2INP	!	28469-714H
IC13	ICA MUX 4053 TRIP 2INP	!	28469-714H
IC14	ICA AMP TL072CP DUAL FET I/P		28461-348Z
IC15	ICA DAC AD7524JN 8BIT	!	28469-400R
IC16	ICD FF D 74LS273 OCT +EDG TR		28462-615U
IC17	ICA AMP TL071CP FET I/P DIL8		28461-347A
IC18	ICA DAC AD7524JN 8BIT	!	28469-400R
IC19	ICA AMP TL071CP FET I/P DIL8		28461-347A
IC20	ICA DAC AD7524JN 8BIT	!	28469-400R
IC21	ICA AMP TL071CP FET I/P DIL8		28461-347A
IC22	ICA MUX 4052 DUAL 4INP	!	28469-713Z
IC23	ICD DEC/DMX 74LS138 3-8		28465-027F
IC24	ICA AMP TL071CP FET I/P DIL8		28461-347A
IC25	ICD INV 74LS04 HEX		28469-171L
IC26	ICA DAC AD7522LN 10BIT MOS	!	28469-402K
IC27	ICA AMP TL071CP FET I/P DIL8		28461-347A
IC28	ICA DAC AD7524JN 8BIT	!	28469-400R
IC29	ICA AMP TL071CP FET I/P DIL8		28461-347A
IC30	ICA AMP NE5534AH H-PRF DIL 8		28461-358J
IC31	ICA AMP NE5532 DUAL LN DIL8		28461-363G

Circuit Ref	Description	Part Number
Unit AD3/1	- AF OSC & MOD CONTROL (continued)	
PLDX	CON PCB MALE 36 FXD RT ANGLE	23435-120L
PLDY	CON PCB MALE 36 FXD RT ANGLE	23435-120L
R1	RES MF 10K 1/4W 2% 100PPM	24773-297M
R2	RES MF 10K 1/4W 2% 100PPM	24773-297M
R3	RES MF 10K 1/4W 2% 100PPM	24773-297M
R4	RES MF 10K 1/4W 2% 100PPM	24773-297M
R5	RES MF 10K 1/4W 2% 100PPM	24773-297M
R6	RES MF 2K56 1/4W 0.5% 25PPM	24753-564F
R7	RES MF 2K56 1/4W 0.5% 25PPM	24753-564F
R8	RES MF 5K05 1/4W 0.5% 50PPM	24753-667G
R9	RES MF 5K05 1/4W 0.5% 50PPM	24753-667G
R10	RES MF 15K83 1/4W 0.5% 25PPM	24753-560Y
R11	RES MF 31K6 1/4W 0.5% 50PPM	24753-498W
R12	RES MF 39K7 1/4W 0.5% 25PPM	24753-561N
R13	RES MF 53K0 1/4W 0.5% 25PPM	24753-562L
R14	RES MF 15K83 1/4W 0.5% 25PPM	24753-560Y
R15	RES MF 31K6 1/4W 0.5% 50PPM	24753-498W
R16	RES MF 39K7 1/4W 0.5% 25PPM	24753-561N
R17	RES MF 53K0 1/4W 0.5% 25PPM	24753-562L
R18	RES MF 10K 1/4W 2% 100PPM	24773-297M
R19	RES MF 10K 1/4W 2% 100PPM	24773-297M
R20	RES MF 10K 1/4W 2% 100PPM	24773-297M
R21	RES MF 22K 1/4W 2% 100PPM	24773-305R
R22	RES MF 12K 1/4W 2% 100PPM	24773-299R
R23	RV CERM 2K LIN .3W 10% FLAT	25748-505T
R24	RES MF 56R 1/4W 2% 100PPM	24773-243H
R25	RES MF 1K3 1/4W 2% 100PPM	24773-276E
R26	RES MF 3K3 1/4W 2% 100PPM	24773-285F
R27	RES MF 22K 1/4W 2% 100PPM	24773-305R
R28	RES MF 3K3 1/4W 2% 100PPM	24773-285F
R29	RES MF 22K 1/4W 2% 100PPM	24773-305R
R30	RES MF 100K 1/4W 2% 100PPM	24773-321L
R31	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R32	RV CERM 500R LIN .3W 10% FLAT	25748-503W
R33	RES MF 2K0 1/4W 2% 100PPM	24773-280U
R34	RES MF 390R 1/4W 2% 100PPM	24773-263P
R35	RES MF 620R 1/4W 2% 100PPM	24773-268B
R36	RES MF 12K 1/4W 2% 100PPM	24773-299R
R37	RV CERM 500R LIN .3W 10% FLAT	25748-503W
R38	RES MF 2K7 1/4W 2% 100PPM	24773-283L
R39	RES MF 330K 1/4W 2% 100PPM	24773-333P
R40	RES MF 330K 1/4W 2% 100PPM	24773-333P

Circuit Ref	Description	Part Number
Unit AD3/1	- AF OSC & MOD CONTROL (continued)	
R41	RES MF 100R 1/4W 2% 100PPM	24773-249J
R42	RES MF 1M0 1/4W 2% 100PPM	24773-346E
R43	RES MF 1M0 1/4W 2% 100PPM	24773-346E
R44	RES MF 5K6 1/4W 2% 100PPM	24773-291S
R45	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R46	RES MF 390R 1/4W 2% 100PPM	24773-263P
R47	RES MF 620R 1/4W 2% 100PPM	24773-268B
R48	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R49	RES MF 33R 1/4W 2% 100PPM	24773-237K
R50	RES MF 1M0 1/4W 2% 100PPM	24773-346E
R51	RES MF 1M0 1/4W 2% 100PPM	24773-346E
R52	RES MF 100K 1/4W 2% 100PPM	24773-321L
R53	RES MF 12K 1/4W 2% 100PPM	24773-299R
R54	RES MF 3K0 1/4W 2% 100PPM	24773-284J
R55	RES MF 330K 1/4W 2% 100PPM	24773-333P
R56	RES MF 330K 1/4W 2% 100PPM	24773-333P
R57	RES MF 1K2 1/4W 2% 100PPM	24773-275H
R58	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R59	RES MF 6K8 1/4W 2% 100PPM	24773-293D
R60	RV CERM 1K LIN .3W 10% FLAT	25748-504D
R61	RES MF 4K3 1/4W 2% 100PPM	24773-288S
R62	RES MF 240R 1/4W 2% 100PPM	24773-258D
R63	RES MF 6K8 1/4W 2% 100PPM	24773-293D
R64	RV CERM 500R LIN .3W 10% FLAT	25748-503W
R65	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R66	RES MF 10K 1/4W 2% 100PPM	24773-297M
R68	RES MF 10K 1/4W 2% 100PPM	24773-297M
R69	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R70	RV CERM 1K LIN .3W 10% FLAT	25748-504D
R71	RES MF 3K9 1/4W 2% 100PPM	24773-287V
R72	RES MF 28K7 1/4W 0.5% 50PPM	24753-671V
R73	RES MF 620R 1/4W 2% 100PPM	24773-268B
R74	RES MF 12K 1/4W 2% 100PPM	24773-299R
R75	RV CERM 500R LIN .3W 10% FLAT	25748-503W
R76	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R77	RES NET 10K 5% 8DIL	24681-511P
R78	RES MF 12K 1/4W 0.5% 50PPM	24753-629L
R79	RES MF 3K0 1/4W 0.5% 50PPM	24753-475C
R80	RES MF 750R 1/4W 0.5% 50PPM	24753-609P
R81	RES MF 250R 1/4W 0.25% 50PPM	24723-389N
R82	RES MF 10K 1/4W 2% 100PPM	24773-297M
R83	RES MF 10K 1/4W 2% 100PPM	24773-297M

Circuit Ref	Description	Part Number
Unit AD3/1	- AF OSC & MOD CONTROL (continued)	
R84	RES MF 10K 1/4W 2% 100PPM	24773-297M
R85	RES MF 10K 1/4W 2% 100PPM	24773-297M
R86	RES MF 240R 1/4W 2% 100PPM	24773-258D
R87	RES MF 10K 1/4W 2% 100PPM	24773-297M
R88	RES MF 390R 1/4W 2% 100PPM	24773-263P
R89	RES MF 240R 1/4W 2% 100PPM	24773-258D
R90	RES MF 39K 1/4W 2% 100PPM	24773-311A
R91	RES MF 10K 1/4W 2% 100PPM	24773-297M
R92	RES MF 2KO 1/4W 2% 100PPM	24773-280U
R93	RES MF 1KO 1/4W 2% 100PPM	24773-273A
TR1	TR NJF J310 25V - 24MA	28459-028E
TR2	TR NJF J310 25V - 24MA	28459-028E
	S/C ACC SKT DIL 16 LOW PROFILE	28488-041E
	S/C ACC SKT DIL 28 LOW PROFILE	28488-045L
Unit AD4/1	- KEYBOARD AD4/1	

25. When ordering, prefix circuit reference with AD4/1

	Complete unit	44828-795F
C1	CAP CER 10N 40V 20%+ PLATE	26387-253M
C2	CAP CER 10N 40V 20%+ PLATE	26387-253M
C3	CAP CER 10N 40V 20%+ PLATE	26387-253M
C4	CAP CER 10N 40V 20%+ PLATE	26387-253M
C5	CAP CER 10N 40V 20%+ PLATE	26387-253M
D1	LAMP LED HLMP1401 2.4V YEL	28624-137D
D2	LAMP LED HLMP1401 2.4V YEL	28624-137D
D3	LAMP LED HLMP1401 2.4V YEL	28624-137D
D4	LAMP LED HLMP1401 2.4V YEL	28624-137D
D5	LAMP LED HLMP1401 2.4V YEL	28624-137D
D6	LAMP LED HLMP1401 2.4V YEL	28624-137D
D7	LAMP LED HLMP1401 2.4V YEL	28624-137D
D8	LAMP LED HLMP1401 2.4V YEL	28624-137D
D9	LAMP LED HLMP1401 2.4V YEL	28624-137D
D10	LAMP LED HLMP1401 2.4V YEL	28624-137D
D11	LAMP LED HLMP1401 2.4V YEL	28624-137D
D12	LAMP LED HLMP1401 2.4V YEL	28624-137D
D13	LAMP LED HLMP1401 2.4V YEL	28624-137D
D14	LAMP LED HLMP1401 2.4V YEL	28624-137D
D15	LAMP LED HLMP1401 2.4V YEL	28624-137D
D16	LAMP LED HLMP1401 2.4V YEL	28624-137D
D17	LAMP LED HLMP1401 2.4V YEL	28624-137D
D18	LAMP LED HLMP1401 2.4V YEL	28624-137D
D19	LAMP LED HLMP1401 2.4V YEL	28624-137D

Circuit Ref	Description	Part Number
Unit AD4/1	- KEYBOARD AD4/1 (continued)	
IC1	ICD DEC/DMX 74LS138 3-8	28465-027F
IC2	ICD FF D 74LS273 OCT +EDG TR	28462-615U
IC3	ICD DEC/DMX 74LS138 3-8	28465-027F
IC4	ICD FF D 74LS273 OCT +EDG TR	28462-615U
IC5	ICD FF D 74LS273 OCT +EDG TR	28462-615U
IC6	ICD BUFF 74LS244 OCT 3ST	28469-182T
IC7	ICD NAND 74LS03 QUAD 2INP O/C	28466-346E
PLAM	CON ASSY PLAM-SKAD	43129-640E
PLDZ	CON PCB MALE 36 FXD RT ANGLE	23435-120L
R1	RES MF 330R 1/4W 2% 100PPM	24773-261D
R2	RES MF 100R 1/4W 2% 100PPM	24773-249J
R3	RES MF 100R 1/4W 2% 100PPM	24773-249J
R4	RES MF 100R 1/4W 2% 100PPM	24773-249J
R5	RES MF 330R 1/4W 2% 100PPM	24773-261D
R6	RES MF 100R 1/4W 2% 100PPM	24773-249J
R7	RES NET 10K 5% 8DIL	24681-511P
SA	SW PUSH 1CO 24V 10MA	23465-411B
SB	SW PUSH 1CO 24V 10MA	23465-411B
SC	SW PUSH 1CO 24V 10MA	23465-411B
SD	SW PUSH 1CO 24V 10MA	23465-411B
SE	SW PUSH 1CO 24V 10MA	23465-411B
SF	SW PUSH 1CO 24V 10MA	23465-411B
SG	SW PUSH 1CO 24V 10MA	23465-411B
SH	SW PUSH 1CO 24V 10MA	23465-411B
SJ	SW PUSH 1CO 24V 10MA	23465-411B
SK	SW PUSH 1CO 24V 10MA	23465-411B
SL	SW PUSH 1CO 24V 10MA	23465-411B
SM	SW PUSH 1CO 24V 10MA	23465-411B
SN	SW PUSH 1CO 24V 10MA	23465-411B
SP	SW PUSH 1CO 24V 10MA	23465-411B
SR	SW PUSH 1CO 24V 10MA	23465-411B
SS	SW PUSH 1CO 24V 10MA	23465-411B
ST	SW PUSH 1CO 24V 10MA	23465-411B
SU	SW PUSH 1CO 24V 10MA	23465-411B
SV	SW PUSH 1CO 24V 10MA	23465-411B
SW	SW PUSH 1CO 24V 10MA	23465-411B
SX	SW PUSH 1CO 24V 10MA	23465-411B
SY	SW PUSH 1CO 24V 10MA	23465-411B
SZ	SW PUSH 1CO 24V 10MA	23465-411B
SAA	SW PUSH 1CO 24V 10MA	23465-411B
SAB	SW PUSH 1CO 24V 10MA	23465-411B

Circuit Ref	Description	Part Number
Unit AD4/1	- KEYBOARD AD4/1 (continued)	
SAC	SW PUSH 1CO 24V 10MA	23465-411B
SAD	SW PUSH 1CO 24V 10MA	23465-411B
SAE	SW PUSH 1CO 24V 10MA	23465-411B
SAF	SW PUSH 1CO 24V 10MA	23465-411B
SAG	SW PUSH 1CO 24V 10MA	23465-411B
SAH	SW PUSH 1CO 24V 10MA	23465-411B
SAJ	SW PUSH 1CO 24V 10MA	23465-411B
SAK	SW PUSH 1CO 24V 10MA	23465-411B
SAL	SW PUSH 1CO 24V 10MA	23465-411B
SAM	SW PUSH 1CO 24V 10MA	23465-411B
SAN	SW PUSH 1CO 24V 10MA	23465-411B
	SPACER (LED)	37590-737R
X40	CON ASSY	43129-640E
Unit AE1	- POWER SUPPLY BOARD	
26. When ordering, prefix circuit reference with AE1		
	Complete unit	44828-446U
C1	CAP ELEC 15000U 16V 10%+ PCB	26422-320S
C2	CAP ELEC 22U 25V 20%+ AX	26415-805K
C3	CAP ELEC 22U 25V 20%+ AX	26415-805K
C4	CAP ELEC 22U 25V 20%+ AX	26415-805K
C5	CAP ELEC 22U 25V 20%+ AX	26415-805K
C6	CAP ELEC 4700U 40V 10%+ PCB	26422-321W
C7	CAP ELEC 2200U 40V 20%+ AX	26415-831P
C8	CAP ELEC 22U 25V 20%+ AX	26415-805K
C9	CAP ELEC 4U7 63V 20%+ AX	26415-801M
C10	CAP ELEC 220U 63V 20%+ AX	26415-820J
C11	CAP ELEC 22U 25V 20%+ AX	26415-805K
C12	CAP ELEC 4U7 63V 20%+ AX	26415-801M
D1	DI BRIDGE 2KBB20R 200V 1.9A	28359-189D
D2	DI BRIDGE 2KBB20R 200V 1.9A	28359-189D
D3	DI BRIDGE 2KBB20R 200V 1.9A	28359-189D
D4	DI RECT 1N4004 400V	28357-028K
D5	DI RECT 1N4004 400V	28357-028K
D6	DI RECT 1N4004 400V	28357-028K
D7	DI RECT 1N4004 400V	28357-028K
D8	DI RECT 1N4004 400V	28357-028K
IC1	ICA VREG- LM337T PROG 1A5	28461-727Z
IC2	ICA VREG+ LM317T PROG 1A5	28461-726A

Circuit Ref	Description	Part Number
Unit AE1	- POWER SUPPLY BOARD (continued)	
R1	RES MF 220R 1/4W 2% 100PPM	24773-257W
R2	RV CERM 50R LIN .5W 10% HORZ	25711-634N
R3	RES MF 680R 1/4W 2% 100PPM	24773-269K
R4	RES MF 220R 1/4W 2% 100PPM	24773-257W
R5	RV CERM 50R LIN .5W 10% HORZ	25711-634N
R6	RES MF 2K7 1/4W 2% 100PPM	24773-283L
R7	RES MF 220R 1/4W 2% 100PPM	24773-257W
R8	RV CERM 50R LIN .5W 10% HORZ	25711-634N
R9	RES MF 2K7 1/4W 2% 100PPM	24773-283L
R10	RES MF 220R 1/4W 2% 100PPM	24773-257W
R11	RV CERM 50R LIN .5W 10% HORZ	25711-634N
R12	RES MF 4K3 1/4W 2% 100PPM	24773-288S
X2	S/C ACC BUSH TO3 0.176"LG INSU	28488-116J
X3	S/C ACC WASHER TO220 IN 1.3K/W	28488-136K
Unit AM0/1	- BASIC MODULE (44990-488D)	

27. When ordering, prefix circuit reference with AM0/1

D1	DI BRIDGE BY261 200V 12A		28359-191W
FS1	FUSE T/LAG 0.50A 20X5 MM	} 210V-240V	23411-056X
FS2	FUSE T/LAG 0.50A 20X5 MM		
FS1	FUSE T/LAG 1.0A 20X5 MM	} 105V-120V	23411-058C
FS2	FUSE T/LAG 1.0A 20X5 MM		
IC1	ICA VREG+ LM350K PROG 3A TO3		28461-722C
IC2	ICA VREG+ LM317K PROG 1A5 TO3		28461-728H
PLA	CON PWR MALE 3 FXD RF FILTER		23423-150L
PLAU	CABLE COAX 89CM SMB-FEM/SMB-FM		43129-655T
PLAV	CABLE COAX 0.3M SMC-FEMX2		43129-656P
PLAY	CON ASSY PLAY-PLAZ		43130-064W
PLBA	CABLE COAX 58CM N-FEM/SMA-MALE		43129-658M
SAP	SW TOG 2CO LEVER MAINS		23462-249Z
SAR	SW SLIDE 2CO PANEL MTG		23467-161W
SAS	SW SLIDE 2CO PANEL MTG		23467-161W
SKB	CABLE WIR 21CM 3 MIN-1ROW-4P/-		43129-694C
SKC	CABLE WIR 26CM 9 1ROW-10P/-		43129-695R
SKE	CABLE WIR 19CM 4 MIN-1ROW-5PX2		43129-643N
SKH	CON ASSY SKH-SKW		43129-645J
SKV	CON ASSY SKV-SKAE		43129-649S

Circuit Ref	Description	Part Number
Unit AM0/1	- BASIC MODULE (continued)	
SKY	CABLE WIR .5M 16 FM-DIL/IDC-FM	43129-691P
SKAB	CABLE RIB 13CM 16 IDC-FM-DILX2	43129-653W
SKAN	CON RF BNC FEM 50 BKHD	23443-442B
SKAP	CABLE COAX 52CM BNC-FEM/SMB-FM	43129-654D
SKDX	CON ASSY SKDX-SKDZ	43130-088J
SKDY	CON ASSY SKDY	43130-087L
SKEC	CON RF BNC FEM 50 BKHD	23443-442B
SKED	CON RF BNC FEM 50 BKHD	23443-442B
T1	TFMR PWR TOROIDAL	43490-089W
X1	H/W FUSE HOLDER PANEL 20X5	23416-192R
X2	H/W COVER FOR FUSE HOLDER	23416-198E
X3	COVER MAINS FILTER	37590-150P
X6	COVER SWITCH	37590-245S
X8	S/C ACC WASHER TO3 INS 0.3K/W	28488-135D
X9	S/C ACC COVER TO3 INSULATING	28488-201X
Unit AT0/1	- 10dB STEP ATTENUATOR ASSY	
28. When ordering, prefix circuit reference with AT0/1		
	Complete unit	44990-478L

Circuit Ref	Description	Part Number
Unit AT2	- ATTENUATOR CONTROL	
29. When ordering, prefix circuit reference with AT2		
	Complete unit	44828-966J
C1	CAP CER 47P 63V 5% PLATE	26343-473L
C2	CAP ELEC 4U7 35V 20% SUBMIN	26421-108A
C3	CAP CER 10P 63V .5PF PLATE	26343-465H
C4	CAP CER 10N 100V 20%+ DISC	26383-055L
C5	CAP TANT 4U7 35V 20% SUBMIN	26486-219P
C6	CAP TANT 4U7 35V 20% SUBMIN	26486-219P
C7	CAP ELEC 470U 16V 20%+ PCB	26421-127W
C8	CAP CER 100P 63V 5% PLATE	26343-477V
D1	DI SIL 1N4148 75V JUNC	28336-676J
D2	DI SIL 1N4148 75V JUNC	28336-676J
D3	DI ZEN BZX79C10 10V 5%	28371-844U
D4	DI SIL 1N4148 75V JUNC	28336-676J
D5	DI SIL 1N4148 75V JUNC	28336-676J
D6	DI SIL 1N4148 75V JUNC	28336-676J
D7	DI SIL 1N4148 75V JUNC	28336-676J
D8	DI SIL 1N4148 75V JUNC	28336-676J
D9	DI SIL 1N4148 75V JUNC	28336-676J
D10	LAMP LED HLMP 1401 2.4V YELLOW	28624-137D
D11	DI RECT 1N4004 400V	28357-028K
IC1	ICA AMP CA3130E GP MOS DIL8 !	28461-361J
IC2	ICA COMP LM311N DIL8	28461-695U
IC3	ICD NOR 74LS02 QUAD 2INP	28466-214Y
IC4	ICD MONO 74LS123 DUAL RETR	28468-309B
IC5	ICD BUFF 7407 HEX O/C	28469-703X
IC6	ICD BUFF 7407 HEX O/C	28469-703X
R1	RES MF 100K 1/4W 2% 100PPM	24773-321L
R2	RES MF 47K 1/4W 2% 100PPM	24773-313H
R3	RES MF 100K 1/4W 2% 100PPM	24773-321L
R4	RES MF 10K 1/4W 2% 100PPM	24773-297M
R5	RES MF 10K 1/4W 2% 100PPM	24773-297M
R6	RES MF 24K 1/4W 2% 100PPM	24773-306B
R7	RES MF 1K3 1/4W 2% 100PPM	24773-276E
R8	RES MF 3K9 1/4W 2% 100PPM	24773-287V
R9	RES MF 10K 1/4W 2% 100PPM	24773-297M
R10	RES MF 10K 1/4W 2% 100PPM	24773-297M
R11	RES MF 510R 1/4W 2% 100PPM	24773-266C
R12	RES MF 47K 1/4W 2% 100PPM	24773-313H
R13	RES MF 10K 1/4W 2% 100PPM	24773-297M
R14	RES MF 24K 1/4W 2% 100PPM	24773-306B
R15	RES MF 3K9 1/4W 2% 100PPM	24773-287V

Circuit Ref	Description	Part Number
Unit AT2	- ATTENUATOR CONTROL (continued)	
R16	RES MF 200R 1/4W 2% 100PPM	24773-256S
R17	RES MF 10K 1/4W 2% 100PPM	24773-297M
R18	RES MF 10K 1/4W 2% 100PPM	24773-297M
R19	RES MF 10R 1/4W 2% 100PPM	24773-225W
R20	RES NET 15KO 5% 9 SIP	24681-603F
TR1	TR PSI BC308B 20V 130M - GEN	28433-455R
TR2	TR NSI BFY51 30V 50M - GEN	28455-827T
TR3	TR PSI 2N2905 40V 200M - GEN	28434-879X
X3	S/C ACC PAD TO5,ETC TO 0.1 "GRD	28488-113Y
Unit AG1/1	- GPIB ADAPTER TRANSCEIVER -	

30. When ordering, prefix circuit reference with AG1/1

Note ...

The GPIB adapter module (AG0), is normally complete with box, mountings and transceiver p.c.b. and supplied as an Optional Accessory Part Number 54433-001U.

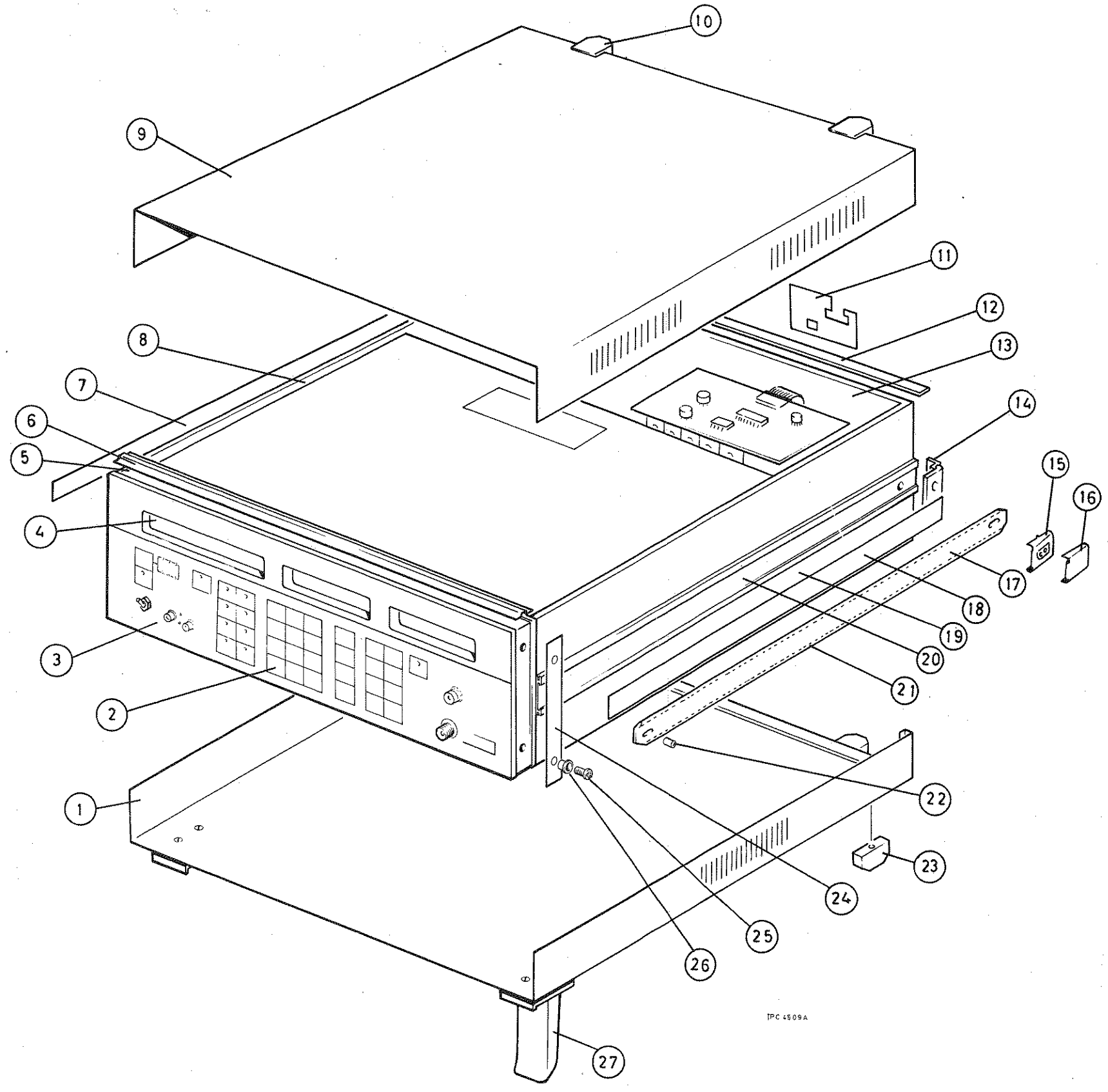
	Transceiver board complete	44828-794J
C1	CAP CER 68PF 63V 5% PLATE	26343-475F
C2	CAP CER 0.01UF 100V 20% DISC	26383-055L
C4	CAP CER 0.01UF 100V 20% DISC	26383-055L
C5	CAP CER 0.01UF 100V 20% DISC	26383-055L
C6	CAP CER 0.01UF 100V 20% DISC	26383-055L
C7	CAP CER 0.01UF 100V 20% DISC	26383-055L
C8	CAP CER 0.01UF 100V 20% DISC	26383-055L
C9	CAP CER 0.01UF 100V 20% DISC	26383-055L
C10	CAP CER 0.01UF 100V 20% DISC	26383-055L
C11	CAP CER 0.01UF 100V 20% DISC	26383-055L
IC1	ICD MONO 74LS123 DUAL RETRIG	28468-309B
IC2	ICD MP SUPP 8291A/7210 GPIB TALK/LIST !	28467-027N
IC3	ICD INV 74LS04 HEX	28469-171L
IC4	ICD TRANSC MC3448 QUAD 3ST GPIB	28469-190R
IC5	ICD TRANSC MC3448 QUAD 3ST GPIB	28469-190R
IC6	ICD TRANSC MC3448 QUAD 3ST GPIB	28469-190R
IC7	ICD TRANSC MC3448 QUAD 3ST GPIB	28469-190R
IC8	ICD NAND 74LS00 QUAD 2 INP	28466-345H
IC9	ICD NAND 74LS20 DUAL 4 INP	28466-347U
IC10	ICD D F/F 74LS374 OCT + EDG TR	28462-618L
PLAK	HEADER MALE	23435-976F
R1	RES MF 10K 1/4W 2%	24773-297M
R2	RES MF 10K 1/4W 2%	24773-297M
SKAJ	VERTICAL MOUNT 24-WAY	23435-979S

31. Order without prefix.

Fig. 1

item	Description	Part no.
1	Bottom outer cover	35903-279B
2	Front panel switch caps, marked:-	
	STORE	37590-745H
	RECALL	37590-746E
	AF OSC	37590-854N
	MOD ALC	37590-372Y
	INCREMENT	37590-373N
	CARRIER FREQ	37590-374L
	FM	37590-375J
	AM	37590-376F
	RF LEVEL	37590-377G
	7	37590-334H
	4	37590-311K
	1	37590-328K
	0	37590-325C
	8	37590-335E
	5	37590-332A
	2	37590-329A
	.	37590-326R
	9	37590-336U
	6	37590-333Z
	3	37590-330B
	-	37590-327B
	MHz/V	37590-390X
	kHz/mV	37590-391M
	Hz/μV	37590-392C
	RAD/%/dB	37590-747U
	INT/EXT	37590-394B
	TOTAL Δ	37590-395K
	UP	37590-396A
	ΦM	37590-743A
	RETURN	37590-398H
	DOWN	37590-399E
	SECOND FUNCT	37590-400B
	AF LEVEL	37590-744Z
	MOD ON OFF	37590-749N
	AF ON OFF	37590-748Y
	CARRIER ON OFF	37590-750U
3	Front panel assy. (2018A)	35904-389W
	Front panel assy. (2019A)	35903-887D
4	Carrier frequency bezel	37590-408N
	Modulation and r.f level bezel	37590-409L
5	Front trim panel	34900-477G
6	Front trim infill	35902-371Z

Fig. 1 item	Description	Part no.
7	Left-hand side trim infill	35902-384V
8	Left-hand side frame assy.	35903-314M
9	Top outer cover	35904-504X
10	Back foot	37590-514L
	Stud	37590-223C
11	Selector plate	35902-441Z
12	Rear trim	34900-470E
13	Rear panel assy.	35904-515H
14	End cap plate	37590-255C
	End cap cover	37590-256R
15	Liner	22315-584T
16	Cover moulding	37590-257B
17	Steel liner	22315-587M
18	Right-hand side trim infill	35902-386W
19	Side rail assy.	34900-723V
20	Right-hand side frame assy.	35903-315C
21	PVC extrusion	22315-590M
22	Bush	35900-785V
23	Rear lower foot	37590-224R
	Stud	37590-223C
24	Side trim infill (handle)	35902-368Z
25	Screw	21857-465C
26	Screw cup washer	21171-550W
27	Front foot	37590-253X
	Tilt stand	37590-254M



Miscellaneous mechanical parts

Chapter 7

SERVICING DIAGRAMS

CONTENTS

CIRCUIT NOTES

Component values

1. Resistors : Code letter R = ohms, k = kilohms (10^3), M = megohms (10^6).

Capacitors : Code letter m = millifarads (10^{-3}), μ = microfarads (10^{-6}), n = nanofarads (10^{-9}), p = picofarads (10^{-12}).

Inductors : Code letter H = henrys, m = millihenrys (10^{-3}), μ = microhenrys (10^{-6}), n = nanohenrys (10^{-9}).

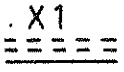
SIC : Value selected during test, nominal value shown.

2. Components are marked normally with two, three or four figures according to the accuracy limit ±10%, ±1% or ±0.1%. The code letter used indicates the multiplier and replaces the decimal point. Because a marking 4m7 could be interpreted as milliohms, millifarads or millihenrys all values are placed near to its related symbol.

Symbols

3. Symbols are based on the provisions of BS 3939 with the following additions:


edge connector



ferrite bead


warning, see page (iv), Notes and Cautions

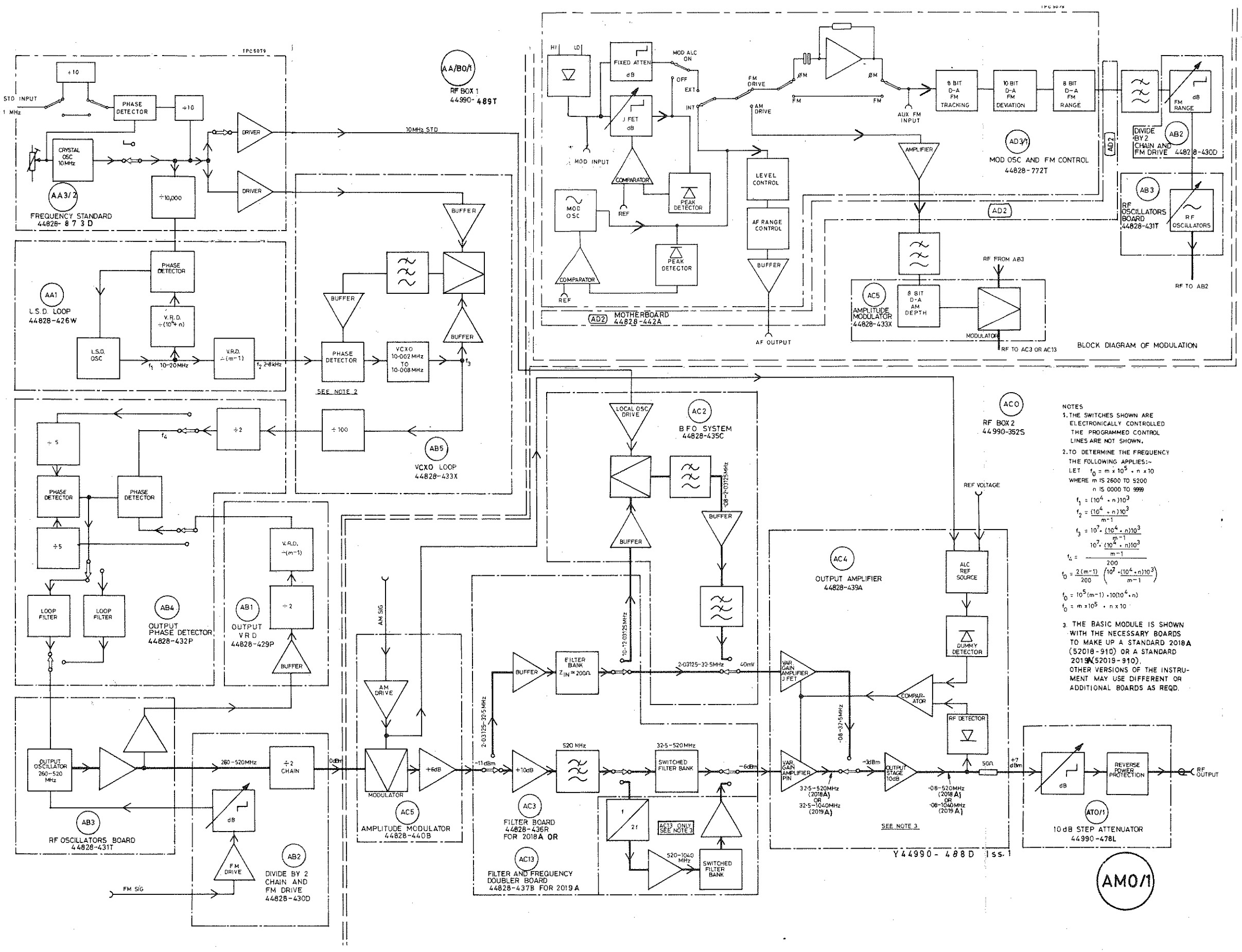

Beryllia : health hazard, see page (iv), Notes and Cautions

unit identification number

P printed component

Unit identification suffixes

4. References to unit identification designators such as AA2, AD3, etc., apply equally to AA2/1, AD3/1 etc., unless otherwise stated.



2018A/2019A Frequency synthesis and signal processing, simplified block diagram

Fig. 1

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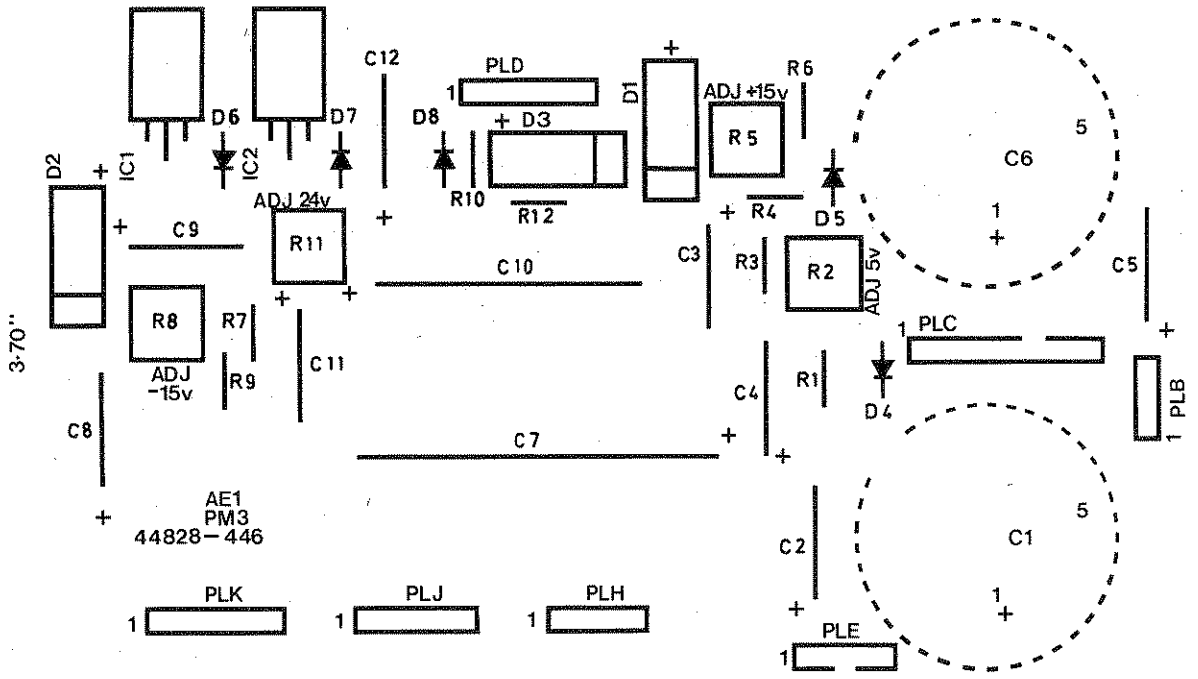

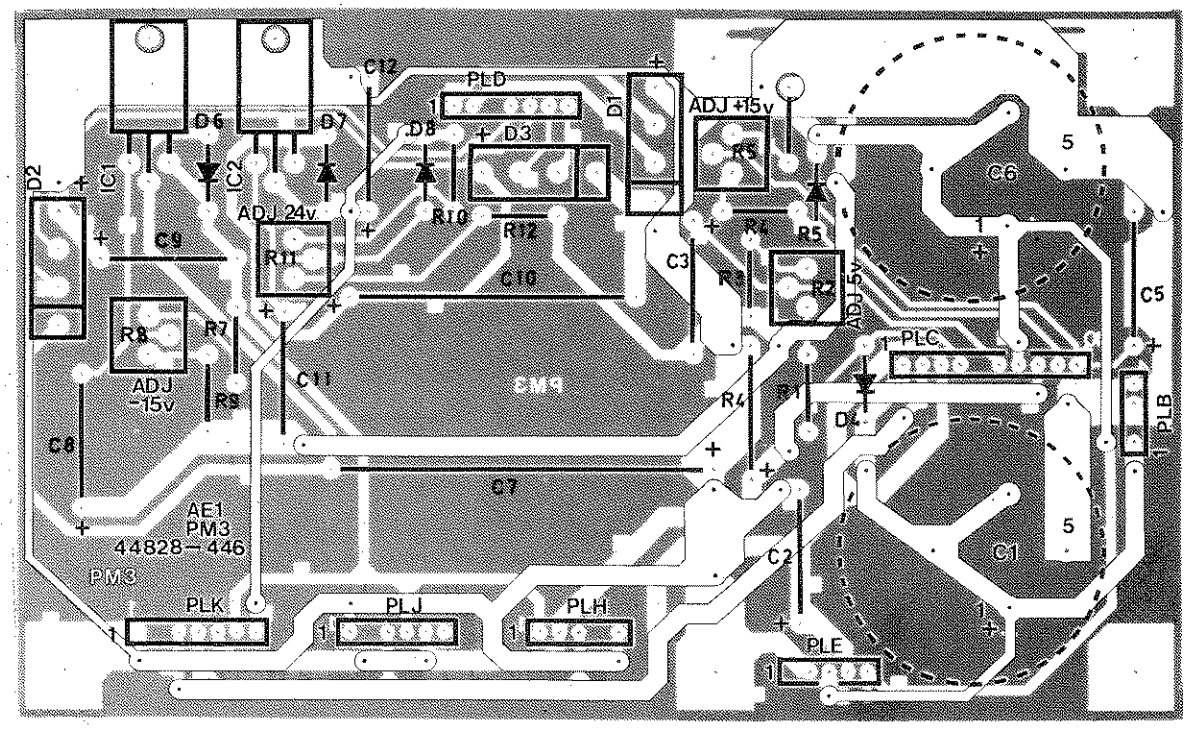

Component layout, AE1

Fig. 2a
Chap. 7
Page 4

Fig. 2a

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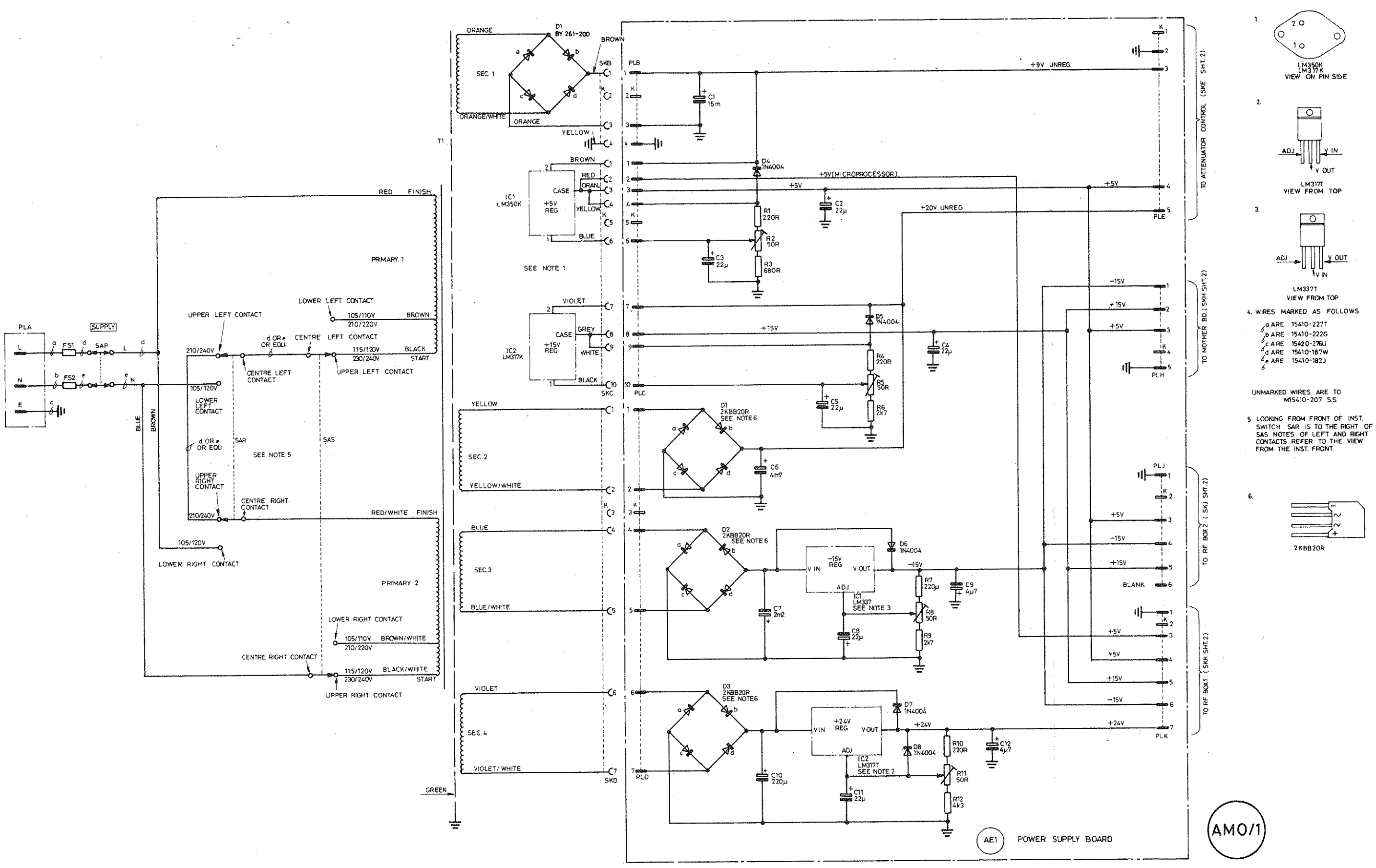


1.

LM350K
LM317K
VIEW ON PIN SIDE

2.

LM317T
VIEW FROM TOP

3.

LM337T
VIEW FROM TOP

4. WIRES MARKED AS FOLLOWS

a ARE 15410-227T
b ARE 15410-222G
c ARE 15420-276U
d ARE 15410-187W
e ARE 15410-182J

UNMARKED WIRES ARE TO M15410-207 S.S.

5 LOOKING FROM FRONT OF INST. SWITCH SAR IS TO THE RIGHT OF SAS NOTES OF LEFT AND RIGHT CONTACTS REFER TO THE VIEW FROM THE INST. FRONT

6.

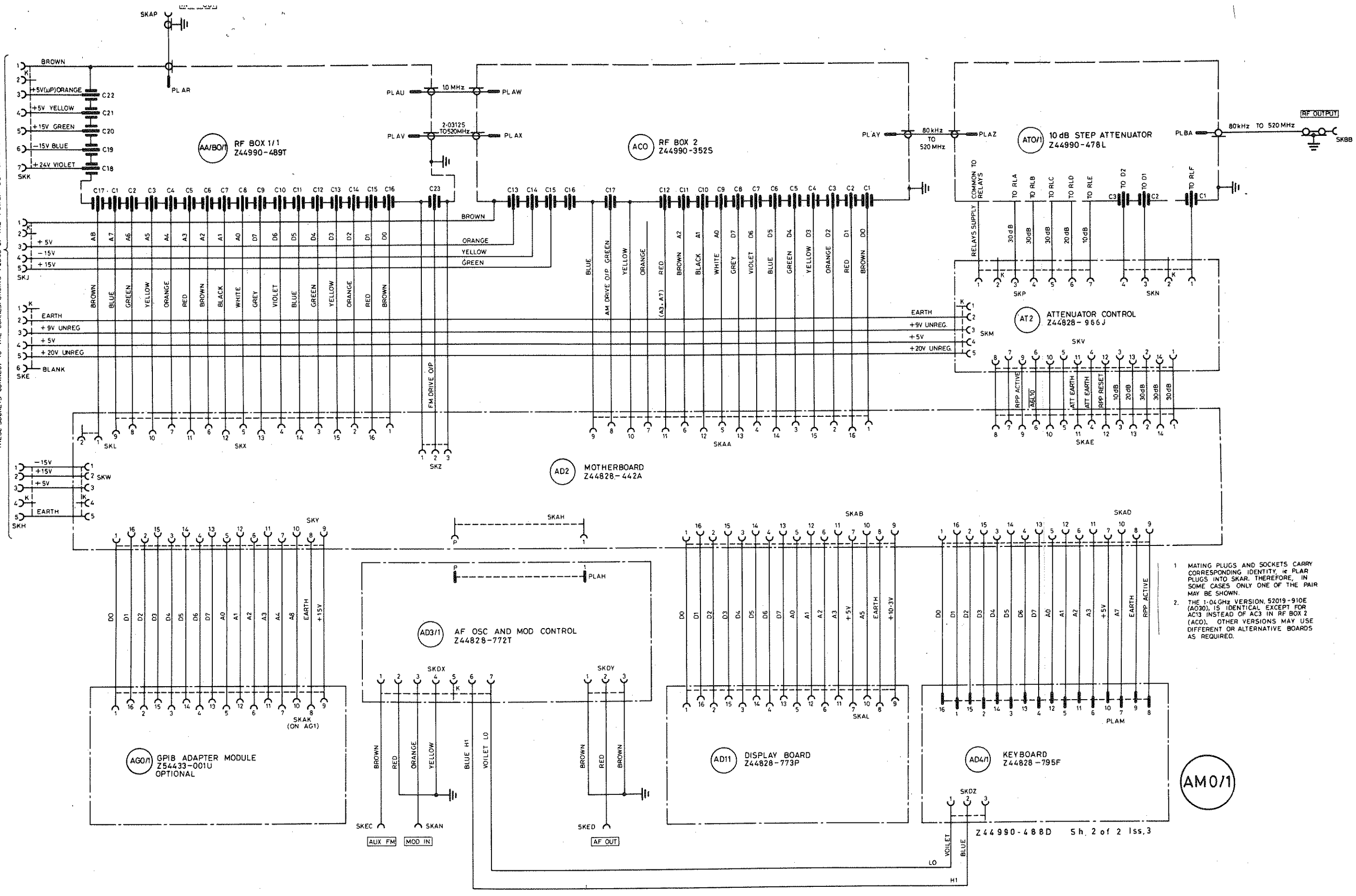
2KBB20R

Z 44990-488D Iss. 2

Power supplies, AM0/1 (includes board AE1)

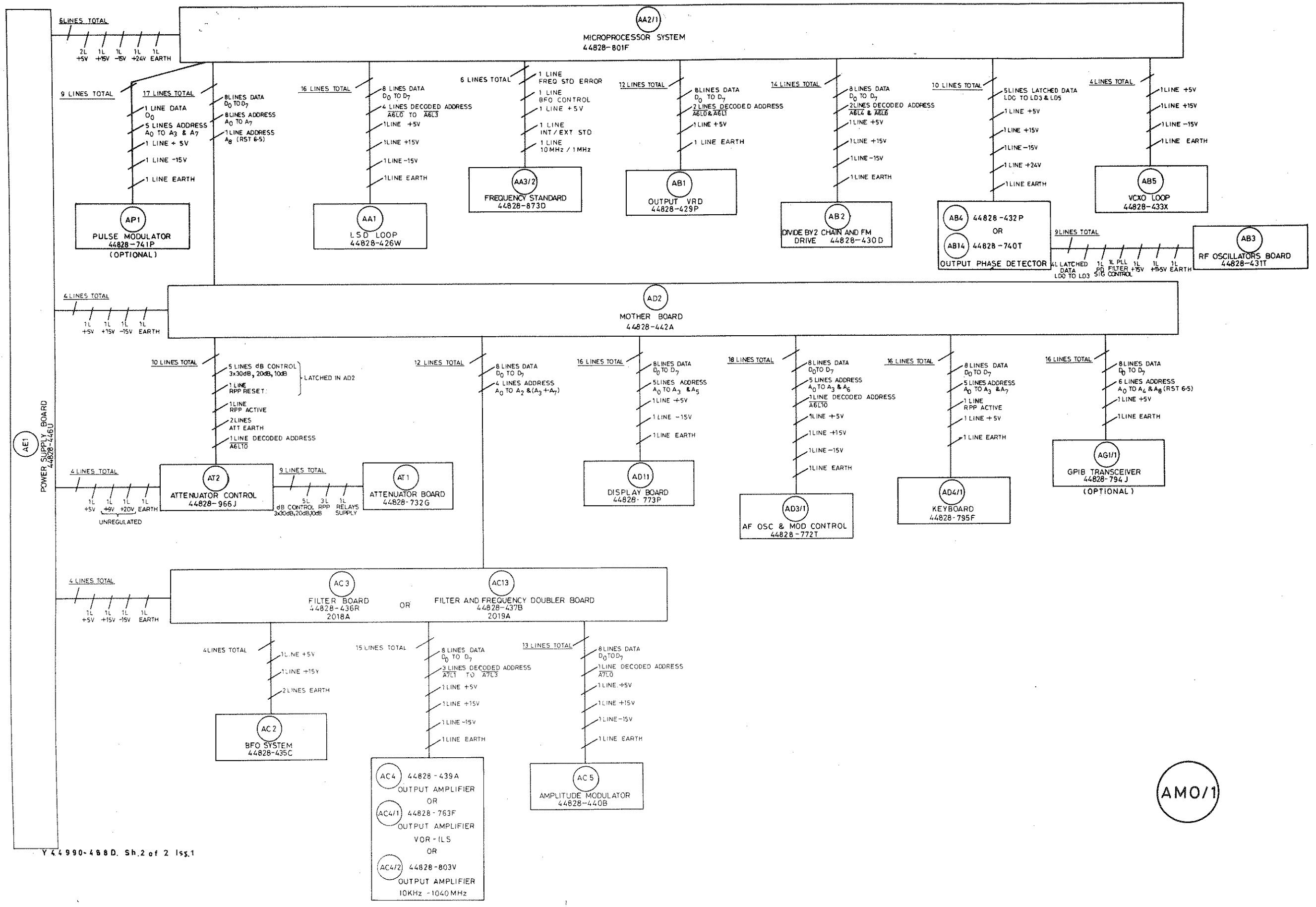
Fig. 2 .

Mar. 88 (Am. 3)



1. MATING PLUGS AND SOCKETS CARRY CORRESPONDING IDENTITY, ie PLAR PLUGS INTO SKAR. THEREFORE, IN SOME CASES ONLY ONE OF THE PAIR MAY BE SHOWN.
2. THE 1·04GHz VERSION, 52019-910E (A030), IS IDENTICAL EXCEPT FOR AC13 INSTEAD OF AC3 IN RF BOX 2 (AC0). OTHER VERSIONS MAY USE DIFFERENT OR ALTERNATIVE BOARDS AS REQUIRED.

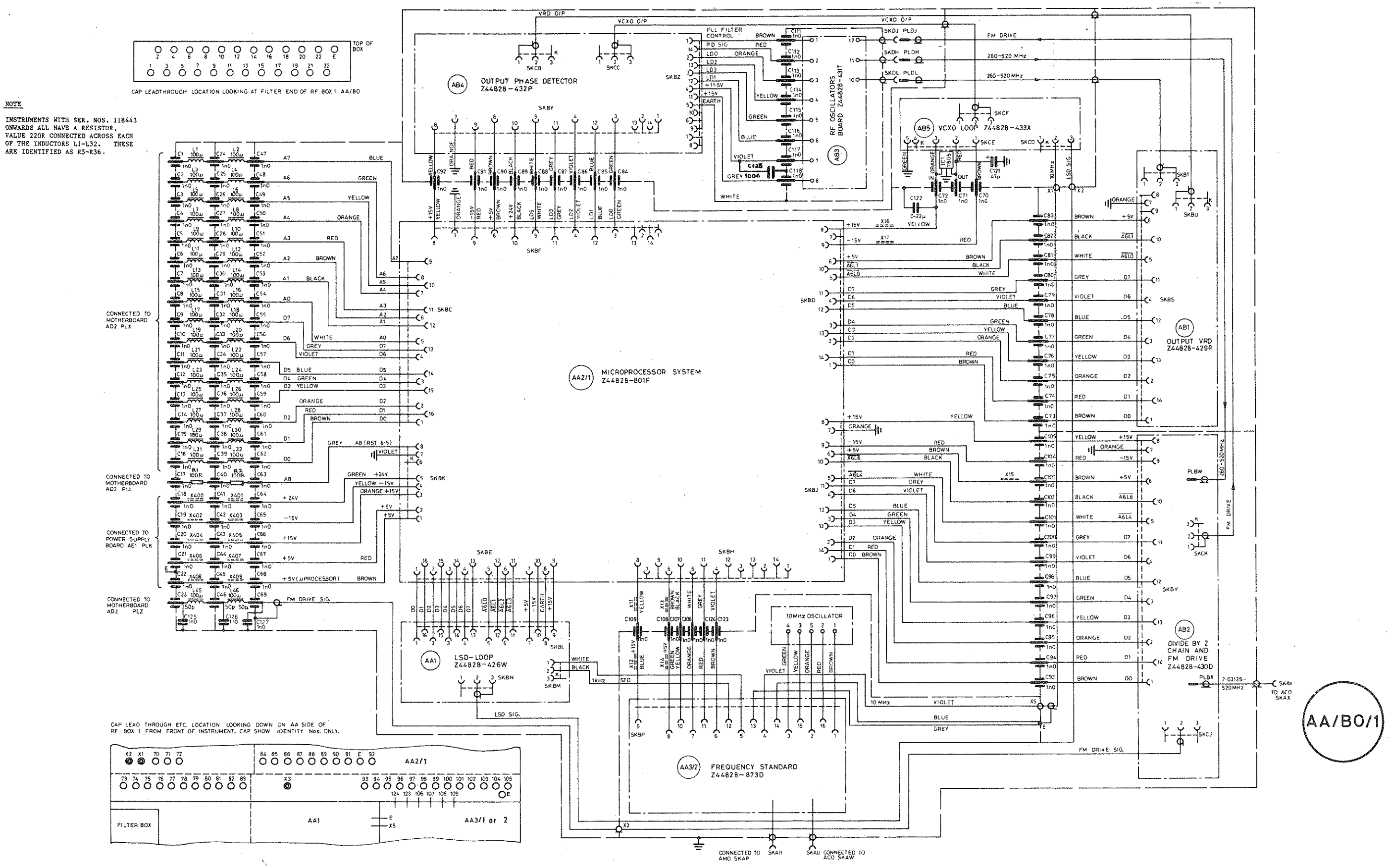
Basic module interconnections, AM0/1



Control and power supply lines, AMO/1

Fig. 4

Jun. 84

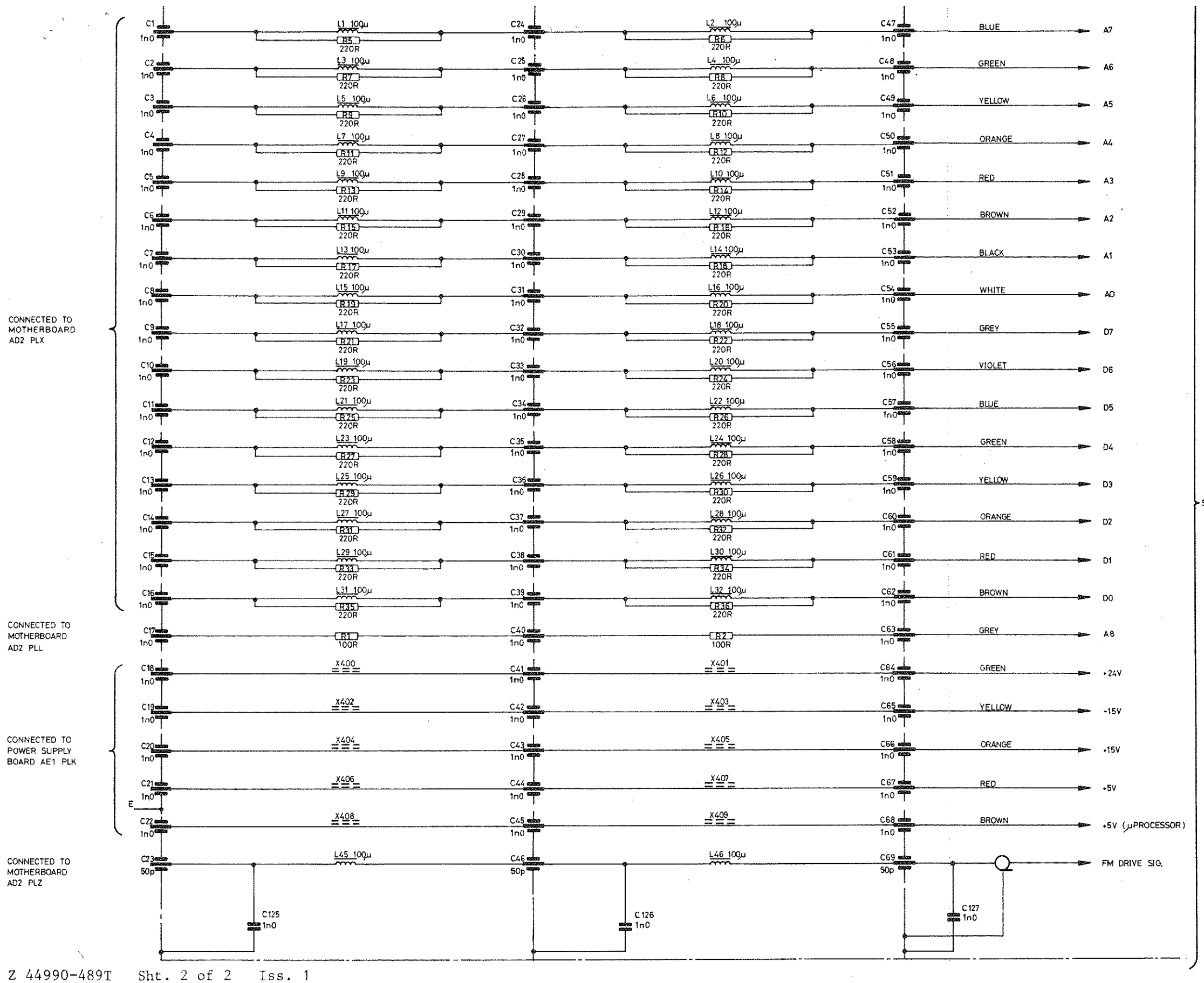


Z 44990-489T Sht. 1 of 2, Iss. 7

Fig. 5

RF box 1 interconnections, AA/BO/1

Mar. 88 (Am. 3)



Z 44990-489T Sht. 2 of 2 Iss. 1

RF Box 1 AA/B0/1

AA/B0/1

Fig. 6
Mar. 88 (Am. 3)

Fig. 6
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Page 13

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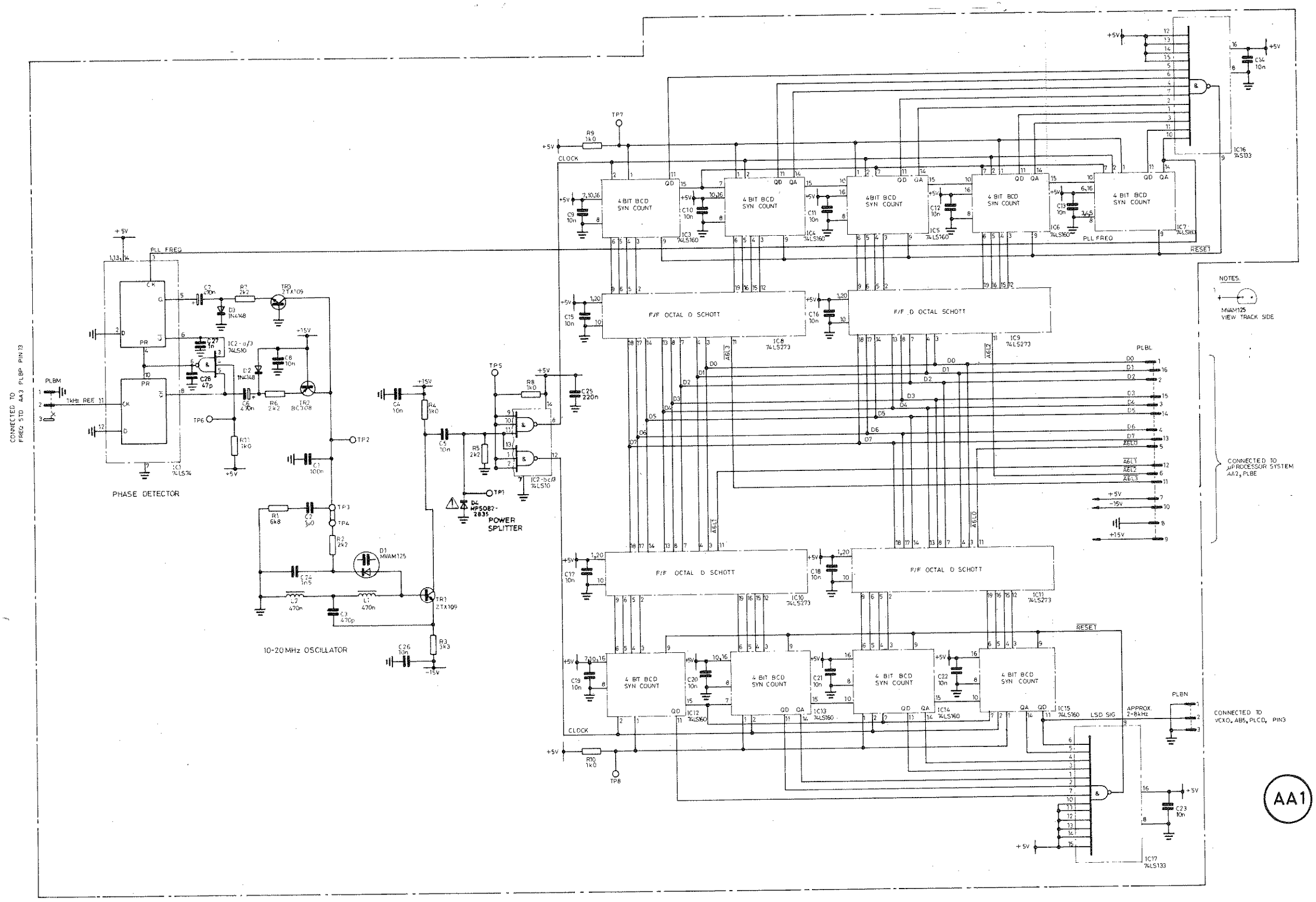
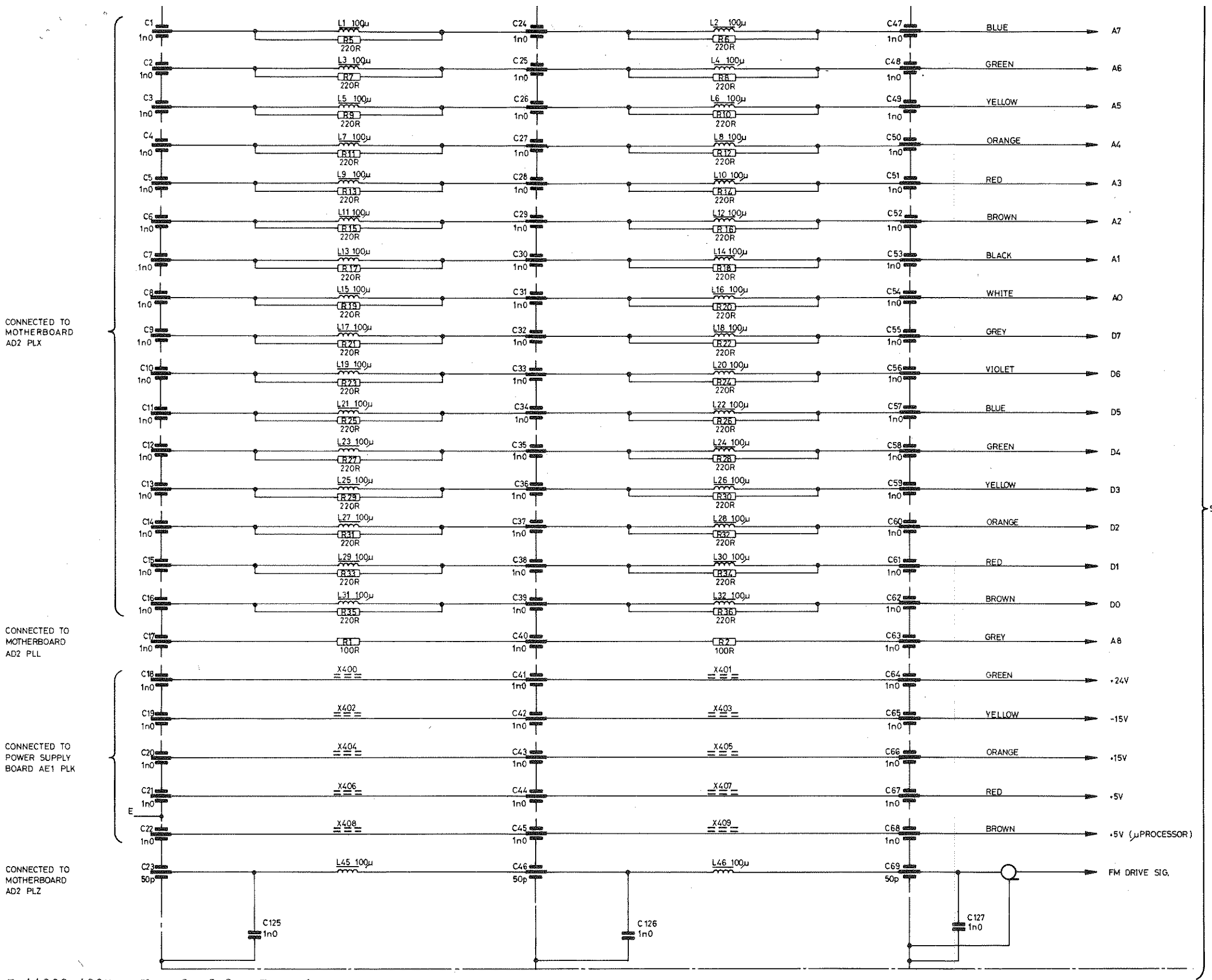


44828-426W Iss. 10

LSD loop, AA1

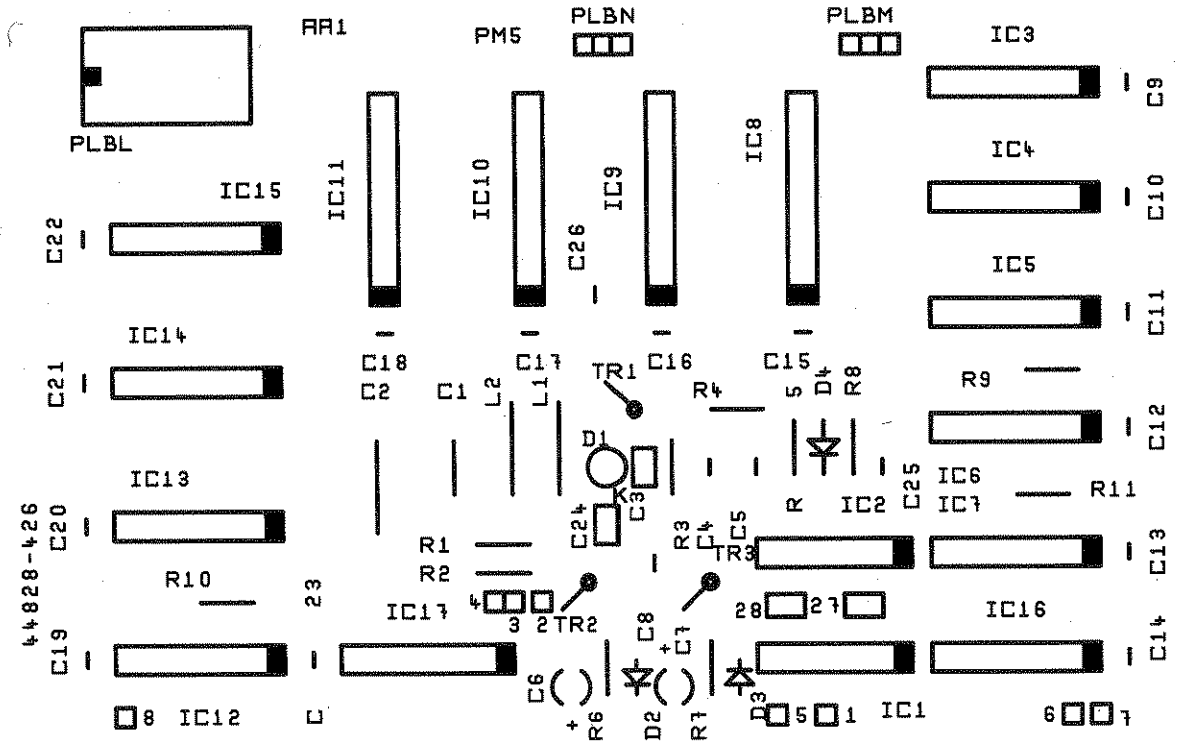
Fig. 7

Mar. 88 (Am. 3)



Z 44990-489T Sht. 2 of 2 Iss. 1

RF Box 1 AA/B0/1



Component layout, AA1

Fig. 7a
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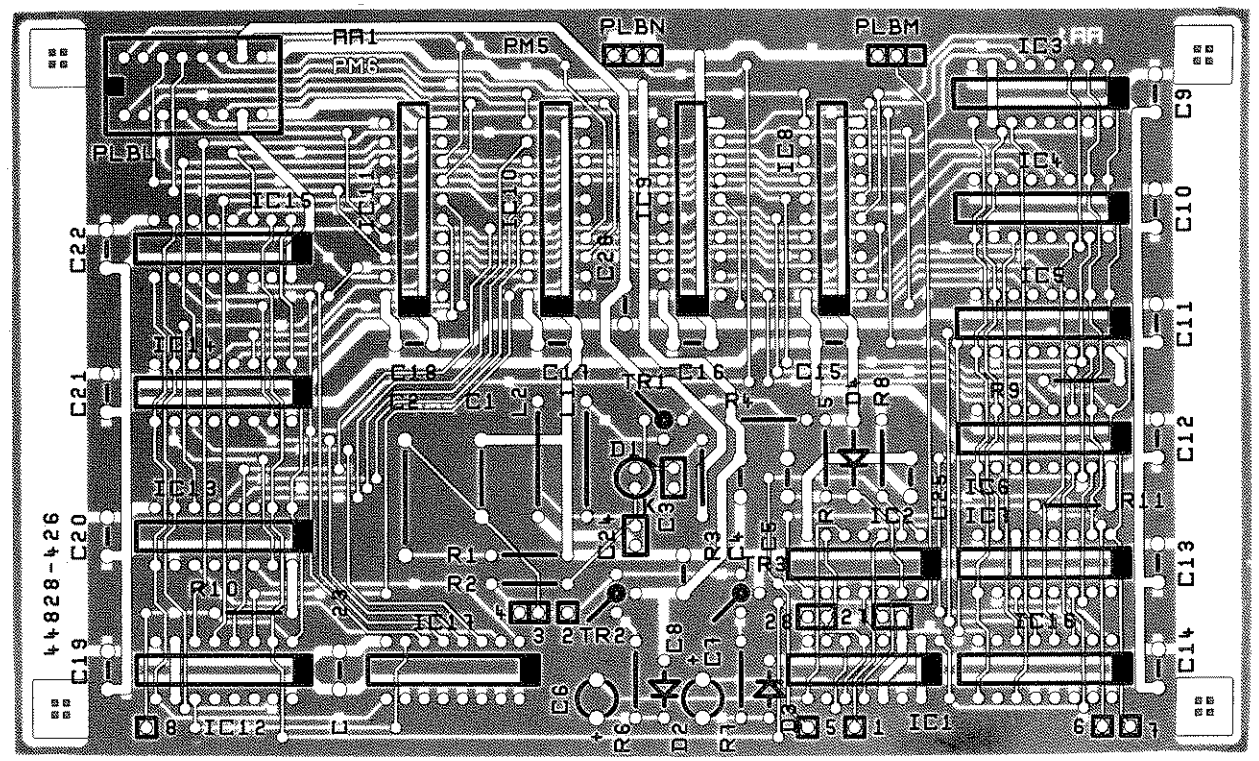

Fig. 7a

Mar. 88 (Am. 3)

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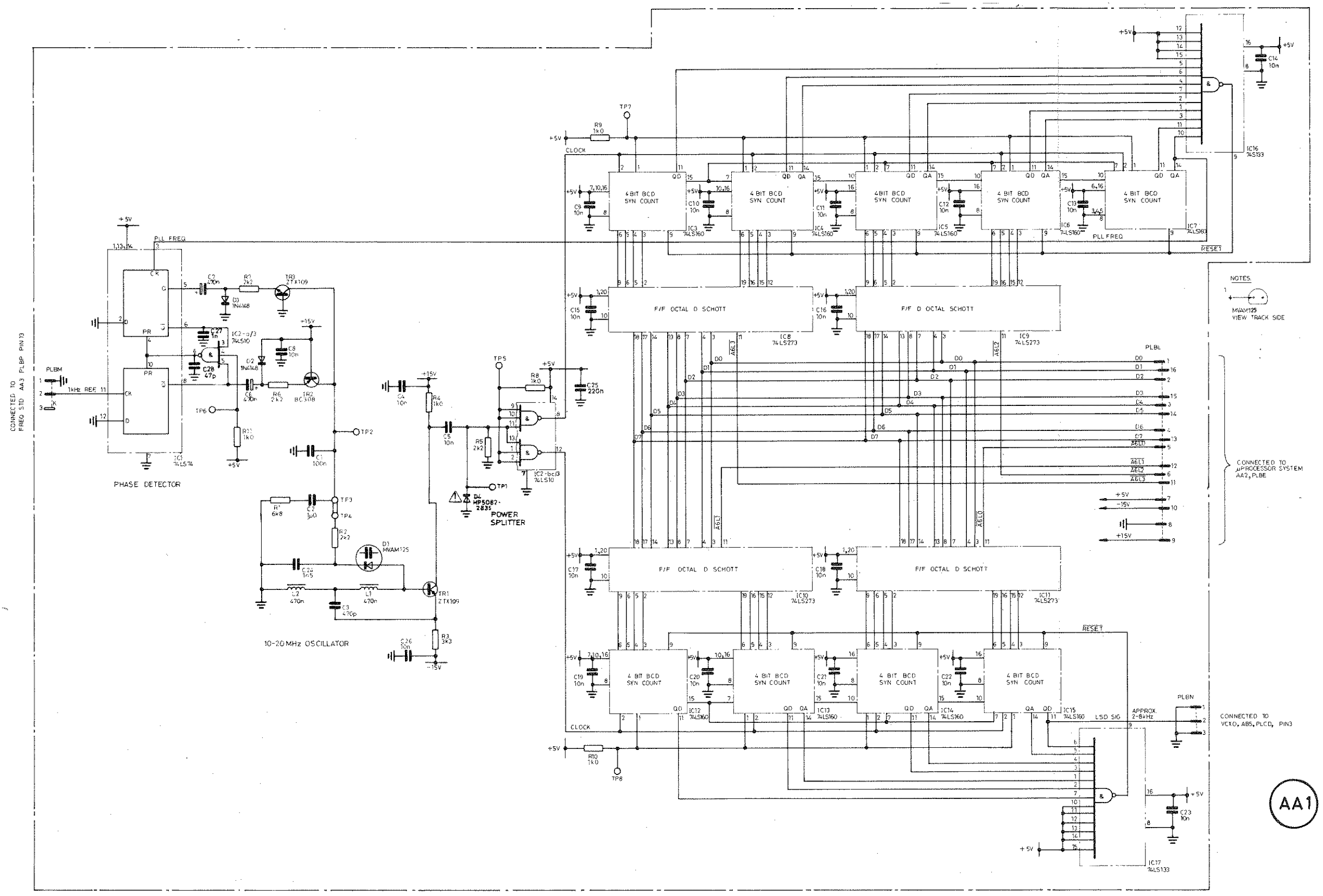
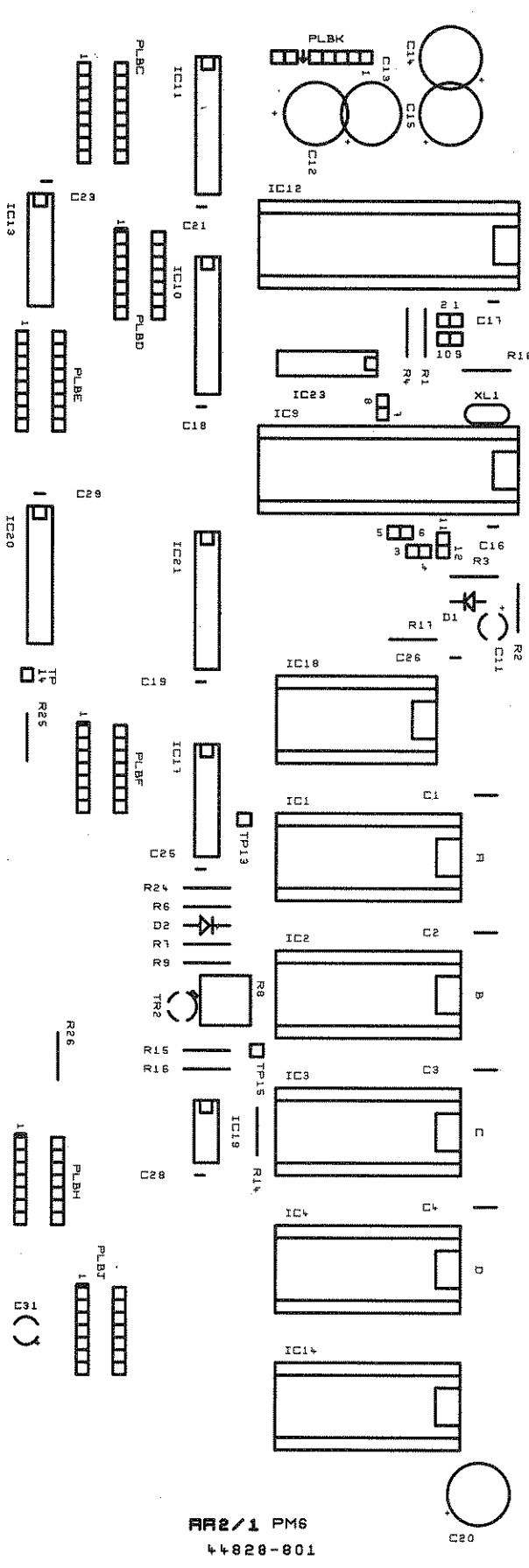


44828-426W Iss. 10

LSD loop, AA1

Fig. 7

Mar. 88 (Am. 3)



Component layout, AA2/1

Fig. 8a
Chap. 7
Page 16

Fig. 8a

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1. COMPONENTS MARKED ⚠ ARE STATIC SENSITIVE, PRECAUTIONS AS PER PCH22810.
2. THE +5V FROM PIN 2 PLBK CONNECTS TO THE POINTS SHOWN, THE +5V FROM PIN 1 CONNECTS TO ALL OTHER +5V POINTS INDICATED.
3. TABLE OF CONNECTIONS FOR ICa(TYPE 2764 UP TO 4 OFF). ALL PIN CONNECTIONS ARE IDENTICAL EXCEPT AS GIVEN IN TABLE.

ICa No.	Ca No.	PIN 20 CONNECTED TO IC17 PIN No.	POSITION ON BOARD
1	1	15	A
2	2	14	B
3	3	13	C
4	4	12	D

AA2/1

Z 44828-801F Iss. 9

Microprocessor system AA2/1

Fig. 8

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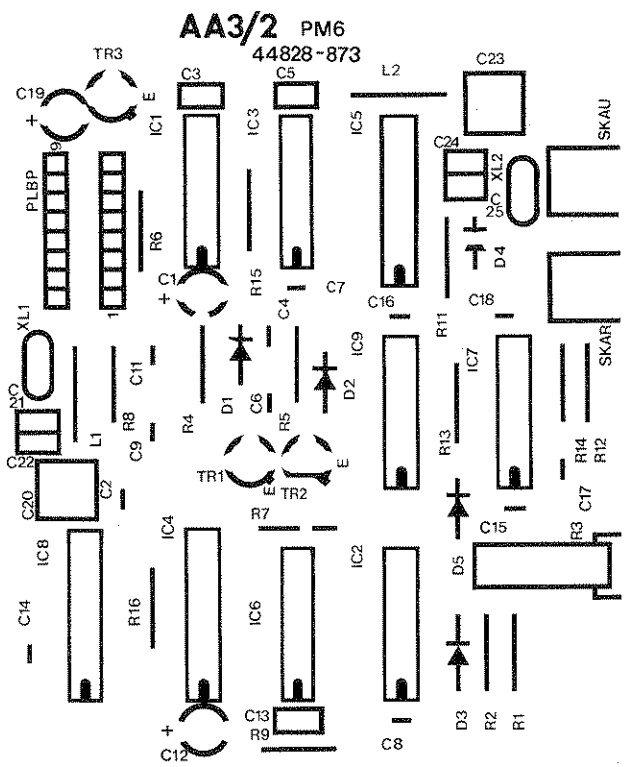
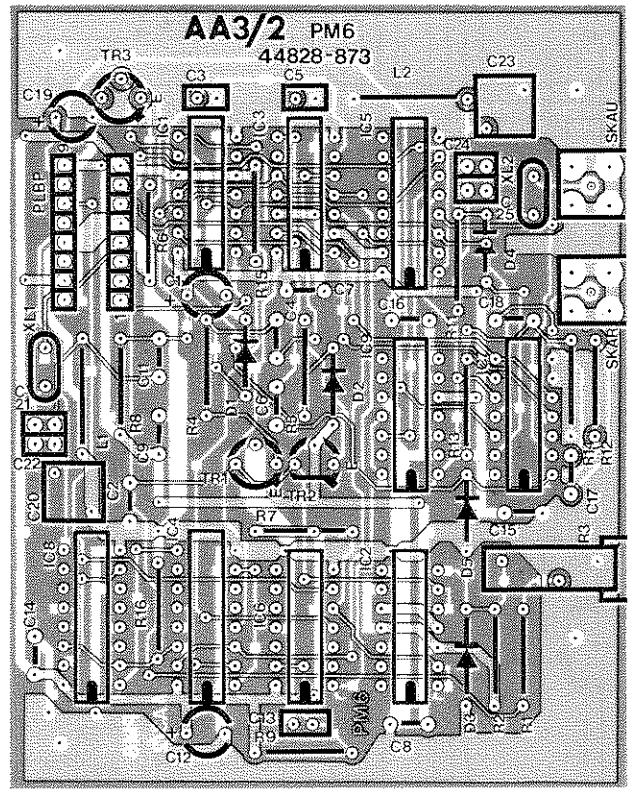
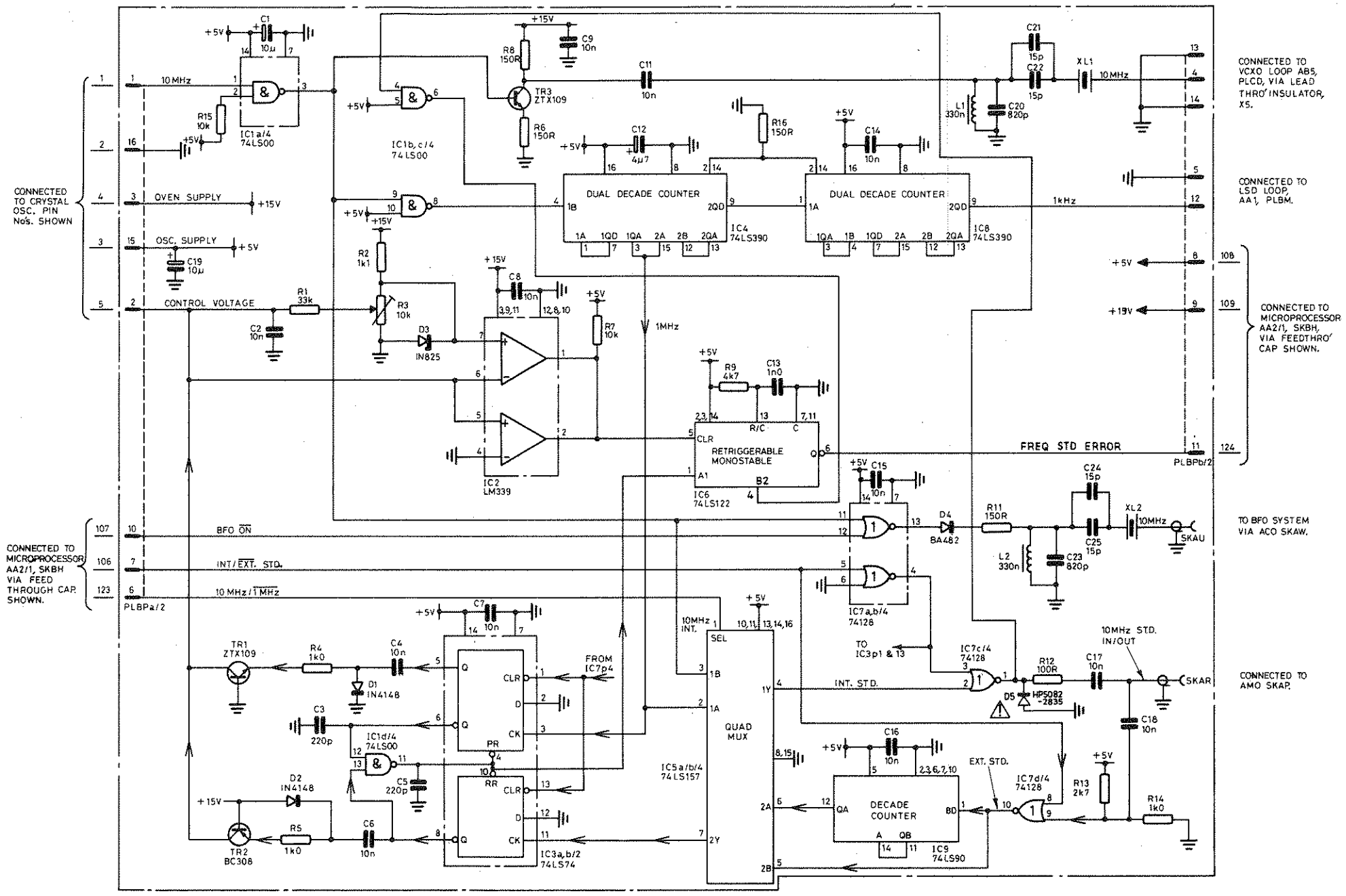




Component layout, AA3/ 2

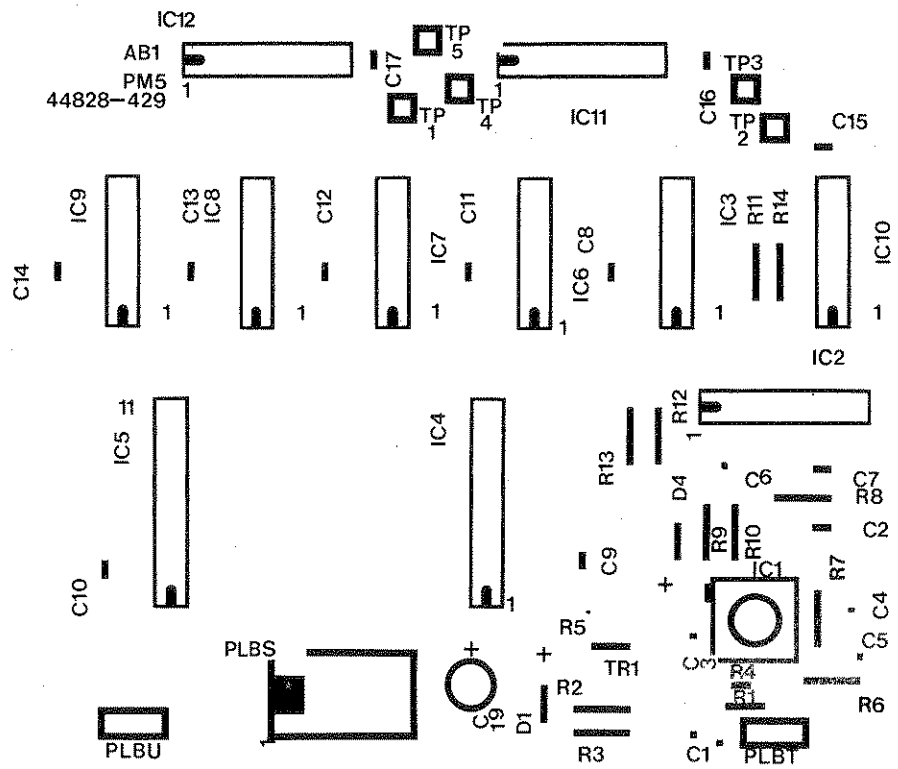


⚠ THIS SYMBOL INDICATES A STATIC-SENSITIVE DEVICE.

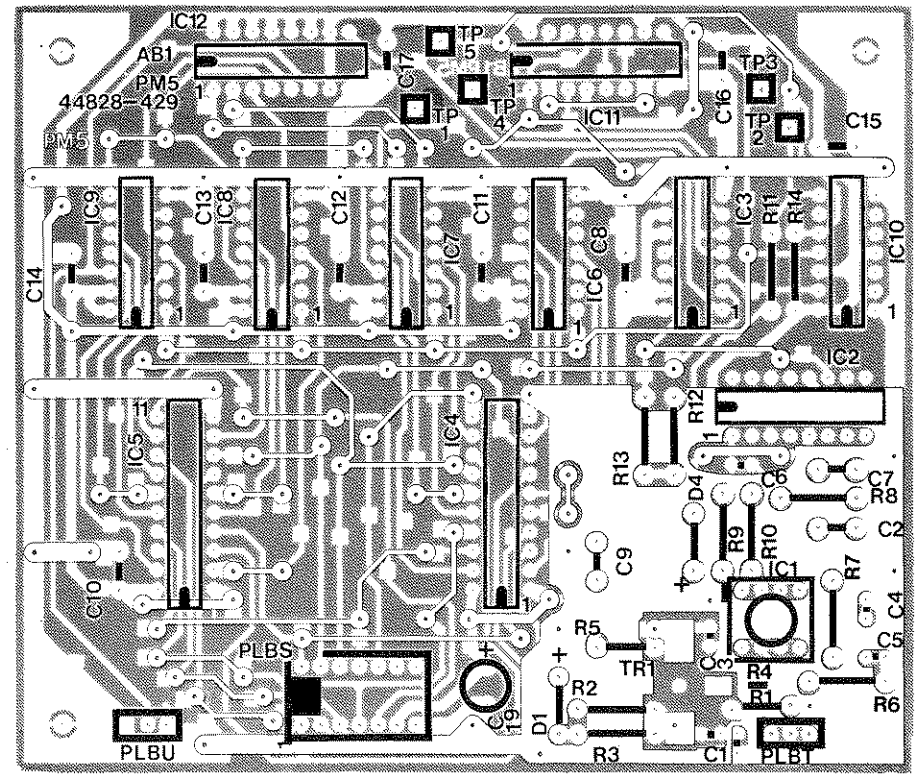
AA3/2

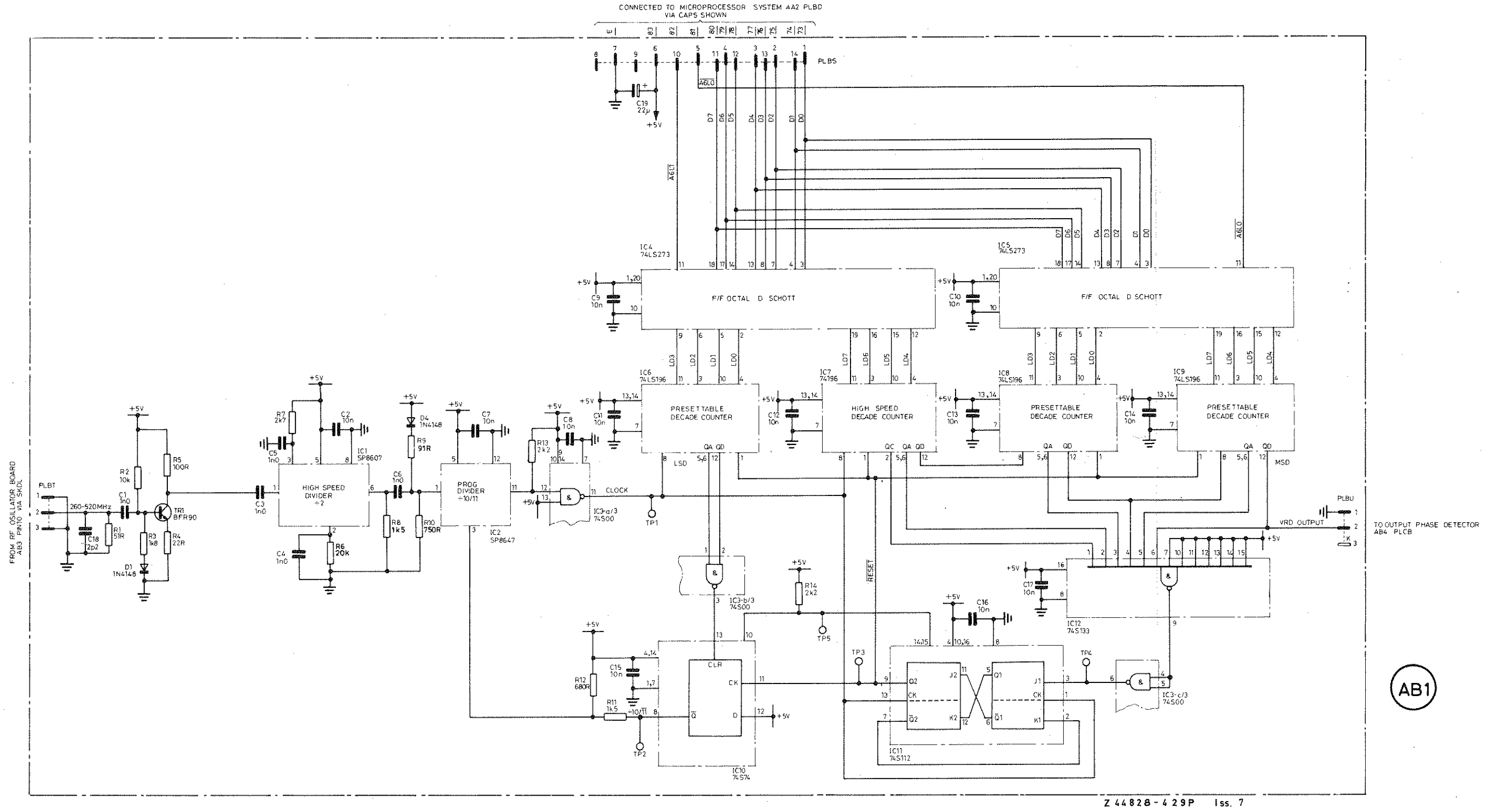
Z 44828-873D Iss. 3

Frequency standard AA3/2



Component layout, AB1

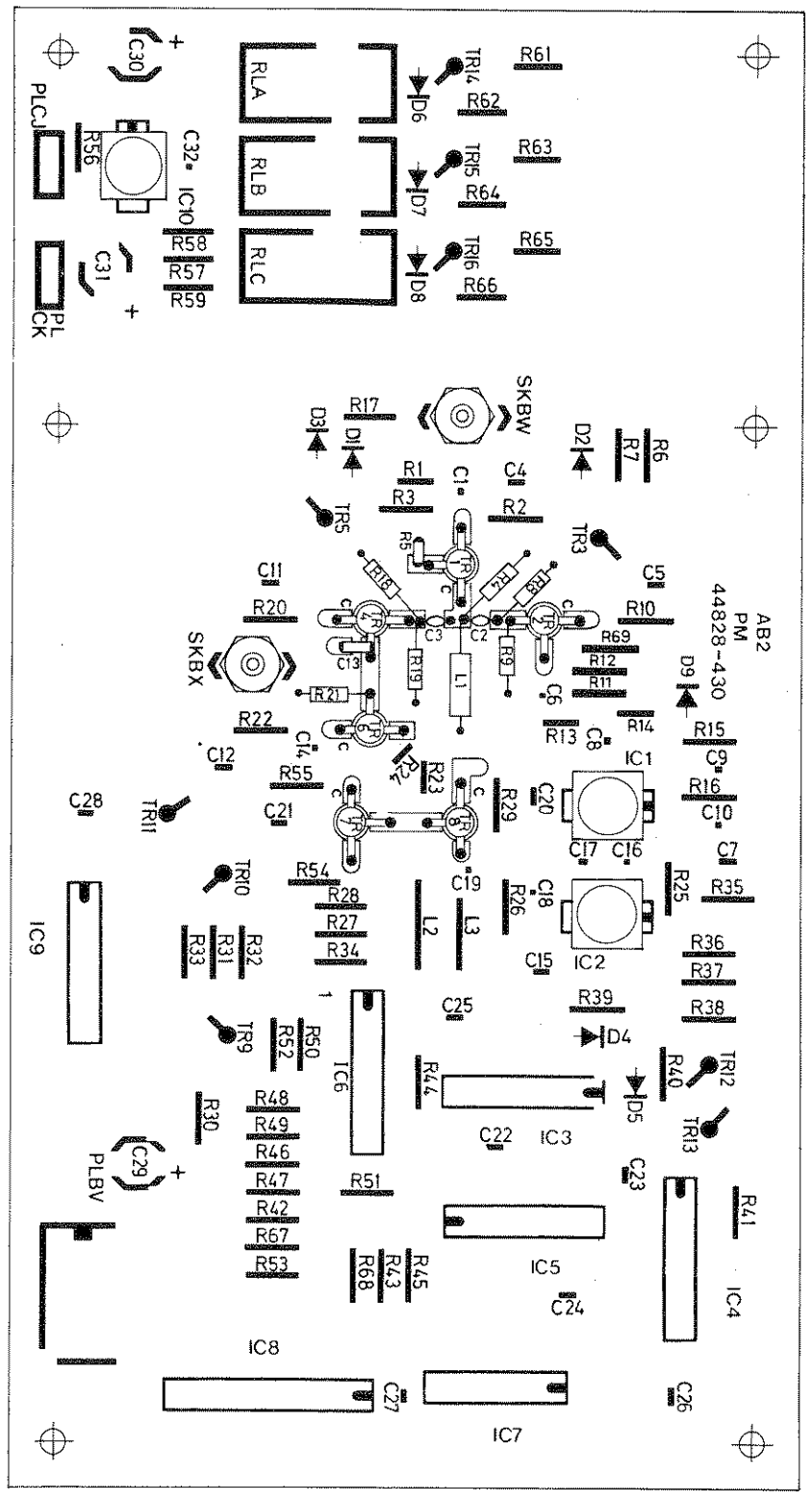




Output v.r.d. AB1

Fig. 10

Mar. 88 (Am. 3)



Component layout, AB2

Fig. 11a
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Fig. 11a

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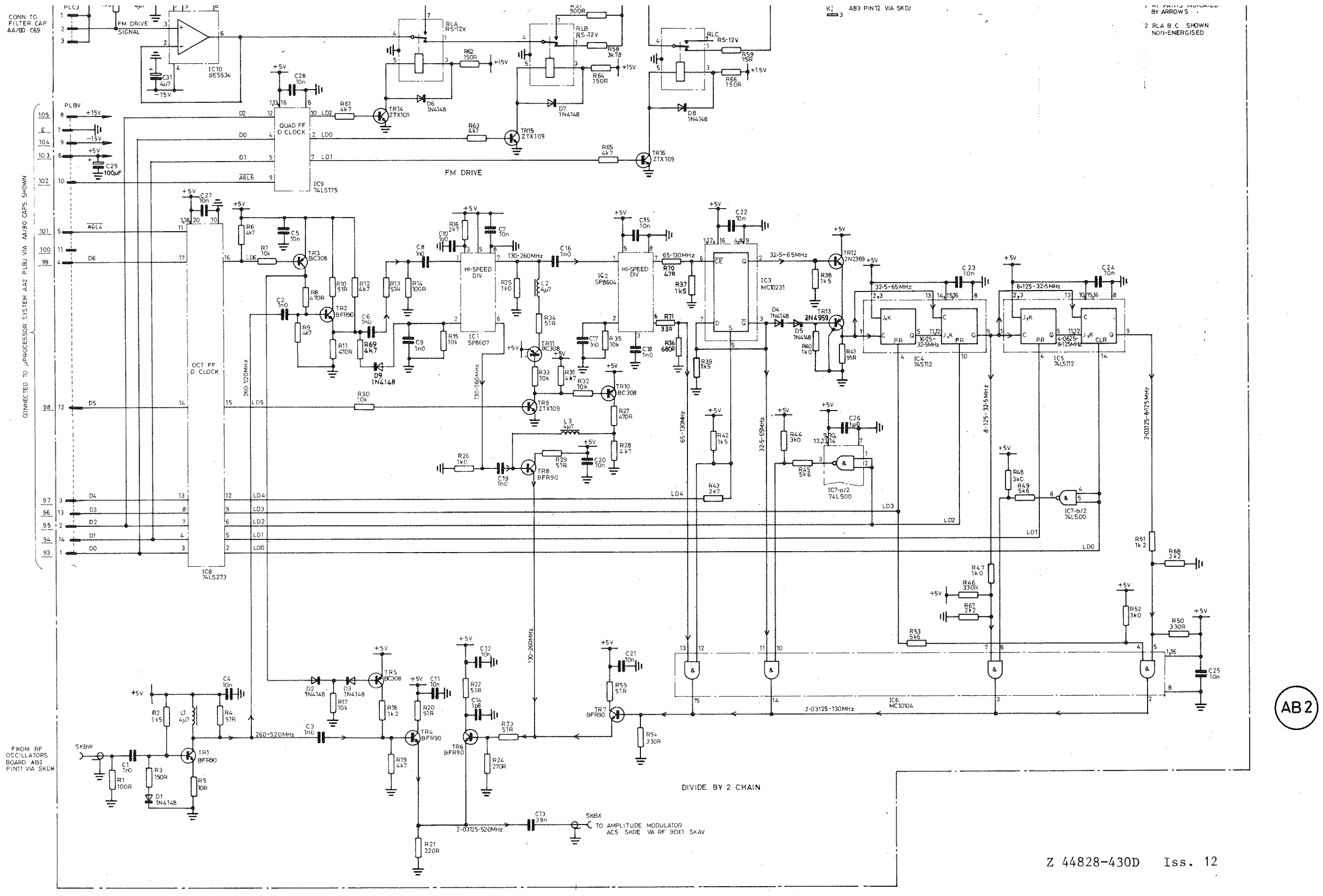
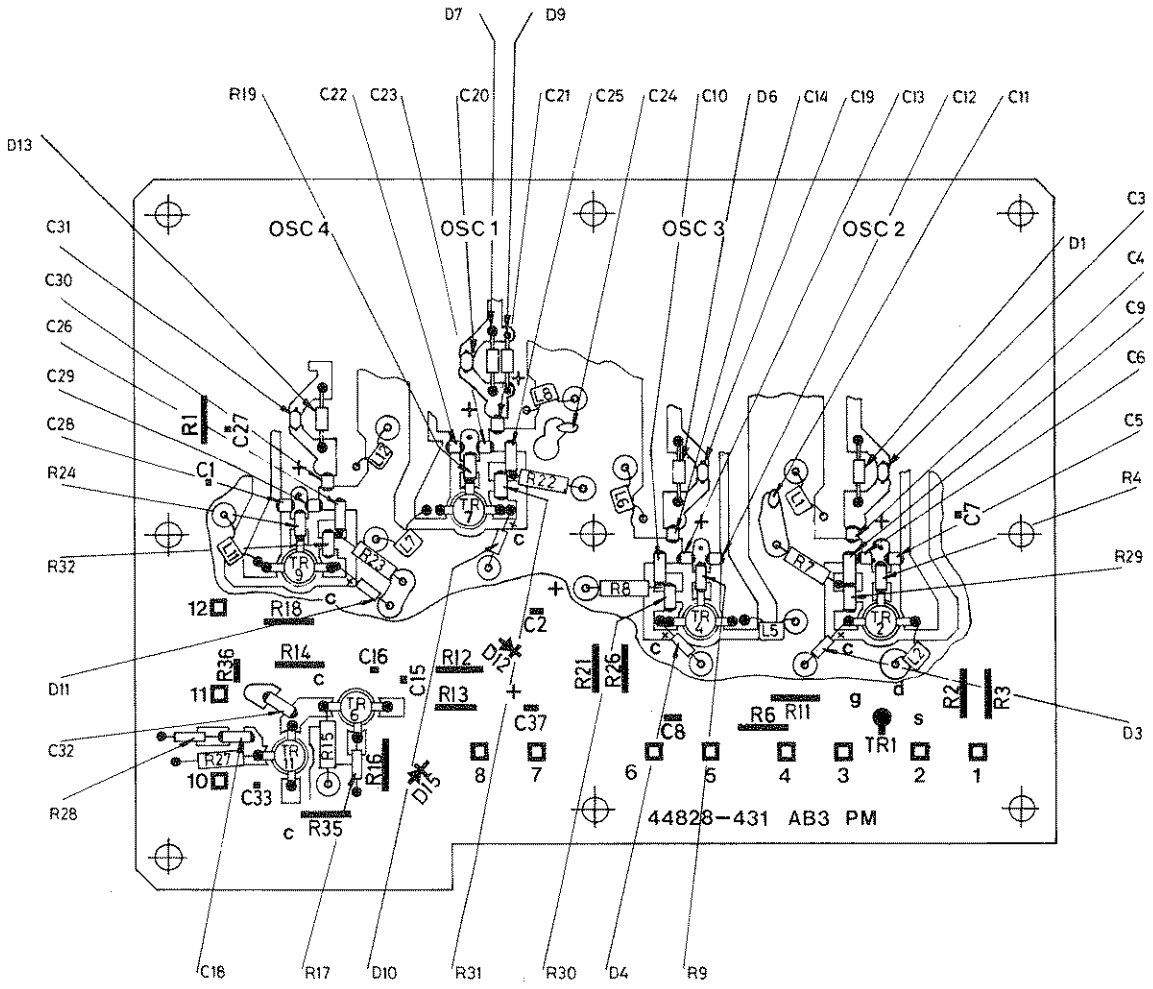


Divide-by-2 chain and f.m. drive, AB2

Fig. 11

Mar. 88 (Am. 3)



Component layout, AB3

Fig. 12a
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Fig. 12a

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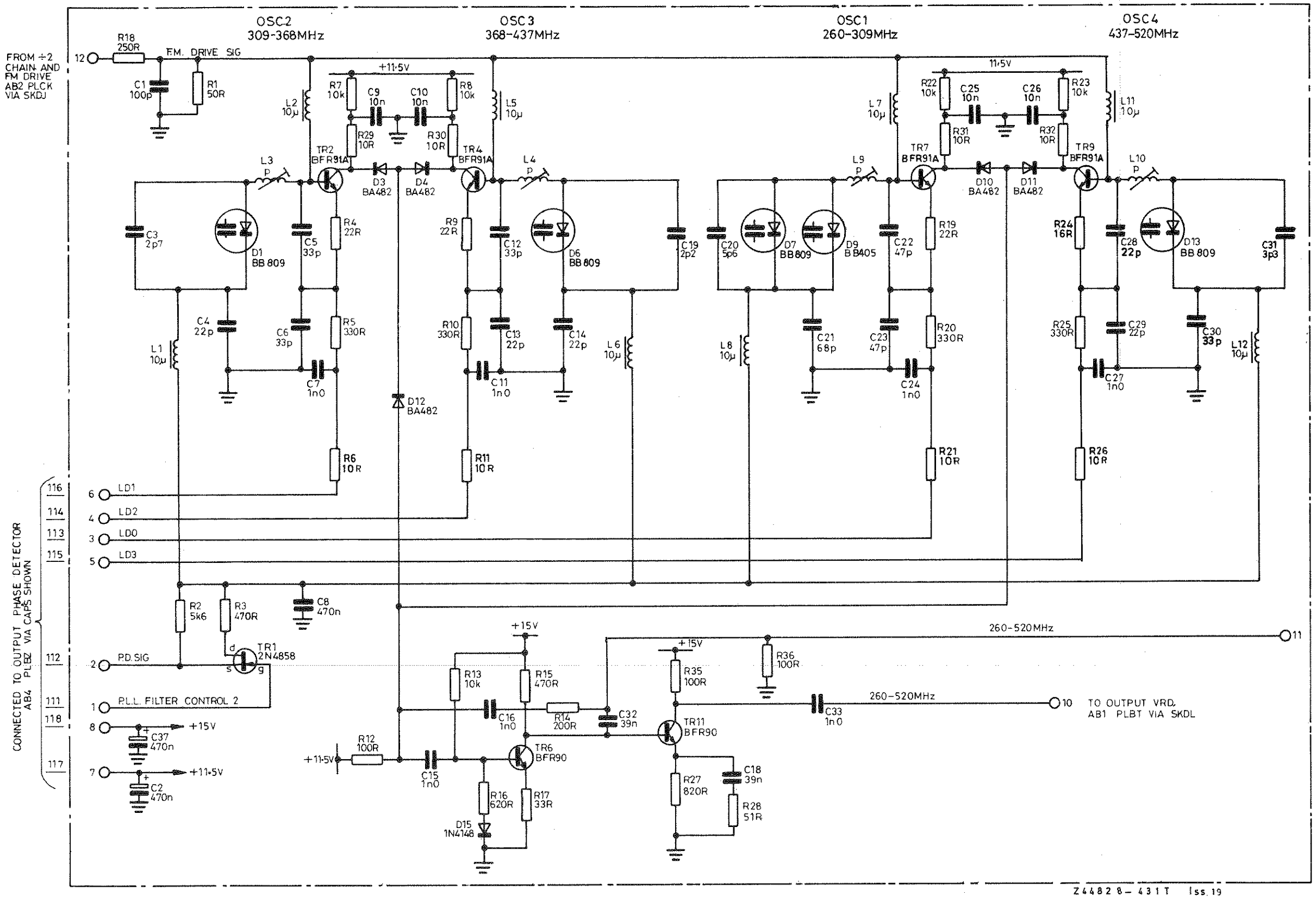
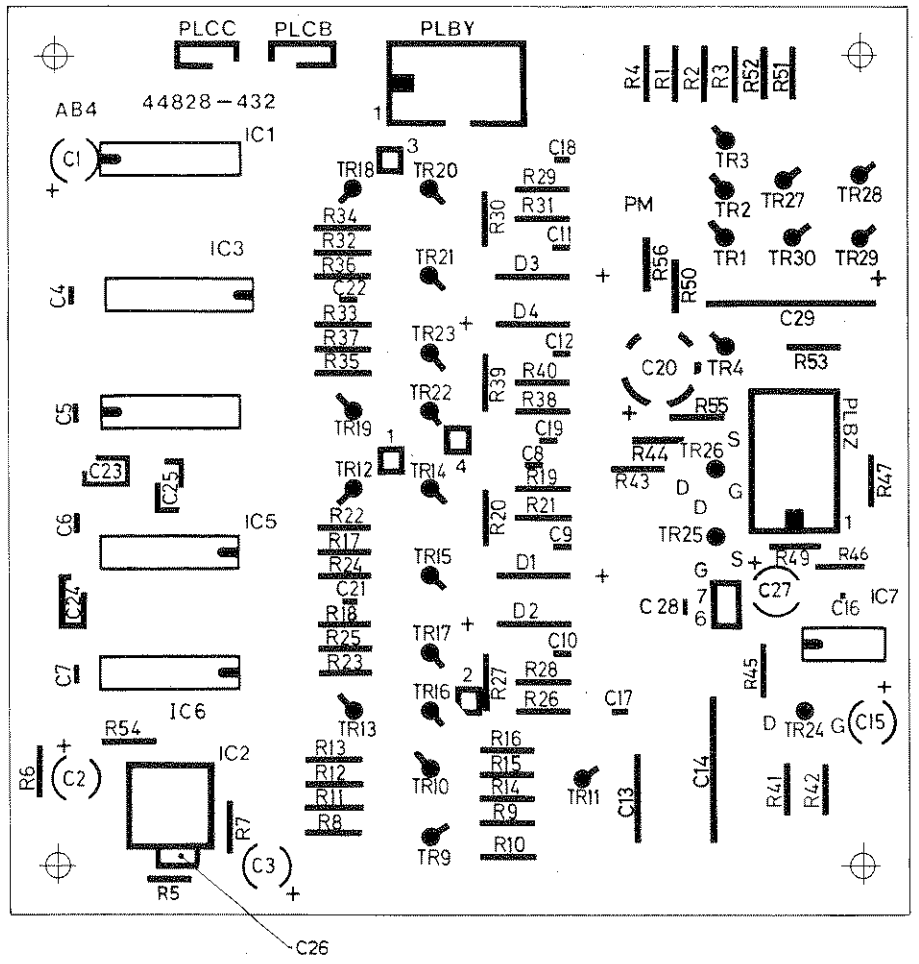
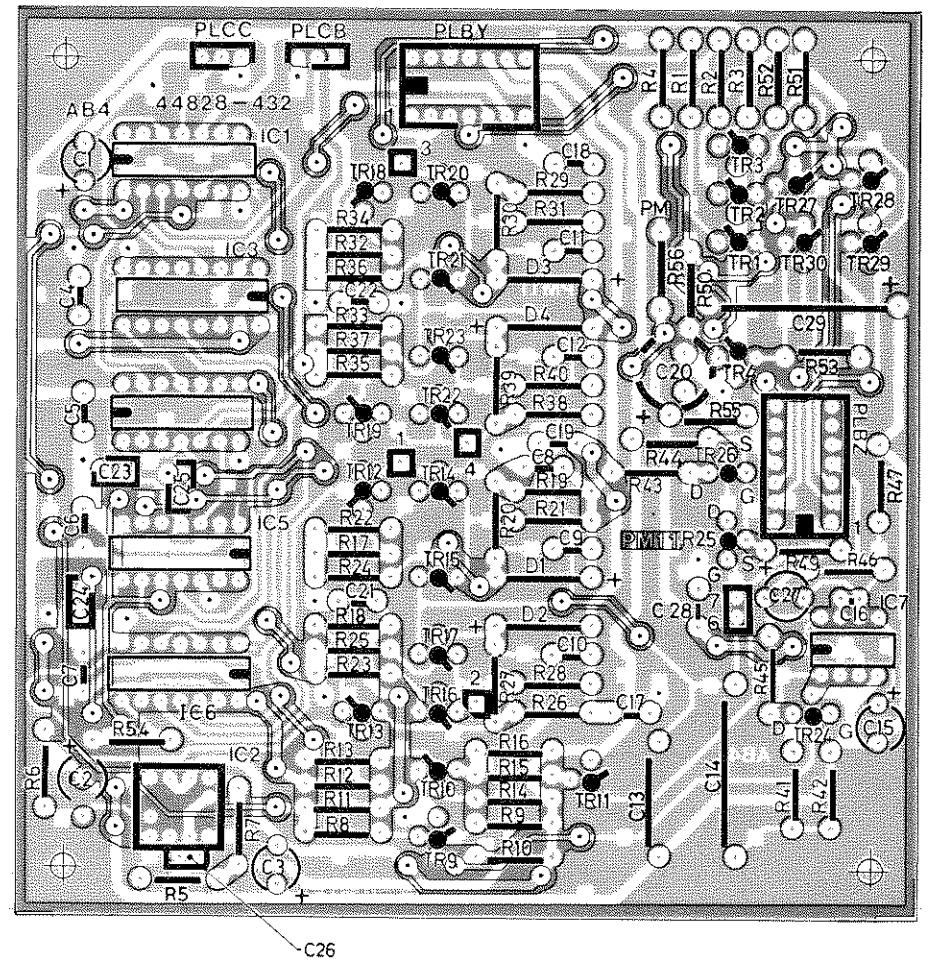


RF oscillators board, AB3

Fig. 12

Mar. 88 (Am. 3)





Component layout, AB4

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Fig. 13a

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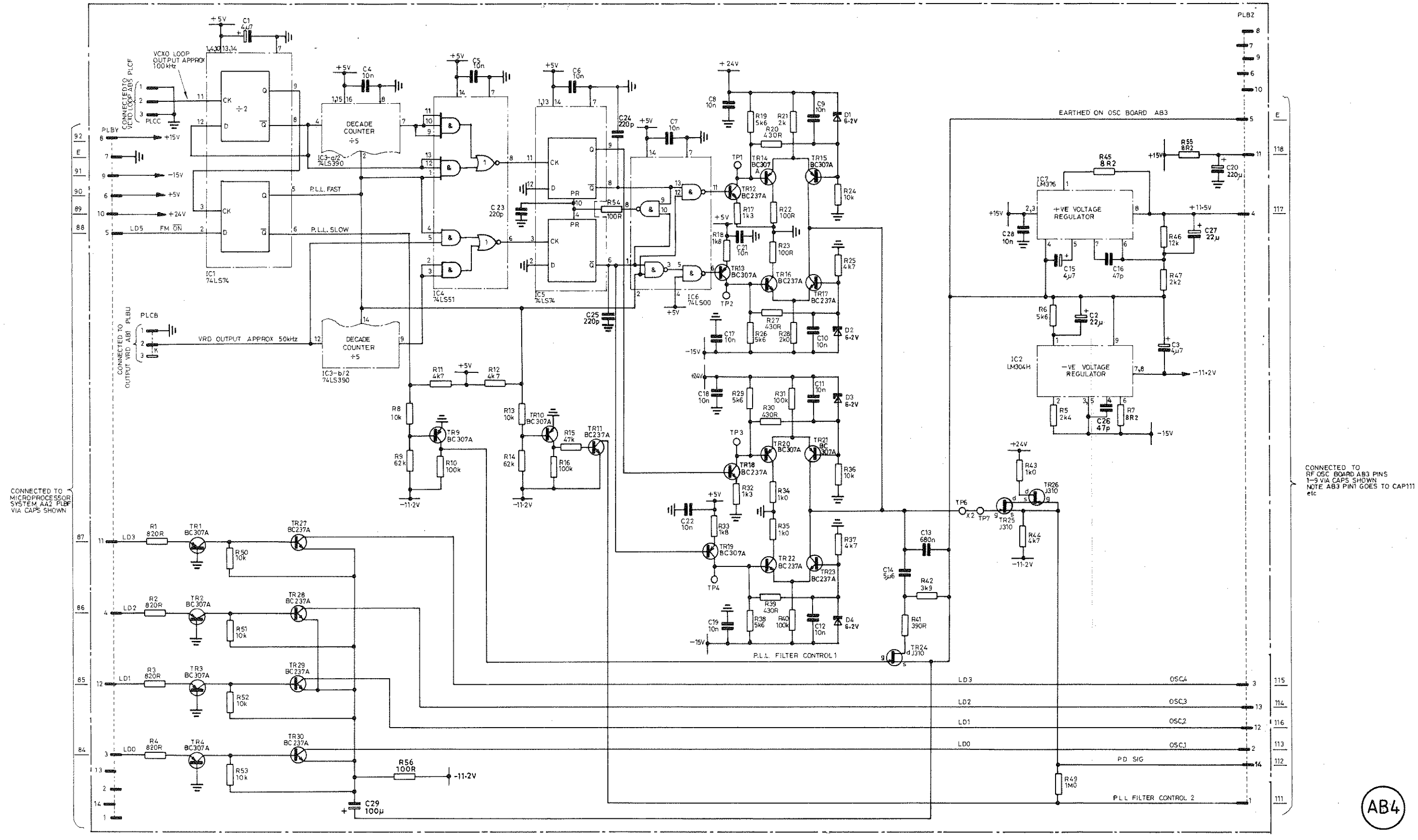
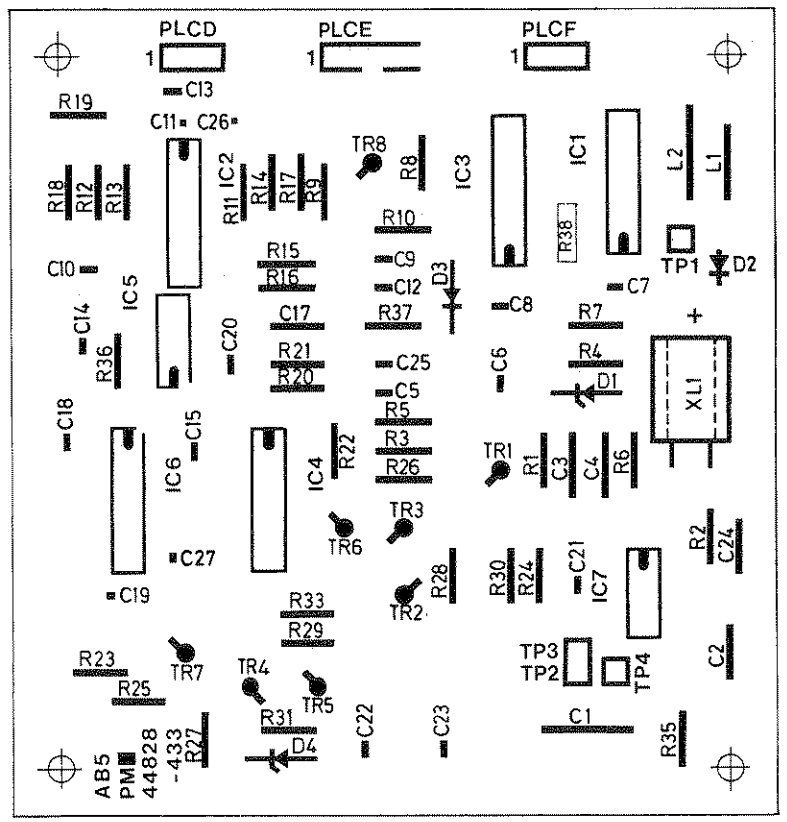


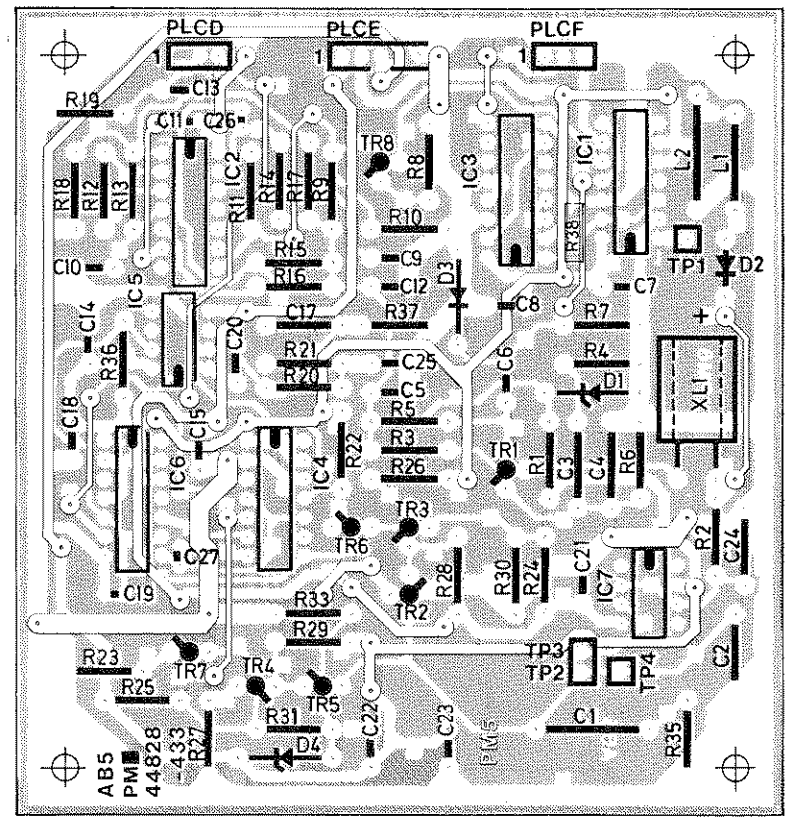
Z 44828-432P Iss. 23

Fig. 13

Mar. 88 (Am. 3)

Output phase detector, AB4





Component layout, AB5

Fig. 14a
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Fig. 14a

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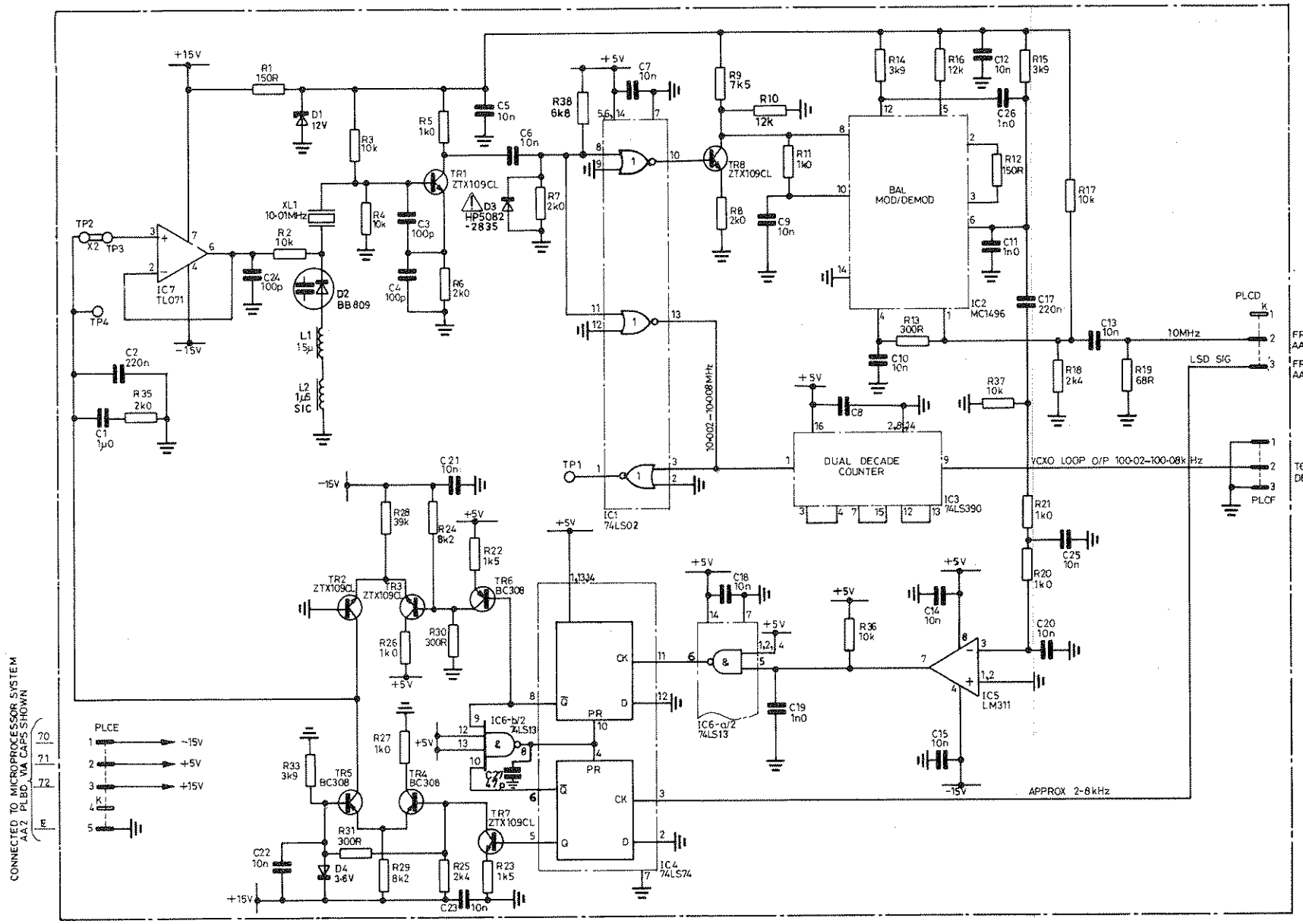
NOTES

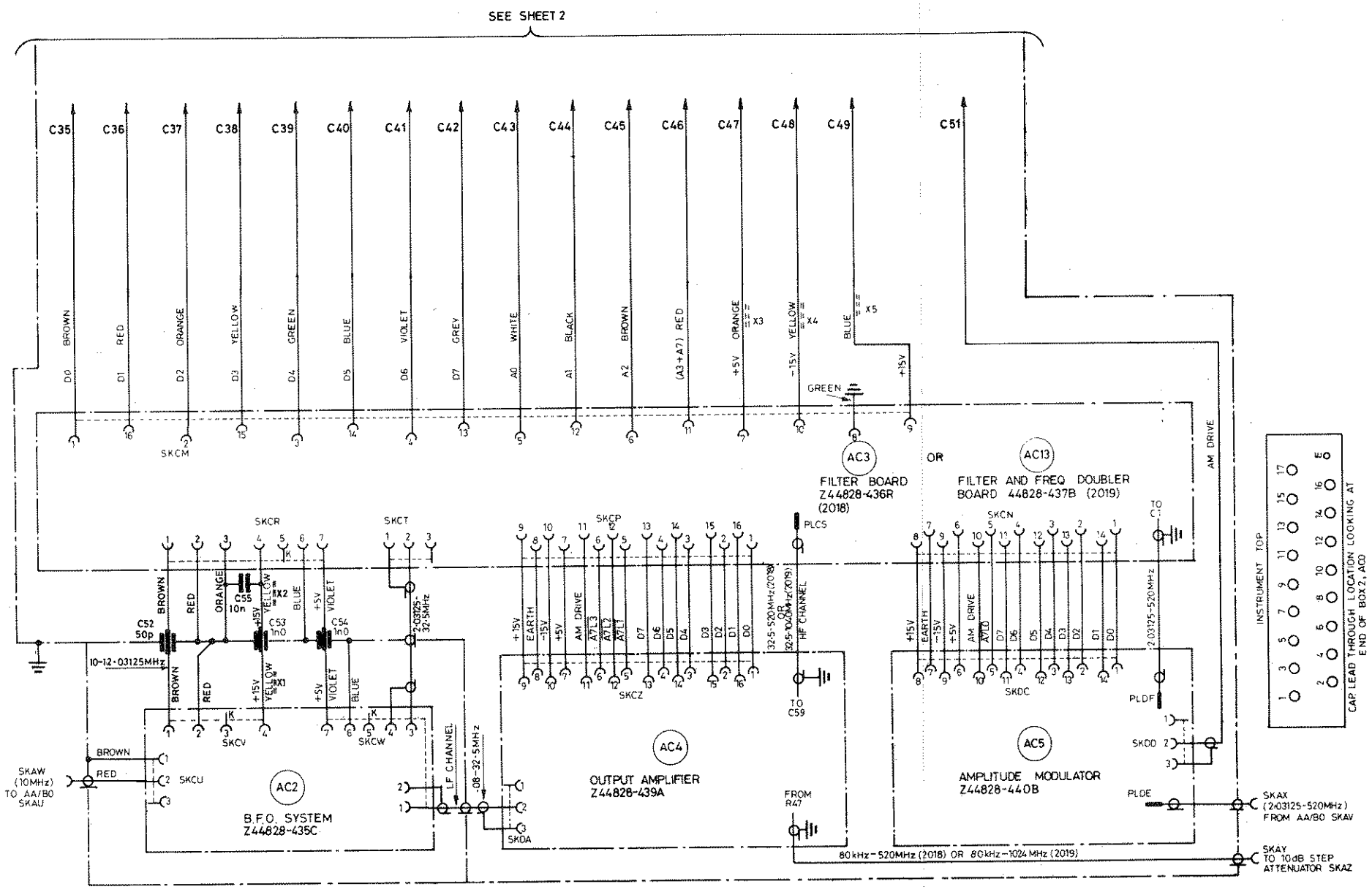
1. COMPONENTS MARKED ⚠ ARE STATIC SENSITIVE.



Z 44828-433X Iss. 19

AB5

Voltage controlled crystal oscillator loop, AB5



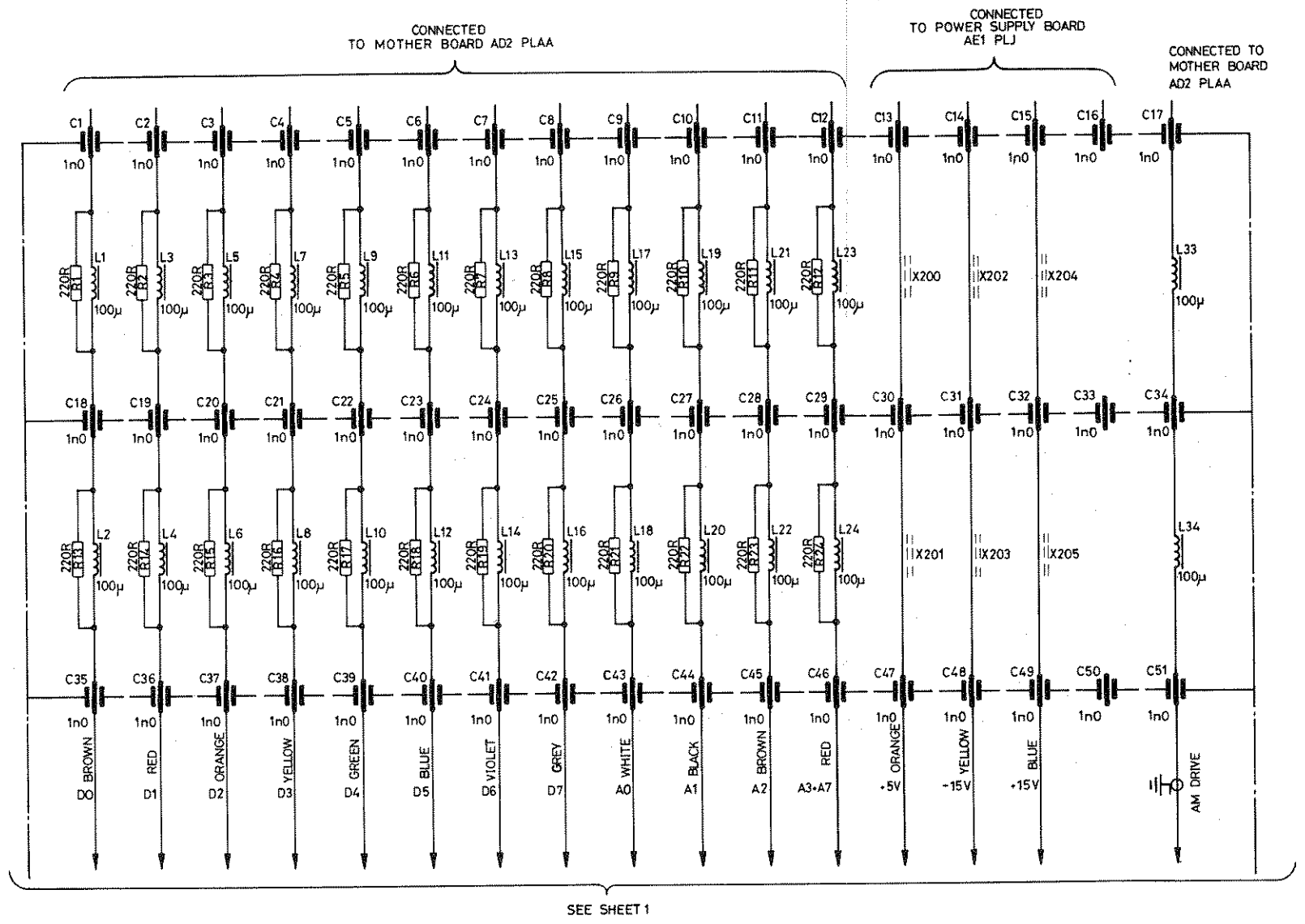
Z 44990-352S Sht. 1 of 2 Iss. 10

AC0

RF box 2 interconnections, AC0

Fig. 15

Mar. 88 (Am. 3)



Z 44990-352S Sht. 2 of 2 Iss. 1

AC0

RF Box 2 interconnections, AC0

Fig. 16

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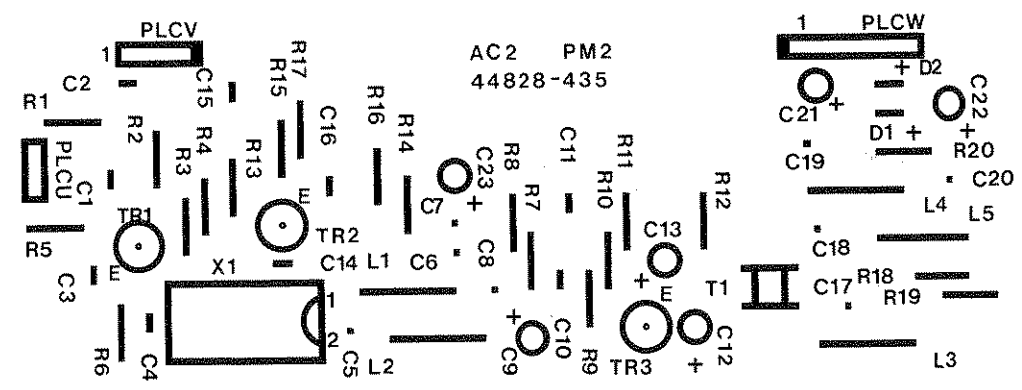

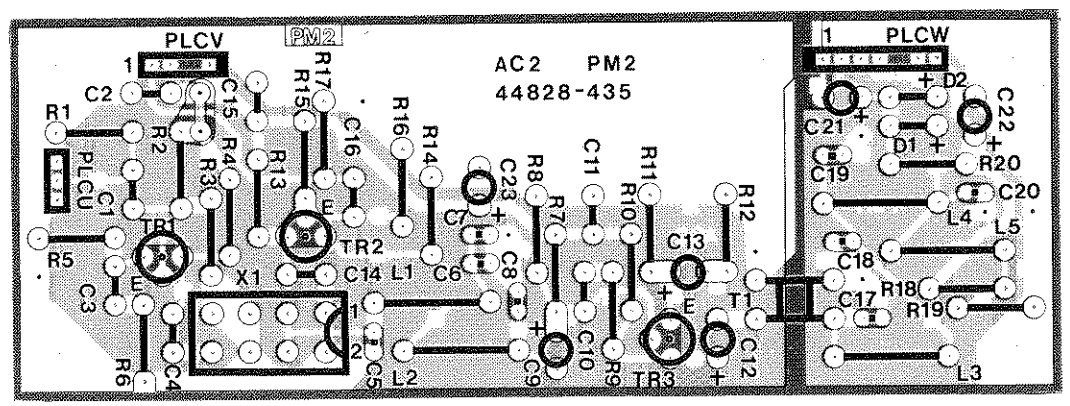

Component layout, AC2

Fig. 17a
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Fig. 17a

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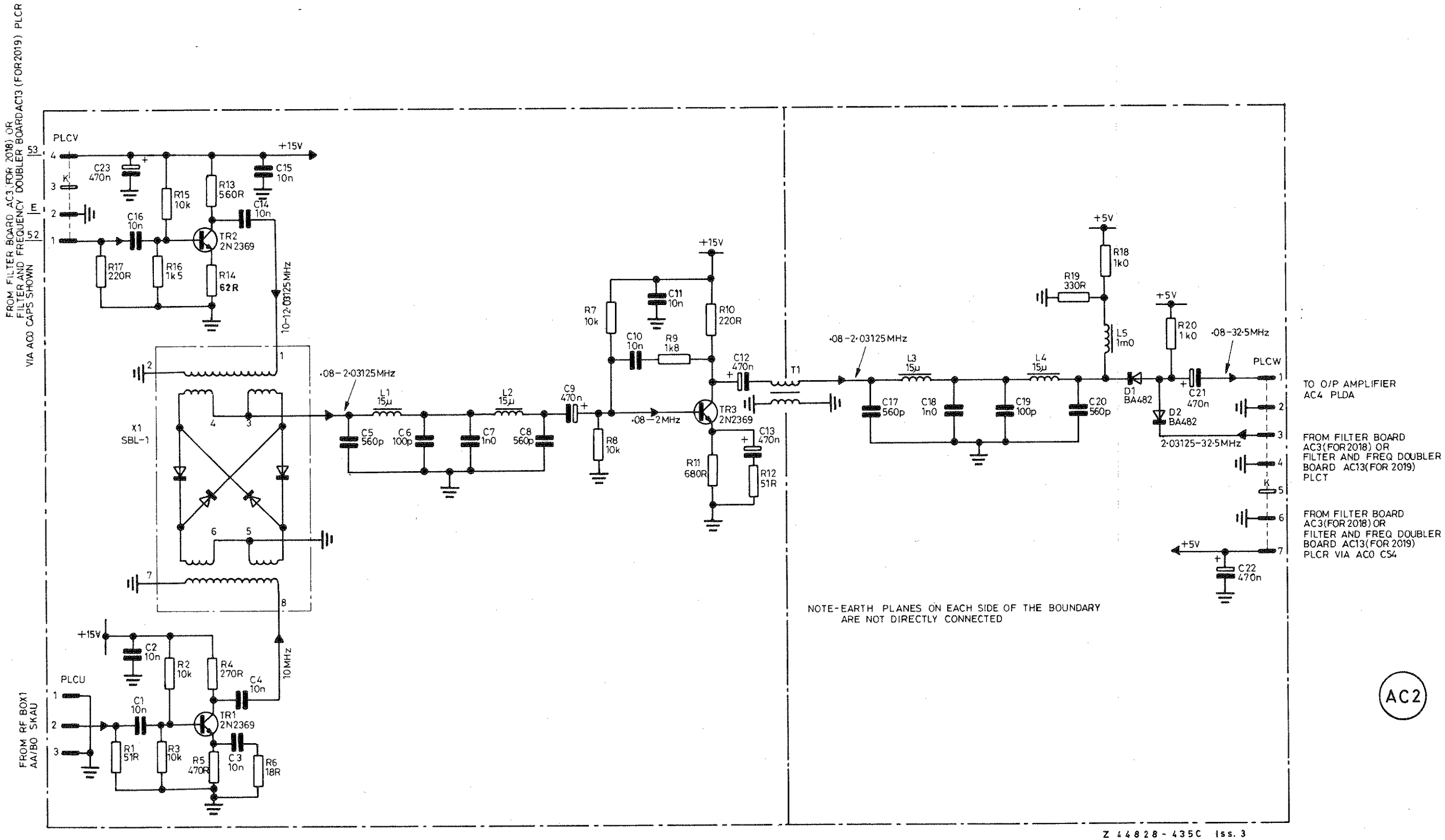
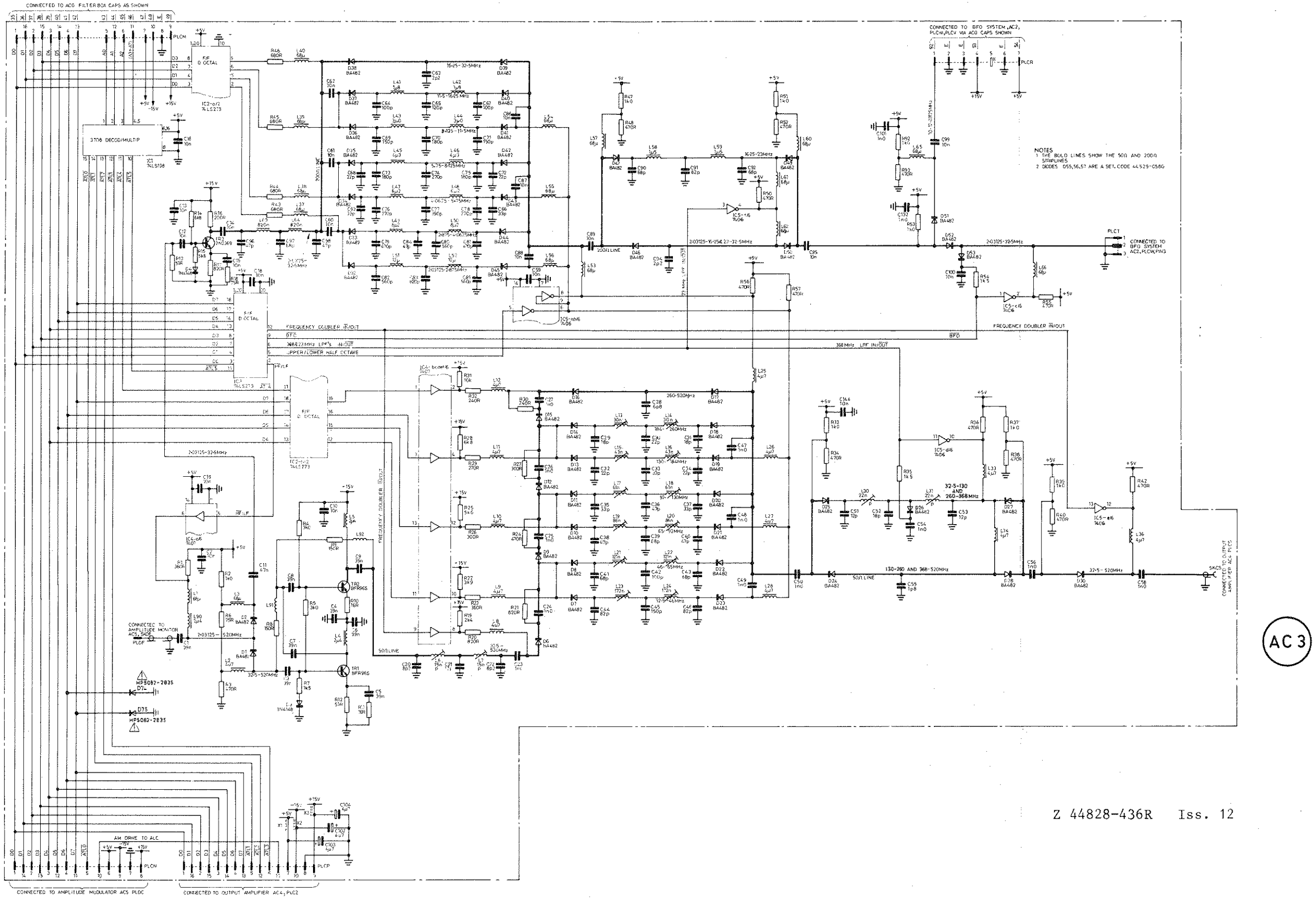


BFO system, AC2

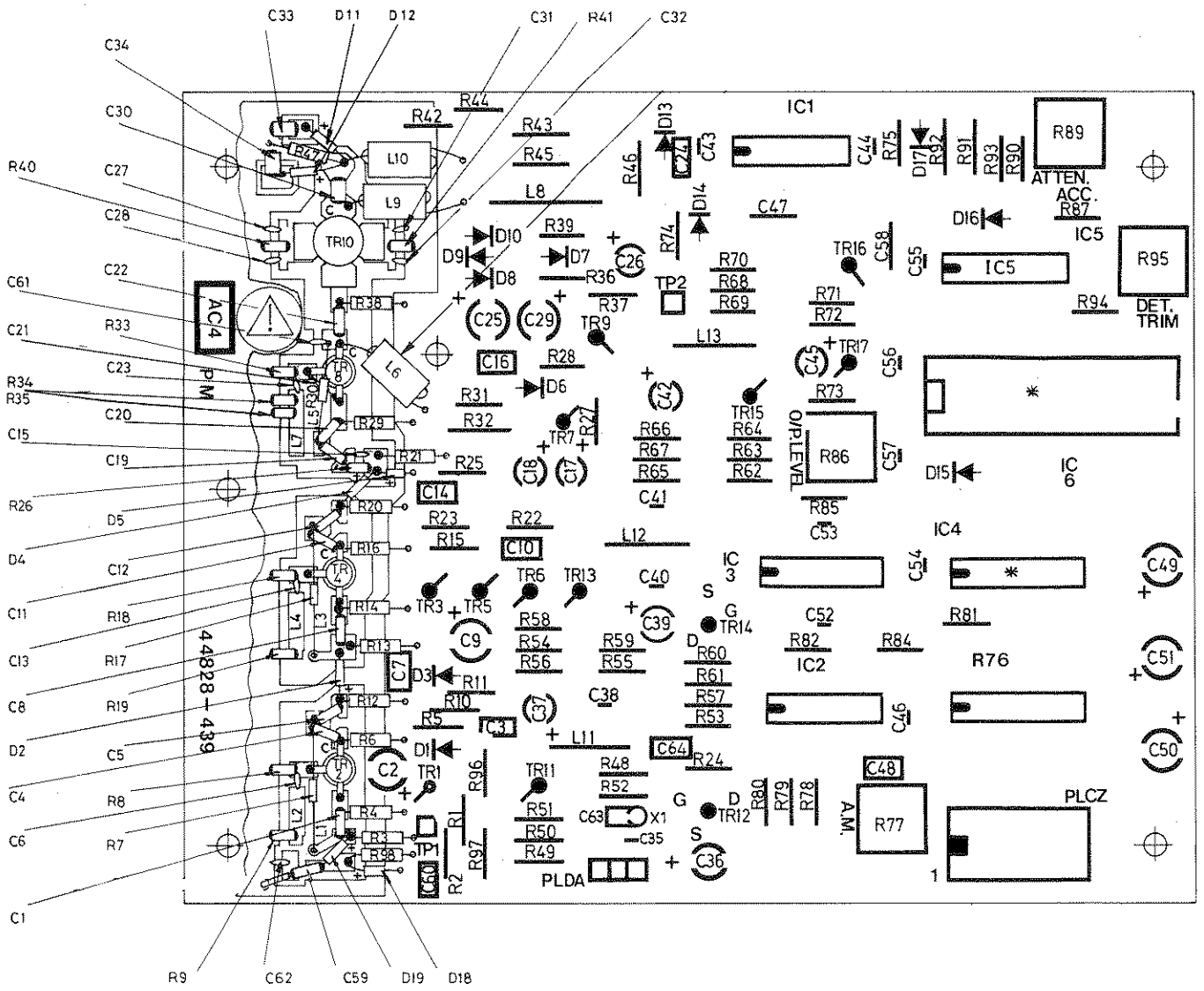
Fig. 17

Mar. 88 (Am. 3)



Z 44828-436R Iss. 12

Filter board, AC3 (for component layout see Fig. 21a)



Component layout, AC4

Fig. 19a
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Fig. 19a

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THE DUST OF WHICH IS TOXIC

2. COMPONENTS MARKED △ ARE STATIC SENSITIVE PRECAUTIONS TO PCH 22810

3. DIODES D11,12,13,16 AND 17 ARE A MATCHED SET, PART Nº 44529-105P

4. FET'S TR12 AND TR14 ARE A MATCHED SET PART Nº C44529-114K.

FROM FILTER BOARD AC3 (FOR 2018) OR FILTER AND FREQ DOUBLER BOARD AC13 (FOR 2019) SKCS

FROM B F O SYSTEM AC5 PLCW

CONNECTED TO FILTER BOARD AC3 (FOR 2018) OR FILTER AND FREQ DOUBLER BOARD AC13 (FOR 2019) PLCP

Z 44828-439A Iss. 24

Output amplifier, AC4

Fig. 19

Mar. 88 (Am. 3)

Fig. 19
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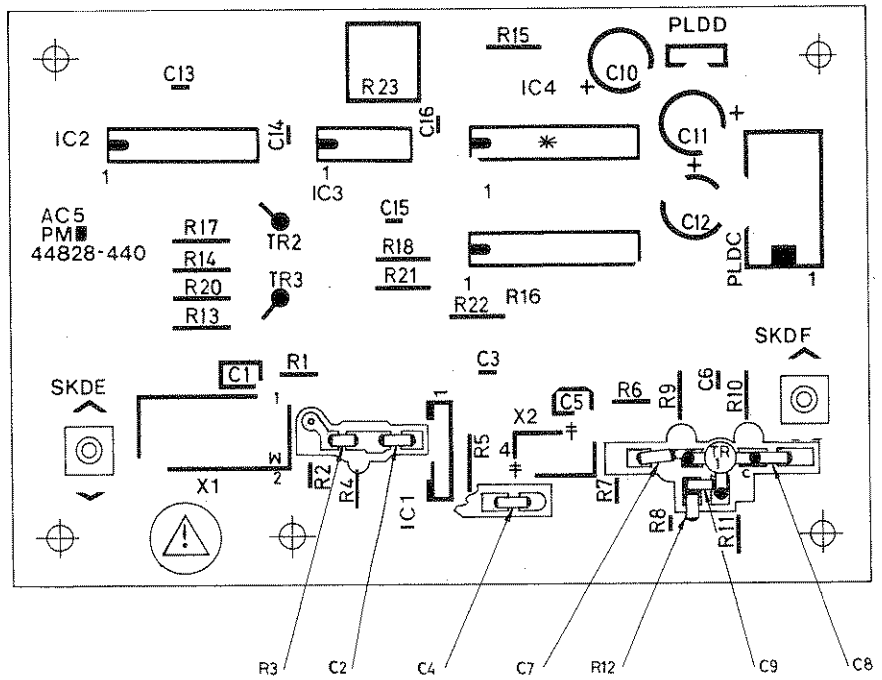
1. WARNING
TR10 INCORPORATES BERYLLIUM OXIDE



Component layout, AC5

Fig. 20a
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Fig. 20a

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1. COMPONENT MARKED ⚠ IS STATIC SENSITIVE, PRECAUTIONS AS PER MIC 2320

FROM DIVIDE BY 2 CHAIN AND FM DRIVE AB2 SKBX VIA AC0 SKAX

2-03125-520MHz 0dBm NOM

SKDE

X1 SBL1

R3 16R

C2 39n

R2 270R

R4 270R

IC1 OM345

+15V

R5 330R

C3 10n

C4 39n

X2 TFM2

C1 1n0

R1 51R

C5 1n0

R6 22R

R7 51R

C6 10n

C7 39n

R8 5k1

R9 10k

R10 240R

TR1 BFR90

R11 240R

C8 39n

C9 39n

R12 16R

2-03125-520MHz 60mV

SKDF

TO FILTER BOARD AC3 (FOR 2018) OR FILTER AND FREQ DOUBLER BOARD AC13 (FOR 2019), C1

PLDC

C11 4µ7

C10 4µ7

C12 4µ7

−15V

+5V

AM DRIVE TO ALC

R13 3k6

R14 510R

R23 500R

R15 330R

R18 3k0

IC3 TL071

C14 10n

C15 10n

R21 18k

R22 18k

TR3 ZTX109

TR2 BC308

R20 10k

C13 10n

+6dB MODE

R17 10k

IC2 7474

A7LO

D7

D6

D5

D4

D3

D2

D1

D0

R16 8x10k

8 BIT D/A CONVERTER

C16 10n

IC4 AD7524

AM DRIVE I/P

PLDD

FROM MOTHER BOARD AD2 PLAA PIN8 VIA AC0 C51

CONNECTED TO FILTER BOARD AC3 (FOR 2018) OR FILTER AND FREQ DOUBLER BOARD AC13 (FOR 2019), PLCN

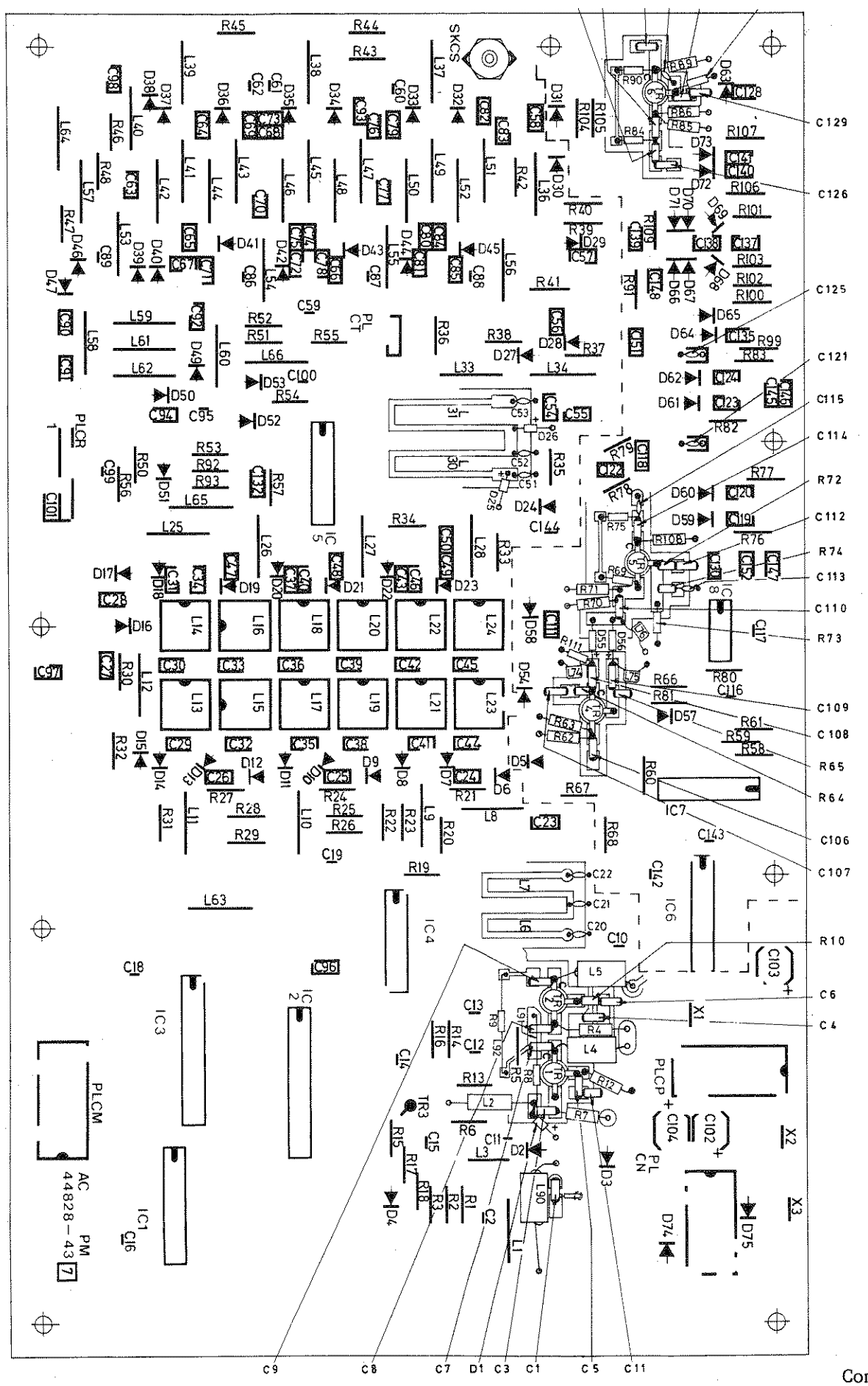
Z 44828 - 440B Iss 8.

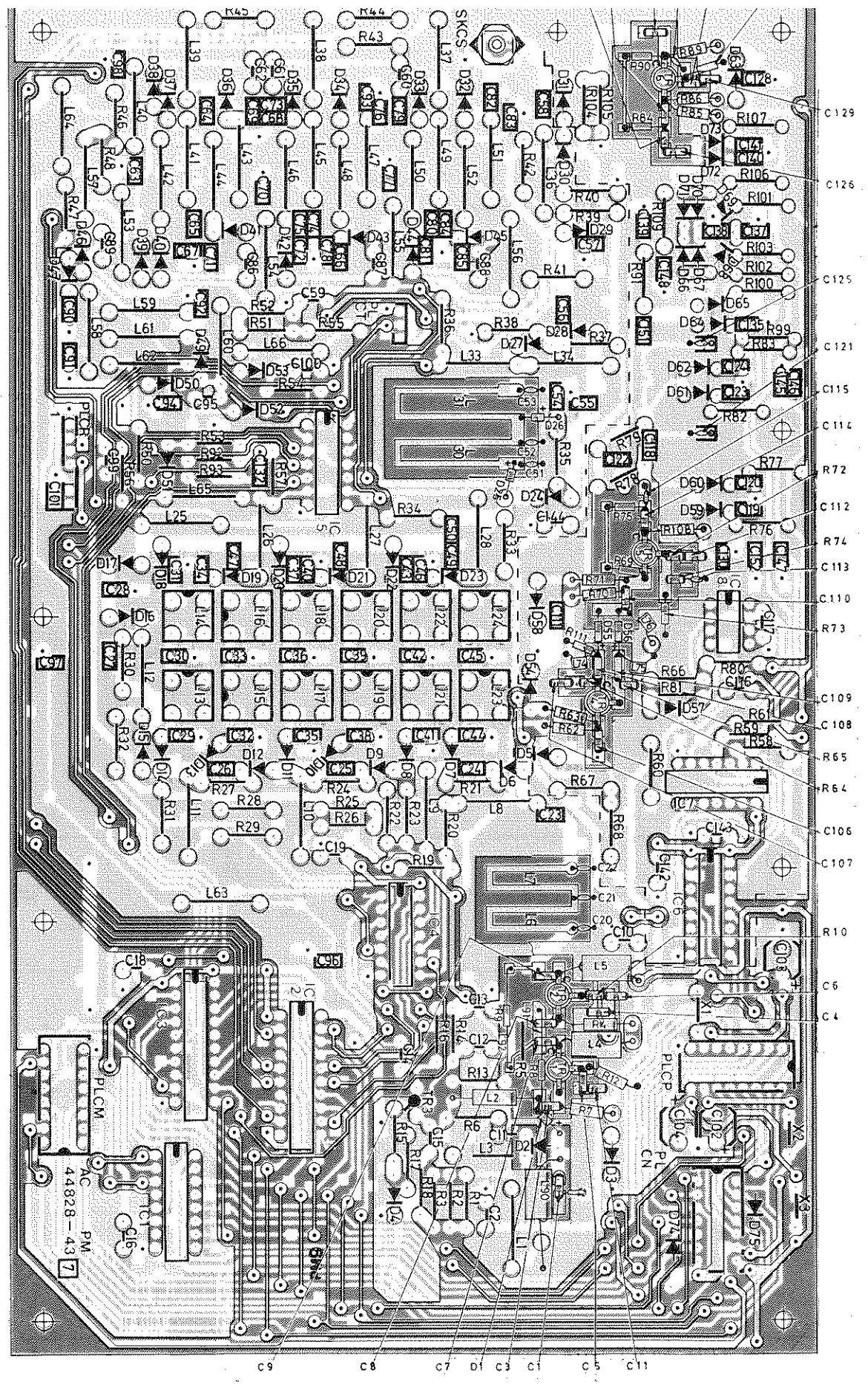
AC5

Amplitude modulator, AC5

Fig. 20

Mar. 88 (Am. 3)





Component layout, AC3 & AC13

Fig. 21a
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Fig. 21a

Mar. 88 (Am. 3)

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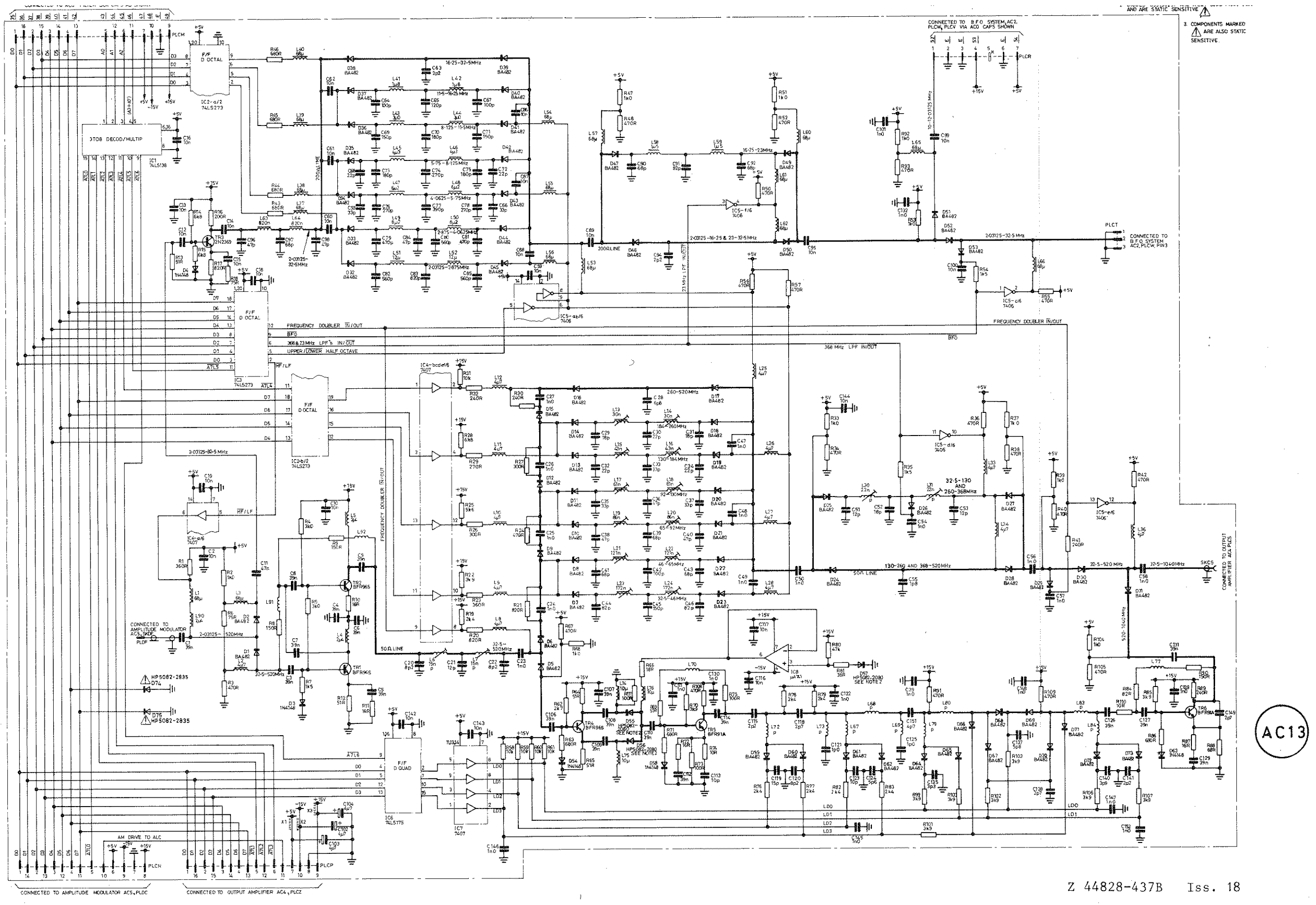
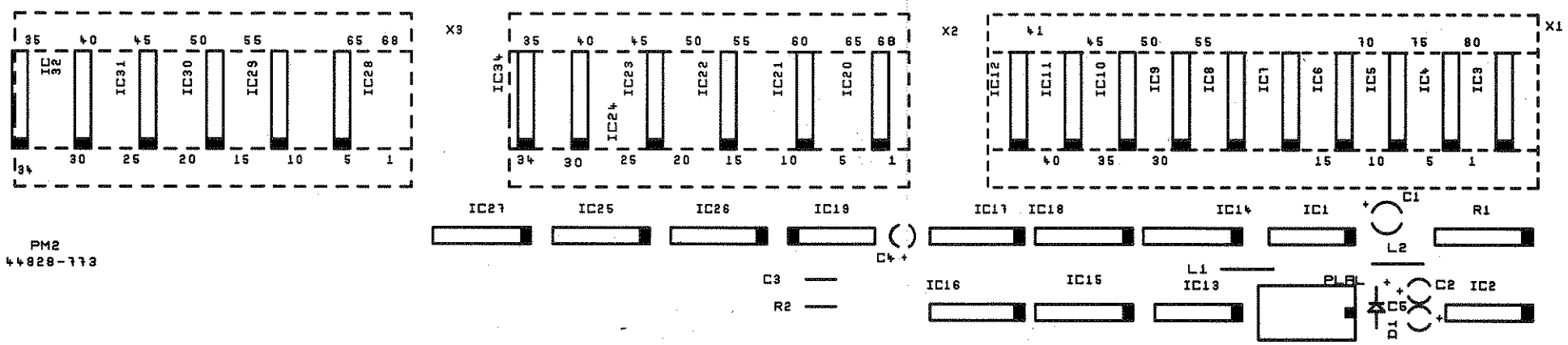


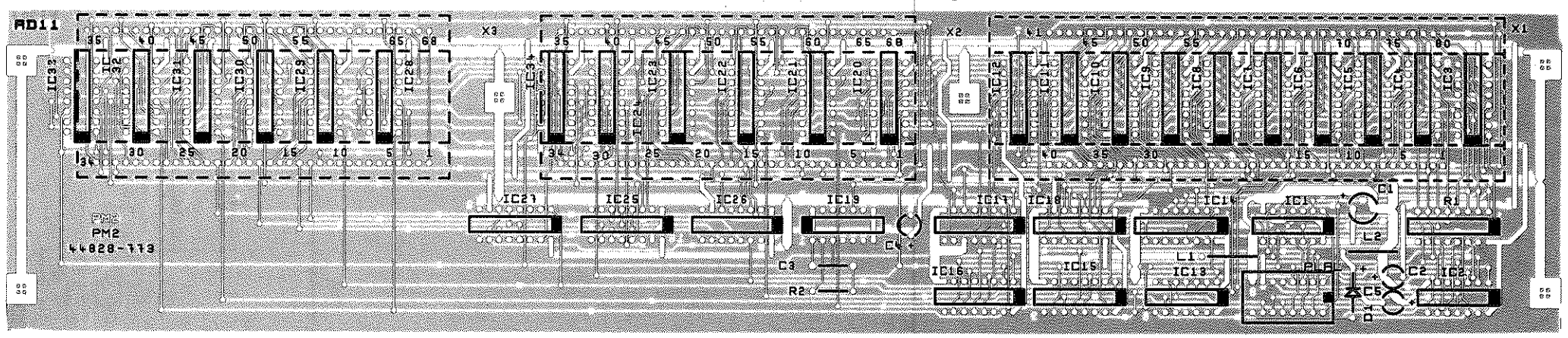
Z 44828-437B Iss. 18

Filter and frequency doubler, AC13 (2019A only)

Fig. 21

Mar. 88 (Am. 3)





Component layout, AD11

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Fig. 22a

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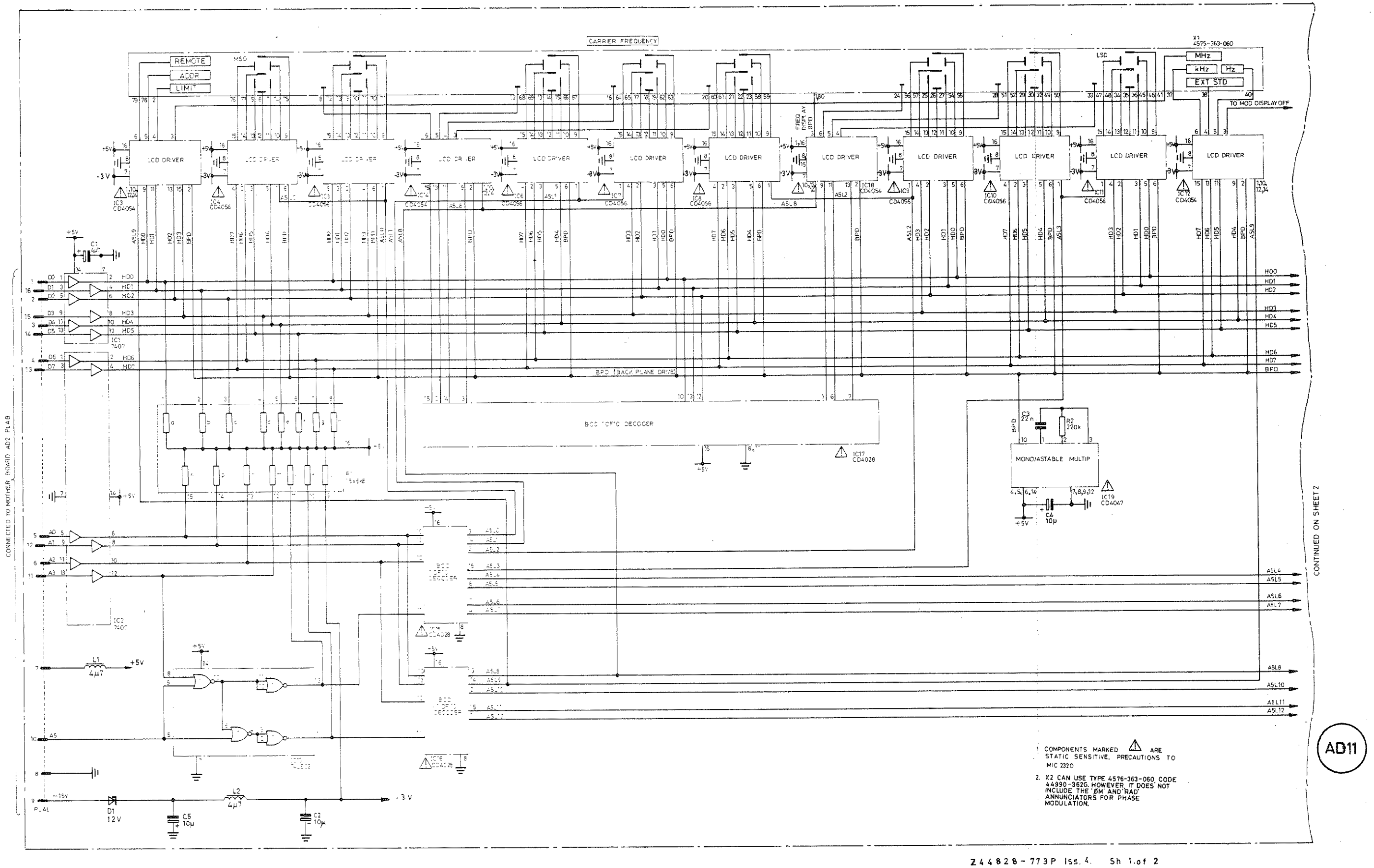


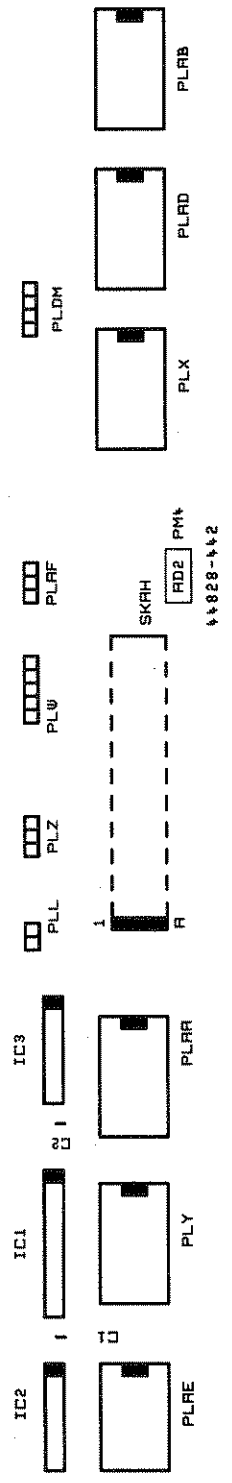
Display board, AD11 (Sheet 1)

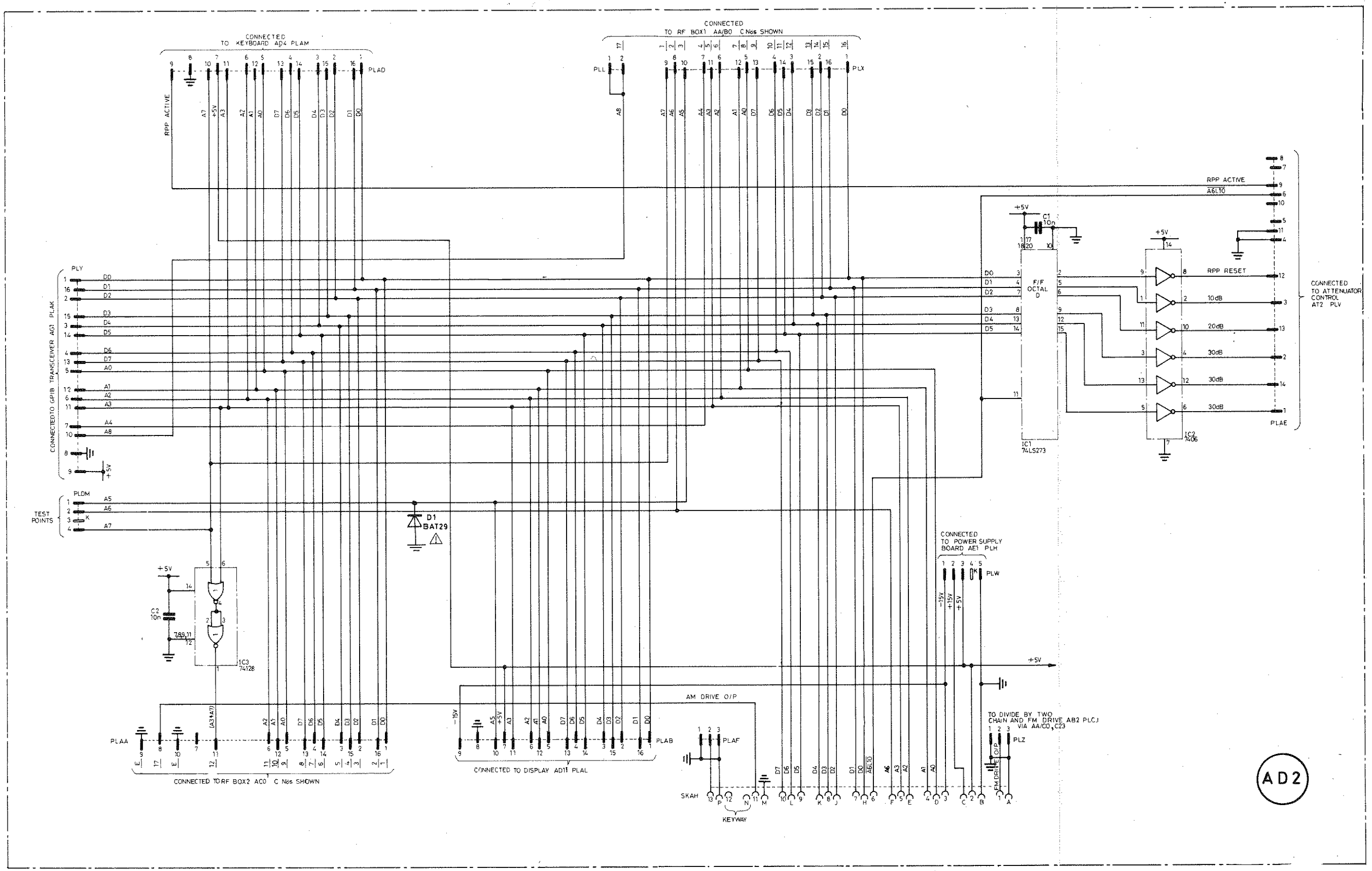
Display board, AD11 (Sheet 2)

Fig. 23

Mar. 88 (Am. 3)

Component layout, AD2



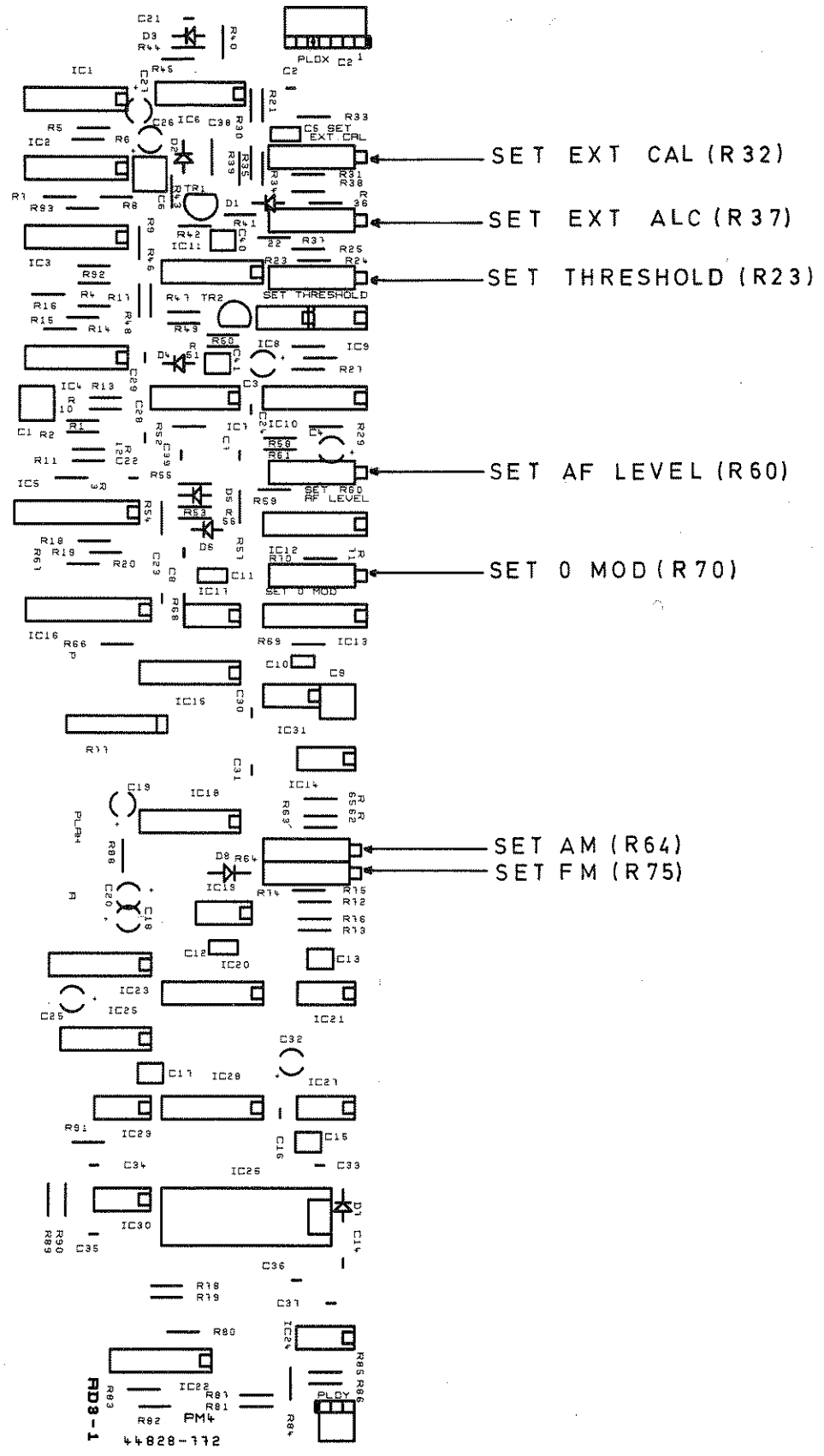


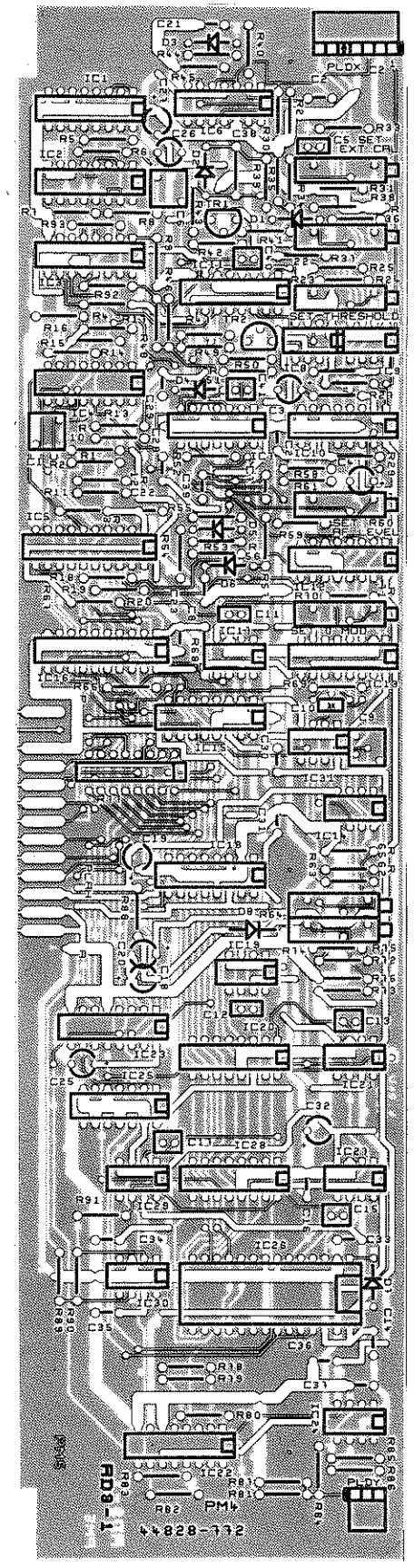
Z 44828-442A Iss. 8

Motherboard, AD2

Fig. 24

Mar. 88 (Am. 3)





Component layout, AD3/1

Fig. 25a
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Fig. 25a

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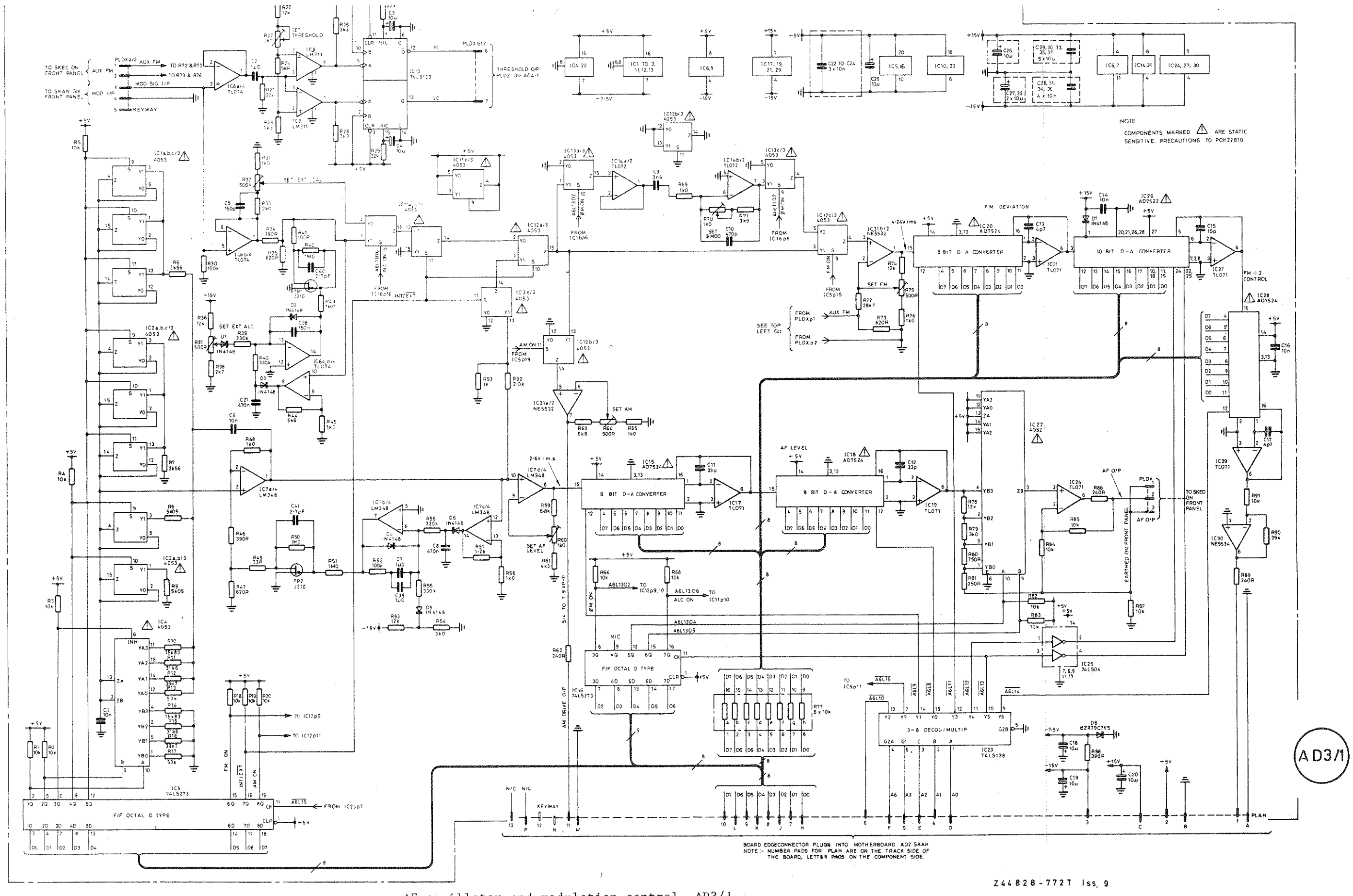

AF oscillator and modulation control, AD3/1

Fig. 25

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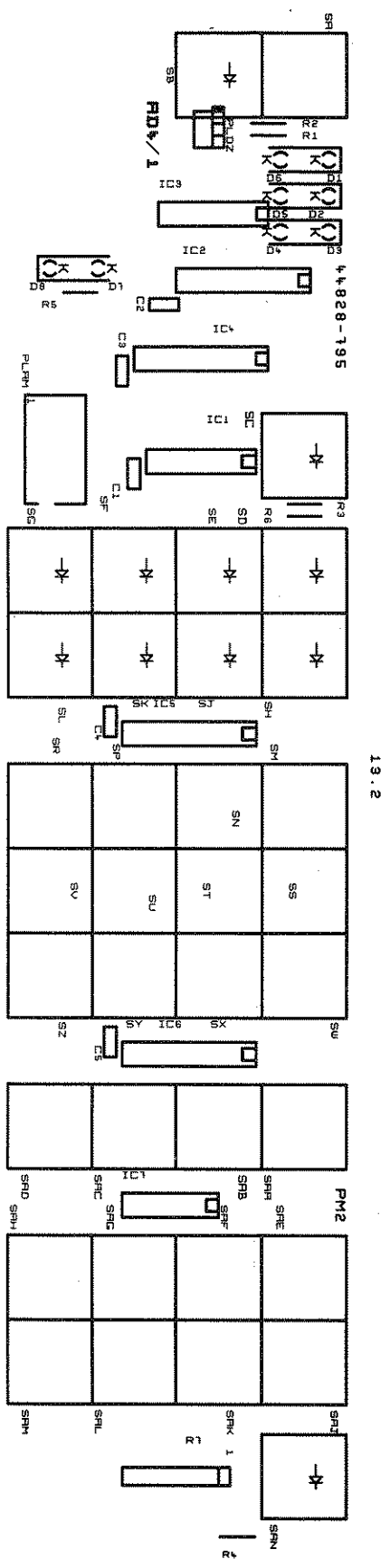

Component layout, AD4/1

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Fig. 26a

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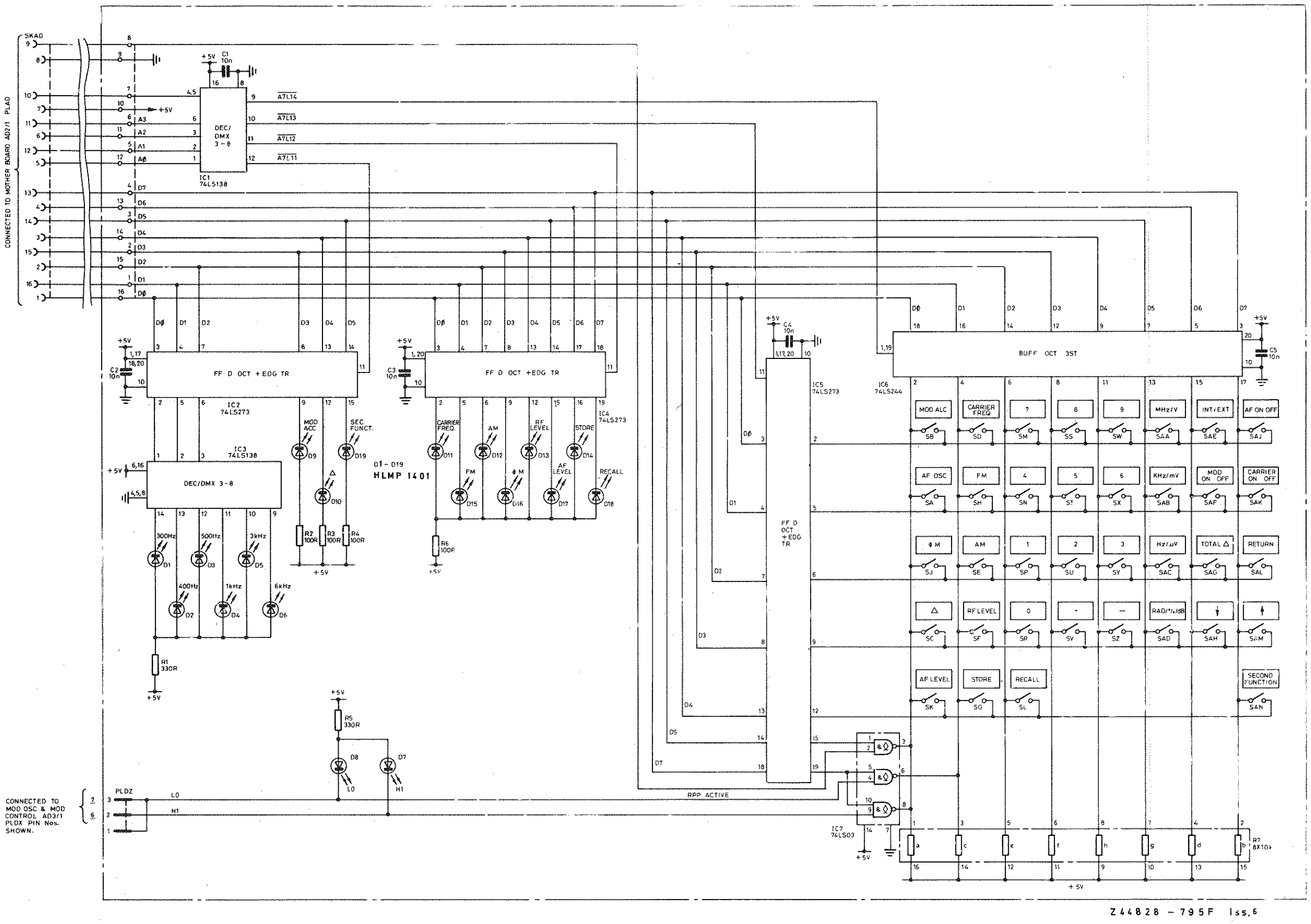
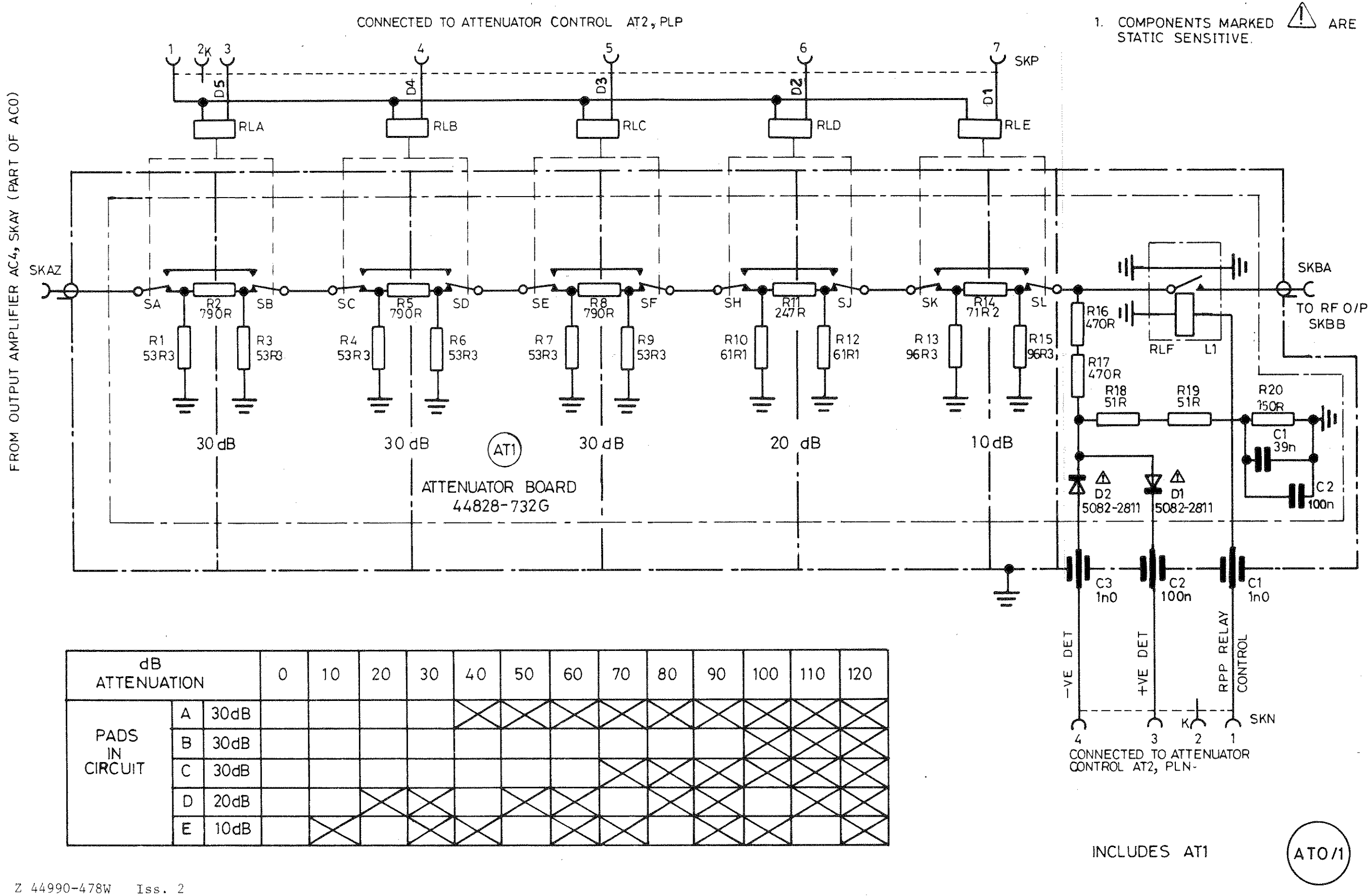


Keyboard, AD4/1



dB ATTENUATION			0	10	20	30	40	50	60	70	80	90	100	110	120
PADS IN CIRCUIT	A	30dB					X	X	X	X	X	X	X	X	X
	B	30dB											X	X	X
	C	30dB								X	X	X	X	X	X
	D	20dB			X	X		X	X		X	X		X	X
	E	10dB		X		X	X		X	X		X	X		X

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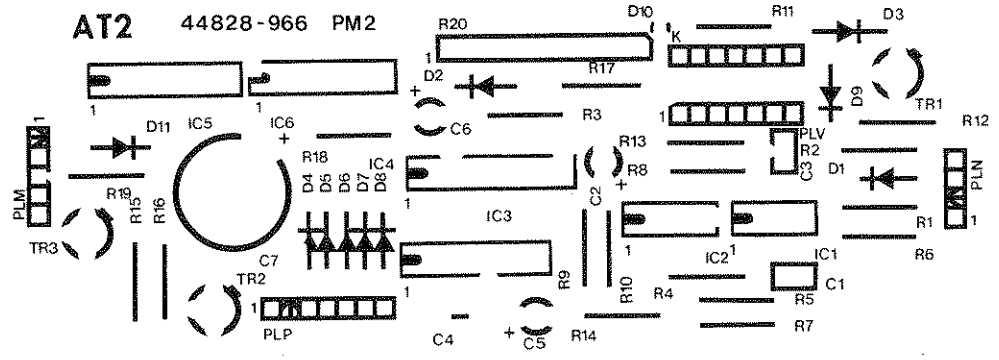
10 dB step attenuator, AT0/1



Component layout, AT2

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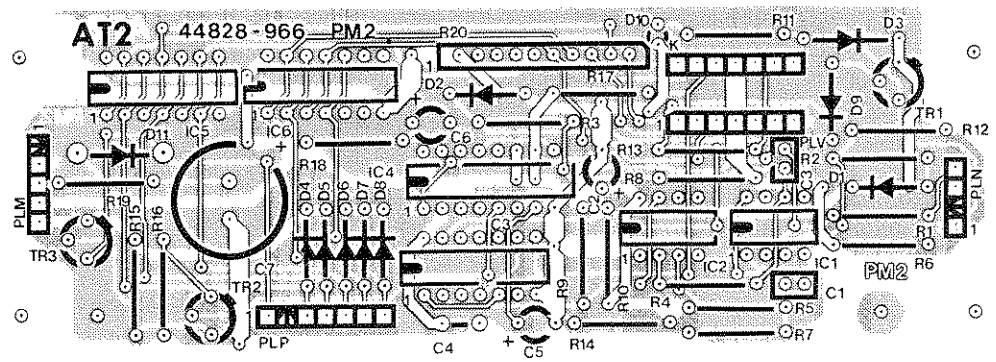

Fig. 28a

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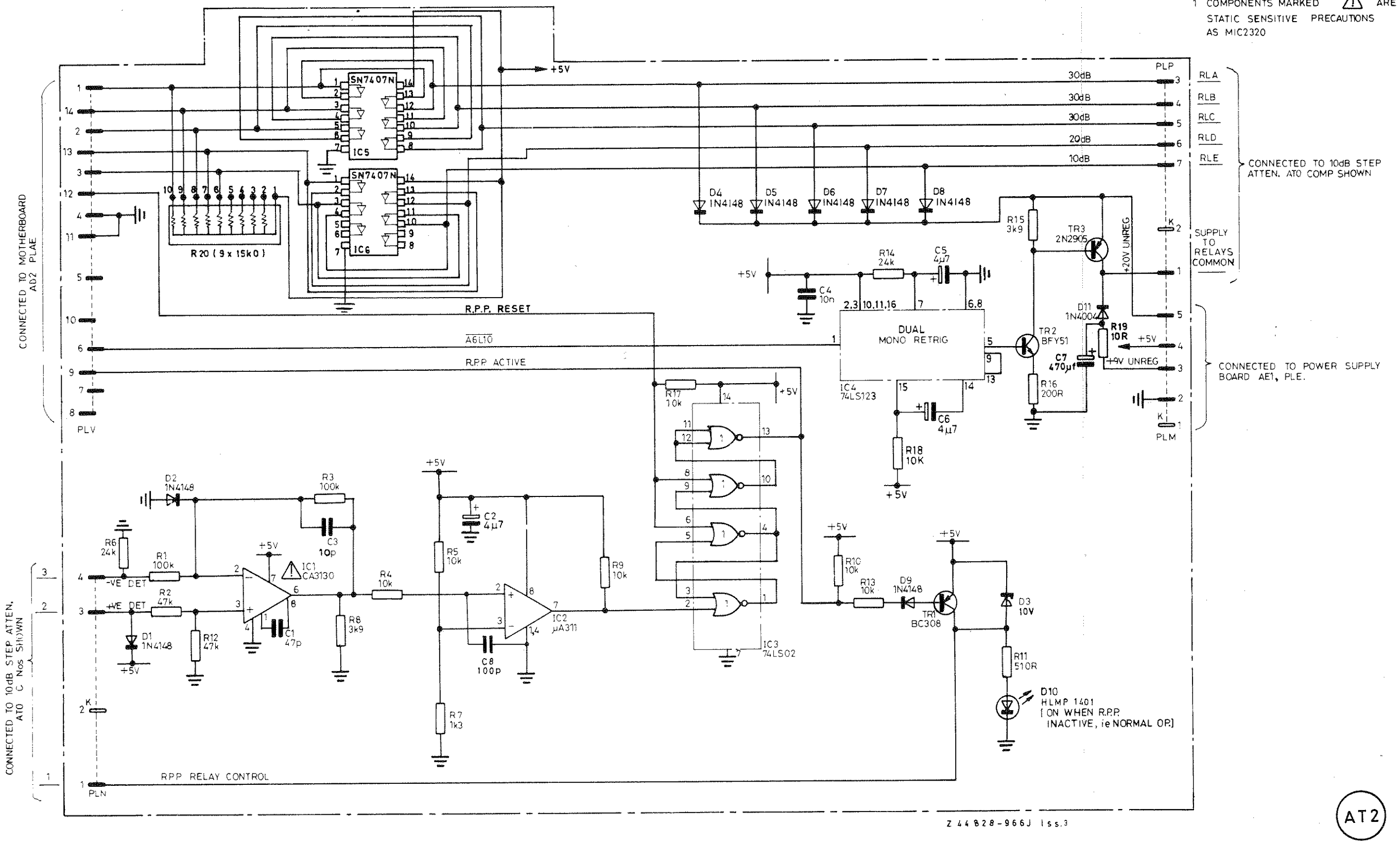

Fig. 28

Attenuator control, AT2

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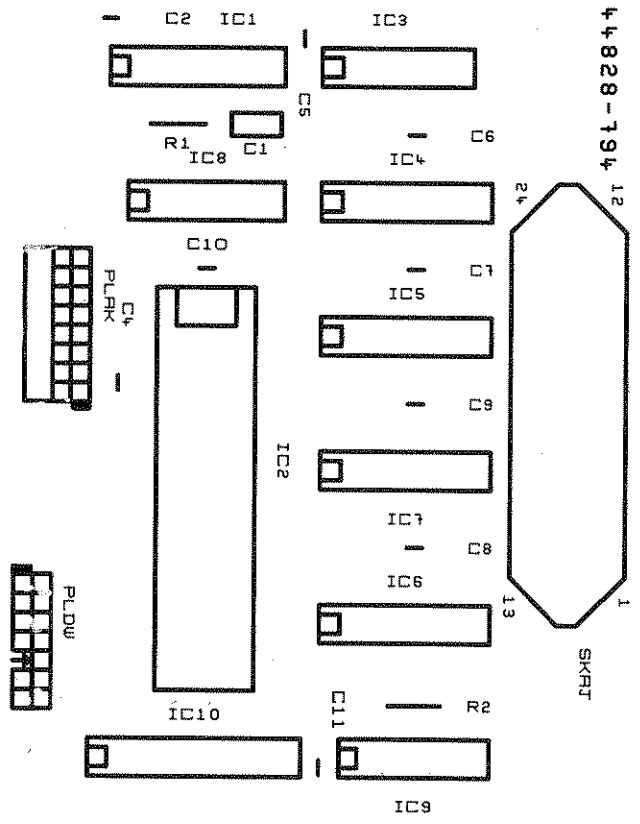

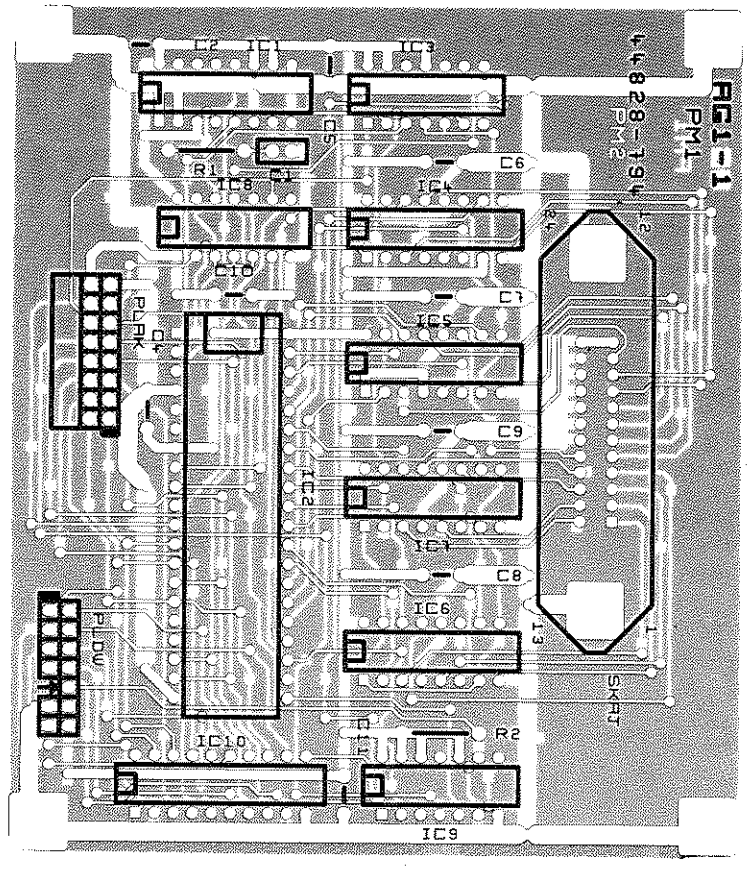

Component layout, AG1/1

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Fig. 29a

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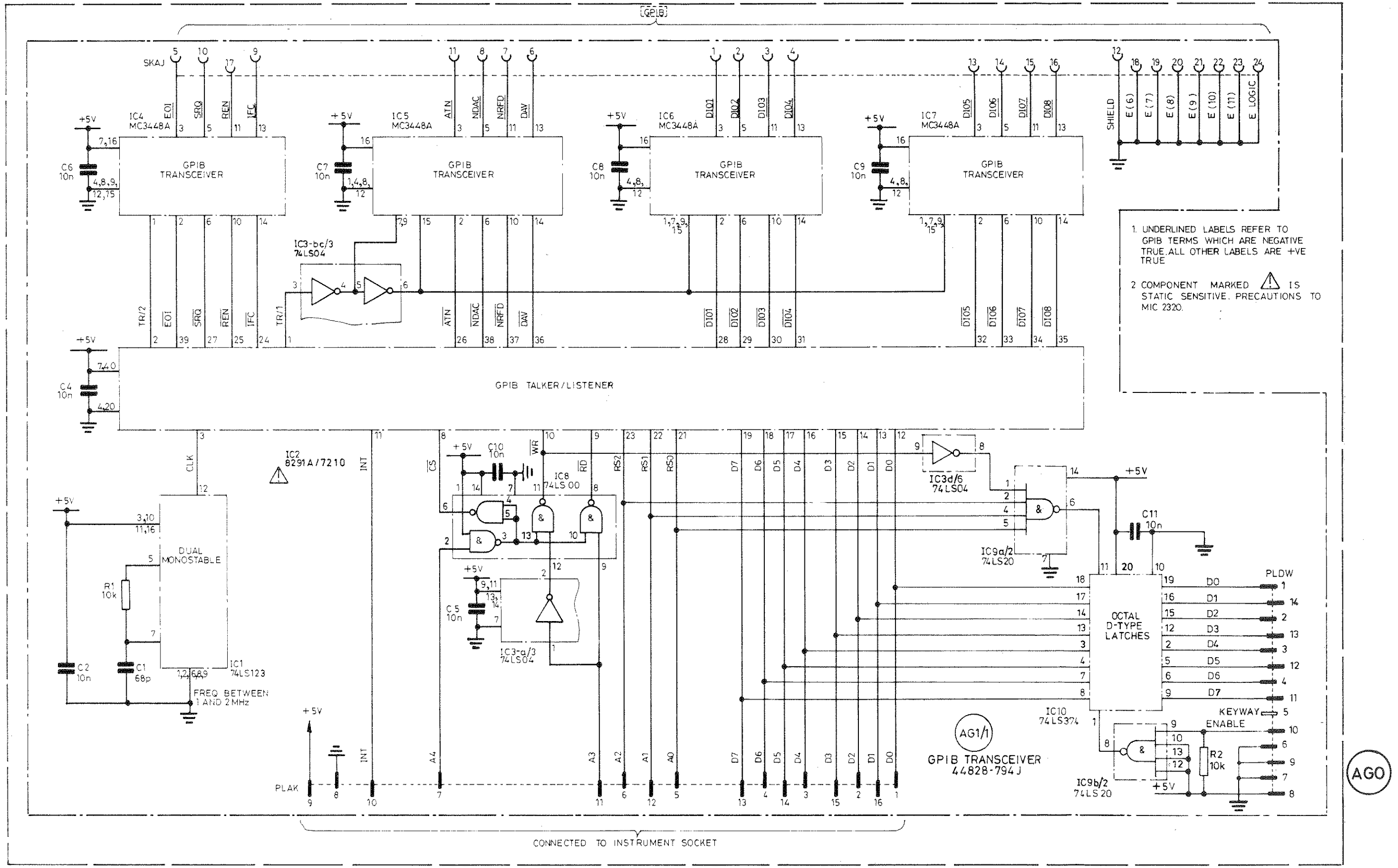

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GPIB adapter module, AG0

Fig. 29

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