DDR4 IBIS Power Integrity Simulation

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Outline

- DDR4 introduction
- Motivation for presentation
- DDR4 IBIS 5.0 model creation
- Power Integrity simulation results
- Conclusions

DDR4 Introduction

- Latest generation of SDRAM memory
  - SDR → DDR1 → DDR2 → DDR3 → DDR4
- 1.2V VDD/VDDQ
- 1600Mbps – 3200Mbps data rates
- Output Drive Impedance – 34, 40, 48 ohms
- DQ bus termination to VDDQ – significant change to signaling versus DDR3
- On-Die Termination is pullup-only to VDDQ
  - RTT_nom has all selections available, 240/(n) where n is 1 to 7 and off. [240, 120, 80, 60, 48, 40, 34]

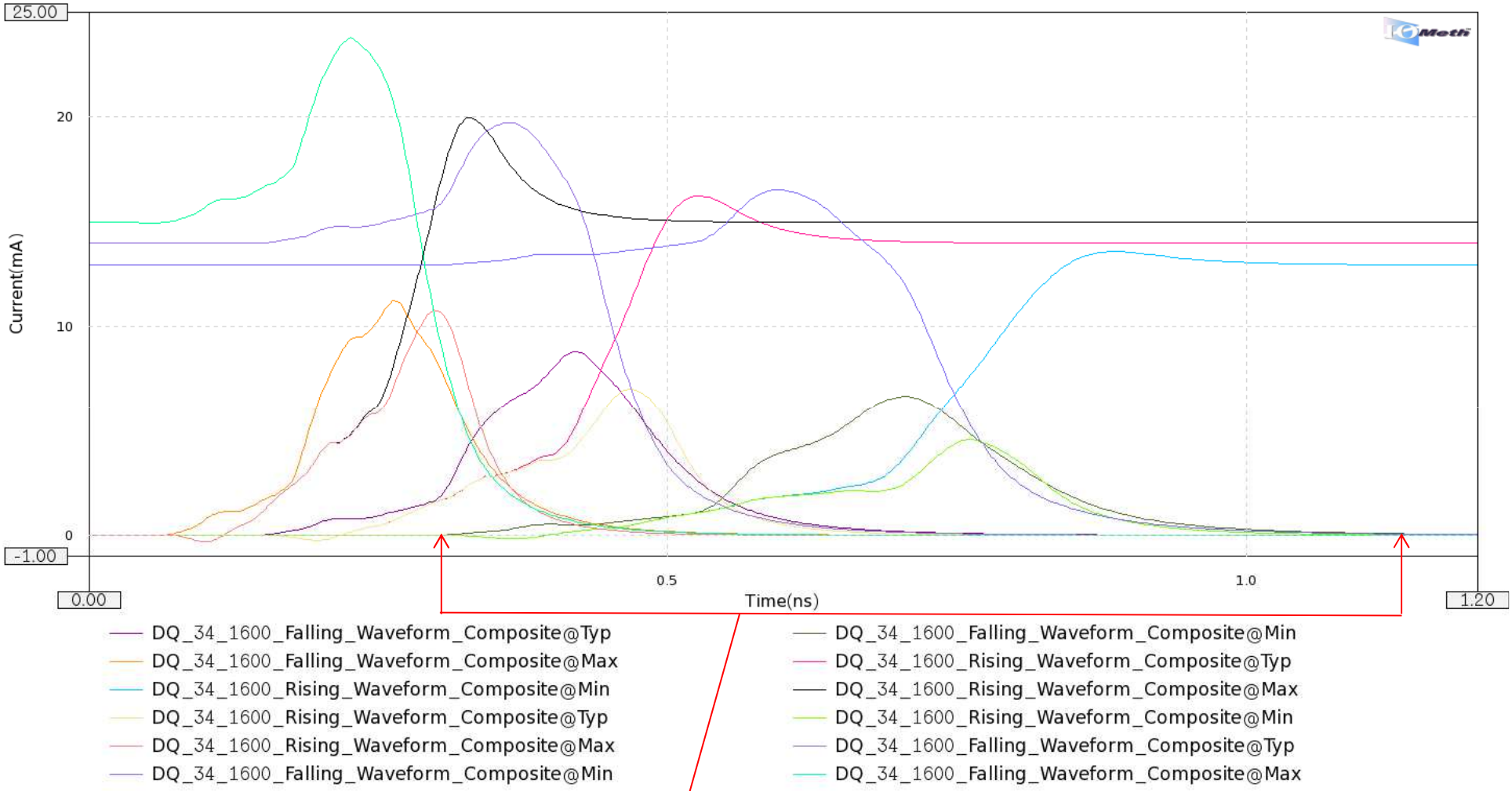
Motivation

- PI capabilities of DDR3-800 models investigated last year
- DDR4-1600+ versus DDR3
  - Higher data rates – overclocking issues?
  - VDDQ terminated bus – do imbalanced VDDQ/VSSQ currents cause any inaccuracies?
  - Different pre-driver characteristics
  - Similar VDDQ/VSSQ decoupling characteristics
- Updated software – how does it handle the new models?

DDR4 IBIS 5.0 Model Creation

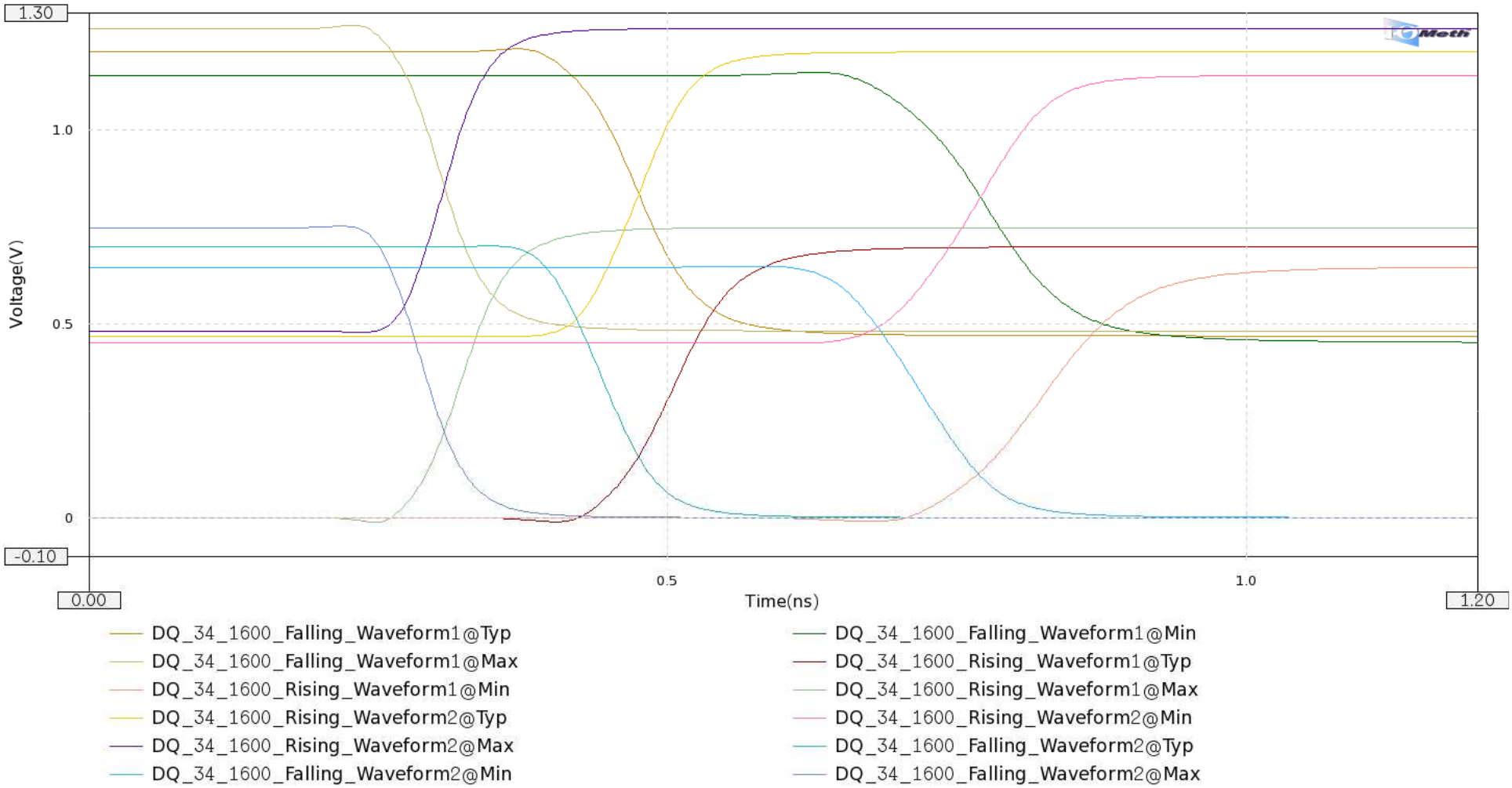
- Automated buffer extraction tool used for quick data extraction
- Extracted I-V, 4 V-t + [Composite Current]s, [ISSO PU] and [ISSO PD]
  - Best-points-fit algorithm applied to all data sets
    - Not critical with 1000 possible data points on V-t and I-t, but what if you need to later downgrade a model to 100 points for IBIS 3.2 compatibility?
    - Critical for data sets with 100 points (I-V)

[Composite Current] Data



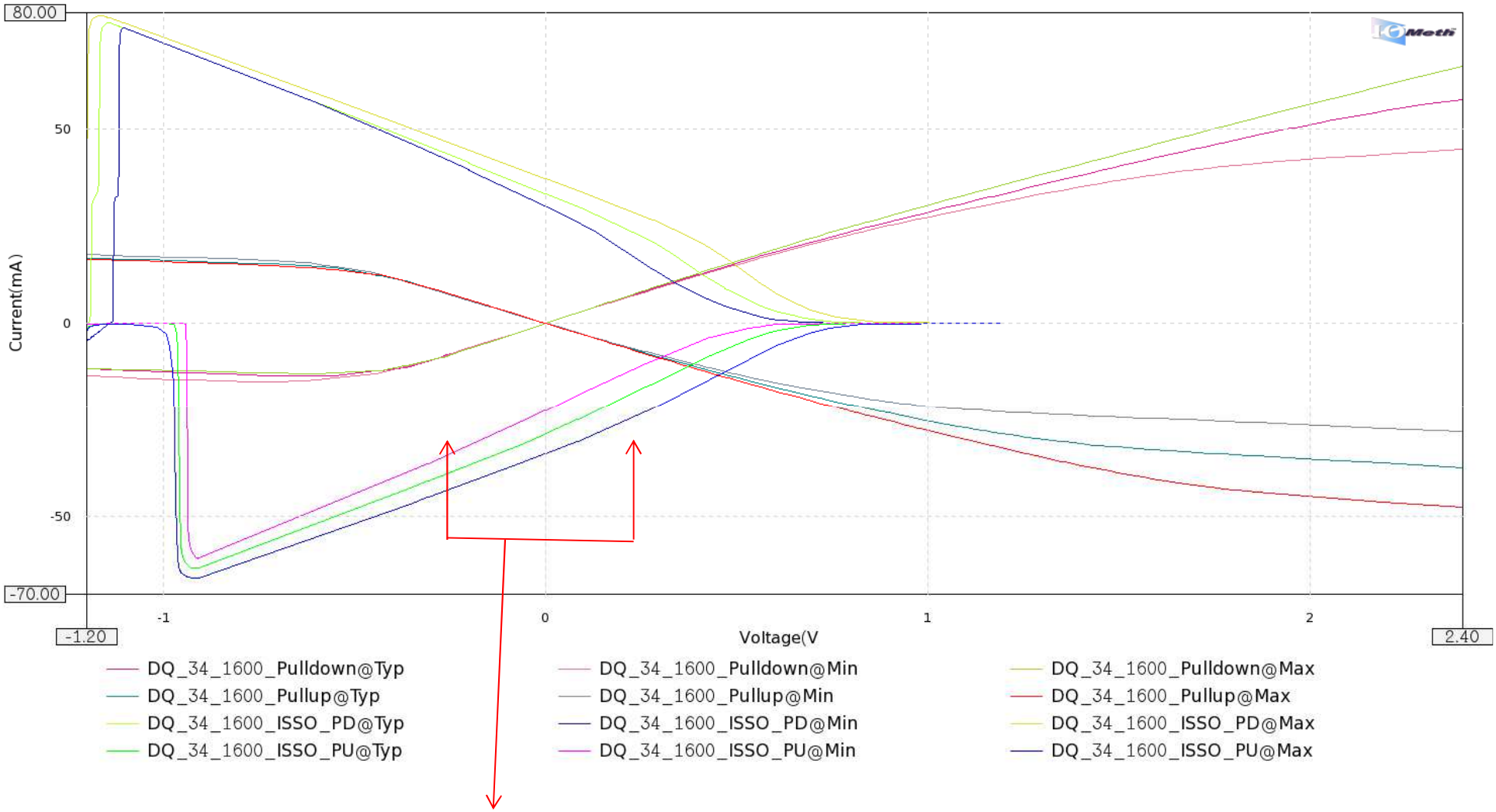
- Note min corner is ~850ps long, bit time is 625ps

V-t Data



- V-t/I-t start/end times match, time points non-correlated

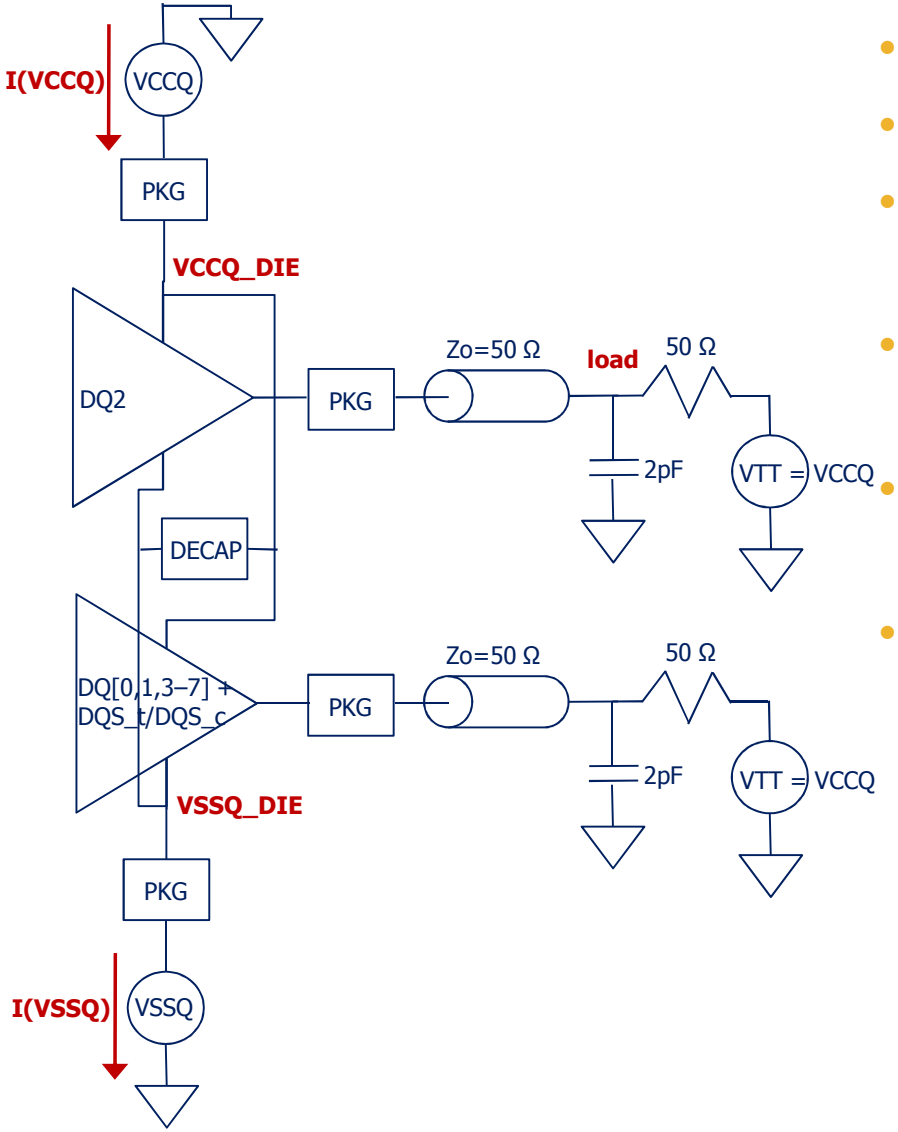
I-V Data – Pullup, Pulldown, ISSO



- ISSO data is very linear in range of Voltage supply swing

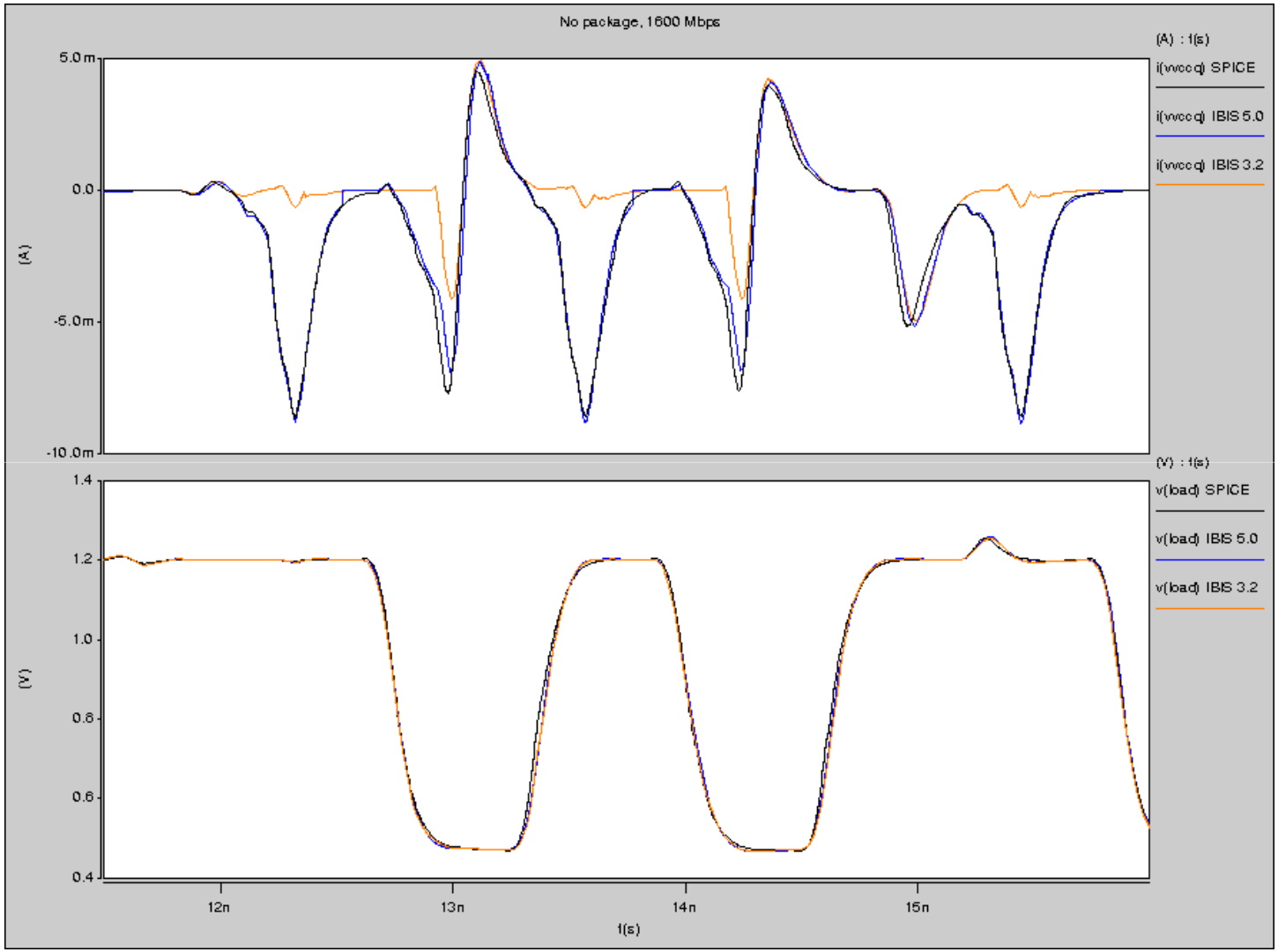
Power Integrity Simulation Results

Simulation Setups



- PRBS pattern, minimum bit width of 625ps.
- Typical corner only.
- On-die decoupling capacitance included as SPICE subckt model
- Sim 1: DQ2 only, no package model
  - Compares IBIS 5.0 directly to SPICE.
- Sim 2: DQ2 only, Lpkg(VSSQ/VSS)=0.15nH, Lpkg(VCCQ)=0.30nH, K=0.2
- Sim 3: DQ[0-7] + DQS_t/DQS_c (DQ2 with different PRBS) with fully coupled SPICE package model
  - Testing real SSO conditions

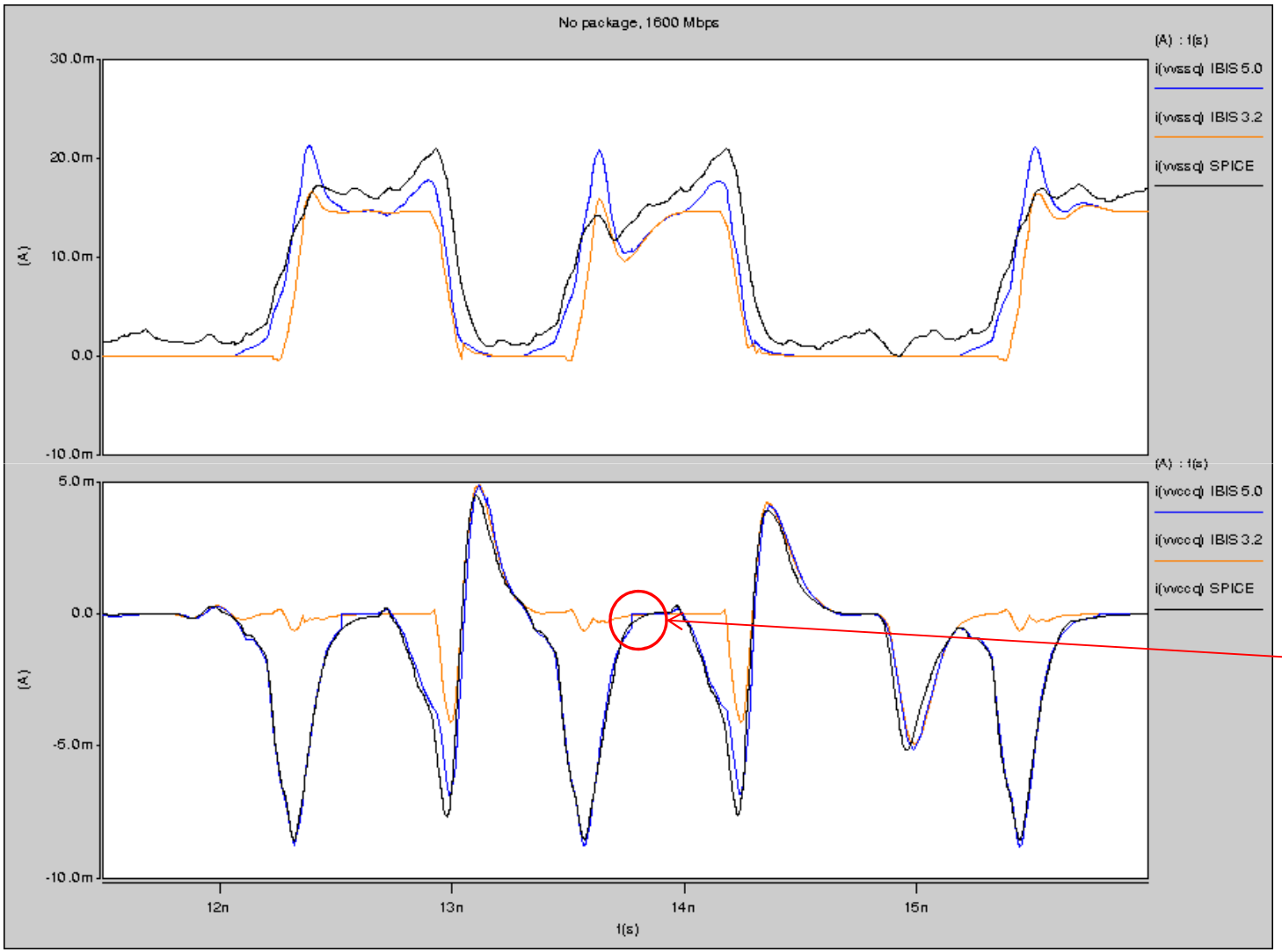
Sim 1, DDR4-1600



VCCQ current matches well.

Significant improvement over IBIS 3.2.

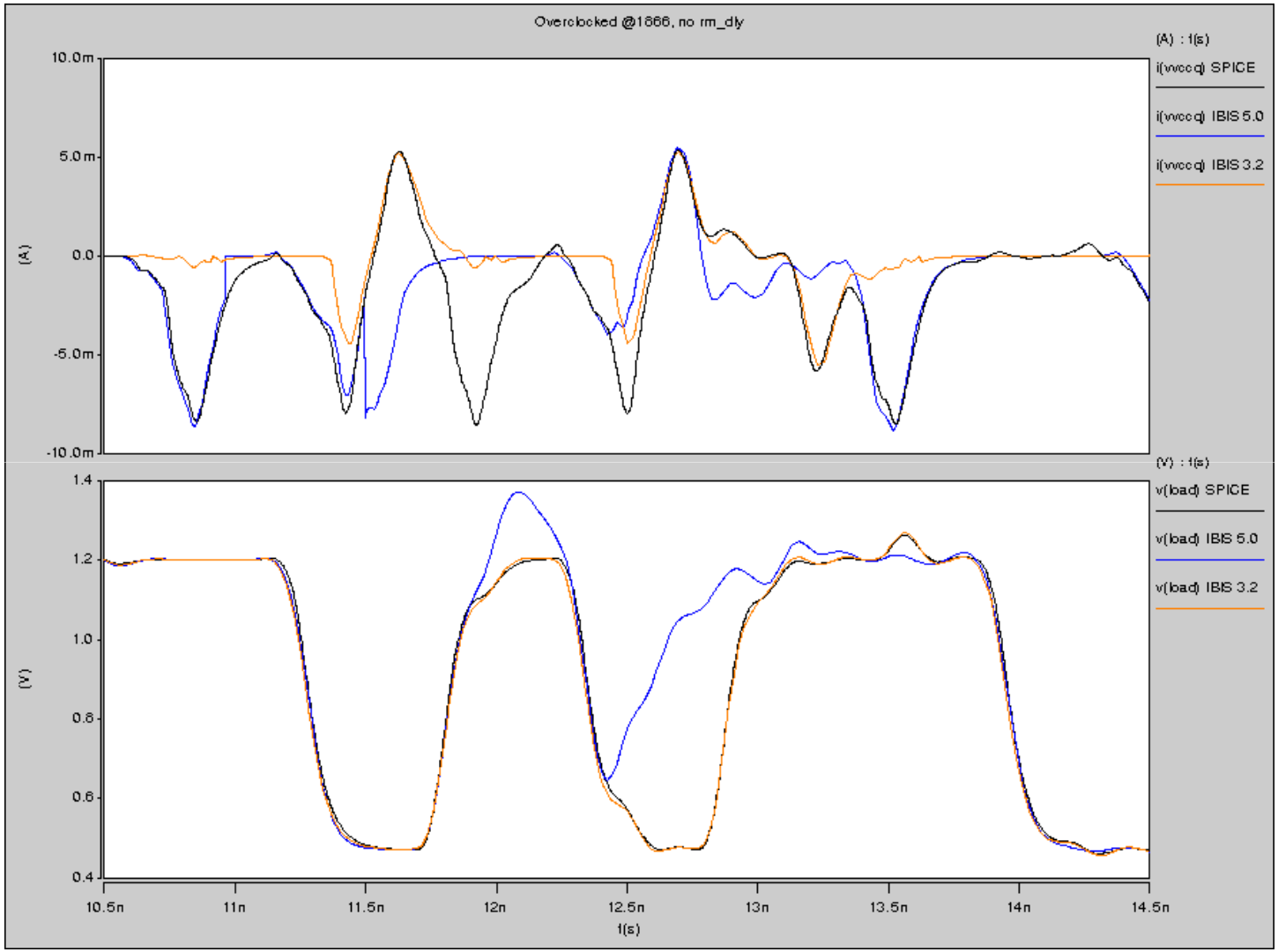
Sim 1, DDR4-1600



VSS/VSSQ shorted on die introduce pre-pre-driver currents that IBIS can't model.

Appears to be a slight overclocking issue in the VCCQ currents. Dead time at end of typical corner V-t curves already chopped.

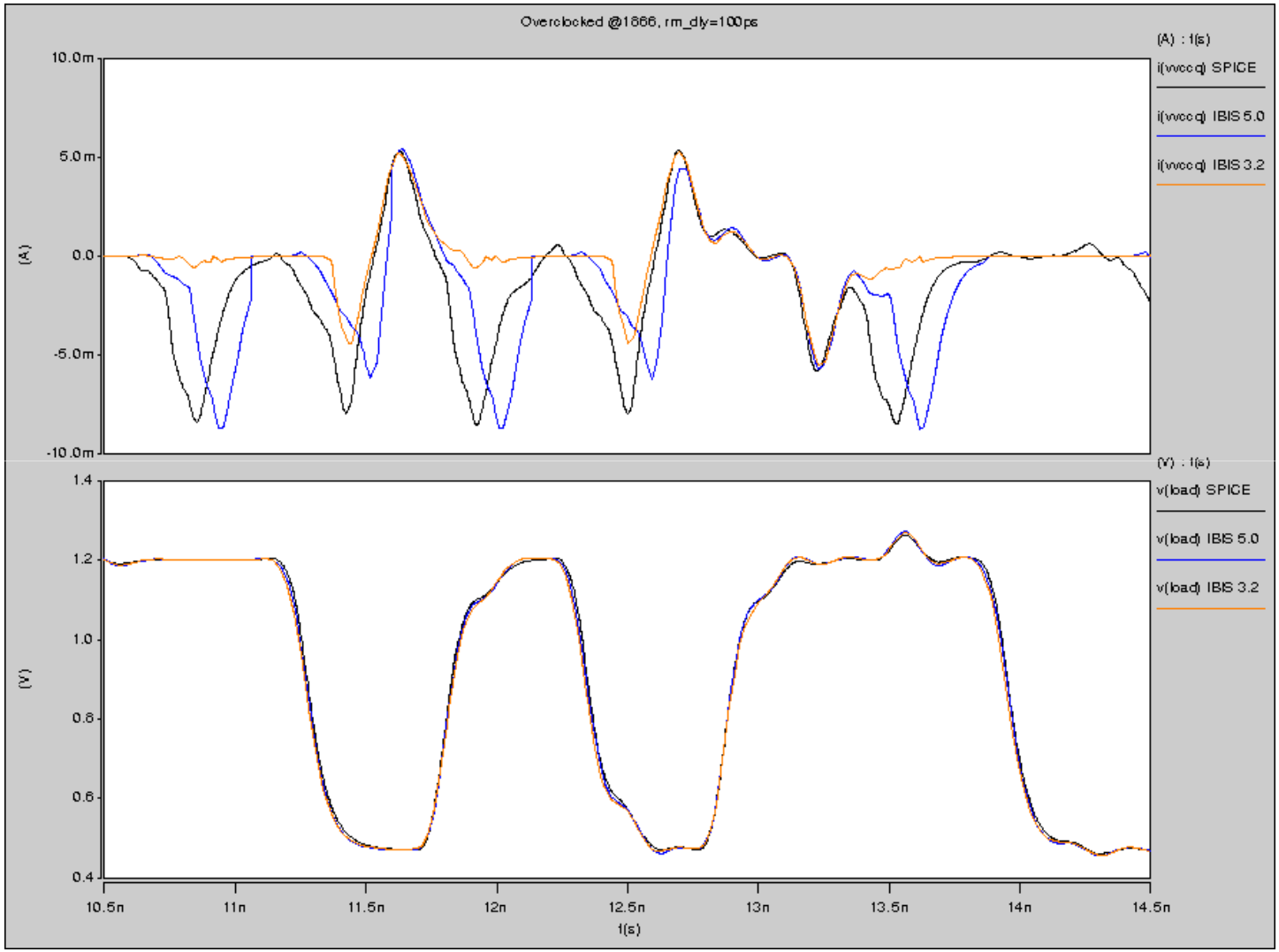
Sim 1, DDR4-1866 (overclocked)



At DDR4-1866, bit time of 536ps causes severe overclocking issues.

V-t waveform is ~750ps long with tail removed. Can still remove ~100ps from start delay. Will this help?

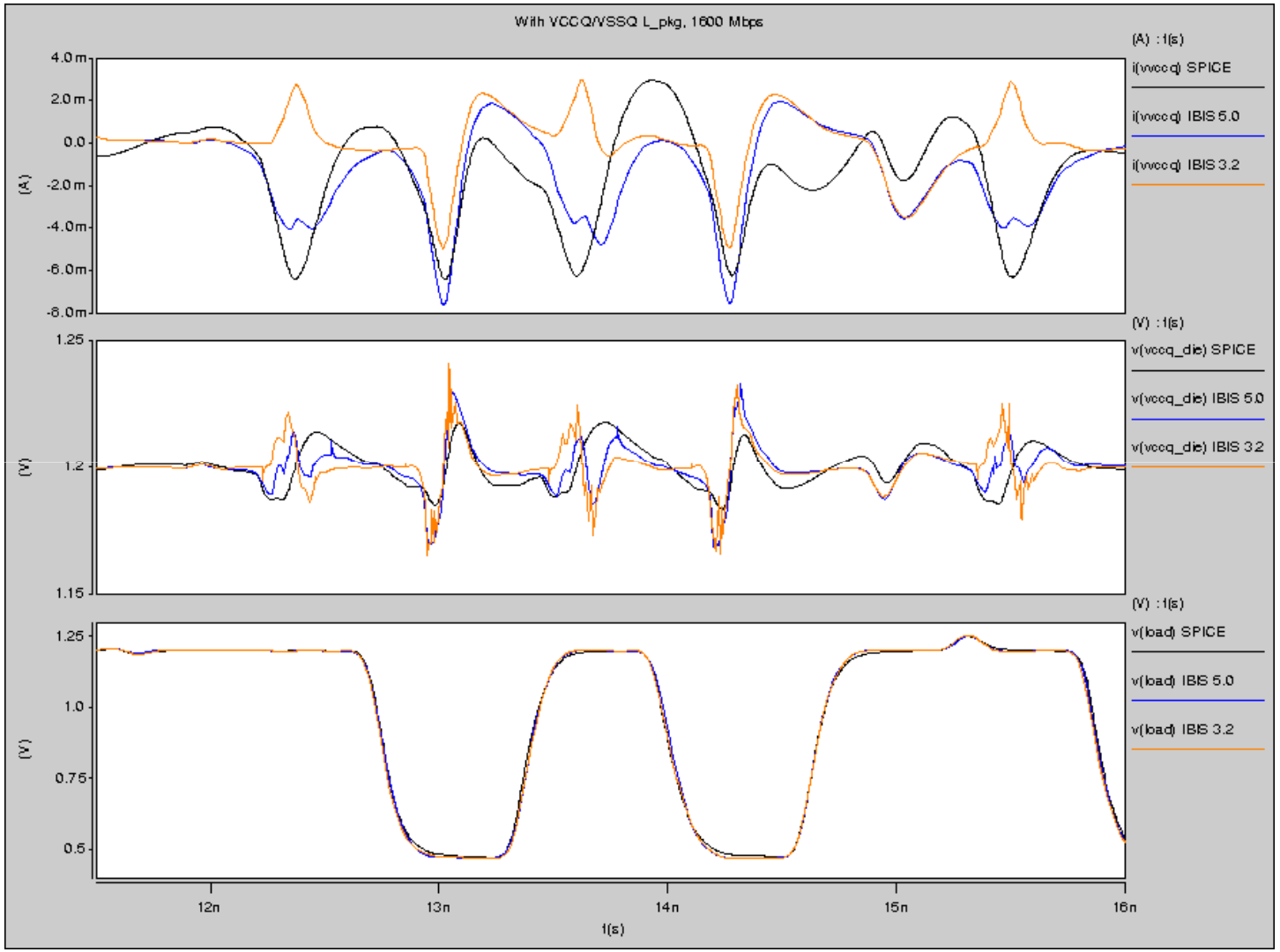
Sim 1, DDR4-1866 (overclocked)



Current wave-form shows overclocking artifacts and is shifted 100ps. Looks like a Bug!

Removing 100ps from initial delay time fixes Voltage waveform at the load.

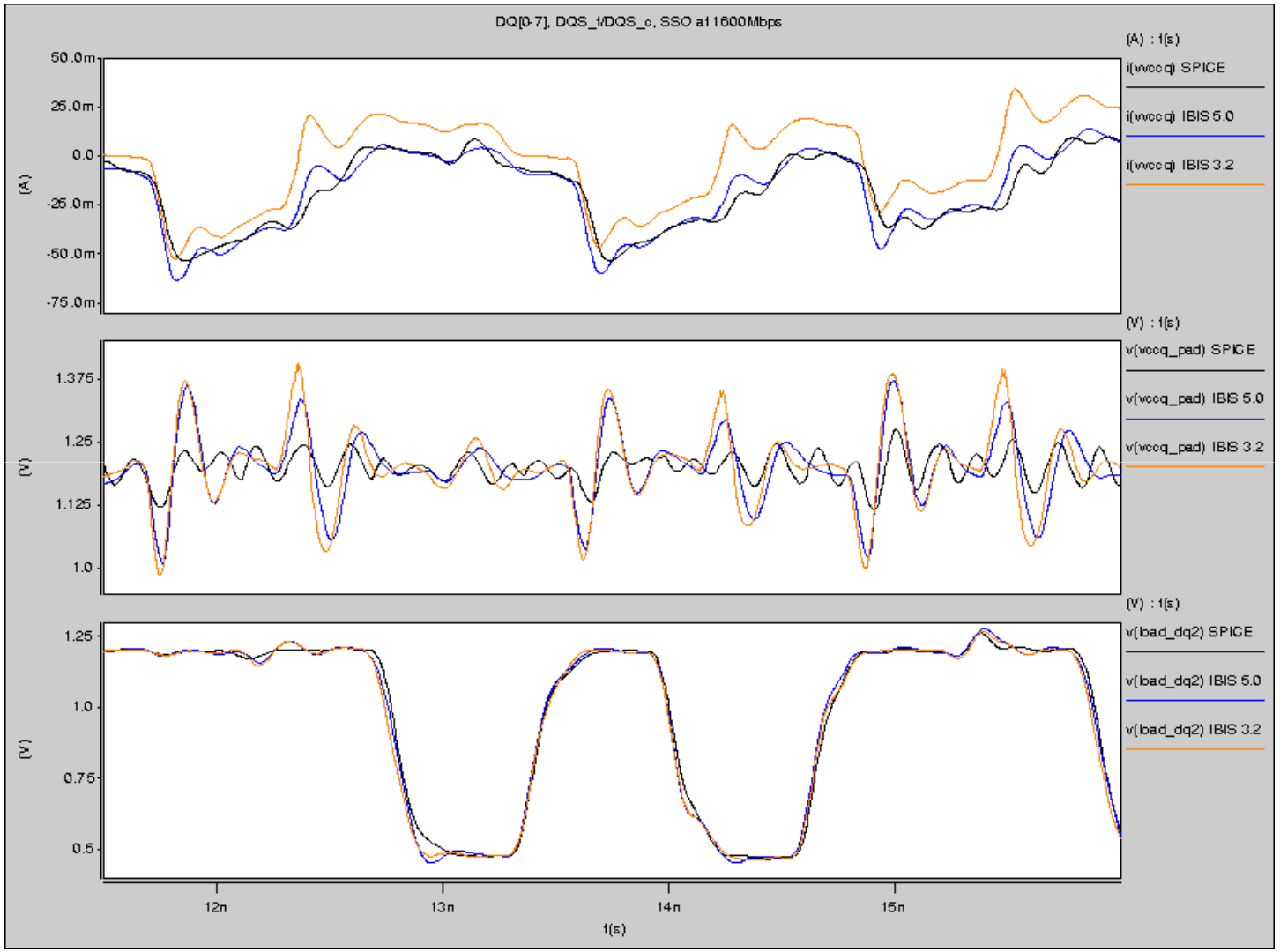
Sim 2, Includes L_pkg



Reasonable correlation between SPICE and IBIS 5.0 models.

More detailed power supply decoupling model might improve results.

Sim 3, Full SSO Simulation



Good VCCQ current correlation between SPICE and IBIS 5.0 models.

VCCQ voltage noise over-estimated.

Slight time delay in SPICE results not modeled in IBIS.

Conclusions

- Overclocking issues with IBIS 5.0 models are a serious concern at 1600Mbps+ data rates.
- DDR4 Power Integrity can be modeled reasonably well with IBIS 5.0.
- Automated IBIS extraction tools for IBIS 5.0 PI data tables will help speed up adoption and prevalence of these models.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