Low-cost, high-signal-quality synthesized-clock generator replaces RF synthesizer in many applications

Stanford Research Systems' $2490 CG635 synthesized-clock generator provides precise, low-jitter digital-clock signals for applications ranging from digital-circuit design to communications-network testing. You can set the clock frequency from 0.001 Hz to 2.05 GHz. Rise and fall times are as short as 100 psec. Jitter is less than 1 psec rms. At 622.08 MHz, phase noise at a 100-Hz offset is below a −80-dBc/Hz level, and the spurious response is below a −70-dBc level. Using the optional 10-MHz rubidium timebase, aging is less than 0.0005 ppm/year, and temperature instability is less than 0.0001 ppm.

You can set the CG635 outputs to standard logic levels, including CMOS, ECL (emitter-coupled logic), PECL (positive ECL), and LVDS (low-voltage differential signaling). You can also continuously adjust offset and amplitude between −5 and 5V. A rear-panel output delivers clocks at RS-485 and LVDS levels over twisted pairs. An optional PRBS (pseudorandom-binary-sequence) generator provides clock and data outputs at LVDS levels for testing serial-data channels. Edge-transition times are typically 80 psec.

The CG635's standard crystal-oscillator timebase provides sufficient accuracy for many applications. To improve frequency stability and reduce aging, you can add an optional oven-stabilized crystal oscillator or rubidium frequency standard. You can also lock the CG635 to an external 10-MHz timebase.

Compared with a typical RF synthesizer, the CG635 has many similarities: excellent frequency resolution, low phase noise, and low spurious output levels. The new generator offers several advantages, however: output frequencies as low as 0.001 Hz, multiple square-wave outputs to 2.05 GHz, and much lower cost.

The CG635 synthesized-clock generator produces extremely clean, low-jitter clock signals over a frequency range of 0.001 Hz to 2.05 GHz. The cost is a fraction of that of RF synthesizers, which, until now, have been the only type of instrument suitable for producing many of the clock signals the new generator produces.

The optional clock-receiver modules, which connect to the CG635 via Category 6 cable and may be a substantial distance from the instrument, provide complementary high-speed transitions at standard logic levels on SMA connectors.—by Dan Strassberg

▶**Stanford Research Systems**, 1-408-744-9040, www.thinksrs.com.

Quad processors power new DSP board

Curtiss-Wright Controls Embedded Computing recently announced the Compact Champ-AV IV, a high-performance CompactPCI DSP board that derives its power from four Freescale (www.freescale.com) MPC7448 PowerPC processors. The board complies with the CompactPCI packet-switching-backplane specification and provides DSP applications with as much as 48 GFLOPS of peak computational power. Each of the board's four processing nodes comprises a 1.5-GHz 7448 processor; 256 or 512 Mbytes of DDR-250 SDRAM; dual 100-MHz, 64-bit PCI-X interfaces; and a Gigabit Ethernet connection. Each node transfers data to adjacent nodes at speeds as high as 1.6 Gbytes/sec. Both PMC sites on the Compact Champ-AV IV support low-voltage differential signaling to the backplane connectors, enabling serial switched interconnections, such as StarLink and FibreChannel.

The Compact Champ-AV IV delivers as much as 48 GFLOPS of peak computational power for advanced DSP applications.

Operating-system support for the Champ-AV IV includes Wind River (www.windriver.com) VxWorks/Tornado. A Linux package will be available by midyear. The Compact Champ-AV IV is available in a commercial-temperature, air-cooled configuration with prices starting at $14,900.—by Warren Webb

▶**Curtiss-Wright Controls Embedded Computing**, www.cwcembedded.com.

▶**According to IDC (www.idc.com), the worldwide storage-software market grew 15% year over year to $2.2 billion in the fourth quarter of 2004. For the full year 2004, storage-software revenue grew 16.1% year over year to $7.9 billion, injecting more than $1 billion of new revenue into the market.**