Model SC-10
10 MHz Ovenized Oscillator

1290-D Reamwood Avenue, Sunnyvale, CA 94089
Revision 1.0 (4/95)

SC10 High Stability Ovenized Quartz Oscillator

The device is a 10 MHz sine oscillator with very low phase noise. The circuit was designed for 3rd overtone 10 MHz stress compensated (SC) crystals. SC cut crystals are used for their low phase noise, low vibration sensitivity, and improved stability against ambient temperature changes.

SC-10 Specifications

Grade		**J**	**K**	**A**
Frequency			10 MHz	
Aging		<1E-9/day	<5E-10/day	<2E-10/day
Allan (1s)		<1E-11	<5E-12	<2E-12
Phase Noise	10Hz	<-120dBc/Hz	<-125dBc/Hz	<-130dBc/Hz
	100Hz		<-150dBc	
	1kHz		<-155dBc	
	10kHz		<-155dBc	
Stability (0 to 50°C)		<±2E-9	< ±1E-9	< ±5E-10
Operating Temp.		0 to 50°C	-10 to +60°C	-20 to +70°C
EFC Range		Standard: 0 to 10 V, +5 nom. Other ranges are available.		
EFC Slope		Standard: +0.5 Hz/V. A negative EFC slope is available.		
Mechanical Tune		+/-3Hz (Nominal)		
Output Level		+13±0.5dBm into 50Ω (≈1Vrms or 2.88Vpp)		
Output Waveform		Sine. Harmonics: 2ω<-45dBc. 3ω and up<-60dBc		
Supply Voltage		+15Vdc or +24Vdc per P/N		
Power		8W warm-up, 3.0W @25°C		
		(Warm-up current may be modified by resistor substitution.)		

Note: The temperature stability specification is derated by 2x between -10°C and 0°C and between +50°C and +60°C. The temperature stability specification is derated by 4x between -20°C and -10°C and between +60°C and +70°C.

Part Number

The part number for the 10MHz SC-cut oven stabilized oscillator is:

SC-10-VS-E-T-S-N-A-CON

where,

VS is **15** for +15Vdc or **24** for +24Vdc supply voltage
E specifies the EFC characteristic (range and slope)
1 for 0 to +10V, 5V nominal, +0.5Hz/V (Standard value)
2 for 0 to +10V, 5V nominal, -0.5Hz/V.
3 for -10 to +10, 0V nominal, +0.25Hz/V
4 for -10 to +10, 0V nominal, -0.25Hz/V
5 for -5 to +5V, 0V nominal, +0.5Hz/V.
6 for -5 to +5V, 0V nominal, -0.5Hz/V.
7 for 0 to +6V, 3V nominal, +0.75Hz/V.
8 for 0 to +6V, 3V nominal, -0.75Hz/V.

T is **J**, **K**, or **A** per the required temperature range
S is **J**, **K**, or **A** per the required stability vs. ambient temperature
N is **J**, **K**, or **A** per the required noise level (both Allan variance and phase noise)
A is **J**, **K**, or **A** per the required daily aging rate
CON is **PIN**, **SMA**, **SMB** or **SMC** for pin, SMA, SMB, or SMC 10MHz connector.

Example: SC-10-15-1-J-J-J-A-SMA is a unit which operates from +15Vdc, has the standard EFC slope and range, has the lowest daily aging specification (2E-10/day), and an SMA rf connector for the 10MHz.

Connector pin-out:	Pin number	Function
	1	+15 or +24 V per P/N
	2	Power ground
	3	10 MHz output
	4	10 MHz ground
	5	+10.00Vdc reference output
	6	EFC ground reference
	7	EFC input

Application Suggestions

All grounds (power, RF, EFC, and case) are connected together at a single point inside the SC10. To avoid ground loops you should provide power to the SC10 from a floating supply, ground the case to your chassis ground via the unit's four standoffs, and "look" differentially at the 10MHz RF output.

EFC (electronic frequency control) potentials should be referenced to the EFC ground pin (pin 7). Noise or pickup on the EFC line will frequency modulate the SC10, degrading phase noise and adding spurs.

Avoid fans, vibration, and ac magnetic fields near the SC10.

The SC10 will reach a steady-state aging rate after about 72 hours of continuous operation. The phase noise of the unit will also require about 72 hours to reach its final value. The frequency hysterisis of a complete cool-down and warm-up cycle will be about ±20 mHz.

Operate the unit for at least 24 hours before adjusting the frequency (via the pot under the screw in the top of the case) to 10.000MHz. Also, be certain to apply the nominal EFC voltage to pin 7 before adjusting the frequency:

EFC Option	Nominal Pin 7 Voltage
1 & 2	+5.00 Vdc or open circuit
3,4,5 or 6	0 Vdc or short pin 6 to pin 7
7 & 8	+3.00 Vdc or 182kΩ between pin 6 and pin 7

The EFC input exhibits a single-pole RC type response with a -3dB point of about 3kHz when driven by a voltage source with an output impedance of 1kΩ or less. This response may be important to consider when phase locking the SC10 to another source via the EFC input.

The 10MHz output has a dc resistance of about 0.1Ω and is intended to drive a 50Ω load. The output level is +13.0dBm, or about 1Vrms or about 2.88Vpp.

Circuit Description (Rev L December 1994)

Power Supplies

The unit runs from a single +15 Vdc or +24Vdc supply. An AD587 voltage reference, U1, provides an accurate, low noise +10.00 Vdc reference for the oscillator, amplitude and temperature control circuits, and a +12 V regulator is used for the output amplifier circuit.

Temperature Controller

The turn-over temperature of a crystal is the temperature at which the frequency of oscillation is at a local maximum, hence the derivative of the frequency vs temperature is zero. A temperature controller is used to maintain the temperature of the block at the turnover temperature.

Three ICs in TO92 packages are used to sense temperature. U5,6 and 7 are LM34s, precision Fahrenheit temperature sensors, which output 10mV/°F. U6 and U7 are located inside the block, directly on the tabs of the TO-220 packages (U3 and U4) which heat the block, and U5 is located outside the block, near the top of the unit, to sense the case temperature.

There is a temperature offset between the TO220 heaters (where the temperature is sensed) and the block. This is because of the finite thermal conductivity the TO220 packages and the heat flow through them. (The temperature control loop would be unstable unless the sensors are placed directly on the heaters.) The magnitude of this offset depends on the case temperature: if the case temperature is low, so that a lot of heat is required to maintain the block at the turnover temperature, the temperature offset will be large. If the control loop were to maintain the U6&7 at a fixed voltage, the block temperature would decrease as the case temperature decreased. To overcome this problem, a small fraction of the case sensor voltage is summed with the block sensor voltage, so that as the case temperature drops the control loop is satisfied only when the block sensors are slightly above the set point.

The crystals have a specified turning point between 65 and 80°C (149 to 176°F) so the output of the U6&7 will be between 1.49 and 1.76 Vdc at the desired temperature.

A proportional/integral controller is used to maintain the temperature of the block at the set point. The weighted sum of the outputs of the three LM34s are compared to the set-point by U2A, 1/2 of an AD822 dual op-amp. If the temperature is below the set-point, the output of the op-amp slews high (with a time constant set by R4,5&6 and C4), to increase the current in the heater/regulators, U3 and U4.

The heating elements U3 and U4 are voltage regulators in TO-220 packages. U3 is an LM7808, a positive +8Vdc regulator (or an LM7812 in the case of a +24Vdc supply). U4 is an LM337, an adjustable negative voltage regulator. The tabs on both regulators are grounded to the block. The op-amp U2B controls the adjustable regulator to maintain a current through the shunt resistors (R8 and R13) which is proportional to the error signal from the proportional/integral amplifier.

Each regulator has its own thermal protection circuit internal to the device. In the event of control loop failure, each regulator would limit its current so that the junction temperature will not exceed 150°C. The regulators may pass a current from 0 to 500 mA in the +15V supply case, or 0 to 320mA in the +24V supply case, dissipating 0 to 7.5W as heat into the block. The maximum power dissipated in the shunt resistor is 150mW.

The set-point temperature is determined by the voltage applied to R1, which is offset and divided by R2 and R3 . During calibration, an external voltage applied to pin 5 of the interface connector is used to adjust the set point to determine the turnover temperature. Before shipping, the jumper JP2 is moved from 2&3 to 3&4, and P1 is set to the voltage corresponding to the turnover temperature. A second jumper on JP2 between 1&2 provides +10.00Vref to pin 5 of the interface connector to serve as a reference or an external EFC divider circuit.

Oscillator

In this circuit, the transistor Q1 is the active component of the oscillator. Q3 and Q4 form a transimpedance amplifier, converting the crystal current (at 10 MHz) to a voltage. Q2 is an AGC (automatic gain control) amplifier, providing just the right amount of base current to Q1 in order to sustain the oscillation.

Oscillation in the crystal is maintained by power added by transistor Q1. The energy added by Q1 on each cycle must exactly match the energy lost in each cycle in order to maintain the oscillation at constant amplitude. Q1's gain is controlled by adjusting its emitter current: the higher the current, the higher the gain.

The oscillator uses a Colpitts configuration. To see this, realize that one side of the crystal is connected to an ac ground (the emitter of Q3) via a net series capacitance. At 10 MHz, the series LC circuit C13 and L1 has a net capacitive reactance, as does the parallel tank circuit, C14 and L2. These tank circuits prevent oscillation at frequencies other than 10 MHz (the fundamental, lower overtones, or B mode frequencies). For the circuit to oscillate, both tanks must have like signs to their reactance, ie., both must have net capacitive or inductive reactance. Above its series resonance at 10.7 MHz the C13/L1 tank is inductive. Below its parallel resonance at 6.5 MHz the C14/L2 tank is inductive.

At 10 MHz, the tank formed by C13 and L1 has the reactance of a 1650 pF capacitor (-j9.6 Ohms), and the C14/L2 tank has the reactance of a 76 pF capacitor (-j208 Ohms). All of the crystal current flows through these reactances. The voltage across the C14/L2 tank is about 20 times the voltage across the C13/L1 tank. The transistor Q4 will add energy to the tank if the emitter ac voltage is greater than .95 times the base ac voltage, which occurs at a emitter bias of about 1 mA.

As the C13/L1 tank is very near series resonance at 10MHz, the tuning of this tank will have a large impact on the tank reactance, hence on the emitter current required by Q1 to sustain the oscillation. When the inductor (L1) is turned completely clockwise (all the way in, so as the maximize the inductance value) the tank's reactance becomes very small, and Q1 cannot provide sufficient gain to sustain oscillation. At this point, the AGC amplifier (Q2) will be completely off, and the collector current in Q1 will be limited by the base current through R17, and by Q1's beta (about 5 mA). As L1 is reduced (by turning counter-clockwise) the circuit will begin to oscillate. L1 controls the amplitude of the output, and should be set so that the output is +13dBm (1Vrms) into 50Ω. With 1Vrms at the output, there will be about 4Vdc at J1, the AGC test point.

Tuning of the other tank (C14/L2) is less critical. At initial calibration the variable inductor, L2, is set about 2 turns counter-clockwise from full-in.

The crystal has a load of about 20 pF, which consists of the series combination of the tank reactances, C8, C9 (selected), the tuning varactors, and C11. Nominally, C9 will be a capacitor in the range of 33-1000pF. With the frequency adjust pot (P2) near the middle position (so that there is +6Vdc at the test point J3) a small inductive or capacitive reactance will be selected for C9 to compensate for unit-to-unit variations in crystal frequency.

In order to oscillate, the crystal will operate just above series resonance, to provide an inductive reactance. This reactance resonates with the load capacitance of 20 pF at a nominal value of 10.000000 MHz. The crystal frequency may be tuned by changing the load reactance from the nominal 20 pF: increasing the load capacitance will lower the frequency of operation. Selecting a large capacitor for C9 will increase the frequency a little bit (compared to a short circuit for C9), selecting a small capacitor for C9 will increase the frequency a lot. An inductor may be selected for C9 to lower the frequency: the larger the inductor, the lower the frequency.

The net reactance in series with the crystal may be tuned by changing the voltage on the dual varactor D1, an MMBV432L. The control voltage to the cathode of this diode has a nominal value of +5.00 Vdc, and may vary from 4.0 to 6.0Vdc with a control voltage from 0 to 10Vdc on the external EFC input. The bias on the other side of the varactor is controlled by the frequency adjust pot, P2, and has a nominal value of 2Vdc, and may be set from 0 to 4Vdc. The voltage tuning characteristic is positive and linear to about 10%. The magnitude of the tuning coefficient depends on the crystal type: for a 10 MHz 3rd OT SC it is about 0.2 Hz/V.

The tuning circuit has been designed to accommodate negative EFC coefficients. For negative EFCs (the frequency goes down when the EFC voltage goes up) D1 is removed and D2 is installed, and R26 is removed and R25 is installed. EFC ranges other than 0-10Vdc are accommodated with different values of R42, R23 and R27.

Power dissipation in the crystal should be kept as low as possible, consistent with the signal-to-noise requirement for the output. The output signal is the amplified crystal current. If the crystal current is small, to keep power dissipation in the crystal low, high amplifier gain will be required, degrading the output's noise level.

The power dissipation in the crystal is inferred by measuring the current through the crystal and knowing the equivalent series resistance of the crystal. The crystal current is measured by measuring the voltage across the C14/L2 tank, whose (capacitive) reactance is about 208Ω. With 1.2 mArms of crystal current, and a maximum Rs of 80Ω, the maximum power dissipation will be 115μW. This drive level is a good compromise between phase noise and aging.

AGC (Automatic Gain Control)

The gain of the active device in the oscillator circuit (Q1) is adjusted to maintain the level of the circulating crystal current. The gain of Q1 is controlled by changing its emitter current, which is controlled by the AGC circuit, Q2. The AGC amplifier maintains constant ac crystal current by maintaining the peak voltage at the output of the transconductance amplifier.

When power is first applied, the amplitude of the oscillation is zero, Q2 is off, and Q1 is operating at about 5mA of emitter current. The oscillation will soon buildup from the noise. As the output amplitude increases, Q2 will start to turn on during the positive peaks of the rf cycles. As Q2 starts to conduct, the voltage at its collector integrates down, reducing the base current to Q1, reducing the loop gain of the oscillator circuit until the power provided by Q1 exactly matches the losses in the circuit (which are primarily losses in the crystal). The dc gain of the AGC circuit is about 25 (R16/R19), and a 30mV change at the collector of Q2 will reduce the output by about 1 dB, which together yield a very stable output amplitude.

Normally, an emitter current of about 1 mA is required in Q1 to sustain oscillation. With Q1's nominal beta of 100, only 10 uA of base current is needed . (Up to 40 uA is available, as limited by R17.) A nominal value for the oscillation amplitude is 0.7Vpp (0.35Vp) at the base of Q1. This is an rms value of 0.26Vrms, or a crystal current of about 1.2mArms.

Output Amplifier

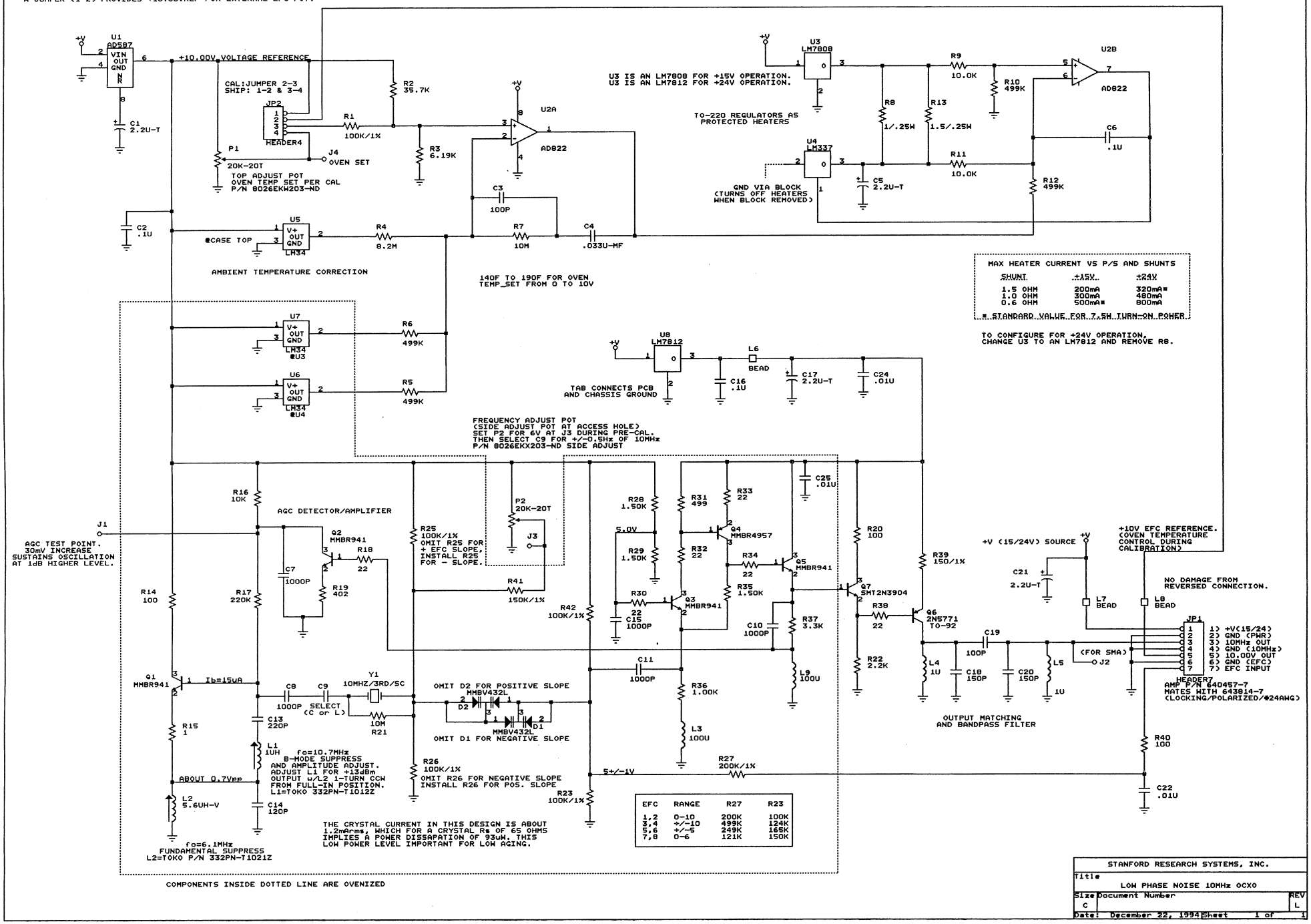
The output amplifier must have a low input impedance, low current and voltage noise, and must provide lots of isolation from the load. The low input impedance is required to maintain a high in-circuit Q for the crystal. Low voltage noise is needed for a low phase noise near the carrier frequency. Low current noise is required for low phase noise far away from the carrier. Finally, good isolation is needed to reduce frequency shifts caused by load changes.

The transconductance amplifier formed by Q3 and Q4 does a good job in all of these areas. The 10MHz current from the crystal (about 1.2mA rms) is applied to the emitter of Q3, which is biased on with about 1.7mA of current. A small fraction (about 10%) of this current enters the emitter of Q3, which is cascoded to R31, a 499Ω collector load resistor. The signal across the load resistor is applied to the base of Q4 (biased on with about 3mA) to generate a collector current of about 1.1mArms. This collector current is returned to the emitter of Q3 through R35, a 1.50kΩ resistor.

The ac voltage at the emitter of Q3 is very nearly zero, as the ac emitter current is only about 0.1mArms. Hence, the input impedance to the amplifier is very low, only a few ohms, despite the low bias current used in Q3. The transimpedance gain, Vout/Iin, is about 1kΩ. The noise voltage has been measured at about 1.2nV/√Hz, and the input noise current at about 15pA/√Hz. Very low noise rf transistors are operated at low bias currents in order to achieve these low noise values.

An emitter follower, Q5, is used to buffer the relatively high output impedance of the transconductance amplifier into the output driver stage. Another emitter follower (Q7) drives the base of the output amplifier, Q6, a 2N5771 transistor biased on with about 25mA. An output network (L4,L5,C18-20) transforms the 50Ω external load to a collector load of about 800Ω for power matching. The network also serves as a bandpass filter, centered on 10MHz, to improve the harmonic distortion specification.

The output matching network provides a low output impedance at dc and at 10MHz, so that the output amplitude is nearly independent of load, and reduces dc errors of comparator stages which may follow.


VOLTAGE APPLIED TO +10.00VREF (PIN 5) DURING CALIBRATION IS USED TO PLATEAU OVEN TEMPERATURE. BEFORE SHIPMENT, THE JUMPER IS MOVED FROM 2-3 TO 3-4 AND P2 IS ADJUSTED TO SET OVEN TO CALIBRATED PLATEAU. A JUMPER (1-2) PROVIDES +10.00VREF FOR EXTERNAL EFC POT.
U1 AD587
+10.00V VOLTAGE REFERENCE
CAL:JUMPER 2-3 SHIP: 1-2 & 3-4
JP2 HEADER4
R1 100K/1%
R2 35.7K
R3 6.19K
P1 20K-20T
TOP ADJUST POT OVEN TEMP SET PER CAL P/N 8026EKW203-ND
J4 OVEN SET
U2A AD822
C1 2.2U-T
C2 .1U
C3 100P
U5 LM34 @CASE TOP
R4 8.2M
R7 10M
C4 .033U-MF
AMBIENT TEMPERATURE CORRECTION
140F TO 190F FOR OVEN TEMP_SET FROM 0 TO 10V
U3 LM7808
U4 LM337
U3 IS AN LM7808 FOR +15V OPERATION.
U3 IS AN LM7812 FOR +24V OPERATION.
TO-220 REGULATORS AS PROTECTED HEATERS
R8 1/.25W
R13 1.5/.25W
R9 10.0K
R10 499K
R11 10.0K
R12 499K
U2B AD822
C6 .1U
C5 2.2U-T
GND VIA BLOCK (TURNS OFF HEATERS WHEN BLOCK REMOVED)
MAX HEATER CURRENT VS P/S AND SHUNTS
SHUNT +15V +24V
1.5 OHM 200mA 320mA*
1.0 OHM 300mA 480mA
0.6 OHM 500mA* 800mA
* STANDARD VALUE FOR 7.5W TURN-ON POWER
TO CONFIGURE FOR +24V OPERATION, CHANGE U3 TO AN LM7812 AND REMOVE R8.
U7 LM34 @U3
U6 LM34 @U4
R6 499K
R5 499K
U8 LM7812
TAB CONNECTS PCB AND CHASSIS GROUND
L6 BEAD
C16 .1U
C17 2.2U-T
C24 .01U
FREQUENCY ADJUST POT (SIDE ADJUST POT AT ACCESS HOLE) SET P2 FOR 6V AT J3 DURING PRE-CAL. THEN SELECT C9 FOR +/-0.5Hz OF 10MHz P/N 8026EKX203-ND SIDE ADJUST
AGC DETECTOR/AMPLIFIER
J1 AGC TEST POINT. 30mV INCREASE SUSTAINS OSCILLATION AT 1dB HIGHER LEVEL.
R16 10K
R14 100
R17 220K
Q2 MMBR941
R18 22
C7 1000P
R19 402
P2 20K-20T
J3
R25 100K/1% OMIT R25 FOR + EFC SLOPE. INSTALL R25 FOR - SLOPE.
R41 150K/1%
R42 100K/1%
R28 1.50K
5.0V
R29 1.50K
R31 499
R33 22
Q4 MMBR4957
R32 22
R34 22
Q5 MMBR941
R30 22
Q3 MMBR941
R35 1.50K
C15 1000P
C10 1000P
R37 3.3K
L9 100U
C25 .01U
R20 100
R22 2.2K
Q7 SMT2N3904
R38 22
Q6 2N5771 TO-92
R39 150/1%
+V (15/24V) SOURCE
C21 2.2U-T
L7 BEAD
L8 BEAD
+10V EFC REFERENCE. COVEN TEMPERATURE CONTROL DURING CALIBRATION)
NO DAMAGE FROM REVERSED CONNECTION.
JP1 HEADER7
1) +V(15/24)
2) GND (PWR)
3) 10MHz OUT
4) GND (10MHz)
5) 10.00V OUT
6) GND (EFC)
7) EFC INPUT
AMP P/N 640457-7
MATES WITH 643814-7 (LOCKING/POLARIZED/@24AWG)
(FOR SMA) J2
C19 100P
C18 150P
C20 150P
L5 1U
L4 1U
OUTPUT MATCHING AND BANDPASS FILTER
Q1 MMBR941
Ib=15uA
C8
C9 1000P SELECT (C or L)
Y1 10MHZ/3RD/SC
10M R21
C13 220P
R15 1
L1 1UH
fo=10.7MHz B-MODE SUPPRESS AND AMPLITUDE ADJUST. ADJUST L1 FOR +13dBm OUTPUT w/L2 1-TURN CCW FROM FULL-IN POSITION. L1=TOKO 332PN-T1012Z
ABOUT 0.7Vpp
L2 5.6UH-V
C14 120P
fo=6.1MHz FUNDAMENTAL SUPPRESS L2=TOKO P/N 332PN-T1021Z
OMIT D2 FOR POSITIVE SLOPE
D2 MMBV432L
D1 MMBV432L
OMIT D1 FOR NEGATIVE SLOPE
C11 1000P
R36 1.00K
L3 100U
R26 100K/1% OMIT R26 FOR NEGATIVE SLOPE INSTALL R26 FOR POS. SLOPE
R23 100K/1%
5+/-1V
R27 200K/1%
R40 100
C22 .01U
EFC RANGE R27 R23
1,2 0-10 200K 100K
3,4 +/-10 499K 124K
5,6 +/-5 249K 165K
7,8 0-6 121K 150K
THE CRYSTAL CURRENT IN THIS DESIGN IS ABOUT 1.2mArms, WHICH FOR A CRYSTAL Rs OF 65 OHMS IMPLIES A POWER DISSAPATION OF 93uW. THIS LOW POWER LEVEL IMPORTANT FOR LOW AGING.
COMPONENTS INSIDE DOTTED LINE ARE OVENIZED
STANFORD RESEARCH SYSTEMS, INC.
Title
LOW PHASE NOISE 10MHz OCXO
Size C
Document Number
REV L
Date: December 22, 1994 Sheet 1 of 1