TEK SERVICE MANUAL

070-6330-00
Product Group 32

2430A DIGITAL OSCILLOSCOPE SERVICE

Tektronix

LIST OF ILLUSTRATIONS

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LIST OF TABLES

OPERATORS SAFETY SUMMARY

The general safety information in this part of the summary is for both operating and servicing personnel. Specific warnings and cautions will be found throughout the manual where they apply and do not appear in this summary.

Terms in This Manual

CAUTION statements identify conditions or practices that could result in damage to the equipment or other property.

WARNING statements identify conditions or practices that could result in personal injury or loss of life.

Terms as Marked on Equipment

CAUTION indicates a personal injury hazard not immediately accessible as one reads the markings, or a hazard to property, including the equipment itself.

DANGER indicates a personal injury hazard immediately accessible as one reads the marking.

Symbols in This Manual

This symbol indicates where applicable cautionary or other information is to be found. For maximum input voltage see Table 1-1.

Symbols as Marked on Equipment

DANGER — High voltage.

Protective gound (earth) terminal.

ATTENTION — Refer to manual.

Power Source

This product is intended to operate from a power source that will not apply more than 250 volts rms between the supply conductors or between either supply conductor and ground. A protective ground connection by way of the grounding conductor in the power cord is essential for safe operation.

Grounding the Product

This product is grounded through the grounding conductor of the power cord. To avoid electrical shock, plug the power cord into a properly wired receptacle before making any connections to the product input or output terminals. A protective ground connection by way of the grounding conductor in the power cord is essential for safe operation.

Danger Arising from Loss of Ground

Upon loss of the protective-ground connection, all accessible conductive parts (including knobs and controls that may appear to be insulated) can render an electric shock.

Use the Proper Power Cord

Use only the power cord and connector specified for the instrument.

Use the Proper Fuse

To avoid fire hazard, use only the fuse specified in the instrument parts list. A replacement fuse must meet the type, voltage rating, and current rating specifications for the fuse that it replaces.

Do Not Operate in Explosive Atmospheres

To avoid explosion, do not operate this instrument in an atmosphere of explosive gasses.

Do Not Remove Covers or Panels

To avoid personal injury, the instrument covers or panels should only be removed by qualified service personnel. Do not operate the instrument without covers and panels properly installed.

SERVICING SAFETY SUMMARY

FOR QUALIFIED SERVICE PERSONNEL ONLY

Refer also to the preceding Operators Safety Summary.

Do Not Service Alone

Do not perform internal service or adjustment of this product unless another person capable of rendering first aid and resuscitation is present.

Use Care When Servicing With Power On

Dangerous voltages exist at several points in this product. To avoid personal injury, do not touch exposed connections or components while power is on.

Disconnect power before removing protective panels, soldering, or replacing components.

Power Source

This product is intended to operate from a power source that does not apply more than 250 volts rms bwetween the supply conductors or between either supply conductor and ground. A protective ground connection by way of the grounding connector in the power cord is essential for safe operation.

SPECIFICATION

INTRODUCTION

The TEKTRONIX 2430A Digital Oscilloscope is a portable, dual-channel instrument with a maximum digitizing rate of 100 Megasamples per second. The scope is capable of simultaneous acquisition of Channel 1 and Channel 2 input signals. It has a real-time useful storage bandwidth of 40 MHz for single-event acquisitions, with an equivalent-time bandwidth of 150 MHz when repetitive acquisitions are acquired. Since both channels are acquired simultaneously, the XY display is available to full bandwidth. Options include a Word Recognition Probe, Video signal triggering, Probe Power, and Rackmounting.

The instrument is microprocessor controlled and menu driven, displaying at the top of the screen alphanumeric CRT readouts of the vertical and horizontal scale factors, trigger levels, trigger source, and cursor measurements. Menus, displayed at the bottom of the CRT display, are used by the operator to select the operating mode.

A user makes decisions as to what operation and mode setup the instrument must have to make the measurement wanted and then selects the proper functions using a combination of front-panel buttons and the displayed menu.

Five menu buttons mounted on the CRT bezel are used to make selections from the entry choices displayed. The top line of the menu display usually contains the menu title, and the bottom line labels the buttons with the control functions they select. The selection is made (indicated by an underscoring of the menu label in the display) when the bezel button below the selected function is pressed. The menus, system operating modes, and auxiliary functions are described in Section 5, "Controls, Connectors, and Indicators" of the Operators manual included with this instrument, and the "Getting Acquainted" procedure in Section 1 of that manual familiarizes the user with menu operation.

VERTICAL SYSTEM

The two vertical channels have calibrated deflection factors from 2 mV to 5 V per division in a 1-2-5 sequence of 14 steps. Use of coded probes having attenuation factors of 1X, 10X, 100X, and 1000X extends the minimum sensitivity to 5,000 V per division (with the 1000X probe) and the maximum sensitivity to 200 μV per division (using a 1X probe in SAVE or AVERAGE expanded mode).

VOLTS/DIV readouts are automatically switched to display a correct scale factor when properly coded probes are attached. Each channel can be separately inverted. ADD and MULT are display functions provided by the processor system.

In SAVE mode, the waveforms may be both horizontally and vertically repositioned, expanded horizontally and vertically, added to each other, or multiplied together for either XY or YT displays.

HORIZONTAL SYSTEM

Horizontal display modes of A, A INTEN, and B Delayed are available. The time base has 28 calibrated SEC/DIV settings in a 1-2-5 sequence from 5 ns per division to 5 s per division. An External Clock mode is provided that accepts clocking signals from 1 MHz to 100 MHz.

The B Trace and the intensified zone on the A INTEN Trace may be delayed by time with respect to the A trigger, and a DELAY by EVENTS function permits the A display to be delayed by a selected number of B Trigger events. In the case of DELAY by EVENTS, the B Trigger SOURCE, COUPLING, SLOPE, and LEVEL controls define the nature of the signal needed to produce events triggering. The number of events required to satisfy the

delay may be set from 1 to 65,536, with a resolution of one event. The DELTA DELAY feature produces two independently settable delayed B Traces in DELAY by TIME.

TRIGGER SYSTEM

The trigger system of the scope provides many features for selecting and processing a signal used in triggering the acquisition system. The conventional features of SOURCE selection, Trigger LEVEL control, Trigger SLOPE, Trigger MODE, and CPLG (coupling) include enhancements not normally found in a conventional oscilloscope.

The choices of VERT, CH1 or CH2, EXT1 or EXT2, LINE, and A*B or WORD (16-bit data word recognition) are available as SOURCE selections for triggering A Horizontal Mode acquisitions. These sources for trigger signals provide a wide range of applications involving specialized triggering requirements. Except for A*B (A AND B) and LINE (power-source frequency), the same Trigger SOURCE selections are available for triggering B acquisitions. The selected trigger signal is conditioned by the choice of input CPLG (coupling). These coupling selections are AC, DC, HF REF, LF REJ, and NOISE REJ. LEVEL control provides a settable amplitude (with CRT readout) at which triggering will occur, and SLOPE control determines on which slope of the triggering signal (plus or minus) the acquisition is triggered.

Trigger MODE choices are AUTO LEVEL, AUTO, NORM, and SINGLE SEQ (single sequence), for the A and A INTENSIFIED Modes, and Triggerable After Delay and Runs After Delay, for the B Mode. AUTO LEVEL provides for automatic leveling on the applied trigger signal. AUTO MODE produces an auto trigger in the event a trigger signal is either not received or not within the limits needed to produce a triggering event. When triggering conditions are met, a normal triggered display results. At SEC/DIV settings of 100 ms per division and longer, the AUTO MODE switches to ROLL. In ROLL MODE, the display is continually updated and trigger signals are disregarded.

NORM (normal) trigger MODE requires that all triggering requirements are met before an acquisition will take place. SINGLE SEQ (single sequence) MODE is a variation of the conventional single-shot displays found on many previous oscilloscopes. In SINGLE SEQ, a single complete acquisition is done on all called-up VERTICAL MODES. Since an acquisition depends on the acquisition mode in effect, many of the scope operating features are altered in SINGLE SEQ. A complete description of this mode is discussed in "Controls, Connectors, and Indicators" in Section 5 of the Operators manual.

The user has a choice of trigger points within the acquired waveform record by selecting the amount of pretrigger data displayed. The trigger location in the record is selectable from a choice of five pretrigger lengths beginning at one-eighth of the record length and increasing to seven-eighths of the record length. A record trigger position is independently selectable for both A and B acquisitions. Additional trigger positions in the record are selectable via the GPIB interface commands.

CURSOR MEASUREMENTS

Time and Voltage cursors are provided for making parametric measurements on the displayed waveforms. Time may be measured either between the cursor positions (DELTA TIME) or between a selected cursor and the trigger point of an acquired waveform (ABSOLUTE). Time cursor readouts are scaled in seconds, degrees, or percentage values. The 1/TIME cursors may be scaled in hertz (Hz), degrees, or percentage.

Voltage cursor measurements on a waveform display can be selected to read either the voltage difference between the cursor positions or the absolute voltage position of a selected cursor with respect to ground. The volts measurement readouts may be scaled in units of volts, decibels (dB), or percent. The Voltage cursors and Time cursors may also be coupled to track together (V@T and SLOPE) and assigned to a particular waveform for ease in making peak-to-peak and slope waveform measurements. The units for V@T may be volts, percent, or dB; SLOPE may have units of slope (VOLTS/SEC), percent (VOLTS/VOLT), or dB.

WAVEFORM ACQUISITION

Waveforms may be acquired in different modes, depending on the measurement requirements. The acquisition modes of NORMAL, ENVELOPE, and AVG (averaging) provide the user with a wide range of measurement adaptability. NORMAL mode provides a continuous acquisition producing a "live" waveform display similar to that seen with an analog oscilloscope. AVG (averaging) mode is especially useful for improving the signal-to-noise ratio of the displayed waveform. Small amplitude signals masked by noise become easily visible for making measurements and analysis by averaging from 2 to 256 acquisitions for removing uncorrelated noise.

Equivalent-time sampling, used for NORMAL and AVG acquisition of recurring periodic signals, extends the useful storage bandwidth to 150 MHz when the REPETITIVE mode is on. Randomly acquired data points taken from a periodic signal are used to fill the complete record of the signal waveform display. Depending on the SEC/DIV setting, as few as 10 samples (at 5 ns/DIV) or as many as 409 (at 200 ns/DIV) samples may be obtained on each trigger event. The user sees the waveform display build up as dots until the entire 1024 data point record is filled.

ENVELOPE mode saves the maximum and minimum data-point values over a selected number of acquisitions from 1 to 256 plus CONT (continuous). The display presents a visual image of the amount of change (envelope) that occurs to a waveshape during the accumulated acquisitions. Frequency, phase, amplitude, and position changes are easily identified when acquiring in ENVELOPE mode. The glitch-catching capability of ENVELOPE mode can capture single-event pulses as narrow as 2 ns at the slowest SEC/DIV setting of 5 seconds per division.

Horizontally, the record length of acquired waveforms is 1024 data points (512 max/min pairs in ENVELOPE mode), of which 500 make up a one-screen display (50 data points per division for 10 divisions). The entire record may be viewed by using the Horizontal POSITION control to position any portion of the record within the viewing area.

STORAGE AND I/O

Acquired waveforms may be saved in any of four REF waveform nonvolatile memories. Any or all of the saved reference waveforms may be displayed for comparison with the waveforms being currently acquired. The source and destination of waveforms to be saved may be user designated. Assignment can be made to save either channel 1 or channel 2 (or the results of an addition or multiplication of the two channels) to any REF memory or to move a stored reference from one REF memory to another. Reference waveforms may also be written into a REF memory location via the GPIB interface.

The scope is fully controllable and capable of sending and receiving waveforms via the standard equipped GPIB interface. This feature makes the instrument ideal for making automated measurements in a production or research and development environment that calls for repetitive data taking. Self- calibration and self-diagnostic features built into the scope to aid in fault detection and servicing are also accessible via commands sent from the GPIB controller.

Another standard feature is the "DEVICES" setting for GPIB Interface control. This feature allows the user to output waveforms (and other on-screen information) to either a HP® Graphics Printer or Plotter from the scope front-panel, providing a way to obtain hard copies of acquired waveforms without putting the scope into a system controller environment.

EXTENDED FEATURES

There are several other features incorporated into this instrument designed to make it more usable, namely, the HELP, AUTOsetup, MEASURE, and AutoStep Sequencer features.

HELP: The HELP function can be used to display operational information about any front-panel control. When HELP mode is in effect, manipulating almost any front-panel control causes the scope to display information about that control. When HELP is first invoked, an introduction to HELP is displayed on screen.

AUTOsetup: The AUTOsetup function is used to automatically setup the scope for a viewable display based on the input signal. The user can specify the waveform characteristic the display is optimized for (front-edge, period, etc.) from a menu displayed upon executing AUTOsetup.

MEASURE: MEASURE automatically extracts parameters from signal input to the scope. In the "SNAPSHOT" mode, 20 different waveform parameters are extracted and displayed for a single acquisition. In the continuous extraction mode, up to four parameters are extracted continuously as the instrument continues to acquire.

AutoStep Sequencer (PRGM): With AutoStep, the user can save single front-panel setups or sequences of setups and associated flow control and Input/Output actions for later recall. If MEASURE and/or OUTPUT are saved as part of these setups they can be used for automatic parameter extraction and data printout. 100 to 800 front-panel setups (depending on complexity) can be stored in one or more sequences.

The complete descriptions of these four features are found in Section 5 of the Operators manual included with this instrument.

The following items are standard accessories shipped with the scope instrument:

2	Probe packages
1	Snap-lock accessories pouch
1	Zip-lock accessories pouch
1	Operators manual
1	Programmer's Reference Guide
1	Users Reference Guide
1	Fuse
1	Power cord (installed)
1	Blue plastic CRT filter (installed)
1	Clear plastic CRT filter
1	Front-panel cover

For part numbers and further information about standard accessories and a list of the optional accessories, refer to "Options and Accessories" (Section 7) in this manual. For additional information on accessories and ordering assistance, contact your Tektronix representative or local Tektronix Field Office.

PERFORMANCE CONDITIONS

The following electrical characteristics (Table 6-1) apply when the scope has been calibrated at an ambient temperature between +20°C and +30°C, has had a warmup period of at least 20 minutes and is operating at an ambient temperature between −15°C and +55°C (unless otherwise noted).

Items listed in the "Performance Requirements" column are verifiable qualitative or quantitative limits that define the measurement capabilities of the instrument.

Environmental characteristics are given in Table 6-2. The scope meets the environmental requirements of MIL-T-28800C for Type III, Class 3, Style D equipment, with the humidity and temperature requirements defined in paragraphs 3.9.2.2, 3.9.2.3, and 3.9.2.4. The rackmounted scope meets the vibration and shock requirements of MIL-T-28800C for Type III, Class 5, Style D equipment when mounted using the rackmount rear-support kit supplied with both the 1R Option and the Rackmount Conversion kit.

Mechanical characteristics of the scope are listed in Table 6-3.

Video Option characteristics are given in Table 6-4.

RECOMMENDED ADJUSTMENTS SCHEDULE

For optimum performance to specification, the internal SELF CAL should be done:

1. If the operating temperature is changed by more that 5°C since the last SELF CAL was performed.

2. Immediately before before making measurements requiring the highest degree of accuracy.

Table 1-1

Electrical Characteristics

Characteristics	Performance Requirements
ACQUISITION SYSTEM—CHANNEL 1 AND CHANNEL 2	
Resolution	8 bits.[a] Displayed vertically with 25 digitization levels (DL)[b] per division, 10.24 divisions dynamic range.[a]
Record Length	1024 samples.[a] Displayed horizontally with 50 samples per division, 20.48-division trace length.[a]
Sample Rate	10 samples per second to 100 megasamples per second (5 s per division to 500 ns per division).
Sensitivity	
Range	80 μV per DL to 0.2 V per DL in a 1-2-5 sequence of 11 steps (2 mV per division to 5 V per division).
Accuracy	
Normal and Average Modes	Within ± (2% + 1 DL) at any VOLTS/DIV setting for a signal 1 kHz or less contained within ±75 DL (±3 divisions) of center when an Autocal has been performed within ±15°C of the operating temperature. Measured on a four- or five-division signal with VOLTS or V@T cursors; UNITS set to delta volts.
Envelope Mode	Add 1% to Normal Mode specifications.
Variable Range	Continuously variable between VOLTS/DIV settings. Extends sensitivity to 0.5 V per DL or greater, 12.5 V per division or greater.
Bandwidth	
Normal and Average Mode; Repet off; SEC/DIV at 0.5 μs or Faster	DC to 40 MHz (calculated useful storage bandwidth—USB).[a] $USB = \frac{F_{(\text{sample freq max})}}{2.5}$ [c]
Normal and Average Modes with Repet On or Continuous Envelope Mode; SEC/DIV at 0.2 μs or Faster (−3 dB bandwidth)	DC to 150 MHz. Bandwidth with a P6133 probe is checked using the obtainable reference signal (six divisions or less) from a terminated 50 Ω system via probe-tip-to-BNC adapter.[a] Bandwidth with external termination is checked using a six-division reference signal from terminated 50 Ω system.[a] Bandwidth with internal termination is checked using a six-division reference signal from a terminated 50 Ω system.

[a]Performance Requirement not checked in the manual.

[b]"DL" is the abbreviation for "digitization level". A DL is the smallest voltage level change that can be resolved by the internal 8-bit A-D converter, with the input scaled to the VOLTS/DIV setting of the channel used. Expressed as a voltage, a DL is equal to 1/25 of a division times the VOLTS/DIV setting.

[c]Sample frequency max. is 100 MHz.

Table 1-1 (cont)

Characteristics	Performance Requirements
AC Coupled Lower −3 dB Point	
1X Probe	10 Hz or less.[a]
10X Probe	1 Hz or less.[a]
Step Response, Repet and Average On; Average Set to 16	
Rise Time	2.3 ns or less (calculated).[a] $T_r \text{ (in ns)} = \frac{350}{\text{BW (in MHz)}}$
Envelope Mode Pulse Response	
Minimum Single Pulse Width for 50% or Greater Amplitude Capture at 85% or Greater Confidence	2 ns.[a]
Minimum Single Pulse Width for Guaranteed 50% or Greater Amplitude Capture	4 ns.[a]
Minimum Single Pulse Width for Guaranteed 80% or Greater Amplitude Capture	8 ns.[a]
Channel Isolation	100:1 or greater attenuation of the deselected channel at 100 MHz; 50:1 or greater attenuation at 150 MHz, for a 10-division input signal from 2 mV/div to 500 mV/div; with equal VOLTS/DIV settings on both channels.
Acquired Channel 2 Signal Delay with Respect to Channel 1 Signal at Full Bandwidth	±250 ps.[a]
Input R and C (1 MΩ)	
Resistance	1 MΩ ±0.5%.[a] In each attenuator, the input resistance of all VOLTS/DIV positions is matched to within 0.5%.[a]
Capacitance	15 pF ±2 pF.[a] In each attenuator, the input capacitance of all VOLTS/DIV positions is matched to within 0.5 pF.[a]

[a]**Performance Requirement not checked in the manual.**

Table 1-1 (cont)

Characteristics	Performance Requirements
Input R (50 Ω)	
Resistance	50 Ω ±1%.[a]
VSWR (DC to 150 MHz)	1.3:1 or better.[a]
Maximum Input Voltage ⚠	5 V rms; 0.5 W·sec for any one-second interval for instantaneous voltages from 5 V to 50 V.
Maximum Input Voltages ⚠	
Input Coupling Set to DC, AC, or GND	400 V (dc + peak ac); 800 V p-p ac at 10 kHz or less.[a]
Common-Mode Rejection Ratio (CMRR); ADD Mode with Either Channel Inverted	At least 10:1 at 50 MHz for common-mode signals of 10 divisions or less with VARIABLE VOLTS/DIV adjusted for best CMRR at 50 kHz.
POSITION	
Range	±(9.3 to 10.4) div., at 50 mV per division with INVERT off, when Self Cal has been done within ±5°C of the operating temperature.
Gain Match Between NORMAL and SAVE	±3 DLs for positions within ±5 divisions from center.
Low-Frequency Linearity	
Normal or Average Mode	3 DLs or less compression or expansion of a two-division, center-screen signal when positioned anywhere within the acquisition window.
20 MHz Bandwidth Limiter	
−3 dB Bandwidth	13 MHz to 24 MHz.
50 MHz Bandwidth Limiter	
−3 dB Bandwidth	40 MHz to 55 MHz.
Rise Time	6.3 ns to 8.7 ns.[a] With a five-division, fast-rise step (rise time of 300 ps or less) using 50 Ω dc input coupling and VOLTS/DIV setting of 10 mV.[a]

[a]Performance Requirement not checked in the manual.

Table 1-1 (cont)

Characteristics	Performance Requirements
TRIGGERING—A and B	
Minimum P-P Signal Amplitude for Stable Triggering from Channel 1, Channel 2, or ADD	
A Trigger	
DC Coupled	0.35 division from DC to 50 MHz, increasing to 1.0 division at 150 MHz; 1.5 divisions at 150 MHz in ADD mode.
NOISE REJ Coupled	1.2 divisions or less from DC to 50 MHz, increasing to 3 divisions at 150 MHz; 4.5 divisions at 150 MHz in ADD mode.
AC Coupled	0.35 division from 60 Hz to 50 MHz; increasing to 1.0 division at 150 MHz, 1.5 divisions at 150 MHz in ADD mode. Attenuates signals below 60 Hz.
HF REJ Coupled	0.50 division from DC to 30 kHz. Attenuates signals above 30 kHz.
LF REJ Coupled	0.50 division from 80 kHz to 50 MHz; increasing to 1.0 division at 150 MHz; 1.5 divisions at 150 MHz in ADD mode. Attenuates signal below 80 kHz.
B Trigger	Multiply all A Trigger specifications by two.
A•B Selected	Multiply all A Trigger specifications by two.
Minimum P-P Signal Amplitude for Stable Triggering from EXT TRIG 1 or EXT TRIG 2 Source	
A Trigger	
EXT Gain = 1	
DC Coupled	17.5 mV from DC to 50 MHz, increasing to 50 mV at 150 MHz.
NOISE REJ Coupled	60 mV or less from DC to 50 MHz; increasing to 150 mV at 150 MHz.
AC Coupled	17.5 mV from 60 Hz to 50 MHz; increasing to 50 mV at 150 MHz. Attenuates signals below 60 Hz.
HF REJ Coupled	25 mV from DC to 30 kHz.
LF REJ Coupled	25 mV from 80 kHz to 50 MHz; increasing to 50 mV at 150 MHz.
EXT Gain = ÷5	Amplitudes are five times those specified for Ext Gain = 1.
B Trigger	Multiply all A Trigger amplitude specifications by two.
A•B Selected	Multiply all A Trigger amplitude specifications by two.
Maximum P-P Signal Rejected by NOISE REJ Coupling Signals within the Vertical Bandwidth	
Channel 1 or Channel 2 Source	0.4 division or greater for VOLTS/DIV settings of 10 mV and higher. Maximum noise rejected is reduced at 2 mV per division and 5 mV per division.
EXT TRIG 1 or EXT TRIG 2 Source	20 mV or greater when Ext Trig Gain = 1. 100 mV or greater when Ext Trig Gain = ÷5.

Table 1-1 (cont)

Characteristics	Performance Requirements
EXT TRIG 1 and EXT TRIG 2 Inputs	
Resistance	1 MΩ ±1%.[a]
Capacitance	15 pF ±3 pF.[a]
Maximum Input Voltage ⚠	400 V (dc + peak ac); 800 V p-p ac at 10 kHz or less.[a]
LEVEL Control Range	
Channel 1 or Channel 2 Source	±18 divisions × VOLTS/DIV setting.[a]
EXT TRIG 1 or EXT TRIG 2 Source	
EXT GAIN = 1	±0.9 volt.[a]
EXT GAIN = ÷5	±4.5 volts.[a]
LEVEL Readout Accuracy (for triggering signals with transition times greater than 20 ns)	
Channel 1 or Channel 2 Source	
DC Coupled	
+15°C to +35°C	Within ± [3% of setting + 3% of p-p signal + (0.2 division × VOLTS/DIV setting) + 0.5 mV + (0.5 mV × probe attenuation factor)].
−15°C to +55°C (excluding +15°C to +35°C)	Add (1.5 mV x probe attenuation) to +15°C to +35°C specification.[a]
NOISE REJ Coupled	Add ± (0.6 division × VOLTS/DIV setting) to DC Coupled specifications. Checked at 50 mV per division.
EXT TRIG 1 or EXT TRIG 2 Source	
EXT GAIN = 1	
DC Coupled	Within ± [3% of setting + 4% of p-p signal + 10 mV + (0.5 mV × probe attenuation factor)].
NOISE REJ Coupled	Add ±30 mV to DC Coupled specifications.
EXT GAIN = ÷5	
DC Coupled	Within ± [3% of setting + 4% of p-p signal + 50 mv + (0.5 mV × probe attenuation factor)].
NOISE REJ Coupled	Add ±150 mV to DC Coupled specifications.

[a]Performance Requirement not checked in manual.

Table 1-1 (cont)

Characteristics	Performance Requirements		
Variable A Trigger Holdoff	**A SEC/DIV[a]**	**MIN HO[a]**	**MAX HO[a]**
	5 ns 10 ns 20 ns 50 ns 100 ns 200 ns	2-4 μs	9-15 μs
	500 ns	5-10 μs	
	1 μs 2 μs 5 μs	10-20 μs 20-40 μs 50-100 μs	100-150 μs
	10 μs 20 μs 50 μs	0.1-0.2 ms 0.2-0.4 ms 0.5-1.0 ms	1-1.5 ms
	100 μs 200 μs 500 μs	1-2 ms 2-4 ms 5-10 ms	10-15 ms
	1 ms 2 ms 5 ms	10-20 ms 20-40 ms 50-100 ms	90-150 ms
	10 ms 20 ms 50 ms	0.1-0.2 s 0.2-0.4 s 0.5-1.0 s	0.9-1.5 s
	100 ms 200 ms	1-2 s 2-4 s	9-15 s
	500 ms 1 s 2 s 5 s	5-10 s	
SLOPE Selection	Conforms to trigger-source waveform and ac-power-source waveform.		
Trigger Position Jitter (p-p)			
SEC/DIV 0.5 μs per Division or Greater			
A and B Triggered Sweeps	0.04 × SEC/DIV setting.[a]		
B RUNS AFTER Delay	0.08 × SEC/DIV setting.[a]		
SEC/DIV 0.2 μs per Division or Less	(0.02 × SEC/DIV setting) + 500 ps[a] Checked at 5 ns/DIV in NORMAL ACQUIRE mode with REPET ON using a 5-division step having less or equal to 1 ns rise time.		

[a]Performance Requirement not checked in the manual.

Table 1-1 (cont)

Characteristics	Performance Requirements
TIME BASE	
Sample Rate Accuracy	
Average Over 100 or More Samples	±0.001%.[a]
External Clock	
Repetition Rate	
Minimum	1 MHz.[a]
Maximum	100 MHz.[a]
Events Count	1 to 65,536[a]
Events Maximum Repetition Rate	100 MHz.[a]
Signal Levels Required for EXT Clock or EVENTS	
Channel 1 or Channel 2 SOURCE	
DC Coupled	0.7 division from DC to 20 MHz; increasing to 2.0 divisions at 100 MHz; 3.0 divisions at 100 MHz in ADD mode.[a]
NOISE REJ Coupled	2.4 divisions or less from DC to 20 MHz; increasing to 6.0 divisions at 100 MHz; 9.0 divisions at 100 MHz in ADD mode.[a]
AC Coupled	0.7 division from 60 Hz to 20 MHz; increasing to 2.0 divisions at 100 MHz; 3.0 divisions at 100 MHz in ADD mode. Attenuates signals below 60 Hz.[a]
HF REJ Coupled	2.0 divisions from DC to 30 kHz. Attenuates signals above 30 kHz.[a]
LF REJ Coupled	2.0 divisions from 80 kHz to 20 MHz; increasing to 4.0 divisions at 100 MHz; 3.0 divisions at 100 MHz in ADD mode. Attenuates signals below 80 kHz.[a]
EXT TRIG 1 or EXT TRIG 2 Source	
Ext Gain = 1	
DC Coupled	35 mV from DC to 20 MHz; increasing to 100 mV at 100 MHz.[a]
NOISE REJ Coupled	120 mV or less from DC to 20 MHz; increasing to 300 mV at 100 MHz.[a]
AC Coupled	35 mV from 60 Hz to 20 MHz; increasing to 100 mV at 100 MHz. Attenuates signals below 60 Hz.[a]
HF REJ Coupled	50 mV from DC to 30 kHz.[a]
LF REJ Coupled	50 mV from 80 kHz to 20 MHz; increasing to 100 mV at 100 MHz.[a]
Ext Gain = ÷ 5	Amplitudes are five times those specified for Ext Gain = 1.[a]
Delay Time Range	(0.04 × B SEC/DIV) to (65,536 × 0.04 × B SEC/DIV).[a]
Delay Time Accuracy	Same as the sample rate accuracy.[a]
Delay Time Resolution	The greater of (0.04 × B SEC/DIV) or 20 ns.

[a]Performance Requirement not checked in the manual.

Table 1-1 (cont)

Characteristics	Performance Requirements
NONVOLATILE MEMORY	
Front-Panel Setting, Waveform Data, Sequencer, and Calibration Data Retention Time	Greater than 3 years.
Battery	3.6-volt, 1.6-Amp Hour, Lithium Thionyl Chloride; Manufacturer EAGLE PICHER, Type LTC16P/P, TEK Part Number 146-0062-00; UL Listed. (See Warning below.) **WARNING** *To avoid personal injury, observe proper procedures for handling and disposal of lithium batteries. Improper handling may cause fire, explosion, or severe burns. Don't recharge, crush, disassemble, heat the battery above 212°F (100°C), incinerate, or expose contents of the battery to water. Dispose of battery in accordance with local, state, and national regulations.* *Typically, small quantities (less than 20) can be safely disposed of with ordinary garbage in a sanitary landfill.* *Larger quantities must be sent by surface transport to a hazardous waste disposal facility. The batteries should be individually packaged to prevent shorting and packed in a sturdy container that is clearly labeled "Lithium Batteries—DO NOT OPEN."*

*Performance Requirement not checked in the manual.

Table 1-1 (cont)

Characteristics	Performance Requirements
SIGNAL OUTPUTS	
CALIBRATOR	CALIBRATOR output amplitudes at 5 MHz are at least 50% of output amplitudes at 1 ms SEC/DIV setting.[a]
Voltage (with A SEC/DIV switch set to 1 ms)	
1 MΩ Load	0.4 V ±1%.[a]
50 Ω Load	0.2 V ±1.5%.[a]
Current (short circuit load with A SEC/DIV switch set to 1 ms)	8 mA ±1.5%.[a]
Repetition Period	

A SEC/DIV Setting[a]	Calibrator Frequency[a]	Calibrator Period[a]	Div/ Cycle[a]
5 ns	5 MHz	200 ns	40
10 ns			20
20 ns			10
50 ns			4
100 ns			2
200 ns			1
500 ns	500 kHz	2 μs	4
1 μs			2
5 μs	50 kHz	20 μs	4
10 μs			2
20 μs			1
50 μs	5 kHz	200 μs	4
100 μs			2
200 μs			1
500 μs	500 Hz	2 ms	4
1 ms			2
2 ms			1
5 ms	50 Hz	20 ms	4
10 ms			2
20 ms			1
50 ms			0.4
100 ms			0.2
200 ms			0.1
500 ms			0.04
1 s			0.02
2 s			0.01
5 s			0.004

Accuracy	±0.001%[a]
Symmetry	Duration of high portion of output cycle is 50% of output period ± (lesser of 500 ns or 25% of period).[a]

[a]Performance Requirement not checked in the manual.

Table 1-1 (cont)

Characteristics	Performance Requirements
CH 2 SIGNAL OUTPUT	
Output Voltage	20 mV per division ±10% into 1 MΩ. 10 mV per divison ±10% into 50 Ω.
Offset	±10 mV into 50 Ω, when dc balance has been performed within ±5°C of the operating temperature.
−3 dB Bandwidth	DC to greater than 50 MHz.
A TRIGGER, RECORD TRIGGER, and WORD RECOGNIZER Output	
Logic Polarity	Negative true. Trigger occurrence indicated by a HI to LO transition.[a]
Output Voltage HI	
Load of 400 μA or Less	2.5 V to 3.5 V.[a]
50 Ω Load to Ground	0.45 V or greater.[a]
Output Voltage LO	
Load of 4 mA or Less	0.5 V or less.[a]
50 Ω Load to Ground	0.15 V or less.[a]
SEQUENCE OUT, STEP COMPLETE Outputs	
Logic Polarity	Negative true. Hi to LO transition indicates the event occurred.
Output Voltage Hi	
Load of 400 μA or less	2.5 V to 3.5 V.[a]
50-Ω Load to Ground	0.45 V or greater.[a]
Output Voltage LO	
Load of 4 mA or less	0.5 V or less.[a]
50-Ω Load to Ground	0.15 V or less.[a]
SEQUENCE IN Input	
Logic Polarity	Negative true. HI to LO transition restarts a paused sequence.[a]
High-Level Input Current	20 μA maximum at Vin = 2.7 V.[a]
Low-Level Input Current	−0.4 mA maximum at Vin = 0.4 V.[a]
High-Level Input Voltage	2.0 V minimum.[a]
Low-level Input Voltage	0.8 V maximum.[a]
Absolute Maximum Ratings	
Vin max	+7.0 V.[a]
Vin min	−0.5 V.[a]

[a]Performance Requirements not checked in manual.

Table 1-1 (cont)

Characteristics	Performance Requirements
	DISPLAY
Graticule	80 mm × 100 mm (8 × 10 divisions).[a]
Phosphor	P31.[a]
Nominal Accelerating Potential	16 kV.[a]
Waveform and Cursor Display, Vertical	
Resolution, Electrical	One part in 1024 (10 bit). Calibrated for 100 points per division.[a]
Gain Accuracy	Graticule indication of voltage cursor difference is within 1% of CRT cursor readout value, measured over center 6 divisions.
Centering; Vectors OFF	Within ±0.1 division.
Offset with Vectors ON	Less than 0.05 division.
Linearity	Less than 0.1 division difference between graticule indication and crt cursor readout when active volts cursor is positioned anywhere on screen and inactive cursor is at center screen.[a]
Vector Response	
NORMAL Mode	
Step Aberration	+4%, −4%, 4% p-p.
Fill	Edges of filled regions match reference lines within ±0.1 division.
ENVELOPE Mode	
Fill	Less than 1% change in p-p amplitude of a 6-division, filled ENVELOPE waveform when switching vectors ON and OFF.
Waveform and Cursor Display, Horizontal	
Resolution, Electrical	One part in 1024 (10 bit). Calibrated for 100 points per division.[a]
Gain Accuracy	Graticule indication at time cursor difference is within 1% of crt cursor readout value, measured over center 6 divisions.
Centering; Vectors OFF	Within ±0.1 division.
Offset with Vectors ON	Less than 0.05 division.
Linearity	Less than 0.1 division difference between graticule indication and crt cursor readout when active time cursor is positioned anywhere along center horizontal graticule line and inactive cursor is at center screen.[a]

[a]**Performance Requirement not checked in the manual.**

Table 1-1 (cont)

Characteristics	Performance Requirements
AC POWER SOURCE	
Source Voltage	
Nominal Ranges	
115 V	90 V to 132 V.[a]
230 V	180 V to 250 V.[a]
Source Frequency	48 Hz to 440 Hz.[a]
Fuse Rating	5 A, 250 V, AGC/3AG, Fast Blow; or 4 A, 250 V, 5 × 20 mm Time-Lag (T).[a] Each fuse type requires a different fuse cap.[a]
Power Consumption	
Typical (standard instrument)	160 watts (250 VA).[a]
Maximum (fully optioned instrument)	200 watts (300 VA).[a]
Primary Grounding[c]	Type test 0.1 Ω maximum. Routine test to check grounding continuity between chassis ground and protective earth ground.[a]

[a]Performance Requirement not checked in the manual.

[c]Routine test is with ROD-L/EPA Electronic Model 100AV Hi-Pot Tester. This tests both the Primary Circuit Dielectric Withstand and Primary Grounding in one operation. Contact Tektronix Product Safety prior to using any other piece of equipment to perform these tests.

Table 1-2

Environmental Characteristics

Characteristics	Performance Requirements
STANDARD INSTRUMENT	
Environmental Requirements	This Oscilloscope meets the environmental requirements of MIL-T-28800C for Type III, Class 3, Style D equipment, with the humidity and temperature requirements defined in paragraphs 3.9.2.2, 3.9.2.3, and 3.9.2.4.
Temperature	
Operating	−15°C to +55°C.
Nonoperating (storage)	−62°C to +85°C.
Altitude	
Operating	To 15,000 feet (4500 meters). Maximum operating temperature decreased 1°C for each 1000 feet (300 meters) above 5000 feet (1500 meters).
Nonoperating (storage)	To 50,000 feet (15,000 meters).
Humidity	
Operating and Storage	Stored at 95% relative humidity for five cycles (120 hours) from 30°C to 60°C, with operation performance checks at 30°C and 55°C.
Vibration	
Operating	15 minutes along each of three axes at a total displacement of 0.025 inch (0.64 mm) p-p (4 g at 55 Hz), with frequency varied from 10 Hz to 55 Hz in one-minute sweeps. Hold 10 minutes at each major resonance, or if none exist, hold 10 minutes at 55 Hz (75 minutes total test time).
Shock	
Operating and Nonoperating	50-g, half-sine, 11-ms duration, three shocks on each face, for a total of 18 shocks.
Transit Drop (not in shipping package)	12-inch (300-mm) drop on each corner and each face (exceeds MIL-T-28800C, paragraphs 3.9.5.2 and 4.5.5.4.2).
Bench Handling	
Cabinet On and Cabinet Off	MIL-STD-810C, Method 516.2, Procedure V (MIL-T-28800C, Paragraph 4.5.5.4.3).
Topple (cabinet installed)	
Operating	Set on rear feet and allow to topple over onto each of four adjacent faces (Tektronix Standard 062-2858-00).
Packaged Transportation	
Drop	Meets the limits of the National Safe Transit Assn., test procedure 1A-B-2; 10 drops of 36 inches (914 mm) (Tektronix Standard 062-2858-00).
Vibration	Meets the limits of the National Safe Transit Assn., test procedure 1A-B-1; excursion of 1 inch (25.4 mm) p-p at 4.63 Hz (1.1 g) for 30 minutes (Tektronix Standard 062-2858-00).

Table 1-2 (cont)

Characteristics	Performance Requirements
Environmental Requirements (cont)	
EMI (electromagnetic interference)	Meets MIL-T-28800C; MIL-STD-461B, part 4 (CE-03 and CS-02), part 5 (CS-06 and RS-02), and part 7 (CS-01, RE-02, and RS-03—limited to 1 GHz); VDE 0871, Category B; Part 15 of FCC Rules and Regulations, Subpart J, Class A; and Tektronix Standard 062-2866-00.
Electrostatic Discharge Susceptibility	Meets Tektronix Standard 062-2862-00. The instrument will not change control states with discharges of less than 10 kV.
X-Ray Radiation	Meets requirements of Tektronix Standard 062-1860-00.
RACKMOUNTED INSTRUMENT	
Environmental Requirements	Listed characteristics for vibration and shock indicate those environments in which the rackmounted instrument meets or exceeds the requirements of MIL-T-28800C with respect to Type III, Class 5, Style D equipment with the rackmounting rear-support kit installed. Refer to the Standard Instrument Environmental Specification for the remaining performance requirements. Instruments will be capable of meeting or exceeding the requirements of Tektronix Standard 062-2853-00, class 5.
Temperature (operating)	−15°C to +55°C, ambient temperature measured at the instrument's air inlet. Fan exhaust temperature should not exceed +65°C.
Vibration	15 minutes along each of three major axes at a total displacement of 0.015 inch (0.38 mm) p-p (2.3 g at 55 Hz), with frequency varied from 10 Hz to 55 Hz to 10 Hz in one-minute sweeps. Hold 10 minutes at each major resonance, or if no major resonance present, hold 10 minutes at 55 Hz (75 minutes total test time).
Shock (operating and nonoperating)	30-g, half-sine, 11-ms duration, three shocks per axis in each direction, for a total of 18 shocks.

Table 1-3

Mechanical Characteristics

Characteristics	Description
STANDARD INSTRUMENT	
Weight	
With Front Cover, Accessories, and Accessories Pouch	≃12.8 kg (28.1 lbs).
Without Front Cover, Accessories, and Accessories Pouch	≃10.9 kg (23.9 lbs).
Domestic Shipping Weight	≃16.4 kg (36 lbs).
Overall Dimensions	See Figure 1-1 for a dimensional drawing.
Height	
With Feet and Accessories Pouch	190 mm (7.48 in).
Without Accessories Pouch	160 mm (6.3 in).
Width (with handle)	330 mm (13.0 in).
Depth	
With Front Cover	479 mm (18.86 in).
With Handle Extended	550 mm (21.65 in).
Cooling	Forced air circulation; no air filter.
Finish	Tektronix Blue vinyl-clad material on aluminum cabinet.
Construction	Aluminum-alloy/plastic-composite chassis (spot-molded). Plastic-laminate front panel. Glass-laminate circuit boards.
RACKMOUNTING	
Rackmounting Conversion Kit	
Weight	4.0 kg (8.8 lbs).
Domestic Shipping Weight	6.3 kg (13.8 lbs).
Height	178 mm (7 in).
Width	483 mm (19 in).
Depth	419 mm (16.5 in).
Rear Support Kit	
Weight	0.68 kg (1.5 lbs).
OPTION 1R	
Rackmounted Instrument (Option 1R)	
Weight	≃15.8 kg (34.9 lbs).
Domestic Shipping Weight	≃18.1 kg (39.9 lbs).
Height	178 mm (7 in).
Width	483 mm (19 in).
Depth	419 mm (16.5 in).

Table 1-4

Option 05 (TV Trigger) Electrical Characteristics

Characteristics	Performance Requirements
VERTICAL—CHANNEL 1 AND CHANNEL 2	
Frequency Response	
Full Bandwidth	
50 kHz to 5 MHz	Within ±1%.
Greater than 5 MHz to 10 MHz	Within +1%, −2%.
Greater than 10 MHz to 30 MHz	Within +2%, −3%. For VOLTS/DIV switch settings between 5 mV and 0.2 V per division with VARIABLE VOLTS/DIV set to CAL. Five-division, 50 kHz reference signals from a 50 Ω system. With external 50 Ω termination on a 1 MΩ input.
20 MHz Bandwidth Limit	
50 kHz to 5 MHz	Within +1%, −4%.
Square Wave Flatness	
Field Rate	
5 mV/div to 20 mV/div	±1%, 1% p-p at 60 Hz with input signal of 0.1 V.
50 mV/div	±1%, 1% p-p at 60 Hz with input signal of 1.0 V. With fast-rise step (rise time 1 ns or less), 1 MΩ dc input coupling, an external 50 Ω termination, and VARIABLE VOLTS/DIV set to CAL. Exclude the first 20 ns following the step transition and exclude the first 30 ns when 20 MHz BW LIMIT is set.
Line Rate	
5 mV/div to 20 mV/div	±1%, 1% p-p at 15 kHz with input signal of 0.1 V.
50 mV/div	±1%, 1% p-p at 15 kHz with input signal of 1.0 V.
TV (Back-Porch) Clamp (CH 2 Only)	
60 Hz Attenuation	18 dB or greater. For VOLTS/DIV switch settings between 5 mV and 0.2 V with VARIABLE VOLTS/DIV set to CAL. Six-division reference signal.
Back-Porch Reference	Within ±1.0 division of ground reference.

Table 1-4 (cont)

Characteristics	Performance Requirements
TRIGGERING	
Sync Separation	Stable video rejection and sync separation from sync-positive or sync-negative composite video, 525 to 1280 lines, 50 Hz or 60 Hz, interlaced or noninterlaced systems.
Trigger Modes	
A Horizontal Mode	All lines: Field 1, selected line (1 to n), Field 2, selected line (1 to n), Alt fields, selected line (1 to n). n is equal to or less than the number of lines in the frame and less than or equal to 1280.
B Horizontal Mode	Delayed by time.
Minimum Input Signal Amplitude for Stable Triggering[a]	
Channel 1 and Channel 2	
Composite Video	2 divisions.
Composite Sync	0.6 division. Peak signal amplitude within 18 divisions of input ground reference.
EXT TRIG 1 or EXT TRIG 2	
EXT GAIN = 1	
Composite Video	60 mV
Composite Sync	30 mV Peak signal amplitude within ±0.9 V from input ground reference.
EXT GAIN = ÷5	
Composite Video	300 mV
Composite Sync	150 mV Peak signal amplitude within ±4.9 V from input ground reference.

[a]**Performance Requirement not checked in manual.**

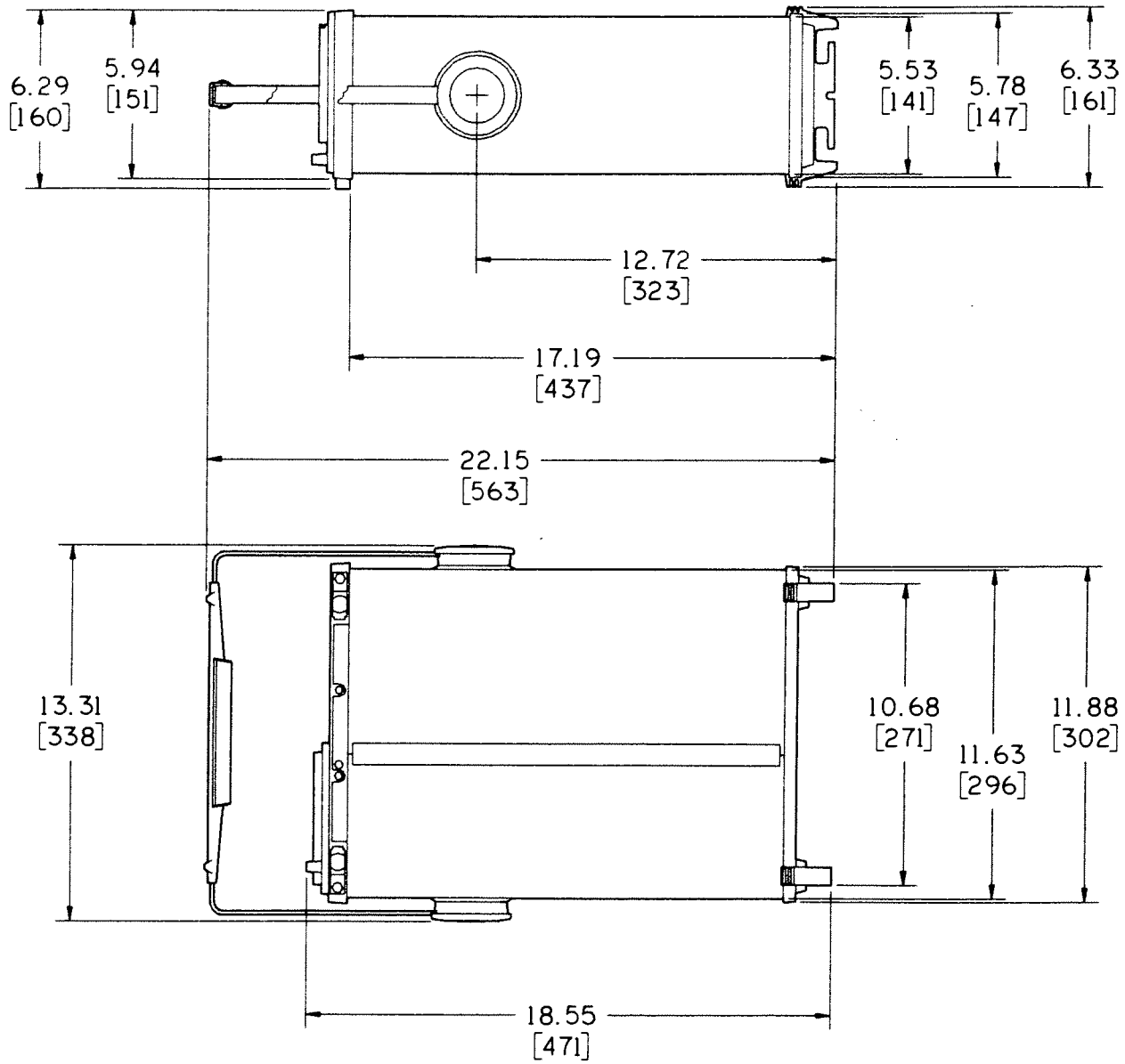


Figure 1-1. Dimensional drawing.

PREPARATION FOR USE

SAFETY

This section tells how to prepare for and to proceed with the initial start-up of the TEKTRONIX 2430A Digital Oscilloscope.

Refer to the Operators and Servicing Safety Summaries at the front of this manual for power source, grounding, and other safety considerations pertaining to the use of the instrument. Before connecting the oscilloscope to a power source, read both this section and the Safety Summaries.

CAUTION

This instrument may be damaged if operated with the LINE VOLTAGE SELECTOR switch set for the wrong applied ac input-source voltage or if the wrong line fuse is installed.

LINE VOLTAGE SELECTION

The scope operates from either a 115 V or 230 V nominal ac power-input source having a line frequency ranging from 48 Hz to 440 Hz. Before connecting the power cord to a power-input source, verify that the LINE VOLTAGE SELECTOR switch, located on the rear panel (see Figure 2-1), is set for the correct nominal ac input-source voltage. To convert the instrument for operation from one line-voltage range to the other, move the LINE VOLTAGE SELECTOR switch to the correct nominal ac source-voltage setting (see Table 2-1). The detachable power cord may have to be changed to match the particular power-source outlet.

LINE FUSE

To verify the proper value of the instrument's power-input fuse, perform the following procedure:

1. Press in the fuse-holder cap and release it with a slight counterclockwise rotation.

2. Pull the cap (with the attached fuse inside) out of the fuse holder.

3. Verify proper fuse value (see Table 2-1).

4. Install the proper fuse and reinstall the fuse-holder cap.

NOTE

A 4 A, 250 V, 5 × 20 mm Time-lag (T) fuse may be substituted for the factory-installed fuse. However, the two types of fuses are NOT directly interchangeable; each requires a different type of fuse cap.

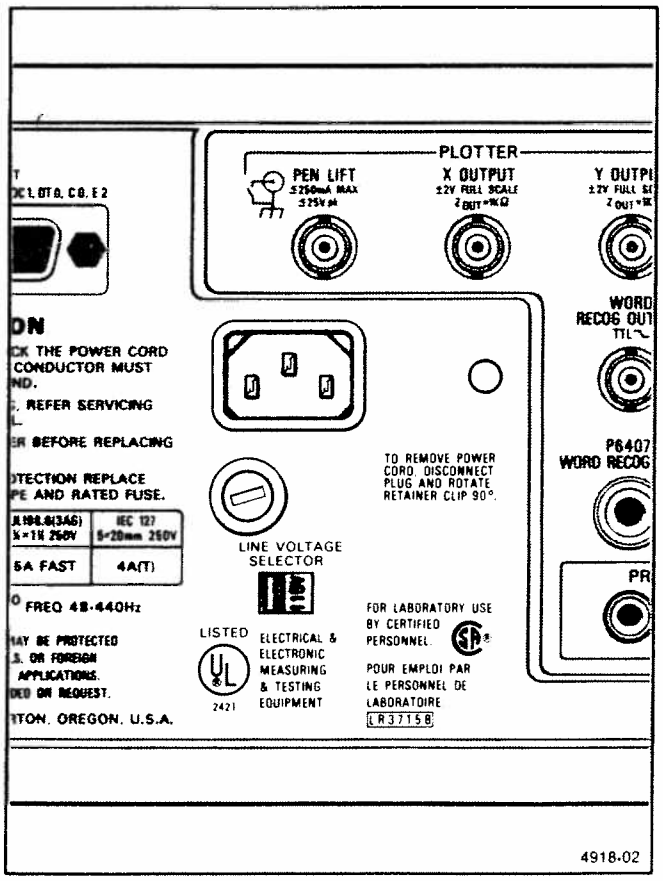
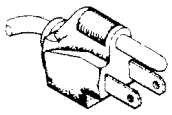
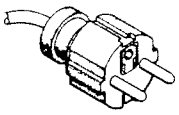
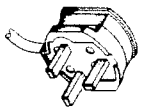
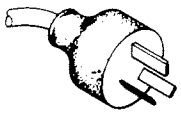
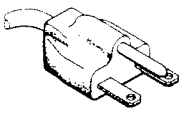
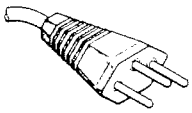


Figure 2-1. LINE VOLTAGE SELECTOR, line fuse, and power cord receptacle.

Table 2-1

Voltage, Fuse, and Power-Cord Data

Plug Configuration	Category	Power Cord And Plug Type	Line Voltage Selector Setting	Voltage Range (AC)	Factory Installed Instrument Fuse	Fuse Holder Cap	Reference Standards[b]
	U.S. Domestic Standard	U.S. 120V 15A	115V	90V to 132V	5A, 250V AGC/3AG Fast-blow (UL 198.6)	AGC/3AG	ANSI C73.11 NEMA 5-15-P UL 198.6
	Option A1	EURO 240V 10-16A	230V	180V to 250V	5A, 250V AGC/3AG Fast-blow (UL 198.6)	AGC/3AG	CEE(7), II, IV, VII IEC 83 IEC 127
	Option A2	UK[a] 240V 6A	230V	180V to 250V	5A, 250V AGC/3AG Fast-blow (UL 198.6)	AGC/3AG	BS 1363 IEC 83 IEC 127
	Option A3	Australian 240V 10A	230V	180V to 250V	5A, 250V AGC/3AG Fast-blow (UL 198.6)	AGC/3AG	AS C112 IEC 127
	Option A4	North American 240V 15A	230V	180V to 250V	5A, 250V AGC/3AG Fast-blow (UL 198.6)	AGC/3AG	ANSI C73.20 NEMA 6-15-P IEC 83 UL 198.6
	Option A5	Switzerland 220V 6A	230V	180V to 250V	5A, 250V AGC/3AG Fast-blow (UL 198.6)	AGC/3AG	SEV IEC 127

[a] A 6A, Type C fuse is also installed inside the plug of the Option A2 power cord.

[b] Reference Standards Abbreviations:

ANSI—American National Standards Institute
AS—Standards Association of Australia
BS—British Standards Institution
CEE—International Commission on Rules for the Approval of Electrical Equipment
IEC—International Electrotechnical Commission
NEMA—National Electrical Manufacturer's Association
SEV—Schweizevischer Elektrotechischer Verein
UL—Underwriters Laboratories Inc.

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POWER CORD

This instrument has a detachable three-wire power cord with a three-contact plug for connection to both the power source and protective ground. The power cord is secured to the rear panel by a cord-set securing clamp. The protective ground contact on the plug connects (through the power cord protective grounding conductor) to the accessible metal parts of the instrument. For protection against electrical shock, insert this plug into a power-source outlet that has a properly grounded protective-ground contact.

Instruments are shipped with the required power cord as ordered by the customer. Information on the available power cords is presented in Table 2-1, and part numbers are listed in "Options and Accessories" (Section 7). Contact your Tektronix representative or local Tektronix Field Office for additional power-cord information.

INSTRUMENT COOLING

To prevent instrument damage from overheated components, adequate internal airflow must be maintained. Before turning on the power, first verify that air-intake holes on the bottom and side of the cabinet and the fan exhaust holes are free of any obstruction to airflow. The scope has a thermal cutout that will activate if overheating occurs. The scope shuts down immediately with no attempt to save waveforms or front-panel conditions if a cutout happens. Power will be disabled to the scope until the thermal cutout cools down, at which time the power-on sequence is redone. The resulting loss of the last front-panel and waveform data will cause the power-on self test to fail and is indicated to the user by a failed CKSUM-NVRAM test (number 6000 in the main EXTENDED DIAGNOSTICS menu). The cause of the overheating must be corrected before attempting prolonged operation of the scope. Pressing the MENU OFF/EXTENDED FUNCTIONS button restores the scope to the normal operating mode.

START-UP

This instrument automatically performs power-up tests each time the instrument is turned on. These tests provide the highest possible confidence level that the instrument is fully functional. If no faults are encountered, the instrument will enter the Scope mode in the either ACQUIRE or SAVE Storage mode, depending on the mode in effect when it was powered off.

If tests are failed, the scope displays the Extended Diagnostics menu. If the failure is in the range of 1000-5300 and the message "HARDWARE PROBLEM—SEE SERVICE MANUAL" is displayed with the menu, see "Diagnostics" in Section 6 for more information. If the failure is in 1000-5300 range, but "RUN SELF CAL WHEN WARMED UP" is displayed, the SELF CAL procedure should be executed from the EXTENDED FUNCTIONS menu (wait for the NOT WARMED UP message to disappear from the SELF CAL menu). If failures persist after the SELF CAL is run (the "HARDWARE PROBLEM—SEE SERVICE MANUAL" message will be displayed), see "Diagnostics" in Section 6 for more information.

Failure of a test in the range of 7000 to 9300 may not indicate a fatal scope fault. Several conditions can occur that will cause a non-fatal failure of the tests. The scope will display "RUN SELF CAL WHEN WARMED UP" to indicate a SELF CAL should be performed. If SELF CAL does not clear the failure ("HARDWARE PROBLEM—SEE SERVICE MANUAL" is displayed), the scope may still be usable for your immediate measurement purposes. For example, if the problem area is in CH 2, CH 1 may still be used with full confidence of making accurate measurements. Press the MENU OFF/EXTENDED FUNCTIONS button to exit EXTENDED DIAGNOSTICS and enter Scope mode.

NOTE

The SELF CAL procedure is detailed in Section 5 of this manual. Refer to Section 6 of this manual for information on the power-up tests and the procedures to follow in the event of a failed power-up test.

A fatal fault in the operating system will cause the scope to abort. No displays are possible, and the user is notified of an abort situation only by the flashing of the Trigger LED indicators (if that is possible). Cycling the power off then back on may clear the problem, but a failure of this magnitude usually requires the scope to be referred to a qualified service person for checkout and repairs. Persistent or reoccurring failures of the power-on or self-diagnostic tests should be brought to the attention of a qualified service person at the first opportunity. Consult your service department, your local Tektronix Service Center, or nearest Tektronix representative if further assistance is needed.

POWER-DOWN

NOTE

POWER INTERRUPTION TO THE INSTRUMENT WHEN THE SELF-CALIBRATION ROUTINE IS EXECUTING INVALIDATES THE INSTRUMENT CALIBRATION CONSTANTS. Upon such an interruption, the instrument sets an internal flag denoting that SELF CAL was running at shutdown. When power is reestablished, the scope will display "RUN SELF CAL WHEN WARMED UP". When the "NOT WARMED UP" message disappears from the SELF CAL menu, the user MUST perform a SELF CAL to escape the EXT DIAG menu (the ↑ menu button MUST be used to access the SELF CAL menu—see Section 6 for more information). If failures persist after the SELF CAL is performed, refer the instrument to qualified service personnel.

For a normal power-off from the scope mode, an orderly power-down sequence retains the SAVE and SAVEREF waveforms, the current front-panel control settings, and any stored front-panel settings. If a power-off or transient power fluctuation occurs during SELF CAL, or EXTENDED CALIBRATION, or the instrument shuts-down at any time due to overheating, the normal power-down sequence is not executed. The result is loss of stored calibration constants or last front-panel control settings (or both) and a failure of the next power-on self-test (6000-6400 range). If front panel, sequencer, or stored waveform information was lost, the error will clear itself on the next power-down/power-up cycle. If calibration constants were lost the instrument will display information indicating if calibration is needed.

If power is momentarily interrupted, starting the power-off sequence, but is reestablished before the sequence completes, the scope will redo the power-on procedure. If the scope is in the middle of a waveform acquisition when power interruption occurs, the waveform data will not be saved, and the invalid waveform data display will be seen when power-on has completed. Press ACQUIRE to restart the acquisition and obtain valid waveform data.

REPACKAGING FOR SHIPMENT

It is recommended that the original carton and packing material be saved in the event it is necessary for the instrument to be reshipped using a commercial transport carrier. If the original materials are unfit or not available, then repackage the instrument using the following procedure.

1. Use a corrugated cardboard shipping carton having a test strength of at least 275 pounds and with an inside dimension at least six inches greater than the instrument dimensions.

2. If the instrument is being shipped to a Tektronix Service Center, enclose the following information: the owner's address, name and phone number of a contact person, type and serial number of the instrument, reason for returning, and a complete description of the service required.

3. Completely wrap the instrument with polyethylene sheeting or equivalent to protect the outside finish and prevent entry of harmful substances into the instrument.

4. Cushion instrument on all sides using three inches of padding material or urethane foam, tightly packed between the carton and the instrument.

5. Seal the shipping carton with an Industrial stapler or strapping tape.

6. Mark the address of the Tektronix Service Center and also your own return address on the shipping carton in two prominent locations.

THEORY OF OPERATION

SECTION ORGANIZATION

This section of the manual is divided into three subsections, with each subsection increasing in detail. The first subsection is the "Simplified Block Diagram Description" which contains a general summary of instrument operation by diagram. A simplified block diagram accompanies the text. Subsection two is the "Detailed Block Diagram Description" which discusses the circuit functions in greater detail and provides a more in-depth look at the acquisition system. A detailed block diagram is located in the foldout pages at the rear of this manual. Generally, both block diagram descriptions follow the signal-flow path as much as possible and not the schematic diagram number order as is done in the "Detailed Circuit Description".

Subsection three is the "Detailed Circuit Description" which discusses the circuitry shown in the schematic diagram foldouts, also located at the rear of this manual. The schematic diagram number associated with each description is identified in the text and is shown on the block diagrams. For best understanding of the circuit being described, refer to the appropriate schematic diagram and the block diagrams. The order of discussion in the circuit descriptions follows the schematic diagram number order.

INTEGRATED CIRCUIT DESCRIPTIONS

Digital logic circuits perform most of the functions within the instrument. Functions and operation of the logic circuits are shown using logic symbols and terms. Most logic functions are described using the positive-logic convention. Positive logic is a notation system in which the more positive of the two logic levels is the HI (or 1) state; the more negative level is the LO (or 0) state. Voltages that constitute a HI or a LO state vary between specific devices. Refer to the device manufacturer's data book for specific electrical characteristics or logical operation of common parts.

The functioning of linear integrated circuit devices in this section is discussed using waveforms or other techniques such as voltage measurements and simplified diagrams, where required, to illustrate their operation.

SIMPLIFIED BLOCK DIAGRAM DESCRIPTION

This discussion is of the block diagram shown in Figure 3-1.

Attenuators and Preamplifiers (diagram 9)

ATTENUATORS. The Attenuators are settable to 1X, 10X, or 100X attenuation, to reduce the input signal level to within the dynamic range of the Preamplifiers. Input coupling for the signal to the Attenuators may be either AC or DC with 1 MΩ termination or DC with 50 Ω termination. Attenuator and coupling switching are controlled by the System μP using register-activated magnetic-latch switches.

PREAMPLIFIERS. The Preamplifiers provide switchable gain setting and buffering of the attenuated input signal. Single-ended input signals are converted to double-ended (differential) output signals. Variable Vertical Mode gain, vertical position, and DC Balance are controlled by input signals to the Preamplifiers. The System μP-controlled gain in combination with the switchable attenuator settings allow the complete range of available VOLTS/DIV switch settings from 2 mV to 5 V to be obtained. Trigger pickoffs provide a sample of the input signal to the trigger system for use as a triggering signal source. With the Video Option installed, a Channel 2 pickoff signal is supplied from the Preamplifiers as a trigger signal source. Also, a Channel 2 Offset signal used to control the back-porch clamping is provided from the Video Option to the Channel 2 Preamplifier.

Peak Detectors and CCD/Clock Drivers (diagram 10)

PEAK DETECTORS. Additional buffering of the signal to the CCDs is provided by the Peak Detectors for all acquisition modes. The bandwidth of the input amplifiers of the Peak Detectors is switchable for FULL, 50 MHz, and 20 MHz bandwidths. In Envelope acquisition mode, dual min-max Peak Detectors detect and hold the minimum and maximum peak signal amplitudes that occur between sampling clocks. Those min and max signal values are then applied to the CCDs for sampling. Control data from the System μP controls the bandwidth selection, and peak detector clock signals multiplex the signal samples from the Peak Detectors to the CCDs. A calibration signal input is provided to the Peak Detectors for use in automatic calibration and diagnostic testing of the acquisition system.

Common-mode adjust circuitry on the output of the Peak Detectors is used to control the overall gain of the Peak Detector/CCD acquisition subsystem. Using digital signals to the DAC system, analog voltages are generated that set the gain of the Common-mode adjust amplifiers. These amplifiers monitor the dc common-mode level of the Peak Detector outputs and match it to the control gain level set by the System μP. That dc level sets the CCD signal gain.

CCD/CLOCK DRIVERS. The CCDs are fast analog shift registers that can hold more that enough samples to fill the complete waveform record of 1024 samples per channel. The extra samples are used to account for the uncertainty of the trigger point location in the 32 samples stored in the input register. Once a trigger occurs, the samples not needed to fill the waveform records are basically discarded. For fast signals, waveform samples are stored very rapidly and then shifted out at a rate that can be handled by the A/D Converter. When the sample rate is slow enough to allow direct conversion of the input samples, a Short Pipeline mode is used to shift samples directly through the CCD registers. The Clock Driver portion of the devices produces the phase clocks that shift the analog data through the CCD registers. Other clocks used to sample the signal and transfer the samples into and out of the CCD arrays are generated in the CCD Clock and System Clock circuits (diagrams 11 and 7 respectively).

CCD Output (diagram 14)

The differential signals from both sides and both channels of the CCD arrays are combined and multiplexed onto a single data line to the A/D Converter. The output clocking is referenced to the sample and phase clocks to maintain the correct data timing relationships of the samples. Waveform data samples are therefore stored in the correct Acquisition Memory locations after being digitized.

A/D Converter and Acquisition Latches (diagram 15)

A/D CONVERTER. The combined samples of analog signals are converted to eight-bit data bytes by the A/D Converter. In Envelope Mode, the data bytes are applied to two magnitude comparators, along with the previous maximum and minimum data bytes to determine if it is greater in magnitude than the last maximum or minimum. If a new data byte is greater, the new data byte is latched into the Acquisition Latches; otherwise, latching does not occur. Clocking to direct the signals into the Acquisition

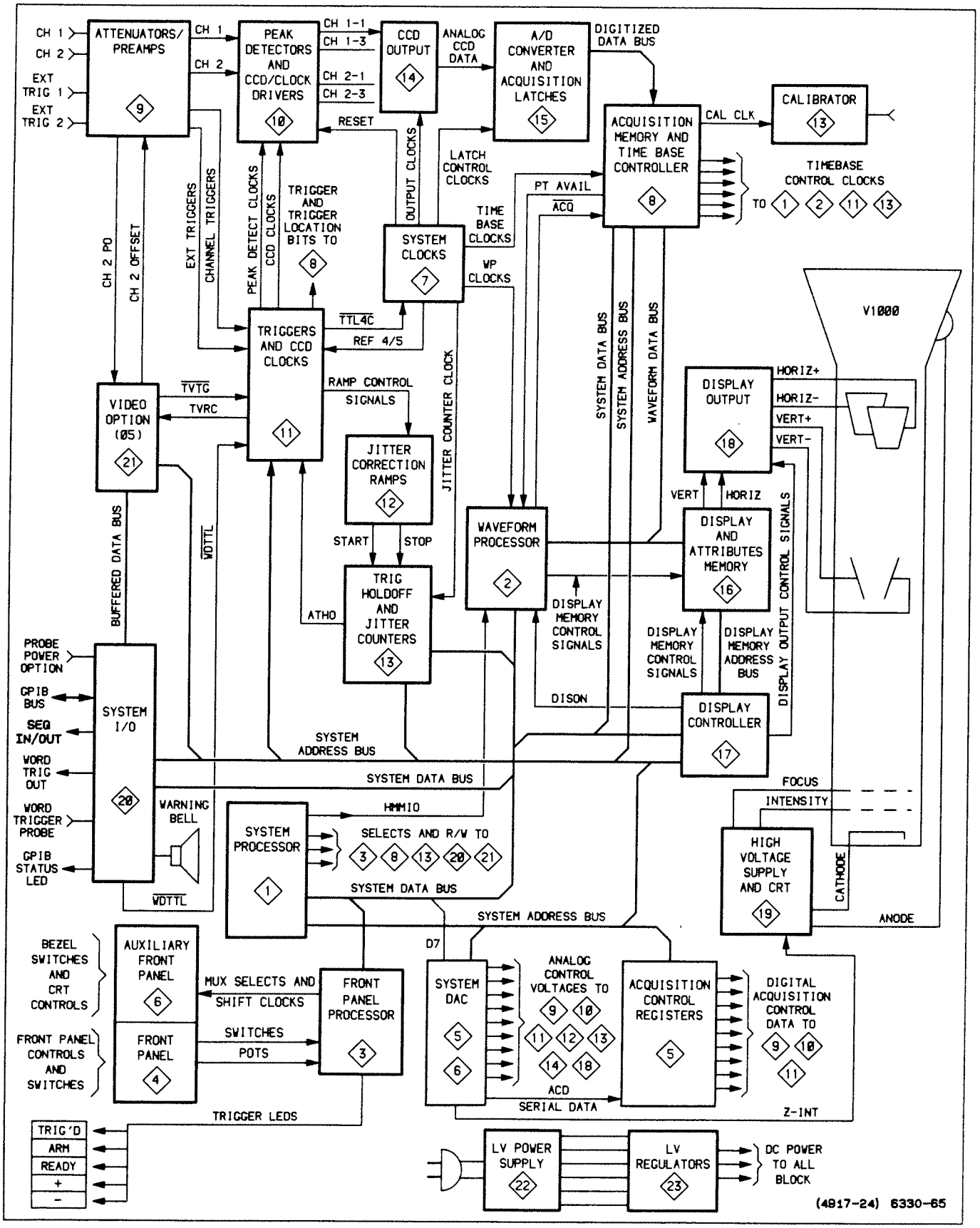

Figure 3-1. Simplified block diagram.

Latches comes from the System Clock circuit and is referenced to the Output Clocks to maintain the correct data input to the magnitude comparators for making the Envelope min-max comparisons.

ACQUISITION LATCHES. For Normal and Average acquisitions, the data bytes are passed directly through the Acquisition Latches to the Acquisition Memory where they are stored temporarily before transfer to Waveform Processor Data Bus and the Waveform Processor Save Memory. The Envelope acquisition waveform bytes in the Acquisition Latches are the maximum and minimum data point values that occurred in the sampling interval. When the SEC/DIV setting reaches the maximum sampling rate, only one min-max pair is present during a sampling interval; and, in that case, the Envelope data byte comparisons are done by a firmware routine as the data is transferred from the Save Memory to the Display Memory.

Time Base Controller and Acquisition Memory (diagram 8)

ACQUISITION MEMORY. Digitized waveform data bytes are transferred from the Acquisition Latches to the Acquisition Memory under control of the Time Base Controller. The data is temporarily stored here before moving to the Waveform Processor Save Memory under control of the Waveform Processor.

TIME BASE CONTROLLER. The Time Base Controller, under direction of the System μP, monitors and controls the acquisition functions. When the pretrigger samples are obtained, the digitization process is started. Samples are counted to store the correct number in the Acquisition Memory, and the trigger point is properly located in the waveform record. Among the various tasks done by the Time Base Controller, Clock signals generated by the Time Base Controller provide the acquisition rate, the calibrator frequency, and enable the Trigger circuitry to accept a trigger after the pretrigger data is acquired.

Waveform Processor (diagram 2)

The Waveform Processor performs the high-speed data-handling operations required to produce and update the CRT displays. Waveform data is transferred from the Acquisition Memory to a "Save" Memory in the Waveform μP work space. Waveforms may be digitally added, multiplied, or averaged, as part of the display processing that the Waveform Processor does before transferring the data to the Display Memory. The Save Memory is kept alive during periods of power-off by the battery-backup system. This back-up system holds the Save waveforms, the reference waveforms and/or front-panel setups for up to three years. The waveform μP memory space and all devices on the Waveform μP address bus are addressable by the System μP via the Bus Connect circuitry for I/O operations.

The Bus Connect circuitry includes logic gating that arbitrates when the Waveform μP memory space (RAM) and addressable devices are under control of the System μP. The System μP may gain control by a BUS REQUEST to which the Waveform μP issues a BUS GRANT signal; or if the Waveform μP is held reset, the System μP issues a BUSTAKE signal. The BUSTAKE is used when the System μP writes a waveform display task list into the Waveform μP Command RAM space. When the reset is then removed from the Waveform μP, it does all the waveform data processing tasks given to it to do by the System μP without further need of System μP action.

Display and Attributes Memory (diagram 16)

The 512 data points to be displayed out of the 1024 data-point record are transferred to the Display Memory from the Waveform μP Save Memory after any required processing such as adding, subtracting, multiplying, or interpolating is done. Subsequent refreshes of the display are then continually made from data stored in the Display Memory, and that memory is only updated as necessary to display different waveforms or portions of the waveform record (a new horizontal position or new waveform called up for display). The Attributes Memory holds all the VOLTS/DIV and SEC/DIV scale factors for each of the waveforms displayed. Readouts of that data are also displayed on the crt.

Display Controller (diagram 17)

The Display Control System controls the display of the waveforms and readouts. Data bytes stored in the Display Memory are read out and D-to-A converted into vertical and horizontal current signals used to generate the waveform dots and readout characters. State-machine circuitry under control of the System μP performs all the display tasks assigned including control of the Z-Axis. The System μP and the Waveform μP are therefore free to carry on with other functions until it becomes necessary to make a display change (such as a menu or display mode change or a waveform data update). Display state-machine clocks are generated from the Time Base Controller 5 MHz clock signal.

Display Output (diagram 18)

Horizontal and vertical signal current from the Display Controller are converted into the deflection voltage signals used to drive the crt deflection plates by the Display Output circuitry. Vector generation circuitry provides a choice of either connected waveform dots (vectors on) or a dots-only waveform display. Display switching circuitry connects the correct deflection signals to the vertical and horizontal output amplifier for YT (vertical signal versus time), XY (horizontal signal versus versus vertical signal), or readout data. Dynamic offset correction of the vertical and horizontal output amplifiers is provided that minimizes trace shift due to intensity changes.

System Processor (diagram 1)

The System μP, under program direction, controls all the functions of the scope and coordinates the functions of the two other microprocessors (the Front-Panel μP and the Waveform μP). The System μP has a 16-bit address bus and a separate 8-bit data bus. No multiplexing of the data bus is required. Addresses are decoded to access the memory-mapped devices on the data bus, and control signals generated by the System μP control communication between the μP and the bus devices. An extensive interrupt circuit enables devices on the bus to request servicing when necessary to get new instructions or take other action. A power-up reset circuit permits an orderly power-on and power-off sequence of the System μP.

Permanent programming used to control the Operating System resides in the System ROM. The System ROM contains one 16K byte × 8-bit memory device and four 64K byte × 8-bit memory devices for a total of 272K bytes of memory. A page-switching scheme is used to permit the System μP to access all the available memory addresses of ROM.

System RAM consists of a single 32K byte × 8-bit memory device. Data needing short-term storage (data used for performing various control functions) as well as data needing long-term storage (calibration constants, the front-panel setup at power down, etc.) are stored in this nonvolatile RAM. A battery-backup system maintains the data in this memory during power off.

NOTE

Although all the data in this memory device is backed up and is, therefore, nonvolatile, that part of the System RAM reserved for data that NEEDS to be backed up is referred to as NVRAM throughout this section. Parts of System RAM that do NOT NEED backing up are referred to as volatile RAM or just RAM.

Front Panel Processor (diagram 3)

The Front Panel μP is a special-purpose device used to respond to switch and control changes. When a control changes, the Front Panel μP informs the System μP so that the operating state may be altered to match the requested change. Potentiometer controls are digitized to provide the necessary change data to the System μP. The System μP notes the control that changed, the amount and direction of change (if a pot), and sends out the necessary commands to make the change. New settings are updated in the nonvolatile RAM so that they will be available in the event of a power-off. On a power-on, the Front-Panel μP receives instructions as to how the switches are to be interpreted and then begins scanning the front panel, watching for a control to change. The System μP is then free to carry on with other functions.

Front Panel (diagram 4) and Auxiliary Front Panel (diagram 6)

All the buttons and knobs of the Front Panel and Auxiliary Front Panel are "soft" controls and do not directly activate a circuit function. This fact allows the switch functions and menu labels to be changed (especially the bezel buttons of the Auxiliary Front Panel which are used to make menu selections) as necessary. Buttons may be defined by the System μP to be push-push on-off, momentary contact, continuous, or toggle switches. Control changes are monitored by the Front Panel μP. Potentiometer controls are digitized; and when a change occurs, the amount and direction of change is sent to the System μP to make the appropriate operational changes. Push buttons that are pressed are interpreted as to what type of switch action occurred (from the switch-type definition list) and that information is sent to the System μP to make the appropriate operational changes.

All the buttons and knobs located to the right of the crt (facing the scope) are monitored via circuitry of the Front Panel. The Auxiliary Front Panel contains the circuitry required to monitor the bezel buttons (menu selection buttons), the push buttons, and the INTENSITY knob (all located directly beneath the crt). Probe coding for the vertical-channel and external-trigger BNC connectors and the 50 Ω overload circuits for CH 1 and CH 2 are also monitored via the Auxiliary Front Panel circuitry.

System Dac (diagrams 5 and 6)

The System Dac is used in normal operation to set the various analog control voltages throughout the instrument. Such things as preamplifier gain, vertical position and centering, trigger levels, holdoff time, common-mode adjust, scale illumination, intensity of the various crt displays, and CCD positions offsets are all controlled by the System μP via the System Dac. Digital values representing the analog voltage levels required for the various controls are written to the digital-to-analog converter (DAC) input registers where they are converted to analog voltage levels at the inputs to the Sample-and-Hold circuits. The Sample-and-Hold circuits maintain a fixed output voltage to the controlled circuit between updates by the System μP.

For calibration and diagnostic purposes, the System Dac is used to send known voltage levels to various circuits. Those levels may then be adjusted to remove offsets and set gain levels to achieve analog calibration or to test the gains and offsets for diagnostic purposes.

Acquisition Control Registers (diagram 5)

The Acquisition Control Registers are the digital control interface between the System μP and the switchable acquisition circuitry. Switching data is written to the

Registers to control the setup of the Peak Detectors, the A/B Trigger Generator, the Trigger Logic Array, and the Phase Clock Array. Additional decoding circuitry produces clocking signals used to load controlling data into Attenuator Register, the CH1 and CH2 Preamplifiers, and the A/B Trigger Generator.

Triggers and CCD Clocks (diagram 11)

TRIGGERS. The Trigger circuits detect when a trigger meeting the setup conditions occurs. Triggering signals are selectable by the A/B Trigger Generator from a choice of the following sources: CH 1, CH 2, EXT 1, EXT 2, and LINE. The Trigger Logic Array makes possible the further choices of TV Trigger ($\overline{\text{TVTG}}$), WORD Trigger ($\overline{\text{WDTTL}}$), or A and B Trigger. Upon receiving a valid trigger, the acquisition in progress is allowed to complete. Conditions for triggering, such as Level, Slope, Coupling, and Mode, are determined by the A/B Trigger Generator. Other triggering conditions such as delay by time, delay by events, and A and B Trigger are decided by the Trigger Logic Array which produces the output gates signaling a trigger event. The System μP sets up the operating modes for the A/B Trigger Generator and the Trigger Logic Array via the Acquisition Control Registers (diagram 5). Control signals to the Jitter Correction Ramps (RAMP and $\overline{\text{RAMP}}$) are generated by the Trigger Logic Array to start measuring the time between the sample clock and the trigger event. That time difference is used to correctly place the samples when repetitive sampling is used.

CCD CLOCKS. The CCD Clocks (used to move data into and out of the CCDs), the Peak Detector Clocks, the ramp-switching signals to the Jitter Correction Ramp circuits, and the trigger location bits (needed to place the trigger position with respect to the waveform data) are all generated by the Phase Clock Array. A master clock signal of either 200 MHz or 250 MHz is generated by the Phase-Locked Loop circuit and voltage-controlled oscillator. The master clock frequency needed is determined by the sampling rate at a particular SEC/DIV switch setting. Frequency dividers in the Phase Clock Array reduce the master clock frequency to the lower rates of the output clocks as determined by the System μP via the Acquisition Control Registers (diagram 5).

Jitter Correction Ramps (diagram 12)

The Jitter Corrections Ramps work in conjunction with the Jitter Counters to detect and measure the time difference between a trigger event (that occurs randomly) and the sample clock. That time difference is used to correctly place sampled data points into the waveform record when those samples are acquired on different triggers (repetitive sampling). Two ramp generators are used, so two time measurements are made. The System μP will determine which measurement is the one actually used. The RAMP and $\overline{\text{RAMP}}$ signals from the Trigger circuits control the start and stop of the ramp signals while the SLRMP1 and SLRMP2 signals control switching between the fast-charging current source and slow-discharging current source. Since the SLRMP signals are related to the sample clock, the amount of charge stored from the fast-charging current source before switching to the slow ramp occurs is a measure of the time difference between the trigger and the sample clock. The Jitter Counters start counting when the SLRMP signal switches to the slow ramp, and they are stopped when a comparator circuit determines that the ramp level has discharged to a fixed reference level.

Trigger Holdoff and Jitter Counters (diagram 13)

TRIGGER HOLDOFF. The A Trigger Holdoff circuit prevents the A/B Trigger Generator (diagram 11) from recognizing a new trigger event for a certain amount of delay time after an acquisition has been completed. The delay allows all of the data handling of the acquired samples to be completed before starting a new waveform acquisition. Minimum holdoff time is dictated by the SEC/DIV switch setting. A front-panel HOLDOFF control permits the user to increase the holdoff time as an aid in improving triggering stability on certain signals.

JITTER COUNTERS. The Jitter Counters (one for RAMP1 and one for RAMP2) start counting the 8 MHz clock when a START signal is received from the Jitter Counter Ramps switching circuit. That start occurs at the beginning of the slow ramp discharge. When the level of the slow ramp decreases to the fixed reference level, a STOP signal generated by a comparator in the Jitter Counter Ramps circuit halts the count. The 8-bit count bytes held in the Jitter Counters are then read by the System μP via address-selected bus buffers as two measures of the time difference between the trigger point and the sample clock. Since the timing between the two ramps is not identical (but both times are referenced), one measurement may have been made with better slope characteristics than the other (over a more linear portion of the discharge curve). The count producing the least ambiguity is used by the System μP to correctly position the waveform samples in the memory when repetitive sampling is done.

Calibrator (diagram 13)

The Calibrator circuitry shapes the CALCLK signal from the Time Base Controller to produce a signal with a faster rise and fall time and very precise amplitude. Frequency of the Calibrator signals changes (within limits) as the SEC/DIV switch changes. Signal amplitude is 400 mV (starting from zero), and the effective output impedance is 50 Ω.

System Clocks (diagram 7)

The System Clocks circuitry produces the fixed-frequency clock signals used throughout the scope. A 40 MHz crystal-controlled oscillator circuit produces the master clock signal that is divided down to provide the various system clocks that are needed. Some of the special clocks generated are the CCD Data Clocks, used primarily to switch the analog signal samples from the CCDs to the input of the A/D Converter and switch the converted data bytes to the Acquisition Latches. The reference frequency (either 4 MHz or 5 MHz) to the Phase Clock Array in the CCD Clock circuitry (diagram 11) is also selected by the System Clocks circuitry. A Secondary Clock Generator state-machine circuit produces three clocking signals to the Waveform μP to control the activity of that device.

High Voltage and CRT (diagram 19)

The High Voltage and CRT circuitry provides the auxiliary voltages needed by the CRT to produce a display. Focus, intensity, trace rotation, astigmatism, geometry, Y-Axis alignment, heater, and cathode-to-anode accelerating voltage are all provided by the various circuits included. These circuits are: the High Voltage Oscillator, the High Voltage Regulator, the +61 V Supply, the Cathode Supply, the Anode Multiplier, the DC Restorer, the Focus and Z-Axis Amplifiers, the Auto Focus Buffer, and the various crt adjustment potentiometers.

System I/O (diagram 20)

The System I/O circuits provide the interfaces between the scope and external devices that may be connected. Included in the interfaces is a standard general-purpose interface bus (GPIB) that permits two-way communication between the System μP and a GPIB controller or other IEEE 488-1980 compatible GPIB devices. The GPIB interface permits waveforms, front-panel setups, and other commands or messages to be both sent and received by the scope.

A second interface is the Word Trigger circuitry used to control the word recognization patterns of the optional Word Recognizer probe. All firmware and hardware (including connectors) required for use of the Word Recognizer probe is supplied as standard equipment. A trigger produced by the probe ($\overline{\text{WDTTL}}$) may be internally selected to trigger the scope, and it may be supplied to an external device via the WORD TRIG OUT connector on the rear panel.

Three BNC connectors comprise a third interface which is used to help control the AutoStep Sequencer. SEQUENCE IN and STEP IN are inputs that accept TTL-compatible signals for starting a sequence and stepping a paused sequence, respectively. SEQUENCE OUT is an output that issues a TTL-compatible signal upon the completion of a sequence. For all three inputs/output, the negative edge of the TTL signal triggers/signals the event.

Probe power connectors are an option for supplying the power requirement of active Tektronix probes. The option consists of two probe power connectors installed on the rear panel of the scope.

An audible alarm bell is provided to give the user warning of events that may require attention. GPIB errors are typical events that produce the warning bell so that a user may take notice of the error event. Another instance that causes the warning bell is an attempted call-up of an invalid operating condition from either the front panel or the GPIB. Typically, warning and error messages are also displayed on the crt to aid the user in determining the nature of the problem.

Video Option (diagram 21)

The Video Option (Option 05) consists of additional installed hardware that enhances triggering on and viewing of composite video signals. Option 05 circuitry contains both Video Processing and Trigger Generation circuitry. Video Processing stabilizes the input signal and separates the video sync signals (horizontal and vertical sync pulses) from the video signal. A wide range of video signal levels are accommodated by using automatic gain control of the amplifier that sets the level into the sync separator. Separated sync pulses are counted to permit the user to select the line number that will produce a trigger event. Back-porch clamping is available for the Channel 2 display, and when used, it removes or reduces the level of power-supply hum that may be accompanying the composite video signal display.

Low Voltage Power Supply (diagram 22)

The majority of the low voltages required to power the scope are produced by a high-efficiency, switching power supply. Input ac power of either 115 V or 230 V within the frequency range of 48 Hz to 400 Hz is rectified and used to drive a switching circuit at a frequency of about 50 kHz. A smaller power transformer is possible with the higher

frequency switching, and much more efficient power transfer is possible. Regulation of the power to the switching transformer is controlled by a pulse-width modulator (PWM) using feedback from one of the rectifier transformer outputs. The PWM controls the on-time of the switching transistors that deliver energy to the transformer primary winding. If the feedback voltage is too low, more energy is supplied by turning on the switching transistors longer. Automatic overvoltage and overcurrent sensing circuits shut down the switching if either type of overload occurs. The ac input has an interference filter, primary line fusing, and a thermal cutout that shuts down the power supply in the event of overheating.

Low Voltage Regulators (diagram 23)

The Low Voltage Regulators remove ac noise and ripple from the rectified output voltages from the power transformer. Each regulator automatically current limits the output and prevents the current from exceeding the normal power limits. This limiting prevents further possible damage to the power supply or other scope circuitry. Each of the power supply regulators controls its output voltage level by comparing the output to a known voltage reference level. To maintain stable and well-regulated output voltages, highly stable reference voltages are developed for making the comparisons.

DETAILED BLOCK DIAGRAM DESCRIPTION

INTRODUCTION

This description of the Detailed Block Diagram (found in the "Diagrams" section of this manual) provides an overview of the operation of many of the circuits and their functions. The emphasis is on the acquisition system, and a "signal flow" approach is used as much as possible. No attempt is made in this discussion to specifically cover all the circuitry shown on the block diagram, though most is covered in general as it relates to those areas described in detail. The components discussed for each schematic diagram are generally outlined in functional blocks on their corresponding schematic diagram. These "function blocks" also appear on the "Detailed Block Diagram" within outlined areas that correspond to the schematic diagrams. Refer to both the Detailed Block Diagram and the Schematic Diagrams as needed while reading the following description.

INPUT SIGNAL CONDITIONING AND ANALOG SAMPLING

Signals applied to the CH 1 and CH 2 input connectors are coupled to their respective attenuators. The CH 1 and CH 2 attenuators (diagram 9) are settable for 1X, 10X, and 100X attenuation, with input-coupling mode choices of AC, DC, and GND. Input termination resistance of either 1 MΩ or 50 Ω is selectable with the DC input coupling choice. The attenuation factor, input coupling mode, and input termination settings for each input are controlled by the System μP (diagram 1) through the Attenuator Control Register (diagram 9), based on the Front Panel control settings chosen by the user.

The attenuated CH 1 and CH 2 signals are buffered by their respective Preamps (diagram 9) before they are passed on to the Peak Detectors. Preamplifier gain is controlled by the System μP using a serial control-data line via the Miscellaneous Register (diagram 1) and the DAC MUX (digital-to-analog converter multiplexer) Select circuit. Serial data is clocked into the internal register of the Preamps via the Control Register Clock Decoder (diagram 5). As with the attenuator settings, the gain-setting data output by the System μP depends on the user-selected Front Panel control settings. The range of attenuation settings coupled with the gain-control settings of the Preamps allows the complete range of available VOLTS/DIV switch settings (from 2 mV to 5 V) to be obtained.

In addition to signal gain and input signal buffering, the Preamps convert the single-ended input signal to a double-ended differential output signal that improves the common-mode rejection ratio. Input ports used to control the DC Balance, the Variable VOLTS/DIV gain, and the Vertical Position are provided in the Preamp stages. Analog control voltages to these inputs are developed by the System DAC and routed to the Preamps via the DAC MUX/0 Sample-and-Hold circuit (diagram 5). Trigger pickoff circuits in each Preamp provide a sample of the vertical signal that may be selected by the Trigger circuitry as the trigger signal source.

The differential output signals from the Preamps are applied to their corresponding Peak Detector. Input amplifiers within the CH 1 and CH 2 Peak Detectors (diagram 10) buffer the applied signals and provide a constant input resistance of about 75 Ω to those signals. The

buffered signals are then either amplified further or "peak detected" and amplified, depending on the acquisition mode setting.

The System μP controls the operating mode of the Peak Detectors via control data writes to the Acquisition Control Registers (diagram 5). Some of the resulting digital outputs drive control inputs on the Peak Detectors, while others control the enabling and disabling of the Peak Detector clock signals from the CCD (charge-coupled device) Phase Clock Generator (diagram 11). The effect of this combined action depends on the acquisition mode selected. For NORMAL and AVG (average) acquisition modes, the peak-detect function of the Peak Detectors is disabled and the input signals are only amplified for application to the CCDs. For ENVELOPE mode, however, the peak-detect portion of the internal circuitry is enabled, and the maximum and minimum signal amplitude levels that occur during a sampling interval are detected. Those maximum and minimum values are then amplified and passed on to the CCDs.

Other inputs to the Peak Detectors control the input amplifier Bandwidth Limit setting (FULL, 50 MHz, or 20 MHz) and provide for the application of the calibration signal used for instrument calibration and self diagnostics. Calibration voltage levels applied to the Peak Detectors are generated by the System μP via the System DAC (diagram 5), DAC MUX 3, and the Cal Ampl circuit (diagram 6). The System μP selects between either the normal signal inputs or the calibration signal inputs using data written to the Acquisition Control Registers. The bandwidth of the input amplifiers of the Peak Detectors is also controlled via the Acquisition Control Registers, based on the user-selected Bandwidth Limit setting.

The signal-sampling process of CCDs (diagram 10) requires that two differential-signal pairs be available from each Peak Detector. Each CCD will use one or both output pairs as input signals, depending on the analog sampling mode. Briefly, the FISO sampling mode (fast-in, slow-out) requires 1056 samples to be shifted into each CCD. Half of the samples for a channel (528) are shifted into one side of one CCD, and the other half are shifted into the second side of the same CCD. The first pair of differential outputs are shifted into a pair of internal registers in one half of the CCD on the same phase of the sample clock. The second pair of differential output signals are identical to the first pair. This second pair is shifted into the two internal registers of the second half of the CCD on the opposite phase of the same sample clock used to shift in the first pair of output signals. This method of sampling produces a maximum sampling rate of 200 megasamples per second using a 100 MHz clock frequency. A second sampling method, called the "Short-Pipeline" mode, uses only half of each CCD and samples only one of the output signal pairs from the Peak Detectors. FISO and Short-Pipeline analog sampling modes are both discussed later in this description and in the "Time Base Controller and Acquisition Memory" portion of the Detailed Circuit Description.

Each differential output signal pair from the Peak Detectors is monitored by a separate Common-Mode Adjust circuit. These Common-Mode Adjust circuits (diagram 10) compare the common-mode voltage against the common-mode adjust voltage output by the System DAC. The common-mode adjust voltage is set by the System μP to control the overall gain of the CCDs based on calibration constants stored in the System μP nonvolatile RAM (diagram 1) as the result of a self calibration.

The common-mode adjusted signal pairs (two per Peak Detector) are applied to their corresponding side of the CCDs. There, they are analog sampled. The process consists of converting the analog voltages into individual, charged "packets" having a charge directly related to the voltage amplitude of the signal sample.

At SEC/DIV settings of 50 μs and faster, the signals are sampled at a faster rate than the maximum conversion rate of the A/D Converter. This mode is the "fast-in, slow-out" (FISO) sampling mode. When enough samples have been stored in the parallel register array of the CCDs to fill a waveform record after a trigger event, sampling stops (fast-in). The stored analog samples are then clocked out of the CCD arrays at a rate that the A/D Converter can handle (hence, slow-out). For SEC/DIV settings slower than 50 μs, the Short-Pipeline sampling mode is used. In Short-Pipeline, the acquisition rates are slower than the maximum digitizing rate of the A/D Converter. Samples are taken at a constant rate in Short-Pipeline mode, but to account for the slower acquisition rates needed for each successively slower SEC/DIV setting (from 100 μs to 5 s), samples that are not needed are ignored. Short-Pipeline mode is so named because the samples do not fill all of the parallel registers within the CCDs, but take a "short" serial path through the CCDs (see the "Detailed Circuit Description" for more information).

Analog samples are continually clocked into the CCDs by the output clocks of the CCD Phase Clock Array until a valid trigger is recognized by the Acquisition System. The Time Base Controller (diagram 8) provides the reference frequency to the CCD Phase Clock Array via the Reference Frequency Selector and the Phase-Locked Loop circuit (diagram 11). Dividers in the CCD Phase Clock Array synthesize the clocking frequencies needed for saving the acquisition at the different SEC/DIV settings. The Time Base Controller also controls the acquisition mode (FISO, Short-Pipeline, or ROLL) and the storing of acquired samples into the Acquisition Memory.

At this point in the sampling process the Time Base Controller is waiting for a triggering gate from the Trigger System to complete the acquisition (see "Acquisition Process and Control"). Extra pretrigger samples acquired while waiting for a trigger will either be flushed out of the output wells of the CCDs (FISO mode) or converted and stored in the circular Acquisition Memory (diagram 8), but not moved to the Save Memory (Short-Pipeline mode). The exception to this is ROLL mode; a trigger event is not required for ROLL acquisitions. Digitized data is moved through the Acquisition System to continually update the display with each waveform data point acquired.

ACQUISITION PROCESS AND CONTROL

To do a waveform acquisition, the System μP addresses the internal instruction registers within the Time Base Controller and then writes the setup data into the registers. The setup data defines the acquisition mode (FISO, Short-Pipeline, or ROLL), the time base clocking rate (for the SEC/DIV setting), the trigger position, and other instructions for how an acquisition is to be made.

Once the setup data is in the Time Base Controller instruction registers, the System μP generates a strobe that starts the acquisition and turns control of the Acquisition System over to the Time Base Controller. The Time Base Controller then begins monitoring the CCD Phase Clocks to determine when an adequate number of analog samples are in the CCDs to fill the pretrigger requirements. When those samples have been obtained, the Time Base Controller enables the Trigger Logic Array (diagram 11) to accept a trigger and begins looking for a triggering gate from the Trigger Logic Array (via the CCD Phase Clock Array). This waiting period is the continuous analog sampling state for the CCDs referred to at the end of the "Input Signal Conditioning and Analog Sampling" discussion.

With the Trigger System enabled, the A/B Trigger Generator (diagram 11) monitors the selected source for a signal that meets the analog triggering criteria. Source selection and triggering criteria are controlled by serial data writes from the System μP (via the Data MUX Select circuit) based on the Front Panel settings selected by the user. When the analog triggering conditions are met, the A/B Trigger Generator gates the Trigger Logic Array. Once enabled, the Trigger Logic Array monitors other triggering criteria (Trigger Mode, Delay Time setting, Hold Off timing, etc.) to determine the actual "Record" trigger point in the waveform data record. The System μP writes data control bits defining the Trigger Logic Array operating mode to the internal registers of the Trigger Logic Array via the Acquisition Control Registers.

When the Trigger Logic Array determines that the additional triggering conditions are also met, the Time Base Controller is gated (via the CCD Phase Clock Array), and the post-trigger samples are taken (if required) to finish the acquisition. How the acquisition is completed after the trigger point is determined, depends on the analog sampling mode in effect.

FISO Mode

For FISO mode, the CH 1 and CH 2 CCDs must each hold 1024 samples (plus some extra samples used in locating the correct trigger point). After the trigger event, the Time Base Controller counts a sampling clock from the CCD Phase Clock Generator to determine when enough post-trigger samples have been shifted into the CCDs to finish the acquisition. When the record is filled, the analog sampling process is stopped by disabling the sampling clocks output by the CCD Phase Clock Generator. Converting the stored analog information into digital data and saving it into the Acquisition Memory is then started. Both the "conversion" and "save" aspects of the acquisition process are discussed in "Analog Data Conditioning and A/D Conversion" and "Acquisition Processing and Display."

Short-Pipeline Mode

For Short-Pipeline acquisitions, each CCD can contain only 37 samples before the "pipe" is full. This means that samples must be continuously shifted through the digitizing process and into Acquisition memory as the samples are being taken. Since the pretrigger and post-trigger distribution of the data in the acquisition record is not defined until a trigger occurs, converted data is continually stored in the Acquisition Memory. If the Acquisition Memory space should become filled before a trigger occurs, newly acquired data will simply displace the old in a circular manner (oldest data replaced first). After a trigger, the Time Base Controller counts another sampling clock to determine when enough samples have been moved into the Acquisition Memory to satisfy the post-trigger requirements and then turns the Acquisition Memory space over to the Waveform μP. The Waveform μP transfers the samples into the Save Memory for eventual display.

DATA CLOCKING TO ACQUISITION MEMORY

FISO Mode

In FISO mode, the Time Base Controller signals the CCD Phase Clock Array (U470, diagram 11) to begin clocking waveform samples out of the CCDs. The Time Base Controller monitors the Trigger Location signals from the CCD Phase Clock Array to determine precisely where in the acquisition the trigger occurred. When the samples

not needed to fill the 1024-point waveform record have been clocked out so that only the samples properly positioned around the trigger point remain in the CCD, the Time Base Controller enables the save acquisition clocking to begin moving the digitized samples from the A/D Converter into the Acquisition Memory, thus saving the waveform record. (See "Detailed Circuit Description" for more trigger point location information.)

To do a waveform save, the Time Base Controller is selected to control writing into the Acquisition Memory via the Memory Mode Control circuit (diagram 8). The $\overline{\text{SAVEACQ}}$ clock circuitry is then enabled to pass a 2 MHz clock signal ($D_2$4XPC) from the CCD Data Clock circuit (diagram 7) to do the memory writes at the FISO rate.

The memory write clock also increments the Acquisition Memory Address Counter to provide the address for writing the next data point into the Acquisition Memory. The address is latched into the Record-End Latch during each memory write so that the beginning of the acquisition record can be determined when the Acquisition Memory is accessed later.

As the samples are being moved into the Acquisition Memory, the Time Base Controller monitors clocks from the CCD Data Clock circuit to determine when the 1024 digitized samples (per each channel) are saved. The Time Base Controller then stops writing to the Acquisition Memory by disabling the write clock and switches control of the memory to the Waveform μP (again, via the Memory Mode Control circuit). The Time Base Controller then strobes the Waveform μP (diagram 2) to signal that the acquisition is complete and the waveform data is available for processing and display.

Short-Pipeline Mode

For Short-Pipeline mode, the Time Base Controller generates an enabling clock that controls the 2 MHz write clock to the Acquisition Memory. The correct enabling rate of the $\overline{\text{SAVEACQ}}$ write clock for the selected SEC/DIV setting is synthesized within the Time Base Controller, using a CCD Data Clock input to obtain the base frequency. This enabling clock turns on the controlling gate circuit to pass only two $\overline{\text{SAVEACQ}}$ clocks (via the Mode Control Circuit) to write to the Acquisition Memory, saving one digitized data point per channel (two in Envelope Mode—one max and one min per channel). Then the synthesized clock from the Time Base Controller disables the $\overline{\text{SAVEACQ}}$ clock for a certain number of clock cycles. Specifically, the number of ungated clock cycles equals the SEC/DIV setting divided by 50 μs, i.e., four clock cycles at a SEC/DIV setting of 200 μs. Therefore, the samples saved in the Acquisition Memory in Short-Pipeline mode produce a constant 50 samples per horizontal division when displayed, regardless of the SEC/DIV setting.

The remainder of the Short-Pipeline save operation is similar to a FISO save. The Acquisition Memory Address Counter is incremented by the clock that writes data to the memory as in FISO, but at the synthesized rate rather than at the 2 MHz FISO rate. As in FISO, the Trigger Location information is used to determine the trigger point location. Enough samples are saved into memory after the trigger point is found to fill the post-trigger requirements before turning control over to the Waveform μP.

ANALOG DATA CONDITIONING AND A/D CONVERSION

Both pairs of the differential output signals from the CH 1 and CH 2 CCDs are applied to the inputs of the corresponding pairs of Single-Ending Amplifiers (diagram 14). Each amplifier converts the differential signal clocked to its inputs to a single-ended output signal. That signal is used to drive the input of a corresponding Sample-and-Hold circuit (also shown on diagram 14).

The CCD Data Clocks and the CCD Output Sample Clocks (diagram 7) control the timing between when the signals are coupled to their corresponding Sample-and-Hold circuits and when the Sample-and-Hold circuit outputs are coupled to the single analog input of the A/D Converter (diagram 15). Briefly for FISO mode, the timing is as follows:

1. A CCD Output Sample clock gates the outputs of both CH 1 Single-Ended amplifiers to the input of their associated Sample-and-Hold circuit. There, the input levels are sampled, and the gating is then disabled to hold the sampled level on the Hold capacitors. One of the CH 1 Sample-and-Hold output circuits is then gated on to pass the sample level to the A/D Converter for digitization.

2. While the output level of the first CH 1 Sample-and-Hold is gated to the A/D Converter, a CCD Output Sample clock gates the outputs of the CH 2 Single-Ended Amplifiers to their corresponding CH 2 Sample-and-Hold circuits. Both the first CH 1 Sample-and-Hold outputs and the inputs to the CH 2 Sample-and-Hold circuit are then ungated, and the first CH 2 Sample-and-Hold output circuit is gated on to pass its held signal level to the A/D Converter.

3. The first CH 2 output is then ungated, and the second CH 1 Sample-and-Hold output and the second CH 2 Sample-and-Hold output are gated on in succession to couple their held levels to the A/D Converter. This multiplexing process continues until 512 samples from both sides of the two CCDs have been converted.

NOTE

The samples are clocked through each side of the CCD at a 500 kHz rate, resulting in an output sampling rate of 1 MHz per channel. Also note that the 4-to-1 gating of the two channels and their respective outputs results in a 2 MHz time-multiplexed (4-to-1) signal to the A/D Converter.

For Short-Pipeline sampling mode, the gating for the inputs to the Sample-and-Hold circuits is the same as in FISO mode. However, since only one side of each CCD is used per channel, only one pair of differential outputs (per CCD) and the corresponding Single-Ended Amplifier and Sample-and-Hold circuits transfers valid waveform samples to the A/D Converter. The Short-Pipeline mode save-acquisition clocking ensures that only the valid converted data is saved (see "Short-Pipeline Mode" in "Acquisition Process and Control"). Observe, however, that the signal to the A/D Converter is still a 2 MHz time-multiplexed signal, but with invalid data half of the time. Since the invalid data is, in effect, discarded by the Short-Pipeline Mode save-acquisition clocking, the A/D Converter continues to operate at a constant 2 MHz conversion rate as in FISO mode.

The time-multiplexed signal is applied to the input of the A/D Converter circuit for digitization. The System Clocks circuit (diagram 7) provides a 2 MHz clock to the converter, for a 2 MHz data-conversion rate of the input signal. The resulting digital output byte is applied in four 8-bit bytes to the Acquisition Latches (diagram 15).

For Normal and Average Acquisition Modes, data is clocked into the Acquisition Latches by the same 2 MHz clock used by the A/D Converter. Enabling of the outputs of the Acquisition Latches is controlled by the CCD Data clocks in a sequence that ensures that the data clocked out from the enabled latch corresponds to the CCD side and Sample-and-Hold circuit that provided it. The 8-bit sample bytes are then saved in Acquisition memory in the same order they were obtained. This "structured" method for saving acquisitions keeps the data in the correct time sequence for display.

For Envelope Mode, the Time Base Controller disables continuous gating of the 2 MHz clock to the Acquisition Latches. This action turns over the gating of that clock to the Envelope Min-Max Comparators (diagram 15). With the 2 MHz clock ungated, the CCD Data Clocks will continue to control the enabling of the outputs of the acquisition latches as described, but the new data bytes are not continually clocked into the latches. The result is that only the data bytes clocked in by the Envelope Min-Max Comparators are sequentially clocked to the Envelope Data bus in the following manner: CH 1 max, CH 2 max, CH 1 min, CH 2 min. This is the same order in which the analog samples are clocked into the A/D Converter.

The output of the A/D Converter is fed to the Envelope Min-Max Comparators (diagram 15). The outputs of the Acquisition Latches are also fed back to those comparators. Due to the previously described timing action of the CCD Data Clocks, the newly digitized minimum or maximum value from the Peak Detectors (see "Input Signal Conditioning and Analog Sampling") is compared to the last value latched into the Acquisition Latch that corresponds to the new point. If the newly acquired point is outside the previous min or max value, the appropriate Envelope Min-Max Comparator gates the 2 MHz clock, and the new data byte is latched into the corresponding acquisition latch.

ACQUISITION PROCESSING AND DISPLAY

Data Transfer to SAVE Memory

Once the 1024 digitized signal bytes per channel are in Acquisition Memory, the Time Base Controller ungates the $\overline{\text{SAVEACQ}}$ clock and switches the the Memory Mode Control circuit to the Waveform μP. It also signals the Waveform μP, via the Display Status Buffer (diagram 2), that the acquisition is complete. The Waveform μP can then access the Acquisition Memory.

When the Waveform μP reads the acquisition done (ACQDN) signal from the Time Base Controller, it writes an address (via the Address Latch) which is decoded by the Register Address Decoding circuit (diagram 2). The decoded address signals the Record-End Latch (diagram 8) to enable its contents (the last addressed memory location for the stored acquisition) to the Waveform μP data bus to be read to determine the location of the last record byte stored. The Waveform μP then uses that location to determine the location of any byte in Acquisition Memory.

The Waveform μP outputs (via its Address Latch) addresses to the Address Counter for Acquisition Memory. The Address Counter is held in its load mode by the Waveform μP (via the Memory Mode Control circuit), passing the address through to Acquisition Memory. The Waveform μP enables the Acquisition Memory and les the clocks (via the Memory Mode Control circuit) to move stored data out to the Waveform Data bus via the Data Bus buffer. This data is written either into the

Waveform Save Memory or into an internal register of the Waveform μP for processing, depending on the display requirements.

Most transfers from Acquisition Memory are straight out of Acquisition Memory, through the Waveform Data Buffer, and into a corresponding memory location in Waveform Save Memory. However, the Waveform μP sometimes disables the Waveform Data Buffer and reads the data directly into its own internal register via the Data Bus Buffer. The Waveform μP then processes it according to tasks assigned by the System μP, using routines stored in its own ROM. For instance, in Envelope mode the Waveform μP will read (into a second internal register) the corresponding byte stored in Waveform Save Memory from the previous acquisition. If the new byte, stored in the first internal register, is determined to be a new max or min value, the Waveform μP uses it to replace the previous value in Waveform Save Memory.

It should be noted that the Waveform Save Memory is a paged RAM memory. The Waveform μP uses a paged address scheme to load waveform data into one of six possible sections, depending on the source (CH 1 or CH 2) or the destination (REF1, REF2, etc) of the waveform. Observe also that the Waveform Save Memory RAMs are supplied power by the Standby Circuit when instrument power is off, allowing for preservation of the waveform data stored in each of the six sections. See the "Detailed Circuit Description" for more information concerning the structuring of the Waveform Save Memory and operation of the Standby Power circuit.

Data Transfer to Display Memory

Once an acquisition is stored in the Waveform Save Memory, it must be moved to the proper locations in Display Memory, from where it is converted back to an analog signal for display. The Waveform μP updates each section of Display Memory at the proper time, based on internal routines stored in Waveform Processor ROM and timing supplied by the Secondary Clocks via the Waveform Processor Clock and Bus Grant Decoding circuit. The Waveform μP also writes attribute changes (such as changes in horizontal position) to the Display Memory (when assigned the task by the System μP).

The Waveform μP addresses (in parallel) both the Waveform Save Memory and the Display RAMs via the Address Multiplexer (diagram 17). The System μP gates the address through to the Display Memory (the Vertical, Horizontal, and Attribute RAMs on diagram 16) via the Display Control Register (diagram 17). The Waveform μP then clocks the data out of its memory into the appropriate Display RAM.

Data Transfer to Display DACs

When the System μP initiates the display of the data stored in Display Memory, it writes (via its data bus) the starting address of that data to the Display Counter (diagram 17). It also outputs an address that latches, via the Register Select Circuit, the starting address into the Display Counter. Simultaneously, data from the System μP initiates, via the Display Control Register (diagram 17), a strobe to the Display State Machine. The Display State Machine then signals the Address Multiplexer, gating the address(es) output by the Display Counter through to Display Memory (diagram 16), and begins to gate a clock from the Display Clocks circuit to the Display Counter. The Display Counter increments for each (display) clock cycle, accessing successive addresses in Display Memory as the System μP clocks the data out of Display Memory.

The System μP uses data writes to the Mode-Control Register (diagram 17) to select which portion of the Display Memory (Vertical, Horizontal, or Attribute) or which register (Volts Cursors or Time Cursors) is selected for output to the Vertical or Horizontal DACs. The System μP also uses the Mode-Control Register to select, via the Horizontal Data Buffers, whether the waveform data in the Horizontal Ram is applied to the Horizontal or Vertical DAC, allowing either YT or XY displays.

It should be noted that the incrementing addresses supplied via the address latch are also applied to the Ramp Buffer. Since each incremental address corresponds directly to the data byte it addresses, and since the output of the Ramp Buffer (diagram 16) will be converted to a staircase waveform by the Horizontal DAC, the addresses can provide the horizontal deflection (or "ramp") necessary for YT displays.

Data Display

Data, waveform or other, is converted to two complementary output currents by each Display DAC. These currents are analog in nature, but reflect the $\pm$256-bit resolution of the DACs. Therefore, the current outputs are a series of discrete analog levels (or steps, if the current is varying), each level corresponding to the 8-bit byte applied to the DAC.

The differential current outputs from the Horizontal and Vertical DACs are converted to single-ended voltages at the input to the Display Output circuitry. Those voltages then drive either the corresponding Horizontal and Vertical Vector Generators (diagram 18) for vector displays or the Horizontal and Vertical Output Amplifiers directly for dot displays.

The Vector Generators consist of a High-Current Difference Amplifier, a Sample-and-Hold circuit, and a Integrator to produce the vectors that connect the sample points in the display. Signals for vectored displays are continuously sampled and held, and integrated. The input voltage integrated is the difference between the voltage level of the sample presently being held and the intergrated level of the sample immediately preceding it. This action allows a smooth transition between the individual steps for a continuous display.

A Display Mode Switcher selects between the Vector Generator signals, a dots-only signal or an envelope display signal. With Envelope mode selected, the signal is passed through an rc integrator that produces vectors between the min-max data points of the Envelope Mode display.

The System μP, based on Front Panel settings, selects the display mode for the Vertical and Horizontal Vector Generators. The selected input, either Vector, Dot, Envelope, or Readout inputs, from each Vector Generator is coupled through to its corresponding Vertical or Horizontal Output circuit (diagram 18). There they are amplified and converted from single-ended to double-ended, to drive the Vertical or Horizontal plates of the crt (diagram 19). Both Vertical and Horizontal Output circuits have voltage offset and gain adjustments and are compensated for "spot wobble" (variations in beam placement on the crt screen with variations in beam intensity) by the Intensity circuit (diagram 6) via the Spot-Wobble Correction circuit.