



MMC 4035

4-STAGE PARALLEL IN/PARALLEL OUT SHIFT REGISTER

GENERAL DESCRIPTION

The MMC 4035 (G and H types) and MMC 4035 (E and F types) are monolithic integrated circuit, available in 16-lead dual in-line plastic or ceramic package. The MMC 4035 integrated circuit is a four-stage clocked signal serial register with provision for synchronous PARALLEL inputs to each stage and SERIAL inputs to the first stage via JK logic. Register stages 2, 3, and 4 are coupled in a serial D flip-flop configuration when the register is in the serial mode (PARALLEL/SERIAL control low). Parallel entry into each register stage is permitted when the PARALLEL/SERIAL control is high. In the parallel or serial mode information is transferred on positive clock transition. When the TRUE/COMPLEMENT control is high, the true contents of the register are available at the output terminals. When the TRUE/COMPLEMENT control is low, the outputs are the complements of the data in the register. The TRUE/COMPLEMENT control functions asynchronously with respect to the CLOCK signal. JK input logic is provided on the first stage SERIAL input to minimize logic requirements particularly in counting and sequence-generation applications. With \overline{JK} inputs connected together, the first stage becomes a D flip-flop. An asynchronous common RESET is also provided.

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FEATURES

- 4-stage clocked shift operation
- Synchronous parallel entry on all 4 stages
- \overline{JK} inputs on first stage
- Asynchronous TRUE/COMPLEMENT control on all outputs
- Static flip-flop operation, master-slave configuration
- Buffered inputs and outputs
- High speed 12 MHz (typ.) at $V_{DD} = 10$ V.

ABSOLUTE MAXIMUM RATINGS

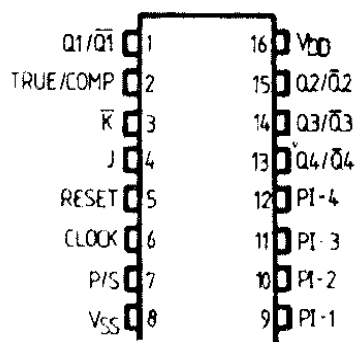
V_{DD}^*	Supply voltage: G and H types E and F types	-0.5 to -0.5 to	20 18	V V
V_i	Input voltage	-0.5 to	$V_{DD} + 0.5$	V
I_i	DC input current (any one input)		± 10	mA
P_{tot}	Total power dissipation (per package) Dissipation per output transistor for $T_A =$ full package-temperature range		200	mW
T_A	Operating temperature: G and H types E and F types	-55 to -40 to	125 85	$^{\circ}$ C $^{\circ}$ C
T_{stg}	Storage temperature	-65 to	150	$^{\circ}$ C

* All voltage values are referred to V_{SS} pin voltage

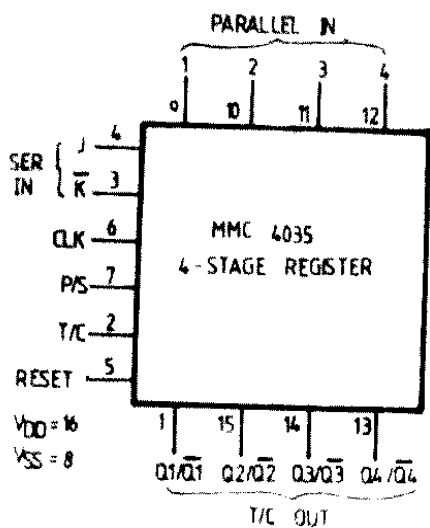
RECOMMENDED OPERATING CONDITIONS

V_{DD}^*	Supply voltage: G and H types E and F types	3 to 3 to	18 15	V V
V_i	Input voltage	0 to	V_{DD}	V
T_A	Operating temperature: G and H types E and F types	-55 to -40 to	125 85	$^{\circ}$ C $^{\circ}$ C

CONNECTION DIAGRAM



FUNCTIONAL DIAGRAM

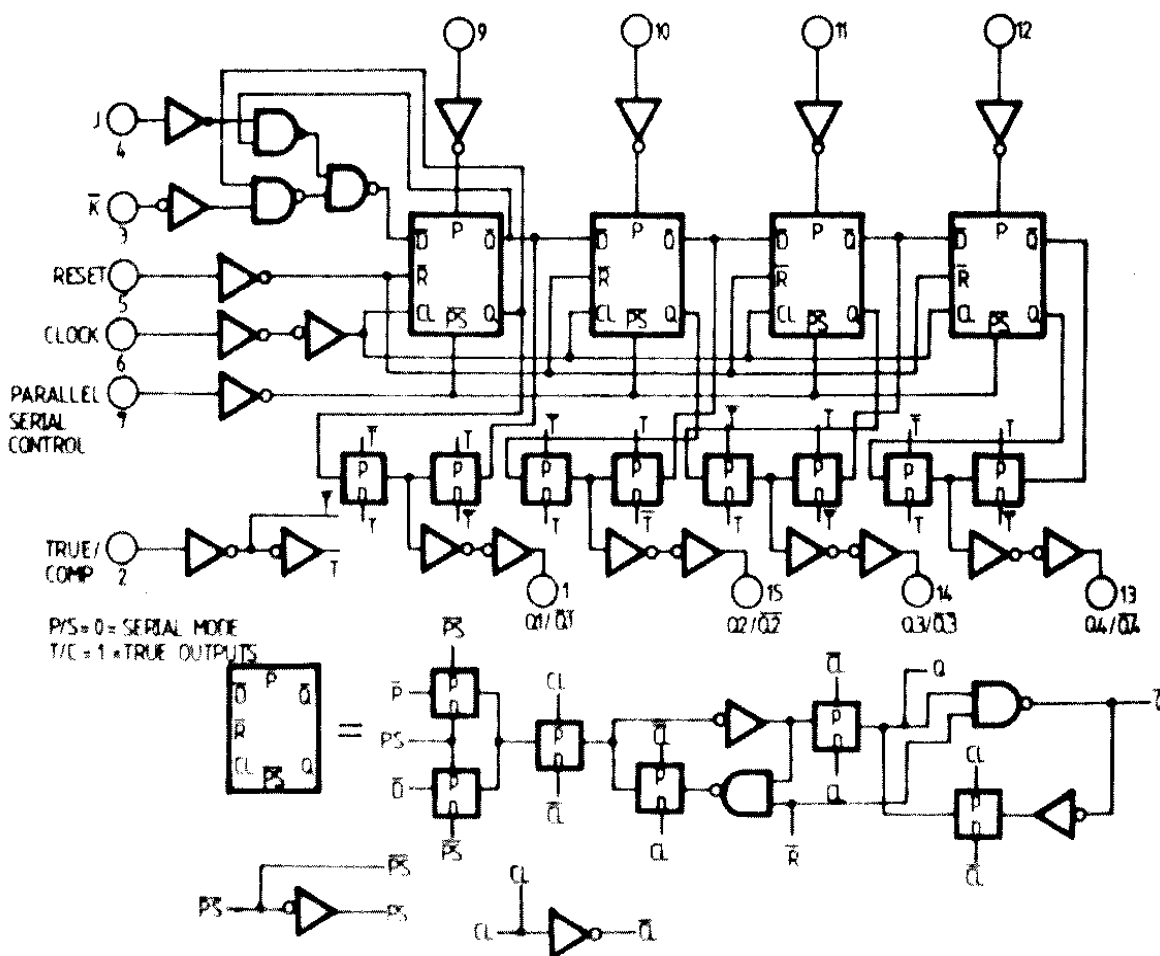


TRUTH TABLE

FIRST STAGE

CLOCK (ϕ)	I_{n-1} (INPUTS)			I_n (OUTPUTS)	
	J	K	R	Q_{n-1}	Q_n
	0	X	0	0	0
	1	X	0	0	1
	X	0	0	1	0
	1	0	0	Q_{n-1}	\bar{Q}_{n-1} TOGGLE MODE
	X	1	0	1	1
	X	X	0	Q_{n-1}	Q_{n-1}
X	X	X	1	X	0

LOGIC DIAGRAM



STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER		TEST CONDITIONS				VALUES						UNIT		
		V _I (V)	V _O (V)	I _O (μ A)	V _{DD} (V)	T _{LOW}		25°C			T _{HIGH}			
						min.	max.	min.	typ.	max.	min.		max.	
I _L	Quiescent current	G, H types	0/5			5		5		0.04	5		150	μ A
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/20			20		100		0.08	100		3000	
	E, F types	0/5			5		20		0.04	20		150		
		0/10			10		40		0.04	40		300		
		0/15			15		80		0.04	80		600		
V _{OH}	Output high voltage			< 1	5	4.95		4.95			4.95		V	
		0/10		< 1	10	9.95		9.95			9.95			
		0/15		< 1	15	14.95		14.95			14.95			
V _{OL}	Output low voltage			< 1	5		0.05			0.05		0.05	V	
		5/0		< 1	10		0.05			0.05		0.05		
		10/0		< 1	15		0.05			0.05		0.05		
V _{IH}	Input high voltage		0.5/4.5	< 1	5	3.5		3.5			3.5		V	
			1/9	< 1	10	7		7			7			
			1.5/13.5	< 1	15	11		11			11			
V _{IL}	Input low voltage		4.5/0.5	< 1	5		1.5			1.5		1.5	V	
			9/1	< 1	10		3			3		3		
			13.5/1.5	< 1	15		4			4		4		
I _{OH}	Output drive current	G, H types	0/5	2.5		5	-2		-1.6	-3.2		-1.15		mA
			0/5	4.6		5	-0.64		-0.51	-1		-0.36		
			0/10	9.5		10	-1.6		-1.3	-2.6		-0.9		
			0/15	13.5		15	-4.2		-3.4	-6.8		-2.4		
		E, F types	0/5	2.5		5	-1.53		-1.36	-3.2		-1.1		
			0/5	4.6		5	-0.52		-0.44	-1		-0.36		
		0/10	9.5		10	-1.3		-1.1	-2.6		-0.9			
		0/15	13.5		15	3.6		3.0	6.8		2.4			
I _{OL}	Output sink current	G, H types	0/5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		E, F types	0/5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I _{IH} / I _{IL}	Input leakage current	G, H types	0/18	Any input	18		± 0.1		$\pm 10^{-5}$	± 0.1		± 1	μ A	
		E, F types	0/15		15		± 0.3		$\pm 10^{-5}$	± 0.3		± 1		
C _I	Input capacitance		Any input						5	7.5			pF	

* T_{LOW} = -55°C for G, H devices; -40°C for E, F devices.* T_{HIGH} = +125°C for G, H devices; +85°C for E, F devices.

The Noise Margin for both "1" and "0" level is:

1 V min. with V_{DD} = 5 V2 V min. with V_{DD} = 10 V2.5 V min. with V_{DD} = 15 V

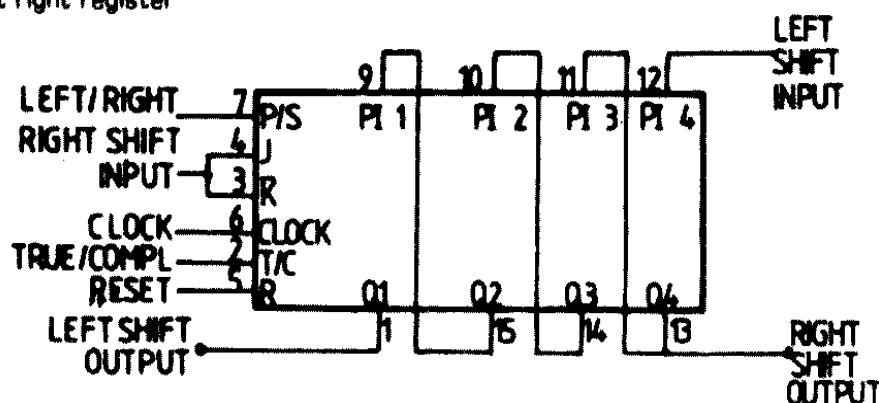
DYNAMIC ELECTRICAL CHARACTERISTICS

($T_A = 25^\circ\text{C}$, $C_L = 50\ \mu\text{F}$, $R_L = 200\ \text{kohm}$, typical temperature coefficient for all $V_{DD} = 0.3\%/^\circ\text{C}$ values, all input rise and fall time = 20 ns)

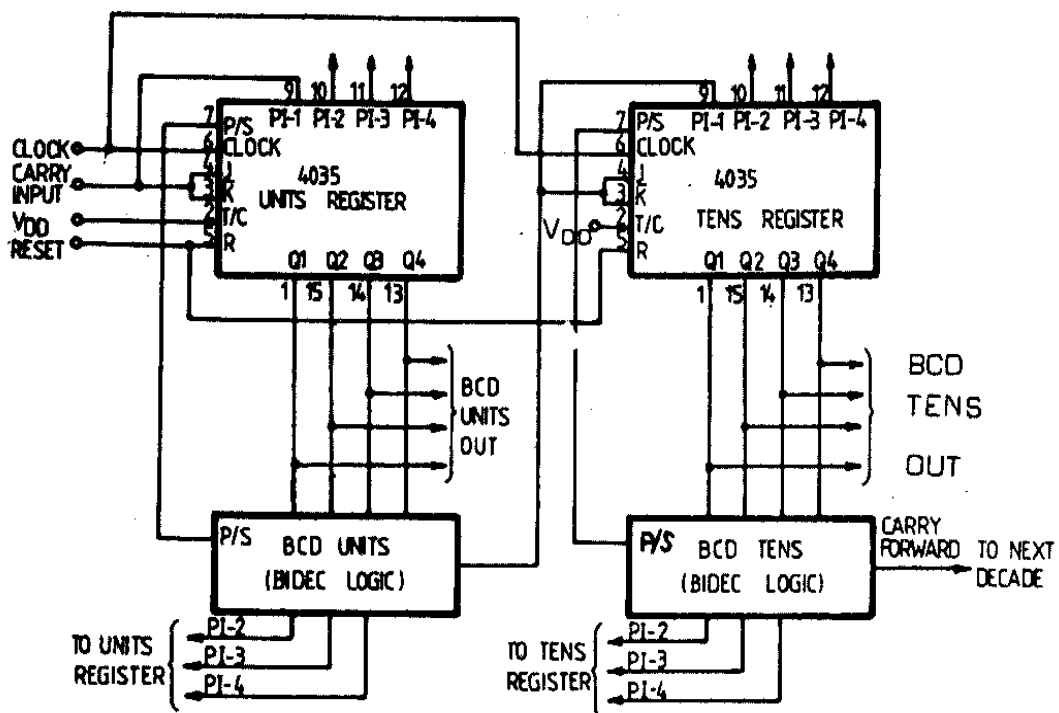
PARAMETER	TEST CONDITIONS V_{DD} (V)	VALUES			Unit
		min.	typ.	max.	
Clocked operation					
t_{PLH} Propagation delay time t_{PHL}	5		250	500	ns
	10		100	200	
	15		75	150	
t_{THL} Transition time t_{TLH}	5		100	200	ns
	10		50	100	
	15		40	80	
f_{CL} Maximum clock input frequency	5	2	4		MHz
	10	6	12		
	15	8	16		
t_W Clock pulse width	5		100	200	ns
	10		45	90	
	15		30	60	
t_r, t_f Clock input rise or fall time	5		15		μs
	10		15		
	15		15		
t_{setup} Data setup time J/R lines	5		110	220	ns
	10		40	80	
	15		30	60	
t_{setup} Data setup time Parallel-In-Lines	5		70	140	ns
	10		25	50	
	15		20	40	
Reset operation					
t_{PLH} Propagation delay time t_{PHL}	5		230	460	ns
	10		100	200	
	15		80	160	
t_W Reset pulse width	5		125	250	ns
	10		55	110	
	15		40	40	

TYPICAL APPLICATIONS

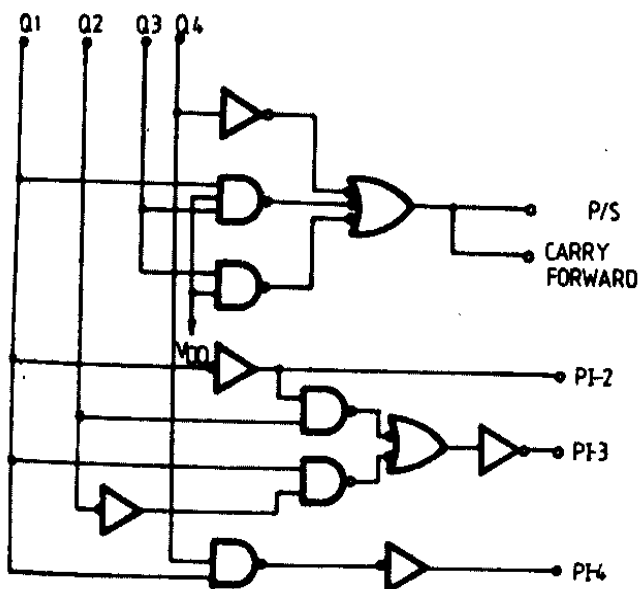
Shift left/shift right register



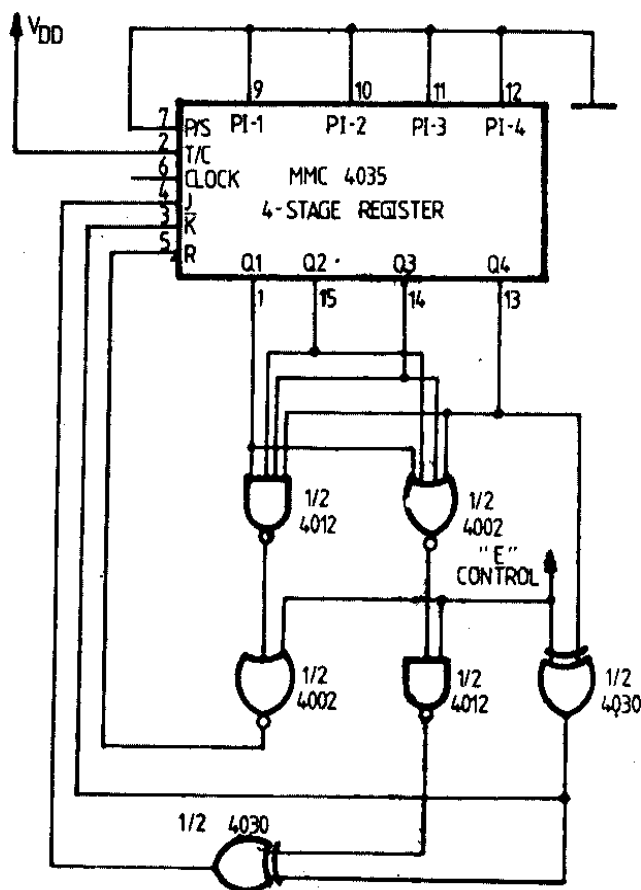
Binary — to — BCD converter



BIDEC logic



Double sequence generator



State sequences

Using a control line (E) two different state sequences can be generated. For example, suppose the following two sequences are desired on command (control line).

Control = E = 0

	Q ₁	Q ₂	Q ₃	Q ₄		Q ₁	Q ₂	Q ₃	Q ₄
	A	B	C	D		A	B	C	D
0	0	0	0	0	15	1	1	1	1
1	1	0	0	0	14	0	0	1	1
2	0	1	0	0	13	1	0	1	1
5	1	0	1	0	10	0	1	0	1
10	0	1	0	1	5	1	0	1	0
4	0	0	1	0	11	1	1	0	1
9	1	0	0	1	6	0	1	1	0
3	1	1	0	0	12	0	0	1	1
6	0	1	1	0	9	1	0	0	1
13	1	0	1	1	2	0	1	0	0
11	1	1	0	1	4	0	0	1	0
7	1	1	1	0	8	0	0	0	1
14	0	1	1	1	1	1	0	0	0
12	0	0	1	1	3	1	1	0 ⁹	0
8	0	0	0	1	7	1	1	1	0