TEKTRONIX®

148-M

148-M INSERTION TEST SIGNAL GENERATOR

INSTRUCTION MANUAL

Tektronix, Inc.
P.O. Box 500
Beaverton, Oregon 97077

Serial Number _____

070-1807-00

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WARRANTY

Tektronix warrants that this product is free from defects in materials and workmanship. The warranty period is one (1) year from the date of shipment. Tektronix will, at its option, repair or replace the product if Tektronix determines it is defective within the warranty period and if it is returned, freight prepaid, to a service center designated by Tektronix.

Tektronix is not obligated to furnish service under this warranty

a. to repair damage resulting from attempts by personnel other than Tektronix representatives to install, repair, or service the product;
b. to repair damage resulting from improper use or from connecting the product to incompatible equipment;
c. if personnel other than Tektronix representatives modify the hardware or software.

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SECTION 1

General Information

The 148-M is a PAL (Phase Alternate Line) television test signal generator capable of supplying several test signals commonly used for test and measurement of video transmission systems or discrete parts of the system. The generated signals are available as full-field composite video test signals on one output, and as Vertical Interval Test Signals (VITS) inserted into the vertical blanking interval on an incoming composite video signal, appearing in combined form on another output.

All time locations of test signals, as to position within both the line and field, are derived by digital counting from a master oscillator, which is locked to the incoming synchronizing pulses. The 148-M may be used in conjuction with the TEKTRONIX 145-M to provide standard test signals with Gen-Locked operation.

Several different test signals may be inserted on successive lines during the vertical blanking interval, providing a simultaneous check of the complete television transmission system.

A Preview mode of operation permits observing the signal with insertion signals added before adding to the program signal.

[1]**Synchronization of signals in both frequency and phase.**

In the event of power failure, or the actuation of a remote bypass switch, a relay switch routes the program signal around the instrument, bypassing all circuitry and thus providing fail-safe protection.

Safety Considerations

The instrument is intended to be operated from a single-phase power source which has one of its current-carrying conductors (neutral) at or near ground (earth) potential. Operation from other power sources where both current-carrying conductors are live with respect to ground (such as phase-to-phase on a multi-phase system) is not recommended, as only the Line Conductor has over-current (fuse) protection within the instrument.

ELECTRICAL CHARACTERISTICS

Performance Conditions

Characteristics and their Performance Requirements described in this section are valid over the stated environmental range, for instruments calibrated at an ambient temperature between +20° C and +30° C. Instrument warmup of 5 minutes is required.

TABLE 1-1

Insertion Control System

Characteristics	Performance Requirements	Supplemental Information
Signal Input Level		
Unity Level	±0.5% of Unity Gain	
VAR	1 V peak-to-peak variable within 3 dB	
PROGRAM Input Impedance	75 Ω nominal	
PROGRAM Input Return Loss		
POWER ON	At least 46 dB to 5 MHz	
POWER OFF or BYPASS	At least 40 dB to 5 MHz	
Output Impedance (All)	75 Ω nominal	
Output Return Loss (All)	At least 36 dB to 5 MHz	

TABLE 1-1 (cont)

Characteristics	Performance Requirements	Supplemental Information
Output Blanking DC Level (All)	0 volts within 50 mV	
Isolation (All)	At least 46 dB to 1 MHz At least 34 dB to 3.58 MHz	
Inserted Signal Amplitude	Within 1% of nominal input amplitude	
Amplitude Ratio		
2T Pulse to Bar	100% ±0.5%	
Mod Sin^2 Pulse	100% ±0.5%	Chrominance to Luminance
Waveform Tilt		
Line Tilt	0.25% or less	
Field Rate Square-Wave	0.5% or less	
Differential Phase (10-90 APL, Standard Input)		
PROGRAM OUTPUT	0.15° or less	0.3° or less at +3 dB
PREVIEW OUTPUT	0.3° or less	
Differential Gain (10-90 APL, Standard Input)		
PROGRAM OUTPUT	0.2% or less	0.4% or less at +3 dB
PREVIEW OUTPUT	0.4% or less	
Luminance Amplitude Non-Linearity	0.25% or less	Unmodulated Staircase
Random Noise Output on PROGRAM OUTPUT	At least 75 dB (RMS) down	Using Weighted and Low Pass Filters (4.2 MHz)
Residual Subcarrier on Non-Inserted Lines	At least 60 dB down	3.58 MHz Bandpass Filter
Hum or Transients on Non-Inserted Lines	At least 60 dB down	Using Weighted and Low Pass Filters (4.2 MHz)
Spurious Signals During:		
Blanking	At least 40 dB down	Low Pass (4.2 MHz)
Active Picture, VITS	At least 60 dB down	Low Pass (4.2 MHz)

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TABLE 1-1 (cont)

Characteristics	Performance Requirements	Supplemental Information
Signal Attenuation In "Delete" Mode		
2T Pulse	At least 70 dB down	Low Pass (4.2 MHz)
Subcarrier (Staircase)	At least 60 dB down	Low Pass (4.2 MHz)
Crosstalk Into Program Channel from Internal Signal		
2T Pulse	At least 70 dB down	Low Pass (4.2 MHz)
Subcarrier (Staircase)	At least 60 dB down	Low Pass (4.2 MHz)
INSERT DELAY Range	At least ±0.5 μs (1 μs total)	
Time Jitter		5 ns or less
Frequency Response	±1% to 5 MHz	
Unwanted Pedestal at Time of VITS Insertion	5 mV or less	

TABLE 1-2

Test Signals

Characteristics	Performance Requirements	Supplemental Information
CCIR-I		
Bar		
Amplitude	700 mV ±1%	
Risetime	230 ns ±15% (2T); 115 ns ±15% (T)	Determined by 2T and T Sin^2 Filters
Pulse		
Pulse to Bar Ratio	100% ±0.5%	
HAD	250 ns ±15% (2T); 125 ns ±15% (T)	Determined by 2T and T Sin^2 Filters
Ringing Amplitude	0.5% or less	
Ringing Duration		2 cycles or less (Determined)
Modulated Sin^2 Pulse	12.5 T	Other pulses available by plug-in filter
Amplitude of Luminance Component	350 mV ±2%	

TABLE 1-2 (cont)

Characteristics	Performance Requirements	Supplemental Information
Amplitude Difference of Peak Chrominance to Peak Luminance	3.5 mV or less	
Chrominance to Luminance Delay	10 ns or less	Measured from baseline
HAD	1.57 μs ±50 ns	
Modulated 5-Step Staircase		
Luminance		
Step Amplitude	140 mV ±1%	700 mV ±1% total
Risetime	230 ns ±15%	Determined by 2T Sin^2 Filter
Chrominance		
Amplitude	280 mV ±1% (peak-to-peak)	
Risetime	400 ns ±25 ns	
Phase of Chrominance Components	180°, ±5°, from the +U axis	
Timing	See Fig. 1-2	
CCIR-II		
Pedestal Amplitude		
700 mV	700 mV ±1%	
Multiburst Amplitude		
700 mV	700 mV ±1%	
350 mV	350 mV ±1%	Top at 525 mV, Bottom at 175 mV
Average Level	350 mV ±5 mV	
Burst Frequencies	0.5 MHz ±3% 1.0 MHz ±3% 2.0 MHz ±3% 3.0 MHz ±3% 3.575 MHz ±3% 4.2 MHz +0% and −2%	
Burst Harmonic Content	−40 dB or less	

TABLE 1-2 (cont)

Characteristics	Performance Requirements	Supplemental Information
Burst Timing	Each burst starts at 0° and consists of a whole number of cycles.	
Modulated Pedestal		
First Chroma Level	140 mV peak-to-peak ±1%	
Second Chroma Level	280 mV peak-to-peak ±1%	
Third Chroma Level	560 mV peak-to-peak ±1%	
Average Level	350 mV ±1%	
Phase	180°, ±5°, from the +U axis	
Envelope Rise & Fall Times	400 ns ±25 ns	
Timing	See Fig. 1-2	
SIG-III		
Bar		
Amplitude	700 mV ±1%	
Risetime	230 ns ±15% (2T); 115 ns ±15% (T)	Determined by 2T and T Sin^2 Filters
Pulse		
Pulse to Bar Ratio	100% ±0.5%	
HAD	250 ns ±15% (2T); 125 ns ±15% (T)	Determined by 2T and T Sin^2 Filters
Ringing Amplitude	0.5% or less	
Ringing Duration		2 cycles or less (determined)
Modulated Sin^2 Pulse	12.5 T	Other pulses available by plug-in filter
Amplitude of Luminance Component	350 mV ±2%	
Amplitude Difference of Peak Chrominance to Peak Luminance	3.5 mV or less	
Chrominance to Luminance Delay	10 ns or less	Measured from baseline
Duration of 12.5 T Pulse	1.57 μs ±50 ns	

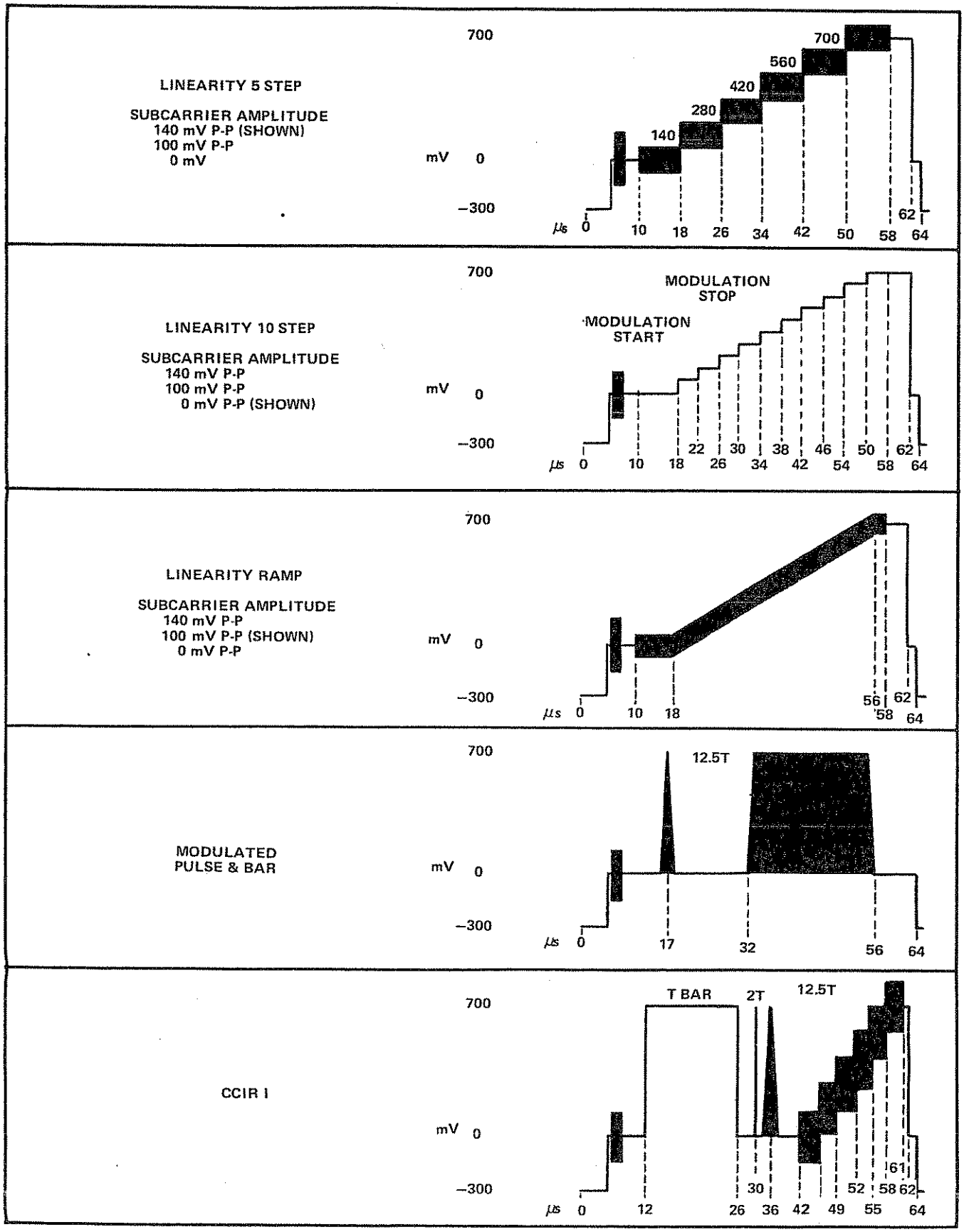
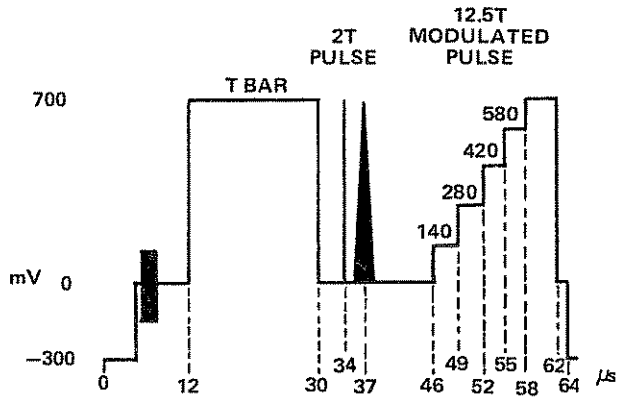
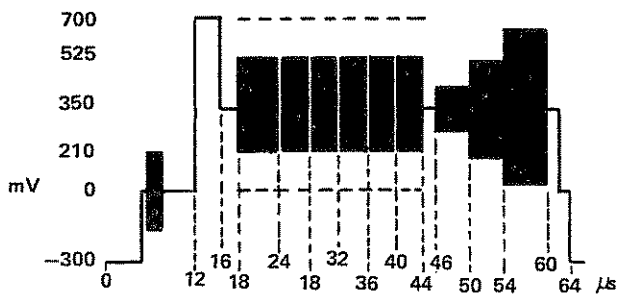


Fig. 1-2. Test signal output timing details.

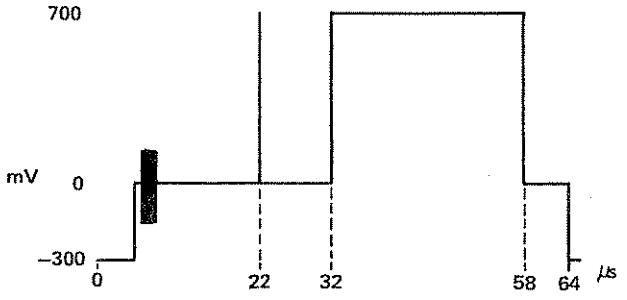


SIG. III



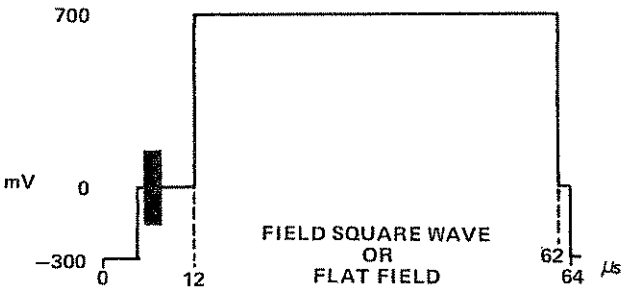
MULTIBURST: 700 mV
350 mV

CCIR II



PULSE & BAR

NOTE:
BAR PORTION OF PULSE
& BAR SIGNAL BETWEEN
LINES 63 AND 215 ONLY.



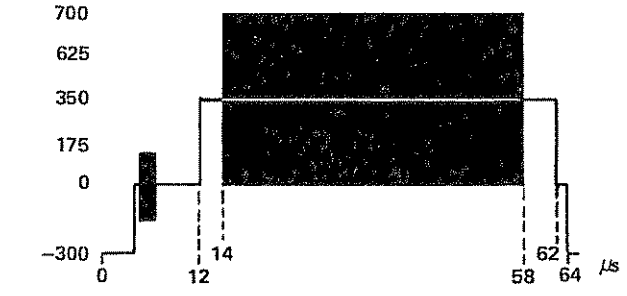
Notes:

1: BLACK (0 mV) BEFORE LINE 74 and AFTER LINE 206 FOR FIELD SQUARE WAVE.

2: VARIABLE AMPLITUDES: 0, 70, 140, 210, 350, 420, 490, 560, 630, or 700 mV.

3: PRESET BLACK: 0 TO 105 mV.

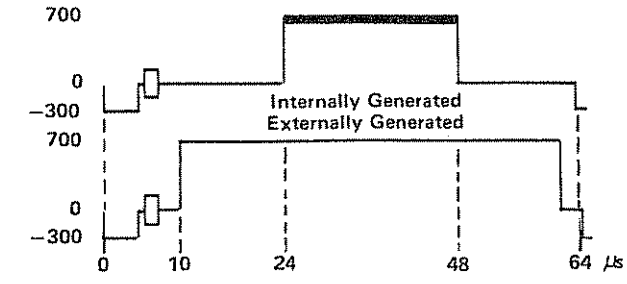
4: PRESET WHITE: 595 TO 700 mV.



FIELD RATE SWEEP GENERATOR

MODULATION AMPLITUDES:
700 mV P-P or 350 mV P-P

NOISE AT PREVIEW OUT IN INSERTION MODE



NOISE AT PREVIEW & FULL FIELD OUTPUTS
IN DELETION MODE

NOTE: NOISE TEST SIGNAL AVAILABLE ON VITS LINES ONLY.

Fig. 1-2 (cont). Test signal output timing details.

TABLE 1-2 (cont)

Characteristics	Performance Requirements	Supplemental Information
Residual Subcarrier on Insertion Line	3.5 mV or less	
Harmonic Content of Subcarrier	−40 dB or greater	
Phase Insertion and Full-Field	180°, ±5°, from the +U axis	
5-Step Luminance Staircase		Programmable for Ramp
Step Amplitude	140 mV ±1%	700 mV ±1% Total
Risetime	230 ns ±15%	Determined by 2T Sin^2 Filter
Timing	See Fig. 1-2	
MOD PULSE & BAR		
Modulated Sin^2 Pulse	12.5 T	Other pulses available by plug-in filter
Amplitude of Luminance Component	350 mV ±2%	
Amplitude Difference of Peak Chrominance to Peak Luminance	3.5 mV or less	
Chrominance to Luminance Delay	10 ns or less	
HAD of 12.5 T Pulse	1.57 μs ±50 ns	
Modulated Bar		
Amplitude of Chrominance	700 mV peak-to-peak ±1%	
Amplitude of Luminance	350 mV ±2%	
Risetime	1.41 μs, ±.05 μs	12.5 T
Residual Subcarrier On Insertion Line	3.5 mV or less	
Harmonic Content of Subcarrier	−40 dB or greater	
Phase Insertion and Full-Field	180°, ±5°, from the +U axis	
Timing	See Fig. 1-2	

TABLE 1-2 (cont)

Characteristics	Performance Requirements	Supplemental Information
LINEARITY		
Luminance		
Staircase Signal		
Step Amplitude		
5 Step	140 mV ±1%	700 mV ±1% Total
10 Step	70 mV ±1%	700 mV ±1% Total
Risetime (All Identical)	230 ns ±15%	Determined by 2T Sin^2 Filter
Ramp Amplitude	700 mV ±1%	
Chrominance		
OFF	No Chrominance	
100 mV	100 mV ±1% peak-to-peak	
140 mV	140 mV ±1% peak-to-peak	
Inherent Differential Gain	0.5% or less	
Inherent Differential Phase	0.2° or less	
Phase	180°, ±5°, from the +U axis	
Timing	See Fig. 1-2	Waveform transitions determined by characteristic instants
FIELD RATE SWEEP GEN		
Swept Frequency Limits	Less than 200 kHz to more than 6 MHz in one field	
Markers	Modulation blanked for 2 line periods 7 times per field (or 3 times per field by plug-jumper)	Swept Frequency is adjusted for approximately 1 MHz per marker
Modulation Amplitude	700 mV (or 350 mV by MULTI-BURST AMPLITUDE switch) ±1% to 5 MHz	
Pedestal Amplitude	350 mV ±5 mV	
Timing	See Fig. 1-2	
FLAT FIELD		
PRESET		
WHITE	85% to 100% of Peak White	Adjustable
BLACK	0% to 15% of Peak White	Adjustable
BOUNCE	Automatic Bounce between WHITE and BLACK	

TABLE 1-2 (cont)

Characteristics	Performance Requirements	Supplemental Information
RATE	Less than 1 sec to more than 10 sec	Adjustable
VAR APL	11 levels, each within 0.5% of nominal levels	
FIELD SQUARE-WAVE		
Amplitude	700 mV ±1%	
Lines at WHITE	Lines 74 through 206; Lines 337 through 469	50% Duty Cycle
Lines at Blanking	All other lines	
Risetime	230 ns ±15%	Determined by 2T Sin^2 Filter
Timing	See Fig. 1-2	
PULSE & BAR		
Pulse		
Pulse to Bar Ratio	100% ±0.5%	
HAD	250 ns ±15% (2T); 125 ns ±15% (T)	Determined by 2T and T Sin^2 Filters
Ringing Amplitude	0.5% or less	
Ringing Duration		2 cycles or less (determined)
Bar		
Amplitude	700 mV ±1%	
Risetime	230 ns ±15%	Determined by 2T Sin^2 Filter
Duration	26 μs/line X 152 lines	Lines 63 through 215; lines 326 through 478
Timing	See Fig. 1-2	
NOISE		Available on VITS lines only
Noise Measurement Signals		
Pedestal Amplitude		
50 mV	50 mV ±5 mV	
350 mV	350 mV ±7 mV	
700 mV	700 mV ±14 mV	
Variable Pedestal Range	At least ±50 mV from nominal, (100 mV Total)	Insertion Mode Only

TABLE 1-2 (cont)

Characteristics	Performance Requirements	Supplemental Information
Noise Amplitude	−20 dB to −59 dB (0 dB = 700 mV)	1 dB increments
Noise Attenuator Accuracy	Within 1 dB	
Noise Spectrum Bandwidth	15 kHz to 5 MHz, flat within 6 dB	
Timing	See Fig. 1-2	

TABLE 1-3

Full- Field Output

Characteristics	Performance Requirements	Supplemental Information
Full-Field Test Signal Outputs		
Relative Amplitudes	Within 1% at both outputs	
Return Loss	At least 36 dB to 5 MHz	
Sync and Burst Timing	See Figs. 1-3 and 1-4	
Sync Amplitude	300 mV ±1%	
Burst Amplitude	300 mV peak-to-peak ±3%	
Amplitude on Successive Lines	Smaller is 97% to 100% of the larger	
Phasing	+135° ±1° from +U axis on odd lines of the first and second fields and on even lines of the third and fourth fields −135° ±1° from +U axis on even lines of the first and second fields and on odd lines of the third and fourth fields Phase difference between burst on successive lines is 90° ±1°	
Chrominance Frequency		
Free Run	3.57561149 MHz ±25 Hz	
Locked Mode	Locked to incoming burst or external Subcarrier	Nominally 3.57561149 MHz ±5 Hz

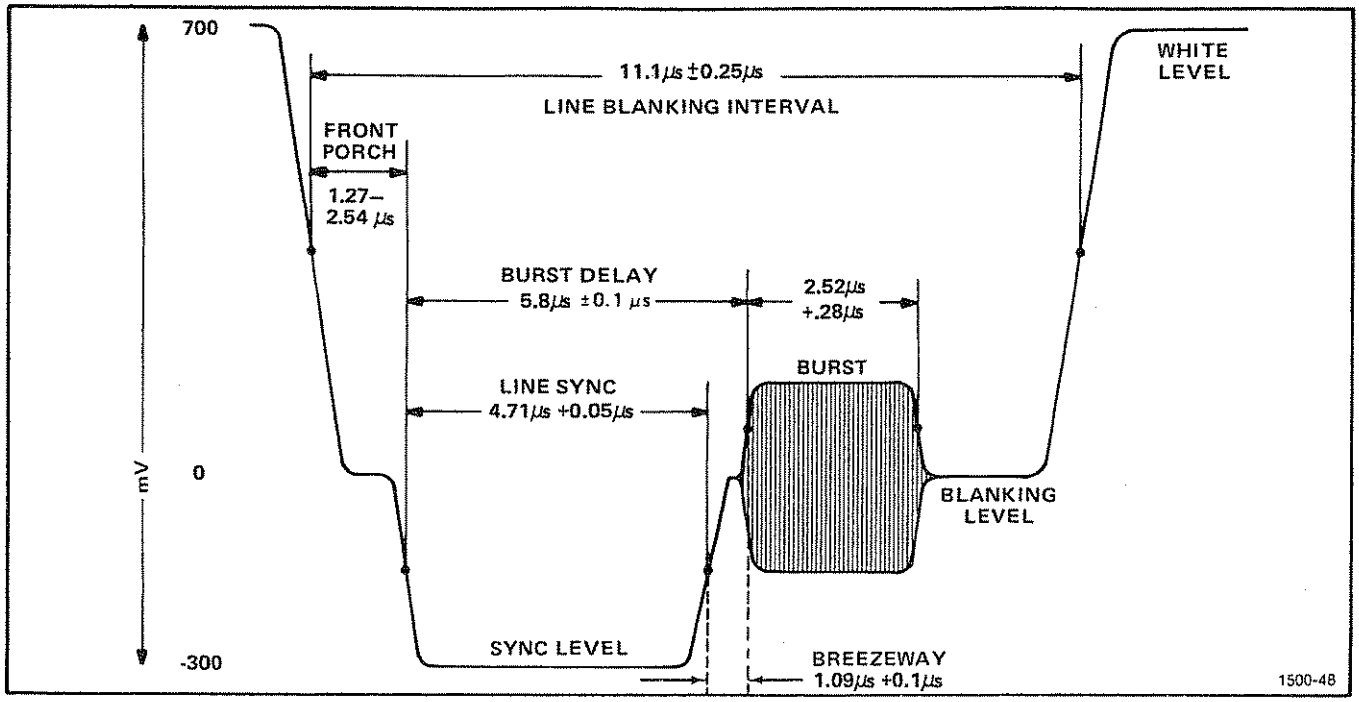


Fig. 1-3. Details of line synchronizing signals.

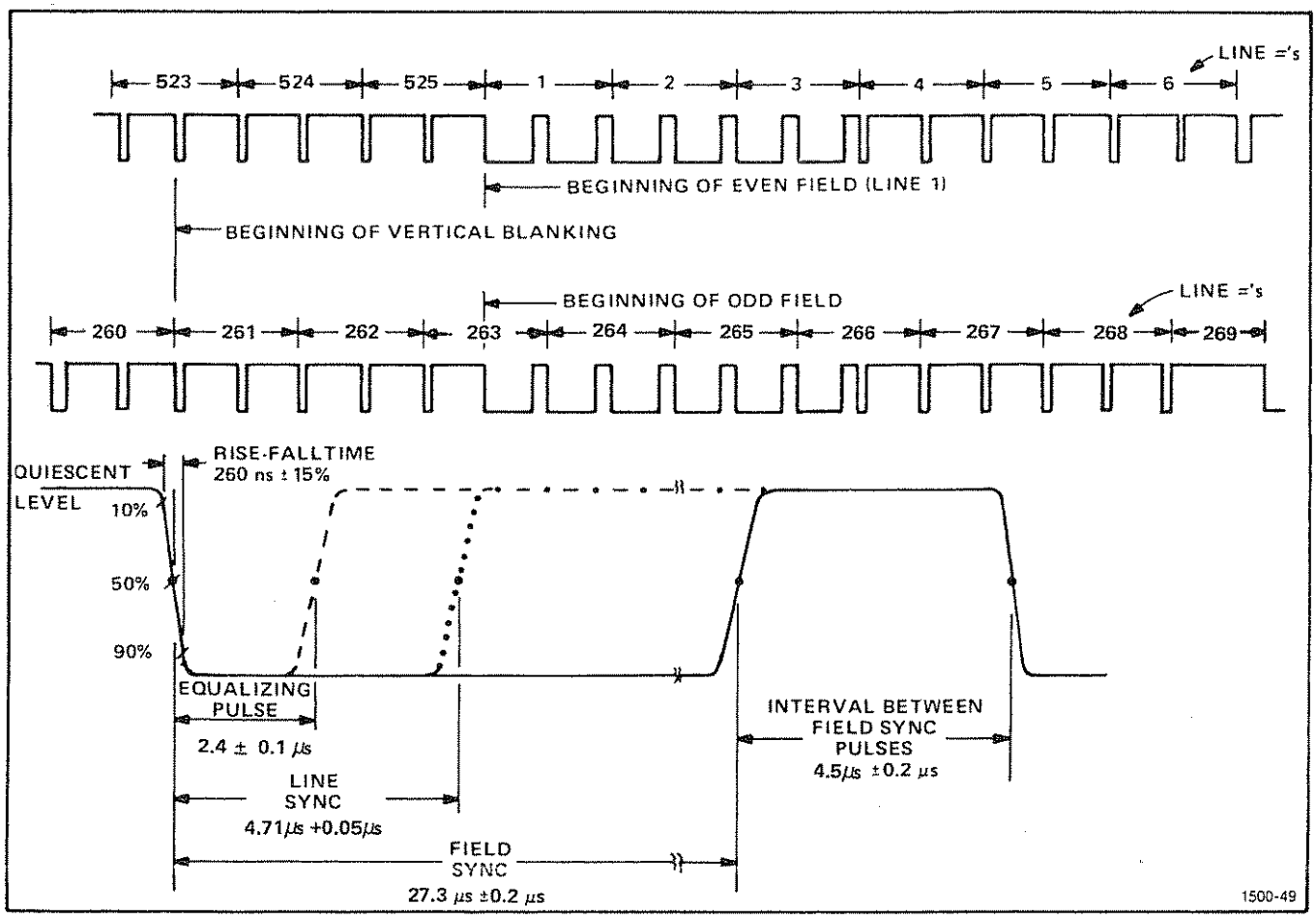


Fig. 1-4. Details of field (vertical) synchronizing signals.

TABLE 1-4

Other Signal Outputs and Inputs

Characteristics	Performance Requirements	Supplemental Information
Outputs		
COMPOSITE SYNC		Disabled with loss of incoming sync in INT or external sync in EXT
Amplitude	4 V, ±10%, negative-going into 75 Ω	
Return Loss	At least −30 dB to 3.6 MHz	
Rise and Fall Times	115 ns ±10%	
CW SUBCARRIER		Disabled with loss of incoming sync or burst in INT, or with loss of any input in EXT
Amplitude	2 V peak-to-peak, ±20%, into 75 Ω	
Return Loss	At least −30 dB to 5 MHz	
Frequency		Locked to incoming burst or EXT SUBCARRIER
NOISE		
Noise Amplitude	−20 dB to −59 dB (0 dB = 700 mV)	Low Pass (4.2 MHz)
Noise Attenuator Accuracy	Within 1 dB	
Noise Spectrum Bandwidth	15 kHz to 5 MHz, flat within 6 dB	
Return Loss	At least −30 dB to 5 MHz	
Inputs		
COMPOSITE SYNC		
Amplitude	2 V peak-to-peak nominal	
Return Loss	At least −30 dB to 5 MHz	Using external 75 Ω termination
BURST FLAG		
Amplitude	2 V peak-to-peak nominal	
Return Loss	At least −30 dB to 5 MHz	Using external 75 Ω termination
PAL PULSE		
Amplitude	2 V peak-to-peak nominal	
Return Loss	At least −30 dB to 5 MHz	Using external 75 Ω termination
SUBCARRIER		
Amplitude	2 V peak-to-peak nominal	
Return Loss	At least −30 dB to 5 MHz	Using external 75 Ω termination

TABLE 1-4 (cont)

Characteristics	Performance Requirements	Supplemental Information
EXT VITS IN		
Level	1 V peak-to-peak nominal	
Return Loss	At least −30 dB to 5 MHz	

TABLE 1-5

Gen Lock

Characteristics	Performance Requirements	Supplemental Information
Input Requirements		Input through PROGRAM LINE INPUT or EXT INPUTS
Sync Source	Nominal 1 V peak-to-peak composite video	
Sync Amplitude	300 mV, within 6 dB	
Burst Amplitude	300 mV, within 12 dB	
Burst/Sync Ratio	Within 6 dB	
Subcarrier Performance		
Phase Error		
With Frequency Change	Within 1° with input burst variation of ±10 Hz from 3.57561149 MHz, nominal burst level	
With Burst Amplitude Change	Within 1° with amplitude change of 3 dB. Within 3° with change in Burst/Sync ratio of −6 dB to +10 dB	
Phase Stability		
Breezeway Effect (See Fig. 1-3 for Location of Breezeway)	0.2° or less for burst timing errors including burst width variance (8-10 cycles) and breezeway variance (±0.28 μs)	
Dynamic APL	0.1° or less with APL variation from 10% to 90%	
Noise Effect	Within 1° with RMS White noise at 24 dB below 700 mV peak-to-peak picture signal	
INSERT SUBCARRIER PHASE		
Range	±10° nominal, via front-panel adjustment	

TABLE 1-5 (cont)

Characteristics	Performance Requirements	Supplemental Information
Subcarrier Lock		
Lock-up Amplitude	At least 150 mV peak-to-peak of burst information to lock	
Drop-out Amplitude	50 mV or less of burst information will allow unlock	(CW Mode)
Loss of Subcarrier Lock		Internal Subcarrier free runs at 3.57561149 MHz ±25 Hz. Subcarrier is not phase locked to sync if external sync is present
Loss of Sync		Indicated by front-panel lamp. Instrument returns instantly to internal subcarrier
INSERT DELAY Range	±0.5 μs (1 μs Total)	

TABLE 1-6

Power Supply

Characteristics	Performance Requirements	Supplemental Information
Line Voltage Range		
115 VAC		
Low	90 V to 110 V	
Medium	104 V to 126 V	
High	112 V to 136 V	
230 VAC		
Low	180 V to 220 V	
Medium	208 V to 252 V	
High	224 V to 272 V	
Crest Factor	At least 1.35	
Line Frequency	48 to 66 Hz	
DC Supply Accuracy		
−15 V		Within 1%
+15 V		Within 1%
+5 V		Within 1%

TABLE 1-6 (cont)

Characteristics	Performance Requirements	Supplemental Information
Regulation		
−15 V		Within 1%
+15 V		Within 1%
+5 V		Within 1%
Ripple		
−15 V		10 mV or less
+15 V		10 mV or less
+5 V		10 mV or less
Maximum Power Consumption	55 V	

TABLE 1-7

Physical

Characteristics	Information			
Finish	Cabinet is blue-vinyl painted; front-panel is anodized aluminum			
Dimensions				
Overall	Rackmount Version		Benchmount Version	
Height	8.81 cm	(3.470 inches)	9.70 cm	(3.820 inches)
Width	48.26 cm	(19.000 inches)	46.29 cm	(18.225 inches)
Length	49.94 cm	(19.66 inches)	48.51 cm	(19.100 inches)
Cabinet				
Height	- - - - -	- - - - -	8.81 cm	(3.470 inches)
Width	42.88 cm	(16.880 inches)	43.43 cm	(17.100 inches)
Length	46.76 cm	(18.410 inches)	46.76 cm	(18.410 inches)
Width Over Sides	44.77 cm	(17.625 inches)	- - - - -	- - - - -
Length with BNC-T	47.24 cm	(18.600 inches)	48.03 cm	(18.910 inches)
Net Weight	9.07 kg	(20 lbs.)	8.26 kg	(19 lbs.)

ENVIRONMENTAL CHARACTERISTICS

The following environmental test limits given in Table 1-8 apply when tested in accordance with the recommended test procedure. This instrument will meet the electrical performance requirements given in this section following an environmental test. Complete details on environmental test procedures, including failure criteria, etc., may be obtained from Tektronix, Inc. Contact your local TEKTRONIX Field Office or representative.

TABLE 1-8
Environmental

Characteristic	Information
Temperature	
Non-Operating Range	−40° C to −65° C
Operating Range	0° C to +50° C
Altitude	
Non-Operating Range	To 50,000 feet
Operating Range	To 15,000 feet

ACCESSORIES

Standard accessories supplied with this instrument are listed in the Mechanical Parts List.

OPERATING INSTRUCTIONS

General

This section of the manual is intended to provide the operator with information necessary for proper operation of the 148-M. Included are (1) Initial Installation information dealing with the various line voltages that may be used to power the instrument, and information regarding Local or Remote operation; (2) Controls and Connectors, a brief discussion of each control and connector; (3) Basic Information, dealing with the different signals generated by the 148-M and how they might be used; (4) First Time Operation, a complete step-by-step procedure using each control and connector; (5) Operating Changes, dealing with all internal changes that can be made for different applications; and (6) Glossary of Terms.

We recommend that the user of this instrument refer to the following reference material as a supplementary source of information.

Weaver, L.E.: TELEVISION VIDEO TRANSMISSION MEASUREMENTS, Marconi Instruments Limited, St. Albans, Herefordshire, England (FEB, 1972)

Television Products Application Notes, Tektronix, Inc.

INSTALLATION

Operating Voltage

WARNING

The instrument is intended to be operated from a single-phase power source that has one of its current carrying conductors (The Neutral Conductor) at or near ground (earth) potential. Operation from other power sources where both current carrying conductors are live with respect to ground (such as phase-to-phase on multi-phase systems) is not recommended, as only the Line Conductor has overcurrent (fuse) protection within the instrument.

The 148-M may be operated from either 115-Vac or 230-Vac (nominal) line voltage source. Quick-change line-voltage plugs, located under the fuse cover on the rear panel, change the transformer primary connections so that the instrument will operate from one line voltage or the other (115 V or 230 V). In addition, the plugs permit one of three line voltage operating ranges to be selected. Table 2-1 lists the voltage ranges that enable the instrument dc power supplies to regulate properly.

TABLE 2-1

115/230 Voltage Selector Plug Position	Range Selector Plug Position	Nominal Line (Center) Voltage	Line Voltage Plug Range[1]	Fuse Values
115 V	LO (Low)	100 Vac	90 to 110 Vac	0.75 A Fast-Blow
	M (Medium)	115 Vac	104 to 126 Vac	
	HI (High)	124 Vac	112 to 136 Vac	
230 V	LO (Low)	200 Vac	180 to 220 Vac	0.5 A Fast-Blow
	M (Medium)	230 Vac	208 to 252 Vac	
	HI (High)	248 Vac	224 to 272 Vac	

[1]Applicable when the line contains less than 2% total distortion.

To convert to a different line voltage, proceed as follows:

1. Disconnect the 148-M from the power source.

2. Unscrew the two captive screws holding the fuse cover. Remove the cover and attached fuses.

3. Pull out the 115/230 Voltage Selector plug, see Fig. 2-1, then rotate the plug 180° and insert it into the opposite set of holes. The 115/230 Voltage Selector plug is located in the upper position for 115 V operation, and in the lower position for 230 V operation.

4. To change the line-voltage operating range (LO, M, or HI), pull out the Range Selector plug and insert it in the desired hole locations. Select a range with a center voltage (see column three in Table 2-1) closely corresponding to the line voltage that will be applied in regular instrument operation.

5. Re-install the cover with the two captive screws and fuses. Be sure the cover fits firmly against the rear panel. This ensures that the line fuses are seated properly in the fuse clips.

6. Before applying power to the instrument, check that the indicating tabs on the selector plugs protrude through the proper holes in the cover for the correct line voltage and the proper operating range.

CAUTION

The 148-M should not be operated with the 115/230 Voltage Selector and/or Range Selector plugs in the wrong position for the line voltage applied.

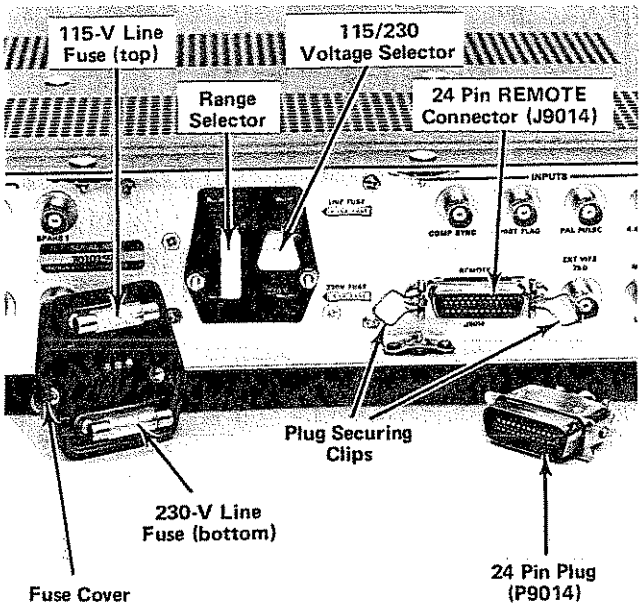


Fig. 2-1. Location of Range and Voltage Selector plugs with fuse cover removed (plugs as shown are set for 115-V medium range operation). Also shown is the REMOTE (J9014) connector, Plug (J9014), and plug securing clips.

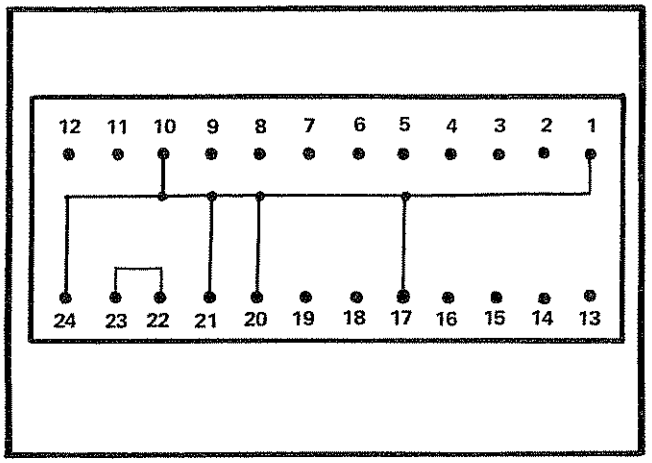


Fig. 2-2. Wiring diagram of Remote Plug for LOCAL operation (factory connected).

Local-Remote Connector

The 148-M may be operated by local or remote means. (Local means 148-M operation from the front panel.) A multi-pin connector, REMOTE J9014 is incorporated on the rear panel, see Fig. 2-1. Installed to this is a REMOTE plug, P9014, Tektronix Part No. 131-0325-00. This plug is factory wired for LOCAL operation, see Fig. 2-2.

To operate Remote, separate switching must be used at the remote location(s). In addition, the multi-pin plug must be wired accordingly. Fig. 2-3 shows the external switching required for remote control of FULL FIELD, PROGRAM, and PROGRAM LINE OUT FULL FIELD BYPASS. The external switching may be separate or combined to be controlled by one operator. Once the necessary wiring is complete, reconnect the plug to the REMOTE connector (J9014) and lock into place with the two securing clips.

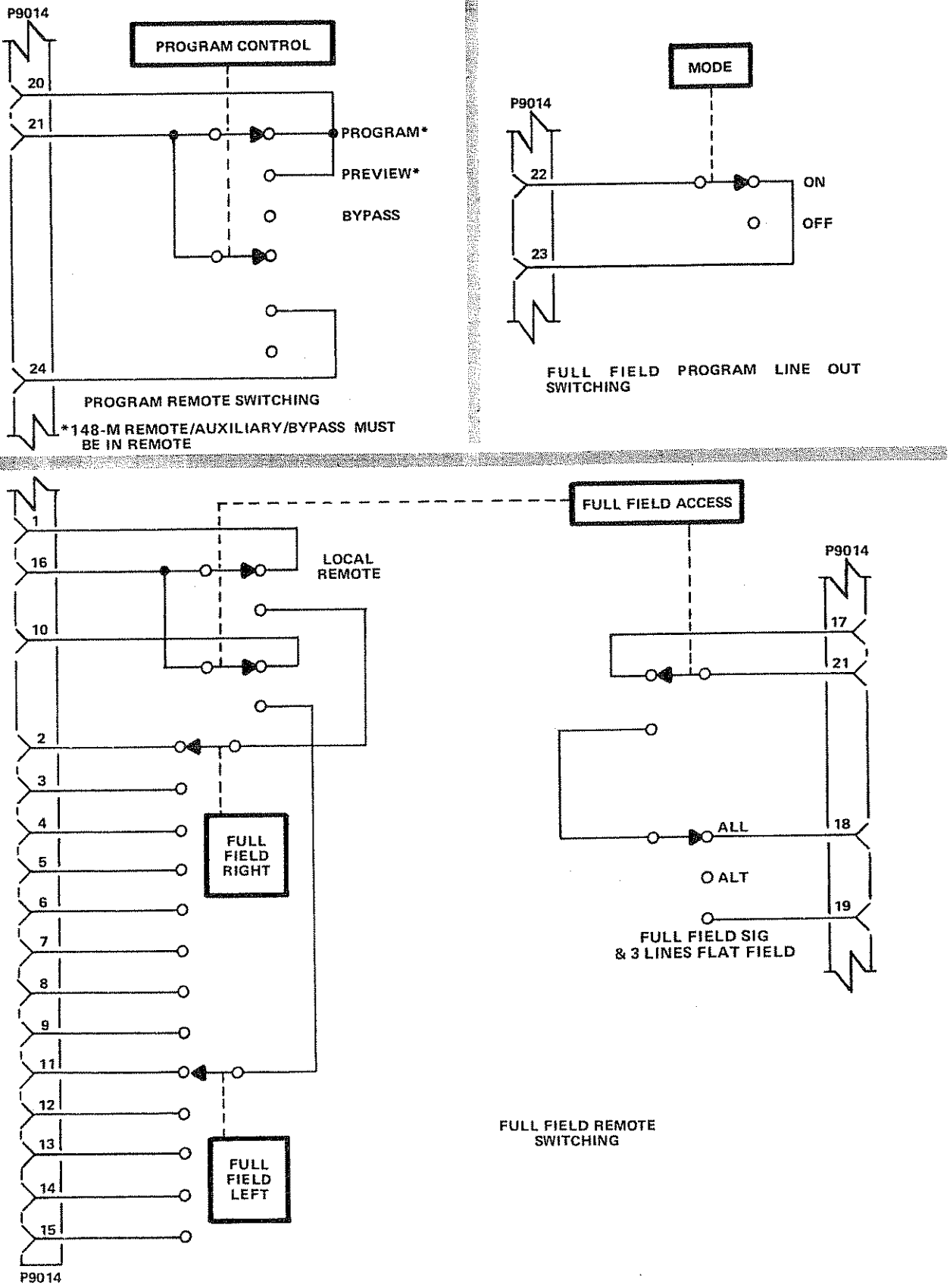


Fig. 2-3. Wiring diagrams for REMOTE operation of the 148-M.

CONTROLS AND CONNECTORS

Introduction

The following describes the functions and operation of the 148-M controls and connectors. Refer to Fig. 2-4 for locations of the controls and connectors.

Front-Panel Controls

POWER — Toggle switch—turns instrument ON and OFF. Green lamp indicates when POWER switch is ON and the instrument is connected to a line voltage source.

SYNC — Selects source of synchronization references.

INT position — Selects timing derived from the program signal.

EXT position — Selects timing derived from signals connected to COMP SYNC, SUB-CARRIER, PAL PULSE and BURST FLAG input connectors.

NOT LOCKED TO PROGRAM Light — Red light—indicates a loss of incoming synchronization information (e.g., loss of incoming program signal or external inputs). In this state, no VITS will be inserted. Full-field signals are generated, but line and field sync are not locked to subcarrier.

INSERTION SIGNAL CONTROL — Selects signal modes and controls their amplitude, phase, and timing relationships.

UNITY GAIN/VAR — UNITY GAIN Position selects a preset gain, normally adjusted for unity gain between program input and program output.

VAR position connects the front-panel LEVEL control to vary the gain of the program amplifier, allowing the incoming signal to match the inserted signal amplitude.

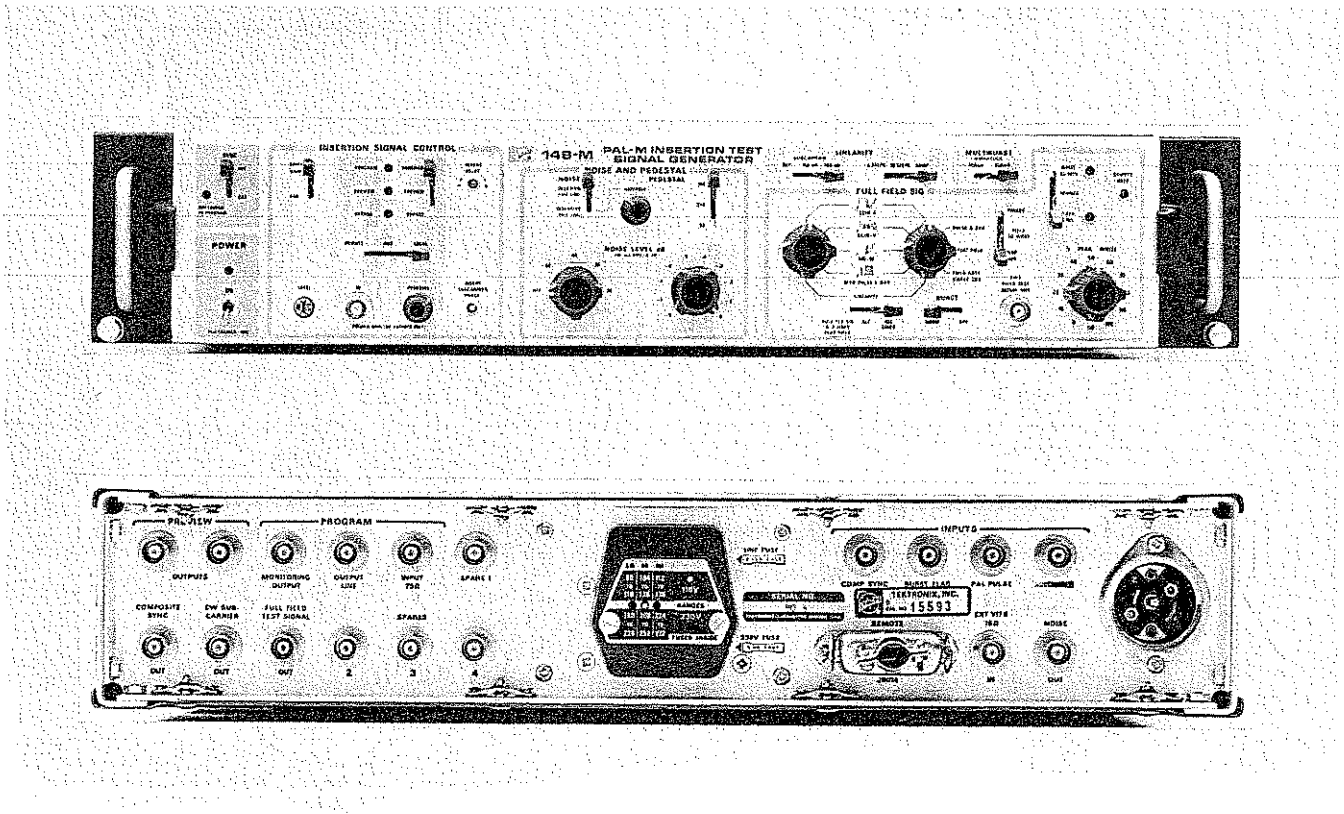


Fig. 2-4. 148-M front- and rear-panel controls and connectors.

LOCAL/AUX/REMOTE

LOCAL Position enables front-panel control of 148-M program or preview modes.

AUX permits a non-video signal (e.g., noise or sinewave) at the AUXILIARY INPUT to be used. This signal then appears at the PREVIEW outputs as composite video. The 148-M is then operating as a sync and blanking inserter. (PROGRAM IN is connected via relay to PROGRAM OUT in this mode.)

AUXILIARY PEDESTAL control provides a dc offset so the auxiliary signal excursion can be positioned between black and white limits of the resulting composite video signal.

In the REMOTE position, operation is controllable by remote switching circuits attached to the rear-panel REMOTE connector.

PROGRAM/PREVIEW BYPASS

PROGRAM position inserts VITS on the PROGRAM, PROGRAM MONITOR, and PREVIEW outputs according to internal programming of test signals.

PREVIEW inserts VITS on the PREVIEW outputs only, allowing verification prior to inserting VITS on PROGRAM OUT.

In BYPASS, incoming signals are switched by relay to the PROGRAM OUTPUT; bypassing the active circuits of the 148-M.

PROGRAM/PREVIEW BYPASS Lamps

When in remote control, the status may not be indicated by the position of the PROGRAM/PREVIEW/BYPASS switch. Green, yellow, and red lamps indicate the status of PROGRAM, PREVIEW, and BYPASS in that order. All lamps extinguished indicates an improper condition, and the 148-M will be in the bypass state.

INSERT SUB-CARRIER PHASE

Screwdriver adjustment controls the phase of the color subcarrier on internally generated signals with respect to the incoming color burst signal.

INSERT DELAY

Adjusts time-positioning of internally generated insertion signals with respect to the incoming signal.

NOISE AND PEDESTAL

Selects conditions of the NOISE signal.

NOISE

Controls information on the VITS lines programmed for NOISE.

DELETION (FULL LINE) deletes incoming VITS on NOISE LINES and inserts a selected PEDESTAL without noise.

INSERTION (HALF LINE) deletes center half of incoming VITS on NOISE lines and inserts half line of VARIABLE PEDESTAL with NOISE. (FULL FIELD OUT has a full line of NOISE and PEDESTAL on VITS lines.)

PEDESTAL (mV)

Switch selects one of three indicated levels (50, 350, or 700 mV) of pedestal on which noise measurements can be made.

VARIABLE

Potentiometer controls a change of at least ±50 mV in the pedestal amplitude, with the NOISE switch in the INSERTION mode. Permits accurate matching of the pedestal level with the level of the measured signal.

NOISE LEVEL dB

Controls the amplitude of the internally generated noise signal from −20 dB to −59 dB in 1 dB and 10 dB increments.

FULL FIELD SIG

Switches and adjustments select the type of signal available at the FULL FIELD TEST SIGNAL OUT jack, and modify certain characteristics of these signals.

Signal Selector (Right)

Selects one of the following eight signals for FULL FIELD TEST SIGNAL OUT: CCIR-I, CCIR-II, SIG-III, MOD PULSE & BAR, LINEARITY, FIELD RATE SWEEP GEN, FLAT FIELD, and PULSE & BAR.

Signal Selector (Left)

Selects one of the following five signals to be alternated with the signal selected by the (Right) Signal Selector: CCIR-I, CCIR-II, SIG-III, MOD PULSE & BAR, and LINEARITY. Switch is inoperative unless the ALL LINES/ALT/FULL FIELD SIG & 3 LINES FLAT FIELD switch is in the alternating (ALT) position.

ALL LINES/ALT/FULL FIELD SIG & 3 LINES FLAT FIELD

Switch selects the sequence of full-field signals.

ALL LINES position puts the signal selected by the right switch on all active lines.

ALT interleaves signals selected by the Right and Left switches on alternate lines.

FULL FIELD SIG & 3 LINES FLAT FIELD sequence is one line of signal selected by the Right switch followed by 3 lines of adjustment pedestal.

FLAT FIELD

Level switch selects amplitude and time of the FLAT FIELD signal.

PRESET

FLAT FIELD signal is controlled by the WHITE/BOUNCE/BLACK switch.

WHITE provides a full-field level between 85% and 100% of peak white. Adjustable by adjacent control.

BLACK is a level between 0% and 15% of peak white, adjustable by adjacent control.

BOUNCE switches between the preset limits of BLACK and WHITE at a rate from 1 to 10 seconds, adjustable by the BOUNCE RATE control.

FIELD SQ WAVE

A 50% duty cycle, 60 Hz squarewave with beginning and end of field at 0% level, and the center of the field at 100% peak white. (Useful in field time distortion measurements.)

VAR APL

% PEAK WHITE switch selects one of eleven levels of FLAT FIELD signal in 10% steps. (50% level is repeated for a rapid change from 0% to 50% to 100%.)

LINEARITY

Switches select components of the LINEARITY test signal.

SUBCARRIER

OFF disables all subcarrier on the LINEARITY signal.

100 mV position selects that amount of peak-to-peak subcarrier, phased at 180° from the +U axis, on the chosen LINEARITY Luminance signal.

140 mV position modulates the luminance signal with 140 mV peak-to-peak of 180° subcarrier.

5 STEPS/10 STEPS/RAMP

5 STEPS position choses a LINEARITY staircase with 5 equal steps.

10 STEPS selects a 10 step staircase.

RAMP selects a linear ramp from black to white.

MULTIBURST AMPLITUDE

700 mV position refers to peak-to peak amplitude of multiburst portion of the CCIR-II signal, centered about 350 mV pedestal.

350 mV position refers to peak-to-peak amplitude of multiburst portion of the CCIR-II signal, centered about a 350 mV pedestal.

BURST

NORM selection allows color burst to be inserted in the normal manner on the full-field signal.

OFF deletes color burst from the full-field signal.

Input Connectors

All input signals (except Remote Plug) are via BNC-type connectors.

AUX IN (1, front-panel)	75 Ω input for non-composite video type signals.
EXT VITS IN (1, rear-panel)	75 Ω input, added to composite video; output to deleter and inserter circuit. Must not have insertion signals on the lines programmed for other 148-M insertion signals. (Must not have sync and burst if not disconnected when AUXILIARY is used.)
PROGRAM LINE IN (1, rear-panel)	75 Ω input for program signal.
Remote Plug (1, rear-panel)	24-pin connector for wiring remote control functions.
COMP SYNC (1, rear-panel)	High impedance input for external synchronization of full-field signals.
PAL PULSE (1, rear-panel)	High impedance input for external synchronization of full-field signals.
BURST FLAG (1, rear-panel)	High impedance input for external synchronization of full-field signals.
SUBCARRIER (1, rear-panel)	High impedance input for external synchronization of full-field signals.

Output Connectors

All output connectors are BNC-type with 75 Ω impedance.

PROGRAM LINE (1, rear-panel)	Program output signal, with insertion signals added or deleted according to program control.
PROGRAM MONITOR (1, rear-panel)	Same as PROGRAM LINE OUT, except no output present in BYPASS mode.
PREVIEW MONITOR (2, rear-panel)	Always have insertion signals added and may have AUXILIARY added.
FULL FIELD TEST SIGNAL (1, front and 1, rear-panel	Full-field test signal.
CW SUBCARRIER (1, rear-panel)	Regenerated subcarrier signal, approximately 2 volts peak-to-peak. Not present unless locked to incoming signals.
COMPOSITE (1, rear-panel)	Regenerated sync signal, approximately 4 volts negative. Not present unless locked to incoming sync.
NOISE OUT (1, rear-panel)	Continouous random noise, variable from −20 dB to −59 dB (0 dB =700 mV).

GENERAL INFORMATION

Television signals are complex waveforms. For this reason, many test units are required to check one characteristic or another of the video system.

The 148-M is one such test unit, but it differs from others in that it will provide all the signals necessary for complete time-domain testing of a video system. All signals generated are controlled by a digital programmer that is Gen-Locked (normally), but may operate from its own oscillator. The 148-M generates the signals shown in Fig. 1-2 of this manual.

LINEARITY—Staircase, either 5 or 10 step, or ramp is available. Subcarrier (phase locked to burst) modulates either the staircase or ramp, and may be turned off by a front-panel control. Measurement of Differential Gain and Differential Phase may be made using the LINEARITY signal.

CCIR-I—This signal is a composite of the Bar, Pulse, Modulated Pulse, and Modulated 5 Step Staircase signals. These signals provide for making several types of measurements on one VITS line.

CCIR-II—This signal contains two useful test signals during one line period. It consists of a Multiburst and a Modulated Pedestal.

The Multiburst signal consists of a white flag (700 mV), and six discrete packets of frequencies from 0.5 MHz to 4.2 MHz. Each burst packet may be set for an exact number of cycles, regardless of the frequency. Multiburst is generally used for quick frequency response verification.

The Modulated Pedestal signal consists of three chrominance levels modulated on the 350 mV pedestal. This signal is useful for determining chrominance-to-luminance crosstalk.

SIG-III—Similar to the CCIR-I signal, except it has no modulation on the 5 Step Staircase.

MOD PULSE & BAR—Consists of a 12.5T Modulated Sin^2 Pulse, and a Modulated Sin^2 Bar with 12.5T rise- and fall-times. This signal is used to measure linear distortions such as chrominance-to-luminance delay and gain inequalities.

PULSE & BAR—Similar to the CCIR recommended signal, except the Bar portion of the signal is only present during the center 152 lines of each field. This signal is used for measuring linear distortions during both line and field time.

FIELD RATE SWEEP GEN—This signal consists of a sinewave that is swept in frequency from about 200 kHz to more than 6 MHz during each field period. Markers are spaced at about 1 MHz intervals. Composite sync and blanking are added to make the signal compatible with clamper circuits. The primary use of the signal is for gain vs. frequency checks.

FIELD SQ WAVE—This signal, similar to the PULSE & BAR signal, has line 74 through 206 of each field at 700 mV, thereby simulating a 60 Hz square-wave. It is capable of passing through clamper amplifiers and is used for accurate measuring of field time distortions.

FLAT FIELD—This composite video signal has, during the active portion of each field, a luminance level variable from 0 to 700 mV in 10% increments, or which bounces automatically between the black and white level at a repetition rate of approximately 1 to 10 seconds. It is used to test clamped amplifiers and systems in general, and for APL-dependent distortions.

NOISE—The calibrated noise generated provides white noise (flat) at 50, 250, or 700 mV luminance levels. This offers a unique signal-to-noise measuring technique, which may be performed during the vertical interval.

FIRST TIME OPERATION

General

The following is primarily intended to familarize operating personnel with the operation of the 148-M. It consists of a step-by-step procedure, which makes use of each front- and rear-panel control and connector. This procedure in most cases simulates the actual in-service operation of the 148-M.

The procedure makes use of a waveform monitor to observe field and line rate displays and a vectorscope to observe phase characteristics. An external video signal source is needed to provide program signal (composite video) and an external Vertical Interval Test Signal (VITS). The following equipment is used: Tektronix 1482 Waveform Monitor, used to observe field and line rate displays; a Tektronix 522A Vectorscope, used to observe phase characteristics; and a Tektronix 145-M Test Signal Generator, used to provide the external video signals. Proper operation of each unit is assumed; refer to the individual operating instructions for each.

Unless stated otherwise, all 148-M front- and rear-panel controls and connectors are in upper-case letters and all other controls and connectors have initial upper-case letters only.

The procedure is arranged in a sequence that depends upon previous control settings and connections, and should be performed in sequence. There are, however, certain places where all equipment is disconnected before starting a step, allowing the operator to start the procedure at this point if desired.

NOTE

The following procedure uses the equipment listed. If substitute equipment is used, control settings and connections may need to be altered .

Procedure

1. Remove the REMOTE plug, P9014.

2. Set the 148-M controls as follows:

Control	Position
INSERTION SIGNAL CONTROL	UNITY GAIN, PROGRAM, and LOCAL
SYNC	INT
POWER	off
NOISE AND PEDESTAL	DELETION, 700 mV, OFF, and 0 dB
FULL FIELD SIG	LINEARITY (Left and Right Selectors) ALL LINES
LINEARITY	5 STEP, 140 mV SUB-CARRIER
MULTIBURST AMPLITUDE	700 mV
FLAT FIELD	PRESET, BLACK 0-15%, and 100% PEAK WHITE
BURST	NORM

3. Check 148-M Range and Voltage selectors for correct positioning.

4. Set the POWER switch ON. Note that the green power-on light, the red NOT LOCKED TO PROGRAM light, and the red BYPASS light are all on.

NOTE

Without Gen-Lock, the 148-M will not delete or insert VITS.

5. Connect the 148-M front-panel FULL FIELD TEST SIGNAL OUT to the Waveform Monitor A Input; terminate the loop-through A Input into 75 Ω.

6. Using the 2 Field Display rate of the Waveform Monitor, note that composite sync and burst are the only signals being generated. Set the Waveform Monitor to the 10 μs/Div position.

7. Connect the REMOTE plug, P9014. Note that the 5 Step LINEARITY signal is now displayed, and the green PROGRAM light is on.

8. Change the LINEARITY switches to display the 10 Step and Ramp LINEARITY signals modulated by the amount of chrominance selected by the SUBCARRIER switch. Return the switches to display the 5 Step signal with 140 mV modulation.

9. Set the FULL FIELD SIG (Right) selector switch to FLAT FIELD. The Waveform Monitor will display a level between 0% and 15% of peak white. Using a small-bladed screwdriver, adjust the BLACK 0-15% control. The level will change from 0% to 15% of peak white.

10. Set the WHITE/BOUNCE/BLACK switch to WHITE. The level should now be between 85% and 100% of peak white. Adjust the WHITE 85-100% control to check its range.

11. Set the WHITE/BOUNCE/BLACK switch to BOUNCE. The signal level will alternate between the limits of BLACK and WHITE, as set by the 0-15% and 85-100% controls. Turn the BOUNCE rate control through its range. The rate of alternation between BLACK and WHITE will vary according to the setting of this control.

12. Set the FLAT FIELD mode switch to FIELD SQ WAVE, and the Waveform Monitor to a 2 Field Display rate. Note that the signal resembles a 60 Hz square-wave. Return the Waveform Monitor to 10 μs/Div.

13. Set the FLAT FIELD mode switch to VAR APL. Look for a 100% peak white (700 mV) level on the signal. Change the VAR APL switch through its settings and note the correct amplitude on the Waveform Monitor. The 50% level is repeated between the 0% and 100% positions to allow quick APL shifts.

14. Set the FULL FIELD SIG (Right) selector switch to FIELD RATE SWEEP GEN. This signal is a swept frequency sinewave, modulated on a 350 mV pedestal. Change the Waveform Monitor to a 2 Field Display rate. See that the modulation is blanked seven times per field. These blanked spots (markers) are spaced at about 1 MHz intervals. Return the Waveform Monitor to the 10 μs/Div Display rate. Set the MULTIBURST AMPLITUDE switch to 350 mV. The amplitude of the FIELD SWEEP GEN modulation goes from 700 mV to 350 mV.

15. Set the FULL FIELD SIG (Right) selector switch to CCIR-II. This signal will be the same as shown in Fig. 1-2. Set the MULTIBURST AMPLITUDE switch to 700 mV. Notice that only the MULTIBURST packets change amplitude, going from 350 mV to 700 mV.

16. Check the remaining positions of the FULL FIELD (Right) selector switch; CCIR-I, SIG-III, MOD PULSE & BAR, and PULSE & BAR. See that these signals match those shown in Fig. 1-2.

17. Set the FULL FIELD SIG mode switch to ALT. Set the right hand selector to FLAT FIELD, and the left hand selector to LINEARITY. The FLAT FIELD and LINEARITY signals will look superimposed. Change the left and right hand selectors to see that all of the signals selected by the left hand selector can be superimposed with all of the signals selected by the right hand selector. Set the Waveform Monitor to a 2 Field Display rate, with the horizontal Mag at X50. Position the display to show the active portion of a field. The signals will appear on alternate lines throughout the field.

18. Set the FULL FIELD SIG mode switch to FULL FIELD SIG & 3 LINES FLAT FIELD. The signal chosen by the right hand selector will be on every fourth line with the remaining three lines having the FLAT FIELD SIGNAL. The usual way to use this feature is to select a LINEARITY signal and vary the VAR APL % PEAK WHITE switch from 0% to 50%, then to 100%. This makes quick measurements for APL dependent distortions. Return the FULL FIELD SIG mode switch to ALL LINES.

19. Set the Waveform Monitor Mag to Off, and to 10 μs/Div Display rate. Turn the BURST switch off. Burst is removed from the composite video signal on the Waveform Monitor. Return the BURST switch to the NORM position.

NOTE

In steps 8 through 19, each FULL FIELD TEST SIGNAL has been demonstrated. Also, these signals were demonstrated in a free-running mode. In the free-running mode, the subcarrier free-runs at approximately 3.58 MHz.

In the steps to follow, the procedure will, where possible, simulate the actual in-service operation of the 148-M.

20. Using 75 Ω coaxial cables and 75 Ω terminations make the following connections:

a. 148-M PROGRAM OUTPUT LINE to Waveform Monitor A Input, A Input loop-through to the Vectorscope CH A input; terminate CH A loop-through into 75 Ω.

c. External Video Source subcarrier to the Vectorscope Ext CW ϕ Ref Input, terminate Ext CW ϕ Ref loop-through into 75 Ω.

d. External Video Source composite sync to the Waveform Monitor Ext Neg Sync Input, Ext Neg Sync Input loop-through to Vectorscope Ext Sync Input, terminate Ext Sync Input loop-through into 75 Ω.

e. External Video Source composite video to the 148-M PROGRAM INPUT.

21. Set the 148-M controls and switches as given in step 2 of this procedure, except set the POWER switch ON and the INSERTION SIGNAL CONTROL to PREVIEW. Set the Vectorscope to view the CH A Input (PROGRAM OUTPUT LINE) in a vector mode using external sync and ϕ reference. Set the Waveform Monitor to view the A Input (PROGRAM OUTPUT LINE) at a 2 Line Display rate using external sync. Set the External Video Source for full-field color bars with a Vertical Interval Test Signal (this procedure makes use of a modulated staircase VITS) on lines 13/276, both fields.

22. Notice that the 148-M front-panel NOT LOCKED TO PROGRAM lamp is extinguished. This indicates the 148-M has been Gen-Locked with the external video and is capable of deletion and insertion. (If this lamp is lit, check that the SYNC switch is set to INT.)

23. Notice that the 148-M PREVIEW lamp is lit to indicate status. In this mode, the external video to the PROGRAM INPUT is being passed to the PROGRAM OUTPUT without interruption, as indicated by the Waveform Monitor and Vectorscope displays.

24. Observe the Waveform Monitor B Input (PREVIEW OUTPUT) at a 2 Field Display rate (use maximum magnification if desired). Notice that the internally generated VITS have been added to the signal. The signal appearing at the PREVIEW OUTPUT in the PREVIEW mode allows the operator to observe the actual signal after insertion without actually going to an "on-the-air" mode of operation.

25. Using Table 2-2, check that all VITS are being inserted on the correct line and field.

26. Set the 148-M INSERTION SIGNAL CONTROL to PROGRAM. Observe the Waveform Monitor A Input (PROGRAM OUTPUT LINE). Notice that the internally generated VITS have been applied to the "on-the-air" signal. Note also that the 148-M front-panel PROGRAM lamp is lit to indicate status.

TABLE 2-2

148-M Factory Commands
VITS Programming

Line	Fields	Signal
14/277	All	NOISE
15/278	All	LINEARITY
16	1,3	SIG-III
17	1,3	CCIR-I
279	2,4	MOD PULSE & BAR
280	2,4	CCIR-II

27. Set the External Video Source to provide a VIT Signal on one of the lines that has been programmed for insertion by the 148-M. Observing the Waveform Monitor display, set the 148-M POWER switch OFF. Note that the external VIT Signal is being displayed. This indicates that external video has bypassed the 148-M, and demonstrates the fail-safe characteristic of the 148-M should loss of power, sync etc., occur during "on-the-air" (PROGRAM) situation. Return the POWER switch to ON.

28. Observing the Waveform Monitor display, interrupt the external composite video to the 148-M PROGRAM INPUT. Notice that the display now consists of the Full-Field signal (as set by the FULL FIELD SIG switch) generated by the 148-M. In the event of loss of incoming video, the 148-M provides internally generated Full-Field test signals at the PROGRAM OUTPUT. (For exception, see Operating Changes, this section for details.) Return the external composite video signal to the 148-M PROGRAM INPUT.

29. Set the Waveform Monitor to view line 14, fields 1 and 3. Set the External Video Source to provide a VIT Signal on line 14, fields 1 and 3. This signal is controlled by the NOISE AND PEDESTAL controls. Set the PEDESTAL (mV) switch to 350 mV, then 50 mV, and back to 700 mV. Note that the pedestal amplitude corresponds to the setting of this switch. (In the DELETION mode, this is the only switch affecting the signal.) Set the NOISE switch to INSERTION. The display should be similar to that obtained in the DELETION mode. Rotate the VARIABLE control. Note that the pedestal level can be changed above and below the level determined by the setting of the PEDESTAL switch. Set the NOISE LEVEL dB switches for −20 dB. Notice that noise has been added to the pedestal. Turn the dB switches through their ranges. They provide noise attenuation from −20 dB to −59 dB in 1 dB steps. (700 mV RMS = 0 dB). Set the dB switches for −20 dB. Rotate the VARIABLE control to center the noise about the 700 mV level.

NOTE

Actual in-service noise measurements will require the use of a 4.2 MHz low-pass filter between the output of the 148-M and the input of the waveform monitor. If triangular noise must be measured, a 4.2 MHz weighting filter should be used. (See Fig. 2-5.)

30. Set the External Video Source to provide a VIT Signal on one of the lines programmed for internal VITS. Observe the Waveform Monitor B Input (PREVIEW OUTPUT) at a 2 Field Display rate. Notice that the external VITS has been deleted. Next, connect an external VIT Signal to the 148-M rear-panel EXT VITS INPUT. Do not terminate the line. (If using a Tektronix Type 145-M Test Signal Generator as the External Video Source, connect the unused Comp Video connector to the 148-M EXT VITS IN connector.) Notice that the external VITS (via the EXT VITS INPUT) has been added to the internally programmed VITS, causing the display to be distorted. This demonstrates why **external VITS to the EXT VITS INPUT must not be programmed on the same line and field as internal VITS.**

31. Observing the Waveform Monitor A Input at a 2 Field Display rate and the Vectorscope CH A Input vectors (both are PROGRAM OUTPUT), set the 148-M INSERTION SIGNAL control to PROGRAM, VAR, and rotate the LEVEL control. The amplitude of the external composite video can now be varied with this control. Observe the vertical interval on the Waveform Monitor with maximum magnification. Rotation of the LEVEL control should not affect the inserted test signals. Turn off the Waveform Monitor magnification and adjust the LEVEL control for an overall signal amplitude of 1 volt peak-to-peak. The LEVEL control allows the operator to match incoming program composite video to the internally generated signals. Set the INSERTION SIGNAL CONTROL to UNITY GAIN.

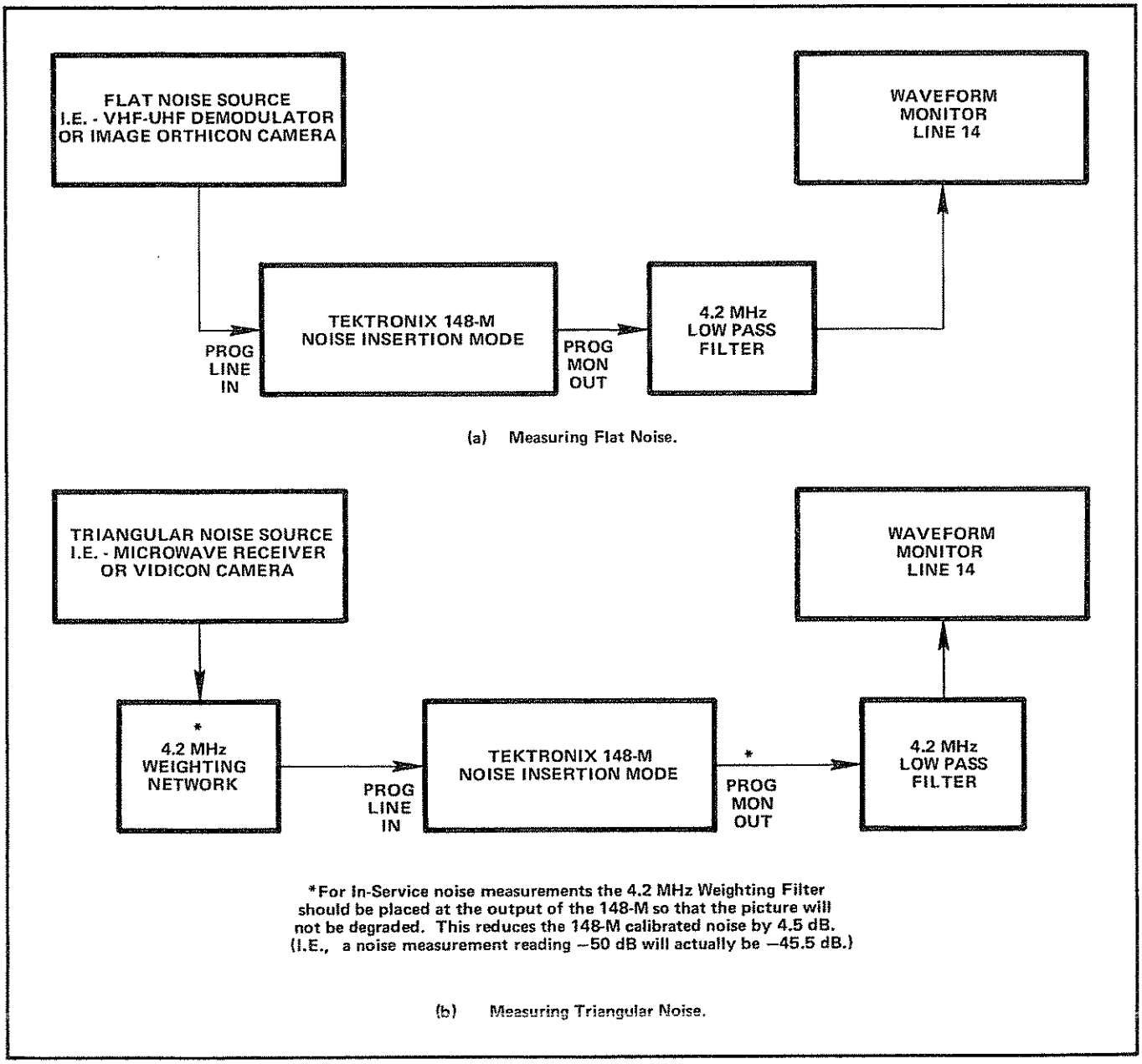
32. Observing the Vectorscope display, rotate the INSERT SUBCARRIER PHASE control. There will be a vector representing the internally generated subcarrier. Set the internal subcarrier to exactly 180° from the +U axis. The INSERT SUBCARRIER PHASE control enables the operator to match the phases of the internal and external subcarriers.

33. Set the 148-M INSERTION SIGNAL CONTROL to AUX and view the Waveform Monitor B Input (PREVIEW OUTPUT) at a 10 μs/Div Display rate. Sync and burst should be double amplitude. Disconnect the 75 Ω cable from the 148-M rear-panel EXT VITS INPUT. Sync and burst should be normal amplitude. This demonstrates why **in AUXILIARY mode and with an external VITS input, there must be no SYNC or BURST added with the external VITS.**

34. Observing the Wavefrom Monitor display, rotate the INSERTION SIGNAL CONTROL PEDESTAL control. Notice that an apparent square-wave can be adjusted from below blanking to greater than 700 mV. Display the PROGRAM MONITOR OUTPUT in place of the PREVIEW OUTPUT on the Waveform Monitor B Input. Notice that there is no output from this connector. Display the Waveform Monitor A Input (PROGRAM OUTPUT). Notice that external composite video is being displayed. The auxiliary signal will only be available at the PREVIEW OUTPUT. In addition, this is the only mode of operation where the PROGRAM OUTPUT and PROGRAM MONITOR OUTPUT do not have the same signals.

35. Display the PREVIEW OUTPUT in place of the PROGRAM MONITOR OUTPUT on the Waveform Monitor B Input. Apply the NOISE OUT signal from the 148-M rear-panel to the front-panel AUXILIARY INPUT connector. Notice that the NOISE signal applied to the AUXILIARY INPUT has been added to the auxiliary pedestal level. Position the auxiliary level to locate all of the NOISE signal between the blanking level and peak white.

36. Set the 148-M INSERTION SIGNAL CONTROL LOCAL/AUX/REMOTE switch to REMOTE. Note that the



(a) Measuring Flat Noise.

*For in-Service noise measurements the 4.2 MHz Weighting Filter should be placed at the output of the 148-M so that the picture will not be degraded. This reduces the 148-M calibrated noise by 4.5 dB. (I.E., a noise measurement reading −50 dB will actually be −45.5 dB.)

(b) Measuring Triangular Noise.

Fig. 2-5. Noise measurement setups.

PREVIEW lamp is lit to indicate status (unless PROGRAM/PREVIEW/BYPASS switch is in BYPASS, then BYPASS lamp is lit at all times). Observe the Waveform Monitor A Input first at a 2 Line Display rate, then a 2 Field Display rate. The external composite video should be appearing at this output without interruption.

37. Display the 148-M rear-panel NOISE OUT on the Waveform Monitor A Input; terminate the A Input loop-through into 75 Ω. Change the NOISE AND PEDESTAL switches. Note that the noise amplitude is controlled only by the NOISE LEVEL dB switches. The signal at this output is continuous (e.g., no line or field sync).

NOTE

An in-line low pass filter must be used with the NOISE OUT connector.

38. Display the 148-M rear-panel COMP SYNC OUTPUT on the Waveform Monitor. Set the Waveform Monitor for a 10 μs/Div Display rate. There will be a very large amplitude (4 V) sync pulse displayed. The bottom of the pulse will be off-screen. Set the 148-M SYNC switch to EXT. The sync pulse will disappear. The 148-M must be Gen-locked to produce an output at this connector. Return the SYNC switch to INT.

39. Connect the 148-M rear-panel CW SUBCARRIER OUTPUT to the Waveform Monitor. Terminate the loop-through into 75 Ω. The subcarrier will fill the screen of the Waveform Monitor. Set the SYNC switch to EXT. The subcarrier will disappear. The 148-M must be Gen-Locked to produce an output at this connector also.

40. Observing the Waveform Monitor display at either a 2 Line or 2 Field Display rate, set the 148-M SYNC switch to EXT. The display should be free-running and the red NOT LOCKED TO PROGRAM lamp should be lit. From the External Signal Source, connect, COMP SYNC, SUBCARRIER, BURST FLAG, and PAL PULSE to the respective input connectors on the 148-M rear-panel. Note that the red NOT LOCKED TO PROGRAM lamp is extinguished and that the display is locked.

This completes the first-time operating procedure.

OPERATING CHANGES

General Information

The 148-M is factory connected to generate test signals that are most frequently used by the television industry. However, many internal changes can be made to alter these signals to meet certain applications.

The following provides information necessary to change or modify the 148-M.

NOTE

Some of the changes or modifications that follow require internal adjustment and programming to comply with industry standards. We recommend that only qualified personnel, thoroughly familiar with calibration procedures and the video signals, make these changes.

Full Field Burst

As shipped from the factory, loss of burst on the PROGRAM IN signal (or loss of PAL pulse, burst flag, or subcarrier in the EXT SYNC mode) will cause the 148-M burst and subcarrier components of the FULL FIELD TEST SIGNALS to free run.

If desired, the free-running burst may be automatically removed from the FULL FIELD TEST SIGNALS with loss of incoming burst. Change the connector on pins 1 and 2 of P482 to pins 2 and 3 (P482 located on the Subcarrier and Sync Out circuit board, see Fig. 2-6).

Loss of Program (PROGRAM mode only)

As shipped from the factory, the FULL FIELD TEST SIGNALS are routed to the PROGRAM OUTPUT LINE in the event that the PROGRAM INPUT signal is interrupted. If desired, the 148-M may be connected so that the PROGRAM OUTPUT LINE is interrupted if the PROGRAM INPUT signal is interrupted. This is accomplished by disconnecting pins 22 and 23 of the remote plug, P9014. (P9014 is located on the rear-panel, see Fig. 2-1.)

ALT & 6 Lines Flat Field

As factory-set, the 148-M will generate a Full Field Signal and 3 lines of Flat Field, when that position of the FULL FIELD SIG Mode switch is selected. To generate Alternate Full Field Signals and 6 lines of Flat Field, move P430 from pins 2 & 3 to pins 1 & 3. This position allows the signal selected by the right hand FULL FIELD SIG Selector switch to be alternated with the signal selected by the left hand switch, followed by 6 lines of Flat Field (retaining the approximate APL percentage). See Fig. 2-6 for location of P430 on the Sync and Subcarrier circuit board.

Line and Field Selection

Vertical Interval Test Signals (VITS) may be selected to appear on lines 10/273 through 18/281 of fields 1 and 3, fields 2 and 4, or all fields. Line and Field selection is accomplished by selecting various internal quick-change pin connectors on the VITS and FF circuit board, see Fig.

2-7. An access door is provided so that VITS selection can be made without removing the top cover from the instrument.

Referring to the VITS and FF circuit board, notice that a rectangular matrix is used to select the Line and Field for each VITS. Two jumper plugs must be used to select the VITS; one for field selection, the other for line selection.

To prevent or disable a particular VITS, move the line jumper plug to the OFF position.

Each matrix row is color-coded to help identify its associated VIT Signals. This color code is listed in Table 2-3 and Fig. 2-7.

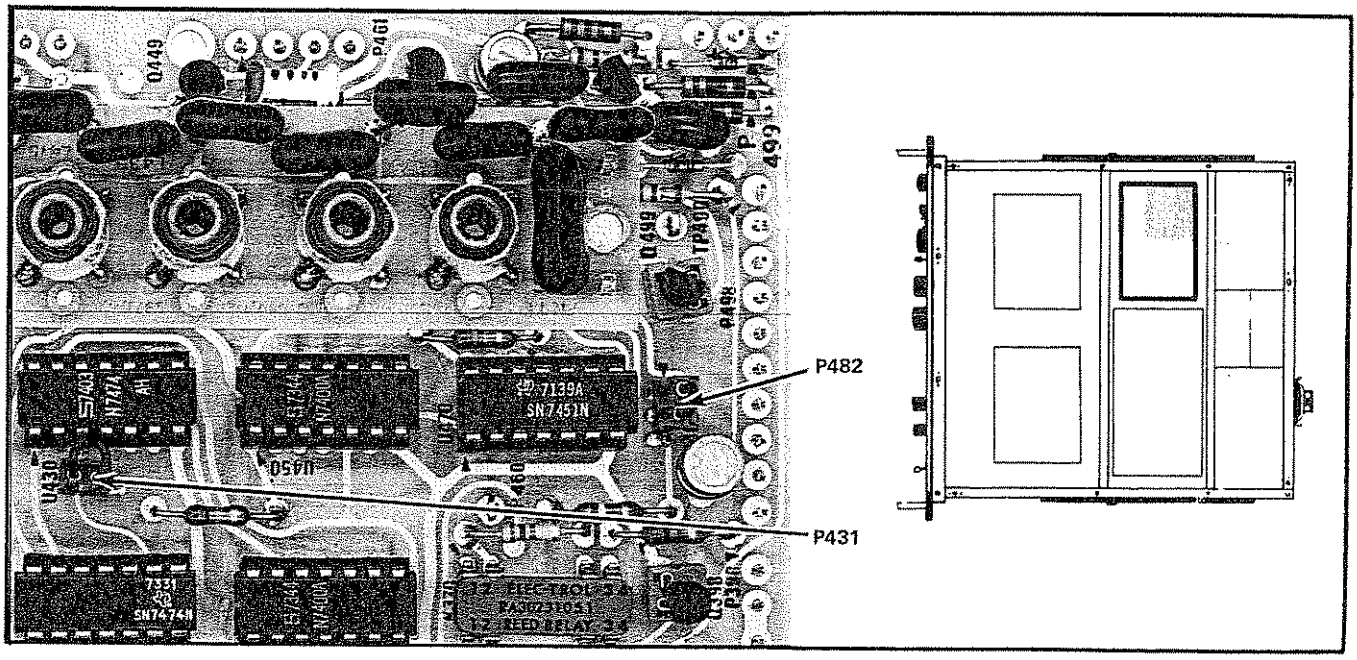


Fig. 2-6. Subcarrier and Sync circuit board showing location of P482, Full Field Burst; and P431, ALT & 6 LINES APL.

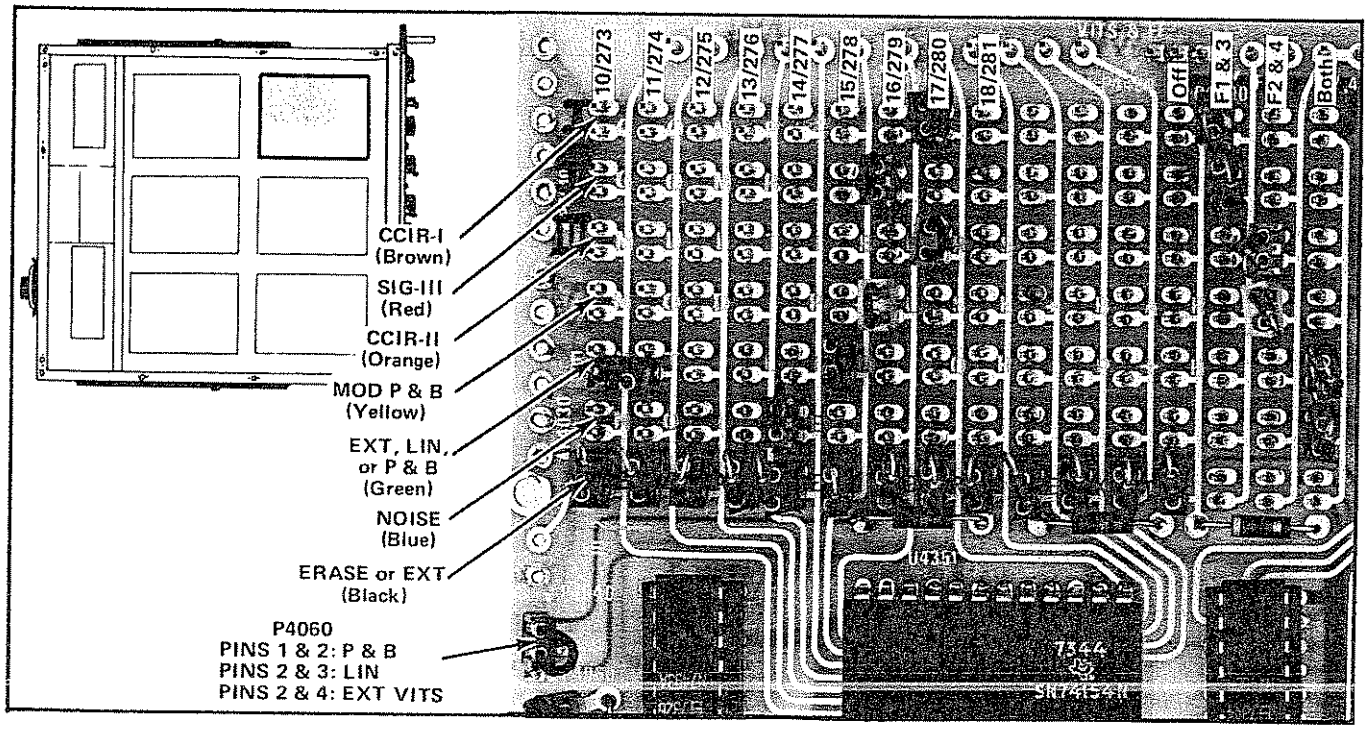


Fig. 2-7. VITS and FF circuit board showing locations of VITS Line and Field selector plugs; VITS Line and Field selection.

TABLE 2-3

VIT Signals	Connector Color
CCIR-I	Brown
SIG-III	Red
CCIR-II	Orange
MOD PULSE & BAR	Yellow
EXT, LIN, or P & B	Green
NOISE	Blue
ERASE	Black

Ext—Linearity—P & B

The operator may select any line from 10/273 through 18/281 of fields 1 and 3, fields 2 and 4, or all fields as follows:

LINEARITY—Pins 2 and 3 of P4060 must be connected.

P & B (Pulse & Bar)—Pins 1 and 2 of P4060 must be connected.

EXTERNAL—Pins 2 and 4 of P4060 must be connected. External VITS applied to rear-panel EXT VITS connector. External VITS only on above programmed line and fields.

NOTE

Any signal applied to EXT VITS IN will add to internally programmed signals if inserted on same line(s).

If sync and burst are present at EXT VITS IN they will add to PREVIEW outputs in AUX and BYPASS. They will also add to FULL FIELD SIGNAL OUT, and PROGRAM LINE OUT (if there is loss of PROGRAM IN).

Erase

Any incoming VIT Signals may be erased (deleted) by the 148-M in the Erase mode. As factory-programmed, incoming VITS on the PROGRAM LINE IN will be deleted only if a 148-M VIT Signal is programmed for the same line and field. To erase incoming VITS that are not already being deleted, connect one of the spare Erase jumpers (cathode inboard) to the desired field and line selection pins in the Erase matrix. Any incoming VITS on the selected field(s) will be erased. To allow a particular VITS to pass, while erasing other incoming VITS, remove (or reverse) the Erase jumper from the matrix line selected. (See Fig. 2-7.)

2T/T Sine-Squared Pulse

As shipped from the factory, the 148-M generates the 2T Pulse. To display the T Pulse in place of the 2T Pulse, (1) change the connector on pins 1 and 2 of P7131 to pins 2 and 3, and (2) change the connector on pins 5 and 6 of P7321 to pins 4 and 5. (P7131 and P7321 are located on Output circuit board, see Fig. 2-8.)

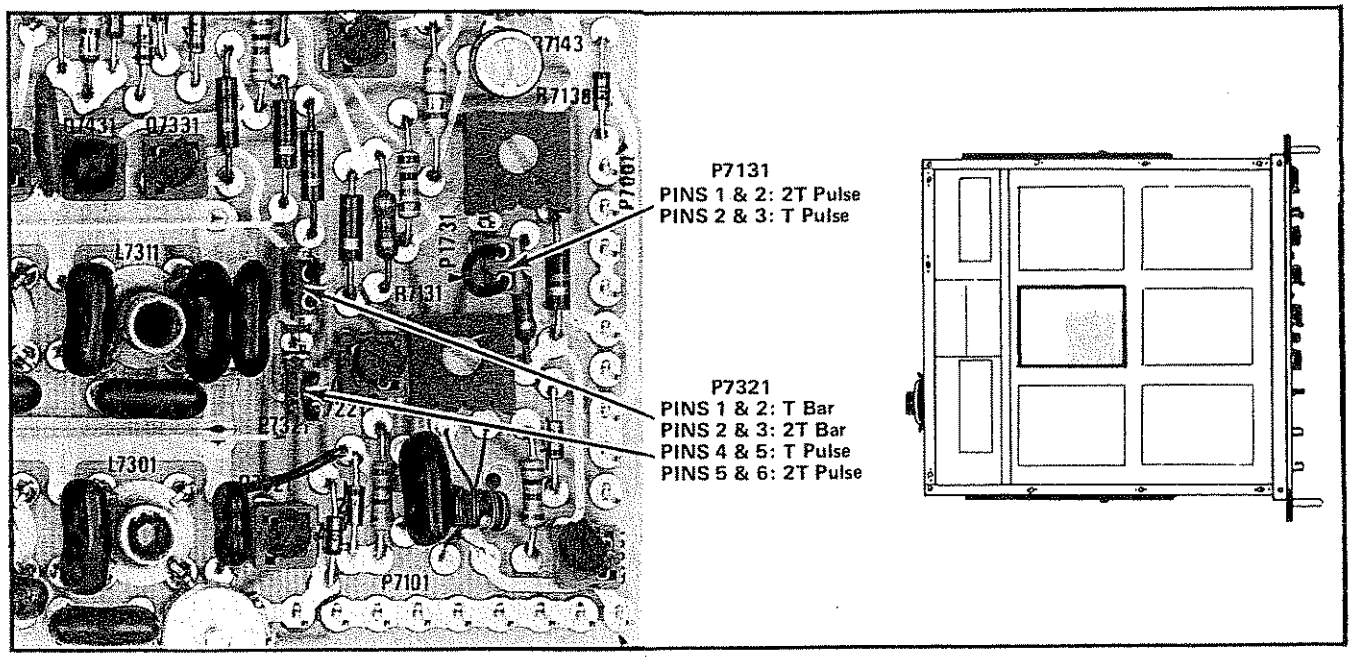


Fig. 2-8. Output circuit board showing locations of P7131 and P7321; 2T/T sine-squared Pulse and T/2T Bar (Integrated Sine-Squared Pulse).

T/2T Bar (Integrated Sine-Squared Pulse)

As shipped from the factory, the 148-M generates the T Bar. To display the 2T Bar in place of the T Bar, change the connector on pins 1 and 2 of P7321 to pins 2 and 3.

Field Sweep Markers

The FIELD RATE SWEEP GEN signal has 7 markers per field, as factory-shipped. To get 3 markers per field, move P1031 so that pin 1 of the connector goes to pin 2 on the circuit board. (See Fig. 2-9.)

Gen-Lock, Burst or CW (Residual Subcarrier)

As shipped from the factory, the 148-M will Gen-Lock to signals containing composite sync with subcarrier present during the burst time interval. In this mode, sound-in-sync will not affect lock.

If desired, the 148-M may be programmed to lock to burst, in the presence of residual subcarrier, without phase shift due to residual subcarrier. This mode should not be used in the presence of sound-in-syncs since the 148-M system uses residual subcarrier at sync time as a reference. Change the connector on pins 2 and 3 of P5150 to pins 1 and 2. (P5150 is located on Gen-Lock circuit board, see Fig. 2-10.)

Horizontal Programming

The 148-M test signal components, shown in Fig. 1-2, and detailed in Table 2-4, are timed by the digital programmer on the Horizontal Timing circuit board. The programmer consists of 32 columns of pin connectors, each column corresponding to a characteristic instant. The characteristic instants are spaced at 2 μs intervals. (The exact spacing is $\frac{63.56\ \mu s}{32} = 1.98625\ \mu s$.)

All wires and connectors which program the 148-M are color coded. (See Fig. 2-11.)

It is possible to reprogram the 148-M to provide test signals with components occuring at selected times. Assume that a user wishes to program the STOC-TV[2] recommended composite signal in place of the CCIR-I composite signal. (See Fig. 2-12.) This signal differs from the CCIR-I signal by placing the Modulated Staircase at the start of the line, and the Bar at the end of the line. The user should determine the characteristic instants that correspond to the functions to be programmed. These instants can be written down in the Instant Timing column of Table 2-4, next to the original timing, for a record of the change. For all components of the new signal, find the program wire of the original signal, and move it to the new instant. For example, to program the Bar portion, move the Set wire (red connector, 9-6 wire) from instant 6 to instant 21. Move the Reset wire (black connector 9-06 wire) from instant 15 to instant 31. Using Table 2-4 and Fig. 2-12 as guides, the rest of the signal, and many other combinations can be programmed.

[2]Satellite Technical and Operational Committee—Television

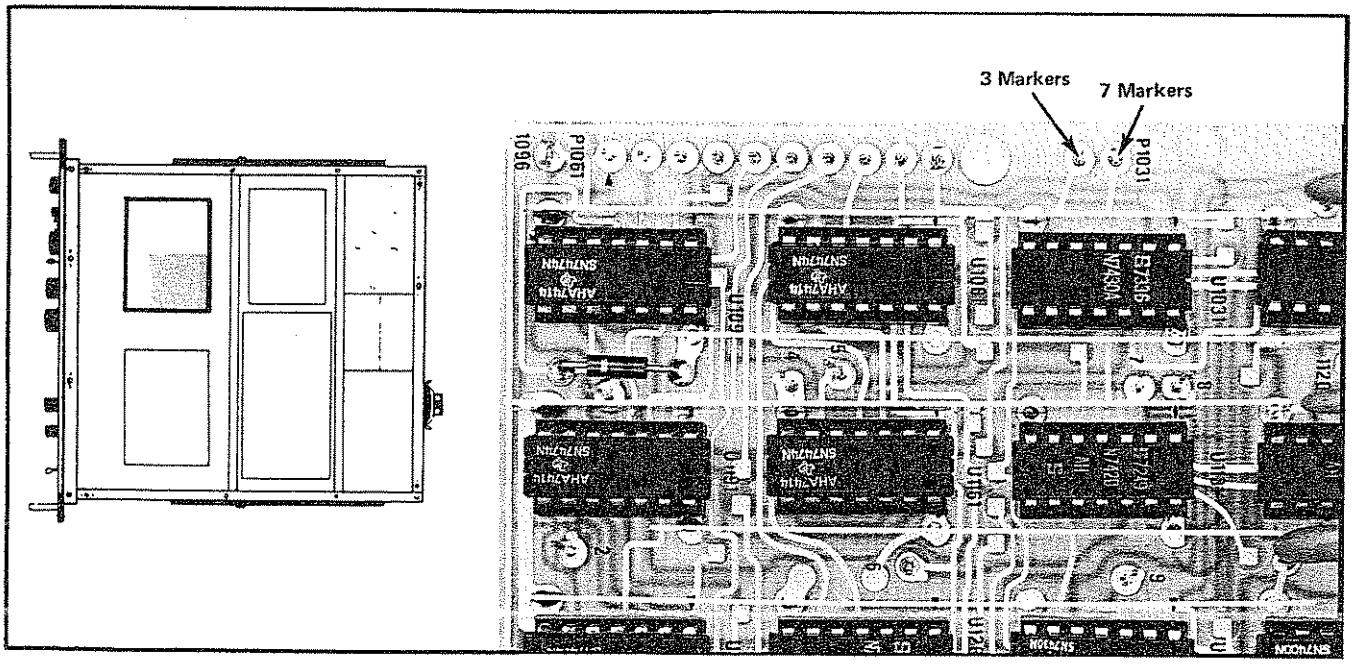


Fig. 2-9. Horizontal and Vertical Counter circuit board showing location of P1031; Field Sweep markers.

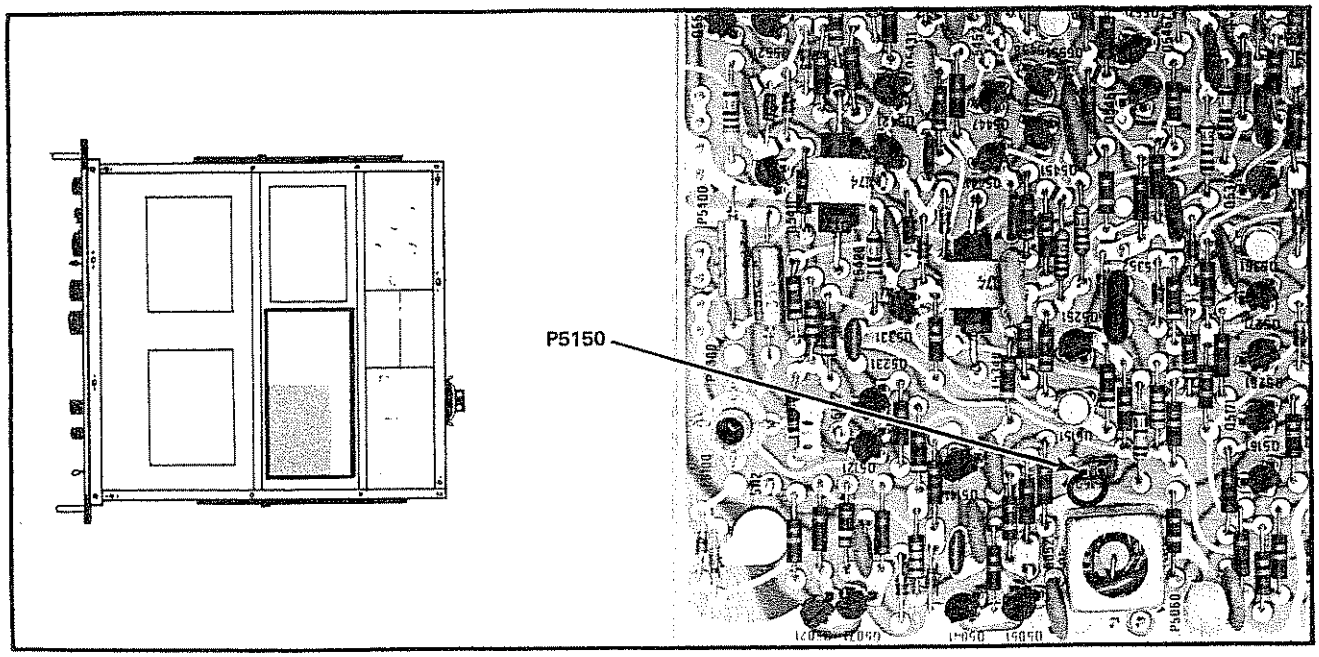


Fig. 2-10. Gen Lock circuit board showing location of P5150; Genlock Burst or CW (Residual Subcarrier).

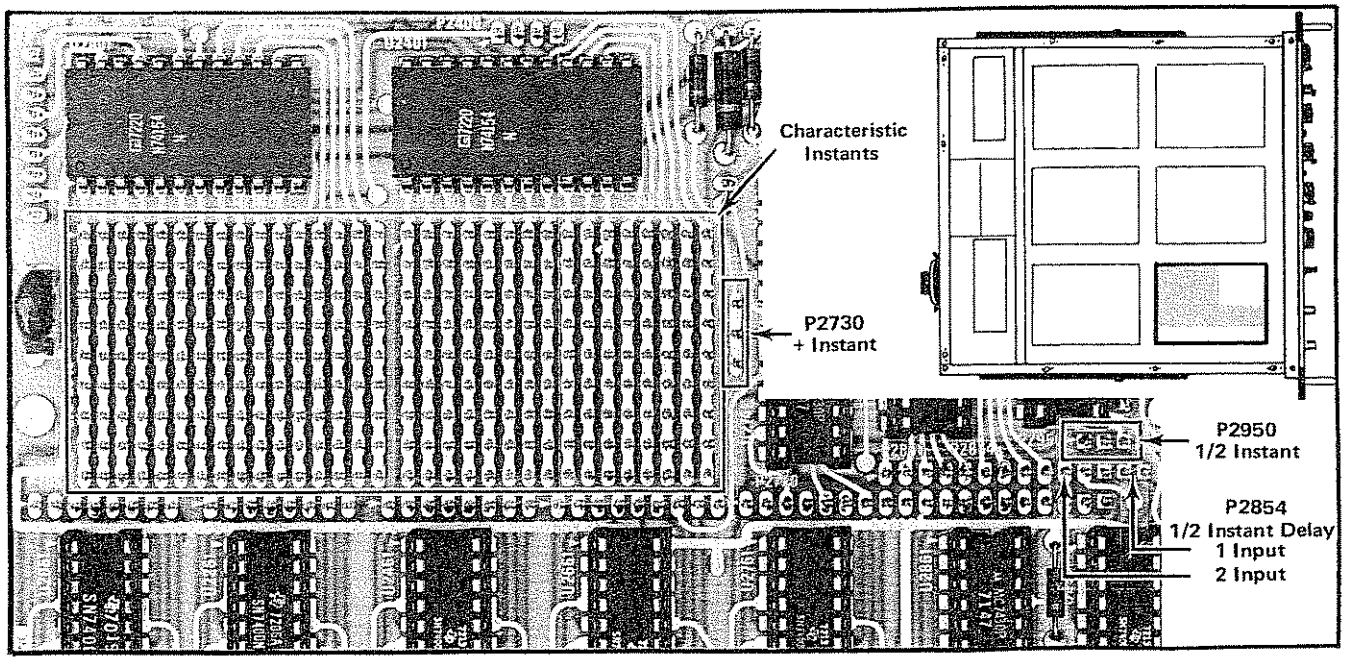


Fig. 2-11. Horizontal Timing circuit board showing locations of Characteristic Instants (use with Table 2-4); Horizontal Programming.

TABLE 2-4 (cont)

Factory Horizontal Programming

Signal	Affected Portion	Function	Connector Color Code	Timing Instant	Key To Table	
					Instant	Wires
PULSE & BAR	Pulse	Set	1	11		
	Var	Set	1	16		
		Reset	1	29		
	Mod Pulse (Disabled)	Set	4	[4]		
		Reset	1	9		
FIELD RATE SWEEP GEN	Modulation Enable	Set	0	7		
		Reset	2	29		
MOD PULSE & BAR	Modulated Pulse	Set	2	8		
	Modulated Bar	Set	0	16		
		Reset	0	29		
NOISE	1/2 Line Insert	Set	0	12		
		Reset	0	24		
SPARE	(Unused outputs)	Set	3	8		
		Reset	0	10		

[4]The Mod Pulse may be enabled by removing the connector from P2730-2 and connecting it to instant 8.

CIRCUIT DESCRIPTION

General

This section of your manual describes the electrical operation of circuits within the 148-M. The description is organized with respect to the schematic diagrams.

The 148-M can be considered as in Fig. 3-1. Basically, the 148-M consists of (1) A relay to provide bypass in the event of loss of power or when the instrument is in the bypass or auxiliary modes, (2) Sync and Subcarrier processing circuits to detect synchronization information, (3) Timing circuits to provide gate signals used for generation of the output signals, (4) Test Signal Generator to generate the various output signals, (5) Program Control Switching to allow the operator to select the mode of operation, (6) Electronic Switches to route all signals to the proper outputs at the proper time, and (7) Output Amplifiers to provide sufficient current to drive the outputs.

Block Diagram

The block diagram relates the schematic circuitry to the operation of the 148-M, and is a transition between Fig. 3-1 and the schematic diagrams.

DIAGRAM ⓪a and ⓪b

The circuitry shown on Diagram 0_a (Program Line Amplifier) is used to condition the input signal applied to the PROGRAM INPUT for further processing (required for insertion of signals) and selects the mode of operation. The circuitry shown on Diagram 0_b (VITS Inserter) routes both internally generated and externally applied signals during selected intervals so that a composite of each is available at the PROGRAM OUTPUT LINE, PROGRAM MONITOR OUTPUT, or PREVIEW OUTPUT connectors.

Relay

The relay circuitry is used to bypass the program signal to the PROGRAM OUTPUT LINE in the event of circuit failure, loss of power, etc., or apply the program signal to the active circuits within the 148-M for processing.

Bypass Indicator

This stage, consisting of emitter follower Q580, detects the condition of the bypass relay. The output of Q580 will be at or near ground when the relay is energized. The output will be around +5 volts if the relay is not energized. This information is used for three purposes. First, the output, which goes to U761-6, turns off the program switch and prevents any signal from entering the program output amplifier. This ensures that there is no signal present on the open contacts of the bypass relay that might cause crosstalk into the program lines. Secondly, the output of this stage is used, as shown on Diagram 4, to operate the bypass indicator lamp. The third use of this signal relates to the auxiliary mode of operation. In this mode of operation the timesharing of the internally generated signals and the incoming signals is reversed. A high output from the Bypass Indicator stage enables U4381A to reverse the VITS Key timing.

Program Amplifier

The Amplifier stage is an ac coupled operational amplifier with unity gain or variable gain (front-panel LEVEL) of the program signal. Coupling Capacitor C520 removes any dc component that may be applied via the PROGRAM LINE IN.

Q540 provides constant current for emitter-coupled amplifier Q510-Q520. Current through Q520, set by R9205 (LEVEL) or R505 (dependent upon the setting of S9205, UNITY GAIN/VAR), flows through R625 (Rf of operational amplifier Q620-Q630) to set the overall circuit gain. The signal at TP820 is applied to the VITS switches (after dc restoration). R720 and CR720 balance out any residual differential phase that may be present in the program amplifier. CR720 is installed either forward or backward, depending on the nature of the differential phase that is present. Refer to the Calibration Procedure for further information.

Back Porch Gate Generator

The stage is used to generate a pulse during back porch time to drive the Back Porch Clamp circuitry.

Q905, normally on, is driven by composite sync (negative-going). On the trailing edge of each sync pulse, Q905 turns off (current shunted via Q900), producing a pulse that is differentiated by C910 and R926. When Q905 turns back on, the differentiated pulse turns Q920 (normally on) off. A negative-going pulse, which has been delayed from sync, is obtained at the collector of Q920,

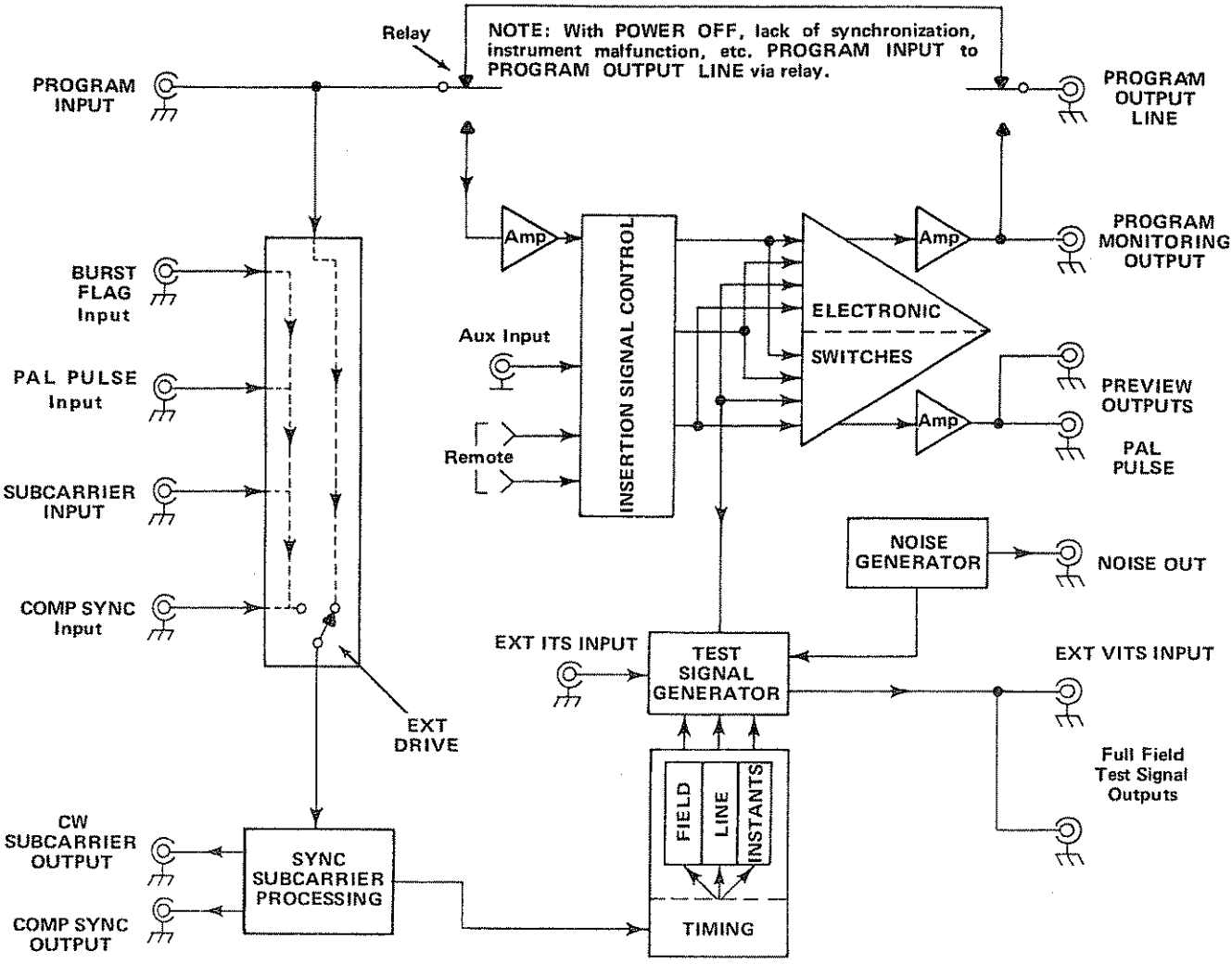


Fig. 3-1. Basic block diagram of the 148-M.

such that during back porch time, the circuit dc-restores the signal appearing at TP801. The pulse-forming circuitry acts like two monostable multivibrators. The first one, consisting of Q900 and Q905, forms the delaying time necessary following the trailing edge of sync. The second monostable consists of Q905 and Q920; it forms the actual clamping pulse.

Back Porch Clamp

Q820 is the active circuit element of this stage. During back porch time, it is biased on and effectively grounds TP801. This dc-restores the signal via C804 in the amplifier stage.

Program Control Switching

Consisting of S9212 and S9213, this stage selects the mode of operation: PROGRAM, PREVIEW, or BYPASS, and REMOTE, AUX, or LOCAL.

VITS Switches

U761 and U861 are used to route the program signal (or auxiliary signal in AUXILIARY mode) to the Output Amplifiers, except when VITS is inserted during the vertical interval. During VITS time, the switches route internally generated signals to the Output Amplifiers as programmed VITS.

Basically, the circuitry acts like two double-pole double-throw switches. In one position, signals applied to pins 2 and 15 reach the differential output, pins 12 and 13. In the other position, signals at pins 7 and 10 reach the output. Switching between the two channels of each switch is dependent upon the condition of pin 4. Signals reaching the output of each switch are also dependent upon the condition of pin 6 (if high, no output will be obtained). Thus, the incoming program signal (or auxiliary) is applied to one channel, the internal signal to the other; dependent upon Program Control Switch settings, a combined output is obtained.

VITS Switch Control

As discussed above, VITS switching is dependent upon the condition of U761 pin 4 and U861 pin 4. The VITS Switch Control stage is used to steer a control signal to pin 4 of each switch so that insertion may occur. Q560, Q570, and Q658 are the active elements of this stage.

For the discussion that follows, assume that the PREVIEW mode of operation is selected, and that VITS is internally programmed to appear during the vertical interval. Under these conditions, the signal at the PROGRAM OUTPUT LINE and MONITORING OUTPUT is the same signal applied to the PROGRAM INPUT; the signal at the PREVIEW OUTPUTS is the PROGRAM INPUT signal, plus the internally generated and inserted VITS. For these conditions to exist, pin 4 of U761 (program switch) must be held low at all times to inhibit insertion in the program channel. That is, in the preview mode of operation the VITS key signal should be steered into the preview switch and away from the program switch. In addition, pin 4 of U861 (preview switch) must be held low, except during VITS time.

S9212 places a ground on P591-6. CR585 and CR588 are forward biased, shutting off Q560 and Q658. With Q560 and Q570 off, pin 4 of each VITS gate is low and only the program signal appears at the respective outputs. During VITS time, a VITS key pulse (via P591-3) reverse biases CR588 to switch current through Q570. Pin 4 of U861 goes high, allowing the VITS (via pin 7 of U861) signal to be routed to the PREVIEW OUTPUTS.

In the PROGRAM mode, it is desired to steer the VITS key signal to both the program switch and the preview switch. In this mode, the ground is removed from P591-6. Q560 therefore is able to conduct, but its collector does not go positive because Q658 is biased on during the low state of the VITS key signal. When the VITS key signal goes positive and cuts off CR588, current flows through Q570. This places a high state voltage on pin 4 of U861 (the preview switch) and through CR664 to the base of Q658, which acts as an emitter follower to deliver the high state voltage to pin 4 of U761. Therefore, both the program switch and the preview switch are furnished with the VITS key signal, and Insertion Test Signals will be seen at the PROGRAM OUTPUT LINE and the PREVIEW OUTPUTS.

Should interruption of the program signal occur, a detector elsewhere in the instrument senses the absence of an incoming signal and at that time develops a high state voltage, which is delivered to P501-2 by way of CR651. This signal cuts off Q658, thus allowing the current through Q650 to hold a high state voltage on pin 4 of U761. This steers the internally generated full field test signal into U761; whichever full field test signal has been selected on the front panel will then appear at the program output. The link from the program loss sensing circuit to P501-2 passes through the remote plug on the rear of the instrument. If this feature is not desired, the connecting jumper may be removed.

Output Amplifiers

The outputs of both U761 and U861 are push-pull signals. Each output amplifier consists of a differential pair followed by a feedback operational amplifier. The differential pair converts the push-pull signal from the program or preview switch to a current. This current drives the input summing junction of the operational amplifier. R868 and R978 (Rf for the two amplifiers) set the gain of each stage. These operational amplifiers provide the low impedance necessary to drive the PROGRAM OUTPUT LINE, MONITORING OUTPUT, and PREVIEW OUTPUTS.

Preview Indicator

Q565, an emitter follower, provides drive for the PROGRAM and PREVIEW lamps.

DIAGRAM ① a and ① b

The Vertical and Horizontal Counter circuitry synchronizes the 148-M to the incoming program composite sync (or black burst), and generates all timing signals required for operation of the 148-M.

Horizontal Integrator, AFC Sampler, 1 MHz Oscillator, Divide-By-64 Counter, and Delayed Feedback

A 1 MHz oscillator generates a pulse that is counted down to the line rate. The line-rate gate is then compared to the external composite sync. Any timing error between these two signals will produce an error voltage to change the oscillator frequency. This action keeps the ÷64 counter in step with the external sync.

1 MHz Oscillator. Q1691 and Q1791 are the active components for the 1 MHz oscillator. CR1740 and L1670 are the frequency-determining components. Sustaining feedback is provided via C1798 and C1995. The output of the oscillator at TP1480 consists of positive-going pulses (limited sinewaves), which are then used to toggle the Divide-by-64 Counters.

Divide-by-64 Counter. U1391 and U1361 are synchronous counters, connected for a divide-by-2, divide-by-4,..., divide-by-64 sequence. 1 MHz to the C_P inputs provides outputs at 32H, 16H, 8H, 4H, 2H, and H rates.

Delayed Feedback. U1461C combines three of the Divide-by-64 Counter outputs to produce a negative gate, approximately 8 μs wide, each horizontal line. During the 8 μs negative interval, this pulse disconnects CR1795 and turns off Q1991, which allows C1780 to charge towards +15 volts (from 0 volts) at an approximate rate of 0.5 V/μs. (Charge path via R1893 and R1760.)

The ramp voltage across C1780 is then compared against the setting of R9209 (INSERT DELAY) and R1988 (Sync Delay) by voltage comparator Q1731 and Q1741. When the ramp voltage exceeds the delay voltage, Q1731 is turned off and a ringing pulse is developed across L1850. This pulse is then peak-detected by CR1930 to drive the AFC Sampler.

AFC Sampler. Q1921 and Q1721 form the AFC Sampler. When Q1921 is turned on, Q1721 acts as a gate that allows the voltage obtained by the ramp in the Horizontal Integrator to be transferred to the variable capacitance diode CR1740, which controls the 1 MHz Oscillator.

Horizontal Integrator. During sync time, this stage produces a ramp that is sampled to control the 1 MHz Oscillator. Composite sync is coupled to switching pair Q1801-Q1811. This switch, during sync time, allows current determined by R1820 to charge C1902 via Q1811 and R1903. This produces a positive (approximately 3 V/μs) ramp, made linear by Q1911. At approximately 4.7 volts positive, Q1901 is saturated to clamp the ramp, preventing breakdown of Q1721 in the AFC Sampler circuit.

At the end of sync time, Q1801 is turned on, and current via R1810 causes the ramp at the emitter of Q1721 to go in a negative direction towards 0 volts at an approximate rate of 2.5 V/μs, made linear by Q1911. Ramp voltage at sample time is transferred via the AFC Sampler stage to the 1 MHz Oscillator, which brings the ÷64 Counter into step with the external sync.

VITS H Blanking

U1331B and U1461A combine the various timing signals from the Divide-by-64 Counter so that U1301A provides the required horizontal blanking that is used to gate (switch) the VIT Signals into the program signal during VITS time.

Vertical Integrator

The vertical integrator produces a ramp during the vertical serration pulses, which is then peak-detected and used to set the Field Counter and Field Recognition circuits. This integrator is similar to the horizontal integrator except for circuit values.

Peak Detector

On the last vertical serration pulse, Q1411 is biased on, producing one negative vertical reset pulse per field to drive the Field Counter and Field Recognition circuit.

Field Recognition

U1301B has square-wave outputs that are used for selecting VITS fields. The clock input, pin 11, receives a six and one-half line wide, field-rate pulse from the divide-by-525 counter. The data (D) input, pin 12, gets an inverted 8 μs wide, line-rate pulse from the divide-by-64 counter. If the data input is high when the clock pulse goes high, pin 9 will go high. This condition occurs at the start of fields 1 & 3. At the start of fields 2 & 4, the data input is low when the clock pulse goes high, so pin 9 switches low. See Fig. 3-2 for timing diagrams.

Clock

This stage (U1461B) is driven by pulses corresponding to instants 15 and 31 (see Operating Instructions or diagram 2_a for details). The pulses are used to toggle the Divide-By-525 Counter.

Divide-By-525 Counter

The counter generates the various timing gates required for one-half line offset used in interlace scanning. The counter is initially set to a count of 499 by a pulse obtained in the Vertical Integrator. It is then toggled from the Clock stage, counting to 1024 in a divide-by-2, divide-by-4,...., divide-by-1024 sequence. On the 1024 count, the counter is reset to a count of 499 and the sequence is repeated. (1024 − 499 = 525.)

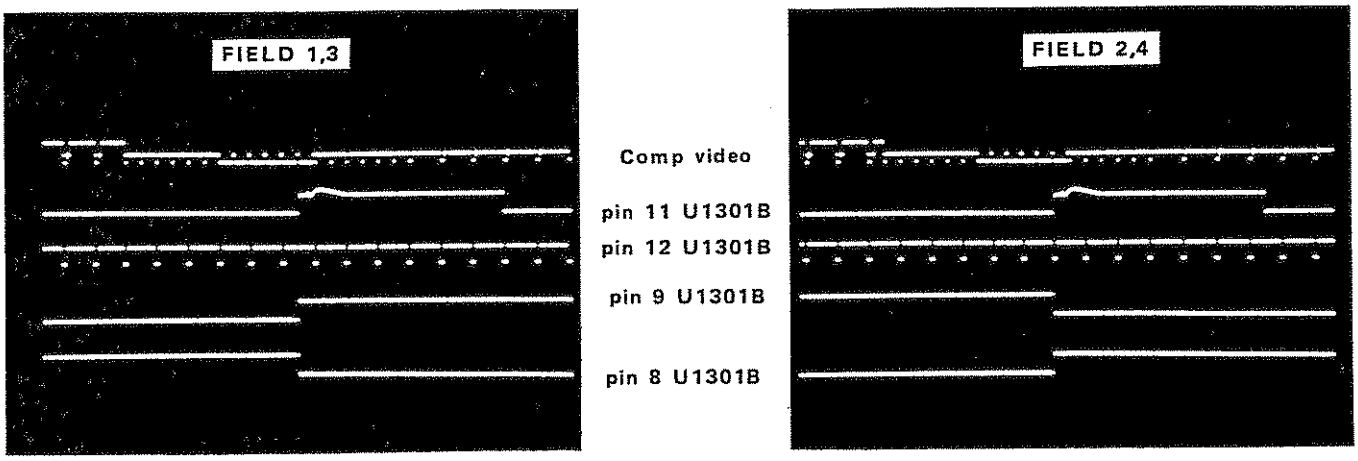


Fig. 3-2. Field Recognition timing waveforms.

Encoder Matrix

The encoder matrix produces timing-gate pulses from the divide-by-525 counter signals. A typical circuit consists of a pair of gates a set-reset flip-flop. For example: The 9 Line Keyout signal is generated by U1031, U1331A, and U1201A & D. This signal is used to change sync timing during vertical sync time. The signal duration is from the start of line 523 until the end of line 6, and from the middle of line 260 to the middle of line 269. U1201A & D, a set-reset flip-flop, will change state when the first low is received at the set input. It won't change state again until a low is received at the reset input. U1031 provides the set enable when all of its inputs are first high. This happens at the start of line 523 and at the middle of line 260. U1331A provides the reset enable when all of its inputs are first high. This occurs at the end of line 6, and at the middle of line 269.

Other signals generated by the encoder matrix are produced in the same way as the 9 Line Keyout. The Vertical Blanking signal duration is from the start of line 523 until the end of line 18, and from the middle of line 260 until the middle of line 281. The Field Sq. Wave signal occurs from the start of line 74 until the end of line 206, and from the start of line 337 until the end of line 469. This is a 60 Hz squarewave with about 50% duty cycle. The Pulse & Bar signal, Bar Enable, occurs between the start of line 63 and the end of line 216, and from the start of line 326 until the end of line 478.

DIAGRAM ② a and ② b

The Horizontal Timing circuitry combines the various signals generated by the Vertical and Horizontal Counters into timing pulses required to generate all test signals.

Instant Decoder

U2001 and U2401 are used to decode the various outputs from the Divide-By-64 Counter. Decoding provides 32 outputs (characteristic instants) about 2 μs apart,

$$\frac{63.56\ \mu s}{32} = 1.98625\ \mu s$$

each having a 1 μs negative-going pulse once each line.

Set-Reset Circuits

There are twenty-three set-reset circuits available on the Horizontal Timing board. The event associated with any given set-reset circuit is labled on Diagram 2_a and 2_b directly above the row of connectors that carry the input signals to the set-reset circuits.

Each set-reset circuit is programmed in the instant decoder matrix. The characteristic instant associated with the command, e.g. set or reset, is indicated above the input signal line. The times indicated are factory programmed.

Multiburst Width

This stage enables the Multiburst generator. U2741 senses low inputs to the various burst R-S flip-flops and triggers the monostable multivibrator U2811A. Pins 3 and 4 of U2811A are negative-edge sensitive when pin 5 is enabled by a high from Diagram 4. U2931C provides negative triggers during every horizontal line, but a high enable from Diagram 4 occurs only on the line and field that are programmed on the VITS line and field matrix. C2730, R2715, and R2720 are the timing components for U2811A. The low output pulse at U2811A and pin 1 is inverted by U2911B, a low input OR gate.

LINEARITY Staircase Logic

The full line linearity signal can be either a 10 step or a 5 step staircase or a ramp. The timing information for this signal is developed from the characteristic instant matrix and delivered to the inputs of OR gates U2831 and U2961C. Each characteristic instant corresponds to a riser on the 10 step staircase. The timing information for the 5 Step staircase signal is derived from the 10 Step timing information through the use of a divide-by-2 counter located on the Staircase circuit board.

1/2 Instant Delay

This stage, consisting of U2931E and U2961D, is used to delay characteristic instants 1 μs. (Factory connected for use with the CCIR-I and SIG-III signals.)

U2931E and U2961D invert negative-going (or low level) pulses from the Instant Decoder. The inverted (positive-going or high level) pulses are differentiated by C2936 or C2958. The negative-going portion of the inverted pulse is thus delayed 1 μs from the negative-going edge of the characteristic instant.

Modulation Logic

This stage provides a pulse that enables modulation to be inserted on the LINEARITY test signal or CCIR-I signal. U2981A generates a low enable output when pin 3 senses a high LINEARITY enable and pin 2 senses a high from the LIN MOD R-S flip-flop.

U2981B generates a low enable output when pin 6 senses a high CCIR-I/SIG-III enable from U2931D and pin 5 senses a high from the CCIR-I MOD R-S flip-flop.

Staircase Logic

This stage provides the timing necessary for the staircase portion of the CCIR-I SIGNAL or the SIG-III SIGNAL.

U2981C generates a low enable output when pin 9 senses a high CCIR-I/SIG-III enable and pin 8 senses a high from the CCIR-I/SIG-III LIN R-S flip-flop.

CCIR-I/SIG-III Five Step Timing

OR gate U2861 senses 5 characteristic instant inputs. Each of these instants corresponds to the time of a riser in the staircase signal used on both the CCIR-I and SIG-III test signals.

Pulse Timing

This circuit provides pulse timing for the T and 2T pulses used on the CCIR-I and SIG-III test signals and the PULSE & BAR full field test signal.

U2721 is 8an AND/OR gate. Pin 8 goes high when pin 9 or 10 and pin 13 or 1 are low. Pin 10 is low for CCIR-I or SIG-III, and pin 1 is low for PULSE & BAR. Pins 9 and 13 sense lows at characteristic times 11 and 17.

U2931F inverts the output from U2721 pin 8 to provide a low output.

Mod Pulse Timing

This stage provides the timing pulses required for the modulated sine-squared pulse. U2721 provides a high enable output to Diagram 9_b at pin 6. Operation of the AND/OR invert gate is similar to the pulse timing circuit.

Bar Timing

This stage provides the switching pulse for the bar, either T or 2T.

U2911A generates a low enable output on pin 1 when pins 2 and 3 are both high. Pin 2 senses a high from the P & B Bar Timing set-reset multivibrator on Diagram 2_a. Pin 3 senses a high for PULSE & BAR full field signal, or for PULSE & BAR/VIT Signal.

U2911C generates a low enable output for CCIR-I/SIG-III insertion test signal. Pin 8 is high for CCIR-I/SIG-III, and pin 9 senses a high from the CCIR-I/SIG-III BAR R-S flip-flop.

DIAGRAM 3a and 3b

The circuitry on Diagram 3_a and 3_b is used to generate and amplify the NOISE test signal and to generate the LINEARITY and FLAT FIELD test signals.

Noise Generator

This stage uses the thermal characteristics of two resistors (R3285 and R3383) to generate the noise.

The generated noise amplitude (approximately 60 μV) may be computed using the formula: $e = \sqrt{4kTR\Delta f}$, where k = Boltzmann Constant, T = 300° K, R = parallel combination of R3285-R3383, and Δf = 5 MHz.

Noise Preamp

Q3360-Q3370 and Q3240-Q3250 are operational amplifiers, each having a gain of approximately 30, as determined by the ratio of R3271 to R3371, and R3341 to R3343, respectively. This provides approximately 70 mV of noise at the collector of Q3240. C3251 and R3270 affect the low frequency cutoff so that the noise spectrum is flat (within the tolerance listed in Section 1).

Noise Amplifier

This stage provides front-panel (NOISE LEVEL dB) dc control of the noise signal.

The 1 dB switch (S9240, located on the front panel) controls the current through the emitters of U3100A and B, which are connected as diodes. The impedance between pin 6 of U3100C and pin 9 of U3100D is set by this current. E.g., increased current reduces the impedance, and less signal is allowed to pass through the noise amplifier.

10 dB switch (S9235) provides a forward bias source for Q3040, Q3050, Q3060, and Q3070. Turning on one of these transistors grounds its collector. As these transistors are connected to a resistor string composed of R3141, R3163, R3171, and R3183, they set the impedance to ground at the base of Q3130. The amplitude of the signal seen by Q3130 is controlled by this impedance. Q3130 and Q3110 are emitter followers to provide low impedance outputs.

Field Square-Wave

This stage ensures that the Field Sq. Wave signal begins and ends at the beginning and end of horizontal lines in all 4 fields. The Field Sq. Wave signal input to this circuit comes from the matrix circuit on Diagram 1_b and is offset 1/2 line in fields 1 and 3.

U3585A is an edge-triggered D flip-flop. The data input (pin 2) is programmed by a high during lines 74 through 206 and 337 through 469, and a low during the remaining lines. Pin 3 is triggered by the positive portion of the H blanking signal from Diagram 8. The set and clear inputs are inhibited by +5 V through R3491. The output on pin 5 is the FIELD SQ. WAVE timing signal to the APL circuit.

Pulse & Bar

This circuit is similar to the Field Square-Wave, except that it's output is the PULSE & BAR/BAR ENABLE to Diagram 4, VITS and FF LOGIC. The data input of U3585B, (pin 12) is programmed by a signal high during lines 63 through 215, and 326 through 478.

Bounce Generator

This circuitry consists of a modified Bowes Oscillator (Q3890 and Q3880), which is front-panel controlled (RATE). This allows the oscillator period to be changed from ≈1 to greater than 10 seconds. The output of the bounce oscillator is used to control the data input of flip-flop U3855B. This flip-flop is clocked by horizontal blanking, so that the bounce transitions will take place coincident with the start of a line. The outputs of this flip-flop are used to control NAND gates U3835D and U3735C.

APL

This stage consists of four current switches that set the level of the FLAT FIELD or FIELD SQ WAVE test signal. U3735D produces a low output when FLAT FIELD ENABLE and H BLANKING (pins 12 and 13) are both high, disconnecting CR3921, CR3821, and CR3723. This permits current from Q3825, Q3820, or Q3720 to flow through CR3911, CR3811, or CR3711, and through R3814 to circuits shown on Diagram 7_a. Q3825 sets BLACK current when the output from U3835D is low, disconnecting CR3823. Q3820 sets WHITE current when the output from U3735C is low, disconnecting CR3725. Q3720 sets VAR current when S9275 is in the VAR APL position, disconnecting CR3721. A high output from U3735D shunts current from these transistors and disconnects CR3911, CR3811, and CR3711, disabling FLAT FIELD signals. Q3920 sets FIELD SQ WAVE current when pin 1 of P3801 is low, pin 8 of P3800 is low, and the output of U3835C is low. S9290 (% PEAK WHITE) selects the current setting resistors for FIELD SQ WAVE.

Linearity Modulation Amplitude

This stage is a programmable current switch (Q3420 and CR3411) that provides sufficient current to the modulator for either 140 mV or 100 mV subcarrier modulation on the LINEARITY test signal.

Control Logic

This stage combines timing and gate signals for the control of staircase and ramp generation for the LINEARITY and CCIR-I/SIG-III signals.

U3735A produces a low output on pin 3 to enable the integrator circuit when pins 1 and 2 are both high. U3735B produces a high output on pin 6 when either pin 5 is low for CCIR-I/SIG-III staircase or pin 4 is low for LINEARITY.

U3775A produces a negative-going pulse on pin 3 when pin 2 is high and pin 1 is pulsed high. U3755C inverts the low pulses from U3875C.

U3875C produces negative-going pulses when pin 8 or pin 9 senses positive pulses from circuits shown on Diagram 2_b. U3875B produces a high output on pin 4 when pin 5 of U3875B is low and S9253 is in the 10 STEP position, grounding pin 6.

U3775A produces positive-going pulses for either 5 STEP LINEARITY or CCIR-I/SIG-III signals. U3855A divides 10 STEP timing by 2 for 5 STEP LINEARITY. U3875A pin 1 is high to enable U3855A when pin 2 and 3 are both low.

U3835A produces a low on pin 3 for RAMP when pins 2 and 1 are both high. U3875D is high on pin 13 when pins 11 and 12 are both low (S9253 grounds pin 11 in RAMP position).

Integrator

This stage consists of a Miller Integrator and a reset circuit; it generates ramp and staircase waveforms.

The Integrator consists of Q3440, Q3430, and Q3530. C3441 and C3443 provide the feedback for integration.

The reset circuit consists of Q3520, Q3510, Q3600, Q3540, CR3531, and CR3533. When U3735A produces a low on pin 3, CR3533 conducts and disconnects CR3531. Q3520 increases conduction and shuts off Q3540. The integrator can now accept drive from either the 10 Step, 5 Step, or Ramp drive sources.

When Ramp is selected, a constant current is drawn from the Integrator input (gate of Q3440). As the gate of Q3440 is drawn positive, the source follows. Q3430 inverts and amplifies, initiating a negative ramp. Q3530 couples this negative excursion to feedback capacitors C3443 and C3441, and also provides a low impedance output.

When U3735A pin 3 goes positive, Q3520 shuts off, and Q3510 conducts, turning on Q3540. Q3540 conducts through CR3531, resetting the Integrator and disconnecting CR3533.

Q3600 clamps the base of Q3540 at +0.5 V. Feedback from the Integrator output to the emitter of Q3540 maintains the quiescent 0 V output level.

10 Step Drive

Each time U3775A pin 3 pulses low, Q3470 conducts and discharges C3470 and C3461 through Q3450. The current demanded by Q3450 drives the Integrator. For each pulse, a negative step is generated by the Integrator.

5 Step Drive

This circuit is similar to the 10 Step Drive circuit, except that C3565 and C3473 have a parallel capacitance twice that of C3470 and C3461, so that the 5 Step staircase is the same amplitude as the 10 Step staircase.

Ramp Drive

This circuit demands a dc current from the Integrator for Ramp generation. When U3835A pin 3 goes low, U3755D pin 8 goes high, disconnecting CR3651. R3616 and R3621 set the dc current demanded by Q3645 from the integrator, setting a linear ramp rate.

DIAGRAM ④

The circuits on Diagram 4 determine which lines will contain the test signals. Test signals may appear on all active lines, inwhich case it is referred to as a full field test signal; or they may occur on selected lines during the vertical blanking interval, in which case they are referred to as Vertical Interval Test Signals. The outputs from the circuitry on Diagram 4 are enabling signals directed to the individual test signal generating circuits.

Line Counter

The line counter establishes gating signals corresponding to each of the available VITS lines.

U4151 is a 4-bit binary counter. The trigger input is a characteristic instant pulse corresponding to time 0 and occurs once every line.

U4351 converts this binary code to decimal output. Both the G1 and G2 inputs must be low for U4351 to operate. The G2 input is connected directly to the vertical blanking signal, so that the decoded VITS line pulses will be present only during the vertical blanking interval. The G1 input is enabled by the VITS Nonsynchronous Inhibit circuit.

VITS Nonsynchronous Inhibit

This circuit prevents any VITS from being inserted into the vertical interval, should loss of vertical sync occur.

U4831B and C form a R-S flip-flop which, when set, produces a high output on pins 6 and 9 and a low output on pins 5 and 8. The high output enables the VITS Key circuit and the low output enables the G1 of U4351. When reset, these outputs are inverted (low on pins 6 and 9, high on pins 5 and 8), inhibiting the VITS Key and U4351.

Vertical blanking is capacitively coupled into the reset input (pin 10) through C4387 to inhibit the VITS line decoder at the start of every vertical blanking interval. A negative pulse from the Vertical Integrator shown on Diagram 1 sets the flip-flop when incoming vertical sync has been processed for the counters.

A LOW FOR NON SYNC from a circuit on Diagram 9_a appears at U4381C pin 10 when any incoming synchronizing signals are missing. This resets the flip-flop, and inhibits the Line Decoder and VITS Key.

VITS Line and Field Matrix

This stage selects lines and fields for insertion of the various VITS.

Each row of pin pairs corresponds to a particular test signal as labeled. Each column corresponds to a particular line. The 3 columns at the extreme right correspond to fields as labeled. Programming plugs placed on the matrix connect selected line and field information to AND gates U4621C, U4621D, U4621B, U4621A, U4641C, U4641D, and U4641A.

When one of the AND gates senses a low on both inputs (line on one, field on the other) the output goes high. The inverter makes this a low enable for the VITS Key and the VITS or Full Field circuit.

VITS Key

This circuit developes the SWITCH CONTROL signal for Diagram 0_b. A high output is present on pin 8 of U4581C when either pin 10 is low for AUX or pin 9 is low for insertion of test signals. A low output is generated by U4551D on pin 11 when U4551D pin 13 is high, U4551C pin 10 is high, and any input to U4821 is low.

Full Field Logic

This circuit provides for the front panel selection of full field test signals. The CCIR-I, SIG-III, CCIR-II, MOD PULSE & BAR, and LINEARITY test signal control methods are identical. For example, the control for the CCIR-I signal is as follows: U4881 pin 6 is high when pins 2 or 3, and pins 4 or 5 are low. Pins 3 and 4 are grounded (by FULL FIELD SIG switches S9260 and S9265) in the CCIR-I position. Pins 2 and 5 are switched high and low by the Alternate Switching Logic circuit on Diagram 9_b. U4851B generates a low enable output when pins 4 and 5 are both high.

The FIELD RATE SWEEP GEN test signal is controlled almost like those above, except the input to pin 10 of U4681 contains the logic for the field markers coming from the Field Rate Sweep Gen logic on Diagram 10.

U4741F and U4651B provide for BAR ENABLE and PULSE ENABLE signals for the full field signal, PULSE & BAR.

VITS or Full Field

This stage receives either low VITS timing pulses from the VITS Line and Field Matrix, or low full-field timing gates from the Full Field Logic circuit. Either input is inverted and passed on to the Control Logic circuit as a high.

Control Logic

This stage processes the enabling signals from the VITS or Full Field circuit and generates the required enabling signals for the test signal generators.

A low (enabling CCIR-I and SIG-III) appears on U4641B pin 4 when pin 5 or pin 6 is high. U4841C generates a high MOD INHIBIT on pin 8 when either pin 9 or pin 10 is low to shut off the Subcarrier Oscillator during the noise measurement mode. Pin 11 of U4841D produces a high MOD PULSE ϕ signal when either pin 12 or 13 is low. This high signal is then applied to the Subcarrier Phase Control circuit on Diagram 8 as an enable during modulated pulse time. U4741B inverts the high from U4651D for a low MOD PULSE & BAR ENABLE. PED and NOISE ENABLE is a low appearing on pin 6 of U4581B when pins 4 and 5 are high. U4841A produces a high BAR ENABLE when pin 1 is low or when pins 4 and 5 of U4841B are high. U4651A produces a high PULSE ENABLE when pin 1 is low or when pins 4 and 5 of U4651B are high.

Noise Logic

There are two modes of use for the 148-M noise measurement circuits. The first mode is deletion of any information on one full line of insertion test signal. This is useful where noise is to be measured at a downstream point, but incoming noise from upstream points is to be deleted. The second mode is the insertion of a meausred amount of noise on the center half of an insertion test line.

Deletion. When full line deletion is required, the desired line is programmed in the VITS Line and Field matrix. A positive-going pulse is then applied to pin 13 of U4581D, a high input and gate. S9225, the front panel NOISE switch, produces an open circuit at P4290-4, allowing U4581D pin 12 to go high through R4580. The resulting low at U4581D pin 11 causes a high at U4481B pin 6, which is then applied to U4481A pin 2. U4481A is a high input AND gate. U4481A pin 1 receives its required high when the vertical blanking signal is at a low state during the period. When U4481A pins 1 and 2 are both high, a low VITS Key is developed at pin 3.

Half Line Insertion. When a measured amount of noise is desired during the center portion of a particular insertion line, S9225 grounds pin 5 of U4281B. This inhibits the path just described and enables the path consisting of U4281B and U4481C. Pin 6 of U4281B must also be low which is the case when noise is called for as an insertion signal. The full field interval is unimportant in this mode since it is prevented from affecting the VITS key by the vertical blanking signal on pin 12 of U4481D. The output of U4281B is now seen to be a high applied to pin 9 of U4481C. Pin 10 of U4481C is high during the center portion of a scanning line, as determined by one of the set-reset circuits on Diagram 2_a. U4481C pin 8 will be low during the center portion of the desired VITS line. This ultimately generates a VITS Key of that same width. Other connections to S9225 ensure that noise is added in this second mode but not in the first, where deletion only is required.

Indicator Logic

This stage controls the operating mode indicator lamps on the front panel.

Two signal lines, labeled HIGH FOR AUX and LOW FOR PREVIEW control this circuit: When HIGH FOR AUX is high, Q4071 conducts, lighting the BYPASS indicator. When HIGH FOR AUX is low, U4281C is enabled. When LOW FOR PREVIEW goes low, U4281C generates a high on pin 10 and Q4091 will conduct, lighting the PREVIEW indicator. When LOW FOR PREVIEW is high, pin 10 of U4281C will be low, enabling U4281D. Q4081 conducts, lighting the PROGRAM indicator.

Auxiliary Logic

The auxiliary mode of operation requires that the VITS Key signal be essentially a composite blanking signal. The VITS switches shown on Diagram 0_b operate in such a fashion that the sync burst and blanking of the 148-M are added or mixed with the incoming auxiliary signal. U4831D combines vertical and horizontal blanking in order to produce a composite blanking signal applied to pin 1 of U4381A. Pin 2 of this gate is high when the front panel switch calls for the auxiliary mode. The desired VITS keying signal is therefore developed at pin 3 of U4381A.

DIAGRAM ⑤a

The Gen-Lock circuitry is used to provide reprocessed composite sync, and lock the internal 3.58 MHz oscillator to the incoming burst signal.

Sync Separator Circuit

The circuit removes sync from the externally applied composite video signal. Processing of the composite sync eliminates any degradation of the incoming composite sync, such as white noise, 60 Hz hum, etc.

Processing of composite sync is accomplished by clamping the sync tip level of the external composite video to a predetermined level, then adjusting the blanking level by controlling the overall circuit gain.

Fig. 3-3 is a block diagram of the Sync Separator circuit, and the description that follows is organized with respect to the block diagram and Diagram 5_a.

The sync tip of the external video signal (applied to the PROGRAM INPUT connector) is clamped at the sync tip level by the Sync Tip Comparator circuit, consisting of voltage comparator Q5371 and CR5480, operating as a current switch. The comparator is rate-limited and uses the dc-coupled sync to activate it. Once the comparator is switched, any tilt from the field or the line rate sync tips is eliminated. The rate limiting allows the feedback loop (through Q5481 and Q5287) to open at the trailing edge of the sync pulse, and makes the loop unresponsive to impulse noises. It also allows the Level Memory (C5288) to average the white noise on the sync tip during the time the loop is closed. This average determines the sync tip level.

The output from the Level Memory is applied to two filters. R5165 and C5063 form a high-pass filter that changes the gain of the summing amplifier from one (at very low frequencies) to a gain of three, above approximately 200 Hz. This variable gain feature allows fast recovery of the sync-tip level. In the feedback loop around Q5161 and Q5281 is a low-pass filter (C5186 and Q5171), that produces negative feedback to 60 Hz signals, effectively reducing 60 Hz hum.

The 50% Level Comparator (Q5271-CR5276) processes the sync at the 50% amplitude point between the sync tip level and the blanking level, ensuring correct sync width.

The Blanking Level Comparator (Q5261-CR5274) uses the difference in the duty factor between the sync pulse width and blanking width to determine the blanking level.

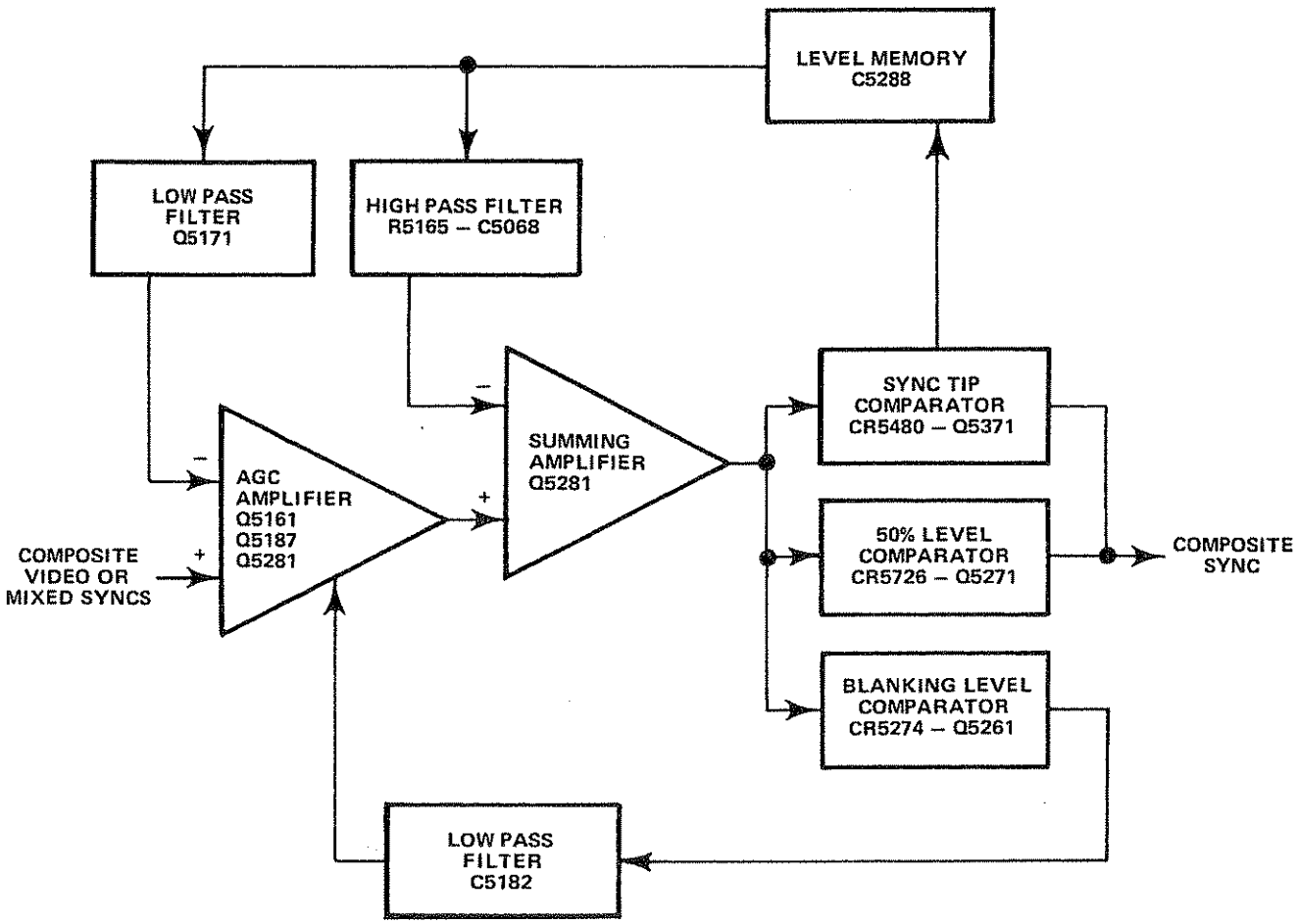


Fig. 3-3. Block diagram of the sync separator circuit.

This method allows the entire system to function because timing information is not required to close the AGC loop. The Low Pass Filter (C5182) averages the output of the Blanking Level Comparator; this voltage controls the overall system gain through Q5187. Q5181 and Q5091 provide quick-charge current for C5182.

Sound-In-Syncs Inhibit

This stage consisting of U5921A and B and U5967A, B, and C, is used to prevent sound-in-syncs from interfering with Gen-Lock. This is because the following circuit (Back Porch Generator) depends upon the trailing edge of sync; sound-in-syncs would cause the Back Porch Generator to operate during the sound-in-syncs pulse.

U5921A produces a pulse that has been delayed from the leading edge of sync. The pulse duration is longer than that of sound-in-syncs, but less than that of sync. This pulse ensures that the Back Porch Generator "sees" only the composite sync and not the sound-in-syncs.

Back Porch Gate Generator

The Gate Generator consists of Q5251 and Q5151. It provides gate pulses to the demodulators that correspond to the time of line sync and back porch, or the time of back porch only.

Negative-going composite sync pulses are applied to CR5258 via the Sync Separator circuit. CR5258 reverse-biases on the leading edge of the composite sync and C5257 charges towards −15 V through R5160. The charge path for C5257 is via Q5251 (normally on) and R5160. The trailing edge of the composite sync forward-biases CR5258, which couples a positive pulse through C5257 and turns Q5251 off, producing a series of negative-going pulses at the collector of Q5251. These pulses are coincident with the trailing edge of the line sync, the equalizing pulses, and the vertical sync pulses.

With P5150 in the BURST position (pins 1 and 2 connected), composite sync pulses via R5259 are added to the delayed pulses from Q5251 and drive Q5151. The

duration of each output (positive-going) pulse to the demodulators corresponds to the duration of the input line sync and back porch. With the BURST-CW jumper wire (P5150) in the CW position (pins 2 and 3), the output pulse duration to the demodulators corresponds to the time of back porch only.

Chroma Amplifier

The Chroma Amplifier consists of the Chroma Trap (C5055 and L5056) and three operational amplifiers in series with external AGC control.

Chroma Pickoff. The trap consists of a series resonant LC circuit (C5055 and L5056). The 3.58 MHz components of the signal, applied to the input, are separated from the external sync by the trap and applied to the Chroma Buffer Amplifier.

Chroma Buffer Amplifier. Q5051 and Q5041 are connected as an operational amplifier with low input impedance. The output (3.58 MHz subcarrier signal current) is regulated by the AGC circuit and applied to a second operational amplifier, Q5031-Q5021.

AGC Circuitry. The gain control circuit components include Q5141 and CR5040. This circuit regulates the subcarrier signal current (through CR5040 to the input of operational amplifier Q5031-Q5021) by shunting a portion of the signal current (at the junction of C5041 and C5043) through CR5040 to ground. The amount of current shunted through CR5040 depends on the current demand of Q5141. If the subcarrier signal current is excessive, an increased negative-going corrective signal from the AGC Comparator is applied to the base of Q5141. This increases the current through Q5141, which increases the current through CR5040. This decreases the impedance across the diode and shunts more of the signal current away from operational amplifier Q5031-Q5021, thereby decreasing signal input to the amplifier stage.

Limiting Amplifier. Q5031 and Q5021 are connected as a low input impedance operational amplifier with the feedback resistance (R5030) shunted by CR5010, CR5012, and C5034. This provides signal limiting to ensure that the subcarrier (due to peak signals) does not leak through the demodulator during non-demodulation time.

Output Amplifier. The output amplifier (Q5121-Q5231), an operational amplifier, ensures adequate drive current for the demodulators. L5100 is adjusted to compensate for subcarrier phase shift errors through the amplifiers.

DIAGRAM ⑤b

Quadrature Demodulators

The Quadrature Demodulator circuits produce output signals (which correspond to the amplitude and phase of burst, if any, from the externally applied composite video signal) to control the internal master oscillator.

Demodulator Driver. Q5511, Q5521, Q5421, and Q5431 are connected as differential comparators. Q5511 and Q5421 are turned on and off, at the subcarrier rate, during line sync and back porch time (or back porch only) to provide switching current to the demodulators. Q5521 and Q5431 are driven by the internally generated subcarrier signal, with Q5521 operating 90° later than Q5431. Subcarrier delay is provided by L5610, C5625, and C5620. R5616 terminates the line. Quadrature shift allows burst demodulation in any quadrant (demodulation may take place between 0 and 360 degrees). Q5511 and Q5421 are driven simultaneously by the Back Porch Generator.

Quad Demodulators. Demodulators Q5331 and Q5411 are forward biased by Q5511 and Q5421 during non-demodulation time. External chrominance from the Chroma AGC Amp is therefore shunted to ground through Q5331 and Q5411. During demodulation time (burst time of the external chrominance signal), Q5331 and Q5411 are switched by the demodulator enable switch at the subcarrier rate. The demodulated chrominance signal is then applied to low-pass filters L5340-C5344 and L5421-C5432. The output of the filters is therefore a dc level that represents the phase and amplitude of the external burst signal, plus the internal subcarrier signal. Under normal operating conditions, the output of Q5331 is an alternating positive and negative dc voltage level during burst time; the output of Q5411 is a negative dc voltage level during burst time. The output of each demodulator filter drives the AC Pulse Amplifiers.

Q5451-Q5457 and Q5441-Q5447 amplify the demodulated chrominance signal level obtained from the filters and drive memory capacitors C5545 and C5458.

Back Porch Clamps. Q5551 and Q5467 hold the inputs to the Quad Phase Burst Rectifiers and Buffer Amplifiers at 0 volts during non-demodulation time. This allows the memory capacitors to charge to a dc level dependent upon the phase and amplitude of the demodulated signal.

During back porch time, a signal applied from the Back Porch Gate Generator turns Q5467 and Q5551 off. This permits the charge on the memory capacitors to drive the Burst Rectifiers and Burst Clamp stages.

Burst Rectifiers. Q5461 and Q5651 are the active components of this stage, and are connected as phase inverters. This allows detection of the demodulated signal in any quadrant.

During back porch time, any charge on memory capacitors C5458 and C5545 drives Q5461 or Q5651 to produce a positive or negative (depending on phase) output. The more negative pulse is then coupled through one of the diodes CR5572, CR5576, CR5660, or CR5651 to drive the PAL Switcher stage.

Burst Lock Disable

Q5487 is the active component of this stage and is used to turn on the Burst Clamps except during Gen-Lock.

With the 148-M operated in the non-Gen Lock mode (no incoming sync), Q5487 is turned on by a signal from the Sync Present Detector (see Diagram 9). This turns the clamp transistors on, clamping the output of the Quad Demodulator stage at all times.

Burst Clamps

The V Burst Clamp and the U Burst Clamp stages are identical; only the V Burst Clamp will be explained.

Q5561, an emitter follower, passes the signal to clamp transistors Q5581 and Q5591. The clamp transistors are driven alternately from the PAL Switcher stage, hence the drive to Q5891, an emitter follower, is clamped in one direction and the drive to Q5591 is clamped in the opposite direction. The drive to Q5991, an emitter follower, is therefore an average of these two clamps.

PAL Switcher

Q5581 provides current, depending upon burst phase, to Q5597 and Q5691, a current switch. It is used to provide alternate switching to the clamp circuits.

PAL Preset

Q5997, an inverting amplifier, is used to control the Bruch Sequence (see discussion of Diagram 8).

DIAGRAM 5C

Subcarrier Oscillator and Frequency Control

The Subcarrier Oscillator and Frequency Control circuitry is used to switch the internal 3.58 MHz oscillator from a free run mode to a locked mode or vice-versa.

500 Hz Filter. R5784-C5680 and R5684-C5788 filter the signal pulses from the Quad Demodulators to provide a signal that corresponds to the amplitude and phase of the external burst.

Quad Phase Rectifier. To provide lockup independent of external burst phase errors versus internal subcarrier phase at the moment of Gen-Lock attempt, Q5871-Q5877 and Q5881-Q5887 are connected as paraphase amplifiers. The output of each amplifier is applied to a peak detector.

Peak Detector. The peak detector circuit consists of CR5874, CR5984, and CR5985. The most negative dc level from the Quad Phase Rectifier circuit is detected and applied to the DC Buffer Amplifier.

DC Buffer Amplifier. Emitter-follower Q5981 acts as a buffer and provides the necessary drive for the AGC Comparator and Burst Present Detector circuits. The output of the buffer is filtered by R5774 and C5866 to ensure an average dc level control voltage to the above circuits. The filter has an approximate bandpass of 5 Hz, which causes noise that appears at this point to be common mode to both sides of comparator Q5781-Q5671.

AGC Comparator. Q5781 and Q5671 are connected as a differential comparator with the base of Q5671 referenced to a fixed DC level. The AGC comparator is biased by the output level of Q5981 so that Q5671 is switched off, thus no AGC current is available to the AGC amplifier. With Gen-Lock, the output from the peak detector drives the AGC comparator so that an AGC current, corresponding to the amplitude of the externally applied burst signal, is developed through Q5671. This current is fed back to the Chroma AGC Amplifier and increases or decreases the overall chroma gain. Under normal Gen-Lock operation, burst amplitudes of approximately 71 mV to approximately 286 mV switch the comparator and produce an AGC output current.

Burst Present Detector. Q5987 and Q5971 are connected as a Schmitt Trigger circuit. If external burst is present, the output dc level from the buffer (Q5981) steps down and triggers the Schmitt circuit. The differential output of the Schmitt circuit drives the subcarrier reference switch.

Subcarrier Reference Switch. Q5921 and Q5941 form this circuit, which is controlled by the Burst Present Detector. When not Gen-Locked, both transistors are saturated. This provides a resistive divider consisting of R5910, R5920 (3.58 MHz adj.), and R5912 connected between −15 volts and ground (through both transistors). Control of the 148-M internal oscillator frequency depends on the setting of R5920. When Q5921 and Q5941

are reverse-biased by the output of the Burst Present Detector, the Subcarrier Reference Switch circuit "floats". Control of the internal master oscillator now depends on the Quad Demodulators output signals that are applied to Error Amplifier Q5937-Q5951.

Error Amplifier and Band Switch. This circuit controls the 148-M oscillator frequency during Gen-Lock mode of operation. Q5937 and Q5951 are connected as an integrating operational amplifier with C5956 as the feedback capacitor. Ri for this amplifier consists of R5762 or R5762 shunted by R5863 and transistor switch Q5861.

The rate of integration of the operational amplifier is changed by switching Band Switch transistor Q5861 on or off. The input resistance (Ri)is low when Q5861 is switched on. This increases the rate and amount that the amplifier output voltage shifts the internal master oscillator. With Q5861 turned off, the rate is relatively slow (Ri high) and the bandwidth shift of the oscillator is narrow, improving the noise immunity of the amplifier. Control of Q5861 is obtained from the Quad Lock Detector circuit.

Quad Lock Detector. The Quad Lock Detector circuit consists of a lock delay circuit (Q5961) and a Schmitt multivibrator circuit (Q5851-Q5857). The output of the multivibrator controls the Band Switch.

During initial Gen-Lock, Q5961 is forward-biased by a negative pulse applied via CR5952 from the Burst Present Detector circuit. This discharges C5950, which turns Q5857 on. The output of the detector (collector circuit of Q5851) is therefore a negative gate that switches Q5861 on. When lock occurs, Q5961 is turned off by the quadrature signal from the Demodulator circuit, allowing C5950 to charge towards +15 volts. This delays triggering the Schmitt multivibrator to turn Q5861 off, which ensures lock has occurred.

Q5931 is part of the Reed Switch Drive Circuit as described with Diagram 9.

3.58 MHz Oscillator

The 3.58 MHz crystal controlled oscillator generates the subcarrier used by the 148-M. In the free-running mode, the frequency will be within 25 Hz of 3.57561149 MHz. In the locked mode, the frequency will be locked to the incoming program burst. The output is amplitude limited and applied to the Subcarrier Output Amplifier (see discussion of Diagram 9) for further processing.

DIAGRAMS ⑥a and ⑥b

The Function Generator generates the field sweep signal and the sinusoidal burst packets of the multiburst signal. The average level and the white reference level of the multiburst signal, the center level of the field sweep signal, and the noise pedestal are also generated on this circuit board.

M. B. Enable

When a multiburst signal is to be generated, Q6103 receives a high state signal from the logic control circuitry on Diagram 4. This causes all of the diodes driven by the cathode of CR6017 to become reverse-biased. This now allows any of the transistors in the column headed by Q6106 to conduct, providing the remaining diode in the emitter circuit is also reverse-biased.

Multivibrator Rate Control

This stage sets the rate of charge and discharge current for the integrator within the Triangle Generator circuit.

The emitter circuits of Q6266 and Q6164 are such that, for any given base voltage, Q6164 demands twice the current as Q6266. This base level is set by emitter follower Q6262. Q6106, Q6212, Q6222, Q6228, Q6233, Q6244, and Q6149 set the current through R6144. Each sets a specific base voltage for Q6266 and Q6164.

Refer to Q6106. When the anode of CR6013 is low, enabling multiburst, and CR6113 receives a low from Diagram 2_a, R6117 and R6304 set the current through Q6106 and R6144. The resulting voltage drop across R6144 sets the base voltage on Q6262.

Q6149 works like the other rate control transistors, except the input to the emitter is a complex signal made up of the control and marker logic developed by the circuits on Diagram 4, and the ramp generated on Diagram 10.

Current Switch

This stage provides charging and discharging current for the integrator within the triangle generator. The Current Switch circuit is controlled by the Triangle Level Detector.

Current demanded by Q6266 is provided by U6170B. U6170A and U6170C form a constant current generator providing the same current flow as in U6170B.

Q6162-Q6068 is a current switch providing current for Q6164. When Q6068 is conducting, pin 1 of U6170 drives the Triangle Generator. When Q6068 is cut off, Q6162 turns on, connecting Q6164 to U6170 pin 1. Because Q6164 requires twice the current available from U6170A and C, an equal amount of current is drawn from the Triangle Generator.

Triangle Generator

This stage is basically an integrator, providing linear positive and negative ramps. The charging and discharging currents driving the integrator determine the ramp rate.

The triangle generator consists of Q6398 and Q6494-Q6482. The latter transistor is normally held in a clamped or conducting condition when no signal is desired from the triangle generator. When it is desired to generate a triangular signal, CR6376 is reverse-biased and Q6482 is cut off. At this time, the frequency determining current described above is allowed to flow in integrating amplifier Q6398-Q6494. The remaining transistors in this section of the circuit form an emitter follower; the voltage at the emitter of Q6593 is essentially the same as that on the collector of Q6494.

When current flows from the Current Switch to the integrator, the base of Q6398 moves negative. The emitter follows, driving the base of Q6494 down negative. Inversion and amplification take place within Q6494. Negative feedback for a linear positive ramp is provided by C6382.

At +5 V ramp amplitude, the Triangle Level Detector switches the Current Switch. When current is drawn from the integrator, the base of Q6398 moves and a negative ramp is generated. The direction of input current will again be switched at −5 V ramp amplitude.

Ramp rate is determined by the magnitude of input current. As current in both directions is of the same magnitude, the ramp rates (positive and negative) are the same, resulting in symmetrical triangle waveforms of a particular frequency.

Triangle Level Detector

When the output of the Triangle Generator reaches +5 V, the voltage at the base of Q6786 turns it on, switching CR6182 to its low state. This turns off Q6068.

When the output of the Triangle Generator reaches −5 V, the voltage at the base of Q6877 reaches turn on bias, switching CR6182 to its high state. This turns on Q6068.

Stop Control

This stage controls the level at which the Triangle Generator stops; and inhibits the generator during non-multiburst time. To generate a burst packet for the multiburst signal, a positive-going pulse of the necessary width is applied the emitter of Q6198 from the Mod Pulse Timing circuit on Diagram 2. This signal in turn causes a positive-going voltage to appear across R6398, turning Q6298 on and Q6392 off. This allows CR6376 to reverse-bias; at that time the Triangle Generator starts to run. When the pulse at the emitter of Q6198 goes low and Q6198 cuts off, the voltage across R6398 does not immediately go back to its negative condition. It is held up by Q6095. Q6095 is driven from a switching pair, Q6091-Q6192, which is essentially in parallel with the switching pair that controls the current reversal in the Current Switch circuit. Q6095 will only allow the voltage across R6398 to go negative during the positive half cycle. This ensures that the burst packet will end only during the positive-going half cycle. The Stop Level circuit determines the burst packet ending point.

Stop Level

This stage sets the quiescent or 0 level of the Triangle Generator.

The voltage at the base of Q6569 is very nearly equal to the output voltage of the Triangle Generator, that is, the collector of Q6494. As the output rises during the positive-going half cycle, it eventually reaches a point where it is equal to the voltage selected by potentiometer R6673. At that point, Q6482 turns on and the Triangle Generator stops.

Diode Shaper

In this circuit 12 diodes (see Diagram 6_b) are used to shape the triangular waveform into a sinusoidal waveform. Each diode is biased at a particular voltage and is connected to the necessary series impedance to produce the desired change of slope of the triangular signal to produce a good approximation of a sinusoidal signal.

Amplifier

Q6653B, Q6758, and Q6852 form an operational amplifier that sets the amplitude of the multiburst. Q6653A and Q6858 provide temperature compensation.

R6942 matches the reference level of all Full Field Test Signals to the vertical blanking level.

R6741 (MB GAIN), in series with R6844, controls the gain of the amplifier. It is shunted by a bandpass limiting network, C6740 and R6736 (MB BANDPASS).

Multiburst Pedestal

Two transistors are used to determine the average level and the white reference level of the multiburst signal. Each of these transistors is held cut off by the high state of the M. B. Enable signal at the anodes of CR6913, CR6918, and CR6923. This signal goes to a low state whenever a multiburst is to be generated. At that time, the other diodes in the emitters of these transistors control the collector current. Q6813 determines the center or average level of the multiburst signal and is adjustable by R6833. The white reference level set by R6835 is switched on by Q6824. Q6803 sets quiescent current in the amplifier on Diagram 7. The circuitry around Q6828 is not used.

Noise Pedestal

This circuit supplies the current to set the pedestal level of the NOISE test signal. It is controlled by the front-panel NOISE and PEDESTAL switches.

The NOISE pedestal is enabled by a low input to the anode of CR6603, allowing Q6715 to conduct through CR6705. PEDESTAL current is set by S9230 and R9230 in the DELETION mode. R9225 modifies the PEDESTAL current when S9225 is in the INSERTION mode. This provides a VARIABLE PEDESTAL.

Field Sweep Pedestal

A low Field Sweep Enable turns off CR6703, allowing current from R6724 to flow through Q6803 and generate a pedestal for the FIELD RATE SWEEP GEN signal.

DIAGRAMS ⑦a and ⑦b

This board contains the two major output amplifiers for the instrument. One amplifier handles luminance signals; the other handles the chrominance, noise, and the burst packets of the multiburst signal. This board also contains the External VITS Amplifier and a clamp circuit, which ensures that the black level of inserted VITS matches that of the incoming program signal. The sine-squared pulse and bar generators, together with the sine-squared shaping filters, are also included on this board.

Pulse Generator

The T or 2T sine-squared pulse is generated by driving a sine-squared shaping filter with a very narrow pulse. When a 2T or T pulse is desired, a negative-going pulse is inverted in L7110 and applied to the base of Q7001. This turns on Q7001 and discharges C7212 through Q7221. The amplitude of this pulse is determined by the value of the voltage to which C7212 was charged prior to its discharge time. This in turn is determined by either R7138 (T pulse) or R7131 (2T pulse). The resulting pulse of current in the collector of Q7221 is applied to either the T or 2T filters.

Bar Generator

Negative-going bar width pulses allow emitter current to flow in Q7241, which is adjustable by R7143. The resulting current is applied to either the T or 2T filter. Selection of T or 2T risetimes or pulse widths for the bar and pulse is made by placing the jumpers on P7321 as described in the operating instructions. Q7531 biases Q7241 and provides thermal compensation.

Modulated Pulse Luminance Amplifier

The modulated sine-squared pulse is composed of the linear addition of a 12.5T luminance pulse and a 12.5T envelope chrominance pulse. The luminance portion of this signal is applied to pin 1 of P7193, passes through Q7630A and is delivered to the modulated pulse luminance filter.

Filters

The T and 2T sine-squared shaping filters are used to produce sine-squared transitions from the very fast Pulse or Bar Generator[1]. Several other inputs are also provided to the T and 2T filters. These include all the various pedestal signals associated with CCIR-II, noise, the FIELD RATE SWEEP GEN signal, and all the various flat field signals. The luminance portion of the staircase and full line linearity signals are also applied to the 2T filters. These various inputs appear on P7101 and pins 3 and 4 of P7001. The modulated pulse luminance filter is used to produce a delay equal in value to the delay of the modulator and its associated bandpass filter, so that both the chrominance portion of the modulated sine-squared pulse and the luminance get the same amount of delay. Thus, the resulting composite pulse exhibits no chrominance-to-luminance delay. Q7431 biases the drive transistors, Q7321 and Q7331.

Luminance Amplifier

The luminance amplifier consisting of Q7711, Q7811, Q7911, and Q7921, receives signals from the outputs of each of the three filters mentioned previously. The amplifier is an operational amplifier whose gain is set by R7735. Its output impedance is low enough to drive three 75 ohm loads. These are the front and rear full field test signal jacks and the termination provided by the External VITS Amplifier.

Chrominance Amplifier

This amplifier is very similar to the Luminance Amplifier; however, associated with its input circuitry are several auxiliary circuits. The chrominance enters this

[1]A Kastelein "A NEW SINE-SQUARED PULSE AND BAR-SHAPING NETWORK" IEEE Transactions of Broadcasting, Volume BC-16, Number 4, DEC. 1970 (pp 84-89).

amplifier at pin 2 of P7691 and may be adjusted in amplitude with R7661. The noise signal enters at pin 6 of P7691. The flow of noise is controlled by two noise gating transistors, Q7551 and Q7651. The level of the noise may be adjusted with R7561. Multiburst and Field Sweep enter at pin 1 of P7491. Signal current flows at all times through R7551 and R7553. This is sufficient to produce the 350 mV amplitude. When the amplitude is desired, Q7481 is cut off by the MULTIBURST AMPLITUDE switch on the front panel and signal current then flows through two parallel paths: R7551-R7553 and R7461-R7581. Both Q7481 and Q7571 are gated to inhibit the passage of the multiburst signal during the 9 Line Keyout pulse.

Ext VITS Amplifier

An external VIT Signal may be inserted on the program output of the 148-M. Such a test signal is applied to J9011 on the rear panel. This signal is amplified by Q7981, Q7971, and Q7961. The output of this amplifier is connected to the VIT Signal input of both the preview and program VIT Signal switches.

VITS Amp Clamp

Since the incoming program signal is clamped to ground, as described in Diagram 0, the internal VIT Signals are also clamped to ground so that, when they are inserted, the two black or ground levels match.

A sampling pulse is supplied to pin 1 of P7003 during the back porch portion of the internally generated test signals. Q7191 is turned on by this clamp pulse and the resulting sampled level is transferred to memory capacitor C7383. This voltage is amplified by high-gain operational amplifier U7291. This amplifier error signal is further amplified in the Ext VITS Amplifier and applied once again to the same point as originally sampled. This restores the back porch level of the VIT Signals to ground.

DIAGRAM 8

The circuitry on Diagram 8 is used to shape and phase signals to drive the modulator. Exceptions: Q8911 and CR8910 form a current switch that is used to set the amplitude of the regenerated composite sync for use with the full-field test signals.

Subcarrier Phase Control

For standard test signals, three discrete phases of subcarrier are needed. These are 135° and 225° for the phase alternating burst, and 180° for all test signals. A CW subcarrier signal is supplied to P8100-1. This signal is steered through one of three phase shift networks, depending upon which test signal component is desired. The two burst phases are determined by the phase shift networks in the emitters of Q8150 and Q8158. Each of these transistors is turned on during alternate horizontal blanking intervals by the four-diode and gate, which is supplied with horizontal blanking by way of P8100-3 and a pair of line alternation pulses from the Bruch Burst Blanking Circuit. The 135° test signal phase is determined by the phase shifter in the emitter of Q8158. The subcarrier signal is steered through this transistor during the active line time. The switching logic is contained in U8110C. The outputs from each of these phase shift channels are combined at the emitter of Q8261. In the collector of this transistor is a parallel resonant circuit containing a voltage-variable capacitor. The dc voltage applied to this element is governed by the INSERT SUBCARRIER PHASE control on the front panel and is required to trim the test signal phase to be properly referenced to the incoming program signal.

Subcarrier Amplifier

The Subcarrier Amplifier circuit ensures that the modulator is always driven with the same amplitude of subcarrier, and corrects for symmetry in the input signal so that the modulator is driven with a balanced waveform.

The limiter amplifier, Q8371, with diodes CR8385 and CR8384, amplifies and limits the peak-to-peak subcarrier amplitude to about 1.2 volts.

The limited (squared) subcarrier signal at the collector of Q8371 is coupled through R8378 and C8574 to a paraphase amplifier (Q8471 and Q8571), which drives the push-pull output stage (Q8579 and Q8679). C8472-R8552 and C8654-R8554 integrate the signal, changing the squared wave to a trapezoidal waveform. This signal is ac coupled through C8558 and C8652 to the bases of Q8579 and Q8679, providing a drive signal with a 50% duty factor.

The amplitude of the triangular signal at the bases of Q8579 and Q8679 drives them into saturation and cutoff, producing a subcarrier-rate square-wave signal across the primary windings of L8660.

Bruch Burst Blanking

The Bruch Burst Blanking circuitry generates an eleven-line wide meandering pulse, which ensures that the first and last bursts of each field will be of the same polarity according to Fig. 3-4. This improves the stability of color synchronization.

U8620A is triggered by VITS H Blanking, and receives a PAL Preset pulse at the Clear input. The output of U8620A is a PAL square-wave; which also controls the PAL Switcher on the Gen-Lock circuit board, and 135° and 225° phase circuits in the Subcarrier Phase Control

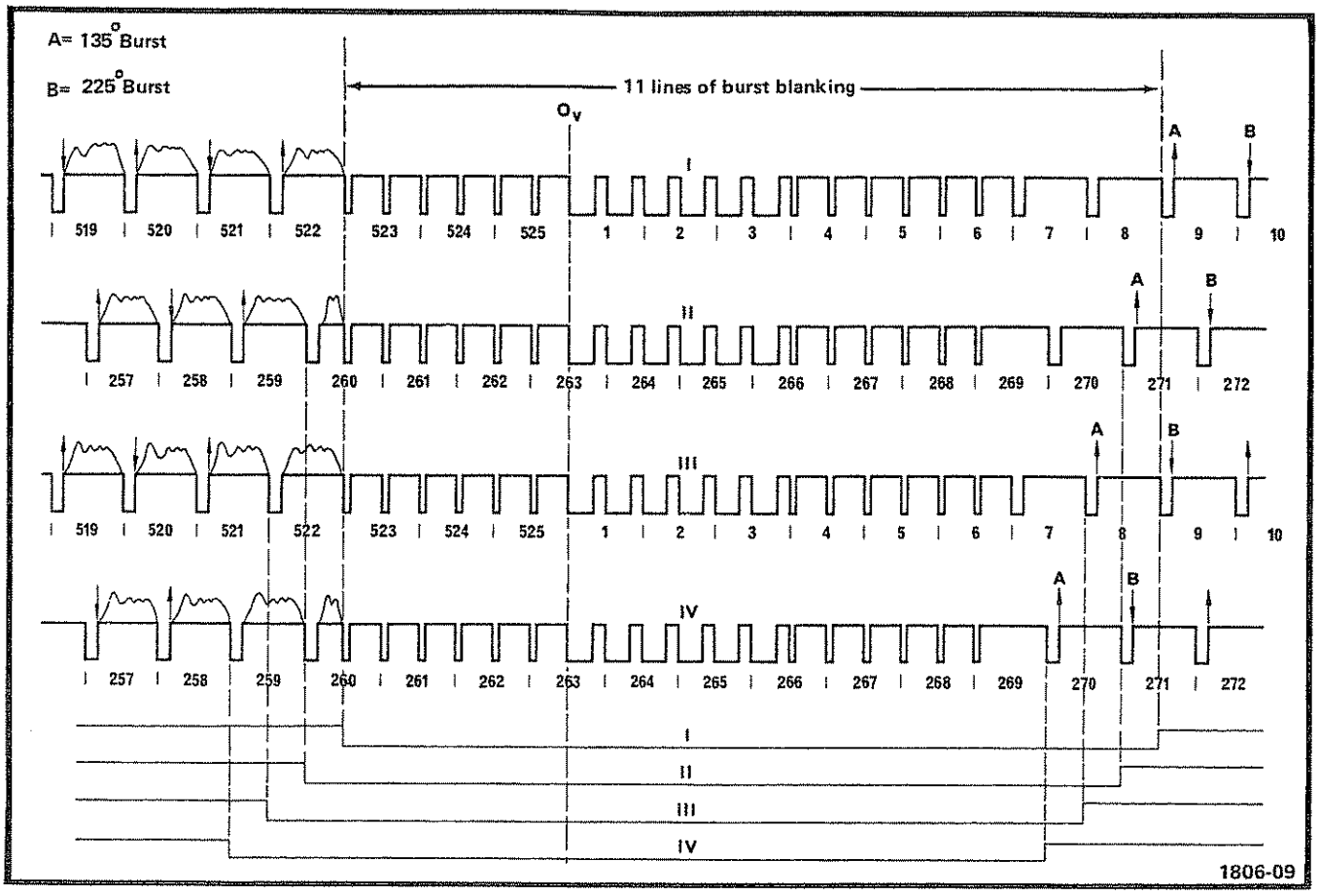


Fig. 3-4. PAL-M burst blanking sequence and field blanking interval. From *CCIR Conclusions of the Interim Meeting of Study Group 11.* Geneva, 1972 Part I, Recommendation 470 (Rev. '72), page 41.

section of the modulator. The complementary PAL square-waves drive the clock pulse inputs of U8720A and B. The Bruch Start signal is inverted by U8820A, then drives the D (data) input of U8720B and the Set input of U8720A. The Bruch Stop signal goes to the Set input of U8720B. The outputs of U8720A and B (field rate pulses with varying widths) are fed to the Set and Reset inputs of U8820B and C. The output of U8820B and C is the eleven-line wide "meandering" gate. This switches CR8536 on, turns Q8641 off, and shuts burst off during gate time.

CCIR-I and CCIR-II Chroma

These two stages consist of 5 current switches, which are used to set the amplitude of the chroma on the CCIR-I and CCIR-II signals for use in the modulator.

Each transistor is a current source whose current is set by the emitter resistance. The transistor conducts when both disconnect diodes in the emitter circuit receive low enabling signals. When either diode is high it shunts current away from the transistor. Q8281 controls CCIR-I chroma. Q8171, Q8172, and Q8279 control the CCIR-II chroma.

Modulator Drive

This stage provides the current required for modulation of the 3.57 MHz subcarrier for burst, modulated sine-squared pulse, modulated sine-squared bar, staircase, CCIR-I, CCIR-II, and SIG-III test signals.

The burst envelope filter consists of L8730 and associated capacitors. Current is steered through Q8641 to make a burst at such times as two conditions are present. One is the burst flag itself and the other is an enabling signal from the Bruch Burst Blanking Circuit. Burst amplitude is set by R8431. Current to produce the chrominance portion of all other test signals flows through the slower filter consisting of L8381 and associated capacitors. The modulated 12.5T pulse appears at P8960-2. A dc-balancing signal derived from the 12.5T sine-squared generation circuit appears at P8960-4. These last two signals are applied to the push-pull input of the modulator drive circuit, which is the base of Q8851A and B. The 12.5T chroma level is set by R8870.

Modulator

The modulator consists of double-balanced modulator U8890. The modulator has two pairs of terminals, one for

the subcarrier or switching signal (pins 7 and 8 of U8890) and the other pair for the modulating signal (pins 1 and 4). Two balance adjustments, R8990 and C8997, ensure that there is no subcarrier output when there is no signal input at the modulating terminals of the modulator.

Bandpass Filter

This stage consists of a pair of series resonant tanks, consisting of L8590, C8498, L8580, and C8488, tuned to 3.57561149 MHz. The placement of these tanks (one in each output lead) ensures symmetrical output; the component values limit sideband output.

Full Field Sync

Q8911 and CR8910 form a current switch for the composite sync current developed in R8938 and R8920. Comp sync from Diagram 9_a switches CR8910, allowing current to flow through Q8911 to the filter circuit on Diagram 7_a. U8820D and CR8924 are not used.

DIAGRAMS 9a and 9b

The circuitry contained on the Subcarrier and Sync board is used to provide current for the burst and composite sync amplifiers for use at the CW SUBCARRIER OUTPUT and COMP SYNC OUTPUT. In addition, sync lock detection, generation of the modulated sine-squared pulse, and the FULL FIELD SIG mode sequence are included.

Comp Sync Amplifier

CR8 and Q21 form a current switch. When CR8 is reverse biased, current through R7 is diverted through Q21, which drives the filter (L20, L120, C32, C28, and C46). The filter limits the risetime of the composite sync signal.

Q71, Q141, and Q151 are the active components of an operational amplifier. R42 is the feedback resistance; the input current is determined by R7. Q61 provides current for reverse-terminating any negative pulses that may appear at the output terminal due to unterminated coaxial cables.

Q381 provides drive to the VITS switch control (see Diagram 0_b) so that, in the event of PROGRAM INPUT interruption, internally generated Full Field signals will be switched to the PROGRAM LINE OUTPUT.

Subcarrier Amplifier

Emitter-follower Q81 serves as a buffer and driver. It isolates the oscillator (see Diagram 5_c) from the output. Because Q81 is biased near cutoff, it clips the negative portion of the input signal so that the drive signal to Q91 pulses the collector tank circuit (L190, C196, C194, and C198).

The output from the tank drives an operational amplifier consisting of Q181 and Q271. This circuit serves as a distribution amplifier to drive the various circuits within the 148-M, plus the CW SUBCARRIER OUT connector. Q171 sets the level at the emitter of Q181, and provides thermal compensation.

A relay, K370, opens the CW Subcarrier output line in the event burst is lost from the driving source. (See Operating Instructions for exception.)

Vert Sync, Horiz Sync, and Regen Sync Timing

These three sections of Diagram 9 are best treated as one. Regenerated sync should be contrasted with separated sync. The latter is stripped from the incoming program signal and therefore contains the identical timing information of that signal, including any jitter if present. The timing for regenerated sync is derived from the internal timing circuits of the 148-M, and is present even in the absence of an incoming signal.

The train of pulses that form the regenerated sync signal are formed in monostable multivibrator U301. There are basically two inputs to this multivibrator: One is a trigger or timing input, which determines the leading edge time location of each of its output pulses (Horiz Sync). The other input determines the width of the pulse (Vert Sync).

The standard composite sync signal requires that the trigger pulses appear at a line repetition rate during most of the active field, including most of the vertical blanking interval. However, during the 9 line interval that includes the equalizing pulses and the vertical sync pulse, the timing information rate must be doubled to twice line rate. Similarly, the width of the regenerated sync pulses must be of line sync width during the active portion of the field, including most of the vertical blanking interval, but must be appropriately narrowed for the equalizer pulses and widened to produce the serrated vertical pulse.

The pulse width of monostable multivibrator U301 is determined by three current paths into the pulse width timing capacitor C337. R356 and R336 provide current at all times and represent the minimum amount required for the production of the serrated vertical pulses. A second path, controlled by Q321, supplies additional current when normal line rate sync pulses are required. This transistor is driven by a 9 Line Keyout pulse, which stops flow of current during the 9 line interval around the vertical sync pulse.

The third current path is supplied with a complex signal that steers the largest amount of current into the monostable multivibrator during the first and last 8 lines of the vertical sync interval. During the middle 8 lines of this interval, the current is interrupted, leaving only the steady minimum value to produce the serrated pulses.

The logic to produce that control signal comes from the Vert Sync circuit. Two characteristic instant pulses drive U321A, producing a twice-line rate timing signal. This timing signal is applied to the trigger input of counter U201. This counter is connected to count by 6, producing an output after the sixth timing pulse at its input. The output pulse lasts for a period of six more twice-line rate pulses, and is combined by U101C with the 9 Line Keyout pulse to produce first a high, then a low, then a high state corresponding to each third of the 9 line interval. This output occurs only once per field (since the 9 line signal itself is used to reset the counter during active field time), and is inverted and applied to the base of Q331 to control the necessary current to produce equalizer and serrated pulses.

The timing pulses to trigger the monostable multivibrator are formed in the section of the diagram headed Horiz Sync. Again, the 9 Line Keyout pulse is required, since the timing during this interval is twice-line rate and outside this interval, at the line rate. U321D acts as an OR gate receiving a characteristic instant on pin 13, which produces line rate triggers. During the 9 Line Keyout interval, U321C permits the passage of a second characteristic instant into pin 12 of U321D. The output on pin 11 then contains twice-line rate triggers during the 9 line interval. Timing control and width control has therefore produced a standard train of composite sync pulses at the output of the monostable multivibrator on pin 6 of U301.

Burst Key

This circuit forms the burst flag pulse. The trailing edge of the horizontal sync pulse drives the base of Q421 negative to −5 V, cutting off Q421. Q421 remains cut off for approximately 1 μs while C415 charges back to 0.6 V. When Q421 turns on, a negative 5 V pulse is passed by Q406 to the base of Q428. Q428 cuts off for approximately 2.5 μs while C407 charges back to +0.6 V. The resulting positive pulse is inverted by Q408 and becomes a low enable to Diagram 8, delayed 1 μs from horizontal sync. In the event burst is lost from the driving source, R408 receives a low inhibit from Diagram 5_c and no burst key is generated.

Non Sync Inhibit

This stage compares incoming Stripped Sync with Regenerated Sync and inhibits the Line Counter and VITS Key circuits (see Diagram 4) if they are not in step.

The output of U101B is high when both inputs are low, and low when either input is high. Because Stripped Sync on pin 5 and Regenerated Sync on pin 6 are of opposite polarity, one input will be high at all times when they are in step. The resulting low output cuts off Q351. C374 charges positive, turning on Q391 which turns off Q394.

Should incoming sync and Regenerated Sync be out of step (or one not present), U101B senses coincident low states on pins 5 and 6. The resulting output turns Q351 on, discharging C374. Since charge time for C374 through R362 is considerably longer than discharge time through Q351, the bias to Q391 is held below conduction. The collector of Q391 is high, turning on Q394, generating a LOW FOR NON SYNC signal.

Due to the impedances of these charge and discharge paths, a full field is required to charge C374, and about 12 unsynchronized lines to discharge C374.

SIN^2 Pulse and Bar Generator

This stage is used to generate the luminance portion of the modulated sine-squared pulse and bar.

For the CCIR-I and SIG-III signals, Q498 (see Diagram 9_b) is turned on by a positive pulse from Diagram 2_b. The collector of Q498 goes negative, discharging C487 through Q466 into a 9-pole Kastelein filter. This pulse of current is shaped into the luminance pulse and is sent to the circuits shown on Diagrams 7_b and 8.

For the MOD PULSE & BAR signal, Q498 is turned on by a pulse from Diagram 10. The modulated bar is formed by Q499, CR498, and CR498, with timing information from Diagrams 2_a and 4. The timing pulses switch current from R499 and R482 through Q499 and into the filter.

Flat Field Logic

A high FLAT FIELD ENABLE is generated at U470B pin 8 when pins 9 and 10, and pins 1 or 13 are low. Two high inputs on pins 1 and 2 are required for a low output on pin 3 of U450A. The operation of U470A is the same as U470B. Q449 acts as an inverter to drive U470A pin 2 and provides an output that is complementary to that of U359A.

Alternate Switching Logic

This circuit provides complementary ALT switching signals to the Full Field Logic circuit on Diagram 4.

The output on pin 3 of U359A is low each time pin 8 of divide-by-2 counter U339B is high and pin 1 of U359A is high. Pin 1 of U359A is grounded by S9280 only in the ALL LINES position of the front panel switch.

FULL FIELD ENABLE is high on pin 8 of U359C when either input is low. Pin 9 is driven by U359B for ALL LINES and ALT modes. When U359B pin 4 is high and the MODIFIED VERT BLANKING on pin 5 is high, the output pin 6 is low. Pin 10 of U359C is driven by U359D for FULL FIELD SIG & 3 LINES FLAT FIELD. U339B is clocked 2 μs after the start of each line and divides by 2 so that pin 9 of U339C is high for one line and low for the next. U430A divides by 2 again, providing an output with alternating polarity every two lines. U359D combines the outputs of U430A and U339B so that the output on pin 11 is low for one line then high for three. All counters are reset by MODIFIED VERT BLANKING and held off for the vertical blanking interval. U450B enables U470B for the 3 lines of flat field.

When the jumper on P430 is moved to pins 1 and 2, ALT & 6 LINES FLAT FIELD is enabled. The input to pin 12 of U359D is changed from the output of U339B to the output of U430B. This adds another divide-by-2 to the circuit, giving an output at pin 11 of U359D of two lines low, then six lines high.

LOW FOR WINDOW appears at pin 1 of P461 when CR456, CR454, and CR452 are all low. U450D inverts FULL FIELD ENABLE.

VERT BLANKING is modified to start and end coincident with the end of a line in all fields by U339A. Pin 5 steps low with pin 1, but does not step high with pin 2 until pin 3 is triggered by the characteristic instant pulse for TIME 31 from Diagram 2_a.

MOD PULSE ENABLE

This is part of the circuitry for MOD PULSE ENABLE on Diagram 2_b. U450C pin 8 is low when pins 9 and 10 are high.

DIAGRAM 10

There are two circuit boards shown on Diagram 10, the Ext Drive and the Field Sweep boards.

Field Sweep Ramp Generator

U9678, C9676, and R9674 form an integrating operational amplifier. Q9670, switched on by the modified vertical blanking signal from Diagram 4, discharges C9676 during the vertical interval. When Q9670 turns off, current flows through R9674. Operational amplifier U9678, keeping its inverting input at 0 volt, supplies voltage at its output so that the current will flow through the capacitor. This produces a negative-going ramp, about 12 volts in amplitude. The amplitude of the ramp is changed by R9672 and R9623 before going to the function generator. Adjusting the amplitude allows positioning of the center frequency.

Field Sweep Logic

When FIELD RATE SWEEP GEN signal is selected, U9601C pins 9 and 10 are grounded, putting a high on the Preset of U9694A. This enables U9694A. The flip-flop receives an H Blanking clock pulse and field marker timing at the data input. This provides field markers at the output on pin 5. These markers are each two lines wide.

U9601D pin 12 receives a high from the control logic on Diagram 4. Pin 13 gets horizontal timing information (FLD SWP LINE ENABLE) from Diagram 2_a. The output goes to the function generator enable circuit on Diagram 2_b.

MOD PULSE & BAR Logic

U9601A pin 2 gets a high from the control logic on Diagram 4 when the MOD PULSE & BAR signal is selected. Pin 1 gets horizontal timing information from Diagram 2_b. U9601B inverts the resulting pulse and sends it to Diagram 9_b to enable the MOD PULSE & BAR modulated pulse.

External Drive Receiver

This stage is used to combine externally applied Composite Sync, CW Subcarrier, PAL Pulse, and Burst Flag so that the 148-M will Gen-Lock without a PROGRAM INPUT signal.

Subcarrier. External CW Subcarrier is applied to amplifiers Q9716 and Q9714 90° out of phase, as set by C9719 (225° Phase) and L9710 (135° Phase). This provides subcarrier at 135° and 225°.

PAL Pulse. Q9735 and Q9745, driven by an external PAL Pulse, clamps the output of the 3.57 MHz 135° and 225° subcarrier at 0 volt except during burst time every other 64 μs (i.e., burst is at 135° on one line, then 225° on the next).

Burst Flag. Q9778 and Q9776, driven by external Burst Flag, clamps the 135° burst and 225° burst at 0 volt except during the time of burst.

Comp Sync. Composite sync is summed (at the junction of C9799 and R9796) with burst to provide the signal required for 148-M Gen-Lock.

DIAGRAM 11

The Low Voltage Power Supply circuit provides three regulated supplies; +15 volts, +5 volts, and −15 volts. Electronic regulation is used to provide stable, low ripple

output voltages. All the supplies are current-limited to prevent instrument damage in the event that a supply is shorted to ground. The primary circuit of the transformer employs voltage and range selector plugs to permit selection of the appropriate line voltage operating range.

Power Input

Power is applied to the primary winding of transformer T9001 via RFI Filter FL9201, the POWER switch S9201, 115-volt line fuse F9201, Voltage Selector S9203, and the Range Selector S9202. The voltage selector plug connects the split primaries of T9001 in parallel for the 115-volt range of operation, or in series for 230-volt operation. A second fuse, F9202, is placed in the 230-volt position to provide the correct protection for 230-volt operation.

The Range Selector plug allows the instrument to regulate properly on high or lower than normal line voltages. Each half of the primary has taps above and below the 115-volt (230) point. As the selector is moved from LO, M, HI, more turns are added to the primary winding. Therefore, whether the primary voltage has increased or decreased, the secondary voltage can be maintained at a nearly constant level.

The RFI Filter serves to prevent external RF interference from appearing across T9001 and also prevents signals generated within the 148-M from being introduced into the AC line.

−15 V Supply

The −15 volt supply provides the reference voltage for the +5 and +15 volt supplies. The reference for the −15 volt supply is a 9.1 volt zener diode, VR9850.

The output from the secondary winding (pins 6 and 7 of P9850) is rectified by a bridge rectifier consisting of CR9870, CR9876, CR9874, and CR9872. The rectified voltage is filtered by C9061 and applied through a −15 volt series regulator stage, Q9085, to the load. Series regulator Q9085 and its driver, Q9850, are controlled by a voltage comparator consisting of Q9856 and Q9854 with associated components. C9852 filters any noise generated by −15 volt reference VR9850.

Q9852 and associated components, is an overload protection circuit. During excessive load current, Q9852 (normally off) turns on and limits the current from the −15 V supply.

+5 and +15 Volt Supplies

Both supplies are similar to the −15 volt supply, except that the +5 V supply uses a full wave rectifier instead of a bridge.

MAINTENANCE AND CALIBRATION

This section of the manual contains information for use in maintenance and calibration of the 148-M as follows:

Maintenance

Preventive Maintenance: Cleaning, lubrication, visual inspection, etc.

Troubleshooting: Aids for isolating trouble to a particular stage, etc.

Corrective Maintenance: Replacement procedures and parts ordering information.

Calibration

Inspection: A list of specifications to be checked when performing an incoming inspection.

Procedure: Step-by-step instructions for returning the 148-M to specification.

MAINTENANCE

PREVENTIVE MAINTENANCE

Preventive maintenance consists of cleaning, visual inspection and lubrication. Preventive maintenance performed on a regular basis may prevent instrument breakdown, and will sustain the reliability of this instrument.

Cleaning

General. The 148-M should be cleaned as often as operating conditions require. Accumulation of dirt in the instrument can cause overheating and component breakdown. Dirt on components acts as an insulating blanket that prevents efficient heat dissipation. It also provides an electrical conduction path.

CAUTION

Avoid the use of chemical cleaning agents that might damage the plastics used in this instrument. Avoid chemicals which contain benzene, toluene, xylene, acetone, or similar solvents.

Exterior. Loose dirt accumulated on the outside of the 148-M can be removed with a soft cloth or small paint brush. The paint brush is particularly useful for dislodging dirt on and around the front-panel controls. Dirt that remains can be removed with a soft cloth dampened in a solution of water and mild detergent. Abrasive cleaners should not be used.

Interior. Dust in the interior of the instrument should be removed occasionally due to its electrical conductivity under high-humidity conditions. The best way to clean the interior is to blow off the accumulated dust with dry, low velocity air. Remove any dirt that remains with a shoft paint brush or a cloth dampened with a mild detergent and water solution. A cotton-tipped applicator is useful for cleaning in narrow spaces.

Lubrication

The reliability of switches and other moving parts can be maintained if they are kept properly lubricated. Use a cleaning-type lubricant (e.g., TEKTRONIX Part No. 006-0172-00) for switch contacts. This lubricant does not affect the electrical characteristics of the switch. To lubricate the switch detent, use a heavier lubricant (e.g., TEKTRONIX Part No. 006-0219-00). Do not over-lubricate.

Visual Inspection

The 148-M should be inspected occasionally for such defects as broken connections, loose or disconnected pin connectors, improperly seated solid-state devices, damaged circuit boards and heat-damaged components.

The correct procedure for most defects is obvious; however, particular care must be taken if heat-damaged components are found. Overheating usually indicates other trouble in the instrument; therefore, it is important that the cause of overheating be corrected to prevent recurrence of the damage.

Transistor and Integrated Circuit Checks

Periodic checks of the transistors and integrated circuits (IC's) used in the 148-M are not recommended. The

best indication of performance is the actual operation of the component in the circuit. Performance of the circuit is thoroughly checked when performing either the performance check or calibration procedure. Any substandard transistors or integrated circuits will usually be detected at that time.

TROUBLESHOOTING

The following information is provided to facilitate troubleshooting of the 148-M. Information contained in other sections of this manual should be used along with the following information to aid in locating the defective component. An understanding of the circuit operation is very helpful in locating troubles.

Troubleshooting Aids

Diagrams. Circuit diagrams are provided on foldout pages at the rear of this manual. Each component, its electrical value and circuit number are shown on the diagrams. In addition, typical voltages that can be expected are also shown.

Each diagram has been assigned a diagram number and name. For example, the first diagram has been assigned the number 0_a and is called PROGRAM LINE AMPLIFIER. (Other circuitry exists on this diagram but, since the program line amplifier is of prime importance, it was so called.) Notice the tinted blue lines that surround most of the circuitry on this diagram. These lines are used to identify a particular circuit board on which the components are physically located. This reference allows for correlation between the diagrams, circuit boards, and electrical parts list. Components on the circuit board that are not shown on diagram 0_a will be found on diagram 0_b.

Table 4-1 lists the various reference diagrams, circuit boards, and electrical numbers used in the 148-M. All components located outside the blue line are chassis mounted components and have circuit numbers from 9000 to 9499.

Circuit Boards. Fig. 4-1 shows the location of each circuit board within the instrument. Each circuit board is shown (full view) opposite the appropriate diagram in the Diagram section. Each electrical component on the board is identified by its circuit number. In most cases, these circuit numbers were assigned on a grid system as a convenience to the user of the instrument. For example, notice the circuit board photo opposite diagram 0_a. The upper left hand corner of this board has been assigned numbers around 500. Proceeding left to right, the numbers go towards 900 at the upper right hand corner. From top to bottom, the numbers increase to 590 at the bottom left corner and 991 at the bottom right corner. Using this method, the physical location of each component is readily available.

TABLE 4-1

Diagram	Function or Circuit Board Name	Circuit Numbers
$9_{a/b}$	Subc & Sync Out	0-499
$0_{a/b}$	VITS Insertion	500-999
1	Vert Counter	1000-1999
$2_{a/b}$	Horiz Timing	2000-2999
$3_{a/b}$	APL-Staircase-Noise	3000-3999
4	VITS & FF	4000-4999
$5_{a/b/c}$	Gen-Lock	5000-5999
$6_{a/b}$	Function Gen	6000-6999
$7_{a/b}$	Output Amplifier	7000-7999
8	Modulator	8000-8999
12	Switching & Chassis	9000-9499
10	Field Swp & Ext Drive	9500-9799
11	Power Supply	9800-9999

Waveforms. Important waveforms (typical) are given opposite the appropriate diagram in the Diagram section. These waveforms aid in determining if a circuit is functioning properly.

Wire Color Codes. All insulated wires in the 148-M are color coded to facilitate circuit tracing. Table 4-2 summarizes the coding system used in the 148-M.

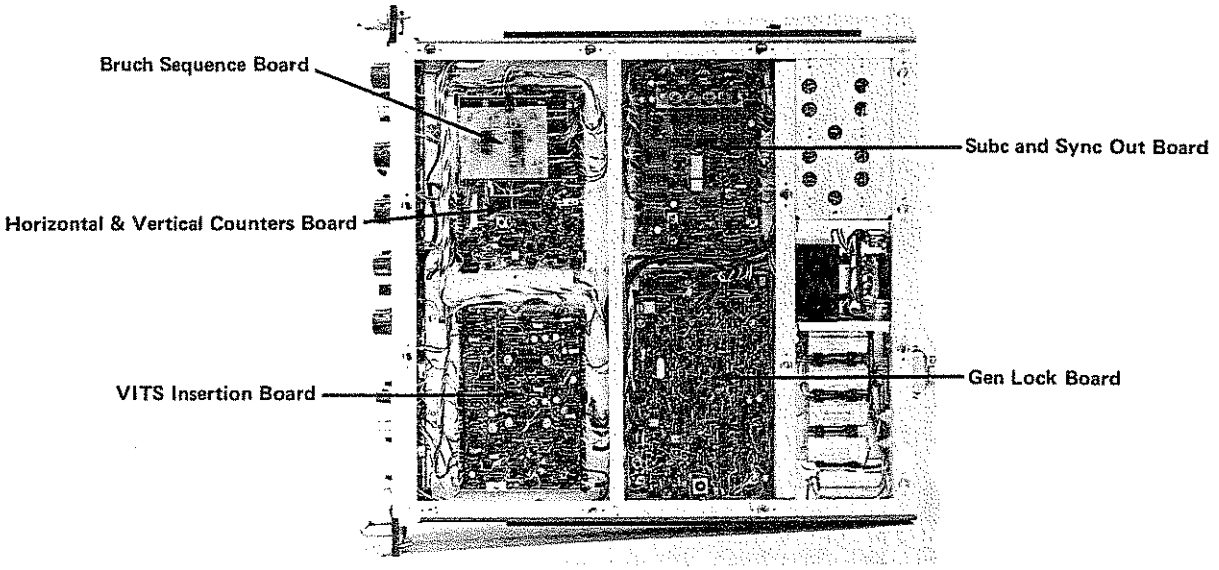
TABLE 4-2

Color Code	Significance
Black	Chassis Ground
White on Black	Floating Ground
Yellow on Green	Safety Ground
Gray[1]	AC Line
White[1]	Signal
Red[2]	$+V_{cc}$
Violet[2]	$-V_{cc}$

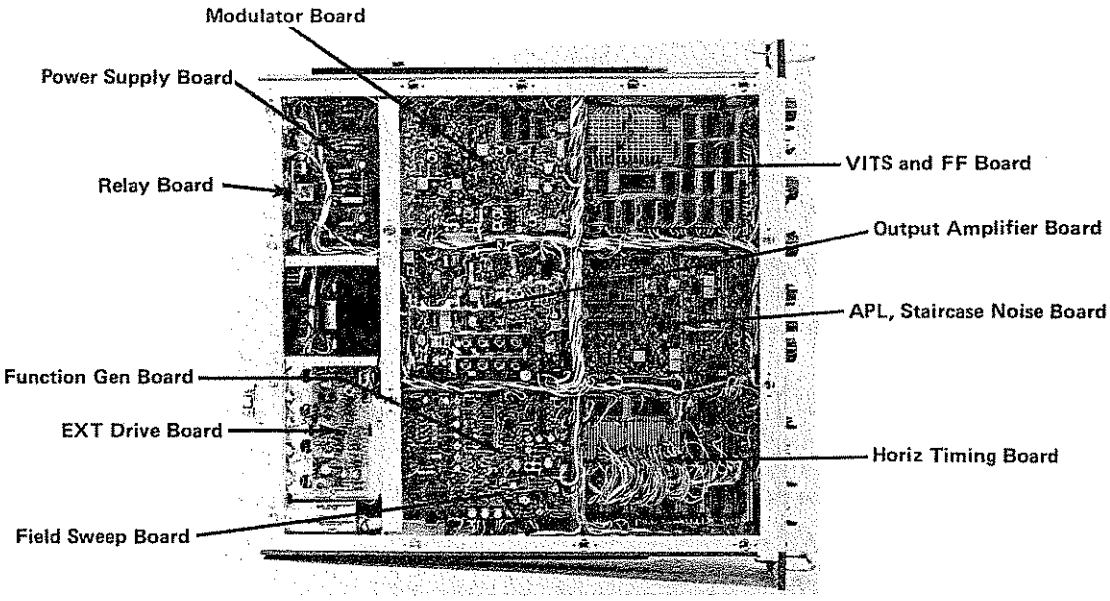
[1]Color Stripes are used on these wires as an aid to circuit tracing.

[2]Color Stripe on wire indicates position of supply with respect to 0 volt (e.g., a black stripe on a red wire would be the first voltage in the positive direction). If a second stripe is used (white only), this indicates a non-regulated supply.

Resistor Color Code. In addition to the brown composition resistors, metal film resistors (identified by their gray or light blue color) are used in the 148-M. The resistance values of composition and metal film resistors are color-coded on the components with the standard EIA color code.



BOTTOM VIEW



TOP VIEW

Fig. 4-1. Location of circuit boards in the 148-M.

Capacitor Markings. The The capacitance value of a common disc capacitor or small electrolytic is marked in microfarads on the side of the component body. The white ceramic capacitors used in the 148-M are color-coded in picofarads using a modified EIA code. "Tear drop" capacitors are color-coded in microfarads using a modified EIA code, with the dot indicating both temperature and the positive (+) side.

Troubleshooting Techniques

This troubleshooting procedure is arranged in an order that checks the simple possibilities before proceeding with extensive troubleshooting.

1. Check Control Settings. Incorrect control settings may indicate trouble that does not exist. If there is any question about the correct function or operation of any control, see the Operating Instructions.

2. Check Operation of Associated Equipment. Many times malfunction of equipment can be traced to associated equipment.

3. Visual Check. Visually inspect the portion of the instrument in which the trouble is located. Look for unsoldered connections, loose pin connectors, broken wires, damaged circuit boards, damaged components, etc.

4. Check Circuit or Instrument Calibration. The apparent trouble may only be a result of misadjustment and may be corrected by calibration. Complete calibration instructions are given in this section.

5. Isolate Trouble to a Circuit. To isolate trouble to a circuit, note the trouble symptoms. The symptoms often identify the circuit in which the trouble is located. When trouble symptoms appear in more than one circuit, check affected circuits by taking voltage and waveform readings.

Incorrect operation of all circuits often indicates trouble in the power supply. Check first for correct voltage of the individual supplies. A defective component elsewhere in the circuit can also appear as a power supply trouble, and affect the operation of other circuits.

The Circuit Description section of this manual can be used as a guide for isolating a trouble. This description explains how the various signal components are combined to form the video signal. By using the front-panel controls and checking the signals at the BNC connectors, it is possible to determine circuits that are functioning properly and those that are not.

When a trouble is isolated to the smallest possible area, proceed with steps 6 through 8 in this troubleshooting procedure to locate the defective component(s).

6. Check Circuit Board Interconnections. After the trouble has been isolated to a particular area or circuit, check the pin connectors on the circuit board for correct connection.

The pin connectors used in this instrument also provide a convenient means of circuit isolation. For example, a short in a power supply can be isolated by disconnecting the power distribution pin connectors at the Power Supply board when making resistance to ground checks.

7. Check Voltage and Waveforms. Often the defective component can be located by checking for the correct voltage or waveform in the circuit. Typical voltages and waveforms are given in the Diagrams section.

NOTE

Voltages and waveforms given on the diagrams are not absolute and may vary slightly between instruments. To obtain operating conditions similar to those used to take these readings, see the back side of the Diagrams Title page.

CAUTION

Due to the component density on the circuit boards, care should be taken with meter leads and probe tips. Accidental shorts can cause abnormal voltages or transients that may destroy many components.

WARNING

"Ground lugs" are not always at ground potential. Check the diagrams before using such connections as a ground for the voltmeter test prod or oscilloscope probe. Some transistor cases may be at voltages that can cause an electrical shock.

8. Check Individual Components. The following procedures describe methods of checking components in the 148-M. Components that are soldered in place should be checked without removal, by isolating the component if circuit conditions allow. If component isolation is questionable, unsolder one end.

a. Transistors. The best check of transistor operation is actual performance under operating conditions. If a transistor is suspected of being defective, it can best be

checked by substituting a new transistor. However, be sure that circuit conditions are not such that a replacement might also be damaged. If substitute transistors are not available, use a dynamic tester such as the TEKTRONIX Type 576.

b. Diodes. A diode can be checked for an open or shorted condition by measuring the resistance between terminals. Use the Rx 1 k scale of an ohmmeter. The resistance should be very high with the leads across the diodes in one direction, and very low when they are reversed.

CAUTION

Do not use an ohmmeter range that has a high internal current. High current may damage some signal diodes. Never test tunnel diodes or back-diodes with an ohmmeter.

9. Repair and Readjust the Circuit. If any defective component or part is located, follow the replacement procedure given in this section. Be sure to check the performance of any circuit that has been repaired or that has had any electrical components replaced.

CORRECTIVE MAINTENANCE

Corrective maintenance consists of component replacement and instrument repair. Special techniques or procedures required to replace components in this instrument are described here.

Obtaining Replacement Parts

All electrical and mechanical replacement parts for the 148-M can be obtained through your local TEKTRONIX Field Office or representative. However, many of the standard electronic components can be obtained locally in less time than is required to order from Tektronix, Inc. Before purchasing or ordering replacement parts, consult the Parts List for value, tolerance, and rating.

NOTE

When selecting replacement parts, it is important to remember that the physical size and shape of a component may affect its performance at high frequencies.

Multiple Terminal Connector Holders. Most inter-circuit connections between the circuit boards, or between the boards and the chassis-mounted components, are made through pin connectors. The terminals in the connector holder are identified with numbers. Connector orientation to the circuit board is keyed with triangles, one on the holder and one on the circuit board. See Fig. 4-2.

Circuit Boards. If the circuit board is damaged beyond repair, the entire assembly, including all soldered-on components, can be replaced.

Transistor and Integrated Circuit Replacement. Transistors and integrated circuits (IC's), should not be replaced unless they are actually defective. Replacement or exchange of components may affect the calibration of the instrument. If a transistor or integrated circuit is removed during routine maintenance, return it to its original socket.

Any replacement component should be of the original type or a direct replacement. Bend the leads to fit the socket and cut the leads to the same length as on the component being replaced. See Fig. 4-3 for basing diagrams.

The chassis-mounted power-supply transistors and their mounting bolts are insulated from the chassis. In addition, silicone grease is used to increase heat transfer capabilities. Re-install the insulators and replace the silicone grease when replacing these transistors. The grease should be applied to both sides of the mica insulators, and should be applied to the bottom side of the transistor where it comes in contact with the insulator.

WARNING

Voltages are present on the exterior surface of the chassis-mounted power supply transistors if the power is applied to the instrument and the POWER switch is on.

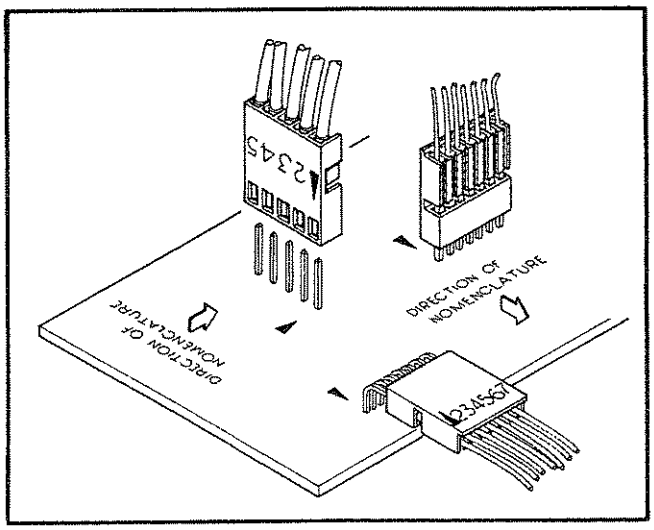


Fig. 4-2. Multipin circuit board connectors.

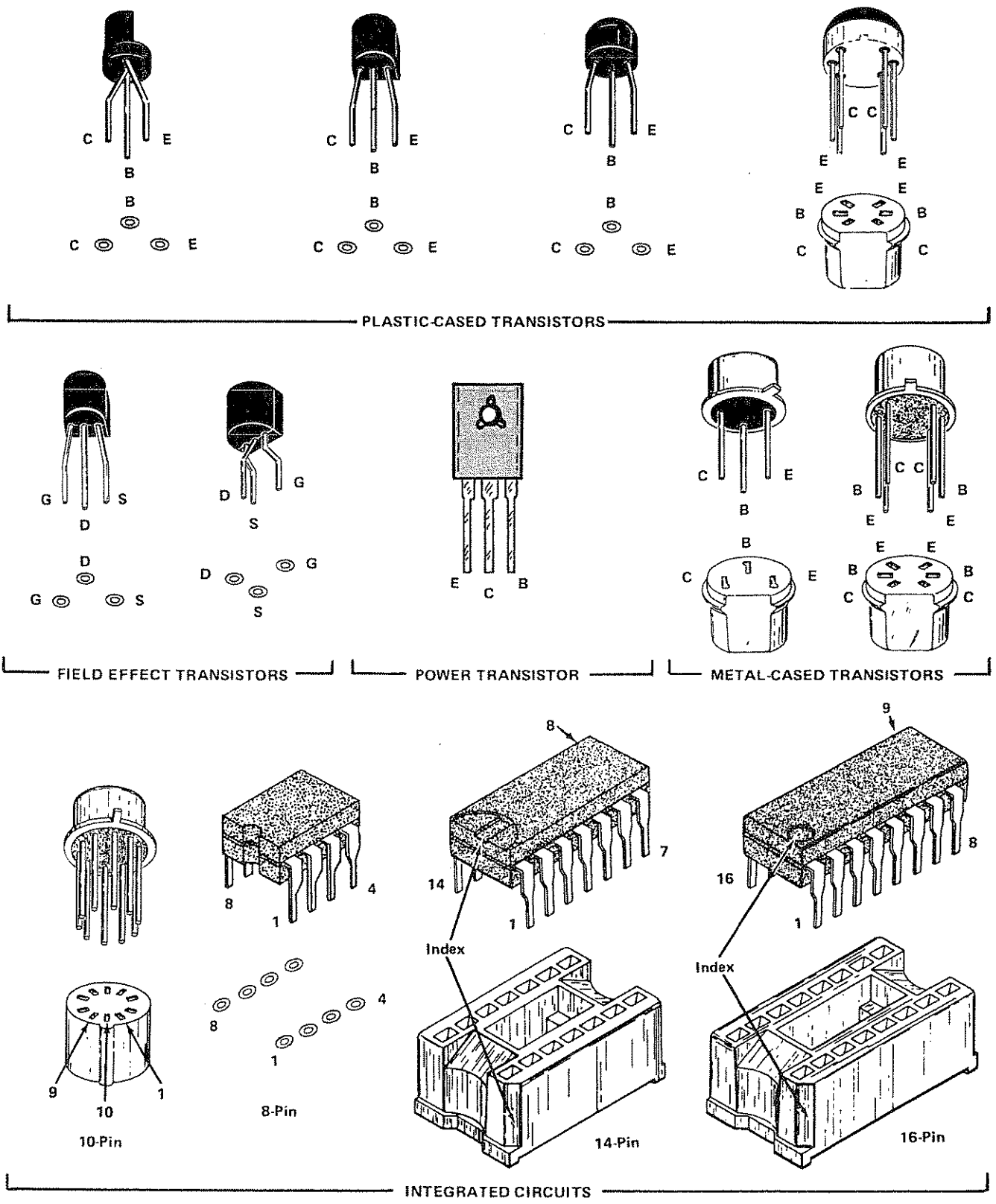
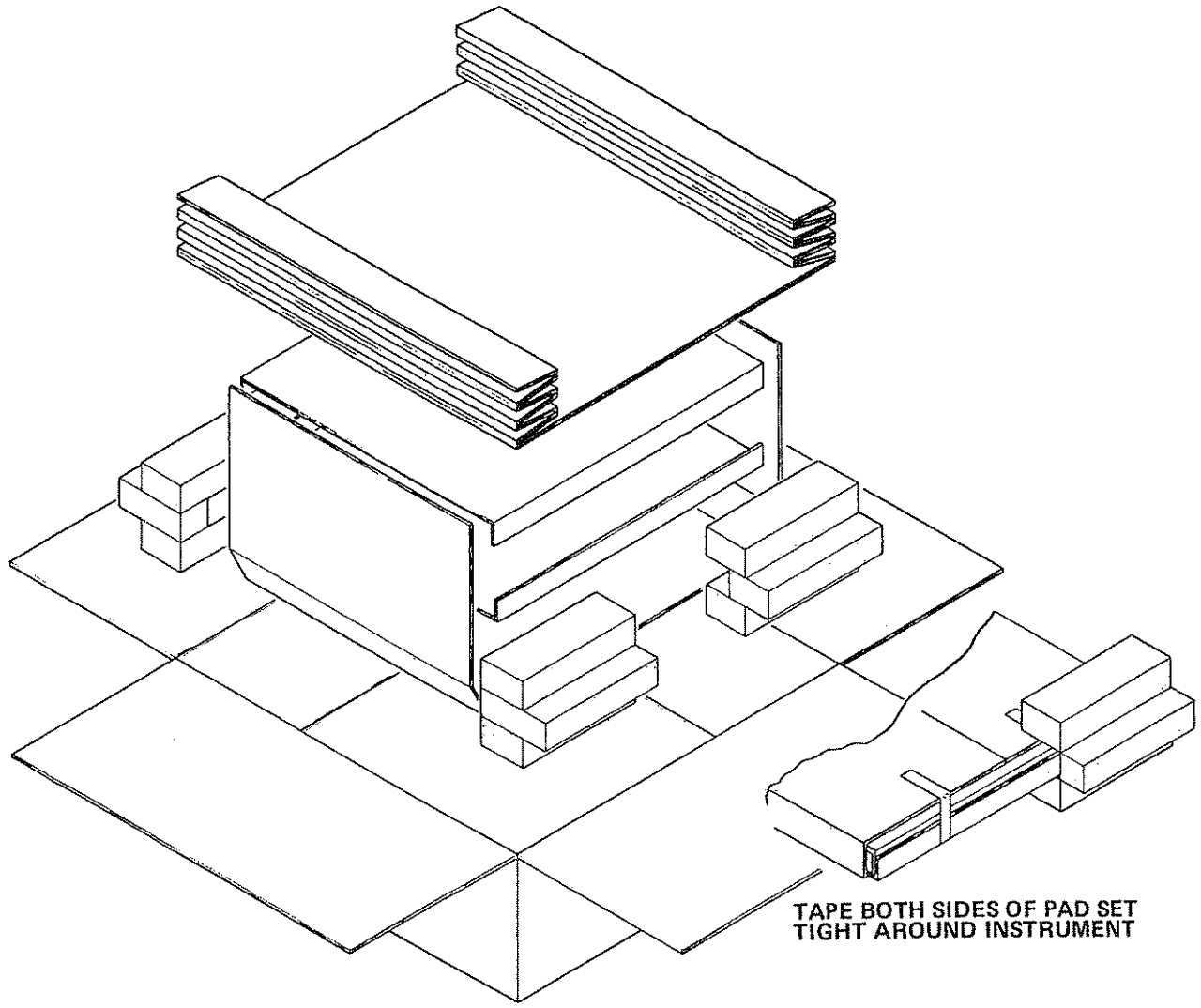


Fig. 4-3. Transistor and Integrated Circuit basing diagrams.



Repackaging for Shipment:

If the Tektronix instrument is to be shipped to a Tektronix Service Center for service or repair, attach a tag showing: owner (with address) and the name of an individual at your firm that can be contacted, complete instrument serial number and a description of the service required.

Save and re-use the package in which your instrument was shipped. If the original packaging is unfit for use or not available, repackage the instrument as follows:

1. Obtain a carton of corrugated cardboard having inside dimensions of no less than six inches more than the instrument dimensions; this will allow for cushioning. Refer to Table 1 for carton test strength requirements.
2. Surround the instrument with polyethylene sheeting to protect the finish of the instrument.
3. Cushion the instrument on all sides by tightly packing dunnage or urethane foam between carton and instrument, allowing three inches on all sides.
4. Seal carton with shipping tape or industrial stapler.

Table 1. Shipping Carton Test Strength.

Gross Weight (lb.)	Carton Test Strength (lb.)
0 — 10	200
10 — 30	275
30 — 120	375
120 — 140	500
140 — 160	600

1929-17

Fig. 4-4. Repackaging instructions.

After any component is replaced, check the operation and calibration of the associated circuits.

Indicator Lamp Replacement. To remove the POWER ON indicator lamp, remove the top dust cover from the instrument, then reach behind the front-panel and unplug the lamp from its socket. To replace the lamp, reverse the procedure.

The NOT LOCKED TO PROGRAM, PROGRAM, PREVIEW, and BYPASS indicators consist of two parts; a lens that is attached to the instrument, and a lens cap (connected to the back of the lens) into which the lamps have been soldered. To remove the lamps, reach behind the front-panel, grasp the lens cap and pull straight away from the front-panel. The lens cap will unsnap from the lens, allowing lamp access. Unsolder the lamp. To replace, solder the new lamp into the lens cap. Then place the lens cap on the back of the lens and apply enough pressure to snap the cap into place over the lens.

Fuse Replacement. Both line fuses are contained in plastic holders in the cover for the Line Voltage Selector Assembly at the rear of the instrument. Use only the correct value replacement fuse. Only the upper fuse within the assembly (3/4 A) is used for 115-volt operation. However, for 230-volt operation both the upper and lower fuse (1/2 A) must be installed.

Switches. If a switch is defective, replace the entire assembly. Replacement switches can be ordered by referring to the Parts List for the applicable part numbers.

Power Transformer Replacement. If the power transformer becomes defective, contact your local TEKTRONIX Field Office or representative for replacement. Replace only with a direct replacement TEKTRONIX transformer.

Power Input Connector and RFI Filter Replacement. The Power Input Connector and RFI Filter is replaceable as a unit and repair should not be attempted. If replacement is necessary, observe proper polarity to ensure instrument protection.

The narrow blade (terminal number 4) should show continuity to terminal number 3, which connects to fuse F9201 (see diagram 11). (The filter contains an internal non-replaceable fuse between these two terminals.) Use care when soldering to terminals numbers 1 and 3, as excess solder could possibly short the filter case.

CALIBRATION

This portion of the manual contains the adjustment sequence for calibrating the 148-M to the performance requirements listed in the Specification section. Limits, tolerances, and waveforms in this procedure are given as calibration guides and are not instrument specifications, unless given in the Specification section.

The Short Form Inspection Procedure is provided so that those familiar with the long-form calibration can check instrument specification without following the step-by-step procedure. Those unfamiliar with the 148-M should follow the complete calibration procedure, omitting all adjustments, to check instrument performance.

SHORT FORM INSPECTION PROCEDURE

		Group	Step
1. CW SUBCARRIER OUT			
Output	2 V ±10%	1	5
2. COMPOSITE SYNC OUT			
a. Aberrations	⩽4%	1	6
b. Amplitude	4 V ±10%	1	6
3. OUTPUT AMPLITUDES			
a. FLAT FIELD, 100% PEAK WHITE	700 mV ±1%	2	2
SYNC	−300 mV ±1%	2	3
Output DC level	0 V ±50 mV	2	4
FLAT FIELD (front)	700 mV ±1%	2	5
b. FULL FIELD SIG Timing (see Fig. 1-2)		2	6

SHORT FORM INSPECTION PROCEDURE (cont)

		Group	Step
4. LUMINANCE			
a. LINEARITY			
RAMP	700 mV ±1%	3	1a
10 STEPS	700 mV ±1%	3	1b
5 STEPS	700 mV ±1%	3	1c
b. SIG-III			
Bar	700 mV ±1%	3	2
c. CCIR-II			
MB White Ref Pedestal	700 mV ±1%	3	3a
CCIR-II Center Level	350 mV ±5 mV	3	3b
d. FLAT FIELD Amplitudes			
FIELD SQ. WAVE	700 mV ±1%	3	4a
PRESET—WHITE	595 to 700 mV	3	4b
BLACK	0 to 105 mV	3	4c
BOUNCE	BLACK to WHITE	3	4d
BOUNCE RATE	≤1 sec. to ≥10 sec.	3	4e
e. NOISE PEDESTAL Amplitudes			
700 mV	700 mV ±2%	3	5a
350 mV	350 mV ±2%	3	5b
50 mV	50 mV ±5 mV	3	5c
5. MODULATOR			
a. Residual Subcarrier	≤2.5 mV	4	1
b. Bandpass Filter	Straight vectors, narrow openings	4	2
c. Harmonics	≥40 dB down	4	3
d. Phasing			
Signal Modulation	180° ±5°	4	4a
+V Burst	135° ±1°	4	4a
−V Burst	225° ±1°	4	4b
Difference between Bursts	90° ±1°	4	4c
6. CHROMINANCE			
a. Burst Amplitude	300 mV p-p ±3%	5	1b
b. LINEARITY Modulation			
100 mV	100 mV p-p ±1%	5	2a
140 mV	140 mV p-p ±1%	5	2b
c. CCIR-I Modulation	280 mV p-p ±1%	5	3
d. CCIR-II Modulated Pedestal			
Level 1	140 mV p-p ±1%	5	4a
Level 2	280 mV p-p ±1%	5	4b
Level 3	560 mV p-p ±1%	5	4c

SHORT FORM INSPECTION PROCEDURE (cont)

		Group	Step
e. Chrominance Risetimes			
Burst	375 ns ±50 ns	5	5a
CCIR-II Modulated Pedestal	400 ns ±25 ns	5	5b
f. MOD PULSE & BAR			
12.5T Pulse, Half Amplitude Duration	1.57 μs ±50 ns	5	6b
Baseline Ripple	⩽3.5 mV	5	6c
Amplitude (pulse-to-bar ratio)	100% ±1%	5	6d
Luminance Components	350 mV ±2%	5	6e
7. PULSE AMPLITUDE AND WIDTH			
a. 2T Pulse			
Amplitude (pulse-to-bar ratio)	100% ±1%	6	1a
Width (HAD)	250 ns ±15%	6	1b
b. T Pulse			
Amplitude (pulse-to-bar ratio)	100% ±1%	6	2
Width (HAD)	125 ns ±15%	6	2
c. Bar Risetimes			
T Bar	115 ns ±15%	6	3
2T Bar	225 ns ±15%	6	3
8. MULTIBURST			
a. Harmonics	40 dB down	7	1
b. Frequencies	500 kHz ±3% 1.0 MHz ±3% 2.0 MHz ±3% 3.0 MHz ±3% 3.57 MHz ±3% 4.2 MHz (+0%, −2%)	7	2
c. MB Length	Cycles start and stop at center	7	3
d. Flatness			
350 mV	±0.5% of 500 kHz amplitude	7	4a
700 mV	±0.5% of 500 kHz amplitude	7	4b
e. MB Average Level	4.2 MHz level matches reference level on 522A	7	5
f. MB Sync Level	Horizontal and vertical sync levels match.	7	6
g. MB Amplitudes			
700 mV	700 mV ±1%	7	7a
350 mV	350 mV ±1%	7	7b

@

SHORT FORM INSPECTION PROCEDURE (cont)

		Group	Step
9. FIELD RATE SWEEP GEN			
a. Timing	≈1 MHz/marker	8	1
b. Amplitudes			
Pedestal	350 mV ±5 mV	8	2a
350 mV	350 mV ±1% to 6 MHz	8	2b
700 mV	700 mV ±1% to 6 MHz	8	2c
10. FULL FIELD DIFF GAIN & PHASE			
a. Diff Gain	≤0.5%	9	1
b. Diff Phase	≤0.2°	9	2
11. NOISE			
a. Amplitude	−20 dB to −59 dB ±1 dB	10	1b
b. Half-line Insertion	(NOISE INSERTION)	10	2
Full-line Pedestal	(NOISE DELETION)	10	2
c. Noise Match	PROGRAM LINE noise matches half-line inserted noise	10	3b
d. VARIABLE Pedestal	±50 mV from pedestal, except, +50 mV and −36 mV from the 50 mV pedestal	10	4a
e. Baseline Transients	≤32 mV	10	4b
f. Noise Spectrum	Flat to 5 MHz ±6 dB	10	5
12. GEN LOCK			
a. NOT LOCKED TO SYNC Light	On when no sync input	11	1b
b. Outputs	No COMP SYNC or CW SUBCARRIER when no comp sync input	11	1b
	No CW SUBCARRIER when no incoming burst or subcarrier	11	1b
c. INT/EXT Mode	TP5698 pulses are same for INT or EXT modes	11	2b
	Loss of any input removes pulses at TP5698	11	2b
d. Sync Stripper	TP5970—5 to 6 V of comp sync in INT or EXT	11	3
	TP5282 amplitude is always 0.8 to 1.2 volts, with or without comp sync	11	3
e. Chroma AGC Ratio	1:1.6	11	4
f. 3.57 MHz Frequency	3.57561149 MHz ±25 Hz	11	5
g. Sound Inhibit	275 ns before end of sync	11	6

SHORT FORM INSPECTION PROCEDURE (cont)

	Group	Step
13. VITS INSERTION—DIFF PHASE & GAIN		
a. PROGRAM OUTPUT LINE: diff phase, ≤0.15° and diff gain, ≤0.2%	12	1b, 1c
VAR LEVEL at Max: diff phase, ≤0.3° and diff gain, ≤0.4%	12	1d
b. PREVIEW OUTPUTS: diff phase, ≤0.3° and diff gain, ≤0.4%	12	2
14. VITS INSERTION		
a. PROGRAM OUTPUT LINE		
Gain Change Between PROGRAM, PREVIEW & BYPASS: Unity gain ±1%, all signals	13	2c
DC Level: within 50 mV of BYPASS LEVEL	13	2b
PROGRAM FLATNESS: within 1% of FF TEST SIGNAL	13	4b
PROGRAM VITS Flatness: within 1% of FF TEST SIGNAL	13	4b
b. PREVIEW OUTPUTS		
Gain, PROGRAM OUTPUT LINE to PREVIEW MONITOR OUT: Unity gain ±1%	13	3c
DC Level: within 50 mV of BYPASS LEVEL	13	3b
PREVIEW VITS Flatness: within 1% of FF TEST SIGNAL	13	4a
PREVIEW Flatness: within 1% of FF TEST SIGNAL	13	4a
Other PREVIEW OUTPUT		
c. INSERT SUBCARRIER PHASE		
≥5° either side of 180°	13	5a
Set for no error, PROGRAM	13	5b
No error, PREVIEW	13	5b
d. Unwanted VITS Pedestal		
PROGRAM & PREVIEW: ≤5 mV	13	2b
e. Amplitude Ratio, PROGRAM	13	2e
2T Pulse-to-Bar: 100% ±0.25% (1.8 mV)		
12.5T Pulse-to-Bar: 100% ±0.5% (3.5 mV)		
12.5T Luminance to Chrominance Change: ≤0.5%		
f. Frequency Response		
±1% to 5 MHz	13	6g
g. Waveform Tilt, PROGRAM & PREVIEW	13	10
26 μs Bar: ≤0.5%		
FIELD Rate SQ WAVE: ≤0.5%		
Line Tilt: ≤0.25%		
15. AUXILIARY PEDESTAL & UNITY GAIN—VAR LEVEL		
a. AUXILIARY PEDESTAL	13	11
≥−70 mV to ≥630 mV		
b. UNITY GAIN—VAR GAIN	13	12
≤70% to ≥140%, PROGRAM & PREVIEW		
c. Bypass Relay	14	4a, 4b

SHORT FORM INSPECTION PROCEDURE (cont)

	Group	Step
16. PROGRAM LINE OUT—ABERRATIONS		
a. Residual Subcarrier: −60 dB (≤0.7 mV)	13	13a
b. Inactive Part of Lines: −40 dB (≤7 mV)	13	3b
c. Active Part of Lines		
Spurious: −60 dB (≤0.7 mV)	13	13c
FF 2T Pulse: −70 dB (≤0.22 mV)	13	13d
FF Subcarrier (Staircase): −60 dB (≤0.7 mV)	13	13d
All Other FF Signals: −60 dB (≤0.7 mV)	13	13d
d. Delete Mode		
2T (from 148-M): −70 dB (≤0.22 mV)	13	13g
Subcarrier (Color Bars): −60 dB (≤0.7 mV)	13	13g
Any Int Signal (Rotate FF Switch): −60 dB (≤0.7 mV)	13	13g
e. Non-inserted Lines		
Hum & Power Line Transients: −60 dB (≤0.7 mV)	13	13e
f. Random Noise		
−75 dB (0.14 mV or less)	13	13f
17. INSERT DELAY & TIMING		
a. Delay: Start of Sync to Start of NOISE or MB VITS, 11.5 to 12.5 μs with INSERT DELAY adjustment.	14	3a
b. INSERT DELAY Range: 1.5 μs or more	14	1a
c. Serration Width: 4.5 μs ±0.2 μs Sync Width: 4.71 μs ±0.05 μs Equalizer Width: 2.4 μs ±0.1 μs	14	2
18. RETURN LOSS		
a. PROGRAM LINE, POWER Off		
At least −30 dB (≤7.5 mV) to 5 MHz	15	3c

CALIBRATION PROCEDURE

General

The calibration procedure is arranged in a sequence designed for calibration with minimum interaction of adjustments and reconnection of equipment. However, some adjustments affect the calibration of other circuits, and it may be necessary to check the operation of other parts of the instrument. Where adjustments interact, they are noted.

The procedure uses the equipment and fixtures listed in the Test Equipment Used list. If test equipment is substituted for that on the list, control settings, setups, and methods of measuring may have to be altered.

The 148-M front- and rear-panel control titles and signal output connectors are capitalized (i.e., COMP SYNC). Internal adjustment titles are initial capitalized only (i.e., Subcarrier Ampl.).

Test Equipment Used

All test equipment is assumed to be correctly calibrated and operating within the given specification.

Test Equipment for Adjustment Steps

1. Waveform Monitor. TEKTRONIX 1482 Waveform Monitor. If a 1480-Series monitor is not available, a test

oscilloscope with differential inputs, and the Chopped Voltage Reference listed in the optional test equpment list should be used.

2. Vectorscope. TEKTRONIX 522A PAL-M Vectorscope or equivalent.

3. Test Oscilloscope. Bandwidth, dc to at least 30 MHz; delaying time base; and vertical deflection factor of at least 5 mV/Div. TEKTRONIX 7603 Oscilloscope with 7A18 Dual Trace Amplifier and 7B53A Dual Time Base or equivalent.

4. Video Signal Source. Signals: PAL-M color bars or modulated staircase (5 steps and 140 mV subcarrier) and VITS insertion; composite sync, subcarrier, PAL pulse, and burst flag. TEKTRONIX 145-M PAL-M Test Signal Generator or equivalent.

5. DC Voltmeter. Capable of measuring 5 and 15 volts within 1%. TEKTRONIX DM 501 or equivalent.

6. Coaxial CABLES (7). 75 Ω with BNC connectors (cable). TEKTRONIX Part No. 012-0074-00 or equivalent.

7. Terminations (3). 75 Ω end-line, with BNC connectors (end-line termination). TEKTRONIX Part No. 011-0102-00 or equivalent.

8. Terminations (2). 75 Ω feed-through with BNC connectors (feed-through termination). TEKTRONIX PART No. 011-0103-02 or equivalent.

9. RMS Voltmeter. Capable of measuring 70 mV to 0.14 V. HEWLETT-PACKARD Model 3400A or equivalent.

10. Filter. Continuous Random Noise Measurement Low Pass Filter, $F_c = 4.2$ MHz. (4.2 MHz Low Pass Filter.) TEKTRONIX Calibration Fixture 015-0212-00 or equivalent.

11. Spectrum Analyzer. Center frequency, 0.1 MHz; resolution, 100 kHz; frequency span, at least 2 MHz/div; RF attenuation range, capable of measuring 40 dB below the reference signal. TEKTRONIX 1401A or equivalent.

Optional Test Equipment

12. Variable Autotransformer. Power supply regulation. Capable of supplying at least 200 volt-amperes over the desired line voltage range. GENERAL RADIO W10MT3W Metered VARIAC Autotransformer or equivalent.

13. Weighting Network. Program Line Out aberrations. Continuous Random Noise Measurement Weighting Network, $F_c = 4.2$ MHz. (4.2 MHz Weighting Network.) TEKTRONIX Calibration Fixture 015-0214-00 or equivalent.

14. Test Oscilloscope. Bandwidth dc to at least 30 MHz; minimum deflection factor, 1 mV/division; two input channels capable of independent or differential operation; time base, at least 0.1 μs/division and slower. TEKTRONIX 7603 Oscilloscope with 7A13 and 7B53A plug-ins or equivalents.

15. Chopped Voltage Reference. TEKTRONIX Calibration Fixture 067-0596-00 (chopper) or equivalent. Use if 1482 Waveform Monitor is not available.

16. Sinewave Generator. Return loss and frequency response. Output of at least 500 mV; frequency range, 50 kHz reference and variable from 1 MHz to 6 MHz. TEKTRONIX SG 503 Leveled Sinewave Generator or equivalent (signal generator).

17. Return Loss Bridge. Use with differential amplifier and signal generator. TEKTRONIX Part No. 015-0149-00.

18. Minimum Loss Attenuator, 50 Ω to 75 Ω. Use with spectrum analyzer and signal generator. TEKTRONIX Part No. 011-0057-00.

Preliminary Procedure

1. Install the rear-panel REMOTE plug P9014. Allow a ten minute warmup at 25°C ±5°C before checking or calibrating the instrument.

2. Set the 148-M switches to the up or to the right position, except:

BURST	NORM
NOISE	OFF
FULL FIELD SIG (left)	LINEARITY
FULL FIELD SIG (right)	FLAT FIELD
% PEAK WHITE	100
FLAT FIELD	VAR APL

3. Connect an external 1-volt peak-to-peak composite video signal to the 148-M PROGRAM INPUT.

NOTE

Unless otherwise noted, connections made to the 148-M are via a 75 Ω coaxial cable.

4. From the 148-M rear-panel FULL FIELD TEST SIGNAL OUT connector, connect a cable to the monitor A Input; loop-through, with another cable, to the vectorscope A Input; terminate the vectorscope loop-through with a 75 Ω end-line termination.

NOTE

Unless otherwise stated, 148-M signals to the test oscilloscope are applied through a cable that is terminated with a feed-through termination at the test oscilloscope input.

5. Externally trigger the test oscilloscope with composite sync.

6. Connect the video signal source composite sync signal to the monitor Ext Sync Input; connect the loop-through, with another cable, to the vectorscope Ext Sync Input; terminate the vectorscope loop-through with a 75 Ω end-line termination.

7. Connect the video signal source subcarrier to the vectorscope Ext ϕ Ref Input; terminate the vectorscope loop-through with a 75 Ω end-line termination.

NOTE

Preliminary steps 2 through 7 are the basic setup for this procedure. If no setup is given at the start of a step, use this one.

GROUP 1—INITIAL

NOTE

Do not adjust the power supplies if they are within the listed tolerances. Adjustment of any supply will affect the operation of other circuits within the instrument. If a complete recalibration is being performed, set each voltage to the exact setting.

1. Check/Adjust Power Supply Voltage

a. Connect a precision dc voltmeter between chassis ground (pin 1 of P9834) and P9852 (−15 V), see Fig. 4-5.

CHECK—Voltage should be −15 V within 1% (−14.85 to −15.15 V).

ADJUST—R9851 (−15 Volt Adj) for −15 V.

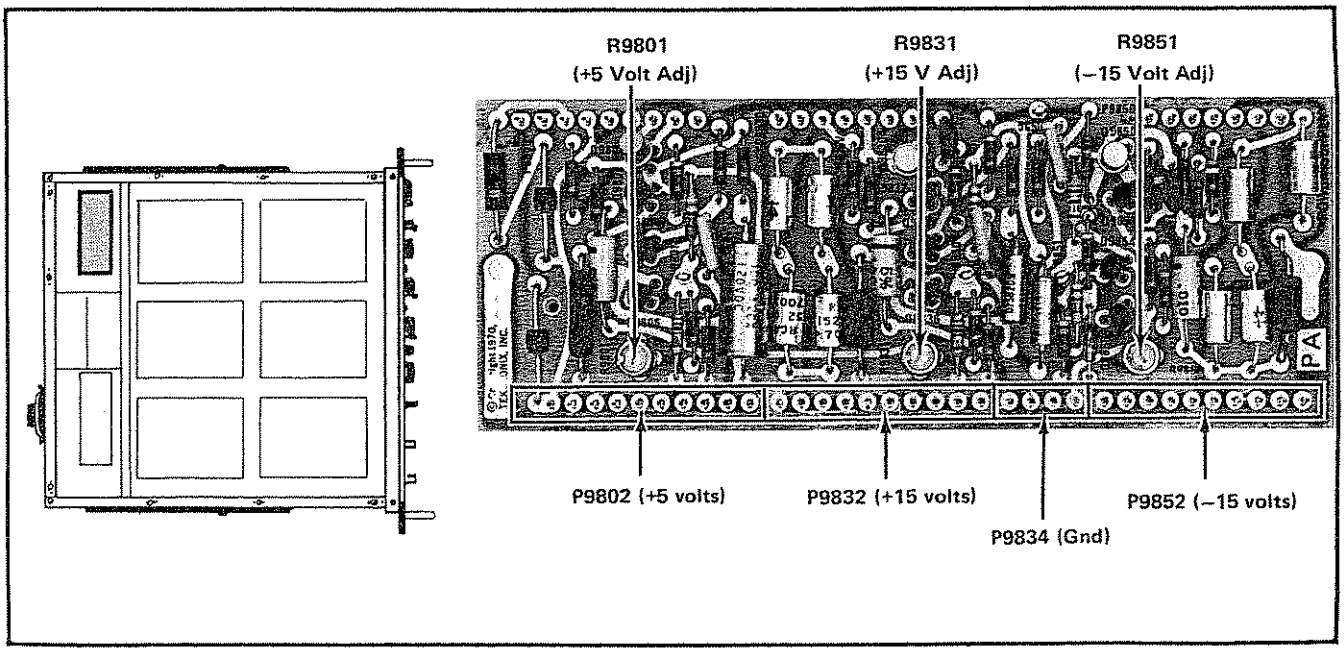


Fig. 4-5. Power Supply test point and adjustment locations.

b. Connect the voltmeter between chassis ground and P9832 (+15 V).

CHECK—Voltage should be +15 V within 1% (14.85 to 15.15 V).

ADJUST—R9831 (+15 Volts Adj) for +15 V.

c. Connect the voltmeter between chassis ground and P9802 (+5 V).

CHECK—Voltage should be +5 V within 1% (4.95 to 5.05 V).

ADJUST—R9801 (+5 Volts Adj) for +5 V.

d. Repeat the above adjustments to remove any interaction.

2. Check Power Supply Ripple

Use a 1X probe between the supply under test and the test oscilloscope.

CHECK—Power line related ripple at these plugs:

Plug	Supply	Max Ripple
P9852	−15 V	10 mV
P9832	+15 V	10 mV
P9802	+5 V	10 mV

3. Check/Adjust 1 MHz Oscillator Lock

Establish a 0-volt (ground) reference point on the test oscilloscope. Connect a 10X probe to TP1720, see Fig. 4-6.

CHECK—Display dc level should be approximately +2.5 V.

ADJUST—L1670 (1 MHz Osc) to position the display midway between the two levels at which the oscillator free-runs (one level near +5 V dc and the other near 0 V dc).

4. Check/Adjust INSERT DELAY Range

Connect the 10X probe to the back of the FULL FIELD TEST SIGNAL OUT connector. Display the full-field signal and establish a horizontal timing reference point.

CHECK—Rotation of the INSERT DELAY control, through its range, should move the display 1 μs or more.

ADJUST—INSERT DELAY control to electrical midrange.

5. Check/Adjust Subcarrier Amplitude

Display the 148-M CW SUBCARRIER OUT on the test oscilloscope.

CHECK—Subcarrier amplitude should be between 1.8 and 2.2 V peak-to-peak.

ADJUST—L190 (Subcarrier Ampl), see Fig. 4-7, for a subcarrier amplitude of 2 V peak-to-peak.

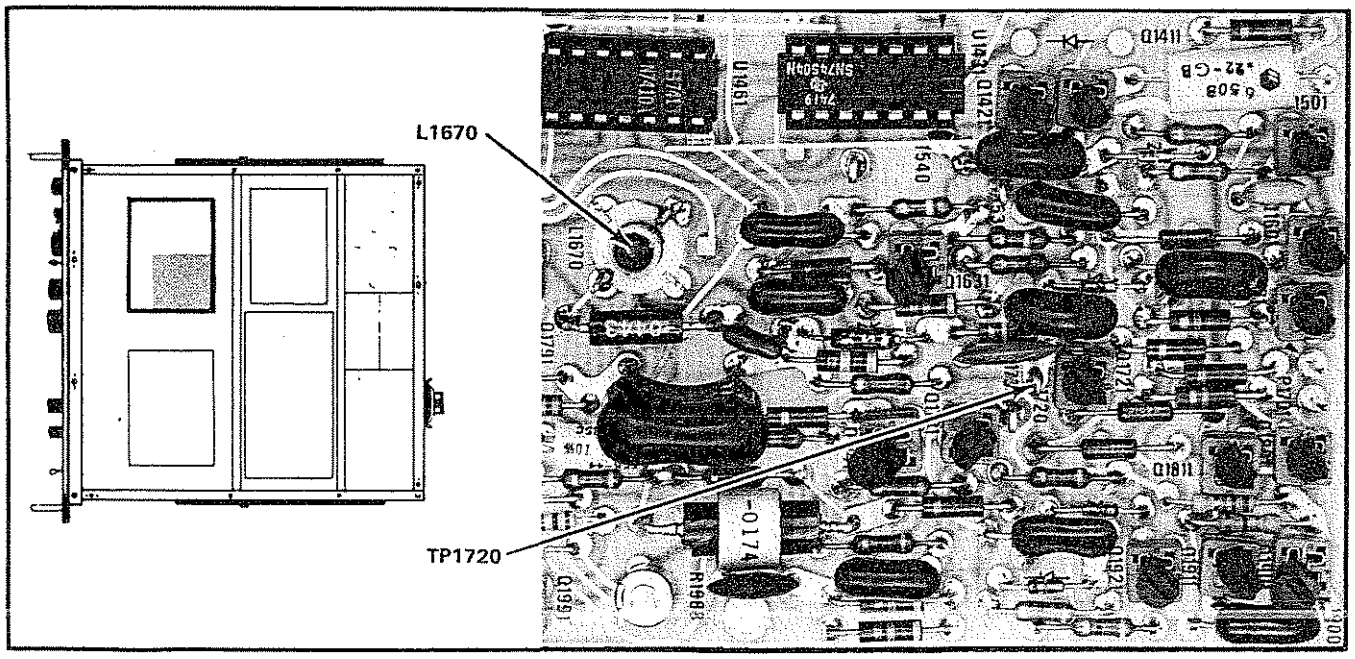


Fig. 4-6. Horizontal Counter test point and adjustment locations.

6. Check/Adjust Composite Sync

Display the 148-M COMP SYNC on the test oscilloscope.

CHECK—Composite Sync amplitude should be between 4 and 5 V peak-to-peak.

CHECK—Aberrations on leading corner of the sync should be 4%, or less, of the total amplitude.

ADJUST—L20 and L120 (Sync Filter), see Fig. 4-7, for the best square corner on the leading edge of sync with aberrations 4% or less.

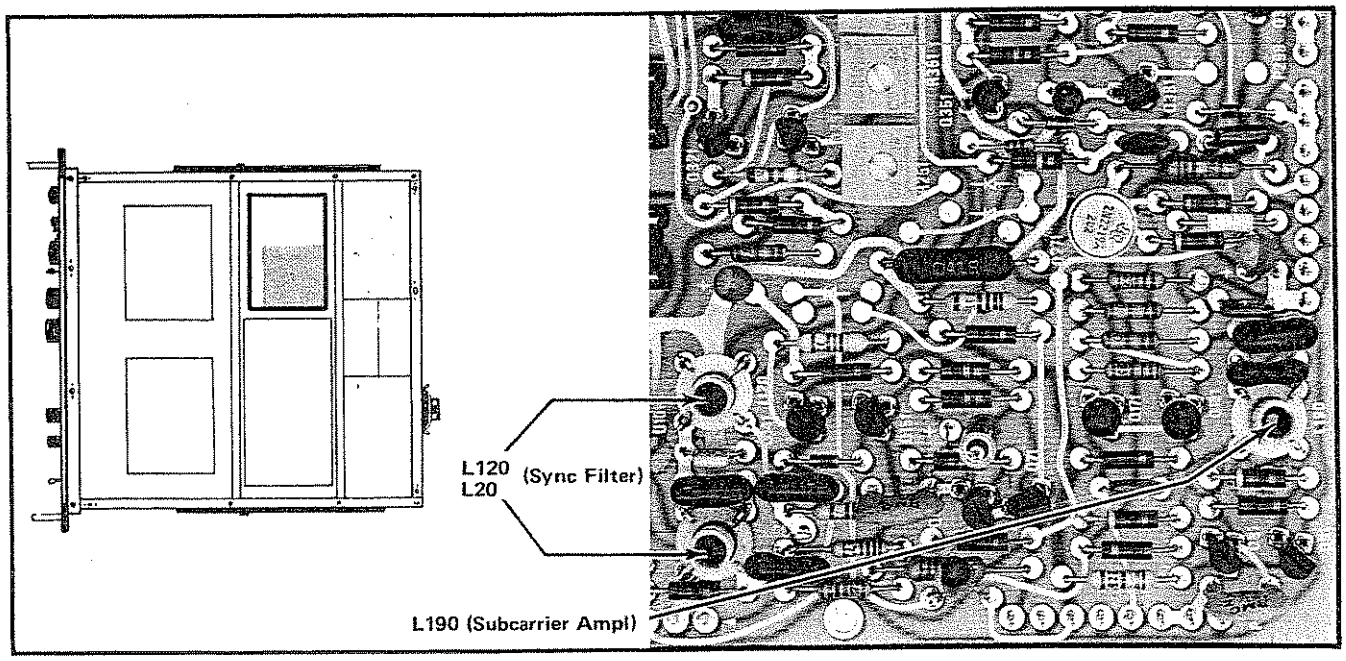


Fig. 4-7. Subcarrier & Sync filter adjustment locations.

GROUP 2—OUTPUT AMPLITUDES

1. Setup

Display the rear-panel FULL FIELD TEST SIGNAL on the A Input of the 1482 Waveform Monitor. Set the Waveform Monitor for Ch. A, DC Cpl'd, 0.2 Volt Full Scale, 10 μs/Div, Mag off, all grey pushbuttons in except DC Restorer is Off, and Waveform Comparison Off. Position the blanking level to midscreen.

Disconnect P8490 (see Fig. 4-8) to remove chrominance from the signal during this part of the procedure. Set R6942 (MB Sync Level, see Fig. 4-9) to match the horizontal and vertical blanking levels. Set R7453 (P & B Sync Level, see Fig. 4-10) to midrange.

Push the Back Porch DC Restorer button (700 mV Cal square-wave), and both the Oper and Cal buttons. Position the display to show the pedestal and the blanking level overlayed.

2. Check/Adjust Pedestal Amplitude

CHECK—Pedestal matches the blanking level within 3.5 minor divisions (700 mV within 1%).

ADJUST—R7735 (Reference Ampl, see Fig. 4-10), so the pedestal exactly overlays the blanking level (700 mV).

3. Check/Adjust Sync Amplitude

Push the 1482 Sync Tip DC Restorer button (1 V Cal square-wave). Position the display to show the overlayed sync tip and pedestal.

CHECK—Sync and pedestal overlays within 1.5 minor divisions (300 mV within 1%).

ADJUST—R8920 (Sync Ampl, see Fig. 4-8), so the sync and pedestal exactly overlay (300 mV within 1%).

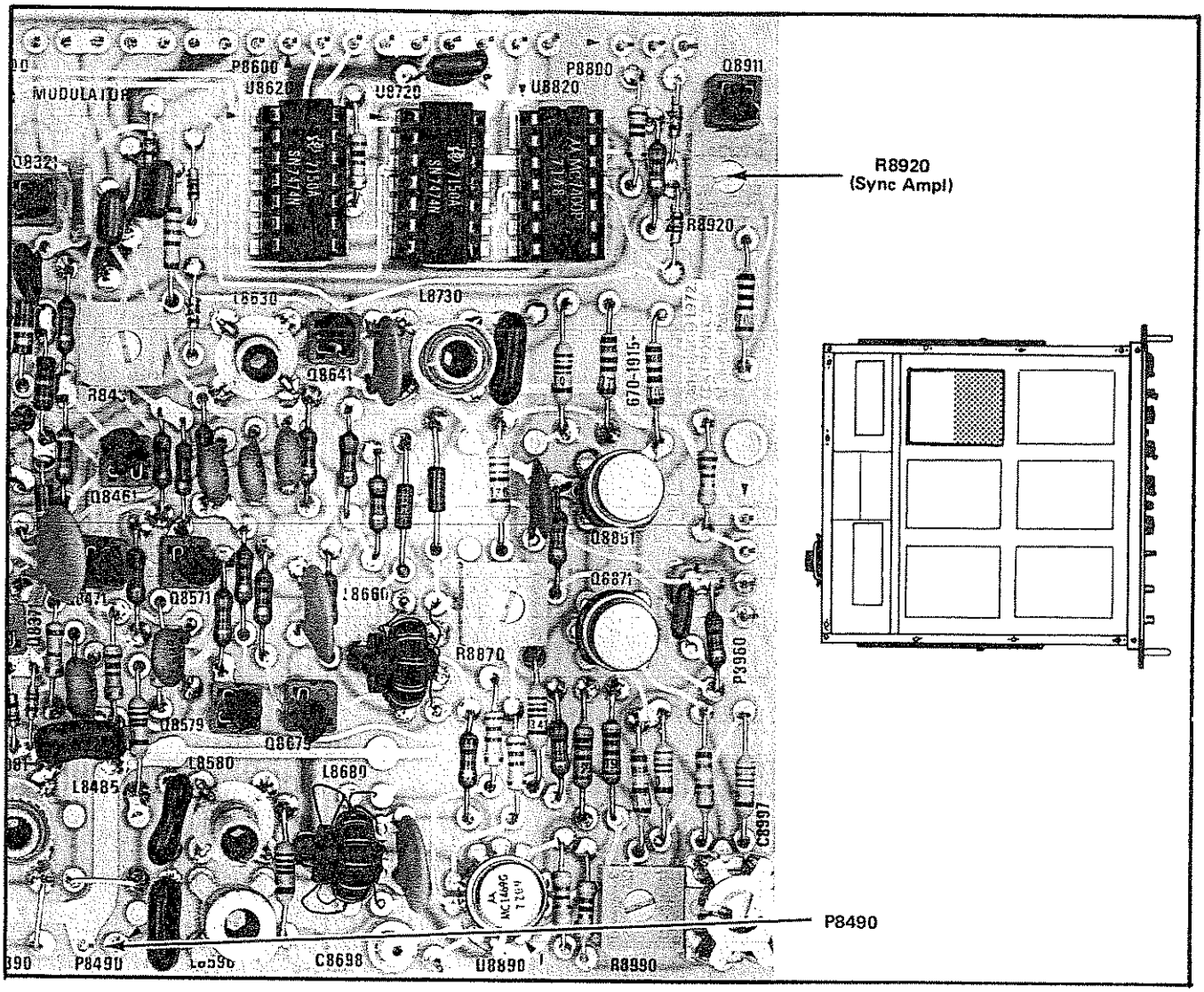


Fig. 4-8. Modulator circuit board locations of P8490 and Sync Ampl adjustment.

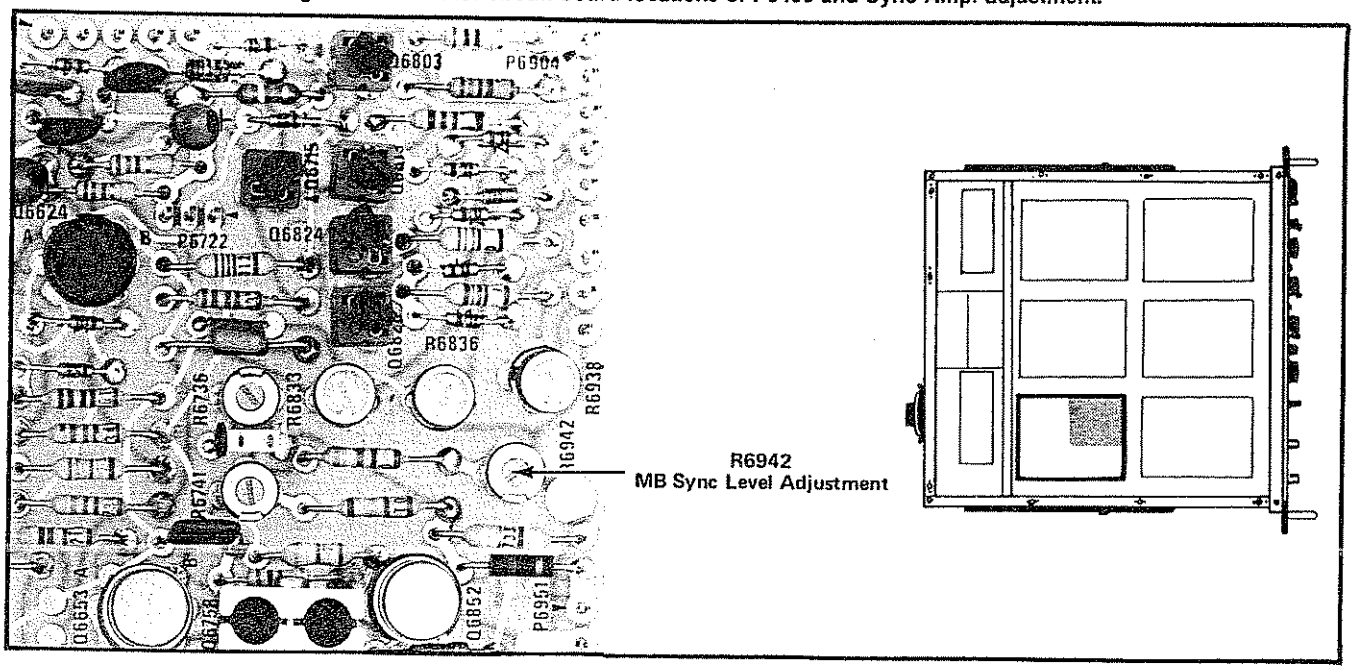


Fig. 4-9. Function Generator circuit board location of MB Sync Level adjustment.

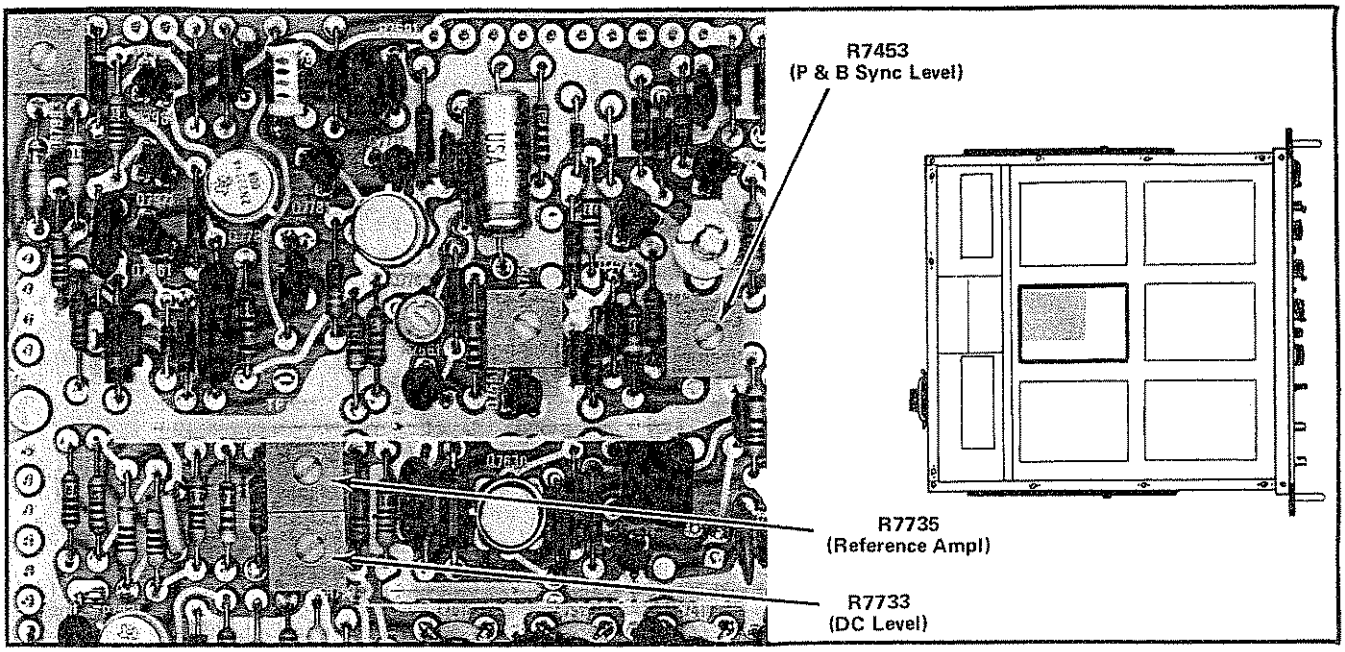


Fig. 4-10. Output Amplifier adjustment locations.

4. Check/Adjust Output DC Level

Push just the 1482 Oper button. Disconnect the FULL FIELD TEST SIGNAL temporarily. Set the 1482 Vertical Position to establish a ground reference on a horizontal graticule line. Reconnect the 148-M to the A Input.

CHECK—Blanking level is at the ground reference line within 2.5 major divisions (0 volt within 50 mV).

ADJUST—R7733 (DC Level, see Fig. 4-10) to position the blanking level to the ground reference line (0 volt).

5. Check FULL FIELD SIGNAL Outputs

Display the front-panel FULL FIELD TEST SIGNAL OUT on the 1482 Waveform Monitor. Push the Back Porch DC Restorer button (700 mV Cal) and both the Oper and Cal buttons.

CHECK—Pedestal amplitude is within 3.5 minor divisions of overlaying the blanking level (700 mV within 1%).

Return the rear-panel FULL FIELD TEST SIGNAL OUT to the A Input of the 1482. Set the 1482 for 1.0 Volt Full Scale.

6. Check Full-Field Signal Timing

Using Fig. 1-2 of this manual as a guide, check that each full-field signal generated by the 148-M is horizontally programmed as shown.

Return the 1482 to 0.2 Volt Full Scale.

GROUP 3—LUMINANCE

1. Check/Adjust LINEARITY Amplitudes

a. Set the 148-M FULL FIELD SIG Mode switch to ALT. Position the display (100% peak white alternating with the LINEARITY RAMP) so 100% PEAK WHITE is at a reference graticule line.

CHECK—LINEARITY RAMP peak matches the 100% PEAK WHITE within 3.5 minor divisions (700 mV within 1%).

ADJUST—R3616 (Ramp Ampl, see Fig. 4-11) to match the RAMP amplitude with the 100% PEAK WHITE (700 mV).

b. Set the 148-M LINEARITY switch to 10 STEPS.

CHECK—LINEARITY 10 STEPS peak matches 100% PEAK WHITE within 3.5 minor divisions (700 mV within 1%).

ADJUST—C3470 (10 Step Ampl, see Fig. 4-11) to match the 10 STEP amplitude with the 100% PEAK WHITE (700 mV).

c. Set the 148-M LINEARITY switch to 5 STEPS.

CHECK—LINEARITY 5 STEPS peak matches 100% PEAK WHITE within 3.5 minor divisions (700 mV within 1%).

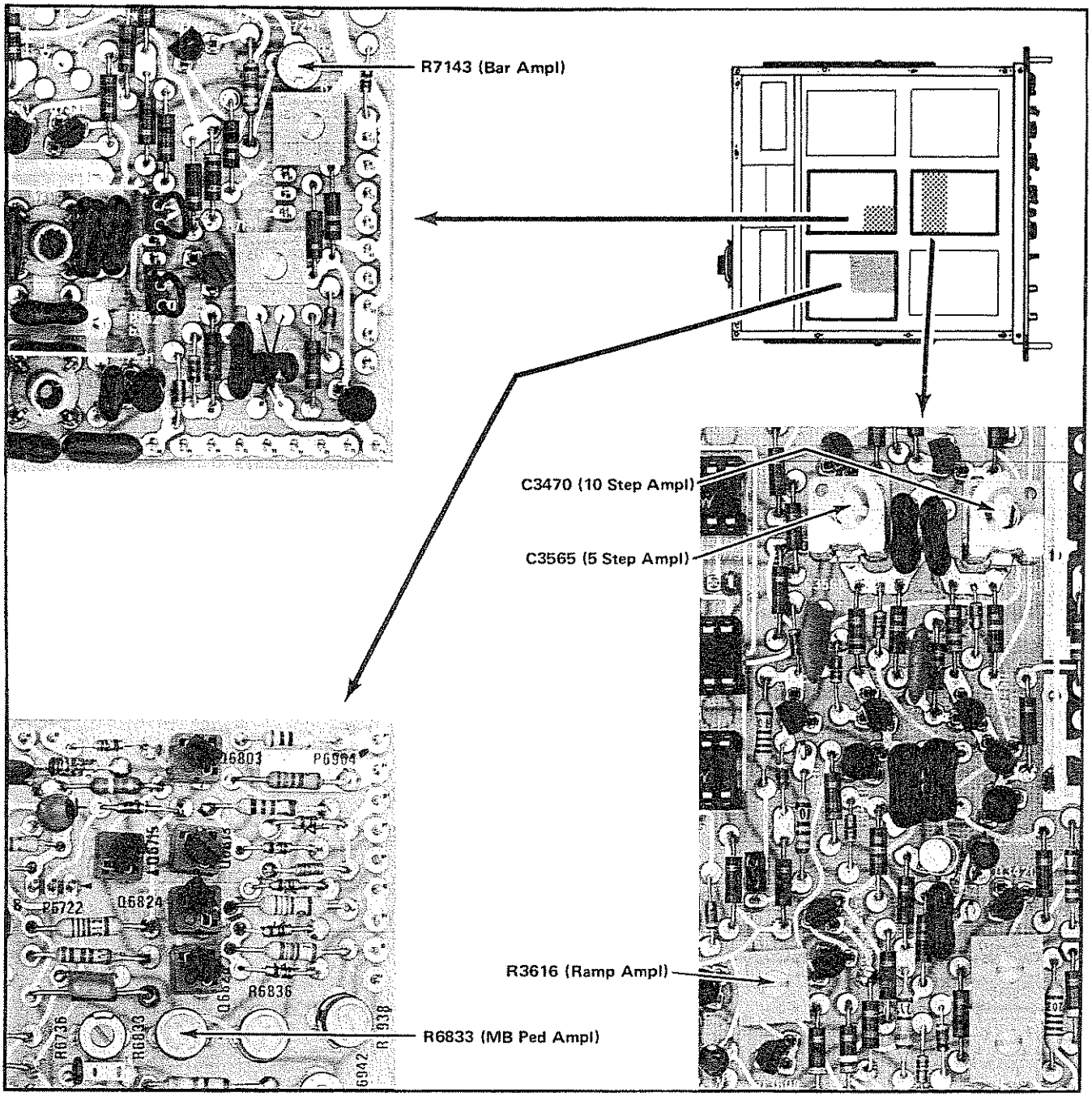


Fig. 4-11. Luminance adjustment locations.

ADJUST—C3565 (5 Step Ampl, see Fig. 4-11) to match the 5 STEPS amplitude with the 100% PEAK WHITE (700 mV).

2. Check/Adjust SIG-III Luminance Amplitudes

Set the 148-M for SIG-III alternating with FLAT FIELD VAR APL. Set the VAR APL switch for 100% PEAK WHITE.

CHECK—Bar matches 100% PEAK WHITE within 3.5 minor divisions (700 mV within 1%).

ADJUST—R7143 (Bar Amplitude, see Fig. 4-11) for bar to exactly match 100% PEAK WHITE (700 mV).

3. Check/Adjust CCIR-II Luminance Amplitudes

a. Set 148-M for CCIR-II signal alternating with 100% PEAK WHITE.

CHECK—MB White Reference Pedestal overlays 100% PEAK WHITE within 3.5 minor divisions (700 mV within 1%).

ADJUST—R6836 (MB Pedestal Amplitude, see Fig. 4-11) for MB White Reference Pedestal to exactly match the 100% PEAK WHITE amplitude (700 mV).

b. Set VAR APL switch to 50% PEAK WHITE.

CHECK—CCIR-II center level overlays the 50% PEAK WHITE within 2.5 minor divisions (350 mV within 5 mV).

4. Check FLAT FIELD Amplitudes

a. Set the FULL FIELD SIG Mode switch to ALL LINES, and VAR APL to 100% PEAK WHITE. Position 100% PEAK WHITE to horizontal reference graticule line on the 1482.

Set FLAT FIELD switch to FIELD SQ WAVE.

CHECK—Amplitude of FIELD SQ WAVE matches amplitude of 100% PEAK WHITE within 3.5 minor divisions (700 mV within 1%).

b. Set the 1482 for 1.0 Volt Full Scale. Position the blanking level to the horizontal reference graticule line. Set the 148-M FLAT FIELD switch to PRESET, and WHITE 85—100%.

CHECK—WHITE adjustment range is 85—100% (595 to 700 mV).

c. Set 148-M for BLACK 0—15%.

CHECK—BLACK adjustment range is 0 to 15% (0 to 105 mV).

d. Set 148-M for BOUNCE.

CHECK—Bounce level alternates between the selected white level and the selected black level.

e. Vary the BOUNCE RATE control.

CHECK—Bounce rate is variable from 1 second or less, at maximum cw, to 10 seconds or more at maximum ccw.

5. Check NOISE PEDESTAL Amplitude (Deletion)

a. Set the 148-M VAR APL and 100% PEAK WHITE. Set the 1482 to 0.2 Volt Full Scale. Position the 100% PEAK WHITE level to the horizontal reference graticule line.

Push the Dig (digital) button and set the Line Selector for line 14.

CHECK—NOISE PEDESTAL amplitude is within 7 minor divisions of the horizontal reference graticule line (700 mV within 2%).

b. Set the NOISE PEDESTAL to 350 mV, and VAR APL to 50% PEAK WHITE. Position the 350 mV pedestal to the reference line.

Push the 1482 Line Selector Off button.

CHECK—50% PEAK WHITE is within 3.5 minor divisions of the reference line (350 mV within 2%).

c. Set the 148-M for a 50 mV NOISE PEDESTAL. Push the Dig Line Selector. Position the blanking level 2.5 major divisions below the horizontal reference graticule line.

CHECK—The 50 mV NOISE PEDESTAL is within 2.5 minor divisions of the horizontal reference graticule line (50 mV within 5 mV).

GROUP 4—MODULATOR

1. Check/Adjust Residual Subcarrier

Connect P8490. Position the blanking level to the horizontal reference graticule line. Push the Line Selector Off button. Set the 148-M for 0% PEAK WHITE.

CHECK—Residual subcarrier is less than 1.25 minor divisions (less than 2.5 mV).

ADJUST—R8990, C8997, and C8698 for minimum residual subcarrier in all positions of the FULL FIELD SIG Selector. (See Fig. 4-12 for adjustment locations.)

2. Check/Adjust Bandpass Filter

Set the 148-M for the SIG-III signal. Observe the 522A Vectorscope.

CHECK—Vectors are straight lines with little or no openings.

ADJUST—L8580 and L8590 (see Fig. 4-12) for minimum vector openings and straight lines.

Recheck step 1 of this group for interaction.

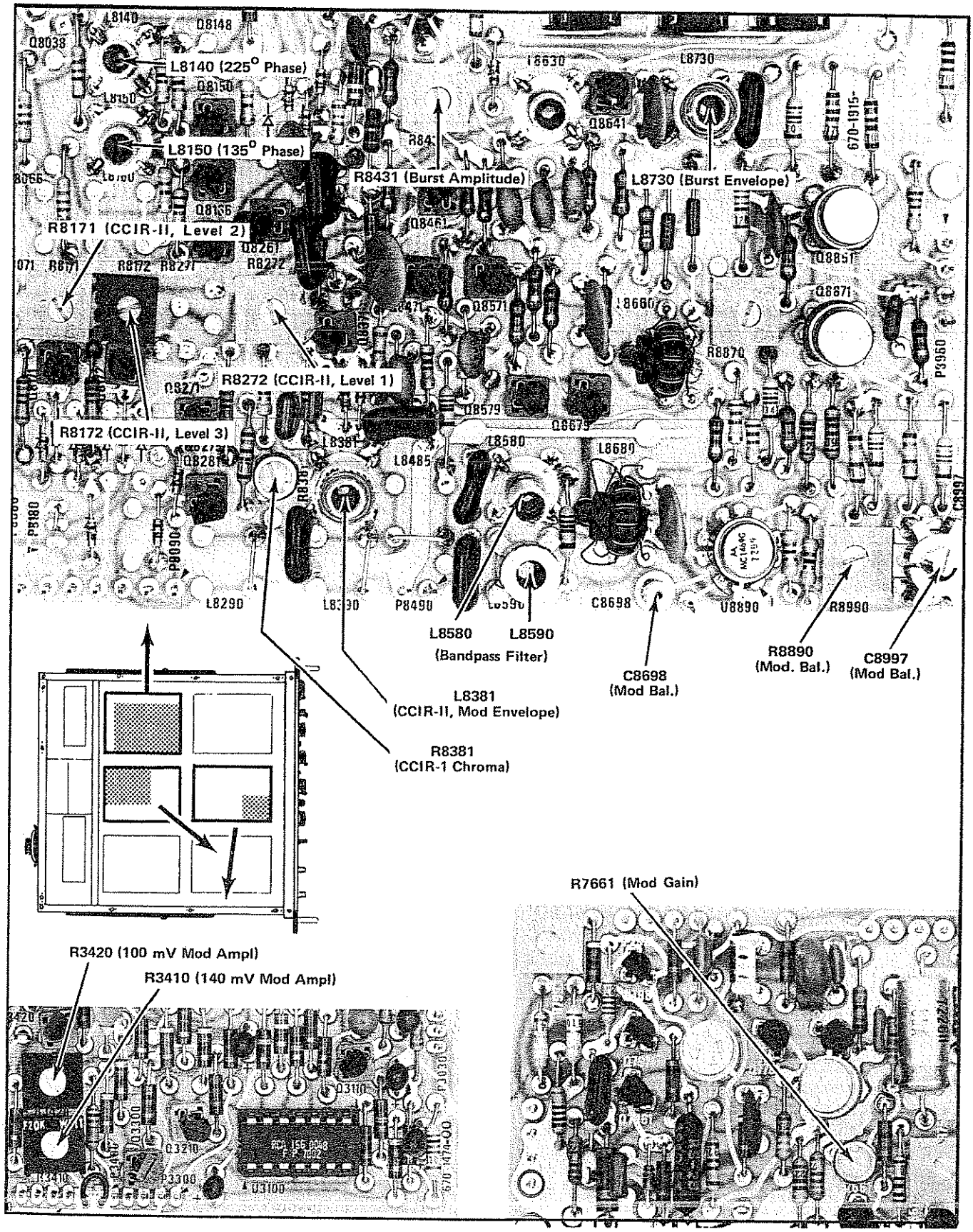


Fig. 4-12. Chrominance adjustment locations.

3. Check Harmonics

Connect the 148-M front-panel FULL FIELD TEST SIGNAL OUT to the input of a Tektronix 1401A Spectrum Analyzer (or equivalent). Connect the 1401A Video Out to the 1482 B Input. Connect the 1401A Sweep Voltage (5 V) to the 1482 External Horizontal Input (check the 1482 Instruction Manual for any special instructions for operating the External Horizontal function). Set the 1482 for 1.0 Volt Full Scale and Ext Display. Setup the 1401A as follows:

POWER	ON
RF ATTEN dB	20
IF GAIN	ccw
VERTICAL DISPLAY	LOG
CENTER FREQ MHz	
1—500	000
FINE	0
SWEEP MODE	FREE RUN
SWEEP RATE	≈10 o'clock
RESOLUTION kHz	100
FREQ SPAN	
MHz/DIV	.5
VAR (CAL IN)	pushed in
VIDEO FILTER	OFF

Allow a 20 minute warmup time for the batteries to charge on the 1401A.

To determine the −40 dB point, set the 1401A RF Atten to 10 dB, and adjust the IF Gain cw until the Multiburst frequencies are of maximum amplitude. Adjust the 1482 Var Volts Full Scale for 6 major divisions of signal. Set the 1401A RF Atten to 60 dB. Position the peaks of the Multiburst frequencies to the horizontal reference graticule line on the 1482. Set the 1401A back to 20 dB.

CHECK—Harmonics at all positions of the FULL FIELD SIG Selector are below the horizontal reference line (≥−40 dB).

If harmonics, other than Multiburst, are of more amplitude than −40 dB, repeat steps 1 and 2 of this group for the best compromise of harmonics, residual subcarrier, and straight vectors.

Return the 1482 to 10 μs/Div Display rate, A Input, and Volts Full Scale Var in detent.

4. Check/Adjust Burst Phase

a. Set the modulated 12.5T pulse vector to the −U axis (180°) with the vectorscope Ch A Phase control. Set the 522A Display switch to +V.

CHECK—+V burst lines up on the graticule marking at 135° within 1°.

ADJUST—L8150 (see Fig. 4-12) for exactly 135° phasing of the +V burst.

b. Set the 522A Display switch to −V.

CHECK—−V burst vector lines up on the graticule marking at 225° within 1°.

ADJUST—L8140 (see Fig. 4-12) for exactly 225° phasing of the −V burst.

c. Set the 522A Display to Both.

CHECK—Phase difference between the two bursts is 90° within 1°.

GROUP 5—CHROMINANCE

1. Check/Adjust Chrominance Amplifier

a. Set the 1482 to 0.2 Volt Full Scale. To verify the scale factor, display a 30% PEAK WHITE signal (210 mV) and adjust the 1482 front-panel Gain control for 10.5 major divisions (0 V to 1.05 V graticule lines).

b. Position the blanking level to the 0.25 V graticule line.

CHECK—Burst peak is on the 1.0 V graticule line within 2.25 minor divisions (150 mV peak, 300 mV peak-to-peak within 3%). Midrange R8431 (Burst Amplitude) for calibration only.

ADJUST—R7661 (Modulation Gain, see Fig. 4-12), for burst peak at the 1.0 V graticule line (150 mV peak, 300 mV peak-to-peak).

Set the blanking level to the 1.05 V graticule line.

CHECK—Negative burst peak is at the 0.3 V horizontal reference line within 2.25 minor divisions (−150 mV peak, 300 mV peak-to-peak).

2. Check/Adjust LINEARITY Modulation

a. Set the 148-M FULL FIELD SIG Selector (right) to LINEARITY. Set LINEARITY switches for 100 mV and 5 STEPS. Position the blanking level to the horizontal reference line.

CHECK—Amplitude of peak-to-peak staircase modulation is 5 major divisions within 0.5 minor division (100 mV peak-to-peak within 1%).

ADJUST—R3420 (100 mV Mod Amplitude, see Fig. 4-12) for exactly 5 major divisions of peak-to-peak staircase modulation (100 mV peak-to-peak).

b. Set the LINEARITY switches for 140 mV and 5 STEPS. Set the FULL FIELD SIG Selector (right) for FLAT FIELD, and the left selector to LINEARITY. Set the FULL FIELD SIG Mode switch to ALT. Change the VAR APL switch from 10% to 30% PEAK WHITE, noting the relative levels of the APL and the staircase modulation.

CHECK—Relative levels of the APL signal and the staircase modulation are the same within 0.7 minor division (140 mV within 1%).

ADJUST—R3410 (140 mV Mod Amplitude, see Fig. 4-12) for exactly 7 major divisions of staircase modulation (140 mV), check as above.

3. Check/Adjust CCIR-I Staircase Modulation

Set the FULL FIELD SIG Selector (left) switch to CCIR-I. Set the VAR APL switch to 40% PEAK WHITE.

CHECK—The relative amplitudes between the blanking level and 40% PEAK WHITE is the same as the staircase modulation amplitude within 1.4 minor divisions (280 mV within 1%).

ADJUST—R8381 (CCIR-I Chroma, see Fig. 4-12), for equal relative amplitudes.

4. Check/Adjust CCIR-II Modulated Pedestal

a. Set FULL FIELD SIG Selector (left) to CCIR-II. Change VAR APL from 40% to 60% PEAK WHITE, noting the relative amplitudes of the APLs and the first modulation level.

CHECK—Relative levels are equal within 0.7 minor division (140 mV within 1%).

ADJUST—R8272 (Level 1, see Fig. 4-12), for equal relative amplitudes (140 mV).

b. Change the VAR APL from 30% to 70% PEAK WHITE, noting the relative amplitudes of the APLs and the second modulation level.

CHECK—Relative levels are the same within 1.4 minor divisions (280 mV within 1%).

ADJUST—R8171 (Level 2, see Fig. 4-12) for equal relative amplitudes (280 mV).

c. Change the VAR APL from 20% to 80% PEAK WHITE, noting the relative amplitudes of the APLs and the third modulation level.

CHECK—Relative amplitudes are the same within 2.8 minor divisions (560 mV within 1%).

ADJUST—R8172 (Level 3, see Fig. 4-12) for equal relative amplitudes.

5. Check/Adjust Chrominance Risetimes

a. Turn the 145-M U BURST switch Off. Mis-adjust R5920 (3.57 MHz adj, see Fig. 4-13) so that the chrominance free runs fast enough to appear solid.

CHECK—Burst risetime is between 325 ns and 425 ns (375 ns within 50 ns).

ADJUST—L8730 (Burst Envelope, see Fig. 4-12) for best transient response and symmetry of burst, with risetime between 325 ns and 425 ns.

b. Set FULL FIELD SIG Selector (right) to CCIR-II, and Mode switch to ALL LINES.

CHECK—Risetimes of Modulated Pedestal are between 375 ns and 425 ns (400 ns within 25 ns).

ADJUST—L8381 (CCIR-II Mod Envelope, see Fig. 4-12) for best transient response of the modulated pedestal, with risetimes between 375 ns and 425 ns.

6. Check/Adjust MOD PULSE & BAR

a. Set the 148-M to alternate MOD PULSE & BAR with the 100% PEAK WHITE signal. See Fig. 4-14 for the location of adjustments for this step. For calibration only, preset the following controls:

R7615 (Modulation Delay) for symmetrical bottom of pulse and bar modulation.

R8870 (Mod Pulse Chroma Gain) for flat bottom of pulse and bar.

R486 (Sin^2 Pulse Gain) for pulse peak at 100% PEAK WHITE (700 mV).

R482 (Sin^2 Bar Gain) for bar peak at 100% PEAK WHITE (700 mV).

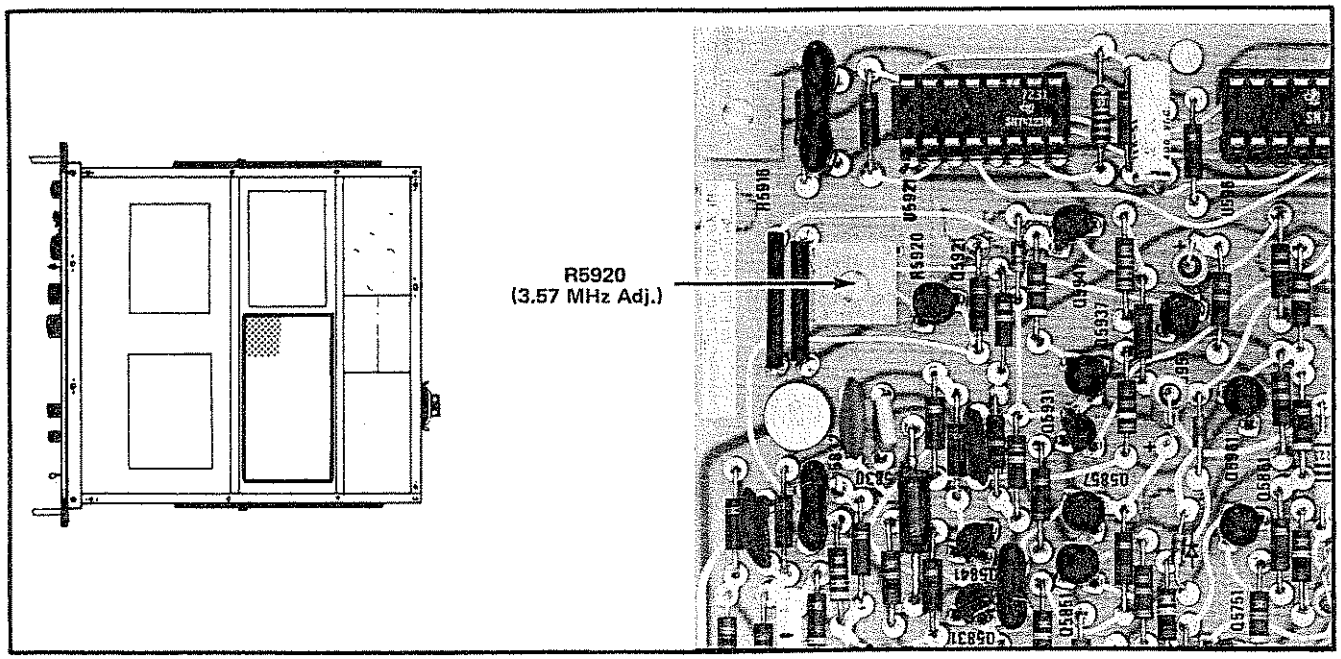


Fig. 4-13. Gen Lock circuit board location of 3.57 MHz frequency adjustment.

b. Set the 1482 Mag to X10. Position the modulated pulse to the center of the graticule.

CHECK—Half Amplitude Duration (HAD) of mod pulse is 1.57 μs within 50 ns, and bar risetime is 1.41 μs within 50 ns.

SELECT—C485 for 1.57 μs HAD within 50 ns.

c. CHECK—Baseline ripple on the bottom of the pulse is 3.5 mV or less.

ADJUST—L415, L435, L455, and L475 (12.5T Filter) for minimum residual subcarrier immediately following the pulse.

ADJUST—R7615 for symmetrical baseline of pulse and bar.

d. CHECK—Amplitude of pulse and bar modulation is from the blanking level to the 100% PEAK WHITE level within 3.5 minor divisions (700 mV within 1%).

ADJUST—R8870 for the chrominance at the bottom of the pulse and bar to end exactly at the blanking level.

ADJUST—R486 for the pulse chrominance to peak at exactly 100% PEAK WHITE (700 mV).

ADJUST—R482 for the bar chrominance to peak at exactly 100% PEAK WHITE (700 mV).

Remove P8490. Set VAR APL to 50%.

CHECK—Luminance components of pulse and bar are 50% PEAK WHITE within 3.5 minor divisions (350 mV within 2%).

Replace P8490. Turn the 145-M U BURST switch ON.

GROUP 6—PULSE AMPLITUDE AND WIDTH

NOTE

See Fig. 4-15 for adjustment and pin connector locations for this group.

1. Check/Adjust 2T PULSE Amplitude and Width

a. Set the FULL FIELD SIG Selector (right) to PULSE & BAR. Set the Mode switch to ALL LINES.

CHECK—2T PULSE amplitude is within 3.5 minor divisions of the BAR amplitude (700 mV within 1%). (Use 1482 Waveform Comparison controls for this measurement.)

b. Set the 1482 for 1.0 Volt Full Scale, Mag to .1 μs/Div. Position the half amplitude point of the 2T PULSE at the horizontal reference graticule line.

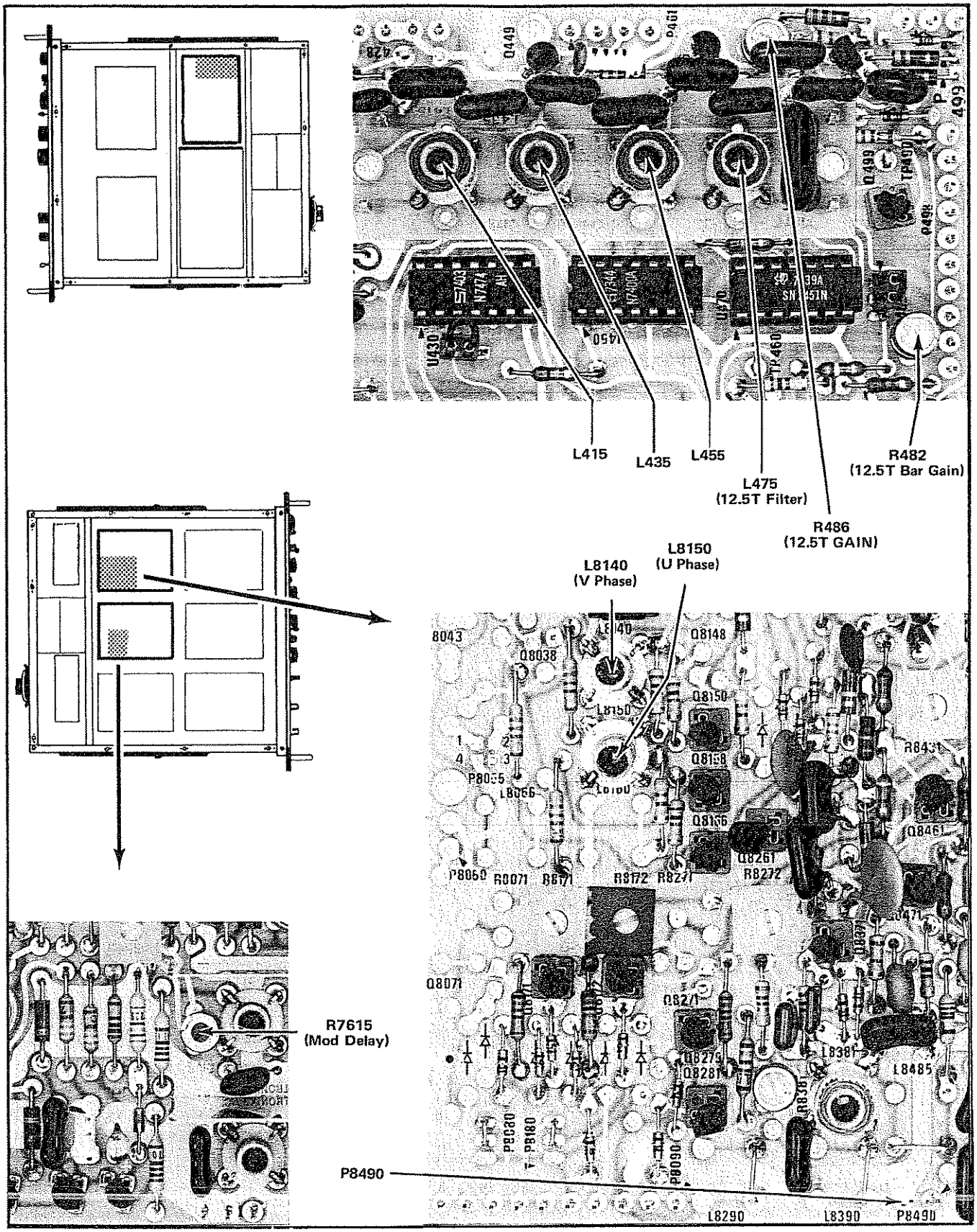


Fig. 4-14. MOD PULSE & BAR adjustments.

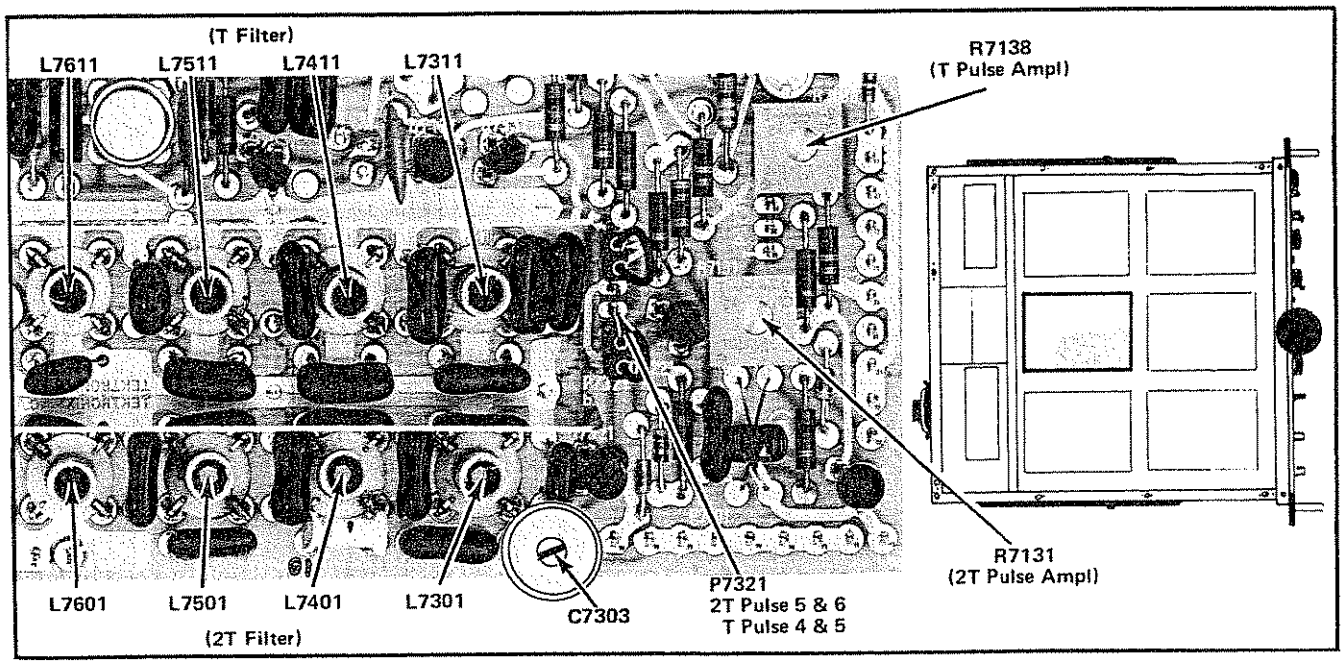


Fig. 4-15. Filter pin connectors and adjustment locations.

CHECK—Half Amplitude Duration is between 212 ns and 288 ns (250 ns within 15%).

Set the 1482 to 0.2 Volt Full Scale.

CHECK—Ringing after the pulse is 1.75 minor divisions or less (0.5% or less).

ADJUST—L7301, L7401, L7501, L7601, and C7303 for a Half Amplitude Duration of 250 ns within 15%, ringing of 0.5% or less, and symmetrical rise and fall times.

ADJUST—R7131 (2T Pulse Amplitude) to match the BAR amplitude exactly.

2. Check/Adjust T PULSE Amplitude and Width

Change the grey connector on P7131 to pins 2 and 3, and the grey connector on P7321 to pins 4 and 5.

CHECK—T PULSE amplitude is within 1% of BAR amplitude, ringing is 1% or less, and Half Amplitude Duration is 125 ns within 15% (106 ns to 144 ns).

ADJUST—L7311, L7411, L7511, and L7611 for a Half Amplitude Duration of 125 ns within 15%, and ringing of 1% or less.

ADJUST—R7138 (T Pulse Ampl) for the T PULSE amplitude to exactly match the BAR amplitude.

Reconnect the grey connectors for a 2T PULSE (P7131-1 & -2; P7321-5 & -6).

3. Check BAR Risetimes

CHECK—BAR risetime is 115 ns within 15% (98 to 132 ns).

Change the violet connector on P7321 to pins 2 and 3.

CHECK—BAR risetime is 230 ns within 15% (195 ns to 265 ns).

Return the violet connector to P7321-4 & -5 (T BAR).

CHECK—BAR tilt is 0.5% or less (3.5 mV or less) in any 10 μs segment.

GROUP 7—MULTIBURST

NOTE

See Fig. 4-17 for adjustment and test point locations.

1. Check/Adjust Harmonics

Connect the 1401A Spectrum Analyzer as in Group 4 Step 3.

Set the FULL FIELD SIG Selector (right) to CCIR-II. Remove P8490.

CHECK—All Multiburst harmonics are lower amplitudes than −40 dB.

ADJUST—C6693, C6788, R6898, and R6977 (MB Harmonics) for minimum harmonics. (−40 dB attenuation or more.)

Replace P8490.

2. Check/Adjust Multiburst Frequencies

Connect a 10X probe from the test oscilloscope input to TP6301. Use the Delay Time Multiplier on the test oscilloscope to check and adjust the Multiburst frequencies according to the following:

Frequency	Test Scope	CHECK	ADJUST
500 kHz	.5 μs/Div	2 cycles in 8.0 Div ±3%	R6304
1.0 MHz	.2 μs/Div	1 cycle in 5.0 Div ±3%	R6202
2.0 MHz	.2 μs/Div	2 cycles in 5.0 Div ±3%	R6314
3.0 MHz	.1 μs/Div	3 cycles in 10.0 Div ±3%	R6324
3.57 MHz		minimum opening on vectorscope (less than 120°)	R6334
4.2 MHz	.1 μs/Div	3 cycles in 7.14 to 7.28 Div (+0, −2%)	R6344

Remove the 10X probe. Recheck harmonics. The harmonics and frequency adjustments are interactive; if either is adjusted, the other must be checked.

3. Check/Adjust for Whole Cycles

Reset the waveform monitor 5 μs/Div and Var in detent.

CHECK—The 500 kHz packet contains at least two complete cycles, and the remaining packets consist of complete sinewaves starting and stopping at the 350 mV reference level.

ADJUST—R7615 (MB Length) for two complete cycles of 500 kHz and complete cycles of the remaining packets.

4. Check/Adjust Multiburst Flatness

a. Set the MULTIBURST AMPLITUDE switch to 350 mV. Set the 1482 to 0.2 Volt Full Scale (calibrated), 2 Field Display, and X50 Mag.

CHECK—Flat tops and bottoms of Multiburst packets are within 1.75 mV (within 0.5%).

ADJUST—R6736 (MB Bandpass) for symmetrical tops and bottoms, and C7463 (350 mV Flatness) for flat tops and bottoms.

b. Set the MULTIBURST AMPLITUDE switch to 700 mV.

CHECK—Flat tops and bottoms of packets are within 3.5 mV (within 0.5%).

ADJUST—C7461 (700 mV Flatness) for flat tops and bottoms.

Recheck the 350 mV flatness, then leave the MULTIBURST AMPLITUDE switch set to 700 mV.

If the packets are not flat, re-do steps 1 through 3 of this group. Adjust for the best compromise between harmonics and flatness.

5. Check/Adjust Multiburst Average Level

Push the vectorscope Y button.

CHECK—The 4.2 MHz level matches the reference level, see Fig. 4-16.

ADJUST—R6673 (MB Centering) to match the level of the 4.2 MHz burst to the reference level.

6. Check/Adjust Multiburst Sync Level

CHECK—Horizontal and vertical sync levels are the same.

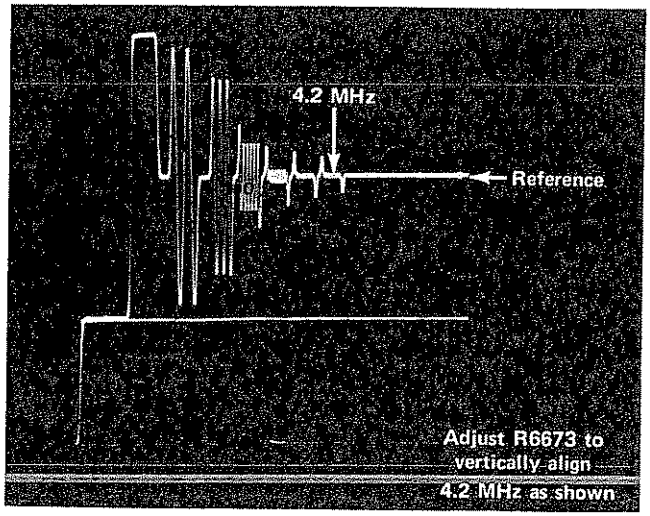


Fig. 4-16. Typical vectorscope display (Y) of Multiburst luminance.

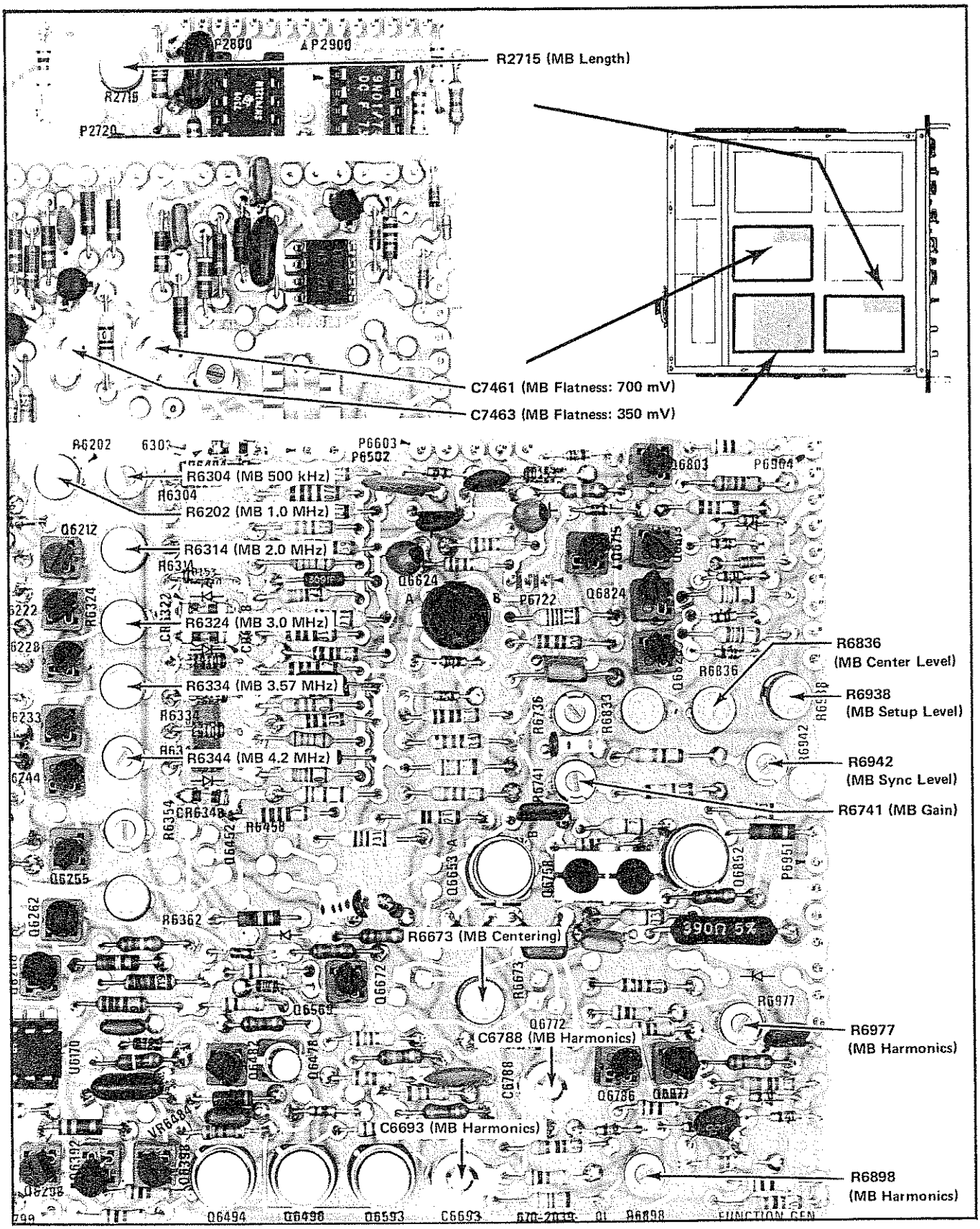


Fig. 4-17. Multiburst adjustment locations.

ADJUST—R6942 (MB Sync Level) to match the horizontal and vertical sync levels.

7. Check/Adjust Multiburst Amplitudes

a. Recheck accuracy of 350 mV pedestal level (R6836) or 350 mV within 5 mV.

CHECK—Amplitude of the 500 kHz packet is from the blanking level to 100% PEAK WHITE within 3.5 minor divisions (700 mV within 1%).

ADJUST—R6741 (MB Gain) for exactly 700 mV, 500 kHz packet.

b. Set the MULTIBURST AMPLITUDE switch to 350 mV.

CHECK—The positive peak of the 500 kHz packet is above the 70% PEAK WHITE level 1.75 major divisions with 1.75 minor divisions, and the negative peak is below the 30% PEAK WHITE level 1.75 major divisions within 1.75 minor divisions (350 mV within 1%).

GROUP 8—FIELD RATE SWEEP GEN

1. Check/Adjust Frequencies

Set the FULL FIELD SIG Selector (Right) to FIELD RATE SWEEP GEN. Set the 1482 to 1.0 Volt Full Scale and 2 Field Display. Push the Var Line Selector button and position the intensified portion of the signal to the first line after the fourth marker with the Line Selector Var control.

Set the 1482 to 10 μs/Div Display and .1 μs/Div Mag.

CHECK—There are 2 complete sinewave cycles in approximately 5 major horizontal divisions (approximately 4 MHz).

ADJUST—R6972 (Field Swp Freq Center), see Fig. 4-18, for two complete cycles in 5 major divisions (4 MHz).

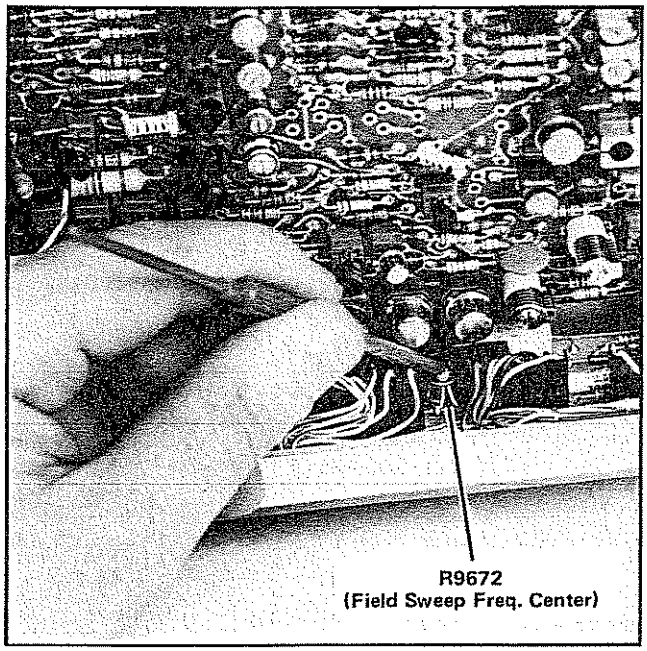


Fig. 4-18. Field Rate Sweep Gen circuit board adjustment location. (CAUTION: Use insulated alignment tool to avoid shorting metal case transistors.)

2. Check Amplitudes

a. Set the 148-M FULL FIELD SIG Mode switch to FULL FIELD SIG & 3 LINES FLAT FIELD: Set the 1482 Mag Off and to 0.2 Volts Full Scale (calibrated).

CHECK—Amplitude of the pedestal matches the 50% PEAK WHITE level within 1.75 minor divisions (350 mV within 1%).

b. Set the 1482 to 2 Field Display.

CHECK—Amplitude of sweep signal is 350 mV peak-to-peak within 1% to 5 MHz (fifth marker). Use test method from Group 7, Step 7b.

c. Set the MULTIBURST AMPLITUDE switch to 700 mV.

CHECK—Amplitude of sweep signal is 700 mV peak-to-peak within 1% to 5 MHz (fifth marker).

@

GROUP 9—FULL FIELD DIFF GAIN & PHASE

1. Check Diff Gain

Set the FULL FIELD SIG switches to LINEARITY, ALL LINES. Set the vectorscope to measure differential gain.

CHECK—Diff gain is 0.5% or less.

2. Check Diff Phase

Set the vectorscope to measure differential phase.

CHECK—Diff phase is 0.2° or less.

GROUP 10—NOISE

1. Check/Adjust Noise Level Accuracy

a. Set the 1482 Line Selector to Dig, Line 14. Set the NOISE switches for −20 dB of inserted noise. Connect (in listed order) from the 148-M NOISE OUT, a 75 Ω coaxial cable, 4.2 MHz Low Pass Filter, 75 Ω Termination, and the RMS Voltmeter.

CHECK—Noise output should be 70 mV rms within 1 dB.

ADJUST—R3260 (Noise Amplitude), see Fig. 4-19, for 70 mV rms.

NOTE

Verification of the NOISE LEVEL switches accuracy requires misadjustment of the noise amplitude.

b. Set R3260 (Noise Amplitude) for a 0 dB reference on the RMS Voltmeter. Use R3270 (Noise Spectrum) if needed.

CHECK—Noise level should be within 1 dB of the front-panel indication.

ADJUST—R3260 (and R3270) for 70 mV rms.

2. Check Half-Line Insertion

Display the PREVIEW OUTPUT signal on the monitor. Set the INSERTION SIGNAL CONTROL switch to PREVIEW.

CHECK—Half-line of noise should be displayed in the middle of the line (NOISE INSERTION) or a full-line of noise pedestal (NOISE DELETION).

3. Check/Adjust Noise Match

a. Connect the video signal source Composite Sync, Burst Flag, PAL Pulse, and Subcarrier to the 148-M respective inputs. Set the SYNC switch to EXT.

b. Connect the NOISE OUT signal to the PROGRAM INPUT. Set the noise pedestal to match the baseline. Insert −20 dB of noise.

CHECK—Noise amplitudes match.

ADJUST—R7561 (Noise Match), see Fig. 4-19, to match the half-line noise amplitude to the PROGRAM LINE noise.

4. Check VARIABLE Pedestal Control

a. Display the FULL FIELD TEST SIGNAL on the monitor. Insert noise, but set the NOISE LEVEL switch to OFF.

CHECK—VAR control range should be from −50 mV to +50 mV (cw) at each pedestal level, except the 50 mV position, which should have range to 14 mV or less.

b. Set the VARIABLE control for minimum amplitude and the PEDESTAL switch to 50 mV.

CHECK—Baseline transients should be 32 mV or less.

5. Check Noise Spectrum

The noise spectrum should be flat to 5 MHz within 6 dB. See Group 4 Step 3 for setup.

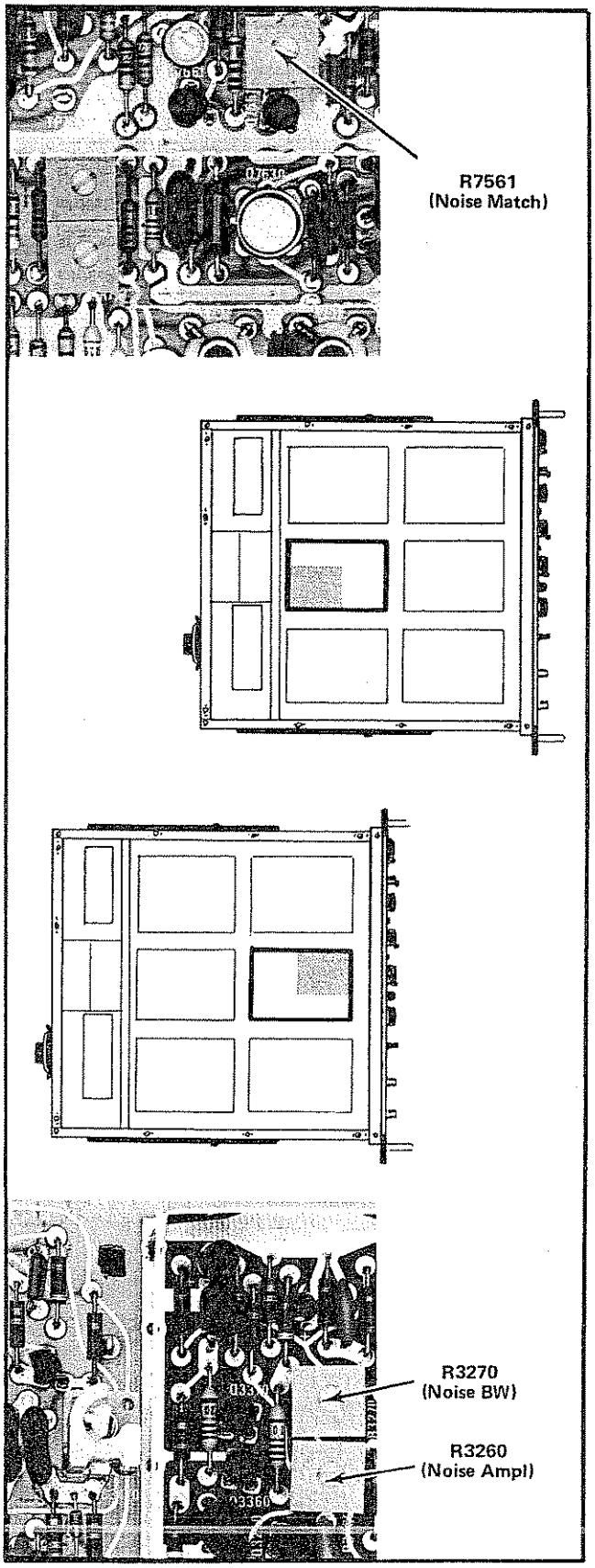


Fig. 4-19. Noise adjustment location.

GROUP 11—GEN LOCK

NOTE

This group of checks requires a video signal source with the ability to shut off its burst and/or sync.

1. Check Light and Output Operation

a. Display the video signal source color bars on the monitor.

CHECK—NOT LOCKED TO PROGRAM light is extinguished and the PROGRAM light should be lit. There should be VITS.

b. Turn off the video signal source sync.

CHECK—NOT LOCKED (red) light is lit; the PROGRAM lamp should be lit. There should be no 148-M VITS. There should be no subcarrier or composite sync outputs from the 148-M.

c. Turn the video signal source sync on and the U burst off.

CHECK—PROGRAM light should be lit. There should be VITS. There should be composite sync output, but no subcarrier output.

d. Turn the video signal source U burst on.

CHECK—There should be a subcarrier output.

3. Disconnect the video signal source.

CHECK—Loss of 148-M VITS and that the 148-M Full-Field signal is on PROGRAM OUT LINE signal, in PROGRAM mode.

CHECK—Burst is present on the Full-Field signal.

2. Check INT/EXT SYNC Mode

a. Connect appropriate 2 V signals from the video signal source to the COMP SYNC, BURST FLAG, PAL PULSE, and SUBCARRIER INPUTS.

CHECK—TP5698, see Fig. 4-20, for 2 pulses, matching in time and width, but with an amplitude ratio of about 5:6.

b. Set the SYNC switch to EXT.

CHECK—TP5698 for 2 pulses with some similarity to the pulses in INT mode.

ADJUST—L9710 (135° Phase) for maximum pulse amplitude; C9719 (225° Phase) to match pulse amplitude and L9772 (Subc Peaking) for flat pulse tops and similarity to the pulses in INT mode.

NOTE

The adjustments for this step are on the small circuit board just forward of the external sync input connectors.

c. Remove, then reconnect, the input signals one at a time.

CHECK—Removal of any of the 4 external sync signals will remove the pulses from TP5698.

d. Leave all external signals connected and set the SYNC switch in EXT.

3. Check Sync Stripper Operation

a. Connect a 10X probe to TP5282.

CHECK—Composite sync amplitude should be between 0.8 and 1.2 V.

b. Connect the probe to plug P5970, pins 2, 3, or 4.

CHECK—Composite sync amplitude should be between 5.0 and 6.0 V.

c. Set the SYNC switch to INT.

CHECK—	
P5970	comp sync 5.0 to 6.0 V
TP5282	comp sync 0.8 to 1.2 V

4. Check Chroma AGC Ratio

NOTE

R5920 (3.57 MHz Adj) is adjusted to make the chroma change easier to see. If it is adjusted, reset it using Step 5.

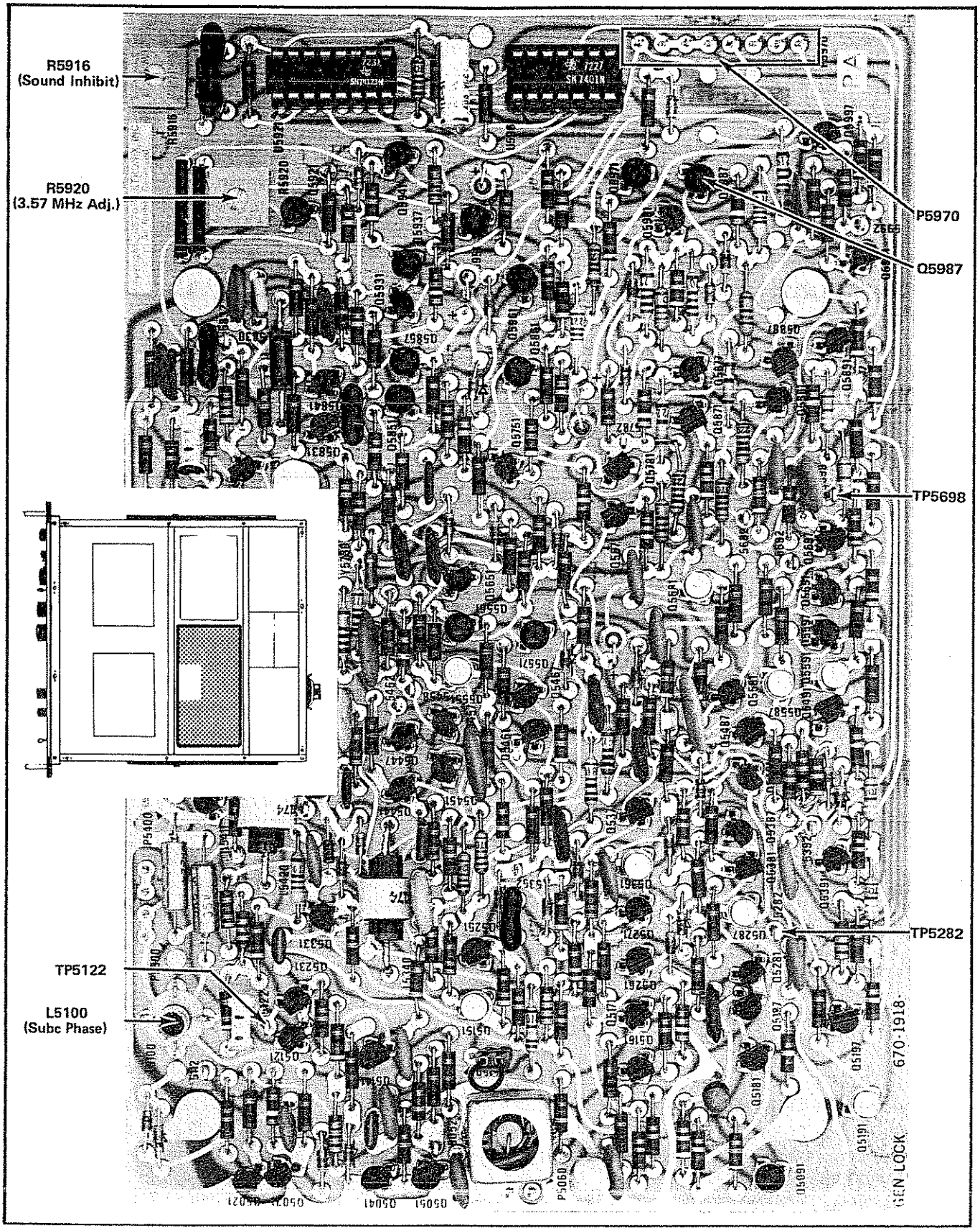


Fig. 4-20. Gen Lock test point, pin connector, and adjustment.

a. Connect a 10X probe to TP5332. Remove Q5987 and adjust R5920 for a chroma variation of about once a second.

CHECK—Burst amplitude ratio should not vary more than 1:1.6.

b. Replace Q5987.

5. Adjust 3.57 MHz Frequency

a. Monitor the Full-Field signal on the vectorscope. Turn the video signal source U burst off.

ADJUST—R5920 (3.57 MHz Adj) for minimum vector rotation. 3.57561149 MHz ±25 Hz.

b. Turn the video signal source U burst on.

6. Check/Adjust Sound Inhibit

Connect a 10X probe to P5970, pins 2, 3, or 4. Display the trailing edge of sync on the test oscilloscope.

CHECK—Sound Inhibit pulse for a trailing edge 275 ns (250 to 300 ns) before the trailing edge of sync.

NOTE

This is a very low writing rate display. If the Sound Inhibit pulse trailing edge cannot be seen, display the signal at U5967B, pin 6, on the test oscilloscope and note its position. Move the probe to U5967B, pin 5, and check for 275 ns between the two signals.

ADJUST—R5916 (Sound Inhibit) for a trailing edge of 275 ns before the trailing edge of sync.

GROUP 12—VITS INSERTION, DIFF PHASE AND DIFF GAIN

1. Check/Adjust PROGRAM LINE OUT

a. Set the video signal source for a full-field modulated staircase test signal. Display the PROGRAM OUTPUT LINE signal on the monitor and vectorscope.

b. Set the vectorscope to measure differential phase.

CHECK—Diff Phase should be 0.15° or less.

c. Set the vectorscope to measure differential gain.

CHECK—Diff Gain should be 0.2% or less.

d. Set the VAR LEVEL to max. Repeat the checks in 1b and 1c except:

CHECK—Diff Phase should be 0.3° or less.

CHECK—Diff Gain should be 0.4% or less.

Set VAR LEVEL controls for unity gain.

2. Check PREVIEW OUTPUTS

Display the PREVIEW OUT signal on the monitor. Repeat the checks in Step 1b and c except:

CHECK—Diff Gain should be 0.4% or less.

CHECK—Diff Phase should be 0.3° or less.

3. Check Programming

a. Display the PROGRAM LINE OUT SIGNAL on the monitor.

CHECK—VITS exist as indicated in Table 4-3 VITS and FF LOGIC.

b. Using Table 4-3 as a guide, check that all internal connectors (as factory connected) are in the appropriate position.

TABLE 4-3

Factory Connected Internal Changes

Board Pin No.	Plug	Pins Nos.	Function
SUBC & SYNC			
P430	Violet	2 & 3 (Outbd)	Alt & 6 Lines Flat Field
P482	Red	1 & 2 (Outbd)	FF Burst-Insert
GEN LOCK			
P5150	Blue	2 & 3 (Fwd)	Subc Lock-CW
OUTPUT			
P7131	Gray	1 & 2 (Outbd)	2T Pulse
P7321	Violet	1 & 2 (Inbd)	T Bar
P7321	Gray	5 & 6 (Outbd)	2T Pulse
VITS & FF LOGIC			
CCIR-I	Brown Diode	F1, F3	
	Brown	17,280	
SIG-III	Red Diode	F1, F3	
	Red	16,279	
CCIR-II	Orange Diode	F2, F4	
	Orange	17,280	
MOD PULSE & BAR	Yellow Diode	F2, F4	
	Yellow	16,279	
EXT, LIN, or P & B	Green Diode	Both	
	Green Diode	15,278	
NOISE	Blue Diode	Both	
	Blue	14,277	
EXT, LIN, P & B			
P4060	Green	2 & 3 (Inbd)	LINEARITY

GROUP 13—VITS INSERTION

NOTE

The adjustments and checks in this group, except Step 1, require that any errors in the full-field signal be noted or adjusted out.

Display the vertical interval of the rear-panel FULL FIELD TEST SIGNAL on the monitor. If the back proch of the CCIR-II and Pulse & Bar signals are not superimposed with the blanking level they will show up as unwanted VITS pedestal error (Steps 2b and 3b).

Small errors may be adjusted out without further recalibration. Adjust R6942 (MB Sync Level), see Fig. 4-17; adjust R7453 (P & B Sync Level), see Fig. 4-22.

The full-field signal output dc level should be close to 0 V. Adjust R7733 (DC Level), see Fig. 4-10.

All adjustments, except step 1, are shown in Fig. 4-21.

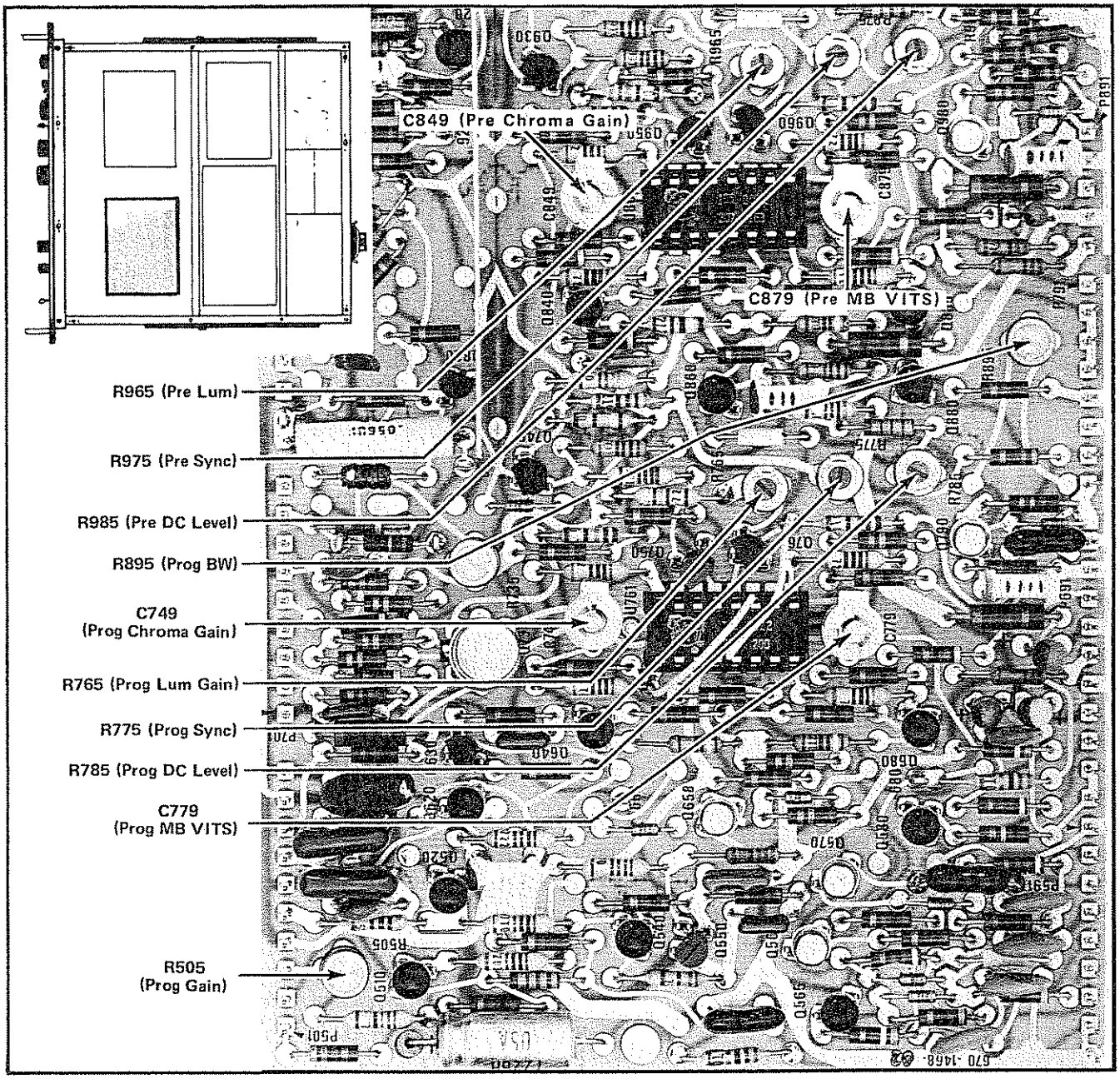


Fig. 4-21. VITS Insertion adjustment.

1. Check/Adjust Auxiliary Sync Level

Display the vertical interval of the PREVIEW OUT signal on the monitor.

CHECK—Display should be similar to the display shown in Fig. 4-22.

ADJUST—R7361 (Aux Sync Level), see Fig. 4-22, to match the levels as shown in Fig. 4-23.

2. Check/Adjust PROGRAM OUTPUT LINE

a. Display the vertical interval of the PROGRAM OUTPUT LINE signal on the monitor. Connect appropriate signals from the video signal source to the COMP SYNC, BURST FLAG, PAL PULSE, and SUBCARRIER INPUTS. Connect a cable from the rear-panel FULL FIELD TEST SIGNAL to the PROGRAM INPUT.

b. Set the FULL FIELD SIG switch to FLAT FIELD and the APL switches to 100. (Set sync switch to EXT.)

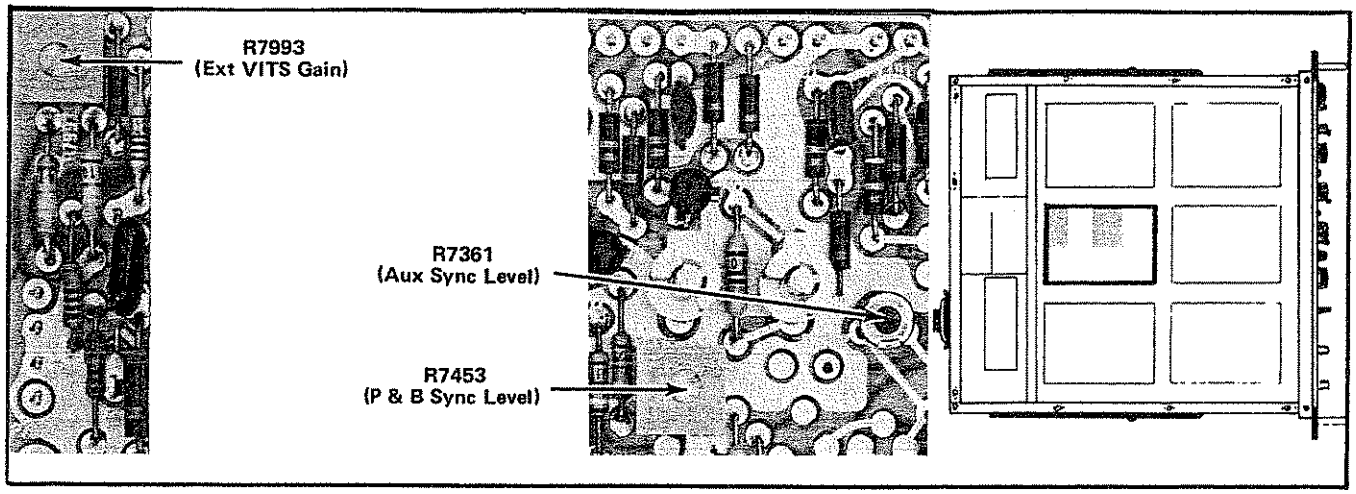


Fig. 4-22. Auxiliary Sync level and external VITS gain adjustment location.

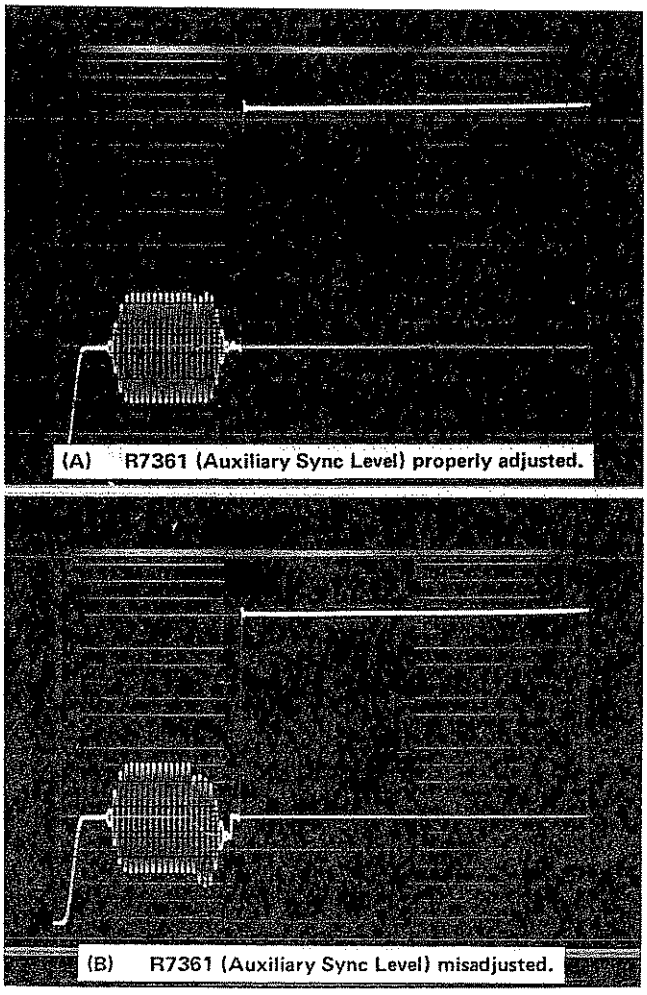


Fig. 4-23. Typical waveform monitor display used to check or adjust auxiliary sync level.

CHECK—VITS blanking level (unwanted VITS pedestal) should be within 5 mV of the blanking level for the non-inserted lines.

ADJUST—R775 (Prog Sync Level) to match the blanking levels.

CHECK—Blanking level (dc) should not change more than 50 mV when switching the INSERTION CONTROL between PROGRAM and BYPASS.

ADJUST—R785 (Prog DC Level) so that no blanking level (dc) change occurs when switching between PROGRAM and BYPASS.

NOTE

The blanking level seen in the BYPASS mode is not necessarily 0 volt, but rather the blanking level of the full-field signal.

c. Switch the INSERTION CONTROL between PROGRAM, PREVIEW, and BYPASS.

CHECK—Blanking level (dc) of the display should not change between any mode. In addition, there should be no amplitude change of the VITS or full-field signals when switching between PROGRAM, PREVIEW, and BYPASS.

ADJUST—R505 (Prog Gain) so that no amplitude change of the insertion signal occurs while switching between PROGRAM and AUXILIARY.

ADJUST—R765 (Prog Lum Gain) so that no amplitude change of the full-field signal occurs while switching between PROGRAM and BYPASS.

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d. Step b and c interact; repeat as necessary.

e. Set the FULL FIELD SIG switch to SIG-III. Switch the INSERTION CONTROL between BYPASS and PROGRAM.

CHECK—2T Pulse to Bar; 100% within 0.25% (1.8 mV).

12.5T Pulse to Bar; 100% within 0.5% (3.5 mV).

12.5T baseline ripple; should be 0.5% or less (3.5 mV).

3. Check/Adjust PREVIEW MONITOR OUT

a. Note the dc level of the PROGRAM OUTPUT LINE blanking level.

b. Display the PREVIEW OUTPUT signal on the test oscilloscope. Set the INSERTION CONTROL switch to PREVIEW.

CHECK—Preview blanking level (dc) should be within 50 mV of the level noted in part a.

ADJUST—R975 (Pre Sync Level) so that the VITS blanking level matches the preview blanking level.

ADJUST—R985 (Pre DC Level) so that the preview blanking level matches the program blanking level. (0 volt plus any full-field blanking level error.)

c. Change the cable to display the PROGRAM OUTPUT LINE signal on the test oscilloscope. Note the overall amplitude of the signal. Change the cable to display the PREVIEW OUTPUT signal.

CHECK—Preview signal overall amplitude should match the program signal overall amplitude within 1%.

ADJUST—R965 (Pre Gain) to match the preview signal to the program signal.

d. Steps b and c interact; repeat as necessary.

e. Change the cable to display the other PREVIEW OUTPUT signal.

CHECK—Preview signals should be the same amplitude.

4. Check Multiburst Flatness

a. Set the FULL FIELD SIG switch to CCIR-II. Switch the INSERTION CONTROL between PREVIEW and BYPASS.

CHECK—Tilt on preview multiburst signal (as measured between the first and last burst packets) should match the tilt of the full-field multiburst signal within 1%.

Repeat check for the multiburst signal inserted in the vertical interval.

b. Display the PROGRAM SIGNAL on the test oscilloscope. Switch the INSERTION CONTROL between PROGRAM and BYPASS.

CHECK—Tilt on program multiburst signal should match the tilt of the full-field multiburst signal within 1%.

Repeat check for the multiburst signal inserted in the vertical interval.

5. Check INSERT SUBCARRIER PHASE

a. Connect the video signal source to the PROGRAM INPUT. Display the PROGRAM OUTPUT signal on the vectorscope.

CHECK—INSERT SUBCARRIER PHASE control range is approximately 28°; range should be at least 5° on either side of 180°.

b. Set the INSERT SUBCARRIER PHASE control to set the VITS vectors to 180°. Display the PREVIEW signal on the vectorscope.

CHECK—VITS vectors should be at 180° (no phase error).

6. Check/Adjust Multiburst Flatness, Subcarrier Phase, and Pulse to Bar Ratios

NOTE

Adjustments in Step 6 affect the checks made in Step 2e, Steps 4a and 4b, and Steps 5a and 5b. After making the adjustments, repeat these checks.

a. Disconnect the video signal source from the PROGRAM INPUT. Display the PROGRAM signal on the test oscilloscope.

CHECK—TTL transients should be no more than 5 mV peak-to-peak.

NOTE

If the writing rate of the test oscilloscope is not sufficient to display these transients, do not adjust R780 or C779 at this time, but go to step c.

b. Preset C779 (Prog MB VITS) for minimum capacitance.

ADJUST—R780 (Program Bandwidth) for minimum TTL transients.

c. Connect the FULL FIELD TEST SIGNAL to the PROGRAM INPUT. Set the FULL FIELD SIG switch to CCIR-II.

ADJUST—C779 (Prog MB VITS) so that the tilt of the full-field multiburst insertion signals are the same in either the PROGRAM or the BYPASS position of the INSERTION CONTROL switch.

ADJUST—C749 (Program Chroma Gain) so that the tilt of the full-field multiburst VITS are the same in either the PROGRAM or the BYPASS position of the INSERTION CONTROL switch.

d. Set the FULL FIELD SIG switch to SIG-III.

ADJUST—R780 (Program Bandwidth) so that the pulse and bar amplitudes are the same in either the PROGRAM or the BYPASS position of the INSERTION CONTROL switch.

e. Steps c and d interact; repeat as necessary.

f. Check that the following signals are within the listed tolerances as the INSERTION CONTROL is switched between BYPASS and PROGRAM.

CHECK—Program signal to full-field signal as follows:

MB VITS; within 1%

Chroma Gain; within 1%.

2T Pulse to Bar ratio; 100% within 0.25% (1.8 mV).

12.5T Pulse to Bar ratio; 100% within 0.5% (3.5 mV).

12.5T baseline ripple change; 0.5% or less (3.5 mV).

g. Connect the Signal Generator through the 50 Ω to 75 Ω Min Loss Atten to the 148-M PROGRAM INPUT. Display the PROGRAM OUTPUT on the test oscilloscope. Sync the 148-M externally. Set the Signal Generator for 500 mV of 5 MHz as observed with the 148-M in the BYPASS mode.

CHECK—Test Oscilloscope display should not change by more than ±1% to 5 MHz when the 148-M mode is changed to PROGRAM.

7. Check/Adjust INSERT SUBCARRIER PHASE

a. Connect the video signal source to the PROGRAM INPUT. Set the SYNC SOURCE switch to INT. Display the PROGRAM SIGNAL on the vectorscope.

CHECK—INSERT SUBCARRIER PHASE control range is approximately 28°; range is at least 5° on either side of 180°.

ADJUST—L5100 (VITS Phase) so that the INSERT SUBCARRIER PHASE control range is at least 5° on either side of 180°.

b. Rotate the INSERT SUBCARRIER PHASE control to set the VITS vector to 180°.

c. Display the PREVIEW OUTPUT signal on the vectorscope.

CHECK—VITS vector should be at 180°.

ADJUST—C849 (Preview Flatness) to set the VITS vector to 180°.

8. Check/Adjust PREVIEW OUTPUT

a. Set the SYNC SOURCE switch to EXT. Connect the rear-panel FULL FIELD TEST SIGNAL to the PROGRAM LINE IN.

b. Display the PREVIEW OUTPUT signal on the monitor and vectorscope. Set the FULL FIELD SIG switch to CCIR-II.

CHECK—Tilt of the full-field multiburst insertion test signals are within 1% in either the PREVIEW or the BYPASS position of the INSERTION CONTROL switch.

ADJUST—C879 (Pre MB VITS) so that the tilt of the full-field multiburst insertion test signals are within 1% in either the PREVIEW or the BYPASS position of the INSERTION CONTROL switch.

CHECK—Tilt of the full-field multiburst signals are within 1% in either the PREVIEW or the BYPASS position of the INSERTION CONTROL switch.

9. Check/Adjust Unity Gain

a. Display the FULL FIELD TEST SIGNAL OUT on the 1482. Set the FULL FIELD SIG switch to FLAT FIELD and the APL switches to 100.

b. Push the Oper, Cal, and Back Porch buttons. Determine, then note the peak-to-peak amplitude of the FLAT FIELD test signal.

c. Connect the FULL FIELD TEST SIGNAL to the PROGRAM INPUT. Connect the PROGRAM OUTPUT to the 1482.

CHECK—PROGRAM OUTPUT signal amplitude should be within 1% of that noted in part b.

ADJUST—R765 (Prog Lum Gain) so that the PROGRAM OUTPUT signal amplitude is the same as noted in part b.

d. Connect the PREVIEW OUTPUT to the 1482.

CHECK—PREVIEW OUTPUT signal amplitude should be within 1% of that noted in part b.

ADJUST—R965 (Pre Lum Gain) so that the PREVIEW OUTPUT signal amplitude is the same as noted in part b.

10. Check Waveform Tilt, Program, and Preview

a. Connect the front-panel FULL FIELD TEST SIGNAL to the 1482 A Input. Connect the rear-panel FULL FIELD TEST SIGNAL OUT to the 1482 B Input. Set the FULL FIELD SIG switch to PULSE & BAR. Obtain a differential display and note any tilt (low frequency slope) of the 26 μs bar.

b. Connect the rear-panel FULL FIELD TEST SIGNAL to the PROGRAM INPUT. Connect the PROGRAM OUTPUT to the 1482 B Input.

CHECK—Tilt should be within 0.5% of that noted in part a (3.6 mV or less).

c. Connect the PREVIEW OUTPUT to the 1482 B Input.

CHECK—Tilt should be within 0.5% of that noted in part a (3.6 mV or less).

d. Connect the rear-panel FULL FIELD TEST SIGNAL to the 1482 B Input. Set the FULL FIELD SIG switch to FIELD SQ WAVE. Obtain a differential display of the field square-wave signal and note any tilt error.

e. Connect the rear-panel FULL FIELD TEST SIGNAL to the PROGRAM INPUT. Connect the PROGRAM OUTPUT to the 1482 B Input.

CHECK—Tilt change should be within 0.5% (3.6 mV or less).

f. Connect the PREVIEW OUTPUT to the 1482 B Input.

CHECK—Tilt change should be within 0.5% (3.6 mV or less), referenced to the full-field signal.

11. Check AUXILIARY PEDESTAL

a. Display the PREVIEW OUTPUT signal on the monitor. Set the INSERTION CONTROL switch to AUXILIARY.

CHECK—AUXILIARY PEDESTAL control range should be from $\leqslant$70 mV to $\geqslant$630 mV.

b. Connect a 0.1 to 0.5 V signal to the AUX IN input (the video signal source subcarrier signal via a X10 attenuator is acceptable).

CHECK—External signal rides on the auxiliary pedestal; it should not affect sync or VITS.

12. Check UNITY GAIN/VAR & LEVEL

Set the INSERTION CONTROL switch to PROGRAM. Set the UNITY GAIN/VAR switch to VAR. Display the PROGRAM OUTPUT signal on the monitor.

CHECK—LEVEL control range should be from 70% (or less) to 140% (or more).

13. Check PROGRAM OUTPUT Aberrations

a. Disconnect the video signal source from the PROGRAM INPUT. Externally sync the 148-M with Burst Flag, PAL Pulse, Subcarrier, and Comp Sync from the video signal source. Connect the PROGRAM OUTPUT to the test oscilloscope.

CHECK—Residual subcarrier, should be −60 dB (0.7 mV) or less, on lines 11 through 16 and lines 20, 21, and 22.

b. Connect a 4.2 MHz Low Pass Filter in series with the PROGRAM OUTPUT signal.

CHECK—All blanking lines and inactive parts of lines. Except for the Insertion Test Signals there should be no signal greater than −40 dB (7.0 mV).

c. CHECK—Active parts of lines for spurious signals, should be no greater than −60 dB (0.7 mV).

d. CHECK—Crosstalk. Rotate the FULL FIELD SIG switch. Signal change (crosstalk) should not exceed:

−70 dB (0.22 mV) for 2T Pulse,

−60 dB (0.7 mV) for subcarrier (CCIR-II),

−60 dB (0.7 mV) for all other Full Field signals.

e. Connect a 4.2 MHz Weighting Network in series with the PROGRAM OUTPUT and the 4.2 MHz Low Pass Filter.

CHECK—Hum and power line related transients, should be no greater than −60 dB (0.7 mV).

f. Connect a 75 Ω termination to the PROGRAM INPUT. Connect the PROGRAM OUTPUT through a 4.2 MHz Weighting Network, 4.2 MHz Low Pass Filter and 75 Ω termination to the RMS Voltmeter.

CHECK—Random noise output, should be no greater than −75 dB (0.14 mV).

g. Connect an external composite video signal which contains a Pulse and Bar inserted between lines 10 and 18 of the vertical interval. Remove the two diode jumpers from the OFF line, ALL FIELD selection jumpers. Add diode jumpers to both field selector rows.

CHECK—Incoming VITS should be deleted as follows:

2T Pulse	−70 dB
Subcarrier	−60 dB

GROUP 14—TIMING

1. Check INSERT DELAY Range

a. Display the FULL FIELD TEST SIGNAL on the 1482. Select a reference point on the signal and vary the INSERT DELAY control.

CHECK—Range of control should be greater than 1 μs.

b. Leave the control at electrical center.

2. Check/Adjust Pulse Width

Observe the sync pulse.

CHECK—Timing accuracy as given below.

Fig. 4-24	Component	Timing
A	serration width	4.3 to 4.7 μs
B	sync width	4.66 to 4.76 μs
C	equalizer width	2.3 to 2.5 μs

ADJUST—Timing accuracy as given below.

Fig. 4-25	Timing
R356 (Serration Width)	4.5 μs
R351 (Sync Width)	4.71 μs
R251 (Equalizer Width)	2.4 μs

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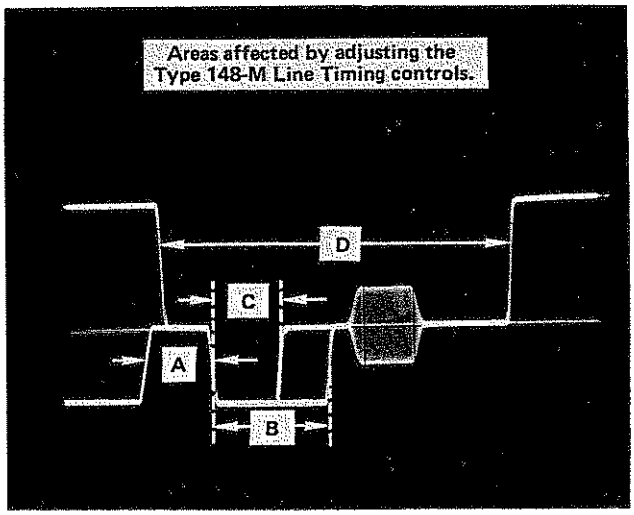

Fig. 4-24. Areas affected by timing adjustments.

3. Check/Adjust Sync Delay

a. Display the vertical interval of the PROGRAM OUTPUT signal on the 1482. INSERT DELAY control should be at electrical center. Observe the sync pulse of the noise, multiburst, or color bar insertion signal.

CHECK—Timing, as shown in Fig. 4-24D, should be 11.1 μs within 0.25 μs.

ADJUST—R1978 (Sync Delay), see Fig. 4-25, for 11.1 μs.

4. Check Bypass Relay

Set the 148-M POWER switch to OFF.

CHECK—Test oscilloscope display should be the video signal source with no VITS inserted.

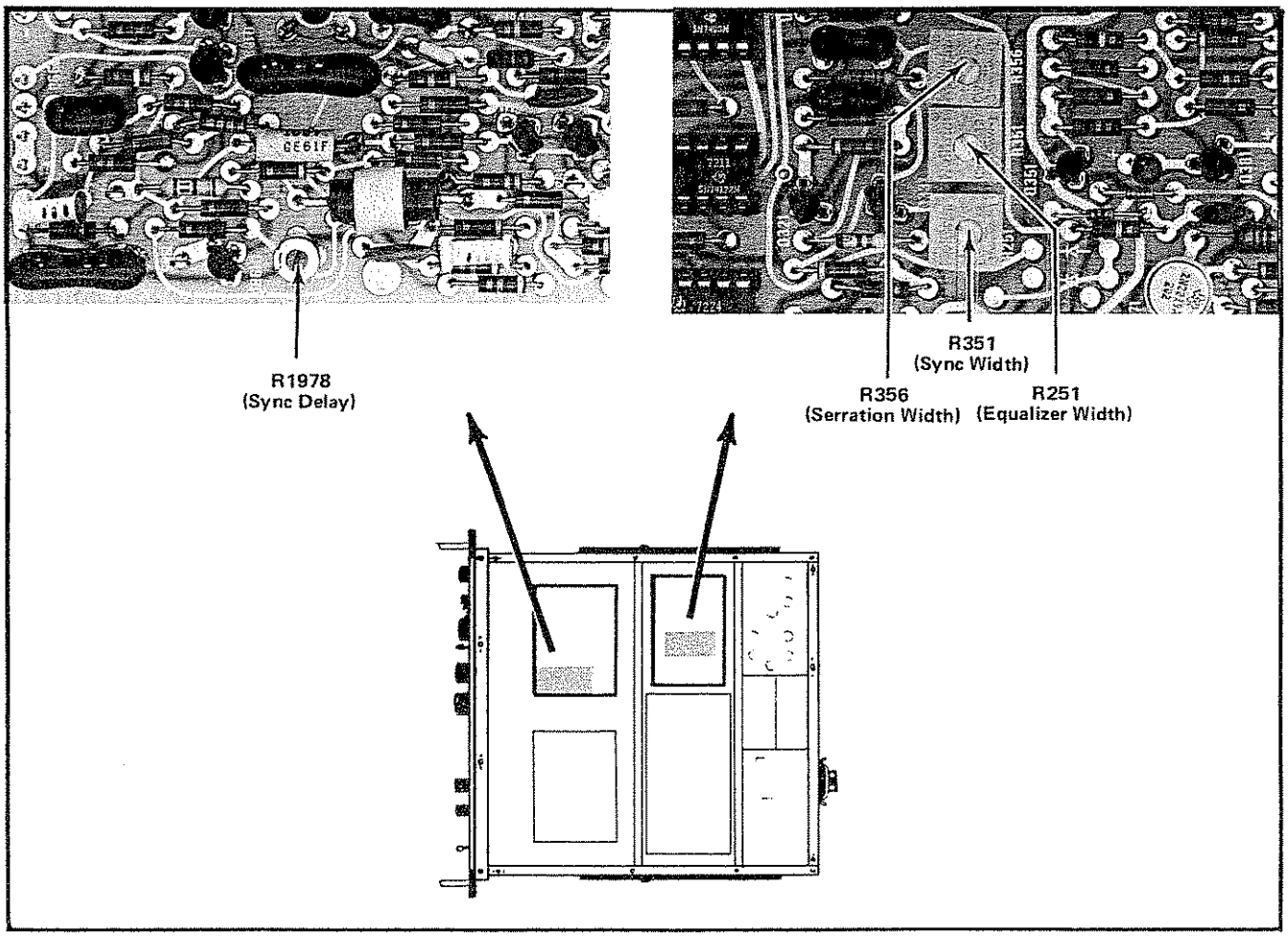

Fig. 4-25. Timing adjustment locations.

5. Check ALT and FULL FIELD SIG & 3 LINES FLAT FIELD Operation

a. Display a field of 148-M FULL FIELD signal, magnified 10 times. Set the Mode switch to ALT.

Display should be the signal selected by the right FULL FIELD SIG switch followed by that selected by the left FULL FIELD SIG switch alternately for the entire field.

b. Set the Mode switch to FULL FIELD SIG & 3 LINES FLAT FIELD.

CHECK—Display should be the signal selected by the right FULL FIELD SIG switch followed by 3 lines of flat field for the entire field.

Return the Mode switch to ALL LINES.

GROUP 15—OPTIONAL CHECKS

This group of checks has been performed at the factory and may not be desired by the user.

1. POWER SUPPLY REGULATION

Requires a variable autotransformer.

Repeat the checks given in GROUP 1, Steps 1 and 2, while varying the autotransformer over the line voltage range listed for the LINE VOLTS selector switch position being used.

2. ERASE

Switch to AUX and verify the video signal source puts VITS on lines 10 through 18, both fields.

Remove the 2 black diode jumpers from the OFF line. Remove all field selection jumpers.

Add a black diode jumper (cathode inboard) to both fields and check for erase on both fields, lines 10 through 18. Check line for signal attenuation in ERASE mode, active line area. Use 4.2 MHz Low Pass Filter.

Move jumper to F2, F4 and check for erase on F2, F4, but not F1, F3. Repeat for F1, F3; but not F2, F4.

Check that OFF does not erase.

3. RETURN LOSS

Requires a return loss bridge, constant amplitude signal generator and a minimum loss attenuator. See Test Equipment Used list, item 15. This is to be used in conjunction with the return loss bridge instruction manual.

a. Connect the sync signal from the video signal source to their respective inputs. Set the SYNC SOURCE switch to EXT. Externally trigger the test oscilloscope from composite sync.

b. Balance the bridge.

c. Check return loss with the POWER switch OFF and the PROGRAM OUTPUT connector terminated with the return loss bridge termination.

CHECK—Return Loss should be at least −30 dB (7.9 mV) from 50 kHz to 5 MHz.

d. Turn the POWER switch ON.

CHECK—Return loss as follows:

PROGRAM OUTPUT LINE	−30 dB to 5 MHz (≤7.9 mV).
PROGRAM MONITOR	−30 dB to 5 MHz (≤7.9 mV)
PREVIEW OUTPUT (both)	−30 dB to 5 MHz (≤7.9 mV)
FULL FIELD OUT (rear)	−34 dB to 5 MHz (≤5 mV)
COMPOSITE SYNC	−30 dB to 3.6 MHz (≤7.9 mV)
EXT VITS INPUT	−30 dB to 5 MHz (≤7.9 mV)
AUX IN	−30 dB to 5 MHz (≤7.9 mV)
NOISE OUT (LEVEL-off)	−30 dB to 5 MHz (≤7.9 mV)
FULL FIELD OUT (front)	−34 dB to 5MHz (≤5 mV)

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4. EXT VITS GAIN

Requires the video signal source VITS amplitude be set to the full-field amplitude or the difference between the two noted. The VITS Insertion board must be programmed to insert an external VITS.

Connect the rear-panel FULL FIELD SIGNAL to the PROGRAM INPUT. Connect the video signal source comp video to the EXT VITS IN. Connect the video signal source signals required for external sync to the 148-M. Set the SYNC switch to EXT. Set the signal to insert a modulated staircase VITS on line 15, field 1 and program the 148-M for it (P4060-1 & 2). Display the VITS area of the PROGRAM OUTPUT signal on the monitor.

Adjust R7993 (Ext VITS Gain), see Fig. 4-22, to match the external VITS amplitude to the COLOR BAR VITS amplitude.

Display the PROGRAM OUTPUT signal on the vectorscope. Set the vectorscope to measure differential gain, then differential phase on line 15, field 1 & 3.

Check Ext VITS amplifier diff gain $\leqslant$0.2%, and diff phase $\leqslant$0.15°.

WARNING

During rackmount installation, interchanging the left and right slide-out track assemblies defeats the extension stop (safety latch) feature of the tracks. Equipment could, when extended, come out of the slides and fall from the rack, possibly causing personal injury and equipment damage.

When mounting the supplied slide-out tracks, inspect both assemblies to find the LH (left hand) and RH (right hand) designations to determine correct placement. Install the LH assembly to your left side as you face the front of the rack and install the RH assembly to your right side. Refer to the rackmounting instructions in this manual for complete information.

RACKMOUNTING

RACKMOUNTING INSTRUCTIONS

Mounting Methods (Figs. 5-1, 5-2, 5-5 and 5-6)

The instruments will fit most commercial consoles and most 19-inch wide racks whose front and rear rail holes conform to Universal, EIA, RETMA and Western Electric hole spacing.

Fig. 5-1 shows the instrument installed in a cabinet-type rack with 1 3/4-inch wide slide-out tracks for a non-tilt installation. The instrument is secured into the rack by means of four captive thumb screws. When the thumb screws on the front panel are loosened, the instrument can be pulled out of the rack like a drawer to its fully extended position (see Fig. 5-2). This position permits many routine maintenance functions to be performed without completely removing the instrument from the rack.

The slide-out tracks easily mount to the cabinet rack front and rear vertical mounting rails if the inside distance between the front and rear rails is within 10 1/2 to 24 1/2 inches. Some means of support (for example, make extensions for the rear mounting brackets) is needed for the rear ends of the slide-out tracks if the tracks are going to be installed in a cabinet rack whose inside dimension between front and rear rails is not the proper distance (10 1/2 inches to 24 1/2 inches).

Instrument Dimension

The last page in this section shows dimensional drawings exclusive of the power cord and cables.

Width—A standard 19-inch rack may be used. The dimension or opening between the front rails must be at least 17 5/8 inches (see Fig. 5-2) for a cabinet rack in which the front lip of the stationary section is mounted behind an untapped front rail as shown in the right-hand illustration of Fig. 5-6. This dimension allows room on each side of the instrument for the slide-out tracks to operate so the instrument can move freely in and out of the rack.

Depth—For proper circulation of cooling air, allow at least 2 inches clearance behind the rear of the instrument and any enclosure on the rack (see dimensional drawing). If it is sometimes necessary or desirable to operate the generator in the fully extended position, use cables that are long enough to reach from the instrument to the location where the signal(s) is to be applied.

Rackmounting in a Cabinet Rack

General Information—The slide-out-tracks for the instrument consists of two assemblies, one for the left side of the instrument and one for the right side. Each assembly consists of three sections as illustrated in Fig. 5-3. The stationary section attaches to the front and rear rails of the rack with inside dimensions as indicated in Fig. 5-2; the chassis section attaches to the instrument and is installed at the factory; the intermediate section fits between the other two sections to allow the instrument to be fully extended out of the rack.

The small hardware components included with the slide-out track assemblies are shown in Fig. 5-4. The hardware shown in Fig. 5-4 is used to mount the slide-out tracks to the rack rails having this compatiblity.

a. Front and rear rail holes must be large enough to allow inserting a 10-32 screw through the rail mounting holes (see Fig. 5-6).

b. Front rail holes may have already been countersunk prior to this installation.

Because of the compatibility given in (b), there will be some screws left over.

The stationary and intermediate sections for both sides of the rack are shipped as a matched set and should not be separated. The matched sets for both sides including hardware are marked 351-0195-00 on the package. To identify the assemblies, note that the automatic latch and intermediate section stop are located near the top of the matched sets when they are properly mated to the chassis sections as shown in Fig. 5-3.

Mounting Procedure—Use the following procedure to mount both sets. See Figs. 5-5 and 5-6 for installation details.

1. To mount the instrument directly above or below another instrument in the cabinet rack, select the appropriate holes in the front rack rails for the stationary sections using Fig. 5-5 as a guide.

2. Mount the stationary slide-out track sections to the front rack rails using either of these methods:

a. If the front rails are not countersunk, use the pan head screws and bar nuts to mount the stationary sections similar to the right-hand illustration shown in Fig. 5-6.

b. If the front rails are countersunk, use the flat head screws and bar nuts to mount the stationary sections as shown in Fig. 5-6 right-hand illustration.

3. Mount the stationary slide-out track sections to the non-tapped rear rails using this method:

a. Mount the left stationary section with hardware provided as shown in the left-hand or center illustration in Fig. 5-6. Note that the rear mounting bracket can be installed either way so the slide-out tracks will fit a deep or shallow cabinet rack.

b. Use Fig. 5-6 as a guide for mounting the right stationary section. Make sure the stationary sections are horizontally aligned so they are level and parallel with each other.

Adjustments

To adjust the slide-out tracks for smooth operation, proceed as follows:

1. Insert the instrument into the rack as described and as shown in steps 1 through 4 of Fig. 5-7 installation procedure.

2. Adjust the slide-out tracks for proper spacing as shown in Fig. 5-8.

Maintenance

The slide-out tracks require no lubrication. The special dark grey finish on the sliding parts is a permanent lubrication.

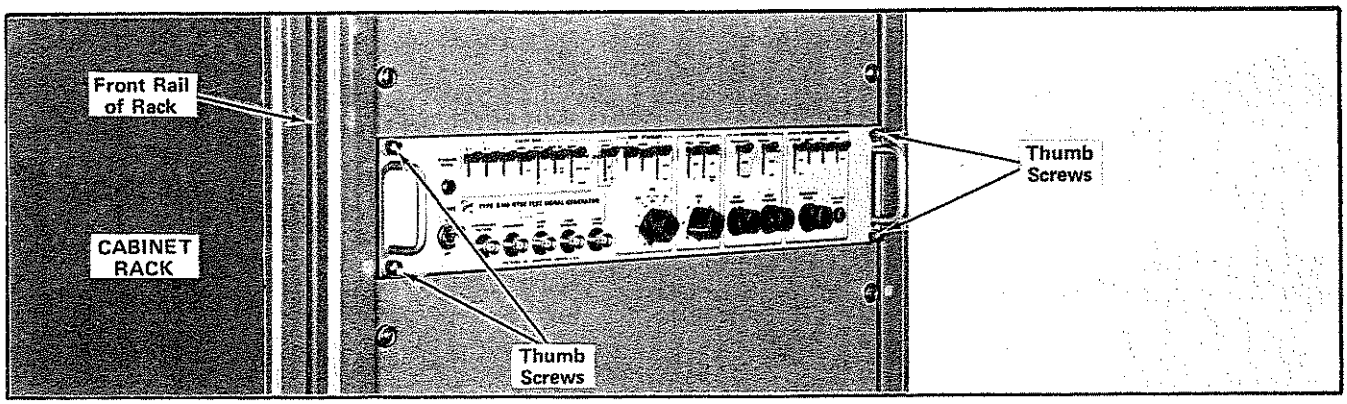


Fig. 5-1. The generator installed in a cabinet rack.

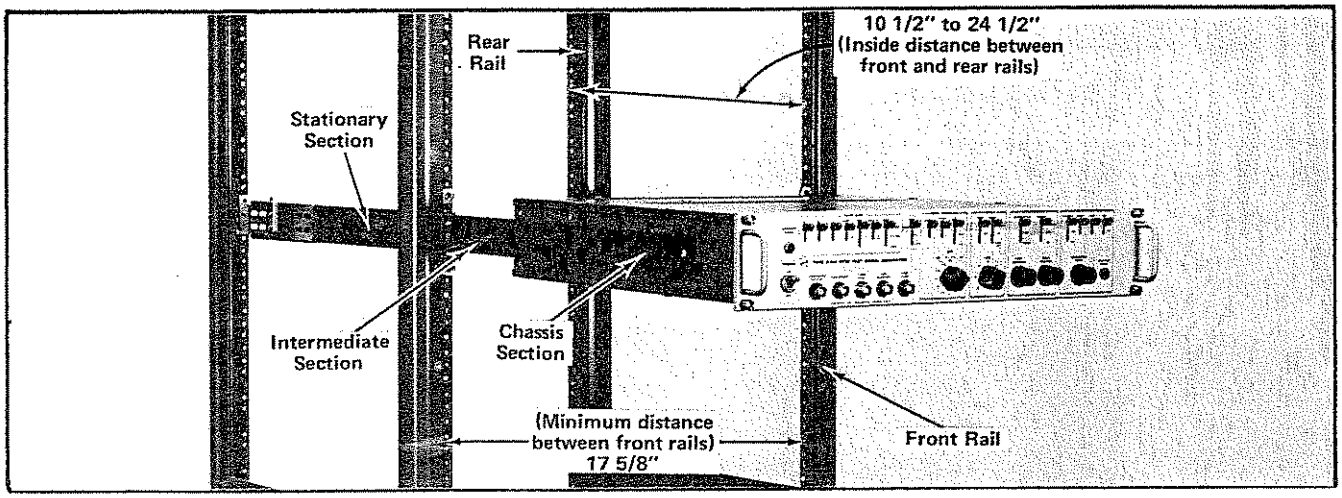


Fig. 5-2. The generator shown in the fully extended position. The cabinet rack slides have been removed from the rack to show mounting.

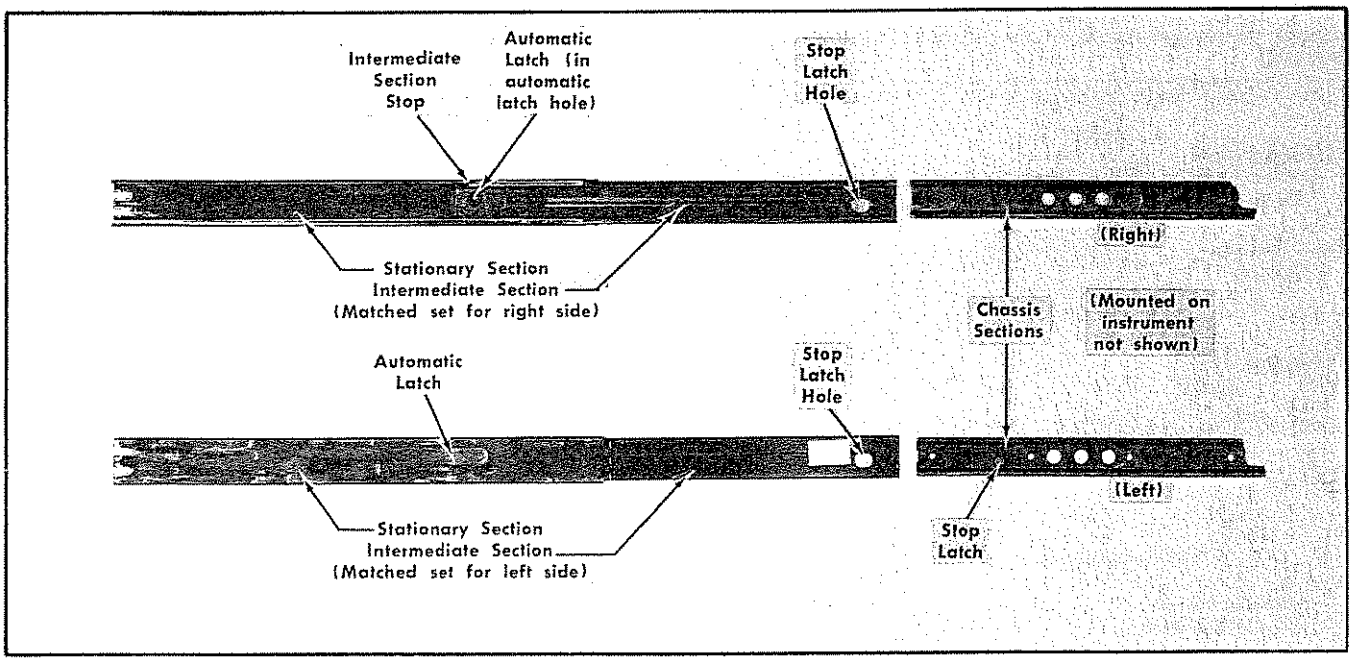


Fig. 5-3. Illustration showing the 1 3/4-inch wide slide-out track assemblies.

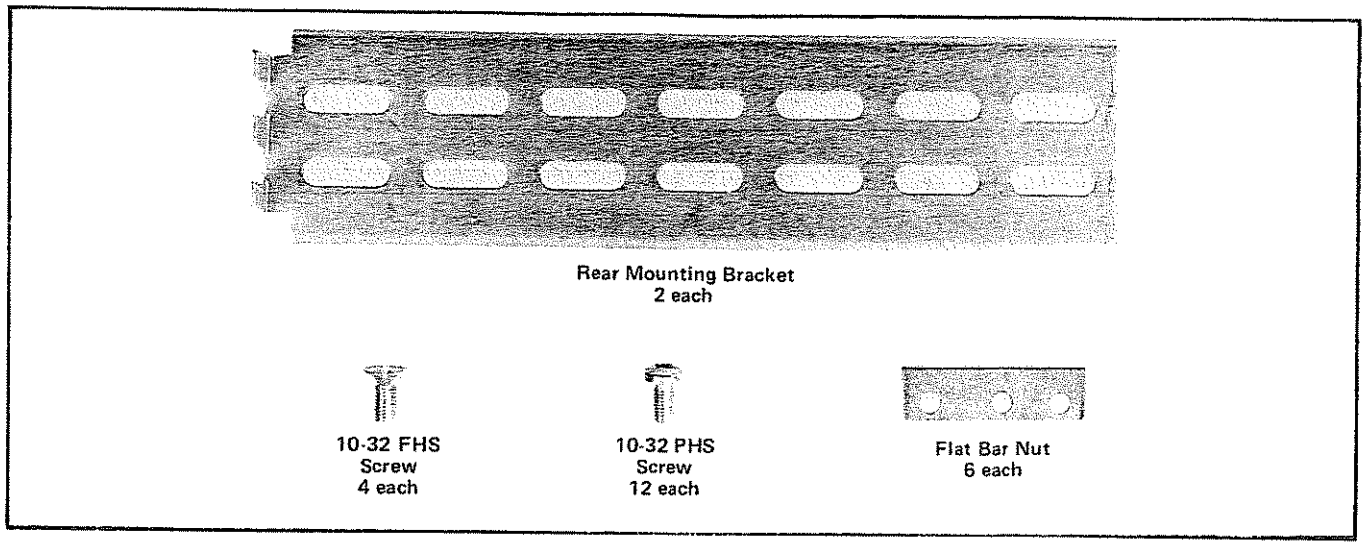


Fig. 5-4. Small hardware components for mounting the stationary sections to the rack rails.

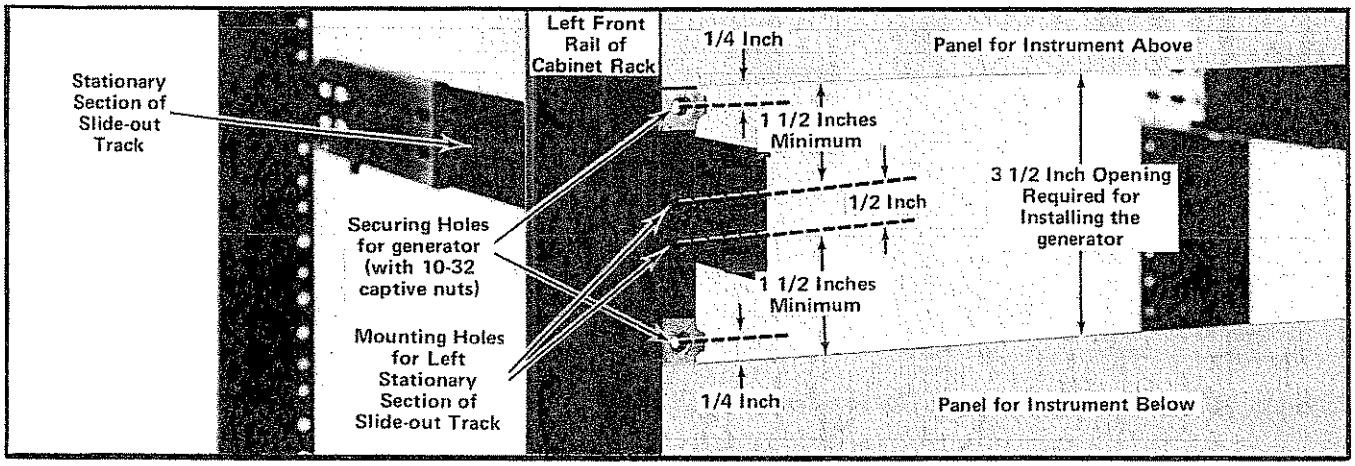


Fig. 5-5. Vertical mounting position of the left stationary section and location of the securing holes. These same dimensions apply to the right front rail.

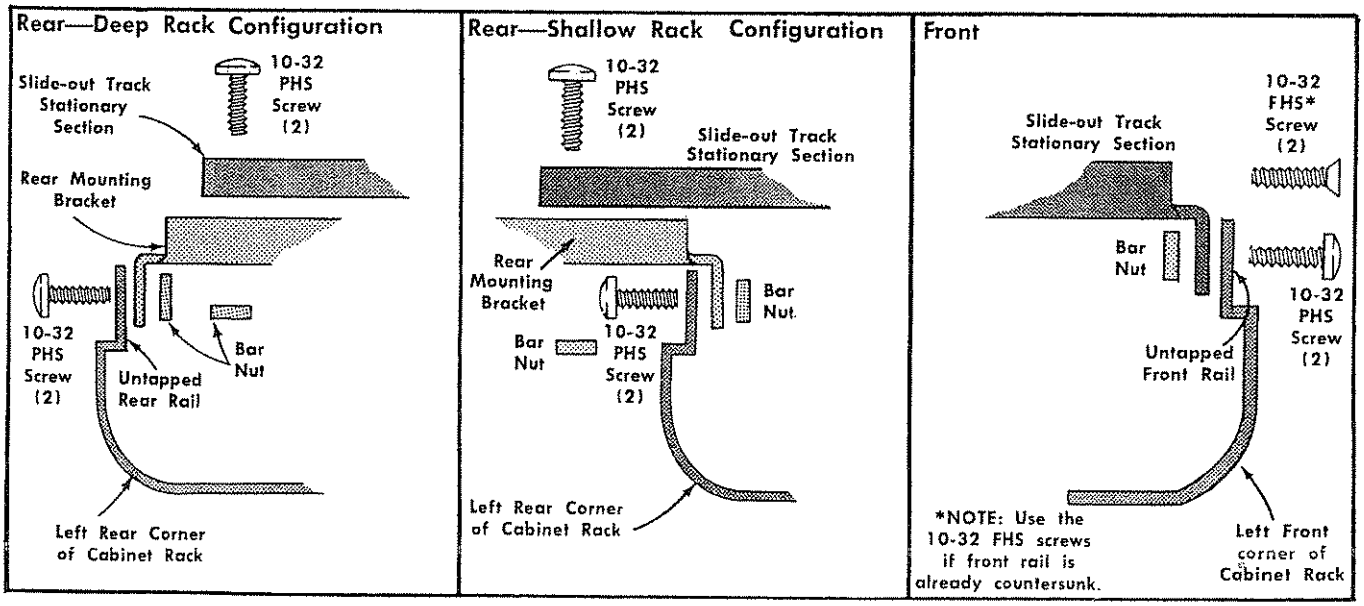


Fig. 5-6. Top view of cabinet rack showing mounting position of the left stationary section to the rails of the rack. Since the rails are not tapped, bar nuts are used to mount the stationary section to the rack rails.

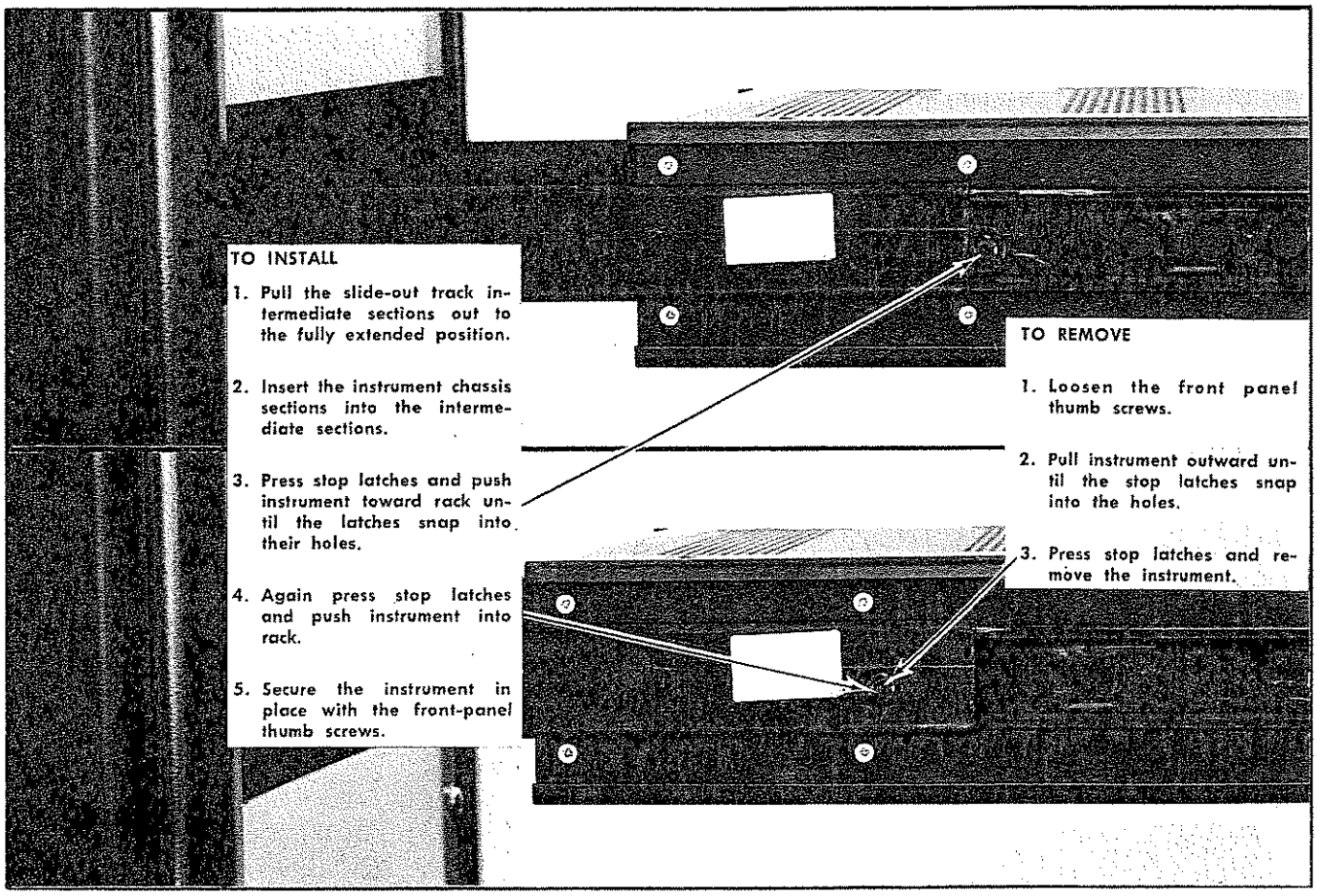


Fig. 5-7. Installing and removing the instrument.

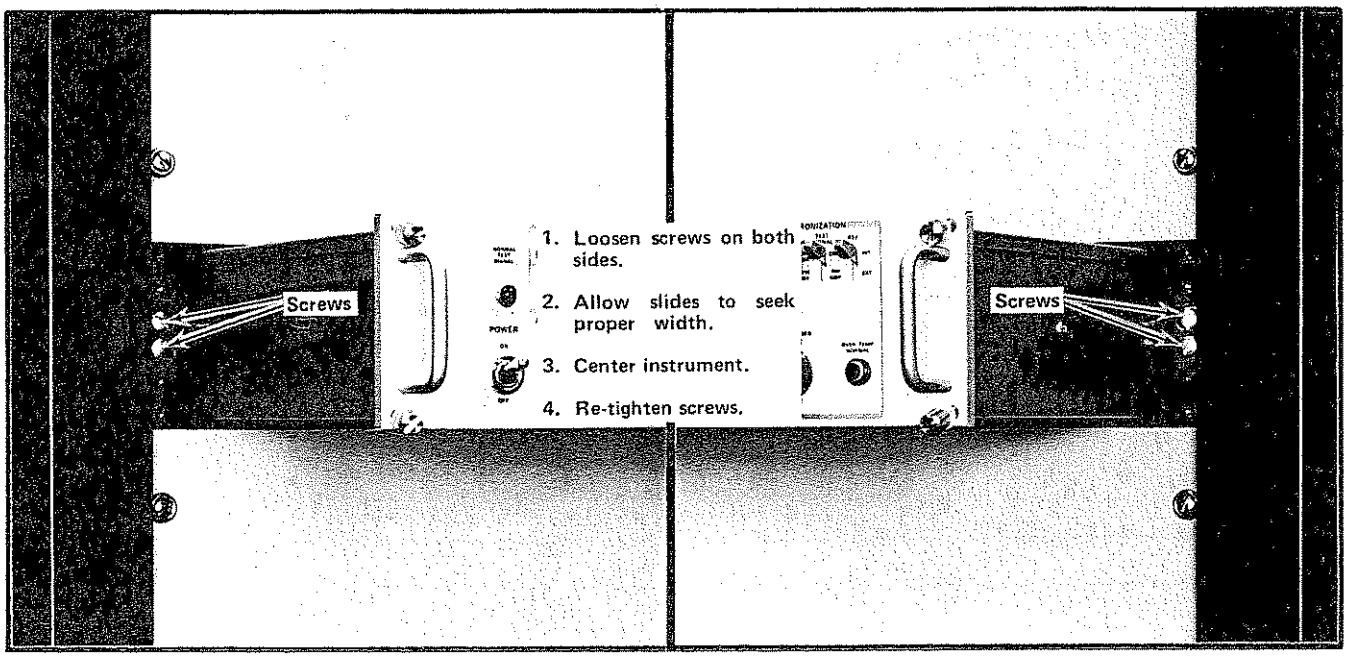
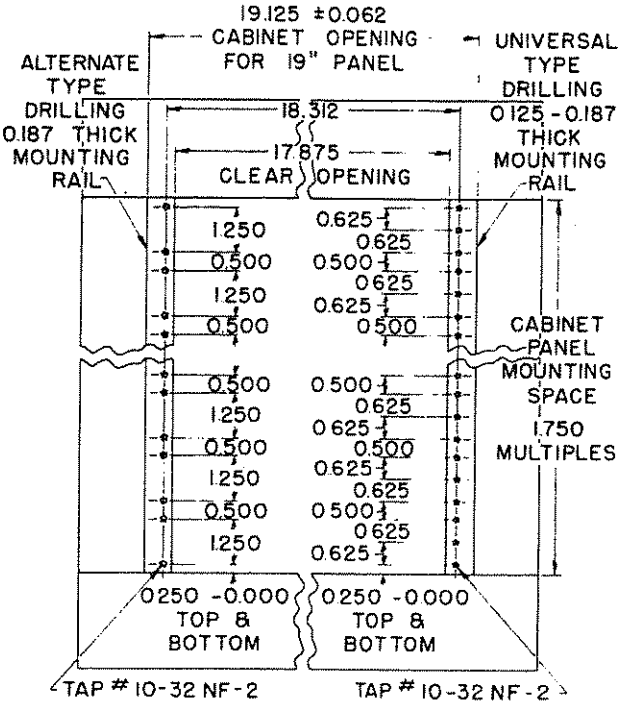
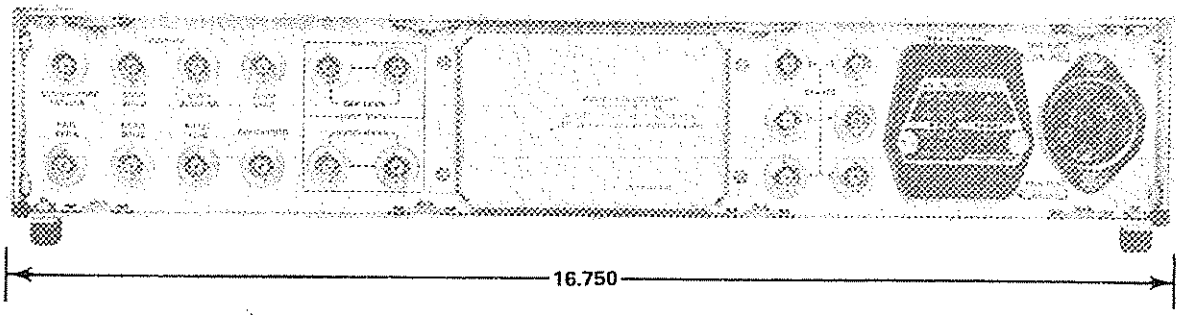
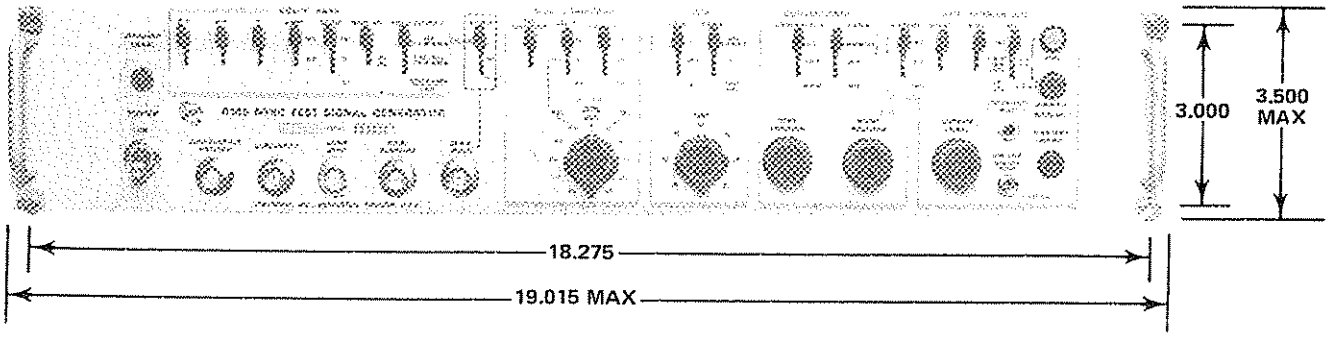


Fig. 5-8. Adjusting the slide-out tracks for smooth sliding action.

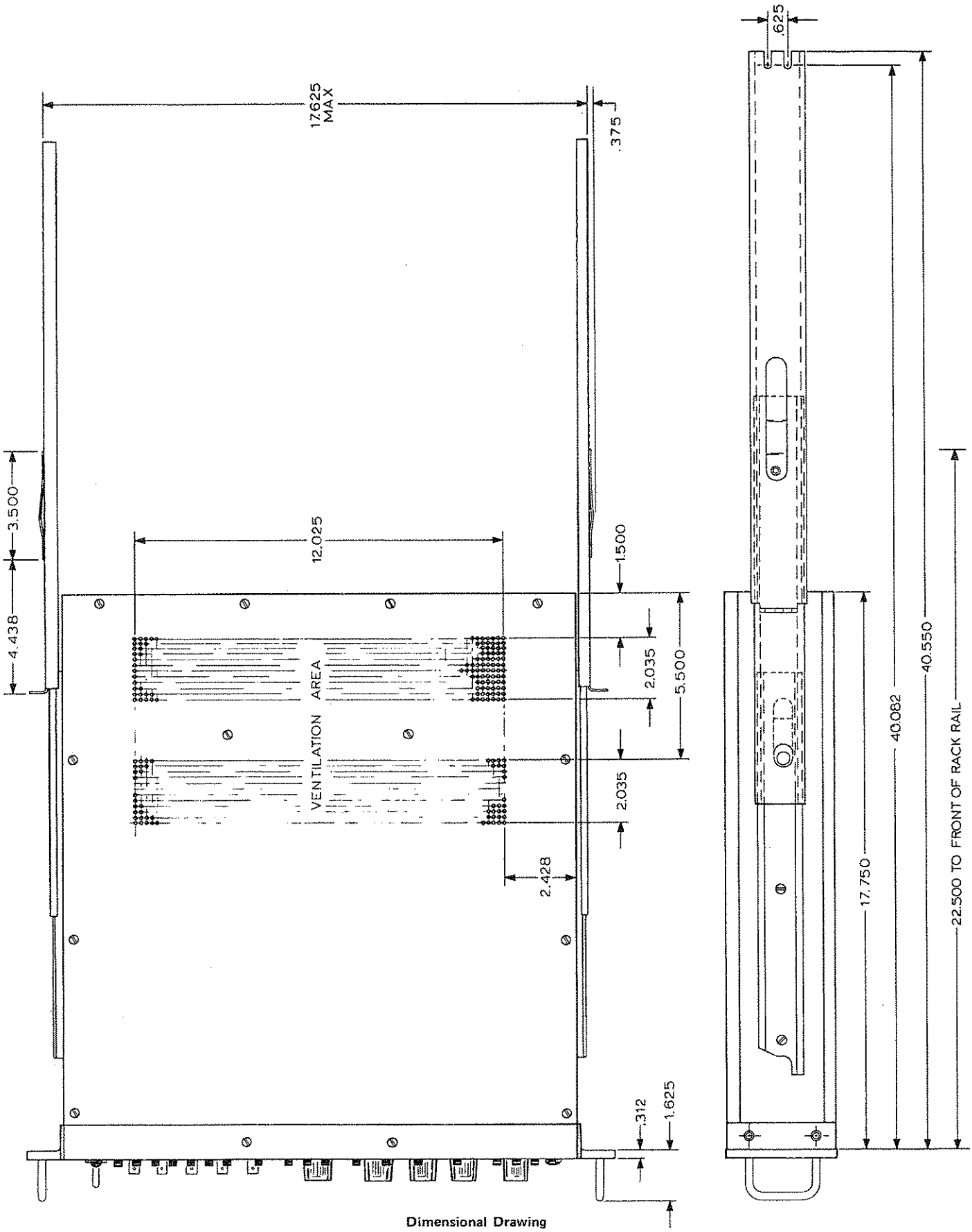
RACK RAIL TYPES







Dimensional Drawing



Dimensional Drawing

OPTIONS

Purpose

This section is meant to provide for documenting catalog options offered for the 148-M. Custom modifications are negotiated and documented separately.

At the time of initial publication, there were no catalog options offered for the 148-M.