

TLA7Bxx Logic Analyzer Series

Product Specifications & Performance Verification

Technical Reference

This document applies to TLA System Software Version 5.6
or higher

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Tektronix

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Preface

This document lists the characteristics and specifications of the TLA7Bxx Logic Analyzer products. It also contains performance verification and functional check procedures for the TLA7ABxx Logic Analyzer module.

For information on safety summaries, environmental considerations, and compliance information, refer to the *Tektronix Logic Analyzer Family Product Safety and Compliance Instructions* (Tektronix part number 071-2591-xx).

Related Documentation

The following table lists related documentation, available as printed documents or as PDF documents on the TLA Documentation CD and on the Tektronix Web site (www.tektronix.com). Other documentation, such as online help, is available on the instrument.

Related documentation

| Item | Purpose |
|--|--|
| TLA Quick Start User manuals | High-level operational overview |
| Online Help | In-depth operation and UI help |
| Installation Reference sheets | High-level installation information |
| Installation manuals | Detailed first-time installation information |
| XYZs of Logic Analyzers | Logic analyzer basics |
| Declassification and Securities instructions | Data security concerns specific to sanitizing or removing memory devices from Tektronix products |
| Application notes | Collection of logic analyzer application specific notes |
| Product Specifications & Performance Verification procedures | TLA Product specifications and performance verification procedures |
| Field upgrade kits | Upgrade information for your logic analyzer |
| Optional service manuals | Self-service documentation for modules and mainframes |

Specifications and Characteristics

All specifications in this document are guaranteed unless noted *Typical*. Typical characteristics describe typical or average performance and provide useful reference information.

Specifications that are marked with the ✓ symbol are checked directly (or indirectly) at your nearest Tektronix location or by using the performance verification procedures described in this document. (See page 13, *Performance Verification Procedures*.)

The performance limits in this specification are valid with these conditions:

- The instrument must be in an environment with temperature, altitude, humidity, and vibration within the operating limits described in these specifications.
- The instrument must have had a warm-up period of at least 20 minutes.

For modules, the performance limits in this specification are valid with these conditions:

- The module must be installed in a Tektronix Logic Analyzer Mainframe.
- The module must have been calibrated/adjusted at an ambient temperature between +18 °C and +28 °C.

Atmospheric Characteristics

Table 1: Atmospheric characteristics

| Characteristic | Description |
|-------------------|---|
| Temperature | <i>Operating (no media in CD or DVD drive of the mainframe)</i> |
| | +0 °C to +40 °C, 15 °C/hr maximum gradient, noncondensing (derated 1 °C per 305 m (1000 ft) above 1524 m (5000 ft) altitude) |
| | <i>Nonoperating (no media)</i> |
| | -20 °C to +60 °C, 15 °C/hr maximum gradient, noncondensing |
| Relative Humidity | <i>Operating (no media)</i> |
| | 5% to 90% relative humidity at 30 °C, 75% relative humidity between 30 °C to 40 °C, noncondensing. Maximum wet bulb temperature: +29.4 °C (derates relative humidity to approximately 57% at +40 °C). |
| | <i>Nonoperating (no media)</i> |
| | 5% to 90% relative humidity to 50 °C, noncondensing. Maximum wet bulb temperature: +40 °C (derates relative humidity to approximately 22% at +50 °C). |
| Altitude | <i>Operating</i> |
| | To 3000 m (9843 ft), (derated 1 °C per 305 m (1000 ft) above 1524 m (5000 ft) altitude. |
| | <i>Nonoperating</i> |
| | 12,000 m (39,370 ft) |

TLA7Bxx Logic Analyzer Module Specifications

Table 2: Input parameters with probes

| Characteristic | Description |
|--|--|
| ✓ Threshold accuracy | $\pm (35 \text{ mV} + 1\% \text{ of threshold voltage setting})$ For certification trace the characteristic |
| Threshold range and step size | |
| Large mode ¹ | Settable from -2.0 V to $+4.5 \text{ V}$ in 5 mV steps |
| Fast mode ² | Settable from -1.8 V to $+2.8 \text{ V}$ in 5 mV steps |
| P6960HS probe | Settable from -1.0 V to $+2.25 \text{ V}$ in 5 mV steps |
| Threshold channel selection | There is an independent threshold control for each signal. |
| ✓ Channel-to-channel skew | $\pm 40 \text{ ps}$ maximum (module only) Add: $\pm 60 \text{ ps}$ for P6810, P6860, and P6880 probes |
| Channel-to-channel skew (Typical) | For module only: $\pm 20 \text{ ps}$ |
| Merged module-to-module skew (Typical) | Inside slave modules (next to master module): $\pm 120 \text{ ps}$ (modules only) Outside slave modules (not next to master module): $\pm 220 \text{ ps}$ (modules only) |
| Sample uncertainty | |
| Asynchronous | Sample period |
| Synchronous | 20 ps |
| Input voltage range | |
| Large mode ¹ | -2.0 V to $+5.5 \text{ V}$ |
| Fast mode ² | -2.5 V to $+3.5 \text{ V}$ |
| P6960HS probe | -1.25 V to $+2.5 \text{ V}$ |
| Minimum slew rate (Typical) | 0.2 V/ns |
| Maximum operating signal swing | |
| Large mode ¹ | $6.0 \text{ V}_{\text{p-p}}$ |
| Fast mode ² | $2.0 \text{ V}_{\text{p-p}}$ |
| Probe overdrive | (Relationship between signal amplitude and threshold setting) |
| Single ended probes | $\pm 150 \text{ mV}$ (Large mode) ¹ $\pm 100 \text{ mV}$ (Fast mode) ² or $\pm 25\%$ of signal swing minimum required beyond threshold, whichever is greater $\pm 50 \text{ mV}$ or $\pm 25\%$ (P6960HS probe) |
| Differential probes | $V_{\text{pos}} - V_{\text{neg}}$ is $\geq 1250 \text{ mV}_{\text{p-p}}$ (Large mode) ¹ $\pm 50 \text{ mV}_{\text{p-p}}$ (Fast mode) ² $V_{\text{pos}} - V_{\text{neg}}$ is $\pm 50 \text{ mV}_{\text{p-p}}$ (P6960HS probe) |
| Maximum nondestructive input signal to probe | $\pm 15 \text{ V}$ $\pm 7.5 \text{ V}$ (P6960HS probe) |

Table 2: Input parameters with probes (cont.)

| Characteristic | Description |
|---|---|
| Minimum input pulse width (single channel) <i>(Typical)</i> | 200 ps (high-density and differential probes) 250 ps (general purpose probe) |
| Electrical delay from probe tip to input connector <i>(Typical)</i> | 7.70 ns \pm 60 ps (general purpose, high-density, and differential probes) |

¹ The Large mode specification applies when the voltage swing of the input signal is over two volts; the performance can degrade in Large mode.

² The Fast mode specification applies when the voltage swing of the input signal is less than two volts; performance is not degraded in Fast mode.

Table 3: Analog output

| Characteristic | Description |
|---|---|
| Number of outputs | Four analog outputs regardless of the module width. Any four of the module's channels can be mapped to the four analog outputs. |
| Attenuation | 10X |
| Bandwidth <i>(Typical)</i> | >3 GHz |
| Accuracy (Gain & Offset) <i>(Typical)</i> | \pm (50 mV + 2% of signal amplitude) |

Table 4: Channel width and depth

| Characteristic | Description |
|---------------------------|-----------------------------|
| Number of data channels | |
| TLA7BB4, TLA7BC4 | 128 data, 8 clock/qualifier |
| TLA7BB3 | 96 data, 6 clock/qualifier |
| TLA7BB2 | 64 data, 4 clock/qualifier |
| Acquisition memory depth | |
| TLA7BB2, TLA7BB3, TLA7BB4 | 64 M per channel, maximum |
| TLA7BC4 | 128 M per channel, maximum |

Table 5: Asynchronous sampling

| Characteristic | Description |
|---|---|
| ✓ Internal sampling period | 1.25 ns, 800 MS, all channels 625 ps, 1600 MS, all channels 313 ps, 3200 MS, half channels 157 ps, 6400 MS, quarter channels 50 ms is the slowest sampling rate. A 1-2-5 sequence is supported, but it starts with 157 ps. |
| ✓ Minimum recognizable word (across all channels) | Channel-to-channel skew + sample uncertainty Example for a P6860 high-density probe and a 1.25 ns sample period: 160 ps (± 60 ps) + 1.25 ns = 1.47 ns This specification applies only with asynchronous sampling. With synchronous sampling, the setup and hold window size applies. |

Table 6: Synchronous sampling

| Characteristic | Description |
|---|--|
| Synchronous sampling | |
| Master clock signals | Clock signals |
| TLA7BB2 | 4 |
| TLA7BB3 | 4 |
| TLA7BB4, TLA7BC4 | 4 |
| | You can enable any or all of the clock signals. For an enabled clock signal, you can select the rising, falling, or both edges as active clock edge(s). The clock signals are stored. |
| Merged slave clock signals | Clock signals |
| TLA7BB2 | 4 |
| TLA7BB3 | 4 |
| TLA7BB4, TLA7BC4 | 4 |
| | (In addition to the two clock signals that the Master can send to merged slave modules, each slave module can have additional clocks.) You can enable any or all of the clock signals For an enabled clock signal you can select the rising, falling, or both edges as active clock edge(s). Merging is allowed with all TLA7Bxx modules. |
| Qualifier signals | Qualifier signals |
| TLA7BB2 | 0 |
| TLA7BB3 | 2 |
| TLA7BB4, TLA7BC4 | 4 |
| | Qualifier signals are stored. |
| ✓ Single channel setup and hold window size | Single channel on single module 220 ps maximum Single channel on two to five merged modules 240 ps maximum If Deskew is used, add 20 ps (one oversampler step size) to the above numbers. |

Table 6: Synchronous sampling (cont.)

| Characteristic | Description |
|----------------------------------|---|
| Setup and hold window range | For each signal, the setup and hold window can be moved from +7.5 ns (setup time, typical) to -7.5 ns (setup time, typical) in 20 ps steps. You can shift the setup and hold window towards the setup region with 0 ns, 2.5 ns, 5 ns, or 7.5 ns. With a 0 ns shift the range is [+7.5, -7.5] ns, with a 2.5 ns shift the range is [+10, -5] ns, and with a shift of 7.5 ns the range is [+15, 0]. The sample point selection region is the same setup and hold window. This is specified for the setup time with typical figures. Hold time follows the setup time by the Setup and hold window size. |
| ✓ Maximum synchronous clock rate | 750 MHz, one sample point per clock, all channels 750 MHz, two sample points per clock, all channels 750 MHz, four samples points per clock, half channels 1400 MHz, one sample point per clock, all channels 1400 MHz, two sample points per clock, half channels |

Table 7: Demultiplex sampling

| Characteristic | Description |
|---|--|
| Base signals (2:1) TLA7BB4, TLA7BC4 | A3[7:0], A2[7:0], A1[7:0], A0[7:0] C3[7:0], C2[7:0] E3[7:0], E2[7:0] CK3, CK2, CK1, CK0 |
| TLA7BB3 | A3[7:0], A2[7:0], A1[7:0], A0[7:0] C3[7:0], C2[7:0] CK1, CK0 |
| TLA7BB2 | A3[7:0], A2[7:0], A1[7:0], A0[7:0] CK3, CK1 |
| Base signals (4:1) TLA7BB4, TLA7BC4 | A3[7:0], A1[7:0] C3[7:0] E3[7:0] CK3, CK1 |
| TLA7BB3 | A3[7:0], A1[7:0] C3[7:0] CK1 |
| TLA7BB2 | A1[7:0] C3[7:0] |
| Time between demultiplex clock edges (<i>Typical</i>) | Same limitations as that for normal synchronous acquisition. |

Table 8: Source synchronous sampling

| Characteristic | Description |
|---|---|
| Source synchronous edge detectors per module | 4 |
| Source synchronous edge detectors with merged modules | Slave modules have four source synchronous edge detectors. Two clocks are passed over from the master module. |
| Clock groups | Four for both single module and for a merged system |
| Size of clock group valid FIFO | Four stages (source synchronous or other) clocks to occur before the clock that completes the Clock Group Valid signal for that group. |
| Source synchronous clock alignment window | Channel-to-channel skew only |
| Source synchronous clock reset | <p>The Clock Group Valid FIFOs can be reset in the following ways:</p> <ol style="list-style-type: none"> 1. By the overflow of a presettable (0-255) 8-bit counter that counts by the 1.25 ns system clock or by the master heartbeat clock (synchronous or asynchronous). An active edge on a source synchronous clock places the reset count to its preset value. The timing is such that an active clock edge will clear the Clock Group Reset before arriving at the FIFO so that no data is lost. 2. By enabling an external reset. In this mode, one of the clock signals must be traded on the master module to act as a level-sensitive reset input. Any one of the clocks can be chosen and a polarity selection is available. This mode affects all Clock Group Complete circuits. <p>The two modes cannot be intermixed; one or the other must be chosen.</p> |

Table 9: Clocking state machine

| Characteristic | Description |
|-----------------|---|
| Pipeline delays | Each signal can be individually programmed with a pipeline delay of 0 through 31 active clock edges. The value held by the pipelines at the beginning of an acquisition can be preset high or low (all stages of a particular signal are forced to the same value). |

Table 10: Trigger system

| Characteristic | Description | | | | | | | | | | | | | | | | | | |
|---|--|---------------------|---------------------|---------------------|--------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|--------------------|---------------------|--------------------|---------------------|--------------------|---------------------|--------------------|---------------------|
| Triggering resources | | | | | | | | | | | | | | | | | | | |
| Word, range, and channel-to-channel compare recognizers | 24, word/range recognizers. The word recognizers can be traded off to form full width, double-bounded range recognizers. The following selections are available: | | | | | | | | | | | | | | | | | | |
| | <table border="1"> <tbody> <tr> <td>24 word recognizers</td> <td>0 range recognizers</td> </tr> <tr> <td>21 word recognizers</td> <td>1 range recognizer</td> </tr> <tr> <td>18 word recognizers</td> <td>2 range recognizers</td> </tr> <tr> <td>15 word recognizers</td> <td>3 range recognizers</td> </tr> <tr> <td>12 word recognizers</td> <td>4 range recognizers</td> </tr> <tr> <td>9 word recognizers</td> <td>5 range recognizers</td> </tr> <tr> <td>6 word recognizers</td> <td>6 range recognizers</td> </tr> <tr> <td>3 word recognizers</td> <td>7 range recognizers</td> </tr> <tr> <td>0 word recognizers</td> <td>8 range recognizers</td> </tr> </tbody> </table> | 24 word recognizers | 0 range recognizers | 21 word recognizers | 1 range recognizer | 18 word recognizers | 2 range recognizers | 15 word recognizers | 3 range recognizers | 12 word recognizers | 4 range recognizers | 9 word recognizers | 5 range recognizers | 6 word recognizers | 6 range recognizers | 3 word recognizers | 7 range recognizers | 0 word recognizers | 8 range recognizers |
| 24 word recognizers | 0 range recognizers | | | | | | | | | | | | | | | | | | |
| 21 word recognizers | 1 range recognizer | | | | | | | | | | | | | | | | | | |
| 18 word recognizers | 2 range recognizers | | | | | | | | | | | | | | | | | | |
| 15 word recognizers | 3 range recognizers | | | | | | | | | | | | | | | | | | |
| 12 word recognizers | 4 range recognizers | | | | | | | | | | | | | | | | | | |
| 9 word recognizers | 5 range recognizers | | | | | | | | | | | | | | | | | | |
| 6 word recognizers | 6 range recognizers | | | | | | | | | | | | | | | | | | |
| 3 word recognizers | 7 range recognizers | | | | | | | | | | | | | | | | | | |
| 0 word recognizers | 8 range recognizers | | | | | | | | | | | | | | | | | | |

Table 10: Trigger system (cont.)

| Characteristic | Description |
|--|---|
| Range recognizer channel order | <p>From most-significant probe group to least-significant probe group:</p> <p>Missing channels for modules with fewer than 136 channels are omitted. When merged, the range recognition extends across the two modules. The master module contains the most-significant groups.</p> |
| TLA7BB4, TLA7BC4 | CK3 Q1 C3 C2 C1 C0 Q3 Q2 E3 E2 E1 E0 CK0 Q0 A3 A2 D3 D2 CK1 CK2 A1 A0 D1 D0 |
| TLA7BB3 | CK3 Q1 C3 C2 C1 C0 CK0 Q0 A3 A2 D3 D2 CK1 CK2 A1 A0 D1 D0 |
| TLA7BB2 | CK3 CK0 C3 C2 A3 A2 CK1 CK2 A1 A0 D1 D0 |
| Glitch detector (Asynchronous clock mode) | <p>Any signal can be individually enabled to detect a glitch.</p> <p>A glitch is two or more signal transitions on a signal between the Asynchronous sample points.</p> |
| Minimum detectable glitch pulse width (<i>Typical</i>) | <p>Minimum input pulse width (single-signal)</p> <p>200 ps for high-density probes</p> <p>250 ps for general purpose probes</p> |
| Setup and hold violation detector (Synchronous clock mode) | <p>Any signal can be individually enabled to detect a setup or hold violation. The window range is from 7.5 ns before the clock edge to 7.5 ns after the clock edge. This range may be shifted towards the positive region by 0 ns, 2.5 ns, 5 ns, or 7.5 ns. With a 0 ns shift the range is [+7.5,-7.5] ns, with a 2.5 ns shift it is [+10,-5] ns, with a 5 ns shift the range is [+12.5, -2.5] ns, and with a shift of 7.5 ns the range is [+15, 0] ns. The sample point selection region is the same as the setup and hold violation window.</p> <p>The size of each signal's setup/hold violation window can be individually programmed. The maximum width of the window (and granularity of adjustment) depends on the decimation setting:</p> <ul style="list-style-type: none"> @ 20 ps granularity, max window size = 2.5 ns @ 40 ps granularity, max window size = 5.0 ns @ 80 ps granularity, max window size = 15 ns <p>Any setup value is subject to variation of up to the skew specification. Any hold value is subject to variation of up to the skew specification.</p> <p>Setup and hold detection is restricted to a group rather than individual signals; you can define individual groups for individual signals.</p> |
| Transition detector | <p>24, any signal can be individually enabled or disabled to detect a rising or falling transition (or either) between the current valid data sample and the previous valid data sample.</p> <p>Transition detection is restricted to a group rather than individual signals; you can define individual groups for individual signals.</p> |
| ✓ Fast counter/timers | <p>Two fast counter/timers. Each is 48 bits wide and can be clocked up to 800 MHz.</p> <p>maximum count = $2^{48}-1$ (including sign bit)</p> <p>maximum time = $\sim 3.5 \times 10^5$ sec = ~ 4 days</p> <p>Zero clock TC latency, with zero reset latency</p> <p>Counters can be reset, do nothing, incremented or decremented.</p> <p>Timers can be reset, not changed, started or stopped.</p> |
| Signal In [3:0] | Mainframe backplane input signal |
| Arm In | Mainframe backplane input signal |

Table 10: Trigger system (cont.)

| Characteristic | Description | |
|--|--|-------|
| Trigger In | Mainframe backplane input signal that causes both the main acquisition and MagniVu acquisition to trigger (if they are not already triggered). | |
| Active trigger resources | 24 maximum (excluding the counter/timers and Signal In) | |
| Trigger states | 16 | |
| ✓ Trigger state machine (TSM) sequence rate | DC to 800 MHz (1.25 ns) For data rates of 800 Mb/s or less, the TSM evaluates one data sample per TSM clock. For data rates greater than 800 Mb/s, the TSM evaluates multiple data samples per TSM clock up to the maximum acquired data rate. | |
| Trigger machine actions | | |
| Main acquisition trigger | Trigger the main acquisition memory. | |
| Main trigger position | Programmable to any data sample (1.25 ns boundaries). | |
| MagniVu trigger | Triggering of MagiVu memory is controlled by the main acquisition trigger machine. | |
| MagniVu trigger position | Programmable within 1.25 ns boundaries and separate from the main acquisition memory trigger position. | |
| Increment and decrement counter | Either of the two counter/timers used as counters can be incremented or decremented. | |
| Snapshot recognizer | Loads the current acquired data sample into the reference value of the word recognizer via a trigger machine action. All the data signals are loaded into their respective word recognizer reference register on a one-to-one manner. With merged modules, the snapshot recognizer only works with the master module. | |
| Snapshot load latency | 325 ns | |
| Start/stop timer | Either of the two counter/timers used as a timer can be started or stopped. | |
| Reset counter/timer | Either of the counter/timers can be reset. When a timer is reset, the timer continues in the started or stopped state it was in prior to the reset. | |
| Signal Out[3:0] | A signal sent to the backplane to be used by other modules. | |
| Trigger Out | A signal sent to the backplane to trigger other modules. | |
| Probe/Trigger/Backplane delay relationships | | |
| Delay time from probe tip to multiplex Signal Out (TLA7Bxx module front panel analog output connector) (Typical) | 9.45 ns, ± 500 ps | |
| Delay time from probe tip to trigger machine action (Typical) | 1254 ns + Sample error | |
| Delay time from trigger machine action to Signal Out (TLA7Bxx module P2 connector) (Typical) | Driving Signal 3:4 | 35 ns |
| | Driving Signal 2:1 | 35 ns |
| Delay time from trigger machine action to Trigger Out (TLA7Bxx module P2 connector) (Typical) | 38 ns | |

Table 10: Trigger system (cont.)

| Characteristic | Description |
|---|--|
| Delay time from Signal In to trigger machine action (not used as ARM) (<i>Typical</i>) | Signal In 4:1 54 ns + Sample CLK ¹ |
| Delay time from Signal In (TLA7Bxx module P2 connector) to trigger machine action (used as ARM) (<i>Typical</i>) | 53 ns + Sample CLK ¹ |
| Delay time from Trigger In (TLA7Bxx module P2 connector) to trigger machine action (<i>Typical</i>) | 38 ns + Sample CLK ¹ |
| Storage control | |
| Global storage | Storage is allowed only if a specified condition is met. This condition can use any of the trigger resources except for the counter/timers. Storage commands defined in the current trigger state will override the global storage control. Global storage can be used to start the acquisition with storage initially turned on (default), or off. |
| By event | Storage may be turned on or off, or only the current sample may be stored. Event storage control overrides any global storage commands. |
| Block storage (This allows users to store a group of samples around a valid data sample when storage control is used.) | When enabled, 31 samples are stored before and after the valid sample. This has meaning only when storage control is being used. Block storage is disallowed when glitch storage or setup and hold violation storage is enabled. |
| Glitch violation storage | Glitch violation information can be stored to acquisition memory with each data sample when asynchronous sampling is used. The acquisition data storage size is reduced by half when this mode is enabled (the other half holds the violation information). The fastest asynchronous sampling rate when Glitch violation storage is enabled is 1.25 ns. |
| Setup and hold violation storage | The acquisition memory can be enabled to store setup and hold violation information with each data sample when synchronous sampling is used. The acquisition data storage size is reduced by one half when this mode is enabled (the other half holds the violation information). The maximum sync clock rate in this mode is 750 MHz. |

¹ Sample CLK is the delay due to logic analyzer sampling. For asynchronous sampling, this delay is equal to the internal sampling period. For synchronous sampling, this delay is equal to time until the next active clock edge.

Table 11: MagniVu feature

| Characteristic | Description |
|-------------------------|---|
| MagniVu memory depth | 128K per channel This acquisition memory is separate from the main acquisition memory. |
| MagniVu sampling period | Data is asynchronously sampled and stored every 20 ps in a separate high resolution memory. The storage speed can be changed (by software) to 40 ps, 80 ps, 160 ps, 320 ps, or 640 ps (with no loss in memory depth) so that the MagniVu memory covers more time at a lower resolution. |

Table 12: Merged modules

| Characteristic | Description |
|--|---|
| Number of merged modules | <p>2, 3, 4, or 5 adjacent modules can be merged. Modules can have unequal channel widths and channel depths.</p> <ul style="list-style-type: none"> ■ When two modules are merged, the master is in the lower numbered slot. ■ When three modules are merged, the master is in the center slot (slave on each side). ■ When four modules are merged, the master is in the next to lowest numbered slot. ■ When five modules are merged, the master is in the center slot (two slaves on each side). |
| Number of channels after merging | Sum of all channels available on each of the merged modules including clocks and qualifiers. No channels are lost when modules are merged. |
| Merged system acquisition depth | The channel depth is equal to that of the shallowest module. |
| Number of clock and qualifier channels after merging | <p>The qualifier signals on the slave modules can only be used as data signals. They cannot influence the actual clocking function of the logic analyzer (for example, log strobe generation).</p> <p>The clock signals on the slave modules can capture data on those modules for source-synchronous applications. Each slave module contributes four additional clock signals to the merge set. All clock and qualifier signals are stored to acquisition memory.</p> |
| Merged system triggering resources | Same as a single module except for range recognizers and the snapshot recognizer. The main difference is that for word recognizers, setup and hold violation detector, glitch detector, and transition detectors, the width is increased to equal the merged signal width. The range recognizer width will increase to the merged signal width up to three modules. Range recognizers are limited to a maximum of four when merged. The Snapshot recognizer only works with the master module in merged module configurations. |

Table 13: Data placement

| Characteristic | Description |
|---|---|
| System time zero placement error (Typical) | <p>$\pm 1.25 \text{ ns} + \text{Mainframe backplane } 10 \text{ MHz skew}$</p> <p>This specifies how well TLA7Bxx modules can place system time zero. All of the stored acquisition data is referenced to this point.</p> |
| Data correlation error (Typical) | <p>$\pm 50 \text{ ps} + \text{System time zero placement error}$</p> <p>The maximum error in being able to place data to the System Time Zero mark.</p> <p>Error sources include:</p> <ul style="list-style-type: none"> System time zero placement error 400 MHz clock variation |
| Relative data timestamp accuracy (Typical) | <p>$\pm 100 \text{ ps} + \text{Sample uncertainty} + \text{mainframe backplane } 10 \text{ MHz clock jitter/tolerance}$</p> <p>A timestamp value relative to System time zero is stored with every data sample.</p> <p>This specification can be used to indicate the accuracy of a time measurement between samples. When measuring between the samples, only the time difference between samples should be used to indicate the accuracy. For example, if one sample has a timestamp of 1 hour, and another sample has a timestamp of 1 hour and 10 ms, then 10 ms is the period of time used to determine the amount of error caused by the 10 MHz clock tolerance.</p> |
| Timestamp counter resolution and duration | <p>20 ps resolution</p> <p>4.17 days duration</p> |

Table 14: NVRAM

| Characteristic | Description |
|--|--|
| Nonvolatile memory retention time (<i>Typical</i>) | Battery is integral to the NVRAM. Battery life is >10 years. The length of time that calibration constants and other information stored in NVRAM is retained in the absence of power to the instrument. |

Table 15: Mechanical

| Characteristic | Description |
|-----------------------|---|
| Construction material | Chassis parts constructed of aluminum alloy; front of instrument is constructed of plastic laminated to steel front panel; circuit boards constructed of glass-laminate. Cabinet is aluminum. |
| Weight | TLA7BB4, TLA7BC4 5 lb. 6 oz. or 2.45 kg TLA7BB3 5 lb. 4 oz. or 2.4 kg TLA7BB2 5 lb. 0.5 oz. or 2.3 kg |
| Overall dimensions | Height 10.32 in. Width 2.39 in. (Width increases by 0.41 in. when the merge connector is in the “up” position.) Depth 14.70 in. |

Performance Verification Procedures

This section contains procedure for performance verification of the logic analyzer. Generally, you should perform these procedures once per year or following repairs that affect certification.

The performance verification procedures check the following specifications:

- Threshold Accuracy
- Setup/Hold Window Size

Test Equipment

The procedures in this section use external, traceable signal sources to test the specifications marked with the ✓ symbol. These specifications are checked directly (or indirectly) by using the performance verification procedures in this section. For convenience, you can also return your TLA7Bxx module to your nearest Tektronix location to have Tektronix perform these procedures.

To complete the performance verification procedures, you will need the equipment listed in the following table:

Table 16: Test equipment

| Test equipment or fixture | Requirements | Example |
|--|--|-----------------------------------|
| Precision voltage reference or a DC signal generator and precision digital voltmeter | (accurate to within ± 5 mV) | |
| Logic analyzer probe | For Threshold Accuracy Test | P6810 |
| | For Setup and Hold Test | P6800 or P6900 series probe |
| Threshold Accuracy test fixture | One required. (See page 14, <i>Threshold Accuracy Test Fixture</i> .) Warm-up time: 30 minutes | |
| TLACAL software | Refer to the <i>TLA7000 Series Logic Analyzer Installation Manual</i> for information on installing and using the TLACAL software. | |
| Deskew fixture | Includes coaxial cable with SMA connector. Use deskew fixture appropriate for your P6800 or P6900 probe. | |
| P6800 Deskew fixture | | Tektronix part number 020-2942-00 |
| P6900 Deskew fixture | | Tektronix part number 020-2940-00 |

Threshold Accuracy Test Fixture

Use this fixture to gain access to the logic analyzer probe pins. The fixture connects all ground pins together, and all signal pins together.

Equipment Required You will need the following items to build the test fixture:

| Item | Description | Example part number |
|---------------------------|---|--------------------------------------|
| Square-pin strip | 0.100 x 0.100, 2 x 8 contacts (or two 1 x 8 contacts) | SAMTEC part number TSW-102-06-G-S |
| Wire | 20 gauge | |
| Soldering iron and solder | 50 W | |

Build Procedure Use the following procedure to build the test fixture.

1. Set the square-pin strip down and lay a wire across one row of pins on one side of the insulator as shown. Leave some extra wire at one end for connecting to a test lead. (See Figure 1.)
2. Solder the wire to each pin in the row.
3. Repeat for the other row of pins.

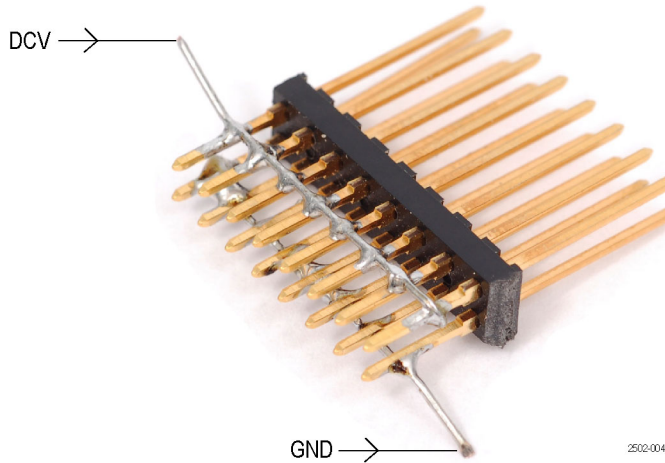


Figure 1: Threshold Accuracy test fixture

Threshold Accuracy Test

This procedure verifies the threshold voltage accuracy of the logic analyzer.

| | |
|---------------------------|---|
| Equipment required | Precision voltage reference or a DC signal generator and precision digital voltmeter (accurate to within ± 5 mV) Threshold Accuracy test fixture P6810 Logic analyzer probe |
| Prerequisites | Warm-up time: 30 minutes |

Test Equipment Setup

Connect a P6810 probe from the logic analyzer to the voltage source, using the Threshold Accuracy test fixture. If the voltage source does not have the required output accuracy, use a multimeter with the required accuracy to verify the voltage output levels specified in the procedure.

TLA7Bxx Setup

To set up the logic analyzer for this test, you must define the characteristics of the channel that you are testing, and then set the trigger parameters:

1. Open the Setup window.
2. In the Group column, enter a name for the probe group that you are testing (“Test” in the example).
 - a. Define the signals for the group that you are testing.
 - b. Set the sampling to Asynchronous, 1.25 ns.
 - c. Set Acquire to Samples.
 - d. Set the Samples per Signal to 128 K or less.
3. Go to the Trigger window and select the Power Trigger tab. Create a trigger program that triggers the logic analyzer when it doesn't see all highs or all lows:
 - a. Click the If Then button.
 - b. Set the channel definition to match the figure shown. (See Figure 2 on page 16.)
 - c. After you set the channel definitions, click OK.

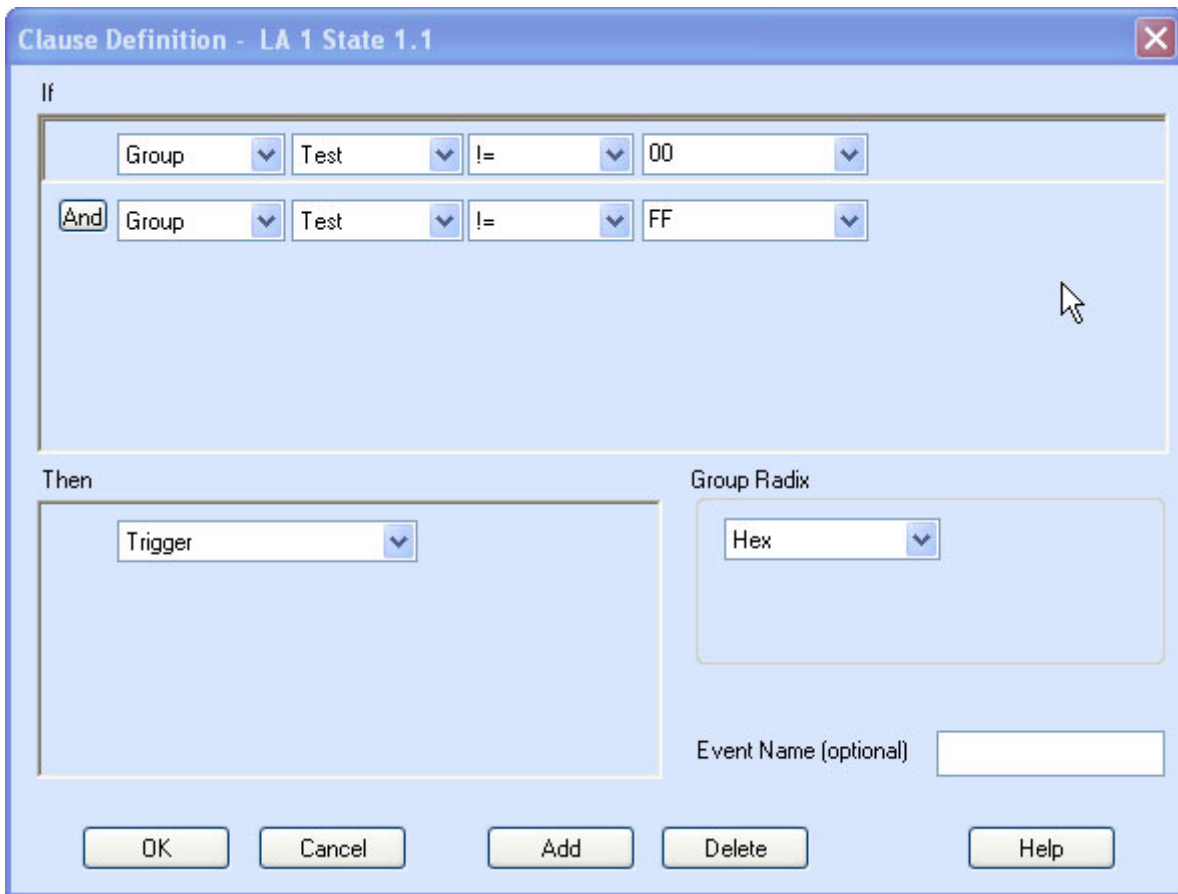


Figure 2: Setting trigger parameters

Verification Procedure

Complete the following steps to complete this procedure. Record the results on the copy of the Calibration Data Sheet.

1. Go to the Setup window of the logic analyzer and set the probe threshold voltages to 4 V.
2. Set the voltage source to 3.875 V.
3. Start the logic analyzer and verify that it does not trigger.
4. Increase the voltage in 10 mV steps, waiting at least 3 seconds between steps to make sure that the logic analyzer continues to run without triggering. Continue until the logic analyzer triggers and then record the voltage.
5. Set the voltage source to 4.125 V.
6. Start the logic analyzer and verify that it does not trigger.
7. Decrease the voltage in 10 mV steps, waiting at least 3 seconds between steps to make sure that the logic analyzer continues to run without triggering. Continue until the logic analyzer triggers and then record the voltage.
8. Add the two voltage values and divide by two. Verify that the result is $4.00\text{ V} \pm 75\text{ mV}$. Record the voltage on the Calibration Data Sheet.
9. Go to the Setup window and set the logic analyzer threshold voltages to -2.0 V .
10. Repeat steps 3 through 8 for -2.105 V and -1.895 V .
11. Add the two voltage values and divide by two. Verify that the result is $-2.00\text{ V} \pm 55\text{ mV}$. Record the voltage on the Calibration Data Sheet.
12. Repeat the procedure for each probe channel group that you want to verify.

Setup & Hold Test

This test uses the Verification part of the TLA7Bxx deskew procedure to verify the setup and hold time. The complete deskew procedures are described in the *TLA7000 Series Logic Analyzers Installation Manual*. The manual is available on your TLA Documentation CD and on the Tektronix Web site. Refer to the installation manual, to install the TLACAL software.

NOTE. *The deskew procedures require the appropriate TLACAL software and deskew test fixture, which are described in the TLA7000 Series Logic Analyzer Installation Manual.*

The following procedure describes the Verification part of the deskew procedure. You should be able to run the Verification procedure without performing the full deskew procedure. If any failures occur, try running the full deskew procedure as described in the *TLA7000 Series Logic Analyzer Installation Manual* and then try the Verification procedure again.

1. Close the TLA application if it is running.
2. Double-click the TLACAL icon on the desktop to start the software.
3. When the TLA Connection dialog box appears, connect to your instrument.

The TLACAL window appears on your desktop. (See Figure 3.)

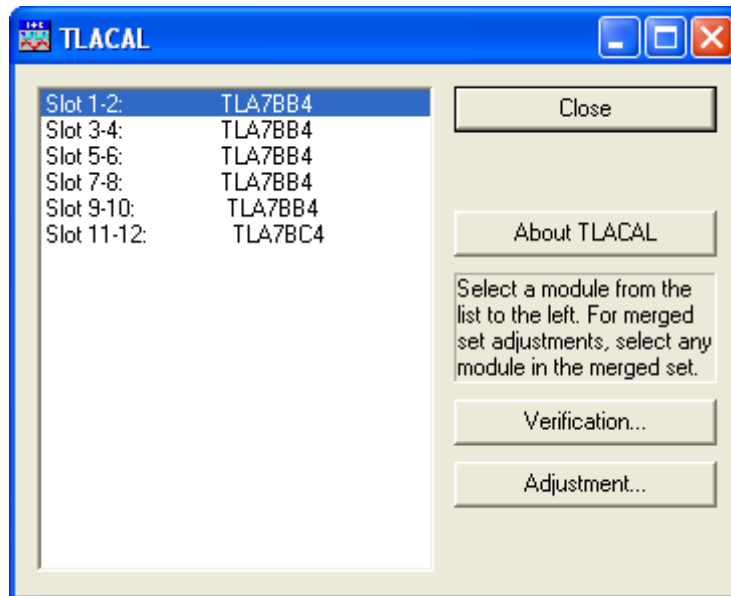


Figure 3: TLACAL startup window

4. In the dialog box, select the module that you want to test.
5. Click the Verification button to start the software. The Verification procedure dialog box appears. (See Figure 4.)

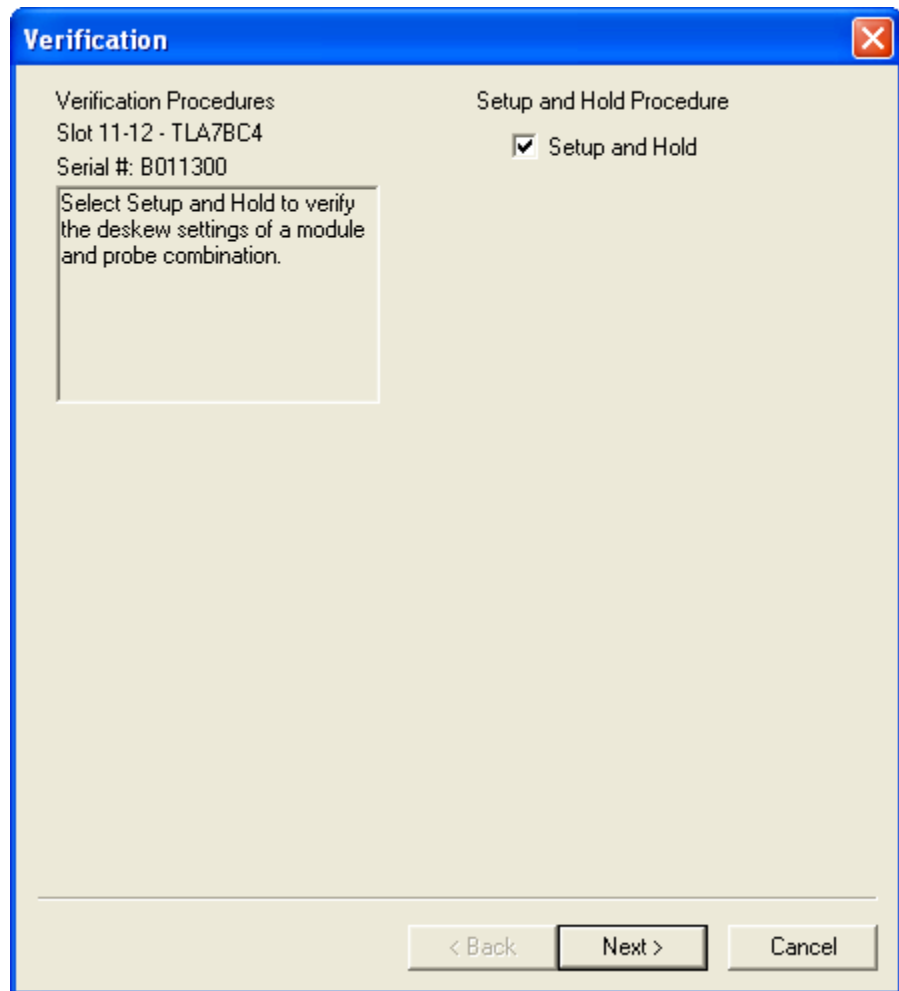


Figure 4: Verification procedure dialog box

6. Verify that Setup and Hold is selected at the top of the dialog box.
7. Click the Next button at the bottom of the dialog box to display the probe connection instructions.
8. Follow the on-screen instructions to connect the probes, clock cable, and the deskew fixture.

9. Click the Next button to begin the procedure and follow the on-screen instructions. The software will begin the verification procedure and display the results in the dialog box.

The procedure has you connect and disconnect probes and the deskew fixture. After you complete the procedures, make sure that the correct probes are connected for your configuration. These procedures are only valid for the probes connected to the specific probe connectors. If you change the probe connections, you must redo the procedures.

NOTE. *If any failures occur, check your probe or deskew fixture connections and reseal them, if necessary. Then click the Back button to restart the test. If the failures continue to occur, try running the Deskew and Adjustment procedures as described in the TLA7000 Series Logic Analyzer Installation Manual. Try running the Verification procedure again.*

10. Click the Finish button to finish the procedure and return to the startup window.

Functional Check Procedures

Functional Verification

Functional verification procedures consist of running the Power-on diagnostics, Extended diagnostics, and acquiring a signal from the SUT.

Power-on and Extended Diagnostics

Do the following steps to run the power-on and extended diagnostics:

NOTE. *Running the extended diagnostics will invalidate any acquired data. If you want to save any of the acquired data, do so before running the extended diagnostics.*

You will need a mainframe with a logic analyzer module installed in the mainframe.

Perform the following tests to complete the functional verification procedure:

NOTE. *If you control your logic analyzer from a remote location, make sure that you select Run Power-on Diagnostics in the TLA Connection dialog box. Otherwise the instrument will bypass the power-on diagnostics.*

1. If you have not already done so, power on the instrument.

The instrument runs the power-on diagnostics each time that you power on the instrument. If any failures occur, the diagnostic window will appear.

2. Go to the System menu and select Calibration and Diagnostics.
3. Scroll through the list of tests and verify that all power-on diagnostics is pass.

NOTE. *Allow the instrument to warm up for 30 minutes before continuing with the Extended diagnostics.*

4. Click the Extended Diagnostics tab.

NOTE. *Disconnect any probes connected to your logic analyzer module. If probes are connected while you run the extended diagnostics, the floating stimulus test will fail. If you do not want to remove the probes, disregard the results of this test. All other tests should pass.*

5. Select the top-most selection for your module in the list of tests. For example, if your logic analyzer module is installed in Slot 3 of your mainframe, select Slot 3:TLA7BB4 - LA.
6. Select the type of test that you want to run (One Time, Continuous, or Until Fail).
7. Click Run to start the tests.

All tests that displayed an "Unknown" status will change to a Pass or Fail status depending on the outcome of the tests.

8. After the tests have been completed, scroll through the list and verify that the instrument passes all tests.

NOTE. *Installing a module in the mainframe provides a means of verifying connectivity and communication between the module and the mainframe. If the instrument fails any test, try using a different module and repeat the tests to isolate the problem to the mainframe or to the module.*

Acquire a Signal

To verify that the logic analyzer module can acquire signals, connect the logic analyzer to a known good signal source through one of the logic analyzer probes.

Power on the logic analyzer and the SUT.

Go to the logic analyzer Setup window and verify that the signal activity connectors show activity for any signals connected to the SUT. The logic analyzer always acquires signals. If the signal activity indicators show the correct activity for the SUT, you have verified that the logic analyzer acquired a signal from the SUT and displayed the information in the Setup window.

NOTE. *If there is no signal activity, verify that the threshold setting is correct for your circuit.*
