NEX-DDR3INTR-HS
DDR3 800-1866MT/s Interposer

For use with the TLA7Bx4 Logic Analyzer Modules

Including these Software Support packages:

B_DDR3D_4A B_DDR3D_2D
R_DDR3D_2A (Reduced Module Count support)
R_DDR3D_1A (Reduced Module Count support)
DDR3SPA

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1.0 OVERVIEW

1.1 General Information

The DDR3 Interposer Products are designed for ease of use. Interposers add extra signal trace length and an extra connector that might affect the quality of the system operation in some systems.

> This Product is designed for capture of DDR3 data rates of 1866MT/s or slower, and may only be used with the Tektronix TLA7BB4 acquisition modules.
> While the Interposer specification is 1866 for UDIMMs, the RDIMMs support have only been specified and validated to 1600. Contact Nexus for updates to this RDIMM specification.

Various Nexus and Tektronix probes interface between the Interposer and the Logic Analyzer. Refer to the section below to match your needs.

This Interposer has been designed to provide a quick and easy connection between Tektronix TLA7BB4 Logic Analyzer acquisition cards and a 240-pin DDR3 (Double Data Rate 3) bus. Contact NEXUS Technology for other available DDR3 Products. The Nexus Technology web site (www.NexusTechnology.com) contains information on the latest software release.

1.2 Customer Product Acceptance

Nexus Technology has designed this interposer to have a minimal effect in your target. As with any interposer solution, approximately one inch of trace length will be added between your target and the target DIMM. Depending on the target layout, memory controller, DIMM type and DIMM socket being probed, an interposer may affect the performance of your system. All users are given 30 days to qualify the interposer in their system. Should performance issues arise it is important to know that alternate solutions are available. Nexus Technology offers NEXVu VDIMMs which provide both optimal probe points (at the memory components) and no added trace length or interposer effects. Also available are memory component products which also provide optimal probe points, extremely small added trace lengths, and extremely small interposer effects.

1.3 Software Package description

The NEX-DDR3INTR-HS support includes the following software packages which require TLA Application software V5.6.703 or later:

> **B_DDR3D_2D** allows the user to acquire Read AND Write data from a single, dual or quad rank DDR3 DIMM running 1333MT/s or slower. This support requires 1ea. NEX-PRB1XL, 3ea. NEX-PRB2XL Low Profile Distributed probes, and two merged Tektronix TLA7BB4 750MHz or 1.4GHz acquisition cards. This support can use Selective Clocking to reduce the number of Idle states acquired by the logic analyzer.

B_DDR3D_4A allows the user to acquire Read AND Write data from a single, dual or quad rank DDR3 DIMM running **1866MT/s** or slower. This support requires 1ea. Tektronix P6960HCD and 3ea. Tektronix P6962HCD probes, and four merged Tektronix TLA7BB4 acquisition cards each with the 1.4GHz state speed option.

R_DDR3D_1A (Reduced Module Count Support) allows the user to acquire Read AND Write data from a single, dual or quad rank DDR3 DIMM running 1333MT/s or slower. This support requires 4ea. NEX-PRB1XL Low Profile Distributed probes and one Tektronix TLA7BB4 750MHz or 1.4GHz acquisition card. There are a few limitations or cautions when using this support:

- Selective clocking is not available

R_DDR3D_2A (Reduced Module Count Support) allows the user to acquire Read AND Write data from a single, dual or quad rank DDR3 DIMM running **1866MT/s** or slower. This support requires 4ea. Tektronix P6960HCD probes and two merged Tektronix TLA7BB4 acquisition cards each with the 1.4GHz state speed option. The limitations and cautions when using this support are:

- Selective clocking is not available
- When using a QR DIMM if one or more Ranks are powered down data may be acquired erratically.

Note that this manual uses some terms generically. For instance, references to the TLA700/7000 apply to all suitable TLA7XXX Logic Analyzers, or PCs being used to control the TLA. NEX-DDR3INTR-HS and X_DDR3D_XX refers to any of the B_DDR3D_2D/_4A or R_DDR3D_1A/_2A software support packages.

This manual assumes that the user is familiar with the DDR3 SDRAM Specification and the Tektronix TLA Logic Analyzers. It is also expected that the user is familiar with the Windows environment used with the TLA.

1.4 Eye size required

The Eye size (stable data) required at the input resistor to the Nexus passive probes (NEX-PRB1XL and NEX-PRB2XL) is 330ps and 0.2V. The eye size for the Tektronix probes is 240ps and 0.2V. Capture accuracy may be affected if a stable eye cannot meet this requirement. The eye is a perfectly shaped diamond with each side equal distant from the center.

1.5 1866MT/s VCC required

1866MT/s capture by the logic analyzer requires a VCC voltage of 1.65V. The user needs to ensure that their system under test can provide and withstand this higher VCC voltage level.

2.0 SOFTWARE INSTALLATION

2.1 General Support Software Information

One CD containing all of the relevant support software and documentation has been included with the NEX-DDR3INTR-HS product. The particular support needed depends on the speed of the DDR3 bus being probed and the TLA configuration. Please note that hardware requirements differ depending on the speed of the DDR3 bus. For more information on the hardware requirements and setup please see Section 3.0.

Support	S/W Support	# of acq. cards	# of probes
1400MT/s or slower Read AND Write Data	B_DDR3D_2D	2 - TLA7BB4 750MHz / 1.4GHz state speed	1 - PRB1XL and 3 - PRB2XL
1400MT/s or slower Read AND Write Data	R_DDR3D_1A Reduced Module Count Support See Section 1.3	1 - TLA7BB4 750MHz / 1.4GHz state speed	4 - PRB1XL
1866MT/s or slower Read AND Write Data	B_DDR3D_4A	4 - TLA7BB4 1.4GHz state speed	1 - P6960HCD and 3 - P6962HCD
1866MT/s or slower Read AND Write Data	R_DDR3D_2A Reduced Module Count Support See Section 1.3	2 - TLA7BB4 1.4GHz state speed	4 - P6960HCD

Table 1- NEX-DDR3INTR-HS Support Software Requirements

2.2 Loading the Support into the TLA

The NEX-DDR3INTR-HS software is installed using the same method as other Windows programs. Place the NEX-DDR3INTR-HS Install CD in the CD drive of the TLA. . Using Windows Explorer select the CD, move to the support_software folder, select the folder of the support to be installed (B_DDR3D_2D, B_DDR3D_4A, R_DDR3D_1A, or R_DDR3D_2A) and then run the MSI file within the folder. The selected software will be installed on the TLA's hard disk.

To load the support into the TLA, first select the desired Logic Analyzer module (different supports require different module counts) in the Setup window, select **Load Support Package** from the **File** pull-down, then choose the name of the software package you want to load and click on **Okay**. Note that the TLA acquisition cards must be properly configured for the selected support package to load properly.

3.0 CONNECTING to the NEX-DDR3INTR-HS INTERPOSER

3.1 General

Care should be taken to support the weight of the acquisition probes so that the Logic Analyzer Interposer board and/or target DIMM socket are not damaged. *For NEX-PRB1XL/2XL probe labeling please refer to the Low Profile Probes manual (LowProfileProbes-MN-XXX) from Nexus.*

3.2 B_DDR3D_2D Support

To acquire DDR3 Read and Write data at speeds up to 1333MT/s requires two merged TLA7BB4 136-channel 750MHz or 1.4GHz acquisition cards and the B_DDR3D_2D support software. The Master card will be in the lower numbered of the two cards and the Slave card is in the adjacent high-numbered slots. The logic analyzer modules should be connected to the DDR3 DIMM Interposer as follows using (1) NEX-PRB1XL probes and three (3) NEX-PRB2XL probes:

TLA Master

Connect the NEX-PRB1XL "C" probe head to the DDR3 Interposer's LEASH (soldered-on coax cable) that is attached to the "P153/163" Coax cable on the Interposer.

Connect the NEX-PRB2XL "A3/2 & A1/0" probe head to the DDR3 Interposer's LEASH that is attached to the "P152/162" Coax cable on the Interposer.

Match the label on the end of the NEX-PRB1XL/2XL probes with the labels on the front of the Tektronix Logic Analyzer Master module and connect.

TLA Slave

Connect the NEX-PRB2XL "A3/2 & A1/0" probe head to the DDR3 Interposer's LEASH (soldered-on coax cable) that is attached to the "P154/164" Coax cable on the Interposer.

Connect the NEX-PRB2XL "C3/2 & E3/2" probe head to the DDR3 Interposer's LEASH that is attached to the "P151/161" Coax cable on the Interposer.

See *Figure 2* for connections. *Table 2* shows the Channel Grouping / Wiring for use with the B_DDR3D_2D support.

3.3 B_DDR3D_4A Support

To acquire DDR3 Read and Write data at speeds up to 1866MT/s requires four merged TLA7BB4 136-channel logic analyzer modules, each having the 1.4GHz state speed option, . Referring to *Figure 1* the Master TLA7BB4 card is in the second to lowest numbered slot

(second from the left) of the four modules; Slave Module #1 will be in the adjacent high-numbered slots; Slave Module #2 is in the lowest numbered slots; and Slave Module #3 is in the highest numbered slots.

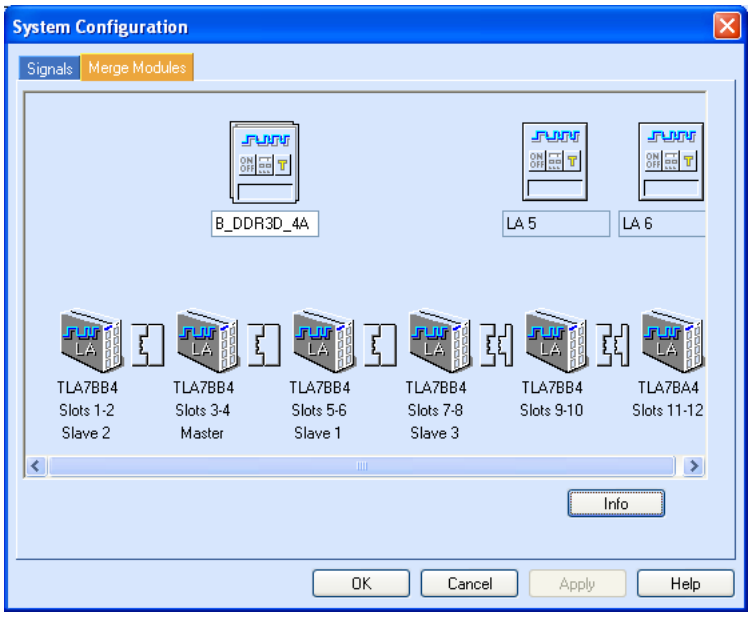

Figure 1 – 7Bx4 Merged Module Configuration

The logic analyzer modules should be connected to the DDR3 DIMM Interposer as follows using (1) Tek P6960HCD probe and three (3) Tek P6962HCD probes:

TLA Master

Connect the P6960HCD probe head to the DDR3 Interposer's LEASH (soldered-on coax cable) that is attached to the "P153/163" Coax cables on the Interposer.

Plug the 'A' TLA connector from the probe into the E3210 input of the Logic Analyzer module and then plug the 'B' TLA connector from the probe into the C3210 input of the module.

TLA Slave #1

Connect the P6962HCD probe head to the DDR3 Interposer's LEASH (soldered-on coax cable) that is attached to "P152/162" Coax Cable on the Interposer.

Plug the probe's TLA connectors into the Slave #1 acquisition module as follows:

B2 connector into the E3210 input
A1 connector into the AD32 input
A2 connector into the AD10 input
B1 connector into the C3210 input

TLA Slave #2

Connect the P6962HCD probe head to DDR3 Interposer's LEASH (soldered-on coax cable) that is attached to "P154/164" Coax Cable on the Interposer.

Plug the probe's TLA connectors into the Slave #2 acquisition module as follows:

B2 connector into the E3210 input
A1 connector into the AD32 input
A2 connector into the AD10 input
B1 connector into the C3210 input

TLA Slave #3

Connect the P6962HCD probe head to DDR3 Interposer's LEASH (soldered-on coax cable) that is attached to "P151/161" position on the Interposer.

Plug the probe's TLA connectors into the Slave #3 acquisition module as follows:

B2 connector into the E3210 input
A1 connector into the AD32 input
A2 connector into the AD10 input
B1 connector into the C3210 input

See *Figure 2* for connection information. *Table 3* shows the Channel Grouping / Wiring for use with the B_DDR3D_4A support.

3.4 R_DDR3D_1A Support (Reduced Module Count support)

To acquire DDR3 Read and Write data at speeds up to 1333MT/s requires one TLA7BB4 136-channel 750MHz or 1.4GHz acquisition card and the R_DDR3D_1A support software. The logic analyzer modules should be connected to the DDR3 DIMM Interposer as follows using (4) NEX-PRB1XL probes:

TLA Module

Connect the NEX-PRB1XL "C" probe head to the DDR3 Interposer's LEASH (soldered-on coax cable) that is attached to the "P153/163" Coax cable on the Interposer.

Connect the NEX-PRB1XL "AD3/2" probe head to the DDR3 Interposer's LEASH that is attached to the "P152/162" Coax cable on the Interposer.

Connect the NEX-PRB1XL "AD1/0" probe head to the DDR3 Interposer's LEASH (soldered-on coax cable) that is attached to the "P154/164" Coax cable on the Interposer.

Connect the NEX-PRB1XL "E" probe head to the DDR3 Interposer's LEASH that is attached to the "P151/161" Coax cable on the Interposer.

Match the label on the end of the NEX-PRB1XL probes with the labels on the front of the Tektronix Logic Analyzer Master module and connect.

See *Figure 2* for connections. *Table 4* shows the Channel Grouping / Wiring for use with the R_DDR3D_1A support.

3.5 R_DDR3D_2A Support (Reduced Module Count support)

To acquire DDR3 Read and Write data at speeds at up to 1866MT/s requires two merged TLA7BB4 136-channel logic analyzer modules, each having the 1.4GHz state speed option, and the R_DDR3D_2A support software. The Master card will be in the lower numbered of the two cards and the Slave card is in the adjacent high-numbered slots.

The logic analyzer modules should be connected to the DDR3 DIMM Interposer as follows using (4) Tek P6960HCD probes:

TLA Master/Slave

Connect the P6960HCD probe head to the DDR3 Interposer's LEASH (soldered-on coax cable) that is attached to the "P151/161" Coax cables on the Interposer.

Plug the 'A' TLA connector from the probe into the E3210 input of the Master Logic Analyzer module and then plug the 'B' TLA connector from the probe into the E3210 input of the Slave module.

Connect the P6960HCD probe head to the DDR3 Interposer's LEASH (soldered-on coax cable) that is attached to the "P152/162" Coax cables on the Interposer.

Plug the 'A' TLA connector from the probe into the AD32 input of the Master Logic Analyzer module and then plug the 'B' TLA connector from the probe into the AD32 input of the Slave module.

Connect the P6960HCD probe head to the DDR3 Interposer's LEASH (soldered-on coax cable) that is attached to the "P153/163" Coax cables on the Interposer.

Plug the 'A' TLA connector from the probe into the C3210 input of the Master Logic Analyzer module and then plug the 'B' TLA connector from the probe into the C3210 input of the Slave module.

Connect the P6960HCD probe head to the DDR3 Interposer's LEASH (soldered-on coax cable) that is attached to the "P154/164" Coax cables on the Interposer.

Plug the 'A' TLA connector from the probe into the AD10 input of the Master Logic Analyzer module and then plug the 'B' TLA connector from the probe into the AD10 input of the Slave module.

See *Figure 2* for connections. *Table 5* shows the Channel Grouping / Wiring for use with the R_DDR3D_2A support.

3.6 Short LEASH probes

The standard product includes 4 LEASH probes connected to this Interposer product. These short probes are soldered directly onto the interposer and interface the Interposer to the Passive probes that connect to the logic analyzer. These LEASH probes are to allow the user to easily install and remove the Interposer product in their system with out the added weight of the passive probe attached. There may be other probing options in the future. Contact Nexus for any updates.

Figure 2 below shows the location on the Interposer of the LEASH probe connections.

Location of HCD connectors, right under metal compression plate, and probe tip board:

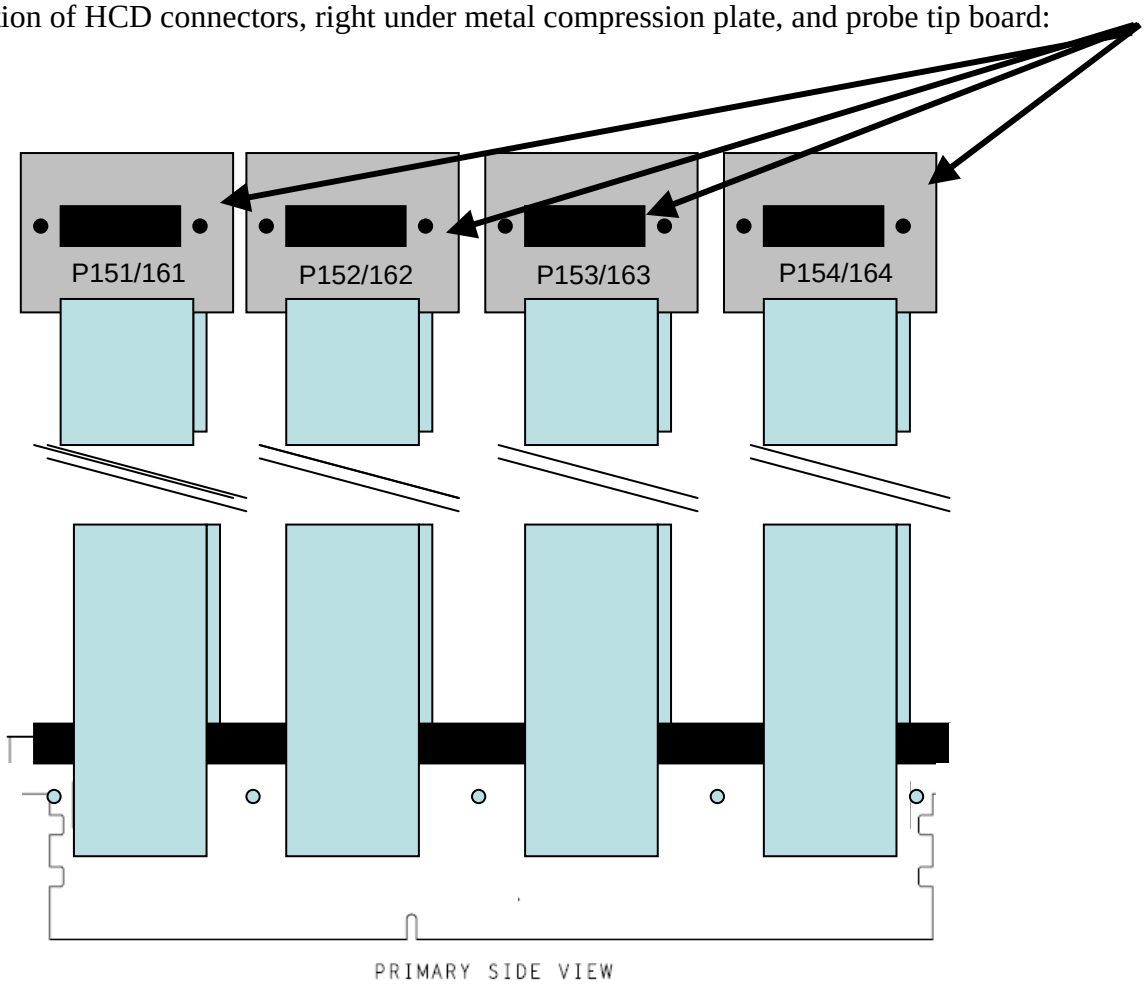

Figure 2 – Drawing of Interposer with probes attached

The four (4) each, 1 foot long, LEASH probes that are soldered onto the Interposer are in turn connected to a variety of probes listed in Sections 3.1-3.6. These probes in turn connect to the

input of the logic analyzer modules. The connection between the LEASH Probes and the logic Analyzer is an "HCD" connector with a pinout as shown below on the LEASH probe.

The strain relief on the LEASH to probe interface, while designed for bench handling, can be damaged by twisting the coax cables. Bends of over 45 degrees in this area should be avoided. The coax connection points are not to be bent under any circumstances,

3.6.1 HCD connector on the LEASH probe pins

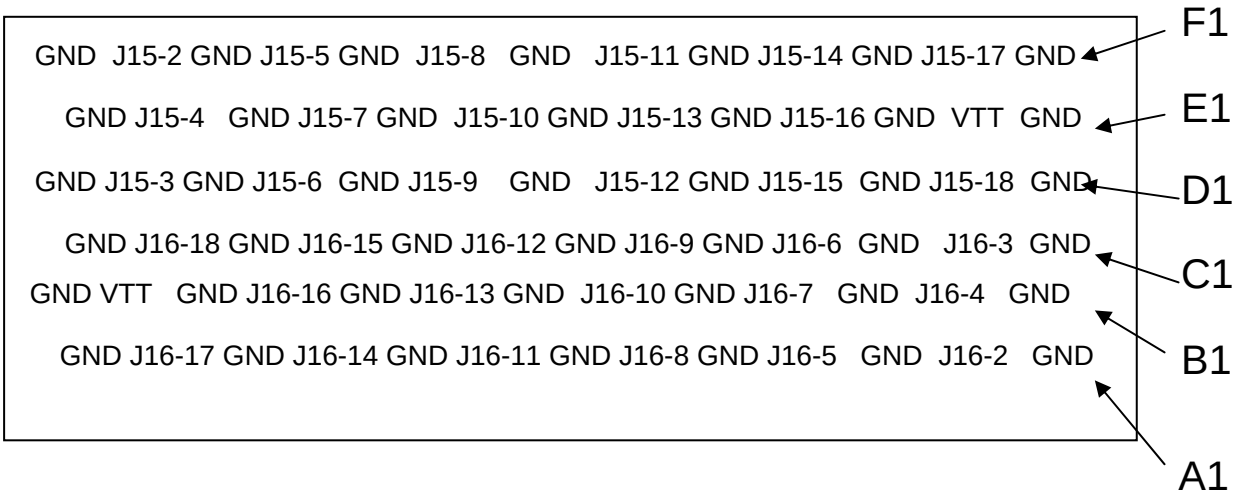

Figure 3 – HCD connector on the LEASH probe

Each LEASH probe connects to the various probes using four screws, two plates and a HCD connector. These parts are supplied.

3.6.2 LEASH probe to the various logic analyzer probes

To connect the leash to the various probes that connect to the logic analyzer follow the below diagram. Care must be taken to not brush the HCD pins sideways (gray part in drawing below). The "Top plate" will have recessed screw holes for the screw heads, and the bottom plate will have threaded screw holes. Align screw holes and guide pin holes. Tighten each screw a small amount while going to each screw in turn to maintain even force with each screw. Take care not to damage the screw heads. There is no force or torque specification for the HCDs. Reasonably tighten the screws down.

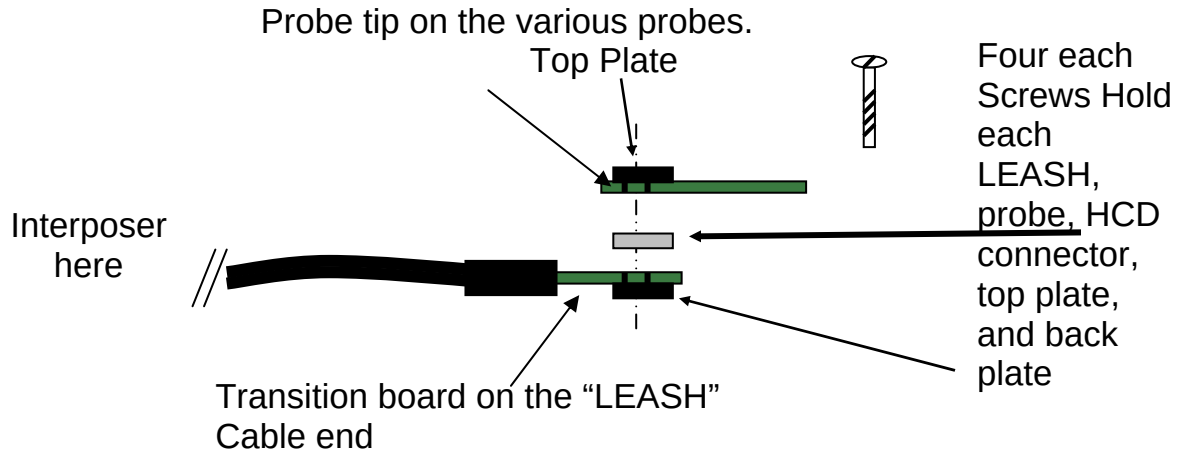

Figure 4 – LEASH probe to HCD Probe connection

3.7 Interposer location in the Target

The Interposer must be installed in the furthest slot from the memory controller.

Group Name	Signal Name	DDR3 Pin #	TLA Input	Group Name	Signal Name	DDR3 Pin #	TLA Input
RdA_DatHi (Hex)	RD_A_DQ63	234	S_A2:0	RdA_DatLo (Hex)	RD_A_DQ31	156	M_A0:6
	RD_A_DQ62	233	S_A2:1		RD_A_DQ30	155	M_A0:3
	RD_A_DQ61	228	S_A2:5		RD_A_DQ29	150	S_C2:0
	RD_A_DQ60	227	S_CK0		RD_A_DQ28	149	S_C2:1
	RD_A_DQ59	115	S_A2:2		RD_A_DQ27	37	M_A0:4
	RD_A_DQ58	114	S_A2:3		RD_A_DQ26	36	M_A0:1
	RD_A_DQ57	109	S_A2:7		RD_A_DQ25	31	S_C2:2
	RD_A_DQ56	108	S_A3:0		RD_A_DQ24	30	S_C2:3
	RD_A_DQ55	225	S_A3:2		RD_A_DQ23	147	S_C2:4
	RD_A_DQ54	224	S_A3:3		RD_A_DQ22	146	S_C2:5
	RD_A_DQ53	219	S_A3:7		RD_A_DQ21	141	S_C3:2
	RD_A_DQ52	218	S_A1:5		RD_A_DQ20	140	S_C3:3
	RD_A_DQ51	106	S_A3:1		RD_A_DQ19	28	S_C2:6
	RD_A_DQ50	105	S_A3:4		RD_A_DQ18	27	S_C2:7
	RD_A_DQ49	100	S_A1:7		RD_A_DQ17	22	S_C3:1
	RD_A_DQ48	99	S_A1:6		RD_A_DQ16	21	S_C3:4
	RD_A_DQ47	216	S_A1:4		RD_A_DQ15	138	S_C3:6
	RD_A_DQ46	215	S_A1:1		RD_A_DQ14	137	S_C3:7
	RD_A_DQ45	210	S_A0:7		RD_A_DQ13	132	S_E3:4
	RD_A_DQ44	209	S_A0:6		RD_A_DQ12	131	S_E3:1
	RD_A_DQ43	97	S_A1:3		RD_A_DQ11	19	S_C3:5
	RD_A_DQ42	96	S_A1:2		RD_A_DQ10	18	S_E3:7
	RD_A_DQ41	91	S_A0:5		RD_A_DQ9	13	S_E3:3
	RD_A_DQ40	90	S_A0:4		RD_A_DQ8	12	S_E3:2
	RD_A_DQ39	207	S_A0:3		RD_A_DQ7	129	S_E3:0
	RD_A_DQ38	206	S_A0:2		RD_A_DQ6	128	S_E2:7
	RD_A_DQ37	201	M_C2:1		RD_A_DQ5	123	S_E2:3
	RD_A_DQ36	200	M_C2:4		RD_A_DQ4	122	S_E2:2
	RD_A_DQ35	88	S_A0:1		RD_A_DQ3	10	S_Q3
	RD_A_DQ34	87	S_A0:0		RD_A_DQ2	9	S_E2:5
	RD_A_DQ33	83	M_C2:6		RD_A_DQ1	4	S_E2:1
	RD_A_DQ32	81	M_C2:7		RD_A_DQ0	3	S_E2:0

Table 2 - B_DDR3D_2D (<=1333MT/s Read and Write) Storage and Trigger Grouping

Notes:

1. All signals on this page are required for accurate post-processing of acquired data
2. The ‘S’ in front of a TLA channel denotes the Slave card of the merged pair

Group Name	Signal Name	DDR3 Pin#	TLA Input	Group Name	Signal Name	DDR3 Pin#	TLA Input
RdB_DatHi (Hex)	RD_B_DQ63	234	S_A2:0^1	RdB_DatLo (Hex)	RD_B_DQ31	156	M_A0:6^1
	RD_B_DQ62	233	S_A2:1^1		RD_B_DQ30	155	M_A0:3^1
	RD_B_DQ61	228	S_A2:5^1		RD_B_DQ29	150	S_C2:0^1
	RD_B_DQ60	227	S_CK0^1		RD_B_DQ28	149	S_C2:1^1
	RD_B_DQ59	115	S_A2:2^1		RD_B_DQ27	37	M_A0:4^1
	RD_B_DQ58	114	S_A2:3^1		RD_B_DQ26	36	M_A0:1^1
	RD_B_DQ57	109	S_A2:7^1		RD_B_DQ25	31	S_C2:2^1
	RD_B_DQ56	108	S_A3:0^1		RD_B_DQ24	30	S_C2:3^1
	RD_B_DQ55	225	S_A3:2^1		RD_B_DQ23	147	S_C2:4^1
	RD_B_DQ54	224	S_A3:3^1		RD_B_DQ22	146	S_C2:5^1
	RD_B_DQ53	219	S_A3:7^1		RD_B_DQ21	141	S_C3:2^1
	RD_B_DQ52	218	S_A1:5^1		RD_B_DQ20	140	S_C3:3^1
	RD_B_DQ51	106	S_A3:1^1		RD_B_DQ19	28	S_C2:6^1
	RD_B_DQ50	105	S_A3:4^1		RD_B_DQ18	27	S_C2:7^1
	RD_B_DQ49	100	S_A1:7^1		RD_B_DQ17	22	S_C3:1^1
	RD_B_DQ48	99	S_A1:6^1		RD_B_DQ16	21	S_C3:4^1
	RD_B_DQ47	216	S_A1:4^1		RD_B_DQ15	138	S_C3:6^1
	RD_B_DQ46	215	S_A1:1^1		RD_B_DQ14	137	S_C3:7^1
	RD_B_DQ45	210	S_A0:7^1		RD_B_DQ13	132	S_E3:4^1
	RD_B_DQ44	209	S_A0:6^1		RD_B_DQ12	131	S_E3:1^1
	RD_B_DQ43	97	S_A1:3^1		RD_B_DQ11	19	S_C3:5^1
	RD_B_DQ42	96	S_A1:2^1		RD_B_DQ10	18	S_E3:7^1
	RD_B_DQ41	91	S_A0:5^1		RD_B_DQ9	13	S_E3:3^1
	RD_B_DQ40	90	S_A0:4^1		RD_B_DQ8	12	S_E3:2^1
	RD_B_DQ39	207	S_A0:3^1		RD_B_DQ7	129	S_E3:0^1
	RD_B_DQ38	206	S_A0:2^1		RD_B_DQ6	128	S_E2:7^1
	RD_B_DQ37	201	M_C2:1^1		RD_B_DQ5	123	S_E2:3^1
	RD_B_DQ36	200	M_C2:4^1		RD_B_DQ4	122	S_E2:2^1
	RD_B_DQ35	88	S_A0:1^1		RD_B_DQ3	10	S_Q3^1
	RD_B_DQ34	87	S_A0:0^1		RD_B_DQ2	9	S_E2:5^1
	RD_B_DQ33	83	M_C2:6^1		RD_B_DQ1	4	S_E2:1^1
	RD_B_DQ32	81	M_C2:7^1		RD_B_DQ0	3	S_E2:0^1

Table 2 – B_DDR3D_2D (<=1333MT/s Read and Write) Storage and Trigger Grouping (cont'd.)

Notes:

1. All signals on this page are required for accurate post-processing of acquired data
2. The 'S' in front of a TLA channel denotes the Slave card of the merged pair
3. All signals on this page are stored in the 7Bx4's Prime memory and will not have a MagniVu display value

Group Name	Signal Name	DDR3 Pin #	TLA Input	Group Name	Signal Name	DDR3 Pin #	TLA Input
WrA_DatHi	WR_A_DQ63	234	S_D2:0	WrA_DatLo	WR_A_DQ31	156	M_D0:6
(Hex)	WR_A_DQ62	233	S_D2:1	(Hex)	WR_A_DQ30	155	M_D0:3
	WR_A_DQ61	228	S_D2:5		WR_A_DQ29	150	S_C0:0
	WR_A_DQ60	227	S_Q1		WR_A_DQ28	149	S_C0:1
	WR_A_DQ59	115	S_D2:2		WR_A_DQ27	37	M_D0:4
	WR_A_DQ58	114	S_D2:3		WR_A_DQ26	36	M_D0:1
	WR_A_DQ57	109	S_D2:7		WR_A_DQ25	31	S_C0:2
	WR_A_DQ56	108	S_D3:0		WR_A_DQ24	30	S_C0:3
	WR_A_DQ55	225	S_D3:2		WR_A_DQ23	147	S_C0:4
	WR_A_DQ54	224	S_D3:3		WR_A_DQ22	146	S_C0:5
	WR_A_DQ53	219	S_D3:7		WR_A_DQ21	141	S_C1:2
	WR_A_DQ52	218	S_D1:5		WR_A_DQ20	140	S_C1:3
	WR_A_DQ51	106	S_D3:1		WR_A_DQ19	28	S_C0:6
	WR_A_DQ50	105	S_D3:4		WR_A_DQ18	27	S_C0:7
	WR_A_DQ49	100	S_D1:7		WR_A_DQ17	22	S_C1:1
	WR_A_DQ48	99	S_D1:6		WR_A_DQ16	21	S_C1:4
	WR_A_DQ47	216	S_D1:4		WR_A_DQ15	138	S_C1:6
	WR_A_DQ46	215	S_D1:1		WR_A_DQ14	137	S_C1:7
	WR_A_DQ45	210	S_D0:7		WR_A_DQ13	132	S_E1:4
	WR_A_DQ44	209	S_D0:6		WR_A_DQ12	131	S_E1:1
	WR_A_DQ43	97	S_D1:3		WR_A_DQ11	19	S_C1:5
	WR_A_DQ42	96	S_D1:2		WR_A_DQ10	18	S_E1:7
	WR_A_DQ41	91	S_D0:5		WR_A_DQ9	13	S_E1:3
	WR_A_DQ40	90	S_D0:4		WR_A_DQ8	12	S_E1:2
	WR_A_DQ39	207	S_D0:3		WR_A_DQ7	129	S_E1:0
	WR_A_DQ38	206	S_D0:2		WR_A_DQ6	128	S_E0:7
	WR_A_DQ37	201	M_C0:1		WR_A_DQ5	123	S_E0:3
	WR_A_DQ36	200	M_C0:4		WR_A_DQ4	122	S_E0:2
	WR_A_DQ35	88	S_D0:1		WR_A_DQ3	10	S_CK2
	WR_A_DQ34	87	S_D0:0		WR_A_DQ2	9	S_E0:5
	WR_A_DQ33	83	M_C0:6		WR_A_DQ1	4	S_E0:1
	WR_A_DQ32	81	M_C0:7		WR_A_DQ0	3	S_E0:0

Table 2 – B_DDR3D_2D (<=1333MT/s Read and Write) Storage and Trigger Grouping (cont'd.)

Notes:

1. All signals on this page are required for accurate post-processing of acquired data
2. The 'M' in front of a TLA channel denotes the Master card of the merged pair
3. The 'S' in front of a TLA channel denotes the Slave card of the merged pair

Group Name	Signal Name	DDR3 Pin #	TLA Input	Group Name	Signal Name	DDR3 Pin #	TLA Input
WrB_DatHi	WR_B_DQ63	234	S_D2:0^1	WrB_DatLo	WR_B_DQ31	156	M_D0:6^1
(Hex)	WR_B_DQ62	233	S_D2:1^1	(Hex)	WR_B_DQ30	155	M_D0:3^1
	WR_B_DQ61	228	S_D2:5^1		WR_B_DQ29	150	S_C0:0^1
	WR_B_DQ60	227	S_Q1^1		WR_B_DQ28	149	S_C0:1^1
	WR_B_DQ59	115	S_D2:2^1		WR_B_DQ27	37	M_D0:4^1
	WR_B_DQ58	114	S_D2:3^1		WR_B_DQ26	36	M_D0:1^1
	WR_B_DQ57	109	S_D2:7^1		WR_B_DQ25	31	S_C0:2^1
	WR_B_DQ56	108	S_D3:0^1		WR_B_DQ24	30	S_C0:3^1
	WR_B_DQ55	225	S_D3:2^1		WR_B_DQ23	147	S_C0:4^1
	WR_B_DQ54	224	S_D3:3^1		WR_B_DQ22	146	S_C0:5^1
	WR_B_DQ53	219	S_D3:7^1		WR_B_DQ21	141	S_C1:2^1
	WR_B_DQ52	218	S_D1:5^1		WR_B_DQ20	140	S_C1:3^1
	WR_B_DQ51	106	S_D3:1^1		WR_B_DQ19	28	S_C0:6^1
	WR_B_DQ50	105	S_D3:4^1		WR_B_DQ18	27	S_C0:7^1
	WR_B_DQ49	100	S_D1:7^1		WR_B_DQ17	22	S_C1:1^1
	WR_B_DQ48	99	S_D1:6^1		WR_B_DQ16	21	S_C1:4^1
	WR_B_DQ47	216	S_D1:4^1		WR_B_DQ15	138	S_C1:6^1
	WR_B_DQ46	215	S_D1:1^1		WR_B_DQ14	137	S_C1:7^1
	WR_B_DQ45	210	S_D0:7^1		WR_B_DQ13	132	S_E1:4^1
	WR_B_DQ44	209	S_D0:6^1		WR_B_DQ12	131	S_E1:1^1
	WR_B_DQ43	97	S_D1:3^1		WR_B_DQ11	19	S_C1:5^1
	WR_B_DQ42	96	S_D1:2^1		WR_B_DQ10	18	S_E1:7^1
	WR_B_DQ41	91	S_D0:5^1		WR_B_DQ9	13	S_E1:3^1
	WR_B_DQ40	90	S_D0:4^1		WR_B_DQ8	12	S_E1:2^1
	WR_B_DQ39	207	S_D0:3^1		WR_B_DQ7	129	S_E1:0^1
	WR_B_DQ38	206	S_D0:2^1		WR_B_DQ6	128	S_E0:7^1
	WR_B_DQ37	201	M_C0:1^1		WR_B_DQ5	123	S_E0:3^1
	WR_B_DQ36	200	M_C0:4^1		WR_B_DQ4	122	S_E0:2^1
	WR_B_DQ35	88	S_D0:1^1		WR_B_DQ3	10	S_CK2^1
	WR_B_DQ34	87	S_D0:0^1		WR_B_DQ2	9	S_E0:5^1
	WR_B_DQ32	83	M_C0:6^1		WR_B_DQ1	4	S_E0:1^1
	WR_B_DQ33	81	M_C0:7^1		WR_B_DQ0	3	S_E0:0^1

Table 2 – B_DDR3D_2D (<=1333MT/s Read and Write) Storage and Trigger Grouping (cont'd.)

Notes:

1. All signals on this page are required for accurate post-processing of acquired data
2. The 'M' in front of a TLA channel denotes the Master card of the merged pair
3. The 'S' in front of a TLA channel denotes the Slave card of the merged pair
4. All signals on this page are stored in the 7Bx4's Prime memory and will not have a MagniVu display value

Group Name	Signal Name	DDR3 Pin #	TLA Input	Group Name	Signal Name	DDR3 Pin #	TLA Input
RdAChkBits	RD_A_CB7	165	M_A1:5	WrAChkBits [4]	WR_A_CB7	165	M_D1:5
(OFF)	RD_A_CB6	164	M_A1:4	(OFF)	WR_A_CB6	164	M_D1:4
	RD_A_CB5	159	M_A1:0		WR_A_CB5	159	M_D1:0
	RD_A_CB4	158	M_A0:7		WR_A_CB4	158	M_D0:7
	RD_A_CB3	46	M_A1:6		WR_A_CB3	46	M_D1:6
	RD_A_CB2	45	M_A1:3		WR_A_CB2	45	M_D1:3
	RD_A_CB1	40	M_CK1		WR_A_CB1	40	M_Q0
	RD_A_CB0	39	M_A0:5		WR_A_CB0	39	M_D0:5
RdBChkBits [4]	RD_B_CB7	165	M_A1:5^1	WrBChkBits [4]	WR_B_CB7	165	M_D1:5^1
(OFF)	RD_B_CB6	164	M_A1:4^1	(OFF)	WR_B_CB6	164	M_D1:4^1
	RD_B_CB5	159	M_A1:0^1		WR_B_CB5	159	M_D1:0^1
	RD_B_CB4	158	M_A0:7^1		WR_B_CB4	158	M_D0:7^1
	RD_B_CB3	46	M_A1:6^1		WR_B_CB3	46	M_D1:6^1
	RD_B_CB2	45	M_A1:3^1		WR_B_CB2	45	M_D1:3^1
	RD_B_CB1	40	M_CK1^1		WR_B_CB1	40	M_Q0^1
	RD_B_CB0	39	M_A0:5^1		WR_B_CB0	39	M_D0:5^1
ADatMsks	A_DM7	230	S_A2:4	BDatMsks [4]	B_DM7	230	S_A2:4^1
(BIN)	A_DM6	221	S_A3:6	(BIN)	B_DM6	221	S_A3:6^1
	A_DM5	212	S_A1:0		B_DM5	212	S_A1:0^1
	A_DM4	203	M_C2:0		B_DM4	203	M_C2:0^1
	A_DM3	152	M_A0:2		B_DM3	152	M_A0:2^1
	A_DM2	143	S_CK3		B_DM2	143	S_CK3^1
	A_DM1	134	S_E3:5		B_DM1	134	S_E3:5^1
	A_DM0	125	S_E2:6		B_DM0	125	S_E2:6^1

Table 2 – B_DDR3D_2D (<=1333MT/s Read and Write) Storage and Trigger Grouping (cont'd.)

Notes:

1. ' # ' denotes a low-true signal
2. The 'M' in front of a TLA channel denotes the Master card of the merged pair
3. The 'S' in front of a TLA channel denotes the Slave card of the merged set
4. Signals in these groups are acquired using the 7Bx4's demux capability and will not have a MagniVu display value

Group Name	Signal Name	DDR3 Pin #	TLA Input
Control [2] (SYM)	CKE1	169	M_A3:2
	CKE0	50	M_A3:1
	S3#	49	M_C2:5
	S2#	48	M_C3:0
	S1#	76	M_C3:4
	S0#	193	M_C3:3
	BA2	52	M_A3:0
	BA1	190	M_C3:7
	BA0	71	M_C1:6
	A15	171	M_CK0
	A14	172	M_A2:5
	A13	196	M_CK3
	A12/BC#	174	M_A2:4
	A10/AP	70	M_C1:3
	RAS#	192	M_C3:6
	CAS#	74	M_C3:5
	WE#	73	M_C1:7
Strobes (HEX)	DQS7	111	S_A2:6
	DQS6	103	S_A3:5
	DQS5	94	S_CK1
	DQS4	85	M_C2:3
	DQS3	34	M_A0:1
	DQS2	25	S_C3:0
	DQS1	16	S_E3:6
	DQS0	7	S_E2:4

Group Name	Signal Name	DDR3 Pin #	TLA Input
Address [2] (Hex)	BA2	52	M_A3:0
	BA1	190	M_C3:7
	BA0	71	M_C1:6
	A15	171	M_CK0
	A14	172	M_A2:5
	A13	196	M_CK3
	A12/BC#	174	M_A2:4
	A11	55	M_A2:6
	A10/AP	70	M_C1:3
	A9	175	M_A2:1
	A8	177	M_A2:0
	A7	56	M_A2:3
	A6	178	M_C0:2
	A5	58	M_A2:2
	A4	59	M_C0:5
	A3	180	M_C1:0
	A2	61	M_Q1
	A1	181	M_C1:1
	A0	188	M_C1:5
Misc [2] (OFF)	MISC1	Placeholder	
	MISC0	Placeholder	
	DDRCK0	184	M_C1:4
Ungrouped	DQS8	43	M_A1:2
	DM8	161	M_A1:1
	ERR_OUT#[3]	53	M_A2:7
	RESET#	168	M_A3:6
	TEST	167	M_A3:7
	ODT0	195	M_C2:0
	ODT1	77	M_C2:1
	PAR_IN	68	M_C1:2

Table 2 – B_DDR3D_2D (<=1333MT/s Read and Write) Storage and Trigger Grouping (cont'd.)

Notes:

1. ' # ' denotes a low-true signal
2. These signals are required for accurate acquisition and post-processing of acquired data
3. The 'M' in front of a TLA channel denotes the Master card of the merged pair
4. The 'S' in front of a TLA channel denotes the Slave card of the merged pair
5. Signals in these groups are acquired using the 7Bx4's demux capability and will not have a MagniVu display value

Group Name	Signal Name	DDR3 Pin #	TLA Input	Group Name	Signal Name	DDR3 Pin #	TLA Input
RdADatHi	RD_A_DQ63	234	S2_A0:0	RdADatLo	RD_A_DQ31	156	S_A2:6
(Hex)	RD_A_DQ62	233	S2_A0:1	(Hex)	RD_A_DQ30	155	S_A2:3
	RD_A_DQ61	228	S2_A0:5		RD_A_DQ29	150	S3_A0:0
	RD_A_DQ60	227	S2_CK1		RD_A_DQ28	149	S3_A0:1
	RD_A_DQ59	115	S2_A0:2		RD_A_DQ27	37	S_A2:4
	RD_A_DQ58	114	S2_A0:3		RD_A_DQ26	36	S_A2:1
	RD_A_DQ57	109	S2_A0:7		RD_A_DQ25	31	S3_A0:2
	RD_A_DQ56	108	S2_A1:0		RD_A_DQ24	30	S3_A0:3
	RD_A_DQ55	225	S2_A1:2		RD_A_DQ23	147	S3_A0:4
	RD_A_DQ54	224	S2_A1:3		RD_A_DQ22	146	S3_A0:5
	RD_A_DQ53	219	S2_A1:7		RD_A_DQ21	141	S3_A1:2
	RD_A_DQ52	218	S2_A3:5		RD_A_DQ20	140	S3_A1:3
	RD_A_DQ51	106	S2_A1:1		RD_A_DQ19	28	S3_A0:6
	RD_A_DQ50	105	S2_A1:4		RD_A_DQ18	27	S3_A0:7
	RD_A_DQ49	100	S2_A3:7		RD_A_DQ17	22	S3_A1:1
	RD_A_DQ48	99	S2_A3:6		RD_A_DQ16	21	S3_A1:4
	RD_A_DQ47	216	S2_A3:4		RD_A_DQ15	138	S3_A1:6
	RD_A_DQ46	215	S2_A3:1		RD_A_DQ14	137	S3_A1:7
	RD_A_DQ45	210	S2_A2:7		RD_A_DQ13	132	S3_A3:4
	RD_A_DQ44	209	S2_A2:6		RD_A_DQ12	131	S3_A3:1
	RD_A_DQ43	97	S2_A3:3		RD_A_DQ11	19	S3_A1:5
	RD_A_DQ42	96	S2_A3:2		RD_A_DQ10	18	S3_A3:7
	RD_A_DQ41	91	S2_A2:5		RD_A_DQ9	13	S3_A3:3
	RD_A_DQ40	90	S2_A2:4		RD_A_DQ8	12	S3_A3:2
	RD_A_DQ39	207	S2_A2:3		RD_A_DQ7	129	S3_A3:0
	RD_A_DQ38	206	S2_A2:2		RD_A_DQ6	128	S3_A2:7
	RD_A_DQ37	201	M_C2:1		RD_A_DQ5	123	S3_A2:3
	RD_A_DQ36	200	M_C2:4		RD_A_DQ4	122	S3_A2:2
	RD_A_DQ35	88	S2_A2:1		RD_A_DQ3	10	S3_CK0
	RD_A_DQ34	87	S2_A2:0		RD_A_DQ2	9	S3_A2:5
	RD_A_DQ33	83	M_C2:6		RD_A_DQ1	4	S3_A2:1
	RD_A_DQ32	81	M_C2:7		RD_A_DQ0	3	S3_A2:0

Table 3 - B_DDR3D_4D (<=1866MT/s Read and Write) Storage and Trigger Grouping

Notes:

1. All signals on this page are required for accurate post-processing of acquired data
2. The ‘M’ in front of a TLA channel denotes the Master card of the merged set
3. The ‘S’ in front of a TLA channel denotes Slave card #1 of the merged set
4. The ‘S2’ in front of a TLA channel denotes Slave card #2 of the merged set
5. The ‘S3’ in front of a TLA channel denotes Slave card #3 of the merged set

Group Name	Signal Name	DDR3 Pin#	TLA Input	Group Name	Signal Name	DDR3 Pin#	TLA Input
RdBDatHi	RD_B_DQ63	234	S2_D0:0	RdBDatLo	RD_B_DQ31	156	S_D2:6
(Hex)	RD_B_DQ62	233	S2_D0:1	(Hex)	RD_B_DQ30	155	S_D2:3
	RD_B_DQ61	228	S2_D0:5		RD_B_DQ29	150	S3_D0:0
	RD_B_DQ60	227	S2_Q0		RD_B_DQ28	149	S3_D0:1
	RD_B_DQ59	115	S2_D0:2		RD_B_DQ27	37	S_D2:4
	RD_B_DQ58	114	S2_D0:3		RD_B_DQ26	36	S_D2:1
	RD_B_DQ57	109	S2_D0:7		RD_B_DQ25	31	S3_D0:2
	RD_B_DQ56	108	S2_D1:0		RD_B_DQ24	30	S3_D0:3
	RD_B_DQ55	225	S2_D1:2		RD_B_DQ23	147	S3_D0:4
	RD_B_DQ54	224	S2_D1:3		RD_B_DQ22	146	S3_D0:5
	RD_B_DQ53	219	S2_D1:7		RD_B_DQ21	141	S3_D1:2
	RD_B_DQ52	218	S2_D3:5		RD_B_DQ20	140	S3_D1:3
	RD_B_DQ51	106	S2_D1:1		RD_B_DQ19	28	S3_D0:6
	RD_B_DQ50	105	S2_D1:4		RD_B_DQ18	27	S3_D0:7
	RD_B_DQ49	100	S2_D3:7		RD_B_DQ17	22	S3_D1:1
	RD_B_DQ48	99	S2_D3:6		RD_B_DQ16	21	S3_D1:4
	RD_B_DQ47	216	S2_D3:4		RD_B_DQ15	138	S3_D1:6
	RD_B_DQ46	215	S2_D3:1		RD_B_DQ14	137	S3_D1:7
	RD_B_DQ45	210	S2_D2:7		RD_B_DQ13	132	S3_D3:4
	RD_B_DQ44	209	S2_D2:6		RD_B_DQ12	131	S3_D3:1
	RD_B_DQ43	97	S2_D3:3		RD_B_DQ11	19	S3_D1:5
	RD_B_DQ42	96	S2_D3:2		RD_B_DQ10	18	S3_D3:7
	RD_B_DQ41	91	S2_D2:5		RD_B_DQ9	13	S3_D3:3
	RD_B_DQ40	90	S2_D2:4		RD_B_DQ8	12	S3_D3:2
	RD_B_DQ39	207	S2_D2:3		RD_B_DQ7	129	S3_D3:0
	RD_B_DQ38	206	S2_D2:2		RD_B_DQ6	128	S3_D2:7
	RD_B_DQ37	201	M_C0:1		RD_B_DQ5	123	S3_D2:3
	RD_B_DQ36	200	M_C0:4		RD_B_DQ4	122	S3_D2:2
	RD_B_DQ35	88	S2_D2:1		RD_B_DQ3	10	S3_Q1
	RD_B_DQ34	87	S2_D2:0		RD_B_DQ2	9	S3_D2:5
	RD_B_DQ33	83	M_C0:6		RD_B_DQ1	4	S3_D2:1
	RD_B_DQ32	81	M_C0:7		RD_B_DQ0	3	S3_D2:0

Table 3 – B_DDR3D_4D (<=1866MT/s Read and Write) Storage and Trigger Grouping (cont'd.)

Notes:

1. All signals on this page are required for accurate post-processing of acquired data
2. The 'M' in front of a TLA channel denotes the Master card of the merged set
3. The 'S' in front of a TLA channel denotes Slave card #1 of the merged set
4. The 'S2' in front of a TLA channel denotes Slave card #2 of the merged set
5. The 'S3' in front of a TLA channel denotes Slave card #3 of the merged set
6. Signals in these groups are acquired using the 7Bx4's demux capability and will not have a MagniVu display value

Group Name	Signal Name	DDR3 Pin #	TLA Input	Group Name	Signal Name	DDR3 Pin #	TLA Input
RdCDatHi	RD_C_DQ63	234	S2_A0:0^1	RdCDatLo	RD_C_DQ31	156	S_A2:6^1
(Hex)	RD_C_DQ62	233	S2_A0:1^1	(Hex)	RD_C_DQ30	155	S_A2:3^1
	RD_C_DQ61	228	S2_A0:5^1		RD_C_DQ29	150	S3_A0:0^1
	RD_C_DQ60	227	S2_CK1^1		RD_C_DQ28	149	S3_A0:1^1
	RD_C_DQ59	115	S2_A0:2^1		RD_C_DQ27	37	S_A2:4^1
	RD_C_DQ58	114	S2_A0:3^1		RD_C_DQ26	36	S_A2:1^1
	RD_C_DQ57	109	S2_A0:7^1		RD_C_DQ25	31	S3_A0:2^1
	RD_C_DQ56	108	S2_A1:0^1		RD_C_DQ24	30	S3_A0:3^1
	RD_C_DQ55	225	S2_A1:2^1		RD_C_DQ23	147	S3_A0:4^1
	RD_C_DQ54	224	S2_A1:3^1		RD_C_DQ22	146	S3_A0:5^1
	RD_C_DQ53	219	S2_A1:7^1		RD_C_DQ21	141	S3_A1:2^1
	RD_C_DQ52	218	S2_A3:5^1		RD_C_DQ20	140	S3_A1:3^1
	RD_C_DQ51	106	S2_A1:1^1		RD_C_DQ19	28	S3_A0:6^1
	RD_C_DQ50	105	S2_A1:4^1		RD_C_DQ18	27	S3_A0:7^1
	RD_C_DQ49	100	S2_A3:7^1		RD_C_DQ17	22	S3_A1:1^1
	RD_C_DQ48	99	S2_A3:6^1		RD_C_DQ16	21	S3_A1:4^1
	RD_C_DQ47	216	S2_A3:4^1		RD_C_DQ15	138	S3_A1:6^1
	RD_C_DQ46	215	S2_A3:1^1		RD_C_DQ14	137	S3_A1:7^1
	RD_C_DQ45	210	S2_A2:7^1		RD_C_DQ13	132	S3_A3:4^1
	RD_C_DQ44	209	S2_A2:6^1		RD_C_DQ12	131	S3_A3:1^1
	RD_C_DQ43	97	S2_A3:3^1		RD_C_DQ11	19	S3_A1:5^1
	RD_C_DQ42	96	S2_A3:2^1		RD_C_DQ10	18	S3_A3:7^1
	RD_C_DQ41	91	S2_A2:5^1		RD_C_DQ9	13	S3_A3:3^1
	RD_C_DQ40	90	S2_A2:4^1		RD_C_DQ8	12	S3_A3:2^1
	RD_C_DQ39	207	S2_A2:3^1		RD_C_DQ7	129	S3_A3:0^1
	RD_C_DQ38	206	S2_A2:2^1		RD_C_DQ6	128	S3_A2:7^1
	RD_C_DQ37	201	M_C2:1^1		RD_C_DQ5	123	S3_A2:3^1
	RD_C_DQ36	200	M_C2:4^1		RD_C_DQ4	122	S3_A2:2^1
	RD_C_DQ35	88	S2_A2:1^1		RD_C_DQ3	10	S3_CK0^1
	RD_C_DQ34	87	S2_A2:0^1		RD_C_DQ2	9	S3_A2:5^1
	RD_C_DQ33	83	M_C2:6^1		RD_C_DQ1	4	S3_A2:1^1
	RD_C_DQ32	81	M_C2:7^1		RD_C_DQ0	3	S3_A2:0^1

Table 3 – B_DDR3D_4D (<=1866MT/s Read and Write) Storage and Trigger Grouping (cont'd.)

Notes:

1. All signals on this page are required for accurate post-processing of acquired data
2. The 'M' in front of a TLA channel denotes the Master card of the merged set
3. The 'S' in front of a TLA channel denotes Slave card #1 of the merged set
4. The 'S2' in front of a TLA channel denotes Slave card #2 of the merged set
5. The 'S3' in front of a TLA channel denotes Slave card #3 of the merged set
6. All signals on this page are stored in the 7Bx4's Prime memory and will not have a MagniVu display value

Group Name	Signal Name	DDR3 Pin#	TLA Input	Group Name	Signal Name	DDR3 Pin#	TLA Input
RdDDatHi	RD_D_DQ63	234	S2_D0:0^1	RdDDatLo	RD_D_DQ31	156	S_D2:6^1
(Hex)	RD_D_DQ62	233	S2_D0:1^1	(Hex)	RD_D_DQ30	155	S_D2:3^1
	RD_D_DQ61	228	S2_D0:5^1		RD_D_DQ29	150	S3_D0:0^1
	RD_D_DQ60	227	S2_Q0^1		RD_D_DQ28	149	S3_D0:1^1
	RD_D_DQ59	115	S2_D0:2^1		RD_D_DQ27	37	S_D2:4^1
	RD_D_DQ58	114	S2_D0:3^1		RD_D_DQ26	36	S_D2:1^1
	RD_D_DQ57	109	S2_D0:7^1		RD_D_DQ25	31	S3_D0:2^1
	RD_D_DQ56	108	S2_D1:0^1		RD_D_DQ24	30	S3_D0:3^1
	RD_D_DQ55	225	S2_D1:2^1		RD_D_DQ23	147	S3_D0:4^1
	RD_D_DQ54	224	S2_D1:3^1		RD_D_DQ22	146	S3_D0:5^1
	RD_D_DQ53	219	S2_D1:7^1		RD_D_DQ21	141	S3_D1:2^1
	RD_D_DQ52	218	S2_D3:5^1		RD_D_DQ20	140	S3_D1:3^1
	RD_D_DQ51	106	S2_D1:1^1		RD_D_DQ19	28	S3_D0:6^1
	RD_D_DQ50	105	S2_D1:4^1		RD_D_DQ18	27	S3_D0:7^1
	RD_D_DQ49	100	S2_D3:7^1		RD_D_DQ17	22	S3_D1:1^1
	RD_D_DQ48	99	S2_D3:6^1		RD_D_DQ16	21	S3_D1:4^1
	RD_D_DQ47	216	S2_D3:4^1		RD_D_DQ15	138	S3_D1:6^1
	RD_D_DQ46	215	S2_D3:1^1		RD_D_DQ14	137	S3_D1:7^1
	RD_D_DQ45	210	S2_D2:7^1		RD_D_DQ13	132	S3_D3:4^1
	RD_D_DQ44	209	S2_D2:6^1		RD_D_DQ12	131	S3_D3:1^1
	RD_D_DQ43	97	S2_D3:3^1		RD_D_DQ11	19	S3_D1:5^1
	RD_D_DQ42	96	S2_D3:2^1		RD_D_DQ10	18	S3_D3:7^1
	RD_D_DQ41	91	S2_D2:5^1		RD_D_DQ9	13	S3_D3:3^1
	RD_D_DQ40	90	S2_D2:4^1		RD_D_DQ8	12	S3_D3:2^1
	RD_D_DQ39	207	S2_D2:3^1		RD_D_DQ7	129	S3_D3:0^1
	RD_D_DQ38	206	S2_D2:2^1		RD_D_DQ6	128	S3_D2:7^1
	RD_D_DQ37	201	M_C0:1^1		RD_D_DQ5	123	S3_D2:3^1
	RD_D_DQ36	200	M_C0:4^1		RD_D_DQ4	122	S3_D2:2^1
	RD_D_DQ35	88	S2_D2:1^1		RD_D_DQ3	10	S3_Q1^1
	RD_D_DQ34	87	S2_D2:0^1		RD_D_DQ2	9	S3_D2:5^1
	RD_D_DQ33	83	M_C0:6^1		RD_D_DQ1	4	S3_D2:1^1
	RD_D_DQ32	81	M_C0:7^1		RD_D_DQ0	3	S3_D2:0^1

Table 3 – B_DDR3D_4D (<=1866MT/s Read and Write) Storage and Trigger Grouping (cont'd.)

Notes:

1. All signals on this page are required for accurate post-processing of acquired data
2. The 'M' in front of a TLA channel denotes the Master card of the merged set
3. The 'S' in front of a TLA channel denotes Slave card #1 of the merged set
4. The 'S2' in front of a TLA channel denotes Slave card #2 of the merged set
5. The 'S3' in front of a TLA channel denotes Slave card #3 of the merged set
6. All signals on this page are stored in the 7Bx4's Prime memory and will not have a MagniVu display value

Group Name	Signal Name	DDR3 Pin #	TLA Input	Group Name	Signal Name	DDR3 Pin #	TLA Input
Wr_ADatHi	WR_A_DQ63	234	S2_E2:0	Wr_ADatLo	WR_A_DQ31	156	S_A2:6
(Hex)	WR_A_DQ62	233	S2_E2:1	(Hex)	WR_A_DQ30	155	S_A2:3
	WR_A_DQ61	228	S2_E2:5		WR_A_DQ29	150	S3_E2:0
	WR_A_DQ60	227	S2_Q3		WR_A_DQ28	149	S3_E2:1
	WR_A_DQ59	115	S2_E2:2		WR_A_DQ27	37	S_A2:4
	WR_A_DQ58	114	S2_E2:3		WR_A_DQ26	36	S_A2:1
	WR_A_DQ57	109	S2_E2:7		WR_A_DQ25	31	S3_E2:2
	WR_A_DQ56	108	S2_E3:0		WR_A_DQ24	30	S3_E2:3
	WR_A_DQ55	225	S2_E3:2		WR_A_DQ23	147	S3_E2:4
	WR_A_DQ54	224	S2_E3:3		WR_A_DQ22	146	S3_E2:5
	WR_A_DQ53	219	S2_E3:7		WR_A_DQ21	141	S3_E3:2
	WR_A_DQ52	218	S2_C3:5		WR_A_DQ20	140	S3_E3:3
	WR_A_DQ51	106	S2_E3:1		WR_A_DQ19	28	S3_E2:6
	WR_A_DQ50	105	S2_E3:4		WR_A_DQ18	27	S3_E2:7
	WR_A_DQ49	100	S2_C3:7		WR_A_DQ17	22	S3_E3:1
	WR_A_DQ48	99	S2_C3:6		WR_A_DQ16	21	S3_E3:4
	WR_A_DQ47	216	S2_C3:4		WR_A_DQ15	138	S3_E3:6
	WR_A_DQ46	215	S2_C3:1		WR_A_DQ14	137	S3_E3:7
	WR_A_DQ45	210	S2_C2:7		WR_A_DQ13	132	S3_C3:4
	WR_A_DQ44	209	S2_C2:6		WR_A_DQ12	131	S3_C3:1
	WR_A_DQ43	97	S2_C3:3		WR_A_DQ11	19	S3_E3:5
	WR_A_DQ42	96	S2_C3:2		WR_A_DQ10	18	S3_C3:7
	WR_A_DQ41	91	S2_C2:5		WR_A_DQ9	13	S3_C3:3
	WR_A_DQ40	90	S2_C2:4		WR_A_DQ8	12	S3_C3:2
	WR_A_DQ39	207	S2_C2:3		WR_A_DQ7	129	S3_C3:0
	WR_A_DQ38	206	S2_C2:2		WR_A_DQ6	128	S3_C2:7
	WR_A_DQ37	201	M_E2:1		WR_A_DQ5	123	S3_C2:3
	WR_A_DQ36	200	M_E2:4		WR_A_DQ4	122	S3_C2:2
	WR_A_DQ35	88	S2_C2:1		WR_A_DQ3	10	S3_CK3
	WR_A_DQ34	87	S2_C2:0		WR_A_DQ2	9	S3_C2:5
	WR_A_DQ33	83	M_E2:6		WR_A_DQ1	4	S3_C2:1
	WR_A_DQ32	81	M_E2:7		WR_A_DQ0	3	S3_C2:0

Table 3 – B_DDR3D_4D (<=1866MT/s Read and Write) Storage and Trigger Grouping (cont'd.)

Notes:

1. All signals on this page are required for accurate post-processing of acquired data
2. The 'M' in front of a TLA channel denotes the Master card of the merged set
3. The 'S' in front of a TLA channel denotes Slave card #1 of the merged set
4. The 'S2' in front of a TLA channel denotes Slave card #2 of the merged set
5. The 'S3' in front of a TLA channel denotes Slave card #3 of the merged set

Group Name	Signal Name	DDR3 Pin #	TLA Input	Group Name	Signal Name	DDR3 Pin #	TLA Input
Wr_BDatHi	WR_B_DQ63	234	S2_E0:0	Wr_BDatLo	WR_B_DQ31	156	S_D2:6
(Hex)	WR_B_DQ62	233	S2_E0:1	(Hex)	WR_B_DQ30	155	S_D2:3
	WR_B_DQ61	228	S2_E0:5		WR_B_DQ29	150	S3_E0:0
	WR_B_DQ60	227	S2_CK2		WR_B_DQ28	149	S3_E0:1
	WR_B_DQ59	115	S2_E0:2		WR_B_DQ27	37	S_D2:4
	WR_B_DQ58	114	S2_E0:3		WR_B_DQ26	36	S_D2:1
	WR_B_DQ57	109	S2_E0:7		WR_B_DQ25	31	S3_E0:2
	WR_B_DQ56	108	S2_E1:0		WR_B_DQ24	30	S3_E0:3
	WR_B_DQ55	225	S2_E1:2		WR_B_DQ23	147	S3_E0:4
	WR_B_DQ54	224	S2_E1:3		WR_B_DQ22	146	S3_E0:5
	WR_B_DQ53	219	S2_E1:7		WR_B_DQ21	141	S3_E1:2
	WR_B_DQ52	218	S2_C1:5		WR_B_DQ20	140	S3_E1:3
	WR_B_DQ51	106	S2_E1:1		WR_B_DQ19	28	S3_E0:6
	WR_B_DQ50	105	S2_E1:4		WR_B_DQ18	27	S3_E0:7
	WR_B_DQ49	100	S2_C1:7		WR_B_DQ17	22	S3_E1:1
	WR_B_DQ48	99	S2_C1:6		WR_B_DQ16	21	S3_E1:4
	WR_B_DQ47	216	S2_C1:4		WR_B_DQ15	138	S3_E1:6
	WR_B_DQ46	215	S2_C1:1		WR_B_DQ14	137	S3_E1:7
	WR_B_DQ45	210	S2_C0:7		WR_B_DQ13	132	S3_C1:4
	WR_B_DQ44	209	S2_C0:6		WR_B_DQ12	131	S3_C1:1
	WR_B_DQ43	97	S2_C1:3		WR_B_DQ11	19	S3_E1:5
	WR_B_DQ42	96	S2_C1:2		WR_B_DQ10	18	S3_C1:7
	WR_B_DQ41	91	S2_C0:5		WR_B_DQ9	13	S3_C1:3
	WR_B_DQ40	90	S2_C0:4		WR_B_DQ8	12	S3_C1:2
	WR_B_DQ39	207	S2_C0:3		WR_B_DQ7	129	S3_C1:0
	WR_B_DQ38	206	S2_C0:2		WR_B_DQ6	128	S3_C0:7
	WR_B_DQ37	201	M_E0:1		WR_B_DQ5	123	S3_C0:3
	WR_B_DQ36	200	M_E0:4		WR_B_DQ4	122	S3_C0:2
	WR_B_DQ35	88	S2_C0:1		WR_B_DQ3	10	S3_Q2
	WR_B_DQ34	87	S2_C0:0		WR_B_DQ2	9	S3_C0:5
	WR_B_DQ32	83	M_E0:6		WR_B_DQ1	4	S3_C0:1
	WR_B_DQ33	81	M_E0:7		WR_B_DQ0	3	S3_C0:0

Table 3 – B_DDR3D_4D (<=1866MT/s Read and Write) Storage and Trigger Grouping (cont'd.)

Notes:

1. All signals on this page are required for accurate post-processing of acquired data
2. The 'M' in front of a TLA channel denotes the Master card of the merged set
3. The 'S' in front of a TLA channel denotes Slave card #1 of the merged set
4. The 'S2' in front of a TLA channel denotes Slave card #2 of the merged set
5. The 'S3' in front of a TLA channel denotes Slave card #3 of the merged set
6. Signals in these groups are acquired using the 7Bx4's demux capability and will not have a MagniVu display value

Group Name	Signal Name	DDR3 Pin #	TLA Input	Group Name	Signal Name	DDR3 Pin #	TLA Input
Wr_CDatHi	WR_C_DQ63	234	S2_E2:0^1	Wr_CDatLo	WR_C_DQ31	156	S_A2:6^1
(Hex)	WR_C_DQ62	233	S2_E2:1^1	(Hex)	WR_C_DQ30	155	S_A2:3^1
	WR_C_DQ61	228	S2_E2:5^1		WR_C_DQ29	150	S3_E2:0^1
	WR_C_DQ60	227	S2_Q3^1		WR_C_DQ28	149	S3_E2:1^1
	WR_C_DQ59	115	S2_E2:2^1		WR_C_DQ27	37	S_A2:4^1
	WR_C_DQ58	114	S2_E2:3^1		WR_C_DQ26	36	S_A2:1^1
	WR_C_DQ57	109	S2_E2:7^1		WR_C_DQ25	31	S3_E2:2^1
	WR_C_DQ56	108	S2_E3:0^1		WR_C_DQ24	30	S3_E2:3^1
	WR_C_DQ55	225	S2_E3:2^1		WR_C_DQ23	147	S3_E2:4^1
	WR_C_DQ54	224	S2_E3:3^1		WR_C_DQ22	146	S3_E2:5^1
	WR_C_DQ53	219	S2_E3:7^1		WR_C_DQ21	141	S3_E3:2^1
	WR_C_DQ52	218	S2_C3:5^1		WR_C_DQ20	140	S3_E3:3^1
	WR_C_DQ51	106	S2_E3:1^1		WR_C_DQ19	28	S3_E2:6^1
	WR_C_DQ50	105	S2_E3:4^1		WR_C_DQ18	27	S3_E2:7^1
	WR_C_DQ49	100	S2_C3:7^1		WR_C_DQ17	22	S3_E3:1^1
	WR_C_DQ48	99	S2_C3:6^1		WR_C_DQ16	21	S3_E3:4^1
	WR_C_DQ47	216	S2_C3:4^1		WR_C_DQ15	138	S3_E3:6^1
	WR_C_DQ46	215	S2_C3:1^1		WR_C_DQ14	137	S3_E3:7^1
	WR_C_DQ45	210	S2_C2:7^1		WR_C_DQ13	132	S3_C3:4^1
	WR_C_DQ44	209	S2_C2:6^1		WR_C_DQ12	131	S3_C3:1^1
	WR_C_DQ43	97	S2_C3:3^1		WR_C_DQ11	19	S3_E3:5^1
	WR_C_DQ42	96	S2_C3:2^1		WR_C_DQ10	18	S3_C3:7^1
	WR_C_DQ41	91	S2_C2:5^1		WR_C_DQ9	13	S3_C3:3^1
	WR_C_DQ40	90	S2_C2:4^1		WR_C_DQ8	12	S3_C3:2^1
	WR_C_DQ39	207	S2_C2:3^1		WR_C_DQ7	129	S3_C3:0^1
	WR_C_DQ38	206	S2_C2:2^1		WR_C_DQ6	128	S3_C2:7^1
	WR_C_DQ37	201	M_E2:1^1		WR_C_DQ5	123	S3_C2:3^1
	WR_C_DQ36	200	M_E2:4^1		WR_C_DQ4	122	S3_C2:2^1
	WR_C_DQ35	88	S2_C2:1^1		WR_C_DQ3	10	S3_CK3^1
	WR_C_DQ34	87	S2_C2:0^1		WR_C_DQ2	9	S3_C2:5^1
	WR_C_DQ33	83	M_E2:6^1		WR_C_DQ1	4	S3_C2:1^1
	WR_C_DQ32	81	M_E2:7^1		WR_C_DQ0	3	S3_C2:0^1

Table 3 – B_DDR3D_4D (<=1866MT/s Read and Write) Storage and Trigger Grouping (cont'd.)

Notes:

1. All signals on this page are required for accurate post-processing of acquired data
2. The 'M' in front of a TLA channel denotes the Master card of the merged set
3. The 'S' in front of a TLA channel denotes Slave card #1 of the merged set
4. The 'S2' in front of a TLA channel denotes Slave card #2 of the merged set
5. The 'S3' in front of a TLA channel denotes Slave card #3 of the merged set
6. All signals on this page are stored in the 7Bx4's Prime memory and will not have a MagniVu display value

Group Name	Signal Name	DDR3 Pin #	TLA Input	Group Name	Signal Name	DDR3 Pin #	TLA Input
Wr_DDatHi	WR_D_DQ63	234	S2_E0:0^1	Wr_DDatLo	WR_D_DQ31	156	S_D2:6^1
(Hex)	WR_D_DQ62	233	S2_E0:1^1	(Hex)	WR_D_DQ30	155	S_D2:3^1
	WR_D_DQ61	228	S2_E0:5^1		WR_D_DQ29	150	S3_E0:0^1
	WR_D_DQ60	227	S2_CK2^1		WR_D_DQ28	149	S3_E0:1^1
	WR_D_DQ59	115	S2_E0:2^1		WR_D_DQ27	37	S_D2:4^1
	WR_D_DQ58	114	S2_E0:3^1		WR_D_DQ26	36	S_D2:1^1
	WR_D_DQ57	109	S2_E0:7^1		WR_D_DQ25	31	S3_E0:2^1
	WR_D_DQ56	108	S2_E1:0^1		WR_D_DQ24	30	S3_E0:3^1
	WR_D_DQ55	225	S2_E1:2^1		WR_D_DQ23	147	S3_E0:4^1
	WR_D_DQ54	224	S2_E1:3^1		WR_D_DQ22	146	S3_E0:5^1
	WR_D_DQ53	219	S2_E1:7^1		WR_D_DQ21	141	S3_E1:2^1
	WR_D_DQ52	218	S2_C1:5^1		WR_D_DQ20	140	S3_E1:3^1
	WR_D_DQ51	106	S2_E1:1^1		WR_D_DQ19	28	S3_E0:6^1
	WR_D_DQ50	105	S2_E1:4^1		WR_D_DQ18	27	S3_E0:7^1
	WR_D_DQ49	100	S2_C1:7^1		WR_D_DQ17	22	S3_E1:1^1
	WR_D_DQ48	99	S2_C1:6^1		WR_D_DQ16	21	S3_E1:4^1
	WR_D_DQ47	216	S2_C1:4^1		WR_D_DQ15	138	S3_E1:6^1
	WR_D_DQ46	215	S2_C1:1^1		WR_D_DQ14	137	S3_E1:7^1
	WR_D_DQ45	210	S2_C0:7^1		WR_D_DQ13	132	S3_C1:4^1
	WR_D_DQ44	209	S2_C0:6^1		WR_D_DQ12	131	S3_C1:1^1
	WR_D_DQ43	97	S2_C1:3^1		WR_D_DQ11	19	S3_E1:5^1
	WR_D_DQ42	96	S2_C1:2^1		WR_D_DQ10	18	S3_C1:7^1
	WR_D_DQ41	91	S2_C0:5^1		WR_D_DQ9	13	S3_C1:3^1
	WR_D_DQ40	90	S2_C0:4^1		WR_D_DQ8	12	S3_C1:2^1
	WR_D_DQ39	207	S2_C0:3^1		WR_D_DQ7	129	S3_C1:0^1
	WR_D_DQ38	206	S2_C0:2^1		WR_D_DQ6	128	S3_C0:7^1
	WR_D_DQ37	201	M_E0:1^1		WR_D_DQ5	123	S3_C0:3^1
	WR_D_DQ36	200	M_E0:4^1		WR_D_DQ4	122	S3_C0:2^1
	WR_D_DQ35	88	S2_C0:1^1		WR_D_DQ3	10	S3_Q2^1
	WR_D_DQ34	87	S2_C0:0^1		WR_D_DQ2	9	S3_C0:5^1
	WR_D_DQ32	83	M_E0:6^1		WR_D_DQ1	4	S3_C0:1^1
	WR_D_DQ33	81	M_E0:7^1		WR_D_DQ0	3	S3_C0:0^1

Table 3 – B_DDR3D_4D (<=1866MT/s Read and Write) Storage and Trigger Grouping (cont'd.)

Notes:

1. All signals on this page are required for accurate post-processing of acquired data
2. The 'M' in front of a TLA channel denotes the Master card of the merged set
3. The 'S' in front of a TLA channel denotes Slave card #1 of the merged set
4. The 'S2' in front of a TLA channel denotes Slave card #2 of the merged set
5. The 'S3' in front of a TLA channel denotes Slave card #3 of the merged set
6. All signals on this page are stored in the 7Bx4's Prime memory and will not have a MagniVu display value

Group Name	Signal Name	DDR3 Pin #	TLA Input	Group Name	Signal Name	DDR3 Pin #	TLA Input
Rd_AChkBits	RDa_CB7	165	S_A3:5	Wr_AChkBits	WRa_CB7	165	S_C3:5
(OFF)	RDa_CB6	164	S_A3:4	(OFF)	WRa_CB6	164	S_C3:4
	RDa_CB5	159	S_A3:0		WRa_CB5	159	S_C3:0
	RDa_CB4	158	S_A2:7		WRa_CB4	158	S_C2:7
	RDa_CB3	46	S_A3:6		WRa_CB3	46	S_C3:6
	RDa_CB2	45	S_A3:3		WRa_CB2	45	S_C3:3
	RDa_CB1	40	S_CK0		WRa_CB1	40	S_CK3
	RDa_CB0	39	S_A2:5		WRa_CB0	39	S_C2:5
Rd_BChkBits[3]	RDb_CB7	165	S_D3:5	Wr_BChkBits[3]	WRb_CB7	165	S_C1:5
(OFF)	RDb_CB6	164	S_D3:4	(OFF)	WRb_CB6	164	S_C1:4
	RDb_CB5	159	S_D3:0		WRb_CB5	159	S_C1:0
	RDb_CB4	158	S_D2:7		WRb_CB4	158	S_C0:7
	RDb_CB3	46	S_D3:6		WRb_CB3	46	S_C1:6
	RDb_CB2	45	S_D3:3		WRb_CB2	45	S_C1:3
	RDb_CB1	40	S_Q1		WRb_CB1	40	S_Q2
	RDb_CB0	39	S_D2:5		WRb_CB0	39	S_C0:5
Rd_CChkBits[4]	RDc_CB7	165	S_A3:5^1	Wr_CChkBits[4]	WRc_CB7	165	S_C3:5^1
(OFF)	RDc_CB6	164	S_A3:4^1	(OFF)	WRc_CB6	164	S_C3:4^1
	RDc_CB5	159	S_A3:0^1		WRc_CB5	159	S_C3:0^1
	RDc_CB4	158	S_A2:7^1		WRc_CB4	158	S_C2:7^1
	RDc_CB3	46	S_A3:6^1		WRc_CB3	46	S_C3:6^1
	RDc_CB2	45	S_A3:3^1		WRc_CB2	45	S_C3:3^1
	RDc_CB1	40	S_CK0^1		WRc_CB1	40	S_CK3^1
	RDc_CB0	39	S_A2:5^1		WRc_CB0	39	S_C2:5^1
Rd_DChkBits[4]	RDd_CB7	165	S_D3:5^1	Wr_DChkBits[4]	WRd_CB7	165	S_C1:5^1
(OFF)	RDd_CB6	164	S_D3:4^1	(OFF)	WRd_CB6	164	S_C1:4^1
	RDd_CB5	159	S_D3:0^1		WRd_CB5	159	S_C1:0^1
	RDd_CB4	158	S_D2:7^1		WRd_CB4	158	S_C0:7^1
	RDd_CB3	46	S_D3:6^1		WRd_CB3	46	S_C1:6^1
	RDd_CB2	45	S_D3:3^1		WRd_CB2	45	S_C1:3^1
	RDd_CB1	40	S_Q1^1		WRd_CB1	40	S_Q2^1
	RDd_CB0	39	S_D2:5^1		WRd_CB0	39	S_C0:5^1

Table 3 – B_DDR3D_4D (<=1866MT/s Read and Write) Storage and Trigger Grouping (cont'd.)

Notes:

1. ' # ' denotes a low-true signal
2. The 'S' in front of a TLA channel denotes Slave card #1 of the merged set
3. Signals in these groups are acquired using the TLA's demux capability and will not have a MagniVu display value
4. Signals in these groups are stored in the 7Bx4's Prime memory and will not have a MagniVu display value

Group Name	Signal Name	DDR3 Pin #	TLA Input	Group Name	Signal Name	DDR3 Pin #	TLA Input
ADatMsks (BIN)	a_DM8	161	S_C3:1	BDatMsks [5] (BIN)	b_DM8	161	S_C1:1
	a_DM7	230	S2_E2:4		b_DM7	230	S2_E0:4
	a_DM6	221	S2_E3:6		b_DM6	221	S2_E1:6
	a_DM5	212	S2_C3:0		b_DM5	212	S2_C1:0
	a_DM4	203	M_E2:0		b_DM4	203	M_E0:0
	a_DM3	152	S_C2:2		b_DM3	152	S_C0:2
	a_DM2	143	S3_Q3		b_DM2	143	S3_CK2
	a_DM1	134	S3_C3:5		b_DM1	134	S3_C1:5
	a_DM0	125	S3_C2:6		b_DM0	125	S3_C0:6
CDatMsks [6] (BIN)	c_DM8	161	S_C3:1^1	DDatMsks [6] (BIN)	d_DM8	161	S_C1:1^1
	c_DM7	230	S2_E2:4^1		d_DM7	230	S2_E0:4^1
	c_DM6	221	S2_E3:6^1		d_DM6	221	S2_E1:6^1
	c_DM5	212	S2_C3:0^1		d_DM5	212	S2_C1:0^1
	c_DM4	203	M_E2:0^1		d_DM4	203	M_E0:0^1
	c_DM3	152	S_C2:2^1		d_DM3	152	S_C0:2^1
	c_DM2	143	S3_Q3^1		d_DM2	143	S3_CK2^1
	c_DM1	134	S3_C3:5^1		d_DM1	134	S3_C1:5^1
	c_DM0	125	S3_C2:6^1		d_DM0	125	S3_C0:6^1

Table 3 – B_DDR3D_4D (<=1866MT/s Read and Write) Storage and Trigger Grouping (cont'd.)

Notes:

1. The 'M' in front of a TLA channel denotes the Master card of the merged set
2. The 'S' in front of a TLA channel denotes Slave card #1 of the merged set
3. The 'S2' in front of a TLA channel denotes Slave card #2 of the merged set
4. The 'S3' in front of a TLA channel denotes Slave card #3 of the merged set
5. Signals in these groups are acquired using the TLA's demux capability and will not have a MagniVu display value
6. Signals in these groups are stored in the 7Bx4's Prime memory and will not have a MagniVu display value

Group Name	Signal Name	DDR3 Pin #	TLA Input	Group Name	Signal Name	DDR3 Pin #	TLA Input
Control_0 [2]	CKE1_0	169	S_A1:2	Control_1 [2,5]	CKE1_1	169	S_A1:2^1
(SYM)	CKE0_0	50	S_A1:1	(SYM)	CKE0_1	50	S_A1:1^1
	S3#_0	49	M_C2:5		S3#_1	49	M_ C2:5^1
	S2#_0	48	M_C3:0		S2#_1	48	M_ C3:0^1
	S1#_0	76	M_ C3:4		S1#_1	76	M_ C3:4^1
	S0#_0	193	M_ C3:3		S0#_1	193	M_ C3:3^1
	BA2_0	52	S_A1:0		BA2_1	52	S_A1:0^1
	BA1_0	190	M_ C3:7		BA1_1	190	M_ C3:7^1
	BA0_0	71	M_C1:6		BA0_1	71	M_C1:6^1
	A15_0	171	S_CK1		A15_1	171	S_CK1^1
	A14_0	172	S_A0:5		A14_1	172	S_A0:5^1
	A13_0	196	M_CK3		A13_1	196	M_CK3^1
	A12/BC#_0	174	S_A0:4		A12/BC#_1	174	S_A0:4^1
	A10/AP_0	70	M_C1:3		A10/AP_1	70	M_C1:3^1
	RAS#_0	192	M_ C3:6		RAS#_1	192	M_ C3:6^1
	CAS#_0	74	M_ C3:5		CAS#_1	74	M_ C3:5^1
	WE#_0	73	M_C1:7		WE#_1	73	M_C1:7^1
Address_0 [2]	BA2_0	52	M_ C3:3	Address_1 [2,5]	BA2_1	52	S_A1:0^1
(Hex)	BA1_0	190	S_A1:0	(Hex)	BA1_1	190	M_ C3:7^1
	BA0_0	71	M_ C3:7		BA0_1	71	M_C1:6^1
	A15_0	171	M_C1:6		A15_1	171	S_CK1^1
	A14_0	172	S_CK1		A14_1	172	S_A0:5^1
	A13_0	196	S_A0:5		A13_1	196	M_CK3^1
	A12/BC#_0	174	M_CK3		A12/BC#_1	174	S_A0:4^1
	A11_0	55	S_A0:4		A11_1	55	S_A0:6^1
	A10/AP_0	70	M_C1:3		A10/AP_1	70	M_C1:3^1
	A9_0	175	S_A0:1		A9_1	175	S_A0:1^1
	A8_0	177	S_A0:0		A8_1	177	S_A0:0^1
	A7_0	56	S_A0:3		A7_1	56	S_A0:3^1
	A6_0	178	M_C0:2		A6_1	178	M_C0:2^1
	A5_0	58	S_A0:2		A5_1	58	S_A0:2^1
	A4_0	59	M_C0:5		A4_1	59	M_C0:5^1
	A3_0	180	M_C1:0		A3_1	180	M_C1:0^1
	A2_0	61	M_Q1		A2_1	61	M_Q1^1
	A1_0	181	M_C1:1		A1_1	181	M_C1:1^1
	A0_0	188	M_C1:5		A0_1	188	M_C1:5^1

Table 3 – B_DDR3D_4D (<=1866MT/s Read and Write) Storage and Trigger Grouping (cont'd.)

Notes:

1. ' # ' denotes a low-true signal
2. These signals are required for accurate acquisition and post-processing of acquired data
3. The 'M' in front of a TLA channel denotes the Master card of the merged set
4. The 'S' in front of a TLA channel denotes Slave card #1 of the merged set
5. Signals in these groups are stored in the 7Bx4's Prime memory and will not have a MagniVu display value

Group Name	Signal Name	DDR3 Pin #	TLA Input	Group Name	Signal Name	DDR3 Pin #	TLA Input
Ungrouped	PAR_IN_0	68	M_C1:2	Ungrouped	RESET#_0	168	S_A1:6
	PAR_IN_1	68	M_C1:2^1		RESET#_1	168	S_A1:6^1
	ERR_OUT#[3]_0	53	S_A0:7		ODT1_0	77	M_C3:1
	ERR_OUT#[3]_1	53	S_A0:7^1		ODT1_1	77	M_C3:1^1
	TEST_0	167	S_A1:7		ODT0_0	195	M_C3:2
	TEST_1	167	S_A1:7^1		ODT0_1	195	M_C3:2^1

Table 3 – B_DDR3D_4D (<=1866MT/s Read and Write) Storage and Trigger Grouping (cont'd.)

Notes:

1. ' # ' denotes a low-true signal
2. The 'M' in front of a TLA channel denotes the Master card of the merged set
3. The 'S' in front of a TLA channel denotes Slave card #1 of the merged set
4. Signals with a '^1' suffix are stored in the 7Bx4's Prime memory and will not have a MagniVu display value

Group Name	Signal Name	DDR3 Pin #	TLA Input	Group Name	Signal Name	DDR3 Pin #	TLA Input
ADataHi (Hex)	A_DQ63	234	A0:0	ADataLo (Hex)	A_DQ31	156	D2:6
	A_DQ62	233	A0:1		A_DQ30	155	D2:3
	A_DQ61	228	A0:5		A_DQ29	150	E2:0
	A_DQ60	227	CK1		A_DQ28	149	E2:1
	A_DQ59	115	A0:2		A_DQ27	37	D2:4
	A_DQ58	114	A0:3		A_DQ26	36	D2:1
	A_DQ57	109	A0:7		A_DQ25	31	E2:2
	A_DQ56	108	A1:0		A_DQ24	30	E2:3
	A_DQ55	225	A1:2		A_DQ23	147	E2:4
	A_DQ54	224	A1:3		A_DQ22	146	E2:5
	A_DQ53	219	A1:7		A_DQ21	141	E3:2
	A_DQ52	218	D1:5		A_DQ20	140	E3:3
	A_DQ51	106	A1:1		A_DQ19	28	E2:6
	A_DQ50	105	A1:4		A_DQ18	27	E2:7
	A_DQ49	100	D1:7		A_DQ17	22	E3:1
	A_DQ48	99	D1:6		A_DQ16	21	E3:4
	A_DQ47	216	D1:4		A_DQ15	138	E3:6
	A_DQ46	215	D1:1		A_DQ14	137	E3:7
	A_DQ45	210	D0:7		A_DQ13	132	E1:4
	A_DQ44	209	D0:6		A_DQ12	131	E1:1
	A_DQ43	97	D1:3		A_DQ11	19	E3:5
	A_DQ42	96	D1:2		A_DQ10	18	E1:7
	A_DQ41	91	D0:5		A_DQ9	13	E1:3
	A_DQ40	90	D0:4		A_DQ8	12	E1:2
	A_DQ39	207	D0:3		A_DQ7	129	E1:0
	A_DQ38	206	D0:2		A_DQ6	128	E0:7
	A_DQ37	201	C2:1		A_DQ5	123	E0:3
	A_DQ36	200	C2:4		A_DQ4	122	E0:2
	A_DQ35	88	D0:1		A_DQ3	10	Q2
	A_DQ34	87	D0:0		A_DQ2	9	E0:5
	A_DQ33	83	C2:6		A_DQ1	4	E0:1
	A_DQ32	81	C2:7		A_DQ0	3	E0:0

Table 4 - R_DDR3D_1A (<=1333MT/s Read and Write) Storage and Trigger Grouping

Notes:

1. All signals on this page are required for accurate post-processing of acquired data

Group Name	Signal Name	DDR3 Pin#	TLA Input	Group Name	Signal Name	DDR3 Pin#	TLA Input
BDataHi	B_DQ63	234	A0:0^1	BDataLo	B_DQ31	156	D2:6^1
(Hex)	B_DQ62	233	A0:1^1	(Hex)	B_DQ30	155	D2:3^1
	B_DQ61	228	A0:5^1		B_DQ29	150	E2:0^1
	B_DQ60	227	CK1^1		B_DQ28	149	E2:1^1
	B_DQ59	115	A0:2^1		B_DQ27	37	D2:4^1
	B_DQ58	114	A0:3^1		B_DQ26	36	D2:1^1
	B_DQ57	109	A0:7^1		B_DQ25	31	E2:2^1
	B_DQ56	108	A1:0^1		B_DQ24	30	E2:3^1
	B_DQ55	225	A1:2^1		B_DQ23	147	E2:4^1
	B_DQ54	224	A1:3^1		B_DQ22	146	E2:5^1
	B_DQ53	219	A1:7^1		B_DQ21	141	E3:2^1
	B_DQ52	218	D1:5^1		B_DQ20	140	E3:3^1
	B_DQ51	106	A1:1^1		B_DQ19	28	E2:6^1
	B_DQ50	105	A1:4^1		B_DQ18	27	E2:7^1
	B_DQ49	100	D1:7^1		B_DQ17	22	E3:1^1
	B_DQ48	99	D1:6^1		B_DQ16	21	E3:4^1
	B_DQ47	216	D1:4^1		B_DQ15	138	E3:6^1
	B_DQ46	215	D1:1^1		B_DQ14	137	E3:7^1
	B_DQ45	210	D0:7^1		B_DQ13	132	E1:4^1
	B_DQ44	209	D0:6^1		B_DQ12	131	E1:1^1
	B_DQ43	97	D1:3^1		B_DQ11	19	E3:5^1
	B_DQ42	96	D1:2^1		B_DQ10	18	E1:7^1
	B_DQ41	91	D0:5^1		B_DQ9	13	E1:3^1
	B_DQ40	90	D0:4^1		B_DQ8	12	E1:2^1
	B_DQ39	207	D0:3^1		B_DQ7	129	E1:0^1
	B_DQ38	206	D0:2^1		B_DQ6	128	E0:7^1
	B_DQ37	201	C2:1^1		B_DQ5	123	E0:3^1
	B_DQ36	200	C2:4^1		B_DQ4	122	E0:2^1
	B_DQ35	88	D0:1^1		B_DQ3	10	Q2^1
	B_DQ34	87	D0:0^1		B_DQ2	9	E0:5^1
	B_DQ33	83	C2:6^1		B_DQ1	4	E0:1^1
	B_DQ32	81	C2:7^1		B_DQ0	3	E0:0^1

Table 4 – R_DDR3D_1A (<=1333MT/s Read and Write) Storage and Trigger Grouping (cont'd.)

Notes:

1. All signals on this page are required for accurate post-processing of acquired data
2. All signals on this page are stored in the 7Bx4's Prime memory and will not have a MagniVu display value

Group Name	Signal Name	DDR3 Pin #	TLA Input	Group Name	Signal Name	DDR3 Pin #	TLA Input
AChkBits	A_CB7	165	D3:5	ADataMsks	A_DM7	230	A0:4
(OFF)	A_CB6	164	D3:4	(BIN)	A_DM6	221	A1:6
	A_CB5	159	D3:0		A_DM5	212	D1:0
	A_CB4	158	D2:7		A_DM4	203	C2:0
	A_CB3	46	D3:6		A_DM3	152	D2:2
	A_CB2	45	D3:3		A_DM2	143	Q3
	A_CB1	40	Q0		A_DM1	134	E1:5
	A_CB0	39	D2:5		A_DM0	125	E0:6
BChkBits [4]	B_CB7	165	D3:5^1	BDataMsks [4]	B_DM7	230	A0:4^1
(OFF)	B_CB6	164	D3:4^1	(BIN)	B_DM6	221	A1:6^1
	B_CB5	159	D3:0^1		B_DM5	212	D1:0^1
	B_CB4	158	D2:7^1		B_DM4	203	C2:0^1
	B_CB3	46	D3:6^1		B_DM3	152	D2:2^1
	B_CB2	45	D3:3^1		B_DM2	143	Q3^1
	B_CB1	40	Q0^1		B_DM1	134	E1:5^1
	B_CB0	39	D2:5^1		B_DM0	125	E0:6^1

Table 4 – R_DDR3D_1A (<=1333MT/s Read and Write) Storage and Trigger Grouping (cont'd.)

Notes:

1. ' # ' denotes a low-true signal
2. Signals in these groups are acquired using the 7Bx4's demux capability and will not have a MagniVu display value

Group Name	Signal Name	DDR3 Pin #	TLA Input	Group Name	Signal Name	DDR3 Pin #	TLA Input
Control[2]	CKE1	169	A3:2	Address[2]	BA2	52	A3:0
(SYM)	CKE0	50	A3:1	(Hex)	BA1	190	C3:7
	S3#	49	C2:5		BA0	71	C1:6
	S2#	48	C3:0		A15	171	CK0
	S1#	76	C3:4		A14	172	A2:5
	S0#	193	C3:3		A13	196	CK3
	BA2	52	A3:0		A12/BC#	174	A2:4
	BA1	190	C3:7		A11	55	A2:6
	BA0	71	C1:6		A10/AP	70	C1:3
	A15	171	CK0		A9	175	A2:1
	A14	172	A2:5		A8	177	A2:0
	A13	196	CK3		A7	56	A2:3
	A12/BC#	174	A2:4		A6	178	C0:2
	A10/AP	70	C1:3		A5	58	A2:2
	RAS#	192	C3:6		A4	59	C0:5
	CAS#	74	C3:5		A3	180	C1:0
	WE#	73	C1:7		A2	61	Q1
Ungrouped	DM8	161	D3:1		A1	181	C1:1
	ERR_OUT#[3]	53	A2:7		A0	188	C1:5
	RESET#	168	A3:6				
	TEST	167	A3:7				
	ODT0	195	C3:2				
	ODT1	77	C3:1				
	PAR_IN	68	C1:2				

Table 4 – R_DDR3D_1A (<=1333MT/s Read and Write) Storage and Trigger Grouping (cont'd.)

Notes:

1. ' # ' denotes a low-true signal
2. These signals are required for accurate acquisition and post-processing of acquired data
3. Signals in these groups are acquired using the 7Bx4's demux capability and will not have a MagniVu display value

Group Name	Signal Name	DDR3 Pin #	TLA Input	Group Name	Signal Name	DDR3 Pin #	TLA Input
ADatHi	A_DQ63	234	M_A0:0	ADatLo	A_DQ31	156	M_D2:6
(Hex)	A_DQ62	233	M_A0:1	(Hex)	A_DQ30	155	M_D2:3
	A_DQ61	228	M_A0:5		A_DQ29	150	M_E2:0
	A_DQ60	227	M_CK1		A_DQ28	149	M_E2:1
	A_DQ59	115	M_A0:2		A_DQ27	37	M_D2:4
	A_DQ58	114	M_A0:3		A_DQ26	36	M_D2:1
	A_DQ57	109	M_A0:7		A_DQ25	31	M_E2:2
	A_DQ56	108	M_A1:0		A_DQ24	30	M_E2:3
	A_DQ55	225	M_A1:2		A_DQ23	147	M_E2:4
	A_DQ54	224	M_A1:3		A_DQ22	146	M_E2:5
	A_DQ53	219	M_A1:7		A_DQ21	141	M_E3:2
	A_DQ52	218	M_D1:5		A_DQ20	140	M_E3:3
	A_DQ51	106	M_A1:1		A_DQ19	28	M_E2:6
	A_DQ50	105	M_A1:4		A_DQ18	27	M_E2:7
	A_DQ49	100	M_D1:7		A_DQ17	22	M_E3:1
	A_DQ48	99	M_D1:6		A_DQ16	21	M_E3:4
	A_DQ47	216	M_D1:4		A_DQ15	138	M_E3:6
	A_DQ46	215	M_D1:1		A_DQ14	137	M_E3:7
	A_DQ45	210	M_D0:7		A_DQ13	132	M_E1:4
	A_DQ44	209	M_D0:6		A_DQ12	131	M_E1:1
	A_DQ43	97	M_D1:3		A_DQ11	19	M_E3:5
	A_DQ42	96	M_D1:2		A_DQ10	18	M_E1:7
	A_DQ41	91	M_D0:5		A_DQ9	13	M_E1:3
	A_DQ40	90	M_D0:4		A_DQ8	12	M_E1:2
	A_DQ39	207	M_D0:3		A_DQ7	129	M_E1:0
	A_DQ38	206	M_D0:2		A_DQ6	128	M_E0:7
	A_DQ37	201	M_C2:1		A_DQ5	123	M_E0:3
	A_DQ36	200	M_C2:4		A_DQ4	122	M_E0:2
	A_DQ35	88	M_D0:1		A_DQ3	10	M_Q2
	A_DQ34	87	M_D0:0		A_DQ2	9	M_E0:5
	A_DQ33	83	M_C2:6		A_DQ1	4	M_E0:1
	A_DQ32	81	M_C2:7		A_DQ0	3	M_E0:0

Table 5 - R_DDR3D_2A (<=1866MT/s Read and Write) Storage and Trigger Grouping

Notes:

1. All signals on this page are required for accurate post-processing of acquired data
2. The ‘M’ in front of a TLA channel denotes the Master card of the merged pair

Group Name	Signal Name	DDR3 Pin#	TLA Input	Group Name	Signal Name	DDR3 Pin#	TLA Input
BDatHi	B_DQ63	234	S_A0:0	BDatLo	B_DQ31	156	S_D2:6
(Hex)	B_DQ62	233	S_A0:1	(Hex)	B_DQ30	155	S_D2:3
	B_DQ61	228	S_A0:5		B_DQ29	150	S_E2:0
	B_DQ60	227	S_CK1		B_DQ28	149	S_E2:1
	B_DQ59	115	S_A0:2		B_DQ27	37	S_D2:4
	B_DQ58	114	S_A0:3		B_DQ26	36	S_D2:1
	B_DQ57	109	S_A0:7		B_DQ25	31	S_E2:2
	B_DQ56	108	S_A1:0		B_DQ24	30	S_E2:3
	B_DQ55	225	S_A1:2		B_DQ23	147	S_E2:4
	B_DQ54	224	S_A1:3		B_DQ22	146	S_E2:5
	B_DQ53	219	S_A1:7		B_DQ21	141	S_E3:2
	B_DQ52	218	S_D1:5		B_DQ20	140	S_E3:3
	B_DQ51	106	S_A1:1		B_DQ19	28	S_E2:6
	B_DQ50	105	S_A1:4		B_DQ18	27	S_E2:7
	B_DQ49	100	S_D1:7		B_DQ17	22	S_E3:1
	B_DQ48	99	S_D1:6		B_DQ16	21	S_E3:4
	B_DQ47	216	S_D1:4		B_DQ15	138	S_E3:6
	B_DQ46	215	S_D1:1		B_DQ14	137	S_E3:7
	B_DQ45	210	S_D0:7		B_DQ13	132	S_E1:4
	B_DQ44	209	S_D0:6		B_DQ12	131	S_E1:1
	B_DQ43	97	S_D1:3		B_DQ11	19	S_E3:5
	B_DQ42	96	S_D1:2		B_DQ10	18	S_E1:7
	B_DQ41	91	S_D0:5		B_DQ9	13	S_E1:3
	B_DQ40	90	S_D0:4		B_DQ8	12	S_E1:2
	B_DQ39	207	S_D0:3		B_DQ7	129	S_E1:0
	B_DQ38	206	S_D0:2		B_DQ6	128	S_E0:7
	B_DQ37	201	S_C2:1		B_DQ5	123	S_E0:3
	B_DQ36	200	S_C2:4		B_DQ4	122	S_E0:2
	B_DQ35	88	S_D0:1		B_DQ3	10	S_Q2
	B_DQ34	87	S_D0:0		B_DQ2	9	S_E0:5
	B_DQ33	83	S_C2:6		B_DQ1	4	S_E0:1
	B_DQ32	81	S_C2:7		B_DQ0	3	S_E0:0

Table 5 – R_DDR3D_2A (<=1866MT/s Read and Write) Storage and Trigger Grouping (cont'd.)

Notes:

1. All signals on this page are required for accurate post-processing of acquired data
2. The 'S' in front of a TLA channel denotes the Slave card of the merged pair
3. Signals in these groups are acquired using the 7Bx4's demux capability and will not have a MagniVu display value

Group Name	Signal Name	DDR3 Pin #	TLA Input	Group Name	Signal Name	DDR3 Pin #	TLA Input
CDatHi (Hex)	C_DQ63	234	M_A0:0^1	CDatLo (Hex)	C_DQ31	156	M_D2:6^1
	C_DQ62	233	M_A0:1^1		C_DQ30	155	M_D2:3^1
	C_DQ61	228	M_A0:5^1		C_DQ29	150	M_E2:0^1
	C_DQ60	227	M_CK1^1		C_DQ28	149	M_E2:1^1
	C_DQ59	115	M_A0:2^1		C_DQ27	37	M_D2:4^1
	C_DQ58	114	M_A0:3^1		C_DQ26	36	M_D2:1^1
	C_DQ57	109	M_A0:7^1		C_DQ25	31	M_E2:2^1
	C_DQ56	108	M_A1:0^1		C_DQ24	30	M_E2:3^1
	C_DQ55	225	M_A1:2^1		C_DQ23	147	M_E2:4^1
	C_DQ54	224	M_A1:3^1		C_DQ22	146	M_E2:5^1
	C_DQ53	219	M_A1:7^1		C_DQ21	141	M_E3:2^1
	C_DQ52	218	M_D1:5^1		C_DQ20	140	M_E3:3^1
	C_DQ51	106	M_A1:1^1		C_DQ19	28	M_E2:6^1
	C_DQ50	105	M_A1:4^1		C_DQ18	27	M_E2:7^1
	C_DQ49	100	M_D1:7^1		C_DQ17	22	M_E3:1^1
	C_DQ48	99	M_D1:6^1		C_DQ16	21	M_E3:4^1
	C_DQ47	216	M_D1:4^1		C_DQ15	138	M_E3:6^1
	C_DQ46	215	M_D1:1^1		C_DQ14	137	M_E3:7^1
	C_DQ45	210	M_D0:7^1		C_DQ13	132	M_E1:4^1
	C_DQ44	209	M_D0:6^1		C_DQ12	131	M_E1:1^1
	C_DQ43	97	M_D1:3^1		C_DQ11	19	M_E3:5^1
	C_DQ42	96	M_D1:2^1		C_DQ10	18	M_E1:7^1
	C_DQ41	91	M_D0:5^1		C_DQ9	13	M_E1:3^1
	C_DQ40	90	M_D0:4^1		C_DQ8	12	M_E1:2^1
	C_DQ39	207	M_D0:3^1		C_DQ7	129	M_E1:0^1
	C_DQ38	206	M_D0:2^1		C_DQ6	128	M_E0:7^1
	C_DQ37	201	M_C2:1^1		C_DQ5	123	M_E0:3^1
	C_DQ36	200	M_C2:4^1		C_DQ4	122	M_E0:2^1
	C_DQ35	88	M_D0:1^1		C_DQ3	10	M_Q2^1
	C_DQ34	87	M_D0:0^1		C_DQ2	9	M_E0:5^1
	C_DQ33	83	M_C2:6^1		C_DQ1	4	M_E0:1^1
	C_DQ32	81	M_C2:7^1		C_DQ0	3	M_E0:0^1

Table 5 – R_DDR3D_2A (<=1866MT/s Read and Write) Storage and Trigger Grouping (cont'd.)

Notes:

1. All signals on this page are required for accurate post-processing of acquired data
2. The 'M' in front of a TLA channel denotes the Master card of the merged pair
3. All signals on this page are stored in the 7Bx4's Prime memory and will not have a MagniVu display value

Group Name	Signal Name	DDR3 Pin#	TLA Input	Group Name	Signal Name	DDR3 Pin#	TLA Input
DDatHi (Hex)	D_DQ63	234	S_A0:0^1	DDatLo (Hex)	D_DQ31	156	S_D2:6^1
	D_DQ62	233	S_A0:1^1		D_DQ30	155	S_D2:3^1
	D_DQ61	228	S_A0:5^1		D_DQ29	150	S_E2:0^1
	D_DQ60	227	S_CK1^1		D_DQ28	149	S_E2:1^1
	D_DQ59	115	S_A0:2^1		D_DQ27	37	S_D2:4^1
	D_DQ58	114	S_A0:3^1		D_DQ26	36	S_D2:1^1
	D_DQ57	109	S_A0:7^1		D_DQ25	31	S_E2:2^1
	D_DQ56	108	S_A1:0^1		D_DQ24	30	S_E2:3^1
	D_DQ55	225	S_A1:2^1		D_DQ23	147	S_E2:4^1
	D_DQ54	224	S_A1:3^1		D_DQ22	146	S_E2:5^1
	D_DQ53	219	S_A1:7^1		D_DQ21	141	S_E3:2^1
	D_DQ52	218	S_D1:5^1		D_DQ20	140	S_E3:3^1
	D_DQ51	106	S_A1:1^1		D_DQ19	28	S_E2:6^1
	D_DQ50	105	S_A1:4^1		D_DQ18	27	S_E2:7^1
	D_DQ49	100	S_D1:7^1		D_DQ17	22	S_E3:1^1
	D_DQ48	99	S_D1:6^1		D_DQ16	21	S_E3:4^1
	D_DQ47	216	S_D1:4^1		D_DQ15	138	S_E3:6^1
	D_DQ46	215	S_D1:1^1		D_DQ14	137	S_E3:7^1
	D_DQ45	210	S_D0:7^1		D_DQ13	132	S_E1:4^1
	D_DQ44	209	S_D0:6^1		D_DQ12	131	S_E1:1^1
	D_DQ43	97	S_D1:3^1		D_DQ11	19	S_E3:5^1
	D_DQ42	96	S_D1:2^1		D_DQ10	18	S_E1:7^1
	D_DQ41	91	S_D0:5^1		D_DQ9	13	S_E1:3^1
	D_DQ40	90	S_D0:4^1		D_DQ8	12	S_E1:2^1
	D_DQ39	207	S_D0:3^1		D_DQ7	129	S_E1:0^1
	D_DQ38	206	S_D0:2^1		D_DQ6	128	S_E0:7^1
	D_DQ37	201	S_C2:1^1		D_DQ5	123	S_E0:3^1
	D_DQ36	200	S_C2:4^1		D_DQ4	122	S_E0:2^1
	D_DQ35	88	S_D0:1^1		D_DQ3	10	S_Q2^1
	D_DQ34	87	S_D0:0^1		D_DQ2	9	S_E0:5^1
	D_DQ33	83	S_C2:6^1		D_DQ1	4	S_E0:1^1
	D_DQ32	81	S_C2:7^1		D_DQ0	3	S_E0:0^1

Table 5 – R_DDR3D_2A (<=1866MT/s Read and Write) Storage and Trigger Grouping (cont'd.)

Notes:

1. All signals on this page are required for accurate post-processing of acquired data
2. The 'S' in front of a TLA channel denotes the Slave card of the merged pair
3. Signals in these groups are acquired using the 7Bx4s's demux capability and will not have a MagniVu display value

Group Name	Signal Name	DDR3 Pin #	TLA Input	Group Name	Signal Name	DDR3 Pin #	TLA Input
AChkBits	A_CB7	165	M_D3:5	CChkBits [3]	C_CB7	165	M_D3:5^1
(OFF)	A_CB6	164	M_D3:4	(OFF)	C_CB6	164	M_D3:4^1
	A_CB5	159	M_D3:0		C_CB5	159	M_D3:0^1
	A_CB4	158	M_D2:7		C_CB4	158	M_D2:7^1
	A_CB3	46	M_D3:6		C_CB3	46	M_D3:6^1
	A_CB2	45	M_D3:3		C_CB2	45	M_D3:3^1
	A_CB1	40	M_Q0		C_CB1	40	M_Q0^1
	A_CB0	39	M_D2:5		C_CB0	39	M_D2:5^1
BChkBits	B_CB7	165	S_D3:5	DChkBits [3]	D_CB7	165	S_D3:5^1
(OFF)	B_CB6	164	S_D3:4	(OFF)	D_CB6	164	S_D3:4^1
	B_CB5	159	S_D3:0		D_CB5	159	S_D3:0^1
	B_CB4	158	S_D2:7		D_CB4	158	S_D2:7^1
	B_CB3	46	S_D3:6		D_CB3	46	S_D3:6^1
	B_CB2	45	S_D3:3		D_CB2	45	S_D3:3^1
	B_CB1	40	S_Q0		D_CB1	40	S_Q0^1
	B_CB0	39	S_D2:5		D_CB0	39	S_D2:5^1
ADatMsks	a_DM8	161	M_D3:1	BDatMsks	b_DM8	161	S_D3:1
(BIN)	a_DM7	230	M_A0:5	(BIN)	b_DM7	230	S_A0:5
	a_DM6	221	M_A1:6		b_DM6	221	S_A1:6
	a_DM5	212	M_D1:0		b_DM5	212	S_D1:0
	a_DM4	203	M_C2:0		b_DM4	203	S_C2:0
	a_DM3	152	M_D2:2		b_DM3	152	S_D2:2
	a_DM2	143	M_Q3		b_DM2	143	S_Q3
	a_DM1	134	M_E1:5		b_DM1	134	S_E1:5
	a_DM0	125	M_E0:6		b_DM0	125	S_E0:6
CDatMsks [3]	c_DM8	161	M_D3:1^1	DDatMsks [3]	d_DM8	161	S_D3:1^1
(BIN)	c_DM7	230	M_A0:5^1	(BIN)	d_DM7	230	S_A0:5^1
	c_DM6	221	M_A1:6^1		d_DM6	221	S_A1:6^1
	c_DM5	212	M_D1:0^1		d_DM5	212	S_D1:0^1
	c_DM4	203	M_C2:0^1		d_DM4	203	S_C2:0^1
	c_DM3	152	M_D2:2^1		d_DM3	152	S_D2:2^1
	c_DM2	143	M_Q3^1		d_DM2	143	S_Q3^1
	c_DM1	134	M_E1:5^1		d_DM1	134	S_E1:5^1
	c_DM0	125	M_E0:6		d_DM0	125	S_E0:6

Table 5 – R_DDR3D_2A (<=1866MT/s Read and Write) Storage and Trigger Grouping (cont'd.)

Notes:

1. The 'M' in front of a TLA channel denotes the Master card of the merged pair
2. The 'S' in front of a TLA channel denotes the Slave card of the merged pair
3. Signals in these groups are stored in the 7Bx4's Prime memory and will not have a MagniVu display value

Group Name	Signal Name	DDR3 Pin #	TLA Input	Group Name	Signal Name	DDR3 Pin #	TLA Input
Control_0 [2]	CKE1_0	169	M_A3:2	Control_1 [2,5]	CKE1_1	169	M_A3:2^1
(SYM)	CKE0_0	50	M_A3:1	(SYM)	CKE0_1	50	M_A3:1^1
	S3#_0	49	M_C2:5		S3#_1	49	M_C2:5^1
	S2#_0	48	M_C3:0		S2#_1	48	M_C3:0^1
	S1#_0	76	M_C3:4		S1#_1	76	M_C3:4^1
	S0#_0	193	M_C3:3		S0#_1	193	M_C3:3^1
	BA2_0	52	M_A3:0		BA2_1	52	M_A3:0^1
	BA1_0	190	M_C3:7		BA1_1	190	M_C3:7^1
	BA0_0	71	M_C1:6		BA0_1	71	M_C1:6^1
	A15_0	171	M_CK0		A15_1	171	M_CK0^1
	A14_0	172	M_A2:5		A14_1	172	M_A2:5^1
	A13_0	196	M_CK3		A13_1	196	M_CK3^1
	A12/BC#_0	174	M_A2:4		A12/BC#_1	174	M_A2:4^1
	A10/AP_0	70	M_C1:3		A10/AP_1	70	M_C1:3^1
	RAS#_0	192	M_C3:6		RAS#_1	192	M_C3:6^1
	CAS#_0	74	M_C3:5		CAS#_1	74	M_C3:5^1
	WE#_0	73	M_C1:7		WE#_1	73	M_C1:7^1
Address_0 [2]	BA2_0	52	M_A3:0	Address_1 [2,5]	BA2_1	52	M_A3:0^1
(Hex)	BA1_0	190	M_C3:7	(Hex)	BA1_1	190	M_C3:7^1
	BA0_0	71	M_C1:6		BA0_1	71	M_C1:6^1
	A15_0	171	M_CK0		A15_1	171	M_CK0^1
	A14_0	172	M_A2:5		A14_1	172	M_A2:5^1
	A13_0	196	M_CK3		A13_1	196	M_CK3^1
	A12/BC#_0	174	M_A2:4		A12/BC#_1	174	M_A2:4^1
	A11_0	55	M_A2:6		A11_1	55	M_A2:6^1
	A10/AP_0	70	M_C1:3		A10/AP_1	70	M_C1:3^1
	A9_0	175	M_A2:1		A9_1	175	M_A2:1^1
	A8_0	177	M_A2:0		A8_1	177	M_A2:0^1
	A7_0	56	M_A2:3		A7_1	56	M_A2:3^1
	A6_0	178	M_C0:2		A6_1	178	M_C0:2^1
	A5_0	58	M_A2:2		A5_1	58	M_A2:2^1
	A4_0	59	M_C0:5		A4_1	59	M_C0:5^1
	A3_0	180	M_C1:0		A3_1	180	M_C1:0^1
	A2_0	61	M_Q1		A2_1	61	M_Q1^1
	A1_0	181	M_C1:1		A1_1	181	M_C1:1^1
	A0_0	188	M_C1:5		A0_1	188	M_C1:5^1

Table 5 – R_DDR3D_2A (<=1866MT/s Read and Write) Storage and Trigger Grouping (cont'd.)

Notes:

1. ' # ' denotes a low-true signal
2. These signals are required for accurate acquisition and post-processing of acquired data
3. The 'M' in front of a TLA channel denotes the Master card of the merged pair
4. The 'S' in front of a TLA channel denotes the Slave card of the merged pair
5. Signals in these groups are stored in the 7Bx4's Prime memory and will not have a MagniVu display value

Group Name	Signal Name	DDR3 Pin #	TLA Input	Group Name	Signal Name	DDR3 Pin #	TLA Input
Ungrouped	PAR_IN_0	68	M_C1:2	Ungrouped	RESET#_0	168	M_A3:6
	PAR_IN_1	68	M_C1:2^1		RESET#_1	168	M_A3:6^1
	ERR_OUT#[3]_0	53	M_A2:7		ODT1_0	77	M_C3:1
	ERR_OUT#[3]_1	53	M_A2:7^1		ODT1_1	77	M_C3:1^1
	TEST_0	167	M_A3:7		ODT0_0	195	M_C3:2
	TEST_1	167	M_A3:7^1		ODT0_1	195	M_C3:2^1
					DDRCLK		M_C1:4
					DQS8		M_D3:2

Table 5 – R_DDR3D_2A (<=1866MT/s Read and Write) Storage and Trigger Grouping (cont'd.)

Notes:

1. ' # ' denotes a low-true signal
2. The 'M' in front of a TLA channel denotes the Master card of the merged pair
3. The 'S' in front of a TLA channel denotes Slave card #1 of the merged pair
4. Signals with a '^1' suffix are stored in the 7Bx4's Prime memory and will not have a MagniVu display value

3.8 Display Groups not in Tables 2, 3, 4 or 5

There are several groups in the List window that are not documented in the tables as these groups are used only by the post-processing display software. To ensure correct data display these groups must not be modified. These groups are:

DataHi
DataLo
ChekBits
DataMasks
MRSAddr

4.0 CLOCK SELECTION

4.1 B_DDR3D_2D Clocking Selections

There are two clocking option fields available when using the B_DDR3D_2D support package. These select fields permit the user to setup the TLA acquisition as follows:

SDRAM Clocking: – Permits selecting the Clocking Mode to be used to acquire DDR3 data. It is important to note that the selection chosen will force unused Chip Selects and CKE1 into inactive states. The field choices are:

S0#; Every Rising Edge (default) – Clocks data using every rising edge of DDR Clock 0. Forces CKE1 low and S1-3# high. No Idle Cycle filtering is done.

S0# & S1#; Every Rising Edge – Clocks data using every rising edge of DDR Clock 0. Forces S2-3# high. No Idle Cycle filtering is done.

S0-3#; Every Rising Edge – Clocks data using every rising edge of DDR Clock 0. No Idle Cycle filtering is done.

S0#; Total L <=5 – utilizes Selective Clocking to reduce acquisition of Idle bus states. Forces CKE1 low and S1-3# high.

S0# & S1#; Total L <=5 - utilizes Selective Clocking to reduce acquisition of Idle bus states. Forces S2-3# high.

S0-3#; Total L <=5 - utilizes Selective Clocking to reduce acquisition of Idle bus states.

S0#; Total L <=6
S0# & S1#; Total L <=6
S0-3#; Total L <=6
.
.
.
S0#; Total L <=25
S0# & S1#; Total L <=25
S0-3#; Total L <=25

The above selections reduce the number of Idle cycles stored by the acquisition card to provide optimum use of the acquisition memory. Data is stored whenever RAS# or CAS# is asserted low along with a valid Chip Select. After every assertion of CAS# (paired with a valid Chip Select) samples are taken during the next *X* DDR Clock cycles to ensure that all valid memory cycles have been acquired. The acquisition then pauses and waits for the next Command. If CAS# and a Chip Select are asserted during these *X* clock cycles the count is reset. The *X*-clock cycle value is determined by adding the maximum Burst Length of 8

clock cycles to the selected maximum Read Latency. So for a selected Total Latency of <= 5 cycles the support software will store a total of 13 clock cycles worth of data after the Read or Write Command appears on the bus.

Refresh Cycles: – Permits choosing whether Refresh Cycles will be stored or not. The field choices are:

Acquire (default) – Refresh Cycles will be stored.

Do Not Acquire – This mode will reduce the number of Refresh cycles stored by the acquisition card to provide optimum use of the acquisition memory.

NOTE: This mode is disabled when the SDRAM Clocking choice is set to a **Every Rising Edge** selection.

4.2 B_DDR3D_4A Clocking Selections

There is one clocking option field available when using the B_DDR3D_4A support package. These select fields permit the user to setup the TLA acquisition as follows:

SDRAM DDR CLK0 Clocking: – Permits selecting the Clocking Mode to be used to acquire DDR3 data. It is important to note that the selection chosen will force unused Chip Selects and CKE1 into inactive states. The field choices are:

S0#; Every Rising Edge (default) – Clocks data using every rising edge of DDR Clock 0. Forces CKE1 low and S1-3# high. No Idle Cycle filtering is done.

S0# & S1#; Every Rising Edge – Clocks data using every rising edge of DDR Clock 0. Forces S2-3# high. No Idle Cycle filtering is done.

S0-3#; Every Rising Edge – Clocks data using every rising edge of DDR Clock 0. No Idle Cycle filtering is done.

4.3 R_DDR3D_1A Clocking Selections

There are three clocking option fields available when using the R_DDR3D_1A support package. These select fields permit the user to setup the TLA acquisition as follows:

Active Chip Selects / Write Latencies: – Allows the user to set the number of active ranks (Chip Selects) that the target DIMM will be using and the Write Latency for the data bus. The field choices are:

___0 1r WL5 (default) – Single Rank DIMM (S0# only active) with a Write Latency of 5 cycles.

__10 2r WL5 – Dual Rank DIMM (S0# and S1# active) with a Write Latency of 5 cycles.

3210 4r WL5 – Quad Rank DIMM (S0-3# active) with a Write Latency of 5 cycles.

___0 1r WL6 – Single Rank DIMM (S0# only active) with a Write Latency of 6 cycles.

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3210 4r WL12 – Quad Rank DIMM (S0-3# active) with a Write Latency of 12 cycles.

Clocking Mode: – Permits choosing whether to acquire data based on the state of the two CKE signals. The field choices are:

CKE Enabled Clocking (default) – Minimizes acquired data when both CKE signals are low (inactive).

Every rising clock edge – Acquires data on every DDRCLK0 rising edge regardless of the state of the CKE signals.

Burst Length: – Permits setting the length of data Bursts The field choices are:

BL8 (default) – Assumes a Burst Length of 8 data transactions.

BL4 – Assumes a Burst Length of 4.

BC# – Monitors the state of the A12/BC# at the time of the Command cycle to determine whether the burst length will be 4 or 8 transactions.

4.4 R_DDR3D_2A Clocking Selections

There are two clocking option fields available when using the R_DDR3D_2A support package. These select fields permit the user to setup the TLA acquisition as follows:

Active Chip Selects / Write Latencies: – Allows the user to set the number of active ranks (Chip Selects) that the target DIMM will be using and the Write Latency for the data bus. The field choices are:

___0 1r WL5 (default) – Single Rank DIMM (S0# only active) with a Write Latency of 5 cycles.

__10 2r WL5 – Dual Rank DIMM (S0# and S1# active) with a Write Latency of 5 cycles.

3210 4r WL5 – Quad Rank DIMM (S0-3# active) with a Write Latency of 5 cycles.

___0 1r WL6 – Single Rank DIMM (S0# only active) with a Write Latency of 6 cycles.

.
.
.

3210 4r WL12 – Quad Rank DIMM (S0-3# active) with a Write Latency of 12 cycles.

Clocking Mode: – Permits choosing whether to acquire data based on the state of the two CKE signals. The field choices are:

CKE Enabled Clocking (1r only) (default) – Minimizes acquired data when both CKE signals are low (inactive) and a Single Rank clocking choice (see Active Chip Selects / Write Latencies description above) is selected.

Every rising clock edge – Acquires data on every DDRCLK0 rising edge regardless of the state of the CKE signals.

Burst Length: – Permits setting the length of data Bursts The field choices are:

BL8 (default) – Assumes a Burst Length of 8 data transactions.

BL4 – Assumes a Burst Length of 4.

5.0 CONFIGURING FOR READ / WRITE DATA ACQUISITION

Prior to configuring your NEX-DDR3INTR-HS support package it is strongly recommended that Appendix A ("How DDR Data is Clocked"), section 5.4 ("Selecting DDR Read Sample Points") and section 5.5. ("Selecting DDR Write Sample Points") be read. This background information is very helpful and facilitates proper support configuration.

5.1 A Note About the Different Data Groups

The NEX-DDR3INTR-HS support software have three different areas where signal groups are defined to provide specific functionality. There are the MagniVu data groups (see Tables 6, 7, 8 and 9) are the groups that contain raw MagniVu data. Storage data groups (see Tables 2, 3, 4 and 5) can be seen in the acquisition card Setup window and contain the data stored in Main Memory which is used for the Listing display. Capture data groups (not defined in this manual) are the groups seen in the TLA's Setup & Hold dialog box and are the groups used to capture data during each DDR clock cycle. The MagniVu and Capture data groups will be referred to in the following explanation on determining and setting the correct sample points to acquire Read and Write data. Please contact your local Tektronix representative for a detailed explanation of the different data group areas and what they mean.

5.2 MagniVu Signals

Because of the design of the Tektronix TLA7Bx4 acquisition cards different data groups need to be defined for use within MagniVu. *Table 6* shows the MagniVu group definitions in the B_DDR3D_2D support; *Table 7* shows the MagniVu group definitions in the B_DDR3D_4A support.; *Table 8* the R_DDR3D_1A support definitions; *Table 9* those for the R_DDR3D_2A support.

Group Name	Signal Name	TLA Input	Group Name	Signal Name	TLA Input
Data_Hi	DQ63	S_A2:0	Data_Lo	DQ31	M_A0:6
	DQ62	S_A2:1		DQ30	M_A0:3
	DQ61	S_A2:5		DQ29	S_C2:0
	DQ60	S_CK0		DQ28	S_C2:1
	DQ59	S_A2:2		DQ27	M_A0:4
	DQ58	S_A2:3		DQ26	M_A0:1
	DQ57	S_A2:7		DQ25	S_C2:2
	DQ56	S_A3:0		DQ24	S_C2:3
	DQ55	S_A3:2		DQ23	S_C2:4
	DQ54	S_A3:3		DQ22	S_C2:5
	DQ53	S_A3:7		DQ21	S_C3:2
	DQ52	S_A1:5		DQ20	S_C3:3
	DQ51	S_A3:1		DQ19	S_C2:6
	DQ50	S_A3:4		DQ18	S_C2:7
	DQ49	S_A1:7		DQ17	S_C3:1
	DQ48	S_A1:6		DQ16	S_C3:4
	DQ47	S_A1:4		DQ15	S_C3:6
	DQ46	S_A1:1		DQ14	S_C3:7
	DQ45	S_A0:7		DQ13	S_E3:4
	DQ44	S_A0:6		DQ12	S_E3:1
	DQ43	S_A1:3		DQ11	S_C3:5
	DQ42	S_A1:2		DQ10	S_E3:7
	DQ41	S_A0:5		DQ9	S_E3:3
	DQ40	S_A0:4		DQ8	S_E3:2
	DQ39	S_A0:3		DQ7	S_E3:0
	DQ38	S_A0:2		DQ6	S_E2:7
	DQ37	M_C2:1		DQ5	S_E2:3
	DQ36	M_C2:4		DQ4	S_E2:2
	DQ35	S_A0:1		DQ3	S_Q3
	DQ34	S_A0:0		DQ2	S_E2:5
	DQ33	M_C2:6		DQ1	S_E2:1
	DQ32	M_C2:7		DQ0	S_E2:0

Table 6 - B_DDR3D_2D (<=1333MT/s Read and Write) MagniVu Channel Grouping

Notes:

1. The ‘M’ in front of a TLA channel denotes the Master card of the merged pair
2. The ‘S’ in front of a TLA channel denotes the Slave card of the merged pair

Group Name	Signal Name	TLA Input	Group Name	Signal Name	TLA Input
DataByte7	DQ63	S_A2:0	DataByte3	DQ31	M_A0:6
	DQ62	S_A2:1		DQ30	M_A0:3
	DQ61	S_A2:5		DQ29	S_C2:0
	DQ60	S_CK0		DQ28	S_C2:1
	DQ59	S_A2:2		DQ27	M_A0:4
	DQ58	S_A2:3		DQ26	M_A0:1
	DQ57	S_A2:7		DQ25	S_C2:2
	DQ56	S_A3:0		DQ24	S_C2:3
DataByte6	DQ55	S_A3:2	DataByte2	DQ23	S_C2:4
	DQ54	S_A3:3		DQ22	S_C2:5
	DQ53	S_A3:7		DQ21	S_C3:2
	DQ52	S_A1:5		DQ20	S_C3:3
	DQ51	S_A3:1		DQ19	S_C2:6
	DQ50	S_A3:4		DQ18	S_C2:7
	DQ49	S_A1:7		DQ17	S_C3:1
	DQ48	S_A1:6		DQ16	S_C3:4
DataByte5	DQ47	S_A1:4	DataByte1	DQ15	S_C3:6
	DQ46	S_A1:1		DQ14	S_C3:7
	DQ45	S_A0:7		DQ13	S_E3:4
	DQ44	S_A0:6		DQ12	S_E3:1
	DQ43	S_A1:3		DQ11	S_C3:5
	DQ42	S_A1:2		DQ10	S_E3:7
	DQ41	S_A0:5		DQ9	S_E3:3
	DQ40	S_A0:4		DQ8	S_E3:2
DataByte4	DQ39	S_A0:3	DataByte0	DQ7	S_E3:0
	DQ38	S_A0:2		DQ6	S_E2:7
	DQ37	M_C2:1		DQ5	S_E2:3
	DQ36	M_C2:4		DQ4	S_E2:2
	DQ35	S_A0:1		DQ3	S_Q3
	DQ34	S_A0:0		DQ2	S_E2:5
	DQ33	M_C2:6		DQ1	S_E2:1
	DQ32	M_C2:7		DQ0	S_E2:0

Table 6 – B_DDR3D_2D (<=1333MT/s Read and Write) MagniVu Channel Grouping (cont'd.)

Notes:

1. The 'M' in front of a TLA channel denotes the Master card of the merged pair
2. The 'S' in front of a TLA channel denotes the Slave card of the merged pair

Group Name	Signal Name	TLA Input	Group Name	Signal Name	TLA Input
CheckBits	CB7	M_A1:5	DataMasks	DM7	S_A2:4
	CB6	M_A1:4		DM6	S_A3:6
	CB5	M_A1:0		DM5	S_A1:0
	CB4	M_A0:7		DM4	M_C2:0
	CB3	M_A1:6		DM3	M_A0:2
	CB2	M_A1:3		DM2	S_CK3
	CB1	M_CK1		DM1	S_E3:5
	CB0	M_A0:5		DM0	S_E2:6
Strobes	DQS8	S_A2:6	Address	BA2	M_A3:0
	DQS7	S_A3:5		BA1	M_C3:7
	DQS6	S_CK1		BA0	M_C1:6
	DQS5	M_C2:3		A15	M_CK0
	DQS4	M_A0:1		A14	M_A2:5
	DQS3	S_C3:0		A13	M_CK3
	DQS2	S_E3:6		A12/BC#	M_A2:4
	DQS1	S_E2:4		A11	M_A2:6
	DQS0	S_E2:4		A10/AP	M_C1:3
Control	CKE1	M_A3:2		A9	M_A2:1
	CKE0	M_A3:1		A8	M_A2:0
	S3#	M_C2:5		A7	M_A2:3
	S2#	M_C3:0		A6	M_C0:2
	S1#	M_C3:4		A5	M_A2:2
	S0#	M_C3:3		A4	M_C0:5
	BA2	M_A3:0		A3	M_C1:0
	BA1	M_C3:7		A2	M_Q1
	BA0	M_C1:6		A1	M_C1:1
	A15	M_CK0		A0	M_C1:5
	A14	M_A2:5	Orphans	PAR_IN	M_C1:2
	A13	M_CK3		ERR_OUT#	S_A0:7
	A12/BC#	M_A2:4		TEST	S_A1:7
	A10/AP	M_C1:3		RESET#	S_A1:6
	RAS#	M_C3:6		ODT1	M_C3:1
	CAS#	M_C3:5		ODT0	M_C3:2
	WE#	M_C1:7	Misc [4]	MISC1	Placeholder
				MISC0	Placeholder
				DDRCK0	M_C1:4

Table 6 – B_DDR3D_2D (<=1333MT/s Read and Write) MagniVu Channel Grouping (cont'd.)

Notes:

1. ' # ' denotes a low-true signal
2. The 'M' in front of a TLA channel denotes the Master card of the merged pair
3. The 'S' in front of a TLA channel denotes the Slave card of the merged pair
4. MISC1 and MISC0 are placeholders only and will not have interesting data on them

Group Name	Signal Name	TLA Input	Group Name	Signal Name	TLA Input
RD_Data_Hi	RD_DQ63	S2_A0:0	RD_Data_Lo	RD_DQ31	S_A2:6
	RD_DQ62	S2_A0:1		RD_DQ30	S_A2:3
	RD_DQ61	S2_A0:5		RD_DQ29	S3_A0:0
	RD_DQ60	S2_CK1		RD_DQ28	S3_A0:1
	RD_DQ59	S2_A0:2		RD_DQ27	S_A2:4
	RD_DQ58	S2_A0:3		RD_DQ26	S_A2:1
	RD_DQ57	S2_A0:7		RD_DQ25	S3_A0:2
	RD_DQ56	S2_A1:0		RD_DQ24	S3_A0:3
	RD_DQ55	S2_A1:2		RD_DQ23	S3_A0:4
	RD_DQ54	S2_A1:3		RD_DQ22	S3_A0:5
	RD_DQ53	S2_A1:7		RD_DQ21	S3_A1:2
	RD_DQ52	S2_A3:5		RD_DQ20	S3_A1:3
	RD_DQ51	S2_A1:1		RD_DQ19	S3_A0:6
	RD_DQ50	S2_A1:4		RD_DQ18	S3_A0:7
	RD_DQ49	S2_A3:7		RD_DQ17	S3_A1:1
	RD_DQ48	S2_A3:6		RD_DQ16	S3_A1:4
	RD_DQ47	S2_A3:4		RD_DQ15	S3_A1:6
	RD_DQ46	S2_A3:1		RD_DQ14	S3_A1:7
	RD_DQ45	S2_A2:7		RD_DQ13	S3_A3:4
	RD_DQ44	S2_A2:6		RD_DQ12	S3_A3:1
	RD_DQ43	S2_A3:3		RD_DQ11	S3_A1:5
	RD_DQ42	S2_A3:2		RD_DQ10	S3_A3:7
	RD_DQ41	S2_A2:5		RD_DQ9	S3_A3:3
	RD_DQ40	S2_A2:4		RD_DQ8	S3_A3:2
	RD_DQ39	S2_A2:3		RD_DQ7	S3_A3:0
	RD_DQ38	S2_A2:2		RD_DQ6	S3_A2:7
	RD_DQ37	M_C2:1		RD_DQ5	S3_A2:3
	RD_DQ36	M_C2:4		RD_DQ4	S3_A2:2
	RD_DQ35	S2_A2:1		RD_DQ3	S3_CK0
	RD_DQ34	S2_A2:0		RD_DQ2	S3_A2:5
	RD_DQ33	M_C2:6		RD_DQ1	S3_A2:1
	RD_DQ32	M_C2:7		RD_DQ0	S3_A2:0

Table 7 - B_DDR3D_4A (<=1866MT/s Read and Write) MagniVu Channel Grouping

Notes:

1. The ‘M’ in front of a TLA channel denotes the Master card of the merged set
2. The ‘S’ in front of a TLA channel denotes Slave card #1 of the merged set
3. The ‘S2’ in front of a TLA channel denotes Slave card #2 of the merged set
4. The ‘S3’ in front of a TLA channel denotes Slave card #3 of the merged set

Group Name	Signal Name	TLA Input	Group Name	Signal Name	TLA Input
RD_DataByte7	RD_DQ63	S2_A0:0	RD_DataByte3	RD_DQ31	S_A2:6
	RD_DQ62	S2_A0:1		RD_DQ30	S_A2:3
	RD_DQ61	S2_A0:5		RD_DQ29	S3_A0:0
	RD_DQ60	S2_CK1		RD_DQ28	S3_A0:1
	RD_DQ59	S2_A0:2		RD_DQ27	S_A2:4
	RD_DQ58	S2_A0:3		RD_DQ26	S_A2:1
	RD_DQ57	S2_A0:7		RD_DQ25	S3_A0:2
	RD_DQ56	S2_A1:0		RD_DQ24	S3_A0:3
RD_DataByte6	RD_DQ55	S2_A1:2	RD_DataByte2	RD_DQ23	S3_A0:4
	RD_DQ54	S2_A1:3		RD_DQ22	S3_A0:5
	RD_DQ53	S2_A1:7		RD_DQ21	S3_A1:2
	RD_DQ52	S2_A3:5		RD_DQ20	S3_A1:3
	RD_DQ51	S2_A1:1		RD_DQ19	S3_A0:6
	RD_DQ50	S2_A1:4		RD_DQ18	S3_A0:7
	RD_DQ49	S2_A3:7		RD_DQ17	S3_A1:1
	RD_DQ48	S2_A3:6		RD_DQ16	S3_A1:4
RD_DataByte5	RD_DQ47	S2_A3:4	RD_DataByte1	RD_DQ15	S3_A1:6
	RD_DQ46	S2_A3:1		RD_DQ14	S3_A1:7
	RD_DQ45	S2_A2:7		RD_DQ13	S3_A3:4
	RD_DQ44	S2_A2:6		RD_DQ12	S3_A3:1
	RD_DQ43	S2_A3:3		RD_DQ11	S3_A1:5
	RD_DQ42	S2_A3:2		RD_DQ10	S3_A3:7
	RD_DQ41	S2_A2:5		RD_DQ9	S3_A3:3
	RD_DQ40	S2_A2:4		RD_DQ8	S3_A3:2
RD_DataByte4	RD_DQ39	S2_A2:3	RD_DataByte0	RD_DQ7	S3_A3:0
	RD_DQ38	S2_A2:2		RD_DQ6	S3_A2:7
	RD_DQ37	M_C2:1		RD_DQ5	S3_A2:3
	RD_DQ36	M_C2:4		RD_DQ4	S3_A2:2
	RD_DQ35	S2_A2:1		RD_DQ3	S3_CK0
	RD_DQ34	S2_A2:0		RD_DQ2	S3_A2:5
	RD_DQ33	M_C2:6		RD_DQ1	S3_A2:1
	RD_DQ32	M_C2:7		RD_DQ0	S3_A2:0

Table 7 – B_DDR3D_4A (<=1866MT/s Read and Write) MagniVu Channel Grouping (cont'd.)

Notes:

1. The 'M' in front of a TLA channel denotes the Master card of the merged set
2. The 'S' in front of a TLA channel denotes Slave card #1 of the merged set
3. The 'S2' in front of a TLA channel denotes Slave card #2 of the merged set
4. The 'S3' in front of a TLA channel denotes Slave card #3 of the merged set

Group Name	Signal Name	TLA Input	Group Name	Signal Name	TLA Input
WR_Data_Hi	WR_DQ63	S2_E2:0	WR_Data_Lo	WR_DQ31	S_C2:6
	WR_DQ62	S2_E2:1		WR_DQ30	S_C2:3
	WR_DQ61	S2_E2:5		WR_DQ29	S3_E2:0
	WR_DQ60	S2_Q3		WR_DQ28	S3_E2:1
	WR_DQ59	S2_E2:2		WR_DQ27	S_C2:4
	WR_DQ58	S2_E2:3		WR_DQ26	S_C2:1
	WR_DQ57	S2_E2:7		WR_DQ25	S3_E2:2
	WR_DQ56	S2_E3:0		WR_DQ24	S3_E2:3
	WR_DQ55	S2_E3:2		WR_DQ23	S3_E2:4
	WR_DQ54	S2_E3:3		WR_DQ22	S3_E2:5
	WR_DQ53	S2_E3:7		WR_DQ21	S3_E3:2
	WR_DQ52	S2_C3:5		WR_DQ20	S3_E3:3
	WR_DQ51	S2_E3:1		WR_DQ19	S3_E2:6
	WR_DQ50	S2_E3:4		WR_DQ18	S3_E2:7
	WR_DQ49	S2_C3:7		WR_DQ17	S3_E3:1
	WR_DQ48	S2_C3:6		WR_DQ16	S3_E3:4
	WR_DQ47	S2_C3:4		WR_DQ15	S3_E3:6
	WR_DQ46	S2_C3:1		WR_DQ14	S3_E3:7
	WR_DQ45	S2_C2:7		WR_DQ13	S3_C3:4
	WR_DQ44	S2_C2:6		WR_DQ12	S3_C3:1
	WR_DQ43	S2_C3:3		WR_DQ11	S3_E3:5
	WR_DQ42	S2_C3:2		WR_DQ10	S3_C3:7
	WR_DQ41	S2_C2:5		WR_DQ9	S3_C3:3
	WR_DQ40	S2_C2:4		WR_DQ8	S3_C3:2
	WR_DQ39	S2_C2:3		WR_DQ7	S3_C3:0
	WR_DQ38	S2_C2:2		WR_DQ6	S3_C2:7
	WR_DQ37	M_E2:1		WR_DQ5	S3_C2:3
	WR_DQ36	M_E2:4		WR_DQ4	S3_C2:2
	WR_DQ35	S2_C2:1		WR_DQ3	S3_CK3
	WR_DQ34	S2_C2:0		WR_DQ2	S3_C2:5
	WR_DQ33	M_E2:6		WR_DQ1	S3_C2:1
	WR_DQ32	M_E2:7		WR_DQ0	S3_C2:0

Table 7 – B_DDR3D_4A (<=1866MT/s Read and Write) MagniVu Channel Grouping (cont'd.)

Notes:

1. The 'M' in front of a TLA channel denotes the Master card of the merged set
2. The 'S' in front of a TLA channel denotes Slave card #1 of the merged set
3. The 'S2' in front of a TLA channel denotes Slave card #2 of the merged set
4. The 'S3' in front of a TLA channel denotes Slave card #3 of the merged set

Group Name	Signal Name	TLA Input	Group Name	Signal Name	TLA Input
WR_DataByte7	WR_DQ63	S2_E2:0	WR_DataByte3	WR_DQ31	S_C2:6
	WR_DQ62	S2_E2:1		WR_DQ30	S_C2:3
	WR_DQ61	S2_E2:5		WR_DQ29	S3_E2:0
	WR_DQ60	S2_Q3		WR_DQ28	S3_E2:1
	WR_DQ59	S2_E2:2		WR_DQ27	S_C2:4
	WR_DQ58	S2_E2:3		WR_DQ26	S_C2:1
	WR_DQ57	S2_E2:7		WR_DQ25	S3_E2:2
	WR_DQ56	S2_E3:0		WR_DQ24	S3_E2:3
WR_DataByte6	WR_DQ55	S2_E3:2	WR_DataByte2	WR_DQ23	S3_E2:4
	WR_DQ54	S2_E3:3		WR_DQ22	S3_E2:5
	WR_DQ53	S2_E3:7		WR_DQ21	S3_E3:2
	WR_DQ52	S2_C3:5		WR_DQ20	S3_E3:3
	WR_DQ51	S2_E3:1		WR_DQ19	S3_E2:6
	WR_DQ50	S2_E3:4		WR_DQ18	S3_E2:7
	WR_DQ49	S2_C3:7		WR_DQ17	S3_E3:1
	WR_DQ48	S2_C3:6		WR_DQ16	S3_E3:4
WR_DataByte5	WR_DQ47	S2_C3:4	WR_DataByte1	WR_DQ15	S3_E3:6
	WR_DQ46	S2_C3:1		WR_DQ14	S3_E3:7
	WR_DQ45	S2_C2:7		WR_DQ13	S3_C3:4
	WR_DQ44	S2_C2:6		WR_DQ12	S3_C3:1
	WR_DQ43	S2_C3:3		WR_DQ11	S3_E3:5
	WR_DQ42	S2_C3:2		WR_DQ10	S3_C3:7
	WR_DQ41	S2_C2:5		WR_DQ9	S3_C3:3
	WR_DQ40	S2_C2:4		WR_DQ8	S3_C3:2
WR_DataByte4	WR_DQ39	S2_C2:3	WR_DataByte0	WR_DQ7	S3_C3:0
	WR_DQ38	S2_C2:2		WR_DQ6	S3_C2:7
	WR_DQ37	M_E2:1		WR_DQ5	S3_C2:3
	WR_DQ36	M_E2:4		WR_DQ4	S3_C2:2
	WR_DQ35	S2_C2:1		WR_DQ3	S3_CK3
	WR_DQ34	S2_C2:0		WR_DQ2	S3_C2:5
	WR_DQ33	M_E2:6		WR_DQ1	S3_C2:1
	WR_DQ32	M_E2:7		WR_DQ0	S3_C2:0

Table 7 – B_DDR3D_4A (<=1866MT/s Read and Write) MagniVu Channel Grouping (cont'd.)

Notes:

1. The 'M' in front of a TLA channel denotes the Master card of the merged set
2. The 'S' in front of a TLA channel denotes Slave card #1 of the merged set
3. The 'S2' in front of a TLA channel denotes Slave card #2 of the merged set
4. The 'S3' in front of a TLA channel denotes Slave card #3 of the merged set

Group Name	Signal Name	TLA Input
CheckBits	CB7	S_A3:5
	CB6	S_A3:4
	CB5	S_A3:0
	CB4	S_A2:7
	CB3	S_A3:6
	CB2	S_A3:3
	CB1	S_CK0
	CB0	S_A2:5
Strobes [2]	DQS8	S_A3:2
	DQS7	S2_A0:6
	DQS6	S2_A1:5
	DQS5	S2_CK0
	DQS4	M_C2:3
	DQS3	S_A2:1
	DQS2	S3_A1:0
	DQS1	S3_A3:6
	DQS0	S3_A2:4
Control [2]	CKE1	S_A1:2
	CKE0	S_A1:1
	S3#	M_C2:5
	S2#	M_C3:0
	S1#	M_E3:4
	S0#	M_E3:3
	BA2	S_A1:2
	BA1	S_A1:1
	BA0	M_C2:5
	A15	M_C3:0
	A14	M_ C3:4
	A13	M_ C3:3
	A12/BC#	S_A1:0
	A10/AP	M_ C3:7
	RAS#	M_C1:6
	CAS#	M_C3:5
	WE#	M_C1:7

Group Name	Signal Name	TLA Input
DataMasks	DM8	S_C3:1
	DM7	S2_E2:4
	DM6	S2_E3:6
	DM5	S2_C3:0
	DM4	M_E2:0
	DM3	S_C2:2
	DM2	S3_Q3
	DM1	S3_C3:5
	DM0	S3_C2:6
Address [2]	BA2	S_A1:2
	BA1	S_A1:1
	BA0	M_C2:5
	A15	M_C3:0
	A14	M_ C3:4
	A13	M_ C3:3
	A12/BC#	S_A1:0
	A11	M_ C3:7
	A10/AP	M_C1:6
	A9	S_CK1
	A8	S_A0:5
	A7	M_CK3
	A6	S_A0:4
	A5	M_C1:3
	A4	M_C0:5
	A3	M_C1:0
	A2	M_Q1
	A1	M_C1:1
	A0	M_C1:5
Orphans	TEST	S_A1:7
	ERR_OUT#	S_A0:7
	PAR_IN	M_C1:2
	RESET#	S_A1:6
	ODT1	M_C3:1
	ODT0	M_C3:2
Misc [2]	DDRCK0	M_C1:4

Table 7 – B_DDR3D_4A (<=1866MT/s Read and Write) MagniVu Channel Grouping (cont'd.)

Notes:

1. ' # ' denotes a low-true signal
2. These signals are required for accurate determination of sample points
3. The 'M' in front of a TLA channel denotes the Master card of the merged set
4. The 'S' in front of a TLA channel denotes Slave card #1 of the merged set
5. The 'S2' in front of a TLA channel denotes Slave card #2 of the merged set
6. The 'S3' in front of a TLA channel denotes Slave card #3 of the merged set

Group Name	Signal Name	TLA Input	Group Name	Signal Name	TLA Input
Data_Hi	DQ63	A0:0	Data_Lo	DQ31	D2:6
	DQ62	A0:1		DQ30	D2:3
	DQ61	A0:5		DQ29	E2:0
	DQ60	CK1		DQ28	E2:1
	DQ59	A0:2		DQ27	D2:4
	DQ58	A0:3		DQ26	D2:1
	DQ57	A0:7		DQ25	E2:2
	DQ56	A1:0		DQ24	E2:3
	DQ55	A1:2		DQ23	E2:4
	DQ54	A1:3		DQ22	E2:5
	DQ53	A1:7		DQ21	E3:2
	DQ52	D1:5		DQ20	E3:3
	DQ51	A1:1		DQ19	E2:6
	DQ50	A1:4		DQ18	E2:7
	DQ49	D1:7		DQ17	E3:1
	DQ48	D1:6		DQ16	E3:4
	DQ47	D1:4		DQ15	E3:6
	DQ46	D1:1		DQ14	E3:7
	DQ45	D0:7		DQ13	E1:4
	DQ44	D0:6		DQ12	E1:1
	DQ43	D1:3		DQ11	E3:5
	DQ42	D1:2		DQ10	E1:7
	DQ41	D0:5		DQ9	E1:3
	DQ40	D0:4		DQ8	E1:2
	DQ39	D0:3		DQ7	E1:0
	DQ38	D0:2		DQ6	E0:7
	DQ37	C2:1		DQ5	E0:3
	DQ36	C2:4		DQ4	E0:2
	DQ35	D0:1		DQ3	Q2
	DQ34	D0:0		DQ2	E0:5
	DQ33	C2:6		DQ1	E0:1
	DQ32	C2:7		DQ0	E0:0

Table 8 - R_DDR3D_1A (<=1333MT/s Read and Write) MagniVu Channel Grouping

Group Name	Signal Name	TLA Input	Group Name	Signal Name	TLA Input
DataByte7	DQ63	A0:0	DataByte3	DQ31	D2:6
	DQ62	A0:1		DQ30	D2:3
	DQ61	A0:5		DQ29	E2:0
	DQ60	CK1		DQ28	E2:1
	DQ59	A0:2		DQ27	D2:4
	DQ58	A0:3		DQ26	D2:1
	DQ57	A0:7		DQ25	E2:2
	DQ56	A1:0		DQ24	E2:3
DataByte6	DQ55	A1:2	DataByte2	DQ23	E2:4
	DQ54	A1:3		DQ22	E2:5
	DQ53	A1:7		DQ21	E3:2
	DQ52	D1:5		DQ20	E3:3
	DQ51	A1:1		DQ19	E2:6
	DQ50	A1:4		DQ18	E2:7
	DQ49	D1:7		DQ17	E3:1
	DQ48	D1:6		DQ16	E3:4
DataByte5	DQ47	D1:4	DataByte1	DQ15	E3:6
	DQ46	D1:1		DQ14	E3:7
	DQ45	D0:7		DQ13	E1:4
	DQ44	D0:6		DQ12	E1:1
	DQ43	D1:3		DQ11	E3:5
	DQ42	D1:2		DQ10	E1:7
	DQ41	D0:5		DQ9	E1:3
	DQ40	D0:4		DQ8	E1:2
DataByte4	DQ39	D0:3	DataByte0	DQ7	E1:0
	DQ38	D0:2		DQ6	E0:7
	DQ37	C2:1		DQ5	E0:3
	DQ36	C2:4		DQ4	E0:2
	DQ35	D0:1		DQ3	Q2
	DQ34	D0:0		DQ2	E0:5
	DQ33	C2:6		DQ1	E0:1
	DQ32	C2:7		DQ0	E0:0

Table 8 – R_DDR3D_1A (<=1333MT/s Read and Write) MagniVu Channel Grouping (cont'd.)

Group Name	Signal Name	DDR3 Pin #	TLA Input	Group Name	Signal Name	DDR3 Pin #	TLA Input
Control[2]	CKE1	169	A3:2	Address[2]	BA2	52	A3:0
(SYM)	CKE0	50	A3:1	(Hex)	BA1	190	C3:7
	S3#	49	C2:5		BA0	71	C1:6
	S2#	48	C3:0		A15	171	CK0
	S1#	76	C3:4		A14	172	A2:5
	S0#	193	C3:3		A13	196	CK3
	BA2	52	A3:0		A12/BC#	174	A2:4
	BA1	190	C3:7		A11	55	A2:6
	BA0	71	C1:6		A10/AP	70	C1:3
	A15	171	CK0		A9	175	A2:1
	A14	172	A2:5		A8	177	A2:0
	A13	196	CK3		A7	56	A2:3
	A12/BC#	174	A2:4		A6	178	C0:2
	A10/AP	70	C1:3		A5	58	A2:2
	RAS#	192	C3:6		A4	59	C0:5
	CAS#	74	C3:5		A3	180	C1:0
	WE#	73	C1:7		A2	61	Q1
Strobes	DQS8	43	D3:2		A1	181	C1:1
(HEX)	DQS7	111	A0:6		A0	188	C1:5
	DQS6	103	A1:5	Orphans	DM8	161	D3:1
	DQS5	94	CK2		ERR_OUT#[3]	53	A2:7
	DQS4	85	C2:3		RESET#	168	A3:6
	DQS3	34	D2:0		TEST	167	A3:7
	DQS2	25	E3:2		ODT0	195	C3:2
	DQS1	16	E1:6		ODT1	77	C3:1
	DQS0	7	E0:4		PAR_IN	68	C1:2

Table 8 – R_DDR3D_1A (<=1333MT/s Read and Write) Storage and Trigger Grouping (cont'd.)

Notes:

1. ' # ' denotes a low-true signal

Group Name	Signal Name	TLA Input	Group Name	Signal Name	TLA Input
Data_Hi_M	DQ63_M	M_A0:0	Data_Lo_M	DQ31_M	M_D2:6
	DQ62_M	M_A0:1		DQ30_M	M_D2:3
	DQ61_M	M_A0:5		DQ29_M	M_E2:0
	DQ60_M	M_CK1		DQ28_M	M_E2:1
	DQ59_M	M_A0:2		DQ27_M	M_D2:4
	DQ58_M	M_A0:3		DQ26_M	M_D2:1
	DQ57_M	M_A0:7		DQ25_M	M_E2:2
	DQ56_M	M_A1:0		DQ24_M	M_E2:3
	DQ55_M	M_A1:2		DQ23_M	M_E2:4
	DQ54_M	M_A1:3		DQ22_M	M_E2:5
	DQ53_M	M_A1:7		DQ21_M	M_E3:2
	DQ52_M	M_D1:5		DQ20_M	M_E3:3
	DQ51_M	M_A1:1		DQ19_M	M_E2:6
	DQ50_M	M_A1:4		DQ18_M	M_E2:7
	DQ49_M	M_D1:7		DQ17_M	M_E3:1
	DQ48_M	M_D1:6		DQ16_M	M_E3:4
	DQ47_M	M_D1:4		DQ15_M	M_E3:6
	DQ46_M	M_D1:1		DQ14_M	M_E3:7
	DQ45_M	M_D0:7		DQ13_M	M_E1:4
	DQ44_M	M_D0:6		DQ12_M	M_E1:1
	DQ43_M	M_D1:3		DQ11_M	M_E3:5
	DQ42_M	M_D1:2		DQ10_M	M_E1:7
	DQ41_M	M_D0:5		DQ9_M	M_E1:3
	DQ40_M	M_D0:4		DQ8_M	M_E1:2
	DQ39_M	M_D0:3		DQ7_M	M_E1:0
	DQ38_M	M_D0:2		DQ6_M	M_E0:7
	DQ37_M	M_C2:1		DQ5_M	M_E0:3
	DQ36_M	M_C2:4		DQ4_M	M_E0:2
	DQ35_M	M_D0:1		DQ3_M	M_Q2
	DQ34_M	M_D0:0		DQ2_M	M_E0:5
	DQ33_M	M_C2:6		DQ1_M	M_E0:1
	DQ32_M	M_C2:7		DQ0_M	M_E0:0

Table 9 - R_DDR3D_2A (<=1866MT/s Read and Write) MagniVu Channel Grouping

Notes:

1. The ‘M’ in front of a TLA channel denotes the Master card of the merged pair

Group Name	Signal Name	TLA Input	Group Name	Signal Name	TLA Input
Data_Hi_S	DQ63_S	S_A0:0	Data_Lo_S	DQ31_S	S_D2:6
	DQ62_S	S_A0:1		DQ30_S	S_D2:3
	DQ61_S	S_A0:5		DQ29_S	S_E2:0
	DQ60_S	S_CK1		DQ28_S	S_E2:1
	DQ59_S	S_A0:2		DQ27_S	S_D2:4
	DQ58_S	S_A0:3		DQ26_S	S_D2:1
	DQ57_S	S_A0:7		DQ25_S	S_E2:2
	DQ56_S	S_A1:0		DQ24_S	S_E2:3
	DQ55_S	S_A1:2		DQ23_S	S_E2:4
	DQ54_S	S_A1:3		DQ22_S	S_E2:5
	DQ53_S	S_A1:7		DQ21_S	S_E3:2
	DQ52_S	S_D1:5		DQ20_S	S_E3:3
	DQ51_S	S_A1:1		DQ19_S	S_E2:6
	DQ50_S	S_A1:4		DQ18_S	S_E2:7
	DQ49_S	S_D1:7		DQ17_S	S_E3:1
	DQ48_S	S_D1:6		DQ16_S	S_E3:4
	DQ47_S	S_D1:4		DQ15_S	S_E3:6
	DQ46_S	S_D1:1		DQ14_S	S_E3:7
	DQ45_S	S_D0:7		DQ13_S	S_E1:4
	DQ44_S	S_D0:6		DQ12_S	S_E1:1
	DQ43_S	S_D1:3		DQ11_S	S_E3:5
	DQ42_S	S_D1:2		DQ10_S	S_E1:7
	DQ41_S	S_D0:5		DQ9_S	S_E1:3
	DQ40_S	S_D0:4		DQ8_S	S_E1:2
	DQ39_S	S_D0:3		DQ7_S	S_E1:0
	DQ38_S	S_D0:2		DQ6_S	S_E0:7
	DQ37_S	S_C2:1		DQ5_S	S_E0:3
	DQ36_S	S_C2:4		DQ4_S	S_E0:2
	DQ35_S	S_D0:1		DQ3_S	S_Q2
	DQ34_S	S_D0:0		DQ2_S	S_E0:5
	DQ33_S	S_C2:6		DQ1_S	S_E0:1
	DQ32_S	S_C2:7		DQ0_S	S_E0:0

Table 9 – R_DDR3D_2A (<=1333MT/s Read and Write) MagniVu Channel Grouping (cont'd.)

Notes:

1. The 'S' in front of a TLA channel denotes the Slave card of the merged pair

Group Name	Signal Name	TLA Input	Group Name	Signal Name	TLA Input
DataByte7_M	DQ63_M	M_A0:0	DataByte3_M	DQ31_M	M_D2:6
	DQ62_M	M_A0:1		DQ30_M	M_D2:3
	DQ61_M	M_A0:5		DQ29_M	M_E2:0
	DQ60_M	M_CK1		DQ28_M	M_E2:1
	DQ59_M	M_A0:2		DQ27_M	M_D2:4
	DQ58_M	M_A0:3		DQ26_M	M_D2:1
	DQ57_M	M_A0:7		DQ25_M	M_E2:2
	DQ56_M	M_A1:0		DQ24_M	M_E2:3
DataByte6_M	DQ55_M	M_A1:2	DataByte2_M	DQ23_M	M_E2:4
	DQ54_M	M_A1:3		DQ22_M	M_E2:5
	DQ53_M	M_A1:7		DQ21_M	M_E3:2
	DQ52_M	M_D1:5		DQ20_M	M_E3:3
	DQ51_M	M_A1:1		DQ19_M	M_E2:6
	DQ50_M	M_A1:4		DQ18_M	M_E2:7
	DQ49_M	M_D1:7		DQ17_M	M_E3:1
	DQ48_M	M_D1:6		DQ16_M	M_E3:4
DataByte5_M	DQ47_M	M_D1:4	DataByte1_M	DQ15_M	M_E3:6
	DQ46_M	M_D1:1		DQ14_M	M_E3:7
	DQ45_M	M_D0:7		DQ13_M	M_E1:4
	DQ44_M	M_D0:6		DQ12_M	M_E1:1
	DQ43_M	M_D1:3		DQ11_M	M_E3:5
	DQ42_M	M_D1:2		DQ10_M	M_E1:7
	DQ41_M	M_D0:5		DQ9_M	M_E1:3
	DQ40_M	M_D0:4		DQ8_M	M_E1:2
DataByte4_M	DQ39_M	M_D0:3	DataByte0_M	DQ7_M	M_E1:0
	DQ38_M	M_D0:2		DQ6_M	M_E0:7
	DQ37_M	M_C2:1		DQ5_M	M_E0:3
	DQ36_M	M_C2:4		DQ4_M	M_E0:2
	DQ35_M	M_D0:1		DQ3_M	M_Q2
	DQ34_M	M_D0:0		DQ2_M	M_E0:5
	DQ33_M	M_C2:6		DQ1_M	M_E0:1
	DQ32_M	M_C2:7		DQ0_M	M_E0:0

Table 9 – R_DDR3D_2A (<=1333MT/s Read and Write) MagniVu Channel Grouping (cont'd.)

Notes:

1. The 'M' in front of a TLA channel denotes the Master card of the merged pair

Group Name	Signal Name	TLA Input	Group Name	Signal Name	TLA Input
DataByte7_S	DQ63_S	S_A0:0	DataByte3_S	DQ31_S	S_D2:6
	DQ62_S	S_A0:1		DQ30_S	S_D2:3
	DQ61_S	S_A0:5		DQ29_S	S_E2:0
	DQ60_S	S_CK1		DQ28_S	S_E2:1
	DQ59_S	S_A0:2		DQ27_S	S_D2:4
	DQ58_S	S_A0:3		DQ26_S	S_D2:1
	DQ57_S	S_A0:7		DQ25_S	S_E2:2
	DQ56_S	S_A1:0		DQ24_S	S_E2:3
DataByte6_S	DQ55_S	S_A1:2	DataByte2_S	DQ23_S	S_E2:4
	DQ54_S	S_A1:3		DQ22_S	S_E2:5
	DQ53_S	S_A1:7		DQ21_S	S_E3:2
	DQ52_S	S_D1:5		DQ20_S	S_E3:3
	DQ51_S	S_A1:1		DQ19_S	S_E2:6
	DQ50_S	S_A1:4		DQ18_S	S_E2:7
	DQ49_S	S_D1:7		DQ17_S	S_E3:1
	DQ48_S	S_D1:6		DQ16_S	S_E3:4
DataByte5_S	DQ47_S	S_D1:4	DataByte1_S	DQ15_S	S_E3:6
	DQ46_S	S_D1:1		DQ14_S	S_E3:7
	DQ45_S	S_D0:7		DQ13_S	S_E1:4
	DQ44_S	S_D0:6		DQ12_S	S_E1:1
	DQ43_S	S_D1:3		DQ11_S	S_E3:5
	DQ42_S	S_D1:2		DQ10_S	S_E1:7
	DQ41_S	S_D0:5		DQ9_S	S_E1:3
	DQ40_S	S_D0:4		DQ8_S	S_E1:2
DataByte4_S	DQ39_S	S_D0:3	DataByte0_S	DQ7_S	S_E1:0
	DQ38_S	S_D0:2		DQ6_S	S_E0:7
	DQ37_S	S_C2:1		DQ5_S	S_E0:3
	DQ36_S	S_C2:4		DQ4_S	S_E0:2
	DQ35_S	S_D0:1		DQ3_S	S_Q2
	DQ34_S	S_D0:0		DQ2_S	S_E0:5
	DQ33_S	S_C2:6		DQ1_S	S_E0:1
	DQ32_S	S_C2:7		DQ0_S	S_E0:0

Table 9 – R_DDR3D_2A (<=1333MT/s Read and Write) MagniVu Channel Grouping (cont'd.)

Notes:

1. The 'S' in front of a TLA channel denotes the Slave card of the merged pair

Group Name	Signal Name	DDR3 Pin #	TLA Input
Control [2]	CKE1	169	M_A3:2
	CKE0	50	M_A3:1
	S3#	49	M_C2:5
	S2#	48	M_C3:0
	S1#	76	M_C3:4
	S0#	193	M_C3:3
	BA2	52	M_A3:0
	BA1	190	M_C3:7
	BA0	71	M_C1:6
	A15	171	M_CK0
	A14	172	M_A2:5
	A13	196	M_CK3
	A12/BC#	174	M_A2:4
	A10/AP	70	M_C1:3
	RAS#	192	M_C3:6
	CAS#	74	M_C3:5
	WE#	73	M_C1:7
CheckBits_M	CB7_M	165	M_D3:5
	CB6_M	164	M_D3:4
	CB5_M	159	M_D3:0
	CB4_M	158	M_D2:7
	CB3_M	46	M_D3:6
	CB2_M	45	M_D3:3
	CB1_M	40	M_Q0
	CB0_M	39	M_D2:5
CheckBits_S	CB7_S	165	S_D3:5
	CB6_S	164	S_D3:4
	CB5_S	159	S_D3:0
	CB4_S	158	S_D2:7
	CB3_S	46	S_D3:6
	CB2_S	45	S_D3:3
	CB1_S	40	S_Q0
	CB0_S	39	S_D2:5
Strobes	DQS7	111	M_A0:6
	DQS6	103	M_A1:5
	DQS5	94	M_CK2
	DQS4	85	M_C2:3
	DQS3	34	M_D2:0
	DQS2	25	M_E3:0
	DQS1	16	M_E1:6
	DQS0	7	M_E0:4

Group Name	Signal Name	DDR3 Pin #	TLA Input
Address [2]	BA2	52	M_A3:0
	BA1	190	M_C3:7
	BA0	71	M_C1:6
	A15	171	M_CK0
	A14	172	M_A2:5
	A13	196	M_CK3
	A12/BC#	174	M_A2:4
	A11	55	M_A2:6
	A10/AP	70	M_C1:3
	A9	175	M_A2:1
	A8	177	M_A2:0
	A7	56	M_A2:3
	A6	178	M_C0:2
	A5	58	M_A2:2
	A4	59	M_C0:5
	A3	180	M_C1:0
	A2	61	M_Q1
	A1	181	M_C1:1
	A0	188	M_C1:5
DataMasks_M	DM8_M	161	M_D3:1
	DM7_M	230	M_A0:5
	DM6_M	221	M_A1:6
	DM5_M	212	M_D1:0
	DM4_M	203	M_C2:0
	DM3_M	152	M_D2:2
	DM2_M	143	M_Q3
	DM1_M	134	M_E1:5
	DM0_M	125	M_E0:6
DataMasks_S	DM8_S	161	S_D3:1
	DM7_S	230	S_A0:5
	DM6_S	221	S_A1:6
	DM5_S	212	S_D1:0
	DM4_S	203	S_C2:0
	DM3_S	152	S_D2:2
	DM2_S	143	S_Q3
	DM1_S	134	S_E1:5
	DM0_S	125	S_E0:6
Misc	DDRCLK	184	M_C1:4
ODT	ODT1	77	M_C3:1
	ODT0	195	M_C3:2
Orphans	TEST	167	M_A3:7
	ERR_OUT#	53	M_A2:7
	PAR_IN	58	M_C1:2
	RESET#	49	M_A3:6

Table 9 – R_DDR3D_2A (<=1866MT/s Read and Write) Storage and Trigger Grouping (cont'd.)

Notes:

1. ' # ' denotes a low-true signal
2. These signals are required for accurate acquisition and post-processing of acquired data
3. The 'M' in front of a TLA channel denotes the Master card of the merged pair
4. The 'S' in front of a TLA channel denotes the Slave card of the merged pair

5.3 Adjusting Input Thresholds for Proper Data Acquisition

5.3.1 Thresholds for NEX-PRB1XL/PRB2XL Probes

The Interposer DDR3 support was designed to work with the new Nexus Low Profile Distributed probes. To maximize the electrical characteristics of the acquired waveforms the probe input resistors values were placed at 510 ohms. This value results in a divide by ten of the signals to the logic analyzer when using the NEX-PRB1X-T and NEX-PRB2X-T probes. The logic analyzer expects a divide by 20. Since the divide value is different than the standard Tektronix probe the voltage swing and offset will be higher than expected, and the thresholds will be different. Instead of the expected 0.75 threshold of approximately 1.9V threshold will be required. Use of the logic analyzer output to a scope will be required to determine the exact threshold for the system under test. Note that the Nexus SPA tool will fine adjust this threshold setting.

5.3.2 Thresholds for Tektronix P696xHCD Probes

Double probing the DDR3 data signals needed for 1866 MT/s acquisitions, yet reducing the load to that of a single probe resulted in a threshold setting on the logic analyzer that the user would not expect. The threshold setting, when using these probes with this product, is defaulted to 3.7V. This can be verified by viewing the signals via the Mux signal output in the front of the logic analyzer module. Note that the Nexus SPA tool will fine adjust this threshold setting.

5.4 DDR3 and DDR3SPA

It is strongly recommended that Nexus' DDR3SPA (DDR3 Sample Point Analyzer) be used to determine the proper sample point setting necessary for accurate Read and Write data acquisition. Given the correct DDR bus parameters (Latency, Burst Length, etc.) SPA will analyze any Read and/or Write bus transactions in MagniVu memory and return suggested sample points. Refer to the DDR SPA documentation for more specific information on using this software.

If for whatever reason DDR3SPA doesn't appear to provide good sample point setting information the following sections describe how to evaluate acquired DDR3 data to determine the proper sample points manually.

5.5 Selecting NEX-DDR3INTR-HS Read Data Sample Points

For the DDR3 Read data to be properly acquired it is necessary to choose the proper sample points to ensure that data is acquired at the proper point in the transaction. Since valid DDR3 Read data is straddled by the Strobes (see *Figure 5*) the Setup & Hold sample point must be set for the valid data that occurs closest to the clock edge. The appropriate clock edge for Reads is determined by adding the Additive Latency value to the CAS Latency value and adding one if

Registered memory (RDIMMs) are being used, resulting in the total number of clock cycles from the Read Command to the first valid Read Data. (If these values are not known the technique described in Section 7.3 can be used to determine the necessary values with the exception of whether or not the memory is RDIMM or UDIMM.) In *Figure 5* the total Read latency is 6 cycles.

The B_DDR3D_2D and R_DDR3D_1A supports sample Read data at two separate times based on each rising edge of the DDR3 clock and stores data every clock cycle. So to acquire both pieces of data the Read 'A' Data Hi/Lo capture groups must have their sample point set to that shown by Sample Pt. #1 in *Figure 5*, and the Read 'B' Data Hi/Lo capture groups must have their sample point set to that shown by Sample Pt. #2.

The B_DDR3D_4A and R_DDR3D_2A supports sample Read data on each rising edge of the DDR3 clock but data is stored every two clock cycles. So to acquire both pieces of data the Read 'A' Data Hi/Lo and Read 'C' Data Hi/Lo capture groups must have their sample point set to that shown by Sample Pt. #1 in *Figure 5*, and the Read 'B' Data Hi/Lo and Read 'D' Data Hi/Lo capture groups must have their sample point set to that shown in the Figure by Sample Pt. #2.

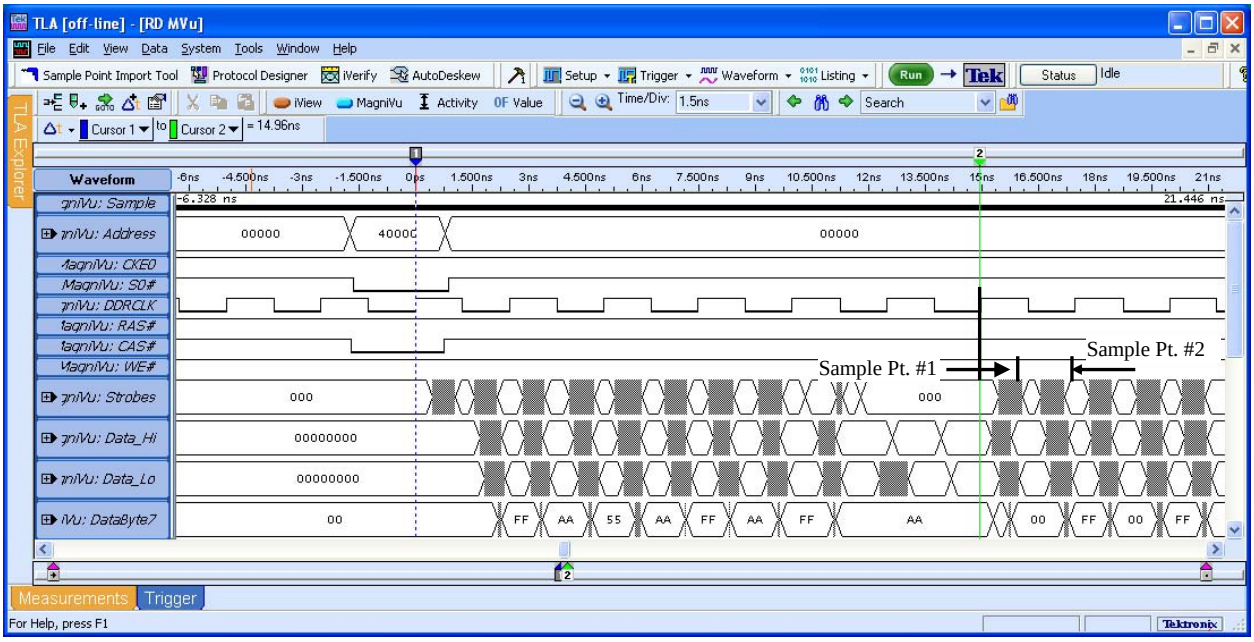


Figure 5 - Read Data Latency = CAS Latency + CAS Additive Latency + RDIMM (5+0+1) = 6 cycles)

5.6 Selecting NEX-DDR3INTR-HS Write Data Sample Points

Unlike valid DDR Read data, valid Write data is bisected by the Strobes. Since valid DDR3 Write data is bisected by the Strobes (see Figure 5) the Setup & Hold sample point must be set for the valid data that occurs closest to the clock edge. The appropriate clock edge for Writes is determined by counting the number of clock cycles specified by the Write Latency MRS value from the Write Command to the first valid Write Data. (If these values are not known the technique described in Section 7.3 can be used to determine them.) In *Figure 6* the total Write latency is 6 cycles (Write Latency plus the additional one cycle delay for RDIMM memory).

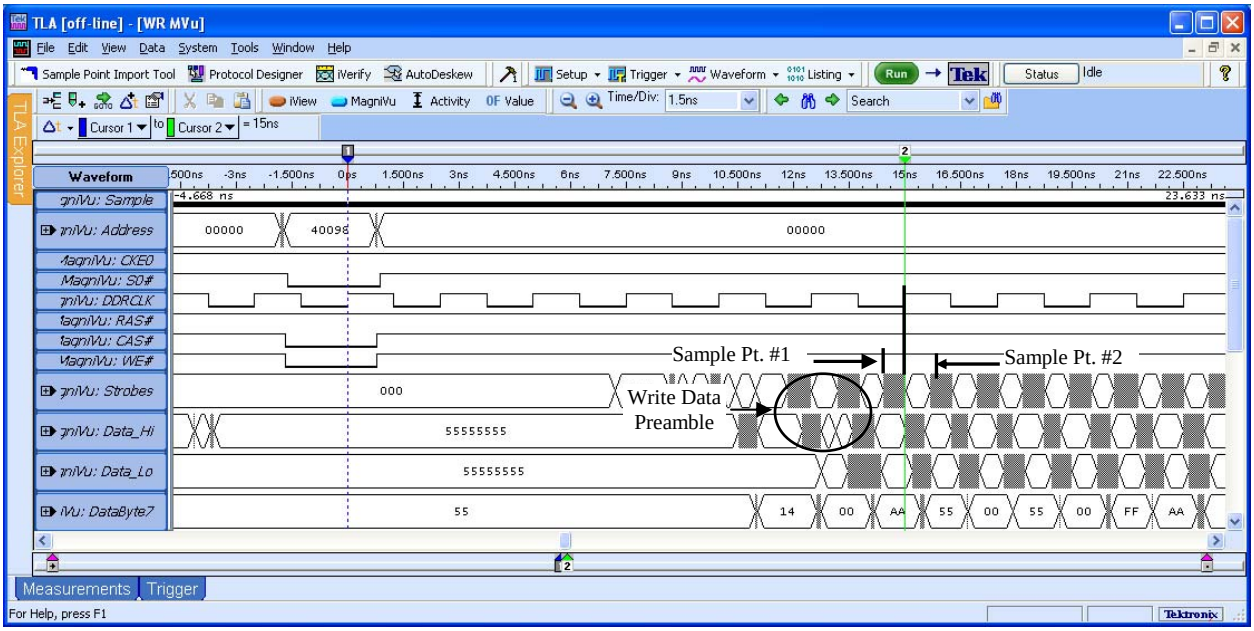


Figure 6 - Write Data Latency = CAS Write Latency + RDIMM (5+1) = 6 cycles

As with acquiring Read data the B_DDR3D_2D / R_DDR3D_1A supports sample Write data twice based on each rising edge of the DDR3 clock and stores data every clock cycle. So to acquire both pieces of data the Write 'A' Data Hi/Lo capture data groups must have their sample point set to that shown by Sample Pt. #1 in *Figure 6*, and the Write 'B' Data Hi/Lo capture groups must have their sample point set to that shown by Sample Pt. #2.

The B_DDR3D_4A / R_DDR3D_2A supports sample Write data twice based on each rising edge of the DDR3 clock but data is stored every two clock cycles. So to acquire both pieces of data the Write 'A' Data Hi/Lo and Write 'C' Data Hi/Lo capture groups must have their sample point set to that shown by Sample Pt. #1 in *Figure 6*, and the Write 'B' Data Hi/Lo and Write 'D' Data Hi/Lo capture groups must have their sample point set to that shown in the Figure by Sample Pt. #2.

NOTE - Because of the design of the TLA acquisition card inputs and the Strobe activity prior to Write data being placed on the data bus it will appear as if the Strobes indicate valid Write data earlier than the data is actually there (see the circle indicated as Write Data Preamble in

Figure 6). These Write Preamble Strobe edges should NOT be used to determine where valid Write data is on the data bus.

5.7 NEX-DDR3INTR-HS Support Setup

Using any of the NEX-DDR3INTR-HS supports it is possible to acquire both Read and Write data by setting the sample point of the data groups appropriately. The following explanation will permit a user to analyze acquired DDR3 data and determine what values to use in setting the Read data sample points.

To adjust the Read Data group sample points first make an appropriate acquisition of Read data by triggering on a Read command. Then create a timing window display of MagniVu data and display the Data Hi and Data Lo 32-bit data groups, the individual Command group signals and the DDR3 clock that was used for the data acquisition (DDRCK0). A sample waveform display of MagniVu Read data is shown in *Figure 7*. To determine the sample point, locate the smallest window of valid Read data during the acquired burst (see *Figure 7*). Note that in this instance the first piece of valid data happens significantly after the rising edge it is associated with. In fact the initial valid data appears at the DDR Clock falling edge. This delay must be taken into account or data will not be aligned properly in the Listing display window. Note that A and B data (corresponding to A and B data groups) have been indicated.

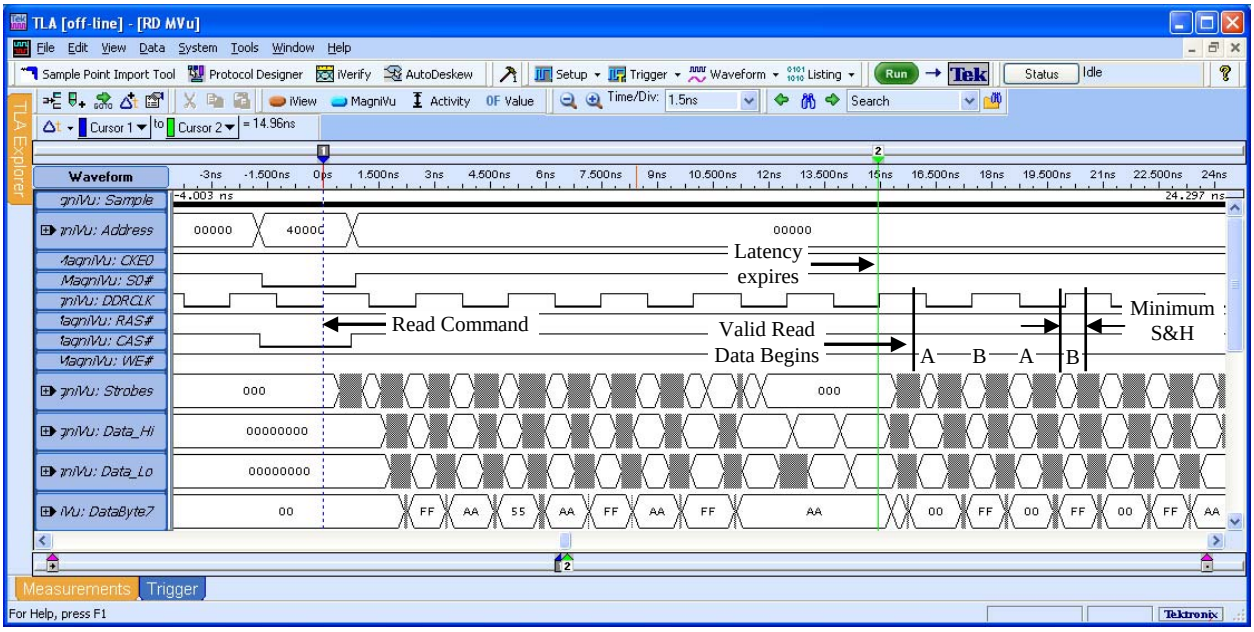


Figure 7 - Locating Minimum Valid NEX-DDR3INTR-HS Read Data Window

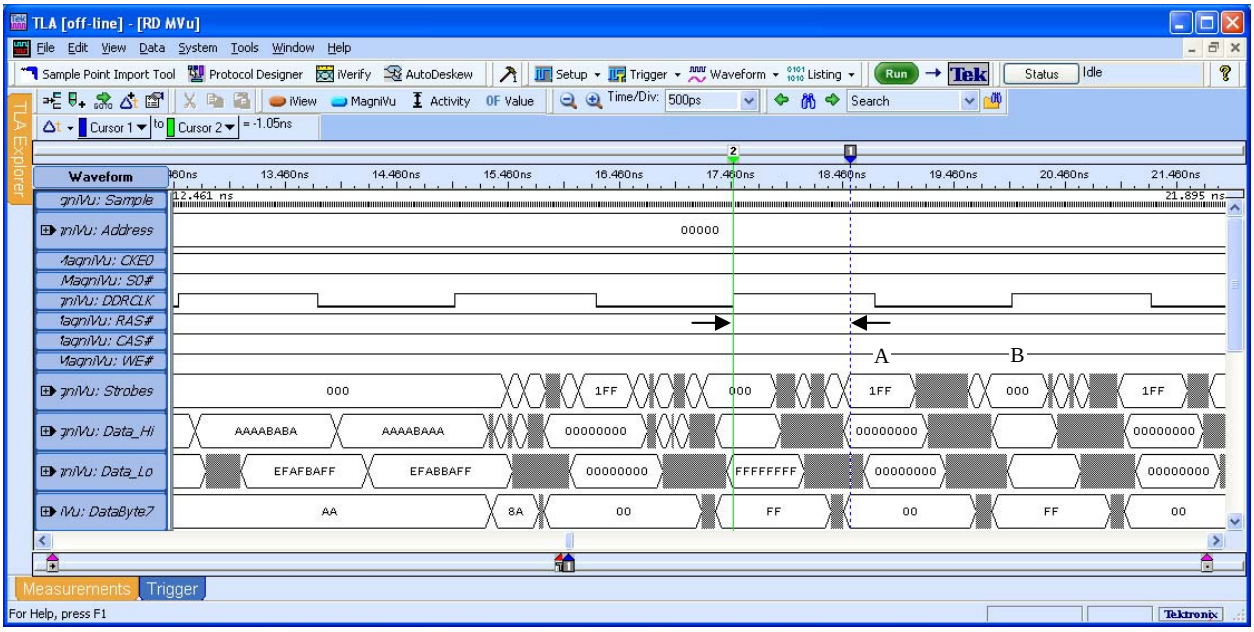


Figure 8 - Measuring NEX-DDR3INTR-HS ‘A’ Data Hi / Lo Read Data Setup & Hold

Zoom in further to determine the Setup and Hold sample point necessary to acquire valid data at that point (*Figure 8*) and use the cursors to measure the time from the clock edge to the start of valid Read data. In this example the delay from edge to data is approximately -1.05ns after the clock edge, meaning that a suitable Setup & Hold value for the ‘A’ Data Hi capture group would be -1.055ns/1.289ns. Note that the ‘A’ Data Lo group is valid somewhat later than the ‘A’ Data Hi group with its valid time starting at approximately 1.23ns after the clock edge, so the Setup & Hold sample point for the ‘A’ Data Lo capture group would be set to -1.23ns/1.465ns.

Now the sample point for the ‘B’ Data Hi and Lo groups must be determined (see *Figure 9*). The next valid Read data (after the cycle measured above) occurs approximately 2.37ns after the rising edge of DDRCK0, so a suitable Setup & Hold value for the B Data Hi capture group would be –2.383ns/2.617ns. As with the A data the ‘B’ Data Lo group is somewhat later than the ‘B’ Data Hi group. The ‘B’ Data Lo valid time starts at approximately -2.52ns so a suitable Setup & Hold value for the ‘B’ Data Lo capture group would be -2.52ns/2.754ns.

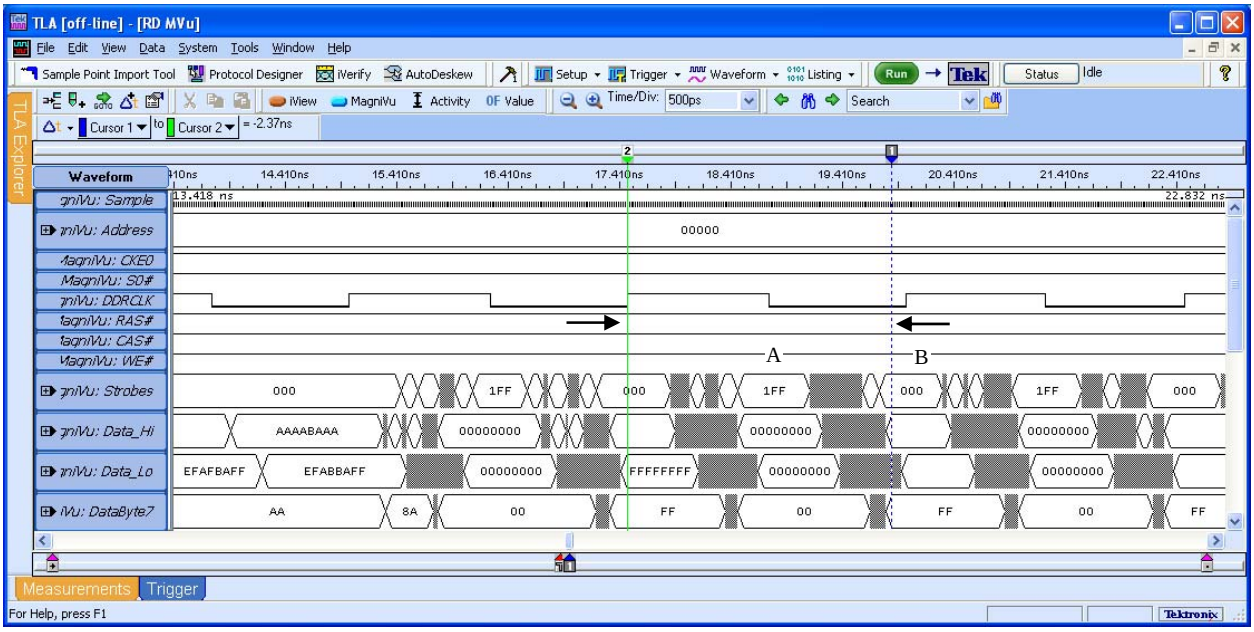


Figure 9 - Measuring NEX-DDR3INTR-HS 'B' Data Hi / Lo Read Data Setup & Hold

Now the sample point positions must be set for the 'A' Data Hi/Lo and 'B' Data Hi/Lo capture groups in the Setup window.

Each 32-bit data group will require its own value programmed from the measurements noted in the MagniVu window.

IMPORTANT – for the B_DDR3D_4A and R_DDR3D_2A supports the values used for the 'A' data groups must also be used for the 'C' data groups, and the values used for the 'B' data groups must also be used for the 'D' data groups.

The capture points are set in the Setup window within the B_DDR3D_XX / R_DDR3D_XX tab (see
Figure 10). In the lower right portion of the window is a scroll field. Scroll down until grayed-out groups are visible, then select the group in which the sample points are to be selected (*Figure 11*). Clicking on the Rising / Falling Edge icon (red arrow) will bring up the window shown in *Figure 12*. Set the Ts value for the Setup time derived from the analysis of the MagniVu data. This should automatically set the appropriate Hold time for the group. As mentioned above, when using the B_DDR3D_4A and R_DDR3D_1A supports the values used for the Read 'A' Data Hi/Lo capture groups must also be used for the Read 'C' Data Hi/Lo capture groups, and the values used for the Read 'B' Data Hi/Lo capture groups must also be used for the Read 'D' Data Hi/Lo capture groups.

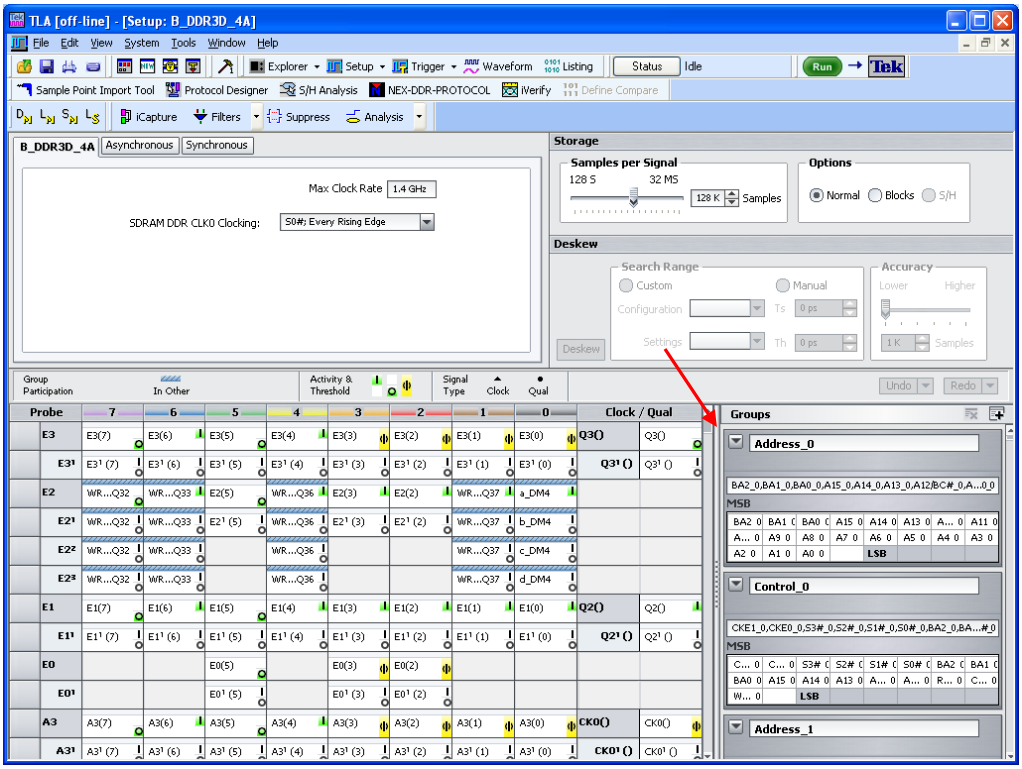


Figure 10 - NEX-DDR3INTR-HS Setup Window

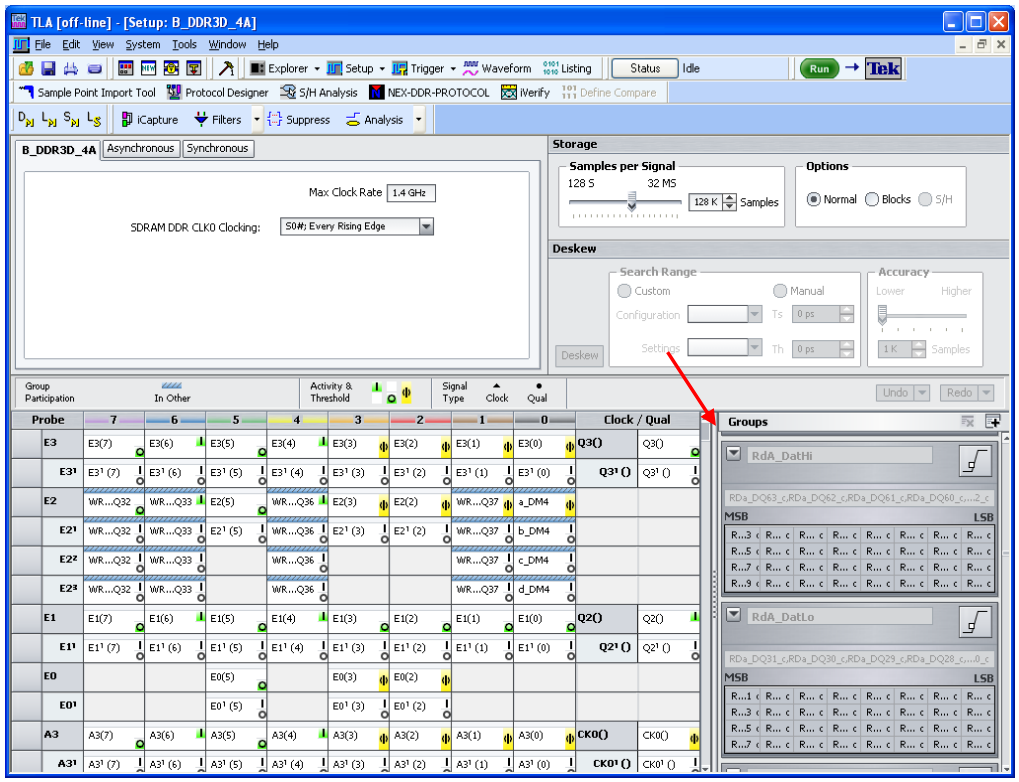


Figure 11 - NEX-DDR3INTR-HS Setup Window

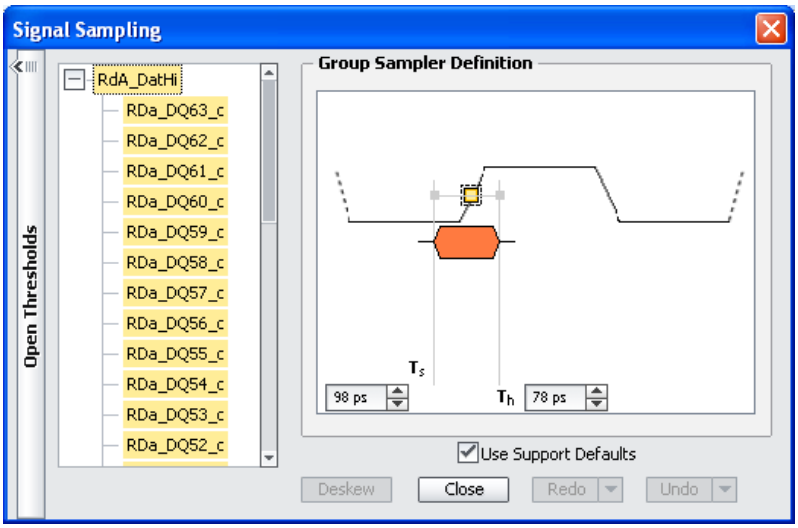


Figure 12 - NEX-DDR3INTR-HS Read Data Capture Point Window

Setting the Setup & Hold values for acquiring Write data is a similar process. To determine the Write Data group sample points first make an appropriate acquisition of Write data by triggering on a Write Command. Then, as above, create a timing window display of MagniVu data and display the Data Hi/Lo 32-bit data groups, the individual Command group signals and the DDR3 clock that was used for the data acquisition (DDRCK0).

NOTE – As mentioned earlier it is important to note that because of the design of the TLA acquisition card inputs and the Strobe activity prior to Write data being placed on the data bus it will appear as if the Strobes indicate valid Write data earlier than the data is actually there (see the circle indicated as Write Data Preamble in *Figure 6*). These Write Preamble Strobe edges should NOT be used to determine where valid Write data is on the data bus.

A sample waveform display of MagniVu Write data is shown in *Figure 13*. To determine the sample point, locate the smallest window of valid Write data during the acquired burst (see *Figure 13*). Note that in this instance the first piece of valid data happens before the rising edge it is associated with. This shift must be taken into account or data will not be aligned properly in the Listing display window. Note that A and B data (corresponding to ‘A’ Data Hi/Lo and ‘B’ Data Hi/Lo data groups) have been indicated. Refer to section 5.6 for important information on properly determining the Write data sample points.

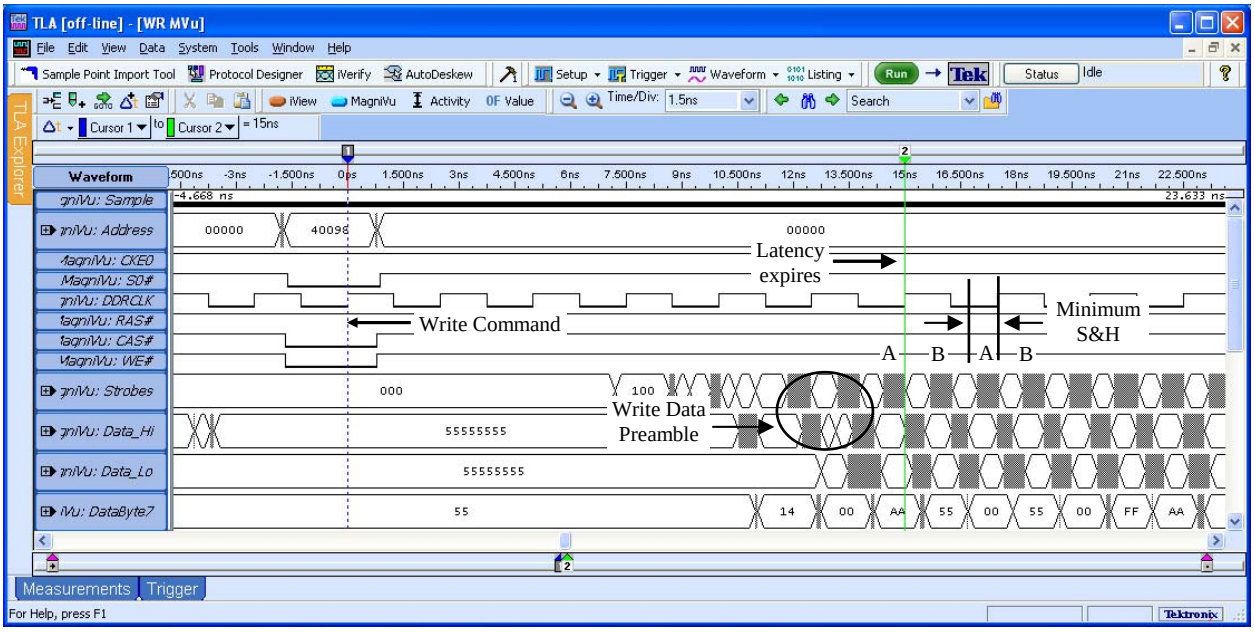


Figure 13 - Locating Minimum Valid NEX-DDR3INTR-HS Write Data Window

Zoom in further to determine the Setup and Hold sample point necessary to acquire valid data at that point (*Figure 14*) and use the cursors to measure the time from the clock edge to the start of valid Write data. In this example the data leads the clock edge by approximately 740ps, meaning that a suitable Setup & Hold value for the 'A' Data Hi capture group would be 742ps/-508ps. Note that the 'A' Data Lo group is valid somewhat later than the Data Hi group with its valid time starting at approximately 430ps prior to the clock edge, so the Setup & Hold sample point for the 'A' Data Lo capture group would be set to 430ps/-195ps.

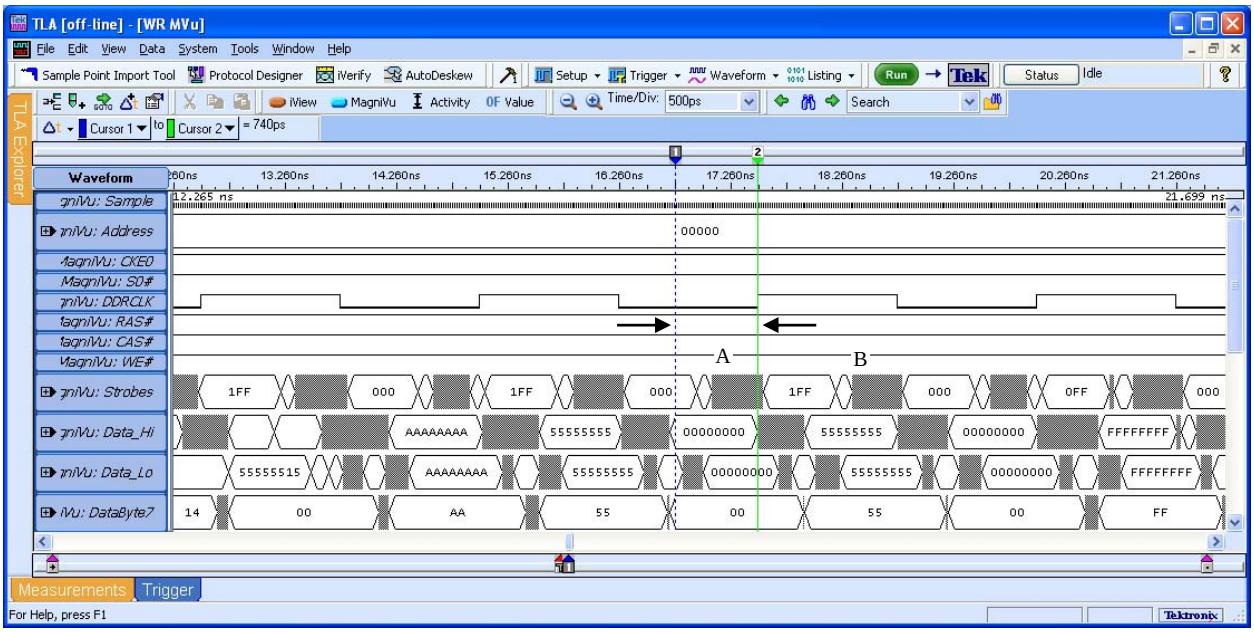


Figure 14 - Measuring NEX-DDR3INTR-HS 'A' Data Hi / Lo Write Data Setup & Hold

Now the sample point for the Write ‘B’ Data Hi and Data Lo groups must be determined (see *Figure 15*). The next valid Write data (after the cycle measured above) occurs approximately 500ps after the rising edge of DDRCK0, so a suitable Setup & Hold value for the ‘B’ Data Hi capture group would be -508ps/742ps. As with the ‘A’ data the ‘B’ Data Lo group is somewhat later than the Data Hi group. The ‘B’ Data Lo valid time starts at approximately -800ps so a suitable Setup & Hold value for the ‘B’ Data Lo capture group would be -801ps/1.035ns.

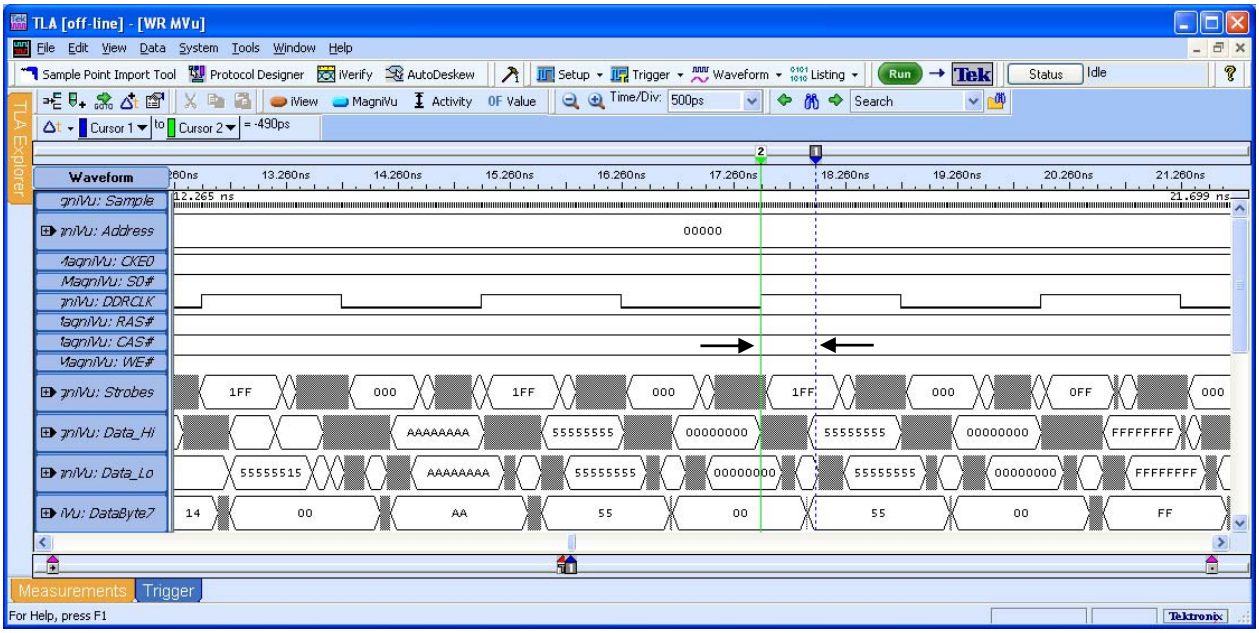


Figure 15 - Measuring NEX-DDR3INTR-HS ‘B’ Data Hi / Lo Write Data Setup & Hold

Now the sample point positions must be set for the ‘A’ Data Hi/Lo and ‘B’ Data Hi/Lo capture groups in the Setup window.

Each 32-bit data group will require its own value programmed from the measurements noted in the MagniVu window.

Note that if the Upper Strobes are being used as Data Masks then the WrtMasks group should have a Setup & Hold value that matches that of the Write Data groups.

The sample point positions must now be set for the ‘A’ capture groups in the Setup window. Note that if the Upper Strobes are being used as Data Masks then the WrtMasks group should have a Setup & Hold value that matches that of the Write Data groups.

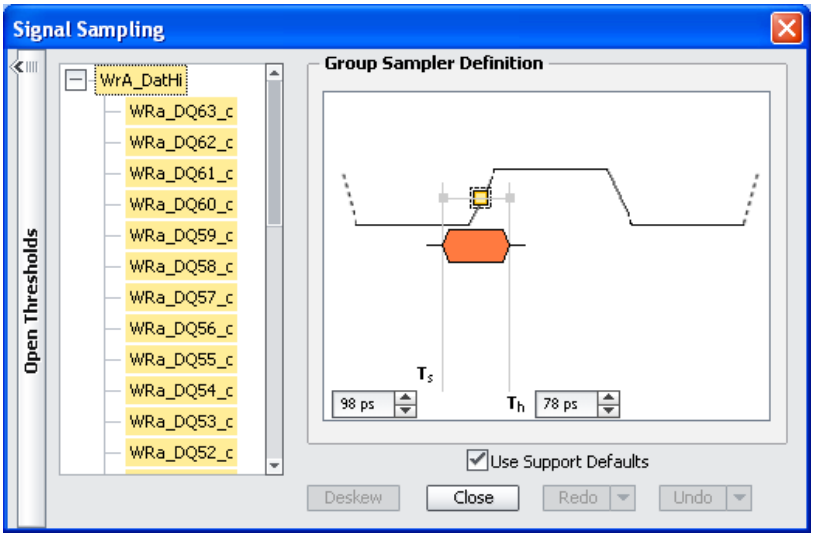


Figure 16 - NEX-DDR3INTR-HS Write Data Capture Point Window

Because of the speeds of DDR3 data it may be necessary to program Setup & Hold values for each of the 8-bit groups that are associated with a given Strobe. This could be required if there is significant skew between the DDR Strobes. *Figure 17* shows some of these additional data groups (DataByte7-0) added to the same Waveform display shown in *Figure 17*. Note that it is now possible to determine the skew between data groups and place these values into the Setup & Hold Window settings in the TLA Setup window (see *Figure 18*). Refer to Appendix F Data Group / Byte / Strobe Cross-Reference for details on which 8-bit groups make up a 32-bit group.

When setting the individual Setup & Hold values it is suggested that the settings for the associated 32-bit group be reset to “Support Package Default”. This will prevent the TLA from displaying warnings that conflicting values have been set for the data bits. The Support Package Default Setup & Hold values are the same as the TLA default values – 117ps/117ps. It will also be necessary to program the Setup & Hold values for all of the 8-bit groups in the affected 32-bit group. If conflicting Setup & Hold points are programmed then the values will have exclamation marks beside them to denote the conflict.

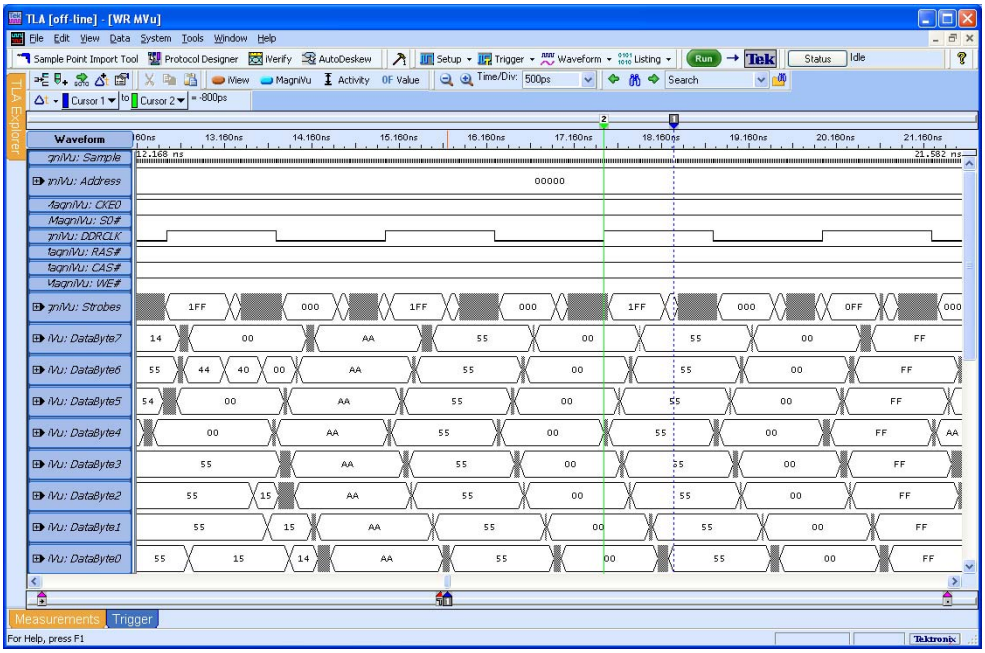


Figure 17 - Viewing Individual 8-bit Read Data Groups

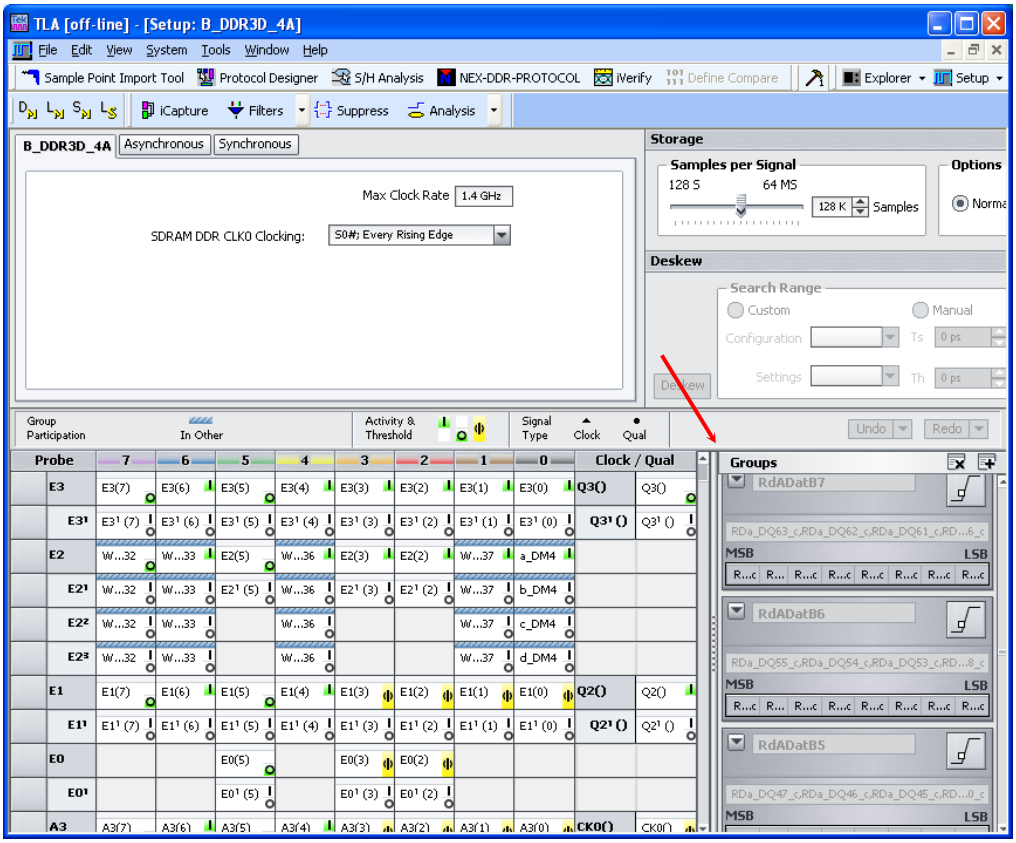


Figure 18 – TLA V5.6 or later - Setting Individual Setup & Hold Values for the 8-bit Read Data Groups

6.0 VIEWING DATA

6.1 Viewing NEX-DDR3INTR-HS Data

When using the NEX-DDR3INTR-HS support packages the raw Address and Data groups are suppressed and are replaced with post-processed data in new groups. This data is displayed in new groups that have the support package name preceding it (i.e., B_DDR3D_XX or R_DDR3D_XX, Address, B_DDR3D_2D or _4D DataHi, etc.). The raw data groups are suppressed so that the display of data can be done in a more user-friendly fashion.

The Command group is suppressed because its function is replaced with a column labeled "X_DDR3D_XX Mnemonics". The Interposer support software includes post-processing code that permits masking out all invalid Read / Write and non-Command data, providing the user a much better overview of bus activity. *Figure 19* shows the default X_DDR3D_XX display where all DDR3 data is displayed.

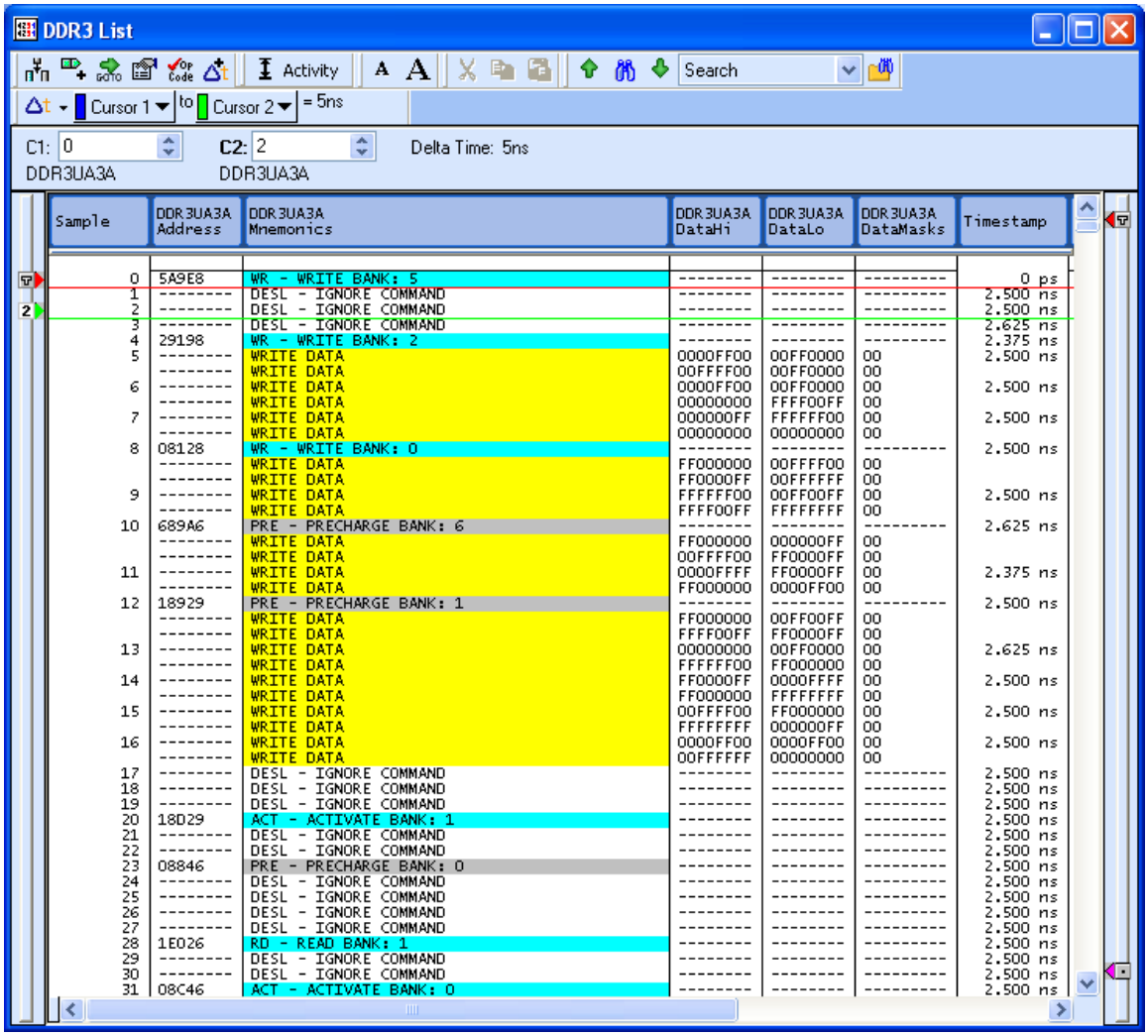


Figure 19 - NEX-DDR3INTR-HS Listing Display

To change the display it is necessary to bring up the window's Properties window (perform a right mouse-click in the State display window) and select the Disassembly tab. This will bring up the configuration window shown in *Figure 20*.

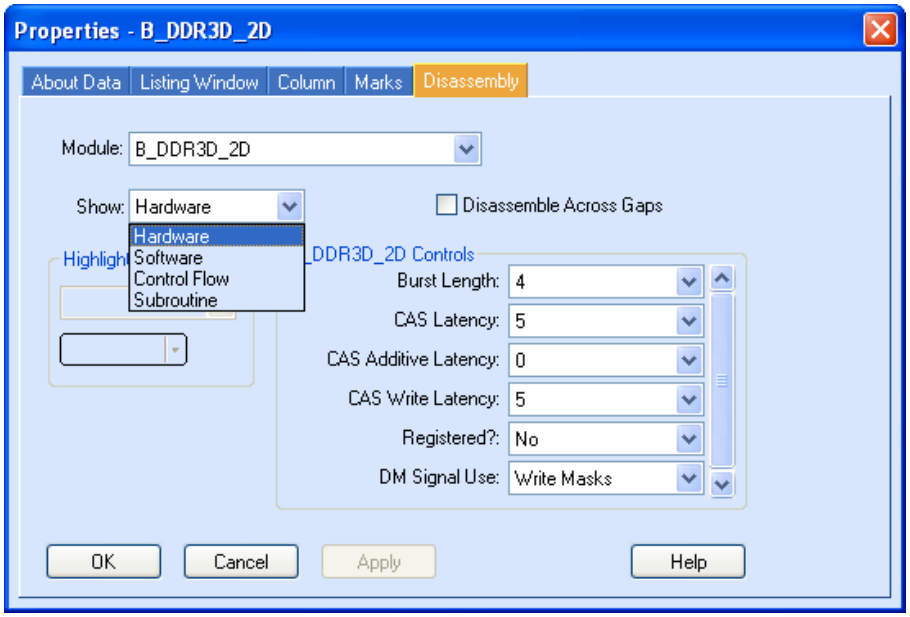


Figure 20 - Disassembly Properties

There are several select fields available in this window, some of which must be set correctly for the post-processing software to work properly. These fields and their selections are:

Burst Length - permits setting the burst length for Read and Write data. Valid choices are 4 (the default) 8, and 4/8 On-the-Fly. This value must be set properly for all valid Read and Write data to be displayed.

CAS Latency (CL) - sets the delay, in clock cycles, from the Read command until the first piece of valid Read data is available. This value must be set properly for all valid Read Data to be displayed. Valid choices are 5 (default), 6, 7, 8, 9 or 10 cycles.

CAS Additive Latency - additional latency for data cycles. This value must also be set properly for valid Read Data to be displayed. Valid choices are 0 (default), CL-1, or CL-2 cycles.

CAS Write Latency – number of clock cycles from Write command to the first Write Data. This value must be set properly for all valid Write Data to be displayed. Valid choices are 5 (default), 6, 7, or 8 cycles.

Registered? – must be set to reflect whether or not Registered DDR memory is used. Default is No. When set to Yes an additional clock cycle delay is added to CAS Latency and to valid Read and Write Data tagging.

DM Signal Use - permits setting Data Mask functionality to Write Masks (default) or Strobes. When set to Write Mask the DM signals will be used to mask Write Data to show which data bytes were valid in the cycle.

In addition to these Disassembly Properties selections, changing the settings in the **Show** field results in display changes as well:

Hardware - (default) displays all acquired cycles

Software - suppresses all idle or wait cycles

Control Flow - shows Address Command and valid Read / Write data cycles

Subroutine - shows valid Read / Write data cycles only

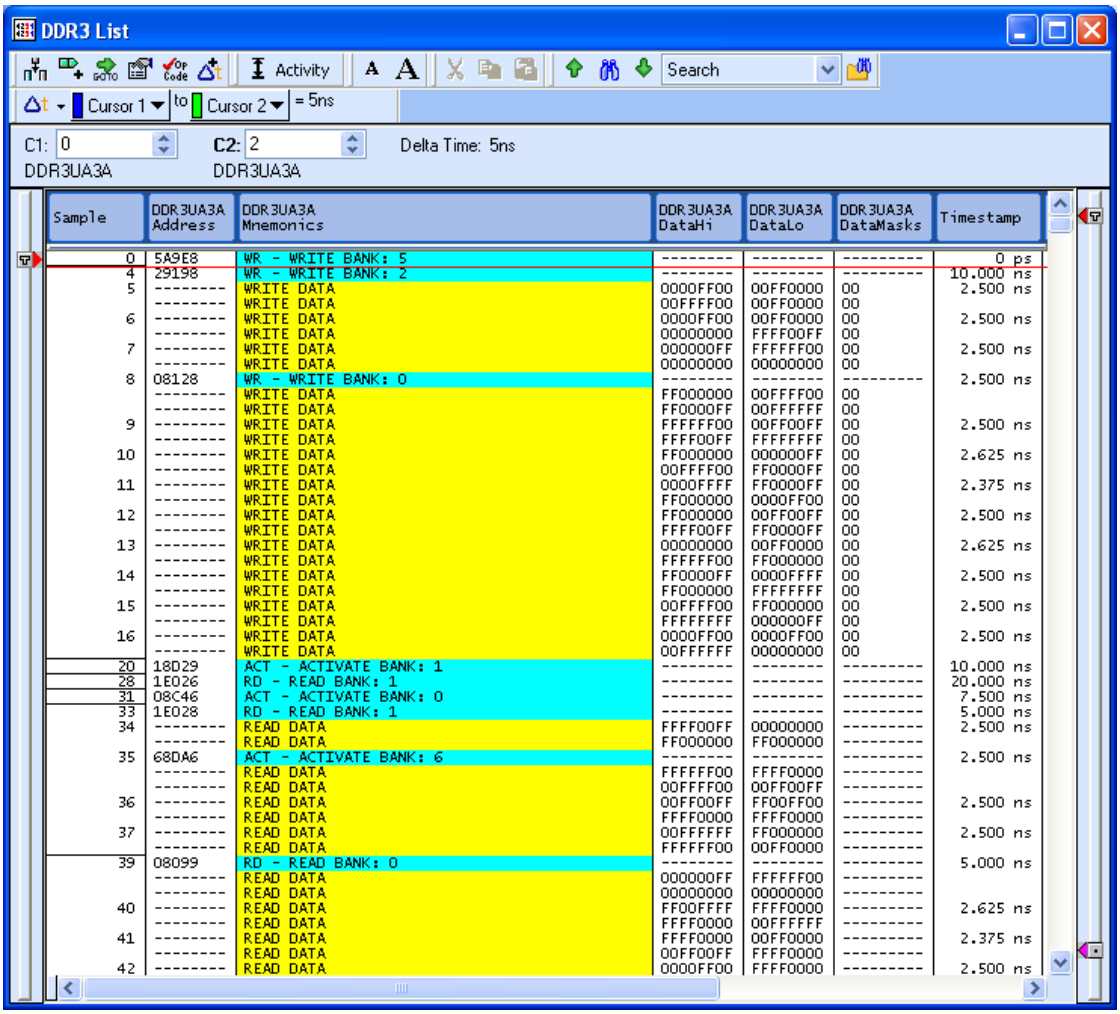


Figure 21 - NEX-DDR3INTR-HS Listing Display - Control Flow

Changing the Show field setting in the display of *Figure 19* from Hardware to Control Flow results in the display of *Figure 21* where only Row and Column Address commands and valid data are displayed. Note that the timestamp is updated to reflect the time between displayed cycles.

6.2 Viewing Raw DDR3 Data using NEX-DDR3INTR-HS XX Supports

In order to make the display of DDR3 data more user-friendly the raw data from the Address, all Data and other groups is suppressed in the software support's Listing display. Instead the post-processing display software formats and reorders the data to tag and display valid DDR3 Address, Commands and Data. Data is reordered chronologically in the display with the oldest data being shown on the line above the newer data.

To see the raw data using the Interposer support package perform a right mouse click in the Listing window, select **Add Column…** then click on the group to be added. Refer to the TLA User's Manual or online help for further information on added or deleting data groups.

6.3 NEX-DDR3INTR-HS Mnemonics Description

Table 10 gives a brief description of each of the text lines displayed in the software support's post-processing software display.

Mnemonic	Description
ACT – BANK ACTIVATE (Sx#) Bank:	Active command – activate a row in a bank for subsequent access (Chip Select 0-3; Bank x)
DESL - IGNORE COMMAND	Deselect function – no new command
(E)MRS – (EXTENDED) MODE REGISTER SET x (Sx#)	Mode Register Set command, registers 0-3; (Chip Select 0-3)
NOP - NO OPERATION (Sx#)	No Operation command (Chip Select 0-3)
PRE – SINGLE BANK PRECHARGE (Sx#) Bank:	Precharge command (Chip Select 0-3; Bank x)
PREA – PRECHARGE ALL BANK (Sx#)	Precharge All command (Chip Select 0-3)
RDA – READ W/AUTO PRECHARGE (Sx#) Bank:	Read command with auto precharge (Chip Select 0-3; Bank x)
RD - READ (Sx#) Bank:	Read command – initiates a burst read access to active row (Chip Select 0-3; Bank x)
READ DATA	Valid Read data on the bus
REF - REFRESH (Sx#)	Self Refresh command (Chip Select 0-3)
WRA – WRITE W/AUTO PRECHARGE (Sx#) Bank:	Write command with auto precharge (Chip Select 0-3; Bank x)
WR - WRITE (Sx~) Bank:	Write command – initiates a burst write access to active row (Chip Select 0-3; Bank x)
WRITE DATA	Valid Write data on the bus
ZQCL – ZQ CALIBRATION LONG (Sx#)	ZQ Calibration Long (Chip Select 0-3)
ZQCS – ZQ CALIBRATION SHORT (Sx#)	ZQ Calibration Short (Chip Select 0-3)

Table 10 - NEX-DDR3INTR-HS Mnemonics Definition

6.4 Viewing Timing Data on the TLA

By default, the TLA will display an acquisition in the Listing (State) mode. However, the same data can be displayed in Timing form by adding a Waveform Display window. This is done by clicking on the **Window** pull-down, selecting **New Data Window**, clicking on **Waveform Window Type**, then choosing the Data Source. Two valid choices are presented: X_DDR3D_XX and X_DDR3D_XX: MagniVu. The first will show the exact same data (same acquisition mode) as that shown in the Listing window, except in Waveform format. The second selection will show all of the channels in 20GHz MagniVu mode, so that edge relationships can be examined around the MagniVu trigger point. MagniVu is very useful and in some cases necessary to see/resolve DDR3 data. With either selection, all channels can be viewed by scrolling down the window. Refer to the TLA System User's Manual for additional information on formatting the Waveform display.

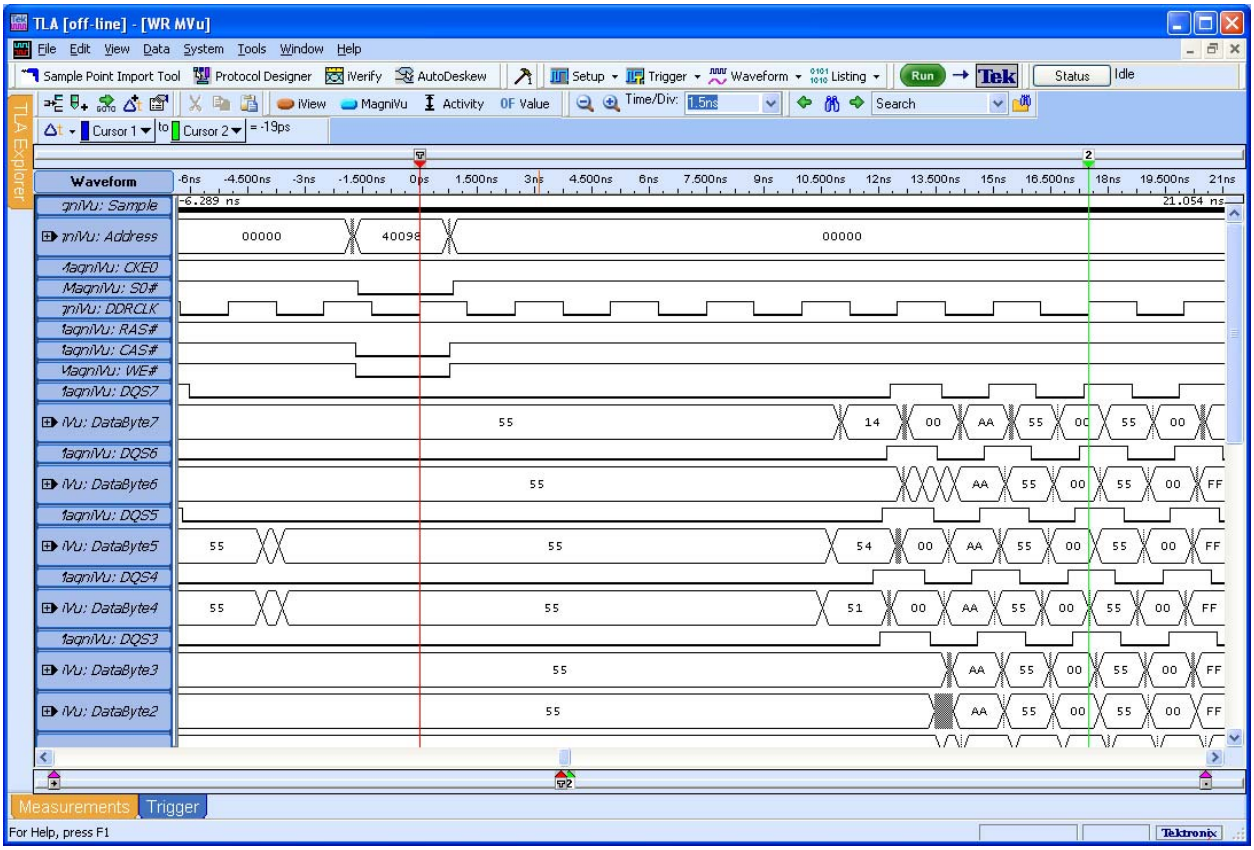


Figure 22 - NEX-DDR3INTR-HS MagniVu Display on TLA

7.0 HINTS & TIPS

7.1 Symbolic Triggering on a Command using NEX-DDR3INTR-HS Supports

A Symbol Table has been included for the Control data groups defined in each of the support packages. The Symbol Table for the X_DDR3D_XX supports is shown in *Table 11*. The use of Symbol Tables when triggering makes it easier for the user to define a given cycle to be triggered on. Rather than trying to remember what signals make up the Control group, the Symbol Table has the appropriate bits already set for the given cycle.

It is important to note that changing the channel definition of the Control group can result in incorrect symbol information being displayed.

Symbol	Definition
cc ssss = x1 1110 for S0#	
cc ssss = 1x 1101 for S1#	
cc ssss = x1 1011 for S2#	
cc ssss = 1x 0111 for S3#	
x in Definition = Don't Care	
MRS – Sx# MODE REGISTER SET	cc ssss xxx xxx xx000
REF – Sx# REFRESH	cc ssss xxx xxx xx001
PRE – Sx# SINGLE BANK PRECHARGE	cc ssss xxx xxx x0010
PREA – Sx# PRECHARGE ALL BANKS	cc ssss xxx xxx x1010
ACT – Sx# ACTIVATE BANK	cc ssss xxx xxx xx011
WR – Sx# WRITE	cc ssss xxx xxx x0100
WRA – Sx# WRITE WITH AUTO PRECHARGE	cc ssss xxx xxx x1100
RD – Sx# READ	cc ssss xxx xxx x0101
RDA – Sx# READ WITH AUTO PRECHARGE	cc ssss xxx xxx x1101
NOP –Sx# NO OPERATION	cc ssss xxx xxx xx111
DES - DEVICE DESELECT	cc ssss xxx xxx xxxxx
ZQCL – Sx# ZQ CALIBRATION LONG	cc ssss xxx xxx x1110
ZQCS – Sx# ZQ CALIBRATION SHORT	cc ssss xxx xxx x0110

Table 11 - NEX-DDR3INTR-HS Control Symbol Table

Signals, left-to-right: CKE1, CKE0, S3#, S2#, S1#, S0#, BA2, BA1, BA0, A15, A14, A13, A12/BC#, A10/AP, RAS#, CAS#, WE#

7.2 B_DDR3D_2D / R_DDR3D_1A - Capturing MRS (Mode Register Set) Cycles

If the characteristics of the DDR target (latency, burst length) are not known it is possible to acquire this information using the TLA so that the post-processing Control settings can be properly set. This information is programmed into the DDR memory upon system boot by use of the MRS (Mode Register Set) command, and is required when using the NEX-DDR3INTR-HS supports for the post-processing software to properly decode the acquisitions. The TLA trigger shown in *Figure 23* can be used to acquire the MRS cycles when using either of these supports.

Note that because there is no Trigger event defined in this example that it will be necessary to Stop the TLA acquisition manually to display the MRS data. A trigger could certainly be added in either (or both) of the Trigger events, but the method shown ensures that the last valid MRS cycles will be acquired regardless of the memory depth setting of the acquisition card.

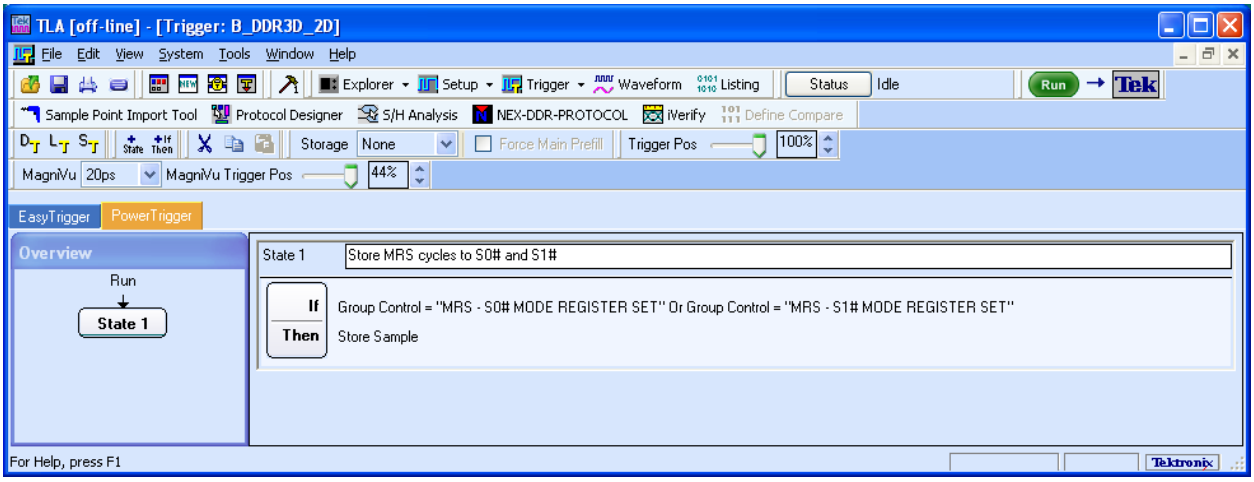


Figure 23 - B_DDR3D_2D MRS Trigger

In the trigger example a Storage condition has been created so that only MRS cycles will be stored. In testing, multiple MRS cycles were seen during the boot process, and the example triggers shown will ensure that all of the MRS cycles will be acquired, an example of which is shown in *Figure 24*. The last acquired MRS cycle will reflect the settings used in the DDR target – in this case, a CAS latency of 2 cycles with a Burst length of 8.

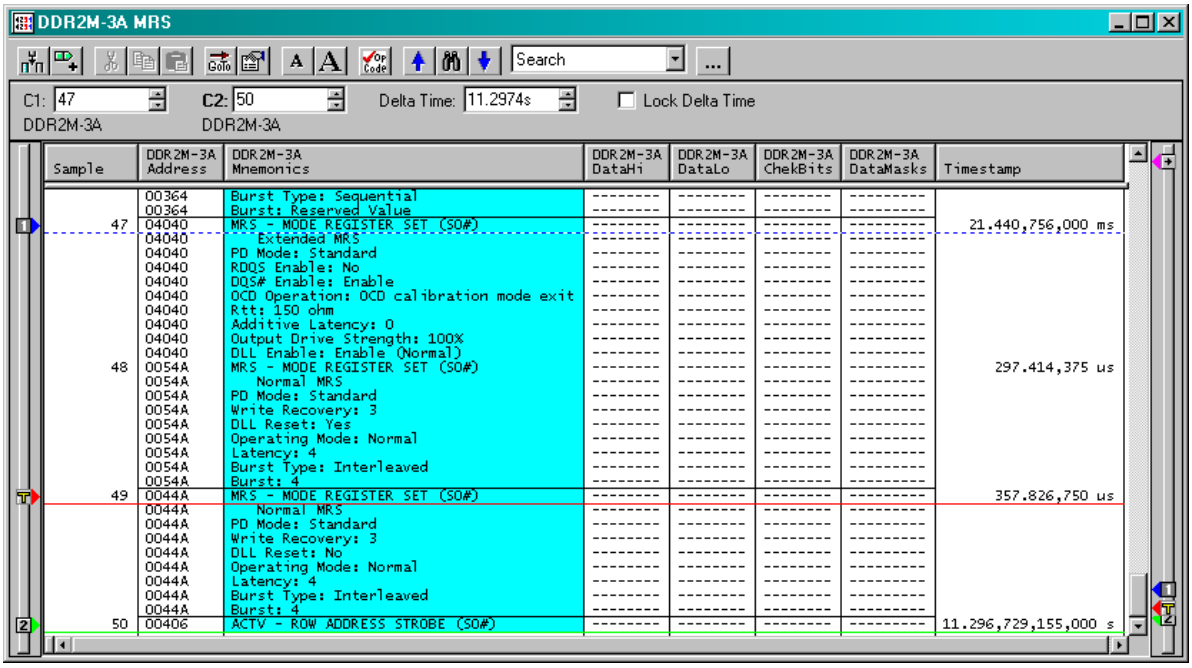


Figure 24 - MRS Cycle Acquisition Disassembly

7.3 B_DDR3D_4A / R_DDR3D_2A Power Triggers

Because of the way data is captured and stored when using the B_DDR3D_4A and R_)DDR3D_2A supports (see Appendix A) triggering on a Command or other DDR3 event has become more complicated. Since two clock cycles of data are stored in the 7BB4 card two tests must be made to determine whether or not an event occurred. The storage / trigger groups that have an _0 suffix to their names are groups whose data is associated with the first clock cycle that is acquired; groups with an _1 suffix are associated with the second clock cycle that is acquired.

IMPORTANT NOTE The Power Triggers should be loaded into the TLA ***ONLY*** through the Load Trigger function in the Trigger window. If they are loaded as Module Setups any user entered settings such as sample points and threshold values will be lost.

Several Power Triggers have been created and included with the B_DDR3D_4A and R_DDR3D_2A supports. They can be found in the C:\My Document\B_DDR3D_4A_Triggers or C:\My Document\R_DDR3D_2A_Triggers folder and can be loaded into the module using the Load Trigger icon or menu pull down. The Triggers have names that try to indicate what they were designed to do, and there are also short descriptions shown for each trigger when it is clicked on from within the Load Trigger menu. The triggers and brief descriptions of each follows:

B_DDR3D_4A / R_DDR3D_2A Even Read Addr Data BL4 Trigger – Designed to trigger on specific Read data from a specific S0# Read address for even latencies with a Burst Length of 4.

B_DDR3D_4A / R_DDR3D_2A Even Read Addr Data BL8 Trigger – Designed to trigger on specific Read data from a specific S0# Read address for even latencies with a Burst Length of 8.

B_DDR3D_4A / R_DDR3D_2A Even Write Addr Data BL4 Trigger – Designed to trigger on specific Write data written to a specific S0# Write address for even latencies with a Burst Length of 4.

B_DDR3D_4A / R_DDR3D_2A Even Write Addr Data BL8 Trigger – Designed to trigger on specific Write data written to a specific S0# Write address for even latencies with a Burst Length of 8.

B_DDR3D_4A / R_DDR3D_2A MRS Cycle Store Trigger – Designed to acquire and store all S0# and S1# MRS cycles. Does not trigger the TLA – it must be stopped manually.

B_DDR3D_4A / R_DDR3D_2A Odd Read Addr Data BL4 Trigger – Designed to trigger on specific Read data from a specific S0# Read address for odd latencies with a Burst Length of 4.

B_DDR3D_4A / R_DDR3D_2A Odd Read Addr Data BL8 Trigger – Designed to trigger on specific Read data from a specific S0# Read address for odd latencies with a Burst Length of 8.

B_DDR3D_4A / R_DDR3D_2A Odd Write Addr Data BL4 Trigger – Designed to trigger on specific Write data written to a specific S0# Write address for odd latencies with a Burst Length of 4.

B_DDR3D_4A / R_DDR3D_2A Odd Write Addr Data BL8 Trigger – Designed to trigger on specific Write data written to a specific S0# Write address for odd latencies with a Burst Length of 8.

B_DDR3D_4A / R_DDR3D_2A Read Command Trigger – Designed to trigger on any S0# or S1# Read Command.

B_DDR3D_4A / R_DDR3D_2A Write Command Trigger – Designed to trigger on any S0# or S1# Write Command.

So to trigger on a Read command to S0# or S1# the trigger program would be as shown in *Figure 25*:

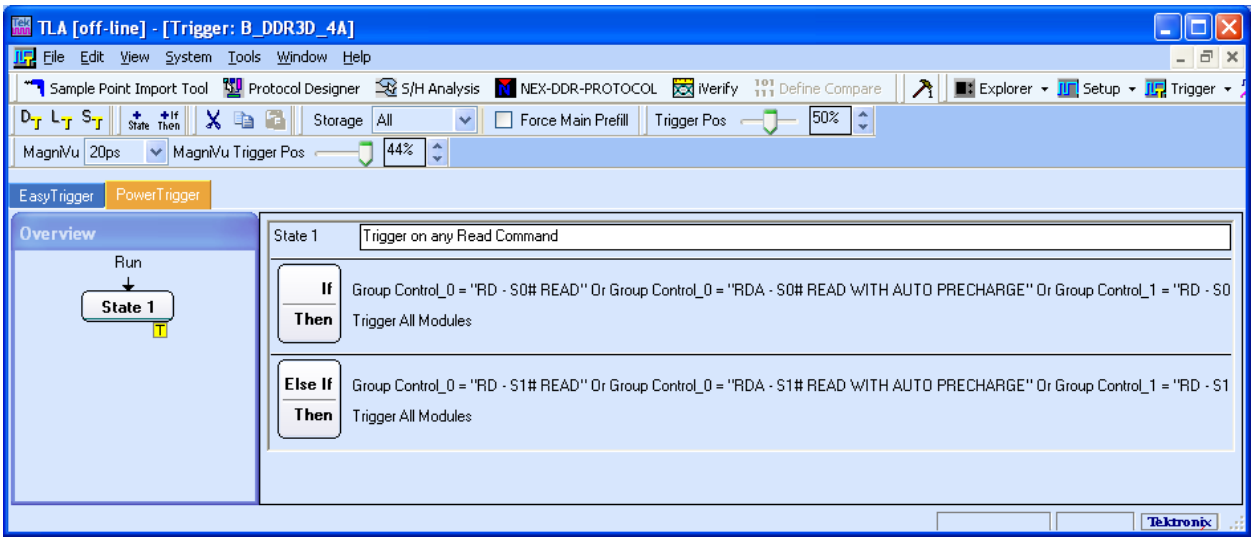


Figure 25 - B_DDR3D_4A / R_DDR3D_2A Read Command Trigger

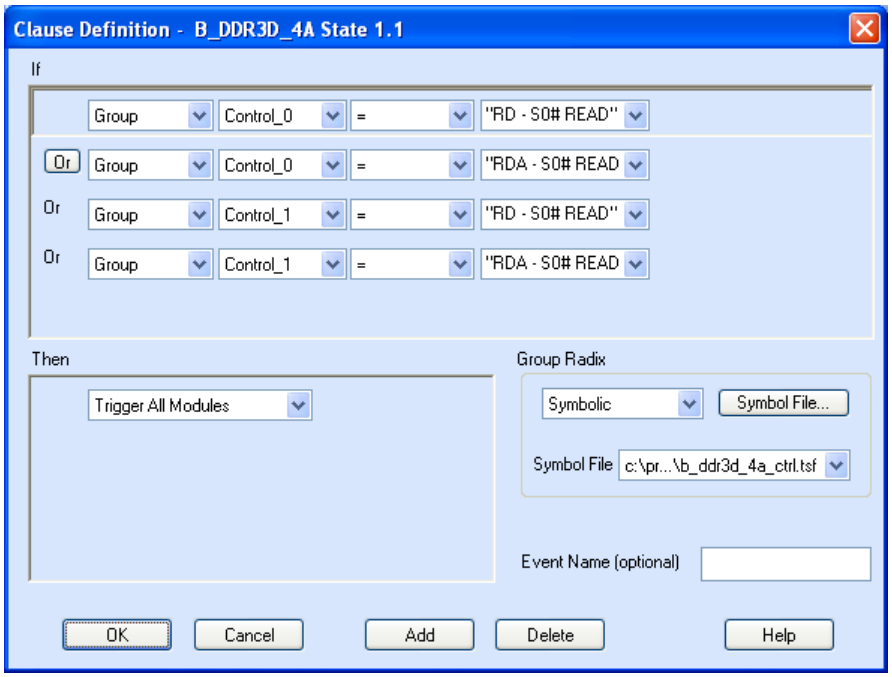


Figure 26 - B_DDR3D_4A / R_DDR3D_2A Read Command Trigger Detail

To trigger on a Read command to a given address followed by specific Read data the trigger in *Figure* 27 could be used when dealing with odd latency values.

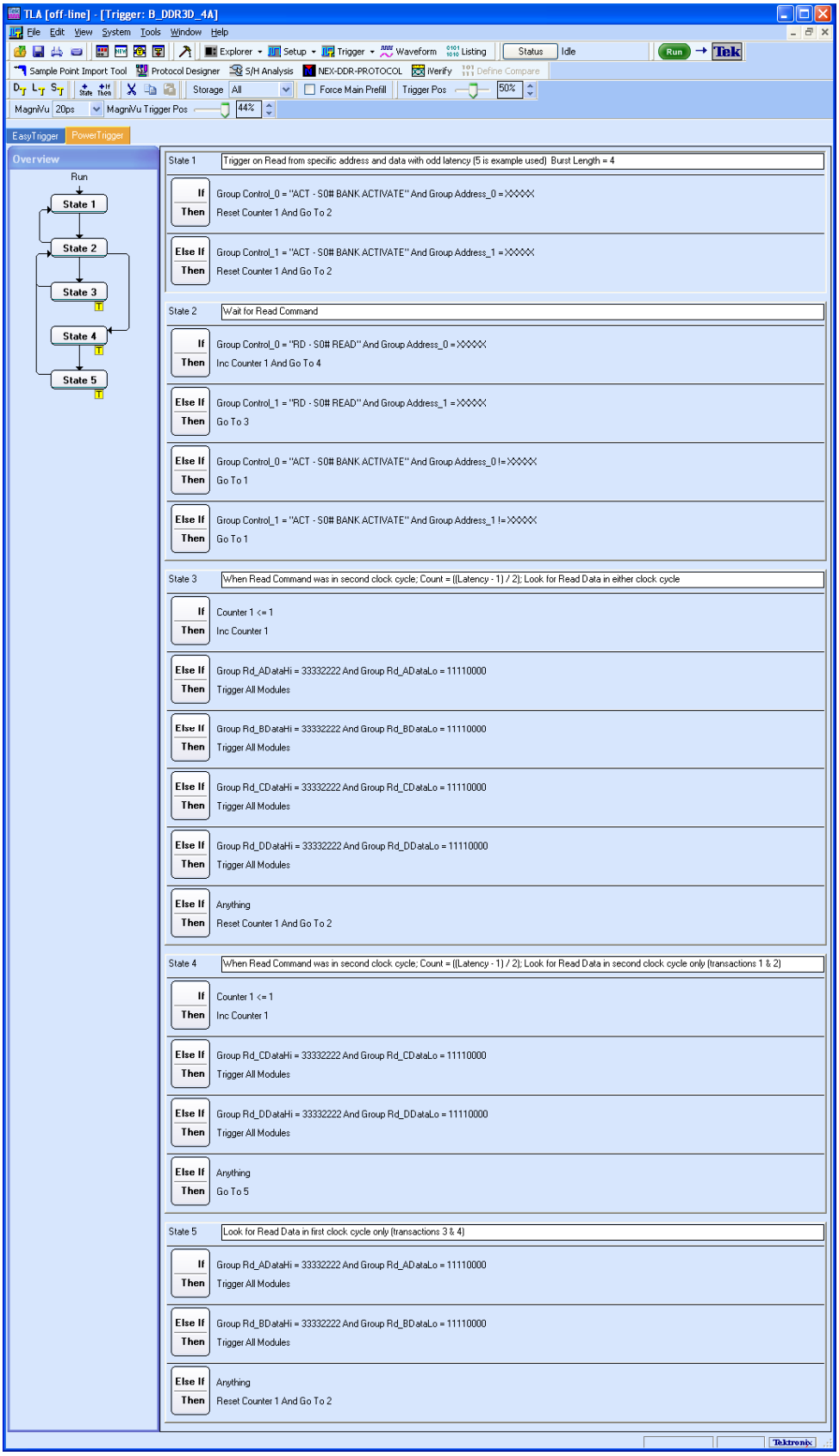


Figure 27 - B_DDR3D_4A / R_DDR3D_2A Read Address and Data Trigger (BL=4; Odd Latencies)

To trigger on Read Address followed by Read Data the trigger in *Figure 28* would be used for even latency values.

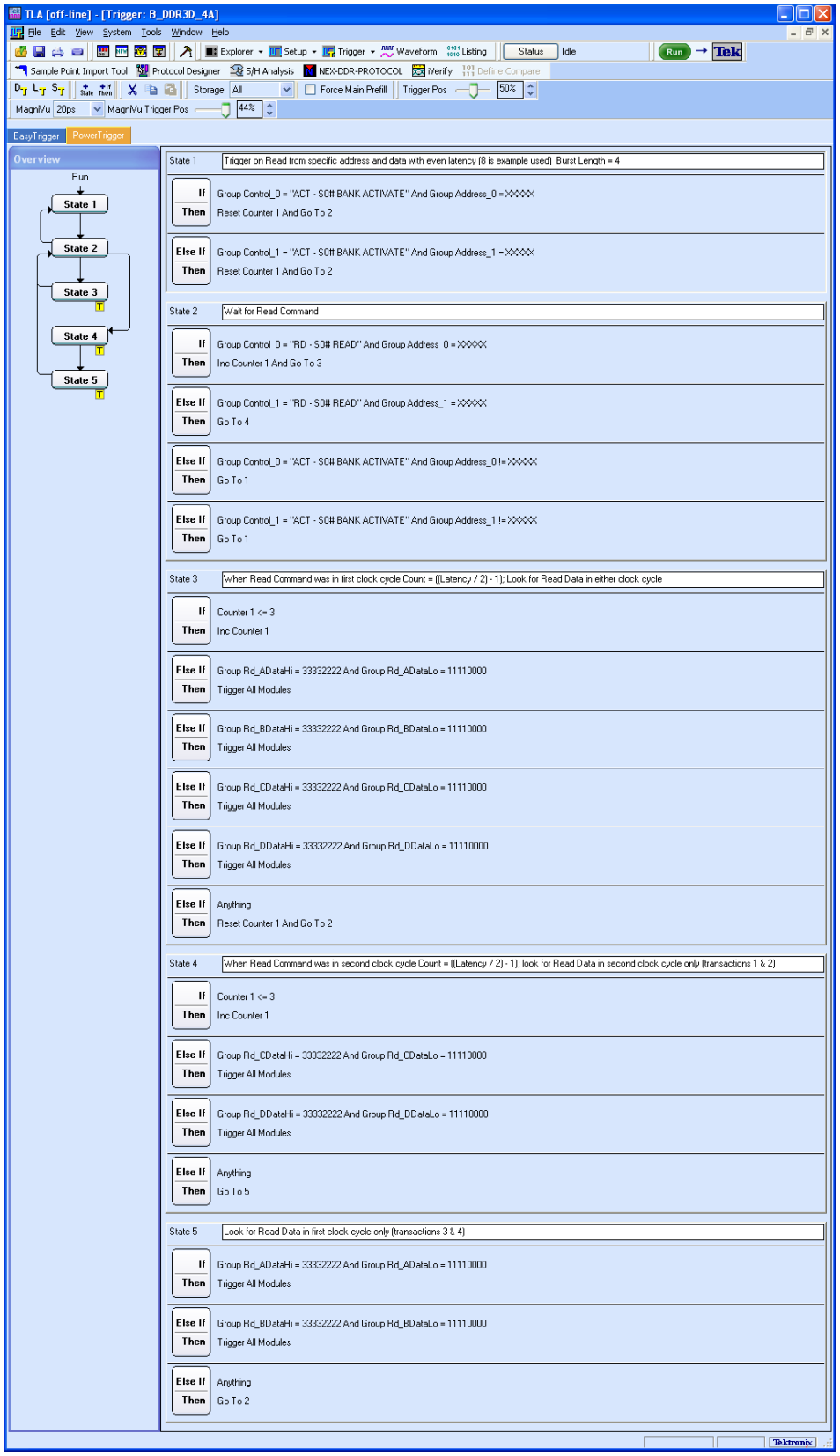


Figure 28 - B_DDR3D_4A / R_DDR3D_2A Read Address and Data Trigger (BL=4; Even Latencies)

7.4 B_DDR3D_4A / R_DDR3D_2A - Capturing MRS (Mode Register Set) Cycles

If the characteristics of the DDR target (latency, burst length) are not known it is possible to acquire this information using the TLA so that the acquisition and post-processing settings can be properly set. This information is programmed into the DDR memory upon system boot by use of the MRS (Mode Register Set) commands, and is required when using the B_DDR3D_4A or R_DDR3D_2A supports for the post-processing software to properly decode the acquisitions. The TLA trigger shown in *Figure 29* can be used to acquire the MRS cycles when using this support.

Note that because there is no Trigger event defined in this example that it will be necessary to Stop the TLA acquisition manually to display the MRS data. A trigger could certainly be added in either (or both) of the Trigger events, but the method shown ensures that the last valid MRS cycles will be acquired regardless of the memory depth setting of the acquisition card.

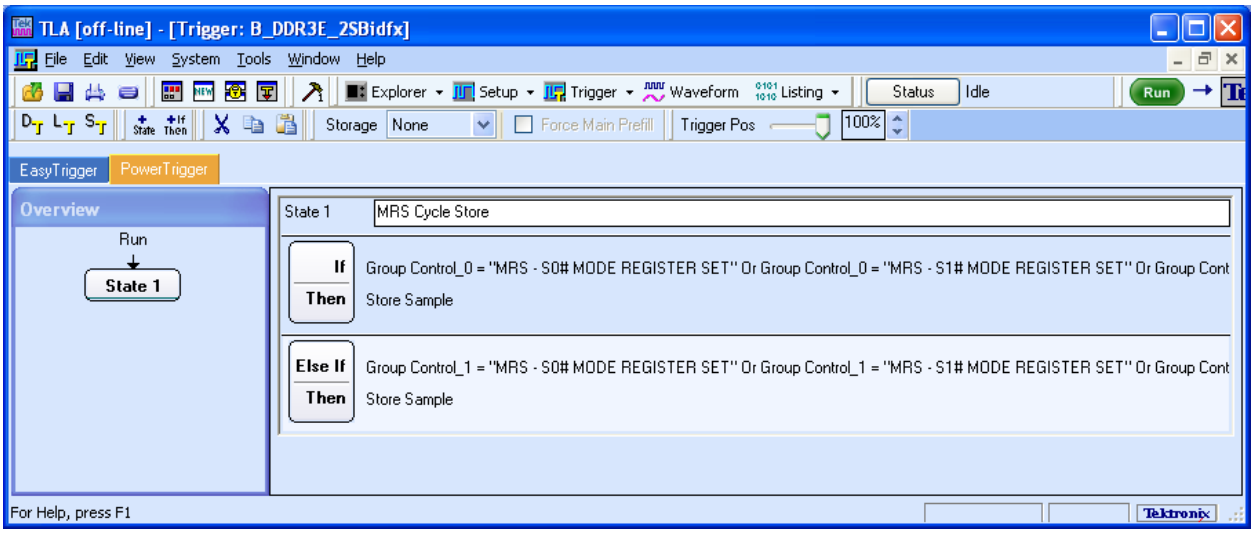


Figure 29 - B_DDR3D_4A / R_DDR3D_2A MRS Trigger

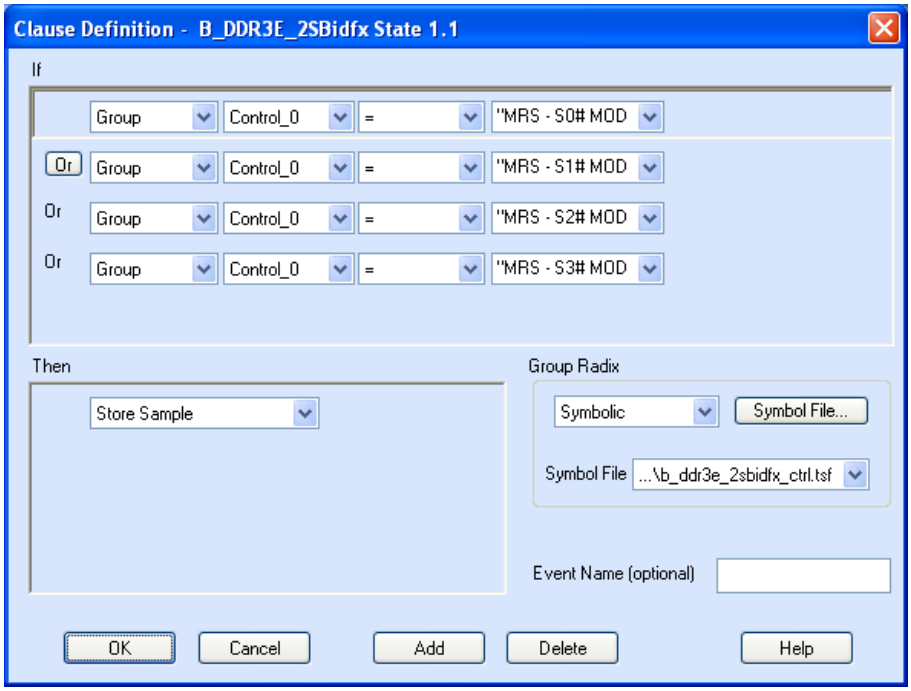


Figure 30 - B_DDR3D_4A / R_DDR3D_2A MRS Trigger Detail

In the trigger example a Storage condition has been created so that MRS cycles for any Chip Select (0, 1, 2 or 3) will be stored. In testing, multiple MRS cycles were seen during the boot process, and the example triggers shown will ensure that all of the MRS cycles will be acquired, an example of which is shown in *Figure 31*. The last acquired MRS cycle will reflect the settings used in the DDR3 target – in this case, a CAS latency of 4 cycles with a Burst length of 4.

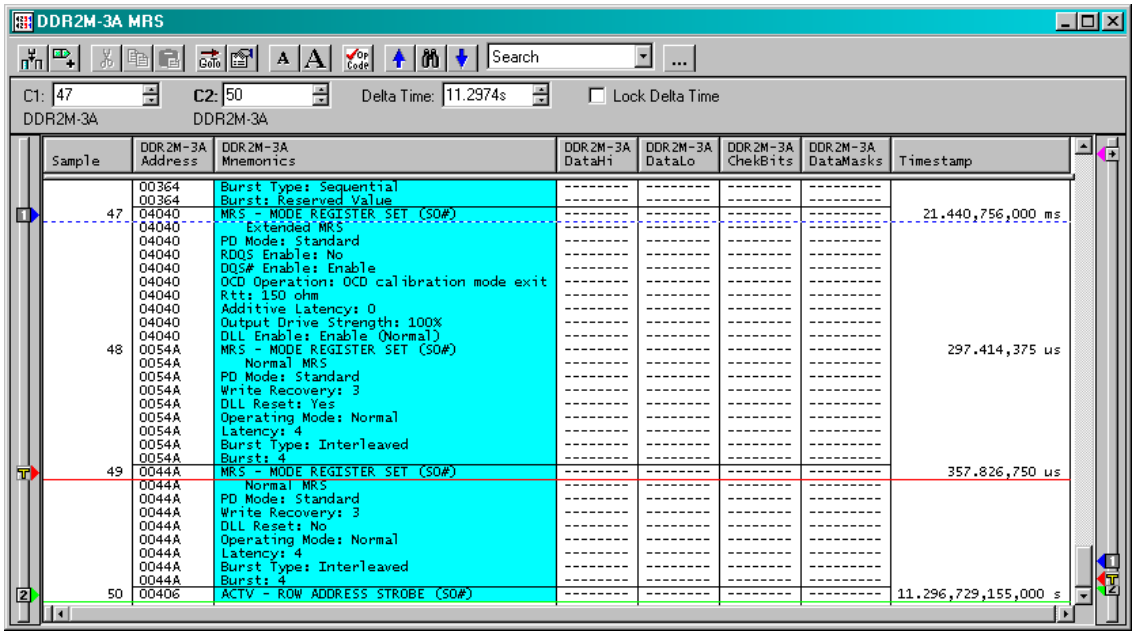


Figure 31 - MRS Cycle Acquisition Disassembly
Shown for reference only

7.5 Address Errors When Decoding MRS Cycles

It may happen when decoding MRS cycles that an error message such as “MRS0 decode error – bit A15” or similar error may be displayed. This happens when the offending Address bit is not in the state specified by JEDEC for MRS cycles. Usually this error happens when A15 or another Address bit is acquired as being high during the MRS cycle rather than being low as the specification requires. If this should happen the easiest temporary fix is to flip the polarity bit of the “bad” address bit in the Setup window so that the decode can proceed. Don’t forget to flip the polarity bit back to normal before continuing with the debug.

7.6 MRS Decode Errors for Ranks other than 0

Some multi-rank DDR3 DIMMs have some Address bits to their odd numbered ranks of memory chips swizzled. In other words, A3 from the target may be taken to A5 on the components, etc. Because of this the MRS decode for the odd ranks on such DIMMs will be incorrect. But since all ranks of a DIMM will have the same Latencies, Burst Lengths, etc. all of the necessary information for proper display decode can be gleaned from the S0# MRS cycles.

7.7 Thresholds

Analog waveforms and their associated thresholds viewed using the Tektronix Analog Mux will display amplitudes and thresholds that are not an exact representation of the actual analog waveform. The Nexus passive probes used on DDR3 NEXVu and Interposer products are designed to supply maximum voltage swing to the Logic analyzer to insure correct digital signal swing capture at the high DDR3 rates. While the Tektronix active P69xx and P68xx series of probe, being general purpose probes, divide the input voltage swing by 20 the passive probes from Nexus divide the signals by approximately 7.5. Since the divide value is different than the standard Tektronix probe the voltage swing and offset will be higher than expected, and the thresholds will be different. Instead of the expected 0.75 threshold of approximately 1.9V threshold will be required. This was designed specifically for DDR3 signals to allow the best possible capture of the digital representation of these signals. Viewing the output of the Logic Analyzer analog mux should be used as a tool to provide fine adjustment of the logic analyzer signal Vref. The threshold value determined in this manner should be used as the threshold setting for the Nexus DDR3 product. Please note: Only the vertical resolution is affected by the Nexus passive probes.

APPENDIX A – How DDR Data is Clocked

A.1 Background

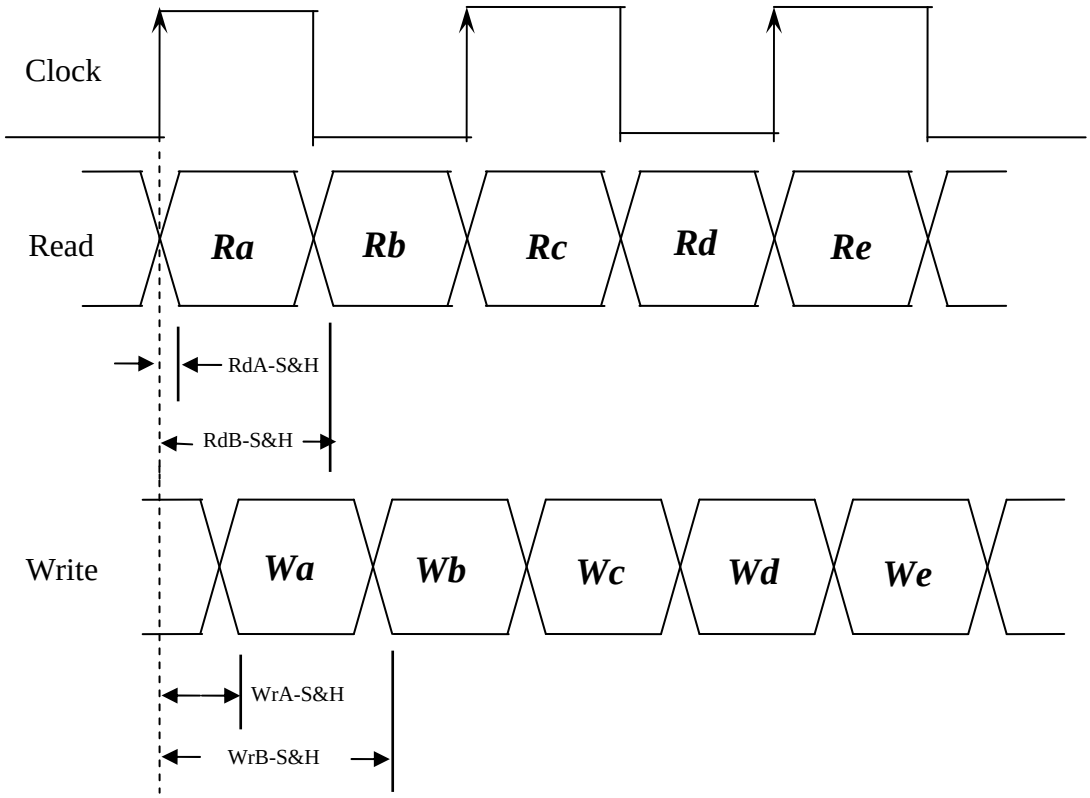
Demultiplexing means that the TLA's Logic Analyzer card can have one data probe connected to the target yet store incoming data in two or four separate data sections of the card. For instance, the A3 data section (8-bits) can be connected to the target and data can be stored in the A3 section ***and*** the D3 section. Using the equivalent of 4X demux (by utilizing both the cross-point switch and prime memory capabilities of the acquisition card), connections made to the A3 channels permit data to be stored in the A3, A3B (prime channels), D3 and D3B sections. A very useful side benefit of using demux is that, since only one set of TLA data channels has to be connected, only one probe load is added to the target, even though data is stored in two or four different locations of the acquisition card.

A.2 DDR Acquisition - General

All of the above is background necessary to understand how the TLA is able to acquire data at rates that initially look too fast. The speeds of DDR3 (1066 MT/s) require different setups to enable proper data acquisition. In addition, instead of trying to use the 8 Data Strobes to acquire data our solution uses CLK0 of the DDR SDRAM Clocks and all data acquisition is adjusted in relation to the clock edges. The 8 Data Strobes cannot be easily used to acquire data as some TLA configurations only support 4 Clock Inputs. Also, the Strobes cannot be used to acquire Address and Command information.

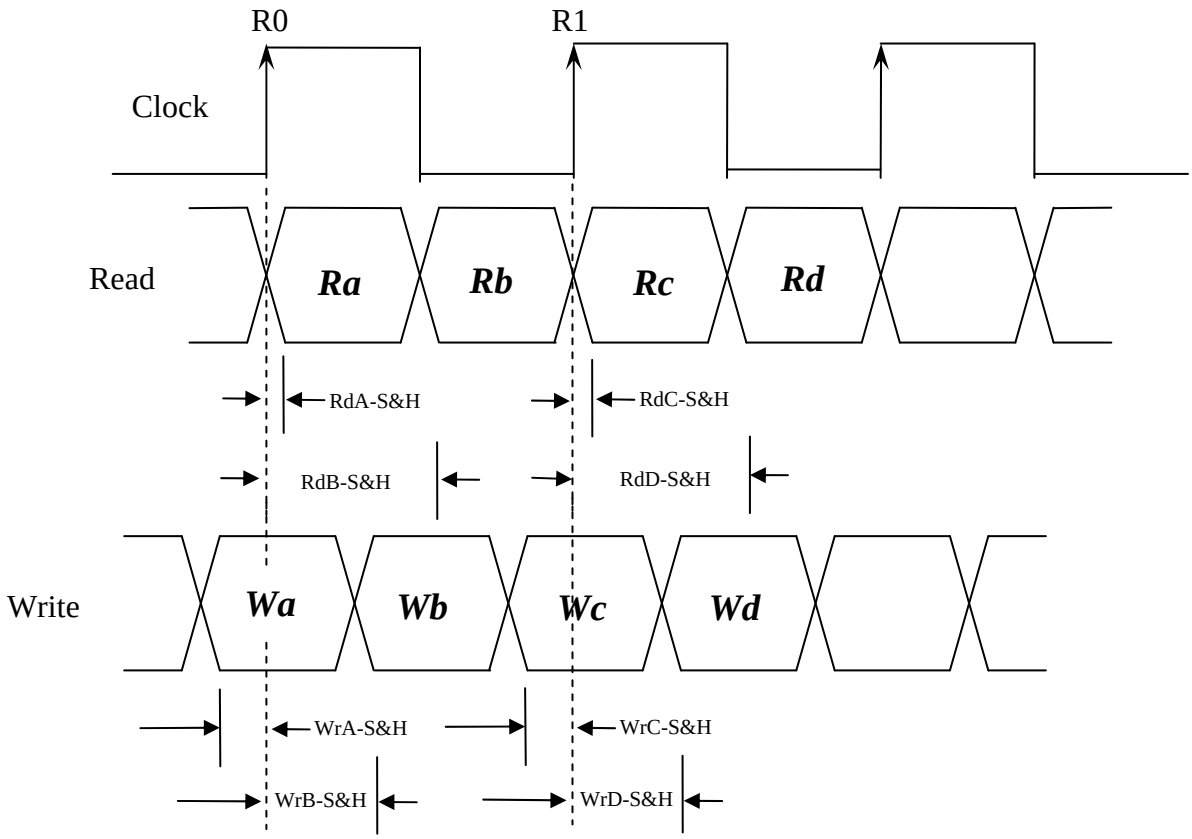
A.3 B_DDR3D_2D / R_DDR3D_1A Acquisition

The B_DDR3D_2A support requires two (2) merged TLA7Bx4 136-channel, 750MHz or 1.4GHz TLA7BB4 acquisition cards used in a TLA7XX logic analyzer and the R_DDR3D_1A support requires a single TLA7Bx4 136-channel 750MHz/1.4GHz acquisition card. Data is acquired using the rising edge of the DDR clock. A_Data information is earlier (older) data than the information stored in B_Data. Different Sample Points must be set for each of the four 32-bit Data groups, and, if necessary, sample points can be set for any of the 8-bit data groups or for individual data bits.



A.4 B_DDR3D_4A / R_DDR3D_2A Acquisition

The B_DDR3D_4A support requires four (4) merged TLA7Bx4 136-channel 1.4GHz TLA7BB4 acquisition cards used in a TLA7XX logic analyzer chassis and the R_DDR3D_2A supports requires two (2) merged TLA7Bx4 136-channel 1.4GHz TLA7BB4 acquisition cards. Data is captured using the rising edge of the DDR clock with data being stored every two DDR clocks. Internal capabilities of the 7BB4 acquisition card are used to capture 4 samples of Read data (two per DDR clock) and 4 samples of Write data (again, two per DDR clock) and then store that information in acquisition card memory.



The ‘A’ and ‘C’ sample points will be the same, as will the ‘B’ and ‘D’ sample points.

APPENDIX B – Setting Sample / Capture Points in TLA V5.6.xxx

Beginning with V5.6 of the TLA Application drastic changes were made in the User Interface. One of the more important ones when it comes to Nexus DDR Memory Supports is where and how the sample points for the Read and/or Write data groups are set.

For TLA Application versions V5.6 and later the sample points are set in the Setup window within the support package tab (see *Figure* 32 using the Nexus B_DDR3D_2D DDR3 DIMM Interposer support as an example).

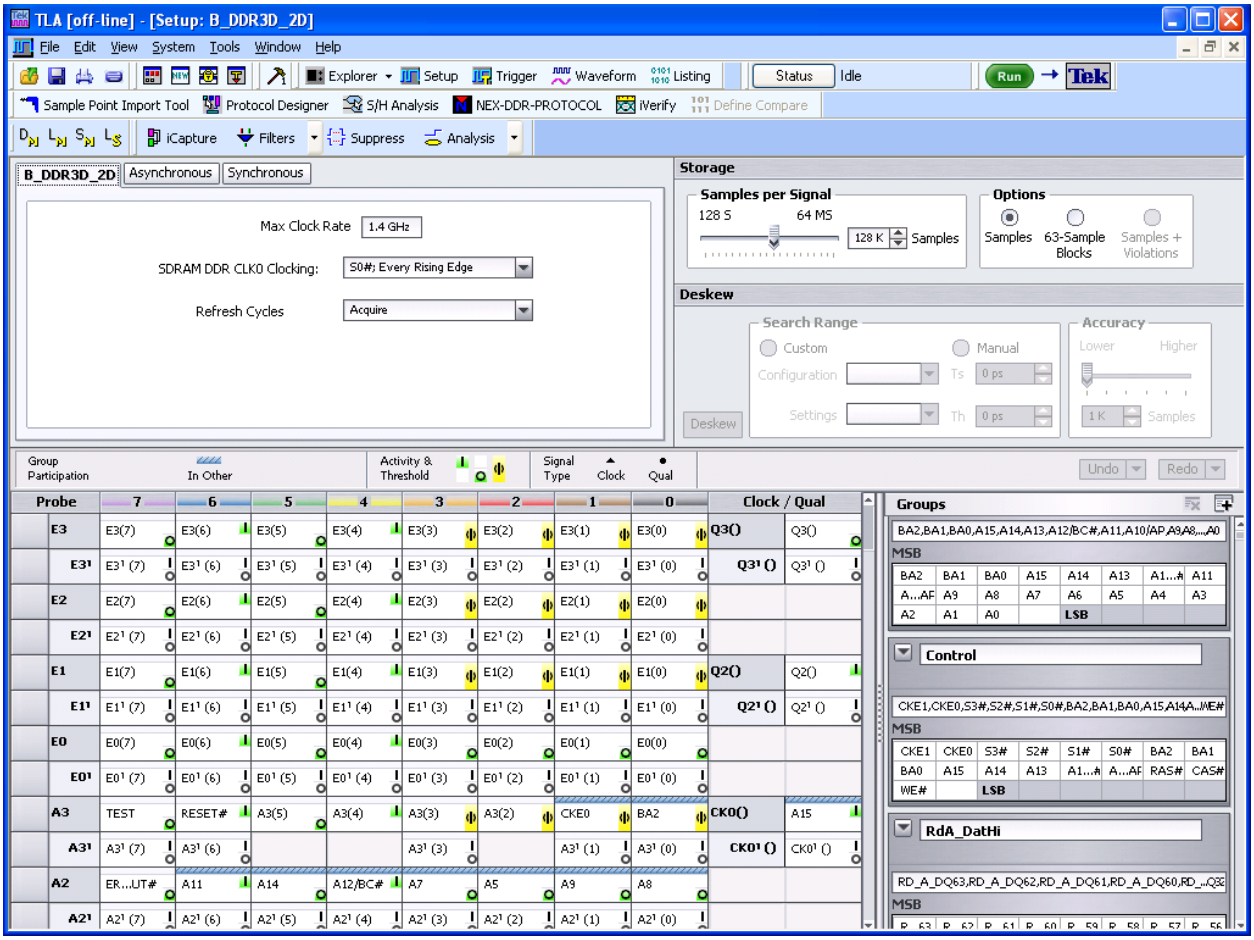


Figure 32 - B_DDR3D_2D Setup Window (TLA V5.6 or later)

In the lower right portion of the window is a scroll field. Scroll down until grayed-out groups are visible, then select the group in which the sample points are to be selected see *Figure 33*. Clicking on the Rising / Falling Edge icon (red arrow) will bring up the window shown in *Figure 34*.

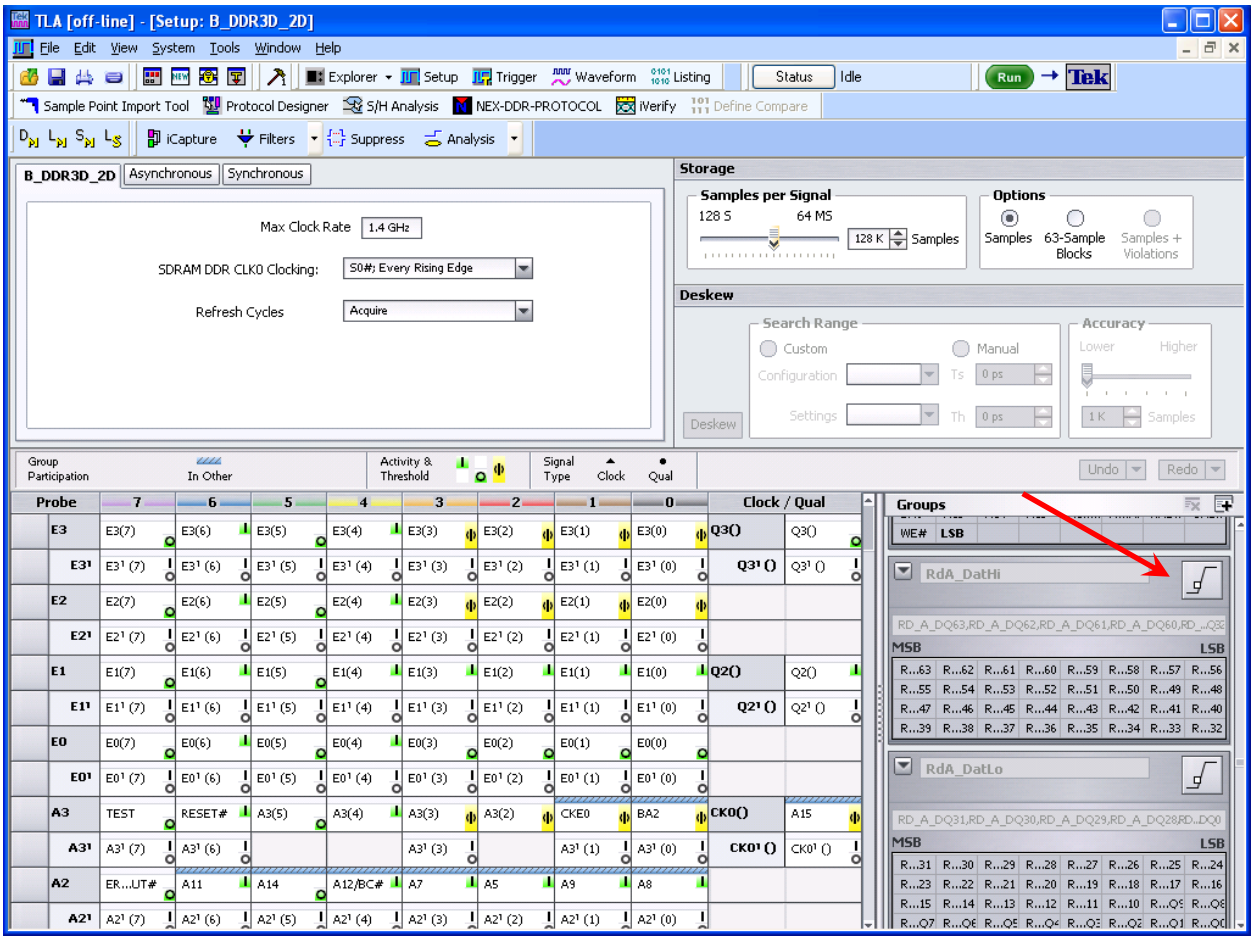


Figure 33 - B_DDRD_2D Setup Window (TLA V5.6 or later)

Set the Ts value for the Setup time derived from the analysis of the MagniVu data performed in Section 5. This should automatically set the appropriate Hold time for the group.

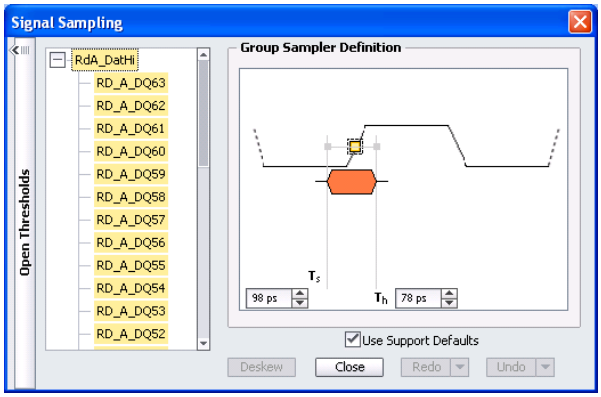


Figure 34 – B_DDR3D_2D Capture Point Window (TLA V5.6 or later)

APPENDIX C - Considerations

C.1 NEX-DDR3INTR-HS Bus Loading

It must be noted that the NEX-DDR3INTR-HS Interposer is designed to minimal effect on the user's circuit. The acquired signals are sampled at top edge connector, and then passed through isolation resistors to the probe. There will be an effective 600 ohm load on all probed signals.

C.2 DIMM connector location for best quality signal capture

An interposer is subject to reflected noise and the quality of the acquisitions should improve if the Interposer is in the furthest slot away from the memory controller. If the memory channel contains two DIMM slots and only one will be used, the slot used must be the furthest away from the memory controller.

APPENDIX D – 240-pin DDR3 DIMM Pinout

Front Side (left 1-60)			Back Side (right 121-180			Front Side (left 61-120)			Back Side (right 181-240)		
Pin #	X64 Non-Parity	X72 ECC	Pin #	X64 Non-Parity	X72 ECC	Pin #	X64 Non-Parity	X72 ECC	Pin #	X64 Non-Parity	X72 ECC
1	VREF	VREF	121	VSS	VSS	61	A2	A2	181	A1	A1
2	VSS	VSS	122	DQ4	DQ4	62	VDD	VDD	182	VDD	VDD
3	DQ0	DQ0	123	DQ5	DQ5	63	CK1	CK1	183	VDD	VDD
4	DQ1	DQ1	124	VSS	VSS	64	CK1#	CK1#	184	CK0	CK0
5	VSS	VSS	125	DM0 DQS9	DM0 DQS9	65	VDD	VDD	185	CK0#	CK0#
6	DQS0#	DQS0#	126	NC DQS9#	NC DQS9#	66	VDD	VDD	186	VDD	VDD
7	DQS0	DQS0	127	VSS	VSS	67	VREF	VREF	187	EVENT#/NC	EVENT#/NC
8	VSS	VSS	128	DQ6	DQ6	68	NC Par_In	NC Par_In	188	A0	A0
9	DQ2	DQ2	129	DQ7	DQ7	69	VDD	VDD	189	VDD	VDD
10	DQ3	DQ3	130	VSS	VSS	70	A10/AP	A10/AP	190	BA1	BA1
11	VSS	VSS	131	DQ12	DQ12	71	BA0	BA0	191	VDD	VDD
12	DQ8	DQ8	132	DQ13	DQ13	72	VDD	VDD	192	RAS#	RAS#
13	DQ9	DQ9	133	VSS	VSS	73	WE#	WE#	193	S0#	S0#
14	VSS	VSS	134	DM1 DQS10	DM1 DQS10	74	CAS#	CAS#	194	VDD	VDD
15	DQS1#	DQS1#	135	NC DQS10#	NC DQS10#	75	VDD	VDD	195	ODT0	ODT0
16	DQS1	DQS1	136	VSS	VSS	76	S1#	S1#	196	A13	A13
17	VSS	VSS	137	DQ14	DQ14	77	RSVD ODT1	RSVD ODT1	197	VDD	VDD
18	DQ10	DQ10	138	DQ15	DQ15	78	VDD	VDD	198	Free	Free
19	DQ11	DQ11	139	VSS	VSS	79	RSVD SPD#	RSVD Spd3	199	VSS	VSS
20	VSS	VSS	140	DQ20	DQ20	80	VSS	VSS	200	DQ36	DQ36
21	DQ16	DQ16	141	DQ21	DQ21	81	DQ32	DQ32	201	DQ37	DQ37
22	DQ17	DQ17	142	VSS	VSS	82	DQ33	DQ33	202	VSS	VSS
23	VSS	VSS	143	DML2, DQS11	DML2 DQS11	83	VSS	VSS	203	DM4 DQS13	DM4 DQS13
24	DQS2#	DQS2#	144	DQS11#	DQS11#	84	DQS4#	DQS4#	204	DQS13#	DQS13#
25	DQS2	DQS2	145	VSS	VSS	85	DQS4	DQS4	205	VSS	VSS
26	VSS	VSS	146	DQ22	DQ22	86	VSS	VSS	206	DQ38	DQ38
27	DQ18	DQ18	147	DQ23	DQ23	87	DQ34	DQ34	207	DQ39	DQ39
28	DQ19	DQ19	148	VSS	VSS	88	DQ35	DQ35	208	VSS	VSS
29	VSS	VSS	149	DQ28	DQ28	89	VSS	VSS	209	DQ44	DQ44
30	DQ24	DQ24	150	DQ29	DQ29	90	DQ40	DQ40	210	DQ45	DQ45
31	DQ25	DQ25	151	VSS	VSS	91	DQ41	DQ41	211	VSS	VSS
32	VSS	VSS	152	DM3 DQS12	DM3 DQS12	92	VSS	VSS	212	DM5 DQS14	DM5 DQS14
33	DQS3#	DQS3#	153	DQS12#	DQS12#	93	DQS5#	DQS5#	213	DQS14#	DQS14#
34	DQS3	DQS3	154	VSS	VSS	94	DQS5	DQS5	214	VSS	VSS
35	VSS	VSS	155	DQ30	DQ30	95	VSS	VSS	215	DQ46	DQ46
36	DQ26	DQ26	156	DQ31	DQ31	96	DQ42	DQ42	216	DQ47	DQ47
37	DQ27	DQ27	157	VSS	VSS	97	DQ43	DQ43	217	VSS	VSS
38	VSS	VSS	158	NC	CB4	98	VSS	VSS	218	DQ52	DQ52
39	NC	CB0	159	NC	CB5	99	DQ48	DQ48	219	DQ53	DQ53
40	NC	CB1	160	VSS	VSS	100	DQ49	DQ49	220	VSS	VSS

APPENDIX D - 240-pin DDR3 DIMM Pinout (cont'd.)

Front Side (left 1-60)			Back Side (right 121-180			Front Side (left 61-120)			Back Side (right 181-240)		
Pin #	X64 Non-Parity	X72 ECC	Pin #	X64 Non-Parity	X72 ECC	Pin #	X64 Non-Parity	X72 ECC	Pin #	X64 Non-Parity	X72 ECC
41	VSS	VSS	161	DM8 DQS17	DM8 DQS17	101	VSS	VSS	221	DM6 DQS15	DM6 DQS15
42	DQS8#	DQS8#	162	DQS17#	DQS17#	102	DQS6#	DQS6#	222	DQS15#	DQS15#
43	DQS8	DQS8	163	VSS	VSS	103	DQS6	DQS6	223	VSS	VSS
44	VSS	VSS	164	NC	CB6	104	VSS	VSS	224	DQ54	DQ54
45	NC	CB2	165	NC	CB7	105	DQ50	DQ50	225	DQ55	DQ55
46	NC	CB3	166	VSS	VSS	106	DQ51	DQ51	226	VSS	VSS
47	VSS	VSS	167	Test	Test	107	VSS	VSS	227	DQ60	DQ60
48	Free	Free	168	Free	Free	108	DQ56	DQ56	228	DQ61	DQ61
KEY			KEY			109	DQ57	DQ57	229	VSS	VSS
49	RESET#	RESET#	169	CKE1	CKE1	110	VSS	VSS	230	DM7 DQS16	DM7 DQS16
50	CKE0	CKE0	170	VDD	VDD	111	DQS7#	DQS7#	231	DQS16#	DQS16#
51	VDD	VDD	171	A15	A15	112	DQS7	DQS7	232	VSS	VSS
52	BA2	BA2	172	A14	A14	113	VSS	VSS	233	DQ62	DQ62
53	NC ERR-OUT#	NC ERR-OUT#	173	VDD	VDD	114	DQ58	DQ58	234	DQ63	DQ63
54	VDD	VDD	174	A12	A12	115	DQ59	DQ59	235	VSS	VSS
55	A11	A11	175	A9	A9	116	VSS	VSS	236	VDDSPD	VDDSPD
56	A7	A7	176	VDD	VDD	117	SA0	SA0	237	SA1	SA1
57	VDD	VDD	177	A8	A8	118	SLC	SLC	238	SDA	SDA
58	A5	A5	178	A6	A6	119	SA2	SA2	239	VSS	VSS
59	A4	A4	179	VDD	VDD	120	VTT	VTT	240	VTT	VTT
60	VDD	VDD	180	A3	A3						

APPENDIX E – Data Flow Through the Probes (coax cable to channel)

Coax wire PIN	Coax P153/163 Channel PRB1X/P6960HCD	Coax P152/162 Channel PRB2X/P6962HCD	Coax P154/164 Channel PRB2X/P6962HCD	Coax P151/161 Channel PRB2X/P6962HCD
J16-2	C2:0	A0:0	A0:0	E2:0
J16-5	C2:5	A0:5	A0:5	E2:5
J16-8	C3:3	A1:3	A1:3	E3:3
J16-11	C1:5	A3:5	A3:5	C3:5
J16-14	C1:0	A3:0	A3:0	C3:0
J16-17	C0:3	A2:3	A2:3	C2:3
J16-4	C2:4	A0:4	A0:4	E2:4
J16-7	C3:2	A1:2	A1:2	E3:2
J16-10	C3:7	A1:7	A1:7	E3:7
J16-13	C1:1	A3:1	A3:1	C3:1
J16-16	C0:6	A2:6	A2:6	C2:6
J16-3	C2:1	A0:1	A0:1	E2:1
J16-6	CLK3	CLK1	CLK1	Q3
J16-9	C3:6	A1:6	A1:6	E3:6
J16-12	C1:4	A3:4	A3:4	C3:4
J16-15	C0:7	A2:7	A2:7	C2:7
J16-18	C0:2	A2:2	A2:2	C2:2
J15-18	C2:2	A0:2	A0:2	E2:2
J15-15	C2:7	A0:7	A0:7	E2:7
J15-12	C3:4	A1:4	A1:4	E3:4
J15-9	C1:6	A3:6	A3:6	C3:6
J15-6	Q1	CLK0	CLK0	CLK3
J15-3	C0:1	A2:1	A2:1	C2:1
J15-16	C2:6	A0:6	A0:6	E2:6
J15-13	C3:1	A1:1	A1:1	E3:1
J15-10	C1:7	A3:7	A3:7	C3:7
J15-7	C1:2	A3:2	A3:2	C3:2
J15-4	C0:4	A2:4	A2:4	C2:4
J15-17	C2:3	A0:3	A0:3	E2:3
J15-14	C3:0	A1:0	A1:0	E3:0
J15-11	C3:5	A1:5	A1:5	E3:5
J15-8	C1:3	A3:3	A3:3	C3:3
J15-5	C0:5	A2:5	A2:5	C2:5
J15-2	C0:0	A2:0	A2:0	C2:0

APPENDIX D – Data Flow Through the Probes (coax cable to channel) (Cont'd.)

Coax wire PIN	Coax P153/163 Channel PRB1X/P6960HCD	Coax P152/162 Channel PRB1X/P6960HCD	Coax P154/164 Channel PRB1X/P6960HCD	Coax P151/161 Channel PRB1X/P6960HCD
J16-2	C2:0	A2:0	A0:0	E2:0
J16-5	C2:5	A2:5	A0:5	E2:5
J16-8	C3:3	A3:3	A1:3	E3:3
J16-11	C1:5	D3:5	D1:5	E1:5
J16-14	C1:0	D3:0	D1:0	E1:0
J16-17	C0:3	D2:3	D0:3	E0:3
J16-4	C2:4	A2:4	A0:4	E2:4
J16-7	C3:2	A3:2	A1:2	E3:2
J16-10	C3:7	A3:7	A1:7	E3:7
J16-13	C1:1	D3:1	D1:1	E1:1
J16-16	C0:6	D2:6	D0:6	E0:6
J16-3	C2:1	A2:1	A0:1	E2:1
J16-6	CLK3	CLK0	CLK1	Q3
J16-9	C3:6	A3:6	A1:6	E3:6
J16-12	C1:4	D3:4	D1:4	E1:4
J16-15	C0:7	D2:7	D0:7	E0:7
J16-18	C0:2	D2:2	D0:2	E0:2
J15-18	C2:2	A2:2	A0:2	E2:2
J15-15	C2:7	A2:7	A0:7	E2:7
J15-12	C3:4	A3:4	A1:4	E3:4
J15-9	C1:6	D2:6	D1:6	E1:6
J15-6	Q1	Q0	CLK2	Q2
J15-3	C0:1	D2:1	D0:1	E0:1
J15-16	C2:6	A2:6	A0:6	E2:6
J15-13	C3:1	A3:1	A1:1	E3:1
J15-10	C1:7	D3:7	D1:7	E1:7
J15-7	C1:2	D3:2	D1:2	E1:2
J15-4	C0:4	D2:4	D0:4	E0:4
J15-17	C2:3	A2:3	A0:3	E2:3
J15-14	C3:0	A3:0	A1:0	E3:0
J15-11	C3:5	A3:5	A1:5	E3:5
J15-8	C1:3	D3:3	D1:3	E1:3
J15-5	C0:5	D2:5	D0:5	E0:5
J15-2	C0:0	D2:0	D0:0	E0:0

APPENDIX F – B_DDR3D_2D Support Pinout

HCD	Coax Pin	TLA Channel	DDR3 Signal
D10	J15-6	CK0	A15
E8	J15-10	A3:7	TEST
D8	J15-9	A3:6	RESET#
A8	J16-11	A3:5	
C8	J16-12	A3:4	
F8	J15-8	A3:3	
E10	J15-7	A3:2	CKE1
B8	J16-13	A3:1	CKE0
A10	J16-14	A3:0	BA2
C10	J16-15	A2:7	ERR_OUT#
B10	J16-16	A2:6	A11
F10	J15-5	A2:5	A14
E12	J15-4	A2:4	A12/BC#
A12	J16-17	A2:3	A7
C12	J16-18	A2:2	A5
D12	J15-3	A2:1	A9
F12	J15-2	A2:0	A8
C4	J16-6	CK1	CB1
B6	J16-10	A1:7	
C6	J16-9	A1:6	CB3
F6	J15-11	A1:5	CB7
D6	J15-12	A1:4	CB6
A6	J16-8	A1:3	CB2
B4	J16-7	A1:2	DQS8
E6	J15-13	A1:1	DM8
F4	J15-14	A1:0	CB5
D4	J15-15	A0:7	CB4
E4	J15-16	A0:6	DQ31
A4	J16-5	A0:5	CB0
B2	J16-4	A0:4	DQ27
F2	J15-17	A0:3	DQ30
D2	J15-18	A0:2	DM3
C2	J16-3	A0:1	DQ26
A2	J16-2	A0:0	DQS3

PRB2X Probe Connection for B_DDR3D_2D software
Coax P152/162

HCD	Coax Pin	TLA Channel	DDR3 Signal
D10	J15-6	CK3	A13
E8	J15-10	C3:7	BA1
D8	J15-9	C3:6	RAS#
A8	J16-11	C3:5	CAS#
C8	J16-12	C3:4	S1#
F8	J15-8	C3:3	S0#
E10	J15-7	C3:2	ODT0
B8	J16-13	C3:1	ODT1
A10	J16-14	C3:0	S2#
C10	J16-15	C2:7	DQ32
B10	J16-16	C2:6	DQ33
F10	J15-5	C2:5	S3#
E12	J15-4	C2:4	DQ36
A12	J16-17	C2:3	DQS4
C12	J16-18	C2:2	
D12	J15-3	C2:1	DQ37
F12	J15-2	C2:0	DM4
C4	J16-6	Q3	A2
B6	J16-10	E3:7	WE#
C6	J16-9	E3:6	BA0
F6	J15-11	E3:5	A0
D6	J15-12	E3:4	CK0
A6	J16-8	E3:3	A10/AP
B4	J16-7	E3:2	PAR_IN
E6	J15-13	E3:1	A1
F4	J15-14	E3:0	A3
D4	J15-15	E2:7	
E4	J15-16	E2:6	
A4	J16-5	E2:5	A4
B2	J16-4	E2:4	
F2	J15-17	E2:3	
D2	J15-18	E2:2	A6
C2	J16-3	E2:1	
A2	J16-2	E2:0	

PRB1X Probe Connection for B_DDR3D_2D software
Coax P153/163

APPENDIX F – B_DDR3D_2D Support Pinout (Cont'd.)

HCD	Coax Pin	TLA Channel	DDR3 Signal	HCD	Coax Pin	TLA Channel	DDR3 Signal
D10	J15-6	CK0	DQ60	D10	J15-6	CK3	DM2
E8	J15-10	A3:7	DQ53	E8	J15-10	C3:7	DQ14
D8	J15-9	A3:6	DM6	D8	J15-9	C3:6	DQ15
A8	J16-11	A3:5	DQS6	A8	J16-11	C3:5	DQ11
C8	J16-12	A3:4	DQ50	C8	J16-12	C3:4	DQ16
F8	J15-8	A3:3	DQ54	F8	J15-8	C3:3	DQ20
E10	J15-7	A3:2	DQ55	E10	J15-7	C3:2	DQ21
B8	J16-13	A3:1	DQ51	B8	J16-13	C3:1	DQ17
A10	J16-14	A3:0	DQ56	A10	J16-14	C3:0	DQS2
C10	J16-15	A2:7	DQ57	C10	J16-15	C2:7	DQ18
B10	J16-16	A2:6	DQS7	B10	J16-16	C2:6	DQ19
F10	J15-5	A2:5	DQ61	F10	J15-5	C2:5	DQ22
E12	J15-4	A2:4	DM7	E12	J15-4	C2:4	DQ23
A12	J16-17	A2:3	DQ58	A12	J16-17	C2:3	DQ24
C12	J16-18	A2:2	DQ59	C12	J16-18	C2:2	DQ25
D12	J15-3	A2:1	DQ62	D12	J15-3	C2:1	DQ28
F12	J15-2	A2:0	DQ63	F12	J15-2	C2:0	DQ29
C4	J16-6	CK1	DQS5	C4	J16-6	Q3	DQ3
B6	J16-10	A1:7	DQ49	B6	J16-10	E3:7	DQ10
C6	J16-9	A1:6	DQ48	C6	J16-9	E3:6	DQS1
F6	J15-11	A1:5	DQ52	F6	J15-11	E3:5	DM1
D6	J15-12	A1:4	DQ47	D6	J15-12	E3:4	DQ13
A6	J16-8	A1:3	DQ43	A6	J16-8	E3:3	DQ9
B4	J16-7	A1:2	DQ42	B4	J16-7	E3:2	DQ8
E6	J15-13	A1:1	DQ46	E6	J15-13	E3:1	DQ12
F4	J15-14	A1:0	DM5	F4	J15-14	E3:0	DQ7
D4	J15-15	A0:7	DQ45	D4	J15-15	E2:7	DQ6
E4	J15-16	A0:6	DQ44	E4	J15-16	E2:6	DM0
A4	J16-5	A0:5	DQ41	A4	J16-5	E2:5	DQ2
B2	J16-4	A0:4	DQ40	B2	J16-4	E2:4	DQS0
F2	J15-17	A0:3	DQ39	F2	J15-17	E2:3	DQ5
D2	J15-18	A0:2	DQ38	D2	J15-18	E2:2	DQ4
C2	J16-3	A0:1	DQ35	C2	J16-3	E2:1	DQ1
A2	J16-2	A0:0	DQ34	A2	J16-2	E2:0	DQ0
PRB2X Probe Connection for B_DDR3D_2D software Coax P154/164				**PRB2X Probe Connection for B_DDR3D_2D software Coax P151/161**			

APPENDIX G – B_DDR3D_4A Support Pinout

HCD	Coax Pin	TLA Channel	DDR3 Signal	HCD	Coax Pin	TLA Channel	DDR3 Signal
D10	J15-6	CK0	CB1	D10	J16-6	CK3	A13
E8	J15-10	A3:7		E8	J16-10	C3:7	BA1
D8	J15-9	A3:6	CB3	D8	J16-9	C3:6	RAS#
A8	J16-11	A3:5	CB7	A8	J15-11	C3:5	CAS#
C8	J16-12	A3:4	CB6	C8	J15-12	C3:4	S1#
F8	J15-8	A3:3	CB2	F8	J16-8	C3:3	S0#
E10	J15-7	A3:2	DQS8	E10	J16-7	C3:2	ODT0
B8	J16-13	A3:1	DM8	B8	J15-13	C3:1	ODT1
A10	J16-14	A3:0	CB5	A10	J15-14	C3:0	S2#
C10	J16-15	A2:7	CB4	C10	J15-15	C2:7	DQ32
B10	J16-16	A2:6	DQ31	B10	J15-16	C2:6	DQ33
F10	J15-5	A2:5	CB0	F10	J16-5	C2:5	S3#
E12	J15-4	A2:4	DQ27	E12	J16-4	C2:4	DQ36
A12	J16-17	A2:3	DQ30	A12	J15-17	C2:3	DQS4
C12	J16-18	A2:2	DM3	C12	J15-18	C2:2	NC
D12	J15-3	A2:1	DQ26	D12	J16-3	C2:1	DQ37
F12	J15-2	A2:0	DQS3	F12	J16-2	C2:0	DM4
C4	J16-6	CK1	A15	C4	J15-6	Q1	A2
B6	J16-10	A1:7	TEST	B6	J15-10	C1:7	WE#
C6	J16-9	A1:6	RESET#	C6	J15-9	C1:6	BA0
F6	J15-11	A1:5		F6	J16-11	C1:5	A0
D6	J15-12	A1:4		D6	J16-12	C1:4	CK0
A6	J16-8	A1:3		A6	J15-8	C1:3	A10/AP
B4	J16-7	A1:2	CKE1	B4	J15-7	C1:2	PAR_IN
E6	J15-13	A1:1	CKE0	E6	J16-13	C1:1	A1
F4	J15-14	A1:0	BA2	F4	J16-14	C1:0	A3
D4	J15-15	A0:7	ERR_OUT#	D4	J16-15	C0:7	
E4	J15-16	A0:6	A11	E4	J16-16	C0:6	
A4	J16-5	A0:5	A14	A4	J15-5	C0:5	A4
B2	J16-4	A0:4	A12/BC#	B2	J15-4	C0:4	
F2	J15-17	A0:3	A7	F2	J16-17	C0:3	
D2	J15-18	A0:2	A5	D2	J16-18	C0:2	A6
C2	J16-3	A0:1	A9	C2	J15-3	C0:1	
A2	J16-2	A0:0	A8	A2	J15-2	C0:0	

P6962HCD 2X Probe Connection for B_DDR3D_4A software
Coax P152/162

P6960HCD 1X Probe Connection for B_DDR3D_4A software
Coax P153/163

APPENDIX G – B_DDR3D_4A Support Pinout (cont'd.)

HCD	Coax Pin	TLA Channel	DDR3 Signal
D10	J15-6	CK0	DQS5
E8	J15-10	A3:7	DQ49
D8	J15-9	A3:6	DQ48
A8	J16-11	A3:5	DQ52
C8	J16-12	A3:4	DQ47
F8	J15-8	A3:3	DQ43
E10	J15-7	A3:2	DQ42
B8	J16-13	A3:1	DQ46
A10	J16-14	A3:0	DM5
C10	J16-15	A2:7	DQ45
B10	J16-16	A2:6	DQ44
F10	J15-5	A2:5	DQ41
E12	J15-4	A2:4	DQ40
A12	J16-17	A2:3	DQ39
C12	J16-18	A2:2	DQ38
D12	J15-3	A2:1	DQ35
F12	J15-2	A2:0	DQ34
C4	J16-6	CK1	DQ60
B6	J16-10	A1:7	DQ53
C6	J16-9	A1:6	DM6
F6	J15-11	A1:5	DQS6
D6	J15-12	A1:4	DQ50
A6	J16-8	A1:3	DQ54
B4	J16-7	A1:2	DQ55
E6	J15-13	A1:1	DQ51
F4	J15-14	A1:0	DQ56
D4	J15-15	A0:7	DQ57
E4	J15-16	A0:6	DQS7
A4	J16-5	A0:5	DQ61
B2	J16-4	A0:4	DM7
F2	J15-17	A0:3	DQ58
D2	J15-18	A0:2	DQ59
C2	J16-3	A0:1	DQ62
A2	J16-2	A0:0	DQ63

P6962HCD 2X Probe Connection for B_DDR3D_4A software Coax P154/164

HCD	Coax Pin	TLA Channel	DDR3 Signal
D10	J15-6	CK0	DQ3
E8	J15-10	A3:7	DQ10
D8	J15-9	A3:6	DQS1
A8	J16-11	A3:5	DM1
C8	J16-12	A3:4	DQ13
F8	J15-8	A3:3	DQ9
E10	J15-7	A3:2	DQ8
B8	J16-13	A3:1	DQ12
A10	J16-14	A3:0	DQ7
C10	J16-15	A2:7	DQ6
B10	J16-16	A2:6	DM0
F10	J15-5	A2:5	DQ2
E12	J15-4	A2:4	DQS0
A12	J16-17	A2:3	DQ5
C12	J16-18	A2:2	DQ4
D12	J15-3	A2:1	DQ1
F12	J15-2	A2:0	DQ0
C4	J16-6	CK1	DM2
B6	J16-10	A1:7	DQ14
C6	J16-9	A1:6	DQ15
F6	J15-11	A1:5	DQ11
D6	J15-12	A1:4	DQ16
A6	J16-8	A1:3	DQ20
B4	J16-7	A1:2	DQ21
E6	J15-13	A1:1	DQ17
F4	J15-14	A1:0	DQS2
D4	J15-15	A0:7	DQ18
E4	J15-16	A0:6	DQ19
A4	J16-5	A0:5	DQ22
B2	J16-4	A0:4	DQ23
F2	J15-17	A0:3	DQ24
D2	J15-18	A0:2	DQ25
C2	J16-3	A0:1	DQ28
A2	J16-2	A0:0	DQ29

P6962HCD 2X Probe Connection for B_DDR3D_4A software Coax P151/161

APPENDIX H – R_DDR3D_2A Support Pinout

HCD	Coax Pin	TLA Channel	DDR3 Signal	HCD	Coax Pin	TLA Channel	DDR3 Signal
D10	J15-6	Q0	CB1	D10	J16-6	CK3	A13
E8	J15-10	D3:7		E8	J16-10	C3:7	BA1
D8	J15-9	D3:6	CB3	D8	J16-9	C3:6	RAS#
A8	J16-11	D3:5	CB7	A8	J15-11	C3:5	CAS#
C8	J16-12	D3:4	CB6	C8	J15-12	C3:4	S1#
F8	J15-8	D3:3	CB2	F8	J16-8	C3:3	S0#
E10	J15-7	D3:2	DQS8	E10	J16-7	C3:2	ODT0
B8	J16-13	D3:1	DM8	B8	J15-13	C3:1	ODT1
A10	J16-14	D3:0	CB5	A10	J15-14	C3:0	S2#
C10	J16-15	D2:7	CB4	C10	J15-15	C2:7	DQ32
B10	J16-16	D2:6	DQ31	B10	J15-16	C2:6	DQ33
F10	J15-5	D2:5	CB0	F10	J16-5	C2:5	S3#
E12	J15-4	D2:4	DQ27	E12	J16-4	C2:4	DQ36
A12	J16-17	D2:3	DQ30	A12	J15-17	C2:3	DQS4
C12	J16-18	D2:2	DM3	C12	J15-18	C2:2	NC
D12	J15-3	D2:1	DQ26	D12	J16-3	C2:1	DQ37
F12	J15-2	D2:0	DQS3	F12	J16-2	C2:0	DM4
C4	J16-6	CK0	A15	C4	J15-6	Q1	A2
B6	J16-10	A3:7	TEST	B6	J15-10	C1:7	WE#
C6	J16-9	A3:6	RESET#	C6	J15-9	C1:6	BA0
F6	J15-11	A3:5		F6	J16-11	C1:5	A0
D6	J15-12	A3:4		D6	J16-12	C1:4	CK0
A6	J16-8	A3:3		A6	J15-8	C1:3	A10/AP
B4	J16-7	A3:2	CKE1	B4	J15-7	C1:2	PAR_IN
E6	J15-13	A3:1	CKE0	E6	J16-13	C1:1	A1
F4	J15-14	A3:0	BA2	F4	J16-14	C1:0	A3
D4	J15-15	A2:7	ERR_OUT#	D4	J16-15	C0:7	
E4	J15-16	A2:6	A11	E4	J16-16	C0:6	
A4	J16-5	A2:5	A14	A4	J15-5	C0:5	A4
B2	J16-4	A2:4	A12/BC#	B2	J15-4	C0:4	
F2	J15-17	A2:3	A7	F2	J16-17	C0:3	
D2	J15-18	A2:2	A5	D2	J16-18	C0:2	A6
C2	J16-3	A2:1	A9	C2	J15-3	C0:1	
A2	J16-2	A2:0	A8	A2	J15-2	C0:0	

P6960HCD 1X Probe Connection for R_DDR3D_2A software
Coax P152/162

P6960HCD 1X Probe Connection for R_DDR3D_2A software
Coax P153/163

APPENDIX H – R_DDR3D_2A Support Pinout (cont'd.)

HCD	Coax Pin	TLA Channel	DDR3 Signal
D10	J15-6	CK2	DQS5
E8	J15-10	D1:7	DQ49
D8	J15-9	D1:6	DQ48
A8	J16-11	D1:5	DQ52
C8	J16-12	D1:4	DQ47
F8	J15-8	D1:3	DQ43
E10	J15-7	D1:2	DQ42
B8	J16-13	D1:1	DQ46
A10	J16-14	D1:0	DM5
C10	J16-15	D0:7	DQ45
B10	J16-16	D0:6	DQ44
F10	J15-5	D0:5	DQ41
E12	J15-4	D0:4	DQ40
A12	J16-17	D0:3	DQ39
C12	J16-18	D0:2	DQ38
D12	J15-3	D0:1	DQ35
F12	J15-2	D0:0	DQ34
C4	J16-6	CK1	DQ60
B6	J16-10	A1:7	DQ53
C6	J16-9	A1:6	DM6
F6	J15-11	A1:5	DQS6
D6	J15-12	A1:4	DQ50
A6	J16-8	A1:3	DQ54
B4	J16-7	A1:2	DQ55
E6	J15-13	A1:1	DQ51
F4	J15-14	A1:0	DQ56
D4	J15-15	A0:7	DQ57
E4	J15-16	A0:6	DQS7
A4	J16-5	A0:5	DQ61
B2	J16-4	A0:4	DM7
F2	J15-17	A0:3	DQ58
D2	J15-18	A0:2	DQ59
C2	J16-3	A0:1	DQ62
A2	J16-2	A0:0	DQ63

P6960HCD 1X Probe Connection for R_DDR3D_2A software Coax P154/164

HCD	Coax Pin	TLA Channel	DDR3 Signal
D10	J15-6	Q2	DQ3
E8	J15-10	E1:7	DQ10
D8	J15-9	E1:6	DQS1
A8	J16-11	E1:5	DM1
C8	J16-12	E1:4	DQ13
F8	J15-8	E1:3	DQ9
E10	J15-7	E1:2	DQ8
B8	J16-13	E1:1	DQ12
A10	J16-14	E1:0	DQ7
C10	J16-15	E0:7	DQ6
B10	J16-16	E0:6	DM0
F10	J15-5	E0:5	DQ2
E12	J15-4	E0:4	DQS0
A12	J16-17	E0:3	DQ5
C12	J16-18	E0:2	DQ4
D12	J15-3	E0:1	DQ1
F12	J15-2	E0:0	DQ0
C4	J16-6	Q3	DM2
B6	J16-10	E3:7	DQ14
C6	J16-9	E3:6	DQ15
F6	J15-11	E3:5	DQ11
D6	J15-12	E3:4	DQ16
A6	J16-8	E3:3	DQ20
B4	J16-7	E3:2	DQ21
E6	J15-13	E3:1	DQ17
F4	J15-14	E3:0	DQS2
D4	J15-15	E2:7	DQ18
E4	J15-16	E2:6	DQ19
A4	J16-5	E2:5	DQ22
B2	J16-4	E2:4	DQ23
F2	J15-17	E2:3	DQ24
D2	J15-18	E2:2	DQ25
C2	J16-3	E2:1	DQ28
A2	J16-2	E2:0	DQ29

P6960HCD 1X Probe Connection for R_DDR3D_2A software Coax P151/161

APPENDIX I – R_DDR3D_1A Support Pinout

HCD	Coax Pin	TLA Channel	DDR3 Signal	HCD	Coax Pin	TLA Channel	DDR3 Signal
D10	J15-6	Q0	CB1	D10	J16-6	CK3	A13
E8	J15-10	D3:7		E8	J16-10	C3:7	BA1
D8	J15-9	D3:6	CB3	D8	J16-9	C3:6	RAS#
A8	J16-11	D3:5	CB7	A8	J15-11	C3:5	CAS#
C8	J16-12	D3:4	CB6	C8	J15-12	C3:4	S1#
F8	J15-8	D3:3	CB2	F8	J16-8	C3:3	S0#
E10	J15-7	D3:2	DQS8	E10	J16-7	C3:2	ODT0
B8	J16-13	D3:1	DM8	B8	J15-13	C3:1	ODT1
A10	J16-14	D3:0	CB5	A10	J15-14	C3:0	S2#
C10	J16-15	D2:7	CB4	C10	J15-15	C2:7	DQ32
B10	J16-16	D2:6	DQ31	B10	J15-16	C2:6	DQ33
F10	J15-5	D2:5	CB0	F10	J16-5	C2:5	S3#
E12	J15-4	D2:4	DQ27	E12	J16-4	C2:4	DQ36
A12	J16-17	D2:3	DQ30	A12	J15-17	C2:3	DQS4
C12	J16-18	D2:2	DM3	C12	J15-18	C2:2	NC
D12	J15-3	D2:1	DQ26	D12	J16-3	C2:1	DQ37
F12	J15-2	D2:0	DQS3	F12	J16-2	C2:0	DM4
C4	J16-6	CK0	A15	C4	J15-6	Q1	A2
B6	J16-10	A3:7	TEST	B6	J15-10	C1:7	WE#
C6	J16-9	A3:6	RESET#	C6	J15-9	C1:6	BA0
F6	J15-11	A3:5		F6	J16-11	C1:5	A0
D6	J15-12	A3:4		D6	J16-12	C1:4	CK0
A6	J16-8	A3:3		A6	J15-8	C1:3	A10/AP
B4	J16-7	A3:2	CKE1	B4	J15-7	C1:2	PAR_IN
E6	J15-13	A3:1	CKE0	E6	J16-13	C1:1	A1
F4	J15-14	A3:0	BA2	F4	J16-14	C1:0	A3
D4	J15-15	A2:7	ERR_OUT#	D4	J16-15	C0:7	
E4	J15-16	A2:6	A11	E4	J16-16	C0:6	
A4	J16-5	A2:5	A14	A4	J15-5	C0:5	A4
B2	J16-4	A2:4	A12/BC#	B2	J15-4	C0:4	
F2	J15-17	A2:3	A7	F2	J16-17	C0:3	
D2	J15-18	A2:2	A5	D2	J16-18	C0:2	A6
C2	J16-3	A2:1	A9	C2	J15-3	C0:1	
A2	J16-2	A2:0	A8	A2	J15-2	C0:0	

NEX-PRB1XL 1X Probe Connection for R_DDR3D_1A software Coax P152/162

NEX-PRB1XL 1X Probe Connection for R_DDR3D_1A software Coax P153/163

APPENDIX I – R_DDR3D_1A Support Pinout (cont'd.)

HCD	Coax Pin	TLA Channel	DDR3 Signal
D10	J15-6	CK2	DQS5
E8	J15-10	D1:7	DQ49
D8	J15-9	D1:6	DQ48
A8	J16-11	D1:5	DQ52
C8	J16-12	D1:4	DQ47
F8	J15-8	D1:3	DQ43
E10	J15-7	D1:2	DQ42
B8	J16-13	D1:1	DQ46
A10	J16-14	D1:0	DM5
C10	J16-15	D0:7	DQ45
B10	J16-16	D0:6	DQ44
F10	J15-5	D0:5	DQ41
E12	J15-4	D0:4	DQ40
A12	J16-17	D0:3	DQ39
C12	J16-18	D0:2	DQ38
D12	J15-3	D0:1	DQ35
F12	J15-2	D0:0	DQ34
C4	J16-6	CK1	DQ60
B6	J16-10	A1:7	DQ53
C6	J16-9	A1:6	DM6
F6	J15-11	A1:5	DQS6
D6	J15-12	A1:4	DQ50
A6	J16-8	A1:3	DQ54
B4	J16-7	A1:2	DQ55
E6	J15-13	A1:1	DQ51
F4	J15-14	A1:0	DQ56
D4	J15-15	A0:7	DQ57
E4	J15-16	A0:6	DQS7
A4	J16-5	A0:5	DQ61
B2	J16-4	A0:4	DM7
F2	J15-17	A0:3	DQ58
D2	J15-18	A0:2	DQ59
C2	J16-3	A0:1	DQ62
A2	J16-2	A0:0	DQ63

NEX-PRB1XL 1X Probe Connection for R_DDR3D_1A software Coax P154/164

HCD	Coax Pin	TLA Channel	DDR3 Signal
D10	J15-6	Q2	DQ3
E8	J15-10	E1:7	DQ10
D8	J15-9	E1:6	DQS1
A8	J16-11	E1:5	DM1
C8	J16-12	E1:4	DQ13
F8	J15-8	E1:3	DQ9
E10	J15-7	E1:2	DQ8
B8	J16-13	E1:1	DQ12
A10	J16-14	E1:0	DQ7
C10	J16-15	E0:7	DQ6
B10	J16-16	E0:6	DM0
F10	J15-5	E0:5	DQ2
E12	J15-4	E0:4	DQS0
A12	J16-17	E0:3	DQ5
C12	J16-18	E0:2	DQ4
D12	J15-3	E0:1	DQ1
F12	J15-2	E0:0	DQ0
C4	J16-6	Q3	DM2
B6	J16-10	E3:7	DQ14
C6	J16-9	E3:6	DQ15
F6	J15-11	E3:5	DQ11
D6	J15-12	E3:4	DQ16
A6	J16-8	E3:3	DQ20
B4	J16-7	E3:2	DQ21
E6	J15-13	E3:1	DQ17
F4	J15-14	E3:0	DQS2
D4	J15-15	E2:7	DQ18
E4	J15-16	E2:6	DQ19
A4	J16-5	E2:5	DQ22
B2	J16-4	E2:4	DQ23
F2	J15-17	E2:3	DQ24
D2	J15-18	E2:2	DQ25
C2	J16-3	E2:1	DQ28
A2	J16-2	E2:0	DQ29

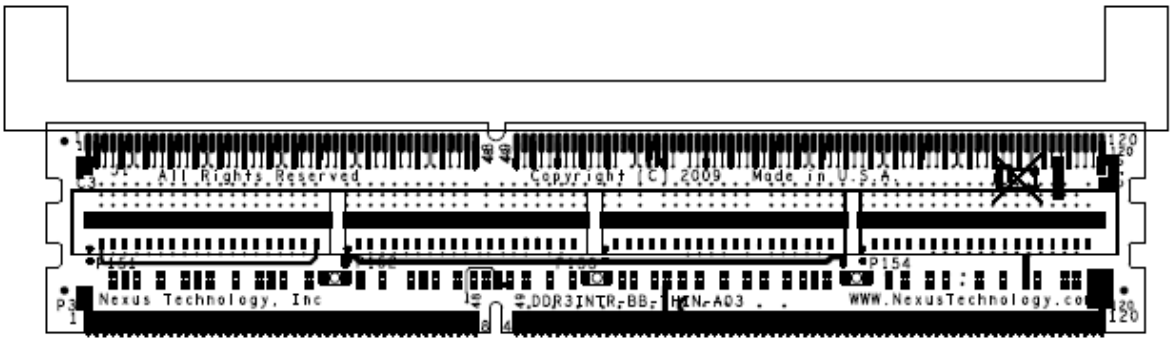
NEX-PRB1XL 1X Probe Connection for R_DDR3D_1A software Coax P151/161

APPENDIX J – Data Group / Data Byte / Strobe Cross-Reference

32-bit Data Group	8-bit Data Group	Strobe	Data Bits
RdADatHi	RdADatB7	DQS7	63,62,61,60,59,58,57,56
	RdADatB6	DQS6	55,54,53,52,51,50,49,48
	RdADatB5	DQS5	47,46,45,44,43,42,41,40
	RdADatB4	DQS4	39,38,37,36,35,34,33,32
RdADatLo	RdADatB3	DQS3	31,30,29,28,27,26,25,24
	RdADatB2	DQS2	23,22,21,20,19,18,17,16
	RdADatB1	DQS1	15,14,13,12,11,10,9,8
	RdADatB0	DQS0	7,6,5,4,3,2,1,0
WrADatHi	WrADatB7	DQS7	63,62,61,60,59,58,57,56
	WrADatB6	DQS6	55,54,53,52,51,50,49,48
	WrADatB5	DQS5	47,46,45,44,43,42,41,40
	WrADatB4	DQS4	39,38,37,36,35,34,33,32
WrADatLo	WrADatB3	DQS3	31,30,29,28,27,26,25,24
	WrADatB2	DQS2	23,22,21,20,19,18,17,16
	WrADatB1	DQS1	15,14,13,12,11,10,9,8
	WrADatB0	DQS0	7,6,5,4,3,2,1,0
RdBDatHi	RdBDatB7	DQS7	63,62,61,60,59,58,57,56
	RdBDatB6	DQS6	55,54,53,52,51,50,49,48
	RdBDatB5	DQS5	47,46,45,44,43,42,41,40
	RdBDatB4	DQS4	39,38,37,36,35,34,33,32
RdBDatLo	RdBDatB3	DQS3	31,30,29,28,27,26,25,24
	RdBDatB2	DQS2	23,22,21,20,19,18,17,16
	RdBDatB1	DQS1	15,14,13,12,11,10,9,8
	RdBDatB0	DQS0	7,6,5,4,3,2,1,0
WrBDatHi	WrBDatB7	DQS7	63,62,61,60,59,58,57,56
	WrBDatB6	DQS6	55,54,53,52,51,50,49,48
	WrBDatB5	DQS5	47,46,45,44,43,42,41,40
	WrBDatB4	DQS4	39,38,37,36,35,34,33,32
WrBDatLo	WrBDatB3	DQS3	31,30,29,28,27,26,25,24
	WrBDatB2	DQS2	23,22,21,20,19,18,17,16
	WrBDatB1	DQS1	15,14,13,12,11,10,9,8
	WrBDatB0	DQS0	7,6,5,4,3,2,1,0

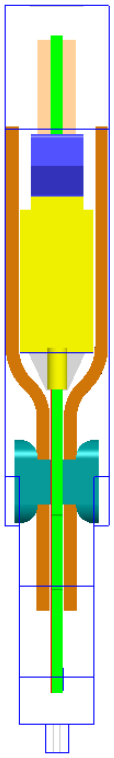
NEX-DDR3INTR-HS Groups/Bytes/Strobes Cross Reference

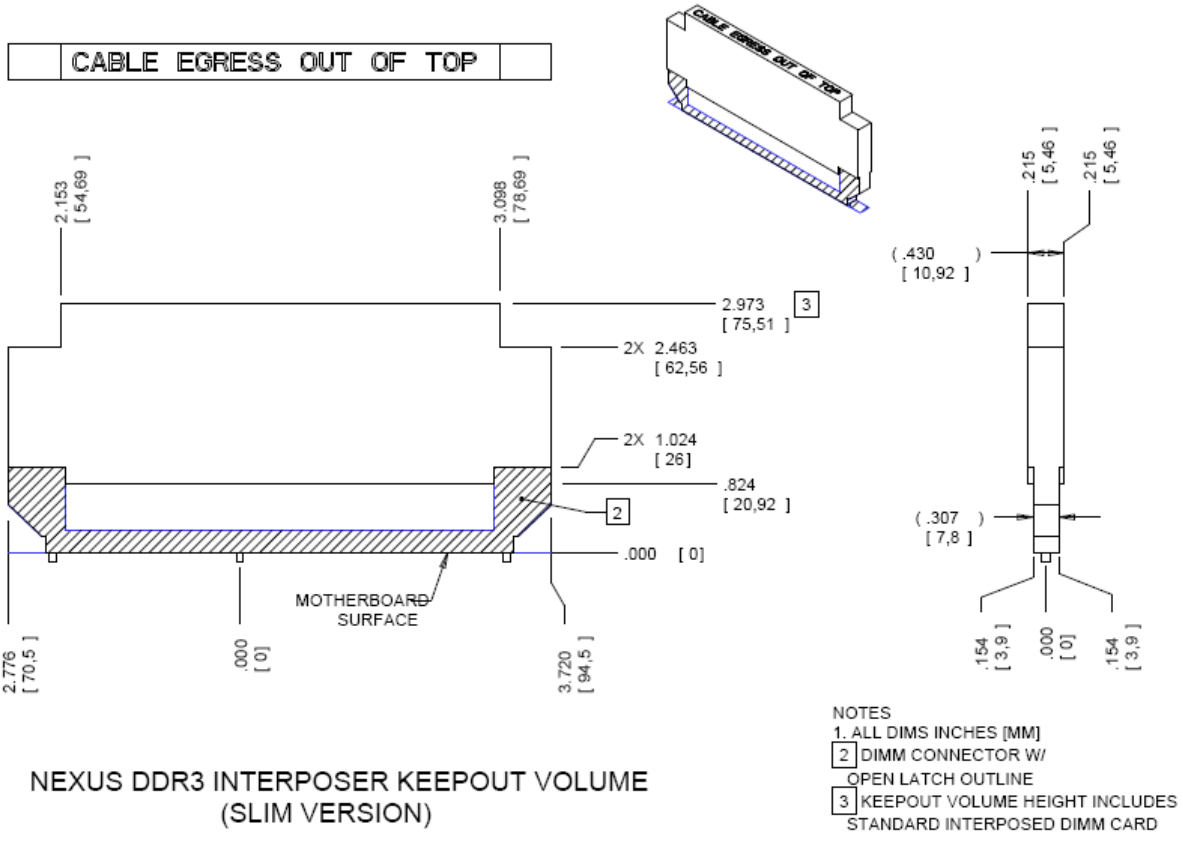
APPENDIX K – NEX-DDR3INTR-HS Silkscreen



Front Silk-screen

APPENDIX L – Keep out area



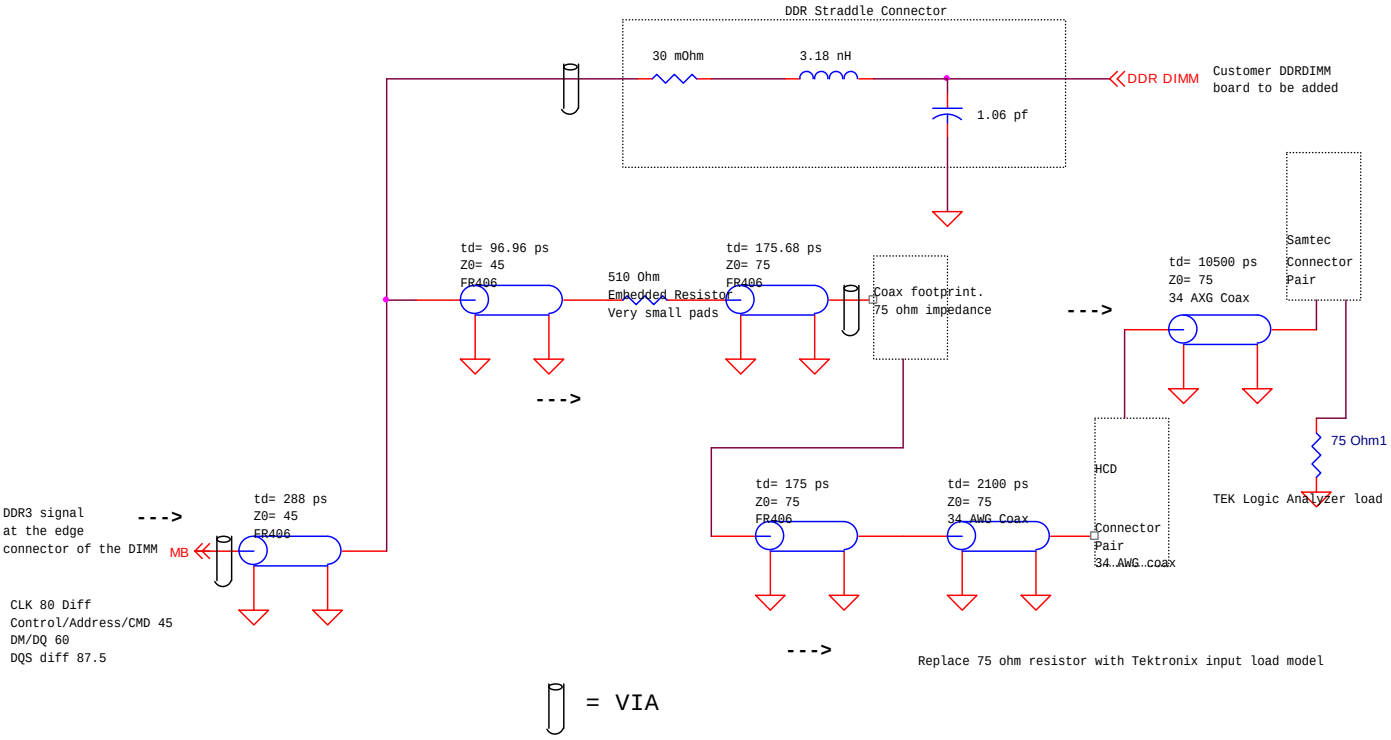


NEXUS DDR3 INTERPOSER KEEPOUT VOLUME
(SLIM VERSION)

NOTES
1. ALL DIMS INCHES [MM]
2 DIMM CONNECTOR W/ OPEN LATCH OUTLINE
3 KEEPOUT VOLUME HEIGHT INCLUDES STANDARD INTERPOSED DIMM CARD

APPENDIX M – Simulation Model

Double this if two Interposers are being used on the same memory channel



APPENDIX N - References

JEDEC PC3-6400/PC3-8500-10660 DDR3 SDRAM Unbuffered DIMM Design Specification Revision 0.1 March 20, 2006.

Tektronix TLA7000 Series Installation Manual
Tek part number 071-1747-03

Tektronix TLA7000 Series Technical Reference Manual
Tektronix part number 071-1764-00

Nexus Low Profile Distributed Probe Manual—
Part number LowProfileProbes-MN-XXX

JEDEC DDR3 SDRAM Standard
JESD79-3 June 2007

APPENDIX O - Support

About Nexus Technology, Inc.

Established in 1991, Nexus Technology, Inc. is dedicated to developing, marketing, and supporting Bus Analysis applications for Tektronix Logic Analyzers.

We can be reached at:

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General Information	**support@nexustechnology.com**
Quote Requests	**quotes@nexustechnology.com**

We will try to respond within one business day.

If Problems Are Found

Document the problem and e-mail the information to us. If at all possible please forward a Saved System Setup (with acquired data) that shows the problem. Please do not send a text listing alone as that does not contain enough data for analysis. To prevent corruption during the mailing process it is strongly suggested that the Setup be zipped before transmission.