WAVETEK

MAINTENANCE MANUAL

Model 91

20 MHz Synthesized Pulse/Function Generator

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WARRANTY

Wavetek warrants that all products manufactured by Wavetek conform to published Wavetek specifications and are free from defects in materials and workmanship for a period of one (1) year from the date of delivery when used under normal operating conditions and within the service conditions for which they were furnished.

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For product warranties requiring return to Wavetek, products must be returned to a service facility designated by Wavetek. Buyer shall prepay shipping charges, taxes, duties and insurance for products returned to Wavetek for warranty service. Except for products returned to Buyer from another country, Wavetek shall pay for return of products to Buyer.

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The Warranty described above is Buyer's sole and exclusive remedy and no other warranty, whether written or oral, is expressed or implied. Wavetek specifically disclaims the implied warranties of merchantability and fitness for a particular purpose. No statement, representation, agreement, or understanding, oral or written, made by an agent, distributor, representative, or employee of Wavetek, which is not contained in the foregoing Warranty will be binding upon Wavetek, unless made in writing and executed by an authorized Wavetek employee. **Under no circumstances shall Wavetek be liable for any direct, indirect, special, incidental, or consequential damages, expenses, losses or delays (including loss of profits) based on contact, tort, or any other legal theory.**

CONTENTS

CONTENTS (Continued)

CONTENTS (Continued)

CONTENTS (Continued)

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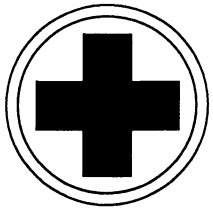
SAFETY FIRST



Protect yourself. Follow these precautions:

- Don't touch the outputs of the instrument or any exposed test wire carrying the output signals. This instrument can generate hazardous voltages and currents
- Don't bypass the power cord's ground lead with two-wire extension cords or plug adapters.
- Don't disconnect the green and yellow safety-earth-ground wire that connects the ground lug of the power receptacle to the chassis ground terminal (marked with  or )
- Don't hold your eyes extremely close to an RF output for a long time. The normally nonhazardous low-power RF energy generated by the instrument could possibly cause eye injury.
- Don't plug in the power cord until directed to by the installation instructions.
- Don't repair the instrument unless you are a qualified electronics technician and know how to work with hazardous voltages.
- Pay attention to the **WARNING** statements. They point out situations that can cause injury or death.
- Pay attention to the CAUTION statements. They point out situations that can cause equipment damage.

WARNING

This instrument normally contains a lithium battery. Where lithium is prohibited, such as aboard U.S. Navy ships, verify that the lithium battery has been removed.

Do not recharge, short circuit, disassemble, or apply heat to the lithium battery. Violating this rule could release potentially harmful lithium. Observe polarity when you replace the battery.

SECTION 1
HOW TO USE THIS MANUAL

1.1. INTRODUCTION

This manual contains information on the testing, calibrating, and servicing of the Wavetek Model 91, 20 MHz Synthesized Pulse/Function Generator.

1.2 WHAT IS IN THIS MANUAL

This manual contains the following sections:

Section 2 Routine Preventive Maintenance.
Section 3 Verification Procedure.
Section 4 Calibration Procedure.
Section 5 Circuit Description.
Section 6 Maintenance (Troubleshooting).
Section 7 The Drawing Package.
Appendix A Product Description and Specifications

1.3 HOW TO USE THIS MANUAL

The purpose of the maintenance manual is to support the technician in keeping the Model 91 functioning correctly. The material in this manual is organized in such a way as to aid the service technician in identifying and isolating a problem with the unit.

Spare And Replacement Parts

Users who plan on servicing the Model 91 may choose to order spare parts from Wavetek. Each assembly contains a parts list; see the drawing package, section 7. All parts listed may be ordered directly from Wavetek. In addition, a recommended spare parts package (Wavetek part number 1200-00-4380) can be ordered from Wavetek.

Suspected Malfunctions

If the Model 91 does not operate correctly, check the instrument setup before trying to isolate the problem; see the *Model 91 Operator's Manual.* Or, perform an AutoCal on the unit to see if the instrument will correct the problem itself; see section 4 of this manual. If there is a problem, performing AutoCal causes the unit to return an error message.

If the problem is known, turn to the appropriate section and correct the fault. Use the Calibration procedure, section 4, when the Model 91 appears out of calibration. Also, the Model 91 provides error messages which can guide the technician to circuit blocks within the instrument; see section 6. Use the maintenance section, section 6, to isolate failures. Section 6 does not isolate problems down to the component level, but only to the circuit block. In addition to the Maintenance section, the Circuit Description, schematics, and assembly drawings all support problem isolation.

1.4 THE OPERATOR'S MANUAL

This manual does not cover the operation of the Model 91. The *Model 91 Operator's Manual* contains that information.

Product description and specifications - Section 1.
Routine Maintenance - Section 2.
Operation (both front panel and remote (GPIB)) - Section 3.

SECTION 2
ROUTINE MAINTENACE

2.1 INTRODUCTION

This section covers routine tasks the Service Technician may perform on the Model 91.

2.2 CALIBRATION

Section 4 of this manual contains both AutoCal and Calibration Procedure instructions.

AutoCal (automatic calibration) provides a quick method of calibrating the Model 91 without the use of external test equipment. AutoCal automatically sets up the instrument and takes internal measurements using internal standards. The Model 91 calculates correction values and stores those values in memory. The Model 91 recalls and loads these correction values at power up. Use AutoCal when Model 91 accuracy is critical, after long term instrument storage or following drastic changes in the environment. Also, perform AutoCal at anytime the Service Technician believes it is necessary.

The Calibration Procedure provides a more extensive method of Model 91 calibration. The Calibration Procedure uses external test equipment and requires opening the instrument for adjustments. Use the Calibration Procedure when the Model 91 displays "CAL REQUIRED" or "FAILED AUTO CAL", after repair, Performance Verification procedure (section 3) failure, or at routine scheduled calibration.

2.3 FUSE REPLACEMENT

To replace the Model 91 fuse (rear panel), use the following instructions.

1. Disconnect the power cord at the instrument. Open the fuse holder cover door. Rotate the fuse-pull to the left to remove the fuse; see figure 2-1.

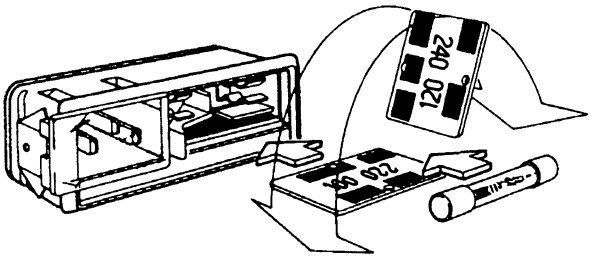


Figure 2-1. Voltage Selector and Fuse

2. Replace the fuse with one having the same current and voltage ratings. The following table lists fuses used with different voltage ranges. Rotate the fuse pull lever back into the normal position. Insert the correct fuse in the fuse holder. Close the fuse holder cover door.

Card Position	Input Vac	Fuse
100	90 to 105	1A, 250 Vac, Slo Blo
120	108 to 126	1A, 250 Vac, Slo Blo
220	198 to 231	1/2A, 250 Vac, Slo Blo
240	216 to 252	1/2A, 250 Vac, Slo Blo

3. Connect the ac line cord to the mating connector at the rear of the unit and power source.

2.4 BATTERY REPLACEMENT

The Model 91 contains a Lithium battery (Panasonic BR-2/3A or equivalent) to power the unit's memory

when power is off. This battery life is typically greater than three years. At power on, the Model 91 checks the battery's condition as part of the power-on Self-test. If Self-test detects a low battery, the display shows "LOW BAT X.XXXV". Replace the battery otherwise the contents of the memory could be lost when power is turned off.

To replace the battery,

1. Remove the top cover and shield. Remove the four screws in the top and the one screw at the rear of the cover. Slide the cover back.

2. With the power ON, replace the old battery, as shown in figure 2-2, with a new battery. Observe the polarity of the battery when installing it. If the power is turned off while replacing the battery, all contents of the RAM will be lost.

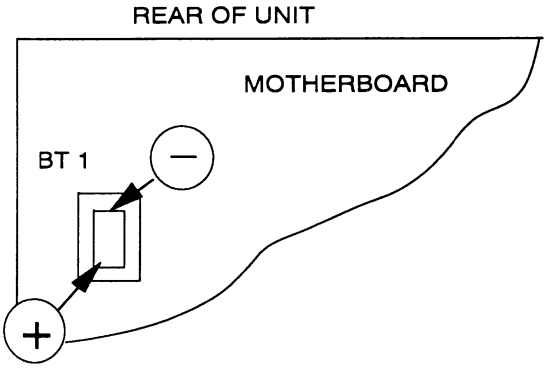


Figure 2-2. RAM Battery

3. Replace the top cover and shield. Secure them using the four screws in the top and the one screw in the rear of the cover.

2.5 FAN MAINTENANCE

The Model 91's fan contains a filter which should be cleaned about every month. Clean the filter more often if the unit is used in a dusty environment.

To clean the Filter,

1. Disconnect the Model 91 from the primary power source.
2. Using a screwdriver, gently pry off the Filter's grill.
3. Remove the foam filter.
4. Clean the foam filter using a mild soapy solution. Thoroughly rinse the filter, and allow it to dry.
5. Place the filter back in the unit, and snap in the Filter's grill.
6. Connect the Model 91 to the primary power source.

SECTION 3
PERFORMANCE VERIFICATION

3.1 PERFORMANCE VERIFICATION

Performance verification tests the operation of every selectable parameter and input/output connector. Furthermore, it verifies the correct operation within each major specification. Use this procedure after a manual calibration (section 4) to confirm the units accuracy. All data obtained during the performance verification should be permanently recorded for future reference. The Verification Form, located at the end of this section, can be used as a master to generate copies. This procedure assumes the person making the tests has a good working knowledge of the Model 91 operation. For information on Model 91 operation, refer to Section 3, Operation of the *Model 91 Operator's Manual.*

Required Test Equipment

Table 3-1 lists the test equipment required to perform the performance verification procedure. Always keep test equipment interconnecting cables as short as possible.

Table 3-1. Required Test Equipment

Test Equipment	Recommended Model
Scope	Tektronix 11402A with 11A52 plug in or equivalent.
THD Analyzer	Hewlett Packard 8903B or equivalent.
DMM	Wavetek Model 1062 or equivalent.
Signal Source	Wavetek Model 23 or equivalent.
Counter/Timer	Hewlett Packard 5335A or equivalent.
Phase Meter	Hewlett Packard 3575A or equivalent.
Signal Source (Option 001)	Wavetek Model 178 or equivalent

Frequency Range

Perform this check to verify the functionality and accuracy of all Model 91 frequency ranges.

1. Initialize the Model 91 by pressing the **SHIFT** and **RESET ALL** key; see table 3-2 for a list of default parameters.

Table 3-2. Model 91 Default Conditions

Parameter	Default Value
Amplitude	5Vpp (2.5 Vp, 1.768 Vrms, 18 dBm)
Burst Count	5
Display	25
Frequency/Period	1kHz (1ms)
Function	Sine
Function Output On/Off	Output Off (50Ω indicator flashes)
Linear/Logarithmic	Linear Sweep
Lock Source	Internal Lock
Logic	Normal
Lower Level	–2.5V
Lower Level Custom	0V
Mode	Continuous
Offset	0V
Phase	0° (0 radians)
Pulse Delay	1µs
Pulse Out	TTL
Pulse Outputs	Off
Pulse Width	500 ns
Recall	Last location stored
Select Output	50Ω, Unbalanced
Store	Last location stored
Sweep Mode	Continuous Sweep
Sweep Start	1kHz
Sweep Stop	10 kHz
Symmetry	50%
Time	1s (1Hz)
Trigger Level	1V
Trigger Frequency	100 Hz (10 ms)
Trigger Slope	Positive
Trig Setup	Internal Trig
Upper Level	+2.5V
Upper Level Custom	+1V

The following keys are not affected by the **RESET ALL** key:

Address
Calibrate
Knob
Local
Man trigger

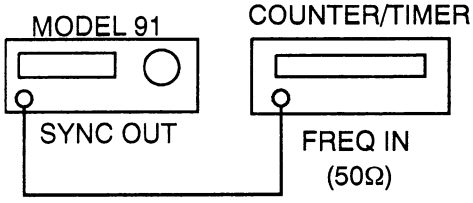


Figure 3-1. Frequency Setup

2. Connect the Model 91 and test equipment as shown in figure 3-1.

3. Program the frequency to the top frequency of each of the upper frequency ranges using the **FREQ/PER** key and knob/keypad.

   20 MHz 2MHz 200 kHz
   20 kHz 2kHz 200 Hz
   20 Hz

   Measure the synthesized frequency accuracy and record the data on the Verification Form - Frequency Ranges, Synthesized.

4. Select Continuous mode (**MODE** key), and set the frequency using the **FREQ/PER** key and knob/keypad:

   20 MHz 2MHz 200 kHz
   20 kHz 2kHz 200 Hz
   20 Hz

   After setting each frequency change to the FM mode (**MODE** key) and measure the frequency. Record the results on the Verification Form - Frequency Ranges, Unlocked FM. Repeat the range measurements for all remaining upper frequency ranges listed.

5. Select Continuous mode (**MODE** key), and set the frequency using the **FREQ/PER** key and knob/keypad:

   2Hz 200 mHz 20 mHz

   Measure the frequency, and record the results on the Verification Form - Frequency Ranges, Unlocked Continuous. Repeat the range measurements for the remaining lower frequency ranges listed.

Frequency Resolution

Perform this test to verify the frequency resolution of the Model 91 on the 2kHz range.

1. Initialize the Model 91 by pressing the **SHIFT** and **RESET ALL** key; see table 3-2 for a list of default parameters.

2. Connect the Model 91 and test equipment as shown in figure 3-1.

4. Set the Model 91 frequency using the **FREQ/PER** key and knob/keypad:

   1999 Hz 1888 Hz 1777 Hz
   1666 Hz 1555 Hz 1444 Hz
   1333 Hz 1222 Hz 1111 Hz
   999 Hz 888 Hz 777 Hz
   666 Hz 555 Hz 444 Hz
   333 Hz 222 Hz

   Measure the synthesized frequency accuracy, and record the results on the Verification Form - Frequency Resolution.

Sine Accuracy (Unbalanced)

Perform this check to verify the accuracy of the sine wave output level from the Unbalanced output connector.

1. Initialize the Model 91 by pressing the **SHIFT** and **RESET ALL** key; see table 3-2 for a list of default parameters. Press the **ON/OFF** key to turn on the output.

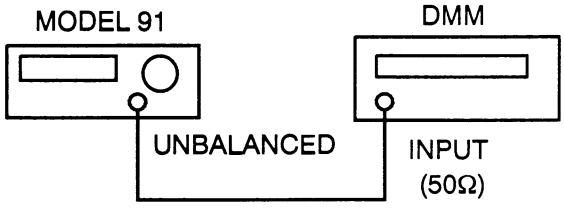


Figure 3-2. Amplitude Accuracy Setup

2. Connect the Model 91 and test equipment as shown in figure 3-2. Remember to terminate the Unbalanced Output into 50Ω.

3. Set the Model 91 to the sine function (**FUNCTION** key). Press the **AMPLITUDE** key and use the keypad to set the amplitude to

   15 Vpp, 1.11 Vpp, 1Vpp,
   100 mVpp.

   Measure the Vrms reading for each amplitude, and record the results on the Verification Form - Sine Accuracy.

Sine Flatness (Unbalanced)

1. Initialize the Model 91 by pressing the **SHIFT** and **RESET ALL** key; see table 3-2 for a list of default parameters. Press the **ON/OFF** key to turn on the output.

2. Connect the Model 91 and test equipment as shown in figure 3-3. Remember to terminate the Unbalanced Output into 50Ω

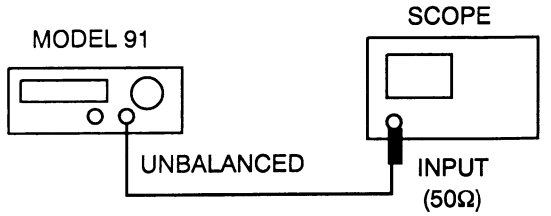


Figure 3-3. Waveforms/Sweep Setup

3. Set the Model 91 to the sine function (**FUNCTION** key). Press the **AMPLITUDE** key and use the keypad to set the amplitude to 10 Vpp. Measure the peak to peak amplitude, and record the results on the Verification Form - Sine Flatness, 1kHz. Press the **FREQ/PER** key and use the keypad to set the frequency to each of the following:

   100 kHz, 1MHz, 16 MHz, 20 MHz.

   At each frequency, measure and record the reading on the Verification Form - Sine Flatness. The actual limits depend on the 1kHz measurement.

Sine Wave Accuracy (Balanced)

1. Initialize the Model 91 by pressing the **SHIFT** and **RESET ALL** key; see table 3-2 for a list of default parameters. Press the **ON/OFF** key to turn on the output.

3. Set the Model 91 to the sine function (**FUNCTION** key). Connect the Balanced Output to the DMM. Repeatedly press the **SHIFT** and **SELECT** keys until the BAL and 135Ω indicators are lit. Press the **AMPLITUDE** key and use the keypad to set the amplitude to each of the following amplitudes.

   15 Vpp, 1Vpp, 100 mVpp.

   Measure the Vrms between the center tap and each leg of the load; figure 3-4. Add the two measurements together and record the results on the Verification Form - Sine Accuracy (Balanced).

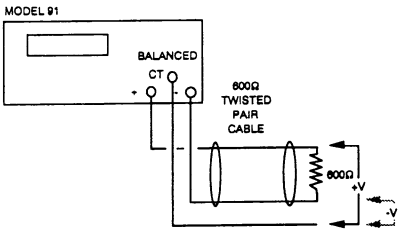


Figure 3-4. Balanced Setup

Sine Wave Purity

1. Initialize the Model 91 by pressing the **SHIFT** and **RESET ALL** key; see table 3-2 for a list of default parameters. Press the **ON/OFF** key to turn on the output.

2. Connect the Model 91 and test equipment as shown in figure 3-5. Be sure to terminate the Unbalanced output with a 50Ω termination. Verify the Sine function is selected.

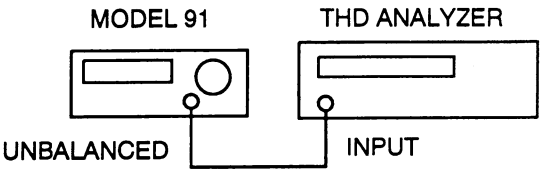


Figure 3-5. Sine Purity Setup

3. Press the **AMPLITUDE** key and use the keypad to set the amplitude to 10 Vpp. Press the **FREQ/PER** key and use the keypad to set the frequency to 2kHz.

   Measure the sine distortion in dB, and record the results on the Verification Form - Sine Wave Purity.

4. Set the frequency to 100 kHz, measure the sine distortion, and record the results on the Verification Form - Sine Purity.

Sine Harmonic Distortion

1. Initialize the Model 91 by pressing the **SHIFT** and **RESET ALL** key; see table 3-2 for a list of default parameters. Press the **ON/OFF** key to turn on the output.

2. Connect the Model 91's Unbalanced Output to the spectrum analyzer. This spectrum analyzer has a 50Ω input impedance, therefore the Model 91's output does not need to terminated. Verify the Sine function is selected.

3. Press the **AMPLITUDE** key and use the keypad to set the amplitude to 10 Vpp. Press the **FREQ/PER** key and use the keypad to set the frequency to 1MHz.

4. Measure the harmonic distortion in dBc, and record the results on the Verification Form - Sine Wave Harmonic Distortion. Repeat this step for 6MHz and 20 MHz.

Triangle Wave Accuracy (Unbalanced)

1. Initialize the Model 91 by pressing the **SHIFT** and **RESET ALL** key; see table 3-2 for a list of default parameters. Press the **ON/OFF** key to turn on the output.
2. Connect the Model 91 and test equipment as shown in figure 3-3 for this measurement. Remember to terminate the Unbalanced Output into 50Ω.
3. Press the **FUNCTION** key and select the Triangle wave. Verify the scope displays the triangle wave. Next connect the Unbalanced Output to the DMM. Press the **AMPLITUDE** key and use the keypad to set the amplitude to 10 Vpp. Measure the Vrms reading, and record the results on the Verification Form - Triangle Accuracy.

Square Wave Accuracy (Unbalanced)

1. Initialize the Model 91 by pressing the **SHIFT** and **RESET ALL** key; see table 3-2 for a list of default parameters. Press the **ON/OFF** key to turn on the output.
2. Connect the Model 91 and test equipment as shown in figure 3-3 for this measurement. Remember to terminate the Unbalanced Output into 50Ω.
3. Press the **FUNCTION** key and select the square wave. Verify the scope displays the square wave. Next connect the Unbalanced Output to the DMM. Press the **AMPLITUDE** key and use the keypad to set the amplitude to 10 Vpp. Measure the Vrms reading, and record the results on the Verification Form - Square Accuracy.

Square/Sync Waveform Characteristics

Perform this test to verify the square wave rise and fall times, square wave aberrations, sync rise and fall times, and sync amplitude.

1. Initialize the Model 91 by pressing the **SHIFT** and **RESET ALL** key; see table 3-2 for a list of default parameters. Press the **ON/OFF** key to turn on the output.
2. Connect the Model 91 and test equipment as shown in figure 3-3 for this measurement. Remember to terminate the Unbalanced Output into 50Ω.
3. Press the **FUNCTION** key and select the square wave Press the **FREQ/PER** keys and use the keypad to set the frequency to 2MHz. Press the **AMPLITUDE** key and use the keypad to set the amplitude to 10 Vpp.
4. Measure the Square wave rise time and record the value on the Verification Form - Square/Sync Waveform. Measure the Square wave fall time and record the value on the Verification Form - Square/Sync Waveform. Measure the Square wave aberrations and record the value on the Verification Form - Square/Sync Waveform.
5. Connect the Sync Out to the scope input connector. Measure the Sync wave rise time and record the value on the Verification Form - Square/Sync Waveform. Measure the Sync wave fall time and record the value on the Verification Form - Square/Sync Waveform. Measure the Sync wave amplitude and record the value on the Verification Form - Square/Sync Waveform.

Pulse Amplitude Accuracy

1. Initialize the Model 91 by pressing the **SHIFT** and **RESET ALL** key; see table 3-2 for a list of default parameters.
2. Connect the Model 91 and test equipment as shown in figure 3-6.

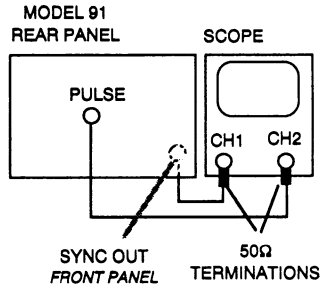


Figure 3-6. Pulse Measurements Setup

3. Select the rear panel PULSE OUT by pressing the **PULSE SETUP** key until REAR OUTPUTS appears on the display. Rotate the Knob until REAR OUTPUTS ON appears.
4. Select the rear outputs sync. Press the **SYNC** key until SYNC REAR appears on the unit's display.
5. Press the **FUNCTION** key and select single pulse.
6. Select the TTL level by pressing the **PULSE SETUP** key until PULSE appears on the display. Rotate the Knob until PULSE TTL appears. TTL is the default.
7. Connect the PULSE OUT to Channel 2 on the Scope. Measure the levels, and record the result on the Verification Form - Pulse Amplitude Accuracy.

Connect the PULSE OUT to channel 2 on the Scope. Measure the levels, and record the result on the Verification Form - Pulse Amplitude Accuracy.

8. Select the CMOS level by pressing the **PULSE SETUP** key until PULSE appears on the display. Rotate the Knob until PULSE CMOS appears. Perform step 6 and record the result on the form.

9. Select the +ECL level by pressing the **PULSE** key until PULSE appears on the display. Rotate the Knob until PULSE +ECL appears. Perform step 6 and record the result on the form.

10. Select the -ECL level by pressing the **PULSE SETUP key** until PULSE appears on the display. Rotate the Knob until PULSE -ECL appears. Perform step 6 and record the result on the form.

Pulse Width

1. Initialize the Model 91 by pressing the **SHIFT** and **RESET ALL** key; see table 3-2 for a list of default parameters.

2. Connect the Model 91 and test equipment as shown in figure 3-6.

3. Select the rear panel PULSE OUT by pressing the **PULSE SETUP** key until REAR OUTPUTS appears on the display. Rotate the Knob until REAR OUTPUTS ON appears.

4. Select the rear outputs sync. Press the **SYNC** key until SYNC REAR appears on the unit's display.

5. Select the TTL level by pressing the **PULSE SETUP** key until PULSE appears on the display. Rotate the Knob until PULSE TTL appears. TTL is the default.

6. Press the **FUNCTION** key and select single pulse.

7. Press the **WIDTH** key Use the keypad to set the pulse width to 15 ns. Record the results on the form (Verification Form - Pulse Width). Then set the width to each of the following values and record the results on the Verification Form - Pulse Width.

400 ns	410 ns	420 ns
430 ns	500 ns	505 ns

Note

Pulse Width is measured from the 50% voltage level on the leading edge of the pulse to the 50% voltage level on the trailing edge of the pulse.

Pulse Delay

1. Initialize the Model 91 by pressing the **SHIFT** and **RESET ALL** key; see table 3-2 for a list of default parameters.

2. Connect the Model 91 and test equipment (as shown in figure 3-6).

3. Press the **FREQ/PER** key and use the keypad to set the frequency to 1MHz. Press the **WIDTH** key and use the keypad to set the pulse width to 10 ns.

4. Select the rear panel PULSE OUT by pressing the **PULSE SETUP** key until REAR OUTPUTS appears on the display. Rotate the Knob until REAR OUTPUTS ON appears.

5. Select the rear outputs sync. Press the **SYNC** key until SYNC REAR appears on the unit's display.

6. Select the TTL level by pressing the **PULSE SETUP** key until PULSE appears on the display. Rotate the Knob until PULSE TTL appears. TTL is the default.

7. Press the **FUNCTION** key and select delayed pulse.

8. Press the **DELAY** key Use the keypad to set the pulse delay 15 ns. Take the measurement and record the results on the Verification Form - Pulse Delay. Next set the pulse width to 100 ns. Then set the pulse delay to each of the following value, and take and record the results on the Verification Form - Pulse Delay.

400 ns	410 ns	420 ns
430 ns	500 ns	505 ns

Note

Pulse Delay is measured from the 50% voltage level on the leading edge of the sync pulse to the 50% voltage level on the rising edge of the pulse output.

Double Pulse

1. Initialize the Model 91 by pressing the **SHIFT** and **RESET ALL** key; see table 3-2 for a list of default parameters.

2. Connect the Model 91 and test equipment (as shown in figure 3-6).

3. Press the **FREQ/PER** key and use the keypad to set the frequency to 1MHz. Press the **WIDTH** key

and use the keypad to set the pulse width to 100 ns.

4. Select the rear panel PULSE OUT by pressing the **PULSE SETUP** key until REAR OUTPUTS appears on the display. Rotate the Knob until REAR OUTPUTS ON appears.

5. Select the rear output sync. Press the **SYNC** key until SYNC REAR appears on the unit's display.

6. Select the TTL level by pressing the **PULSE SETUP** key until PULSE appears on the display. Rotate the Knob until PULSE TTL appears. TTL is the default.

7. Press the **FUNCTION** key and select double pulse.

8. Press the **DELAY** key and use the keypad to set the position of the second pulse to 500 ns (the default). Take the measurement and record the results on the Verification Form - Double Pulse.

Note

Double Pulse is measured from the 50% voltage level on the leading edge of the sync pulse to the 50% voltage level on the rising edge of the second Pulse output.

Then, press the **DELAY** key and use the keypad to set the position of the second pulse to 505 ns. Take the measurement and record the results on the Verification Form - Double Pulse.

Pulse Rise/Fall and Aberrations

Perform this test to verify the rise-time, fall-time, overshoot, and undershoot of the pulse and sync outputs.

1. Initialize the Model 91 by pressing the **SHIFT** and **RESET ALL** key; see table 3-2 for a list of default parameters.

2. Connect the Model 91 and test equipment (as shown in figure 3-6).

3. Select the rear panel PULSE OUT by pressing the **PULSE SETUP key** until REAR OUTPUTS appears on the display. Rotate the Knob until REAR OUTPUTS ON appears.

4. Select the rear output sync signal. Press the **SYNC** key until SYNC REAR appears on the unit's display.

5. Select the TTL level by pressing the **PULSE SETUP** key until PULSE appears on the display. Rotate the Knob until PULSE TTL appears. TTL is the default.

6. Press the **FUNCTION** key and select single pulse.

7. Press the **WIDTH** key. Use the keypad to set the pulse width to 100 ns. Press the **FREQ/PER** key and use the keypad to set the frequency to 5MHz.

8. Connect the Pulse Output to the scope. Take the following measurements and record the results on the Verification Form - Pulse Rise/Fall and Aberrations.

   Pulse Output Rise Time
   Pulse Output Fall Time
   Positive Aberration on the Pulse Output
   Negative Aberrations on the Pulse Output

   Connect the Sync Output to the scope. Take the following measurements and record the result on the Verification Form - Pulse Rise/Fall and Aberrations.

   Sync Output Rise Time
   Sync Output Fall Time
   Sync Output Amplitude.

DC Output and Attenuator Accuracy

1. Initialize the Model 91 by pressing the **SHIFT** and **RESET ALL** key; see table 3-2 for a list of default parameters. Press the **ON/OFF** key to turn on the output.

2. Connect the Model 91's Unbalanced Output to the DMM (set for Vdc) as shown in figure 3-2. Terminate the Unbalanced Output into 50Ω.

3. Press the **FUNCTION** key and select the DC function. Press the **OFFSET** key and use keypad to set the dc voltage to +7.5 Vdc. Measure the dc output and record the data on the Verification Form - DC Output. Repeat this process for 0Vdc and -7.5 Vdc.

VCG/FM

Perform this check to verify the frequency accuracy of the Model 91 when its frequency is controlled by and external voltage.

1. Initialize the Model 91 by pressing the **SHIFT** and **RESET ALL** key; see table 3-2 for a list of default parameters.

2. Connect the Model 91 and test equipment as shown in figure 3-7.

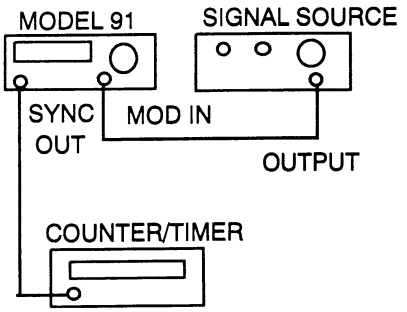


Figure 3-7. VCG/FM Setup

3. Press the **FREQ/PER** key and use the knob or keypad to set the frequency to 100 kHz. The default mode is Continuous.

   Press the **MODE** key and select the FM mode; this locks the Model 91 on the 200 kHz range. Press the **FREQ/PER** key and use the knob or keypad to set the frequency to 200 Hz (1/1000 of the 200 kHz range).

   Measure the Center Frequency and record the data on the Verification Form - VCG/FM.

4. Apply a +5 Vdc level to the MOD IN connector. Measure the Deviation Frequency and record the results on the Verification Form - VCG/FM.

Triggered Mode

1. Initialize the Model 91 by pressing the **SHIFT** and **RESET ALL** key; see table 3-2 for a list of default parameters. Press the **ON/OFF** key to turn on the output.

2. Connect the Model 91 and test equipment as shown in figure 3-8.

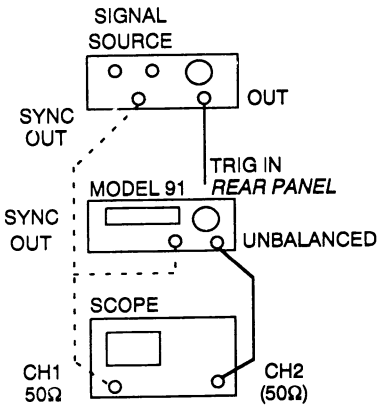


Figure 3-8. Trigger Measurement Setup

3. Set the Model 91 to the (Internal) Triggered mode (**MODE** key). Internal trigger is the default. Verify the scope displays an internally triggered 5Vpp sine wave. Record Yes or No on the Verification Form - Triggered Mode Setting, Internal Triggered Sine Wave.

4. Set the Model 91 to the External Triggered mode. Press the **TRIG SETUP** key until the unit displays TRIG SOURCE, and rotate the Knob until the unit displays TRIG SOURCE EXT. Set the external trigger source for a 100 Hz TTL square wave. Connect the signal source output to the TRIG IN connector on the unit's rear panel.

5. Verify the scope displays an externally triggered 5Vpp sine wave. Record Yes or No on the Verification Form - Triggered Mode Setting, External Triggered Sine Wave.

Trigger Level Test

Perform this test to perform a functional test of the trigger slope control and verify the trigger level accuracy.

1. Initialize the Model 91 by pressing the **SHIFT** and **RESET ALL** key; see table 3-2 for a list of default parameters.

2. Connect the Model 91 and test equipment as shown in figure 3-8 except replace the signal source with a ±5 V dc source.

3. Select the rear panel PULSE OUT by pressing the **PULSE** key until REAR OUTPUTS appears on the display. Rotate the Knob until REAR OUTPUTS ON appears.

4. Select the rear output sync. Press the **SYNC** key until SYNC REAR appears on the unit's display.

5. Select the TTL level by pressing the **PULSE** key until PULSE appears on the display. Rotate the Knob until PULSE TTL appears. TTL is the default.

6. Press the **FUNCTION** key and select external width (E.W.).

7. Press the **TRIG SETUP** key until TRIG SLOPE appears then use the knob to select TRIG SLOPE POS. Again press the **TRIG SETUP** key until TRIG LEVEL appears, and use the knob or keypad to set the level to +5V. Gradually increase the dc trigger voltage starting at 0V. At +5V the External Width output should change states. Note and record the level on the Verification Form - Trigger Level, Positive Slope +5V. Setup the

slope and levels to as listed, and record the results on the Verification Form. When checking positive slopes, start the trigger voltage below the trigger level and gradually increase the level.

For negative slopes, start the trigger voltage above the trigger level and gradually increase the level.

Pos Slope 0V level
Pos Slope -5V level
Neg Slope +5V level
Neg Slope 0V level
Neg Slope -5V level

Gated Mode

1. Initialize the Model 91 by pressing the **SHIFT** and **RESET ALL** key; see table 3-2 for a list of default parameters. Press the **ON/OFF** key to turn on the output.

2. Connect the Model 91 and test equipment as shown in figure 3-8. Connect the Model 91 SYNC OUT to the scope's trigger input.

3. Set the Model 91 to the (Internal) Gate mode (**MODE** key). Internal gate is the default. Verify the scope displays an internally gated 5Vpp sine wave. Record Yes or No on the Verification Form - Gate Mode Setting Internal Gated Sine Wave.

4. Set the Model 91 to the External Gate mode. Press the **TRIG SETUP** key until the unit displays TRIG SOURCE, and rotate the Knob until the unit displays TRIG SOURCE EXT. Set the external source for a 100 Hz TTL square wave. Connect the signal source output to the TRIG IN connector on the rear panel.

5. Verify the scope displays an externally gated 5Vpp sine wave. Record Yes or No on the Verification Form - Gate Mode Setting External Gated Sine Wave.

Burst Mode

1. Initialize the Model 91 by pressing the **SHIFT** and **RESET ALL** key; see table 3-2 for a list of default parameters. Press the **ON/OFF** key to turn on the output.

2. Connect the Model 91 and test equipment as shown in figure 3-8.

3. Set the Model 91 to the (Internal) Burst mode (**MODE** key). Internal burst is the default. Verify the scope displays an internal triggered burst of 5, 5Vpp sine waves. Record Yes or No on the Verification Form - Burst Mode Setting Internal Burst Sine Wave.

4. Set the Model 91 to the external triggered burst mode. Press the **TRIG SETUP** key until the unit displays TRIG SOURCE, and rotate the Knob until the unit displays TRIG SOURCE EXT. Set the signal source for a 100 Hz TTL square wave.

   Connect the signal source to the TRIG IN connector on the rear panel. Synchronize the scope off the signal source.

5. Verify the scope displays an externally triggered burst of 5, 5Vpp sine waves. Record yes or No on the Verification Form - Burst Mode Setting External Gated Sine Wave.

Amplitude Modulation

1. Initialize the Model 91 by pressing the **SHIFT** and **RESET ALL** key; see table 3-2 for a list of default parameters. Press the **ON/OFF** key to turn on the output.

2. Connect the Model 91 and test equipment as shown in figure 3-9.

3. Set the signal generator for a 1kHz, 2.7 Vpp (open circuit) sine wave. Set Model 91 for 100 kHz (**FREQ/PER** key and knob/keypad) and the AM mode (**MODE** key). Verify the scope displays normal amplitude modulation of approximately 100%. Record Yes or No on the Verification Form - Amplitude Modulation Setting 100% AM..

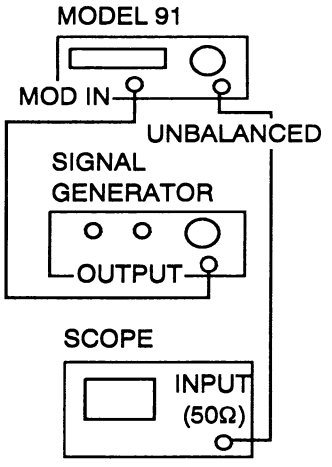


Figure 3-9. AM Setup

Suppressed Carrier

1. Initialize the Model 91 by pressing the **SHIFT** and **RESET ALL** key; see table 3-2 for a list of default parameters. Press the **ON/OFF** key to turn on the output.

2. Connect the Model 91 and test equipment as shown in figure 3-9.

3. Set Model 91 to the SCM mode (MODE key). With the MOD IN signal disconnected, verify the scope displays no output.

4. Set the signal source for +2Vdc. Connect the signal source output to the Model 91 MOD IN. Verify the scope displays a 4Vpp sine wave. Record Yes or No) on the Verification Form - Suppressed Carrier Modulation Setting 4Vpp SCM.

Sweep

1. Initialize the Model 91 by pressing the **SHIFT** and **RESET ALL** key; see table 3-2 for a list of default parameters. Press the **ON/OFF** key to turn on the output.

2. Connect the Model 91 and test equipment as shown in figure 3-10. Connect the Model 91's SYNC OUT to the scope's trigger input.

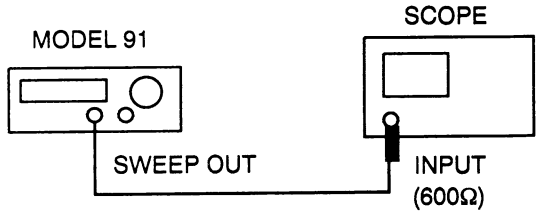


Figure 3-10. Sweep Out Setup

3. Press the **MODE** key until the SWEEP indicator is lit. Press the **SWEEP MODE** key until the unit displays Continuous Sweep. Verify the scope displays a sweep output (1kHz to 10 kHz, 1 second sweep), and record the results on the Verification Form - Sweep Setting Sweep Output.

4. Connect the Model 91's SWEEP OUT to the scope input. Verify the scope displays a 1 second sweep ramp (600Ω impedance), and record the results on the Verification Form - Sweep Setting Sweep Output.

Symmetry

Perform this check to verify the accuracy of the Model 91's fixed and variable symmetry.

1. Initialize the Model 91 by pressing the **SHIFT** and **RESET ALL** key; see table 3-2 for a list of default parameters.

2. Connect the Model 91 and test equipment as shown in figure 3-3 to perform this procedure.

3. Press the **FREQ/PER** key and use the knob or keypad to set the frequency to 1kHz.

4. Measure the symmetry of the square wave at the Sync Output. Record the results on the Verification Form - Symmetry, 50%.

5. Setup the symmetry using the **SHIFT** and **SYMMETRY** keys and knob/keypad:
   10% 90%
   Measure the symmetry accuracy for each setting. The specified value represents the time in µs for the negative half of the cycle. Record the data on the Verification Form - Symmetry.

External Lock and Phase Shift

1. Initialize the Model 91 by pressing the **SHIFT** and **RESET ALL** key; see table 3-2 for a list of default parameters. Press the **ON/OFF** key to turn on the output.

2. Connect the Model 91 and test equipment as shown in figure 3-11, except leave the signal source disconnected.

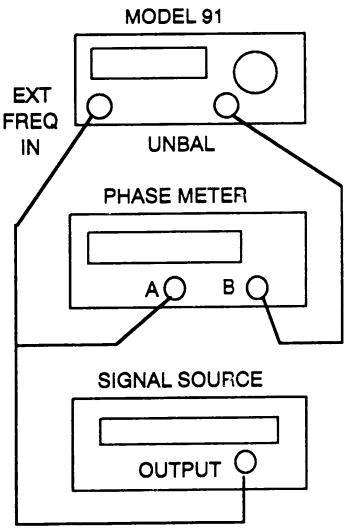


Figure 3-11. External Lock Setup

3. Set the Model 91 to external lock (**LOCK SOURCE** key). Verify the Model 91 displays EXTLOC, the UNLOCK indicator flashes, and EXT indicator remains lit. Record (Record Yes or No) the results on the form (Verification Form - External Lock Setting Source Disconnected).

4. Set the signal source for a 10 kHz, 5Vpp sine wave. Connect the signal source to the Model 91 EXT FREQ IN connector. Verify the Model 91 displays EXTLOC 10.00 KHZ (approximate reading), UNLOCK indicator remains off, and the EXT indicator remains lit. Record (Record Yes or No) the results on the form (Verification Form - External Lock Setting Source Connected). The Model 91 automatically changes it frequency to match the frequency of the external source.

5. Set the Model 91 phase angle as per the "Setting" on the Verification Form. Measure the phase angle at each step. Measure the phase angle as per the Specified Value, and record results on the form.

Front Panel

Did the annunciators and the display perform correctly during the Verification Procedure? Record the results on the Verification Form - Front Panel Display/Annunciators.

Option 001 - High Frequency Stability Reference

Perform the following checks only if the Model 91 contains an Option 001.

1. Turn the Model 91 Power on.

2. Connect the Model 91 REF OUT on the rear panel to a Counter/Timer. The counter should be referenced to a highly accurate standard such as WWV.

3. Verify the REF OUT frequency measures between 10 MHz ±1ppm (9.999,990 MHz to 10.000,010 MHz). Record the results on the Verification Form - Option 001, REF OUT.

4. Connect the Model 91 REF IN on the rear panel to a signal source. Set the signal source to 10.001 MHz, 1Vrms sine wave (always properly terminate the signal source). Measure the REF OUT frequency. The REF OUT frequency must measure ±2Hz of the signal source frequency. Record the results on the Verification Form - Option 001, External Reference.

VERIFICATION FORM

Date _____ Technician _____ Serial No _____

Frequency Ranges

Synthesized

Settings	Data Record	Specified Value
20 MHz	_____ MHz	19.9998 to 20.0002 MHz
2 MHz	_____ MHz	1.99998 to 2.00002 MHz
200 kHz	_____ kHz	199.998 to 200.002 kHz
20 kHz	_____ kHz	19.9998 to 20.0002 kHz
2 kHz	_____ kHz	1.99998 to 2.00002 kHz
200 Hz	_____ Hz	199.998 to 200.002 Hz
20 Hz	_____ Hz	19.9998 to 20.0002 Hz

Unlocked FM

Settings	Data Record	Specified Value
20 MHz	_____ MHz	19.4 to 20.6 MHz
2 MHz	_____ MHz	1.94 to 2.06 MHz
200 kHz	_____ kHz	194 to 206 kHz
20 kHz	_____ kHz	19.4 to 20.6 kHz
2 kHz	_____ kHz	1.94 to 2.06 kHz
200 Hz	_____ Hz	194 to 206 Hz
20.00 Hz	_____ Hz	19.4 to 20.6 Hz

Unlocked Continuous

Settings	Data Record	Specified Value
2.000 Hz	_____ Hz	1.94 to 20.6 Hz
200.0 mHz	_____ Hz	194 to 206 mHz
20.00 mHz	_____ mHz	19.4 to 20.6 mHz

Frequency Resolution

Settings	Data Record	Specified Value
1999 Hz	_____ Hz	1998.98 to 1999.02 Hz
1888 Hz	_____ Hz	1887.98 to 1888.02 Hz
1777 Hz	_____ Hz	1776.98 to 1777.02 Hz
1666 Hz	_____ Hz	1665.98 to 1666.02 Hz
1555 Hz	_____ Hz	1554.98 to 1555.02 Hz
1444 Hz	_____ Hz	1443.99 to 1444.01 Hz
1333 Hz	_____ Hz	1332.99 to 1333.01 Hz
1222 Hz	_____ Hz	1221.99 to 1222.01 Hz
1111 Hz	_____ Hz	1110.99 to 1111.01 Hz
999 Hz	_____ Hz	998.99 to 999.01 Hz
888 Hz	_____ Hz	887.991 to 888.009 Hz
777 Hz	_____ Hz	776.992 to 777.008 Hz
666 Hz	_____ Hz	665.993 to 666.007 Hz
555 Hz	_____ Hz	554.994 to 555.006 Hz
444 Hz	_____ Hz	443.996 to 333.003 Hz
333 Hz	_____ Hz	332.997 to 333.003 Hz
222 Hz	_____ Hz	221.998 to 222.002 Hz

VERIFICATION FORM (CONTINUED)

Sine Wave Accuracy

Setting	Data Record	Specified Value
15.0 Vpp	_____ Vrms	5.187 to 5.419 Vrms
1.11 Vpp	_____ Vrms	0.3746 to 0.4102 Vrms
1Vpp	_____ Vrms	0.3445 to 0.3627 Vrms
100 m Vpp	_____ Vrms	36.9 to 37.1 mVrms

Sine Flatness

Setting	Data Record	Specified Value
1 kHz	_____ Vpp	9.832 to 10.168 Vpp
100 kHz	_____ Vpp	0.9727 x (1kHz Vpp) to 1.0280 x (1kHz Vpp)
1MHz	_____ Vpp	0.9727 x (1kHz Vpp) to 1.0280 x (1kHz Vpp)
16 MHz	_____ Vpp	0.9332 x (1kHz Vpp) to 1.0715 x (1kHz Vpp)
20 MHz	_____ Vpp	0.9332 x (1kHz Vpp) to 1.0715 x (1kHz Vpp)

Sine Wave Accuracy (Balanced)

Setting	Data Record	Specified Value
15 Vpp	_____ Vrms	5.187 to 5.419 Vrms
1Vpp	_____ Vrms	0.3445 to 0.3627 Vrms
100 mVpp	_____ Vrms	36.9 to 37.1 mVrms

Sine Wave Purity

Setting	Data Record	Specified Value
THD at 2kHz	_____ dB	≤ – 46 dB (0.5%)
THD at 100 kHz	_____ dB	≤ – 46 dB (0.5%)

Sine Harmonic Distortion

Setting	Data Record	Specified Value
1MHz	_____ dBc	≤– 40 dBc
6MHz	_____ dBc	≤– 30 dBc
20 MHz	_____ dBc	≤– 25 dBc

Triangle Wave Accuracy (Unbalanced)

Setting	Data Record	Specified Value
10 Vpp	_____ Vrms	4.23 to 4.43 Vrms

Square Wave Accuracy (Unbalanced)

Setting	Data Record	Specified Value
10 Vpp	_____ Vrms	4.89 to 5.11 Vrms

Square Wave/Sync Out Transition Time

Unbalanced Output

Setting	Data Record	Specified Value
Rise Time	_____ ns	< 9ns
Fall Time	_____ ns	< 9 ns
Pos. Trans. % aberration	_____ mVpp	< 520 mVpp
Neg. Trans. % aberration	_____ mVpp	< 520 mVpp

VERIFICATION FORM (CONTINUED)

Sync Out Setting	Data Record	Specified Value
Rise Time	_____ ns	< 13 ns
Fall Time	_____ ns	< 13 ns
Amplitude	_____ Vpp	2Vpp to 4Vpp

Pulse Amplitude Accuracy

Pulse Out Setting	Data Record	Specified Value
TTL Upper Level	_____ Vdc	+2.425 to +2.575 Vdc
TTL Lower Level	_____ Vdc	–0.025 to +0.025 Vdc
CMOS Upper Level	_____ Vdc	+3.895 to +4.105 Vdc
CMOS Lower Level	_____ Vdc	–0.025 to +0.025 Vdc
+ECL Upper Level	_____ Vdc	+3.993 to +4.207 Vdc
+ECL Lower Level	_____ Vdc	+3.111 to +3.289 Vdc
–ECL Upper Level	_____ Vdc	–0.882 to –0.918 Vdc
–ECL Lower Level	_____ Vdc	–1.764 to –1.836 Vdc

Pulse Out Setting	Data Record	Specified Value
TTL Upper Level	_____ Vdc	+2.425 to +2.575 Vdc
TTL Lower Level	_____ Vdc	–0.025 to +0.025 Vdc
CMOS Upper Level	_____ Vdc	+3.895 to +4.105 Vdc
CMOS Lower Level	_____ Vdc	–0.025 to +0.025 Vdc
+ECL Upper Level	_____ Vdc	+3.993 to +4.207 Vdc
+ECL Lower Level	_____ Vdc	+3.111 to +3.289 Vdc
–ECL Upper Level	_____ Vdc	–0.882 to –0.918 Vdc
–ECL Lower Level	_____ Vdc	–1.764 to –1.836 Vdc

Pulse Width

Setting	Data Record	Specified Value
15 ns	_____ ns	5.075 to 20.075 ns
400 ns	_____ ns	393 to 409 ns
410 ns	_____ ns	402.95 to 417.05 ns
420 ns	_____ ns	412.9 to 427.1 ns
430 ns	_____ ns	422.85 to 437.15 ns
500 ns	_____ ns	492.5 to 507.5 ns
505 ns	_____ ns	497.5 to 512.5 ns

Pulse Delay

Setting	Data Record	Specified Value
15 ns	_____ ns	5.075 to 20.075 ns
400 ns	_____ ns	393 to 409 ns
410 ns	_____ ns	402.95 to 417.05 ns
420 ns	_____ ns	412.9 to 427.1 ns
430 ns	_____ ns	422.85 to 437.15 ns
500 ns	_____ ns	492.5 to 507.5 ns
505 ns	_____ ns	497.5 to 512.5 ns

VERIFICATION FORM (CONTINUED)

Double Pulse

Setting	Data Record	Specified Value
500 ns	_____ ns	492.5 to 507.5 ns
505 ns	_____ ns	497.5 to 512.5 ns

Pulse Rise/Fall and Aberrations

Pulse Out

Setting	Data Record	Specified Value
Rise Time	_____ ns	≤3ns
Fall Time	_____ ns	≤3ns
Positive Aberrations	_____ V	≤0.2V
Negative Aberrations	_____ V	≤0.2V

Sync Out

Setting	Data Record	Specified Value
Rise Time	_____ ns	≤6ns
Fall Time	_____ ns	≤6ns
Amplitude	_____ Vpp	2 to 4 Vpp

DC Output/Attenuator Accuracy

Setting	Data Record	Specified Value
+7.499V	_____ Vdc	+7.348 to +7.652 Vdc
0V	_____ Vdc	-0.001 to +0.001 Vdc
-7.499V	_____ Vdc	-7.652 to -7.348 Vdc

VCG/FM

Setting	Data Record	Specified Value
1/1000 Frequency	_____ Hz	176 to 226 Hz
Deviation Frequency	_____ Hz	95 to 105 kHz

Triggered Mode

Setting	Data Record	Specified Value
Internal Triggered Sine Wave	_____	Record: Yes or No
External Triggered Sine Wave	_____	Record: Yes or No

Trigger Level Test

Setting	Data Record	Specified Value
Pos Slope +5V	_____ V	+4.5 to +5.5 V
Pos Slope 0V	_____ V	-250 to +250 mV
Pos Slope -5V	_____ V	-5.5 to -4.5V
Neg Slope +5V	_____ V	+5.5 to +4.5V
Neg Slope 0V	_____ V	+250 to -250 mV
Neg Slope -5V	_____ V	-4.5 to -5.5V

Gate Mode

Setting	Data Record	Specified Value
Internal Gated Sine Wave	_____	Record: Yes or No
External Gated Sine Wave	_____	Record: Yes or No

VERIFICATION FORM (CONTINUED)

Burst Mode

Setting	Data Record	Specified Value
Internal Burst Sine Wave	_____	Record: Yes or No
External Burst Sine Wave	_____	Record: Yes or No

Amplitude Modulation

Setting	Data Record	Specified Value
~100% AM	_____	Record: Yes or No

Suppressed Carrier Modulation

Setting	Data Record	Specified Value
~4Vpp SCM	_____	Record: Yes or No

Sweep

Setting	Data Record	Specified Value
Sweep Output	_____	Record: Yes or No
Sweep Ramp	_____ s	0.99 to 1.01s

Symmetry

Settings	Data Record	Specified Value
50% Symmetry	_____ %	49.9 to 50.1%
10% Symmetry	_____ %	9.9 to 10.1 %
90% Symmetry	_____ %	89.1 to 90.9 %

External Lock

Setting	Data Record	Specified Value
Source Disconnected	_____	Record: Yes or No
Source Connected	_____	Record: Yes or No

Phase Angle

Setting	Data Record	Specified Value
0° Phase	_____ °	-4° to +4°
+90° Phase	_____ °	+86° to +94°
+180° Phase	_____ °	+176° to +184°
-90° Phase	_____ °	-94° to -86°
-180° Phase	_____ °	-184° to -176°

Front Panel

	Data Record	Specified Value
Display/Annunciators	_____	Record: Yes or No

Option 001 - High Frequency Stability Reference

Setting	Data Record	Specified Value
Ref Out	_____ MHz	9.999,990 MHz to 10.000,010MHz
External Reference	_____ MHz	External Reference frequency ±2%

SECTION 4
CALIBRATION PROCEDURE

4.1 CALIBRATION

Wavetek maintains a factory Customer Service department for customers not possessing the necessary personnel or test equipment to calibrate or repair the instrument. Before returning the instrument, contact the Customer Service Department by calling or writing:

Wavetek San Diego, Inc.
9045 Balboa Ave.
San Diego, CA 92123
Telephone: (619) 279-2200
TWX: (910) 335-2007
FAX (619) 565-9558

The Model 91 provides two calibration methods: AutoCal and Calibrate.

4.1.1 AutoCal

AutoCal (automatic calibration) provides a quick method of calibrating the Model 91 without using external test equipment. AutoCal automatically sets up the instrument and takes internal measurements using internal standards. The Model 91 calculates correction values and stores those values in memory. At powered up, the unit recalls these correction values from its memory for use during operation. Use AutoCal when accuracy is critical, after long term instrument storage, following drastic changes in the environment, or when the operator believes AutoCal is necessary.

4.1.2. Calibration Procedure

The calibration provides a more extensive method of calibration. The Calibration Procedure uses external test equipment and requires opening the instrument and making adjustments. Use the Calibration Procedure when the Model 91 displays **CAL REQUIRED** or **FAILED AUTOCAL**, after repair, Performance Verification failure (section 3), or scheduled routine calibration. Paragraph 4.3 contains the Calibration procedure.

4.2 AUTOCAL PROCEDURE

AutoCal requires no external test equipment. In fact, test equipment can not be connected to any of the input connectors otherwise the AutoCal circuitry could incorrectly calibrate the instrument. Also, disconnect all outputs from the instrument otherwise the sudden changes in the instrument's output waveforms could damage external equipment.

To AutoCal the Model 91, perform the following steps.

1. Turn on the Model 91 and allow it to warm up for 20 minutes. Pressing the **CALIBRATE** key during the 20 minute warm up time displays the countdown time, after the 20 minutes the Model 91 begins AutoCal. Pressing any other key while running the count down timer, aborts AutoCal and returns the instrument to normal operation.

   Remember to remove all input and output connections to the Model 91 before pressing AutoCal.

2. If the unit has been on for more than 20 minutes, press the **CALIBRATE** key (**SHIFT** and **CALIBRATE**) and allow the unit time to complete the AutoCal cycle. While running AutoCal, the Model 91 displays **CALIBRATING**. When completed, the Model 91 displays **AUTOCALIBRATED** and the unit returns to its last setting. If the AutoCal fails, the Model 91 displays an error message which identifies the parameter - ERR (*Keyword*); for example ERR VSINCAL. If this occurs occasionally, try to Calibrate the unit again. Note the error keywords and report the errors when the unit is returned for scheduled maintenance. Refer to paragraph 6.7.6 for a listing of error messages.

4.3 CALIBRATION PROCEDURE

To perform the complete manual calibration procedure follow the steps listed below. This procedure contains a series of steps which the Model 91 guides you through. During this procedure, the Model 91 automatically sets itself to the right conditions. Some calibration steps may require you to make changes using front panel controls.

Table 4-1. Recommended Test Equipment

Test Equipment	Recommended Model
Scope	Tektronix 2465 or equivalent (≥300 MHz bandwidth, 2 vertical inputs, sum and invert channels, internal 50Ω termination.
Distortion Analyzer	Hewlett Packard 8903B or equivalent (20 Hz to 100 kHz bandwidth).
Digital Voltmeter	Fluke 8050A true RMS AC Voltmeter.
Function Generator	Wavetek Model 23 or equivalent.
Frequency Counter	Hewlett Packard 5335A or equivalent (Better than 1ppm accuracy, phase measurement, 9 digit/second resolution, 2ns single shot width providing better than 1° phase resolution at 1MHz.
Phase Meter	Hewlett Packard 3575A or equivalent.
Calibration Cover	Wavetek: 1400-02-5776

NOTE

Use rear panel for all ground connections unless otherwise specified.
All indications and waveforms are referenced to chassis ground unless otherwise specified.

4.3.1 Adjustments

Throughout this procedure are illustrations identifying the adjustments used in the steps. For a detailed look at the adjustment locations, refer to the assembly drawings located in section 7 of this manual. Figure 4-1 shows the individual board locations.

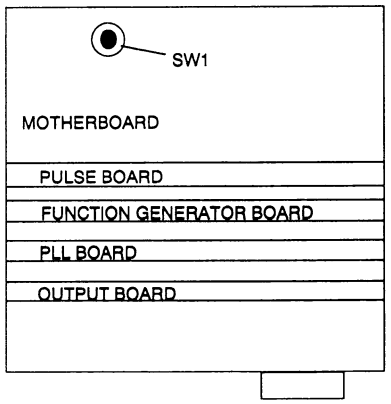


Figure 4-1. Board Locator

4.3.2 Keys

While performing the Calibration Procedure, the following keys have these functions.

CALIBRATE Pressing this key during the Calibration Procedure turns off the Calibration mode.

PARAM RESET During the Calibration Procedure, this key resets all the calibration factors to their default values.

OFFSET During the Calibration Procedure, this key functions as the forward cursor. Pressing the "**OFFSET**" key advances the procedure to the next calibration step.

AMPLITUDE During the Calibration Procedure, this key functions as the reverse cursor. Pressing the "**AMPLITUDE**" key returns the procedure to the previous calibration step.

Knob During the Calibration Procedure, the Knob changes and enters calibration data. In some steps, it alternate between two functions.

Keypad During the Calibration Procedure, the numeric keypad enters calibration data. Use the **ENTER** key to accept data entered using the numeric keypad.

4.3.3 Precalibration Setup

Before beginning calibration, disconnect the Model 91 from its power source and remove five top cover screws. Slide the top cover off, and remove the inner shield. Slide the top cover back on.

Wavetek offers a Calibration Covers, part of Option 004 - Service Kit, which replaces the top cover and inner shield. This cover permits access to the calibration adjustments while stabilizing the unit's internal temperature.

NOTE

Keep the top cover in place during the procedures except when necessary to make an internal adjustment.

WARNING

The Model 91 uses a three-wire power cable. When connected to a grounded AC power receptacle, this cable grounds the instrument front panel and cabinet. Do not use extension cords or AC adapters without a ground.

WARNING

This instrument uses internal batteries that contain more than 0.2 grams of Lithium. Do not charge or short this battery. A hazard of explosion and or contamination exists.

1. Verify the power cable connects the Model 91 to a primary power source. Disconnected all other cables.

2. Set the **POWER** On/Off switch to On.

   When power is first applied, the Model 91 performs a Self-Test which checks the internal battery, mother board memory and storage memory. If the unit passes Self-test, it displays: **WAVETEK MODEL 91**.

4.3.4 Calibration Procedure

Step 1 Initial Steps

1. Allow the unit to warm up 20 minutes. Remove the screws from the top cover; paragraph 6.9. Then slide the top cover back. Press and hold down the internal calibration switch SW1 (figure 4-2) while pressing the **SHIFT** and **CALIBRATE** keys. Slide the cover back on.

2. Verify the Model 91 display reads **WVTK SN XXXXXXXX** or **WVTK SN 0**. Press the **OFFSET** key to step to **USER SN XXXX**. USER SN allows entry of an identification number via the Knob or keypad.

3. When finished, press the **OFFSET** key to advance to **500KHZ REF C150**. Pressing the **OFFSET** key stores the User Number.

Step 2 Adjust Frequency Reference

If calibrating a standard Model 91 (one without Option 001, TCXO Frequency Reference) perform items 1 through 4 of this step. If Option 001 is installed perform items 5 through 7.

1. Connect the test equipment as shown in figure 4-2.

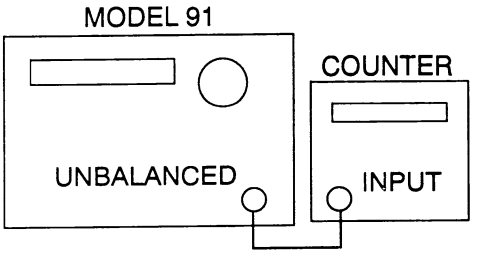


Figure 4-2. Frequency Reference Setup

2. Connect the UNBALANCED Output of the Model 91 to the Counter's input connector. On the Model 91, press the **ON/OF** key to turn on the output.

3. Measure the frequency at the UNBALANCED output connector. Verify the counter reads 500 kHz ±1Hz. If incorrect, slide the cover back, and adjust C150 (see figure 4-3) until the counter reads 500 kHz ± 1Hz. Then slide the cover back on.

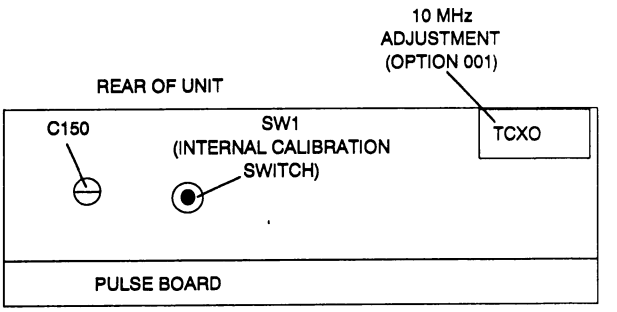


Figure 4-3. Frequency Reference/TCXO Locator

4. When completed, press **OFFSET** key to advance to the next step. The displays reads **R33,97,USINE XXX**.

If the Option 001, TCXO Frequency Reference is installed, perform item 1 of this step and continue on using the following steps.

5. Connect the counter/timer to the Model 91 REF OUT connector, located on the rear panel.

6. Measure the frequency at the REF OUT connector. Verify the counter reads 10 MHz ±2Hz.

   If incorrect, remove the sticker from the TCXO and adjust the trimmer (see figure 4-3) until the counter reads 10 MHz ±2Hz.

   When finished, replace the sticker on the TCXO. Slide the cover on.

7. When completed, press **OFFSET** key to advance to the next step. The displays reads **R33,97,USINE XXX**.

Step 3. Adjust Sine Wave

1. The Model 91 display reads **R33, 97, USINE XXX** where XXX represents the internal value of the VSINE dc control voltage. Connect the test equipment as shown in figure 4-4.

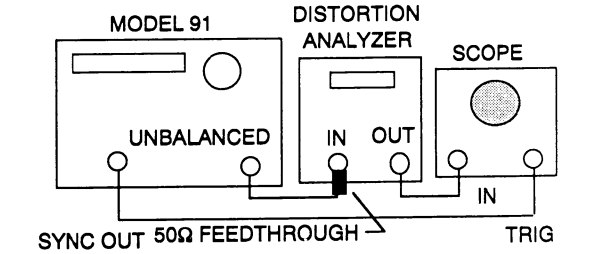


Figure 4-4. Sine Wave Adjust Setup

2. Set the distortion analyzer controls to display the Model 91 output signal Total Harmonic Distortion (THD) in dB.

3. On the Model 91, slowly adjust the **Knob** until the scope displays minimum THD. Verify that reading is better than – 50 dB at 10 kHz.

4. If incorrect, set the scope controls to display the distortion analyzer output. Slide the cover back. Adjust R33 (figure 4-5) until waveform peaks are clearly visible in the residue.

   Adjust R97 (figure 4-5) until the waveform peaks are symmetrical, one above the average value of the residue signal and one below.

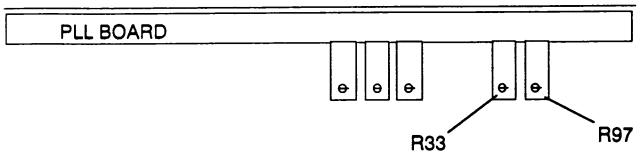


Figure 4-5. R33/R97 Locator

5. Adjust R33 until the peaks disappear into the residue.

6. Observe the overall ripple in the residue displayed on the scope. Turn the **Knob** CW until the waveform peaks are clearly visible in the residue; repeat step 5.

   If the overall ripple decreased, continue turning the **Knob** CW.

   If the overall ripple has increased, turn the **Knob** CCW.

7. Repeat steps 5 and 6 until:

   The amplitude of the overall ripple in the residue signal displayed on the scope is minimum. The THD as measured on the distortion analyzer is better than – 50 dB.

8. Disconnect the test equipment and slide the cover back on.

9. On the Model 91, press the **OFFSET** key to advance to the next step. Verify the display flashes **CALIBRATING** and then indicates **SCM NULL -XXX**.

Step 4. SCM Null

1. The Model 91 displays **SCM NULL -XXX** where -XXX represent the SCM null value.

2. Connect the test equipment as shown in figure 4-6. Set the scope for 50 mV/div (Vdc).

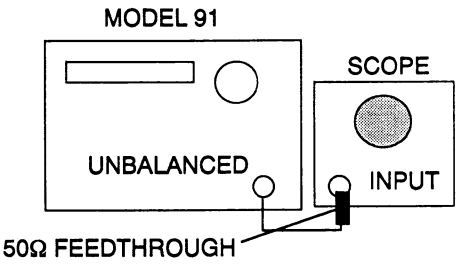


Figure 4-6. SCM Null Setup

3. View the carrier null signal on the scope. If necessary, slide the cover back and adjust R146 (see figure 4-7) to center the scope trace. Then use the **Knob** to adjust for best square wave signal null. Slide the top cover back on.

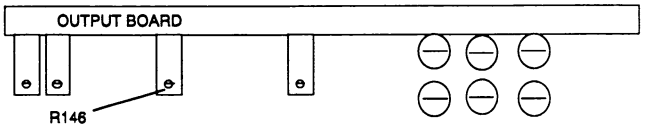


Figure 4-7. R146 Locator

4. Press the **OFFSET** key to step to **TRI NULL R25 2**.

Step 5 Null Triangle

1. The Model 91 display reads **TRI NULL R25 2**. Connect test equipment (DVM set to Vdc) as shown in figure 4-8.

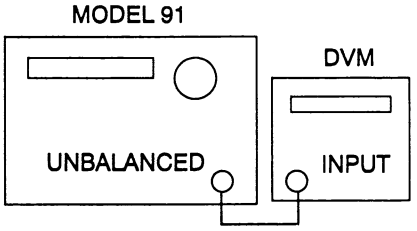


Figure 4-8. Triangle Null Setup

2. The DVM measures the dc offset value of the 2Vpp triangle.

3. Rotate the **Knob** on the Model 91 until display reads **TRI NULL R25 15**. The DVM measures the dc offset value of the 15 Vpp triangle.

4. Use the **Knob** to move between 2 and 15. Slide the cover back, and adjust the Output board's R25 (see figure 4-9) until the dc offset change between 2 and 15 is less than 2mV at both amplitudes. Slide the cover back on.

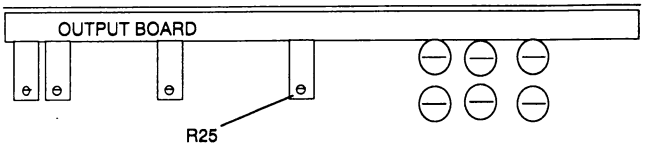


Figure 4-9. R25 Locator

5. Press the **OFFSET** key to advance to the next step. Verify the display flashes **CALIBRATING** and then displays **TRI OFFSET R146**.

Step 6 Adjust Triangle Offset

1. The Model 91 display reads **TRI OFFSET R146**. Leave the test equipment connected as shown in figure 4-8.
2. Slide the cover back, and adjust the Output board's R146 (see figure 4-10) until the DVM reads 0Vdc ±2mVdc of triangle offset. Slide the cover back on.

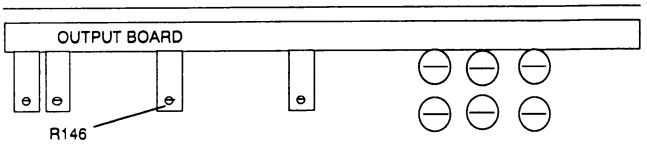


Figure 4-10. R146 Locator

3. Press the **OFFSET** key to advance to the next step. Verify the display flashes **CALIBRATING** then displays **SINE NULL R64**.

Step 7 Null Sine Wave

1. The Model 91 display reads **SINE NULL R64**. Leave the test equipment connected as shown in figure 4-8.
2. Slide the cover back. Adjust the PLL board's R64 (see figure 4-11) until the DVM reads 0 ±2mVdc of sine offset. Slide the cover back on.

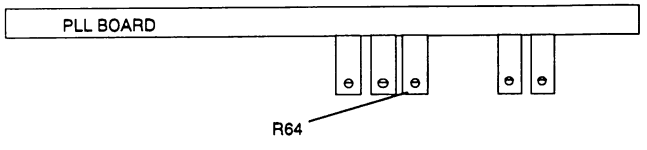


Figure 4-11. R64 Locator

3. On the Model 91, press the **OFFSET** key to advance to the next step. Verify the display flashes **CALIBRATING** and then displays **SQUARE 0 R158**.

Step 8 Null Square

1. The Model 91 display reads **SQUARE 0 R158**. Leave the test equipment connected as shown in figure 4-8.
2. Slide the cover back, and adjust the Output board's R158 (see figure 4-12) until the DVM reads 0Vdc ±2mVdc of square offset. Slide the cover back on.

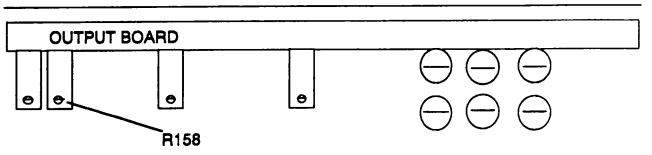


Figure 4-12. R158 Locator

3. Press the **OFFSET** key to advance to the next step. Verify the display flashes **CALIBRATING** then displays **TRI AMPL R211 1**.

Step 9 Adjust Triangle Amplitude

1. The Model 91 displays **TRI AMPL R211 1**. Connect the test equipment (Scope set for Vdc) as shown in figure 4-13. Note the amplitude of the triangle wave.

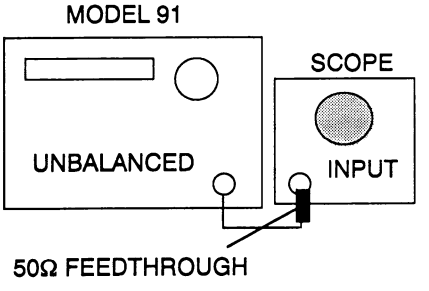


Figure 4-13. Triangle Amplitude Setup

2. On the Model 91, rotate the **Knob** until the display reads **TRI AMPL R211 2**. Note the amplitude of the square wave.
3. Use the **Knob** to step between the triangle and square waves. Slide the cover back. Adjust R211 (figure 4-14) on the PLL board until the peak to peak amplitude of the triangle matches the peak to peak amplitude of the square wave. Slide the cover back on.

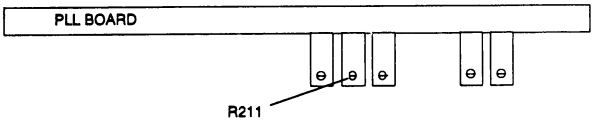


Figure 4-14. R211 Locator

4. Press the **OFFSET** key to advance to the next step. Verify the display flashes **CALIBRATING** then displays **SIN AMPL R208 0**.

Step 10 Adjust Sine Amplitude

1. The Model 91 display reads **SIN AMPL R208 0**. Leave the test equipment connected as shown in figure 4-13.
2. On the Model 91, rotate the **Knob** until the display reads **SIN AMPL R208 2**. Note the amplitude of the square wave.
3. Use the **Knob** to step between the sine and square waves. Slide the cover back. Adjust R208 on the PLL board (see figure 4-15) until the peak to peak amplitude of the sine wave matches the peak to peak amplitude of the square wave. Slide the cover back on.

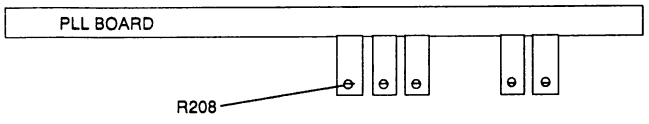


Figure 4-15. R208 Locator

4. Press the **OFFSET** key to advance to the next step. Verify the display flashes "=**CALIBRATING** then displays **HF SYM R9**.

Step 11 Adjust High Frequency Symmetry

1. The Model 91 display **HF SYM R9**. Leave the test equipment connected as shown in figure 4-13.
2. Slide the cover back. Adjust R9 on the output board (see figure 4-16) while observing the scope. Use the scopes delta time cursors to measure the two halves of the square's time symmetry between the 50% points. Adjust R9 until the time symmetry is equal ±0.5 ns. Slide the cover back on.

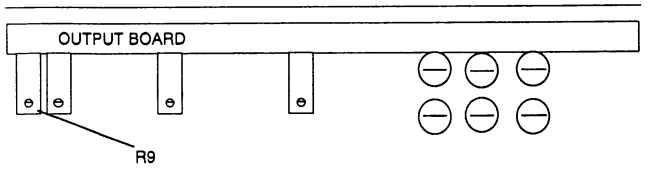


Figure 4-16. R9 Locator

3. Press the **OFFSET** key to advance to the next step. Verify the display flashes **CALIBRATING** then displays **HF QUAL R69, ..., R86**.

Step 12 Adjust High Frequency Waveform Quality

1. The Model 91 display reads **HF QUAL R69, ... , R86**. Leave test equipment as shown in figure 4-13.
2. Slide the cover back. Adjust R69, R70, R67, R86, R84, and R87 on the output board (see figure 4-17) for best time symmetry and aberrations. The leading and trailing edge transition time must be less than 8ns. Transition time is measured between the 10% and 90% points of the square wave. Aberration must be less than 4%. The Model 91 unbalanced output must be terminated with three feet of coax cable and the cable terminated with a 50Ω terminator for specified waveform quality. Slide the cover back on.

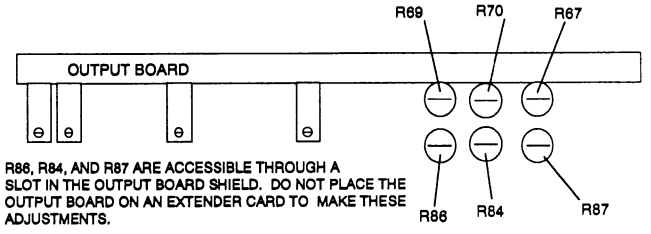


Figure 4-17. R69, R70, R86, R87, R84, and R67 Locator

3. Press the **OFFSET** key to advance to the next step. Verify the display flashes **CALIBRATING** then displays **PHASE 0 XXXXX**.

Step 13 Adjust Phase 0°

1. The Model 91 display reads **PHASE 0 XXXXX**, where XXXXX represents a calibration value. Connect the test equipment as shown in figure 4-18.

NOTE
A phase meter could be used in place of a scope in steps 13, 14, 15, and 16.

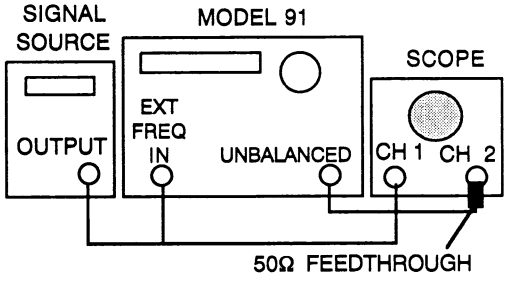


Figure 4-18. Phase Setup

2. Set the signal source controls as follows:
   Set Function to Sine.
   Frequency to 2.01 kHz.
   Output Level to 5Vpp.
3. Set the scope controls as follows:
   Trigger to channel 1.
   Adjust Channel 1 and 2 gain and offset controls to display identical superimposed waveforms.
   Select channel 2 Invert.
   Select 1 and 2 Add.
4. On the Model 91,

   Adjust the **Knob** to null the waveform on the scope.

Press the **OFFSET** key. Verify the display flashes **CALIBRATING** then displays **PHASE +180 XXXXX.**

Step 14 Adjust Phase +180°

1. The Model 91 displays **PHASE +180 XXXXX** where XXXXX represents a calibration value. Leave the test equipment connected as shown in figure 4-18. Do not change the signal source.

2. Set the scope controls as follows:

   If necessary, adjust Channel 1 and 2 gain and offset controls to display identical superimposed waveforms.

3. On the Model 91,

   Adjust the **Knob** to null (minimum displayed signal) the "added" waveform on the scope display.

   Press the **OFFSET** key advance to the next step. Verify the display flashes **CALIBRATING** and then displays **PHASE -180 Y XXXXX**.

Step 15 Adjust Phase -180°

1. The Model 91 displays **PHASE -180 XXXXX,** where XXXXX represents a calibration value. Leave the test equipment connected as shown in figure 4-18. Do not change the signal source. The scope should not need adjustment.

2. On the Model 91,

   Adjust the **Knob** to null (minimum displayed signal) the waveform on the scope display.

   Press **OFFSET** key to advance to the next step. Verify that the display flashes **CALIBRATING** and then displays **SQ PHASE 0 XXXXX**.

Step 16 Adjust Square Phase 0°

1. The Model 91 displays **SQ PHASE 0 XXXXX** where XXXXX represents a calibration value. Leave the test equipment connected as shown in figure 4-18. Do not change the signal source.

2. Set the scope controls as follows:

   Turn off Add.

   Observe the sine wave reference on channel 1.
   Trigger on channel 1.
   Observe the square wave on channel 2.
   Superimpose the sine over the square wave.
   Increase the gain of channel 1 (sine) by 10.

   Using the scope's controls, adjust channel 1 for 0Vdc offset.

   Using the scope's horizontal time and trigger slope, set the negative-going zero crossing of the sine wave and square wave to occur at the center of the graticule. Magnify the center of the display by X10.

3. On the Model 91

   Adjust the **Knob** to null so the square's transition passes through the sine's zero crossing point.

4. Set the scope as follows:

   Change the trigger slope to display the positive-going transition. If an error exists, split the difference between the two slopes using the Model 91's **Knob**.

5. On the Model 91,

   Press the **OFFSET** key to advance to the next step. Verify the display flashes **CALIBRATING** and then displays **WIDTH 10.0 NS XXX**.

Step 18. Adjust 10 ns Width Analog One-Shot

1. The Model 91 displays **WIDTH 10.0 NS XXX**. Connect the test equipment as shown in figure 4-19.

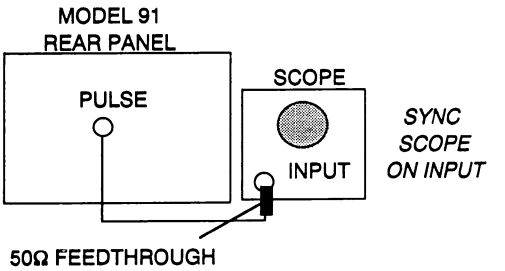


Figure 4-19. Pulse Width Setup

2. On the scope, set the scope's time base to display a 10 ns ±0.1 ns pulse width.

3. On the Model 91, rotate the **Knob** until the scope displays a 10.0 ns ±0.1 ns pulse width.

   Press the **OFFSET** key to advance to the next step. Verify the display flashes **CALIBRATING** then displays **AWDTH 20.0 NS XXX**.

Step 19. Adjust 20 ns Width Analog One-Shot

1. The Model 91 displays **AWDTH 20.0 NS XXX**. Connect the test equipment as shown in figure 4-19.

2. On the scope, set the scope's time base to display a 20 ns ±0.1 ns pulse width.

3. On the Model 91, rotate the **Knob** until the scope displays a 20.0 ns ±0.1 ns pulse width.

   Press the **OFFSET** key to advance to the next step. Verify the display flashes "**CALIBRATING** then displays **DWDTH 20.0 NS XXX**.

Step 20. Adjust 20 ns Width Digital One-Shot

1. The Model 91 displays **DWDTH 20.0 NS XXX**. Connect the test equipment as shown in figure 4-19.
2. On the scope, set the scope's time base to display a 20 ns ±0.1 ns pulse width.
3. On the Model 91, rotate the **Knob** until the scope displays a 20.0 ns ±0.1 ns pulse width.

   Press the **OFFSET** key to advance to the next step. Verify the display flashes **CALIBRATING** then displays **DWDTH 30.0 NS XXX**.

Step 21. Adjust 30 ns Width Digital One-Shot

1. The Model 91 displays **DWDTH 30.0 NS XXX**. Connect the test equipment as shown in figure 4-19.
2. On the scope, set the scope's time base to display a 30 ns ±0.1 ns pulse width.
3. On the Model 91, rotate the **Knob** until the scope displays a 30.0 ns ±0.1 ns pulse width.

   Press the **OFFSET** key to advance to the next step. Verify the display flashes **CALIBRATING** then displays **DELAY 0 NS (REF)**.

Step 22. 0 ns Delay Reference

1. The Model 91 displays **DELAY 0 NS (REF)**. Connect the test equipment as shown in figure 4-20.

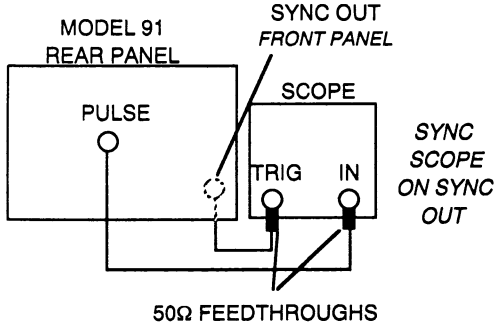


Figure 4-20. Pulse Delay Setup

2. On the scope, set the time base to measure delay with 0.1 ns resolution. Measure and note the delay relative to the Sync Out. This measured value becomes the 0 ns Reference Value. Sync the scope from the trigger input.
3. On the Model 91, press the **OFFSET** key to advance to the next step. Verify the display flashes **CALIBRATING** then displays the words **ADLY 10.0 NS XXX**.

Step 23. Adjust 10 ns Delay Analog One-Shot

1. The Model 91 displays **ADLY 10.0 NS XXX**. Connect the test equipment as shown in figure 4-20.
2. On the scope, set the time base so a pulse 10 ns can be resolved to ±0.1 ns. Sync the scope from the trigger input.
3. On the Model 91, rotate the **Knob** until the scope displays a 10.0 ns ±0.1 ns pulse delay relative to the 0ns Reference Value (step 22).

   Press the **OFFSET** key to advance to the next step. Verify the display flashes **CALIBRATING** then displays **DDLY 10.0 NS XXX**.

Step 24. Adjust 10 ns Delay Digital One-Shot

1. The Model 91 displays **DDLY 10.0 NS XXX**. Connect the test equipment as shown in figure 4-20.
2. On the scope, set the time base so a pulse 10 ns can be resolved to ±0.1 ns. Sync the scope from the trigger input.
3. On the Model 91, rotate the **Knob** until the scope displays a 10.0 ns ±0.1 ns pulse delay relative to the 0ns Reference Value (step 22).

   Press the **OFFSET** key to advance to the next step. Verify the display flashes **CALIBRATING** then displays **DDLY 20.0 NS XXX**.

Step 25. Adjust 20 ns Delay Digital One-Shot

1. The Model 91 displays **DDLY 20.0 NS XXX**. Connect the test equipment as shown in figure 4-20.
2. On the scope, set the time base so a pulse 20 ns can be resolved to ±0.1 ns. Sync the scope from the trigger input.
3. On the Model 91, rotate the **Knob** until the scope displays a 20.0 ns ±0.1 ns pulse delay relative to the 0ns Reference Value (step 22).

   Press the **OFFSET** key to advance to the next step. Verify the display flashes **CALIBRATING** then displays the words **DBL 20.0 NS XXX**.

Step 25. Adjust 20 ns Double Pulse

1. The Model 91 displays **DBL 20.0 NS XXX**. Connect the test equipment as shown in figure 4-20.
2. On the scope, set the time base so a double pulse delay can be resolved to ±0.1 ns.

3. On the Model 91, rotate the **Knob** until the scope displays a double pulse whose leading edges are 20.0 ns ±0.1 ns apart.

   Press the **OFFSET** key to advance to the next step. Verify the display flashes **CALIBRATING** then displays **DLY UB OUT XXX**.

Step 26. Adjust Unbalanced Out Sync Delay

1. The Model 91 displays **DLY UB OUT XXX**. Connect the test equipment as shown in figure 4-21.

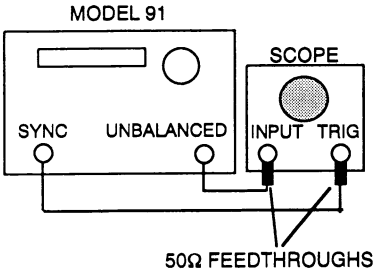


Figure 4-21. Unbalanced Setup

2. On the scope, set the time base to display a pulse to ±0.1 ns resolution. Sync the scope from the trigger input.

3. On the Model 91, rotate the **Knob** until the scope displays a pulse delay of 0.0 ns ±0.1 ns relative to the Sync Out.

   Press the **OFFSET** key to advance to the next step. Verify the display flashes **CALIBRATING** then displays **REMOVE CABLES**.

   Remove all cables from the Pulse Out, Sync Out, and Unbalanced Out connectors. Press the **OFFSET** key to advance to the next step. Verify the display flashes **CALIBRATING** then displays the word **CONFIDENCE**.

Step 27. Confidence Check

1. The Model 91 displays **CONFIDENCE** which tests and verifies the accuracy of the Model 91's voltage reference, DVM, and output amplifier. Connect test equipment (DMM set to Vdc) as shown in figure 4-22 (no termination).

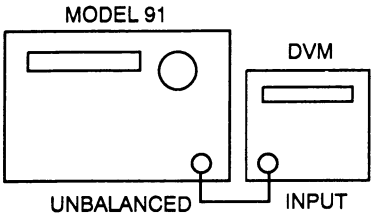


Figure 4-22. Confidence Check Setup

2. Measure the Model 91's unloaded output dc voltage with the DVM. Verify the output voltage measures between +9.8 and +10.2 Vdc.

3. On the Model 91, press the **OFFSET** key to advance to the next step. Verify the display flashes **CALIBRATING** and then displays **AUTOCAL ENABLE**.

Step 28. Auto Cal Enable/Disable

1. The Model 91 displays **AUTOCAL ENABLE**. Use the **Knob** to step from **AUTOCAL ENABLE** to **AUTOCAL DISABLE**.

   When enabled, the operator can AutoCal the Model 91 as described in paragraph 4.2.

   When disabled, the operator cannot run the AutoCal procedure. If AutoCal is selected (**SHIFT** and **CALIBRATE**), the Model 91 displays the message **AUTO CAL DISABLED**.

2. On the Model 91, press the **CALIBRATE** key. Verify the Model 91 displays **CALIBRATION OFF**. The Calibration Procedure is now complete.

   CAUTION

   Failing to perform step 28 item 2 will keep the calibrations parameters from being stored in memory, and the unit's calibration will be corrupted.

Step 29 Wrap up Calibration

1. Remove the power and disconnect the test equipment.

2. Install the shield and top cover using the five screws.

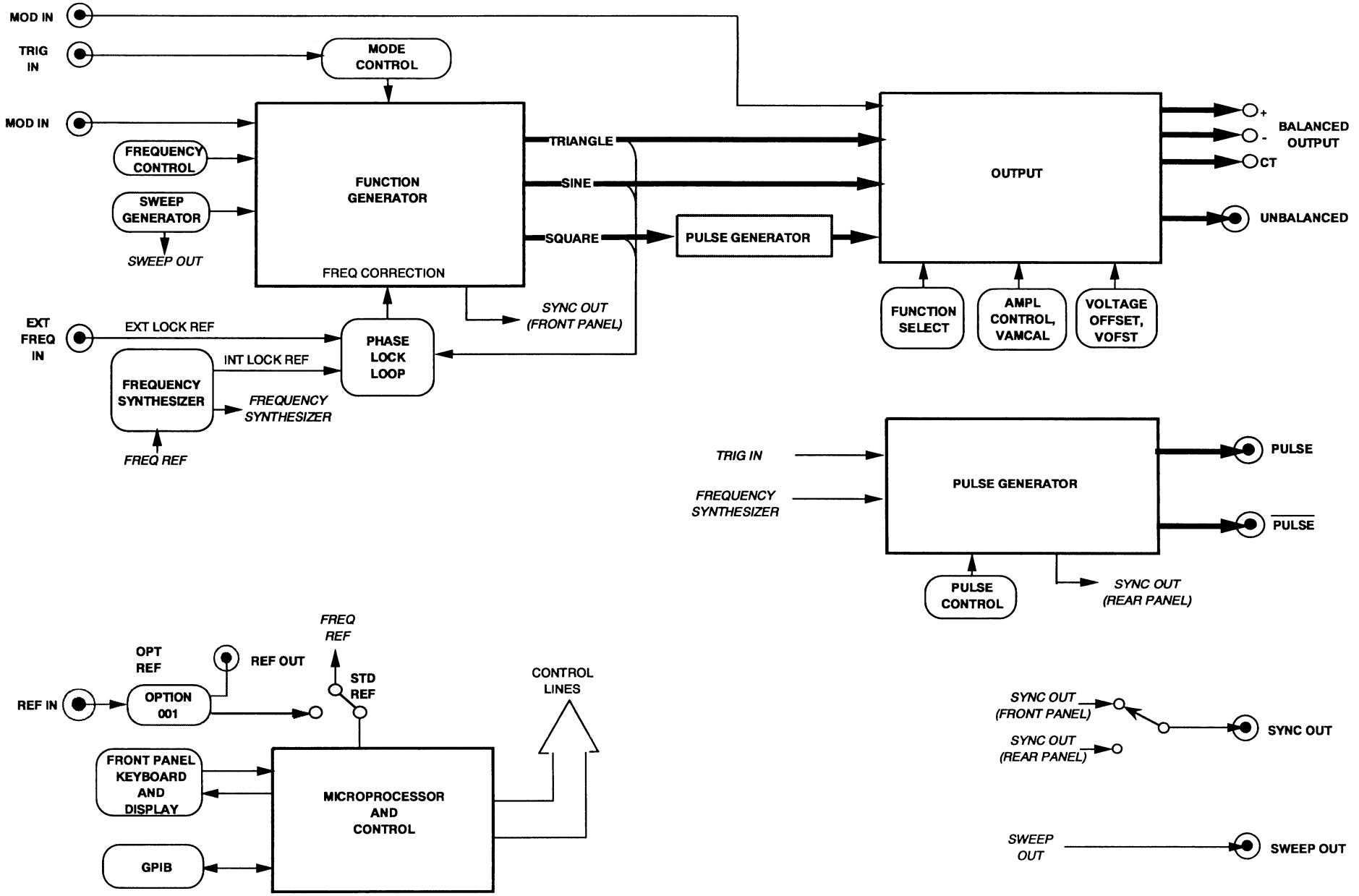


Figure 5-1. Model 91 Functional Block Diagram

SECTION 5
CIRCUIT DESCRIPTION

5.1 THE MODEL 91

Section 5 performs two functions. It introduces the Model 91's major circuit blocks. Also, it describes how the blocks interconnect for the various operating modes. This section concludes with a detailed block circuit description with emphasis on signal flow and control within the block.

5.1.1 Introduction

The Model 91 consists of four major functional blocks (function generator, pulse generator, output , and microprocessor section) as shown in figure 5-1. All functional blocks are contained on six separate assemblies (the Mother, Output, Function Generator, Phase Lock, Pulse, and Front Panel Boards).

5.1.2 Major Blocks

5.1.2.1 Function Generator Block

The Function Generator block produces the Model 91's triangle, square and sine waves. These three waveforms drive the output block. Also, the function generator block controls the frequency and symmetry of the waveforms. Four inputs control the generator's frequency: Frequency Control, Sweep Generator, and Phase Lock Loop, plus external Modulation Input.

Frequency Control sets up the generator's fixed frequency. If a synthesizer mode is selected, the Phase Lock Loop supplies a frequency correction voltage which locks the Function Generator's frequency to an internal or external frequency. The Phase Lock Loop receives its internal frequency input from the Frequency Synthesizer which is referenced to the Freq Ref or optional reference. For external phase lock, the phase lock loop receives its signal via the Ext Freq In connector allowing a phase shift of the output waveform relative to the source. If the sweep mode is selected, Frequency Control sets the start frequency and Sweep Generator sets the stop frequency and sweep width. Another input, Mod In, frequency modulates instantaneous frequency of the generator.

The Mode Control enables the Function and Pulse Generators to produce continuous waveforms, single cycled triggered waveforms, and multiple cycled gated and burst waveforms. Burst produces a user-defined number of cycles.

5.1.2.2 Pulse Generator Block

The pulse generator contains the width and delay one-shots that can be configured to produce the normal, delayed, and double pulse outputs as well as the external width output. Two sources (frequency synthesizer and trigger input) control the pulse repetition rate. The pulse generator provides two outputs: front panel output via the Output block (to 20 MHz) and rear panel outputs (to 50 MHz). In addition, the rear panel output supplies square waves to 100 MHz. Like the Function Generator, the pulse generator permits triggered, gated, and burst modes.

5.1.2.3 Output Block

The Output block selects the waveform, controls the output level and offset, and drives the external devices. The output level can be fixed or modulated (Amplitude Modulated or Suppressed Carrier Modulated).

5.1.2.4 Microprocessor Section

The Microprocessor Section provides the processing and interfacing for the Model 91. It supplies the analog control voltages, such as frequency control voltage or amplitude control voltage. It also controls the signal routing within the unit. The Microprocessor Section also interfaces with the display/keyboard and the GPIB interface.

5.2 Functional Signal Flow

5.2.1 Introduction

Figure 5-1 provides an overall diagram of the Model 91. Because the Model 91 is a firmware driven instrument, it is hard to get a feel of signal flow throughout the instrument. The following figures illustrate how the various blocks link together during different operating modes. These figures provide simplified diagrams. More detailed diagrams will be provided as part of the detailed block description

5.2.2 Function Generator Operating Modes

Figures 5-2 through 5-9 illustrate the signal flow through the Model 91's block for the function generator modes.

Non-Synthesized

This is the basic function generator operating mode. The frequency control block supplies a voltage to the function

generator block that controls the generator frequency (see figure 5-2).

Conditions:

Mode:	Continuous
Function:	Sine, Triangle, or Square
Frequency:	to 20 MHz

Figure 5-2. Non-Synthesized Operation

FM/VCG

Figure 5-3 illustrates the FM/VCG mode's signal flow. Like the non-synthesized mode, the frequency control sets the center (FM) or start (VCG) frequency, but an external signal via MOD IN varies the generator's frequency.

Conditions:

Mode:	FM
Function:	Sine, Triangle, or Square
Symmetry:	50%

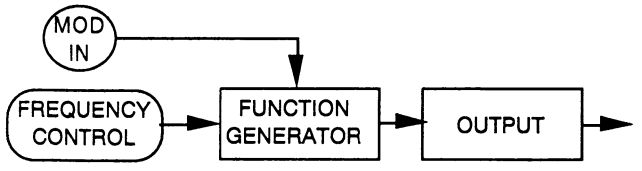


Figure 5-3. FM/VCG

Synthesized/Internal Reference

This mode improves the frequency accuracy of the unit. See figure 5-4. The phase lock loop monitors the function generator's output, compares the frequency to the frequency synthesizer's output, and produces a correction voltage that controls the frequency of the function generator. The frequency synthesizer is referenced to either the standard frequency reference or optional TCXO reference.

Conditions:

Mode :	Continuous, AM ,and SCM
Function:	Sine, Triangle, and Square
Frequency:	20 Hz to 20 MHz
Lock Source:	Internal

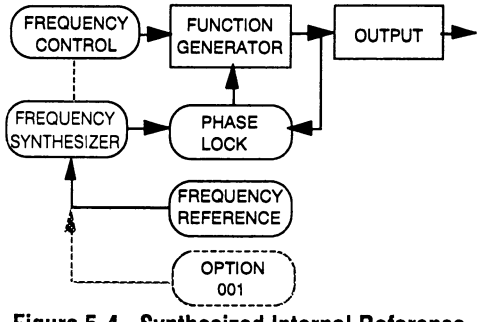


Figure 5-4. Synthesized Internal Reference

External Reference/Phase Shift

In this mode, the Model 91 allows its frequency to be referenced to an external signal source via the EXT FREQ IN connector. The Model 91 measures the external frequency and adjusts the frequency control voltage to match the input frequency. Like the Synthesized/Internal Reference mode, the phase lock loop monitors and corrects the function generator. Also, in this mode, the phase relative to the EXT FREQ IN signal can be shifted.

Conditions:

Mode :	Continuous, AM ,and SCM
Function:	Sine, Triangle, and Square
Frequency:	20 Hz to 20 MHz
Lock Source:	External

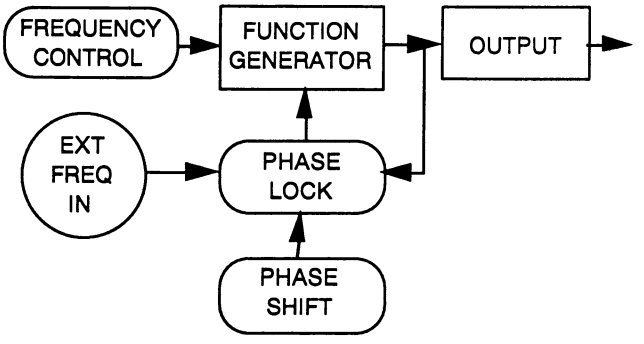


Figure 5-5. External Reference/Phase Shift

Sweep Mode

In this mode, the Model 91 produces a swept frequency output. Frequency Control sets the lowest frequency. The microprocessor via the sweep generator sets the sweep length and sweep type.

Conditions:

Mode:	Sweep
Function:	Sine, Triangle, and Square
Frequency:	Three decade limit
Sweep Type:	Linear or Logarithmic sweep up or down

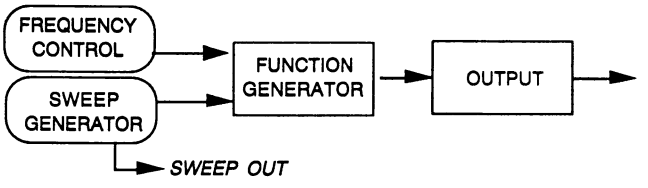


Figure 5-6. Sweep Mode

AM and SCM Mode

In these modes, an external signal at MOD IN controls the instantaneous amplitude of the output signal. Figure 5-7 illustrates the signal flow for AM and SCM modes.

Conditions:

Mode:	AM or SCM
Function:	Sine, Triangle, and Square
Lock Source:	Internal or External

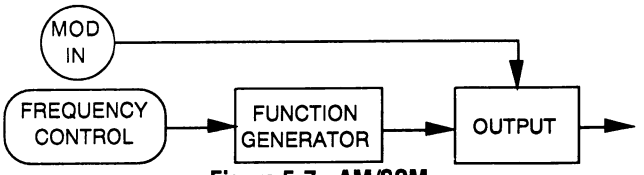


Figure 5-7. AM/SCM

Internal Trigger

In this mode, the Model 91 uses its own internal frequency synthesizer as a trigger source; see figure 5-8. In triggered modes, the Mode control circuit shuts off the function generator until a trigger signal is received.

Conditions:

Mode:	Trigger, Gated, and Burst
Functions:	Sine, Triangle, and Square
Trigger Setup:	Internal Trigger

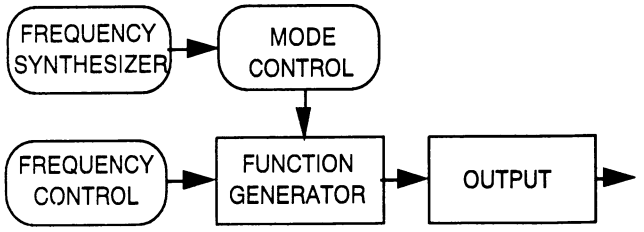


Figure 5-8. Internal Trigger

External Trigger

In this mode, the Model 91 uses an external signal at TRIG IN to trigger the function generator; see figure 5-9. In triggered modes, the Mode control circuit shuts off the function generator until a trigger signal is received.

Conditions:

Mode:	Trigger, Gated, and Burst
Functions:	Sine, Triangle, and Square
Trigger Setup:	External Trigger

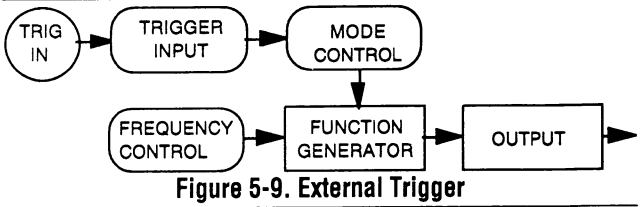


Figure 5-9. External Trigger

5.2.3 Pulse Generator Operating Modes

Figures 5-10 through 5-15 illustrate the signal flow through the Model 91's block for the pulse generator modes.

Normal and Delayed Pulses

When either continuous normal or delayed pulses are selected, the Model 91's frequency synthesizer triggers the pulse generator's delay one-shot. For normal pulses, the delay one-shot runs at a fixed minimal delay. In the delayed pulse mode, the delay one-shot delays the pulse by a programmed value. In either case, the delay one-shot drives the width one-shot which produces the output pulse. Pulses can be routed to the front panel outputs at frequencies to 20 MHz and rear panel outputs to 50 MHz. Refer to figure 5-10.

Conditions:

Function:	Normal and Delayed
Mode:	Continuous
Output:	Front or Rear Outputs

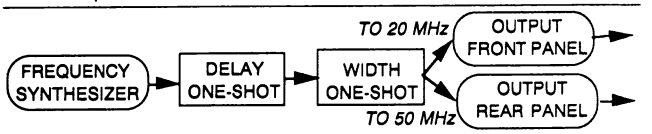


Figure 5-10. Normal and Delayed Pulses

Triggered Normal and Delayed Pulse

In the triggered mode, a TRIG IN signal via the trigger amplifier and mode control triggers the delay one-shot. The remaining circuits in the pulse generator function the same as in the normal and delayed pulse modes. Refer to figure 5-1.

If gate and burst are selected, the function generator provides the trigger source for the pulse generator.

Conditions:

Function:	Normal and Delayed
Mode:	Trigger
Output:	Front or Rear Outputs

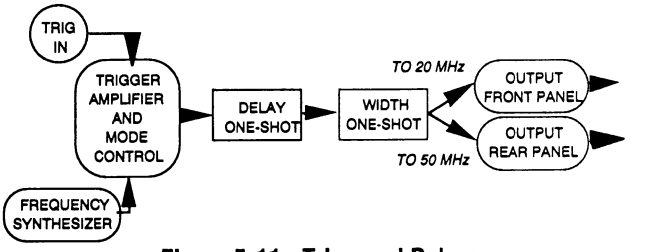


Figure 5-11. Triggered Pulses

Double Pulses

When the double pulse function is selected, the triggering source triggers both the delay and width one-shots; see figure 5-12. The trigger source initially triggers the width one-shot to produce the first pulse. The delay one-shot triggers the width one-shot producing the second pulse. If the continuous mode is selected, the frequency synthesizer provides the trigger source. In the triggered mode, a TRIG IN signal via the trigger amplifier and mode control triggers the one-shots. If gate and burst are selected, the function generator provides the trigger source for the pulse generator.

Conditions:

Function:	Double Pulse
Mode:	Continuous and Triggered
Output:	Front or Rear Outputs

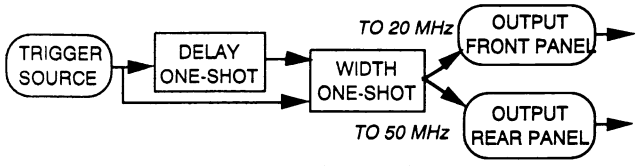


Figure 5-12. Double Pulse

50 MHz Square Wave

Between 50.002 and 100 MHz, the pulse generator is used to produce high frequency square waves. These square waves are only available from the rear panel outputs. See figure 5-13.

Conditions:

Function:	Square Wave
Mode:	Continuous
Output:	Rear Outputs
Frequency:	50.002 to 100 MHz

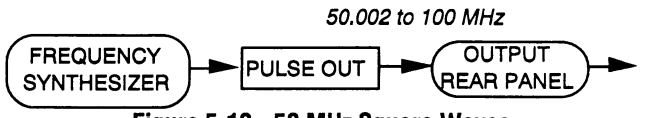


Figure 5-13. 50 MHz Square Waves

External Width

If the external width mode is selected, the unit produces an output derived from the trigger input. See figure 5-14.

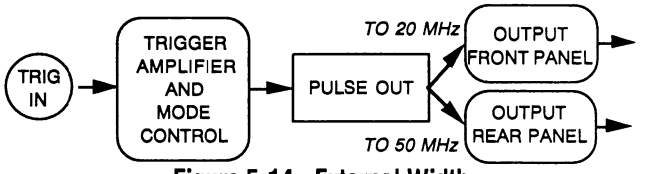


Figure 5-14. External Width

5.3 MODEL 91 BLOCK DESCRIPTIONS

Paragraph 5.3 provides a detailed description of the blocks within the Model 91. The purpose of these detailed descriptions is to describe the function, explain signal flow, and define controls of each block.

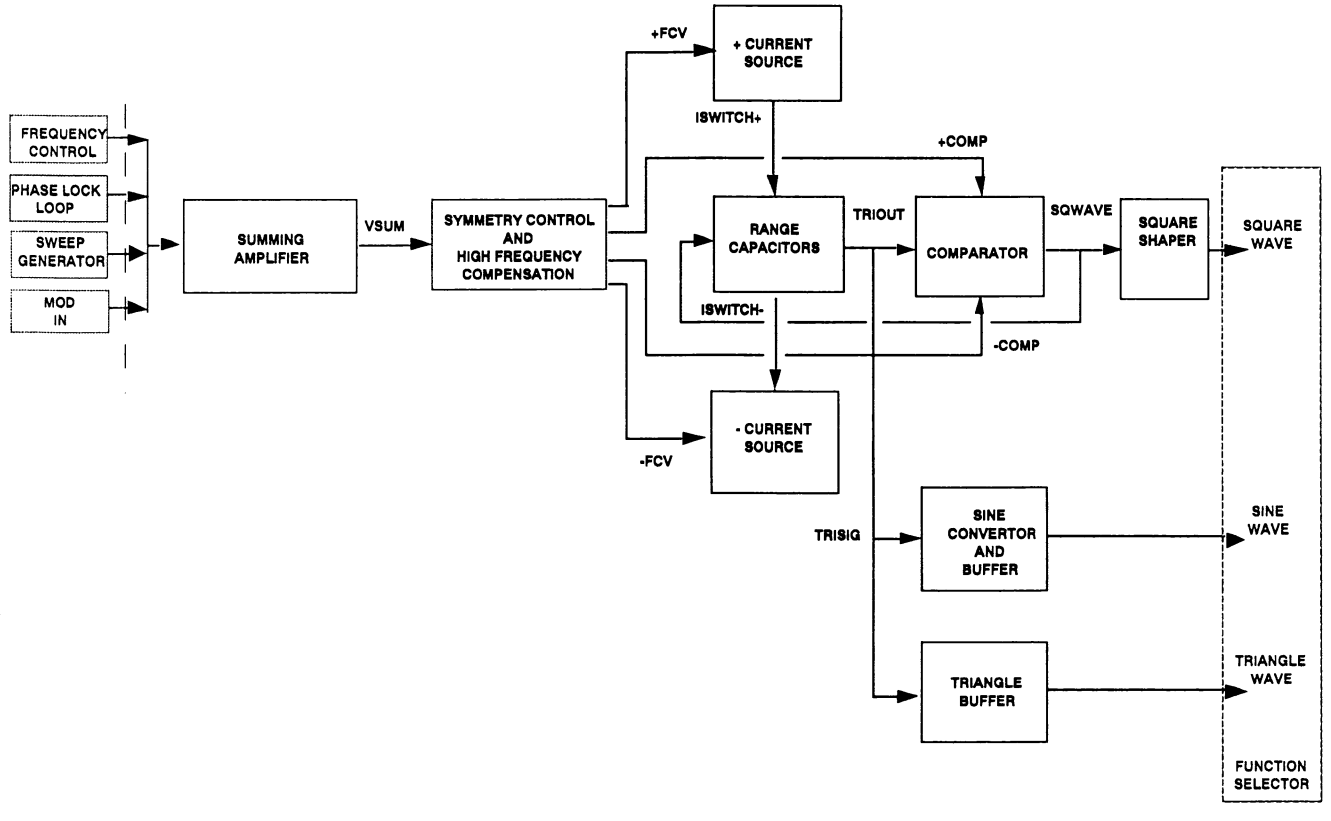


Figure 5-15. Function Generator Block Diagram

5.3.1 Function Generator

5.3.1.1 Introduction

The function generator section produces the Model 91's square and triangle waves, as well as the sine wave. The Function Generator block (see figure 5-15) contains:

VCG Summing Amplifier;

Symmetry Control;

The Function Generator Loop consisting of the VCG Current Sources, Frequency Range Capacitors, Capacitance Multiplier, Triangle Buffer, Comparator, and Diode Gates;

High Frequency Compensation;

Trigger (Mode) Control;

Sine Convertor.

The VCG Summing Amplifier produces an output voltage proportional to the sum of the programmed frequency values. This voltage drives the symmetry control which produces an equal but opposite voltage that controls the positive and negative current sources.

The following example illustrates how the function generator loop operates; see figure 5-16. Assume the comparator's output is high. This switches the diode gate (CR35 - CR38) allowing the current via +COMP to flow into the resistor (R102) thus establishing the positive "reference square wave" voltage. The positive reference voltage is about +1.25V ($V=+I_{COMP} \times R102$). Also when the comparator output is high, the other diode gate (CR27 - CR30) is biased to allow the current, $I_{SWITCH+}$, to charge the Frequency Range Capacitor. Charging the capacitor with a constant current produces a linear ramp. When the ramp voltage reaches the positive reference square voltage, the Comparator output switches low. With the comparator's output low, the diode gate (CR35 - CR38) switches and allows the current via -COMP to flow from the resistor (R102) establishing the negative reference square wave voltage - about -1.25V. At the same time, the Comparator switches diode gate (CR27 - CR30) and allows the current $I_{SWITCH-}$ to discharge the Frequency Range Capacitor. The Frequency Range Capacitor determines the waveform's frequency range. Increasing the currents increases the frequency. Increasing the Frequency Range Capacitor decreases the frequency. The opposite of each is also true. This cycle repeats producing simultaneous triangle and square waves. The timing diagram with figure 5-16 illustrates waveform timing.

The Triangle Buffer isolates the Frequency Range Capacitor from the Comparator. An output from the comparator drives a square shaper producing a square wave. The triangle also drives the sine convertor producing the sine wave. High frequency compensation adjusts the reference level within the comparator compensating for delay times within the loop at higher frequencies.

Normally, the current sources, $I_{SWITCH+}$ and $I_{SWITCH-}$, produce equal but opposite polarity currents. To change the symmetry (duty cycle) of the waveform, the Model 91 changes the ratio of the current sources. For example, the $I_{SWITCH+}$ source may supply more than half of the current, while the $I_{SWITCH-}$ source may supply less than half of the current.

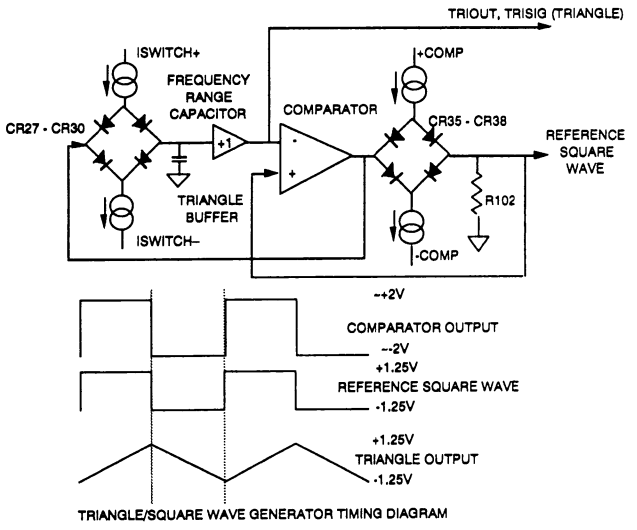


Figure 5-16. Function Generator Loop

5.3.1.2 VCG Summing Amplifier

The VCG Summing Amplifier (U5 - schematic 1104-00-3342 sheet 2 of 7) algebraically adds fours inputs: MOD IN, VFREQ, SWEEP, and VLOOP. These input signals control the frequency of the function generator's waveform. MOD IN provides the FM/VCG input which can be an ac (FM) or dc (VCG) signal. VFREQ supplies a dc value representing the function generator's programmed frequency via the DAC Sample and Hold Network on the Motherboard (schematic 1104-00-3440 sheet 5 of 10). The Sweep Generator (schematic 1104-00-3342 sheet 2 of 7) produces a ramp that drives the SWEEP input. VLOOP is an analog frequency correction signal supplied by the phase lock loop. Another input, VCGZERO, is an AutoCal correction voltage supplied by the DAC Sample and Hold Network on the Motherboard. Output from the VCG Summing amplifier, VSUM, drives the Symmetry Control (paragraph 5.3.1.3).

Most inputs to the VCG Summing Amplifier are connected by analog switches (U4A - U4D). Each switch is controlled by a control line from the board's interface logic. The MOD IN signal connects to the amplifier when $\overline{FM}$ line (U4A) goes low. At the same time, the FM line goes high disconnecting (U4D) the FM/VCG input resistor (R3) from

ground. When FM/VCG is not selected, switch (U4D) is closed. Control line $\overline{FR7}$ switches in added phase lock filtering at 200 kHz and below. When the frequency is set to <20 mHz (FR0) or symmetry is not 50%, the control line $\overline{SCALE}$ inserts a resistor (R8) which divides the VFREQ input by 10 allowing the unit to operate on the middle decade of the selected frequency range. All control lines used in the VCG Summing Amplifier are supplied from the Function Generator Input Logic (paragraph 5.3.6.4).

5.3.1.3 Symmetry Control

Symmetry Control (schematic 1104-00-3342 sheet 3 of 7) controls the time symmetry of the function generator's waveform. The input, VSUM from the VCG Summing Amplifier drives two similar circuits one controlling the charging current (U7C) and the other controlling the discharging current (U7D). The two outputs from the circuit, +FCV and -FCV, supply equal but opposite polarity (at 50% symmetry) voltages. The voltages, +FCV and -FCV, drive the VCG Current Sources and the High Frequency Compensation circuit.

The +FCV circuit consists of the inverting amplifier (U9) with the DAC (U7C, U10) that controls the gain of the circuit. The DAC (U12B, U11A) provides an offset adjustment. The Microprocessor Section on the Motherboard loads the data values into these DACs.

The –FCV circuit consists of the non-inverting amplifier (U15) with the DAC (U7D, U16) controlling the gain. The DAC (U12A, U11B) provides an offset adjustment. The Microprocessor Section on the Motherboard loads the data values into these DACs.

At 50% symmetry (symmetrical waveform), each circuit provides equal outputs. As the symmetry setting changes away from 50% in either direction, one circuit provides greater amplification and the other less amplification. The DACs by themselves provide linear gain, but placing them in the feedback paths of U9 and U14 provides an overall circuit gain of the inverse function of the symmetry setting.

The AutoCal circuit measures the +FCV and –FCV voltage and provides correction values to the offset DACs data lines.

5.3.1.4 High Frequency Compensation

The High Frequency Compensation circuit (schematic 1104-00-3342 sheet 4 of 7) corrects for internal circuit time delays within the function generator loop. On the 200 kHz to 2 MHz and 2 MHz to 20 MHz frequency ranges, this circuit decrease the current, +COMP and –COMP, which decreases the reference square wave voltage. This causes the Comparator to switch earlier, cancelling the tendency of the triangle to grow in amplitude as the frequency increases.

The High Frequency Compensation circuit consists of two DACs (U12C, U12D). The DAC uses the +FCV and –FCV voltages as references. The Microprocessor Section loads data into the DACs which adjusts the gain of the output. Outputs from the DACs ,+COMP and –COMP, are derived from the +FCV and –FCV voltages.

5.3.1.5 Trigger Control and Trigger Baseline Compensation

Trigger Baseline Compensation (schematic 1104-00-3342 sheet 4 of 7) controls the quiescent baseline level during non-continuous modes of operation. A single line, RUN, from Mode control (paragraph 5.3.5) controls the triangle wave by either forcing the TRINODE line to "ground" (trigger, gate, and burst modes) or "open" (continuous mode). With the RUN line low, the TRINODE line is forced to ground. With RUN high, the generator runs continuously.

This circuit consists of amplifiers (U19 and U20) and transistors (Q5, Q6, and Q7). Amplifier (U19) and transistor (Q5) form a voltage to current converter. A voltage equal to VSOURCE appears across the resistor (R38) producing a current I_{R30}. The current mirror (U20, Q7) reflects the current I_{R30} off the –VCG supply. The drop across R39 also equals +FCV. U20 forces a drop equal to +FCV across R40, but R40 is half the value of R39 which produces a current equal to 2($I_{SWITCH+}$). When RUN goes high, the current, 2($I_{SWITCH+}$), flows through the diode (CR10) reverse biasing diodes CR7 and CR8. This releases the TRINODE line and allows the function generator to run.

When the RUN line goes low, the diode (CR10) is reversed biased and the current flows through diodes CR8 and CR9. A current equal to $I_{SWITCH+}$ flows through each diode. This forces the TRINODE to ground potential and stops the function generator. The Mode Control and Burst Counter logic on the Pulse Board controls the RUN line.

5.3.1.6 VCG Current Sources

The VCG current sources (schematic 1104-00-3342 sheet 3 of 7) convert the two symmetry control voltages, +FCV and –FCV, into two currents, I_{SWITCH} + and I_{SWITCH} –. Because the current sources are mirror images, only the positive current source will be described.

The positive current source consists of two amplifiers (U13 and U14) and two transistors (Q1 and Q2). U13 and Q1 form a voltage to current converter. U13 forces the voltage drop across R31 to produce the current, I_{R31}. The current, I_{R31}, also flows through the resistor, R30, producing a voltage equal to +FCV. The current mirror stage (U14 and Q2) forces a voltage drop across R36 equal to +FCV. The current through R36 is $I_{SWITCH+}$ and drives the diode switch (CR35 - CR38). Another output from this current source,

VSOURCE, drives the Trigger Baseline Compensation circuit.

The negative current source (U17, Q3, U18, Q4) is identical to the positive current source. U17 and Q3 form the voltage to current converter, and U18 and Q4 forms the current mirror.

At 50%, the two resistors (R31 and R32) connect directly to ground. But selecting variable symmetry places R131 between the junction of R31 and R32 and ground. The control line $\overline{\text{SYM ON}}$ switches R131.

5.3.1.7 Frequency Range Capacitors

The frequency range switches (schematic 1104-00-3342 sheet 5 of 7) select the frequency range capacitors that are connected to the TRINODE line. On the 20 MHz range, the timing capacitance is a 15 pF capacitor (C67) and stray capacitance about 50 pF total; all other capacitors are switched out. For the 2 MHz through 200 Hz ranges, capacitance is added by relay or transistor switches, table 5-1 lists the capacitance for each range. Below 200 Hz, the capacitance multiplier controls the frequency ranges.

When the continuous, AM, or SCM mode is selected, the Model 91 uses only the top decade of each frequency range which allows a 10:1 frequency change. When the FM/VCG or Sweep mode is selected, the Model 91 locks to the range of the programmed upper frequency. This allows the frequency to be changed a full three decades (1000:1 frequency change). Table 5-1 lists the frequency range for both types of conditions.

Capacitance for the 2MHz, 200 kHz, 20 kHz, and 2kHz ranges is controlled by relay or transistor switches which are enabled by control lines from the boards interface logic. When a control line goes low, the capacitor is switched in. Table 5-1 lists the control lines and their associated ranges and capacitors. Paragraph 5.3.6.4 describes the function generator interface logic.

When non-symmetrical waveforms are selected, the Model 91 switches to the next higher range to compensate for a 1/10th decrease in current source output.

5.3.1.8 Capacitance Multiplier

Lower frequencies require larger capacitors that often fail to maintain the precise value over time needed for accurate frequencies. To eliminate the need for large capacitors, the Model 91 uses a Capacitance Multiplier (schematic 1104-00-3342 sheet 6 of 7) to simulate large capacitors by dividing the current at the TRINODE. When the VCG Current Source supplies current, ISWITCH+, to the Frequency Range Capacitor, the Capacitance Multiplier draws a portion of the current from TRINODE to decrease the charging time. When the VCG Current Source draws current, SWITCH–, from the Frequency Range Capacitor, the capacitance multiplier adds current to TRINODE to decrease the discharging time.

Table 5-1. Range Control and Values >200 Hz

Frequency Range			
CW, AM, and SCM 10:1 - Top Decade	**VCG/FM and Sweep 1000:1 Three Decades**	**Capacitance**	**Control Lines**
20 -2 MHz	20 MHz - 20 kHz	50 pF - (15 pF + Stray) C67	None
2MHz - 200 kHz	2MHz - 2kHz	490 pF - C57, C58, C67	≤$\overline{\text{FR8}}$
200 kHz - 20 kHz	200 kHz - 200 Hz	0.00519 µF - C55,C57, C58, C67	≤$\overline{\text{FR7}}$, ≤$\overline{\text{FR8}}$
20 kHz - 2kHz	20 kHz - 20 Hz	0.05219 µF - C53,C55,C57, C58, C67	≤$\overline{\text{FR6}}$, ≤$\overline{\text{FR7}}$, ≤$\overline{\text{FR8}}$
2kHz - 200 Hz	2kHz - 2Hz	0.52219 µF - C52, C53,C55,C57, C58, C67	≤$\overline{\text{FR5}}$, ≤$\overline{\text{FR6}}$, ≤$\overline{\text{FR7}}$ ≤$\overline{\text{FR8}}$

Table 5-2. Range Control and Values <200 Hz Frequency Range

CW, AM, and SCM 10:1 - Top Decade	**VCG/FM and Sweep 1000:1 Three Decades**	**Resistance**	**Control Lines**
200 Hz - 20 Hz	200 Hz -	10 kΩ - R67	$\overline{\text{FR4}}$
20 Hz - 2Hz	20 Hz - 20 mHz	110 kΩ - R67, R68	$\overline{\text{FR4}}$, $\overline{\text{FR3}}$
2Hz - 200 mHz	2Hz - 2mHz	1.11 MΩ - R67, R68, R69	$\overline{\text{FR4}}$, $\overline{\text{FR3}}$, $\overline{\text{FR2}}$
200 mHz - 20 mHz	200 mHz - 2mHz	11.11 MΩ - R67, R68, R69, R71	All high
20 mHz - 2mHz	20 mHz - 2mHz	See Note	See Note

Note:

The Model 91 does not switch to the 20 mHz range. It actually keeps the same range capacitors as the 200 mHz range, but it decreases the input to the VCG Summing Amplifier by 1/10th effectively dropping down a decade range by switching in, $\overline{\text{SCALE}}$,an additional input resistor (R8) in series with the VFREQ input.

The capacitance multiplier consists of two amplifiers (U23 and U24). The amplifier (U23) acts as a non-inverting amplifier that generates an amplified version of the TRINODE triangle waveform on one side of C62. A capacitor converts a constant slope voltage into a constant current, thus the capacitor (C62) converts the triangle voltage into a current "square wave" at the inverting input of the amplifier (U24). The output of U24, TP11, contains a square wave which is 180° out of phase with the function generator's triangle (figure 5-16). The signal at TP11 is a composite of the out-of-phase square wave and the in phase triangle because the triangle connects directly to the non-inverting input of U24. The output from U24 drives the resistor (R129) with the composite signal. But since both sides of R129 have a triangle signal, the differential signal will be the square wave which causes constant current in R129 in alternating directions with the square wave. When the ISWITCH+ is selected by the diode bridge, most of the charging current is drawn out of the TRINODE through R129 to the negative portion of TP11's square wave. When ISWITCH- is selected, the positive portion of TP11's square wave sources current through R129 to TRINODE. The net effect is the frequency range capacitor is charged and discharged at a slower rate when the relay (K4) switches the Capacitance Multiplier to the TRINODE. Resistors R67, R68, R69, and R71 determine the square current to inverted square voltage gain of U24, and generate the bottom four frequency ranges of the function generator. Refer to table 5-2.

5.3.1.9 Comparator

The Comparator (schematic 1104-00-3342 sheet 7 of 7) compares the output from the triangle buffer, TRIOUT, to the reference square wave level and produces an output that drives both diode gates. Figure 5-17 illustrates a simplified comparator circuit.

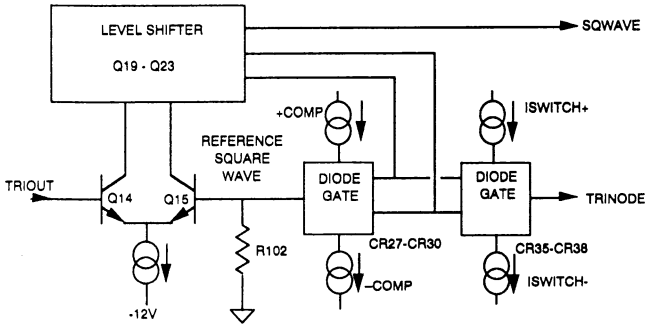


Figure 5-17. Simplified Comparator

The transistors (Q14 and Q15), connected as a differential amplifier, compare the TRIOUT (base Q14) to the reference square wave. The level shifter (Q19, Q20, Q21, Q22 and Q23) converts the input from Q14 and Q15 collector signals into a bipolar signal that can drive the diode gates and the SQWAVE output. Diode gate (CR27, CR28, CR29, CR30) switches between the compensation current sources, +COMP and –COMP, generating the reference square wave (I_{COMP} x R102). The compensation current source is adjustable over a small range in order to provide high-frequency compensation (paragraph 5.3.1.4). Also, the comparator drives the other diode gate (CR35, CR36, CR37, CR38) that switches the VCG current sources, I_{SWITCH} + and I_{SWITCH} –. These currents charge and discharge the Frequency Range Capacitor. Two JFETs (Q25 and Q26) buffer the diode gate (CR27 - CR30) from the I_{SWITCH} + and I_{SWITCH} – current sources.

5.3.1.10 Triangle Buffer

The triangle buffer (schematic 1104-00-3342 sheet 6 of 7) isolates the triangle node, TRINODE, from the buffer's output, TRIOUT. The triangle buffer consists of a source follower (Q11) buffered by an emitter follower (Q12). The circuit provides dc stability by monitoring the input and outputs with U25 and controlling the drain current in Q11 so the V_{CS} remains at 0V. Q13 is the controlled current source.

5.3.1.11 Sine Convertor

The sine convertor shapes the triangle into a sine wave. The convertor actually consists of three circuits; the variable supply, the sine convertor itself, and the sine buffer.

The variable supply (schematic 1104-00-3437 sheet 6 of 6) produces an isolated ±12V, +12VADJ and -12VADJ, used by the sine convertor. To provide minimum sine distortion, the internal calibration network on the motherboard measures the sine distortion and produces a correction voltage, VSINCAL which fine tunes the sine convertor by adjusting the variable supply. The resistor (R97) provides an adjustment of the rations of the variable supply.

The sine convertor (schematic 1104-00-3437 sheet 5 of 6) transforms the triangle from the triangle buffer on the function generator board into a sine wave. The sine convertor uses the logarithmic response characteristic of the ten matched diodes to approximate the sine current output, SINCO (TP13). The resistor (R33) adjusts the sine convertor's input level.

The sine buffer (schematic 1104-00-3437 sheet 5 of 6) converts the sine current supplied by the sine convertor in to two sine wave signals, SIN1 and SIN 3. The signal SIN1 drives the function selector on the output assembly, and provides the carrier for the XY multiplier. Signal SIN3 is routed to the phase lock-loop's sine zero-crossing detector. The resistor R64 adjusts the buffer's dc level. The resistor R208 controls the sine wave amplitude.

5.3.2 Pulse Generator

The Pulse Generator (schematic 1104-00-3438), see figure 5-18, consists of the pulse generator trigger multi-

plexer, delay circuit, width circuit, and pulse register and output circuit. Also, figure 5-18 illustrates signal flow through the pulse generator. Both the delay and width circuits each contain logic circuits and two one-shots. The pulse board also contains the trigger amplifier (paragraph 5.3.5.2), mode logic (paragraph 5.3.5.3), and sync multiplexer and driver (paragraph 5.3.2.4). Figure 5-18 does not show the control lines. The control lines will be described in the circuit level descriptions.

The pulse generator trigger multiplexer selects and routes the pulse trigger sources to the one-shots via the width and delay logic circuits. The one-shot's outputs drive the pulse output multiplexer via the pulse generator output register. The pulse output multiplexer selects the pulse driver signal source. The sync multiplexer selects the appropriate signal (front or rear) for the sync driver. During the normal or single pulse operation, the delay one shot always drives the width one-shot, but the delay one shot is set to a minimum value. For double pulses, the delay one shot triggers the width one shot on the delay one-shots initial trigger and again on the delayed output.

5.3.2.1 Pulse Generator Trigger Multiplexer

The pulse generator trigger multiplexer (schematic 1104-00-3438 sheet 5 of 11) contains the data selector (U14) and "glitcher" (U46A and U15D). The data selector (U14) selects the trigger sources (manual trigger, square wave, frequency synthesizer, and external trigger) to trigger the pulse generator's one-shots. The line, POFF, enables the data selector when high. Each trigger source is selected using control lines from the Processor interface; see table 5-3. The "glitcher" (U46A and U15D) produces a ~3ns wide trigger pulse which gates (U15B and U15C) route to the one-shots.

Table 5-3. Trigger Mux Data Selector

Input line	Function	Control Line	State
PMAN	Pulse Manual Trigger	$\overline{\text{PMANSEL}}$	Low
ESQR	Square Wave	$\overline{\text{SQRSEL}}$	Low
HFSYNTH	Frequency Synthesizer	$\overline{\text{SYNTHSEL}}$	Low
EXTRG	External Trigger	$\overline{\text{EXTSEL}}$	Low

5.3.2.2 Delay and Width One-Shots

The delay and width one-shots each consist of analog and digital one-shots which are selected based on programmed delay and width times. When delays are less than 10 ns (100 ps resolution), the trigger pulse activates the analog one-shot. When delays are greater than 10 ns (10 ns resolution), the trigger pulse triggers the digital one-shot which will trigger the analog one-shot. Also see table 5-4.

Table 5-4. On-Shot Selection

Condition	One-Shot
Delay <10 ns	Delay Analog
Delay >10 ns	Delay Digital
Width 10 - 20 ns	Width Analog
Width >20 ns	Width Digital

5.3.2.2.1 Signal Flow Through the One-Shots

The "glitcher" produces the 3ns, DLYIN, trigger pulse that triggers the delay one-shot. The gates (U15B and C) route the trigger pulse to the delay one-shot's digital, $\overline{\text{DLDGSEL}}$, one-shot or the analog, $\overline{\text{DLALSEL}}$, one-shot. The delay one-shot generates a 4ns pulse, WDIN, relative to the DLYIN trigger pulse. The time between DLYIN and WDIN is the programmed delay.

Gates (U16B and U16C) route the pulse, WDIN, to the width one-shot. These gates select the width's digital, $\overline{\text{WDDGSEL}}$ low, or analog, $\overline{\text{WDALSEL}}$ low, one-shots. The pulse, $\overline{\text{WDIN}}$ low, clears the flip-flop (U17A). The output from the width one-shot, WDPLS, clocks the flip-flop. The $\overline{Q}$ output from the flip-flop supplies the pulse output at the programmed width and delay time. The data selector (U18) routes the pulse, $\overline{\text{PLSSEL}}$ low, from the flip-flop to the normal/complement selector (U19C). The line, COMP, selects either the normal or complement outputs. The selector's differential outputs (PLS and $\overline{\text{PLS}}$) drive the output PIN drivers and the level translator (U19C). The output from buffer (U10C), SQWAVE, drives the Output Board's function selector.

5.3.2.2.2 One-Shot Operation

The Model 91's microprocessor factors the delays into

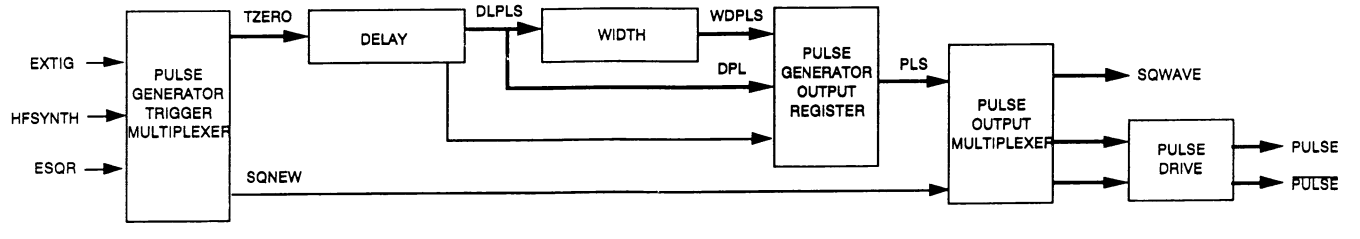


Figure 5-18. Simplified Pulse Generator Block Diagram

"X" 40 ns steps + "Y" 10 ns steps + "Z" ns steps. The Model 91 loads the "X" and "Y" values in the counters and the "Z" value into the analog one-shot. When triggered (DLDIG), the flip-flop (U24A- Delay, U31A - Width) clears enabling the gated oscillator. The Johnson counter counts down "Y" 10 ns, then begins clocking the divide by N (or "X" in this case) counter (U26 - Delay, U32 - Width). This counter then counts down "X" 40 ns steps which resets the flip-flop (U24B - Delay, U31B - Width). Resetting the flip-flop disables the gated oscillator and triggers the analog one-shot. The analog one-shot produces a pulse "Z" ns later. Therefore, the total X*40 ns +Y*10 ns + Z*1ns equals the programmed delay.

The delay and width one-shots (schematic 1104-00-3438 sheets 6 and 7) are identical, thus only the delay one-shot will be described. Both delay and width one-shot reference designators will be listed.

5.3.2.2.3 Analog One-Shot

The analog one-shot, see figure 5- 19, contains the flip-flop (U24A- Delay, U31 - Width), the buffer (U27A - Delay, U33A - Width), the current source (Q1 and Q2 - Delay, Q3 and Q4 - Width), Timing capacitor (C17 - Delay, C26 - Width), Comparator (U27B - Delay, U33B - Width), and output buffer (U27C - Delay (U33C - Width). The *letters* used in figure 5-19 correspond to the timing diagram; figure 5-20.

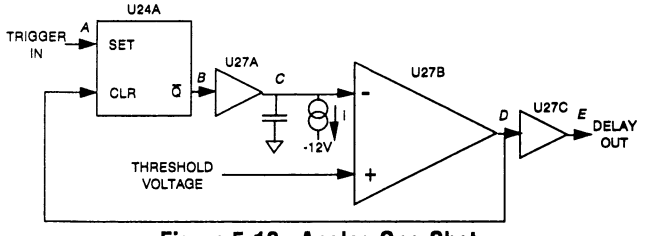


Figure 5-19. Analog One-Shot

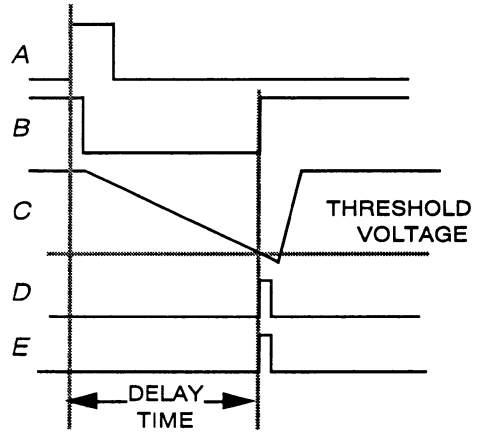


Figure 5-20 Analog One-Shot Timing Diagram

In its quiescent state, the $\overline{Q}$ output of the flip-flop (U24A) sits at a logic high which allows the capacitor (C17) to charge to about 4.1V. The buffer (U27A) isolates the capacitor from the $\overline{Q}$ output. When triggered (*A*), $\overline{Q}$ switches to a logic low (*B*) causing the capacitor (C17) to discharge through the current source producing a linear ramp. Transistor, Q1, buffers C17 from the current source. Comparator, U27B, monitors the ramp and reset the flip-flop, U24A, when the threshold level is reached (DANALVL - Delay, WANALVL - Width). Resetting U24 causes the rapid recharging of C17 to 4.1V. When the capacitor is recharged, the comparator produces a pulse (*D*). The time delay between the trigger pulse (*A*) and the output pulse (*E*) is proportional to the threshold voltage (DANALVL) and the value of the capacitor, C17, and inversely proportional to the discharging current. The threshold voltage determines the time delay because both the discharge current and capacitor, C17, are fixed.

The threshold voltages, the "Z" value described in paragraph 5.3.2.2.2 ,originate from the Level Control DAC and runs through the Analog One-Shot Control amplifier (schematic 1104-00-3438 sheet 10 of 11).

5.3.2.2.4 Digital One-Shot

The digital one-shot contains a gated oscillator (figure 5-21), Johnson counter, and +N counter (1104-00-3438 sheets 6 and 7).

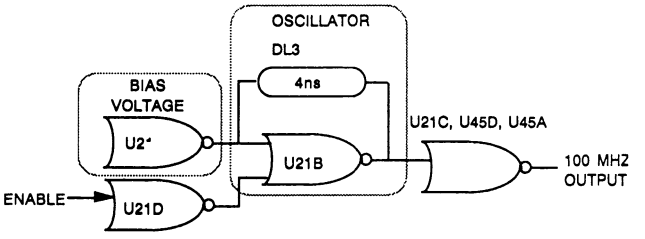


Figure 5-21. Gated Oscillator

The gated oscillator (U21B and DL3 - Delay, U28B and DL4 - Width) generates the 100 MHz clocks for the counters. The 4ns delay line (DL3 - Delay, DL4 - Width) and the propagation delay of U21B/U28B determine the oscillator's frequency. The exact frequency is unimportant, because during AutoCal the microprocessor section measures the frequency and stores a correction value.

The Johnson counter (U22 and U23 - Delay, U29 and U30 - Width) divides the 100 MHz clock (10 ns) by four providing the 40 ns clock for the 25 MHz Divide by N counter.

The microprocessor sends data, $\overline{DH14}$, $\overline{DH23}$, $\overline{DH12}$, $\overline{DH34}$, via the pulse generator's interface to the Johnson counter which represents the "Y" value. Thus, this counter counts down "Y" times 10 ns steps before triggering the analog one-shot.

The 25 MHz divide by N counter (U26 - Delay, U32 - Width) is loaded with serial data (SDATA) from the pulse genera-

tor board's interface. This counter steps down "X" times 40 ns steps before triggering the analog one-shot (see paragraph 5.3.2.2.3).

5.3.2 3 Pulse Output Amplifier

The pulse generator's output amplifier is a pin driver (U40) that converts the pulse generator's fixed outputs, PLS and $\overline{\text{PLS}}$, into pulses with adjustable upper and lower levels. Refer to schematic 1104-00-3438 sheet 11 of 11. The pulse generator's outputs, a differential ECL output, are level shifted by a differential amplifier (Q9 and Q10) to a 0 to +1V acceptable to the pin driver's inputs. The pulse output level is set by the pulse upper level lines, PULVL and $\overline{\text{PULVL}}$, and lower level lines, PLLVL and $\overline{\text{PLLVL}}$. These levels are not accurate, during AutoCal the microprocessor section measures offset and gain errors of the pin driver and stores correction values.

The pin drivers have special power supplies that can be shut down by a temperature monitoring circuit. The temperature sensor, which is attached to the pin driver, produces a 10 mV/degree output (schematic 1104-00-3438 sheet 8 of 11). When the temperature exceeds a threshold set by resistors R86, R87, R88, and R89, U41B changes state ultimately causing the lines, FAULT1 AND FAULT2, to shut down the pin driver's power supplies. The supplies shut off at 100°C turns back on when the temperature drops below 80°C.

The upper and lower level control voltages originate from the Level Control DAC (schematic 1104-00-3438 sheet 9 of 11). The microprocessor writes the voltage and DAC number to the level DAC (U34) via a three wire serial data link; SDATA, SCLK, and DACEN. The DAC's outputs, OUT 1 through OUT4 set the PULSE and $\overline{\text{PULSE}}$ upper and lower levels.

5.3.2.4 Sync Selector and Driver

The sync circuit (schematic 1104-00-3438 sheets 5 and 8) consists of a data selector, U20, which selects one of four sync sources. The unit's firmware selects the best sync source based on the unit's operating mode and function. At frequencies below 20 MHz (function generator modes and functions), the trigger sync selector line ($\overline{\text{TRGSYSL}}$) goes low to enable the ECL trigger source (ETRGS) from the mode control circuit as the sync source. For pulse functions, the output from the pulse generator trigger multiplexer drives the data selector and time delay circuit. When the delay select 0 select line ($\overline{\text{DLSEL}}$) goes low, the multiplexer's output supplies the sync signal. The time delay circuit; U46B, DL1, and DL2; provides selectable delays of 10 ($\overline{\text{DL20SEL}}$ goes low) and 50 ns ($\overline{\text{DL40SEL}}$ goes low). The data selector, U20, supplies a ECL differential output that is translated into single ended TTL levels by the differential amplifier, Q5 and Q6. The resistors, R106 through R109, terminate the data selector's outputs. The transistors, Q5 and Q6, function as a current switch that drives the current through R28 directly to ground via Q5 or through the parallel combination of R99 and the 50Ω sync output termination. Important: the Sync Output must be terminated into 50Ω for proper operation.

5.3.2.5 Square Waves

For square waves below 20 MHz, the Pulse Generator Trigger Multiplexer (U14) routes the square wave, ESQR, directly to the data selector (U18) when SQRSEL goes low. For square waves above 20 MHz, the Pulse Generator Trigger Multiplexer (U14) routes the frequency synthesizer, HFSYNTH, directly to the Pulse Output Multiplexer (U18) when $\overline{\text{SYNTHSL}}$ goes low. The Pulse Output Multiplexer routes the square wave through the Pulse Output, PLS and $\overline{\text{PLS}}$, to the Normal/Complement selector, when SNEWSEL goes low. If front panel outputs are used (≤20 MHz) the square wave drives the Output Board's Function Selector. If the rear panel outputs are used (≤100 MHz), the square wave drives the pin driver. See figure 5-22.

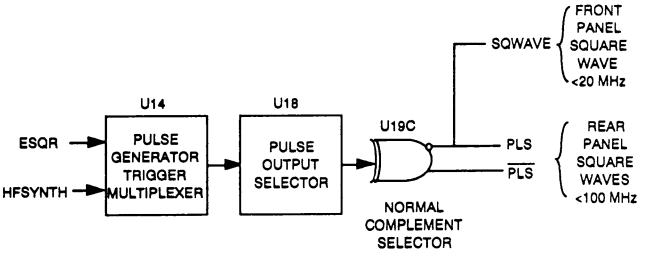


Figure 5-22. Square Wave

5.3.2.6 External Width

When the external width mode is selected, the EXTRG line from the Trigger Amplifier drives the Pulse Generator Trigger Multiplexer ($\overline{\text{EXTSEL}}$ goes low) This routes the trigger amplifier output directly to the Pulse Output Multiplexer. From the Multiplexer, the signal runs to either the front or rear panel outputs. The external width waveform characteristics depends on the trigger level and slope. See figure 5-23.

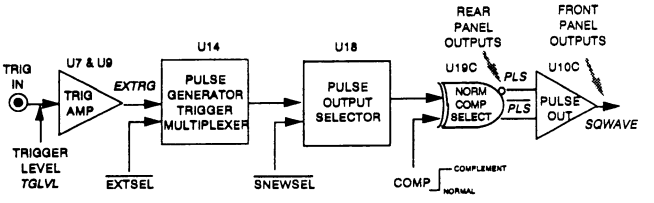


Figure 5-23. External Width

5.3.3 OUTPUT SECTION

5.3.3.1 General

The Model 91's output section (see figure 5-21) consists of nine circuit blocks: the Function Selector with Square Shaper, XY Multiplier, AM Summing Amplifier, Preamplifier, Power Amplifier, 0/20 dB Attenuator, Balanced Output Drivers, Unbalanced Output Attenuator Network and Impedance Control, and Balanced Output Attenuator network and Impedance Control. The output section, shown in figure 5-21, is located on three separate assemblies in the Model 91: Phase Lock Loop board, Output board and Motherboard. In figure 5-24, the bold lines represent the signal flow through the Output section. The waveform, selected by the Function Selector, flows through the XY Multiplier where its amplitude is determined by the amplitude controlling signal. The waveform is then amplified and routed through attenuators to the selected output connector.

5.3.3.2 Square Shaper and Function Selector

The square shaper (schematic 1104-00-3335 sheet 2 of 6) converts the TTL level square wave or pulse signal (SQWAVE) from the Pulse Generator to a bipolar, 2Vpp square wave. The shaper's input is a non-saturating input transistor (Q1), which produces fast switching edges. This transistor drives the level shifter (Q5 and Q6) whose output is a 3Vpp square wave which switches the diode gate (CR3 - CR6). The gate switches the positive and negative current sources which drive the load resistor (R16T). The +2 amplifier (U11) buffers the square wave and drives the Function Selector. The square wave level is approximately 1Vpp at TP1. The two transistors Q2 and Q4 are used to enable and disable the Square Shaper. When the SQRON line goes high, the Square Shaper is enabled.

The function selector circuit selects and routes either the Sine (SIN1), Triangle (TRIOUT), square (2Vpp SQUARE), or pulse (OPTSIG) waveform to the preamplifier, PREAMPIN. The function selector, located on the Output board, consists of four relays (K1 - triangle, K2 - square, K3 - sine, and K4 - OPTSIG (Pulse) (schematic 1104-00-3335 sheet 2 of 6)). Microprocessor Section (schematic 1104-00-3440 sheet 3 of 10) switches the relays via the interface latch (U2 - schematic 1104-00-3335 sheet 1 of 6). When one of the relay control lines ($\overline{SINSEL}$, $\overline{TRISEL}$, $\overline{SQSEL}$, $\overline{OPSEL}$) goes low, the relay will be closed. Only one relay will close at a time. In addition, the function selector terminates each waveform input and sets the amplitude of each waveform to approximately 1Vpp using resistor networks.

5.3.3.3 XY Multiplier and Preamplifier

The XY Multiplier and Preamplifier (schematic 1104-00-3335 sheet 3 of 5) control or modulate the amplitude of the selected function. The multiplier's Y input receives it's input (PREAMPIN) from the function selector. All function levels are about 1Vpp. The AM Summing Amplifier on the Phase Locked Loop board (schematic 1104-00-3437 sheet 6 of 6) supplies the multiplier's X input, AMSIG. A dc level at the X input controls the generator's amplitude level, and an ac signal modulates the generator's amplitude. The ±6V Supplies (U14A, U14D, Q27, and Q26) provide the power for the XY Multiplier.

The multiplier (U4) is a wide-band device producing differential output currents which are the product of the PREAMPIN signal and the AMSIG input. The resistors (R33 and R34) convert the multiplier's output current into voltage. A pair of Darlington emitter followers (Q22, Q23, Q24, and Q25) buffers the signal from the XY Multiplier's output and drives the differential amplifier (U5). The differential amplifier (U5) converts the differential output from the emitter followers to a single-ended output, PREOUT, of about 6Vpp (full amplitude). PREOUT is offset about +3.5 Vdc to compensate for offsets in the multiplier circuit. The multiplier offset circuit (U14C and U12) supplies a compensation voltage, COMPOUT, to the output amplifier which compensates for offset in the PREOUT signal.

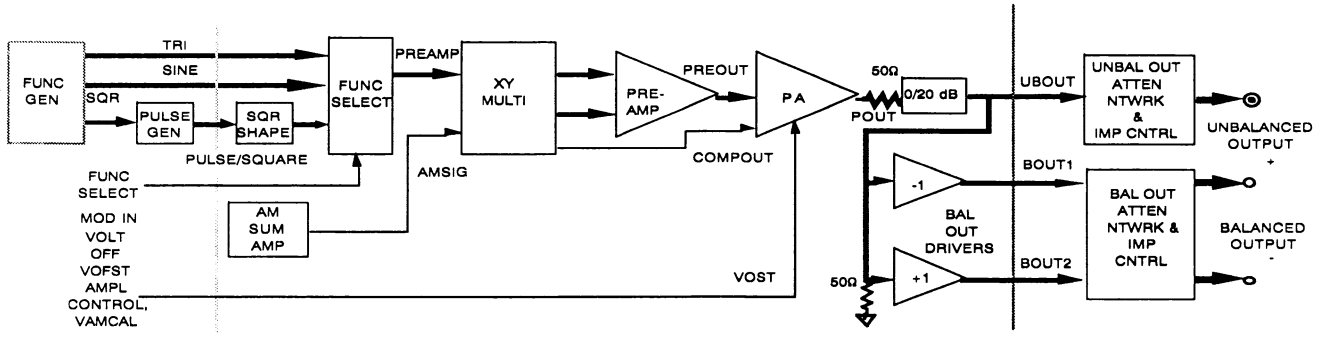


Figure 5-24. Output Section Block Diagram

5.3.3.4 Output Amplifier

The power amplifier (schematic 1104-00-3335 sheet 4 of 6) is a fixed gain, wide-band inverting amplifier with a complimentary symmetry output stage. This amplifier provides the current and voltage needed to drive the unit's outputs. The Output Amplifier has three signal inputs: PREOUT, COMPOUT, and VOFST. PREOUT is the selected function from the Preamplifier. COMPOUT is the multiplier compensating voltage from the multiplier's offset circuit. VOFST supplies the offset voltage to either dc offset the waveform or dc output level. VOFST is generated by the DAC Sample and Hold Network on the Motherboard. Both the COMPOUT and VOFST inputs contain inductors which improve the transient response.

The power amplifier has two distinct signal paths: the ac path and the dc path. The ac path provides the wide-band and high speed required by the unit's output. The ac path routes the signal through C36, C49, and the emitter followers (Q12 and Q16) to the current sources (Q13 and Q17). Emitter followers (Q14, Q15, Q18, and Q19) buffer the current source from the PAOUT and feedback resistor (R79 and R80). The dc path provides the low frequency path and dc stability of the output amplifier. The dc path runs through the differential amplifier (Q9 and Q10). DC gain rolls off with frequency (about 80 kHz). The RC network (C31 and R47) determines the roll-off frequency. The differential amplifier (Q9 and Q10) drives the inverting stage of Q11 whose output adjusts the dc bias of the current source. The amplifier's 50Ω output impedance is set by the resistors (R95, R96, and R97). PAOUT also drives the Output Board's Peak Detector.

5.3.3.5 –20 dB Attenuator

The –20 dB attenuator circuit (schematic 1104-00-3335 sheet 5 of 6) together with the XY Multiplier and -40 dB Attenuators (Motherboard) controls the level of the output waveform. The -20 dB attenuator attenuates the power amplifier's PA OUT signal by switching in or out resistors R98 through R108. The microprocessor circuit via the Output board's data register (U3) closes the relay (K5) when the $\overline{\text{ATTEN-20}}$ goes low. R169T and C105T improve the transient response of the attenuator.

5.3.3.6 Balanced Drivers

Relay K6 (schematic 1104-00-3335 sheet 5 OF 6) selects either the Balanced or Unbalanced output and routes the signal from the –20 dB attenuator to either the Unbalanced Output Attenuator Network and Impedance Network or to the Balanced Drivers. If balanced output is selected, the signal is routed through two amplifiers which produce two 180° out of phase signals, BOUT1 and BOUT2. The amplifier (U6) is a unity gain inverting amplifier. The other amplifier (U7) is a unity gain, non-inverting amplifier. The 50Ω source and load (R104 - R108) reduce the input level by 1/2 which produces a net gain of ±1/2 in the two amplifiers. The two outputs, BOUT2 and BOUT1, run to the Balanced Output Attenuator Network and Impedance Control (Motherboard). Both signals also drive the Peak Detector.

The balanced/unbalanced relay (K6) is controlled by the BAL-UB line from the latch (U3). When the BAL-UB line goes low, the Unbalanced output is selected. When the line goes high, the Balanced output is selected.

5.3.3.7 Unbalanced Output Attenuator Network and Impedance Control

The Unbalanced Output Attenuator Network and Impedance Control block on the Motherboard (schematic 1104-00-3395 sheet 7 of 10) serves two functions. It selects the output impedance of the instrument and provides 0dB or -40 dB of attenuation.

If the unbalanced output is selected, the UBOUT signal from the Output Amplifier goes through a -40 dB attenuator (K1 – R69 through 74). The relays (K2 and K3) and their associated resistors select the output impedance (50Ω, 75Ω, or 600Ω). The relay (K6) opens the output when the Unbalanced Output is turned off. The output from this block drives the Unbalanced Output connector.

The attenuator relay (K1) is switched when U30 pin 15 goes low. When K2 and K3 are disabled (U30 pins 14 and 13 high), the output impedance is 50Ω. When relay K2 is disabled (U30 pin 14 high) and relay (K3) is enabled (U30 - pin 13 low), the output impedance is 75Ω. When both K2 and K3 are enabled (U30 - pins 14 and 13 low), the output impedance is 600Ω.

5.3.3.8 Balanced Output Attenuator Network and Impedance Control

The Balanced Output Attenuator Network and Impedance Control block on the Motherboard (schematic 1104-00-3440 sheet 7 of 10) serves two functions. It selects the output impedance of the instrument and provides –40 dB of attenuation.

If the balanced output is selected, the BOUT 1 and BOUT2 signals from the Balanced Driver are routed .through the –40 dB attenuator (K4 along with resistors R80 through R89). The relay (K5 and its resistors) select the output impedance (135Ω and 600Ω). The output from this block drives the front panel's Balanced Output connectors.

The attenuator relay (K4) is switched when U30-pin 19 goes low. When K5 is disabled (U30 - pin 12 high), the balanced output impedance is 135Ω. When K5 is enabled (U30 - pin 12 low), the output impedance is 600Ω.

The control line, $\overline{POE}$, from the Microprocessor resets the attenuators to -40 dB at power up or power down.

5.3.4. Frequency Control

5.3.4.1 Introduction

Frequency Control covers those items affecting the Model 91's frequency . These items include the primary frequency control - VFREQ, the sweep generator, the phase lock loop and synthesizer, and Mod In (FM/VCG).

5.3.4.2 VFREQ

The VFREQ line is the Model 91's basic frequency control. The line originates at the Motherboard's DAC Sample and Hold Network (paragraph 5.3.6.5) and runs to the Function Generator's VCG Summing Amplifier (paragraph 5.3.1.2). The VFRQ is a dc voltage between +8 Vdc and +0.8 Vdc which represents the programmed frequency of the unit. VFREQ controls the frequency in the Continuous and AM modes. For FM, VFREQ sets the center frequency. For VCG, VFREQ sets the minimum frequency. For sweep mode, the VFREQ sets the start frequency.

5.3.4.3 Sweep Generator

The Sweep Generator (schematic 1104-00-3342 sheet 2 of 7) consists of an 8-bit DAC (U7A) and its buffer amplifier (U8) which produces the sweep voltage (0 to +8V) for the function generator. Another part of the sweep generator, DAC (U7B), supplies the sweep output ramp to the Sweep Out connector. VFREQ from the DAC Sample and Hold Network sets the Function Generator to the start frequency (paragraphs 5.3.4.2 and 53.1.2). Another dc voltage from the DAC Sample and Hold Network, VSLEN, provides the reference for the sweep DAC (U7A). To produce the sweep, the Microprocessor sends sweep DAC data (0000 0000 to 1111 1111 for sweep up or 1111 1111 to 0000 0000 for sweep down) representing the sweep voltage for the function generator. The programmed sweep time determines microprocessor generated data rate. The Microprocessor also sends the data to produce the sweep shape: linear or logarithmic sweep. The sweep DAC is hardwired in the write mode. The sweep DAC receives data input when the $A/\overline{B}$ and $\overline{DS2}$ lines are high, and the $\overline{DS1}$ line is low.

The DAC (U7B), part of the Sweep Generator DAC, and amplifier (U6B) supplies the SWEEP OUT ramp. The Microprocessor writes data (0000 0000 to 1111 1111 for sweep up or 1111 1111 to 0000 0000 for sweep down) to the DAC when the $\overline{DS1}$ and $A/\overline{B}$ lines are low, and $\overline{DS2}$ line is high. The shape of the output will always be linear regardless of whether linear or log sweep is selected. The sweep time determines the rate of the data from the Microprocessor. The DAC reference voltage, supplied by Zener diode (CR1) is –6 Vdc.

5.3.4.4 Synthesizer - Phase Lock Loop

5.3.4.4.1 Introduction

The Synthesizer - Phase Lock Loop controls the frequency of the function generator by comparing the frequency of outputs from the function generator against a frequency reference resulting in a correction voltage which drives the function generator; see figure 5-25. The Synthesizer - Phase Lock Loop circuit consists of six blocks located on three assemblies.

The phase detector compares the frequency from the variable source (function generator) with the reference source (Frequency synthesizer or external frequency input). The detector produces an output that is filtered by the Lock Loop Filter. The filter's output provides a correction signal, VLOOP, to the function generator which will alter the function generator's frequency.

5.3.4.4.2 Frequency Sources

Variable

Variable sources originate at the function generator and are selected by the source selector (paragraph 5.3.4.4.3). The square wave is routed directly to the phase detector. Both the sine and triangle waves are routed through a zero crossing detector.

The Sine/Triangle Zero Crossing Detector (schematic 1104-00-3437 sheet 2 of 6) converts the sine wave or triangle signal, ZCSIG into a square wave. As the signal passes through its zero crossing point, the crossing detector's output level changes high or low producing a square wave. This output is one of the input signals, Z-CROSS, to the source selector circuit. The zero crossing detector consists of a high speed comparator. Its feedback resistors (R2 and R3) ensure noise immunity. Two control lines, SELA and SELB, enable the Zero Crossing Detector.

Reference Sources

Frequency Synthesizer - Internal Source

The frequency synthesizer (see figure 5-26) supplies the internal lock source for the Model 91's phase lock loop. In addition, the frequency synthesizer generates the internal trigger source as well as the pulse generator's trigger. The frequency synthesizer consists of a phase detector which drives the VCO (Voltage Controlled Oscillator) via the Loop Filter. The VCO produces frequencies between 25.000 MHz and 50.000 MHz in 1kHz increments. Below 25 MHz, the synthesizer divides the 25 to 50 MHz output down to the programmed frequency.

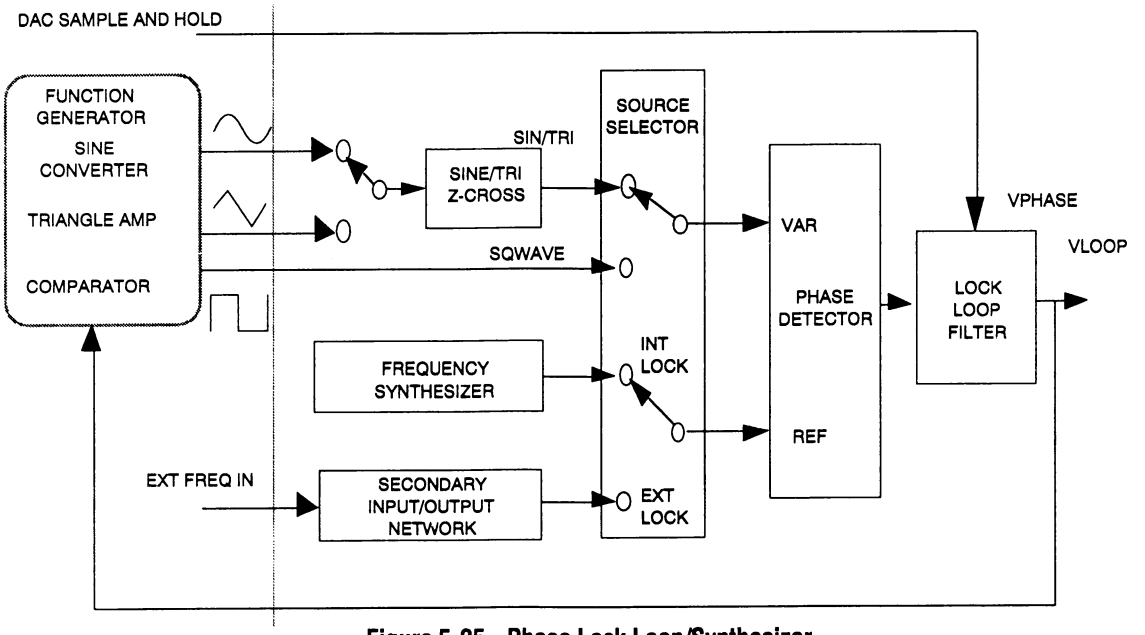


Figure 5-25. Phase Lock Loop/Synthesizer

The frequency synthesizer provides two sets of outputs: SYNTH and HF SYN. The SYNTH line supplies botn the Internal trigger source and internal reference for phase detector. The line, HF SYN, triggers the pulse generator.

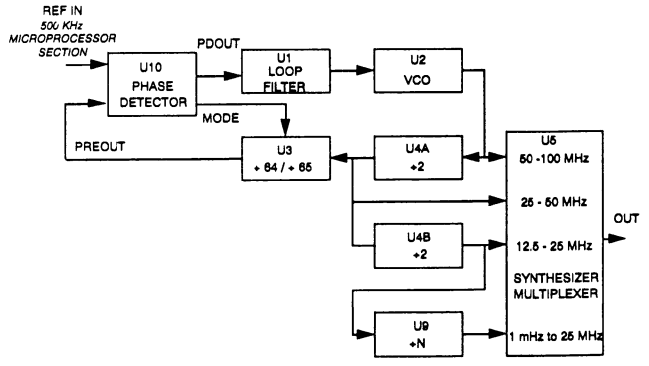


Figure 5-26. Frequency Synthesizer

Frequency Synthesizer References

The standard reference for the frequency synthesizer originates from the Microprocessor Section's Processor Support Chip via the SHCLK line (schematic 1104-00-3440 sheet 3 of 10). The motherboard routes the SHCLK line to the 2:1 multiplexer (U36 - schematic 1104-00-3440 sheet 4 of 10) which routes the signal to the Synthesizer board as REF IN. This provides the standard reference source to the frequency synthesizer (schematic 1104-00-3460 sheet 3 of 3).

The optional TCXO (schematic 1104-00-3466) supplies the 500 kHz reference, 500KHZ, for the frequency synthesizer. In addition, it detects the presence of an external 10 MHz reference and provides a 10 MHz reference output. The external frequency reference connects to the rear panel TRIG IN connector . The comparator (U1) squares up the input signal, converting the signal to TTL levels. A parallel resonant tank circuit comprised of L2 and C6 rejects reference signals outside of the 9 to 11 MHz range. The diode (CR1) and capacitor (C7) peak detect the tank's output and, if the external reference is correct, turns on Q1. The gates (U4A, U4C, and U4B) form a multiplexer that selects either the external reference signal or the TCXO's output. The TCXO (U2) is a temperature stabilized crystal oscillator with a 10 MHz output. The output buffer (Q3 and Q4) drives the Ref Out connector.

Frequency Synthesizer's Phase Detector

The phase detector (U10) contains the control circuitry and programmable dividers required for operation as a dual modulus prescaled phase lock loop; see schematic 1104-00-3460 sheet 3 of 3). The detector receives its 500 kHz input, REFIN, from the microprocessor section on the motherboard. If installed, the optional TCXO supplies the reference. The detector's output, PDOUT, drives the loop filter. Also, the detector supplies a buffered 500 kHz reference, REFOUT back to the motherboard. A divider internal to the detector divides the reference by 500 down to 1kHz. The detector also supplies a buffered 1kHz output, FVAR to the motherboard. Another output from the detector (LD, U10 pin 7) drives the UNOCK indicator. The detector also controls the division ratio (+65 or +64) of the prescalar (U3).

Frequency Synthesizer's Loop Filter

The loop filter for the frequency synthesizer controls the dynamics of the synthesizer loop and removes unwanted frequency sidebands (see schematic 1104-00-4360 sheet 1 of 3). The filter, U1A determines the loop dynamics (overshoot and settling time). Filter (U1B) is a second order, low pass filter that removes the reference frequency sidebands from the VLOOP signal that controls the VCO's frequency.

Frequency Synthesizer's VCO

The Voltage Controlled Oscillator (U2) produces the 50 to 100 MHz output for the frequency synthesizer. The VCO (U2) provides the gain around the resonant circuit formed by the inductor (L1) and Varactor diode (CR1). The varactor's diodes capacitance is inversely proportional to its reverse bias voltage. Changing the voltage on the cathode of CR1 varies the output frequency of U2. The VCO's tuning range is about 2.5 to 1 (45 to 110 MHz). Diodes (CR2 and CR3) form a clamp that prevents the varacter from becoming forward biased by the loop filter (U1) at power on. The output from U2 drives both the multiplexer (U5) and Divide by 2 flip-flop (U4A).

Counters and Dividers

At power on, the Model 91's microprocessor writes a serial data stream to the input decoder (U8), programmable divider (U9), and phase detector (U10) to initialize the counters. Each time the unit's frequency is changed, the microprocessor recalculates the programmed value and loads the new frequency data into U9 and U10. At the same time range data is loaded into U8.

The divide by two flip-flop divides the VCO's output in half producing the 25 to 50 MHz output. This flip-flop's output, VCO/2, drives the multiplexer (U5), the divide by four flip-flop (U4B), and the +64/65 prescalar (U3).

The divide by four flip-flop (actually divide by two) divides the VCO/2 input in half producing the 12.5 to 25 MHz output, VCO/4. The flip-flop's Q and Q/ outputs drive the differential amplifier (Q1 and Q1) which converts the ECL outputs into TTL levels, DNC IN, required by the programmable divide by N divider (U9).

Multiplexer

The frequency range multiplexer (U5) selects the pulse trigger frequency. The multiplexer receives its control line from the serial to parallel convertor (U8). The following lists the control lines and the frequency ranges they select.

Frequency Range	Line
50 to 100 MHz	$\overline{FR4}$
25 to 50 MHz	$\overline{FR3}$
12.5 to 25 MHz	$\overline{FR2}$
1mHz to 12.5 MHz	$\overline{FR1}$

The gates (U11) form a 2:1 multiplexer that selects either the 12.5 to 25 MHz range or <12.5 MHz for the SYNTH line. The SYNTH line drives the other phase detector (paragraph 5.3.4.4.4) via the source selector (paragraph 5.3.4.4.3). This line also supplies the internal trigger source.

External Frequency Input

An external input connected to the EXT FREQ In connector runs through the Secondary Input/Output Network (schematic 1104-00-3440 sheet 6 of 10) to the Source Selector (paragraph 5.3.4.4.3) which drives the phase detector. In the Secondary Input/Output Network, the external frequency signal squares the signal and compensates the signal for any non-symmetry.

5.3.4.4.3 Source Selector

The source selector circuit (schematic 1104-00-3437 sheet 2 of 6) selects one of each set of frequency sources as inputs for the phase detector.

Reference Frequency Sources

SYNTH	Internal frequency synthesizer
BXFREQ	External reference source (TRIG/LOCK IN connector)

Variable Frequency Sources

SQWAVE	Square wave
PLS/SQR	Not used
Z-CROSS	Sine or triangle wave converted to square wave

Two control lines, SELA and SELB, to the Source Selector choose the frequency sources. One reference frequency source and one variable frequency source will be selected. When SYNTH is selected, SQWAVE will also be selected. When BXFREQ is selected, either of the three variable frequency waveforms can be selected. The $\overline{LOCK}$ line enables (low) the Source Selector.

5.3.4.4.4 Phase Detector

The Phase Detector consists of two bi-quinary (+2 and +5) Counters, the Phase Comparator, and the Charge Pump (schematic 1104-00-3437 sheets 2 and 3 of 6). Each input to the Phase Comparator runs through the +10 (20 - 2MHz range) or the +2 (all other ranges) counters (U4A and U4B) prescaling the input frequency. The phase comparator, a PAL, compares the reference frequency signal and the variable frequency signal, and produces an output based on edge arrival times of each monitored signal. The comparator generates one of three possible output conditions using the VLAGR and VLEADR lines. These lines drive the charge pump.

The Charge Pump (schematic 1104-00-3437 sheet 3 of 6) controls the current to and from the Lock Loop Filter. The Charge Pump consists of a diode gate (CR2 - CR5), a positive current source (Q1), and a negative current

source (Q2). The diodes (CR1 and CR6) provide temperature compensation for their respective current sources. The VLAGR and VLEADR inputs from the phase comparator switch the charge pump current. The duration and direction of current represents the phase difference between the selected reference frequency signal and the variable frequency signal. The time difference between the edges determines the amount of current pumped into the lock loop filter. The phase difference between the edges determines the direction of current flow. When the signals arrive concurrently, no current is pumped to the Lock Loop Filter.

5.3.4.4.5 Lock Loop Filter

The Lock Loop Filter circuit (schematic 1104-00-3437 sheet 3 of 6) converts the pulsating current from the Charge Pump into a dc error voltage, VLOOP. The error voltage, VLOOP, gradually changes the VCG Summing Amplifier output signal, VSUM, to match the generator frequency and phase with the reference frequency.

When the reference to generator frequency difference is too large for the system to handle, the UNLOCK indicator on the front panel will flash. When FM or sweep modulation is selected, the $\overline{\text{LOCK}}$ line is high, opening the VLOOP line, and the UNLOCK indicator remains on.

The filter characteristics of the circuit are controlled by the Microprocessor Section, based on the signal frequency. Solid state switches (U17A - U17D) select the various filter circuit combinations. VPHASE supplies the voltage that varies the phase (PHASE key or PHASE command).

5.3.5 Mode Control

5.3.5.1 Introduction

Mode Control (schematic 1104-00-3438 sheet 4 of 11) turns on and off the Function Generator Loop (paragraph 5.3.1) via the control line, RUN. The Mode Control consists of the Mode Control GAL (U9), Burst Counter (U13), and Trigger Amplifier (U7), Trigger Control (U12A), as well as the board I/O logic (schematic 1104-00-3438 sheet 2 of 11).

5.3.5.2 Trigger Amplifier

The trigger amplifier (U7 - schematic 1104-00-3438 sheet 3 of 11), a high speed comparator, compares the Trig In signal against the TRGLVL voltage. TRGLVL, trigger level, is a 0 to 5V level proportional to the programmed -5V to +5V trigger level. The resistors (R3 and R117) provide an offset current shifting the trigger level range. The diodes (CR2 and CR3) protect the comparator's input by limiting the voltage swing to ±0.7V. The resistors (R4 and R5) provide a small amount of hysteresis around the comparator, providing noise immunity. The comparator supplies negative ECL output which drives the Zener diodes (CR4 and CR5). These diodes shift the levels to positive ECL levels. The buffer (U8B) isolates the Zener diodes from the slope selection circuits. The slope selection circuit (U9A and U9B) selects the trigger slope by enabling either the true, $\overline{\text{PSLOPE}}$ low, or complement, $\overline{\text{NSLOPE}}$ low, comparator's output, EXTRG. EXTRG drives the pulse generator trigger multiplexer. EXTRG also drives the differential output amplifier (U9D). These differential outputs, AXETRG and $\overline{\text{AXETRG}}$, drive the mode control. Trigger Control (U12A), a JK Flip Flop, provides the RUN line that controls the operation of the Function Generator (Trigger Baseline Compensation -paragraph 5.3.1.5).

5.3.5.3 Mode Control

The Mode Control (U9 - 1104-00-3438 sheet 4 of 6), a programmed GAL, controls the function generator's operating mode. The input lines, MCNTL1 and MCNTL2 select the operating mode, and the input line, SRCNTL, selects the trigger source. SRCNTL low selects External Source, BXFEQ, and SRCNTL high selects Internal Source, SYNTH. Another line, MANTRIG, represents pressing the MAN TRIG key or its GPIB equivalent. The BURST line from the Burst Counter controls Mode Control in the burst and internal gate modes. Table 5-5 describes the relationship between the Mode Control input control lines and the selected modes. Mode Control produces three control lines; RSET, JSET, and KSET; for the trigger control.

Table 5-5. Mode Control

Control Line	Cont Mode	Trig Mode	Int Gate Mode	Ext Gate Mode	Burst Mode
MCNTL1	0	0	1	0	1
MCNTL2	0	1	1	1	1

When the gate or burst modes are selected while using pulse functions, the mode control uses the function generator, ESQR, as the pulse generator's trigger source.

5.3.5.4 Trigger Control

Continuous Mode To place the function generator in the continuous mode, the Mode Control holds its RSET line low which forces the Trigger Control's RUN line high and allows the function generator to run.

Triggered Mode For the triggered mode, the Mode Control strobes the RSET line low to start the function generator after a triggering event. Also, the Mode Control holds JSET line low and KSET line high. The next negative transition of the SQR (square) from the function generator clocks the Trigger Control, which changes the RUN line to low and turns off the function generator. The function generator will always complete a full cycle.

Internal Gate and Burst Mode Internal gate mode is actually a burst mode. The Model 91 determines what should be the correct number of cycles for 50% duty cycle of the

internal gate frequency, and sets up the Burst Counter. The Mode Control strobes the RSET line low which starts the function generator. Also, the Mode Control places JSET high and KSET low. Once the Burst Counter determines the correct number of cycles has occurred, it places the Mode Control's BURST high which sets JSET low and KSET high until the Trigger Control's QNOT line goes high.

External Gate The Mode Control strobes the RSET line low which starts the function generator. Also, the Mode Control holds JSET high and KSET low as long as the trigger input is true. When the trigger input goes false, JSET goes low and KSET goes high until the QNOT goes high.

5.3.5.5 Burst Counter

The Burst Counter (U13), a programmable +N down counter, signals the Mode Control when the programmed number of cycles is completed. The Microprocessor loads the serial data, BRSDIN, into the Burst Counter using the serial clock, BRCLK when the serial input is enabled, SRSEN. The counter, when clocked, BRCP, counts down to zero and the BURST line to the Mode Control goes low, indicating that the burst has been completed.

5.3.6 Microprocessor And Interfaces

5.3.6.1 Introduction

The Microprocessor and its interfaces provides the data processing and routing throughout the Model 91. This block includes the Microprocessor Section, Function Generator Interface, Pulse Board Interface, Phase Lock Board Interface, Output Board Interface, Front Panel (Keyboard and Display) Interface, and the GPIB Interface. All interfaces, except the GPIB interface, are located on individual boards. Also, the DAC Sample and Hold Network and Internal Calibration Network operate with the Microprocessor Section. Figure 5-27 illustrates the relationship between the Microprocessor Section and Interfaces, as well as lists the Interface's enabling lines and data busses.

5.3.6.2 Microprocessor Section

The Microprocessor Section (schematic 1104-00-3440 sheet 3 of 10) controls all operations within the Model 91. The Microprocessor Section consists of the Microprocessor, Read Only Memory - ROM, Calibration/Scratch Pad Memory, and Processor Support Chip, plus support circuits. The Microprocessor section receives its input data from the front panel or GPIB interface, processes the data, and provides data and control lines for internal operation. Figure 5-28 provides a simplified look at the Microprocessor Section.

The microprocessor (U6) executes operating instructions based on firmware stored in the ROM (U12). Another memory, the Calibration/Scratch Pad RAM (U11) stores the calibration data taken during Auto Cal and manual calibration. This memory also stores the instrument setup at power off and ten stored settings, as well as providing a temporary storage register during data processing. The RAM accepts data (writes) when its WE line goes low. If the WE line is high, the microprocessor section reads data from the RAM. A RAM backup battery (BT1) prevents the loss of data when power is turned off. A flashing life light verifies microprocessor sequencing. The PAL (U35) provides additional address decoding for the ROM (U12) expanding the memory size for the Model 91 firmware.

The Processor Support Chip (U7) controls the interfacing with other parts of the Model 91, as well as, decoding the lower eight address lines, A0 - A7. Seven card select lines from the Processor Support Chip enable interfaces in the Model 91.

$\overline{\text{GPIB}}$	GPIB interface
$\overline{\text{ROM}}$	ROM via U35
$\overline{\text{RAM}}$	AM via U35
$\overline{\text{FPSTB}}$	Front Panel
$\overline{\text{OBSTB}}$	Output Board
$\overline{\text{FGSTB}}$	Function Generator
$\overline{\text{OXSTB}}$	Pulse Board

Four Quiet Address Lines, QA0 - QA3, address the board interfaces in the Model 91. In addition, the Processor Support Chip connects the eight Quiet Data Lines, QD0 - QD7, to the board interfaces in the Model 91. These lines are bidirectional and active when the microprocessor needs to communicate with the board interfaces.

Also, the Processor Support Chip controls the frequency synthesizer via the SEN, SDATA, and SCLK lines. SEN enables the synthesizer, SDATA supplies serial data which loads the synthesizer's + M and + N counters. SCLK clocks the data into the counters.

The Processor Support Chip also produces five sets of control lines for the Sample and Hold Network. The SHEN line enables the network's DAC. SHDATA supplies the serial data that loads the DAC, and SHCLK clocks the data into the DAC. SHSEQM enables the sample and hold selector channel. SHSEL0, SHSEL 1, and SHSEL 2 select the sample and hold selector channels.

Another set of lines control the voltage measurement portion of the Model 91's internal calibration network. The lines, DVM0 - DVM5, select the inputs to the internal calibration network. $\overline{\text{DVM LB}}$ and $\overline{\text{DVM HB}}$ select either the higher or lower order byte to be read by the microprocessor. DVMRUN instructs the DVM to run. DVM-RDY tells the microprocessor it has data to send. During the frequency related portion of the Auto cal cycle, the Processor Support

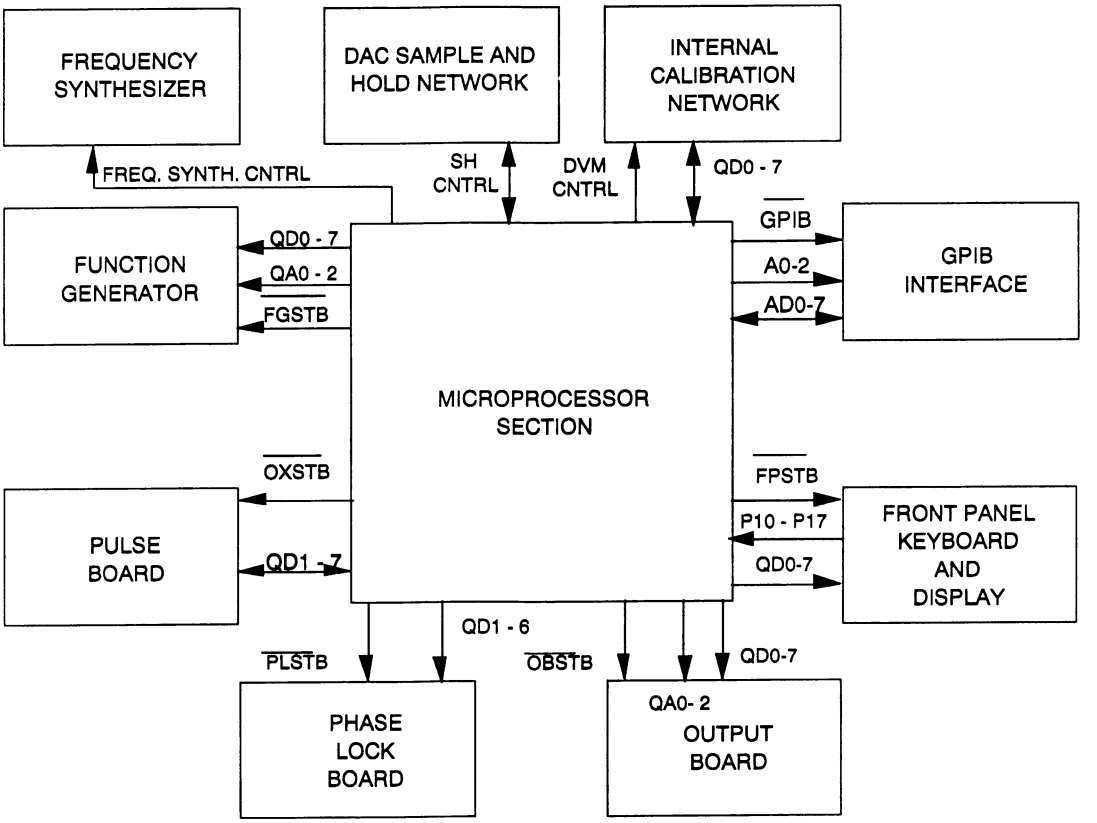


Figure 5-27. Microprocessor and Interfaces

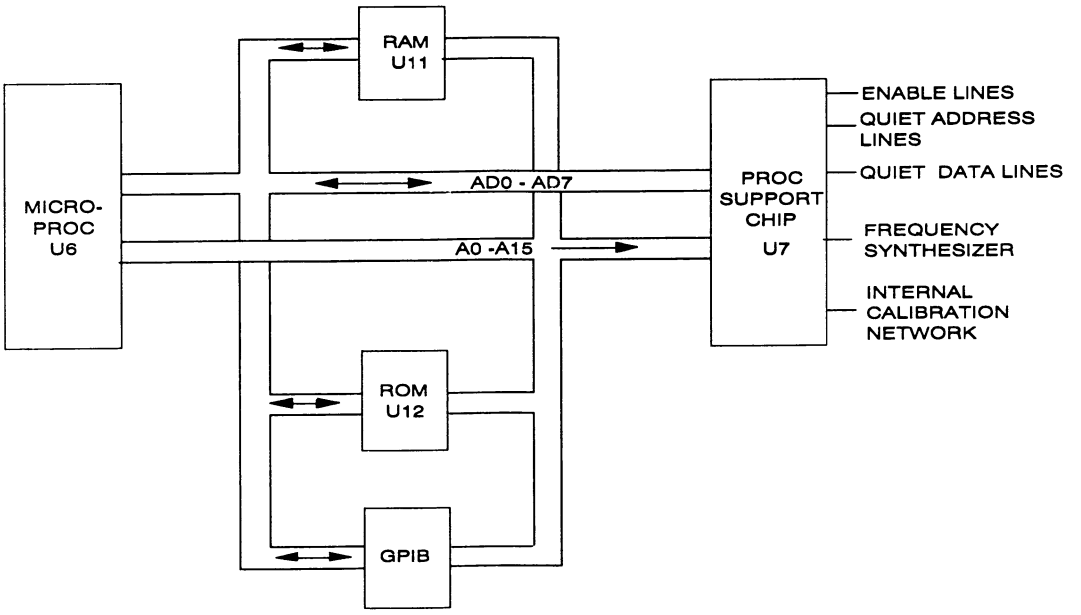


Figure 5-28. Microprocessor Section

Chip and microprocessor measure the SQWAVE, BXFREQ, and SYNTH frequency, period and symmetry. The FREQOUT line connects the Processor Support Chip and the microprocessor.

Two lines, RKA and RKB, decode the rotary encoder's (front panel control knob) rotation.

5.3.6.3 GPIB Interface

The GPIB interface circuit (schematic 1104-00-3391 sheet 10) allows remote operation of the Model 91 using an external IEEE-488 compatible controller. The GPIB circuit consists of a GPIB controller and two transceivers.

The GPIB controller (U8) functions as a traffic controller, permitting data to flow in either direction when the correct control information is received. The 'handshaking' routine will ensure neither the signal generator nor the remote controller will send data faster than the other can use. The controller has internal registers where control, data, and address words are loaded and stored until needed or requested. The controller bus connects to the microprocessor circuit address bus A0 - A2. The identification address of an instrument is determined by five bits in the controller address register. The default address (09) automatically loads into the controller from RAM at first (cold start) turn-on. A new address can be entered using the front panel keyboard. The GPIB line from the processor support chip enables the GPIB interface. The E clock from the microprocessor supplies the timing for the GPIB controller. The $\overline{R/W}$ line (read - high, write - low) controls the direction of data flow through the GPIB controller.

The transceivers (U9 and U10) permit bidirectional data flow. They have sufficient input sensitivity to minimize false signals and sufficient drive current to minimize signal loss. The transceiver (U9) handles the GPIB data lines, and the transceiver (U10) handles the GPIB control lines. Direction of data flow through the transceivers is controlled by the GPIB interface chip's T/R2 line.

5.3.6.4 Board Interfaces

The following boards have interface logic circuits that convert data lines into control lines for use on that board.

Function Generator

Schematic 1104-00-3342 sheet 1 of 7,

Phase Lock Loop

Schematic 1104-00-3437 sheet 1 of 6.

Pulse Board

Schematic 1104-00-3438 sheet 1 of 8.

Output board

Schematic 1104-00-3335 sheet 1 of 6.

Display /keyboard

Schematic 1104-00-3322 sheet 3 of 4.

5.3.6.4.1 Function Generator Interface

The function generator's interface logic consists of the input decoder (U1) and data registers (U2 and U3).

The decoder (U1) generates the clocks, CLK0 - CLK5, that will be used on the function generator board. The decoder inputs (QA0, QA1, and QA2) originate from the Microprocessor Section. The data clock selected by the address lines goes low at the decoder when $\overline{FGSTB}$ card select line goes low. Two enable lines of the decoder (G1 and G2A) are hardwired enabled. After the $\overline{FGSTB}$ card select line returns high, all decoder outputs return high. Table 5-6 provides a truth table for the decoder and defines the CLK outputs for the function generator board interface logic.

The registers (U2 and U3) latch data on their inputs on the rising edge of their clocks. The data is generated by the Microprocessor Section. The register (U3) supplies the frequency range control lines for the Frequency Range Switches and Capacitance Multiplier.

Table 5-6. Function Generator Decoder

Decoder Inputs				Output	Function
QA0	QA1	QA2	$\overline{FGSTB}$		
0	0	0	⊓	CLK0	Clocks Data Register U2
1	0	0	⊓	CLK1	Clocks $\overline{DS1}$ Sweep Generator
0	1	0	⊓	CLK2	Clocks $\overline{DS2}$ Sweep Generator
1	1	0	⊓	CLK3	Clocks $\overline{DS1}$ Symmetry Control
0	0	1	⊓	CLK4	Clocks $\overline{DS2}$ Symmetry Control
1	0	1	⊓	CLK5	Clocks Range Register U3
0	1	1	⊓	$\overline{PLSTB}$	Card select for Phase Lock Loop Interface

5.3.6.4.2 Phase Lock Loop Interface

The phase lock loop board's interface logic consists of a single Octal data register (U1). The register latches the data on its input lines, QD0 - QD7, on the rising edge of the $\overline{\text{PLSTB}}$ card select line. The function generator interface supplies the card select line, and the Microprocessor Section supplies the data lines.

5.3.6.4.3 Pulse Board Interface

The Pulse board interface logic consists of an octal flip-flop (U1) and five shift registers (U2, U3, U4, U5, and U6). The octal D flip-flop (U1) latches the Quiet Data Bus, QD0 - QD7, on the rising edge of the $\overline{\text{OXSTB}}$ signal. The microprocessor writes a data pattern to the flip-flop (U1) which produces a serial data stream from U1 pin 12. U1 pin 13 provides the serial data clock. The serial data is clocked into the shift registers (U2, U3, U4, U5, and U6). The output lines from the shift registers control circuits on the pulse board. The remaining outputs from the flip-flop (U1) latch data into devices throughout the pulse board. Table 5-7 lists and defines the decoded control lines for the pulse board.

Table 5-7. Pulse Control

Control Line	Function
$\overline{\text{DNCRST}}$	Resets One-Shot Divide by N Counters
DLYEN	Enables Delay One-Shot's Divide by N Counter
WDEN	Enables Width One-Shot's Divide by N Counter
BREN	Enables Burst Counter
DACEN	Enables Level Control DAC
RSTCNT	Clears Width Output flip-flop & Sets delay and width digital one-shots
$\overline{\text{DLALSEL}}$	Enables Delay Analog One-Shot
$\overline{\text{DLDGSEL}}$	Enables Delay Digital One-Shot
$\overline{\text{WDALSEL}}$	Enables Width Analog One-Shot
$\overline{\text{WDDGSEL}}$	Enables Delay Digital One-Shot
$\overline{\text{PSLOPE}}$	Enables Trigger Amplifier Positive Slope
$\overline{\text{NSLOPE}}$	Enables Trigger Amplifier Negative Slope
$\overline{\text{EREFSEL}}$	Selects SH Clock during AutoCal at Pulse Output Multiplexer
$\overline{\text{DBSEL}}$	Enables Double Pulse at Pulse Output Multiplexer
$\overline{\text{SNEWSEL}}$	Enables Square Wave at Pulse Output Multiplexer
$\overline{\text{PLSSEL}}$	Selects Pulse Output at Pulse Output Multiplexer

Table 5-7. Pulse Control (Continued)

Control Line	Function
$\overline{\text{DLTSTSL}}$	Selects Test Pulse Out during AutoCal at Pulse Output Multiplexer
$\overline{\text{PMANSEL}}$	Select Pulse Manual Trigger at Pulse Generator Trigger Multiplexer
$\overline{\text{SQRSEL}}$	Selects Square wave at Pulse Generator Trigger Multiplexer
$\overline{\text{SYNTHSEL}}$	Selects HF SYNTH at Pulse Generator Trigger Multiplexer
$\overline{\text{EXTSEL}}$	Selects External Trigger Source at Pulse Generator Trigger Multiplexer
SCLK	Serial Clock for Pulse Generator
SDATA	Serial Data for Pulse Generator
$\overline{\text{DL0SEL}}$	Selects 0 delay at Sync Multiplexer
$\overline{\text{DL50SEL}}$	Selects 50 ns Delay at Sync Multiplexer
$\overline{\text{DL20SEL}}$	Selects 20 ns Delay at Sync Multiplexer
$\overline{\text{TRGSYSL}}$	Select Front Panel as Sync Source at Sync Multiplexer
$\overline{\text{CALP}}$	Connects 50Ω load to Pulse Out during AutoCal
$\overline{\text{CALNP}}$	Connects 50Ω load to $\overline{\text{Pulse}}$ Out during AutoCal
ENABLE	Enables pin driver
COMP	Select Complement or Normal Pulse Output.
$\overline{\text{DH14}}$	Data Input of Digital Delay One-Shot
$\overline{\text{DH23}}$	Data Input of Digital Delay One-Shot
$\overline{\text{DH12}}$	Data Input of Digital Delay One-Shot
$\overline{\text{DH34}}$	Data Input of Digital Delay One-Shot
$\overline{\text{WH14}}$	Data Input of Digital Width One-Shot
$\overline{\text{WH23}}$	Data Input of Digital Width One-Shot
$\overline{\text{WH12}}$	Data Input of Digital Width One-Shot
$\overline{\text{WH34}}$	Data Input of Digital Width One-Shot
MCNTL1	Model Control Line
MCNTL2	Model Control Line
SRCNTL	Selects Internal or External Trigger Source (Model Control)
MANTRIG	Input for Front Panel Manual Trigger (Model Control)
PLSTM	Pulse Trigger Mode - Controls Function

Table 5-7. Pulse Control (Continued)

Control Line	Function
	Generator during Pulse Functions
POFF	Enable Pulse Trigger Multiplexer
EXDIV	Selects Trigger Frequency Divider
PMAN	Input for Pulse Manual Trigger

5.3.6.4.4 Output Board Interface

The output board's interface logic consists of the input decoder (U1) and data registers (U2 and U3). The input decoder produces the clocks which drive the data registers. The decoder inputs originate from the Microprocessor Section. When the decoder is enabled and $\overline{\text{OBSTB}}$ pulse goes low, a low pulse occurs on the decoder output line selected by QA0 - QA2. The registers latch data, QD0 - QD7, on the rising edge of their respective clocks. Table 5-8 defines the decoder outputs.

5.3.6.4.5 Front Panel (Keyboard and Display)

The front panel provides local operator interface to the function generator. This assembly contains the following circuits:

Control Knob Circuit
Display
Keyboard Circuit
Annunciation Circuit

Control Knob The control knob (SW1 - schematic 1104-00-3322 sheet 1 of 4) rotates continuously in both directions. Rotating the knob pulses its two output lines, RKA and RKB, with TTL logic levels. The Microprocessor Section on the motherboard counts these pulses to determine the amount of change and compares the phase relationship of the output lines to determine the direction of rotation.

Display The display (schematic 1104-00-3322 sheet 1 of 4) consists of the display driver (U1), Vacuum Fluorescent display (VFD1), and data latch (U3). The VFD is a triode vacuum tube with phosphorus coated anode that illuminates when electrons strike it. Each digit consists of 16 anodes with one grid. Elements of a digit lights when both the anode (+15V) and grid (+15V) are biased on. A -24V biases the grids off. The display driver (U1) controls the multiplexed arrangement of anodes and grids.

The driver receives clocked, DSCLK, serial data, DSDATA, from the input latch (U3) via the level shifter (Q1 and Q2). Another line to the driver, DSPOR, provides a power on reset to the driver.

The display circuit is powered by its own +15 V dc regulator (VR1) which uses the +22 V dc for its input. The fluorescent display filament ($8V_{rms}$ superimposed on -5Vdc) receives its power from the FILA and FILB lines. All power is supplied from the motherboard.

Keyboard The keyboard circuit (schematic 1104-00-3322 sheet 2 of 4) consists of an eight-column, six-row matrix, input register (U3), and decoder (U2). Control signal, FPREG, latches the quiet data bus, QD0-QD2, lines into the latch which drives the decoder. The decoder steps through the six rows, making each row high (+5V) one at a time. When a key is pressed, the high appears on the column associated with that switch. The column lines (P10 - P17) connect directly to the microprocessor circuit. The microprocessor determines which key has been pressed by analyzing the row/column status.

Annunciator Circuit The Light Emitting Diode, LED, circuit (schematic 1104-00-3344 sheets 2 and 3) consists of LEDs (CR4 - CR27), decoder (U4), and data register (U5 - U7). The LEDs identify the selected mode and function. Two other LEDs (CR1 and CR2) connected to the data register (U3) are also part of the LED circuit. The decoder (U4) converts quiet addresses, QA0 and QA1, into clocks for the four registers. Each of four registers (U3, U5 - U7) reads the quiet data bus, QD0 - QD7, and when any of the latches goes low, the LED annunciator lights. Conversely, when a latch output goes high, the LED annunciator remains off.

5.3.6.5 DAC Sample and Hold Network

The DAC/Sample and Hold Network (schematic 1104-00-3395 sheet 5 of 10) provides the various control voltages required throughout the Model 91. The values for these control voltages are determined during AutoCal and calibration. This circuit consists of the 16 bit DAC (U18), the 1 of 8 selector (U19), and the eight hold capacitors (C49 - 56) and buffers.

Table 5-8. Output Decoder

Decoder Inputs				Output	Function
QA0	QA1	QA2	$\overline{\text{OBSTB}}$		
0	0	0	⊓	CLK0	Clocks Attenuator Selector (Motherboard)
1	0	0	⊓	CLK1	Clocks Data Register U3
1	1	0	⊓	CLK33	Clock Data Register U2

The microprocessor section loads serial data, SHDATA, using the clock, SHCLK. The line, SHEN, enables the DAC. Output from the DAC drives the selector. The microprocessor section's SHSEL0 - SHSEL2 lines select the channel. The voltage from the selector charges the selected capacitor (C49 - C56). The microprocessor section updates the DAC and selects the next channel. Thus, the microprocessor cycles through channels continuously refreshing the capacitors. Buffers (U20 - U24) provide a high impedance which hold the charge on the capacitors.

The DAC supplies a maximum output of ±3 Vdc. Some control voltages require voltages greater than the ±3 Vdc, therefore, some control voltages are amplified.

5.3.6.6 Internal Calibration Network

During AutoCal, the Internal Calibration Network, in conjunction with circuits on other boards, makes various voltage and frequency measurements and stores correction data in memory. On power up, these correction values are recalled from memory and, via the Sample and Hold Network, routed to control circuits within the Model 91.

Each of the test points may have more than one value; for example frequency related test points may have different values for different frequency ranges. Figure 5-29 illustrates the internal calibration network used with in the Model 91. The network shown can simply be thought of as a series of selector switches that ultimately route a single test point to the DVM. The calibration network consists of two parts: the voltage measurement section (schematic 1104-00-3440 sheet 2 of 10) and the frequency measurement section (schematic 1104-00-3440 sheet 3 of 10). Both sections provide inputs to the Microprocessor section, or to be more specific, the Processor Support Chip.

The heart of the voltage measurement section is the DVM (U4 - Motherboard). The DVM receives a single dc voltage from the Multiplexer, Mux, (U3). The DVM is referenced to the +10 Vdc voltage reference, VREF, (U32 - schematic 1104-00-3440 sheet 8 of 10).

The DVM MUX 1 (U3 - schematic 1104-00-3440 sheet 2 of 10) selects one of its eight inputs for the DVM. Table 5-9 describes the control lines, inputs and the function of the Mux inputs. Test points connected to this multiplexer come from either the Motherboard or other multiplexers.

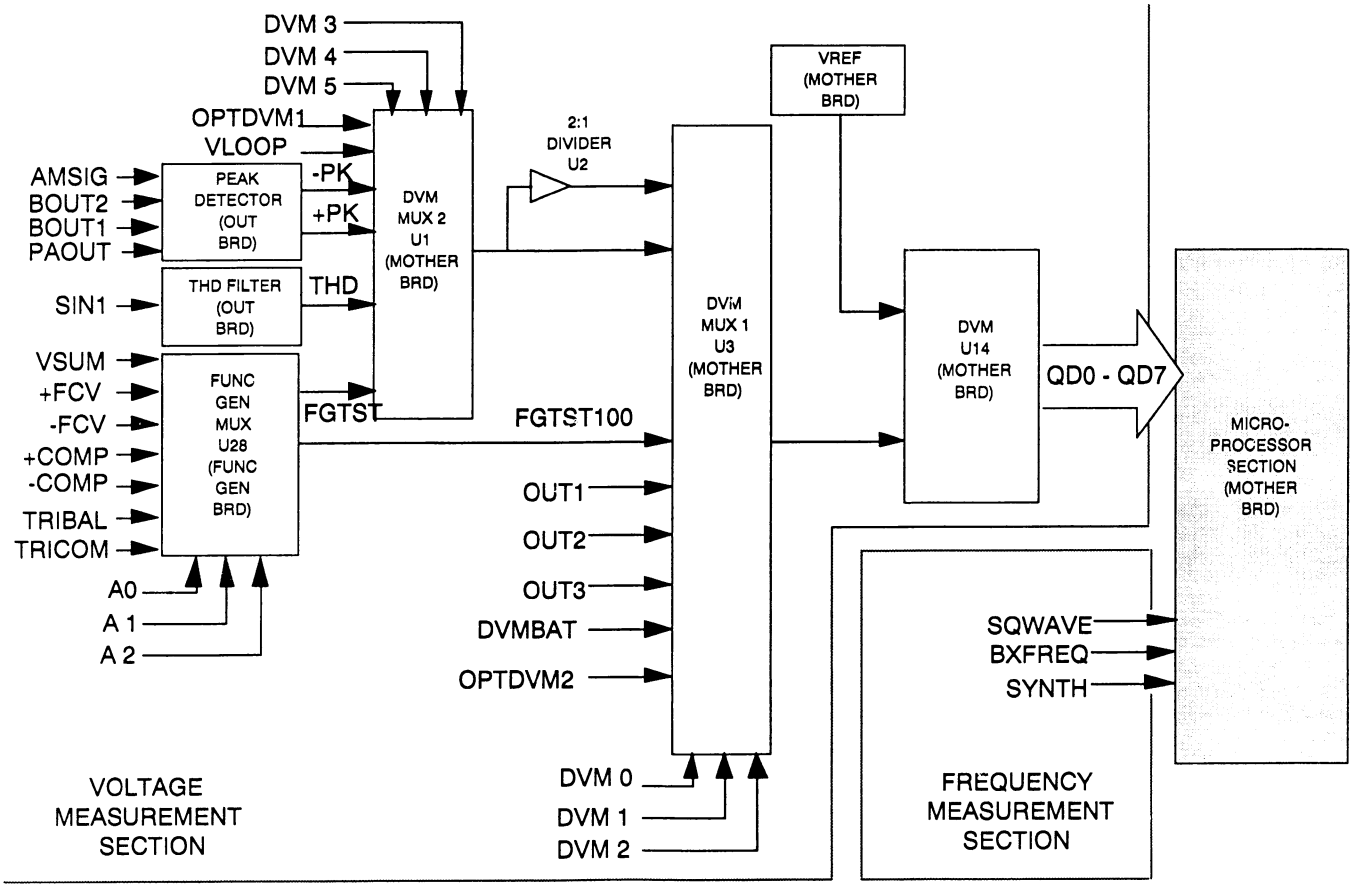


Figure 5-29. Internal Calibration

The DVM MUX 2 (U1 - Schematic 1104-00-3440 sheet 2 of 10) also selects one of eight inputs. But, its inputs originate on the Output, Phase Lock Loop, and Function Generator boards. Table 5-10 describes the inputs and the control lines (DVM3, DVM4, and DVM5) that selects them. This mux provides two outputs. A direct output for voltages less than +4Vdc, and a reduced (1/2) output for voltages greater than +4Vdc.

The function generator's Autocalibration circuit (schematic 1104-00-3342 sheet 4 of 7) consists of an analog multiplexer (U28) which selects one of eight test points on the function generator board. The amplifier, U29A buffers the multiplexer's output. Another amplifier, U29B, amplifies the lower level signals by X101. The two amplifier outputs (FSTST and FGTST100) drives the Internal Calibration Network's DVM MUX 2. Table 5-11 describes the inputs and the control lines (A0, A1, and A2) that selects them.

The Output Board's Peak Detector (schematic 1104-00-3335 sheet 6 of 6) selects and routes one of four voltages to the positive and negative Peak Detectors. The Peak Detectors consist of a positive half (U9A and U9D) and a negative half (U9B and U9C). Both detectors function the same, except for the polarity of the outputs, therefore only the positive peak detector will be described. Applying a positive voltage to U9A causes the amplifier's output to swing positive charging capacitor (C69) through diode (CR28). The amplifier (U9D) buffers the capacitor's voltage and provides feedback to the input amplifier (U9A). As the input voltage is reduced, the diode (CR28) becomes reversed biased and the capacitor (C69) holds a charge that represents the most positive (peak) voltage. The diode (CR35) provides local feedback to the input amplifier (U9A) while holding the peak. The transistor (Q20) discharges the capacitor (C69) when the PKRST line goes low which resets the peak detector. The relay (K7) bypasses the peak detector when the Internal Calibration Network measure dc voltages from the Output Board. Three switches (U8A - U8C) select the inputs to the peak detector. Table 5-12 describes the inputs and the control lines that selects them.

Table 5-9. DVM Mux 1

DVM0	DVM1	DVM2	Name	Function
0	0	0	OUT1	Unbalanced output from Unbalanced Output and Impedance Network"
1	0	0	OUT2	BAL OUT (+) from Balanced Output Attenuator Network and Impedance Control
0	1	0	OUT3	BAL OUT (-) from Balanced Output Attenuator Network and Impedance Control
1	1	0	FGTST100	Low level function generator measurements
0	0	1	DVM BAT	Measures memory back up battery voltage Microprocessor Section
1	0	1	OPTDVM2	Identifies Option 001 / 002.
0	1	1		Output from DVM MUX2. Voltages >+4V.
1	1	1		Output from DVM MUX2. Voltages <+4V.

Table 5-10. DVM Mux 2

DVM3	DVM4	DVM5	Name	Function
0	0	0	FGTST	Output from Function Generator Mux U28 on Function Generator Board.
1	0	0	TEST IN	TP 1
0	1	0	+PK	Positive peak detector output from Output Board
1	1	0	THD	THD filter output from Output Board.
0	0	1	Ground	Circuit Common
1	0	1	-PK	Negative peak detector output from Output Board
0	1	1	VLOOP	Phase Lock Loop filter output from Phase Lock Loop Board
1	1	1	OPTDVM1	Optional High Voltage Output amplifier output.

Table 5-11. Function Generator Mux.

A0	A1	A2	Name	Function
0	0	0	Ground	Analog Ground
1	0	0	VSUM	VCG Summing Amplifier Output from Function Generator Board.
0	1	0	+FCV	Positive Symmetry Control output from Function Generator Board.
1	1	0	-FCV	Negative Symmetry Control output from Function Generator Board.
0	0	1	+COMP	Positive Output from the High Frequency Compensation DAC on the Function Generator Board
1	0	1	-COMP	Negative Output from the High Frequency Compensation DAC on the Function Generator Board.
0	1	1	TRIBAL	Triangle Buffer output from the Function Generator Board
1	1	1	TRICOM	Triangle Buffer's Analog Ground from the Function Generator Board

The THD Filter is a Twin Tee Notch filter that receives its input , SIN1, from the Sine Buffer on the Phase Lock Loop Board. The Filter (schematic 1104-00-3437 sheet 6 of 6) consists of the actual filter (U10B) and a rms Detector (U10A). The notch filter has a center frequency of about 10 kHz. The rms Detector provides a dc voltage proportional to the harmonics of the 10 kHz sine wave input.

The Frequency Measurement Section consists of three inputs to the Microprocessor Section; refer to paragraph 5.3.6.2.

Table 5-12. Peak Detector

Control Line	Input Name	Function
$\overline{\text{SELPRE}}$	AMSIG	Amplitude control signal from AM buffer from Phase Lock Loop Board.
$\overline{\text{SELBAL2}}$	BOUT2	Negative Balance Driver output from Output Board.
$\overline{\text{SELBAL1}}$	BOUT1	Positive Balance Driver output from Output Board.
$\overline{\text{SELPA}}$	PA OUT	Power Amplifier output from Output Board.

AutoCal- Pulse Generator

During AutoCal, the microprocessor section programs a delay of 1ms based on a 10 ns clock period. The data selector (U18), $\overline{\text{DLTSTSL}}$ low, selects the programmed delay or SHCLK for calibration. To calibrate the digital section's delay, the flip-flop, U17B produces a pulse whose width equals the AutoCal's programmable delay. The microprocessor measures this pulse via the signal (SQWAVE) and calibrates the digital one-shot. To measure the SHCLK, The data selector ($\overline{\text{EREFSEL}}$) routes the line (EREF), which is the 500 kHz Sample and Hold clock, to the SQWAVE output. The microprocessor measures this frequency and provides a correction value for the E clock (SHCLK via U7 on Motherboard).

SECTION 6
MAINTENANCE

6.1 INTRODUCTION

This section presents information, which when used with the Verification Procedure (Section 3), the Circuit Description (Section 5), and the Schematic and Assembly Drawings (Section 7), returns the Model 91 to proper operating condition. This section covers:

Factory Service,
Problem Isolation,
Disassembly and Reassemble - including board removal.

6.2 ROUTINE MAINTENANCE

Section 2 of this manual covers routine maintenance of the Model 91.

6.3 FACTORY SERVICE

Wavetek maintains a factory repair department for those customers not possessing the personnel or test equipment to troubleshoot the instrument. If an instrument is returned to the factory for calibration or repair, a detailed description of the problem symptoms should be attached to minimize turnaround time.

Wavetek San Diego, Inc.
9045 Balboa Ave.
San Diego, CA 92123
Telephone: (619) 279-2200
TWX: (910) 335-2007
FAX: (619) 565-9558

Before returning the instrument, call Wavetek's Customer Service department and obtain a Return Authorization Number; Wavetek uses this number to identify your instrument while it is in for repair.

The instrument should be packed according to the instructions in paragraph 2.3 of the *Model 91 Operator's Manual.*

6.4 BEFORE BEGINNING

Before beginning the troubleshooting process, verify that the instrument setup is correct. See section 3 of the *Model 91 Operator's Manual.*

Visually inspect the instrument for physical damage, paragraph 6.6.1.

1. Check the primary source.
2. Check the power cord.
3. Verify the primary supply voltage and the units voltage selection match; see paragraph 2.4.1 of the *Model 91 Operator's Manual.*
4. Check the unit's fuse; see paragraph 2.3 of this manual.

6.5 TROUBLESHOOTING PHILOSOPHY

The intent of this section is not to isolates failures to the component level but to give service technicians a set of "tools" that will guide them to the most likely circuit or circuits. From that point, the service technician must turn to the appropriate set of schematics and assembly drawings in the rear of this manual, and together with the circuit description (section 5) isolate the faulty component.

6.6 BEFORE TROUBLESHOOTING

6.6.1 Inspection

Before beginning the troubleshooting procedure, use the following inspection procedures to locate obvious malfunctions with the Model 91.

1. Inspect all external surfaces of Model 91 for physical damage, breakage, loose or dirty contacts, and missing components.
2. Remove top cover, shield, and bottom cover to access components; paragraph 6.9.

WARNING

The Model 91 contains high voltages. After power is removed, discharge capacitors to ground before working inside the instrument to prevent electrical shock.

CAUTION

Do not disconnect or remove any board assemblies in the Model 91 unless the instrument is unplugged. Some board assemblies contain devices that can be damaged if the board is removed with the power on. Several components, including MOS devices, can be damaged by electrostatic discharge. Use conductive foam and grounding straps when servicing is required around sensitive components. Use care when unplugging ICs from high-grip sockets.

3. Inspect printed circuit board surfaces for discoloration, cracks, breaks, and warping.
4. Inspect printed circuit board conductors for breaks, cracks, or cuts.
5. Inspect all assemblies for burnt or loose components.
6. Inspect all chassis-mounted components for looseness, breakage, loose contacts or conductors.
7. Inspect the Model 91 for disconnected, broken, cut, loose, or frayed cables or wires.

6.6.2 Test Point Access

Test point access on the vertically mounted boards requires that, during signal tracing, a board be connected to the mother board through special extender cards.

Since only one board can be extended at a time and still allow access to components and test points, the person performing the troubleshooting should review the fault and the fault isolation steps logically to determine a plan that will require the least amount of board removal and reinstallation.

CAUTION

Do not install or remove vertical board assemblies from the mother board with the operating power ON. Damage to components on the assemblies will occur if the assemblies are removed or inserted with operating power on.

CAUTION

Before removing Pulse board, disconnect cables which are attached to board through holes in the rear shield.

Test points called out in the following procedures are shown on the assembly drawings and the schematic diagrams for each vertical board and the mother board. Three types of test points are shown. Numbered test points which are actual reference designator components on the board, and numbered test points which are locations on components that have been added as an aid in fault isolation. The final test points are actually pins on ICs and connectors.

Some circuits on the mother board and the phase lock loop board are shielded by rectangular metal cans soldered to the board traces. Test points located under these shields must be accessed from the solder side of the boards. Do not remove the shields except if repair is required in the shielded area.

6.6.3 Board Location

Figure 6-1 shows the location of the board assemblies in the Model 91.

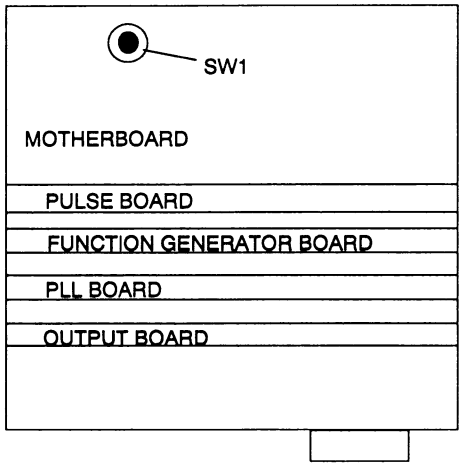


Figure 6-1. Board Locations

6.7 FAULT ISOLATION

This paragraph provides a series of procedures that when followed will point to recommended circuit blocks. Skip those procedures that do not apply to your symptom. Each circuit block reference will contain additional references to the proper Circuit Description paragraphs and Schematic and Assembly drawings. Use the circuit descriptions in conjunction with the schematics to gain a deeper understanding of the circuit block. Table 6-1 lists the recommended equipment necessary to troubleshoot the Model 91.

6.7.1 Front Panel Not Active - Neither the front panel's display, annunciators, or keyboard Function.

1. Check the primary source; paragraph 6.4.
2. Visually inspect the unit; paragraph 6.6.

Secondary Supplies

1. Remove the top cover (see paragraph 6.9.1 - Top Cover/Shield Removal)
2. Check the unit's secondary supplies using the digital voltmeter. Table 6-2 lists the power supplies, their voltages and tolerances, as well as drawing references. Test Points are located on the Motherboard. All voltages are referenced to analog ground (TP6).

   Also check the power supplies distribution system by measuring the voltages at each of the connectors on the Motherboard. Refer to the instrument schematic 1004-00-0649 and schematic 1104-00-3440 sheet 1.

Table 6-1. Recommended Equipment

Equipment	Requirements
Scope	Dual trace, 250 MHz Bandwidth
Digital Voltmeter	Three Digit Accuracy (minimum).
Frequency Counter	>Four Digits of resolution, <±10 ppm accuracy. (Synthesizer and Optional Frequency Reference.)
Board Extender Kit	Wavetek part number 1100-00-3411

In addition, check the power supplies on the following circuit board.

Display/Keyboard P12 shown on schematic 1104-00-3322 sheet 2.

Output Board, P10 & J11 shown on schematic 1104-00-3335 sheet 1.

Phase Lock Loop Board, J8 & J9 shown on schematic 1104-00-3437 sheet 1

Function Generator Board, J6 & J7 shown on schematic 1104-00-3342 sheet 1.

Pulse Board, J30 & J31 shown on schematic 1104-00-3438 sheet 1.

Synthesizer Module, J32 & J33 shown on schematic 1104-00-3460 sheet 1.

Power Supplies check OK.

1. Check the Microprocessor Section: Schematic 1104-00-3440 Sheet 3 of 10, Assembly drawing 1101-00-3440 sheet 1 of 3. For a description of the Microprocessor Section's circuits, refer to paragraph 5.3.6.2.
2. Check the microprocessor section: paragraph 6.8.17.

   HINTS

   Check the supply voltages to the circuits within the Microprocessor Section.

   Using a scope, check the Microprocessor's control and data lines (paragraph 6.8.17). Most lines should be active. Lines stuck high or low could identify a defective device.
3. If the keypad and display still does not operate, check major data lines into the front panel input decoder, U4.

   FPS Enables front panel keyboard/display

   FPREG Clocks QD0 - QD7 into decoder.

   QD0 - QD7 Input Data

   Refer to schematic 1104-00-3322 sheet 2 of 4, assembly drawing 1101-00-3322 sheet 1 of 2, circuit description paragraph 5.3.6.4.5.

6.7.2 Front Panel Not Active - Keyboard Does Not Work

1. Refer to schematic 1104-00-3322, assembly drawing 1101-00-3322 sheet 1 of 2.
2. Check the supply voltages to the circuits within the Keyboard.

   Using the scope, check the control and data lines in the keyboard; see circuit description paragraph 5.3.6.4.5 - Keyboard. Most lines should be active. Lines stuck high or low could identify a defective device.

6.7.3 Front Panel Not Active - Display Does Not Work

1. Refer to schematic 1104-00-3322, assembly drawing 1101-00-3322 sheet 1 of 2.
2. Check the supply voltages to the circuits within the Display.

   Using the scope, check the control and data lines on the display; see circuit description paragraph 5.3.6.4.5 - Display. Most lines should be active. Lines stuck high or low could identify a defective device.

6.7.4 Front Panel Not Active - Annunciators Do Not Work

1. Refer to schematic 1104-00-3322, assembly draw-

Table 6-2 Power Supply Test Points

Test Point	Supply Voltage	Tolerance	Schematic Drawing	Assembly Drawing
JMP 4	+12VDC	±0.2 Vdc	1104-00-3440 Sheet 8 of 10	1101-00-3440 Sheet 1 of 3
JMP 5	-12VDC	±0.2 Vdc	1104-00-3440 Sheet 8 of 10	1101-00-3440 Sheet 1 of 3
JMP 6	+5V	±0.2 Vdc	1104-00-3440 Sheet 8 of 10	1101-00-3440 Sheet 1 of 3
TP14	+24 VDC	±0.2 Vdc	1104-00-3440 Sheet 9 of 10	1101-00-3440 Sheet 1 of 3
TP15	-24VDC	±0.2 Vdc	1104-00-3440 Sheet 9 of 10	1101-00-3440 Sheet 1 of 3

ing 1101-00-3322 sheet 1 of 2.

2. Check the supply voltages to the circuits within the Display.

   Using the scope, check the control and data lines in the Annunciator circuit; see circuit description paragraph 5.3.6.4.5 - Annunciator Circuit. Most lines should be active. Lines stuck high or low could identify a defective device.

6.7.5 Self Test and Self Test Error Messages

When power is first applied, the Model 91 performs Self Test. Self test checks the unit's internal battery, Motherboard memory, and storage memory. Failure of any of the tests will cause the Model 91 to display an error message. Table 6-3 defines the error messages. If Self Test is successful, the Model 91 will display "Wavetek Model 91".

6.7.6 AutoCal and AutoCal Error Messages

The Model 91 contains a powerful fault isolation tool: AutoCal. AutoCal measures numerous "test points" in the Model 91. It compares these measurements against either a frequency standard or voltage standard. AutoCal attempts to make corrections for any deviations. But if AutoCal can not bring the measurement within limits, the Model 91 produces an error message. The Model 91 runs AutoCal until it hits its first error. Then it stops until the error is fixed by either performing the Calibration procedure, section 4, or isolating and fixing the problem. Continue running AutoCal until all problems have been identified and fixed.

To AutoCal the Model 91, perform the following steps. AutoCal requires no external test equipment. In fact, test equipment should not be connected to the Model 91 input connectors, otherwise the AutoCal could alter the calibration of the instrument. Also, disconnect all inputs and outputs from the instrument otherwise the sudden changes in the instrument's output waveforms could damage external equipment.

1. Turn on the Model 91 and allow it to warm up for 20 minutes. Pressing the **CALIBRATE** key during the 20 minute warm up time displays the count-down time, after the 20 minutes the Model 91 begins AutoCal. Pressing any other key during the count down aborts AutoCal and returns the instrument to normal operation.

   REMEMBER

   Remove all input and output connections to the Model 91 before pressing Autocal.

2. After a 20 minute warm up, press the **SHIFT** and **CALIBRATE** key and allow the unit time to complete the AutoCal cycle. While running AutoCal, the Model 91 displays "**CALIBRATING**". When completed successfully, the Model 91 displays "**AUTO-CALIBRATED**". Then the unit returns to its last operational setup. If the AutoCal fails the Model 91 displays an error message which identifies the parameter - **ERR** (*Keyword*); for example **ERR USINCAL**. If this occurs occasionally, try to AutoCal the unit again. Note the error keywords and report the errors when the unit is returned for scheduled maintenance.

3. If repeating the AutoCal procedure a second time returns the same message, try the following steps before beginning block isolation. This procedure erases the calibration values stored in the Model 91 memory and replaces the calibration values with nominal calibration values.

A. After a 20 minute warm up, press the internal calibration switch while pressing the **CALIBRATE** key (paragraph 4.3, Step 2 Initial Steps).

B. Press the **PARAM RESET** key to load the Model 91's nominal calibration values.

C. Press the **CALIBRATE** key to return to normal operation.

D. Perform the Calibration Procedure (paragraph 4.3).

Following is a listing of the AutoCal error messages in AutoCal sequential order. Included is a brief description of the AutoCal step. In addition, each step contains Pass/Fail instructions. Also, because each of these steps use the Model 91's internal calibration network, check out the Internal Calibration Network (refer to paragraph 5.3.6.6).

VCG0 This check removes frequency shift error

Table 6-3. Self Test Error Messages

Display	Probable Cause	Corrective Action
Low batt x.xxx v	Internal battery voltage low.	Unit is available for immediate operation. Refer to paragraph 2.3 for battery replacement.
Cal Required	Internal battery dead.	Unit has lost its calibration data but can be used after performing and passing AutoCal. Instrument may not meet all specifications.

in the function generator. The test sets the generator to 200 Hz on the 200 kHz range and using the internal calibration network adjusts out 1000:1 frequency errors (<0.7 Hz deviation).

Passes: Verifies the function generator operates correctly. No message will be displayed and AutoCal moves to the next step.

Fail: If the unit displays the VCGO message, it means the Function Generator may not be working correctly. Use the procedure in paragraph 6.8.1 to isolate the faulty circuit.

VFREQ0

This check zeros the VCG summing amplifier with the VFREQ input connected. It also zeros the Function Generator board's AutoCal circuit. Test requires the VSUM voltage be <20 mV of analog ground.

Passes: Verifies the VCG Summing Amplifier and Auto Calibration circuit operates correctly. No message will be displayed and AutoCal moves to the next step.

Fail: If the unit displays the VFREQ0 message, it means the VCG Summing Amplifier or Auto Cal circuit may not be working correctly. Use the procedure in paragraph 6.8.1 to check the VCG Summing Amplifier. Use paragraph 6.8.9 to check the function generator's AutoCal circuit.

VFREQ0 SCL

This check zeros the VCG Summing amplifier with the VFREQ input disconnected. It also zeros the Function Generator board's AutoCal circuit. Test requires the VSUM voltage be <10 mV of analog ground.

Passes: Verifies the VCG summing Amplifier and Auto Calibration circuit operates correctly. No message will be displayed and AutoCal moves to the next step.

Fail: If the unit displays the VFREQ0 message, it means the VCG summing amplifier or AutoCal circuit may not be working correctly. Use the procedure in paragraph 6.8.1 to check the VCG summing amplifier.

S+VCGOFF

This check zeros (<20 mV) the positive symmetry control relative to the analog ground.

Passes: Verifies the positive symmetry control works. No message will be displayed and AutoCal moves to the next step.

Fails: Check the Symmetry Control (paragraph 6.8.3).

S–VCGOFF

This check zeros (<20 mV) the negative symmetry control relative to the analog ground.

Passes: Verifies the negative symmetry control works. No message will be displayed and AutoCal moves to the next step.

Fails: Check the Symmetry Control (paragraph 6.8.3).

VTRIBAL

This check zeros (<59 mV) the triangle buffer, TRIBAL, relative to analog ground, TRICOM.

Passes: Verifies the negative high frequency compensation control works. No message will be displayed and AutoCal moves to the next step.

Fails: Check the Triangle Buffer, Compensation, and Comparator (paragraph 6.8.2).

SYMM50PCT

This check sets the symmetry control to 50%, symmetry off, and adjusts for 50% ±0.03% symmetry at 201 Hz on the 200 kHz range.

Passes: Verifies the symmetry control and current sources work. No message will be displayed and AutoCal moves to the next step.

Fails: Check the symmetry control (paragraph 6.8.3) and VCG current sources (paragraph 6.8.4).

+VCGOFF

This check turns on the symmetry, sets the symmetry to 50%, and adjusts the symmetry to 50%.

Passes: Verifies the symmetry control and current sources work. No message will be displayed and AutoCal moves to the next step.

Fails: Check the symmetry control (paragraph 6.8.3).

SWPLENGTH This check sets VSLEN (sweep length) DAC reference input and adjusts the sweep DAC to a specified frequency.

Passes: Verifies the sweep generator works. No message will be displayed and AutoCal moves to the next step.

Fails: Check the Sweep Generator (paragraph 6.8.10) and VSLEN (DAC Sample and Hold Network, paragraph 6.8.18).

SCALE This check sets VFREQ input to a full scale level (200 kHz on the 200 kHz range). The Model 91 switches IN SCALE reducing the frequency to 20 kHz (10:1). The internal calibration network adjusts VFREQ to 20 kHz ± 1Hz

Passes: Verifies the frequency accuracy at 10:1 on the 200 kHz range. No message will be displayed and AutoCal moves to the next step.

Fails: Check the function generator (paragraph 6.8.1). Also check the DAC Sample and Hold Network (paragraph 6.8.18).

TOFR7 This check sets the function generator to the 200 kHz range. The internal calibration network measures and adjusts VFREQ to 200 kHz ± 10 Hz.

Passes: Verifies the frequency accuracy at the top of the 200 kHz range. No message will be displayed and AutoCal moves to the next step.

Fails: Check Frequency Range Switch Circuit (paragraph 6.8.7). Also check the function generator (paragraph 6.8.1).

TOFR6 This check sets the function generator to the 20 kHz range. The internal calibration network measures and adjusts VFREQ to 20 kHz ± 1Hz.

Passes: Verifies the frequency accuracy at the top of the 20 kHz range. No message will be displayed and AutoCal moves to the next step.

Fails: Check Frequency Range Switch Circuit (paragraph 6.8.7). Also check the function generator (paragraph 6.8.1).

TOFR5 This check sets the function generator to the 2kHz range. The internal calibration network measures and adjusts VFREQ to 200 kHz ± 0.15 Hz.

Passes: Verifies the frequency accuracy at the top of the 2kHz range. No message will be displayed and AutoCal moves to the next step.

Fails: Check Frequency Range Switch Circuit (paragraph 6.8.7). Also check the function generator (paragraph 6.8.1).

TOFR4 This check sets the function generator to the 200 Hz range. The internal calibration network measures and adjusts VFREQ to 200 Hz ± 0.01 Hz.

Passes: Verifies the frequency accuracy at the top of the 200 Hz range, and verifies the operation of the capacitance multiplier. No message will be displayed and AutoCal moves to the next step.

Fails: Check the capacitance multiplier (paragraph 6.8.8) and Frequency Range Switch Circuit (paragraph 6.8.7). Also check the function generator (paragraph 6.8.1).

TOFR3 This check sets the function generator to the 20 Hz range. The internal calibration network measures and adjusts VFREQ to 20 Hz ± 0.02 Hz.

Passes: Verifies the frequency accuracy at the top of the 20 Hz range, and verifies the operation of the capacitance multiplier. No message will be displayed and AutoCal moves to the next step.

Fails: Check the capacitance multiplier (paragraph 6.8.8) and Frequency Range Switch Circuit (paragraph 6.8.7). Also check the function generator (paragraph 6.8.1).

COMP9+/- This check sets the function generator to 20 MHz range. Then sets VFREQ to 2MHz. Next the VFREQ value is set for 20 MHz, and the high frequency compensation DAC adjusted for 20 MHz. The cycle repeats for up to 20 iterations.

Passes: Verifies the 20 MHz range 10:1 frequency linearity. No message will be displayed and AutoCal moves to the next step.

Fails: Check the high frequency compensation circuit (paragraph 6.8.6). Also check the function generator (paragraph 6.8.1).

COMP8+/- This check sets the function generator to 2MHz range. Then it sets VFREQ to

200 kHz. Next the VFREQ value is set for 2MHz, and the high frequency compensation DAC adjusted for 2MHz. The cycle repeats for up to 20 iterations.

Passes: Verifies the 2MHz range 10:1 frequency linearity. No message will be displayed and AutoCal moves to the next step.

Fails: Check the high frequency compensation circuit (paragraph 6.8.6). Also check the function generator (paragraph 6.8.1).

FINDNOTCH — This check sets the function generator to a 10 kHz sine wave. Then using the notch filter and internal calibration network adjusts the frequency (VFREQ) to 10 kHz.

Passes: Verifies the sine convertor and buffer, variable supply, and notch filter operates correctly. No message will be displayed and AutoCal moves to the next step.

Fails: Check the Sine Buffer, Sine Converter, and Variable Supply (paragraph 6.8.11).

OFSTZERO — This check sets the function to dc and the offset voltage to 0Vdc. Then measuring the power amplifier output with the internal calibration network, adjusts the offset (VOFST) to <9 mV.

Passes: Verifies the operation of the power amplifier. No message will be displayed and AutoCal moves to the next step.

Fails: Check the power amplifier (see paragraph 6.8.14). Also, check the DAC Sample and Hold Network (paragraph 6.8.18).

OFSTGAIN — This check sets the function to dc and the offset voltage to 5Vdc. Then measuring the power amplifier output with the internal calibration network, adjusts the offset gain (VOFST) to +5Vdc ±9mV.

Passes: Verifies the operation of the power amplifier. No message will be displayed and AutoCal moves to the next step.

Fails: Check the power amplifier (see paragraph 6.8.14). Also check the DAC Sample and Hold Network (paragraph 6.8.18).

BALOFFST — This check sets the function to dc and the offset voltage to 0Vdc. The internal calibration network measures the two balanced outputs and adjusts the offset voltage (VOFST) so the difference between the two outputs is <3 mVdc.

Passes: Verifies the operation of the balanced drivers. No message will be displayed and AutoCal moves to the next step.

Fails: Check the balanced drivers (paragraph 6.8.14).

SINEAMPL — This check sets the function to sine wave and using the peak detector, measures the peak to peak amplitude of the sine wave, and adjusts amplifier output via VAMCAL to 20 ±0.03 Vpp.

Passes: Verifies the operation of the function selector, preamplifier and multiplier, and AM buffer. No message will be displayed and AutoCal moves to the next step.

Fails: Check the function selector (paragraph 6.8.14), preamplifier/multiplier (paragraph 6.8.14), and AM buffer (paragraph 6.8.14).

TRIAMPL — This check sets the function to triangle wave and using the peak detector, measures the peak to peak amplitude of the triangle wave, and adjusts amplifier output via VAMCAL to 20 ±0.03 Vpp.

Passes: Verifies the operation of the function selector, preamplifier and multiplier, and AM buffer. No message will be displayed and AutoCal moves to the next step.

Fails: Check the function selector (paragraph 6.8.14), preamplifier/multiplier (paragraph 6.8.14), and AM buffer (paragraph 6.8.14).

SQURAMPL — This check sets the function to square wave and using the peak detector, measures the peak to peak amplitude of the square wave, and adjusts amplifier output via VAMCAL to 20 ±0.03 Vpp.

Passes: Verifies the operation of the function selector, preamplifier and multi-

plier, and AM buffer. No message will be displayed and AutoCal moves to the next step.

Fails: Check the function selector (paragraph 6.8.14), preamplifier/multiplier (paragraph 6.8.14), and AM buffer (paragraph 6.8.14).

BALAMPL This check adjusts the balanced output amplitude to 20 ±0.03 Vpp by measuring the balanced driver output with the peak detector and varying VAMCAL.

Passes: Verifies the operation of the balanced drivers. No message will be displayed and AutoCal moves to the next step.

Fails: Check the balanced drivers (paragraph 6.8.14). Also, check the -20 dB Attenuator (paragraph 6.8.14).

VSINCAL This check sets the function generator to a 10 kHz sine wave. Then using the notch filter and internal calibration network adjusts the sine wave harmonic distortion.

Passes: Verifies the sine convertor and buffer, variable supply, and notch filter operates correctly. No message will be displayed and AutoCal moves to the next step.

Fails: Check the Sine Buffer, Sine Converter, and Variable Supply. See paragraph 6.8.11.

DLY DIG This step checks the delay digital one-shot's gatable oscillator by setting the pulse generator's trigger frequency to 300 Hz and pulse delay to 1ms. The Microprocessor section measures the delay and stores a delay value representing a 1ms delay.

Passes: Verifies calibration of gatable oscillator. No message will be displayed and AutoCal moves to the next step.

Fails: Check the pulse generator's gatable oscillator (paragraph 6.8.16).

WDTH DIG This step checks the width digital one-shot's gatable oscillator by setting the pulse generator's trigger frequency to 300 Hz and pulse width to 1ms. The Microprocessor section measures the width and stores a width value representing a 1ms width.

Passes: Verifies calibration of gatable oscillator. No message will be displayed and AutoCal moves to the next step.

Fails: Check the width one-shot's gatable oscillator (paragraph 6.8.16).

PUL NORM UPR This check sets the function to external width, the pulse type to normal custom, and the custom lower level to -1.8V. The unit steps the custom upper level from -1.4V to +4.2V. The Microprocessor Section measures and stores correction values of each of the steps.

Passes: Verifies the operation of the Pulse Driver and Level Control DAC. No message will be displayed and AutoCal moves to the next step.

Fails: Check the Pulse Driver (paragraph 6.8.16) and Level Control DAC (paragraph 6.8.16).

PUL COMP UPR This check sets the function to external width, the pulse type to complement custom, and the custom lower level to -1.8V. The unit steps the custom upper level from -1.4V to +4.2V. The Microprocessor Section measures and stores correction values of each of the steps.

Passes: Verifies the operation of the Pulse Driver and Level Control DAC. No message will be displayed and AutoCal moves to the next step.

Fails: Check the Pulse Driver (paragraph 6.8.16) and Level Control DAC (paragraph 6.8.16).

PUL NORM LWR This check sets the function to external width, the pulse type to normal custom, and the custom upper level to +4.2V. The unit steps the custom lower level from +3.8 to -1.8V. The Microprocessor Section measures and stores correction values of each of the steps.

Passes: Verifies the operation of the Pulse Driver and Level Control DAC. No message will be displayed and AutoCal moves to the next step.

Fails: Check the Pulse Driver (paragraph 6.8.16) and Level Control DAC (paragraph 6.8.16).

PUL COMP LWR This check sets the function to external width, the pulse type to complement custom, and the custom upper level to

+4.2V. The unit steps the custom lower level from +3.8 to -1.8V. The Microprocessor Section measures and stores correction values of each of the steps.

Passes: Verifies the operation of the Pulse Driver and Level Control DAC. No message will be displayed and AutoCal moves to the next step.

Fails: Check the Pulse Driver (paragraph 6.8.16) and Level Control DAC (paragraph 6.8.16).

6.8 BLOCK ISOLATION

The following procedures provide a method of isolating faulty circuit blocks.

Paragraph 6.8.1	Function Generator
Paragraph 6.8.2	Triangle Buffer/Comparator
Paragraph 6.8.3	Symmetry Control
Paragraph 6.8.4	VCG Current Sources
Paragraph 6.8.5	Trigger Baseline Compensation
Paragraph 6.8.6	High Frequency Compensation
Paragraph 6.8.7	Frequency Range Switches
Paragraph 6.8.9	Function Generator AutoCal
Paragraph 6.8.10	Sweep Generator
Paragraph 6.8.11	Sine Convertor, Buffer, and Variable Supply
Paragraph 6.8.12	Mode Control and Burst Counter
Paragraph 6.8.13	Trigger Amplifier
Paragraph 6.8.14	Output Section
Paragraph 6.8.15	Frequency Synthesizer and Phase Lock Loop
Paragraph 6.8.16	Pulse Generator
Paragraph 6.8.17	Microprocessor Section
Paragraph 6.8.18	DAC Sample and Hold Network
Paragraph 6.8.19	GPIB Section
Paragraph 6.8.20	Board Interfaces

Most steps use test points; see paragraph 6.6.2.

6.8.1 Function Generator

Refer to the function generator assembly drawing (1101-00-3342) and schematic (1104-00-3342 sheets 2 through 7) in section 7 of this manual. Also, refer to paragraph 5.2 of this manual. Reset the unit by pressing **SHIFT** and **RESET ALL** keys.

1. First check the function generator board's power input. Schematic 1104-00-3342 sheet 1.

TP20	+5 Vdc
TP23	-12 Vdc
TP25	+24 Vdc
TP26	-24 Vdc

2. Check the following test points which will step you forward through the function generator. If the value at a test point is incorrect, isolate and repair the fault of the circuit between the good and bad test points.

22	VLOOP	Locked: +0.1 Vdc (Normal). Unlocked: -0.5 Vdc (Faulty).
TP2	VSUM	-2 Vdc
TP4	-FCV	-4 Vdc.
TP3	+FCV	+4 Vdc
U22A-1	+COMP	~+2.6 Vdc
U22B-7	-COMP	~-2.6 Vdc
TP6	VI+	+17 Vdc.
TP7	VI-	-17 Vdc.
TP9	TRINODE	2.5Vpp Triangle@1kHz.
TP12	TRIOUT	2.5Vpp triangle@1kHz.
TP15	SQWAVE	2.25 Vpp square @ 1kHz.

6.8.2 Triangle Buffer/Comparator

Refer to the function generator assembly drawing (1101-00-3342) and schematic (1104-00-3342 sheets 6 and 7) in section 7 of this manual. Also, refer to paragraph 5.2.2 - Comparator and Triangle Buffer. Reset the unit by pressing **SHIFT** and **RESET ALL** keys.

1. First step through the function generator using the steps in paragraph 6.8.1, and confirm the triangle buffer and comparator circuits are faulty.
2. Check the following test points which will step you through the triangle buffer and comparator. If the value at a test point is incorrect, isolate and repair the fault of the circuit between the good and bad test points.

28	ISWITCH+	 3.5 Vpp @ 1kHz.
29	ISWITCH-	 3.5 Vpp @ 1kHz.
TP9	TRINODE	2.5Vpp Triangle@1kHz
TP12	TRIOUT	2.5Vpp Triangle@1kHz.
27	TRI/SQR	 2.5 Vpp @ 1kHz.
18	SQ1	1Vpp square offset +8 Vdc @ 1kHz.
19	SQ2	4Vpp Square @ 1kHz.
TP15	SQWAVE	2.5Vpp Square@1kHz.
TP13	REFSQR	2.5Vpp square@1kHz.

6.8.3 Symmetry Control

Refer to the function generator assembly drawing (1101-00-3342) and schematic (1104-00-3342 sheet 3) in section 7 of this manual. Also, refer to paragraph 5.2.4. Reset the unit by pressing **SHIFT** and **RESET ALL** keys.

1. First isolate the symmetry control circuit using paragraph 6.8.1.
2. Check the following test points which will step you

through the symmetry control circuit. If the value at a test point is incorrect, isolate and repair the fault of the circuit between the good and bad test points.

TP2	VSUM	-2 Vdc.
21	DAC Ref	-6 Vdc
TP3	+FCV	+4 Vdc
TP4	-FCV	-4 Vdc

3. Verify the data line are active. U12, pins 9, 10, 11, 12, 13, 14, 15, and 16. U17, pins 9, 10, 11, 12, 13, 14, 15, and 16. The following table identifies the enable DAC.

	DS1	DS2	A/B
Pin #	**19**	**20**	**17**
U7C Enabled	1	0	1
U7D Enabled	1	0	0
U12B Enabled	0	1	0
U12A Enabled	0	1	1

6.8.4 VCG Current Sources

Refer to the function generator assembly drawing (1101-00-3342) and schematic (1104-00-3342 sheet 3) in section 7 of this manual. Also, refer to paragraph 5.2.2.2, VCG Current Sources. Reset the unit by pressing **SHIFT** and **RESET ALL** keys.

1. First isolate the symmetry control circuit using paragraph 6.8.1.
2. Check the following test points which will step you through the symmetry control circuit. If the value at a test point is incorrect, isolate and repair the fault of the circuit between the good and bad test points.

TP3	+FCV	+4 Vdc.
TP5	+VCG	+19 Vdc.
TP6	VI+	+17 Vdc.
28	ISWITCH+	⊓⊓ 3.5 Vpp @ 1kHz.
TP4	-FCV	-4 Vdc.
TP8	-VCG	-19 Vdc.
TP7	-VI	-17 Vdc.
29	ISWITCH–	⊔⊔ 3.5 Vpp @ 1kHz.

6.8.5 Trigger Baseline Compensation

Refer to the function generator assembly drawing (1101-00-3342) and schematic (1104-00-3342 sheet 4) in section 7 of this manual. Also, refer to paragraph 5.2.5, Trigger Baseline Compensation. Reset the unit by pressing **SHIFT** and **RESET ALL** keys.

1. First isolate the symmetry control circuit using paragraph 6.8.1. Note, if the generator does not run, check this circuit.
2. Check the following test points which will step you through the trigger baseline compensation circuit. If the value at a test point is incorrect, isolate and repair the fault of the circuit between the good and bad test points.

U19-3	VSOURCE	+17 Vdc
TP5	+VCG	+19 Vdc
TP8	-VCG	-19 Vdc
17	RUN	+4 Vdc for continuous. 0Vdc off.
TP9	TRINODE	2.5 Vpp

6.8.6 High Frequency Compensation

Refer to the function generator assembly drawing (1101-00-3342) and schematic (1104-00-3342 sheet 4) in section 7 of this manual. Also, refer to paragraph 5.2.5. Reset the unit by pressing **SHIFT** and **RESET ALL** keys.

1. First isolate the symmetry control circuit using paragraph 6.8.1.
2. Check the following test points which will step you through the high frequency circuit. If the value at a test point is incorrect, isolate and repair the fault of the circuit between the good and bad test points.

TP3	+FCV	+4 Vdc
U12C-2	Vref	-5 Vdc
U22A-1	+COMP	≈+2.6 Vdc
TP4	-FCV	-4 Vdc
U12A-8	Vref	+5 Vdc
U22B-7	-COMP	≈-2.6 Vdc

3. Verify the data lines are active. U12, pins 9, 10, 11, 12, 13, 14, 15,. The following material identifies the enabled DAC.

	DS1	DS2	A/B
Pin #	**19**	**20**	**17**
U12C Enabled	1	0	1
U12D Enabled	1	0	0

Table 6-4. Frequency Range Capacitors

Range	Capacitors	Control
20 - 2 MHz	50 pF - (15 pF + Stray) C67	None
2MHz - 200 kHz	490 pF - C57, C58, C67	≤$\overline{FR8}$
200 kHz - 20 kHz	0.00519 µF - C55,C57, C58, C67	≤$\overline{FR7}$, ≤$\overline{FR8}$
20 kHz - 2kHz	0.05219 µF - C53,C55,C57, C58, C67	≤$\overline{FR6}$, ≤$\overline{FR7}$, ≤$\overline{FR8}$
2kHz - 200 Hz	0.52219 µF - C52, C53,C55,C57, C58, C67	≤$\overline{FR5}$, ≤$\overline{FR6}$, ≤$\overline{FR7}$ ≤$\overline{FR8}$

Table 6-5 Capacitance Multiplier Ranges

Range	Resistors	Control
200 Hz - 20 Hz	10 kΩ - R67	$\overline{FR4}$
20Hz - 2Hz	110 kΩ - R67, R68	$\overline{FR4}$, $\overline{FR3}$
2Hz - 200 mHz	1.11 MΩ - R67, R68, R69	$\overline{FR4}$, $\overline{FR3}$, $\overline{FR2}$
200 mHz - 20 mHz	11.11 MΩ - R67, R68, R69, R71	All high
20 mHz - 2mHz	See Note	

NOTE

The Model 91 does not switch to the 20 mHz range. It actually keeps the same range capacitors as the 200 mHz range. But the Model 91decreases the input to the VCG Summing Amplifier by 1/10th effectively dropping down a decade range by switching in, $\overline{SCALE}$, an additional input resistor (R8) in series with the VFREQ input.

6.8.7 Frequency Range Switches

Refer to the function generator assembly drawing (1101-00-3342) and schematic (1104-00-3342 sheet 5) in section 7 of this manual. Also, refer to paragraph 5.2.2.3, Frequency Range Capacitors and Ranges. Reset the unit by pressing **SHIFT** and **RESET ALL** keys.

1. First isolate the frequency range capacitor circuit using paragraph 6.8.1.
2. Check the test point, TP9 - TRINODE, for a 2.5 Vpp triangle @ 1kHz.
3. Verify the following frequency range control lines are low: ≤$\overline{FR5}$, ≤$\overline{FR6}$, ≤$\overline{FR7}$ ≤$\overline{FR8}$. Note, in the default settings, the 2kHz to 200 Hz range is selected. For all frequencies above 200 Hz, refer to the control lines and capacitors listed in table 6-4.

6.8.8 Capacitance Multiplier

Refer to the function generator assembly drawing (1101-00-3342) and schematic (1104-00-3342 sheet 6) in section 7 of this manual. Also, refer to paragraph 5.2.2.4, Capacitance Multiplier. Reset the unit by pressing **SHIFT** and **RESET ALL** keys.

1. First verify the function generator operates correctly using paragraph 6.8.1.
2. Change the unit's frequency to 100 Hz. Check the test point, TP11 - CAP MULT, for ⌇⌇ 5Vpp @ 100 Hz.

Also verify the 2KHz range capacitor is selected: 0.52219 µF - C52, C53, C55, C57, C58, C67 (≤$\overline{FR5}$, ≤$\overline{FR6}$, ≤$\overline{FR7}$ ≤$\overline{FR8}$).

For frequencies below 200 Hz, refer to the control lines and capacitors listed in table 6-5.

6.8.9 Function Generator Auto Calibration

Refer to the function generator assembly drawing (1101-00-3342) and schematic (1104-00-3342 sheet 4) in section 7 of this manual. Also, refer to paragraph 5.6.6. This circuit is active only when Autocal is being performed. The following describes the function generator AutoCal mux controls.

A0	A1	A2	Name
U28 Pin	1	16	15
0	0	0	Ground
1	0	0	VSUM
0	1	0	+FCV
1	1	0	-FCV
0	0	1	+COMP
1	0	1	-COMP
0	1	1	TRIBAL
1	1	1	TRICOM

6.8.10 Sweep Generator

Refer to the function generator assembly drawing (1101-00-3342) and schematic (1104-00-3342 sheet 2) in section 7 of this manual. Also, refer to paragraph 5.4.3. Reset the unit by pressing **SHIFT** and **RESET ALL** keys.

1. First verify the function generator operates correctly using paragraph 6.8.1.
2. Select the sweep mode.
3. Check the following test points which will step you through the sweep generator. If the value at a test point is incorrect, isolate and repair the fault of the circuit between the good and bad test points.

J6-39	VSLEN	
U7A-8	Vref	-3 x (VSLEN)
U8-6	Sweep Out	Approx. 3 x (VSLEN)

Check the sweep DAC.

	DS1	DS2	A/B
Pin #	**19**	**20**	**17**
U7A Enabled	0	1	1

Verify the DAC data lines (U7 - 9, 10, 11, 12, 13, 14,15, and 16) step from 00000000 to 11111111.

4. Check the Sweep Out (Ramp) generator test points.

U7A-21	Vref	-6 Vdc
SWEEP OUT Con.		0 to +5V linear ramp.

Check the Sweep Out DAC.

	DS1	DS2	A/B
Pin #	**19**	**20**	**17**
U7A Enabled	0	1	0

Verify the DAC data lines (U7 - 9, 10, 11, 12, 13, 14, 15, and 16) step from 00000000 to 11111111.

6.8.11 Sine Convertor, Buffer, and Variable Supply

Refer to the Phase Lock Loop assembly drawing (1101-00-3438) and schematic (1104-00-33438 sheets 5 and 6) in section 7 of this manual. Reset the unit by pressing **SHIFT** and **RESET ALL** keys.

1. First verify the function generator operates correctly using paragraph 6.8.1.
2. Check the following test points which will step you through the sine wave circuits. If the value at a test point is incorrect, isolate and repair the fault of the circuit between the good and bad test points.

25	TRISIG	2.5 Vpp triangle @ 1kHz.
27	SINSIG	2.5 Vpp triangle @ 1kHz.
TP13	SINCO	0.6 Vpp sine @ 1kHz.
TP10	SIN	2 Vpp sine @ 1kHz.
TP14	+12VADJ	Approximately +12 Vdc.
TP15	-12VADJ	Approximately -12 Vdc.

6.8.12 Mode Control and Burst Counter

Refer to the Pulse board assembly drawing (1101-00-3438) and schematic (1104-00-3438 sheet 4) in section 7 of this manual. Reset the unit by pressing **SHIFT** and **RESET ALL** keys.

1. Check the test point, TP5 - RUN, +4 Vdc.
2. Select the Triggered Mode. Check the test point, TP5 - RUN, 0Vdc.

   Press the Man Trig key on the front panel. TP5 toggles to +4 Vdc and returns to 0Vdc.
3. Refer to paragraph 5.3.5 for a detailed description of the mode control and burst counter circuits.

6.8.13 Trigger Amplifier

Refer to the Pulse board assembly drawing (1101-00-3438) and schematic (1104-00-3438 sheet 3) in section 7 of this manual. Reset the unit by pressing **SHIFT** and **RESET ALL** keys. Connect a 1kHz 1Vpp sine wave to the Trig In connector.

P1-1	1kHz, 1Vpp sine wave
U9A-4	$\overline{\text{PSLOPE}}$ low
U9B-7	$\overline{\text{NSLOPE}}$ high
TP3	EXTRG 1kHz square wave

6.8.14 Output Section

This procedure steps through each block of the output block. Refer to the Output board assembly drawing (1101-00-3335), Motherboard assembly drawing (1101-00-3440), Output board schematic (1104-00-3335) , and Motherboard schematic (1104-00-3440 sheet 7) in section 7 of this manual. Also, refer to the output section circuit description, paragraph 5.3.3.

Check the following test points which will step you through the output section. If the value at a test point is incorrect, isolate and repair the fault of the circuit between the good and bad test points.

1. Square Shaper (schematic 1104-00-3335 sheet 2). Reset the unit by pressing **SHIFT** and **RESET ALL** keys.

   Sine Function Selected

Q2 base	SQRON	~0Vdc

   Square Function Selected

Q2 base	SQRON	>+2.5Vdc
JMP1	SQWAVE	2.25 Vpp square @ 1kHz.
TP1	2V P-P SQUARE	1Vpp square @ 1kHz.
2. Function Selector (schematic 1104-00-3335 sheet 2). Reset the unit by pressing **SHIFT** and **RESET ALL** keys.

   Sine Function Selected

19	PREAMPIN	1Vpp sine @ 1kHz.

   Square Function Selected

19	PREAMPIN	1Vpp square @ 1kHz.

   Triangle Function Selected

19	PREAMPIN	1Vpp triangle @ 1kHz.

   On the Phase Lock Loop Board, (schematic 1104-00-3437 sheet 4),

26	TRIOUT	1.5 Vpp triangle @ 1kHz.
3. Preamplifier and Multiplier (schematic 1104-00-3335 sheet 3). Reset the unit by pressing **SHIFT** and **RESET ALL** keys.

19	PREAMPIN	1Vpp sine @ 1kHz.
TP11	+6V	+6 Vdc
TP12	-6V	-6 Vdc
TP2	PREOUT	1.5 Vpp sine @ 1kHz offset +4 Vdc.
4. AM Summing Amplifier (schematic 1104-00-3437 sheet 6). Reset the unit by pressing **SHIFT** and **RESET ALL** keys.

16	VAMCAL	Approximately 1.55 Vdc.
TP12	AMSIG	-1.5 Vdc.

5. Power Amplifier (schematic 1104-00-3335 sheet 4). Reset the unit by pressing **SHIFT** and **RESET ALL** keys.

TP2	PREOUT	1.5 Vpp sine @ 1kHz offset +4 Vdc.
17	+22V	+22 Vdc
16	-22V	-22 Vdc
TP4	PA_OUT	8Vpp sine @ 1kHz.

6. -20 dB Attenuator (schematic 1104-00-3335 sheet 5). Reset the unit by pressing **SHIFT** and **RESET ALL** keys.

TP4	PA_OUT	8Vpp sine @ 1kHz.
J11-1	UBOUT	5Vpp sine into 50Ω (10 Vpp unterminated).

7. Unbalanced Output Attenuator Network and Impedance Control (schematic 1104-00-3440 sheet 7). Reset the unit by pressing **SHIFT** and **RESET ALL** keys. Turn the Output On.

P11-1	UBOUT	5Vpp sine into 50Ω (10 Vpp unterminated).
Unbal Out Connector		5Vpp sine into 50Ω (10 Vpp unterminated).

8. Balanced Drivers (schematic 1104-00-3335 sheet 5). Reset the unit by pressing **SHIFT** and **RESET ALL** keys. Select the 600Ω Balanced Output. Turn the output On.

18	Bal In	5Vpp sine @ 1kHz.
TP6	BOUT2	5Vpp sine @ 1kHz.
TP7	BOUT1	5Vpp sine @ 1kHz.

9. Balanced Output Attenuator Network and Impedance Control (schematic 1104-00-3440 sheet 7). Reset the unit by pressing **SHIFT** and **RESET ALL** keys. Select the 600Ω Balanced Output. Turn the output On.

   On the Output board, check:

TP6	BOUT2	5Vpp sine @ 1kHz.
TP7	BOUT1	5Vpp sine @ 1kHz.

   On the Motherboard, check:

J21	BAL OUT (-)	5Vpp sine terminated.
J20	BAL OUT (+)	5Vpp sine terminated.

6.8.15 Frequency Synthesizer and Phase Lock Loop

This procedure steps you through the frequency synthesizer and phase lock loop. Also, refer to paragraph 5.3.4.4. Refer to the following drawings:

Synthesizer Module assembly drawing 1101-00-3460

Synthesizer Module schematic 1104-00-3460

Motherboard assembly drawing 1101-00-3440.

Motherboard schematic 1104-00-3440 sheet 4.

Phase Lock Loop assembly drawing 1101-00-3437

Phase Lock Loop schematic 1104-00-3437 sheets 2 and 3.

Reset the unit by pressing **SHIFT** and **RESET ALL** keys.

1. Check the following test points on the frequency synthesizer (schematic 1104-00-3460). If the value at a test point is incorrect, isolate and repair the fault of the circuit between the good and bad test points.

U10-1	REFIN	3.5 Vpp square @ 500 kHz.
U10-8	PREOUT	Alternates between 625 and 615 kHz.
DS1	UNLOCK	Indicator off when locked. May flash when making large frequency changes.
TP7	DNCOUT	
TP3	VCO	80 MHz ECL pulses
TP5	VCO/2	40 MHz ECL pulses
TP6	VCO/4	20 MHz ECL pulses
TP8	TTLVCO/4	20 MHz TTL pulses
TP1	VLOOP	
TP9	SYNTH	1kHz pulses

HF SYNTH Mux (Pulse Trigger Source)

U5-5	$\overline{FR4}$	Selects 50 to 100 MHz
U5-7	$\overline{FR3}$	Selects 25 to 50 MHz
U5-12	$\overline{FR2}$	Selects 12.5 to 25 MHz
U5-13	$\overline{FR1}$	Selects 12.5 MHz and below.

2. Check the following test points on the phase lock loop (schematic 1104-00-3437 sheets 2, 3, and 4). If the value at a test point is incorrect, isolate and repair the fault of the circuit between the good and bad test points.

TP3	SYNTH	⊓⊓⊓ ~4Vp TTL 50 ns pulses @ 1kHz.
TP1	Z-CROSS	~5Vpp Square @ 1kHz.
19	SQWAVE	~3 Vpp Square @ 1kHz
20	1Y	⊓⊓⊓ ~4Vp pulses
21	2Y	~3 Vpp square
22		3.5 Vp pulses
23		3.5 Vp pulses
TP7	VLEADR	⊔⊔⊔ ~4Vp pulses @ 500 Hz.
TP8	VLAGR	⊓⊓⊓ ~4Vp pulses @ 500 Hz.

TP9	PLLER (VLOOP)	Locked: +0.1Vdc Unlocked: -12 Vdc.

3 If Option 001 - Frequency Reference is installed, check the following test points on the phase lock loop (schematic 1104-00-3466).

U4-1	TCXO Output	~4Vpp square @ 10 MHz ± 1ppm.
U3B-12	500KHZ	~3.5 Vpp square @ 500 kHz.
REF OUT	TTL square @ 10 MHz.	

Connect a 10 MHz TTL signal to the Ref In connector.

U1-1	EXTREF	TTL square @ 10 MHz.

6.8.16 Pulse Generator

CAUTION

Running the Pulse Board on Extender boards without a fan could cause the pin driver's temperature sensor to shut down the pin driver's power supplies.

HINT

If running the pulse board on extender cards, use an external fan or remove the pin driver.

1. First check the Pulse board's power input. Schematic 1104-00-3438 sheet 1.

J30A-12	+5 Vdc
J31A-6	-12 Vdc
J31A-8	+12 Vdc

2. Check the following test points which will step you forward through the pulse generator. If the value at a test point is incorrect, isolate and repair the fault of the circuit between the good and bad test points. Reset the unit by pressing **SHIFT** and **RESET ALL** keys. Select normal pulse.

Pulse Generator Trigger Multiplexer

U14-6	$\overline{\text{PMANSEL}}$	Selects Manual Triggered pulses
U14-9	$\overline{\text{SQRSEL}}$	Selects Square wave.
U14-12	SYNTHSL	Selects internal triggered pulses
U14-14	$\overline{\text{EXTSEL}}$	Selects external triggered pulses
TP2	HFSYNTH	1kHz pulses
TP11	DLYIN	3ns pulse @ 1kHz

Delay Select

U15C-10	$\overline{\text{DLDGSEL}}$	Selects digital delay (>10ns)
U15B-6	$\overline{\text{DLALSEL}}$	Selects analog delay (<10ns)
U15A-4	$\overline{\text{DBLSEL}}$	Selects double pulses
TP8	WDIN	3ns pulse @ 1kHz delayed 1us relative DLYIN.

Width Select

U16B-7	$\overline{\text{WDALSEL}}$	Select analog width (<10ns)
U16C-11	$\overline{\text{WDDGSEL}}$	Select digital width (>10ns)
TP9	WDPLS	4ns pulse @ 1kHz delayed 500 ns relative to WDIN.
U17A-3		500 ns wide pulse delayed 1us relative DLYIN

Pulse Output Selector

U18-4	$\overline{\text{EREFSEL}}$	Selects EREF (SH CLK) during AutoCal
U18-9	$\overline{\text{SNEWSEL}}$	Selects square wave function
U18-11	$\overline{\text{PLSSEL}}$	Selects pulse functions
U18-13	DLTSTSL	Selects delay test during AutoCal.

Normal/Complement Select

U19C-14	COMP	Low selects normal pulse. High selects complement pulse.
TP10	$\overline{\text{PLS}}$	500 ns wide pulse delayed 1 us at 1kHz rate.
U10C-10	SQWAVE	500 ns wide pulse delayed 1 us at 1kHz rate.

Pulse Driver

Check the following points on the Pulse Driver (schematic 1104-00-3438 sheet 11 and drawing 1101-00-3438).

C43+	+12V	+12V Input
C44-	-12V	-12V Input
C47+	+10.3V	PIN Driver power source
C48-	-5.8V	PIN Driver power source
Q9 & Q10		0 to 1V differential input to PIN Driver.
R113	ENABLE	+5V to enable PIN driver.
P5	$\overline{\text{PULSE}}$	TTL 500 ns wide pulse delayed 1 us at 1kHz rate.
P6	PULSE	TTL 500 ns wide pulse delayed 1 us at 1kHz rate.

Level Control DAC

Check the following points on the Level Control DAC (schematic 1104-00-3438 sheet 9 and drawing 1101-00-3438).

U34	DAC Out	Check for a dc level (between 0 and +5Vdc) on pins 15, 2, 3, 4, 5, 6, 7, and 10.
U35B-7	VW	Analog width one-shot control voltage (between 0 and +5Vdc).

U35B-1	VD	Analog width one-shot control voltage (between 0 and +5Vdc).
U35D-14	TRGLVL	Trigger level control voltage (between 0 and +5Vdc).
U36A-1	$\overline{\text{PLLVL}}$	PIN driver lower level control voltage (between ±10V offset negative).
U36B-7	PLLVL	PIN driver lower level control voltage (between ±10V offset negative).
U36D-14	$\overline{\text{PULVL}}$	PIN driver upper level control voltage (between ±10V offset negative).
U36C-8	PULVL	PIN driver upper level control voltage (between ±10V offset negative).

6.8.17 Microprocessor Section

1. Check the Microprocessor Section: Schematic 1104-00-3440 Sheet 3 of 10, Assembly drawing 1101-00-3440 sheet 1 of 3. For a description of the Microprocessor Section' circuits, refer to paragraph 5.3.6.2.

2. Observe the Microprocessor's Life Lite. During normal operation the Microprocessor's Life Lite blinks at a rate of about 2 or 3 blinks per second. If the Life Lite blinks, the Microprocessor Section is functioning correctly.

   Non-Blinking Life Lite - Microprocessor Section inoperative. The LED may be continuously on or off. If continuously on, the power supplies are probably operational and the fault is in the microprocessor circuits. If continuously off, the possibility of power supply failure should be checked prior to microprocessor circuit troubleshooting.

3. Check the supply voltages to the circuits within the Microprocessor Section.

U6-7	+5V	Check +5V supply relative to ground U6-1.
U7-1, 22, 43,55	+5V	Check +5V supply relative to ground U6-23, 44, 64, 84.

4. Using the scope, check the control and data lines. Most lines should be "moving". Lines stuck high or low could identify a defective device.

   Microprocessor

U6-6	Reset	Normally high. At power on, remains low to allow power supplies to come up then switches high.
U6-2 & 3	XTAL 1/2	4MHz sinusoid signal ~ 0 to 4V.
U6-40	E-Clock	1MHz 50% duty cycle.
U4-39	AS	1MHz 30% duty cycle address strobe.
U4-5	IRQ	Normally high, goes low when Processor Control Chip or GPIB interrupting.
U4-4	NMI	Wired High
U4-37-30	AD0-AD7	Active, check for stuck bits.
U4-29-22	P40-47	Active, check for stuck bits.

Processor Control Chip

U7-63	MRST	Normally high. At power on, remains low to allow power supplies to come up then switches high.
U7-75	E (E Clock)	1MHz 50% duty cycle.
U7-39	AS	1MHz 30% duty cycle address strobe.
U7-73-66	AD0-AD7	Active, check for stuck bits.
U7-61 - 54	A8 - A15	Active, check for stuck bits.
U7-81 - 83 &2-6	A0 - A7	Active, check for stuck bits.

6.8.18 DAC Sample and Hold Network

Refer to the Motherboard assembly drawing (1101-00-3440 sheet 5) and schematic (1104-00-3440 sheet 5) in section 7 of this manual. Also refer to the circuit description, paragraph 5.3.6.5 of this manual. Reset the unit by pressing **SHIFT** and **RESET ALL** keys.

Check the following test points. If the value at a test point is incorrect, isolate and repair the fault of the circuit between the good and bad test points.

TP7	SHDAC	Verify a stepped waveform.
R33/R34	VOFST	~0Vdc
U21B-7	VAMCAL	Verify a dc voltage.
U22B-7	VSLEN	Verify a dc voltage.
U23B-7	VFREQ	Verify a dc voltage.
U22A-1	VCGZERO	Verify a dc voltage.
U24B-7	VPHASE	Verify a dc voltage.
U21A-1	VSINCAL	Verify a dc voltage.
U24A-1	VTRIBAL	Verify a dc voltage.

6.8.19 GPIB Section

Refer to the Motherboard assembly drawing (1101-00-3440) and schematic (1104-00-3440 sheet 10) in section 7 of this manual. Also refer to the circuit description, paragraph 5.6.3 of this manual.

To troubleshoot the GPIB section,

1. Check the digital control lines to the GPIB board. Verify the overhead signals work correctly (E clock, Read/Write, chip select).
2. Check the address and data lines between the GPIA (U8) and the microprocessor section.
3. Check the lines connecting the GPIA and transceiver (U9 and U10).
4. Check the lines between the transceiver and the GPIB controller.

6.8.20 Board Interfaces

Each of the Model 91's boards contain interface circuits that "translates" address/data information from the microprocessor section for use on the board. Troubleshooting these interfaces by checking the each board's enable lines and verifying the activity on the address and data lines.

Function Generator Board Interface

Schematic: 1104-00-3342 sheet 1.

Assembly: 1101-00-3342

Circuit Description: paragraph 5.3.6.4.1.

Phase Lock Loop Board Interface

Schematic: 1104-00-3437 sheet 1.

Assembly: 1101-00-3437

Circuit Description: paragraph 5.3.6.4.2.

Pulse Board Interface

Schematic: 1104-00-3438 sheet 2.

Assembly: 1101-00-3438

Circuit Description: paragraph 5.3.6.4.3.

Output Board Interface

Schematic: 1104-00-3335 sheet 1.

Assembly: 1101-00-3335

Circuit Description: paragraph 5.3.6.4.4.

Front Panel Interface

Schematic: 1104-00-3322 sheet 2.

Assembly: 1101-00-3322

Circuit Description: paragraph 5.3.6.4.5.

6.9 DISASSEMBLY AND REASSEMBLY

6.9.1 Disassembly

Top Cover/Shield Removal

1. Set the Power switch to Off (extended).
2. Remove the power cable from the rear panel power connector.
3. Remove the five screws that secure the top cover; four in the top and one at the rear.

   Two of the four top cover screws are located under the Calibration Label.
4. Slide the top cover toward the rear and remove. Then lift off the shield.

Bottom Cover Removal

1. Set the Power switch to Off (extended).
2. Remove the power cable from the rear panel power connector.
3. Remove the three screws that secure the bottom cover; one in the bottom cover and two in the rear. The one screw on the bottom cover is located under the Calibration Label.
4. Slide the bottom cover towards the rear and remove.

6.9.2 Board Removal/Replacement

To remove the Output, PLL, Function Generator, or Pulse board,

1. Perform the steps in paragraph 6.9.1 - Top Cover/ Shield Removal.
2. Disconnect the cable from the Output Board. Disconnect the four cables from the Pulse Board.
3. Lift out the board using the extractors.

To replace the Output, PLL, Function Generator, or Pulse board

1. Place the board in its guide and press it down to lock it in the connector
2. Connect the cable to the Output Board. Connect the four cables to the Pulse Board.
3 Perform the steps in paragraph 6.9.3 - Top Cover/ Shield Reassembly.

6.9.3 Reassembly

Bottom Cover Replacement

1. Turn the Model 91 upside down.
2. Slide the bottom cover into the slots on the bottom.
3. Secure the bottom cover with three screws (two in the rear and one on the bottom cover).

Top Cover Replacement

1. Turn the Model right side up.
2. Install the shield, aligning the screw holes.
3. Slide the top cover into the slots on the top.
4. Secure the top cover using five screws (one at the rear and four in the top). The four top cover screws must line up with the holes in the shield.

SECTION 7
PARTS LISTS AND SCHEMATICS

7.1 DRAWINGS

The following assembly drawings, schematics, and parts lists are arranged in order shown below.

7.1.1 Assembly Drawing

All of the mechanical assembly drawings are show in this section. These drawings contain enough detail and clarity to assist the repair technician in the disassembly and reassembly of the Model 91 The parts lists for each assembly drawing immediately follow that drawing.

7.1.2. Schematics

All of the schematics for the Model 91 are shown in this section. Schematic drawings containing a proprietary message may not be copied for resale or use in any other publication nor for any use other than the repair and maintenance of the instrument associated with this manual.

7.1.3 Parts Lists

The parts lists for each individual board or assembly are shown immediately following that board or assembly. The parts lists contain Wavetek and manufacturers parts information. All manufacturers are listed by a Wavetek code designation.

7.2 ADDENDA

Under Wavetek's product improvement program, the latest electronic designs and circuits are incorporated into each Wavetek instrument as quickly as development and testing permits. Because of the time needed to compose and print instruction manuals, it is not always possible to include the most recent changes in the initial printing. Whenever this occurs, addendum pages are prepared to summarize the changes made and are inserted immediately inside the rear cover. If no such pages exist, the manual is correct as printed.

7.3 ORDERING PARTS

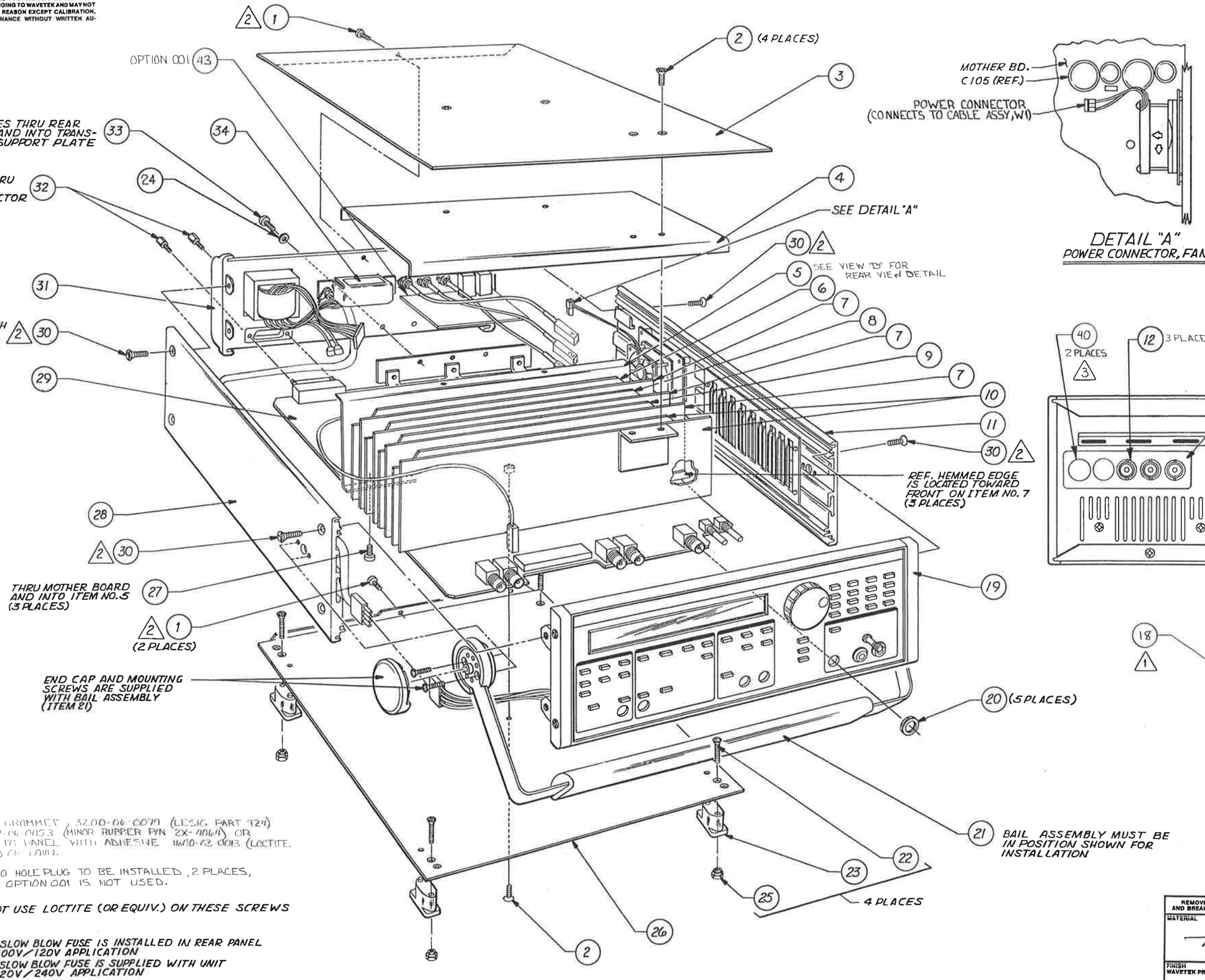
When ordering spare parts, please specify the part number, circuit reference, board, serial number of the unit, and, if applicable, the function performed.

The number etched into a printed circuit board is the board part number. The assembly (Printed circuit board and components on the board) part number is stamped on the board.

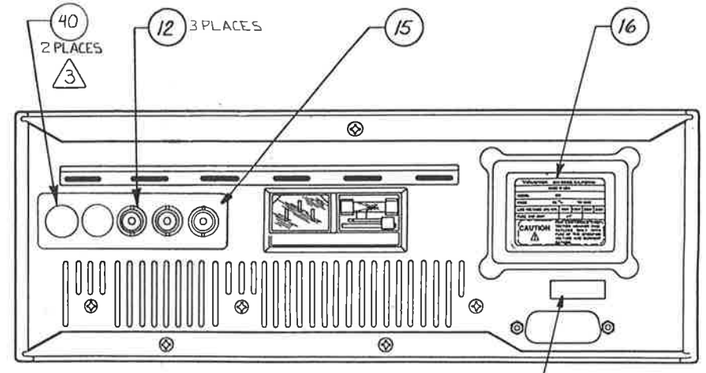
DRAWING	DRAWING NUMBER
Top Assembly Drawing	1001-00-0649
Instrument Schematic	1004-00-0649
Instrument Parts List	1000-00-0649
Installation Drawing	0002-00-0649
Motherboard Schematic	1104-00-3440
Motherboard Assembly	1101-00-3440
Motherboard Parts List	1100-00-3440
	1200-00-3440
Synthesizer Schematic	1104-00-3597
Synthesizer Assembly	1101-00-3597
Synthesizer Parts List	1100-00-3597
Front Panel Assembly	1101-00-3439
Front Panel Assembly Parts List	1100-00-3439
Display / Keyboard Assembly Schematic	1104-00-3322
Display / Keyboard Assembly	1101-00-3322

DRAWING	DRAWING NUMBER
Display / Keyboard Assembly Parts List	1100-00-3322
Output Board Schematic	1104-00-3335
Output Board Assembly	1101-02-3335
Output Board Parts List	1100-00-3335
Phase Lock Board Schematic	1104-00-3437
Phase Lock Board Assembly	1101-00-3437
Phase Lock Board Parts List	1100-00-3437
Function Generator Board Schematic	1104-00-3342
Function Generator Board Assembly	1101-00-3342
Function Generator Board Parts List	1100-00-3342
Pulse Board Schematic	1104-00-3438
Pulse Board Assembly	1101-00-3438
Pulse Board Parts Lists	1100-00-3438 1200-00-3438
Rear Panel Assembly	1101-00-3441
Rear Panel Assembly Parts List	1100-00-3441
Option 001 TCXO Assembly	1001-00-0663
Option 001 TCXO Parts Lists	1000-00-0663
TCXO Schematic	1104-00-3466
TCXO Assembly	1101-00-3466
Rack/Handle Assembly	1101-00-3353
Rack/Handle Parts List	1100-00-3353
Recommended Spares Parts List	1200-00-3480

REV	ECO	BY	DATE	APP
A	ERO NO. 91-328	MS	7-10-91	



DETAIL "A"
POWER CONNECTOR, FAN



△3 INSTALL GROMMET, 3200-06-0079 (LESSIC. PART 924) OR 3200-06-0053 (MINOR RUBBER P/N 2X-4066A) OR EQUIV. TO PANEL WITH ADHESIVE 1600-02-0003 (LOCTITE P/N 401) OR EQUIV.

△3 ITEM 40 HOLE PLUG TO BE INSTALLED, 2 PLACES, WHEN OPTION 001 IS NOT USED.

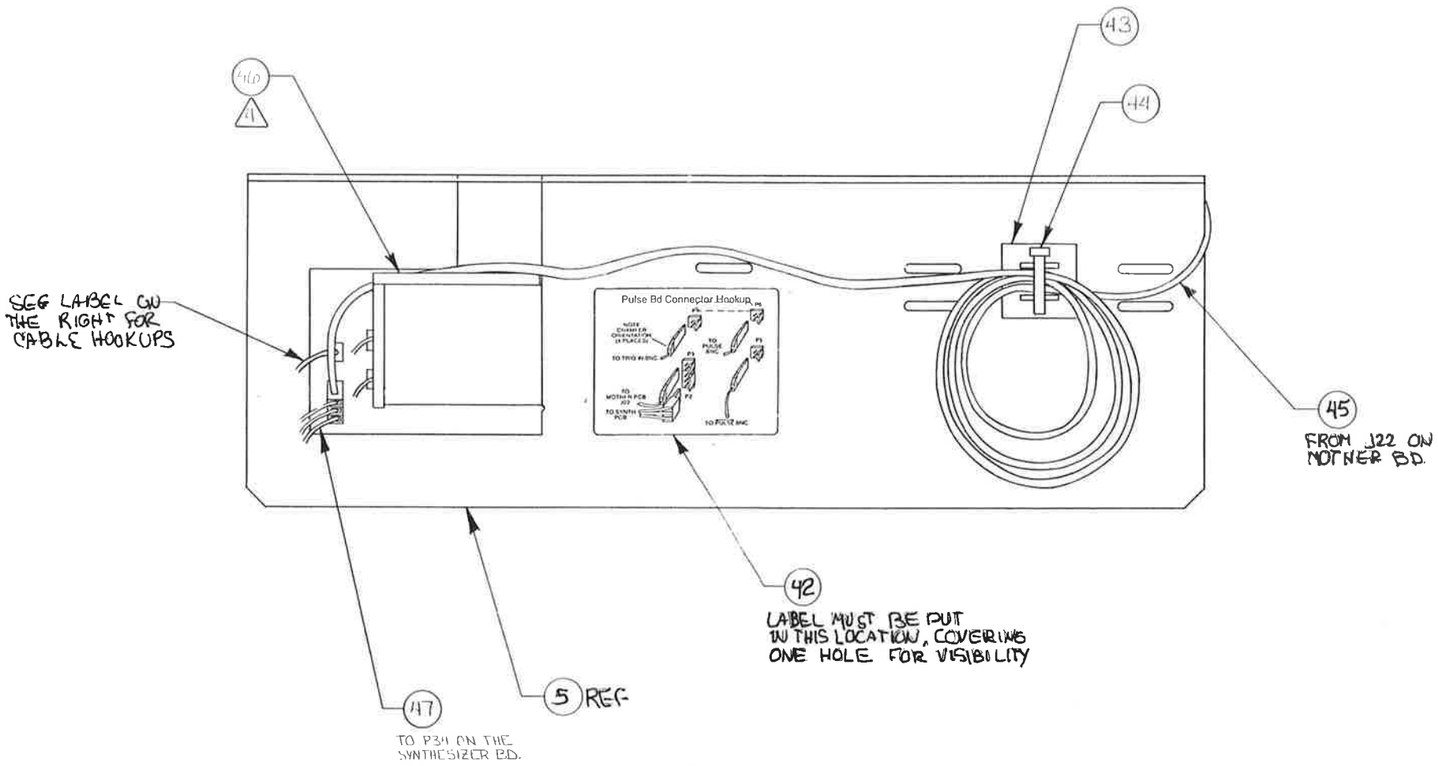
△2 DO NOT USE LOCTITE (OR EQUIV.) ON THESE SCREWS

△1 1. 5A 250V SLOW BLOW FUSE IS INSTALLED IN REAR PANEL FOR 100V/120V APPLICATION
3/4A 250V SLOW BLOW FUSE IS SUPPLIED WITH UNIT FOR 220V/240V APPLICATION

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN D. COOPER	DATE 5-11-90	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	CHECKED	7/12/91	TITLE: TOP ASSEMBLY DRAWING
	MFG. ENGR.	7/12/91	
FINISH WAVETEK PROCESS	RELEASE APPROV.	7/12/91	
DO NOT SCALE DRAWING	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS ± / DECIMALS XX ± / XXX ± / ANGLES ± /		SIZE D · FSCM NO. 23338 · DWG. NO. 1001-00-0649 · REV A · SCALE NONE · MODEL 91 · SHEET 1 OF 2

REV	ECO	BY	DATE	APP



VIEW B

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE
MATERIAL	CHECKED SWA	7/12/91
	PROJ. ENGR. Gus B Mu Gu	7/24/91
	RELEASE APPROV.	
FINISH WAVETEK PROCESS	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES .XX ± .XXX °	
DO NOT SCALE DRAWING		

WAVETEK SAN DIEGO, CALIFORNIA

TITLE: TOP ASSEMBLY DRAWING

SIZE	FSCM NO.	DWG. NO.	REV
D	23338	1001-00-0694	A

SCALE NONE | MODEL 91 | SHEET 2 OF 2

REV	ECO	BY	DATE	APP
A	ERO:# 91328	MS	7-9-91	

"HOT" "COM" "NEUT"

F1 1.5 ASB

REAR PANEL

T1

CORCOM 6J4

1A3A1

BLK
VIO
WHT/BLK
GRY
WHT/GRY

L N B J

GRN/YEL

AWG 22 WHT
AWG 22 RED
AWG 22 BLK
AWG 22 GRN

REAR PANEL

RIGHT SIDE PLATE ASSEMBLY

FAN

RED BLK

J1

GND -FAN

MOTHER BOARD PCA

P3 J3

ON

1A1SW1

POWER OFF

FRONT PANEL ASSEMBLY

NOTE: UNLESS OTHERWISE SPECIFIED

AWG 24 BLU
AWG 24 BLU
AWG 24 GRN
AWG 24 WHT/GRN
AWG 24 GRN
AWG 24 ONG
AWG 24 WHT/ONG
AWG 24 ONG
AWG 24 RED
AWG 24 WHT/RED
AWG 24 RED

REAR PANEL ASSEMBLY

J4 P4 — +/- 22V SUPPLY INPUT
J22 P22 — +/- 12V SUPPLY INPUT
J23 P23 — VFD FILAMENT SUPPLY
+5V SUPPLY INPUT

PULSE PULSE TRIGIN

P6 PULSE GND
P5 PULSE GND
P1 TRIG GND

TCXO OPTION

J3 GND
J2 REFOUT
REFIN GND

+5V
+5V
EXTDET
EXTEN
-5V
OPTOVM2
500 KHZ
10MHZ
GND
GND

P35

(MOTHER BOARD)

GPIB CONNECTOR

DIO1 DIO2 DIO3 DIO4 EOI DAV NRFD NDAC IFC SRQ ATN DIO5 DIO6 DIO7 DIO8 REN GND GND GND GND GND GND

REAR PANEL

PULSE BOARD

J30 P30

SQWAVE SYNTH DGND QA0 QA2 DGND QD6 QD4 QD2 QD0 DGND +5PV AGND AGND AGND N/C N/C N/C MOD_IN BXFREQ PLS/SQR DGND OXSTB QA1 QA3 QD7 QD5 QD3 QD1 DGND +5PV AGND OBSTG AGND SHCLK N/C N/C N/C

SYNC GND
P3

HFSYNTH GND HFSYNTH
P2

J31 P31

OXDVM AGND SQR RUN AGND -12PV AGND +12PV AGND +22PV AGND -22PV OPTDVM AGND SQR OSCIN AGND -12PV AGND +12PV AGND +22PV AGND -22PV

FUNCTION GENERATOR PCA

J6 P6

SQWAVE SYNTH PLSTB QA0 QA2 DGND QD6 QD4 QD2 QD0 DGND +5PV AGND N/C AGND TRIOUT AGND VLOOP AGND MOD_IN BXFREQ PLS/SQR DGND FGSTB QA1 DGND QD7 QD5 QD3 QD1 DGND +5PV AGND N/C AGND VCGZERO VFREQ FGTST VSLEN AGND

J7 P7

SWPOUT TRISIG VIATBAL AGND AGND -12PV AGND +12PV AGND +22PV AGND -22PV FGTST100 AGND SQR RUN AGND -12PV AGND +12PV AGND +22PV AGND -22PV

SYNTHESIZER BOARD (1/2)

J32 P32

GND SCLK SDATA GND SCSN MRES GND XFR2 XFR1 GND REFIN REFOUT GND GND FREF VREF GND LOCK GND SYNTH GND GND HFSYNTH HFSYNTH GND GND

HFSYNTH GND HFSYNTH
P34

SYNTHESIZER BOARD (1/2)

J33 P33

GND +12V +12V GND -12V GND +5V +5V GND GND +12V +12V GND -12V GND -12V GND +5V +5V GND

PHASE LOCK LOOP PCA

J8 P8

SQWAVE SYNTH DGND QA0 QA2 TRISEL QD6 QD4 QD2 QD0 DGND +5PV AGND N/C AGND TRIOUT1 AGND AMSIG AGND SIN1 BXFREQ PLS/SQR DGND PLSTB QA1 DGND QD7 QD5 QD3 QD1 DGND +5PV AGND N/C AGND TRIOUT AGND VLOOP AGND VPHASE

J9 P9

MOD_IN AGND TRISIG AGND AGND -12PV AGND +12PV AGND +22PV AGND -22PV AGND AGND AGND VAMCAL VSINCAL AGND -12PV AGND +12PV AGND +22PV AGND -22PV

OUTPUT BOARD PCA

J10 P10

SQWAVE SYNTH DGND QA0 QA2 TRISEL QD6 QD4 QD2 QD0 DGND +5PV AGND AGND CLK0 TRIOUT AGND AMSIG AGND VOFST BXFREQ PLS/SQR DGND FGSTB QA1 DGND QD7 QD5 QD3 QD1 DGND +5PV AGND N/C OPTSIG AGND TRIOUT AGND AMSIG AGND SIN1

J11 P11

UBOUT AGND BOUT1 BOUT2 AGND -12PV AGND +12PV AGND +22PV AGND -22PV THD AGND -PK +PK AGND -12PV AGND +12PV AGND +22PV AGND -22PV

J22 SYNC GND
AGND

J12 P12

GND FP5 QA0 QA1 QD6 QD7 QD4 QD5 QD2 QD3 QD0 QD1 GND GND P10 P11 P12 P13 P14 P15 P16 P17 GND GND +5PV +5PV CHA GND CHB FIL_A FIL_B GND GND +22PV +22PV GND GND -22PV -22PV

DISPLAY/KEYBOARD PCA

P13 J13

AWG 22 BLK

J14

"CT"

SYNC-OUT J15 — SYNC OUT
DGND
XFREQ IN J16 — EXT FREQ IN
GND
MOD_IN J17 — MOD/VCF IN
GND
SWPOUT J18 — SWEEP OUT
RAG4
UBOUT ATTN J19 — UNBAL OUT
GND
BOUT1 ATTN J20 — (+) BAL OUT
BOUT2 ATTN J21 — (-) BAL OUT

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN A. TARO FIFER	DATE 10-17-90	WAVETEK SAN DIEGO, CALIFORNIA	
MATERIAL	CHECKED JM	7/12/91	TITLE SCHEMATIC, INSTRUMENT	
	PROJ. ENGR.	7/12/91		
FINISH WAVETEK PROCESS	RELEASE APPROV.	7/12/91		
DO NOT SCALE DRAWING	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES ± .XX ± .XXX ± ±		SIZE D / FSCM NO. 23338 / DWG. NO. 1004-00-0649 / REV A	
			SCALE NONE / MODEL 91 / SHEET 1 OF 1	

1004-00-0649 A

REV	ECO	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
52	SCREW, 6-32 X 1/2, FH, ZINC, 100 DEG	0203-00014	VIC-T	0203-00014	2
REF	A/D TOP MODEL 91	1001-00-0649	WVTK	1001-00-0649	1
REF	ACCEPTANCE TEST SPECIFICATION MODEL 91	1002-00-0649	WVTK	1002-00-0649	1
NONE	INSTRUMENT SCHEMATIC MODEL 91	1004-00-0649	WVTK	1004-00-0649	1
NONE	MANUAL MODEL 91 OPERATORS	1006-00-0649-01	WVTK	1006-00-0649	1
NONE	MANUAL MODEL 91 MAINTENANCE	1006-00-0649-02	WVTK	1006-00-0649	1
NA	QUICK REFERENCE GUIDE MODEL 91	1006-00-0649-03	WVTK	1006-00-0649	1
REF	CALIBRATION PROCEDURE MODEL 91	1008-00-0649	WVTK	1008-00-0649	1
16	S/N LABEL/INFO MODEL 91	1009-00-0649	WVTK	1009-00-0649	1
10	PCA, OUTPUT BOARD	1100-00-3335	WVTK	1100-00-3335	1
8	PCA, FUNCTION GENERATOR	1100-00-3342	WVTK	1100-00-3342	1
9	PCA, PHASE LOCK LOOP	1100-00-3437	WVTK	1100-00-3437	1

WAVETEK PARTS LIST | TITLE: MODEL 91, 20 MHz SYNTHESIZED | ASSEMBLY NO. 1000-00-0649 | REV D

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
	ORIENTATION				
32	HARDWARE KIT, GPIB CONN	554808-1	AMP	2100-07-0024	1
18	FUSE, 1 1/2A, 250V, S-B	MDX 1-1/2	BUSS	2400-05-0021	1
43	MOUNT, ADHESIVE	ABMS-A-C	PANDT	2800-00-0001	1
44	TY-WRAP	TY-523M	TB	2800-00-0006	1
51	HANDLE, RETRACTABLE	2800-07-0035	WAVTK	2800-07-0035	1
54	FOOT	10603-026	SCHRF	2800-08-0020	2
53	FOOT WITH TIP-UP	10603-025	SCHRF	2800-08-0021	2
20	NUT, HEX, 1/2-28	1-329631-2	AMP	2800-16-0025	5
25	NUT, HEX, 8-32, 3/32 THK, .25 FLT, MINI, SS	2800-16-8106	CMCRL	2800-16-8106	4
40	HOLE PLUG, .562 DIA, BLK	DP562BLK/2653	HEYCO	2800-35-0010	2
24	LOCKWASHER, #8 SPLIT RING, SS	#8SRLW	CMRCL	2800-42-8000	7
1	SCREW PLPS PAN M/S 18-8 S/S 6-32X3/8	MS 51957-28	CMRCL	2800-48-6106	3
33	SCREW PLPS PAN M/S 18-8 S/S 8-32X1/2	SCREW PH 8-32X1/2	CMRCL	2800-48-8108	3

WAVETEK PARTS LIST | TITLE: MODEL 91, 20 MHz SYNTHESIZED | ASSEMBLY NO. 1000-00-0649 | REV D

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
6	PCA, PULSE BD	1100-00-3438	WVTK	1100-00-3438	1
19	FRONT PANEL ASSY	1100-00-3439	WVTK	1100-00-3439	1
29	MOTHERBOARD ASSY-91	1100-00-3440	WVTK	1100-00-3440	1
31	REAR PANEL ASSY - 91	1100-00-3441	WVTK	1100-00-3441	1
47	SYNTHESIZER CABLE ASSY	1200-00-3524	WVTK	1200-00-3524	1
45	CABLE ASSY, COAX, 28"	1200-00-3532	WVTK	1200-00-3532	1
11	SIDE PANEL ASSY, RIGHT	1200-00-3582	WVTK	1200-00-3582	1
28	LEFT SIDE PANEL	1200-00-3593	WVTK	1200-00-3593	1
34	LABEL, CAUTION	859-1400	WVTK	1400-01-1400	1
7	SHIELD, INNER	1400-02-3323	WVTK	1400-02-3323	3
4	SHIELD, TOP	1400-02-3353	WVTK	1400-02-3353	1
3	COVER, TOP	1400-02-3532	WVTK	1400-02-3532	1
26	COVER, BOTTOM	1400-02-4522	WVTK	1400-02-4522	1
5	REAR SHIELD-91	1400-02-5149	WVTK	1400-02-5149	1
15	LABEL, BNC CONNECTOR	1400-02-5150	WVTK	1400-02-5150	1
42	LABEL, CABLE	1400-02-5170	WVTK	1400-02-5170	1

WAVETEK PARTS LIST | TITLE: MODEL 91, 20 MHz SYNTHESIZED | ASSEMBLY NO. 1000-00-0649 | REV D

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
30	SCREW, 8-32X7/16, 100DEG FH, PHLPS, SS	2800-54-8107	CMCRL	2800-54-8107	8
22	SCREW, 8-32 X 1/2, 100 DEG, FH, PHLPS, SS	2800-54-8108	CMCRL	2800-54-8108	4
27	SCREW, PH, 6-32 X 5/16, PHLPS, NYLOK, SS	2800-59-6105	CMRCL	2800-59-6105	3
2	SCREW, 6-32/3/8, FH, PHLPS, 100DEG, SS, NYLOK, PATCH	2800-60-6106	CMRCL	2800-60-6106	5
46	EXTRU, RUBBER, U CHNL, 1/16 INSIDE, 1/8 OUTSIDE	924	LESIQ	3200-06-0079	5
NONE	CARTON, 21 1/2x21x12 1/4	3300-00-0023	WVTK	3300-00-0023	1
NONE	PWR CORD, SHIELDED	6001-80-0009	WVTK	6001-80-0009	1
12	CABLE ASSY, 50 OHM COAX, BNC-PINS, 101/4LG	98-0300-5796-6	3M	6002-01-0000	3

WAVETEK PARTS LIST | TITLE: MODEL 91, 20 MHz SYNTHESIZED | ASSEMBLY NO. 1000-00-0649 | REV D

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE
MATERIAL	CHECKED	
	PROJ. ENGR.	
	RELEASE APPROV.	
FINISH WAVETEK PROCESS	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES ± .XX ± .XXX ± °	
DO NOT SCALE DRAWING		

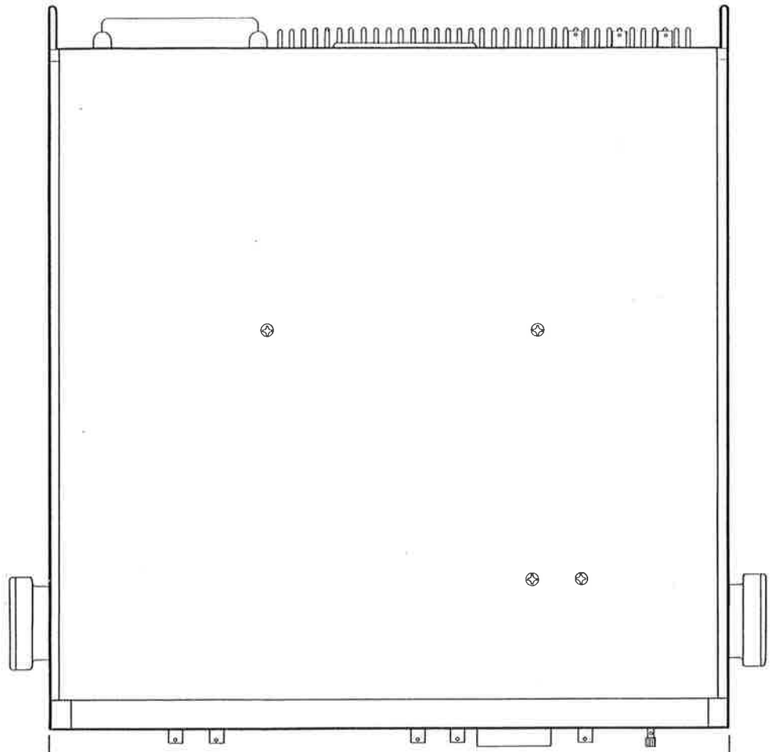
WAVETEK SAN DIEGO • CALIFORNIA

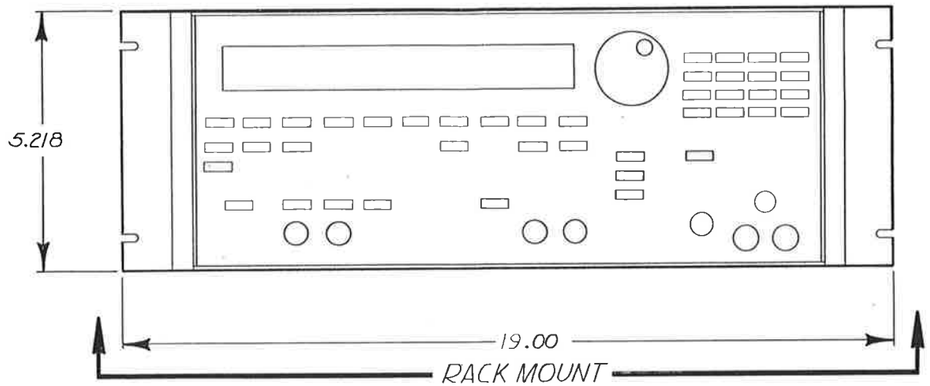
TITLE: MODEL 91 20 MHZ SYNTHESIZED

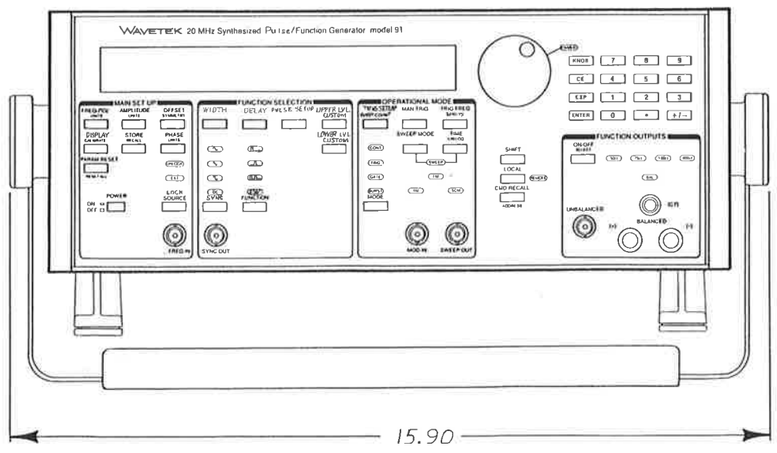
SIZE	FSCM NO.	DWG. NO.	REV
D	23338	1000-00-0649	D

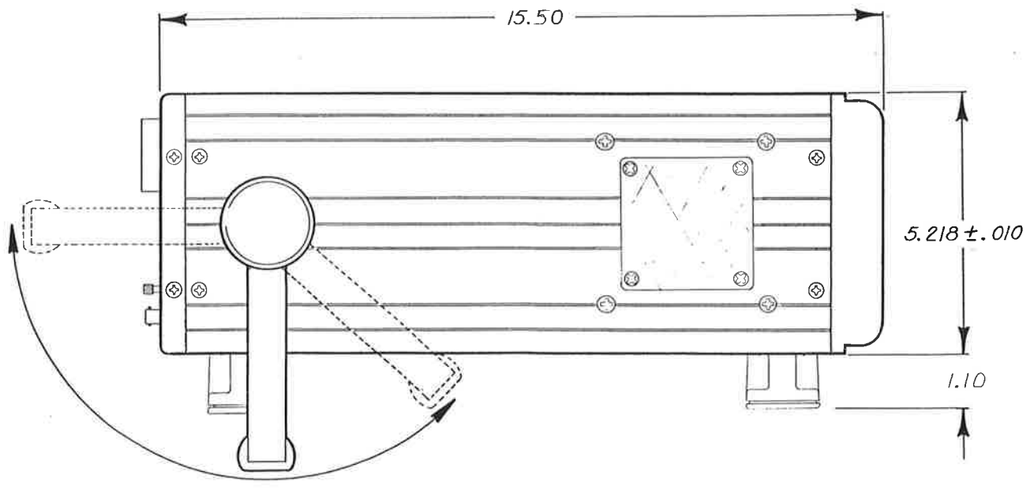
SCALE | MODEL 91 | SHEET 1 OF 1

REV	ECO	BY	DATE	APP
A	ERO NO. 5[illegible]	[illegible]	[illegible]	[illegible]









NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN RO FIFER	DATE 4-8-91	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	CHECKED [illegible]	6/10/91	TITLE: INSTALLATION DRAWING
	PROJ. ENGR [illegible]	7/12/91	
FINISH WAVETEK PROCESS	RELEASE APPROVED [illegible]	7/12/91	
DO NOT SCALE DRAWING	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES ± / .XX ± .05 .XXX ± .020 ± 1°		SIZE D · FSCM NO. 23338 · DWG. NO. 0002-00-0649 · REV A · SCALE 3/4 · MODEL 91 · SHEET 1 OF 1

0002-00-0649 | A

REV	ECO	BY	DATE	APP
A	PROTO BUILD	---	---	---
B	ERO NO. 91-325	JMT	4/24/91	KMA

POWER SUPPLY AC INPUT UNREGULATED

P4
- 1, 2, 3 — +/-12V SUPPLY UNREGULATED VOLTAGE
- 4, 5, 6 — VFD FILAMENT SUPPLY
- 7, 8, 9, 10 — +/-24 SUPPLY UNREGULATED VOLTAGE

P23 / P22 — +5V REGULATED SUPPLY

FRONT PANEL BOARD CONNECTOR

J12

DGND	1	2	QA0
QD6	3	4	QD4
QD2	5	6	QD0
DGND	7	8	P10
P12	9	10	P14
P16	11	12	DGND
+5PV	13	14	DGND
DGND	15	16	FIL_A
DGND	17	18	+24PV
DGND	19	20	-24PV
FPSTB	21	22	QA1
QD7	23	24	QD5
QD3	25	26	QD1
DGND	27	28	P11
P13	29	30	P15
P17	31	32	DGND
+5PV	33	34	AKA
AKB	35	36	FIL_B
DGND	37	38	+24PV
DGND	39	40	-24PV

OUTPUT BOARD CONNECTORS

P10

SQWAVE	1	2	SYNTH
DGND	3	4	QA0
QA2	5	6	TRISEL
QD6	7	8	QD4
QD2	9	10	QD0
DGND	11	12	+5PV
AGND	13	14	
CLKO	15	16	TRIOUT1
AGND	17	18	AMSIG
AGND	19	20	VOFST
BXFREQ	21	22	PLS/SQR
DGND	23	24	OBSTB
QA1	25	26	DGND
QD7	27	28	QD5
QD3	29	30	QD1
DGND	31	32	+5PV
AGND	33	34	OBSIG
AGND	35	36	MOD_IN
AGND	37	38	AMSIG
AGND	39	40	SIN1

P11

UBOUT	1	2	AGND
BOUT1	3	4	BOUT2
AGND	5	6	-12PV
AGND	7	8	+12PV
AGND	9	10	+24PV
AGND	11	12	-24PV
THD	13	14	AGND
-PK	15	16	+PK
AGND	17	18	-12PV
AGND	19	20	+12PV
AGND	21	22	+24PV
AGND	23	24	-24PV

PHASE LOCK LOOP BOARD CONNECTORS

P8

SQWAVE	1	2	SYNTH
DGND	3	4	QA0
QA2	5	6	TRISEL
QD6	7	8	QD4
QD2	9	10	QD0
DGND	11	12	+5PV
AGND	13	14	*
*	15	16	TRIOUT1
AGND	17	18	AMSIG
AGND	19	20	SIN1
BXFREQ	21	22	PLS/SQR
DGND	23	24	PLSTB
QA1	25	26	DGND
QD7	27	28	QD5
QD3	29	30	QD1
DGND	31	32	+5PV
AGND	33	34	*
*	35	36	AGND
AGND	37	38	VLOOP
AGND	39	40	VPHASE

P9

MOD_IN	1	2	AGND
TRISIG	3	4	AGND
-12PV	5	6	AGND
+12PV	7	8	AGND
+24PV	9	10	AGND
-24PV	11	12	AGND
VAMCAL	13	14	VSINCAL
AGND	15	16	-12PV
AGND	17	18	AGND
+12PV	19	20	AGND
+24PV	21	22	AGND
-24PV	23	24	

FUNCTION GENERATOR BOARD CONNECTORS

P6

SQWAVE	1	2	SYNTH
PLSTB	3	4	QA0
QA2	5	6	DGND
QD6	7	8	QD4
QD2	9	10	QD0
DGND	11	12	+5PV
AGND	13	14	*
*	15	16	*
AGND	17	18	VLOOP
AGND	19	20	MOD_IN
BXFREQ	21	22	PLS/SQR
DGND	23	24	FGSTB
QA1	25	26	DGND
QD7	27	28	QD5
QD3	29	30	QD1
DGND	31	32	+5PV
AGND	33	34	*
*	35	36	VCGZERO
VFREQ	37	38	FGTST
VSLEN	39	40	AGND

P7

SWPOUT	1	2	TRISIG
VTRIBAL	3	4	AGND
-12PV	5	6	AGND
+12PV	7	8	AGND
+24PV	9	10	AGND
-24PV	11	12	FGTST100
AGND	13	14	SQR
RUN	15	16	AGND
-12PV	17	18	AGND
+12PV	19	20	AGND
+24PV	21	22	AGND
-24PV	23	24	

AUXILLARY BOARD CONNECTORS

P30

SYNTH	SQWAVE	1	2
	DGND	3	4 QA0
	QA2	5	6 DGND
	QD6	7	8 QD4
	QD2	9	10 QD0
	DGND	11	12 +5PV
	AGND	13	14
		15	16 *
		17	18 *
		19	20 MOD_IN
	BXFREQ	21	22 PLS/SQR
	DGND	23	24 OXSTB
	QA1	25	26 QA3
	QD7	27	28 QD5
	QD3	29	30 QD0
	DGND	31	32 +5PV
	AGND	33	34 OBSIG
	AGND	35	36 SHCLK
		37	38
JMP8	SEXDIVEX	39	40 POE

8

P31

	OPTDVM1	1	2 AGND
SQR		3	4 RUN
	AGND	5	6 -12PV
	AGND	7	8 +12PV
	AGND	9	10 +24PV
	AGND	11	12 -24PV
	OPTDVM2	13	14 AGND
		15	16 500KHZ
	AGND	17	18 -12PV
	AGND	19	20 +12PV
	AGND	21	22 +24PV
	AGND	23	24 -24PV

9. INSTALL JMP10 ON PINS 1 & 2 FOR MODEL 91. INSTALL ON PINS 2 & 3 FOR MODELS 90 AND 95.
8. INSTALL JMP8 FOR MODELS 90 AND 95.
7. ⏚D =DGND, ⏚A =AGND.
6. SEE BILL OF MATERIALS FOR PROGRAMMED PART NUMBER.
5. * = PART INSTALLED IN SOCKET.
4. CAPACITORS VALUED IN MICROFRADS (uF).
3. RESISTORS VALUED IN OHMS, 1/8W, 1%.
2. FOR INSTRUMENT INTERCONNECTION, SEE THE INSTRUMENT SCHEMATIC.
1. INSTALL JMP1 ON PINS 1 & 2 FOR BIPOLAR EXT FREQ INPUTS. INSTALL ON PINS 2 & 3 FOR TTL EXT FREQ INPUTS.

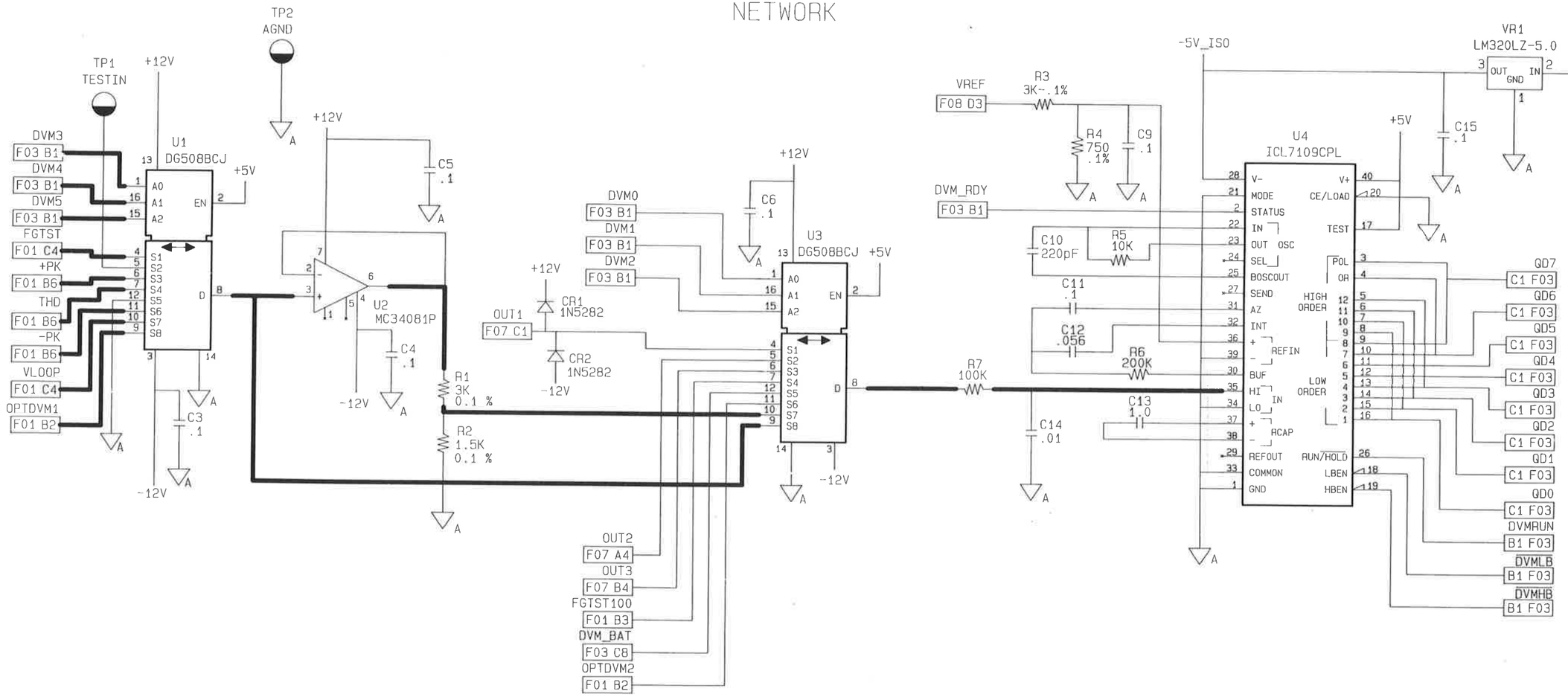
NOTE UNLESS OTHERWISE SPECIFIED

CAD JOB #: B076B

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN FIFER A.Talmadge-Lee	12/90	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	CHECKED JMT	4/24/91	TITLE: SCHEMATIC, MOTHER BOARD
	PROJ. ENGR.	4/24/91	
	RELEASE APPROV.	5/1-/91	
FINISH WAVETEK PROCESS	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES .XX ± .XXX ± °		SIZE D · FSCM NO. 23338 · DWG. NO. 1104-00-3440 · REV B
DO NOT SCALE DRAWING			SCALE NONE · MODEL 91 · SHEET 1 OF 10

REV	ECO	BY	DATE	APP

DVM
INTERNAL CALIBRATION NETWORK



CAD JOB #: B076B

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN A.Talmadge-Lee	DATE 12/90	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	CHECKED JM	6/26/91	TITLE: SCHEMATIC, MOTHER BOARD
	PROJ. ENGR.	6/26/91	
FINISH WAVETEK PROCESS	RELEASE APPROV.		
DO NOT SCALE DRAWING	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES: FRACTIONS DECIMALS ANGLES ± .XX ± .XXX ± ±		SIZE D · FSCM NO. 23338 · DWG. NO. 1104-00-3440 · REV B · SCALE NONE · MODEL 91 · SHEET 2 OF 10

REV	ECO	BY	DATE	APP

MICRO PROCESSOR SECTION

+5V
R8 10K
C17 .1
U5 TL7705A
SENSE RESIN CT REF RESET RESET
C18 22
C19 .1
SW1 39-405
DVM_BAT B5 F02
R9 10K
R10 10K
R11 10K
R12 49.9K
R13 274
R14 49.9K
Q11 VN10KM
CR6 LTL-3231A
Q1 2N3904
CR4 HP2811
CR5 MBR120
R15 2.21K
BT1 BR2/3A
C150 7-35pF
C20 15pF
C21 68pF-NOM
Y1 4MHz
C22 .1
U6 MC6803L
XTAL1 XTAL2 RESET E R/W AS
AD0 P30 AD1 P31 AD2 P32 AD3 P33 AD4 P34 AD5 P35 AD6 P36 AD7 P37
CR3 HP2811
P20 TIN P21 TOUT P22 SCLK P23 RX P24 TX
A8 P40 A9 P41 A10 P42 A11 P43 A12 P44 A13 P45 A14 P46 A15 P47
NMI IRQ
P10 F01 D7
P11 F01 C7
P12 F01 D7
P13 F01 C7
P14 F01 D7
P15 F01 C7
P16 F01 D7
P17 F01 D7
E C7 F10
R/W C7 F10
MRST B4 F04 B4 F10 C7 F10
C23 .1
C24 .1
R133 10K
U7 * PSC288
MRST VCC IRQ WE PRST
E R/W AS
AD0 AD1 AD2 AD3 AD4 AD5 AD6 AD7
GPIB ROM RAM
FPS OBS LBS OXB
QA0 QA1 QA2 QA3
QD0 QD1 QD2 QD3 QD4 QD5 QD6 QD7
SEN SDAT SCK
SHSEL0 SHSEL1 SHSEL2 SHSEQM SHCLK SHDATA SHEN
DVMHB DVMLB DVM5 DVM4 DVM3 DVM2 DVM1 DVM0 DVMRUN DVMRDY
VSS
C6 F10
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15
SQWAVE F01 D6
BXFREQ F01 C6
SEXDIVEX F01 B1
FREQOUT SQWAVE BXFREQ SYNTH
RKA F01 C7
RKB F01 C7
C147 .01
C146 .01
IRQ C5 F10
POE D6 F01
GPIB C7 F01
FPSTB D7 F01
OBSTB D5 F01
FGSTB C6 F01
OXSTB C3 F01
QA0 D1 F01
QA1 D1 F01
QA2 D1 F01
QA3 C3 F01
QD0 B8 F07
QD1 B8 F07
QD2 B8 F07
QD3 B8 F07
QD4 B8 F07
QD5 B8 F07
QD6 B8 F07
QD7 B8 F07
SEN D8 F04
SDATA D8 F04
SCLK B8 F04
SHSEL0 C8 F05
SHSEL1 C8 F05
SHSEL2 C8 F05
SHSEQM C8 F05
SHCLK B8 F05
SHDATA B8 F05
SHEN B8 F05
DVMHB B1 F02
DVMLB B1 F02
DVM5 C7 F02
DVM4 C7 F02
DVM3 C7 F02
DVM2 C5 F02
DVM1 C5 F02
DVM0 C5 F02
DVMRUN B1 F02
DVMRDY C4 F02
RAMB
Q12 VN10KM
C29 .1
U11 HM6264LP-15
OE WE CS1 CS2
I/O1 I/O2 I/O3 I/O4 I/O5 I/O6 I/O7 I/O8
AD0 AD1 AD2 AD3 AD4 AD5 AD6 AD7
U12 * 6
ROMB
CE OE/VPP
O0 O1 O2 O3 O4 O5 O6 O7
U35 GL20V8
I1/CLK I2 I3 I4 I5 I6 I7 I8 I9 I10 I11 I12 I13 I14/OE
Q1 Q2 Q3 Q4 Q5 Q6 Q7 Q8
AS ROMA RAMA
ROMB RAMB A15B
C149 .1

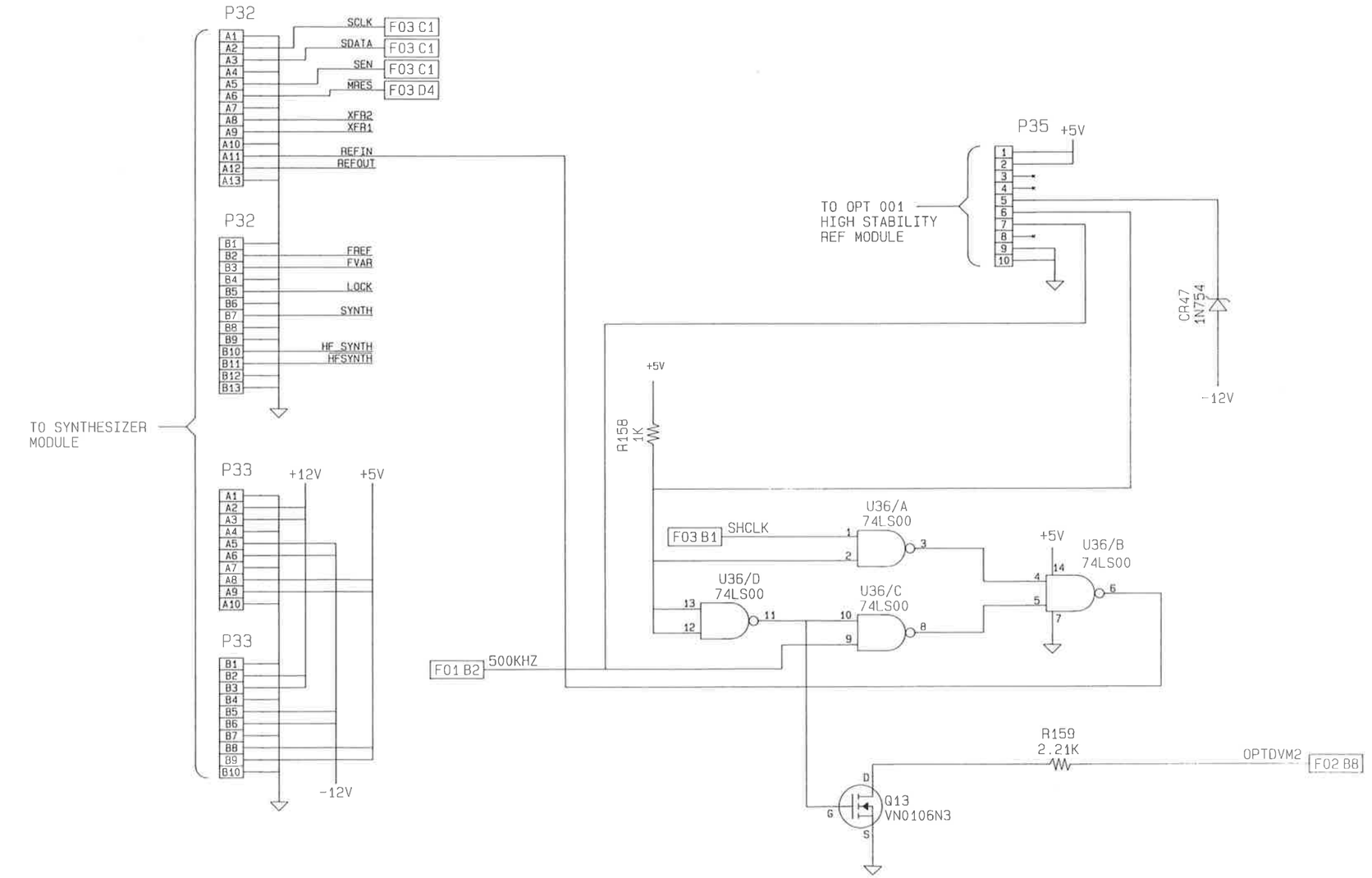
* PART IN SOCKET

NOTE: UNLESS OTHERWISE SPECIFIED

CAD JOB #: B076B

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN A. Talmadge-Lee	DATE 12/90	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	CHECKED	6/91	TITLE: SCHEMATIC, MOTHER BOARD
	PROJ. ENGR.	6/20/91	
	RELEASE APPROV.		
FINISH WAVETEK PROCESS	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES .XX .XXX		SIZE D · FSCM NO. 23338 · DWG. NO. 1104-00-3440 · REV B
DO NOT SCALE DRAWING			SCALE NONE · MODEL 91 · SHEET 3 OF 11

REV	ECO	BY	DATE	APP



NOTE UNLESS OTHERWISE SPECIFIED

CAD JOB #: B076B

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN A.Talmadge-Lee	DATE 12/90	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	CHECKED JWL	6/91	TITLE: SCHEMATIC, MOTHER BOARD
	PROJ. ENGR.		
	RELEASE APPROV.		
FINISH WAVETEK PROCESS	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES .XX ±, .XXX ±, °		SIZE D · FSCM NO. 23338 · DWG. NO. 1104-00-3440 · REV B
DO NOT SCALE DRAWING			SCALE NONE · MODEL 31 · SHEET 1 OF 10

1104-00-3440 R

REV	ECO	BY	DATE	APP

U19 CD4051B
U18 PCM56P
U20B
U21B
U22B
U23A MC34082P
U20A 4 MC34082P
U22A MC34082P
U21A MC34082P
U24B
U24A MC34082P
U23B
Q3 2N2219A
Q2 2N2905A
CR7 1N5282
CR8 1N5282
R28 1k
R29 3.65K
R30 1k
R31 4.99K
R32 4.99K
R33 15
R34 15
R35 3.32K
R36 10K
R37 3.32K
R156 TRIM
R157 TRIM
C46 .1
C47 .1
C48 .1
C49 .1
C50 .1
C51 .47
C52 .47
C53 .1
C54 .47
C55 .1
C56 .1
C57 .1
C58 .1
C59 .1
C60 .1
C61 .1
C62 .1
+5V
-5V_ISO
+12V
-12V
SHSEQM F03 C1
SHSEL0 F03 C1
SHSEL1 F03 C1
SHSEL2 F03 C1
SHCLK F03 C1
SHDATA F03 C1
SHEN F03 C1
TP7 SHDAC
TP8 GND
VAMCAL B5 F01
VSLEN C4 F01
VOFST C6 F01
TRANSIPAD
VCGZERO C4 F01
VFREQ C4 F01
VPHASE C5 F01
VSINCAL B5 F01
VTRIBAL B4 F01

NOTE UNLESS OTHERWISE SPECIFIED

CAD JOB #: B076B

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN A.Talmadge-Lee	DATE 12/90	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	CHECKED	4/91	TITLE: SCHEMATIC, MOTHER BOARD
	PROJ. ENGR.	4/24/91	
FINISH WAVETEK PROCESS	RELEASE APPROV.		
DO NOT SCALE DRAWING	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES .XX ± .XXX ± °		SIZE D · FSCM NO. 23338 · DWG. NO. 1104-00-3440 · REV B · SCALE NONE · MODEL 91 · SHEET 5 OF 11

REV	ECO	BY	DATE	APP

SECONDARY INPUT/OUTPUT NETWORK

EXT FREQ INPUT J16
R38 1K
R39 9.09K
Q4 2N3904
Q5 2N4122
R40 4.99K
R41 1.5K
R42 2K
R43 2K
C64 .1
CR9 1N5282
CR10 1N5282
CR11 1N5282
CR12 1N5282
JMP1
-12V
C65 .1
TP9 LIMXFREQ
R44 1M
C121 5.1pF
R45 200
R46 200
C73 .1
R138 15
+5V
C144 TRIM
R47 3.92K
U26 LT1016CJ
R48 100
TP10 BXFREQ
BXFREQ C4 F01
R49 681
C75 22
C76 .1
CR13 1N751A
-12V
C77 .1
TP11 GND

+12V
C66 .1
R57 10k
C67 22
C68 22
R59 1M
+12V
R58 100
U29A MC34082P
-12V
R60 1K
C70 .1
R62 1M
R63 1K
U29B
R61 576
R64 1K
C72 .1

+5V_I/O
CR14 1N5282
FB2
+5V
R67 2.21k
C81 220
C82 .1
C83 .1

J17 MOD_IN C2 F01
J18 SWPOUT B4 F01
C201 .01
SYNC_OUT J15
C202 .01
J22 PULSE SYNC
JMP10
C148 330pF
R65 15
C74 100pF
CR15 1N5282
R66 51.1 1W-0.1%
U28A 75121

+5V
C78 22
C79 .1
R160 200
SYNTH F01 D2
U27 74ALS253
R51 TBD
R52 TBD
R53 TBD
SHCLK F03 B1
PLS/SQR F01 D4
MSELA B7 F07
MSELB B7 F07
R54 200
R55 TBD
R56 78.7
SQWAVE F01 D4

+5V_I/O
U28B
C80 .1

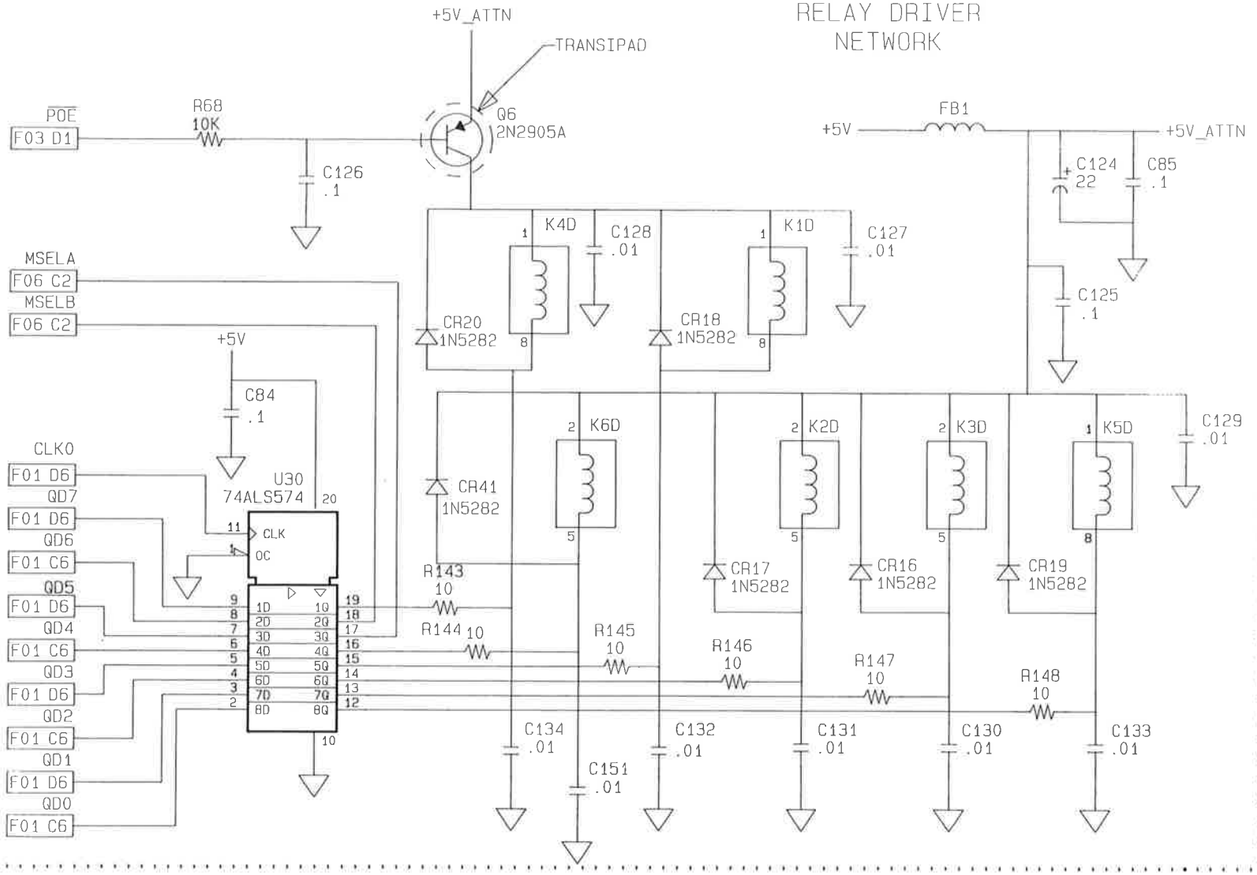
CAD JOB #: B076B

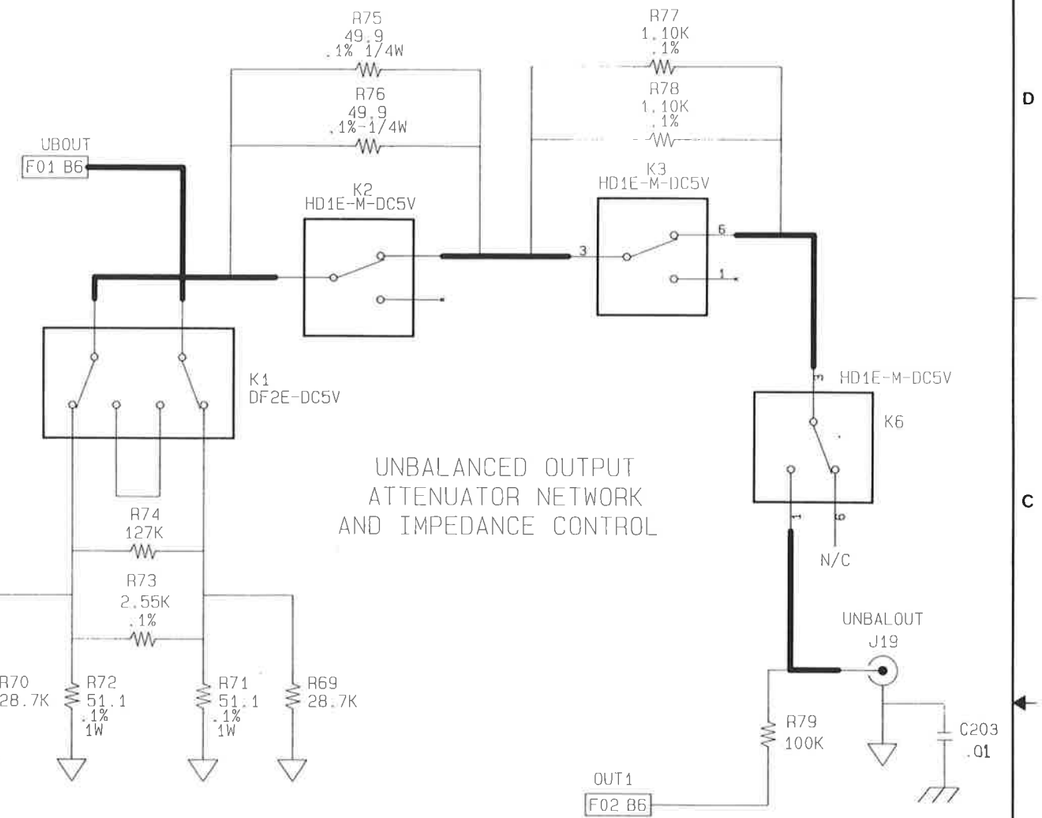
NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN A. Talmadge-Lee	DATE 12/90	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	CHECKED	6/20/91	TITLE: SCHEMATIC, MOTHER BOARD
	PROJ. ENGR.	6/20/91	
	RELEASE APPROV.		
FINISH WAVETEK PROCESS	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES .XX ± .XXX ± °		SIZE D | FSCM NO. 23338 | DWG. NO. 1104-00-3440 | REV B
DO NOT SCALE DRAWING			SCALE NONE | MODEL 91 | SHEET 6 OF 10

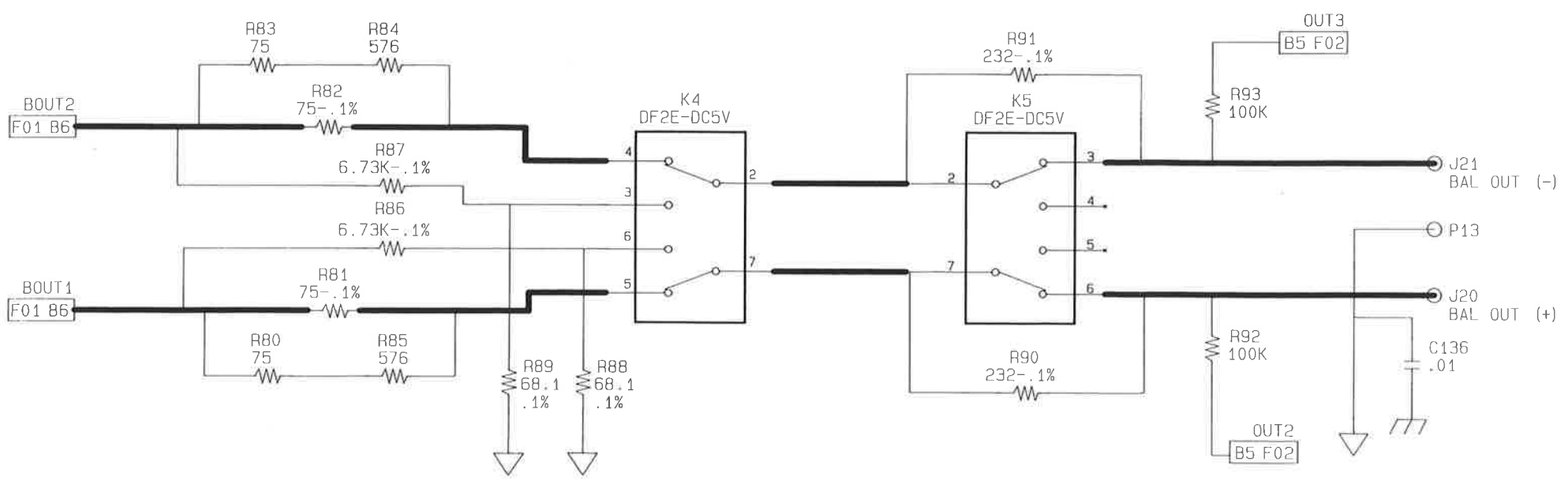
REV	ECO	BY	DATE	APP

RELAY DRIVER NETWORK





UNBALANCED OUTPUT ATTENUATOR NETWORK AND IMPEDANCE CONTROL



BALANCED OUTPUT ATTENUATOR NETWORK AND IMPEDANCE CONTROL

NOTE UNLESS OTHERWISE SPECIFIED

CAD JOB #: B0768

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN A. Talmadge-Lee	DATE 12/90	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	CHECKED JWL	4/24/91	TITLE: SCHEMATIC, MOTHER BOARD
	PROJ. ENGR.	4/24/91	
	RELEASE APPROV.		
FINISH WAVETEK PROCESS	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES .XX .XXX		SIZE D · FSCM NO. 23338 · DWG. NO. 1104-00-3440 · REV B
DO NOT SCALE DRAWING			SCALE NONE · MODEL 91 · SHEET 7 OF 10

1104-00-3440 B

REV	ECO	BY	DATE	APP

+/- 12V POWER SUPPLIES

+/- 12V UNREGULATED POWER SUPPLY INPUT

P4-3

P4-1

P4-2

CR21 MBR360

CR22 MBR360

CR23 MBR360

CR24 MBR360

CR25 1N4002

CR26 1N4002

CR27 1N4002

CR28 1N4002

C86 .01

C87 .1

+C88 4700

C89 .1

+C90 4700

VR3 LM317T (IN, OUT, ADJ)

R94 1.8-1/2W

R95 1.8-1/2W

R96 3.92K

C91 100

R98 392

R97 3.92K

C92 .1

U31A MC34082P

R99 2K .1%

R100 10K .1%

R101 7.5K .1%

VREF F02 C4 / F08 A7

U32 LT1021 (IN, OUT, GND)

+C95 2200

C96 .1

+12REF F09 D4

JMP4

+12VDC

+12PV

GND

R102 3.74K

U31B MC34082P

R103 7.5K .1%

+C97 2200

C98 .1

R108 3.92K

VR4 LM337T (ADJ, IN, OUT)

R106 3.92K

C94 100

R107 392

R105 1.8-1/2W

R104 1.8-1/2W

C155 1000

R155 25-3W

P36

TO FAN

JMP5

-12VDC

-12PV

+5V POWER SUPPLY

DASH LINES INDICATE HEATSINK AND TRANSIPAD

+5V UNREGULATED POWER SUPPLY INPUT

P23

P22

C99 .01

CR44 MBR1535CT

CR44 MBR1535CT

CR45 MBR1535CT

CR46 MBR1535CT

+C100 6800

+C101 6800

R109 40.2

Q10 TIP-36

CR29 1N4002

Q7 2N2905A

R110 165

R115 1K .1%

+C103 1000

R116 499

C104 .1

JMP6

+5V

+5PV

R111 3K-.1%

Q8 Q9 2N3904 (2)

C156 47-TANT

R112 1K .1%

C102 .1

R113 182

R114 1K .1%

VREF F08 D3

GND

NOTE UNLESS OTHERWISE SPECIFIED

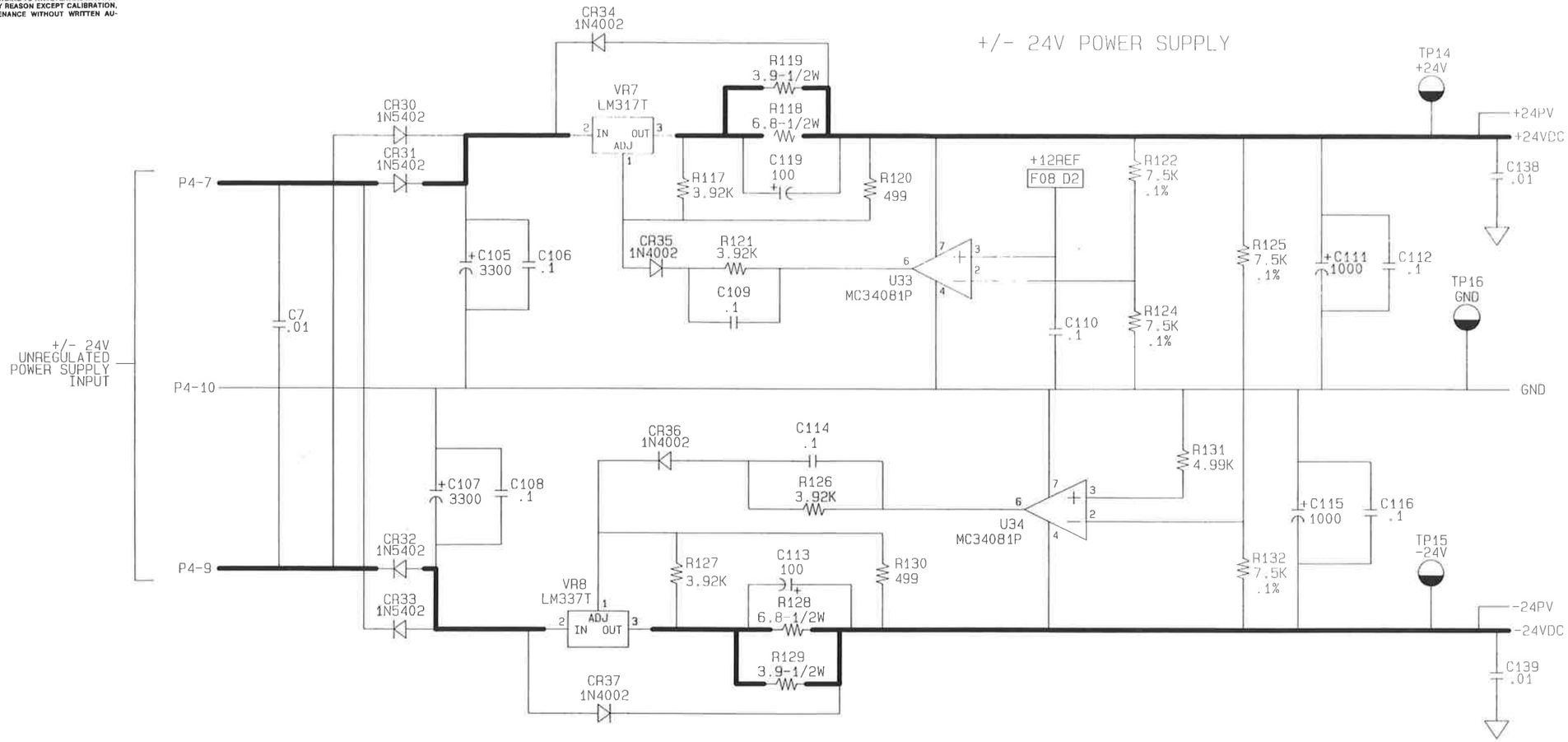
CAD JOB #: B076B

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN A.Talmadge-Lee	DATE 12/90	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	CHECKED JM	6/91	TITLE: SCHEMATIC, MOTHER BOARD
	PROJ. ENGR.	6/20/91	
	RELEASE APPROV.		
FINISH WAVETEK PROCESS	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±		SIZE D · FSCM NO. 23338 · DWG. NO. 1104-00-3440 · REV B
DO NOT SCALE DRAWING			SCALE NONE · MODEL 91 · SHEET 5 OF 10

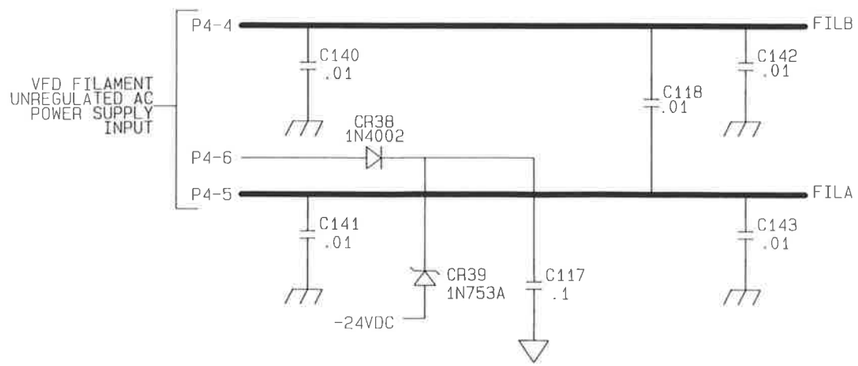
1104-00-3440 B

REV	ECO	BY	DATE	APP

+/- 24V POWER SUPPLY



VFD AC FILAMENT SUPPLY



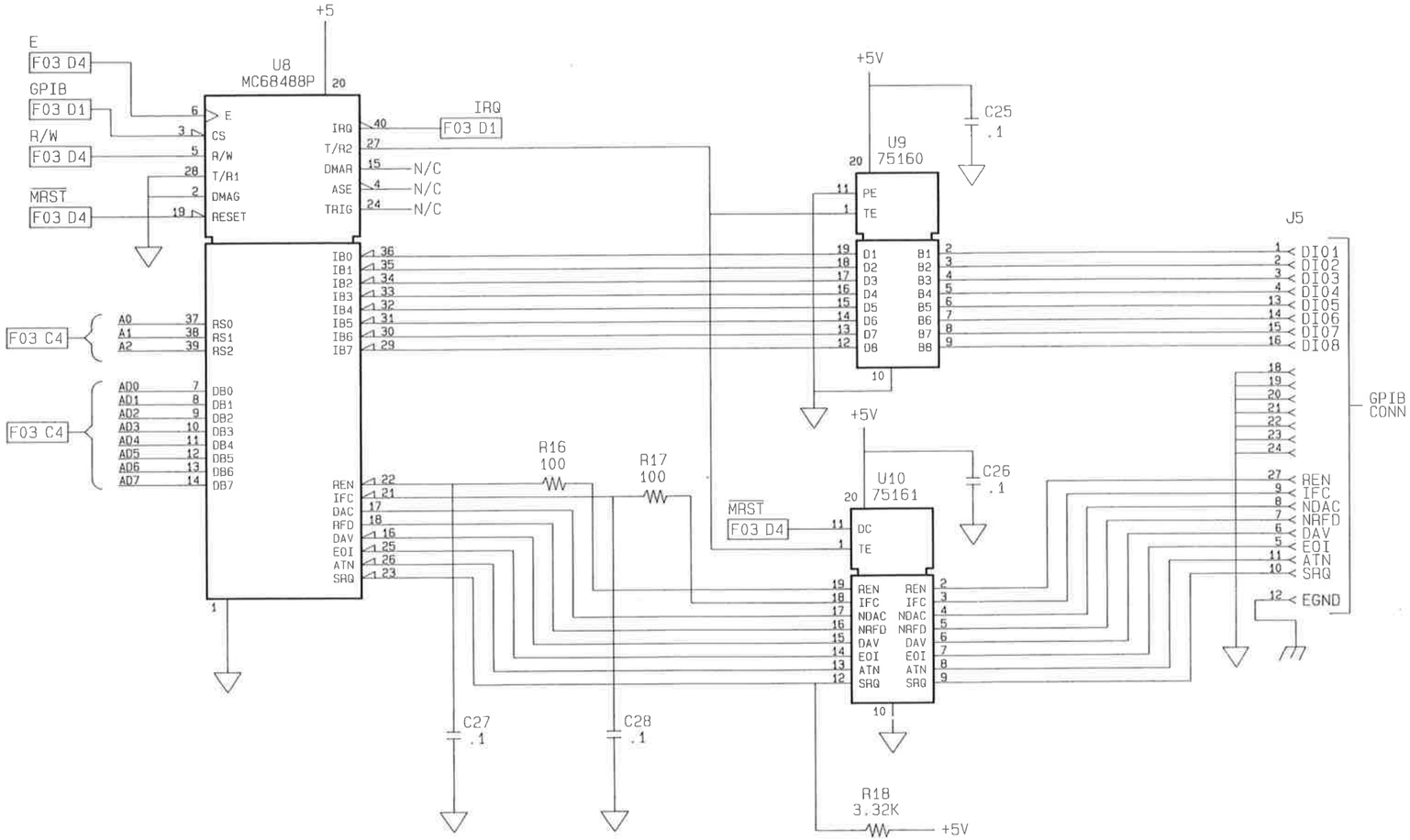
NOTE UNLESS OTHERWISE SPECIFIED

CAD JOB #: B076B

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN A.Talmadge-Lee	DATE 12/90	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	CHECKED JM	6/24/91	TITLE: SCHEMATICS, MOTHER BOARD
	PROJ. ENGR.	6/24/91	
	RELEASE APPROV.		
FINISH WAVETEK PROCESS	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES .XX ±, .XXX ±, °		SIZE D; FSCM NO. 23338; DWG. NO. 1104-00-3440; REV B
DO NOT SCALE DRAWING			SCALE NONE; MODEL 91; SHEET 9 OF 10

REV	ECO	BY	DATE	APP

GPIB SECTION



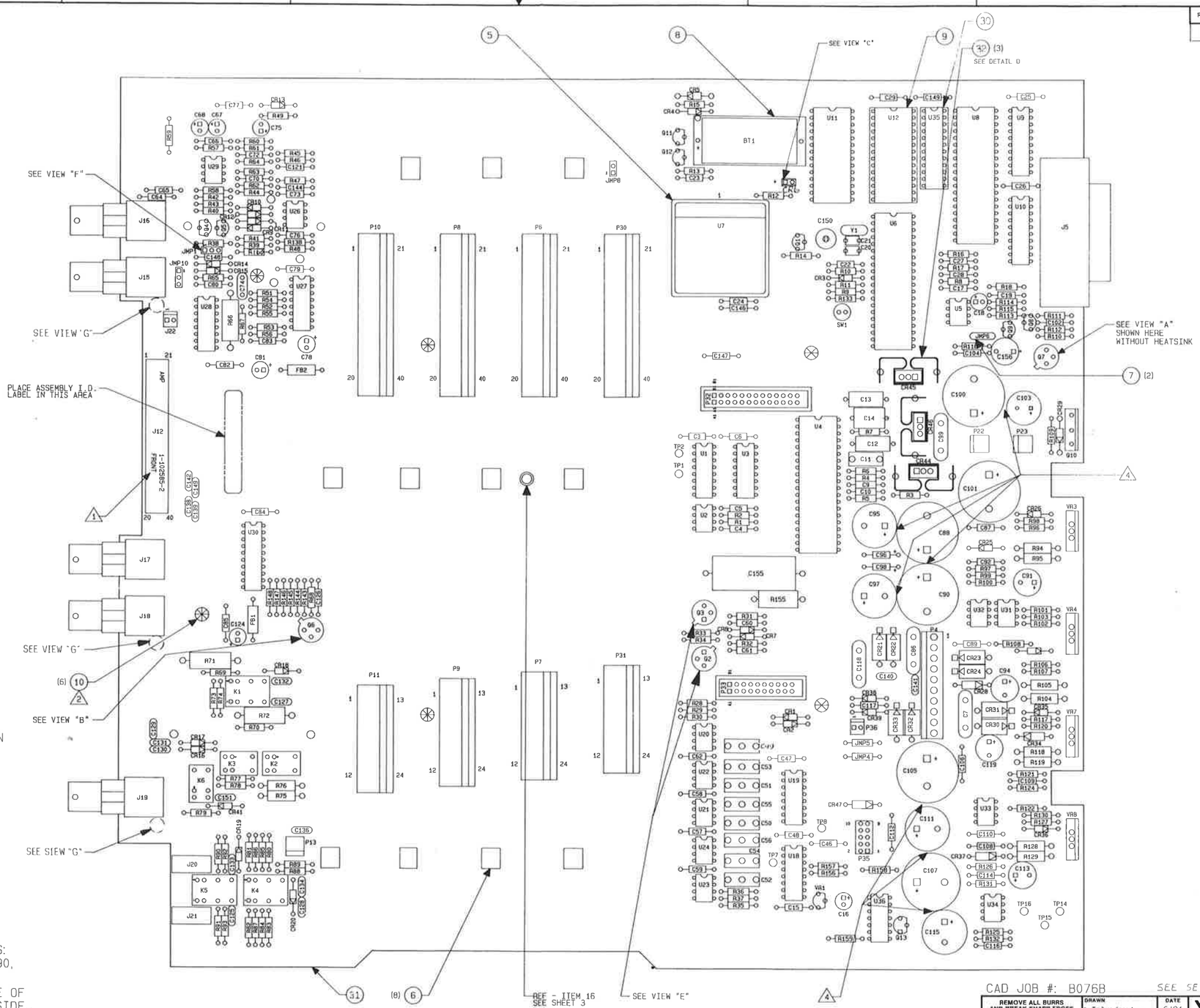
NOTE: UNLESS OTHERWISE SPECIFIED

CAD JOB #: B076B

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN A. Talmadge-Lee	DATE 12/90	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	CHECKED	6/91	TITLE: SCHEMATIC, MOTHER BOARD
	PROJ. ENGR.	6/20/91	
	RELEASE APPROV.		
FINISH WAVETEK PROCESS	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES .XX ±, .XXX ± °		SIZE D · FSCM NO. 23338 · DWG. NO. 1104-00-3440 · REV B
DO NOT SCALE DRAWING			SCALE NONE · MODEL 91 · SHEET 10 OF 10

1104-00-3440 | 3

REV	ECO	BY	DATE	APP
E	ERO 91-325	[illegible]	5/91	



11. INSTALL SHORTING JUMPER JMP1 BETWEEN PINS 1 & 2 (BIPOLAR CONFIGURATION).
10. INSTALL SHORTING JUMPER JMP7 ON PINS 1 & 2 FOR STD INSTRUMENT AND PINS 2 & 3 FOR OPTION 001.
9. ASSEMBLE PER WAVETEK WORKMANSHIP STANDARDS.
8. REFERENCE DESIGNATIONS DO NOT APPEAR ON PARTS.
7. FOR ASSEMBLY INTERCONNECTION, SEE INSTRUMENT SCHEMATIC.
6. SEE 1104-00-3440 FOR SCHEMATIC.
5. COMPONENTS UNDER ITEM NO. 18 TO BE .325 MAX FROM SURFACE OF BOARD.
4. INSTALL CLEAR RTV BETWEEN CAPACITORS: C115-C107, C107-C111, C111-C105, C97-C90, C90-C88, C88-C95, C103-C100.
3. INSTALL CANS FLUSH TO COMPONENT SIDE OF P.C. BOARD. SOLDER TABS TO CIRCUIT SIDE.
2. ITEM 10 (SPACERS) TO BE INSTALLED FROM BOTTOM SIDE OF BOARD (CIRCUIT SIDE).
1. MANUFACTURER'S MARKING INDICATES CORRECT ORIENTATION OF CONNECTOR.

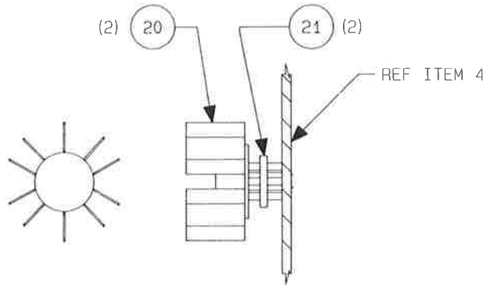
NOTE UNLESS OTHERWISE SPECIFIED

CAD JOB #: B076B

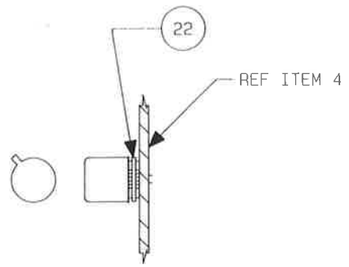
SEE SEPARATE PARTS LIST

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN A. Talmadge-Lee	DATE 6/91	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	CHECKED JM	6/20/91	TITLE: PCA, MOTHER BOARD
	PROJ. ENGR. [signature]	6/20/91	
	RELEASE APPROVAL [signature]	6/20/91	
FINISH WAVETEK PROCESS	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES XX ± XXX ± °		SIZE D · FSCM NO. 23338 · DWG. NO. 1101-00-3440 · REV B
DO NOT SCALE DRAWING			SCALE NONE · MODEL 91 · SHEET 1 OF 3

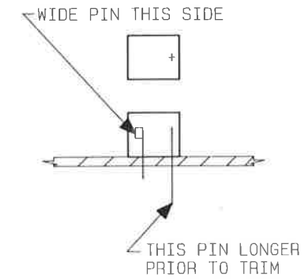
REV	ECO	BY	DATE	APP



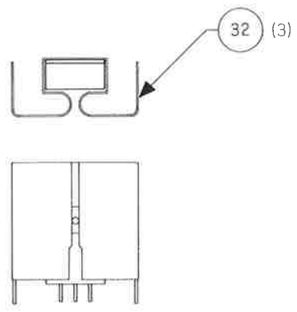
VIEW "A"
SCALE = 2/1



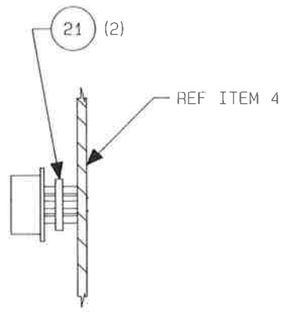
VIEW "B"
SCALE= 2/1



VIEW "C"
NOT TO SCALE



VIEW "D"
NOT TO SCALE



VIEW "E"
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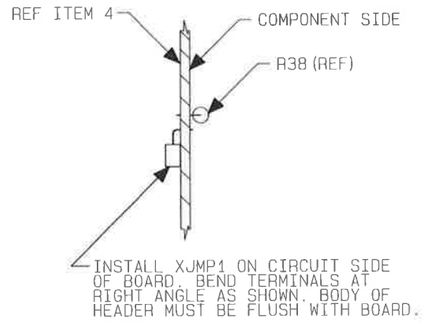
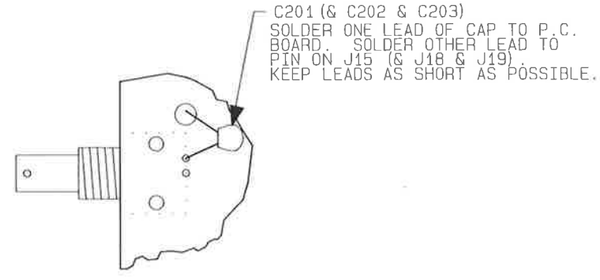


VIEW "F"
SCALE = 2/1



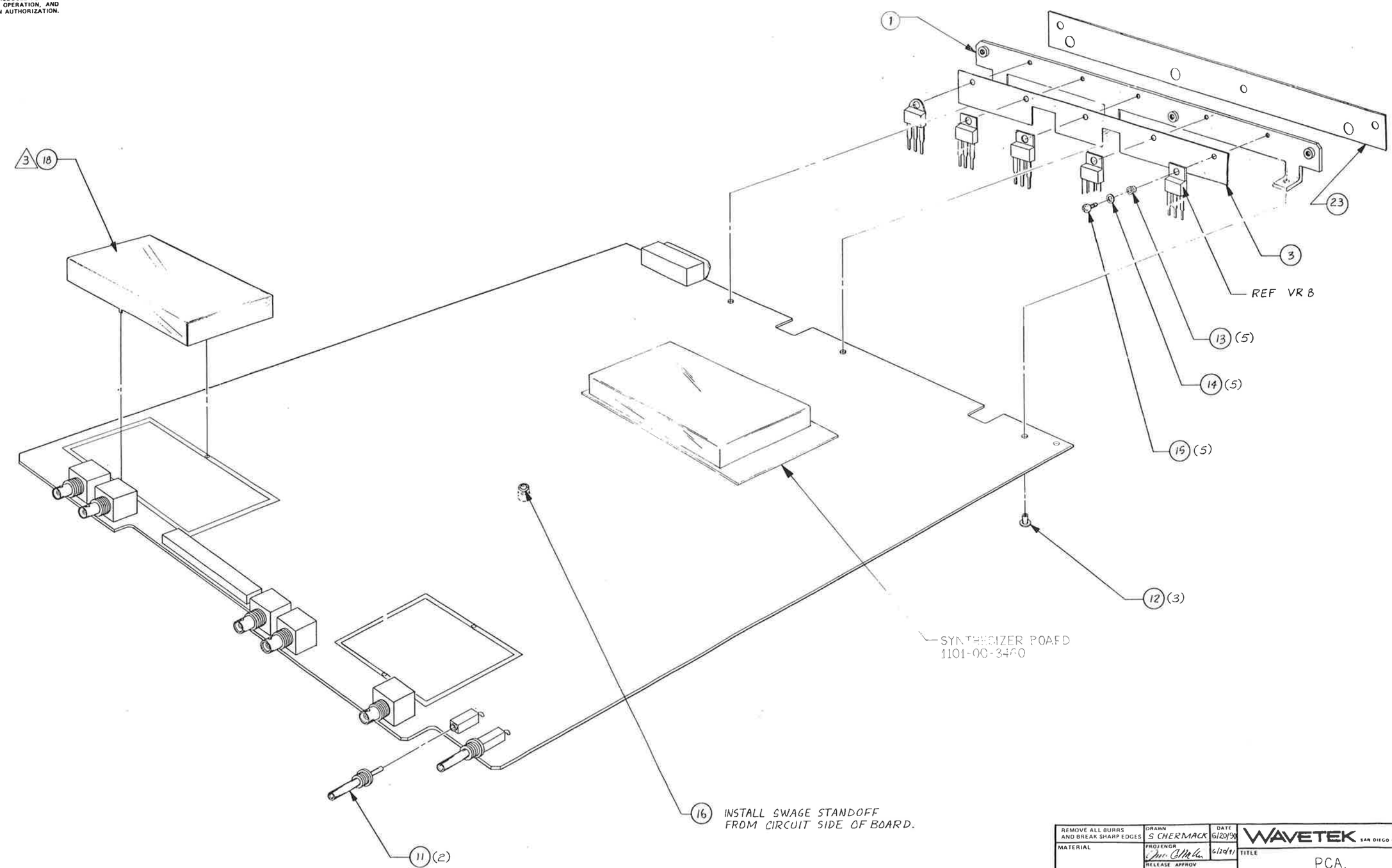
VIEW "G"
SCALE = 2/1

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN [illegible]	DATE 6/17/91	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	CHECKED SM	6/20/91	TITLE PCA, MOTHERBOARD
	PROJ. ENGR. [illegible]	6/20/91	
	RELEASE APPROV.		
FINISH WAVETEK PROCESS	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES .XX ± .XXX ± °		SIZE D · FSCM NO. 23338 · DWG. NO. 1101-00-3440 · REV B
DO NOT SCALE DRAWING			SCALE AS NOTED · MODEL 91 · SHEET 2 OF 3

8 7 6 5 4 3 2 1

REV	ECN	BY	DATE	APP
	SEE SHEET #1			



NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN S CHERMACK	DATE 6/20/90	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR	6/20/91	TITLE PCA, MOTHERBOARD
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1° XX ±.030		
	DO NOT SCALE DWG		MODEL NO. 90 SERIES
	SCALE NONE		DWG NO 1101-00-3440 REV B
			CODE IDENT 23338 SHEET 3 OF 3

8 7 6 5 4 3 2 1

REV	ECO	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	PCA, SYNTHESIZER BD-91	1100-00-3597	WVTK	1100-00-3597	1
NONE	A/D MOTHERBOARD - 91	1101-00-3440	WVTK	1101-00-3440	1
NONE	SCHEMATIC MOTHERBOARD 91	1104-00-3440	WVTK	1104-00-3440	1
NONE	91 MOTHERBOARD PREWAVE LOAD	1200-00-3440	WVTK	1200-00-3440	1
18	CAN, FREQ IN/SYNC OUT	1400-02-3453	WVTK	1400-02-3453	1
3	THERMAL GASKET-REAR PANEL-A	1400-02-4400	WVTK	1400-02-4400	1
23	THERMAL GASKET-REAR PANEL-B	1400-02-4410	WVTK	1400-02-4410	1
1	SUPPPORT PLATE, TRANSISTOR	1400-02-5007	WVTK	1400-02-5007	1
C201 C202 C203	CAP CER MON .01MF 50V Z5U +80/-20% RAD LD .2	1C20Z5U103M050B	SPRAG	1500-01-0311	3
J15 J16 J17 J18 J19	CONN, BNC(PC)	227161-1	AMP	2100-01-0019	5
XJMP1	CONN, HEADER, 3 PIN	929834-01-03	APTRN	2100-02-0196	1
JMP1 JMP10	JUMPER, FEMALE, 2 POSITION, 0.1 SPACE	929950-00	APTRN	2100-02-0213	2

WAVETEK PARTS LIST | TITLE: MOTHERBOARD ASSY-91 | ASSEMBLY NO. 1100-00-3440 | REV F

PAGE 1

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
11	CONN PIN, INSERT	2100-05-0061	WVTK	2100-05-0061	2
16	STANDOFF, SW, 6-32X5/32, 1/16 SW, BR, ZN PL	3045-B-632-B MODL=5/32	RAF	2800-06-0062	1
20	HEAT SINK	207	WAKE	2800-11-0001	1
13	WASHER	5607-150	SESTM	2800-11-0015	5
12	RIVET, 1/8 BODY DIA, 1/8-3/16 GRIP SS	SSD43SSBS	EMHRT	2800-12-0055	3
10	HOLE PLUG, BINDER HEAD, NTRAL NYLON	207-120241-03-0101	FASTX	2800-35-0009	6
14	WASHER, LOCK REG, S/S #4	MS 35338-135	CMRCL	2800-45-4000	5
15	SCREW PLPS PAN M/S 18-8 S/S 4-40X1/4	MS 51957-13	CMRCL	2800-48-4104	5
JMP6	JUMPER	461-2871-01-03-10	CAMBN	3000-00-0034	1
BT1	BATTERY, 3V LITHIUM	BR-2/3A	PANAS	4000-02-0008	1
Q10	TRANS	TIP-36	TI	4902-00-0360	1
VR3 VR7	VOLT REGULATOR, 3 TERMINAL ADJUSTABLE POS	LM317T	NSC	7000-03-1700	2
VR4 VR8	VOLT REGULATOR	LM337T	NSC	7000-03-3700	2

WAVETEK PARTS LIST | TITLE: MOTHERBOARD ASSY-91 | ASSEMBLY NO. 1100-00-3440 | REV F

PAGE 2

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
U35	PROG, GAL, USES 8000-20-8015 FOR MOD 91, REF U35, V2.0	8600-00-0679	WVTK	8600-00-0679	1
U12	PROG, EPROM, USES 8002-75-1200 FOR MOD 91, REF U12, V1.1	8600-00-0719	WVTK	8600-00-0719	1

WAVETEK PARTS LIST | TITLE: MOTHERBOARD ASSY-91 | ASSEMBLY NO. 1100-00-3440 | REV F

PAGE 3

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	CHECKED		TITLE: MOTHERBOARD ASSY
	PROJ. ENGR.		
	RELEASE APPROV.		
FINISH WAVETEK PROCESS	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES ± .XX ± .XXX ± ±		SIZE D | FSCM NO. 23338 | DWG. NO. 1100-00-3440 | REV F
DO NOT SCALE DRAWING			SCALE | MODEL 91 | SHEET 1 OF 1

REV	ECO	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R155	RES, WW, 3W, 5%, 25 OHM	23J25R	OHMIT	0610-00113	1
VR1	Q: N.V. REG 5V (79L05)	LM320LZ-5.0	NSC	120.0054	1
CR39	SL ZR 6.2V 5% 400MW (1N753A)	1N753A	ROHM	131.9620	1
C74	CAP CER MON 100PF 50V COG 5% RAD LD SP .2	5028E050RD101J	KYCRA	1500-01-0103	1
C118 C7 C86 C99	CAP, CER, .01MF, 1KV	QAP-103	CRL	1500-01-0309	4
C146 C147	CAP CER MON .01MF 50V, AXIAL	CAC02Z5U103Z100A	CORNQ	1500-01-0310	2
C127 C128 C129 C130 C131 C132 C133 C134 C136 C138 C139 C140 C141 C142 C143 C151	CAP CER MON .01MF 50V Z5U +80/-20% RAD LD .2	1C20Z5U103M050B	SPRAQ	1500-01-0311	16
C102 C104 C106 C108 C109 C110 C112 C114 C116 C117 C126 C149 C15 C17 C19 C22 C23 C24 C25 C26 C27 C28 C29 C3 C4 C46 C47 C48 C5 C57 C58 C59 C6 C60 C61 C62 C64 C65 C66 C70 C72 C73 C76 C77 C79 C80 C82 C83 C84 C85 C87 C89 C9 C92 C96 C98	CAP, CER, MON, .1MF, 50V, AXIAL	CAC03Z5U104Z050A	CORNQ	1500-01-0405	56
C20	CAP CER MON 15PF 50V COG 5% RADIAL LD BP	5028E050RD150J	KYCRA	1500-01-5003	1

WAVETEK PARTS LIST — TITLE: 91 MOTHERBOARD PREWAVE LOAD — ASSEMBLY NO. 1200-00-3440 — REV B — PAGE 1

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
.2					
C10	CAP, CER, 220PF, 100V, AXIAL	CAC02CD0221J100A	CORNQ	1500-02-2106	1
C148	CAP, CER, 330PF, 100V, AXIAL	CAC02CD0331J100A	CORNQ	1500-03-3106	1
C121	CAP, CER, 5.1PF, 200V, AXIAL	SA102A5R1DAA	AVX	1500-05-1906	1
C21	CAP, CERAMIC, 68PF, 100V, 5%, RAD LEAD .2	SR211A680JAA	AVX	1500-06-8016	1
C113 C119 C91 C94	CAP, ELECT, 100MF, 35V RADIAL LEAD, SP .20	NRE101M35V10X12.5	NIC	1500-31-0102	4
C111 C115	CAP, ELECT, 1000MF/50V RADIAL LEAD, SP .30	NRE102M50V16X25	NIC	1500-31-0203	2
C103	CAP, ELECT, 1000MF/16V RADIAL LEAD, SP .20	NRE102M16V10X20	NIC	1500-31-0211	1
C155	CAP, ELECT, 1000MF, 35V	39D108G035GL6	SPRAQ	1500-31-0212	1
C81	CAP, ELECT, 220MF/10V	ECEA1AU221	PANAS	1500-32-2001	1
C124 C16 C18 C67 C68 C75 C78	CAP, ELECT, 22MF, 25V, RADIAL	SRA25VB22RM6X7LL	UNCON	1500-32-2002	7
C95 C97	CAP, ELECT, 2200MF, 16V RADIAL LEAD, SP .30	ECEA1CV2228C	PANAS	1500-32-2201	2

WAVETEK PARTS LIST — TITLE: 91 MOTHERBOARD PREWAVE LOAD — ASSEMBLY NO. 1200-00-3440 — REV B — PAGE 2

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
C105 C107	CAP, ELECT, 3300MF, 50V RADIAL LEAD, SP .40	NRE 3300/50	NIC	1500-33-3202	2
C88 C90	CAP, ELECT, 4700MF/25V RADIAL LEAD, SP .50	NRSA472M25V18X36	NIC	1500-34-7202	2
C100 C101	CAP ELECT 16V RADIAL LS .40	NRE682M16V22X41	NIC	1500-36-8201	2
C14	CAP, POLYC, .01MF, 100V, AXIAL	C318103F	BISHO	1500-41-0304	1
C11 C49 C50 C53 C55 C56	C05 CAP, MET POLY, .1MF, 100V/160V DC, .4 LS	171104J160D	MALRY	1500-41-0434	6
C13	CAP, MYLAR, 1MF, 100V, RADIAL	PMT2R1.0K100	ITT	1500-41-0524	1
C51 C52 C54	CAP, MET-POLY, 5%, 47MF, 63V RADIAL LEAD SP .2	168474J63F	MALRY	1500-44-7413	3
C12	CAP, POLYPRO, .056MF, 200V, 2%, AXIAL	QA1C563-Q	IMB	1500-45-6300	1
C150	CAP, VAR, 7-35PF 250V	7S-TRIKO-02 7/35PF(OBS	TRIKO	1500-53-5000	1
C156	CAP, TANT, 47MF, 20V	196D476X9020PE4(OBS)	SPRAQ	1500-74-7601	1
31	MOTHER BD 91 REF: SPEC 0008-00-0455 REV C	1700-00-3440	WVTK	1700-00-3440	1

WAVETEK PARTS LIST — TITLE: 91 MOTHERBOARD PREWAVE LOAD — ASSEMBLY NO. 1200-00-3440 — REV B — PAGE 3

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
P4	CONN, HEADER	1-640386-0	AMP	2100-02-0079	1
J20 J21	PC JACK	09-9094-1-04	CONCD	2100-02-0190	2
XJMP10	CONN, HEADER, 3 PIN	929834-01-03	APTRN	2100-02-0196	1
XJMP8	CONN, HEADER, 2 PIN, 0.1 SPACE	929834-01-02	APTRN	2100-02-0208	1
J12	CONN, HEADER, 40 PIN, RECPT, 2X20, .1 CTR PCMT	1-102585-2	AMP	2100-02-0256	1
P11 P31 P7 P9	CONN, HEADER, 24 PIN, PCMT, .1 CTR, 2X12, SHRD	102692-2	AMP	2100-02-0257	4
P10 P30 P6 P8	CONN, HEADER, 40 PIN, PCB MT, .1 CTR, 2X20, SHRD	1-102692-3	AMP	2100-02-0258	4
J5	CONN, RECP, GPIB, 24POS, .125 TAIL, RT ANG, PC MT	488-2R4-24BM32K9	BURND	2100-02-0259	1
J22 P36	HEADER 2 PIN, .025 CENTER, FRICTION LOCK	641126-2	AMP	2100-02-0284	2
P35	HEADER, 10PIN, VERTICAL RETAIN/EJECTOR LATCH	501-1027ES	TH&BE	2100-02-0292	1
P32	CONN, STRIP, 26 PIN, .7" BOARD SPACE	ZSS-113-02-L-D-615	SAM	2100-02-0296	1

WAVETEK PARTS LIST — TITLE: 91 MOTHERBOARD PREWAVE LOAD — ASSEMBLY NO. 1200-00-3440 — REV B — PAGE 4

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
P33	CONN, STRIP, 20 PIN, .7" BOARD SPACEING	ZSS-110-02-L-D-615	SAM	2100-02-0297	1
9	SOCKET, IC, 28 PIN	DILB28P-108T	BURND	2100-03-0081	1
30	SOCKET, DUAL BEAM, LO RISE, 24 PIN	802-0241642	WELCN	2100-03-0088	1
5	SOCKET, 84 PIN, PLCC, THRU HOLE	821573-1	AMP	2100-03-0094	1
7	SOCKET, CLSD ENTRY, .040 PINS	450-3752-01-06-00	CAMB	2100-03-0096	2
P13 P22 P23	TERMINAL TAB (FASTON)	62747-1	AMP	2100-04-0038	3
TP11 TP16 TP2 TP8	TEST POINT, BLK, PC	TP-104-01-00	COMPO	2100-04-0054	4
TP1 TP10 TP14 TP15 TP7 TP9	TEST POINT, RED, PC	TP-104-01-02	COMPO	2100-04-0055	6
Y1	CRYSTAL, 4MHZ	180-502	MTRON	2300-99-0004	1
6	FUSE HOLDER, CLIP	102071	LITFU	2400-05-0031	11
22	TRANSIPAD	10123N(OBS)	METRS	2800-11-0003	1
21	TRANSIPAD	531-218	BIVAR	2800-11-0004	3
32	HEATSINK, TO-220, CLIP-ON	5749028033	AAVID	2800-11-0040	3
8	BATTERY HOLDER	BH 2/3A	MPD	3000-00-0137	1

WAVETEK PARTS LIST — TITLE: 91 MOTHERBOARD PREWAVE LOAD — ASSEMBLY NO. 1200-00-3440 — REV B — PAGE 5

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
FB1 FB2	BALUN CORE, FERRITE, 680 OHMS	2943666671	FARIT	3100-00-0017	2
K1 K4 K5	RELAY, 2 FORMC, 5V, DIP 14	DF2E-DC5V	AROMT	4500-00-0033	3
K2 K3 K6	RELAY, 1 FORMC, 5V, .312H, .296W	HD1E-M-DC5V	AROMT	4500-00-0034	3
R104 R105 R94 R95	RES, C, 1/2W, 5%, 1.8	RC-1/2-1R8J	STKPL	4700-25-0189	4
R119 R129	RES, C, 1/2W, 5%, 3.9	RC-1/2-3R9J	STKPL	4700-25-0399	2
R118 R128	RES, C, 1/2W, 5%, 6.8	RC-1/2-6R8J	STKPL	4700-25-0689	2
R112 R114 R115	RES, MF, 1/8W, .1%, 1K	RN55E-1001B	MEPCO	4701-02-1001	3
R100	RES, MF, 1/8W, .1%, 10K	RN55E-1002B	MEPCO	4701-02-1002	1
R77 R78	RES, MFLM, 1/8W, .1%, 1.1K	5033RE1101B	MEPCO	4701-02-1101	2
R2	RES, MF, 1/8W, .1%, 1.5K	RN55E-1501B	CORNQ	4701-02-1501	1
R99	RES, MF, 1/8W, .1%, 2K	RN55E-2001B	MEPCO	4701-02-2001	1
R90 R91	RES, MFLM, 1/8W, .1%, 232	5033RE2320B	MEPCO	4701-02-2320	2
R73	RES, MFLM, 1/8W, .1%, 2.55K	5033RE2551B	MEPCO	4701-02-2551	1
R1 R111 R3	RES, MF, 1/8W, .1%, 3K	RN55E-3001B	MEPCO	4701-02-3001	3

WAVETEK PARTS LIST — TITLE: 91 MOTHERBOARD PREWAVE LOAD — ASSEMBLY NO. 1200-00-3440 — REV B — PAGE 6

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	CHECKED		TITLE: 91 MOTHERBOARD PREWAVE LOAD
	PROJ. ENGR.		
FINISH WAVETEK PROCESS	RELEASE APPROV.		
DO NOT SCALE DRAWING	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES ± .XX ± .XXX ± ±		SIZE D · FSCM NO. 23338 · DWG. NO. 1200-00-3440 · REV B · SCALE · MODEL 91 · SHEET 1 OF 2

REV	ECO	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R86 R87	RES, MFLM, 1/8W, .1%, 6.73K	5033RE6731B	MEPCO	4701-02-6731	2
R88 R89	RES, MFLM, 1/8W, .1%, 68.1	CMF-556R1BT-9	DALE	4701-02-6819	2
R4	RES, MF, 1/8W, .1%, 750	RN55E-7500B	MEPCO	4701-02-7500	1
R101 R103 R122 R124 R125 R132	RES, MF, 1/8W, .1%, 7.5K	RN55E-7501B	MEPCO	4701-02-7501	6
R81 R82	RES, MFLM, 1/8W, .1%, 75	5033RE7509B	MEPCO	4701-02-7509	2
R16 R17 R48 R58	RES, MF, 1/8W, 1%, 100	RN55D-1000F	TRW	4701-03-1000	4
R138 R28 R30 R38 R60 R63 R64	RES, MF, 1/8W, 1%, 1K	RN55D-1001F	TRW	4701-03-1001	7
R10 R11 R133 R36 R5 R57 R68 R8 R9	RES, MF, 1/8W, 1%, 10K	RN55D-1002F	TRW	4701-03-1002	9
R7 R79 R92 R93	RES, MF, 1/8W, 1%, 100K	RN55D-1003F	TRW	4701-03-1003	4
R44 R59 R62	RES, MF, 1/8W, 1%, 1M	RN55D-1004F	TRW	4701-03-1004	3
R143 R144 R145 R146 R147 R148	RES, MF, 1/8W, 1%, 10	5043ED10R100F	MEPCO	4701-03-1009	6
R74	RES, MFLM, 1/8W, 1%, 127K	5033RD1273F	MEPCO	4701-03-1273	1
R41	RES, MF, 1/8W, 1%, 1.5K	RN55D-1501F	TRW	4701-03-1501	1

WAVETEK PARTS LIST | TITLE: 91 MOTHERBOARD PREWAVE LOAD | ASSEMBLY NO. 1200-00-3440 | REV B

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R139 R33 R34 R65	RES, MF, 1/8W, 1%, 15	RN55D-15R0F	TRW	4701-03-1509	4
R110	RES, MF, 1/8W, 1%, 165	RN55D-1650F	TRW	4701-03-1650	1
R113	RES, MF, 1/8W, 1%, 182	RN55D-1820F	TRW	4701-03-1820	1
R45 R46 R54	RES, MF, 1/8W, 1%, 200	RN55D-2000F	TRW	4701-03-2000	3
R42 R43	RES, MF, 1/8W, 1%, 2K	RN55D-2001F	TRW	4701-03-2001	2
R6	RES, MF, 1/8W, 1%, 200K	RN55D-2003F	MEPCO	4701-03-2003	1
R15 R159 R67	RES, MF, 1/8W, 1%, 2.21K	RN55D-2211F	TRW	4701-03-2211	3
R13	RES, MF, 1/8W, 1%, 274	RN55D-2740F	TRW	4701-03-2740	1
R69 R70	RES, MF, 1/8W, 1%, 28.7K	RN55D-2872F	TRW	4701-03-2872	2
R18 R35 R37	RES, MF, 1/8W, 1%, 3.32K	RN55D-3321F	TRW	4701-03-3321	3
R29	RES, MF, 1/8W, 1%, 3.65K	RN55D-3651F	TRW	4701-03-3651	1
R102	RES, MF, 1/8W, 1%, 3.74K	RN55D-3741F	TRW	4701-03-3741	1
R107 R98	RES, MF, 1/8W, 1%, 392	RN55D-3920F	TRW	4701-03-3920	2
R106 R108 R117 R121 R126 R127 R47 R96 R97	RES, MF, 1/8W, 1%, 3.92K	RN55D-3921F	TRW	4701-03-3921	9
R109	RES, MF, 1/8W, 1%, 40.2	RN55D-40R2F	TRW	4701-03-4029	1
R116 R120 R130	RES, MF, 1/8, 1%, 499	RN55D-4990F	TRW	4701-03-4990	3

WAVETEK PARTS LIST | TITLE: 91 MOTHERBOARD PREWAVE LOAD | ASSEMBLY NO. 1200-00-3440 | REV B

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R131 R31 R32 R40	RES, MF, 1/8W, 1%, 4.99K	RN55D-4991F	TRW	4701-03-4991	4
R12 R14	RES, MF, 1/8W, 1%, 49.9K	RN55D-4992F	TRW	4701-03-4992	2
R61 R84 R85	RES, MF, 1/8W, 1%, 576	RN55D-5760F	TRW	4701-03-5760	3
R49	RES, MF, 1/8W, 1%, 681	RN55D-6810F	TRW	4701-03-6810	1
R80 R83	RES, MFLM, 1/8W, 1%, 75	5033RD75R0F	MEPCO	4701-03-7509	2
R56	RES, MF, 1/8W, 1%, 78.7	RN55D-78R7F	TRW	4701-03-7879	1
R39	RES, MF, 1/8W, 1%, 9.09K	RN55D-9091F	TRW	4701-03-9091	1
R75 R76	RES, MFLM, 1/4W, .1%, 49.9	5043RE49R9B	MEPCO	4701-12-4999	2
R66 R71 R72	RES, MFLM, 1W, .1%, 51.1	5053RE51R1B(OBS)	MEPCO	4701-32-5119	3
JMP4 JMP5	RES, 0 OHM JUMPER	JP02T68Q	ROHM	4799-00-0087	2
CR13	DIODE, ZENOR, 5.1V, 500MW, GIB, IN751A	1N751A	FAIR	4801-01-0751	1
CR47	DIODE, ZENER, 6.8V	1N754A	MOT	4801-01-0754	1
CR1 CR10 CR11 CR12 CR14 CR15 CR16 CR17 CR18 CR19 CR2 CR20 CR41 CR7 CR8 CR9	DIODE, HIGH CONDUCTANCE, ULTRA FAST	1N5282	FAIR	4801-01-5282	16
CR25 CR26 CR27 CR28 CR29 CR34 CR35 CR36 CR37 CR38	DIODE, 1N4002 GEN PURPOSE RECT. 100V, 1A	1N4002	FAIR	4801-02-0001	10

WAVETEK PARTS LIST | TITLE: 91 MOTHERBOARD PREWAVE LOAD | ASSEMBLY NO. 1200-00-3440 | REV B

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
CR21 CR22 CR23 CR24	RECT, SCHTKY BARRIER, 3A, 60V	MBR360	MOT	4806-00-3600	4
CR44 CR45 CR46	RECT, SCHOT BARRIER, CNTR-TAP, 15A, 35V	MBR1535CT	MOT	4806-01-5350	3
CR30 CR31 CR32 CR33	DIODE, 3A, 200V	1N5402	MOT	4806-01-5402	4
CR5	DIODE, RECT, SCH BARRIER	MBR120P	MOT	4806-02-0120	1
CR3 CR4	DIODE 5082-2811 SCHOTTKY, 15V, 20MA	5082-2811	HP	4809-02-2811	2
CR6	LED, GREEN, RECT BAR	LTL-3231A	LITE	4899-00-0057	1
Q3	TRANS 2N2219A NPN GENERAL PURPOSE TO-5	2N2219A	NSC	4901-02-2191	1
Q2 Q6 Q7	TRANS 2N2905A PNP GENERAL PURPOSE TO-5	2N2905A	NSC	4901-02-9051	3
Q1 Q4 Q8 Q9	TRANS 2N3904 NPN GENERAL PURPOSE TO-92	2N3904	FAIR	4901-03-9040	4
Q5	TRANS, GENERAL PURPOSE, PNP, TO-92	PN4122	NSC	4901-04-1220	1
Q11 Q12 Q13	TRANS	VN10KM	SILCON	4902-00-0100	3
SW1	SWITCH, MIN PUSHBUTTON, SPST BLK	39-405	GRAHL	5102-00-0015	1

WAVETEK PARTS LIST | TITLE: 91 MOTHERBOARD PREWAVE LOAD | ASSEMBLY NO. 1200-00-3440 | REV B

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
U18	DAC, SERIAL INP, 16 BIT, MONO	PCM56P	BURR	7000-00-5600	1
U1 U3	MUX, CMOS, D 4C, 8 CHAN/DUAL 4 CHAN ANAL	DG508ACJ	SILCON	7000-05-0800	2
U26	COMPARATOR, ULTRA FAST, 10NS	LT1016CN8	LINTE	7000-10-1600	1
U32	VOLTAGE REFERENCE, 10V, 8 PIN DIP	LT1021CCN8-10	LINTE	7000-10-2101	1
U4	ADC, 12 BIT	ICL7109CPL	INTSIL	7000-71-0900	1
U5	RESET GEN	TL7705ACP	TI	7000-77-0501	1
U2 U33 U34	OP AMP, HI SLEW RTE, WIDEBND, JFET, STD	MC34081P	MOT	7003-40-8100	3
U20 U21 U22 U23 U24 U29 U31	OP AMP, HI SLEW RTE, WIDEBND, JFET DUAL	MC34082P	MOT	7003-40-8200	7
U28	DRIVER, DUAL LINE	SN75121N	TI	7007-51-2100	1
U19	MUX/DEMUX, ANALOG	CD4051BE	RCA	8000-40-5100	1
U11	SRAM, 8KX8, 120NS, CMOS	CXK5864BP-12L	SONY	8000-62-6400	1
U6	MICROPROCESSOR, 8BIT	EF6803P	SGS	8000-68-0300	1
U36	GATE, NAND, QUAD 2-INP, TTL	SN74LS00N	TI	8000-74-0010	1

WAVETEK PARTS LIST | TITLE: 91 MOTHERBOARD PREWAVE LOAD | ASSEMBLY NO. 1200-00-3440 | REV B

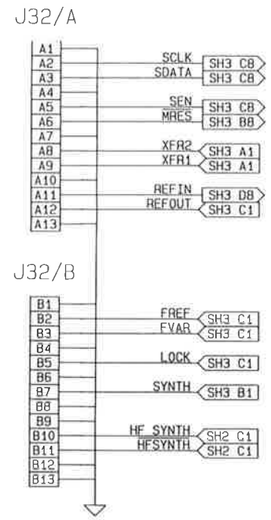
REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
U8	ADPT, GPIB INTERFACE	MC68488P	MOT	8006-84-8800	1
U27	MUX/SEL, DUAL 1 OF 4 DATA, 3/STATE	SN74ALS253N	TI	8007-42-5300	1
U30	FLIP-FLOP, OCTAL D	SN74ALS574N	TI	8007-45-7450	1
U9	XCVR, OSC BUS, TTL	75160	TI	8007-51-6000	1
U10	TRANSCEIVER, OCT BUS, TTL	SN75161BN	TI	8007-51-6100	1
U7	GATE ARRAY, 84 PIN, PSC288	PSC288	PLESS	8700-00-0003	1

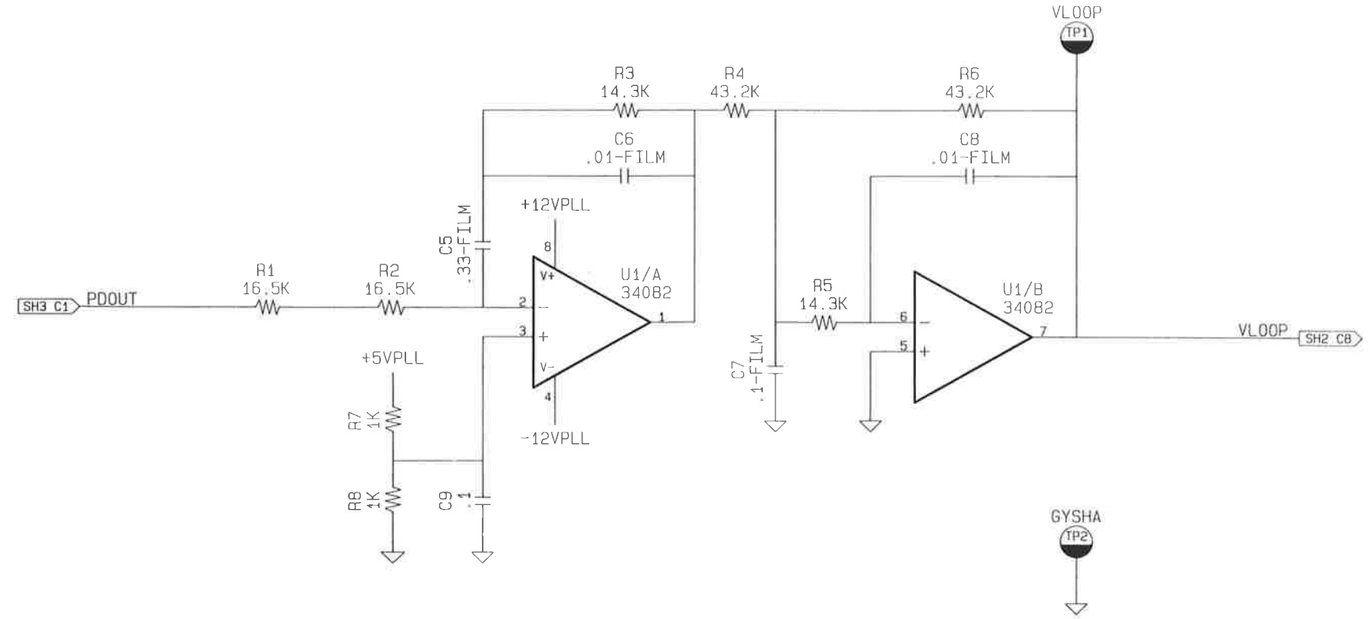
WAVETEK PARTS LIST | TITLE: 91 MOTHERBOARD PREWAVE LOAD | ASSEMBLY NO. 1200-00-3440 | REV B

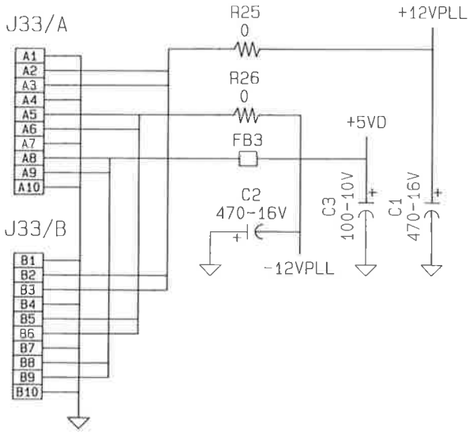
NOTE: UNLESS OTHERWISE SPECIFIED

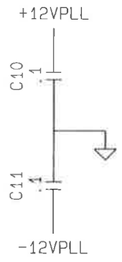
REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	CHECKED		TITLE: 91 MOTHERBOARD PREWAVE LOAD
	PROJ. ENGR.		
	RELEASE APPROV.		
FINISH WAVETEK PROCESS	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES ± .XX ± .XXX ± ±		SIZE D | FSCM NO. 23338 | DWG. NO. 1200-00-3440 | REV B
DO NOT SCALE DRAWING			SCALE | MODEL 91 | SHEET 2 OF 2

REV	ECO	BY	DATE	APP
A	ECO# 92-021	1/4	1 92	









REF. DES. LAST USED	REF. DES. NOT USED
U11	
R26	
C33	C4, 12, 14, 19
Q3	
CR6	CR4
F4B	
RN1	
P34	
DS1	

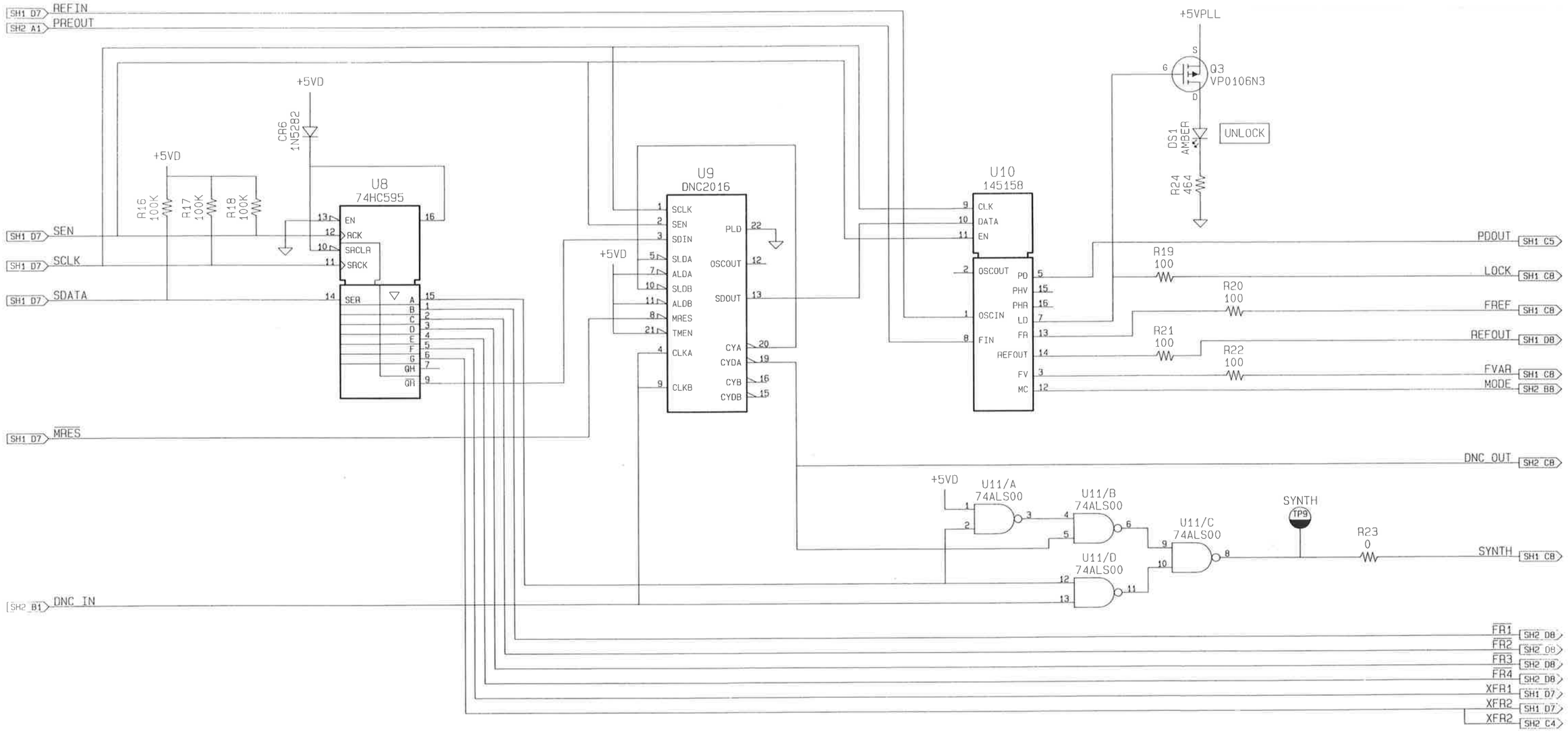
3. CAPACITORS VALUED IN MICROFARADS (uF).
2. RESISTORS VALUED IN OHMS, 1/8W, 1%.
1. FOR INSTRUMENT INTERCONNECTION, SEE INSTRUMENT SCHEMATIC.

NOTE: UNLESS OTHERWISE SPECIFIED

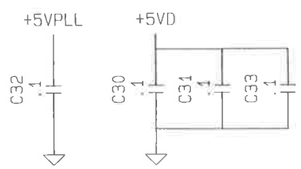
CAD JOB #: B077C

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN A.Tarr	DATE 12/91	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	CHECKED		TITLE: SCHEMATIC, SYNTHESIZER MODULE
	PROJ. ENGR.		
FINISH WAVETEK PROCESS	RELEASE APPROV.		
DO NOT SCALE DRAWING	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES .XX ± .XXX ± °		SIZE D · FSCM NO. 23338 · DWG. NO. 1104-00-3597 · REV A · SCALE NONE · MODEL 91 · SHEET 1 OF 3

REV	ECO	BY	DATE	APP



	U8	U9	U10	U11
	74HC595	DNC2016	145158	74ALS00
+5VPLL			4	
+5VD		6, 18		14
GND	8	14, 17	6	7
CAP	C30	C31	C32	C33



NOTE UNLESS OTHERWISE SPECIFIED

CAD JOB #: B077C

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN A.Tarr	DATE 12/91
MATERIAL	CHECKED	
	PROJ. ENGR.	
	RELEASE APPROV.	
FINISH WAVETEK PROCESS	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES .XX ± .XXX ±	
DO NOT SCALE DRAWING		

WAVETEK SAN DIEGO, CALIFORNIA

TITLE: SCHEMATIC, SYNTHESIZER MODULE

SIZE	FSCM NO.	DWG. NO.	REV
D	23338	1104-00-3597	A

SCALE NONE | MODEL 91 | SHEET 2 OF 3

REV	ECO	BY	DATE	APP

SH3 B1 FR4
SH3 B1 FR3
SH3 B1 FR2
SH3 B1 FR1
SH3 B1 DNC OUT
DNCOUT TP7
+5VD
VCO TP3
+5VPLL
+12VPLL
C17 22-15V
C16 .1
C15 .01
U2 MC1648
VCC1 VCC2 VEE1 VEE2
L1 99nH
FB4
C20 .1
C21 22-15V
C18 .01
R9 274
CR3 1N747A 3.6V
CR2 HP5082-2811
C36 5pF
CR1 MV1404
C13 .01
R10 4.99K
R11 4.99K
SH1 C1 VLOOP
C35 220pF
GYSHD TP4
C22 .001
U3 MC12017
VCC SIG SGND CONT VREG OUT PULLUP GND
C23 .001
C24 .1
SH3 B1 MODE
U4/A MC10H131
CCLK SET CLK D CLR Q
U4/B MC10H131
XFR2 SH3 B1
RN1/G 470
RN1/H 470
RN1/I 470
RN1/D 470
RN1/C 470
R14 165
R13 39.2
2N3906 Q1
2N3906 Q2
C25 .1
VCO/2 TP5
VCO/4 TP6
TTLVCO/4 TP8
CR5 1N5282
R15 4.02K
U5 MC10H121
U6 78M05 IN OUT COM
C28 1-35V
C29 1-35V
HFSYNTH SH1 C7
HF SYNTH SH1 C7
P34
RN1/B 470
RN1/A 470
DNC IN SH3 B8
PREOUT SH3 D8

	U4	U5
	10H131	10H121
+5VD	1, 16	1, 16
GND	8	8
CAP	C26	C27

+5VD
C26 .1
C27 .1

NOTE: UNLESS OTHERWISE SPECIFIED

CAD JOB #: B077C

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN A.Tarr	DATE 12/91
MATERIAL	CHECKED	
	PROJ. ENGR.	
	RELEASE APPROV.	
FINISH WAVETEK PROCESS	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES ± .XX ± .XXX ± ±	
DO NOT SCALE DRAWING		

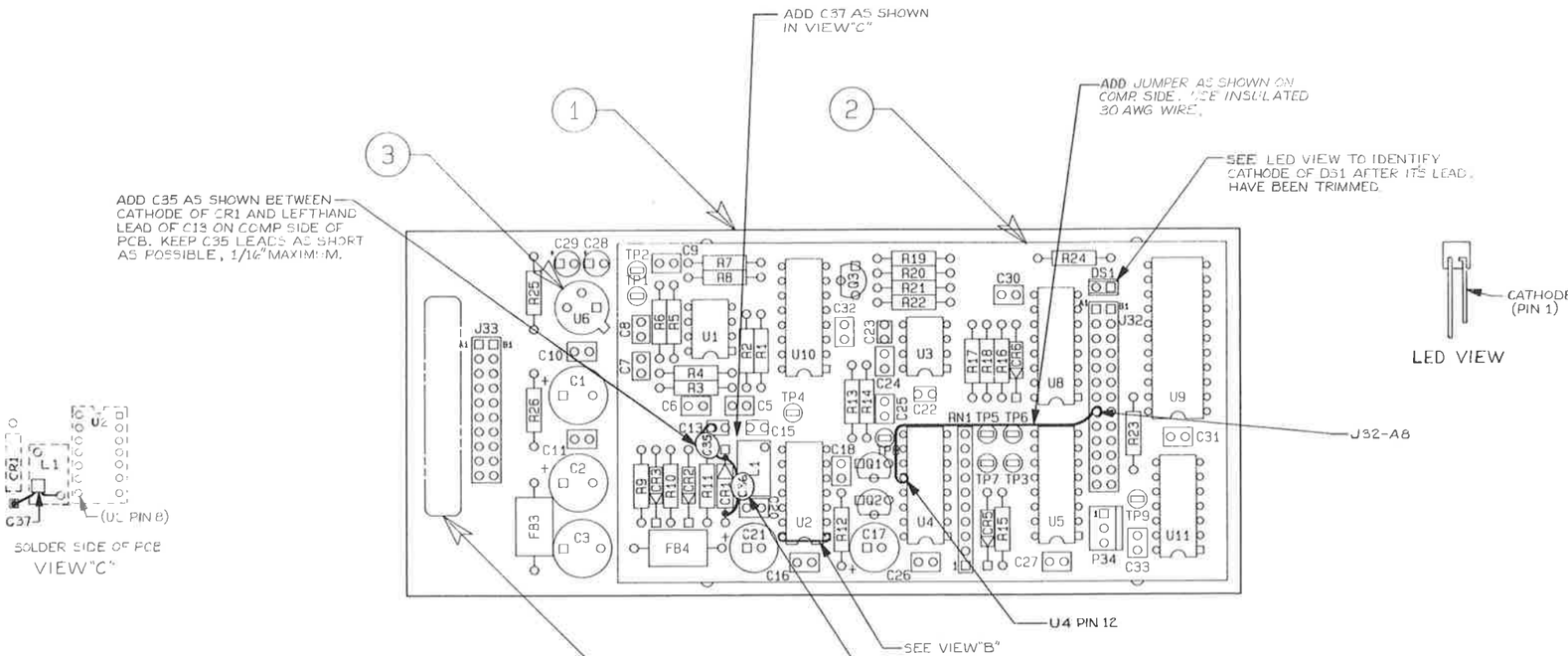
WAVETEK SAN DIEGO, CALIFORNIA

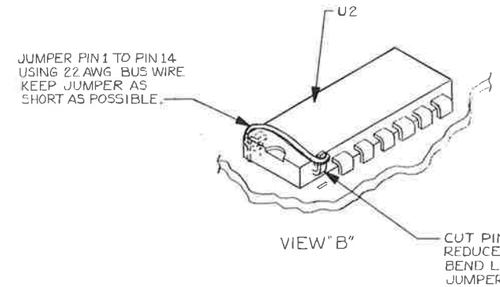
TITLE: SCHEMATIC, SYNTHESIZER MODULE

SIZE	FSCM NO.	DWG. NO.	REV
D	23338	1104-00-3597	A

SCALE NONE | MODEL 91 | SHEET 2 OF 2

REV	ECO	BY	DATE	APP
A	ECO 92-021	SC	12/17/91	JM





5. APPLY WAVETEK TYPE 1 LABEL, (EPC # MCW10F .25x1.5 WHITE VINYL CLOTH OR EQUIV.), SHOWING ASSY P/N REVISION AND MANUFACTURERS DATE INFORMATION.

4. ASSEMBLE PER WAVETEK WORKMANSHIP STANDARDS.
3. REFERENCE DESIGNATIONS DO NOT APPEAR ON PARTS.
2. FOR ASSEMBLY INTERCONNECTION, SEE INSTRUMENT SCHEMATIC.
1. SEE 1104-00-3460 FOR SCHEMATIC.

NOTE UNLESS OTHERWISE SPECIFIED

CAD JOB #: B077B

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN A. Talmadge-Lee	DATE 5/91
MATERIAL	CHECKED J.M.	6-20-91
	PROJ. ENGR. J. McCOSH	6-20-91
	RELEASE APPROV. N.E. MILLER	6-20-91
FINISH WAVETEK PROCESS	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES .XX ± .XXX ± ±	
DO NOT SCALE DRAWING		

WAVETEK SAN DIEGO, CALIFORNIA

TITLE: PCA, SYNTHESIZER MODULE

SIZE	FSCM NO.	DWG. NO.	REV
D	23338	1101-00-3597	A
SCALE NONE	MODEL 91	SHEET 1 OF 1	

1101-00-3597 A

REV	ECO	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
REF	A/D SYNTHESIZER BD-91	1101-00-3597	WVTK	1101-00-3597	1
REF	SCHEMATIC, SYNTHESIZER BD-91	1104-00-3597	WVTK	1104-00-3597	1
NONE	SYNTHESIZER BD PRE-WAVE LOAD-91	1200-00-3597	WVTK	1200-00-3597	1
2	CAN, M/B SYNTHESIZER	1400-02-5139	WVTK	1400-02-5139	1
C36	CAP, CER DISK, 5PF, 1KV, 10%	0311-00018	WVTK	1500-00-5011	1
C37	CAP CER MON .01MF 50V Z5U +80/-20% RAD LD .2	1C20Z5U103M050B	SPRAG	1500-01-0311	1
C35	CAP, CER, 220PF, 1KV	DD-221	CRL	1500-02-2111	1
J33	SOCKET, 20 PIN, ST, LOW INSERT	SSW-110-02-G-D	SAM	2100-03-0001	1
J32	SOCKET, 26 PIN, ST, LOW INSERT	SSW-113-02-G-D	SAM	2100-03-0110	1
U2	OSC EMT CUPLD, ECL	MC1648P	MOT	8100-16-4810	1

WAVETEK PARTS LIST | TITLE: PCA, SYNTHESIZER BD-91 | ASSEMBLY NO. 1100-00-3597 | REV A | PAGE 1

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
CR3	DIODE ZENER, 1N747A 400MW 3.6V 5%	1N747A	MOT	0374-00080	1
C22 C23	CAP, CER, .001 MF, +-10%, 50V, X7R, .1" LS	SR155C102KAA	AVX	1500-01-0207	2
C13 C15 C18	CAP, CER, .01MF, +-10%, 50V, X7R, .1"LS	SR155C103KAA	AVX	1500-01-0307	3
C10 C11 C16 C20 C24 C25 C26 C27 C30 C31 C32 C33 C9	CAP, CER, .1 MF, 50V, X7R, +-10%, .1" LS	SR205C104KAA	AVX	1500-01-0415	13
C1 C2	CAP, ALUM ELECT, 470MF, 20%, 16V, RADAIL .2" SP, 10MM DIAx12.5MM HT	KME16VB471M10X12LL	UNCON	1500-34-7114	2
C7	CAP, MET POLYS, .1MF, 10%, 63V, .1 "LS	MKS02-0.1MF-10%-63V	WIMA	1500-41-0418	1
C5	CAP, MET POLYS, .33 MF, +-20%, 50V, .1"LS	MKS02-.33MF-20%-50V	WIMA	1500-41-0421	1
C6 C8	CAP, MET POLYS, 0.01MF, +-20%, 63V, .1"LS	MKS02-0.01MF, 20%-63V	WIMA	1500-41-0422	2
C28 C29	CAP, TANT, 1MF, 35V	196D1050035HA1(OBS)	SPRAG	1500-71-0512	2
C3	CAP, TANT, 100MF, 10V	199D107X9010EE4	SPRAG	1500-71-0711	1

WAVETEK PARTS LIST | TITLE: SYNTHESIZER BD PRE-WAVE LOAD-91 | ASSEMBLY NO. 1200-00-3597 | REV A | PAGE 1

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R9	RES, MF, 1/8W, 1%, 274	RN55D-2740F	TRW	4701-03-2740	1
R13	RES, MF, 1/8W, 1%, 39.2	RN55D-39R2F	TRW	4701-03-3929	1
R15	RES, MF, 1/8W, 1%, 4.02K	RN55D-4021F	TRW	4701-03-4021	1
R4 R6	RES, MF, 1/8W, 1%, 43.2K	RN55D-4322F	TRW	4701-03-4322	2
R24	RES, MF, 1/8W, 1%, 464	RN55D-4640F	TRW	4701-03-4640	1
R10 R11	RES, MF, 1/8W, 1%, 4.99K	RN55D-4991F	TRW	4701-03-4991	2
RN1	RES NETWORK 470 10PIN SIP BUSS	4310R-101-471	BOURN	4770-00-0009	1
R23 R25 R26	RES, 0 OHM JUMPER	JP02T68Q	ROHM	4799-00-0087	3
CR5 CR6	DIODE, HIGH CONDUCTANCE, ULTRA FAST	1N5282	FAIR	4801-01-5282	2
CR1	DIODE, HIGH CAP TUNING	MV1404	MOT	4803-02-1404	1
CR2	DIODE 5082-2811 SCHOTTKY, 15V, 20MA	5082-2811	HP	4809-02-2811	1
DS1	LED, AMBER, RECT BAR	LTL-3251A	LITE	4899-00-0056	1
Q1 Q2	TRANS 2N3906 PNP GENERAL PURPOSE TO-92	2N3906(OBS)	FAIR	4901-03-9060	2
Q3	TRANS, FET P CHANNEL	VP0106N3	SUPER	4902-01-0601	1

WAVETEK PARTS LIST | TITLE: SYNTHESIZER BD PRE-WAVE LOAD-91 | ASSEMBLY NO. 1200-00-3597 | REV A | PAGE 3

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
C17 C21	CAP, TANT, 22MF, 15V	196D226X9015KA1(OBS)	SPRAG	1500-72-2601	2
1	PCB SYNTHESIZER BD REF: SPEC 0008-00-0455 REV C	1700-00-3460	WVTK	1700-00-3460	1
L1	INDUCTOR, 99 NH, 5%, G66	132-07	COILC	1800-00-0050	1
P34	CONN, HEADER, 3 PIN, .100 MTA	640456-3	AMP	2100-02-0116	1
TP2 TP4	TEST POINT, BLK, PC	TP-104-01-00	COMPD	2100-04-0054	2
TP1 TP3 TP5 TP6 TP7 TP8 TP9	TEST POINT, RED, PC	TP-104-01-02	COMPD	2100-04-0055	7
3	TRANSIPAD	10123N(OBS)	METRS	2800-11-0003	1
FB3 FB4	BALUN CORE, FERRITE, 680 OHMS	2943666671	FARIT	3100-00-0017	2
R19 R20 R21 R22	RES, MF, 1/8W, 1%, 100	RN55D-1000F	TRW	4701-03-1000	4
R7 R8	RES, MF, 1/8W, 1%, 1K	RN55D-1001F	TRW	4701-03-1001	2
R16 R17 R18	RES, MF, 1/8W, 1%, 100K	RN55D-1003F	TRW	4701-03-1003	3
R3 R5	RES, MF, 1/8W, 1%, 14.3K	RN55D-1432F	TRW	4701-03-1432	2
R14	RES, MF, 1/8W, 1%, 165	RN55D-1650F	TRW	4701-03-1650	1
R1 R2	RES, MF, 1/8W, 1%, 16.5K	RN55D-1652F	TRW	4701-03-1652	2

WAVETEK PARTS LIST | TITLE: SYNTHESIZER BD PRE-WAVE LOAD-91 | ASSEMBLY NO. 1200-00-3597 | REV A | PAGE 2

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
U1	OP AMP, HI SLEW RTE, WIDEBND, JFET DUAL	MC34082P	MOT	7003-40-8200	1
U11	GATE, NAND, QUAD 2-INP, TTL	SN74LS00N	TI	8000-74-0010	1
U8	SHFT REG, 8-BIT, CMOS, OUTPUT CLR	SN74HC595N	TI	8000-74-5950	1
U6	VOLT REGULATOR	LM78M05CH	NSC	8000-78-0501	1
U5	GATE, OR AND/OR AND INVER DUAL WIDE, ECL	MC10H121P	MOT	8001-01-2100	1
U4	FLIP-FLOP, DUAL D, MAS/SL, ECL	MC10H131P	MOT	8001-01-3101	1
U3	PRESCALER, DUAL MODULUS, DIVIDE-BY-64/65, ECL	MC12017P	MOT	8012-01-1700	1
U10	PLL SERIES INPUT FREQ SYNTHESIZER	MC145158P(OBS)	MOT	8014-51-5800	1
U9	GATE ARRAY, COUNTER, SYNCH, MULTI-MODE, 32-BIT	CLA53047BA	PLESS	8700-00-0005	1

WAVETEK PARTS LIST | TITLE: SYNTHESIZER BD PRE-WAVE LOAD-91 | ASSEMBLY NO. 1200-00-3597 | REV A | PAGE 4

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES | MATERIAL | FINISH WAVETEK PROCESS | DO NOT SCALE DRAWING

DRAWN | DATE | CHECKED | PROJ. ENGR. | RELEASE APPROV.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES ± .XX ± .XXX ± ±

WAVETEK SAN DIEGO • CALIFORNIA

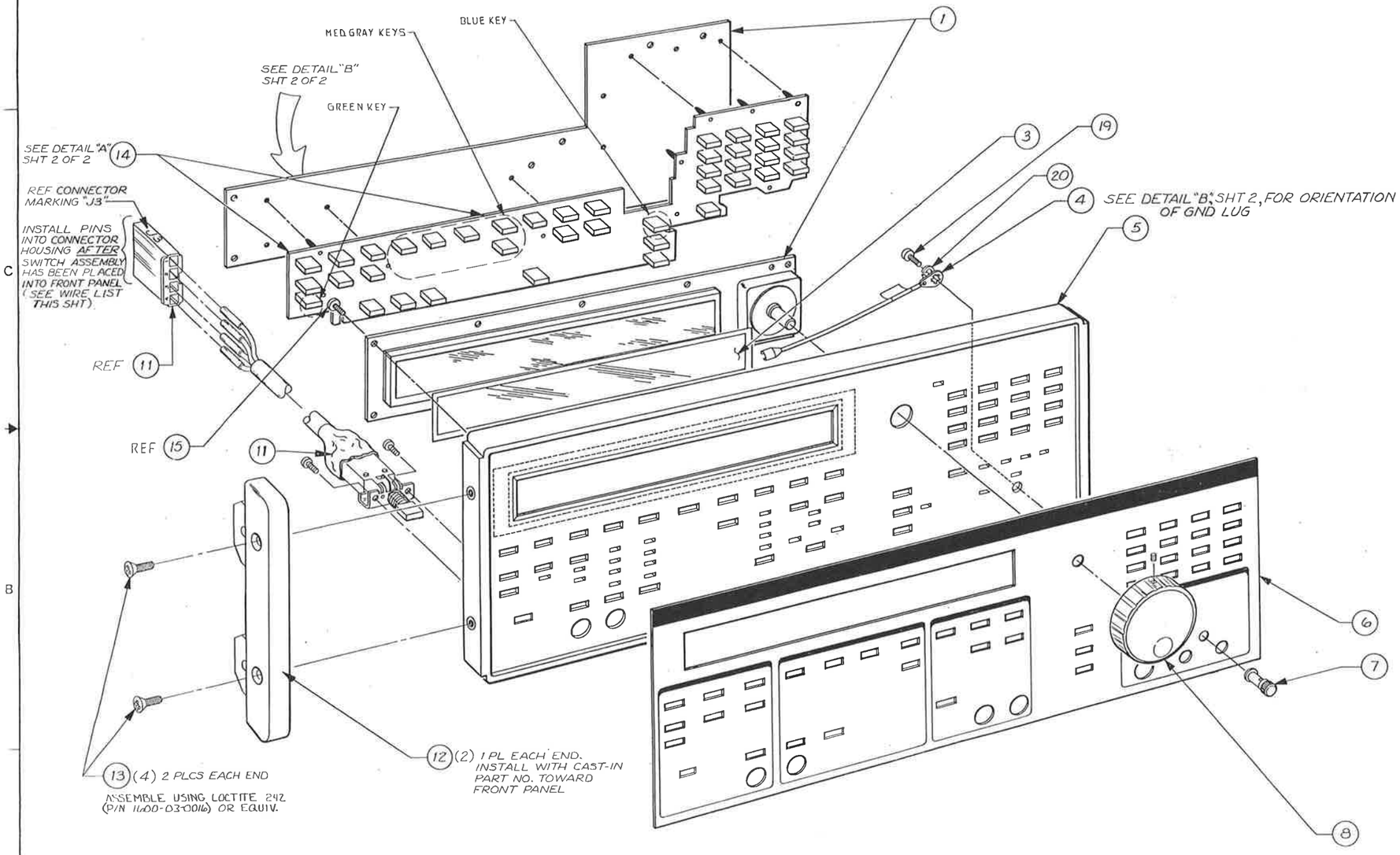
TITLE: PCA, SYNTHESIZER BD-91 WITH PRELOAD

SIZE	FSCM NO.	DWG. NO.	REV
D	23338	1100-00-3597	A

SCALE | MODEL 91 | SHEET 1 OF 1

MODIFIED FROM DWG 1101-00-3321

REV	ECO	BY	DATE	APP
A	ECO 91-[illegible]	[illegible]		[illegible]



WIRE LIST

"J3" CONN PIN NO.	WIRE COLOR
3	RED
2	WHT
4	GRN
1	BLK

SEE SEPARATE PARTS LIST

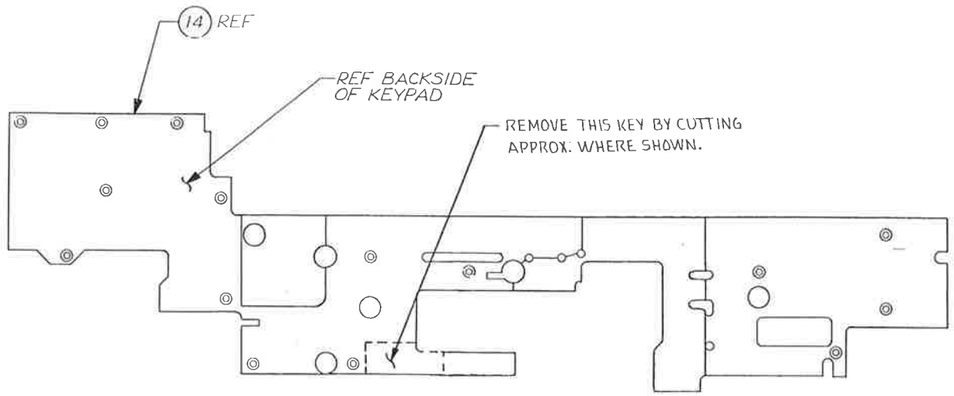
1. MARK ASSEMBLY NO. "1101-00-3439", LATEST REV. AND DATE CODE, PER MIL-STD-130, APPROX WHERE SHOWN.

NOTE: UNLESS OTHERWISE SPECIFIED

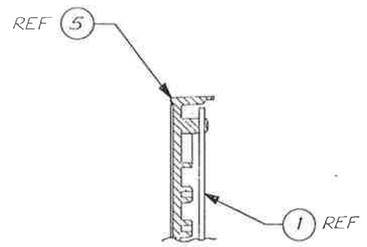
REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN NM SC/AP	DATE 5-18-90	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	CHECKED N. S. Miller	9/21/91	TITLE: ASSEMBLY, FRONT PANEL
	PROJ. ENGR N. S. Miller	9/21/91	
	RELEASE APPROV N. S. Miller	9/21/91	
FINISH WAVETEK PROCESS	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES ± / .XX ± .XXX ± / ±		SIZE D; FSCM NO. 23338; DWG. NO. 1101-00-3439; REV A
DO NOT SCALE DRAWING			SCALE ∧ ONE; MODEL 91; SHEET 1 OF 2

1101-00-3439 A

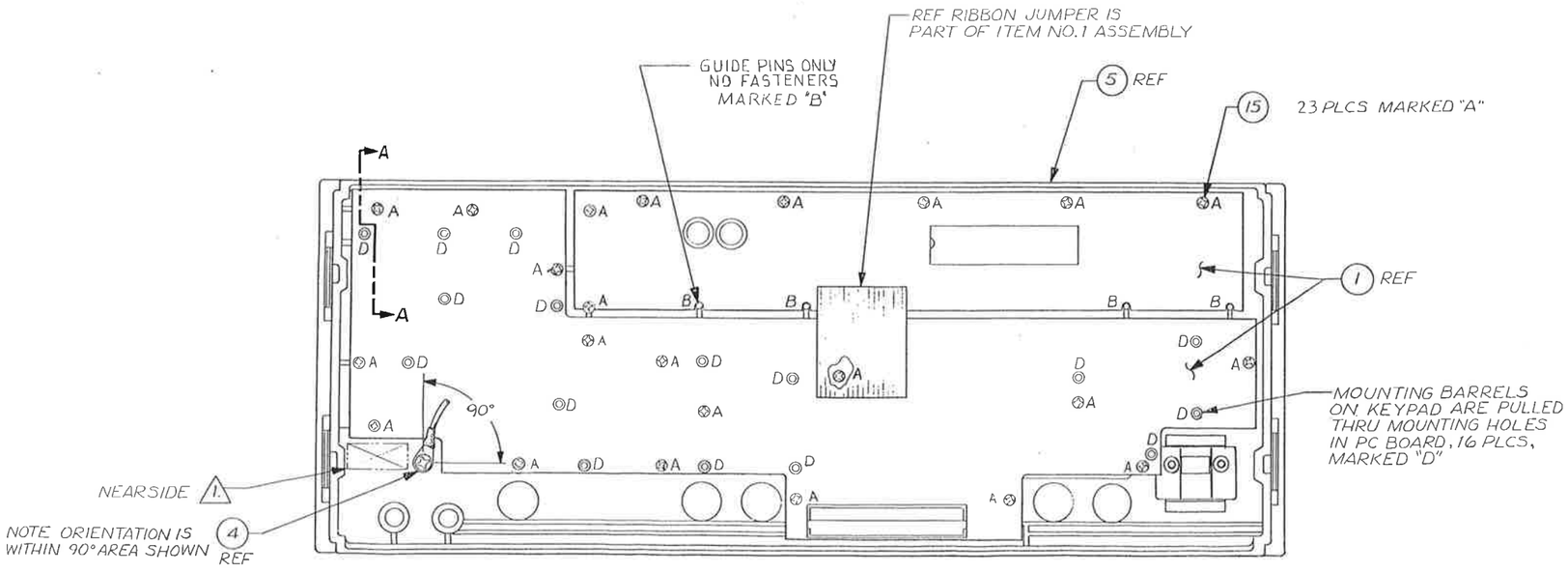
REV	ECN	BY	DATE	APP



DETAIL "A"
(KEYPAD PREP. NOTE: KEYS OF KEYPAD ARE NOT SHOWN)



SECTION VIEW A-A



DETAIL "B"
(PC BOARD TO FRONT PANEL INSTALLATION)

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN SC	DATE 5-11-90	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENG Jim B Mc Cue	7/12/91	TITLE: ASSEMBLY, FRONT PANEL
FINISH WAVETEK PROCESS	RELEASE APPROV		
	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX — ANGLES ±1° XX —		
	DO NOT SCALE DWG	MODEL NO. 91	DWG NO. 1101-00-3439 REV A
	SCALE NONE	CODE IDENT 23338	SHEET 2 OF 2

1101-00-3439 A

REV	ECO	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
1	PCA, DISPLAY/ KEYBOARD	1100-00-3322	WVTK	1100-00-3322	1
NA	A/D FRONT PANEL 91	1101-00-3439	WVTK	1101-00-3439	1
8	ENCODER KNOB ASSY REF: A/D 1201-00-3380	1200-00-3380	WVTK	1200-00-3380	1
11	CABLE ASSY, AC SWITCH AND CABLE	1200-00-3391	WVTK	1200-00-3391	1
4	WIRE ASSY	1207-00-3010	WVTK	1207-00-3010	1
14	KEY PAD, MODEL 95	1400-02-3420-02	CRT	1400-02-3420	1
12	CORNER BRACKET, PAINTED	1400-02-5034	WVTK	1400-02-5034	2
3	WINDOW, DISPLAY	1400-02-5073	WVTK	1400-02-5073	1
5	FRONT PANEL MOLDED	1400-02-5087	WVTK	1400-02-5087	1
6	OVERLAY, DISPLAY-91	1400-02-5120	WVTK	1400-02-5120	1
7	LUG, GROUNDING	159	SMITH	2100-04-0043	1
20	WASHER, LOCK, REG 8/8 #6	MS 35338-136	CMRCL	2800-43-6000	1
13	SCREW, 8-32 X 1/2, 100 DEG, FH, PHLPS, SS	2800-54-8108	CMCRL	2800-54-8108	4
15	SCREW, 2 X 5/16, TYPE B, THD FORM, PH, SS	2800-57-2905	CMRCL	2800-57-2905	23
19	SCREW, PH, 6-32 X 5/16, PHLPS, NYLOK, SS	2800-59-6105	CMRCL	2800-59-6105	1

WAVETEK PARTS LIST	TITLE	ASSEMBLY NO.	REV
	FRONT PANEL ASSY	1100-00-3439	A
		PAGE 1	
		PAGE 2	

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	CHECKED		TITLE: FRONT PANEL ASSY
	PROJ. ENGR.		
	RELEASE APPROV.		
FINISH WAVETEK PROCESS	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES .XX ± .XXX ± °		SIZE D · FSCM NO. 23338 · DWG. NO. 1100-00-3439 · REV A
DO NOT SCALE DRAWING			SCALE · MODEL 91 · SHEET 1 OF 1

REV	ECO	BY	DATE	APP

DISPLAY BOARD

VR1
78L15
IN COM OUT

+22V
-22V
+15ISO
+5V

C3 100
C4 .1
C9 22
C8 .1
C7 .1
C2 100
C1 .1
C6 .1
C18 100

R1 2.49K
R2 2.49K
R3 2.49K
R4 10K
R5 10K
R6 10K

Q1 2N3904
Q2 2N3904
Q3 2N3904

U1
10957P40
SCLK
DATA
POR

RN1 47K
RN2 47K
RN3 47K
RN4 47K

VFD1
ITRON FG1611A1

AD16 AD15 AD14 AD13 AD12 AD11 AD10 AD9 AD8 AD7 AD6 AD5 AD4 AD3 AD2 AD1
SGA SGC SGD SGF SGG SGH SGO SGK SGI SGM SGJ SGP SGL SGN PNT TAIL SGB SGE
G1 G2 G3 G4 G5 G6 G7 G8 G9 G10 G11 G12 G13 G14 G15 G16
PA PB PC PD PE PF PG PH PI PJ PK PL PM PN PDP PCOM F1 F2

J1B
-22V 1
GND 2
+22V 3
GND 4
FILA 5
FILB 6
GND 7
CHA 8
CHB 9
DSPOR 10
DSPCLK 11
DSPDATA 12
F02 B8

SW1
ROTARY
ENCODER
CHA CHB COM

C5 .1

3. FOR INSTRUMENT INTERCONNECTION, SEE INSTRUMENT SCHEMATIC.
2. ALL CAPACITORS ARE IN MICROFARADS (uF).
1. ALL RESISTORS ARE IN OHMS, 1/8W, 1%, MF.

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN A. TALMADGE	DATE 7-11-90	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	CHECKED		TITLE: SCHEMATIC, DISPLAY/KEYBOARD
	PROJ. ENGR.		
FINISH WAVETEK PROCESS	RELEASE APPROV.		
DO NOT SCALE DRAWING	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES .XX .XXX		SIZE D · FSCM NO. 23338 · DWG. NO. 1104-00-3322 · REV A · SCALE NONE · MODEL 90 SERIES · SHEET 1 OF 4

REV	ECO	BY	DATE	APP

FPREG
F03 D6
QA1
F03 D8
QA0
F03 D8
FPS
F03 D8

P12
1 GND
2
3
4
5 GD6
6 GD7
7 GD4
8 GD5
9 GD2
10 GD3
11 GD0
12 GD1
13 GND
14
15 P10
16 P11
17 P12
18 P13
19 P14
20 P15
21 P16
22 P17
23 GND
24
25 +5PV
26
27
28 CHA
29 GND
30 CHB
31 FIL A
32 FIL B
33 GND
34
35 +22PV
36
37 GND
38
39 -22PV
40

+5V
U3
74ALS574
20
11 CLK
1 OC
GD0 2 1D 1Q 19
GD1 3 2D 2Q 18
GD2 4 3D 3Q 17
GD3 5 4D 4Q 16
GD4 6 5D 5Q 15
GD5 7 6D 6Q 14
GD6 8 7D 7Q 13
GD7 9 8D 8Q 12
10

C19
.1

RN7
100
1
7
CR1

RN7
100
1
5
CR2

+5V
U2
4051
16
C16
.1
11 S0
10 S1
9 S2
6 G
+5V
3 A
B0 13
B1 14
B2 15
B3 12
B4 1
B5 5
B6 2
B7 4
7
8

J1A
-22V 1
GND 2
+22V 3
4
FIL A 5
FIL B 6
CHA 7
CHB 8
DSPOR 9
DSPCLK 10
DSPDATA 11
12
F01 B8

* SEE SHEET 4 FOR KEY ASSIGNMENTS

A1 A2 A3 A4 A5 A6 A7 A8
B1 B2 B3 B4 B5 B6 B7 B8
C1 C2 C3 C4 C5 C6 C7 C8
D1 D2 D3 D4 D5 D6 D7 D8
E5 E6 E7 E8
F1 F3 F5 F6 F7 F8

P10
P11
P12
P13
P14
P15
P16
P17

RN5
10K
10 9 8 7 6 5 4 3 2 1

RN9
10K
10 9 8 7 6 5 4 3 2 1

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN A. TALMADGE	DATE 7-11-90	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	CHECKED	7-20-90	TITLE: SCHEMATIC, DISPLAY/KEYBOARD
	PROJ ENGR	7/24/90	
FINISH WAVETEK PROCESS	RELEASE APPROV.	7/24/90	
DO NOT SCALE DRAWING	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES XX ± XXX ± °		SIZE D · FSCM NO. 23338 · DWG NO. 1104-00-3322 · REV A · SCALE NONE · MODEL 90 SERIES · SHEET 2 OF 4

1104-00-3341 A

REV	ECO	BY	DATE	APP

+5V

C15 .1

QA0 F02 D8
QA1 F02 D8
FPS F02 D8

U4 74ALS138

A, B, C, G1, G2A, G2B, EN
Y0, Y1, Y2, Y3, Y4, Y5, Y6, Y7
N/C, N/C, N/C, N/C

FPREG C8 F03

U5 74ALS574

CLK, OC
1D 2D 3D 4D 5D 6D 7D 8D
1Q 2Q 3Q 4Q 5Q 6Q 7Q 8Q

C12 .1

RN8 100 — CR4
RN8 100 — CR5
RN8 100 — CR6
RN8 100 — CR7
RN8 100 — CR8
RN8 100 — CR9
RN8 100 — CR10
RN8 100 — CR11

C13 .1

* SEE SHEET 4 FOR LED ASSIGNMENTS

U6 74ALS574

C11 .1

RN8 100 — CR12
RN10 100 — CR13
RN10 100 — CR14
RN10 100 — CR15
RN7 100 — CR3
RN7 100 — CR17
RN7 100 — CR18
RN7 100 — CR19

QD3

C10 .1

* SEE SHEET 4 FOR LED ASSIGNMENTS

U7 74ALS574

C14 .1

RN10 100 — CR20
RN10 100 — CR21
RN10 100 — CR22
RN10 100 — CR23
R8 100 — CR24
RN10 100 — CR25
R9 100 — CR26
R7 100 — CR27

C17 .1

* SEE SHEET 4 FOR LED ASSIGNMENTS

F02 C8 QD0
F02 C8 QD1
F02 C8 QD2
F02 C8 QD3
F02 C8 QD4
F02 C8 QD5
F02 C8 QD6
F02 C8 QD7

RN6 10K

+5V

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN A. TALMADGE	DATE 7-13-90	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	CHECKED	7-26-90	TITLE: SCHEMATIC, DISPLAY/KEYBOARD
	PROJ. ENGR.	8/16/90	
FINISH WAVETEK PROCESS	RELEASE APPROV.	8/20/90	
DO NOT SCALE DRAWING	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES XX ± XXX ±		SIZE D · FSCM NO. 23338 · DWG. NO. 1104-00-3322 · REV A · SCALE NONE · MODEL 90 SERIES · SHEET 3 OF 4

1104-00-3322

REV	ECO	BY	DATE	APP

LED ASSIGNMENTS

	90	95
CR1	UNLOCK	UNLOCK
CR2	EXT	EXT
CR3		DL
CR4	600	600
CR5	135	135
CR6	75	75
CR7	BAL	BAL
CR8	50	50
CR9	ENABLE	ENABLE
CR10	REMOTE	REMOTE
CR11	HV OPT	
CR12	AM	AM
CR13	FM	FM
CR14	SWEEP	SWEEP
CR15	SCM	SCM
CR17		~
CR18		⊓
CR19		∿
CR20	TRIG	TRIG
CR21	GATE	GATE
CR22	CONT	CONT
CR23	BURST	BURST
CR24	DC	ARB4
CR25	⊓	ARB3
CR26	∿	ARB2
CR27	~	ARB1

KEY ASSIGNMENTS - MODEL 90

	1	2	3	4	5	6	7	8
A	AMPL	FREQ		SYMM	1	0	7	4
B	OFFSET	DISPLAY		SOURCE	2	.	8	5
C	STORE	RESET	PHASE	FUNCTION	3	+/-	9	6
D	→		←	BURST CNT	EXP	ENTER	KNOB	CE
E					CMD RECALL	ON/OFF	LOCAL	SHIFT
F	MAN TRIG		SWEEP MODE			MODE	TRIG FREQ	TIME

KEY ASSIGNMENTS - MODEL 95

	1	2	3	4	5	6	7	8
A	AMPL	FREQ	SYNC ADDR	FILTER	1	0	7	4
B	OFFSET	Z-AXIS	CURSORS	PHASE	2	.	8	5
C	STORE	RESET	ADDRESS	FUNCTION	3	+/-	9	6
D	EDIT	SOURCE	DATA	BURST CNT	EXP	ENTER	KNOB	CE
E					CMD RECALL	ON/OFF	LOCAL	SHIFT
F	MAN TRIG		SWEEP MODE			MODE	TRIG FREQ	TIME

NOTE UNLESS OTHERWISE SPECIFIED

CAD JOB #: B068A

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN A. TALMADGE	DATE 7-11-90	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	CHECKED	7-16-90	TITLE: SCHEMATIC, DISPLAY/KEYBOARD
	PROJ. ENGR.	7-16	
FINISH WAVETEK PROCESS	RELEASE APPROV.	7/16/90	
DO NOT SCALE DRAWING	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES ± .XX ± .XXX ± °		SIZE D · FSCM NO. 23338 · DWG. NO. 1104-00-3322 · REV A · SCALE NONE · MODEL 90 SERIES · SHEET 4 OF 4

1104-00-3322

REV	ECN	BY	DATE	APP
A	ERO#90-462	PT	7/9/90	

NOTES:

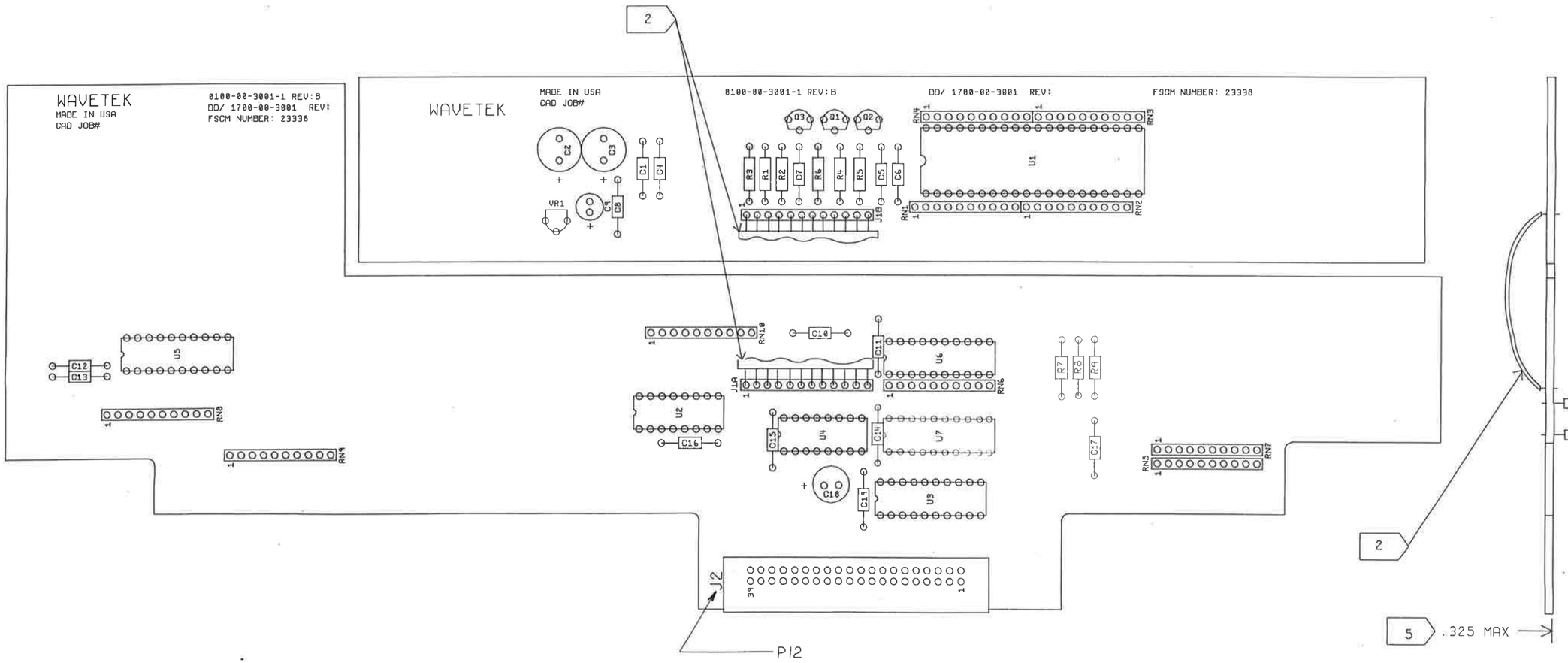
1. COMPONENTS MOUNTED ON COMPONENT SIDE OF PCB SHOWN ON SHEET 1, COMPONENTS MOUNTED ON SOLDER SIDE OF PCB SHOWN ON SHEET 2.

2. RIBBON CABLE IS INSTALLED BETWEEN J1A ON LOWER KEYBOARD PCB AND J1B ON UPPER DISPLAY PCB.

3. LEADS OF COMPONENTS MOUNTED ON COMPONENT SIDE OF PCB OPPOSITE DISPLAY (VFD1), MUST HAVE LEADS TRIMMED TO WITHIN .050 OF PCB SURFACE.

4. MOUNTING OF DISPLAY (VFD1):
   - A. INSTALL AND SOLDER COMPONENTS ON COMPONENT SIDE OF PCB.
   - B. TRIM LEADS OF COMPONENT ON UPPER BOARD PER NOTE 3.
   - C. ATTACH DISPLAY CUSHION (PN: 1400-02-3510) TO DISPLAY, POSITIONING CUSHION SO THAT IT DOES NOT OVERLAP DISPLAY.
   - D. PLACE DISPLAY (VFD1) WITH ATTACHED CUSHION ON SOLDER SIDE OF PCB MAKING SURE THAT THE SURFACE OF THE CUSHION IS FLUSH TO THE PCB SURFACE. PINS OF COMPONENTS ON OPPOSITE SIDE OF PCB WILL PIERCE THE CUSHION.
   - E. ALLOW DISPLAY (VFD1 ON COMPONENT SIDE) TO SELF-LEVEL BEFORE SOLDERING THE PINS OF DISPLAY.

5. LEDS (CR1 THRU CR27) MAY BE MOUNTED FLUSH TO PCB.



COMPONENT SIDE

NOTE: THIS CONNECTOR IS MARKED J2 ON THE PC BOARD SILKSCREEN

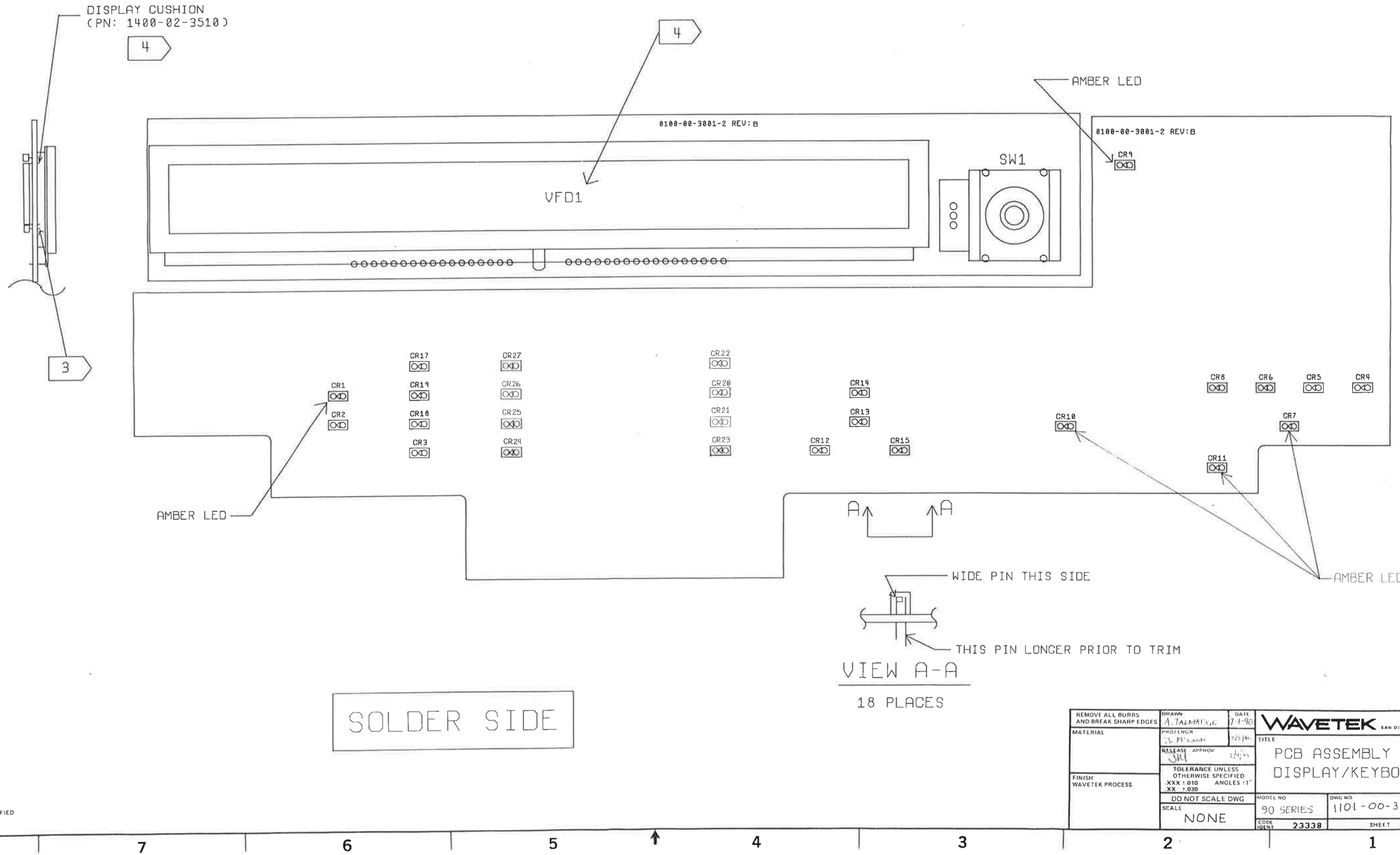
SEE SEPARATE PARTS LIST

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN A. TALMADGE	DATE 7-1-90	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR C. BY COSTA	7/9/90	TITLE PCB ASSEMBLY - DISPLAY/KEYBOARD
	RELEASE APPROV	7/9/90	
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1° XX ±.030		
	DO NOT SCALE DWG	MODEL NO. 90 SERIES	DWG NO. 1101-00-3322 REV A
	SCALE NONE	CODE IDENT 23338	SHEET 1 OF 2

REV	ECN	BY	DATE	APP

SEE SHEET #1



VIEW A-A

18 PLACES

SOLDER SIDE

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN A. TALMAI'c	DATE 7-1-90	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR J. Miranda		TITLE PCB ASSEMBLY - DISPLAY/KEYBOARD
FINISH WAVETEK PROCESS	RELEASE JM	APPROV	
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1° XX ± .030		
	DO NOT SCALE DWG	MODEL NO 90 SERIES	DWG NO 1101-00-3322 REV A
	SCALE NONE	CODE IDENT 23338	SHEET 2 OF 2

REV	ECO	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	A/D, DISPLAY/ KEYBOARD	1101-00-3322	WVTK	1101-00-3322	1
NONE	S/D DISPLAY, KEYBOARD	1104-00-3322	WVTK	1104-00-3322	1
NONE	CUSHION, DISPLAY	1400-02-3510	WVTK	1400-02-3510	1
C1 C10 C11 C12 C13 C15 C16 C19 C4 C5 C6 C7 C8	CAP,CER,MON,.1MF,50V, AXIAL	CAC03Z5U104Z050A	CORNG	1500-01-0405	13
C18 C2 C3	CAP,ELECT,100MF,35V RADIAL LEAD,SP .20	NRE101M35V10X12.5	NIC	1500-31-0102	3
C9	CAP,ELECT,22MF,25V,RA DIAL	SRA25VB22RM6X7LL	UNCON	1500-32-2002	1
NONE	PCB, DISPLAY/KEYBOARD REF: SPEC 0008-00-0455 REV C	1700-00-3001	WVTK	1700-00-3001	1
NONE	CONN,HEADER,40 PIN,PCB MT, .1 CTR,2X20,SHRD	1-102692-3	AMP	2100-02-0258	1
VFD1	DISPLAY,VAC,FLOUR	FQ1611A1	ITRON	2400-03-0019	1
R7 R8 R9	RES,MF,1/8W,1%,100	RN55D-1000F	TRW	4701-03-1000	3
R4 R5 R6	RES,MF,1/8W,1%,10K	RN55D-1002F	TRW	4701-03-1002	3
R1 R2 R3	RES,MF,1/8W,1%,2.49K	RN55D-2491F	TRW	4701-03-2491	3
RN5 RN6 RN9	RES NETWORK 10K 2%	4310R-101-103	BOURN	4770-00-0008	3

WAVETEK PARTS LIST	TITLE	ASSEMBLY NO.	REV
	PCA, DISPLAY/ KEYBOARD	1100-00-3322	C
		PAGE 1	

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
	10PIN SIP BUSS				
RN1 RN2 RN3 RN4	RES NETWORK 47K 2% 10PIN SIP BUSS	4310R-101-473	BOURN	4770-00-0030	4
RN10 RN7 RN8	RES NETWORK 10PIN SIP 100 OHM BUSS	4310R-101-101	BOURN	4770-00-0054	3
CR1 CR10 CR11 CR7 CR9	LED,AMBER,RECT BAR	LTL-3231A	LITE	4899-00-0056	5
CR12 CR13 CR14 CR15 CR17 CR18 CR19 CR2 CR20 CR21 CR22 CR23 CR24 CR25 CR26 CR27 CR3 CR4 CR5 CR6 CR8	LED,GREEN,RECT BAR	LTL-3231A	LITE	4899-00-0057	21
Q1 Q2 Q3	TRANS 2N3904 NPN GENERAL PURPOSE TO-92	2N3904	FAIR	4901-03-9040	3
SW1	ENCODER, ROTARY, MADE FROM 5104-00-0027	5109-00-0001	WVTK	5109-00-0001	1
J1A	CABLE,FLEX,JMP,ASSY	1-86943-1	AMP	6001-60-0017	1
VR1	VOLT REGULATOR, POSITIVE	78L15	TI	7000-78-1501	1
U2	MUX/DEMUX, ANALOG	CD4051BE	RCA	8000-40-5100	1
U1	CONTROLLER,ALPH NUM DISP,40V	10957P-50	ROCK	8001-09-5700	1
U4	DECODER/DEMUX, 3 TO 8 LINE	SN74ALS138N	TI	8007-41-3800	1

WAVETEK PARTS LIST	TITLE	ASSEMBLY NO.	REV
	PCA, DISPLAY/ KEYBOARD	1100-00-3322	C
		PAGE 2	

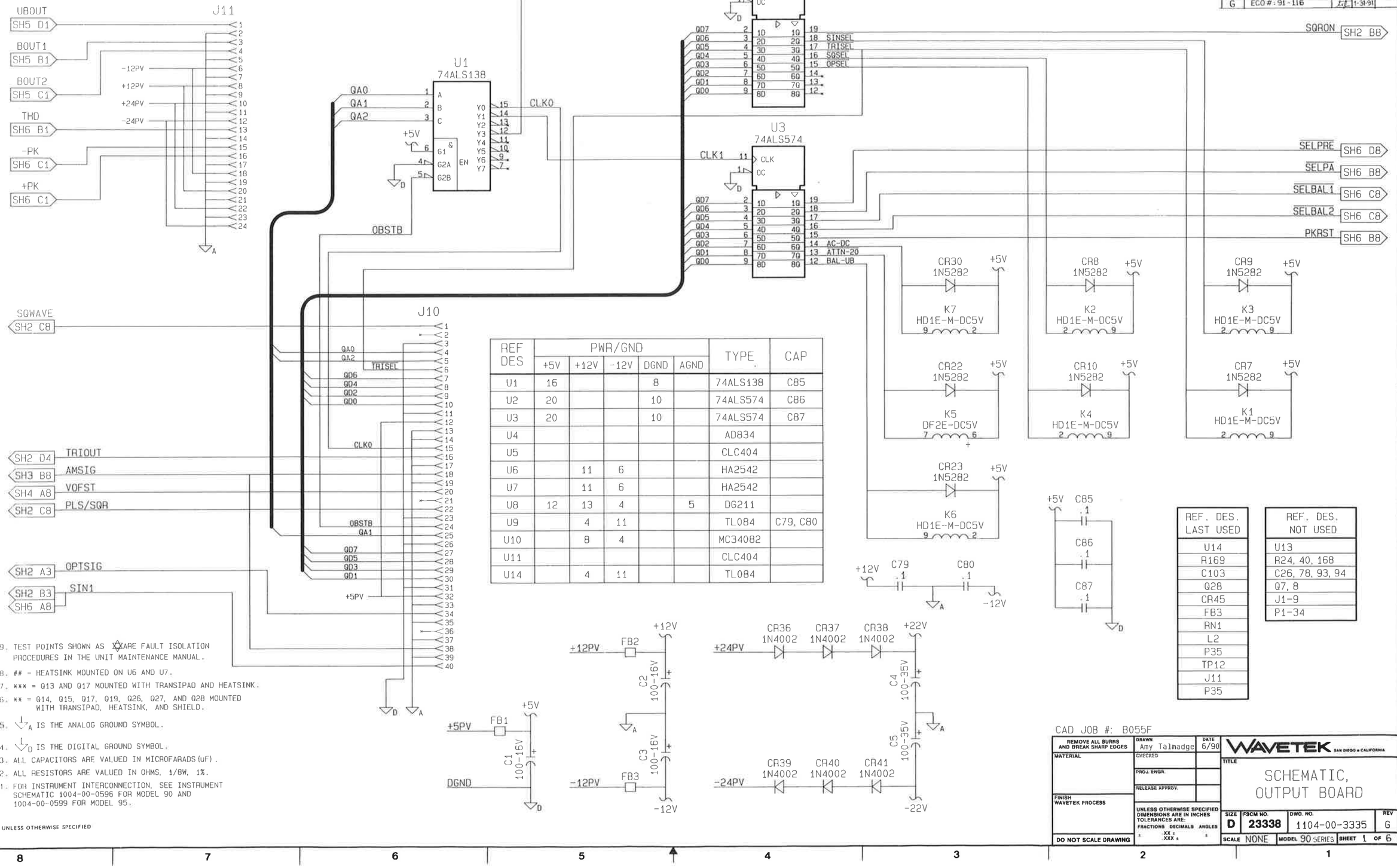
REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
U3 U5 U6 U7	FLIP-FLOP, OCTAL D	SN74ALS574N	TI	8007-45-7450	4

WAVETEK PARTS LIST	TITLE	ASSEMBLY NO.	REV
	PCA, DISPLAY/ KEYBOARD	1100-00-3322	C
		PAGE 3	

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	CHECKED		TITLE: PCA, DISPLAY KEYBOARD
	PROJ. ENGR.		
FINISH WAVETEK PROCESS	RELEASE APPROV.		
DO NOT SCALE DRAWING	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES .XX ±, .XXX ±, ±		SIZE D · FSCM NO. 23338 · DWG. NO. 1100-00-3322 · REV C · SCALE · MODEL 91 · SHEET 1 OF 1

REV	ECO	BY	DATE	APP
A	ERO NO. 90-441	A.P.	1/29/90	D.E.F.
B	ECO #: 90-476	A.T.	2/27/90	J.M.
C	ECO #: 90-497	A.T.	3-4-90	M.S.
D	ECO #: 90-530	A.T.	3-4-90	M.S.
E	ECO #: 90-557	A.T.	3-4-90	M.S.
F	ECO #: 91-040	A.T.	11-5-90	M.S.
G	ECO #: 91-116		1-31-91	



REF DES	PWR/GND +5V	+12V	-12V	DGND	AGND	TYPE	CAP
U1	16			8		74ALS138	C85
U2	20			10		74ALS574	C86
U3	20			10		74ALS574	C87
U4						AD834	
U5						CLC404	
U6		11	6			HA2542	
U7		11	6			HA2542	
U8	12	13	4		5	DG211	
U9		4	11			TL084	C79, C80
U10		8	4			MC34082	
U11						CLC404	
U14		4	11			TL084	

REF. DES. LAST USED
U14
R169
C103
Q28
CR45
FB3
RN1
L2
P35
TP12
J11
P35

REF. DES. NOT USED
U13
R24, 40, 168
C26, 78, 93, 94
Q7, 8
J1-9
P1-34

9. TEST POINTS SHOWN AS ✡ ARE FAULT ISOLATION PROCEDURES IN THE UNIT MAINTENANCE MANUAL.
8. ## = HEATSINK MOUNTED ON U6 AND U7.
7. *** = Q13 AND Q17 MOUNTED WITH TRANSIPAD AND HEATSINK.
6. ** = Q14, Q15, Q17, Q19, Q26, Q27, AND Q28 MOUNTED WITH TRANSIPAD, HEATSINK, AND SHIELD.
5. ⏚A IS THE ANALOG GROUND SYMBOL.
4. ⏚D IS THE DIGITAL GROUND SYMBOL.
3. ALL CAPACITORS ARE VALUED IN MICROFARADS (uF).
2. ALL RESISTORS ARE VALUED IN OHMS, 1/8W, 1%.
1. FOR INSTRUMENT INTERCONNECTION, SEE INSTRUMENT SCHEMATIC 1004-00-0596 FOR MODEL 90 AND 1004-00-0599 FOR MODEL 95.

NOTE UNLESS OTHERWISE SPECIFIED

CAD JOB #: B055F

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN Amy Talmadge	DATE 6/90
MATERIAL	CHECKED	
	PROJ. ENGR.	
	RELEASE APPROV.	
FINISH WAVETEK PROCESS	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES .XX ± .XXX ± °	
DO NOT SCALE DRAWING		

WAVETEK SAN DIEGO, CALIFORNIA

TITLE: SCHEMATIC, OUTPUT BOARD

SIZE	FSCM NO.	DWG. NO.	REV
D	23338	1104-00-3335	G

SCALE NONE | MODEL 90 SERIES | SHEET 1 OF 6

1104-00-3335 | G

REV	ECO	BY	DATE	APP

SQUARE SHAPER

FUNCTION SELECTOR

+12V
R7 4.75K
R9 100
R8 49.9
Q6 2N5771
Q5 2N3563
CR2 HP2811
R6 1.21K
C10 .1
R5 68.1
C11 22, 25V
C88 .1
C24 2.2, 25V TANT
SQR OFFSET
R158 500
R14 1.5K
R10 33.2
R11 220-1/2W-5%
R12 620-1/2W-5%
R13 220-1/2W-5%
-12V
CR3 HP2811
CR4 HP2811
CR5 HP2811
CR6 HP2811
R15 1.78K
R16T 59-NOM
C7 .1
MODEL 90
JP1
SQWAVE
SH1 C8
C6 22pF
CR1 HP2811
MODEL 91
JP2
PLS/SQR
SH1 B8
R1 100
Q1 2N3563
SQRON
SH1 D1
R3 2K
Q2 2N3904
R2 2K
C8 .1
Q3 2N4122
C25 2.2-25V TANT
Q4 2N3904
R4 1K
C9 22-25V
C89 .1
-12V
+6V
C90 .1
U11 CLC404
C91 .1
-6V
R38T 46.4, NOM
R139 499
C92T 5.1pF, NOM
R140 499
R138 33.2
R152T 499-NOM
R153T 499-NOM
2V p-p SQUARE
TP1
TRIOUT
SH1 B8
R17 100
R18 TRIM
C12T 47pF
R149 TRIM
R19 332
K1 HD1E-M-DC5V
PREAMPIN
SH3 C8
K2 HD1E-M-DC5V
SIN1
SH1 A8
R150T 576-NOM
R20 332
K3 HD1E-M-DC5V
OPTSIG
SH1 A8
R21T 332-NOM
R22 TRIM
R151 TRIM
R23 332
K4 HD1E-M-DC5V

NOTE UNLESS OTHERWISE SPECIFIED

CAD JOB #: B055F

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN Amy Talmadge	DATE 6/90	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	CHECKED		TITLE: SCHEMATIC, OUTPUT BOARD
	PROJ. ENGR.		
FINISH WAVETEK PROCESS	RELEASE APPROV.		
DO NOT SCALE DRAWING	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES XX ± XXX ± °		SIZE D; FSCM NO. 23338; DWG. NO. 1104-00-3335; REV G; SCALE NONE; MODEL 90 SERIES; SHEET 2 OF 6

1104-00-3335 G

REV	ECO	BY	DATE	APP

PREAMPLIFIER AND MULTIPLIER

+12V
R141 10K
U14/A TL084
R142 46.4
Q26 ** 2N2219A
C13 .1
C14 .1
C15 220-10V
R32 200
R34 100
R33 100
C23 .1
+6V
TP11
C29 10-25V
R159 33.2
Q22 2N3563
C95 .1
MULT FEED THRU
R25 2K
+6V
-6V
C20 .01
19
R161 68.1
Q23 2N5943
R160 681
PREAMPIN
SH2 D1
R26 10K
U4
AD834
+VS
Y1
Y2
X1
X2
-VS
W1
W2
R28 332
R175T 301K-NOM
AMSIG
SH1 B8
R27 1K
R143 20K
C19 56pF
R30 499
R29 75
R31 332
R35 10
R36 10
C21 .01
-6V
TP12
U14/D TL084
Q27 ** 2N2905
C17 .1
C18 220-10V
C22 .1
C30 10-25V
R144 20K
C16 .1
R148 46.4
-12V
R162 365-1W
C97 .1
+12V
R163 33.2
Q24 2N3563
C96 .1
R165 68.1
Q25 2N5943
R164 681
R166 365-1W
C98 .1
+6V
R167 24.9K
R169 35.7K
U14/B TL084
R154 10
CR43 1N5282
C28 100UF-10V TANT
+12V
CR11 1N4002
CR12 1N4002
C27 47uF-20V TANT
C100 3.9pF
R45 499
R42T 576
R43T 316
PREOUT
TP2
R37 68.1
U5 CLC404
FB6
R155 21.5
PREOUT
SH4 B8
R44 68.1
C101 47uF-20V TANT
R41 499
C102 47uF-20V TANT
ACOM
TP3
** Q28 2N2905
R46 681
-12V
CR44 1N5282
CR45 1N754A-6.8V
R137 20K
C103 .1
+12V
R128 10K
U14/C TL084
U12 LH0002CN
COMPOUT
SH4 B8
-12V
R147 2.21K
+12V
R145 100
-12V
20K R146
MULT OFFSET

NOTE UNLESS OTHERWISE SPECIFIED

CAD JOB #: B055F

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN Amy Talmadge	DATE 6/90	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	CHECKED		TITLE: SCHEMATIC, OUTPUT BOARD
	PROJ. ENGR.		
	RELEASE APPROV.		
FINISH WAVETEK PROCESS	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES .XX ±.1 .XXX ± °		SIZE D · FSCM NO. 23338 · DWG. NO. 1104-00-3335 · REV G
DO NOT SCALE DRAWING			SCALE NONE · MODEL 90 SERIES · SHEET 3 OF 6

1104-00-3335 G

REV	ECO	BY	DATE	APP

POWER AMP

+12V
C33 .1
R52 499
R53 499
CR13 1N5282
Q10 2N4122
C31 47pF
R54 249
Q11 2N2369A
Q9 MP312
R47 499
R48 49.9
R49 49.9
R51 499
R50 2.49K
C32 .1
-12V
R55 33.2
CR14 1N753A
C34 .01
R64 100
R65 33.2
C40 27UF-35V
C38 .01
C39 .01
R63 1.5K
FB9
Q12 2N5943
R67 100
C41 220pF
R66 39.2
CR46 1N4737
C104 .01
R69 500
C43 .1
R70 100
C42 220pF
Q13 *** SRF2573
C44 .1
R75 10-1/2W-5%
R76 10-1/2W-5%
C47 10-25V
C48 .1
+22V
C45 .01
C46 10-25V
R71 10
R72 10
Q15 ** 2N3866
Q14 ** 2N3866
PA_OUT
TP4
CR20 1N5282
PA_OUT
SH5 C8
SH6 C8
CR21 1N5282
-22V
ACOM
TP5
C36 .01
R62 1K-1/2W-5%
C37 .01
R79 1.69K-1/4W
R80 1.69K-1/4W
CR15 1N5282
CR16 1N5282
R73 10-1/2W-5%
R74 10-1/2W-5%
C49 .01
R77 23.7K
R78 1K-1/2W-5%
CR17 1N5282
CR18 1N5282
R88 10
CR19 1N5282
R91 10-1/2W-5%
R92 10-1/2W-5%
R89 10
Q18 ** 2N5160
R90 10
Q17 *** SRF2574
Q19 ** 2N5160
R170 15K
C26 120pF
R56 75
R57 75
PREOUT
SH3 C1
R39 294
COMPOUT
SH3 B1
L1 2.2mH
R58 464
R59 464
R60 499
R61 499
VOFST
SH1 B8
L2 2.2mH
C35 .01
Q16 2N5583
R81 1K
C50 .01
FB10
C51 .01
R82 100
R83 33.2
C52 27UF-35V
R84 100
C53 100pF
R86 100
C54 .1
R87 100
C55 100pF
R85 39.2
R93 10-1/2W-5%
R94 10-1/2W-5%
C59 .01
C60 10-25V
C58 10-25V
-22V
C56 .1
C57 .1
16
17

NOTE UNLESS OTHERWISE SPECIFIED

CAD JOB #: B055F

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN Amy Talmadge	DATE 6/90	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	CHECKED		TITLE: SCHEMATIC, OUTPUT BOARD
	PROJ. ENGR.		
	RELEASE APPROV.		
FINISH WAVETEK PROCESS	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES XX ± .XXX ±		SIZE D · FSCM NO. 23338 · DWG. NO. 1104-00-3335 · REV G
DO NOT SCALE DRAWING			SCALE NONE · MODEL 90 SERIES · SHEET 4 OF 6

REV	ECO	BY	DATE	APP

-20dB ATTENUATOR

PA_OUT
SH4 B1

R95 4.99K
R96 100-1W-.25%
R97 100-1W-.25%

K5
DF2E-DC5V

K5

R98 41.2K
R99 249-1/4W-.1%

R100 4.75K
R101 61.9-1W-.1%
R102 61.9-1W-.1%
R103 4.75K

R169T 61.9-NOM
C105T 47pF-NOM.

BALANCED DRIVERS

K6
HD1E-M-DC5V

18

UBOUT
SH1 D8

RN1/C 1K-2W

C62T 15pF
RN1/D 1K-2W
C81 .1
C61T 27pF-NOM.
+12V
U6 ## HA2542
V+ COMP V- BL1 BL2
C82 .1
-12V

RN1/B 1K-2W
RN1/A 1K-2W

TP6
CR24 1N5282
CR25 1N5282

BOUT2
SH6 D8
SH1 D8

RN1/G 1K-2W
C64 TRIM
RN1/H 1K-2W
C83 .1
C63 33pF
U7 ## HA2542
C84 .1
RN1/E 1K-2W
RN1/F 1K-2W

TP7
CR26 1N5282
CR27 1N5282

BOUT1
SH6 C8
SH1 D8

R104 100-1W-.25%
R105 100-1W-.25%
R106 12.1
R107 12.1
R108 12.1

NOTE UNLESS OTHERWISE SPECIFIED

CAD JOB #: B055F

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN Amy Talmadge	DATE 6/90	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	CHECKED		TITLE: SCHEMATIC, OUTPUT BOARD
	PROJ. ENGR.		
FINISH WAVETEK PROCESS	RELEASE APPROV.		SIZE D · FSCM NO. 23338 · DWG. NO. 1104-00-3335 · REV G
DO NOT SCALE DRAWING	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES XX ± .XXX ± °		SCALE NONE · MODEL 90 SERIES · SHEET 5 OF 6

1104-00-3335 G

REV	ECO	BY	DATE	APP

PEAK DETECTOR

AMSIG (SH3 B1) → R109 1K → U8/A DG211 (3, 2, 1)
SELPRE (SH1 C1) → R110 2.49K → C65 .1 → A
BOUT2 (SH5 C1) → R111 1K → U8/B DG211 (6, 7, 8)
SELBAL2 (SH1 C1) → R112 2.49K → C66 .1 → A
BOUT1 (SH5 B1) → R113 1K → U8/C DG211 (11, 10, 9)
SELBAL1 (SH1 C1) → R114 2.49K → C67 .1 → A
PA_OUT (SH4 B1) → R115 2K-.1% → U8/D DG211 (14, 15, 16)
R116 1K-.1% → A
OPTDRV P35 → R134 0 → A
SELPA (SH1 C1) → R117 2.49K → C68 .1 → A
PKRST (SH1 C1)

U8/A DG211 → U9/A TL084 (3, 2, 1)
CR28 1N5282
CR35 1N5282
C69 .1-PP → A
R118 10M → A
R156 10K
U9/D TL084 (12, 13, 14)
K7 HD1E-M-DC5V (10, 5, 1)
+PK TP9
+PK SH1 C8

R119 10K
Q20 2N3904
Q21 2N4122 → A

U8/B DG211 → U9/B TL084 (5, 6, 7)
CR29 1N5282
CR42 1N5282
C70 .1-PP → A
R120 10M → A
R157 10K
U9/C TL084 (10, 9, 8)
-PK TP10
-PK SH1 C8

+12V
R131 16.5K
R132 1K
CR32 1N5282
CR31 1N5282 → A
CR33 1N5282
THD SH1 D8

C71 910pF-SM-1%
C72 910pF-SM-1%
R121 17.8K → A
R122 17.8K → A
C75 1.5pF
THD TP8
R127 499K
R129 28.7K
C76 .1
C77 .1 → A
R133 47.5K → A
CR34 1N751A → A

SIN1 (SH1 A8) → U10/B 34082 (5, 6, 7)
R123 6.19K
R124 17.8K
R125 17.8K
R126 6.19K
C73 910pF-SM-1% → A
C74 910pF-SM-1% → A
R135 4.99K → A
R136 1K → A
U10/A 34082 (2, 3, 1)
R130 4.99K

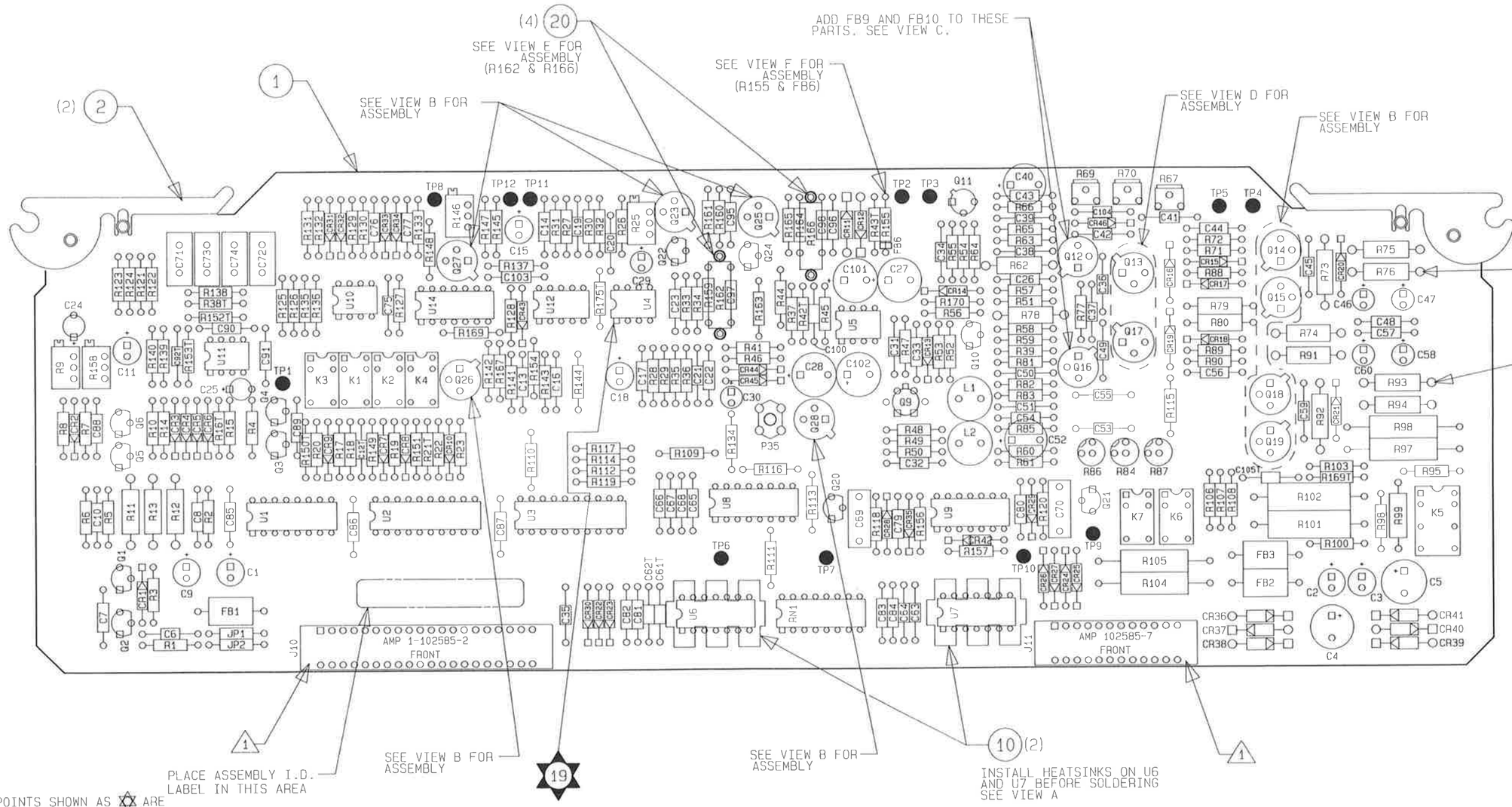
NOTE UNLESS OTHERWISE SPECIFIED

CAD JOB #: B055F

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN Amy Talmadge	DATE 6/90	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	CHECKED		TITLE: SCHEMATIC, OUTPUT BOARD
	PROJ. ENGR.		
FINISH WAVETEK PROCESS	RELEASE APPROV.		
DO NOT SCALE DRAWING	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES .XX ± .XXX ± °		SIZE D · FSCM NO. 23338 · DWG. NO. 1104-00-3335 · REV G · SCALE NONE · MODEL 90 SERIES · SHEET 6 OF 6

1104-00-3335 G

REV	ECO	BY	DATE	APP
B	ERO NO. 90-453	AT	7/30/90	M.S.
C	ECO #: 90-530	AT	9/5/90	M.S.
D	ECO NO. 90-557	AT	9/5/90	M.S.
E	ECO NO. 91-040	AT	11/5/90	M.S.
F	ECO #: 91-116	AT	2/1/91	



6. TEST POINTS SHOWN AS ✡ ARE FAULT ISOLATION PROCEDURES IN THE UNIT MAINTENANCE MANUAL.
5. ASSEMBLE PER WAVETEK WORKMANSHIP STANDARDS.
4. REFERENCE DESIGNATIONS DO NOT APPEAR ON PARTS.
3. FOR ASSEMBLY INTERCONNECTION, SEE INSTRUMENT SCHEMATIC.
2. SEE 1104-00-3335 FOR SCHEMATIC.
1. MANUFACTURER'S MARKING INDICATES CORRECT ORIENTATION OF CONNECTOR.

NOTE UNLESS OTHERWISE SPECIFIED

CAD JOB #: B055F

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN: Amy Talmadge	DATE
MATERIAL	CHECKED	
	PROJ. ENGR.	
	RELEASE APPROV.	
FINISH: WAVETEK PROCESS	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. TOLERANCES ARE: FRACTIONS DECIMALS ANGLES XX ± XXX ±	
DO NOT SCALE DRAWING		

WAVETEK SAN DIEGO, CALIFORNIA

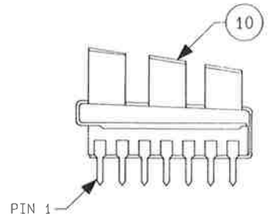
TITLE: PCA, OUTPUT BOARD

SIZE	FSCM NO.	DWG. NO.	REV
D	23338	1101-00-3335	F

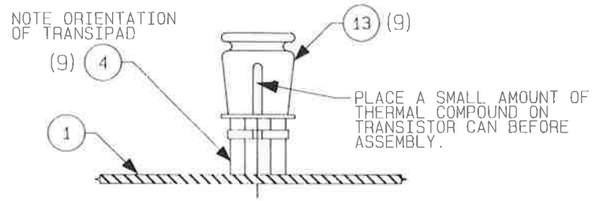
SCALE 2/1 | MODEL 90 SERIES | SHEET ___ OF ___

1101-00-3335 F

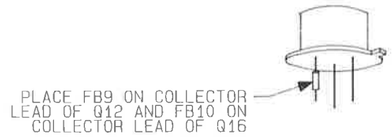
REV	ECO	BY	DATE	APP



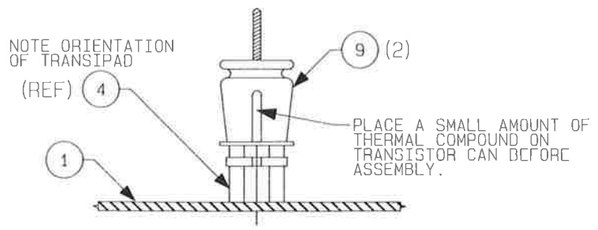
VIEW A
SCALE: NONE



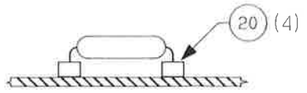
VIEW B
SCALE: NONE



VIEW C
SCALE: NONE



VIEW D
SCALE: NONE



VIEW E
SCALE: NONE

VIEW F
SCALE: NONE

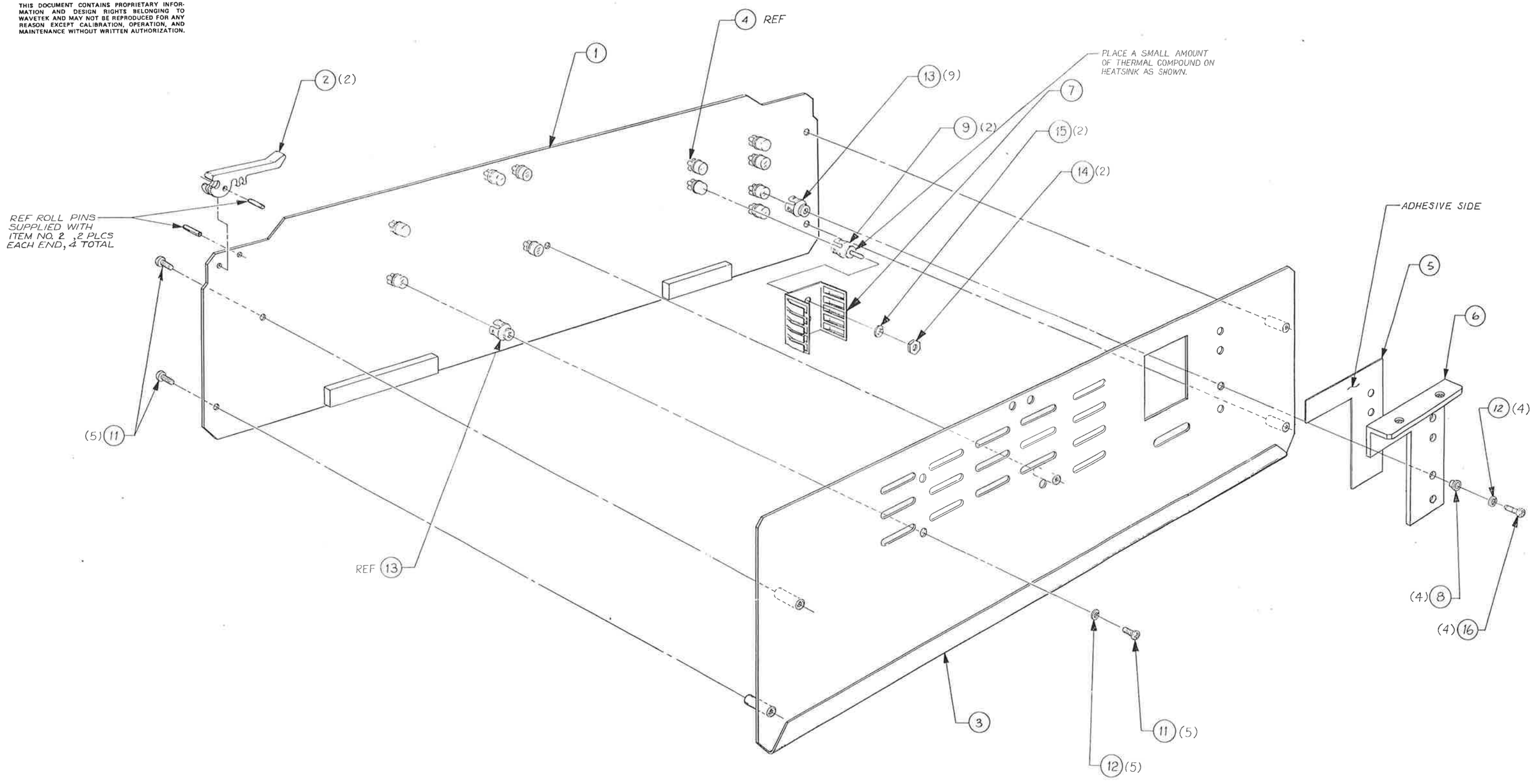
NOTE UNLESS OTHERWISE SPECIFIED

CAD JOB #: B055F

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN: Amy Talmadge	DATE: 7/90	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	CHECKED		TITLE: PCA, OUTPUT BOARD
	PROJ. ENGR.		
FINISH WAVETEK PROCESS	RELEASE APPROV.		
DO NOT SCALE DRAWING	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES XX ± XXX ±		SIZE: D · FSCM NO.: 23338 · DWG. NO.: 1101-00-3335 · REV: F · SCALE: NONE · MODEL: 90 SERIES · SHEET 2 OF 3

1101-00-3335 F

REV	ECN	BY	DATE	APP



NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN S.C / A.T.	DATE 7/90	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJENGR	7/90	TITLE PCA, OUTPUT BOARD
	RELEASE APPROV	7/90	
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1° XX ±.030		
	DO NOT SCALE DWG		MODEL NO. 90 SERIES · DWG NO. 1101-00-3335 · REV H
	SCALE NONE		CODE IDENT 23338 · SHEET 3 OF 3

REV	ECO	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
11	SCREWB 4-40 X 3/16	0202-00314	R.Q.	0202-00314	10
CR46	DIODE ZENER, 1N4737 1W 7.5V 10%	1N4737A	MOT	0374-00082	1
R162 R166	RES, MF, 1/2W, 1%, 365 OHM	RN65D3650F	DALE	0588-03650	2
REF	MODEL 90 SUB-ASY FUNCTION TEST PROCESS	1008-00-0596-1	WVTK	1008-00-0596	1
NONE	A/D, OUTPUT BOARD	1101-00-3335	WVTK	1101-00-3335	1
NONE	SCHEMATIC, OUTPUT BD	1104-00-3335	WVTK	1104-00-3335	1
U12	U: CURRENT AMP, 100MA	LH0002CN	NSC	120.1022	1
CR14	SL ZR 6.2V 5% 400MW (1N753A)	1N753A	ROHM	131.9620	1
3	SHIELD, OUT PUT BOARD	1400-02-5066	WVTK	1400-02-5066	1
6	HEAT SINK, OUT PUT BOARD	1400-02-5067	WVTK	1400-02-5067	1
5	THERMAL GASKET, OUT PUT BOARD	1400-02-5068	WVTK	1400-02-5068	1
7	HEAT SINK, MODIFICATION	1400-02-5085	WVTK	1400-02-5085	1
C53 C55	CAP, CER, 100PF, 100V, AXIAL	CAC02CG0101J100A(OBS)	CORNG	1500-01-0106	2

WAVETEK PARTS LIST | TITLE: PCA, OUTPUT BOARD | ASSEMBLY NO.: 1100-00-3335 | REV: AA

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
C104 C20 C21 C34 C35 C36 C38 C39 C45 C49 C50 C51 C59	CAP CER MON .01MF 50V, AXIAL	CAC02Z5U103Z100A	CORNG	1500-01-0310	13
C10 C103 C13 C14 C16 C17 C22 C23 C32 C33 C37 C43 C44 C48 C54 C56 C57 C65 C66 C67 C68 C7 C76 C77 C79 C8 C80 C81 C82 C83 C84 C85 C86 C87 C88 C89 C90 C91 C95 C96 C97 C98	CAP, CER, MON, .1MF, 50V, AXIAL	CAC03Z5U104Z050A	CORNG	1500-01-0405	42
C26	CAP, CER, 120PF 200V 5% AXIAL	SA102A121JAA	AVX	1500-01-2106	1
C62T	CAP, CER, 15PF, 100V, AXIAL	CAC02CG150J100A	CORNG	1500-01-5006	1
C75	CAP, CER, 1.5PF, 200V, AXIAL	SA102A1R5DAA	AVX	1500-01-5906	1
C41 C42	CAP, CER, 220PF, 100V, AXIAL	CAC02CG221J100A	CORNG	1500-02-2106	2
C61T	CAP, CER, 27PF, 5%, COG, 100V, AXIAL	CAC02CG270J100A	CORNG	1500-02-7006	1
C63T	CAP CER 33PF 200V 5% AXIAL	CAC02CD330J100A(OBS)	CORNG	1500-03-3006	1
C100T C92T	CAP, CERAMIC, 3.9PF +.5PF, 200V AXIAL.	C114C399D2G5CA	KEMET	1500-03-9906	2

WAVETEK PARTS LIST | TITLE: PCA, OUTPUT BOARD | ASSEMBLY NO.: 1100-00-3335 | REV: AA

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
C105T C12 C6	CAP CER 47PF 200V 5% AXIAL	CAC02CG047OJ100A(OBS)	CORNG	1500-04-7006	3
C19	CAP, CER, 56PF, 100V, 5%, AXIAL	CAC02CG560J100A	CORNG	1500-05-6000	1
C31	CAP, CER, 82PF, 100V, 5%, COG, AXIAL	SA102A820JAA	AVX	1500-08-2006	1
C71 C72 C73 C74	CAP, MICA, 910PF, 100V, 1%, RADIAL	DM15-911F	ARCO	1500-19-1101	4
C29 C30 C46 C47 C58 C60	CAP, ELECT, 10MF/25V RADIAL LEAD, BP .10	NRE 10/63	NIC	1500-31-0002	6
C4 C5	CAP, ELECT, 100MF, 35V RADIAL LEAD, BP .20	NRE101M35V10X12.5	NIC	1500-31-0102	2
C1 C2 C3	CAP, ELECT, 100MF/16V RADIAL LEAD, BP .20	NRE101M16V6.3X11	NIC	1500-31-0111	3
C15 C18	CAP, ELECT, 220MF/10V	ECEA1AU221	PANAS	1500-32-2001	2
C11 C9	CAP, ELECT, 22MF, 25V, RADIAL	SRA25VB22RM6X7LL	UNCON	1500-32-2002	2
C69 C70	COG CAP, MET POLY, .1MF, 100V/160V DC, .4 LS	171104J160D	MALRY	1500-41-0434	2
C28	CAP, TANT, 100MF, 10V	199D107X9010EE4	SPRAG	1500-71-0711	1
C24 C25	CAP, TANT, 2.2MF, 25V	199D225X9025AA2	SPRAG	1500-72-2502	2

WAVETEK PARTS LIST | TITLE: PCA, OUTPUT BOARD | ASSEMBLY NO.: 1100-00-3335 | REV: AA

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
C40 C52	CAP, TANT 27UF, 35V+/-10%, 0.25LS	199D276X9035FE4	SPRAG	1500-72-7602	2
C101 C102 C27	CAP, TANT, 47MF, 20V	196D476X9020PE4(OBS)	SPRAG	1500-74-7601	3
1	PCB, OUTPUT BOARD	1700-00-3335	WVTK	1700-00-3335	1
L1 L2	INDUCTOR, 2.2 MHY, 40MA, RADIAL	181LY-222J	TOKO	1800-00-0046	2
J11	CONN, HEADER, 24 PIN, RECPT, 2X12, .1 CTR, PCMT	102585-7	AMP	2100-02-0255	1
J10	CONN, HEADER, 40 PIN, RECPT, 2X20, .1 CTR PCMT	1-102585-2	AMP	2100-02-0256	1
TP3 TP5	TEST POINT, BLK, PC	TP-104-01-00	COMPO	2100-04-0054	2
TP1 TP10 TP11 TP12 TP2 TP4 TP6 TP7 TP8 TP9	TEST POINT, RED, PC	TP-104-01-02	COMPO	2100-04-0055	10
P35	CONN, SUB MIN	27-848	AMPH	2100-07-0011	1
20	SPACER, COMP, MUNTING, .085OD, .032ID, .300LG	938.300"	BIVAR	2800-04-0024	4
2	PC BD EJECTOR	87-2-C	BRIT	2800-07-0032	2
4	TRANSIPAD	531-218	BIVAR	2800-11-0004	11

WAVETEK PARTS LIST | TITLE: PCA, OUTPUT BOARD | ASSEMBLY NO.: 1100-00-3335 | REV: AA

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
9	HEATSINK	2606SH5E	WAKE	2800-11-0012	2
8	WASHER	5607-150	SEBTM	2800-11-0015	4
13	HEATSINK, TO5, EPOXY INS	260-4T5E	WAKE	2800-11-0031	9
10	HEATSINK, 14-16 PIN DIP, ALUM, BLK AN, CLIPON	5802B	AAVID	2800-11-0034	2
14	NUT, HEX, 6-32, Z	MS35649-264	COML	2800-14-6100	2
22	WASHER, SHOULDER, #4 CLEARANCE, NYLON .030 THK, .030 SHOULDER	5607-45	SEA	2800-27-0011	2
24	SCREW, 4-40X3/16 PHP, Z 4-40 X 3/16	4-40X3/16 PLPS PAN	CMRCL	2800-38-4103	5
12	WASHER, LOCK REQ, S/S #4	MS 35338-135	CMRCL	2800-45-4000	9
15	WASHER, LOCK, REQ S/S #6	MS 35338-136	CMRCL	2800-45-6000	2
16	SCREW PLPS PAN M/S 18-8 S/S 4-40X3/8	MS 51957-15	CMRCL	2800-48-4106	4
FB6	FERRITE BEAD	56-590-65/3B	FERRX	3100-00-0001	1
FB1 FB2 FB3	BALUN CORE, FERRITE, 680 OHMS	2943666671	FARIT	3100-00-0017	3

WAVETEK PARTS LIST | TITLE: PCA, OUTPUT BOARD | ASSEMBLY NO.: 1100-00-3335 | REV: AA

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
23	INSULATOR, THERMAL, SELF ADHESIVE .510 OD x .140 ID, .009 THK	7403-09AC-19	BERGQ	3100-00-0022	2
K5	RELAY, 2 FORMC, 5V, DIP 14	DF2E-DC5V	AROMT	4500-00-0033	1
K1 K2 K3 K4 K6 K7	RELAY, 1 FORMC, 5V, .312H, .296W	HD1E-M-DC5V	AROMT	4500-00-0034	6
R84 R86 R87	POT, TRIM, 100	3329H-1-101	BOURN	4600-01-0100	3
R67 R70	POT, 1 TURN, SIDE TRIM, 1/4" DIA, 100ohm	3329W-1-101	BOURN	4601-01-0101	2
R69	POT, 1 TURN, SIDE TRIM, 1/4" DIA, 500 OHM	3329W-1-501	BOURN	4601-01-0500	1
R25	POT, SIDE TRIM, 20T, 2K	68XR2K	BECK	4609-90-0010	1
R146	POT, SIDE TRIM, 20T, 20K	68XR20K	BECK	4609-90-0011	1
R158	POT, SIDE TRIM, 20T, 500	68XR500	BECK	4609-90-0014	1
R9	POT, SIDE TRIM, 20T, 100	68XR100	BECK	4609-90-0017	1
R73 R74 R75 R76 R91 R92 R93 R94	RES, C, 1/2W, 5%, 10	RC-1/2-10J	STKPL	4700-25-0100	8
R62 R78	RES, C, 1/2W, 5%, 1K	RC-1/2-102J	STKPL	4700-25-1001	2
R11 R13	RES, C, 1/2W, 5%, 220	RC-1/2-221J	STKPL	4700-25-2200	2

WAVETEK PARTS LIST | TITLE: PCA, OUTPUT BOARD | ASSEMBLY NO.: 1100-00-3335 | REV: AA

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE
MATERIAL	CHECKED	
	PROJ. ENGR.	
FINISH WAVETEK PROCESS	RELEASE APPROV.	
DO NOT SCALE DRAWING	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES °	

WAVETEK SAN DIEGO, CALIFORNIA

TITLE: PCA OUTPUT BOARD

SIZE	FSCM NO.	DWG. NO.	REV
D	23338	1100-00-3335	AA

SCALE | MODEL 91 | SHEET 1 OF 2

REV	ECO	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R12	RES, C, 1/2W, 5%, 620	RC-1/2-621J	STKPL	4700-25-6200	1
R116	RES, MF, 1/8W, 1%, 1K	RN55E-1001B	MEPCO	4701-02-1001	1
R115	RES, MF, 1/8W, 1%, 2K	RN55E-2001B	MEPCO	4701-02-2001	1
R1 R145 R17 R33 R34 R64 R82	RES, MF, 1/8W, 1%, 100	RN55D-1000F	TRW	4701-03-1000	7
R109 R111 R113 R132 R136 R27 R4 R81	RES, MF, 1/8W, 1%, 1K	RN55D-1001F	TRW	4701-03-1001	8
R119 R128 R141 R144 R156 R157 R26	RES, MF, 1/8W, 1%, 10K	RN55D-1002F	TRW	4701-03-1002	7
R118 R120	RES, MF, 1/4W, 10M, 1%	5053YD10M000F	MEPCO	4701-03-1005	2
R154 R35 R36 R71 R72 R88 R89 R90	RES, MF, 1/8W, 1%, 10	5043ED10R100F	MEPCO	4701-03-1009	8
R6	RES, MF, 1/8W, 1%, 1.21K	RN55D-1211F	TRW	4701-03-1211	1
R106 R107 R108	RES, MFLM, 1/8W, 1%, 12.1	5033RD12R1F	MEPCO	4701-03-1219	3
R14 R63	RES, MF, 1/8W, 1%, 1.5K	RN55D-1501F	TRW	4701-03-1501	2
R131	RES, MF, 1/8W, 1%, 16.5K	RN55D-1652F	TRW	4701-03-1652	1
R15	RES, MF, 1/8W, 1%, 1.78K	RN55D-1781F	TRW	4701-03-1781	1
R121 R122 R124 R125	RES, MFLM, 1/8W, 1%, 17.8K	5033RD1782F	MEPCO	4701-03-1782	4

WAVETEK PARTS LIST | TITLE: PCA, OUTPUT BOARD | ASSEMBLY NO. 1100-00-3335 | REV AA

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R66 R85	RES, MF, 1/8W, 1%, 39.2	RN55D-39R2F	TRW	4701-03-3929	2
R98	RES, MF, 1/8W, 1%, 41.2K	RN55D-4122F	TRW	4701-03-4122	1
R58 R59	RES, MF, 1/8W, 1%, 464	RN55D-4640F	TRW	4701-03-4640	2
R142 R148	RES, MF, 1/8W, 1%, 46.4	RN55D-46R4F	TRW	4701-03-4649	2
R100 R103 R7	RES, MF, 1/8W, 1%, 4.75K	RN55D-4751F	TRW	4701-03-4751	3
R133	RES, MF, 1/8W, 1%, 47.5K	RN55D-4752F	TRW	4701-03-4752	1
R139 R140 R152 R153 R30 R41 R45 R47 R51 R52 R53 R60 R61	RES, MF, 1/8, 1%, 499	RN55D-4990F	TRW	4701-03-4990	13
R130 R135 R95	RES, MF, 1/8W, 1%, 4.99K	RN55D-4991F	TRW	4701-03-4991	3
R127	RES, MF, 1/8W, 1%, 499K	RN55D-4993F	TRW	4701-03-4993	1
R48 R49 R8	RES, MF, 1/8W, 1%, 49.9	RN55D-49R9F	CORNG	4701-03-4999	3
R38	RES, MF, 1/8W, 1%, 54.9	RN55D-54R9F	TRW	4701-03-5499	1
R150 R42	RES, MF, 1/8W, 1%, 576	RN55D-5760F	TRW	4701-03-5760	2
R16	RES, MF, 1/8W, 1%, 59	RN55D-59R0F	TRW	4701-03-5909	1
R123 R126	RES, MF, 1/8W, 1%, 6.19K	RN55D-6191F	TRW	4701-03-6191	2
R169T	RES, MF, 1/8W, 1%, 61.9	RN55D-61R9F	TRW	4701-03-6199	1
R160 R164 R46	RES, MF, 1/8W, 1%, 681	RN55D-6810F	TRW	4701-03-6810	3

WAVETEK PARTS LIST | TITLE: PCA, OUTPUT BOARD | ASSEMBLY NO. 1100-00-3335 | REV AA

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
CR11 CR12 CR36 CR37 CR38 CR39 CR40 CR41	DIODE, 1N4002 GEN PURPOSE RECT, 100V, 1A	1N4002	FAIR	4801-02-0001	8
CR1 CR2 CR3 CR4 CR5 CR6	DIODE 5082-2811 SCHOTTKY, 15V, 20MA	5082-2811	HP	4809-02-2811	6
Q26	TRANS 2N2219A NPN GENERAL PURPOSE TO-5	2N2219A	NSC	4901-02-2191	1
Q11	TRANS, SILICON, PLANAR, EPITAXIAL, NPN, TO-18	2N2369A	MOT	4901-02-3691	1
Q27 Q28	TRANS 2N2905A PNP GENERAL PURPOSE TO-5	2N2905A	NSC	4901-02-9051	2
Q1 Q12 Q22 Q24 Q5	TRANS, NPN, TO-92	2N3563	FAIR	4901-03-3630	5
Q14 Q15	TRANS	2N3866	MOT	4901-03-8660	2
Q2 Q20 Q4	TRANS 2N3904 NPN GENERAL PURPOSE TO-92	2N3904	FAIR	4901-03-9040	3
Q10 Q21 Q3	TRANS, GENERAL PURPOSE, PNP, TO-92	PN4122	NSC	4901-04-1220	3
Q18 Q19	TRANS	2N5160-18(OBS)	MOT	4901-05-1600	2
Q16 Q6	TRANS 2N5771 PNP SWITCH TO-92	2N5771	NSC	4901-05-7710	2
Q23 Q25	TRANS, NPN, HIGH FREQ	2N5943	MOT	4901-05-9430	2

WAVETEK PARTS LIST | TITLE: PCA, OUTPUT BOARD | ASSEMBLY NO. 1100-00-3335 | REV AA

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R32	RES, MF, 1/8W, 1%, 200	RN55D-2000F	TRW	4701-03-2000	1
R2 R3	RES, MF, 1/8W, 1%, 2K	RN55D-2001F	TRW	4701-03-2001	2
R137 R143	RES, MF, 1/8W, 1%, 20K	RN55D-2002F	TRW	4701-03-2002	2
R155	RES, MF, 1/8W, 1%, 21.5	RN55D-21R5F	TRW	4701-03-2159	1
R147	RES, MF, 1/8W, 1%, 2.21K	RN55D-2211F	TRW	4701-03-2211	1
R77	RES, MF, 1/8W, 1%, 23.7K	RN55D-2372F	TRW	4701-03-2372	1
R54	RES, MF, 1/8W, 1%, 249	RN55D-2490F	TRW	4701-03-2490	1
R110 R112 R114 R117 R50	RES, MF, 1/8W, 1%, 2.49K	RN55D-2491F	TRW	4701-03-2491	5
R167	RES, MF, 1/8W, 1%, 24.9K	RN55D-2492F	TRW	4701-03-2492	1
R129	RES, MF, 1/8W, 1%, 28.7K	RN55D-2872F	TRW	4701-03-2872	1
R39	RESISTOR, METAL FILM, 1/8W, 1%, 294 OHM.	5043ED294R0F	MEPCO	4701-03-2940	1
R175	RES, MF, 1/8W, 1%, 301K	RN55D-3013F	TRW	4701-03-3013	1
R43	RES, MF, 1/8W, 1%, 316	RN55D-3160F	TRW	4701-03-3160	1
R19 R21 R23 R28 R31	RES, MF, 1/8W, 1%, 332	RN55D-3320F	TRW	4701-03-3320	5
R10 R138 R159 R163 R55 R65 R83	RES, MF, 1/8W, 1%, 33.2	RN55D-33R2F	TRW	4701-03-3329	7
R169	RES, MF, 1/8W, 1%, 35.7K	RN55D-3572F	TRW	4701-03-3572	1

WAVETEK PARTS LIST | TITLE: PCA, OUTPUT BOARD | ASSEMBLY NO. 1100-00-3335 | REV AA

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R161 R165 R37 R44 R5	RES, MF, 1/8W, 1%, 68.1	RN55D-68R1F	TRW	4701-03-6819	5
R29 R56 R57	RES, MFLM, 1/8W, 1%, 75	5033RD75R0F	MEPCO	4701-03-7509	3
R170	RES, MF, 1/8W, 1%, 9.53K	RN55D-9531F	TRW	4701-03-9531	1
R99	RES, MFLM, 1/4W, 1%, 249	5043RE2490B	MEPCO	4701-12-2490	1
R101 R102	RES, MFLM, 1W, 1%, 61.9	5053RE61R9B	MEPCO	4701-32-6199	2
R79 R80	RES, MF, 1/4W(1/2W@70 C), 1%, 1.69K ohm	5053HD1K690F	MECEN	4701-33-1691	2
R104 R105 R96 R97	RES, MF, 1W, .25%, T2 100	5053RC100R0C	MEPCO	4701-38-1000	4
RN1	RES NETWORK 1K 2W 16PIN DIP	4116R-001-102	BOURN	4770-00-0019	1
JP1 R134 R20	RES, 0 OHM JUMPER	JP02T6BQ	ROHM	4799-00-0087	3
CR34	DIODE, ZENOR, 5.1V, 500MW, QIB, IN751A	1N751A	FAIR	4801-01-0751	1
CR45	DIODE, ZENER, 6.8V	1N754A	MOT	4801-01-0754	1
CR10 CR13 CR15 CR16 CR17 CR18 CR19 CR20 CR21 CR22 CR23 CR24 CR25 CR26 CR27 CR28 CR29 CR30 CR31 CR32 CR33 CR35 CR42 CR43 CR44 CR7 CR8 CR9	DIODE, HIGH CONDUCTANCE, ULTRA FAST	1N5282	FAIR	4801-01-5282	28

WAVETEK PARTS LIST | TITLE: PCA, OUTPUT BOARD | ASSEMBLY NO. 1100-00-3335 | REV AA

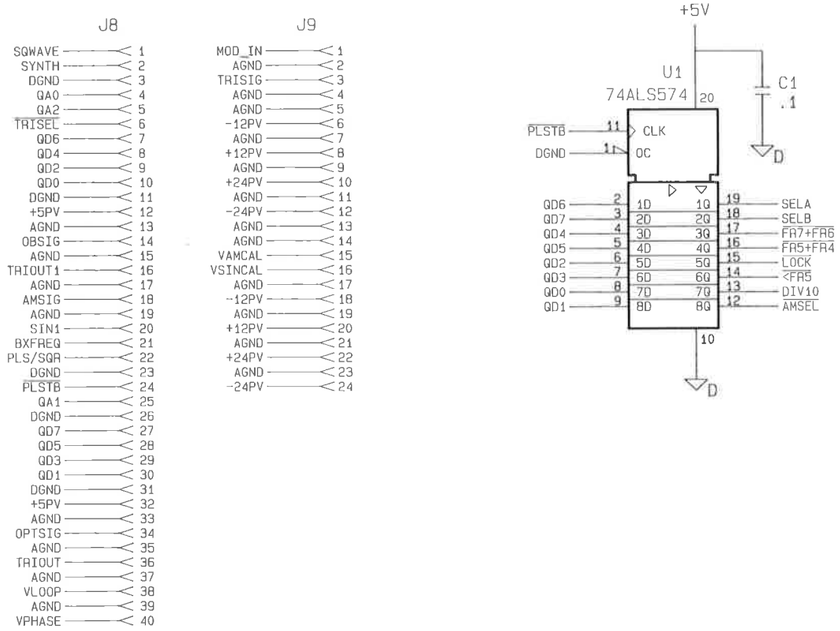
REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
Q13	TRANS	4902-02-5730	WVTK	4902-02-5730	1
Q17	TRANS	4902-02-5740	WVTK	4902-02-5740	1
U14 U9	OP AMP, QUAD BIMOS MOS/FET INPUT	TL084CN	TI	7000-00-8400	2
U11 U5	WIDWBAND HIGH SLEW RATE OP AMP	CLC404AJP	COMLR	7000-04-0410	2
G9	TRANS, MONO, DUAL, NPN SUBSTITUTE FOR 7000-08-1100}REPLACEMENT FOR 7000-08-1100	LS312-52	LINSY	7000-08-1200	1
U4	MULTIPLIER, ANALOG, WIDEBAND	AD834JN	ANDEV	7000-08-3410	1
U6 U7	OP AMP, WIDEBND, HI SLRTE, HI OUT	HA3-2542-5	HARIS	7000-25-4200	2
U10	OP AMP, HI SLEW RTE, WIDEBND, JFET DUAL	MC34082P	MOT	7003-40-8200	1
U8	SW, QUAD ANALOG, CMOS	DG211CJ	SLCON	8000-02-1100	1
U1	DECODER/DEMUX, 3 TO 8 LINE	SN74ALS138N	TI	8007-41-3800	1
U2 U3	FLIP-FLOP, OCTAL D	SN74ALS574N	TI	8007-45-7450	2

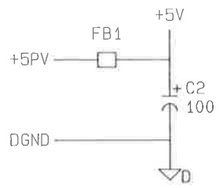
WAVETEK PARTS LIST | TITLE: PCA, OUTPUT BOARD | ASSEMBLY NO. 1100-00-3335 | REV AA

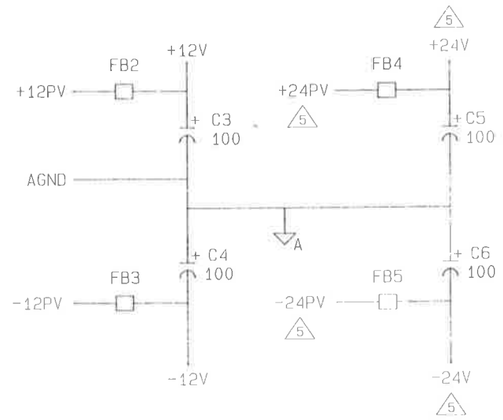
NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	CHECKED		TITLE: PCA OUTPUT BOARD
	PROJ. ENGR.		
FINISH WAVETEK PROCESS	RELEASE APPROV.		
DO NOT SCALE DRAWING	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS ± / DECIMALS .XX ± .XXX ± / ANGLES ±		SIZE D · FSCM NO. 23338 · DWG NO. 1100-00-3335 · REV AA · SCALE · MODEL 91 · SHEET 2 OF 2

REV	ECO	BY	DATE	APP
A	ECO 10-[illegible] CCS 2 FROM: 1104-00-334	[illegible]	[illegible]	[illegible]
B	ECO"91-121	RA	3/91	[illegible]







6. ♦ = MATCHED DIODE SET 4898-00-0015.
5. ⏚A = ANALOG GROUND SYMBOL.
4. ⏚D = DIGITAL GROUND SYMBOL.
3. ALL CAPACITORS ARE IN MICROFARADS (uF).
2. ALL RESISTORS ARE IN OHMS, 1/8W, 1%, MF.
1. FOR ASSEMBLY INTERCONNECTION, SEE INSTRUMENT SCHEMATIC.

NOTE UNLESS OTHERWISE SPECIFIED

CAD JOB #: B0630

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN A.C.T.	DATE 7/90	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	CHECKED [illegible]	9/4/90	TITLE SCHEMATIC, PHASE LOCK LOOP
	PROJ. ENGR.		
	RELEASE APPROV. [illegible]	10/19/90	
FINISH WAVETEK PROCESS	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES . .XX . .XXX .		SIZE D · FSCM NO. 23338 · DWG NO. 1104-00-3437 · REV B
DO NOT SCALE DRAWING			SCALE NONE · MODEL 90 SERIES · SHEET 1 OF 6

REV	ECO	BY	DATE	APP

SINE/TRI Z-CROSS

ZCSIG F04 B1
R1 301
R4 392
R2 200
R3 2.49K
U2 LT1016CN8
C8 .1
C11 4.7 50V
C9 .1
C12 4.7
R154 15 +5V
TP4 DGND
TP1 Z-CROSS
TP2 BXFREQ
TP3 SYNTH
R5 681
CR20 1N751A
C10 .1 -12V
R82 4.99K
R155 392
CR19 1N5282
CR18 1N5282

BXFREQ F01 C7
SYNTH F01 C7
SQWAVE F01 C7
PLS/SQR F01 C7
SELA F01 C5
SELB F01 C5

SOURCE SELECTOR

+5V
C13 .1
U3 74ALS253
LOCK C5 F01

U4B 74LS390
U4A 74LS390
C14 .1
FB7
R8 4.7 1/4W
C15 .1
DIV10 C5 F01
U5
VLEADR C8 F03
VLAGR B8 F03

PHASE COMPARATOR

NOTE UNLESS OTHERWISE SPECIFIED

CAD JOB #: B063C

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN A.C.T.	DATE 7/90	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	CHECKED JM	7/2/90	TITLE: SCHEMATIC, PHASE LOCK LOOP
	PROJ. ENGR.		
FINISH WAVETEK PROCESS	RELEASE APPROV.		
DO NOT SCALE DRAWING	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES XX.; XXX ;		SIZE D · FSCM NO. 23338 · DWG. NO. 1104-00-3437 · REV G · SCALE NONE · MODEL 90 SERIES · SHEET 2 OF 6

1104-00-3437 G

REV	ECO	BY	DATE	APP

LOCK LOOP FILTER

VPHASE
F01 B7

CHARGE PUMP

+12V
C16 .1
R9 7.5K
R10 7.5K
CR1 1N5282
Q1 2N5771
C17 .1
+5V
TP7
R6 1.5K
VLEADR
F02 C1
CR2 1N5282
CR3 1N5282
R11 30.1K
+12V
R109 15K
TP8
VLAGR
F02 C1
CR5 1N5282
CR4 1N5282
Q2 2N3563
CR6 1N5282
C18 .1
R12 7.5K
R13 7.5K
C19 .1
-12V
D

NOTE UNLESS OTHERWISE SPECIFIED

+12V
CR22 1N751A 5.1V
R15 165
C20 220
R16 7.5K
R17 7.5K
C21 4.7
R18 7.5K
R19 7.5K
C22 1
C24 1
R23 5.49K
C25 220
C26 220
R24 5.49K
C28 2.2
C29 2.2
C27 .0047
C73 470pF
R130 7.5K
C74 .01
C30 .1
+12V
R14 1K
R20 1K
C23 .01
R21 750
R22 750
C31 4.7
U6 MC34081P
-12V
C32 .1
R27 10
TP9 PLLER
R29 110K
+5V
+12V
U7A DG211
-12V
U7D
U7B
U7C
R30 2.49K
C34 .1
FR5+FR4
C5 F01
R28 2.49K
C33 .1
FR7+FR6
C5 F01
R32 2.49K
C36 .1
LOCK
C5 F01
VLOOP
C5 F01
C38 10
C37 10
R31 2.49K
C39 .1
<FR5
C5 F01

CAD JOB #: B063C

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN A.C.T.	DATE 7/90	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	CHECKED SM	7/24/90	TITLE: SCHEMATIC, PHASE LOCK LOOP
	PROJ. ENGR		
FINISH WAVETEK PROCESS	RELEASE APPROV.		
DO NOT SCALE DRAWING	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES .XX ±.XXX ± °		SIZE D · FSCM NO. 23338 · DWG. NO. 1104-00 3437 · REV C · SCALE NONE · MODEL 90 SERIES · SHEET 3 OF 6

1104-00 3437 3

REV	ECO	BY	DATE	APP

SINSIG
C8 F05

TRISIG
F01 C7

K2
HDIE-M-DC5V

CR27
IN753A

-12V

C108
.1

10K
R218

R220
121

R211
100

R223
30.1

CLC404
U12

R212
10

R213
499

R214
499

R215
100

R216
100

FB10

FB11

TRIOUT1
C7 F01

ZCSIG
C8 F02

HDIE-M-DC5V
K3

SIN3
F05 B1

R300
249

C300
10pF

R217
10K

.1
C107

CR26
1N753A

+12V

+5V

+5V

K2

K3

IN5282
CR25

R219
10K

TRISEL
F01 C7

Q13
VN10KM

C106
.1

NOTE UNLESS OTHERWISE SPECIFIED

CAD JOB #: B063C

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN A.C.T.	DATE 7/90	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	CHECKED	7/1/90	TITLE SCHEMATIC, PHASE LOCK LOOP
	PROJ. ENGR.	7/1/90	
FINISH WAVETEK PROCESS	RELEASE APPROV.	7/2/90	
DO NOT SCALE DRAWING	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES .XX ± .XXX ± °		SIZE D · FSCM NO. 23338 · DWG. NO. 1104-00-3437 · REV B · SCALE NONE · MODEL 90 SERIES · SHEET 4 OF 6

1104-00-3437 B

REV	ECO	BY	DATE	APP

SINE CONVERTER

+12VADJ
F06 D5

R37 10K
R38 2K
R39 30.1K
C41 .1
R40 150
R52 200
R62 100K
R41 39.2
R55 27.4
R42 392
CR11 *
CR12 *
CR13 *
R49 1.5K NOM
R53 10
R54 24.9
R56 10
CR7 *
CR8 *
SINSIG
F04 D2
R33 100
R34 21.5
R35 155-180FAK-B01
R36 10
R50 1K-500K
R57 21.5
R58 21.5
C40 10pF
C43 15pF
R146 24.9
R59 10
R51 1.5K NOM
R147 10
CR9 *
CR10 *
CR16 *
R43 392
CR14 *
CR15 *
R44 39.2
R61 27.4
R45 150
R60 200
R63 100K
R46 10K
R47 2K
R48 30.1K
-12VADJ
F06 B5
C42 .1

* DIODE SET 5082-2811.

SINE BUFFER

TP11 AGND
+12V
C113 TRIM
R68 301
R70 301
C102 NOM
C46 .1
CR17 1N5282
Q3 2N5771
R74 15
Q4 2N2369A
+12V
R64 100K
R65 15K
-12V
C103T 2.7pF, NOM
CR23 1N751A
R79T 150, NOM
SIN1
C5 F01
TP13 SINCO
Q5 AD812
TP10 SIN
R75 392
R77 40.2
R128 100
SIN3
C4 F04
R67 165
R71 15
R69 15
R76 140
R208 500
R80 1.21K
R81 1.21K
R72 2K
R73 2K
R210 1K-500K
R224 150
C53 .1
R301 NOM 523
C301 NOM 15pF

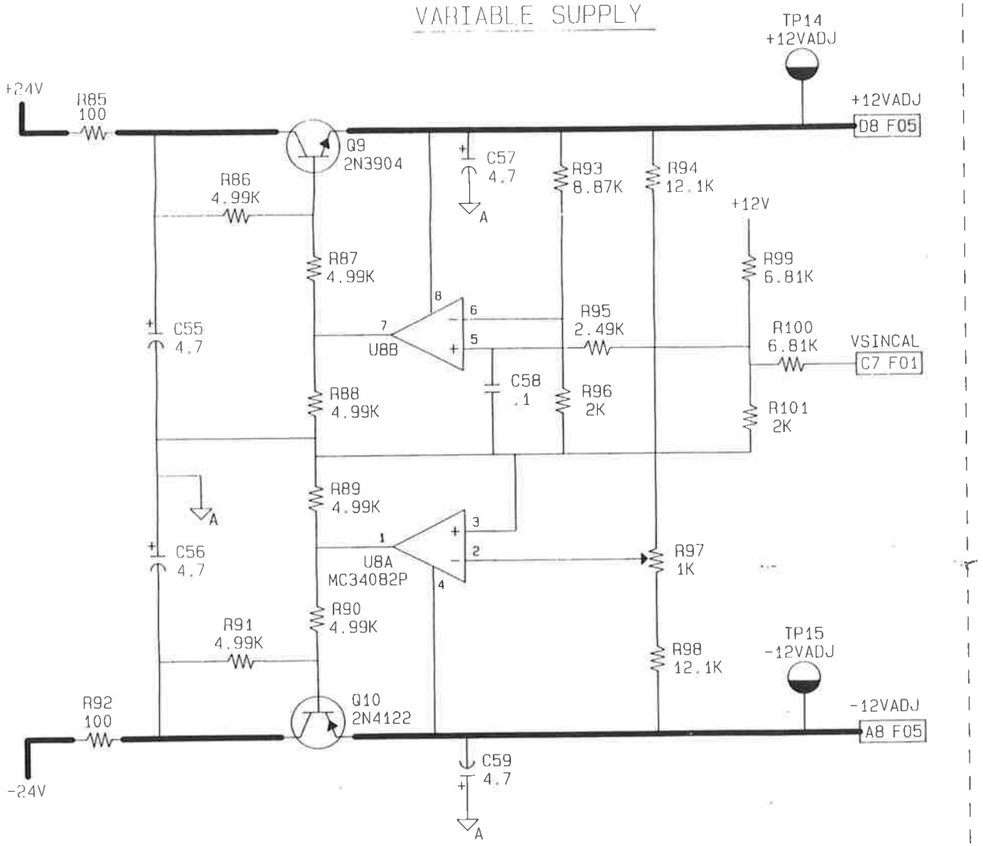
NOTE UNLESS OTHERWISE SPECIFIED

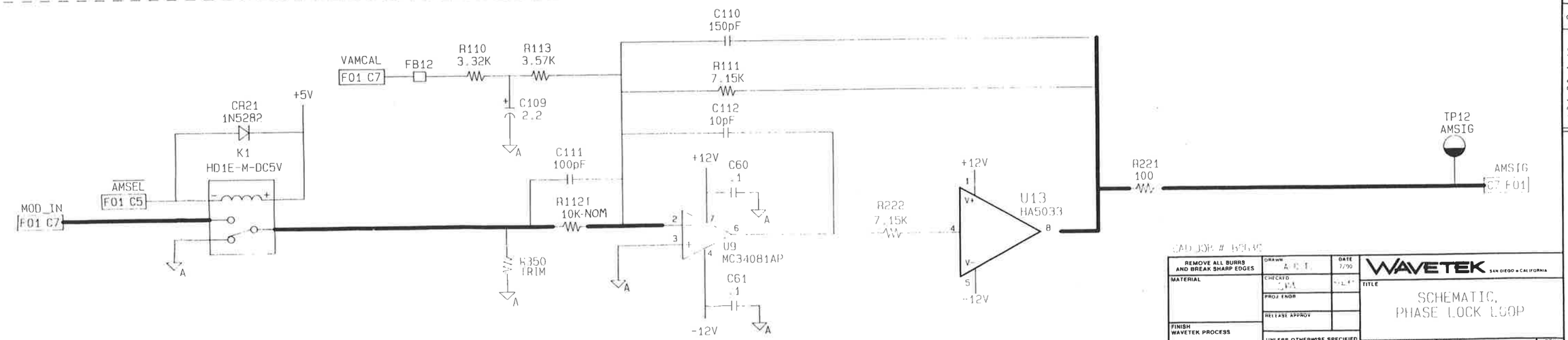
REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN A.C.T.	DATE 7/90	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	CHECKED SM	7/12/90	TITLE: SCHEMATIC, PHASE LOCK LOOP
	PROJ. ENGR.		
	RELEASE APPROV.		
FINISH WAVETEK PROCESS	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES .XX ± .XXX ± °		SIZE D · FSCM NO. 23338 · DWG. NO. 1104-00-3437 · REV B · SCALE NONE · MODEL 90 SERIES · SHEET 5 OF 6
DO NOT SCALE DRAWING			

1104-00-3437 B

REV	ECO	BY	DATE	APP

VARIABLE SUPPLY





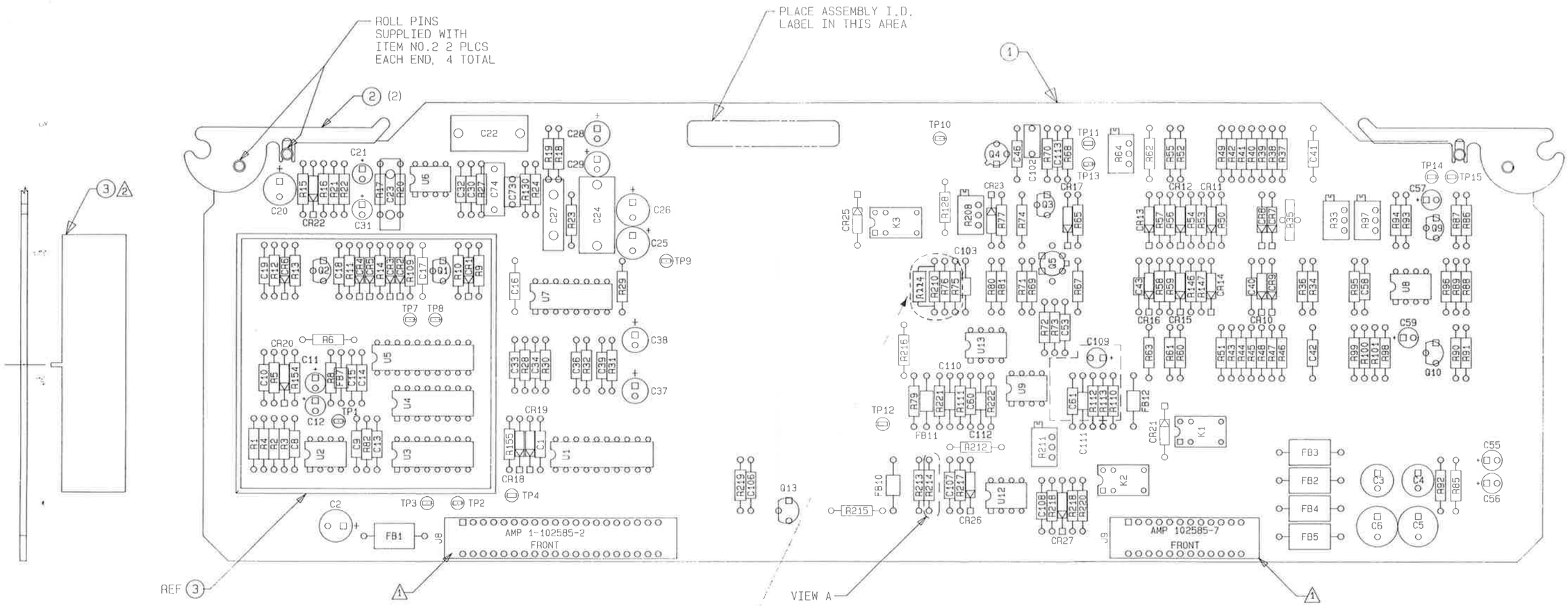
NOTE UNLESS OTHERWISE SPECIFIED

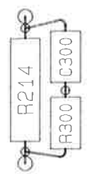
CAD JOB # 23338

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN A. R. T.	DATE 7/90	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	CHECKED		TITLE: SCHEMATIC, PHASE LOCK LOOP
	PROJ ENGR		
	RELEASE APPROV		
FINISH WAVETEK PROCESS	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE FRACTIONS DECIMALS ANGLES XX ± XXX ±		SIZE D · FSCM NO 23338 · DWG NO 1104-00-3437 · REV B · SCALE NONE · MODEL 90 SERIES · SHEET 6 OF 6
DO NOT SCALE DRAWING			

1104-00-3437 B

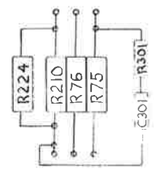
REV	ECO	BY	DATE	APP
A	ECO 90-554 -CLS I FROM: 1101-00-3341	MA	[illegible]	[illegible] 10/3/90
B	ECO#91-121	MA	1-91	[illegible]





VIEW "A"
SCALE: NONE

ACCEPTABLE VALUES FOR R112T	
R112T	
9.76K	
10K	
10.5K	



VIEW "B"
SCALE: NONE

6. ASSEMBLE PER WAVETEK WORKMANSHIP STANDARDS.
5. REFERENCE DESIGNATIONS DO NOT APPEAR ON PARTS.
4. FOR ASSEMBLY INTERCONNECTION, SEE INSTRUMENT SCHEMATIC.
3. SEE 1104-00-3341 FOR SCHEMATIC.
2. INSTALL CAN FLUSH TO COMPONENT SIDE OF P.C. BOARD. SOLDER TABS ON CIRCUIT SIDE.
1. MANUFACTURER'S MARKING INDICATES CORRECT ORIENTATION OF CONNECTOR.

NOTE UNLESS OTHERWISE SPECIFIED

CAD JOB #: B063D

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN: Amy Talmadge	DATE: 6/20/90	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	CHECKED: D.FISH	6/29/90	TITLE: PCA, PHASE LOCK LOOP BOARD
	PROJ. ENGR: D.E.FISH	6/29/90	
	RELEASE APPROV: JM	10/9/90	
FINISH WAVETEK PROCESS	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES .XX ± .XXX ±		SIZE: D; FSCM NO.: 23338; DWG. NO.: 1101-00-3437; REV: B
DO NOT SCALE DRAWING			SCALE: 2/1; MODEL: 90 SERIES; SHEET 1 OF 1

REV	ECO	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
REF	MODEL 90 SUB-ASY FUNCTION TEST PROCESS	1008-00-0596-1	WVTK	1008-00-0596	1
NONE	A/D PHASE LOCK LOOP	1101-00-3437	WVTK	1101-00-3437	1
NONE	SCHEMATIC, PHASE LOCK LOOP	1104-00-3437	WVTK	1104-00-3437	1
R8	RES, CFLM 4.7 OHM 5% 1/4W	5043CX4R700J	MEPCO	116.9471	1
CR26 CR27	SL ZR 6.2V 5% 400MW (1N753A)	1N753A	ROHM	131.9620	2
3	CAN, SYNTHESIZER	1400-02-3443	WVTK	1400-02-3443	1
C112 C300T C40	CAP CER 10PF 200V 5% AXIAL	CAC02CD0100J100A(DBS)	CORNG	1500-01-0006	3
C111	CAP, CER, 100PF, 100V, AXIAL	CAC02CD0101J100A(DBS)	CORNG	1500-01-0106	1
C1 C10 C106 C107 C108 C13 C14 C15 C16 C17 C18 C19 C30 C32 C33 C34 C36 C39 C41 C42 C46 C53 C58 C60 C61 C8 C9	CAP, CER, MON, .1MF, 50V, AXIAL	CAC03Z5U104Z050A	CORNG	1500-01-0405	27
C43	CAP, CER, 15PF, 100V, AXIAL	CAC02CD0150J100A	CORNG	1500-01-5006	1
C110	CAP, CER, 150PF, 100V, 5%, AXIAL	CAC02CD0151J100A	CORNG	1500-01-5100	1

WAVETEK PARTS LIST | TITLE: PCA, PHASE LOCK LOOP | ASSEMBLY NO. 1100-00-3437 | REV D

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
C103T	CAP, CER, 1.5PF, 200V, AXIAL	SA102A1R5DAA	AVX	1500-01-5906	1
C73	CAP, CER, 470PF, 1KV	DD-471	CRL	1500-04-7111	1
C301T	CAP, CER, 5.1PF, 200V, AXIAL	SA102A5R1DAA	AVX	1500-05-1906	1
C37 C38	CAP, ELECT, 10MF, 20%, 16V, END MOUNT	3477CB100M016JMBS	MEPCO	1500-31-0001	2
C5 C6	CAP, ELECT, 100MF, 35V RADIAL LEAD, SP .20	NRE101M35V10X12.5	NIC	1500-31-0102	2
C2 C3 C4	CAP, ELECT, 100MF, 25V, RADIAL LEAD-SP SIZE	NRE101M25V6.3X11	NIC	1500-31-0122	3
C20 C25 C26	CAP, ELECT, 220MF, 20%, 16V, RADIAL END MOUNT, 0.14 LEAD SPACE	16TW68220M	RUBY	1500-32-2104	3
C11 C12 C21 C31 C55 C56 C57 C59	CAP, ELECT, 4.7MF/50V RADIAL LEAD, SP .10	ECEA1HV47SC	PANAS	1500-34-7903	8
C23 C74	CAP, MYLAR, .01MF, 100V	225P10391WD3	SPRAG	1500-41-0314	2
C22 C24	CAP, MYLAR, 1MF, 100V, RADIAL	PMT2R1.0K100	ITT	1500-41-0524	2
C27	CAP, MYLAR, .0047MF, 100V, RADIAL	225P47291WD3	SPRAG	1500-44-7204	1
C109 C28 C29	CAP, TANT, 2.2MF, 25V	199D225X9025AA2	SPRAG	1500-72-2502	3

WAVETEK PARTS LIST | TITLE: PCA, PHASE LOCK LOOP | ASSEMBLY NO. 1100-00-3437 | REV D

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	PCB, PHASE LOCK LOOP BD	1700-00-3341	WVTK	1700-00-3341	1
J9	CONN, HEADER, 24 PIN, RECPT, 2X12, .1 CTR, PCMT	102585-7	AMP	2100-02-0255	1
J8	CONN, HEADER, 40 PIN, RECPT, 2X20, .1 CTR PCMT	1-102585-2	AMP	2100-02-0256	1
TP11 TP4	TEST POINT, BLK, PC	TP-104-01-00	COMPO	2100-04-0054	2
TP1 TP10 TP12 TP13 TP14 TP15 TP2 TP3 TP7 TP8 TP9	TEST POINT, RED, PC	TP-104-01-02	COMPO	2100-04-0055	11
2	PC BD EJECTOR	87-2-C	BRIT	2800-07-0032	2
FB1 FB2 FB3 FB4 FB5	BALUN CORE, FERRITE, 680 OHMS	2943666671	FARIT	3100-00-0017	5
FB10 FB11 FB12 FB7	BALUN CORE, FERRITE, 82 OHMS	2743015111	FARIT	3100-00-0018	4
K1 K2 K3	RELAY, 1 FORMC, 5V, .312H, .296W	HD1E-M-DC5V	AROMT	4500-00-0034	3
R64	POT, SIDE TRIM, 20T, 100K	68XR100K	BECK	4609-90-0012	1
R208	POT, SIDE TRIM, 20T, 500	68XR500	BECK	4609-90-0014	1

WAVETEK PARTS LIST | TITLE: PCA, PHASE LOCK LOOP | ASSEMBLY NO. 1100-00-3437 | REV D

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R97	POT, SIDE TRIM, 20T, 1K	68XR1K	BECK	4609-90-0015	1
R211 R33	POT, SIDE TRIM, 20T, 100	68XR100	BECK	4609-90-0017	2
R128 R215 R216 R221 R85 R92	RES, MF, 1/8W, 1%, 100	RN55D-1000F	TRW	4701-03-1000	6
R14 R20	RES, MF, 1/8W, 1%, 1K	RN55D-1001F	TRW	4701-03-1001	2
R217 R218 R219 R37 R46	RES, MF, 1/8W, 1%, 10K	RN55D-1002F	TRW	4701-03-1002	5
R62 R63	RES, MF, 1/8W, 1%, 100K	RN55D-1003F	TRW	4701-03-1003	2
R147 R212 R222 R27 R36 R53 R56 R59	RES, MF, 1/8W, 1%, 10	5043ED10R100F	MEPCO	4701-03-1009	8
R29	RES, MF, 1/8W, 1%, 110K	RN55D-1103F	TRW	4701-03-1103	1
R220	RES, MF, 1/8W, 1%, 121	RN55D-1210F	TRW	4701-03-1210	1
R80 R81	RES, MF, 1/8W, 1%, 1.21K	RN55D-1211F	TRW	4701-03-1211	2
R94 R98	RES, MF, 1/8W, 1%, 12.1K	RN55D-1212F	TRW	4701-03-1212	2
R76	RES, MF, 1/8W, 1%, 140	RN55D-1400F	TRW	4701-03-1400	1
R224 R40 R45 R79	RES, MF, 1/8W, 1%, 150	RN55D-1500F	TRW	4701-03-1500	4
R49 R51 R6	RES, MF, 1/8W, 1%, 1.5K	RN55D-1501F	TRW	4701-03-1501	3
R109 R65	RES, MF, 1/8W, 1%, 15K	RN55D-1502F	TRW	4701-03-1502	2
R154 R69 R71 R74	RES, MF, 1/8W, 1%, 15	RN55D-15R0F	TRW	4701-03-1509	4

WAVETEK PARTS LIST | TITLE: PCA, PHASE LOCK LOOP | ASSEMBLY NO. 1100-00-3437 | REV D

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R15 R67	RES, MF, 1/8W, 1%, 165	RN55D-1650F	TRW	4701-03-1650	2
R2 R52 R60	RES, MF, 1/8W, 1%, 200	RN55D-2000F	TRW	4701-03-2000	3
R101 R38 R47 R72 R73 R96	RES, MF, 1/8W, 1%, 2K	RN55D-2001F	TRW	4701-03-2001	6
R34 R57 R58	RES, MF, 1/8W, 1%, 21.5	RN55D-21R5F	TRW	4701-03-2159	3
R300T	RES, MF, 1/8W, 1%, 249	RN55D-2490F	TRW	4701-03-2490	1
R28 R3 R30 R31 R32 R95	RES, MF, 1/8W, 1%, 2.49K	RN55D-2491F	TRW	4701-03-2491	6
R146 R54	RES, MF, 1/8W, 1%, 24.9	RN55D-24R9F	TRW	4701-03-2499	2
R55 R61	RES, MF, 1/8W, 1%, 27.4	RN55D-27R4F	TRW	4701-03-2749	2
R113	RES, MF, 1/8W, 1%, 2.94K	5033RD2K490F	MEPCO	4701-03-2941	1
R1 R68 R70	RES, MF, 1/8W, 1%, 301	RN55D-3010F	TRW	4701-03-3010	3
R11 R39 R48	RES, MF, 1/8W, 1%, 30.1K	RN55D-3012F	TRW	4701-03-3012	3
R223	RES, MF, 1/8W, 1%, 30.1	RN55D-30R1F	TRW	4701-03-3019	1
R110	RES, MF, 1/8W, 1%, 3.32K	RN55D-3321F	TRW	4701-03-3321	1
R155 R4 R42 R43 R75	RES, MF, 1/8W, 1%, 392	RN55D-3920F	TRW	4701-03-3920	5
R41 R44	RES, MF, 1/8W, 1%, 39.2	RN55D-39R2F	TRW	4701-03-3929	2
R77	RES, MF, 1/8W, 1%, 40.2	RN55D-40R2F	TRW	4701-03-4029	1
R213 R214	RES, MF, 1/8, 1%, 499	RN55D-4990F	TRW	4701-03-4990	2

WAVETEK PARTS LIST | TITLE: PCA, PHASE LOCK LOOP | ASSEMBLY NO. 1100-00-3437 | REV D

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R82 R86 R87 R88 R89 R90 R91	RES, MF, 1/8W, 1%, 4.99K	RN55D-4991F	TRW	4701-03-4991	7
R301	RES, MF, 1/8W, 1%, 523	RN55D-5230F	TRW	4701-03-5230	1
R23 R24	RES, MF, 1/8W, 1%, 5.49K	RN55D-5491F	MEPCO	4701-03-5491	2
R5	RES, MF, 1/8W, 1%, 681	RN55D-6810F	TRW	4701-03-6810	1
R100 R99	RES, MF, 1/8W, 1%, 6.81K	RN55D-6811F	TRW	4701-03-6811	2
R111	RES, MF, 1/8W, 1%, 7.15K	RN55D-7151F	TRW	4701-03-7151	1
R21 R22	RES, MF, 1/8W, 1%, 750	RN55D-7500F	TRW	4701-03-7500	2
R10 R12 R13 R130 R16 R17 R18 R19 R9	RES, MF, 1/8W, 1%, 7.5K	RN55D-7501F	TRW	4701-03-7501	9
R93	RES, MF, 1/8W, 1%, 8.87K	RN55D-8871F	TRW	4701-03-8871	1
R112T	RES, MF, 1/8W, 1%, 9.09K	RN55D-9091F	TRW	4701-03-9091	1
CR20 CR22 CR23	DIODE, ZENOR, 5.1V, 500MW, QIB, IN751A	1N751A	FAIR	4801-01-0751	3
CR1 CR17 CR18 CR19 CR2 CR21 CR25 CR3 CR4 CR5 CR6	DIODE, HIGH CONDUCTANCE, ULTRA FAST	1N5282	FAIR	4801-01-5282	11
CR10 11 12 13 14 15 16 7 8 9	DIODE SET, 5082-2811 QTY: 10: 4809-02-2811	4898-00-0015	KLQ	4898-00-0015	1
Q4	TRANS, SILICON, PLANAR,	2N2369A	MOT	4901-02-3691	1

WAVETEK PARTS LIST | TITLE: PCA, PHASE LOCK LOOP | ASSEMBLY NO. 1100-00-3437 | REV D

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE
MATERIAL	CHECKED	
	PROJ. ENGR.	
	RELEASE APPROV.	
FINISH WAVETEK PROCESS	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES .XX ±.03 .XXX ±.005 ±	
DO NOT SCALE DRAWING		

WAVETEK SAN DIEGO • CALIFORNIA

TITLE: PCA PHASE LOCK LOOP

SIZE	FSCM NO.	DWG. NO.	REV
D	23338	1100-00-3437	D

SCALE | MODEL 91 | SHEET 1 OF 2

REV	ECO	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
	EPITAXIAL, NPN, TO-18				
Q2	TRANS, NPN, TO-92	2N3563	FAIR	4901-03-5630	1
Q9	TRANS 2N3904 NPN GENERAL PURPOSE TO-92	2N3904	FAIR	4901-03-9040	1
Q10	TRANS, GENERAL PURPOSE, PNP, TO-92	PN4122	NSC	4901-04-1220	1
Q1 Q3	TRANS 2N5771 PNP SWITCH TO-92	2N5771	NSC	4901-05-7710	2
Q13	TRANS	VN10KM	SLCON	4902-00-0100	1
R39	THERMISTOR 18.6 OHMS +/-25% CUST COATED	155-180FAK-B01	FENWL	5300-00-0002	1
R210 R50	THERMISTER, 50 OHM, +-10%, @ 25 DEG C	1K-500-K	MCI	5300-00-0013	2
U12	WIDWBAND HIGH SLEW RATE OP AMP	CLC404AJP	COMLR	7000-04-0410	1
Q5	TRANS, MONO, DUAL, NPN SUBSTITUTE FOR 7000-08-1100>REPLACEMENT FOR 7000-08-1100	LS312-52	LINSY	7000-08-1200	1
U2	COMPARATOR, ULTRA FAST, 10NS	LT1016CN8	LINTE	7000-10-1600	1
U13	VIDEO BUFFER	HA3-5033-5	HARIS	7000-50-3300	1

WAVETEK PARTS LIST | TITLE: PCA, PHASE LOCK LOOP | ASSEMBLY NO. 1100-00-3437 | REV D

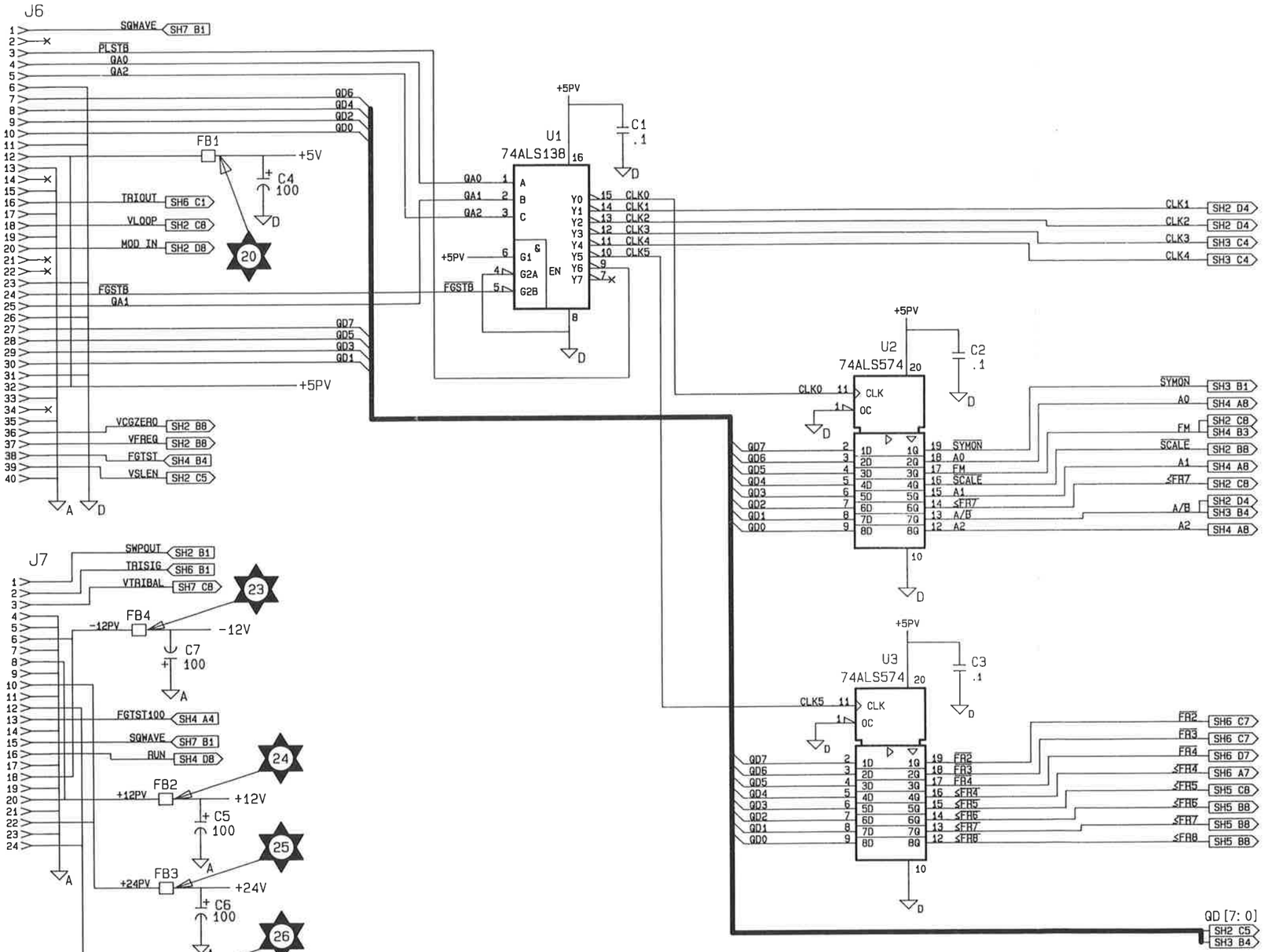
REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
U6	OP AMP, HI SLEW RTE, WIDEBND, JFET, STD	MC34081P	MOT	7003-40-8100	1
U9	OP AMP, HI SLEW RTE, WIDEBND, JFET, PRIME	MC34081AP	MOT	7003-40-8101	1
U8	OP AMP, HI SLEW RTE, WIDEBND, JFET DUAL	MC34082P	MOT	7003-40-8200	1
U7	SW, QUAD ANALOG, CMOS	DG211CJ	SLCON	8000-02-1100	1
U3	MUX/SEL, DUAL 1 OF 4 DATA, 3/STATE	SN74ALS253N	TI	8007-42-5300	1
U4	COUNTER, DUAL 4B BCD, TTL	74LS390PC	FAIR	8007-43-9010	1
U1	FLIP-FLOP, OCTAL D	SN74ALS574N	TI	8007-45-7450	1
U5	PAL, PROG USES 1 EA 8000-16-8000 FOR 1288 PHASE DET. V1.0	8600-00-0497	WVTK	8600-00-0497	1

WAVETEK PARTS LIST | TITLE: PCA, PHASE LOCK LOOP | ASSEMBLY NO. 1100-00-3437 | REV D

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	CHECKED		TITLE: PCA PHASE LOCK LOOP
	PROJ. ENGR.		
	RELEASE APPROV.		
FINISH WAVETEK PROCESS	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES .XX .XXX		SIZE D · FSCM NO. 23338 · DWG. NO. 1100-00-3437 · REV D
DO NOT SCALE DRAWING			SCALE · MODEL 91 · SHEET 2 OF 2

REV	ECO	BY	DATE	APP
A	ERO # 90-441			



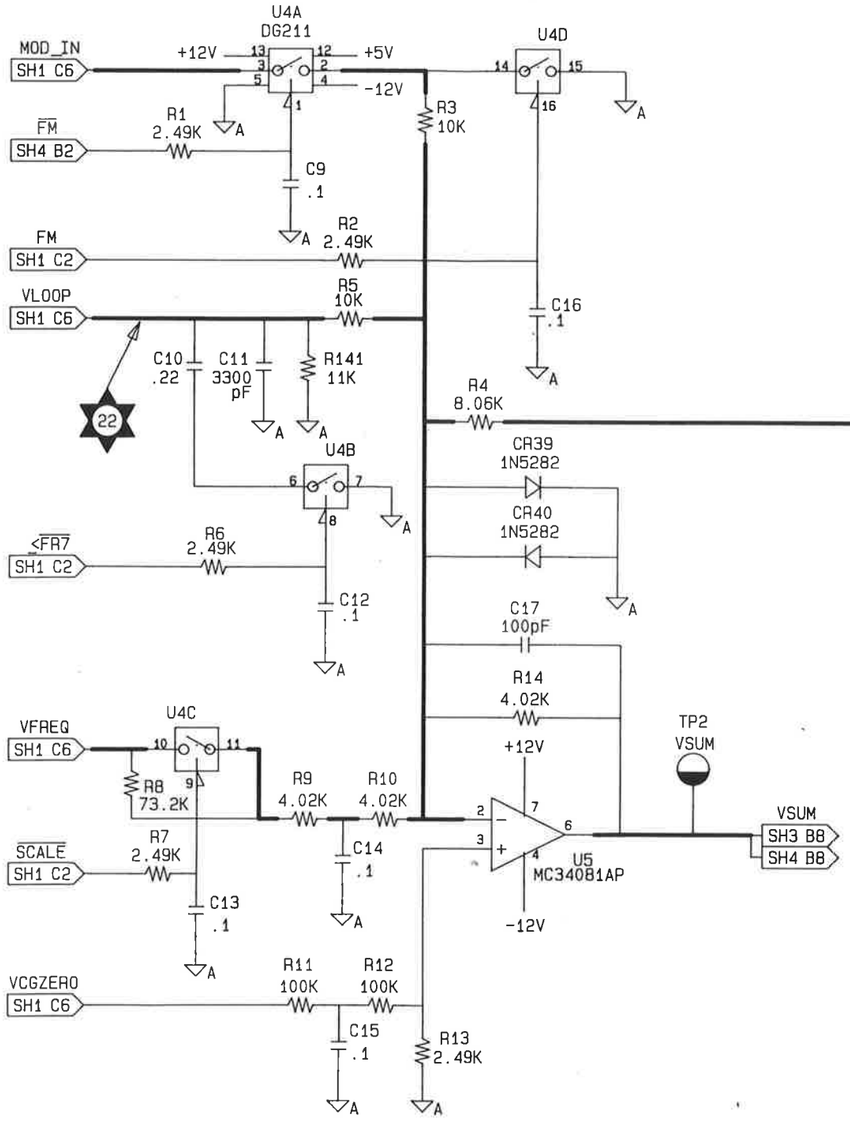
5. TEST POINTS SHOWN AS ✡ ARE FAULT ISOLATION PROCEDURES IN THE UNIT MAINTENANCE MANUAL.
4. ⏚A = ANALOG GROUND SYMBOL.
3. ⏚D = DIGITAL GROUND SYMBOL.
2. ALL CAPACITORS ARE IN MICROFARADS.
1. ALL RESISTORS ARE IN OHMS, 1/8W, 1%, MF.

NOTE UNLESS OTHERWISE SPECIFIED

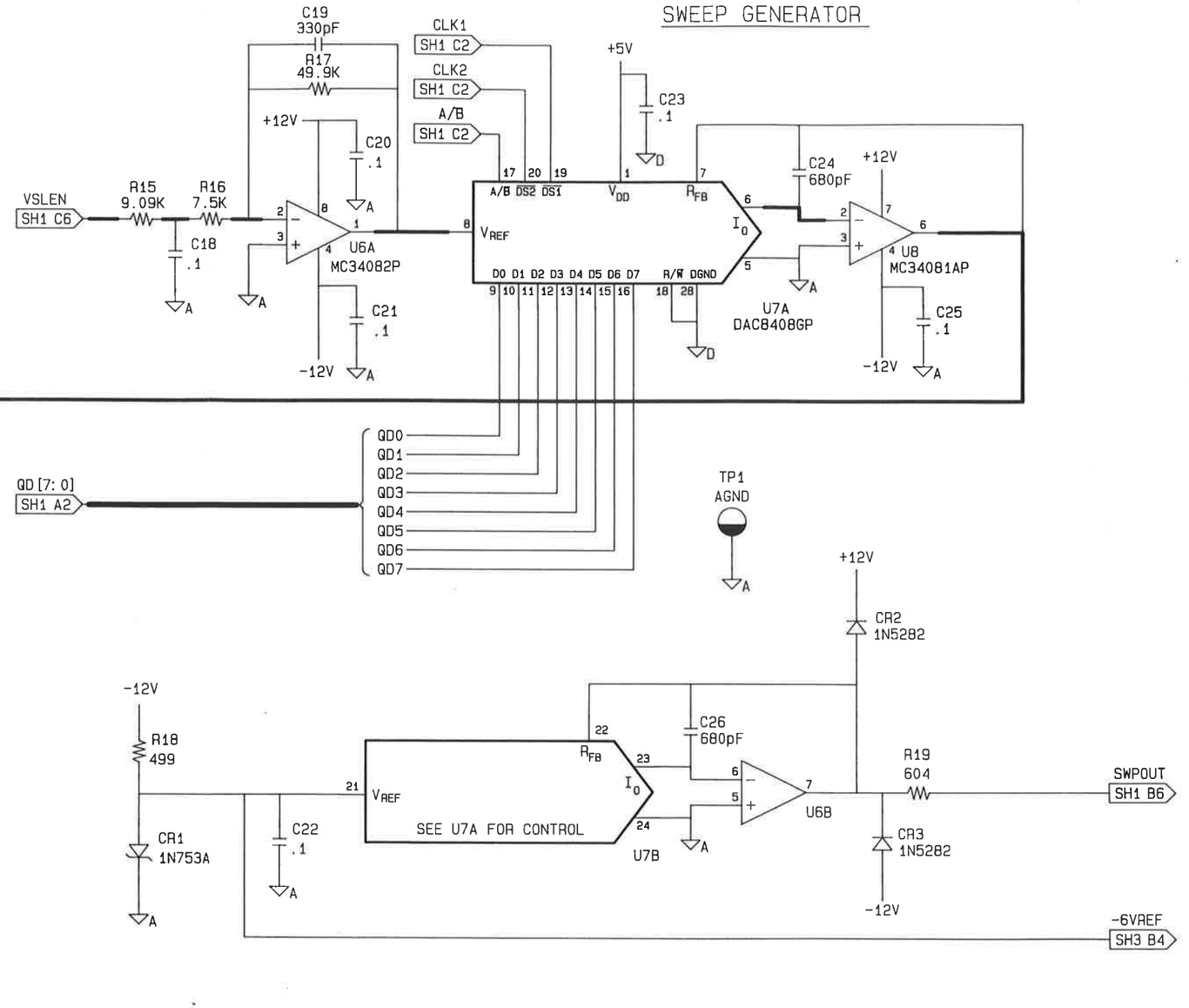
REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN A. TALMADGE	DATE 5-8-90	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	CHECKED D. FISH	5/21/90	TITLE: SCHEMATIC, FUNCTION GENERATOR
	PROJ. ENGR.	5/21/90	
	RELEASE APPROV.	5/24/90	
FINISH WAVETEK PROCESS	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES .XX ±.01 .XXX ±.005		SIZE D · FSCM NO. 23338 · DWG. NO. 1104-00-3342 · REV A · SCALE NONE · MODEL 90 SERIES · SHEET 1 OF 7
DO NOT SCALE DRAWING			

REV	ECO	BY	DATE	APP

VCG SUMMING AMPLIFIER



SWEEP GENERATOR



NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN A. TALMADGE	DATE 5-8-90	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	CHECKED		TITLE: SCHEMATIC, FUNCTION GENERATOR
	PROJ. ENGR.		
FINISH WAVETEK PROCESS	RELEASE APPROV.		
DO NOT SCALE DRAWING	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES .XX ± .XXX ± °		SIZE D · FSCM NO. 23338 · DWG. NO. 1104-00-3342 · REV A · SCALE NONE · MODEL 90 SERIES · SHEET 2 OF 7

REV	ECO	BY	DATE	APP

SYMMETRY CONTROL

VCG CURRENT SOURCES

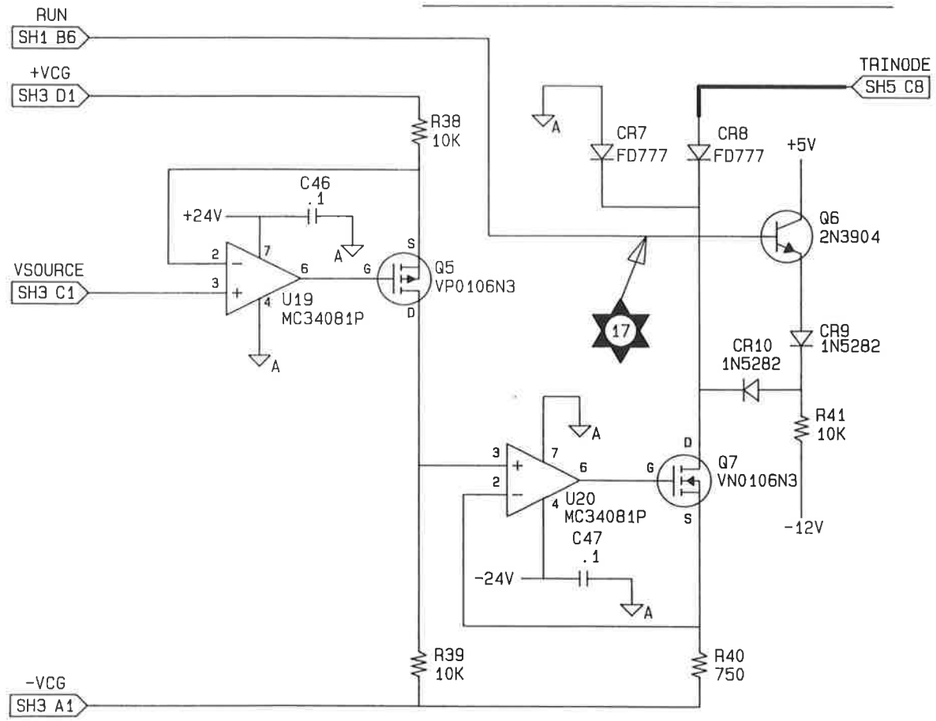
+12V
C29 22pF
U10 MC34081P
-12V
U7C
SEE U7A FOR CONTROL
R22 2.49M
R21 10M
TP3 +FCV
+FCV SH4 D5 SH4 B8
R20 4.99K
U9 MC34081P
C30 22pF
U11A MC34082P
C35 47pF
U12B
SEE U12A FOR CONTROL
+5V
C37 .1
CLK3 SH1 C2
CLK4 SH1 C2
A/B SH1 C2
-6VREF SH2 A1
VSUM SH2 B5
R23 10M
R24 2.49M
U11B
C36 47pF
U12A DAC8408GP
DS1 DS2 A/B
DGND R/W D7 D6 D5 D4 D3 D2 D1 D0
QD0 QD1 QD2 QD3 QD4 QD5 QD6 QD7
QD [7: 0] SH1 A2
C31 .1
C32 22pF
C33 .1
U16 MC34081P
U7D
TP4 -FCV
-FCV SH4 B5 SH4 B8
R25 10K .1%
R26 10K .1%
U15 MC34081P
C34 22pF
R27 4.99K
21
CR4 1N746A
+24V
R29 10
R28 10K
C38 22
R30 10k 0.1%
R36 1.5K 0.1%
TP5 +VCG
+VCG SH4 D8
TP6 VI+
C44 .1
U14 LT1001CN8
Q2 VP0106N3
ISWITCH+ SH7 D3
VSOURCE SH4 C8
C39 .1
U13 LT1001CN8
Q1 2N5485
C40 .1
R131 100K
R31 10K 0.1%
K1 HDIE-5V
R32 10K 0.1%
CR6 1N5282
SYMON SH1 C2
C41 .1
U17 LT1001CN8
Q3 2N5462
ISWITCH- SH7 A3
C42 .1
U18 LT1001CN8
Q4 VN0106N3
TP7 VI-
C45 .1
R33 10K 0.1%
TP8 -VCG
R37 1.5K 0.1%
-VCG SH4 B8
C43 22
R34 10
CR5 1N746A
R35 10K

NOTE UNLESS OTHERWISE SPECIFIED

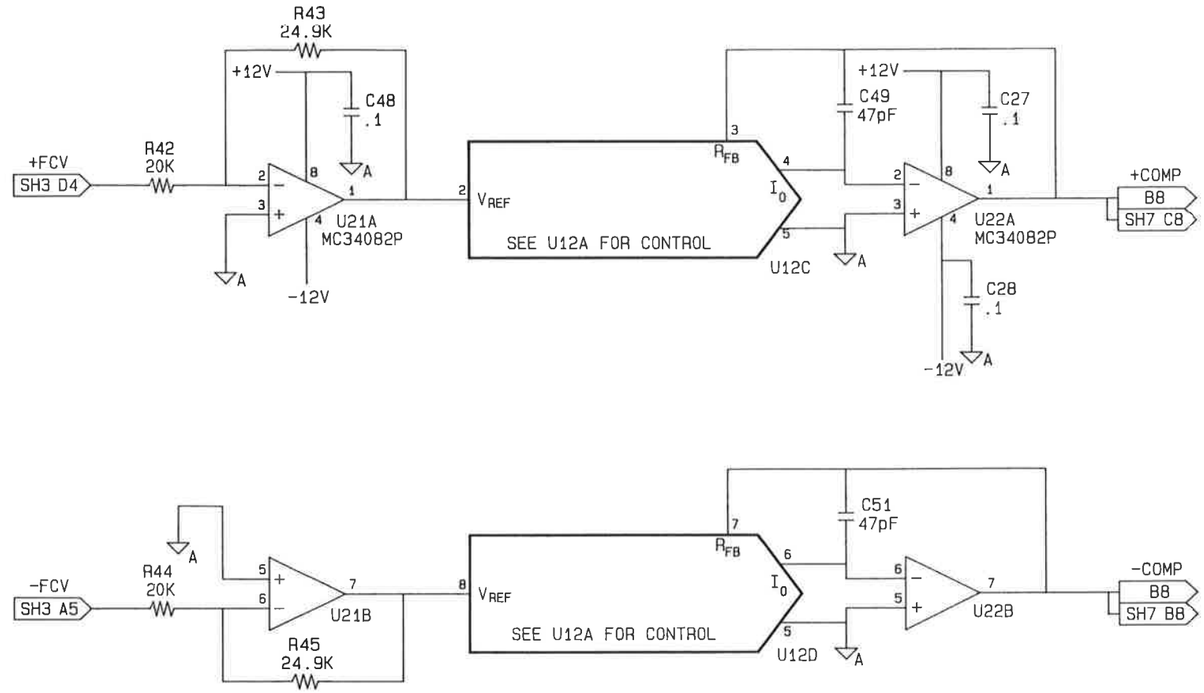
REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN A. TALMADGE	DATE 5-8-90	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	CHECKED		TITLE: SCHEMATIC, FUNCTION GENERATOR
	PROJ. ENGR.		
FINISH WAVETEK PROCESS	RELEASE APPROV.		
DO NOT SCALE DRAWING	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES XX ; .XXX ;		SIZE D · FSCM NO. 23338 · DWG. NO. 1104-00-3342 · REV A · SCALE NONE · MODEL 90 SERIES · SHEET 3 OF 7

REV	ECO	BY	DATE	APP

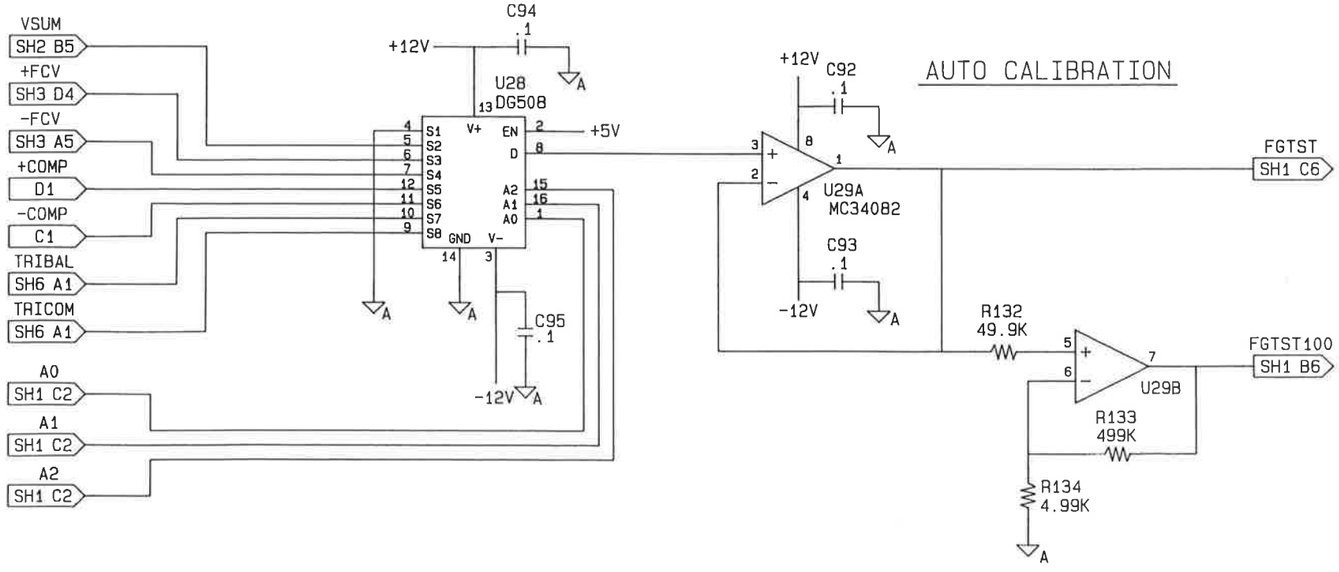
TRIGGER BASELINE COMPENSATION

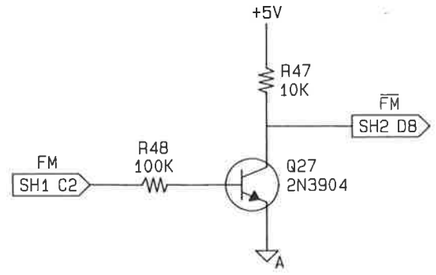


HIGH FREQUENCY COMPENSATION



AUTO CALIBRATION



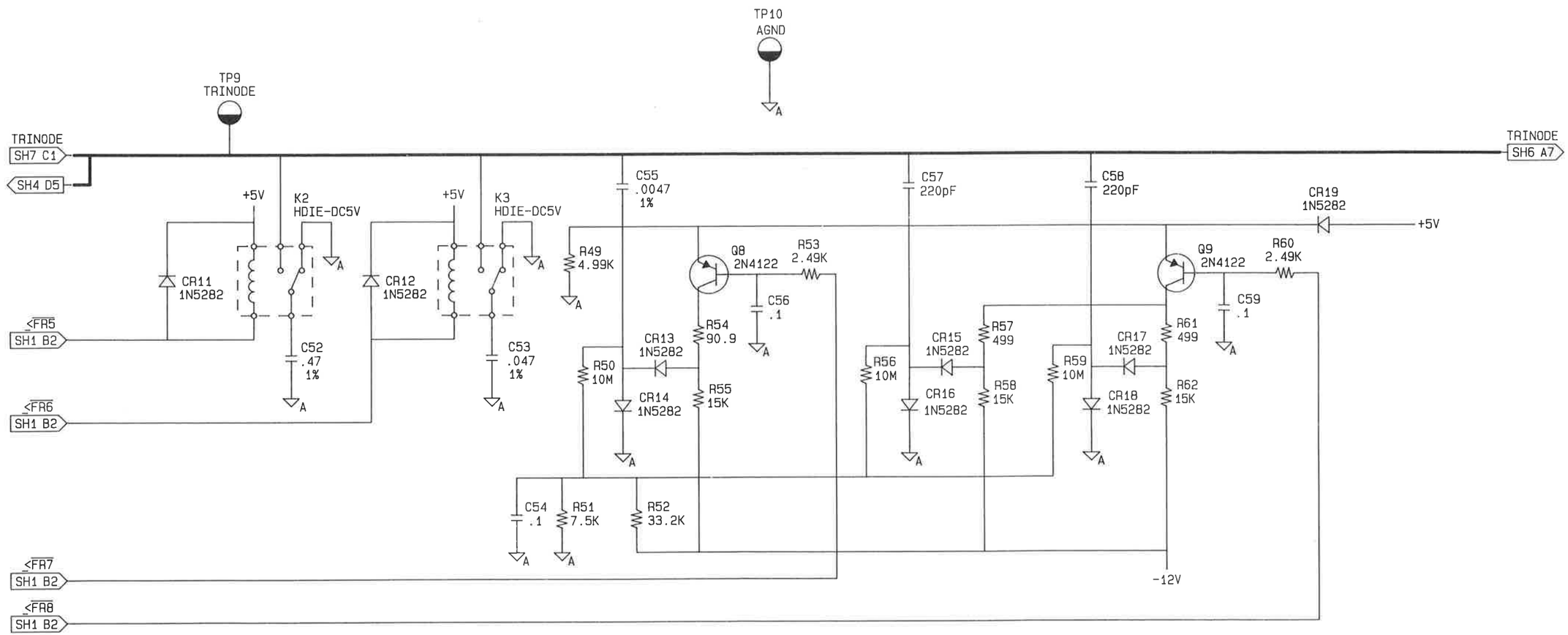


NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN A. TALMADGE	DATE 5-8-90	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	CHECKED		TITLE: SCHEMATIC, FUNCTION GENERATOR
	PROJ. ENGR.		
	RELEASE APPROV.		
FINISH WAVETEK PROCESS	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES .XX ±.XXX		SIZE D; FSCM NO. 23338; DWG. NO. 1104-00-3342; REV. A
DO NOT SCALE DRAWING			SCALE NONE; MODEL 90 SERIES; SHEET 4 OF 7

REV	ECO	BY	DATE	APP

FREQUENCY RANGE SWITCHES

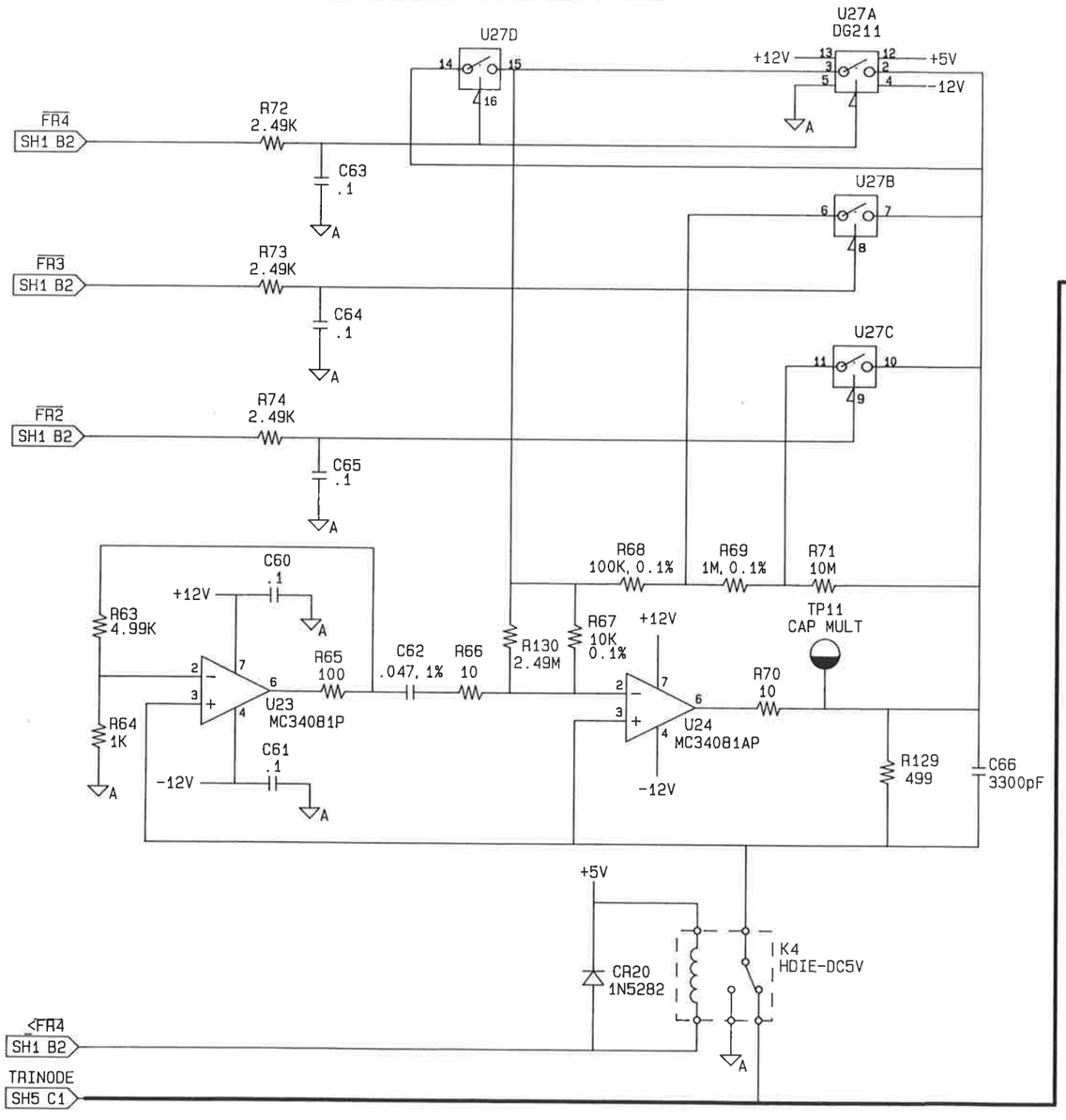


NOTE UNLESS OTHERWISE SPECIFIED

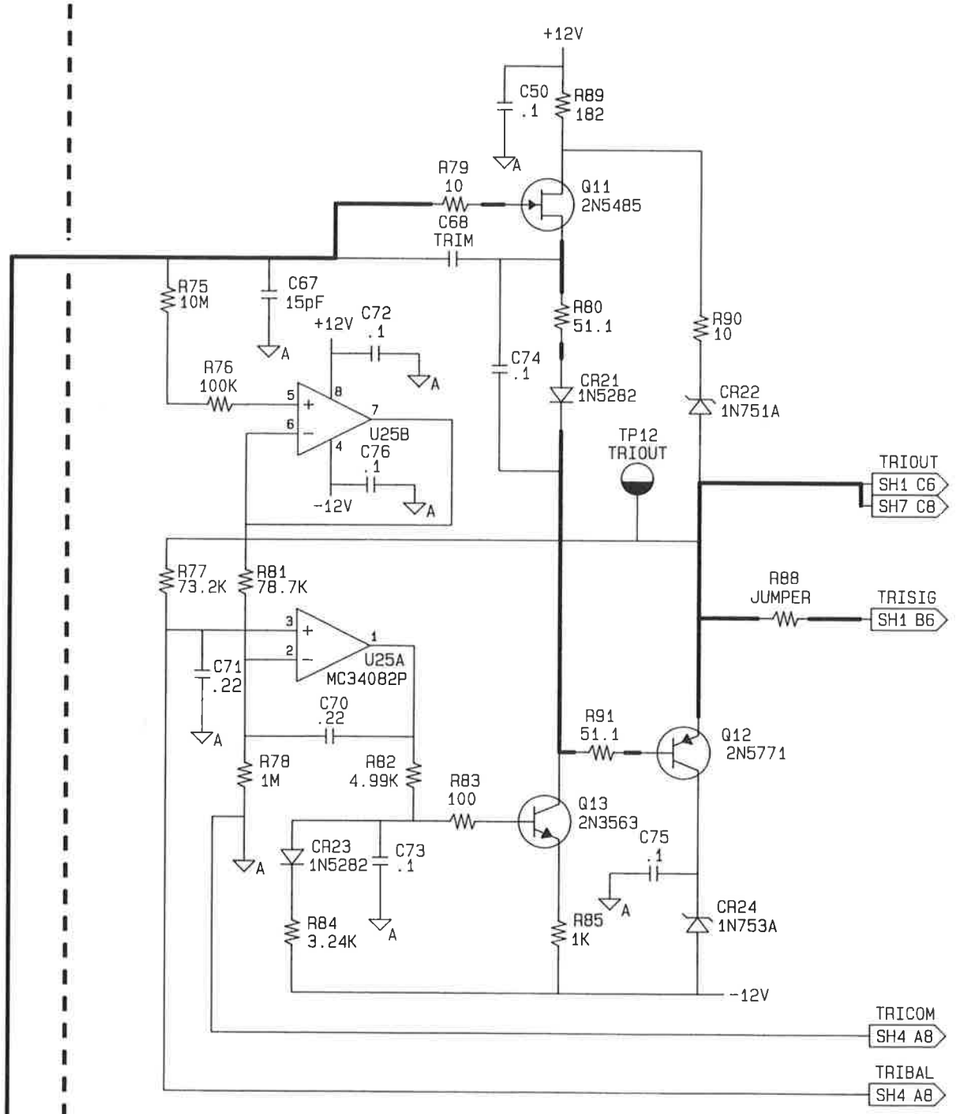
REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN A. TALMADGE	DATE 5-8-90	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	CHECKED		TITLE: SCHEMATIC, FUNCTION GENERATOR
	PROJ. ENGR.		
	RELEASE APPROV.		
FINISH WAVETEK PROCESS	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES .XX ± .XXX ±		SIZE D · FSCM NO. 23338 · DWG. NO. 1104-00-3342 · REV A
DO NOT SCALE DRAWING			SCALE NONE · MODEL 90 SERIES · SHEET 5 OF 7

REV	ECO	BY	DATE	APP

CAPACITANCE MULTIPLIER



TRIANGLE BUFFER



NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN A.TALMADGE	DATE 5-8-90	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	CHECKED		TITLE: SCHEMATIC, FUNCTION GENERATOR
	PROJ. ENGR.		
FINISH WAVETEK PROCESS	RELEASE APPROV.		
DO NOT SCALE DRAWING	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES XX ± XXX		SIZE D · FSCM NO. 23338 · DWG. NO. 1104-00-3342 · REV A · SCALE NONE · MODEL 90 SERIES · SHEET 6 OF 7

REV	ECO	BY	DATE	APP

COMPARATOR

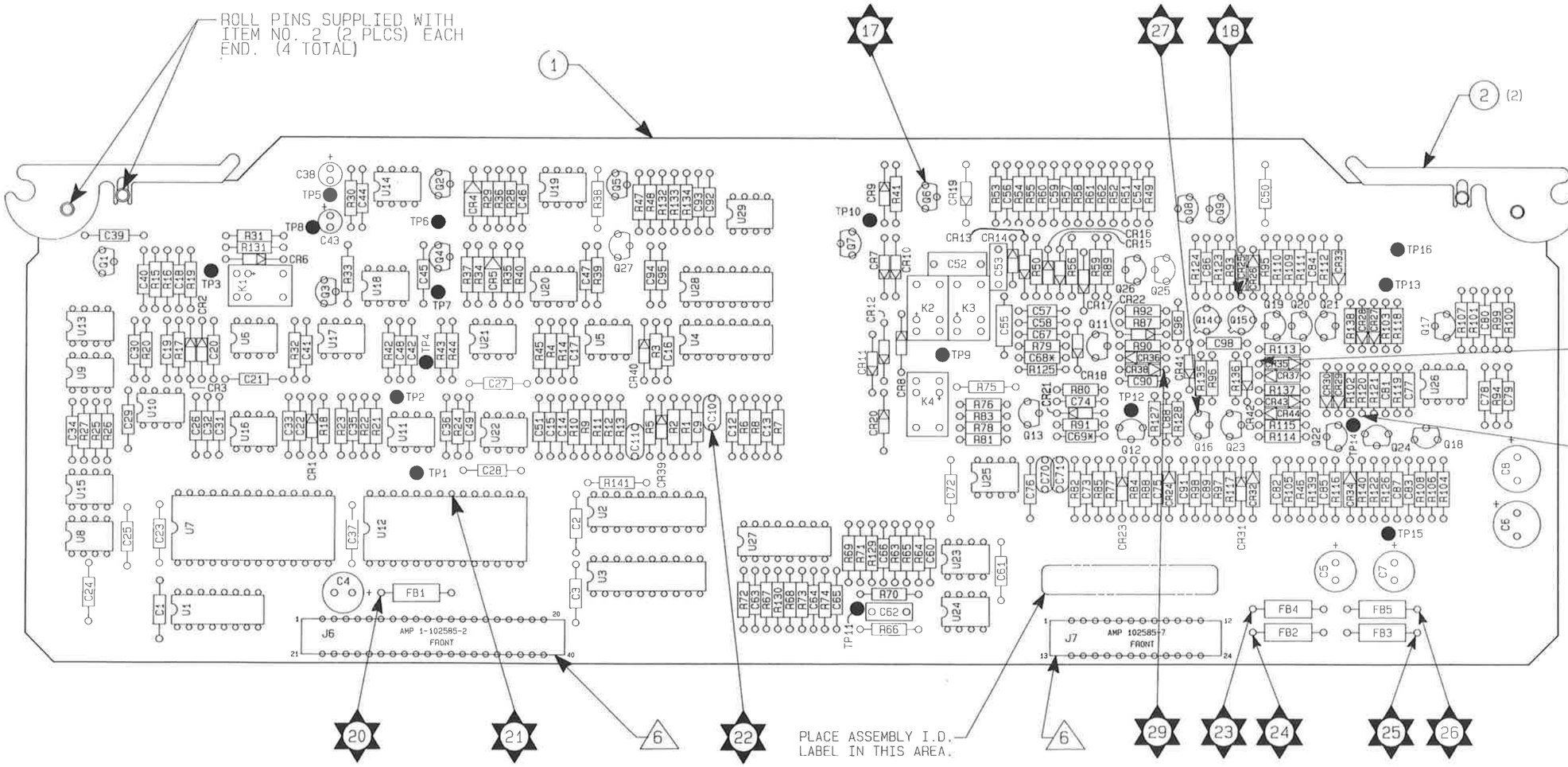
+12V
-12V
ISWITCH+ SH3 C1
ISWITCH- SH3 B1
+COMP SH4 D1
-COMP SH4 C1
VTRIBAL SH1 B6
TRIOUT SH6 C1
TRINODE SH5 C8
SQWAVE SH1 D6 SH1 B6

R93 1.1K
R95 1.1K
R101 9.09K
R100 2.37K
R107 750
C80 .1
C77 .1
U26B
R109 249
R110 21.5
R113 10
CR33 1N753A
R112 33.2
C84 .1
R138 4.99K
R111 249
R119 33.2
C87 .1
R118 2.87K
R123 4.64K
R124 7.5K
C86 .1
Q25 2N5462
Q17 2N4122
Q19 2N5771
Q21 2N3563
CR25 FD777
CR26 FD777
18
Q20 2N5771
28
19
Q24 2N3563
R120 825
R125 27.4
R121 182
TP14 SWSQR
CR35 FD777
CR36 FD777
CR37 FD777
CR38 FD777
TP15 SQWAVE
C90 1.5pF
R140 39.2
R126 78.7
R94 1K
TP13 REF SQR
CR27 1N5282
CR28 1N5282
CR43 1N5282
R137 316
Q14 2N2369A
Q15 2N2369A
C79 .1
R99 9.09K
R92 100
C96 120pF
R87 10
CR41 FD777
CR42 FD777
10pF
C98
R102 100
R103 2.87K
C81 330pF
CR29 1N5282
CR30 1N5282
CR44 1N5282
R115 301
R135 10K
R96 100
R136 10K
TP16 AGND
29
R104 2.37K
27
Q16 2N3563
U26A MC34082P
Q18 2N3904
R114 10
Q22 2N5771
Q26 2N5485
R97 78.7
R46 33.2
Q23 2N3563
C82 .1
R105 1K
C78 .1
C89 TRIM
CR31 1N5282
CR32 1N753A
R116 33.2
C85 .1
CR34 1N753A
R127 7.5K
C88 .1
R122 2K
R106 9.09K
R98 1K
R108 750
R117 392
R139 4.99K
R128 4.64K
C83 .1
C91 .1

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN A. TALMADGE	DATE 5-8-90	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	CHECKED		TITLE: SCHEMATIC, FUNCTION GENERATOR
FINISH WAVETEK PROCESS	PROJ. ENGR.		
DO NOT SCALE DRAWING	RELEASE APPROV.		SIZE D · FSCM NO. 23338 · DWG. NO. 1104-00-3342 · REV A
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES .XX ±.01 .XXX ±.005			SCALE NONE · MODEL 90 SERIES · SHEET 7 OF 7

REV	ECO	BY	DATE	APP
A	ECO No 90-441	KV	6/6/90	DCS
B	ECO No. 90-537	TF	6/29/90	DCS



7. TEST POINTS SHOWN AS ✡ ARE FAULT ISOLATION PROCEDURES IN THE UNIT MAINTENANCE MANUAL.
6. MANUFACTURER'S MARKING INDICATES CORRECT ORIENTATION OF CONNECTOR.
5. * = TRIM.
4. ASSEMBLE PER WAVETEK WORKMANSHIP STANDARDS.
3. REFERENCE DESIGNATIONS DO NOT APPEAR ON PARTS.
2. FOR ASSEMBLY INTERCONNECTION, SEE INSTRUMENT SCHEMATIC.
1. SEE 1104-00-3342 FOR SCHEMATIC.

NOTE UNLESS OTHERWISE SPECIFIED

CAD JOB #: B065C

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN Amy Talmadge	DATE 6/20/90	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	CHECKED D. Fish	6/29/90	TITLE: PCA, FUNCTION GENERATOR BOARD
	PROJ. ENGR. D. Fish	6/29/90	
FINISH WAVETEK PROCESS	RELEASE APPROV. D. Fish	6/29/90	
DO NOT SCALE DRAWING	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES XX ± .XXX ± °	SIZE D	FSCM NO. 23338
		DWG. NO. 1101-00-3342	REV B
		SCALE 2/1	MODEL 90 SERIES
		SHEET 1 OF 1	

REV	ECO	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
REF	MODEL 90 SUB-ASY FUNCTION TEST PROCESS	1008-00-0596-1	WVTK	1008-00-0596	1
NONA	A/D, PCA, FUNCTION GENERATOR	1101-00-3342	WVTK	1101-00-3342	1
NONE	S/D, PCA, FUNCTION GENERATOR	1104-00-3342	WVTK	1104-00-3342	1
CR1 CR24 CR32 CR33 CR34	SL ZR 6.2V 5% 400MW (1N753A)	1N753A	ROHM	131.9620	5
C98	CAP CER 10PF 200V 5% AXIAL	CAC02C0G100J100A(OBS)	CORNG	1500-01-0006	1
C17	CAP, CER, 100PF, 100V, AXIAL	CAC02C0G101J100A(OBS)	CORNG	1500-01-0106	1
C1 C12 C13 C14 C15 C16 C18 C2 C20 C21 C22 C23 C25 C27 C28 C3 C31 C33 C37 C39 C40 C41 C42 C44 C45 C46 C47 C48 C50 C54 C56 C59 C60 C61 C63 C64 C65 C72 C73 C74 C75 C76 C77 C78 C79 C80 C82 C83 C84 C85 C86 C87 C88 C9 C91 C92 C93 C94 C95	CAP, CER, MON, .1MF, 50V, AXIAL	CAC03Z5U104Z050A	CORNG	1500-01-0405	59
C96	CAP, CER, 120PF 200V 5% AXIAL	SA102A121JAA	AVX	1500-01-2106	1
C67	CAP, CER, 15PF, 100V, AXIAL	CAC02C0G150J100A	CORNG	1500-01-5006	1

WAVETEK PARTS LIST | TITLE: PCA, FUNCTION GENERATOR | ASSEMBLY NO. 1100-00-3342 | REV F

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
	DIAL				
C53 C62	CAP, MYLR, .047MF, 50V	C5R473F	ELPAC	1500-44-7303	2
C52	CAP, MYLR, .47MF, 50V	C5R474F	ELPAC	1500-44-7403	1
NONE	PCB, FUNCTION GENERATOR BD	1700-00-3342	WVTK	1700-00-3342	1
J7	CONN, HEADER, 24 PIN, RECPT, 2X12, .1 CTR, PCMT	102585-7	AMP	2100-02-0255	1
J6	CONN, HEADER, 40 PIN, RECPT, 2X20, .1 CTR PCMT	1-102585-2	AMP	2100-02-0256	1
TP1 TP10 TP16	TEST POINT, BLK, PC	TP-104-01-00	COMPO	2100-04-0054	3
TP11 TP12 TP13 TP14 TP15 TP2 TP3 TP4 TP5 TP6 TP7 TP8 TP9	TEST POINT, RED, PC	TP-104-01-02	COMPO	2100-04-0055	13
NONE	PC BD EJECTOR	87-2-C	BRIT	2800-07-0032	2
FB1 FB2 FB3 FB4 FB5	BALUN CORE, FERRITE, 680 OHMS	2943666671	FARIT	3100-00-0017	5
K1 K2 K3 K4	RELAY, 1 FORMC, 5V, .312H, .296W	HD1E-M-DC5V	AROMT	4500-00-0034	4
R25 R26 R30 R31 R32 R33 R67	RES, MF, 1/8W, .1%, 10K	RN55E-1002B	MEPCO	4701-02-1002	7

WAVETEK PARTS LIST | TITLE: PCA, FUNCTION GENERATOR | ASSEMBLY NO. 1100-00-3342 | REV F

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R42 R44	RES, MF, 1/8W, 1%, 20K	RN55D-2002F	TRW	4701-03-2002	2
R110	RES, MF, 1/8W, 1%, 21.5	RN55D-21R5F	TRW	4701-03-2159	1
R109 R111	RES, MF, 1/8W, 1%, 249	RN55D-2490F	TRW	4701-03-2490	2
R1 R13 R2 R53 R6 R60 R7 R72 R73 R74	RES, MF, 1/8W, 1%, 2.49K	RN55D-2491F	TRW	4701-03-2491	10
R130 R22 R24	RES, MFLM, 1/8W, 2.49M, 1%	CMF-552494F T-8	DALE	4701-03-2494	3
R125	RES, MF, 1/8W, 1%, 27.4	RN55D-27R4F	TRW	4701-03-2749	1
R103 R118	RES, MF, 1/8W, 1%, 2.87K	RN55D-2871F	TRW	4701-03-2871	2
R115	RES, MF, 1/8W, 1%, 301	RN55D-3010F	TRW	4701-03-3010	1
R43 R45	RES, MF, 1/8W, 1%, 30.1K	RN55D-3012F	TRW	4701-03-3012	2
R137	RES, MF, 1/8W, 1%, 316	RN55D-3160F	TRW	4701-03-3160	1
R84	RES, MF, 1/8W, 1%, 3.24K	RN55D-3241F	TRW	4701-03-3241	1
R100 R104	RES, MF, 1/8W, 1%, 3.32K	RN55D-3321F	TRW	4701-03-3321	2
R52	RES, MF, 1/8W, 1%, 33.2K	RN55D-3322F	TRW	4701-03-3322	1
R112 R116 R119 R46	RES, MF, 1/8W, 1%, 33.2	RN55D-33R2F	TRW	4701-03-3329	4
R117	RES, MF, 1/8W, 1%, 392	RN55D-3920F	TRW	4701-03-3920	1
R140	RES, MF, 1/8W, 1%, 39.2	RN55D-39R2F	TRW	4701-03-3929	1

WAVETEK PARTS LIST | TITLE: PCA, FUNCTION GENERATOR | ASSEMBLY NO. 1100-00-3342 | REV F

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
C90	CAP, CER, 1.5PF, 200V, AXIAL	SA102A1R5DAA	AVX	1500-01-5906	1
C29 C30 C32 C34	CAP, CER, 22PF, 100V, AXIAL	CAC02C0G220J100A(OBS)	CORNG	1500-02-2006	4
C57 C58	CAP, CER, 220PF, 100V, AXIAL	CAC02C0G221J100A	CORNG	1500-02-2106	2
C10 C70 C71	CAP, CER, .22MF, 25V	CW30C224K	CRL	1500-02-2409	3
C19 C81	CAP, CER, 330PF, 100V, AXIAL	CAC02C0G331J100A	CORNG	1500-03-3106	2
C11 C66	CAP, CER, 3300PF, 100V, 20%, AXIAL	CAC02X7R332M100A(OBS)	CORNG	1500-03-3206	2
C35 C36 C49 C51	CAP CER 47PF 200V 5% AXIAL	CAC02C0G470J100A(OBS)	CORNG	1500-04-7006	4
C55	CAP, CER, 4700PF, 50V, 2%	592CC0G4726050E	SPRAG	1500-04-7213	1
C24 C26	CAP, CER, 680PF, 100V, AXIAL	CAC02C0G681J100A	CORNG	1500-06-8106	2
C6 C8	CAP, ELECT, 100MF, 35V RADIAL LEAD, SP .20	NRE101M35V10X12.5	NIC	1500-31-0102	2
C4 C5 C7	CAP, ELECT, 100MF, 25V, RADIAL LEAD-SP SIZE	NRE101M25V6.3X11	NIC	1500-31-0122	3
C38 C43	CAP, ELECT, 22MF, 25V, RA	SRA25VB22RM6X7LL	UNCON	1500-32-2002	2

WAVETEK PARTS LIST | TITLE: PCA, FUNCTION GENERATOR | ASSEMBLY NO. 1100-00-3342 | REV F

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R68	RES, MF, 1/8W, .1%, 100K	RN55E-1003B	MEPCO	4701-02-1003	1
R69	RES, MFLM, 1/8W, 0.1%, 1.0M	CMF-55-1004BT-9	DALE	4701-02-1004	1
R36 R37	RES, MF, 1/8W, .1%, 1.5K	RN55E-1501B	CORNG	4701-02-1501	2
R102 R65 R83 R92 R96	RES, MF, 1/8W, 1%, 100	RN55D-1000F	TRW	4701-03-1000	5
R105 R64 R85 R94 R98	RES, MF, 1/8W, 1%, 1K	RN55D-1001F	TRW	4701-03-1001	5
R135 R136 R28 R3 R35 R38 R39 R41 R47 R5	RES, MF, 1/8W, 1%, 10K	RN55D-1002F	TRW	4701-03-1002	10
R11 R12 R131 R48 R76	RES, MF, 1/8W, 1%, 100K	RN55D-1003F	TRW	4701-03-1003	5
R78	RES, MF, 1/8W, 1%, 1M	RN55D-1004F	TRW	4701-03-1004	1
R21 R23 R50 R56 R59 R71 R75	RES, MF, 1/4W, 10M, 1%	5053YD10M000F	MEPCO	4701-03-1005	7
R113 R114 R29 R34 R66 R70 R79 R87 R90	RES, MF, 1/8W, 1%, 10	5043ED10R100F	MEPCO	4701-03-1009	9
R93 R95	RES, MF, 1/8W, 1%, 1.1K	RN55D-1101F	TRW	4701-03-1101	2
R141	RES, MF, 1/8W, 1%, 11K	RN55D-1102F	TRW	4701-03-1102	1
R55 R58 R62	RES, MF, 1/8W, 1%, 15K	RN55D-1502F	TRW	4701-03-1502	3
R121 R89	RES, MF, 1/8W, 1%, 182	RN55D-1820F	TRW	4701-03-1820	2
R122	RES, MF, 1/8W, 1%, 2K	RN55D-2001F	TRW	4701-03-2001	1

WAVETEK PARTS LIST | TITLE: PCA, FUNCTION GENERATOR | ASSEMBLY NO. 1100-00-3342 | REV F

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R10 R14 R9	RES, MF, 1/8W, 1%, 4.02K	RN55D-4021F	TRW	4701-03-4021	3
R123 R128	RES, MF, 1/8W, 1%, 4.64K	RN55D-4641F	TRW	4701-03-4641	2
R129 R18 R57 R61	RES, MF, 1/8, 1%, 499	RN55D-4990F	TRW	4701-03-4990	4
R134 R138 R139 R20 R27 R49 R63 R82	RES, MF, 1/8W, 1%, 4.99K	RN55D-4991F	TRW	4701-03-4991	8
R132 R17	RES, MF, 1/8W, 1%, 49.9K	RN55D-4992F	TRW	4701-03-4992	2
R133	RES, MF, 1/8W, 1%, 499K	RN55D-4993F	TRW	4701-03-4993	1
R80 R91	RES, MF, 1/8W, 1%, 51.1	RN55D-51R1F	TRW	4701-03-5119	2
R19	RES, MF, 1/8W, 1%, 604	RN55D-6040F	TRW	4701-03-6040	1
R107 R108	RES, MF, 1/8W, 1%, 681	RN55D-6810F	TRW	4701-03-6810	2
R40	RES, MF, 1/8W, 1%, 750	RN55D-7500F	TRW	4701-03-7500	1
R124 R127 R16 R51	RES, MF, 1/8W, 1%, 7.5K	RN55D-7501F	TRW	4701-03-7501	4
R81	RES, MF, 1/8W, 1%, 78.7K	RN55D-7872F	TRW	4701-03-7872	1
R126 R97	RES, MF, 1/8W, 1%, 78.7	RN55D-78R7F	TRW	4701-03-7879	2
R101 R106 R4	RES, MF, 1/8W, 1%, 8.06K	RN55D-8061F	TRW	4701-03-8061	3
R120	RES, MF, 1/8W, 1%, 825	RN55D-8250F	TRW	4701-03-8250	1
R15 R99	RES, MF, 1/8W, 1%, 9.09K	RN55D-9091F	TRW	4701-03-9091	2

WAVETEK PARTS LIST | TITLE: PCA, FUNCTION GENERATOR | ASSEMBLY NO. 1100-00-3342 | REV F

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO ◎ CALIFORNIA
MATERIAL	CHECKED		TITLE: PCA FUNCTION GENERATOR
	PROJ. ENGR.		
	RELEASE APPROV.		
FINISH: WAVETEK PROCESS	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. TOLERANCES ARE: FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±		SIZE D | FSCM NO. 23338 | DWG. NO. 1100-00-3342 | REV F
DO NOT SCALE DRAWING			SCALE | MODEL 91 | SHEET 1 OF 2

REV	ECO	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R54	RES, MF, 1/8W, 1%, 90.9	RN55D-90R9F	TRW	4701-03-9099	1
R88	RES, 0 OHM JUMPER	JP02T680	ROHM	4799-00-0087	1
R77 R8	RES, MFLM, 1/8W, 1%, 73.2 K	5033RE7322F	MEPCO	4799-00-0234	2
CR4 CR5	DIODE, ZENER, 3.3V, 5% TOL, 500MW, G/B, IN746A	1N746A	FAIR	4801-01-0746	2
CR22	DIODE, ZENOR, 5.1V, 500MW, QIB, IN751A	1N751A	FAIR	4801-01-0751	1
CR10 CR11 CR12 CR13 CR14 CR15 CR16 CR17 CR18 CR19 CR2 CR20 CR21 CR23 CR27 CR28 CR29 CR3 CR30 CR31 CR39 CR40 CR43 CR44 CR6 CR9	DIODE, HIGH CONDUCTANCE, ULTRA FAST	1N5282	FAIR	4801-01-5282	26
CR25 CR26 CR35 CR36 CR37 CR38 CR7 CR8	DIODE, ULTRA FAST	1N4244	T/CSF	4807-02-0777	8
NA NA1	DIODE 5082-2811 SCHOTTKY, 15V, 20MA	5082-2811	HP	4809-02-2811	2
Q14 Q15	TRANS, SILICON, PLANAR, EPITAXIAL, NPN, TO-18	2N2369A	MOT	4901-02-3691	2
Q13 Q16 Q21 Q23 Q24	TRANS, NPN, TO-92	2N3563	FAIR	4901-03-5630	5
Q18 Q27 Q6	TRANS 2N3904 NPN	2N3904	FAIR	4901-03-9040	3

WAVETEK PARTS LIST | TITLE: PCA, FUNCTION GENERATOR | ASSEMBLY NO. 1100-00-3342 | REV F

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
Q17 Q8 Q9	GENERAL PURPOSE TO-92 TRANS, GENERAL PURPOSE, PNP, TO-92	PN4122	NSC	4901-04-1220	3
Q25 Q3	TRANS, P-CHANNEL JFETS	2N5462	MOT	4901-05-4620	2
Q1 Q11 Q26	TRANS, N-CHANNEL JFETS	2N5485	MOT	4901-05-4850	3
Q12 Q19 Q20 Q22	TRANS 2N5771 PNP SWITCH TO-92	2N5771	NSC	4901-05-7710	4
Q4 Q7	TRANS, FET N CHANNEL	VN0106N3	SUPER	4902-01-0600	2
Q2 Q5	TRANS, FET P CHANNEL	VP0106N3	SUPER	4902-01-0601	2
U28	MUX, CMOS, D 4C, 8 CHAN/DUAL 4 CHAN ANAL	D0508ACJ	SLCON	7000-05-0800	1
U13 U14 U17 U18	OP AMP, LOW DRIFT, LOW OFFSET	LT1001CN8	LINTE	7000-10-0180	4
U12 U7	DAC, QUAD 8 BIT, MULT W/MEM, CMOS	DAC8408GP	PMI	7000-84-0800	2
U10 U15 U16 U19 U20 U23 U9	OP AMP, HI SLEW RTE, WIDEBND, JFET, BTD	MC34081P	MOT	7003-40-8100	7
U24 U5 U8	OP AMP, HI SLEW RTE, WIDEBND, JFET, PRIME	MC34081AP	MOT	7003-40-8101	3

WAVETEK PARTS LIST | TITLE: PCA, FUNCTION GENERATOR | ASSEMBLY NO. 1100-00-3342 | REV F

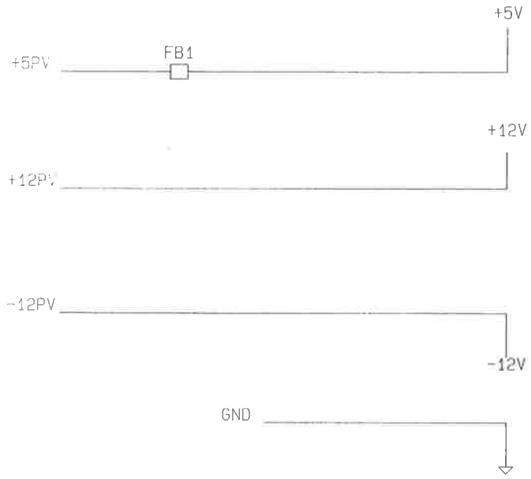
REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
U11 U21 U22 U25 U26 U29 U6	OP AMP, HI SLEW RTE, WIDEBND, JFET DUAL	MC34082P	MOT	7003-40-8200	7
U27 U4	SW, QUAD ANALOG, CMOS	DG211CJ	SLCON	8000-02-1100	2
U1	DECODER/DEMUX, 3 TO 8 LINE	SN74ALS138N	TI	8007-41-3800	1
U2 U3	FLIP-FLOP, OCTAL D	SN74ALS574N	TI	8007-45-7450	2

WAVETEK PARTS LIST | TITLE: PCA, FUNCTION GENERATOR | ASSEMBLY NO. 1100-00-3342 | REV F

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	CHECKED		TITLE: PCA FUNCTION GENERATOR
	PROJ. ENGR.		
	RELEASE APPROV.		
FINISH WAVETEK PROCESS	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES ± .XX ± .XXX ± °		SIZE D | FSCM NO. 23338 | DWG. NO. 1100-00-3342 | REV F
DO NOT SCALE DRAWING			SCALE | MODEL 91 | SHEET 2 OF 2

REV	ECO	BY	DATE	APP
A	ERO 91-325	[illegible]	6/1/91	[illegible]



J30/A

1	SQWAVE	SH5 D1
2	SYNTH	SH4 C8
3	GND	
4	QA0	
5	QA2	
6	GND	
7	QD6	SH2 C8
8	QD4	SH2 C8
9	QD2	SH2 C8
10	QD0	SH2 C8
11	GND	
12	+5PV	
13	GND	
14	GND	
15	GND	
16		
17		
18		
19		
20	MODIN	

J30/B

21	BXFREG	
22	PLS/SQR	
23	GND	
24	OXSTB/	SH2 C8
25	QA1	
26	QA3	
27	QD7	SH2 C8
28	QD5	SH2 C8
29	QD3	SH2 C8
30	QD1	SH2 C8
31	GND	
32	+5PV	
33	GND	
34	OBSIG	
35	GND	
36	SHCLK	SH4 B8
37		
38		
39	SEXDIVEX	SH4 C1
40		

J31/A

1	OPTDVM1	SH11 B1
2	GND	
3	SQR	SH4 C8
4	RUN	SH4 C1
5	GND	
6	-12V	
7	GND	
8	+12V	
9	GND	
10	+22V	
11	GND	
12	-22V	

J31/B

13	OPTDVM2	
14	GND	
15	SQR	SH4 C8
16	500KHZ	
17	GND	
18	-12V	
19	GND	
20	+12V	
21	GND	
22	+22V	
23	GND	
24	-22V	

I/O

LAST REF DES USED		
R116	RN14	NOT USED
P6	FB1	U42-U44
Q10	K2	C6, C15
U46	DL4	C24, C54
C84		C67, R98
TP11		CR15
CR30		CR17
J31		CR18

3. RESISTORS VALUED IN OHMS, 1/8W, 1%.
2. CAPACITORS VALUED IN MICROFARADS (uF).
1. FOR UNIT INTERCONNECTION, SEE INSTRUMENT SCHEMATIC.

NOTE UNLESS OTHERWISE SPECIFIED

CAD JOB #: B074B

REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH WAVETEK PROCESS
DO NOT SCALE DRAWING

		DATE
DRAWN	RO FIFER	5/91
CHECKED	[illegible]	6/12/91
PROJ. ENGR.	[illegible]	6/12/91
RELEASE APPROV.		

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS DECIMALS ANGLES
XX ± .XXX ±

WAVETEK SAN DIEGO • CALIFORNIA

TITLE
SCHEMATIC,
PULSE BOARD

SIZE	FSCM NO.	DWG. NO.	REV
D	23338	1104-00-3438	A
SCALE NONE	MODEL 91	SHEET 1 OF 11	

1104-00-3438 A

REV	ECO	BY	DATE	APP

PROCESSOR INTERFACE

U1 74HCT574 — CLK, OC, 1D–8D, 1Q–8Q; SH1 B5 OXSTB/; SH1 B6 QD0, SH1 B5 QD1, SH1 B6 QD2, SH1 B5 QD3, SH1 B6 QD4, SH1 B5 QD5, SH1 B6 QD6, SH1 B5 QD7

U2 74HC595 — EN, RCK, SRCLR, SRCK, SER, A–H, QH, SQH

U3 74HC595 — EN, RCK, SRCLR, SRCK, SER, A–H, QH, SQH

U4 74HC595 — EN, RCK, SRCLR, SRCK, SER, A–H, QH, SQH

U5 74HC595 — EN, RCK, SRCLR, SRCK, SER, A–H, QH, SQH

U6 74HC595 — EN, RCK, SRCLR, SRCK, SER, A–H, QH, SQH

+5V

CR29 1N5282

CR1 1N5282

C76 .1

C75 .1

C1 .1

C2 .1

ONCAST SH2 D1, SH6 C8, SH7 C8
DLYEN SH6 C8
WDEN SH7 C8
BAEN SH4 D8
DACEN SH9 C8
RSTCNT SH5 D8, SH6 C8, SH7 C8
DLALSEL SH5 D8
DLDGSEL SH5 D8
WDALSEL SH5 B8
WDDGSEL SH5 B8
PSLOPE SH3 D8
NSLOPE SH3 D8
EREFSEL SH5 D8
DBLSEL SH5 D8
SNEWSEL SH5 D8
PLSSEL SH5 D8
DLTSTSEL SH5 D8
PMANSEL SH5 C8
SQRSEL SH5 C8
SYNTHSL SH5 C8
EXTSEL SH5 C8
SCLK SH4 C8, SH6 C8, SH7 C8, SH9 C8
SDATA SH4 C8, SH6 C8, SH7 C8, SH9 C8
DL0SEL SH5 B8
DL50SEL SH5 B8
DL20SEL SH5 B8
TRGSYSL SH5 B8
CALP SH11 B1
CALNP SH11 A1
ENABLE SH11 C8
COMP SH5 D8
DH14 SH6 B8
DH23 SH6 B8
DH12 SH6 B8
DH34 SH6 B8
WH14 SH7 B8
WH23 SH7 B8
WH12 SH7 B8
WH34 SH7 B8
MCNTL1 SH4 D8
MCNTL2 SH4 D8
SRCNTL SH4 C8
MANTRIG SH4 C8
PLSIM SH4 C8
PDFF SH5 C8
EXDIV SH4 C8
PMAN SH5 C8

POWER DISTRIBUTION CHART

IC	U1	U2	U3	U4	U5	U6
+5V	20					
GND	10	8	8	8	8	8
PINS NOT USED						9

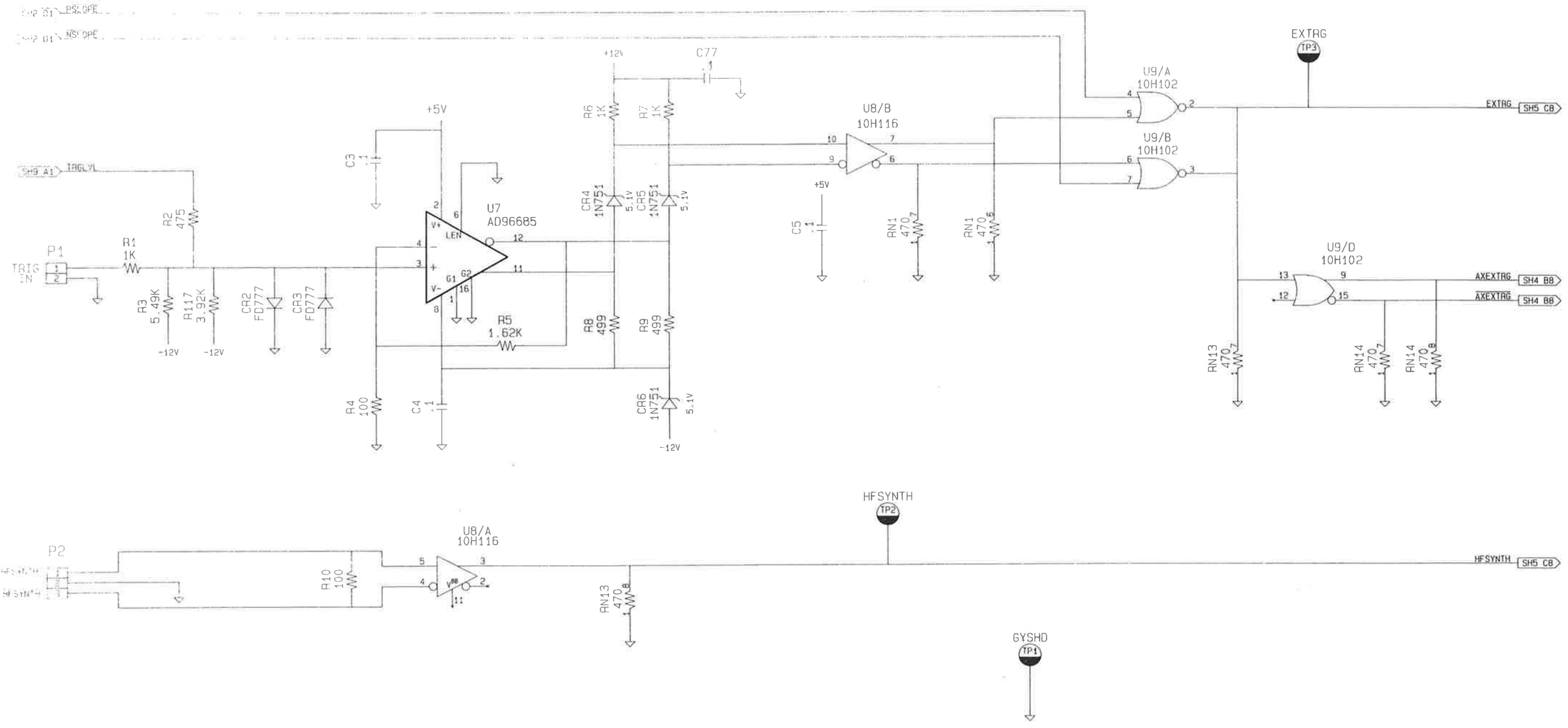
NOTE UNLESS OTHERWISE SPECIFIED

CAD JOB #: B074B

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN RO FIFER	DATE 5/91	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	CHECKED JM	6/91	TITLE: SCHEMATIC, PULSE BOARD
	PROJ. ENGR.	6/20/91	
FINISH WAVETEK PROCESS	RELEASE APPROV.		
DO NOT SCALE DRAWING	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES .XX ±.01 .XXX ±.005 °	SIZE D	FSCM NO. 23338
		DWG. NO. 1104-00-3438	REV A
		SCALE NONE	MODEL 91
		SHEET 2 OF 11	

1104-00-3438 A

REV	ECO	BY	DATE	APP



TRIGGER AMPLIFIER

POWER DISTRIBUTION CHART				
IC	U7	U8	U9	
+5V		1, 16	1, 16	
GND		8	8	
PINS USED	5, 7, 9, 10, 13, 14, 15	3, 11	10, 11, 12, 14	

NOTE UNLESS OTHERWISE SPECIFIED

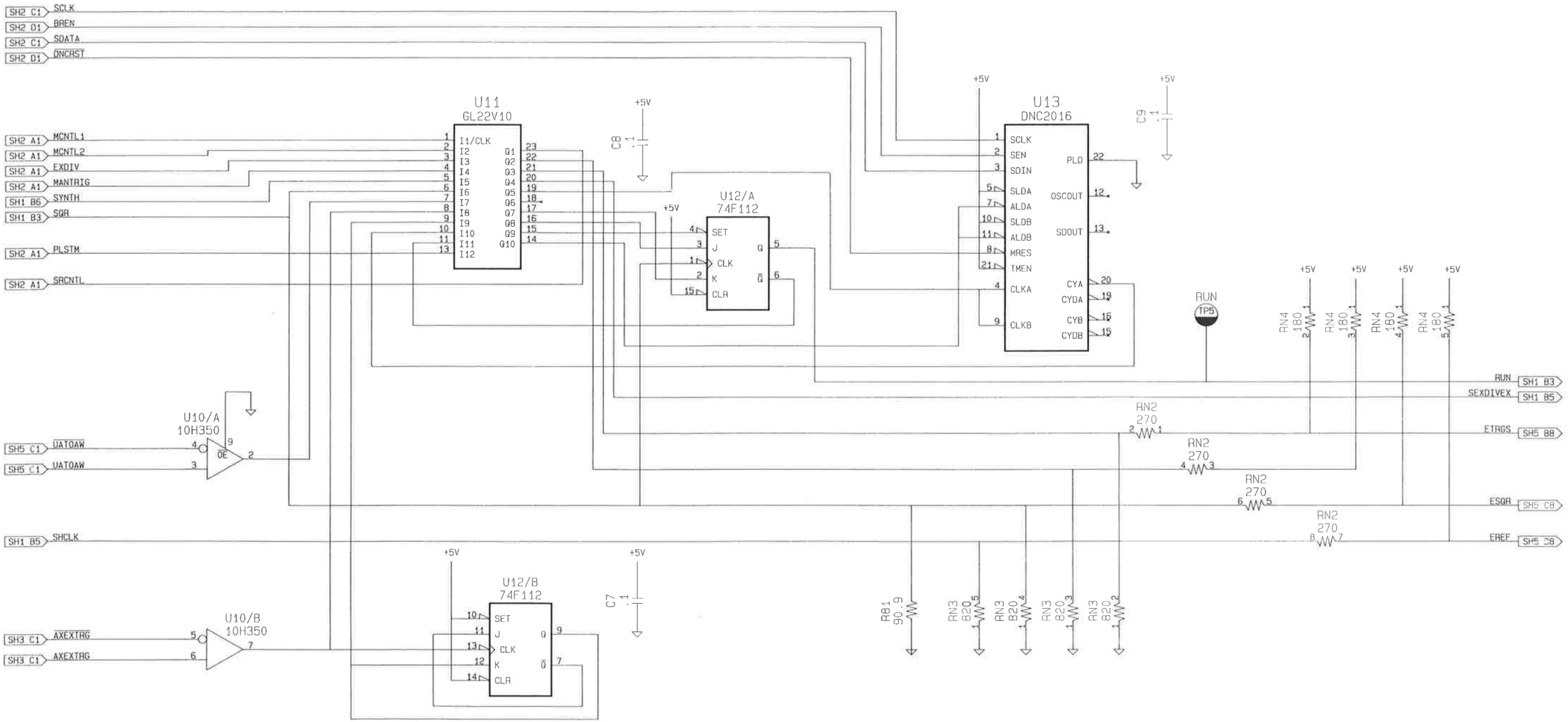
CAD JOB #: B074B

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN RO FIFER	DATE 5/91	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	CHECKED JM	6/20/91	TITLE SCHEMATIC, PULSE BOARD
	PROJ. ENGR.	6/20/91	
	RELEASE APPROV.		
FINISH WAVETEK PROCESS	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES .XX ±, .XXX ±, °		SIZE D · FSCM NO. 23338 · DWG. NO. 1104-00-3438 · REV A
DO NOT SCALE DRAWING			SCALE NONE · MODEL 91 · SHEET 3 OF 11

1104-00-3438 A

REV	ECO	BY	DATE	APP

MODE CONTROL



POWER DISTRIBUTION CHART				
IC	U10	U11	U12	U13
+5V	1, 16	24	16	6, 18
GND	8	12	8	14, 17
PINS NOT USED	13, 14, 15	18		12, 13 15, 16 19

NOTE UNLESS OTHERWISE SPECIFIED

CAD JOB #: B074B

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN RO FIFER 5/91	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	CHECKED Jun 6/91	TITLE SCHEMATIC, PULSE BOARD
	PROJ. ENGR 6/27/91	
	RELEASE APPROV.	
FINISH WAVETEK PROCESS	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES XX ± XXX ± °	SIZE D · FSCM NO. 23338 · DWG. NO. 1104-30-3438 · REV A
DO NOT SCALE DRAWING		SCALE NONE · MODEL 91 · SHEET 4 OF 11

REV	ECO	BY	DATE	APP

PULSE GENERATOR

SH2 B1 COMP
SH2 D1 EREFSEL
SH2 C1 SNEWSEL
SH2 C1 PLSSEL
SH2 C1 DLTSTSL
SH4 B1 EREF
SH2 D1 RSTCNT
SH2 C1 DBLSEL
SH2 D1 DLALSEL
SH2 D1 DLDGSEL

U14 10H121
SH2 A1 PMAN
SH2 C1 PMANSEL
SH4 B1 ESQR
SH2 C1 SQRSEL
SH3 B1 HFSYNTH
SH2 C1 SYNTHSL
SH3 D1 EXTRG
SH2 C1 EXTSEL
SH2 A1 POFF

U46/A 10H102
R11 499
C10 10pF-MICA
RN5/F 470
RN5/A 470
RN13/E 470

U15/A 10H102
U15/B 10H102
U15/C 10H102
U15/D 10H102
DLYIN TP11
RN5 470
RN6 470
R85 475

U16/D 10H102
CR30 1N5282
WDIN TP8
U16/B 10H102
U16/C 10H102
R84 475
TONE TP7

U17/A 10H131
U17/B 10H131B

U18 10H121
RN5 470
RN6 470
RN14 470

+5V C11 .1 C12 .1 C13 .1

U19/C 10H107
PLS TP10
U10/C 10H350
SQWAVE SH1 B6
PLS SH11 B8
PLS SH11 B8
UATOAW SH4 B8
UATOAW SH4 B8

DLALOG SH6 D8
DLDIG SH6 C8
DELAY ONE SHOT (SHT 6)
SH6 D1 DLPLS
WDPLS TP9
GYSHD TP6
WDALOG SH7 D8
WDDIG SH7 C8
WIDTH ONE SHOT (SHT 7)
SH7 D1 WDPLS

SH2 D1 WDALSEL
SH2 D1 WDDGSEL

SH2 B1 DLOSEL
SH2 B1 DL50SEL
SH2 B1 DL20SEL
SH4 C1 ETRGS
SH2 B1 TRGSYSL

U46/B 10H102
DL1 50nS
DL2 50nS
R102 475
R103T 110 NOM
R82 365
R105T 110 NOM
R83 365
R104T 200 NOM

U20 10H121
SYNC SH8 C8
SYNC SH8 D8

POWER DISTRIBUTION CHART

IC	U14	U15	U16	U17	U18	U19	U20
+5V	1, 16	1, 16	1, 16	1, 16	1, 16	1, 16	1, 16
GND	8	8	8	8	8	8	8
PINS NOT USED		2,4 5		10, 13, 15	3, 6, 10 15	2, 3, 4 5, 6, 10 7, 9, 11	6, 10 15

NOTE UNLESS OTHERWISE SPECIFIED

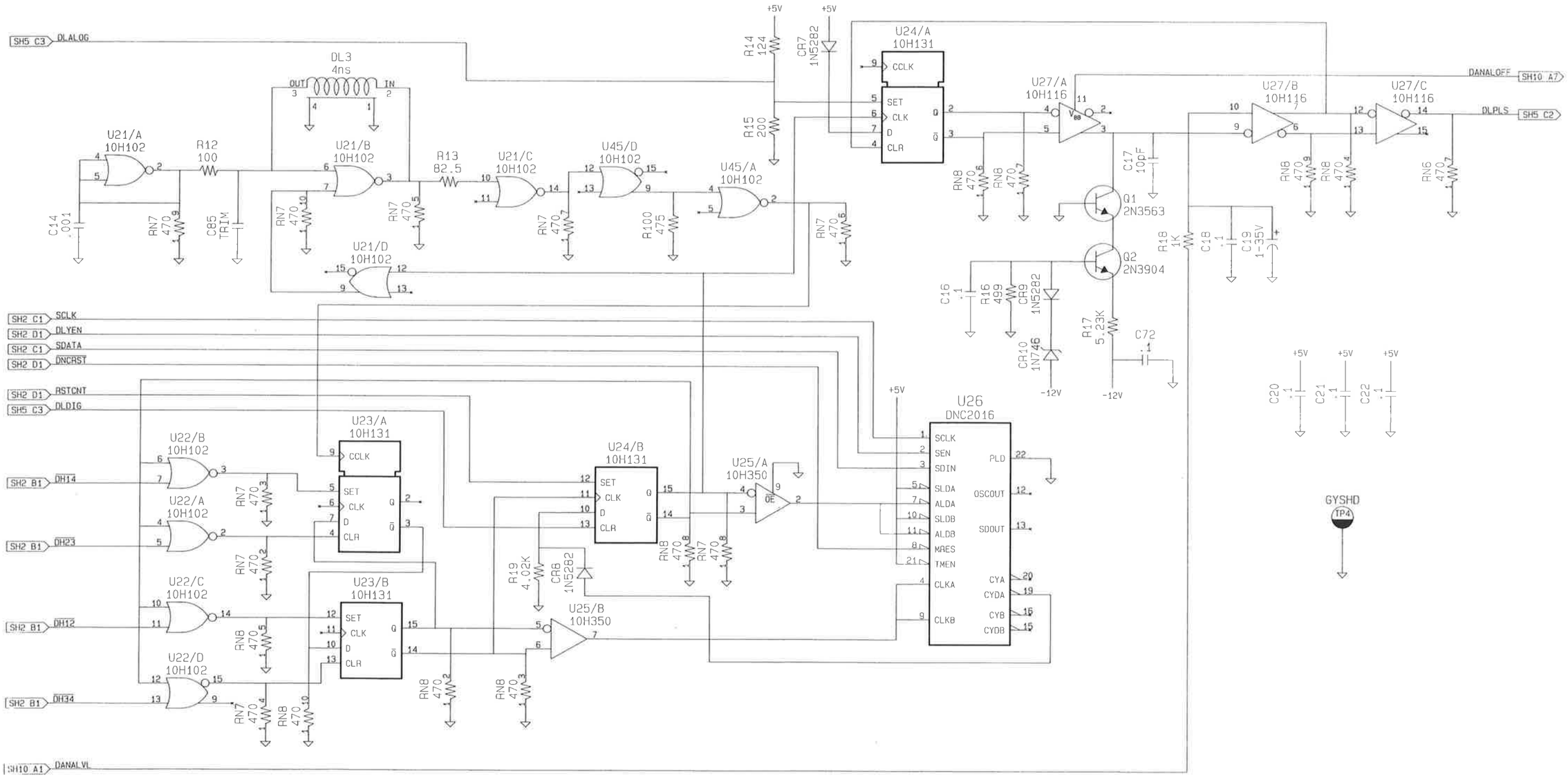
CAD JOB #: B074B

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN RO FIFER	DATE 5/91	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	CHECKED	6/20/91	TITLE: SCHEMATIC, PULSE BOARD
	PROJ. ENGR.	6/20/91	
	RELEASE APPROV.		
FINISH WAVETEK PROCESS	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES .XX ± .01 .XXX ± .005		SIZE D · FSCM NO. 23338 · DWG. NO. 1104-00-3438 · REV A
DO NOT SCALE DRAWING			SCALE NONE · MODEL 91 · SHEET 5 OF 11

1104-00-3438 A

REV	ECO	BY	DATE	APP

DELAY ONE SHOT



POWER DISTRIBUTION CHART

IC	U21	U22	U23	U24	U25	U26	U27	U45
+5V	1, 16	1, 16	1, 16	1, 16	1, 16	6, 18	1, 16	1, 16
GND	8	8	8	8	8	14, 17	8	8
PINS NOT USED	11, 13 15	9	2, 6 11	9		12, 13 15, 16 20	2, 15	3, 5, 6 7, 10, 11 13, 14, 15

NOTE UNLESS OTHERWISE SPECIFIED

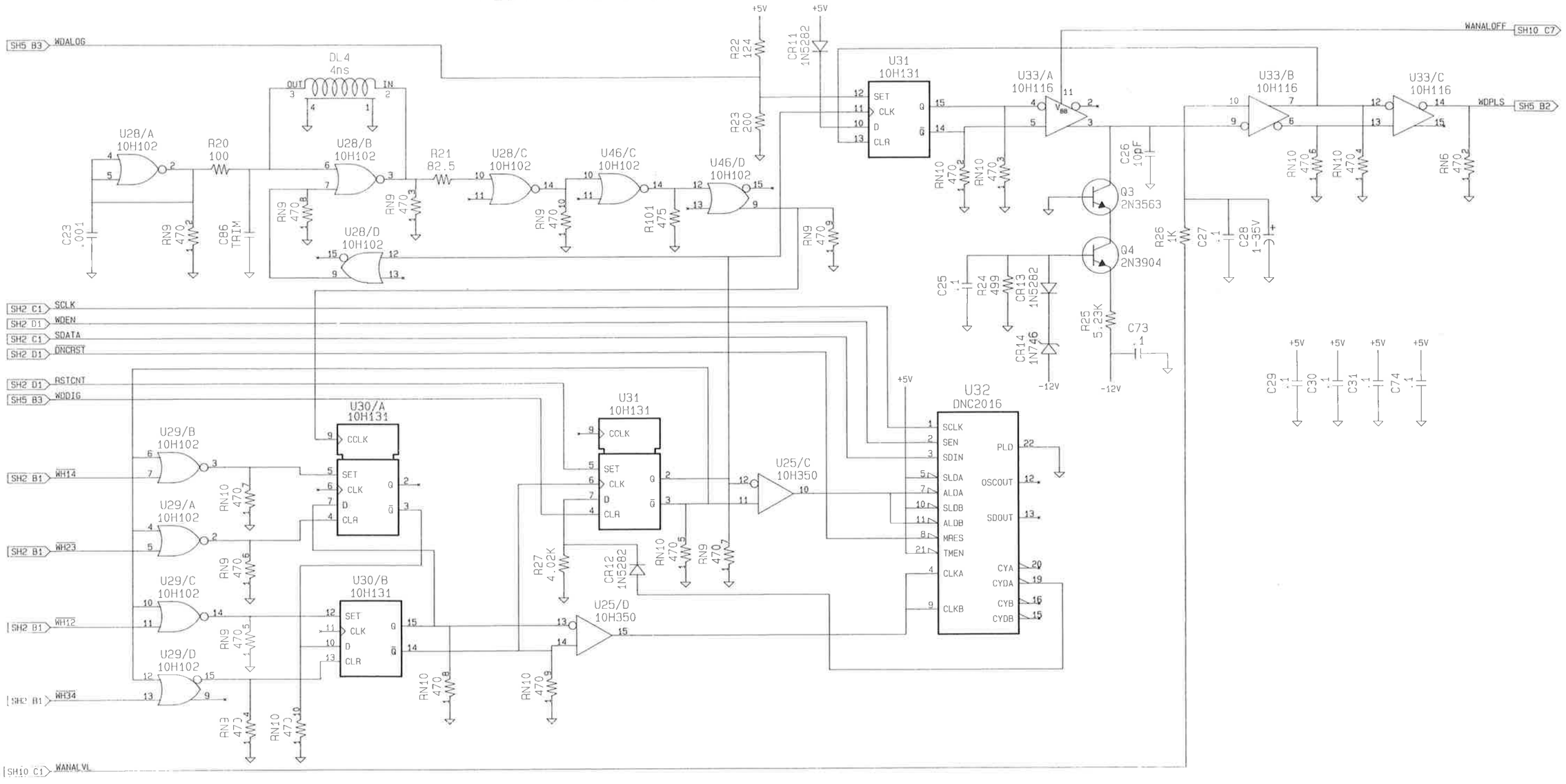
CAD JOB #: B074B

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN: RO FIFER	DATE: 5/91	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	CHECKED: JM	6/20/91	TITLE: SCHEMATIC, PULSE BOARD
	PROJ. ENGR.	6/20/91	
	RELEASE APPROV		
FINISH WAVETEK PROCESS	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES XX ± XXX ±		SIZE D | FSCM NO. 23338 | DWG. NO. 1104-00-3438 | REV A
DO NOT SCALE DRAWING			SCALE NONE | MODEL 91 | SHEET 6 OF 11

1104-00-3438 | A

REV	ECO	BY	DATE	APP

WIDTH ONE SHOT



POWER DISTRIBUTION CHART

IC	U28	U29	U30	U31	U32	U33	U46
+5V	1, 16	1, 16	1, 16	1, 16	6, 18	1, 16	1, 16
GND	8	8	8	8	14, 17	8	8
PINS NOT USED	11, 13 15	9	2, 6 11	9	12, 13 15, 16 20	2 15	5, 7 11, 13 15

NOTE UNLESS OTHERWISE SPECIFIED

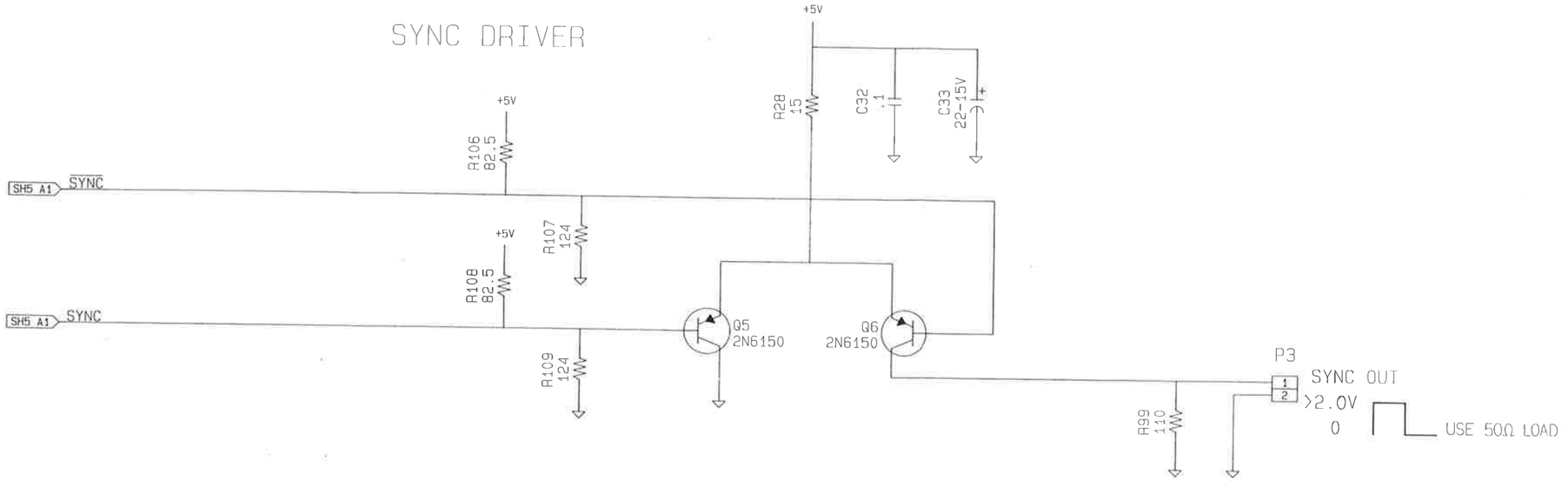
CAD JOB #: B074B

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN RO FIFER	DATE 5/91	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	CHECKED		TITLE SCHEMATIC, PULSE BOARD
	PROJ. ENGR.		
	RELEASE APPROV.		
FINISH WAVETEK PROCESS	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES .XX ± .XXX ± °		SIZE D FSCM NO. 23338 DWG. NO. 1104-00-3438 REV A
DO NOT SCALE DRAWING			SCALE NONE MODEL 91 SHEET 7 OF 11

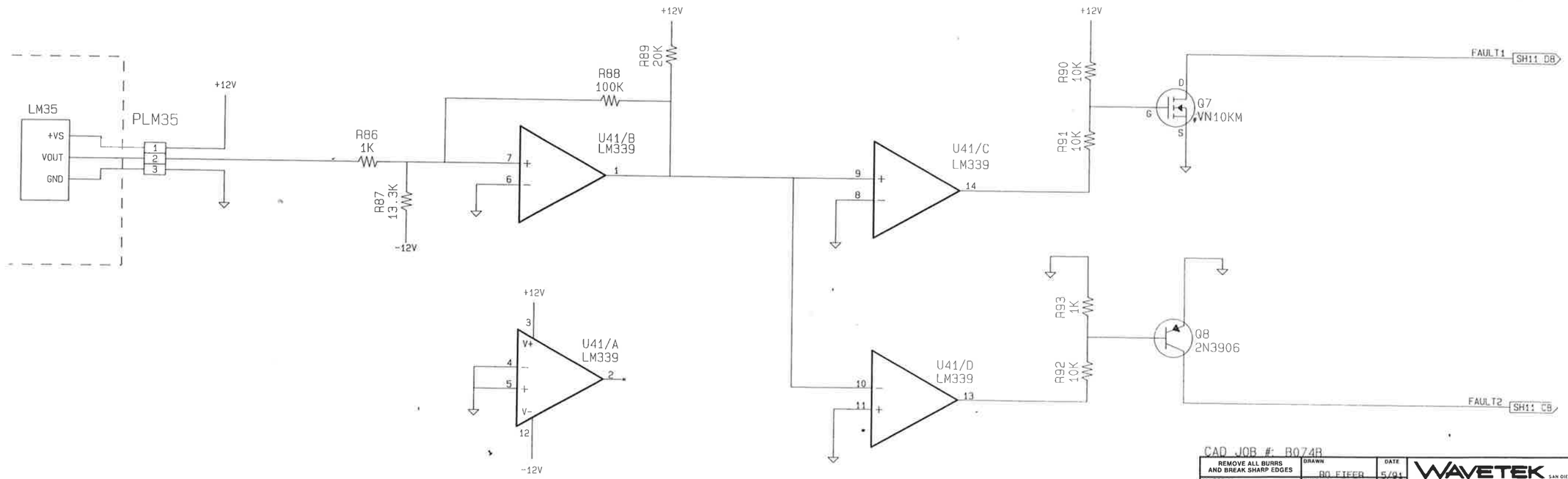
1104-00-3438 A

REV	ECO	BY	DATE	APP

SYNC DRIVER



OVERTEMPERATURE DETECTOR



NOTE UNLESS OTHERWISE SPECIFIED

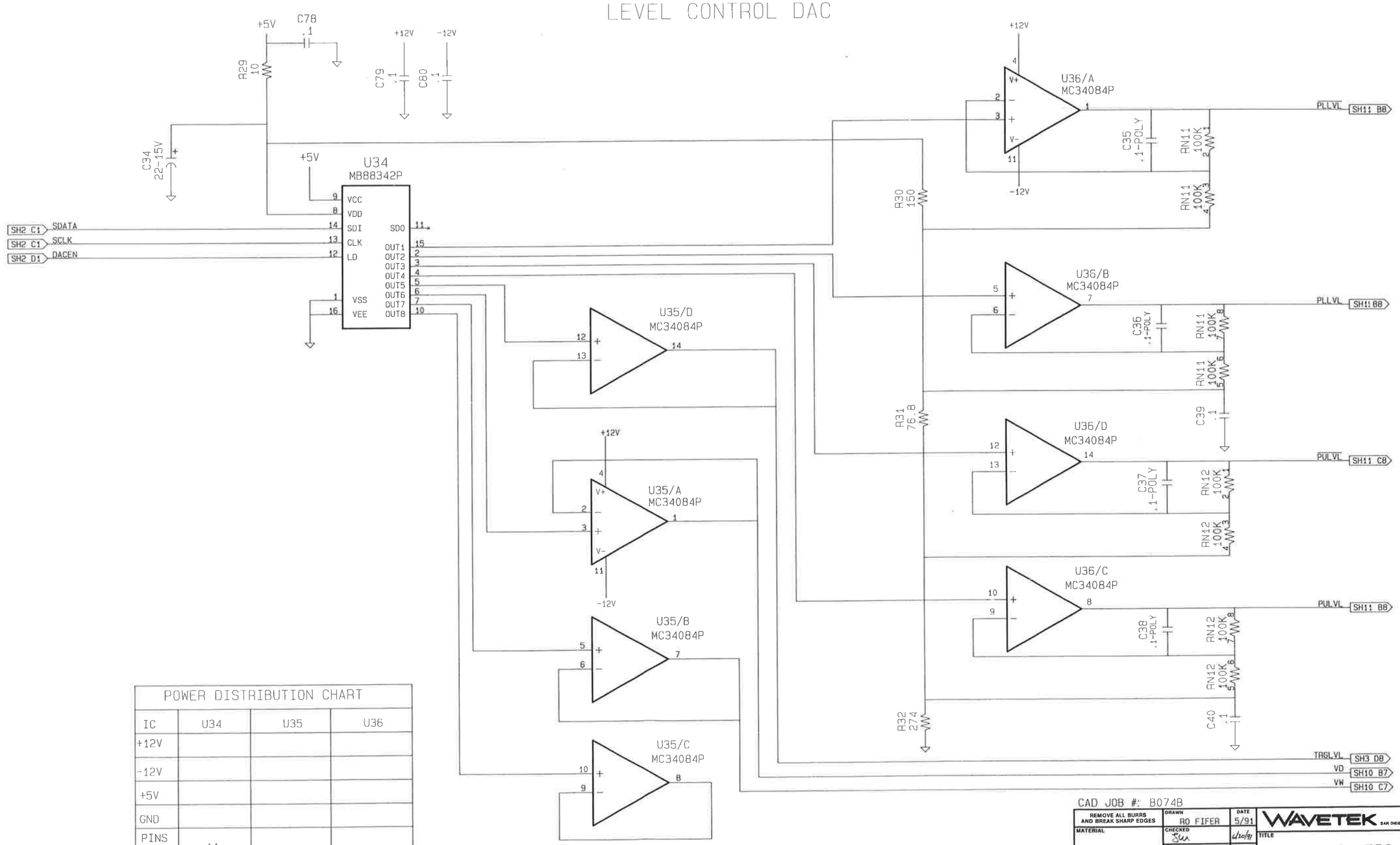
CAD JOB #: B074B

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN BO FIEFER	DATE 5/91	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	CHECKED Jim	6/20/91	TITLE SCHEMATIC, PULSE BOARD
	PROJ. ENGR.	6/20/91	
	RELEASE APPROV.		
FINISH WAVETEK PROCESS	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES XX ± .XXX ± °		SIZE D · FSCM NO. 23338 · DWG. NO. 1104-00-3438 · REV L
DO NOT SCALE DRAWING			SCALE NONE · MODEL 91 · SHEET 6 OF 11

1104-00-3438 A

REV	ECO	BY	DATE	APP

LEVEL CONTROL DAC



POWER DISTRIBUTION CHART			
IC	U34	U35	U36
+12V			
-12V			
+5V			
GND			
PINS NOT USED	11		

NOTE UNLESS OTHERWISE SPECIFIED

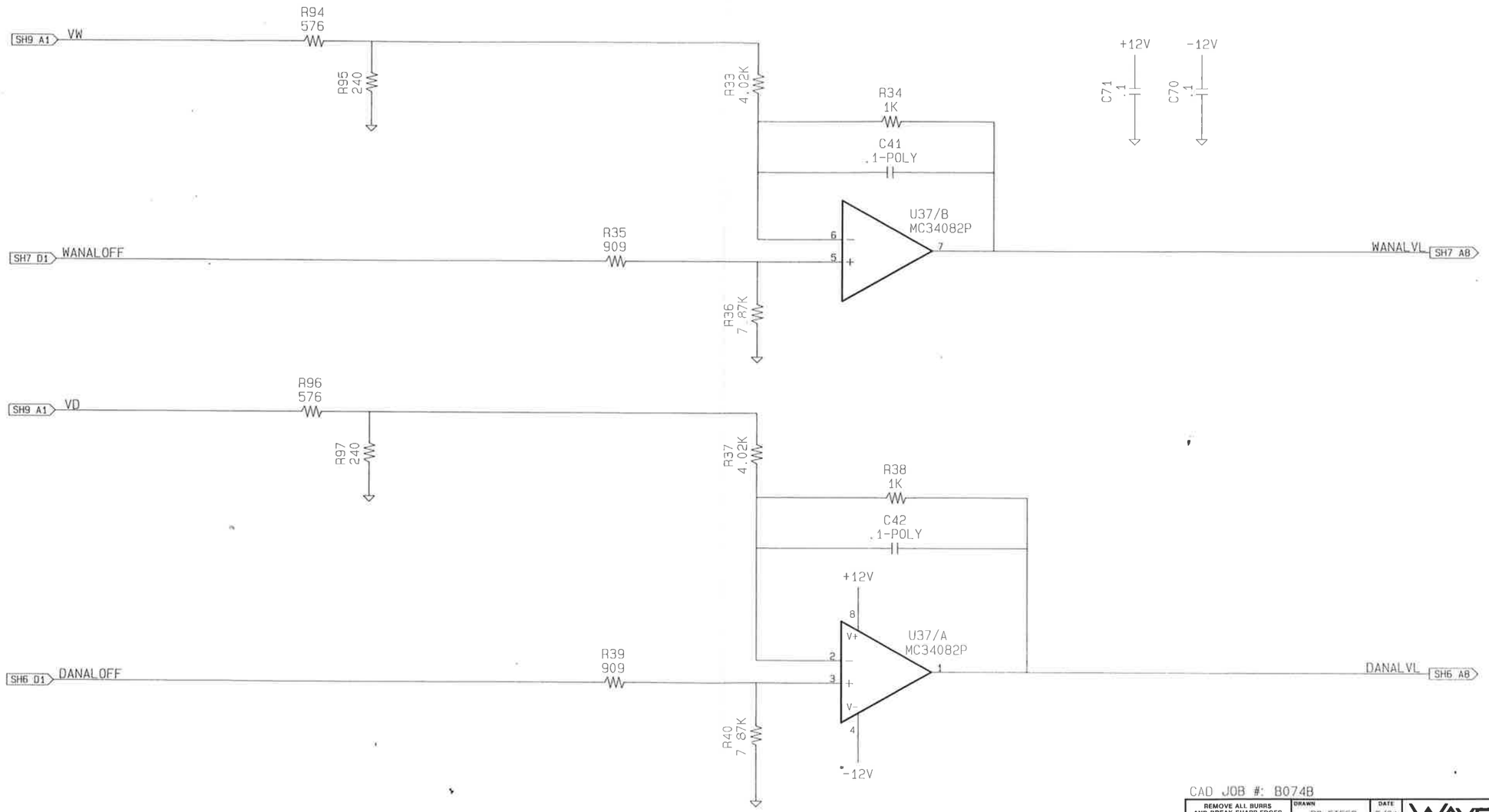
CAD JOB #: B074B

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN RO FIFER	DATE 5/91	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	CHECKED		TITLE
	PROJ. ENGR.	6/20/91	SCHEMATIC, PULSE BOARD
	RELEASE APPROV.		
FINISH WAVETEK PROCESS	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES .XX .XXX		SIZE D FSCM NO. 23338 DWG. NO. 1104-00-3438 REV A
DO NOT SCALE DRAWING			SCALE NONE MODEL 91 SHEET 9 OF 11

1104-00-3438 A

REV	ECO	BY	DATE	APP

ANALOG ONE SHOT CONTROL



NOTE UNLESS OTHERWISE SPECIFIED

CAD JOB #: B074B

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN RD FIFER	DATE 5/91	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	CHECKED		TITLE SCHEMATIC, PULSE BOARD
	PROJ. ENGR		
FINISH WAVETEK PROCESS	RELEASE APPROV		
DO NOT SCALE DRAWING	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES XX ± XXX ±		SIZE D · FSCM NO. 23338 · DWG. NO. 1104-00-3438 · REV A · SCALE NONE · MODEL 91 · SHEET 10 OF 11

1104-00-3438 A

REV	ECO	BY	DATE	APP

PULSE DRIVERS

U38 LT1086CT — IN, OUT, ADJ — +12V, +10.3V

U39 LT337AT — ADJ, IN, OUT — -12V, -5.8V

U40 PINDRVR

U8/C 10H116

Q9 2N5771, Q10 2N5771

SH8 B1 FAULT1

SH8 A1 FAULT2

SH2 B1 ENABLE

SH9 B1 PULVL

SH9 B1 PULVL

SH9 D1 PLLVL

SH9 C1 PLLVL

SH5 C1 PLS

SH5 C1 PLS

P4 DIE + TEMP −

P5 PULSE

P6 PULSE

OPTDVM1 SH1 B3

CALP SH2 B1

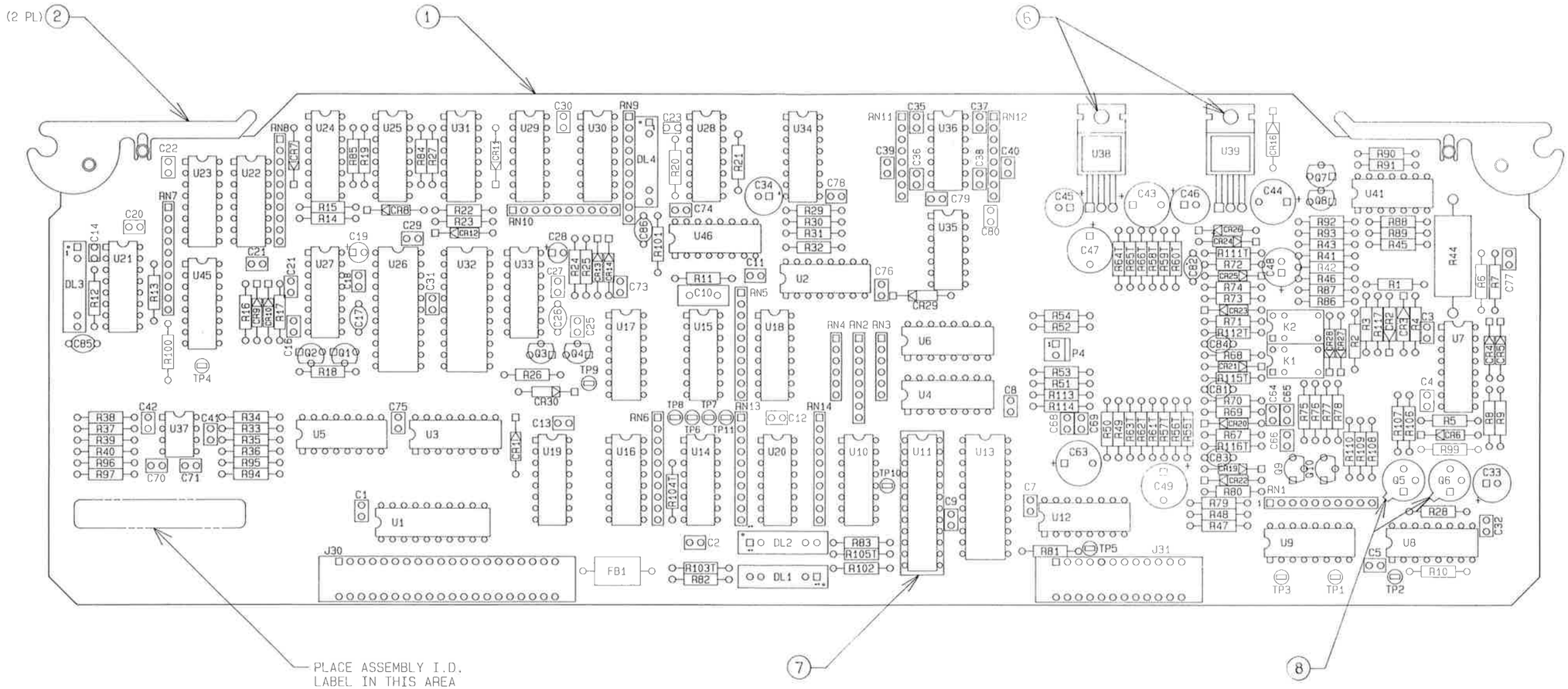
CALNP SH2 B1

CAD JOB #: B074B

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN BO FITER	DATE 5/91	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	CHECKED	6/20/91	TITLE SCHEMATIC, PULSE BOARD
	PROJ. ENGR.	6/24/91	
FINISH WAVETEK PROCESS	RELEASE APPROV.		
DO NOT SCALE DRAWING	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES .XX ± .XXX ± °		SIZE D FSCM NO. 23338 DWG. NO. 1104-00-3438 REV A SCALE NONE MODEL 91 SHEET 11 OF 11

NOTE UNLESS OTHERWISE SPECIFIED

REV	ECO	BY	DATE	APP
A	ERO 91-325			



4. ASSEMBLE PER WAVETEK WORKMANSHIP STANDARDS.
3. REFERENCE DESIGNATIONS DO NOT APPEAR ON PARTS.
2. FOR ASSEMBLY INTERCONNECTION, SEE INSTRUMENT SCHEMATIC.
1. SEE 1104-00-3438 FOR SCHEMATIC.

NOTE UNLESS OTHERWISE SPECIFIED

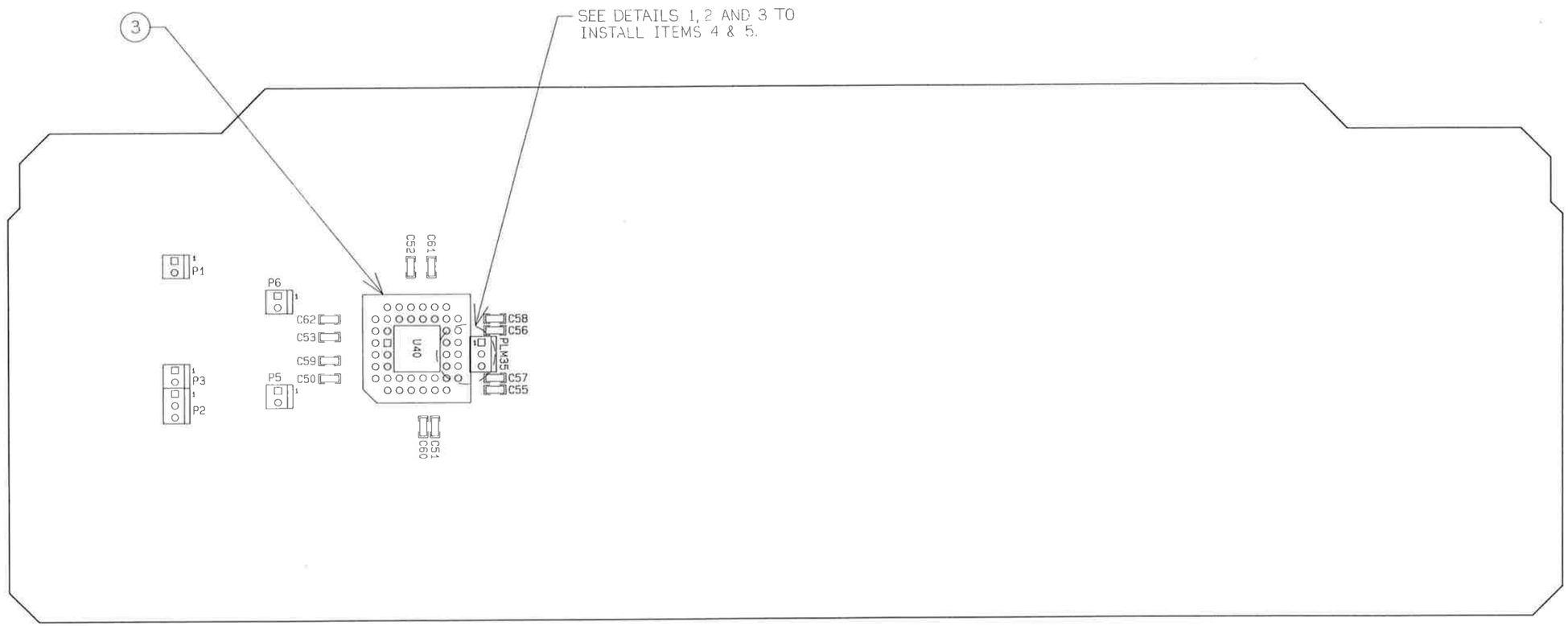
CAD JOB #: B074B

SEE SEPARATE PARTS LIST

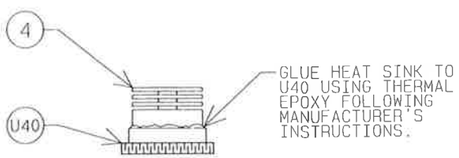
REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN Ro Fifer 6/91	WAVETEK SAN DIEGO, CALIFORNIA	
MATERIAL	CHECKED 6/20/91	TITLE	
	PROJ. ENGR. 6/24/91	PCA, PULSE BOARD	
FINISH WAVETEK PROCESS	RELEASE APPROV 7/30/91		
	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES .XX ±, .XXX ±, °	SIZE D / FSCM NO. 23338 / DWG. NO. 1101-00-3438 / REV A	
DO NOT SCALE DRAWING		SCALE 2/1 / MODEL 91 / SHEET 1 OF 2	

1101-00-3438 A

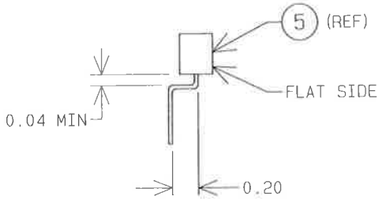
REV	ECO	BY	DATE	APP



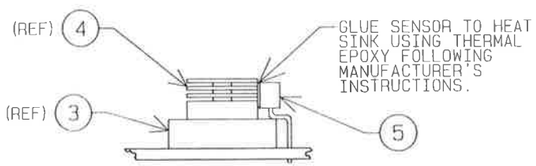
DETAIL 1
HEATSINK INSTALLATION



DETAIL 2
SENSOR LEAD PREP



DETAIL 3
SENSOR INSTALLATION



NOTE UNLESS OTHERWISE SPECIFIED

CAD JOB #: B074B

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN N.Fifer/A.T.	DATE 6/91	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	CHECKED JM	7/24/91	TITLE PCA, PULSE BOARD
	PROJ. ENGR. Gail McLea	7/24/91	
	RELEASE APPROV.		
FINISH WAVETEK PROCESS	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES .XX ± .XXX ± °		SIZE D · FSCM NO. 23338 · DWG. NO. 1101-00-3438 · REV A
DO NOT SCALE DRAWING			SCALE 2/1 · MODEL 91 · SHEET 2 OF 2

1101-00-3438 A

REV	ECO	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	A/D PULSE BD	1101-00-3438	WVTK	1101-00-3438	1
NONE	SCHEMATIC, PULSE BD	1104-00-3438	WVTK	1104-00-3438	1
R120	RES, MFLM 1.33K 1% 1/8W TO	RN55C1331F	KAGAN	111.1330	1
R119T	RES, MFLM 1.36K 1% 1/8W TO	NA	NA	111.1360	1
NONE	PULSE BD PREWAVE LOAD 91	1200-00-3438	WVTK	1200-00-3438	1
C50 C51 C52 C53 C55 C56 C57 C58 C59 C60 C61 C62	CAP, SMD CER +80-20% 25U 50V 0.1MF	C1206C104Z5UAC	KEMET	1500-81-0401	12
P2	CONN, HEADER, 3 PIN, .100 MTA	640456-3	AMP	2100-02-0116	1
P1 P3 P5 P6	HEADER 2 PIN, .025 CENTER, FRICTION LOCK	641126-2	AMP	2100-02-0284	4
3	SOCKET, IC, PLCC, 44PIN, THRU-HOLE	GILE44P-41OT	BURND	2100-03-1575	1
2	PC BD EJECTOR	87-2-C	BRIT	2800-07-0032	2
4	HEATSINK, IC-TYPE, LCC/FLT PAK, .655 SQ.	2281B	THERM	2800-11-0041	1
6	RIVET PLASTIC	231-080551-05-0101	FASTX	2800-60-0008	2
R210	RES, MF, 1/8W, 1%, 4.99K	RN55D-4991F	TRW	4701-03-4991	1

WAVETEK PARTS LIST | TITLE: PCA, PULSE BD | ASSEMBLY NO.: 1100-00-3438 | REV: F

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
5	CENTIGRADE TEMP SENSOR	LM35DZ	NAT	7000-00-3500	1
U39	REG, NEG, ADJ, 3 TERM, 1%	LT337AT	LTECH	7000-03-3702	1
U38	REGULATOR, POS. ADJ, LOW DROPOUT	LT1086CT	LINTE	7000-10-8600	1
U40	PIN DRIVER, HIGH SPEED	HL108020	HITEC	8010-80-2200	1
U11	PROG, GAL, USES 8000-22-1000 FOR MOD 91, REF U11, V1.0	8600-00-0681	WVTK	8600-00-0681	1

WAVETEK PARTS LIST | TITLE: PCA, PULSE BD | ASSEMBLY NO.: 1100-00-3438 | REV: F

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	CHECKED		TITLE: PCA PULSE BOARD
	PROJ. ENGR.		
FINISH WAVETEK PROCESS	RELEASE APPROV.		
DO NOT SCALE DRAWING	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±		SIZE D · FSCM NO. 23338 · DWG. NO. 1100-00-3438 · REV F · SCALE · MODEL 91 · SHEET 1 OF 1

REV	ECO	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
C83 C84	CAP,CER,10PF,1KV	DD-100LL	CRL	1500-01-0001	2
C17 C26	CAP, CER, DISC, 10PF,1KV, C0G,5%, RAD LD .25	10TCCG10	SPRAG	1500-01-0031	2
C14 C23	CAP,CER,.001 MF,+-10%,50V,X7R,.1" LS	SR155C102KAA	AVX	1500-01-0207	2
C1 C11 C12 C13 C16 C18 C2 C20 C21 C22 C25 C27 C29 C3 C30 C31 C32 C39 C4 C40 C5 C64 C65 C68 C69 C7 C70 C71 C72 C73 C74 C75 C76 C77 C78 C79 C8 C80 C9	CAP,CER,.1 MF,50V,X7R,+-10%,.1" LS	SR205C104KAA	AVX	1500-01-0415	39
C81 C82	CAP,CER,15PF,1KV	DD-150	CRL	1500-01-5011	2
C10	CAP,MICA,10PF,500V,1%	CM05CD100D03	CDE	1500-11-0006	1
C35 C36 C37 C38 C41 C42 C66	CAP,MET POLYS,.1MF,10%,63V,.1 "LS	MKS02-0.1MF-10%-63V	WIMA	1500-41-0418	7
C19 C28	CAP, TANT, 1MF, 35V	196D1050035HA1(DBS)	SPRAG	1500-71-0512	2
C33 C34 C45 C46 C48	CAP,TANT,22MF,15V	196D226X9015KA1(DBS)	SPRAG	1500-72-2601	5
C43 C44 C47	CAP,TANT 27UF,35V+/-10%,0.25LS	199D276X9035FE4	SPRAG	1500-72-7602	3
C49 C63	CAP,TANT,47MF,20V	196D476X9020PE4(DBS)	SPRAG	1500-74-7601	2

WAVETEK PARTS LIST | TITLE: PULSE BD PREWAVE LOAD 91 | ASSEMBLY NO. 1200-00-3438 | REV F

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
K1 K2	RELAY,1 FORMC,5V,.312H,.296W	HD1E-M-DC5V	AROMT	4500-00-0034	2
R44	RES,C,2W,5% 10	RC42GF100J	AB	4700-43-1009	1
R75 R76	RES,MF,1/8W,.1%,100	RN55E1000BJ	PHLP	4701-02-1000	2
R77	RES,MF,1/8W,.1%,15K	5033RE1502B	MEPCO	4701-02-1502	1
R78	RES,MFILM,.1%,1/8W,75 K OHM	CMF-55-7502BT1	DALE	4701-02-7502	1
R10 R105 R12 R20 R4	RES,MF,1/8W,1%,100	RN55D-1000F	TRW	4701-03-1000	5
R1 R114 R18 R26 R34 R38 R41 R6 R7 R86 R93	RES,MF,1/8W,1%,1K	RN55D-1001F	TRW	4701-03-1001	11
R90 R91 R92	RES,MF,1/8W,1%,10K	RN55D-1002F	TRW	4701-03-1002	3
R88	RES,MF,1/8W,1%,100K	RN55D-1003F	TRW	4701-03-1003	1
R29 R51 R52 R53 R54 R69 R70 R73 R74 R79 R80	RES,MF,1/8W,1%,10	5043ED10R100F	MEPCO	4701-03-1009	11
R55 R56 R59 R60 R61 R62 R66 R99	RES,MFILM,1%,1/8W,100 PPM,110 OHM	CMF-55-1100-FT1	DALE	4701-03-1100	8
R42 R46	RES,MF,1/8W,1%,121	RN55D-1210F	TRW	4701-03-1210	2
R68 R72	RES,MFLM,1/8W,1%,12.1	5033RD12R1F	MEPCO	4701-03-1219	2
R107 R109 R14 R22 R64	RES,MF,1/8W,1%,124	RN55D-1240F	TRW	4701-03-1240	5

WAVETEK PARTS LIST | TITLE: PULSE BD PREWAVE LOAD 91 | ASSEMBLY NO. 1200-00-3438 | REV F

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R113 R19 R27 R33 R37	RES,MF,1/8W,1%,4.02K	RN55D-4021F	TRW	4701-03-4021	5
R117	RES,MF,1/8W,1%,4.12K	RN55D-4121F	TRW	4701-03-4121	1
R45	RES,MFILM,1/8W(1/4W@70 OC),1%,442 OHM	CCF55-4420F	DALE	4701-03-4420	1
R100 R101 R102 R84 R85	RES,MF,1/8W,1%,475	5033RD4750F	MEPCO	4701-03-4750	5
R16 R2 R24 R50 R8 R9 R94 R96	RES,MF,1/8,1%,499	RN55D-4990F	TRW	4701-03-4990	8
R47 R48	RES,MF,1/8W,1%,49.9	RN55D-49R9F	CORNG	4701-03-4999	2
R17 R25 R3	RES,MF,1/8W,1%,5.49K	RN55D-5491F	MEPCO	4701-03-5491	3
R112T	RES,MF,1/8W,1%,56.2	RN55D-56R2F	TRW	4701-03-5629	1
R49	RES,MF,1/8W,1%,5.76K	RN55D-5761F	TRW	4701-03-5761	1
R115T	RES,MF,1/8W,1%,59	RN55D-59R0F	TRW	4701-03-5909	1
R43	RES,MF,1/8W,1%,6.98K	RN55D-6981F	TRW	4701-03-6981	1
R57 R58	RES,MFLM,1/8W,1%,75	5033RD75R0F	MEPCO	4701-03-7509	2
R36 R40	RES,MF,1/8W,1%,7.87K	RN55D-7871F	TRW	4701-03-7871	2
R106 R108	RES,MF,1/8W,1%,82.5	RN55D-82R5F	TRW	4701-03-8259	2
R81	RES,MF,1/8W,1%,90.9	RN55D-90R9F	TRW	4701-03-9099	1

WAVETEK PARTS LIST | TITLE: PULSE BD PREWAVE LOAD 91 | ASSEMBLY NO. 1200-00-3438 | REV F

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
1	PULSE BD REF; SPEC 0008-00-0455 REV C	1700-00-3438	WVTK	1700-00-3438	1
DL2	DELAY LINE, 10 NS, 50 OHM	1513-10A	DDD	1800-00-0048	1
DL3 DL4	DLY LINE,PASSIVE,4 NSEC,188 OHM,SNL-IN-LN	EP123109	PCA	1800-00-0051	2
DL1	DELAY LINE,50NS,100NS	1513-50B	DDD	1800-00-0053	1
J31	CONN,HEADER,24 PIN,RECPT,2X12,.1 CTR, PCMT	102585-7	AMP	2100-02-0255	1
J30	CONN,HEADER,40 PIN,RECPT,2X20,.1 CTR PCMT	1-102585-2	AMP	2100-02-0256	1
7	SOCKET,DUAL BEAM,LO RISE, 24 PIN	802-0241642	WELCN	2100-03-0088	1
TP1 TP4 TP6	TEST POINT,BLK,PC	TP-104-01-00	COMPO	2100-04-0054	3
TP10 TP11 TP2 TP3 TP5 TP7 TP8 TP9	TEST POINT,RED,PC	TP-104-01-02	COMPO	2100-04-0055	8
8	TRANSIPAD	10123N(DBS)	METRS	2800-11-0003	2
FB1	BALUN CORE,FERRITE,680 OHMS	2943666671	FARIT	3100-00-0017	1

WAVETEK PARTS LIST | TITLE: PULSE BD PREWAVE LOAD 91 | ASSEMBLY NO. 1200-00-3438 | REV F

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R87	RES,MF,1/8W,1%,13.3K	RN55D-1332F	TRW	4701-03-1332	1
R30	RES,MF,1/8W,1%,150	RN55D-1500F	TRW	4701-03-1500	1
R28 R67 R71	RES,MF,1/8W,1%,15	RN55D-15R0F	TRW	4701-03-1509	3
R5	RES,MF,1/8W,1%,1.62K	RN55D-1621F	TRW	4701-03-1621	1
R63	RES,MF,1/8W,1%,165	RN55D-1650F	TRW	4701-03-1650	1
R104 R15 R23 R65	RES,MF,1/8W,1%,200	RN55D-2000F	TRW	4701-03-2000	4
R89	RES,MF,1/8W,1%,20K	RN55D-2002F	TRW	4701-03-2002	1
R35 R39	RES,MF,1/8W,1%,2.21K	RN55D-2211F	TRW	4701-03-2211	2
R95 R97	RES,MF,1/8W,1%,240	RN55D-2400F	MEPCO	4701-03-2400	2
R11	RES,MF,1/8W,1%,249	RN55D-2490F	TRW	4701-03-2490	1
R32	RES,MF,1/8W,1%,274	RN55D-2740F	TRW	4701-03-2740	1
R116T	RES,MF,1/8W,1%,27.4	RN55D-27R4F	TRW	4701-03-2749	1
R111T	RES,MF,1/8W,1%,30.1	RN55D-30R1F	TRW	4701-03-3019	1
R13 R21	RES,MF,1/8W,1%,332	RN55D-3320F	TRW	4701-03-3320	2
R82 R83	RES,MF RN55D 365 OHM 1%	5043ED365R0F	MEPCO	4701-03-3650	2
R110	RES,MF,1/8W,1%,39.2	RN55D-39R2F	TRW	4701-03-3929	1

WAVETEK PARTS LIST | TITLE: PULSE BD PREWAVE LOAD 91 | ASSEMBLY NO. 1200-00-3438 | REV F

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R31	RESISTOR, METAL FILM, 1/8W., 1%, 76.8 OHM	CT4-76R8-1%	CORNO	4701-23-7689	1
RN1 RN10 RN13 RN14 RN5 RN6 RN7 RN8 RN9	RES NETWORK 470 10PIN SIP BUSS	4310R-101-471	BOURN	4770-00-0009	9
RN2	RES NETWORK,SIP,ISOL,270 OHM,4 RES	4608X-102-271	BOURN	4770-00-0067	1
RN3	RES NETWORK,SIP,BUSSED,82 0 OHM,5 RES	4606-101-821	BOURN	4770-00-0068	1
RN4	RES NETWORK,SIP,BUSSED,18 0 OHM,5 RES	4606X-101-181	BOURN	4770-00-0069	1
RN11 RN12	RES NETWORK,8-PIN,ISOL,10 0K	4608X-102-104F	BOURN	4770-00-0100	2
CR10 CR14	DIODE, ZENER, 3.3V, 5% TOL,500MW,Q/B,IN746A	1N746A	FAIR	4801-01-0746	2
CR4 CR5 CR6	DIODE, ZENOR, 5.1V, 500MW, QIB, IN751A	1N751A	FAIR	4801-01-0751	3
CR1 CR11 CR12 CR13 CR19 CR20 CR21 CR22 CR23 CR24 CR25 CR26 CR27 CR28 CR29 CR30 CR7 CR8 CR9	DIODE, HIGH CONDUCTANCE, ULTRA FAST	1N5282	FAIR	4801-01-5282	19

WAVETEK PARTS LIST | TITLE: PULSE BD PREWAVE LOAD 91 | ASSEMBLY NO. 1200-00-3438 | REV F

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	CHECKED		TITLE: PULSE BD PREWAVE LOAD
	PROJ. ENGR.		
	RELEASE APPROV.		
FINISH WAVETEK PROCESS	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±		SIZE D | FSCM NO. 23338 | DWG. NO. 1200-00-3438 | REV F
DO NOT SCALE DRAWING			SCALE | MODEL 91 | SHEET 1 OF 2

REV	ECO	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
CR16	TRANSIENT ABSORBER, 6.8V	P6KE6.8A	MOT	4801-02-0009	1
CR2 CR3	DIODE, ULTRA FAST	1N4244	T/C&F	4807-02-0777	2
Q1 Q3	TRANS, NPN, TO-92	2N3563	FAIR	4901-03-9630	2
Q2 Q4	TRANS 2N3904 NPN GENERAL PURPOSE TO-92	2N3904	FAIR	4901-03-9040	2
Q8	TRANS 2N3906 PNP GENERAL PURPOSE TO-92	2N3906(OBS)	FAIR	4901-03-9060	1
Q5 Q6	TRANS	2N5160-18(OBS)	MOT	4901-05-1600	2
Q10 Q9	TRANS 2N5771 PNP SWITCH TO-92	2N5771	NSC	4901-05-7710	2
Q7	TRANS	VN10KM	SLCON	4902-00-0100	1
U41	COMPARATORS, QUAD VOLTAGE	0665-00364	WVTK	7000-03-3900	1
U34	DAC, OCTAL, 8-BIT, SERIAL	M88B342-P	FUJI	7000-88-3420	1
U7	COMPARATOR, HIGH SPEED, ECL	AD96685BQ	AD	7000-96-6850	1
U37	OP AMP, HI SLEW RTE, WIDEBND, JFET DUAL	MC34082P	MOT	7003-40-8200	1

WAVETEK PARTS LIST | TITLE: PULSE BD PREWAVE LOAD 91 | ASSEMBLY NO. 1200-00-3438 | REV F

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
U35 U36	OP AMP, HI SLEW RTE, WIDEBND JFET	MC34084P	MOT	7003-40-8400	2
U12	FLIP FLOP, DUAL J-K, NEG EDGE TRIG	74F112PC	NSC	8000-74-0112	1
U1	FLIP-FLOP, OCTAL, D-TYPE, HCT-CMOS, TTL INP	MC74HCT574AN	MOT	8000-74-5741	1
U2 U3 U4 U5 U6	SHFT REG, 8-BIT, CMOS, OUTPUT CLR	SN74HC595N	TI	8000-74-5950	5
U15 U16 U21 U22 U28 U29 U45 U46 U9	MECL 10KH HIGH-SPEED ECL	MC10H102P	MOT	8001-01-0201	9
U19	XOR/XNOR, MECL, 2-INPUT, TRIPLE	MC10H107P	MOT	8001-01-0701	1
U27 U33 U8	RECEIVER-TRIP LN ECL	MC10H116P	MOT	8001-01-1601	3
U14 U18 U20	GATE, OR AND/OR AND INVER DUAL WIDE, ECL	MC10H121P	MOT	8001-01-2100	3
U17 U23 U24 U30 U31	FLIP-FLOP, DUAL D, MAS/SL, ECL	MC10H131P	MOT	8001-01-3101	5
U10 U25	TRANSLATOR, ECL TO TTL	MC10H350P	MOT	8001-03-5000	2
U13 U26 U32	GATE ARRAY, COUNTER, SYNCH, MULTI-MODE, 32-BIT	CLA530478A	PLESS	8700-00-0005	3

WAVETEK PARTS LIST | TITLE: PULSE BD PREWAVE LOAD 91 | ASSEMBLY NO. 1200-00-3438 | REV F

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT

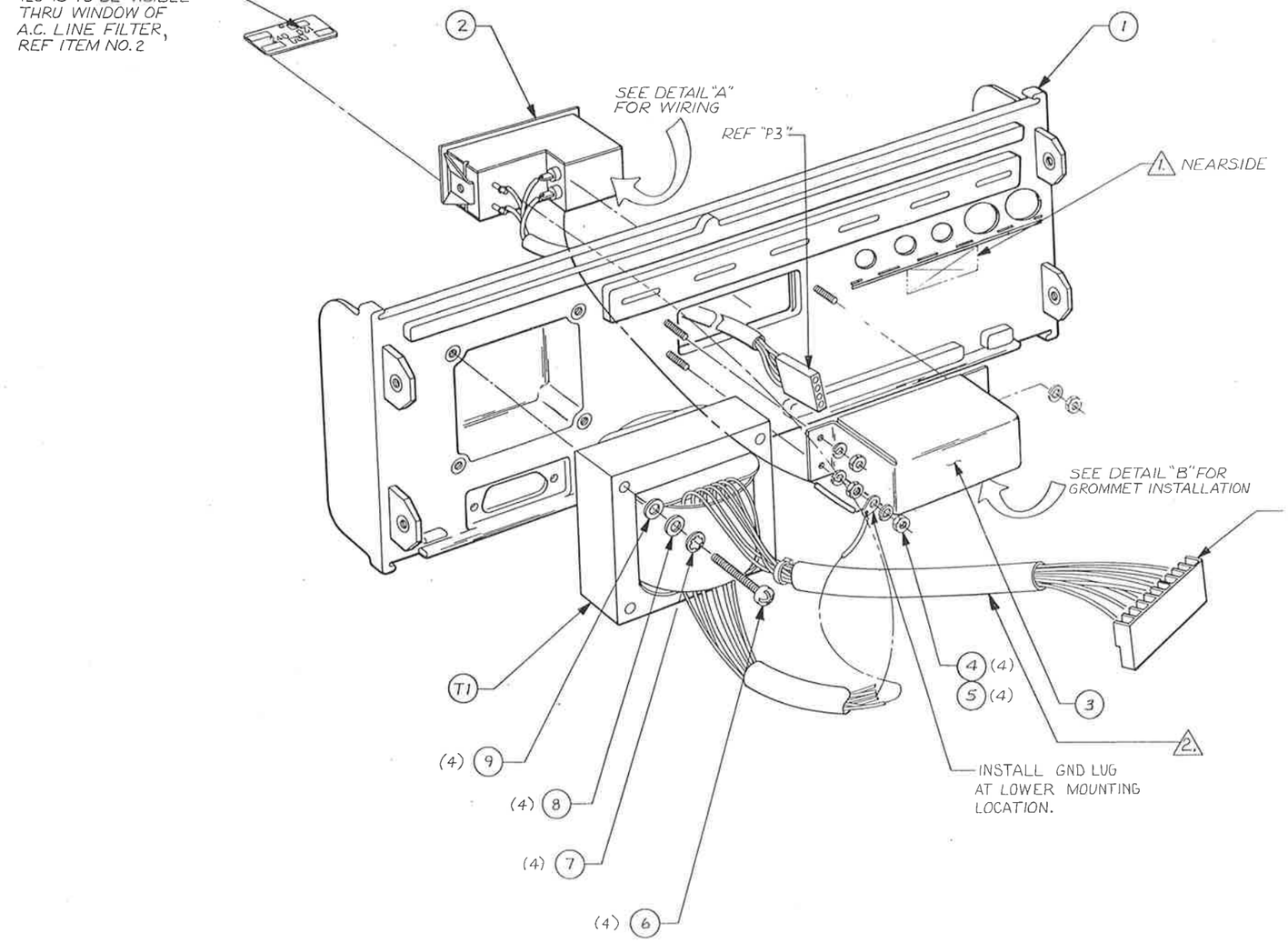
WAVETEK PARTS LIST | TITLE: PULSE BD PREWAVE LOAD 91 | ASSEMBLY NO. 1200-00-3438 | REV F

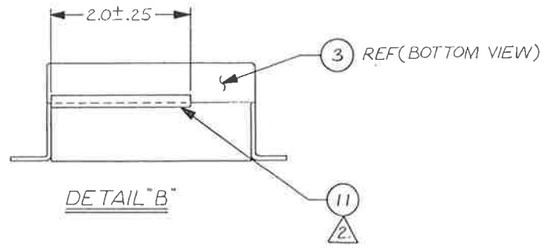
NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	CHECKED		TITLE: PULSE BD PREWAVE LOAD 91
	PROJ. ENGR.		
	RELEASE APPROV.		
FINISH WAVETEK PROCESS	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES .XX ± .XXX ± ±		SIZE D | FSCM NO. 23338 | DWG. NO. 1200-00-3438 | REV F
DO NOT SCALE DRAWING			SCALE | MODEL 91 | SHEET 2 OF 2

MODIFIED FROM DWG 1101-00-3325

REV	ECO	BY	DATE	APP
A	ERO NO. 91-328	MT	3/21	

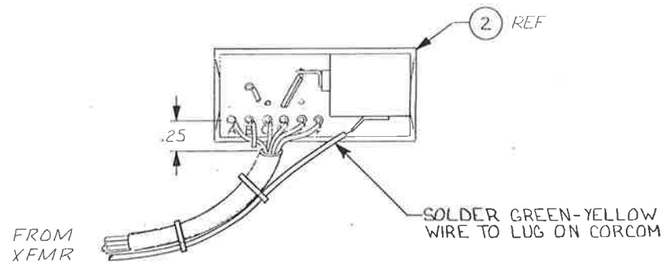




DETAIL "B"

WIRE LIST

XFMR WIRE COLOR	LINE FILTER TERM. MARKING
VIOLET	A
BLACK	C
GRAY	D
WHT/BLK	E
WHT/GRAY	F



DETAIL 'A'
XFMR WIRE HOOKUP

SEE SEPARATE PARTS LIST

2. INSTALL GROMMET 3200-06-0079 (LESIG PART 924) OR 3200-06-0053 (MINOR RUBBER PART NO. ZX-4064) OR EQUIV. TO SHIELD (ITEM 3) WITH ADHESIVE 1600-03-0013 (LOCTITE PART NO. 414) OR EQUIV.

1. MARK ASSEMBLY NO. "1101-00-3441," LATEST REV, AND DATE CODE , PER MIL-STD-130, APPROX WHERE SHOWN.

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN RO FIFER	DATE 4-8-91	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL —	CHECKED M. S. Muth	6/20/91	TITLE ASSEMBLY, REAR PANEL
	PROJ ENGR Jean C McGee	7/12/91	
	RELEASE APPROV M. S. Muth	7/12/91	
FINISH WAVETEK PROCESS —	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES XX ± .03 XXX ± .010 ± 1°		SIZE D | FSCM NO. 23338 | DWG. NO. 1101-00-3441 | REV A
DO NOT SCALE DRAWING			SCALE NONE | MODEL 91 | SHEET 1 OF 1

1101-00-3441

REV	ECO	BY	DATE	APP

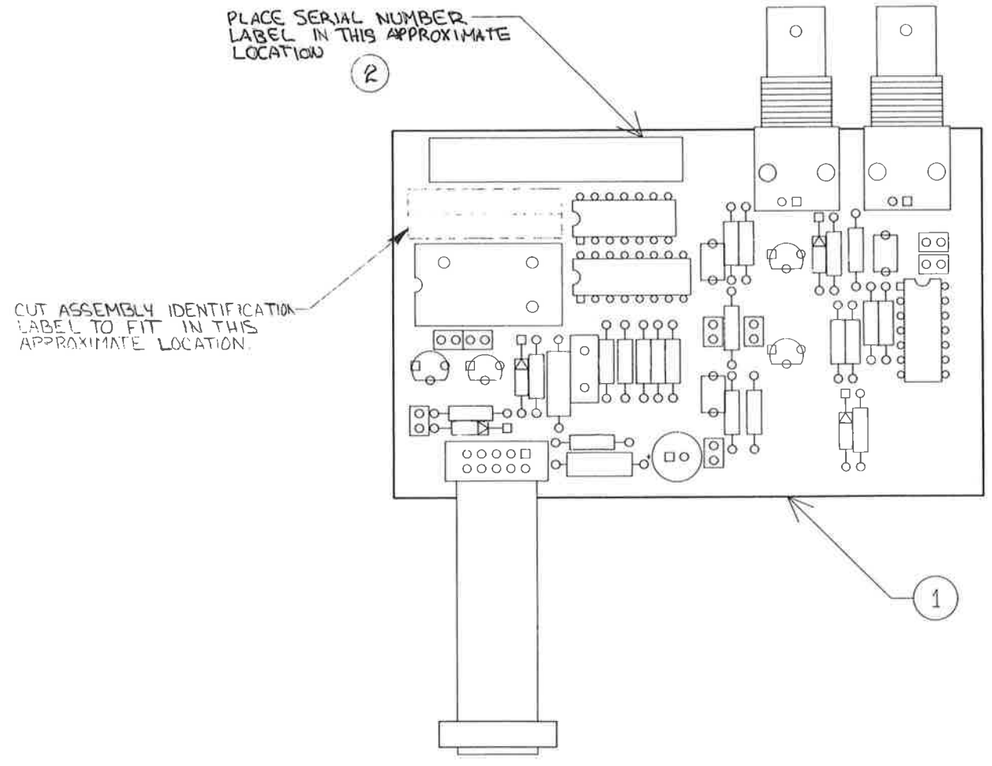
REFERENCE DESIGNATORS	PART DESCRIPTION	DRIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NA	A/D REAR PANEL-91	1101-00-3441	WVTK	1101-00-3441	1
2	LINE FILTER CABLE ASSY	1200-00-3508	WVTK	1200-00-3508	1
3	SHIELD, AC CONN	1400-02-3463	WVTK	1400-02-3463	1
1	REAR PANEL PAINTED			1400-02-5144	1
4	NUT, HEX, 4-40	MS35649-244	COML	2800-14-4100	4
9	WASHER, #8 FIBER SIN 470	#8 FIBER WASHER	CMRCL	2800-28-8000	4
6	PAN HD, PLIP, 8-32x2 1/2, STAINLESS	8-32 x 2 1/2 PAN	CMRCL	2800-38-8322	4
5	WASHER, LOCK REG, 8/8 #4	MS 35338-135	CMRCL	2800-45-4000	4
8	WASHER, #8, FLT, SS, THK .050, ID .174, OD .375	2800-46-8000	CMRCL	2800-46-8000	4
7	WASHER, #8, INT TOOTH, LOCK, SS	2800-56-0002	CMRCL	2800-56-0002	4
11	EXTRU, RUBBER, U CHNL, 1/16 INSIDE, 1/8 OUTSIDE	924	LESIG	3200-06-0079	2
T1	TRANSFORMER, POWER, MODEL 91	5600-00-0051	ENSIG	5600-00-0051	1

WAVETEK PARTS LIST	TITLE	ASSEMBLY NO.	REV
	REAR PANEL ASSY - 91	1100-00-3441	B
		PAGE 1	

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	CHECKED		TITLE: REAR PANEL ASSY - 91
	PROJ. ENGR.		
	RELEASE APPROV.		
FINISH WAVETEK PROCESS	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES .XX ± .XXX ± ±		SIZE D; FSCM NO. 23338; DWG. NO. 1100-00-3441; REV B
DO NOT SCALE DRAWING			SCALE; MODEL 91; SHEET 1 OF 1

REV	ECO	BY	DATE	APP
A	ERO 91-380	NS	8-13	AM



SEE SEPARATE PARTS LIST

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN Ro Fifer	DATE 8/13/91	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	CHECKED		TITLE: PCA, TCXO OPT-001 BD
	PROJ ENGR	8/19/91	
FINISH WAVETEK PROCESS	RELEASE APPROV	8/13/91	
DO NOT SCALE DRAWING	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES ± .XX ± .XXX ± °		SIZE D · FSCM NO. 23338 · DWG. NO. 1001-00-J663 · REV A · SCALE 2/1 · MODEL 91 · SHEET 1 OF 1

REV	ECO	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	A/D TCXO BD-OPTION 001	1001-00-0663	WVTK	1001-00-0663	1
1	PCA, TCXO BD-91	1100-00-3466	WVTK	1100-00-3466	1
2	SERIAL TAG	1400-01-6950	WVTK	1400-01-6950	1

WAVETEK PARTS LIST | TITLE: TCXO BD-OPTION 001 | ASSEMBLY NO. 1000-00-0663 | REV A
PAGE 1

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	A/D TCXO BD-91	1101-00-3466	WVTK	1101-00-3466	1
NONE	SCHEMATIC, TCXO BD-91	1104-00-3466	WVTK	1104-00-3466	1
NONE	TCXO OPT BD PREWAVE LOAD 91	1200-00-3466	WVTK	1200-00-3466	1
2	CABLE ASSY, RIBBON, 10 PIN, PCB-TO-IDC	6002-00-0051	WVTK	6002-00-0051	1

WAVETEK PARTS LIST | TITLE: PCA, TCXO BD-91 | ASSEMBLY NO. 1100-00-3466 | REV B
PAGE 1

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R19	RES, MF, 1/8W, 1%, 249	RN55D-2490F	TRW	4701-03-2490	1
R15 R18	RES, MF, 1, 8W, 1%, 46, 4	RN55D-46R4F	TRW	4701-03-4649	2
R13 R20	RES, MF, 1/8, 1%, 499	RN55D-4990F	TRW	4701-03-4990	2
R5	RES, MF, 1/8W, 1%, 4, 99K	RN55D-4991F	TRW	4701-03-4991	1
R12	RES, MF, 1/8W, 1%, 750	RN55D-7500F	TRW	4701-03-7500	1
R14 R17	RES, MF, 1/8W, 1%, 825	RN55D-8250F	TRW	4701-03-8250	2
R3	RES, 0 OHM JUMPER	JP02T680	ROHM	4799-00-0087	1
CR1 CR2	DIODE, HIGH CONDUCTANCE, ULTRA FAST	1N5282	FAIR	4801-01-5282	2
CR3 CR4	DIODE 5082-2811 SCHOTTKY, 15V, 20MA	5082-2811	HP	4809-02-2811	2
Q1 Q4	TRANS 2N3904 NPN GENERAL PURPOSE TO-92	2N3904	FAIR	4901-03-9040	2
Q3	TRANS 2N3906 PNP GENERAL PURPOSE TO-92	2N3906(OBS)	FAIR	4901-03-9060	1
Q2	TRANS	VN10KM	SLCON	4902-00-0100	1
U1	COMPARATOR, DUAL DIFFERENTIAL, SENSE AMP	NE521N	SIG	7000-05-2100	1

WAVETEK PARTS LIST | TITLE: TCXO OPT BD PREWAVE LOAD 91 | ASSEMBLY NO. 1200-00-3466 | REV
PAGE 2

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
C11 C13 C2 C4 C5 C7 C8 C9	CAP, CER, .1 MF, 50V, X7R, +-10%, .1" LS	SR205C104KAA	AVX	1500-01-0415	8
C10 C12 C3	CAP, CER, 470PF, 1KV	DD-471	CRL	1500-04-7111	3
C6	CAP, MICA, 75PF, 500V	DM15-750J	ARCO	1500-17-5000	1
C1	CAP, TANT, 22MF, 15V	196D226X9015KA1(OBS)	SPRAG	1500-72-2601	1
1	PCB, TCXO BD REF: SPEC 0008-00-0455 REV C	1700-00-3466	WVTK	1700-00-3466	1
L2	CHOKE, 3.3MH, 10%	1537-24	DLVAN	1800-00-0006	1
L1	INDUCTOR, 390MH	2500-08	DELVN	1800-00-0023	1
J2 J3	CONN, BNC(PC)	227161-1	AMP	2100-01-0019	2
U2	OSCILLATOR, TEMP COMPENSATED 10MHZ XTAL, 14 PIN DIP, 0.030 LEADS	740B2A1	MONIT	2300-99-0026	1
NONE	NUT, HEX, 1/2-28	1-329631-2	AMP	2800-16-0025	2
R2 R4 R7	RES, MF, 1/8W, 1%, 100	RN55D-1000F	TRW	4701-03-1000	3
R10 R6 R8 R9	RES, MF, 1/8W, 1%, 1K	RN55D-1001F	TRW	4701-03-1001	4
R1 R11	RES, MF, 1/8W, 1%, 10K	RN55D-1002F	TRW	4701-03-1002	2
R16	RES, MF, 1/8W, 1%, 1.21K	RN55D-1211F	TRW	4701-03-1211	1

WAVETEK PARTS LIST | TITLE: TCXO OPT BD PREWAVE LOAD 91 | ASSEMBLY NO. 1200-00-3466 | REV
PAGE 1

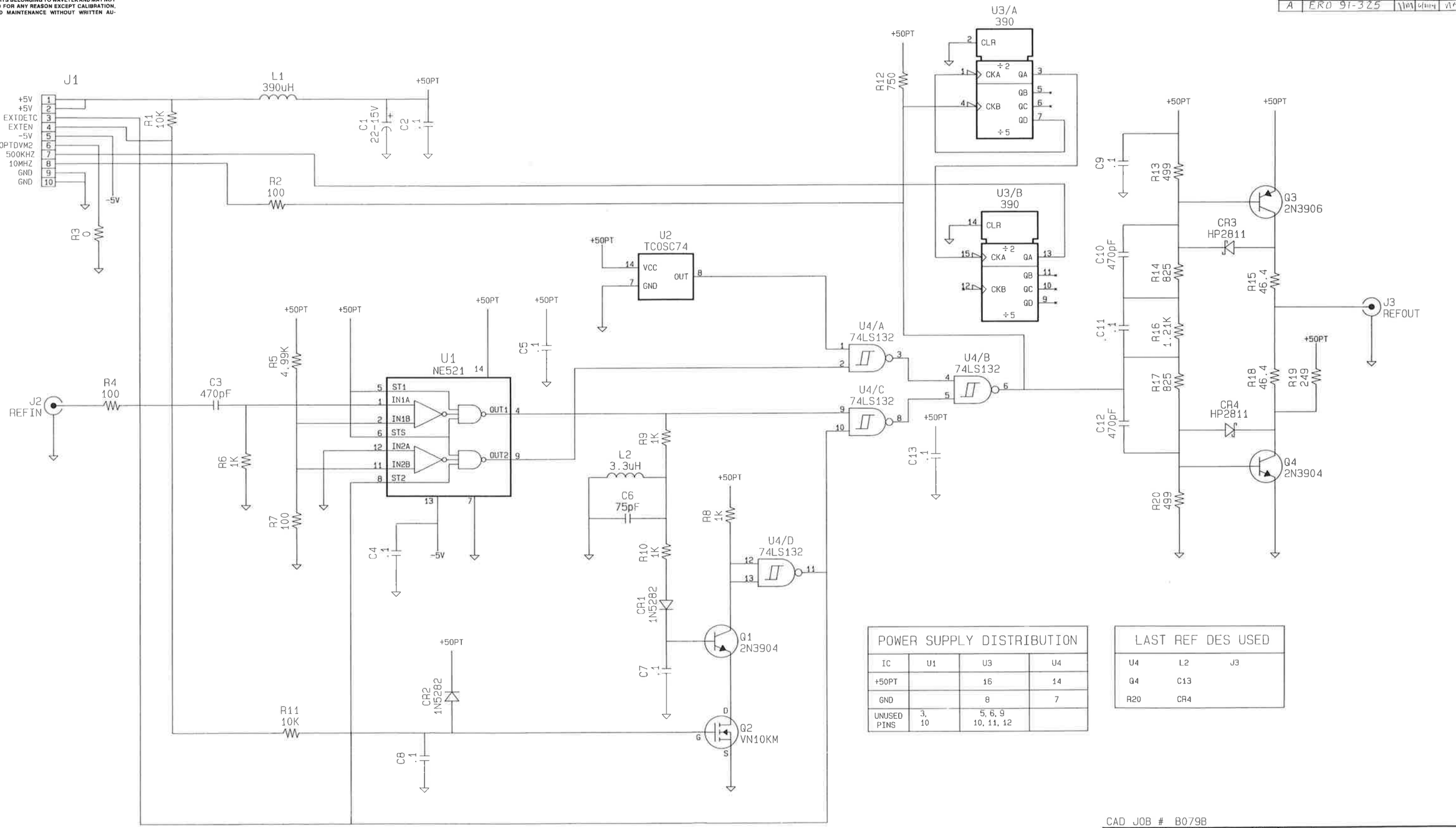
REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
U4	GATE, NAND, QUAD S/TRIG, TTL	74LS132	TI	8007-41-3210	1
U3	COUNTER, DUAL 4B BCD, TTL	74LS390PC	FAIR	8007-43-9010	1

WAVETEK PARTS LIST | TITLE: TCXO OPT BD PREWAVE LOAD 91 | ASSEMBLY NO. 1200-00-3466 | REV
PAGE 3

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	CHECKED		TITLE: TCXO BD OPTION 001
	PROJ. ENGR.		
	RELEASE APPROV.		
FINISH WAVETEK PROCESS	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES .XX ± .XXX ± °		SIZE D | FSCM NO. 23338 | DWG. NO. 1000-00-0663 | REV A
DO NOT SCALE DRAWING			SCALE | MODEL 91 | SHEET 1 OF 1

REV	ECO	BY	DATE	APP
A	ERO 91-325	WA	4/30/91	WA



POWER SUPPLY DISTRIBUTION			
IC	U1	U3	U4
+50PT		16	14
GND		8	7
UNUSED PINS	3, 10	5, 6, 9 10, 11, 12	

LAST REF DES USED		
U4	L2	J3
Q4	C13	
R20	CR4	

3. RESISTORS ARE VALUED IN OHMS, 1/8W, 1%.
2. CAPACITORS ARE VALUED IN MICROFARADS (uF).
1. FOR UNIT INTERCONNECTION, SEE INSTRUMENT SCHEMATIC.

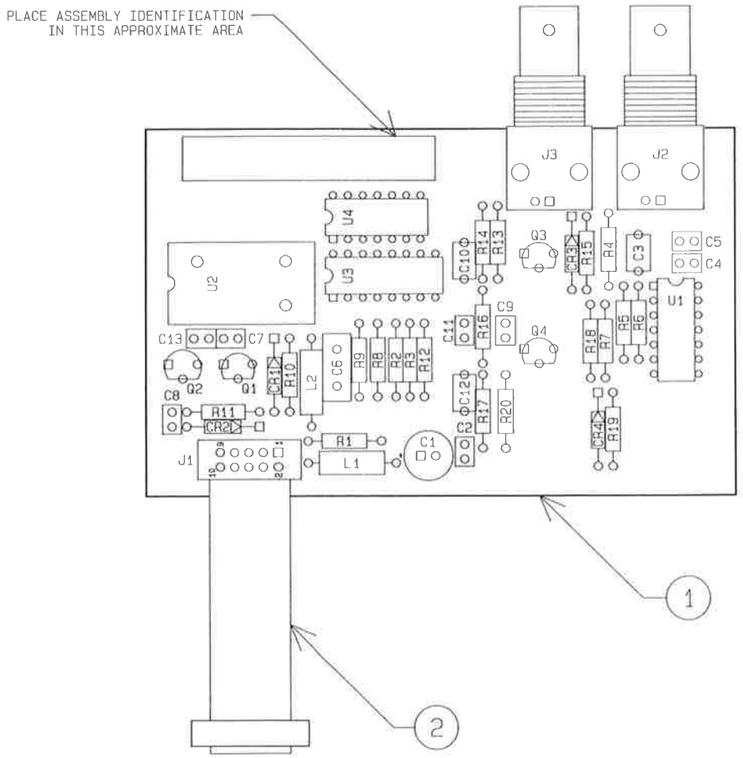
NOTE UNLESS OTHERWISE SPECIFIED

CAD JOB # B079B

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN RD FIFER	DATE 5/3/91	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	CHECKED JWL	4/30/91	TITLE SCHEMATIC, TCXO OPT.-001 BD
FINISH WAVETEK PROCESS	PROJ. ENGR. Joel E. Nelson	6/24/91	
	RELEASE APPROV. N. K. Null	6/24/91	
DO NOT SCALE DRAWING	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES ± .XX ± .XXX ± ±		SIZE D · FSCM NO. 23338 · DWG. NO. 1104-00-3466 · REV A · SCALE NONE · MODEL 91 · SHEET 1 OF 1

1104-00-3466 A

REV	ECO	BY	DATE	APP
A	EKO 91-325			



1. ASSEMBLE PER WAVETEK WORKMANSHIP STANDARDS.
3. REFERENCE DESIGNATIONS DO NOT APPEAR ON PARTS.
2. FOR ASSEMBLY INTERCONNECTION, SEE INSTRUMENT SCHEMATIC.
1. SEE 1104-00-3466 FOR SCHEMATIC.

NOTE UNLESS OTHERWISE SPECIFIED

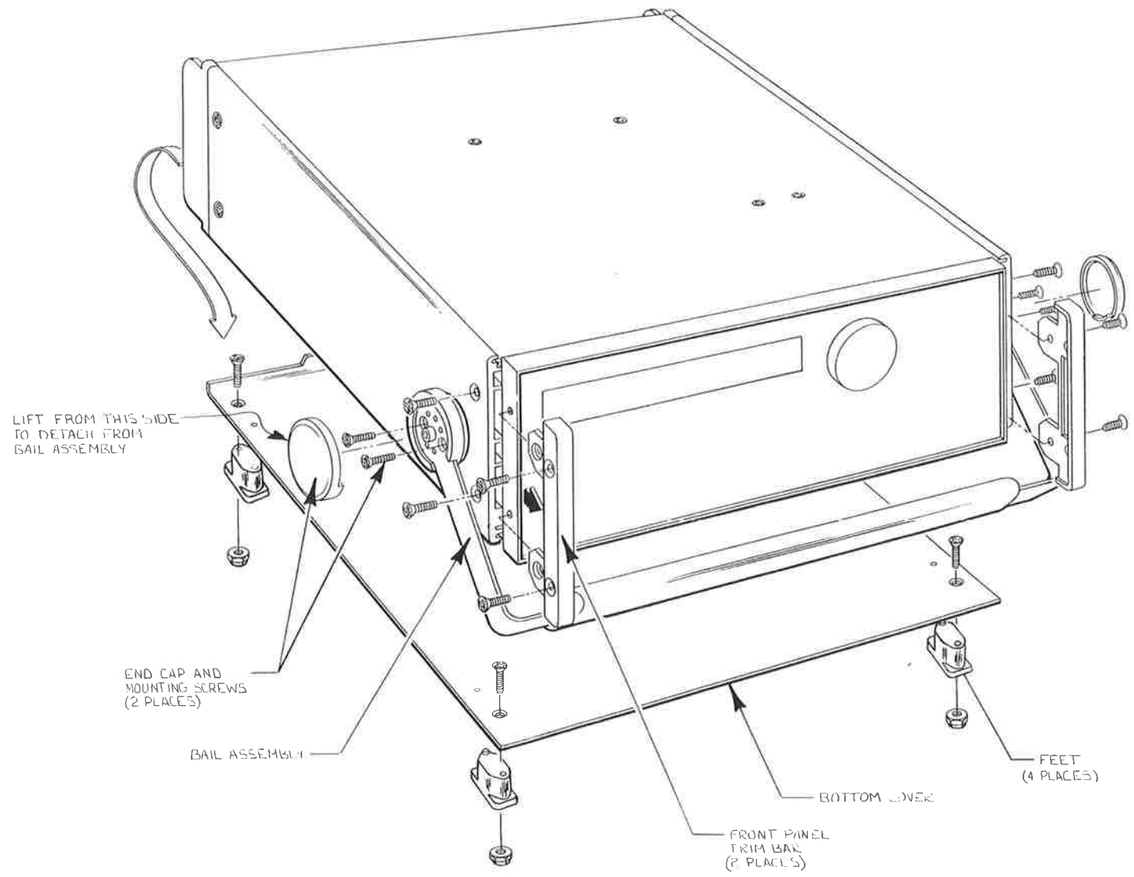
CAD JOB #: B0798 SEE SEPARATE PARTS LIST

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN: Ro Fifer 5/91	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	CHECKED: JM 6/20/91	TITLE: PCA, TCXO OPT-001 BD
	PROJ. ENGR: 6/20/91	
FINISH WAVETEK PROCESS	RELEASE APPROV: 6/20/91	
DO NOT SCALE DRAWING	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES XX ± XXX ± °	SIZE D; FSCM NO. 23338; DWG. NO. 1101-00-3466; REV A; SCALE 2/1; MODEL 01; SHEET 1 OF 1

REV	ECO	BY	DATE	APP
A	ERO NO. 90-441	AP	4/4/90	[illegible]
B	ECO # 90-519	MS	7/1/90	[illegible]
C	ECO # 90-536	MS	7/13/90	[illegible]

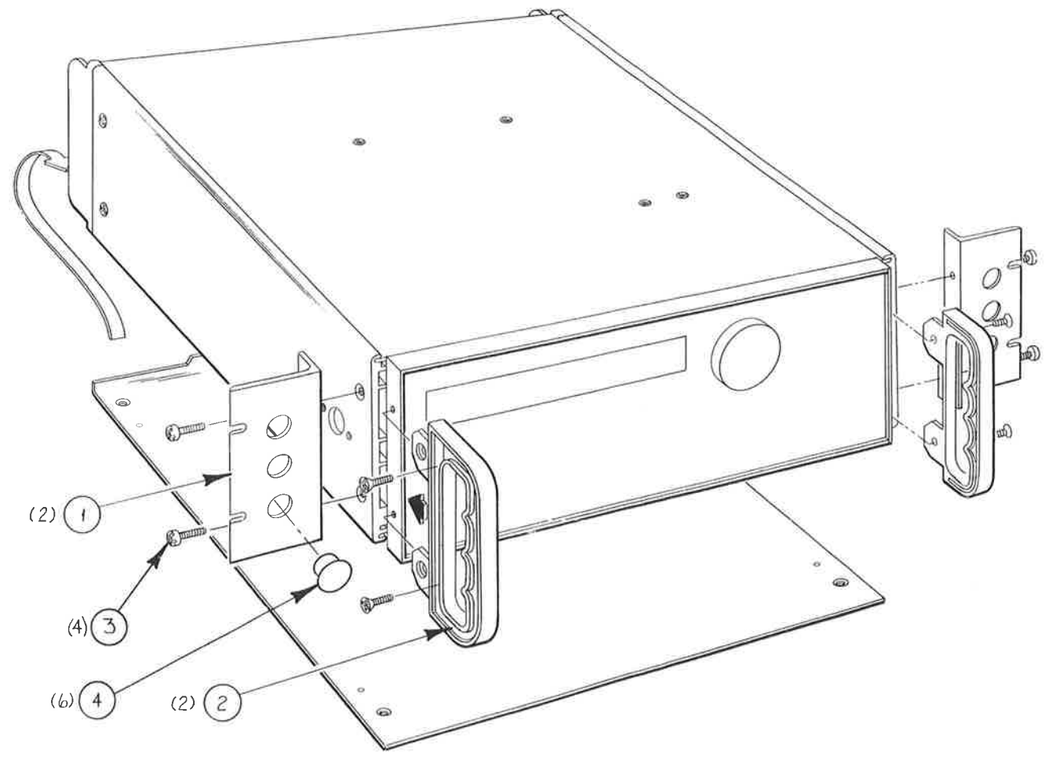
DISASSEMBLY OF STANDARD ITEMS

1. REMOVE BAIL ASSEMBLY BY PLACING IN POSITION AS SHOWN.
2. REMOVE END CAP AND MOUNTING SCREWS (2 ON EACH SIDE).
3. REMOVE BOTTOM COVER.
4. REMOVE FEET (4 PLACES).
5. REMOVE FRONT PANEL TRIM BARS BY REMOVING 4 MOUNTING SCREWS EACH SIDE, AS SHOWN.



ASSEMBLY OF RACK/HANDLE KIT

1. INSTALL BOTTOM COVER
2. INSTALL HANDLE ITEM 2 (2 PLACES) (ATTACH WITH FORWARD SET OF SCREWS ONLY)
3. INSTALL RACK EAR ITEM 1 (2 PLACES) USING ITEM 3 SCREWS (DIFFERENT FROM SCREWS THAT WERE REMOVED DURING STEP 5 OF DISASSEMBLY).
4. INSTALL HOLE PLUGS, ITEM 4 (6 PLACES).



SEE SEPARATE PARTS LIST

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN D. COOPER	DATE 5-11-90	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL —	CHECKED		TITLE: RACK / HANDLE KIT
	PROJ. ENGR.		
FINISH WAVETEK PROCESS —	RELEASE APPROV.	6/29/90	
DO NOT SCALE DRAWING	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES .XX ± .1 .XXX ± .1 ° 1		SIZE D · FSCM NO. 23338 · DWG. NO. 1101-00-3353 · REV C · SCALE NONE · MODEL 90/95 · SHEET 1 OF 1

1101-00-3353 C

REV	ECO	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
REF	A/D, RACK HANDLE KIT	1101-00-3353	WVTK	1101-00-3353	1
2	HANDLE, PTD	1400-02-3252	WVTK	1400-02-3252	2
1	RACKEAR 90/95	1400-02-3101	WVTK	1400-02-3101	2
4	HOLE PLUG, .562 DIA., BLK	DP562BLK/2653	HEYCO	2800-35-0010	6
3	SCREW, PAN, CAD I, CROSS RECESS, 8-32 X 5/8	8-32 X 5/8 PAN	CMRCL	2800-38-8110	4

WAVETEK PARTS LIST	TITLE	ASSEMBLY NO.	REV
	RACK/HANDLE KIT, OPTION 003	1100-00-3353	A
		PAGE 1	

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	CHECKED		TITLE: RACK HANDLE KIT OPTION 003
	PROJ. ENGR.		
	RELEASE APPROV.		
FINISH WAVETEK PROCESS	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES .XX ± .XXX ±		SIZE D · FSCM NO. 23338 · DWG. NO. 1100-00-3353 · REV A
DO NOT SCALE DRAWING			SCALE · MODEL 91 · SHEET 1 OF 1

REV	ECO	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	ENCODER KNOB ASSY REF: A/D 1201-00-3380	1200-00-3380	WVTK	1200-00-3380	1
NONE	SL ZR 6.2V 5% 400MW (1N753A)	1N753A	ROHM	131.9620	1
NONE	CONN, BNC(PC)	227161-1	AMP	2100-01-0019	2
NONE	FUSE, 3/4A, 250V, S-B	313-750	LITFU	2400-05-0011	5
NONE	FUSE, 1 1/2A, 250V, S-B	MDX 1-1/2	BUSS	2400-05-0021	5
NONE	RELAY, 2 FORMC, 5V, DIP 14	DF2E-DC5V	AROMT	4500-00-0033	1
NONE	RELAY, 1 FORMC, 5V, .312H, .296W	HD1E-M-DC5V	AROMT	4500-00-0034	1
NONE	DIODE, ZENER, 3.3V, 5% TOL, 500MW, Q/B, IN746A	1N746A	FAIR	4801-01-0746	1
NONE	DIODE, ZENOR, 5.1V, 500MW, QIB, IN751A	1N751A	FAIR	4801-01-0751	1
NONE	DIODE, HIGH CONDUCTANCE, ULTRA FAST	1N5282	FAIR	4801-01-5282	2
3	DIODE, 1N4002 GEN PURPOSE RECT. 100V, 1A	1N4002	FAIR	4801-02-0001	1
NONE	DIODE, ULTRA FAST	1N4244	T/CSF	4807-02-0777	1

WAVETEK PARTS LIST	TITLE	ASSEMBLY NO.	REV
	SPARES KIT 91	1200-00-3480	A
		PAGE 1	

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	TRANS 2N2219A NPN GENERAL PURPOSE TO-5	2N2219A	NSC	4901-02-2191	2
NONE	TRANS 2N2905A PNP GENERAL PURPOSE TO-5	2N2905A	NSC	4901-02-9051	2
NONE	TRANS, NPN, TO-92	2N3563	FAIR	4901-03-5630	2
NONE	TRANS	2N3866	MOT	4901-03-8660	2
NONE	TRANS	2N5160-1B(OBS)	MOT	4901-05-1600	2
NONE	TRANS 2N5583 PNP HIGH FREQ TO-39	2N5583	MOT	4901-05-5830	2
NONE	TRANS 2N5771 PNP SWITCH TO-92	2N5771	NSC	4901-05-7710	2
NONE	TRANS, NPN, HIGH FREQ	2N5943	MOT	4901-05-9430	1
NONE	TRANS, FET N CHANNEL	VN0106N3	SUPER	4902-01-0600	2
NONE	TRANS, FET P CHANNEL	VP0106N3	SUPER	4902-01-0601	2
NONE	TRANS	4902-02-5730	WVTK	4902-02-5730	1
NONE	TRANS	4902-02-5740	WVTK	4902-02-5740	1
NONE	VOLT REGULATOR, 3 TERMINAL ADJUSTABLE POS	LM317T	NSC	7000-03-1700	1

WAVETEK PARTS LIST	TITLE	ASSEMBLY NO.	REV
	SPARES KIT 91	1200-00-3480	A
		PAGE 2	

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	REG, NEG, ADJ, 3 TERM, 1%	LT337AT	LTECH	7000-03-3702	1
NONE	COMPARATOR, DUAL DIFFERENTIAL, SENSE AMP	NE521N	SIG	7000-05-2100	1
NONE	REGULATOR, POS. ADJ, LOW DROPOUT	LT1086CT	LINTE	7000-10-8600	1
NONE	DAC, OCTAL, 8-BIT, SERIAL	MB88342-P	FUJI	7000-88-3420	1
NONE	OP AMP, HI SLEW RTE, WIDEBND, JFET, STD	MC34081P	MOT	7003-40-8100	2
NONE	OP AMP, HI SLEW RTE, WIDEBND, JFET DUAL	MC34082P	MOT	7003-40-8200	2
NONE	OP AMP, HI SLEW RTE, WIDEBND JFET	MC34084P	MOT	7003-40-8400	1
NONE	MECL 10KH HIGH-SPEED ECL	MC10H102P	MOT	8001-01-0201	1
NONE	PIN DRIVER, HIGH SPEED	HL108020	HITEC	8010-80-2200	1
NONE	PRESCALER, DUAL MODULUS, DIVIDE-BY-64/65, ECL	MC12017P	MOT	8012-01-1700	1
NONE	GATE ARRAY, 84 PIN, PSC288	PSC288	PLESS	8700-00-0003	1

WAVETEK PARTS LIST	TITLE	ASSEMBLY NO.	REV
	SPARES KIT 91	1200-00-3480	A
		PAGE 3	

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	CHECKED		TITLE: SPARES KIT 91
	PROJ. ENGR.		
	RELEASE APPROV.		
FINISH WAVETEK PROCESS	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES ± .XX ± .XXX ± °		SIZE D; FSCM NO. 23338; DWG. NO. 1200-00-3480; REV A; SCALE; MODEL 91; SHEET 1 OF 1
DO NOT SCALE DRAWING			

APPENDIX A
GENERAL

A.1 THE MODEL 91

The Model 91, 1mHz to 20 MHz programmable, Synthesized Pulse/Function Generator, produces sine, triangle, square, and pulse functions, plus dc. Functions can be continuous, triggered, gated, burst, AM (amplitude modulation), SCM (suppressed carrier modulation), FM (frequency modulation) or swept. Balanced or unbalanced output is programmable from 1mV to 30 Vpp (into an open circuit) with selectable output impedances.

As a pulse generator, the Model 91 produces single, double, and delayed pulses to 50 MHz. In addition, the Model 91 produces external width outputs as well as square waves at 50% duty cycle to 100 MHz.

At frequencies above 20 Hz (all functions - Continuous, AM, and SCM modes), the Model 91 phase locks its function generator to its internal frequency synthesizer (internal phase lock) improving the frequency accuracy to ±(10 ppm). An optional frequency reference (Option 001) improves the frequency accuracy to better than 1ppm. Also, the Model 91 can phase lock to an external source (same conditions as internal phase lock). When locked to an external source, the phase of the Model 91 output can be varied ±180°. In addition, the internal frequency synthesizer acts as an accurate internal trigger source for the trigger, gate, or burst modes.

A.2 FUNCTION GENERATOR SPECIFICATIONS

A.2.1 Non-Synthesized/Synthesized Frequency

Non- Synthesized Operation

1mHz to 19.99 Hz Continuous;
0.1 Hz to 19.99 Hz, AM and SCM;
1mHz to 20 MHz, Triggered, Gated, Burst, Sweep, or FM.

Synthesized operation

20 Hz to 20 MHz, Continuous, AM, and SCM.

A.2.2 Frequency

A.2.2.1 Frequency Range

1mHz to 20 MHz;
20 Hz to 20 MHz, Synthesized;
1 mHz to 1MHz, 600Ω Output Impedance (Balanced and Unbalanced Outputs).

A.2.2.2 Frequency Modulation and Sweep Ranges

Internally, the Model 91 operates using ten frequency ranges. In the FM and Sweep modes, the frequency limits must be kept within one of these ranges. The following table lists the ten ranges and the maximum frequency deviation (1000:1 or three decades) allowed for that range.

FM/SWEEP RANGE

Normal Range	Minimum Frequency
20 - 2.001 MHz	20k
2 - 0.2001 MHz	2kHz
200 - 20.01 kHz	200 Hz
20 - 2.001 kHz	20 Hz
2 - 0.2001 kHz	2Hz
200 - 20.01 Hz	0.2 Hz
20 - 2.001 Hz	0.02 Hz
2 - 0.2001 Hz	0.002 Hz
200 - 20mHz [1]	2mHz
20 - 2mHz [2]	2mHz

[1] *100:1 or two decades only.*

[2] *10:1 or one decade only.*

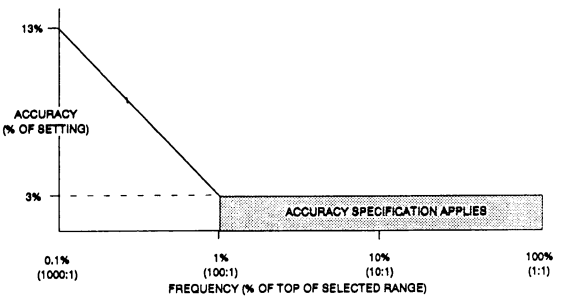
A.2.2.3 Frequency Resolution

5 digits, synthesized;
4 digits, non-synthesized.

A.2.2.4 Frequency Accuracy

±10 ppm synthesized;
±1ppm Option 001.

Nonsynthesized frequency accuracy



A.2.2.5 Stability

VS temperature:

±2 ppm/°C for synthesized 15°C to 25°C;
±1ppm Option 001: 0°C to 50°C;
<100 ppm/°C for non-synthesized.

VS time:

±10 ppm/year for synthesized;
±1ppm/year Option 001;
±0.1% for non-synthesized within 10 minutes;
±0.5% for non-synthesized within 24 hours.

A.2.2.6 Synthesizer/Internal Lock

The Model 91 can be phase locked at frequencies ≥20 Hz (continuous, AM or SCM mode) to an internal crystal referenced frequency synthesizer which improves the generator's frequency accuracy and stability. A front panel annunciator (UNLOCK) indicates phase lock conditions.

A.2.2.7 External Lock

The Model 91 can be phase locked at frequencies ≥20 Hz (continuous, AM or SCM mode) to an external phase lock signal. Model 91 measures the external signal, sets the generator's frequency, and locks the generator to the source. When external phase locked, the external source controls the generator's frequency, stability and purity. Also, external phase lock permits programing the phase angle relative to the positive-going zero crossing of the external sine wave. Phase angle may be set from ±180° (± π radians) with 1° resolution and, in the range of 50 Hz to 10 MHz, ±(4°+20 ns) accuracy. If the external signal has dc offset, the Model 91 ignores the offset and phase locks reference to the "0°" point on the external sine wave. Pulse functions can not be externally phase locked.

A.2.3 Functions

A.2.3.1 Time Symmetry

When time symmetry is fixed at 50%, symmetry accuracy is <±(0.2%+5 ns).

Time symmetry is variable from 5% to 95% in 1% steps to 2 MHz. Variable symmetry linearly decreases to a fixed 50% at 20 MHz. Accuracy is <±(1% + 5 ns).

A.2.3.2 Sine

Sine Distortion at 10 Vpp into 50Ω:

All outputs

<1% (-40 dB) THD 1mHz to 20 Hz;
<0.5% (-46 dB) THD 20 Hz to 100 kHz.

Unbalanced Output 50Ω and 75Ω, no harmonics above:

-40 dBc, 100 kHz to 2MHz,
-30 dBc, 2MHz to 6MHz,
-25 dBc, 6MHz to 20 MHz.

A.2.3.3 Triangle

Triangle Linearity:

10% to 90% nonlinearity:

±1%, 1mHz to 100 kHz;
±2%, 100 kHz to 2MHz;
±10%, 2MHz to 5MHz.

A.2.3.4 Square

Square Transition Time:

The transition time (rise/fall) is <9ns, 10% to 90%, Unbalanced Output into 50 Ω impedance.

Aberrations:

Overshoot and ringing are <(5%+20 mV) of the peak to peak amplitude.

1.3.3.5 dc Function

The dc function provides a variable dc voltage (±15V) at the Unbalanced Output.

Range

±1mV to ±7.5V terminated;
±2mV to ±15V open circuit.

Resolution

4 digits; may be reduced if both offset and waveform amplitude are programmed.

Accuracy

±(2%+1mV) to 9.99 mV terminated;
±(2%+2mV) to 999 mV terminated;
±(2%+10 mV) to 7.5V terminated.

A.2.4 Modes

A.2.4.1 Continuous

In this mode, the Model 91 supplies a continuous waveform at the selected frequency. The unit automatically selects its internal synthesizer at frequencies at or above 20 Hz. Display shows internal or external locking source selection and current frequency (programmed frequency if internal is selected, or external frequency if external lock is selected).

A.2.4.2 Triggered

In this mode, the Model 91 remains quiescent at trigger baseline of selected function until a trigger event occurs (positive-going transition at the rear panel Trig In connector, Manual Trigger, GPIB trigger command, or internal trigger rate generator). This initiates a single waveform or pulse period at the programmed frequency and, after completing the waveform, returns the generator to the quiescent baseline value ready for another triggering cycle. When square waves ≤20 MHz are selected, there will be a 1/4 cycle delay between the trigger input and the square wave output. Internal or external phase lock is disabled in the triggered mode.

The external trigger frequency will be displayed each time the TRIG FREQ key is pressed. The generator can also be triggered using the internal trigger synthesizer. Accuracy of triggered waveform period is <±3%.

A.2.4.3 Gated

In this mode, the Model 91 functions the same as the Triggered mode, except the generator runs continuously as long as the triggering signal is true. The generator starts and stops in the quiescent state, and the Model 91 always completes its last cycle. The maximum generator frequency is limited to 20 MHz. The minimum gating frequency is half the generator's frequency. Internally gated waveforms have an approximate 1:1 on/off cycle. The display shows the internal or external trigger source selection and, if internal gated, the programmed internal triggering frequency.

A.2.4.4 Burst

In this mode, the Model 91 functions the same as the Triggered mode, except that the number of cycles generated, when triggered, is programmable from 1 to 1,000,000. The generator starts and stops in the quiescent state. The display shows internal or external trigger source selection and the programmed burst count. The maximum generator frequency in the Burst mode is limited to 20 MHz. In external trigger, the Model 91 displays the trigger frequency each time the TRIG FREQ key is pressed.

A.2.4.5 Amplitude Modulation

In this mode, the Model 91 functions the same as the continuous mode except an external signal at the MOD IN connector modulates the instantaneous amplitude of the selected carrier. The output can be modulated from 0 to 100%. Average amplitude is as programmed except signal level with no modulation is less than 7.5 Vpp. The display shows the internal or locking source as well as the programmed frequency. Minimum generator frequency for the AM mode is 0.1 Hz.

A.2.4.6 Suppressed Carrier (SCM)

In this mode, the Model 91 functions the same as the AM mode, except the selected function (carrier) is zero amplitude until an external signal is applied. Minimum generator frequency for the SCM mode is 0.1 Hz. Three selectable scale factors (Vout/Vin) determine the output/input signal ratio. SCM can only be selected when the Continuous signal level is less than 7.5 Vpp.

A.2.4.7 Frequency Modulation

In the FM mode, an instantaneous signal at the MOD IN connector controls the frequency of the generator. Connecting a dc level to the MOD IN connector shifts the generator to a frequency based on the magnitude of the level. Connecting an ac signal to the MOD IN deviates the frequency of the generator about its programmed frequency. The Model 91 only can be frequency modulated a maximum of three decades (1000:1) on any of the ten ranges (see paragraph 1.3.2.2). Internal or external phase lock is not selectable in this mode. The display shows the scale factor (Hz/V) for the selected frequency range.

A.2.4.8 Sweep

In this mode, the Model 91 frequency can be swept between programmable start and stop frequencies. The Model 91 sweeps up to three decades (1000:1) on any of the ten ranges (see paragraph A.2.2.2). The Model 91 provides three sweep modes: continuous sweep, triggered sweep, or manual sweep. In addition, there are two sweep types: linear and logarithmic. Sweep time can be programmed from 100 ms to 100s. Start/Stop frequency accuracies are shown in paragraph A.2.2.4 - Non-Synthesized frequency accuracy figure. Sweep start and stop frequencies can be selected to allow sweep up and down of frequencies. All 50% symmetrical waveforms can be swept. In addition, pulses (≤20 MHz) can be swept.

A.2.5 Amplitude

A.2.5.1 Range

1mVpp to 15 Vpp terminated into selected output impedance; 2mVpp to 30 Vpp into an open circuit. The peak amplitude + offset must not exceed 7.5 Vp.

A.2.5.2 Resolution

4 Digits (1mV min):

2mVpp to 20 Vpp Open Circuit,
1mVpp to 10 Vpp Terminated;

4-1/2 Digits:

20 Vpp to 30 Vpp Open Circuit,
10 Vpp to 15 Vpp Terminated.

10 mV when using the Upper and Lover Level keys.

Resolution may be reduced when the waveform is offset.

A.2.5.3 Accuracy

All functions at 1kHz, % of setting:

±(2%+1mV) to 100 mVpp terminated;
±(2% + 2mV) to 1Vpp terminated;
±(2% + 10 mV) to 15 Vpp terminated.

A.2.5.4 Flatness

Relative to 1kHz:

Unbalanced 50Ω
<2MHz

±0.3 dB, sine and square;
±0.5 dB, triangle.

2MHz to 20 MHz
±0.75 dB, sine and square;
±1.5 dB, triangle.

Balanced at 135Ω (≤3 feet of RG-58)

<100 kHz
±0.3 dB, sine.

100 kHz to 1MHz
±0.75 dB, sine.

A.2.6 Offset

Offset permits the selected waveform at the Unbalanced output to be dc offset relative to the 0V baseline or dc output of the dc function.

A.2.6.1 Range

±7.5V terminated;

±15V open circuit.

The peak amplitude plus offset must not exceed 7.5 Vp.

A.2.6.2 Resolution

4 digits; may be reduced if both offset and waveform amplitude are programmed.

A.2.6.3 Accuracy

±(2% +1mV) to 9.99 mV terminated;

±(2%+2mV) to 999 mV terminated;

±(2%+10 mV) to 7.5V terminated.

A.2.7 Outputs

A.2.7.1 Sync Out

Sync Out is a female BNC connector which supplies a TTL compatible pulse output at programmed frequency and symmetry in phase with the square function. Output level is 0 to >2V into 50Ω termination. The 10% to 90% transition times are less than 6ns (≤3 feet RG-58). To minimize sync delay, always select Front Sync while using the function generator. This output must be terminated with 50Ω.

A.2.7.2 Sweep Out

Sweep Out is a female BNC connector, which supplies a 0 to +6V (approximate) ramp to indicate sweep position. Source impedance is 600Ω (±10%). Inactive when not in Sweep Mode.

A.2.7.3 Unbalanced Out

The unbalanced output, a female BNC connector, provides the single-ended source of programmed function at selected frequency, amplitude, symmetry, and offset. Source impedance is 600Ω ± 1% to 1MHz; 50Ω or 75Ω ± 1% to 20 MHz. Unbalanced output is unavailable when the balanced output is selected. The Model 91 limits the Unbalanced Output frequency to 20 MHz. This output is protected from over voltages.

A.2.7.4 Balanced

Balanced outputs, dual "banana jack" connectors, provide differential zero offset outputs of the selected function at programmed frequency, amplitude and symmetry. A universal binding post is provided for signal common "center tap" connection. Source impedance is programmable as 135Ω ± 1% or 600Ω ± 1% to 1MHz. Output unbalance is <1% to 100 kHz. Balanced output is unavailable when the unbalanced output is selected. This output is protected from short circuits and over voltages.

A.2.8 Inputs

A.2.8.1 External Frequency Input

In phase lock, EXT FREQ IN accepts the signal that phase locks the Model 91 to the external source. The Model 91 measures the frequency, sets the unit to match the source frequency, and phase locks the generator to the source. This external frequency may be read by pressing the TRIG FREQ key. Model 91 phase lock range is 20 Hz to 20 MHz in the Continuous, AM or SCM modes. The input signal may be a bipolar sine wave (600 mVpp to 30 Vpp into 10 kΩ) or TTL signal which is selected by an internal jumper (paragraph 2.4.6). Input impedance is 10 kΩ±2%. This input is protected by it high impedance input.

A.2.8.2 Modulation Input

MOD IN, a female BNC connector, serves as the modulation input for FM (VCG), AM, and SCM. Input impedance is 10 kΩ ±20%. Bandwidth is dc to 1MHz. Maximum input level is ±20 Vpp (into 10 kΩ).

FM

In FM, an external signal provides linear control of waveform frequency around the programmed frequency. A ±10V input signal causes a 1000:1 frequency change (selected frequency range is the top decade in a possible three decade frequency span). An ac signal varies the frequency around the programmed frequency. A dc level sets the generator to a single frequency. VCG bandwidth is dc to 100 kHz limited by 0.06 V/μs maximum slew rate. FM bandwidth is dc to 100 kHz deviation rate; with maximum envelope distortion of 1.78% (-35 dB) taken with 10 MHz carrier frequency, 1kHz modulation frequency and 1MHz (10%) depth (sine wave modulation).

AM

In the AM mode, an external signal provides linear control of waveform amplitude around the programmed

amplitude value. Displayed amplitude dependent scale factor specifies approximate Vpp (into 10 kΩ) required for 100% modulation. AM bandwidth is dc to 1MHz; with a maximum envelope distortion of 2% taken with 1MHz carrier frequency, 1kHz modulation frequency and 70% AM (sine wave modulation).

SCM

In the SCM mode, an external signal linearly controls the waveform's amplitude about the zero carrier level. The Model 91 displays a scale factor (2.4V/V, 0.24 V/V, or 0.024 V/V) which defines the amount of Mod In signal level to produce a SCM output level. SCM bandwidth is dc to 1MHz. Maximum envelope distortion is 2% (1MHz carrier and 1kHz modulation).

A.2.8.3 Trigger Input

Trig In, a rear panel BNC connector, serves as the external trigger input for both the function and pulse generator. The generator triggers from greater than 500 mVpp bipolar or TTL signal. Input impedance is 1kΩ shunted by <10 pF. The input is protected up to ±15 Vdc. The Model 91 triggers on either the positive or negative slope (selectable) of the input signal. Also, it permits the triggering level to be within ±5 Vdc (100 mV resolution). Trigger level accuracy is ±(5%+250 mV).

A.3 PULSE GENERATOR

A.3.1 Period/Frequency

1mHz to 50 MHz for pulses, 1mHz to 100 MHz (1000s to 10 ns) for square pulses at the rear panel Pulse Outputs. 20 Hz to 100 MHz synthesized. Above 20 MHz continuous and triggered modes only.

A.3.1.1 Resolution

5 digits, 1mHz to 50.000 MHz;

4-1/2 digits, 50.002 to 100 MHz (2kHz minimum resolution).

A.3.1.2 Accuracy

Same as Function Generator: Accuracy; see paragraph A.2.2.3.

A.3.1.3 Stability

Same as Function Generator: Stability; see paragraph A.2.2.4.

A.3.1.4 Synthesizer/Internal Phase Lock

Same as Function Generator: Synthesizer/Internal Phase Lock; see paragraph 1.3.2.5.

A.3.1.5 External Phase Lock

Same as Function Generator: External Phase Lock; see paragraph A.2.2.6.

A.3.2 Functions

A.3.2.1 Single Pulse

In this mode, the Model 91 produces one pulse each pulse period with variable pulse width. The single pulse is coincident with the pulse sync output. Pulse repetition rate up to 50 MHz at rear panel pulse outputs and 20 MHz at front panel outputs.

A.3.2.2 Delayed Pulse

In this mode, the Model 91 produces one pulse each pulse period delayed (variable) relative to the pulse sync output. Like the single pulse, the delayed pulse has variable pulse width. Pulse repetition rate up to 50 MHz at rear panel pulse outputs and 20 MHz at front panel outputs.

A.3.2.3 Double Pulse

In this mode, the Model 91 produces one pair of pulses each pulse period. Both pulses have the same variable pulse width. The position of the second pulse is set by using delay. The first pulse is coincident with the pulse sync output. Pulse repetition rate up to 25 MHz at rear panel pulse outputs and 20 MHz at front panel outputs.

A.3.2.4 External Width

Output pulse period and width determined by the external trigger signal. The setup of trigger level and slope determines the shape of the external width pulse. When using the front panel outputs, the external width frequency range is dc to 20 MHz. When using the rear panel output, the external width frequency range is dc to 50 MHz.

A.3.3 Pulse Width

Range: 10 ns to 2000s.

Resolution: 4 digits, limited to 100 ps.

Accuracy: ±(1.0%+5ns).

Jitter: ±(0.050%+100 ps).

Duty Cycle: Maximum duty cycle is 70% of periods down to 50 ns, decreasing to 25% at 20 ns period.

A.3.4 Pulse Delay

Range: 0 ns to 2000 s.

Resolution: 4 digits, limited to 100 ps.

Accuracy: ±(1.0%+5ns).

Jitter: ±(0.05%+100 ps).

Duty Cycle: Maximum duty cycle is 70% of periods down to 50 ns, decreasing to 25% at 20 ns period.

A.3.5 Pulse Timing Definitions

t0 = Trigger Input

t1 = Sync Output

t2 = Pulse Output

(t1-t0) = <45 ns for the rear sync output; <90 ns for front sync output.

(t2-t1) = Programmable Delay

A.3.6 Modes

Continuous, Triggered, Gated, Burst, Amplitude Modulation, Suppressed Carrier (SCM), Frequency Modulation, and Sweep are the same as Function Generator Modes. However, the continuous mode operates up to 100 MHz, and triggered operates to 50 MHz.

A.3.7 Amplitude

Amplitude specifications are the same as Function Generator: Amplitude. When using front panel outputs, varying the amplitude affects the pulse's programmed upper and lower levels.

A.3.8 Offset

Offset specifications are the same as Function Generator: Offset. Varying the offset affects the pulse's programmed upper and lower level.

A.3.9 Upper and Lower Levels

A.3.9.1 Unbalanced/Balanced Outputs

When using pulse functions, the output levels can be set using upper and lower level. Upper level range is -6.499 to +7.5V and must be more positive than the lower level. Lower level range is -7.5 to +6.499V and must be more negative than the upper level. Varying the upper and lower levels affects the programmed amplitude and offset.

A.3.9.2 Pulse Outputs

See Pulse /Pulse Complement Outputs. The Model 91 permits the setting of custom upper and lower levels:

Upper Level	-1.4 to +4.2V
Lower Level	-1.8 to +3.8V

The upper level must be more positive (>0.4V) than the lower level. Custom level resolution is 100 mV.

A.3.10 Outputs

A.3.10.1 Sync Out

The Sync Out signal for the pulse generator occurs at the 50% point on the lead edge of the internal sync signal (t1). In external width, the Sync Out signal is a TTL representation of the external width trigger signal. Sync Out amplitude is 0 to >2V in to 50Ω termination. Transition time is <6 ns (≤3 feet of RG 58). This connector must be terminated with 50Ω. Use the SYNC key to select either SYNC FRONT or SYNC REAR depending on the output used.

A.3.10.2 Sweep Out

Same as Function Generator: Sweep Out; see paragraph A.2.7.2.

A.3.10.3 Unbalanced Out

Same as Function Generator: Unbalanced Out; see paragraph A.2.7.3.

A.3.10.4 Balanced

Same as Function Generator: Balanced Out; see paragraph A.2.7.4.

A.3.10.5 Pulse/Pulse Complement Out

These rear panel pulse output BNC connectors provide the selected pulse outputs at four fixed levels and one custom level. Pulses Outputs can be either TTL, CMOS, +ECL, -ECL, or Custom. Pulse and Pulse Out source impedance is 50Ω. The Pulse Complement Output supplies the inverse of the Pulse Output pulse. Between 50 and 100 MHz, the Model 91 limits the pulse outputs to 2.5 Vpp. Following is a list of programmable levels (specified into 50Ω termination).

Logic Selection	Upper Level	Lower Level
TTL	+2.5V	0V
CMOS	+4V	0V
+ECL[1]	+4.1V	+3.2V
-ECL[2]	-0.9V	-1.8V
Custom[3]	-1.4 to +4.2V	-1.8 to +3.8V

[1] Vcc = +5V, Vee = 0V.

[2] Vcc = 0V, Vee = -5.2V.

[3] Lower Level <0.4V<Upper Level.

Accuracy : ±(2%+50 mV) of setting

Termination: 50Ω termination

Source Impedance: 25Ω

Protection: These outputs are momentarily protected to ±15 Vdc.

Perturbations

TTL	0.25V
CMOS	0.19V
+ECL	0.36V
-ECL	0.36V

Rise/Fall Time

TTL	3.75 ns
CMOS	5ns
+ECL	3.5 ns
-ECL	3.5 ns
Custom	2.5 ns+1.75 ns/V (>1V output)

Skew: <1.5 ns.

A.3.11 Inputs

A.3.11.1 External Frequency Input

External Frequency Input function the same as described in Function Generator: External Frequency Input.

A.3.11.2 Modulation Input

Modulation Input functions the same as described in Function Generator: Modulation Input.

A.3.11.3 Trigger Input

Trigger Input functions the same as described in Function Generator: Trigger Input. In the External Width function, the trigger signal duration and rate set the pulse width and repetition rate.

A.4 USER INTERFACE

A.4.1 Display

The Model 91 contains a 16 digit, Vacuum Florescent Display (VFD). Display intensity is adjustable between 1 and 31 (relative units) with 25 being the default intensity. All selectable parameters display the parameter name, the numeric value and the unit. In addition, the display shows GPIB messages, various utilities, maintenance and diagnostic information.

A.4.2 GPIB Programming

A.4.2.1 Address

Valid GPIB addresses for the Model 91 are 0-30 (default address is 9), front panel selectable and battery backed-up.

A.4.2.2 Subsets

SH1, AH1, SR1, RL1, PP0, DC1, DT0, C0, T6, L4, TE0, LE0, and E1.

A.5 STORED SETTINGS

The Model 91 permits up to five complete setups to be stored in its internal memory. These settings can be recalled and used at any time.

A.6 OPTIONS

A.6.1 001: Frequency Reference

This option improves the reference frequency from an adjustable crystal to an adjustable TCXO with a ± 1 ppm performance over the operating temperature range. A rear panel EXT REF IN connector accepts TTL or Bipolar sine wave (>500 mVpp at 10 MHz) reference input. The REF OUT connector provides TTL compatible 10 MHz pulses capable of driving a 50Ω termination.

A.6.2 003: Handles and Rack Adapter

This option consists of a pair of handles and rack adapters that attach to the left and right sides of the Model 91. The rack adapters allow the instrument to be mounted in a standard 19 inch rack. Also included are a pair of handles which may be installed in place of the existing front panel corner pieces.

A.6.3 004: Service Kit

This option supplies a set of extender cards which provide access to the plug-in boards during maintenance. This option also includes a temperature - stablizing calibration cover.

A.7 GENERAL

A.7.1 Physical Specifications

A.7.1.1 Dimensions

35.6 cm (14 in.) wide, 13.3 cm (5.219 in.) high and 43.2 cm (17 in.) deep.

A.7.1.2 Weight

Approximately 10.0 kg (22 lb.) net; 14.1 kg (31 lb.) shipping.

A.7.1.3 Power

90 to 108, 108 to 126, 198 to 231, or 216 to 252 Vrms; 48 to 440 Hz; 1 phase; <130 VA.

A.7.2 Environmental Specifications

The Model 91 conforms to MIL-T-28800C, class 5.

A.7.2.1 Temperature Range

0°C to +50°C for operation;

-40°C to +70°C for storage.

A.7.2.2 Warm Up Time

Allow 20 minutes for specified operation at ambient temperature of last Auto Cal ± 10°C. Auto Cal should be performed when the ambient temperature has changed >± 10°C.

A.7.2.3 Operational Humidity

11°C to 30°C at 95% relative humidity;

31°C to 40°C at 75% relative humidity;

41°C to 50°C at 45% relative humidity.

A.7.2.4 Altitude

To 10,000 ft. (3050m.) for operation;

To 15,000 ft. (4570m.) for non-operating.

A.7.2.5 Vibration (Operating)

Vibration level of 0.013 in. from 5 to 55 Hz (2g acceleration at 55 Hz.).

A.7.2.6 Shock (Non-operating)

40g, 9ms half-sine wave.

A.7.2.7 Bench Handling (Operating)

4 in. or point of balance drop, any face, solid wooden surface.

A.7.2.8 Electromagnetic Compatibility

The Model 91 has been tested to MIL-STD-461A Notice 4 (EL) and meets the emission and susceptibility requirements of CE02, CE04, CS02, CS06, RE02, RE02.1, and RS03. However, the Model 91 does not conform to REO 1 (line and related harmonics up to 7th harmonics).