WAVETEK

PRELIMINARY OPERATION AND MAINTENANCE MANUAL

Model 1391

INCLUDING SCPI AND MATE/CIIL LANGUAGE DESCRIPTIONS

50 MHz VXI Pulse Generator

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50 MHz VXI Pulse Generator

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Manual Revision N/R, 9/92 (Harris)
Manual Part Number 1006-00-0694

WARRANTY

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WAVETEK

September 17, 1992

Dear User,

Thank you for choosing Wavetek for your requirements for a MATE/CIIL compatible pulse generator. You will find the 1391 MATE follows in the outstanding tradition of high performance pulse generators from Wavetek.

Enclosed with the 1391 MATE is the Preliminary Operators Manual. The preliminary manual contains all of the information that you will need to setup and program the instrument both in CIIL, and the local language of SCPI. However, this preliminary manual does not contain several sections which will be included in the final version. These sections include, Calibration(although a section on performance verification is included), Maintenance, Troubleshooting, and Self-test.

The final version of the manual with these sections should be complete within 6-8 weeks. At that time we will make sure that all users will be updated.

We trust that this will not be an inconvenience, and apologize for the delay.

Best Regards,

John L. Johnston
VXI Product Marketing Manager

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Instruments Division

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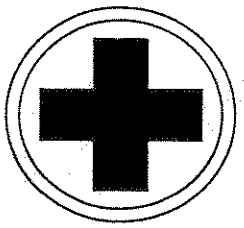
SAFETY FIRST



PROTECT YOURSELF. Follow these precautions:

- Don't touch the outputs of the instrument or any exposed test wiring carrying the output signals. This instrument can generate hazardous voltages and currents.
- Don't bypass the VXI chassis' power cord's ground lead with two-wire extension cords or plug adaptors.
- Don't disconnect the green and yellow safety-earth-ground wire that connects the ground lug of the VXI chassis power receptacle to the chassis ground terminal (marked with ⏚ or ⚠).
- Don't hold your eyes extremely close to an rf output for a long time. The normally nonhazardous low-power rf energy generated by the instrument could possibly cause eye injury.
- Don't energize the VXI chassis until directed to by the installation instructions.
- Don't repair the instrument unless you are a qualified electronics technician and know how to work with hazardous voltages.
- Pay attention to the **WARNING** statements. They point out situations that can cause injury or death.
- Pay attention to the CAUTION statements. They point out situations that can cause equipment damage.

CONTENTS

CONTENTS (Continued)

CONTENTS (Continued)

CONTENTS (Continued)

APPENDIX

TABLES

ILLUSTRATIONS

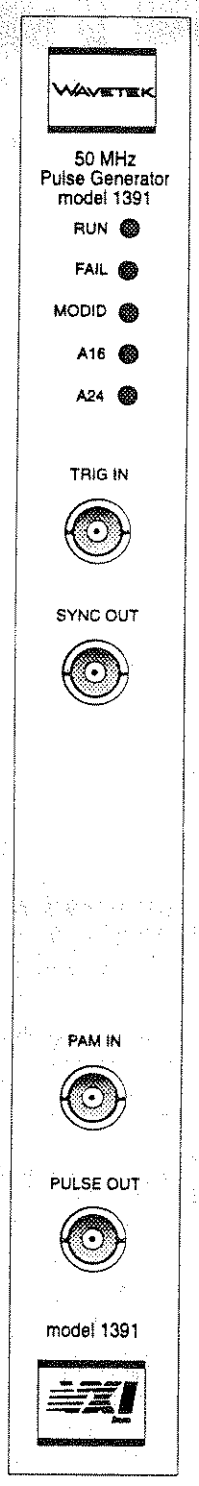


Figure 1-1. Model 1391 50 MHz VXI Pulse Generator

1.1 The Model 1391

The Model 1391 is a 1 mHz to 50 MHz "C" size VXI Programmable Pulse Generator. It can generate single, double, and delayed pulses with programmable period, width, delay, rise/fall transitions, and output levels. The generator operates as a continuous, triggered, gated or burst pulse source up to 50 MHz. Additionally, the Model 1391 can be programmed for a square wave function (~50% time symmetry) up to 100 MHz. Pulse characteristics are programmable with 4 digit resolution, with width and delay up to 2000 seconds, and rise/fall transition times settable from 5 ns to 50 µs.

The pulse ouput amplitude may be specified as upper and lower levels, which can be programmed in a ±16 V window (±8V into 50Ω termination). Peak to peak amplitude, upper level value minus lower level value, is continuously variable in 10 mV steps from 150 mVp-p to 16 Vp-p (50Ω). The pulse amplitude (upper, lower, or both) may be modulated (PAM) with an external signal.

Control of the pulse generator adheres to the SCPI (Standard Commands for Programmable Instruments) format Version 1.0, April 1990 (refer to the SCPI manual for further information). SCPI is an industry standard language for remote instrument programming. Using any manufacturer's VXI chassis, the Model 1391 can be controlled using the SCPI language and the appropriate controller.

Multiple pulse generators may be linked and operated together inside one VXIbus chassis. Series operation is provided by full support of the VXIbus SUMBUS. A signal programmed at the output may be sent to the SUMBUS, or signal present at the SUMBUS may be summed into the model 1391 output. In parallel operation, model 1391's may be slaved to a master clock/trigger bus on the VXIbus backplane to create a multichannel pulse generator.

The model 1391 has extensive self-adjustment utilities built in. Calibration constants are maintained in non-volatile memory.

1.2 Specifications

1.2.1 Functions

Programmable single, double or delayed pulse and fixed (~50%) duty cycle square wave.

1.2.2 Operating Modes

Continuous:
Pulse period generated continuously internal to the model 1391 at programmed frequency/period. Selected pulse waveform is continuously output at PULSE OUT with programmed pulse characteristics. Period timing signal appears at SYNC OUT (if enabled) and may be selected for output to the backplane. Pulse periods programmable up to 25 MHz in double pulse, 50 MHz in single or delayed pulse, and 100 MHz in square wave. Pulse Amplitude Modulation may be enabled for external signal at PAM IN.

Triggered:
As above for Continuous mode, except that pulse period generation is disabled. Output quiescent until triggered by an external signal at TRIG IN, a TTLTRG or ECLTRG signal, internal trigger frequency, or a VXIbus command, then generates one pulse period with the programmed pulse waveform and pulse characteristics. Triggered pulse periods operate to 25 MHz in double pulse, 50 MHz in single or delayed pulse and square wave.

Gated:
Similar to triggered mode except output continues for the duration of gate signal. The last pulse period started is completed.

Burst:
Similar to triggered mode except programmable number of pulse periods in a burst. Burst length, initiated by the trigger signal, is programmable between 2 and 1,000,000 cycles.

1.2.3 Inputs

Trig In:
Front panel BNC input for external triggering signal. Variable trigger level control accepts TTL or variable amplitude bipolar signals. In addition, any of the trigger lines on the VXIbus backplane can be selected as the trigger input, see Trigger Input (from VXI Backplane). TRIG IN is protected for short circuit and ±20 V input range.

Variable Trigger Level:

Range:	± 10 V
Resolution:	50 mV
Accuracy:	± 500 mV
Minimum input level:	750 mVpp
Maximum input level:	± 20 V
Minimum pulse width:	10 ns
Input impedance:	≥1kΩ shunted by ≤10 pF

PAM In:
Front panel BNC connector, used to externally Pulse Amplitude Modulate the model 1391. PAM modulation scale factor is set so that a 1 volt input at this connector will result in a 2 volt change in upper/lower level amplitude at the PULSE OUT connector. Input is protected to ±50 V inputs.

Input impedance:	≥1 kΩ
Bandwidth:	dc to >20 kHz
Accuracy	± 5%

SUMBUS Input (from VXI Backplane):
Analog signals on the VXIbus SUMBUS line may be summed into a model 1391 PULSE OUT with a fixed scale factor. A full-scale PULSE OUT signal of 16 Vpp requires an 80 mApp input signal driving the SUMBUS line. SUMBUS receiver specifications are:

Scale factor:	0.2V/mA
Accuracy:	± 5%
Input impedance:	>10 kΩ in parallel with <20 pF

Trigger Input (from VXI Backplane):
Any one of the eight VXIbus TTLTRG lines or either of the two ECLTRG lines may be selected as the trigger input for the model 1391. When a TTLTRG line is selected, the triggering signal on that line is limited to a maximum of 12.5 MHz by the VXIbus specification.

1.2.4 Outputs

Pulse Output:
Front panel BNC output, supplies the 150 mVpp to 16 Vpp pulse waveform into a 50Ω termination. Programmable on or off (Zoff > 500 kΩ). Output is protected against short circuits.

Source Impedance:	50Ω.

Sync Output:
TTL level pulse into 50Ω. Programmable as either the pulse period (MARKer:TYPE CLOCk) or as a copy of the external gating signal (MARKer:TYPE GATE). When in continuous mode, the Sync Output is a square wave defining the timing of a pulse period. In gated or burst modes, the Sync signal may be programmed to be true from the triggering event to the end of the gate or burst. The SYNC OUT is short circuit protected.

TTL Compatible:	<0.4 to >2.0 V into 50Ω
Timing:	50% point of rising edge defines the start of a pulse period. Configuration dependent delay (see Trigger Latency, Figure 1-2 and the table below) following trigger event.
Transition time:	<5ns with 3 feet RG-58 50Ω coax cable terminated into 50Ω.

Trigger Delays ($t_1 - t_0$)

Configuration	Trigger Latency
External Trigger	typically 55 ns **
ECL Trigger*	typically 52 ns **
TTL Trigger*	typically 52 ns **

* Trigger delays measured for a single pulse, 0 ns delay.

** Add 22 ns when unit is configured as the Master

SUMBUS Output (to VXI Backplane):
Pulse output signals from the model 1391 may be summed onto the VXIbus SUMBUS line with levels proportional to the pulse output. A full-scale PULSE OUT signal of 16 Vpp results in an 80 mApp signal driving the SUMBUS line. SUMBUS driver specifications are:

Scale factor:	5 mA/V
Accuracy:	± (5% + 500 µA)
Output impedance:	>10 kΩ in parallel with <20 pF
Compliance:	1.2 V minimum

Trigger Output (to VXI Backplane):
Any one of the eight VXIbus TTLTRG lines or either of the two ECLTRG lines may be selected to be driven by a signal from the model 1391. The internal trigger, the external trigger input, or the pulse waveform may be selected to be output. When a TTLTRG line is selected, the triggering signal on that line is limited to a maximum of 12.5 MHz by the VXIbus specification.

1.2.5 Pulse Characteristics

See Figure 1-2 for an illustration defining the various pulse characteristics. Pulse functions are programmable using operating mode, pulse period (frequency), width, delay, transition times, and amplitude levels.

NOTE: All pulse characteristics specifications require high-quality 50Ω cable (≤3 feet RG-59 or equivalent) and a high-frequency 50Ω (≥ 1W) termination at the far end of the cable from the PULSE OUT BNC.

Pulse Period:

Range:	10 ns to 1000 s (1 mHz to 100 MHz)
Resolution:	4 digits, limited by 1 mHz
Accuracy:	Same as the VXIbus CLK10 reference in continuous mode (± 0.01% typical), ± 2% of setting in non-continuous modes.

Pulse Width:

Range:	10 ns to 2000 s
Resolution:	4 digits, limited by 100 ps
Accuracy:	± (1% + 2 ns)
Jitter:	± (0.05% + 100 ps)
Duty Cycle:	95% limited by minimum off-time of 10 ns.

Pulse Delay:

Range:	0 ns to 2000 s
Resolution:	4 digits, limited by 100 ps
Accuracy:	± (1% + 5 ns)
Jitter:	± (0.05% + 100 ps)
Duty Cycle:	95% limited by minimum off-time of 12 ns.

Rise and Fall Transitions:

Range:	5 ns to 50 µs (<8 ns above 12 Vpp)
Resolution:	4 digits, limited by 100 ps
Accuracy:	± (5% + 2 ns)
Aberrations (Vpp):	< (5% of Vpp + 20 mV)

NOTE: The ratio of rise time to fall time may not exceed 10:1. For Amplitudes > 12 Vpp the Aberrations specification applies for transitions ≥ 7 ns.

Upper and Lower Levels:

Range:	± 8 V
Resolution:	10 mV
Accuracy:	± 100 mV

NOTE: The minimum amplitude (upper – lower) may not be less than 150 mVpp. Pulses less than 500 mVpp are restricted to a ± 2V window.

1.2.6 Multichannel Operation

Multiple 1391 modules may be operated together in series or in parallel to create a multichannel pulse generator.

Series (SUMBUS) Operation
A module may be selected to drive the SUMBUS, receive from the SUMBUS, or disconnect from the SUMBUS. Allows the signal from one module to be summed with the signal at the output of another. Allows for more complex waveform generation than provided with simple pulse generator features, such as multi-level pulses.

Parallel (Master/Slave) Operation
Up to 10 model 1391 modules may be operated in Master/Slave configuration within a VXIbus chassis. This mode of operation uses the high bandwidth and tight timing of the ECL trigger lines to couple the start of triggered pulse periods of Slave modules to the trigger output of the Master module. Sets the "start of pulse period" (t_1) timing points of adjacent modules into close agreement. Modules further away will have a timing delay of approximately 0.5 ns per slot, dependent upon the VXIbus chassis backplane.

1.3 GENERAL

1.3.1 SCPI Programming

Conforms to SCPI Version 1992.0 and IEEE-488.2 standard mandated commands. Root level commands include:

DIAGnostic	**OUTP**ut	**SOUR**ce
STATus	**SYST**em	**TRIG**ger
INITiate	**CAL**ibration	**RES**et

1.3.2 VXIbus Interface

Message Based Device (MBD), 256 byte input buffer. Supports the following subsets/protocols:

A16/A24 D16/D24 Master, A16/A24 D16/D24 Slave;
VXIbus Instrument Protocol (I);
VXIbus IEEE-488.2 Instrument Protocol (I4);
Event Generator, Response Generator;
DC (Dynamically Configurable) Device.

The model 1391 supports all Word Serial Commands specified in the VXIbus System Specification (Rev. 1.4), Tables E.1 and E.2 for the above subset/protocol classification.

1.3.3 Environmental

Temperature Range:

Operating:	Specifications apply 0°C to 50°C, when calibrated at 23°C ± 3°C.
Storage:	-40°C to +71°C (RH not controlled).
Warm-up Time:	30 minutes for specified operation, except stability specifications require 60 minutes.

Altitude:

Operating:	Sea level to 10,000 ft.
Storage:	Sea level to 15,000 ft.

Relative Humidity (non-condensing):

0°C to +10°C:	not controlled.
+11°C to +30°C:	95 ± 5% RH max.
+31°C to +40°C:	75 ± 5% RH max.
+41°C to +50°C:	45 ± 5% RH max.
Vibration:	0.013 in., 5 to 55 Hz, 2g max.
Shock:	Non-operating, 40 g, 9 ms half-sine.
Bench Handling:	Non-operating, 4 inch or point of balance drop, any face, solid wooden surface.

1.3.4 Size

Dimensions:	Single slot, "C" size VXI module.
Weight:	1.65 kg (3.63 lb) net; x.xx kg (x.xx lb) shipping.

1.3.5 Power

Total: < 47 Watts

Voltage	Peak Current	Dynamic Current
+24 Vdc	0.4 A	0.3 A
+12 Vdc	1.0 A	0.1 A
+5 Vdc	1.0 A	0.2 A
–2 Vdc	1.1 A	0.1 A
–5.2 Vdc	1.8 A	0.1 A
–12 Vdc	0.8 A	0.1 A
–24 Vdc	0.4 A	0.3 A

1.3.6 Reliability

>22,000 hours MTBF at 25°C, ground benign. MIL-HDBK-217 calculation at 50% component stress.

1.3.7 Cooling Requirement

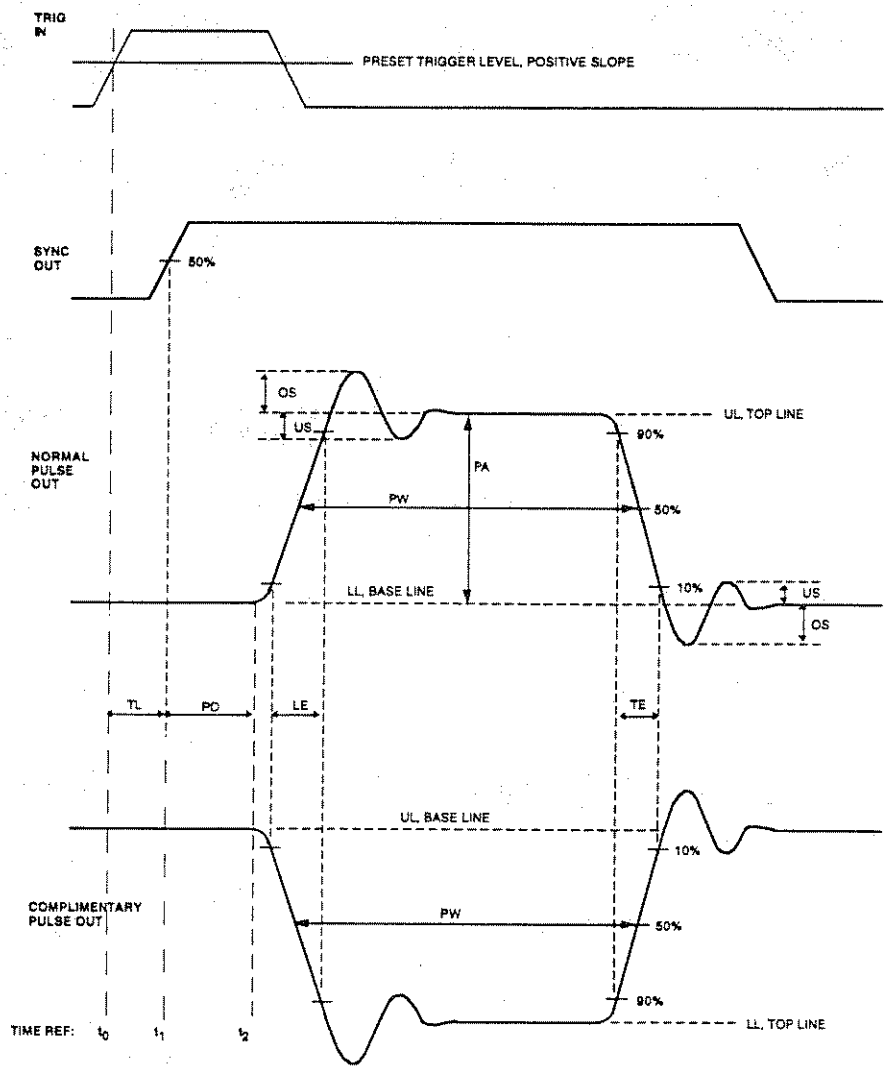
Within a VXI mainframe with cooling air. Minimum airflow requirement for 10°C rise is 0.381mm (.015 in) H_2O at 11.34 l/sec (24 CFM).

1.3.8 Safety

Designed and tested to MIL-T-28800D, UL-1244, and the VXI System Specification, Revision 1.4.

1.3.9 EMC

Designed and tested to MIL-STD-461C, Part 7, RE-02, and VXI System Specification, Revision 1.4; RE, RS, CE, CS.



t_0 — TIME AT TRIGGER EVENT
t_1 — START OF PULSE PERIOD
t_2 — START OF DELAYED PULSE
UL — UPPER LEVEL VOLTAGE
LL — LOWER LEVEL VOLTAGE
PA — PULSE AMPLITUDE = (UL - LL)
TL — TRIGGER LATENCY = $t_1 - t_0$
PD — PULSE DELAY = $t_2 - t_1$
PW — PULSE WIDTH
LE — LEADING EDGE TRANSITION TIME
TE — TRAILING EDGE TRANSITION TIME
OS — OVERSHOOT
US — UNDERSHOOT
ABS — ABERRATIONS (pk-pk) = (OS + US)/PA * 100%

Figure 1.2 Definitions of Pulse Characteristics

2.1 RECEIVING INSPECTION

Check the shipment at the time of delivery and inspect each box for damage. Describe any box damage and list any shortages on the delivery invoice.

2.1.1 Unpacking Instructions

1. **Unpack the boxes.** Unpack the boxes in a clean and dry environment. Save all the packing material in case the instrument must be returned for repair.
2. **Inspect the shipment for damage.** Inspect the equipment carefully for any signs of mechanical damage regardless of the condition of the shipping boxes.
3. **If necessary, file a claim.** In the case of mechanical damage, call the shipper immediately and start the claim process.
4. **Call Wavetek.** Call Wavetek's Customer Service representative (619 279-2200) to inform them that the shipment arrived damaged. Please be prepared to provide a detailed damage report.

2.1.2 Returning Equipment

Follow these steps when you return equipment to Wavetek:

1. **Save the packing material.** Always return equipment in its original packing material and boxes. If you use inadequate material, you'll have to pay to repair any shipping damage as carriers won't pay claims on incorrectly packed equipment.
2. **Call Wavetek Customer Service and ask for a return authorization.** The Wavetek Customer Service representative (619 279-2200) will ask for your name, telephone number, company name, equipment type, model number, serial number, and a description of the problem.
3. **Pack and ship the equipment.**

2.2 PREPARATION FOR STORAGE OR SHIPMENT

2.2.1 Packaging

If at all possible, always use the original shipping container. However, when using packing materials other than the original, use the following guidelines:

1. Wrap the Model 1391 in ESD sensitive packing material.
2. Use a double-walled cardboard shipping container.

Protect all sides, including the top and bottom, with shock absorbing material (minimum of 2 inch thick material) to prevent movement of the Model 1391 within the container. Seal the shipping container with approved sealing tape. Mark "FRAGILE" on all sides, top, and bottom of the shipping container.

2.2.2 Storage

The Model 1391 should be stored in a clean, dry environment. In high humidity environments, protect the Model 1391 from temperature variations that could cause internal condensation. The following environmental conditions apply to both shipping and storage;

Temperature	–40°C to +71°C
Relative Humidity	not controlled, non-condensing.
Altitude	<15000 ft
Vibration	< 2g
Shock	< 40g

2.3 PREPARATION FOR USE

Paragraph 2.3 covers the following topics:

Logical Address Selection
Data Transfer Bus Arbitration
Installation

2.3.1 Logical Address Selection

The VXI chassis Resource Manager identifies units in the system by the unit's logical address. The VXI logical address can range from 0 to 255. However, addresses 0 and 255 are reserved for special functions. Address 0 identifies the Resource Manager. Address 255 permits the Resource Manager to dynamically address the unit based on the unit's VXI chassis slot.

To change the Model 1391's logical address, use the eight position DIP switch (figure 2-1) accessible from the side panel. The Model 1391 uses binary values (2^0 to 2^7) to set the address using the active low address switch. This means the OFF position represents a logical 1. Conversely, an ON position represents a logical 0. Switch position number one is the least significant bit of the address. Insert A in figure 2-1 illustrates a switch set to a logical address of 3.

Wavetek ships the Model 1391 with a logical address of 255 for Dynamic Configuration. Refer to insert B in figure 2-1.

2.3.2 Data Transfer Bus Arbitration

The Model 1391 has VMEbus Mastership capability. This means the Pulse Generator, when enabled, sends Responses and Events as signals to its Commander. The Model 1391 cannot drive the interrupt lines.

The Model 1391 is configured as a level 3 requestor by the factory. The level 3 Bus Request and Bus Grant lines are used (BR3*, BG3IN*, and BG3OUT*). The other Bus Grant lines are daisy-chained by jumpers. The VMEbus specifications describe three priority schemes: Prioritized, Round-robin, and Single level. The Prioritized arbitration assigns the bus according to a fixed priority scheme where each of four bus lines has a priority from highest (BR3*) to lowest (BR0*). Round-robin arbitration assigns the bus on a rotating basis. Single level arbitration only accepts requests on BR3*.

If a different requestor level is required, the jumpers must be changed. The following instructions and figure 2-2 will aid in reconfiguring the Model 1391 to

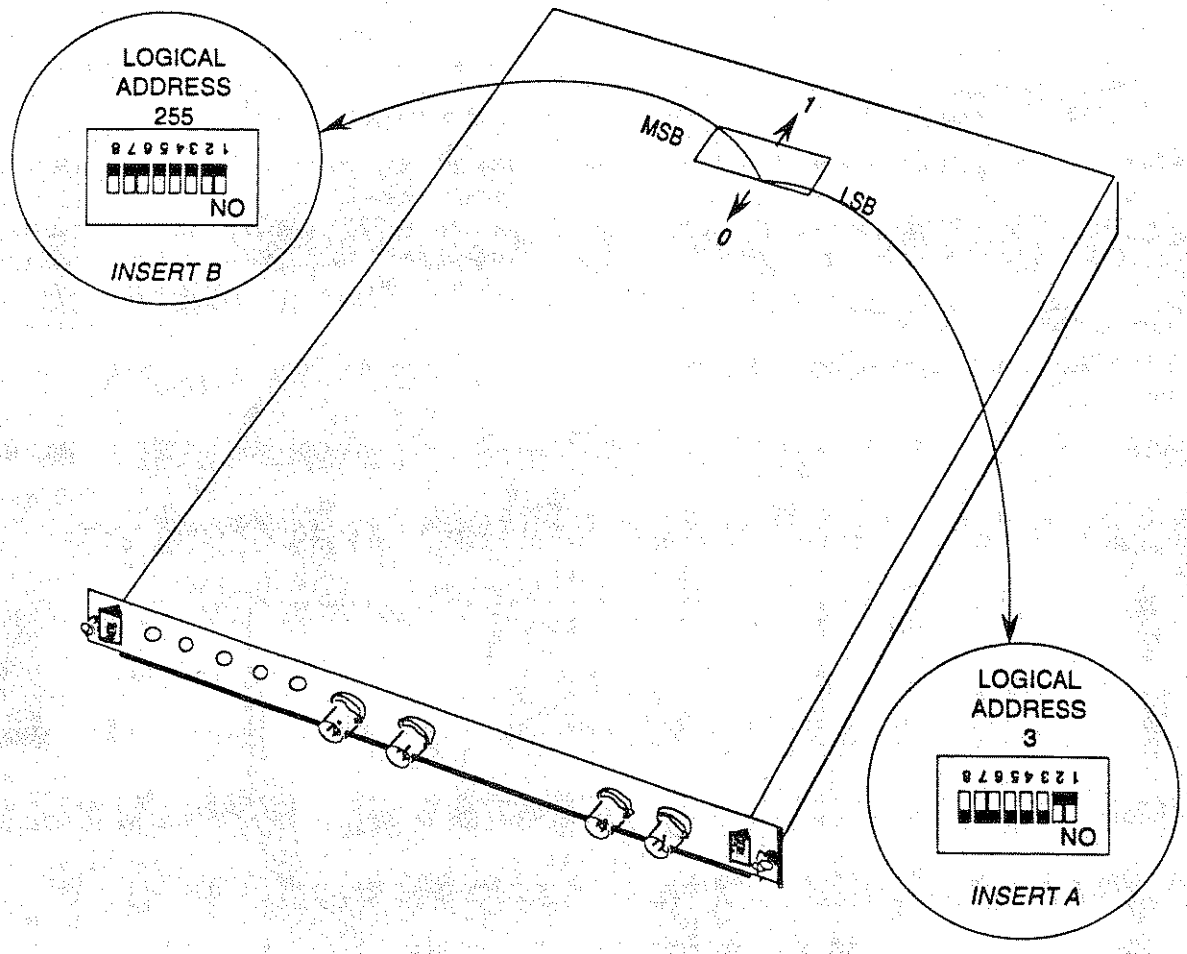


Figure 2-1. Set the Logical Address

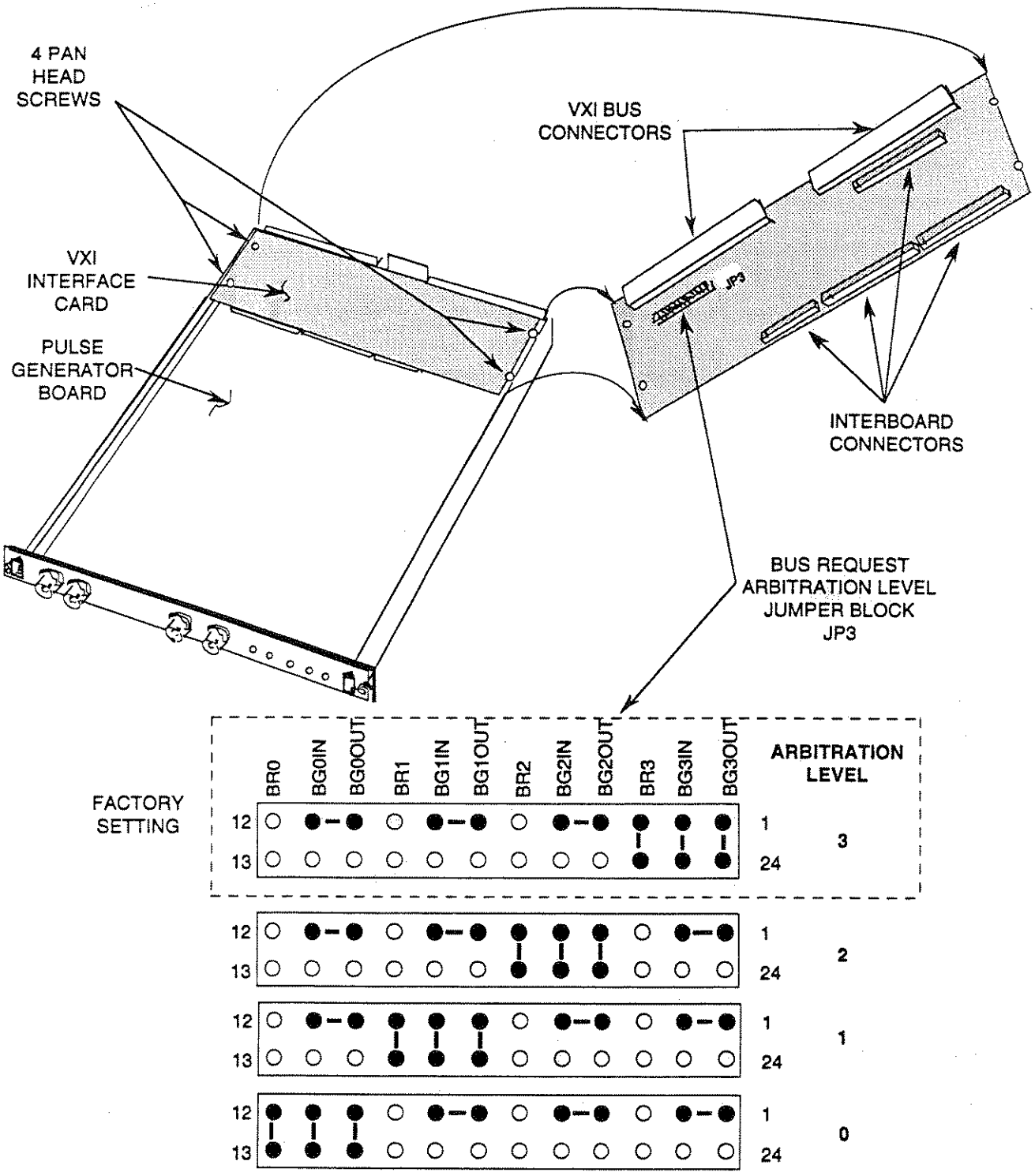


Figure 2-2. Bus Arbitration Level Jumpers

a new level. Refer to the VMEbus specification for more information on *'data transfer bus arbitration'*.

CAUTION

The Pulse Generator contains CMOS devices which are sensitive to static electricity. When performing the bus arbitration level change, static electricity discharge straps should be worn.

1. Remove the four flat head screws on the Model 1391 left side panel, remove the panel.
2. Remove the four pan head screws holding the VXI Interface card to the main Pulse Generator board.
3. Slowly and gently lift the VXI Interface card up from the Pulse Generator board. Considerable force may be required as there are four connectors between the two boards with a total of 136 pins. Do not use a metallic prying tool.
4. Change the data transfer bus arbitration jumpers to the desired level. Refer to figure 2-2.
5. Carefully install the VXI Interface card onto the Pulse Generator board. Install the four pan head screws, the side panel and the four flat head screws.

2.4 INSTALLATION

The instrument will be installed in a VXI mainframe in any slot except slot 0 (zero). When inserting the instrument into the mainframe, it should be gently rocked back and forth to seat the connectors into the backplane receptacles. The ejectors will be at right angles to the front panel when the instrument is properly seated into the backplane. The two captive screws above and below the ejectors are used to secure the instrument into the chassis.

2.5 INITIAL CHECKOUT AND OPERATION VERIFICATION

This procedure provides the operator, service technician, receiving inspector, etc. with a quick method of verifying the functional operation of the Model 1391. This procedure does not test the unit's specifications. This procedure assumes the Model 1391 is properly installed in a "C" size VXI chassis with a VXI controller in slot 0. Required tools and test equipment are given in table 2-1.

Table 2-1. Test Equipment and Tools

Equipment	Comments
Oscilloscope	Bandwidth: ≥100 MHz
Signal Source	Frequency: 10 kHz
	Output: ±1V sine wave
BNC 50Ω Feed-through (2ea)	Accuracy: 0.5% Power: 2W
BNC Coax Cable (3ea)	RG58U, 3 ft. length

Because each step in the procedure is dependent on the preceding step, start with step 1 and continue through to the end. Do not send any command unless specifically instructed to do so within the procedure.

1) Verify proper LED operation during instrument power-up

LED	Normal Result
Run	On
Fail	Off
MODID	Flashes
A16	Flashes
A24	Off

2) Send: `*tst?`

If response = 0, continue

If response ≠ 0, decode error value (see Appendix D).

NOTE

If the test fails on a new or newly factory repaired unit, call Wavetek Customer Service at 619/279-2200 or FAX 619/565-9558.

3) Connect two coax cables between the Model 1391 PULSE OUT and SYNC OUT connectors and the

oscilloscope. Use a 50Ω terminator on each cable. Connect the SYNC OUT to CH1 and the PULSE OUT to CH2, and synchronize the oscilloscope internally from CH1.

Send: `outp on;:mark on`

Verify the SYNC waveform on CH1 is a 1 MHz, TTL level square. Verify the pulse waveform on CH2 as follows:

NOTE

Numeric values should not be verified for accuracy in this operational checkout, but should be checked visually on the oscilloscope trace for approximate accuracy. Use the Performance Verification Procedure in Section 5 of this manual, if required, to test the unit to specification.

- single pulse; 1 µs period
- ±0.5 V upper and lower levels
- 250 ns pulse width
- ≤5 ns leading and trailing transition times

4) Verify the various pulse functions (waveforms) and pulse characteristics:

Send: `puls:del 600e-9`

Verify the single pulse is now delayed 600 ns relative to the rising edge of the SYNC.

Send: `puls:doub on`

Verify double pulses with the second pulse delayed 400 ns relative to the rising edge of the SYNC.

Send: `func squ`

Verify a 50% square wave output coincident with the SYNC.

Send: `func puls;freq 200e3`

Verify the waveform returns to double pulse, and that the waveform period (determined by the sync) has increased to 5 µs.

Send:
```
puls:doub:del 2e-6
puls:widt 8e-7
tran:stat on
tran:lead 1e-7;tra 3e-7
```

Verify the double pulses now have a leading transition time of 100 ns, a pulse width (between the 50% points) of 800 ns, a trailing transition time of 300 ns, and that the second is delayed from the first by 2 µs.

5) Verify the output levels as follows:

Send: `volt:high 4;low -2`

Verify the output levels change from ±0.5 V to a low level of –2V and a high level of +4V.

6) Set the external generator up for a ±1V, 10 kHz sine wave. Connect the external signal to the Model 1391 TRIG IN connector.

Send:
```
init:cont off
trig:lev 0
```

Verify a double pulse with all of the characteristics set up in steps 3 and 4, except that the pulse period is now triggered by the 10 kHz rate set by the external signal.

Send: `trig:coun 3`

Verify the double pulses are now triggered for 3 periods (six pulses in all) at the 10 kHz rate.

Send: `trig:gate on`

Verify the double pulse periods are gated on for approximately half the time by the 10 kHz external signal.

Send: `init:cont on`

Verify continuous operation.

7) Move the cable from the the TRIG IN connector to the the PAM IN connector.

Send: `pulm on;ampl pos`

Verify the lower level is at zero volts and that the upper level is being amplitude modulated around its 4V median level with a ±2V sinusoidal envelope.

8) This completes the operational verification. Disconnect the test equipment.

3.1 Introduction

This section provides the Operator/Programmer with the information needed to operate the Model 1391 Pulse Generator in a VXI system. The unit resides in a VXI chassis and is subject to all of the restrictions and benefits of that environment.

Paragraph 3.2 describes the Model 1391 connectors and LED indicators. Paragraph 3.3 defines the Model 1391 SCPI programming messages. Paragraph 3.4 demonstrates how to operate the Model 1391 using the defined messages.

3.2 Connectors and LED Indicators

This paragraph describes the Model 1391 front panel connectors and LED indicators. Figure 3-1 illustrates the front panel; bold numbers identify the indicators and connectors. Table 3-1 describes the function of each item shown in figure 3-1.

3.3 Model 1381 Programming

The Model 1391 communicates within the SCPI (Standard Commands for Programmable Instruments) and IEEE 488.2 standards. It may also communicate using the CIIL (Control Interface Intermediate Language) language described in the MATE specification as an option. When the CIIL language is included, the "Native" SCPI language is also retained, because it has a much broader set of features. For MATE/CIIL information, refer to Appendix A at the end of this manual.

The standard Model 1391 must respond to two types of commands: SCPI commands and IEEE 488.2 Common Commands. The IEEE 488.2 Common Commands support functions that are common to all instruments, such as reset, self test and status reporting. Common Commands are non-heirarchical (can be included within SCPI commands without disturbing their heirarchical relationships) and are easily identified by their leading asterisk (*).

SCPI commands support functions that are specific to the instrument. The SCPI language is heirarchical, requiring commands to be entered in a very specific fashion, and this manual contains tabular and graphical representations of the logic used by the SCPI *parser* (the 1391's firmware) to process commands.

This section provides the following information:

3.3.1 SCPI Command Table

Table 3-2 lists the SCPI commands used in the Model 1391 and indicates their hierarchical relationships. The IEEE 488.2 Common Commands are listed in a separate table (Table 3-4). The SCPI Command Table is organized as follows:

Keyword	Parameter Form	Notes
[SOURce]		
:FREQuency		
[:CW]	<numeric_value>	
:MODE	<list>	
STARt	<numeric_value>	
STOP	<numeric_value>	

The indentations of *keywords* indicates their hierarchical relationships according to a tree system. The left-most edge is called the *root node*. Keywords closer to the root node are higher in hierarchy; lower nodes are to the right of their parent node. To program or query a settable parameter, the full path must be defined to reach the keyword appended with the required parameter form. A SCPI programming string typically starts at the root node and proceeds to the right through branch nodes to the *leaf node*. This string of keywords separated by colons and completely defining a single path is defined as a Program Header, and is commonly referred to as a "command" (see paragraph 3.3.2) or as a "query" (see paragraph 3.3.2.6). A Program Header followed by Program Data is defined as a Program Message Unit (paragraph 3.3.2.1).

In the example above, the left-most keyword, [SOURce], is directly off the root node. Nodes in this position are called *Subsystems*, and all keywords

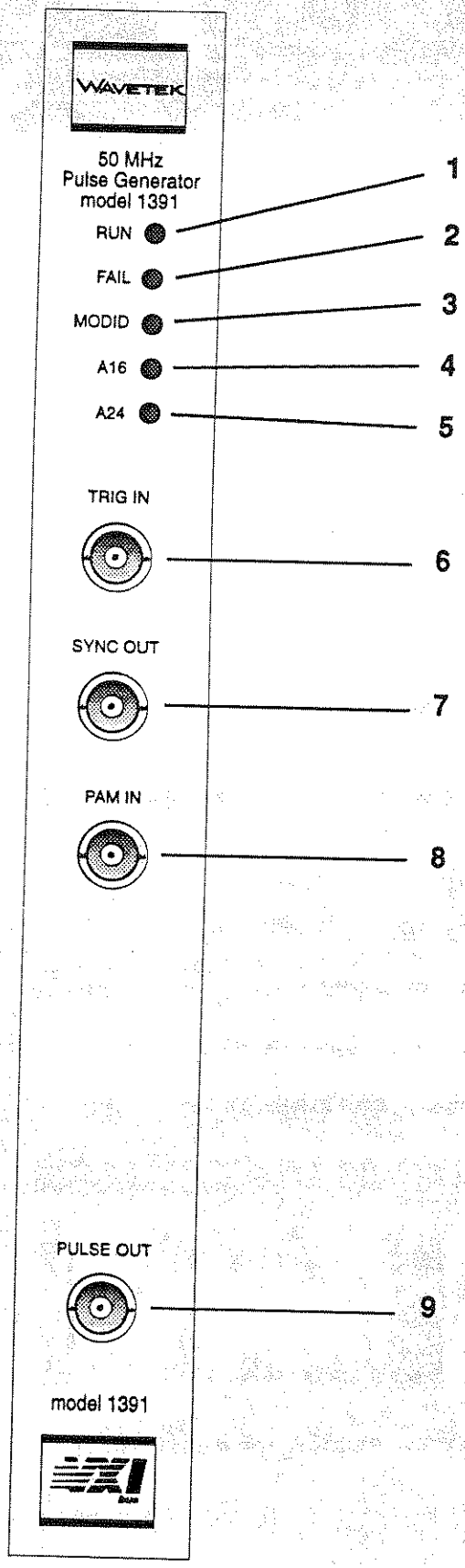


Figure 3-1. Model 1391 Front Panel

Table 3-1. Model 1391 Front Panel

Item	Item Name	Function
1	RUN LED Indicator	When lit, indicates the VXIbus Interface Module microprocessor is running.
2	FAIL LED Indicator	When lit, indicates the VXIbus Interface Module registers are not initialized.
3	MODID LED Indicator	This indicator turns on momentarily indicating the Resource Manager has detected the presence of the model 1391.
4	A16 LED Indicator	When lit, indicates that devices on the VXIbus are accessing the generator's A16 registers.
5	A24 LED Indicator	This indicator illuminates during a VMEbus access to the A24 shared memory. This LED will not function in a Model 1391.
6	TRIG IN Connector	This connector receives the external trigger signal for the Model 1391's triggered, gated, and burst modes.
7	SYNC OUT Connector	This connector outputs TTL pulses for waveform synchronization.
8	PAM IN Connector	This connector is the input for external signals to Pulse Amplitude Modulate the PULSE OUT levels.
9	PULSE OUT Connector	This connector supplies the generator's waveform output. Output level is 150 mVpp to 16 Vpp into 50Ω.

indented under [SOURce] are part of the Source Subsystem. FREQuency is one of the main parameters under the Source Subsystem. The third level keywords under FREQuency set or query the various frequency related parameters. The brackets around the SOURce and CW keywords indicate that they are *implied nodes*, and they may be included in or omitted from the message at the programmer's option. When included, do not use the brackets in the command. Referring to Table 3-2, [SOURce] is the only Model 1391 Subsystem which is in brackets. This is the default Subsystem, and is assumed unless another Subsystem is specified at the start of a command.

The root node itself is an implied node and is not directly programmed. A colon at the start of a command resets the SCPI parser (included in instrument firmware) to the root node. A leading colon at the root node location is unnecessary (see paragraph 3.3.2.3).

3.3.1.1 Long and Short Form Keywords

The Model 1391 recognizes specific keywords that must be in the accepted long or short format. No other form of the keyword is accepted. For example, to send 'frequency' as part of a message, the short form keyword, shown in the table as upper case letters 'FREQ', or the long form of the same keyword containing both upper and lower case characters 'FREQuency' may be sent. Equal weight is given to upper and lower case characters when sending messages to the Model 1391.

3.3.2 Command Message Format

The following paragraphs provide the programmer/ operator with an introduction to the general rules that must be followed when sending messages to the Model 1391. For an understanding beyond what is covered in this paragraph, refer to the appropriate SCPI and IEEE 488.2 documents.

Operating the Model 1391 is easy, provided the programmer/operator pays strict attention to the message format, as shown in this manual. Each character, including spaces, must be properly placed or the Model 1391 will record any unrecognized parts of the command string as an error.

Table 3-2 shows the Model 1391 message structure and message relationships. Refer to this while working within this paragraph.

Note

The Model 1391 records programming errors in its memory. The programmer/operator must use the 'SYSTEM:ERROR?' *query to review these errors.*

3.3.2.1 Program Message Unit

The Program Header (command or query) has been previously defined as a complete single path to a leaf node. It consists of one or more keywords separated by colons. It may also have a leading colon used to explicitly select the root node as the starting point. A Program Message Unit, <pmu>, consists of a Program Header followed (optionally) by Program Data.

3.3.2.2 Program Message

The Program Message (message) consists of one or more <pmu>'s deliminated by semicolons and followed by a Program Message Terminator, <pmt>.

3.3.2.3 Program Message Delimiters

To piece together the Program Message, the Model 1391 expects commands and parameters in the correct order (per Table 3-2), separated by defined delimiters: colons (:), semicolons (;), and spaces ( ).

Use the colon to separate keywords (nodes) within a Program Message Unit, for example,

```
VOLT:LEV:IMM:AMPL 5
```

Do not insert spaces between keywords and colons. Placing the optional colon at the beginning of a Program Message Unit ensures the parser starts from the "root" or top level. For example, a complete message with the leading colon is as follows:

```
:OUTP ON
```

The leading colon at the beginning of any new message is optional because the Program Message Terminator (<pmt>) at the end of the previous message sets the parser to the "root" level. The leading colon is not shown for most messages in this section.

The semicolon is used as a Program Message Unit Separator (<pms>). It permits the message units to be linked together in a single message. The colon may follow the semicolon to start the next message unit at the "root". For example,

```
SOUR:FREQ:CW 1E4;:OUTP ON
```

Without the colon following the semicolon, the message must start within the same subsystem as the previous message. For example:

```
SOUR:FUNC SQU;FREQ:CW 1E4
```

A space separates the Program Header from its data, as shown in the previous example.

3.3.2.4 Parameter Forms

For the Model 1391, parameters may be in the form of a decimal numeric value (numeric_data), alpha characters (character_data), or Boolean data. Examples of all three are:

```
FREQ 1000 (numeric_data)
FUNC SQU (character_data)
OUTP ON (Boolean_data)
```

Notice that in all cases, a space separates the header from data.

Numeric data values for most parameters may be in the form of an integer, a fixed or floating point value, or a special keyword as shown in the following:

integer;

```
FREQ 1000
```

fixed point;

```
FREQ 10.1
```

floating point;

```
FREQ 10E3
```

special form character;

```
FREQ MIN
```

When any of the three special form decimal numeric value keywords, 'MINimum', 'MAXimum', or 'DEFault', are sent, the parameter being addressed is set to a predetermined numeric value. The 'MAXimum' and 'MINimum' numeric values are the upper and lower limit values of the parameter. The 'DEFault' numeric value is within the limits of the parameter selected. Defaults values are listed in paragraph 3.4.3.

The Model 1391 uses several character data keywords. These are shown in Table 3-2.

Boolean data expresses an enabled ('on' or '1') or disabled ('off' or '0') state.

3.3.2.5 Program Message Terminators

The Model 1391 accepts New Line (NL, <LF>), END, or NL with END as the Program Message Terminator (<pmt>). However, the END (<EOI>) is the preferred <pmt> because it initiates an immediate transfer from the command/data buffer to the Language Processor for parsing. The other terminators may be delayed until the buffer fills.

Table 3-2. Model 1391 Command Summary

KEYWORD	PARAMETER FORM	NOTES
CALibrate [:ALL]?		
INITiate [:IMMediate] :CONTinuous	<Boolean_data> (<OFF | 0 | ON | 1>)	
OUTPut :ECLTrg<n> [:STATe] :SOURce [:STATe] :SUMBus [:STATe] :TTLTrg<n> [:STATe] :SOURce	<Boolean_data> (<OFF | 0 | ON | 1>) <TRIP | PULSe> <Boolean_data> (<OFF | 0 | ON | 1>) <Boolean_data> (<OFF | 0 | ON | 1>) <Boolean_data> (<OFF | 0 | ON | 1>) <TRIP | PULSe>	<n>=0 to 1 VXIbus ECLTrigger lines <n>=0 to 7 VXIbus TTLTrigger lines
RESet		
[SOURce] :FREQuency [:CW | FIXed] :FUNCtion [:SHAPe] :MARKer :TYPE [:STATe] :PULSe :WIDTh :DELay :DOUBle :DELay [:STATe] :POLarity :PERiod :TRANsition :STATe [:LEADing] :TRAiling :AUTO :SUMBus [:STATe] :VOLTage [:LEVel] [:IMMediate] :HIGH :LOW [:AMPLitude] :OFFSet	<numeric_value> (<MINimum | MAXimum | DEFault>) <shape_name>, (<PULSe | SQUare>) <CLOCk | GATE> <Boolean_data> (<OFF | 0 | ON | 1>) <numeric_value> (<MINimum | MAXimum | DEFault>) <numeric_value> (<MINimum | MAXimum | DEFault>) <numeric_value> (<MINimum | MAXimum | DEFault>) <Boolean_data> (<OFF | 0 | ON | 1>) <NORMal | COMPlement | INVerted> <numeric_value> (<MINimum | MAXimum | DEFault>) <Boolean_data> (<OFF | 0 | ON | 1>) <numeric_value> (<MINimum | MAXimum | DEFault>) <numeric_value> (<MINimum | MAXimum | DEFault>) <Boolean_data> (<OFF | 0 | ON | 1>) <Boolean_data> (<OFF | 0 | ON | 1>) <numeric_value> (<MINimum | MAXimum | DEFault>) <numeric_value> (<MINimum | MAXimum | DEFault>) <numeric_value> (<MINimum | MAXimum | DEFault>) <numeric_value> (<MINimum | MAXimum | DEFault>)	

Table 3-2. Model 1391 Command Summary (Continued)

KEYWORD	PARAMETER FORM	NOTES
[SOURce] (Continued) :PULM [:STATe] :AMPLitude	<Boolean_data> (<OFF | 0 | ON | 1>) <BIPolar | POSitive | NEGative>	
STATus :OPERation :CONDition? :ENABle [:EVENt]? :QUEStionable :CONDition? :ENABle [:EVENt]? :PRESet	<numeric_value> <numeric_value>	
SYSTem :ERRor? :DATE :TIME :VERSion? :LANGuage :CIIL	<year>, <month>, <day> <hour>, <minute>, <second>	
TRIGger :COUNt :LEVel :GATE [:STATe] :MODE :MODE :SLOPe :SOURce :TIMer	<numeric_value> (<MINimum | MAXimum | DEFault>) <numeric_value> (<MINimum | MAXimum | DEFault>) <Boolean_data> (<OFF | 0 | ON | 1>) <SYNChronous | EXTWidth> <MASTer | SLAVe> <POSitive | NEGative> <INTernal | BUS | EXTernal | TTLTrg<n>| ECLTrg<n> | TOFF> <numeric_value> (<MINimum | MAXimum | DEFault>)	<n> = 0 to 7 VXIbus TTLTrigger lines or 0 to 1 ECLTrigger lines.
DIAGnostic :CALibrate? :CALibrate :MEASure :SAVE :INIT	<step> <step>,<numeric_value>	

3.3.2.6 Queries

Unless otherwise indicated, each header with a parameter form also has a query form so that the current setting may be reported back. A query is programmed by following the leaf node keyword with a question mark (?), no space. For example, send:

```
SOUR:FREQ:CW?
```

or the reduced form:

```
FREQ?
```

to query the frequency setting. The response for this query is a floating point numerical value representing the frequency in Hertz. For example, if the response is 1 kHz, the returned value is:

```
1.000000E+03
```

For queries that include parameters, the question mark and a space are inserted prior to the parameter:

```
FREQ? MAX
```

Some commands may exist in query form only:

```
SYSTEM:ERROR?
```

Some queries are mandated such as `*ESE?`, `*SRE?`, and `*TST?`; see paragraph 3.3.4.

3.3.3 Model 1391 SCPI Commands

This paragraph introduces the operator to the Model 1391 SCPI command set. Paragraph 3.4 covers the relationship between these units. For a description of message format, refer to paragraph 3.3.2. This paragraph uses only the short form keyword recognized by the Model 1391 (refer to Table 3-2). Program Message Terminators are assumed, and therefore not shown in the examples. However, most optional keywords are shown to document the program flow.

3.3.3.1 CALibrate Subsystem

The IEEE-488.2 calibration query (see paragraph 3.3.2.6) causes an internal self calibration to be performed and a response to be placed in the Output Queue. The response to the `*CAL?` query is an ASCII string representing an integer value. The value of 0 is returned if the self calibration passed and a non-zero value in the range of 32767 to -32768 is returned if the self calibration failed. The interpretation of the value returned in the event of a failed self calibration is listed in Appendix C.

The `*CAL?` query invokes the same internal self calibration functions and returns the same reponse as the SCPI `CALibrate[:ALL]?` query. Following is the CALibrate Substem excerpted from the SCPI Command Table:

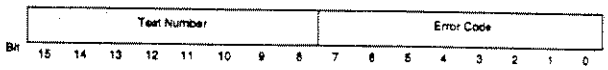
```
CALibrate
  [:ALL]?
```

`CALibrate[:ALL]?`

Performs a calibration of the output amplitude and offset voltage levels and stores the calibration data in non-volatile memory. If the calibration is successful, use of the data is enabled. If the calibration is unsuccessful for any reason, use of the data is disabled and default correction factors are used.

This query returns a value of 0 if the auto-calibration is successful and a non-zero positive integer value if not. The response value will indicate the nature of the failure.

The value of a 16-bit Self Calibration Status Word is returned in response to the calibration query. The format of the Status Word is shown below:



Self Calibration Status Word

The Self Calibration Status Word is split into two fields, one occupying the lower eight bits and the other occupying the upper eight bits.

The Calibration Number field contains the number of the first sub-calibration in which a failure was detected. Sub-calibration numbers range from 1 to 255. Sub-calibrations are performed in the same sequence as they are numbered.

The Error Code field contains a bit weighted code that is unique to the sub-calibration. Refer to Appendix C for more information.

3.3.3.2 INITiate Subsystem

```
INITiate
  [:IMMediate]
  :CONTinuous     <Boolean>
```

`INITiate[:IMMediate]`

This command is included to support the SCPI specification, but it does not alter the setup of the model 1391.

`INITiate:CONTinuous <ON|1|OFF|0>`

This command selects between continuous mode of operation and a non-continuous (triggered, gated, or burst) mode of operation.

3.3.3.3 OUTPut Subsystem

```
OUTPut
  :ECLTrg<n>
     [:STATe]      <Boolean_data>
     :SOURce       <TRIP | PULSe>
  [:STATe]         <Boolean_data>
  :SUMBus
    [:STATe]       <Boolean_data>
  :TTLTrg<n>
     [:STATe]      <Boolean_data>
     :SOURce       <TRIP | PULSe>
```

`OUTPut:ECLTrg<n>[:STATe] <Boolean>`

Enables the selected model 1391 SOURce signal to drive one of the VXIbus backplane ECL Trigger Lines. Each ECL Trigger Line output can be separately enabled. Valid numeric suffixes (<n>) are in the range 0 through 1. Default selection is "OFF" (0), enabled with "ON" or "1".

`OUTPut:ECLTrg<n>:SOURce <TRIP|PULSe>`

Selects the signal (internal to the 1391) which is to be enabled to drive one of the backplane ECL Trigger Lines. The default selection is the "trigger pulse", TRIP, which exists at the circuit node between a signal selector and the inputs to the width and delay *one-shot generators*. The selector chooses one signal among several, dependant upon operating mode, to trigger the one-shots. The PULSe signal is the output of the one-shots before it is applied to the analog output conditioning circuit blocks.

`OUTPut[:STATe] <Boolean>`

Controls the state of the function output relay, turning the signal to the PULSE OUT on or off. Default selection is "OFF" (0), enabled with "ON" or "1".

`OUTPut:SUMBus[:STATe] <ON|1|OFF|0>`

Connects or disconnects the Model 1391 to the VXIbus backplane SUMBUS line. Default selection is "OFF" (0); enabled with "ON" or "1". When ON, the Model 1391 drives the SUMBUS with a current proportional to the voltage waveform at PULSE OUT.

`OUTPut:TTLTrg<n>[:STATe] <Boolean>`

Enables the selected model 1391 SOURce signal to drive one of the VXIbus backplane TTL Trigger Lines. Each TTL Trigger Line output can be separately enabled. Valid numeric suffixes (<n>) are in the range 0 through 7. Default selection is "OFF" (0), enabled with "ON" or "1".

`OUTPut:TTLTrg<n>:SOURce <TRIP|PULSe>`

Selects the signal (internal to the 1391) which is to be enabled to drive one of the backplane TTL Trigger Lines. The default selection is the "trigger pulse", TRIP, which exists at the circuit node between a signal selector and the inputs to the width and delay *one-shot generators*. The selector chooses one signal among several, dependant upon operating mode, to trigger the one-shots. The PULSe signal is the output of the one-shots before it is applied to the analog output conditioning circuit blocks.

3.3.3.4 RESet Subsystem

`RESet`

Resets all parameters to their default state (see paragraph 3.4.3).

3.3.3.5 SOURce Subsystem

```
[SOURce]
  :FREQuency
    [:CW | FIXed] <numeric_value>
  :FUNCtion
    [:SHAPe]      <PULSe | SQUare>
  :MARKer
    :TYPE         <CLOCk | GATE>
    [:STATe]      <Boolean>
  :PULSe
    :WIDTh        <numeric_value>
    :DELay        <numeric_value>
    :DOUBle
      :DELay      <numeric_value>
      [:STATe]    <Boolean>
    :POLarity     <NORMal|COMPlement|
                  INVerted>
    :PERiod       <numeric_value>
    :TRANsition
      :STATe      <Boolean>
      [:LEADing]  <numeric_value>
      :TRAiling   <numeric_value>
        :AUTO     <Boolean>
  :SUMBus
    [:STATe]      <Boolean>
  :VOLTage
    [:LEVel]
      [:IMMediate]
        :HIGH     <numeric_value>
        :LOW      <numeric_value>
        [:AMPLitude] <numeric_value>
        :OFFSet   <numeric_value>
```

`[SOURce:]FREQuency`
`[:CW | FIXed ] <numeric_value>`

Alternate "Hz" units for controlling the pulse period. FREQuency and PERiod are "coupled" parameters, so that programming one updates the value of the other. "CW" and "FIXed" are interchangable. Parameter values range from a MINimum of 0.001 Hz to a MAXimum of 100 MHz. DEFault value is 1 MHz.

`[SOURce:]FUNCtion`
`[:SHAPe] <PULSe|SQUare>`

Selects the shape of the output signal. For the Model 1391, the Functions available at the PULSE OUT are the PULSe and the SQUare. Additionally, with the PULSe selected, other PULSe parameters in this Subsystem are used to select single, delayed, or double pulses within each period. Default selection is PULSe.

`[SOURce:]MARKer[:STATe] <ON|1|OFF|0>`

Enables or disables the SYNC output. Default selection is "OFF" (0); enabled with "ON" or "1".

`[SOURce:]MARKer:TYPE <CLOCk|GATE>`

Selects the method used to generate the SYNC output.

- CLOCk — A signal derived from the repetition rate (period) generator.
- GATE — A signal derived from the triggering circuitry. The GATE signal goes true when a trigger/gate/burst cycle is initiated, and goes false when the trigger/gate signal goes false.

`[SOURce:]PULSe:WIDTh <numeric_value>`

Sets the width of the pulse waveform in seconds. Defined as the time between the 50% points of leading and trailing transitions. Each pulse period can have single or double pulses. Width parameter values range from a MINimum of 10 ns to a MAXimum of 2000 s. DEFault value is 250 ns.

`[SOURce:]PULSe:DELay <numeric_value>`

Sets the delay of a single pulse waveform in seconds. Defined as the time between the start of a pulse period (50% point of SYNC OUT) and the 0% point of the leading transition of a single pulse. Delay parameter values range from a MINimum of 0 ns to a MAXimum of 2000 s. DEFault value is 0 ns.

`[SOURce:]PULSe:DOUBle:DELay`
`<numeric_value>`

Sets the delay of a double pulse waveform in seconds. Defined as the time between the start of a pulse period (50% point of SYNC OUT) and the 0% point of the leading transition of the second pulse. Delay parameter values range from a MINimum of 20 ns to a MAXimum of 2000 s. DEFault value is 400 ns.

`[SOURce:]PULSe:DOUBle[:STATe] <ON|1|OFF|0>`

Enables or disables the double pulse function. Default selection is "OFF" (0); enabled with "ON" or "1". Enabling the double pulse selects the `PULSe:DOUBle:DELay` parameter in place of the `PULSe:DELay` parameter.

`[SOURce:]PULSe:POLarity <NORMal|COMPlement>`

Allows the internal signal at the *one-shot generator* output to be inverted (complemented) before being applied to the output circuits and to the PULSE OUT. Default selection is NORMal.

- NORMal Pulse leading transitions are rising transitions. Pulse width is active high.
- COMPlement Pulse leading transitions are falling transitions. Pulse width is active low.
- INVerted Alias for COMPlement.

`[SOURce:]PULSe:PERiod <numeric_value>`

Sets the period of the pulse waveform in seconds. Defined as the time between the 50% points of the rising transitions of two adjacent SYNC OUT waveforms (MARKer:TYPE CLOCk). This is the same as the time between two adjacent, *identical* transitions at the PULSE OUT. Each pulse period can have single or double pulses. Period parameter values range from a MINimum of 10 ns to a MAXimum of 1000 s. DEFault value is 1 µs. PERiod is "coupled" to the FREQuency parameter such that changing one parameter updates the other.

`[SOURce:]PULSe:TRANsition:STATe <ON|1|OFF|0>`

Sets the pulse transition time generators ON or OFF. Default is OFF. If the state is off, then the transitions are set to the minimum values of 5 ns. If the state is on, the transitions are determined by the values for LEADing and TRAiling.

`[SOURce:]PULSe:TRANsition[:LEADing] <numeric_value>`

Sets the width of the pulse waveform transitions in seconds when TRANsition state is ON. Defined as the time between the 10% point and 90% point of a leading transition. LEADing parameter values range from a MINimum of 5 ns to a MAXimum of 50 µs. DEFault value is 5 ns.

`[SOURce:]PULSe:TRANsition:TRAiling <numeric_value>`

Sets the width of the pulse waveform transitions in seconds when TRANsition state is ON. Programming this value sets "auto-trailing" OFF if it is ON. Defined as the time between the 10% point and 90% point of a trailing transition. TRAiling parameter values range from a MINimum of 5 ns to a MAXimum of 50 µs. DEFault value is 5 ns.

`[SOURce:]PULSe:TRANsition:TRAiling:AUTO <ON|1|OFF|0>`

When enabled, causes the parameter values for the TRAiling transition time to be set along with the LEADing transition time. When disabled, the TRAiling transition has its own parameter values, and LEADing and TRAiling transitions are independant, restricted only by the maximum 10:1 ratio. Default selection is "OFF" (0); enabled with "ON" or "1".

`[SOURce:]SUMBus[:STATe] <ON|1|OFF|0>`

Connects or disconnects the Model 1391 to the VXIbus backplane SUMBUS line. Default selection is "OFF" (0); enabled with "ON" or "1". When set to ON, the Model 1391 sums the waveform on the SUMBUS with the PULSE OUT waveform.

`[SOURce:]VOLTage[:LEVel][:IMMediate]:HIGH <numeric_value>`

Sets the amplitude in volts peak (50Ω) of the upper level of the pulse waveform at the PULSE OUT. Should be programmed along with the LOW LEVel parameter (see the NOTE below). HIGH level parameter values range from a MINimum of –7.850 V (50Ω) to a MAXimum of +8V (50Ω). DEFault value is +0.50 V (50Ω).

NOTE

The AMPLitude and OFFSet parameters, and the HIGH and LOW level parameters, are two ways of setting the output levels. Use HIGH and LOW together, or use AMPLitude and OFFSet together. These are "coupled" functions – setting up one pair causes the other pair to update to equivalent values.

`[SOURce:]VOLTage[:LEVel][:IMMediate]`
`:LOW <numeric_value>`

Sets the amplitude in volts peak (50Ω) of the lower level of the pulse waveform at the PULSE OUT. Should be programmed along with the HIGH LEVel parameter (see the NOTE above). LOW level parameter values range from a MINimum of –8V (50Ω) to a MAXimum of +7.850 V (50Ω). DEFault value is –0.50 V (50Ω).

`[SOURce:]VOLTage[:LEVel][:IMMediate]`
`:OFFSet <numeric_value>`

Sets the offset in volts dc (50Ω) of the pulse waveform at the PULSE OUT. Should be programmed along with the AMPLitude LEVel parameter (see the NOTE above). OFFSet parameter values range from a MINimum of –7.925 Vdc (50Ω) to a MAXimum of +7.925 Vdc (50Ω). DEFault value is 0.

`[SOURce:]VOLTage[:LEVel][:IMMediate]`
`[:AMPLitude] <numeric_value>`

Sets the amplitude in volts peak-to-peak (50Ω) of the pulse waveform at the PULSE OUT. Should be programmed along with the OFFSet LEVel parameter (see the NOTE above). AMPLitude parameter values range from a MINimum of 0.150 Vpp (50Ω) to a MAXimum of 16 Vpp (50Ω). DEFault value is 1 Vpp (50Ω).

NOTE

Restrictions on output levels: The sum of Vpk amplitude (half the programmed Vpp value) and the absolute offset value cannot exceed 8V. Additionally, for pulses less than 0.5 Vpp, this restriction is reduced to 2 V.

When setting the output in terms of HIGH and LOW levels, the HIGH level must be at least 0.15 V more positive than the LOW level. HIGH and LOW levels are programmed within a ±8 V window, reduced to a ±2 V window when (upper – lower) is less than 0.5 V.

`[SOURce:]PULM[:STATe] <ON|1|OFF|0>`

Connects or disconnects the PAM IN connector to the Model 1391. This enables or disables Pulse Amplitude Modulation. Default selection is "OFF" (0); enabled with "ON" or "1".

`[SOURce:]PULM:AMPLitude`
`<BIPolar|POSitive|NEGative>`

Determines how the Model 1391 pulse amplitude modulates the PULSE OUT signal using the PAM input. Default selection is BIPolar.

- BIPolar — The PULSE OUT waveform's lower level is a mirror image of its upper level. The instantaneous amplitude of the levels is a linear function of the signal at the PAM input.
- POSitive — The PULSE OUT waveform's lower level is fixed at the programmed `OFFSet` setting. The instantaneous amplitude of the upper level is a linear function of the signal at the PAM input.
- NEGative — The PULSE OUT waveform's upper-level is fixed at the programmed `OFFSet` setting. The instantaneous amplitude of the lower level is an inverted linear function of the signal at the PAM input.

3.3.3.6 SYSTem Subsystem

```
SYSTem
  :ERRor?
  :DATE     <year>,<month>,<day>
  :TIME     <hour>,<minute>,<second>
  :VERSion?
  :LANGuage
    :CIIL
```

`SYSTem:DATE <year>,<month>,<day>`

Sets the system date using the following format: yyyy,mm,dd.

`SYSTem:ERRor?`

Returns the next message from the system error queue. With each query, the unit returns a number followed by a brief description. The error queue holds up to eight errors, with one returned for each query sent, until the queue is empty. Table 3-3 describes the system error messages.

`SYSTem:TIME <hour>,<minute>,<second>`

Sets the system time using the following 24 hour format: hh,mm,ss.

`SYSTem:TIME?`

Returns the system's idea of the time in the following format:

`<hour>,<minute>,<second>`

`SYSTem:VERSion?`

Returns the system's firmware version number in the following format:

`<manufacturer>,<model>,<serial_number | 0>,<firmware_level | 0>`

`SYSTem:LANGuage:CIIL`

Used only with the MATE/CIIL option. A unit with the option installed uses CIIL as its default command language and SCPI as its alternate or "native" command language. Many of the more complex features in the SCPI command set are not implemented in CIIL. When in CIIL, the operator can use the CIIL GAL command to go to SCPI to accomplish a task needing the additional features. This command is used to return to CIIL from SCPI.

3.3.3.7 TRIGger Subsystem

```
TRIGger
  :COUNt          <numeric_value>
  :LEVel          <numeric_value>
  :GATE
    :MODE         <SYNchronous|EXTWidth>
    [:STATe]      <Boolean>
  :MODE           <MASTer|SLAVe>
  :SLOPe          <POSitive|NEGative>
  :SOURce         <INTernal|BUS|EXTernal
                  |TTLTrg<n>|ECLTrg<n>|TOFF>
  :TIMer          <numeric_value>
```

NOTE

When INITiate:CONTinuous is ON, the pulse generator mode is continuous, regardless of the settings in this Subsystem. When INITiate:CONTinuous is OFF, the mode is non-continuous and determined by these settings. When GATE[:STATe] is OFF, the pulse generator is in a triggered mode if the COUNt parameter is 1, or in a burst mode if the COUNt is set higher than 1. When the GATE[:STATe] is ON, the pulse generator is in a gated mode, using either the SYNChronous or EXTWidth sub-modes.

`TRIGger:COUNt <numeric_value>`

This command sets the number of pulse periods generated after a trigger is received. MINimum and DEFault value is 1. MAXimum value is 1,000,000.

`TRIGger:GATE[:STATe] <ON|1|OFF|0>`

This enables or disables gated mode of operation. See the above note. Default selection is "OFF" (0); enabled with "ON" or "1".

`TRIGger:GATE:MODE <SYNChronous|EXTWidth>`

Selects the GATE sub-mode. Default is SYNChronous.

- **SYNChronous** The pulse generator is quiescent at the lower level value. When a trigger is received, the generator outputs pulse periods (with selected pulse parameters) as long as the gat-

ing signal is true. When the gating signal goes false before the 50% point of the current period, the generator completes its current period, and then returns to the quiescent state. When the gating signal goes false beyond the 50% point of the current period, the generator completes its current period and the next full period, and then returns to the quiescent state.

- EXTWidth — When the triggering signal is false, the pulse generator outputs its lower level. When the triggering signal is true, the pulse generator outputs its upper level. Transition times can be programmed.

`TRIGger:LEVel <numeric_value>`

This command selects the voltage threshold level for the trigger comparator. This determines the triggering point on an external signal applied to the TRIG IN connector. Determine TRIGger SLOPe at the same time. MINimum value is –10 V and MAXimum value is +10V. DEFault value is 1V.

`TRIGger:MODE <MASTer|SLAVe>`

This command selects whether a 1391 module is independent, a master or a slave. A master supplies a trigger to other modules. A slave picks up the trigger from a master. Master/Slave triggering operation allows multiple modules in a VXIbus chassis to operate as a multiple channel pulse generator system. Timing between channels is very tightly controlled. When set to SLAVe, but not making use of a trigger from a master, then the module is "independent". Default is SLAVe.

- MASTer — The module supplies its SYNC OUT signal to an ECLTrg line for slave modules to use.
- **SLAVe** — Can pick up the master trigger from an ECLTrg line.

`TRIGger:SLOPe <POSitive|NEGative>`

This command selects whether a trigger is initiated as the external signal at TRIG IN passes through the threshold set by trigger LEVel in a positive-going or a negative-going direction. Default is POSitive.

`TRIGger:SOURce <INTernal|BUS|EXTernal|TTLTrg<n>|ECLTrg<n>|TOFF>`

Selects the source of the trigger signal. The trigger signal is used to initiate activity when the instrument is in a non-continuous mode of operation. Default is INTernal.

- EXTernal — Selects an external signal at the TRIG IN connector as the trigger source.
- **INTernal** — Selects the Model 1391 internal signal programmed by the trigger TIMer as the trigger source.
- BUS — Selects the IEEE-488 bus (488.1 GET command or 488.2 *TRG command) or the VXIbus (Word Serial Trigger command) as the triggering source.
- TTLTrg<n> — Selects one of the VXIbus TTL Trigger Lines from the backplane. Valid numeric suffixes are in the range 0 through 7.
- ECLTrg<n> — Selects one of the VXIbus ECL Trigger Lines from the backplane. Valid numeric suffixes are 0 and 1.
- TOFF — Disables all trigger sources.

`TRIGger:TIMer <numeric_value>`

Sets the period of an internal periodic signal source. The timer signal acts as a trigger when it is the selected trigger source. MINimum value is 20 ns and MAXimum value is 2000 s. DEFault value is 10 ms.

3.3.3.8 DIAGnostic Subsystem

```
DIAGnostic
  :CALibrate?      <step>
  :CALibrate
    :MEASure       <numeric_value>
    :SAVE
    :INIT
```

`DIAGnostic:CALibrate? <step>`

Initiates the manual calibration system. The <step> entered is the manual calibration step number that is to be set up for and performed. Some steps in the manual calibration procedure are handled automatically by the Model 1391, and this will be indicated by the return message. Manual steps requiring measurements with external test equipment and/or adjustments will return a message giving the appropriate instructions.

`DIAGnostic:CALibrate:MEASure <step>,<numeric_value>`

When the particular step requires an external measurement (see above), this command allows the operator to

enter the value measured into the Model 1391's volatile memory. These values may be entered step-by-step as the data is taken, or all at once at the end of a successful manual calibration. See the next command for making the new data non-volatile.

`DIAGnostic:CALibrate:SAVe`

Transfers the block of calibration data values from volatile to non-volatile memory. After the manual calibration has been successfully completed, the operator should send this command so that the new values are used to optimize the unit's accuracy.

`DIAGnostic:CALibrate:INIT`

Replaces the current calibration data values in non-volatile memory with a set of "default" values in ROM. The default values are nominal values which should aid in troubleshooting whether a unit's malfunction is due to miscalibration or to hardware failure.

3.3.3.8 STATus Subsystem

```
STATus
  :OPERation
    :CONDition?
    :ENABle       <NRf>
    [:EVENt]?
  :PRESet
  :QUEStionable
    :CONDition?
    :ENABle       <NRf>
    [:EVENt]?
```

`STATus:OPERation:CONDition?`

Returns the contents of the Operation Condition Register. The Model 1391 supports this query, but will only return the value "0", indicating operational condition.

`STATus:OPERation:ENABle <NRf>`

Sets the enable mask of the Operation Event Register, which allows true conditions to be reported in the summary bit. The Model 1391 supports the command by saving the mask value and by not generating an error, although the Status registers do not exist.

The <NRf> notation indicates that SCPI's <numeric_value> format is not used in this case. Refer to the IEE488.2 <DECIMAL NUMERIC PROGRAM DATA>, flexible Numeric Representation for more information.

The "`STATus:OPERation:ENABle?`" query returns the enable mask of the Operation Event Register. The Model 1391 returns the value sent previously with the command above using the <NR1> format.

`STATus:OPERation[:EVENt?]`

Returns the contents of the Operation Event Register. The Model 1391 supports this query, but will only return the value "0", indicating operational condition.

`STATus:PRESet`

Sets the enable registers to all 1's. The Model 1391 accepts the command without performing any action.

`STATus:OPERation:CONDition?`

Returns the contents of the Operation Condition Register. The Model 1391 supports this query, but will only return the value "0", indicating operational condition.

`STATus:OPERation:ENABle <NRf>`

Sets the enable mask of the Operation Event Register, which allows true conditions to be reported in the summary bit. The Model 1391 supports the command by saving the mask value and by not generating an error, although the Status registers do not exist.

The <NRf> notation indicates that SCPI's <numeric_value> format is not used in this case. Refer to the IEE488.2 <DECIMAL NUMERIC PROGRAM DATA>, flexible Numeric Representation for more information.

The "`STATus:OPERation:ENABle?`" query returns the enable mask of the Operation Event Register. The Model 1391 returns the value sent previously with the command above using the <NR1> format.

`STATus:OPERation[:EVENt?]`

Returns the contents of the Operation Event Register. The Model 1391 supports this query, but will only return the value "0", indicating operational condition.

Table 3-3. Error Messages

Error Number	Message	Error Number	Message
0	"No error"	-222	"Data out of range"
-100	"Command error"	-223	"Too much data"
-101	"Invalid character"	-224	"Illegal parameter value"
-102	"Syntax error"	-230	"Data corrupt or stale"
-103	"Invalid separator"	-231	"Data questionable"
-104	"Data type error"	-240	"Hardware error"
-105	"GET not allowed"	-241	"Hardware missing"
-108	"Parameter not allowed"	-250	"Mass storage error"
-110	"Command header error"	-251	"Missing mass storage"
-111	"Header separator error"	-252	"Missing media"
-112	"Program mnemonic too long"	-253	"Corrupt media"
-113	"Undefined header"	-254	"Media full"
-114	"Header suffix out of range"	-255	"Directory full"
-120	"Numeric data error"	-257	"file name error"
-121	"Invalid character in number"	-258	"Media protected"
-123	"Exponent too large"	-260	"Expression error"
-124	"Too many digits"	-261	"Math error in expression"
-128	"Numeric data not allowed"	-270	"Macro error"
-130	"Suffix error"	-271	"Macro syntax error"
-131	"Invalid suffix"	-272	"Macro execution error"
-134	"Suffix too long"	-273	"Illegal macro label"
-140	"Character data error"	-274	"Macro parameter error"
-144	"Character data too long"	-275	"Macro definition too long"
-148	"Character data not allowed"	-276	"Macro recursion error"
-150	"String data error"	-277	"Macro redefinition not allowed"
-151	"Invalid string data"	-278	"Macro header not found"
-158	"String data not allowed"	-280	"Program error"
-160	"Block data error"	-281	"Cannot create program"
-161	"Invalid block data"	-282	"Illegal program name"
-168	"Block data not allowed"	-283	"Illegal variable name"
-170	"Expression error"	-284	"Program currently running"
-171	"Invalid expression"	-285	"Program syntax error"
-178	"Expression data not allowed"	-286	"Program run time error"
-180	"Macro error"	-300	"Device specific error"
-181	"Invalid outside macro definition"	-310	"System error"
-183	"Invalid inside macro definition"	-311	"Memory error"
-184	"Macro parameter error"	-312	"PUD Memory lost"
-200	"Execution error"	-314	"Save/recall memory lost"
-201	"Invalid while in local"	-315	"Configuration memory lost"
-202	"Settings lost due to rtl"	-330	"Self test failed"
-210	"Trigger error"		

3.3.4 IEEE-488.2 Common Commands

The *CAL? self calibrate query, the *TST? self test query, and the *TRG command are discussed elsewhere in this manual (along with their equivalent SCPI query or command).

The *CAL? query is equivalent to the SCPI CALibrate[:ALL]? query. The self calibration query is discussed in Appendix C of this operator's manual.

The *TST? query is discussed in Appendix D of this operator's manual.

The *TRG is an IEEE Common Command used to provide a properly sequenced trigger and execute to an addressed 488.2 device. It triggers the Model 1391 via the VXI data bus ('BUS' must be selected as the trigger source in the Trigger subsystem).

The previous paragraphs describe in detail the three most commonly used IEEE Common Commands. Table 3-4 briefly describes the messages mandated by the 488.2 standards, plus optional commands supported by the model 1391.

3.4 Model 1391 Operation

The following paragraphs describe the SCPI language commands for various modes of operation for the Model 1391.

Before beginning, review the data in paragraphs 3.4.1, 3.4.2, and 3.4.3.

3.4.1 Output Terminations

Each output connector must be properly terminated during its use to minimize signal reflection or power loss due to an impedance mismatch. High quality 50Ω coax cable and terminations should be used for pulse waveform fidelity. Terminators should be placed at the end of the coax cable at the point of signal delivery. Figure 3-2 shows proper 50Ω termination for the PULSE OUT connector, with R_S representing the Model 1391 source impedance, R_L representing the termination or load resistance, and R_{IN} representing the receiving instrument input impedance. Table 3-5 lists all the input and output impedances of the Model 1391.

Table 3-5 Input and Output Impedances

Connector	Impedance
PULSE OUT	50Ω
SYNC OUT	50Ω, TTL (0 to >2.0 V terminated)
TRIG IN	≥1 kΩ, ≤10 pF
PAM IN	≥1 kΩ

Table 3-4 IEEE 488.2 Common Commands

Command	Function	Description
*CAL?	Calibration Query	Starts self-cal, places pass/fail response in output queue
*CLS	Clear Status Command	Clears Status Data Registers, forces OCIS/OQIS
*ESE	Standard Event Status Enable	Sets Event Status Enable Register bits
*ESE?	Standard Event Status Enable Query	Returns contents of Event Status Enable Register
*ESR?	Standard Event Status Register Query	Returns contents of Event Status Register
*IDN?	Identification Query	Identifies devices over the system interface
*OPC	Operation Complete Command	Requires oper. comp. message in Event Status Reg.
*OPC?	Operation Complete Query	ASCII '1' in dev. out. queue when operations complete
*RST	Reset Command	Resets the device
*SRE	Service Request Enable Command	Sets Service Request Enable Register bits
*SRE?	Service Request Enable Query	Returns contents of Service Request Enable Register
*STB?	Read Status Byte Query	Returns status and master summary status bytes
*TRG	Trigger Command	Initiates a properly sequenced trigger and execute
*TST?	Self Test Query	Starts self-test, places pass/fail response in output queue
*WAI	Wait - to - Continue Command	Blocks device commands until 'No-Op-Pend' flag is true

3.4.2 Input/Output Protection

The Model 1391 provides protection for internal circuitry connected to input and output connectors. Refer to the Specifications in Section 1 of this manual to determine the level of protection associated with each input or output connector.

3.4.3 Power On/Reset Defaults

At power on, or as the result of sending `*RST` or `RESet`, the Model 1391 defaults to the following conditions:

Subsystem	SOURce
Operational Mode	CONTinuous
Function Shape	PULSe
Frequency value	1 MHz
Upper Level value	+0.5 V into 50Ω
Lower Level value	–0.5 V into 50Ω
Amplitude value	1 Vpp
Offset value	0 Vdc
Pulse Output	OFF
Pulse Period value	1 µs
Pulse Width value	250 ns
Pulse Delay value	0 ns
Double Pulse state	OFF
Double Pulse Delay	400 ns
Pulse Transition state	OFF (5 ns)
Leading Transition	5 ns
Trailing Transition	5 ns
Auto-Trailing state	OFF
Pulse Polarity value	NORMal
Sync Marker Output	OFF
Sync Marker Type	CLOCk
PAM Input	Disabled (Off)
PAM Mode	BIPolar
Sumbus	Off (not input or output)
Sumbus Mode	DRIVe
Trigger Mode	SLAVe
TTL Trigger Lines	Off (not input or output)
ECL Trigger Lines	Off (not input or output)
Trigger Slope	Positive
Trigger Level value	+1.0 V
Trigger Source	Internal
Trigger Timer	10 ms (100 Hz)
Trigger Count	1
Gate State	OFF
Gate Sub-Mode	SYNChronous

3.4.4 Continuous Operation

This paragraph shows how to set up the Model 1391 for a pulse waveform output using the default settings provided at power-on. The subsequent paragraphs under this heading will then demonstrate the continuous mode pulse period, pulse waveforms and characteristics, and the output levels. All of the parameters shown here are detailed in earlier paragraphs. Much of the information given here directly transfers to other modes.

Connect the Model 1391's PULSE OUT connector (terminated) to the device under test, as shown in figure 3-3. Use the SYNC OUT signal as a synchronizing source. Figure 3-4 illustrates the SYNC OUT and PULSE OUT relationships.

At power on, the Model 1391's PULSE OUT is always turned OFF. To enable the PULSE OUT connector, send the command:

```
OUTP:STAT ON
```

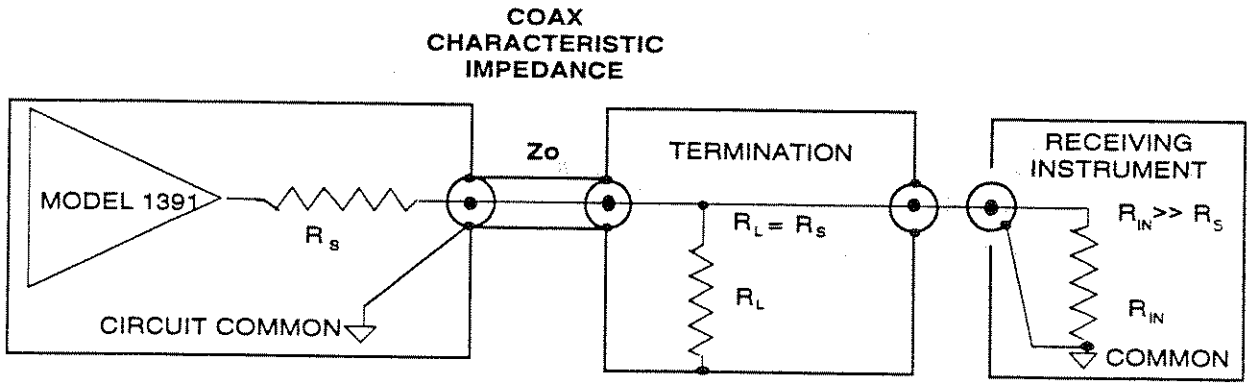


Figure 3-2. Output Termination

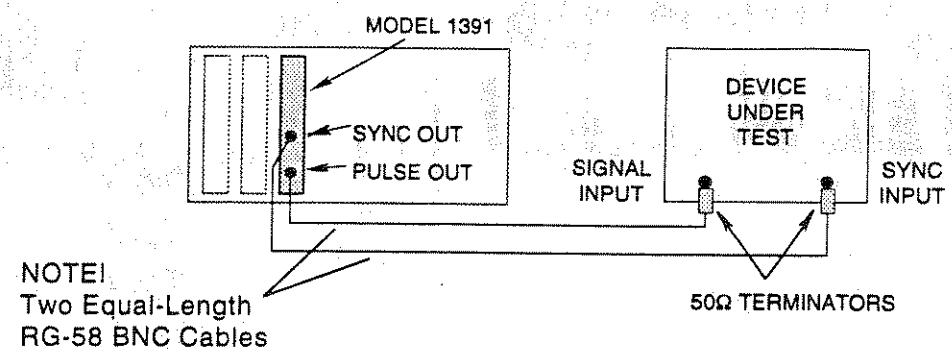


Figure 3-3. Model 1391 Basic Operation Setup

At power on, the Model 1391's SYNC OUT is always turned OFF. To enable the SYNC OUT connector, send the command:

```
SOUR:MARK:STAT ON
```

The two previous commands could be shortened and combined as follows:

```
OUTP ON;:MARK ON
```

Set up a 2 channel, high bandwidth oscilloscope as the DUT in Figure 3-3. Connect the SYNC to CH 1 and the PULSE to CH 2. Trigger the scope internally from CH 1. Compare the pulse waveform to Figure 3-4 below. The default pulse waveform should be a Single Pulse with its 0% point coincident with the 50% point of the rising edge of the SYNC, as shown in the diagram. The pulse period is 1 µs and the Leading Transition (t_r) and Trailing Transition (t_f) should both be no more than 5 ns. Verify 250 ns Pulse Width.

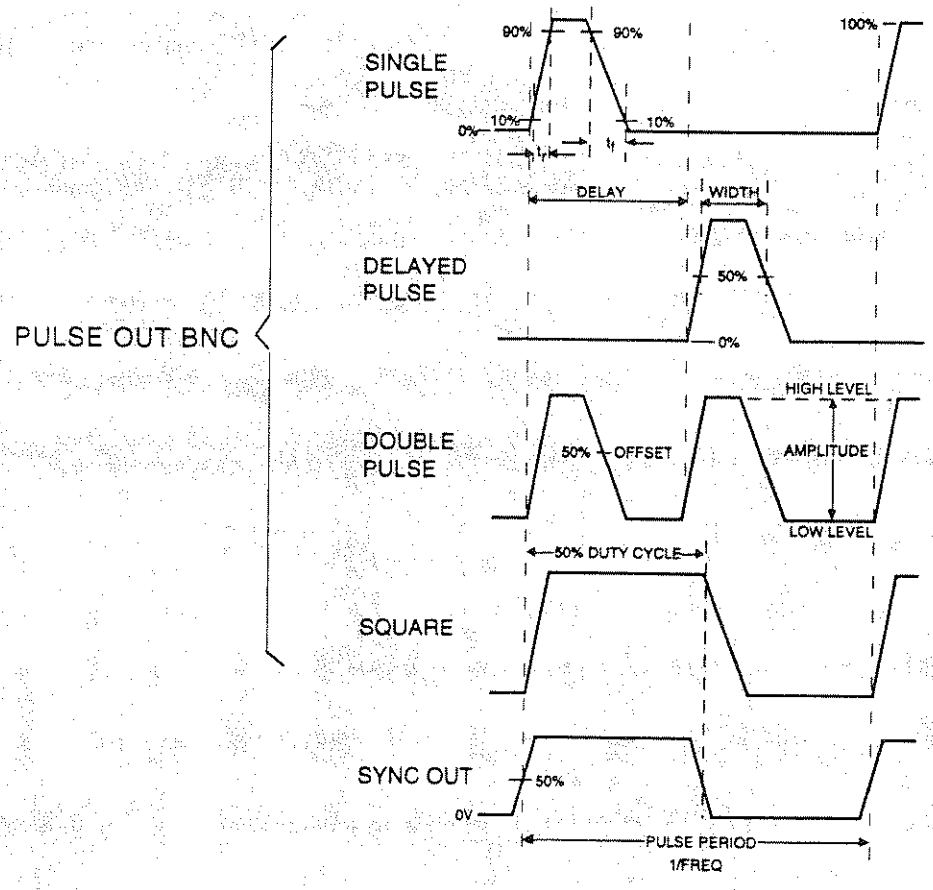


Figure 3-4. Continuous Waveform Characteristics

3.4.4.1 Frequency/Period Parameters

The FREQuency and PERiod parameters are "coupled", meaning that setting one updates the other appropriately. The current default settings from the previous setup are 1 µs period and 1 MHz frequency. Change the period from 1 µs to 5 µs by sending:

```
PULS:PER 5E-6
```

Verify the frequency value has been updated by sending the query:

```
FREQ?
```

The returned response should be `'FREQ 2E5'` (200 kHz). The display on the oscilloscope should now have a pulse period of 5 µs, with the other pulse parameters remaining the same.

3.4.4.2 Pulse Parameters

Programmable pulse parameters included in this paragraph are the WIDTh, LEADing TRANsition, TRAiling TRANsition, DELAY, and DOUBle DELay. Paragraphs 3.4.4 and 3.4.4.1 above have the Model 1391 set up in its default values except that the PULSE and SYNC outputs are ON and the period has been changed to 5 µs. There should be a 250 ns single pulse with 5 ns transitions on the oscilloscope. Change the single pulse width and transition times as follows:

```
PULS:TRAN:STAT ON
PULS:TRAN:TRA:AUTO ON
PULS:TRAN 200E-9
PULS:WIDT 1E-6
```

The first command enables the transition times for programming to values other than the default minimum of 5 ns. The second command causes the trailing transition to be programmed along with the leading transition. The next command sets the leading (and thus both) transition to 200 ns, and the final command changes the single pulse width to 1 µs. The oscilloscope display should now show a 1 µs wide single pulse with 200 ns transitions. Decouple the trailing transition from the leading transition as follows:

```
PULS:TRAN:TRA:AUTO OFF
PULS:TRAN:TRA 600E-9
```

The trailing transition should increase to 600 ns. Change from a single to a delayed pulse as follows:

```
PULS:DEL 3E-6
```

The pulse should now start 3 µs after the SYNC rather than coincident with the SYNC. Set up a double pulse as follows:

```
PULS:DOUB:DEL 2E-6
PULS:DOUB ON
```

The double pulse should appear much like the one in Figure 3-4. Note that the delay values for the delayed pulse and the double pulse are two independent parameters.

3.4.4.3 Output Levels

Leave the unit set up per the previous paragraph. Note that the default settings for output amplitudes of the pulse waveform result in levels of ±0.5 V into a 50Ω termination.

The output levels can be set up using the AMPLitude and OFFSet parameters, or by using the HIGH and LOW level parameters. Use HIGH and LOW together, or use AMPLitude and OFFSet together. These are "coupled" functions – setting up one pair causes the other pair to update to equivalent values.

Setting up the output is not as simple as many of the other parameters. Because the output amplifier is only capable of generating an output within a fixed "window" without limiting, there are interactions between the settings. This window is ±8V with the attenuator off and ±2V with the attenuator on.

When using the AMPLitude and OFFSet parameters, the sum of Vpk amplitude (half the programmed Vpp value) and the absolute value of the offset parameter cannot exceed 8V. Additionally, for pulses less than 0.5 Vpp, this restriction is reduced to 2 V.

When setting the output in terms of HIGH and LOW levels, the HIGH level must be at least 0.15 V more positive than the LOW level. HIGH and LOW levels are programmed within a ±8 V window, reduced to a ±2 V window when (upper – lower) is less than 0.5 V.

Set up the pulse waveform for negative supply ECL levels using AMPLitude and OFFSet parameters as follows:

```
VOLT 8E-1
VOLT:OFFS -1.3
```

Observe normal ECL levels on the oscilloscope waveform. The upper level should be –0.9V and the lower level should be –1.7V.

Set up the pulse waveform for CMOS levels using HIGH and LOW LEVel parameters as follows:

```
VOLT:HIGH 5
VOLT:LOW 0
```

The waveform should change to CMOS levels.

Note that the pulse waveform is "false" at the lower level and pulses "true" to the upper level. This is NORMal PULSe POLarity. Reverse the levels by programming the following:

```
PULS:POL COMP (or INV)
```

Note the change in the waveform from positive to negative logic. This feature can be used to increase duty cycle to >95% by programming the complement of the desired waveform.

3.4.4.4 Pulse/Square Functions

Paragraph 3.4.4.2 demonstrates how to set up single, delayed and double pulses. These three waveforms are available under the default setting:

```
[SOUR:]FUNC[:SHAP] PULS
```

The Model 1391's default settings are designed to provide a "generic" starting point for common operations. Reset the unit (`RESet` or `*RST`) and then turn the PULSE and SYNC outputs back on (see paragraph 3.4.4). This is the single pulse. Observe a delayed pulse by sending:

```
PULS:DEL 100E-9
```

Observe a double pulse by sending:

```
PULS:DOUB ON
```

And finally, observe the SQUare function by sending:

```
FUNC SQU
```

The square has the same timing characteristics as a CLOCk SYNC, and its transitions and levels are settable like the PULSe waveforms. Additionally, the square's upper frequency is extended to 100 MHz.

3.4.5 Marker Operation

The pulse waveform Marker is the SYNC OUT waveform. The SYNC waveform can be set up as a pulse *period* marker, or as a non-continuous mode timing marker. The continuous mode default setting is as a period marker. This can be programmed as follows:

```
MARK:TYPE CLOC
```

For the non-continuous modes, GATE and BURSt, the marker type can be changed as follows:

```
MARK:TYPE GATE
```

The GATE SYNC will be described in paragraphs 3.4.9 and 3.4.10 and in the related figures.

3.4.6 SUMBUS Operation

SUMBUS operation requires the use of at least two Model 1391s or one 1391 and a VXIbus module supporting the SUMBUS. This discussion assumes two Model 1391s. The modules may be located anywhere in the VXIbus chassis (except slot 0).

Note that the scale factors (see Section 1) for outputting to the SUMBUS (5 mA/V) and inputting from the SUMBUS (0.2 V/mA) are reciprocals. This means that there is an end-to-end scale factor of 1 Vin/Vout for two Model 1391s.

NOTE

This simple 1 Vin/Vout scale factor applies to unattenuated amplitudes. Use 1 V/V if both the driving and the receiving units are unattenuated (both have their amplitudes ≥0.5 Vpp). This 1 V/V factor is also valid if both have their amplitudes set <0.5 Vpp. If the unit driving the SUMBUS is below and the receiving unit is above 0.5 Vpp, use a 0.25 Vin/Vout scale factor. If the unit driving the SUMBUS is above and the receiving unit is below 0.5 Vpp, use a 4 Vin/Vout scale factor.

Designate one of the units as the Driver. Its amplitude setting is Vin. Designate the other as the Receiver. Its amplitude setting is Vout. The Receiver unit will have its PULSE OUT and SYNC OUT connected to the oscilloscope as in Figure 3-4. First, set up the pulse waveforms of both units to match Figure 3-5, as follows:

Driver:

```
RES
OUTP ON;:MARK ON
PULS:PER 1E-3
PULS:WIDT 500E-6
PULS:DEL 200E-6
```

Receiver:

```
RES
OUTP ON;:MARK ON
PULS:PER 1E-3
PULS:WIDT 200E-6
PULS:DOUB ON
PULS:DOUB:DEL 600E-6
```

Now, set up the Driver as the Master and the Receiver as the Slave (Master/Slave Operation is explained in paragraph 3.4.11), as follows:

Driver:

```
TRIG:MODE MAST
OUTP:ECLT0 ON
```

Receiver:

```
INIT:CONT OFF
TRIG:SOUR:ECLT0
```

This slaves the Receiver's period to the Driver's. Finally, enable the SUMBUS, as follows:

Driver:

```
SUMB:MODE DRIV;SUMB ON
```

Receiver:

```
SUMB:MODE REC;SUMB ON
```

The oscilloscope waveform should look like the "RECEIVER W/SUMBUS" waveform in the figure. Note that the Driver and Receiver waveforms were at their default amplitudes of 1 Vpp. The summed waveform should be 2 Vpp because of the 1 V/V scale factor.

3.4.7 PAM Operation

PAM operation requires a Model 1391 and an external signal source to drive the PAM IN connector. Setting the Pulse Modulation (PULM) STATe ON enables signals at the PAM IN input to amplitude modulate the pulse level(s) around the value set by the programmed VOLTage setting. PAM is accomplished with four-quadrant multiplication of the 1391's pulse signal and the external PAM IN signal. Pulse Modulation has three sub-modes of operation. "POSitive AMPLitude" modulation causes the lower level to be fixed at zero volts and the median value upper level to be at its programmed value. The signal at PAM IN will amplitude modulate the instantaneous value of the upper level around this median value. The *envelope* of the modulated upper level will have the same shape as the external signal, limited by the >20 kHz bandwidth of the PAM input. The scale factor between the amplitude of the external signal and the amplitude of the modulation envelope is 2V of change in the output level per 1V of change in the external signal. This scale factor is reduced to 0.5 V of change in the output per 1V of change in the external signal when the programmed amplitude is set below 0.5 Vpp.

"NEGative AMPLitude" PAM is the mirror image of the POSitive case. The upper level is fixed at zero volts and the lower level is amplitude modulated. Note that the modulation envelope is also the mirror image of the external signal.

"BIPolar AMPLitude" modulation is essentially the sum of the POSitive and NEGative sub-modes.

The programmer/operator needs to be aware of two things when setting up PULseModulation. First, the output swing is limited to a window of ±8V (±2V for Vpp amplitudes less than 0.5 Vpp). Since the 1391's firmware has no knowledge of the external signal's amplitude and offset, the unit cannot issue an output stage clipping warning as it does with an AMPLitude/OFFSet setting conflict. Second, the multiplier can be overdriven resulting in overmodulation (including a polarity reversal of the pulses because of four-quadrant

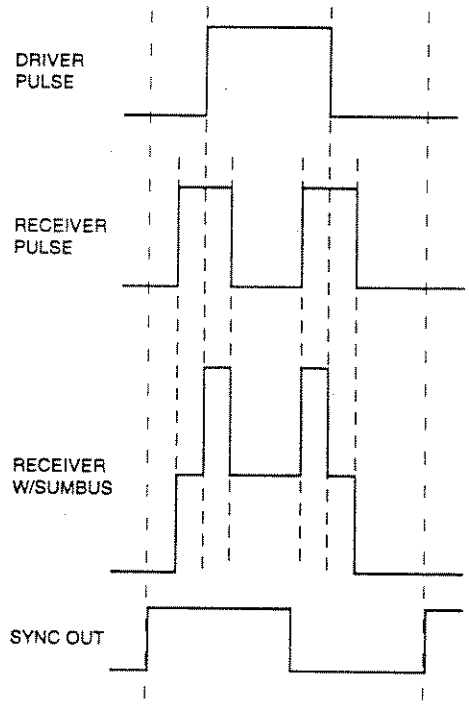


Figure 3-5 SUMBUS Waveforms

operation). To avoid these problems, the desired PAM waveform should be designed using the following steps:

1) Sketch the desired PAM output waveform. From the sketch, select the required pulse characteristics (paragraph 3.4.4), PULM sub-mode, and the median pulse output level(s). Ensure that the required waveform can be produced within the 1391's output window capability.

2) Program the Model 1391 for pulse period, function, transitions, width and delay for the required pulse characteristics as discussed in the previous paragraphs. Turn on the pulse output.

3) Based on the PULM sub-mode selected from the sketch, set up the pulse upper and lower levels to the desired median level(s). Note that for POSitive or NEGative sub-modes, the programmed value of the level which is to be set to zero by the sub-mode is not important.

4) Enable the PAM IN and select a sub-mode, for example:

```
PULM ON
PULM:AMPL POS
```

Verify the PULSE OUT waveform to ensure it matches the sketch.

5) Set up the external signal waveshape and amplitude. From the Vpp amplitude of the envelope in the sketch and the known scale factor, set the external signal's Vpp amplitude. Connect the external signal to the PAM IN connector. The ≥1 kΩ input impedance should not reduce the signal amplitude unless its source impedance is very high.

6) Compare the result to the sketch and fine adjust the external signal as necessary. In general, the oscilloscope should be synchronized to the lowest frequency component in the waveform, the external signal.

3.4.8 Triggered Operation

In the triggered mode, the Model 1391's output remains quiescent until triggered by the trigger source. All Model 1391 functions may be triggered. When triggered, the Model 1391 produces one complete waveform period, then returns to the quiescent state. The quiescent state for POSitive POLarity is the lower level. The quiescent state for NEGative POLarity is the upper level. The unit may be triggered by using

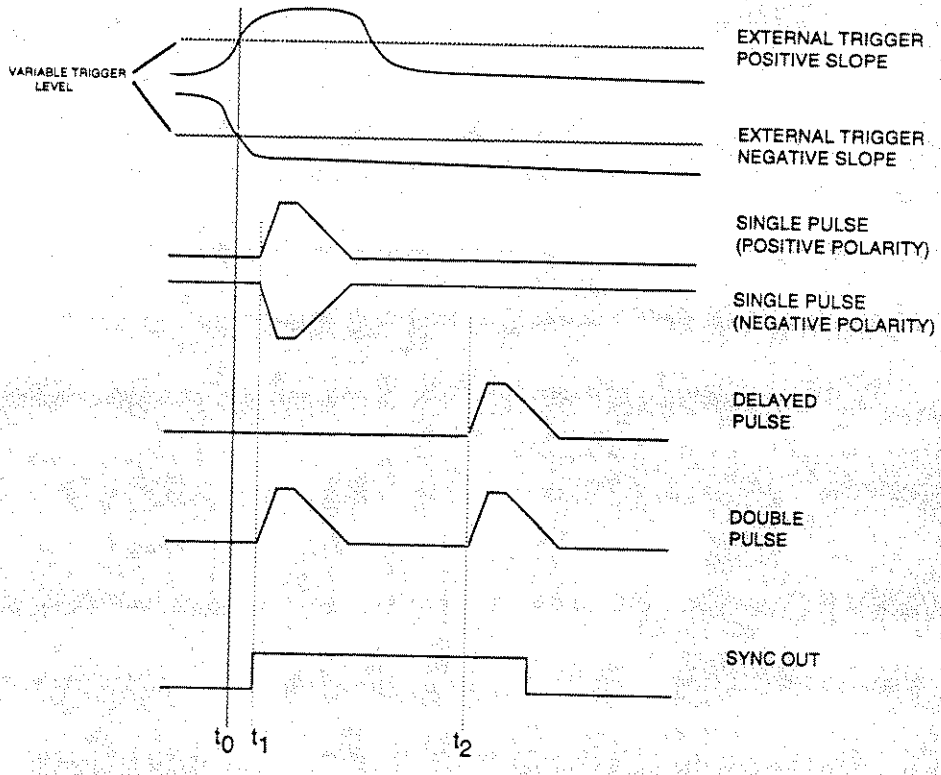


Figure 3-6. Triggered Waveform Characteristics

the internal trigger TIMer, the external TRIG IN, the trigger command, or the VXI trigger bus input.

To set the Model 1391 for the triggered mode, follow the instructions in paragraph 3.4.4, then change the mode to triggered by sending:

```
INIT:CONT OFF
```

The default settings select triggered modes rather than one of the other non-continuous modes. These default settings are:

```
TRIG:GATE OFF
TRIG:COUN 1
```

In order to properly trigger the 1391, the TRIGger SOURce, MODE, TIMer, SLOPe and LEVel may also need to be set up.

3.4.8.1 Level and Slope Parameters

The TRIger LEVel and SLOPe parameters are used to tailor the response of the trigger input comparator to external triggering signals applied to the TRIG IN connector. This is only applicable when the triggering SOURce is selected as EXTernal. The LEVel should be set to a voltage level which corresponds to a point on the external signal where the dV/dt value of the signal's transitions is maximum. This minimizes triggering uncertainty (jitter). The SLOPe selection determines whether the 1391 is triggered on a positive-going or a negative-going transition through the selected voltage level. See Figure 3-6.

3.4.8.2 External Trigger Input

First set up the desired pulse characteristics per paragraph 3.4.4. Each trigger input will initiate one pulse period with these selected characteristics. Then determine the level and slope requirements (see the previous paragraph) for the external signal to be applied to the TRIG IN connector, and program the unit for triggered mode, external source. For example, for an external TTL triggering input:

```
RES
(PULSE CHARACTERISTICS)
TRIG:SLOP POS;LEV 1;SOUR EXT
INIT:CONT OFF
```

The result will be one period of the selected pulse waveform each time the external TTL signal makes a low-to-high transition. Note that the period of the external signal must be greater than the pulse period. Figure 3-7 illustrates triggering of each of the pulse functions. The SQUare may also be triggered, with timing coincident with the SYNC.

The pulse waveform could be complemented by sending the command:

```
PULS:POL COMP
```

Referring to Figure 3-6, the time t_0 is shown to be the point where the selected external signal transition, positive-going or negative-going, crosses the programmed trigger level voltage. The time t_1 is the 50% point of the rising edge of the SYNC OUT (MARKer:TYPE CLOCk). The time t_2 is the 0% point on the leading edge of a delayed pulse. The time $(t_1 - t_0)$ is a fixed circuit delay between the triggering event and the start of a waveform period. Both the sync output (50% point) and the non-delayed pulse (0% point) occur at t_1, regardless of the operating mode. The time $(t_2 - t_1)$ is the programmable DELay parameter.

3.4.8.3 Internal Trigger

The trigger slope and level parameters have no effect on an internal trigger source. To trigger the generator internally, set up the internal trigger TIMer to a value greater than the pulse period. Using the previous example as a starting point, select the internal triggering source and program the TIMer as follows:

```
TRIG:SOUR INT;TIM <value>
```

Where <value> is the desired triggering period. Triggered periods operate to 25 MHz in double pulse, 50 MHz in single or delayed pulse, and 100 MHz in square.

3.4.8.4 BUS Trigger Commands

To trigger the generator using the IEEE 488 bus (external host) or the VXIbus, set up the generator in a triggered mode as described in above, then select the bus trigger command by sending:

```
TRIG:SOUR BUS
```

Trigger the generator by sending either the 488.2 `*TRG` or 488.1 `GET` command over the 488 bus, or the word serial `Trigger` over the VXIbus. The `*TRG` command is mandated to be recognized by the Commander and by the Model 1391. The `GET` command causes the Commander to send the VXIbus word Serial `Trigger` command to addressed devices which support `Trigger` and do not have their DIR bit cleared to 0 (seee VXIbus System Specification). Trigger level or slope do not apply when using the `BUS` as the trigger source, and the bus commands only have effect when the Model 1391 is in a triggered mode of operation and the selected trigger source is `BUS`.

3.4.8.5 VXI TTL/ECL Trigger Bus Input

The Model 1391 may also be triggered from the VXIbus TTL or ECL trigger lines on the backplane. The signal must be placed on the bus from another source within the VXI chassis.

To use the trigger bus as a trigger source, first set up the Model 1391 per the previous examples. Next, select one of the eight TTL trigger lines by sending the message:

```
TRIG:SOUR TTLT<n>
```

Where <n> represents one of the eight TTL Trigger lines, 0 through 7. Alternatively, select one of the two ECL trigger lines by sending the message:

```
TRIG:SOUR ECLT<n>
```

Where <n> represents one of the two ECL Trigger lines, 0 or 1. The ECL trigger lines will have higher bandwidth and tighter timing coupling between modules. Note that a TTL trigger line has a maximum bandwidth of 12.5 MHz per the VXIbus specification.

The selected signal will trigger the Model 1391 on the leading edge. Trigger level or slope does not apply when using one of the TTL Trigger lines as the trigger source.

The Model 1391 also offers a special operation mode optimized for triggering a 1391 from a 1391 using the ECL trigger lines (see paragraph 3.4.11).

3.4.8 Gated Operation

The synchronous gated mode is identical to the triggered mode, except the output from the Model 1391 starts from the quiescent state, produces continuous pulse periods for the duration of the trigger signal, then returns to the quiescent state. All waveforms may be gated (see figure 3-7).

To view synchronous gated mode, set up the Model 1391 pulse characteristics per the previous examples, and set the unit up for trigger mode using an EXTernal SOURce at the TRIG IN input. To observe gate mode properly, set the oscilloscope to both display and sync to the external triggering signal on CH1, and to display the 1391 PULSE OUT on CH2. Then switch from triggered to gated mode:

```
TRIG:GATE ON
```

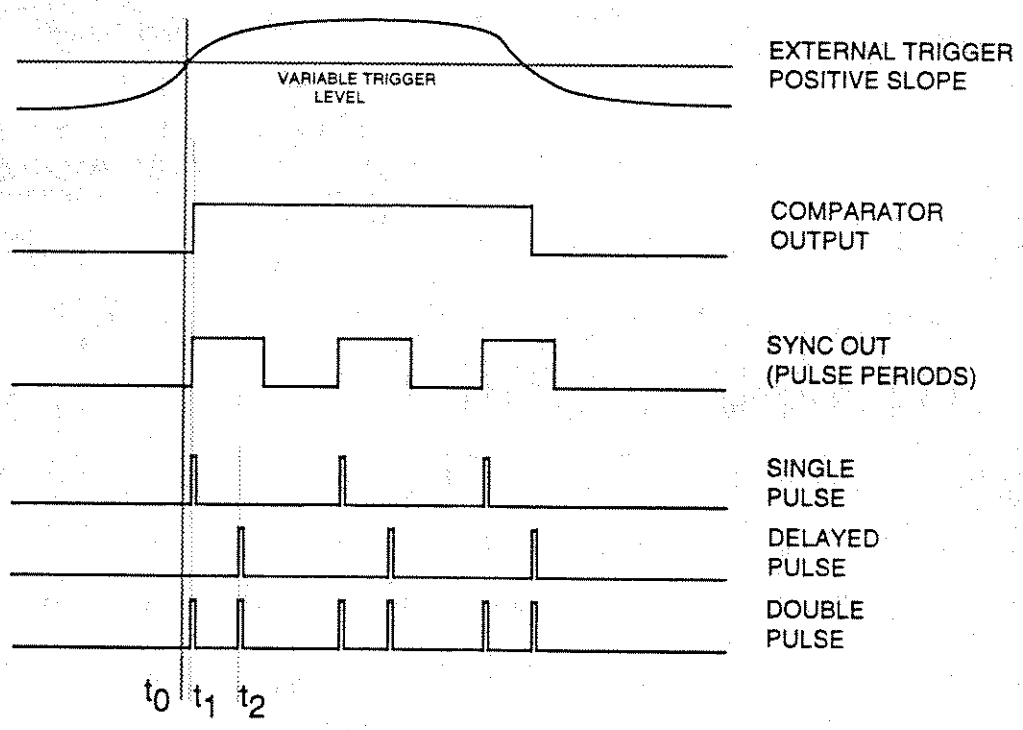


Figure 3-7. Synchronous Gate Waveform Characteristics

The default setting is "synchronous" rather than "external width" gate mode, which can be programmed with the command:

```
TRIG:GATE:MODE SYNC
```

The SYNC OUT should appear as in Figure 3-7. Change the Sync waveform to be similar to the "COMPARATOR OUTPUT" waveform in the figure by sending:

```
MARK:TYPE GATE
```

Gate mode may also use various trigger sources. The unit may be triggered by the external TRIG IN as described above, the internal source as described in paragraph 3.4.8.3, or the VXI trigger bus input as described in paragraph 3.4.8.5. The BUS trigger commands as defined in paragraph 3.4.8.4 do not provide a trigger duration and are not valid in gated mode.

3.4.9.1 External Width Operation

In external width, the Model 1391 produces an output pulse whose period and width are determined by the selected triggering signal and the trigger level and slope settings, as shown in figure 3-8. To select external width, set up the 1391 in gated mode as described above and then send the command:

```
TRIG:GATE:MODE EXTW
```

Frequency or period commands are not required for external width. All other pulse characteristics are as described in paragraph 3.4.4. The external width accepts trigger inputs from all four trigger sources: external TRIG IN, internal trigger generator, VXI Trigger Bus, and the Trigger command. However, the most useful trigger source for external width is the external TRIG IN connector. This is because an externally defined signal is used and the trigger level and slope are adjustable as described in paragraph 3.4.8.1. To select the TRIG IN connector as the trigger source, send the command:

```
TRIG:SOUR EXT
```

To select the internal signal source (the frequency synthesizer) for the External Width function, send the following:

```
TRIG:TIM <value>:SOUR INT
```

The internal TIMer value is defined in paragraph 3.4.8.3. It is not recommended that this setup be used, since the identical result may be obtained by simply using a continuous square function.

A third trigger source for external width is the VXI backplane, described in paragraph 3.4.8.4. The period and width of the instrument output is dependent on the characteristics of the selected signal. A backplane signal is selected by programming one of the eight TTL trigger lines by sending the message:

```
TRIG:SOUR TTLT<n>
```

Where <n> represents one of the eight TTL Trigger lines, 0 through 7. Alternatively, select one of the two ECL trigger lines by sending the message:

```
TRIG:SOUR ECLT<n>
```

Where <n> represents one of the two ECL Trigger lines, 0 or 1. The ECL trigger lines will have higher bandwidth and tighter timing coupling between modules. Note that a TTL trigger line has a maximum bandwidth of 12.5 MHz per the VXIbus specification.

The remaining trigger source available to the Model 1391 in external width is the trigger command '*TRG',

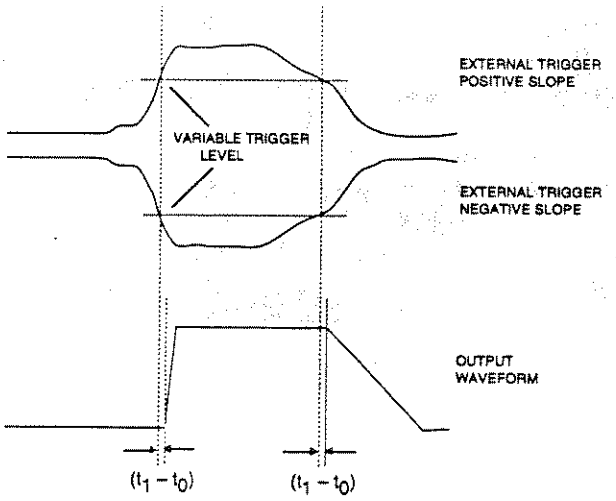


Figure 3-8. External Width Waveform Characteristics

described in paragraph 3.4.8.3. When using the trigger command, the period and width of the output signal is determined by the *TRG bit. To select the trigger command, send:

```
TRIG:SOUR BUS
```

A pulse will be generated, whose width will be a function of the commander's *TRG write cycle time.

3.4.10 Burst Operation

The burst mode is identical to the triggered mode, except when a trigger is received, the Model 1391 leaves its quiescent state, produces a predefined number of pulse periods, then returns to its quiescent state. Burst waveforms (with COUNt set to "3") will be identical to the gate waveforms illustrated in Figure 3-7.

To observe the burst mode, set up the Model 1391 for triggered mode as described in paragraph 3.4.8, then send the burst mode command:

```
TRIG:COUN <n>
```

Where the value <n> is a number greater than 1 and up to 1 million. Numeric values are explained in paragraph 3.3.1.4. For burst count messages, numeric values may be in the form of an integer or floating point value, or one of the special case character keywords, 'MAXimum', 'MINimum', or 'DEFault'. Burst duration depends on the period or frequency programmed.

Both types of Sync waveform (see Gate Mode) are valid and programmable in Burst Mode.

A burst is initiated when the unit is triggered by the selected trigger source. The trigger source may be the external TRIG IN, as described in paragraph 3.4.8.2, the internal trigger source as defined in paragraph 3.4.8.3, the BUS trigger command as described in paragraph 3.4.8.4, or the VXI trigger bus input as described in paragraph 3.4.8.5.

3.4.11 Master/Slave Operation

Master/Slave triggering allows a VXIbus chassis with more than one Model 1391 module installed to operate as a multichannel pulse generator system. An ECL Trigger line is used to distribute the Master's trigger signal to the Slaves to ensure tight coupling. Additionally, signal timing is optimized to closely match the t_1 points (start of a pulse period, see Figure 3-7 and paragraph 3.4.8.2) of the Master module to an adjacent Slave module. Slave modules further away from the Master will have a backplane delay of approximately 0.5 ns per slot. Therefore, for best timing performance, the 1391 modules in the Master/Slave group should be adjacent to one another and the Master should be the one in the middle of the group.

The default setting for a 1391 module is "Slave", which allows it to be a Slave module in a Master/Slave group or an independent module. Once the Master module is chosen, send it the command:

```
TRIG:MODE MAST
```

There can only be one Master connected to a group of Slaves using one particular ECL Trigger line. Program the ECL Trigger line to be used by the group by sending the following command to the Master:

```
OUTP:ECLT<n> ON
```

Set up the Slaves to receive the Master's trigger on this particular ECL Trigger line by sending the following command to *each* Slave:

```
TRIG:SOUR:ECLT<n>
```

The Master is operated in continuous mode or a non-continuous mode with its trigger source set to anything other than the particular ECL Trigger line being used to trigger the Slaves. The Slaves must be set to a non-continuous mode with the trigger source set up as above. Each module, Master or Slave, can have all pulse characteristics (see paragraph 3.4.4) set up independently. The only restriction is that the master repetition period determined by the signal placed on the ECL Trigger line by the Master (essentially the signal that drives its SYNC OUT) is the longest period produced by any module. Each time a Slave is triggered by the Master, it must complete its output sequence, taking into consideration its period and COUNt value, and return to a quiescent state before the next Master trigger.

3.4.12 Status Commands

This subsystem contains the Status reporting registers. Neither the Operation, nor the Questionable registers are implemented in the Model 1391. All queries will return a "0" (zero). The Enable subcommands for each register will be accepted, but will not perform any function. Preset may be exercised, but will perform no function.

4.1 INTRODUCTION

Figure 4-1 shows the Wavetek Model 1391 VXIbus Pulse Generator overall block diagram. The VXIbus connects to the module at backplane connectors P1 and P2, which supply the module with a digital interface, power supplies, trigger lines and a master clock. The module contains three printed circuit boards: the VXI Interface Board, pulse generator Main Board, and the pulse generator Amplifier Board. The VXI Interface Board contains the VXIbus P1 and P2 connectors and provides an interface between the VXIbus and the Main Board. The Main Board receives control signals and data from the interface and generates pulse waveforms. The Amplifier Board plugs into the Main Board and provides the high voltage, 50Ω source impedance pulse output signal to the PULSE OUT connector.

Under the direction of its VXIbus Commander (and more directly, the VXI Interface Board), the Wavetek Model 1391 Pulse Generator module produces pulse waveforms at the PULSE OUT BNC connector, and a TTL level pulse at the SYNC OUT BNC connector for pulse waveform synchronization. It also receives external triggering inputs at the TRIG IN BNC and external modulating signals at the PAM IN BNC.

The Model 1391 can also drive or receive triggering signals on the TTLTRIG or ECLTRIG lines on the VXIbus chassis backplane. This allows inter-module triggering and Master/Slave operation. In this manner, each 1391 module can be one channel in a multi-channel pulse generator system.

The VXIbus chassis backplane also provides an analog SUMBUS, which is utilized by the Model 1391.

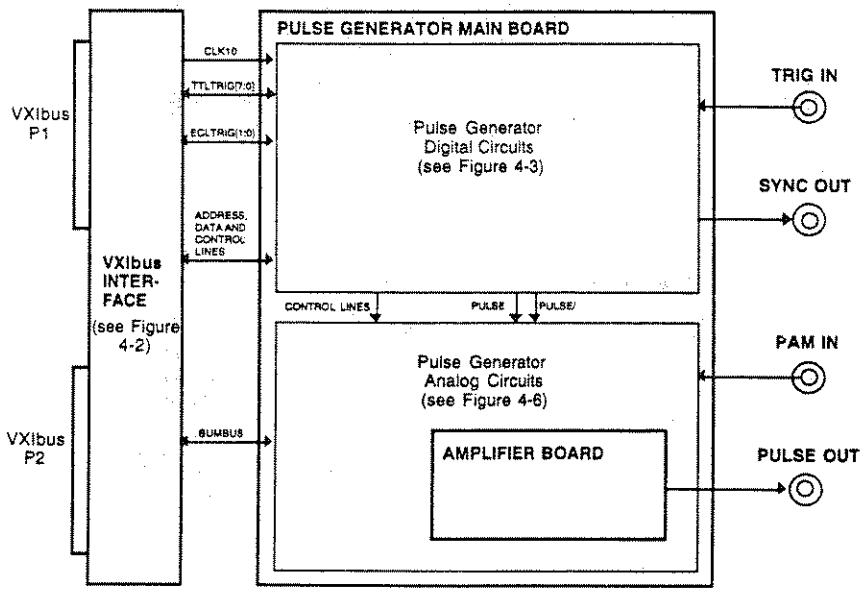


Figure 4-1. Model 1391 Pulse Generator Overall Block Diagram

4.2 VXI INTERFACE BOARD

All operating instructions and data for the Model 1391 module originate from its Commander, located within the VXI chassis. The VXI Interface Board, mounted within the Model 1391 module, transfers signals between the Pulse Generator and the VXIbus. An eight-position rocker switch located on the interface board determines the module's logical address.

Because of its high density, multi-layer printed circuit card utilizing LSI and custom ASIC surface mount parts, the Interface Board is documented in this manual only as necessary to support repair at the factory. Maintenance information is provided to aid in fault isolation to the board level.

4.2.1 VXIbus Overview

A block diagram of the VXI Interface Board is given in Figure 4-2. The VXIbus is contained in the chassis' backplane, and interconnects to the 1391 module P1 and P2 connectors. Refer to the VXIbus System Specifications for electrical specifications of the P1 and P2 connectors, the CLK10 line, the MODID line, the TTLTRG*/ECLTRIG* lines, and the TTLTRG*/ ECLTRIG* protocols if detailed information is needed on the inputs to the VXI Interface Board.

The VXIbus System Specifications will also provide system architecture information that will be of help to understand the various tasks that the interface board performs. For Wavetek's implementation, the following sections should be understood: Device Overview, Message Based Devices, Message Based Device Communication Protocols, VXIbus and IEEE-488.2 Instrument Protocols, Shared Memory (present, but not used in the Model 1391), and Dynamic Configuration. The Wavetek VXIbus chip is an ASIC device which implements these protocols under direction of the interface 68HC000 CPU and system firmware.

4.2.2 Interface Board

The block diagram segments the Interface Board into a VXI INTERFACE block, a CPU & MEMORY block and an INSTRUMENT INTERFACE block. The VXI INTERFACE block contains the P1 and P2 connectors, the VXI ASIC device, the Shared Memory, module addressing, and various drivers and transceivers. The VXI ASIC device implements the complete VXIbus Message Based Device interface. It generates control signals that regulate the transfer of data between the interface CPU and the VXIbus. The VXIbus A16 registers are located within the ASIC. It also controls the RUN, FAIL, MODID, A16 and A24 LEDs on the mod-

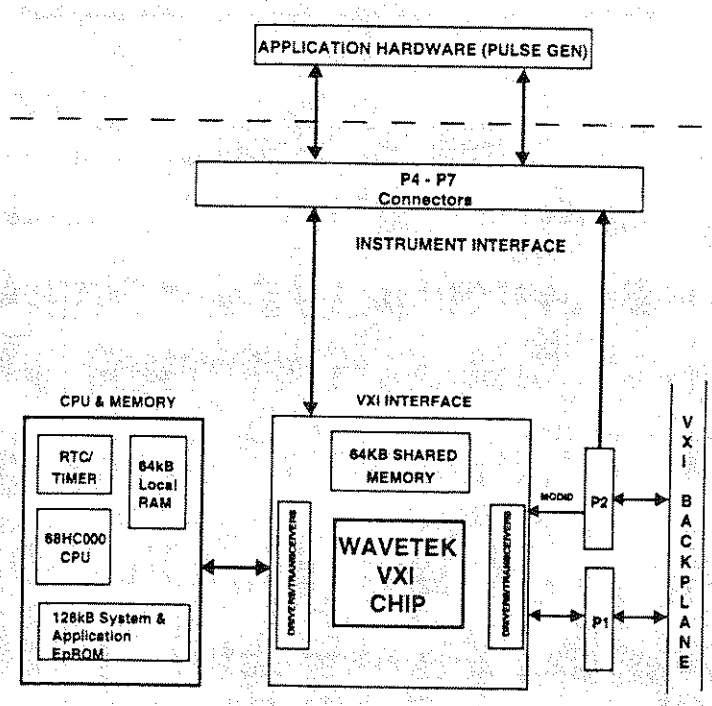


Figure 4-2. VXIbus Interface Board Block Diagram

ule's front panel. The VXI interface contains 32 k x 16 RAM as 64 k bytes of A24/D16 Shared Memory which may be used to efficiently move large quantities of data. The Logical Address Switch and Bus Arbitration jumpers are explained in Section 2 of this manual.

The CPU & MEMORY block contains the microprocessor, local RAM and ROM, decoders, a real time clock/timer, the interrupt controller, a bus error timer and various drivers and transceivers. The local ROM consists of 128k of EPROM containing VXIbus System and Application (the 1391 Pulse Generator) code. There is also 64 k bytes of local static RAM for variable data, stack and heap. The real time clock provides timer and event capability. Up to seven interrupt inputs may be priority encoded; three from the application (not used in the 1391), three from the VXI ASIC, and one from the real time clock. The bus error timer generates a local BERR\ signal if data transfer acknowledgment (local DTACK\) is not given before time-out occurs. BERR\ is generated if a microprocessor access cycle exceeds 16 µs.

The INSTRUMENT INTERFACE block consists of connectors P4 through P7. The pinouts and signal names of the interface between the VXI Interface Board and the Main Board are shown in sheet 1 of the 1391 Pulse Board schematic, 1104-00-3612, in Section 7 of this manual. These address, data, and control signals are described in paragraph 4.3.2 and are illustrated in Figure 4-4.

4.3 PULSE GENERATOR BOARD – DIGITAL CIRCUITS

Refer to Figures 4-1 and 4-3, other indicated figures, and the Main Board schematic 1104-00-3612 in Section 7 of this manual for the paragraphs under this heading. The Main Board is naturally divided into "digital" and "analog" circuits, as indicated in Figure 4-1. These paragraphs will describe the theory of operation for the "digital" circuit blocks. The paragraphs under the 4.4 heading will be concerned with the "analog" circuit blocks of the Main Board and the with the Amplifier Board.

The interconnection of the digital circuits of the pulse generator is illustrated in Figure 4-3. The main signal path is indicated by the heavier signal lines. This signal path is for normal operation in Continuous Mode. The signal path will be different for each mode. The following paragraphs give a quick overview of the purpose of each digital circuit block shown in Figure 4-3. These descriptions will be followed by detailed circuit descriptions concentrating on each block.

Frequency Synthesizer

The synthesizer's output is a squarewave with a programmable frequency range of 1 mHz to 100 MHz. The synthesizer produces the basic timing signal for the continuous modes. The synthesizer also provides the internal trigger source for non-continuous modes. The synthesizer's output is routed to the SYNC output to provide clock outputs from 50 MHz to 100 MHz.

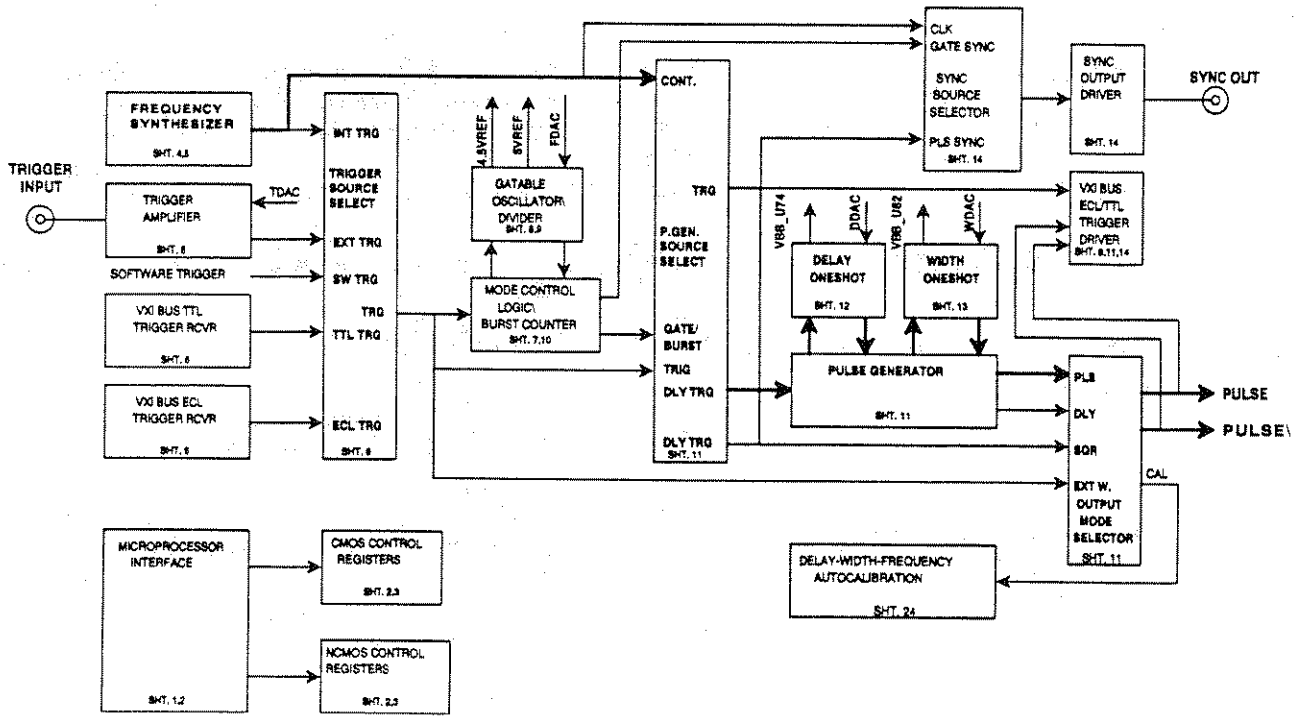


Figure 4-3. Pulse Generator Digital Circuits Block Diagram

Trigger Amplifier

The trigger amplifier conditions the external triggering signal applied to the TRIG IN BNC connector. The trigger level is controlled by the TDAC signal from the analog section.

VXI Bus TTL Trigger Receiver

The trigger receiver selects one of the 8 VXIbus TTL Trigger Lines to trigger the model 1391 when non-continuous modes are selected.

VXI Bus ECL Trigger Receiver

The trigger receiver selects one of the two VXIbus ECL Trigger Lines to trigger the model 1391 when non-continuous modes are selected.

Trigger Source Selector

The trigger source selector selects one of five triggering sources to trigger the model 1391 when non-continuous modes are selected.

Mode Control Logic/Burst Counter

The mode control logic provides a gating signal to the gatable oscillator/divider upon receiving a trigger when gated or burst modes are selected. In gated mode, the oscillator runs for the duration of the triggering signal. When burst mode is selected, the gatable oscillator runs until the programmed number of cycles have been produced. The mode logic also provides an output GATE SYNC, routed to the sync output driver, coincident with the oscillator's gating signal.

Gatable Oscillator/Divider

The oscillator's output is a squarewave with a programmable frequency range of 25 to 50 MHz when gated on by the mode control logic. The oscillator's frequency is controlled by the FDAC signal from the analog section. The oscillator also provides two reference voltages, 4.5VREF and 5VREF used by the analog section. The divider produces frequencies from 1 mHZ to 50 MHz from the oscillator's output.

PGEN Source Selector

The source selector selects the pulse generator's triggering source. The selector produces three outputs, TRG, DLY TRG, and DLY TRG G, from the selected triggering source. The TRG output is the triggering source. This output can be routed to the VXI bus ECL Trigger Lines to drive other model 1391's configured as slaves. The DLY TRG output is the triggering source delayed by about 20 nS. This output is routed to the sync output driver to produce a synchronizing output coincident with the pulse output. The DLY TRG G signal is a narrow glitch coincident with the leading edge of the DLY TRG signal. This signal clocks the pulse generator. The 20 nS delay between the TRG signal and the DLY TRG and DLY TRG G signals accounts for the time delays incurred driving and receiving the VXIbus ECL Trigger Lines so that master and slave model 1391's are time synchronized.

Delay and Width Oneshots

The delay and width one-shots produce narrow output glitches at a programmed time delay after they are triggered. The oneshots have two sections; a coarse resolution digital section and a fine resolution analog section. The digital sections provide 10 ns steps, while the analog sections provide 100 ps steps. The analog delay sections are controlled by the DDAC and WDAC signals from the analog section. The VBB_U74 and VBB_U82 signals are used to generate the control voltages.

Pulse Generator

The pulse generator circuitry routes the DLY TRG G signal to the delay and width oneshots. The delay one-shot is always triggered by the DLY TRG G signal. The delay one-shot's output triggers the width oneshot. The signal routing for normal and delayed pulses are the same. A normal pulse is a delayed pulse with zero programmed delay. When the width one-shot is triggered, a flip-flop is set. The flip-flop is reset by the width one-shot's output. The flip-flop's output is a pulse whose width is determined by the width one-shot's programmed time delay.

When double pulses are selected, the DLY TRG G signal triggers both the width and delay one-shots. The width one-shot is immediately triggered, producing a pulse, and then retriggered by the delay one-shot, producing a second pulse. When the delay oneshot is triggered, a second flip-flop is set. The output of the delay one-shot resets the flip-flop. This flip-flop produces a pulse whose width is equal to the programmed delay. This pulse, DLY, is used to calibrate the delay one-shot.

Output Mode Selector

The output mode selector selects the signals to drive the differential ECL signals PULSE and PULSE\. These signals drive the analog section, the VXI bus ECL/TTL trigger lines, and the autocalibration circuitry. For normal, delayed, and double pulses, the pulse generator's output is selected. For squarewave outputs, the DLY TRG signal is selected. The TRG signal is selected for external width mode. The DLY signal is selected during an autocalibration of pulse delay. The CAL signal is a TTL version of the PULSE and PULSE\ signals.

Sync Source Selector

The sync source selector selects one of three signals to drive the sync output driver. The selector also has several programmable time delays to account for the model 1391's many operating modes.

Two types of sync are available from the model 1391; *pulse sync* is coincident with the rising edge of the pulse output, *gate sync* is high when bursts of pulses are generated or the pulse generator is gated.

When square waves over 50 MHz are programmed, the frequency synthesizer's output is routed to the sync driver.

Sync Output Driver

The sync output driver level shifts the sync source selector's ECL output to drive TTL levels into a 50 ohm load.

VXI Bus ECL/TTL Trigger Driver

The trigger driver routes the PULSE or the TRG signal to any one of the 8 VXI bus TTL trigger lines. The PULSE and TRG signals can also be routed to either of the two VXI bus ECL trigger lines as well.

Delay - Width - Frequency Autocalibration

The autocalibration circuitry is used to characterize the gated oscillator frequency and the delay and width one-shots digital section's periods.

Microprocessor Interface

The interface allows the microprocessor's parallel data bus to talk to the serial data CMOS and NCMOS control registers.

CMOS and NCMOS Control Registers

The registers control the analog and digital sections of the model 1391. The CMOS control registers have 0 to +5 volt output levels, and are used to control analog section and the VXI bus TTL trigger driver and receiver sections. The NCMOS control registers have -5.2 to -0.6 V output levels that are compatible with the ECL logic used throughout the model 1391.

4.3.1 Interconnect and Power Distribution

Sheet 1 of the Model 1391 Pulse Board schematic shows all of the connections between the pulse generator and the VXI Interface Board. All power supplies and instrument control originates from the VXI Interface Board. Coded lines are identified as follows: 'A' for address; 'D' for data, 'L' for a VXI Interface Board origin, and 'B' for a buffered line. Each front panel LED is independently enabled (logic low) or disabled (logic high) by the VXI Interface Board through control lines VA16 LD\, MID_LD\, FAIL_LD\ and RUN_LD\.

4.3.2 Digital Interface and Data Registers

Refer to Figure 4-4 and Pulse Board schematic sheets 2 and 3. Three types of digital control signals direct the Model 1391 operations: dynamic control, strobed control, and static control. Dynamic control lines originate from programmable logic devices U2 and U3. These lines are synchronized to Interface Board microprocessor system timing and are controlled by LR/W (Read/Write) and LUDS\ (data strobe) to insure proper timing. LUDS\ is enabled after the 16 data bus lines have stabilized following a data change. Address lines (LA[01:05 and 14:20]) are always controlled by the Interface Board microprocessor. Parallel Data lines (LD[00:15]) are bidirectional between the Interface and Pulse Boards. Parallel Data is restricted to the devices on sheet 24 of the Pulse Board schematic. The Pulse Board data interface on sheets 2 and 3 of the schematic is uses serial data on the bidirectional LD00 data line.

U2 acknowledges successful data transfer between the Pulse Board and VXI Interface Board (DTACK\). Absence of this important signal results in a Bus Error (BERR\) at the Interface microprocessor. U2 also generates three strobes for the data register decoders. REGSA strobes U1, REGSB strobes U8, and REGSC strobes U9. U1, U8, and U9 generate all of the strobed control signals. The RLYEN\ dynamic control signal generated by U2 determines when the attenuator relays can be energized (sheets 21 and 22 of the Pulse Board schematic). U2 also generates the DAC1_LD and DAC2_LD dynamic control signals which load data to the DACs on sheet 15 of the schematic.

U3 buffers the bidirectional LD00 serial data line as LDATA00, which is the source of data to all of the serial data registers, which produce all of the static contol lines for the pulse generator circuitry. U3 controls the reading and writing of serial data to and from U4, the serial Calibration Data Memory. U4 is a 4096 bit EEPROM, organized as 256 sixteen bit words. CS_SMEM\ and SMEM_CLK are dynamic controls lines to U4, LDATA00 is the input data, and SMEMDOUT is the output data. This allows the microprocessor to read from and write to the Calibration Data Memory, U4, using U3 and LD00. CS_ADC\ and CS_901\ are dynamic control signals used to select the ADC (U109, Analog-to-Digital Converter) and the Counter/Timer (U112) on sheet 24 of the schematic. ADC_SCLK is the ADC clock.

When both REGSA (from U2) and LUDS\ (from the VXI Interface Board) are low, 3 to 8 line decoder U1 briefly enables (pulses low) one of eight control lines (Y0 through Y7), as determined by the status of address lines LA[14:16]. Four of these eight strobed control lines operate the three serial data registers U7, U11, and U15, which produce the static control lines

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Figure 4-4. Digital Interface and Data Registers

for the pulse generator circuits that operate at normal TTL or CMOS levels. S_CLK\ clocks all serial data. R_EN1\, R_EN3\, and R_EN2\ strobe registers U7, U11, and U15. U7 controls the output attenuator relays (sheet 21) and the frequency reference (sheet 24). U11 controls transition time range selection (TR1\, TR2\, TR3\ lines to sheet 19 and the LE<10NS and TE<10NS lines to sheet 17) and PAM enable and modes (PAMEN\, NPSEL\, and PPSEL\ lines to sheet 16). The serial data outputs of U7 and U11 are also used to supply data for the quad DACs, U87 and U89 on sheet 15. R_EN3\ is sent to enable serial data register U15 (sheet 3), which controls the selection of TTLTRIG* outputs to and inputs from the VXIbus backplane (sheet 6).

The remaining U1 generated signals control the ADC (U109, U110, and U11 on sheet 24) and the BUS trigger. SWTRIG\ is the software generated trigger signal. ADCL_EN\, ADCL_CLK\, and ADCR_CLK\ are sent to select and enable serial data registers U110 and U111. The serial data output of U109 is connected to the serial data input of U110, cascading them to transform the serial ADC data into 16 bit words [LD00:16] for the microprocessor.

U5 and U6 are level shifters, which translate the normal CMOS levels of the LA[14:16], REGSB, REGSC, LUDS\, LDATA00, S_CLK\, and LRESET\ signal lines to NCMOS. These signals, now with a "T" in front of their names, control two more data decoders, U8 and U9. These decoders operate as described for U1, except that their outputs (strobed control lines) are at NCMOS levels.

TDATA00, TS_CLK\, and TRESET\ are buffered by U10 and are sent as inputs to the NCMOS data registers (U13 through U20, except U15, on sheet 3).

U8 generates the strobes, R_CLK[0:6]\, for the NCMOS data registers. U9's outputs are buffered by U12 and sent as strobed control signals to various pulse generator circuits. DDNCEN and WDNCEN are sent to the Delay and the Width one-shots (sheets 12 and 13) to enable the DNC2016 counters. Likewise, CDNCEN, SDNCEN, and BDNCEN are sent to DNC-2016 enable pins in the clock divider (sheet 9), frequency divider (sheet 5), and the burst counter (sheet 10). PLLEN enables the single-chip PLL, U21, on sheet 4. BRSTCNT (buffered reset to counters) initializes and clears the Mode Control logic (sheet 7), the Burst Counter (sheet 10), the Pulse Generator (sheet 11), the Delay one-shot (sheet 12), and the Width one-shot (sheet 13).

The NCMOS data registers, strobed by U8, are on sheet 3 of the Pulse Board schematic. These are U13 through U20, excluding U15. NCMOS levels are created by running CMOS devices with –5.2V at their ground pins and –0.6V (a diode drop from ground) at their supply pins. The resulting NCMOS logic levels can be used as static control lines to ECL logic without further logic level translation.

4.3.3 Frequency Synthesizer

The frequency synthesizer consists of two sections; a phase locked loop (Pulse Board schematic, sheet 4) and a frequency divider\selector (sheet 5). The phase locked loop produces an ECL level square wave between 50 and 100 MHz with 10 KHz resolution. A basic phase locked loop consists of a phase comparator, a loop filter, a VCO, and a programmable (÷ N) counter. The phase comparator drives the VCO via the loop filter until the ÷ N counter's output is the same frequency and phase as the reference frequency. For

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Figure 4-5. Dual Modulus PLL

output frequencies between 50.01 and 100.00 MHz, "N" ranges between 5001 and 10000, with a reference frequency (1 LSB step) of 10 kHz. The loop filter determines the loop dynamics as well as supresses reference frequency sidebands. The model 1391 employs a slightly different loop, called Dual Modulus prescaling. This technique produces an additional digit of resolution at the same time as it scales down the 100 MHz VCO frequency to a value that the ÷ N counter can manage. A simplified dual modulus phase locked loop is shown in figure 4-5. The VCO's output is applied to the dual modulus prescaler. The prescaler divides F_{out} by "P" or "(P+1)" under control of the MC signal. The prescaler's output drives two low speed counters; ÷ A and ÷ N. The divide by A counter controls the prescaler's division ratio.

The counter system operates as follows. The overall division ratio, N total, is factored into two parts; A and N. Values for A and N are calculated from the equation: $N_{total} = (N*P)+A$. The counter system divides F_{out} by the value "(P+1)" A times and then divides F_{out} by the value "P" (N-A) times. In the model 1391, "P" equals 64. For example, to produce a 100.00 MHz output, N_{total} = 10000, therefor A = 16 and N = 156 (10000 = 16 * 65 + 140 * 64).

Refer to the schematic, sheet 2. The phase locked loop's reference is provided by the 10 MHz VXI bus CLK10 signals, BCLK10+ and BCLK10–. U29 buffers the reference to drive U21's reference input. U21 contains a reference divider programmed to divide by 1000 to provide the 10 kHz reference for the phase locked loop. U21 also contains the divide by A and N counters along with the phase comparator. U21's dividers are programmed serialy by the microprocessor. Serial data, PLLDATA, is clocked into U21 by the S_CLKA\ signal. The data is latched into U21 by the PLLEN line. The phase detector's output is applied to the loop filter comprised of U23 and it's associated components. The phase detector's output contains 10KHz reference frequency components that would modulate the VCO's output. The sideband suppression filter, comprised of U22 and it's associated components filter out the reference frequency components. Additional high frequency filtering is provided by R-C filter R14-C23. U24 and it's associated components form the VCO. The VCO's frequency is determined by the LC tank circuit comprised of L1 and varactor diodes CR14 thru CR17. As the voltage on the varactor diodes cathodes rises, the diodes capacitance decreases, increasing the VCO's frequency. CR13, CR18, and R15 limit the range of the VCO's control voltage to ensure startup when power is applied. U24's 50.01 to 100.00 MHz output is buffered by U30. U25 divides the buffered VCO output by 64 or 65 as selected by U21's MC output. The phase locked loop is powered by isolated supplies provided by U26 thru U28. The VCO's 50.01 to 100.00 MHz output is successivly divided by two to provide lower output frequencies. The buffered VCO output is applied to multiplexer U33 and to divide by two stage U32\A. U32\A's output drives hte multiplexer, U33, and the second divide by two stage U32\B.

4.3.4 TBF

4.3.5 Diagnostic Interface

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4.4 PULSE GENERATOR BOARD – ANALOG CIRCUITS

Refer to the model 1391 Analog Block Diagram (figure 4-6). The sheet numbers shown inside the circuit blocks correspond to the schematic diagram sheet numbers of the model 1391 main board (1104-00-3612).

4.4.1 Main High Speed Analog Signal Path

The differential ECL level pulse from the pulse generator circuitry is applied to the level shifter. The level shifter converts the ECL (-0.9 to -1.8 volt) levels to a pulse of about 3 Vp-p centered around ground to drive the current switch. The current switch alternately switches the REI1 and FEI1 currents from the transition control current sources into the timing capacitors. As the timing capacitors charge, a linear voltage ramp is produced. The larger the REI1 or FEI1 current, the faster the timing capacitor will charge, providing faster edge transitions. Four ranges of timing capacitors can be selected to allow programming slower edge transitions. A larger timing capacitor produces a slower edge speed.

The limiter restrains the voltage on the timing capacitor to 1.2 volts p-p. The resulting trapezoidal waveform has smooth leading and trailing edges but large amounts of overshoot that is dependent on the programmed edge speed. The trapezoid shaper clips off the top and the bottom parts of the trapezoidal waveform. The shaper also allows selective clipping of the top or bottom portions of the waveform to produce positive- or negative-going pulses. The multiplier provides gain control to adjust the peak-to-peak output amplitude of the pulse. The pulse amplitude can be modulated via the PAM IN BNC connector. The output amplifier provides voltage and current gain to produce 16 Vp-p pulses into a 50 Ω load. The output amplifier includes 3 attenuators to produce low level pulses. The signal on the VXI SUMBUS can also be added to the pulse output using the sumbus driver.

The sumbus driver contains circuitry to drive and receive the signal on the VXI Sumbus. The sumbus driver produces a current output to the sumbus proportional to the amplitude of the pulse output.

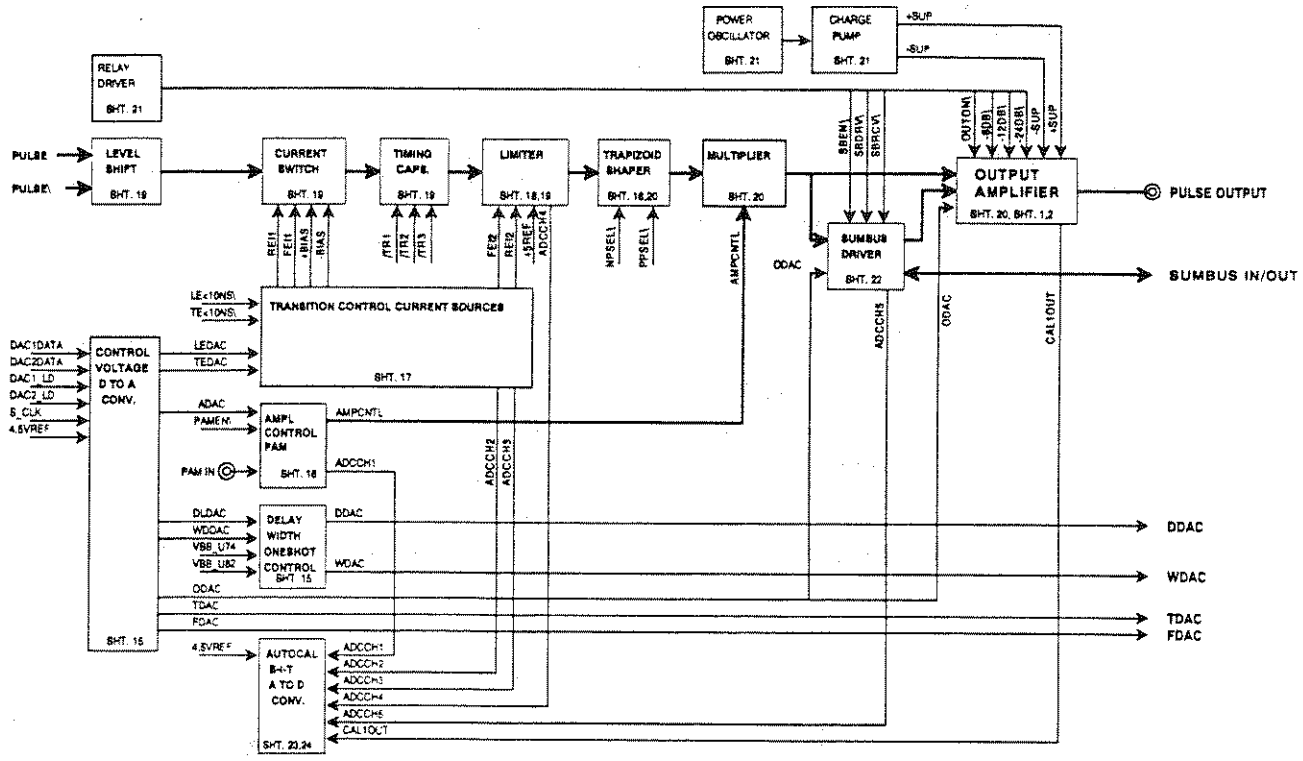

Figure 4-6. Pulse Generator Analog Circuits Block Diagram.

Support Circuitry

The support circuitry provides the control voltages and currents required by the high speed analog signal path, and other sections of the model 1391.

Control Voltage D to A Convertors

The Digital to Analog Convertors (DAC) provide control voltages to adjust the pulse output transitions, amplitude, and offset, the analog width and delay one-shots, the trigger level, and the gated oscillator frequency.

Transition Control Current Sources

The current sources produce current outputs proportional to the control voltage DAC LEDAC and TEDAC outputs to control the leading and trailing edge speeds.

Amplitude Control / PAM

This circuitry processes the control voltage DAC output ADAC, and the PAM IN signal to produce the control voltage for the multiplier, AMPCNTL, to vary the output amplitude.

Delay/Width One-shot Control

This circuitry processes the control voltage DAC outputs DLDAC and WDDAC to produce the control voltages for the width and delay analog oneshots, DDAC and WDAC.

Relay Driver

This circuitry buffers the control lines to drive the relays in the output amplifier and sumbus driver.

Power Oscillator

The power oscillator provides a 12 Vp-p, 100 KHz square wave to drive the charge pump voltage convertor.

Charge Pump

The charge pump produces approximate ± 30 V power supply rails, +SUP and -SUP, from the ± 24 V VXIbus supplies and the power oscillator output. These high voltage supplies are required for the output amplifier.

Autocal-BIT A to D Convertor

The Analog to Digital Converter (ADC) measures the output amplifier output to calibrate the pulse amplitude and offset. The ADC also monitors several control voltages throughout the analog circuitry for the "Built In Test" function.

4.4.2 Level Shift

See Schematic Diagram Sheet 19 (1100-04-3612). U98 receives the differential pulse signal from the pulse generator. Dual diodes CR45 and CR46 biased by R125 thru R128 level shift U98's output about 1.2 volts negative. The bases of Q41 and Q42 swing thru about -2.1 to -3 volts. Q41 and Q42 are configured as a long-tailed pair biased from a constant current source via diodes CR47 and CR48. Q43 and it's associated components form a constant current source.

The voltage across CR50 is impressed across R132 producing a collector current in Q43 of about 28 mA. CR49 offsets the Vbe of Q43 providing first order temperature compensation of current. When pin 6 of U98 is high (pin 7 is low), Q41 is turned on and current flows from ground thru Q41 and CR47 into Q43. Q42 is off and it's collector sits at about +1.5 volts as set by the voltage divider R133 and R134. With pin 6 low, Q41 turns off and Q42 turns on and Q42's collector sits at about -1.5 volts. To increase the speed of the level shifter, Q41 and Q42 are not allowed to turn completely off. R129 and R130 provide a small (about 1 mA) current bleed to keep the stage biased.

4.4.3 Current Switch

See Schematic Diagram Sheet 19 (1104-00-3612). Complementary emitter followers Q44 and Q45 buffer the level shifter output to drive the diode switching bridge. CR51, biased by R135-R138, compensates for the Vbe's of Q44 and Q45. C96 and C97 provide AC bypass around CR51 to preserve the edge speeds.

The diode bridge comprised of CR52 thru CR54 alternately switches the FEI1 and the REI1 currents into the timing capacitors. Common base stages Q46 and Q47 buffer the diode bridge from the output capacitance of the current sources, and stray PCB capacitances. The bases of Q46 and Q47 are baised at about ± 5 volts by a resistive divider located in the transition control current sources. When the level shifter's output is high (about +1.5 volts), CR53 is forward biased and Q44 sources current into the REI1 current source and reverse biases the lower section of CR54. CR52 is reverse biased and the FEI1 current flows thru the upper section of CR54 and into the timing capacitor. When the level shifter's output is low (about -1.5 volts), CR52 is forward biased and Q45 sinks the current from the FEI1 current source and reverse biases the upper section of CR54. CR53 is reverse biased and the REI1 current flows out of the timing capacitor thru the lower section of CR54.

4.4.4 Timing Capacitors

See Schematic Diagram Sheet 19 (1104-00-3612). Four ranges of transition time are provided by timing capacitors C106 thru C109. The fastest transition range is set by C106 and stray capacitances. Timing capacitors C107 thru C109 are switched in one at a time by diode switches CR56 thru CR58 driven by level shifter Q48.

The operation of the three diode switches are the same. Only the C107 switch will be explained. C107 is selected by driving the TR1/ line to a CMOS logic low (0 volts) which turns on Q48/A. Current flows thru Q48/A and R147 and forward biases both sections of CR56. The bottom end of C107 then see's a low impedance to ground and is effectively put in parallel with C106 slowing down the edge speed.

With the TR1/ signal at a CMOS logic high (+5 V), Q48/A is turned off and it's collector is pulled to –12 volts via R148 reverse biasing the upper section of CR56. The lower section of CR56 is reverse biased to about -7.2 volts, set by voltage divider R145 and R146, via R142.

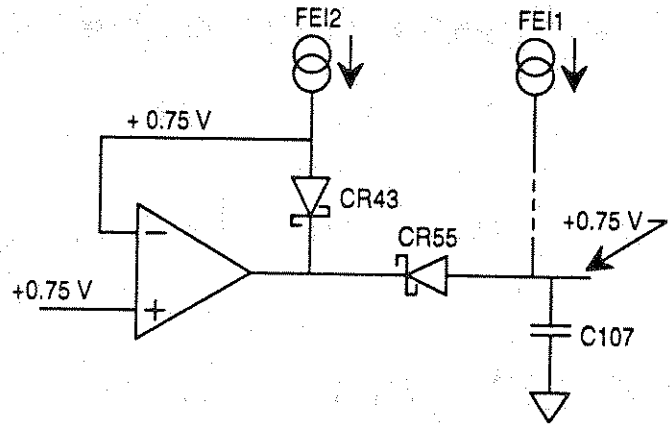

Figure 4-7. Simplified Upper Level Limiter.

4.4.5 Limiter

See Schematic Diagram Sheets 18,19 (1104-00-3612). The voltage across the timing capacitor is limited to about ± 0.75 volts by the limiting circuit. U48/D buffers the 5 volt reference applied to inverting amplifier U97/D. RN26/A and R124 set the gain to -0.15 producing the lower limit level of -0.75 volts. U97/B, arranged as a unity gain inverter, produces the upper limit level of 0.75 volts. A simplified upper level limiter circuit is shown in figure 4-7. Feedback around U97/C maintains the voltage on the inverting input at +0.75 volts. As the voltage across the timing capacitor rises, CR55 conducts and the FEI1 current flows into U97. With FEI2 equal to FEI1, the voltage drop across CR43 is equal to the voltage drop across CR55, the voltage across the timing capaictor will limit at +0.75 volts.

Refer to the schematic. Q40 buffers the output of U97/C to sink the FEI1 and FEI2 currents. CR35 reduces the power dissipation in Q40. RN26/E bleeds a small current (about 1 mA) into Q40 to stabilize it's operating point. R221 and C77 provide U97/C with loop compensation. R256 limits Q40's base current on turn on, as well as damping high frequency oscillations. The lower level limiter operates in the same manner but with reversed polarities. R223 and R224 are part of the built in test circuitry. The midpoint of these resistors will sit very near zero volts when the limiter circuitry is operating correctly.

4.4.6 Trapezoid Shaper

See Schematic Diagram Sheets 16,20 (1104-00-3612). U99, configured as a non-inverting amplifier with a gain of 1.67, buffers the voltage on the timing capacitors to drive the diode shaper. R162 shapes the transient response of U99. U99 is powered from about +/- 6.9 volts via CR61 and CR62. The output of U99, BUTT, is waveform of about 2.5 volts p-p with smooth leading and trailing edges, but ugly top and bottom. The uglyness is caused by the turn off time of the limiter diodes. The diode shaper clips off the ugly top and bottom portions of the waveform.

A simplified shaper is shown in Figure 4-8. The bridge is fed constant currents via R157 and R158. When the BUTT signal is high, current flows thru R157 and the upper section of CR60 into R163, producing a voltage of about 0.5 volts. At the same time the lower section of CR59 is forward biased and current flows from the BUTT signal into R158. When the BUTT signal swings low, current flows thru R163 and the lower section of CR60 into R158, producing a voltage drop of about -0.5 volts across R163. At the same time, the upper section of CR59 is forward biased and current flows thru R157 and into the BUTT signal.

The end result is a clean 1 Vpp waveform across R163. If either of the constant currents is turned off, the waveform will be clipped at ground, producing monopolar pulses. Q34 sections C and B are configured as switches that turn off the current sources. Q34 sections A and D level shift the control signals NPSEL/ and PPSEL/ to drive the switches.

4.4.7 Multiplier

See Schematic Diagram Sheet 20 (1104-00-3612). The output of the trapezoid shaper is applied to the four quadrant multiplier, U101. Resistors R226 and R227 terminate the unused differential inputs of U101. R170 and R171 decouple the multiplier's negative power supply. R169 biases U101's positive power supply. U101 produces a differential current output, proportional to the product of the trapezoidal waveform and the AMPCNTL signal, into R172 and R231. Resistors R228, R232, R230, and R233 level shift the output to within the input common mode range of U102. U102 converts the multiplier's differential output into a single ended signal of about 2 Vpp maximun when the output is 16 Vpp into 50 Ω.

U102 is powered from the ± 5.2 volt rails via CR33 and CR34. Additional voltage gain is provided by non-inverting amplifier U100 and it's associated components. R166 and R167 set the voltage gain to about 2.6. R165 is used to shape U100's transient response. R168 isolates U100's output from the stray capacitance of the track leading to the sumbus driver.

4.4.8 Output Amplifier

See the Schematic Diagram Sheet 21 (1104-00-3612) and Schematic Diagram Sheets 1,2 (1104-00-3605). The multiplier's output signal, OADRV, drives the output amplifier board. The output amplifier is a discrete inverting stage that provides both voltage and current gain. The amplifier's output is the sum of the AMPDRV, SUMIN, and ODAC signals. The amplifier's gain for the AMPDRV and SUMIN signals is about -6.2 set by the ratios of the feedback resistors, R34, R35, and R38 to the input resistors R5 and R9. The gain for the ODAC signal is about -1.1 set by the ratio of the feedback resistors, R34, R35, and R38 to the input resistor R10. The output amplifier has two signal paths. There is a high speed AC path and a low speed DC correction path. The AC path is divided into two complementary sections, one for each polarity. Only the positive path will be described. C11 AC couples the virtual earth of the amplifier into the common base amplifier Q2. CR5 biases Q2's base to +15 volts, while R20 sets the stage's operating current to about 8mA. Emitter follower stage Q4 buffers Q2's collector to drive the gain stage Q6. Dual diode CR1 temperature compensates the Vbe's of Q2 and Q4. R22

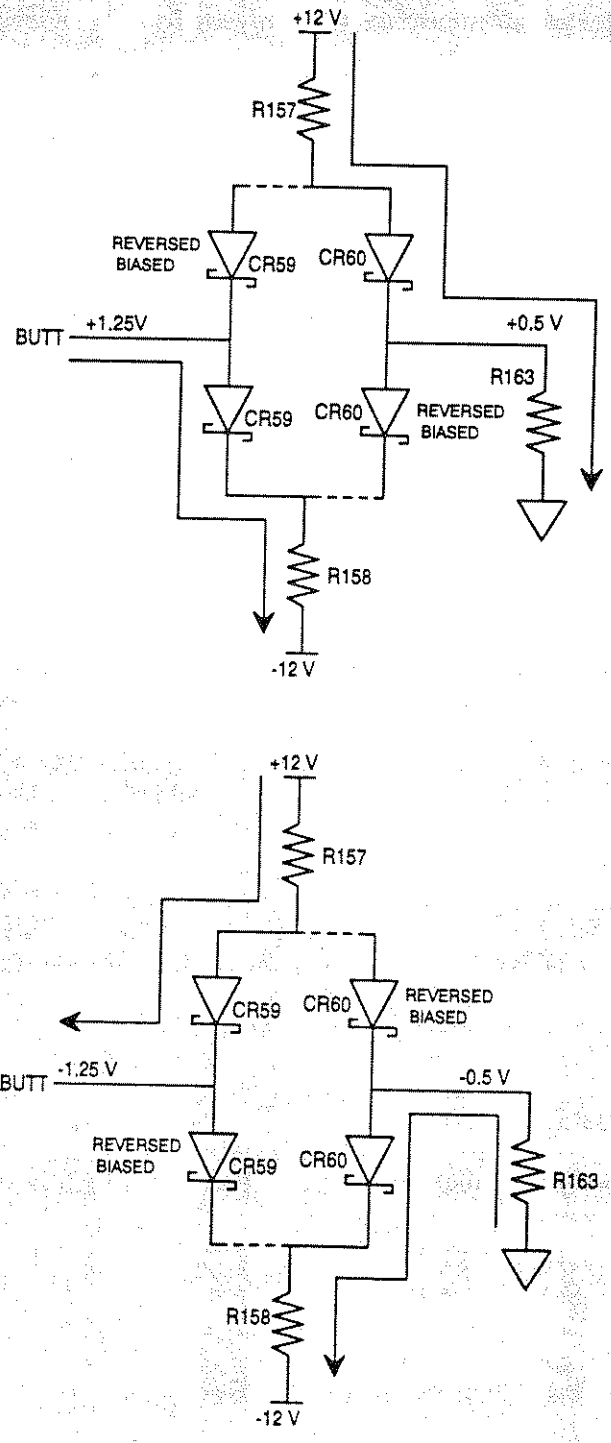

Figure 4-8. Simplified Trapezoid Shaper.

bleeds a small current into CR5 to ensure startup when power is applied. Q6 operates as a constant current source that is modulated by the AC signal. Q6's voltage gain is very high as it's collector load is the high impedance seen looking into the current source Q7. RC network C15 - R32 adjusts the overshoot of the stage. Local feedback around the AC path via C17 and C19 adjusts the waveform quality. Complementary emitter followers Q8 and Q9 buffer the gain stage's output. Diodes CR7 thru CR9 set the quiescent current in Q8 and Q9. R42 thru R45 prevent thermal runaway in Q8 and Q9. Protection diodes CR10 and CR11 limit the amplifier's output to the power supply voltages.

The amplifier's DC path is comprised of U3 and it's associated components, Q1, and CR14. U3 maintains the amplifier's virtual earth at zero volts by stealing current from Q6 via Q1. CR14 reduces the power dissipation in Q1. The operating current of Q6 is larger than that of Q7 so that Q1 alwas has to pull current from Q6. U3 is powered from voltage regulators U1 and U2. Zener diodes CR12 and CR13 reduce the power dissipation in the regulators.

The amplifier's 50 Ω output impedance is set by the parallel combination of R46 and R47. R11 allows for measuring the amplifier's output directly during an autocalibration. The amplifier's 50 Ω output is applied to three relay selected "pi" section attenuators. Relay K4 is used to dissable the output of the amplifier.

4.4.8 Sumbus Driver

See Schematic Diagram Sheet 22 (1104-00-3612). The sumbus driver is a wideband current output amplifier. A simplified schematic is shown in figure 4-9.

U105/B maintains the emitter of Q55 at about -3 volts, forcing a current of about 100 mA thru R191. This current is the sum of Q55's collector current and the current flowing in R189 and R187-R188. U104, configured as a unity gain differential amplifier, forces the voltage across R189 to be equal to the input signal SUMBDRV. Q54 buffers the output of U104. R189 is selected so that a 1 V pp input signal causes a 0 to 80 mA current in R189. Resistors R178 and R179 bias U104's inputs to zero volts forcing a constant 10 mA to flow in R187-R188. Q55's collector current will then swing between 10 and 90 mA. The 50 mA constant current source offsets Q55's collector current, producing an 80 mApp current into the VXI sumbus.

Referring to the schematics, CR65 provides a reference voltage referred to the +12 volt rail. A portion of the reference is impressed across R192 by U105/A and Q56, producing a collector current in Q56 of 50 mA, independent of power supply variations. R196 allows for adjusting the nominal current to set the zero offset of the driver. Relay K1 decouples the sumbus circuitry from the VXI backplane. R500 and R501 provide an internal 25 ohm load to allow testing of the sumbus circuitry. U106 configured as a non-inverting gain of two receives the SUMBUS signal. R200 adjusts the transient response of U106. U107, with an inverting gain of about 1.5, provides an overall gain of -3 between the VXI sumbus and the output amplifier. R204 adjusts the transient response of U107. U106 and U107 are powered from about +/-6.9 volts via zener diodes CR67 and CR68.

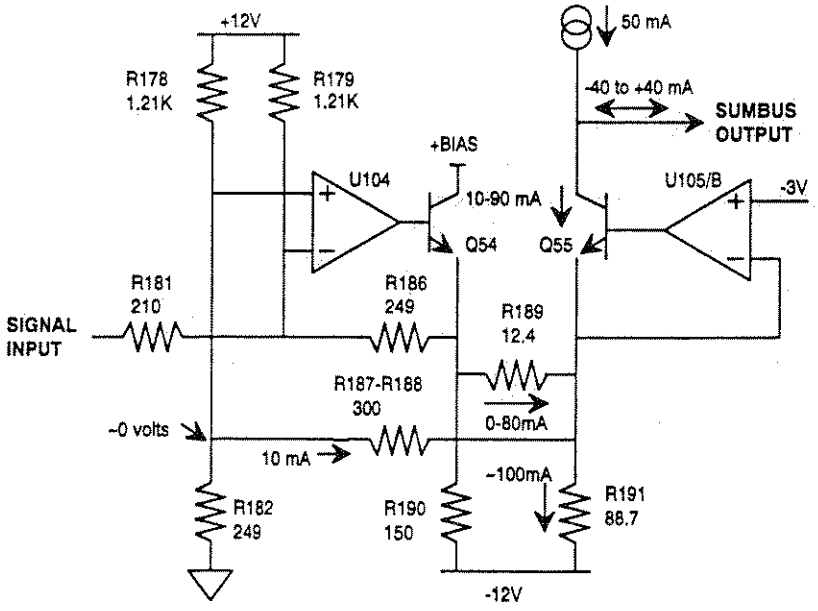

Figure 4-9. Simplified SUMBUS Driver.

4.4.10 Control Voltage D to A Convertors

See Schematic Diagram Sheet 15 (1104-00-3612). U48/B buffers the 4.5 volt reference voltage applied to quad 12 bit D to A convertors U87 and U89. Serial data, DAC1DATA and DAC2DATA, is clocked into the DAC's by the serial data clock signal S_CLK\. The data is latched with the DAC1_LD and DAC2_LD signals. Quad DAC U87 provides control voltages to the delay and width one-shot controls, the gatable oscillator, and the trigger amplifier. Voltage follower U90/B buffers the trigger level control voltage. Quad DAC U89 provides control voltages to the transition control current sources, the amplitude control/PAM circuitry, and the output amplifier. U90/A and it's associated components offset the DAC output and provide voltage gain to produce a bipolar output control voltage to set the output amplifier offset. R109 and the series/parallel combination of R110, R107-R108 provide a gain of about 7.26 to the DAC output and a gain of about -3.72 to the 4.5 volt reference. The net result is an output voltage swing of about ± 15.9 volts. Zener diodes CR30 and CR31 reduce the ± 24 volt rails to about ± 17.2 volts to power U90.

4.4.11 Amplitude Control/PAM Circuitry

See Schematic Diagram Sheet 16. The zero to 4.5 volt control signal ADAC is inverted by unity gain amplifier U93/C before being applied to the summing amplifier U93/D. The summing amp has a gain of about -0.232, providing a zero to 1 volt output control voltage to the multiplier AMPCNTL. The PAM_IN signal is inverted by unity gain amplifier U93/B and applied to the summing amplifier via analog switch U94/C. R113 adjusts the PAM scale factor to account for component tolerances. The summing amplifier's output can be monitored for testing via R213.

4.4.12 Transition Control Current Sources

See Schematic Diagram Sheet 17 (1104-00-3612). The trailing edge of the waveform is controlled by the TEDAC signal from the control voltage D to A convertors. U93/A buffers the DAC output to drive the two voltage dividers R214-R215 and R116-R117. Analog switches U94/A and B select which divider drives the current source. When a trailing edge speed of 10 ns or greater is programmed, the TE<10NS\ signal is high enabling U94/A via Q40, which selects the R214-R215 divider. The divider provides about a 0.28 volt input to the current source for a full scale TEDAC output. For trailing edges faster than 10 ns, the R116-R117 divider provides about a 3.5 volt input to the trailing edge current source.

U96/A drives the bases of Q38 sections D, B, and C via level shift zener CR39. Varying the base voltage of Q38 varies the collector currents. Q38/D's collector current produces a voltage drop across RN25/E. Common base stage Q38/A provides a constant collector load for Q38 section D. Q38/A's base is biased to about +5 volts by voltage divider RN24/D-R217. Negative feedback around the loop drives the voltage across RN25/E equal to the input control voltage at TP30. Because Q38 sections B and C are similar to section D, and their emitter resistors are equal, the collector currents will be equal to that of section D. Resistors R120 and R122 stop parasitic oscillations in Q38.

The leading edge of the waveform is controlled by the LEDAC signal from the control voltage D to A convertors. U96/C, an inverting amplifier with selectable gain, inverts and scales the LEDAC signal. When leading edges of 10 ns or greater are programmed, U96/C provides an input to the leading edge current source of about -0.28 volts for a full scale LEDAC output. When edges faster than 10 ns are programmed, the LE<10NS\ signal enables analog switch U94/D placing R118 in parallel with R216. U96/C then provides an input of about -3.5 volts to the leading edge current source.

The operation of the leading edge current source is the same as that of the trailing edge. The voltages across RN25 sections E and A can be monitored by R219 and R220 for testing.

4.4.13 Delay - Width One-shot Control

See Schematic Diagram sheet 15 (1104-00-3612). U85 section A, buffers the DAC output to drive inverting amplifier U85/D. The amplifier has an inverting gain of about 0.83 producing a swing of about 0.37 volts for a zero to full scale swing of the DAC. The amplifier adds an offset to the signal that tracks the threshold of the ECL comparator in the one-shot. The amplifier has a non-inverting gain of about 0.8 to the offset voltage. The amplifier's overall output is a swing from about -1 volts to about -1.37 volts to control the delay analog one-shot.

The operation of the width analog one-shot circuitry is identical to that of the delay one-shot.

4.4.14 Relay Driver

See Schematic Diagram Sheet 21 (1104-00-3612). U103 buffers the control lines to drive the relays in the output amplifier and SUMBUS driver circuits. Q53 and associated components switch the power supply to the relay coils. A flip-flop in the microprocessor interface section is set upon power up, which turns off Q53. Once the microprocessor is alive and in a known state, the flip-flop is reset, driving the RLYEN\ low, turning on the power to the relays.

4.4.15 Power Oscillator

See Schematic Diagram Sheet 21 (1104-00-3612). U118 a universal timer, running in the astable mode, oscillates at about 100 kHz. It's output at pin 3 is a 0 to 12 volt square wave. Complementary MOSFET's Q51 and Q52 buffer U118's output to drive the charge pump circuitry. C213 provides transient current to the MOSFET's. L2 decouples the switching spikes from the +12 volt supply. F1, a self-resetting circuit protector, shuts down the oscillator if excessive current is drawn.

4.4.16 Charge Pump

See Schematic Diagram Sheet 21 (1104-00-3612). The dual charge pump generates about ± 36 volt rails (unloaded) for the output amplifier. When loaded the rails drop to about ± 32 volts. The charge pump operates by stacking the ± 24 volt supplies on top of the power oscillator's 12 Vpp output. Simplified charge pumps are shown in Figure 4-10.

For the positive pump: When the power oscillator's output is low, C221 is charged to +24 volts thru CR37. When the oscillator's output swings up to +12 volts, CR37 is reverse biased and the top of C221 sits at +36 volts. C221's charge is dumped into C217 and C225 thru CR73. When the oscillator's output swings low again, CR73 is reverse biased preventing the discharge of C217 and C225. This cycle is repeated at about a 100 kHz rate.

For the negative pump: When the power oscillator's output is high, C222 is charged to 36 volts thru CR38. When the oscillator's output swings down to zero volts, CR38 is reverse biased and the bottom of C222 sits at -36 volts. C222's charge is dumped into C218 and C226 thru CR74. When the oscillator output swings high again, CR74 is reverse biased preventing the discharge of C218 and C226. This cycle is repeated at about a 100 kHz rate.

Going back to the schematic diagrams, multiple capacitors are used in parallel to reduce the ESR to improve the output voltage regulation. Self resetting circuit protectors, F2 and F3, disconnect the ± 24 volt supplies from the charge pumps if excessive currrent is drawn from the output amplifier.

4.4.17 Autocal/ Built - In - Test Circuitry

See Schematic Diagram Sheets 23,24 91104-00-3612). Unity gain followers U108 and U120 buffer the inputs of the A to D convertor U109. The outputs of the buffers are restrained to ± 5 volts by the dual diodes to protect the ADC from over-voltage. Resistor R209 is part of a voltage divider used to calibrate the output amplifier. U109 is a 12 bit succesive approximation convertor with a serial data output. Shift registers U110 and U111 convert the serial data to parallel data to simplify interfacing with the microprocessor. The A to D is clocked by a 4 MHz signal generated by dividing down the 16 MHz system clock.

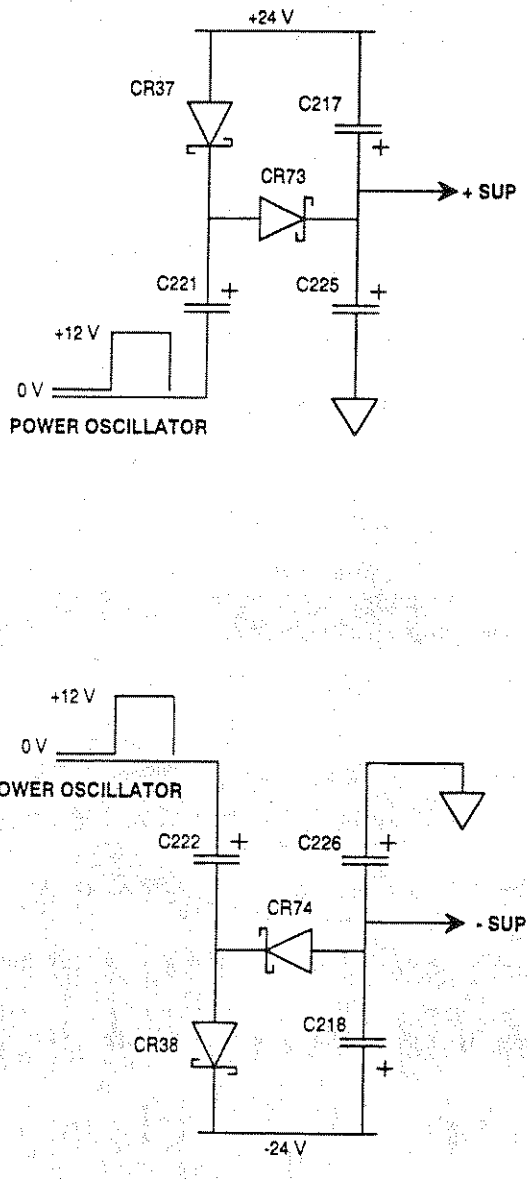

Figure 4-10. Simplified Charge Pump Circuits.

5.1 FACTORY REPAIR

Wavetek maintains a factory repair department for those customers not possessing the necessary personnel or test equipment to maintain the instrument. If an instrument is returned to the factory for calibration or repair, a detailed description of the specific problem should be attached to minimize the turn-around time.

5.2 CALIBRATION

Calibration is the process of *Scheduled Maintenance* as described in this section of the Model 1391 manual. Through Calibration, the unit is certified to be operational and within the specifications listed in Section 1 of this manual. The Calibration is valid over a specified *Calibration Interval*. After the interval (typically 1 year), the operator returns the unit to the metrology laboratory for Calibration. Units returned at the scheduled interval, without a failure description, may be calibrated and returned to the operator using the procedures in this section of the manual.

Start the Calibration with the *Performance Verification Procedure* following immediately in this section. Performance Verification tests the unit vigorously to the specifications in Section 1, using external test equipment and signals at the unit's input and output connectors. There are Performance Verification Data sheets at the end of this section which are intended to be copied and used to record the data values from the verification test. Completed Performance Verification Data sheets with no out-of-tolerance readings is sufficient for certification of Calibration and return to the operator.

If there are out-of-tolerance readings, perform the Alignment Procedure later in this section. After successful completion of alignment, repeat the Performance Verification Procedure.

If the Alignment Procedure cannot be run successfully, or if the Performance Verification Data still has out-of-tolerance readings after alignment, then refer to Section 6 of this manual for *Fault Isolation*.

The Performance Verification Procedure may also be run before and after *Unscheduled Maintenance* (Troubleshooting) to locate problems and to ensure that all failures have been repaired.

5.3 REQUIRED TEST EQUIPMENT

The test equipment required to perform the Performance Verification Procedure and the Alignment Procedure is listed in table 5-1.

Table 5-1. List of Test Equipment

Equipment	Quantity	Specifications
VXI Requirements	1	VXI chassis
	1	VXI slot-0 controller
	1	VXI "C" size extender board (Optional-see text)
Multimeter	1	HP 3478A or equiva lent
Oscilloscope	1	Tektronix 2465 or equivalent
Frequency Counter	1	HP 5334A Universal Counter
Adaptor	1	BNC female to double banana jacks
Coaxial cable	1	BNC male connectors, RG58U cable
Probe	2	10 MΩ
50Ω Termination	1	Feedthrough, 0.1% accuracy, 2W

5.4 PERFORMANCE VERIFICATION PROCEDURE

TBF

5.5 ALIGNMENT PROCEDURE

TBF

6.1 TROUBLESHOOTING

To be supplied with the Revision "A" manul (without the "Preliminary" designation).

7.1 DRAWINGS

The following schematics and assembly drawings are in the arrangement shown below.

7.2 ERRATA

Under Wavetek's product improvement program, the latest electronic designs and circuits are incorporated into each Wavetek instrument as quickly as development and testing permit. Because of the time needed to compose and print instruction manuals, it is not always possible to include the most recent changes in the initial printing. Whenever this occurs, errata pages are prepared to summarize the changes made and are inserted inside the shipping carton with this manual. If no such pages exist, the manual is correct as printed.

7.3 ORDERING PARTS

When ordering spare parts, please specify part number, circuit reference, board, serial number of unit and, if applicable, the function performed.

NOTE

An assembly drawing number is not necessarily the assembly part number. However, the assembly parts list number is the assembly part number.

DRAWING	DRAWING NUMBER
Outline Drawing	0002-00-0694
Instrument Schematic	1004-00-0694
Instrument Assembly Drawing	1001-00-0694
Instrument Parts List	1000-00-0694
Main Board Schematic	1104-00-3612
Main Board Assembly	1101-00-3612
Main Board Parts List	1100-00-3612
Amplifier Board Schematic	1104-00-3605
Amplifier Board Assembly Drawing	1101-00-3605
Amplifier Board Parts List	1100-00-3605
Spares Kit Parts List	1200-00-3613

A.1 INTRODUCTION

This appendix covers the remote operation of the Model 1391 VXIbus Pulse Generator using the CIIL language in a MATE system. Section 3 of this manual covers the "Native" SCPI operation of the unit. This appendix discusses the MATE system (hardware and language) and the commands and syntax the Model 1391 MATE Pulse Generator will recognize.

A.2 THE MATE SYSTEM

The MATE (Modular Automatic Test Equipment), an Air Force specification for automated test systems, standardizes general purpose test equipment interconnection, installation, and control syntaxes. To recognize MATE commands, the unit must be specified as a "Model 1391 MATE" rather than a standard Model 1391 at the time of purchase.

A.2.1 MATE Hardware

Because of constraints of the VXIbus environment, VXIbus modules do not implement a complete MATE hardware configuration. There will be no panel mounted MATE interface enable switch or Discrete Fault Indication connector usually associated with MATE equipment. Nor is there a front panel display device to indicate MATE status at power-on.

MATE compatibility is limited to CIIL language processing in VXIbus modules. In the Model 1391 MATE, this is accomplished with an instrument ROM change, where both the SCPI and CIIL language parsers are contained in the instrument's firmware. MATE units default into the CIIL parser at power-on.

A.2.2 MATE Language

The operator programs the MATE system controller using the ATLAS language. The controller communicates with the Model 1391 MATE via the IEEE-488 bus (external host) or via the VXIbus (embedded controller) using the CIIL command strings. The Model 1391 MATE uses its language parser to translate the CIIL command strings into the Model 1391's native SCPI language. This appendix deals with only the CIIL commands.

ATLAS (Abbreviated Test Language for All Systems) is an easy-to-read English-like language. The ATLAS language does not allow partial instrument setups. This means all items, except defaults, must be entered in each string. For further information on the ATLAS programming language, refer to ANSI/IEEE Std 416-1981, IEEE Std 716-1982, and IEEE Std 717-1982.

The system uses the CIIL (Control Interface Intermediate Language) language to communicate between the controller and the Pulse Generator. The CIIL commands are sent as an ASCII string. The CIIL language uses standard sets of commands which allow the Model 1391 MATE to be used in test systems without the necessity of rewriting the test software. However, this limits the language to standard commands that will function for all manufactures of a specific type of test equipment. To utilize any unique features of the Model 1391 MATE, it is necessary to use the `GAL` command to exit from the CIIL language and use the native language of the Model 1391 MATE. Use `SYST:LANG:CIIL` command while in native language to return to CIIL. For more information on the CIIL language, refer to Air Force standard 2806763 Revision C, 21 June 1988. The following list defines the Model 1391 MATE's MATE/CIIL capabilities:

- Set up of Pulse Generator functions and pulse characteristics.
- Burst, triggered, gated or continuous output mode setup.
- Output amplitude and dc offset control.
- Output frequency/period/pulse repetition rate control.
- External trigger/gate slope and level control.
- Pulse amplitude modulation.

A.3 THE MODEL 1391 MATE IN THE MATE SYSTEM

A.3.1 System Connection

The Model 1391 MATE is part of a VXIbus system, and it resides in a VXIbus chassis. As such, it is subject to all benefits and restrictions of the VXIbus environment. When the MATE controller is external to the VXIbus chassis, it communicates over the GPIB bus to the GPIB/VXIbus *translator* located in the Commander (slot 0) slot of the VXIbus chassis. In this case, the VXIbus chassis has a Primary GPIB Address and the 1391 MATE module within the chassis is reached with a GPIB Secondary Address. When the VXIbus Commander is an embedded controller, the GPIB bus is not involved and communication between the Commander and the 1391 MATE module is restricted to the VXIbus Protocols.

The system interconnections for a 1391 MATE unit are the same as for the standard unit described in Section 3 of this manual.

A.3.2 Identifying a Model 1391 MATE

There are two methods of verifying a 1391 is a MATE unit. First, check the "rear panel" of the module; the serial tag between the P1 and P2 connectors will indicate "1391 MATE" for a MATE unit and "1391" for a standard unit under the model number. Also, if the module(s) are plugged into the VXIbus chassis, a standard unit will respond with full Manufacturer and Model number information to the mandated IEEE-488.2 `*IDN` command, whereas the 1391 MATE unit responds with a "space" character, indicating a non-MATE command.

A.4 THE CIIL LANGUAGE

The notations listed in Table A-1 represent the elements of CIIL command strings used in this manual. These notations aid in describing the correct syntax for command strings. In practice the controller transmits the ASCII code for the indicated syntax.

A.4.1 CIIL Command Strings

Shown below is the standard form of the CIIL command string:

```
<op code><b><noun><b><channel
number>[<b><set code><b><mod-
ifier<b><value>..]<cr,lf>
```

Table A-2 defines the command string items used by the Model 1391 MATE. Figure A-1 contains the detailed Pulse/Timing Generator syntax diagrams.

A.4.2 Syntax Paths

The path, as shown in Figure A-1, through the syntax diagram follows the standard form of the CIIL command string. All commands appearing on the syntax path must be included in that command string. When the Model 1391 MATE receives a `<cr,lf>` (carriage return and line feed), the unit assumes the command string is complete. On the diagram, a solid line bypassing some commands indicate defaults; adjacent to each default line is a default value. To get a default, omit the default command from the string.

Table A-1. CIIL Notations

Notation	Meaning
|	Separator between elements in a set of values. Only one element of the values presented may be selected.
<>	These brackets surround elements in a string that are necessary for a complete command string.
[ ]	These brackets surround optional elements in a command string and are not necessary for a complete command string.
...	Indicates that other elements may be required or desired as part of the command string.
b	Indicates the necessity for an ASCII space in the part of the command string where it appears.
chan num	Indicates that a channel number must be specified as part of the command string where it appears.
set code	Indicates that a CIIL set code must appear as part of the command string where it appears. There are only three set codes. They are: SET|SRN|SRX.
noun	Indicates that a CIIL noun must appear as part of the command string where it appears.
modifier	Indicates that a CIIL modifier must appear as part of the command string where it appears.
value	Indicates that a numeric value must appear as part of the command string where it appears. This number can be expressed in floating point, engineering or integer notation. Can also indicate a non numeric value; the possible non-numeric choices in that instance are given in the syntax diagrams.
<cr, lf>	Indicates the necessity for an ASCII carriage return followed by a line feed in the command string where it appears.

Table A-2. Model 1381 MATE CIIL Commands

Type	CIIL Command	Description	Limits
Op Code	CLS	Closes - activates Pulse Generator output	None
	CNF	Initiates confidence test	None
	FNC	Selects function	PDC, PDT, SQW, or PAM.
	IST	Initiates self-test	None
	OPN	Opens - deactivates Pulse Generator output.	None
	RST	Reset-deactivates Pulse Generator output and returns Pulse Generator to power-up conditions.	None
	STA	Requests status	None
Noun	PAM	Pulse Amplitude Modulation	None
	PDC	Selects single pulse output.	
	PDT	Selects double pulse output.	
	SQW	Selects square wave output.	
Chan Num	:CH0	Selects module	0 only
Set Codes	SET	Set value	None, each code has the same effect on the Model 1391 MATE.
	SRN	Set minimum	
	SRX	Set maximum	
Modifiers	BURS	Sets up burst count.	PDC, PDT, SQW, or PAM: 1 to 10e6 counts.
	CAMP	Sets pulse carrier amplitude (PAM).	PAM only; 0.15 to 16.0 Vpp, (50Ω).
	CFRQ	Sets pulse carrier frequency (PAM).	PAM only; 0.001 Hz to 50e6 Hz.
	DCOF	Sets up dc offset of selected waveform.	PDC, PDT, or SQW; -8.0 to +8.0 Vdc (50Ω).
	DELA	Sets pulse delay relative to sync output.	PDC or PAM; 0.0 ns to 2000 s.
	FREQ	Sets frequency of square wave	SQW only; 0.001 Hz to 10e6 Hz.
	GALV	Sets external gate level.	PDC, PDT, SQW, or PAM; -10.0 Vdc to +10.0 Vdc.

Table A-2. Model 1391 MATE CIIL Commands (Continued)

Type	CIIL Command	Description	Limits
Modifiers (continued)	GASC	Selects either internal or external gate source.	PDC, PDT, SQW, or PAM; INT or EXT.
	GSTA	Selects the external gate start slope.	PDC, PDT, SQW, or PAM. POS or NEG; must be opposite of GSTO.
	GSTO	Selects the external gate stop slope.	PDC, PDT, SQW, or PAM. POS or NEG; must be opposite of GSTA.
	MDSC	Selects the PAM modulation source: internal or external.	PAM only; EXT only.
	PERI	Sets period of single pulse or square.wave.	PDC or SQW; 10e-9 to 1000 s.
	PLWD	Sets pulse width for single and double pulse and PAM.	PDC, PDT, or PAM; 10e-9 to 2000 s.
	PRFR	Sets pulse repetition rate for single and double pulses and PAM.	PDC, PDT, or PAM; 0.001 to 50e6 Hz (25e6 Hz for double).
	RISE	Set the rise time (10% to 90%) of the leading transitions.	PDC, PDT, SQW, or PAM; 5e-9 to 50e-6 s.
	FALL	Set the fall time (10% to 90%) of the trailing transitions.	PDC, PDT, SQW, or PAM; 5e-9 to 50e-6 s.
	SPCG	Set delay between two pulses in the double pulse mode.	PDT only; 20e-9 to 2000 s.
	TIMP	Sets Pulse Generator output impedance.	PDC, PDT, SQW, or PAM; 50Ω only.
	TRFR	Sets internal triggering frequency.	PDC, PDT, SQW, or PAM; 20e-9 to 2000 s.
	TRLV	Sets external trigger level.	PDC, PDT, SQW, or PAM; +10.0 to -10.0 Vdc.
	TRSC	Selects internal or external triggering source.	PDC, PDT, SQW, or PAM; INT or EXT.
	TRSL	Selects external trigger slope.	PDC, PDT, SQW, or PAM; POS or NEG.
	VLPK	Sets amplitude peak value.	PDC, PDT, or SQW; 75e-3 to 8.0 Vpk
	VLPP	Sets square wave amplitude peak to peak value.	SQW only; 150e-3 to 16.0 Vpp.
	VRMS	Sets square wave RMS amplitude.	SQW only; 75e-3 to 8.0 Vrms.

NOTE

See Figure A-1 at the rear of this section for MATE syntax diagrams.

A.5. USING THE PULSE GENERATOR IN THE MATE SYSTEM

A.5.1 Power Up Settings

At power up the Pulse Generator defaults to the following conditions:

Output Frequency:	1 MHz.
Waveform:	single pulse; 250 ns width.
Amplitude:	upper +0.5V.
	lower -0.5V.
Mode:	Continuous.
Output:	Off.

To close the output relay, send the CIIL command string:

`CLS<b>:CH0<cr,lf>`

A.5.2 Using CNF (Confidence) Op Code

Use `CNF` (confidence) to test overall Model 1391 MATE operation by programming predetermined module set-ups and verifying the instrument provides the expected output. At the completion of the confidence test, the unit resets to the power-on condition. Use `STA` (status) to verify the Model 1391 MATE has passed the confidence test. To initiate the confidence test, send the command: `CNF<cr,lf>`. See Appendix D for detailed information on the `*TST` self test which is run following this command.

A.5.3 Using IST (Instrument Self Test) Op Code

Use `IST` (instrument self test) to activate the built in test (BIT) to functionally check the module. During the test the instrument uses its own DVM, counter, trigger generator, and VXIbus system clock to evaluate the module. The diagnostics will isolate failures, if they occur, to the module. If a failure is reported, further diagnostics, not necessarily supported in CIIL can be run on a module level to assist in troubleshooting. Use `STA` (status) to verify the unit has passed the self test. To initiate the instrument self test, send the command: `IST<cr,lf>`. See Appendix D for detailed information on the `*TST` self test which is run following this command.

A.5.4 Using STA (Status) Op Code

Send `STA` (status) after a confidence test (`CNF`), internal self-test (`IST`), or setup command (`FNC` transmission). The `STA` command causes the Model 1391 MATE to return one of two valid responses.

`"F07PLG00:<ASCII message><cr,lf>"` indicates a failure was detected during the confidence test, or an error was detected in the information received in the instrument setup command.

`"<b><cr,lf>"` indicates no failures or errors.

To check the status, send the command: `STA<cr,lf>`.

A.5.5 Using the CLS (Close Output) Op Code

The Pulse Generator initializes with the output relay open. Send the `CLS` command string to close the output relay to obtain an output. Send the command string:

`CLS<b>:CH0<cr,lf>`

A.5.6 Using the FNC Op Code

Use the `FNC` command to set up the Pulse Generator. The syntax diagrams, figure A-1, illustrate the `FNC` paths required to set up the generator.

A.5.6.1 Pulse Out Output Amplitude and Timing

Figure 3-4 shows the pulse waveforms and their associated amplitude and timing modifiers.

Values for the voltage peak (`VLPK`) modifier set the peak amplitude for the pulsed dc (`PDC`) and the pulsed dc train (`PDT`) waveforms; the waveform baseline for all waveforms is specified by the dc offset (`DCOF`) value.

Square wave (`SQW`) amplitude can be specified with the modifiers shown; volts-peak-to-peak (`VLPP`) can only be used to specify a value for the square wave peak-to-peak, specifying values for `VLPK` or `VRMS` sets the peak value of the square wave.

Specifying a value for the period (`PERI`) sets the period for all waveforms; the spacing (`SPCG`) value sets the time between the leading edge of the first and second pulses for pulsed dc trains (`PDT`) only.

Specifying a value for the pulse width (`PLWD`) sets the pulse width for pulsed dc and pulsed dc trains only. The transition times for all pulses and the square wave can be set with the rising (`RISE`) and falling (`FALL`) transition times commands.

The pulse repetition frequency (`PRFR`) modifier can be used to specify a value for pulse repetition frequency as an alternative for setting the waveform period.

A.5.6.2 Pulsed DC (PDC) Waveform Programming

Table A-3 shows the modes and controls supported by CIIL for single pulse generation. Refer to the syntax diagram, figure A-1, to find the required command strings for the desired setup.

A.5.6.3 Pulsed DC Train (PDT) Waveform Programming

Table A-4 shows the modes and controls supported by CIIL for double pulse generation. Refer to the syntax diagram, figure A-1, to find the required command strings for the desired setup.

A.5.6.4 Square wave (SQW) Waveform Programming

Table A-5 shows the modes and controls supported by CIIL for square wave generation. Refer to the syntax diagram, figure A-1, to find the required command strings for the desired setup.

A.5.6.5 Triggering

In the triggered mode, the Pulse Generator starts a waveform when it receives a valid trigger. The following describes the trigger commands. The triggered mode cannot be used for square waves.

Specify the non-numeric values (EXT or INT) to select the trigger source (TRSC). EXT (external) selects the module's TRIG IN input BNC connector as the trigger source. INT (internal) selects Model 1391's internal trigger (TRFR) bus as the trigger source.

Specify the non-numeric values to select the trigger slope (TRSL): positive (POS) or negative (NEG).

Specify the numeric value to sets the trigger level (TRLV).

A.5.6.6 Gating

In the gated mode, the Model 1391 MATE produces a waveform as long as the trigger (gate) is active. Figure 3-7 shows the relationship between the gating signal and the Pulse Out.

Specifying either POS (positive) or NEG (negative) sets the gate start slope (GSTA) or the gate stop slope (GSTO). These values set the trigger slope on which the waveform starts and stops.

The gate start slope (GSTA) and gate stop slope (GSTO) values can never be both positive or both negative. Specifying one value without the other causes the Model 1391 MATE to automatically switch, if necessary, the remaining unspecified modifier value to the opposite slope. Specifying equal values results in an error message and termination of the command string. See Table A-6 at the rear of this appendix for error messages.

A.5.6.7 Burst

In the Burst mode, the Model 1391 MATE produces a user programmed number of waveforms each time the trigger is valid. The burst (BURS) value sets the number of waveform periods generated for each trigger.

A.5.6.8 Output Impedance

The test equipment impedance value (TIMP) selects the module's output impedance. The only allowable value for the Model 1391 is 50Ω.

A.6 SYNTAX EXAMPLES

Follow the syntax diagram, figure A-1, to help understand the CIIL command strings given in the examples.

A.6.1 Pulsed DC (PDC) Continuous

This CIIL command string sets the Pulse Generator output for continuous 10 ns, 4V pulses with a delay of 20 ns. The pulse repetition frequency is 1MHz, and the dc offset is 1V. Output impedance is set to 50Ω. The transition times will be at their default value of 5 ns.

```
FNC<b>PDC<b>:CH0<b>SET<b>VLPK<b>4<b>
SET<b>PLWD<b>10e-9<b>SET<b>PRFR<b>
1e6<b>SET<b>DELA<b>20e-9<b>SET<b>
DCOF<b>1<b>SET<b>TIMP<b>50<cr,lf>
```

A.6.2 Triggered Pulsed DC (PDC)

This CIIL command string sets up the Pulse Generator for triggered 10 ns, 2V pulses. An external source triggers the pulses on the negative slope at +3V. The waveform is offset +2V. The output impedance is 50Ω. The leading edge is 10 ns, and the trailing edge is minimum (5 ns).

```
FNC<b>PDC<b>:CH0<b>SET<b>VLPK<b>2<b>
SET<b>PLWD<b>10e-9<b>SET<b>TRSC<b>
EXT<b>SET<b>TRSL<b>NEG<b>SET<b>TRLV<b>3<b>
SET<b>DCOF<b>2<b>SET<b>TIMP<b>50<b>
SET<b>RISE<b>10e-9<b>SRN<b>FALL<b>
5e-9<cr,lf>
```

A.6.3 Pulsed DC Train (PDT) Burst

This CIIL command string sets up the Pulse Generator for a triggered burst of 50, 10 ns, 5V double pulses at 1 MHz and 20 ns spacing between the double pulses. The external source triggers the module on the positive slope (default slope) at +2V. The pulses are offset +1V. The output impedance is 50 Ω (default impedance).

```
FNC<b>PDT<b>:CH0<b>SET<b>VLPK<b>5<b>
SET<b>PRFR<b>1e6<b>SET<b>BURS<b>50<b>
SET<b>TRSC<b>EXT<b>SET<b>TRLV<b>2<b>
SET<b>PLWD<b>10e-9<b>SET<b>SPCG<b>
20e9<b>P1POS<b>P2POS<b>SET<b>DCOF<b>
1<cr,lf>
```

Table A-3. Available Pulsed DC Waveform Modes and Controls

Supported Modes	Trigger Controls	Gate Controls	Burst Controls
Continuous	Trigger Freq (TRFR)	Gate Start Slope (GSTA)	Burst Count (BURS)
Triggered	Trigger Slope (TRSL)	Gate Stop Slope (GSTO)	Trigger Freq (TRFR)
Burst	Trigger Level (TRLV)	Gate Level (GALV)	Trigger Slope (TRSL)
Gated	Trigger Source (TRSC)	Trigger Freq (TRFR)	Trigger Level (TRLV)
			Trigger Source (TRSC)

Table A-4. Available Pulsed DC Train Waveform Modes and Controls

Supported Modes	Trigger Controls	Gate Controls	Burst Controls
Continuous	Trigger Freq (TRFR)	Gate Start Slope (GSTA)	Burst Count (BURS)
Triggered	Trigger Slope (TRSL)	Gate Stop Slope (GSTO)	Trigger Freq (TRFR)
Burst	Trigger Level (TRLV)	Gate Level (GALV)	Trigger Slope (TRSL)
Gated	Trigger Source (TRSC)	Trigger Freq (TRFR)	Trigger Level (TRLV)
			Trigger Source (TRSC)

Spacing between double pulses must be specified with the SPCG modifier, its attendant value and the modifiers "P1POS<b>P2POS". These modifiers cannot be used in command strings that control Pulsed DC (PDC) or Square wave (SQW) outputs.

Table A-5. Available Square wave Modes and Controls

Supported Modes	Trigger Controls	Gate Controls	Burst Controls
Continuous	Trigger Freq (TRFR)	Gate Start Slope (GSTA)	Burst Count (BURS)
Triggered	Trigger Slope (TRSL)	Gate Stop Slope (GSTO)	Trigger Freq (TRFR)
Burst	Trigger Level (TRLV)	Gate Level (GALV)	Trigger Slope (TRSL)
Gated	Trigger Source (TRSC)	Trigger Freq (TRFR)	Trigger Level (TRLV)
			Trigger Source (TRSC)

The trigger controls are used for the burst mode only.

A.6.4 Continuous Square Wave (SQW)

This example sets up the Pulse Generator for continuous 2 Volt peak-to-peak, 2 MHz square waves. The defaults for dc offset and output impedance are used.

```
FNC<b>SQW<b>:CH0<b>VLPP<b>2<b>SET<b>
FREQ<b>2e6<cr,lf>
```

A.6.5 Gated Pulse DC Train

In this example the Pulse Generator produces gated 10 ns, 5V double pulses at a 1 MHz rate. The space between the double pulses is 20 ns. An external source gates the Pulse Generator on the negative slope and stops on the positive slope. Threshold level 1V. DC offset and output impedance are the default values.

```
FNC<b>PDT<b>:CH0<b>SET<b>VLPK<b>5<b>
SET<b>PERI<b>1e-6<b>SET<b>GASC<b>
EXT<b>SET<b>GSTA<b>NEG<b>SET<b>GSTO<b>
POS<b>SET<b>GALV<b>1<b>SET<b>PLWD<b>
10e-9<b>SET<b>SPCG<b>20e-9<b>P1POS
<b>P2POS<cr,lf>
```

A.7 SELECTING PULSE AMPLITUDE MODULATION (PAM)

The Pulse Generator can be pulse amplitude modulated from an external source. To externally modulate the Pulse Generator, apply a modulating signal not greater than 20 kHz to the PAM IN input. The CAMP command sets the pulse amplitude, and the CFRQ sets the pulse carrier frequency.

A.7.1 PAM Example

In this example, the Pulse Generator (at address 3) produces a 2MHz, 3Vp-p, 300ns pulse. The external signal (MATE compatible Function Generator at address 2) modulates the Pulse Generator with a 3Vp-p, 6 kHz triangle wave.

Write @ secondary address 2:

```
"FNC<b>TRI<b>:CH0<b>SET<b>VLPP<b>3<b>
SET<b>FREQ<b>6E3<cr><lf>"
```

Write @ secondary address 3:

```
"FNC<b>PAM<b>:CH0<b>SET<b>CAMP<b>3<b>SET
<b>CFRQ<b>2E6<b>SET<b>MDSC<b>INT<b>SET
<b>PLWD<b>300E-9<cr><lf>"
```

A.8 PULSE GENERATOR ERROR MESSAGES

Table A-6 lists all the possible Pulse/Timing Generator error messages that could occur during normal operation. Each message contains in quotes a brief explanation of the messages meaning. One of two ASCII strings ("`F07PLG00(MOD):`" or "`F07PLG00(DEV):`") precedes each error message.

When the term <ASCII> appears in the error messages listed below, it represents any continuous string of ASCII characters except space, tab, LF, CR. . This string can represent valid nouns, modifiers, or data, as well as misspelled or garbage strings. If the string syntax is valid, then the string could be out of order or there could be some other reason the string was not accepted.

Table A-8. Error Messages

Error Message	Comments
"<ASCII> not allowed"	This ASCII string cannot be used as entered.
"<ASCII> missing"	A mandatory modifier is missing in the command string. For example, the PDC command requires a VLPK modifer.
"<ASCII> limit error"	The value sent exceeds the modifier's limit.
"GSTA/GSTO slope error"	Both the gate start and stop slopes were set to the same value.
"channel number error"	Only channel 0 can be used with the Pulse Generator, because it has only one programmable output.
"setting missing from FNC command"	The command string was correct up to the mandatory SET modifier which is missing.
"INT/EXT not allowed with <ASCII>"	The modifier is correct, but INT or EXT are not valid modifier values.
"POS/NEG not allowed with <ASCII>"	The modifier is correct, but POS or NEG are not valid modifier values.
"numeric value not allowed with <ASCII>"	The modifier sent does not accept numeric values. TRSC and GASC are examples of modifiers that do not take numeric values.
"value needed with <ASCII>"	The modified noted in the ASCII string requires a value.
"command terminated before complete"	"FNC PDC<cr><lf>" causes this error message. The command string is correct up to the terminating characters. But, the entire command string is incomplete.
"<ASCII>"	This message represents any Pulse Generator dependent error message.
"TRSL/TRLV only allowed with TRSC EXT"	Trigger slope and trigger level values are only valid when set up for an external trigger source.
"GSTA/GSTO/GALV only allowed with GASC EXT"	Gate slope and level only valid when using an external gate source.
"BURS not allowed with GASC"	Burst mode uses TRSC (internal or external trigger source).

Format of common commands

OPN<b>:CH0<CR/LF>
CLS<b>:CH0<CR/LF>

RST<b> ⟨ PDC / PDT / SQW / PAM ⟩ <b>:CH0<CR/LF>

IST<CR/LF>
CNF<CR/LF>
STA<CR/LF>

Modifiers Supported in each Function (noun)

	PAM	PDC	PDT	SQW
BURS	x	x	x	x
CAMP	x			
CFRQ	x			
DCOF		x	x	x
DELA	x	x		
FALL	x	x	x	x
FREQ				x
GALV	x	x	x	x
GASC	x	x	x	x
GSTA	x	x	x	x
GSTO	x	x	x	x
MDSC	x			
PERI		x		x
PLWD	x	x	x	
PRFR	x	x	x	
RISE	x	x	x	x
SPCG			x	
TIMP	x	x	x	x
TRFR	x	x	x	x
TRLV	x	x	x	x
TRSC	x	x	x	x
TRSL	x	x	x	x
VLPK		x	x	x
VLPP				x
VRMS				x

Figure A-1. Pulse Generator CIIL Syntax Diagrams.

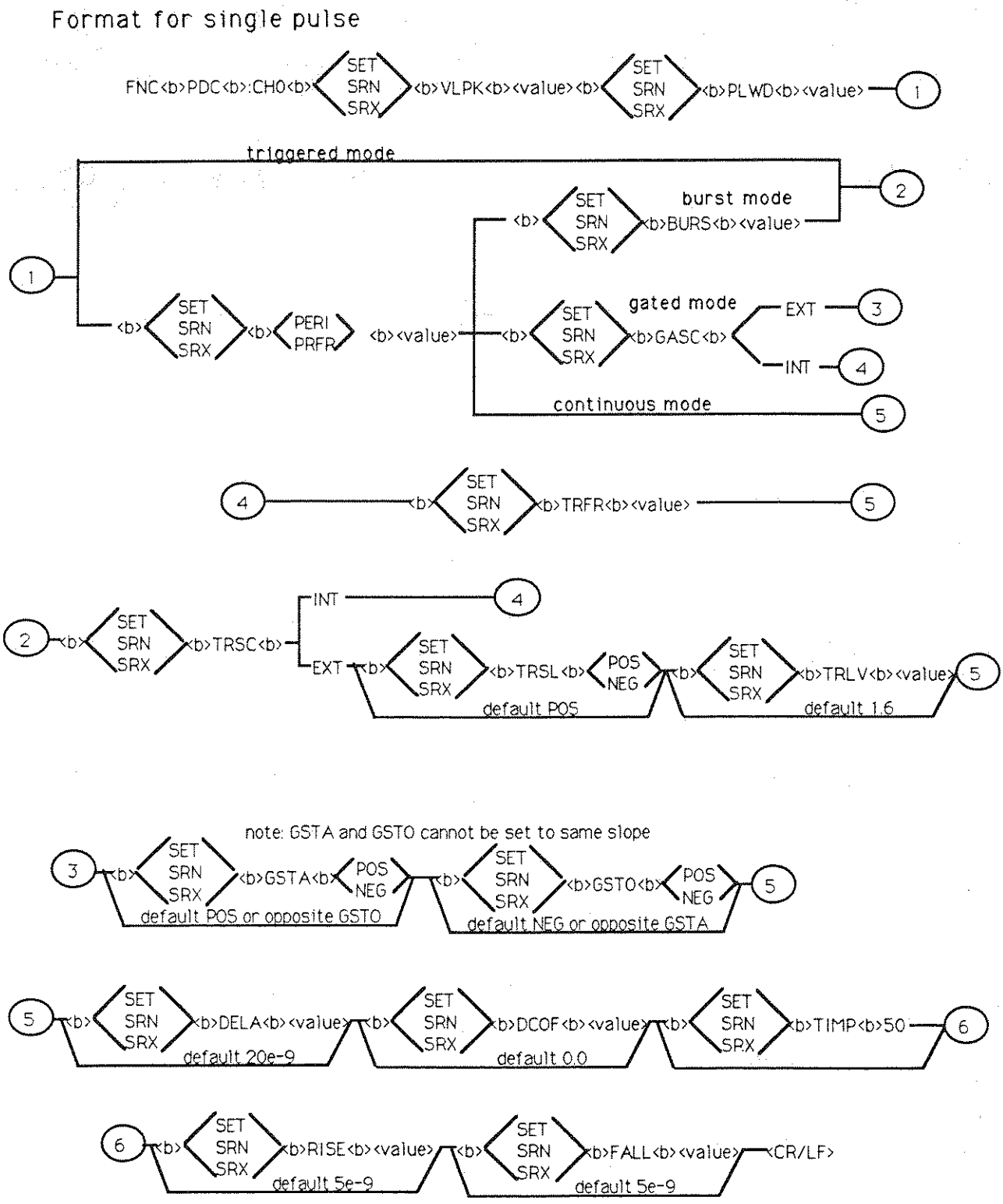

Figure A-1. Pulse Generator CIIL Syntax Diagrams (Continued).

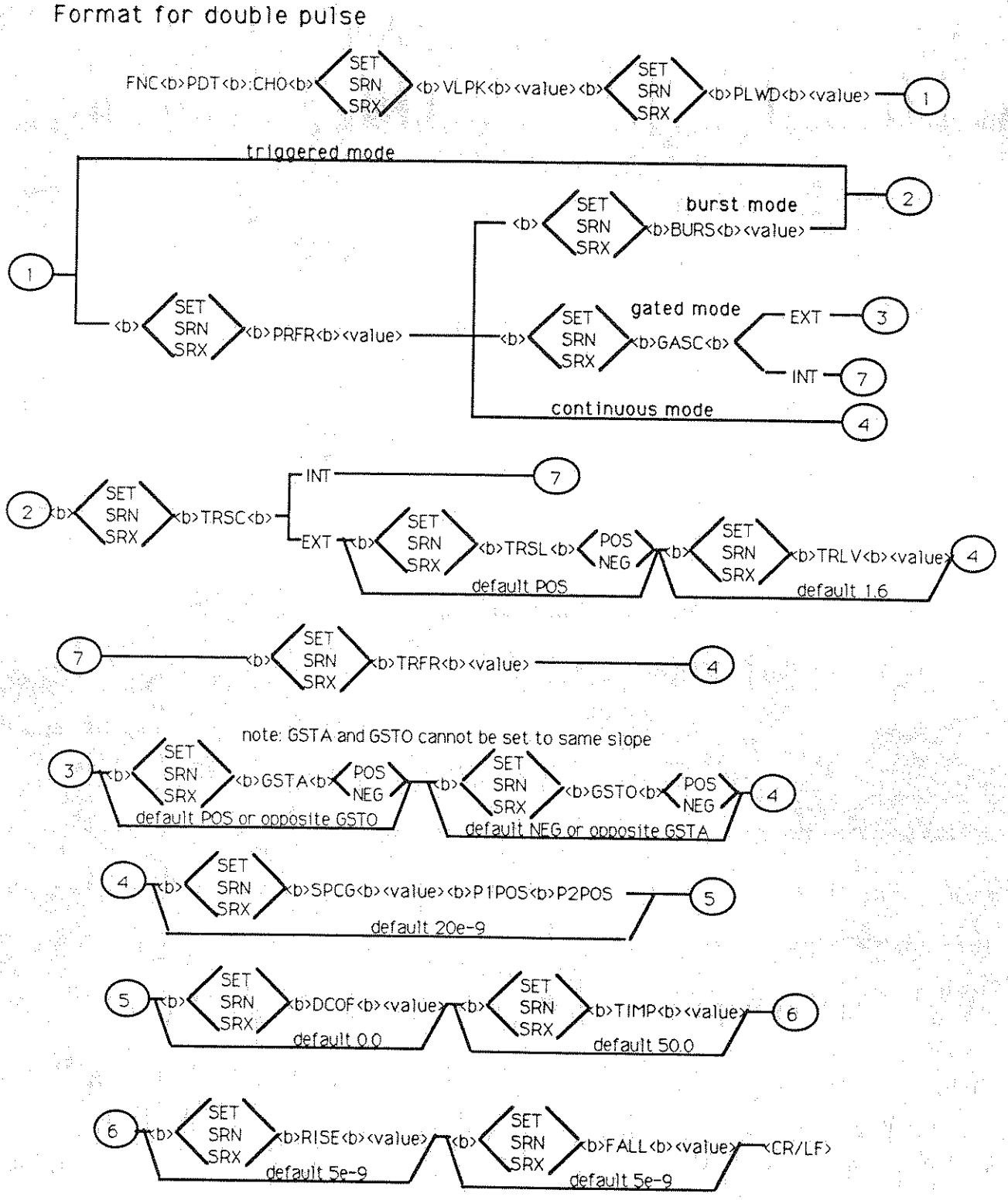

Figure A-1. Pulse Generator CIIL Syntax Diagrams (Continued).

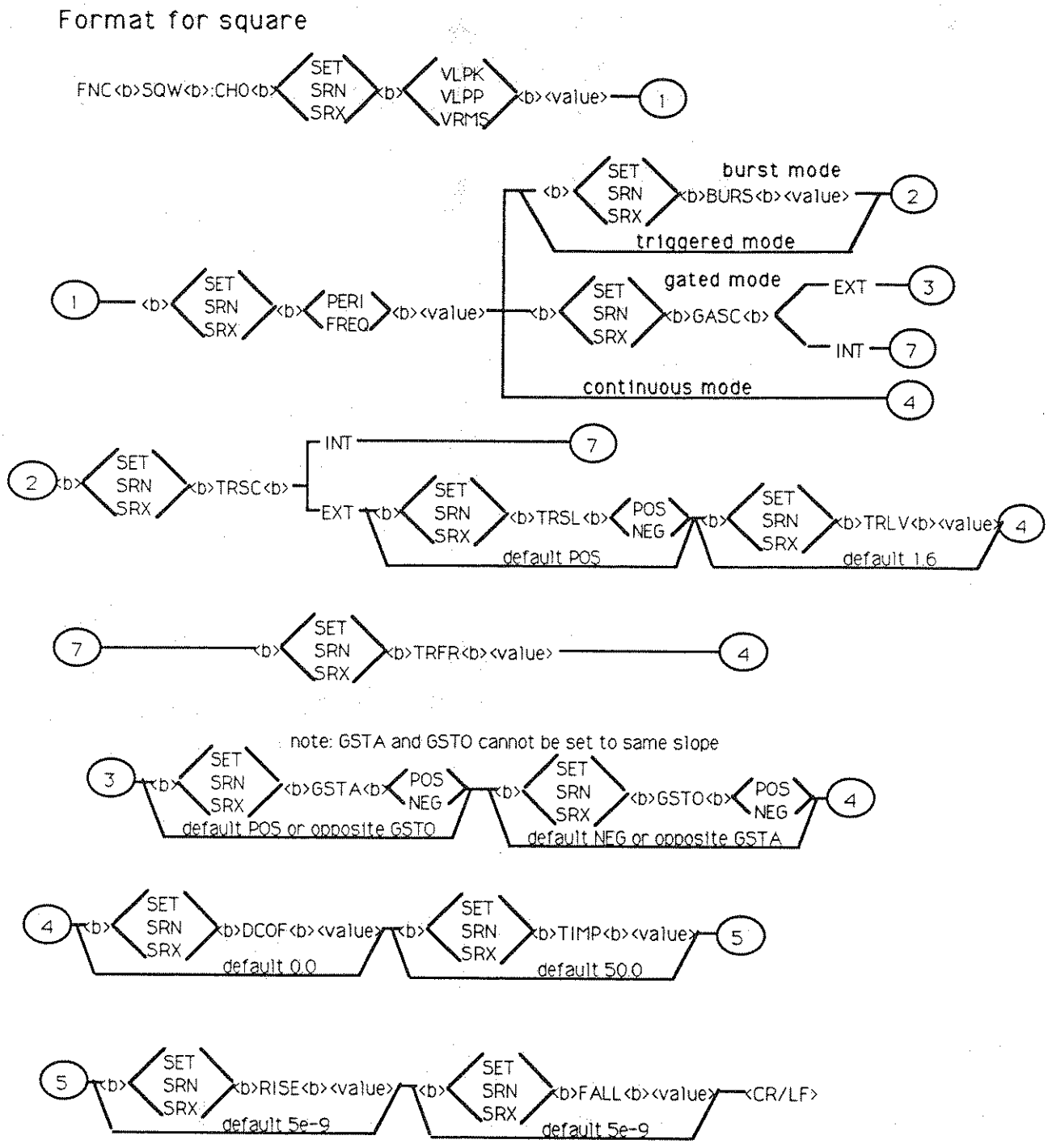

Figure A-1. Pulse Generator CIIL Syntax Diagrams (Continued).

Format for pulse amplitude modulation

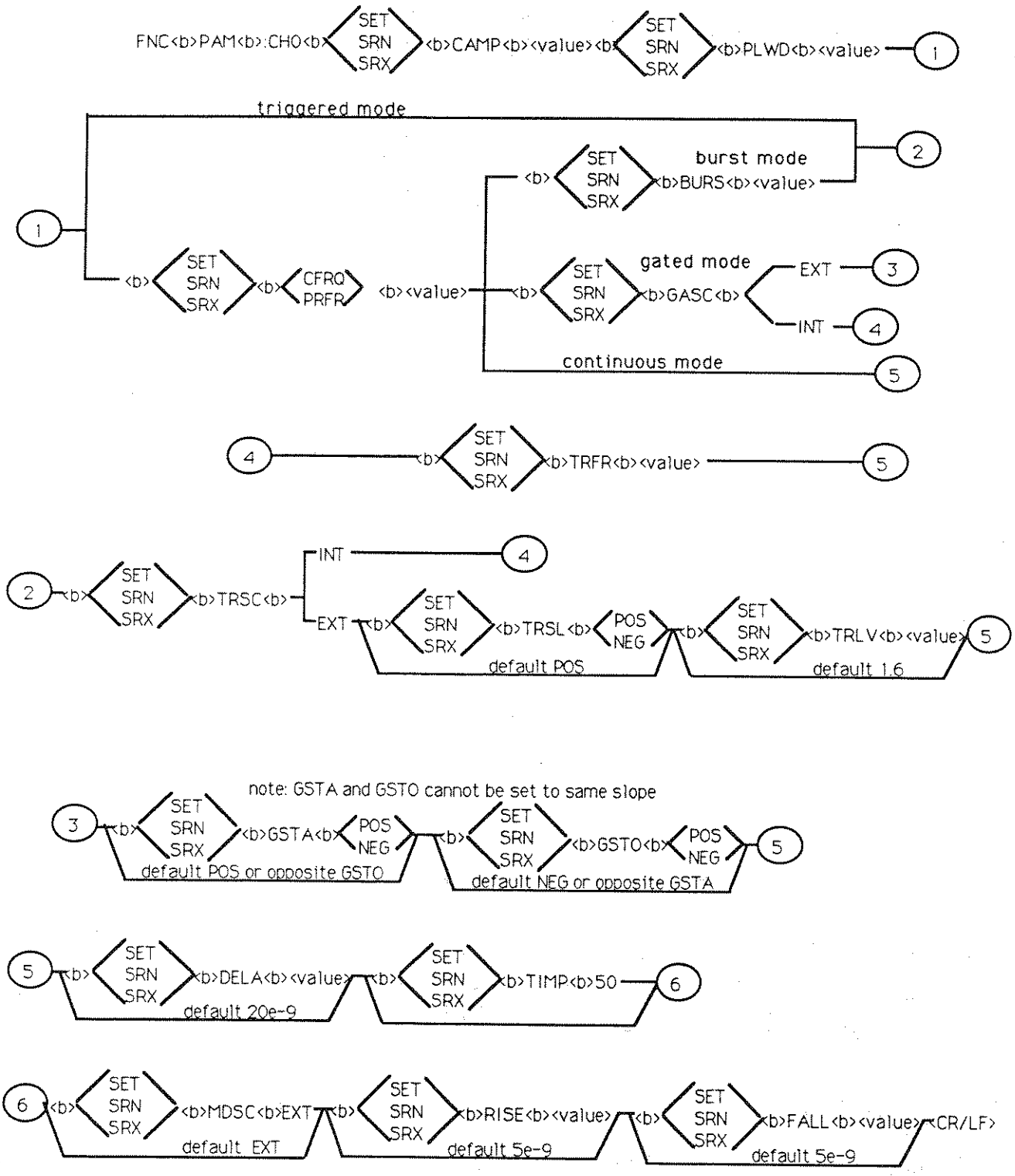

Figure A-1. Pulse Generator CIIL Syntax Diagrams (Continued).

B.1 INTRODUCTION

See the attached fold-out.