OH214

MODEL
360B
VECTOR NETWORK ANALYZER

SYSTEM MAINTENANCE MANUAL

Wiltron

490 JARVIS DRIVE ● MORGAN HILL, CA 95037-2809

P/N: 10410-00116
REVISION: C
PRINTED: FEBRUARY 1994

TABLE OF CONTENTS

Chapter 1
General Information

Table of Contents

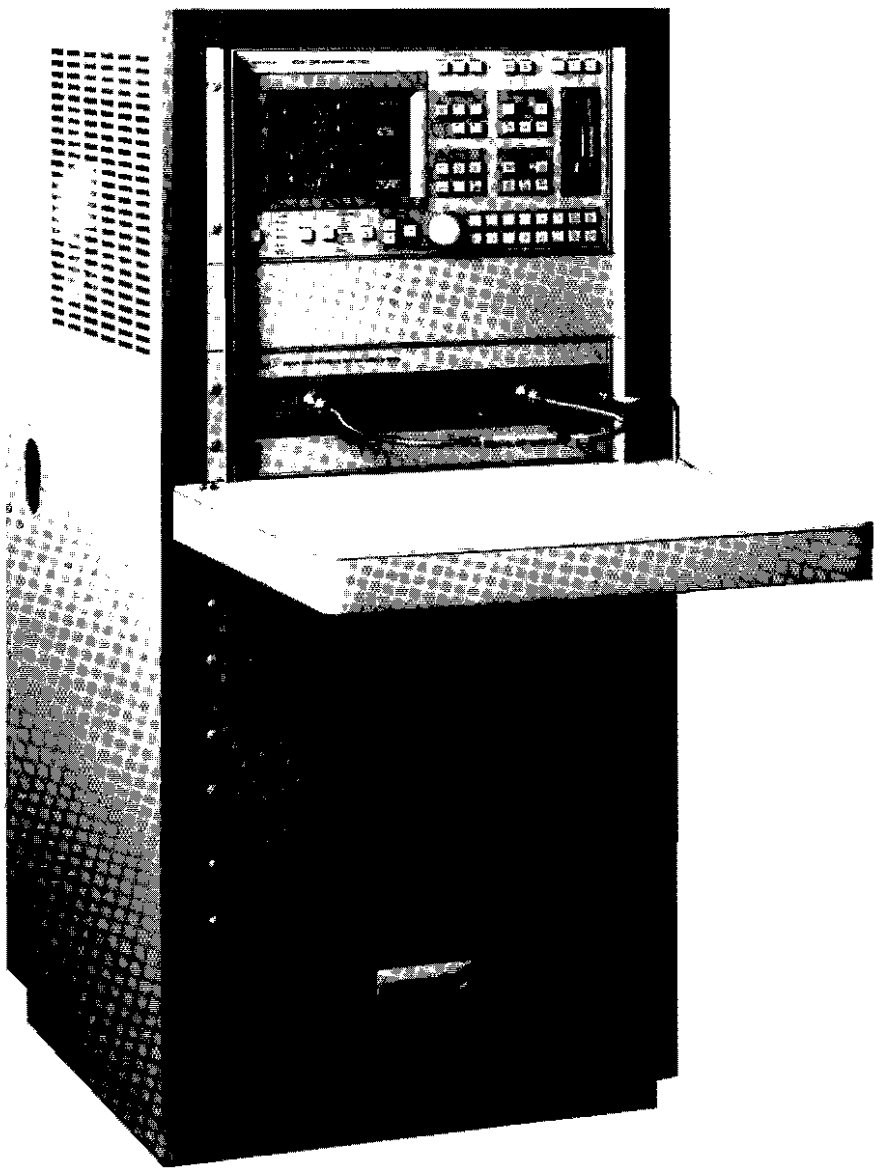


Figure 1-1. *Model 360B Vector Network Analyzer System (Shown installed in Model 360C1 System Console*

Chapter 1
General Information

1-1 SCOPE OF MANUAL

This manual provides general and service information for the Model 360B Vector Network Analyzer (VNA) system (Figure 1-1). (Throughout this manual, the terms *360B VNA* and *360B* will be used interchangeably to refer to the system.) Manual organization is shown in the narrative Table of Contents that precedes this chapter. The information in this manual provides for fault isolation to the assembly level for system instruments. Covered instruments consist of network analyzer, signal (frequency) source, test sets, and 360ACM used with the 3635B mm-wave test set.

1-2 INTRODUCTION

This chapter provides general information about the 360B VNA system. It also provides replaceable-assembly information and a listing of recommended test equipment for servicing 360B VNA system instruments.

1-3 IDENTIFICATION NUMBER

All WILTRON instruments are assigned a unique six-digit ID number, such as "701001." This number is affixed to a decal on the rear panel of each unit. In any correspondence with either WILTRON Customer Service or your Anritsu/Wiltron Service Center, please use this number.

NOTE

The system operating software is keyed to the analyzer identification number. For systems having certain option installed, the operating-system will only load on the serial-numbered 360B for which the software is identified.

1-4 RELATED MANUALS

Manuals related to the operation and maintenance of the 360B VNA system are listed in Table 1-1. This table also lists the 360B VNA optional equipment manuals.

Table 1-1. List of Related Manuals

Title	Description	Part Number
Model 360B Vector Network Analyzer Operating Manual	Provides operating information for the 360B VNA.	10410-00110
Model 360B Vector Network Analyzer Getting Started Guide	Provides a tutorial for quickly getting started making measurements with the 360 VNA system. Manual is bound with the 360B OM, but can be ordered separately.	10410-00111
Model 360B Vector Network Analyzer GPIB Programming Manual	Provides programming information for the 360B GPIB interface.	10410-00113
360B GPIB Quick Reference Guide	Alphabetically list and briefly describes all 360B GPIB commands. Provides references to fulier command descriptions located in 360B GPIB PM. Manual is bound with the 360B GPIB PM, but can be ordered separately.	10410-00114
Model 36XX Calibration and Verification Kit Operation and Maintenance Manual	Provides operating instructions and maintenance information for the Models 3650, 3651, 3652, 3653, and 3654 Calibration Kits and the Models 3666, 3667, 3668, and 3669 Verification Kits.	10100-00024

1-5 SERVICE INFORMATION

Module Exchange Program. WILTRON Customer Service and the Anritsu/Wiltron Service Centers provides an module exchange program that includes the parts and assemblies listed in Table 1-2.

Table 1-2. Exchangeable Subassemblies, 1 of 6

WILTRON Part Number	Description
	360 Vector Network Analyzer
D14364-3	A1 LO 1 Phase Lock PCB Assembly
D14351-3	A2 LO 2 Phase Lock PCB Assembly
D14366-3	A3 Cal/3rd L.O. PCB Assembly
D14352-3	A4 A/D Converter PCB Assembly
D34355-3	A5 10 MHz Reference PCB Assembly
D34605-3	A6 Source Lock PCB Assembly
D14353-4	A7 Synchronous Detector A PCB Assembly
D14353-5	A8 Synchronous Detector B PCB Assembly
D14353-6	A9 Synchronous Detector R PCB Assembly
D34624-3	A10 Blanking/Synchronous PCB Assembly
D37995-3	A11 I/O VGA Processor PCB Assembly
D34520-3	A12 Main 2 Processor PCB Assembly
D38057-3	A13 Main 1 Processor PCB Assembly
D34680-3	A14 Power Supply Control PCB Assembly
D36965-3	A15 Power Supply Convertor PCB Assembly
D37574-3	A16 Test Set I/O PCB Assembly
D34656-3	A18 Power Supply Motherboard
D38112	Front Panel Assembly 360B, includes disk drive
D36993	Color Display VGA Assembly

Table 1-2. Exchangeable Subassemblies, 2 of 6

WILTRON Part Number	Description
	36xxA Series Test Sets
D30701-4	A1T IF Amplifier, Channel B PCB Assembly
D34519-3	A2T IF Amplifier, Reference Channel PCB Assembly
D30701-5	A3T IF Amplifier, Channel A PCB Assembly
D30704-3	A4T LO 2 PCB Assembly
D34603-3	A5T LO 1 PCB Assembly
D34760-3	A5T Power Distribution PCB Assembly, 3635B
D37611-3	A6T Digital Interface PCB Assembly
D34636-3	A7T Attenuator Driver PCB Assembly
D35558-3	A27T Amplifier/Switch Driver PCB Assembly
	3600 RF Components, 20 GHz and below
D21852	A8T Buffer Amplifier Assembly, Channel B, 3610A, 3620A
D21851	A10T Buffer Amplifier Assembly, Channel A, 3610A, 3620A
D15320-1	A12T Power Amplifier Assembly
B19820-1	A13T Transfer Switch, with cable, 3610A, 3620A
D20363	A14T/A15T Coupler, 3610A, 3620A
C21586	A18T/A19T Bias Tee, Female - Female
C21587	A18T/A19T Bias Tee, Male - Female
4412K	A20T/A21T/A22T Step Attenuator, 70 dB, 20 GHz
D34511	A24T Source Lock / Reference Select Assembly
D17900	A25T RF Splitter
	3600 RF Components, 40 GHz and below
D17929	A8T Buffer Amplifier Assembly, Channel B, 3611A, 3621A, 3630A
D21854	A8T Buffer Amplifier Assembly Channel B, 3611A, 3621A, 3630A
D17928	A10T Buffer Amplifier Assembly, Channel A, 3611A, 3621A, 3630A

Table 1-2. Exchangeable Subassemblies, 3 of 6

WILTRON Part Number	Description
D15320-1	A12T Power Amplifier Assembly
B19821-1	A13T Transfer Switch, B19821 with cable, 3611A, 3621A
D15825	A14T/A15T Coupler, 3611A, 3621A
C21586	A18T/A19T Bias Tee, Female - Female
C21587	A18T/A19T Bias Tee, Male - Female
4612K	A20T/A21T/A22T Step Attenuator, 70 dB, 40 GHz
D34511	A24T Source Lock / Reference Select Assembly
	3600 RF Components, 60 GHz
D21856	A8T Buffer Amplifier Assembly. Channel B
C21421	A8T Buffer Amplifier Assembly, Channel B
D21855	A10T Buffer Amplifier Assembly, Channel A
C21420	A10T Buffer Amplifier Assembly, Channel A
D21405-1	A12T Power Amplifier / Multiplier Assembly, D21405 with cable
D21350-1	A13T Transfer Switch, D21350 with cable
D20600	A14T/A15T Coupler, 60 GHz
D22811	A14T/A15T Coupler 62.5 GHz
V250	A18T/A19T Bias Tee, 60 GHz
4712V	A20T/A21T/A22T Step Attenuator, 70 dB, 60 GHz
D34511	A24T Source Lock / Reference Select Assembly
D21395	A25T RF Splitter
D21360	A28T/A29T SPDT/Splitter
C23356	A30T Channel B Tripler Assembly, 60 GHz, Includes 1000-37 Isolator, 1040-15 Tripler, D21319 Mux coupler, C21372 Amplifier and C21382 High Pass Filter. This must be replaced as an entire assembly.

Table 1-2. Exchangeable Subassemblies, 4 of 6

WILTRON Part Number	Description
C23361	A30T Channel B Tripler Assembly, 62.5 GHz. Includes 1000-37 Isolator, 1040-15 Tripler, D21319 Mux coupler, C21372 Amplifier and C21382 High Pass Filter. This must be replaced as an entire assembly.
C23355	A31T Channel A Tripler Assembly, 60 GHz. Includes 1000-37 Isolator, 1040-15 Tripler, D21319 Mux coupler, C21372 Amplifier and C21382 High Pass Filter. This must be replaced as an entire assembly.
C23360	A31T Channel A Tripler Assembly, 62.5 GHz. Includes 1000-37 Isolator, 1040-15 Tripler, D21319 Mux coupler, C21372 Amplifier and C21382 High Pass Filter. This must be replaced as an entire assembly.
	3600 RF Components, 65 GHz
D39098-5	A27T Amplifier/Switch Driver PCB Assembly
C26220	A31T Channel A Tripler Assembly, 65 GHz. Includes 1040-17 Tripler, D26224 Mux coupler, C25593 Amplifier and other components. This must be replaced as an entire assembly.
C26221	A30T Channel A Tripler Assembly, 65 GHz. Includes 1040-17 Tripler, D26225 Mux coupler, C25593 Amplifier and other components. This must be replaced as an entire assembly.
ND26237	A25T RF Splitter
D26219	A12T Power Amplifier / Multiplier Assembly
D26222	A10T Buffer Amplifier Assembly, Channel A
D26223	A8T Buffer Amplifier Assembly. Channel B
ND26180	A14T/A15T Coupler 65 GHz
ND26179	A20T/A21T/A22T Step Attenuator, 70 dB, 65 GHz
ND26181	A18T/A19T Bias Tee, 65 GHz
B39096*	Cable Assembly, Auxiliary Power
551-1095*	Auxiliary Power Connector (rear panel)
40-56*	Auxiliary Power Supply (USA)
40-57*	Auxiliary Power Supply (UK)
40-58*	Auxiliary Power Supply (Europe)

* These components are not on the module exchange program; however, they may be ordered as standard replacement parts.

Table 1-2. Exchangeable Subassemblies, 5 of 6

WILTRON Part Number	Description
	3635B Millimeter VNA RF Components
1091-87	A11T Power Splitter
C21660	A20T RF Input Amplifier, 11–20 GHz
D23385	A21T/A22T LO Amplifier, 8–15 GHz
D21925-1	A9T Transfer Switch
D22447	A10T Channel A Buffer/Amplifier Assembly
D20876	A8T Channel B Buffer/Amplifier Assembly
	360 ACM
D37719-3	A100 PCB Assembly
B37862	15 Volt PSU Assembly
B37862	12 Volt PSU Assembly
	360SS Series System Source
D32101-3	A1 GPIB PCB Assembly
ND34470	A4 ALC PCB and Coupler Assembly, 360SS47
ND35979	A4 ALC PCB and Coupler Assembly, 360SS69
D32105-3	A5 Frequency Instruction PCB Assembly
D34710-11	A10 FM PCB Assembly
D32113-3	A13 Power Supply PCB Assembly
	360SS RF Components
60-102	Frequency Doubler Amplifier, 360SS69
C8090-5	Down Converter Assembly, cabled D9157A
D13355	PIN Switch Assembly, 360SS69
D13611	DPDT PIN Switch, 8-26.5 GHz
D18696	PIN Switch Assembly, 360SS47
ND31355	13.25 to 20 GHz Amplifier, 360SS69
ND19075	18 to 26.5 GHz Amplifier, 360SS69

Table 1-2. Exchangeable Subassemblies, 6 of 6

WILTRON Part Number	Description
ND35918	2 to 8 GHz Oscillator Assembly, 360SS47
ND35919	2 to 8 GHz Oscillator Assembly, 360SS69
ND35934	8 to 12.4 GHz Oscillator Assembly, 360SS47
ND35935	8 to 12.4 GHz Oscillator Assembly, 360SS69
ND35950	12.4 to 20 GHz Oscillator Assembly, 360SS47
ND35951	12.4 to 18 GHz Oscillator Assembly, 360SS69
ND35958	18 to 26.5 GHz Oscillator Assembly, 360SS69
C20812	Output Connector Assembly

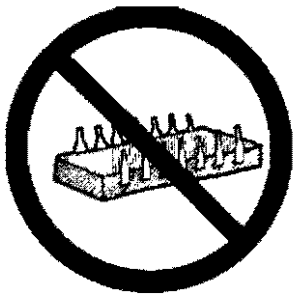
Static Handling

Figure 1-2 provides procedures that should be followed when handling static sensitive parts.

CAUTION

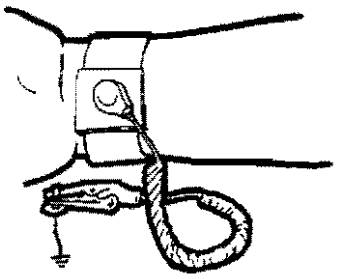
WILTRON highly recommends that you use a grounded wrist strap when handling 360B VNA System PCBs and components. The 360B VNA system contains parts that can be damaged by static electricity.

1. Do not touch exposed contacts on any static sensitive component.

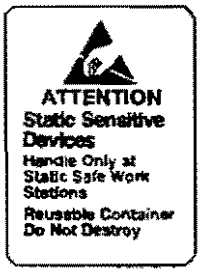


2. Do not slide static sensitive component across any surface.

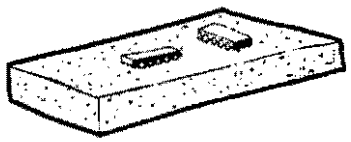
3. Do not handle static sensitive components in areas where the floor or work surface covering is capable of generating a static charge.



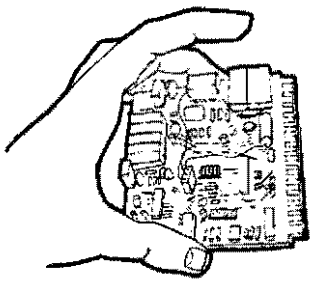
4. Wear a static-discharge wristband when working with static sensitive components.



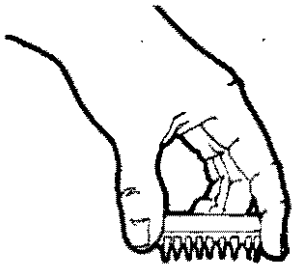
5. Label all static sensitive devices.



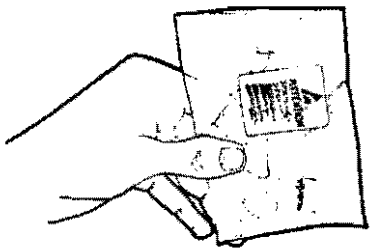
6. Keep component leads shorted together whenever possible.



7. Handle PCBs only by their edges. Do not handle by the edge connectors.



8. Lift & handle solid state devices by their bodies – never by their leads.



9. Transport and store PCBs and other static sensitive devices in static-shielded containers.

10. ADDITIONAL PRECAUTIONS:

- Keep workspaces clean and free of any objects capable of holding or storing a static charge.
- Connect soldering tools to an earth ground.
- Use only special anti-static suction or wick-type desoldering tools.

Figure 1-2. *Static Handling Procedures*

1-6 RECOMMENDED TEST EQUIPMENT

Table 1-3 lists the recommended test equipment for maintaining and servicing the 360B VNA system.

Table 1-3. *Recommended Test Equipment (1 of 2)*

Instrument	Critical Specification	Recommended Manufacturer/Model
Spectrum Analyzer, with Diplexer and External Mixers	*Frequency:* 0.01 to 60 GHz *Resolution:* 10 Hz	Tektronix, Inc. Model 494P,with External Mixers: WM 490K (18 to 26.5 GHz) WM 490A (26.5 to 40 GHz) WM 490U (40 to 60 GHz) WM 490V (50 to 60 GHz) Diplexer PN: 015-0385-00
Power Meter, with Power Sensors	*Range:* –30 to +20 dBm (1µW to 100 mW) *Other:* GPIB-controllable	Hewlett-Packard Model 437B, with Option 22 (GPIB), and Power Sensors: HP 8485A (0.01 to 26.5 GHz) HP 8487A (0.05 to 50 GHz)
Digital Multimeter	*Resolution:* 4-1/2 digits *DC Accuracy:* 0.002% +2 counts *DC Input Z:* 10 MΩ *AC Accuracy:* 0.07% +100 counts (to 20 kHz) *AC Input Z:* 1 MΩ	John Fluke, Inc. Model 8840A, with Option 8840A-09 (True RMS AC)
Frequency Counter, with External Mixers	*Range:* 0.01 to 60 GHz *Input Z:* 50Ω *Resolution:* 1 Hz *Other:* External Time Base Input	EIP Microwave, Inc. Model 578A, with External Mixers: Option 91 (26.5 to 40 GHz) Option 92 (40 to 60 GHz) Option 93 (60 to 90 GHz)
Oscilloscope	*Bandwidth:* DC to 150 MHz *Vertical Sensitivity:* 2 mV/ division *Horiz Sensitivity:* 50 ns/ division	Tektronix, Inc. Model 2445
Function Generator	*Output Voltage Range:* 300 mV to 10V *Functions:* 200 Hz Sine Wave 100 Hz Square Wave	Hewlett-Packard Model 3325A
Local Oscillator (LO) Test Fixture	N/A	WILTRON T1512 (Figure 1-3)
PCB Extender Card	N/A	WILTRON Part Number: D30709-3

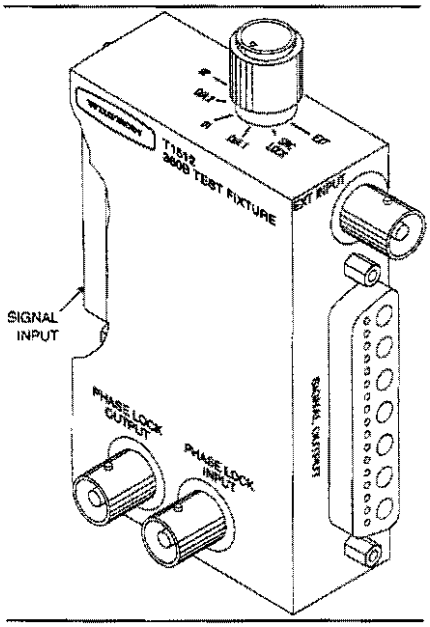


Figure 1-3. *WILTRON T1512 360B Test Fixture*

Table 1-3. Recommended Test Equipment (2 of 2)

Instrument	Critical Specification	Recommended Manufacturer/Model
Test Cables	N/A	WILTRON Part Number: ND34060
Measurement Calibration Kit	Kit contains high-precision opens, shorts, broadband loads, and sliding load	WILTRON Company Model 3650, 3651, 3652, 3653 or 3654/3654B* (Included with Model 360B VNA System)
Measurement Calibration Kit	Q-, U-, V-, or W-band waveguide components (For use with Model 3635B Test Set, only)	WILTRON Company 3655Q, 3655U, 3655V, or 3655W, depending on Model 364XB-X Module being used. (Included with Model 360B VNA System)
Microwave Cable	Frequency: 18, 40, 60, or 65 GHz, depending on connector type	WILTRON Company 3670X50*-1 and -2 (X = K, A, or V, depending on test set connector type)
Assurance Air Line	Frequency: 60 GHz	WILTRON Company Part Number: T1519 (K Connector, female) T1520 (3.5 mm, female) T1521 (V Conn, female–60 GHz) T1542 (V Conn, female–65 GHz)
Precision Offset Termination	Frequency: 40 GHz	WILTRON Company 29X50-15 (X = K, A, depending on test set connector type)
Precision Offset Termination	Frequency: 60 or 65 GHz	WILTRON Company Part Number: SC4417 (60 GHz) Part Number: SC4732 (65 GHz)

* Operation to 65 GHz with "B" versions of these products

Chapter 2
360B VNA System

Table of Contents

Chapter 2
360B VNA System

2-1 INTRODUCTION

This chapter describes the Model 360B Vector Network Analyzer System. The description is organized into an overall description, a description of system components, and a discussion on system operation. Chapters 3 and 4 respectively provide information for verifying performance and troubleshooting the system.

2-2 SYSTEM DESCRIPTION

The 360B VNA system characterizes a device-under-test (DUT) through the measurement of its forward and reverse transmission and reflection characteristics as a function of frequency. These characteristics are referred to as scattering parameters, or S-parameters. There are four S-parameters:

S_{11} = Forward Reflection
S_{21} = Forward Transmission
S_{12} = Reverse Transmission
S_{22} = Reverse Reflection

The VNA system mathematically compares the relative magnitude and phase changes between the signal incident to the DUT and the reflected or transmitted signal from the DUT to derive the S-parameters. It then presents the S-parameters graphically on a color display, printer, or plotter.

2-3 SYSTEM COMPONENTS

The 360B VNA system consists of three main components:

- Signal Source
- Test Set
- Vector Network Analyzer (VNA)

Figure 2-1 shows the 360B VNA system configuration and illustrates the interconnections between the signal source, test set, and VNA. The following paragraphs contain brief descriptions of each system component.

Signal Source The signal source provides the stimulus to the DUT via the test set. The frequency range of the signal source and the test set establish the frequency range of the VNA system. The signal source is controlled and phase-locked by the VNA and provides clean, phase-locked stimulus signals at programmed frequency points for precise test data. Frequency accuracy is assured by phase-locking both the signal source and the system local oscillators to the same 10 MHz reference time base. Frequency resolution is 100 kHz.

Two system signal sources are available: Model 360SS47 (10 MHz to 20 GHz) and Model 360SS69 (10 MHz to 40 GHz). Frequency coverage to 60 GHz is available by using the Model 360SS69 Signal Source with a Model 3612A, 3622A, or 3631A Test Set that includes a frequency tripler. In addition, the WILTRON Series 66XXB Sweep Generators and Series 67XXB Swept Frequency Synthesizers can be used as system signal sources.

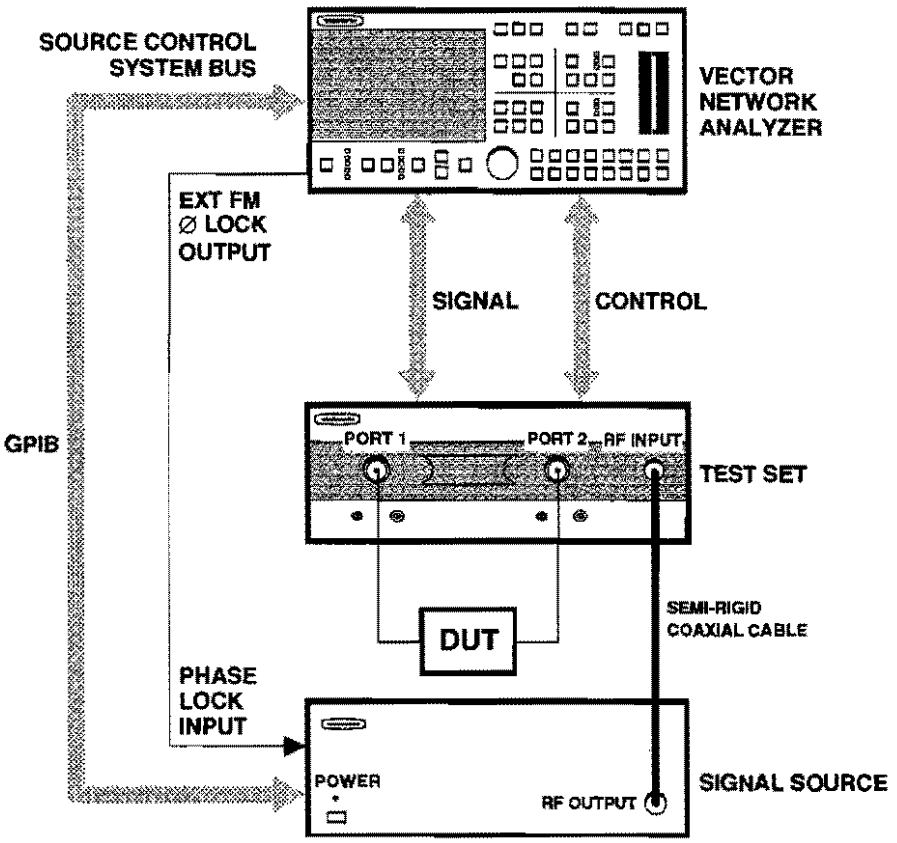


Figure 2-1. 360B VNA System Interconnections

The Test Set

The test set contains the measurement components for the 360B VNA system. The test set, under direct control of the VNA, performs the following:

- Stimulus signal routing from the signal source to the DUT through one of the test ports (Port 1 or Port 2).
- Signal separation and down conversion of the incident, reflected, and transmitted signals at Ports 1 and 2 into four IF signals (Test A, Reference A, Test B, and Reference B).
- Amplification of the IF signals.

Test sets are available that allow vector measurements for different applications. The test set types include active and passive device test sets with automatic signal reversing, frequency conversion test sets, and a millimeter-wave test set. Coaxial test sets include multiple models that cover frequency ranges from 10 MHz to 60 GHz. The millimeter-wave test set provides frequency coverage from 33 to 110 GHz in four waveguide bands (Q, U, V, and W).

VNA

The VNA is the system controller, signal processor, and display unit for all versions of the 360B VNA system. Its front panel controls provide menu selections for test functions, test parameters, measurement enhancements, and frequencies. The VNA sends frequency, power, and sweep information to the signal source over the dedicated source control system (GPIB) bus. It controls the test set functions through a dedicated digital bus via the CONTROL and SIGNAL cable assemblies. The VNA analyzes the IF signals from the test set for phase and magnitude data. It displays the results of this analysis (measurement data) as well as test parameters and system status on a large color display. The data presented on the display can be output to a plotter or printer or routed to the rear panel (external) GPIB or Centronics interface.

2-4 SYSTEM OPERATION

During a typical measurement, the microwave signal source, under direct control of the VNA, outputs an RF signal to the test set to provide stimulus to the DUT (Figure 2-2). The system signal source is phase-locked with the VNA's internal 10 MHz crystal oscillator. An external 10 MHz frequency standard may be substituted for the system's internal 10 MHz oscillator for maximum attainable frequency accuracy.

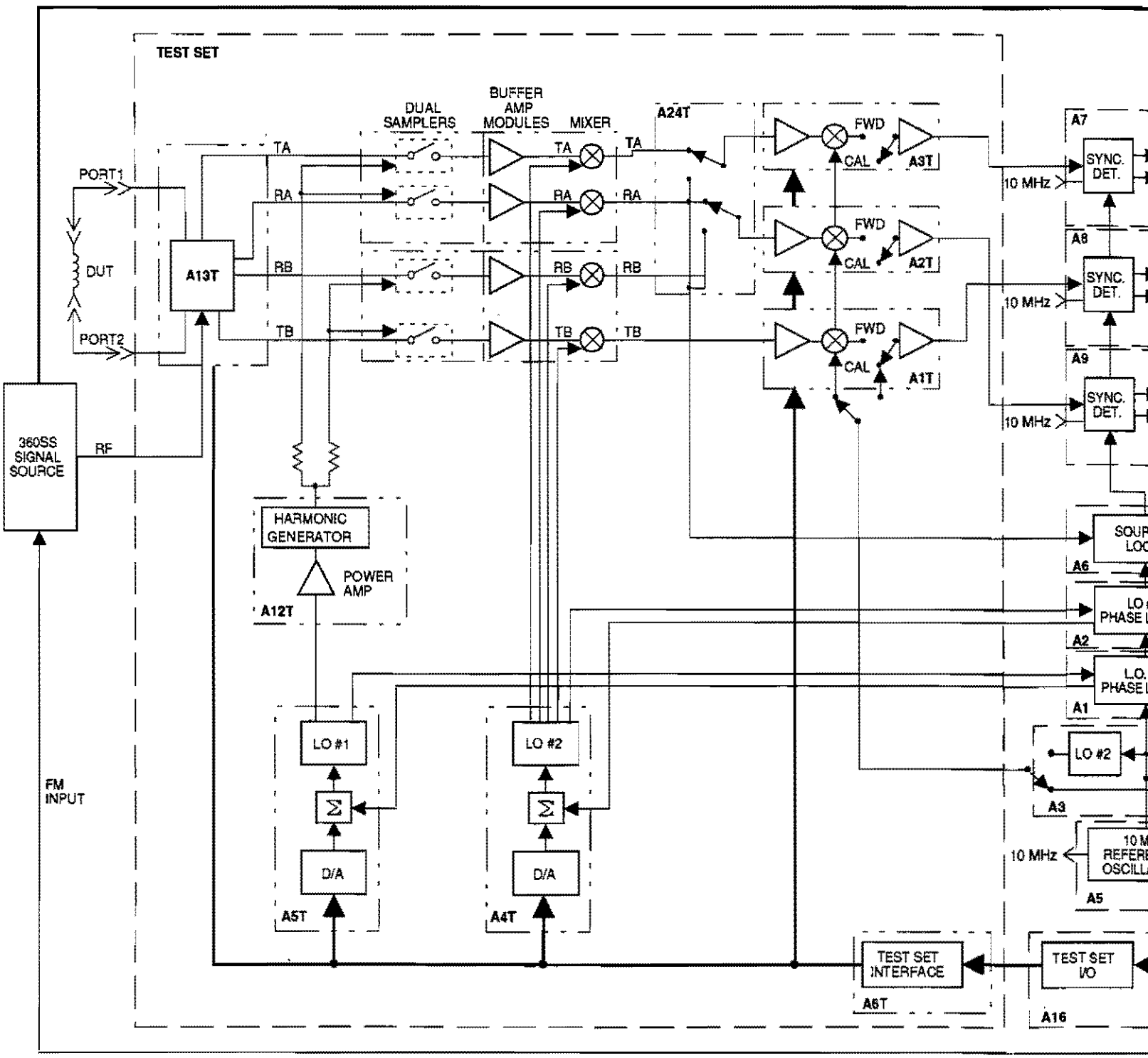
In the test set, the stimulus signal is sent to the DUT through one of the test set's test ports (Port1 or Port 2). When there is any impedance mismatch between the test port and the DUT input port, some of the signal incident at the DUT input port is reflected back to the test set and some travels into the DUT. In the case of two port DUTs (that is, those having an input and output port) the portion of the stimulus signal that travels through the DUT goes to the second test port for measurement.

In addition to stimulus signal routing from the signal source to the DUT, the test set also serves as the front end of the VNA receiver. Within the test set are signal separation and down conversion devices that separate and down convert the incident, reflected, and transmitted signals at Port 1 and Port 2 into four distinct intermediate (IF) signals. The incident signals are fed to Reference Channels A and B and the reflected or transmitted signals are fed to Test Channels A and B. Heterodyne frequency conversion is used to improve upon the inherent limitations of broadband diode detectors. It also provides significant improvement in dynamic range, harmonic rejection, and sensitivity.

Each of the four IF signals carries embedded magnitude and phase information relative to a reference signal. Down conversion of the signals does not affect the magnitude and phase relationship, only the frequency is changed. The IF signals go to selection switches in the test set that control (1) which signals are sent to the test set's IF amplifiers and then on to the synchronous detectors of the VNA, and (2) which reference signal will be used for phase-locking the system signal source.

The VNA source lock circuitry compares the selected reference signal's frequency and phase to that of a signal derived from the 10 MHz crystal oscillator in the VNA. If the system is not properly phase-locked, a correction voltage is generated that drives the FM Ø LOCK input to the system signal source, forcing it to source lock to the correct frequency and phase.

Additional signal processing is implemented within the VNA. The magnitude and phase information embedded on the analog IF signals is first detected, then converted to digital data. The VNA processors, controlled by embedded firmware coupled with system software, manipulate this digital data. Short-term system errors are normalized and digital compensation is generated and applied. The resultant S-parameter data characterizing the DUT is then presented on the VNA color display, output to a printer or plotter, or routed to the rear panel (external) GPIB interface.


TEST SET
DUAL SAMPLERS
BUFFER AMP MODULES
MIXER
A24T
PORT1
PORT2
DUT
A13T
TA
RA
RB
TB
FWD
CAL
A3T
A2T
A1T
A7
A8
A9
SYNC. DET.
10 MHz
360SS SIGNAL SOURCE
RF
HARMONIC GENERATOR
POWER AMP
A12T
A6
A2
A1
A3
LO #1
LO #2
Σ
D/A
A5T
A4T
FM INPUT
TEST SET INTERFACE
A6T
TEST SET I/O
A16
A5

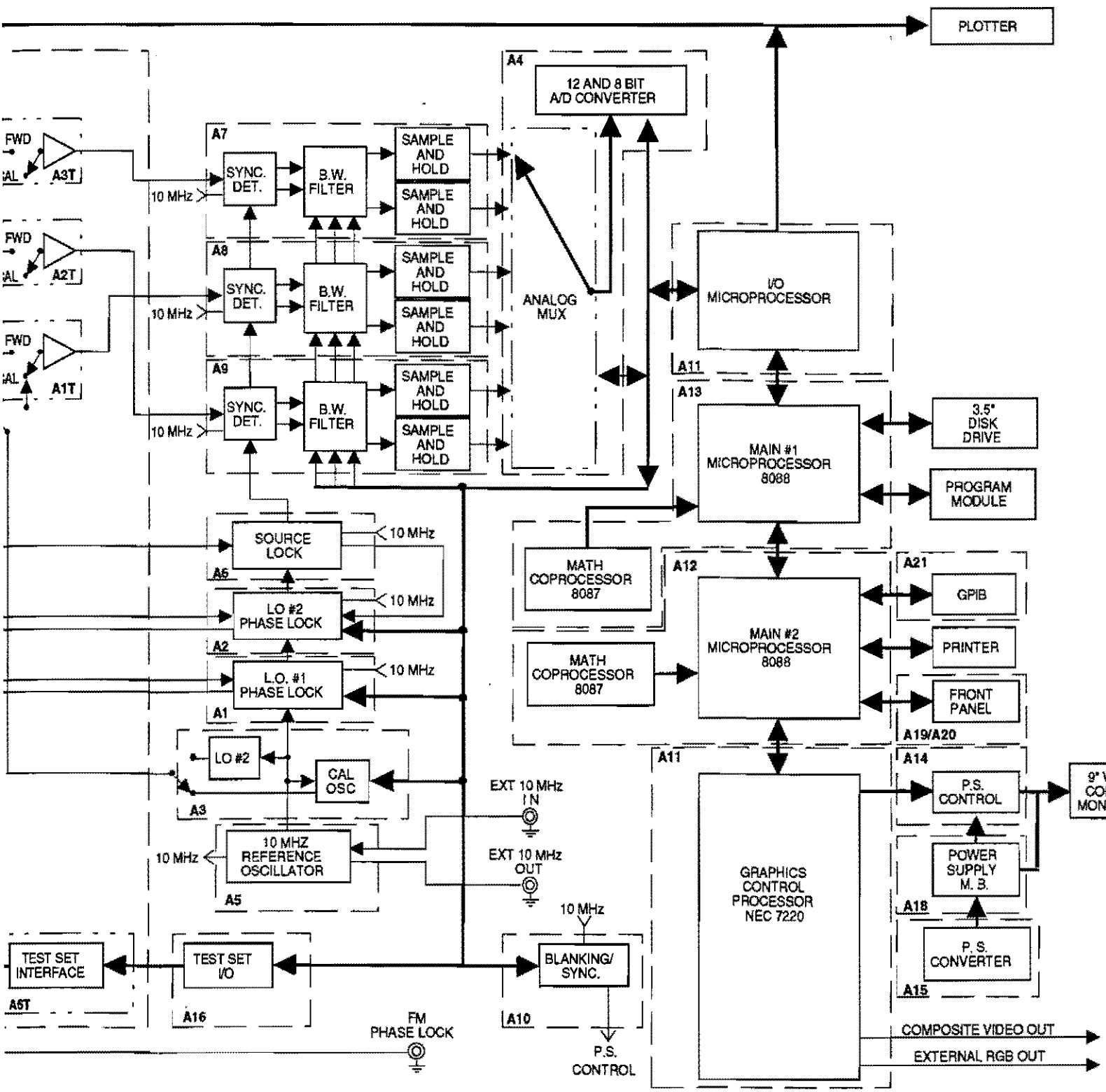


Figure 2-2. 360B VNA System Block Diagram

Chapter 3
360B VNA System Performance Tests and Adjustments

Table of Contents

Chapter 3
360B VNA System Performance Tests and Adjustments

3-1 INTRODUCTION

This chapter provides performance tests and adjustments for the 360B analyzer unit and test sets. Performance tests and adjustments for the 360XX Signal Source are provided in Chapter 10.

3-2 TEST EQUIPMENT

Recommended test equipment and manufacturer is listed in Chapter 1, Table 1-3. Equipment needed for individual model adjustments is listed with the model adjustments.

3-3 PERFORMANCE TESTS AND ADJUSTMENTS — GENERAL

Performance tests are provided for the 361XA/362XA, 3630A/3631A, and 3635B. Adjustments are provided for the 361XA/362XA and 3630A/3631A. The performance tests and adjustment procedures are located behind tabs for the applicable test set model.

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3-1 INTRODUCTION

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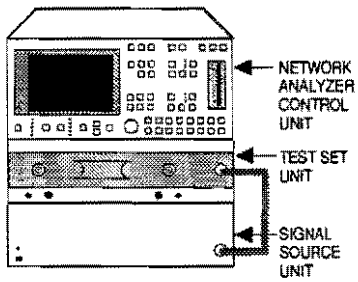
Anritsu VNA Performance Verification Software, part number 2300-237, supports 360 and 360B systems with 361xA and 362xA models. This software is used to verify that the 360B system is making accurate, traceable S-parameter measurements. Complete instructions are found in the User's Guide, which is shipped with the software and is automatically installed on the controller when the software is installed.

3-4 PERFORMANCE TESTS, MODELS 361XA/362XA

This tab section contains five performance tests that can be used to verify Model 360B VNA system operation. Setup instructions and performance procedures are included for each test. Test results can be compared with the specified limits that are provided for each test.

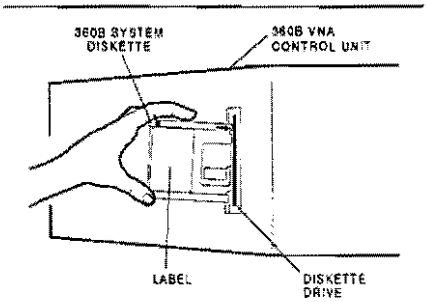
These tests do not establish measurement traceability; such verification requires using an appropriate WILTRON verification kit. Successful completion of these procedures indicates that your 360B VNA system is operating properly and is capable of making accurate measurements.



Required Equipment

The following equipment is required to perform the operation verification tests:

- ☐ Calibration kit, with Option 1: Sliding Termination.
- ☐ Flexible microwave cable (through line).
- ☐ Precision air line for up-to 40 GHz measurements.
- ☐ Precision offset for up-to 40 GHz measurements.
- ☐ Assurance air line for 60 and 65 GHz measurements.
- ☐ 20 dB offset termination for 60 and 65 GHz measurements.



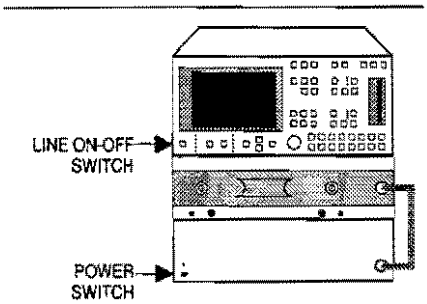
Initial System Setup

Perform the following steps before starting the performance tests.

Step 1. Verify that the 360B VNA system has been installed per Chapter 2–Installation of the Model 360B VNA Operation Manual (P/N 10410-00110).

Step 2. Install the 360B VNA system diskette into the disk drive of the network analyzer.

Step 3. Apply power to the frequency signal source then to the network analyzer. Loading of the system software takes approximately 1 minute (at which time the system is ready to make measurements).



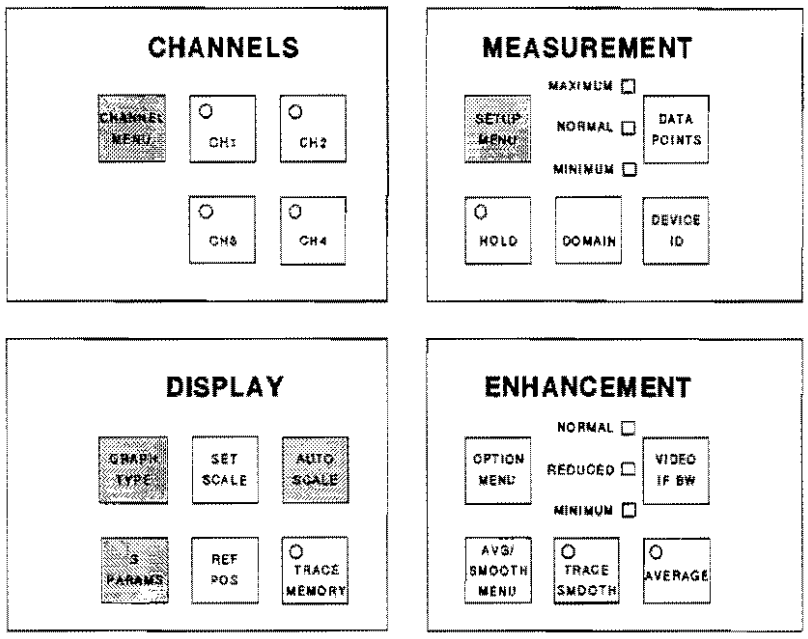
NOTE

Allow the system to warm up for at least 60 minutes to ensure operation to performance specifications.

3-5 SAMPLER EFFICIENCY TEST, MODELS 361XA/362XA

This test verifies that each individual receiver channel in the Model 361XA/362XA Coaxial Test Set operates properly. Measurement calibration of the system is *not* required for this test.

This test requires that you press a specified front panel keys and make choices from the displayed menu(s). The keys used in this test are shown below.

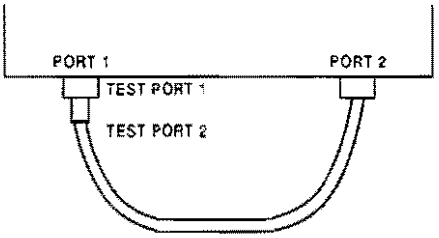


Key	Menu Choice
SETUP MENU	START: 500 MHz STOP: High End Frequency
CHANNEL MENU	FOUR CHANNELS
GRAPH TYPE	LOG MAGNITUDE (All channels)
AUTO SCALE	ON (All channels)
S-PARAMS	Channel 1: REF A Channel 2: TST A Channel 3: TST B Channel 4: REF B (See Figure 3-1 or 3-2)

Test Setup

Setup 360B VNA as described below.

Step 1. Connect Test Ports 1 and 2 together (below.)



Step 2. Set up the network analyzer as shown in table at left.

To independently measure the output of the individual test set channels, you must redefine the selected parameter for each display channel. You may redefine the parameters *manually*, as shown below for Channel 1, or *automatically*, as shown in Figure 3-2. The parameters are redefined as:.

$\frac{a_1}{1}$ = Test Set Channel 1 **REF A**

$\frac{b_1}{1}$ = Test Set Channel 2 **TST A**

$\frac{b_2}{1}$ = Test Set Channel 3 **TST B**

$\frac{a_2}{1}$ = Test Set Channel 4 **REF B**

Step 1. Press S PARAMS key.

Step 2. Make menu choices as shown in the following flow diagram.

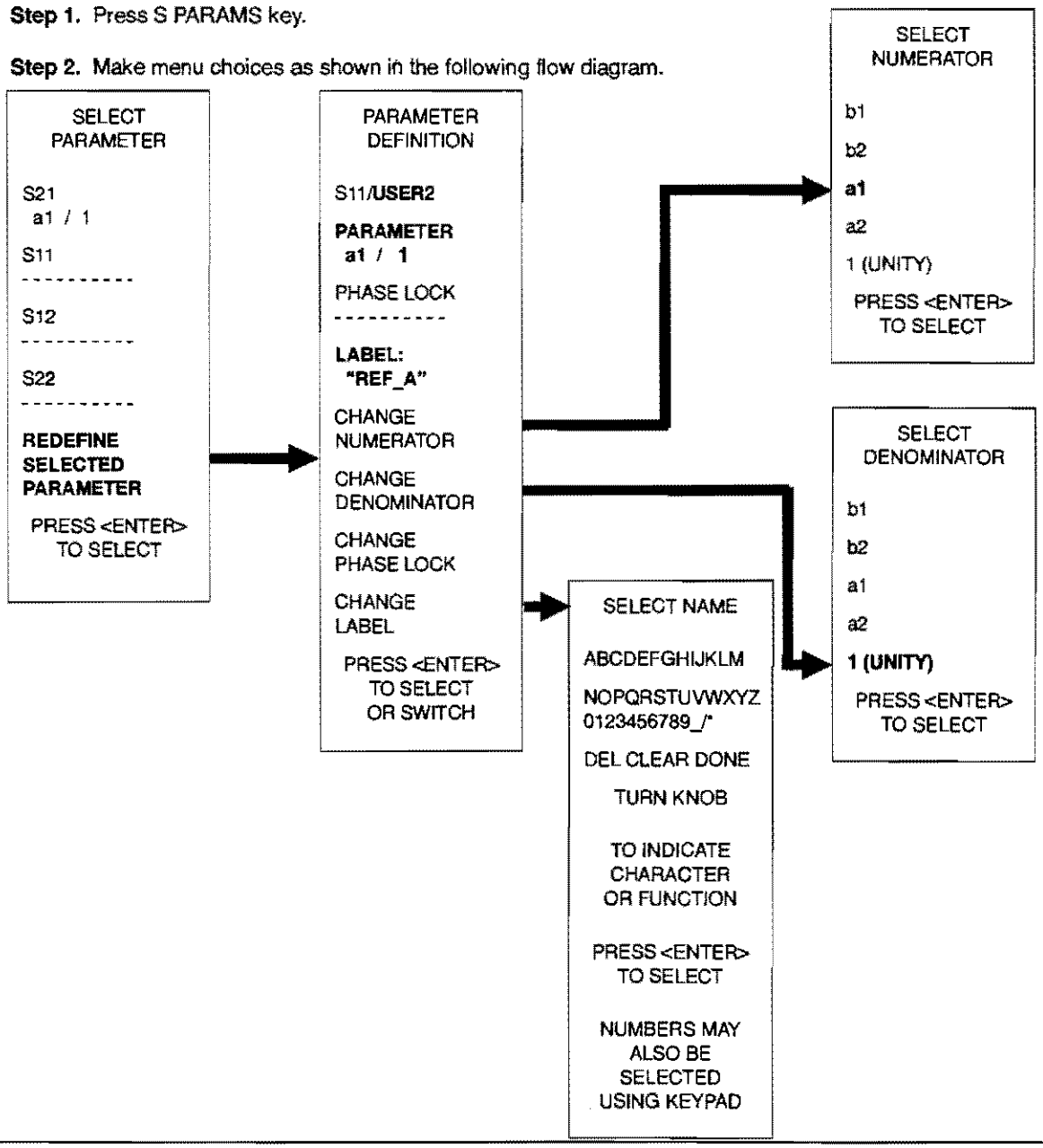


Figure 3-1. *Redefining Selected Parameter Manually for Sampler Efficiency Testing*

To independently measure the output of the individual test set channels, you must redefine the selected parameter for each display channel. You may redefine the parameters *automatically*, as shown below, or *manually*, as shown in Figure 3-1. The parameters are redefined as:.

$\frac{a_1}{1}$ = Test Set Channel 1 **REF A**

$\frac{b_1}{1}$ = Test Set Channel 2 **TST A**

$\frac{b_2}{1}$ = Test Set Channel 3 **TST B**

$\frac{a_2}{1}$ = Test Set Channel 4 **REF B**

Step 1. Press OPTION MENU key.

Step 2. Make menu choices as shown in the following flow diagram.

Step 3. Press SETUP MENU key; set START frequency to 500 MHz.

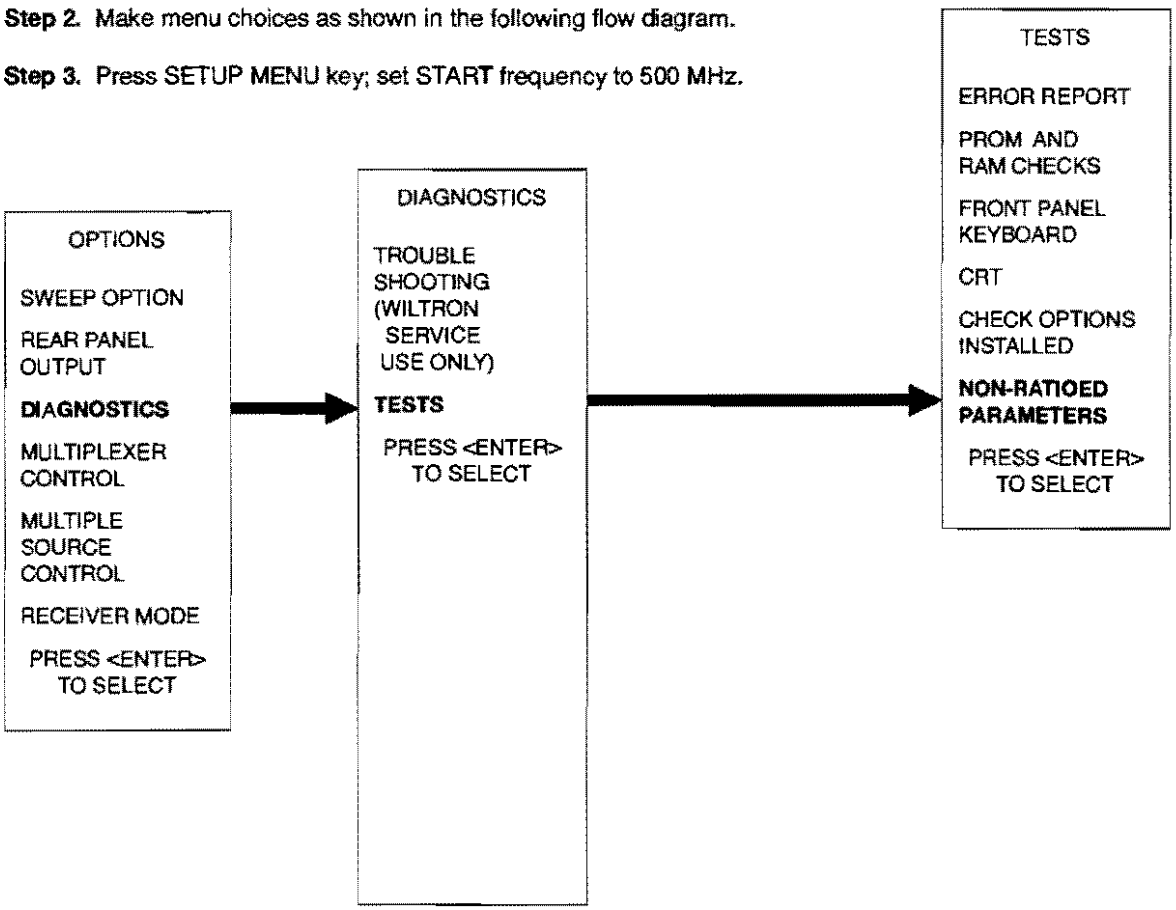
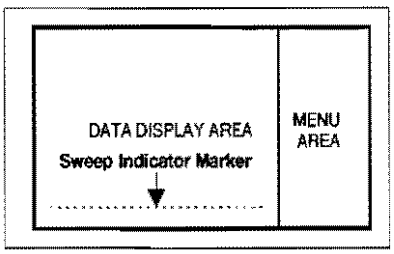


Figure 3-2. *Redefining Selected Parameter Automatically for Sampler Efficiency Testing*



Test Procedure

Perform test as described below.

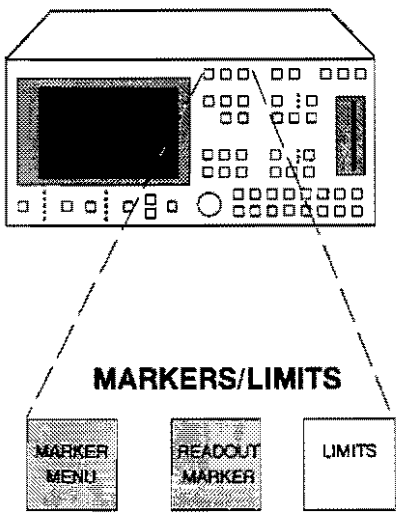
Step 1. Observe sweep indicator (top left) and allow at least one complete sweep to occur.

Step 2. Verify that the maximum-value to minimum-value amplitude slope (Figure 3-3) meets the specifications shown below.

Frequency	Reference Channels	Test Channels
20 GHz	<14 dB	<15 dB
40 GHz	<25 dB	<28 dB
50 GHz	<40 dB	<55 dB
60 GHz	<40 dB	<55 dB
65 GHz	<45 dB	<65 dB

Step 3. Verify that the minimum amplitude meets the specifications shown below.

Test Set	REF A	REF B	TST A	TST B
3610A	–40	–40	–42	–40
3620A	–38	–38	–43	–34
3611A	–42	–42	–52	–52
3621A	–41	–41	–55	–47
3612A	–53	–53	–78	–75
3622A	–55	–55	–78	–76
3613A	–53	–53	–78	–75
3623A	–55	–55	–78	–76
3615A	–53	–53	–78	–75
3625A	–55	–55	–78	–76



NOTE

Use the MARKER MENU and READOUT MARKER keys (bottom left) and menus to obtain precise frequency and amplitude values.

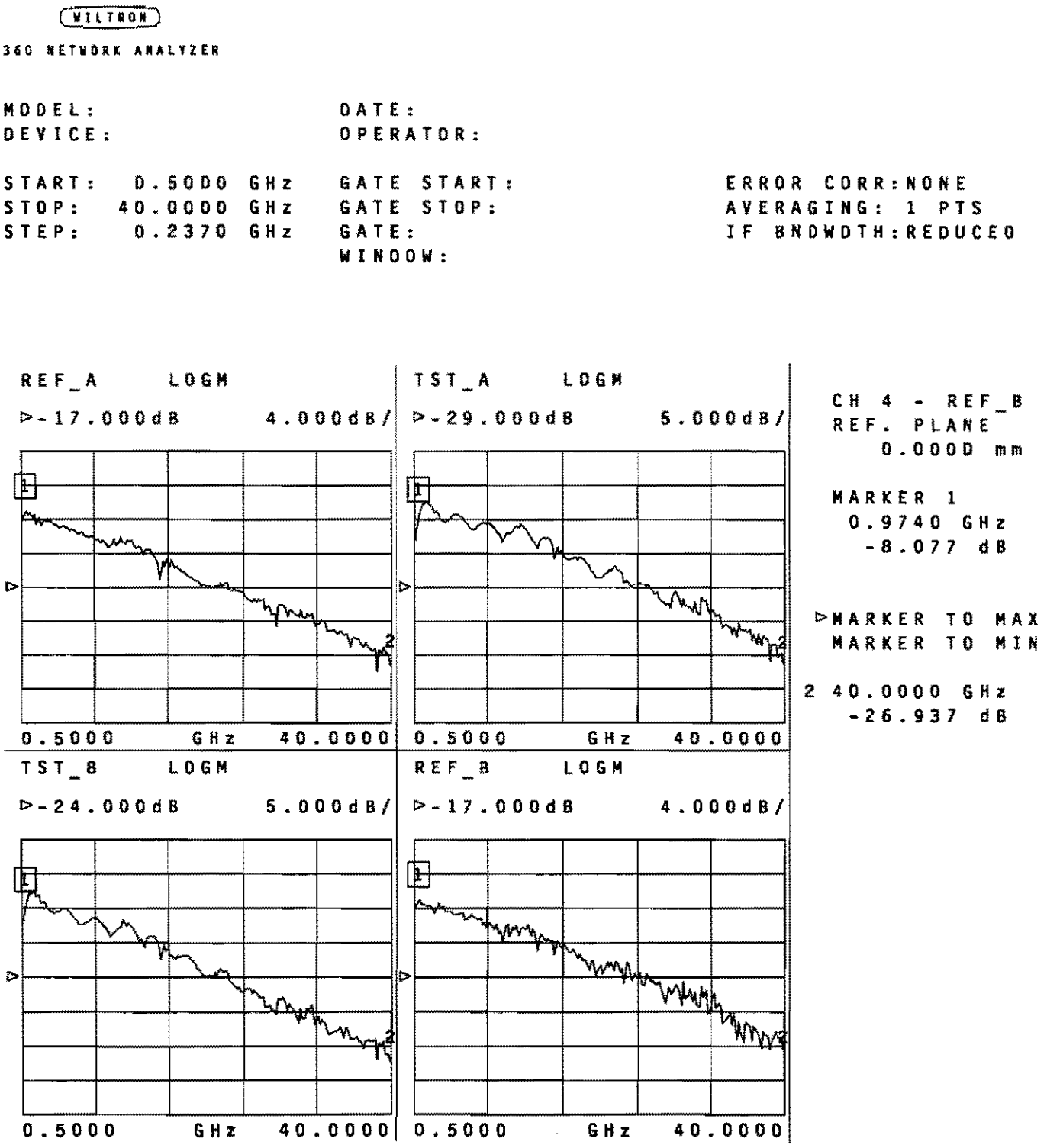


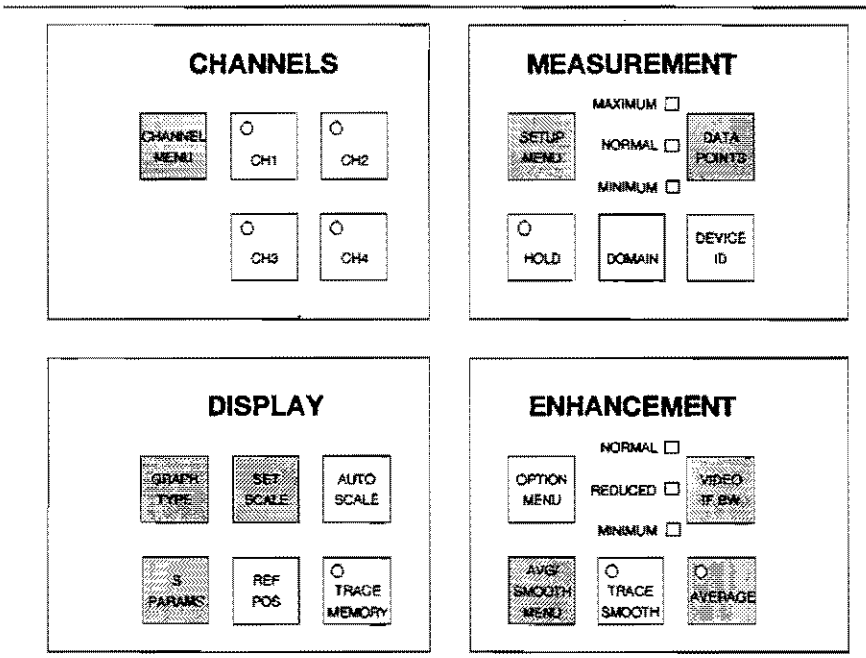
Figure 3-3. *Sampler Efficiency Test Waveforms*

3-6 HIGH LEVEL NOISE TEST, MODELS 361XA/362XA

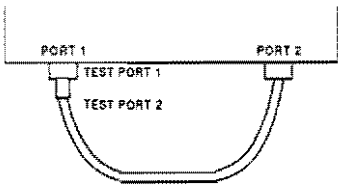
The following test verifies that the high-level noise in the 360B VNA will not significantly affect the accuracy of subsequent measurements. High-level noise is the random noise that exists in the 360B VNA System. Because it is non-systematic, it cannot be accurately predicted or measured. Thus, it cannot be removed using conventional error-correction techniques. Calibration of the system is *not* required for this test.

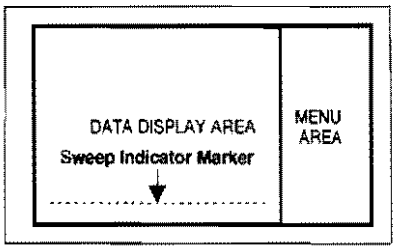
This test requires that you press a specified front panel key and make choices from the displayed menu(s). The keys used in this test are highlighted below.

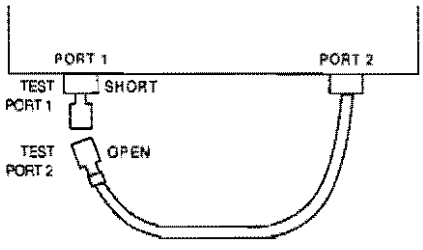
Key	Menu Choice
SETUP MENU	START: 40 MHz STOP: High-end frequency
CHANNEL MENU	DUAL CHANNELS 1-3
GRAPH TYPE	LOG MAGNITUDE (Both channels)
SET SCALE	RESOLUTION: 0.010 dB/DIV REF VALUE: 0.0 dB (Both channels)
S-PARAMS	Channel 1 – S12 Channel 3 – S21
AVG/ SMOOTH MENU	AVERAGING 128 MEAS. PER POINT
AVERAGE	ON
DATA POINTS	NORMAL
VIDEO IF BW	REDUCED
LIMITS	LIMIT 1 ON 0.020 dB (3610A/20A, and 3611A/21A), or: 0.040 dB (3612A/22A 3613A/23A, and 3615A/25A) LIMIT 2 ON –0.020 dB (3610A/20A and 3611A/21A) or: –0.040 dB (3612A/22A 3613A/23A, and 3615A/25A)



Test Setup Setup 360B VNA as described in table at left.







Test Procedure

Perform test as described below.

Step 1. Connect Test Port 1 and Test Port 2 (top left) together.

Step 2. Press CH 1 key.

Step 3. Press TRACE MEMORY key.

Step 4. Choose **VIEW DATA** from menu and press ENTER key.

Step 5. While observing sweep indicator (middle left), allow at least two complete sweeps to occur.

Step 6. Choose **STORE DATA TO MEMORY** from menu and press ENTER key.

Step 7. Choose **VIEW DATA ÷ MEMORY** from menu and press ENTER key.

Step 8. While observing sweep indicator (middle left), allow at least two complete sweeps to occur.

Step 9. Verify that the peak-to-peak High Level Noise falls within the area between the two limit lines (Figure 3-4).

Step 10. Press CH 3 key.

Step 11. Repeat steps 4 thru 9 for channel 3.

Step 12. Press S PARAMS key; set CH 1 for S_{11} and CH 3 for S_{22}.

Step 13. Connect a Short to Test Port 1 and an Open to Test Port 2 (left).

Step 14. Repeat steps 2 thru 9.

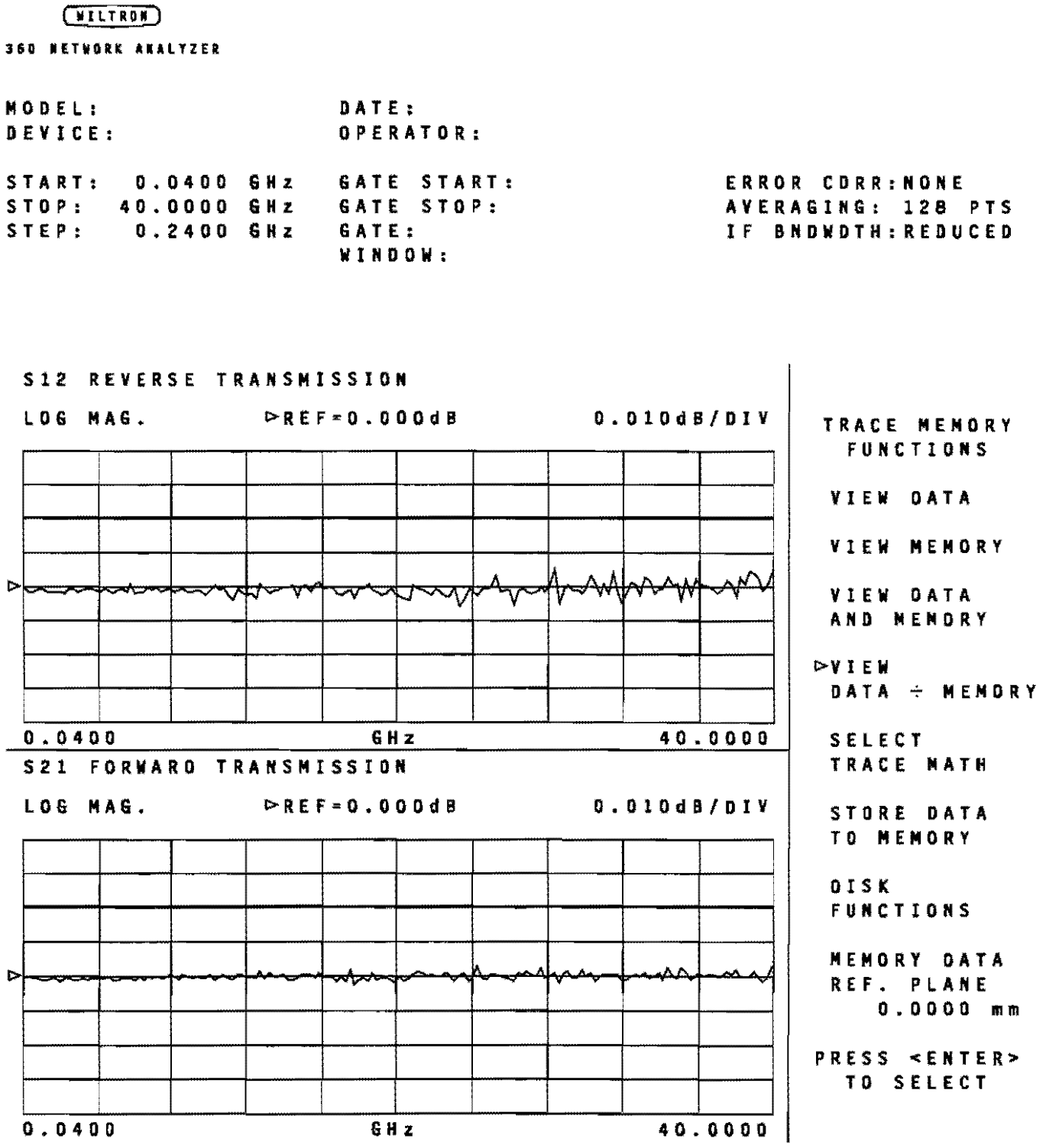
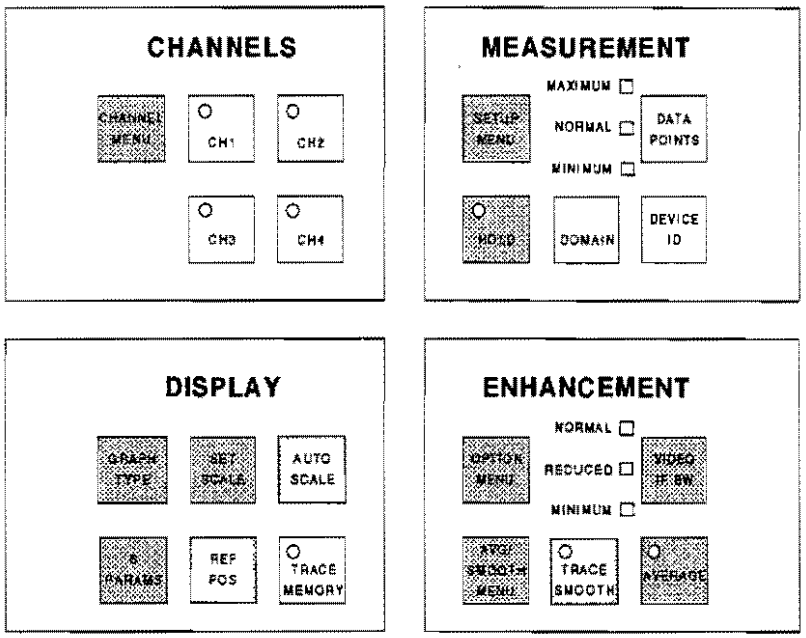


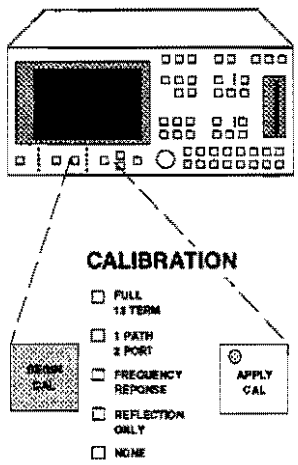
Figure 3-4. High Level Noise Test Waveform

3-7 SYSTEM DYNAMIC RANGE TEST, MODELS 361XA/362XA

This test verifies that the system dynamic range meets specifications. System dynamic range is the ratio of power incident on Port 2 in a through line connection to the noise floor at Port 2 (forward measurements only). The system must be calibrated and the error correction *applied* for this test.

This test requires that you press a specified front panel key and make choices from the displayed menu(s). The keys used in this test are highlighted below.





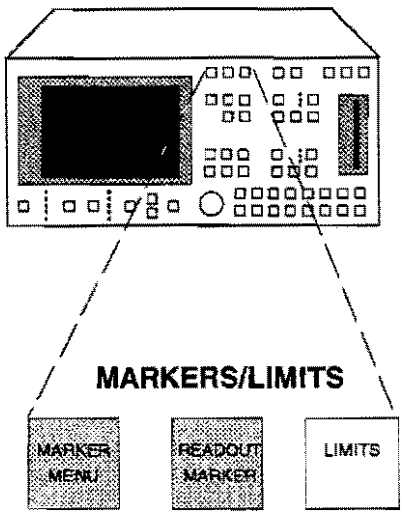
Test Setup Perform the test setup procedures, as described below.

Step 1. Press BEGIN CAL key (left).

Step 2. Using the menu prompts, perform a Full 12-Term **SLIDING LOAD** calibration over the full system operating range. (If necessary, refer to the 360B OM, Chapter 8, for detailed procedures.)

NOTE
Use 1024 averages and minimum IF bandwidth during the Isolation step in the calibration. These settings will be called out in subsequent procedures.

Key	Menu Choice
SETUP MENU	START: 40 MHz STOP: High-end frequency
CHANNEL MENU	SINGLE CHANNEL
GRAPH TYPE	LOG MAGNITUDE
SET SCALE	RESOLUTION: 10.0 dB/DIV REF VALUE: -50.0 dB REF LINE: TOP
S-PARAMS	S21
AVG/ SMOOTH MENU	1024 MEAS. PER POINT
AVERAGE	ON
VIDEO IF BW	MINIMUM
OPTION MENU	SWEEP OPTIONS then POINTS DRAWN IN C.W.: 100



Test Procedure

Step 3. Before pressing the ENTER key at the **ISOLATION DEVICES** menu prompt, press the AVG/SMOOTH MENU key and change averaging to **1024 MEAS. PER POINT.**

Step 4. When the isolation measurement is complete, press the AVG/SMOOTH MENU key and change averaging to **32 MEAS. PER POINT;** continue the calibration.

Step 5. Once the calibration process has finished, verify that the APPLY CAL key indicator is lit.

Step 6. Set up the network analyzer as shown in the table at top left.

Perform the test procedure as described below.

Step 1. Connect Broadband Terminations to Test Port 1 and Test Port 2 of the test set

Step 2. While observing the sweep indicator, allow two (forward and reverse directions) complete sweeps to occur, then press the HOLD key.

Step 3. Press the MARKER MENU key (bottom left), and select **MARKER 1** to be **ON.**

Step 4. Press the SETUP MENU key, select the **C.W.MODE** to be **ON**, and set the frequency to **40 MHz.**

Step 5. Press the READOUT MARKER key.

Step 6. Position the cursor to **MARKER TO MAX**, press the ENTER key, and record the value (Figure 3-5).

Step 7. Position the cursor to **MARKER TO MIN**, press the ENTER key, and record the value.

Step 8. Substract value in step 7 from that in step 6. To reduce measurement uncertainty, ensure that the difference is greater than 15 dB.

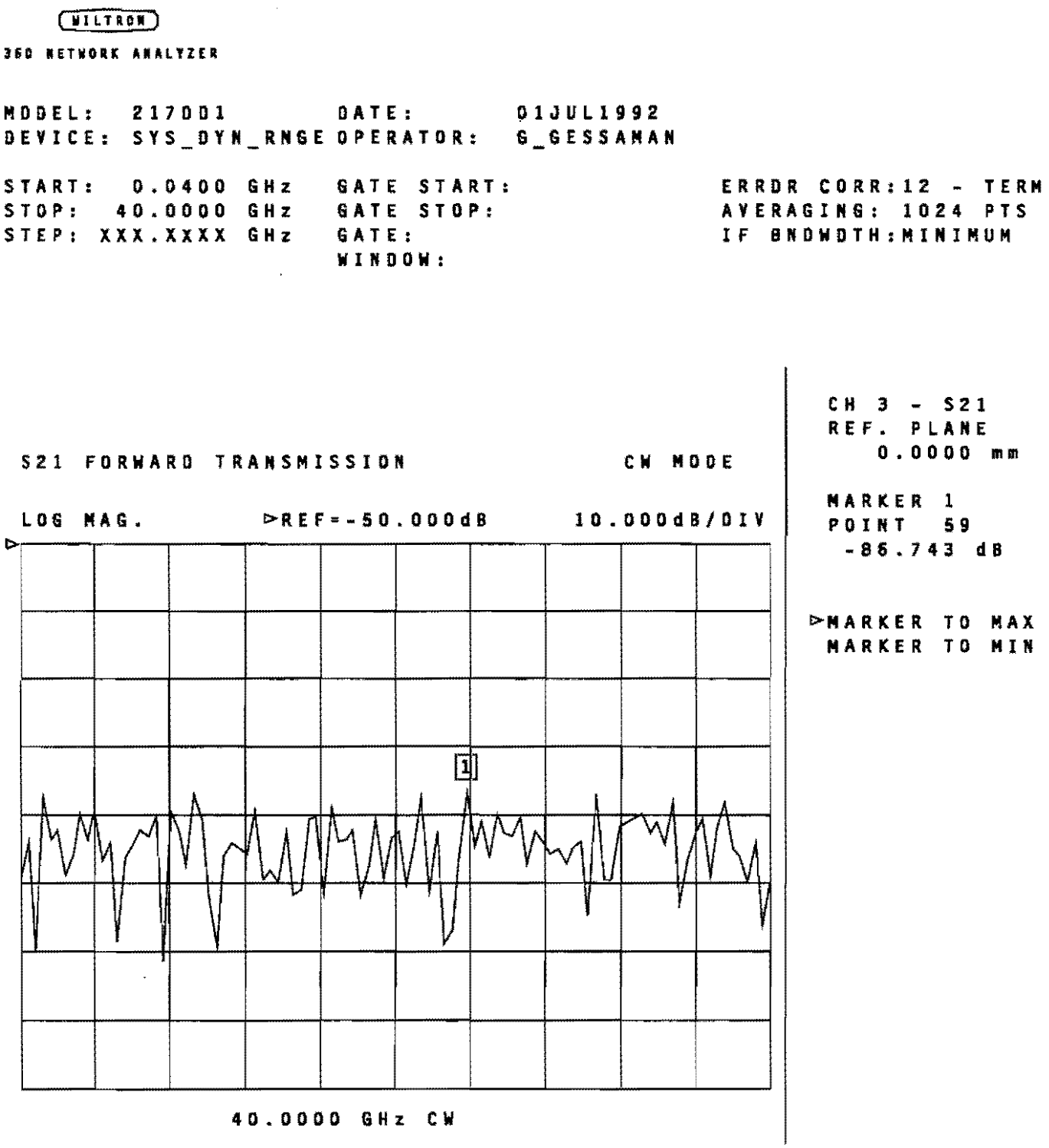


Figure 3-5. *Dynamic Range Test Waveform*

Step 9. Substract 6 dB from the value measured in step 6. This is the system dynamic range. Verify that its value compares favorably with the Table 3-1 value for 0.04 GHz.

Step 10. Repeat steps 4 through 9 for remaining frequencies in Table 3-1.

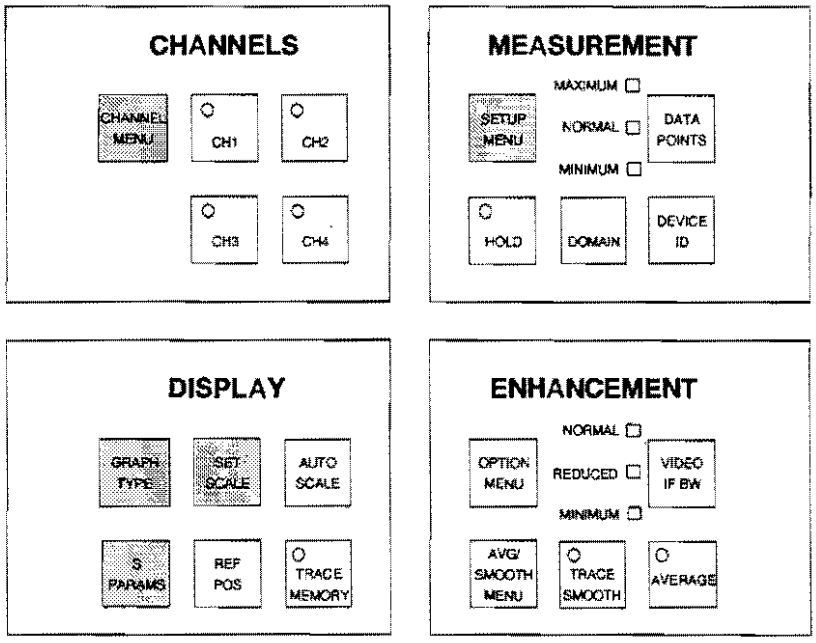
Table 3-1. *Dynamic Range Chacteristics*

Test Set Model	Frequency (GHz)	System Dynamic Range (dB)
3610A Reversing Test Set	0.04 1.0 20.0	–91 –108 –101
3611A Reversing Test Set	0.04 1.0 20.0 40.0	–86 –102 –96 –86
3612A 3615A to 50 GHz Reversing Test Set	0.04 1.0 20.0 40.0 50.0 60.0	–85 –101 –91 –83 –75 –70
3613A Reversing Test Set	0.04 1.0 20.0 40.0 60.0 65.0	–85 –101 –91 –83 –70 –62
3620A Active Device Test Set	0.04 1.0 20.0	–94 –110 –102
3621A Active Device Test Set	0.04 1.0 20.0 40.0	–89 –105 –97 –85
3622A 3625A to 50 GHz Active Device Test Set	0.04 1.0 20.0 40.0 50.0 60.0	–85 –101 –89 –79 –70 –65
3623A Active Device Test Set	0.04 1.0 20.0 40.0 60.0 65.0	–85 –101 –89 –79 –65 –60

3-8 EFFECTIVE DIRECTIVITY TEST, MODELS 361XA/362XA

This test verifies that the effective directivity of the system meets specifications. The system *must* be calibrated and the error correction *must be applied* for this test to be valid.

This test requires that you press a specified front panel keys and make choices from the displayed menu(s). The keys used in this test are shown below.



Key	Menu Choice
SETUP MENU	START: 40 MHz STOP: High-end frequency
CHANNEL MENU	SINGLE CHANNEL Channel 1
GRAPH TYPE	LOG MAGNITUDE
SET SCALE	RESOLUTION: 1.0 dB/Div REF VALUE: -15.0 dB (or value of termination offset) REFERENCE LINE: TOP
S-PARAMS	S11

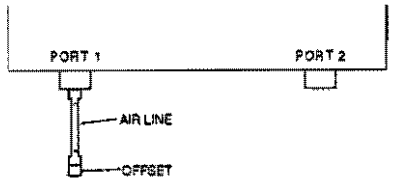
Test Setup

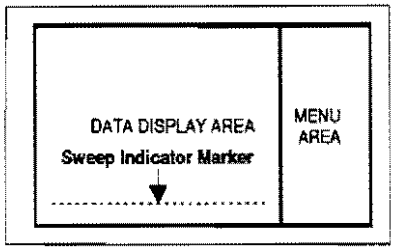
Perform the test setup procedures, as described below.

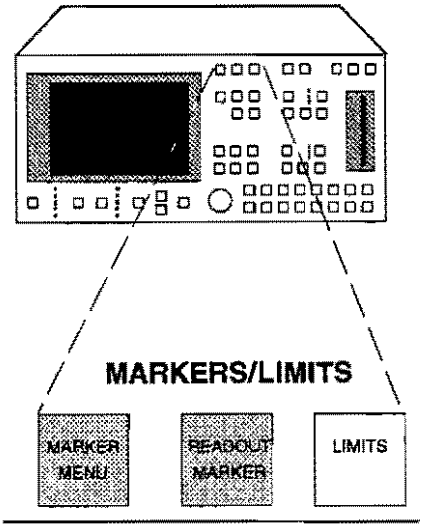
Step 1. Perform a full 12-term calibration, or use the calibration performed in paragraph 3-7.

Step 2. Ensure that the APPLY CAL key indicator is on.

Step 3. Set up the network analyzer as shown in the table at left







Test Procedure

Perform the test procedure as described below.

Step 1. Connect an Air Line and an Offset to Test Port 1 (top left).

Step 2. While observing sweep indicator (middle left), allow at least one complete sweep to occur.

Step 3. Press MARKER MENU key (bottom left) and select **MARKER 1, MARKER 2,** and **MARKER 3,** to be **ON.**

Step 4. Using rotary knob, position markers 1 and 3 to adjacent peaks of the worst-case ripple (one with the greatest amplitude); position marker 2 to the bottom of the trough (Figure 3-6).

Step 5. Using the MARKER MENU and READOUT MARKER key menus, record the absolute value of markers 1 and 3; subtract one from the other, halve the difference and add it to the value of the marker at the lowest peak. This is the average value of the two peaks.

Step 6. Record the value of marker 2.

Step 7. Substract the value recorded in step 5 from that recorded in step 6 (Example: 0.24 dB). This is the "REF ± X Peak to Peak Ripple dB" value that you will use next in the Microwave Measurement Chart (Table 3-3, page 3-22).

Step 8. Turn to page 3-22 and find the "REF ± X Peak to Peak Ripple dB" value closest to your measured value (0.2454 for the example in step 7).

Step 9. Move your finger across to the "X dB Below Reference" column. Add the value from this column (Example: 37) to the >REF = value that appears on the 360B measurement screen. *This is the effective directivity value for* PORT 1 (52 db for the example: 37 + 15 = 52).

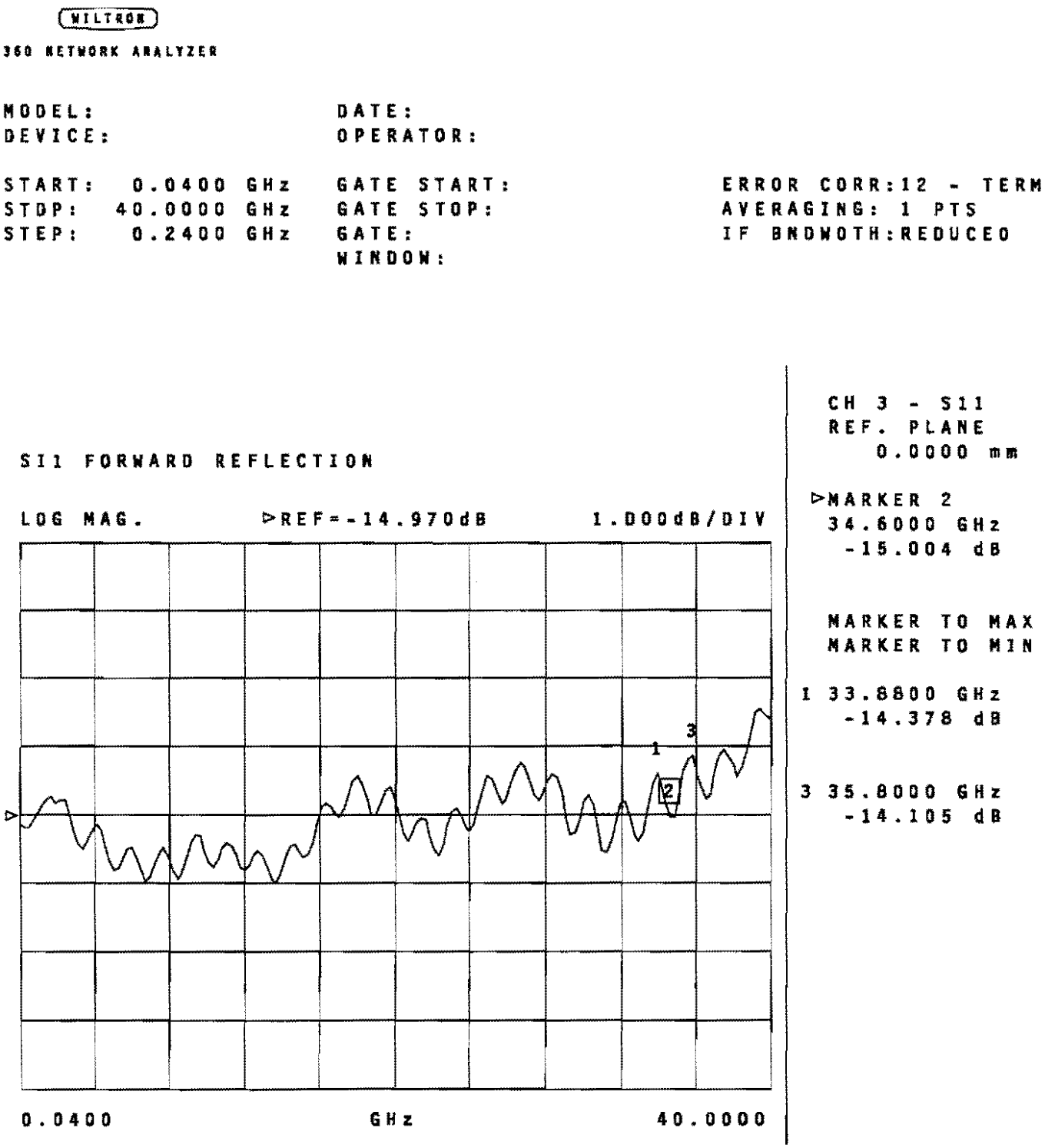


Figure 3-6. *Effective Directivity Test Waveform*

Table 3-2. Test Port Chacteristics

Connector	Frequency (GHz)	Directivity (dB)
GPC-7	0.04	>52
	1.0	>52
	18.0	>52
3.5 mm	0.04	>44
	1.0	>44
	20.0	>44
	26.5	>44
K	0.04	>42
	1.0	>42
	20.0	>42
	40.0	>38
V	0.04	>40
	1.0	>40
	20.0	>40
	40.0	>36
	50.0	>34
	60.0	>34
	65.0	>32

Step 10. Verify that the directivity value meets the specification in Table 3-2 for each band. If it does not, repeat steps 4 through 9 for each band.

NOTE

The procedure above measures the characteristics of Test Port 1 only. To measure the characteristics of Test Port 2, a second calibration must be performed with the test cable connected to Test Port 1 instead of Test Port 2. (This allows measurements at the Test Port 2 connector that are not influenced by the quality of the test port cable.

Step 11. To measure the characteristics of Test Port 2, perform steps 12 through 14.

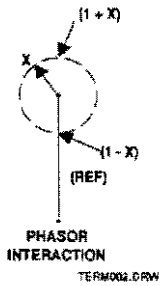
Step 12. Press the S PARAMS key and change to **S22.**

Step 13. Move the Air Line and Offset to Test Port 2.

Step 14. Repeat steps 4 through 10 for the S_{22} parameter.

Table 3-3. Microwave Measurement Chart

Conversion tables for return loss, reflection coefficient, and SWR with tabular values for interaction of a small phasor X with a large phase (unity reference) expressed in dB related to reference.

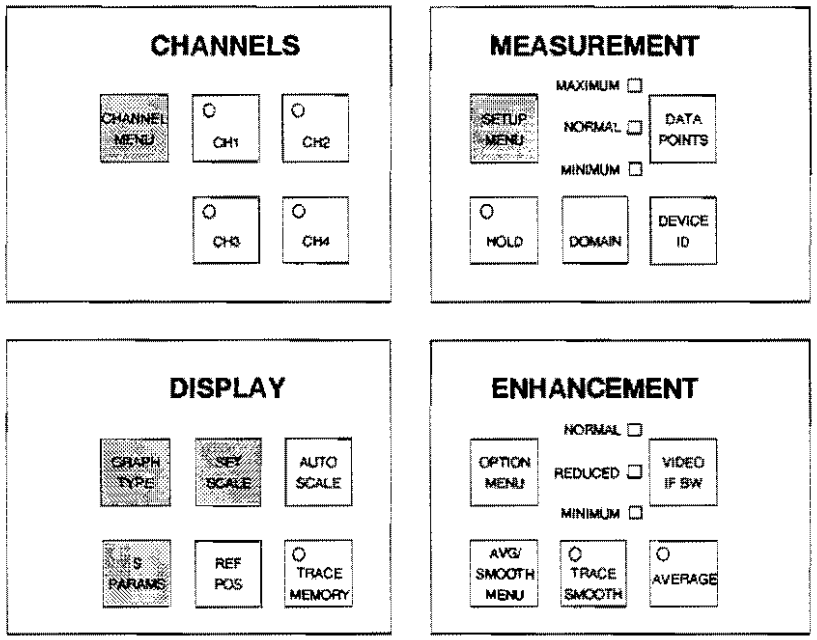


			Relative to Unity Reference			
SWR	Reflection Coefficient	Return Loss (dB)	X dB Below Reference	REF + X dB	REF − X dB	REF ± X Peak to Peak Ripple dB
17.3910	0.8913	1	1	5.5350	−19.2715	24.8065
8.7242	0.7943	2	2	5.0790	−13.7365	18.8145
5.8480	0.7079	3	3	4.6495	−10.6907	15.3402
4.4194	0.6310	4	4	4.2489	−8.6585	12.9073
3.5698	0.5623	5	5	3.8755	−7.1773	11.0528
3.0095	0.5012	6	6	3.5287	−6.0412	9.5699
2.6146	0.4467	7	7	3.2075	−5.1405	8.3480
2.3229	0.3981	8	8	2.9106	−4.4096	7.3204
2.0999	0.3548	9	9	2.6376	−3.8063	6.4439
1.9250	0.3162	10	10	2.3866	−3.3018	5.6884
1.7849	0.2818	11	11	2.1567	−2.8756	5.0322
1.6709	0.2512	12	12	1.9465	−2.5126	4.4590
1.5768	0.2239	13	13	1.7547	−2.2013	3.9561
1.4985	0.1995	14	14	1.5802	−1.9331	3.5133
1.4326	0.1778	15	15	1.4216	−1.7007	3.1224
1.3767	0.1585	16	16	1.2778	−1.4988	2.7766
1.3290	0.1413	17	17	1.1476	−1.3227	2.4703
1.2880	0.1259	18	18	1.0299	−1.1687	2.1986
1.2528	0.1122	19	19	0.9237	−1.0337	1.9574
1.2222	0.1000	20	20	0.8279	−0.9151	1.7430
1.1957	0.0891	21	21	0.7416	−0.8108	1.5524
1.1726	0.0794	22	22	0.6639	−0.7189	1.3828
1.1524	0.0708	23	23	0.5941	−0.6378	1.2319
1.1347	0.0631	24	24	0.5314	−0.5661	1.0975
1.1192	0.0562	25	25	0.4752	−0.5027	0.9779
1.1055	0.0501	26	26	0.4248	−0.4466	0.8714
1.0935	0.0447	27	27	0.3796	−0.3969	0.7765
1.0829	0.0398	28	28	0.3391	−0.3529	0.6919
1.0736	0.0355	29	29	0.3028	−0.3138	0.6166
1.0653	0.0316	30	30	0.2704	−0.2791	0.5495
1.0580	0.0282	31	31	0.2414	−0.2483	0.4897
1.0515	0.0251	32	32	0.2155	−0.2210	0.4365
1.0456	0.0224	33	33	0.1923	−0.1967	0.3890
1.0407	0.0200	34	34	0.1716	−0.1751	0.3467
1.0362	0.0178	35	35	0.1531	−0.1558	0.3090
1.0322	0.0158	36	36	0.1366	−0.1388	0.2753
1.0287	0.0141	37	37	0.1218	−0.1236	0.2454
1.0255	0.0126	38	38	0.1087	−0.1100	0.2187
1.0227	0.0112	39	39	0.0969	−0.0980	0.1949
1.0202	0.0100	40	40	0.0864	−0.0873	0.1737
1.0180	0.0089	41	41	0.0771	−0.0778	0.1548
1.0160	0.0079	42	42	0.0667	−0.0693	0.1380
1.0143	0.0071	43	43	0.0613	−0.0617	0.1230
1.0127	0.0063	44	44	0.0546	−0.0550	0.1096
1.0113	0.0056	45	45	0.0487	−0.0490	0.0977
1.0101	0.0050	46	46	0.0434	−0.0436	0.0871
1.0090	0.0045	47	47	0.0387	−0.0389	0.0776
1.0080	0.0040	48	48	0.0345	−0.0346	0.0692
1.0071	0.0035	49	49	0.0308	−0.0309	0.0616
1.0063	0.0032	50	50	0.0274	−0.0275	0.0549
1.0057	0.0028	51	51	0.0244	−0.0245	0.0490
1.0050	0.0025	52	52	0.0218	−0.0218	0.0436
1.0045	0.0022	53	53	0.0194	−0.0195	0.0389
1.0040	0.0020	54	54	0.0173	−0.0173	0.0347
1.0036	0.0018	55	55	0.0154	−0.0155	0.0309
1.0032	0.0016	56	56	0.0138	−0.0138	0.0275
1.0028	0.0014	57	57	0.0123	−0.0123	0.0245
1.0025	0.0013	58	58	0.0109	−0.0109	0.0219
1.0022	0.0011	59	59	0.0097	−0.0098	0.0195
1.0020	0.0010	60	60	0.0087	−0.0087	0.0174

3-9 EFFECTIVE SOURCE MATCH TEST, MODELS 361XA/362XA

This test verifies that the effective source match of the system meets specifications. The system must be calibrated and the error correction must be applied for these tests.

This test requires that you press a specified front panel keys and make choices from the displayed menu(s). The keys used in this test are shown below.



Key	Menu Choice
SETUP MENU	START: 40 MHz STOP: 20 GHz (3610A/20A) 40 GHz (3611A/21A) 50 GHz (3615A/25A) 60 GHz (3612A/22A) 65 GHz (3613A/23A)
CHANNEL MENU	SINGLE CHANNEL
GRAPH TYPE	LOG MAGNITUDE
SET SCALE	RESOLUTION: 0.02 dB/DIV REF VALUE: 0 dBm
S-PARAM	S11

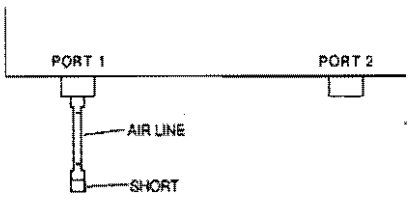
Test Setup

Perform the test setup procedures, as described below.

Step 1. Perform a full 12-term calibration, or use the calibration performed in paragraph 3-7.

Step 2. Ensure that the APPLY CAL key indicator is on.

Step 3. Set up the network analyzer as shown in the table at left.



Test Procedure

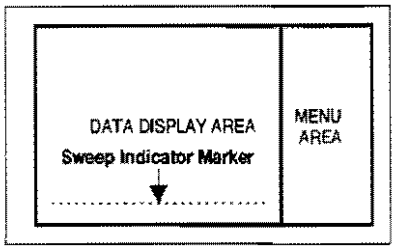
Perform the test procedure as described below.

Step 1. Connect an Air Line and a Short to PORT 1 of the test set (left).

Step 2. While observing sweep indicator (middle left), allow at least one complete sweep to occur.

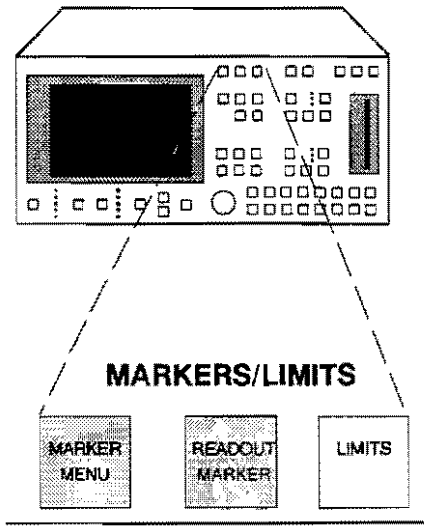
Step 3. Press MARKER MENU key (bottom left), and select **MARKER 1, MARKER 2,** and **MARKER 3,** to be **ON.**

Step 4. Using rotary knob, position markers 1 and 3 to adjacent peaks of the ripple with the greatest negative trough; position marker 2 to the bottom of the trough (Figure 3-7).



Step 5. Using the MARKER MENU and READOUT MARKER key menus, record the absolute value of markers 1 and 3; subtract one from the other, halve the difference and add it to the value of the marker at the lowest peak. This is the average value of the two peaks.

Step 6. Record the marker 2 value.



Step 7. Substract the value recorded in step 5 from that recorded in step 6. This is the "REF ± X Peak to Peak Ripple dB" value that you will use next in the Microwave Measurement Chart (Table 3-3, page 3-22.).

Step 8. Turn to page 3-22 and find the "REF ± X Peak to Peak Ripple dB" value closest to your measured value.

Step 9. Move your finger across to the "X dB Below Reference" column. Add the value from this column to the >REF = value that appears on the 360B measurement screen. *This is the effective source match value for* PORT 1.

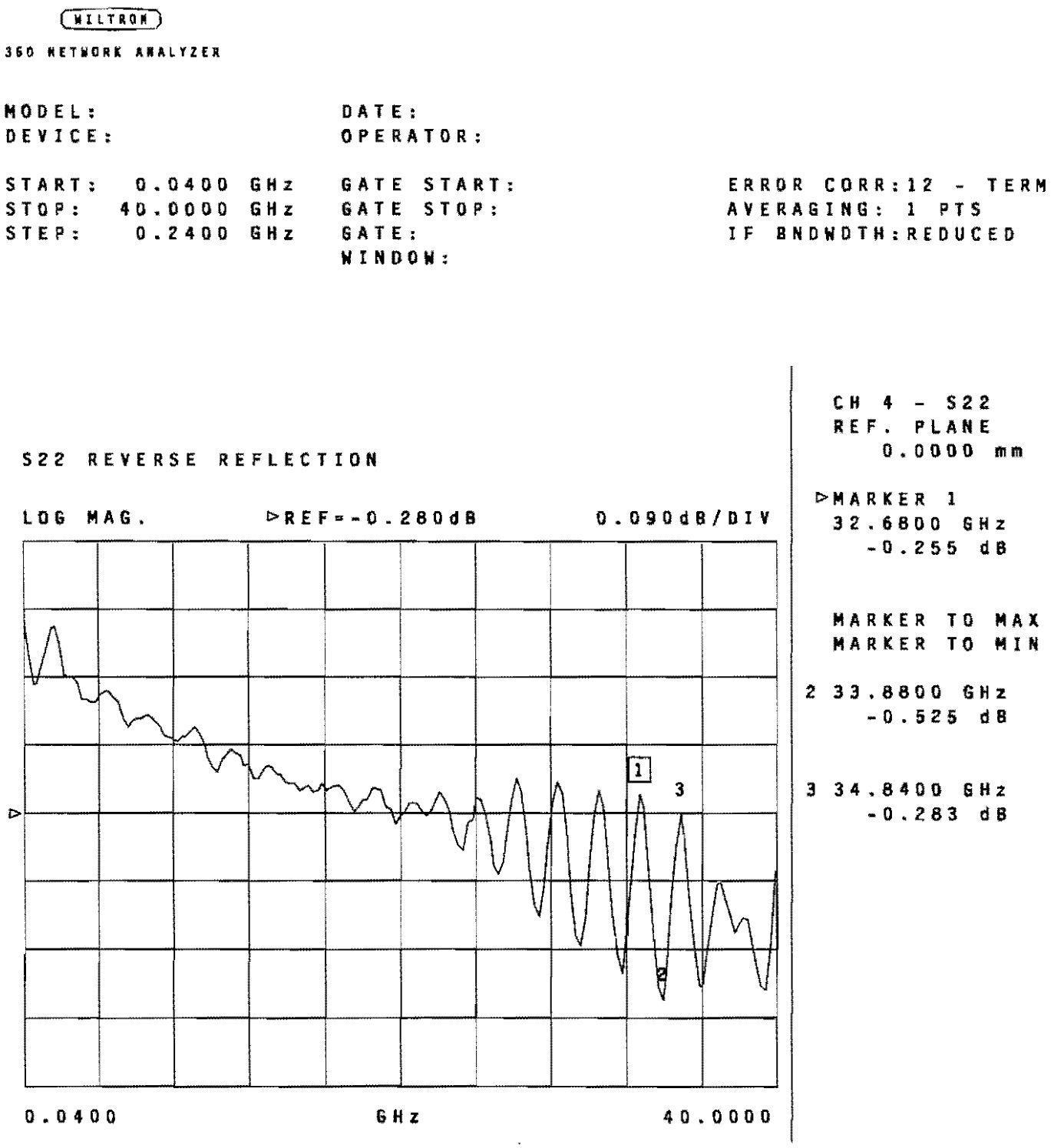


Figure 3-7. *Effective Source Match Test Waveform*

Table 3-4. Source Match Specifications

Connector	Frequency (GHz)	Source Match (dB)
GPC-7	0.04	>44
	1.0	>44
	18.0	>42
3.5 mm	0.04	>40
	1.0	>40
	20.0	>38
	26.5	>34
K	0.04	>40
	1.0	>40
	20.0	>38
	40.0	>33
V	0.04	>38
	1.0	>38
	20.0	>36
	40.0	>32
	50.0	>28
	60.0	>28
	65.0	>26

Step 10. Verify that the source match meets the specification in Table 3-4 for each band. If it does not, perform steps 4 through 9 for each band.

NOTE

The procedure above measures the characteristics of Test Port 1 only. To measure the characteristics of Test Port 2, a second calibration must be performed with the test cable connected to Test Port 1 instead of Test Port 2. (This allows measurements at the Test Port 2 connector that are not influenced by the quality of the test port cable.

Step 11. To measure the characteristics of Test Port 2, perform steps 12 through 14.

Step 12. Press the S PARAMS key and change to **S22.**

Step 13. Move the Air Line and Short to Test Port 2.

Step 14. Repeat steps 4 through 10 for the S_{22} parameter.

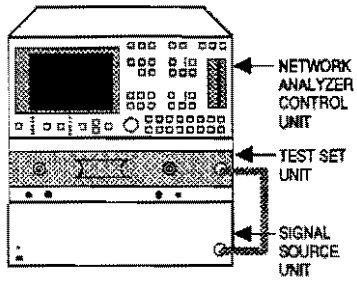
3-10 ADJUSTMENTS, MODELS 361XA/362XA

The only adjustments that can be performed in the field are to the A5T LO 1 PCB and the A4T LO 2 PCB. A detailed procedure for adjusting these two PCBs is provided in paragraph 3-11.

Required Equipment

The following equipment is required to perform the A5T PCB and A4T PCB adjustments:

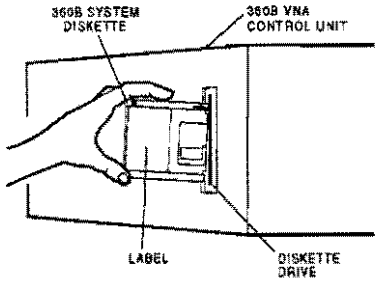
- ☐ 360B Test Fixture
- ☐ PCB Extender
- ☐ Coaxial Adapter Cables
- ☐ Digital Multimeter



Initial System Setup

Perform the following steps before starting the performance tests.

Step 1. Verify that the 360B VNA system has been installed per Chapter 2–Installation of the Model 360B VNA Operation Manual (P/N 10410-00110).

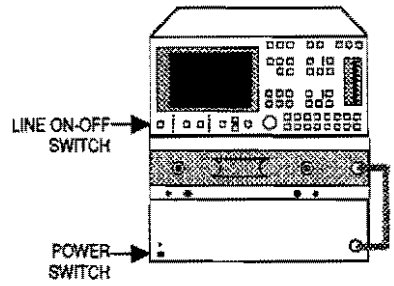


Step 2. Install the 360B VNA system diskette into the disk drive of the network analyzer.

Step 3. Apply power to the frequency signal source then to the network analyzer. Loading of the system software takes approximately 1 minute (at which time the system is ready to make measurements).

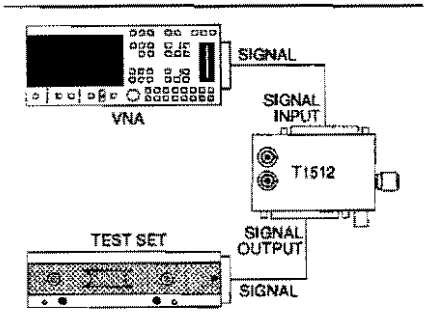
NOTE

Allow the system to warm up for at least 60 minutes to ensure operation to performance specifications.



3-11 A5T AND A4T PCB ADJUSTMENTS, MODELS 361XA/362XA

This paragraph provides a detailed procedure for verifying and adjusting the A5T PCB and A4T PCBs.



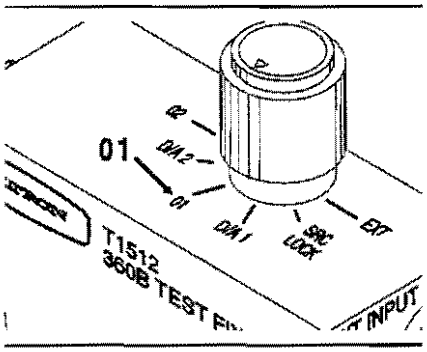
Initial setup From rear of console or cabinet, connect the T1512 Test Fixture in series with the SIGNAL connectors on the VNA and test set (top left).

Verification To determine whether or not the A5T and A4T PCBs are operating properly, perform the following steps.

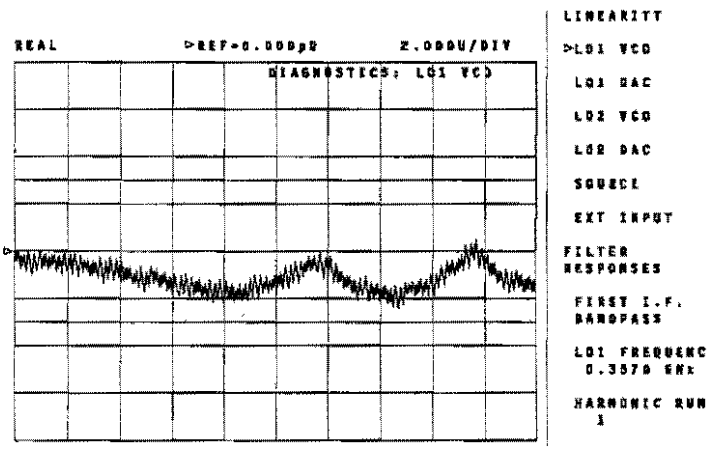
Step 1. Set the rotary knob on the T1512 to 01 (middle left).

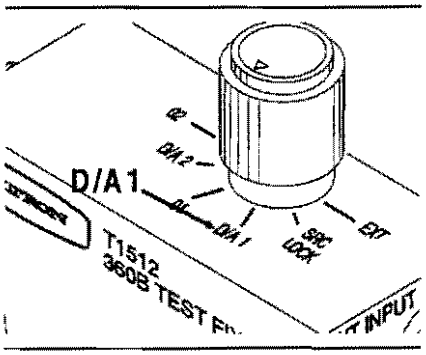
Step 2. Press OPTION MENU key on VNA.

Step 3. Select **DIAGNOSTICS**, then **TROUBLESHOOTING**, then **LO1 VCO** when the applicable menu appears.



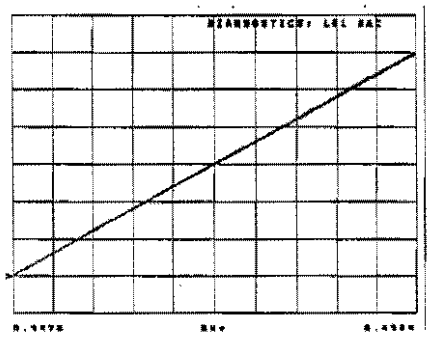
Step 4. Check that waveform displayed on VNA is between the two limit lines (below). If it is, the A5T PCB is adjusted properly.

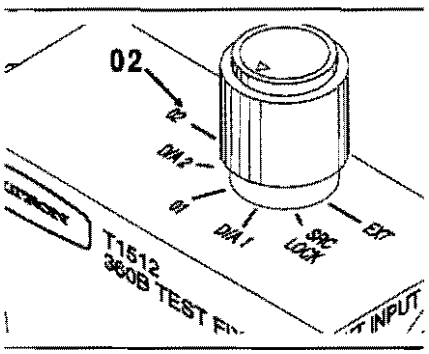


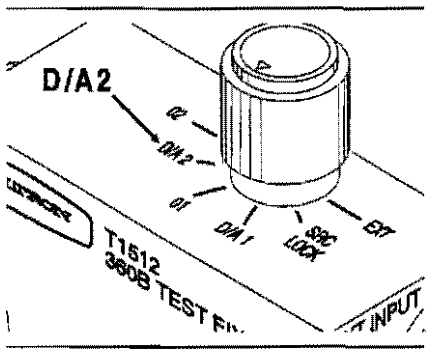


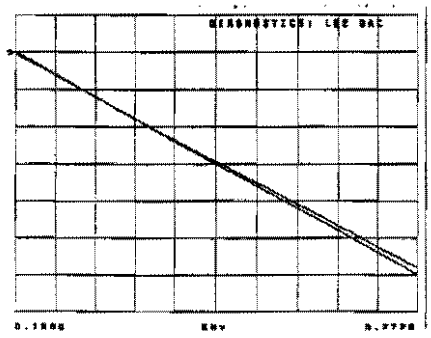
Step 5. Select **LO 1 DAC** on displayed VNA menu.

Step 6. Set the rotary knob on the T1512 to D/A 1 (bottom left).







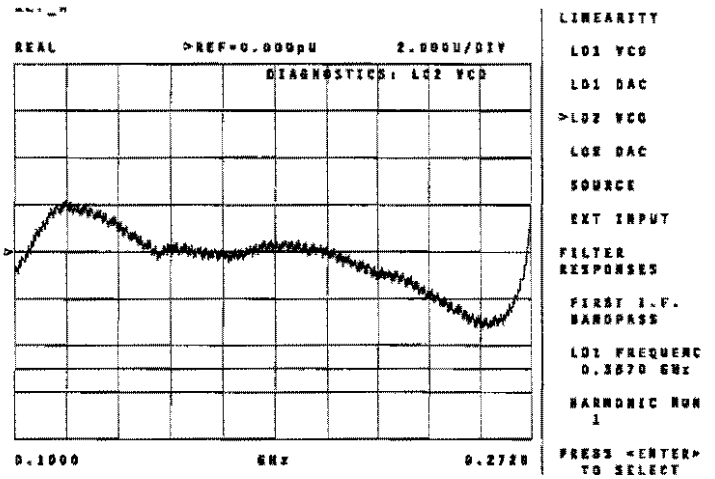


Step 7. Check that the measured data (red cursor) is superimposed on the memory trace (green cursor) in the waveform displayed on the VNA (top left). Also, ensure the amplitude is +12V (6 divisions). If it is, perform the LO 1 adjustment, below; if not, replace the A5T PCB.

Step 8. Set the rotary knob on the T1512 to 02 (middle left).

Step 9. Select **LO2 VCO** on displayed VNA menu.

Step 10. Check that waveform displayed on VNA is between the two limit lines (below). If it is, LO 2 is adjusted properly.



Step 11. Select **LO 2 DAC** on displayed VNA menu.

Step 12. Set the rotary knob on the T1512 to D/A 2 (middle left).

Step 13. Check that the measured data (red cursor) is superimposed on the memory trace (green cursor) in the waveform displayed on the VNA (bottom left). Also, ensure the amplitude is +12V (6 divisions). If it is, perform the LO 2 adjustment, below; if not, replace the A4T PCB.

LO 2 Adjustment

Adjust LO 2 as follows:

Step 1. Turn off power to the 360B system.

Step 2. Disconnect cabling and remove test set from console or cabinet.

Step 3. Reconnect cable between CONTROL connectors on VNA and test set.

Step 4. Reconnect T1512 in series with SIGNAL connectors on VNA and test set.

Step 5. Remove the top cover from the test set (paragraph 6-6).

Step 6. Remove the A4T PCB (paragraph 6-7) and place it on a PCB extender.

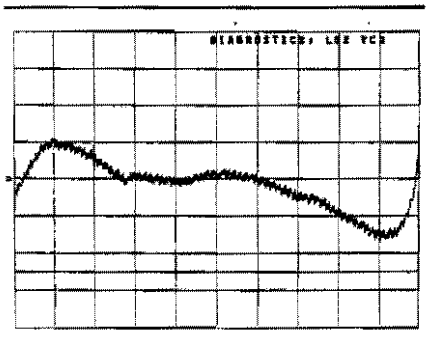
Step 7. Use coaxial adapter cables, if necessary, to connect RF output connector (J1) to mating connector on test set.

NOTE
You can leave connectors A4TJ2 – J5 disconnected for this adjustment.

Step 8. Turn on power to the 360B system.

Step 9. Set the rotary knob on the T1512 to 02.

Step 10. Press OPTION MENU key on VNA.

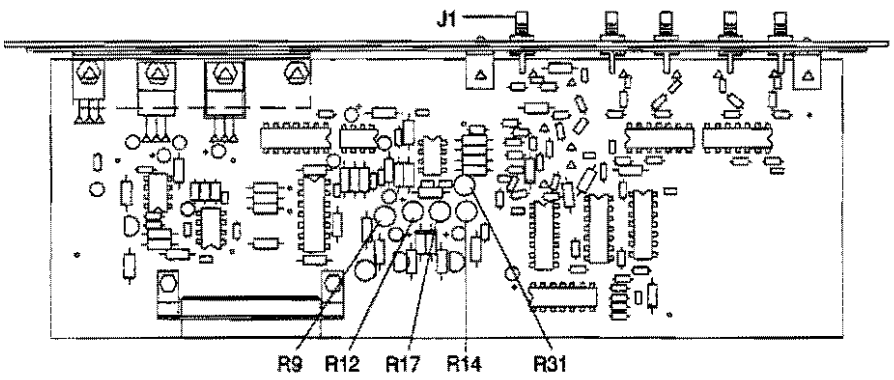


Step 11. Select **DIAGNOSTICS**, then **TROUBLESHOOTING**, then **LO2 VCO** when the applicable menu appears.

Step 12. Adjust potentiometers R9, R12, R14, R17, and R31 (facing page) so that the VNA-displayed waveform falls between the limit lines (left).

Step 13. Remove the T1512, replace test set covers, and reinstall test set in console or cabinet.

Step 14. Verify that LO 2 is still within the limit lines.



LO 1 Adjustment

Adjust LO 1 as follows:

Step 1. Turn off power to the 360B system.

Step 2. Disconnect cabling and remove test set from console or cabinet.

Step 3. Reconnect cable between CONTROL connectors on VNA and test set.

Step 4. Reconnect T1512 in series with SIGNAL connectors on VNA and test set.

Step 5. Remove the top cover from the test set (paragraph 6-6).

Step 6. Remove the A5T PCB (paragraph 6-7) and place it on PCB extender.

Step 7. Use coaxual adapter cables, if necessary, to connect RF output connector to mating connector on test set.

Step 8. Turn on power to the 360B system.

Step 9. Set the rotary knob on the T1512 to 01.

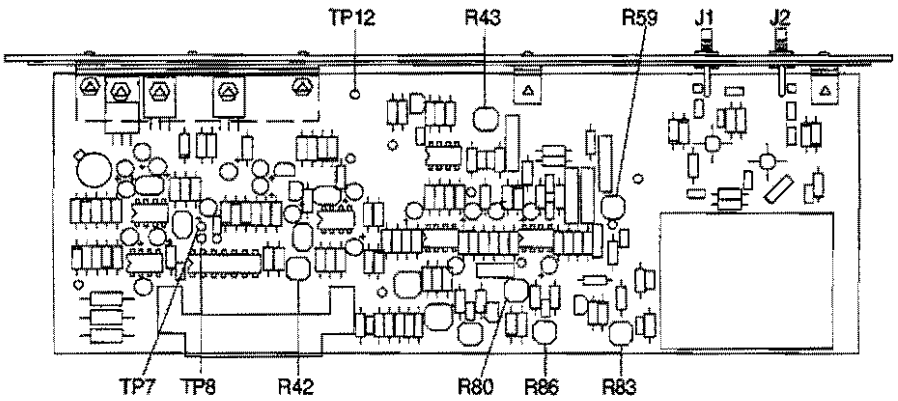
Step 10. Press OPTION MENU key on VNA.

Step 11. Select **DIAGNOSTICS**, then **TROUBLESHOOTING**, then **LO1 VCO** when the applicable menu appears.

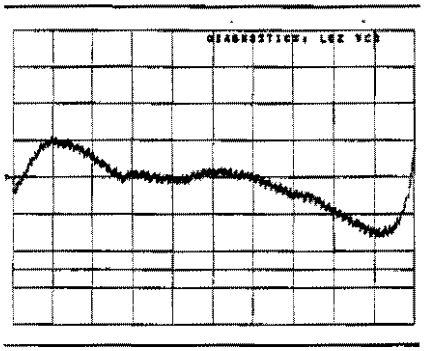
Step 12. Press SETUP MENU key on VNA.

Step 13. Select **C.W. MODE** on the displayed menu and set for **536.5 MHz.**

Step 14. Connect digital multimeter between TP8 (+) and TP12(–) (below).



Step 15. Adjust R42 (above) on A5T for –12.00 ±3 mV.



Step 16. Check that TP7 is between +11.85V and +12.00V.

Step 17. Adjust potentiometers R43, R59, R80, R83, and R86 (above) so that the VNA-displayed waveform falls between the limit lines (left).

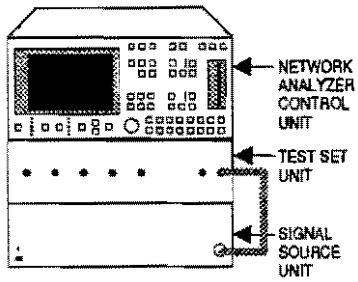
Step 18. Remove the T1512, replace test set covers, and reinstall test set in console or cabinet.

Step 19. Verify that LO 1 is still within the limit lines.

3-12 PERFORMANCE TESTS, MODELS 3630A/3631A

This tab section contains five performance tests that can be used to verify Model 360B VNA system operation using the 3630A or 3631A Test Set. Setup instructions and performance procedures are included for each test. Test results can be compared with the specified limits that are provided for each test.

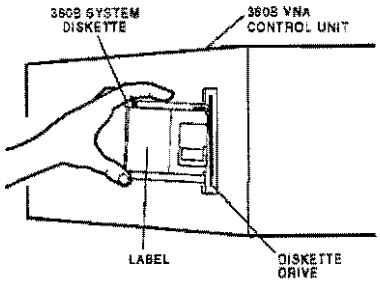
These tests do not establish measurement traceability; such verification requires using an appropriate WILTRON verification kit. Successful completion of these procedures indicates that your 360B VNA system is operating properly and is capable of making accurate measurements.



Required Equipment

The following equipment is required to perform the operation verification tests:

- ☐ Power Meter with Power Sensor to 40 GHz (60 GHz for 3631A)
- ☐ Calibration kit, with Option 1: Sliding Termination.
- ☐ Flexible microwave cable (through line).



Initial System Setup

Perform the following steps before starting the performance tests.

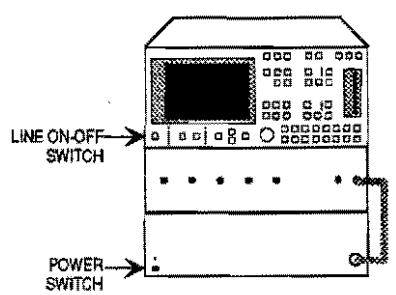
Step 1. Verify that the 360B VNA system has been installed per Chapter 2–Installation of the Model 360B VNA Operation Manual (P/N 10410-00110).

Step 2. Install the 360B VNA system diskette into the disk drive of the network analyzer.

Step 3. Apply power to the frequency signal source then to the network analyzer. Loading of the system software takes approximately 1 minute (at which time the system is ready to make measurements).

NOTE

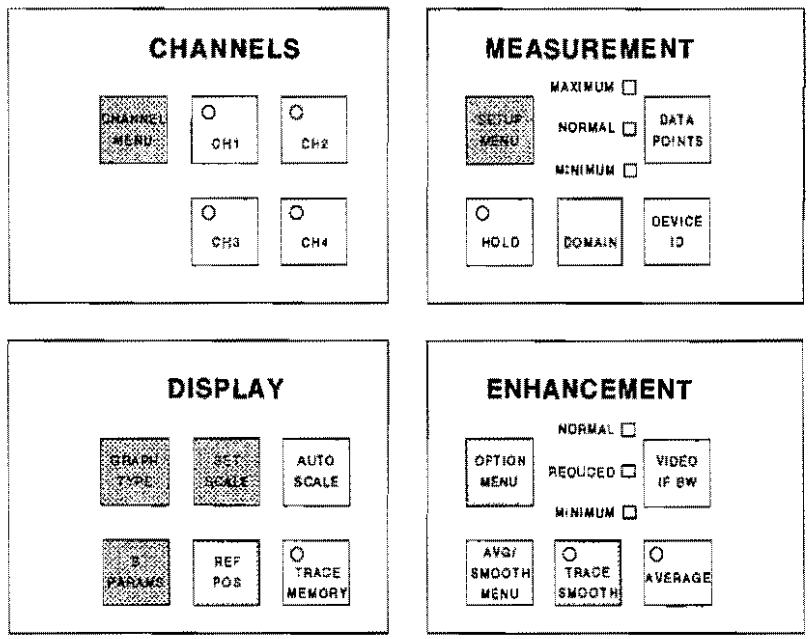
Allow the system to warm up for at least 60 minutes to ensure operation to performance specifications.



3-13 FULL-BAND PERFORMANCE TEST, MODELS 3630A/3631A

This test verifies that each individual receiver channel in the Model 3630A/3631A Frequency Converter Test Set operates properly, and that all four channels exhibit similar power-slope characteristics.

This test requires that you press specified front panel keys and make choices from the displayed menus. The keys used in this test are shown below.

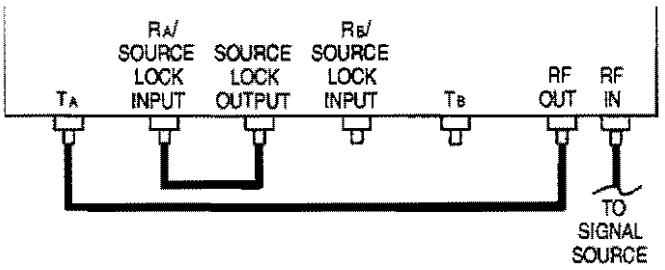


Key	Menu Choice
SETUP MENU	START: 0.01 GHz STOP: High-end frequency TEST SIGNALS; then SOURCE 1 PWR: 5 dBm PORT 1 SOURCE: 20 dB
CHANNEL MENU	SINGLE CHANNEL
GRAPH TYPE	LOG MAGNITUDE (All four channels)
S-PARAMS	USER 1: (Channel 3) Parameter: Ra/1 Phase Lock: Ra USER 2: (Channel 1) Parameter: Ta/1 Phase Lock: Ra USER 3: (Channel 2) Parameter: Tb/1 Phase Lock: Ra USER 4: (Channel 4) Parameter: Rb/1 Phase Lock: Rb (See Figure 3-8)
SET SCALE	RESOLUTION: 20 dB/DIV REF VALUE: 0 dB (All four channels)

Test Setup

Setup 360B VNA as described below.

Step 1. Connect cable between SOURCE LOCK OUTPUT and R_A/ SOURCE LOCK INPUT connectors; connect a second cable between RF OUT and T_A connectors (below).



Step 2. Set up the network analyzer as shown in table at left.

To independently measure the output of the individual test set channels, you must redefine the selected parameter for each display channel. For this test, the parameters need to be redefined as shown below.

$\frac{T_a}{1}$ = Test Set Channel 1, Phase Lock = Ra

$\frac{T_b}{1}$ = Test Set Channel 2, Phase Lock = Ra

$\frac{R_a}{1}$ = Test Set Channel 3, Phase Lock = Ra

$\frac{R_b}{1}$ = Test Set Channel 4, Phase Lock = Rb

Step 1. Press S PARAMS key.

Step 2. Make menu choices as shown in the following flow diagram.

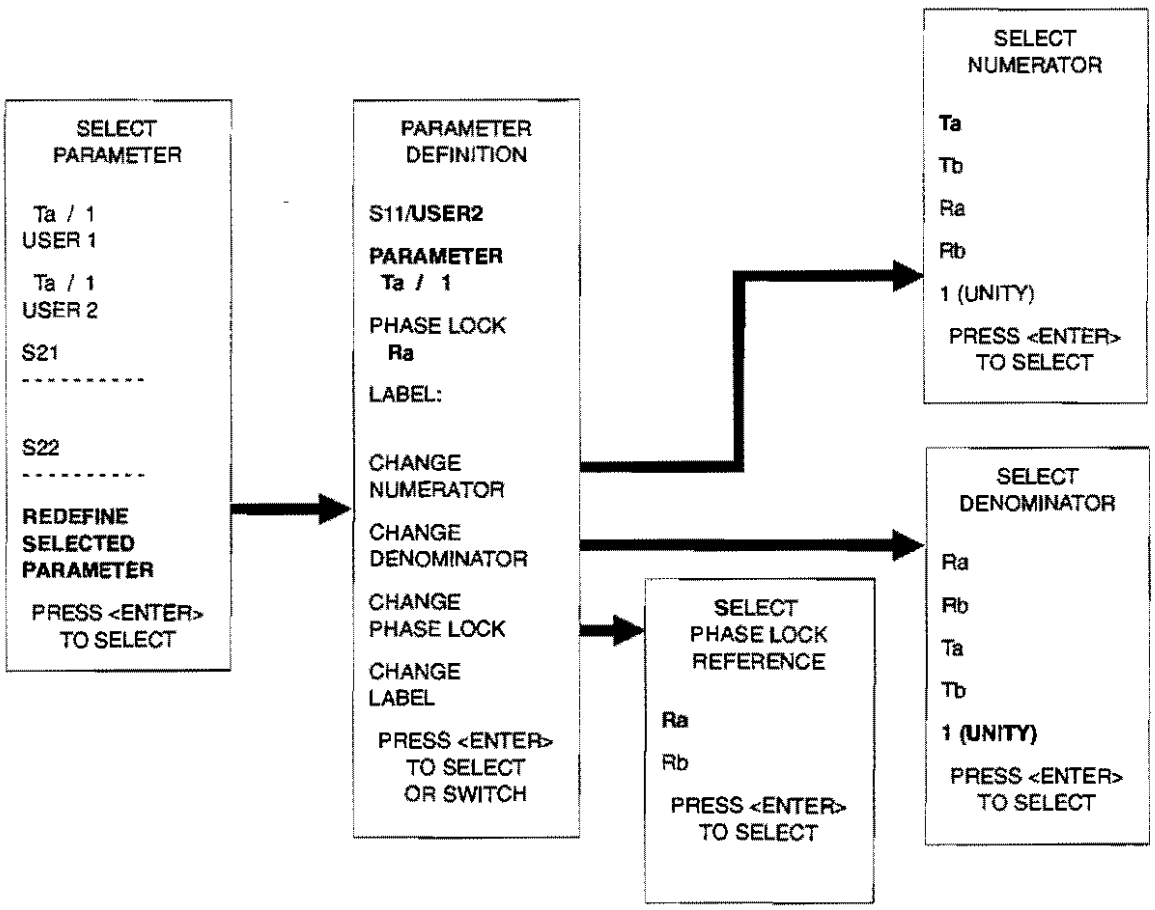


Figure 3-8. *Redefining Selected Parameter for Full-Band Testing*

Test Procedure

Perform test as described below.

Step 1. Press CH 1 key.

Step 2. Observe that trace has power slope similar to that shown in Figure 3-9, and that no power holes (10 dB or greater) exists anywhere on trace.

NOTE

At the conclusion of the test, verify that all four channels exhibit similar slope characteristics.

Step 3. Move cable from connector T_A to connector T_B.

Step 4. Press CH 2 key.

Step 5. Observe that trace has power slope similar to that shown in Figure 3-9, and that no power holes (10 dB or greater) exists anywhere on trace.

Step 6. Press CH 3 key.

Step 7. Observe that trace has power slope similar to that shown in Figure 3-9, and that no power holes (10 dB or greater) exists anywhere on trace.

Step 8. Move cable from connector SOURCE LOCK OUTPUT to connector R_B / SOURCE LOCK INPUT.

Step 9. Press CH 4 key.

Step 10. Observe that trace has power slope similar to that shown in Figure 3-9, and that no power holes (10 dB or greater) exists anywhere on trace.

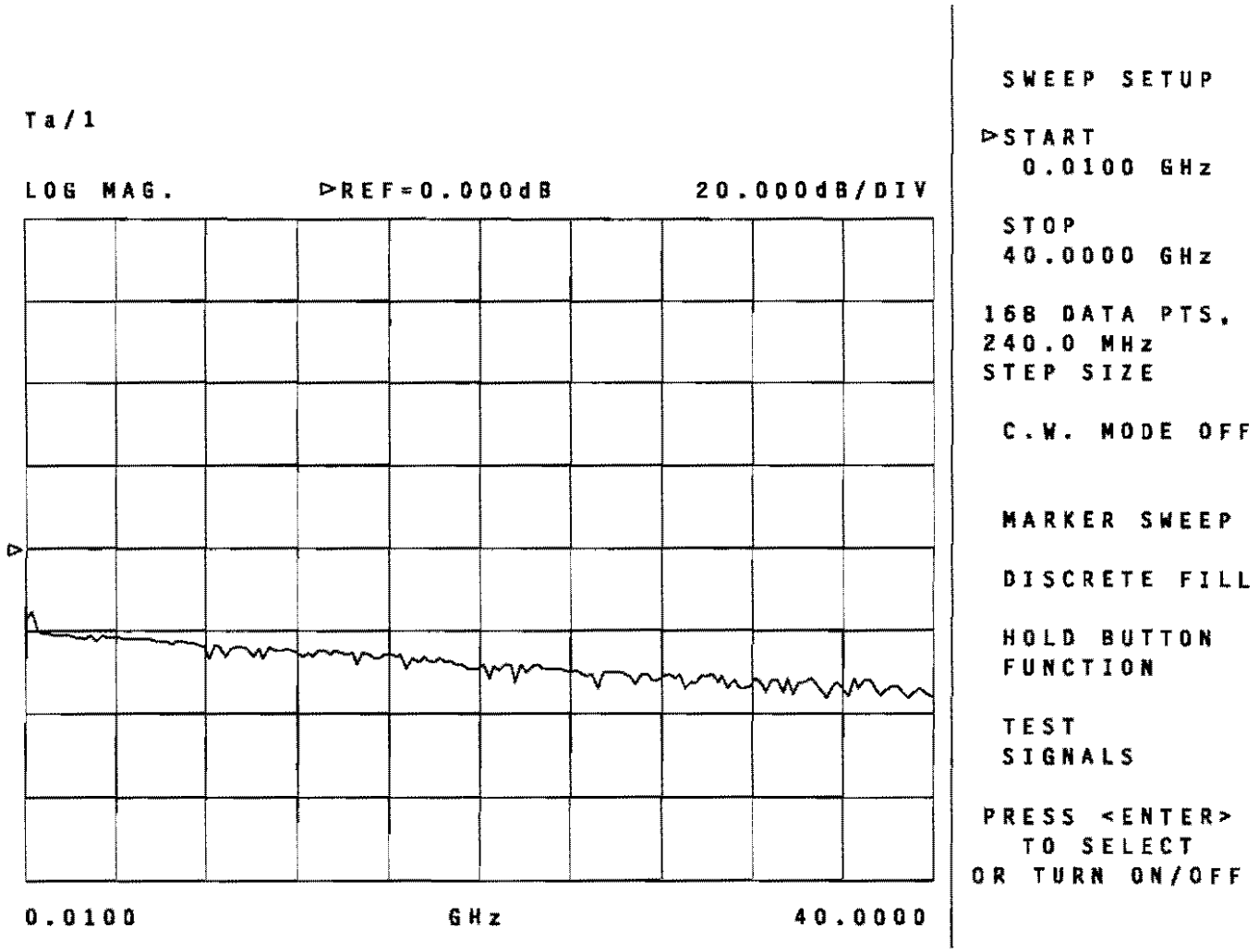


Figure 3-9. *Full-Band Test Waveform*

3-14 SET SOURCE POWER LEVEL, MODELS 3630A/3631A

The following test uses a power meter to calibrate Source output power setting at four frequency points across the 0.01 to 40 or 60 GHz range. The adjusted power settings will be used in later procedures to verify compression setting, noise floor, and magnitude tracking.

Test Setup

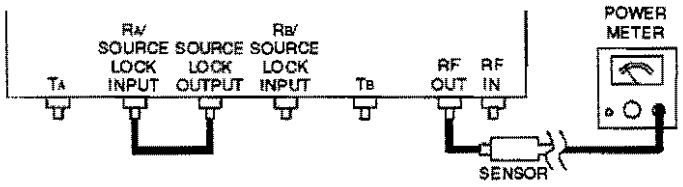
Setup 360B VNA as described below.

Step 1. Connect cable to RF OUT connector; leave other end unterminated.

Step 2. Connect power sensor on power meter to unterminated end of cable connected in Step 1 (below).

Step 3. Connect cable between SOURCE LOCK OUTPUT and RA/SOURCE LOCK INPUT connectors (below).

Test Procedure



Perform test as described below.

Step 1. Press SETUP MENU key.

Step 2. Select **TEST SIGNALS.**

Step 3. Select **SOURCE 1 PWR**, and set level for 5.0 dBm; then select **PREVIOUS MENU.**

Step 4. Move cursor to **C.W. MODE** and press ENTER key.

Step 5. Set CW frequency for 0.01 GHz.

Step 6. Select **TEST SIGNALS.**

Step 7. Move cursor to **SOURCE 1 PWR** when next menu appears, and adjust level for −10 dBm ±0.1 dB, as indicated on power meter.

Table 3-5. *Source 1 Power Settings*

Frequency (GHz)	SOURCE 1 PWR Setting	Typical Setting
0.01		–2.3
1		–2.5
20		0.8
40		3.6
60		

Step 8. Record **SOURCE 1 PWR** setting in Table 3-5.

Step 9. Press SETUP MENU key.

Step 10. Move cursor to **C.W. MODE** and change frequency to 1 GHz.

NOTE

If unable to set frequency to exactly 1 GHz, select **DISCRETE FILL** and select four frequencies per the menu sequence shown in Figure 3-10.

Step 11. Select **TEST SIGNALS.**

Step 12. Select **SOURCE 1 PWR,** and adjust level for –10 dBm ±0.1 dB, as indicated on power meter.

Step 13. Record **SOURCE 1 PWR** setting in Table 3-5.

Step 14. Repeat steps 9 thru 13 for 20 GHz, 40 GHz, and 60 GHz — as applicable.

NOTE

Set Cal Factor on power meter as required for each frequency.

Using the discrete fill feature overrides the default frequency resolution and allows selected fill frequencies to be accurately set using C.W. MODE selection in SETUP menu. To set discrete fill frequencies, proceed as follows.

Step 1. Press SETUP MENU key.

Step 2. Make menu choices and press ENTER key as shown in the following flow diagram.

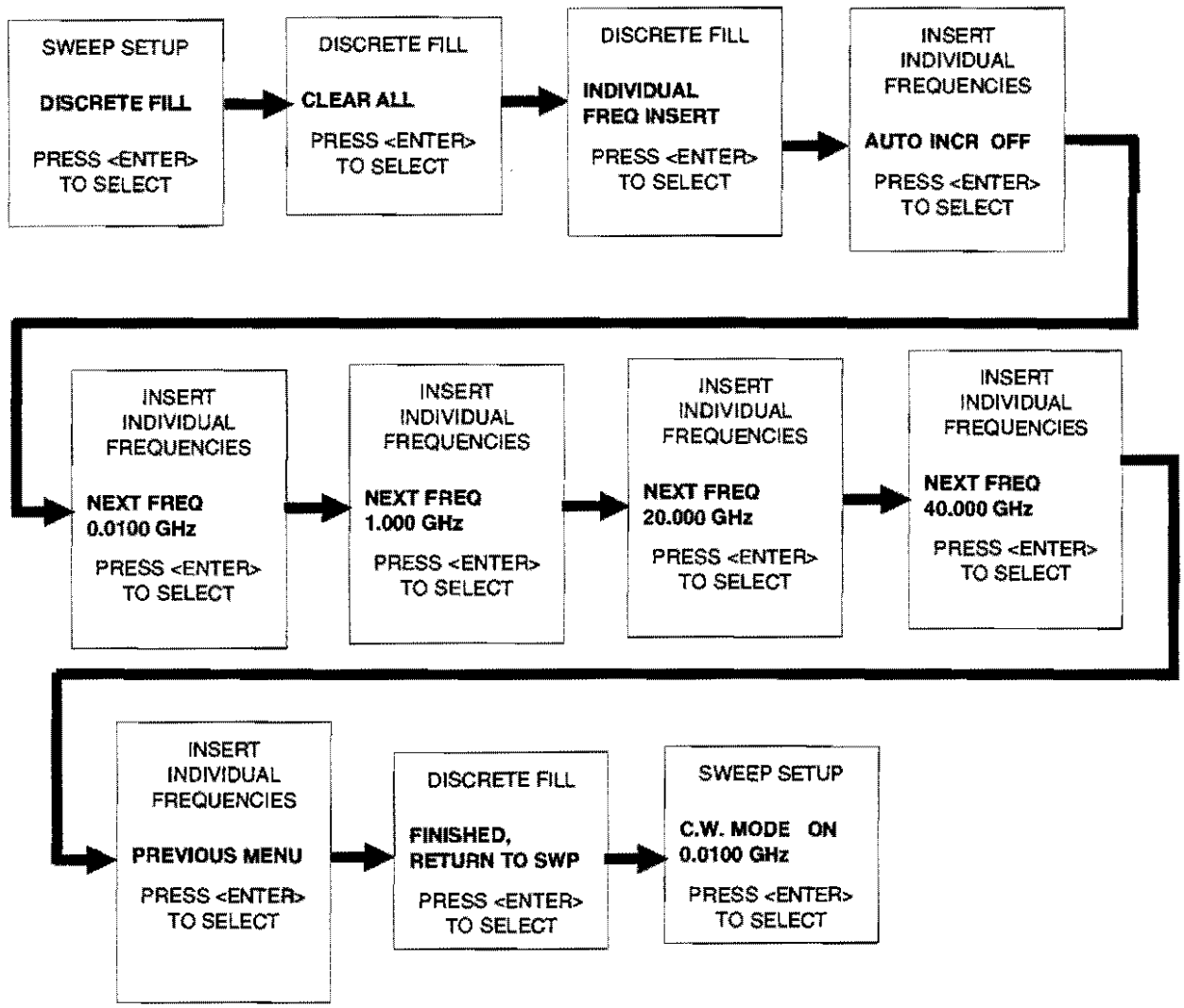
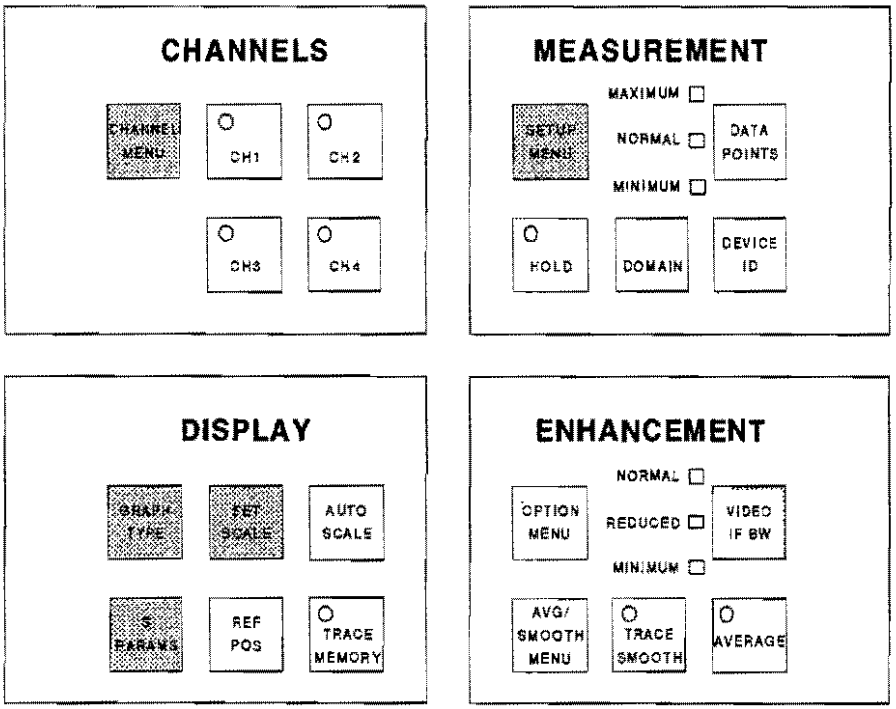


Figure 3-10. Using Discrete Fill Function

3-15 COMPRESSION LEVEL TEST, MODELS 3630A/3631A

This test verifies that the compression level is 0.1 dB or less for a specified power input level.

This test requires that you press specified front panel keys and make choices from the displayed menus. The keys used in this test are shown below and on next page.

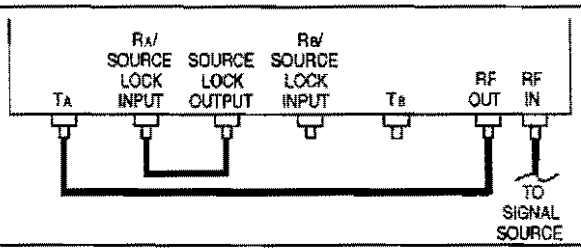


Key	Menu Choice
SETUP MENU	START: 0.01 GHz STOP: High-end frequency
CHANNEL MENU	SINGLE CHANNEL
GRAPH TYPE	LOG MAGNITUDE (Channels 1 and 2)
S-PARAMS	USER 2: (Channel 1) Parameter: Ta/Ra Phase Lock: Ra (See Figure 3-7)
SET SCALE	RESOLUTION: 20 dB/DIV REF VALUE: 0 dB (Channels 1 and 2)
MARKER MENU	MARKER 1 ON

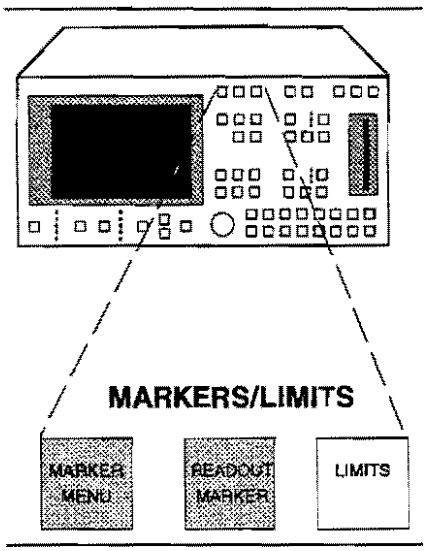
Test Setup

Set up 360B VNA as described below.

Step 1. Connect cable between SOURCE LOCK OUTPUT and R_A / SOURCE LOCK INPUT connectors; connect a second cable between RF OUT and T_A connectors (below).



Step 2. Set up network analyzer as shown in table at left.



Test Procedure

Perform the test procedure as described below.

Step 1. Press SETUP MENU key.

Step 2. Move cursor to **C.W. MODE** and enter **0.010 GHz.**

Step 3. Select **TEST SIGNALS;** then set **SOURCE 1 PWR** to 5 dB below the level recorded for 0.01 GHz in Table 3-5, on page 3-39. *However,* if the calculated level is lower than –7.0, set power to –7.0.

Example:
Table 3-5 level: –2.3 dBm.
Set power to –7.0 dBm
(–2.3) – (–5) = –7.3,
which is less than –7.0.

Step 4. Press TRACE MEMORY key.

Step 5. Select in turn **VIEW DATA** and wait one complete sweep, **STORE DATA TO MEMORY,** then **VIEW DATA ÷ MEMORY.**

Step 6. Press SETUP MENU key, select **TEST SIGNALS,** then raise power level to that recorded for 0.01 GHz in Table 3-5 (–2.3 dBm for the *Example*).

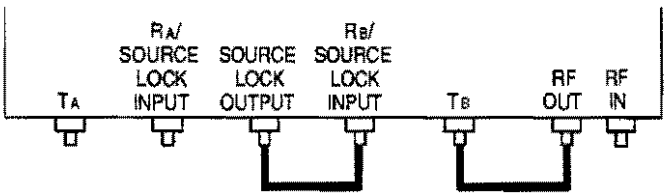
Step 7. Press READOUT MARKER key (top left), and record value in the appropriate column of Table 3-6. The readout value should be less than 0.1 dB.

Step 8. Repeat steps 1 thru 7 for 1, 20, 40, and 60 GHz — as applicable.

Table 3-6. *Compression Level for Channel T_A*

Frequency (GHz)	READOUT MARKER (dBm)	Typical Setting (dBm)
0.01		–0.02
1		–0.08
20		–0.05
40		–0.07
60		

Step 9. Connect cable between SOURCE LOCK OUTPUT and R_B / SOURCE LOCK INPUT connectors; connect a second cable between RF OUT and T_B connectors (below).



Step 10. Press CH 2 key.

Step 11. Press S PARAMS key.

Step 12. Select **USER 3** and set user-defined parameters to **Tb/Rb** and Phase Lock to **Rb.**

Step 13. Repeat steps 7 thru 12 for the four frequencies in Table 3-7 . Use this table to record READOUT MARKER key values.

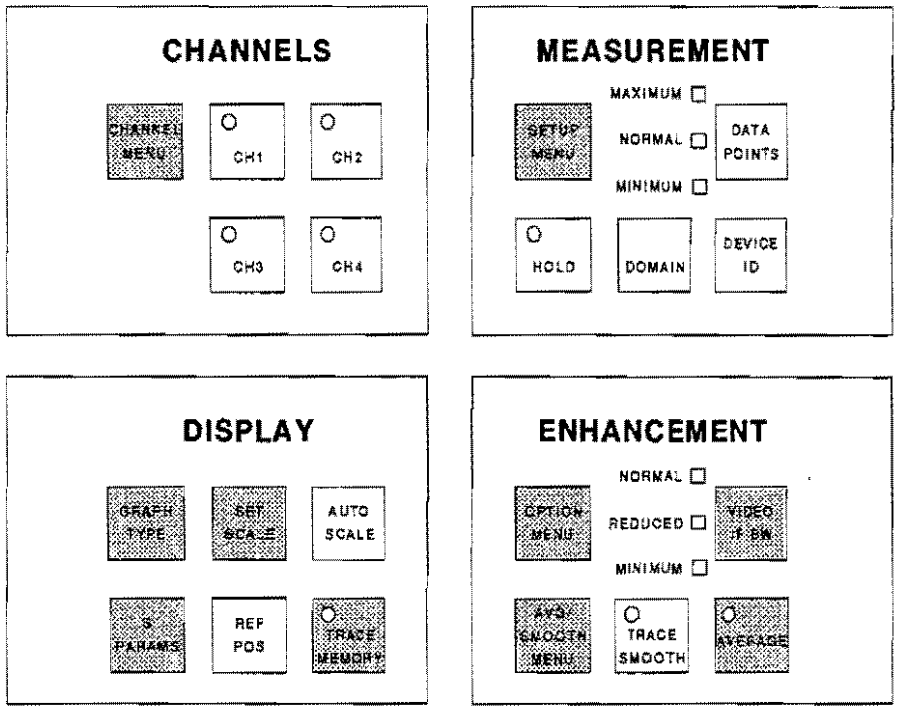
Table 3-7. *Compression Level for Channel T_B*

Frequency (GHz)	READOUT MARKER (dBm)	Typical Setting (dBm)
0.01		–0.02
1		–0.04
20		–0.05
40		–0.07
60		

3-16 NOISE FLOOR/ RECEIVER DYNAMIC RANGE TEST, MODELS 3630A/3631A

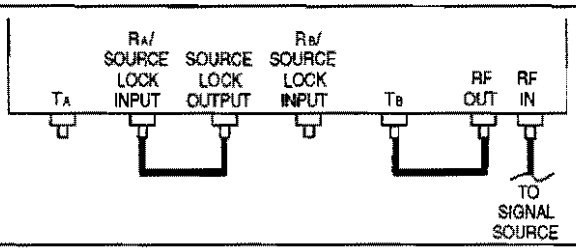
This test verifies that the noise floor meets the guaranteed performance specifications.

This test requires that you press specified front panel keys and make choices from the displayed menus. The keys used in this test are shown below and on next page.



Test Setup Set up 360B VNA as described below.

Step 1. Connect cable between SOURCE LOCK OUTPUT and R_A / SOURCE LOCK INPUT connectors; connect a second cable between RF OUT and T_B connectors (below).



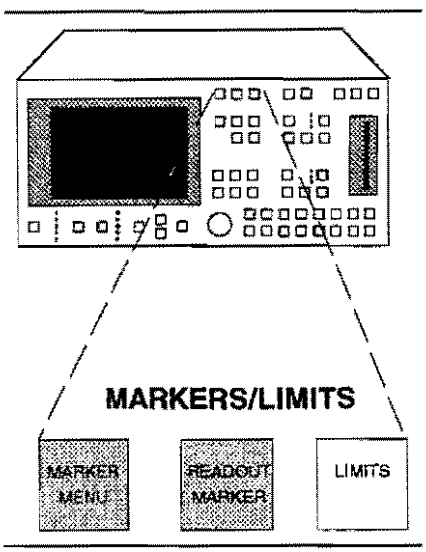
Key	Menu Choice
SETUP MENU	START: 0.01 GHz STOP: 40.0 GHz
CHANNEL MENU	SINGLE CHANNEL
S-PARAMS	S21 (Channel 1) (Parameter: Tb/Ra Phase Lock: Ra)

Step 2. Set up network analyzer as shown in table at left.

Test Procedure

Perform the test procedure as described below.

Key	Menu Choice
GRAPH TYPE	LOG MAGNITUDE
SET SCALE	RESOLUTION: 20 dB/DIV REF VALUE: –80 dB
OPTION MENU	SWEEP OPTIONS; then POINTS DRAWN IN C.W. 20
AVG/ SMOOTH MENU	AVERAGING: 1024 MEAS. PER POINT
AVERAGE	ON
VIDEO IF BW	MINIMUM



Step 1. Press the BEGIN CAL key.

Step 2. Select from displayed prompts to perform a **STANDARD, COAXIAL, FREQUENCY RESPONSE ONLY, TRANSMISSION** calibration at 0.010 GHz.

Step 3. When the CONFIRM CALIBRATION PARAMETERS menu appears, select **TEST SIGNALS.**

Step 4. Set the **SOURCE 1 PWR** selection to the power level recorded in Table 3-5, page 3-39, for the applicable frequency; then select **RESUME CAL.**

Step 5. Follow the displayed prompts to complete the calibration.

Step 6. Disconnect the cable from T_B; connect 50Ω termination to connectors T_B and the end of the cable connected to RF OUT.

Step 7. Set up network analyzer as shown in table at top left.

Step 8. Press TRACE MEMORY key.

Step 9. Select in turn **VIEW DATA** and wait one complete sweep, **STORE DATA TO MEMORY,** then **VIEW DATA – MEMORY.**

NOTE
Use **SELECT TRACE MATH** menu option to change to **VIEW DATA – MEMORY.**

Step 10. Allow one full sweep to occur, then press the HOLD key.

Step 11. Press MARKER MENU key (bottom left) and enable **MARKER 1.**

Step 12. Press READOUT MARKER key (bottom left), select **MARKER TO MAX** and record value in the "Dynamic Range" column of Table 3-8.

Table 3-8. *Dynamic Range Measurement and Specification*

Frequency (GHz)	Dynamic Range (dB)	Specification (dBm)	
		3630A	3631A
0.01		–107	–107
1		–107	–107
20		–105	–105
40		–97	–97
60			–77

Step 13. Repeat steps 1 thru 12 for 1, 20, 40, and 60 GHz, as applicable.

Step 14. Calculate the noise floor and record it in Table 3-9. The formula is

$$Noise\ Floor\ (dBm) = (-10\ dBm^{*}) - Dynamic\ Range\ (dB)$$

NOTE

–10 dBm is the power level of the signal applied to the T_B input connector. This value is then used to derive the noise floor in absolute power units (dBm).

Table 3-9. *Noise Floor Measurement and Specification*

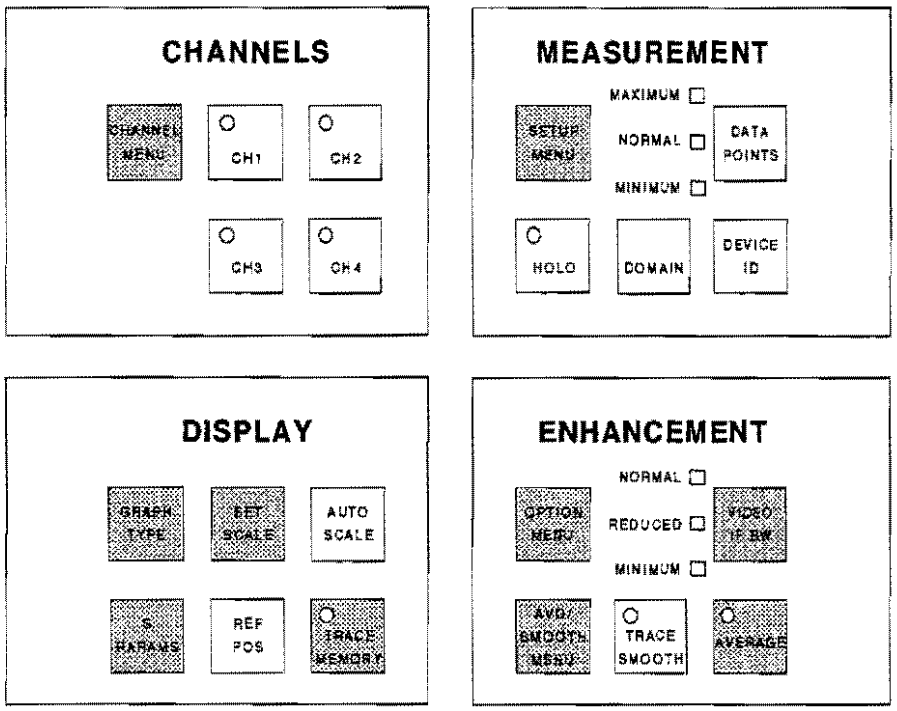
Frequency (GHz)	Noise Floor (dBm)	Specification (dBm)	
		3630A	3631A
0.01		–117	–117
1		–117	–117
20		–115	–115
40		–107	–107
60			–90

3-17 MAGNITUDE TRACKING TEST, MODELS 3630A/3631A

This test checks the tracking of the Port 2 Source step-attenuator and the resulting signal level. There is no specification for this signal level.

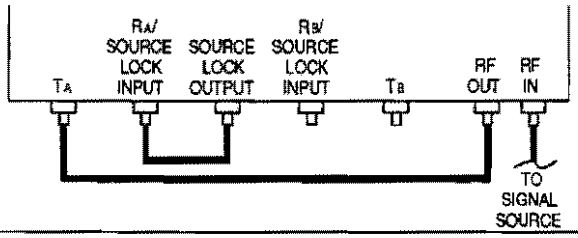
This test requires that you press specified front panel keys and make choices from the displayed menus. The keys used in this test are shown below and on next page.

Key	Menu Choice
SETUP MENU	START: 0.01 GHz STOP: 40.0 GHz
CHANNEL MENU	SINGLE CHANNEL
GRAPH TYPE	LOG MAGNITUDE
S-PARAMS	USER 2: (Channel 1) Parameter: Ta/Ra Phase Lock: Ra (See Figure 3-8)
SET SCALE	RESOLUTION: 20 dB/DIV REF VALUE: 0 dB
MARKER MENU	MARKER 1 ON POINT 4
OPTIONS	SWEEP OPTIONS; then POINTS DRAWN IN C.W. 20
AVG/ SMOOTH MENU	AVERAGING: 100 MEAS. PER POINT
AVERAGING	ON
VIDEO IF BW	MINIMUM



Test Setup Set up 360B VNA as described below.

Step 1. Connect cable between SOURCE LOCK OUTPUT and R_A / SOURCE LOCK INPUT connectors; connect a second cable between RF OUT and T_A connectors (below).



Step 2. Set up network analyzer as shown in table at left.

Table 3-10. *Port 2 Source Tracking, Signals T_A and R_A*

Frequency (GHz)	Port 2 Source (dB)	Signal Level		
		Ta/Ra	Tb/Ra	Rb/Ra
0.01	0	0	0	0
	20			
	40			
	60			
1.0	0	0	0	0
	20			
	40			
	60			
20	0	0	0	0
	20			
	40			
	60			
40	0	0	0	0
	20			
	40			
	60			
60	0	0	0	0
	20			
	40			
	60			

Test Procedure

Perform the test procedure as described below.

Step 1. Press SETUP MENU key.

Step 2. Move cursor to **C.W. MODE** and enter **0.010 GHz.**

Step 3. Select **TEST SIGNALS;** then set **PORT 2 SOURCE** to 0 dB.

Step 4. Press TRACE MEMORY key.

Step 5. Select in turn **VIEW DATA, STORE DATA TO MEMORY,** then **VIEW DATA + MEMORY.**

Step 6. Press SETUP MENU key.

Step 7. Select **TEST SIGNALS;** then set **PORT 2 SOURCE**step attenuator value to 20 dB.

Step 8. Press READOUT MARKER key (left), and record value in the appropriate column of Table 3-10.

Step 9. Repeat steps 6 thru 8 for 40 and 60 dB settings in Table 3-10.

Step 10. Repeat steps 1 thru 9 for remaining, applicable, Ta/Ra frequency and Port 2 Source settings in Table 3-10.

Step 11. Connect cable between RF OUT and T_B connectors.

Step 12. Press S PARAMS key and change user parameter setting to Tb/Ra.

Step 13. Repeat steps 1 thru 9 for applicable Tb/Ra frequency and Port 2 Source step attenuator settings in Table 3-10.

Step 14. Connect cable between RF OUT and Rb/SOURCE LOCK INPUT connectors.

Step 15. Press S PARAMS key and change user parameter setting to Rb/Ra.

Step 16. Repeat steps 1 thru 9 for applicable Rb/Ra frequency and Port 2 Source step attenuator settings in Table 3-10.

3-18 ADJUSTMENTS, MODELS 3630A/3631A

The only adjustments that can be performed in the field are to the A5T LO1 PCB and the A4T LO2 PCB. A detailed procedure for adjusting these two PCBs is provided in paragraph 3-11 for the Models 361XA/362XA Test Sets. Refer to that procedure for adjustment instructions.

Table 3-8. *Dynamic Range Measurement and Specification*

Frequency (GHz)	Dynamic Range (dB)	Specification (dBm)	
		3630A	3631A
0.01		102	107
1		102	107
10		98	107
20		98	105
30		87	105
40		87	97
50			85
60			80

Table 3-9. *Noise Floor Measurement and Specification*

Frequency (GHz)	Noise Floor (dBm)	Specification (dBm)	
		3630A	3631A
0.01		–112	–117
1		–112	–117
10		–108	–117
20		–108	–115
30		–108	–115
40		–97	–107
50			–95
60			–90

Step 11. Press MARKER MENU key (bottom left) and enable **MARKER 1.**

Step 12. Press READOUT MARKER key (bottom left), select **MARKER TO MAX** and record value in the "Dynamic Range" column of Table 3-8.

Step 13. Repeat steps 1 thru 12 for 1, 20, 40, and 60 GHz, as applicable.

Step 14. Calculate the noise floor and record it in Table 3-9. The formula is

$$Noise\ Floor\ (dBm) = (-10\ dBm*) - Dynamic\ Range\ (dB)$$

NOTE

-10 dBm is the power level of the signal applied to the T_B input connector. This value is then used to derive the noise floor in absolute power units (dBm).

3-19 PERFORMANCE TESTS, MODELS 3635B/364XB MODULES

This tab section contains five performance tests that can be used to verify Model 360B VNA mm-wave system operation. Setup instructions and performance procedures are included for each test. Test results can be compared with the specified limits that are provided for each test.

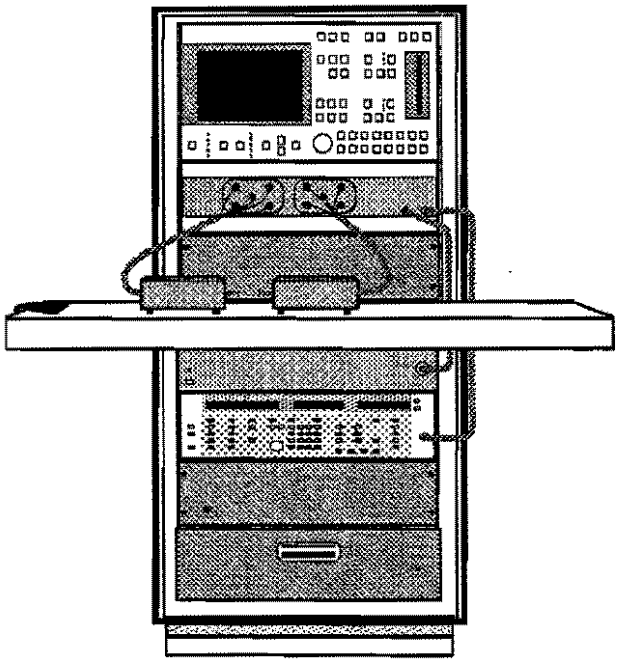
These tests do not establish measurement traceability; such verification requires using an appropriate WILTRON verification kit. Successful completion of these procedures indicates that your 360B mm-wave system is operating properly and is capable of making accurate measurements.

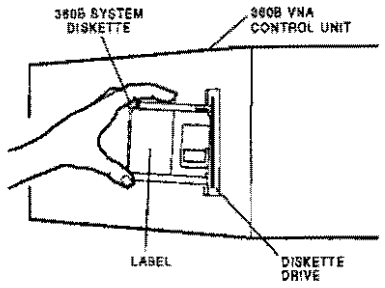
Required Equipment

The following equipment is required to perform the operation verification tests:

- ☐ Calibration kit, with Option 1: Sliding Termination.

Initial System Setup





Perform the following steps before starting the performance tests.

Step 1. Verify that the 360B VNA system has been installed correctly, per the 360B Operation Manual (P/N 10410-00110), Chapter 2.

Step 2. Install the precision-straight waveguide sections that are contained in the calibration kit on the waveguide output connector of each mm-wave module.

NOTE

These waveguide sections (test port adapters) use high precision flanges to improve connection repeatability and calibration quality. They *must* be used to ensure specified system performance.

Step 3. Install the 360B VNA system diskette into the disk drive of the network analyzer.

Step 4. Apply power to the frequency signal sources then to the network analyzer. Loading of the system software takes approximately 1 minute (at which time the system is ready to make measurements).

Step 5. Press the SETUP MENU key, select **WR & PORT MODEL NUMBERS**, and configure your system for the types of microwave modules installed.

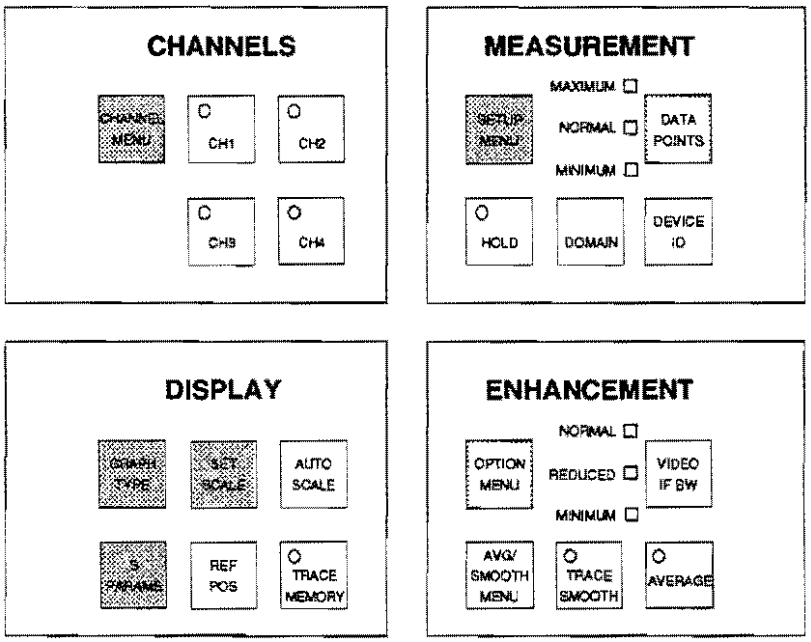
NOTE

Allow the system to warm up for at least 60 minutes to ensure operation to performance specifications.

3-20 NON-RATIOED POWER LEVEL TEST MODELS 3635B/364X

This test verifies that each individual receiver channel operates properly. Measurement calibration of the system is *not* required for this test.

This test requires that you press a specified front panel key and make choices from the displayed menu(s). The keys used in this test are shown below.

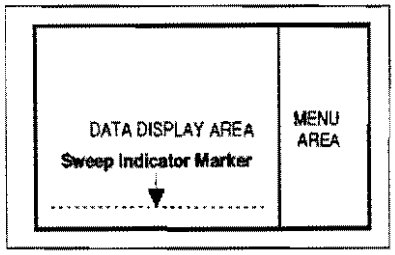


Key	Menu Choice
SETUP MENU	START: Low-end Freq STOP: High-end Freq
CHANNEL MENU	DUAL CHANNEL 1-3
GRAPH TYPE	LOG MAGNITUDE (Both channels)
S-PARAMS	Channel 1: a1/1 Channel 3: b1/1 (See Figure 3-1, page 3-7)
SET SCALE	RESOLUTION: 3.0 dB/DIV REF VALUE –10.0 dB (Both channels)
LIMITS	LIMIT 1 ON 0.000 dB LIMIT 2 ON –20.0 dB (Both channels)

Test Setup Setup 360B VNA as described below.

Step 1. Install a flush short on the output of the 3640B-X module connected to PORT 1.

Step 2. Set up the network analyzer as shown in table at left.



Key	Menu Choice
CHANNEL MENU	DUAL CHANNEL 2-4
S-PARAMS	USER DEFINED: Channel 2 for b2/1 and Channel 4 for a2/1.

Key	Menu Choice
CH 3	ON
CHANNEL MENU	SINGLE CHANNEL
S-PARAMS	USER DEFINED: Channel 3 for b2/1.

Test Procedure

Perform test as described below.

Step 1. Observe sweep indicator (top left) and allow at least one complete sweep to occur.

Step 2. Verify that the measurement traces fall within the limit line (Figure 3-10).

Step 3. If the second module to be tested is also a Model 3640B-X Transmission/Reflection module, change setup to that shown at middle left and perform step 4 (otherwise skip to step 6):

Step 4. Install a flush short to the output of the 3640B module on PORT 2 .

Step 5. Verify that the measurement traces fall within the limit lines.

Step 6. If the second module to be tested is a Model 3641B-X, connect the two modules together and change the setup to that shown at bottom left.

Step 7. Verify that the measurement trace falls below the limit line (Figure 3-11).

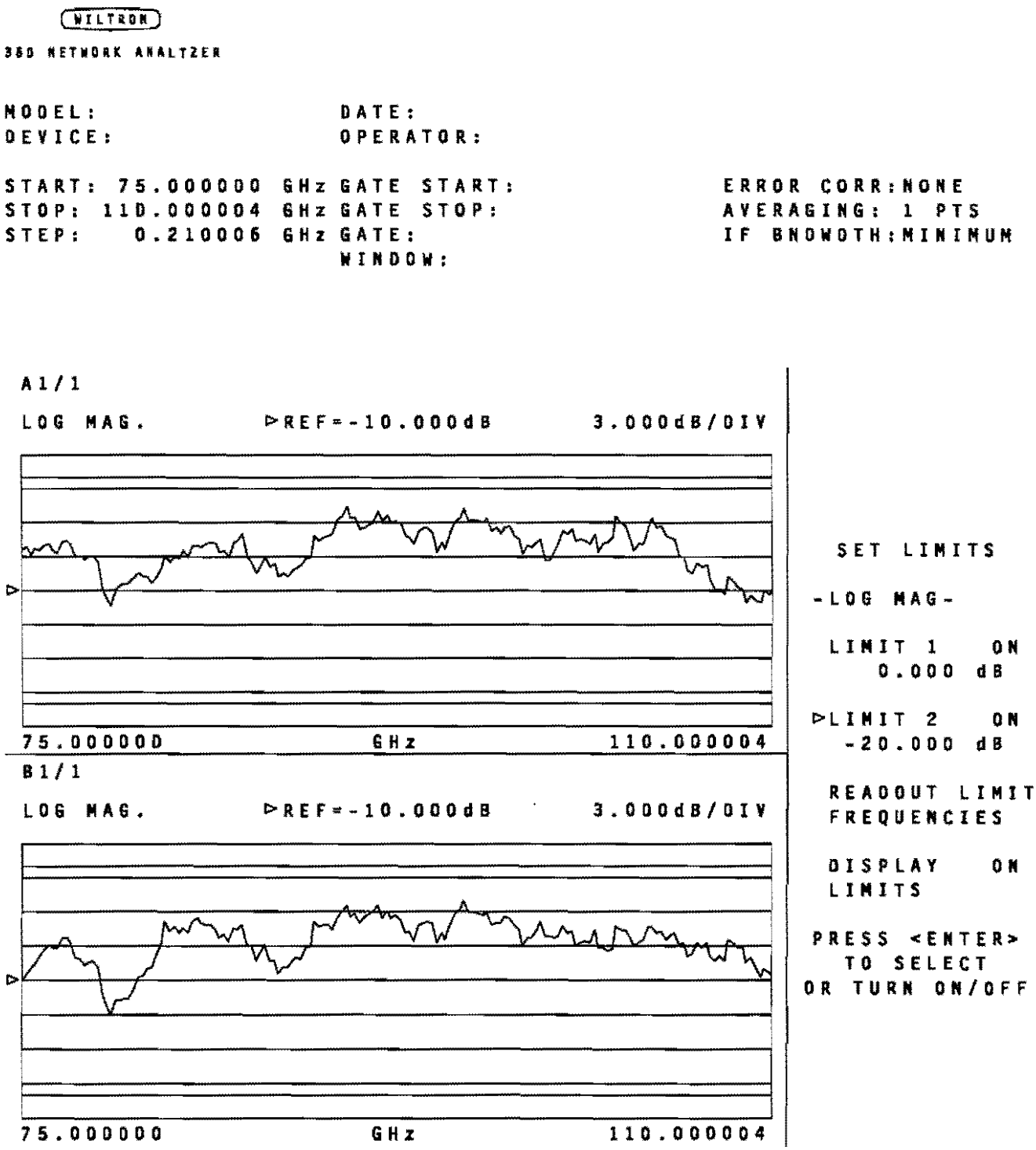


Figure 3-10. *Non-Ratioed Power Level Test Dual Channel Waveform for a 3640B-X Module*

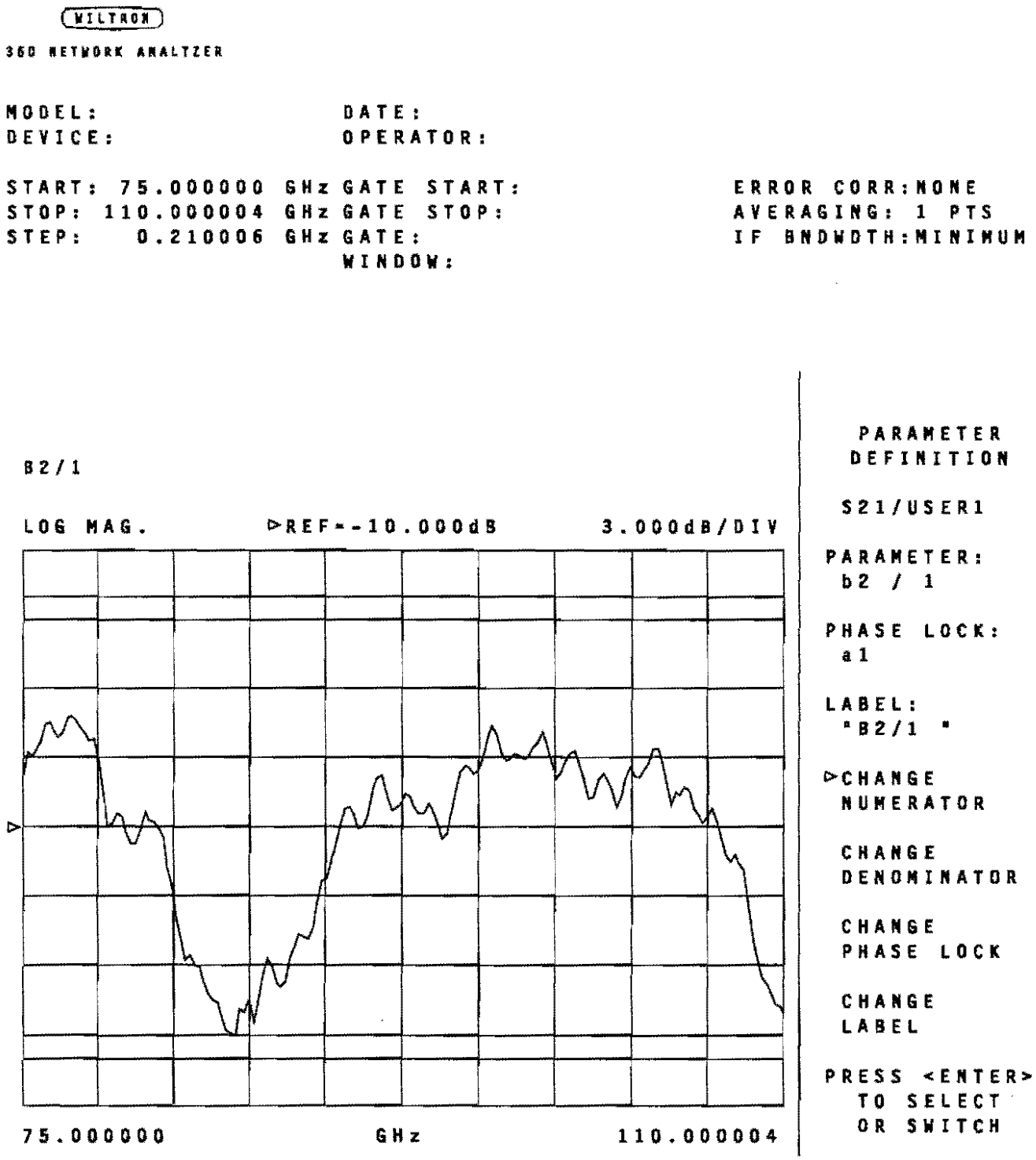


Figure 3-11. *Non-Ratioed Power Level Test Single Channel Waveform for a 3640B / 3641B Module Set*

3-21 HIGH LEVEL NOISE TEST, MODELS 3635B/364X

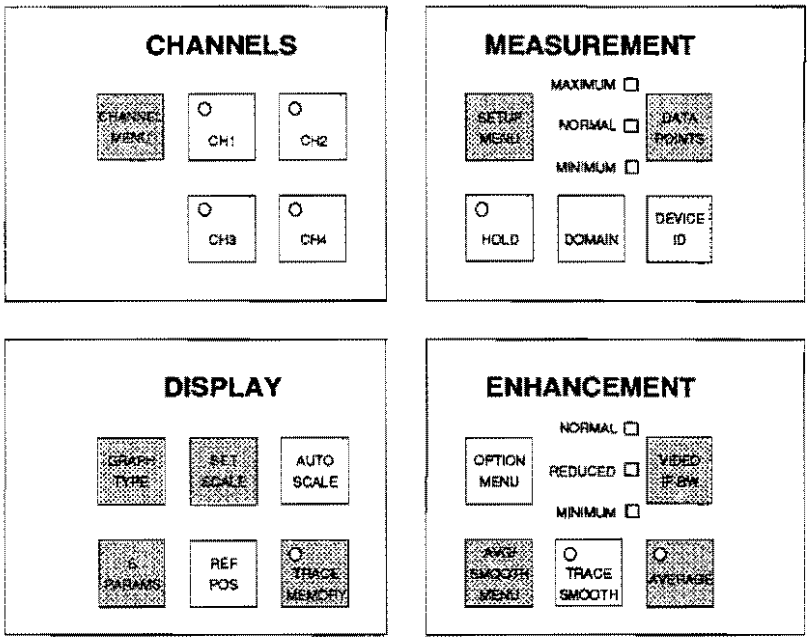
The following test verifies that the high-level noise in the 360B VNA will not significantly affect the accuracy of subsequent measurements. High-level noise is the random noise that exists in the 360B VNA System. Because it is non-systematic, it cannot be accurately predicted or measured. Thus, it cannot be removed using conventional error-correction techniques. Calibration of the system is *not* required for this test.

NOTE

This test is not applicable if you are only using a single 3640B-X module on Port 1.

This test requires that you press a specified front panel key and make choices from the displayed menu(s). The keys used in this test are shown below.

Key	Menu Choice
SETUP MENU	START: Low-end freq. STOP: High-end freq.
CHANNEL MENU	DUAL CHANNELS 1-3 (two 3640B-Xs) SINGLE CHANNEL 3 (One 3640B-X and one 3641B-X)
GRAPH TYPE	LOG MAGNITUDE (Both channels)
SET SCALE	RESOLUTION: 0.050 dB/DIV REF VALUE: 0.0 dB (Both channels)
S-PARAMS	Channel 1 – S_{12} Channel 3 – S_{21}
AVG/ SMOOTH MENU	AVERAGING 128 MEAS. PER POINT
AVERAGE	ON
DATA POINTS	NORMAL
VIDEO IF BW	REDUCED
LIMITS	LIMIT 1 ON 0.030 dB (Q Band) 0.040 dB (U Band) 0.060 dB (V Band) 0.070 dB (W Band) LIMIT 2 ON –0.030 dB (Q Band) –0.040 dB (U Band) –0.060 dB (V Band) –0.070 dB (W Band)



Test Setup Setup the 360B as shown at left.

Test Procedure

Perform test as described below.

Step 1. Connect the two modules together.

Step 2. If using two 3640B-Xs, press CH 1 key and perform steps 3 through 9. Otherwise, skip to step 10.

Step 3. Press TRACE MEMORY key.

Step 4. Choose **VIEW DATA** from menu and press ENTER key.

Step 5. While observing sweep indicator (left), allow at least two complete sweeps to occur. (One complete sweep, if using single channel display.)

Step 6. Choose **STORE DATA TO MEMORY** from menu and press ENTER key.

Step 7. Choose **VIEW DATA ÷ MEMORY** from menu and press ENTER key.

Step 8. While observing sweep indicator (top left), allow at least two complete sweeps to occur. (One complete sweep, if using single channel display.)

Step 9. Verify that the peak-to-peak High Level Noise falls within the area between the two limit lines (Figures 3-12 and 3-13).

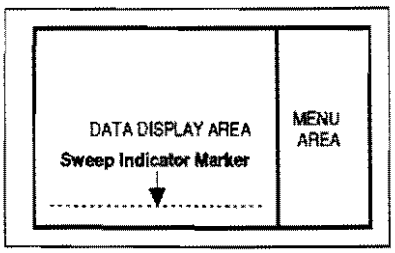
Step 10. Press CH 3 key.

Step 11. Repeat steps 4 thru 9 for channel 3.

Step 12. Change setup as shown in table at bottom left.

Step 13. Attach flush short to waveguide port on 3640B-X on PORT 1 (and PORT 2, if two are used); leave waveguide port on 3641B-X unterminated.

Step 14. Repeat steps 2 thru 9.



Key	Menu Choice
S-PARAMS	Channel 1: S_{11} (One 3640B-Xandone3641B-X) Channel 3: S_{22} (two 3640B-Xs)
SET SCALE	RESOLUTION: 0.050 dB/DIV REF VALUE: 0.0 dB (Both channels)
LIMITS	LIMIT 1 ON 0.010 dB (Q Band) 0.010 dB (U Band) 0.030 dB (V Band) 0.040 dB (W Band) LIMIT 2 ON –0.010 dB (Q Band) –0.010 dB (U Band) –0.030 dB (V Band) –0.040 dB (W Band)

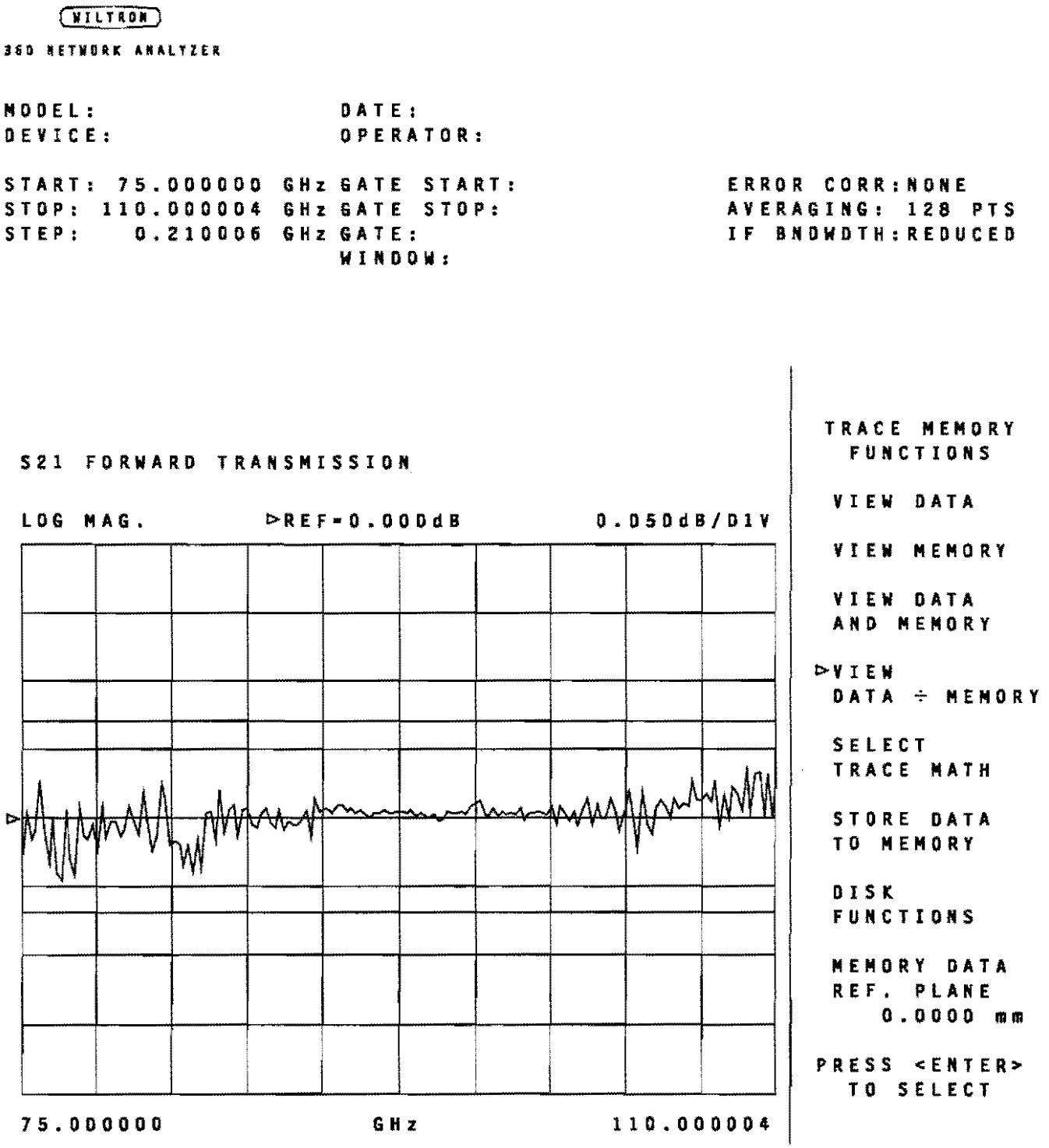


Figure 3-12. *High Level Noise Test, S_{21} Forward Transmission*

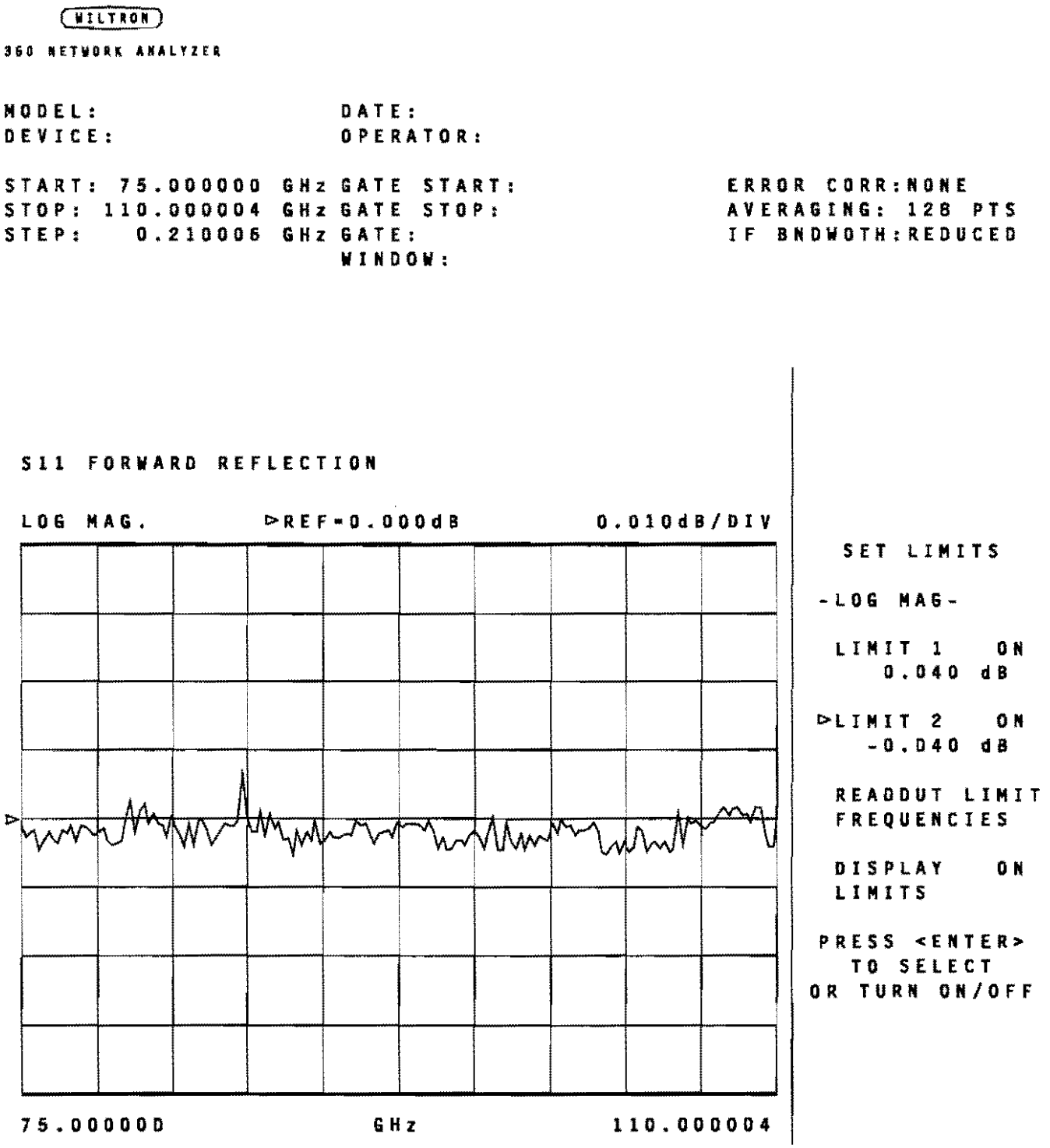


Figure 3-13. *High Level Noise Test, S_{11} Forward Reflection*

3-22 SYSTEM DYNAMIC RANGE TEST, MODELS 3635B/364XB

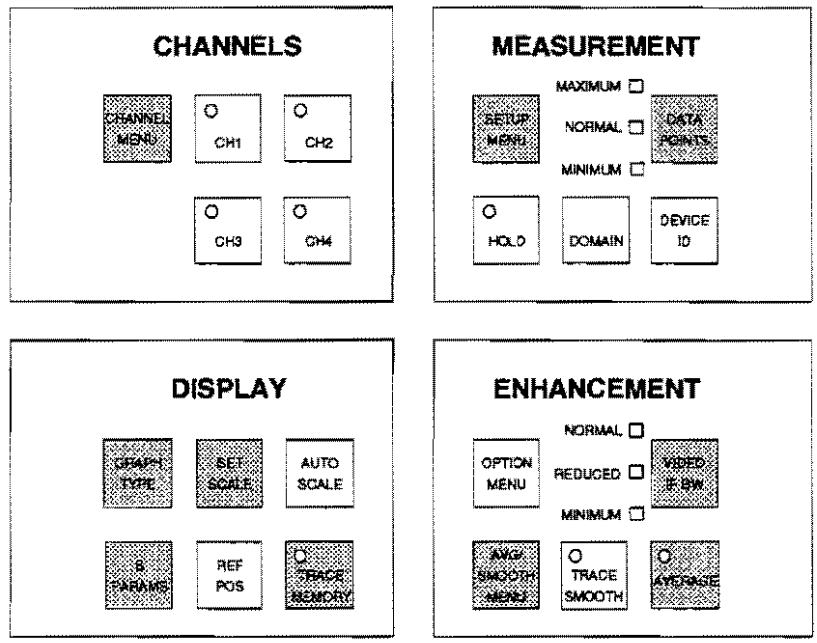
This test verifies that the system meets its dynamic range specifications. Dynamic range is defined as the ratio of the power incident on Port 2 in a through line connection to the noise floor at Port 2. This definition differs slightly from the classical definition of available receiver dynamic range, which takes into account the maximum signal level at Port 2 for 0.1 dB compression.

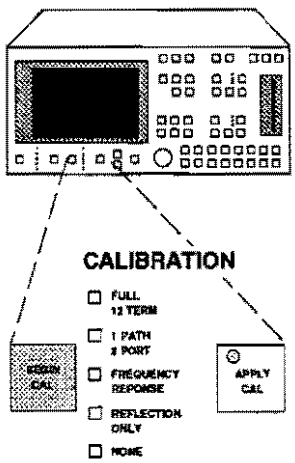
For this test, the system *must* be calibrated and the error correction *must be applied* for this test to be valid.

NOTE

This test is not applicable if you are only using a single 3640B-X module on Port 1.

This test requires that you press a specified front panel key and make choices from the displayed menu(s). The keys used in this test are shown below.





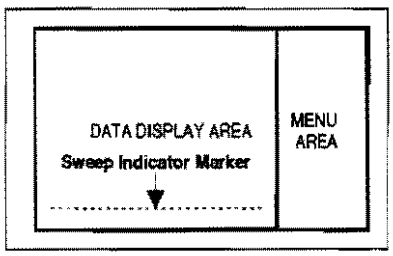
Test Setup Perform the test setup procedures, as described below.

Step 1. Press BEGIN CAL key (left).

NOTE

In step 2, use 12-term calibration if two 3640B-Xs are installed; otherwise, use 1 PATH 2 PORT (8-term) calibration.

Key	Menu Choice
SETUP MENU	START: Low-end freq. STOP: High-end freq.
CHANNEL MENU	DUAL CHANNELS 1-3 (two 3640B-Xs) SINGLE CHANNEL 3 (One 3640B-X and one 3641B-X)
GRAPH TYPE	LOG MAGNITUDE (Both channels)
SET SCALE	RESOLUTION: 20 dB/DIV REF VALUE: 0.0 dB REFERENCE LINE: TOP (Both channels)
S-PARAMS	Channel 1 – S_{12} Channel 3 – S_{21}
AVG/ SMOOTH MENU	AVERAGING 1024 MEAS. PER POINT
AVERAGE	ON
DATA POINTS	NORMAL
VIDEO IF BW	MINIMUM
LIMITS	LIMIT 1 ON –98 dB (Q Band) –97 dB (U Band) –90 dB (V Band) –80 dB (W Band)



Test Procedure

Step 2. Using the menu prompts, perform a 12-or 8-term **SLIDING LOAD** calibration over the full system operating range. (If necessary, refer to the 360B OM, Chapter 8, for detailed procedures.)

Step 3. Before pressing the ENTER key at the **BROADBAND LOAD** menu prompt, press the AVG/SMOOTH MENU key and change averaging to **1024 MEAS. PER POINT**; then press the AVERAGE key to turn averaging on.

Step 4. When the broadband measurement is complete, press the AVG/SMOOTH MENU key and change averaging to **32 MEAS. PER POINT**; continue the calibration.

Step 5. Ensure that the APPLY CAL key indicator is on.

Step 6. Set up the network analyzer as shown in the table at top left.

Perform the test procedure as described below.

Step 1. Attach a flush short to the PORT 1 module waveguide output.

Step 2. Connect a precision termination to the PORT 2 module waveguide output (if applicable).

Step 3. While observing sweep indicator (bottom left), allow at least one complete sweep to occur.

Step 4. Verify that the trace falls below the limit line at all frequencies (Figure 3-14).

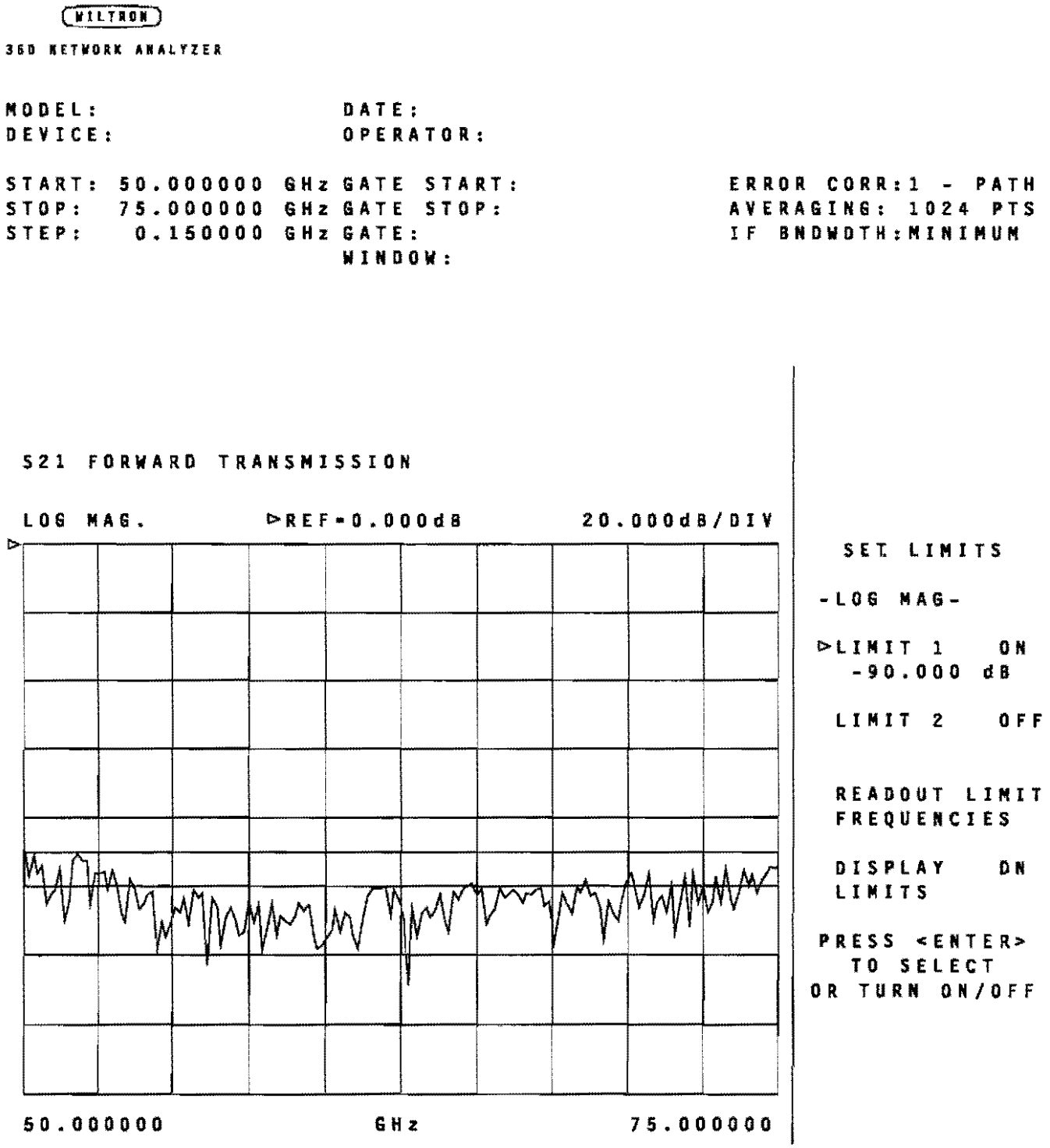


Figure 3-14. *System Dynamic Range Test Waveform*

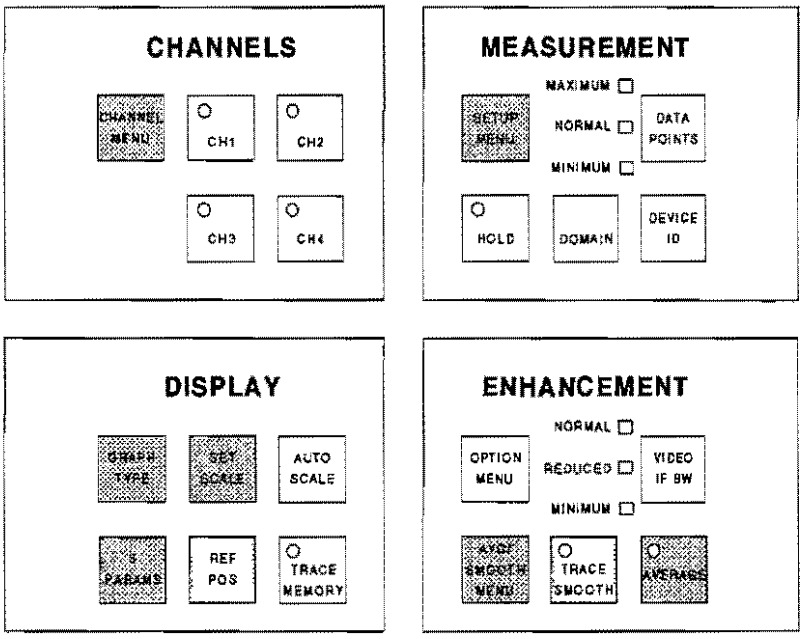
3-23 SOURCE MATCH/ DIRECTIVITY TEST, MODELS 3635B/364XB

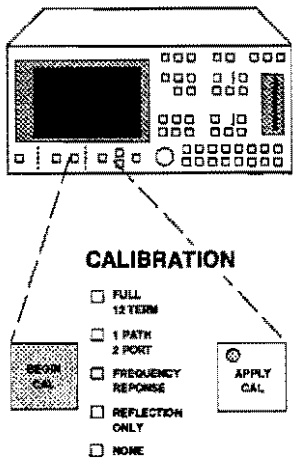
This test verifies that the source match and directivity of the system meet specifications. The system *must* be calibrated and the error correction *must be applied* for these tests.

NOTE

This test is not applicable if you are only using a single 3640B-X module on Port 1.

This test requires that you press a specified front panel keys and make choices from the displayed menu(s). The keys used in this test are shown below.





Test Setup Perform the test setup procedures, as described below.

NOTE

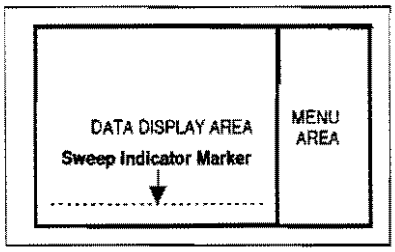
If measurement calibration is valid, skip to step 5.

Step 1. Press BEGIN CAL key (left).

NOTE

In step 2, use 12-term calibration if two 3640B-Xs are installed; otherwises, use reflection-only calibration.

Key	Menu Choice
SETUP MENU	START: Low-end freq. STOP: High-end freq.
CHANNEL MENU	SINGLE CHANNEL Channel 1
GRAPH TYPE	LOG MAGNITUDE
SET SCALE	RESOLUTION: 0.0 dB/Div1 REF VALUE: 0.0 dB REFERENCE LINE: TOP
S-PARAMS	S11



Test Procedure

Perform the test procedure as described below.

Step 1. Set up the network analyzer as shown in the table at top left.

Step 2. Attach a second high-precision waveguide section to the module on PORT 1.

Step 3. Attach a flush short to the PORT 1 module waveguide output.

Step 4. While observing sweep indicator (middle left), allow at least one complete sweep to occur.

Step 5. Press MARKER MENU key (left), and select **MARKER 1, MARKER 2, and MARKER 3,** to be **ON.**

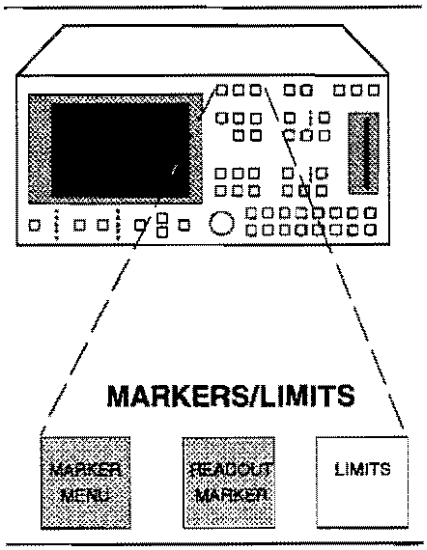
Step 6. Using rotary knob, position markers 1 and 2 to adjacent peaks of the ripple with the greatest negative trough; position marker 3 to the bottom of the trough (Figure 3-15, page 3-67.

Step 2. Using the menu prompts, perform a 12 term or reflection only **SLIDING LOAD** calibration over the full system operating range. (If necessary, refer to the 360B OM, Chapter 8, for detailed procedures.)

Step 3. Before pressing the ENTER key at the **BROADBAND LOAD** menu prompt, press the AVG/SMOOTH MENU key and change averaging to **1024 MEAS. PER POINT;** then press ENTER key to resume calibration.

Step 4. When the broadband measurement is complete, press the AVG/SMOOTH MENU key and change averaging to **32 MEAS. PER POINT;** continue the calibration.

Step 5. Ensure that the APPLY CAL key indicator is on.



Step 7. Using the MARKER MENU and READOUT MARKER key (left) menus, record the absolute value of markers 1 and 2; subtract one from the other, halve the difference and add it to the value of the marker at the lowest peak. This is the average value of the two peaks.

Step 8. Record the marker 3 value.

Step 9. Substract the value recorded in step 7 from that recorded in step 8. This is the Peak to Peak Ripple value that you will use next in Table 3-13, below.

Table 3-13. *Source Match / Directivity Peak-to-Peak Ripple*

Band	Peak-to-Peak Ripple
Q	0.1548 dB
U	0.2187 dB
V	0.2753 dB
W	0.3467 dB

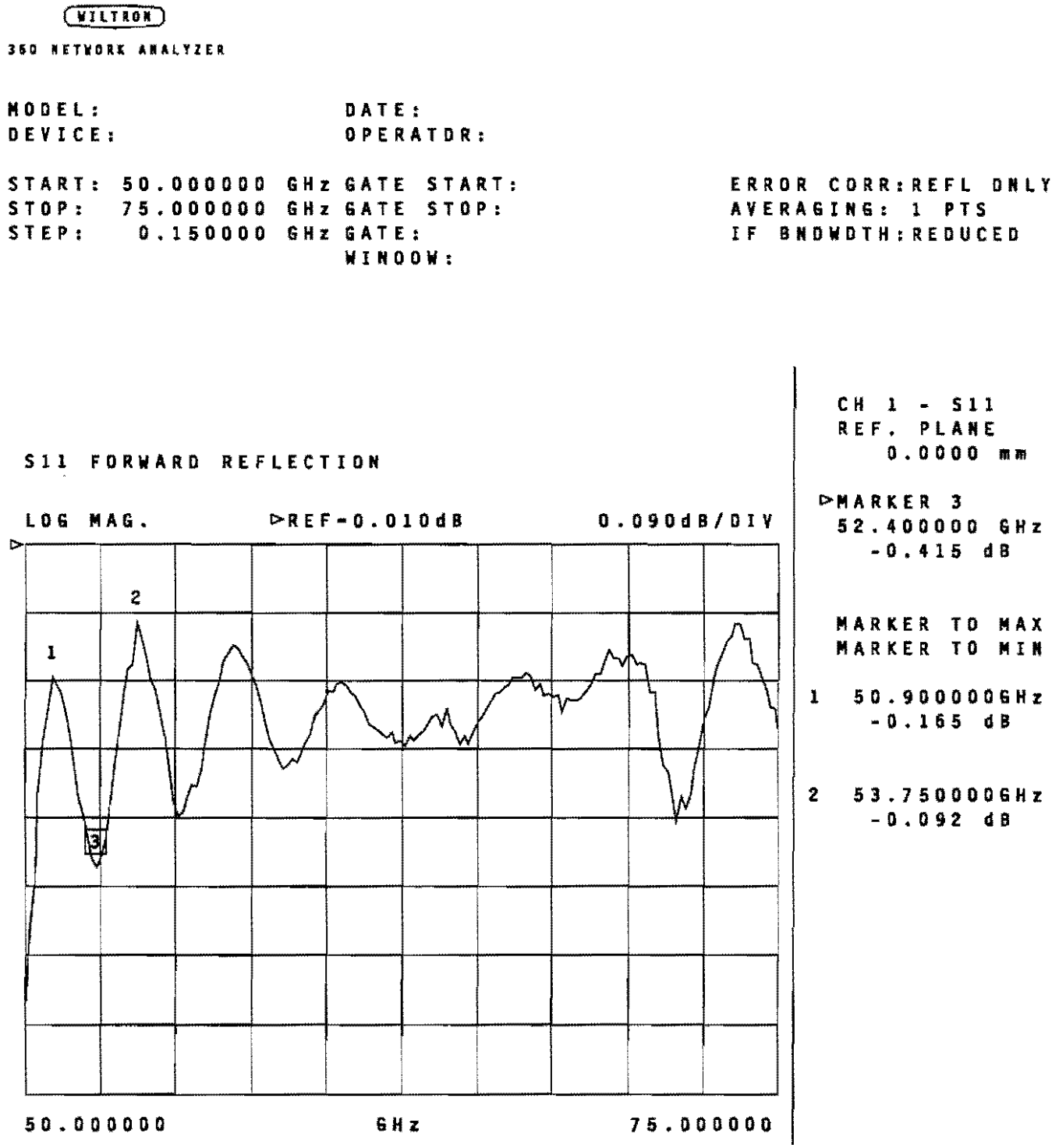


Figure 3-15. Source Match / Directivity Test Waveform

Chapter 4
360B VNA System Troubleshooting

Table of Contents

Chapter 4
360B VNA System Troubleshooting

4-1 INTRODUCTION

This chapter provides information and procedures for troubleshooting the 360B analyzer unit and test sets. Troubleshooting information and procedures for the 360SSXX Signal Source are provided in Chapter 10.

4-2 TEST EQUIPMENT

Recommended test equipment for troubleshooting is listed in Chapter 1, Table 1-3.

4-3 ERROR MESSAGES

The 360B VNA System uses messages to flag malfunctions and isolate them to one or more modules. These messages consist of those that identify malfunctions isolated to the 360B VNA unit and those related to other units within the system. Refer to Tables 4-1 and 4-2 for listings.

4-4 MALFUNCTIONS NOT DISPLAYING ERROR MESSAGES

System malfunctions or abnormalities that do not display an error message include problems with the monitor, bias tee, and step attenuator. Trobleshooting procedures for these problems are provided in Tables 4-27 thru 4-29.

4-5 TROUBLESHOOTING TABLES

The troubleshooting tables that begin on page 4-9 provide help in isolating malfunctions to a replaceable subassembly. In cases where any of several subassemblies could be causing the problem, troubleshooting is by way of subassembly replacement. The list of replacement items is by order of most-likely to least-likely suspect.

Table 4-1. *Error Codes Isolated to the 360B VNA Unit (1 of 3)*

Code	Message Text	Action
000	FIFO RESET FAILURE	Replace A12 PCB
002	PROM CHECKSUM FAILURE #2	Replace A12 PCB
003	BATTERY BACKED RAM FAILURE	Replace A12 PCB
004	EXTENDED MEMORY FAILURE	Replace A12 PCB
005	DYNAMIC RAM FAILURE #2	Replace A12 PCB
006	TIMER FAILURE #2	Replace A12 PCB
007	INTERRUPT CONTROLLER FAILURE #2	Replace A12 PCB
008	NUMERIC PROCESSOR FAILURE #2	Replace A12 PCB
009	FRONT PANEL INTERFACE FAILURE	See Table 4-3
010	PRINTER INTERFACE FAILURE	See Table 4-4
011	GRAPHICS DISPLAY INTERFACE FAILURE	See Table 4-5
012	GPIB INTERFACE FAILURE	Replace A12 PCB
013	RESPONSE TIMEOUT #1	See Table 4-6
014	INTER-PROCESSOR COMMUNICATIONS FAILURE #1	See Table 4-6
015	RESPONSE TIMEOUT I/O PROCESSOR	See Table 4-7
016	INTER-PROCESSOR COMMUNICATIONS FAILURE I/O	See Table 4-7
020	FIFO TO #2 FAILED RESET	See Table 4-6
022	FIFO TO I/O FAILED RESET	See Table 4-8
023	PROM CHECKSUM FAILURE #1	Replace A13 PCB
024	DYNAMIC RAM FAILURE #1	Replace A13 PCB
025	TIMER FAILURE #1	Replace A13 PCB
026	INTERRUPT CONTROLLER FAILURE #1	Replace A13 PCB
027	DISK DRIVE CONTROLLER FAILURE	Replace A13 PCB

Table 4-1. *Error Codes Isolated to the 360B VNA Unit (2 of 3)*

Code	Message Text	Action
028	DISK DRIVE FAILURE	See Table 4-9
029	NUMERIC PROCESSOR FAILURE #1	Replace A13 PCB
031	DISK DRIVE NOT READY FOR TEST	See Table 4-10
040	PROM CHECKSUM FAILURE I/O	Replace A11 PCB
041	RAM FAILURE I/O	Replace A11 PCB
042	TIMER\INTERRUPT LOOPBACK FAILURE	Replace A11 PCB
043	GPIB INTERFACE FAILURE I/O	Replace A11 PCB
044	FIFO FAILURE I/O	See Table 4-7
050	A1 COMMUNICATIONS FAILURE	Replace A1 PCB
051	A2 COMMUNICATIONS FAILURE	Replace A2 PCB
052	A3 COMMUNICATIONS FAILURE	Replace A3 PCB
053	A4 COMMUNICATIONS FAILURE	Replace A4 PCB
054	A5 COMMUNICATIONS FAILURE	Replace A5 PCB
055	A6 COMMUNICATIONS FAILURE	Replace A6 PCB
056	A10 COMMUNICATIONS FAILURE	Replace A1O PCB
057	8 BIT A/D CONVERTER FAILURE	Replace A4 PCB
058	STEERING DAC FAILURE	Replace A4 PCB
059	12 BIT A/D OR STEERING DAC FAILURE	Replace A4 PCB
100	DISK DRIVE NOT READY	See Table 4-10
101	PROGRAM DATA ERROR	See Table 4-15
102	PROGRAM FILE MISSING	See Table 4-15
103	DISK ERROR	See Table 4-10
104	UNKNOWN DISK ERROR	Replace disk drive

Table 4-1. *Error Codes Isolated to the 360B VNA Unit (3 of 3)*

Code	Message Text	Action
105	PROGRAM DATA ERROR ON #2	See Table 4-16
114	PROGRAM ERROR	See Table 4-10
115	PROCESSOR COM ERROR	See Table 4-10
131	DISK READ ERROR	See Table 4-10
132	DISK WRITE ERROR	See Table 4-10
134	DISK NOT READY	See Table 4-10
170	PRINTER NOT READY	See Table 4-4
171	PLOTTER NOT READY	See Table 4-19
301	LOCK FAILURE ABCDE	See Table 4-20
302	A/D FAILURE	Replace A4 PCB

Table 4-2. Error Codes Relating to System Units Other Than 360B VNA (1 of 2)

Code	Message Text	Action
	Error Codes Related to the 360B VNA or Test Set	
060	TEST SET NOT CONNECTED OR NOT WORKING	See Table 4-11
061	TEST SET CHAN A CAL PHASING FAILURE	See Table 4-12
062	TEST SET CHAN A CAL LEVEL FAILURE	See Table 4-12
063	TEST SET CHAN A GAIN FAILURE	See Table 4-12
064	TEST SET CHAN A PHASE RANGING FAILURE	See Table 4-12
065	TEST SET CHAN B CAL LEVEL FAILURE	See Table 4-13
066	TEST SET CHAN B CAL PHASING FAILURE	See Table 4-13
067	TEST SET CHAN B GAIN FAILURE	See Table 4-13
068	TEST SET CHAN B PHASE RANGING FAILURE	See Table 4-13
069	TEST SET REF CHAN CAL PHASING FAILURE	See Table 4-14
070	TEST SET REF CHAN CAL LEVEL FAILURE	See Table 4-14
071	TEST SET REF CHAN GAIN FAILURE	See Table 4-14
072	TEST SET REF CHAN PHASE RANGING FAILURE	See Table 4-14
112	NO TEST SET	See Table 4-18
301	LOCK FAILURE -BCDE	See Table 4-21
301	LOCK FAILURE -B-DE	See Table 4-22
301	LOCK FAILURE --CDE	See Table 4-23

Table 4-3. *Error Codes Relating to System Units Other Than 360B VNA (2 of 2)*

Code	Message Text	Action
	Error Codes Related to the 360B VNA or Source	
110	SRC ID FAILURE	See Table 4-17
301	LOCK FAILURE —DEF	See Table 4-24
400	GPIB ERROR	See Table 4-26
	Error Codes Related to the Test Set or Source	
303	RF OVERLOAD	See Table 4-25
	Error Codes Related to the 360B VNA System	
301	LOCK FAILURE —DE	See Table 4-24
	Error Codes Related to the 360B VNA System With 3635A Test Set	
301	LOCK FAILURE —DE	See Tables 4-30 and 4-31

Table 4-3. Troubleshoot Error Message 009 (1 of 1)

ERROR MESSAGE 009

Step 1. Turn the VNA off, then on again. Do not touch any controls or keys during the self test.

QUESTION: *Is error message gone?*

YES: Problem is cleared.

NO: Go to next step.

Step 2. Replace the A12 PCB in the VNA, and ask next question.

QUESTION: *Is error message gone?*

YES: Problem is cleared.

NO: Go to next step.

Step 3. Replace the front-panel-to-motherboard cable.

QUESTION: *Is error message gone?*

YES: Problem is cleared.

NO: Call customer service.

Table 4-4. *Troubleshoot Error Message 010 or 170 (1 of 1)*

ERROR MESSAGE 010 or 170

Step 1. Try a different printer.

QUESTION: *Is error message gone?*

YES: Problem is cleared.

NO: Go to next step.

Step 2. Try a different printer cable.

QUESTION: *Is error message gone?*

YES: Problem is cleared.

NO: Go to next step.

Step 3. Replace the A12 PCB in the VNA (paragraph 5-25).

QUESTION: *Error message gone?*

YES: Problem is cleared.

NO: Call Customer Service.

Table 4-5. *Troubleshoot Error Message 011 (1 of 1)*

ERROR MESSAGE 011

Step 1. Replace the A12 PCB in the VNA (paragraph 5-25).

QUESTION: *Is error message gone?*

YES: Problem is cleared.

NO: Go to next step.

Step 2. Replace the A13 PCB in the VNA (paragraph 5-25).

QUESTION: *Is error message gone?*

YES: Problem is cleared.

NO: Call Customer Service.

Table 4-6. *Troubleshoot Error Message 013, 014 or 020 (1 of 1)*

ERROR MESSAGE 013, 014, OR 020

Step 1. Replace the A13 PCB in the VNA (paragraph 5-25).

QUESTION: *Is error message gone?*

YES: Problem is cleared.

NO: Go to next step.

Step 2. Replace the A12 PCB in the VNA (paragraph 5-25).

QUESTION: *Is error message gone?*

YES: Problem is cleared.

NO: Call Customer Service.

Table 4-7. Troubleshoot Error Message 015, 016, or 044 (1 of 1)

ERROR MESSAGE 015, 016, OR 044

Step 1. Replace the A11 PCB in the VNA (paragraph 5-25).

QUESTION: *Is error message gone?*

YES: Problem is cleared.

NO: Go to next step.

Step 2. Replace the A12 PCB in the VNA (paragraph 5-25).

QUESTION: *Is error message gone?*

YES: Problem is cleared.

NO: Go to next step.

Step 3. Replace the A13 PCB in the VNA (paragraph 5-25).

QUESTION: *Is error message gone?*

YES: Problem is cleared.

NO: Call Customer Service.

Table 4-8. Troubleshoot Error Message 022 (1 of 1)

ERROR MESSAGE 022

Step 1. Replace the A13 PCB in the VNA (paragraph 5-25).

QUESTION: *Is error message gone?*

YES: Problem is cleared.

NO: Go to next step.

Step 2. Replace the A11 PCB in the VNA (paragraph 5-25).

QUESTION: *Is error message gone?*

YES: Problem is cleared.

NO: Call Customer Service.

Table 4-9. Troubleshoot Error Message 028 (1 of 1)

ERROR MESSAGE 028

Step 1. Turn the VNA off. Remove and reinstall the diskette, then turn the power back on.

QUESTION: *Is error message gone?*

YES: Problem is cleared.

NO: Go to next step.

Step 2. Replace disk drive assembly (paragraph 5-26).

QUESTION: *Is error message gone?*

YES: Problem is cleared.

NO: Call Customer Service.

Table 4-10. Troubleshoot Error Message 031, 100, 103, 114, 115, 131, 132, or 134 (1 of 2)

ERROR MESSAGE 031, 100, 103, 114, 115, 131, 132, OR 134

Step 1. Check that diskette is installed in drive.

QUESTION: *Is diskette installed?.*

YES: Go to step 2.

NO: Go to step 6.

Step 2. Try another diskette.

QUESTION: *Is error message gone?*

YES: Problem is cleared.

NO: Go to next step.

Step 3. Try replacing motherboard-to-drive cables P1 and P3.

QUESTION: *Is error message gone?*

YES: Problem is cleared.

NO: Go to next step.

Step 4. Check whether +12V and +5V is present on motherboard connector P4, pins 1 and 4 (below).

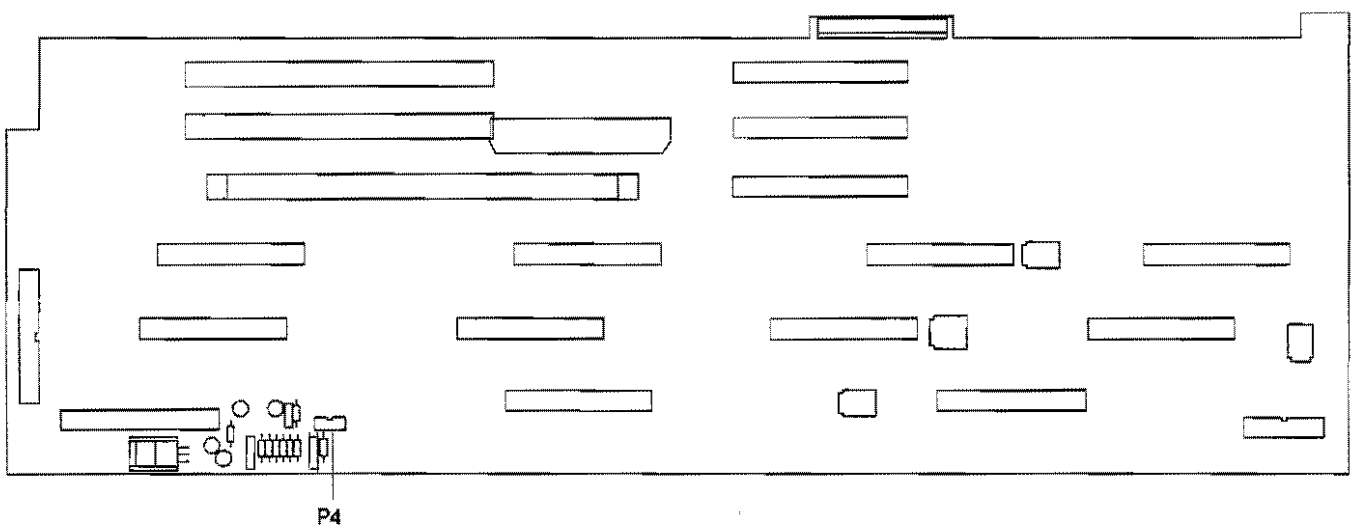


Table 4-10. Troubleshoot Error Message 031, 100, 103, 114, 115, 131, 132, or 134 (2 of 2)

QUESTION: *Are voltages incorrect?*

YES: Troubleshoot +12V Regulator and +5V line on motherboard, and ask next question.

NO: Go to next step.

Step 5. Replace disk drive assembly.

QUESTION: *Is error message gone?*

YES: Problem is cleared.

NO: Replace A17 PCB in VNA (paragraph 5-25), and ask next question.

QUESTION: *Is error message gone?*

YES: Problem is cleared.

NO: Call Customer Service.

Step 6. Turn the VNA off. Remove and reinstall the diskette, then turn the power back on.

QUESTION: *Does the message on the monitor read "LOADING PROGRAM FROM DISK"?*

YES: Problem is cleared.

NO: Call Customer Service.

Table 4-11. *Troubleshoot Error Message 060 (1 of 1)*

ERROR MESSAGE 060

Step 1. Check that cable between CONTROL connector on Test Set and VNA is properly connected.

QUESTION: *Is control cable connected correctly?*

YES: Try a different cable, and ask next question.

QUESTION: *Is error message gone?*

YES: Problem is cleared.

NO: Go to next step.

NO: Connect cable, and ask next question.

QUESTION: *Is error message gone?*

YES: Problem is cleared.

NO: Go to next step.

Step 2. Replace the following items in the order shown. After each replacement, ask next question.

- A6T PCB in Test Set (paragraph 6-12)
- A16 PCB in VNA (paragraph 5-25)
- Control cable assembly in Test Set
- Control cable assembly in VNA

QUESTION: *Is error message gone?*

YES: Problem is cleared.

NO: Replace next item, or call customer service after last item.

Table 4-12. *Troubleshoot Error Message 061, 062, 063, or 064 (1 of 1)*

ERROR MESSAGE 061, 062, 063, OR 064

Step 1. Check that cable between SIGNAL connector on Test Set and VNA is properly connected.

QUESTION: *Is signal cable correctly connected?*

YES: Go to next step.

NO: Connect cable, and ask next question.

QUESTION: *Is error message gone?*

YES: Problem is cleared.

NO: Go to next step.

Step 2. Replace the following items in the order shown. After each replacement, ask next question.

- SIGNAL cable between Test Set and VNA
- A7 PCB in VNA (paragraph 5-25)
- A3T PCB in Test Set (paragraph 6-7)
- A10 PCB in VNA (paragraph 5-25)
- A6T PCB in Test Set (paragraph 6-9)
- A16 PCB in VNA (paragraph 5-25)
- A5 PCB in VNA (paragraph 5-25)
- A16T Power Divider Assembly in Test Set (paragraph 6-19)

QUESTION: *Error message gone?*

YES: Problem is cleared.

NO: Replace next item, or call customer service after last item.

Table 4-13. Troubleshoot Error Message 065, 066, 067, or 068 (1 of 1)

ERROR MESSAGE 065, 066, 067, OR 068

Step 1. Check that cable between SIGNAL connector on Test Set and VNA is properly connected.

QUESTION: *Is signal cable correctly connected?*

YES: Go to next step.

NO: Connect cable, and ask next question.

QUESTION: *Is error message gone?*

YES: Problem is cleared.

NO: Go to next step.

Step 2. Replace the following items in the order shown. After each replacement, ask next question.

- SIGNAL cable between Test Set and VNA
- A8 PCB in VNA (paragraph 5-25)
- A1T PCB in Test Set (paragraph 6-7)
- A10 PCB in VNA (paragraph 5-25)
- A6T PCB in Test Set (paragraph 6-9)
- A16 PCB in VNA (paragraph 5-25)
- A4 PCB in VNA (paragraph 5-25)
- A5 PCB in VNA (paragraph 5-25)
- A16T Power Divider Assembly in Test Set (paragraph 6-19)

QUESTION: *Error message gone?*

YES: Problem is cleared.

NO: Replace next item, or call customer service after last item.

Table 4-14. Troubleshoot Error Message 069, 070, 071, or 072 (1 of 1)

ERROR MESSAGE 069, 070, 071, OR 072

Step 1. Check that cable between SIGNAL connector on Test Set and VNA is properly connected.

QUESTION: *Is signal cable correctly connected?*

YES: Go to next step.

NO: Connect cable, and ask next question.

QUESTION: *Is error message gone?*

YES: Problem is cleared.

NO: Go to next step.

Step 2. Replace the following items in the order shown. After each replacement, ask next question.

- SIGNAL cable between Test Set and VNA
- A9 PCB in VNA (paragraph 5-25)
- A2T PCB in Test Set (paragraph 6-7)
- A10 PCB in VNA (paragraph 5-25)
- A6T PCB in Test Set (paragraph 6-9)
- A16 PCB in VNA (paragraph 5-25)
- A4 PCB in VNA (paragraph 5-25)
- A5 PCB in VNA (paragraph 5-25)
- A16T Power Divider Assembly in Test Set (paragraph 6-19)

QUESTION: *Error message gone?*

YES: Problem is cleared.

NO: Replace next item, or call customer service after last item.

Table 4-15. Troubleshoot Error Message 101 or 102 (1 of 1)

ERROR MESSAGE 101 OR 102

Step 1. Check that diskette is installed in drive.

QUESTION: *Is diskette installed?*

YES: Go to next step.

NO: Install diskette.

Step 2. Try another diskette.

QUESTION: *Is error message gone?*

YES: Problem is cleared.

NO: Replace disk drive assembly, and ask next question.

QUESTION: *Is error message gone?*

YES: Problem is cleared.

NO: Call Customer Service.

Table 4-16. *Troubleshoot Error Message 105 (1 of 2)*

ERROR MESSAGE 105

Step 1. Check that diskette is installed in drive.

QUESTION: *Is diskette installed?*

YES: Go to step 2.

NO: Go to step 6.

Step 2. Try another diskette.

QUESTION: *Is error message gone?*

YES: Problem is cleared.

NO: Go to next step.

Step 3. Try replacing motherboard-to-drive cables P1 and P3.

QUESTION: *Is error message gone?*

YES: Problem is cleared.

NO: Go to next step.

Step 4. Check whether +12V and +5V is present on motherboard connector P4, pins **1** and 4 (below).

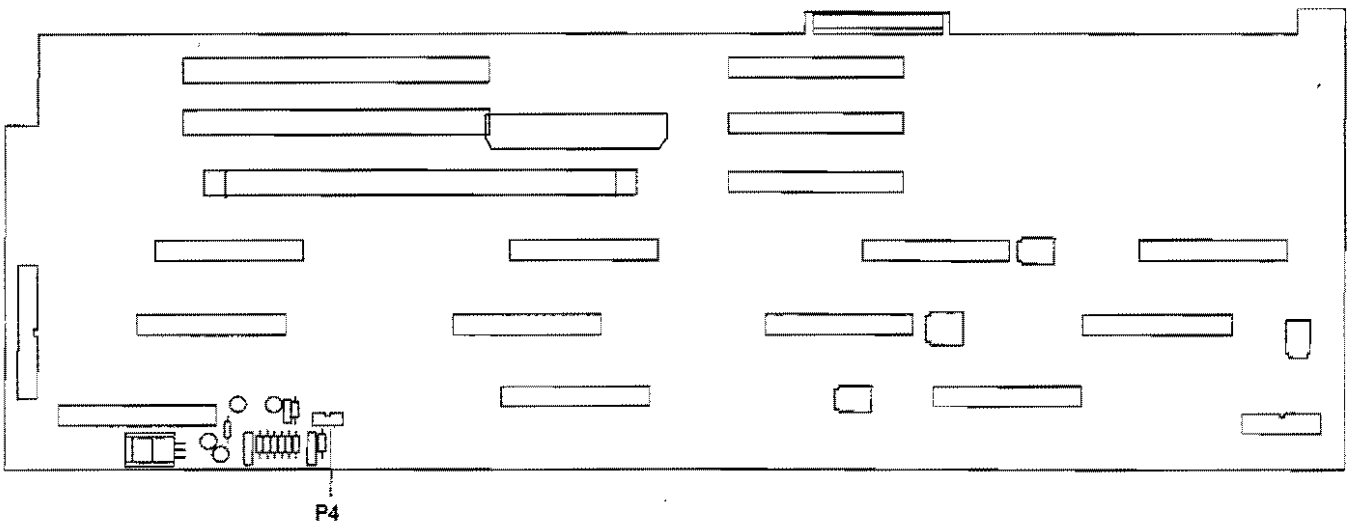


Table 4-16. *Troubleshoot Error Message 105 (2 of 2)*

Step 5. Replace disk drive assembly.

QUESTION: *Is error message gone?*

YES: Problem is cleared.

NO: Try replacing A17 PCB then A12 PCB in VNA (paragraph 5-25), and ask next question.

QUESTION: *Is error message gone?*

YES: Problem is cleared.

NO: Call Customer Service.

Step 6. Turn the VNA off. Remove and reinstall the diskette, then turn the power back on.

QUESTION: *Does the message on the monitor read "LOADING PROGRAM FROM DISK"?*

YES: Problem is cleared.

NO: Call Customer Service.

Table 4-17. Troubleshoot Error Message 110 (1 of 2)

ERROR MESSAGE 110

Step 1. Check that Signal Source is turned on.

QUESTION: *Is Signal Source On?*

YES: Go to next step.

NO: Turn on Signal Source.

Step 2. Check that GPIB cable is connected to 360 system bus.

QUESTION: *Is GPIB cable connected?*

YES: Go to next step.

NO: Connect cable.

Step 3. Try a different GPIB interconnect cable.

QUESTION: *Is error message gone?*

YES: Replace cable .

NO: Go to next step.

Step 4. Check that GPIB address within UTILITY MENU key menu matches address for Signal Source on rear panel.

QUESTION: *Do addresses match?*

YES: Replace GPIB cable.

NO: Reconfigure address, and ask next question.

QUESTION: *Is error message gone?*

YES: Problem is cleared.

NO: Go to next step.

Table 4-17. Troubleshoot Error Message 110 (2 of 2)

Step 5. Replace A1 PCB in Signal Source (paragraph 10-25).

QUESTION: *Is error message gone?*

YES: Problem is cleared.

NO: Go to next step.

Step 6. Replace GPIB cable assembly in Signal Source.

QUESTION: *Is error message gone?*

YES: Problem is cleared.

NO: Replace A11 PCB in VNA (paragraph 5-25), and ask next question.

QUESTION: *Is error message gone?*

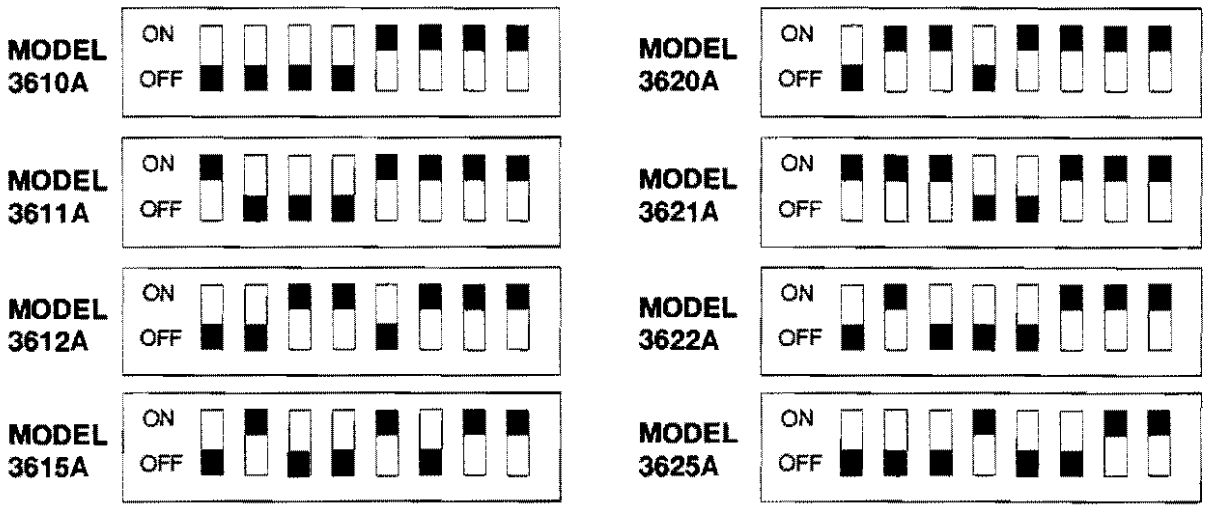
YES: Problem is cleared.

NO: Call Customer Service.

Table 4-18. Troubleshoot Error Message 112 (1 of 1)

ERROR MESSAGE 112

Step 1. For 361X and 362X Test Sets, check and reset as necessary the switch settings on the A6T PCB in the Test Set (below), and ask next question. For all other models, go to next step.



QUESTION: *Is error message gone?*

YES: Problem is cleared.

NO: Go to next step.

Step 2. Replace the following items in the order shown. After each replacement, ask next question.

- A6T PCB in Test Set (paragraph 6-9)
- A16 PCB in VNA (paragraph 5-25)
- A11 PCB in VNA (paragraph 5-25)
- Control cable between Test Set and VNA

QUESTION: *Is error message gone?*

YES: Problem is cleared.

NO: Call customer service.

Table 4-19. *Troubleshoot Error Message 171 (1 of 1)*

ERROR MESSAGE 171

Step 1. Check that GPIB cable is connected between the 360 SYSTEM BUS connector and the plotter.

QUESTION: *Is cable connected.*

YES: Go to next step.

NO: Connect cable.

Step 2. Check that plotter is on line; if not, turn it on.

QUESTION: *Is error message gone?*

YES: Problem is cleared.

NO: Go to next step.

Step 3. Check that GPIB address within UTILITY MENU key menu matches plotter address on rear panel.

QUESTION: *Do addresses match?*

YES: Replace A11 PCB in VNA (paragraph 5-25), and ask next question.

NO: Reconfigure address, and ask next question.

QUESTION: *Is error message gone?*

YES: Problem is cleared.

NO: Call Customer Service.

Table 4-20. Troubleshoot Error Message 301 ABCDE (1 of 1)

ERROR MESSAGE 301 ABCDE.

Step 1. Check VNA serial number on rear panel.

QUESTION: *Is serial number 703015 or below?*

YES: Go to next step.

NO: Replace 10 MHz oscillator assembly in VNA, and ask next question.

QUESTION: *Is error message gone?*

YES: Problem is cleared.

NO: Go to next step.

Step 2. Replace A5 PCB in VNA (paragraph 5-25).

QUESTION: *Is error message gone?*

YES: Problem is cleared.

NO: Call Customer Service.

Table 4-21. Troubleshoot Error Message 301 -BCDE (1 of 1)

ERROR MESSAGE 301 -BCDE

Step 1. Check that interconnect cables are seated and connectors have no damaged pin.

QUESTION: *Are cables OK?*

YES: Go to next step.

NO: Connect cables and/or repair bent pins.

Step 2. Replace the items below in the order listed, then ask next question.

- A6T PCB in Test Set (paragraph 6-9)
- A16 PCB in VNA (paragraph 5-25)
- A11 PCB in VNA (paragraph 5-25)

QUESTION: *Is error message gone?*

YES: Problem is cleared.

NO: Replace next item, or troubleshoot Error Message 301 —CDE (Table 4-23) after last replacement.

Table 4-22. Troubleshoot Error Message 301 -B-DE (1 of 1)

ERROR MESSAGE 301 -B-DE.

Step 1. Check that interconnect cables are seated and connectors have no damaged pins.

QUESTION: *Are cables OK?*

YES: Go to next step.

NO: Connect cables and/or repair bent pins.

Step 2. Adjust the A5T PCB in the Test Set (paragraph 3-11), then ask next question.

QUESTION: *Is error message gone?*

YES: Problem is cleared.

NO: Go to next step.

Step 3. Replace the items below in the order listed, then ask next question.

- A5T PCB in Test Set (paragraph 6-7)
- A1 PCB in VNA (paragraph 5-25)
- A16 PCB in VNA (paragraph 5-25)
- A6T PCB in Test Set (paragraph 6-9)

QUESTION: *Is error message gone?*

YES: Problem is cleared.

NO: Replace next item, or call customer service after last item.

Table 4-23. Troubleshoot Error Message 301 —CDE (1 of 1)

ERROR MESSAGE 301 —CDE.

Step 1. Check that interconnect cables are seated and connectors have no damaged pins.

QUESTION: *Are cables OK?*

YES: Go to next step.

NO: Connect cables and/or repair bent pins.

Step 2. Adjust the A4T PCB in the Test Set (paragraph 3-11), then ask next question.

QUESTION: *Is error message gone?*

YES: Problem is cleared.

NO: Go to next step.

Step 3. Replace the items below in the order listed, then ask next question.

- A4T PCB in Test Set (paragraph 6-7)
- A2 PCB in VNA (paragraph 5-25)
- A16 PCB in VNA (paragraph 5-25)
- A6T PCB in Test Set (paragraph 6-9)
- A11 PCB in VNA (paragraph 5-25)

QUESTION: *Is error message gone?*

YES: Problem is cleared.

NO: Replace next item, or call customer service after last item.

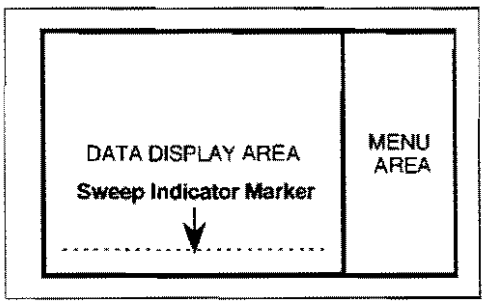
Table 4-24. Troubleshoot Error Message 301 —DE/DEF (1 of 6)

ERROR MESSAGE 301 —DE/DEF

Step 1. Check for presence of signal in both forward and reverse directions.

- If failure occurs in both directions, go to next step.
- If failure occurs only in forward direction, go to step 3.
- If failure occurs only in reverse direction, go to step 6.

Step 2. Determine the frequency band in which the failure occurs. Observe the sweeping indicator (below).



QUESTION: *Does system fail only between 40 and 270 MHz?*

NO: Go to next question.

YES: Perform a confidence test on the Signal Source (paragraph 10-13), then ask next question.

QUESTION: *Is the output power correct?*

NO: Troubleshoot the Signal Source (paragraph 10-3).

YES: Replace the items below in the order listed. Check whether error message goes away after each replacement. If it does, the problem is cleared. If it does not, call Customer Service.

- A4T PCB in Test Set (paragraph 6-7)
- A2 PCB in VNA (paragraph 5-25)

QUESTION *Does system fail between 40 and 270 MHz, 600 and 1000 MHz, 40 and 65 GHz,* and *in all four YIG bands?*

Table 4-24. Troubleshoot Error Message 301 —DE/DEF (2 of 6)

NO: Go to next question.

YES: Perform a confidence test on the Signal Source (paragraph 10-13), then ask next question.

QUESTION: *Is the output power correct?*

NO: Troubleshoot the Signal Source (paragraph 10-3).

YES: Replace the items below in the order listed. Check whether error message goes away after each replacement. If it does, the problem is cleared. If it does not, call Customer Service.

- A6 PCB in VNA (paragraph 5-25)
- A16 PCB in VNA (paragraph 5-25)
- A24T Source Lock/LRL module in Test Set (paragraph 6-20)
- A6T PCB in Test Set (paragraph 6-9)
- A13T Transfer Switch in Test Set (paragraph 6-14)
- A11 PCB in VNA (paragraph 5-25)

QUESTION *Does system fail between 40 and 270 MHz, 600 and 1000 MHz, 40 and 65 GHz, in only certain oscillator bands, and/or in all four YIG bands?*

NO: Go to next question.

YES: Perform a confidence test on the Signal Source (paragraph 10-13), then ask next question.

QUESTION: *Is the output power correct?*

NO: Troubleshoot the Signal Source (paragraph 10-3).

YES: Replace the items below in the order listed. Check whether error message goes away after each replacement. If it does, the problem is cleared. If it does not, call Customer Service.

- A5T PCB in Test Set (paragraph 6-7)
- A1 PCB in VNA (paragraph 5-25)
- A6T PCB in Test Set (paragraph 6-9)
- A11 PCB in VNA (paragraph 5-25)

Table 4-24. Troubleshoot Error Message 301 —DE / DEF (3 of 6)

- A16T Power Divider PCB in Test Set (paragraph 6-19)
- A6T PCB in Test Set

QUESTION *Does system only fail between 40 and 65 GHz?*

NO: Go to next question.

YES: Perform a confidence test on the Signal Source (paragraph 10-13), then ask next question.

QUESTION: *Is the output power correct?*

NO: Troubleshoot the Signal Source (paragraph 10-3).

YES: Replace the items below in the order listed. Check whether error message goes away after each replacement. If it does, the problem is cleared. If it does not, call Customer Service.

- A27T PCB in Test Set (paragraph 6-10)
- Ribbon cable from A27T PCB to motherboard in Test Set
- A6T PCB in Test Set (paragraph 6-9)

QUESTION *Does system only fail in certain oscillator bands?*

YES: Perform a confidence test on the Signal Source (paragraph 10-13), then ask next question.

NO: Call Customer Service.

Table 4-24. Troubleshoot Error Message 301 —DE/DEF (4 of 6)

Step 3. Determine frequency where failure occurs.

QUESTION: *Does failure only occur between 40 and 65 GHz?*

YES: Go to step 5.

NO: Go to next step.

Step 4. Replace the items below in the order listed. Ask next question after each replacement.

- Control cable between Test Set and VNA
- A6T PCB in Test Set (paragraph 6-9)
- A13T Transfer Switch in Test Set (paragraph 6-14)
- A4T PCB in Test Set (paragraph 6-7)
- A10T Channel A Buffer Amplifier in Test Set (paragraph 6-16)
- A2T PCB in Test Set (paragraph 6-7)
- A24T Source Lock/LRL module in Test Set (paragraph 6-20)
- A27T PCB in Test Set (paragraph 6-10)
- A28T Secondary Channel A A13T Transfer Switch in Test Set (paragraph 6-14)
- A30T Channel A Tripler Assembly in Test Set (paragraph 6-15)
- Ribbon Cable between A27T PCB and Motherboard in Test Set
- Motherboard in Test Set

QUESTION: *Is error message gone?*

YES: Problem is cleared.

NO: Replace next item, or call customer service after last item.

Step 5. Replace the items below in the order listed. Ask next question after each replacement.

- A6T PCB in Test Set (paragraph 6-9)
- A27T PCB in Test Set (paragraph 6-10)
- A29T Secondary Channel B in Test Set (paragraph 6-14)
- A31T Channel B Tripler in Test Set (paragraph 6-15)
- Ribbon Cable between A27T PCB and Motherboard in Test Set
- Motherboard in Test Set

Table 4-24. Troubleshoot Error Message 301 —DE/DEF (5 of 6)

QUESTION: *Is error message gone?*

YES: Problem is cleared.

NO: Replace next item, or call customer service after last item.

Step 6. Determine frequency where failure occurs.

QUESTION: *Does failure only occur between 40 and 65 GHz?*

YES: Go to step 8.

NO: Go to next step.

Step 7. Replace the items below in the order listed. Ask next question after each replacement.

- Control cable between Test Set and VNA
- A6T PCB in Test Set (paragraph 6-9)
- A13T Transfer Switch in Test Set (paragraph 6-14)
- A4T PCB in Test Set (paragraph 6-7)
- A8T Channel B Buffer Amplifier in Test Set (paragraph 6-16)
- A24T Source Lock/LRL module in Test Set (paragraph 6-20)
- A27T PCB in Test Set (paragraph 6-10)
- A29T Secondary Channel B Transfer Switch in Test Set (paragraph 6-14)
- A31T Channel B Tripler Assembly in Test Set (paragraph 6-15)
- Ribbon Cable between A27T PCB and Motherboard in Test Set
- Motherboard in Test Set

QUESTION: *Is error message gone?*

YES: Problem is cleared.

NO: Replace next item, or call customer service after last item.

Table 4-24. Troubleshoot Error Message 301 —DE/DEF (6 of 6)

Step 8. Replace the items below in the order listed. Ask next question after each replacement.

- A6T PCB in Test Set (paragraph 6-9)
- A27T PCB in Test Set (paragraph 6-10)
- A29T Secondary Channel B Transfer Switch in Test Set (paragraph 6-14)
- A31T Channel B Tripler Assembly in Test Set (paragraph 6-15)
- Ribbon Cable between A27T PCB and Motherboard in Test Set
- Motherboard in Test Set

QUESTION: *Is error message gone?*

YES: Problem is cleared.

NO: Replace next item, or call customer service after last item.

Table 4-25. Troubleshoot Error Message 303 (1 of 1)

ERROR MESSAGE 303

Step 1. Perform a confidence test on the Signal Source (paragraph 10-13), then ask next question.

QUESTION: *Is the output power correct?*

NO: Troubleshoot the Signal Source (paragraph 10-3).

YES: Go to next step.

Step 2. Determine which channel causes the error message to occur.

QUESTION: *Does error message occur in all channels?*

YES: Replace the A6T PCB in the Test Set (paragraph 6-9).

NO: Go to next question.

QUESTION: *Does error message only occur in Test B channel?*

YES: Replace the A1T PCB in the Test Set (paragraph 6-7).

NO: Go to next question.

QUESTION: *Does error message only occur in Reference channel?*

YES: Replace the A2T PCB in the Test Set (paragraph 6-7).

NO: Call Customer Service.

Table 4-26. Troubleshoot Error Message 400 (1 of 1)

ERROR MESSAGE 400

Step 1. Check that Signal Source is turned on.

QUESTION: *Is Signal Source On?*

YES: Go to next step.

NO: Turn On Signal Source.

Step 2. Check that GPIB address within UTILITY MENU key menu matches source address on rear panel.

QUESTION: *Do addresses match?*

YES: Replace GPIB cable.

NO: Reconfigure address, and ask next question.

QUESTION: *Is error message gone?*

YES: Problem is cleared.

NO: Go to next step.

Step 3. Check that plotter has paper loaded.

QUESTION: *Is paper loaded?*

YES: Go to next step.

NO: Install paper.

Step 4. Replace the following items in the order shown. After each replacement, ask next question.

- A1 PCB in Signal Source (paragraph 10-25)
- A16 PCB in VNA (paragraph 5-25)

QUESTION: *Is error message gone?*

YES: Problem is cleared.

NO: Replace next item, or call customer service after last item.

Table 4-27. Monitor Problems (1 of 1)

MONITOR PROBLEMS

Step 1. Replace the items below in the order listed. Ask next question after each replacement.

- A12 PCB in VNA (paragraph 5-25)
- A11 PCB in VNA (paragraph 5-25)
- A14 PCB in VNA (paragraph 5-25)

QUESTION: *Is error message gone?*

YES: Problem cleared.

NO: Replace next item, or replace monitor after last item.

Step 2. Replace the items below in the order listed. After each replacement, ask next question.

- A15 PCB in VNA (paragraph 5-25)
- A18 PCB in VNA (paragraph 5-25)

QUESTION: *Is error message gone?*

YES: Problem is cleared.

NO: Replace next item, or replace monitor after last item.

Table 4-28. Bias Tee Problems (1 of 1)

BIAS TEE PROBLEMS

Step 1. Check that the front panel fuses in the Test Set are not blown.

QUESTION: *Are fuses blown?*

YES: Replace fuses, and ask next question.

NO: Go to next step.

QUESTION: *Did fuses blow again?*

YES: Go to next step.

NO: Problem is cleared.

Step 2. Replace the A18T or A19T Bias Tee (paragraph 6-12).

QUESTION: *Is problem corrected?*

YES: Problem is cleared.

NO: Go to next step.

Step 3. Replace the items below in the order listed. After each replacement, ask next question.

- A7T PCB in Test Set (paragraph 6-10)
- A6T PCB in Test Set (paragraph 6-9)

QUESTION: *Is problem corrected?*

YES: Problem is cleared.

NO: Replace next item, or call customer service after last item.

Table 4-29. Step Attenuator Problems (1 of 1)

STEP ATTENUATOR PROBLEMS

Step 1. Replace the items below in the order listed. After each replacement, ask next question.

- A7T PCB in Test Set (paragraph 6-10)
- A20T, A21, or A22T (as applicable) Step Attenuator in Test Set (paragraph 6-12)

QUESTION: *Is problem corrected?*

YES: Problem is cleared.

NO: Replace next item, or call customer service after last item.

Table 4-30. Error Message 301 —DE for System With Model 3635B Test Set When Port 2 Module is a 3641 (1 of 1)

ERROR MESSAGE 301 —DE

Step 1. Replace the items below in the order listed. After each replacement, ask next question.

- A20T RF Input Amplifier in Test Set (paragraph 6-22)
- A9T Transfer Switch in Test Set (paragraph 6-14)
- A6T PCB in Test Set (paragraph 6-9)
- A5T PCB in Test Set (paragraph 6-8)
- A21T Port 1 L.O. Amplifier in Test Set (paragraph 6-24)
- A11T L.O. 1 Power Splitter in Test Set (paragraph 6-25)
- A24T Source Lock/LRL module in Test Set (paragraph 6-20)

QUESTION: *Is error message gone?*

YES: Problem is cleared.

NO: Replace next item, or call customer service after last item.

Table 4-31. Error Message 301 —DE for System With Model 3635B Test Set When Port 2 Module is a 3640 (1 of 2)

ERROR MESSAGE 301 —DE

Step 1. Check for presence of signal in both forward and reverse directions.

- If failure occurs in both directions, go to next step.
- If failure occurs in only one direction, go to step 3.

Step 2. Replace the items below in the order listed. After each replacement, ask next question.

- A20T RF Input Amplifier in Test Set (paragraph 6-22)
- A9T Transfer Switch in Test Set (paragraph 6-14)
- A6T PCB in Test Set (paragraph 6-9)
- A5T PCB in Test Set (paragraph 6-7)
- A11T L.O. 1 Power Splitter in Test Set (paragraph 6-24)
- A24T Source Lock/LRL module in Test Set (paragraph 6-20)

QUESTION: *Is error message gone?*

YES: Problem is cleared.

NO: Replace next item, or call customer service after last item.

Step 3. Swap Port 1 and Port 2 364XB Modules.

QUESTION: *Is error message gone?*

YES: Problem is cleared.

NO: Go to next question.

QUESTION: *Does failure occur in the opposite direction?*

YES: Replace defective module.

NO: Go to next step.

Table 4-31. Error Message 301 —DE for System With Model 3635B Test Set When Port 2 Module is a 3640 (2 of 2)

Step 4. Replace the items below in the order listed. After each replacement, ask next question.

- A9T Transfer Switch in Test Set (paragraph 6-14)
- A6T PCB in Test Set (paragraph 6-9)
- A5T PCB in Test Set (paragraph 6-7)
- A11T L.O. 1 Power Splitter in Test Set (paragraph 6-25)
- A24T Source Lock/LRL module in Test Set (paragraph 6-20)

QUESTION: *Is error message gone?*

YES: Problem is cleared.

NO: Replace next item, or call customer service after last item.

Chapter 5
360B VNA
Information

Table of Contents

Chapter 5
360B VNA Information

5-1 INTRODUCTION

This chapter describes the Model 360B Vector Network Analyzer (VNA). The information is organized as follows:

- *VNA Description.* Provides an overall description and a block diagram of the VNA.
- *Assembly Descriptions.* Provides descriptions and block diagrams for the VNA major printed circuit boards (PCBs).
- *Remove and Replace.* Provides removal and replacement procedures for the major assemblies.

5-2 REPLACEABLE SUBASSEMBLIES

WILTRON maintains a module exchange program for selected VNA modules. If a malfunction occurs in one of these modules, it can be exchanged. Upon request and typically within 24 hours, WILTRON or an Anritsu/Wiltron Service Center will ship an exchange module. The customer has 30 days in which to return the defective item. All exchange parts are warranted for 90 days from the date of shipment or for the balance of the original-part warranty—whichever is longer.

A listing of exchangeable subassemblies is provided in Chapter 1, Table 1-2.

5-3 VNA DESCRIPTION

The 360B VNA unit provides the control and display function for the system. Its front panel controls provide menu selections for test functions, test parameters, measurement enhancements, and frequencies. It sends frequency information to the signal source over a dedicated system (GPIB) bus. A large color screen displays test parameters, system status information, and measurement data. The VNA also supplies hard copy printouts to a printer or plotter. Figure 5-1, page 5-6, shows the assembly layout. Figure 5-2, page 5-7, is a block diagram of the VNA and test set.

As shown in Figure 5-2, the phase-locked output of the signal source feeds its RF energy to the A13T Transfer Switch in the test set. This switch, which is also a signal splitter, provides two functions. It ensures that the RF signal is applied to both the test and reference channels and it supplies RF out to the DUT for forward or reverse measurements.

In the forward direction the A13T Transfer Switch passes the RF signal to Port 1, via a directional coupler. This coupler is sensitive to the power that reflects into the port while it rejects the power that is transmitted from the port. This reflected signal (T_A) is measured and ratioed with the incident, or reference, signal (R_A) and establishes the ratio of T_A/R_A. This is the basic forward reflection S-parameter, S_{11}. The power that exits Port 1 passes through the DUT and into Port 2; there it is coupled into the Samplers as T_B. The signal-level relationship of T_B/R_A is the basic forward transmission S-parameter, S_{21}. Similarly, when A13T is in the reverse position, the microwave energy passes to Port 2 and sets up signal-level relationships that go on to define S_{12} (T_B/R_B) and S_{22} (T_A/R_B), which are the reverse reflection and transmission terms.

The signals R_A, R_B, T_A, and T_B are down converted by mixers in the sampler to 89 MHz and then by mixers in the buffer amplifiers to 2.25 MHz. Though changed to a lower frequency in this and succeeding frequency conversions, all magnitude and phase relationships of the input signals remain they were at the carrier frequency. The A24 Source Lock/LRL module multiplexes the Test A and Reference A/B signals to the channel amplifiers and source lock PCB in the VNA. The Test B signal goes directly to the A1T channel amplifier.

At the output of the three channel amplifiers, the signal is down converted a third time to 83-1/3 kHz and applied to the A7, A8, and A9 PCBs in the VNA. Here, in the A7 – A9 PCB "Sync Det," the 83-1/3 kHz signals are converted to dc real and imaginary components. The sample-and-hold and multiplexer circuits in the PCBs route these signals to the A/D converter for conversion to digital signals.

The magnitude vector coming from the detectors is represented by the vector sum of the real and imaginary components. The phase is represented by the arctangent of the imaginary divided by the real components. To reconstruct the S-parameter, the digital processing section computes the appropriate signal ratios.

The digital processing section consists of three 8088-based microprocessor systems:

- Human Interface/Display Processor (Main #2)
- Vector Processor (Main #1)
- I/O Processor

I/O Processor The I/O processor controls the signal source and plotter via a dedicated GPIB. It controls the test set via a dedicated digital bus. It also controls all analog circuits and processes and corrects the data from the A/D converter.

Vector Processor (Main #1) The vector processor processes data received from the I/O processor via FIFO (first-in, first-out) registers. This includes the ratioing of the transmission/reflection variables to calculate the S-parameters, along with the necessary error correction. Additionally, this processor provides accuracy enhancements and controls the operation of the 3.5-inch diskette drive.

Human Interface Processor (Main #2) The human interface processor controls the interaction with the front panel, the external GPIB, and the parallel printer. It gives command and pixel addressing to the graphics control processor to create the various display functions and menus. Additionally, it is responsible for controlling the calibration sequencing, data formatting, frequency selection coordinate conversion, and scaling.

Graphics Control Processor The graphics control processor receives commands and data from the human interface processor. It formats the data it receives. And it outputs the display information to the color monitor.

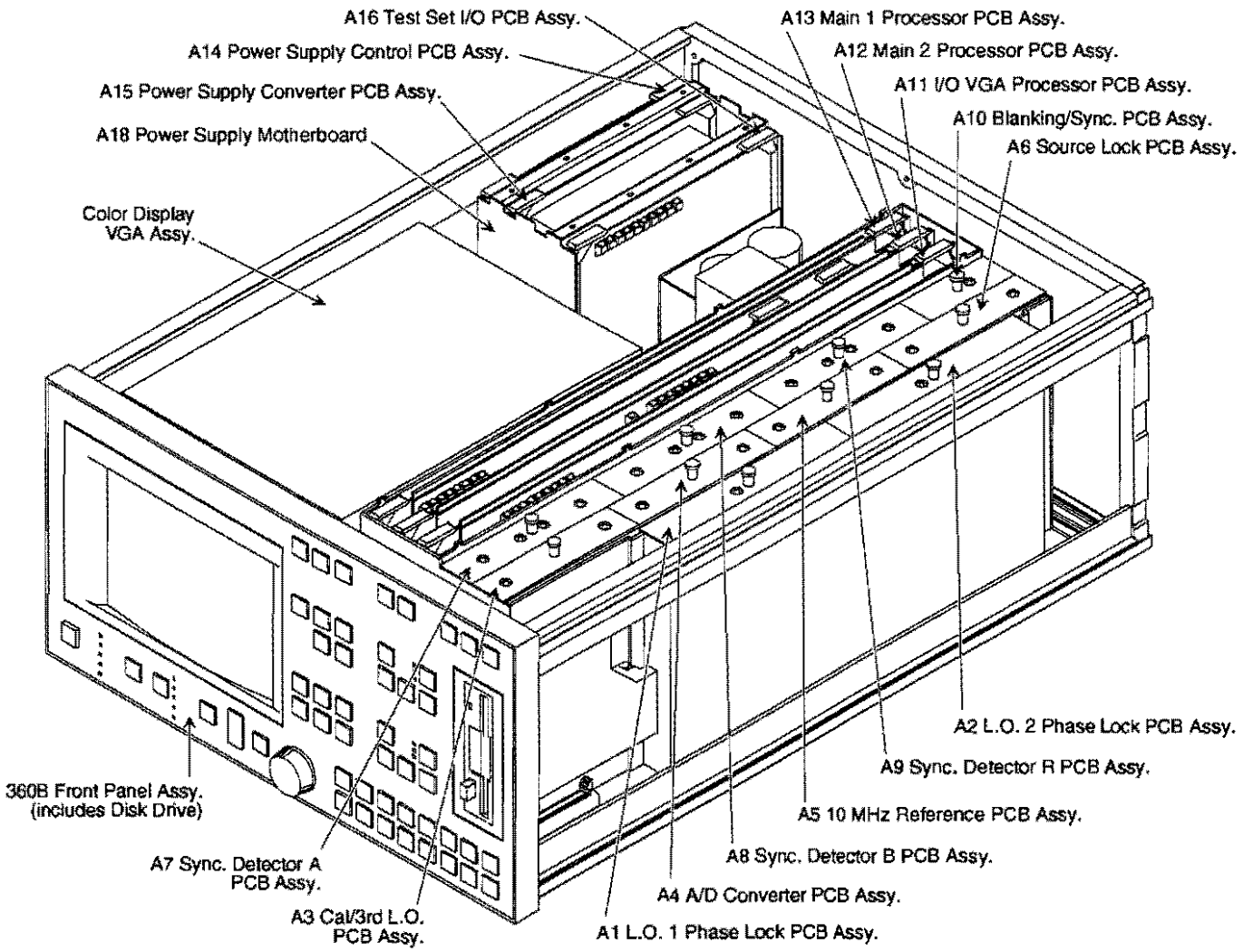
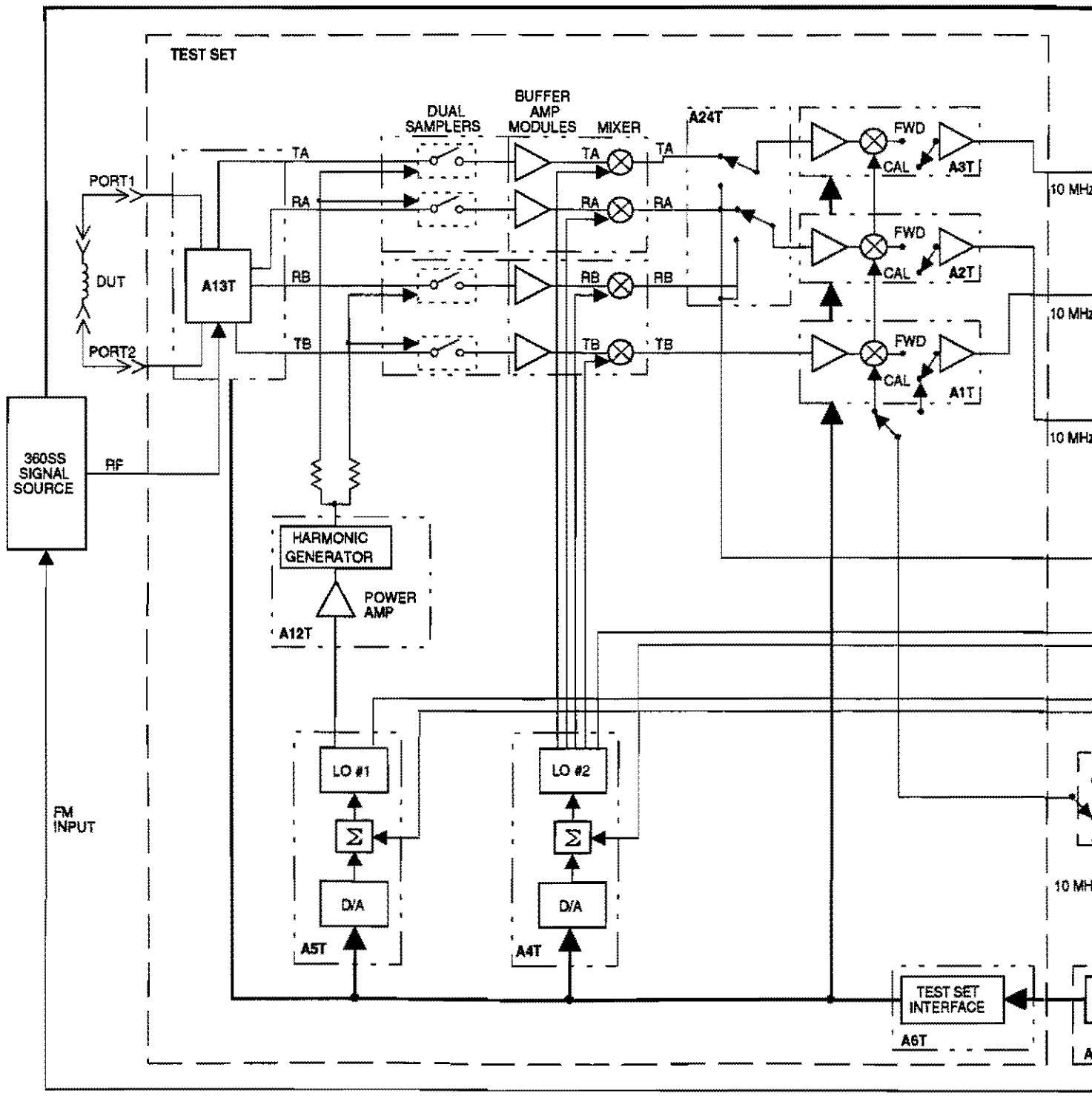


Figure 5-1 *360B VNA Assembly Locations*


TEST SET
DUAL SAMPLERS
BUFFER AMP MODULES
MIXER
A24T
FWD
CAL
A3T
A2T
A1T
10 MHz
PORT1
PORT2
DUT
A13T
TA
RA
RB
TB
360SS SIGNAL SOURCE
RF
HARMONIC GENERATOR
POWER AMP
A12T
LO #1
LO #2
Σ
D/A
A5T
A4T
FM INPUT
TEST SET INTERFACE
A6T

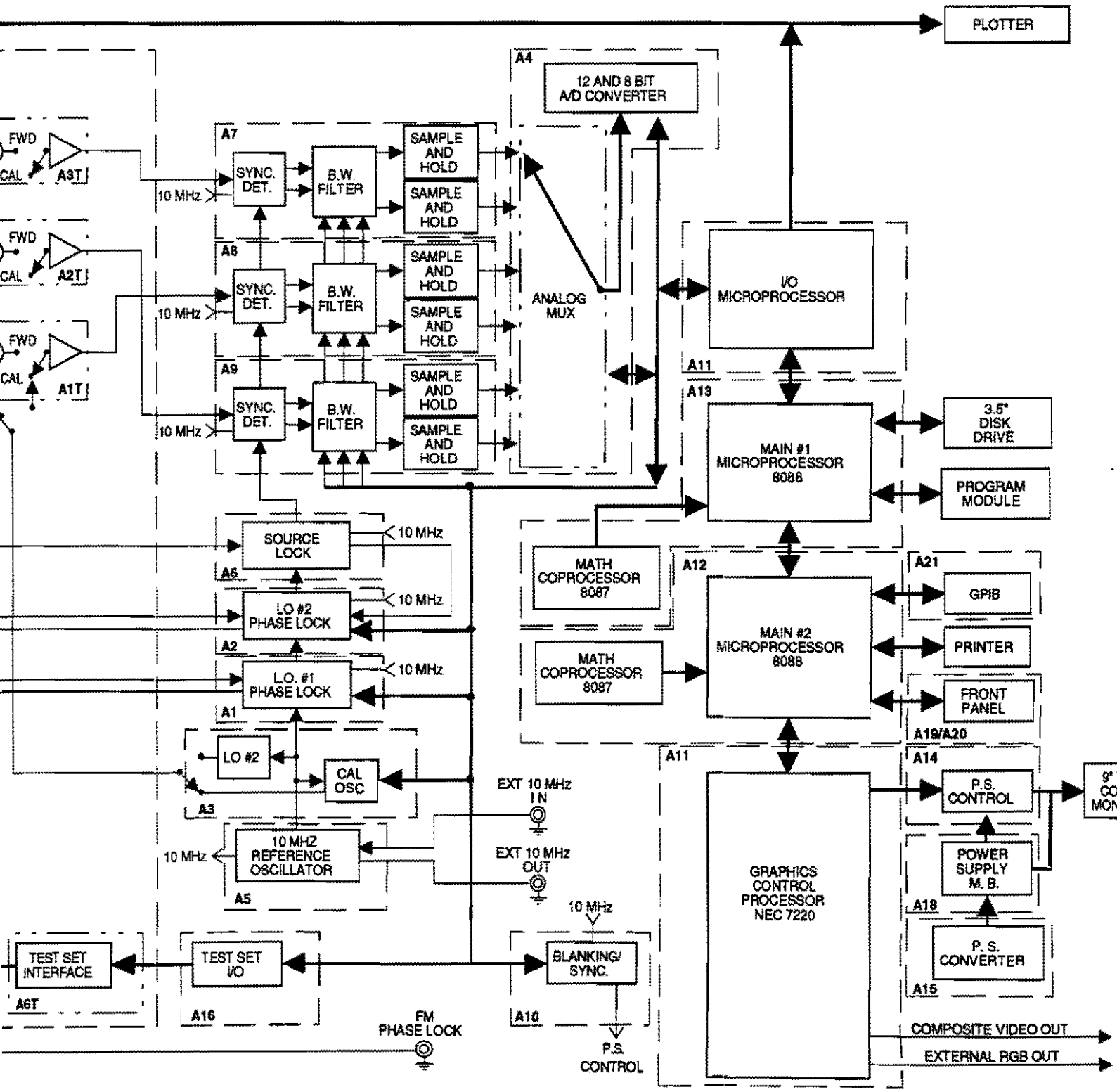


Figure 5-2. 360B VNA System Block Diagram

5-4 A1 LO 1 PHASE LOCK PCB CIRCUIT DESCRIPTION

The A1 Phase Lock PCB (Figure 5-3) is the phase-lock circuit for the first local oscillator (LO1), which is located on the A5T board in the test set.

The input signal from the LO1 board goes through a divide by M divider. M is a programmable value between 714.0 and 1073.9. The output of the divider then passes to a phase/frequency comparator (ϕ). The phase/frequency comparator compares this signal with a reference frequency of 500 kHz. A divide by 20 divider (÷20) divides a 10 MHz reference signal to derive the 500 kHz. A summing amplifier (Σ) sets the gain of the phase/frequency detector. The summing amplifier compares a dc reference voltage with the level of the Vϕ DET signal. The Vϕ DET level is proportional to the frequency of the LO1 signal.

A second output from the phase/frequency detector goes to a lock detector. The lock detector informs the I/O processor whether or not phase-lock has occurred.

If the frequency of LO1 is too low, a negative signal passes to the loop filter, this causes a corresponding positive output of the filter that signals the LO to increase the frequency.

If the frequency of the LO is too high, a positive signal passes to the loop filter, this causes a corresponding negative output of the filter that signals the LO to decrease the frequency.

The output of the loop filter has a 50 kHz notch filter to filter out the fractional N sidebands produced in the ÷M divider.

A Level Detector circuit determines if the input LO signal is of adequate amplitude. The level detector then provides a status bit to the I/O processor.

The LOCK and LEVEL signals drive the STATUS line. If either of these signals are low the status output is set low. The I/O processor monitors this line, if it senses a low signal, it displays a 301: LOCK FAILURE error message. It also sends a message to the Main 1 Processor and uses the most recent valid data.

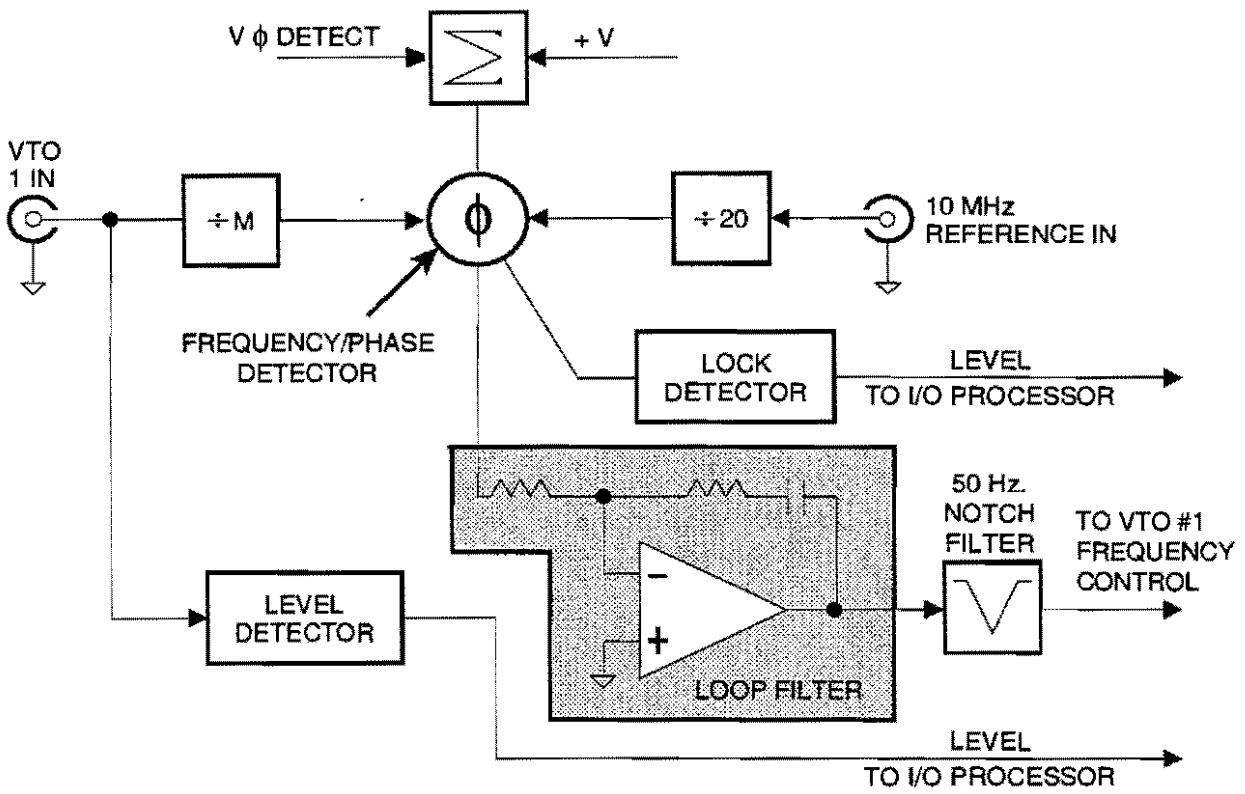


Figure 5-3. *A1 LO 1 Phase Lock PCB Block Diagram*

5-5 A2 LO 2 PHASE LOCK PCB CIRCUIT DESCRIPTION

The A1 PCB and the A2 PCB are operationally similar. The only functional difference is the ability to disable the phase lock circuit when using a synthesizer. When the 360 powers up, it checks to see if a synthesizer is installed. If so, the A2PCB phase lock is disabled. When the A2 PCB is disabled, the A6 Source Lock PCB phase-locks the synthesizer.

The A2 LO 2 Phase Lock PCB (Figure 5-4) is the phase lock circuit for the second local oscillator (LO2) located on the A4T PCB in the test set. This circuit phase locks the LO2 oscillator.

The input signal from the A4T PCB goes through a divide by K divider. K is programmable between 196.0 and 544.5. The output of the divider then passes to a phase/frequency comparator (ϕ). The phase/frequency comparator compares this signal with a reference frequency of 500 kHz. A divide by 20 divider ($\div 20$) divides a 10 MHz reference signal to derive the 500 kHz. A summing amplifier (Σ) sets the gain of the frequency/phase detector. The summing amplifier compares a dc reference voltage with the level of the Vϕ DET signal. The Vϕ DET is proportional to the frequency of the LO2 signal.

A second output from the phase/frequency detector goes to a lock detector. The lock detector informs the I/O processor whether or not phase-lock is established.

If the frequency of LO2 is too low, a negative signal passes to the loop filter, this causes a corresponding positive output of the filter that signals the LO to increase the frequency.

If the frequency of the LO is too high, a positive signal passes to the loop filter. This causes a corresponding negative output of the filter that signals the LO to decrease the frequency.

The output of the loop filter has a 50 kHz notch filter to filter out the fractional N sidebands produced in the $\div$K divider

A Level Detector circuit determines if the input LO signal is of adequate amplitude. The level detector then provides a status bit to the I/O processor indicating if the level is adequate or not.

The LOCK and LEVEL signals drive the STATUS line. If either of these signals are low the status output is set low. The I/O processor monitors this line, if it sense a low signal, it displays a 301:LOCK FAILURE on the CRT. It also sends a message to the Main 1 Processor and uses the most recent valid data.

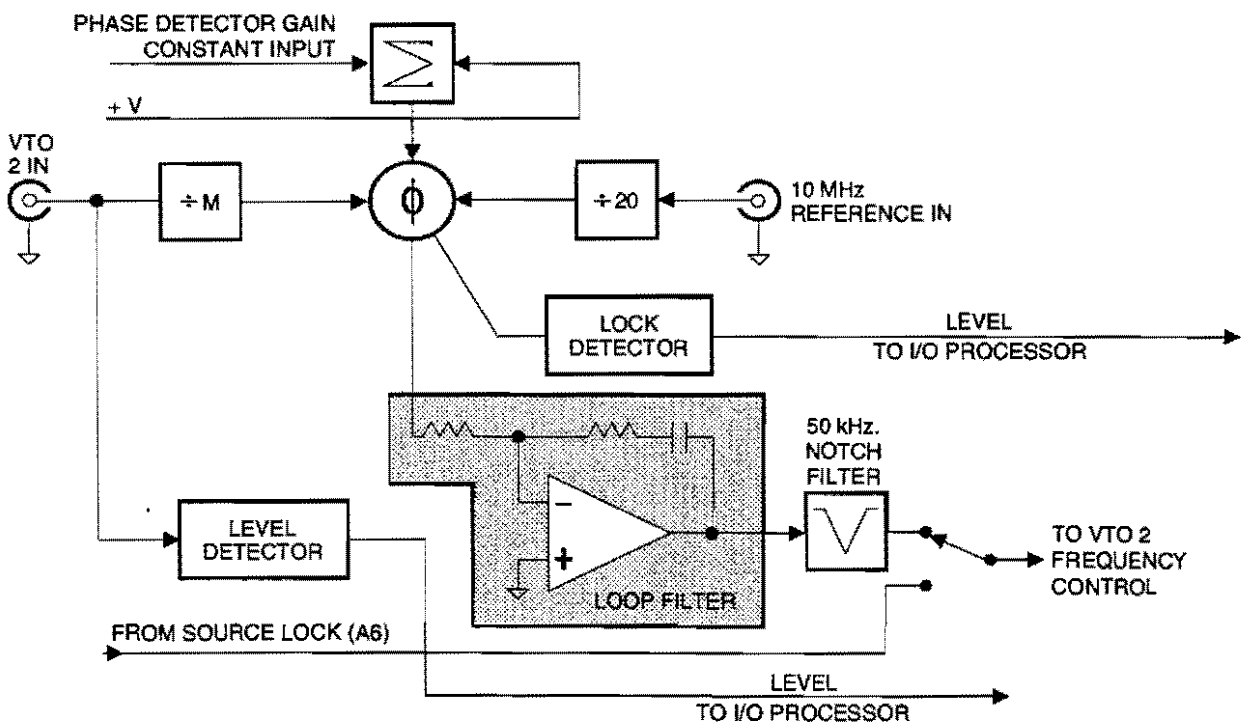


Figure 5-4. A2 LO 2 Phase Lock PCB Block Diagram

5-6 A3 CAL/3rd LO PCB CIRCUIT DESCRIPTION

The A3 CAL/3rd LO PCB (Figure 5-5) has two modes of operation. One is the CAL mode, the other is the LO3 mode.

LO3 Mode

In this mode the circuit is a phase-locked 2.333 MHz local oscillator. Two signals are input to the phase comparator (ϕ). One signal is taken from the 10 MHz reference signal. The reference signal is divided by the ÷15 circuit. The other signal is derived from the 9.33 MHz signal generated on the A3 PCB. This signal is divided by 14 (÷14) to derive a 666 kHz signal. The phase comparator performs two major functions:

- It supplies the error amplifier with a voltage proportional to the phase difference between the LO3 signal and the reference signal. The error amplifier then controls the input to the 9.33 MHz VCO to adjust to the proper phase.
- The phase detector provides the lock detector with a voltage level indicating whether or not the circuit is phase-locked. The lock detector then provides the appropriate level on the 2.333 MHz OK bit. This bit is then read by the I/O processor.

CAL Mode

In CAL mode the divide-by-120 divider (÷120) divides the 10 MHz reference signal. This produces an 83 1/3 kHz output. The I/O processor sends incremental data to the divide-by-120 divider. The output of this divider drives a sine look-up ROM. The output of this circuit is input to the 8-bit D/A converter. The output of the D/A converter is the approximation of an 83 1/3 kHz sinewave. The 100 kHz lowpass filter filters out the sidebands that the D/A converter generates. The 83 1/3 kHz sinusoidal signal is then applied to the IF amplifiers during CAL mode.

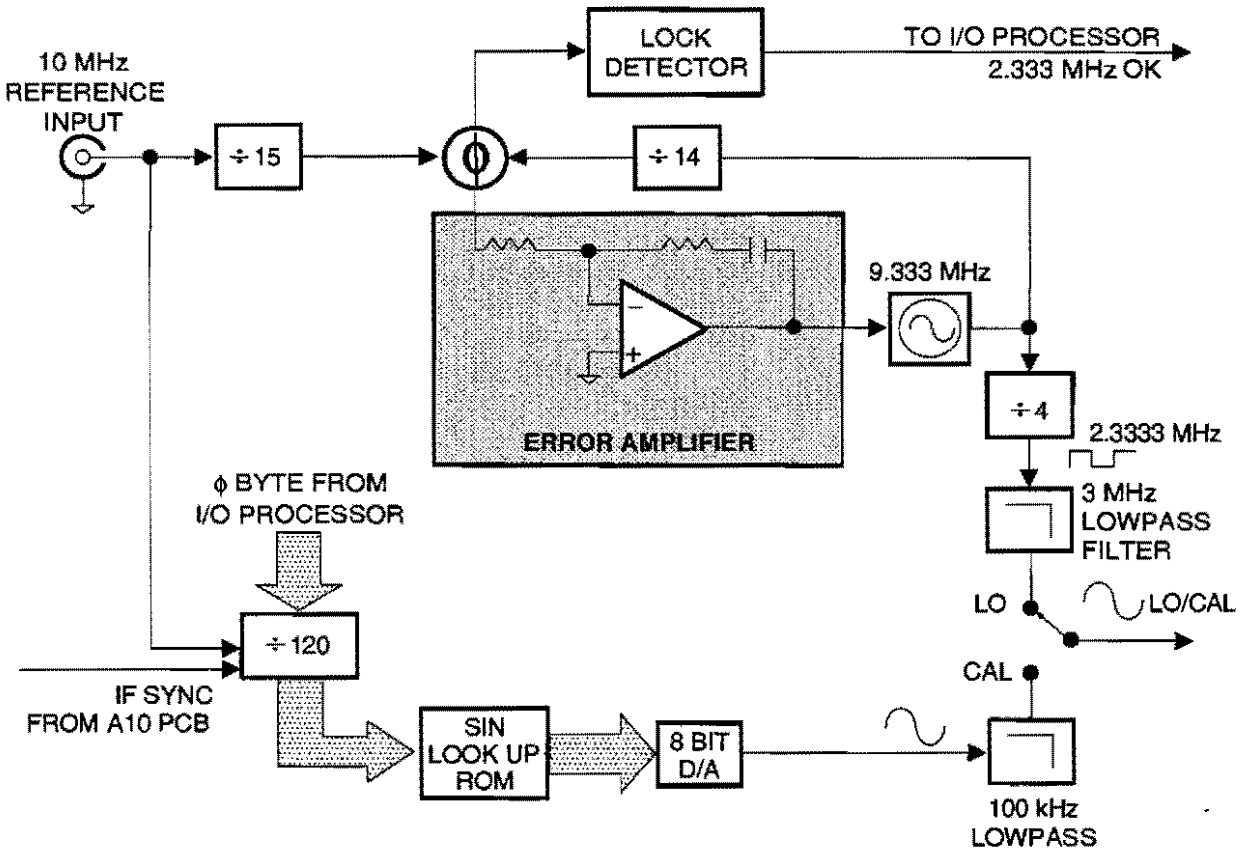


Figure 5-5. A3 CAL 3rd LO PCB Block Diagram

5-7 A4 A/D CONVERTER PCB CIRCUIT DESCRIPTION

The A4 A/D Converter PCB (Figure 5-6) has two modes of operation, calibration and normal. (A calibrate cycle is completed approximately every three minutes to guarantee absolute accuracy.) The A4 PCB performs a 19-bit analog to digital conversion. The input range of the overall circuit is –5V to +5V. The linearity of the circuit is better than 1 part in 2^{16}. The following paragraphs describe the circuit operation in normal and cal modes.

Normal Mode

Input signals are multiplexed into the A/D circuit by an analog multiplexer. Six of these signals are voltages corresponding to the real and imaginary components of the Test A, Test B, and Reference channels. The other three are used during the calibration cycle.

Two A/D converters combine to provide 19 bits of resolution. An 8-bit D/A converter, a summing amplifier, and a successive approximation register (SAR) combine to form an 8-bit A/D converter. This A/D converter provides the most significant eight bits of the 19-bit word. Upon completion of the 8-bit conversion, a ±1-bit residue exists at the output of the analog summing amplifier. A 64-gain amplifier amplifies this signal then passes it to a 12-bit A/D for conversion into the least significant twelve bits. The I/O processor then reads these two digital words and combines them into a single 19-bit word. The most significant bit of the 12-bit word and the least significant bit of the 8-bit word overlap to guarantee continuity. Hardware linearity is severely limited by the ± ½ LSB accuracy of the 8-bit D/A converter. However, a software calibration algorithm measures the nonlinearity and mathematically compensates.

The overall A/D circuit has several functional modes. These include:

- Eight-bit conversion only (most significant byte).
- Twelve- bit conversion only (least significant byte).
- Eight- bit followed by twelve bit (full 19 bits).

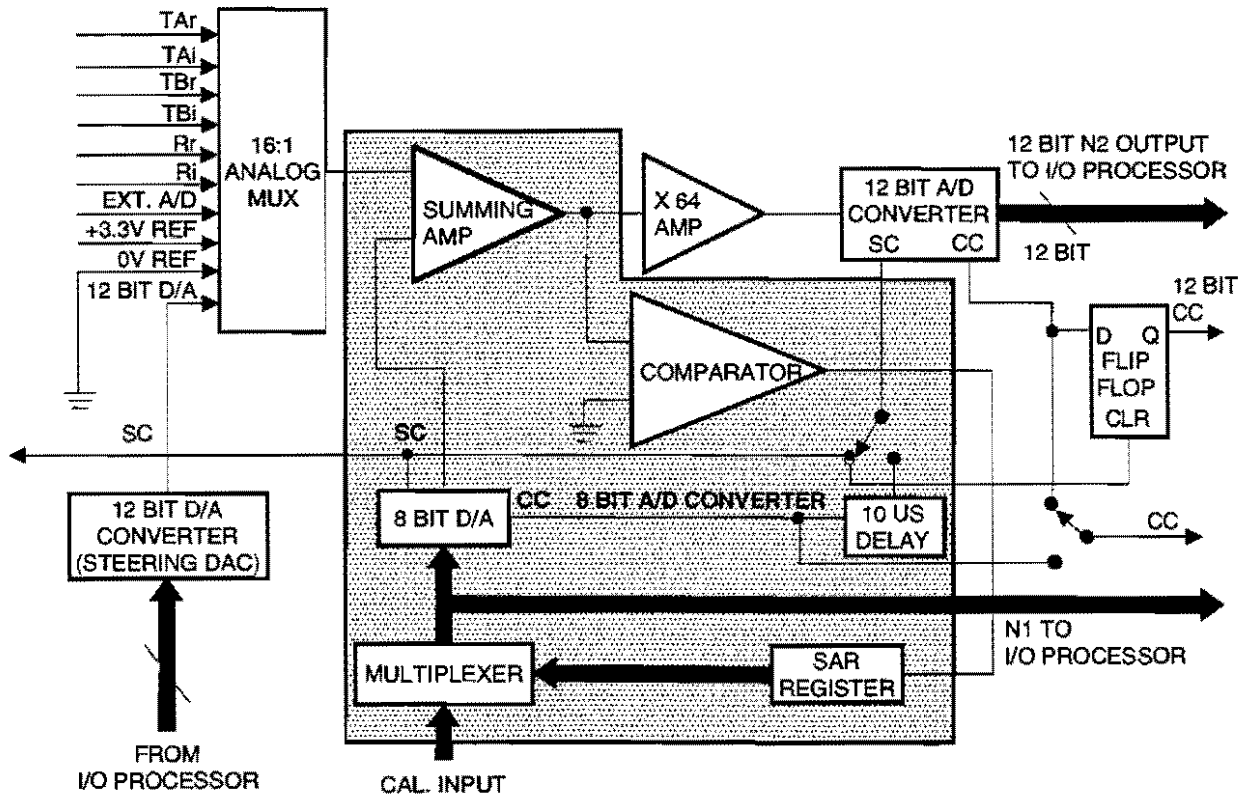


Figure 5-6. A4 A/D Converter PCB Block Diagram

A/D Control Signals

The start conversion signal (SC) controls when the conversion begins. The conversion complete signal (CC) indicates the conversion is completed. Depending on the functional mode of operation, the steering circuit routes the SC signal to the appropriate A/D converter and selects the appropriate CC signal. In the full 19-bit conversion mode, SC starts the 8-bit conversion. The 8-bit CC signal triggers a delay of 10 ms, then triggers the start of the 12-bit A/D conversion; 10 µs later, the CC signal indicates that the 12-bit conversion is complete.

Cal Mode

Once every 3 minutes the VNA performs a calibration cycle. During this cycle it measures and corrects errors or drifts that occur in the system. Two calibrations related to the A/D circuits are:

- Measurement of the 8 bit D/A's bit weights to allow for software compensation of any non-linear effects
- Measurement of the voltage standards allowing software compensation for gain and offset effects.

The analog multiplexer selects the input channel connected to the steering DAC. This is summed with the output of the 8-bit DAC. The I/O processor adjusts the steering DAC to keep the sum of its output and the output of the 8-bit D/A within the acceptable range of the 12-bit A/D's input.

The VNA, using the I/O processor and 12-bit A/D converter, measures the bit weights of the 8-bit DAC using the following procedure:

- Sets the 8 bit DAC to 2N–1.
- Adjusts the steering DAC's output.
- Changes the 8 bit DAC's output to 2 N.
- Measures the bit-weight difference [2N– (2N–1)].
- Compensates for the difference from ideal using software correction algorithms. This algorithm minimizes nonlinearities in the step sizes.

The A/D linearity is dramatically improved using the above algorithm. However, the performance of the 12 bit A/D limits the overall circuit's stability and accuracy. Temperature and aging affect the performance of the 12 bit A/D converter. This can result in gain and offset errors. To compensate for these errors, the 360B measures two reference voltages as part of the calibration cycle. These two voltages provide information that allows for software correction of the gain and offset errors.

5-8 A5 10 MHz REFERENCE PCB CIRCUIT DESCRIPTION

The A5 10 MHz Reference PCB (Figure 5-7) generates the system reference signal. The 10 MHz reference signal can come from either of two sources:

- The EXT 10 MHz REF connector on the rear panel. This input is for using an external reference source.
- The internal 10 MHz crystal oscillator in the 360B VNA.

The presence detector monitors the EXT 10 MHz input. When the presence detector detects an external input signal, it sets a bit that informs the I/O processor of the external signal. It also switches the input to the EXT 10 MHz input.

Regardless of the source, the 10 MHz sine wave then passes through a Schmidt trigger converting it to a square wave signal.

The signal branches to two places, as shown below:

- PCBs that require the 10 MHz reference signal. These include: A1, A2, A3, A6, A7, A8, A9, and A10.
- 12 MHz lowpass filter. This circuit filters the10 MHz square-wave signal to a sine wave by removing the harmonics. The sinusoidal signal is then available on the rear panel 10MHz OUT connector.

The level detectors are ANDed together to provide the I/O processor with a 10 MHz OK status bit.

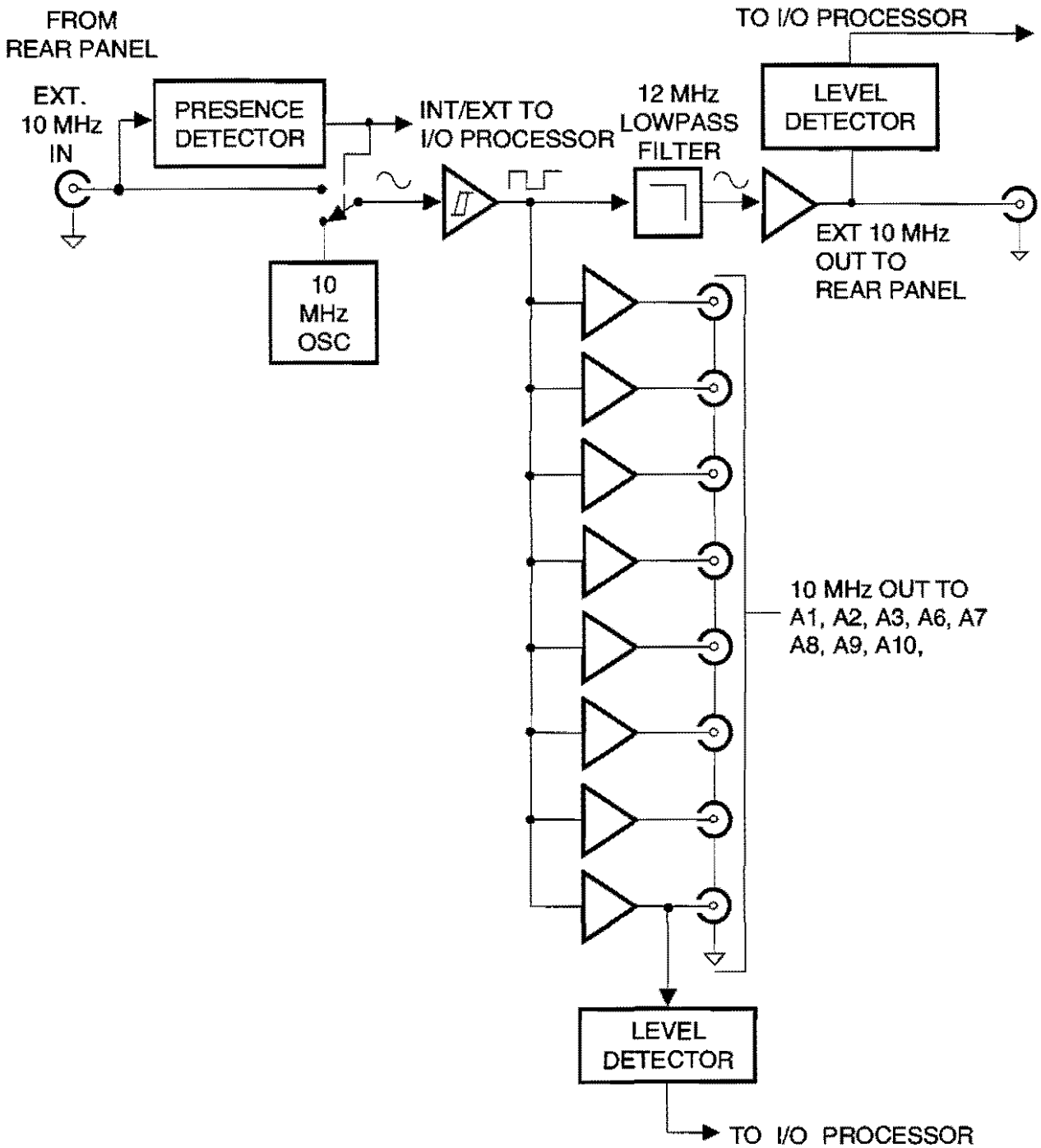


Figure 5-7. A5 10 MHz Reference PCB Block Diagram

5-9 A6 SOURCE LOCK PCB CIRCUIT DESCRIPTION

The A6 Source Lock PCB (Figure 5-8) provides source lock control. Its purpose is to phase-lock the source to the desired frequency and phase. A 10 MHz reference signal is divided to 1 MHz by a divide-by-10 circuit. This signal is phase-compared with a 1 MHz signal from a 9 MHz internal VCO that has been divided by nine. If the signals are in phase, the lock detect circuit sets a bit that relates this fact to the I/O processor.

The 9 MHz signal is also divided by 4. This results in a 2.25 MHz signal. Two phases — zero and ninety degrees — of this 2.25 MHz square-wave signal are then supplied to the phase-detect and lock-detect mixers.

The source-lock input is supplied to both of these mixers. The result of mixing produces the sums and differences of the signals. The sums, harmonics, and fundamental frequencies are filtered out of the lock detect mixer's output using a 3 MHz lowpass filter. When the frequencies are both 2.25 MHz, the difference is 0 Hz, or dc. The magnitude of the dc is proportional to the phase difference between the signals.

Depending on the polarity input from the I/O Processor, the dc is then either inverted or not inverted. This level is then compared with a threshold voltage (V_{TH}). If the level is greater than the threshold voltage, the output disables the search oscillator and signals the I/O processor that the sweeper is phase-locked. If the level is not equal to the threshold voltage, the search oscillator will increase or decrease the level resulting in a change in the FM phase lock level provided to the sweeper. This will change the output signal frequency. This process repeats itself until the sweeper locks to the correct frequency and phase.

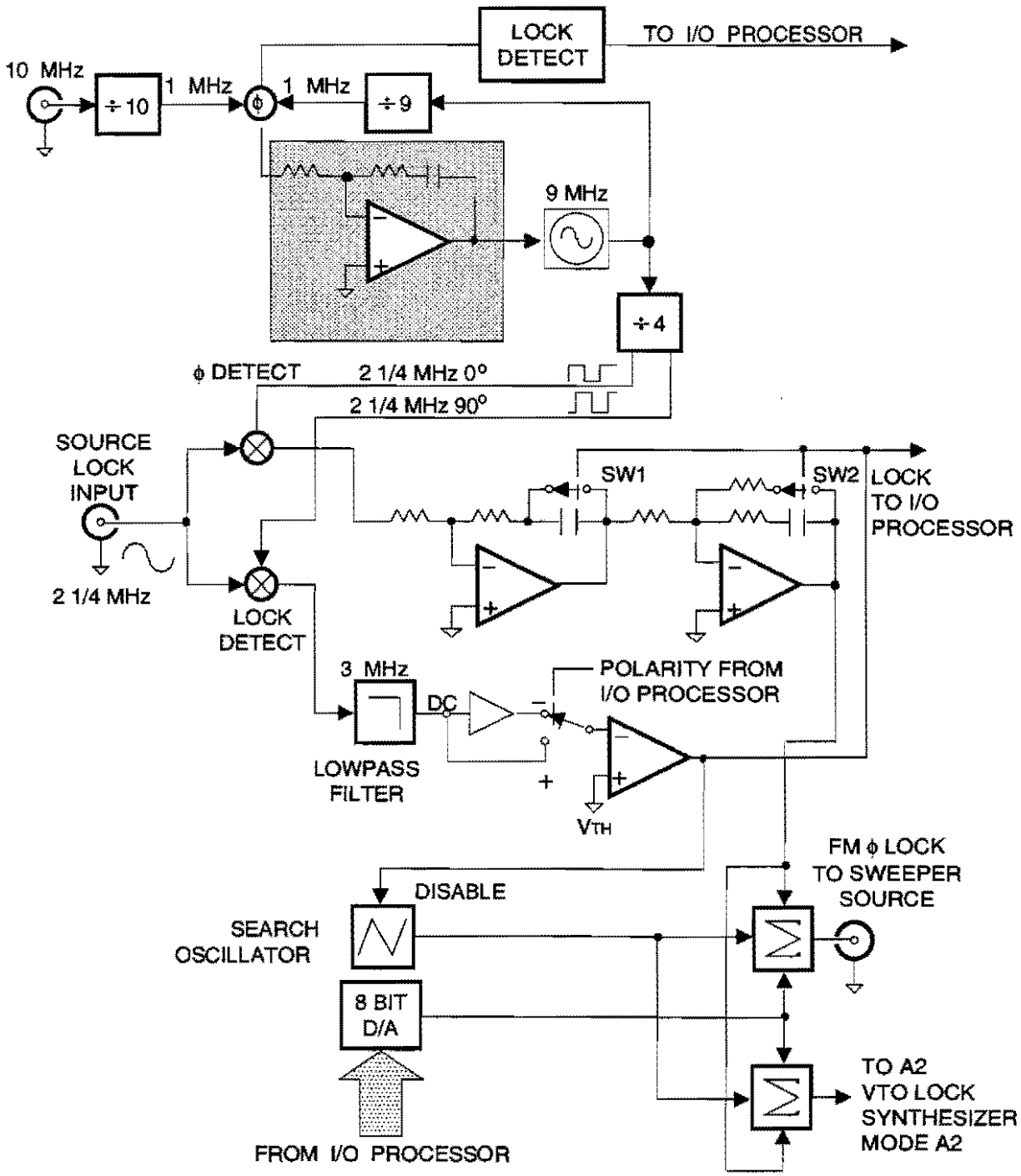


Figure 5-8. A6 Source Lock PCB Block Diagram

5-10 A7 SYNC DET "A" PCB CIRCUIT DESCRIPTION

The A7 Sync Det "A" PCB is a synchronous detector circuit. The I/O processor sends a phase byte to the divide-by-120 circuit (÷120). This byte addresses two look up tables. One produces the sine of the number from the divider. The other produces the cosine of the number from the counter.

Two multiplying D/A converters convert the outputs of the sine and cosine look-up ROMS to analog form. The multiplying D/A performs two functions—converting the digital signals to analog and producing sums and differences of the 83 1/3 kHz signals.

Since the frequencies of the converted signals and the input from the IF are both 83 1/3 kHz, the sum is 166.66 kHz and the difference is 0 Hz, or dc. The harmonics are filtered out with 100 kHz lowpass filters.

The outputs of the filters represent the sine and cosine functions and contain a dc element that is proportional to the magnitude and phase of the signals.These dc signals are then filtered out by the selection of the various bandpass filters (10 kHz, 1 kHz, and 100 Hz).

The outputs are buffered and applied to a sample-and-hold circuit. The output of the sample and hold circuit represents the magnitude of the IF signal's real and imaginary components.

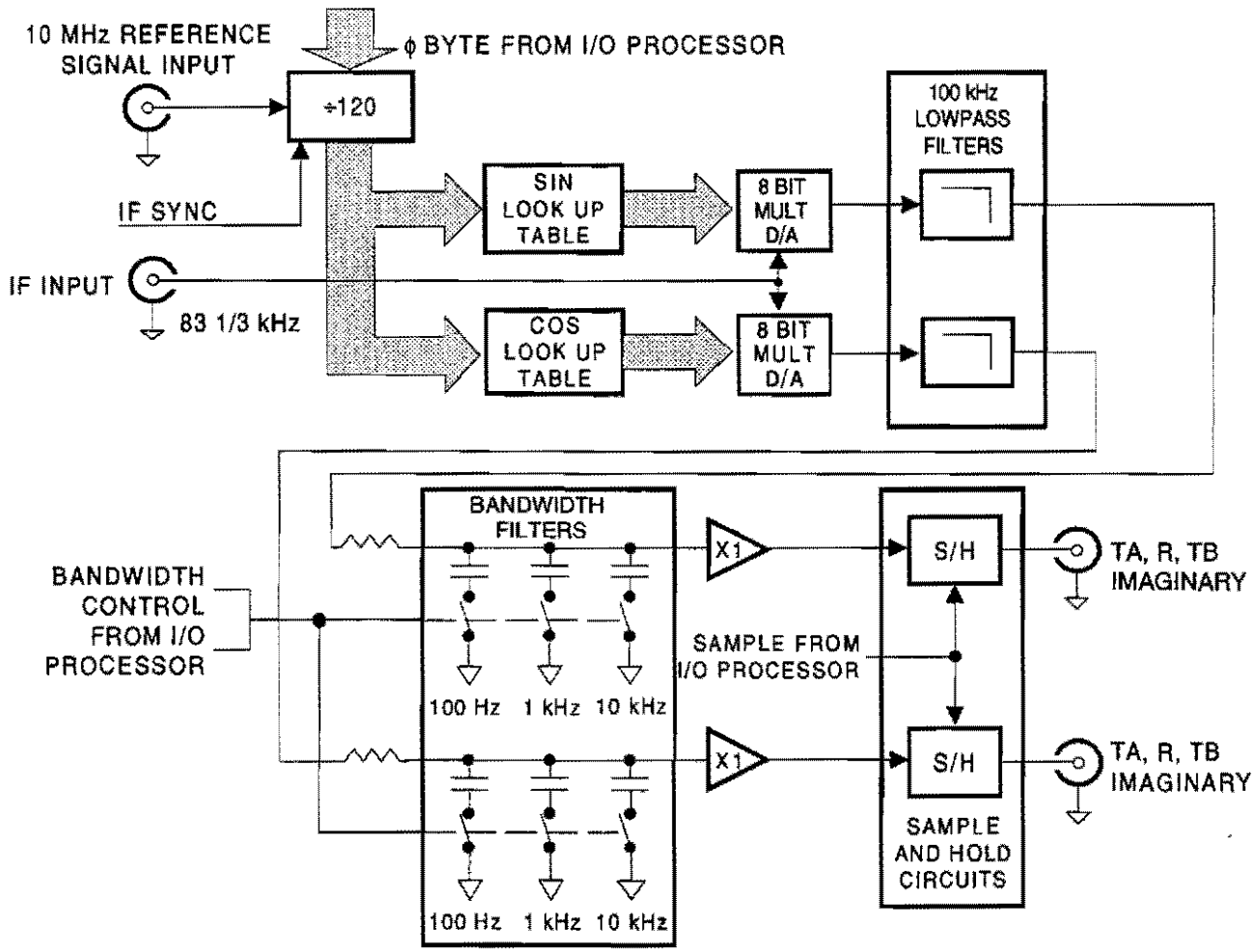


Figure 5-9. *A7 Sync Det "A" PCB Block Diagram*

5-11 A8 SYNC DET "B" PCB CIRCUIT DESCRIPTION

The A8 Sync Det "B" PCB (Figure 5-10) is a synchronous detector circuit. The I/O processor sends a phase byte to the divide-by-120 counter (÷120). This byte addresses two look up tables. One produces the sine of the number from the divider. The other produces the cosine of the number from the counter. Two multiplying D/A converters convert the outputs of the sine and cosine look-up ROMS to analog form. The multiplying A/D performs two functions, which are converting the digital signals to analog form and producing sums and differences of the 83 1/3 kHz signals.

Since the frequencies of the converted signals and the input from the IF are both 83 1/3 kHz, the sum is 166.66 kHz and the difference is 0 Hz, or dc. The harmonics are filtered out with 100 kHz lowpass filters.

The outputs of the filters represent the sine and cosine functions and contain a dc element that is proportional to the magnitude and phase of the signals. The dc signals are then filtered out by the selection of the various bandpass filters (10 kHz, 1 kHz, and 100 Hz).

The outputs are buffered and applied to a sample-and-hold circuit. The output of this circuit represents the magnitude of the IF signal's real and imaginary components.

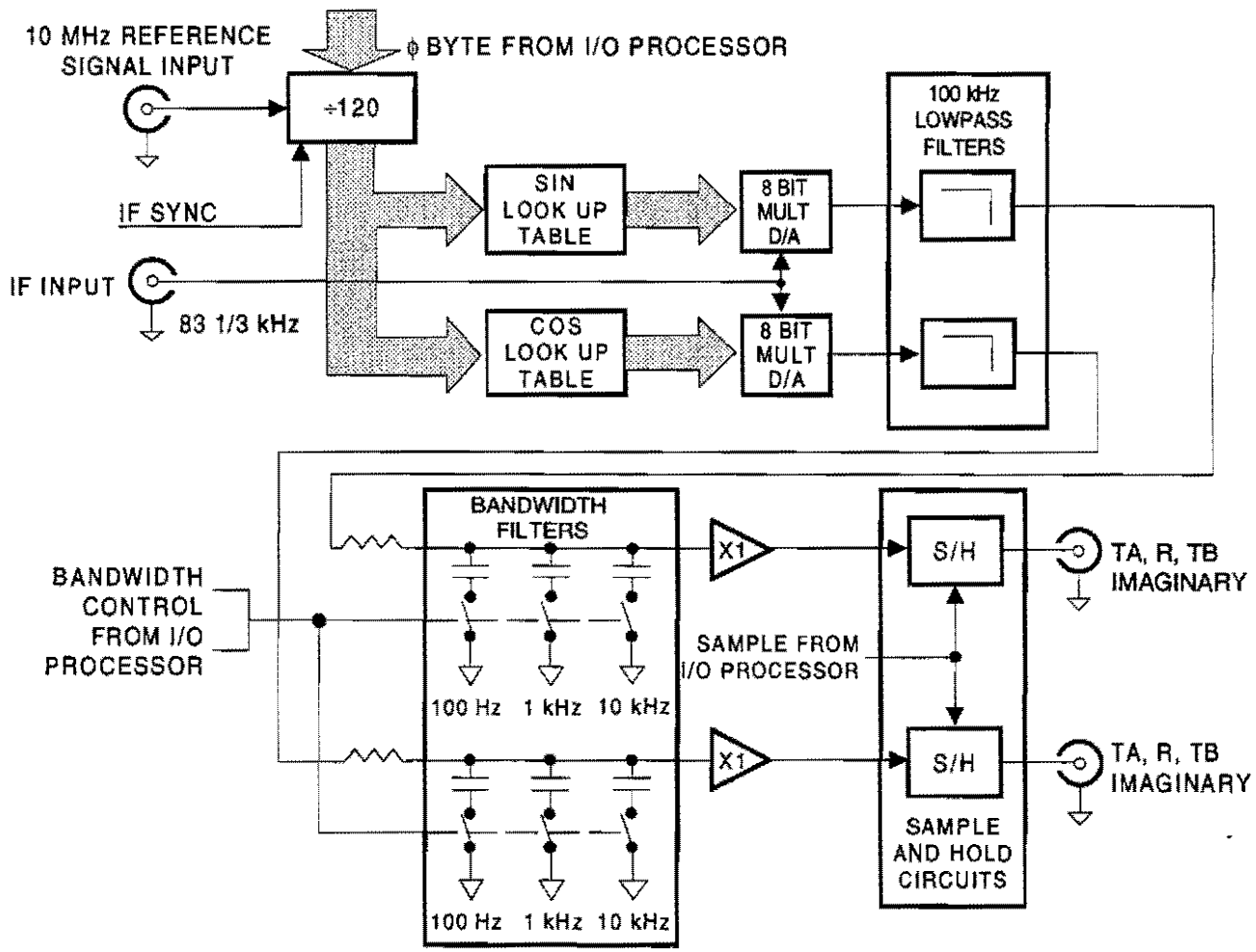


Figure 5-10. A8 Sync Det "B" PCB Block Diagram

5-12 A9 SYNC DET "R" PCB CIRCUIT DESCRIPTION

The A9 Sync Det "R" PCB (Figure 5-11) is a synchronous detector circuit. The I/O processor sends a phase byte to the divide-by-120 counter (÷120). This byte addresses two look up tables. One produces the sine of the number from the divider. The other produces the cosine of the number from the counter.

Two multiplying D/A converters convert the outputs of the sine and cosine look-up ROMS to analog form. The multiplying A/D performs two functions, which are converting the digital signals to analog form and producing sums and differences of the 83 1/3 kHz signals. Since the frequencies of the converted signals and the input from the IF are both 83 1/3 kHz, the sum is 166.66 kHz and the difference is 0 Hz, or dc.

The harmonics are filtered out with 100 kHz lowpass filters. The outputs of the filters represent the sine and cosine functions and contain a dc element that is proportional to the magnitude and phase of the signals. These are then filtered out by the selection of the various bandpass filters (10 kHz, 1 kHz, and 100 Hz).

The outputs are buffered and applied to a sample and hold circuit. The output of the sample and hold circuit represents the magnitude of the IF signal's real and imaginary components.

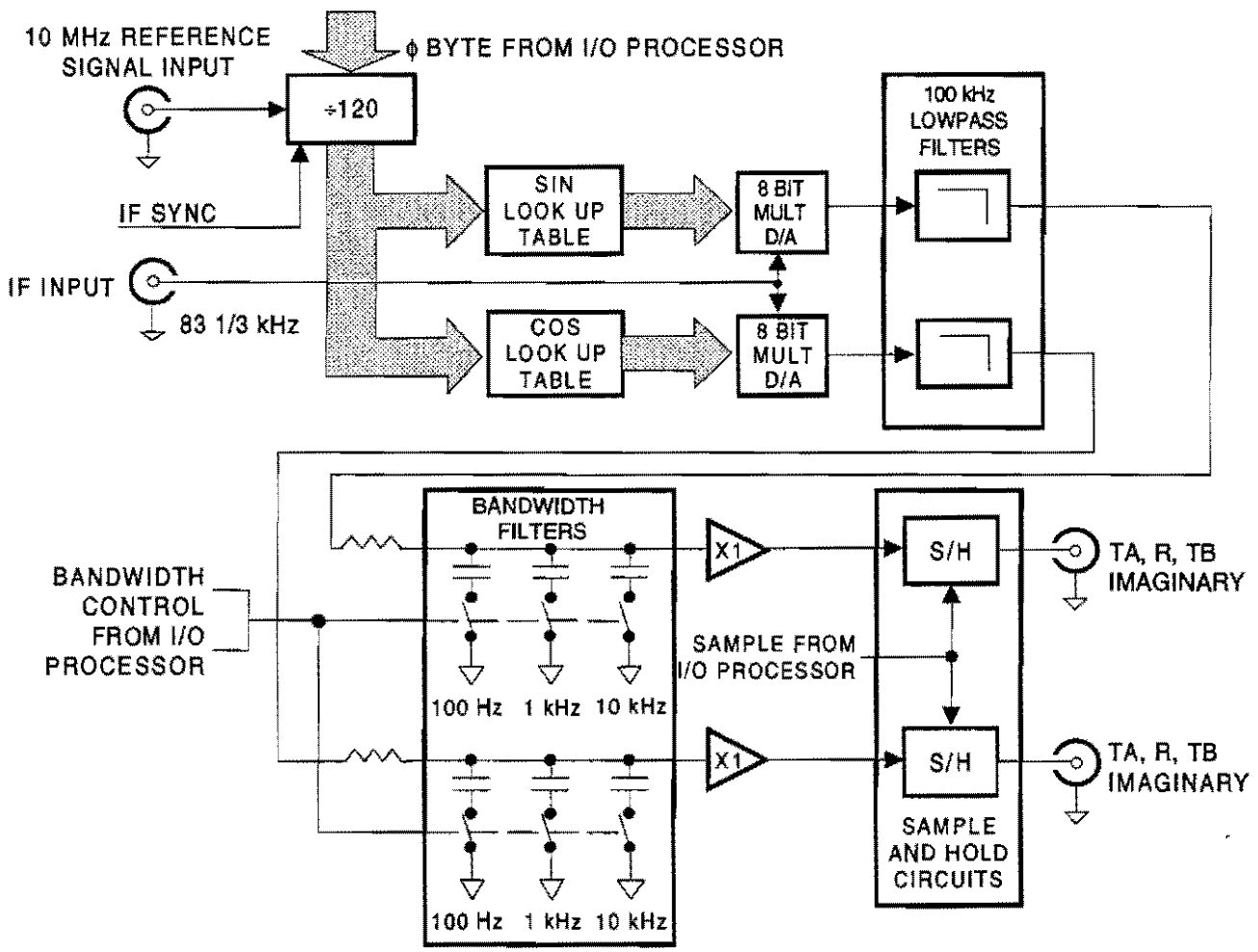


Figure 5-11. A9 Sync Det "R" PCB Block Diagram

5-13 A10 PS/IF PCB CIRCUIT DESCRIPTION

The A10 PS/IF PCB (Figure 5-12) is the external digital control board. This board has many functions including:

- Power supply synchronization
- IF synchronization
- Pulse catching of external digital control pulses
- Serial number identification
- ±10V external voltage generation

The power supply synchronization consists of two circuits. A divide-by-45 divider reduces the 10 MHz reference signal to the necessary 222 kHz signal required for power supply synchronization. A presence detector circuit informs the I/O processor that the 222 kHz signal is present.

Similarly, the IF synchronization consists of two circuits. A divide-by-120 divider reduces the 10 MHz reference signal frequency to the necessary 83 1/3 kHz required for synchronization. A presence detector informs the I/O processor of the presence of this signal.

The pulse catching circuit performs three basic functions. It converts any external input pulses to the absolute value of the input pulse. This means that regardless of the polarity of the pulse it will be converted to the proper polarity by the absolute value (ABS) circuit.

A Schmitt trigger cleans up the edges of this pulse. The pulse catching circuit stores the pulse until the I/O processor has time to read it. After the pulse is read, the microprocessor tells the I/O processor if more than one pulse has been received since the I/O processor last read the output of the catching circuit. This eliminates the need for synchronization between the external pulse generator and the I/O processor. Additionally it frees the I/O processor from having to constantly poll the external pulse input.

The mainframe serial number ID is factory set and addresses a number that is unique to each instrument. It is important to note that the switch bank should never be changed or application programs designed for operation on the specific unit will not function.

The ±10 volt output to the rear panel is provided for an analog output to the VNA. This voltage level is derived from a 12-bit D/A converter that converts a digital word from the I/O processor into the desired voltage level out.

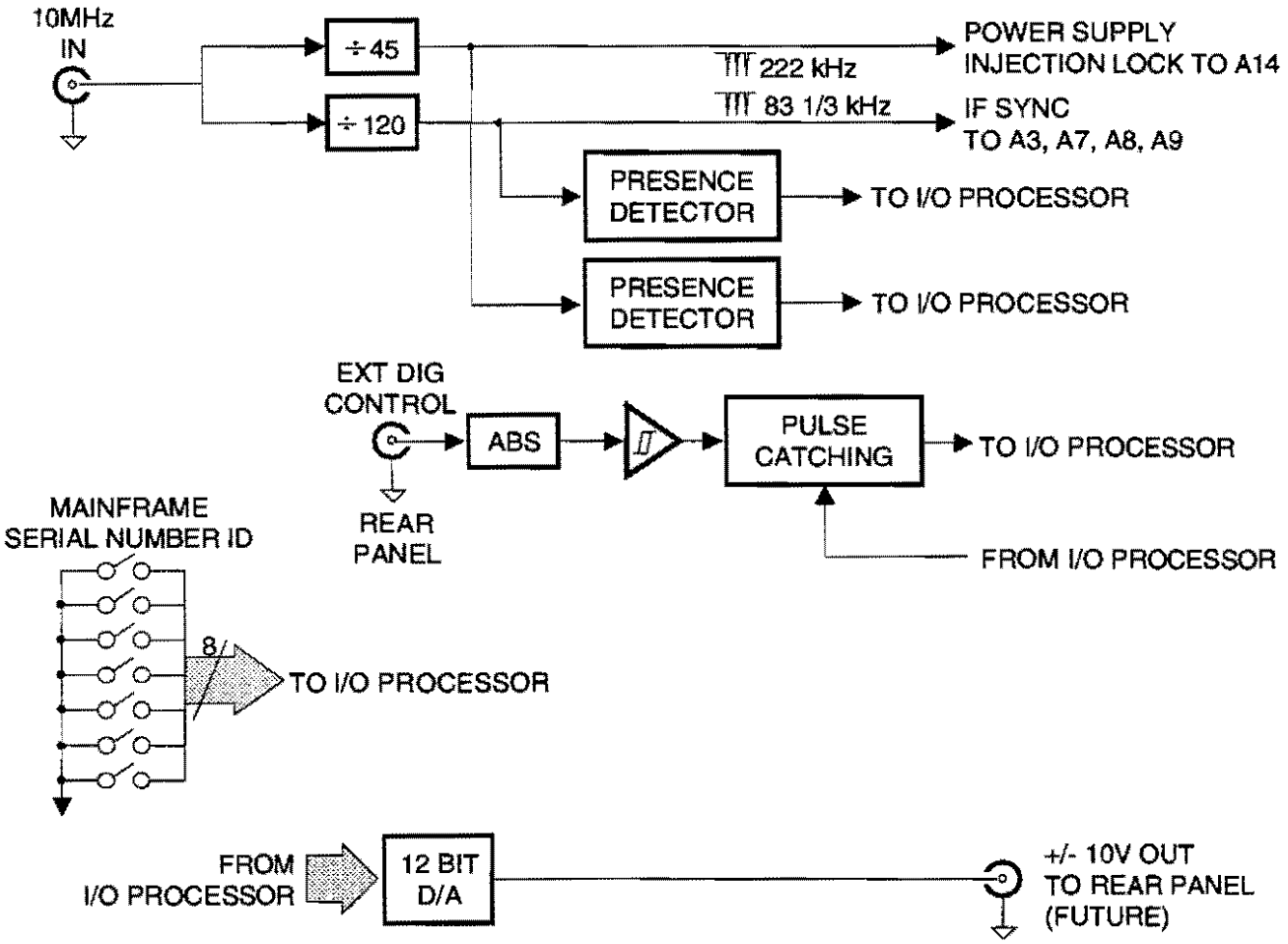


Figure 5-12. A10 P.S./I.F. PCB Block Diagram

5-14 A11 I/O PROCESSOR PCB CIRCUIT DESCRIPTION

The A11 I/O Processor PCB (Figure 5-13) controls the operation of the signal source and plotter through a dedicated GPIB interface bus. It controls the test set through a dedicated digital bus. This processor also controls all analog circuits and processes and corrects the data from the A/D converter.

The I/O processor is an 8088 microprocessor based system. It has 128 K bytes of on-board RAM. A UPD7210C GPIB bus controller IC controls the talker, listener, and controller functions of the GPIB. This IC combined with two bus transceiver ICs perform the necessary handshaking and interface to the GPIB bus. Two FIFOs interface to the A13 PCB processor. One FIFO is responsible for storing data to be read from the A13 PCB, the other stores data that is to be sent to the A13 PCB. In addition to the 128 K bytes of on-board RAM, 192 K bytes of RAM is dedicated as graphics memory. A UPD7220ADC graphics processor controls the interface to the CRT. All inputs and outputs to the I/O processor are buffered, this includes interface to the following:

- Pixel Data to the CRT
- A12 Data
- Mainframe Data
- Test Set Control
- 16 K bytes of EPROM for internal self-test and booting

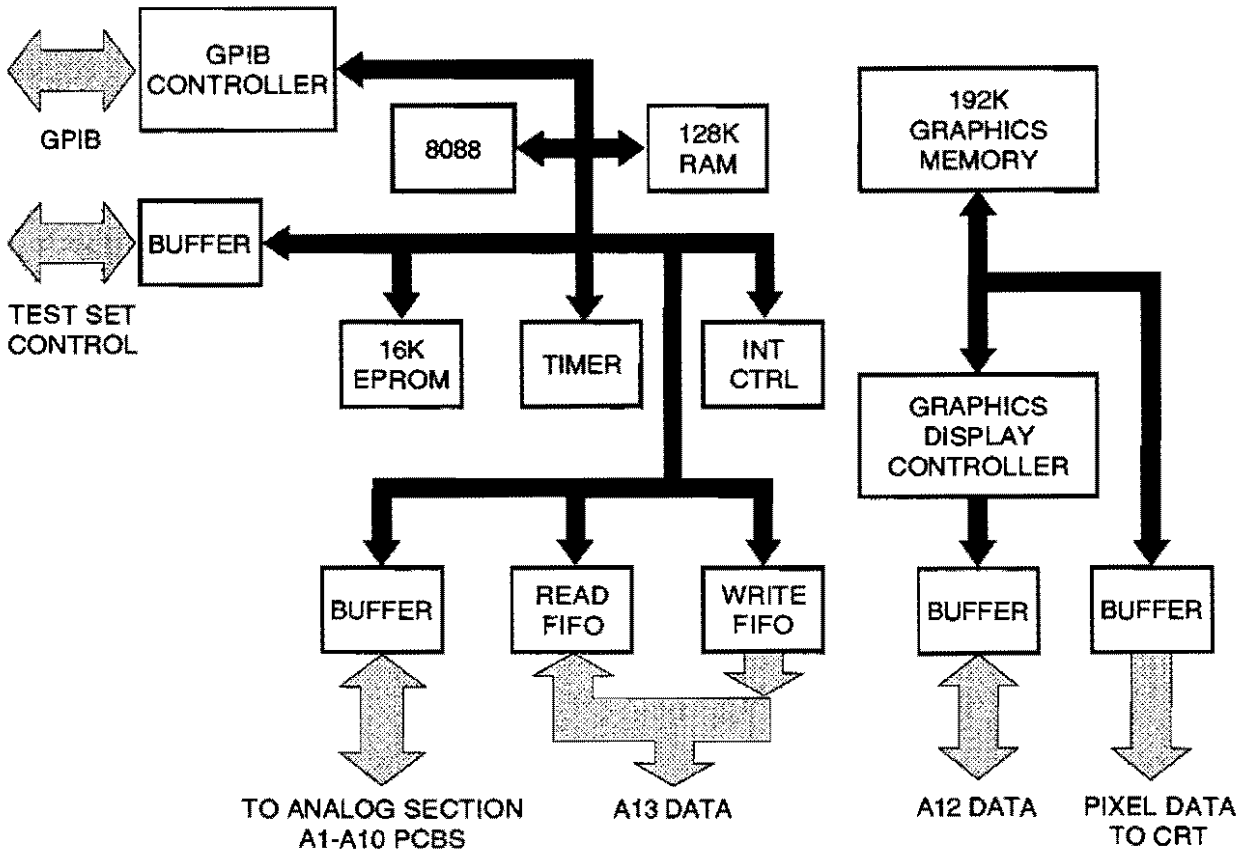


Figure 5-13. *A11 I/O Processor PCB Block Diagram*

5-15 A12 MAIN 2 PROCESSOR PCB CIRCUIT DESCRIPTION

The A12 Main 2 Processor PCB (Figure 5-14) is the human interface processor. It is one of three microprocessor based circuits. The human interface processor controls the interaction with the front panel, the external GPIB bus, and the parallel printer. Additionally it gives commands to the graphics control processor to create the various display functions.

The heart of the circuit is an 8088 microprocessor chip. An 8087 numeric coprocessor complements the 8088 and performs the numerical calculations. This greatly improves speed and frees the 8088 for other tasks.

The 8088 addresses 1024 K (1 M byte) of volatile RAM and 32 K of battery-backed nonvolatile RAM. The interface to the GPIB is handled through a UPD 7210C dedicated GPIB controller.

An 8254 programmable timer generates interrupts on a 10-second interval. This allows for update of a counter for real-time clock emulation. The read and write FIFOs carry information between the processors on the A11, A12, and A13 PCBs.

Data can also be transferred to and from the A11 PCB (I/O Processor) using a buffer.

16 K bytes of EPROM are provided for self-test and boot-up.

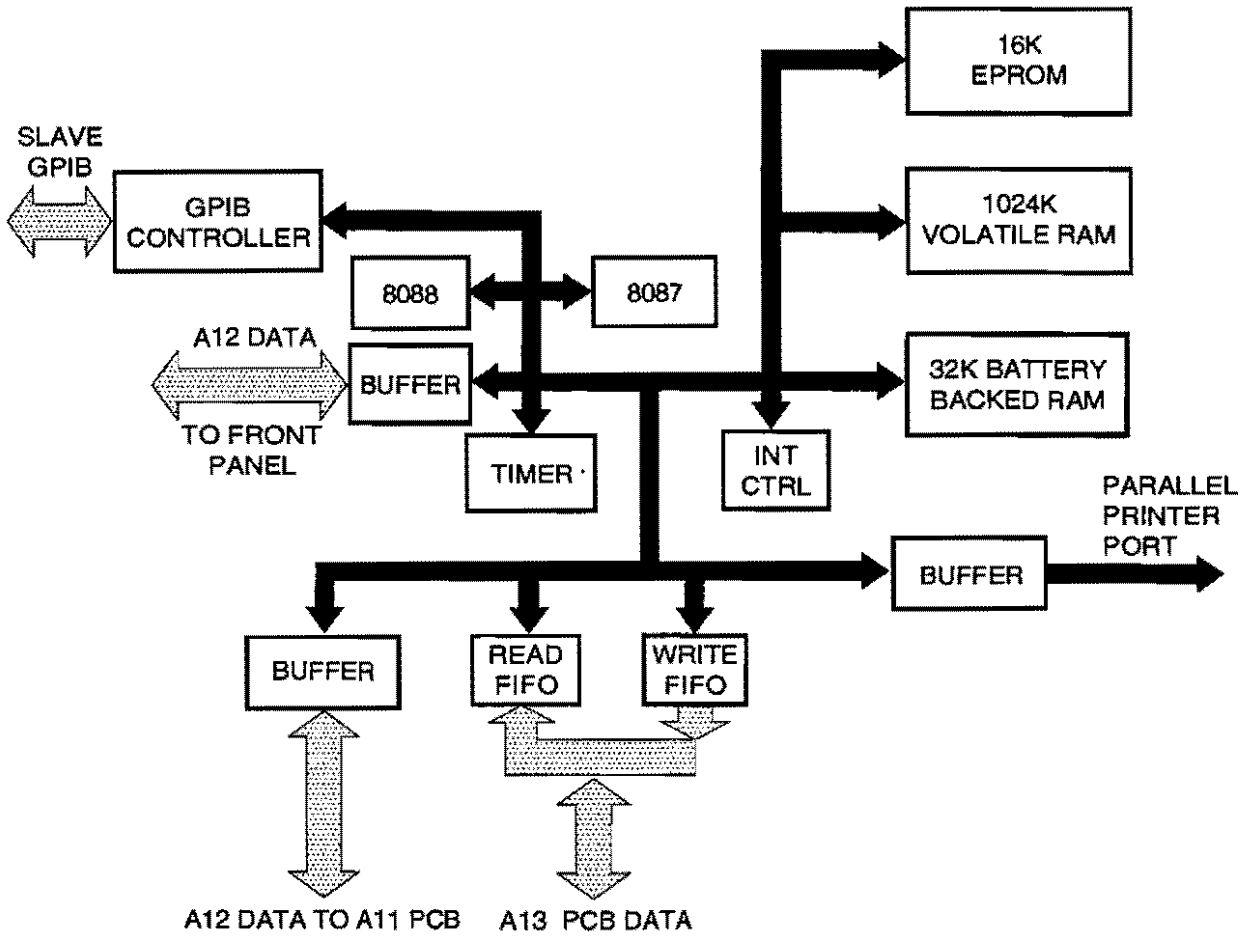


Figure 5-14. *A12 Main 2 Processor PCB Block Diagram*

5-16 A13 MAIN 1 PROCESSOR PCB CIRCUIT DESCRIPTION

The A13 Main 1 Processor PCB (Figure 5-15) is the vector processor. It is also called the Main #1 processor. The vector processor processes data received from the I/O processor via the FIFO registers. This includes the ratioing of the transmission/reflection variables to calculate the S-parameters and the necessary error correction and accuracy enhancements.

The Main #1 Processor has an 8088 microprocessor that works in conjunction with an 8087 numeric co-processor. An MC3201 floppy disk controller chip interfaces to the 3.5 inch floppy disk drive. The system has 512K of internal RAM. An 8259A generates interrupts for the disk drive and timer. 16 K bytes of EPROM are provided for self-test and boot-up. Time domain hardware (DSP and 32 K byte of static RAM) are also on this PCB.

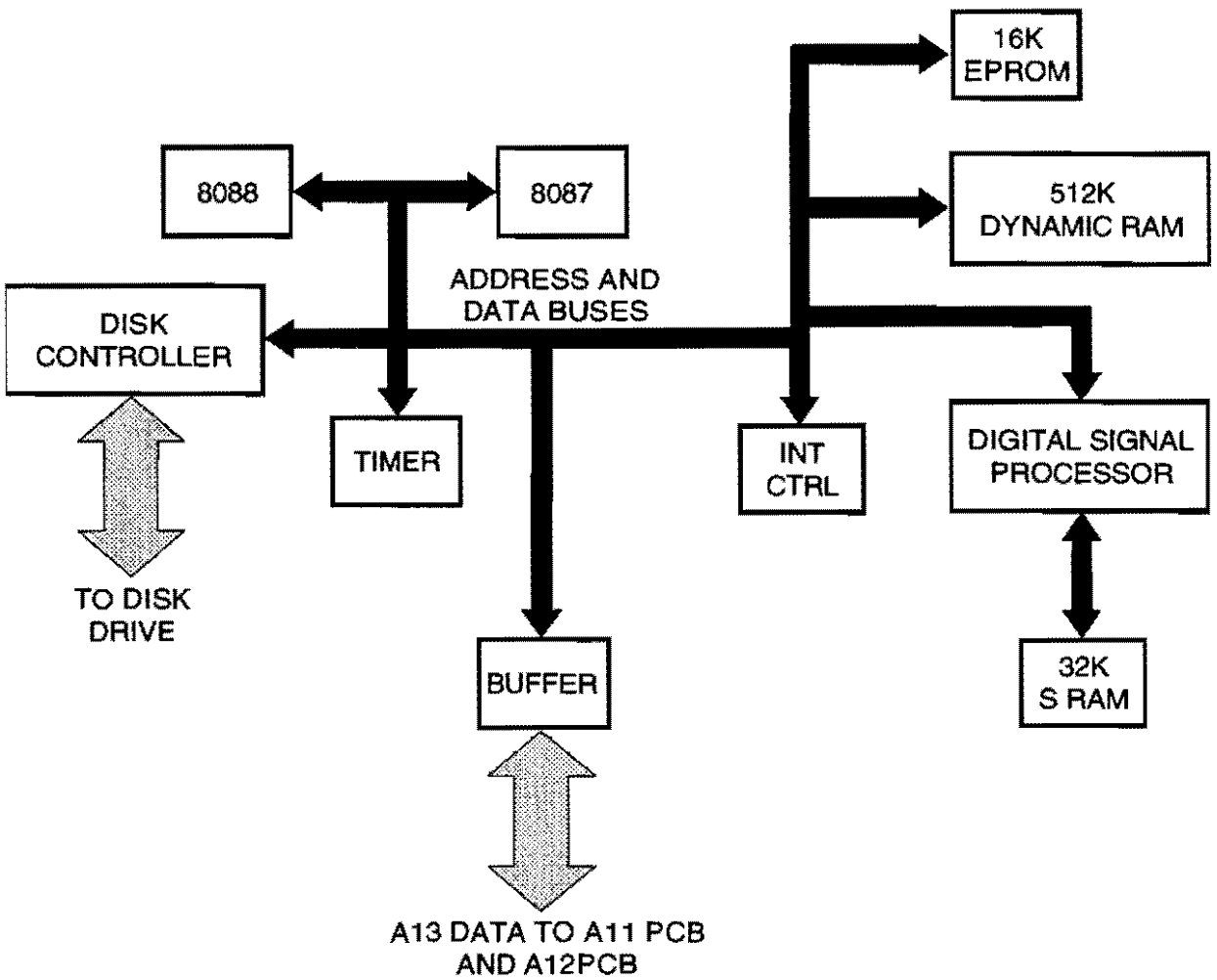


Figure 5-15. A13 Main 1 Processor PCB Block Diagram

5-17 A14 POWER SUPPLY CONTROL PCB CIRCUIT DESCRIPTION

The A14 Power Supply Control PCB (Figure 5-16) controls the power supply. It has the following functions:

- Controlling the regulation of the switching power supply
- Over-voltage protection
- Over-temperature protection
- Over-current Protection
- Line voltage level detection
- Level translation for the video monitor

The controlling element is the pulse width modulator (PWM). The duty-cycle of its output pulse directly controls output voltage. It has two outputs that drive the power FETs on the A15 PCB. It has four inputs:

- 111 kHz reference signal. This signal is derived from the 222 kHz signal. A ÷2 circuit divides this signal in half.
- Shut Down. This input tells the PWM to shutdown the power supply. Three levels are OR'ed together to produce this output. They are the over-temperature, overvoltage, and regulation-detect. If any of these levels are high the shut-down level will be HIGH.
- +18VDC. This voltage starts the PWM. The 18V level comes from the rectified 18VAC winding of the 60 Hz transformer. It provides the PWM with the necessary startup voltage until the 18V dc output voltage stabilizes. The 18 Vac signal from the 60 Hz input transformer is also sensed by the Hi-Low Line Detector. This sends data to the I/O processor indicating the condition of the ac line voltage.
- V Control. This input controls the duty cycle of the PWM. The duty cycle of the PWM controls the on and off time of the power FETs on the A15 PCB. This controls the output voltage of the power supply regulator.

The loop amplifier has a 5.3 Vdc reference voltage on the non-inverting input. The operational amplifier changes the output such that the voltage on the inverting input matches that on the non-inverting input. This changes the input to the voltage-control pin of the PWM. The voltage change causes a change in the PWM output duty-cycle. The duty-cycle change results in a change of the regulated output voltage.

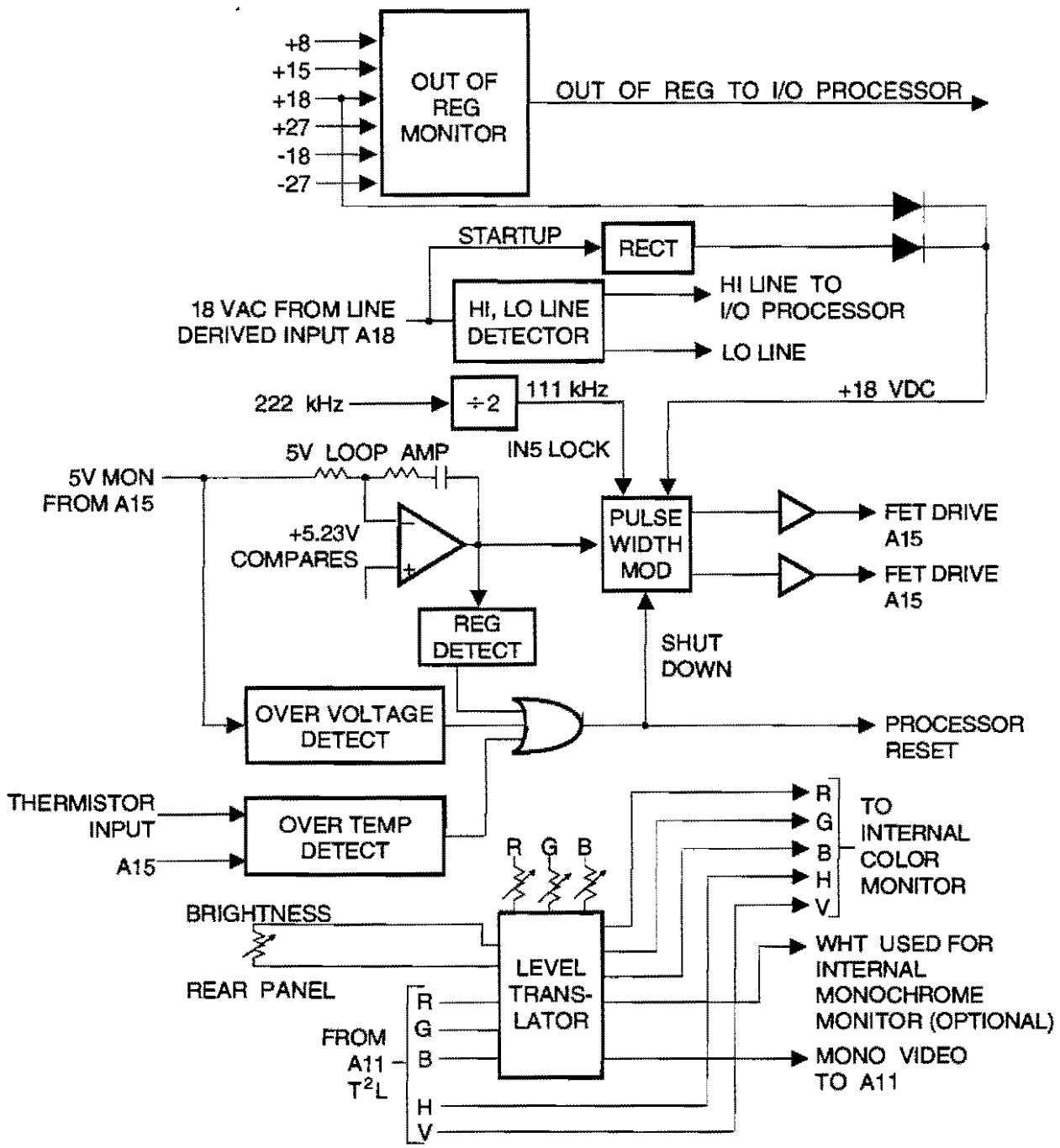


Figure 5-16. *A14 Power Supply Control PCB Block Diagram*

5-18 A15 POWER SUPPLY CONVERTER PCB CIRCUIT DESCRIPTION

The A15 Power Supply Converter PCB (Figure 5-17) is a dc-to-dc converter that converts ±165V from the A18 PCB to a variety of filtered dc voltage levels. These filtered voltages are then regulated on the PCBs that use them.

Two power MOSFETs drive the primary of transformer T1. They are biased with a ±165V dc voltage. This gives adequate drive voltage to drive the primary of the transformer. The pulse-width modulated signals from the A14 PCB turn the power MOSFETs on and off.

The secondary circuits are typical power supply rectifier and filter circuits. Each of them use the appropriate taps off the secondary of T1. The drive signals to the power MOSFETs are approximately 111 kHz. This produces very high frequency, easily filtered ripple signals.

A thermistor is physically mounted on the heat sink of the power MOSFETs. This provides feedback to the over-temperature detector circuit on the A14 PCB. The over-temperature detector shuts the power supply down when the temperature crosses a pre-defined threshold.

The PWM on A14 PCB performs the shutdown of the signals driving the power MOSFETs. The functional block diagram illustrates the waveforms at various points in the circuit.

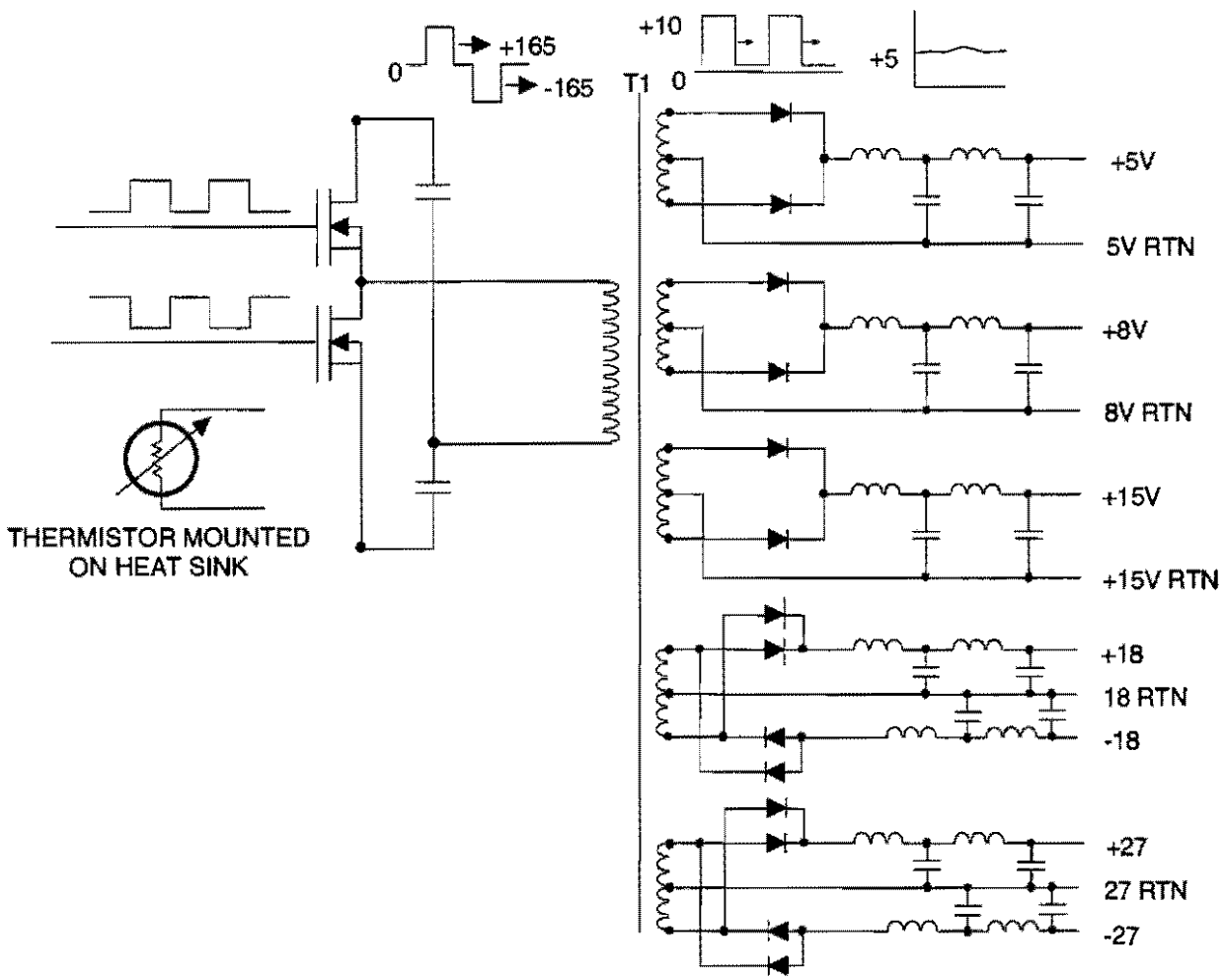


Figure 5-17. A15 Power Supply Converter PCB Block Diagram

5-19 A16 TEST SET I/O PCB CIRCUIT DESCRIPTION

The A16 Test Set I/O PCB (Figure 5-18) provides fused dc voltages to the test set. The A18 PCB supplies the raw dc voltages to the A16 PCB.

The voltage values are +8V, ±18V, and ±27V. Additionally the A16 PCB generates a timing strobe that synchronizes activities between the test set and the analyzer mainframe.

This PCB also monitors the voltage levels of the dc power. These circuits are called power detect circuits.

5-20 A17 SYSTEM MOTHERBOARD PCB CIRCUIT DESCRIPTION

The A17System Motherboard PCB acts as a conduit between all of the other PCBs in the system. Additionally it has circuitry that ensures the proper power-up sequence of the 3.5 inch diskette drive.

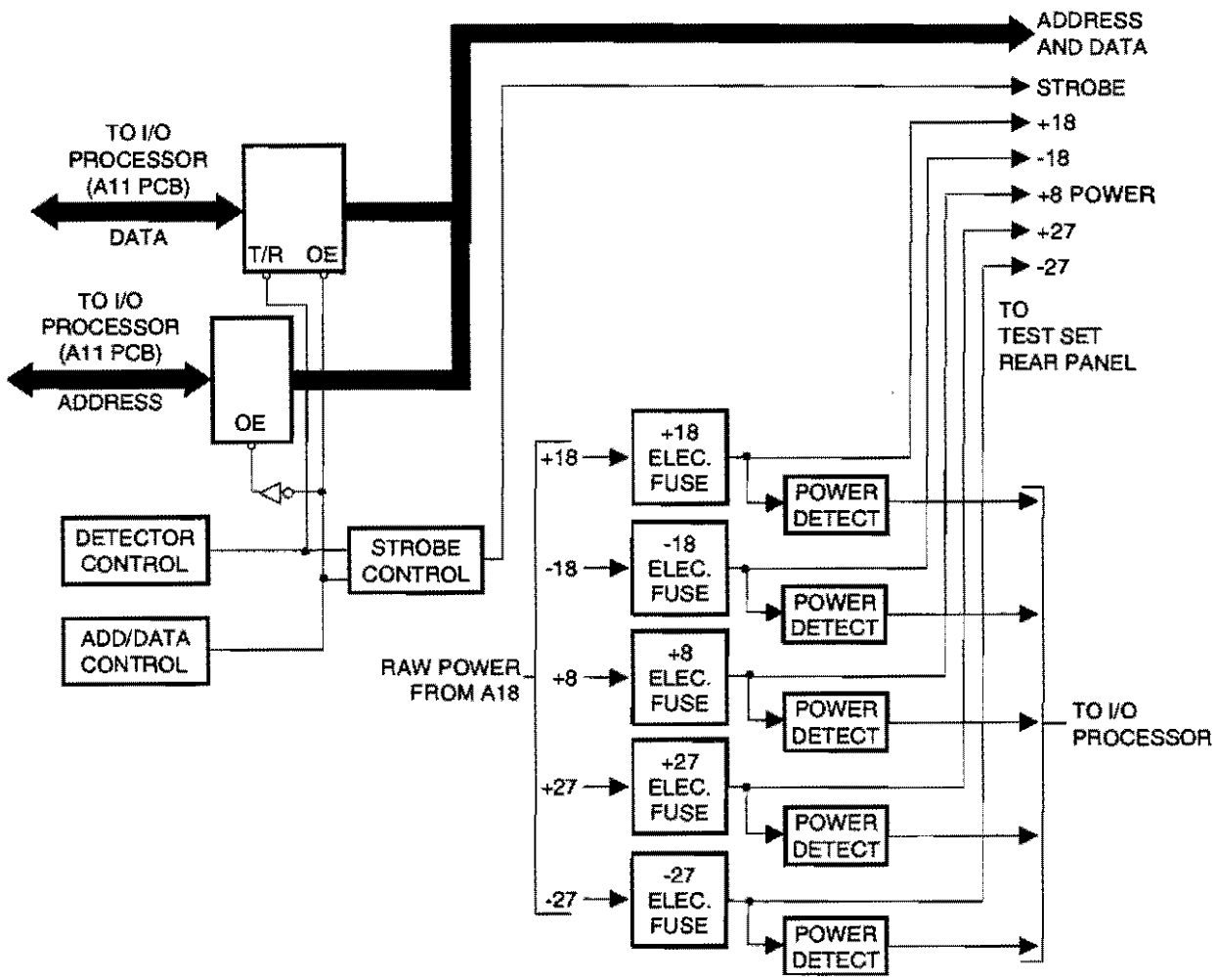


Figure 5-18. A16 Test Set I/O PCB Block Diagram

5-21 A18 POWER SUPPLY MOTHERBOARD PCB CIRCUIT DESCRIPTION

The A18 Power Supply Motherboard PCB (Figure 5-19) the following functions:

- Provides power supply bus and connectors for the power supply PCBs.
- Contains the rectifiers and filters for the ±165 Vdc that biases the power MOSFETs on the A15 PCB.
- Provides the interface to the rear-panel line fuse.
- Provides interface to the rear-panel 110/220V line voltage selector.
- Provides the step-down 18V start-up transformer.
- Provides EMI filtering.
- Regulates the monitor voltage from the A15 PC.

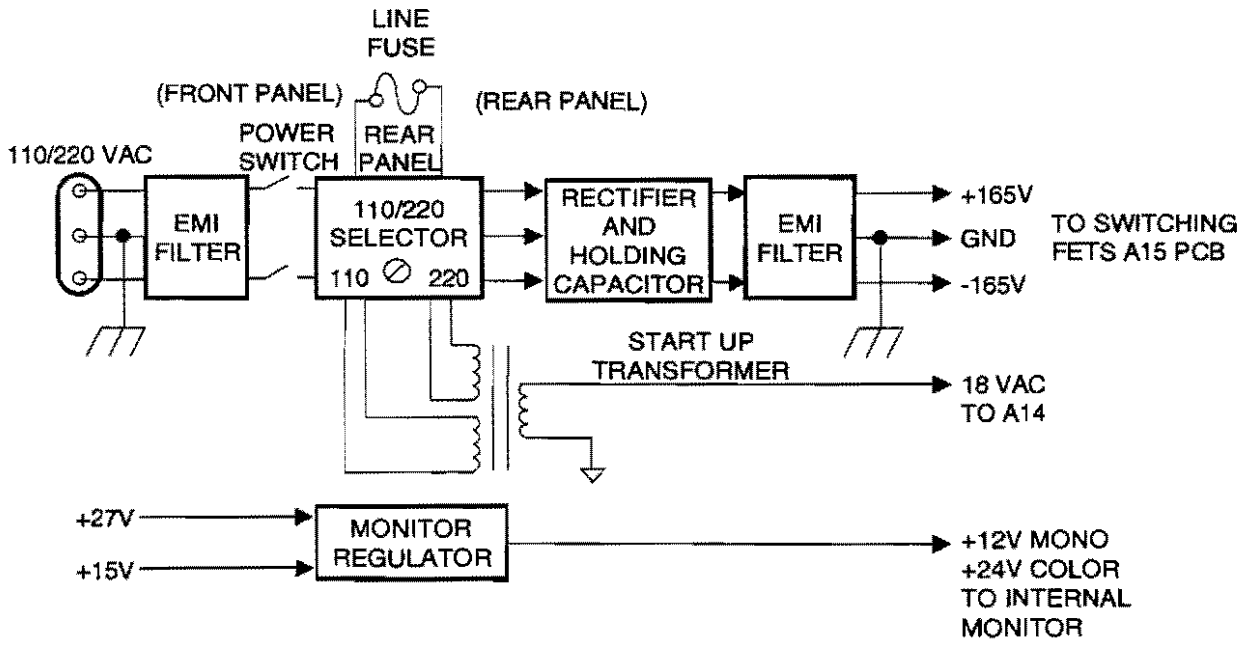


Figure 5-19. *A18Power Supply Motherboard PCB Block Diagram*

5-22 A19 FRONT PANEL, MAIN, PCB CIRCUIT DESCRIPTION

The A19 Front Panel, Main, PCB (Figure 5-20) is the main front panel circuit board. It contains the switch matrix of all front panel switches. It also has the front panel LEDs mounted on it, as well as the digital front panel knob.

The information coming to and from the front panel interfaces to the A20 PCB.

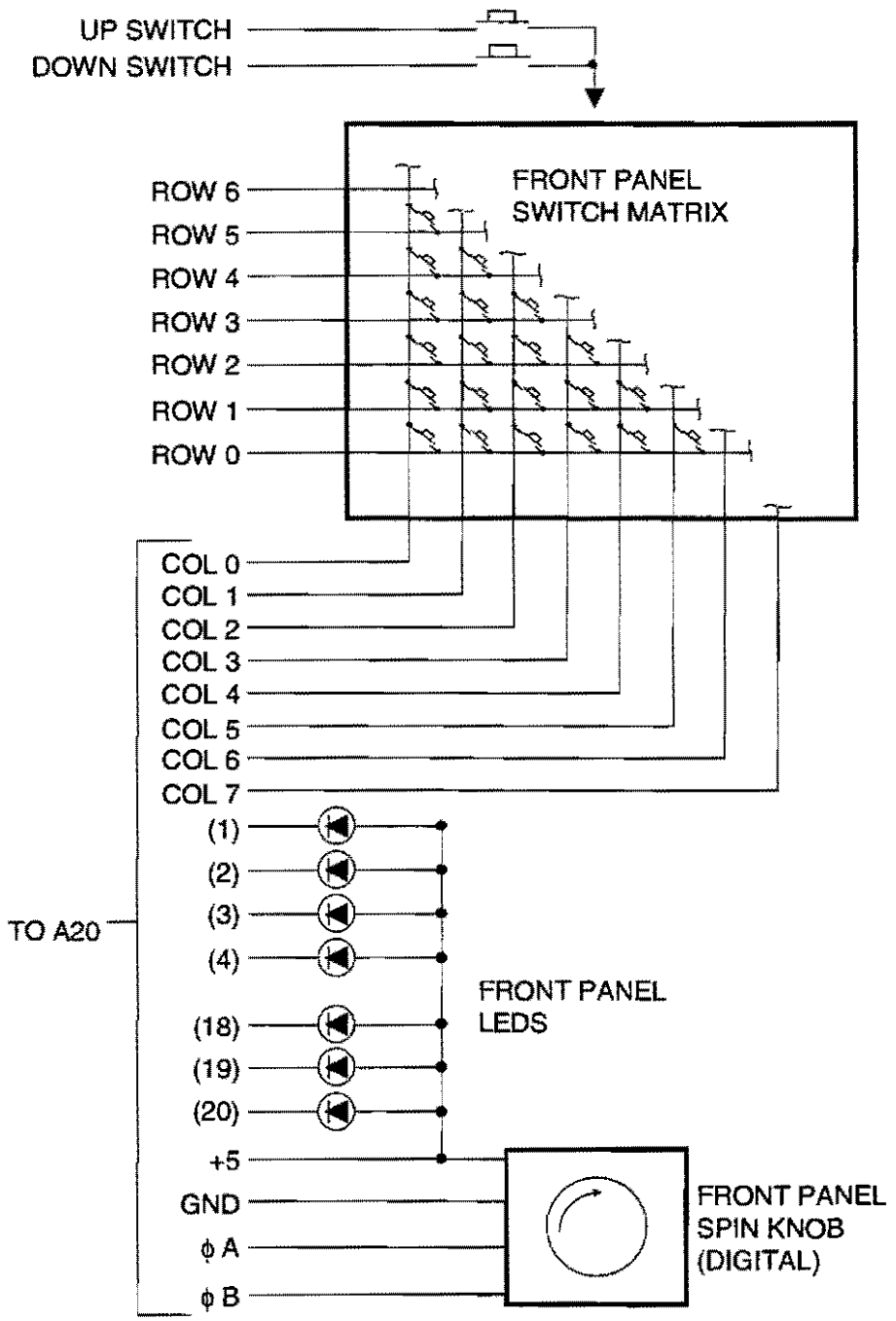


Figure 5-20. A19 Front Panel, Main, PCB Block Diagram

5-23 A20 FRONT PANEL CONTROL PCB CIRCUIT DESCRIPTION

A20 Front Panel Control PCB (Figure 5-21) is the digital front-panel control board. It contains all of the decode logic and key-scan circuitry for the front panel switches and the digital rotary knob.

Additionally it contains the necessary drivers and buffers for the beeper as well as all of the front-panel LEDs.

An Intel 8279 acts as a key-scan decoder to decode the front-panel switches.

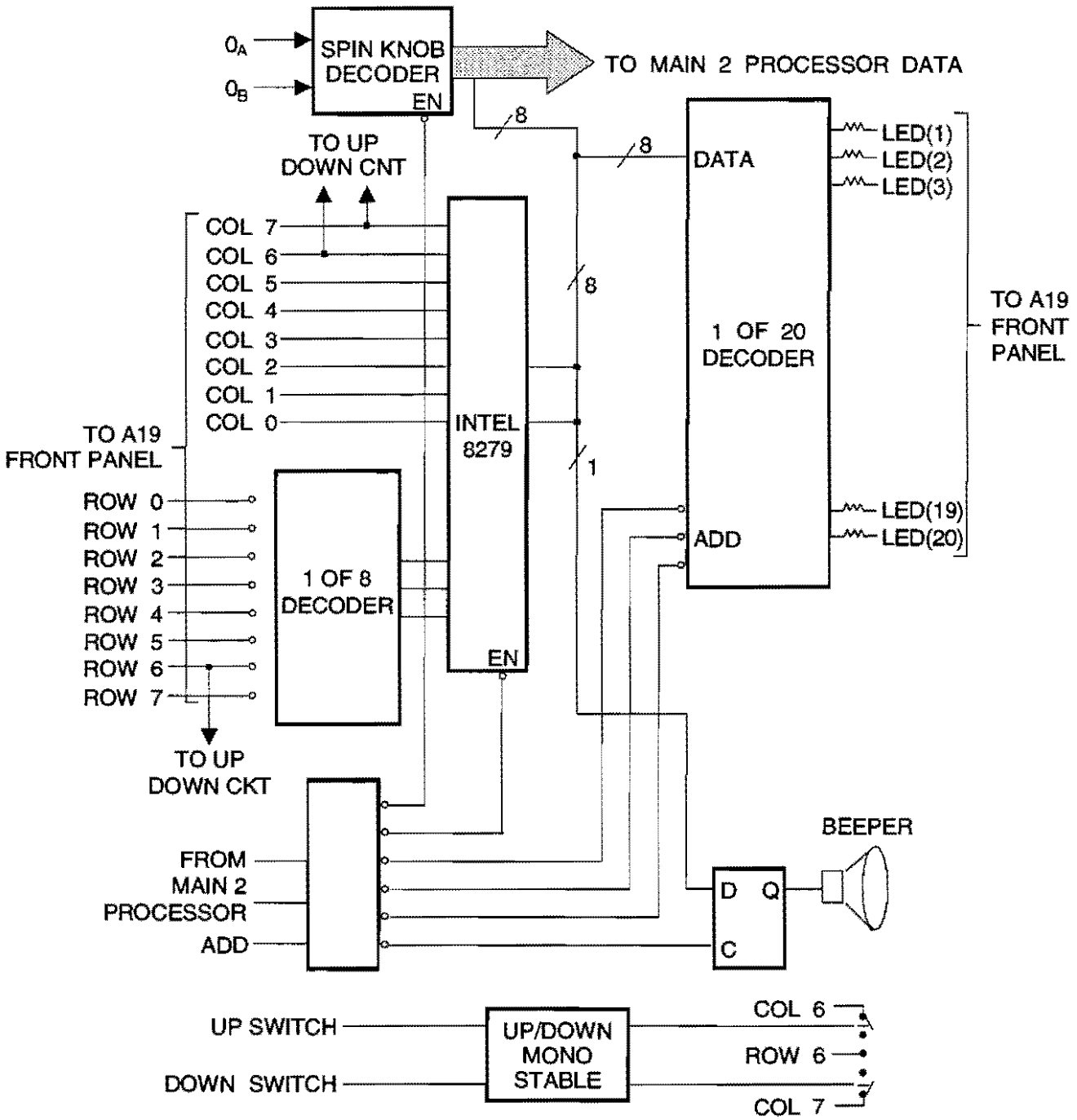


Figure 5-21. *A20 Front Panel Control PCB Block Diagram*

5-24 REMOVE AND REPLACE COVERS

This paragraph provides instructions for removing top, bottom, and side covers. To replace covers, reverse the removal process.

Procedure

Top and Bottom Covers

Step 1. On rear panel, loosen screws and remove the feet from the four corners.

Step 2. Slide the top and bottom covers toward the rear and remove.

Side Covers

Step 1. Remove top and bottom covers.

Step 2. Grasp rack-slide handle at front, and slide side panels to the rear and remove.

5-25 REMOVE AND REPLACE PRINTED CIRCUIT BOARDS

This paragraph provides instructions for removing and replacing printed circuit boards (PCBs). To replace PCBs, reverse the removal process. Refer to Figure 5-1, on page 5-6, for PCB locations.

Preliminary Remove top cover (paragraph 5-24).

Procedure

A1 thru A10 PCBs

Step 1. Remove RF cables by pulling straight-away.

Step 2. Loosen the top-mounted, phillips-head retaining screws.

Step 3. Grasp handle and pull PCB up and out of card cage.

CAUTION

All of the PCBs contain static-sensitive components. Refer to Figure 1-2, page 1-10, for precautionary instructions. Failure to follow these instructions may result in damage to the PCB.

A11 thru A13, and A21 PCBs

Step 1. Slide retaining clasp on each of eight cover latces toward center and remove cover.

Step 2. Lift up on edge tabs and remove PCB from motherboard connector.

A14 PCB

Step 1. Unsnap retaining clip on A14P2 housing and disconnect ribbon cable connector.

Step 2. Lift up on edge tabs and remove PCB from motherboard connector.

A15 PCB

Step 1. Remove 10 screws, lock washers, and flat-washer, and remove cover.

Step 2. Lift up on edge tabs and remove PCB from motherboard connector.

A16 PCB

Lift up on edge tabs and remove PCB from mother-board connector.

5-26 REMOVE AND REPLACE FRONT PANEL AND DISK DRIVE ASSEMBLY

This paragraph provides instructions for removing and replacing the front panel and disk drive assembly. To replace the assembly, reverse the removal process.

Preliminary Remove top, bottom, and side covers (paragraph 5-24).

Procedure

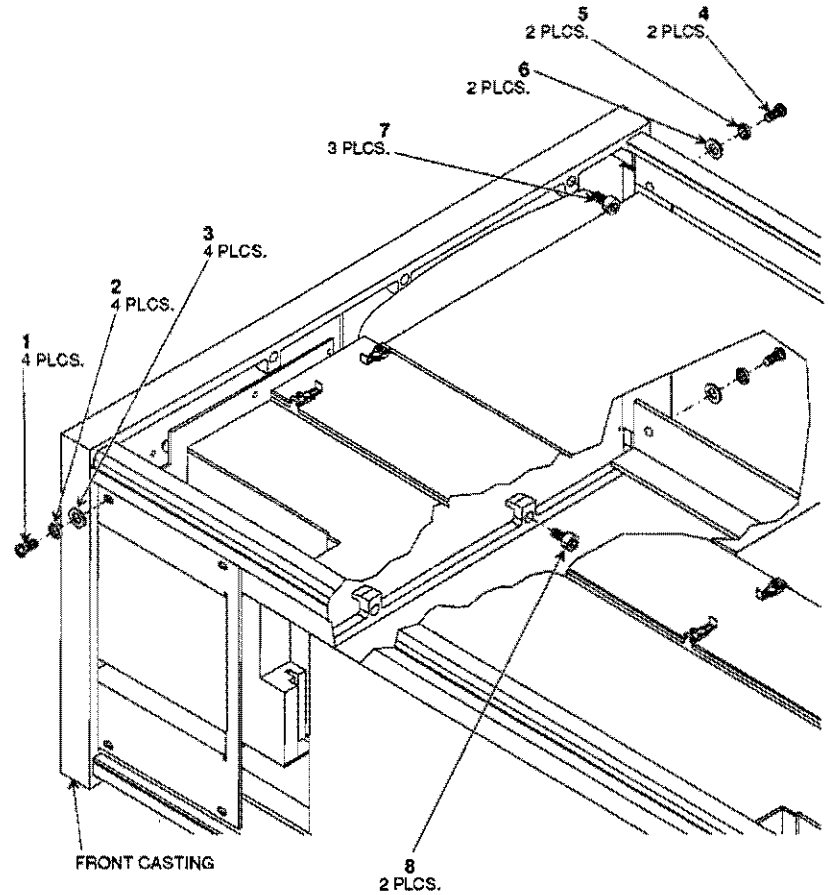
Step 1. Remove four screws (1), flat washers (2), and lockwashers (3) from right side.

Step 2. Remove two screws (4), flat washers (5), and lockwashers (6) from left side.

Step 3. Remove three screws (7) from the inside of top casting (not shown).

Step 4. Remove two screws (8) from the inside of the bottom casting.

Step 5. Slide the front panel out from the front.



5-27 REMOVE AND REPLACE COLOR DISPLAY VGA ASSEMBLY

This paragraph provides instructions for removing and replacing the color display VGA assembly. To replace the assembly, reverse the removal process.

Preliminary Remove top, bottom, and side covers (paragraph 5-24).

Procedure

Step 1. Remove the following connectors from the color display housing and PCB mounted on its rear.

- ☐ 3 ea ribbon cable connectors from PCB.
- ☐ 1 ea 4-pin molex connector from right side of housing.
- ☐ 1 ea 2-pin molex connector from left side of housing.
- ☐ 1 ea line-power plug from housing.

NOTE
Loosing the thrumbscrews and pulling the PCB away from the housing will facilitate removing the cables.

Step 2. Remove four bolts from the underside of the chassis.

Step 3. Lift the color display housing out through the top of the analyzer.

NOTE
You do not have to remove the front panel.

Chapter 6
36XXA Test Sets, General Information

Table of Contents

Chapter 6
36XXA Test Sets, General Information

6-1 INTRODUCTION

This chapter provides general information for the test sets. It also includes remove and replace procedure for test set assemblies.

6-2 REPLACEABLE SUBASSEMBLIES

WILTRON maintains a module exchange program for selected signal source modules. If a malfunction occurs in one of these modules, it can be exchanged. Upon request and typically within 24 hours, WILTRON or an Anritsu/Wiltron Service Center will ship an exchange module. The customer has 30 days in which to return the defective item. All exchange parts are warranted for 90 days from the date of shipment or for the balance of the original-part warranty—whichever is longer.

A listing of exchangeable subassemblies is provided in Chapter 1, Table 1-2.

6-3 OVERALL CIRCUIT DESCRIPTION

An overall functional description of the test set is given below. This description is organized into a general description of the test set and operation of the test set within the system.

General

The test set contains the measurement components for the 360B VNA system. The test set, under direct control of the VNA, performs the following:

- Stimulus signal routing from the signal source to a device-under-test (DUT) through one of the test ports (Port 1 or Port 2).
- Signal separation and down conversion of the incident, reflected, and transmitted signals at Ports 1 and 2 into four IF signals (Test A, Reference A, Test B, and Reference B).
- Amplification of the IF signals.

There are test sets available that allow vector measurements for different applications. The test set types include active and passive device test sets with automatic signal reversing, frequency conversion test sets, and a millimeter-wave test set. Most test set types include multiple models covering differing frequency ranges from 10 MHz to 60 GHz. The millimeter-wave test set provides frequency coverage from 33 to 110 GHz in four waveguide bands (Q, U, V, and W).

System Operation

During a typical measurement, the microwave signal source, under direct control of the VNA, outputs an RF signal to the test set to provide stimulus to the DUT. The system signal source is phase-locked with the VNA's internal 10 MHz crystal oscillator. An external 10 MHz frequency standard may be substituted for the system's internal 10 MHz oscillator for maximum attainable frequency accuracy.

In the test set, the stimulus signal is sent to the DUT through one of the test set test ports (Port 1 or Port 2). When there is any impedance mismatch between the test port and the DUT input port, some of the signal incident at the DUT input port is reflected back to the test set and some travels into the DUT. In the case of two port DUTs — those having an input and output port — the portion of the stimulus signal that travels through the DUT goes to the second test port for measurement.

In addition to stimulus-signal routing from the signal source to the DUT, the test set also serves as the front end of the VNA receiver.

Within the test set there are signal separation and down conversion devices that separate and down convert the incident, reflected, and transmitted signals at Port 1 and Port 2 into four distinct intermediate frequency (IF) signals. The incident signals are fed to Reference Channels A and B and the reflected or transmitted signals are fed to Test Channels A and B.

Heterodyne frequency conversion is used to improve upon the inherent limitations in broadband diode detectors. It also provides significant improvement in dynamic range, harmonic rejection, and sensitivity.

Each of the four IF signals carries embedded magnitude and phase information relative to a reference signal. Down conversion does not affect the magnitude and phase relationship, only the frequency is changed. The IF signals go to selection switches in the test set. These switches determine the following:

- Which signals are sent to the test set IF amplifiers and then on to the synchronous detectors of the VNA.
- Which reference signal will be used for phase-locking the system signal source.

The VNA source lock circuitry compares the selected reference signal frequency and phase to that of a signal derived from the 10 MHz crystal oscillator in the VNA. If the system is not properly phase-locked, a correction voltage is generated that drives the FM Ø LOCK input to the system signal source. This signal forces the source to lock to the correct frequency and phase.

Additional signal processing is implemented within the VNA. The magnitude and phase information embedded on the analog IF signals is first detected; then it is converted to digital data.

The VNA processors — controlled by firmware coupled with downloadable software — manipulate this digital data according to theoretical modelling

techniques. Short-term system errors are normalized and digital compensation is generated and applied. The resultant S-parameter data that characterizes the DUT is then

- presented on the VNA color display,
- output to a printer or plotter, or
- routed to the rear panel (external) GPIB interface.

6-4 TEST SET SIGNAL DESCRIPTIONS

All test sets use the same signal designations. The following is a description of the test set signals, their derivation, and their relationships. To aid understanding, use the overall block diagram for your model of test set — Figures 7-3 or 7-4 (in Chapter 7), Figure 8-1 (in Chapter 8), or Figure 9-2 (in Chapter 9) — while reading the following discussion.

The test sets have two front panel ports that are used for connection to the DUT. They are designated Port 1 and Port 2. When the DUT stimulus signal originates at Port 1, an LED next to that port lights. This indicates a measurement in the *forward* direction. When the DUT stimulus signal originates at Port 2, an LED next to that port lights. Conversely, this indicates a measurement in the *reverse* direction.

The VNA controlled switching of the stimulus signal between Ports 1 and 2 eliminates the need to physically reverse the DUT during the measurement process. This VNA system feature is referred to as *fully-reversing.*

Within the test sets, signal separation and down conversion of the incident, reflected, and transmitted signals at Ports 1 and 2 results in four IF signals. They are defined as:

- R_A (Reference, Channel A) – this signal contains information about the stimulus signal in the forward direction (incident signal) from Port 1 to the DUT.
- T_A (Test, Channel A) – in the forward measurement mode, this signal contains information about the reflected signal from the DUT back to Port 1. In the reverse measurement mode, this signal contains information about the transmitted signal from the DUT to PORT 1.
- R_B (Reference, Channel B) – this signal contains information about the stimulus signal in the reverse direction (incident signal) from Port 2 to the DUT.
- T_B (Test, Channel B) – in the forward measurement mode, this signal contains information about the transmitted signal from the DUT to Port 2. In the reverse measurement mode, this signal contains information about the reflected signal from the DUT back to Port 2.

The four IF signals maintain these channel definitions as they are down-converted to the second IF while passing through the A8T and A10T Buffer Amplifiers. Before processing by the A1T, A2T, and A3T IF Amplifiers, the desired relationship of Channels A, B, and R is established by the selection switches in the A24T Source Lock/Reference Select assembly, as is the choice of source lock signal.

The VNA's display menus are designed for use with all VNA test set models. Therefore, to accommodate those test sets that do not contain front-end signal separation devices, signal paths are designated by the names used in the definitions of multi-port devices. The VNA menus for test ports are:

- a_1 – normally equivalent to R_A (depending on the configuration selected via menu control)
- a_2 – normally equivalent to R_B (depending on the configuration selected via menu control)
- b_1 – normally equivalent to T_A (depending on the configuration selected via menu control)
- b_2 – equivalent to T_B.

The VNA system mathematically compares the relative magnitude and phase changes between the reference and test channels to derive the S-parameters used to characterize a DUT. Table 6-1 shows the relationship between the multi-port device definitions and the VNA system measurement channels in deriving the S-parameters. (Do not confuse the four measurement channels with the four display channels, CH1 thru CH4, selected by the push buttons at the right of the VNA display.)

Table 6-1. *S-parameter Definitions*

S Parameter	Multi-Port Device Definition Ratio	VNA Measurement Channel Ratio	Measurement Definition
S_{11}	$\frac{b1}{a1}$	$\frac{T_A}{T_B}$	Forward Reflection
S_{12}	$\frac{b1}{a2}$	$\frac{T_A}{R_B}$	Reverse Transmission
S_{21}	$\frac{b2}{a1}$	$\frac{T_B}{R_A}$	Forward Transmission
S_{22}	$\frac{b2}{a2}$	$\frac{T_B}{R_B}$	Reverse Reflection

6-5 REMOVE AND REPLACE PROCEDURES

Procedures for removing and replacing subassemblies listed in Table 1-2 are provide in subsequent paragraphs.

6-6 REMOVE AND REPLACE COVERS

This paragraph provides instructions for removing top, bottom, and side covers. To replace covers, reverse the removal process.

Procedure

Top and Bottom Covers

Step 1. On rear panel, loosen screws and remove the feet from the four corners.

Step 2. Slide the top and bottom covers toward the rear and remove.

Side Covers

Step 1. Remove top and bottom covers.

Step 2. Grasp rack-slide handle at front, and slide side panels to the rear and remove.

6-7 REMOVE AND REPLACE A1T THRU A5T PCBS

This paragraph describes how to remove the A1T thru A5T PCBs. The A1T thru A4T procedures are applicable for all models; the A5T procedure applies to all except 3635B. To replace PCBs, reverse the removal process.

NOTE

Refer to Figures 7-1, 7-2, 8-2, or 9-3 (as applicable) for component locations.

Preliminary Remove all four system covers (paragraph 6-6).

Procedure

Step 1. Loosen connector and remove attached coaxial cables.

Step 2. Remove 14 screws and lockwashers from outer edges of cover plate.

Step 3. Tug on cover plate handle to lift PCB straight up and out.

NOTE

After replacing cables, torque connectors to 8 inch-pounds.

CAUTION

All of the referenced PCBs contain static-sensitive components. Refer to Figure 1-2, page 1-10, for precautionary instructions. Failure to follow these instructions may result in damage to the PCB.

6-8 REMOVE AND REPLACE A5T PCB (3635B)

This paragraph describes how to remove the A5T Power Distribution PCB on Model 3635B. To replace PCB, reverse the removal process.

NOTE
Refer to Figure 9-3 for PCB location.

Preliminary Remove the top cover (paragraph 6-6).

Procedure

Step 1. Disconnect the three cable assemblies connected to J1, J2, and J3.

Step 2. Remove 6 screws and pull PCB straight up and out.

CAUTION

All of the referenced PCBs contain static-sensitive components. Refer to Figure 1-2, page 1-10, for precautionary instructions. Failure to follow these instructions may result in damage to the PCB.

NOTE

- These screws are accessible through the bottom of the instrument — through holes in the A23T Motherboard.
- After replacing cables, torque connectors to 8 inch-pounds.

6-9 REMOVE AND REPLACE A6T PCB

This paragraph describes how to remove the A6T Power Distribution PCB. To replace PCB, reverse the removal process.

CAUTION

The referenced PCB contains static-sensitive components. Refer to Figure 1-2, page 1-10, for precautionary instructions. Failure to follow these instructions may result in damage to the PCB.

NOTE

Refer to Figures 7-1, 7-2, 8-2, or 9-3 (as applicable) for component locations.

Preliminary Remove the top cover (paragraph 6-6).

Procedure

Step 1. Loosen thumbscrew, located in the middle-top of the PCB, by turning it counterclockwise.

Step 2. Lift up on the the two edge tabs and pull PCB straight up and out.

6-10 REMOVE AND REPLACE A7T OR A27T PCB

This paragraph describes how to remove the A7T Attenuator Driver PCB or A27T Amplifier Switch/Driver PCB on Model 362XA test sets. To replace PCB, reverse the removal process.

NOTE

Refer to Figures 7-1 or 7-2 (as applicable) for component locations.

Preliminary Remove the top cover (paragraph 6-6).

Procedure

Step 1. Loosen thumbscrew, located in the middle-top of the PCB, by turning it counterclockwise.

Step 2. Lift up on the the two edge tabs and pull PCB straight up and out.

6-11 REMOVE AND REPLACE COMPENSATION CABLE ASSEMBLIES

This paragraph describes how to remove the compensation cable assemby on the Model 3610A. To replace this assembly, reverse the removal process.

NOTE
Refer to Figure 7-1 for assembly location.

Preliminary Remove the top cover (paragraph 6-6).

Procedure

Step 1. Loosen four connectors, as described below:

- ☐ A14J2, connected to J2 on coupler.
- ☐ A11J2, connected to J2 on Sampler A.
- ☐ A17J1, connected to rear panel.
- ☐ A13J4, connected to transfer switch.

Step 2. Remove two screws, lockwashers, and flat washers and standoffs on either side of cable assemblies.

Step 3. Lift the two semi-rigid cables up and out.

NOTE
After replacing cables, torque connectors to 8 inch-pounds.

6-12 REMOVE AND REPLACE A20T THRU A22T ATTENUATORS AND A18T/A19T BIAS TEES

This paragraph describes how to remove the A20, A21, and A22 Attenutor assemblies and A18T and A19T Bias Tees on Model 362XA. To replace the attenuator(s), reverse the removal process.

NOTE

Refer to Figures 7-1 or 7-2 (as applicable) for component locations.

Preliminary Remove the top cover (paragraph 6-6).

Procedure

Step 1. Loosen connectors and remove cables between attenuator input (or bias tee input) and coupler/connector output.

Step 2. Loosen connector and push cable back from attenuator output connector.

Step 3. Remove appropriate ribbon cable connector from A7J1, A7J2, or A7J3.

Step 4. Loosen connector and remove cables from top of bias tee, if applicable.

Step 5. Remove two screws, lockwashers, and flat washers from bottom of bracket.

Step 6. Lift attenuator and bracket straight up and out.

Step 7. If applicable, remove bias tee by loosening connector, then removing screw, lockwasher, and flatwasher.

Step 8. Remove remaining screw(s) and separate attenuator from bracket.

NOTE

After replacing cables, torque connectors to 8 inch-pounds.

6-13 REMOVE AND REPLACE A30T AND A31T TRIPLERS

This paragraph describes how to remove the A30T and A31T Tripler assembly on the Models 3612A, 3613A, 3615A, 3622A, 3623A, 3625A, and 3631A Test Sets. To replace the tripler(s), reverse the removal process.

NOTE

Refer to Figures 7-1, 7-2, or 8-2 (as applicable) for component locations.

Preliminary Remove the top cover (paragraph 6-6).

Procedure

Step 1. Loosen connectors and remove three cables from connectors stated below:

- ☐ J1 and J2 on Mux Coupler
- ☐ RF IN on Amplifier.

Step 2. Remove black and white twisted-pair connector from motherboard.

NOTE

Remove black and white twisted-pair from cable clamps and ties as applicable.

Step 3. Remove two screws, lockwashers, and flat washers from bottom of bracket.

Step 4. Lift tripler assembly and bracket straight up and out.

NOTE

After replacing cables, torque connectors to 8 inch-pounds.

6-14 REMOVE AND REPLACE A13T (A9T) TRANSFER SWITCH

This paragraph describes how to remove the A13T (A9T on 3635B) Transfer Switch—or, for models 3612A, 3613A, 3615A, 3622A, 3623A, and 3625A; the A13T Transfer Switch, and A28/A29 Splitter Switch assemblies. To replace the assemblies, reverse the removal process.

NOTE

Refer to Figures 7-1, 7-2, or 9-3 (as applicable) for component locations.

Preliminary Remove the top cover (paragraph 6-6).

Procedure

Step 1. Loosen connectors and remove cable from transfer switch (or transfer-SPDT switches on 3622A).

Step 2. Remove applicable twisted-wiring harness connector(s) from motherboard connector(s).

Step 3. Remove two screws and lockwashers from bracket, and remove transfer switch assembly.

NOTE

After replacing cables, torque connectors to 8 inch-pounds.

6-15 REMOVE AND REPLACE A25T RF SPLITTER

This paragraph describes how to remove the A25T RF Splitter assembly on Models 361X/362X. To replace the splitter, reverse the removal process.

NOTE

Refer to Figures 7-1 or 7-2 (as applicable) for component locations.

Preliminary Remove the top cover (paragraph 6-6).

Procedure

Step 1. Loosen connectors at both ends of cables W11 thru W14.

Step 2. Remove two screws and lockwashers and lift cable-tie-bracket assembly up and out.

Step 3. Remove eight screws from Sampler A/ Sampler B cover plate and lift plate up and out.

Step 4. Loosen connector and remove RF splitter.

NOTE

After replacing cables, torque connectors to 8 inch-pounds.

6-16 REMOVE AND REPLACE A8T AND/OR A10T BUFFER AMPLIFIERS

This paragraph describes how to remove the A8T and A10T Buffer Amplifier Assemblies. To replace the buffer amplifiers, reverse the removal process.

NOTE

Refer to Figures 7-1, 7-2, 8-2, or 9-3 (as applicable) for component locations.

Preliminary Prepare for removing the buffer amplifiers as described below.

Step 1. Remove the top cover (paragraph 6-5).

Step 2. Remove the compensation cable assemblies, if applicable for your model (paragraph 6-11).

Step 3. Remove the attenuator assemblies if applicable for your model (paragraph 6-12).

Step 4. Remove the tripler assemblies if applicable for your model (paragraph 6-13).

Step 5. Remove the transfer switch or transfer switch/splitter, if applicable for your model (paragraph 6-14).

Step 6. Remove the RF splitter, if applicable for your model (paragraph 6-15).

Procedure Remove the A8T and A10T assemblies as described below.

Step 1. Remove all coaxial cable connectors.

Step 2. Remove two shielded-harness connectors from motherboard connectors.

Step 3. Remove three screws from the top of the A8T or A10T assembly.

Step 4. Slide the assembly out from under the support brackets, being careful not to damage the power supply feedthroughs.

NOTE

After replacing cables, torque connectors to 8 inch-pounds.

6-17 REMOVE AND REPLACE A12T POWER AMPLIFIER

This paragraph describes how to remove the A12T Power Amplifier assembly. To replace the power amplifer, reverse the removal process.

NOTE

Refer to Figures 7-1, 7-2, 8-2, or 9-3 (as applicable) for component locations.

Preliminary Remove the top cover (paragraph 6-6).

Procedure

Step 1. Remove coaxial connectors from input and output connectors.

Step 2. Remove shielded-pair wiring harness from motherboard connector.

Step 3. Remove two hex-head screws, lockwashers, and flat washers from bracket.

Step 4. Slide power amplifer to rear and lift up and out.

NOTE

After replacing cables, torque connectors to 8 inch-pounds.

6-18 REMOVE AND REPLACE A13T AND A17T INTERFACE ASSEMBLIES

This paragraph describes how to remove the A13T and A17T Front Panel Port Interface Assemblies on Model 3635B. To replace these assemblies, reverse the removal process.

NOTE
Refer to Figure 9-3 for component locations.

Preliminary Remove the top cover (paragraph 6-6).

Procedure

Step 1. Remove the appropriate cable harness plug from the A5T Power Distribution PCB at connector A5J1 (for the A13T) or connector A5J2 (for the A17T).

Step 2. Remove the two semi-rigid coaxial cables at the rear of the A13T or A17T assembly.

Step 3. Remove the two flexible coaxial cables at the rear of the A13T or A17T assembly.

Step 4. Remove four screws and pull assemblies away from panel.

NOTE
After replacing cables, torque connectors to 8 inch-pounds.

6-19 REMOVE AND REPLACE A16T POWER DIVIDER

This paragraph describes how to remove the A16T Power Divider. To replace power divider, reverse the removal process.

NOTE

Refer to Figures 7-1, 7-2, 8-2, or 9-3 (as applicable) for component locations.

Preliminary Remove the top cover (paragraph 6-6).

Procedure

Step 1. Remove four coaxial cables from assembly top.

Step 2. Remove the four screws and lockwasher and lift power divider up and out.

NOTE

After replacing cables, torque connectors to 8 inch-pounds.

6-20 REMOVE AND REPLACE A24T SOURCE LOCK ASSEMBLY

This paragraph describes how to remove the A24T Source Lock/LRL Assembly. To replace this assembly, reverse the removal process.

NOTE

Refer to Figures 7-1, 7-2, 8-2, or 9-3 (as applicable) for component locations.

Preliminary Remove the top cover (paragraph 6-6).

Procedure

Step 1. Remove the two shielded-cable harness connectors from mating connectors on motherboard.

Step 2. Remove six coaxial cables connected to the A24T assembly.

Step 3. Remove cable assemblies W18, W20, W22, and W40, to obtain unobstructed access.

Step 4. Remove six screws and lockwashers and lift assembly up and out.

NOTE

After replacing cables, torque connectors to 8 inch-pounds.

6-21 REMOVE AND REPLACE A14T/A15T COUPLER CONNECTORS

This paragraph describes how to remove the A14T and A15T Coupler/Connector Assemblies on Models 361X and 362X. To replace these assemblies, reverse the removal process.

NOTE

Refer to Figures 7-1 or 7-2 (as applicable) for component locations.

Preliminary Remove top cover (paragraph 6-6).

Procedure **Models 3610 and 3620**

Step 1. Remove compensation cable assembly (3610) (paragraph 6-11).

Step 2. Remove the remaining cable from A14T, the two cables that attach to A15T, and the cable that attaches to the RF IN connector.

Step 3. Remove large nuts from front side of connectors.

Step 4. Remove three hex-head screws and lockwashers from rear side of connectors.

Step 5. Remove the two screws, lockwashers, and flat washers that secure the couplers to the brackets.

Step 6. Remove the two screws, lockwashers, flat washers, and rubber grommets from the bottom of the brackets; remove the brackets.

Step 7. Slide the couplers back and lift up and away.

Models 3611, 3621, 3612, and 3622

Step 1. Remove the two cables that attach to each coupler.

Step 2. Remove large nuts from frontside of connectors.

Step 3. Remove three hex-head screws and lockwashers from rearside of connectors.

Step 4. Remove two screws, lockwashers, and flat washers that secures coupler to bracket.

Step 5. Rotate couplers to clear brackets and remove.

6-22 REMOVE AND REPLACE A20T RF INPUT AMPLIFIER (MODEL 3635B)

This paragraph describes how to remove the A20T RF Input Amplifier on Model 3635B Test Set. To replace this assembly, reverse the removal process.

NOTE

Refer to Figure 6-1 for component locations.

Preliminary Remove top and side covers (paragraph 6-6).

Procedure

Step 1. Remove two RF cables.

Step 2. Remove the connector from A5J3, and free the black/white twisted-wire pair for removal.

Step 3. Tag wires red and black wires and desolder from pins.

Step 4. From side, remove four screws from bracket and remove amplifier.

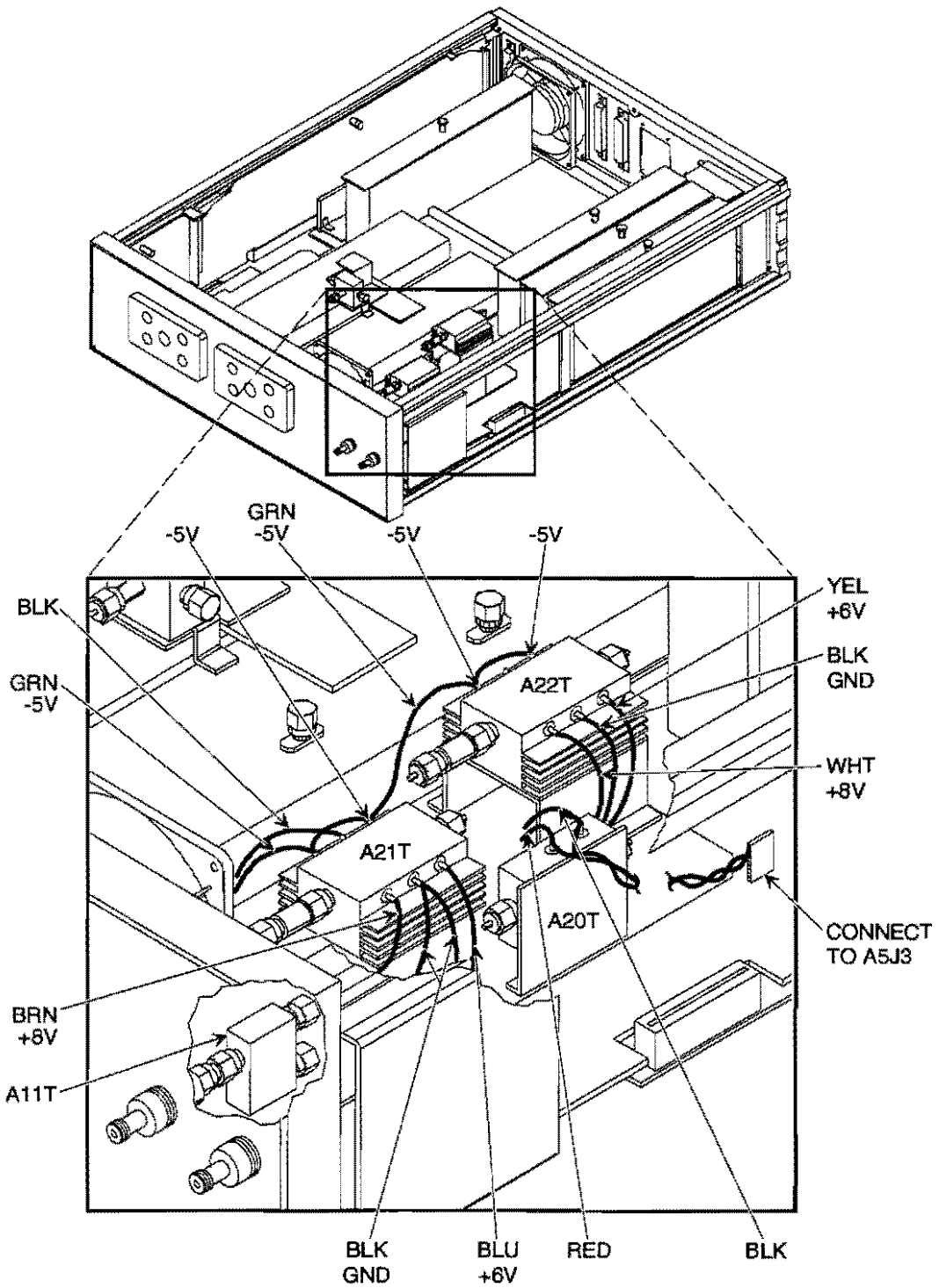


Figure 6-1. RF Component Locations, Model 3635B

6-23 REMOVE AND REPLACE A22T PORT 2 LO AMPLIFIER (MODEL 3635B)

This paragraph describes how to remove the A22T Port 2 LO Amplifier on Model 3635B Test Set. To replace this assembly, reverse the removal process.

NOTE
Refer to Figure 6-1 for component locations.

Preliminary Remove top cover (paragraph 6-6).

Procedure

Step 1. Remove two RF cables.

Step 2. Tag and desolder five wires.

Step 3. Remove four screws and remove amplifier.

6-24 REMOVE AND REPLACE A21T PORT 1 LO AMPLIFIER (MODEL 3635B)

This paragraph describes how to remove the A21T Port 1 LO Amplifier on Model 3635B Test Set. To replace this assembly, reverse the removal process.

NOTE
Refer to Figure 6-1 for component locations.

Preliminary Remove top cover (paragraph 6-6).

Procedure

Step 1. Remove two RF cables.

Step 2. Tag and desolder six wires.

Step 3. Remove four screws and remove amplifier.

6-25 REMOVE AND REPLACE A11T LO 1 POWER SPLITTER (MODEL 3635B)

This paragraph describes how to remove the A11T LO 1 Power Splitter on Model 3635B Test Set. To replace this assembly, reverse the removal process.

NOTE
Refer to Figure 6-1 for component locations.

Preliminary Remove top cover (paragraph 6-6).

Procedure

Step 1. Remove two RF cables.

Step 2. Remove connector from backside of LO1 INPUT connector.

Step 3. Remove splitter.

Chapter 7
361XA/362XA Test Sets Information

Table of Contents

Chapter 7
361XA/362XA Test Sets Information

7-1 INTRODUCTION

This chapter describes the series 361XA and 362XA Test Sets. It provides an overall functional description and descriptions of major PCB's, subassemblies, and RF deck assemblies for these units.

7-2 OVERALL FUNCTIONAL DESCRIPTION

Models 3610A through 3615A are Reversing Test Sets, and Models 3620A through 3625A are Active Device Test Sets (Table 7-1). All models contain the same *basic* circuitry and assemblies, and all provide automatic signal reversing. They differ only in that the Active Device Test Sets contain bias tees and additional step attenuators. The corresponding models of both series (3610A/ 3620A, 3613A/3623A, etc) cover the same frequency ranges.

Table 7-1. *Test Set Models, Frequency Ranges, and Test Port Connector Types*

Model	Type	Frequency Range (GHz)
K Male Connector		
3610A	Reversing	0.04 – 20
3611A	Reversing	0.04 – 40
3620A	Active Device	0.04 – 20
3621A	Active Device	0.04 – 40
V Male Connector		
3612A	Reversing	0.04 – 60
3613A	Reversing	0.04 – 65
3615A	Reversing	0.04 – 50
3622A	Active Device	0.04 – 60
3623A	Active Device	0.04 – 65
3625A	Active Device	0.04 – 50

The models in each series are similar in construction and operation, but differ in frequency range. Table 7-1 lists the test set models, their frequency ranges, and their test port connector types. The major assembly locations for models 3610A, 3611A, 3620A, and 3621A are shown in Figure 7-1 (next page). Figure 7-2 shows the major assembly locations for models 3612A, 3613A, 3622A, and 3623A.

Because of their similarities, the functional descriptions and block diagrams have been combined for the test sets. Information that is unique to a particular test set model or series of models is noted both in the descriptions and on the block diagrams.

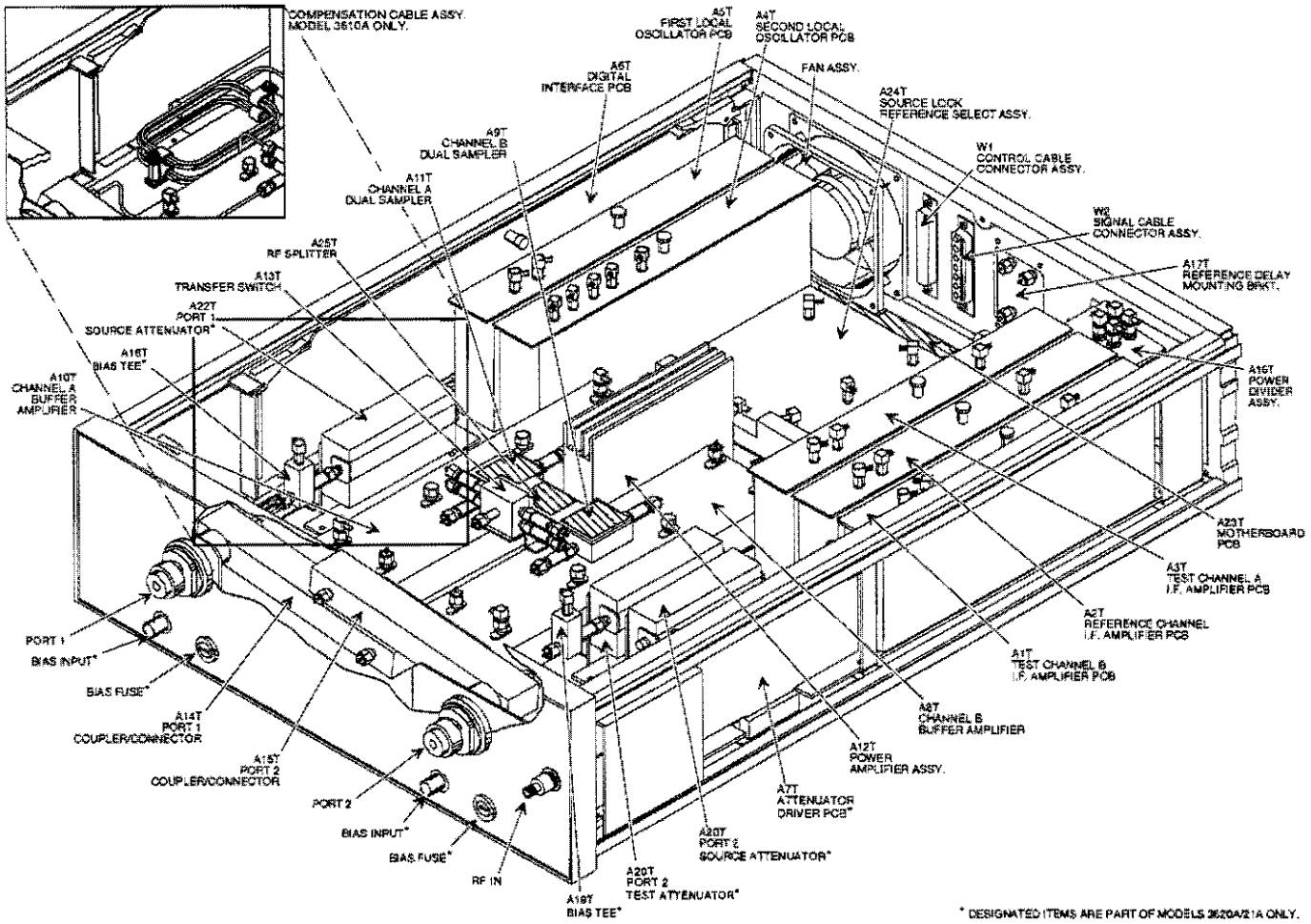


Figure 7-1. *Location Diagram for 3610A/3611A and 3620A/3621A Major Assemblies*

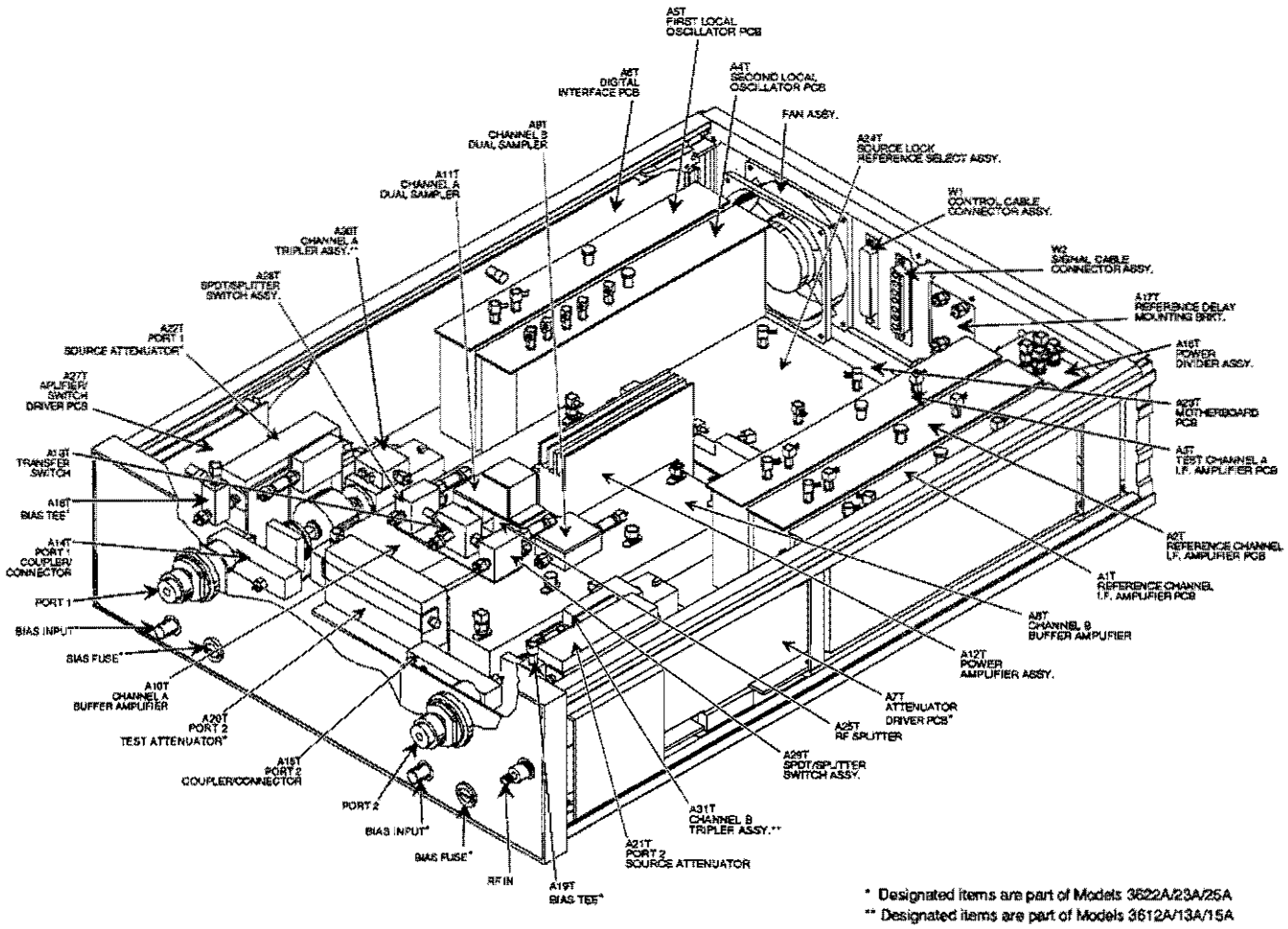


Figure 7-2. Location Diagram for 3612A/13A/15A and 3622A/23A/25A Major Assemblies

7-3 TEST PORT CONVERTERS

Test port converters provide a convenient means of user reconfiguration of the test set's connector type. Table 7-2 contains a listing of test port converters available for the Models 3610A/11A and Models 3620A/21A Test Sets. Table 7-3 provides a similar list for the Models 3612A, 3613A, 3615A, 3622A, 3623A and 3625A Test Sets.

NOTE

Use wrench (WILTRON part number 01-202) for changing the test port converters listed in Tables 7-2 and 7-3.

Table 7-2. *Test Port Converters for 3610A/3611A and 3620A/3621A*

WILTRON Part Number	Description
34UA50	Universal/GPC-7
34UK50	Universal/K Connector, Male
34UN50	Universal/N, Male
34UNF50	Universal/N, Female
34UQ50	Universal/2.4 mm, Male
34US50	Universal/APC 3.5

Table 7-3. *Test Port Converters for 3612A/13A/15A and 3622A/23A/25A*

WILTRON Part Number	Description
34YA50	Universal/GPC-7
34YK50	Universal/K Connector, Male
34YV50B	Universal/V Connector, Male
34SS50	Universal/SSMA, Male

7-4 FUNCTIONAL DESCRIPTION, 3610A/11A AND 3620A/21A TEST SETS

The 3610A/11A and 3620A/21A Test Sets (Figure 7-3, page 7-11) are similar in construction and operation, each model differs only in the bandwidth of the RF components. That is, the RF components that comprise the transfer switch assembly, coupler assemblies, buffer amplifier/sampler assemblies, step attenuators, and bias tees are selected to cover the frequency range of the particular test set model.

Signal Routing and Separation

The RF signal from the signal source is switched by the A13T transfer switch to PORT 1 of the test set via the A14T coupler or to PORT 2 via the A15T coupler. The switching of A13T is controlled by the VNA through the A6T Digital Interface PCB. Splitters within A13T split the RF signal with a portion going to PORT 1 or PORT 2 and a portion going to the reference channels (R_A or R_B).

In the forward measurement mode, A14T couples the signal reflected from the DUT to test channel A (T_A) and A15T couples the signal that passes through the DUT to test channel B (T_B). In the reverse measurement mode, A15T couples the signal reflected by the DUT to test channel B (T_B) and A14T couples the signal that passes through the DUT to test channel A (T_A). Simultaneously with the action described above for forward and reverse measurements, the signal source supplies a sample of its output to reference channels R_A and R_B.

The Models 3620A and 3621A Active Device Test Sets contain three step attenuators — A20T, A21T and A22T — and the bias tees (A18T and A19T) in the PORT 1 and PORT 2 stimulus signal lines and the step attenuator (A20T) in the forward transmission line. A21T and A22T are used to adjust the stimulus signal to the DUT, and A20T is used to control the DUT output power.

The step attenuators attenuate signals in 10 dB steps for a maximum attenuation of 70 dB (A20T is limited to a maximum attenuation of 40 dB). Attenuation is controlled by the VNA, via the A7T Attenuator Driver PCB. The A18T and A19T bias tees apply an appropriate dc bias voltage to those active DUTs that require it. Bias voltage can be applied to the test set via front or rear panel connectors.

First and Second IF Down Conversion

The test sets have two primary modes of operation: direct and heterodyne. The direct mode is for frequencies between 40 MHz and 270 MHz. The heterodyne mode is for frequencies from 270 MHz to 40 GHz.

In the direct mode, dual samplers A9T and A11T are like closed switches and send the test (T_A and T_B) and reference (R_A and R_B) signals to the buffer amplifiers A8T and A10T.

In the heterodyne mode, A9T and A11T switch either at the frequency of the first local oscillator (LO 1) or at harmonics of the first LO. The A5T LO 1 PCB—controlled by the VNA — outputs a 357 MHz to 536.5 MHz LO frequency.

The first LO output goes to the A12T power amplifier assembly, where it is amplified to drive the harmonic generator. This produces the harmonic pulses necessary for heterodyning in the samplers.

The A12T first LO output goes to A9T and A11T, via the A25T RF splitter assembly. The switching action of a sampler causes a mixing of the first LO frequencies and the input signal (T_A, T_B, R_A, or R_B). This heterodyning action provides the desired intermediate frequency (IF) of 89 ±4 MHz. The resultant first IF signals are input to buffer amplifiers A8T and A10T.

In the buffer amplifiers, the direct mode signal (40 MHz to 270 MHz) or first IF signal (89 MHz) is mixed with the second local oscillator (LO 2) signal. The A4T LO 2 PCB, which is controlled by the VNA, outputs an LO frequency in the range between 12.25 MHz and 272.25 MHz.

The heterodyning of the direct mode/first IF and second LO frequencies produces the desired second IF of 2.25 MHz. The buffer amplifier assemblies provide 0 dB conversion gain. The second IF test and reference signals (T_A, R_A, and R_B) from the A8T and A10T buffer amplifiers go to the A24T Source Lock/Reference Select assembly. The second IF test signal T_B — which is output by one half of the A8T buffer amplifier — goes directly to the A1T Channel B IF Amplifier.

Source Lock/ Reference Signal Selection

The A24T Source Lock/Reference Select assembly (also referred to as the LRL Module), contains switches for selecting the desired second IF signal source for the A2T Reference Channel IF Amplifier, the A3T Channel A IF Amplifier, and the VNA Source Lock circuitry.

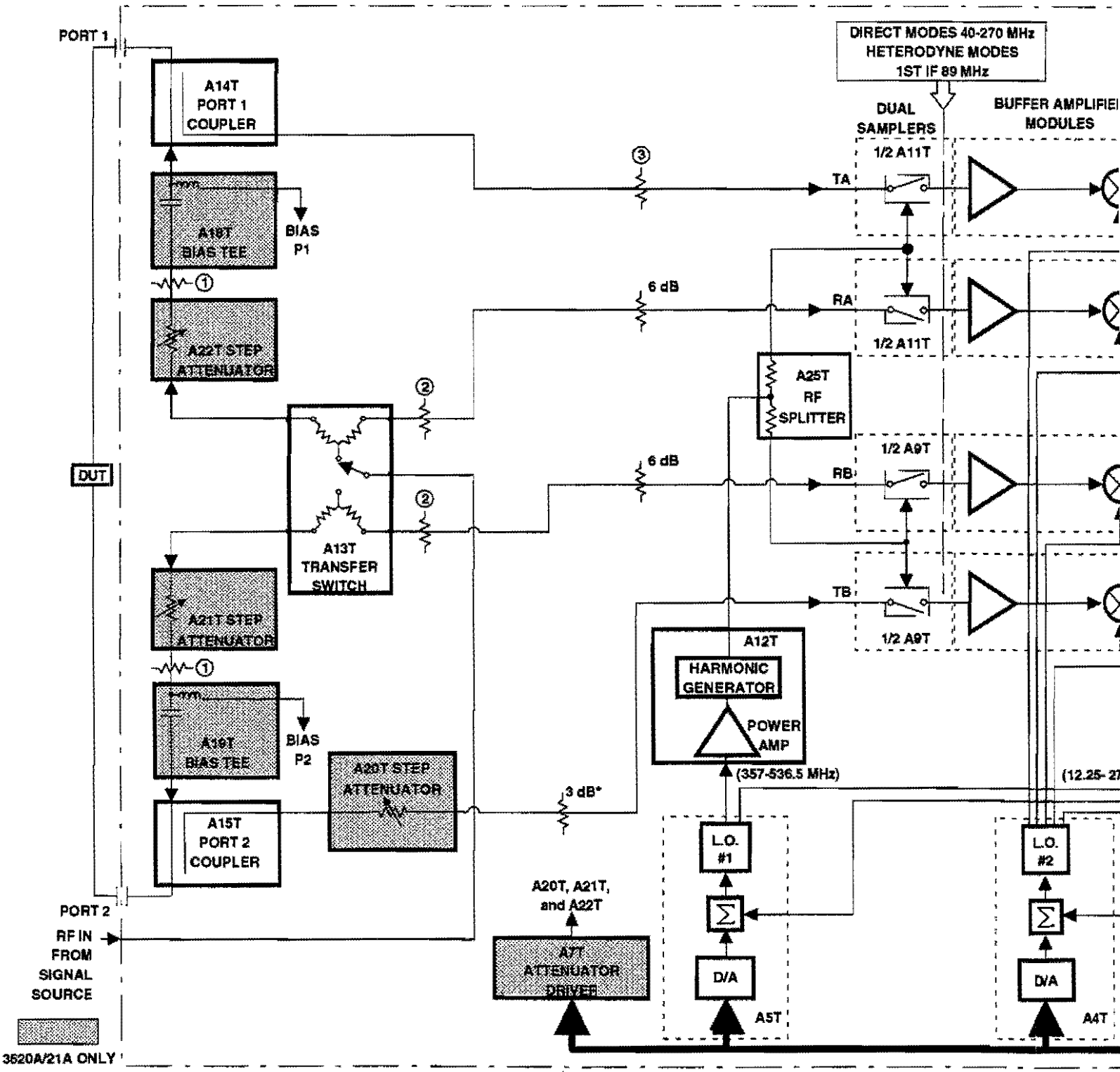
The A24T switches are controlled by the VNA through the A6T Digital Interface PCB. The second IF signal source for the A2T Reference Channel IF Amplifier is either R_A or R_B. The second IF signal source for the A3T Channel IF Amplifier is either T_A or R_A. The second IF signal source for the VNA source lock circuitry is R_A for forward measurements and R_B for reverse measurements.

Third IF Down Conversion and Amplification

The A1T, A2T, and A3T Channel IF Amplifiers have two modes of operation — measurement (LO) and calibration (CAL). In the measurement mode, the second IF signal is mixed with the third local oscillator (LO 3) signal of 2⅓ MHz received from the VNA via the A16T Three-Way Power Divider.

The heterodyning of the second IF and third LO frequency produces the desired third IF of 83⅓ kHz. The third IF signal is then amplified as required by five gain-ranging amplifiers before being output to the VNA synchronous detector circuits. The gain-ranging amplifiers are controlled by the VNA, through the A6T Digital Interface PCB.

The VNA automatically places the Channel IF Amplifiers in the calibration mode every three minutes. In this mode, an 83⅓ kHz signal is received from the VNA via the A16T Three-Way Power Divider. This 83⅓ kHz calibration signal goes directly to the gain-ranging amplifiers. These amplifier are then automatically calibrated to assure optimum accuracy and predictability of the Channel IF Amplifier outputs.


PORT 1
A14T
PORT 1
COUPLER
A18T
BIAS TEE
BIAS
P1
A22T STEP
ATTENUATOR
DUT
A13T
TRANSFER
SWITCH
A21T STEP
ATTENUATOR
A19T
BIAS TEE
BIAS
P2
A20T STEP
ATTENUATOR
A15T
PORT 2
COUPLER
PORT 2
RF IN
FROM
SIGNAL
SOURCE
3520A/21A ONLY
DIRECT MODES 40-270 MHz
HETERODYNE MODES
1ST IF 89 MHz
DUAL
SAMPLERS
BUFFER AMPLIFIE
MODULES
1/2 A11T
TA
RA
1/2 A11T
6 dB
6 dB
A25T
RF
SPLITTER
1/2 A9T
RB
TB
1/2 A9T
A12T
HARMONIC
GENERATOR
POWER
AMP
(357-536.5 MHz)
3 dB*
A20T, A21T,
and A22T
A7T
ATTENUATOR
DRIVER
L.O.
#1
D/A
A5T
L.O.
#2
D/A
A4T

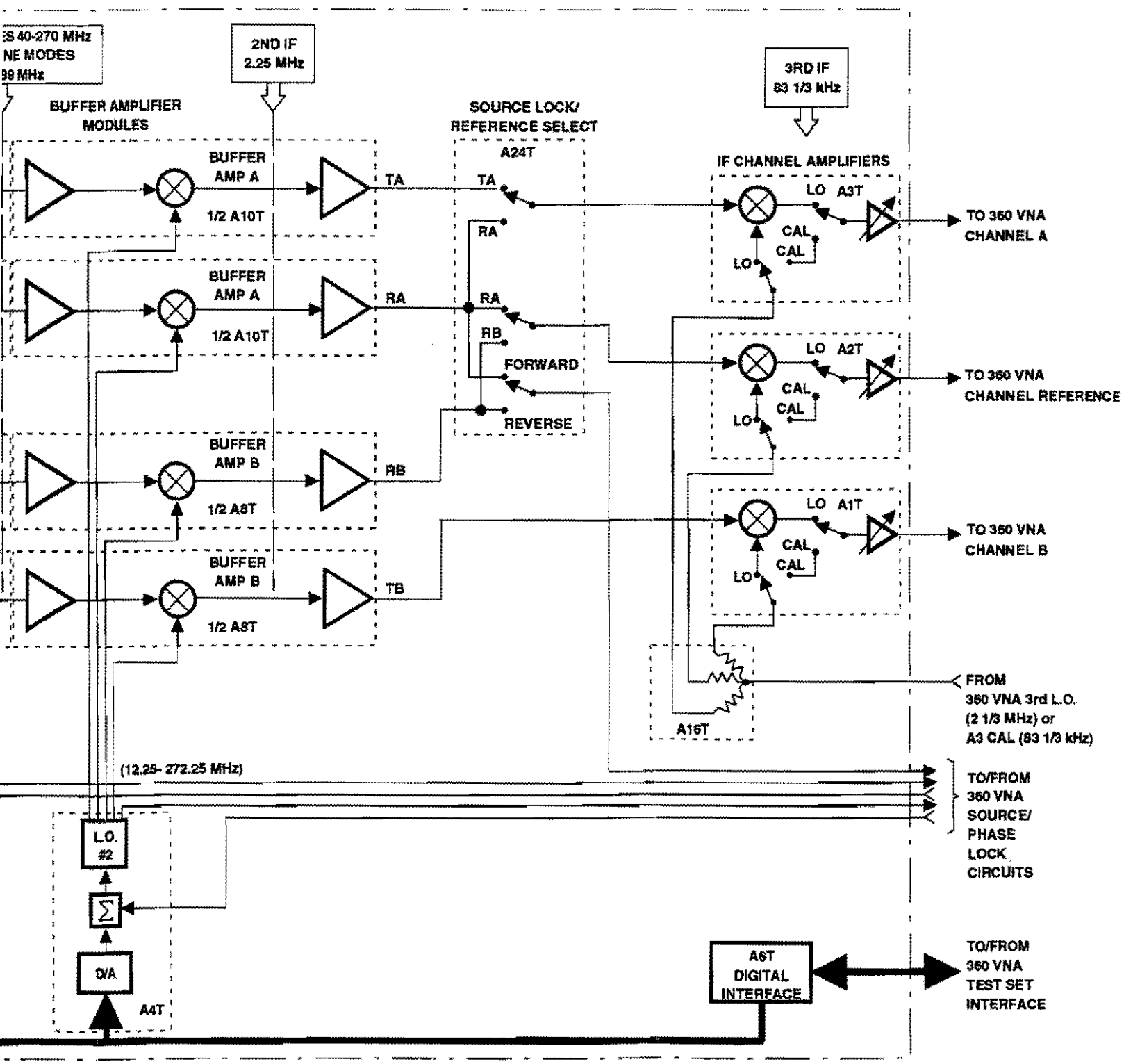
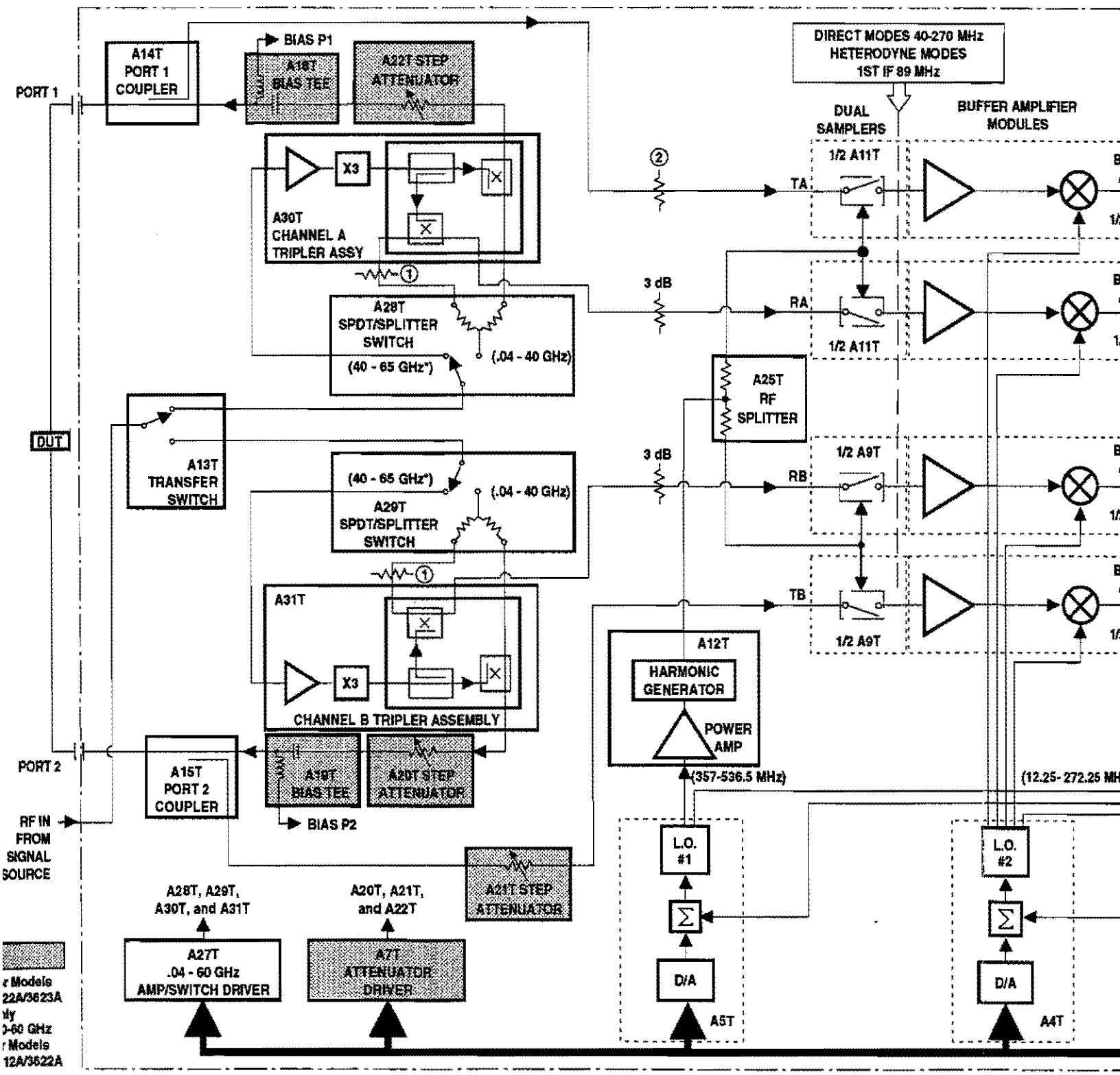


Figure 7-3. Models 3610A, 11A, 20A, 21A Block Diagram


PORT 1
A14T
PORT 1
COUPLER
BIAS P1
A18T
BIAS TEE
A22T STEP
ATTENUATOR
DIRECT MODES 40-270 MHz
HETERODYNE MODES
1ST IF 89 MHz
DUAL
SAMPLERS
BUFFER AMPLIFIER
MODULES
1/2 A11T
TA
X3
A30T
CHANNEL A
TRIPLER ASSY
3 dB
RA
A28T
SPDT/SPLITTER
SWITCH
(40 - 65 GHz*)
(.04 - 40 GHz)
1/2 A11T
A25T
RF
SPLITTER
DUT
A13T
TRANSFER
SWITCH
3 dB
1/2 A9T
RB
(40 - 65 GHz*)
(.04 - 40 GHz)
A29T
SPDT/SPLITTER
SWITCH
A31T
TB
1/2 A9T
A12T
HARMONIC
GENERATOR
X3
POWER
AMP
CHANNEL B TRIPLER ASSEMBLY
PORT 2
A15T
PORT 2
COUPLER
A19T
BIAS TEE
A20T STEP
ATTENUATOR
(357-536.5 MHz)
(12.25- 272.25 MH
BIAS P2
RF IN
FROM
SIGNAL
SOURCE
L.O.
#1
L.O.
#2
A21T STEP
ATTENUATOR
A28T, A29T,
A30T, and A31T
A20T, A21T,
and A22T
A27T
.04 - 60 GHz
AMP/SWITCH DRIVER
A7T
ATTENUATOR
DRIVER
D/A
D/A
A5T
A4T

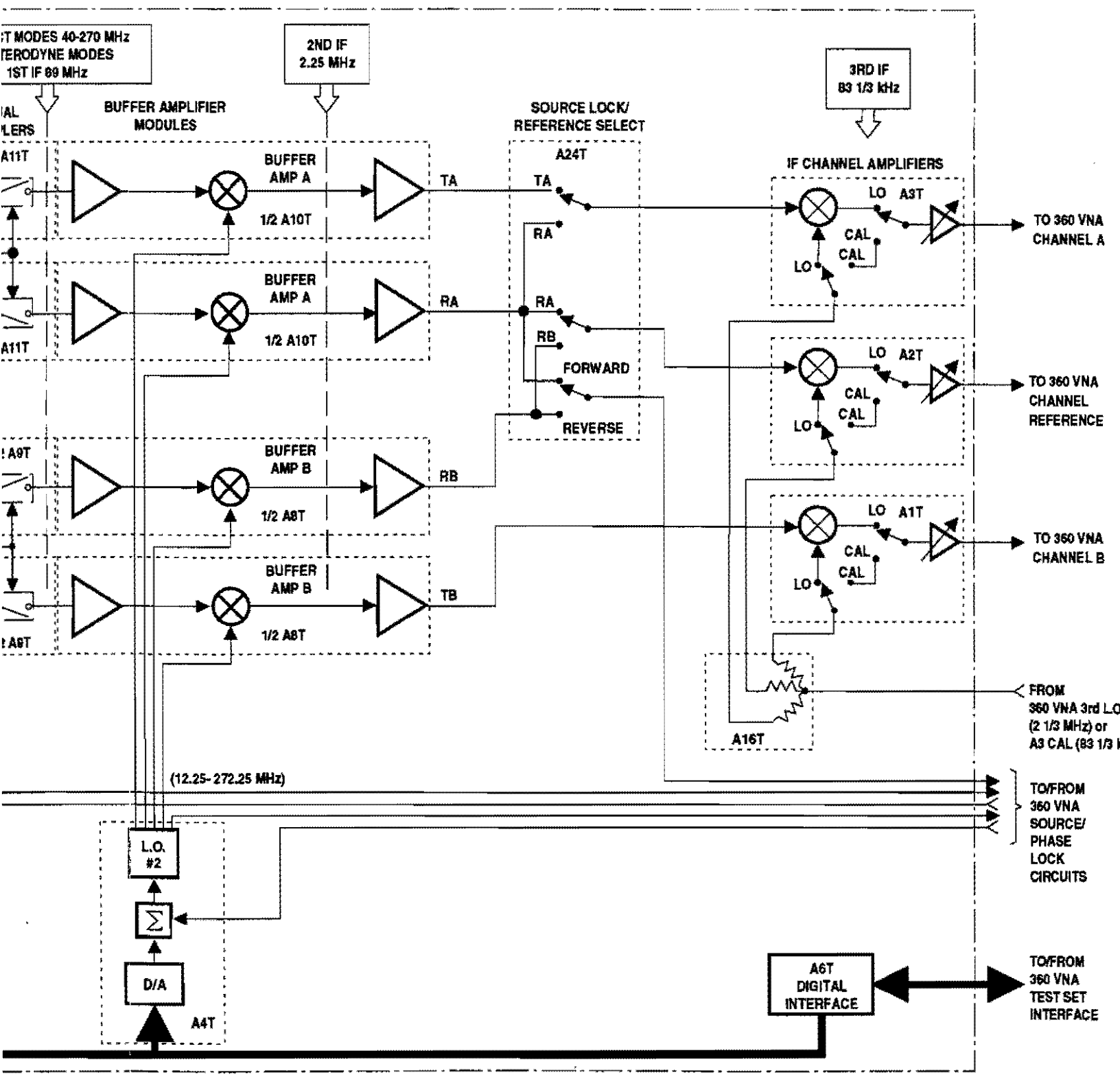


Figure 7-4. Models 3612A, 13A, 22A, 23A Block Diagram

7-5 FUNCTIONAL DESCRIPTION, 3612A/13A/15A AND 3622A/23A/25A TEST SETS

These test sets (Figure 7-4, facing page) contain the same basic circuitry and assemblies. Models 3612A and 3622A cover the same frequency (0.04 – 40 GHz), as do models 3615A and 3625A (0.04 – 50 GHz) and 3613A, 3623A (0.04 – 65 GHz, see Table 7-1). The active device test sets, 3622A/3623A/25A, differ from the 3612A/3613A/15A in that they contain bias tees and additional step attenuators.

Signal Routing and Separation

The RF signal from the 360SS69 Signal Source is switched by the A13T Transfer Switch to the A28T (Channel A) or A29T (Channel B) SPDT/Splitter Switch Assembly. The switching of A13T is controlled by the VNA through the A6T Digital Interface PCB. SPDT/Splitter Switch Assemblies A28T and A29T have two switch positions — 40 MHz to 40 GHz and 40 GHz to 60 GHz (40 GHz to 65 GHz for models 3613A and 3623A, 40 GHz to 50 GHz, for models 3615A and 3625A). The VNA controls the switching of A28T and A29T through the A27T Amplifier/ Switch Driver PCB.

In the forward measurement mode, A13T switches the signal source RF signal to A28T. If the VNA is operating in the 40 MHz to 40 GHz range, the A28T splitter feds a portion of the signal to the PORT 1 coupler, A14. It also feds a portion to the reference channel (R_A) through the multiplexer coupler that is part of the A30T Channel A Tripler Assembly.

If the VNA is operating above 40 GHz, A28T routes the signal source RF signal to the A30T Channel A Tripler Assembly*. The A30T assembly is powered-on by the VNA via the A27T Amplifier/Switch Driver PCB. The signal source RF signal is amplified and tripled to obtain the desired 40 GHz to 60 GHz (or 40 GHz to 50 or 65 GHz) signal. The resultant RF signal goes to the multiplexer coupler, which feds portion of it to the PORT 1 coupler (A14) and a portion to the reference channel (R_A).

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* The A30T/A31T Tripler Assemblies used in the 3612A/3622A and 3613A/3623A/3615A/3625A test sets are functionally alike, but differ in upper frequency range (60 GHz to 50 or 65 GHz). Refer to the description for the A30T/A31T Tripler Assemblies on page 7-38.

A14T couples the signal reflected from the DUT to test channel A (T_A) and A15T couples the signal that passes through the DUT to test channel B (T_B).

In the reverse measurement mode, A13T switches the signal source RF signal to A29T. If the VNA is operating between 40 MHz and 40 GHz, the A29T splitter feds a portion of the signal the PORT 2 coupler, A15. It also feds a portion to reference channel (R_B) through the multiplexer coupler that is part of the A31T Channel A Tripler Assembly.

If the VNA is above 40 GHz, A29T routes the signal source RF signal to the A31T Channel B Tripler Assembly. The A31T assembly is powered-on by the VNA via the A27T Amplifier/Switch Driver PCB. The signal source RF signal is amplified and tripled to obtain the desired 40 GHz to 60 GHz (or 40 GHz to 50 or 65 GHz) signal. The resultant RF signal goes to the multiplexer coupler, which feds portion of it to the PORT 2 coupler (A15) and a portion to the reference channel (R_B).

A15T couples the signal reflected from the DUT to test channel B (T_B), and A14T couples the signal that passes through the DUT to test channel A (T_A).

The 3622A and 3623A and 3625A Active Device Test Sets contain bias tee A18T and step attenuator A22T in the PORT 1 stimulus signal line. Similarly, bias tee A19T and step attenuator A20T are included in the PORT 2 stimulus signal line. These models also include a third step attenuator, A21T, in the forward receive path between coupler A15T and the input to test channel B (T_B).

First and second IF down conversion, source lock/reference signal selection, and third IF down conversion and amplification is functionally identical for all of the Models 361XA and 362XA Test Sets.

7-6 A1T, A2T, and A3T CHANNEL IF AMPLIFIER PCB CIRCUIT DESCRIPTION

The A1T, A2T, and A3T Channel IF Amplifier assemblies (Figure 7-5) are functionally equivalent. The A1T and A3T PCBs are mechanically identical; only the PCB cover plates are different. The A2T PCB has a different component layout and card-edge connector pin configuration. The following functional description applies to all three.

The Channel IF Amplifier PCBs have two modes of operation: measurement (LO) and calibration (CAL). In the measurement mode, the 2.25 MHz second IF signal input goes via a buffer amplifier to a 2.25 MHz bandpass filter that removes harmonics and other unnecessary signals. The output from the filter is split into two separate signal paths. The signals are then phase-shifted; one signal by +45° and the other by –45°. Each of the phase-shifted signals is mixed with a 2⅓ MHz third local oscillator signal received from the VNA.

One of the frequencies produced in each mixer is 83⅓ kHz — the difference of the two frequencies. The two phase-shifted, heterodyned signals are then filtered, phase shifted back to 0°, and summed in an amplifier to reject the image frequency. The output passes through an 83⅓ kHz bandpass filter that rejects all harmonics and subharmonics of the fundamental frequencies. The 83⅓ kHz third IF signal then goes to five gain-ranging amplifiers that have selectable gains of one or four.

The third IF signal output is maintained at an acceptable level through automatic gain control (AGC). The peak detector, at the output of the gain-ranging amplifiers, detects the peak signal level and sends a dc voltage representing this level to the comparator. The comparator determines if the dc voltage is in the necessary range of levels required by the VNA synchronous detectors. The comparator outputs one of three signals:

- L=> 0 dB — overload peak signal level condition
- L=> –12 dB — maximum peak signal level condition
- L=> –24 dB — minimum peak signal level condition.

These signals are sent via the A6T Digital Control PCB to the VNA. Responding to these signals, the VNA sends data through A6T to control the gain ranging amplifiers maintaining the peak signal level between 0 and –24 dB.

Third IF peak signal levels affect the amplifiers as follows:

- When the peak signal level is between 0 and –24 dB, all amplifiers are set to a gain of one.
- When the peak level drops below –24 dB, the first gain-ranging amplifier is set to a gain of four. The gain of the first amplifier remains at four until the signal reaches a peak level above –24 dB.
- If the peak signal drops to a level below –36 dB, the second gain-ranging amplifier is set to a gain of four.
- If the peak signal drops to a level below –48 dB, the third gain-ranging amplifier is set to a gain of four.
- If the peak signal drops to a level below –60 dB, the fourth gain-ranging amplifier is set to a gain of four.
- If the peak signal drops to a level below –72 dB, the fifth gain-ranging amplifier is set to a gain of four.

In this way the third IF signal is incrementally boosted each time the signal level at the peak detector drops 12 dB after the initial –24 dB threshold.

The VNA automatically places the A1T thru A3T Channel IF Amplifiers in the calibration mode every three minutes. In the calibration mode, an 83⅓ kHz signal is received from the VNA and sent directly to the gain-ranging amplifiers. The signal level is then incrementally increased by individually programming each of the gain-ranging amplifiers in succession. The outputs are then measured and compared to expected values. The VNA then trims each of the amplifiers using a software algorithm to achieve optimum accuracy and predictability.

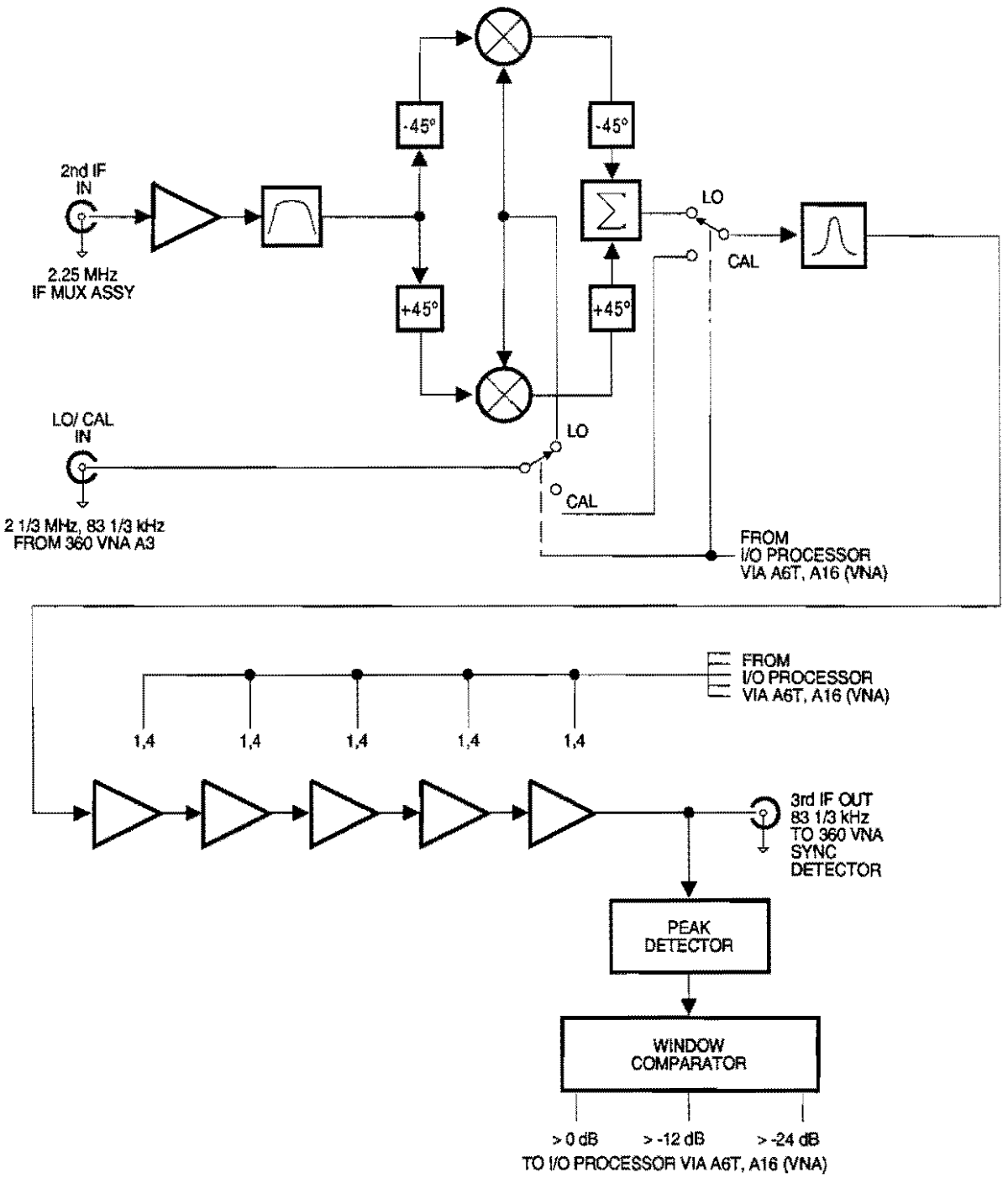


Figure 7-5. *A1T, A2T, and A3T Channel IF Amplifier PCB Block Diagram*

7-7 A4T LO 2 PCB CIRCUIT DESCRIPTION

The A4T LO 2 PCB (Figure 7-6) provides the second local oscillator (LO) signal to the A8T and A10T Buffer Amplifiers. There it mixes with the first IF signal to produce the second IF of 2.25 MHz. The A4T circuitry consists of a loop gain control circuit, a summation amplifier, an 8-bit digital-to-analog converter (DAC), a linearizer, a voltage-tuned oscillator (VTO), a series of divide-by-2 frequency dividers, a window comparator, a frequency range selection circuit, and several buffer amplifiers.

The frequency control input is a variable dc voltage coming from the A2 LO 2 Phase Lock PCB of the VNA. The window comparator determines if the dc voltage has the levels required for a phase lock. The output of the window comparator sends a status bit to the I/O processor of the VNA for diagnostic purposes.

If the test set signal source is a synthesizer, the VNA's I/O processor — operating through the A6T Digital Interface PCB — changes the attenuation in loop gain control circuit to compensate for loop gain changes each time a different frequency range is selected.

The VNA's I/O processor pre-tunes the VTO by sending a byte to the 8-bit DAC via the A6T Digital Interface PCB. The output of the DAC is summed with the frequency control input in the summation amplifier. The DAC output coarse tunes the VTO frequency output. The frequency control input fine tunes the frequency output.

The output of the summation amplifier is linearized to compensate for nonlinearities in the VTO. The output of the VTO is a 98 MHz to 272.25 MHz signal. One output is buffered and sent to the VNA's A2 LO 2 Phase Lock PCB. The other output is sent to a series of divide-by-2 frequency dividers.

Depending on selection, the frequency range selection circuit sends the VTO output signal directly to the output buffer amplifiers or through any of the frequency dividers before being sent to the output buffer amplifiers. The buffer amplifier outputs are the second local oscillator frequencies and have a frequency range from 12.25 MHz (divide by 8) to 272.25 MHz (divide by 1).

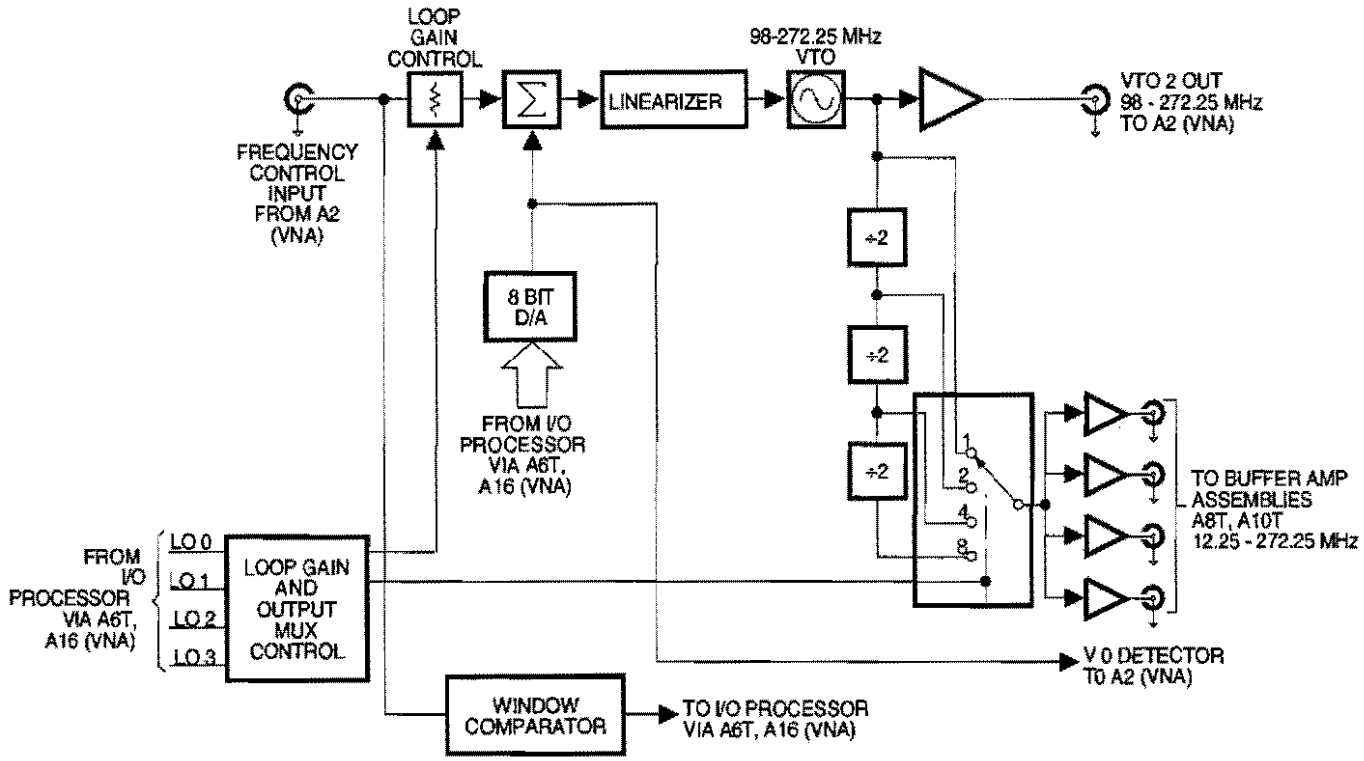


Figure 7-6. *A4T LO 2 PCB Block Diagram*

7-8 A5T LO 1 PCB CIRCUIT DESCRIPTION

During the heterodyne mode of operation, the A5T LO 1 PCB (Figure 7-7) provides the first local oscillator signal (LO 1) to the A12T Power Amplifier assembly. In A12T, the LO 1 signal is amplified to drive the harmonic generator, producing the harmonic pulses necessary for heterodyning in the samplers, A9T and A11T.

The A5T circuitry consists of a summation amplifier, an 8-bit digital-to-analog converter (DAC), a 100 kHz/150 kHz notch filter, a linearizer, a voltage-tuned oscillator (VTO), a window comparator, and two buffer amplifiers.

The frequency control input is a variable dc voltage coming from the A1 LO1 Phase Lock PCB of the VNA. The window comparator determines if the dc voltage is in the necessary range of levels required for a phase lock. The output of the window comparator sends a status bit to the I/O Processor of the VNA for diagnostic purposes.

- The VNA's I/O processor pre-tunes the VTO by sending a byte to the 8-bit DAC via the A6T Digital Interface PCB. The output of the DAC is summed with the frequency control input in the summation amplifier.

The DAC output coarse tunes the VTO frequency output and the frequency control input fine tunes the frequency output. The output of the Summation Amplifier is first filtered by the 100 kHz/150 kHz notch filter to remove unwanted signals and then linearized to compensate for nonlinearities in the VTO. The output of the VTO is a 357 MHz to 536.5 MHz signal.

One output is sent to the A1 LO1 Phase Lock PCB in the VNA. The other output is sent to a buffer amplifier. When the test set is in the heterodyne mode, the VNA's I/O processor turns on the buffer amplifier sending the first local oscillator signal to the A12T Power Amplifier Assembly.

In the direct mode (40 to 270 MHz), the A12T Power Amplifier is turned off and the first local oscillator signal is attenuated.

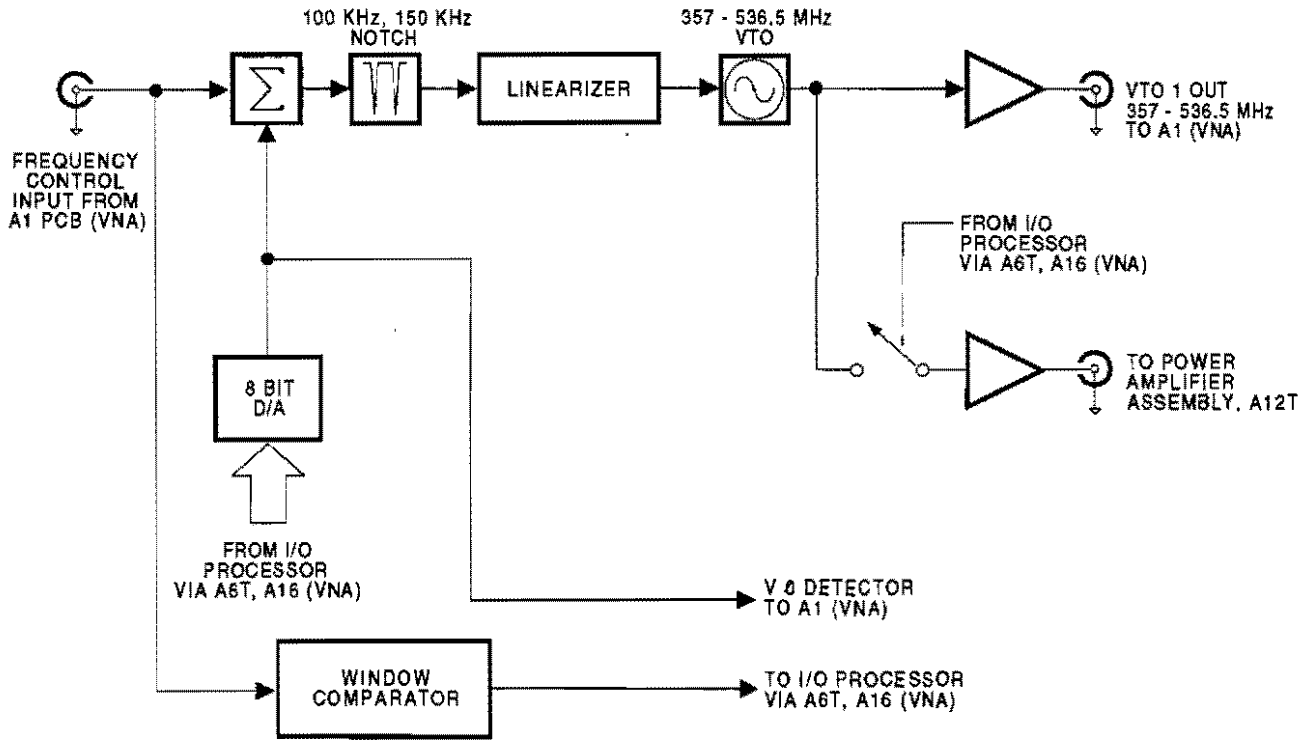


Figure 7-7. A5T LO 1 PCB Block Diagram

7-9 A6T DIGITAL INTERFACE PCB CIRCUIT DESCRIPTION

The A6T Digital Interface PCB (Figure 7-8) provides digital interface between the VNA and test set. The A6T circuitry consists of a bi-directional bus transceiver, latches, buffers, strobe decode logic, three-to-eight decoders, and power filtering and regulation circuits.

The address and data bus connects the test set to the VNA's A16 Test Set I/O PCB. Upon receiving a strobe pulse from the VNA, the strobe decode logic circuit enables the input latch to latch in first the address byte and then the data byte. This enables the decoders to read the address data and select the appropriate device.

The bus transceiver is a bi-directional interface for the input data going to and output data coming from the test set circuits. When bit 7 of the address data byte is set high, the change in logic level of the bus transceiver direction input (DIR) reverses the direction of the data bus. If the data byte is to be written to the test set, the 3-to-8 decoder enables the appropriate latch. If the data byte is coming from the test set and going to the VNA, the 3-to-8 decoder enables the appropriate buffer.

The power regulation and filtering circuitry regulates and filters the +8 Vdc, –18 Vdc, and +18 Vdc from the VNA, producing the +5 Vdc to power the A6T PCB and the +15 Vdc and –15 Vdc to power the A8T, A10T, and A12T PCBs.

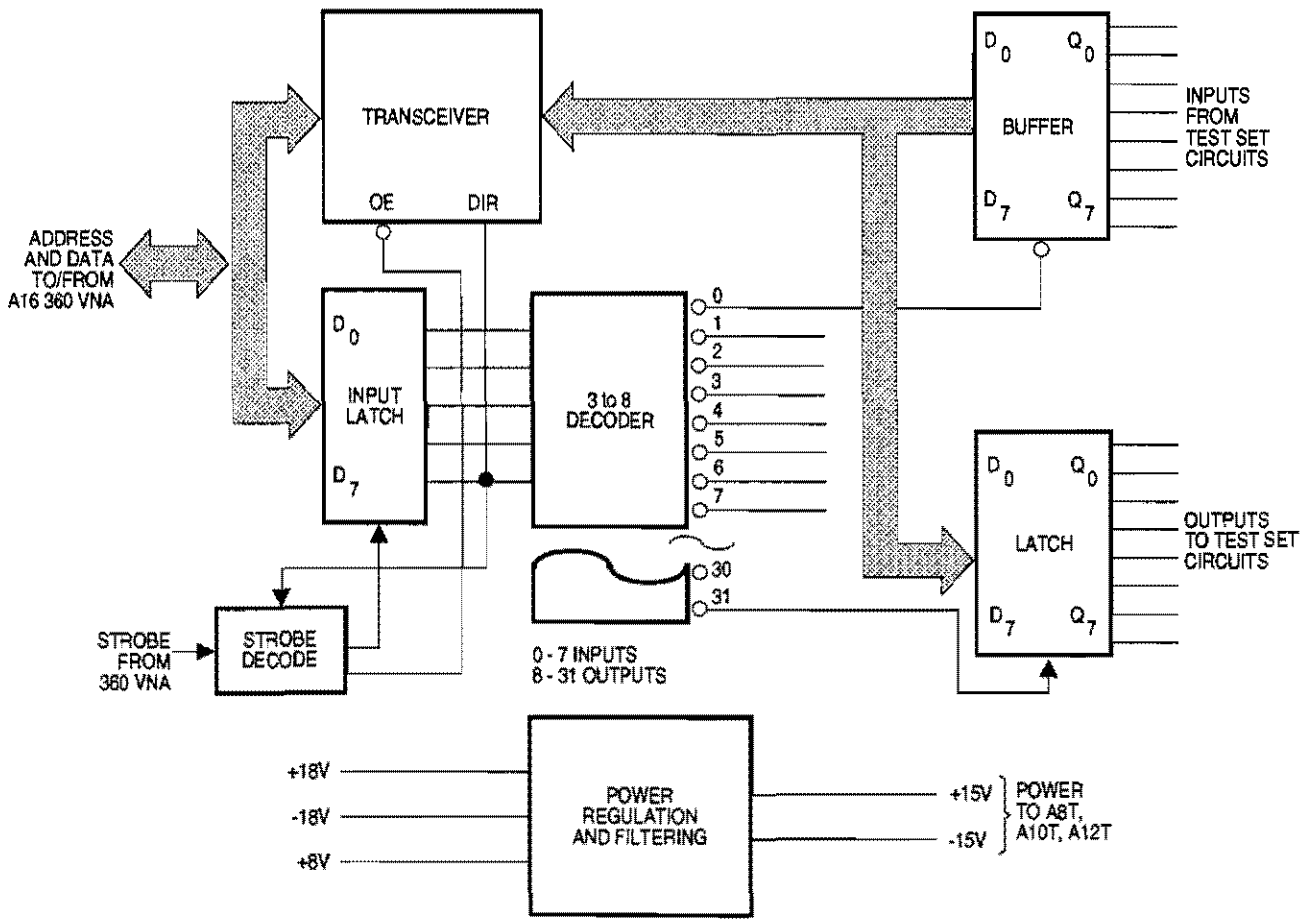


Figure 7-8. A6T Digital Interface PCB Block Diagram

7-10 A7T ATTENUATOR DRIVER PCB CIRCUIT DESCRIPTION

The A7T Attenuator Driver PCB (Figure 7-9) provides drive for the A20T, A21T, and A22T step attenuators and the bias enable relay. The A7T circuitry consists of three latch and coil drivers and a bias enable circuit.

The four data bits (D0-D3), received from the VNA's I/O Processor determines the value to which the step attenuators are to be set. The VNA then sends an attenuator strobe pulse, via the A6T Digital Processor PCB, to activate the selected latch and coil driver circuit to set the step attenuator to this value. Using this same method, the VNA activates the bias enable circuit to enable PORT 1 and PORT 2 bias voltage.

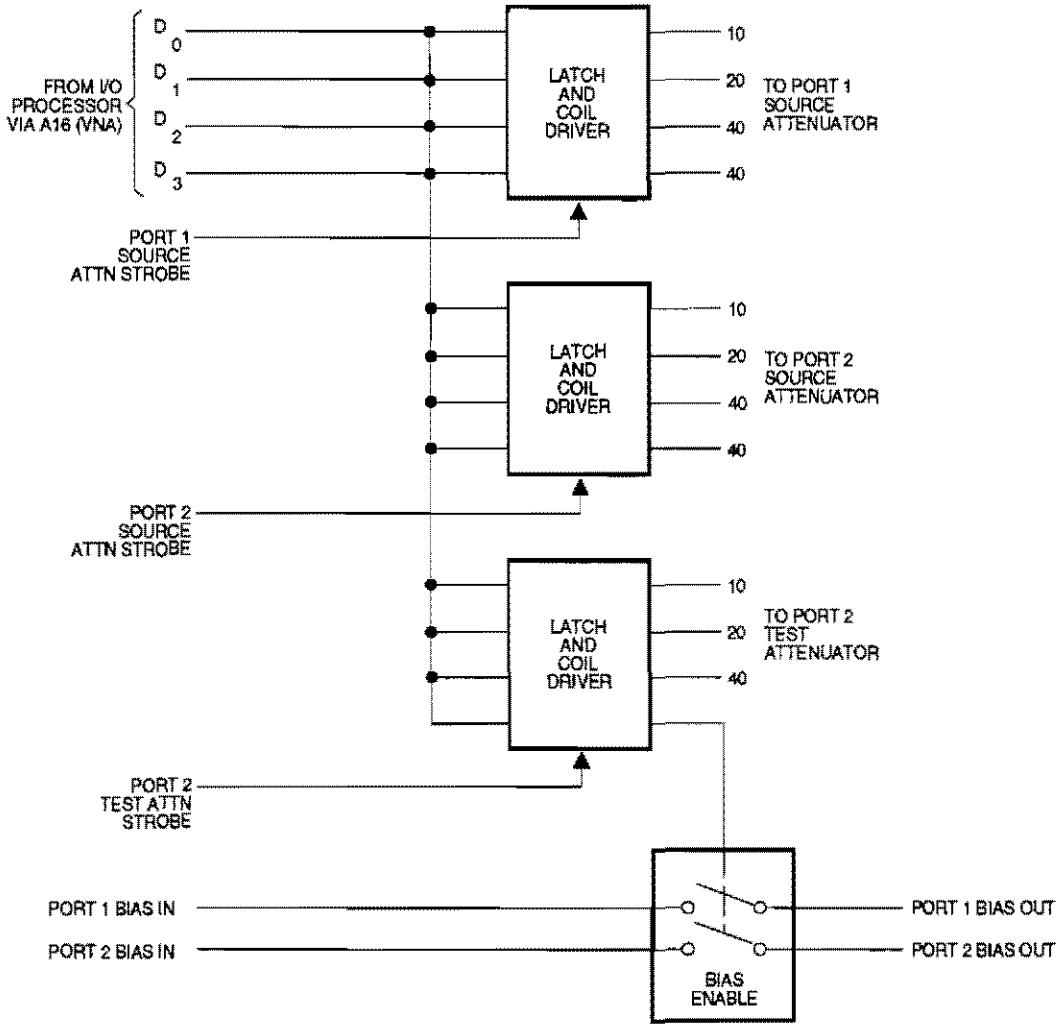


Figure 7-9. *A7T Attenuator Driver PCB Block Diagram*

7-11 A23T MOTHERBOARD PCB CIRCUIT DESCRIPTION

The A23T Motherboard PCB contains no active devices. It electrically connects the circuits within the test set. It also provides electrical interface to the VNA through the rear panel SIGNAL and CONTROL connectors.

Additionally, the A23T PCB holds the connectors that are the physical interface to the PCB assemblies of the test set.

7-12 A24T SOURCE LOCK/REFERENCE SELECT ASSEMBLY CIRCUIT DESCRIPTION

The A24T Source Lock/Reference Select assembly (Figure 7-3 or 7-4), also referred to as the LRL Module, contains a source lock reference circuit and a series of FET switches that provide selection of the source of the second IF signal for the A2T Reference Channel IF Amplifier, the A3T Channel A IF Amplifier, and the VNA source lock circuitry. The switches are controlled by the VNA via the A6T Digital Interface PCB. The second IF signal source selections are:

- A2T Reference Channel IF Amplifier – R_A or R_B
- A3T Channel A IF Amplifier – T_A or R_A
- VNA Source Lock – R_A for forward measurements, R_B for reverse measurements

The R_A or R_B signal entering the source lock reference circuit is buffered and passes through a 3 MHz low-pass filter where undesirable frequencies are filtered out. The signal is sampled by a level detector to determine if it is of sufficient amplitude to achieve a phase lock. The VNA's I/O processor monitors the level detector output (via the A6T Digital Interface PCB) to help in determining the cause of a lock failure should one occur.

The signal output from the 3 MHz low-pass filter also goes to a limiter that keeps it within a specified tolerance level. It then passes through a 2.25 MHz bandpass filter to select only the desired 2.25 MHz second IF signal. The signal output from the filter is buffered and sent to the VNA's A6 PCB where it becomes the source lock reference frequency.

7-13 A27T AMPLIFIER/ SWITCH DRIVER PCB CIRCUIT DESCRIPTION

The A27T Amplifier/Switch Driver PCB (Figure 7-10) provides switch drive current for the A28T and A29T SPDT/Splitter Switch assemblies, +5 Vdc power for the amplifiers in the A30T and A31T Tripler assemblies, and sampler bias voltage for the A9T and A11T Sampler assemblies. The A27T circuitry consists of data latches and switch driver, amplifier power, sampler bias, and power filtering and regulation circuits.

The VNA's I/O processor provides switch and amplifier control data (D0-D7) to the data latches. Upon receiving the strobe pulses from the VNA via the A6T Digital Control PCB, the control data is latched-in, thus enabling the selected switch drivers and amplifier power circuits.

When the VNA is operating in the 40 GHz to 60 GHz range, the A27T PCB outputs the following:

- Switch driver current to the A28T and A29T SPDT/Splitter Switch assemblies to place them in the 40 to 60 GHz position.
- +5 Vdc power to drive the amplifiers in the A30T and A31T Tripler assemblies.
- Sampler bias voltage to the A9T and A11T Sampler assemblies. Sampler bias voltage is factory adjusted to enhance the sampler performance above 50 GHz.

When the VNA is operating in the 40 MHz to 40 GHz range, The A27T PCB outputs switch driver current to the A28T and A29T SPDT/Splitter Switch assemblies to place them in the 40 MHz to 40 GHz position. The amplifier power and sampler bias voltage outputs are disabled.

The power filtering and regulation circuitry filters and regulates the +8 Vdc, –18 Vdc, and +18 Vdc from the VNA, producing the +5 Vdc, –8 Vdc, +15 Vdc, and –15 Vdc required to power the A27T circuitry.

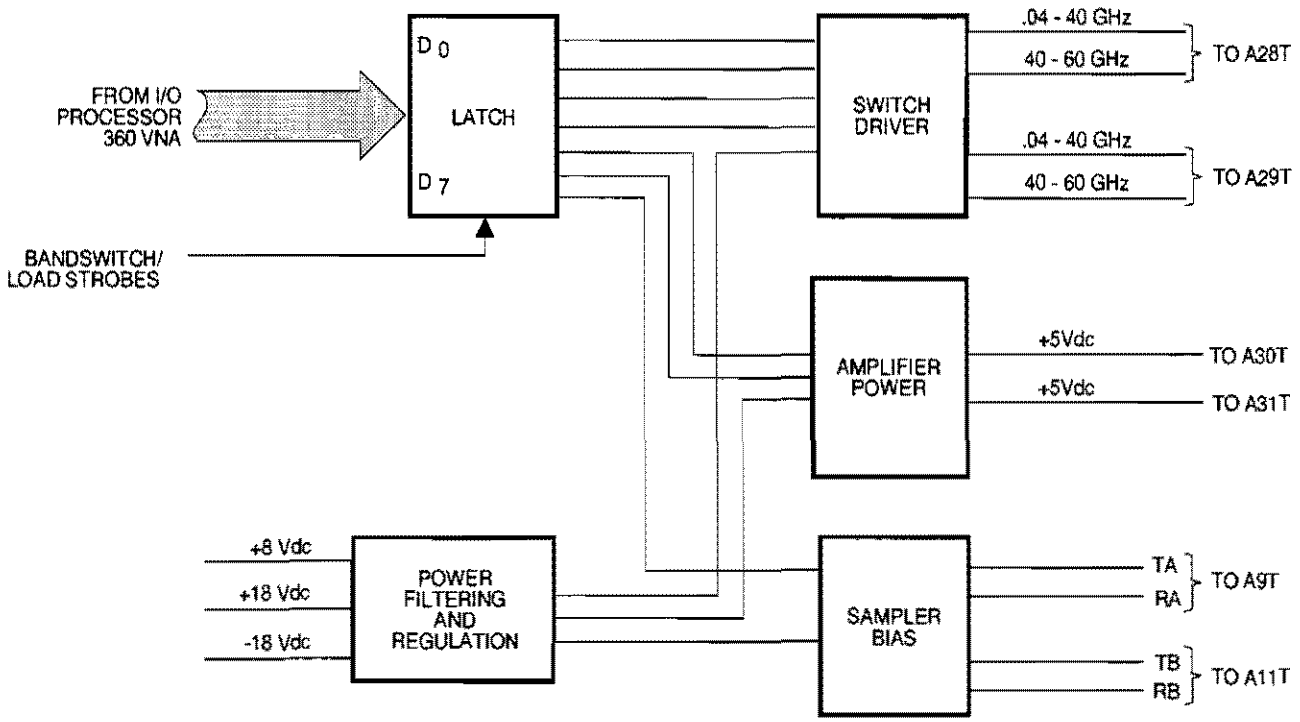


Figure 7-10. *A27T Amplifier/Switch Driver PCB Block Diagram*

7-14 RF DECK ASSEMBLY DESCRIPTIONS

The following paragraphs provide functional descriptions for each of the RF components/assemblies that make up a typical RF Deck assembly. Refer to Figure 7-3 or 7-4, as applicable for your model, while reading the following descriptions.

A8T/A9T and A10T/A11T Buffer Amplifier/ Sampler Assemblies

A buffer amplifier/sampler assembly consists of a buffer amplifier assembly and a sampler assembly grouped as a single unit. the buffer amplifier/ sampler assembly has a single WILTRON part number and is always replaced as a single unit. The part number and serial number are found on the buffer amplifier.

The A8T/A9T Channel B Buffer Amplifier/Sampler and the A10T/A11T Channel A Buffer Amplifier/ Sampler assemblies provide down conversion of the 40 MHz to 60 (or 65*) GHz RF input signals to the second IF frequency of 2.25 MHz.

A9T and A11T are dual sampler assemblies. Each samples two channels. A9T samples Test Channel B (T_B) and Reference Channel B (R_B) and A11T sample Test Channel A (T_A) and Reference Channel A (R_A). The dual sampler assemblies consist of electronically controlled switch circuits.

For frequencies in the range of 40 MHz to 40 GHz, bias voltage to control the sampler switches is received from the A6T Digital Interface PCB via the buffer amplifier assembly. For frequencies above 40 GHz, bias voltage is received from the A27T Amplifier/Switch Driver PCB via the buffer amplifier assembly.

When the test set is operating in the direct mode (40 MHz to 270 MHz), the sampler switches are biased to close, which passes the input RF signal directly to the buffer amplifier assembly. When the test set is operating in the heterodyne mode (270 MHz to 40 GHz), the sampler switches are self-biasing. They switch at the rate of the first local oscillator frequencies.

* Test Set Models 3613A and 3623A only

This sampler switching action causes a mixing (heterodyning) of the first local oscillator frequencies and the input RF signal. One of the signals that results from this heterodyning is the 89 MHz first IF. This signal goes to the buffer amplifier assembly. When the test set is in the heterodyne mode above 50 GHz, the sampler-switch-bias voltage is factory adjusted to enhance sampler performance.

A8T and A10T are dual-buffer-amplifier assemblies. Each down-converts two channels to second IF signals. A8T down-converts Test Channel B (T_B) and Reference Channel B (R_B) and A10T down-converts Test Channel A (T_A) and Reference Channel A (R_A). The buffer amplifier assemblies provide 0 dB conversion gain (RF in to 2nd IF out). The buffer amplifiers have slopes which result in a conversion gain of –10 dB at high frequencies (approximately 40 GHz).

The direct mode (40 MHz to 270 MHz) or heterodyne mode (first IF of 89 ±4 MHz) signal inputs to the buffer amplifier are first amplified; then they pass through a notch filter to eliminate unwanted harmonics; then they go to mixer circuit. In this circuit, they mix with the second local oscillator signal to produce the desired second IF of 2.25 MHz.

The second IF signal passes through a low-pass filter to eliminate unwanted frequencies. It then goes to a buffer amplifier for output. The T_A, R_A, and R_B second IF signal outputs go to the A24T Source Lock/Reference Select Assembly, and the T_B second IF output goes to the A1T Channel B IF Amplifier PCB.

A12T Power Amplifier Assembly

The A12T Power Amplifier assembly contains the 500 MHz power amplifier and harmonic generator. The power amplifier amplifies the first local oscillator signal to achieve adequate power levels to drive the harmonic generator.

When the test set is operating in the direct mode, the VNA sends a signal to the A6T Digital Interface PCB. This signal disables A12T by removing the +15V power. When the test set is operating in the heterodyne mode, the power amplifier amplifies the first local oscillator signal. This signal causes the harmonic generator to produce harmonic pulses that are necessary for heterodyning to take place in samplers A9T and A11T.

A13T Transfer Switch Assembly

There are two configurations of the A13T Transfer Switch assembly. In the Models 3610A/11A and 3620A/21A Test Sets, the A13T assembly consists of an electronic switch and a pair of resistive splitters. In the Models 3612A/13A/15A and 3622A/23A/25A Test Sets, the A13T assembly consists of an electronic switch only.

The A13T Transfer Switch assembly receives the RF signal from the VNA system signal source and switches it to PORT 1 for forward measurements and to PORT 2 for reverse measurements. The switching of A13T is controlled by the VNA, via the A6T Digital Interface PCB.

In the Models 3610A/11A and 3620A/21A, the resistive splitters within A13T split the RF signal. A portion of this signal goes to a test port and a portion goes to the reference channel (R_A or R_B). The resistive splitters maintain the same RF power, magnitude, and phase relationship between the RF signals that go to the test port and reference channel.

In the Models 3612A/13A/15A and 3622A/23A/25A, the RF signal is routed to PORT 1 and PORT 2 via the A28T and A29T SPDT/Splitter Switch assemblies. Signal splitting is accomplished in the A28T and A29T SPDT/Splitter Switch assemblies for frequencies in the 40 MHz to 40 GHz range. It is accomplished in the A30T and A31T Tripler assemblies for frequencies above 40 GHz.

A14T/A15T Coupler / Connector Assemblies

The A14T and A15T Coupler/Connector assemblies are the directional couplers for the test ports – A14T for test port 1 and A15T for test port 2.

In the forward measurement mode, the A14T assembly couples the stimulus signal to the DUT. It couples the reflected signal from the DUT to test channel A (T_A). In the reverse measurement mode, the stimulus signal that travels through the DUT is coupled by A14T to T_A.

In the reverse measurement mode, the A15T assembly couples the stimulus signal to the DUT and couples the reflected signal from the DUT to test channel B (T_B). In the forward measurement mode, the stimulus signal that travels through the DUT is coupled by A15T to T_B.

A16T Power Divider Assembly

The A16T Three-Way Power Divider assembly receives the calibration (83⅓ kHz) or third local oscillator (2⅓ MHz) signal from the VNA A3 PCB and divides it between three paths of equal impedance: A1T, A2T, and A3T. This enables the same oscillator (LO 3) to drive all three mixer circuits with equal amplitude and minimum loss.

A17T Reference Delay Mounting Bracket

The A17T assembly is the reference delay mounting bracket. This rear panel mounted, mechanical assembly has four connectors and two cable loops, W30 and W31. The two cable loops allow the two reference channels, R_A and R_B, to be used as a receiver. This provides for custom-defined user parameters with any combination of channels.

A18T/A19T Bias Tees

The A18T and A19T Bias Tee assemblies are components of the Models 362XA Active Device Test Sets only.

The A18T and A19T Bias Tee assemblies provide bias capability to PORT 1 and PORT 2 respectively. They are necessary to supply dc voltage to active DUTs requiring bias.

A bias tee functionally consists of a coupling capacitor and an inductor. The capacitor couples the RF signal; the inductor provides a low impedance path for the dc voltage and a high impedance path for RF. In this way, the bias tee assemblies provide dc bias voltage to the active DUTs with minimum signal loss.

A20T, A21T, and A22T Step Attenuators

The A20T, A21T, and A22T Step Attenuator assemblies are components of the Models 362XA Active Device Test Sets only. A20T is the PORT 2 test attenuator, A21T is the PORT 2 source attenuator, and A22T is the PORT 1 source attenuator.

A20T, A21T, and A22T are digitally-programmable, 10 dB, 0 to 70 dB step attenuators. Attenuation is controlled by the VNA via the A7T Attenuator Driver PCB.

A20T, the PORT 2 test attenuator, controls the signal level from the DUT. A maximum attenuation of 40 dB can be selected for A20T. A21T, the PORT 2 source attenuator, and A22T, the PORT 1 source attenuator control the stimulus signal level. A maximum of 70 dB can be selected for A21T and A22T.

The step attenuator assemblies consist of three attenuator pads –40 dB, –20 dB, and –10 dB. Any combination of these three attenuator pads can be switched in through digitally-selected solenoid switches. Each attenuator pad can also be bypassed by switching in an internal thruline.

A25T RF Splitter Assembly:

The A25T RF Splitter assembly splits the harmonic generator output signal from the A12T Power Amplifier assembly into two paths of equal impedance. The two paths supply signals that are rich in harmonics to the A9T and A11T Samplers for heterodyning.

A28T and A29T SPDT/Splitter Switch Assemblies

The A28T and A29T SPDT/Splitter Switch assemblies are components of the Models 3612A/13A/15A and 3622A/23A/25A Test Sets only.

The A28T and A29T SPDT/Splitter Switch assemblies have two switch positions — 40 MHz to 40 GHz and above 40 GHz. A28T and A29T switching is controlled by the VNA through the A27T Amplifier/Switch Driver PCB.

When the VNA is operating in the 40 MHz to 40 GHz range, the switches are positioned such that the RF signal goes through the A28T and A29T splitter. Part of the RF signal goes to the test ports,via the couplers, and part goes to the reference channels. Both parts go through the multiplexer couplers of the A30T and A31T Tripler assemblies.

When the VNA is in the above 40 GHz range, the switches are positioned such that the RF signal is routed to the inputs of the A30T and A31T Tripler assemblies.

A30T and A31T Tripler Assemblies

The A30T and A31T Tripler assemblies are components of Test Set Models 3612A/13A/15A and 3622A/23A/25A only. These assemblies are frequency triplers that enable the test set to provide frequency coverage to 50**, 60, or 65* GHz.

The dc power for the A30T and A31T Tripler assemblies is controlled by the VNA through the A27T Amplifier/Switch Driver PCB. For test set models 3613A and 3623 A, the dc power for the A30T and A31T assemblies is provided by a 40-5x Auxiliary Power Supply via the rear panel AUXILIARY POWER INPUT connector.

When the VNA is operating in the 40 GHz to 60 (or 65) GHz range, power is applied to the A30T and A31T Tripler assemblies. The switches in the A28T and A29T SPDT/Splitter Switch assemblies are positioned such that the RF signal is routed to the inputs of the tripler assemblies.

The 13.33 GHz to 16.67, 20, or 21.67 GHz signals are amplified then tripled in frequency to obtain the final output of 40 to 50, 60 or 65 GHz. From the multiplier, the RF signal goes through an isolator, which prevents the reflection of RF energy back to the multiplier, and a high-pass filter, which eliminates unwanted frequencies.

The RF signal is sent to the multiplexer coupler, where a portion of it is coupled out to the test ports and another portion to the reference channels.

When the VNA is in the 40 MHz to 40 GHz range, power to A30T and A31T is removed and the switches in A28T and A29T are positioned such that the RF signal is routed through the splitter within A28T and A29T. The split RF signal is sent through the multiplexer couplers of A30T and A31T to PORT 1 and PORT 2 and on to the reference channels.

* Test Set Models 3613A and 3623A only
** Test Set Models 3615A and 3625A

Chapter 8
3630A/3631A Test Sets Information

Table of Contents

Chapter 8
3630A/3631A Test Sets Information

8-1 INTRODUCTION

This chapter describes the 3630A and 3631A Test Sets. It provides installation and operation information, an overall functional description, mainframe PCB descriptions, and RF deck assembly descriptions.

8-2 INSTALLATION AND OPERATION

The 363XA Frequency Converter Test Sets are four-channel receivers that measure magnitude and phase of frequency conversion devices. They can operate with two source signals and the receiver signal, all at different frequencies and controlled from the VNA front panel.

These test sets can be configured by the user to address a wide variety of applications. Information pertaining to the operation of these test sets is provided in Appendix A, at the rear of this manual.

8-3 FUNCTIONAL DESCRIPTION

The 3630A and 3631A Test Sets (Figure 8-1, page 8-7) are similar in construction and operation. The 3631A differs only by having an additional front end frequency multiplier for its higher frequency operation to 60 GHz. Figure 8-2, page 8-8, shows assembly locations.

Front End

The test sets receive RF energy from the source. This energy is divided. A portion goes to a step attenuator, then out to the RF OUT port. Another portion goes out to the SOURCE LOCK OUT port. The device-under-test (DUT) uses these two signals and returns the Test A/B (T_A and T_B) and Reference A/B (R_A and R_B) signals to the test set front panel ports.

First and Second IF Down Conversion

The test sets have two primary modes of operation: direct and heterodyne. The direct mode is for frequencies between 40 MHz and 270 MHz. The heterodyne mode is for frequencies from 270 MHz to 40 GHz.

In the direct mode, dual samplers A9T and A11T are like closed switches and send the test (T_A and T_B) and reference (R_A and R_B) signals to the buffer amplifiers A8T and A10T.

In the heterodyne mode, A9T and A11T switch either at the frequency of the first local oscillator (LO 1) or at harmonics of the first LO. The A5T First Local Oscillator PCB— controlled by the VNA — outputs a 357 MHz to 536.5 MHz LO frequency.

The first LO output goes to the A12T power amplifier assembly, where it is amplified to drive the harmonic generator. This produces the harmonic pulses necessary for heterodyning in the samplers.

The A12T first LO output goes to A9T and A11T, via the A25T RF splitter assembly. The switching action of a sampler causes a mixing of the first LO frequencies and the input signal (T_A, T_B, R_A, or R_B). This heterodyning action provides the desired intermediate frequency (IF) of 89 MHz ±4 MHz. The resultant first IF signals are input to buffer amplifiers A8T and A10T.

In the buffer amplifiers, the direct mode signal (40 MHz to 270 MHz) or first IF signal (89 MHz) is mixed with the second local oscillator (LO 2) signal. The A4T LO 2 PCB, which is controlled by the VNA, outputs an LO frequency in the range between 12.25 MHz and 272.25 MHz.

The heterodyning of the direct mode/first IF and second LO frequencies produces the desired second IF of 2.25 MHz. The buffer amplifier assemblies provide 0 dB conversion gain. The second IF test and reference signals (T_A, R_A, and R_B) from the A8T and A10T buffer amplifiers go to the A24T Source Lock/Reference Select assembly. The second IF test signal T_B — which is output by one half of the A8T buffer amplifier — goes directly to the A1T Channel B IF Amplifier.

Source Lock/ Reference Signal Selection

The A24T Source Lock/Reference Select assembly (also referred to as the LRL Module), contains switches for selecting the desired second IF signal source for the A2T Reference Channel IF Amplifier, the A3T Channel A IF Amplifier, and the VNA Source Lock circuitry.

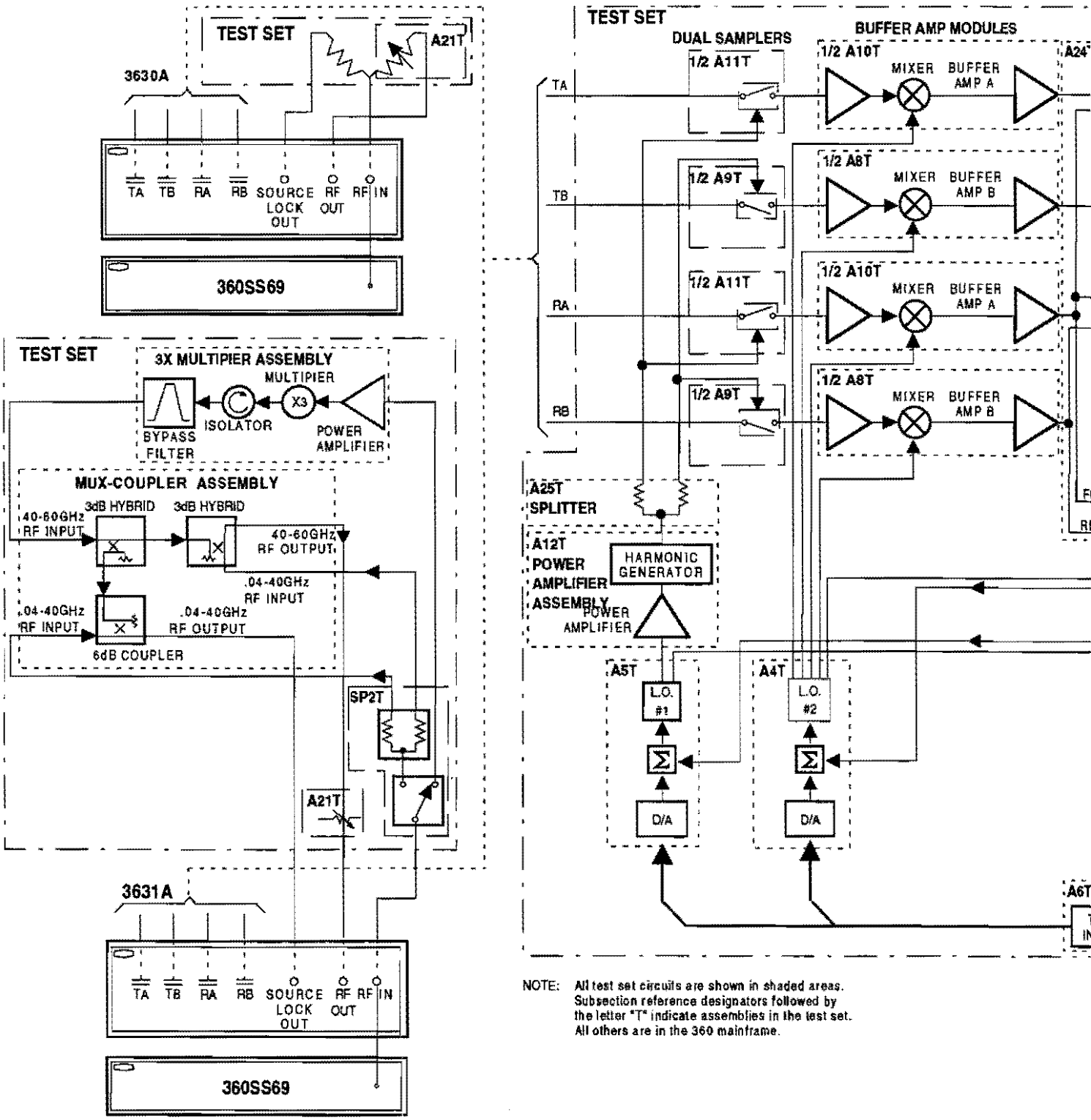
The A24T switches are controlled by the VNA through the A6T Digital Interface PCB. The second IF signal source for the A2T Reference Channel IF Amplifier is either R_A or R_B. The second IF signal source for the A3T Channel IF Amplifier is either T_A or R_A. The second IF signal source for the VNA Source Lock circuitry is R_A for forward measurements and R_B for reverse measurements.

Third IF Down Conversion and Amplification

The A1T, A2T, and A3T Channel IF Amplifiers have two modes of operation — measurement (LO) and calibration (CAL). In the measurement mode, the second IF signal is mixed with the third local oscillator (LO 3) signal of 2⅓ MHz received from the VNA via the A16T Three-Way Power Divider.

The heterodyning of the second IF and third LO frequency produces the desired third IF of 83⅓ kHz. The third IF signal is then amplified as required by five gain-ranging amplifiers before being output to the VNA Synchronous Detector circuits. The gain-ranging amplifiers are controlled by the VNA, through the A6T Digital Interface PCB.

The VNA automatically places the Channel IF Amplifiers in the calibration mode every three minutes. In this mode, an 83⅓ kHz signal is received from the VNA via the A16T Three-Way Power Divider. This 83⅓ kHz calibration signal goes directly to the gain-ranging amplifiers. These amplifier are then automatically calibrated to assure optimum accuracy and predictability of the Channel IF Amplifier outputs.



NOTE: All test set circuits are shown in shaded areas. Subsection reference designators followed by the letter "T" indicate assemblies in the test set. All others are in the 360 mainframe.

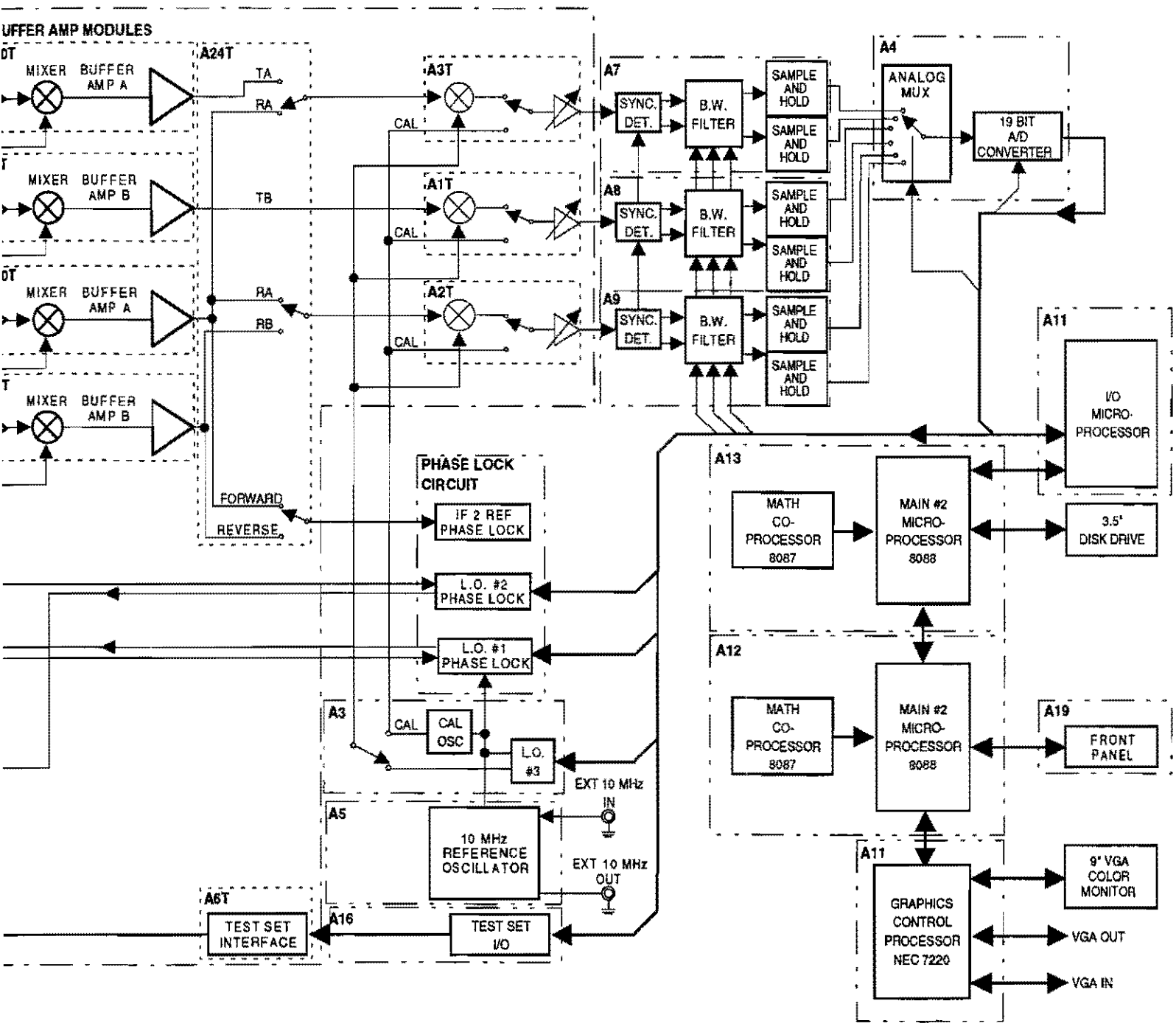


Figure 8-1. Models 3630A/3631A Block Diagram

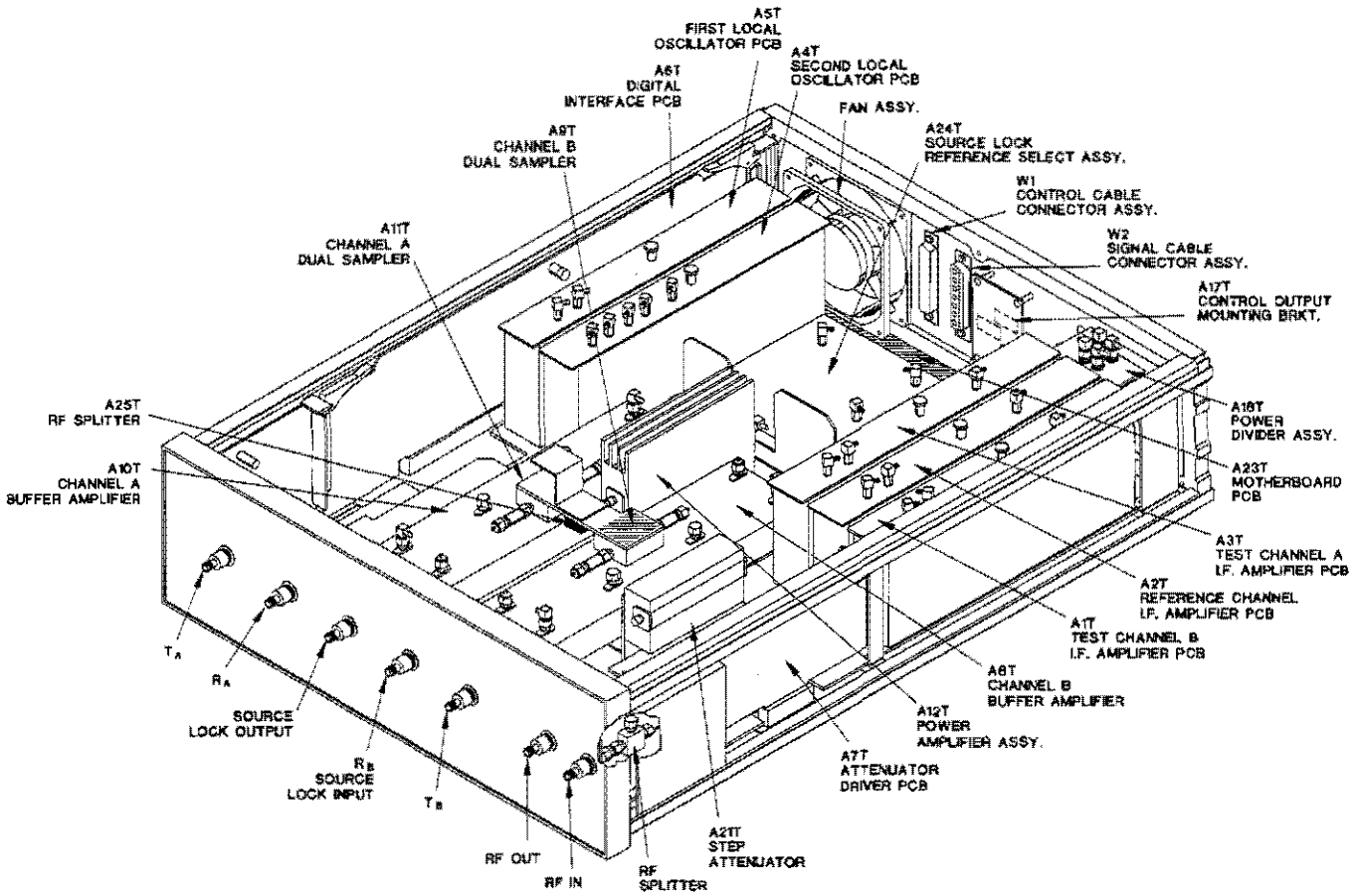


Figure 8-2. Model 3630A/3631A Assembly Locations

8-5 A1T, A2T, and A3T CHANNEL IF AMPLIFIER PCB CIRCUIT DESCRIPTION

The A1T, A2T, and A3T Channel IF Amplifier assemblies (Figure 8-3) are functionally equivalent. The A1T and A3T PCBs are mechanically identical; only the PCB cover plates are different. The A2T PCB has a different component layout and card-edge connector pin configuration. The following functional description applies to all three.

The Channel IF Amplifier PCBs have two modes of operation: measurement (LO) and calibration (CAL). In the measurement mode, the 2.25 MHz second IF signal input goes via a buffer amplifier to a 2.25 MHz bandpass filter that removes harmonics and other unnecessary signals. The output from the filter is split into two separate signal paths. The signals are then phase-shifted; one signal by +45° and the other by −45°. Each of the phase-shifted signals is mixed with a 2⅓ MHz third local oscillator signal received from the VNA.

One of the frequencies produced in each mixer is 83⅓ kHz — the difference of the two frequencies. The two phase-shifted, heterodyned signals are then filtered, phase shifted back to 0°, and summed in an amplifier to reject the image frequency. The output passes through an 83⅓ kHz bandpass filter that rejects all harmonics and subharmonics of the fundamental frequencies. The 83⅓ kHz third IF signal then goes to five gain-ranging amplifiers that have selectable gains of one or four.

The third IF signal output is maintained at an acceptable level through automatic gain control (AGC). The peak detector, at the output of the gain-ranging amplifiers, detects the peak signal level and sends a dc voltage representing this level to the comparator. The comparator determines if the dc voltage is in the necessary range of levels required by the VNA synchronous detectors. The comparator outputs one of three signals:

- L=> 0 dB — overload peak signal level condition
- L=> −12 dB — maximum peak signal level condition
- L=> −24 dB — minimum peak signal level condition.

These signals are sent via the A6T Digital Control PCB to the VNA. Responding to these signals, the VNA sends data through A6T to control the gain ranging amplifiers maintaining the peak signal level between 0 and −24 dB.

Third IF peak signal levels affect the amplifiers as follows:

- When the peak signal level is between 0 and –24 dB, all amplifiers are set to a gain of one.
- When the peak level drops below –24 dB, the first gain-ranging amplifier is set to a gain of four. The gain of the first amplifier remains at four until the signal reaches a peak level above –24 dB.
- If the peak signal drops to a level below –36 dB, the second gain-ranging amplifier is set to a gain of four.
- If the peak signal drops to a level below –48 dB, the third gain-ranging amplifier is set to a gain of four.
- If the peak signal drops to a level below –60 dB, the fourth gain-ranging amplifier is set to a gain of four.
- If the peak signal drops to a level below –72 dB, the fifth gain-ranging amplifier is set to a gain of four.

In this way the third IF signal is incrementally boosted each time the signal level at the peak detector drops 12 dB after the initial –24 dB threshold.

The VNA automatically places the A1T thru A3T Channel IF Amplifiers in the calibration mode every three minutes. In the calibration mode, an 83⅓ kHz signal is received from the VNA and sent directly to the gain-ranging amplifiers. The signal level is then incrementally increased by individually programming each of the gain-ranging amplifiers in succession. The outputs are then measured and compared to expected values. The VNA then trims each of the amplifiers using a software algorithm to achieve optimum accuracy and predictability.

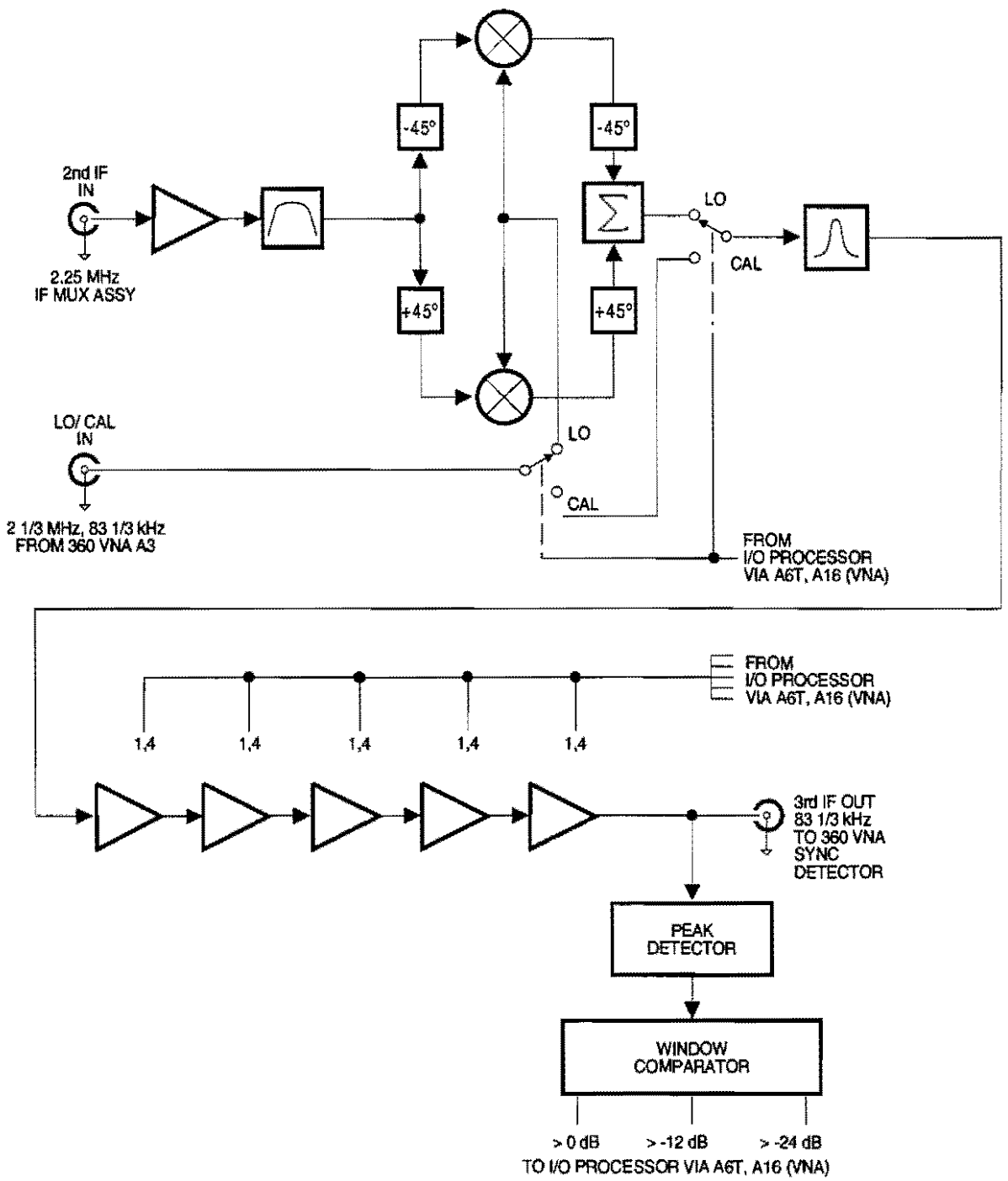


Figure 8-3. *A1T, A2T, and A3T Channel IF Amplifier PCB Block Diagram*

8-6 A4T LO 2 PCB CIRCUIT DESCRIPTION

The A4T LO 2 PCB (Figure 8-4) provides the second local oscillator (LO) signal to the A8T and A10T Buffer Amplifiers. There it mixes with the first IF signal to produce the second IF of 2.25 MHz. The A4T circuitry consists of a loop gain control circuit, a summation amplifier, an 8-bit digital-to-analog converter (DAC), a linearizer, a voltage-tuned oscillator (VTO), a series of divide-by-2 frequency dividers, a window comparator, a frequency range selection circuit, and several buffer amplifiers.

The frequency control input is a variable dc voltage coming from the A2 LO 2 Phase Lock PCB of the VNA. The window comparator determines if the dc voltage has the level required for a phase lock. The output of the window comparator sends a status bit to the I/O processor of the VNA for diagnostic purposes.

If the test set signal source is a synthesizer, the VNA's I/O processor — operating through the A6T Digital Interface PCB — changes the attenuation in loop gain control circuit to compensate for loop gain changes each time a different frequency range is selected.

The VNA's I/O processor pre-tunes the VTO by sending a byte to the 8-bit DAC via the A6T Digital Interface PCB. The output of the DAC is summed with the frequency control input in the summation amplifier. The DAC output coarse tunes the VTO frequency output. The frequency control input fine tunes the frequency output.

The output of the summation amplifier is linearized to compensate for nonlinearities in the VTO. The output of the VTO is a 98 MHz to 272.25 MHz signal. One output is buffered and sent to the VNA's A2 LO 2 Phase Lock PCB. The other output is sent to a series of divide-by-2 frequency dividers.

Depending on selection, the frequency range selection circuit sends the VTO output signal directly to the output buffer amplifiers or through any of the frequency dividers before being sent to the output buffer amplifiers. The buffer amplifier outputs are the second local oscillator frequencies and have a frequency range from 12.25 MHz (divide by 8) to 272.25 MHz (divide by 1).

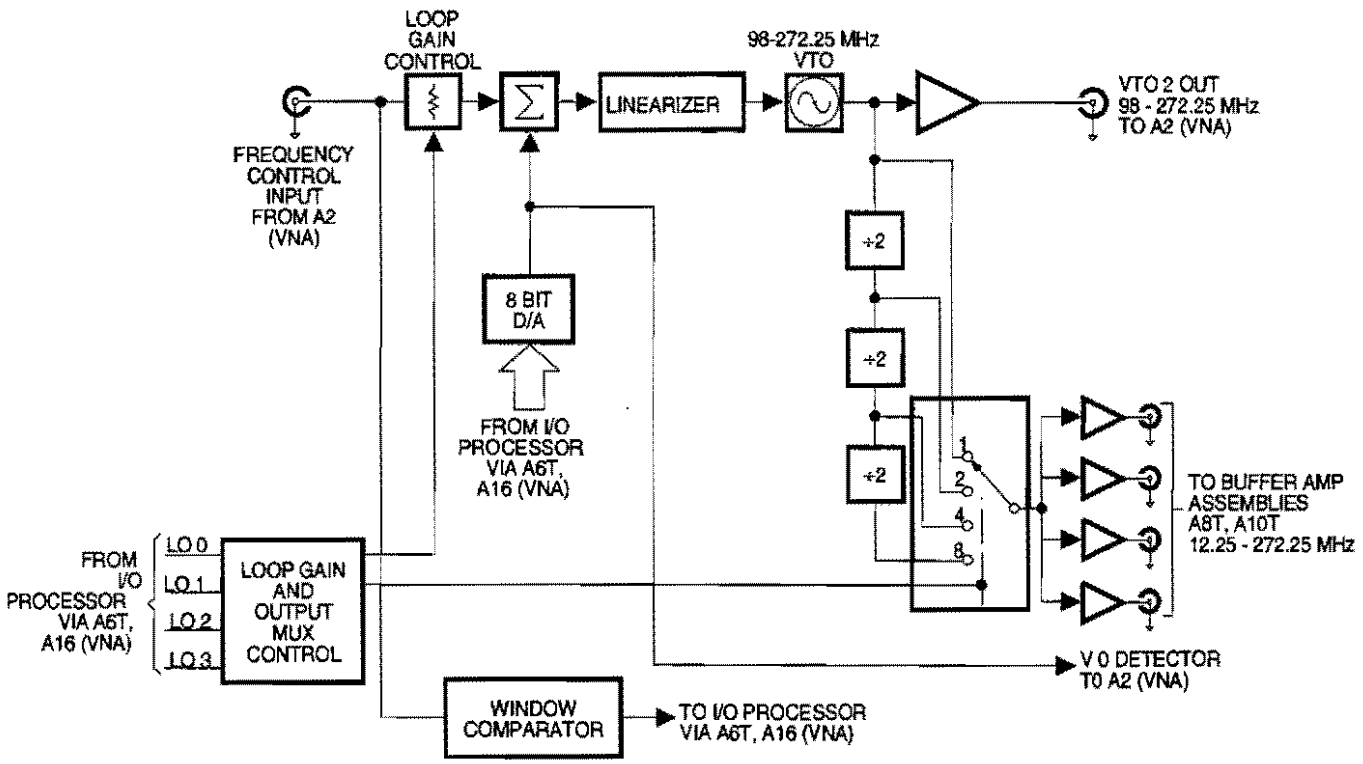


Figure 8-4. A4T LO 2 PCB Block Diagram

8-7 A5T LO 1 PCB CIRCUIT DESCRIPTION

During the heterodyne mode of operation, the A5T LO 1 PCB (Figure 8-5) provides the first local oscillator signal (LO 1) to the A12T Power Amplifier assembly. In A12T, the LO 1 signal is amplified to drive the harmonic generator, producing the harmonic pulses necessary for heterodyning in the samplers, A9T and A11T.

The A5T circuitry consists of a summation amplifier, an 8-bit digital-to-analog converter (DAC), a 100 kHz/150 kHz notch filter, a linearizer, a voltage-tuned oscillator (VTO), a window comparator, and two buffer amplifiers.

The frequency control input is a variable dc voltage coming from the A1 LO1 Phase Lock PCB of the VNA. The window comparator determines if the dc voltage is in the necessary range of levels required for a phase lock. The output of the window comparator sends a status bit to the I/O Processor of the VNA for diagnostic purposes.

- The VNA's I/O processor pre-tunes the VTO by sending a byte to the 8-bit DAC via the A6T Digital Interface PCB. The output of the DAC is summed with the frequency control input in the summation amplifier.

The DAC output coarse tunes the VTO frequency output and the frequency control input fine tunes the frequency output. The output of the Summation Amplifier is first filtered by the 100 kHz/150 kHz notch filter to remove unwanted signals and then linearized to compensate for nonlinearities in the VTO. The output of the VTO is a 357 MHz to 536.5 MHz signal.

One output is sent to the A1 LO1 Phase Lock PCB in the VNA . The other output is sent to a buffer amplifier. When the test set is in the heterodyne mode, the VNA's I/O processor turns on the buffer amplifier sending the first local oscillator signal to the A12T Power Amplifier Assembly.

In the direct mode (40 to 270 MHz), the A12T Power Amplifier is turned off and the first local oscillator signal is attenuated.

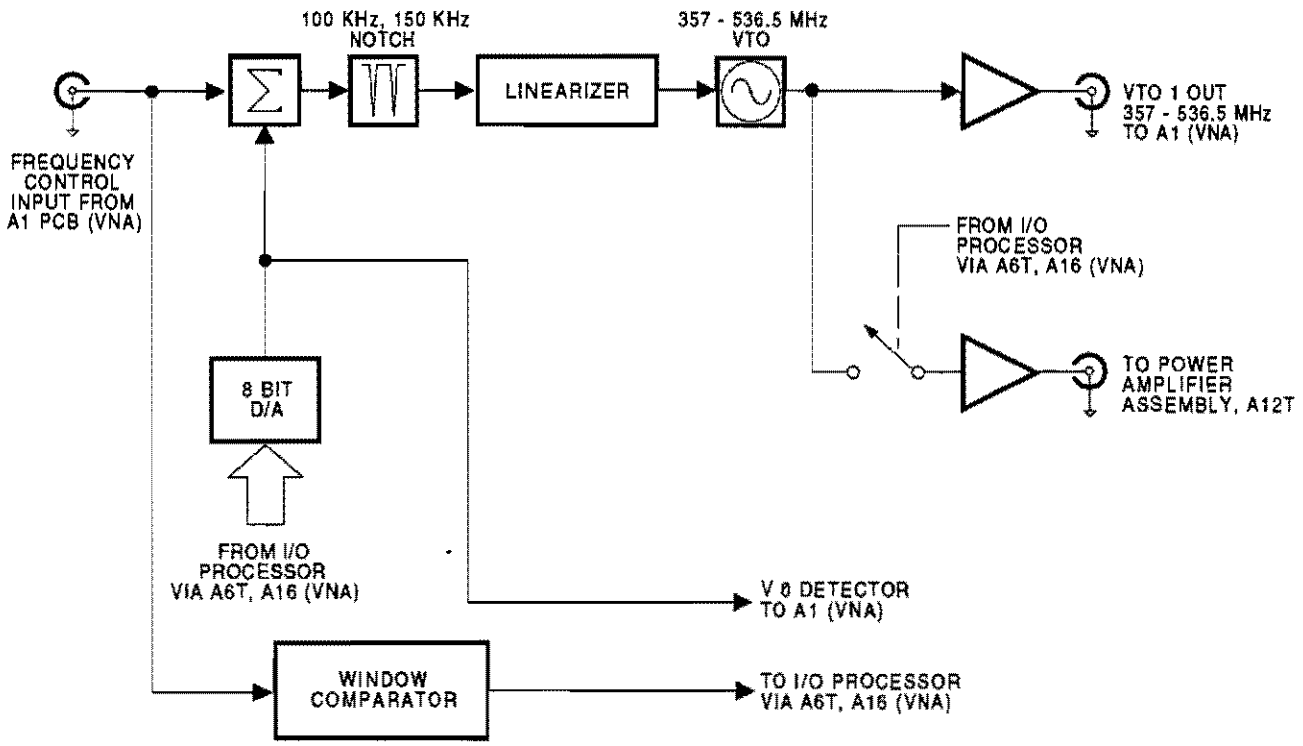


Figure 8-5. A5T LO 1 PCB Block Diagram

8-8 A6T DIGITAL INTERFACE PCB CIRCUIT DESCRIPTION

The A6T Digital Interface PCB (Figure 8-6) provides digital interface between the VNA and test set. The A6T circuitry consists of a bi-directional bus transceiver, latches, buffers, strobe decode logic, three-to-eight decoders, and power filtering and regulation circuits.

The address and data bus connects the test set to the VNA's A16 Test Set I/O PCB. Upon receiving a strobe pulse from the VNA, the strobe decode logic circuit enables the input latch to latch in first the address byte and then the data byte. This enables the decoders to read the address data and select the appropriate device.

The bus transceiver is a bi-directional interface for the input data going to and output data coming from the test set circuits. When bit 7 of the address data byte is set high, the change in logic level of the bus transceiver direction input (DIR) reverses the direction of the data bus. If the data byte is to be written to the test set, the 3-to-8 decoder enables the appropriate latch. If the data byte is coming from the test set and going to the VNA, the 3-to-8 decoder enables the appropriate buffer.

The power regulation and filtering circuitry regulates and filters the +8 Vdc, –18 Vdc, and +18 Vdc from the VNA, producing the +5 Vdc to power the A6T PCB and the +15 Vdc and –15 Vdc to power the A8T, A10T, and A12T RF modules.

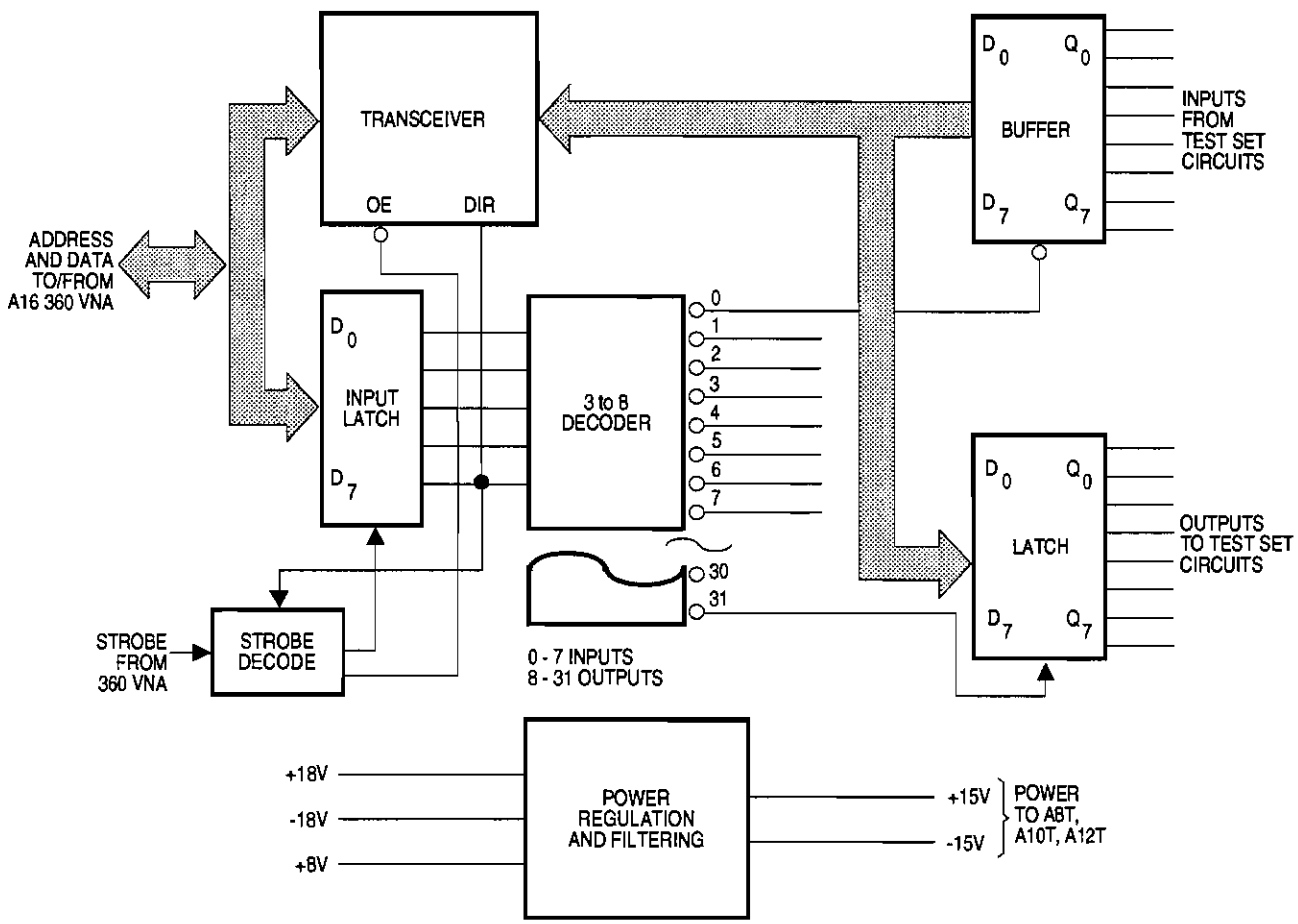


Figure 8-6. *A6T Digital Interface PCB Block Diagram*

8-9 A23T MOTHERBOARD PCB CIRCUIT DESCRIPTION

The A23T Motherboard PCB contains no active devices. It electrically connects the circuits within the test set. It also provides electrical interface to the VNA through the rear panel SIGNAL and CONTROL connectors.

Additionally, the A23T PCB holds the connectors that are the physical interface to the PCB assemblies of the test set.

8-10 A24T SOURCE LOCK/REFERENCE SELECT ASSEMBLY CIRCUIT DESCRIPTION

The A24T Source Lock/Reference Select assembly, also referred to as the LRL Module, contains a source lock reference circuit and a series of FET switches that provide selection of the source of the second IF signal for the A2T Reference Channel IF Amplifier, the A3T Channel A IF Amplifier, and the VNA source lock circuitry. The switches are controlled by the VNA via the A6T Digital Interface PCB. The second IF signal source selections are:

- A2T Reference Channel IF Amplifier – R_A or R_B
- A3T Channel A IF Amplifier – T_A or R_A
- VNA Source Lock – R_A for forward measurements, R_B for reverse measurements

The R_A or R_B signal entering the source lock reference circuit is buffered and passes through a 3 MHz low-pass filter where undesirable frequencies are filtered out. The signal is sampled by a level detector to determine if it is of sufficient amplitude to achieve a phase lock. The VNA's I/O processor monitors the level detector output (via the A6T Digital Interface PCB) to help in determining the cause of a lock failure should one occur.

The signal output from the 3 MHz low-pass filter also goes to a limiter that keeps it within a specified tolerance level. It then passes through a 2.25 MHz bandpass filter to select only the desired 2.25 MHz second IF signal. The signal output from the filter is buffered and sent to the VNA's A6 PCB where it becomes the source lock reference frequency.

8-11 RF DECK ASSEMBLY DESCRIPTIONS

The following paragraphs provide functional descriptions for each of the RF components/assemblies that make up a typical RF Deck assembly. Refer to Figure 8-1 while reading the following descriptions.

A8T/A9T and A10T/A11T Buffer Amplifier/ Sampler Assemblies

A buffer amplifier/sampler assembly consists of a buffer amplifier assembly and a sampler assembly grouped as a single unit. the buffer amplifier/ sampler assembly has a single WILTRON part number and is always replaced as a single unit. The part number and serial number are found on the buffer amplifier.

The A8T/A9T Channel B Buffer Amplifier/Sampler and the A10T/A11T Channel A Buffer Amplifier/ Sampler assemblies provide down conversion of the 40 MHz to 60 GHz RF signals to the second IF of 2.25 MHz.

A9T and A11T are dual sampler assemblies. Each samples two channels. A9T samples Test Channel B (T_B) and Reference Channel B (R_B) and A11T sample Test Channel A (T_A) and Reference Channel A (R_A). The dual sampler assemblies consist of electronically controlled switch circuits.

For frequencies in the range of 40 MHz to 40 GHz, bias voltage to control the sampler switches is received from the A6T Digital Interface PCB via the buffer amplifier assembly. For frequencies above 40 GHz, bias voltage is received from the A27T Amplifier/Switch Driver PCB via the buffer amplifier assembly.

When the test set is operating in the direct mode (40 MHz to 270 MHz), the sampler switches are biased to close, which passes the input RF signal directly to the buffer amplifier assembly. When the test set is operating in the heterodyne mode (270 MHz to 40 GHz), the sampler switches are self-biasing. They switch at the rate of the first local oscillator frequencies.

This sampler switching action causes a mixing (heterodyning) of the first local oscillator frequencies and the input RF signal. One of the signals that results from this heterodyning is the 89 MHz first IF. This signal goes to the buffer amplifier assembly. When the test set is in the heterodyne mode above 50 GHz, the sampler-switch-bias voltage is factory adjusted to enhance sampler performance.

A8T and A10T are dual-buffer-amplifier assemblies. Each down-converts two channels to second IF signals. A8T down-converts Test Channel B (T_B) and Reference Channel B (R_B) and A10T down-converts Test Channel A (T_A) and Reference Channel A (R_A). The buffer amplifier assemblies provide 0 dB conversion gain (RF in to 2nd IF out). The buffer amplifiers have slopes which result in a conversion gain of –10 dB at high frequencies (approximately 40 GHz).

The direct mode (40 MHz to 270 MHz) or heterodyne mode (first IF of 89 ±4 MHz) signal inputs to the buffer amplifier go to mixer circuit. In this circuit, they mix with the second local oscillator signal to produce the desired second IF of 2.25 MHz.

The second IF signal passes through a low-pass filter to eliminate unwanted frequencies. It then goes to a buffer amplifier for output. The T_A, R_A, and R_B second IF signal outputs go to the A24T Source Lock/Reference Select Assembly, and the T_B second IF output goes to the A1T Channel B IF Amplifier PCB.

A12T Power Amplifier Assembly

The A12T Power Amplifier assembly contains the 500 MHz power amplifier and harmonic generator. The power amplifier amplifies the first local oscillator signal to achieve adequate power levels to drive the harmonic generator.

When the test set is operating in the direct mode, the VNA sends a signal to the A6T Digital Interface PCB. This signal disables A12T by removing the +15V power. When the test set is operating in the heterodyne mode, the power amplifier amplifies the first local oscillator signal. This signal causes the harmonic generator to produce harmonic pulses that are necessary for heterodyning to take place in samplers A9T and A11T.

A16T Power Divider Assembly

The A16T Three-Way Power Divider assembly receives the calibration (83⅓ kHz) third local oscillator (2⅓ MHz) signal from the VNA A3 PCB and divides it between three paths of equal impedance: A1T, A2T, and A3T. This enables the same oscillator (LO 3) to drive all three mixer circuits with equal amplitude and minimum loss.

A17T Control Output Mounting Bracket

The A17T assembly is the control output mounting bracket. This mechanical assembly has three connectors for the external connection of WILTRON components (two step attenuators and a transfer switch).

A21T 0–70 dB Step Attenuator Assembly

The A21T 0–70 dB Step Attenuator assembly consists of three attenuator pads. These pads produce attenuation to 40 dB, 20 dB, and 10 dB. Any combination of these three attenuators can be switched-in through digitally selected solenoid switches.

A25T RF Splitter Assembly

The A25T RF Splitter assembly splits the harmonic generator output signal from the A12T Power Amplifier assembly into two paths of equal impedance. The two paths supply signals that are rich in harmonics to the A9T and A11T Samplers for heterodyning.

Chapter 9
3635B Test Set Information

Table of Contents

Chapter 9
3635B Test Set Information

9-1 INTRODUCTION

This chapter describes the 3635B Test Set and the Models 3640X-B and 3641X-B mm-Wave Modules, which comprise the test set portion of a mm-Wave VNA System. This material provides overall functional description, mainframe PCB descriptions, and RF deck assembly descriptions.

9-2 mm-WAVE VNA SYSTEM CONFIGURATION

Figure 9-2 shows a functional block diagram of the WILTRON mm-wave VNA system. This configuration includes instrumentation functions from each of the three basic building blocks of a VNA system:

- Signal Sources:
  Model 360SS47 System Source (or 6647B or 6747B) (LO input)
  Model 6729B Swept Frequency Synthesizer (RF input)

- Test Set: Model 3635B mm-Wave Test Set with:
  one Model 3640B(Q, U, V, or W) mm-Wave Module for Port 1 and either a second 3640B module, or a 3641B (Q, U, V, or W) mm-Wave module for Port 2.

- Vector Network Analyzer:
  Model 360B VNA

- 360ACM Auxilary Control Module
  The mm-Wave VNA system requires an auxiliary control panel (not shown on diagram) to supply it with operating voltages. This instrument mounts in the 360C3 console. Appendix B provides installation and maintenance information.

9-3 FUNCTIONAL DESCRIPTION

The mm-wave VNA system requires two signal source (Figure 9-2, page 9-7). They provide LO and RF signals to the mm-wave modules. The 33 GHz to 110 GHz signals applied to the DUT are down-converted within the modules to a 270 MHz IF signal. Figure 9-3, page 9-8, shows assembly locations.

The VNA controls the two signal sources through the dedicated Source Control System IEEE-488 bus (GPIB). Do not confuse this with the other rear panel VNA GPIB connection which is used with an external controller. In the mm-wave VNA system configuration, as shipped from

the factory, the 360SS47 (test set LO IN) is set to GPIB address 5. The 6729B (test set RF IN) is set to GPIB address 4.

The signal sources provide clean, phase-locked test signals at programmed frequency points for precise test data. The frequency range of the sources determine the frequency range of the VNA. Frequency accuracy of the sources is an important factor in the accuracy of VNA measurements — especially phase accuracy.

The mm-wave VNA system phase-locking scheme is unique among the WILTRON VNA family. The system multiple phase-lock loops provide a stable set of four 2.25 MHz IF frequencies. The primary frequency reference for the system is the internal 10 MHz reference in the Model 6729B Swept Frequency Synthesizer; no frequency reference external to the VNA system is required. The second and third local oscillators are referenced to the VNA 10 MHz Reference — a very stable time base.

Overall system phase lock is maintained by controlling the 360SS47 via its rear panel PHASE LOCK INPUT. Comparison of one of the 2.25 MHz IF signals to the VNA 10 MHz reference provides the correction signal necessary to readjust the 360SS47 frequency. In this manner, all four 2.25 MHz IF signals remain stable.

Because the LO 2 and LO 3 signal outputs are shared by all channels—and because they both use the VNA 10 MHz reference — any noise or phase errors in the respective LO will be canceled out in the channel comparison circuits that follow in the VNA.

Any failure in the VNA phase-lock scheme will be sensed by one of the many Lock Detect circuits. A flag will then be sent to the VNA microprocessor circuits and a LOCK FAILURE message will be displayed on the CRT. System phase-lock problems will be much easier to isolate with a clear understanding of the individual phase-lock loop interactions.

System frequency accuracy and resolution are critical concerns in the VNA. These characteristics are directly traceable to the system sources. Frequency accuracy and resolution are two terms that are often misunderstood.

Frequency accuracy is a measure of the deviation, or drift, from the selected frequency. In other words, it is the frequency stability. The 10 MHz time base in the 6729B has less than 1 Hz drift per day for each 1 GHz of frequency.

Frequency resolution is the smallest frequency step increment available for a selected frequency. The 360SS47 resolution is 100 kHz. The 6729B resolution is 1 kHz. However, because the 6729B RF Output goes through a frequency multiplier in the mm-wave module — which

is necessary to achieve the very high frequencies required for down-conversion — the 1 kHz resolution is multiplied by the harmonic value (that is, at the nth harmonic, the resolution is n kHz).

9-4 mm-WAVE MODULES DESCRIPTION

The mm-wave modules provide two functions: signal routing and down-conversion. There are two types of modules: 3640B-X Transmission/Reflection Modules and 3641B-X Transmission-only Modules. Each of the modules are available in one of four frequency ranges, denoted by waveguide band as shown in Tables 9-1 and 9-2 (left).

Details of the mm-wave modules are shown in Figure 9-2. Although the modules contain no field-serviceable parts, it is necessary to fully understand their construction and signal flow to deduce and isolate module-related problems.

Figure 9-2 shows two modules in place. To determine the appropriate frequencies applied to the mm-wave modules by the signal sources, refer to Figure 9-1 on the following page.

Table 9-1. *Model 3640B-X Transmission/Reflection Modules*

Model	Frequency Range (GHz)	Waveguide Flange
3640B-Q	33 to 50	WR-22
3640B-U	40 to 60	WR-19
3640B-V	50 to 75	WR-15
3640B-W	75 to 110	WR-10

Table 9-2. *Model 3641B-X Transmission Modules*

Model	Frequency Range (GHz)	Waveguide Flange
3641B-Q	33 to 50	WR-22
3641B-U	40 to 60	WR-19
3641B-V	50 to 75	WR-15
3641B-W	75 to 110	WR-10

The correct combination of LO and RF inputs to the mm-wave modules will produce the proper 270 MHz IF output to the test set input buffer amplifiers. To accomplish this, the 6729B Swept Frequency Synthesizer RF Output is tuned to a frequency such that a predictable harmonic output from the module's Frequency Multiplier circuit will cause a resulting DUT stimulus frequency that is exactly 270 MHz away from a predictable harmonic of the 360SS47 System Source (multiplication of the 360SS47 LO IN signal takes place within the mixer).

The following formulas apply to each band (all values are expressed in GHz). Example values relative to the beginning and end of band are given to the right of each formula.

Signal Source Formula	Signal Source Frequency Range
Q Band (33 to 50 GHz Measurement Frequency Range), where F = Desired Measurement Frequency	
LO IN (360SS47) = 1/4 (F+0.27)	8.3175 to 12.5675 GHz
RF IN (6729B) = 1/3F	11 to 16.333 GHz
U Band (40 to 60 GHz Measurement Frequency Range), where F = Desired Measurement Frequency	
LO IN (360SS47) = 1/4 (F–0.27)	10.0675 to 15.0675 GHz
RF IN (6729B) = 1/3F	13.333 to 20 GHz
V Band (50 to 75 GHz Measurement Frequency Range), where F = Desired Measurement Frequency	
LO IN (360SS47) = 1/5 (F–0.27)	10.054 to 15.054 GHz
RF IN (6729B) = 1/4F	12.5 to 18.75 GHz
W Band (75 to 110 GHz Measurement Frequency Range), where F = Desired Measurement Frequency	
LO IN (360SS47) = 1/8 (F+0.27)	9.40875 to 13.78375 GHz
RF IN (6729B) = 1/6F	12.5 to 18.333 GHz

To determine the actual values of the sources for any specific measurement frequency value, apply the appropriate Signal Source Formulas.

For example, to determine the signal source frequency values for a V band system measurement at 66.0 GHz:

LO IN (360SS47) = 1/5 (F–0.27) = 1/5 (66.0–0.27) = 0.2 x 65.73 = 13.146 GHz
RF IN (6729B) = 1/4F = 1/4 x 66.0 = 16.5 GHz

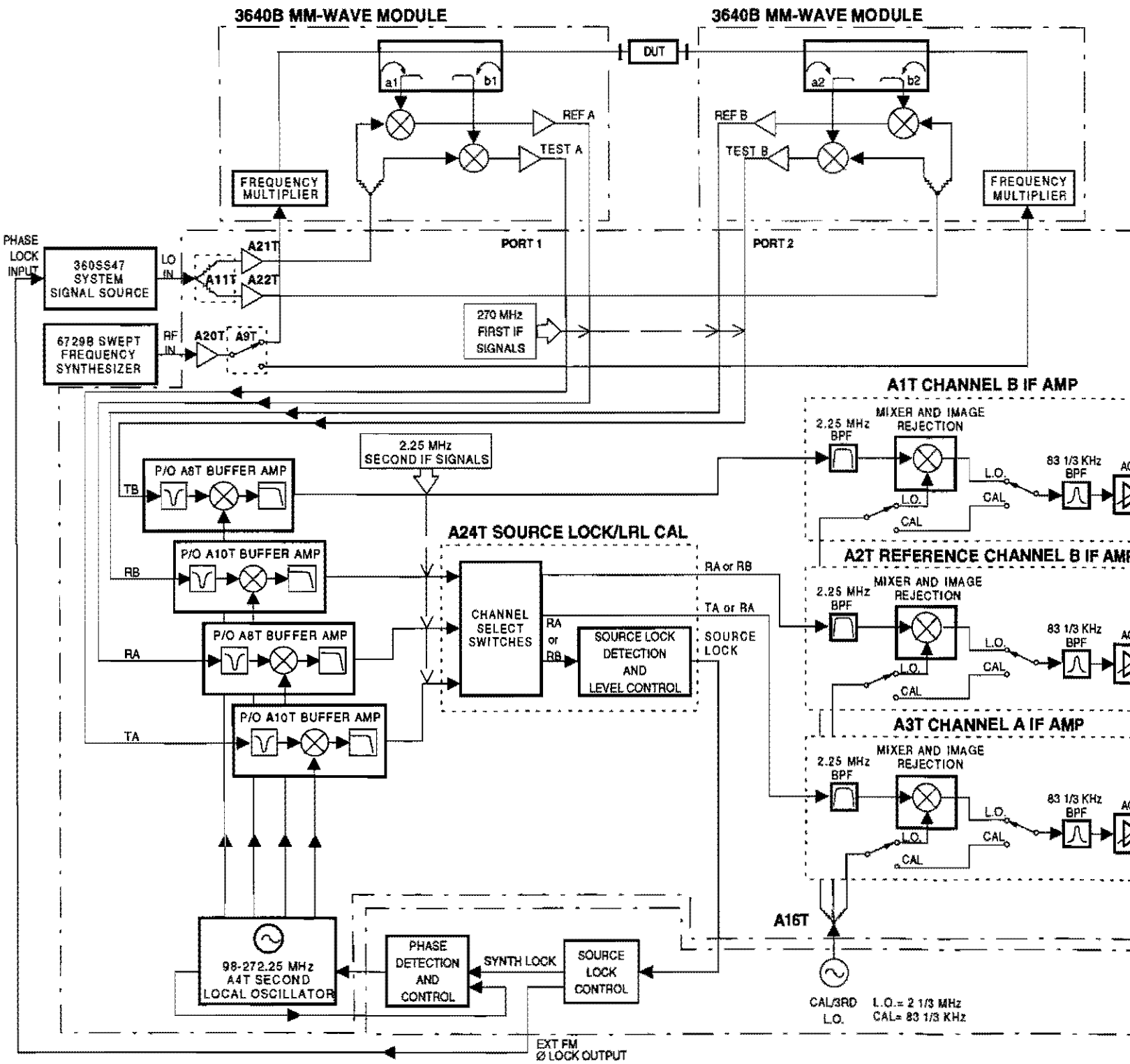
Following this through the mm-wave frequency multiplier and mixer circuits,

The LO IN (360SS47) output is multiplied 5 times:13.146 GHz x 5 = 65.730 GHz

The RF IN (6729B) output is multiplied 4 times:16.5 GHz x 4 = 66.0 GHz

Notice that the resulting difference between the LO IN and RF IN frequencies is 270 MHz, the first IF value.

Figure 9-1. *mm-Wave Module Frequency Determination*


3640B MM-WAVE MODULE
3640B MM-WAVE MODULE
DUT
a1
b1
a2
b2
REF A
TEST A
REF B
TEST B
FREQUENCY MULTIPLIER
FREQUENCY MULTIPLIER
PORT 1
PORT 2
PHASE LOCK INPUT
360SS47 SYSTEM SIGNAL SOURCE
LO IN
A21T
A11T
A22T
67298 SWEPT FREQUENCY SYNTHESIZER
RF IN
A20T
A9T
270 MHz FIRST IF SIGNALS
A1T CHANNEL B IF AMP
2.25 MHz SECOND IF SIGNALS
P/O A8T BUFFER AMP
TB
MIXER AND IMAGE REJECTION
2.25 MHz BPF
83 1/3 KHz BPF
L.O.
CAL
P/O A10T BUFFER AMP
RB
A24T SOURCE LOCK/LRL CAL
RA or RB
TA or RA
P/O A8T BUFFER AMP
RA
CHANNEL SELECT SWITCHES
RA or RB
SOURCE LOCK DETECTION AND LEVEL CONTROL
SOURCE LOCK
A2T REFERENCE CHANNEL B IF AMP
P/O A10T BUFFER AMP
TA
A3T CHANNEL A IF AMP
A16T
98-272.25 MHz A4T SECOND LOCAL OSCILLATOR
PHASE DETECTION AND CONTROL
SYNTH LOCK
SOURCE LOCK CONTROL
CAL/3RD L.O.
L.O.= 2 1/3 MHz
CAL= 83 1/3 KHz
EXT FM
Ø LOCK OUTPUT

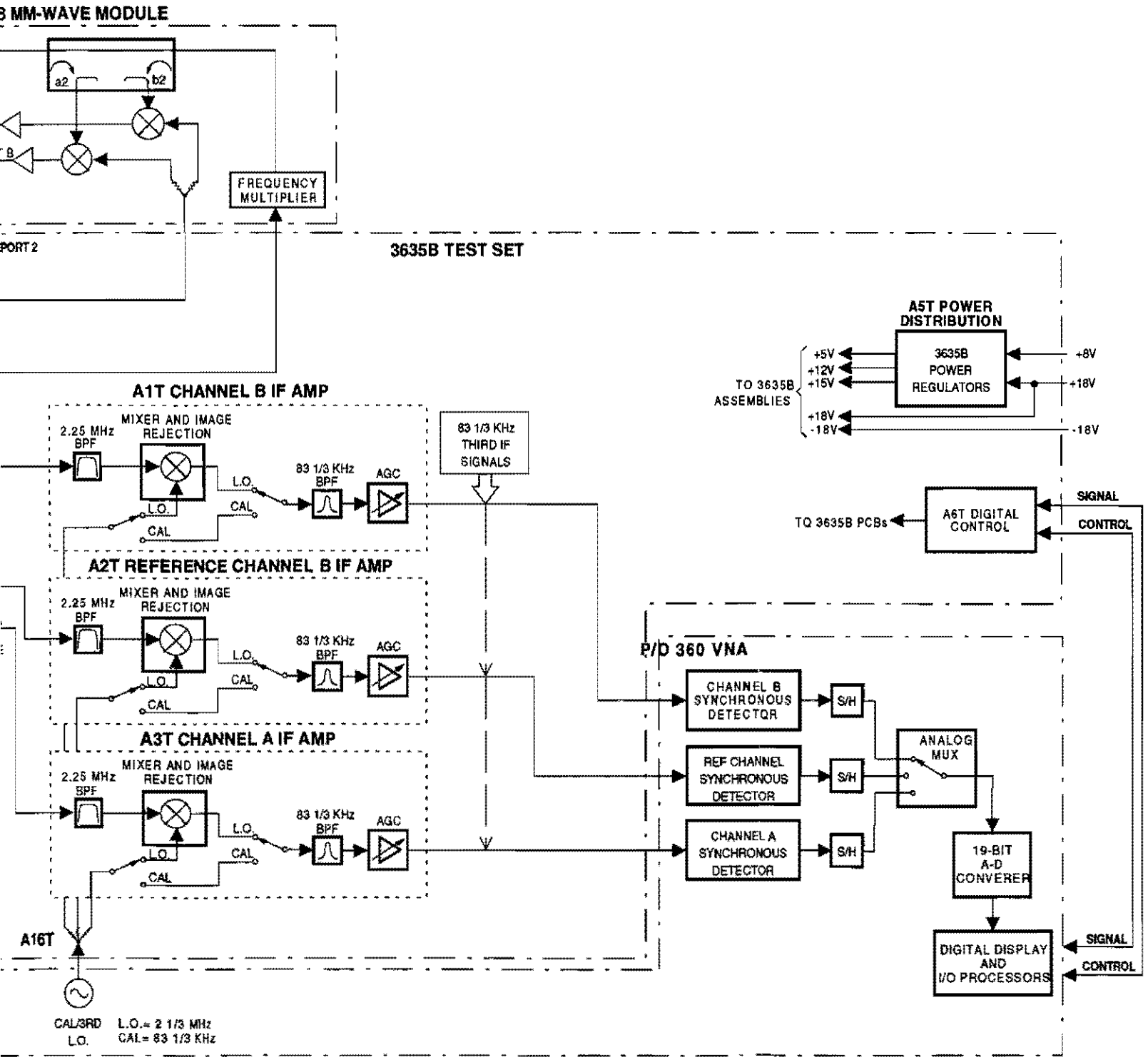


Figure 9-2. *mm-Wave VNA System Block Diagra*

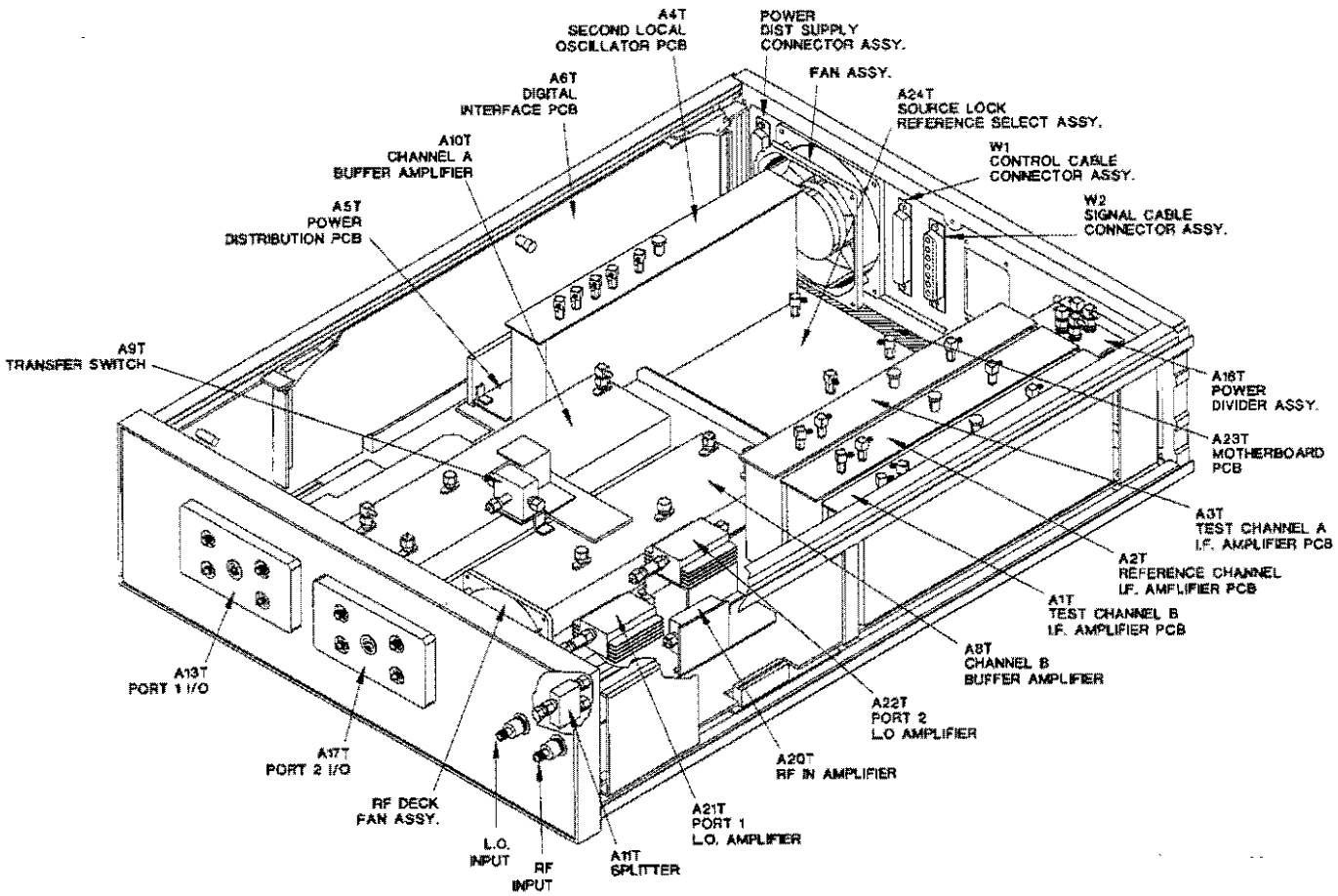


Figure 9-1. *Model 3635B Asssembly Locations*

9-4 A1T, A2T, and A3T CHANNEL IF AMPLIFIER PCB CIRCUIT DESCRIPTION

The A1T, A2T, and A3T Channel IF Amplifier assemblies (Figure 9-4) are functionally equivalent. The A1T and A3T PCBs are mechanically identical; only the PCB cover plates are different. The A2T PCB has a different component layout and card-edge connector pin configuration. The following functional description applies to all three.

The Channel IF Amplifier PCBs have two modes of operation: measurement (LO) and calibration (CAL). In the measurement mode, the 2.25 MHz second IF signal input goes via a buffer amplifier to a 2.25 MHz bandpass filter that removes harmonics and other unnecessary signals. The output from the filter is split into two separate signal paths. The signals are then phase-shifted; one signal by +45° and the other by –45°. Each of the phase-shifted signals is mixed with a 2⅓ MHz third local oscillator signal received from the VNA.

One of the frequencies produced in each mixer is 83⅓ kHz — the difference of the two frequencies. The two phase-shifted, heterodyned signals are then filtered, phase shifted back to 0°, and summed in an amplifier to reject the image frequency. The output passes through an 83⅓ kHz bandpass filter that rejects all harmonics and subharmonics of the fundamental frequencies. The 83⅓ kHz third IF signal then goes to five gain-ranging amplifiers that have selectable gains of one or four.

The third IF signal output is maintained at an acceptable level through automatic gain control (AGC). The peak detector, at the output of the gain-ranging amplifiers, detects the peak signal level and sends a dc voltage representing this level to the comparator. The comparator determines if the dc voltage is in the necessary range of levels required by the VNA synchronous detectors. The comparator outputs one of three signals:

- L=> 0 dB — overload peak signal level condition
- L=> –12 dB — maximum peak signal level condition
- L=> –24 dB — minimum peak signal level condition.

These signals are sent via the A6T Digital Control PCB to the VNA. Responding to these signals, the VNA sends data through A6T to control the gain ranging amplifiers maintaining the peak signal level between 0 and –24 dB.

Third IF peak signal levels affect the amplifiers as follows:

- When the peak signal level is between 0 and –24 dB, all amplifiers are set to a gain of one.
- When the peak level drops below –24 dB, the first gain-ranging amplifier is set to a gain of four. The gain of the first amplifier remains at four until the signal reaches a peak level above –24 dB.
- If the peak signal drops to a level below –36 dB, the second gain-ranging amplifier is set to a gain of four.
- If the peak signal drops to a level below –48 dB, the third gain-ranging amplifier is set to a gain of four.
- If the peak signal drops to a level below –60 dB, the fourth gain-ranging amplifier is set to a gain of four.
- If the peak signal drops to a level below –72 dB, the fifth gain-ranging amplifier is set to a gain of four.

In this way the third IF signal is incrementally boosted each time the signal level at the peak detector drops 12 dB after the initial –24 dB threshold.

The VNA automatically places the A1T thru A3T Channel IF Amplifiers in the calibration mode every three minutes. In the calibration mode, an 83⅓ kHz signal is received from the VNA and sent directly to the gain-ranging amplifiers. The signal level is then incrementally increased by individually programming each of the gain-ranging amplifiers in succession. The outputs are then measured and compared to expected values. The VNA then trims each of the amplifiers using a software algorithm to achieve optimum accuracy and predictability.

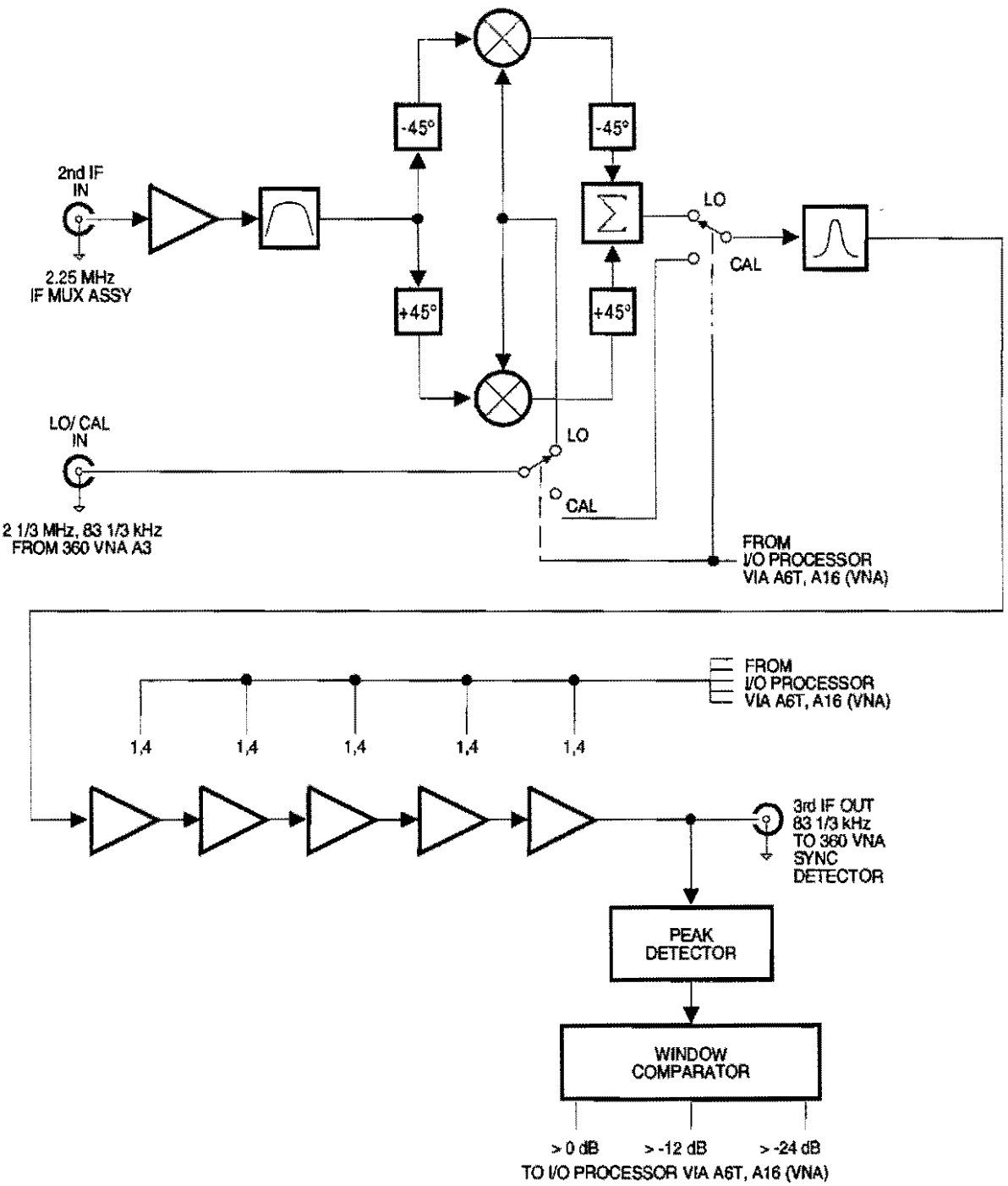


Figure 9-4. *A1T, A2T, and A3T Channel IF Amplifier PCB Block Diagram*

9-5 A4T LO 2 PCB CIRCUIT DESCRIPTION

The A4T LO 2 PCB (Figure 9-5) provides the second local oscillator (LO) signal to the A8T and A10T Buffer Amplifiers. There it mixes with the first IF signal to produce the second IF of 2.25 MHz. The A4T circuitry consists of a loop gain control circuit, a summation amplifier, an 8-bit digital-to-analog converter (DAC), a linearizer, a voltage-tuned oscillator (VTO), a series of divide-by-2 frequency dividers, a window comparator, a frequency range selection circuit, and several buffer amplifiers.

The frequency control input is a variable dc voltage coming from the A2 LO 2 Phase Lock PCB of the VNA. The window comparator determines if the dc voltage has the required levels required for a phase lock. The output of the window comparator sends a status bit to the I/O processor of the VNA for diagnostic purposes.

If the test set signal source is a synthesizer, the VNA's I/O processor — operating through the A6T Digital Interface PCB — changes the attenuation in loop gain control circuit to compensate for loop gain changes each time a different frequency range is selected.

The VNA's I/O processor pre-tunes the VTO by sending a byte to the 8-bit DAC via the A6T Digital Interface PCB. The output of the DAC is summed with the frequency control input in the summation amplifier. The DAC output coarse tunes the VTO frequency output. The frequency control input fine tunes the frequency output.

The output of the summation amplifier is linearized to compensate for nonlinearities in the VTO. The output of the VTO is a 98 MHz to 272.25 MHz signal. One output is buffered and sent to the VNA's A2 LO 2 Phase Lock PCB. The other output is sent to a series of divide-by-2 frequency dividers.

Depending on selection, the frequency range selection circuit sends the VTO output signal directly to the output buffer amplifiers or through any of the frequency dividers before being sent to the output buffer amplifiers. The buffer amplifier outputs are the second local oscillator frequencies and have a frequency range from 12.25 MHz (divide by 8) to 272.25 MHz (divide by 1).

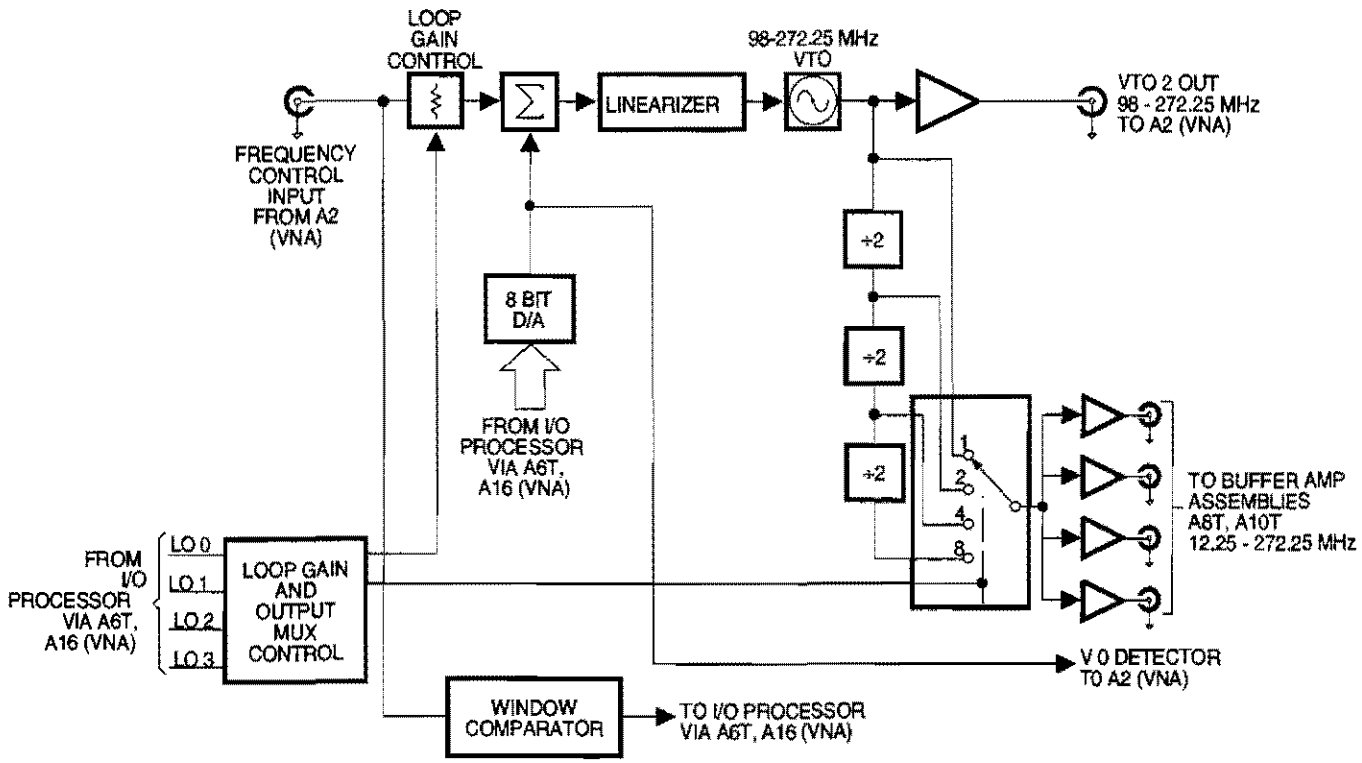


Figure 9-5. *A4T LO 2 PCB Block Diagram*

9-6 A5T POWER DISTRIBUTION PCB CIRCUIT DESCRIPTION

The A5T Power Distribution PCB filters and regulates the raw voltages received from the 360B VNA and distributes them throughout the test set.

9-7 A6T DIGITAL INTERFACE PCB CIRCUIT DESCRIPTION

The A6T Digital Interface PCB (Figure 9-6) provides digital interface between the VNA and test set. The A6T circuitry consists of a bi-directional bus transceiver, latches, buffers, strobe decode logic, three-to-eight decoders, and power filtering and regulation circuits.

The address and data bus connects the test set to the VNA's A16 Test Set I/O PCB. Upon receiving a strobe pulse from the VNA, the strobe decode logic circuit enables the input latch to latch in first the address byte and then the data byte. This enables the decoders to read the address data and select the appropriate device.

The bus transceiver is a bi-directional interface for the input data going to and output data coming from the test set circuits. When bit 7 of the address data byte is set high, the change in logic level of the bus transceiver direction input (DIR) reverses the direction of the data bus. If the data byte is to be written to the test set, the 3-to-8 decoder enables the appropriate latch. If the data byte is coming from the test set and going to the VNA, the 3-to-8 decoder enables the appropriate buffer.

The power regulation and filtering circuitry regulates and filters the +8 Vdc, –18 Vdc, and +18 Vdc from the VNA, producing the +5 Vdc to power the A6T PCB and the +15 Vdc and –15 Vdc to power the A8T, A10T, and A12T PCBs.

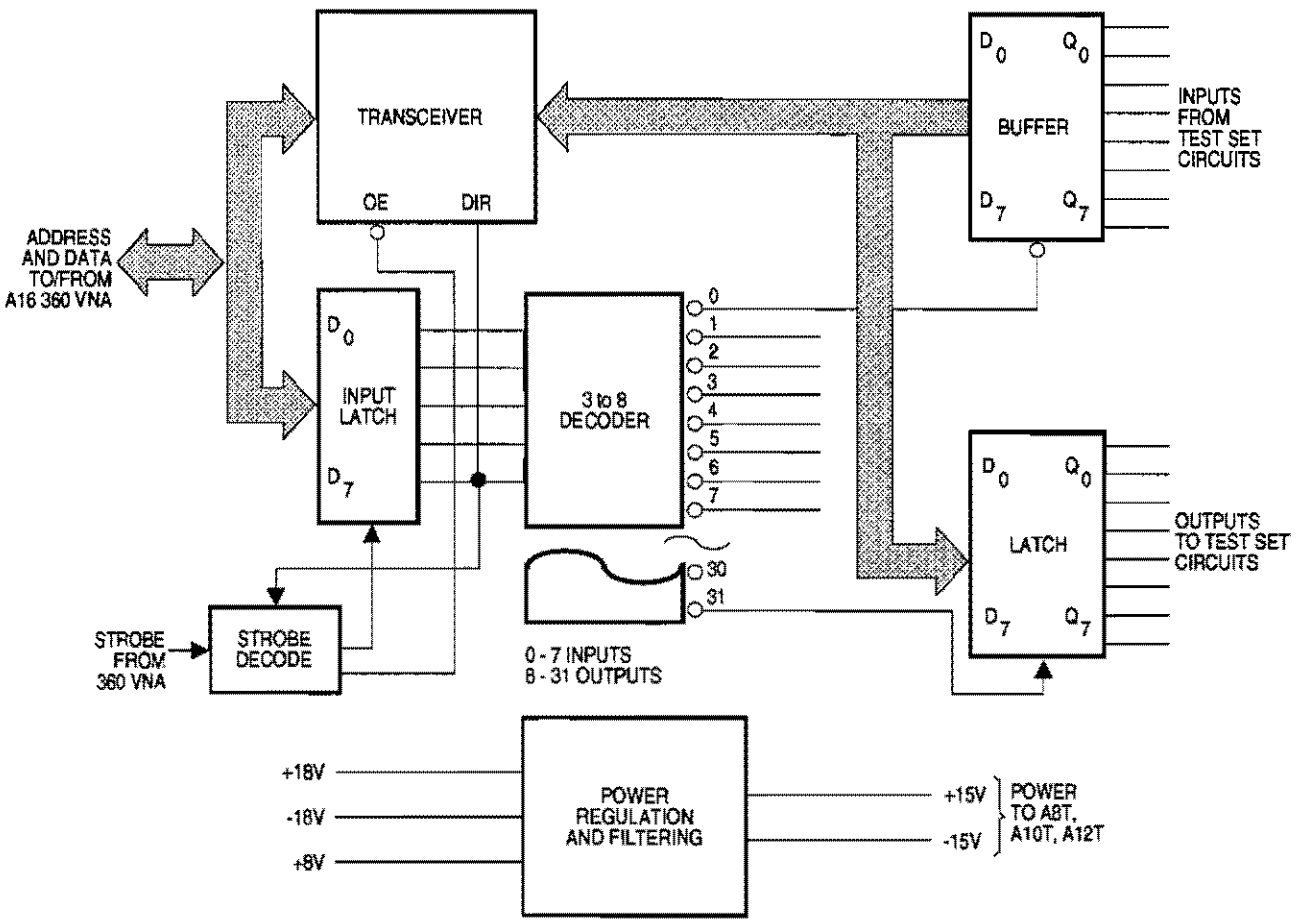


Figure 9-6. *A6T Digital Interface PCB Block Diagram*

9-8 A23T MOTHERBOARD PCB CIRCUIT DESCRIPTION

The A23T Motherboard PCB contains no active devices. It electrically connects the circuits within the test set. It also provides electrical interface to the VNA through the rear panel SIGNAL and CONTROL connectors.

Additionally, the A23T PCB holds the connectors that are the physical interface to the PCB assemblies of the test set.

9-9 A24T SOURCE LOCK/REFERENCE SELECT ASSEMBLY CIRCUIT DESCRIPTION

The A24T Source Lock/Reference Select assembly, also referred to as the LRL Module, contains a source lock reference circuit and a series of FET switches that provide selection of the source of the second IF signal for the A2T Reference Channel IF Amplifier, the A3T Channel A IF Amplifier, and the VNA source lock circuitry. The switches are controlled by the VNA via the A6T Digital Interface PCB. The second IF signal source selections are:

- A2T Reference Channel IF Amplifier – R_A or R_B
- A3T Channel A IF Amplifier – T_A or R_A
- VNA Source Lock – R_A for forward measurements, R_B for reverse measurements

The R_A or R_B signal entering the source lock reference circuit is buffered and passes through a 3 MHz low-pass filter where undesirable frequencies are filtered out. The signal is sampled by a level detector to determine if it is of sufficient amplitude to achieve a phase lock. The VNA's I/O processor monitors the level detector output (via the A6T Digital Interface PCB) to help in determining the cause of a lock failure should one occur.

The signal output from the 3 MHz low-pass filter also goes to a limiter that keeps it within a specified tolerance level. It then passes through a 2.25 MHz bandpass filter to select only the desired 2.25 MHz second IF signal. The signal output from the filter is buffered and sent to the VNA's A6 PCB where it becomes the source lock reference frequency.

9-10 RF DECK ASSEMBLY DESCRIPTIONS

The following paragraphs provide functional descriptions for each of the RF components/assemblies that make up a typical RF Deck assemby. Refer to Figure 9-2 while reading the following descriptions. None of these assemblies have user-serviceable parts; replacement assemblies are available.

A8T and A10T Buffer Amplifier Assemblies — The A8T and A10T PCBs are the Channel B and A Buffer Amplifier assemblies, respectively. They also include mixers that downconvert the 270 MHz first IF to the 2.25 MHz second IF. The assemblies each provide 0 dB conversion gain. Because the first level of down conversion is provided in the mm-wave modules, these assemblies do not have samplers.

A9T Transfer Switch Microcircuit — The A9T Transfer Switch routes the RF Output of the 6729B Swept Frequency Synthesizer to the mm-wave module(s) attached to PORT 1 or PORT 2. It operates directly under control from the 360B VNA control circuits via the test set A6T Digital Interface. This signal serves as the RF stimulus for the DUT.

A11T Power Splitter Microcircuit — The A11T Power Splitter routes the 360SS47 System Signal Source RF Output to both PORT 1 and PORT 2. This signal serves as the local oscillator stimulus for the mixers in the mm-wave modules.

A16T Power Splitter Microcircuit — The A16T Power Splitter receives the 3rd Local Oscillator/ Cal signal from the 360B VNA A3 PCB and routes three similar signals to the A1T, A2T, and A3T IF Amplifiers.

A20T RF IN Power Amplifier Microcircuit — The A20T amplifies the RF IN signal from the 6729B Swept Frequency Synthesizer for application to the DUT (through the A9T Transfer Switch and the mm-wave modules).

A21T PORT 1 LO Power Amplifier Microcircuit — The A21T amplifies the RF IN signal from the 360SS47 System Signal Source for application to the PORT 1 mm-wave module's mixers. This unit is identical to the A22T Amplifier.

A22T PORT 2 LO Power Amplifier Microcircuit — The A22T amplifies the RF IN signal from the 360SS47 System Signal Source for application to the PORT 2 mm-wave module's mixers. This unit is identical to the A21T Amplifier.

Chapter 10
360SSXX Signal Source Information

Table of Contents

Chapter 10
360SSXX Signal Source Information

10-1 INTRODUCTION

This chapter describes the 360SS47 and 360SS69 Signal Sources. It also provides functional descriptions for major assemblies and confidence tests, calibration, and remove and replace procedures.

10-2 REPLACEABLE SUBASSEMBLIES

WILTRON maintains a module exchange program for selected signal source modules. If a malfunction occurs in one of these modules, it can be exchanged. Upon request and typically within 24 hours, WILTRON or a Wiltron/Anritsu Service Center will ship an exchange module. The customer has 30 days in which to return the defective item. All exchange parts are warranted for 90 days from the date of shipment or for the balance of the original-part warranty—whichever is longer.

A listing of exchangeable subassemblies is provided in Chapter 1, Table 1-2.

10-3 TROUBLESHOOTING

This paragraph provides four troubleshooting tables designed to lead to the most-likely PCB or assembly causing the indicated malfunction. Table 10-1 provides an overall troubleshooting procedure; Table 10-2, a procedure for troubleshooting the A1 PCB; Table 10-3, a procedure for troubleshooting the A4 PCB, and Table 10-4, a procedure for troubleshooting the A5 thru A9 PCBs.

Table 10-1. *Overall Troubleshooting Procedure (1 of 4)*

Symptom	Procedure
301 LOCK FAILURE —DE	Because of the 360B's phase-lock loop structure, this is the most difficult system failure to troubleshoot. There are at least 30 different circuits or components that can cause this error code. The following are procedures that will help you isolate the fault to the major assembly. 1. Determine whether the failure occurs in both forward (S_{11}, S_{21}) and reverse (S_{22}, S_{12}) measurements. If the problem occurs • at all frequencies in *both* directions, the fault could be in the analyzer, signal source, or test set. Refer to paragraph 4, below, for further isolation tips. • at only certain frequencies in *both* directions, the fault could be in the signal source. Refer to paragraph 3, below, for further isolation tips. • in only *one* direction, the fault could be in the test set. *To check whether the failure occurs in both forward and reverse measurements, proceed as follows:* a. Press the DEFAULT PROGRAM key. b. Press the CHANNEL MENU and select the SINGLE DISPLAY menu option. c. Press the S PARAMS key and select the S12 menu option. d. Allow two sweeps to occur, as indicated by the blue sweeping indicator at the bottom of the display.

Table 10-1. *Overall Troubleshooting Procedure (2 of 4)*

Symptom	Procedure
301 LOCK FAILURE —DE (Continued)	e. Note whether the failure condition is still present. f. Press the S PARAMS key and select the S21 menu option. g. Allow two sweeps to occur. h. Note whether the failure condition is still present. 2. Determine whether the failure occurs across the full sweep or only in portions of the sweep. If the problem occurs • only in certain bands, it is likely in the source. Refer to paragraph 3, below, for troubleshooting tips. • at all frequencies, it could be in the analyzer, test set, or source. Refer to paragraph 4, below, for procedures on how to isolate the problem further. *To check whether the error condition occurs at all frequencies or in only selected bands, proceed as follows:* a. With the system turned on and sweeping, observe the blue sweeping-indicator at the bottom of the display b. If the sweeping-indicator cursor is moving very slowly from the beginning to the end of the sweep, that indicates the problem is at all frequencies. c. If the cursor only moves slowly over some part of the sweep, that indicates the problem is isolated to one or more frequency bands. Paragraph 3 describes how to isolate the problem further. 3. If you have determined that the problem is in the source, the following procedure will help to isolate it to a subassembly. a. Determine the frequency band or bands in which the sweep slows down, as follows:

Table 10-1. *Overall Troubleshooting Procedure (3 of 4)*

Symptom	Procedure
301 LOCK FAILURE —DE (Continued)	(1) Press the MARKER MENU key. When the menu appears, select MARKER 1 to be ON. (2) Using the rotary knob, position the marker to the section of the displayed trace where the sweep starts to slow down. (3) Note the frequency and determine the band. The frequency bands are as follows: (a) Het Band, ≤2 GHz (b) Band 1, 2 GHz to 8 GHz (c) Band 2, 8 to 12.4 GHz (d) Band 3, 12.4 to 18 (20) GHz (e) Band 4, 18 (20) to 27.5 GHz (f) Doubler Band, 27.5 to 40 GHz (4) After determining the frequency band, refer to Table 10-4 for further troubleshooting. 4. Assume that you have determined the error to be occurring at all frequencies. To determine whether the source may be the cause, proceed as follows: a. Perform frequency and power-level verification of the source. Refer to Tables 10-3 and 10-4 b. If the verification shows that the source has no problems with output power or frequency, check that the resistance of the FM coils used with the YIG oscillators are not open or shorted to ground. (You will have to remove the source from the console to make this check.)

Table 10-1. *Overall Troubleshooting Procedure (4 of 4)*

Symptom	Procedure
303 RF OVERLOAD	There is too much microwave power coming from the source—no leveling. Refer to Table 10-3 and perform ALC verification. If the source fails this test, replace the A4 PCB and coupler assembly.
110 SRC ID ERROR	The source fails to return its identification code on power up or self test. Check the following: 1. *System Bus Interconnect Cable.* If the cable is properly connected, it may be defective. 2. *GPIB Ribbon Cable.* In the source, check the ribbon cable that connects the A1 PCB with the rear panel connector. It could be defective. 3. *Source Not Turned On or Power Supply Defective.* Check LED on front panel; verify that it is lit steadily and not flashing. 4. *A1 PCB in Source Defective.* Refer to Table 10-2 for A1 PCB troubleshooting instructions. 5. *A5 PCB in Source Defective.* Refer to Table 10-4 for A5 PCB troubleshooting instructions.
400 GPIB ERROR	The analyzer fails to detect a response from the peripheral from which it has requested action. To determine if the source caused the error message, make the same checks outlined for the error message 110 SRC ID ERROR above. The difference between this message and the 110 message is that 110 occurs only on power-up. Error code 400 occurs at anytime a peripheral fails to respond to a request for service.

Table 10-2. *A1 PCB Troubleshooting Procedure (1 of 1)*

Symptom	Procedure

110 SRC ID ERROR (A1 PCB is suspect, see Table 10-1)	To determine whether the A1 PCB may be the cause of the error message, you will need to use an external controller. Proceed as follows:
	1. With the source installed in the console, remove the SYSTEM BUS interconnection to the analyzer. Connect an external controller to the SYSTEM BUS port.
	2. Type the following HP BASIC commands into the controller: (This example is for an HP85 Controller.)
	`10 OUTPUT 705; "OI"`
	`20 ENTER 705; A$`
	`30 DISP A$`
	`RUN`
	3. The source should return the following message:
	`36XXF.FFFHHHPPWWW —`
	`Example: 36690.01040.000-12`
	Where:
	X = model number—47 or 69.
	F = low frequency value—Example: 0.010
	H = high frequency value—Example: 40.0
	P = high power value—Example: 00
	W = low power value—Example: -12
	4. If the above message is not returned, replace the A1 PCB (paragraph 10-25).

Table 10-3. *A4 PCB Troubleshooting Procedure (1 of 2)*

Symptom	Procedure
303 RF OVERLOAD	To determine whether the A4 PCB or other ALC loop components may be the cause of the error message 1. Use the 360B VNA to program the source for a predetermined frequency. As follows: a. On the source, disconnect the BNC cable from the PHASE LOCK INPUT connector. b. On the VNA, press the SETUP MENU key. c. From the displayed menu, (1) Select CW MODE to be ON and enter a test frequency. *Example:* 2.05 GHz (2) Select REDUCED TEST SIGNALS. (3) Select SOURCE POWER when the next menu appears; then enter a power level. *Example:* +10 dBm. (4) Press the HOLD key. d. With a power meter connected to the RF OUTPUT connector on the source, verify that the measured power is within ±2 dB of the selected power. e. From the menu, select the next power level to be tested (typically a mid-range power level). *Example:* +5 dBm. f. Verify that the measured power level is within ±2 dB of the selected power. g. Repeat steps e and f for the next power level. (Typically, the minimum power level. Example: 0 dBm.) 2. Use an external controller to program the source for a series of power levels, as follows: a. Connect the test equipment as shown in Figure 10-1. I b. On the controller, type the following program: (This example is for an HP85 Controller.)

Table 10-3. *A4 PCB Troubleshooting Procedure (2 of 2)*

Symptom	Procedure
303 RF OVERLOAD (Continued)	10 DISP "SELECT FREQUENCY IN GHZ" 20 INPUT A (midfrequency of the suspect band) 30 OUTPUT 705; "CF1",A,"GHZ" 40 DISP "ENTER POWER LEVEL IN dBm" 50 INPUT P* 60 OUTPUT 705; "LVL",P,"DM" 70 GOTO 40 RUN * Typically, check the suspect band at three power levels: guaranteed power, –5 dB down, and –10 dB down from guaranteed power. c. Verify that the measured frequency is within ±2 dB of the power level entered for the P variable. d. If the power level is not proper, replace the A4 PCB and coupler.

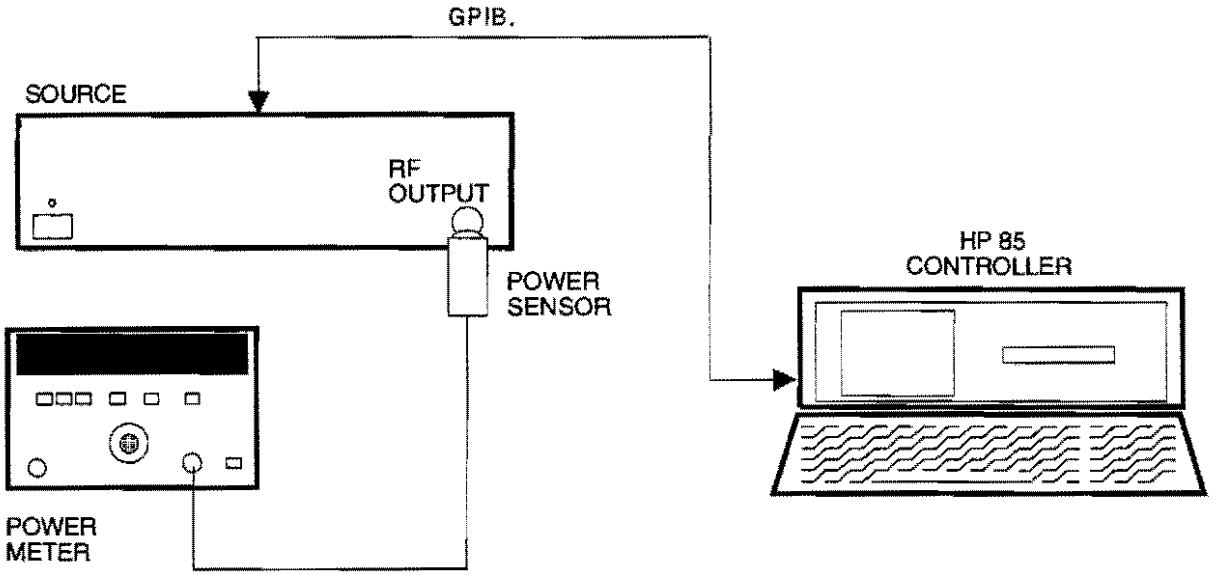


Figure 10-1. *Test Setup for Programming a Series of Power Levels*

Table 10-4. *A5 PCB Troubleshooting Procedure (1 of 1)*

Symptom	Procedure

301 LOCK FAILURE —DE (A5 PCB is suspect, see Table 10-1)	To determine whether the A5 PCB may be the cause of the error message, you have to set the source for a series of CW frequencies then verify that the output frequency is within the tolerance window. You will need to use an external controller. Proceed as follows:
	1. Connect the test equipment as shown in Figure 10-2.
	2. On the controller, type the following program: (This example is for an HP85 Controller.)
	`10 DISP "SELECT FREQUENCY IN GHZ"`
	`20 INPUT A (test frequency [0.01 for 10 MHz])`
	`30 OUTPUT 705; "CF1",A,"GHZ"`
	`30 GOTO 10`
	`RUN`
	3. Verify that the measured frequency is within ±40 MHz of the frequency entered for the A variable.
	4. Repeat steps 2 and 3 for the next test frequency.
	5. If the frequency is off by the same amount in all bands, replace the A5 PCB (paragraph 10-25). However, if the frequency is incorrect in only one band, then replace the applicable YIG Driver PCB (A6-A9), YIG Oscillator and attaching parts, and RF deck mounted transistors for the affected band (Figure 10-25 or 10-26).

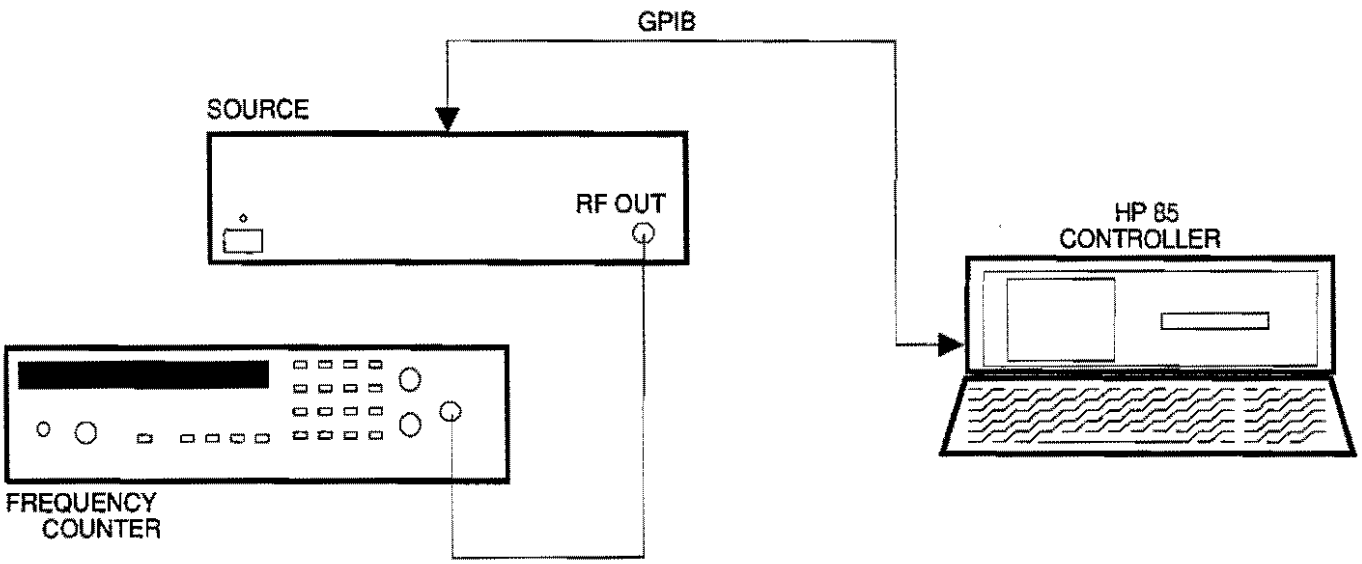


Figure 10-2. *Test Setup for Programming a Series of Frequencies*

10-4 OVERALL CIRCUIT DESCRIPTION

The 360SSXX contains both circuitry that is universal for all models and frequency components that are model dependent (Figures 10-3 and 10-4).

Universal Circuits

A1 GPIB Interface PCB Provides overall control for RF signal generation. It interfaces with the analog circuits via the μP Bus. Paragraph 10-5 describes the A1 PCB.

A4 Automatic Level Control PCB Controls the RF-output-signal leveling loop. The input for this loop is the built-in coupler/ detector, which provides for internal leveling. The loop output device is the PIN switch attenuator current-driver circuits (not shown) located on the A6-A9 YIG Driver PCBs. These current-driver circuits operate the MOD DRIVER 1, 2, 3, and 4 lines used to control Mod and PIN switch attenuation. The A4 also

- Sets the magnitude of the RF output power, which the user selects using the analyzer REDUCE SIGNALS MENU.
- Provides the RF SLOPE correction to the output power signal.

Paragraph 10-6 describes this PCB.

A5 Frequency Instruction PCB Generates center-frequency tuning and bandswitch voltages for the A6-A9 YIG Driver PCBs. The bandswitch-control and center-frequency tuning voltages are both on the FCEN signal. The frequency-tuning DAC (digital-to-analog converter) is selected on A5 and used to control the center frequency. The FREQUENCY VERNIER signal enters A5 via the μP Bus. The linearizing ROM signal enters via the FC Bus (frequency correction bus). Paragraphs 10-7 thru 10-9 describe the A5 PCB and frequency generation circuits.

A10 FM/ Attenuator PCB Provides a tuning current for the YIG Osc 1-4 FM (frequency modulation) coils and the Osc 1 YIG tracking filter. The tracking filter tuning current is derived from the TRACK FILTER 1 voltage generated on the A6 PCB. The FM coil tuning current is derived from the external FM signal. This signal comes from the rear panel, via the EXT FM ØLOCK INPUT connector. Paragraph 10-10 describes the A10 PCB.

A14 Motherboard PCB

Provides an interconnecting plane for the A1 through A10 PCBs. The A14 PCB also intefaces, via connectors, with the A1-A10 PCBs, the rear panel connectors, and RF Deck components. The A14 PCB also contains PIN Switch port drive circuitry and part of the switching power supply circuitry. Paragraph 10-11 describes this PCB.

A13 Switching Power Supply PCB

This PCB, along with the power supply circuits on the A14 PCB, provides power supply voltages for the signal source circuits. Paragraph 10-11 describes the A13/A14 Switching Power Supply.

Model Dependent Circuits—360SS47

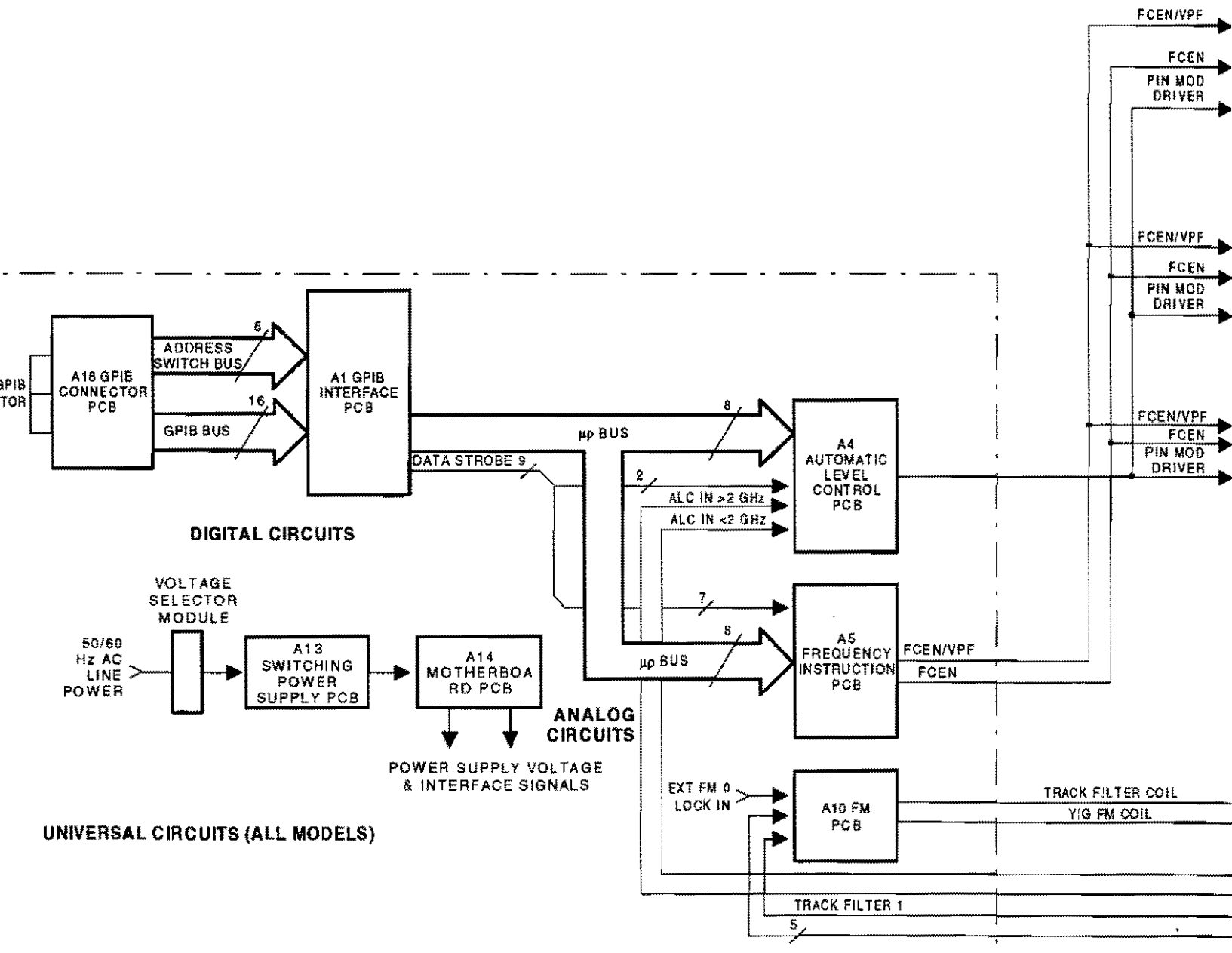
The model-dependent circuits and components for the 360SS47 consist of the A6 YIG Driver PCBs and the components shown on the RF Deck (Figure 10-3). The A6 Het-YIG Driver PCB provides tuning and bias currents for the YIG tuning coil. The tuning current is derived from the **F CEN** signal supplied by the A5 PCB. The oscillator bias current is generated on the A6 PCB. Along with tuning and bias currents, the A6 PCB also generates a tracking filter voltage that it supplies to the A10 PCB. This voltage indirectly provides tuning for the YIG tracking filter that is built into the Osc 1 YIG module. Except for the MOD DRIVER signals previously described, the other A6-A8 outputs are control lines. The SNB and SNR lines are select-next-band and select-next-ROM lines, respectively. When the presently selected oscillator band has reached its upper-most frequency, the SNB line selects the next oscillator band. The HET YIG SEL and YIG 1, 2, and 3 SEL lines go to the A10 PCB.

Paragraph10-9 describes the A6-A8 PCBs.

The RF Deck is a subassembly. It contains all the sweep generator RF components. Paragraph 10-12 describes this subassembly.

Model Dependent Circuits—360SS69

The model-dependent circuits and components for this model are also shown in Figure 10-4. The circuit description is similar to that for the Model 360SS47 described above.


FCEN/VPF
FCEN
PIN MOD DRIVER
FCEN/VPF
FCEN
PIN MOD DRIVER
FCEN/VPF
FCEN
PIN MOD DRIVER
A18 GPIB CONNECTOR PCB
6
ADDRESS SWITCH BUS
16
GPIB BUS
A1 GPIB INTERFACE PCB
8
µp BUS
DATA STROBE 9
2
ALC IN >2 GHz
ALC IN <2 GHz
A4 AUTOMATIC LEVEL CONTROL PCB
DIGITAL CIRCUITS
VOLTAGE SELECTOR MODULE
50/60 Hz AC LINE POWER
A13 SWITCHING POWER SUPPLY PCB
A14 MOTHERBOARD PCB
7
8
µp BUS
A5 FREQUENCY INSTRUCTION PCB
FCEN/VPF
FCEN
ANALOG CIRCUITS
POWER SUPPLY VOLTAGE & INTERFACE SIGNALS
EXT FM 0
LOCK IN
A10 FM PCB
TRACK FILTER COIL
YIG FM COIL
TRACK FILTER 1
5
UNIVERSAL CIRCUITS (ALL MODELS)

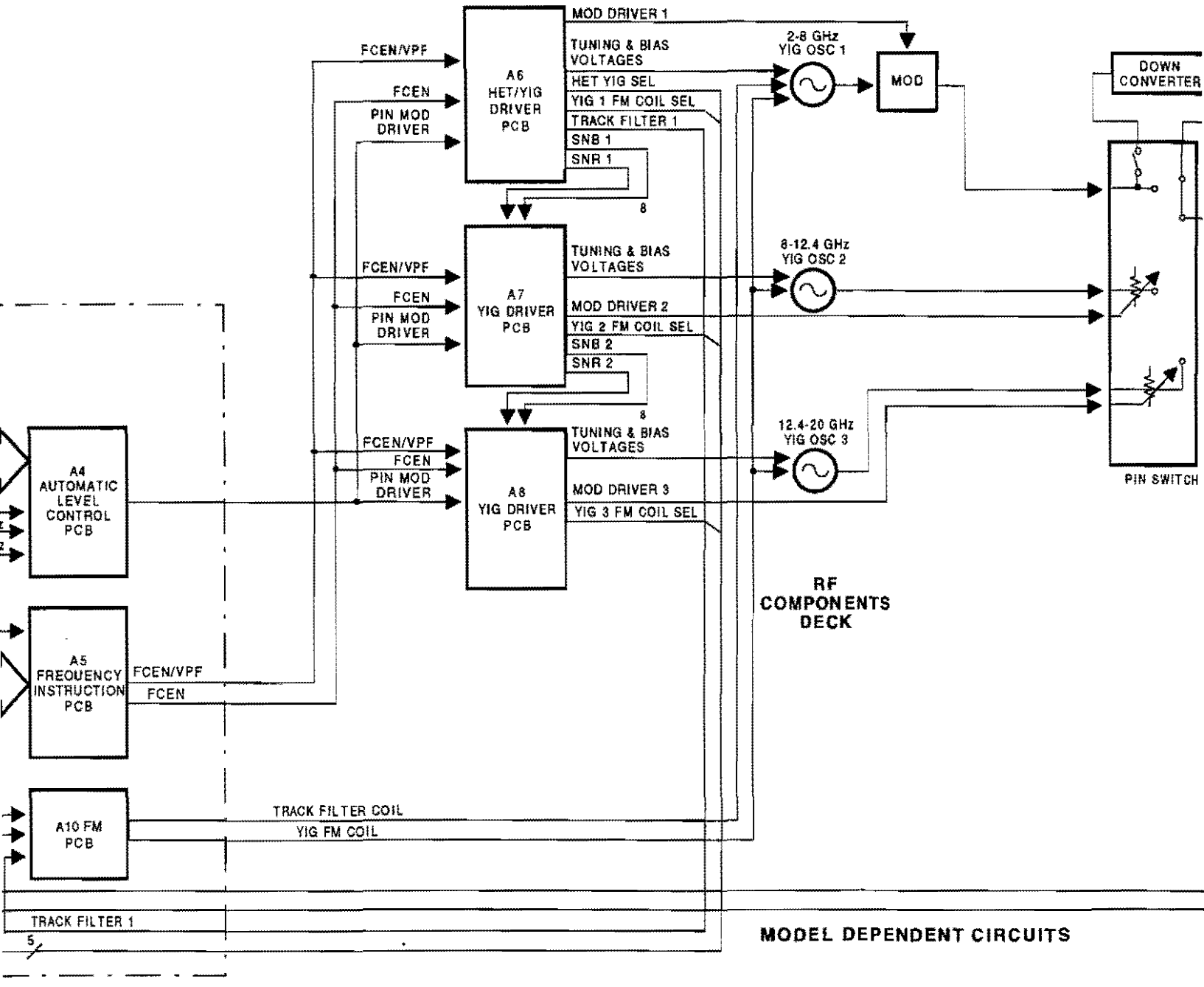
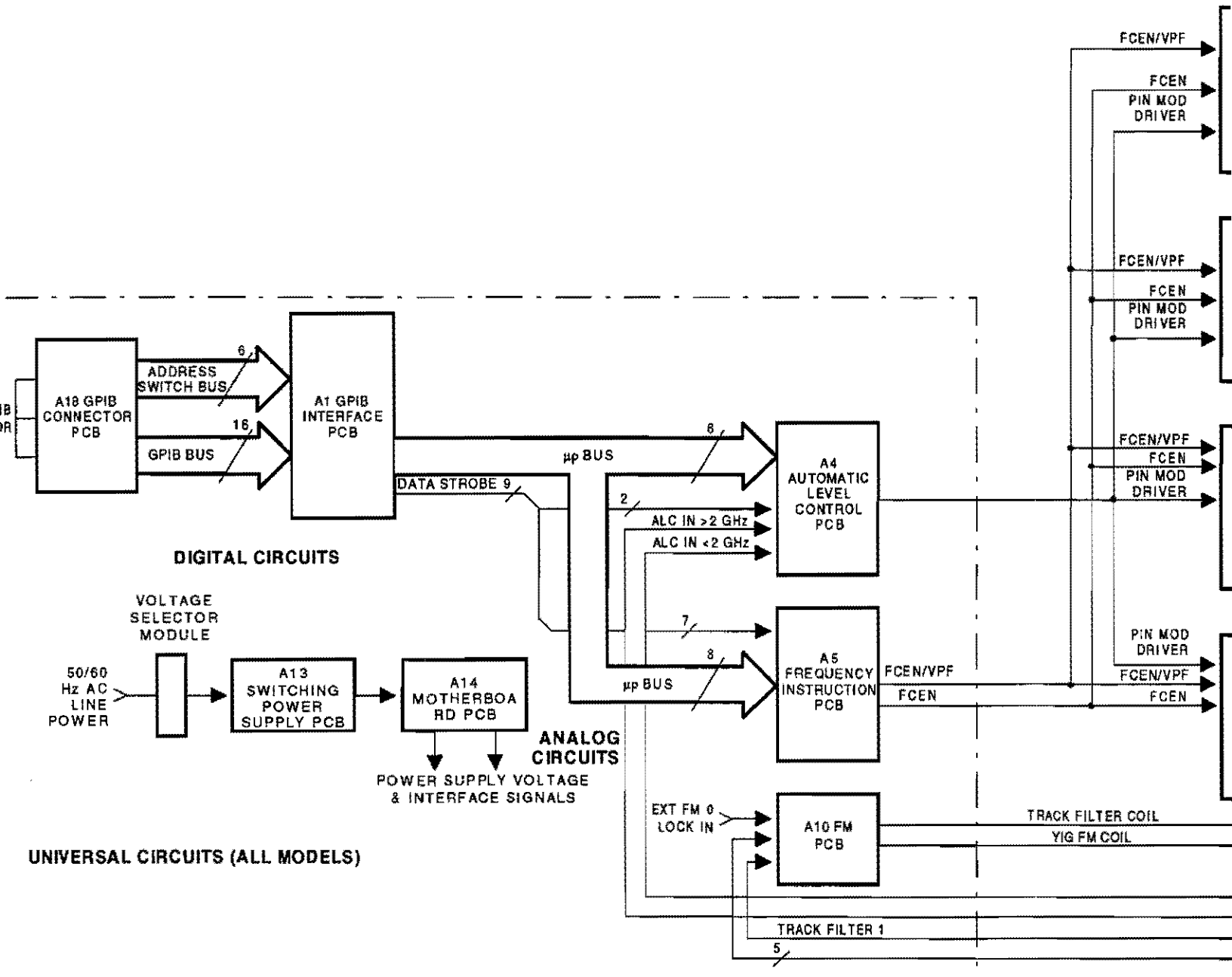


Figure 10-3. Model 360SS45/47 Overa


A18 GPIB CONNECTOR PCB
ADDRESS SWITCH BUS
6
GPIB BUS
16
A1 GPIB INTERFACE PCB
DATA STROBE 9
µp BUS
6
A4 AUTOMATIC LEVEL CONTROL PCB
2
ALC IN >2 GHz
ALC IN <2 GHz
DIGITAL CIRCUITS
VOLTAGE SELECTOR MODULE
50/60 Hz AC LINE POWER
A13 SWITCHING POWER SUPPLY PCB
A14 MOTHERBOARD PCB
POWER SUPPLY VOLTAGE & INTERFACE SIGNALS
ANALOG CIRCUITS
7
8
µp BUS
A5 FREQUENCY INSTRUCTION PCB
FCEN/VPF
FCEN
EXT FM & LOCK IN
A10 FM PCB
TRACK FILTER COIL
YIG FM COIL
TRACK FILTER 1
5
UNIVERSAL CIRCUITS (ALL MODELS)
FCEN/VPF
FCEN
PIN MOD DRIVER
FCEN/VPF
FCEN
PIN MOD DRIVER
FCEN/VPF
FCEN
PIN MOD DRIVER
PIN MOD DRIVER
FCEN/VPF
FCEN

Figur

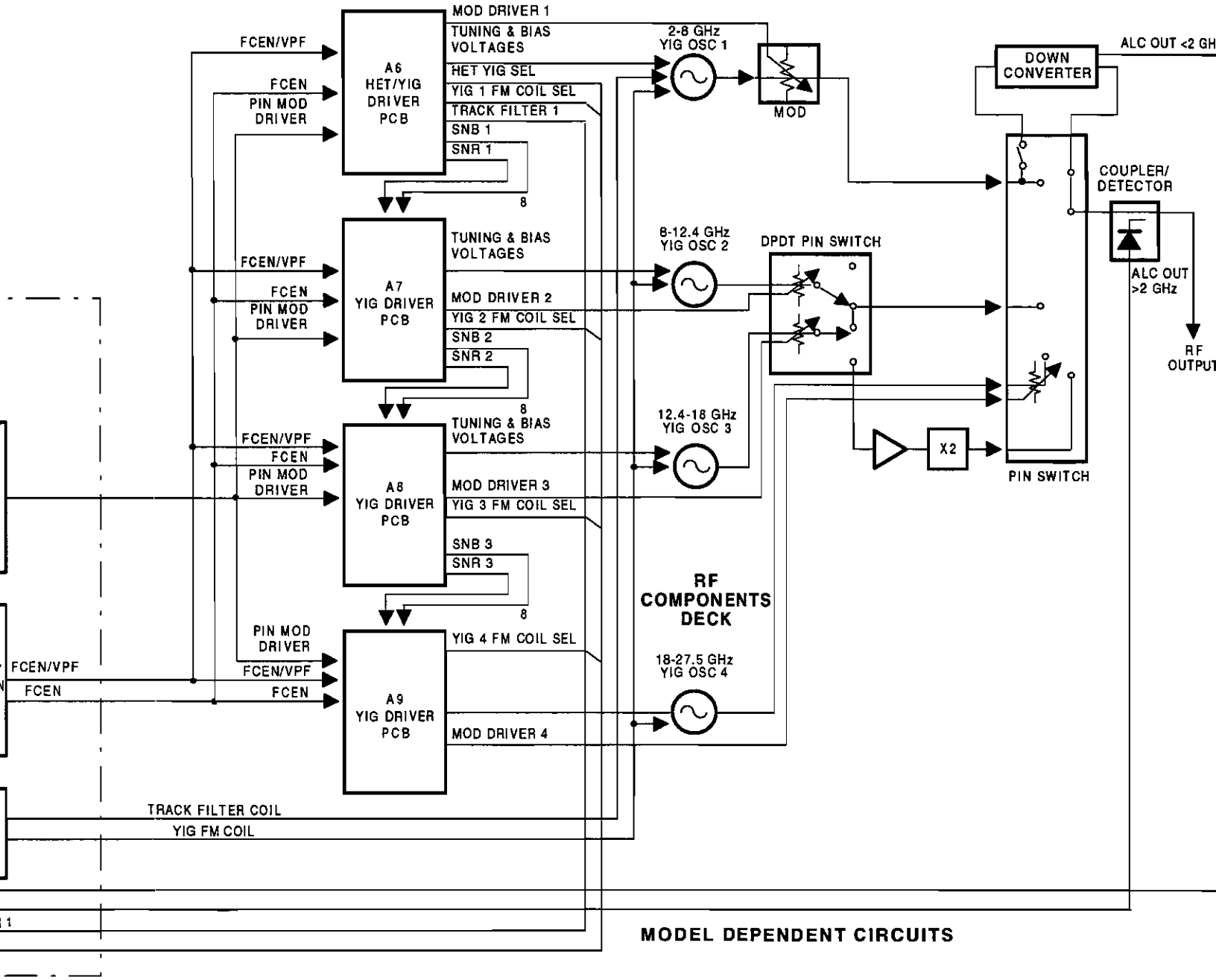


Figure 10-4. *Model 360SS69 Overall Block Diagram*

10-5 GPIB SETUP AND INTERCONNECTION

Automated microwave measurements are provided through the GPIB port. Specific GPIB information — including interface connections, cable requirements, and addressing instructions — is contained in the following paragraphs.

Interface Connector

Interface between the sweep generator and other devices on the GPIB is via a 24-wire interface cable. The interface cable is specifically constructed with each end containing a connector shell with two connector faces. These double-faced connectors allow for parallel connection of two or more cables to a single device.

Cable Length Restrictions

The GPIB system can accommodate up to fifteen instruments at any one time. To achieve design performance on the bus, the proper timing and voltage level relationships must be maintained. If either the cable length between separate instruments or the accumulated cable length between all instruments is too long, the data and control lines cannot be driven properly and the system may fail to perform. Cable length restrictions are as follows:

- No more than 15 instruments may be installed on the bus.
- Total accumulative cable length in meters may not exceed 2 times the number of bus instruments, or 20 meters – whichever is less.

GPIB Interconnection

The only interconnection required for GPIB operation is between the sweep generator and the controller. To accomplish this interconnection, a special cable is required. This cable – WILTRON Part No. 2100-1, -2, -4 or -5 (1, 2, 4 or 5 meters in length) – is available from the factory.

GPIB Address

The GPIB address is hardwired to Address=5.

A1 GPIB PCB Description

The A1 GPIB PCB provides the interface between the signal source and the bus. This is a replaceable assembly; it contains no user-replaceable parts.

10-6 A4 ALC PCB CIRCUIT DESCRIPTION

The A4 ALC PCB, along with circuitry on the RF Deck and the YIG Driver PCB (A6, A7, A8, or A9), provides for the automatic leveling of the RF output power. An overall block diagram of the ALC loop is shown in Figure 10-5.

The output from the RF Oscillator goes to the RF Coupler/Detector via the PIN Switch. The coupler sends a detected sample of the output signal to the the appropriate Preamp circuit on the A4 PCB. The Log Amp/Shaper amplifies and shapes the detector output signal and changes its relationship to the main power signal from logarithmic to linear.

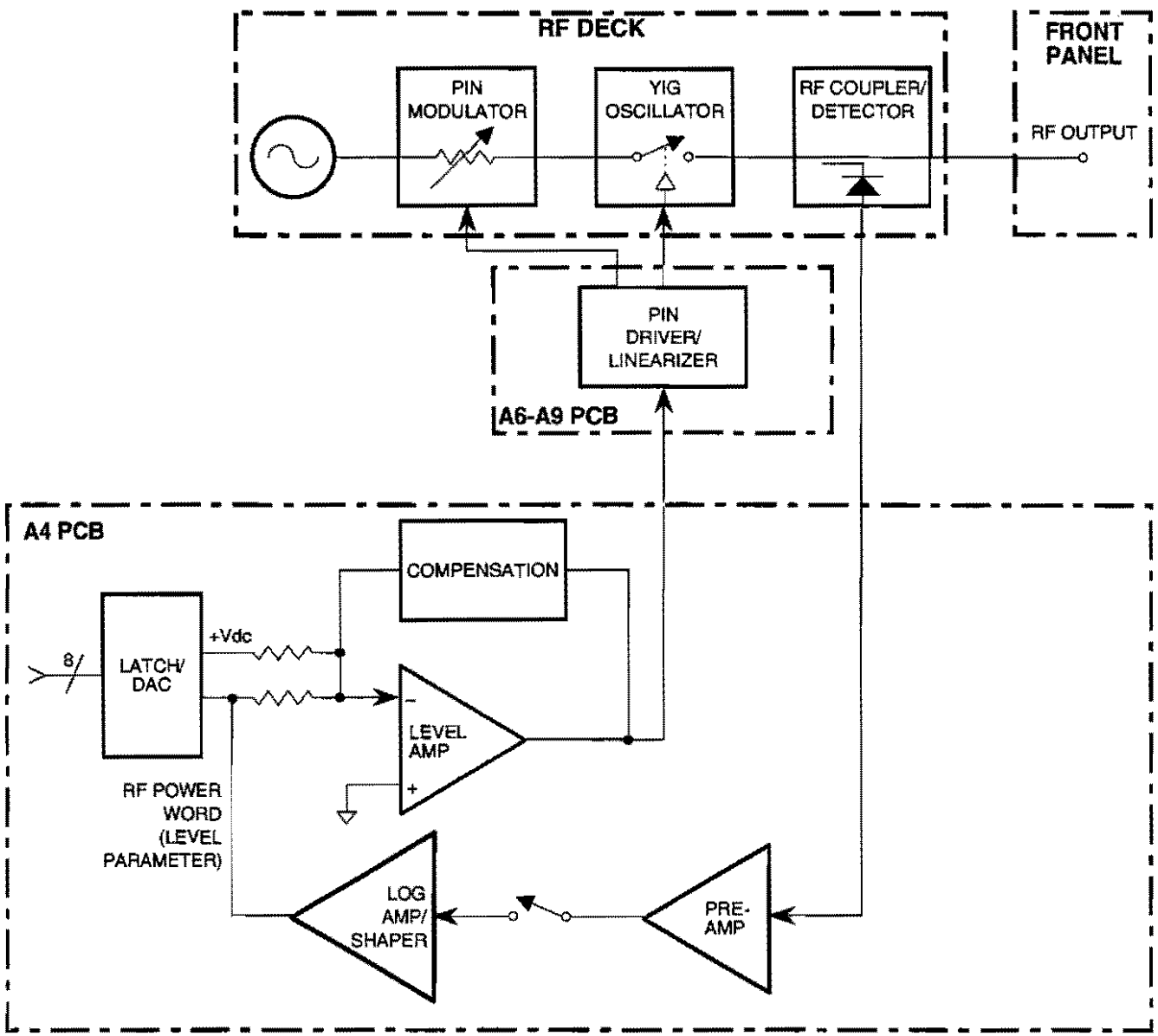
The Log Amp/Shaper output is summed at the Level Amp with the voltage output from the Reference DAC. The DAC output is the analog voltage representation of the digital power word selected via the GPIB. The ALC loop contains a log amplifier to provide the signal source with the means for setting output power in dBm.

The output of the Level Amp goes to either the A6, A7, A8, or A9 PCB PIN Driver/Linearizer circuit (depending on which YIG oscillator band is supplying the output power). This circuit provides an adjustment for customizing the loop gain for each YIG oscillator band.

The A4 PCB leveling circuit provides overall control of the RF output power. The A4 PCB has two preamplifiers for internal leveling: a Het (Heterodyne) Band and a YIG Band(s) circuit. The output signal from the preamplifier circuit goes to the Log Amp/Shaper circuit, which provides gain and shaping for this signal.

The Level Amp and its associated input circuitry gives the A4 PCB overall control over the level of the signal source output power signal.

The remaining block is the Compensation circuit. This circuit stabilizes the loop.



* This figure does not show all of the inputs that are summed into the level amp. See the A4 PCB overall block diagram for complete circuit.

Figure 10-5. *ALC Loop Block Diagram*

10-7 A5 FREQUENCY INSTRUCTION PCB CIRCUIT DESCRIPTION

The A5 Frequency Instruction PCB (Figure 10-6) provides linearized YIG oscillator tuning voltages to the A6, A7, A8 and A9 YIG Driver PCBs. The A5 PCB also supplies a regulated +10V bandswitch-reference voltage to the A6-A9 YIG Driver PCBs, and an RF Slope control voltage to the A4 ALC PCB.

The linearized YIG tuning voltage, **FCEN,** goes to the YIG Driver PCBs. There, it is used to generate the YIG oscillator tuning current. The **FSEL** signal is summed with the **FCORR** signal to produce the linearized YIG oscillator tuning voltage, **FCEN.** The **FSEL** and **FCORR** signals are the outputs of the Center Frequency and Correction Frequency DAC's (digital-to-analog converters) respectively. The input to the Center Frequency DAC is a 16-bit group from the GPIB microprocessor representing the selected frequency. The input to the Correction Frequency DAC is an 8-bit word from the 64K ROM (read only memory) where the frequency correction data is stored. The input to the ROM are the 13 MSB's (most significant bits) of the latched 16-bit GPIB group representing the selected frequency.

The microprocessor applies the two 8-bit words that constitute the center-frequency-control group to the FCEN DAC, via FCEN Latches 1 and 2. Word number 1 (the most significant word—MS word) loads into latch number 2 when the microprocessor clocks the **SP0** line LOW. Word number 2 (the least significant word—LS word) loads into latch number 1 when the microprocessor clocks **SP1** LOW. After word number 2 latches, the microprocessor clocks both the **SP0** and **SP1** lines LOW, which loads the DAC. This latching arrangement simultaneously applies all sixteen bits of the center-frequency-control group to the FCEN DAC.

The **FCEN/VPF** signal is the output of the Step Frequency DAC circuit. It goes to the YIG Driver PCBs to control band selection. The **FCEN/VPF** signal path contains an overcurrent protection circuit to protect the YIG oscillators from damaging current levels. Activation of the overcurrent protection circuitry lights an on board LED. The input to the Step Frequency DAC is a 12-bit group from the GPIB microprocessor. This 12-bit group is formed using two 8-bit words (the remaining 4-bits in word number 1 are not used).

The input digital group is loaded into the Step Frequency DAC when the microprocessor clocks **SP3** and **SP4** LOW.

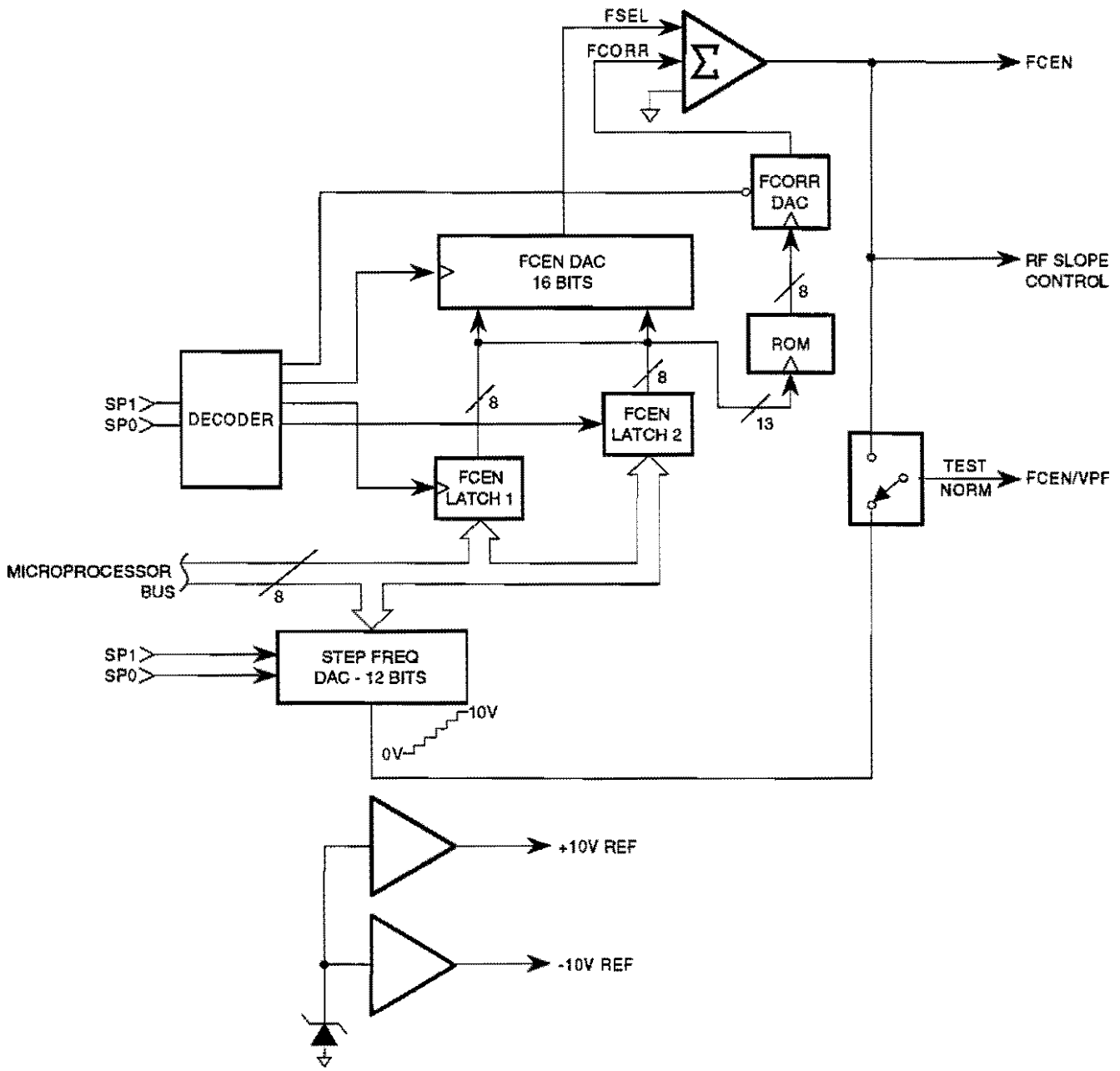


Figure 10-6. *A5 Frequency Instruction PCB Block Diagram*

10-8 OVERALL FREQUENCY GENERATION

The three YIG Driver PCBS for the 360SS47 — or the four YIG Driver PCBs for the 360SS69 — function together to cover the output frequency range. This circuit discussion is divided into overall frequency generation and PCB discription. Refer to the overall block diagram (Figure 10-3 or 10-4, as appropriate) while reading this description.

The YIG Driver PCBs provide drive currents for their associated YIG oscillator tuning coils and for PIN Switch A4S1. They also provide modulating currents for the ALC-loop PIN attenuator. The PCBs also develop the oscillator-bandswitch logic voltages.

NOTE

In the following circuit discussion, the L or H that precedes a signal-line name indicates the line's active (or true) logic state.

The 360SS uses three, or four, YIG oscillators to sweep its frequency range. Each YIG oscillator requires a YIG Driver PCB. The three main signals used to develop tuning and bias currents are the F CEN, $\Delta F >$ 50 MHz, and F CORR signals from the A5 Frequency Instruction PCB. These three signals feed in parallel to all YIG driver PCBs. However, because the H SNB (select next band) oscillator-bandswitch lines on the A7, A8, and/or A9 PCBs are initially false, the A6 PCB is the only one that can use the signals. There, they are summed and used to generate the frequency sweep.

The fourth A5 signal, FCEN/VPF, provides for oscillator bandswitching. A bandswitch occurs on the A6 PCB at 2 GHz and again at 8 GHz. At 2 GHz, the L HET PIN Select line goes false. This switches both the 0.01-to-2 GHz Down Converter Band (also referred to as Het (heterodyne) band) out of the circuit and the S/C-band (2-to-8 GHz) YIG in. At approximately 8 GHz, several events occur:

- The YIG oscillator tuning coil leaves the oscillator tuned to a rest frequency of 8 GHz.
- The Mod Driver line on the A6 PCB sets the Mod attenuator to maximum attenuation, and the L PIN Select line causes the S/C-band element in the PIN Switch to turn off. This action attenuates by 60 dBc or less the feedthrough of the S/C-band YIG oscillator signal.

The SNB and SNR (select-next-band and select-next-ROM) lines on the A6 PCB toggle from low to high, causing the X-Band (8-to-12.4 GHz) YIG oscillator and A5 PCB linearizer ROM to be selected. When the X-Band YIG oscillator is selected, the A7 PCB sums the three signals from the A5 Frequency Instruction PCB (F Cen, $\Delta F > 50$ MHz, F Corr) and uses them to generate the X-band sweep. This sweep starts at 8 GHz. As on the A6 PCB, the FCEN/VPF signal from A15 provides for oscillator bandswitching. The A7 PCB has only one bandswitch point (12.4 GHz) and when it is reached, the following occur:

- The YIG oscillator tuning coil leaves the oscillator tuned to its rest frequency (approximately 12.4 GHz).
- The Mod Driver line on the A7 PCB sets the X-band attenuator in PIN Switch to maximum attenuation. The L PIN Select line turns the X-band switch off. This action attenuates by 60 dBc or less the feedthrough of the X-band signal.
- The SNB and SNR lines on the A7 PCB toggle from low to high and select the Ku-Band YIG oscillator and ROM. The Ku-band (A8 PCB) and K-band (A9 PCB) circuit action is similar to that described for S/C and X bands.

10-9 A6–A9 YIG DRIVER PCB CIRCUIT DESCRIPTION

The YIG Driver PCBs are similar in their design and operation. The major difference is that the A6 S/C-Band YIG Driver PCB also drives the Down Converter. It also contains circuits for controlling the tracking filter that is built into the S/C-band circuit. The X- and Ku-band circuits are similar, except for the absence of tracking filter and HET (down converter) lines.

NOTE

In the following circuit discussion, the L or H that precedes a signal-line name indicates the line's active (or true) logic state.

The A6 PCB contains four functional blocks (Figure 10-7). The YIG oscillator and Tracking Filter Control circuits provide for tuning the YIG oscillator and its built-in tracking filter. The tracking filter provides harmonic suppression. The inputs to this block are the F Corr, $\Delta F > 50$ MHz, F CEN and CW FILTER control signals from the A5 Frequency Instruction PCB.

The Bandswitch and ROM Select Logic and Control circuits provide for bandswitching between the three YIG Driver PCBs. Its input is the F CEN/VPF. Its outputs are the L YIG FM COIL SEL, L HET YIG SEL, L HET PIN SEL, L PIN SEL, L SNB, L SNR, and L YIG SEL control lines.

The PIN Driver Linearizer circuit processes the control line for the S/C-band Modulator circuit, which for this band is a separate component. For the other two bands, the modulator/attenuator pad is built into the PIN Switch. The modulator provides ALC control for their associated YIG oscillator output signal.

The A5 PCB linearizer ROM circuit provides compensation for its associated YIG oscillator. Many YIG oscillators, though inherently linear, often have linearity errors due to magnetic saturation effects. This ROM provides for up to ±64 MHz of frequency correction.

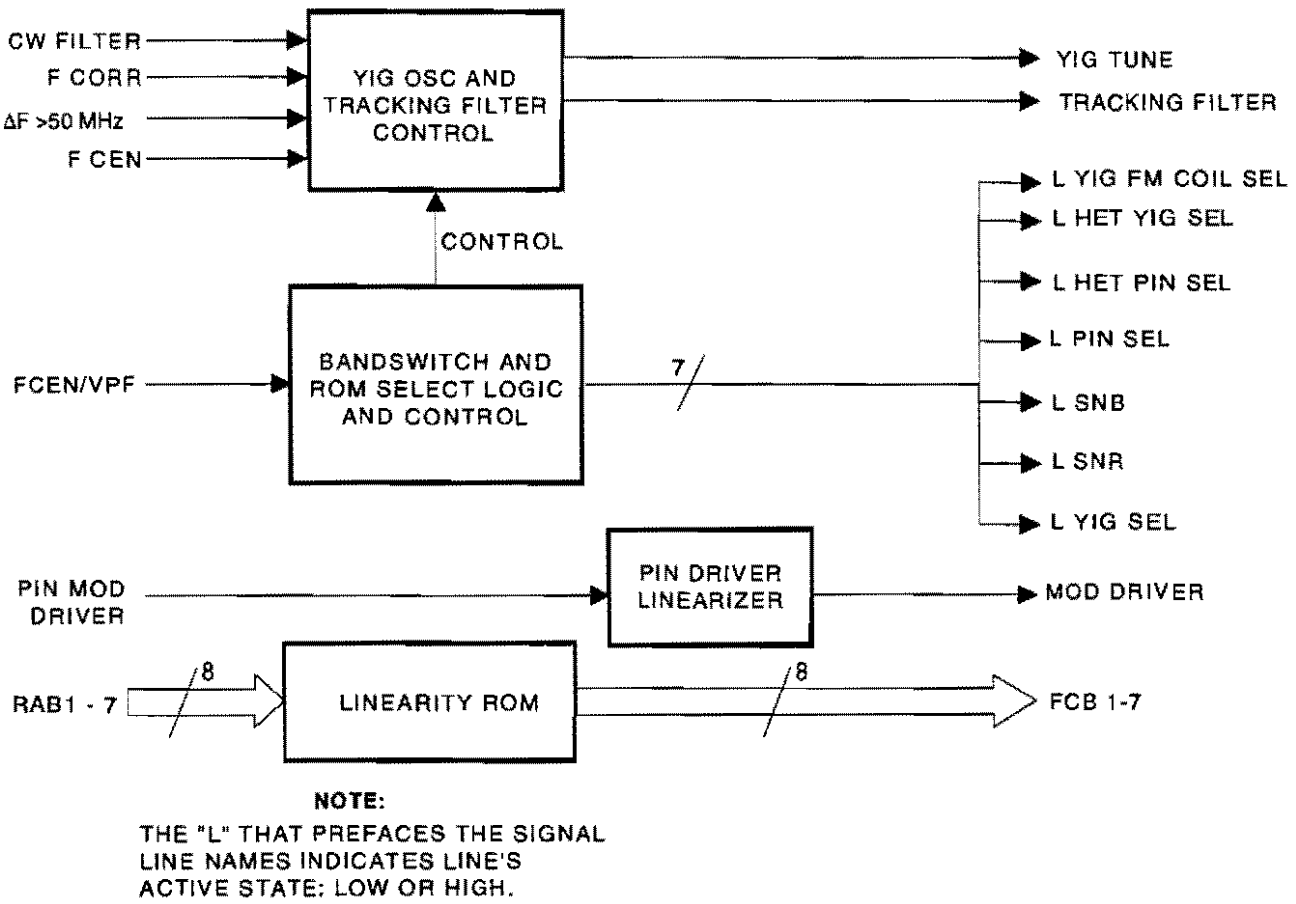


Figure 10-7. A6–A9 YIG Driver PCB Block Diagram

10-10 A10 FM/ ATTENUATOR PCB CIRCUIT DESCRIPTION

The A10 FM/Attenuator PCB (Figure 10-8) generates FM modulation for the YIG oscillators and drive for the 2-to-8 GHz YIG tracking filter.

NOTE

In the following circuit discussion, the L or H that precedes a signal-line name indicates the line's active (or true) logic state.

The signal input for the A10 PCB enters on either the EXT FM Input signal line, the ΔF ≤50 MHz signal line, or on both concurrently. The ΔF ≤50 MHz signal line is from the A5 Frequency Instruction PCB. If the operator selects a delta frequency sweep mode (ΔF CF, ΔF M1) and a sweep width (ΔF) of 50 MHz or less, this input is a voltage ramp. The amplitude of this ramp depends on the sweep width. For a sweep width of 50 MHz, the amplitude is 10V (from –5V to +5V). For sweep widths less than 50 MHz, the amplitude is proportionally less than 10V. The EXT FM Input signal line is from the rear panel EXT FM Ø LOCK INPUT connector.

The Variable Gain circuit provides a voltage gain for the FM input signal. Stage gain depends on which of the available YIG oscillators is supplying the output frequency. The output of this circuit goes to the FM Coil Current Driver circuit. The output from the FM Coil Current Driver circuit drives the YIG oscillator FM tuning coils. This coil current returns to ground via the Current Sense resistor, which is effectively in series with the FM coils. The voltage drop across the Current Sense resistor is proportional to the current through the FM coils.

While the S/C- and X-Band YIG oscillators and the K-band and Ku-band (360SS69) oscillators receive their drive and FM coil currents in series, only one oscillator band at a time has its output switched to the sweep generator RF output circuit. This RF output switching is a function of the PIN Switch.

Besides supplying the input for the FM coil-current driver circuits, the Variable Gain circuit also supplies the input for the Tracking Filter current-driver circuit. A tracking filter is used only with the S/C-band YIG oscillator. This filter is a high-Q YIG bandpass filter that resides in the same module as the YIG oscillator. It is in series with the YIG oscillator and tracks at the same frequency. It attenuates harmonic and spurious signals.

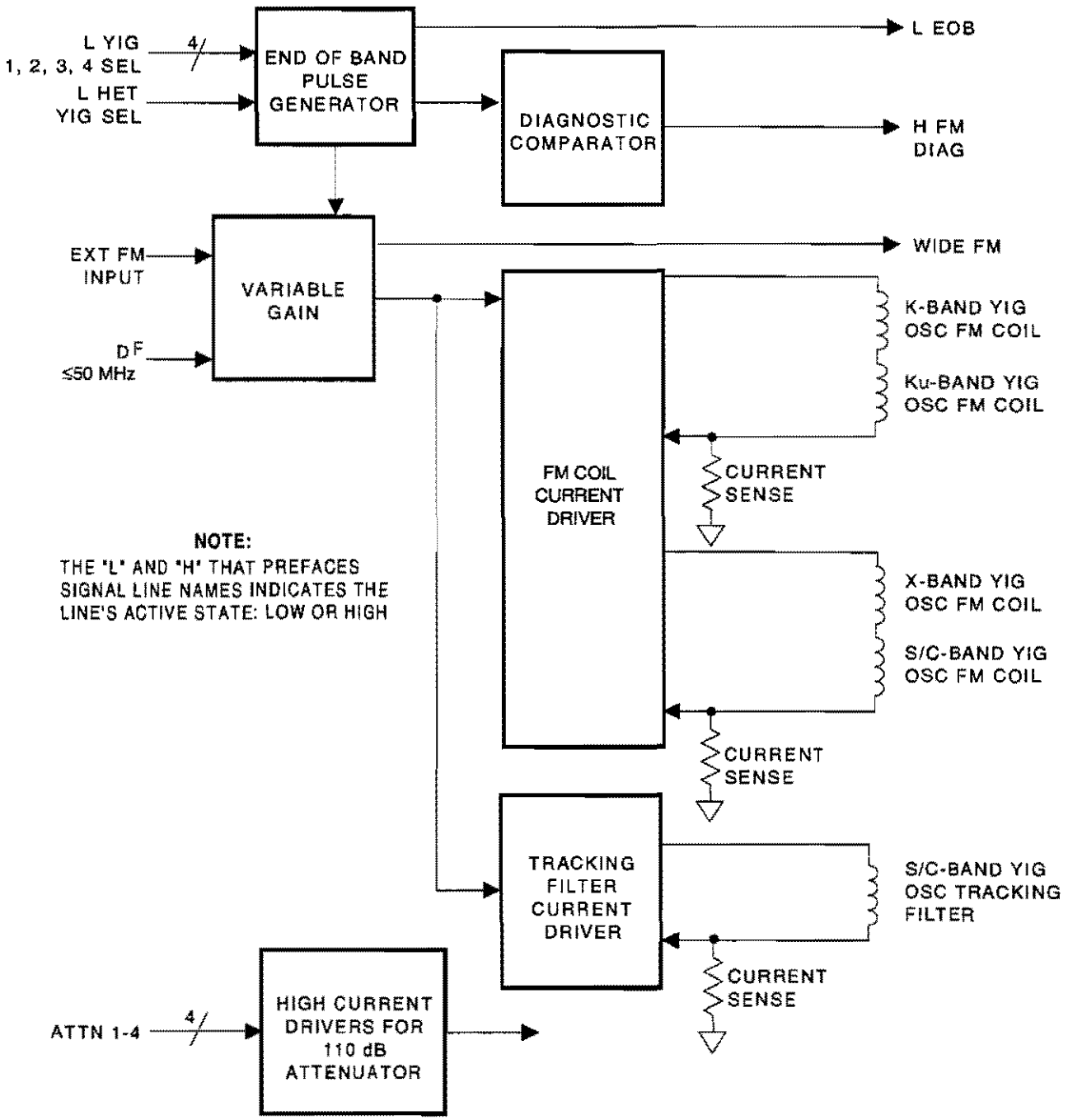


Figure 10-8. *A10 FM/Attenuator PCB Block Diagram*

10-11 SWITCHING POWER SUPPLY CIRCUIT DESCRIPTION

The A13/A14 Switching Power Supply (Figure 10-9) is a half-bridge, quasi-square-wave, high-efficiency +5V converter. It also contains the following circuits:

- ±15V LC (low current) supply
- ±15V HC (high current) supply
- +12V regulated supply
- +24V regulated supply
- –39V regulated supply
- +18V unregulated supply
- +28V unregulated supply

As shown in Figure 10-9, the switching power supply circuits and components are dispersed over the following PCBs and assemblies:

- *A16 Rear Panel Assembly.* Line Voltage Selector Module and Fan.
- *A14 Motherboard PCB.* Off-Line Rectifier, Start-up Transformer, Power Switch, Over-Voltage Sense, Out-of-Reg Sense, Line Sense, –39V, +24V, and ±15V LC Regulator circuits.
- *A13 Switching Power Supply PCB.* Control Amplifier, Soft-Start Control, Shut-Down Timer, Over-Current Sense, Pulse-Width Modulator, and Switching Transistors circuits.
- *A0 Basic Frame Assembly.* –39V Regulator pass transistor and ±15V HC Regulator circuits.

The ac line power entering the signal source is input to the Off-Line Rectifier circuit. This circuit is a full-wave voltage doubler (120V line) or a full-wave bridge rectifier (220V line). The circuit's voltage output for either input-line voltage is 330 Vdc (±165 Vdc). Resistors sense the circuit's output current. If the current exceeds three amperes, it activates the optically coupled Over-Current Sense circuit. When activated, this circuit causes the Shut Down Timer to turn off the switching transistor drive voltage. The ±165 Vdc output from the Off-Line Rectifier circuit goes to the dc-isolated Switching Transistors on the A13 PCB.

CAUTION

Use an isolation transformer between the signal source and the ac line whenever you are performing maintenance on the switching power supply. Because this power supply references portions of its circuitry to the peak negative or positive line voltage, you must use an isolation transformer to protect test instruments.

The Switching Transistors alternately switch between +165 Vdc and –165 Vdc at a 50 kHz rate. These transistors are driven by the Pulse-Width Modulator (PWM) circuit. This circuit develops a train of pulses. The duty cycle of this pulse train varies between 25% and 40% (approximately), depending on the amplitude of control voltage Vc. This Vc-voltage amplitude is determined by either the Control Amplifier, the Soft-Start Control circuit, or the Shut-Down Timer circuit.

The input to the Control Amplifier is the +5V SENSE line from the motherboard. This line senses the voltage across the +5V load. The output of the Control Amplifier forces the PWM to adjust the duty cycle to whatever is necessary to maintain +5V at the sense line.

The input to the Soft-Start Control circuit is +12V from the +12V Regulator. At the instant you press the POWER key on the Analyzer, +12V is applied to this circuit. It causes the output of the +5V supply to be minimum. Gradually, as a circuit capacitor charges, the the duty cycle of the circuit's output pulse train increases and the +5V supply output voltage increases. When the Control Amplifier senses that 5 volts has been reached (approximately 20 ms), regulation occurs. If a malfunction were to occur, the Over-Voltage circuit would trigger the Shut-Down Timer circuit at approximately 5.7 volts.

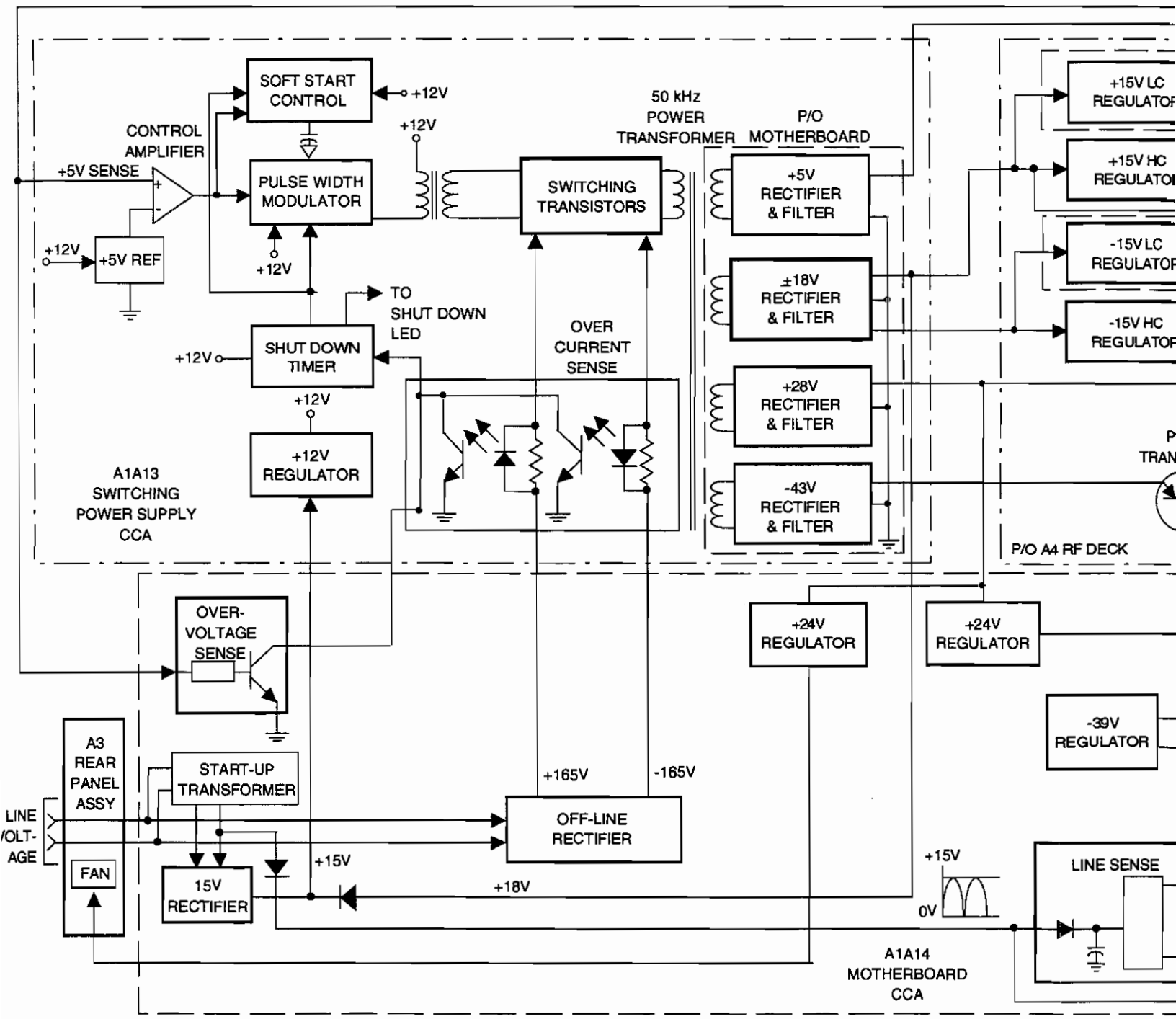
The input to the Shut-Down Timer circuit is a trigger pulse caused by the OVER-VOLTAGE/CURRENT line going LOW. When triggered, this circuit generates a 1-second pulse (approximately) that causes the input to the PWM to go to +12V. This shuts down the Switching Transistors. After the Shut Down Timer circuit times out, the power supply soft-starts. However, if the condition causing the Shut Down Timer circuit trigger is still present, it generates another pulse and shuts the supply down again. This pulsing operation continues until either the overvoltage/current condition is corrected or POWER switch is pressed to OFF.

The dc isolation transformer on the output of the PWM couples its output to t he Switching Transistors. These transistorss require a bias of approximately 5V to be switched on. Their output form a composite waveform. The peak-to-peak value of this waveform is directly proportional to the peak value of the 120V line (or directly proportional to the peak-to-peak value of the 220V line).

This waveform is coupled to the five secondaries of the 50 kHz Power Transformer. The reduced voltages appearing in the transformer secondaries are also proportional to the line voltage. These reduced voltages are rectified and passed through inductors which function as integrators.

The five rectifier circuits—excepting the +5V circuit—supply their respective outputs to voltage regulators. The –39V Regulator is driven by the –43V supply. The +24V Regulator is driven by the +28V supply. The –15V LC (low current) and HC (high current) Regulators are driven by the –18V supply. And the +15V LC and HC Regulators are driven by the +18V supply. The unregulated +18V also goes to the YIG driver bias supply on the A6-A9 PCBs and to the +15V Rectifier circuit.

The remaining two circuits are the Out of Reg Sense and the Line Voltage Sense circuits. The Out of Reg Sense circuit detects when any of the regulated supplies goes out of tolerance. If such a condition exists, the L OR diagnostic line goes TRUE and the A14 OUT OF REG indicator LED lights. The Line Voltage Sense circuit detects when the ac line exceeds the +5% or –10% limits required for circuit operation. This circuit also detects whether the Line Voltage Selector Module PCB is correctly positioned for the available line voltage. If either the line voltage is incorrect or the PCB is improperly positioned, the appropriate L HL or L LL diagnostic line will go TRUE, and the LED indicator will light.


SOFT START CONTROL
+12V
CONTROL AMPLIFIER
+5V SENSE
PULSE WIDTH MODULATOR
+12V
+5V REF
+12V
50 kHz POWER TRANSFORMER
SWITCHING TRANSISTORS
P/O MOTHERBOARD
+5V RECTIFIER & FILTER
±18V RECTIFIER & FILTER
+28V RECTIFIER & FILTER
-43V RECTIFIER & FILTER
+15V LC REGULATOR
+15V HC REGULATOR
-15V LC REGULATOR
-15V HC REGULATOR
TO SHUT DOWN LED
SHUT DOWN TIMER
+12V
OVER CURRENT SENSE
+12V REGULATOR
A1A13 SWITCHING POWER SUPPLY CCA
P/O A4 RF DECK
OVER-VOLTAGE SENSE
+24V REGULATOR
+24V REGULATOR
-39V REGULATOR
A3 REAR PANEL ASSY
START-UP TRANSFORMER
+165V
-165V
OFF-LINE RECTIFIER
LINE VOLT-AGE
FAN
15V RECTIFIER
+15V
+18V
+15V
0V
LINE SENSE
A1A14 MOTHERBOARD CCA

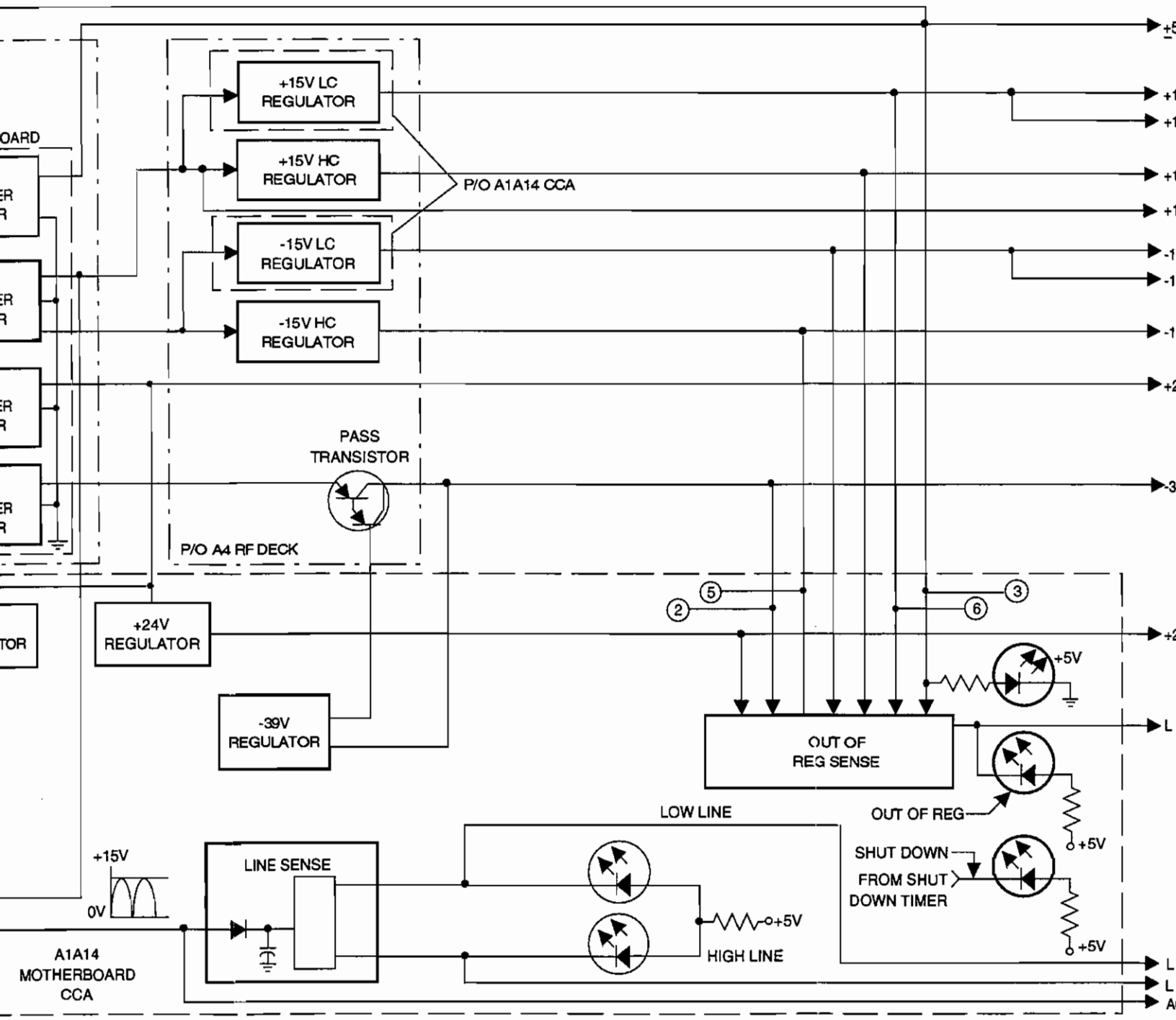
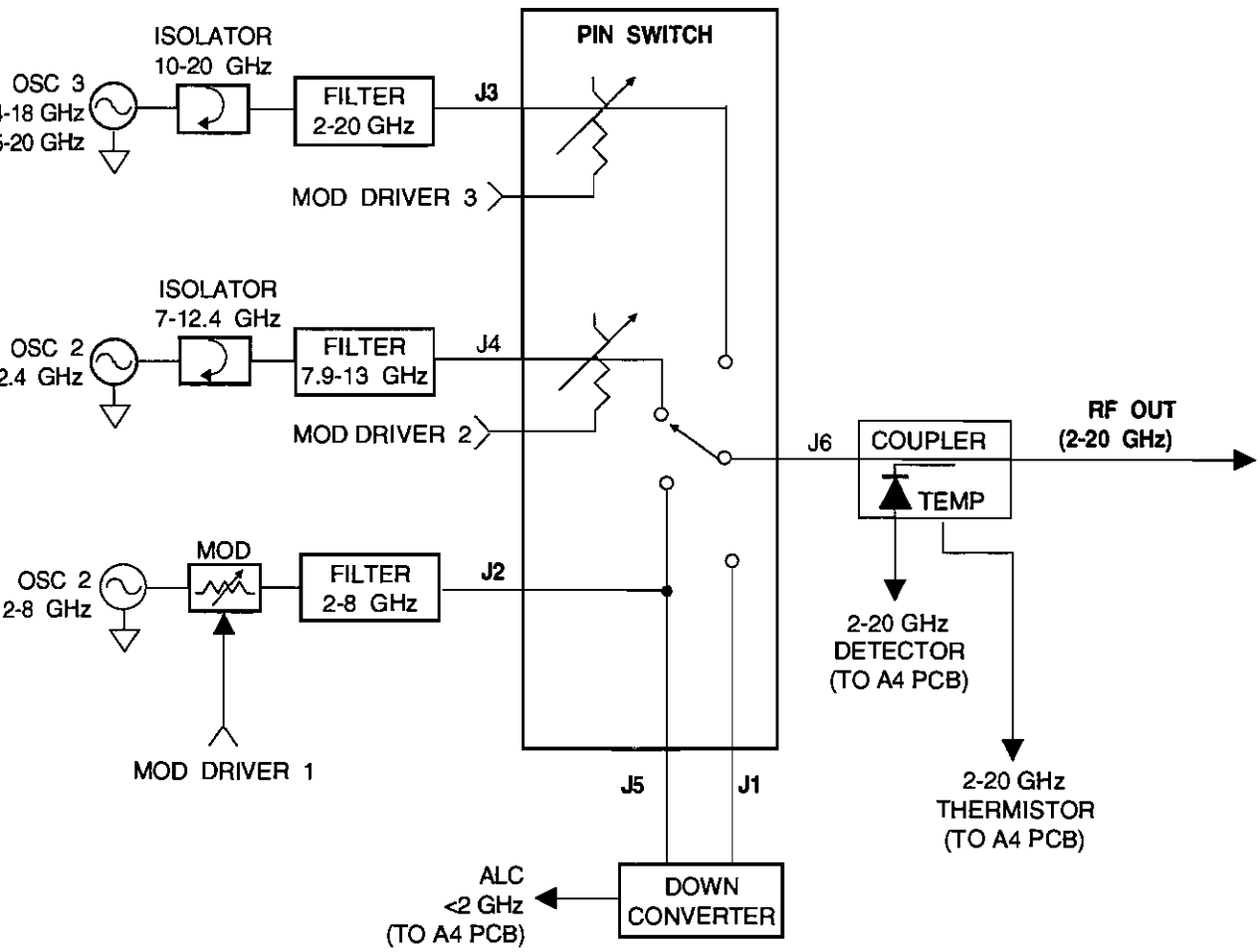
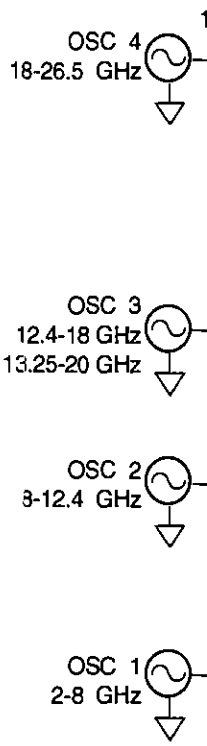
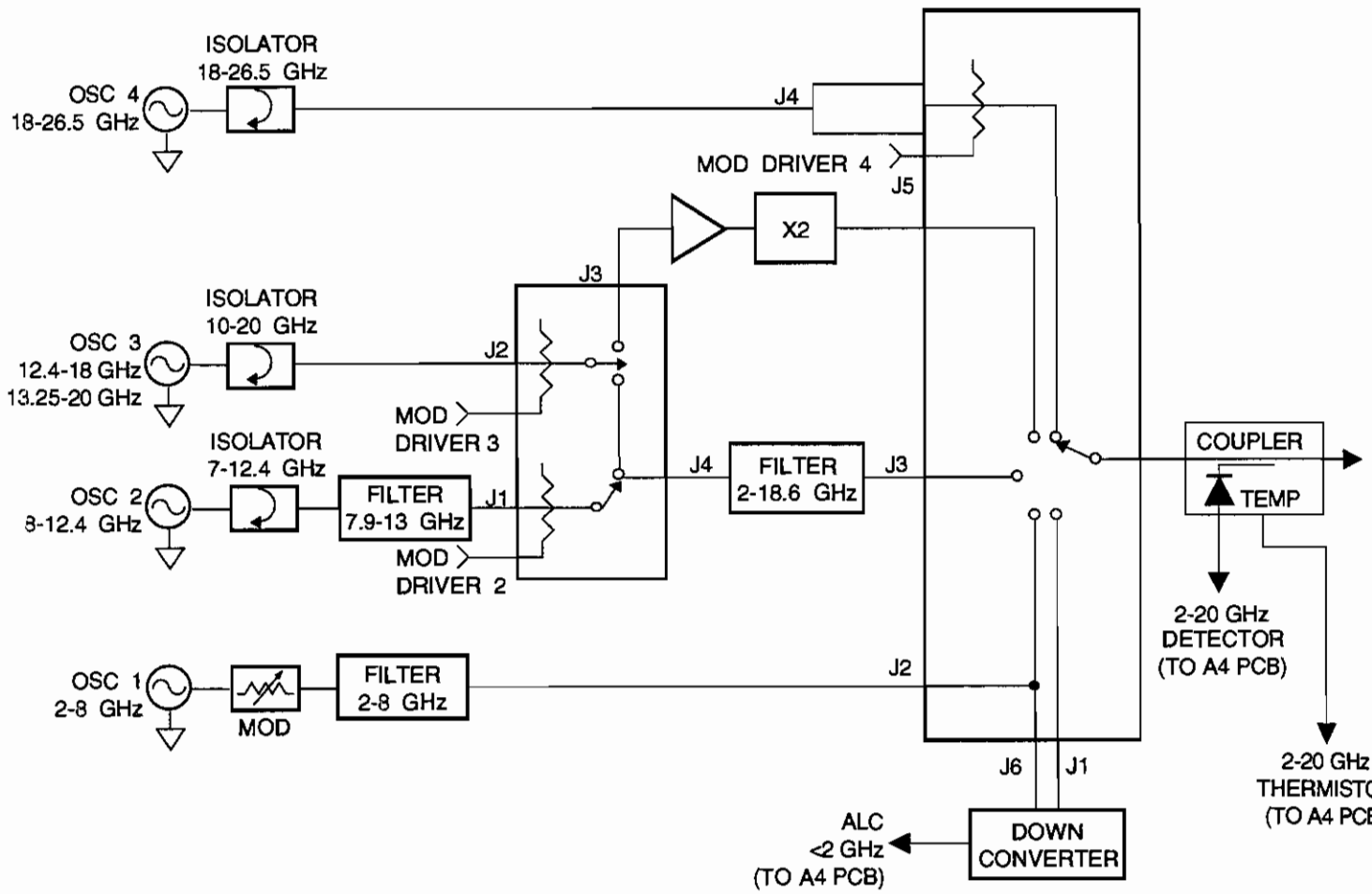


Figure 10-9. *Switching Power Supply Block*





360SS47 RF DECK



360SS69 RF DECK

Figure 10-10. *Model 360SS47 and 360SS69 RF Deck Block Diagrams*

10-12 RF DECK MODULE DESCRIPTIONS

The RF Deck modules are used to generate CW-frequency RF signals and to route such signals to the front panel RF OUTPUT connector. Figure 10-10 on the facing page provides block diagrams showing RF component configurations for the Models 360SS47 and 360SS69.

Oscillators The YIG-tuned oscillators are generally of the GaAs FET type and are manufactured primarily by WILTRON.

MOD (Modulator) The MOD unit is a current-controlled variable attenuator that provides amplitude control and power leveling for the Osc 1 output. It also provides impedance matching and isolation for the Osc 1 YIG.

Isolators The Isolators prevent reflected RF energy from returning to the YIG and causing frequency pulling. They attenuate the forward-wave energy by 0.7 dB and the reverse-wave energy by approximately 20 dB.

Filters The filters provide lowpass filtering for the RF frequencies, to reduce harmonics.

PIN Switch The PIN Switch is a current controlled variable attenuator. It switches between the available YIGs so that only one at a time is coupled to the RF output circuit. The switch also provides the means for amplitude-modulating and power-leveling the RF output signals.

Heterodyne Down Converter The Heterodyne Down Converter generates the 0.01 to 2 GHz frequency outputs. When you select a frequency in the range of 0.01 to 2 GHz, the Osc 1 YIG operates between 4.61 and 6.6 GHz. Its output is routed to the Down Converter via the PIN Switch. At the down converter it mixes with the output from a 4.6 GHz local oscillator. The difference frequency is amplified and provides the 0.01 to 2 GHz output.

Coupler The Coupler samples and detects the 2 GHz RF output for use in internal power leveling. The detected sample, along with a voltage representing the coupler's temperature, is routed to the A4 PCB.

10-13 CONFIDENCE TEST

The confidence test requires a GPIB controller. First, you use the controller to program the signal source for known frequency and power levels. Then you use external test equipment to determine if the programmed settings are being achieved. The confidence tests can be accomplished with the source installed in the console. To do so, remove the SYSTEM BUS interconnection between the source and analyzer and replace it with a GPIB interconnection between the source and an external controller (Figure 10-11).

Recommended Test Equipment Table 10-5 provides a listing of test equipment needed to perform the confidence test.

Table 10-5. *Recommended Test Equipment for Confidence Testing*

Instrument	Critical Specifications	Manufacturer
Power Meter	GPIB Controllable	Hewlett-Packard Model 436A , with Option 22
Power Sensor	Frequency Range: 0.05–26.5 GHz Power Range: –30 to 20 dBm (1 µW to 100 mW)	Hewlett-Packard Model 8485A
Power Sensor	Frequency Range: 0.05–40 GHz Power Range: –30 to 20 dBm (1 µW to 100 mW)	Hewlett-Packard Model 8487A
Digital Multimeter	Resolution: 4½ digits DC Accuracy: 0.002% + 2 counts DC Input Impedance: 10 MΩ AC Accuracy: 0.07% + 100 counts AC Input Impedance: 1 MΩ	John Fluke Inc. Model 8840A, with Option 8804A-09 (True AC RMS)
Frequency Counter	Frequency Range: 0.01 to 40 GHz Input Impedance: 50Ω Resolution: 1 Hz External Time Base Input: 1 MΩ	EIP Microwave Inc. Model 548A, with External Mixers: Option 91 (26.5 to 40 GHz) Option 92 (40 to 60 GHz)
Oscilloscope	Bandwidth: DC to 150 MHz Vertical Sensitivity: 2 mV/division Horizontal Sensitivity: 50 ns/division	Tektronix Inc. Model 2445
Spectrum Analyzer with External Mixer	Frequency Range: 0.01 to 100 GHz Resolution Bandwidth: 100 Hz	Tektronix Inc. Model 494 with External Mixer (PN 015-300085-00)

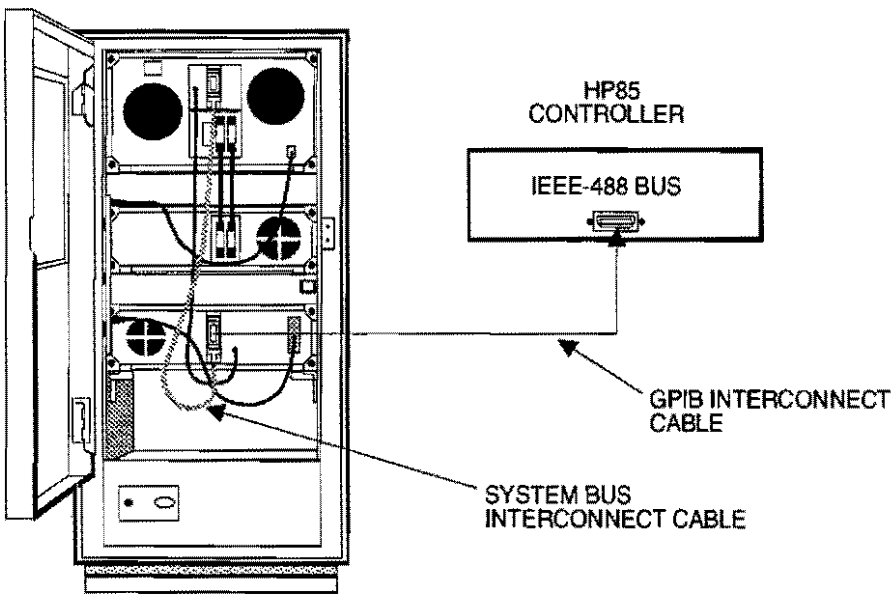


Figure 10-11. *Test Equipment Setup for Confidence Test*

Testing the ALC Loop

To determine whether the A4 PCB and overall ALC loop is functioning properly, proceed as follows:

Connect the test equipment as shown in Figure 10-12. If you wish to remove the source from the console, refer to paragraph 10-15 for removal instructions.

From the controller keyboard, type the following code: (Example is for an HP85 Controller.)

```
10  DISP "SELECT FREQUENCY IN GHZ"
20  INPUT A*
30  OUTPUT 705; "CF1",A,"GHZ"
40  DISP "ENTER POWER LEVEL IN dBm"
50  INPUT P*
60  OUTPUT 705; "LVL",P,"DM"
70  GOTO 10
RUN
```

Typically, you should check the high-end, mid-band, and low-end frequencies in each band at three power levels: guaranteed power, –5 dB and –10 dB down from guaranteed power.

Verify that the measured frequency is within ±2 dB of the power level entered for the program's P variable.

Repeat for the next frequency/power level.

If the power level is within the ±2 dB tolerance window, the ALC loop can be assumed to be functioning properly.

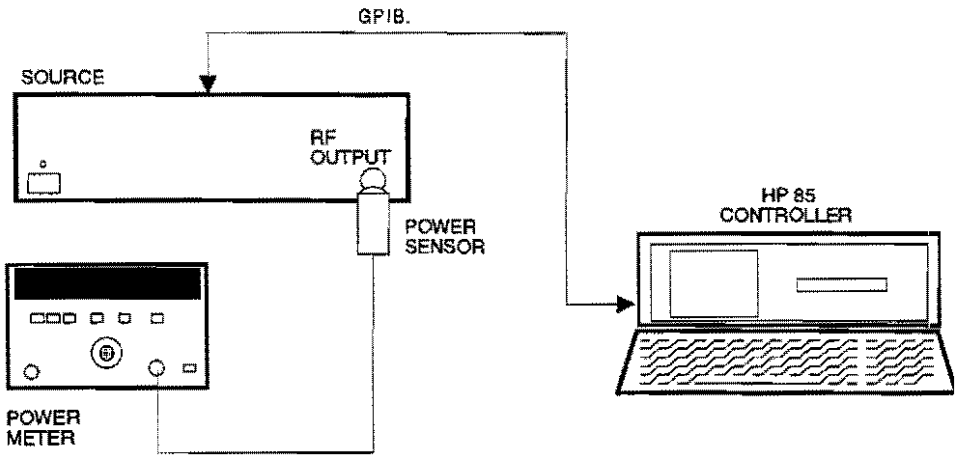


Figure 10-12. *Test Equipment Setup for ALC Loop Confidence Test*

Testing the Frequency Generation Subsystem

The following procedure verifies that the 360SS is producing the proper output frequency. To determine proper operation, you have to set the source for a series of CW frequencies in each band then verify that the output frequency is within the tolerance window.

Connect the test equipment as shown in Figure 10-13.

From the controller keyboard, type the following code: (Example is for an HP85 Controller.)

```
10 DISP "SELECT FREQUENCY IN GHZ"
20 INPUT A*
30 OUTPUT 705; "CF1",A,"GHZ"
40 GOTO 10
RUN
```

Typically, you should check the high-end, mid-band, and low-end frequencies in each band.

Verify that the measured frequency is within ±40 MHz of the frequency entered for the program's "A" variable.

Repeat for the next frequency.

If the measured frequencies are within their tolerance window, the Frequency Generation Subsystem can be assumed to be functioning properly.

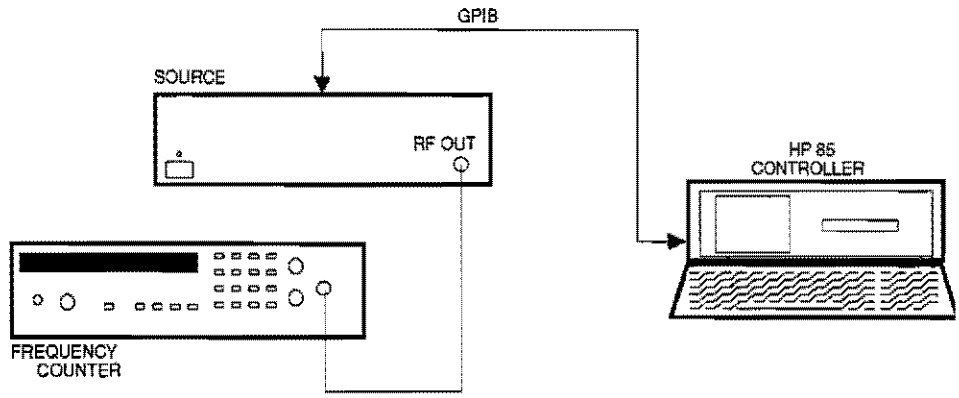


Figure 10-13. *Test Equipment Setup for Frequency Generation Subsystem Confidence Test*

Testing the FM Phaselock Circuit

This test checks that the source has a 6 MHz-per-volt response to an input dc voltage.

Connect the test equipment as shown in Figure 10-14.

From the controller keyboard, type the following code: (Example is for an HP85 Controller.)

```
10 DISP "SELECT FREQUENCY IN GHZ"
20 INPUT A*
30 OUTPUT 705; "CF1",A,"GHZ"
40 GOTO 10
RUN
```

Set the power supply for +4 volts.

Observe that the frequency counter indicates the programmed frequency (`INPUT A` variable), –24 MHz ± 2.4 MHz.

Set the power supply for –4 volts.

Observe that the frequency counter indicates the programmed frequency, +24 MHz ± 2.4 MHz.

If the shifts in frequency are within the tolerance windows, the A10 PCB phase-lock circuits can be assumed to be functioning properly.

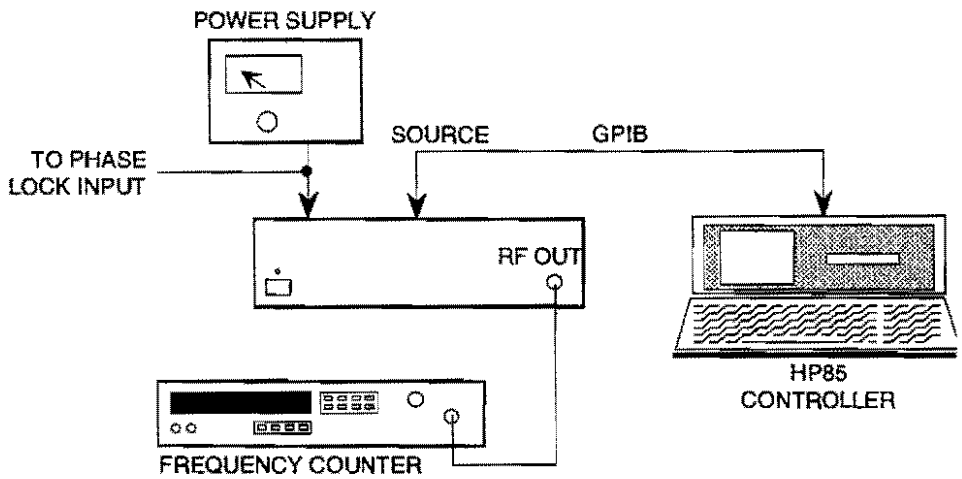


Figure 10-14. *Test Equipment Setup for FM Phase-Lock Confidence Test*

10-14 ADJUSTMENT PROCEDURES

This paragraph provides adjustment procedures that you should perform following the repair or replacement of printed circuit boards (PCBs), which are listed in Table 10-6.

Table 10-6. Recommended Adjustments Following Repair or Replacement

PCB	Adjustment
A4 PCB	ALC Loop Calibration and Adjustments (page 10-64)
A5 PCB	A5 PCB Frequency Adjustments (page 10-50)
A6 PCB	A6-A9 YIG Oscillator Bandswitch Adjustments (page 10-52) A6-A9 YIG Bias Check (page 10-56) 2–8 GHz Band (Osc 1) Tracking Filter Adjustments (page 10-62) 2 GHz Bandswitch Compensation Adjustment (page 10-63) ALC Loop Calibration and Adjustments (page 10-64)
A7–A9 PCB	Same as above, except 2 GHz Bandswitch Compensation Adjustment
A10 PCB	None
A13 PCB	Power Supply Adjustments (page 10-70)

Recommended Test Equipment

Table 10-7 lists the test equipment needed for performing the adjustment procedures.

Table 10-7. *Recommended Test Equipment for Adjustments*

Instrument	Critical Specifications	Manufacturer
Power Meter	GPIB Controllable	Hewlett-Packard Model 436A , with Option 22
Power Sensor	Frequency Range: 0.05–26.5 GHz Power Range: –30 to 20 dBm (1 µW to 100 mW)	Hewlett-Packard Model 8485A
Power Sensor	Frequency Range: 0.05–40 GHz Power Range: –30 to 20 dBm (1 µW to 100 mW)	Hewlett-Packard Model 8487A
Digital Multimeter	Resolution: 4½ digits DC Accuracy: 0.002% + 2 counts DC Input Impedance: 10 MΩ AC Accuracy: 0.07% + 100 counts AC Input Impedance: 1 MΩ	John Fluke Inc. Model 8840A, with Opt ion 8804A-09 (True AC RMS)
Frequency Counter	Frequency Range: 0.01 to 40 GHz Input Impedance: 50Ω Resolution: 1 Hz External Time Base Input: 1 MΩ	EIP Microwave Inc. Model 548A, with External Mixers: Opt ion 91 (26.5 to 40 GHz) Option 92 (40 to 60 GHz)
Oscilloscope	Bandwidth: DC to 150 MHz Vertical Sensitivity: 2 mV/division Horizontal Sensitivity: 50 ns/division	Tektronix Inc. Model 2445
Spectrum Analyzer with External Mixer	Frequency Range: 0.01 to 100 GHz Resolution Bandwidth: 100 Hz	Tektronix Inc. Model 494 with External Mixer (PN 015-300085-00)

10-15 A5 PCB FREQUENCY ADJUSTMENTS

This paragraph provides instructions for adjusting the A5 F Center DAC voltages, and the A6-A9 bandswitch reference voltages. These voltages should be checked and adjusted, if necessary, following maintenance on any of the A6-A9 PCBs or when any of the frequency specifications are found to be out of tolerance.

Step 1. Set up the test equipment as shown in Figure 10-15.

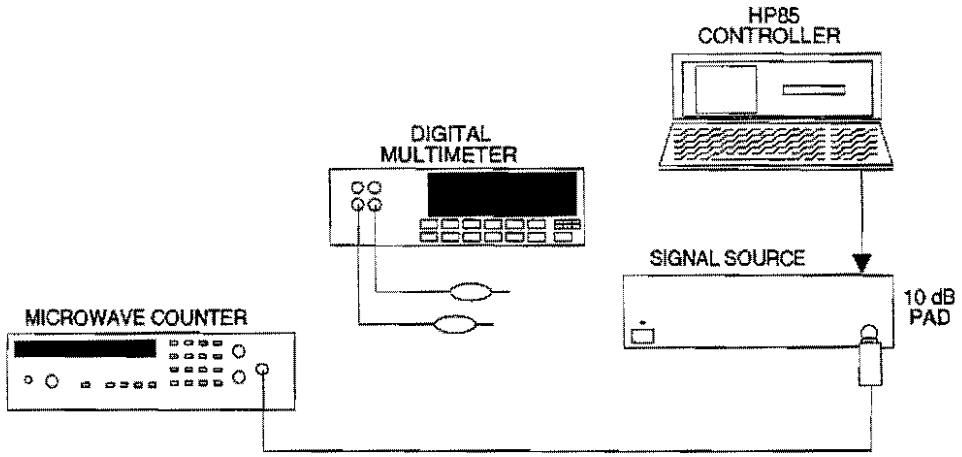


Figure 10-15. *Test Equipment Setup for ALC Loop Confidence Test*

Step 2. Remove top cover.

Step 3. Reset the 360SS by cycling the line power off and on.

Step 4. Connect the digital multimeter leads between A5TP6 (+) and A5TP1 (–) (Figure 10-16).

Step 5. Verify that the digital multimeter indicates +10 ±0.1V.

Step 6. Connect the digital multimeter leads between A5TP3 (+) and A5TP1 (–).

Step 7. Verify that the digital multimeter indicates –10 ± 0.1V.

NOTE

Steps 8 thru 12 are not routine adjustments. They should be performed only if A5U10 has been replaced.

Step 8. Remove the cover from the F Center circuit (U5,U9, U10) (Figure 10-16).

Step 9. Reset the 360SS by cycling the line power off and on.

Step 10. Reset the F_{Cen} DAC by connecting one end of a short jumper wire to A5TP1; contact the other end of the jumper first to A5U6, pin 3, then to A5U6, pin 2.

Step 11. Connect the digital multimeter test leads between A5TP5 (+) and A5TP4 (–).

Step 12. Adjust A5R8 for 0V ±50 µV.

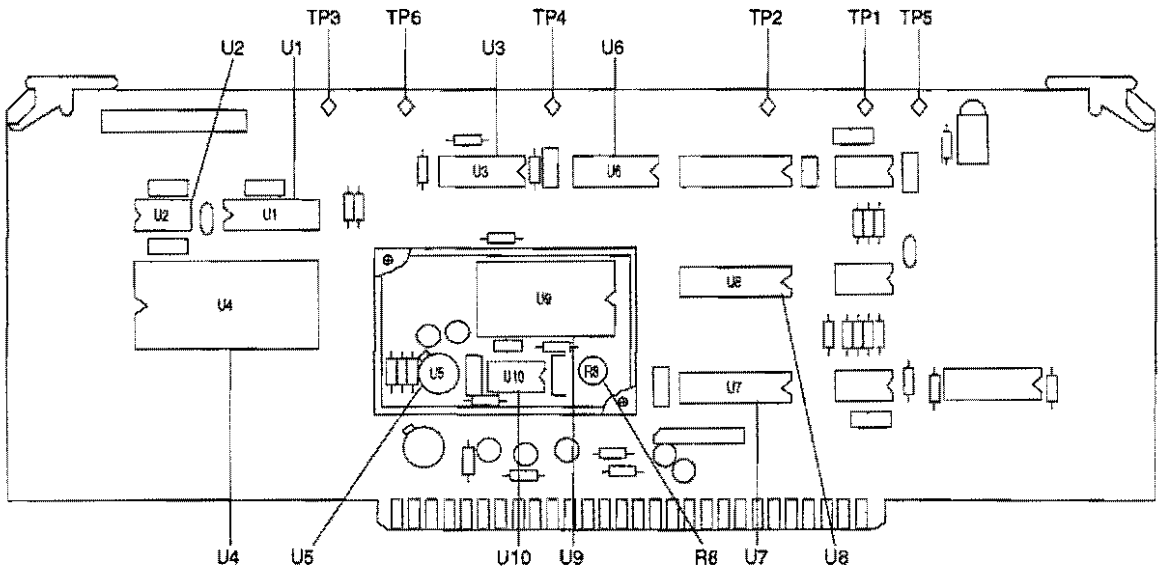


Figure 10-16. *A5 PCB Component Locations*

10-16 A6-A9 YIG OSCILLATOR BANDSWITCH ADJUSTMENTS

The 360SS Series signal sources use three or four YIG driver PCBs, depending on the model. These adjustments should be performed following maintenance on the A6–A9PCBs.

A6 PCB, 2 GHz

Adjust the 2-8 GHz YIG oscillator to bandswitch at 2 GHz, as follows:

Step 1. Set up the test equipment as was shown in Figure 10-15.

Step 2. Remove the top cover.

Step 3. Reset the 360SS by cycling the line power off and on.

Step 4. Move A5P3 jumper to pins 2 and 3 (Figure 10-16).

Step 5. From the controller keyboard, type the following code: (Example is for an HP85 Controller.)

Step 6.
```
10 DISP "SELECT FREQUENCY IN GHZ"
20 INPUT A*
30 OUTPUT 705; "CF1",A,"GHZ"
40 GOTO 10
RUN
```

NOTE

Save the above program to disk; it will be used often throughout the procedures in this chapter.

Step 7. Enter 2 GHz on controller keyboard.

Step 8. Connect the digital multimeter test leads between A6TP5 (+) and A6TP1 (–) (Figure 10-17).

Step 9. Adjust A6R67 counterclockwise for 0V (TTL low).

Step 10. Readjust A6R67 clockwise for +5V (TTL high).

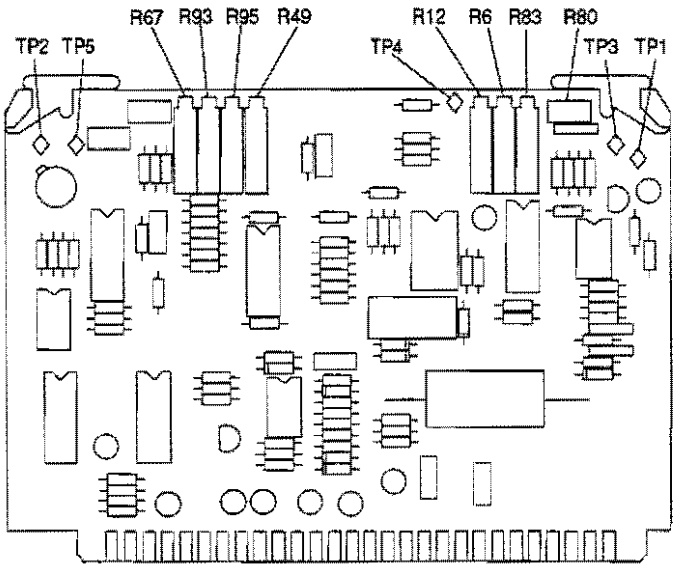


Figure 10-17. *A6 PCB Component Locations*

A6 PCB, 8 GHz

Adjust the 2-8 GHz YIG oscillator to bandswitch at 8 GHz, as follows:

Step 1. Enter 8 GHz on controller keyboard.

Step 2. Move the digital multimeter (+) lead to A6TP3.

Step 3. Adjust A6R49 (Figure 10-17) counterclockwise for 0V (TTL low).

Step 4. Readjust A6R49 clockwise for +5V(TTL high).

A7 PCB

Adjust the 8–12.4 GHz YIG oscillator to bandswitch at 12.4 GHz, as follows:

Step 1. Enter 12.4 GHz on controller keyboard.

Step 2. Connect the digital multimeter test leads between A7TP3 (+) and A7TP1 (–) (Figure 10-18).

Step 3. Adjust A7R49 counterclockwise for 0V (TTL low).

Step 4. Readjust A7R49 clockwise for +5V (TTL high).

A8 PCB

Adjust the 12.4–18 GHz YIG oscillator to bandswitch at 18 GHz, as follows:

Step 1. Enter 18 GHz on controller keyboard.

Step 2. Connect the digital multimeter test leads between A8TP3 (+) and A8TP1 (–) (Figure 10-18).

Step 3. Adjust A8R49 counterclockwise for 0V (TTL low).

Step 4. Readjust A8R49 clockwise for +5V (TTL high).

Step 5. When bandwidth adjustment is completed, move A5P3 jumber to pins 1 and 2.

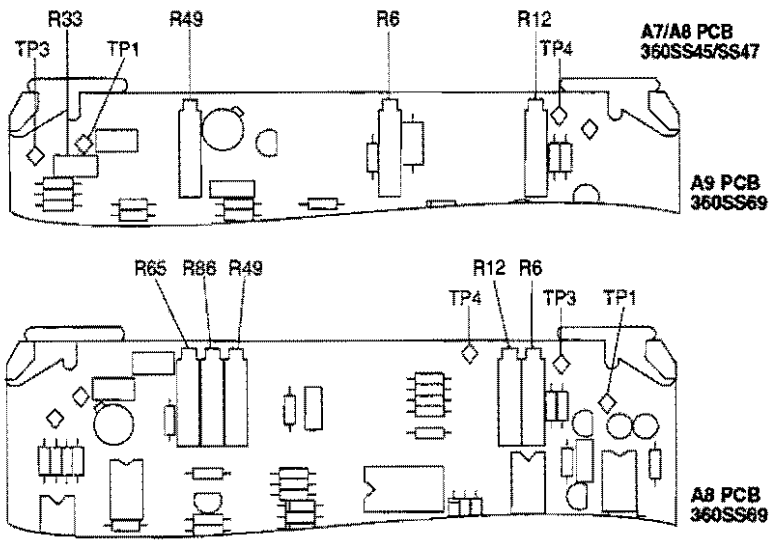


Figure 10-18. *A7 PCB thru A9 PCB Component Locations*

A9 PCB

Adjust the 18–26.5/27.5 GHz YIG oscillator to bandswitch at 26.5 or 27.5 GHz, as follows:

Step 1. Check A1A6 PCB for label indicating bandswitch point. If not there, skip to step 3.

Step 2. On the controller keyboard, enter the bandswitch frequency.

Step 3. Connect the digital multimeter test leads between A9TP3 (+) and A9TP1 (–) (Figure 10-18).

Step 4. On the controller keyboard, enter 26.3 GHz; then increment frequency by 0.1 GHz until DMM switches from 0V to +5V. (That is the bandswitch frequency).

Step 5. Adjust A9R49 counterclockwise for 0V (TTL low).

Step 6. Readjust A9R49 clockwise for +5V (TTL high).

10-17 A6-A9 YIG BIAS CHECK

This paragraph provides instructions for checking YIG oscillator bias voltages.

Step 1. Set up the test equipment as was shown in Figure 10-15.

Step 2. Remove the top cover.

Step 3. Press the POWER switch to ON.

A6 PCB YIG Check the non-adjustable bias voltage on the 2–8 GHz YIG oscillator, as follows:

Step 1. Connect digital multimeter between A6TP4 (+) and A6TP1 (–) (Figure 10-17).

Step 2. Verify voltage is +15V.

Step 3. Move digital multimeter (+) lead to A14P14, pin 15 (Figure 10-23, page 10-73)

Step 4. Verify voltage is –5V.

A7 PCB YIG Check the non-adjustable bias voltage on the 8–12.4 GHz YIG oscillator, as follows:

Step 1. Connect the digital multimeter between A7TP4 (+) and A7TP1 (–) (Figure 10-18).

Step 2. Verify voltage is +15V.

A8 PCB YIG For 360SS47 only, check the non-adjustable bias voltage on the 8–12.4 GHz YIG oscillator, as follows:

Step 1. Connect the digital multimeter between A8TP4 (+) and A8TP1 (–) (Figure 10-18).

Step 2. Verify voltage is +12V.

A9 PCB YIG For 360SS69, check the non-adjustable bias voltage on the 18–26.5 GHz YIG oscillator, as follows:

Step 1. Connect the digital multimeter between A9TP4 (+) and A9TP1 (–) (Figure 10-18).

Step 2. Verify voltage is +12V.

10-18 FREQUENCY ADJUSTMENTS

This paragraph provides instructions for adjusting the signal source output frequency. Frequency adjustment procedures are provided for each YIG-tuned oscillator, and for the Het (heterodyne) Band. The signal source output frequency should be adjusted following maintenance on the A5 and A6 thru A9 PCBs, and when any of the YIG oscillators are replaced.

NOTE

Allow the instrument to warm up 30 minutes before attempting any frequency adjustment.

Step 1. Set up the test equipment as was shown in Figure 10-15.

Step 2. Remove the top cover.

Step 3. Cycle the line power off and on.

Oscillator 1 Adjust the 2–8 GHz oscillator, as follows:

Step 1. Enter 2.1 GHz on controller keyboard.

Step 2. Wait 10 seconds for the frequency to settle.

Step 3. Enter 7.9 GHz on controller keyboard.

Step 4. Wait 10 seconds for the frequency to settle.

Step 5. Repeat steps 1 thru 4 two more times, to set the YIG's hysteresis.

Step 6. Enter 2.1 GHz on controller keyboard.

Step 7. Wait 10 seconds for the frequency to settle.

Step 8. Adjust A6R12 (Figure 10-17) for 2.100 GHz ±2 MHz.

Step 9. Enter 7.9 GHz on controller keyboard.

Step 10. Wait 10 seconds for the frequency to settle.

Step 11. Adjust A6R6 (Figure 10-17) for 7.9 GHz ±2 MHz.

Step 12. Repeat steps 6 thru 11 until the two frequencies are within their 2 MHz tolerance.

0.01 GHz Band

Adjust the 0.01–2 GHz heterodyne band, as follows:

Step 1. Enter 0.01 GHz on controller keyboard.

Step 2. Adjust A6R83 (Figure 10-17) for 1 GHz ±1 MHz.

Step 3. Set the frequency, again, to 1 GHz.

Step 4. Enter 0.01 GHz on controller keyboard.

Step 5. Verify that the counter reads 10 MHz ±10 MHz. If not, readjust A6R12.

Step 6. Enter 1.9 GHz on controller keyboard.

Step 7. Verify that the counter reads 1.9 GHz ±10 MHz. If not, readjust A6R12.

Step 8. Repeat steps 1 thru 7 as necessary until the frequencies at both ends of the heterodyne range are within their ±10 MHz tolerance window.

Oscillator 2

Adjust the 8–12.4 GHz oscillator, as follows:

Step 1. Enter 8.1 GHz on controller keyboard.

Step 2. Wait 10 seconds for the frequency to settle.

Step 3. Enter 12.3 GHz on controller keyboard.

Step 4. Wait 10 seconds for the frequency to settle.

Step 5. Repeat steps 1 thru 4 two more times, to set the YIG's hysteresis.

Step 6. Enter 8.1 GHz on controller keyboard.

Step 7. Wait 10 seconds for the frequency to settle.

Step 8. Adjust A7R12 (Figure 10-18) for 8.1 GHz ±2 MHz.

Step 9. Enter 12.3 GHz on controller keyboard.

Step 10. Wait 10 seconds for the frequency to settle.

Step 11. Adjust A7R6 for 12.3 GHz ±2 MHz.

Step 12. Repeat steps 6 thru 11 until the two frequencies are within their ±2 MHz tolerances.

Oscillator 3 Adjust the 12.4–18 (or 20) GHz oscillator, as follows:

Step 1. Enter 12.5 GHz on controller keyboard.

Step 2. Wait 10 seconds for the frequency to settle.

Step 3. For 360SS69, enter 17.9 GHz on controller keyboard.

For 360SS47, enter 20 GHz on controller keyboard.

Step 4. Wait 10 seconds for the frequency to settle.

Step 5. Repeat steps 1 thru 4 two more times, to set the YIG's hysteresis.

Step 6. Enter 12.5 GHz on controller keyboard.

Step 7. Wait 10 seconds for the frequency to settle.

Step 8. Adjust A8R12 (Figure 10-18) for 12.5 GHz ±2 MHz.

Step 9. For 360SS69, enter 17.9 GHz on controller keyboard.

Step 10. For 360SS47, enter 20 GHz on controller keyboard.

Step 11. Wait 10 seconds for the frequency to settle.

Step 12. Adjust A8R6 (Figure 10-18) for 17.9 GHz ±2 MHz, for the 360SS69; or 20 GHz ±2 MHz, for the 360SS47.

Step 13. Repeat steps 6 thru 11 until the two frequencies are within their ±2 MHz tolerances.

NOTE
Perform the following steps only for the 360SS69.

Step 14. Enter 28 GHz on controller keyboard.

Step 15. Wait 10 seconds for the frequency to settle.

Step 16. Enter 40 GHz on controller keyboard.

Step 17. Wait 10 seconds for the frequency to settle.

Step 18. Repeat steps 14 thru 17 two more times, to set the YIG's hysteresis.

Step 19. Enter 28 GHz on controller keyboard.

Step 20. Wait 10 seconds for the frequency to settle.

Step 21. Adjust A8R68 (Figure 10-18) for 28 GHz ±2 MHz.

Step 22. Enter 40 GHz on controller keyboard.

Step 23. Wait 10 seconds for the frequency to settle.

Step 24. Adjust A8R65 (Figure 10-18) for 40 GHz ±2 MHz.

Step 25. Repeat steps 19 through 24 until the two frequencies are within their ±2 MHz tolerances.

Oscillator 4 For the 360SS69, adjust the 18–26.5 GHz oscillator, as follows:

Step 1. Enter 18.1 GHz on controller keyboard.

Step 2. Wait 10 seconds for the frequency to settle.

Step 3. Enter 26.4 or 27.4 GHz (as determined in paragraph 10-16) on controller keyboard.

Step 4. Wait 10 seconds for the frequency to settle.

Step 5. Repeat steps 1 thru 4 two more times, to set the YIG's hysteresis.

Step 6. Enter1 18.1 GHz on controller keyboard.

Step 7. Wait 10 seconds for the frequency to settle.

Step 8. Adjust A9R12 (Figure 10-18) for 18.1 GHz ±2 MHz.

Step 9. Enter 26.4 or 27.4 GHz, as applicable, on controller keyboard.

Step 10. Wait 10 seconds for the frequency to settle.

Step 11. Adjust A9R6 (Figure 10-18) for 26.5 GHz.

Step 12. Repeat steps 6 through 11 until the two frequencies are within their ±2 MHz tolerances.

10-19 2-8 GHz BAND (OSC 1) TRACKING FILTER ADJUSTMENTS

This paragraph provides instructions for adjusting the 2-8 GHz band (OSC 1) tracking filter. These adjustments should be performed following maintenance on the A6 PCB or when the power output of the signal source is below its specified tolerance in the 2-8 GHz band.

Step 1. Connect the test equipment as was shown in Figure 10-15.

Step 2. Remove the top cover from the signal source.

Step 3. Reset the signal source by cycling the line power off and on.

Step 4. Enter 2.1 GHz on controller keyboard.

Step 5. Set the 360SS for an unleveled output power, type :

```
10 OUTPUT 705;"LVO"
RUN
```

Step 6. Adjust A6R93 (Figure 10-17) for maximum output power.

Step 7. Recall frequency program (page 10-52) and enter 7.9 GHz on controller keyboard.

Step 8. Adjust A6R95 (Figure 10-17) for maximum output power.

Step 9. Repeat steps 4 thru 8 until no further adjustment is necessary.

Step 10. Enter 2.1 GHz on controller keyboard.

Step 11. Verify output power exceeds the RESET power level (+10 dBm for 360SS47 or +5 dBm for 360SS69).

Step 12. Repeat steps 10 and 11 for 3 GHz, 4 GHz, 5 GHz, 6 GHz, and 7 GHz.

10-20 2 GHz BANDSWITCH COMPENSATION ADJUSTMENT

This paragraph provides instructions for adjusting the signal source so that the frequency shift is minimal. Perform this adjustment following maintenance on the A6 PCB, or when a frequency shift is detected. The adjustment consists of setting a resistor to a predetermined point.

Step 1. Turn A6R80 (Figure 10-17) clockwise for a full rotation .

Step 2. Turn A6R80 counterclockwise 1/8 of a rotation.

10-21 ALC LOOP ADJUSTMENTS

This paragraph describes the ALC (automatic level control) loop adjustments. It also provides instructions for adjusting the ALC. Perform the ALC loop adjustment procedures following the repair or replacement of any ALC loop components.

ALC Loop Bandwidth

Adjust the ALC loop bandwidth as follows:

Step 1. Set up the test equipment as shown in Figure 10-19.

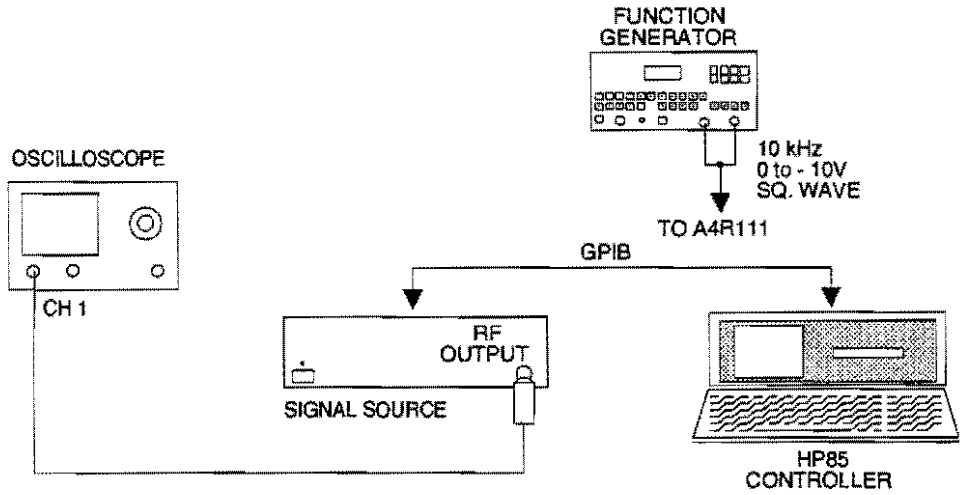


Figure 10-19. *Test Equipment Setup for ALC Loop Confidence Test*

Step 2. Remove the top cover.

Step 3. Withdraw the A4 PCB and clip the center conductor lead on the function generator output to the bottom of A4R111 (Figure 10-20). Clip the shield lead to A4TP2.

Step 4. Reinstall the A4 PCB and press the POWER switch to ON.

NOTE

Steps 5 through 9 describe how to adjust the function generator for a 10 kHz squarewave at a voltage that causes a 10 dB excursion of the signal source output signal.

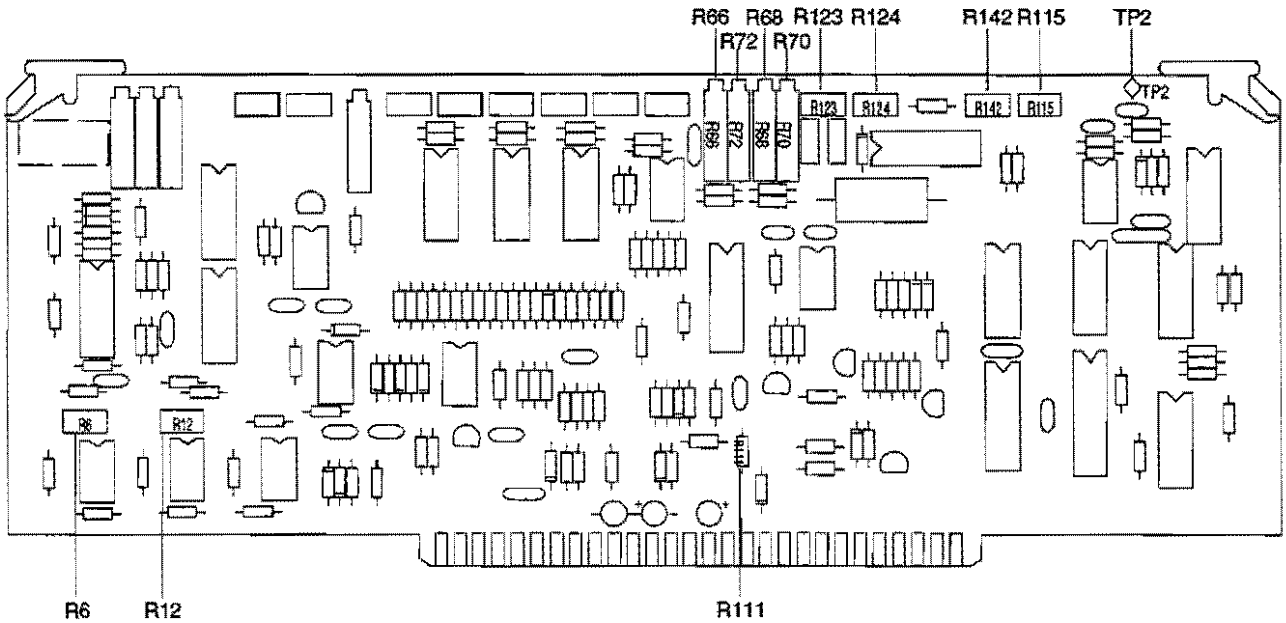


Figure 10-20. *A4 PCB Component Locations*

Step 5. Turn the function generator off.

Step 6. Adjust the oscilloscope vertical controls to position the trace on the bottom graticule line. This is now the reference line for the maximum-output power signal from the signal source.

Step 7. Set the output power 10 dB below the reset output power by typing the below listed HP-85 BASIC code on the controller keyboard. (Substitute the reset output power value for the term X. This value is 10 dBm for 360SS47 or +5 dBm for 360SS69.)

```
10 OUTPUT 705;"LVLXDB"
RUN
```

Step 8. Observe that the oscilloscope trace deflects upward, and note the graticule line that the trace rests on. This graticule line is now the reference for the minimum output power signal.

Step 9. Turn on the function generator and set the function and frequency controls to produce a 10 kHz squarewave.

Step 10. Adjust the amplitude and dc offset controls to position the top of the squarewave on the minimum-power reference line. Position the bottom of the squarewave on the maximum-power reference line.

Osc 1 (A4/A6 PCBs) Loop

Adjust the A4/A6 PCB ALC loop bandwidth as follows:

Step 1. Recall frequency program (page 10-52) and enter 5 GHz on controller keyboard.

Step 2. Adjust the oscilloscope vertical and horizontal controls to display a square wave similar to that shown in Figure 10-21.

Step 3. Adjust A4R123 (Figure 10-20) and A6R33 (Figure 10-17) for a squarewave with minimum overshoot.

Het Band (A4/A6 PCBs) Loop

Adjust the A4/A6 PCB heterodyne ALC loop bandwidth as follows:

Step 1. Enter 1 GHz on controller keyboard.

Step 2. Adjust the vertical and horizontal oscilloscope controls to display a squarewave similar to that shown in Figure 10-21.

Step 3. Adjust A4R124 (Figure 10-20) and A6R66 (Figure 10-17) for a square wave with minimum overshoot. (Recheck the adjustment at 5 GHz.

Osc 2 (A7 PCB) Loop

Adjust the A7 PCB ALC loop bandwidth as follows:

Step 1. Enter 10 GHz on controller keyboard.

Step 2. Adjust A7R33 (Figure 10-18) for the best square wave response (least distortion).

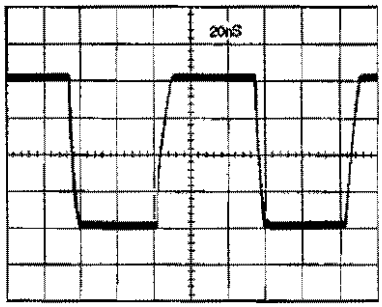


Figure 10-21. ALC Loop Adjustment Square Wave

Osc 3 (A8 PCB) Loop

Adjust the A8 PCB ALC loop bandwidth as follows:

Step 1. Enter 15 GHz on controller keyboard.

Step 2. Adjust A8R33 (Figure 10-18) for a square wave with minimum overshoot.

Step 3. If 360SS69, continue to OSC 4 (A9 PCB) Loop. If 360SS47, turn line power off, withdraw the A4 PCB, and disconnect the function generator.

Step 4. Reinstall the A4 PCB and press the POWER switch back to ON.

Osc 4 (A9 PCB) Loop

Adjust the A9 PCB ALC loop bandwidth as follows:

Step 1. Enter 22 GHz on controller keyboard.

Step 2. Adjust A9R33 (Figure 10-18) for a square wave with minimum overshoot.

Step 3. Turn the line power off, withdraw the A4 PCB and disconnect the function generator.

Step 4. Reinstall the A4 PCB and press the POWER switch back to ON.

Low Level Noise

Adjust low-level noise on the A4 PCB, as follows:

NOTE
Perform this adjustment only if A4 PCB has been replaced.

Step 1. Enter 2.1 GHz on controller keyboard.

Step 2. Adjust A4R12 (Figure 10-20) for minimum jitter (amplitude variations), as indicated on the oscilloscope.

Step 3. Enter 7.9 GHz on controller keyboard.

Step 4. Adjust A4R6 for minimum jitter.

Power Level

Adjust output power as follows:

Step 1. Reset the 360SS by cycling the line power off and on.

Step 2. Enter 2.1 GHz on controller keyboard.

Step 3. For the 360SS69:

a. Adjust A4R66 (Figure 10-20) for +5 dBm ±0.5 dB.

b. Set the output power to –5 dBm, type:

```
10 OUTPUT 705;"LVL-5DM"
RUN
```

c. Adjust A4R72 (Figure 10-20) for –5 dBm ±0.5 dB.

Step 4. For the 360SS47:

a. Adjust A4R66 (Figure 10-20) for +10 dBm ±0.5 dB.

b. Set the output power to 0 dBm, type:

```
10 OUTPUT 705;"LVL10DM"
RUN
```

c. Adjust A4R72 (Figure 10-20) for 10 dBm ±0.5 dB.

RF Slope

Adjust the slope of the RF output power, as follows:

Step 1. For the 360SS47:

a. Set the frequency to 20 GHz, type:

```
10 OUTPUT 705;"CF120GH"
RUN
```

b. Set the power to 10 dBm, type:

```
10 OUTPUT 705;"LVL10DM"
RUN
```

c. Adjust A4R66 (Figure 10-20) for +10 dBm ±0.5 dB.

d. Repeat step 1(a) for 2.1 GHz and verify that the power level is 10 dBm. If not, readjust A4R66 as required.

Step 2. For the 360SS45/SS69:

a. Set the frequency to 40 GHz, type:

```
10 OUTPUT 705;"CF140GH"
RUN
```

b. Set the power to 5 dBm, type:

```
10 OUTPUT 705;"LVL5DM"
RUN
```

c. Adjust A4R66 (Figure 10-20) for +5 dBm ±0.5 dB.

d. Repeat step 2(a) for 2.1 GHz and verify that the power level is 5 dBm. If not, readjust A4R66 as required.

10-22 POWER SUPPLY ADJUSTMENTS

This paragraph provides instructions for adjusting the OUT OF REG, HIGH LINE, and LOW LINE motherboard adjustments. They should be made (1) if power supply problems are suspected or (2) after maintenance has been performed on any of the A13/A14 power supply circuits.

Out-of-Regulation

Adjust the out-of-regulation potentiometer as follows:

Step 1. Adjust A14R89 (Figure 10-23) clockwise to its limit.

Step 2. While observing the A14 OUT OF REG indicator, readjust A14R89 counterclockwise until the indicator goes out. Stop.

Step 3. While counting the number of potentiometer turns, continue to adjust A14R89 counterclockwise until the indicator lights. Stop.

Step 4. Readjust A14R89 clockwise, halfway between the indicator's on and off states.

Low Line Voltage

Adjust the low-line potentiometer as follows:

Step 1. Turn off the 360SS.

Step 2. Connect the test equipment as shown in Figure 10-22.

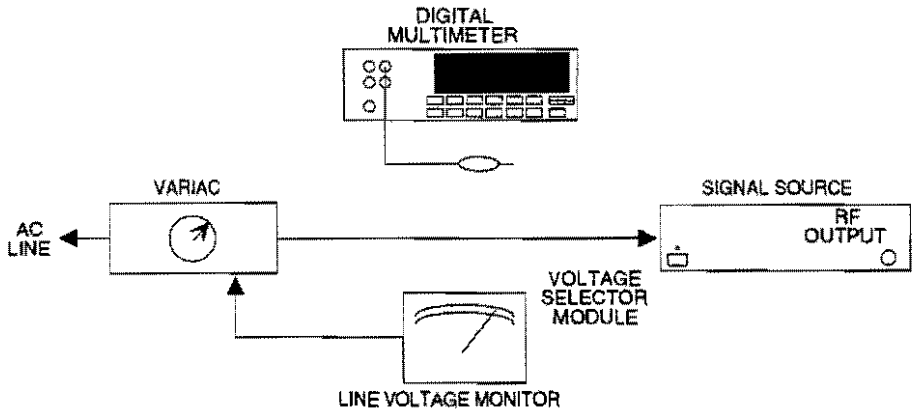


Figure 10-22. *Test Equipment Setup for Power Supply Adjustments*

Step 3. Adjust the variac for 92 Vac (20% below the nominal line voltage), as observed on the line voltage monitor.

Step 4. Turn on the 360SS.

Step 5. Adjust A14R79 (LOW) (Figure 10-23) to its clockwise limit; then readjust counterclockwise until the A14 LOW LINE indicator lights.

Step 6. Readjust the variac for 115 Vac (nominal line voltage), and ensure that the LOW LINE indicator is not lit.

High Line Voltage

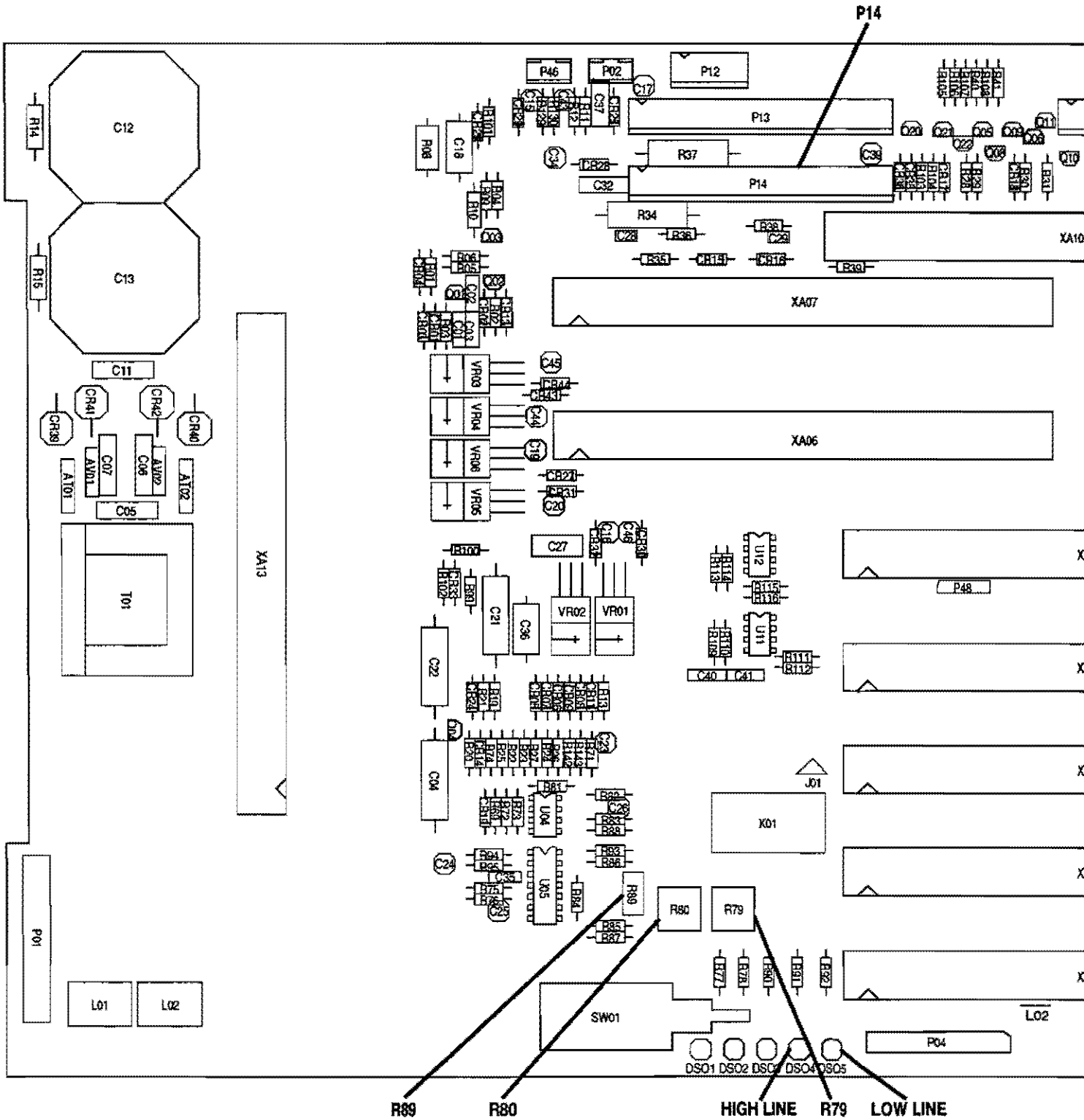
Adjust the high-line potentiometer as follows:

Step 1. Connect the test equipment as was shown in Figure 10-22.

Step 2. Adjust the variac for 138 Vac (20% above the nominal line voltage).

Step 3. Adjust A14R80 (HIGH) (Figure 10-23) to its clockwise limit; then readjust counterclockwise until the HIGH LINE indicator lights.

Step 4. Readjust the variac for 115 Vac (nominal line voltage), and ensure that the HIGH LINE indicator is not lit.


P14
R89
R80
HIGH LINE
R79
LOW LINE
C12
C13
C11
R14
R15
T01
XA13
P01
L01
L02
P46
P02
P12
P13
P14
XA10
XA07
XA06
P48
P04
SW01
X01
J01
VR01
VR02
VR03
VR04
VR05
VR06
U04
U05
U11
U12
DSO1 DSO2 DSO3 DSO4 DSO5

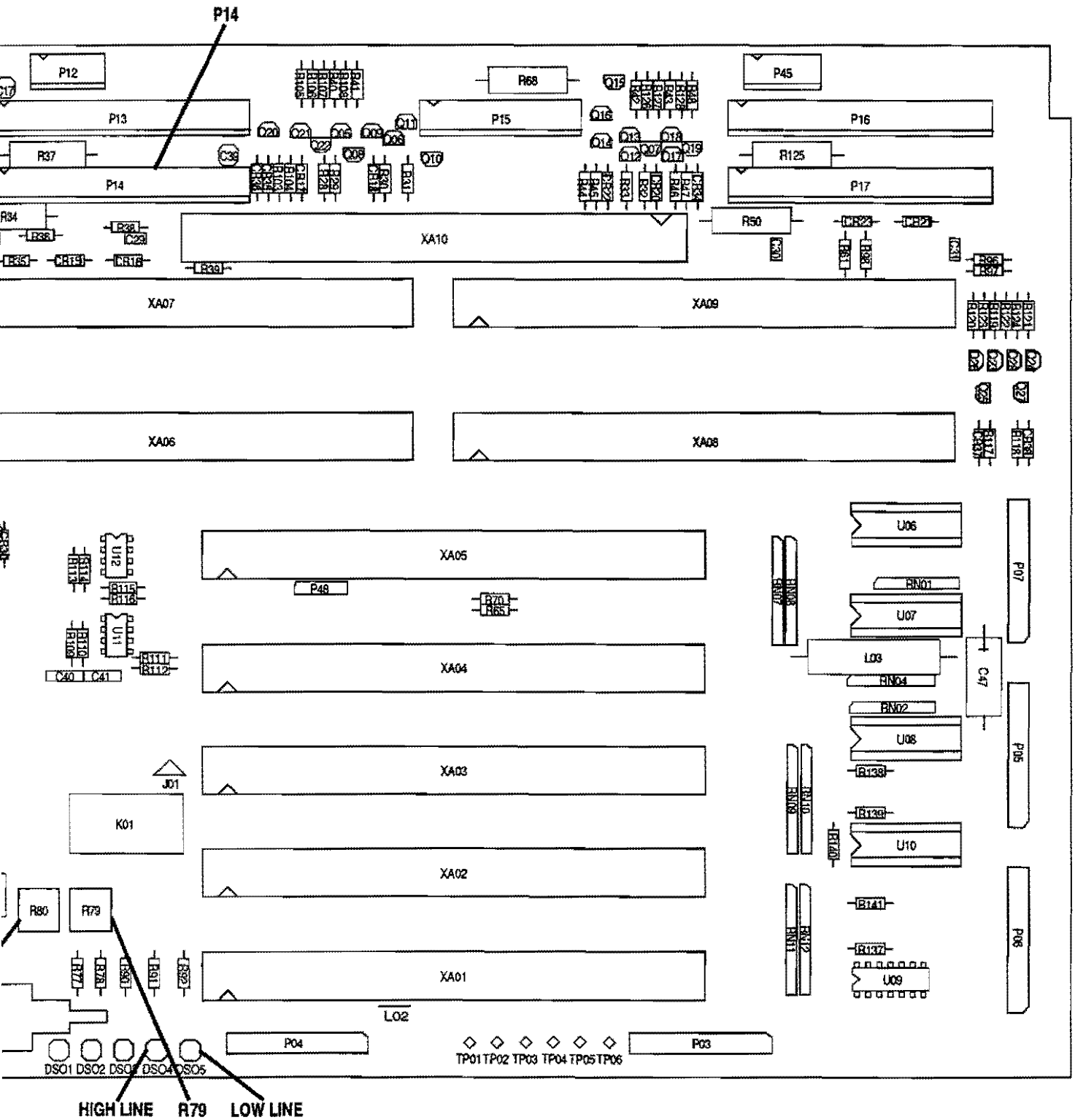


Figure 10-23. *A14 Motherboard PCB, Test Po*
Connector, Indicator, and Adjustment Locations

10-23 REMOVE AND REPLACE PROCEDURES

Procedures for removing and replacing signal source subassemblies listed in Table 1-2 are provide in subsequent paragraphs.

10-24 REMOVE AND REPLACE COVERS

This paragraph provides instructions for removing top, bottom, and side covers. To replace covers, reverse the removal process.

Procedure

Top and Bottom Covers

Step 1. Turn off ac power and disconnect the input line voltage.

Step 2. On rear panel, loosen screws and remove the feet from the four corners.

Step 3. Slide the top and bottom covers toward the rear and remove.

Side Covers

Step 1. Remove top and bottom covers.

Step 2. Grasp rack-slide handle at front, and slide side panels to the rear and remove.

10-25 REMOVE AND REPLACE PCBS (EXCEPT A13)

This paragraph describes how to remove the the signal source PCBs, all but the A13. It is covered in the next paragraph. To replace these PCBs, reverse the removal process.

Preleminary Remove top cover (paragraph 10-24).

Procedure

Step 1. Loosen captive screw and lift PCB retaining bracket out of the way.

Step 2. Lift up on edge tabs and pull PCB straight up and out.

CAUTION

All of the referenced PCBs contain static-sensitive components. Refer to Figure 1-2, page 1-10, for precautionary instructions. Failure to follow these instructions may result in damage to the PCB.

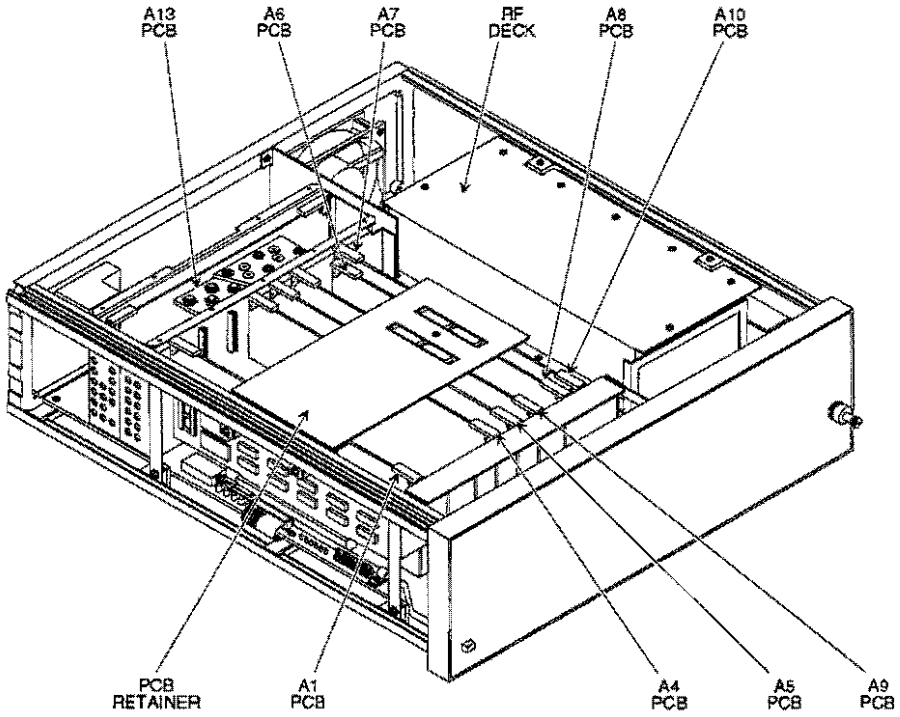


Figure 10-24. *360SSXX PCB Locations*

10-26 REMOVE AND REPLACE A13 SWITCHING POWER SUPPLY PCB

This paragraph describes how to remove the A13 Switching Power Supply PCB. To replace this PCBs, reverse the removal process.

NOTE

Refer to figure 10-24 for PCB location.

WARNING

Voltages hazardous to life are present through the A13/A14 Switching Power Supply, even when you have the power turned off and the ac line cord removed. Before performing maintenance on this power supply, observe the following precautions: After turning the ac power off and removing the line cord, allow 5 minutes for the capacitor voltages to decay. Avoid touching the terminals on the line fuse when power is on, +165 Vdc is present.

CAUTION

The referenced PCB contains static-sensitive components. Refer to Figure 1-2, page 1-10, for precautionary instructions. Failure to follow these instructions may result in damage to the PCB.

Preliminary Remove top cover (paragraph 10-24).

Procedure

Step 1. Remove ten screws and lockwashers from the top cover of the card-cage assembly, and remove the cover.

Step 2. Lift up on edge tabs and pull PCB straight up and out.

NOTE

The A13 PCB power supply switching-frequency is in the RF spectrum (50 kHz). To prevent the radiation, insure that the card-cage cover is securely seated and fastened with *all ten screws* before reapplying the ac power.

10-27 REMOVE AND REPLACE A YIG OSCILLATOR

This paragraph describes how to remove and replace a typical YIG oscillator. To replace the oscillator, reverse the removal process.

NOTE

Refer to Figure 10-25 for 360SS47 and Figure 10-26 for 360SS69 components locations.

Preliminary Remove all four covers (paragraph 10-24).

Procedure

Step 1. Remove the RF deck cover by removing six screws, lockwashers, and flat washers from inside edge and seven screws and lockwashers from front, back, and outside edges.

Step 2. For 2–8 GHz oscillator

- ☐ Remove connector from Match Modulator output. Leave match modulator attached, it is included with replacement oscillator.
- ☐ Remove connector from P14 on motherboard.
- ☐ Remove two screws from oscillator bottom and remove oscillator.

Step 3. For 8-12 GHz oscillator:

- ☐ Remove connector from Isolator output. (For 360SS69, remove the cable/filter assy between the Isolator and DPDT PIN switch.)
- ☐ Remove connector from P13 on motherboard.
- ☐ Remove two screws from oscillator bottom and remove oscillator.

Step 4. For 12–18GHz (360SS69) or 12–20 GHz (360SS47) oscillator:

- ☐ Remove cable from between oscillator output and DPDT PIN switch.
- ☐ Remove connector from P16 on motherboard.
- ☐ Remove two screws from oscillator bottom and remove oscillator.

Step 5. For 18–26.5 GHz oscillator (360SS69):

- ☐ Remove cable from between oscillator output and multi-port PIN switch.
- ☐ Remove connector from P17 on motherboard.
- ☐ Remove two screws from oscillator bottom and remove oscillator.

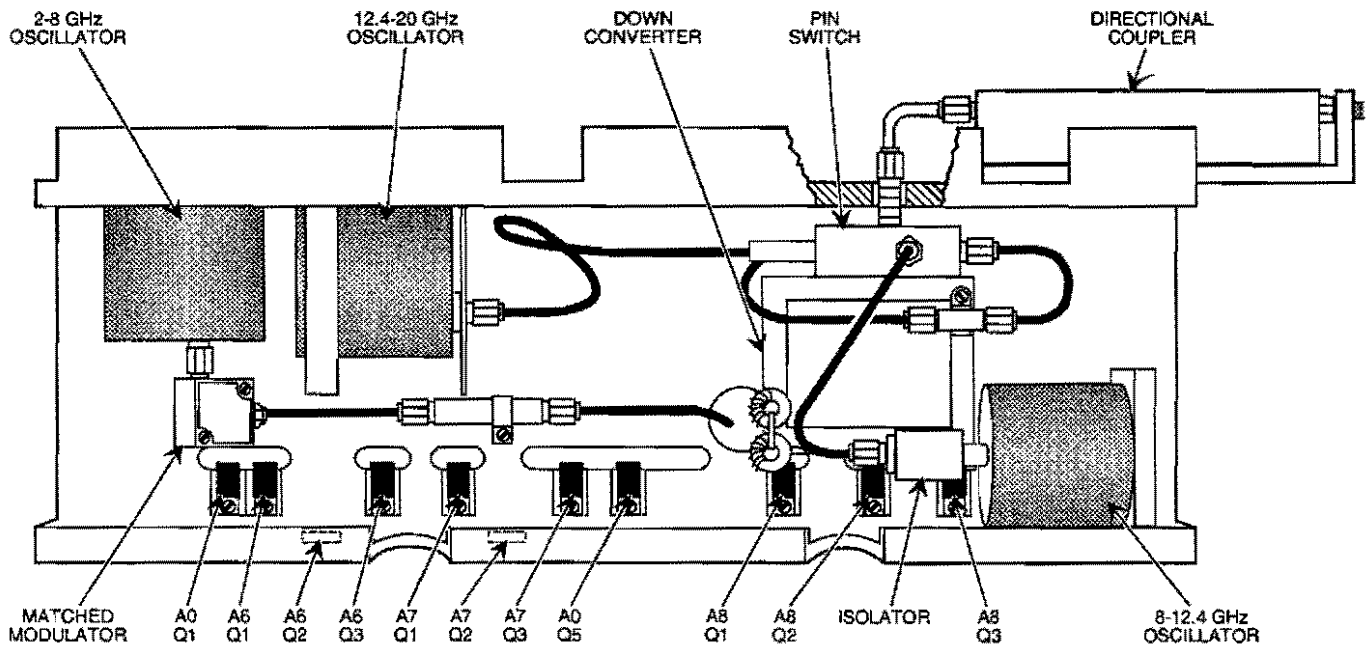


Figure 10-25. *360SS47 RF Deck Component Locations*

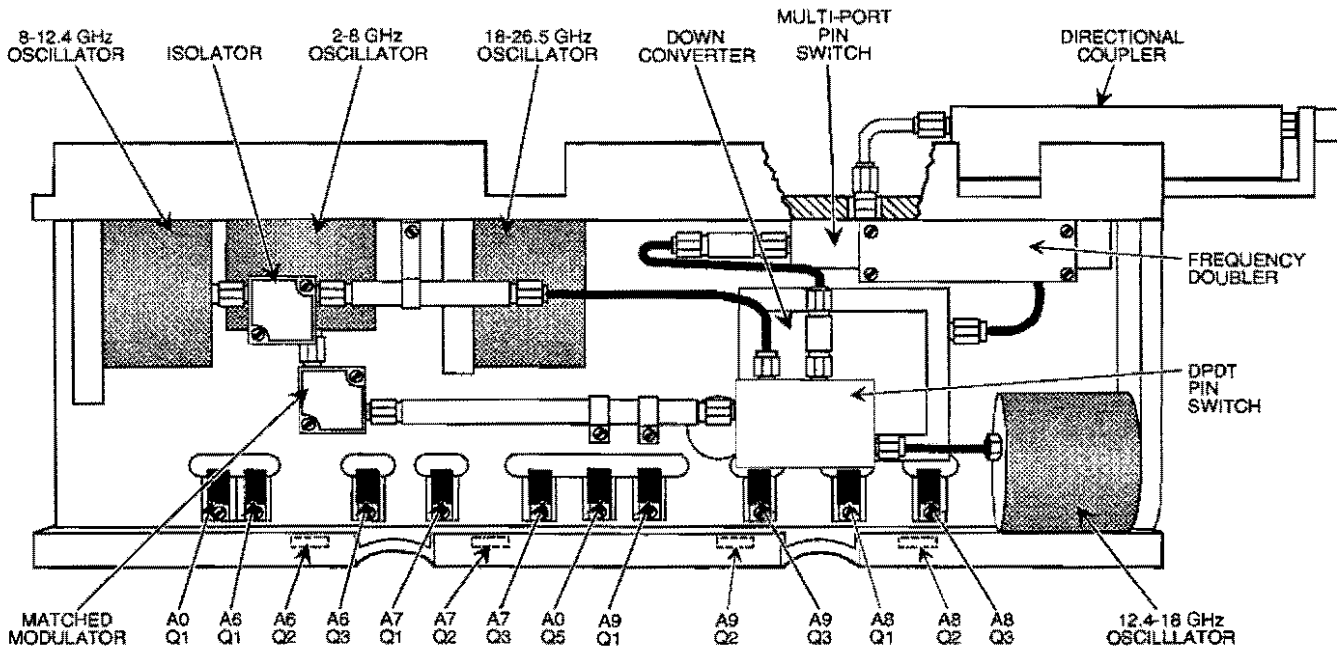


Figure 10-26. *360SS69 RF Deck Component Locations*

10-28 REMOVE AND REPLACE A PIN SWITCH

This paragraph describes how to remove a PIN switch.To replace the PIN switch, reverse the removal process.

NOTE

Refer to figure 10-25 or 10-26 for component location.

Preliminary Remove all four covers (paragraph 10-24).

Procedure

Step 1. Remove the RF deck cover by removing six screws, lockwashers, and flat washers from inside edge and seven screws and lockwashers from front, back, and outside edges.

Step 2. For the 360SS47:

- ☐ Remove five RF cable connectors.
- ☐ Remove connector from P15 on motherboard.
- ☐ Remove two mounting screws from the backside of the RF deck.
- ☐ Remove the switch and standoffs.
- ☐ Remove two screws and lockwashers and remove standoffs; save standoffs for use on replacement switch.

Step 3. For 360SS69 multi-port PIN switch:

- ☐ Remove the frequency doubler (paragraph 10-31) to gain access.
- ☐ Remove six cable connectors.
- ☐ Proceed as described above for 360SS47.

Step 4. For 360SS69 DPDT PIN switch:

- ☐ Remove six cable connectors.
- ☐ Remove connector from P45 on motherboard.
- ☐ Remove the switch.

10-29 REMOVE AND REPLACE THE DIRECTIONAL COUPLER

This paragraph describes how to remove the directional coupler. To replace this component, reverse the removal process.

NOTE

Refer to figure 10-25 or 10-26 for component location.

Preliminary Remove all four covers (paragraph 10-24).

Procedure

Step 1. Remove the RF deck cover by removing six screws, lockwashers, and flat washers from inside edge and seven screws and lockwashers from front, back, and outside edges.

Step 2. For 360SS47:

- ☐ Remove black cable connector from DC OUT on coupler and pull black wire away from adjacent pin.
- ☐ Remove two RF cable connectors from coupler.
- ☐ Remove two screws and remove coupler.

Step 3. For 360SS69:

- ☐ Remove black cable connector from DC OUT on coupler and pull black wire away from adjacent pin.
- ☐ Remove connector from RF IN on coupler
- ☐ Remove two screws; pull directional coupler back to free output connector, then remove.

10-30 REMOVE AND REPLACE THE DOWN CONVERTER

This paragraph describes how to remove the down converter. To replace this component, reverse the removal process.

NOTE

Refer to figure 10-25 or 10-26 for component location.

Preliminary Remove all four covers (paragraph 10-24).

Procedure

Step 1. Remove the RF deck cover by removing six screws, lockwashers, and flat washers from inside edge and seven screws and lockwashers from front, back, and outside edges.

Step 2. For 360SS47:

- ☐ Remove two RF cable connectors.
- ☐ Remove connector from P12 on motherboard.
- ☐ Remove two mounting screws from the underside of the RF deck.
- ☐ Remove the down converter.

Step 3. For 360SS69:

- ☐ Remove DPDT PIN switch (paragraph 10-28) to gain access.
- ☐ Remove two RF cable connectors.
- ☐ Remove connector from P12 on motherboard.
- ☐ Remove two mounting screws from the underside of the RF deck.
- ☐ Remove the down converter.

10-31 REMOVE AND REPLACE THE FREQUENCY DOUBLER

This paragraph describes how to remove the frequency doubler on the 360SS69. To replace this component, reverse the removal process.

NOTE

Refer to Figure 10-26 for component location.

Preliminary Remove all four covers (paragraph 10-24).

Procedure

Step 1. Remove the RF deck cover by removing six screws, lockwashers, and flat washers from inside edge and seven screws and lockwashers from front, back, and outside edges.

Step 2. Remove two RF cable connectors.

Step 3. Remove two screws, and remove the frequency doubler.

Appendix A
Model 363XA Test Set Operation

Table of Contents

Appendix A
Model 363XA Test Set Operation

A-1 INTRODUCTION

The 363XA Frequency Converter Test Sets are user configurable and can be used to address a wide variety of applications that include: frequency conversion devices (mixers), antenna and radar cross section, and high power S-parameters. This appendix describes these applications and provides operating instructions for a variety of test applications.

A-2 POWER LEVEL CONSIDERATIONS

Power level inputs to the 363XA should be less than –10 dBm at all inputs to avoid compression in the output signals. The reference signal selected for phase lock should be between –10 and –25 dBm. A convenient signal for the reference is available at the source lock output connector.

A-3 360B SYSTEM CONFIGURATIONS USING 363XA TEST SETS

Examples of the use of the 363XA in the 360 Vector Network Analyzer system are discussed in the following paragraphs.

Antenna Test A simple antenna test setup for short distance measurements to 40 GHz is shown in Figure A-1. The source is placed at the transmit antenna and the test set at receive antenna. The 360 VNA unit can be remote up to 30 feet from the test set, allowing the source and test set to be placed in the chamber with the antennas.

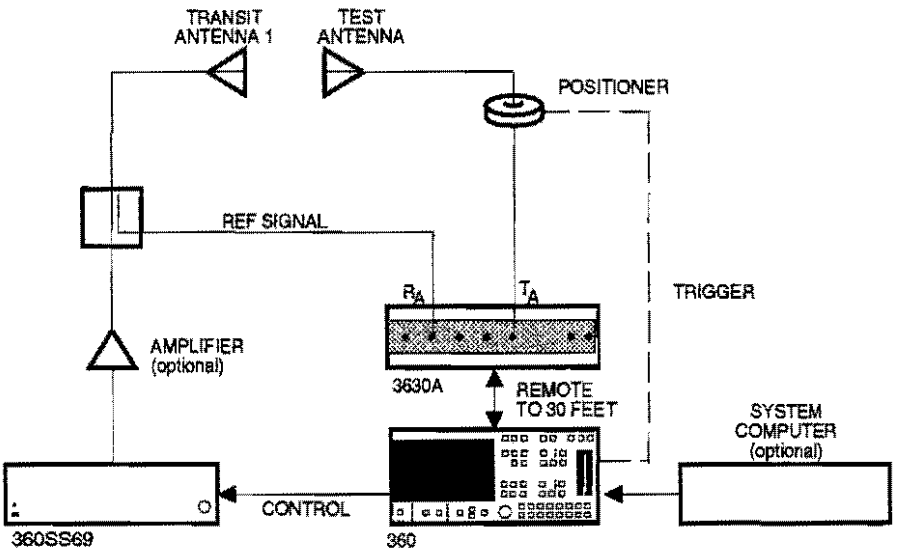


Figure A-1. *Short Distance Antenna Test Range*

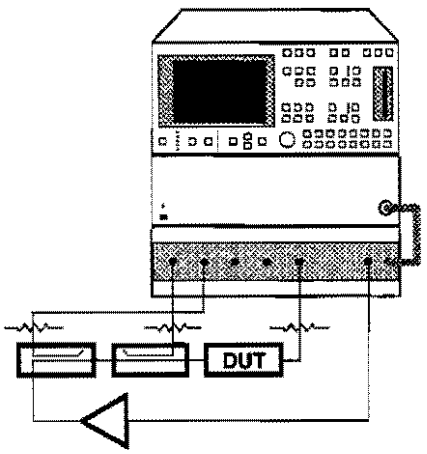


Figure A-2. S-Parameter Measurement of a High Power Device

S_{11} and S_{21} Measurement of High Power Device

A device-under-test (DUT) that requires high input power can be tested as shown in Figure A-2. Here signal R_A is not fed from the source lock output, but rather from the output of the amplifier. Care must be taken not to exceed the maximum linear operation input level. During calibration, RF input to the amplifier is attenuated so that the maximum input level into T_A is not exceeded when Opens and Shorts from the calibration standards are connected.

Using the 3630A/3631A Attenuator/ Switch Drivers

The 3630A and 3631A Frequency Converter Test Sets contain three connectors on the rear panel (Figure A-3) that are configured to drive two step attenuators and a transfer switch. Using these connectors and WILTRON components, it is possible to configure a 3630A or 3631A for many different applications. Figure A-4 (next page) shows a 3630A configured for full reversing S-Parameter measurement.

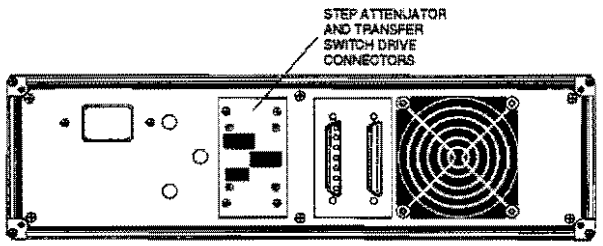


Figure A-3. 363XA Test Set Rear Panel

The attenuator drive voltages are consistant with many of the available microwave switches. This makes the 3630A useful for applications requiring external signal switching (Figure A-5). Table A-1 provides pin configuration for the attenuator drive connectors.

Table A-1. Attenuator Drive Connector Pin Configuration

Pin	Attenuation Control	External Switch Control
1	—	—
2	10 dB IN	SWITCH 1, POSITION 2 (ON)
3	40 dB OUT	SWITCH 3, POSITION 1 (OFF)
4	—	—
5	20 dB IN	SWITCH 2, POSITION 2 (ON)
6	+24 Vdc	+24 Vdc
7	—	—
8	—	—
9	40 dB IN	SWITCH 3 POSITION 2 (ON)
10	—	—
11	20 dB OUT	SWITCH 2, POSITION 1 (OFF)
12	—	—
13	10 dB OUT	SWITCH 1, POSITION 1 (OFF)
14	—	—

The switches are controlled by the attenuator control in the Reduced Test Signals menu. When the appropriate attenuation is selected, the corresponding pin of the connector is grounded. It is possible to place any of the three switches in either position by specifying the appropriate attenuator setting. Specifying 10 dB would set switch 1 to on, 20 dB would set switch 2 to on, 30 dB would set switches 1 and 2 to on, etc.

Note that the Port 2 Test Attenuator control is only 0 to 40 dB. This means, when driving external switches, it is impossible to turn all 3 switches on at the same time through that connector.

Fiqure A-6 shows how the Port 2 Source Attenuator connector could be connected to control three HP33311 switches. Note the switching method and control voltage are both compatible, meaning no interface circuitry is needed.

With the 3630A and 3631A external switch control connectors, it is possible to configure a number of automated measurements without requiring manual switch control.

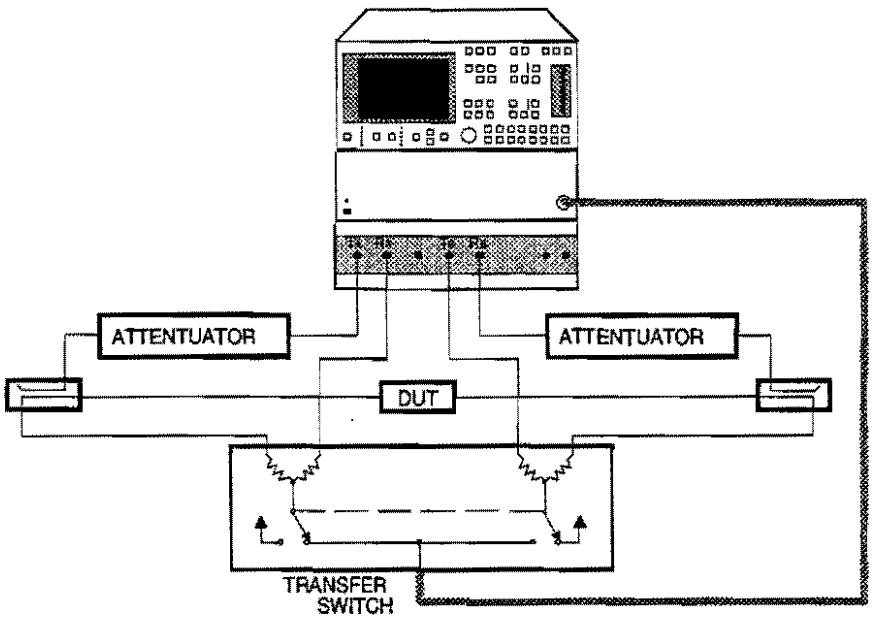


Figure A-4. *36X3A Configured to Measure Full Reversing S-Parameters*

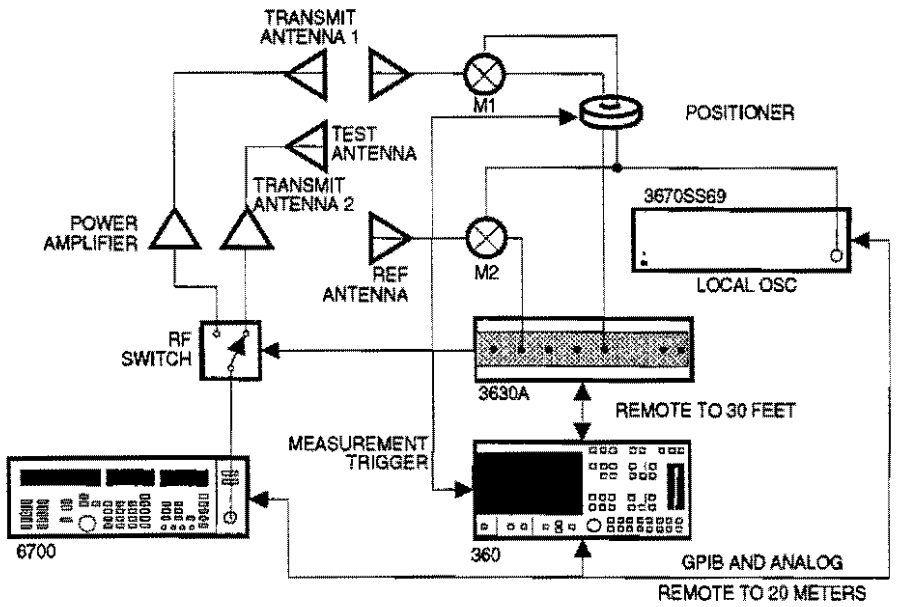


Figure A-5. *Switched Transmit Antennas*

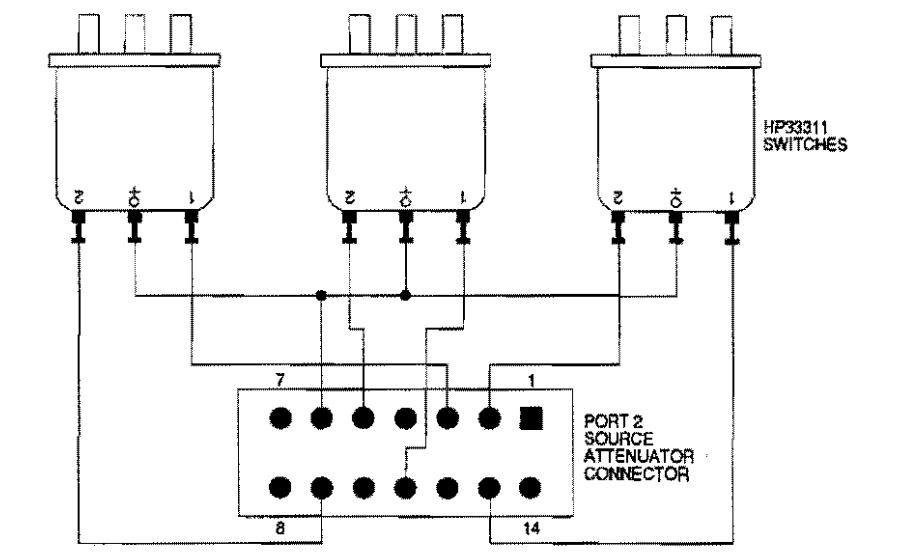


Figure A-6. *Port 2 Source Attenuator Connector Controlling Three HP33311 Switches*

A-4 OPERATION

The 363XA Frequency Converter Test set is operated under VNA program control during measurements. This section provides information on setting up the VNA to present measurement data provided by the test set.

Table A-2. S-Parameter Definitions

S Param.	Multi-Port Ratio	Meas. Chan. Ratio	Meas. Def.
S_{11}	$\frac{b1}{a1}$	$\frac{T_A}{R_A}$	Forward Reflection
S_{11}	$\frac{b1}{a2}$	$\frac{T_A}{R_B}$	Reverse Transmission
S_{11}	$\frac{b2}{a1}$	$\frac{T_B}{R_A}$	Forward Transmission
S_{11}	$\frac{b2}{a2}$	$\frac{T_B}{R_B}$	Reverse Reflection

Preoperational Setup, Discussion

When a fully reversing test set is used with the 360B VNA system, the system ratios the relative magnitude and phase of the S-parameter values for the DUT. These S-parameters are equivalent to the "Multi-Port Ratios" given in Table A-2.

Within fully reversing test sets, signal separation and down conversion of the incident, reflected, and transmitted signals at PORT 1 and PORT 2 result in four IF signals. They are defined as:

- R_A (Reference, Channel A) – this signal contains information about the stimulus signal in the forward direction (incident signal) from PORT 1 to the DUT.
- T_A (Test, Channel A) – in the forward measurement mode, this signal contains information about the reflected signal from the DUT back to PORT 1. In the reverse measurement mode, this signal contains information about the transmitted signal from the DUT to PORT 1.
- R_B (Reference, Channel B) – this signal contains information about the stimulus signal in the reverse direction (incident signal) from PORT 2 to the DUT.
- T_B (Test, Channel B) – in the forward measurement mode, this signal contains information about the transmitted signal from the DUT to PORT 2. In the reverse measurement mode, this signal contains information about the reflected signal form the DUT back to PORT 2.

The IF signal ratios that are equivalent to the "S-Param." and "Multi-Port Ratios" are listed in Table A-2 in the column headed "Meas. Chan. Ratio."

However, the front-panel nomemclature for the test signals applied to it is consistent with the nomenclature of the IF signal channels of a reversing test set (R_A, T_A, R_B, T_B).

The 360B VNA system can measure the ratio of any two of the test signals applied to the 363XA test set. The ratio need not be an S-parameter. Either R_A or R_B can be selected as the reference signal.

The operator must define the ratio he wants to measure by choosing among items presented on a series of menus shown on the VNA display screen. The nomenclature used in these menus is consistent with front panel nomenclature of the 363XA test set. For purposes of setting-up the VNA for making a measurement using the 363XA test set, the following is true:

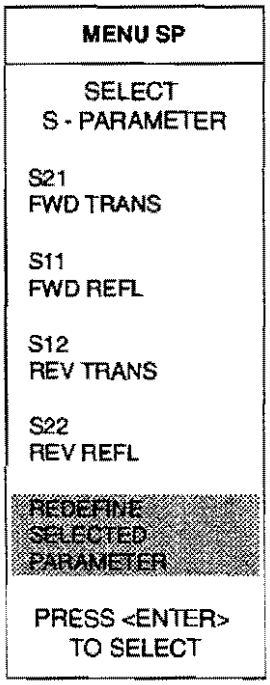
- a1 is comparable to R_A
- a2 is comparable to R_B
- b1 is comparable to T_A
- b2 is comparable to T_B

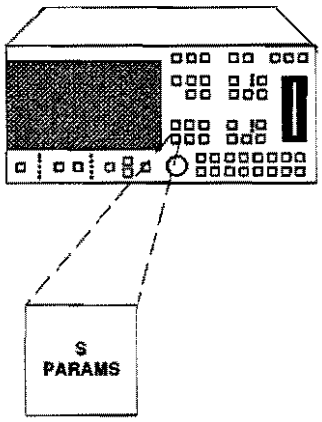
Preoperational Setup Procedure

After the 363XA has been installed in the 360B VNA system and the system is turned on, the VNA will probably display four S-parameters on the screen. Although this is consistent with a standard reversing test set, the 363XA Frequency Converter Test Set is not usually used in this mode. Therefore, the VNA should be put in single (or dual) channel mode consistent with the phase lock signal connection (R_A or R_B).

Define the signal configuration using the menus provided on the 360 VNA as follows:

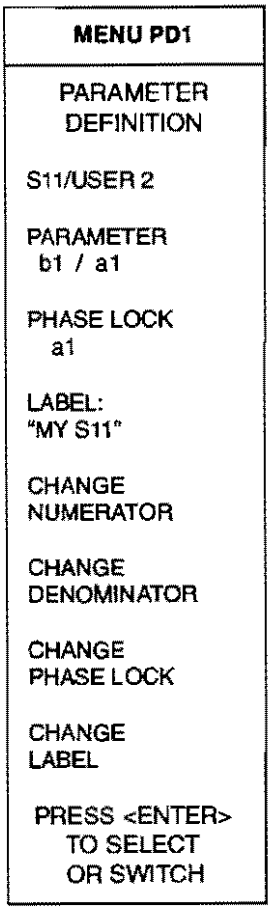
Step 1. Press the front panel S-PARAMS key on the 360B VNA (below). This brings menu SP (left) to the screen.





Step 2. Select the parameter to be redefined by moving the cursor next to the parameter and pressing ENTER.

Step 3. Select the **REDEFINE SELECTED PARAMETER** menu option and press ENTER. This brings the menu PD1.

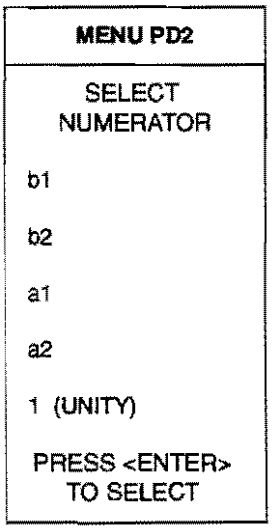


Step 4. With the cursor next to the selected parameter at the top of the menu press ENTER, to toggle to **USER 2**.

Note the following:

- The definition of the parameter to be measured is shown as a ratio of terms of measurement characteristic of a multiport device (a1, a2, b1, b2) under **PARAMETER**.
- The selected phase lock reference is shown under **PHASE LOCK**.
- The name assigned the measurement parameter is shown under **LABEL**.

Each of the above can be changed to suit the conditions of the measurement.



Change Measured Parameter Definition

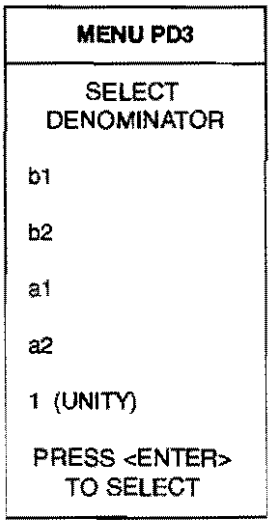
The definition of the measured parameter can be changed by changing the numerator, the denominator, or both. Change the numerator as follows:

Step 1. Move the cursor to **PARAMETER** then press ENTER.

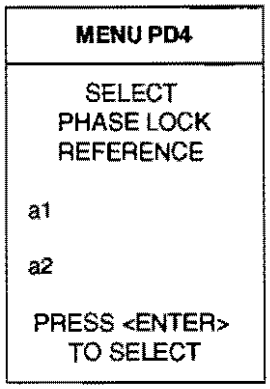
Step 2. Select **CHANGE NUMERATOR** and press ENTER. This brings menu PD2 (left) to the screen.

Step 3. Choose the numerator of the parameter by selecting **b1**, **b2**, **a1**, **a2**, or **1 (UNITY)** as appropriate for the measurement. Note that the nomenclature of the signals applied to the 363XA test set in the following way:

- b1 is the signal applied at T_A
- b2 is the signal applied at T_B
- a1 is the signal applied at R_A/SOURCE LOCK INPUT
- a2 is the signal applied at R_B/SOURCE LOCK INPUT



The denominator of the definition of the measured parameter can be changed. Select **CHANGE DENOMINATOR** in menu SP (page A-11). This calls-up menu PD3 (left). Then, using the method given in Step 3, choose the denominator appropriate for the testing requirements.



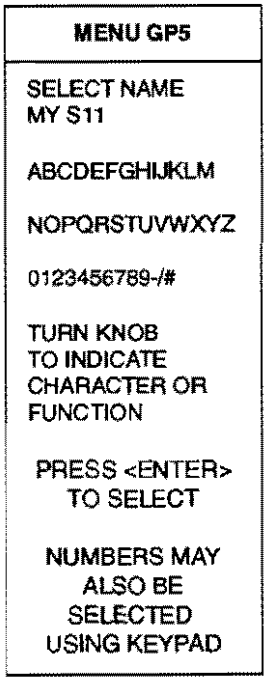
Change Phase Lock

The phase lock reference for a measurement can be selected as a1 or a2; these correspond to the R_A/SOURCE LOCK INPUT and the R_B/SOURCE LOCK INPUT respectively.

Change the phase lock reference as follows:

Step 1. With menu SP displayed (page A-11), move the cursor to **PHASE LOCK** then press ENTER. This brings menu PD4 to the screen.

Step 2. Select **a1** or **a2** as appropriate for the testing requirements.



Change Label

The redefined parameter can be given a suitable name or label. This will appear on the screen you use to name the measured parameter.

Create a label for the redefined parameter as follows:

Step 1. With menu SP displayed (page A-11), move the cursor to **CHANGE LABEL** then press ENTER. This brings menu GP5 to the screen.

Step 2. Create a name for the measurement parameter by selecting a series of up to five alphanumeric characters from among those provided on this menu. Use the control knob to move the cursor to the first alphanumeric to be used in the intended name. Press ENTER to select character and note that it appears in the first blank space below **SELECT NAME** at the top of the menu.

Step 3. Repeat step 2 and choose up to five characters. If an error is made, select **DEL** to delete character or select **CLEAR** to clear name.

Step 4. When the name is complete, select **DONE.**

Dual Source Control

Applications for the 363XA test set such as mixer measurement systems using external mixers require control of two sources and receiver. This is accomplished using the Dual Source Control option which is covered in the Model 360B Vector Network Analyzer System Operator Manual.

Appendix B
360ACM
Auxiliary Control Module
Maintenance Information

Table of Contents

Appendix B
360ACM
Auxiliary Control Module
Maintenance Information

B-1 INTRODUCTION

The 360ACM Auxiliary Control Module (360ACM or, ACM) is a system auxiliary unit that supplies +5V (or –5V), +6V, +8V and +15V (or –15V) power supply voltages to the 3635B Test Set.

B-2 REPLACEABLE SUBASSEMBLIES

WILTRON maintains a module exchange program for selected signal source modules. If a malfunction occurs in one of these modules, it can be exchanged. Upon request and typically within 24 hours, WILTRON or a Wiltron/Anritsu Service Center will ship an exchange module. The customer has 30 days in which to return the defective item. All exchange parts are warranted for 90 days from the date of shipment or for the balance of the original-part warranty—whichever is longer. A listing of exchangeable subassemblies is provided in Chapter 1, Table 1-2.

B-3 INSTALLATION

To install the 360ACM into the system, proceed as follows:

CAUTION

If the 360ACM Line Module Assembly is incorrect for the line voltage used, operation may result in damage to the 360ACM.

Step 1. Verify that the 360ACM Line Module Assembly (rear panel) is set for the correct line voltage (Figure B-1).

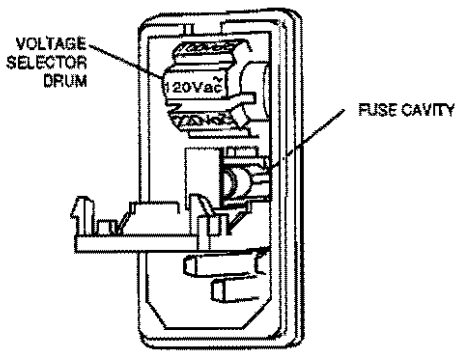
Step 2. Prepare the system console to position the 360ACM in the desired location. The preferred location is at the bottom of the system console.

Step 3. Fasten the 360ACM into the location prepared in step 2 above with the mounting hardware provided.

Step 4. Connect the auxiliary dc power cable from the rear panel of the ACM to the rear panel POWER DIST SUPPLY connector of the 3635B Test Set.

Step 5. Connect the power cable to the ACM Line Module Assembly and to the system console power strip.

LINE VOLTAGE SELECTOR MODULE



To change the line voltage from that shown on the Line Voltage Module selector drum, proceed as follows:

Step 1. Remove the power cord from the line voltage module.

Step 2. Insert the blade of a small screwdriver into the slot at the top-center of the module, and pry open the cover.

Step 3. Remove the voltage selector drum by pulling straight out.

Step 4. Rotate the drum so that the desired line voltage marking faces out, then reinstall the drum.

Step 5. Remove the fuse cartridge from the right-hand fuseholder. The fuse cartridge is identified with a white arrow and is located beneath the voltage selector drum.

Step 6. Check that the proper fuse is installed (see table).

Step 7. Change to the correct fuse, if necessary, and replace the fuse cartridge.

Step 8. Close the cover, and ensure that the desired line voltage value is displayed through the opening in the cover.

Step 9. Reinstall the line cord.

Figure B-1. *Setting the Line Voltage*

B-4 FUNCTIONAL OVERVIEW

Figures B-2 thru B-4 show the location and the interconnection of the major assemblies that comprise the 360ACM. The major assemblies are:

- 12V Power Supply Assembly,
- 15V Power Supply Assembly,
- A100 Auxiliary Control Module PCB Assembly,
- Line Module Assembly,
- Power Transformer,
- Duplex Outlet Assembly,
- Rear Panel Connector/Cable Assemblies.

The A100 Auxiliary Control Module PCB Assembly contains power-on logic relays (K1 and K2), voltage regulators (VR1 – VR4), a 12V time delay circuit (Q1, Q2), and fuses for the power supply assemblies (F1 – F4). This assembly routes primary power from the Line Module Assembly to the 12V and 15V power supply assemblies via relay K1 and fuses F1–F4.

Transistors Q1 and Q2 comprise a time delay circuit that delays the output of the 12V power supply assembly approximately one-half second at turn-on. The output of Q1 is applied to the inputs of voltage regulators VR1 and VR2.

Voltage regulators VR1 and VR2 output 6V and 8V, respectively. Voltage Regulator VR4 converts the output of the 15V power supply assembly to 5V. All of these voltages are routed via connector J8 to the rear panel 15 pin "D" connector, which is the main interface to the 360VNA test set.

Voltage Regulator VR3 converts the output of the 12V power supply assembly to 5V; this second 5V power source is used to light the front panel POWER indicator LED. It is also routed to the rear panel BNO connector (via connector J7) and is the RP BNC SIG voltage fed to the 3642A Noise Figure Module (used only with 360NF20A Noise Figure Systems). This voltage is used by the 3642A for amplifier biasing.

B-5 PREVENTIVE MAINTENANCE

There are no 360ACM components that require preventive maintenance.

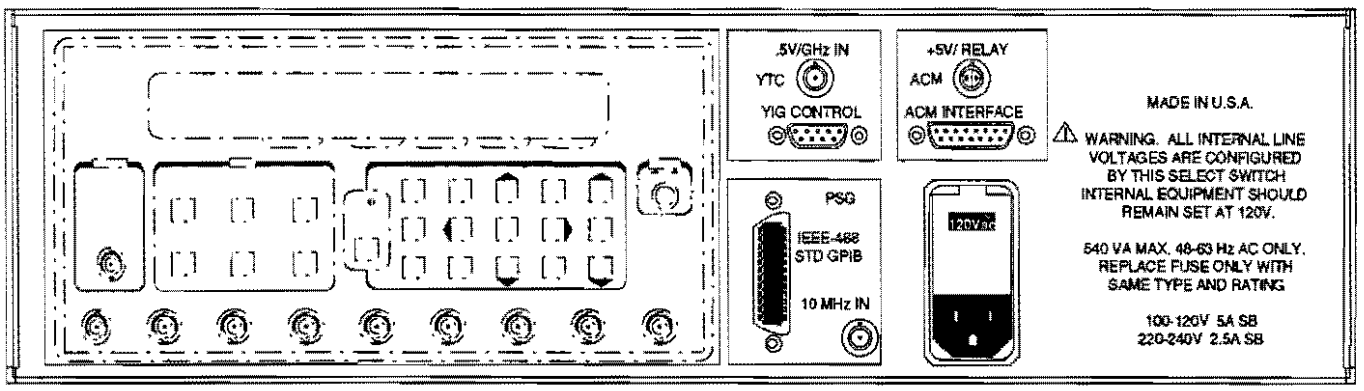


Figure B-2. 360 ACM Rear Panel

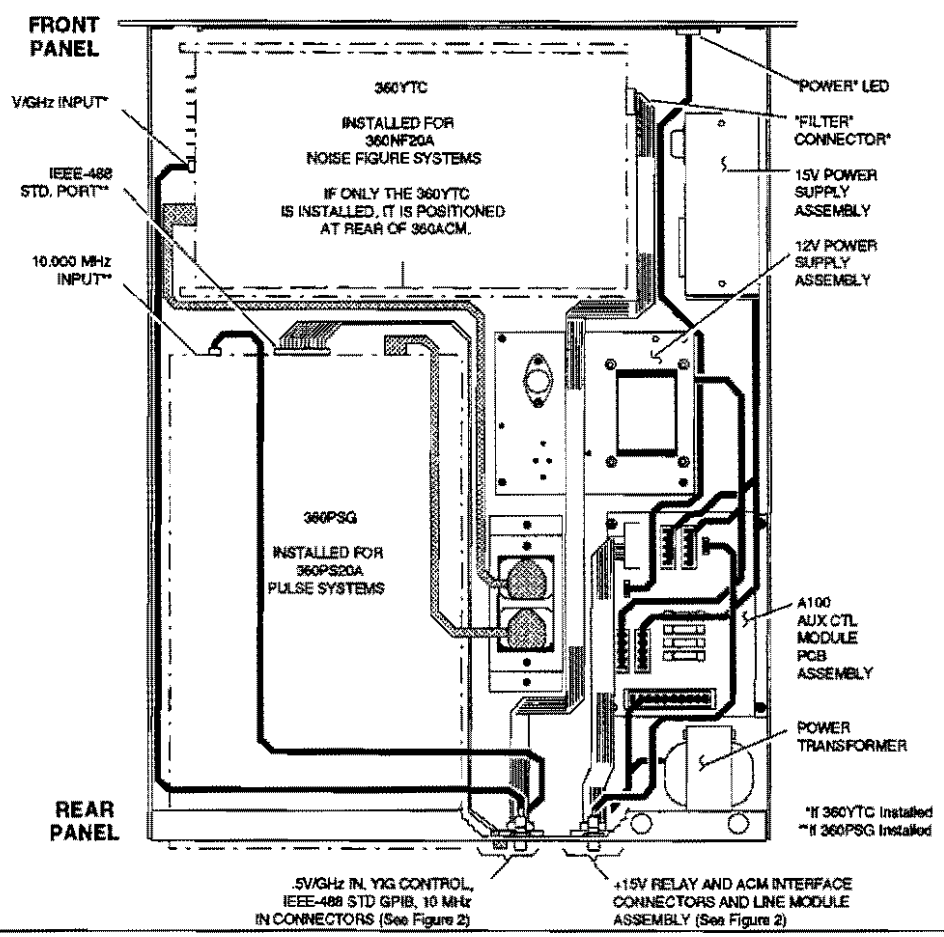


Figure B-3. Parts Locations

B-6 TROUBLESHOOTING PROCEDURES

Field troubleshooting and repair is limited to replacement of defective power supply modules and replacement of voltage regulators and fuses located on the A100 auxiliary control module PCB assembly. All major 360ACM assemblies (including the entire A100 Auxiliary Control Module PCB assembly) may also be replaced, as required.

To troubleshoot, proceed as follows:

Step 1. Remove power from the system.

Step 2. Unfasten screws securing 360ACM front panel to system console and slide unit out of system console.

Step 3. Remove the screws securing the top cover and remove cover.

Step 4. Remove the four screws securing the A100 auxiliary control module PCB protective cover and remove cover.

WARNING

Voltages hazardous to life are exposed when operating the 360ACM with the A100 auxiliary control module PCB protective cover removed. Use extreme caution when operating in this manner.

Step 5. Apply power to the system in normal manner. Measure the voltages listed in Table B-1. Note that the voltage at TP6 is the output voltage of the 15V power supply assembly and that TP8 is the output voltage of the 12V power supply assembly (after time-delay circuit).

Step 6. If there are no dc voltages present at the test points, *carefully* determine if line voltage is present between fuses F1 and F2 and between F3 and F4 of the A100 PCB. If line voltage is not present, disconnect power cord and check the Line Module Assembly fuse (Figure B-4).

WARNING

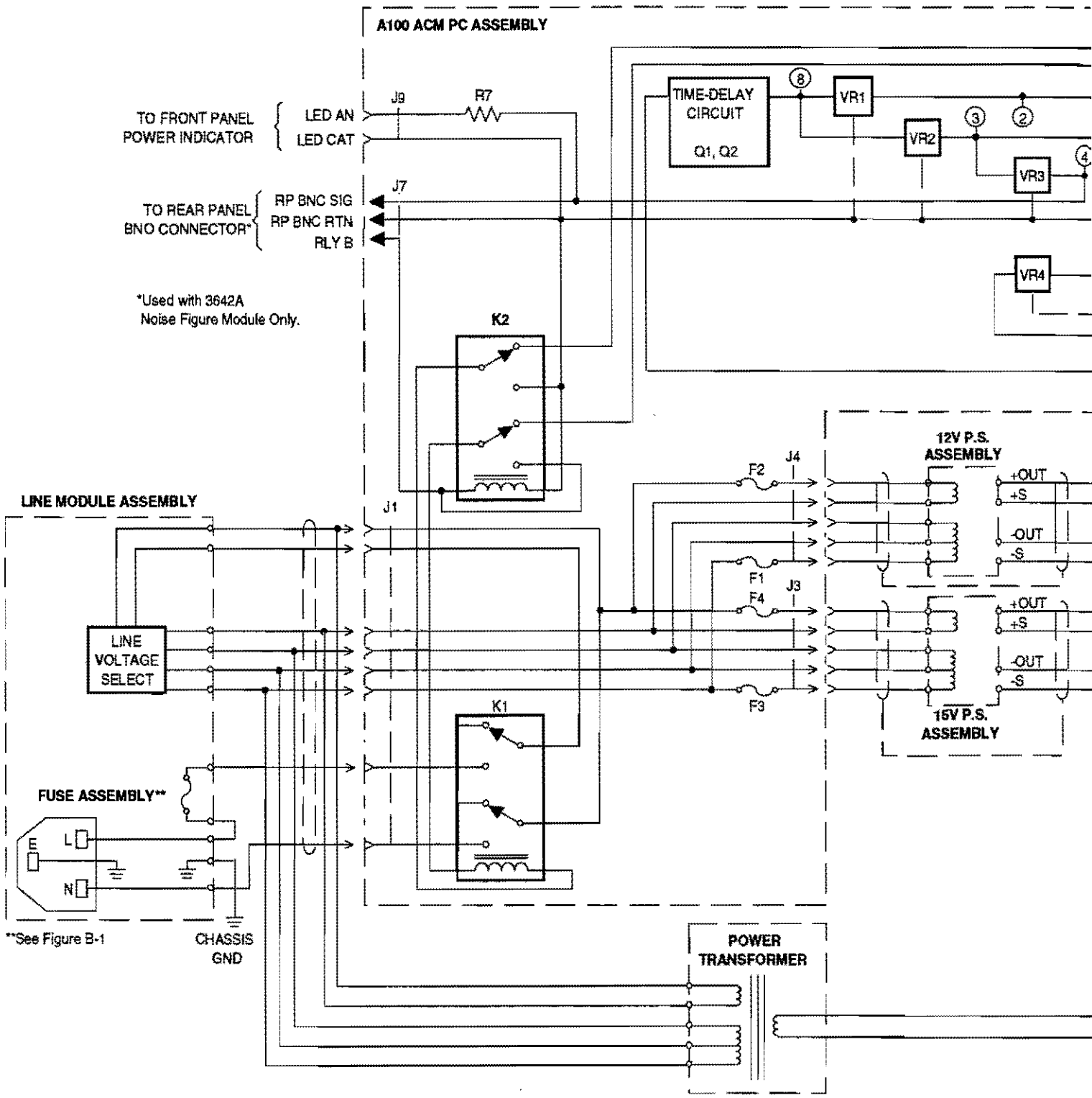
Line voltages hazardous to life are normally present on these fuses. Voltages up to 240 Vac may be present.

Step 7. If Line Module Assembly fuse is OK, re-apply line voltage to the 360ACM and carefully measure the dc voltage across the coil of relay K1 (measure across CR1). This voltage is supplied by the test set and should measure 5V ± 0.3Vdc. If voltage is OK, K1 is defective.

Table B-1. *Test Point Voltages*

Test Point	Measured Voltage (Vdc)*	Reference Point
TP2	6.0 ± 0.2	TP 1
TP3	8.0 ± 0.2	TP 1
TP4	5.0 ± 0.2	TP 1
TP5	5.0 ± 0.2	TP 1
TP6	15.0 ± 0.3	TP 1
TP8	11.5 ± 0.3	TP 1

* Measure voltages with a voltmeter having ungrounded, floating inputs.


A100 ACM PC ASSEMBLY
TO FRONT PANEL POWER INDICATOR
LED AN
LED CAT
J9
R7
TIME-DELAY CIRCUIT
Q1, Q2
VR1
VR2
VR3
VR4
TO REAR PANEL BNO CONNECTOR*
RP BNC SIG
RP BNC RTN
RLY B
J7
*Used with 3642A Noise Figure Module Only.
K2
K1
LINE MODULE ASSEMBLY
J1
LINE VOLTAGE SELECT
FUSE ASSEMBLY**
E
L
N
**See Figure B-1
CHASSIS GND
F1
F2
F3
F4
J3
J4
12V P.S. ASSEMBLY
15V P.S. ASSEMBLY
+OUT
+S
-OUT
-S
POWER TRANSFORMER

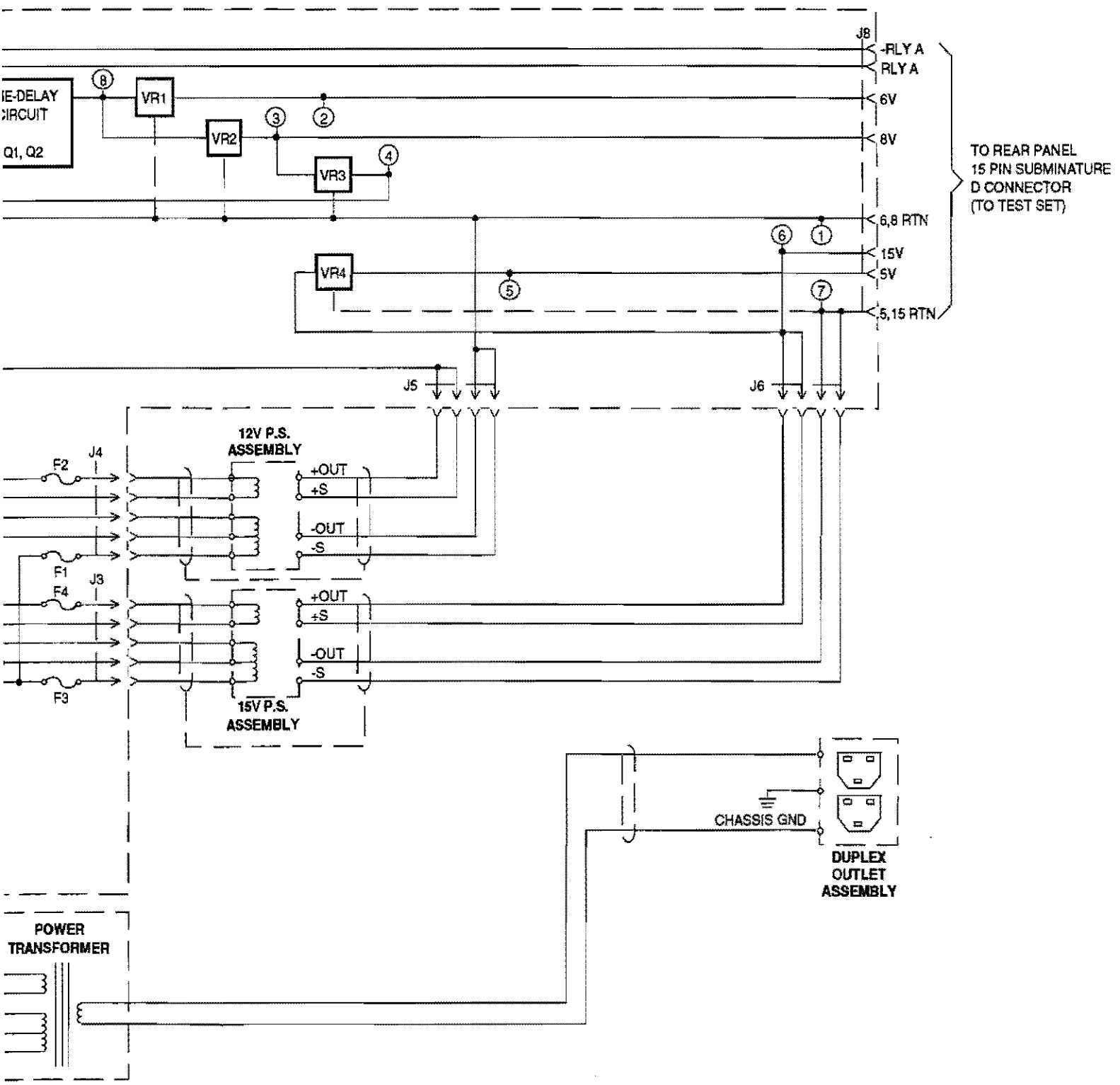


Figure B-4. *Interconnection Diagram*

Step 8. If line voltage is present, check that fuses F1–F4 are not open (that is, no voltage drop across each fuse). If the fuses are OK and there is no dc output (or incorrect output) from either power supply assembly, replace the suspected assembly.

If there are dc voltages present at the test points, but they are the wrong value, determine which voltage regulator or power supply module output(s) are at fault. Before replacing a suspected voltage regulator, determine that excessive current is not being drawn by the test set (i.e, overheating cables, shorted cables, overheating test set components, etc).

If the +5V is OK at TP4, but the front panel POWER LED is not lit, check for defective cable connection at A100(J9), or defective cable, or defective LED.

B-7 SPECIFICATIONS

Specifications for the 360 ACM are stated below.

Power-Requirements	W/O 360PSG or 360YTC: 100/120/220/240V, 60/50 Hz, 190 VA max
	With 360PSG or 360YTC: 100/120/220/240V, 60/50 Hz, 540 VA max
Dimensions:	133H x 432W x 603D mm (5.25H x 17W x 23.75D in.)
Weight (W/O 360PSG or 360YTC):	Approx 10.9 kg (24 lb.)

Subject Index

0 – 9

A

B

C

D

E

F

G

H

I

M

N

O

P

R

S

T

U

V

Y