eASIC Technology & Nextreme Architecture

Tomer Kabakov

Director of Sales

tomer@easic.com

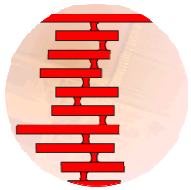
Tel: 054-4304032

eASIC at a Glance

- Fabless Semiconductor Company
- Provider of Structured ASIC Products
- Founded in 1999
- Headquarters in Santa Clara, California
- R&D facilities in Romania and Malaysia
- Worldwide sales and design support teams
- Shipping chips to customers and generating revenues
- Private company, funded by venture capital firms and private investors (including: Vinod Khosla, Kleiner Perkins Caufield and Byers (KPCB), Crescendo Ventures, and Evergreen Partners)

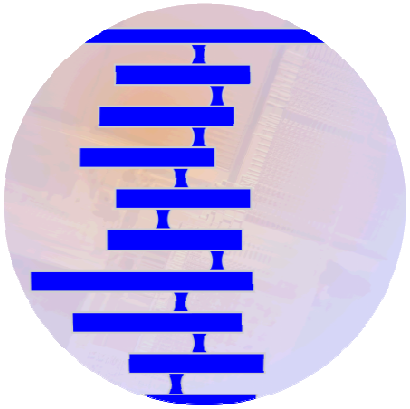
The eASIC Advantage – Affordable Customization

ASIC



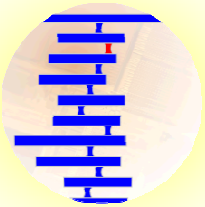
~40 unique layers
Large upfront cost ($25M)
18 month design cycle
48% probability of respin
12 week turn-around
Expensive design tools

FPGA



No unique layers
High power
High unit cost

eASIC



One unique layer

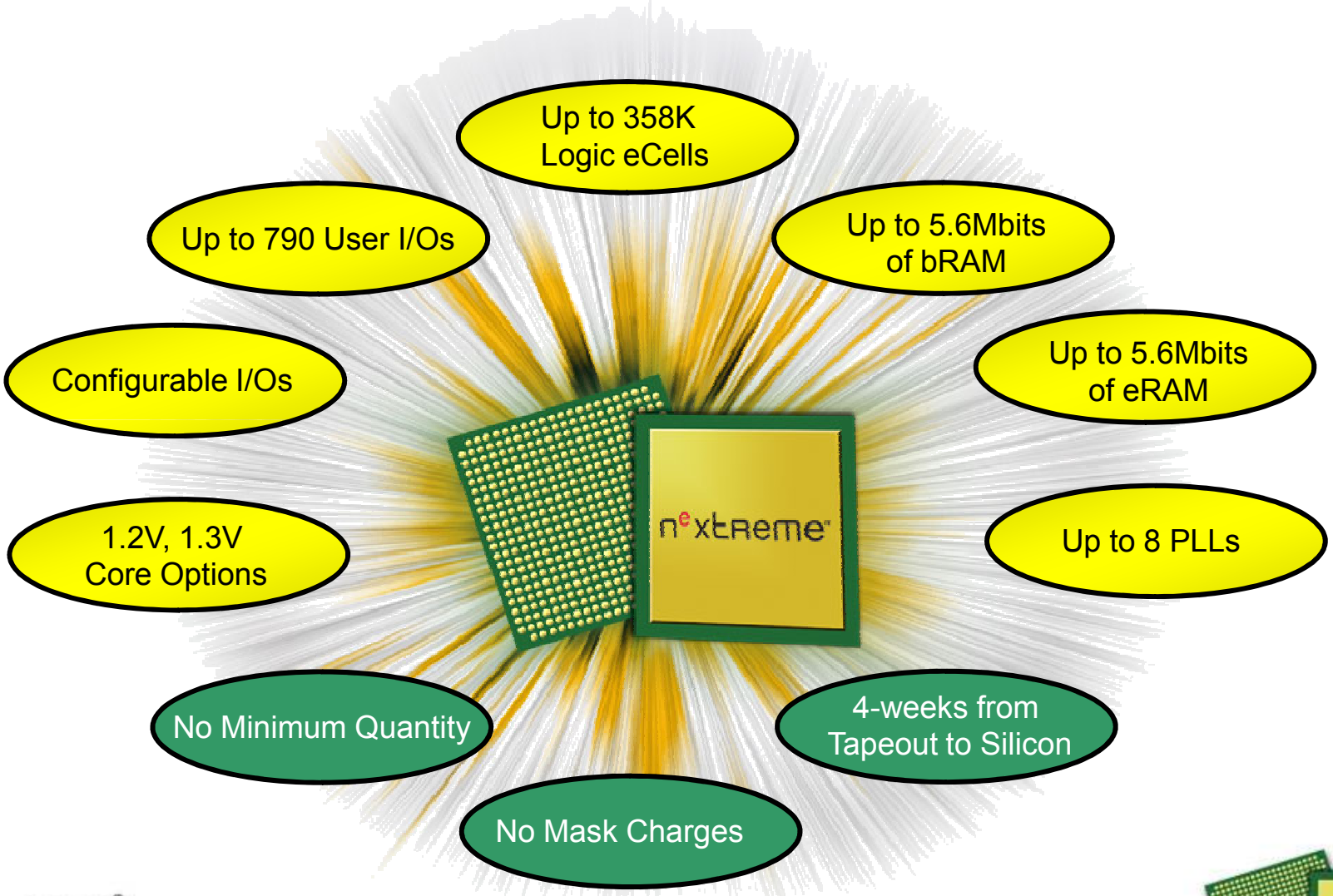
The eASIC Advantage

Small upfront costs ($K)
2 month design cycle
Low respin probability
4 week turn-around
Low tools cost

Ability to differentiate
Create multiple derivatives

Up to 20% of the power
Up to 40% of the cost

Nextreme Structured ASIC Introduction



Nextreme Design Win Sample

Cell phone Projector

Security

Video Surveillance

Broadcast Camera

NVR/DVR

Wireless Basestations

Military Communications

Multi-computing

Image Processing

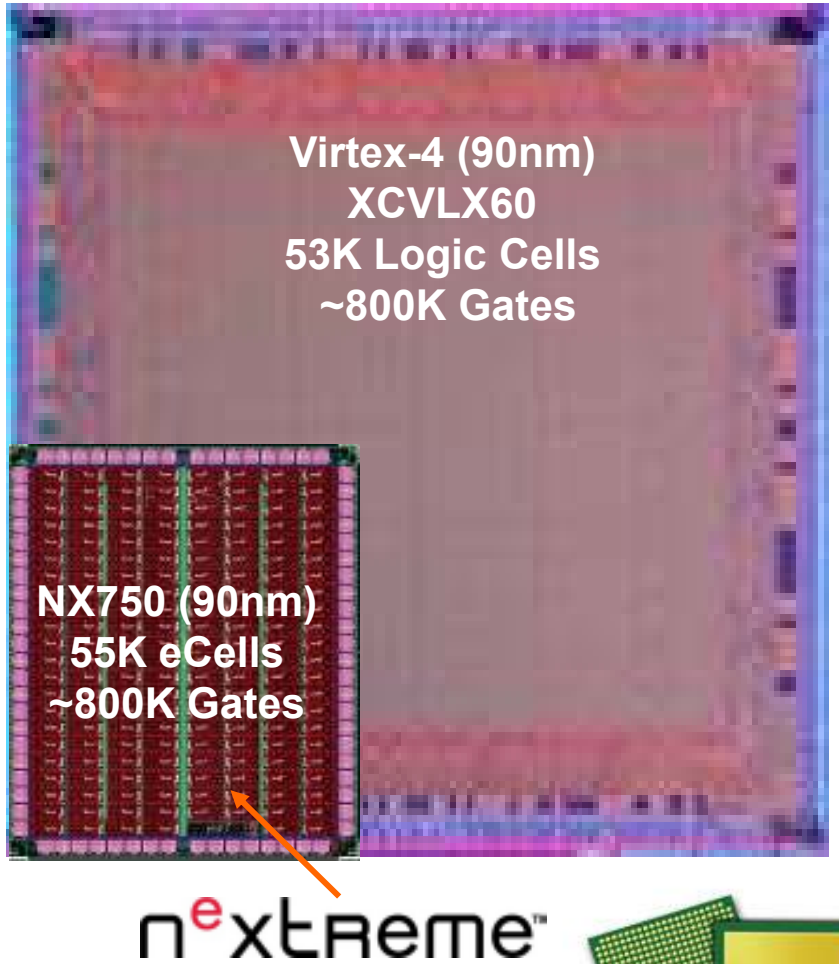
Instrumentation

Gateways

At Last an ASIC Alternative to FPGA

- Can you give up multiple times electrically re-programmable for:
  - A chip that is 10% to 60% the unit price of an FPGA
  - 10% the power of an FPGA
  - Up to 4x performance improvement over an FPGA
- How? - Late stage via and bit stream structured ASIC

Drawn to Scale



nextreme

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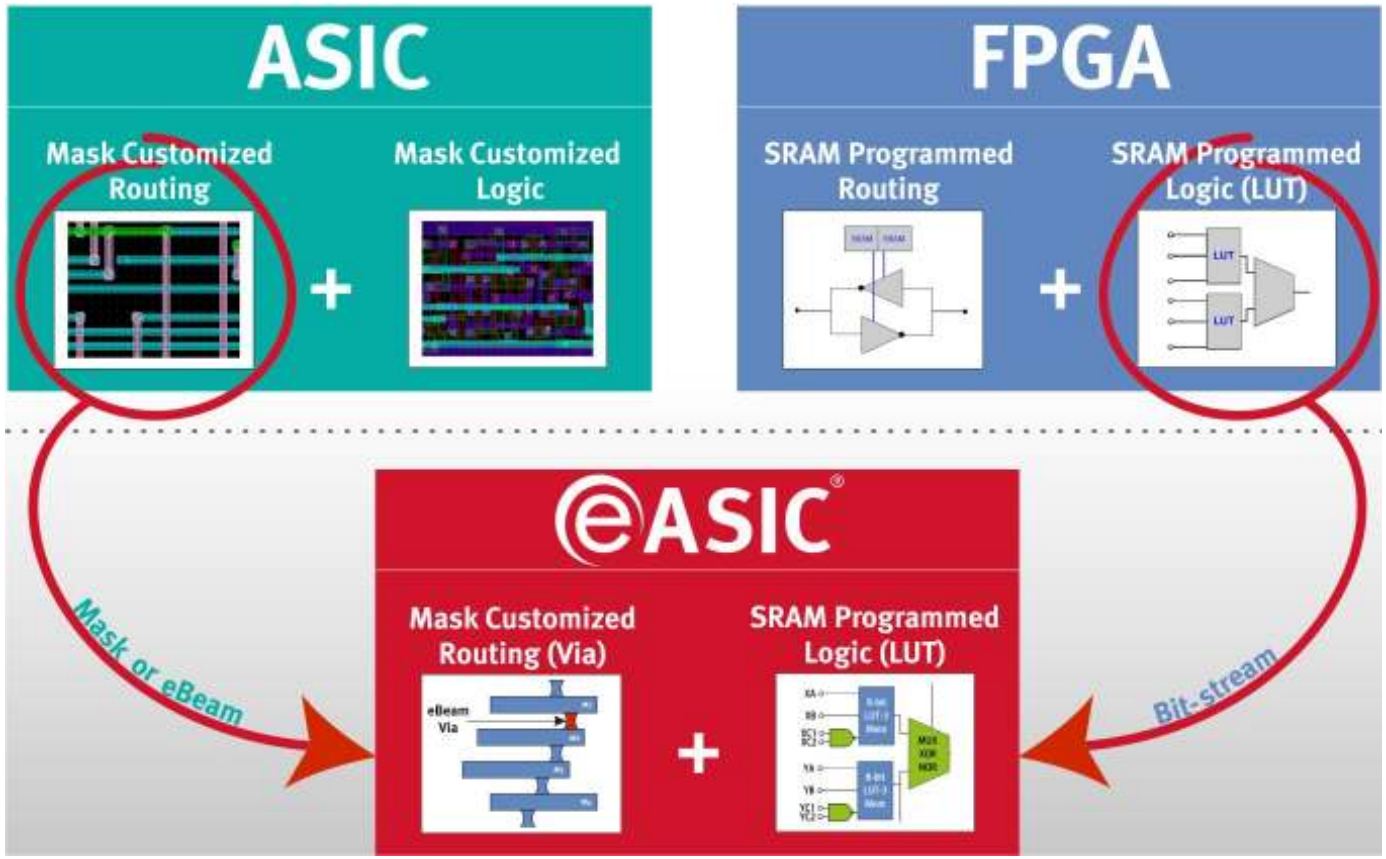
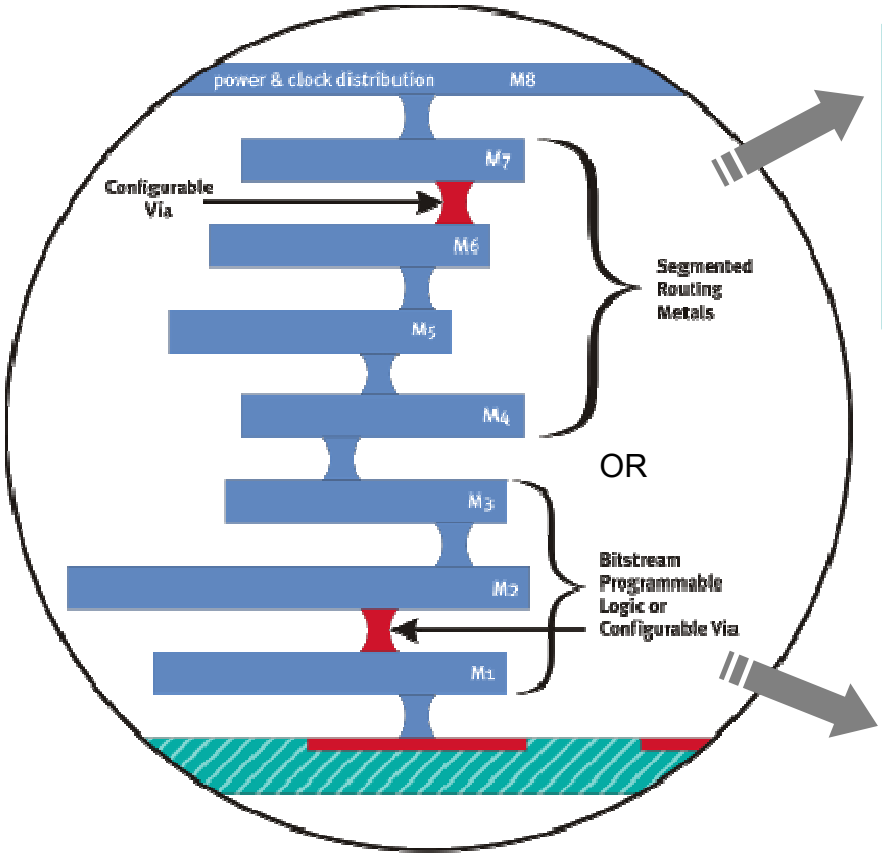
Nextreme: Disruptive Technology



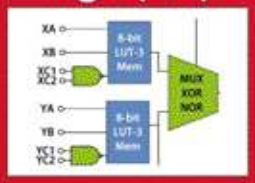
eASIC's "Divide and Conquer" customization method:
Logic is customized with Bit-stream or with single Via-mask
Routing is customized with single Via-mask or - maskless (eBeam)

Time to Production – Breakthrough



nextreme SL

SRAM Programmed Logic (LUT)



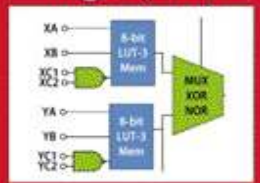
Reprogrammable LUT

Maximum flexibility
Shortest turnaround time

Ideal for prototypes

nextreme VL

Via Programmed Logic (LUT)



Fixed LUT

No external bitstream
Instant On
No inrush current

Ideal for production

Identical Devices – Two Tape-out Options

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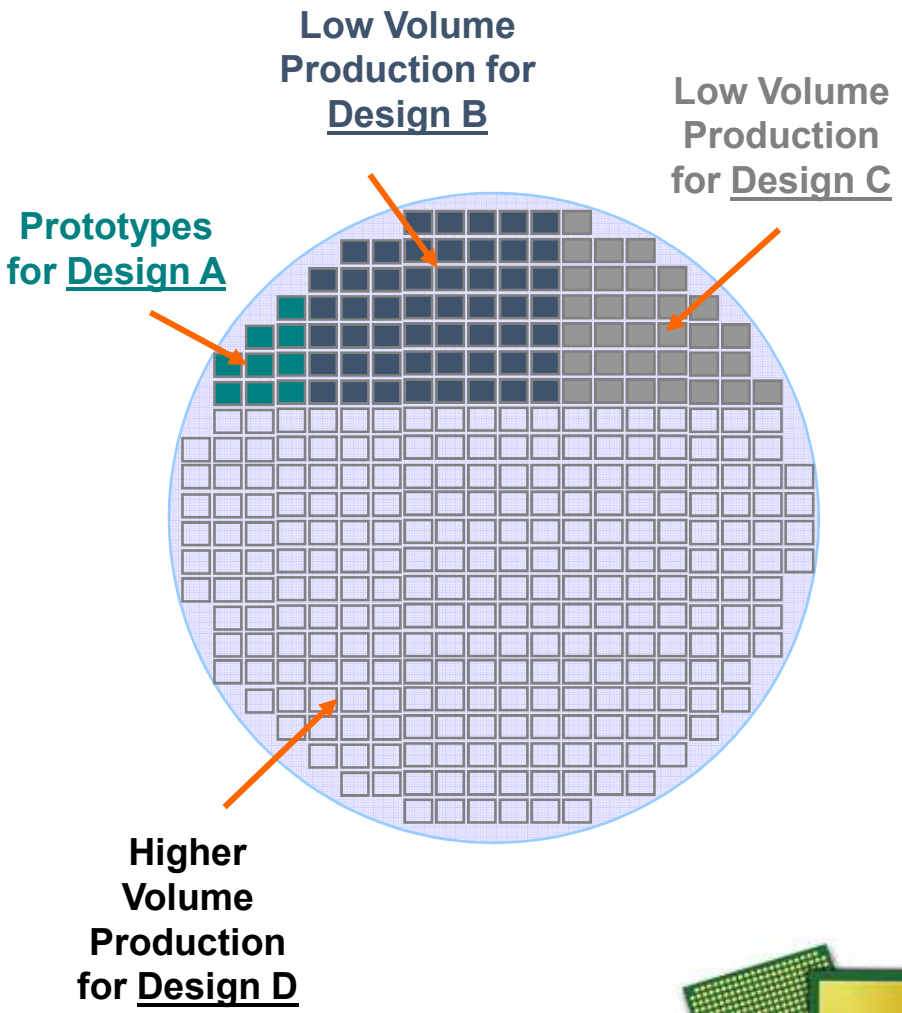
Low Manufacturing Cost and Risk

- No Minimum Order Quantity
- Wafer Sharing
- 4-week Turnaround

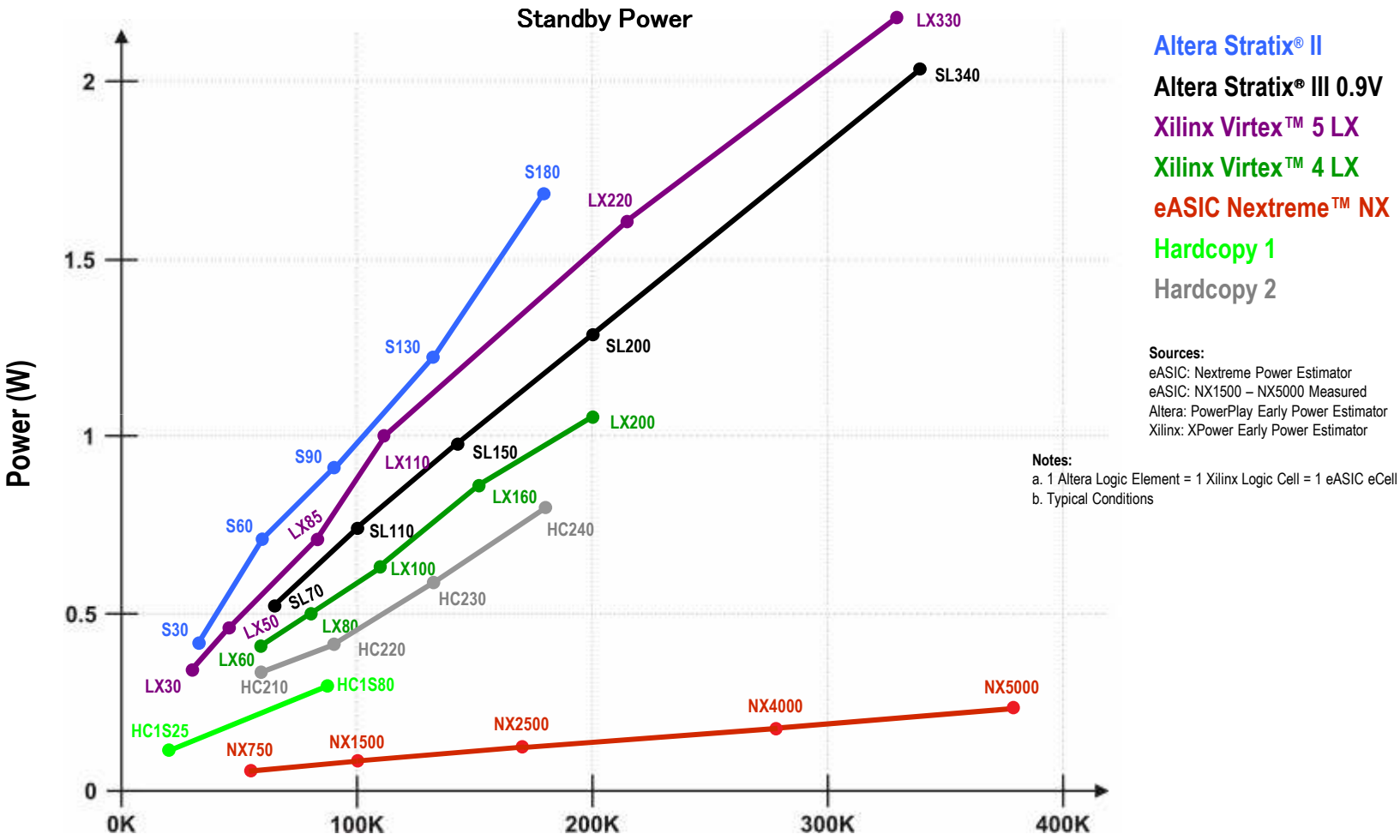


Nextreme Family Details

	Gates*	eCells	Distributed RAM (Max.)		Block RAM		PLLs	Max. User I/O
			eRAM Blocks	eRAM Bits	bRAM Blocks	bRAM Bits		
NX750LP	350,000	26,624	104	416K	13	416K	4	260
NX750	750,000	55,296	216	864K	27	864K	6	310
NX1500	1,500,000	100,352	392	1568K	49	1568K	8	449
NX2500	2,500,000	169,984	664	2656K	83	2656K	10	586
NX4000	4,000,000	276,480	1080	4320K	135	4320K	10	748
NX5000	5,000,000	358,400	1400	5600K	175	5600K	10	790

*** Combination of Logic and Memory**

Static Power Comparison

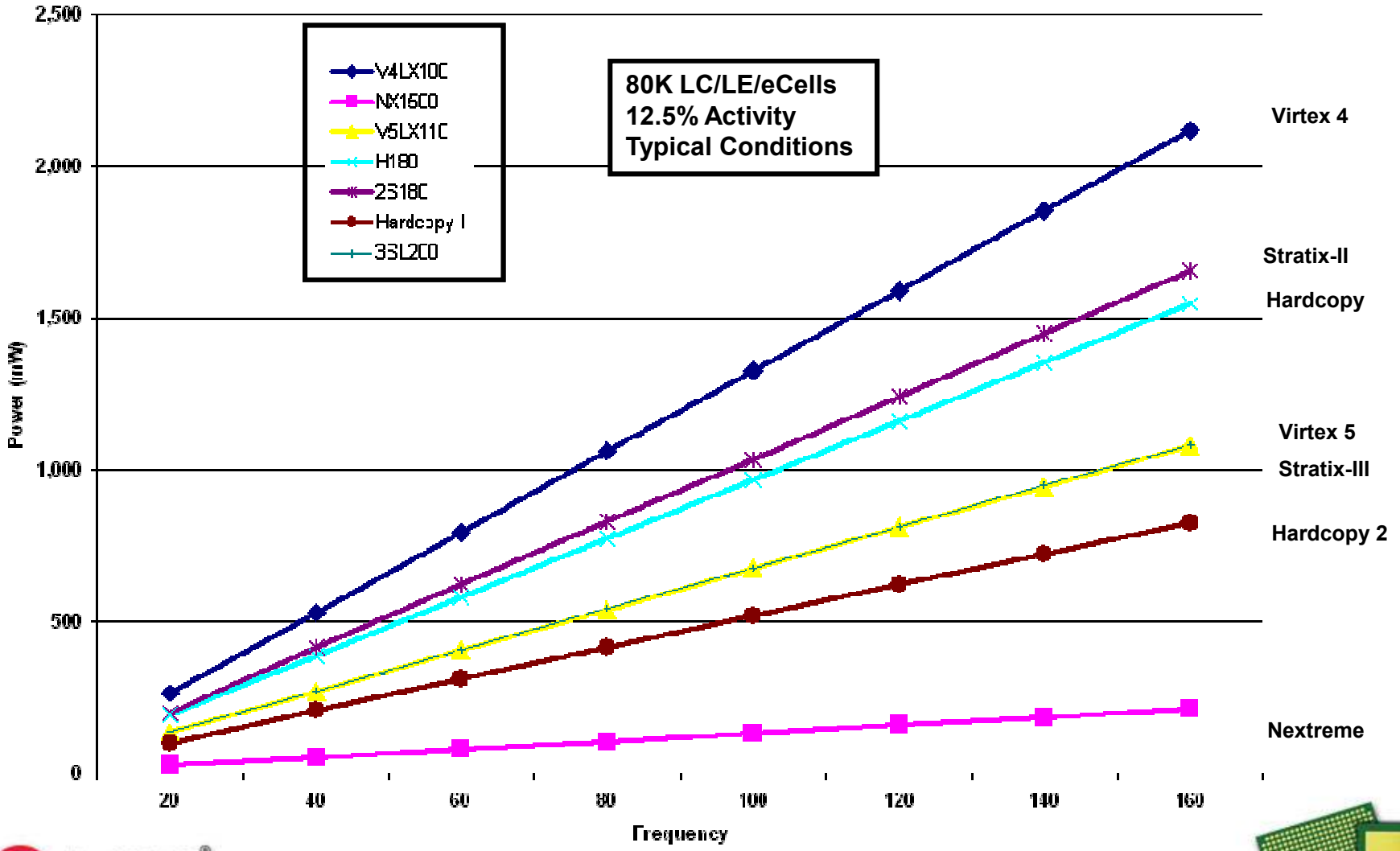


Altera Stratix® II
Altera Stratix® III 0.9V
Xilinx Virtex™ 5 LX
Xilinx Virtex™ 4 LX
eASIC Nextreme™ NX
Hardcopy 1
Hardcopy 2

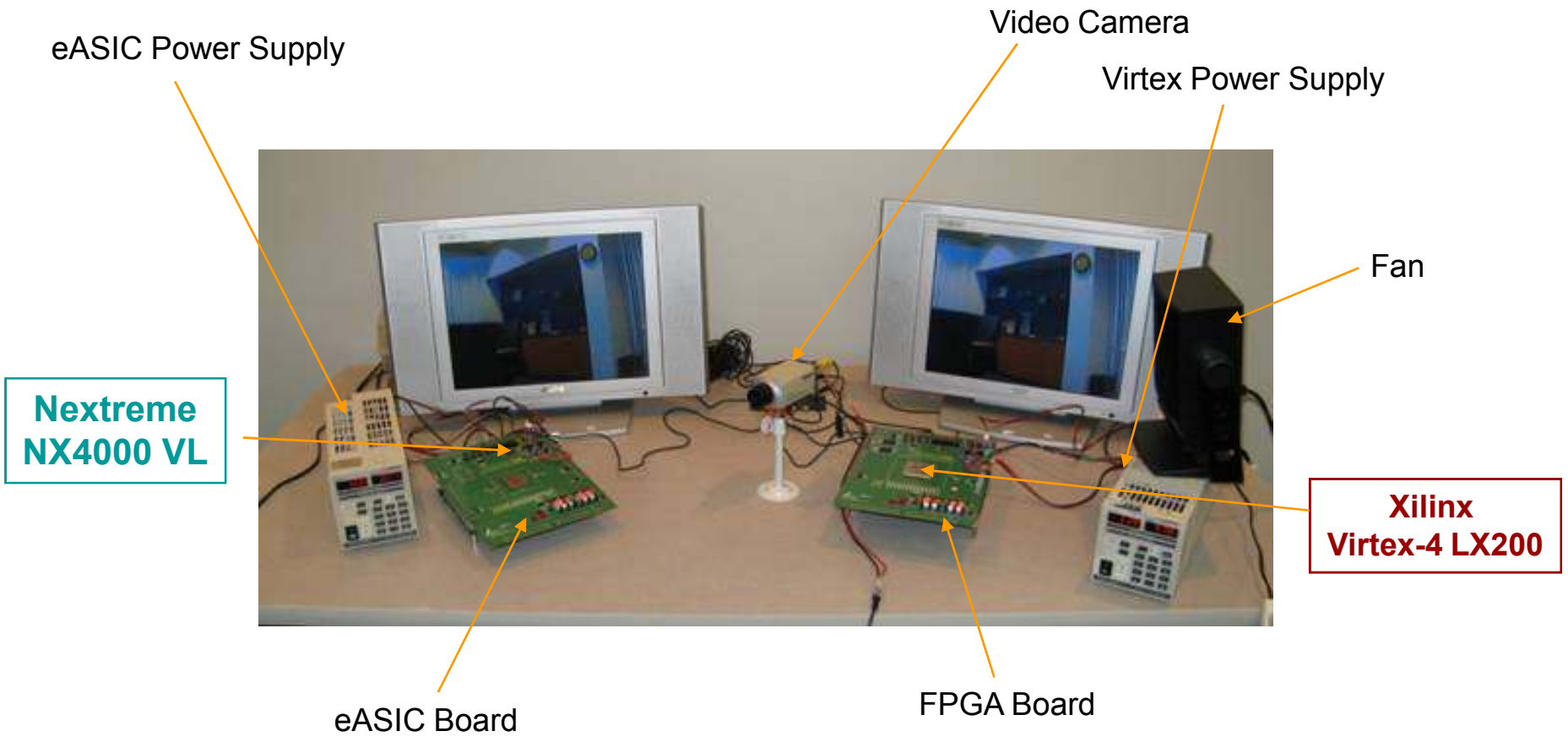
Sources:
eASIC: Nextreme Power Estimator
eASIC: NX1500 – NX5000 Measured
Altera: PowerPlay Early Power Estimator
Xilinx: XPower Early Power Estimator

Notes:
a. 1 Altera Logic Element = 1 Xilinx Logic Cell = 1 eASIC eCell
b. Typical Conditions

Dynamic Power Comparison



Video Processing Power Consumption Bake-off

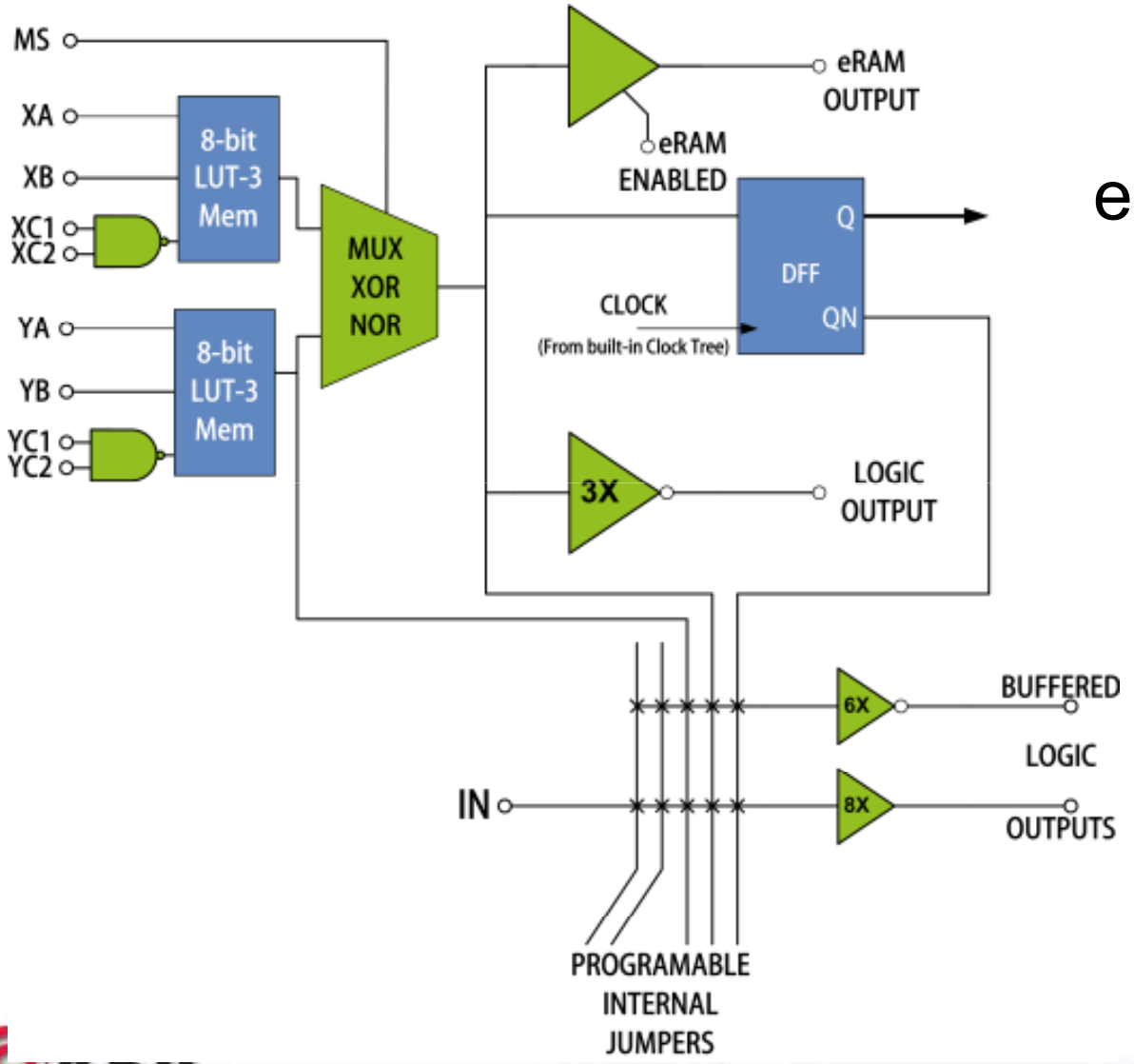


Nextreme – 13X to 15X Lower Power Than FPGAs

	Virtex-4 LX200 FPGA	Nextreme NX4000 VL Structured ASIC	Power Consumption Improvement Using Nextreme
Static Power:			
No Clocks	768 mW	120 mW	**6X**
Total Power:			
RGB Filter (Algorithm 1)	4.8 W	360 mW	**13X**
RGB Filter (Algorithm 2)	5.83 W	420 mW	**14X**
RGB Filter (Algorithm 3)	5.66 W	370 mW	**15X**
RGB Filter (Algorithm 4)	5.72 W	380 mW	**15X**

Nextreme Architecture

Nextreme Technology; eCell

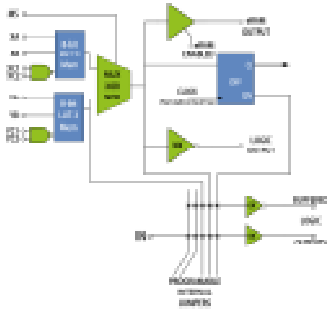


eCell Components

- 2x 3-input LUT
- 2x 2-input NAND
- MUX
- DFF
- Output drivers
- Configuration jumpers

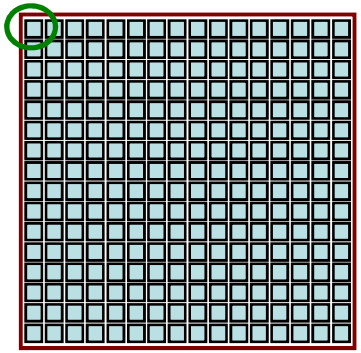
Nextreme Hierarchy - eCore and bRAM

eCell



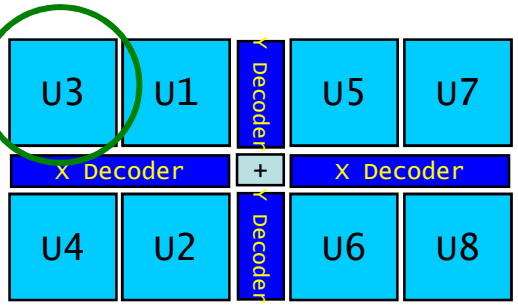
can be configured as logic or 16-bits eRAM

eUnit
(256 eCells)



256 eCells or 4Kb eRAM

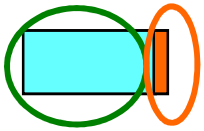
eCore
(8 eUnits)



2048 eCells or 32Kb eRAM

bRAM

32Kbits of bRAM
Configurable as
1K x 32
2K x 16
4K x 8
8K x 4
16K x 2
32K x 1



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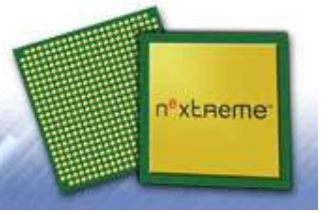
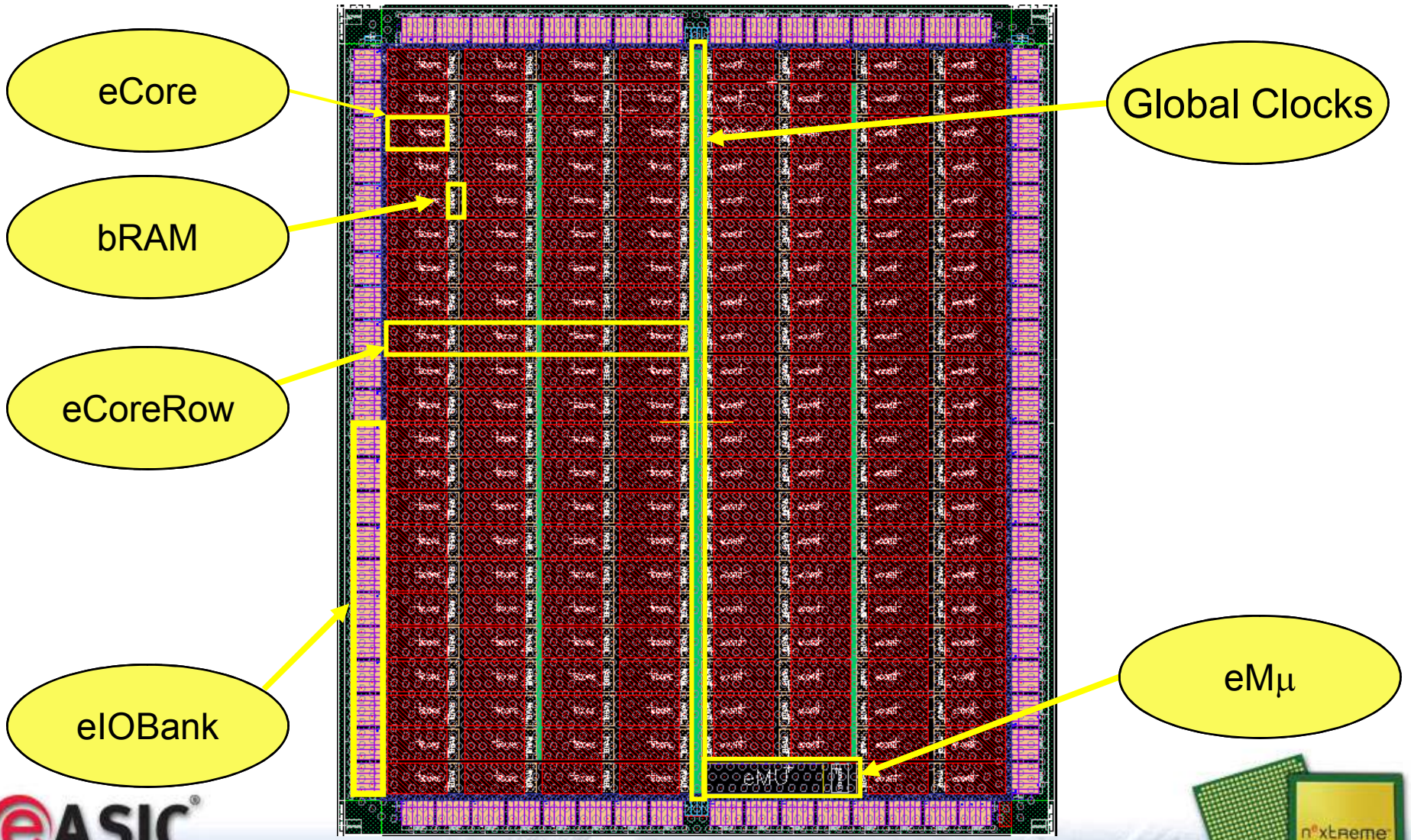


Nextreme Technology; Device Layout



Nextreme Summary

nextreme™
Structured ASIC

Low Development Cost

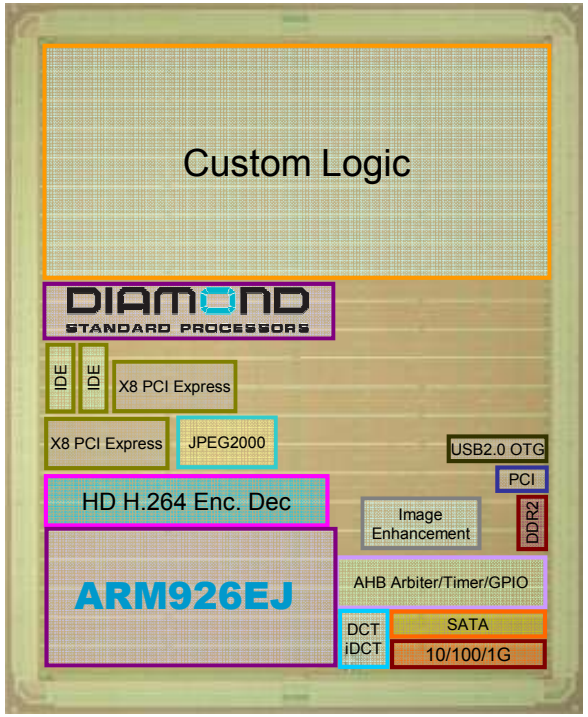
- No Mask Charges
- No MOQ
- Free Diamond Processors
- FPGA like Tool Cost

Low Power

- In battery applications today
- 10-20X lower power than FPGAs

Cost Competitive

- Cell-based ASIC like unit cost



Performance

- HD Encoding in Hardware capabilities
- ARM926 at 175MHz

Rapid Changes/Derivatives

- 2-6 week design turn
- 4 weeks manufacturing
- Rapid software changes using Diamond Processors

Time to Market

- Simple “FPGA like” design flow
- IP library: Diamond Processors, peripherals, interfaces etc.
- Industry standard µP tools/kits

Thank You

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